IMAGER BOARD
Model 800

RasterOps Corporation

0002-0154

March 23, 1990

Revision B1

Introduction

The Imager is a dedicated longword BITBLT-FILL engine optimized for the NuBus. The Imager has 8 modes of operation: FILL-CONSTANT, FILL-PATTERN, PRAM-FILL, BITBLT, INVERT-FILL, INVERT-PATTERN, INVERT-PRAM-FILL, and INVERT-BITBLT. In addition the programmer can enable BUS-LOCKING to prevent other NuBus masters from interrupting an operation.This function combined with automatic Block Transfer enable the Imager to fill data at a peak rate of 9 million pixels-per-second, and blit data at a peak rate of 4.5 million pixels-per second on a fast block mode video board.

The Imager has been designed for maximum performance by minimizing the amount of software overhead required to initiate an operation and by a novel use of a large pixel Cache (SRAM). A flexible architecture has been created which allows any 32 bit address within the Macintosh computer to be accessed for each operation. A programmable translation memory (TRAM) is placed discontinuous data the motherboard to the video board. This function is required for the Macintosh IIci and future machines with non-contiguous main memory. A large pixmap memory (PRAM) is included to allow offscreen pixmaps to reside locally and to be moved at high speed to the video cards.

The Imager can support up to two Block-Mode capable videocards and an unlimited number of non-Block-Mode video cards. The Imager is not limited to just video cards, but can be used with memory cards as well.

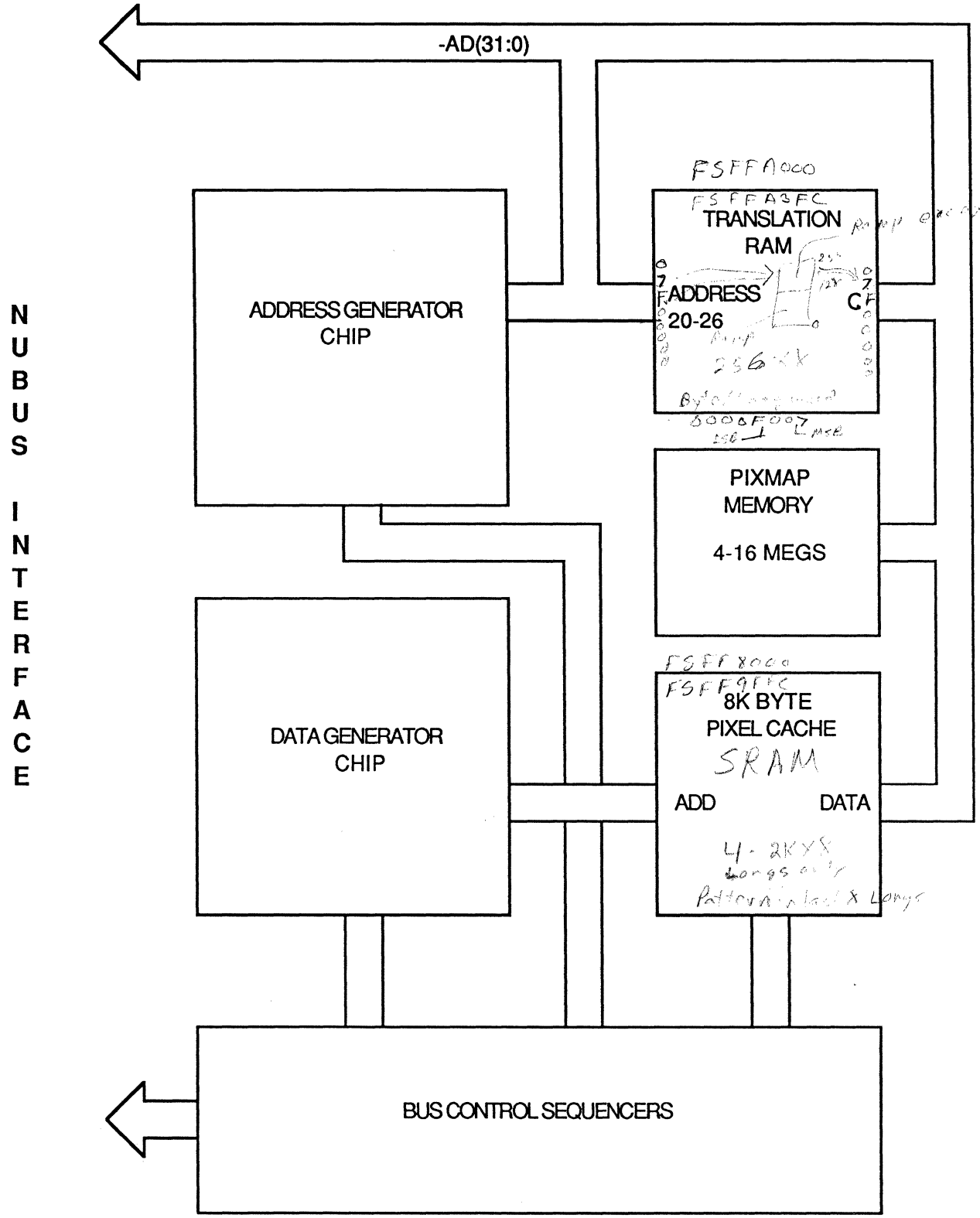
The Imager resides in its own NuBus slot and has a power consumption of 2 Amp.

Reference Documents

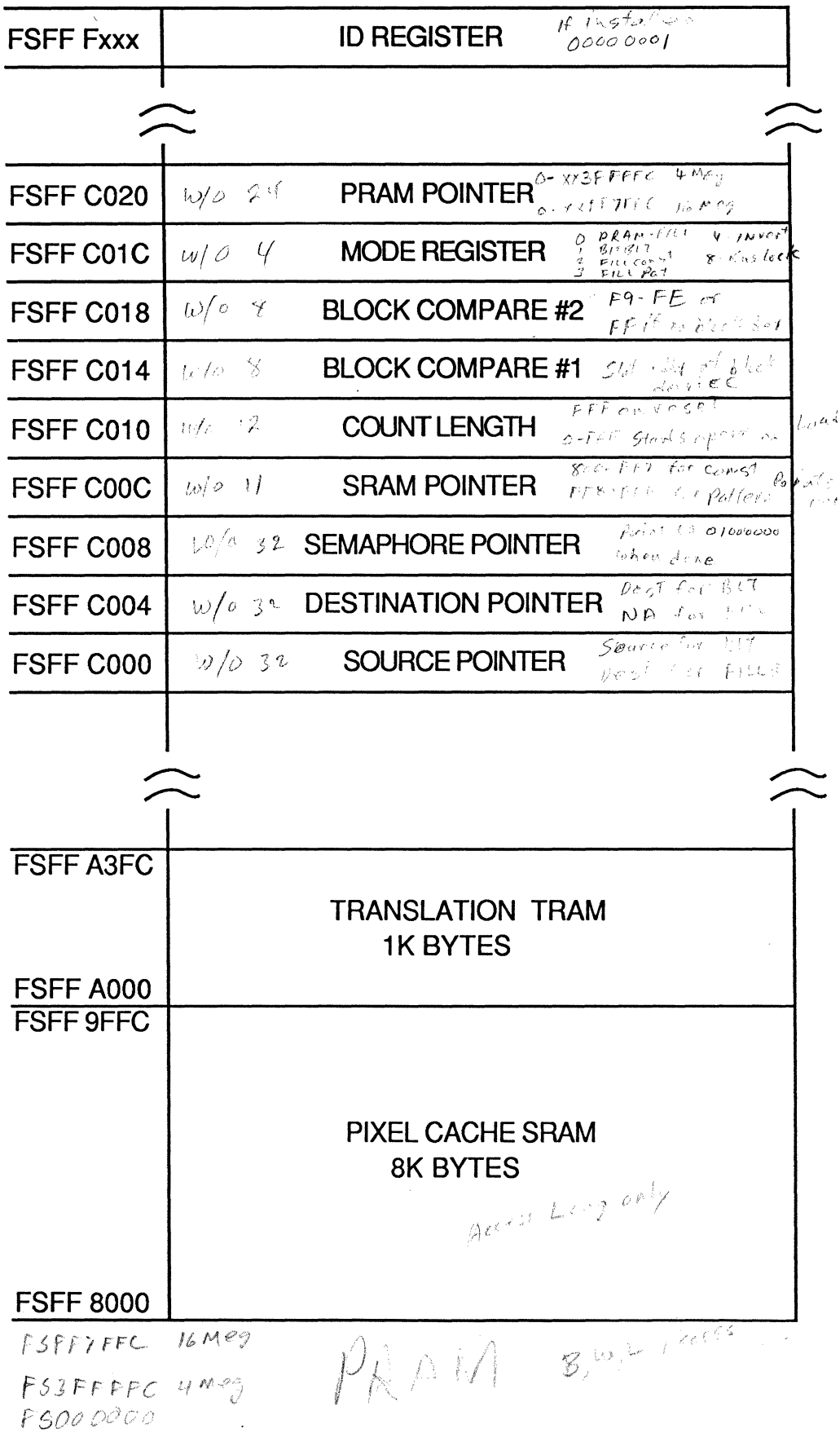
The following is a list of related documents for the Imager product:

Schematic	0002-0149
Assembly Drawing	0002-0150
PC Fab drawing/Artwork	0002-0151
Board List of Materials	0002-0152
Top Assembly LM	800
Manual	0700-0044

Block Diagram



Imager Register Address Map



Pixel Cache SRAM

The Pixel Cache SRAM (SRAM will be used from now on) is comprised of four 2048 x 8-25ns static rams arranged as long words. The SRAM may be written to or read from whenever the Imager is not busy with an operation (FILL, etc.). Locations 0 - 2039 are used for BITBLT and FILL-CONSTANT mode, while locations 2040 - 2047 are dedicated for the 8 pixel pattern used in FILL-PATTERN mode. The SRAM should be loaded with an appropriate fill color or pattern before an operation is started. If the programmer uses locations near the end of the SRAM (ie location 2039) for the fill color and BITBLT operations are shorter than 2039 pixels in length, then the fill color will not be over-written during BITBLT. It is mandatory that the fill pattern be loaded at locations 2040 - 2047.

The SRAM pointer (FSFFC00C) should be set to 0 for BITBLT operations. The SRAM pointer can be set to any location that the programmer desires for FILL-CONSTANT operations. The FILL-PATTERN operation requires that the SRAM pointer be set to a value between 2040 and 2047. Once the SRAM pointer increments to location 2047, the next pointer location will be location 2040. This wrap-around technique is the method used to fill a repeating pattern with an arbitrary offset within the eight pixel pattern. The SRAM pointer is not used in PRAM-FILL operations.

The data from the SRAM which is written to the NuBus may be inverted by setting the INVERT bit in the mode register. This mode should not be selected when reading or writing the SRAM from the motherboard CPU at addresses (FSFF8000 - FSFF9FFC).

Translation Ram (TRAM)

The Translation Ram (TRAM will be used from now on) is comprised of one 256 x 8 -25ns static ram placed between the local 32 bit address bus and the NuBus. The TRAM may be written to or read from whenever the Imager is not busy with an operation. The TRAM is hardwired such that it tranlates seven local address lines, A20 - A26, through the second 128 locations of the table before presenting these addresses to the NuBus. The first 128 entries in the 256 location TRAM are loaded with linear ramps. The linear ramps are used in conjunction with some hardware such that no translation occurs on any address beyond 07FFFFF (The motherboard's Program Ram). On Macintosh products with contiguos Program Ram physical addressing (MacII, IIx, IIcx) the second 128 locations of the TRAM must be loaded with linear ramps also such that no translation occurs on any address.

The TRAM can be loaded from CPU addresses FSFFA000 - FSFFA3FC. The TRAM data lines (D0 - D6) are hardwired to the NuBus Address/Data lines AD20 - AD26. This presents a problem for the programmer because the data bytes are swapped between the NuBus and the motherboard CPU. Because of this, the TRAM data lines D0 - D3 are connected to the CPU data lines D12 - D15. Similarly the TRAM data lines D4 - D6 are connected to the CPU data lines D0 - D2.

The table on the following page is suggested for the first half of the TRAM. This table should also be repeated in the second half of the TRAM when the Imager is used in the MacII, IIx, IIcx.

TRAM Tables

FSFFA000	00000000
FSFFA004	00001000
FSFFA008	00002000
•	•
FSFFA03C	0000F000
FSFFA040	00000001
FSFFA044	00001001
FSFFA048	00002001
•	•
FSFFA07C	0000F001
FSFFA080	00000002
FSFFA084	00001002
FSFFA088	00002002
•	•
FSFFA0BC	0000F002
FSFFA0C0	00000003
FSFFA0C4	00001003
FSFFA0C8	00002003
•	•
FSFFA0FC	0000F003
FSFFA100	00000004
FSFFA104	00001004
FSFFA108	00002004
•	•
FSFFA13C	0000F004
FSFFA140	00000005
FSFFA144	00001005
FSFFA148	00002005
•	•
FSFFA17C	0000F005
FSFFA180	00000006
FSFFA184	00001006
FSFFA188	00002006
•	•
FSFFA1BC	0000F006
FSFFA1C0	00000007
FSFFA1C4	00001007
FSFFA1C8	00002007
•	•
FSFFA1FC	0000F007

TRAM Conversion for Mac IIci

The memory on the Mac IIci is not contigous. The beginning physical address of each of the two sets of four SIMMs (banks A and B) are separated by a 64 megabyte address gap. The MMU inside the 68030 is programmed to make this memory logically contiguous after software has determined how much memory is in each bank. The chart below shows the physical addresses of memory for each of the many memory configurations of the Mac IIci. It would be impractical to create a table like on the previous page for each configuration, but instead, the proggrammer should create an algorithm for the general case and rotate the bits within the word to handle the byte-swapping problem as discussed earlier.

	Bank A Start Address	**Bank B Start Address**
1 Meg System	00000000- 000FFFFF	No Memory
2 Meg System	00000000- 000FFFFF	04000000- 040FFFFF
4 Meg System	00000000- 003FFFFF	No Memory
5 Meg System	00000000- 000FFFFF	04000000- 043FFFFF
8 Meg System	00000000- 003FFFFF	04000000- 043FFFFF
16 Meg System	00000000- 00FFFFFF	No Memory
17 Meg System	00000000- 000FFFFF	04000000- 04FFFFFF
20 Meg System	00000000- 003FFFFF	04000000- 04FFFFFF
32 Meg System	00000000- 00FFFFFF	04000000- 04FFFFFF

It is possible for the Mac IIci to hold up to 128 megabytes of memory when 16 megabyte SIMMs are available. The table above can be extended to reflect this with one restriction: If there are two different sizes of memory used for Bank A than for Bank B, then bank A must contain the smaller SIMMs. This is a restriction recommended by Apple since Bank A is shared with internal video. This forces the largest memory group to be not shared.

Source Register (FSFFC000)

The Source Register is a 32 bit register used by the Imager to determine the source address for the data which will be copied in BITBLT mode, or the address of the data to be filled in FILL, FILL-PATTERN, and PRAM-FILL modes. The 32 bit address is translated through the TRAM to allow the Imager to function in all types of Macintosh platforms.

The Source Register may only be loaded when the Imager is Idle (The Imager is set to idle on reset or after the Semaphore value has been transferred) and before the Count Register is loaded. The Source Register is a wrtite only register.

Destination Register (FSFFC004)

The Destination Register is a 32 bit register used by the Imager to determine the destination address for the data which will be copied in BITBLT mode. The 32 bit address is translated through the TRAM to allow the Imager to function in all types of Macintosh platforms.The Destination Register is not used in either of the fill modes.

The Destination Register may only be loaded when the Imager is Idle (The Imager is set to idle on reset or after the Semaphore value has been transferred) and before the Count Register is loaded. The Destination Register is a wrtite only register.

Semaphore Register (FSFFC008)

The Semaphore Register is a 32 bit register used by the Imager at the end of an operation to point to a location within the motherboard's address space (usually between 0 and 7FFFFFF). The value placed at this pointed to location is hardwired on the Imager to be a 01000000. This value is placed at the ponter location when the Imager has completed an operation. The CPU may access the pointed to location as a long, word, or byte. Like the Source and Destination Register, the Semaphore Register may only be loaded when the Imager is idle.The Semaphore Register on the Imager is a write only register.

SRAM Pointer (FSFFC00C)

The SRAM Pointer is a 11 bit register used by the Imager to select the starting location in the local pixel Cache where data will be stored. Internally a 12 bit counter is used for simplification of the hardware. Because of this, Data bit 11 must always be a Logic 1 so that the pointer address matches the data that has been writen to the SRAM by the CPU. It is required that this pointer be set to 800_h for BITBLT operations. The pointer can be set to any desired location between 800_h and $FF7_h$ for FILL-CONSTANT operations (It is assumed that the foreground color is at this SRAM location). The pointer must be set to any location between $FF8_h$ and FFF_h for FILL-PATTERN operations. The pointer will wrap-around to location $FF8_h$ after the data at location FFF_h has been written.This will continue until the FILL-PATTERN operation has completed. The SRAM Pointer is not used in PRAM-FILL operations. The SRAM Pointer may be loaded when the Imager is idle. The SRAM Pointer is a write only register.

Count Length (FSFFC010)

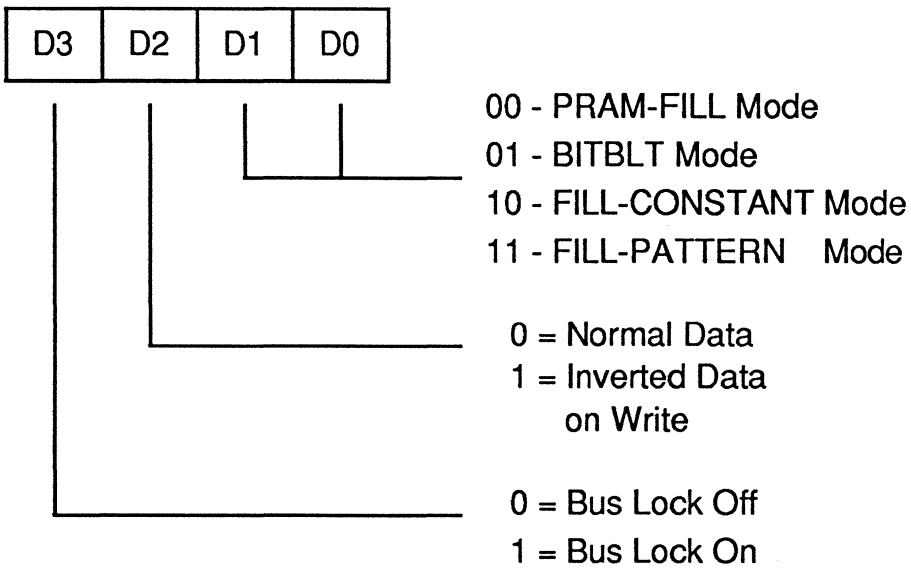
The Count Length register is a 12 bit register used by the Imager to determine the length of the operation to be done. This register is set to FFF_h on reset. Whenever the value in the Count Length is beween 0 and FFE_h the Imager starts an operation. Because of this "auto-starting" mechanism, it is important that the Count Length register be loaded last before an operation. The Count Length register should be loaded with a value of N-1, where N is the number of pixels to be Copied, Filled, etc. The Count Length register is a write only register.

Block Compare#1 (FSFFC014), Block Compare#2 (FSFFC018)

The Block Compare registers are 8 bit registers used by the Imager to determine if the NuBus address pointed to by the Source or Destination Registers is a block capable device. Hardware inside the Imager compares these eight bit registers with the upper byte of the 32 bit addresses from the Source or Destination Registers. It is up to the programmer to determine what NuBus addresses are block capable. One method is by using video board ID numbers. Another method would be to test a video card's block mode readiness by copying known patterns of data from the motherbord RAM to the video card with block mode enabled (Block Compare register matches the video board's address). Then repeat the test with block mode disabled. If the board is block capable, then the data should match. The Block Compare registers must be loaded to FF_h if no block devices are present. The acceptable range of block capable values is $F9_h$ to FE_h. The Block Compare registers are write only and may be loaded when the Imager is idle.

Mode Register (FSFFC01C)

The Mode Register is a 4 bit register used by the Imager to determine the type of operation to be performed. The Mode Register is write only and must be loaded when the Imager is idle. A definition of the individual bits follows:



PRAM Pointer (FSFFC020)

The PRAM Pointer is a 24 bit register used to point to the starting address in PRAM where offscreen data is to be read from during PRAM-FILL operations. The acceptable values for this register are xx000000 - xxFF7FFC for boards with 16 megabytes of PRAM. Values of xx000000 - xx3FFFFC are required for boards with 4 megabytes of PRAM. The PRAM Pointer is write only and may only be loaded when the Imager is idle.

ID Register (FSFFFxxx)

The ID Register is a 32 bit register which can be read by software to determine if the Imager is present in the system. The value of the ID register is 00000001_{hex}.

PRAM Memory Array (FS000000 - FS3FFFFC, 4 Meg) or (FS000000 - FSFF7FFC, 16 Meg)

The PRAM Memory is a large amount of fast dynamic RAM used for holding off-screen pixmaps. This memory can be accessed as bytes, words, or longs. Only 24 of the 32 bits of the memory (3 SIMM's) needs to be populated for 24 bit display boards. If any 32 bit display boards are in the Macintosh computer then all 32 bits of PRAM (4 SIMM's) needs to be populated.