AE6 Hardware External Reference Specification

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Introduction:

The AE6 is a non-intelligent Ethernet adapter for the Apple NuBus personal computer. It makes use of a 3 chip LAN chipset from National Semiconductor Corp. The 3 chips are a Network Interface Controller (NIC), Serial Network Interface (SNI), and a Coax Transceiver Interface (CTI).

This document provides both technical specifications for the adapter card and programatic guidelines specific to the AE6 implementation. The document may be used in conjunction with National's specification document titled DP8390/NS32490 Network Interface Controller (preliminary edition dated July, 1986).

Overview

Resources:

* 16K bytes of RAM
* 32K bytes of ROM
* Apple NuBus interface
* on-board 'Thin Net' transceiver
* multipacket buffering
* 'Thick Net' tranceiver connection

Architecture:

The AE6 is a low cost Ethernet adapter designed to provide the Apple PC to Ethernet connection. It supports back to back packet reception with multi-packet buffering using a 16K byte dual ported local memory. The adapter is structured to allow host access for fault isolation.

Network Interface Controller:

The Network Interface Controller (NIC) performs all Media Access Control (MAC) layer functions for transmission and reception of Ethernet packets. The NIC provides buffer management that supervises storage of received packets to the local memory. During packet transmission, the NIC will insert preamble and sync to the transmitted packet, and optionally compute and append CRC bytes. Upon packet reception, the NIC accomplishes network address decoding and filtering, and performs CRC checking.

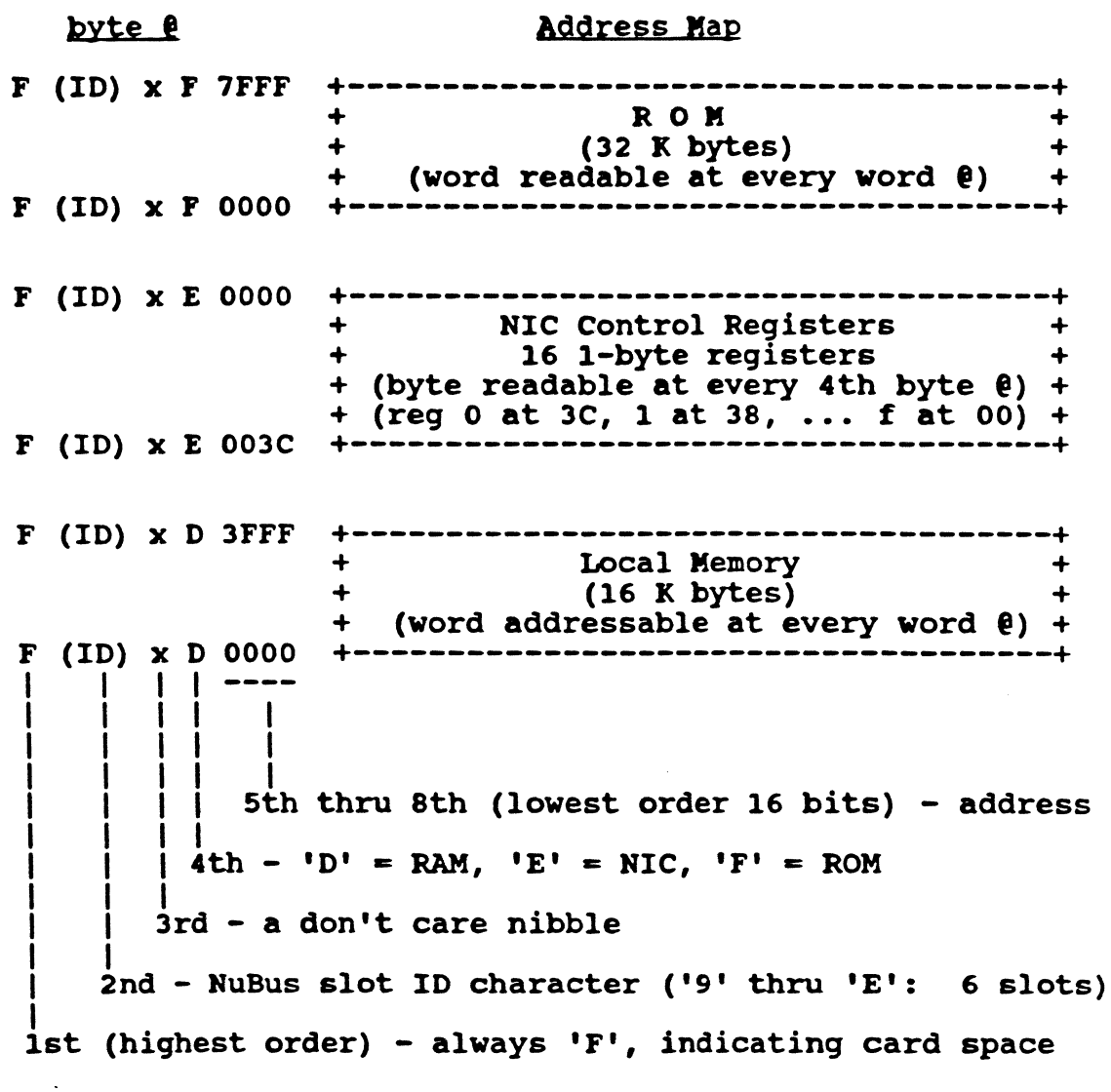
The NIC supports serial data transfers to the SNI and byte parallel register transfers to the host.

Local Memory:

The local memory consists of 16K bytes of static RAM segmented into transmit and receive buffers by setting NIC registers. Each segment is further divided into 256 byte pages. The Transmit Start Register points to the first page in the transmit buffer, and the Page Start and Page Stop registers define the page boundaries of the receive buffer. See National's specification DP8390/NS32490 Network Interface Controller, sections '7.0 Packet Reception' and '8.0 Packet Transmission' for details of buffer initializations, receive ring management, packet header structure, and transmission sequences.

Address Assignments:

The following addresses are to be used in accessing the AE6.



Note that the 8 nibbles (4 bits each) of address are interpreted as above.

NIC Register Addresses:

On the AE6, the NIC's registers are addressed as follows:

Address	RA0-RA3	Page 0 read	Page 0 write
E003C	00h	Command Register	Command Register
E0038	01h	CLDA0	PSTART
E0034	02h	CLDA1	PSTOP
E0030	03h	Boundary	Boundary Register
E002C	04h	Transmit Status	Transmit Page Start
E0028	05h	NCR	TBCR0 Register
E0024	06h	FIFO	TBCR1 Register
E0020	07h	Interrupt Status	Interrupt Status
E001C	08h	CRDA0	RSAR0
E0018	09h	CRDA1	RSAR1
E0014	0Ah	reserved	RBCR0
E0010	0Bh	reserved	RBCR1
E000C	0Ch	Receive Status	Receive Configuration
E0008	0Dh	CNTR0	Transmit Configuration
E0004	0Eh	CNTR1	Data Configuration
E0000	0Fh	CNTR2	Interupt Mask Register

Assignments for page 1 and page 2 NIC registers follow the same RA0-RA3 to address translation (into E0000 - E003C range) as above list for page 0. The contents of the 2 highest order bits in the command register (PS0 and PS1) define which page of registers is being read and written to thru addresses E0000 - E003C at any given time.

Technical Specifications:

The following table lists characteristics of the input/output pins:

NuBus Signal	Sink Current	Source Current
ACK*	24mA	- 0.5mA
AD31* - AD16*	64mA	- 0.5mA
AD15* - AD8*	24mA	- 0.5mA
AD7* - AD0*	24mA	- 0.4mA
CLK*	0	- 1.4mA
ID3* - ID0*	0	- 1.1mA
NMRQ*	24mA	0
RESET*	0	- 1.05mA
START*	0	- 0.75mA
TM0*	24mA	- 0.20uA
TM1*	24mA	- 0.25mA

Voltage Tolerance

+5 Volts +/- 10%
+12 volts +/- 5%

Isolation Voltage

500 Volts RMS (using onboard transceiver)

Power Dissipation

@ +5 Volts 6.5 watts
@ +12 Volts 3.6 watts

Temperature Variation

0 - 50 degrees Celsius (operating)

Humidity

10% - 90% non-condensing

Tranceiver selection

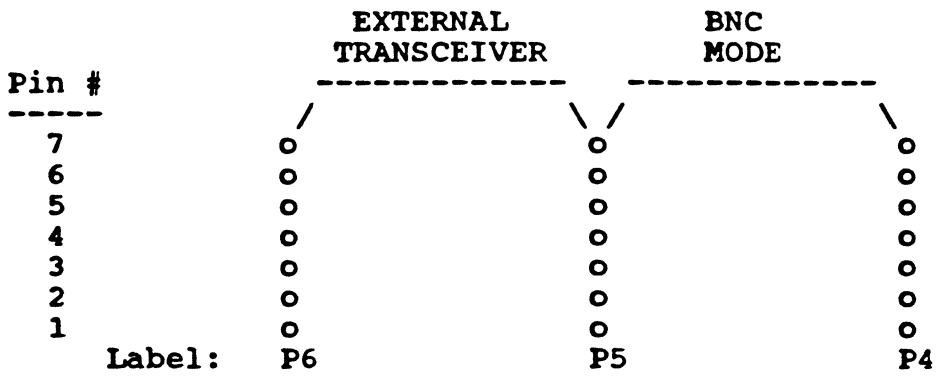
BNC Mode

To transmit and/or receive on " Thin Net " (RG-58 coax) place the blue jumper shorting block in position P5/P4. To confirm your selection verify that the LED (CR12) is illuminated.

External Transceiver Mode

To transmit and/or receive on " Thick Net " place the blue jumper shorting block in position P5/P6.

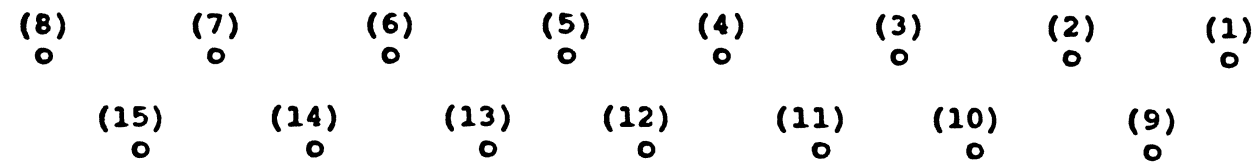
Jumper pin block



BNC Pin Assignments

Pin #	P6	P5	P4
7	o (D +12v)	o (+12v)	o (BNC +12v)
6	o (D coll+)	o (coll+)	o (BNC coll+)
5	o (D coll-)	o (coll-)	o (BNC coll-)
4	o (D rec+)	o (rec+)	o (BNC rec+)
3	o (D rec-)	o (rec-)	o (BNC rec-)
2	o (D xmit+)	o (xmit+)	o (BNC xmit+)
1	o (D xmit-)	o (xmit-)	o (BNC xmit-)

15 Pin D Connector diagram:



Pin #	Signal Name
1	Ground
2	D coll+
3	D xmit+
4	Ground
5	D rec+
6	Ground
7	nc
8	Ground
9	D coll-
10	D xmit-
11	Ground
12	D rec-
13	D +12v
14	Ground
15	nc

Programmatic Guidelines

Programatic Recommendations and Notes:

A. As setup for the Apple NuBus interface, direct access to local memory is provided to the host processor, and as such no use is made of the NIC's remote DMA channel nor of the NIC's Send Packet command for automatic unloading of the receive ring.

B. Programming Sequences recommended below assume 16K bytes of local memory, segmented into transmit and receive buffers with the first 2 K bytes (D0000 - D07FF) assigned as transmit buffer and the remaining 14 K Bytes (D0800 - D3FFF) as a receive ring.

C. The Interrupt Status Register is reset by writing FFh to itself. This results in the clearing of the 7 low order bits. Individual bit level resets are not currently possible. After each ISR reset, the IMR should be restored.

D. In handling the removal of packets from the receive ring and the freeing of buffer space for additional packets, the Boundary pointer is used. Exercise care to make certain that the boundary register lags at least one behind the last freed buffer page.

E. Interrupts to the host processor are masked off or enabled via the Interrupt Mask Register. The cause of the interrupt is presented in the Interrupt Status Register, whether the host interrupt is masked or enabled. This allows event servicing either via an interrupt service routine which checks the ISR to determine interupt cause, or via polling of the ISR.

F. Special care should be taken in modifying the NIC Command Register. In particular, only a single command function may be modified on a single write to the Command Register. Thus, to change from Stop Mode (21h in the CR) to Start Mode with Transmit Packet (26h in the CR) one must first write 22h (changes from Stop to Start Mode) and then write 26h (adds the TXP, Transmit Packet command).

Recommended programming sequences:

A. Initialization Sequence:

1 Set Command Register to 21h (stop mode, page 0 registers).

2 Set Data Configuration Register to 29h.

3 Set Transmit Configuration Register to 00h.

4 Set Receive Configuration Register to 20h, Monitor mode.

5 Set Page Start Register to 08h.

6 Set Page Stop Register to 40h.

7 Set Boundary Register to 3Fh.

8 Set Command Register to 61h (move to page 1 registers).

9 Set Current Register to 08h.

10 Set 6 Physical Address Registers to the node's assigned address.

11 Set 8 Multicast Address Registers to the node's assigned multicast bits.

12 Set Command Register to 21h (back to page 0).

13 Reset Interrupt Status Register by writing FFh.

14 Set Interrupt Mask Register to enable desired interrupts.

15 Ready host software to receive interrupts.

16 Set Command Register to 22h (start mode).

17 Set Receive Configuration Register to desired packets.

B. Transmit Sequence:

1 Load the packet into the transmit buffer beginning on a 256 byte page boundary.

2 Set the Transmit Configuration Register (to 0 for normal operation).

3 Set the Transmit Page Start Register to point to the beginning of the packet in the transmit buffer.

4 Load the Transmit Byte Count Registers (low and high bytes) to the length of the packet to be transmitted.

5 Set the Interrupt Mask Register transmit interrupt bit(s), if an interrupt routine is to handle completed and/or errored transmissions.

6 Set the Command Register to 22h to start the NIC, if it is not already started. Then set the Command register to 26h to initiate transmission of the packet.

7 Upon completion, status indications are available in the ISR and the Transmit Status Register, and interrupts as programmed into the IMR will occur.

C. Receive Sequence:

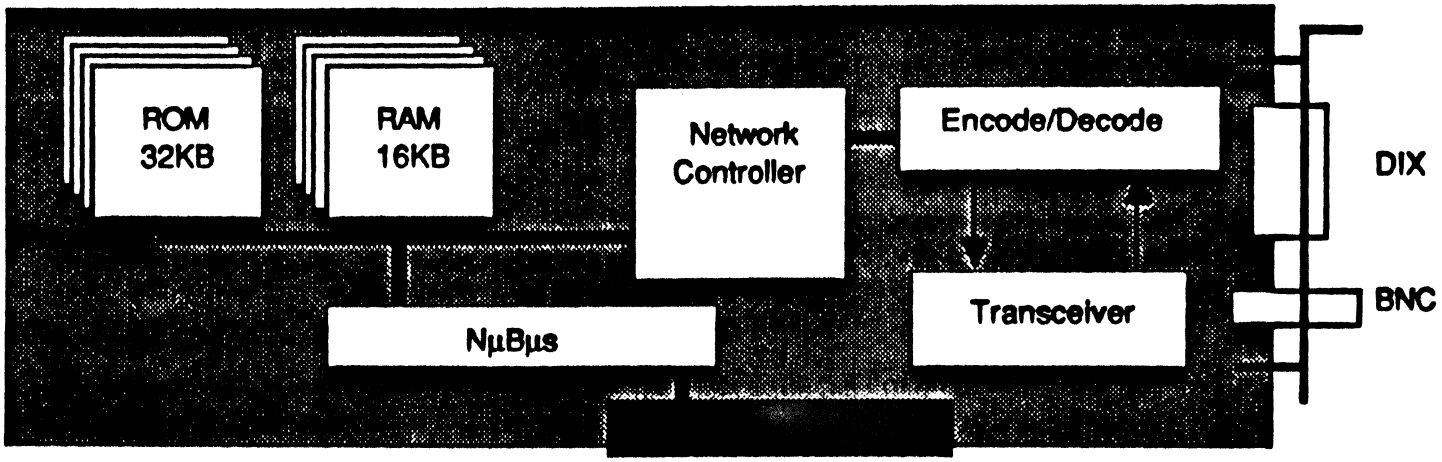
1 Be certain buffer ring inits are completed as in Initialization Sequence above.

2 Set the Interrupt Mask Register receive interrupt bit(s), if an interrupt routine is to handle completed and/or errored receptions.

3 Set the Receive Configuration Register to receive desired packet types only while NIC is already started. (NIC should be in Monitor mode when started.) Reception will commence with the first packet sensed with appropriate destination address after setting the RCR.

4 Upon receipt of a packet, status indications are available in the ISR, the Receive Status Register, and the first byte of the ring packet header.

5 When all data for the packet has been processed, and local memory containing the packet may be freed for additional packets, set the Boundary Register to point to the last page of this finished packet. (This keeps Boundary 1 behind where we expect to next find a packet.)


ROM
32KB
RAM
16KB
Network
Controller
Encode/Decode
DIX
Transceiver
BNC
NμBμs