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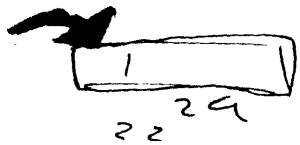
Programmers Model for the Big Mac

Introduction

This document describes the Big Mac from the programmers view of the machine which includes a description of the address space map, the system registers and the decoding of the I/O devices and their registers. The Big Mac MMU and decoding logic maps the 32 bit address space of the 68020 into two address spaces, one for RAM and the other for Screen, ROM and I/O. There exists a 5 bit register named the High Decode Map register which controls the position of the ROM and provides a mechanism to limit the number of address bits used for decoding logical addresses. The HDM register can be programmed to cause the high address bits (those above A23) to be significant to the decoding hardware. This allows a range of address space sizes from 24 to 32 bits. In the smallest configuration, the address space is limited to 16Mb and the upper eight bits are insignificant to decoding which will allow software to use the upper eight bits as tags. In the largest configuration, the address space is 4Gb and none of upper bits are available.



Address Space Map

The address space map is determined by the 5 bit HDM register and the FC2 signal (ie. user/supervisor bit from the 68020). See the following page for drawings of the supervisor and user state address space maps. There are five configurations which are defined as follows:

FC2	HDM3	HDM4	HDM5	VMsize	RAMsize	I/O SLOT ROM SCREEN
1	X	X	X	16Mb	10Mb	A23
0	1	1	1	16Mb	8Mb	A23
0	0	1	1	32Mb	16Mb	A24*A23
0	0	0	1	512Mb	256Mb	A28*A24*A23
0	0	0	0	4Gb	2Gb	A31*A28*A24*A23

Note: The first configuration (ie. FC2 = 1) is supervisor state and the last four configurations (ie. FC2 = 0) are user state.

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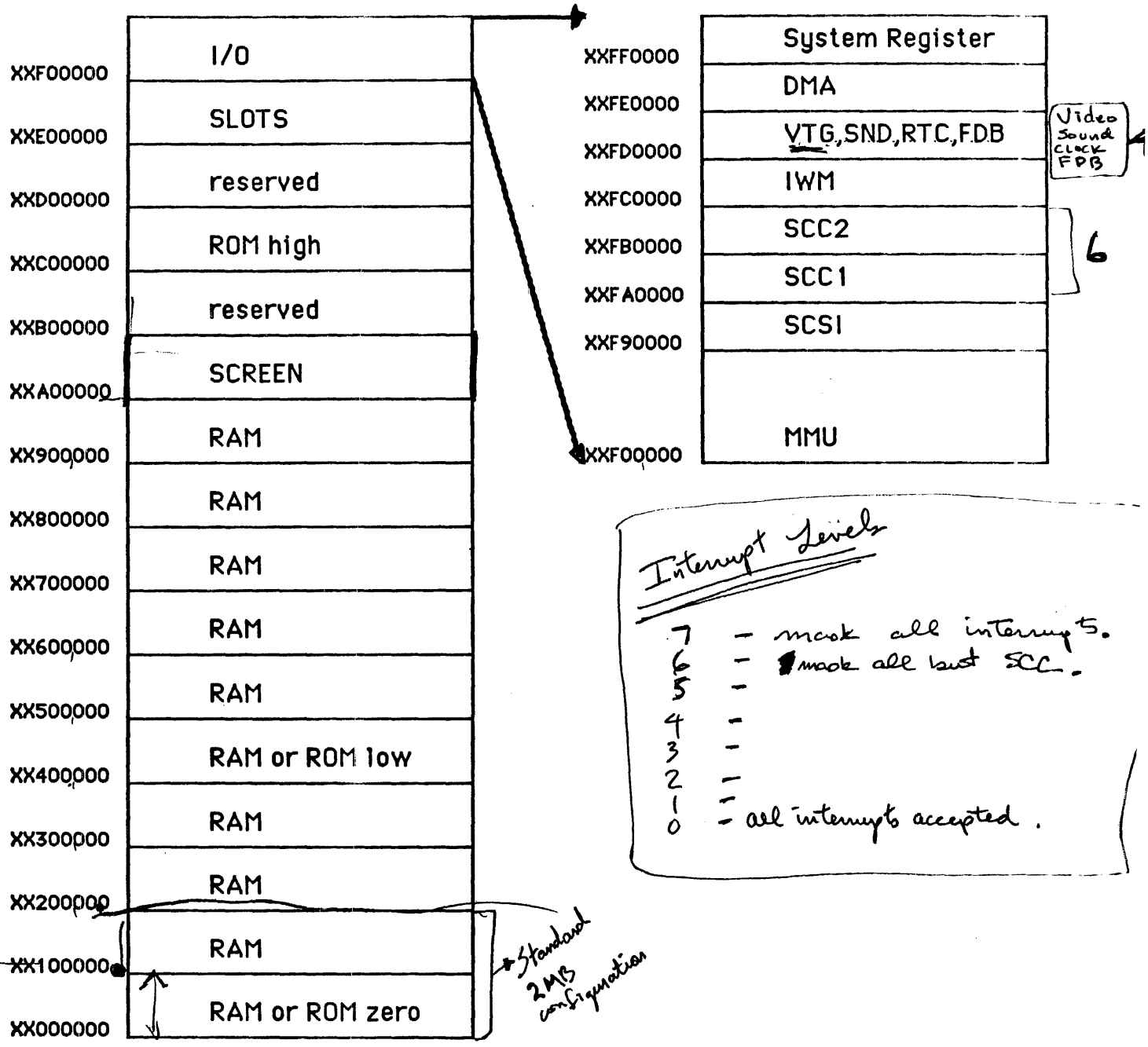
Big Mac Address Space Map (Supervisor State)



Interrupt Levels

7 – mask all interrupts.
6 – mask all but SCC.
5 –
4 –
3 –
2 –
1 –
0 – all interrupts accepted.

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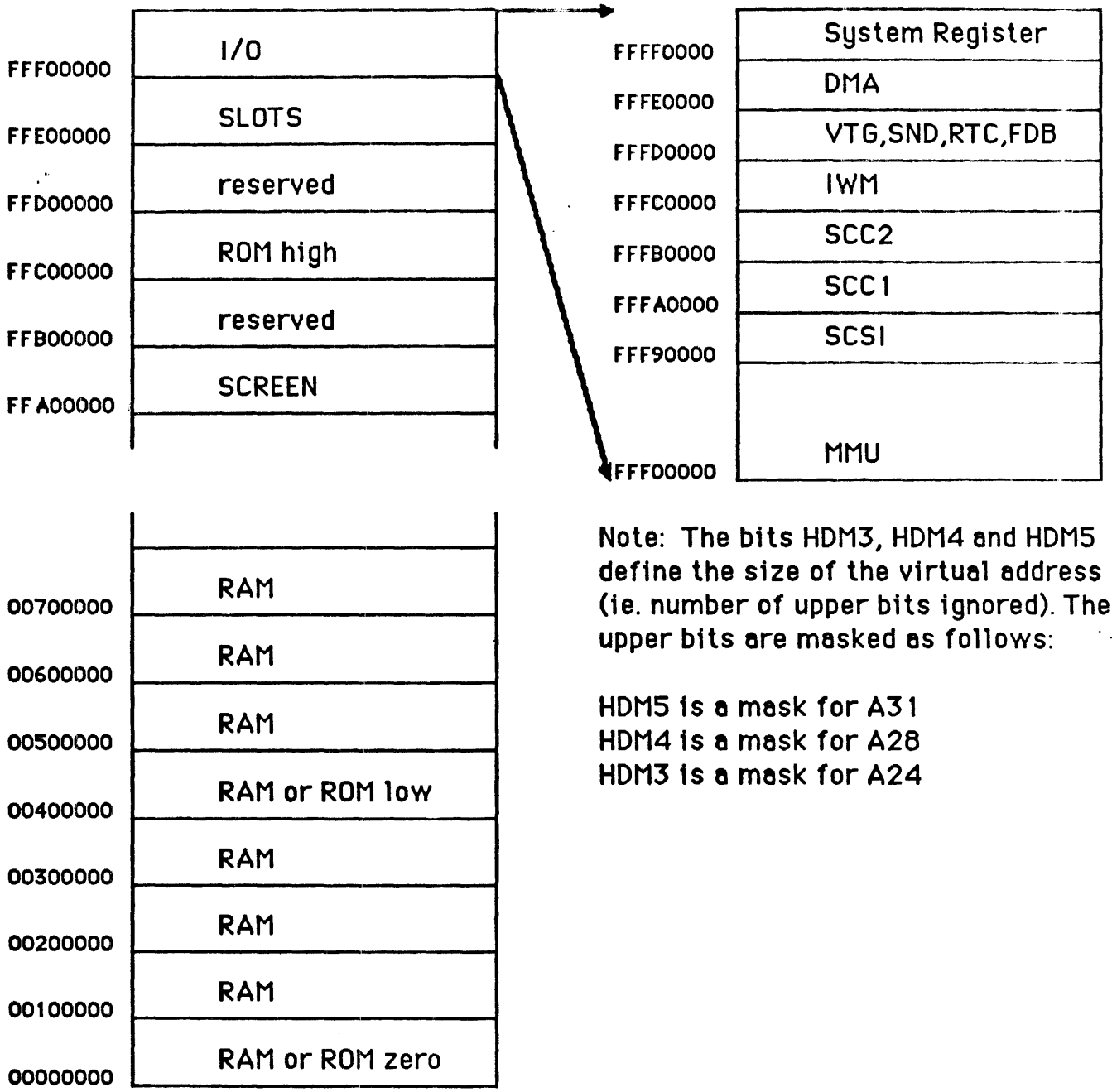
Big Mac Address Space Map (User State)



Note: The bits HDM3, HDM4 and HDM5 define the size of the virtual address (ie. number of upper bits ignored). The upper bits are masked as follows:

HDM5 is a mask for A31
HDM4 is a mask for A28
HDM3 is a mask for A24

ROM Control

The position of the ROM is determined by the 5 bit HDM register and the FC2 signal (ie. user/supervisor bit from the 68020). The HDM1 bit overlays the ROM at location zero (ie. at power on) and the HDM2 bit is the ROM low/high select line. The configurations are defined as follows:

	FC2	HDM1	HDM2	HDM3	HDM4	HDM5	Location	ROM high bit decode	
Supervisor	1	0	X	X	X	X	XX000000, XX400000, XXC00000		(Overlay)
	1	1	1	X	X	X	XX400000	A23	(Low)
	1	1	0	X	X	X	XXC00000	A23	(High)
User	0	1	1	X	X	X	XX400000	A23	
	0	1	0	1	1	1	XXC00000	A23	
	0	1	0	0	1	1	FFC00000	A24*A23	
	0	1	0	0	0	1	FFC00000	A28*A24*A23	
	0	1	0	0	0	0	FFC00000	A31*A28*A24*A23	

Note: The first three configurations (ie. FC2 = 1) are supervisor state with the high byte always ignored. The last five configurations are user state with the options to ignore some or all of the upper address bits.

I/O SLOTS ROM SCREEN Addresses

The I/O, SLOTS, ROM and SCREEN are decoded using addresses A20 through A23 as follows:

Address	Device	Comments
FFF00000	I/O	Decoded using A16-A19 for I/O devices
FFE00000	SLOTS	256Kb per slot
FFD00000	Reserved	
FFC00000	ROM	Dependent on HDM1 and HDM2 bits
FFB00000	Reserved	
FFA00000	SCREEN	Two video pages 100Kb each

Note: The [illegible] determined by FC2 and HDM3, HDM4 and HDM5.

Input/Output Addresses

The I/O space is decoded using addresses A16 through A19 into eight spaces as follows:

	Address	Device	Register Decode Bits	Register Offset
0-8	FFF00000	MMU	A12 thru A19 for GE MMU or A1 thru A8 for SIG MMU	$1000 $2
9	FFF90000	SCSI	A4,A5,A6	$10
A	FFFA0000	SCC1	A1,A2	$2
B	FFFB0000	SCC2	A1,A2	$2
C	FFFC0000	MMU	A9,A10,A11,A12	$200
D	FFFD0000	VTG	A4,A5,A6	$10
E	FFFE0000	DMA	A1-A7	$2
F	FFFF0000	REGISTER	A1,A2,A3	$2

System Register

The system register is only accessible in supervisor state and is defined as follows:

Bit(s)	Field	Description
0	HDM1	ROM overlay line
1	HDM2	ROM low/high select line
2	HDM3	Mask for address bit A24
3	HDM4	Mask for address bit A28
4	HDM5	Mask for address bit A31
5	USRIOE	Enables user access to I/O devices: SCSI, IWM, DMA
6	VIDPG	Selects high/low video page
7	OFFEN	Off enable
8	SV0	Sound volume bit 0 LSB
9	SV1	Sound volume bit 1
10	SV2	Sound volume bit 2
11	SV3	Sound volume bit 3 MSB
12	ENAT1	Enable Apple Talk for SCC1
13	ENAT2	Enable Apple Talk for SCC2
14	DIMPICT	Dim picture control signal
15	HDLED	Enable for Hard Disk LED

6-23 DMABYTE Data for High byte Registers for DMA accesses to RAM

Note: Address bit A3 is used as the High Byte Registers write select. Address bits A2 and A1 are used to address the four High Byte Registers.