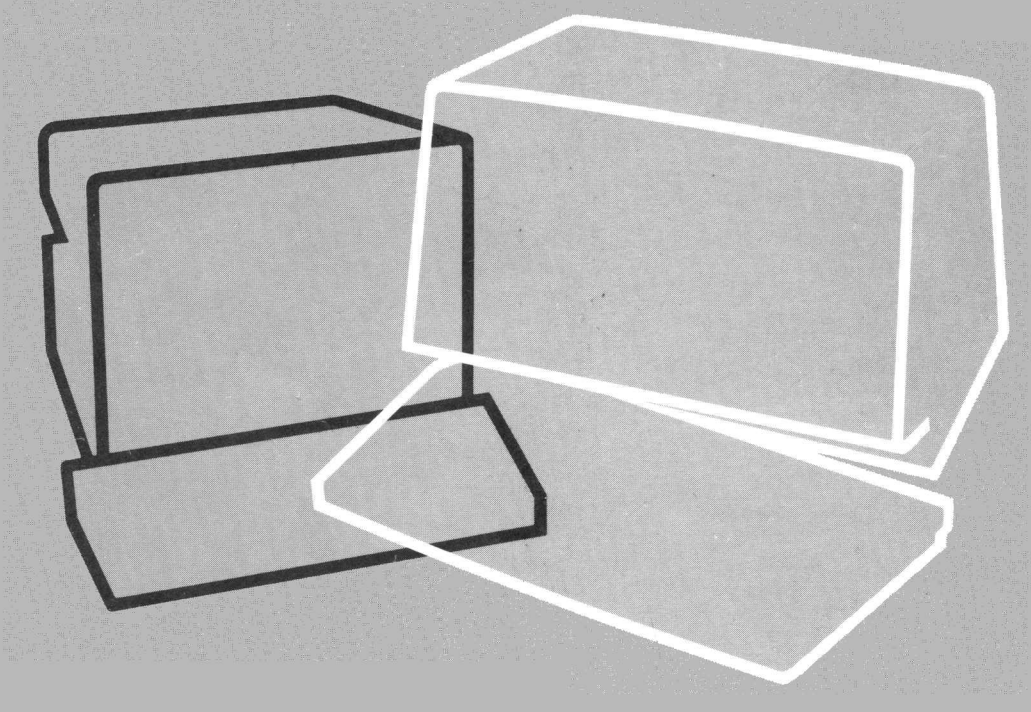
Technical Manual



ANN ARBOR

TABLE OF CONTENTS

CASE 1-1

MONITOR BOARD
- Theory of Operation 2-1
- Setup Procedure 2-6
- Troubleshooting Guide 2-9
- Replacement Parts 2-13

LOGIC BOARD
- Theory of Operation 3-1
- Replacement Parts 3-13

KEYBOARD 4-1

ACCESSORIES
- Computer Cable 5-1
- Printer Cable 5-2

DRAWINGS
- 201185 Monitor Board
- 201197 Terminal Board
- 201199 I/O Board
- 205305 E-Case
- 210000 D-Case

The terminal is supplied in two different case configurations: the Ann Arbor E-Case (see drawings 205305) and D-Case (see drawings 210000). The two cases differ only in size and esthetics. The electronics within them (Monitor board and Logic board) are identical.

INSTALLATION ACCESS

In both cases, access for installation is via an access door at the rear of the case. All connections to the terminal are made behind this door (see User Guide, Checkout and Installation). No connectors protrude from the back to be knocked loose, damaged, or occupy extra space. The door safely clamps the cables as they issue from the case. Any excess cable lengths may be stored within the case for a neater installation.

MAINTENANCE ACCESS

Access for installation is perfectly safe to un-trained personnel. Neither the CRT nor hazardous portions of the circuitry are accessible through the access door.

Access for maintenance is NOT SAFE for untrained personnel. The CRT is made of glass and will implode if broken. The Monitor board generates voltages up to 17KV and portions of its circuitry operate with a "hot" ground.

ACCESS FOR MAINTENANCE SHOULD BE ATTEMPTED ONLY BY QUALIFIED TECHNICAL PERSONNEL.

In the E-Case, access for maintenance is by removal of the rear hood. Place the unit with its screen down. Remove the access door, and unplug the P1-connector (horizontal white connector below the keyboard connector). Remove the two screws at the side of the hood (that attach it to the bezel) and lift it free. Steer the P1-connector so that it doesn't catch on the Logic board. This exposes the Monitor board for debug. To expose the Logic board, remove the four screws attaching it to the hood and lay it in the bottom of the hood (or other insulated surface), and re-connect P1.

In the D-Case, access for maintenance is by removal of the top cover. Remove the four screws from the base and lift off the cover. This exposes both the Monitor and Logic boards for debug.

BOARD REPLACEMENT

To replace the Logic board, unplug the P1 connector (and the keyboard and I/O cables if plugged in), and remove the four screws attaching it to the hood (E-Case) or frame (D-case).

To replace the Monitor board:

1. Unplug the CRT socket.

2. Detach the anode cap. Use a grounded screwdriver under the rubber cap, shorting out the pins (to discharge any residual high voltage that might be present). Squeeze the pins together slightly to release the cap from the tube.

3. Unplug the yoke connectors, RED/BLK near the front of the board, YEL/GRN near the back of the board.

4. Detach the GND spring at the top and bottom of the tube.

5. Remove the four screws attaching the board to the frame.

6. Unplug the in-line Power and Contrast pot connectors.

Reverse the procedure to install the new board. After installing a new Monitor board, the setup procedure (given in the Monitor section) should be followed.

THEORY OF OPERATION

The Monitor board contains the monitor electronics, and the power supply for both the Monitor and the Logic boards.

The Monitor board consists of six sections:

100 Power Supply
200 Vertical Deflection circuit
300 Video Drive circuit
400 Horizontal Deflection circuit
500 CRT Bias network
600 Bell circuit

The Monitor board drawings (see drawings 201185) consist of three sheets. Sheet #1 is an Assembly drawing of the board showing component locations. Component designations carry their section number. Sheet #2 is a Schematic drawing of the 100 and 600 sections of the board. Sheet #3 is a Schematic drawing of the 200 through 500 sections of the board.

The sections are described below in reference to their Schematic drawings.

100 POWER SUPPLY

A switch-mode power supply is used to provide good efficiency over a wide range of incoming line voltages. Elimination of the line transformer eliminates display "swim" when used on off-frequency lines. By synchronizing the switching with the horizontal sweep rate, any switching noise that might be coupled into the display is masked in the horizontal blank period.

INPUT CIRCUIT. The incoming line voltage is full-wave rectified by a diode bridge D100 and stored (at about 160VDC) in capacitor C108. F100 and S100 fuse and switch the AC line. Capacitors C100, C103, C111, C112 provide filtering of the line. Thermistor RT100 limits the surge current during a cold start. C104, C105, C106, C107 reduce diode switching transients. R101 is a bleeder to discharge C108 following power off.

SWITCHING CIRCUIT. The voltage on C108 is impressed across a switching transformer T100 and a switching transistor Q105. When Q105 is on, T100 charges from C108. When Q105 is turned off, the collapsing magnetic field dumps the energy stored in T100 into the secondary windings. The induced voltages are rectified and filtered to provide the required DC supplies. D112, R116, C135 form a snubber network that protects Q105 during turn-off.

SWITCHING REGULATOR CIRCUIT. One of the secondary windings (pins 5, 6) is rectified and filtered (through D104, R110, C130) to form a control voltage. This voltage feeds a switching regulator circuit, consisting of IC100 and Q101-104. This circuit operates at the horizontal sweep rate of the monitor, and controls the on-time of Q105 so as to maintain the voltage constant with varying line and load.

The control voltage at C130 is divided through R112, RV100, R127 to about 2 volts and fed into the comparator input (pin 4) of IC100. C141, R133 provide

AC feed-forward compensation across the divider for improved ripple rejection. Within IC100, the control voltage is compared against a 2-volt internal reference, and an error voltage generated at pin 5.

The error voltage is divided and filtered by R132, R131, C128 and applied to the base of Q102. R132, R131 set the maximum on-time of Q5 to about 60% of the horizontal sweep time. Q102 buffers the error signal through R135 into the pulse-width modulator input (pin 8) of IC100. R136 sets the minimum on-time of Q105 to about 15% of the horizontal sweep.

The output of IC100 (pin 1) is a square wave having a frequency determined by the input at pin 7 and a duty cycle determined by the input at pin 8. At pin 7, R122, C138 set a free-running oscillator frequency slightly lower then the horizontal sweep rate. The oscillator is then locked to the horizontal sweep by an input from the flyback transformer T401 coupled through C139 to the base of Q101.

Q103, Q104 amplify the square wave and provide push-pull drive to the base of Q105. At normal line, Q105 should be on about 1/3 of the horizontal sweep time. When the line drops or the load increases, the on-time increases. When the line rises or the load decreases, the on-time decreases.

START-UP CIRCUIT. The regulator circuits are powered (through R143, D111, C127, C126) from the same winding as the control voltage is derived. At initial turn-on, this supply is not active. A start-up circuit (Q108-110) provides power to the regulator circuits during this period.

At turn-on, the voltage across C108 is impressed across R103 and zener D113, providing a 24-volt reference to the start-up circuit. C109 charges through R102. When the voltage across C109 builds sufficiently, Q108 turns on, turning on Q109 and Q110. C109 discharges through Q110 into the 30-volt supply, powering the regulator. When the voltage across C109 drops sufficiently, Q108 turns off, turning off Q109 and Q110, and the process repeats, if required, as the voltage across the control winding builds.

CURRENT LIMITING. A current-limit circuit (Q107, Q106, Q111, Q100) protects the switching circuit during turn-on, or shorts on any of the secondary voltage supplies.

The average current through the switching circuit is monitored by R117, C136 in the emitter of Q105. This signal is filtered and divided through R130, C145, R138, R140 to the base of Q107. Q107 is normally off, and Q100 holds the enable input of IC100 low (about 1.2V).

If the average current becomes excessive, Q107 turns on. This turns on Q111 which discharges C143, and (through Q100) pulls the enable input of IC100 high (above 2V). This disables the comparator, causing the on-time of Q105 to pull back to its minimum setting. The secondary voltages drop back, the overcurrent signal drops back, and Q107 and Q111 turn off.

Because C143 is discharged, Q100 cannot immediately re-enable the comparator. Rather, as C143 charges, the voltage at pin 3 slowly drops, the on-time of Q105 slowly increases, and the secondary voltages come up gradually.

If the short persists, Q107 will again turn on, and the regulator will pull back and try again. However, during each Q111 on-period, C146 is being charged through D101 and R158. If the short persists through several trys (ie, it is a "hard" fault), the voltage across C146 will become large enough to turn Q106 on. This latches the supply into a pulled-back state, and can be relieved only by powering down and correcting the fault.

200 VERTICAL DEFLECTION CIRCUIT

The vertical deflection circuit is shown at the top of sheet 3. It accepts vertical sync pulses from the logic board and controls the Y-axis of the CRT.

IC200 is the vertical oscillator. R204, R202, C202 set a free-running oscillator frequency slightly lower than the vertical sweep rate. The oscillator is then locked to the vertical sweep by the sync pulses from the logic board.

The oscillator output (pin 6) is a sawtooth waveform developed across C202. C202 is charged (through R202, R204) while the sync pulse input (pin 5) is high, and discharges (through R204) when the input goes low. Zener D200 in the 12V supply stabilizes the waveform against power supply variations.

Q207 is a Darlington amplifier/buffer. It has a high input impedance so as not to load down the charging of C202, and provides a low impedance source of the sawtooth waveform to Q200. RV200 in the emitter of Q207 provides for vertical height adjustment.

Q200 and Q201 form a differential amplifier that compares the generated sawtooth with a signal related to the current actually flowing through the yoke (R224) and the voltage across it (R214). The signal is modified by low-pass filter R210, RV202, and C208 to provide for linearity adjustment of the vertical sweep.

Q202 buffers the output of the differential amplifier and drives the output transistors Q203 and Q204. The transistors are biased by the network R213, D201, R219, R217, R218, and the emitter resistors R216, R220.

During trace time, the transistors drive the yoke with a positive-going ramp from about -2V to +2V. C213 is charged to about 24V through R221 and D202. The retrace generator Q205 is biased off by R222, R223, C214.

When vertical retrace occurs, Q205 is turned on (through C214, R223). This pulls the plus side of C213 to -12V, which pulls the yoke (through Q204) to about -36V, resulting in a fast (about 400 microsecond) vertical retrace.

300 VIDEO AMPLIFIER
500 CRT BIAS NETWORK

The video amplifier is shown at the lower-left of sheet 3. It accepts video and blanking signals from the logic board and, in conjunction with the CRT bias network, controls the Z-axis of the CRT.

Q300, Q301 form a non-inverting video amplifier with a gain of 1 to 1.5. TTL-level video from the logic board is ac-coupled into the amplifier through C313. C302 adds a little leading-edge peaking to the video for better character definition. RV300 sets the amplifier gain (and is the external 'brightness' control).

Q303 sets the black-level of the video at the input to the amplifier. It is turned on during horizontal retrace, by a pulse coupled from the flyback transformer T401 (pin 8), and gates in a voltage, set by the black-level adjustment RV300, to control the charge on C313, holding the black-level constant regardless of signal input.

Q305, Q304 form a cascode amplifier that drives the CRT. L300 provides additional video peaking. D300 (in series with the 70V supply) ensures CRT cutoff at power-down to avoid phosphor burn.

Q302 pulls the input to the amplifier to GND (video off) in response to a video-blanking signal from the logic board, if provided.

In the CRT, the video amplifier drives the cathode. G1 (control grid) bias is set by R502, RV500, R501. G2 (accelerating anode) bias is set by R503, R504.

400 HORIZONTAL DEFLECTION CIRCUIT.

The horizontal deflection circuit is shown at the lower right of sheet 3. It accepts horizontal sync pulses from the logic board and controls the X-axis of the CRT.

IC400 is the horizontal oscillator. RV403, R414, C409 set the free-running oscillator frequency. The horizontal flyback pulse is shaped into a sawtooth and coupled to pin 4 of IC400 through the network R410, R413, C401, C402. Horizontal sync is differentiated and coupled to pin 3 by R400, C400. Pins 3 and 4 are the inputs of a phase comparator which produces an output voltage proportional to the phase difference between the sync and sawtooth inputs at pin 5. R412, C408 filter the voltage, and R411 couples it to pin 7 to provide dynamic control of the oscillator frequency and phase. The oscillator output (pin 1) is a square-wave at the horizontal frequency, having a duty cycle determined by R401, R402. The output is buffered by Q400 and transformer-coupled through T400 to the base of Q401.

When Q401 is on, the flyback transformer T401 charges from the 70V supply. When Q401 is turned off, the collapsing magnetic field looks into a parallel resonant circuit consisting of C410 and the circuit containing the horizontal winding of the yoke (L405). The energy stored in T401 is dumped rapidly into the yoke circuit, causing the beam to "flyback" to the left edge of the

screen.

When the voltage across the circuit trys to ring back through zero, D400 conducts and the yoke circuit gradually discharges, sweeping the beam toward the center of the screen. When the beam nears the center of the screen, Q104 takes over, actively continuing the sweep and re-charging T401.

Some of the energy stored in T401 is dumped to other loads.

a) Flyback pulse feedback to the horizontal oscillator and the -70V supply.
b) Flyback sync pulse to the switching regulator (winding A, B)
c) Filament power for the CRT (winding 7, 8)
d) 500V supply for the CRT focus and G2-bias circuits (D401)
e) 17KV anode supply for the CRT (D403)

The other components in the yoke circuit provide correction for the sweep. L406 is a variable inductor that provides for horizontal width adjustment. L407 is an adjustable saturable reactor that compensates for non-linearities at the end of the sweep due to yoke resistance. C415 provides "S" correction at the extreme ends of the scan.

The G4 (focus) grid of the CRT is set by RV400 for best focus at the center of the screen. A dynamic focus circuit (Q402) permits this focus to be maintained over the full sweep. The voltage developed across C415 forms a parabola across the sweep. An adjustable amount of this voltage may be picked off by RV401, and added to the DC level set by RV400.

SETUP PROCEDURE

EQUIPMENT REQUIRED.

a) Line-isolated variable AC supply (Variac) with current meter

b) Voltmeter

c) Oscilloscope with 100X probe

SETUP PROCEDURE.

1. Preset all controls to mechanical center, except:

   a. RV300 (contrast) full counter-clockwise (minimum contrast)

   b. RV301 (black-level) fully counter-clockwise from rear (minimum drive)

2. Connect monitor to isolated supply with voltage turned down to zero.

3. Turn on monitor and variac. Adjust the voltage up slowly, making sure that the switching supply starts. Adjust to 120VAC if no problems occur.

4. If the raster comes up too bright, adjust RV500 (brightness) so that raster is just on.

5. Adjust RV202 (vertical linearity) and RV200 (vertical height) for approximately 7" height.

6. Adjust L406 (horizontal width) for approximately 10" width. (Note: On high sweep rate units, L406 may be shorted out by a jumper on the back of the board, for maximum width. If it is necessary to reduce the width, remove this jumper.

7. Adjust RV100 (B+) for 70VDC at junction of R105 and C117. Check the +12V, -12V, +5V, -5V supplies for proper levels. (The latter 3 supplies may be as much as 1V high as there is no logic board load.)

8. Check that the CRT filament voltage (brown leads of the CRT socket) is between 5.9 and 6.7VAC. If outside of this range, the filament dropping resistor (R428) should be changed in the range 2.7 to 4.7 ohm, 1 watt.

9. Turn off the monitor. Connect the logic board. Turn on the monitor.

10. Check the unit for proper operation:

   a. Adjust RV403 (horizontal hold) for horizontal pull-in, if needed.

   b. Check that raster is locked-in vertically.

c. Check that video is present. (May require adjustment of brightness and contrast controls. Adjust for normal level.)

d. Re-adjust height (approx 7") and width (approx 10") if needed.

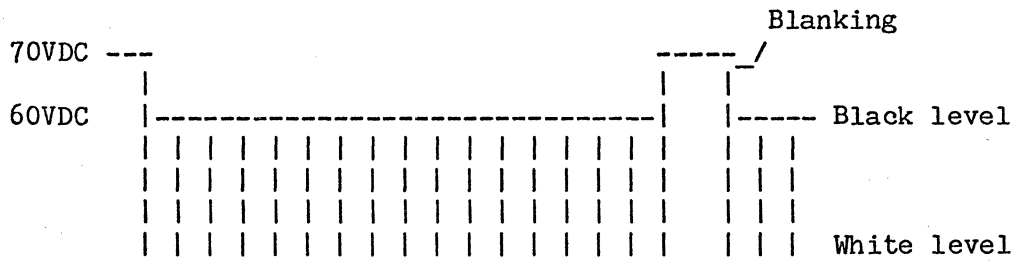
11. Reset the 70V supply, and check all supplies for proper levels. Fill the screen with characters. If the logic board provides for both 'bright' and 'dim' characters, use 'bright'. Reduce the line voltage slowly. The line current will increase (from about 0.5A) to a level which causes the over-current protection circuit to attempt to shut down the supply. Check that this 'trip point' occurs between 0.65A and 0.9A line current. Reset the line voltage to 120VAC.

12. Short out TP1 (horizontal sync) with a short clip-lead. Adjust RV403 for horizontal free-running frequency. Remove clip-lead. Horizontal should pull-in to sync. Video should be phased on raster so that there is no fold-over.

13. Connect oscilloscope to TP2 (CRT cathode). Set vertical on DC at 20V (p-p) per division. Set horizontal sweep at horizontal rate (or vertical rate if logic board generates only vertical blanking).

14. Set up contrast, brightness, and black-level.

a. With RV300 (contrast) at minimum, adjust RV301 (black-level) so that the black-level of the video signal (see diagram) is at 60VDC. (Caution: Do not mis-adjust this control, as over-dissipation of the video amplifier Q304 may result.)



b. Turn the contrast control to maximum. The video output should be capable of 40V (p-p) from black level to peak white without compression.

c. With the contrast set for normal level, adjust RV500 (brightness) so that the background level is slightly blacker than black. If the unblanked raster is not black, or if very little reserve control remains, the brightness range of RV500 may be adjusted by changing R501 in the range 56K to 82K ohm, 1/2 watt.

d. Turn the contrast control to minimum. The characters must still be visible (but should be dimmer than a normal setting). If the character brightness is too high, the brightness control may be adjusted slightly to bring the brightness level down. (Caution: Under no circumstances should turning the contrast control to minimum result in a completely blank display. At maximum contrast, this will cause the video amplifier to compress and cause streaking of the displayed video.

15. Adjust RV200 and RV202 (vertical height and linearity), if needed.

16. Adjust L406 and L407 (horizontal width and linearity), if needed.

17. Check the display geometry of the CRT and yoke. Re-centering of the display may be done if it improves the geometry. If the display is not acceptable, magnets may be moved or changed, but they should always be glued in place in the liner pockets provided.

18. Re-adjust the vertical height and linearity, and the horizontal width and linearity, for proper aspect ratio (about 7" H x 10" W). (Note: To adjust horizontal linearity, turn the biasing magnet in L407 until the left side of the raster just stops moving toward the center of the screen. At the same time, the right side will be moving toward the outside edge of the screen. The correct effect is to compress the left side and stretch the right.)

19. Adjust the dynamic focus as follows:

a. Connect oscilloscope to TP3. Set vertical on DC, 100V per division.

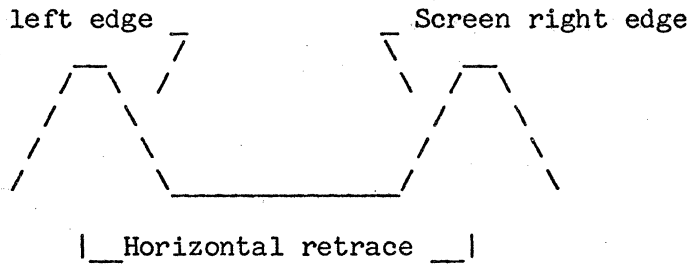
b. Adjust RV401 (dynamic focus) so that there is no dynamic correction.

c. Adjust RV400 (focus) for best focus at the center of the screen. Note the DC voltage required.

d. Adjust RV400 for best focus in the upper-left corner of the screen. Again, note the DC voltage required.

e. Adjust RV401 so that the amplitude of correction (at TP3; see diagram) is the difference between the voltage readings noted above.

f. Again, adjust RV400 for best center focus. The upper-left corner should now be in focus.



20. The monitor is now set up properly.

TROUBLESHOOTING

The following is intended to provide troubleshooting hints in the various sections of the Monitor board, based on an understanding of the previous sections. It is not intended to be an exhaustive troubleshooting procedure.

100 POWER SUPPLY

1. No raster; no power supply voltages.

    a. Check fuse. If open:

        1) Check Q105 for short. If Q105 is shorted, check also R117.

        2) Check D100 for short.

        3) Check C108 for short.

    b. Check voltage at D111. If the power supply is trying to start, the voltage will rise toward 30V, fall back to about 6V, and repeat. If it is not trying to start

        1) Check that C108 charges to about 160VDC.

        2) Check that D113 provides 24V reference.

        3) Check the start-up circuit (Q108, Q109, Q110, C109).

    c. Disconnect the secondary loads from T100, one at a time starting with +70V, to see whether a heavy load or short in the secondary is causing the supply to current limit and shut down. If lifting a secondary permits the supply to come up, troubleshoot to the section causing the overload.

    d. Check Q105 for low resistance. Also check R117 for high resistance (which will cause the current-limit circuit to sense an overload).

    e. Check the switching regulator circuit (IC100).

    f. Check the current-limit circuit (Q107, Q106, Q111, Q100).

    g. Check for oscillator input at IC100 pin 7 (Q101, C138).

    h. Check for faulty Q102, Q103, Q104.

200 VERTICAL DEFLECTION

1. No vertical deflection.

   a. Check for output from vertical output circuit (Q203, Q204). If no output, check for signal at output of previous stages (Q202, Q200/201, Q207, IC200). The output of Q200/201 is a square wave at the vertical rate. All others are of sawtooth waveshape.

   b. Check yoke circuit.

2. Reduced height.

   a. Check vertical height adjustment (RV200).

   b. Check for low B+ voltage (+12V).

   c. Check for low gain in one of the vertical stages.

3. Poor linearity (top or bottom compressed).

   a. Check linearity adjustment (RV202).

   b. Check diff amp (Q200/201).

   c. Check vertical output (Q203/204).

4. Loss of vertical sync.

   a. Check for sync pulse from Logic board. If not present, troubleshoot to Logic board.

   b. Check vertical oscillator (IC200).

300 VIDEO DRIVE

1. No video; raster OK.

   a. Check for video signal from Logic board. If not present, troubleshoot to Logic board.

   b. Check for signal at base of Q305. If not present, check video circuit (Q300, Q301, Q302, Q303).

   c. Check for signal at TP2. If not present, check video drivers (Q304, Q305).

   d. Replace CRT.

2. No video; raster brightness too high.

   a. Check for short, or improper bias, in video drivers (Q304, Q305).

3. Weak video; raster and video present, but poor contrast.

   a. Adjust brightness (RV500), contrast (RV300), and black-level (RV301). See Setup procedure.

   b. Check video amp (Q300, Q301) and contrast control circuit.

   c. Check black-level clamp circuit (Q303).

   d. Check video drivers (Q304, Q305) for leakage or low gain.

   e. Replace CRT.

4. Brightness level variations

   a. Check CRT video and grid inputs for corresponding variations in voltage.

   b. Replace CRT.

5. No raster; power supply and high voltage OK.

   a. Check filament voltage.

   b. Check brightness adjustment (RV500) and bias of G1.

   c. Check bias at G2 and G4.

   d. Replace CRT.

400 HORIZONTAL DEFLECTION

1. No raster; no high voltage.

   a. Check for +70V. If not present, disconnect pin 3 of T401 (flyback). If this allows +70V to come up, look for shorted Q401 or diode in the collector circuit of Q401.

   b. Check for output from the horizontal oscillator (IC400 pin 1). If not present, check pin 7 for sawtooth signal (at the free-running oscillator frequency). If no signal, check for bad C409, RV403. Check pin 6 for +8V. If not present, check for +12V supply or shorted C403. If all OK, replace IC400.

   c. Check for input to base of Q401. If not present, check Q400, T400.

   d. Check for pulse at collector of Q401. If not present, replace Q401. Note: If there is a signal at the collector, but not the proper level or waveform, check for faulty flyback, yoke, or component in the yoke circuit.

   e. Check for open high-voltage rectifier (D403).

2. Reduced horizontal scan.

   a. Check base drive at Q401. If not OK, check oscillator (IC400) and drive (Q400, T400) circuits.

   b. Check yoke and yoke series components.

3. Loss of horizontal sync.

   a. Check for sync pulse from Logic board. If not present, troubleshoot to Logic board.

   b. Check horizontal oscillator (IC400).

4. Loss of horizontal sync or drift after warmup.

   a. Check for faulty C409, C403, or other capacitor in the oscillator circuit.

   b. Check horizontal oscillator (IC400).

5. Blooming raster (large raster; low high voltage).

   a. Check for proper drive at base of Q401.

   b. Check for shorted high-voltage rectifier (D403).

   c. Check for bad retrace cap (C410) or S-cap (C415).

6. Compressed characters at right side of raster.

   a. Check for proper drive at base of Q401.

   b. Check for phase problem at IC400 pin 4.

   c. Check the linearity coil (L407).

   d. Check the other yoke series components.

REPLACEMENT PARTS.

The Monitor board is built in 115VAC and 230VAC versions. Where part differences exist, the 230VAC parts are identified by the label #2.

REPLACEMENT BOARDS

210402A	S/A MON BD 8500 (115VAC)	
210403B	S/A MON BD 8598 (230VAC)	#2

INTEGRATED CIRCUITS

Z100	180113	IC MC1391P
Z200	180104	IC 555
Z400	180113	IC MC1391P
Z600	180104	IC 555

TRANSISTORS

Q100	170035	XSTR MPSA70
Q101	170035	XSTR MPSA70
Q102	170027	XSTR MPSA20
Q103	170028	XSTR MPSU05
Q104	170032	XSTR NSDU56
Q105	170040	XSTR SJE2319
Q105#2	170041	XSTR MJ12004
Q106	170027	XSTR MPSA20
Q107	170027	XSTR MPSA20
Q108	170035	XSTR MPSA70
Q109	170027	XSTR MPSA20
Q110	170027	XSTR MPSA20
Q111	170035	XSTR MPSA70
Q200	170027	XSTR MPSA20
Q201	170027	XSTR MPSA20
Q202	170031	XSTR 92PU57
Q203	170034	XSTR 2N5496
Q204	170033	XSTR 2N6109
Q205	170032	XSTR NSDU56
Q207	170024	XSTR MPSA13
Q300	170027	XSTR MPSA20
Q301	170035	XSTR MPSA70
Q302	170027	XSTR MPSA20
Q303	170035	XSTR MPSA70
Q304	170037	XSTR MPSU03
Q305	170036	XSTR 2N3704
Q400	170032	XSTR NSDU56
Q401	170038	XSTR 2N6308
Q402	170039	XSTR BUX86
Q600	170035	XSTR MPSA70
Q601	170027	XSTR MPSA20

DIODES

D100	160064	BRIDGE VS447
D100#2	160066	BRIDGE VS847
D101	160004	DIODE 2N4148
D102	160004	DIODE 2N4148
D103	160004	DIODE 2N4148
D104	160041	DIODE BY206
D105	160041	DIODE BY206
D106	160046	DIODE MR810
D107	160053	DIODE MR850
D108	160046	DIODE MR810
D109	160046	DIODE MR810
D111	160041	DIODE BY206
D112	160042	DIODE BY208
D113	160043	DIODE 1N4749
D200	160062	DIODE 1N5236
D201	160048	DIODE 1N4448
D202	160033	DIODE 1N4003
D203	160033	DIODE 1N4003
D300	160038	DIODE 1N4004
D301	160004	DIODE 1N4148
D400	160044	DIODE MR818
D401	160044	DIODE MR818
D402	160041	DIODE BY206

RESISTORS (All rstrs 1/4W unless specified)

RV100	150929	TMPT 100
RV200	150926	TMPT 10K
RV202	150925	TMPT 5K
RV301	150925	TMPT 5K
RV400	150922	POT 2M
RV401	150926	TMPT 10K
RV403	150925	TMPT 5K
RV500	150934	TMPT 250K
R100	150106	RSTR 68K
R100#2	150098	RSTR 33K
R101	150315	RSTR 150K 1/2W
R101#2	150323	RSTR 330K 1/2W
R102	151304	RSTR 22K 2W GL
R102#2	151302	RSTR 47K 2W GL
R103	151301	RSTR 15K 3W GL
R103#2	151302	RSTR 47K 3W GL
R105	151101	RSTR 4.7 1W GL
R110	150034	RSTR 68
R112	150081	RSTR 6.2K
R113	151306	RSTR 180 2W GL
R113#2	150544	RSTR 330 1W
R114	150022	RSTR 22
R114#2	150034	RSTR 68
R115	150231	RSTR 47 1/2W
R116	151300	RSTR 1K 2W GL
R116#2	150302	RSTR 47K 3W GL (2 in parallel)

R117	151303	RSTR 2.6 1W GL
R117#2	151500	RSTR 5.0 3W GL
R118	150271	RSTR 2.2K 1/2W
R119	150048	RSTR 270
R120	150562	RSTR 1K 1W
R121	150114	RSTR 150K
R122	150090	RSTR 15K
R123	150048	RSTR 270
R124	150058	RSTR 680
R126	150130	RSTR 680K
R127	150052	RSTR 390
R128	150108	RSTR 82K
R129	150090	RSTR 15K
R130	150062	RSTR 1.0K
R131	150100	RSTR 39K
R132	150086	RSTR 10K
R133	150054	RSTR 470
R134	150050	RSTR 330
R135	150062	RSTR 1.0K
R136	150126	RSTR 470K
R137	150038	RSTR 100
R138	150088	RSTR 12K
R139	150078	RSTR 4.7K
R140	150084	RSTR 8.2K
R141	150086	RSTR 10K
R142	150239	RSTR 100 1/2W
R143	150167	RSTR 2.2
R144	150498	RSTR .47 1W
R145	150223	RSTR 22 1/2W
R146	150090	RSTR 15K
R147	150086	RSTR 10K
R148	150167	RSTR 2.2
R151	150098	RSTR 33K
R152	150122	RSTR 330K
R153	150014	RSTR 10
R157	150090	RSTR 15K
R158	150094	RSTR 22K
R159	150134	RSTR 1.0M
R200	150251	RSTR 330 1/2W
R202	150114	RSTR 150K
R203	150064	RSTR 1.2K
R204	150062	RSTR 1.0K
R205	150038	RSTR 100
R206	150062	RSTR 1.0K
R207	150102	RSTR 47K
R208	150062	RSTR 1.0K
R209	150086	RSTR 10K
R210	150073	RSTR 3.0K
R212	150062	RSTR 1.0K
R213	150014	RSTR 10
R214	150106	RSTR 68K
R215	150235	RSTR 68 1/2W
R216	150197	RSTR 1.0 1/2W
R217	150253	RSTR 390 1/2W
R218	150253	RSTR 390 1/2W

R219	150018	RSTR 15
R220	150197	RSTR 1.0 1/2W
R221	150253	RSTR 390 1/2W
R222	150074	RSTR 3.3K
R223	150052	RSTR 390
R224	150197	RSTR 1.0 1/2W
R225	150259	RSTR 680 1/2W
R226	150235	RSTR 68 1/2W
R300	150223	RSTR 22 1/2W
R301	150215	RSTR 10 1/2W
R302	150070	RSTR 2.2K
R303	150038	RSTR 100
R305	150086	RSTR 10K
R306	150090	RSTR 15K
R307	150050	RSTR 330
R310	150070	RSTR 2.2K
R311	150074	RSTR 3.3K
R312	151400	RSTR 1.2K 3W GL
R314	150038	RSTR 100
R315	150062	RSTR 1.0K
R317	150050	RSTR 330
R318	150036	RSTR 82
R319	150042	RSTR 150
R320	150042	RSTR 150
R321	150066	RSTR 1.5K
R322	150030	RSTR 47
R323	150046	RSTR 220
R324	150040	RSTR 120
R325	150056	RSTR 560
R326	150028	RSTR 39
R328	150094	RSTR 22K
R330	150086	RSTR 10K
R331	150132	RSTR 820K
R333	150050	RSTR 330
R400	150066	RSTR 1.5K
R401	150069	RSTR 2.0K
R402	150071	RSTR 2.4K
R404	150042	RSTR 150
R405	150064	RSTR 1.2K
R406	150054	RSTR 470
R407	150538	RSTR 100 1W
R408	150239	RSTR 100 1/2W
R410	150084	RSTR 8.2K
R411	150110	RSTR 100K
R412	150078	RSTR 4.7K
R413	150038	RSTR 100
R414	150086	RSTR 12K
R415	150195	RSTR 0.5 1/2W
R416	150239	RSTR 100 1/2W
R418	150215	RSTR 10 1/2W
R419	150622	RSTR 330K 1W
R420	150062	RSTR 1.0K
R422	150098	RSTR 33K
R423	150058	RSTR 680
R424	150319	RSTR 220K 1/2W

R425	150331	RSTR 680K 1/2W
R426	150315	RSTR 150K 1/2W
R427	150327	RSTR 470K 1/2W
R428	150506	RSTR 4.7 1W
R429	150311	RSTR 100K 1/2W
R430	150110	RSTR 100K
R431	150086	RSTR 10K
R432	150070	RSTR 2.2K
R501	150305	RSTR 56K 1/2W
R502	150315	RSTR 150K 1/2W
R503	150315	RSTR 150K 1/2W
R504	150351	RSTR 4.7M 1/2W
R600	150082	RSTR 6.8K
R601	150117	RSTR 200K
R602	150075	RSTR 3.6K
R603	150075	RSTR 3.6K
R604	150106	RSTR 68K
R605	150086	RSTR 10K
R606	150263	RSTR 1K 1/2W
R607	150086	RSTR 10K

CAPACITORS

C100	140701	CPTR .33MF 125V
C100#2	140702	CPTR .33MF 300V
C103	140115	CPTR 5000PF 3KV CD
C104	140112	CPTR 1000PF 1KV CD
C105	140112	CPTR 1000PF 1KV CD
C106	140112	CPTR 1000PF 1KV CD
C107	140112	CPTR 1000PF 1KV CD
C108	140417	CPTR 300MF 200V EL
C108#2	140418	CPTR 150MF 450V EL
C109	140409	CPTR 470MF 50V EL
C111	140115	CPTR 5000PF 3KV CD
C112	140115	CPTR 5000PF 3KV CD
C116	140412	CPTR 150MF 100V EL
C117	140505	CPTR .22MF 630V MY
C118	140413	CPTR 1000MF 16V EL
C120	140414	CPTR 2200MF 10V EL
C122	140415	CPTR 470MF 10V EL
C124	140413	CPTR 1000MF 16V EL
C126	140404	CPTR 100MF 50V EL
C127	140112	CPTR 1000PF 1KV CD
C128	140112	CPTR 1000PF 1KV CD
C129	140112	CPTR 1000PF 1KV CD
C130	140405	CPTR 4.7MF 50V EL
C132	140200	CPTR 220PF 1KV TS
C133	140200	CPTR 220PF 1KV TS
C134	140507	CPTR 2MF 50V MY
C135	140705	CPTR 2200PF 600V PP
C135#2	140712	CPTR .001MF 2KV PP
C136	140404	CPTR 100MF 50V EL
C137	140416	CPTR 100MF 16V EL
C138	140018B	CPTR 6800PF 33V PS

C139	140208	CPTR 680PF 1KV CD
C140	140112	CPTR 1000PF 1KV CD
C141	140420	CPTR 10MF 50V EL
C142	140403	CPTR 3.3MF 50V EL
C143	140403	CPTR 3.3MF 50V EL
C144	140508	CPTR .01MF 100V MY
C145	140112	CPTR 1000PF 1KV CD
C146	140403	CPTR 3.3MF 50V EL
C200	140503	CPTR .001MF 100V MY
C202	140013	CPTR .22MF 100V MY
C204	140405	CPTR 4.7MF 50V EL
C205	140421	CPTR 470MF 16V EL
C206	140416	CPTR 100MF 16V EL
C208	140405	CPTR 4.7MF 50V EL
C209	140403	CPTR 3.3MF 50V EL
C210	140201	CPTR 270PF 1KV TS
C211	140404	CPTR 100MF 50V EL
C213	140404	CPTR 100MF 50V EL
C214	140406	CPTR 1MF 50V EL
C215	140421	CPTR 470MF 16V EL
C300	140416	CPTR 100MF 16V EL
C301	140407	CPTR 10MF 100V EL
C302	140207	CPTR 390PF 1KV TS
C305	140202	CPTR 39PF 1KV TS
C306	140508	CPTR .01MF 100V MY
C307	140209	CPTR 330PF 1KV CD
C308	140710	CPTR 47MF 16V EL
C310	140015	CPTR 6800PF 100V MY
C311	140403	CPTR 3.3MF 50V EL
C313	140709	CPTR 2.2MF 50V EL
C400	140200	CPTR 220PF 1KV TS
C401	140014	CPTR .1MF 100V MY
C402	140502	CPTR .033MF 100V MY
C403	140419	CPTR 220MF 16V EL
C404	140408	CPTR 22MF 16V EL
C405	140107	CPTR 5000PF 1KV CD
C406	140112	CPTR 1000PF 1KV CD
C407	140015	CPTR 6800PF 100V MY
C408	140406	CPTR 1MF 50V EL
C409	140018B	CPTR 6800PF 33V PS
C410	140700	CPTR 8200PF 1.2KV PP
C411	140200	CPTR 220PF 1KV TS
C414	140112	CPTR 1000PF 1KV CD
C415	140600	CPTR .82MF 200V PC
C416	140107	CPTR 5000PF 1KV CD
C417	140107	CPTR 5000PF 1KV CD
C419	140505	CPTR .22MF 630V MY
C421	140504	CPTR .047MF 400V MY
C422	140014	CPTR .1MF 100V MY
C501	140205	CPTR .02MF 1KV CD
C502	140505	CPTR .22MF 630V MY
C600	140503	CPTR .001MF 100V MY
C601	140130	CPTR .047MF 16V CD
C602	140422	CPTR 3.3MF 50V EL

OTHER

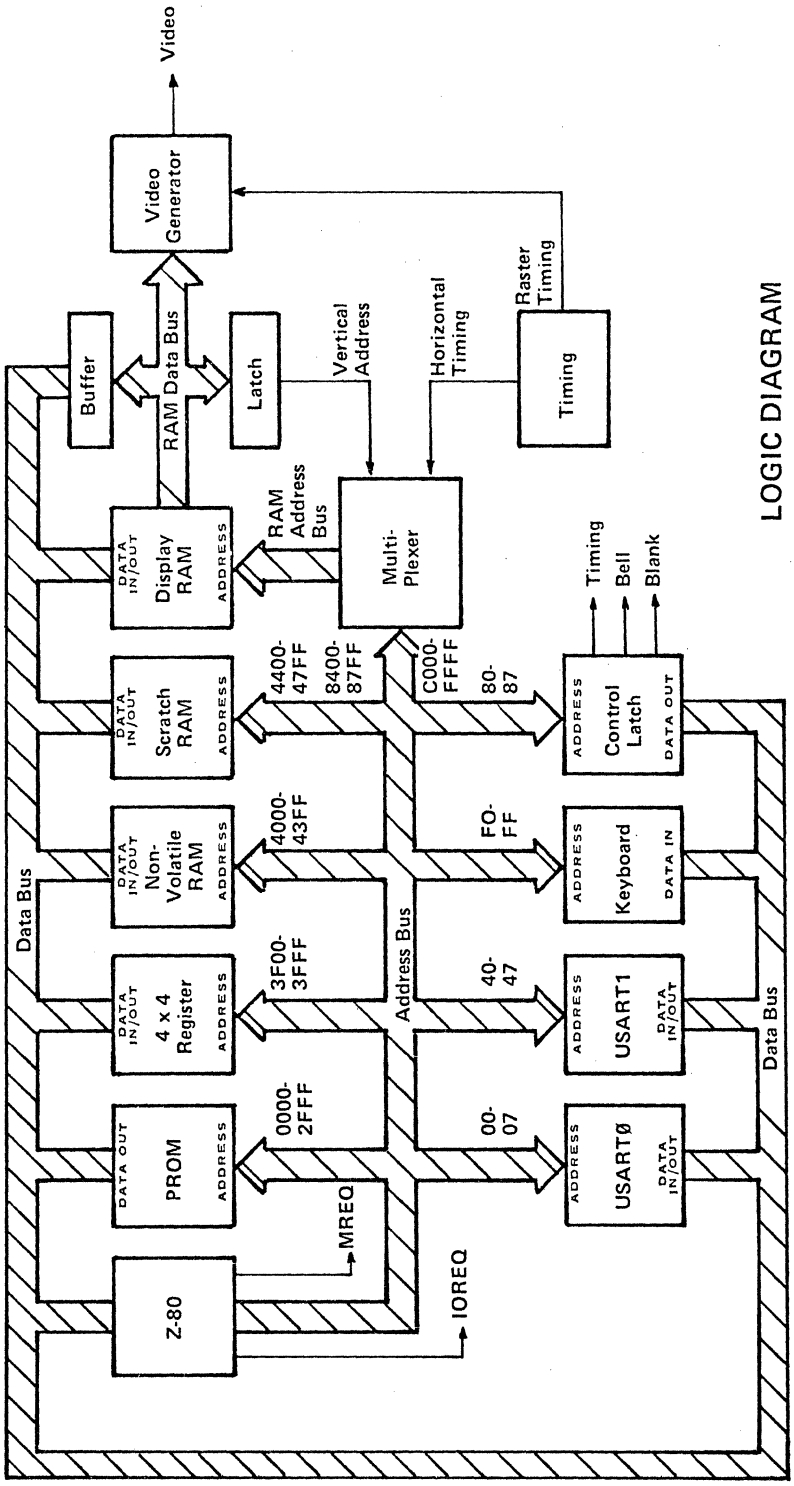
CR600	070051	TRANSDUCER
L300	131029	COIL 8.2uH
L302	131028	COIL 220uH
L406	131073	WIDTH COIL
L407	131072	LIN COIL
T100	131036	XFMR 110V
T100#2	131037	XFMR 220V
T400	131041	HVDR XFMR
T401	131070	FLYBK 18.6
	210400	S/A TUBE 4N071 (P4 CRT w/ yoke)
	210401	S/A TUBE 39N071 (P39 CRT w/ yoke)

LOGIC

The Ambassador logic board is composed of two PC cards. P/N 210303 is the main logic board (see drawings 201197). Sheets #1-3 are Schematic drawings of the board. Sheet #4 is an Assembly drawing showing component locations. P/N 210304 is a daughter board that mounts on the main logic board. It contains the I/O circuits and some non-volatile memory (see drawings 201199). Sheet #1 is a Schematic drawing of the board. Sheet #2 is the Assembly drawing.

A block diagram of the logic is shown on the next page. The theory of operation that follows is organized around this diagram. Each section of the description references the applicable sheet of the schematic.

LOGIC DIAGRAM



MEMORY ADDRESSING (201197 sht 3).

The memory decoder (9D) divides the 16-bit memory address space into 4 equal (16K byte) segments. See memory map below. A second decoder (9E) further subdivides the low-order segment into 4K-byte segments as shown.

0000-0FFF	PROM #1 (3F)
1000-1FFF	PROM #3 (6F)
2000-2FFF	PROM #2 (5F)
3000-3EFF	Not used
3F00-3FFF	4x4 Register (7B)
4000-43FF	Non-volatile RAM (16H,18H)
4400-47FF	Scratch RAM (17H,19H)
4800-7FFF	Not used
8000-83FF	Not used
8400-87FF	Scratch RAM (8F)
8800-BFFF	Not used
C000-FFFF	Display RAM (3E,4E,5E,6E,7E,8E)

PROM READ (201197 sht 3). Three ROM/PROM locations (6F, 5F, 3F) are provided. They are shown configured for 2732 PROMs (4K bytes each). They contain the Z80 program. See Manual Suplement for description.

4x4 REGISTER READ/WRITE (201197 sht 1). The register file (7B) is a 4-nybble RAM which controls the line counter (see TIMING CIRCUITS). In conjunction with the control latch (which controls the vertical counter), it provides the Z80 with control of the number of data lines displayed on the screen.

NON-VOLATILE RAM READ/WRITE (201199 sht 1). Two 1K x 4-bit CMOS RAM locations (16H, 18H) are provided. These locations are powered by a 3V lithium battery to provide the Z80 with non-volatile memory for storage of the terminal's setup parameters (ie, variables that must be retained through power off and power outages). A CMOS gate (20E) provides orderly power on/off to the CMOS RAM, as well as generating the master power-clear reset (PC*) to the rest of the logic following power-on.

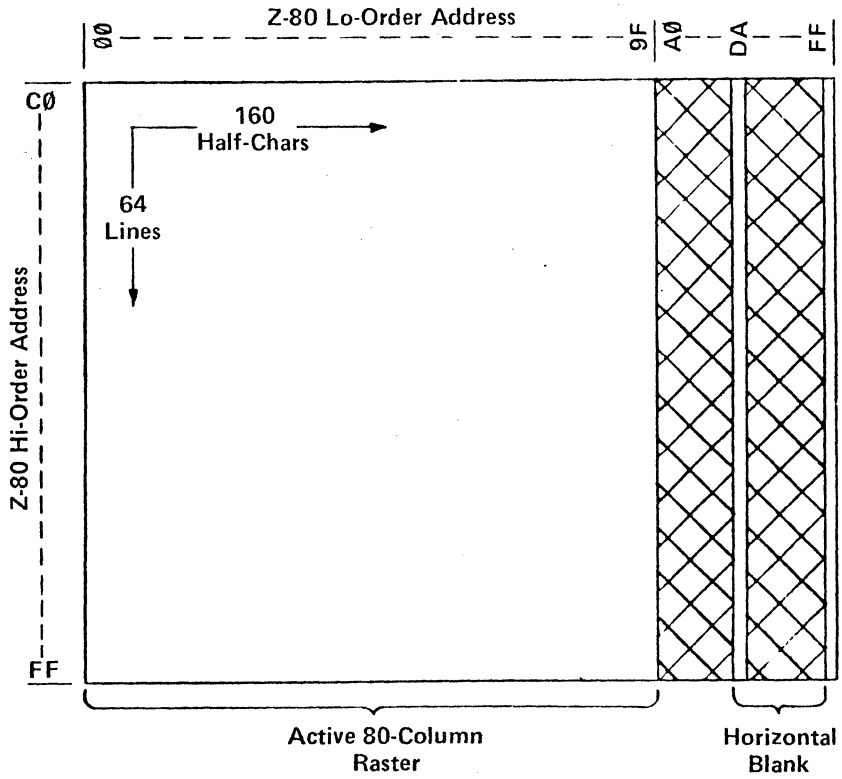
SCRATCH RAM READ/WRITE (201197 sht 3). Two 1K x 4-bit (17H, 19H) and one 1K x 8-bit (8F) static RAM locations are provided. They are used by the Z80 for working storage.

DISPLAY MEMORY READ/WRITE (201197 sht 2). The display memory is composed of six 16K x 1-bit dynamic RAMs (3E, 4E, 5E, 6E, 7E, 8E) organized as 2 (sequential) addresses per character (12 bits- 7 bits for character, 5 for character rendition). See diagram. Read/write control of the memory is multiplexed between the raster timing counters and the Z80 through four multiplexers (1E,

2E, 1D, 2D). The counters control the memory during the visible raster; the Z80 during video blank.

The high-order address bytes address display lines (up to 64 lines). The low-order bytes address (half-) characters within the line (up to 80 characters). The lines are not necessarily displayed in sequence on the screen. Address DA at the end of each line contains a pointer to the next line to be displayed. During the visible raster, it is automatically read into a latch (4D) and routed back through the multiplexers as the high-order bytes of the next read address. During video blank, the locations may be read/written by the Z80 to provide fast edting, scrolling, etc.

The memory is automatically refreshed as the data are read out to the display. As each (half-) character is read, its entire column is refreshed. The low-order addresses A0 through D9 and DC through FD are not used (and not refreshed) by the terminal. (Note: Low-order addresses FE and FF are refreshed, but are not used as additional Z80 memory since any read/write to low-order addresses E0-FF causes latch 4D to be loaded. Location DA contains the pointer to the next line. Location DB contains data relative to line status.)



I/O ADDRESSING (201197 sht 3).

The I/O decoder (9E) divides the 8-bit I/O address space into four equal parts: USART0 enable (UE0*), USART1 enable (UE1*), keyboard enable (RKB*), and control latch enable (WCN*).

00-3F	USART0 (16F)
40-7F	USART1 (18F)
80-BF	Control Latch (1B)
C0-FF	Keyboard Latch (11H)

USART READ/WRITE (201199 sht 1). The USARTs (16F, 18F) are Signetics 2651s. USART0 services the printer port; USART1 services the computer port. The Z80 reads/writes data and status/control from/to the USARTs at the I/O addresses shown below.

USART0	USART1	I/O OPERATION
00	40	Read Receive Holding Register
01	41	Write Transmit Holding Register
02	42	Read Status Register
03	43	Write SYN1/SYN2/DLE Registers
04	44	Read Mode Registers 1/2
05	45	Write Mode Registers 1/2
06	46	Read Command Register
07	47	Write Command Register

CONTROL LATCH WRITE (201197 sht 1). The control latch (1B) is a one-to-eight non-inverting decoder with latched outputs. It is written from DB7 (the data bus MSB). It is used for internal control functions as shown.

ADR	1B-	CONTROL FUNCTION
80	4	SET VC2. Addresses 80, 82, and 84 preset the vertical counter each frame to control the number of data lines displayed on the screen.
81	9	BELL INITIATE. 0 turns on the bell through flip-flop 1A and holds it on. 1 turns it off.
82	6	SET VC4.
83	11	INTERLACE ENABLE. 0 enables non-interlaced display by holding the frame flip-flop 2A reset. 1 enables interlaced display by permitting it to toggle.
84	5	SET VC3
85	10	BLINK TIMING. 0 blanks the video of the characters tagged for blink rendition. 1 unblanks them.
86	7	BLANK VIDEO. 0 blanks the video. 1 unblanks it.
87	12	RESET VC. 0 resets the vertical counter and holds it reset. 1 releases it to count.

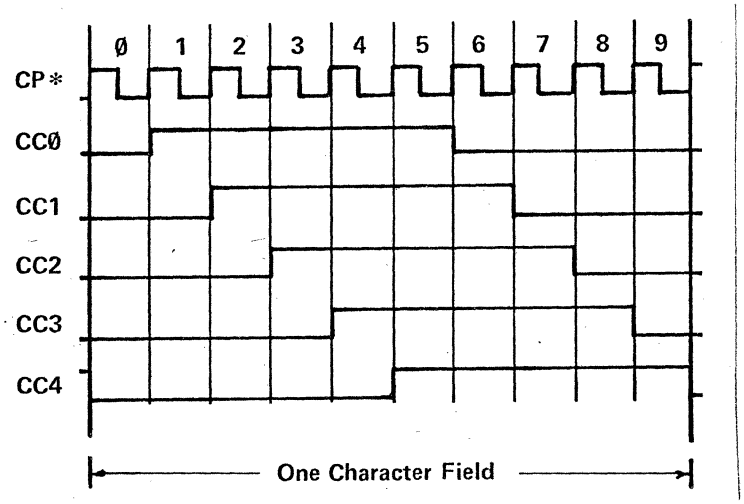
KEYBOARD READ (201197 sht 3). The keyboard contains an array of mechanical switches interconnected as a matrix of 12 rows by 8 columns. The rows are addressed through two decoders (11F,12F) with the addresses shown. The state of the keys in the addressed row are read back through a latch (11H).

Hex Address	DB							
	0	1	2	3	4	5	6	7
F2		{ [	A	B	C	D	E	F
F3	G	H	I	J	K	L	M	N
F4	O	P	Q	R	S	T	U	V
F5	W	X	Y	Z	~ \	" '	¦ \	Pause
F6	Move Up	! 1	@ 2	# 3	$ 4	% 5	^ 6	& 7
F7	* 8	(9	_ -	: ;	< ,	+ =	> .	? /
F8	Enter	ø	.	Move Down	) ø	SSA 1	↓ 2	ESA 3
F9	← 4	Home 5	→ 6	T-Clr 7	↑ 8	T-Set 9	Reset	Setup
FA	PF1	PF2	PF3	Back Space	PF4	Break	PF5	PF6
FB	Del	PF7	PF8	PF9	PF10	PF11	PF12	Erase
FC	Edit	Line Feed	Delete	}]	Insert	Print	Return	Send
FF	Caps Lock	Space Bar	← Tab →	Ctrl	Esc	Shift	Shift	

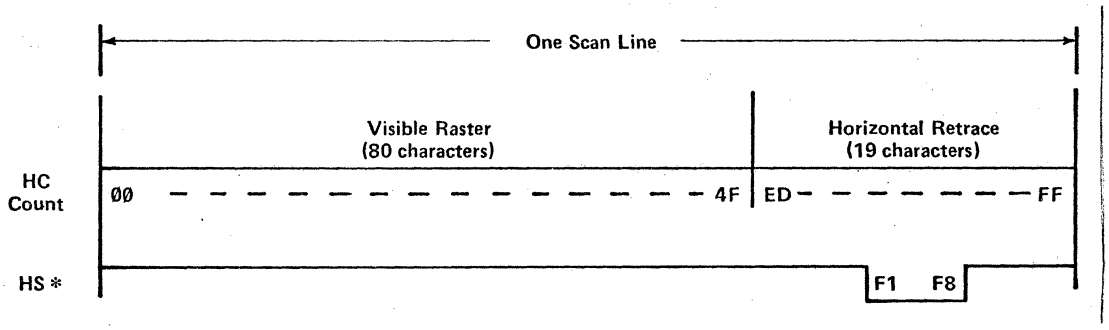
TIMING CIRCUITS (201197, sht 1).

The timing circuits provide a time base for the terminal over 2 video frames (for interlaced operation) in increments of the dot clock (one dot time on the screen). They provide horizontal and vertical sync to the monitor, timing and blanking to the video generation circuits, and miscellaneous logic signals.

CHARACTER COUNTER. The character counter (12C, 11C) counts dot times modulo 10 to define a 10-dot-wide character field. The gate (11B) ensures that the counter comes up in a legal state.



HORIZONTAL COUNTER. The horizontal counter (1C, 2C) counts character fields (CC4*) modulo 99 to define the scan line at 99 character counts wide. The visible portion of the scan line contains 80 character counts; the counter reads 00 (left-most character field) to 4F (right-most character field). At the end of count 4F, the counter is synchronously preset to ED (ie, -19) to provide 19 character counts for horizontal retrace. The horizontal sync (HS*) for the monitor is decoded at counts F1 through F8.



LINE COUNTER. The line counter (6B) counts scan lines in groups of from 2 to 9 lines as determined by the 4x4 register file (7B). The last line in each group is marked by the signal LOF* (LC count 0), at the end of which the counter synchronously presets to the next value read from the register. The value preset is 17 minus the number of scan lines required in the group. The number of scan lines required is a function of whether the monitor is being driven non-interlaced or interlaced and the vertical position of the sweep.

During non-interlaced operation:

7B-4/5 = 1/0 during the top portion of each character field and the 1st portion of vertical blank. Output from the register during this period is the number of scan lines in the bottom portion of the character field and the 2nd half of vertical balnk (=8).

7B-4/5 = 0/0 during the bottom portion of each character field (except the last scan line of the last character line) and the 2nd portion of vertical blank. Register output is the number of scan lines in the top portion of the character field (=2, 3, 4, 5, 6, 7, or 8).

7B-4/5 = 0/1 during the last scan line before vertical blank. Register output is the number of scan lines in the 1st half of vertical blank (=3, 4, or 5).

During interlaced operation:

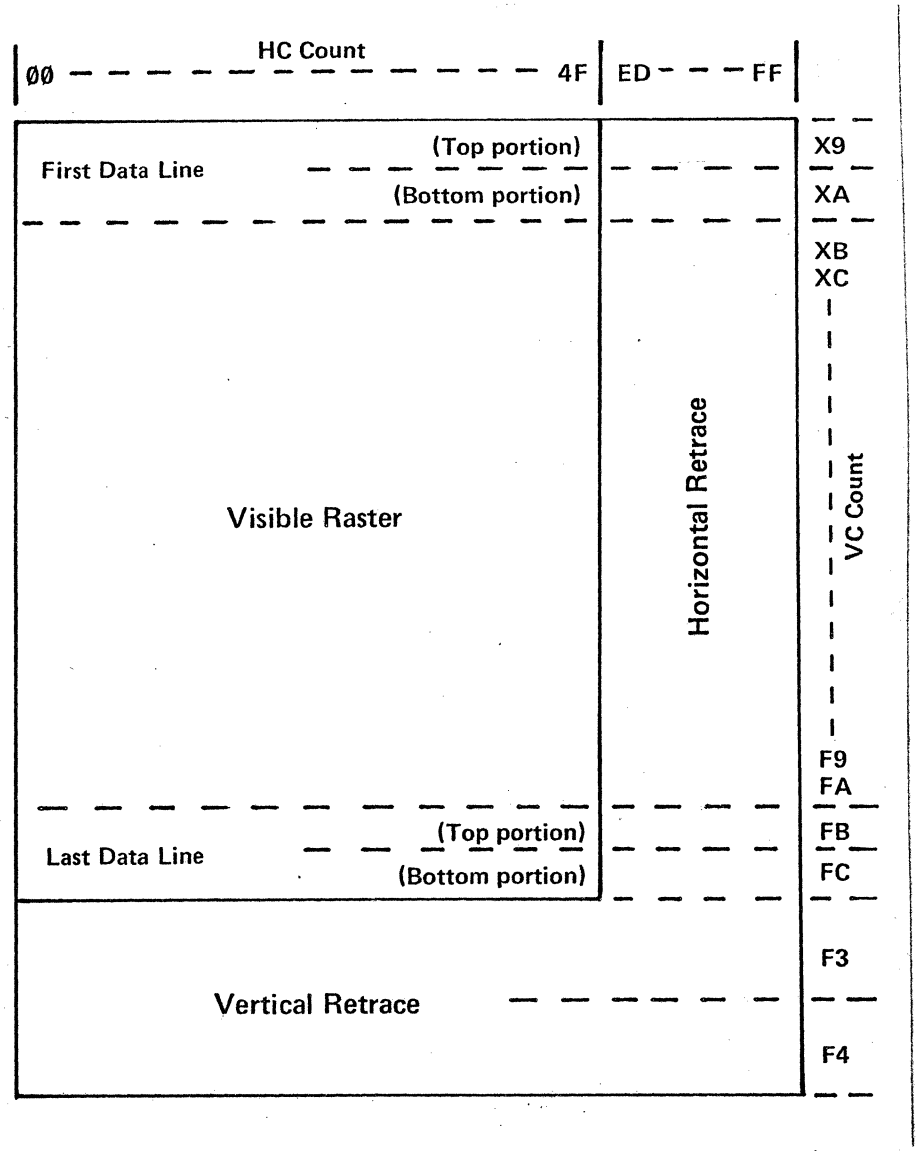
7B-4/5 = 0/0 during the visible raster (except the last scan line) and the 2nd portion of vertical blank. The output of the register during this period is the number of scan lines in the character field (=5, 6, 7, or 8).

7B-4/5 = 0/1 during the last scan line in the visible raster. Register output is the number of scan lines in the 1st portion of vertical blank (=3, 4, or 5).

7B-4/5 = 1/0 during Frame 0 sync. Register output is the number of scan lines in the 2nd portion of Frame 0 vertical blank (=8 or 9).

7B-4/5 = 1/1 during Frame 1 sync. Register output is the number of scan lines in the 2nd portion of Frame 1 vertical blank (=8 or 9).

VERTICAL COUNTER. The vertical counter (2B, 3B) counts the groups of scan lines (LOF* from the line counter) to define the frame (ie, one vertical sweep through the raster). The low-order counter (3B) counts mod 4 (9-A-B-C) during the visible portion of the raster and mod 2 (3-4) during vertical blank. The high-order counter (2B) counts mod 16 but is preset at the end of count F to a value determined by the control latch (1B). The value preset is 15 minus half the number of (non-interlaced) data lines displayed. The minimum number of lines displayable is 18 and the maximum is 30. During interlaced display, an additional flip-flop (2A) is toggled at the end of count F4 to define frame count 0 or 1. Vertical sync is decoded by a flip-flop (2A) as count F3 (frame 0) or count F3 delayed by one-half scan line (frame 1).



VIDEO GENERATION (201197 sht 2). The video generation circuits are shown at the bottom of sheet 2. The data to be displayed (stored as half-characters, ie, 2 addresses per character, in display memory) are read into the video generation circuits during video unblank (ie, during the active raster). A full data line of characters are read through the circuits during each scan line.

The first half of each character is read into a latch (6D) near mid-character-time (at the end of CC count 5). The second half of the character is read into another latch (4C) at the end of the character time (at the end of CC count 9). Simultaneously, the first half is copied from latch 6D into a third latch (7D) providing the full 12-bit-wide character in parallel during the following character time.

The character portion of the data (6 bits from latch 4C and 1 bit from latch 7D), form the high-order 7-bits of address to the character generator ROM (6C). The ROM contains a dot-matrix representation of each displayable character (up to 128) in an (up to) 8 x 8 font. The 3 low-order bits of address are derived from the line counter and determine which of the 8 lines of the font are required. During CC count 7, this line is strobed into the video shift register (8C) to be shifted out in synchronism with the dot clock (CP*) as video.

While the character portion of the data is being decoded through the ROM, the rendition portion is held in latch 7D. At the same time as the font line is strobed into the video shift register, this data is copied from latch 7D to a fourth latch (8D) where it is held for one character time to operate on the video bit stream coming from the register to effect the specified rendition.

A logic 1 from pin 7 (of latch 8D) specifies "blink". It permits a firmware-generated timing signal to pass through a gate (13D) to selectively inhibit/enable passage of the video bit stream through a gate (11B).

A logic 0 from pin 12 specifies "security". It inhibits passage of the video through a gate (11B), preventing its display.

A logic 1 from pin 2 specifies "reverse". It inverts the video through a gate (12D) causing display of a black image on a green background.

A logic 1 from pin 10 specifies "underline". The multiplexer (9D) gates it with two timing signals that limit it to the last scan line of the character field, which is then OR'ed into the video through a gate (13D).

A logic 0 from pin 5 specifies "bold". It is delayed one dot time through a flip-flop (12E) to line it up with the video which has been re-clocked through the other flip-flop (12E), and controls a resistor divider which increases the video amplitude at the base of the video drive transistor (Q2).

The video is then passed to the monitor electronics, with the separately derived horizontal and vertical syncs, for display on the screen.

MNEMONICS

*	Not (Indicates active low.)
BLE	Blink Enable
CAS*	Column Address Strobe
CC0-CC4	Character Count 0 thru 4
CP*	Clock Pulse
CS4*	Chip Select 4
CS8*	Chip Select 8
CTS	Clear To Send
CUB 81	Column Unblank 81
DB0-DB7	Data (bus) Bit 0 thru 7
DCAS*	Display Column Address Strobe
DE	Display Enable (Video Blank)
DLUB	Delayed Line Unblank
DRAS*	Display Row Address Strobe
DRE*	Display Ram Enable
DSR	Data Set Ready
HC0-HC6	Horizontal Count 0 thru 6
HOV	Horizontal Overflow
HS*	Horizontal Sync
IEN	Interlace Enable
INT*	Interupt (Indicates to Z80 that I/O needs to be serviced following instruction currently being executed.)
IORQ*	Input/Output Request (Indicates that lower half of address bus holds a valid I/O address for read or write by Z80. It is generated when an interupt is being acknowledged.)
KR0*-KR7*	Keyboard Receive 0 thru 7
KS	Keyboard Strobe (For use with encoded keyboard input.)
KSL0*-KSL7*	Keyboard Send Line 0 thru 7
LC1-2	Line Count 1 and 2
LOF*	Last Of Field
LUB*	Line Unblank
M1*	Machine Cycle 1 (Indicates that Z80 is in machine cycle 1 or the fetch cycle.)
MLC4-6	Multiplexed Line Count 4 thru 6
MREQ*	Memory Request (Indicates that the address bus holds a valid address for memory read or write.)
NMI*	Non-Maskable Interupt (Has higher priority than Interupt.)
PC	Power on Clear (Initial reset.)
RADR0-6	Ram Address 0 thru 6
RAS*	Row Address Strobe
RCLD*	Row Count Load
RCLE	Row Count Load Enable
RD*	Read (Indicates that Z80 wants to read memory.)
RDB0-5	Ram Data (bus) bit 0 thru 5
RE3*	Register Enable 3000
RFSH*	Refresh (Indicates that the lower 7 bits of the address bus contains a refresh address for dynamic memory. This operation automatically takes place during the fetch cycle.)
RKB*	Read Keyboard
RTS	Ready To Send
RW*	Read/Write
RWR*	Ram Write
RXD	Received Data

TXD	Transmitted Data
UE0-1*	USART Enable 0 and 1
VC0-3	Vertical Count 0 thru 3
VS*	Vertical Sync
VUB*	Vertical Unblank
WCN*	Write Contol Latch
WR*	Write (Indicates Z80 wants to write memory or I/O.)
ZADR0-15	Z80 Address 0 thru 15
ZADS	Z80 Address Strobe
ZCAS	Z80 Column Address Strobe
ZCLK*	Z80 Clock
ZRAS*	Z80 Row Address Strobe

REPLACEMENT BOARDS

210303D	S/A LGC BD 9700
210304E	S/A LGC BD 9900

INTEGRATED CIRCUITS

Z1A	180096	IC 74LS74
Z1B	180121	IC 74LS259
Z1C	180090	IC 74LS161
Z1D	180108	IC 74LS258
Z1E	180108	IC 74LS258
Z1F	180211	IC Z80A
Z2A	180096	IC 74LS74
Z2B	180090	IC 74LS161
Z2C	180090	IC 74LS161
Z2D	180108	IC 74LS258
Z2E	180108	IC 74LS258
Z3A	180071	IC 74LS04
Z3B	180090	IC 74LS161
Z3E	180203	IC TMS4116-20
Z3F	180224	IC 2732
Z4C	180091	IC 74LS174
Z4D	180091	IC 74LS174
Z4E	180203	IC TMS4116-20
Z5A	180095	IC 74LS00
Z5B	180114	IC 74LS157
Z5D	180115	IC 74LS367
Z5E	180203	IC TMS4116-20
Z5F	180224	IC 2732
Z6A	180124	IC 74LS27
Z6B	180090	IC 74LS161
Z6C	180226	IC ROM 508A
Z6D	180091	IC 74LS174
Z6E	180203	IC TMS4116-20
Z6F	180224	IC 2732
Z7A	180086	IC 74LS10
Z7B	180127	IC 74LS170
Z7D	180091	IC 74LS174
Z7E	180203	IC TMS4116-20
Z8F	180227	IC 4016
Z8A	180087	IC 74LS32
Z8B	180096	IC 74LS74
Z8C	180097	IC 74LS166
Z8D	180091	IC 74LS174
Z8E	180203	IC TMS4116-20
Z9A	180085	IC 74LS08
Z9B	180087	IC 74LS32
Z9D	180117	IC 74LS139
Z9E	180117	IC 74LS139
Z10A	180123	IC 74LS02
Z10H	180123	IC 74LS02
Z11B	180086	IC 74LS10
Z11C	180096	IC 74LS74

Z11D	180126	IC 74LS51
Z11E	180114	IC 74LS157
Z11F	180125	IC 74LS145
Z11H	180122	IC 74LS374
Z12B	180071	IC 74LS04
Z12C	180092	IC 74LS175
Z12D	180116	IC 74LS86
Z12E	180096	IC 74LS74
Z12F	180125	IC 74LS145
Z13C	180096	IC 74LS74
Z13D	180095	IC 74LS00
Z13E	180085	IC 74LS08
Z14D	180129	IC 75189A
Z14F	180102	IC 75188
Z15D	180071	IC 74LS04
Z15F	180102	IC 75188
Z16F	180209	IC 2651
Z16H	180205	IC D444
Z17H	180204	IC 2114
Z18D	180124	IC 74LS27
Z18F	180209	IC 2651
Z18H	180205	IC D444
Z19H	180204	IC 2114
Z20E	180128	IC 4011

TRANSISTORS

Q1	170027	XSTR MPSA20
Q2	170027	XSTR MPSA20
Q101	170027	XSTR MPSA20

DIODES

D1	160004	DIODE 1N4148
D3	160055	DIODE TVS505
D4	160055	DIODE TVS505
D5	160055	DIODE TVS505
D6	160056	DIODE 12V
D7	160055	DIODE TVS505
D9	160055	DIODE TVS505
D101	160065	DIODE 1N4734A 5V
D102	160004	DIODE 1N4148
D103	160004	DIODE 1N4148
D104	160004	DIODE 1N4148
D105	160004	DIODE 1N4148
D106	160004	DIODE 1N4148
D107	160055	DIODE TVS505

RESISTORS (All rstrs 1/4W)

RV1	150925	TMPT 5K
RV101	150909	TMPT 50K

R1	150068	RSTR 1.8K
R2	150100	RSTR 39K
R3	150086	RSTR 10K
R4	150086	RSTR 10K
R5	150086	RSTR 10K
R6	150022	RSTR 22
R7	150062	RSTR 1.0K
R8	150034	RSTR 68
R10	150046	RSTR 220
R11	150082	RSTR 6.8K
R12	150082	RSTR 6.8K
R13	150082	RSTR 6.8K
R14	150082	RSTR 6.8K
R15	150082	RSTR 6.8K
R16	150082	RSTR 6.8K
R17	150082	RSTR 6.8K
R18	150082	RSTR 6.8K
R19	150086	RSTR 10K
R20	150086	RSTR 10K
R21	150086	RSTR 10K
R22	150050	RSTR 330
R23	150086	RSTR 10K
R101	150100	RSTR 39K
R102	150062	RSTR 1.0K
R103	150090	RSTR 15K
R104	150110	RSTR 100K
R105	150134	RSTR 1.0M
R106	150117	RSTR 200K
R107	150058	RSTR 680
R112	150086	RSTR 10K
R114	150086	RSTR 10K
R115	150082	RSTR 6.8K
R116	150014	RSTR 10
R117	150034	RSTR 68
R118	150038	RSTR 100
R122	150086	RSTR 10K
R124	150086	RSTR 10K
R125	150082	RSTR 6.8K
R126	150014	RSTR 10
R127	150034	RSTR 68
R128	150038	RSTR 100

CAPACITORS

C1	140210	CPTR 120PF 1KV CD
C3	140101	CPTR 68PF 1KV CD
C5	140200	CPTR 220PF 1KV TS
C6	140130	CPTR .047MF 16V CD
C8	140106	CPTR 820PF 1KV CD
C9	140106	CPTR 820PF 1KV CD
C10	140130	CPTR .047MF 16V CD
C11	140130	CPTR .047MF 16V CD
C12	140130	CPTR .047MF 16V CD
C13	140130	CPTR .047MF 16V CD

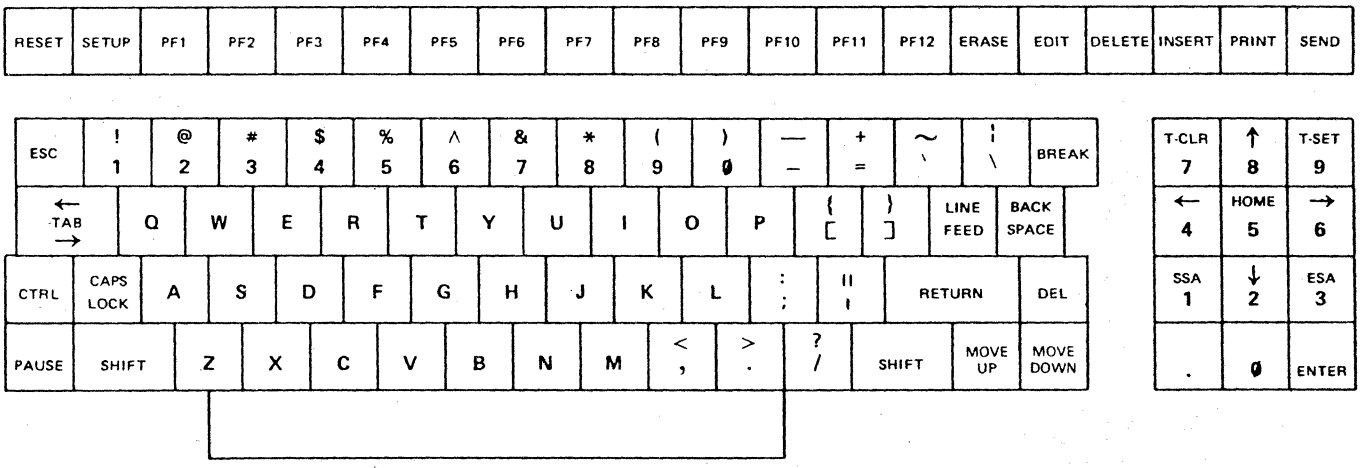
C14	140130	CPTR .047MF 16V CD
C15	140130	CPTR .047MF 16V CD
C16	140130	CPTR .047MF 16V CD
C17	140130	CPTR .047MF 16V CD
C18	140130	CPTR .047MF 16V CD
C19	140130	CPTR .047MF 16V CD
C20	140130	CPTR .047MF 16V CD
C21	140130	CPTR .047MF 16V CD
C22	140130	CPTR .047MF 16V CD
C23	140130	CPTR .047MF 16V CD
C24	140408	CPTR 22MF 16V EL
C25	140408	CPTR 22MF 16V EL
C26	140130	CPTR .047MF 16V CD
C27	140130	CPTR .047MF 16V CD
C28	140408	CPTR 22MF 16V EL
C29	140130	CPTR .047MF 16V CD
C30	140130	CPTR .047MF 16V CD
C31	140408	CPTR 22MF 16V EL
C101	140200	CPTR 220PF 1KV TS
C102	140406	CPTR 1MF 50V EL
C103	140405	CPTR 4.7MF 50V EL
C104	140200	CPTR 220PF 1KV TS
C105	140200	CPTR 220PF 1KV TS
C106	140130	CPTR .047MF 16V CD
C107	140130	CPTR .047MF 16V CD
C109	140130	CPTR .047MF 16V CD
C123	140130	CPTR .047MF 16V CD
C125	140130	CPTR .047MF 16V CD
C126	140130	CPTR .047MF 16V CD
C127	140130	CPTR .047MF 16V CD
C128	140408	CPTR 22MF 16V EL
C129	140408	CPTR 22MF 16V EL
C130	140408	CPTR 22MF 16V EL

OTHER

X1	132024	XTAL 18.414MHZ
X101	132021	XTAL 5.068MHZ
	070050	BATTERY 3V LITHIUM

KEYBOARD. The Ambassador keyboard is composed of several mechanical switch arrays. The switches are interconnected in a 12-row by 8-column matrix (see diagram) and routed by an integral flat-cable to the Keyboard connector on the Logic board. The microprocessor on the Logic board scans the keyboard by addressing the rows and reading the columns to determine which keys are depressed (see Logic board description). The keyboard contains no electronics except for blocking diodes at several of the bottom-row switch positions. The keyboard is supplied in both E-case (p/n 210269) and D-case (p/n 210256) packaging.

KEYBOARD LAYOUT



SWITCH INTERCONNECT. Closure at the designated switch positions is sensed across the designated Keyboard connector pins.

Conn Pin	W	X	Y	Z	AA	BB	CC	DD
T		{ [	A	B	C	D	E	F
S	G	H	I	J	K	L	M	N
N	O	P	Q	R	S	T	U	V
M	W	X	Y	Z	~ `	" '	: \	Pause
L	Move Up	! 1	@ 2	# 3	$ 4	% 5	^ 6	& 7
K	* 8	(9	— -	: ;	< ,	+ =	> .	? /
J	Enter	0	.	Move Down	) 0	SSA 1	↓ 2	ESA 3
H	← 4	Home 5	→ 6	T-Clr 7	↑ 8	T-Set 9	Reset	Setup
F	PF1	PF2	PF3	Back Space	PF4	Break	PF5	PF6
E	Del	PF7	PF8	PF9	PF10	PF11	PF12	Erase
D	Edit	Line Feed	Delete	}]	Insert	Print	Return	Send
A	Caps Lock	Space Bar	← Tab →	Ctrl	Esc	Shift	Shift	

KEYBOARD CONNECTOR
(Plug side shown)

B-D-F-J-L-N-R-T-V-X-Z-BB-DD
A-C-E-H-K-M-P-S-U-W-Y-AA-CC
--- Cable ---

COMPUTER CABLE

The Computer cable (p/n 210225) configures the terminal as RS232 Data Terminal Equipment (DTE) for interface with RS232 Data Communications Equipment (DCE) such as a computer, modem, coupler, etc. The small connector plugs into the lower connector (P4) on the Logic daughter board (Communications I/O port).

CONNECTORS (wiring side shown)

```
        *****     -Key
Pt    B-D-F-J-L
      A-C-E-H-K


Pe    13--12--11--10--9--8--7--6--5--4--3--2--1
        25--24--23--22-21-20-19-18-17-16-15-14
```

INTERCONNECT

Pt	COLOR	Pe	SIGNAL
A	BRN	20	DATA TERMINAL READY. Control output from terminal. The terminal holds this line in the 'on' condition.
B	GRN	3	RECEIVED DATA. Data input to terminal.
D	RED	5	CLEAR TO SEND. Control input to terminal. An 'off' condition on this pin causes the terminal to disable or suspend transmission. An 'on' condition causes it to enable or resume transmission. The terminal recognizes no connection at the interface (ie, open) as an 'on' condition.
E	BLU	4	REQUEST TO SEND. Control output from terminal. The terminal holds this line in the 'on' condition.
K	BLK	7	SIGNAL GROUND.
L	WHT	2	TRANSMITTED DATA. Data output from terminal.

PRINTER CABLE

The Printer cable (p/n 210163) configures the terminal as RS232 Data Communication Equipment (DCE) for interface with RS232 Data Terminal Equipment (DTE) such as a printer. The small connector plugs into the upper connector (P5) on the Logic daughter board (Printer I/O port).

CONNECTORS (wiring side shown)

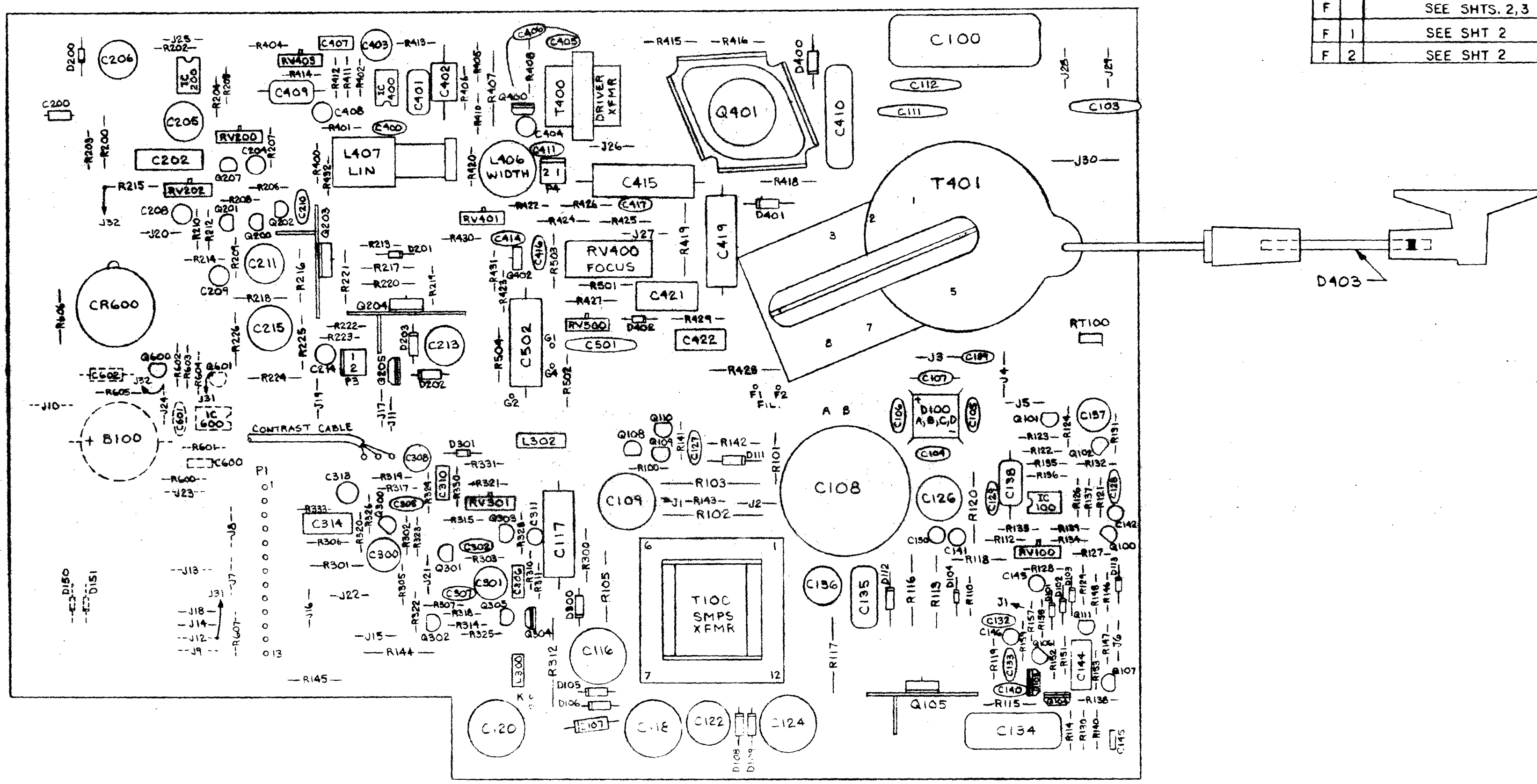
```
        *****     -Key
Pt    B-D-F-J-L
      A-C-E-H-K


Pe    1--2--3--4--5--6--7--8--9--10--11--12--13
       14-15-16-17-18-19-20-21-22--23--24--25
```

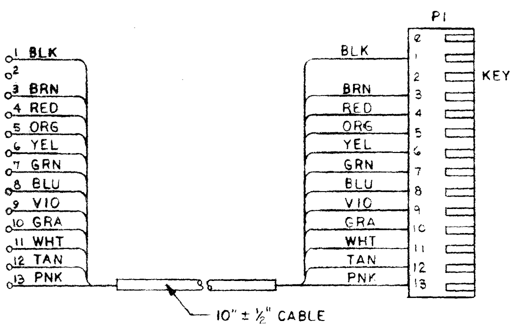
INTERCONNECT

Pt	COLOR	Pe	SIGNAL
A	BRN	6	DATA SET READY. Control input to the printer. The terminal holds this line in the 'on' condition.
B	GRN	2	TRANSMITTED DATA. Data output from the printer. The terminal recognizes DC3 as a command to disable or suspend printing and DC1 to enable or resume printing. It ignores all other codes.
D	RED	20	DATA TERMINAL READY. Control output from the printer. An 'off' condition on this pin causes the terminal to disable or suspend printing. An 'on' condition causes it to enable or resume printing. The terminal recognizes no connection at the interface (ie, open) as an 'on' condition.
E	BLU	8	CARRIER DETECT. Control input to the printer. The terminal holds this line in the 'on' condition.
K	BLK	7	SIGNAL GROUND.
L	WHT	3	RECEIVED DATA. Data input to printer.

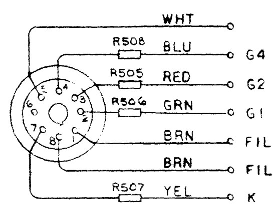
PART NUMBER 201185F

LET	R	REVISION	DATE	DRN	CHK	ENG
D	2	ADDED J30. MOVED SOME COMPONENTS TO INCREASE FOIL SPACING.	7-30-80	G.S.		
D	3	SEE SHTS. 2,3	9-10-80	G.S.		
E		SEE SHT 3	12-3-80	G.S.		
F		SEE SHTS. 2,3	2-19-81	G.S.		
F	1	SEE SHT 2	5-21-81	G.S.		
F	2	SEE SHT 2	5-26-81	G.S.		





DETAIL A
TERMINAL BD



DETAIL B
CRT SOCKET

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES

TOLERANCES
.X = ±
.XX = ±
.XXX = ±
ANGLES = ±
CHAMFER = ±

REMOVE ALL BURRS AND SHARP EDGES RADII AND FILLETS .010 TO .020

DO NOT SCALE THIS DRAWING

MATERIAL

FINISH

NAME	G.S.				
DATE	3-3-80				
BY	DRAWN	CHECKED	MECH ENGR	ELEC ENGR	APPROVED

ANN ARBOR TERMINALS INC
6107 JACKSON ROAD • ANN ARBOR, MICHIGAN 48103 • 313-769-0926

MONITOR BD

SIZE C — PART NUMBER 201185F

SCALE — WT — SHEET 1 OF 3

PART NUMBER 2011851						
LET	R	REVISION	DATE	DRN	CHK	ENG
J	2	[illegible]	10-22-79	[illegible]		[illegible]
H	3	R107 WAS 10K, R145 WAS .25W	7-13-79	[illegible]		[illegible]
G		SEE SHT 3	5-4-79	[illegible]		[illegible]
F		R102 WAS 68K, R103 WAS 33K	4-19-79	[illegible]		[illegible]
E	1	FIG (230V OPTION) WAS ADDED	3-21-79	[illegible]		[illegible]
D	2	REVISED BELL OPTION	2-26-79	[illegible]		[illegible]

P1 TERMINAL BD. CONNECTOR

1 VIDEO IN
2 NC
3 NC
4 -12V
5 -5V
6 COMP BLANK IN
7 +5V (J13)
8 +12V TO R200, R215, J20 +12V (J16)
9 HORZ SYNC IN
10 GND TO BELL OPTION (J7, J8) GND
11 VERT SYNC IN (J14)
12 BATTERY (J12)
13 BELL ENABLE* BELL ENABLE

120V USA OR 230V EUROPE 0 TO 400HZ INPUT
BLK (230V=BRN)
WHT (230V=BLU)
GRN (230V=GRN/YEL)
CHASSIS PAN
F100 1.5A SLOW BLOW
S-100
C100 .33 125 VAC U.L. 230V=300VAC V.D.E.
L100
J28 J29
C103 .005 3KV
C112 .005 3KV
C111 .005 3KV
J30
RT100 2D304 MIDWEST COMPONENTS
C104 .001 1KV
C105 .001 1KV
D100 A,B,C,D VARO VS447 ATLANTIC SEMI BR-34 BRIDGE
C106 .001 1KV
C107 .001 1KV
C108 300µf 200V 230V=150µf 450V
R101 150K .5W 230V=330K .5W
R102 22K 2W(CGW) 230V=47K 3W(CGW)
R103 15K 3W (CGW) 230V=47K 3W (CGW)
J1 TO D113 CATHODE
Q108 MPSA70
Q109 MPSA20
Q110 MPSA20
R100 68K 230V=33K
R141 10K
R142 100 .5W
C109 470µf 50V
+30V SOURCE
J2
C126 100µf 50V
C127 .001
D111 BY206
R143 2.2
T-100 115V=131036 230V=131037
225mA
D105, BY206 — R105 4.7 1W — C116 150 100V — C117 22 630V — +70V SOURCE
D106, MR810 — J15 J16 — C118 1000 16V — +12V SOURCE
D107, MR850 — R144 .47 1W — C120 2200 10V — +5V SOURCE
COLD GND
D108, MR810 — R145 22 .5W — C122 470 10V — -5V SOURCE
D109, MR810 — C124 1000 16V — -12V SOURCE
R110 68
D104 BY206
C130 4.7µf 50V 20%
POWER SUPPLY SYNC INPUT FROM T401
B J3 C139 680pf J4 J5
A
+30V
R120 1K 1W
R124 680
Q101 MPSA70
R122 15K 5%
R123 270
+8.5V REG. SOURCE
C137 100µf 16V
REF 2V
COMP
C138 .005µF 5% polystyrene
TO IC100 PIN 6
IC100B MC1391
PWM
R118 2.2K .5W
R119 270
C132 220pf X5E
C133 2.2pf X7E
C104 NSDU56
R113 180 2W(CGW) 230V=150 1W
Q103 MPSU07
C134 2µf 50V SPRAGUE 225P
C140 .001
R115 47 .5W
R114 22 230V=6E
D112 BY206
R116 1K 2W (CGW) 230V=2.47K, 3W IN PARALLEL
C135 .0022µf 1000V
R117 2.6 3W (CGW) 230V=5 5W (CGW)
C136 100µf 50V
R126 680K
R137 100
C142 3.3µf 20% 50V
R132 10K
R131 39K
C128 .001
R121 150K
C129 .001
R135 1K
R136 470K
G102 MPSA20
C141 10µf 20% 50V
R133 470
R112 6.2K
RV100 100 V ADJ
R134 330
R127 390
J1 TO R100, R103
+24V REG
D113 IN4749 24V
C143 3.3µf 50V
R146 15K
Q111 MPSA70
R148 2.2
R147 10K
D102 IN4148
D103 IN4148
R139 4.7K
R128 82K
R129 15K
Q100 MPSA70
R157 15K
Q106 MPSA20
R158 22K
D101 IN4148
C146 3.3µf 50V
R159 1M
C144 .01µf
R151, 33K
R152 330K
Q107 MPSA20
R153 10
R138 15K
R140 6.2K
R130 1K
C145 .001
IC100A MC1391
VOLT
CUR
V REF 5V
+5V
D151 IN4148
D150 IN4148
J12 TO J12
B100
BATTERY OPTION
+5V +5V +12V +5V
J32 J24 J23
R602 3.6K
R603 3.6K
TO P1 PIN 12
J31
Q600 MPSA70
R600 6.8K
R601 200K
IC600 NE555
R604 68K
Q601 MPSA20
R605 10K
R606 1K .5W
C602 3.3µf 50V
CR600
C600 .001µf
C601 .047
J10
BELL ENABLE J13
J9
R607 10K
-12V
BELL OPTION

NOTES:
1. ISOLATION TRANSFORMER MUST BE USED TO TAKE MEASUREMENTS IN THIS AREA.
2. GROUND SYMBOLS
   - EARTH GROUND
   - SIGNAL GROUND
   - POWER SUPPLY GROUND (VOLTAGE WITH RESPECT TO EARTH OR SIGNAL GROUND IS ONE HALF LINE VOLTAGE.)

POWER SUPPLY

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES
TOLERANCES .X=± .XX=± .XXX=± ANGLES=± CHAMFER=±
REMOVE ALL BURRS AND SHARP EDGES RADII AND FILLETS .010 TO .020
DO NOT SCALE THIS DRAWING
MATERIAL
FINISH

NAME	G.S.				
DATE	3-3-80				
BY	DRAWN	CHECKED	MECH ENGR	ELEC ENGR	APPROVED

ANN ARBOR TERMINALS INC
6107 JACKSON ROAD • ANN ARBOR, MICHIGAN 48103 • 313-769-0826

MONITOR BD

SIZE D | PART NUMBER 2011851 | SCALE — | WT — | SHEET 2 OF 2

PART NUMBER	201185F			
LET	R	REVISION	DRN	CHK	ENG
B	2	SEE SHT 1	GS		
D	3	ADDED R326	GS		
F		C314 WAS .15μf 100V	GS		
F		C313 WAS 15μf 100V. C308 WAS 15μf. R410 WAS .25W.	GS		
F	1	C406 WAS CONNECTED TO +12V	GS		
F	2	SEE SHT 2	GS		

+12V R200 330 .5W — D200 IN5236 7.5V 10% — C206 100μf 16V — J25 — +12V — R215 68 .5W — C205 470μf 16V — J20 +12V

IC 200 555 VERT OSC (pins 1–8) — R203 1.2K — C200 .001 100V — R202 150K — R204 1K — R205 100 — C202 .22 100V — RV200 10K HT — C204 4.7μf 50V — R206 1K — R207 47K

Q207 MPSA13 VERT AMP. — Q200 MPSA20 DIFF. AMP — Q201 MPSA20 DIFF. AMP — R208 1K — R209 10K — R210 3K — RV202 5K V. LIN — C208 4.7μf 50V — R212 1K — R214 68K — C209 3.3μf 50V — C211 100μf 50V

Q202 92PU57 VERT DRIVER — C210 270pf X5E — R213 10 — Q203 2N5496 VERT OUTPUT (H.S.) — D201 IN4448 — R216 1 .5W — R219 15 — R217 390 .5W — R218 390 .5W — Q204 2N6109 VERT OUTPUT (H.S.) — C212 — D202 IN4003 — D203 IN4003 — C213 100μf 50V — R220 1 .5W — R221 390 .5W — R222 3.3K — Q205 NSDU56 RETRACE GENERATOR — R223 390 — C214 1μf 50V — R225 680 .5W — R224 1 .5W — P3-J3 — L405B VERT YOKE 12mh 4.6Ω

-12V R226 68 .5W — C215 470μf 16V — -12V

+70V R300 22 .5W — D300 IN4004 — R301 10 .5W — C300 100μf 16V — C301 10μf 100V

R302 2.2K — C302 390pf X5E — R303 100 — R309 — Q301 MPSA70 VID AMP — C305 39pf X5E — R305 10K — J22 — R306 47K — C314 2200pf — C.B. IN — Q302 MPSA20 BLANKER — R347 — R310 2.2K — C306 .01 100V mylar — R311 3.3K — C304 MPSU03 VID OUTPUT — R312 1.2K 4W — L300 8.2μh — R316 — T.P.2

VID. IN — R333 330 — C313 2.2μf 50V — Q300 MPSA20 VID AMP — R320 150 — R328 22K — R317 330 — R319 150 — RV300 250 CONTRAST — R324 120 — C312 — R315 1K — R326 39 — C306 47μf 16V — R323 220 — J21 — R322 47 — R307 330 — R325 560 — Q305 2N3704 VID AMP — ECB TOP VIEW — R314 47 — R318 82 — C307 470pf X5E

Q303 MPSA70 BLACK LEVEL CLAMP — RV301 5K BLK. LEVEL ADJ. — R321 1.5K — R329 — C311 3.3μf 50V — C310 6800pf — D301 IN4148 — L302 220μh — T401 PIN 8 — R330 10K — R331 820K — C309

+12V — J17 — R404 150 — R405 1.2K — +8.5V REG. SOURCE — C403 220μf 16V — R402 2.4K — R401 2.4K — R407 100 1W — C404 22μf 16V — R406 47Ω — C406 .001 — Q400 NSDU56 — R408 100 .5W — C405 .005μf — T400 DRIVER XFMR — R415 .5 .5W — R416 100 .5W — Q401 2N6308 (H.S.) — 590V

T.P.1 — HORZ. SYNC — J11 — R400 1.5K — R432 2.2K — C400 220pf X5E — TO IC400.6 — R409 — IC400 MC1391 HORZ OSC. — R410 8.2K — C401 .1μf — C402 .033 — R413 100 — -70V — +12V — R412 4.7K — C407 6800pf — R411 100K — C408 1μf 50V — TO IC400.6 — R414 12K — C409 .0068μf polystyrene 5% — RV403 5K H. FREQ ADJ.

T401 BOTTOM VIEW — 05 10 — 20 — 07 30 — 08 40

CRT — BRN — BRN — TO T401 — YEL — R507 560 — K — G1 — G2 — G4 — IN CRT LEADS

+70V R502 150K .5W — RV500 250K BRIGHTNESS — R501 56K .5W — -70V — GRN — RED — +500V R503 150K .5W — BLUE — C501 .02μf 1KV — C502 .22 630V — R504 4.7M .5W

T.P.3

*NOTE: CLINTON PICTURE TUBE CE531 R428=2.7 1W CE689 R428=4.7 1W

+70V — T401 H.V. XFMR — 95V — C421 .047 400V — -70V SOURCE — D402 BY206 — *R428 4.7 1W — TO L302 — TO CRT FIL F1 F2 — R429 100K .5W — C422 .1μf 100V mylar — TO POWER SUPPLY C139. POWER SUPPLY SYNC SOURCE SEE SHT.2 — 10V — PIN B — D403 VARO HIB02

TOP VIEW FLYBACK CORE — A B — SYNC SOURCE WINDING INFORMATION

+500V — RV400 2M FOCUS — R427 470K .5W — -70V — C416 .005 1KV

+70V — R419 330K 1W — C419 .22μf 630V — J27 — +500V SOURCE — D401 MR816 — C418 — R418 1K .5W — P4-J4 — J26 — HORZ. YOKE — L405A 700μh 1.1Ω — P4-J4 — L406 WIDTH — C411 R420 220pf 1K — L407 LIN — R421 — C413 — C412 — R422 33K — R433 — C415 .82 200V "S" CAP

+500V — R426 150K .5W — R424 220K .5W — C417 .005 1KV — R425 680K .5W — +12V — R430 100K — RV401 10K DYN FOCUS ADJ — C414 .001 — R431 10K — Q402 BU-X86 (B C E) — R423 680

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TOLERANCES .X=± .XX=± .XXX=± ANGLES=± CHAMFER=±	NAME	G.S.				
	DATE	3-3-80	4-7-80			
	BY	DRAWN	CHECKED	MECH ENGR	ELEC ENGR	APPROVED
REMOVE ALL BURRS AND SHARP EDGES RADII AND FILLETS .010 TO .020	ANN ARBOR TERMINALS, INC. 6107 JACKSON ROAD • ANN ARBOR, MICHIGAN 48103 • 313-769-0826					
DO NOT SCALE THIS DRAWING	MONITOR BD					
MATERIAL						
FINISH	SIZE D	PART NUMBER 201185F				
	SCALE —	WT —	SHEET 3 OF 3			

PART NUMBER	201197B				
LET	R	REVISION	DATE	DRN	CHK	ENG
A	1	ADDED CR, C9.	10-13-80	GS		JR
A	2	X1 WAS 16.666. J23 WAS HI.	2-2-81	GS		JR
A	3	ADDED R23.	3-24-81	GS		JR
B		BOARD REVISION. C8, C9 WERE 820pf. J16, J25, J26 MOVED.	8-6-81	GS		JR

+5
R1 1.8K
X1 18.414 MHz
R2 39K
Q1
C1 120
12B 04
LS175 12C
CC0 CC0* CC1 CC1* CC2 CC2* CC3 CC3*
11B 10
11C 74 CC4 CC4*
13E 08
C2
LS51 11D
12D 86
10A 02
ZCLK
DCAS*
DRAS*
CC0
CC0*
CC1*
CC2
CC2*
CC4*
CP*
DLUB
HOV
LUB*
J23 J22 HI
1C LS161
7A 10
2C LS5161
3A 04
8B 74
9A 08
P1 9 HS*
HC0 HC1 HC2 HC3 HC4 HC5 HC6
CUB 81
ZADR0 ZADR1 ZADR2 ZADR5
DB0 DB1 DB2 DB3 DB7
WCN*
PC*
RKB*
1B LS259
1A 74
7B LS670/170
RE3*
13 BELL ENABLE
BLE
R3 10K
R4 10K
R5 10K
LPC*
C9 1000pf
C8 1000pf
3B LS161
2B LS161
5A 00
6B LS161
LC2
LC1
LOF*
RCLE
6A 27
DE
VC3 VC2 VC1
NMI*
2A 74
VS
11 VS*
NMI*
6 VUB*
8A 32
FC
5B LS157
MLC4
MLC5
MLC6
IEN

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TOLERANCES
.X = ±
.XX = ±
.XXX = ±
ANGLES = ±
CHAMFER = ±

REMOVE ALL BURRS AND SHARP EDGES
RADII AND FILLETS .010 TO .020

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MATERIAL

FINISH

	NAME	DRAWN	CHECKED	MECH ENGR	ELEC ENGR	APPROVED
	JFLOWERS				JR	
DATE	3-13-80				7-2-80	

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TERMINAL BD.

SIZE D | PART NUMBER 201197B | SCALE — | WT — | SHEET 1 OF 4

PART NUMBER		201197B			
LET	R	REVISION	DATE	DRN	CHK	ENG
A	3	ADDED R23	3-24-81	KS		JH
B		SEE SHT 1	9-6-81	KS		JF

P2: V, DD, CC, BB, AA, Z, Y, X, W — KR7✱, KR6✱, KR5✱, KR4✱, KR3✱, KR2✱, KR1✱, KR0✱

R18, R11 — R11-R18 6.8K — +5V

R19 10K, R20 10K — +5V

11H LS374 — DB7, DB6, DB5, DB4, DB3, DB2, DB1, DB0

KSL2✱, KS, J19

P3: ✱24 — KS

ZCLK

+5V

1F Z80A

ZADR15 5, ZADR14 4, ZADR13 3, ZADR12 2, ZADR11 1, ZADR10 40, ZADR9 39, ZADR8 38, ZADR7 37, ZADR6 36, ZADR5 35, ZADR4 34, ZADR3 33, ZADR2 32, ZADR1 31, ZADR0 30

DB7, DB6, DB5, DB4, DB3, DB2, DB1, DB0

WAIT✱

KSL2✱ T, KSL3✱ S, KSL4✱ N, KSL5✱ M, KSL6✱ L, KSL7✱ K — 12E LS145 — ZADR0, ZADR1, ZADR2, ZADR3

KSL8✱ U, KSL9✱ J, KSL10✱ H, KSL11✱ F, KSL12✱ E, KSL13✱ D, KSL14✱ C, KSL15✱ B, A, P, R — 12F LS145 — ZADR0, ZADR1, ZADR2, ZADR3

13D 00

17

P1: 22, 20 +5V, 36 +5V, 7 +5V; 16 +12V, 8 +12V; -5V 5 -5V; 19 -12V, 4 -12V; 23, 18, 35 GND, 10 GND

C24,25 22µf; C10-23 .047µf; D3; C28 22µf; C26,27 .047µf; C31 22µf; C29,30 .047µf

3, 12, 2 NO CONNECTION

MREQ✱ — 12B 04 — 9B 32 — 9D LS139

RFSH✱, ZADR12, J17 — 8F MK 4118 — WR✱, RD✱, CS8✱, ZADR11

6F PROM #3 — ZADR10, ZADR9, ZADR8, ZADR7, ZADR6, ZADR4, ZADR3, ZADR2, ZADR1, ZADR0, ZADR11

5F PROM #2 — ZADR10, ZADR9, ZADR8, ZADR7, ZADR5, ZADR4, ZADR3, ZADR2, ZADR1, ZADR0, ZADR11

3F PROM #1 — ZADR10, ZADR9, ZADR8, ZADR7, ZADR6, ZADR4, ZADR3, ZADR2, ZADR1, ZADR0, ZADR11

J16, 9E LS139 — ZADR13, ZADR11, ZADR12

ZADR6, ZADR7, ZADR6, ZADR5, ZADR7

NMI✱, CCØ, HOV, CUB81, RCLE, DLUB, LUB✱

11C 74, 13C 74, 13C 74 — HI

3B 32, 8A 32, 10A 02, 13D 00, 9A 08, 9B 32, 12B 04

R21 10K — +5V

R23 10K, R22 330 — +5V

11D LS51 — RCLD✱

P3: 4 DB0, 3 DB1, 2 DB2, 1 DB3, 39 DB4, 37 DB5, 38 DB6, 40 DB7

25 ZCLK, 34 PC✱

ZADS✱, ZADS, ZCAS, ZCAS✱

ZRAS✱

32 INT✱, 31 RW✱, 33 M1✱, 29 RD✱, 26 WR✱, 30 IORQ✱, 28 UE0✱, 27 UE1✱, WCN✱, RKB✱

21 CS4✱, 5 ZADR0, 6 ZADR1, 7 ZADR2, 8 ZADR3, 9 ZADR4, 10 ZADR5, 11 ZADR6, 12 ZADR7, 13 ZADR8, 14 ZADR9, 15 ZADR10, ZADR11, ZADR12, ZADR13

DRE✱, RE3✱

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TOLERANCES .X = ± .XX = ± .XXX = ± ANGLES = ± CHAMFER = ±

REMOVE ALL BURRS AND SHARP EDGES RADII AND FILLETS .010 TO .020

DO NOT SCALE THIS DRAWING

MATERIAL

FINISH

NAME	JFLOWERS			JR
DATE	3-13-80			7-2-80
BY	DRAWN	CHECKED	MECH ENGR	ELEC ENGR	APPROVED

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TERMINAL BD.

SIZE D — PART NUMBER 201197B

SCALE — WT — SHEET 3 OF 4

PART NUMBER 20-1197B					
LET	R	REVISION	DATE	DRN	CHK	ENG
A	1	SEE SHT 1	10-13-80	GS		JR
A	2	SEE SHT 1	5-2-81	GS		JR
A	3	SEE SHT 1	5-29-81	GS		JR
B		J25, J26 MOVED	8-6-81	GS		JR

ZAD5*
ZCAS
DB0
DB1
DB2
DB3
DB4
DB5
CP*
IEN
CC4*
MLC4
LC1
LC2
MLC5
CC1*
CC2
BLE
CUB81
DE
CC0*
CC2*
MLC6
LOF*

1F LS258 · 2E LS258 · 1D LS258 · 2D LS258 · 4D LS174 · 8A 32 · 5D LS367 · 11E LS157 · 3E 4116 · 4E 4116 · 5E 4116 · 6E 4116 · 7E 4116 · 8E 4116 · 4C LS174 · 6C FONT PROM · 8C LS166 · 13E 08 · 9A 08 · 12D 86 · 11B 10 · 10A 02 · 13D 00 · 6D LS174 · 7D LS174 · 8D LS174 · 9D LS139 · 12E 74 · 10H LS02 · C3 68 · C4 · C5 220 · C6 .047 · C7 22 · R6 22 · R7 1K · R8 68 · R9 · RV1 5K · R10 220 · Q2 · D1 IN4148 · P1 VIDEO OUT

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REMOVE ALL BURRS AND SHARP EDGES RADII AND FILLETS .010 TO .020

DO NOT SCALE THIS DRAWING

MATERIAL

FINISH

NAME	J FLOWERS			J R	
DATE	3-13-80			7-2-80	
BY	DRAWN	CHECKED	MECH ENGR	ELEC ENGR	APPROVI

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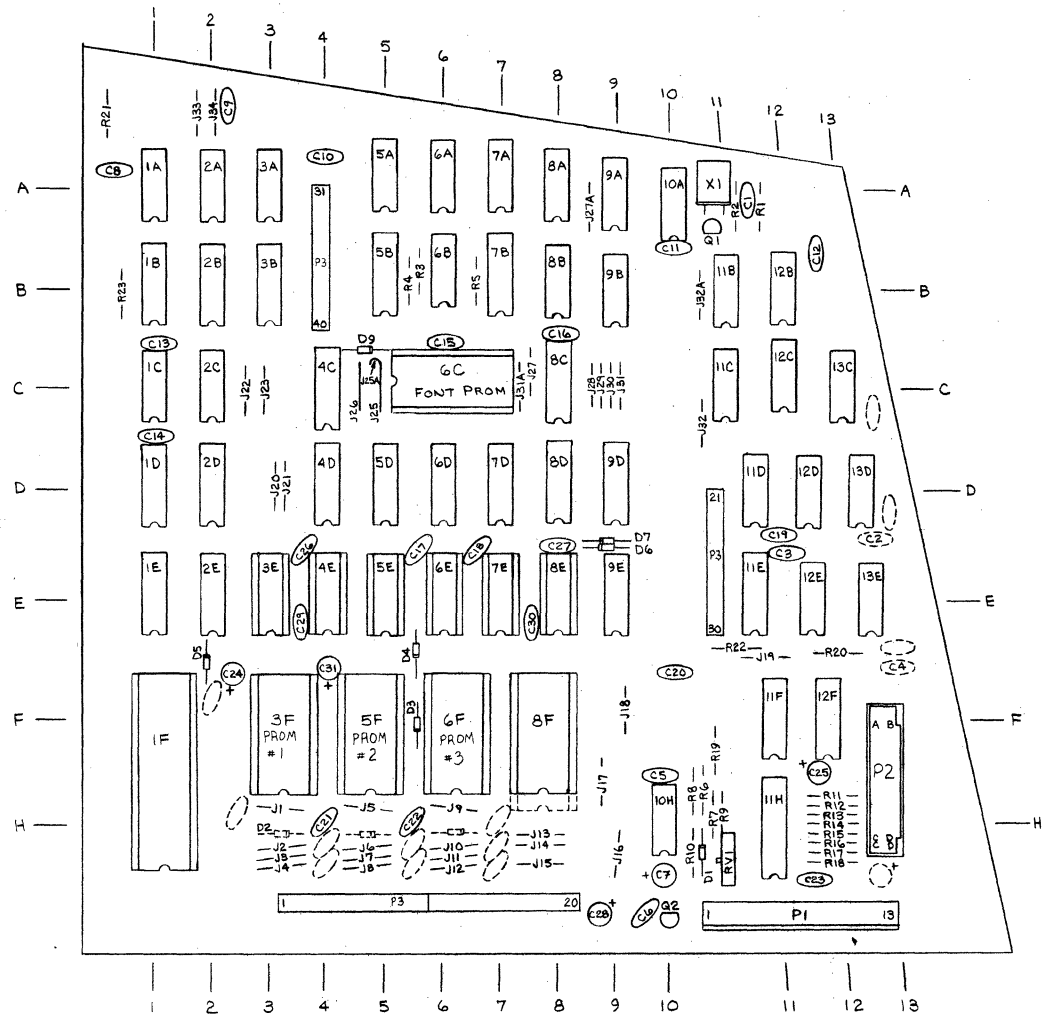
TERMINAL BD.

SIZE D

PART NUMBER 20-1197B

PART NUMBER		201197B				
LET	R	REVISION	DATE	DRN	CHK	ENG
A	1	ADDED C8, C9	10-13-80	G.S.		JR
A	2	X1 WAS 16.666 MHZ. J23 WAS HI.	2-2-81	G.S.		JR
A	3	ADDED R23	3-24-81	G.S.		JR
B		J16, J25, J26 MOVED	8-6-81	G.S.		JR



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.XXX = ±
ANGLES = ±
CHAMFER = ±

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RADII AND FILLETS .010 TO .020

DO NOT SCALE THIS DRAWING

MATERIAL

FINISH

NAME	G S			JR	
DATE	6-24-80			7-2-80	
BY	DRAWN	CHECKED	MECH ENGR	ELEC ENGR	APPROVED

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TERMINAL BD.

SIZE	PART NUMBER	
C	201197B	
SCALE 1:1	WT	SHEET 4 OF 4

LET	R	REVISION	DATE	DRN	CHK	ENG
A	1	SEE SHT 2.	10-1-80	GS		JR
A	2	RV101 WAS 250K	3-5-81	GS		JR
A	3	R103 WAS 1K	4-20-81	GS		JR
A	4	JUMPERS J1,J2 DELETED. JUMPERS J14,J15,IC16H ADDED.	5-14-81	GS		JR
B	-	BOARD REVICION. J16,J17 PROVIDED. R106 WAS 560K	9-30-81	GS		JR

PART NUMBER 201199B

P3

M1*	33
IORQ*	30
RD*	29
CS4*	21
RW*	31
PC*	34
WR*	26
DBØ	4
DB1	3
DB2	2
DB3	1
DB4	39
DB5	37
DB6	38
DB7	40
ZADRØ	5
ZADR1	6
ZADR2	7
ZADR3	8
ZADR4	9
ZADR5	10
ZADR6	11
ZADR7	12
ZADR8	13
ZADR9	14
ZADRIØ	15
INT*	32
UEØ*	28
UE1*	27
ZCLK	25
KS	24
SPARE	17
+12V	16
+5V	22, 20, 36
GND	23, 18, 35
-12V	19

P5: R, P, N, M, L, E, A, B, J, H, F, C, D, K

P4: D, K, C, B, F, H, J, A, E, L, M, N, P, R

MD: 75189A

15D: L804

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TOLERANCES .X = ± .XX = ± .XXX = ± ANGLES = ± CHAMFER = ±

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DO NOT SCALE THIS DRAWING

MATERIAL

FINISH

	NAME	DRAWN	CHECKED	MECH ENGR	ELEC ENGR	APPROVED
DATE	6-27-80				7-2-80	
BY	G.S				JR	

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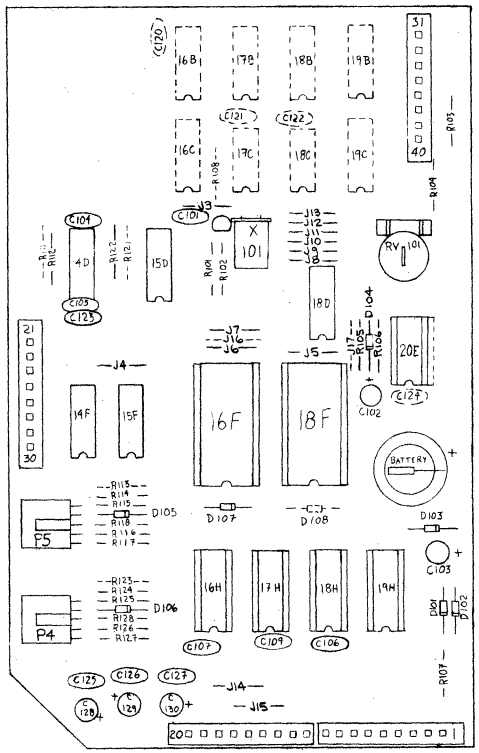
I/O BOARD

SIZE D | PART NUMBER 201199B | SCALE | WT | SHEET 1 OF 2

PART NUMBER 201199 B

LET	R	REVISION	DATE	DRN	CHK	ENG
A	1	ADDED R112, R122, DELETED R113, R123.	10-1-80	GS.		JR
A	2	SEE SHT 1	3-5-81	GS		JR
A	3	SEE SHT 1	4-20-81	GS.		JR
A	4	SEE SHT 1	5-14-81	GS		JR
B		SEE SHT 1	9-30-81	GS		JR



UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES

TOLERANCES
.X = ±
.XX = ±
.XXX = ±
ANGLES = ±
CHAMFER = ±

REMOVE ALL BURRS AND SHARP EDGES
RADII AND FILLETS .010 TO .020

DO NOT SCALE THIS DRAWING

MATERIAL

FINISH

NAME	M@M			JR	
DATE	6-30-80			7-2-80	
BY	DRAWN	CHECKED	MECH ENGR	ELEC ENGR	APPROVED

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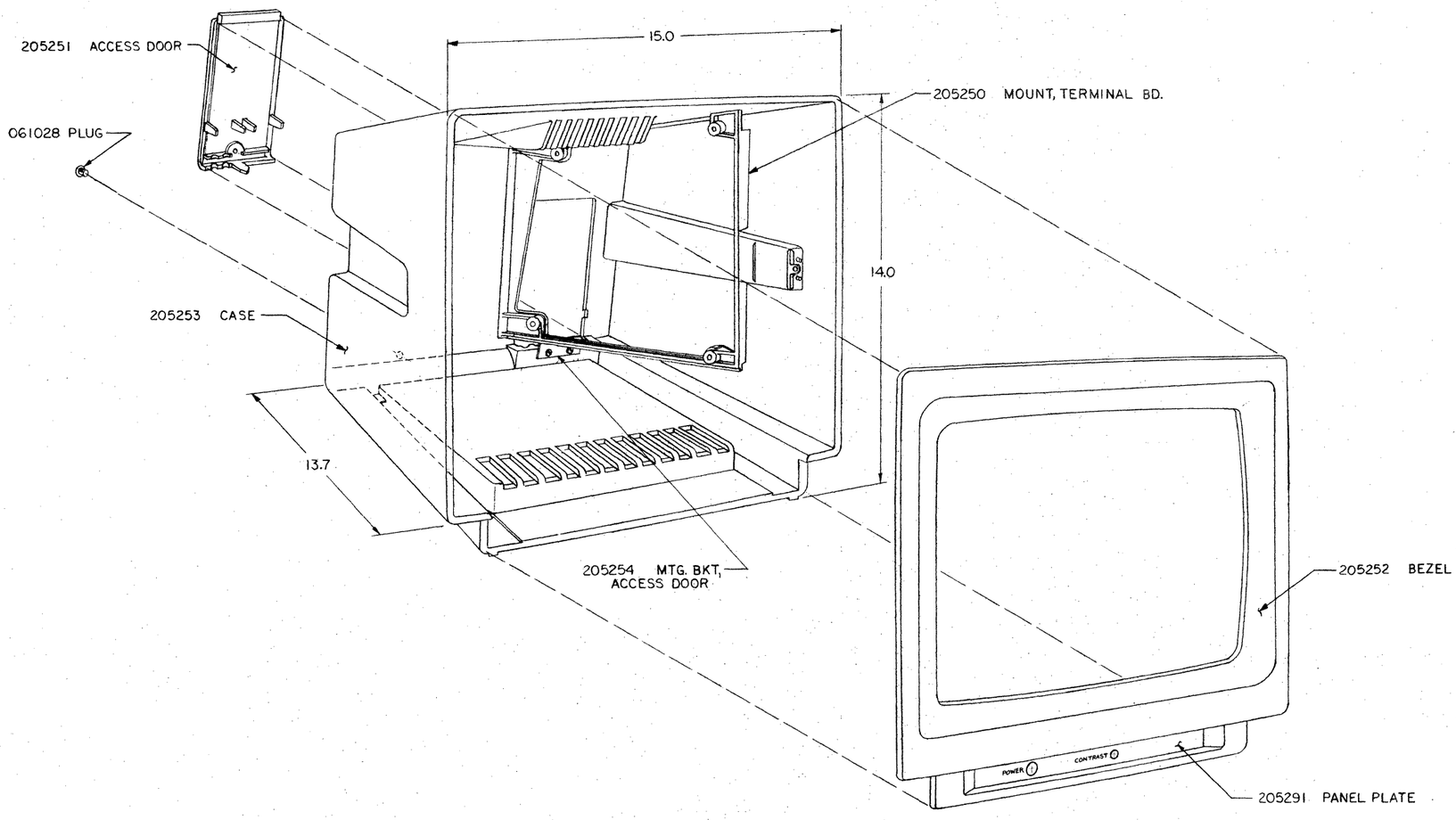
I/O BOARD

SIZE C | PART NUMBER 201199B

SCALE | WT | SHEET 2 OF 2

PART NUMBER	205305A				
LET	R	REVISION	DATE	DRN	CHK	ENG



UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES

TOLERANCES
.X = ±
.XX = ±
.XXX = ±
ANGLES = ±
CHAMFER = ±

REMOVE ALL BURRS AND SHARP EDGES
RADII AND FILLETS .010 TO .020

DO NOT SCALE THIS DRAWING

MATERIAL

FINISH

NAME	G.S				DS
DATE	2-23-79	6/14/79			6-4-22
BY	DRAWN	CHECKED	MECH ENGR	ELEC ENGR	APPROVED

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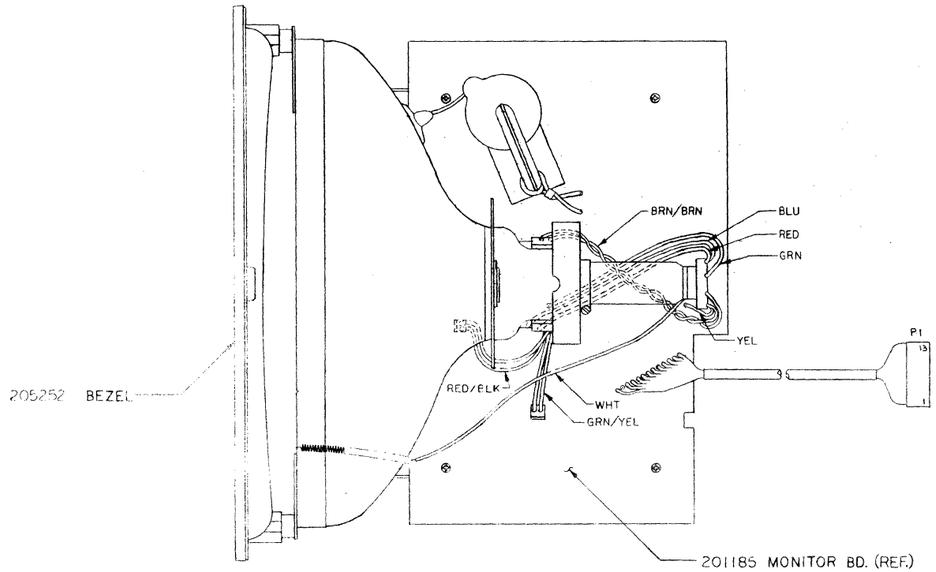
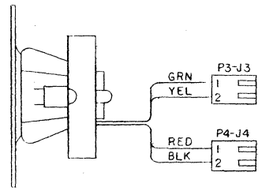
E-CASE (600)

SIZE	PART NUMBER
D	205305A

SCALE 1/2 | WT | SHEET 1 OF 2

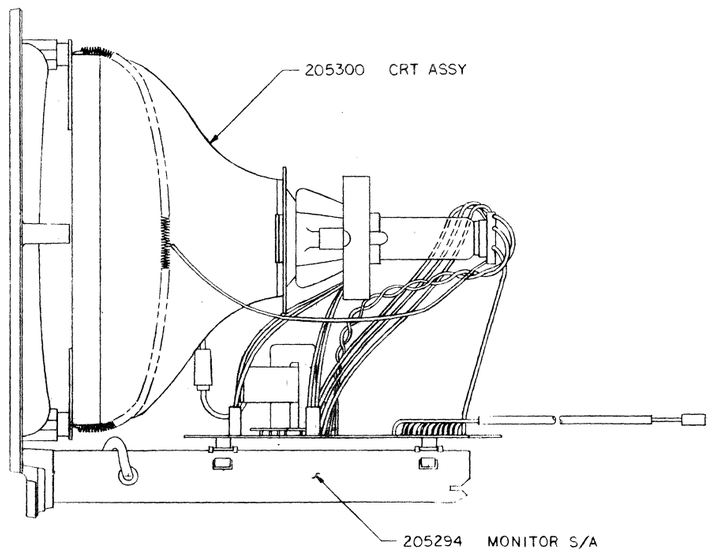
PART NUMBER	205305A				
LET	R	REVISION	DATE	DRN	CHK	ENG





080097 CONN 2F (2 REQ'D)
080009 PIN (4 REQ'D)

YOKE DETAIL



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TOLERANCES
.X = ±
.XX = ±
.XXX = ±
ANGLES = ±
CHAMFER = ±

REMOVE ALL BURRS AND SHARP EDGES
RADII AND FILLETS .010 TO .020

DO NOT SCALE THIS DRAWING

MATERIAL

FINISH

NAME	G.S.				DS
DATE	3-22-79				6-4-79
BY	DRAWN	CHECKED	MECH ENGR	ELEC ENGR	APPROVED

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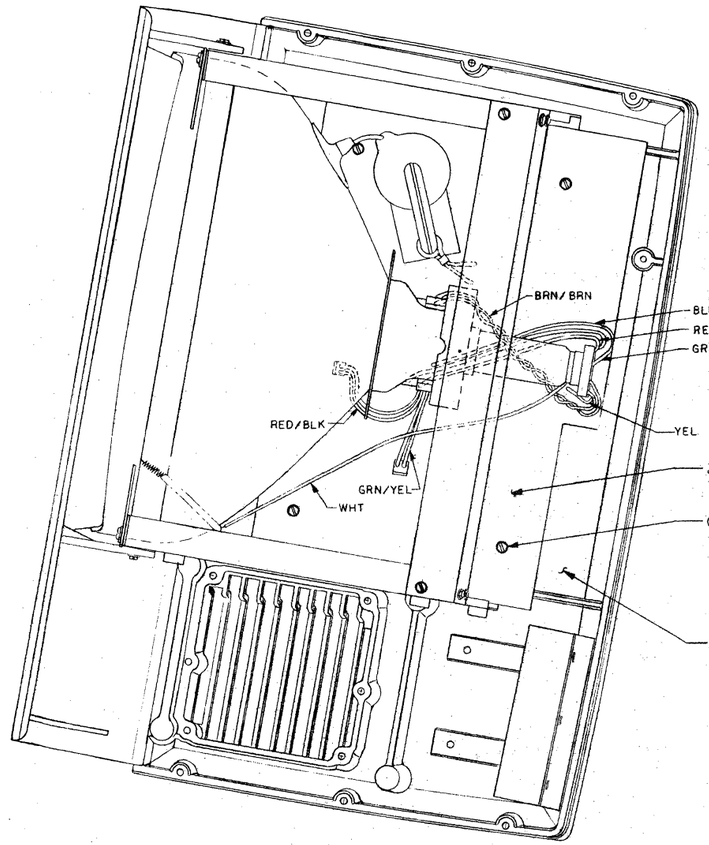
E-CASE 600

SIZE	PART NUMBER
D	205305A

SCALE | WT | SHEET 2 OF 2

PART NUMBER		210000B				
LET	R	REVISION	DATE	DRN	CHK	ENG
B	-	DELETED CONNECTOR PANEL ADDED CONTROL PANEL	1-22-81	GS		



201185 MONITOR BD.

060544A SCREW #8X16 SHWH (4)

210004B S/A BASE 700

060822A SCREW 10-32 X 8 RH (4)
060833A WASHER #10 FLAT (4)

210001D S/A TUBE 4N034

210135A S/A FRAME 700

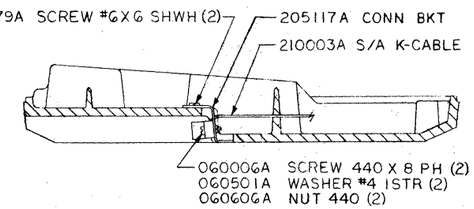
210006E S/A BEZEL 700

210246A S/A CONTROL PANEL
060536A SCREW #8X8 SHWH (2)

205318A SHIM (2)

060544A SCREW #8X16 SHWH (2)

060540A SCREW #8X12 SHWH (2)



ASSEMBLY INSTRUCTIONS

1. INSTALL K-CABLE S/A
2. MOUNT FRAME S/A TO BASE
3. PLACE MONITOR BD. IN FRAME
4. MOUNT C-PANEL S/A TO BASE
5. SECURE MONITOR BD. TO FRAME
6. INSTALL TUBE S/A IN FRAME
7. MAKE FINAL WIRE CONNECTIONS

UNLESS OTHERWISE SPECIFIED:
DIMENSIONS ARE IN INCHES
AND INCLUDE CHEMICALLY
APPLIED OR PLATED FINISHES

TOLERANCES
.X = ±
.XX = ±
.XXX = ±
ANGLES = ±
CHAMFER = ±

REMOVE ALL BURRS AND SHARP EDGES
RADII AND FILLETS .010 TO .020

DO NOT SCALE THIS DRAWING

MATERIAL

FINISH

	DRAWN	CHECKED	MECH ENGR	ELEC ENGR	APPROVED
NAME	G.S.		J.R.R.		
DATE	6-16-80		7-2-80		

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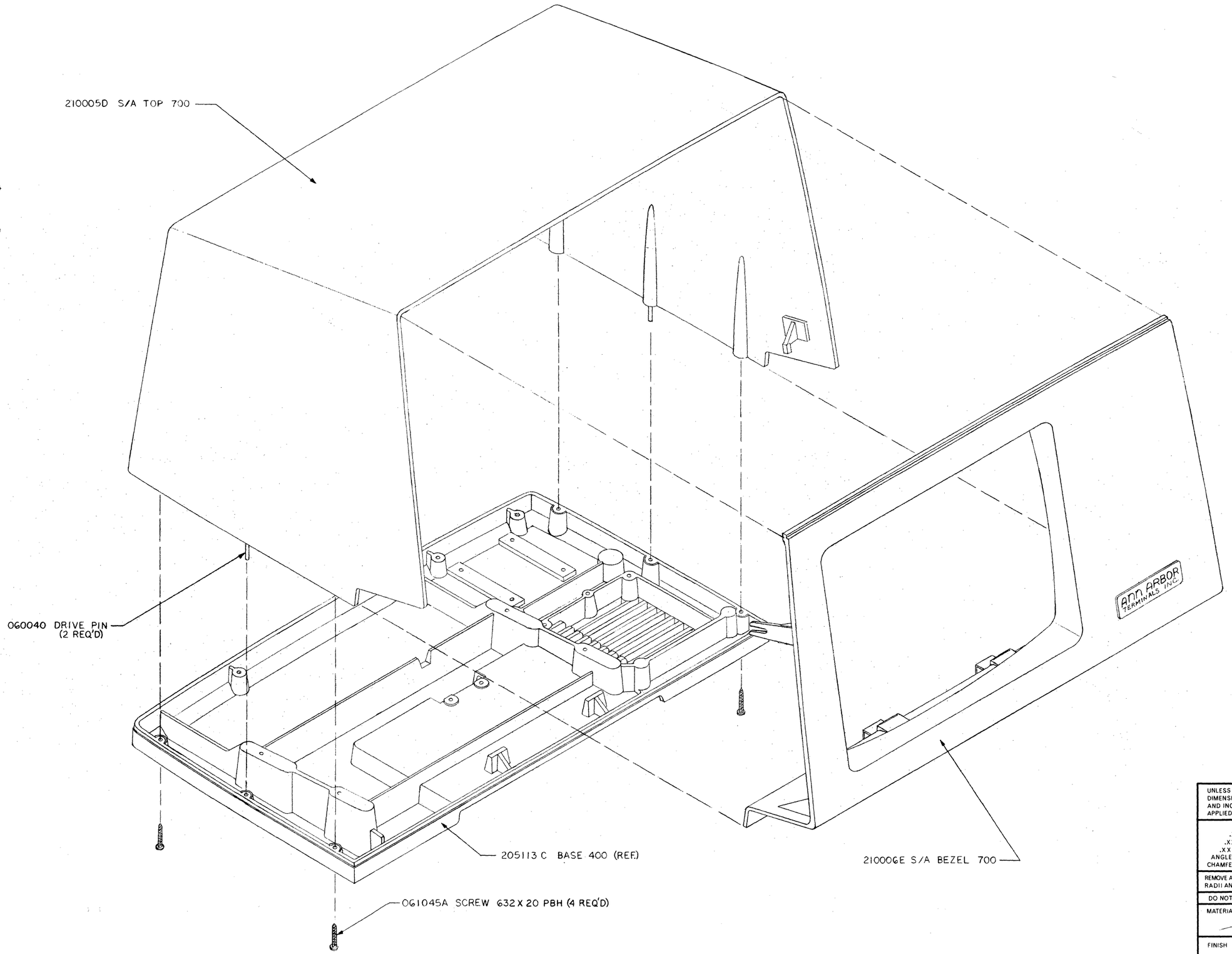
S/A D CASE 700

SIZE D

PART NUMBER 210000B

PART NUMBER		210000B				
LET	R	REVISION	DATE	DRN	CHK	ENG
B	–	ADDED PROVISION FOR CONTROL PANEL ACCESS DOOR	1-22-80	GS		



UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES

TOLERANCES
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REMOVE ALL BURRS AND SHARP EDGES
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DO NOT SCALE THIS DRAWING

MATERIAL

FINISH

	DRAWN	CHECKED	MECH ENGR	ELEC ENGR	APPROVE
NAME	G.S.		J.M.		
DATE	6-20-80		7-2-80		

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S/A D-CASE 700

SIZE D | PART NUMBER 210000B

SCALE 1:2 | WT ——— | SHEET 2 OF 2

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