AMPEX

PYXIS
DISK STORAGE DRIVE
OPERATION AND MAINTENANCE
TECHNICAL MANUAL

3315507–01

Rev. A 12/82

AMPEX MEMORY PRODUCTS DIVISION

AMPEX

Ampex Corporation · One of The Signal Companies

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INTRODUCTION

This manual provides maintenance personnel with information necessary to install, operate, and maintain the Pyxis disk storage drive.

The maintenance manual is arranged in five sections. The scope of each section is described in the following paragraphs.

Section I, General Information, contains the Pyxis functions, physical and electrical descriptions, and equipment specifications.

Section II, Installation, contains information to enable maintenance personnel to uncrate, inspect, and install the Pyxis. Preliminary checks are also contained in this section.

Section III, Operation, explains and shows the location and use of status and fault isolation indicators, step rate and drive configuration selections, as well as powering-up or powering-down procedures for the disk drive.

Section IV, Theory of Operation, explains the drive operations and gives a detailed description of each function. Simplified logic and block diagrams, timing diagrams, and waveforms are included.

Section V, Maintenance, contains corrective maintenance procedures.

Appendix A contains reference drawings.

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SECTION I

GENERAL INFORMATION

1.1 GENERAL DESCRIPTION

The Pyxis Model 7/13/20/27 disk drives are fixed-media, random-access, rotating memory storage devices that enable the central processing unit (CPU) of a data processing system to store and retrieve blocks (records) of data on rotating disks. The drive functions as the input/output device for the CPU and can operate as a single stand-alone, or it may be operated with similar disk drives in daisy-chain configuration.

There are four disk drives (Models 7, 13, 20, and 27) in the Pyxis series containing 1, 2, 3 or 4 magnetic disks which range in total data storage from 6.7 megabytes to 26.67 megabytes, unformatted, and 5.24 megabytes to 20.97 megabytes, formatted. Access to data is provided by one moving head per disk surface. The heads are an integral part of the head disk assembly (HDA) and never require alignment in the field. Data is recorded on the disk surfaces using modified frequency modulation (MFM) techniques.

The drive incorporates an open-loop, stepper-motor-type positioning system. The major components of the drive are illustrated in Figure 1-1 and are explained in the following paragraphs.

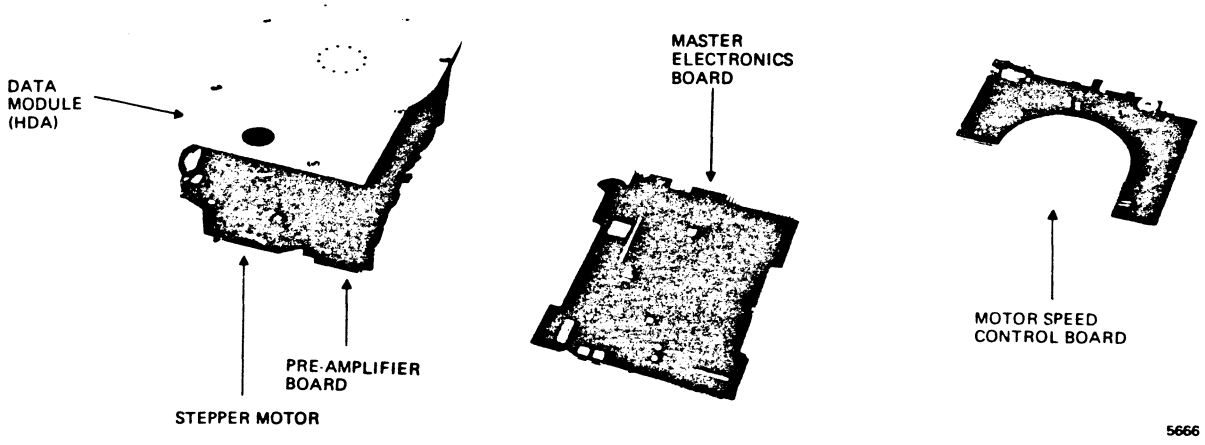


Figure 1-1. Major Component Location

1.1.1 Head Disk Assembly

The head disk assembly, shown in Figure 1-2, is a completely sealed module that houses the read/write heads, disks, positioner assembly, stepper motor, and filters. The spindle-mounted disks are rotated by the dc motor as the read/write heads fly over the surface of the disk. The stepper motor positions the heads over the disk, using positioning information from a microprocessor. Within the sealed module, the airflow generated by disk rotation causes air to flow from the disk chamber (upper chamber) through an aperture into the drive chamber (lower chamber) and to return via a recirculating filter.

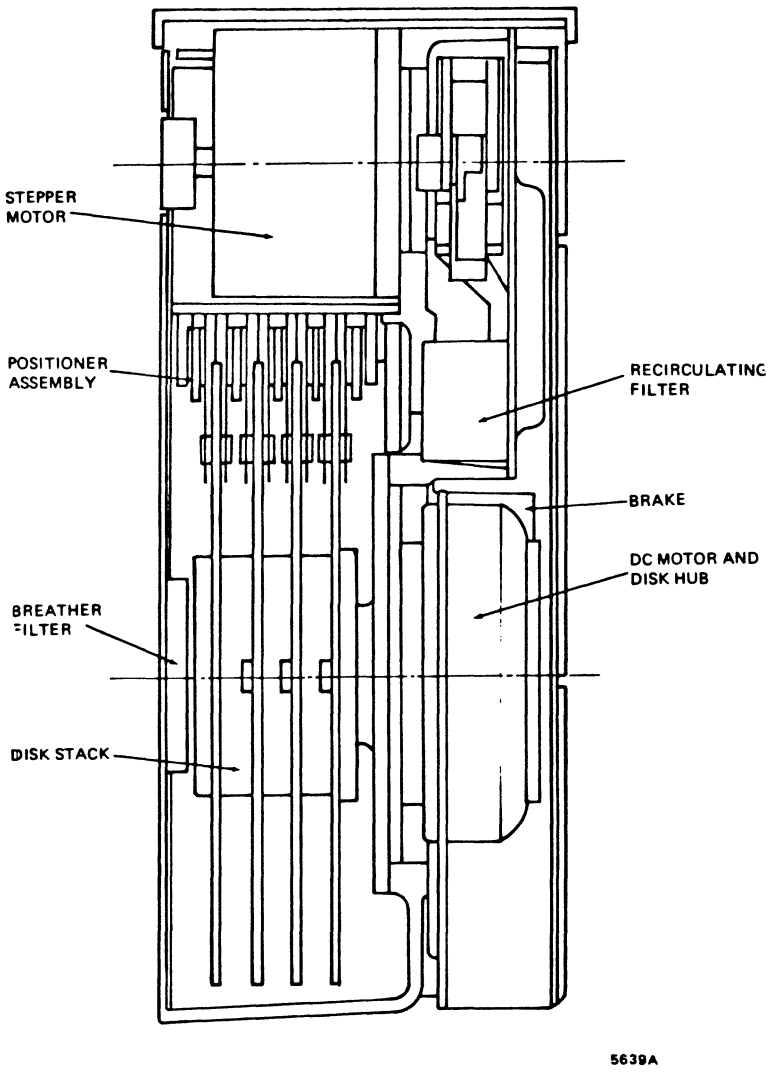


Figure 1-2. Head Disk Assembly

1.1.2 DC Motor and Brake

The dc motor is a brushless, two-phase external rotor motor with integral hub and commutation effected by a Hall sensor. The rotational speed of the motor is 3600 revolutions per minute (rpm). The disk hub is grounded to the master electronics board via the motor shaft and a button contact. The brake is a plunger-solenoid designed to stop the motor in five seconds and to provide a restraining torque during handling.

1.1.3 Disk Electronics

The electronics assembly consists of three standard printed circuit board assemblies (PCBAs); master electronics, preamplifier and motor speed control.

1.1.4 Power Supply

The dc supply voltages (+12 and +5 volts) to the disk drive are supplied by the user and input to the drive on connector J3.

1.2 FUNCTIONAL CONCEPT

The simplified block diagram in Figure 1-3 shows the functional concept of the Pyxis disk drive. Additional detailed explanations of the logic areas occur in Section IV.

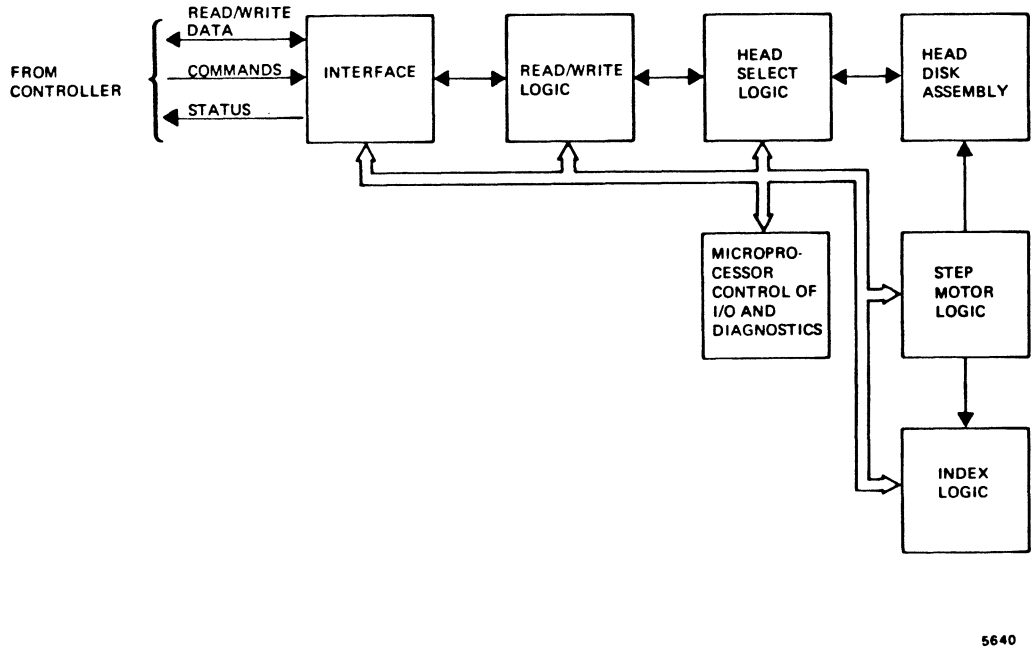


Figure 1-3. Pyxis Simplified Block Diagram

1.2.1 Interface Logic

The interface logic translates the input/output signals of the disk drive to ensure drive-to-controller signal compatibility. Disk drive logic signal levels are transistor-to-transistor logic (TTL) compatible. The transmission line signals are differential signals.

1.2.2 Read/Write Logic

To execute read or write commands, the drive must be free of faults and the selected head must be at the correct location on the disk (i.e., on cylinder). During a read command, the read/write logic recovers data from the disk, processes the data, and transfers the data to the controller. During a write command, the read/write logic receives data from the controller, processes the data and writes it on the disk.

1.2.3 Head Select Logic

The head select logic receives and decodes the addresses of a specific head.

1.2.4 Step Motor Logic

A four-phase stepper motor is used to control the read/write heads in the proper sequence at a rate and direction determined by a microprocessor.

1.2.5 Index Logic

The square wave output of the Hall sensor in the dc motor is processed to produce a pulse every disk revolution. This pulse is used as an interface signal to mark a fixed reference point relative to the disk.

1.3 EQUIPMENT SPECIFICATIONS

Performance characteristics for Pyxis drives are listed in Table 1-1. Environmental specifications are listed in Tables 1-2 and 1-3. The approved Ampex shipping container protects the drive (with stepper transit lock) against damage when the container in transit or storage is subjected to shock and vibration as listed in Table 1-3.

Table 1-1. Performance Characteristics

Characteristics	Specifications			
Storage capacity (unformatted)	Model 7	Model 13	Model 20	Model 27
Disks per drive	1	2	3	4
Cylinders	320	320	320	320
Tracks per cylinder	2	4	6	8
Data bytes per track	10,417	10,417	10,417	10,417
Tracks per drive	640	1280	1920	2560
Capacity (megabytes)	6.67	13.33	20.0	26.67
Spare capacity	One extra (spare) cylinder is available*			
Storage capacity (formatted)				
Data bytes per sector	256	256	256	256
Data sectors per track	32	32	32	32
Data bytes per track	8192	8192	8192	8192
Capacity (megabytes)	5.24	10.49	15.73	20.97
Media defects (maximum number)	2	4	6	8
Recording parameters				
Bit density	9000 bpi (inner track, nominal)			
Coding	Modified-frequency-modulation (MFM)			
Track density	360 tracks per inch (average)			
Rotational parameters				
Disk rotational speed	3600 (± 1%) rpm			
Data transfer rate	5 Mbits per second			
Cylinder access time				
Ramp mode				
Single cylinder	18 milliseconds (average)			
320 cylinders	215 milliseconds (maximum)			
Cylinder access (average)	90 milliseconds			
3 milliseconds step mode				
Single cylinder	18 milliseconds (average)			
320 cylinders	1035 milliseconds (maximum)			
Cylinder access (average)	360 milliseconds			

* Extra (spare) cylinder would be 320 where the first cylinder is 0.

Table 1-1. Performance Characteristics (Contd.)

Characteristics	Specifications
Cylinder Access Time (Contd.)	
Slow pulse mode**	
Single cylinder	23 milliseconds (average)
320 cylinders	step rate=pulse rate
Cylinder access (average)	step rate=pulse rate
Data access time	
Average latency	8.3 milliseconds
Average data access time/ramp mode	98.3 milliseconds
Average data access time/3 milliseconds step mode	368.3 milliseconds
Head switching time	5 microseconds (maximum)
Error rates (These error rates are valid only when the drive is used according to specification. Media defects or equipment failures are excluded. Written data should be verified as being correctly written. All media defects should be flagged.)	
Seek errors	1 in 10^6 seeks
Recoverable read errors	1 in 10^{10} bits
Nonrecoverable read errors	1 in 10^{12} bits

** This option requires the removal of jumper A from pin 14 of the microprocessor on the master electronics board.

Table 1-2. Environmental Requirements

Storage	Transit	Operating
Temperature: -40°F to 158°F -40°C to 70°C	 -40°F to 158°F -40°C to 70°C	 50°F to 122°F 10°C to 50°C
Temperature gradient: 27°F per hour 15°C per hour	 27°F per hour 15°C per hour	 18°F per hour 10°C per hour
Humidity: 5-90% RH no condensation	 5-90% RH no condensation	 10-85% RH no condensation
Humidity gradient: 20% per hour	 20% per hour	 20% per hour
Altitude: -1000 to +40,000 ft	 0 to +40,000 ft	 -1000 to +10,000 ft
RF Interference: --	 --	 1 volt/meter rms (1.5 Hz - 10GHz)
Magnetic field: --	 --	 0.0003 tesla, max.
Emitted acoustic noise: --		 54 db, max. (continuous), scale A at 1 meter

* AMPEX single-box shipping container, stepper motor locked.

Table 1-3. Vibration and Shock Requirements

Characteristics	Specifications
Vibration, non operating	
Storage or transit	0.2 inch peak to peak displacement at 5 to 20 Hz and 3.5g peak acceleration at 20 to 500 Hz in any of three mutually perpendicular axis.
System or freestanding	0.040 inch peak to peak displacement at 5 to 30 Hz and 2.0g peak acceleration at 30 to 500 Hz in any of three mutually perpendicular axis; resonance points of unit excluded.
Vibration, operating*	0.006 inch peak to peak displacement in any of three mutually perpendicular axis over frequency range of 5 to 60 Hz and 1.0g peak acceleration at 60 to 500 Hz except for vibrations along axis perpendicular to front facia where acceleration is 0.5g at 60 to 100 Hz and 1.0g at 100 to 500 Hz; excitation applied to mounting brackets (resonance points excluded).
Shock, non operating**	
Storage or transit	Single box - Withstand drop on any side or corner from 36 inches (stepper motor locked). Ten pack - Withstand drop on bottom surface from 9 inches (stepper motors locked).
System or freestanding	Shocks applied to mounting brackets 3g peak in any of three mutually perpendicular axis, less than 10 milliseconds duration, and 2 shocks/sec maximum.
Shock, operating**	Shocks applied to mounting brackets 3g peak in any of three mutually perpendicular axis, less than 10 milliseconds duration, and 2 shocks/sec maximum.

* Vibrations are sinusoidal
** Shocks are half-cycle sinusoidal waveforms.

SECTION II

INSTALLATION

2.1 GENERAL

This section contains unpacking, installation, and checkout information for the Pyxis Model 7/13/20/27 Disk Storage Drive.

2.2 UNPACKING

Prior to unpacking the drive, inspect the packaged drive to determine whether any damage has been incurred during shipment.

1. Using the shipping documents, verify that all items have been received.
2. Open protective shipping carton at top.
3. Remove drive from shipping carton.
4. Remove plastic cover.
5. Inspect each package article to determine whether any damage has been incurred during shipment.
6. Verify that connectors, indicators, and protruding parts are undamaged.
7. Check ID nameplate against shipping papers to verify that drive part number and serial number are correct.
8. When practical, store shipping containers for reuse.
9. Record any damage, and report damage to the applicable carrier.

2.3 EQUIPMENT PLACEMENT

Equipment placement consists of mounting the drive, planning the layout, routing the input/output cables and grounding the equipment.

2.3.1 Shipping Lock

The stepper motor shipping lock (label) is fixed to the top cover of the drive and covers a plastic pulley on the stepper motor shaft. The lock prevents movement of the read/write heads across the disk surfaces during shipment. This label is not affixed to the plastic pulley on units that are fitted with the automatic stepper motor lock.

CAUTION

The label must be removed before power is applied to the disk drive. Once the label is removed, the stepper motor shaft should never be rotated by hand; head disk damage could result.

2.3.2 Step Rate Selection

The disk drive has a step rate operational range of 10 microseconds to 8 milliseconds. This operational range has three bands; two ranges are automatically selected by the microprocessor, and one is selected by removing Link A on the master electronics board.

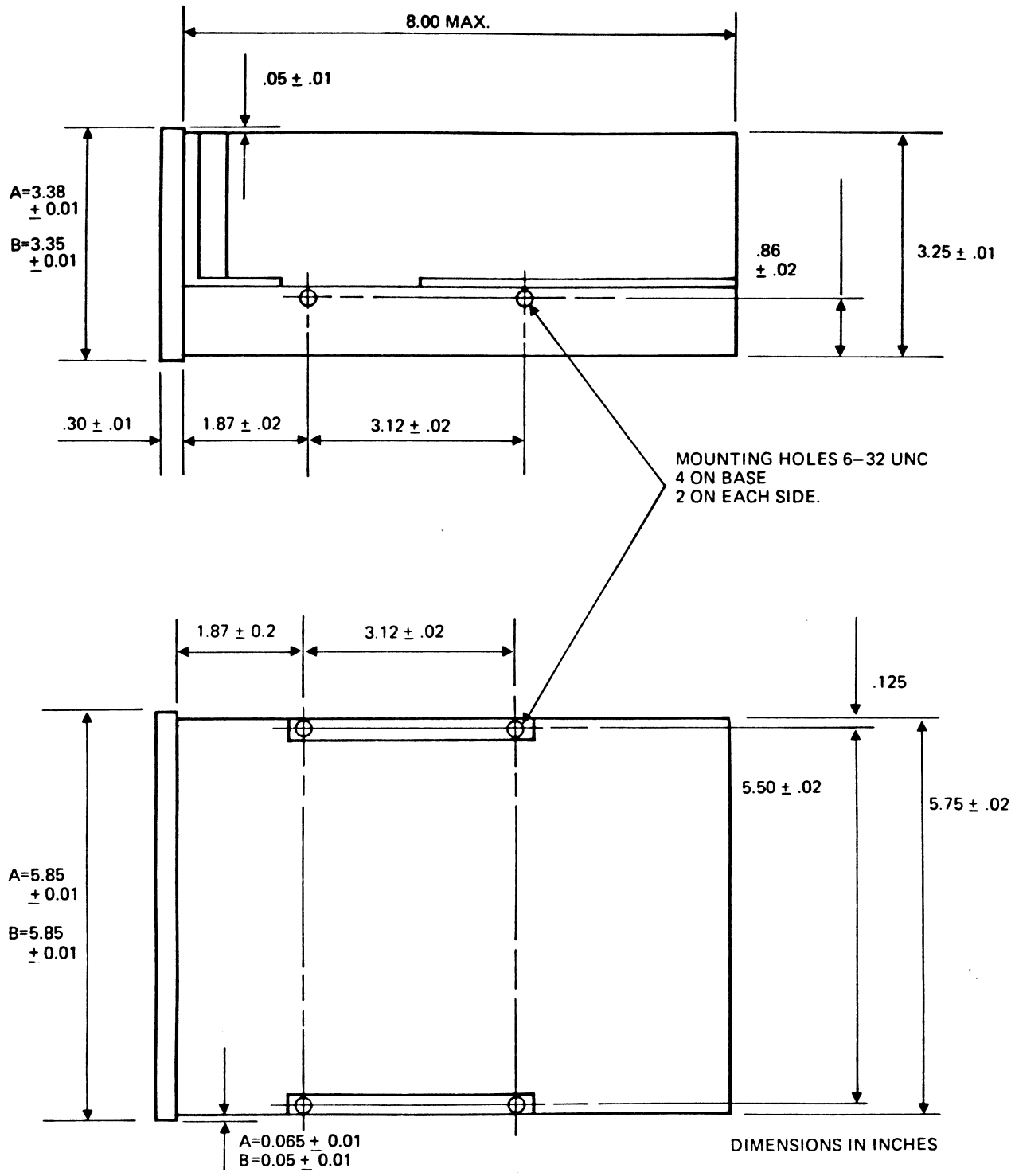
Link A in: step rate 10 microseconds to 200 microseconds
Link A in: step rate 700 microseconds to 3.1 milliseconds
Link A out: step rate 3.1 milliseconds to 8.0 milliseconds

2.3.3 Equipment Mounting

Side brackets with tapped holes are provided with each drive and permit base or side mounting as shown in Figure 2-1. These brackets are fixed to the drive chassis via shock-absorbing grommets. The drive can be oriented in any axis. When installing into an enclosure, at least 0.1 inch clearance must be maintained around the entire drive to allow vibration isolation, prevent obstruction of the breather filter, and prevent creation of ground loops.

2.3.4 Multiple-Drive Configuration

The Pyxis disk drive can be connected in a daisy-chain configuration with up to four drives in the chain (Figure 2-2). Each drive has a four-pole drive switch, accessible through a port in the side bracket, which is used to identify the drive in the chain (Figure 2-3). To identify a drive, the pole corresponding to the number of the drive in the chain is closed. Only one pole in each drive switch can be in the closed position.



NOTE:
A = VENTED FACIA
B = PLAIN FACIA

Figure 2-1. Mounting Details

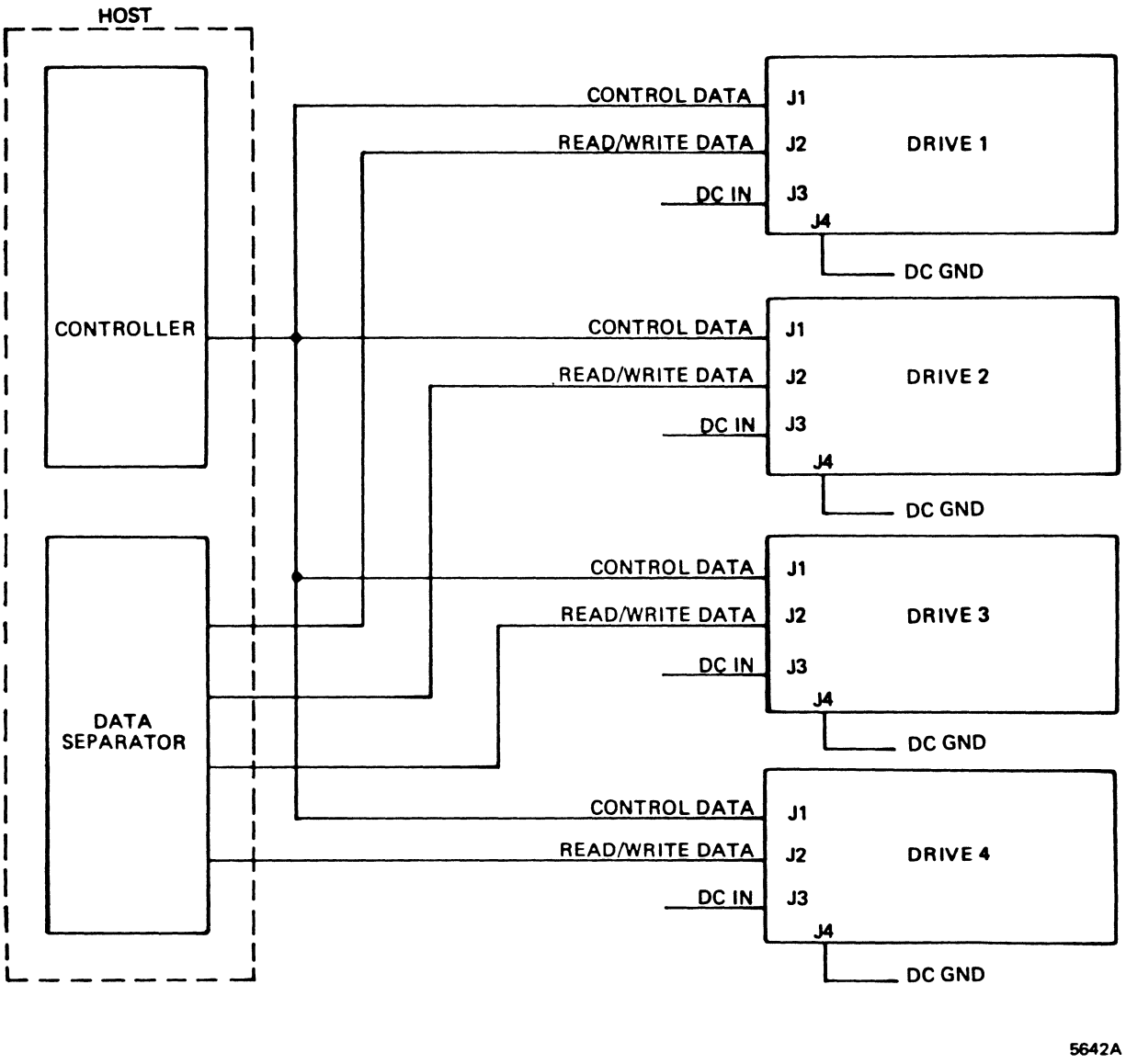


Figure 2-2. Daisy-Chain Configuration

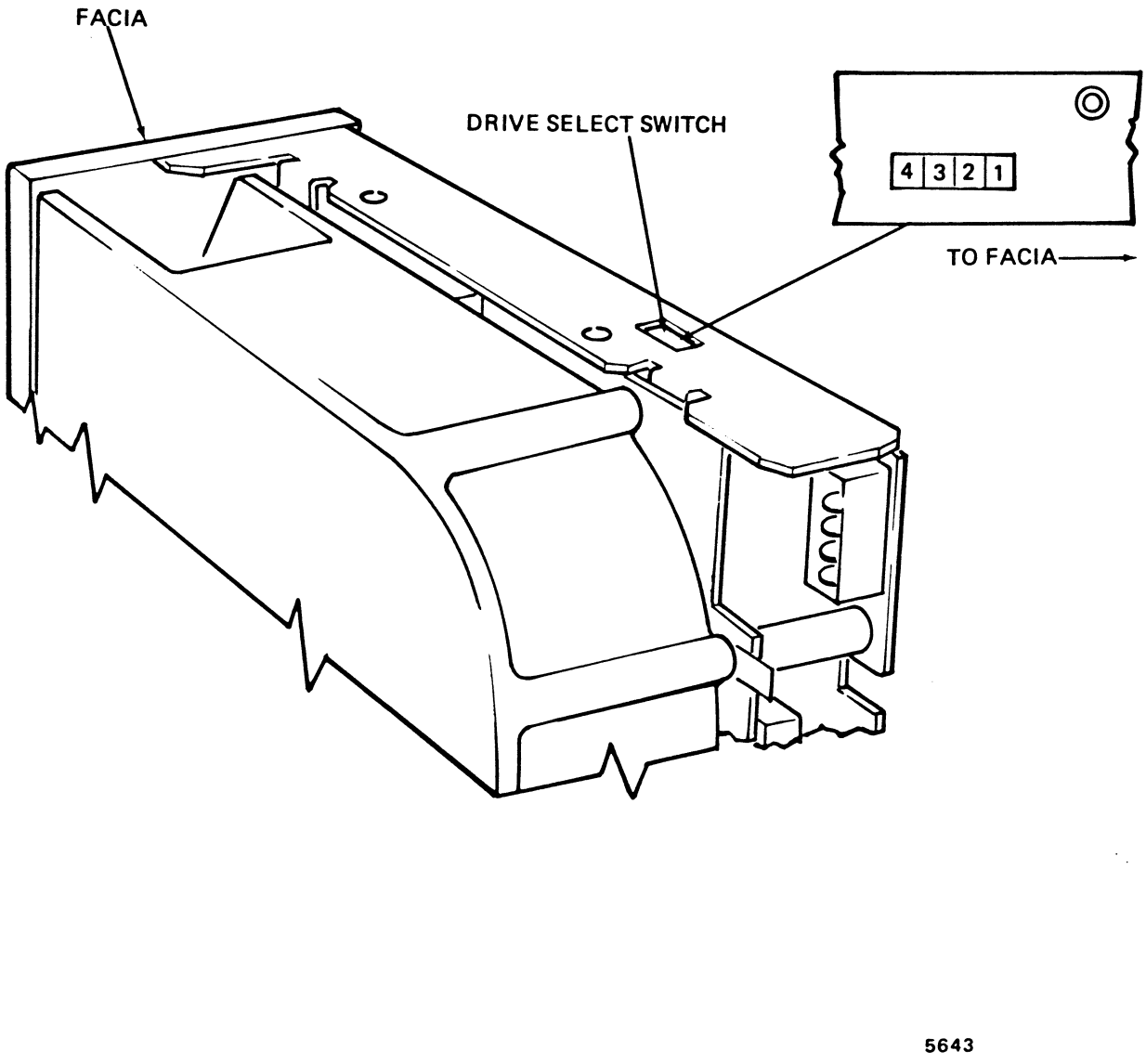


Figure 2-3. Drive Select Switch Location

In the daisy-chain configuration, the line terminator pack is removed for all drives except for the last one in the chain. All drives are supplied for single usage (i.e., pole 1 is closed and the terminator pack is installed).

2.3.5 Grounding

Host and disk drive logic ground are connected together by twisted-pair connector J3 (Figure 2-4). The frame ground is installed from the HDA (dc ground) by rubber grommets. Both logic and HDA grounds are connected internally via a master board standoff.

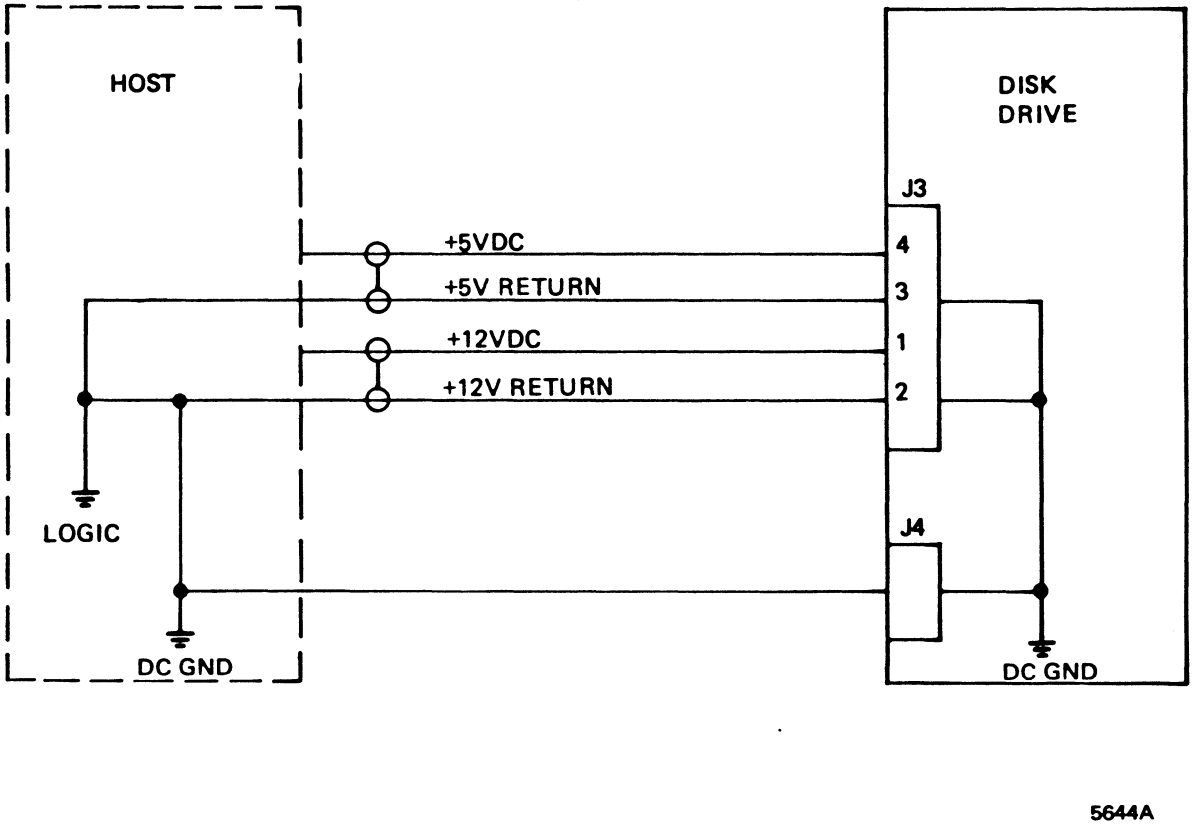


Figure 2-4. Disk Drive Grounding

2.4 PREINSTALLATION CHECKS

There are no preinstallation checks on the Pyxis disk drive.

2.5 SYSTEM INSTALLATION

Installation of the drive consists of connecting the power, control and read/write cables from the host system to the drive.

2.5.1 Connector and Cable Requirements

The cable connectors required are standard-insulation, displacement-type connectors designed for use with flat-ribbon or twisted-pair cable. Part numbers (and vendors) are listed in Table 2-1 as a reference to the type of connectors required. Equivalent connectors from other vendors may be used.

Table 2-1. Cable Connector Data

Cable Connector	Description
Control cable Cable connector J1	34-position, AMP P/N 88373-3
Read/write cable Cable connector J2	20-position, AMP P/N 88373-6
Power connector J3	Mate-N-Lok 4-pin AMP P/N 350211-1
Ground connector J4	Faston AMP P/N 61664-1

2.5.2 Control Cable

The control cable (J1) carries the control and status information which is exchanged between the drive and the control unit in the host system. Pin assignments and signal names are listed in Table 2-2.

Table 2-2. Control Signal Pin Assignments

Ground Return	Pin	Signal Name
1	2	Reduced Write Current
3	4	Head Select 2
5	6	Write Gate
7	8	Seek Complete
9	10	Track 000
11	12	Write Fault
13	14	Head Select 0
15	16	Reserved (To J2 Pin 7)
17	18	Head Select 1
19	20	Index
21	22	Ready
23	24	Step
25	26	Drive Select 1
27	28	Drive Select 2
29	30	Drive Select 3
31	32	Drive Select 4
33	34	Direction In

2.5.3 Read/Write Cable

All differential MFM coded data transmitted between the disk drive and the host system is carried by the read/write cable (J2). Pin assignments and signal names are listed in Table 2-3.

Table 2-3. Read/Write Signal Pin Assignments

Ground Return	Pin	Signal Name
2	1	Drive Selected
4	3	Reserved
6	5	Spare
8	7	Reserved (To J1 Pin 16)
10	9	Spare
12	11	GND
	13	+MFM Write Data
	14	-MFM Write Data
16	15	GND
	17	+MFM Read Data
	18	-MFM Read Data
20	19	GND

2.5.4 Power Cable

The disk drive requires only dc power which is supplied by the host system on power cable J3. Table 2-4 lists the pin assignments and voltages for the power cable.

Table 2-4. Power Cable Pin Assignments

Pin	Signal
1	+12 Vdc
2	+12 Vdc Return
3	+5 Vdc Return
4	+5 Vdc

2.5.5 Ground Connector

Ground connector J4 connects disk drive dc ground to the host system dc ground.

2.5.6 Terminator

If the drive is the last drive in a daisy-chain installation or is the only drive connected to the host system controller, a removable resistor terminator pack (provided with each drive) must be installed for the control interface (J1) lines.

.6 ILLEGAL ADDRESS MAP

An illegal address map supplied with each drive informs the user of areas of media defects. A media defect is a physical characteristic of the media which results in a repetitive read error when a properly adjusted unit is operated within specific operating conditions. Valid data must not be written over known media defects; therefore, sector/track deallocation or other techniques must be utilized to avoid these areas.

A label fixed to each drive indicates the addresses of sectors which should be ignored by the host. These sector addresses are identified by cylinder. head, and sector. No illegal addresses exist in cylinders 0, 1, and 2. The format used for this purpose is 33 sectors/track, each sector consisting of 256 bytes.

SECTION III

OPERATION

3.1 GENERAL DESCRIPTION

This section contains operating instructions for the Pyxis disk drive. Operating instructions consist of indicator functions, power-on/off procedures and voltage checks.

3.2 INDICATORS

When they are lit, the two red LEDs fixed to the master electronics board are visible through the facia. The Power On LED is located closest to the center of the facia and is on when the drive is Ready and no error is present. It is also used to indicate fault conditions in the drive (Table 3-1). Fault conditions are described in detail in Section V.

The Power On LED will not come on, indicating an error, if +5 volt supply does not come up and stabilize within one second. (The microprocessor does not receive an initial reset.)

The Select LED comes on (provided the Power On LED is on) when the drive is ready and selected by the host.

3.3 POWER-ON PROCEDURES

The Pyxis requires +12 volts and +5 volts dc source power, and these voltages are measured at drive connector J3. At power-on, the drive motor takes 4 amperes at +12 volts. A graph of the starting current for the drive is shown in Figure 3-1. For power-up or power-down sequences, the +12 volt and +5 volt supplies may be applied or removed in any order. However, if the +5 volt power is applied first, the +12 volt should follow within 5 seconds or the fault detection circuitry will issue an error indication.

On power-up, the drive performs an automatic re-calibration sequence which includes a disk speed check, accurate to ±1 percent of nominal, a seek to track 000 and an index pulse selection. The host may use status Ready to sense the completion of this sequence. The time until Ready turns true varies for each model of the Pyxis series. Maximum times are as follows:

Model	Time to Ready
7	13 seconds
13	15 seconds
20	18 seconds
27	22 seconds

Table 3-1. Diagnostic and Failure Code Indicators

Action	Abnormal Result	Result
Power-up drive		LED flashes at 0.5 second intervals After 25 seconds maximum, LED stops flashing and remains on. Heads are at track 0.
Code 1	LED displays*. . . -	No index track data burst at track-2 or track-3
Code 2	LED displays . . - .	No flag 0 from track 0 detector
Code 3	LED displays . . - -	Motor speed exceeds ±1% tolerance during power-up
Code 4	LED displays . - . .	Motor speed exceeds +10%, -5% tolerance during normal operation
Code 5	LED displays . - . -	Flag 0 always true
Code 6	LED displays . - - .	Step pulse while Write Gate true
Code 7	LED displays . - - -	Static write fault condition**
Code 8	N/A	
Code 9	LED displays - . . -	Microprocessor self-test failed
Code 10	LED displays - . - .	No Index
Code 11	LED displays - . - - LED remains OFF LED remains ON LED flashes (erratic)	Motor not up to speed Firmware/microprocessor fault Firmware/microprocessor fault Firmware/microprocessor fault
Code 12	LED displays - - . .	Found index track data burst, but cannot set index

* For the fault codes, a four-bit binary code is used. Long flash (-) = logic 1, a short flash (.) = logic 0, with the most significant bit (MSB) occurring first.

** Write Fault Conditions:
1. Write current and no Write Gate
2. No write current and Write Gate
3. More than one read/write head selected
4. 12-volt supply drops below 10.3 volts
5. 5-volt supply drops below 4.5 volts

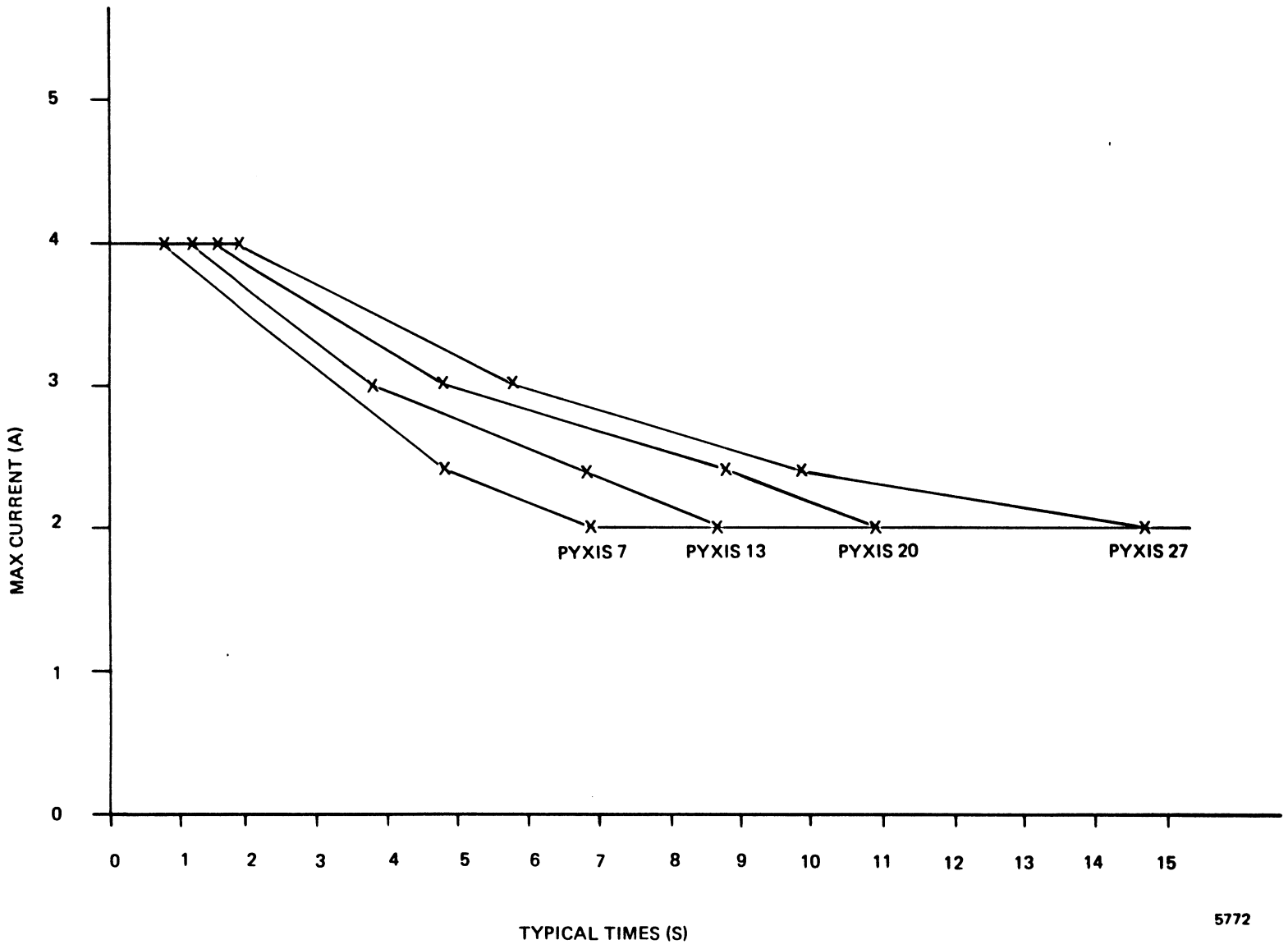


Figure 3-1. Starting Current

3.3.1 Power Supply Checks

The following loads are used to check the power supplies. For the 12-volt supply, the power-up current is measured using a standard load of 3 ohms in parallel with 1 millihenry and the operating current is measured using 5 ohms in parallel with 1 millihenry. With a 7-ohm resistive load on the 5-volt supply and the aforementioned loads on the 12-volt supply, noise and ripple should be no more than 100 millivolts peak-to-peak up to 500 hertz and 50 millivolts peak-to-peak from 500 hertz to 5 megahertz.

The power requirements of the Pyxis drive are listed in Table 3-2.

Table 3-2. Power Requirements

Voltage (Vdc)	Tolerance	Current Nominal	Current Maximum
+5	±5%	0.65A	0.75A
+12	±10%	2.0A	2.4A

SECTION IV

THEORY OF OPERATION

4.1 GENERAL

This section describes the theory of operation for the Pyxis 7/13/20/27 disk drive. This information provides maintenance personnel with a comprehensive understanding of the functions and operations of the drive. A brief discussion of disk recording principles is followed by a functional description of the disk drive unit explaining how the drive interfaces with the host controller and describes interface signals. The physical locations of the logics and their interconnections are shown in the detailed diagram of Figure 4-1.

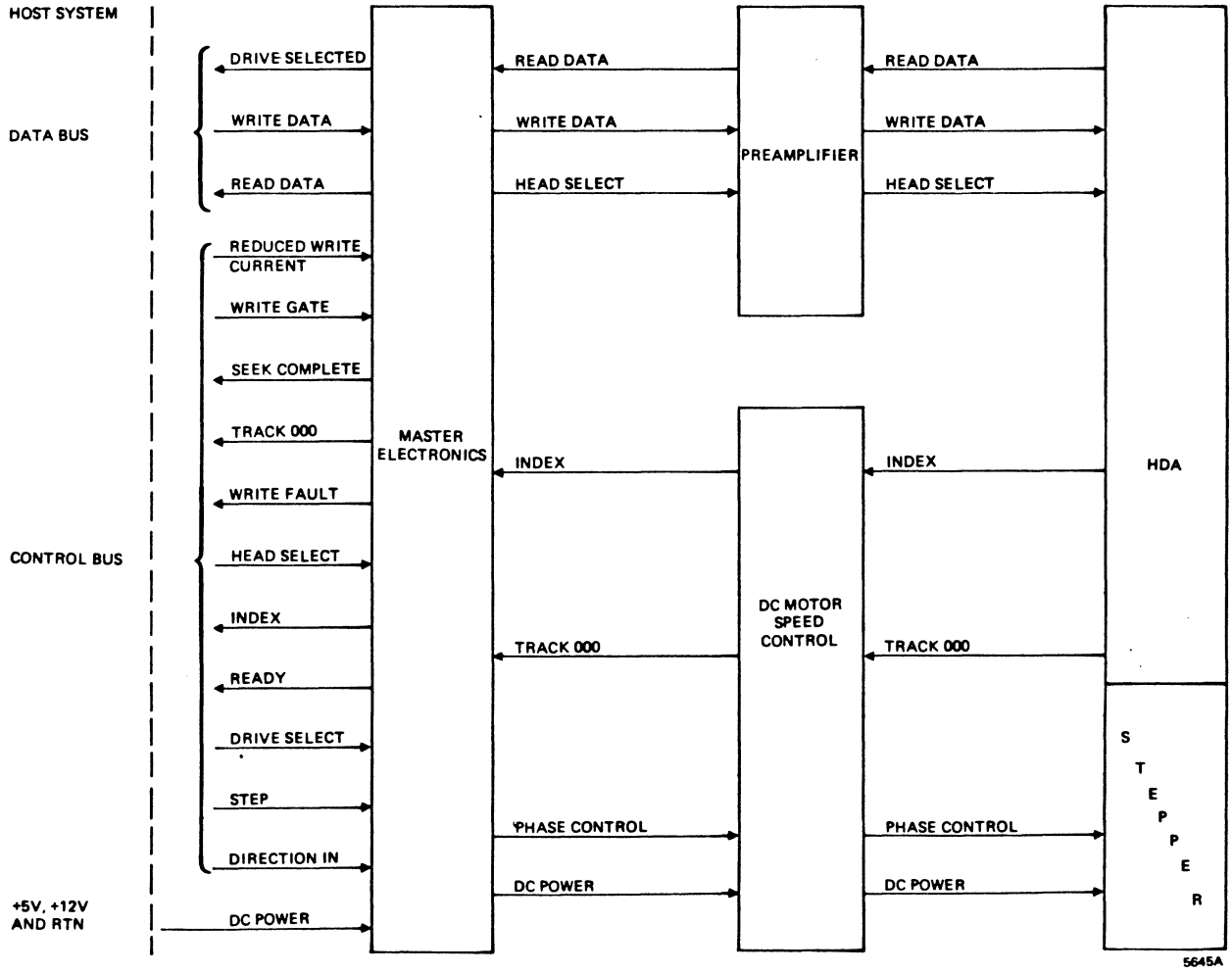


Figure 4-1. Pyxis Block Diagram

4.2 BASIC DISK PRINCIPLES

The recording medium for the drive is a stack of one to four 5 1/4-inch disks with two to eight recording surfaces (see Figure 4-2).

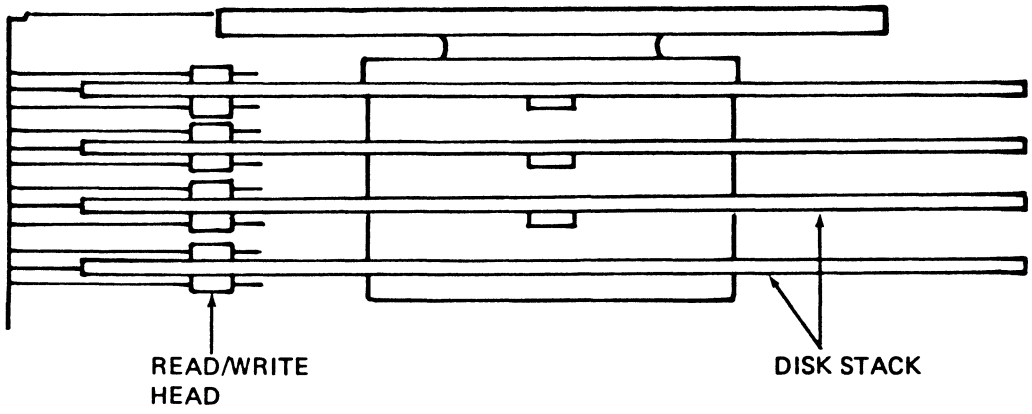


Figure 4-2. Surface and Head Geometry

Each disk is coated with a layer of magnetic oxide. The coating is burnished to a flatness that allows the read/write heads to fly in proximity to the surface without actual physical contact.

Data is recorded in serial fashion on concentric rings on each disk surface by holding the head in a fixed position over the rotating disk. These rings are referred to as tracks. The disk drive unit positions the heads precisely over the tracks. Corresponding track positions, both upper and lower on each disk, are referred to as one cylinder of data.

A center-tapped coil is mounted on the core of the read/write head to perform the read/write function. The recording flux direction is controlled by energizing the center-tap connection, causing current to flow through the bifiler winding from the center tap to either one end or the other. When reading, the ends of the coil are switched to the input of the read amplifier. Data is erased by writing new data on the track. The read/write coil is mounted onto the core of the ferrite slider. As the disk rotates, it pulls a film of air around its surface. This moving air moves under the slider and exerts an upward force on the shoe. A downward pressure is placed on the slider by the spring flexure of the head. The head shoe then flies at a point where the downward force of the load spring is equal in force to the air pressure under the head.

The flying height of the slider is influenced in part by the air-bleed channel in the middle of the slider. This channel allows some air to bleed from under the slider, decreasing the air pressure and allowing the head to fly closer to the disk surface. The average flying height of the head is 19 microinches. (The head is closer on an inner track because the inner track portion of the disk is moving at a slower speed than the outer track portion of the disk, resulting in less air pressure on the inner track than on the outer track.)

The slider is mounted to the head arm assembly via a spring gimbal-mount. This allows the flying attitude of the slider to vary slightly so that it can follow minor surface variations without contacting the disk surface.

All heads are mounted on a carriage so that the heads and carriage move as one unit. The carriage moves the heads radially over the disk's surfaces. All the heads are positioned to the same cylinder at any given time.

4.3 CONTROL LINES

The control data is exchanged between drive and control unit via the control cable (paragraph 2.5.2). The following paragraphs define the control interface signals.

4.3.1 Reduced Write Current

The Reduced Write Current signal from the host system enables a current sink during a write, diverting current from the head and effectively reducing the write current.

4.3.2 Write Gate

When True, the Write Gate signal from the host enables the current source and Write drive signals. When False, this signal enables Read Data to be transferred from the drive to the host.

4.3.3 Seek Complete

The Seek Complete status signal is generated by the microprocessor in the master electronics board when the value of an internal 8-bit counter equals the desired stepper motor phase changes (determined by the Step and Direction In input signals).

4.3.4 Track 000

The Track 000 status line is set true when the read/write heads are positioned over track 00.

4.3.5 Write Fault

The Write Fault signal is true under the following fault conditions:

1. Write current in a head when Write Gate is false.
2. No write current in any head when both Write Gate and Drive Selected are true.
3. More than one head is selected.
4. The 12-volt supply is below 10.3 volts.
5. The 5-volt supply is below 4.5 volts.
6. Motor speed exceeds ±1% tolerance at the end of the power-up sequence.
7. Motor speed exceeds ±10% tolerance.
8. No Index signal.
9. Motor not up to speed.
10. Step signal received while Write Gate is true.

4.3.6 Head Select

Up to eight read/write heads may be selected using a 3-bit code on the Head Select 0, Head Select 1 and Head Select 2 lines. Table 4-1 is a head select matrix showing the logic level required on each Head Select line to select the desired read/write head.

Table 4-1. Head Select Decode Matrix

Line	HD0	HD1	HD2	HD3	HD4	HD5	HD6	HD7
Head Select 0	False	True	False	True	False	True	False	True
Head Select 1	False	False	True	True	False	False	True	True
Head Select 2	False	False	False	False	True	True	True	True

4.3.7 Index

The Index signal is a 200 microsecond output pulse used to mark a fixed reference point relative to the disk.

4.3.8 Ready

The Ready signal is true when the drive is ready to read or write (with or without an implied seek) and the other output lines are valid. Ready remains true until power-off or until there is a Write Fault. The Ready signal is false under the following conditions:

1. The drive is undergoing power-up.

2. Motor speed is out of tolerance (+10%, -5% of nominal).

3. Write Fault is true.

4.3.9 Drive Select

The Drive Select signal from the host system corresponds with the drive select switch setting of the drive. If the Drive Select signal does correspond, and the Ready signal is true, a Drive Selected true signal is returned to the host system via the data lines.

4.3.10 Step

The Step signal pulse from the host system is used in conjunction with the Direction In signal to move the stepper motor. This pulse input to the microprocessor is used to clock an internal 8-bit counter which is reset prior to each seek. Once the first step pulse is received, the processor issues stepper motor phase changes until the number of changes equals the value in the counter.

4.3.11 Direction In

The Direction In signal from the host controller determines the direction of motion of the stepper motor. The microprocessor receives the first step pulse of any seek, samples the input and internally stores the result.

4.4. DATA LINES

The disk drive transmits and receives differential data coded in modified-frequency-modulation (MFM) via the data cable (paragraph 2.5.3). Decoding is done by the host system. Precompensation (early and late) of write data is used for certain data patterns. The following paragraphs describe the read/write data, as well as the Drive Selected signal.

4.4.1 MFM Read Data

Data signals from the disk drive, recovered by reading a prerecorded track, are transmitted to the host system using an EIA RS-422 standard differential line driver, as shown in Figure 4-3. This balanced voltage signal will drive up to 20 feet of twisted-pair or flat-ribbon cable with an impedance (Z) of 105 ohms. The recommended receiver is shown in Figure 4-4. The transition of +MFM read data going more positive than -MFM read data represents a magnetic flux transition on the disk under the selected head. Timings are shown in Figue 4-5.

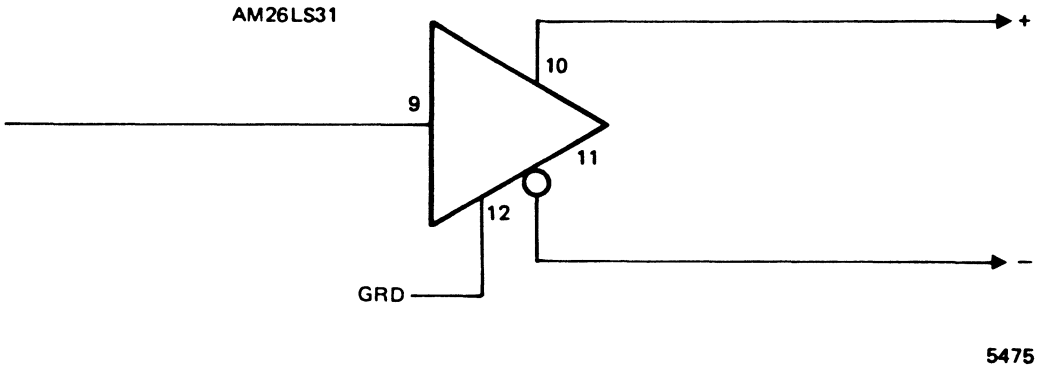


Figure 4-3. Differential Read Data Line Driver

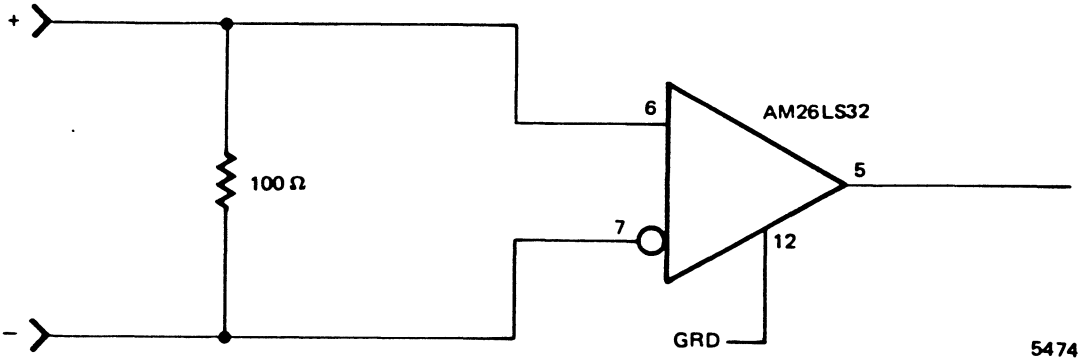
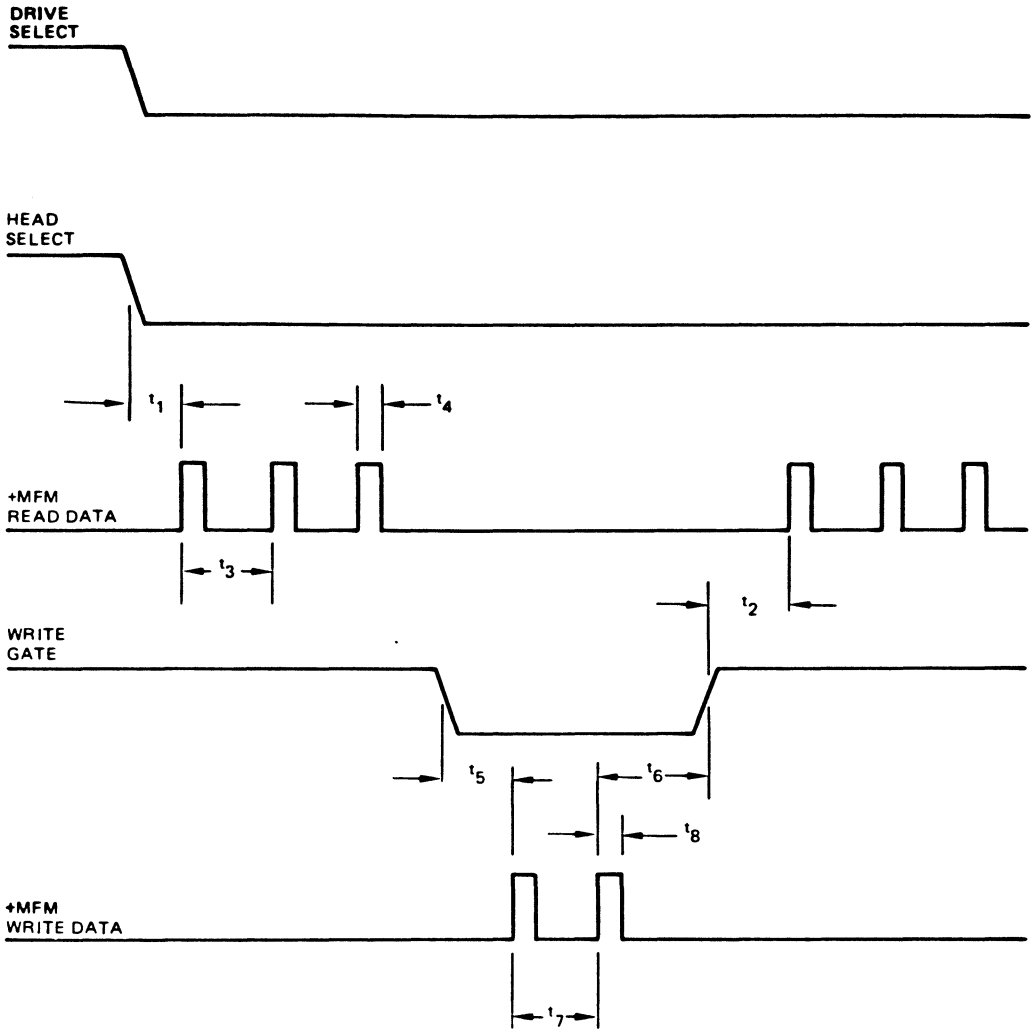


Figure 4-4. Differential Write Data Line Receiver



LABEL	DESCRIPTION	MIN	TYP	MAX
t_1	SELECT TO READ DATA (μS)	—	—	5
t_2	WRITE TO READ RECOVERY (μS)	—	—	5
t_3	READ BIT CELL (ns)	—	200	—
t_4	READ DATA PULSE WIDTH (ns)	25	—	85
t_5	WRITE GATE TRUE TO WRITE DATA (ns)	—	—	400
t_6	WRITE DATA TO WRITE GATE FALSE (ns)	—	—	400
t_7	WRITE BIT CELL (ns)	—	200	—
t_8	WRITE DATA PULSE WIDTH (ns)	25	—	—

5478B

Figure 4-5. Read/Write Timing

4.4.2 MFM Write Data

The MFM write data is transmitted by the host system to the disk drive using a standard differential line driver. (The line driver and the line receiver are the same type as used in transmission of the read data. Refer to Figures 4-3 and 4-4.) The transition of the +MFM Write data going more positive than -MFM Write data results in a flux reversal on the disk under the selected head, provided Write Gate is true and the drive is selected (Drive Select is true). MFM write data is inactive when Write Gate is false.

4.4.2.1 Write Precompensation

During Write, it may be desirable to apply an advance or delay on MFM bits when they occur in certain patterns. This advance or delay compensates for peak shift on the disk due to pulse crowding. From an analysis of 4-bit sequences, a preferred precompensation scheme is shown in Table 4-2 and Figure 4-6. Late or early compensation applies only to the third bit of each pattern. No other patterns should be compensated.

The value of compensation should be 10 to 12 nanoseconds, and it is recommended that the value apply to all cylinders.

Table 4-2. Write Data Precompensation

Data Sequence	Direction of Shift
dcba	
0000	On Time Clock
0001	Late Clock
0010	On Time Data
0011	Early Data
0100	--
0101	--
0110	Late Data
0111	On Time Data
1000	Early Clock
1001	On Time Clock
1010	On Time Data
1011	Early Data
1100	--
1101	--
1110	Late Data
1111	On Time Data

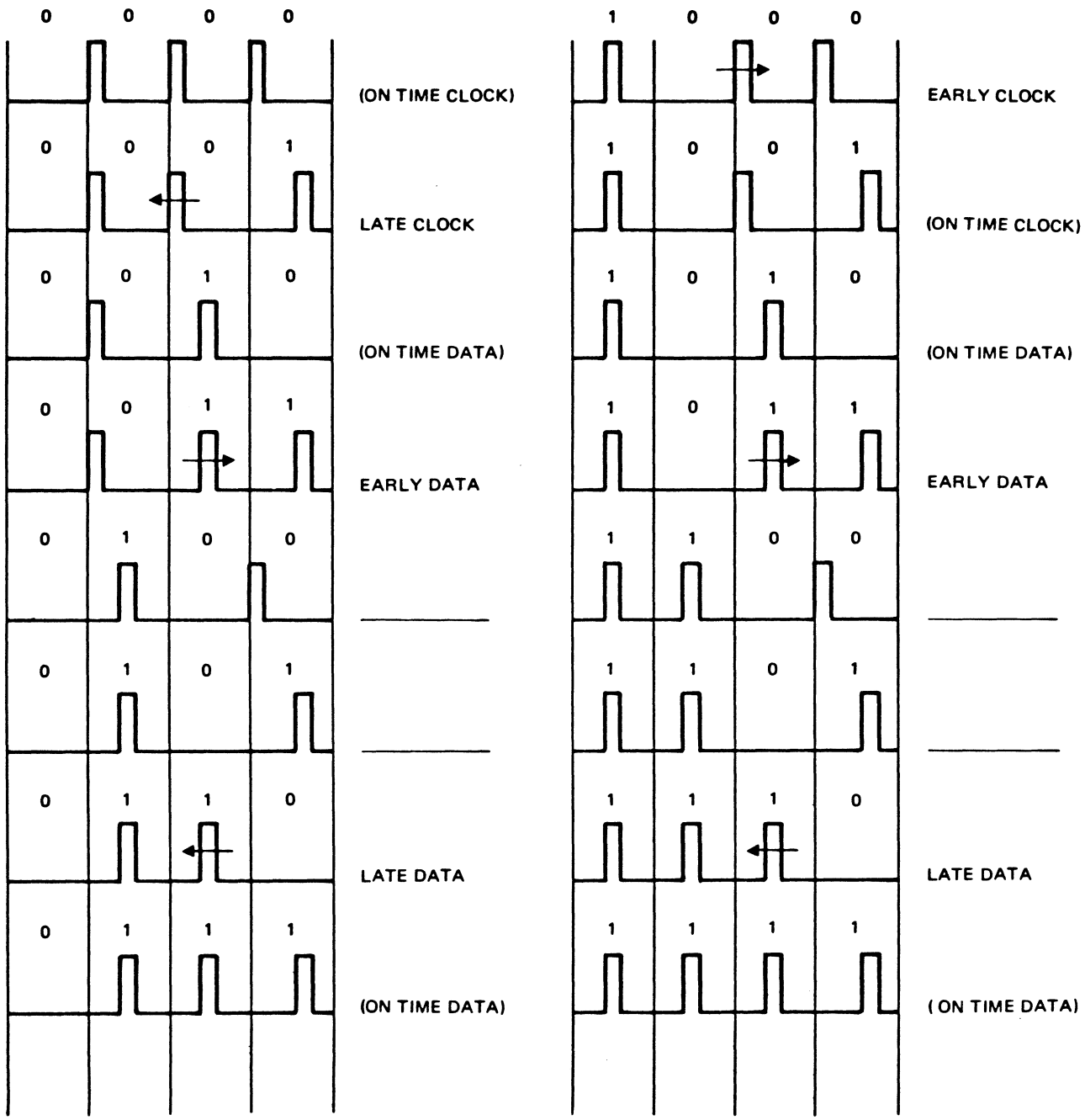


Figure 4-6. Write Data Precompensation

SECTION V

MAINTENANCE

5.1 GENERAL

This section provides information necessary for the maintenance of the Pyxis 7/13/20/27 Disk Storage Drive. Included are removal and replacement procedures for major subassemblies and a description of the built-in diagnostics. Pyxis requires no preventive maintenance and has no adjustments.

5.2 DIAGNOSTICS

The Pyxis diagnostics are divided into three sections: 1) Power-up Diagnostics, 2) Operational Error, and 3) Fault Diagnostics.

5.2.1 Power-Up Diagnostics

During the power-up sequence in the drive, a number of automatic diagnostic routine sequences are performed before the drive becomes ready for system usage. When a fault occurs, an appropriate error code is displayed in the fault indicators. Table 5-1 lists the description of these tests and the applicable error code.

The Power On LED is used to flash error messages when fault conditions occur in the drive. A 4-bit binary code is used (long flash = logic 1 and short flash = logic 0) with the most significant bit occurring first. (e.g. short, short, long, long = 3(0011)

Table 5-1. Power-up Sequence Error Codes

Error Code	Error
1(0001)	No index track data burst at track 2 or track 3
2(0010)	No flag 0 from track 0 detector
3(0011)	Motor speed exceeds ±1% tolerance
5(0101)	Flag 0 always true
9(1001)	Microprocessor self-test failed
10(1010)	No Index
11(1011)	Motor not up to speed

The power-up sequence error codes are detailed in the following paragraphs

5.2.1.1 Codes 9, 10 and 11

The first check is a microprocessor self-test. A check sum is performed on all the code bytes, and failure results in the display of fault code 9. Following the self-test, the microprocessor checks for an Index pulse (Hall sensor output) from the dc motor. If this does not occur during a period of 8 seconds, then fault code 10 is displayed. Since this condition is likely to be the result of the dc motor not starting, the microprocessor attempts to reduce head/disk static friction (during a period of 8 seconds) by moving the positioner four times (one track in alternate directions).

The dc motor speed is then checked to determine if it is within 3600 rpm ±1%. Each check takes one motor revolution, and during this time the Power On LED is flashed at intervals of approximately 0.5 second. If the processor does not see four consecutive speed samples correct to ±1% within 25 seconds, it will display fault code 11.

5.2.1.2 Codes 5 and 2

When the speed check is successfully completed, Write Fault interrupts are enabled. The microprocessor then begins the recalibration of the actuator to track 00. Two possible fault codes may occur. If Flag 00 does not go false within 25 steps towards the center of the disk, fault code 5 will be displayed. After going false, if Flag 00 cannot then be set true within 512 steps in the out direction, fault code 2 is displayed.

5.2.1.3 Codes 1 and 3

After calibrating the actuator to track 00, the processor initiates a routine to select the correct Index pulse. The actuator is moved to track -2 to find the index data burst on head 0 and so select the corresponding Hall sensor phase, thus establishing Index. This operation involves checking for the data burst on track -3 if it cannot be located in track -2. Failure to complete this operation results in fault code 1 if link B is present and does not if link B is cut. The actuator is then re-positioned on track 00, and a final check made on the dc motor speed. If it is not within ±1% tolerance, fault code 3 is displayed.

At the successful completion of the power-up routine, Ready and Track 00 are both set true and the head selects are enabled.

5.2.2 Operational Error Check

During normal system usage and/or diagnostic self-testing, a number of built-in self-tests are performed. If any error conditions are detected by the microprocessor, an error code is displayed by the Power On LED indicator. Table 5-2 lists the tests and the applicable error codes.

Table 5-2. Operational Error Codes

Error Code	Error
4(0100)	Motor speed exceeds +10%, -5% tolerance during normal operation.
6(0110)	Step pulse while Write Gate is true
7(0111)	Static Write Fault condition: 1) Write current and no Write Gate, or 2) No write current, no Write Gate, or 3) More than one read/write head selected, or 4) 12-volt supply below 10.3 volts, or 5) 5-volt supply below 4.5 volts

The operational error codes are detailed in the following paragraphs.

5.2.2.1 Codes 4 and 6

While the processor is waiting for a step pulse from the interface, it continuously monitors the dc motor speed. Should the speed vary from nominal by more than +10% or -5%, fault code 4 will be displayed. The processor will not allow a step pulse to be received while Write Gate is true. This is considered to be a catastrophic controller fault. The drive returns to Write Gate status and displays fault code 6.

5.2.2.2 Code 7

On receipt of a Write Fault interrupt from the drive's hardware detection circuitry, the processor latches this condition, delays for 2 seconds and samples the hardware input to check if the Write Fault condition still exists. If it does, fault code 7 is displayed. If not, the processor enters the power-up routine thus setting the actuator to track 00.

5.2.3 Fault Diagnostics

Table 5-3 shows the likely causes and corrective action for power-up sequence and operational faults. The simplest action is to remove and replace either the master electronics board or motor speed board and verify that the fault code persists.

Table 5-3. Fault Diagnostics

Fault Code	Possible Causes	Corrective Action
1	a. Faulty flag 00 position	Contact service organization
	b. Fault in data burst detection circuitry	Replace master board
	c. Fault in head 0 or preamp board	Contact service organization or replace preamp board
2, 5	a. Transit lock label not removed	Remove
	b. Connector fault between motor speed board and stepper motor/flag 00 assembly	Check connector and/or replace board
	c. Short circuit between motor speed board and casting	Reassembly board
	d. Faulty flag 00 transducer	Contact service organization
	e. Fault in stepper motor control circuitry	Replace master board or motor speed board
	f. Faulty stepper motor	Contact service organization
	g. Defective positioner assembly	Contact service organization
3, 4	Brake failure	Replace
10, 11	a. No 12V supply	Check supply/connector
	b. Faulty dc motor/Hall element	Contact service organization
	c. Faulty motor speed board	Replace
6	a. Controller/Interface fault	Check controller/connector
	b. Faulty master board	Replace
7	a. Faulty master board	Replace
	b. Faulty preamp board	Replace
	c. 5V and/or 12V too low	Check supply
9	Faulty microprocessor	Replce master board

In practice, however, the most likely sources of trouble are (a) power supplies out of tolerance, and (b) step rates out of the drive constraints. In any event, the following should be verified:

1. The shipping label is removed

2. The connectors are clean and properly attached

3. The interface terminator is present, or absent, according to the configuration

4. Link A is removed for the 3.1 milliseconds to 8.0 milliseconds range

5. The drive chassis is free of any system metalwork

6. The dc power lines are short-twisted pairs

7. Data and control cables are properly shielded and do not run close to high current switching circuits

5.3 REMOVAL AND REPLACEMENT PROCEDURES

The following paragraphs detail the removal and replacement procedures for the major Pyxis subassemblies. Be sure to read each procedure before attempting removal or replacement.

There is no preventive maintenance, and there are no adjustments on the drive. Field repair is restricted to brake and board replacement and selection of the spare Hall sensor.

NOTE

Repair to the HDA can only be effected by the use of Ampex special tooling and Class 100 cleanroom conditions. Users are reminded that removal of the HDA covers will render the warranty void.

The tools required for field repair consist of the following:

1. Pozidrive screwdriver, No. 2

2. Box spanner, 1/4 in. AF

3. Hex driver, Allen, 5/64 in.

4. Feeler gauge, .015 in.

Access to the brake, preamplifier board and motor speed board is accomplished by first removing the master electronics board and then the side bracket/facia assembly.

5.3.1 Master Electronics Board Removal

NOTE

On drives fitted with the vented facia and two-piece side frames, remove the facia before removing the master board.

1. Using the Allen hex driver, remove the six screws securing the board to the drive. Carefully loosen connector J4 from the preamplifier board and lift the master board free from the drive.

2. Disconnect flat cable connector J5 from the motor speed control board.

5.3.2 Master Electronics Board Replacement

1. Connect flat cable connector J5 to the motor speed control board, ensuring that the connector is properly polarized.

2. Ensure that connector J4 mates properly with the pre-amplifier board.

3. Secure the board to the drive with six screws.

5.3.3 Brake Removal

1. Remove the master electronics board as described in paragraph 5.3.2, but do not disconnect flat cable connector J5 from the motor speed control board.

2. Disconnect brake connector J6 from the motor speed control board.

3. Using the box spanner, remove the two nuts securing the brake to the casting and remove the brake.

5.3.4 Brake Replacement

1. Position the replacement brake, and refit the nuts loosely.

2. Place the feeler gauge between the motor rotor and the brake pad, and push the brake body so that the plunger is fully depressed against its spring.

3. Ensure that the center line of the brake lines up with the motor center, and lock the nuts.

4. Reconnect the power connector, ensuring correct polarization.

WARNING

Before powering up the drive, make sure the motor is free of obstructions. Do not touch the spinning motor.

5. Power up the drive with the master electronics board lying alongside, and verify that the brake does not contact the motor rotor. Ensure that the master electronics board is isolated from metallic parts.

6. Power off and verify that stopping time is within 5 to 8 seconds.

7. Refit the master electronics board as described in paragraph 5.3.2.

5.3.5 Motor Speed Control Board Removal

1. Remove the master electronics board as described in paragraph 5.3.1.

2. Remove the screw securing the left mounting bracket to the casting.

3. Disconnect brake connector J6, dc motor connector J9 and stepper motor connector J8 from the motor speed control board.

4. Unscrew both the rear standoff with ground tab and left standoff; remove the motor speed board.

5. If the spare Hall element is to be connected, remove the link on the motor speed board and reconnect it as shown on the Motor Speed Control PWBA Assembly Drawing, Appendix A.

5.3.6 Motor Speed Control Board Replacement

1. Install the replacement motor speed board, insert the ground tab and tighten the rear standoff. Insert and tighten the left standoff.

2. Reconnect stepper motor connector J8, dc motor connector J9 and brake connector J6, ensuring correct polarization of the connectors.

3. Insert the screw securing the left mounting bracket to the casting.

4. Refit the master electronics board as described in paragraph 5.3.2.

5.3.7 Preamplifier Board Removal/Replacement

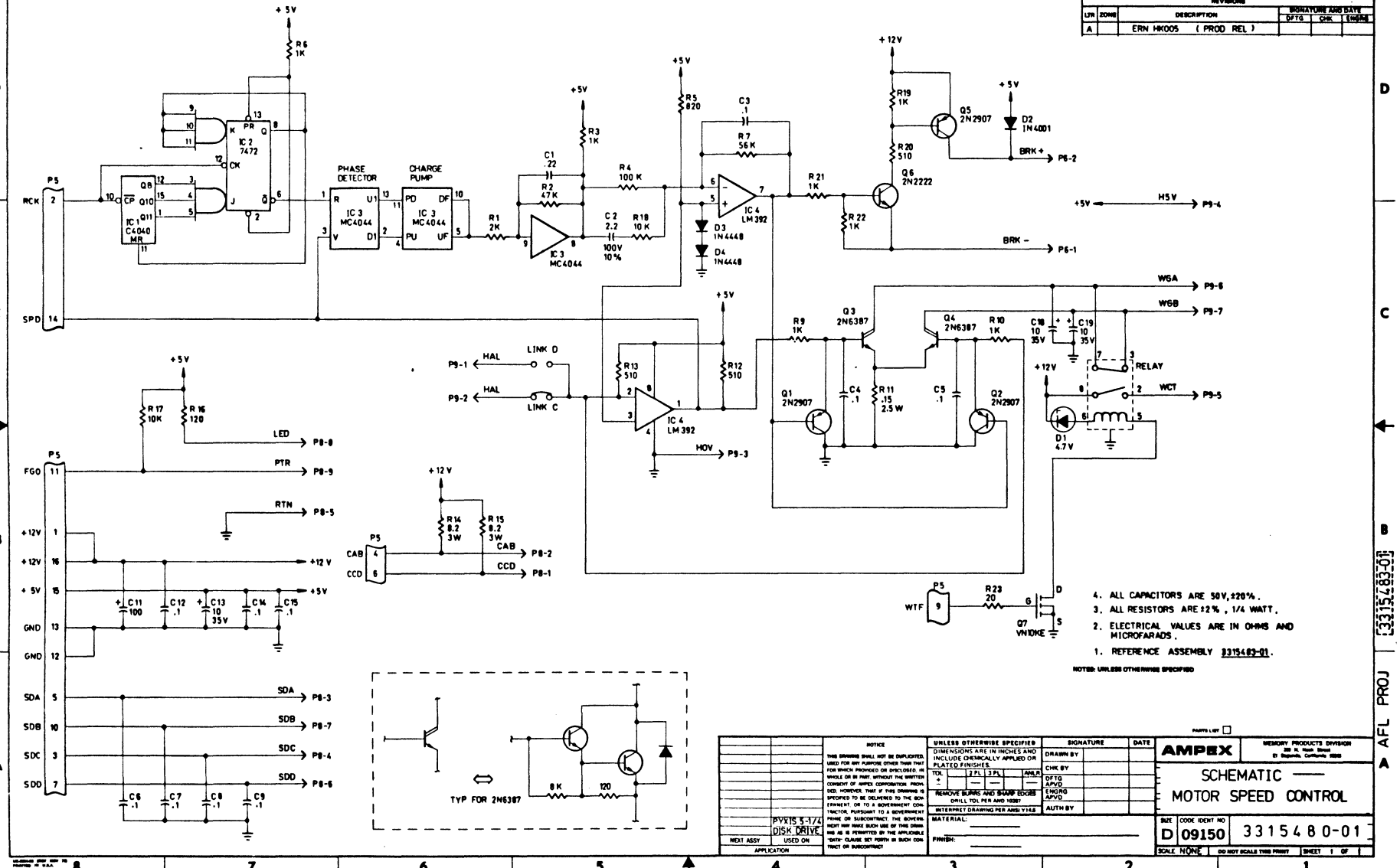
(Not recommended as field replaceable).

APPENDIX A

REFERENCE DRAWINGS

This appendix contains schematics and assembly drawings for the Pyxis disk drive.

PCBA	SCHEMATIC	ASSY. DWG.
Master Electronics Board	3315470-01	3315473-01
Motor Speed Control Board	3315480-01	3315483-01
Preamplifier Board	3315490-01	3315493-01



REVISIONS				
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE DFTG	CHK
A		ERN HK005 (PROD REL)		

4. ALL CAPACITORS ARE 50V, ±20%.
3. ALL RESISTORS ARE ±2%, 1/4 WATT.
2. ELECTRICAL VALUES ARE IN OHMS AND MICROFARADS.
1. REFERENCE ASSEMBLY 3315483-01.

NOTES: UNLESS OTHERWISE SPECIFIED

NEXT ASSY	USED ON	PVRIS 5-174 DISK DRIVE	APPLICATION

NOTICE: THIS DRAWING SHALL NOT BE DUPLICATED, USED FOR ANY PURPOSE OTHER THAN THAT FOR WHICH PROVIDED OR DISCLOSED, IN WHOLE OR IN PART, WITHOUT THE WRITTEN CONSENT OF AMPEX CORPORATION. PROVIDED, HOWEVER, THAT IF THIS DRAWING IS SPECIFIED TO BE DELIVERED TO THE GOVERNMENT OR TO A GOVERNMENT CONTRACTOR, PURSUANT TO A GOVERNMENT PRIME OR SUBCONTRACT, THE GOVERNMENT MAY MAKE SUCH USE OF THIS DRAWING AS IS PERMITTED BY THE APPLICABLE "DATA" CLAUSE SET FORTH IN SUCH CONTRACT OR SUBCONTRACT.

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES.
TOL: ANGLE ± — | 2 PL ± — | 3 PL ± —
REMOVE BURRS AND SHARP EDGES
DRILL TOL PER ANSI 10387
INTERPRET DRAWING PER ANSI Y14.5

SIGNATURE / DATE
DRAWN BY
CHK BY
DFTG APVD
ENGRG APVD
AUTH BY
MATERIAL:
FINISH:

PARTS LIST

AMPEX — MEMORY PRODUCTS DIVISION, 200 N. Main Street, El Segundo, California 90245

SCHEMATIC
MOTOR SPEED CONTROL

SIZE D | CODE IDENT NO 09150 | 3315480-01

SCALE NONE | DO NOT SCALE THIS PRINT | SHEET 1 OF

AFL PROJ 3315483-01

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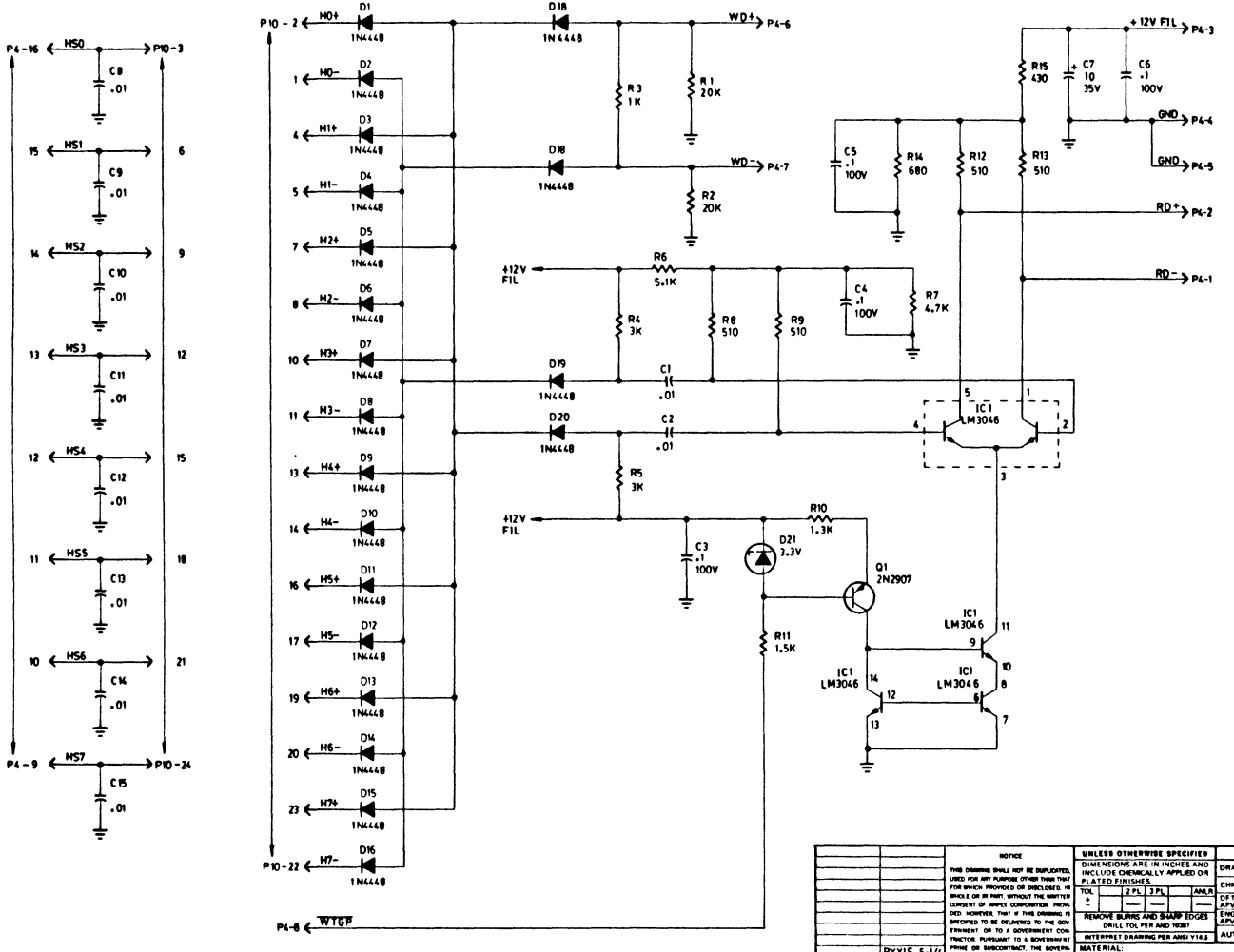

4. ALL CAPACITORS ARE 50V, ±20%.
3. ALL RESISTORS ARE ±2%, 1/4 WATT.
2. ELECTRICAL VALUES ARE IN OHMS AND MICROFARADS.
1. REFERENCE ASSEMBLY 3315493-01.

NOTES: UNLESS OTHERWISE SPECIFIED

3315490-01

AFL PROJ

PARTS LIST ☐

NEXT ASSY	USED ON
APPLICATION	PYXIS 5-1/4 DISK DRIVE

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UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES.
TOL ± | 2 PL | 3 PL | ANGLE
REMOVE BURRS AND SHARP EDGES
INTERPRET DRAWING PER ANSI Y14.5

SIGNATURE		DATE
DRAWN BY		6/28
CHK BY		
DFTG APVD		
ENGRG APVD		
AUTH BY		

MATERIAL:
FINISH:

AMPEX MEMORY PRODUCTS DIVISION

SCHEMATIC —
PRE-AMPLIFIER BD

SIZE	CODE IDENT NO	
D	09150	3315490-01

SCALE NONE | DO NOT SCALE THIS PRINT | SHEET | OF

REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE DFTG	CHK	ENGRG
A		ERN HK005 (PROD REL)			

REF TABLE	
LAST USED	NOT USED
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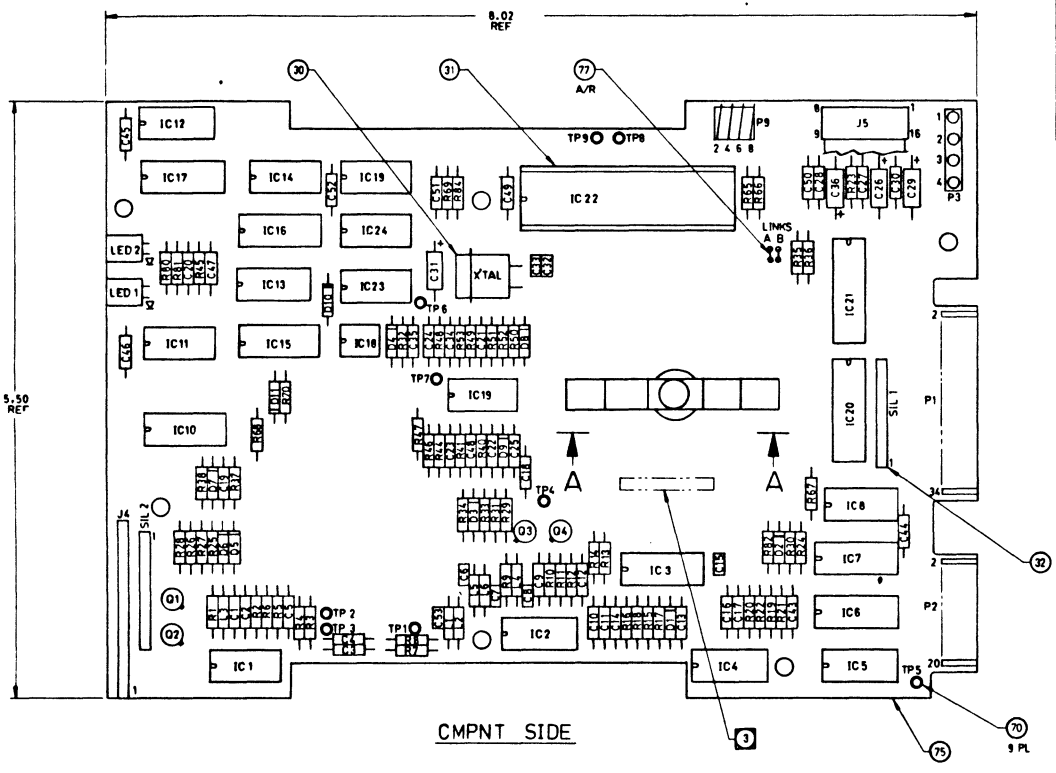
Q 4	——
D 11	——
C 53	C37 THRU C42
R 84	R54 THRU 64, R71 THRU 79, 83, R 39, 42, 43
L 6	——



CMPNT SIDE

10 GRAPHITE DISC TO BE CONCENTRIC WITH CIRCULAR PAD WITHIN .010.

9. MAXIMUM COMPONENT HEIGHT ABOVE PWB TO BE .25.

8. CROP ALL COMPONENT LEADS TO .060 MAX.

7. REFERENCE SCHEMATIC 3315470-01.

6. HEAVY LINE ON DIODES DENOTES CATHODE END.

5. PLUS SIGN ON CAPACITORS DENOTES POSITIVE LEAD.

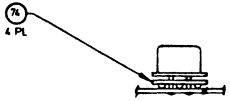
4. COMPONENT REF DESIGNATIONS ARE FOR REF ONLY.

3 MARK PART NO. & ISSUE LTR PER AMPEX SPEC 3124500, PARA 3.1.

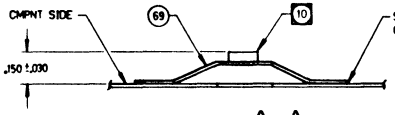
2. PART NO. TO BE 3315473-01.

1. ASSEMBLE PER AMPEX STANDARDS.

NOTES: UNLESS OTHERWISE SPECIFIED



INSTALLATION OF Q1 THRU Q4



VIEW A-A

NEXT ASSY	USED ON
3315444-01	
3315443-01	PVXIS 5-1/4
3315442-01	DISK
3315441-01	DRIVE

APPLICATION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES.
TOL ± 2 PL .3 PL ANGL —
REMOVE BURRS AND SHARP EDGES
DRILL TOL PER ANSI 1038?
INTERPRET DRAWING PER ANSI Y14.5
MATERIAL:
FINISH:

SIGNATURE	DATE
DRAWN BY	
CHK BY	
DFTG APVD	
ENGRG APVD	
AUTH BY	

PARTS LIST 50

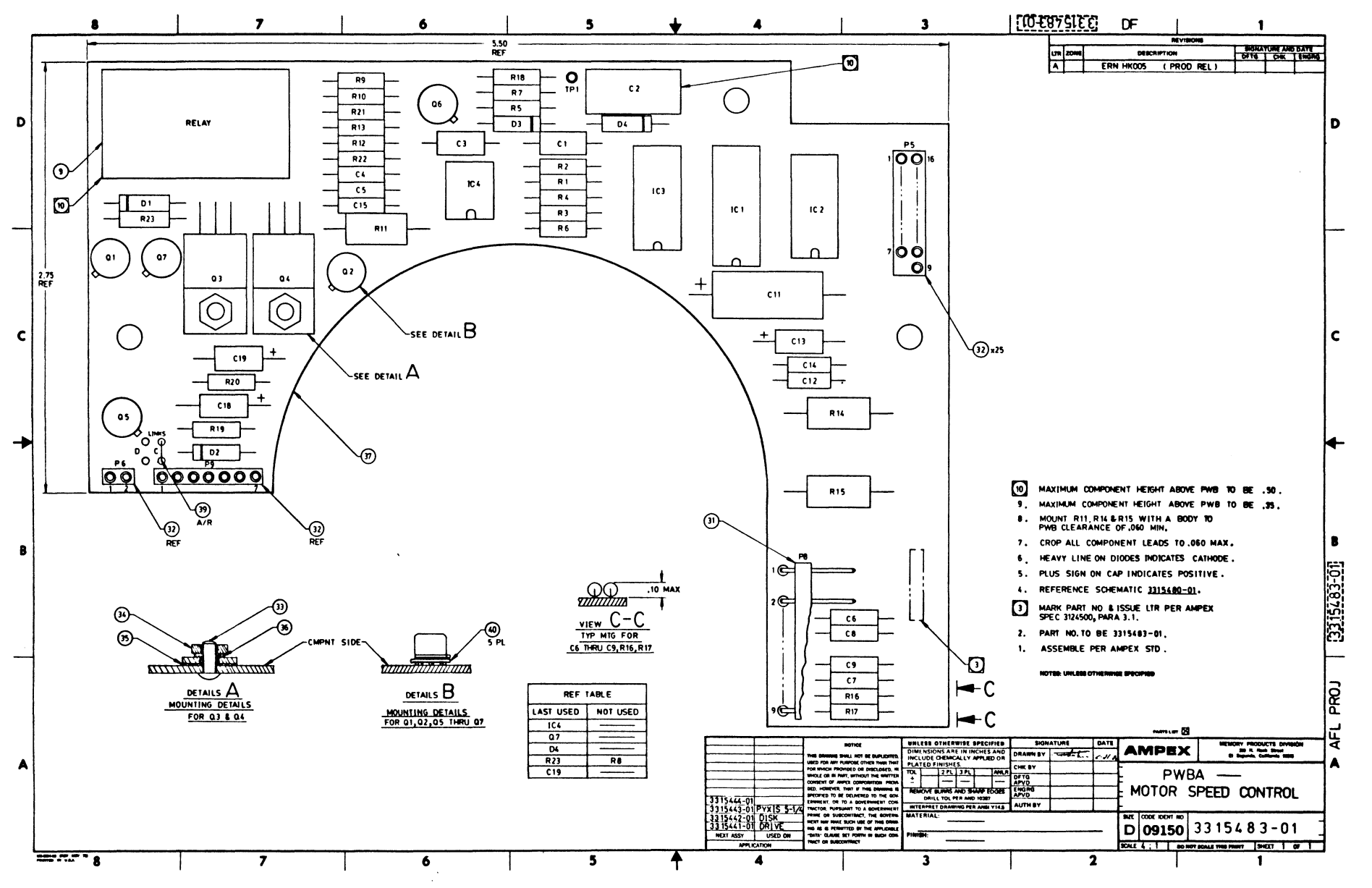
AMPEX — MEMORY PRODUCTS DIVISION, 200 R. Main Street, El Segundo, California 90245

PWBA —— MASTER ELECTRONICS

SIZE	CODE IDENT NO	3315473-01
D	09150	

SCALE 2/1 — DO NOT SCALE THIS PRINT — SHEET 1 OF 1

AFL PROJ 3315473-01


3315483-01 DF
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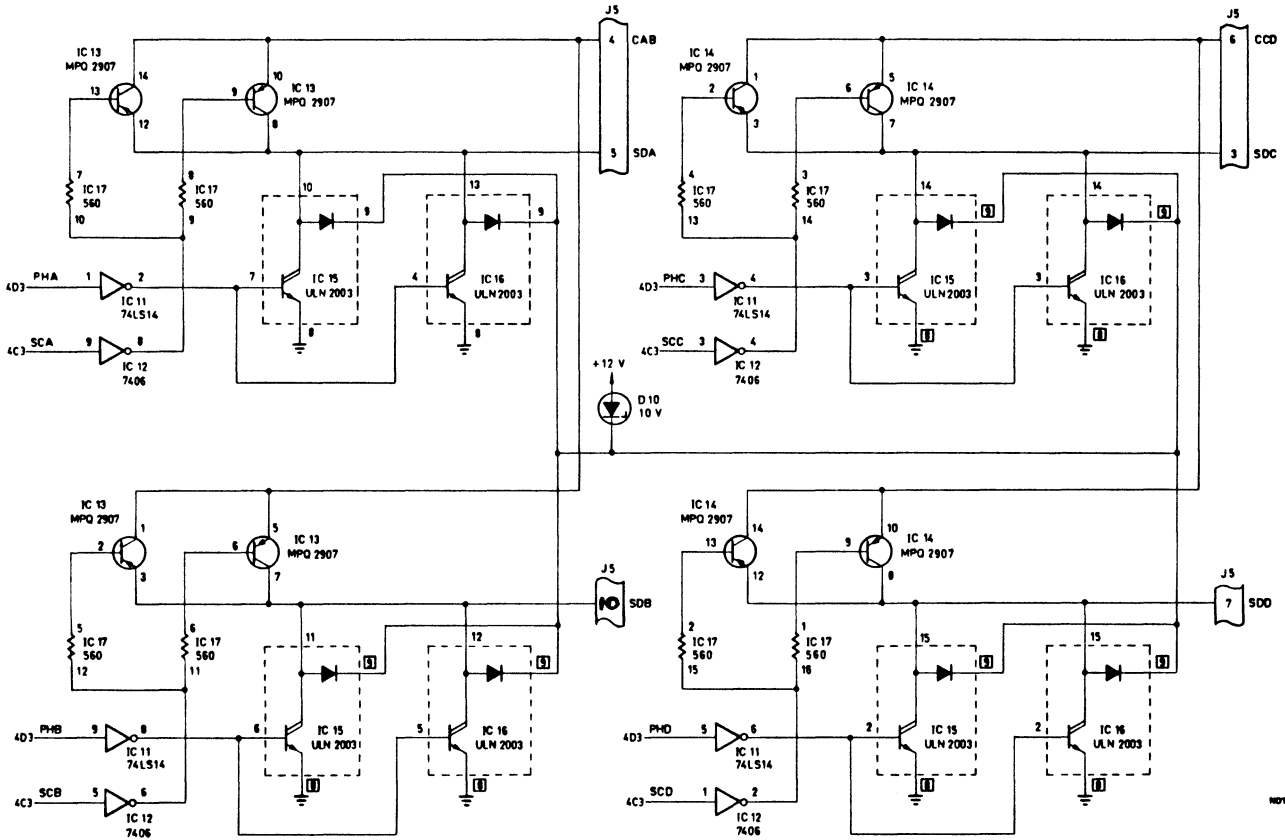
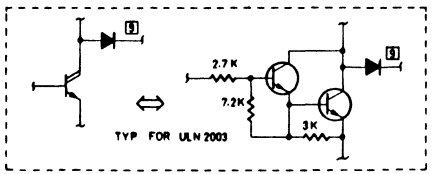
A ERN HK005 (PROD REL)
5.50 REF
2.75 REF
RELAY
R9 R10 R21 R13 R12 R22 C4 C5 C15 R11
Q6
R18 R7 R5 D3
TP1
C2 D4
C3 C1
IC4
R2 R1 R4 R3 R6
IC3
IC1
IC2
P5
D1 R23
Q1 Q7 Q3 Q4 Q2
C11
C13 C14 C12
C19 R20 C18 R19 D2
Q5
LINKS D C
P6 P9
R14
R15
P8
C6 C8 C9 C7 R16 R17
SEE DETAIL B
SEE DETAIL A
A/R
REF
REF
x25
.10 MAX
VIEW C-C
TYP MTG FOR C6 THRU C9, R16, R17
CMPNT SIDE
5 PL
DETAILS A
MOUNTING DETAILS FOR Q3 & Q4
DETAILS B
MOUNTING DETAILS FOR Q1, Q2, Q5 THRU Q7
REF TABLE
LAST USED NOT USED
IC4
Q7
D4
R23 R8
C19
10. MAXIMUM COMPONENT HEIGHT ABOVE PWB TO BE .50.
9. MAXIMUM COMPONENT HEIGHT ABOVE PWB TO BE .35.
8. MOUNT R11, R14 & R15 WITH A BODY TO PWB CLEARANCE OF .060 MIN.
7. CROP ALL COMPONENT LEADS TO .060 MAX.
6. HEAVY LINE ON DIODES INDICATES CATHODE.
5. PLUS SIGN ON CAP INDICATES POSITIVE.
4. REFERENCE SCHEMATIC 3315480-01.
3. MARK PART NO & ISSUE LTR PER AMPEX SPEC 3124500, PARA 3.1.
2. PART NO. TO BE 3315483-01.
1. ASSEMBLE PER AMPEX STD.
NOTES: UNLESS OTHERWISE SPECIFIED
3315444-01
3315443-01 PYXIS 5-1/4
3315442-01 DISK
3315441-01 DRIVE
NEXT ASSY USED ON
APPLICATION
NOTICE
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES.
TOL ± 2 PL 3 PL ANGLES
REMOVE BURRS AND SHARP EDGES
DRILL TOL PER ANSI Y14.5
INTERPRET DRAWING PER ANSI Y14.5
MATERIAL:
FINISH:
SIGNATURE DATE
DRAWN BY
CHK BY
DFTG APVD
ENG/PG APVD
AUTH BY
PARTS LIST
AMPEX
MEMORY PRODUCTS DIVISION
PWBA — MOTOR SPEED CONTROL
SIZE D CODE IDENT NO 09150 3315483-01
SCALE 4:1 DO NOT SCALE THIS PRINT SHEET 1 OF 1
AFL PROJ
3315483-01

REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE DFTG	CHK	ENGRG
A		ERN HK005 (PROD REL)			





4. INDUCTORS ARE IN MICROHENRY, ±10%.
3. RESISTORS ARE IN OHMS, ±2%, 1/4 WATT.
2. CAPACITORS ARE IN MICROFARADS, 50V OR GREATER.
1. REFERENCE ASSEMBLY 3315473-01.

NOTES: UNLESS OTHERWISE SPECIFIED

PARTS LIST ☐

NEXT ASSY	USED ON
APPLICATION	PYXIS 5¼ DISK DRIVE

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES.
TOL ± | 2 PL | 3 PL | ANGLE
REMOVE BURRS AND SHARP EDGES
DRILL TOL PER ANSI Y14.5
INTERPRET DRAWING PER ANSI Y14.5
MATERIAL:
FINISH:

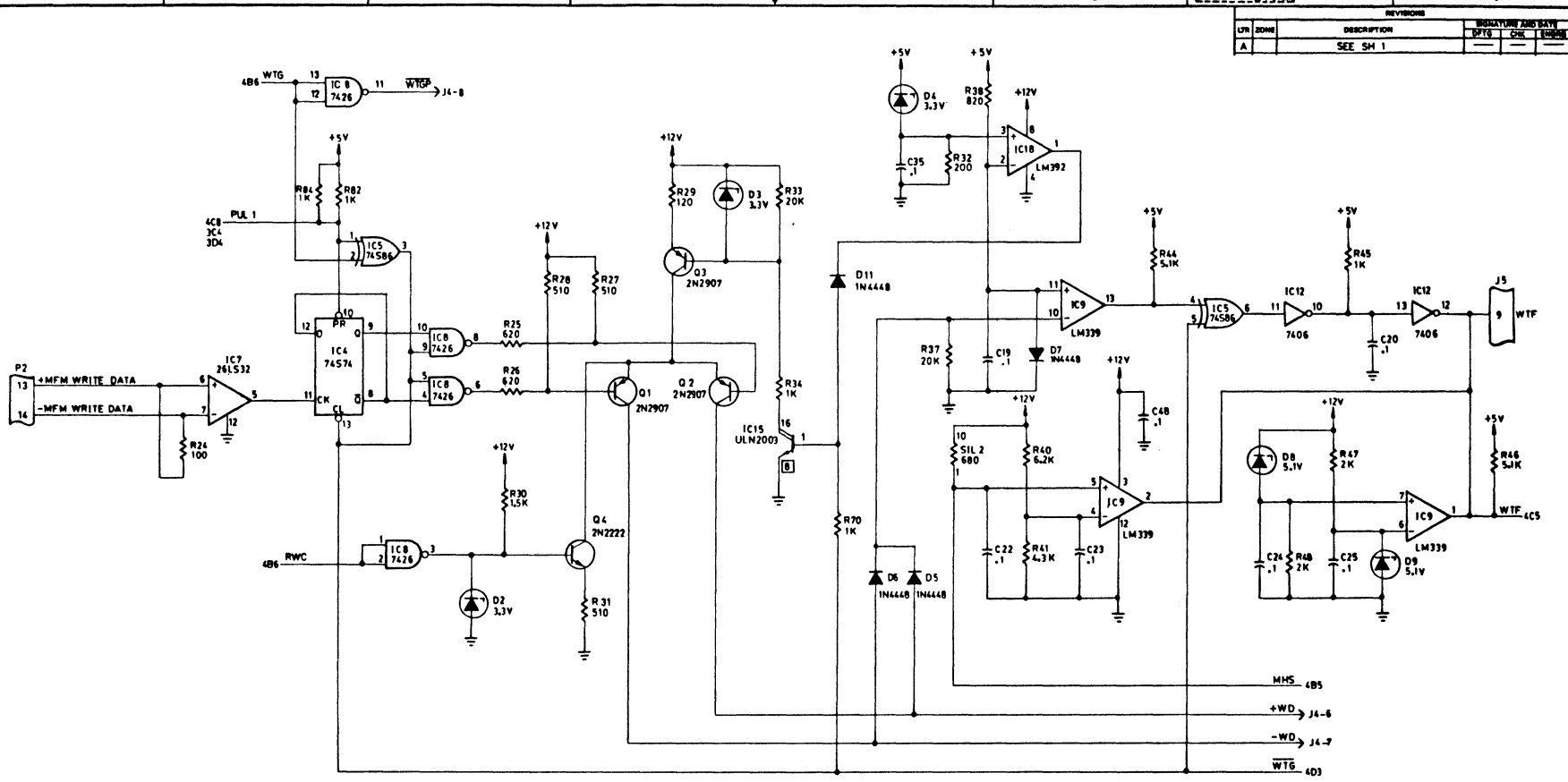
SIGNATURE		DATE
DRAWN BY		6-11-82
CHK BY		
DFTG APVD		
ENGRG APVD		
AUTH BY		

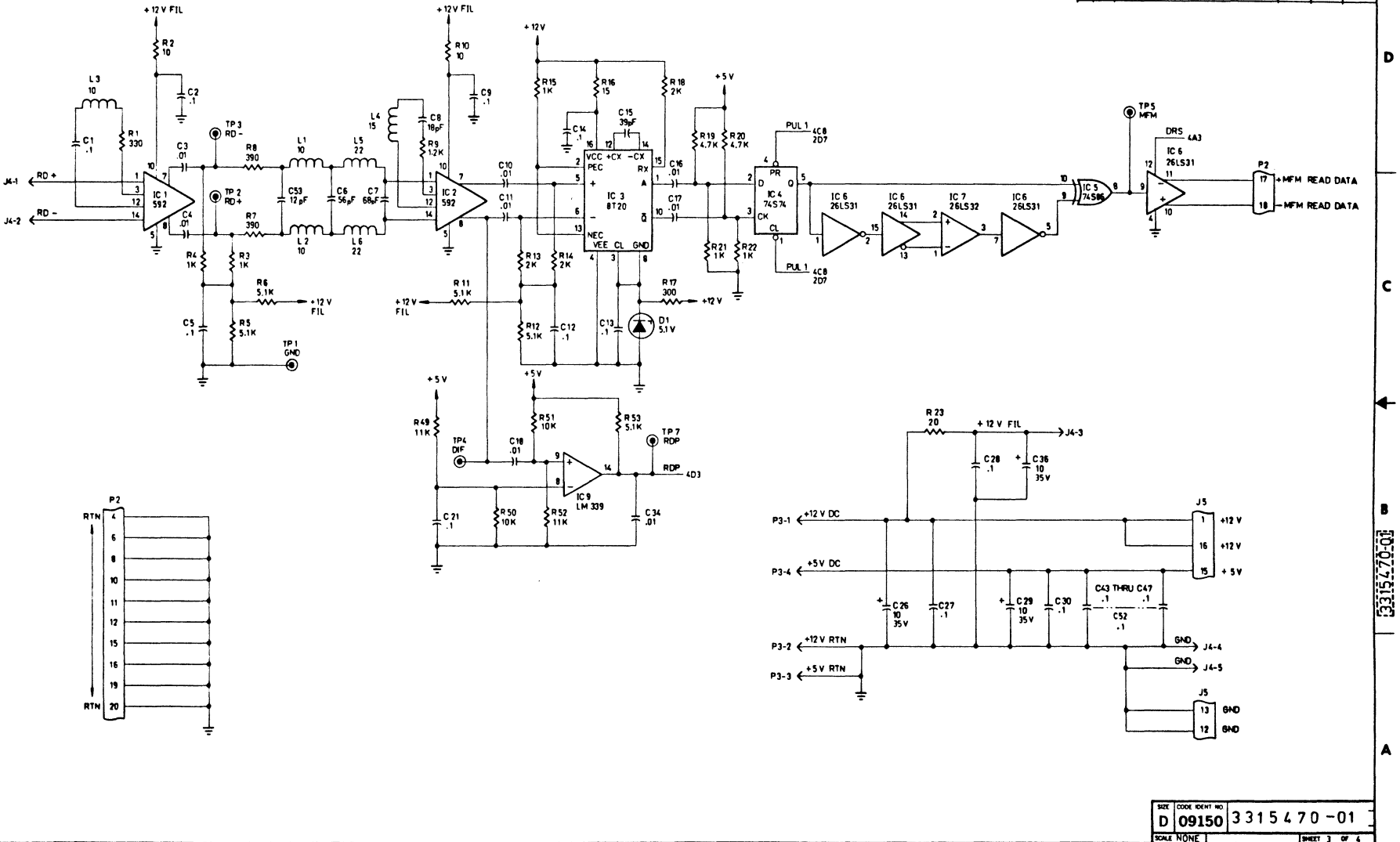
AMPEX
MEMORY PRODUCTS DIVISION
SCHEMATIC — MASTER ELECTRONICS BD

SIZE	CODE IDENT NO.	
D	09150	3315470-01

SCALE NONE | DO NOT SCALE THIS PRINT | SHEET 1 OF 4

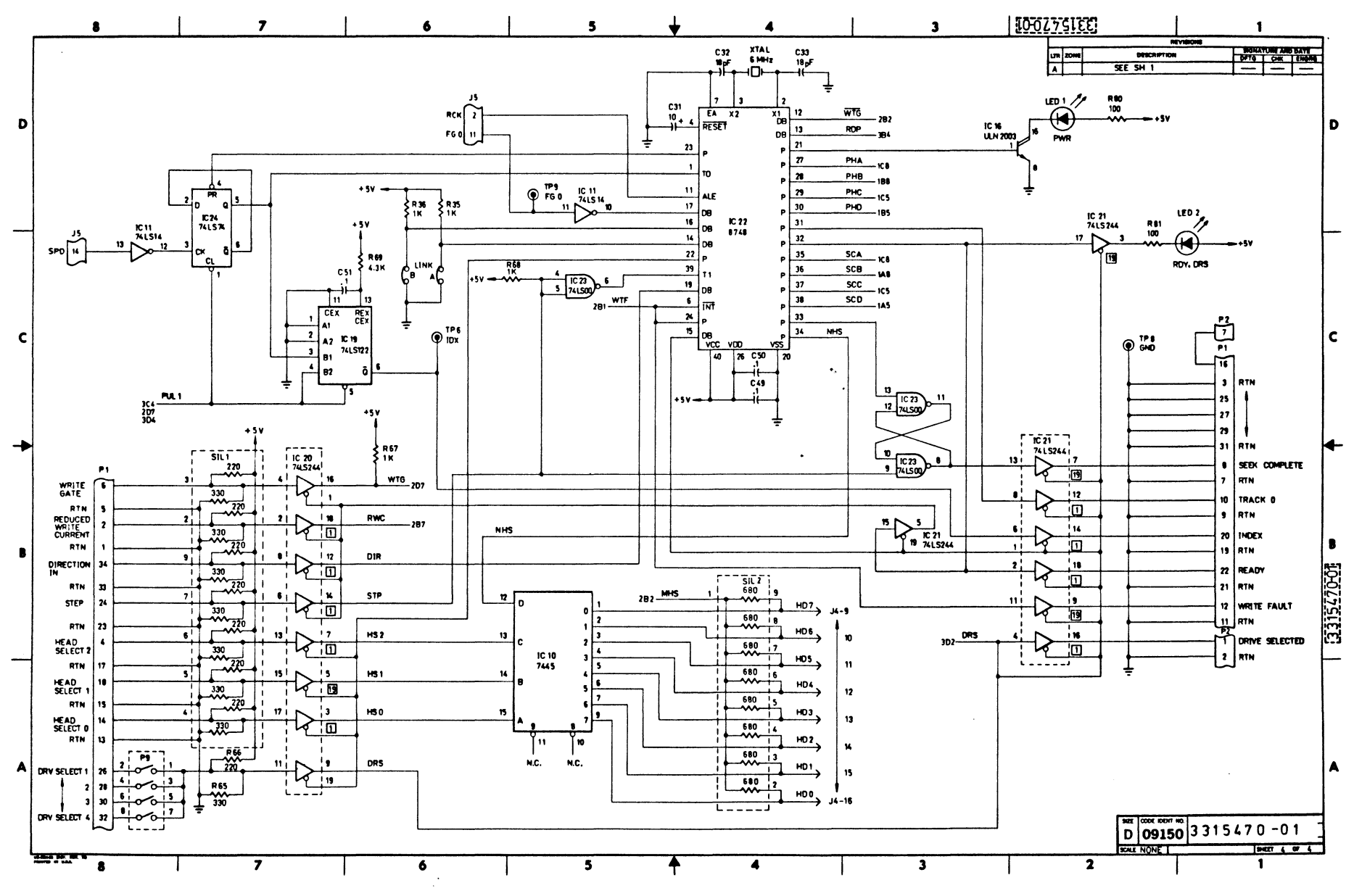
AFL PROJ 3315470-01


REVISIONS
LTR ZONE DESCRIPTION DATE CHK APPD
A SEE SH 1
WTG 4B6
IC 8 7426
WTGP J4-8
PUL 1
4C8 3C4 3D4
IC5 74S86
IC4 74S74
IC7 26LS32
P2
+MFM WRITE DATA
-MFM WRITE DATA
R24 100
R84 1K
R82 1K
R25 620
R26 620
R28 510
R27 510
IC8 7426
Q1 2N2907
Q2 2N2907
Q3 2N2907
R29 120
D3 3.3V
R33 20K
R34 1K
IC15 ULN2003
D11 1N4448
R70 1K
D4 3.3V
R38 820
C35 .1
R32 200
IC18 LM392
R44 5.1K
IC9 LM339
R37 20K
C19 .1
D7 1N4448
IC5 74S86
IC12 7406
R45 1K
C20 .1
J5
WTF
C48 .1
SIL 2 680
R40 6.2K
C22 .1
R41 4.3K
C23 .1
D8 5.1V
R47 2K
R46 5.1K
WTF 4C5
C24 .1
R48 2K
C25 .1
D9 5.1V
R30 1.5K
Q4 2N2222
RWC 4B6
D2 3.3V
R31 510
D6 1N4448
D5 1N4448
MHS 4B5
+WD J4-6
-WD J4-7
WTG 4D3
3315470-01
SIZE D
CODE IDENT NO. 09150
3315470-01
SCALE NONE
SHEET 2 OF 4

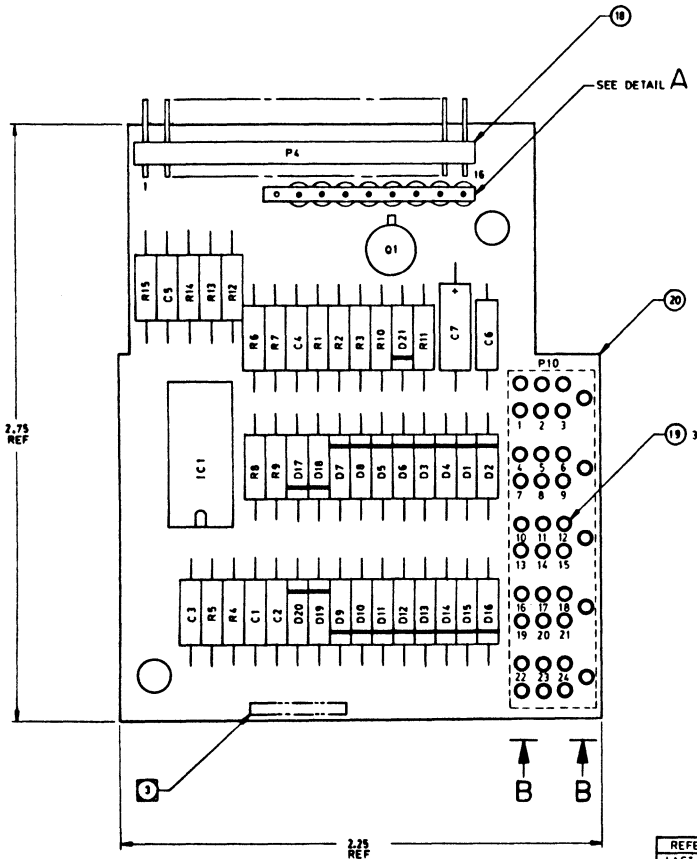


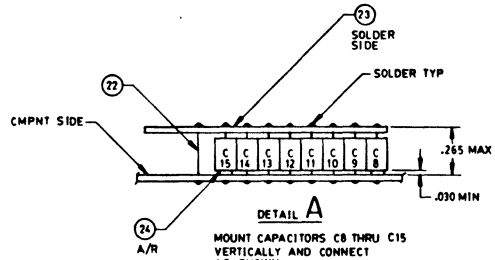
SIZE	CODE IDENT NO	
D	09150	3315470-01

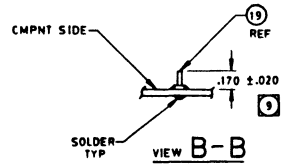
SCALE NONE SHEET 3 OF 4


3315470-01
REVISIONS
LTR ZONE DESCRIPTION DATE (YR/MO/DA) APPD CHK ENGRG
A SEE SH 1
C32 18pF
XTAL 6 MHz
C33 18pF
C31 10 + 4
IC 22 8748
EA X2 X1 RESET
WTG ROP PHA PHB PHC PHD SCA SCB SCC SCD NHS WTF
VCC VDD VSS
C50 .1
C49 .1
J5
RCK FG 0
TP9 FG 0
IC 11 74LS14
IC 24 74LS74
PR D Q CK CL
SPD
PUL 1
3C4 2D7 3D4
R36 1K
R35 1K
R69 4.3K
C51 .1
LINK
IC 19 74LS122
CEX REX A1 A2 B1 B2
TP6 IDX
R68 1K
IC 23 74LS00
WTF 2B1
+5V
LED 1 PWR
R80 100
IC 16 ULN 2003
LED 2 RDY, DRS
R81 100
IC 21 74LS244
TP8 GND
P2 P1
RTN SEEK COMPLETE TRACK 0 INDEX READY WRITE FAULT DRIVE SELECTED
P1
WRITE GATE
REDUCED WRITE CURRENT
DIRECTION IN
STEP
HEAD SELECT 2
HEAD SELECT 1
HEAD SELECT 0
DRV SELECT 1 2 3 4
SIL 1 220 330
IC 20 74LS244
WTG 2D7
RWC 2B7
DIR
STP
HS2
HS1
HS0
DRS
R67 1K
R66 220
R65 330
P9
NHS
IC 10 7445
N.C. N.C.
SIL 2 680
HD7 HD6 HD5 HD4 HD3 HD2 HD1 HD0
J4-9 J4-16
2B2 MHS
3D2 DRS
SIZE D
CODE IDENT NO. 09150
3315470-01
SCALE NONE
SHEET 4 OF 4

REVISIONS				
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE DFT'G	CHK
A		ERN HK005 (PROD REL)		







9. PIN TO BE CUT TO DIM SHOWN.
8. REFERENCE SCHEMATIC 3315490-01.
7. HEAVY LINE ON DIODES INDICATES CATHODE.
6. PLUS SIGN ON CAP INDICATES POSITIVE.
5. MAXIMUM COMPONENT HEIGHT ABOVE PWB TO BE .25.
4. CROP ALL COMPONENT LEADS TO .060 MAX.
3. MARK PART NO. AND ISS LTR PER AMPEX SPEC 3124500, PARA 3.1.
2. PART NO. TO BE 3315493-01.
1. ASSEMBLE PER AMPEX STD.

NOTES: UNLESS OTHERWISE SPECIFIED

REFERENCE TABLE	
LAST USED	NOT USED
R15	
C15	
D21	
IC1	
Q1	

NEXT ASSY	USED ON	APPLICATION
3315444-01		
3315443-01	PYXIS 5-1/4	
3315442-01	DISK	
3315441-01	DRIVE	

NOTICE: THIS DRAWING SHALL NOT BE DUPLICATED, USED FOR ANY PURPOSE OTHER THAN THAT FOR WHICH PROVIDED OR DISCLOSED, IN WHOLE OR IN PART, WITHOUT THE WRITTEN CONSENT OF AMPEX CORPORATION. PROVIDED, HOWEVER, THAT IF THIS DRAWING IS SPECIFIED TO BE DELIVERED TO THE GOVERNMENT, OR TO A GOVERNMENT CONTRACTOR, PURSUANT TO A GOVERNMENT PRIME OR SUBCONTRACT, THE GOVERNMENT MAY MAKE SUCH USE OF THIS DRAWING AS IS PERMITTED BY THE APPLICABLE "DATA" CLAUSE SET FORTH IN SUCH GOVERNMENT OR SUBCONTRACT

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES. TOL ± 2 PL ± 3 PL ± ANGLES ±. REMOVE BURRS AND BREAK EDGES. DRILL TOL PER AMP 10287. INTERPRET DRAWING PER ANSI Y14.5. MATERIAL: FINISH:

SIGNATURE	DATE
DRAWN BY	6/11/82
CHK BY	
DFTG APVD	
ENGRG APVD	
AUTH BY	

PARTS LIST ☒

AMPEX — MEMORY PRODUCTS DIVISION, 201 N. Nash Street, El Segundo, California 90245

PWBA — PRE-AMPLIFIER

SIZE D | CODE IDENT NO 09150 | 3315493-01

SCALE 4/1 | DO NOT SCALE THIS PRINT | SHEET 1 OF 1

AFL PROJ 3315493-01