7200 INTERFACE ADAPTER

Chapter 1

GENERAL INFORMATION

1-1 INTRODUCTION

This chapter contains general information pertaining to the AMCOMP 7200 Interface Adapter (figure 1-1) for the 8500 Series Disc Memory Units. The information in this chapter consists of general description, functional description, physical description and optional configurations.

1-2 GENERAL DESCRIPTION

The 7200 Interface Adapter Card makes possible the substitution of the AMCOMP 8500 Series Disc Memory Units for the 7200 Series Disc Memory Units. The adapter card is used in the 8500 Disc Unit in conjunction with either the standard 8500 Interface board or the AMCODE board depending on the customers sector length. The interface connector assembly on the rear panel of the 8500 Disc Unit is changed to match the current 7200 interface cable connector.

1-3 FUNCTIONAL DESCRIPTION

The 7200 Interface Adapter Card supplies compatable control lines, signal levels and required line terminations between the Controller and the 8500 Series Disc Memory Units.

1-4 PHYSICAL DESCRIPTION

The 7200 Interface Adapter consists of one printed circuit board installed in the 8500 Disc Memory Unit. The adapter card is plugged into the second card slot nearest to the rear panel of the 8500 Disc Unit. The adapter card overall size is 11.24 inches in length and 5.24 inches in height.

1-5 OPTIONAL CONFIGURATIONS

The 8500 Series Disc Memory Units are available in a variety of configurations depending on speed, whether they are sealed or not sealed, or whether they are equipped with 7200 Interface Adapter Card. Table 1-1 outlines the basic configurations.

TABLE 1-1. OPTIONAL CONFIGURATIONS

MODEL NUMBER	DISC SPEED 1800 RPM	3600 RPM	SEALED		7200 ADAPTER		BASIC UNIT
			YES	NO	YES	NO	
8510	X			X		X	8510
8513	X		X			X	8510
8517	X			X	X		8510
8518	X		X		X		8510
8530		X		X		X	8530
8533		X	X			X	8530
8537		X		X	X		8530
8538		X	X		X		8530

Chapter 2

INSTALLATION AND CHECKOUT

2-1 INTRODUCTION

This chapter contains information pertaining to the unpacking and inspection of the 7200 Interface Adapter.

2-2 UNPACKING AND INSPECTION

The 7200 Interface Adapter is shipped as an integral part of the 8500 Disc Memory. Unpacking and inspection procedures should be as defined by the 8500 Disc Memory Operation and Maintenance Manual.

Chapter 3

INTERFACE

3-1 INTRODUCTION

The chapter contains figure 3-1 which shows the interface line receivers and drivers and the interconnect signals between the controller and the 7200 Interface Adapter and between the 7200 Interface Adapter and the 8500 Disc Memory. These signals are described in the 7200 and 8500 Series Disc Memory Unit Operation and Maintenance Manuals.

3-2 INTERFACE CIRCUITS

The 7200 Interface Adapter logic used is standard positive logic having the following levels.

LOGICAL 1 (HIGH) = 3.0 $\pm$ 0.6 VDC

LOGICAL 0 (LOW) = 0.2 $\pm$ 0.2 VDC

The adapter card drivers and receivers are shown in figure 3-2.

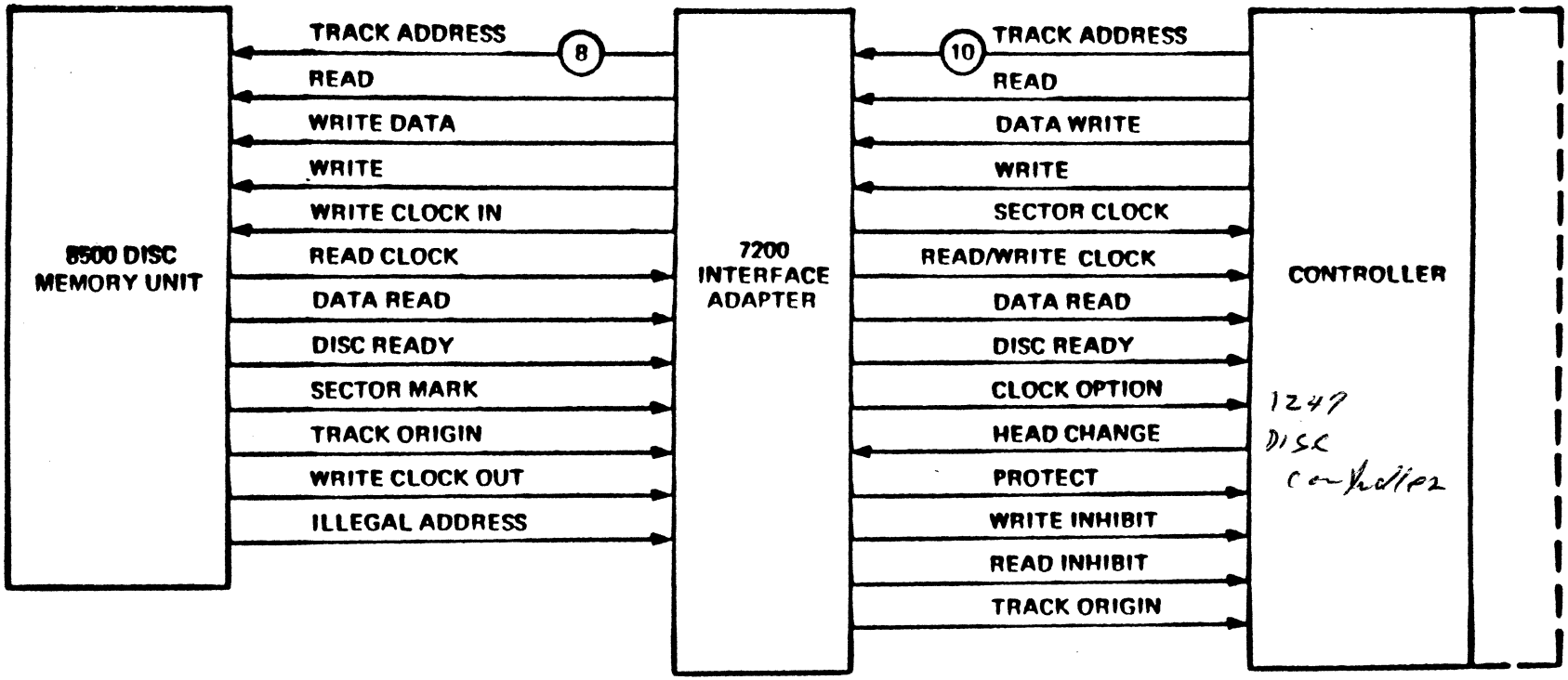


Figure 3-1. 7200 Adapter Interface Signals, Block Diagram

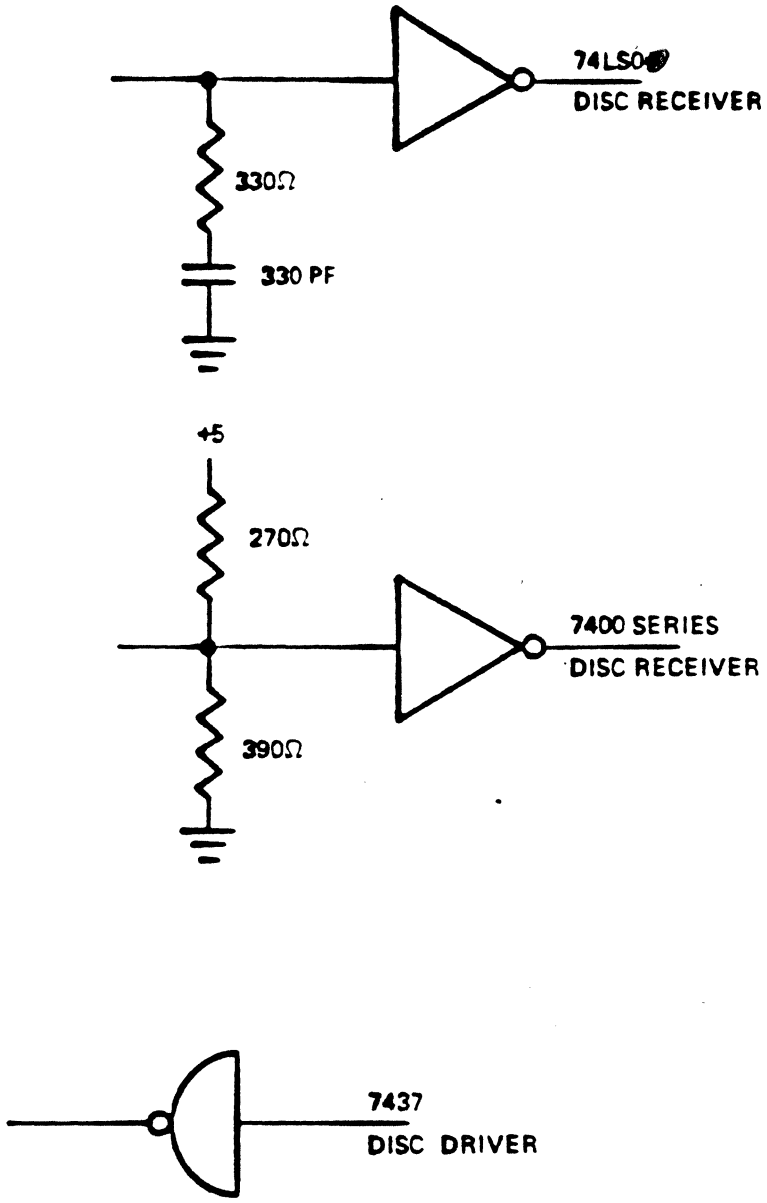


Figure 3-2. Typical Line Receiver/Driver Configuration

Chapter 4

THEORY OF OPERATION

4-1 INTRODUCTION

This chapter contains detailed circuit descriptions of the 7200 Interface Adapter Card. The theory for the circuit descriptions is taken from logic diagram 1940130. Signal definitions are listed in table 4-1.

4-2 SIGNAL MNEMONICS AND DEFINITIONS

Table 4-1 contains a complete list of signal mnemonics and definitions used for the 7200 Interface Adapter.

TABLE 4-1. SIGNAL MNEMONICS AND DEFINITIONS

MNEMONIC	DESCRIPTION	FUNCTION
-WRITE/$\overline{WR}$	WRITE COMMAND	Enables data to be recorded on disk.
-HC	HEAD CHANGE	Asserted at head select time - generates read/write inhibit.
DISC RDY/-DISK READY	DISC READY	Indicates disk is up to required speed, etc..
$\overline{WCO}$	WRITE CLOCK OUT	Pre-recorded write timing data.
$\overline{RD\ DATA}$/+READ DATA	READ DATA	Data being read from disk.
$\overline{SM}$	SECTOR MARK	Pre-recorded beginning of sector.
$\overline{TO}$/-TO	TRACK ORIGIN	Pre-recorded beginning of track.
RD CLK	READ CLOCK	Read timing data.
-READ/$\overline{RD}$	READ COMMAND	Enables data to be read from disk.
+DATA WRITE/$\overline{WR\ DATA}$	WRITE DATA	Data being written on disk.
-WRITE INH	WRITE INHIBIT	Signals to controller indicating operation.

TABLE 4-1. SIGNAL MNEMONICS AND DEFINITIONS (Continued)

MNEMONIC	DESCRIPTION	FUNCTION
-READ INH	READ INHIBIT	(Write or Read) should be delayed.
$\overline{\text{WCI}}$	WRITE CLOCK IN	Clocks in write data during write operation.
+CLK OPT	CLOCK OPTION	Optional WCO.
-SEC CLK	SECTOR CLOCK	Defines the start of a sector.
$\overline{\text{UNIT 0}}$	UNIT Ø	Indicates unit Ø is selected.
-R/W CLK	READ/WRITE CLOCK	Used by controller to generate write data and strobe read data.

4-3 DISC READY

The signal $\overline{\text{DISC RDY}}$ (figure 4-1) enters the adapter card from the disk, goes through a double inversion at U2-5 and U18-9 and leaves the adapter card as -DISC READY to the controller. When -DISC READY is low, the disk unit is ready to reliably transmit or receive data.

4-4 READ DATA

The signal $\overline{\text{RD DATA}}$ (figure 4-1) enters the adapter card from the disk, goes through an inversion at U18-13 and leaves the adapter card as +DATA READ to the controller. During a READ operation, this line provides serial NRZ data from the selected data head in synchronization with the R/W CLK.

4-5 WRITE DATA

The signal +DATA WRITE (figure 4-1) enters the adapter card from the controller, goes through an inversion at U9-13 and leaves the adapter card as $\overline{\text{WR DATA}}$ to the disk.

This line will carry serial NRZ data to be recorded on the disk by the selected data head.

4-6 READ

The signal -READ (figure 4-1) enters the adapter card from the controller, goes through a double inversion and leaves the adapter card as $\overline{\text{RD}}$ to the disc. The -READ command will be low until the last bit has been received.

4-7 -READ/WRITE CLOCK

The signal $\overline{\text{RD CLK}}$ from the disk is delayed and gated with +READ at U16 (figure 4-2) to form -R/W CLK to the controller. The delay of $\overline{\text{RD CLK}}$ can be adjusted to form the conditions R/W CLK (RETARDED) or R/W CLK (ADVANCED)

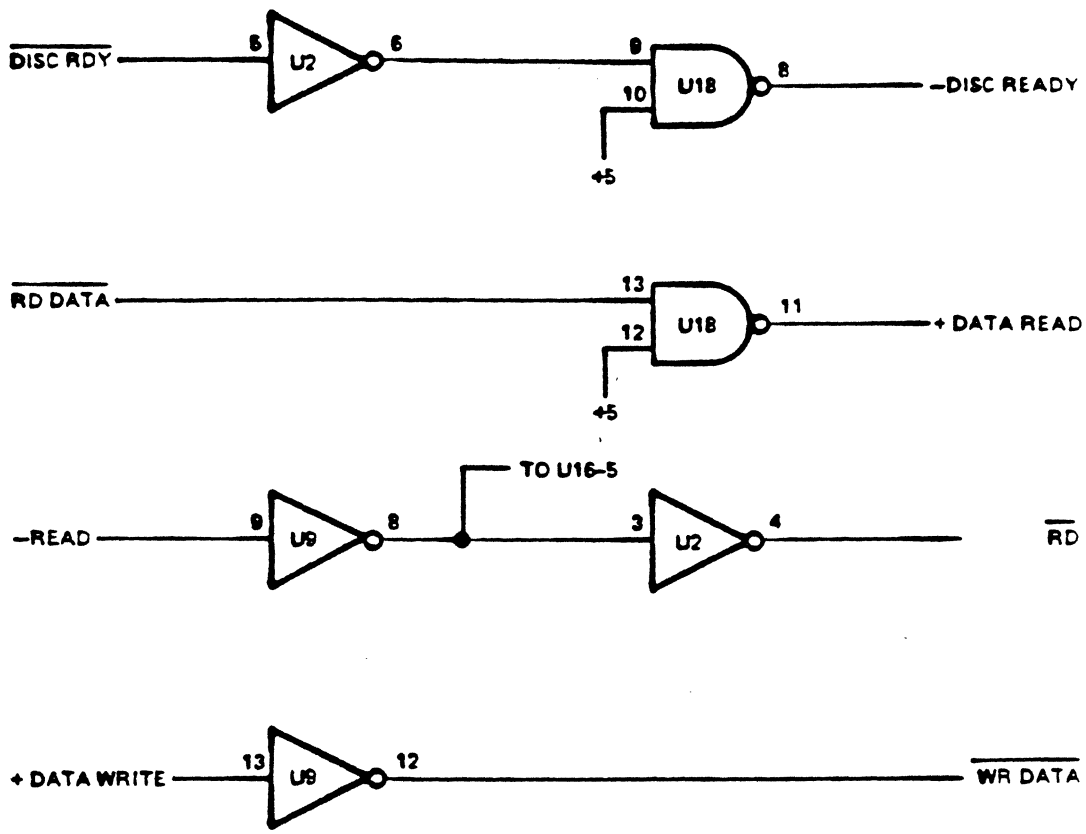


Figure 4-1. Adapter Board Partial Circuit Diagram

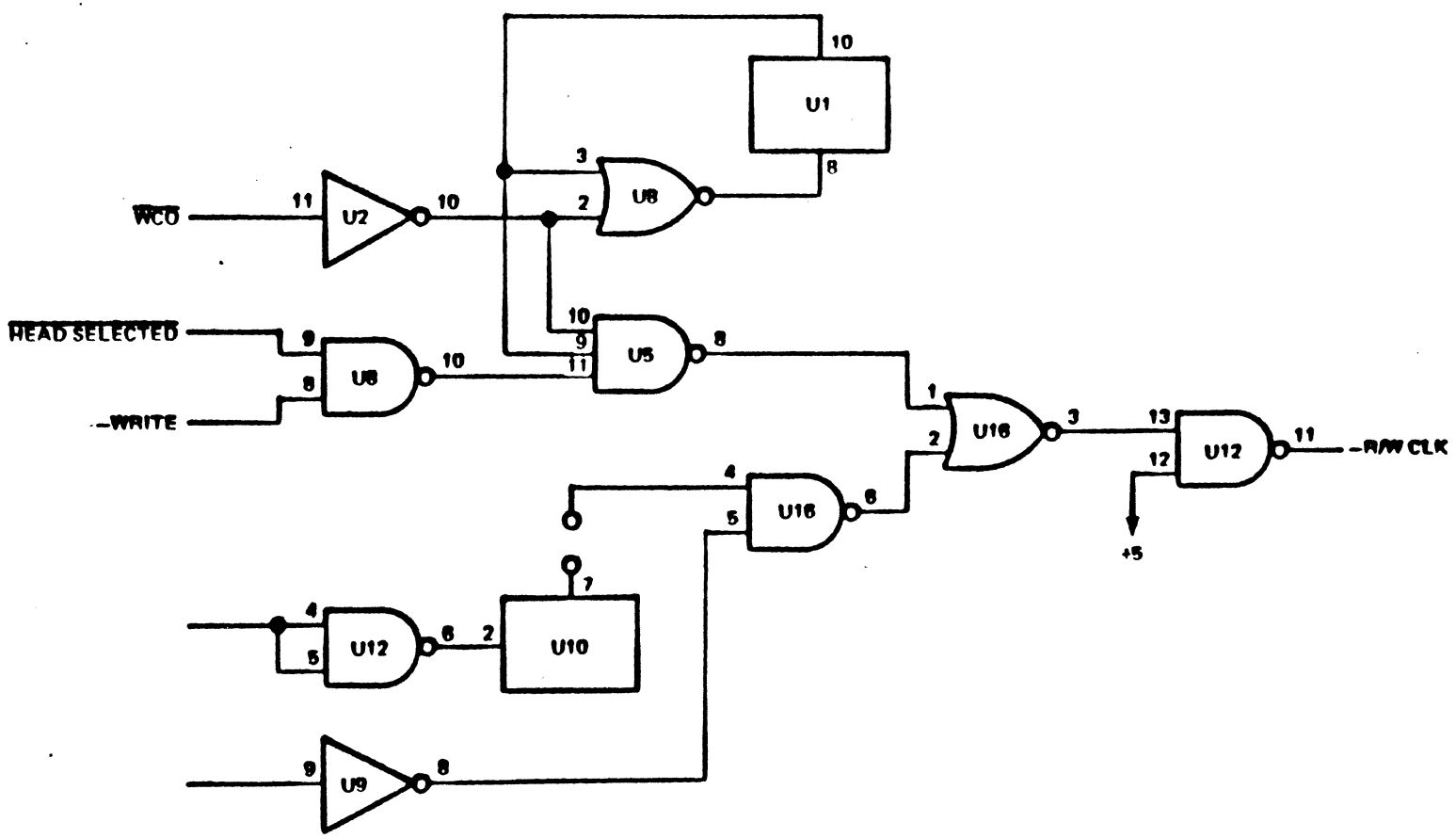


Figure 4-2. Read/Write Clock Circuits Simplified Diagram

figure 4-3). The delayed R/W CLK is applicable only during a read operation and during a read, the R/W CLK pulse indicates that valid data is present on the DATA READ line and continues until the READ signal is terminated.

During a WRITE operation (figure 4-2 and 4-4) WRITE CLOCK OUT (WCO) is gated with WRITE signal and WR signal at U5 to form the signal -/W CLOCK. The $\overline{WR}$ signal is a level delayed by U1, 5 bit times. -/W CLOCK is applied to an OR-GATE, U16-1 and is gated out to the controller as -R/W CLK. During write, the R/W CLK pulse indicates to the controller that the disk has accepted data on the DATA WRITE line and that the next bit of data should be placed on the line. The pulse is emitted only during actual data transfer until the WRITE signal is terminated.

4-8 WRITE DELAY

When +WRITE is high (figure 4-5 and 4-6), the clear signal at U1-9 is removed. WCO is gated through U8-2 to the input of U1 starting the timing sequence of U1. U1 is a shift register, therefore, after five input pulses (five bit times) the output of U1-10 goes high, U1-10 going high causes a low at U1-8 not allowing any further shifting of the shift register. When U1-10 is high, $\overline{WR}$ is low. When +WRITE goes low a clear signal is applied to U1-9, resetting the output at U1-10 to a low causing $\overline{WR}$ to go high and terminating write sequence. When $\overline{WR}$ is low, data on the DATA WRITE line will be recorded on the disk. The -WRITE signal will remain low until the last bit of data has been transmitted.

4-9 WRITE INHIBIT AND READ INHIBIT

During a head change (-HC) (figure 4-7 and 4-8) with +WRITE being low, a low is applied to the trigger input of U17-2, U17-3 goes high, U17-7/6 starts ramping high at a charge rate established by R42 and C18. With U17-3 going high, a high is applied to U18-5 and U18-2 establishing both WRITE INH and READ INH. When U17-7/6 reaches approximately 3 volts, the output at U17-3 goes low causing U18-6 and U18-3 to go high.

During a write operation, U8-4 goes low setting U17-3 high, U17-3 going high causes a low at U18-3 establishing READ INH, WRITE INH remains high. U19-8 is held low, therefore, C18 is not allowed to charge so the output at U17-3 stays high until the end of write. When write goes low, U19-8 goes high allowing C18 to charge, when the threshold is reached U17-3 goes low causing U18-3 to go high.

4-10 SECTOR CLOCK

When SECTOR MARK ($\overline{SM}$) goes low (figure 4-9 and 4-10) and WCO goes high, QD is set low and QB is set high. QD going low causes Enable P to go high allowing the counter U11 to count. At count 4 QB goes low and remains low until count 6, then going high and remaining high until count 8, then going low. At count 8, QD goes high causing Enable P to go low stopping the counter.

4-11 TRACK ORIGIN

This signal $\overline{TO}$ (figure 4-11 and 4-12) enters the adapter card from the disk and is applied to a one-shot (U3), generating an output pulse 2.25 μsec duration. This output pulse leaves the adapter card as -TO to the controller.

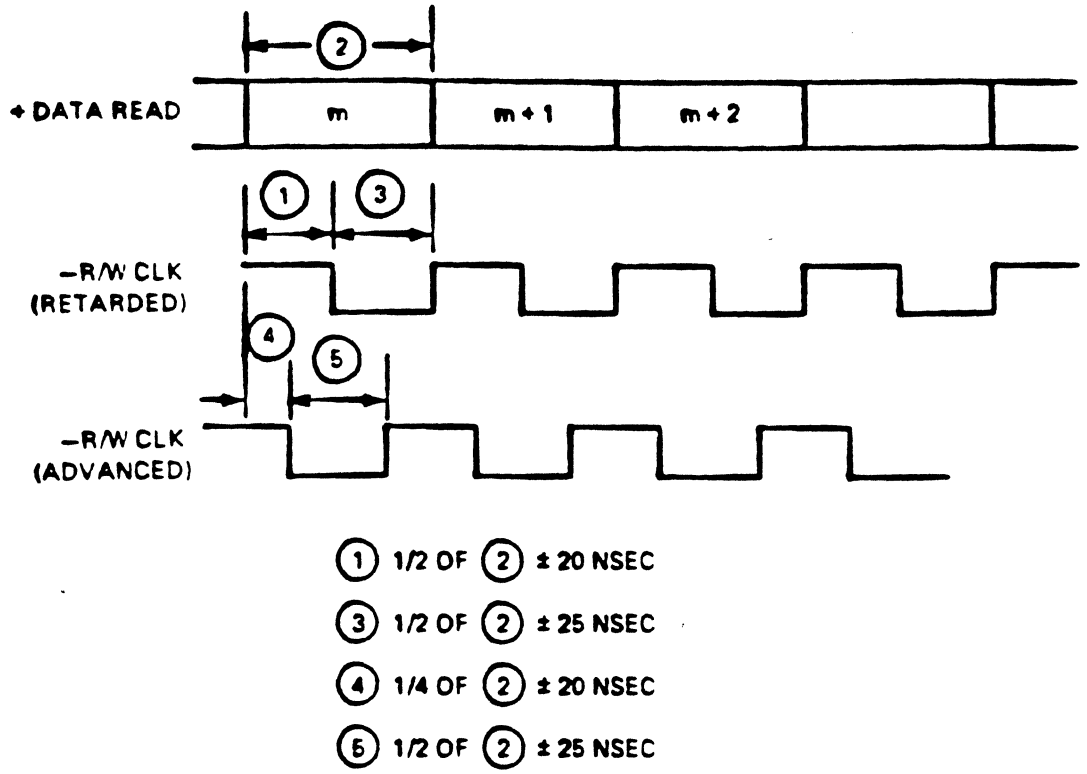


Figure 4-3. R/W Clock During Read Timing Diagram

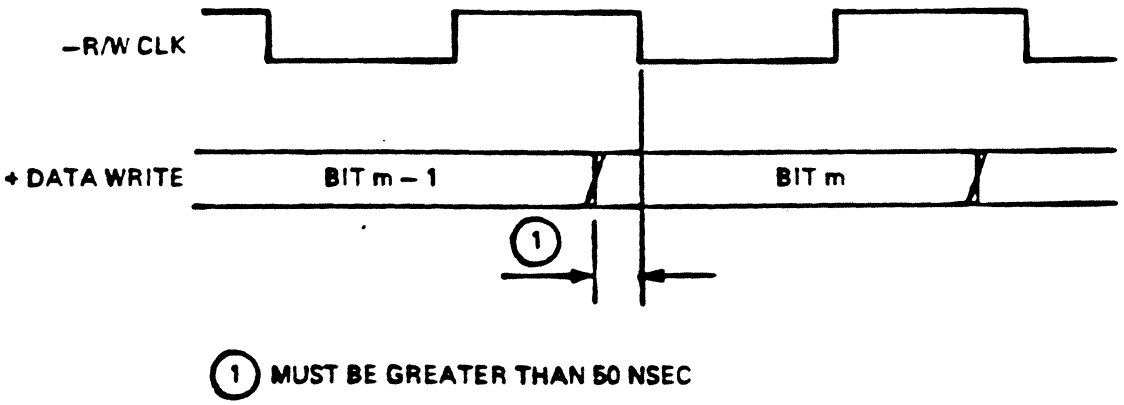


Figure 4-4. R/W Clock During Write Timing Diagram

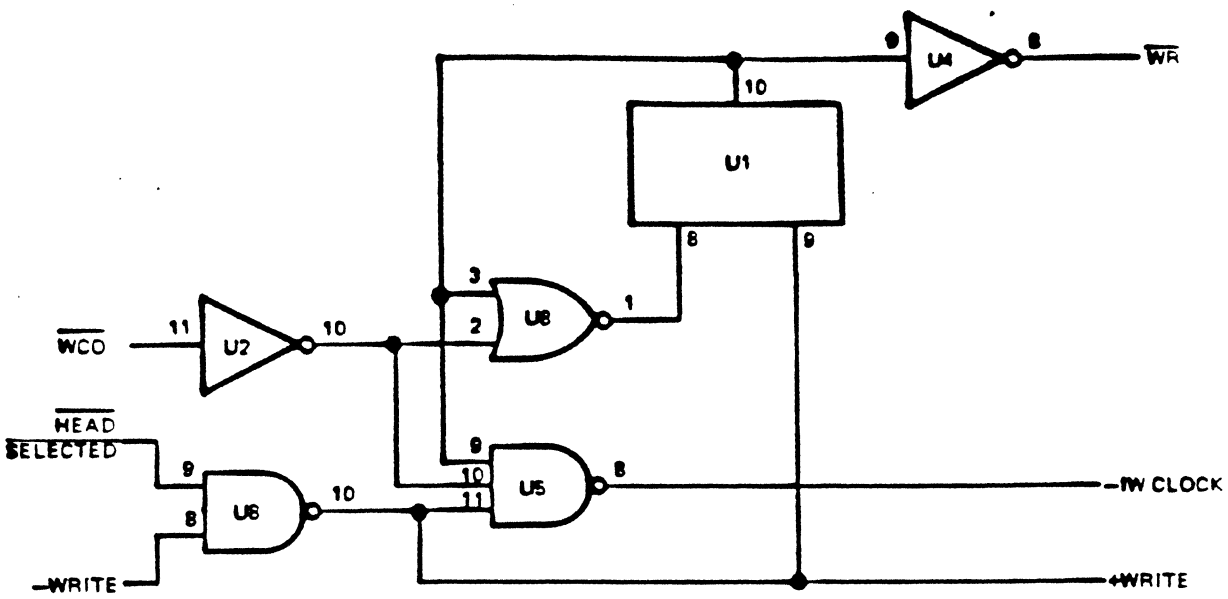


Figure 4-5. Write Delay Circuits Simplified Diagram

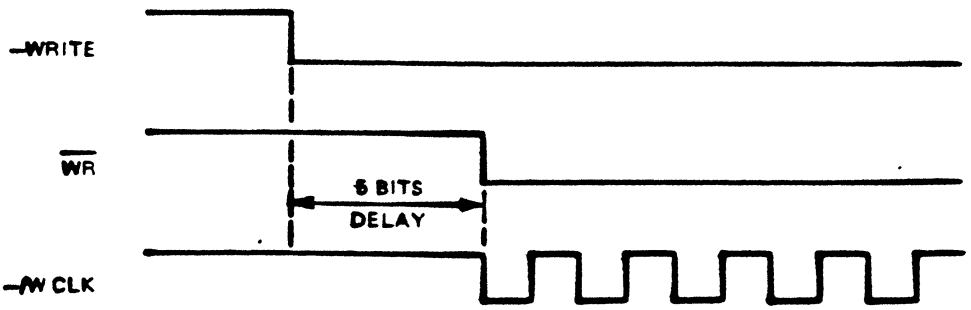


Figure 4-6. Write Delay Timing Diagram

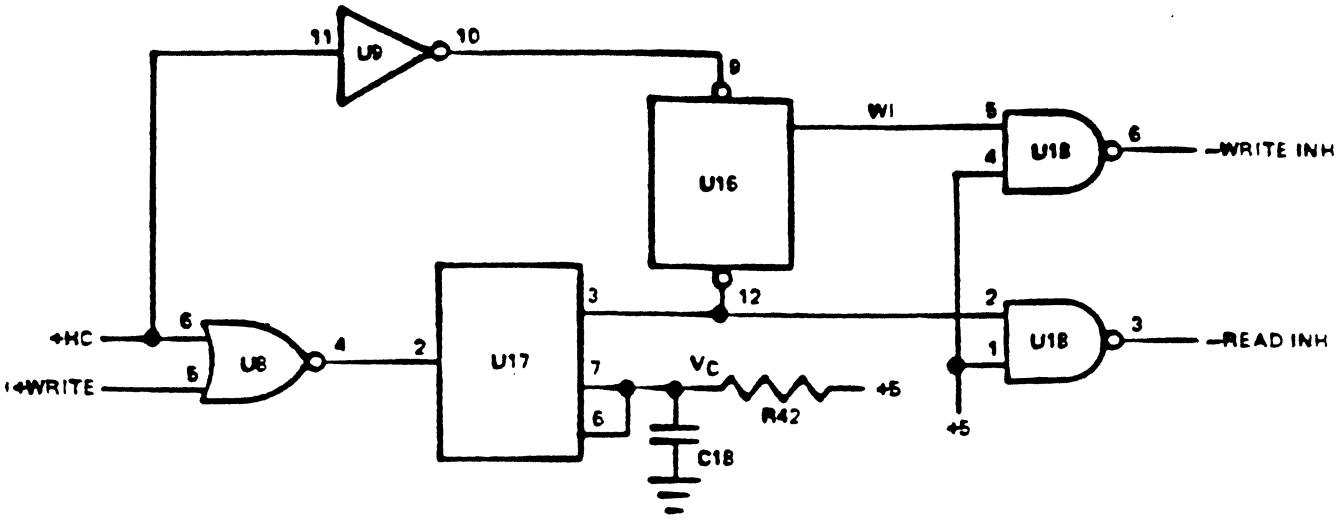


Figure 4-7. Write and Read Inhibit Circuits Simplified Diagram

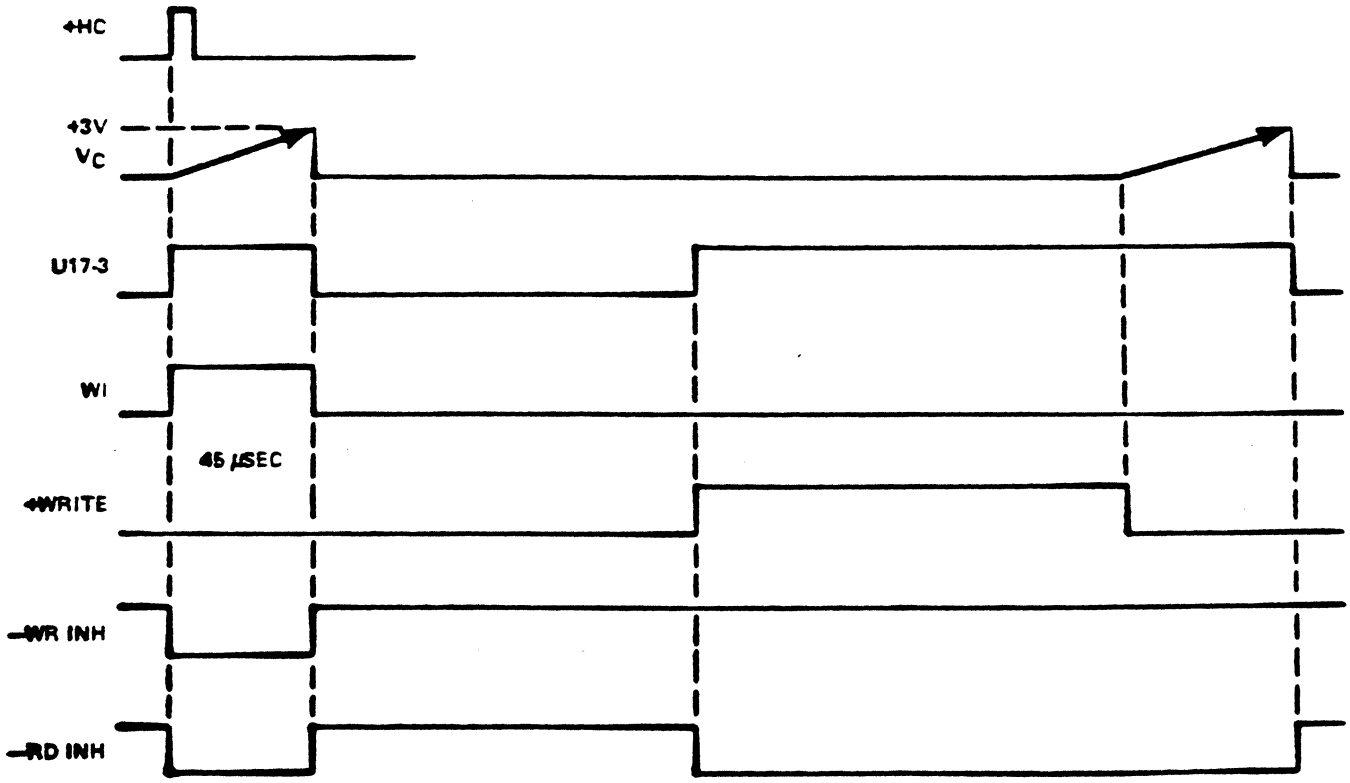


Figure 4-8. Write and Read Inhibit Timing Diagram

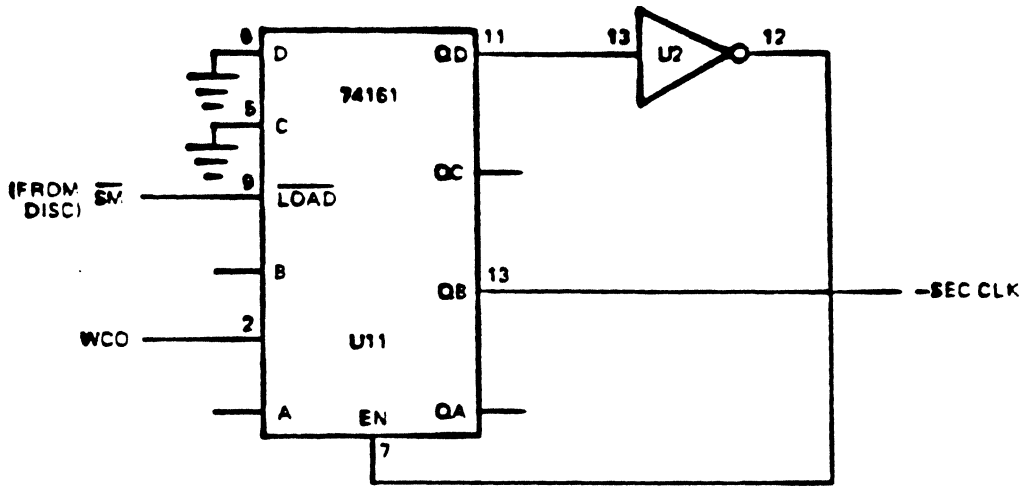


Figure 4-9. Sector Clock Circuit Simplified Diagram

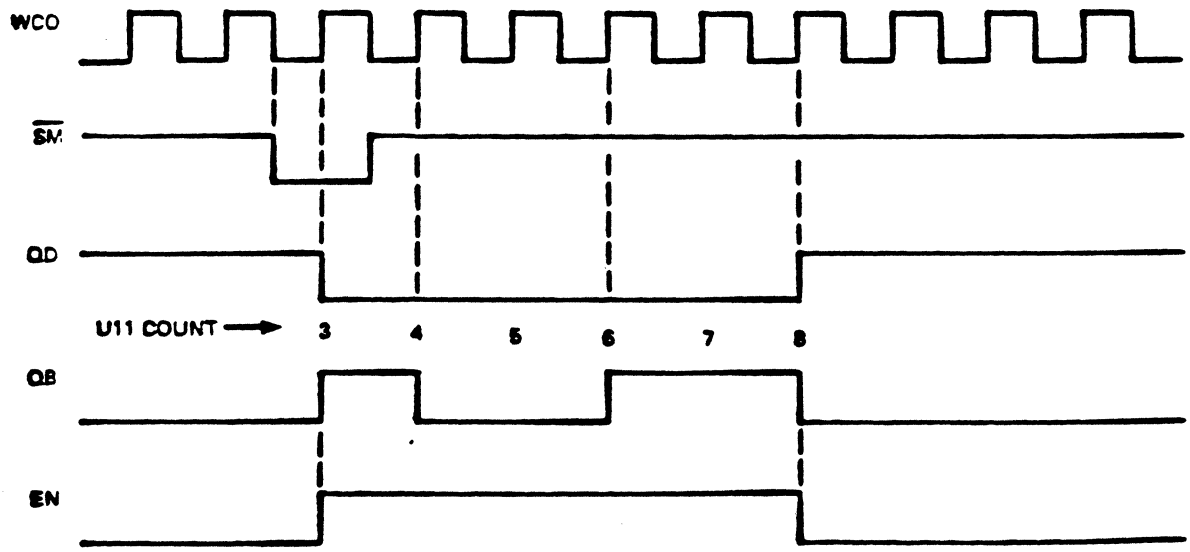


Figure 4-10. Sector Clock Timing Diagram

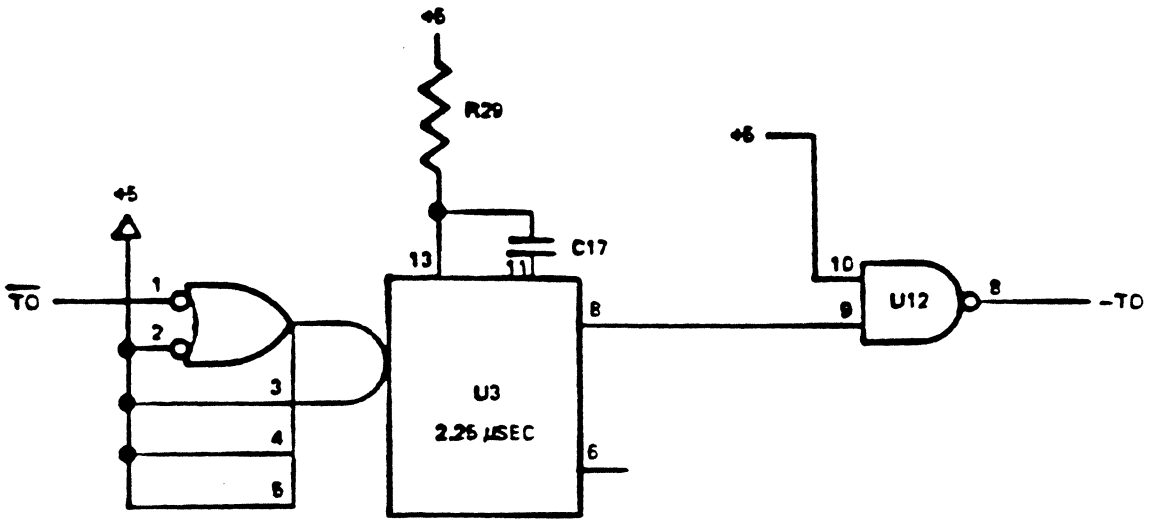


Figure 4-11. Track Origin Circuit Simplified Diagram

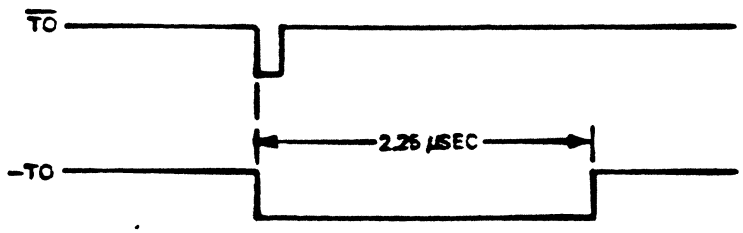


Figure 4-12. Track Origin Timing Diagram

The T0 pulse is a single pulse occurring once per revolution at a constant point on the disk.

4-12 HEAD SELECTION

The 8 line to 3 line encoder's U13 and U6 converts an X-Y-Z address to a binary address (figure 4-13). One X and one Y line being true selects a head out of a group of 64. Z0 and Z1 lines provide a binary address to select one of four groups of 64 heads that may be available.

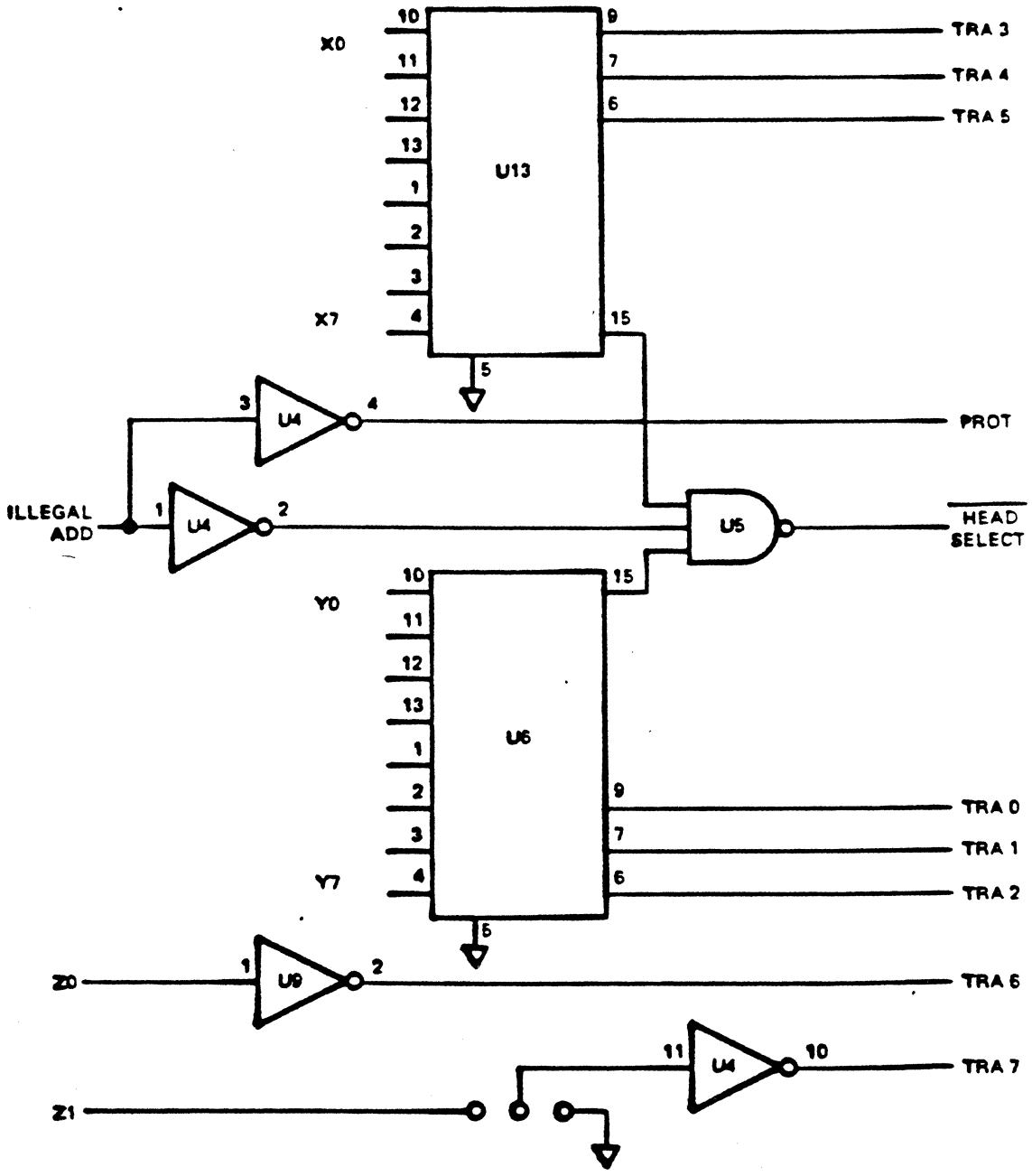


Figure 4-13. Head Selection Circuit Simplified Diagram

Chapter 5

MAINTENANCE

5-1 INTRODUCTION

The maintenance for the 7200 Interface Adapter consists of the board level. Maintenance is described in the following paragraph. Included in this chapter is troubleshooting tools.

5-2 BOARD-LEVEL TROUBLESHOOTING

The following outline is used to isolate a malfunction via board level of maintenance. The technician may have other ways of checking the equipment but the sequence described below is suggested for a quick fault isolation.

a. Verify that power is on.

b. Verify that the adapter board is plugged into equipment chassis properly.

c. Verify that cable connectors in system are connected properly.

d. Check voltage inputs from system power supply.

e. Run diagnostics to isolate the malfunction to a specific device. If equipment other than the adapter card is faulty, refer to the appropriate maintenance manual. If adapter card is malfunctioning, proceed to the next step.

f. Remove the faulty adapter card and route it for repair. Replace with a new card and run diagnostics to check it out.

5-3 TROUBLESHOOTING TOOLS

Below is a list of tools that should be available for extensive troubleshooting (fault isolation to the component level).

a. Oscilloscope - necessary for all troubleshooting except swapping of board.

b. Chip Clips - these clips are attached to chips to allow scoping of their pins.

c. Digital Volt-Ohmmeter - required for checking power supplies, voltages, resistances and continuity. (A scope may be used in most cases, if preferred.)

d. Standard field service tool kit.

5-4 CLOCK AND SECTOR WRITING

The writing of clocks and sectors requires the use of 8500 Disc Test Unit. The 7200 Adapter Card must be removed and the simulator connected to the disc unit. Refer to the 8500 Series Disc Memory Unit Operation and Maintenance Manual for clock and sector writing procedure.

Chapter 6

DRAWINGS AND PARTS LISTS

6-1 INTRODUCTION

This chapter contains a schematic and assembly drawing list, a replaceable parts list and drawings required to work with and maintain the 7200 Interface Adapter Card.

6-2 SCHEMATIC AND ASSEMBLY DRAWINGS

Table 6-1 lists the adapter card drawings included in this chapter.

TABLE 6-1. 7200 INTERFACE ADAPTER DRAWINGS

DRAWING NUMBER	TITLE
1940130	Schematic/Logic Diagram
1040130	Adapter PC Board Assembly

6-3 REPLACEABLE PARTS LIST

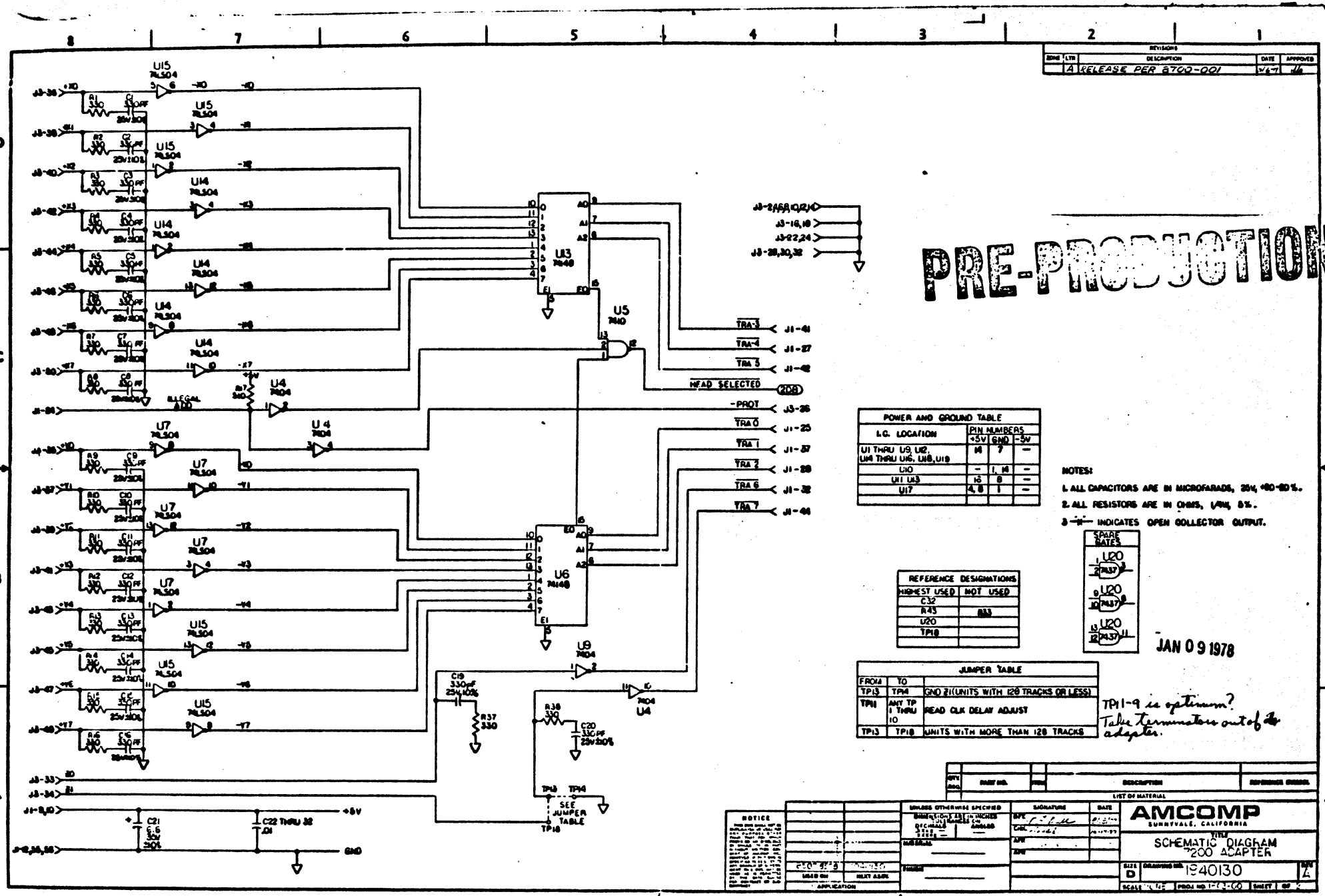
Replaceable parts are listed in Table 6-2. This table includes the AMCOMP part number of each part listed, the part description and location on the adapter board.

TABLE 6-2. 7200 INTERFACE ADAPTER REPLACEABLE PARTS

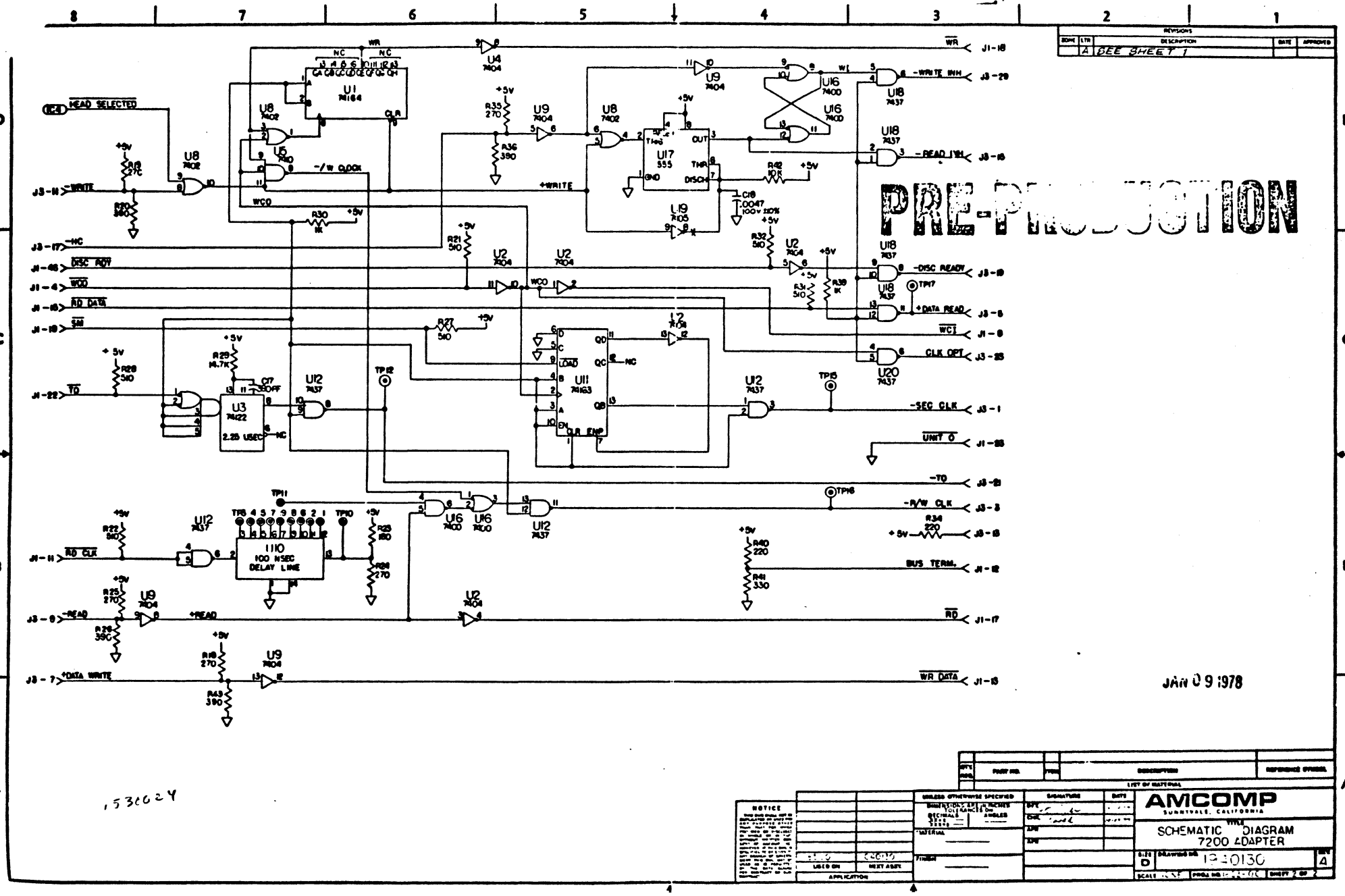
PART NUMBER	DESCRIPTION/LOCATION	QUANTITY
	Capacitors	
01200103-23	Tantalum, 6.8µf, 35V, 10%/C21	1
01400108-07	Ceramic, .0047µf, 100V, 10%/C18	1
01416103-01	Ceramic, 01µf, 25V, $^{+80\%}_{-20\%}$/C22 thru C32	11
01383331-01	Mica, 330pf/C1 thru C16, C19, C20	18
01383391-01	Mica, 390pf/C17	1

TABLE 6-2. 7200 INTERFACE ADAPTER REPLACEABLE PARTS (Continued)

PART NUMBER	DESCRIPTION/LOCATION	QUANTITY
	Resistors	
04122102-01	FXD Comp., 1K ohms, 1/4W, 5%/R30, R39	2
04122103-01	FXD Comp., 10K ohms, 1/4W, 5%/R42	1
04122181-01	FXD Comp., 180 ohms, 1/4W, 5%/R23	1
04122221-01	FXD Comp., 220 ohms, 1/4W, 5%/R40, R34	2
04122271-01	FXD Comp., 270 ohms, 1/4W, 5%/R18, R19, R24, R25, R35	5
04122331-01	FXD Comp., 330 ohms, 1/4W, 5%/R1 thru R16, R37, R38, R41	19
04122391-01	FXD Comp., 390 ohms, 1/4W, 5%/R20, R26, R36, R43	4
04122511-01	FXD Comp., 510 ohms, 1/4W, 5%/R17, R21, R22, R27, R28, R31, R32	7
04122153-01	FXD Comp., 15K ohms, 1/4W, 5%/R29	1
	Integrated Circuits	
03000120-01	NE 555/U17	1
03200218-01	74163N/U11	1
03200257-01	74LS04N/U7, U14, U15	3
03200284-01	74148N/U6, U13	2
03201109-01	7410J/U5	1
03201118-01	7437J/U12, U18, U20	3
03204122-01	74122N/U3	1
03204164-01	74164N/U1	1
03207400-01	7400/U16	1
03207402-01	7402/U8	1
03207404-01	7404/U2, U4, U9	3
03207405-01	7405/U19	1
55000104-01	Delay Line, 100 nsec, 100 ohm/U10	1

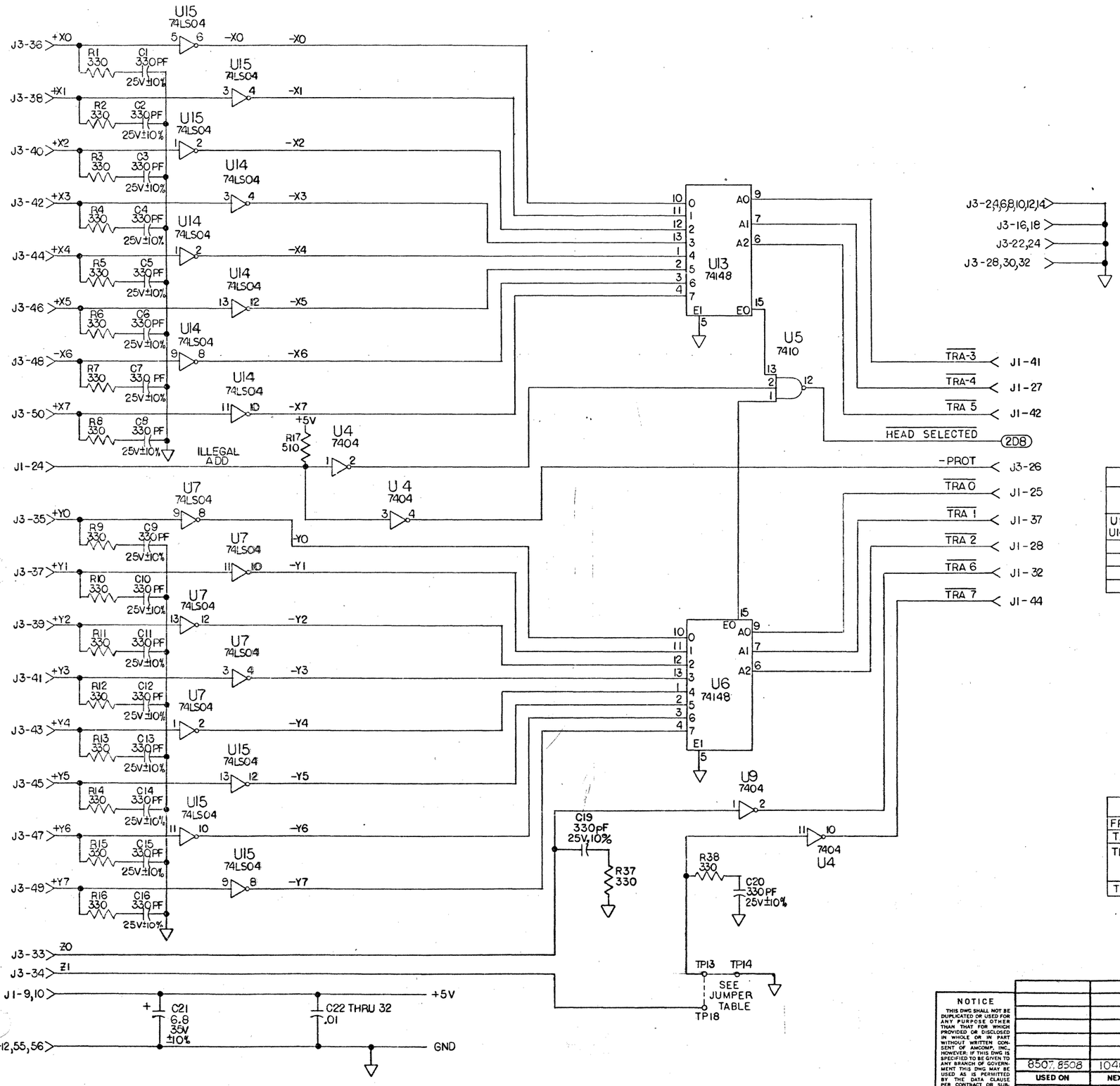


7200 ADAPTER



REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
A SEE SHEET 1
PRE-PRODUCTION
HEAD SELECTED
-WRITE
-HC
DISC RDY
WCO
RD DATA
SM
TO
RD CLK
-READ
+DATA WRITE
-/W CLOCK
+WRITE
WR
-WRITE INH
-READ INH
-DISC READY
+DATA READ
WCI
CLK OPT
-SEC CLK
UNIT 0
-TO
-R/W CLK
BUS TERM.
RD
WR DATA
U1 74164
U3 74122
2.25 USEC
U11 74163
U17 555
U16 7400
U18 7437
U20 7437
U12 7437
U2 7404
U9 7404
U8 7402
U5 7410
U4 7404
U19 7405
U20 7437
1110 100 NSEC DELAY LINE
TP11
TP10
TP12
TP15
TP16
TP17
C18 .0047 100V ±10%
C17 390FF
+5V
JAN 09 1978
1530024
LIST OF MATERIAL
NOTICE
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON
DECIMALS
ANGLES
MATERIAL
FINISH
SIGNATURE
DATE
USED ON
NEXT ASSY
APPLICATION
AMCOMP
SUNNYVALE, CALIFORNIA
TITLE
SCHEMATIC DIAGRAM
7200 ADAPTER
SIZE D
DRAWING NO. 1940130
REV A
SCALE
SHEET 2 OF 2

REVISIONS				
ZONE	LTR.	DESCRIPTION	DATE	APPROVED
	A	RELEASE PER 3700-001	7/6/77	WG
	B	REVISED PER E.O. 53174	9/9/76	



POWER AND GROUND TABLE			
I.C. LOCATION	PIN NUMBERS +5V	GND	-5V
U1 THRU U9, U12, U14 THRU U16, U18, U19	14	7	—
U10	—	1, 14	—
U11 U13	16	8	—
U17	4, 8	1	—

NOTES:

1. ALL CAPACITORS ARE IN MICROFARADS, 25V, +80-20%.
2. ALL RESISTORS ARE IN OHMS, 1/4W, 5%.
3. ~~"X"~~ INDICATES OPEN COLLECTOR OUTPUT.

REFERENCE DESIGNATIONS	
HIGHEST USED	NOT USED
C32	
R43	R33
U20	
TP18	

SPARE GATES
U20 (7437) 1, 2, 3
U20 (7437) 9, 10, 8
U20 (7437) 13, 12, 11

JUMPER TABLE		
FROM	TO	
TP13	TP14	GND ZI (UNITS WITH 128 TRACKS OR LESS)
TP11	ANY TP 1 THRU 10	READ CLK DELAY ADJUST
TP13	TP18	UNITS WITH MORE THAN 128 TRACKS

QTY. REQ.	PART NO.	ITEM	DESCRIPTION	REFERENCE SYMBOL

LIST OF MATERIAL

NOTICE
THIS DWG SHALL NOT BE DUPLICATED OR USED FOR ANY PURPOSE OTHER THAN THAT FOR WHICH PROVIDED OR DISCLOSED IN WHOLE OR IN PART WITHOUT WRITTEN CONSENT OF AMCOMP, INC., HOWEVER, IF THIS DWG IS SPECIFIED TO BE GIVEN TO ANY BRANCH OF GOVERNMENT THIS DWG MAY BE USED AS IS PERMITTED BY THE DATA CLAUSE PER CONTRACT OR SUBCONTRACT.

USED ON	NEXT ASSY.
8507,8508	1040130

APPLICATION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON DECIMALS .XX± .XXX± ANGLES —
MATERIAL —
FINISH —

SIGNATURE	DATE
DFT.	8/18/77
CHK.	10-17-77
APR.	12-5-77
ATE	

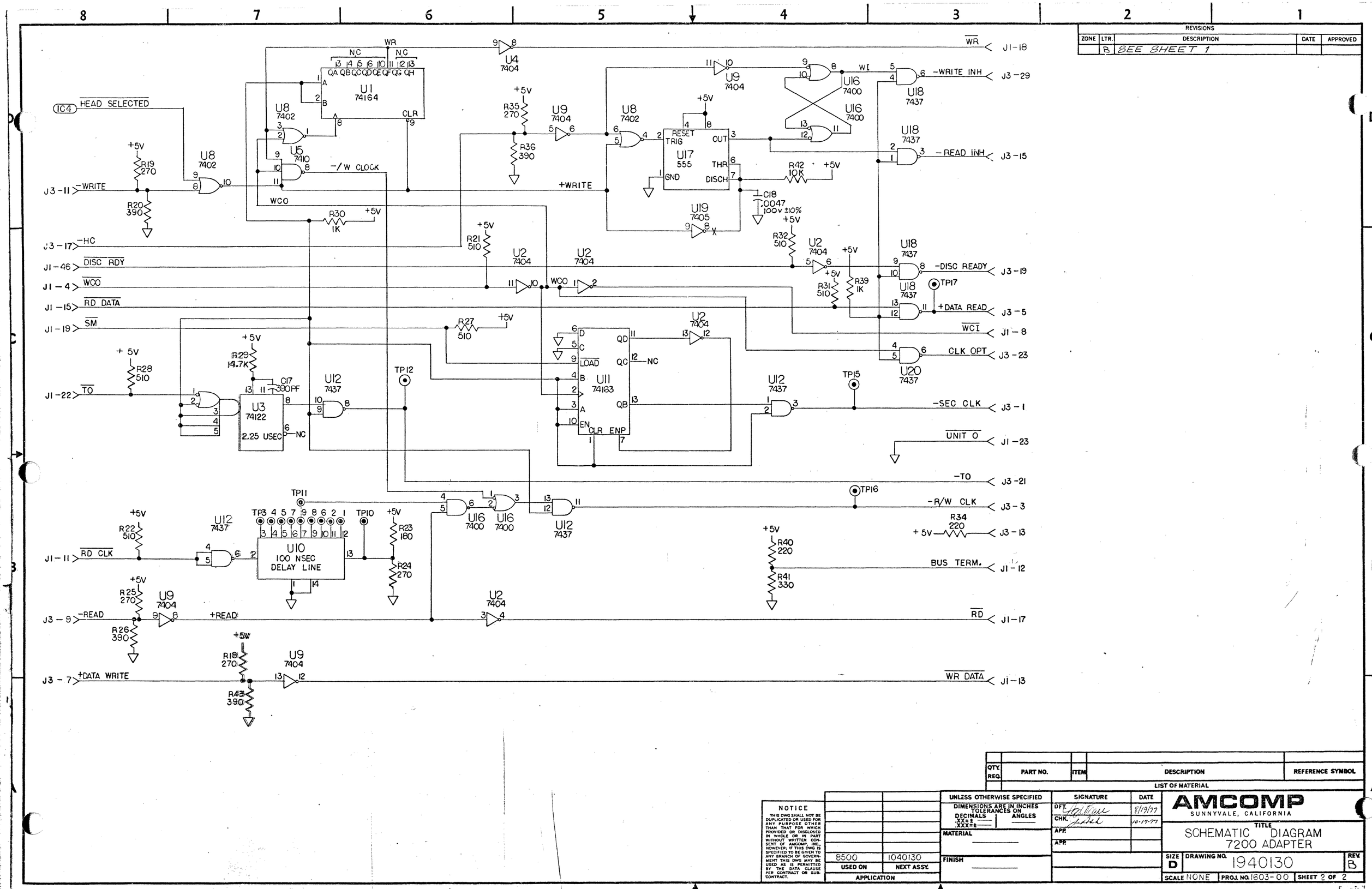
AMCOMP
SUNNYVALE, CALIFORNIA

TITLE
SCHEMATIC DIAGRAM
7200 ADAPTER

SIZE	DRAWING NO.	REV.
D	1940130	B

SCALE NONE | PROJ. NO. 1603-00 | SHEET 1 OF 2

6-5/6



QTY. REQ.	PART NO.	ITEM	DESCRIPTION	REFERENCE SYMBOL

LIST OF MATERIAL

NOTICE

THIS DWG SHALL NOT BE DUPLICATED OR USED FOR ANY PURPOSE OTHER THAN THAT FOR WHICH PROVIDED OR DISCLOSED IN WHOLE OR IN PART WITHOUT WRITTEN CONSENT OF AMCOMP, INC., HOWEVER; IF THIS DWG IS SPECIFIED TO BE GIVEN TO ANY BRANCH OF GOVERNMENT THIS DWG MAY BE USED AS IS PERMITTED BY THE DATA CLAUSE PER CONTRACT OR SUBCONTRACT.

USED ON	NEXT ASSY.
8500	1040130

APPLICATION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON
DECIMALS .XX=± .XXX=±
ANGLES
MATERIAL
FINISH

SIGNATURE	DATE
DFT. [signature]	8/19/77
CHK. [signature]	10-17-77
APP.	
APP.	

AMCOMP
SUNNYVALE, CALIFORNIA

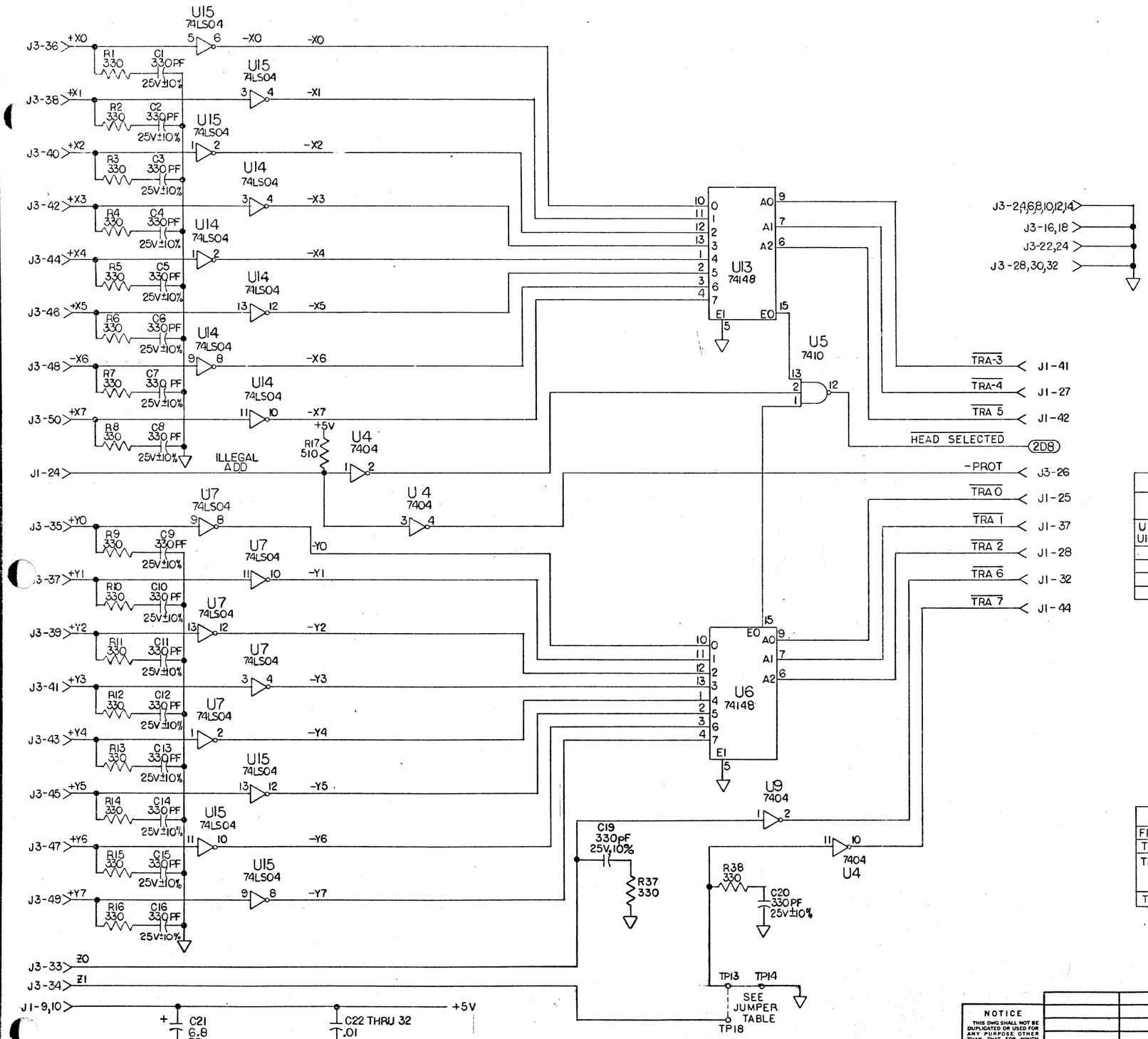
TITLE
SCHEMATIC DIAGRAM
7200 ADAPTER

SIZE D | DRAWING NO. 1940130 | REV. B

SCALE NONE | PROJ. NO. 1603-00 | SHEET 2 OF 2

6-7/8

REVISIONS				
ZONE	LTR.	DESCRIPTION	DATE	APPROVED
	A	RELEASE PER 8700-001	7/6/77	JLO
	B	REVISED PER E.O. 53174	9/9/77	[illegible]



POWER AND GROUND TABLE			
I.C. LOCATION	PIN NUMBERS +5V	GND	-5V
U1 THRU U9, U12, U14 THRU U16, U18, U19	14	7	—
U10	—	1, 14	—
U11 U13	16	8	—
U17	4, 8	1	—

NOTES:

1. ALL CAPACITORS ARE IN MICROFARADS, 25V, +80-20%.
2. ALL RESISTORS ARE IN OHMS, 1/4W, 5%.
3. "X" INDICATES OPEN COLLECTOR OUTPUT.

REFERENCE DESIGNATIONS	
HIGHEST USED	NOT USED
C32	
R43	R33
U20	
TP18	

SPARE GATES
U20 1 2 7437 3
U20 9 10 7437 8
U20 13 12 7437 11

JUMPER TABLE		
FROM	TO	
TP13	TP14	GND Z1(UNITS WITH 128 TRACKS OR LESS)
TP11	ANY TP 1 THRU 10	READ CLK DELAY ADJUST
TP13	TP18	UNITS WITH MORE THAN 128 TRACKS

QTY REQ.	PART NO.	ITEM	DESCRIPTION	REFERENCE SYMBOL

LIST OF MATERIAL

NOTICE
THIS DWG SHALL NOT BE DUPLICATED OR USED FOR ANY PURPOSE OTHER THAN THAT FOR WHICH PROVIDED OR DISCLOSED IN WHOLE OR IN PART WITHOUT WRITTEN CONSENT OF AMCOMP, INC. HOWEVER, IF THIS DWG IS SPECIFIED TO BE GIVEN TO ANY BRANCH OF GOVERNMENT THIS DWG MAY BE USED AS IS PERMITTED BY THE DATA CLAUSE PER CONTRACT OR SUB-CONTRACT.

USED ON	NEXT ASSY.
8507 8508	1040130

APPLICATION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON DECIMALS XXX± — XXX± — ANGLES —
MATERIAL
FINISH

SIGNATURE	DATE
DFT. [illegible]	8/18/77
CHK. [illegible]	10-17-77
APP. [illegible]	12-5-77
APP.	

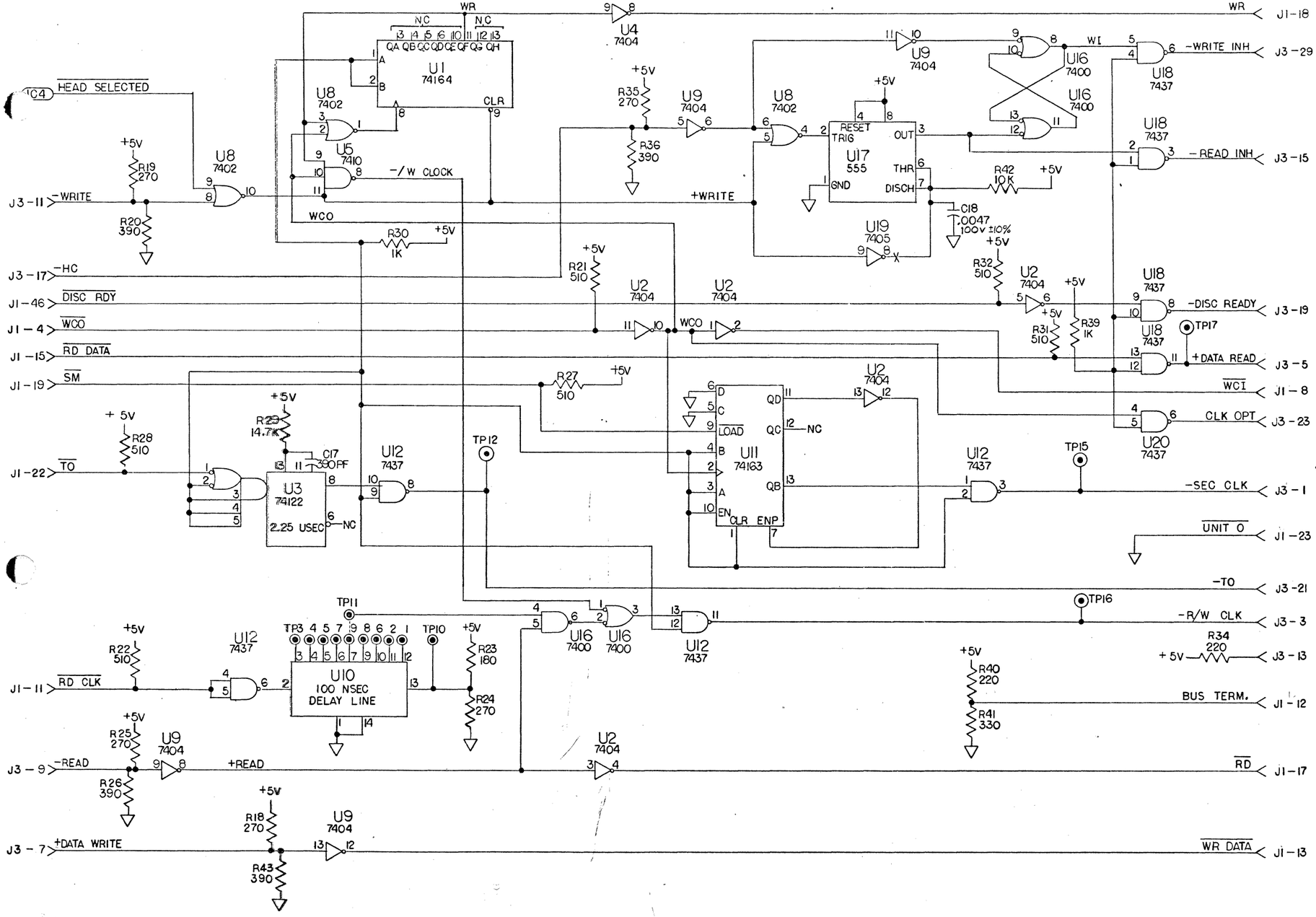
AMCOMP
SUNNYVALE, CALIFORNIA

TITLE
SCHEMATIC DIAGRAM
7200 ADAPTER

SIZE D | DRAWING NO. 1040130 | REV. B
SCALE NONE | PROJ. NO. 1603-00 | SHEET 1 OF 2

6-5/6

REVISIONS				
ZONE	LTR.	DESCRIPTION	DATE	APPROVED
	B	SEE SHEET 1		



QTY. REQ.	PART NO.	ITEM	DESCRIPTION	REFERENCE SYMBOL

LIST OF MATERIAL

NOTICE
THIS DWG SHALL NOT BE DUPLICATED OR USED FOR ANY PURPOSE OTHER THAN THAT FOR WHICH PROVIDED OR DISCLOSED IN WHOLE OR IN PART WITHOUT WRITTEN CONSENT OF AMCOMP, INC., HOWEVER, IF THIS DWG IS SPECIFIED TO BE GIVEN TO ANY BRANCH OF GOVERNMENT THIS DWG MAY BE USED AS IS PERMITTED BY THE DATA CLAUSE PER CONTRACT OR SUBCONTRACT.

8500	1040130
USED ON	NEXT ASSY.

APPLICATION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON DECIMALS XX=± XXX=± ANGLES
MATERIAL
FINISH

SIGNATURE	DATE
DFT.	8/19/77
CHK.	10-19-77
APP.	
APP.	

AMCOMP
SUNNYVALE, CALIFORNIA

TITLE
SCHEMATIC DIAGRAM
7200 ADAPTER

SIZE	DRAWING NO.	REV.
D	1940130	B

SCALE NONE | PROJ. NO. 1603-00 | SHEET 2 OF 2

6-7/8