TECHNICAL MANUAL

AM-720
MEMORY BOARDS

DWM-00720-00

REV. A00

alpha micro

ALPHA MICRO SYSTEMS
17881 Sky Park North
Irvine, Ca. 92714

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1.0 INTRODUCTION.

This manual provides operating and maintenance instructions for the AM-720 memory circuit board manufactured by Alpha Microsystems Inc., located in Irvine, California. Circuit board description, operating and usage instructions, programming, theory of operation, and maintenance instructions are included to provide the user with the information necessary to use this cirucit board to its full capability.

1.1 CIRCUIT BOARD DESCRIPTION.

The AM-720 memory circuit board is a 256k x 18 bit dynamic MOS read/write memory. Memory boards can be addressed up to 16 megabytes with extended addressing (A0 thru A23). Interface is provided for the AM-720 to operate through an optional Error Checking/Correction (ECC) board via a 26-pin connector on the top of the board. Refresh for the dynamic memory is located on the board and byte parity checking and generation are provided.

A simplified block diagram of the circuit board is shown in Figure 1-1. For a complete detailed description of circuit board operation, see Section IV of this manual. For programming requirements, see Section III of this manual.

1.2 APPLICATION.

The AM-720 performs read/write (word and byte) bus cycles according to S-100 Bus protocol and is compatible with all Alpha Micro products.

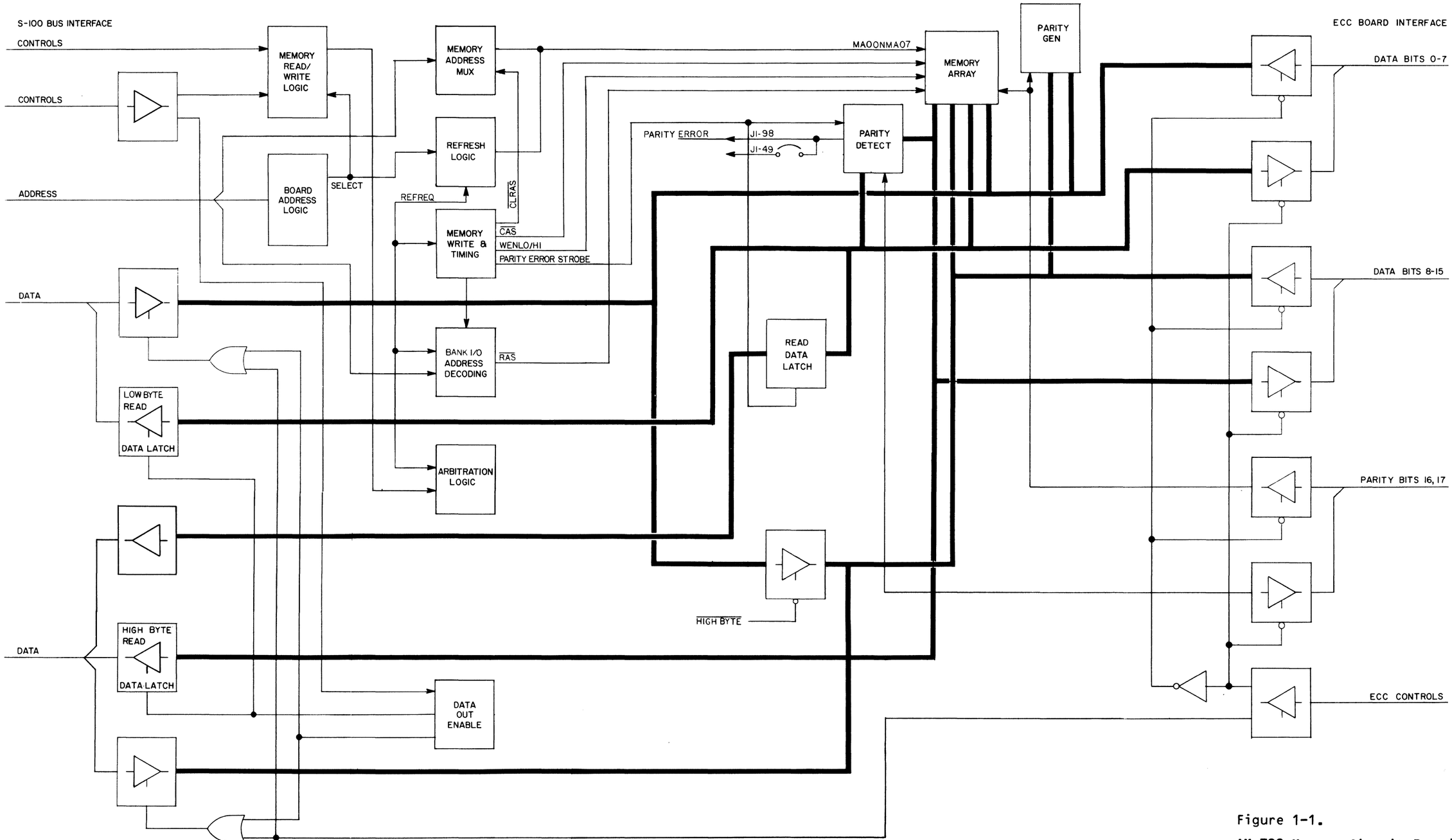


Figure 1-1.
AM-720 Memory Circuit Board
Simplified Block Diagram

2.0 INTRODUCTION.

This section contains information on the use of the AM-720 memory circuit board. Capabilities, specifications, interface wiring, and user option descriptions are provided for the successful integration of the AM-720 into the user's system.

2.1 CAPABILITIES AND SPECIFICATIONS.

This circuit board operates from the standard S-100 Bus structure either directly or through an optional Error Checking/Correction (ECC) circuit board. One AM-720 board provides 256k x 18 bit memory capability with on-board byte parity generator/detector. The AM-720 operates in a system with extended addressing capability (address bits A0-A23) NOTE: Bank I/O with standard addressing is also provided, but is not practical to use. Detailed specifications are contained in Table 2-1.

Table 2-1. AM-720 Specifications.

PARAMETER	SPECIFICATION
CPU Type	AM-100/T (use with AM-700 memory partition controller) and AM-100/L
Data Transfer	Directly to S-100 Bus or through optional Error Checking Correction (ECC) board.
Memory	256k x 16 bit dynamic MOS read/write. Memory contents are volatile.
Refresh	On-board circuitry.
Addressing	16 megabytes with extended addressing (A0-A23)
Read/Write	Read/write bus cycles according to S-100 Bus protocol.
Parity	Onboard byte parity generator/detector.
Circuit Board	10" x 9" with 100 pin connector to S-100 Bus and 26 pin connector to optional ECC board.
Environment Temperature Humidity	 0°C to 55°C 10% to 80% (non-condensing)
Power Requirements	+16V +7.5V -16V ACTIVE - 2.3A - STANDBY - 1.4A -
Data Access Time	From PSYNC : 185
Memory Cycle Time	320 ns

2.2 INTERFACE DESCRIPTION AND WIRING.

The AM-720 memory circuit board is fully S-100 Bus compatible. Data may be transferred to/from memory directly from the S-100 Bus via the bottom edge connector or via an optional Error Checking Correction (ECC) board via the top edge connector.

2.2.1 S-100 Bus Interface.

The AM-720 circuit board is compatible with the S-100 Bus with extended addressing (A0-A23). Data is transferred through the data in and data out lines with either the 8-bit configuration or 16-bit configuration. See paragraph 2.3 for selection of the various user options.

The bus connections are made via the bottom edge connector and are listed in Table 2-2. See Section IV for complete descriptions of all interface signals.

2.2.2 ECC Board Interface.

An interface to the optional ECC board is made via the top edge connector. With the ECC board, memory data transfers are through the ECC board instead of through the S-100 Bus. ECC board wiring is listed in Table 2-3. See paragraph 2.3 for jumper requirements for interface selection and Section IV for complete descriptions of all interface signals.

Table 2-2. Alpha Micro Bus Interface Signals List

MNEMONIC	NAME	PIN NO.
+7.5V	+ 7.5vdc Power	1
+16V	+ 16vdc Power	2
$\overline{VI8}$	Vectored Interrupt 8	3
$\overline{VI0}$	Vectored Interrupt 0	4
$\overline{VI1}$	Vectored Interrupt 1	5
$\overline{VI2}$	Vectored Interrupt 2	6
$\overline{VI3}$	Vectored Interrupt 3	7
$\overline{VI4}$	Vectored Interrupt 4	8
$\overline{VI5}$	Vectored Interrupt 5	9
$\overline{VI6}$	Vectored Interrupt 6	10
$\overline{VI7}$	Vectored Interrupt 7	11
RTC	Real Time Clock, 50Hz or 60Hz	12
POWFAIL	AC Power Failure Status	13
$\overline{VI9}$	Vectored Interrupt 9	14
A18	Address 18	15
A16	Address 16	16
A17	Address 17	17
$\overline{STATDSB}$	Status Disable	18
$\overline{C/CDSB}$	Command/Control Disable	19
GND	Ground	20

Table 2-2.(con't) Alpha Micro Bus Interface Signals List

MNEMONIC	NAME	PIN NO.
$\overline{\text{IODIS}}$	I/O Disable	21
$\overline{\text{ADDDSB}}$	Address Disable	22
$\overline{\text{DODSB}}$	Data Bus Disable	23
Ø2	Phase 2 Clock	24
$\overline{\text{STVAL}}$	Status and Address Valid	25
PHLDA	DMA Request Acknowledge	26
PWAIT	Processor Wait	27
N/U	Not Used	28
A5	Address 5	29
A4	Address 4	30
A3	Address 3	31
A15	Address 15	32
A12	Address 12	33
A9	Address 9	34
DOUT 1/D1	Data Bus Bit 1	35
DOUT 0/D0	Data Bus Bit 0	36
A10	Address 10	37

Table 2-2.(con't) Alpha Micro Bus Interface Signals List

MNEMONIC	NAME	PIN NO.
DOUT 4/D4	Data Bus Bit 4	38
DOUT 5/D5	Data Bus Bit 5	39
DOUT 6/D6	Data Bus Bit 6	40
DIN 2/D10	DATA BUS BIT 10	41
DIN 3/D11	Data Bus Bit 11	42
DIN 7/D15	Data Bus Bit 15	43
SMI	Bus Master OP Code Fetch	44
SOUT	I/O Output Cycle	45
SINP	I/O Input Cycle	46
SMEMR	Memory Read Cycle	47
SHLTA	HLT Acknowledge	48
$\overline{\text{PERR}}$	Parity Error Pulse	49
GND	Ground	50
+7.5V	+7.5vdc Power	51
-16V	-16vdc Power	52
GND	Ground	53
$\overline{\text{SLAVECLR}}$	Reset Signal To All I/O Devices	54

Table 2-2.(con't) Alpha Micro Bus Interface Signals List

MNEMONIC	NAME	PIN NO.
$\overline{\text{DMA0}}$	DMA Controller Arbitration	55
$\overline{\text{DMA1}}$	Lines For Use With Standard	56
$\overline{\text{DMA2}}$	S-100 Bus DMA System	57
$\overline{\text{SXTRQ}}$	16 Bit Cycle	58
A19	Address 19	59
N/U	Not Used	60
A20 A21 A22 A23	Address 20 Address 21 Address 22 Address 23	61 62 63 64
$\overline{\text{ADVAL}}$	Address Valid On Data Bus	65
$\overline{\text{WRDIS}}$	Write Disable	66
$\overline{\text{PHANTOM}}$	ROM Memory Enable	67
N/U N/U	Not Used Not Used	68 69
Gnd	Ground	70
N/U	Not Used	71
PRDY	Processor Ready	72

Table 2-2.(con't) Alpha Micro Bus Interface Signals List

MNEMONIC	NAME	PIN NO.
N/U	Not Used	73
$\overline{\text{PHOLD}}$	DMA Request	74
$\overline{\text{PRESET}}$	Preset	75
PSYNC	Processor Sync, Start of Bus Cycle	76
$\overline{\text{PWR}}$	Write Strobe	77
PDBIN	Data Bus Input Command	78
A0	Address 0	79
A1	Address 1	80
A2	Address 2	81
A6	Address 6	82
A7	Address 7	83
A8	Address 8	84
A13	Address 13	85
A14	Address 14	86
A11	Address 11	87
DOUT 2/D2	Data Bus Bit 2	88
DOUT 3/D3	Data Bus Bit 3	89
DOUT 7/D7	Data Bus Bit 7	90
DIN 4/D12	Data Bus Bit 7	91
DIN 5/D13	Data Bus Bit 13	92
DIN 6/D14	Data Bus Bit 14	93
DIN 1/D9	Data Bus Bit 9	94
DIN 0/D8	Data Bus Bit 8	95

Table 2-2.(con't) Alpha Micro Bus Interface Signals List

MNEMONIC	NAME	PIN NO.
SINTA	Interrupt Acknowledge	96
$\overline{\text{SWO}}$	Bus Master Output	97
$\overline{\text{ERROR}}$	Memory Error Interrupt	98
$\overline{\text{BERR}}$	Bus Error	99
GND	Ground	100

Table 2-3. ECC Board Interface Signals

MNEMONIC	NAME	PIN NO.
GND	Ground	1
-	Not Used	2
ECCD1	ECC Data Bit 1	3
ECCD0	ECC Data Bit 0	4
ECCD7	ECC Data Bit 7	5
ECCD2	ECC Data Bit 2	6
ECCD6	ECC Data Bit 6	7
ECCD3	ECC Data Bit 3	8
ECCD5	ECC Data Bit 5	9
ECCD4	ECC Data Bit 4	10
ECCD8	ECC Data Bit 8	11
ECCD17	ECC Data Bit 17	12
ECCR/W	ECC Read/Write	13
ECCD16	ECC Data Bit 16	14
ECCENABLE	ECC Enable	15
ECCD9	ECC Data Bit 9	16

Table 2-3. (Con't) ECC Board Interface Signals

MNEMONIC	NAME	PIN NO.
ECCREFCLK	ECC Refresh Clock	17
ECCD10	ECC Data Bit 10	18
ECCD15	ECC Data Bit 15	19
ECCD11	ECC Data Bit 11	20
ECCD14	ECC Data Bit 14	21
ECCD12	ECC Data Bit 12	22
-	Not Used	23
ECCD13	ECC Data Bit 13	24
-	Not Used	25
-	Not Used	26

2.3 USER OPTIONS.

The AM-720 memory circuit board accommodates several options that are selected by the user for specific requirements. These options are for CPU type, addressing configuration selection, reset select, ECC board select, parity error select, parity output select, and phantom memory select. Location of jumpers is shown in Figure 2-1.

2.3.1 CPU Select

A jumper must be installed to make the AM-720 compatible with the system CPU. Place a jumper in the location corresponding to the CPU type as follows:

Jumper	CPU
W15, 100T	AM-100/T CPU
W16, 100L	AM-100/L CPU

2.3.2 Addressing Configuration Selection.

The AM-720 is configured for extended addressing (A0-A23). Make selections for system compatibility as follows:

For extended addressing configuration the board address is set by placing jumpers at address bits A19 through A23. That is, place jumpers at jumper block positiions A19, $\overline{A19}$, A20, $\overline{A20}$, A21, $\overline{A21}$, A22, $\overline{A22}$, A23 and $\overline{A23}$. Also for extended addressing configuration, jumper W7 must be removed and jumpers W8 and W9 must be in place.

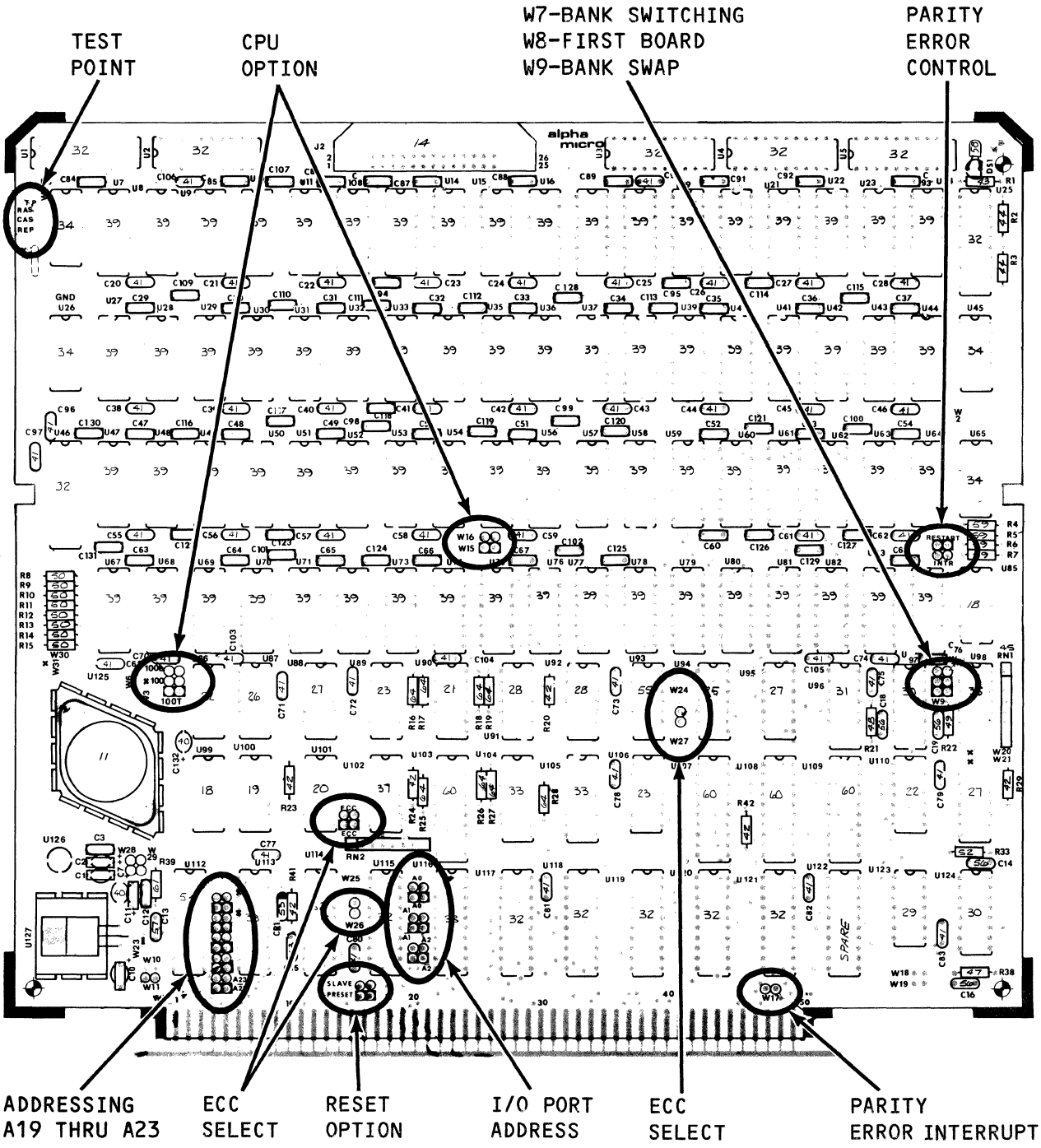


Figure 2-1. Location of Option Jumpers

2.3.2.1 Memory Bank Swap.

If trouble is suspected in the memory ICs, provision has been made to physically swap the memory banks by removing jumper W9. With W9 in place, memory IC configuration is as follows:

Bank 1	U7-U24
Bank 2	U27-U44
Bank 3	U47-U64
Bank 4	U67-U84

With W9 removed, bank 1 is swapped with bank 4 and bank 2 is swapped with bank 3 as follows:

Bank 1	U67-U84
Bank 2	U47-U64
Bank 3	U27-U44
Bank 4	U7 -U24

2.3.3 Reset Select.

The source of the AM-720 reset signal may be selected to be from bus signal PRESET on pin 75 or SLAVECLR on pin 54. Make selection for reset source as follows:

PRESET	Pin 75	Install "PRESET" Remove "SLAVE"
SLAVECLR	Pin 54	Install "SLAVE" Remove "PRESET"

Standard configuration is PRESET jumper installed.

2.3.4 ECC Board Select.

When the AM-720 operates through an ECC board, an ECC ENABLE signal from the ECC board sets the data I/O to operate through the ECC board. For non-ECC operations install the ECC/jumper. The memory refresh can be selected to originate either from the AM-720 or the ECC board. If refresh is to be from the ECC board, cut the etch at W10 and install a jumper at W11.

2.3.5 Parity Error Selections.

Parity error interrupt is enabled by setting bit 3 of the I/O register. Powerup or reset will disable this function. After the parity error enable bit is set, a parity error will cause an interrupt.

1. For AM-100/T Rev A through Rev C system:

    a. Parity error will cause an interrupt through bus pin J1-98.

    b. Install jumper "W17" and "INTR".

    c. Once asserted, the interrupt line will be terminated only by clearing interrupt enable bit.

2. For AM-100/T Rev D and later systems or AM-100/L.

    a. Parity error will cause an interrupt through bus pin J1-49.

    b. Install jumper RESTART; make sure jumper W17 is out.

The LED on the upper right corner will be lit when a parity error has been detected. The LED will not be turned off until the system is reset.

3.0 INTRODUCTION.

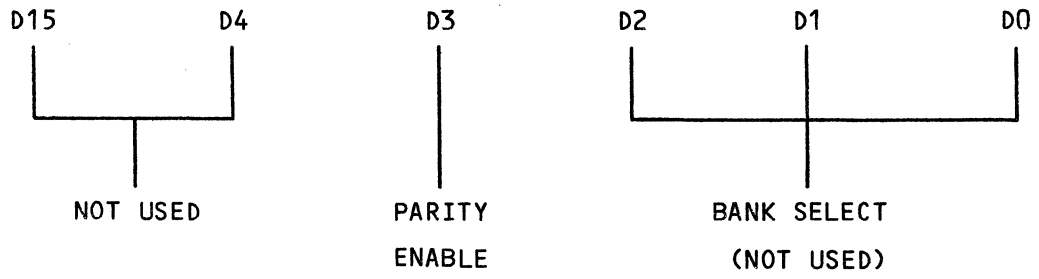
This section provides the programming requirements for the AM-720 memory circuit board. The AM-720 can be used with either the AM-100/T (with an AM-700 board) or AM-100/L CPU systems. Ensure that all the correct options have been selected and that the requirements of Section II have been met.

3.1 EXTENDED ADDRESSING

The AM-720 memory address can start at any 512KB boundary for the contiguous 512KB portion of memory contained on the board. The board can accommodate a 16 megabyte system addressing capability with extended addressing (A0-A23).

3.2 I/O REGISTER

The I/O addresses should be set to 100 octal for all AM-720 boards. (Install jumper block $\overline{A0}$, $\overline{A1}$, and $\overline{A2}$.) The I/O register bit assignments for each board are as follows:



4.0 INTRODUCTION.

The AM-720 memory circuit board contains integrated circuit elements for the data processing necessary for the performance of the functions described in Sections I, II and III of this manual. This section describes the functional theory of operation of the circuit board and also provides information for each of the integrated circuit elements.

4.1 CIRCUIT BOARD OPERATION.

The AM-720 circuit board is a 256k x 18 bit dynamic MOS read/write memory. The functional block diagram of the circuit board is shown in Figure 4-1. The circuit board schematic, parts list, and component cross-reference list is contained in Section IV of this manual. Table 4-1 contains a list of the signals used in this circuit board with descriptions of their functions. For Alpha Micro bus interface signals, see Table 2-2.

The AM-720 consists of an array of dynamic memory ICs with circuitry for memory refresh and data read and write. Logic is included for parity generation and checking. Addressing capability is provided for extended addressing (A0-A23). Memory data can be written/read directly via the bus or through an error checking/correction (ECC) board.

Selection of the various optional capabilities of the AM-720 are described in Section II of this manual.

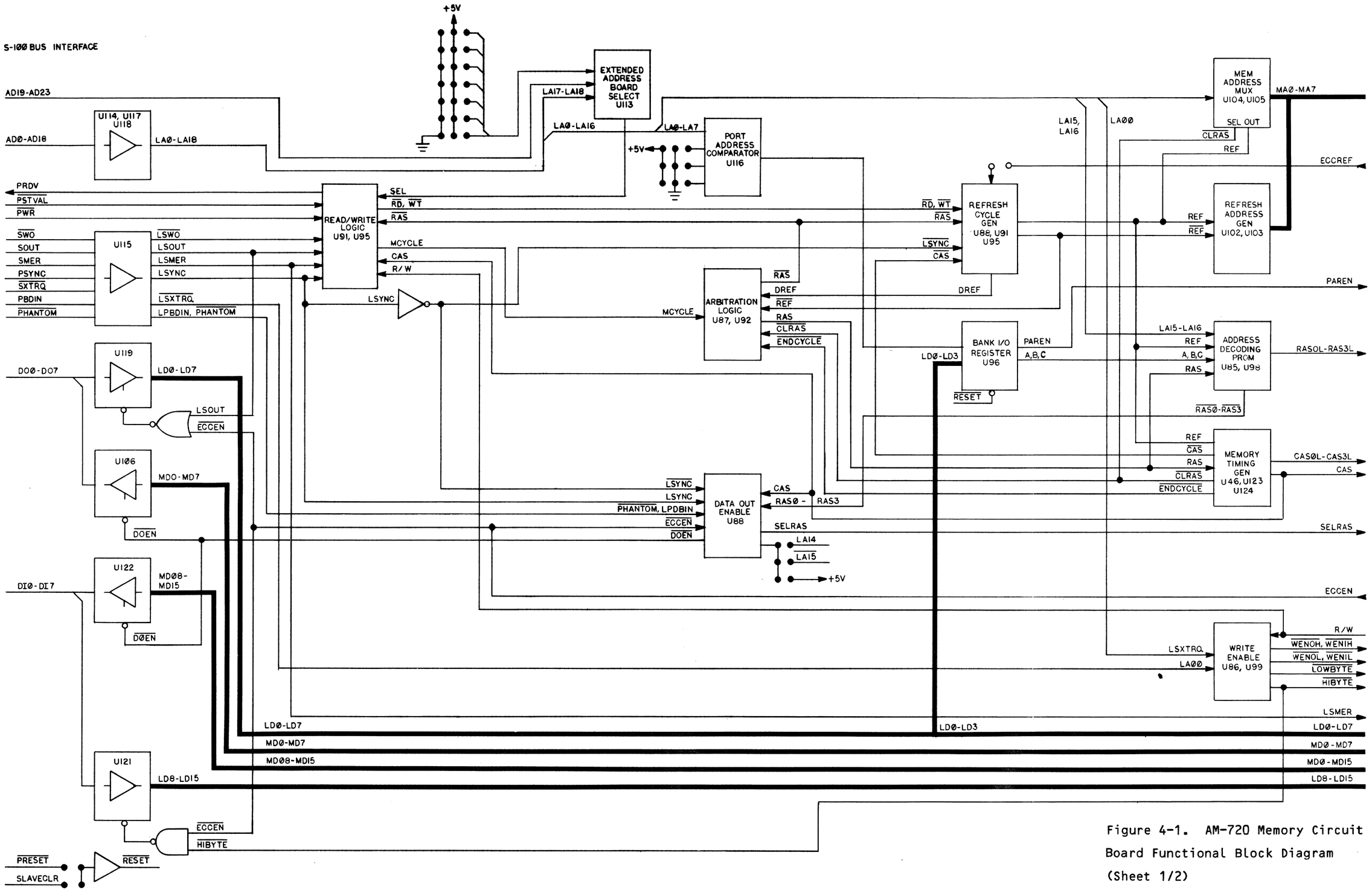


Figure 4-1. AM-720 Memory Circuit Board Functional Block Diagram (Sheet 1/2)

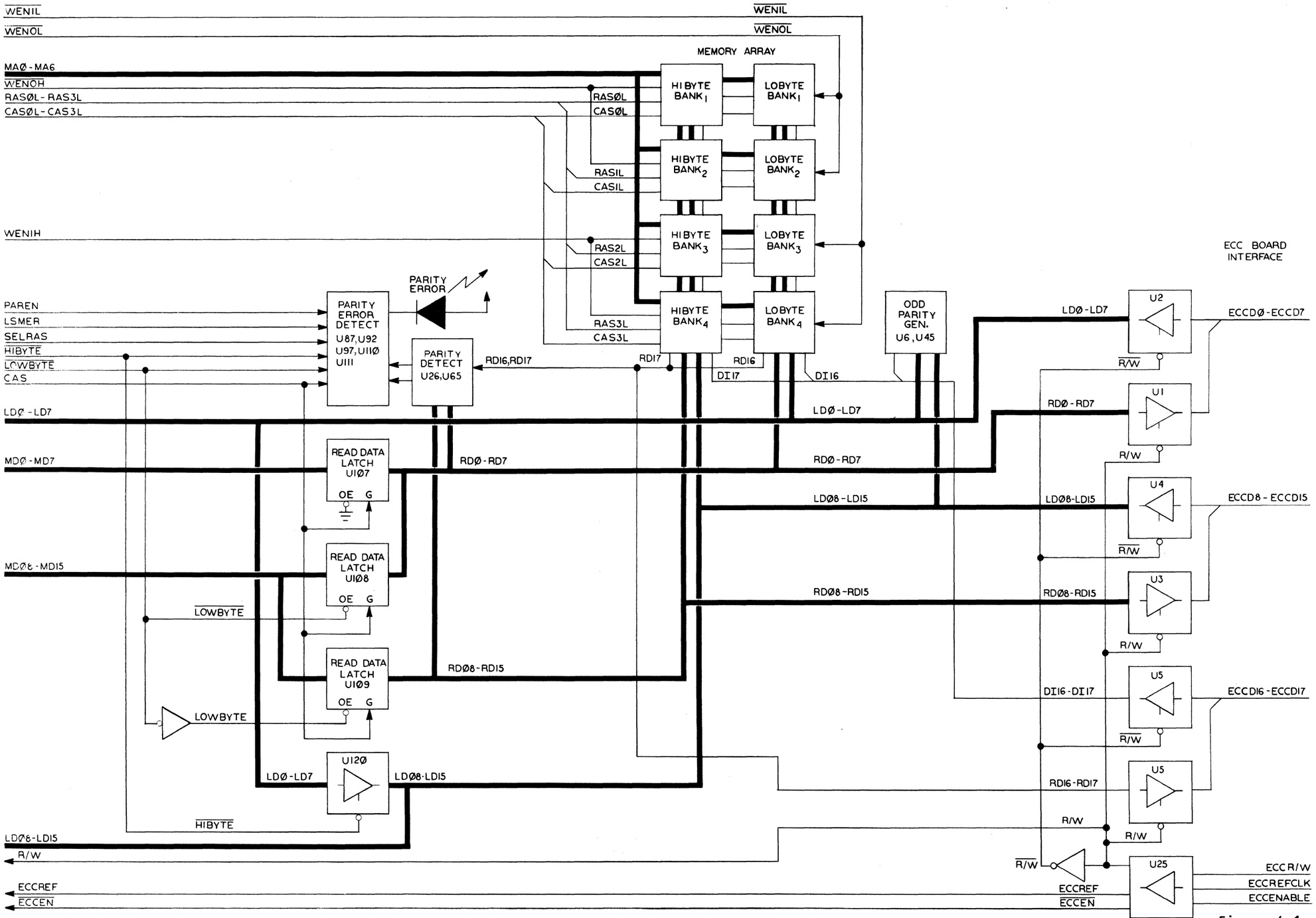


Figure 4-1. AM-720 Memory Circuit Board Functional Block Diagram (Sheet 2/2)

Table 4-1. AM-720 Signal Descriptions

SIGNAL	NAME	SCHEM PAGE OF SOURCE	DESCRIPTION
A, B, C	Memory Address Decode Bits	1	Outputs of bank switching register to operate address decoding PROM. (NOT USED)
CAS $\overline{CAS}$	Column Address Strobe	1	Generated by the memory timing and the arbitration logic to latch the column address bits into the memory array.
$\overline{CAS0L}$- $\overline{CAS3L}$	Column Address Strobe Banks 0-3	2	Column address strobe signals for memory banks 1-4.
CLRAS $\overline{CLRAS}$	Column/Row Address Select	1	Memory timing generator output to generate CAS, RAS and switch the memory address select MUX from the row address to the column address.
DI16, DI17	Parity Bits	3	Parity bits from the ECC board or the parity generator to the memory.
$\overline{DOEN}$	Data Output Enable	2	Generated by the data output enable logic to assert memory data to the S-100 Bus data lines.

Table 4-1 (Con't.) AM-720 Signal Descriptions

SIGNAL	NAME	SCHEM PAGE OF SOURCE	DESCRIPTION
DREF	Delayed Refresh	1	Memory refresh signal delayed to allow refresh address to stabilize.
ECCEN	ECC Board Enable	3	Enable signal from the ECC board to inhibit data from the S-100 Bus.
ECCREF	ECC Board Refresh	3	Memory refresh clock from the ECC board.
ENDCYCLE	End Cycle	1	Output of a one-shot triggered by RAS to the arbitration logic to inhibit memory or refresh cycle inputs after a memory cycle begins.
HIBYTE	Select High Byte	2	Output of the write enable logic to select data bits 8-15.
LA00-LA23	System Address Bus	1	Tri-state address bus driven directly from S-100 Bus address lines.

Table 4-1 (Con't.) AM-720 Signal Descriptions

SIGNAL	NAME	SCHEM PAGE OF SOURCE	DESCRIPTION
LD00-LD15	Output Data Bus	1	Tri-state data bus to memory from either the ECC board or from the S-100 Bus data lines.
LOWBYTE	Select Low Byte	2	Output of the write enable logic to select data bits 0-7.
LPBDIN	Board Data Bus Input Command	1	Generated directly from PDBIN on S-100 Bus.
LPHANTOM	Board Phantom	1	Generated directly from PHANTOM on S-100 Bus.
LPWR	Board Write Strobe	1	Generated directly from PWR on S-100 Bus.
LSMER	Board Memory Read Cycle	1	Generated directly from SMER on S-100 Bus.
LSOUT	Board I/O Output Cycle	1	Generated directly from SOUT on S-100 Bus.

Table 4-1 (Con't.) AM-720 Signal Descriptions

SIGNAL	NAME	SCHEM PAGE OF SOURCE	DESCRIPTION
LSWO	Board Bus Master Output	1	Generated directly from SWO on S-100 Bus.
LSXTRQ	Board 16-Bit Cycle	1	Generated directly from SXTRQ on S-100 Bus.
LSYNC $\overline{\text{LSYNC}}$	Board Processor Sync	1	Generated directly from PSYNC on S-100 Bus.
MA0-MA7	Memory Address Lines	2	Address data from either the refresh address generator or system address data.
MCYCLE	Memory Cycle	1	Memory read or write cycle in process. Used for arbitration logic and to generate PRDY on the S-100 Bus if REFRESH is in process.
MD00-MD15	Memory Data Bus	1	Memory data bus from memory to S-100 Bus data lines.
PAREN	Parity Enable	1	Generated from data bit 3 in the bank I/O register to enable the parity error detection.

Table 4-1 (Con't.) AM-720 Signal Descriptions

SIGNAL	NAME	SCHEM PAGE OF SOURCE	DESCRIPTION
RAS $\overline{\text{RAS}}$	Row Address Strobe	1	Generated by the memory timing and the arbitration logic to latch the row address bits into the memory array.
RAS0- RAS3	Row Address Strobe 0-3	1	Row address strobe signals for memory banks 1-4.
$\overline{\text{RAS0L}}$- $\overline{\text{RAS3L}}$	Row Address Strobe Banks 0-3	1	Row address strobe signals for memory banks 1-4.
RD	Read	1	Memory read signal used to generate a memory cycle and inhibit a refresh request.
RD00-RD15 RD16, RD17	Memory Read Bits	4,5	Data read from the memory array. Bits 0-15 are data, bits 16 and 17 are parity.
REF $\overline{\text{REF}}$	Refresh	1	Memory refresh signal advances the refresh address counter, enables the output of the refresh address latch, inhibits data from the address bus LA01-LA16, inhibits a memory read/write cycle, and inhibits CAS.

Table 4-1 (Con't). AM-720 Signal Descriptions

SIGNAL	NAME	SCHEM PAGE OF SOURCE	DESCRIPTION
REFREQ	Refresh Request	1	Memory refresh request output of refresh cycle generator.
RESET	Reset	1	Board reset signal from S-100 Bus signal either PRESET or SLAVECLR.
R/W $\overline{R/W}$	Read/Write	3	Read/write select signal from ECC board Read/Write select.
SEL $\overline{SEL}$	Board Select	1	Output of the board select address comparator for extended addressing configuration.
SELRAS	Select Row Address Strobe	2	Asserted when any of RAS0-RAS3 are asserted. Used to generate DOEN.
WEN0H WEN1H	Write Enable High Byte	2	Write enable signals for the high byte section of the memory array.

Table 4-1 (Con't.) AM-720 Signal Descriptions

SIGNAL	NAME	SCHEM PAGE OF SOURCE	DESCRIPTION
WEN0L WEN1L	Write Enable Low Byte	2	Write enable signals for the low byte section of the memory array.
WT	Write	1	Memory write signal used to generate a memory cycle and inhibit a refresh request.

4.1.1 Memory Array.

The memory array consists of 72 memory modules of 65,536 one-bit locations each. The modules are configured in four banks of 18 bits each; 16 bits of data and two parity bits.

4.1.1.1 Memory Module.

The 16 address bits required to decode 1 of the 65,536 cell locations within the device are multiplexed onto the 8 address inputs MA0-MA7 and latched into the on-chip address latches by applying two strobes. Read and write operations are selected by a write enable signal (low for write, high for read). The timing strobes are asserted when driven low.

The two strobes are Row Address Strobe (RAS) and Column Address Strobe (CAS). The memory cycle begins when RAS is asserted and the seven row address bits are already applied via the memory address MUX (U104 and U105). The row address bits are LA08-LA14, LA16.

Signal RAS then sets the CLRAS flip-flop which switches the memory address MUX to the column address from bits LA01-LA07, LA15. For a complete description of the memory module, see paragraph 4.2.11.

4.1.1.2 Memory Array.

The memory modules are laid out in an array of 4 rows with 18 modules in each row for 16 data bits and 2 parity bits. Address control bits MA0-MA7 are connected in each row which forms a bank of 128K bytes. Memory can be read or written in either byte mode or word mode. During word operation, both enable signals WENH and WENL (Word Enable High and Word Enable Low) are asserted to enable all 18 bits. During byte operation, either high byte or low byte is enabled.

4.1.2 Memory Refresh.

The entire memory must be refreshed every two milliseconds. This can be a normal read or write cycle which refreshes the memory or a board refresh cycle. A board refresh cycle differs from a normal memory cycle in that only RAS is asserted. The memory is refreshed for all row addresses.

A board refresh request is initiated by REFREQ from the refresh cycle generator which is asynchronous. This is driven by an onboard oscillator or from the ECC board depending on user options. With an asynchronous refresh, a refresh cycle and a system memory cycle can be requested simultaneously. Therefore the REF flip-flop is gated by RD and WT and LSYNC so a refresh cycle cannot occur while a memory cycle is in process. The arbitration logic also inhibits a memory cycle while a refresh cycle is in process. Signal DREF (Delayed Refresh) generates RAS after the address lines have had time to settle.

The refresh addresses are generated by the refresh address generator U102 and are latched into U103. Signal REF inhibits the output at the memory address MUX and REF enables the output of the refresh address latch.

4.1.3 Addressing.

The AM-720 can operate as a 16 megabyte system with extended addressing (A0-A23). For extended addressing operation, board select comparator U113 detects the assigned board address and generates SEL. This enables memory read/write logic to initiate the desired memory cycle. Address bits from the S-100 Bus (LA01-LA16) are applied directly to the memory address MUX. Signal CLRAS then selects the appropriate row and column addresses for the memory cycle.

4.1.4 Parity.

The AM-720 is designed with byte parity capability. Parity bits are DI16 which is odd parity for data bits LD00-LD07 and DI17 for data bits LD08-LD15. Parity is generated during memory write operations by U6 and U45 and stored in the memory array.

During memory read operations, wrong parity is detected and causes a parity error interrupt on the S-100 Bus. The parity detectors are U26 for data bits RD00-RD07, RD16 and U65 for bits RD08-RD15, RD17 (bits 16 and 17 are the parity bits). These two detector outputs are ORed to set the parity error interrupt and light the LED at the edge of the board. The LED stays lit until the system is reset. Parity error interrupt is enabled by setting bit 3 of the I/O register. Power-up or reset disables this function.

4.1.5 ECC Board Interface.

The ECC board interface is through the connector on top of the board. Access to AM-720 data busses is through drivers U1-U5 and U25. The ECC board controls memory read/write operations by generating R/W to control the interface drivers, write enable logic and memory read/write logic.

ECC enable (ECCEN) is asserted when the ECC board is operating and inhibits the data out enable logic.

The ECC board can also provide memory refresh signals to the refresh request logic. This is jumper selectable by jumpers W10 and W11.

4.1.6 Data Transfer Operations.

Data transfer operation is the same through the ECC board or directly through the S-100 Bus. Memory write and read timing is shown in Figure 4-2.

4.1.6.1 Memory Write.

For a memory write cycle, the board is addressed generating SEL from the board select comparator. S-100 Bus signals SWO (bus master output cycle) and SOUT (I/O output cycle) are ANDed with write strobe PWR to generate a write memory cycle WT and MCYCLE. This sets row address strobe (RAS) for the memory to accept row address data. Signal CLRAS is asserted to switch the memory address MUX from the row address bits (LA08-LA14,LA16) to the column address (LA00-LA07,LA15) and generate the column address strobes to the memory array. The memory then accepts valid data from the write data bus LD00-LD15. The cycle terminates when CLRAS clears RAS which clears WT and MCYCLE.

4.1.6.2 Memory Read.

For a memory read cycle, the board is addressed generating SEL as with a write cycle. S-100 Bus signals PSYNC (Processor Sync), STVAL (Status and Address Valid), and SMER (Memory Read Cycle) are combined to set RD and MCYCLE. This generates row and column address strobes in the same timing as with a memory write cycle. Valid data from the memory is then applied to read data bus RD00-RD15. The cycle terminates when CLRAS clears RAS which clears RD and MCYCLE. Signal CAS clocks the parity error logic to generate a parity interrupt and light the parity LED should a parity error occur.

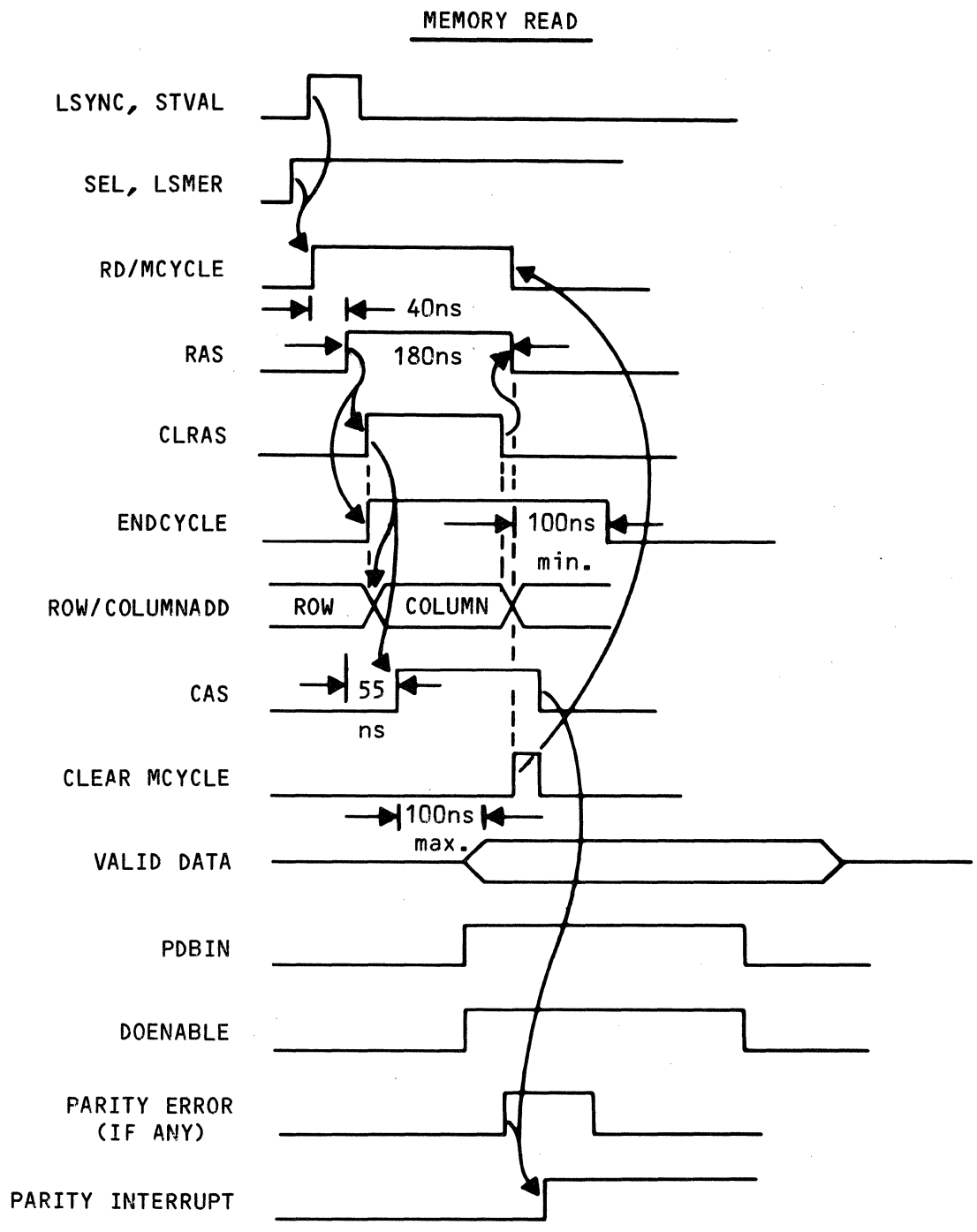


Figure 4-2. Memory Timing (Sheet 1/2)

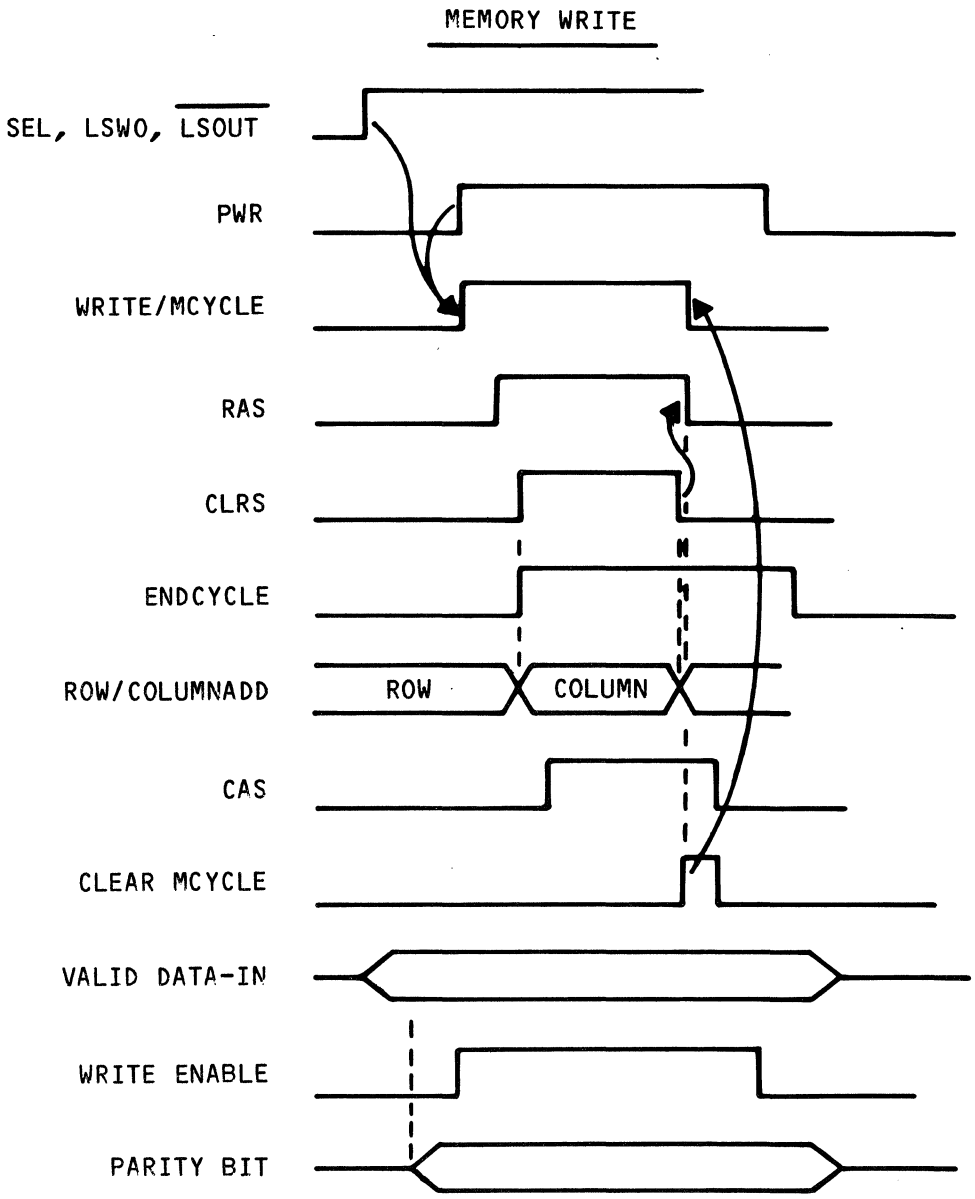


Figure 4-2. Memory Timing (Sheet 2/2)

4.2 CIRCUIT MODULE DESCRIPTION.

This section describes the operation of the individual circuit modules contained on the AM-720 circuit board. The control logic and interface modules are described with logic and connection diagrams for each one.

4.2.1 Eight-Bit Equal-To Comparator (U113).

This device is an eight-bit equal-to comparator that compares two eight-bit words for equality with provision for expansion or external enabling. The matching of the two eight-bit inputs plus a logic low on the EIN input produces an active low on the output EOUT. The outputs are valid where A0-A7 and B0-B7 are expressed as either assertions or negations. This is also true for a pair of Terms, i.e., A0 can be compared with B0 at the same time A1 is compared with B1. It is essential that the polarity of the paired Terms be maintained. For logic and connections see Figure 4-3.

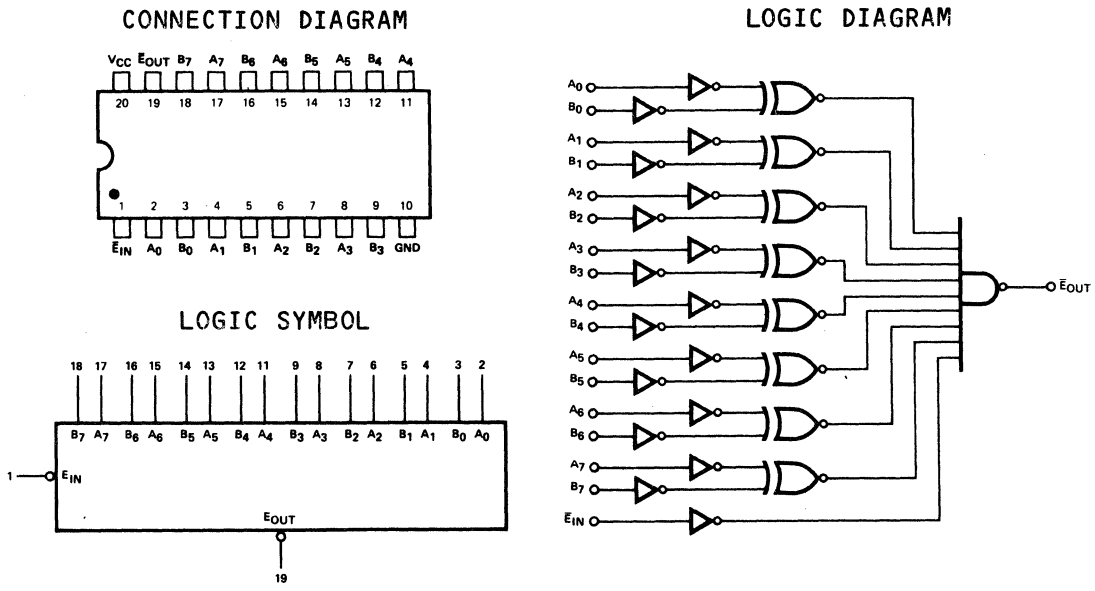
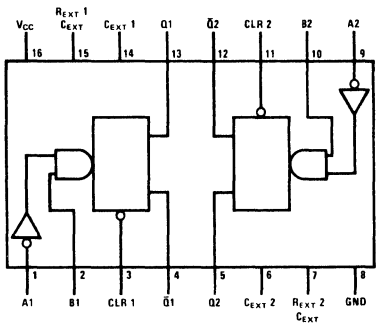


Figure 4-3. Equal to Comparator Logic and Connections

4.2.2 Dual Retriggerable One-Shots With Clear (U97, U124). See Figure 4-4 for logic diagram and truth table.

LOGIC DIAGRAM



TRUTH TABLE

INPUTS			OUTPUTS	
A	B	CLR	Q	$\overline{Q}$
H	X	H	L	H
X	L	H	L	H
L	↑	H	⎍	⎏
↓	H	H	⎍	⎏
X	X	L	L	H

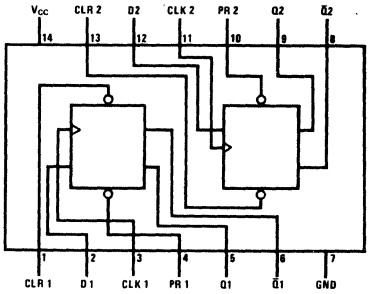
Notes: ⎍ = one high-level pulse, ⎏ = one low-level pulse.
To use the internal timing resistor of 54121/74121, connect R_{INT} to V_{CC}.
An external timing capacitor may be connected between C_{EXT} and R_{EXT}/C_{EXT} (positive).
For accurate repeatable pulse widths, connect an external resistor between R_{EXT}/C_{EXT} and V_{CC} with R_{INT} open-circuited.
To obtain variable pulse widths, connect external variable resistance between R_{INT} or R_{EXT}/C_{EXT} and V_{CC}.

Figure 4-4. One-Shot Connections

4.2.3 Dual D Positive-Edge-Triggered Flip-Flops With Preset and Clear (U88, U91, U92, U95, U111).

For logic and connections, see Figure 4-5.

CONNECTION DIAGRAM



TRUTH TABLE

INPUTS				OUTPUTS	
PR	CLR	CLK	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q0	$\bar{Q}0$

Notes: ⎍⎍ = high-level pulse; data inputs should be held constant while clock is high; data is transferred to output on the falling edge of the pulse.

Q0 = the level of Q before the indicated input conditions were established.

TOGGLE: Each output changes to the complement of its previous level on each active transition (pulse) of the clock.

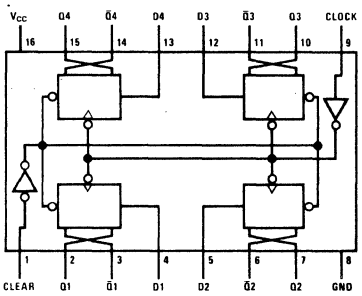
*This configuration is nonstable, that is, it will not persist when preset and clear inputs return to their inactive (high) level.

Figure 4-5. Dual-D Flip-Flop Connections

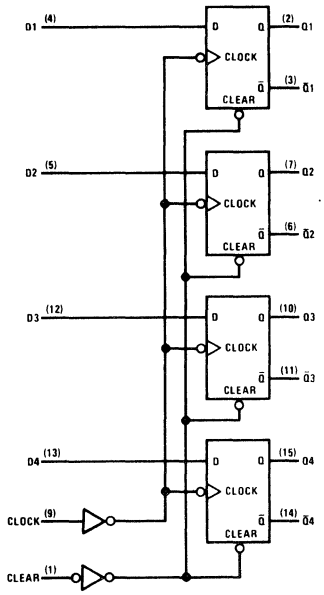
4.2.4 Quad D Flip-Flops With Clear (U96).

These positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. They feature a direct clear input and complementary outputs from each flip-flop. Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output. For logic and connections, See Figure 4-6.

CONNECTION DIAGRAM



LOGIC DIAGRAM



TRUTH TABLE

INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\bar{Q}$†
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\bar{Q}_0$

H = High Level (steady state)
L = Low Level (steady state)
X = Don't Care
↑ = Transition from low to high level
Q_0 = The level of Q before the indicated steady-state input conditions were established.
† = 175, LS175, and S175 only

Figure 4-6. Quad D Flip-Flops with Clear, Logic and Connections

4.2.5 Noninverting Octal Bus Driver (U1-U5, U25, U46, U106, U115, U117-U121).

These buffers provide the drive capability for tri-state bus requirements and are noninverting. For logic and connections, see Figure 4-7.

CONNECTION DIAGRAM

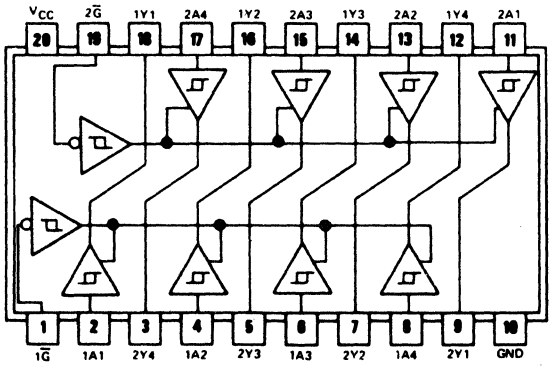
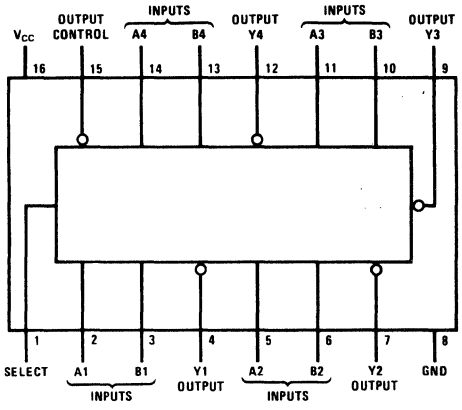


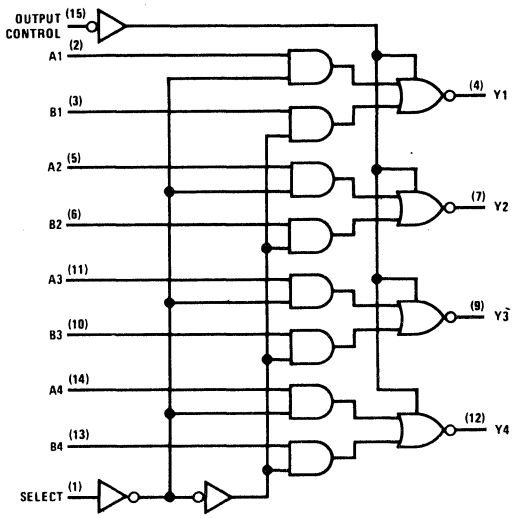
Figure 4-7. Noninverting Bus Driver Connections

4.2.6 Tri-State Quad Two-Data Selectors/Multiplexers (U104, U105). These multiplexers feature tri-state outputs that interface directly with data lines of bus sytems. With all but one of the common outputs disabled (at a high impedance state), the low impedance of the single enabled output will drive the bus line to a high or low logic level. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output enable circuitry is designed such that the output disable times are shorter than the output enable times. For logic and connections, see Figure 4-8.

CONNECTION DIAGRAM



LOGIC DIAGRAM



TRUTH TABLE

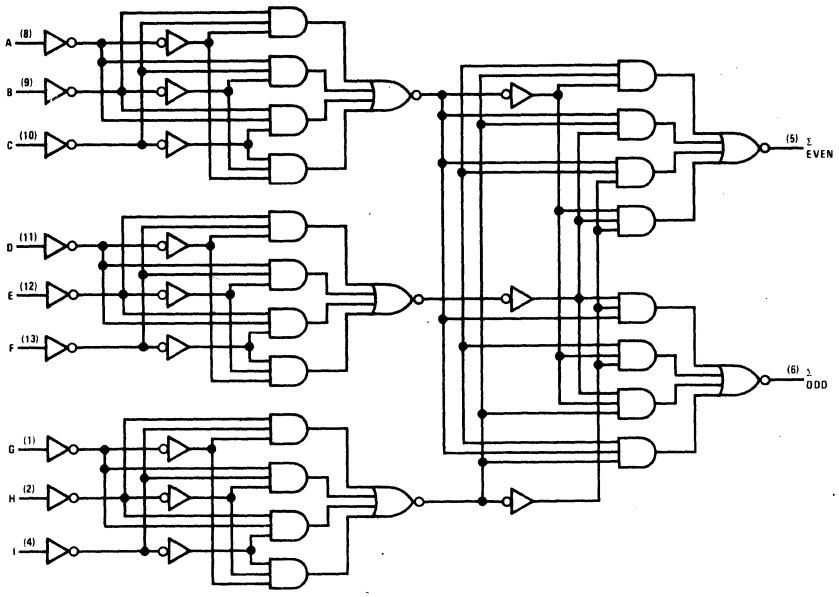
INPUTS				OUTPUT Y
OUTPUT CONTROL	SELECT	A	B	LS257 S257
H	X	X	X	Z
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = High Level, L = Low Level, X = Don't Care,
Z = High Impedance (off)

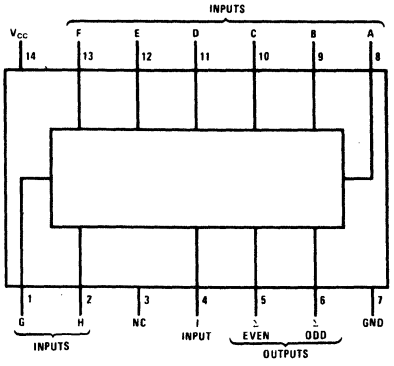
Figure 4-8. Two-Data Selectors/Multiplexer Connections

4.2.7 Nine-Bit Parity Generator/Checker (U6, U26, U45, U65). This universal, nine-bit parity generator/checker utilizes Schottky-clamped TTL high-performance circuitry and features odd/even outputs to facilitate operation of either odd or even parity applications. For logic and connections, see Figure 4-9.

LOGIC DIAGRAM



CONNECTION DIAGRAM



TRUTH TABLE

NUMBER OF INPUTS (A THRU I) THAT ARE HIGH	OUTPUTS	
	Σ EVEN	Σ ODD
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

Figure 4-9. Nine-Bit Parity Generator/Checker

4.2.8 1024-Bit Programmable Read Only Memory (U98).

This device is a field-programmable, 1024-bit, read only memory organized as 256 words of four bits each. This high-speed, Schottky-clamped, TTL memory array is addressed in 8-bit binary with full on-chip decoding. Two overriding chip-select inputs are provided, which, when either one or both are high, cause all four outputs to be in the high impedance state.

The address of a 4-bit word is accomplished through the buffered binary select inputs, with a low level at both chip-select inputs. Where multiple devices are used in a memory system, the chip-select inputs allow easy decoding of additional address bits.

Data can be electronically programmed at any of the 1024-bit locations. Prior to programming, the memory contains a low logic level output condition at all bit locations. The programming procedure is irreversible; once altered, the output for that bit is permanently programmed to provide a high logic level. Outputs never having been altered may later be programmed to supply a high level output. Operation of the device within the recommended operating conditions will not alter the memory content. For logic and connections, see Figure 4-10.

LOGIC/CONNECTION DIAGRAM

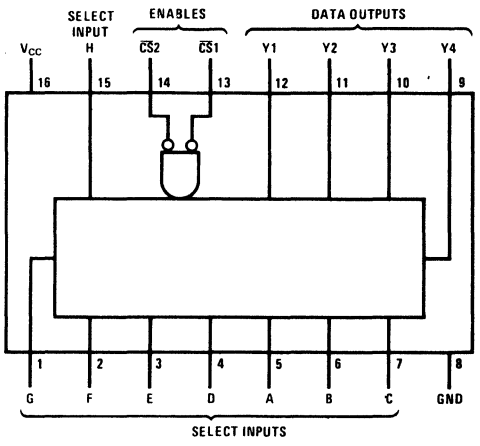
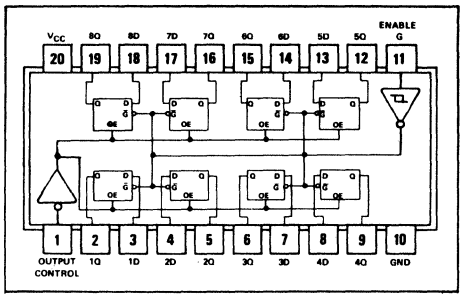


Figure 4-10. 1024-Bit Programmable Read Only Memory

4.2.9 Octal D-Type Transparent Latch (U103, U107-U109).
This 8-bit register is a transparent D-type latch with three-state outputs. While the enable (G) is high, the Q outputs follow the data (D) inputs. When the enable is low, the output will be latched at the level of the data that was set up. For logic and connections, see Figure 4-11.

CONNECTION DIAGRAM



TRUTH TABLE

OUTPUT CONTROL	ENABLE G	D	OUTPUT
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

LOGIC DIAGRAM

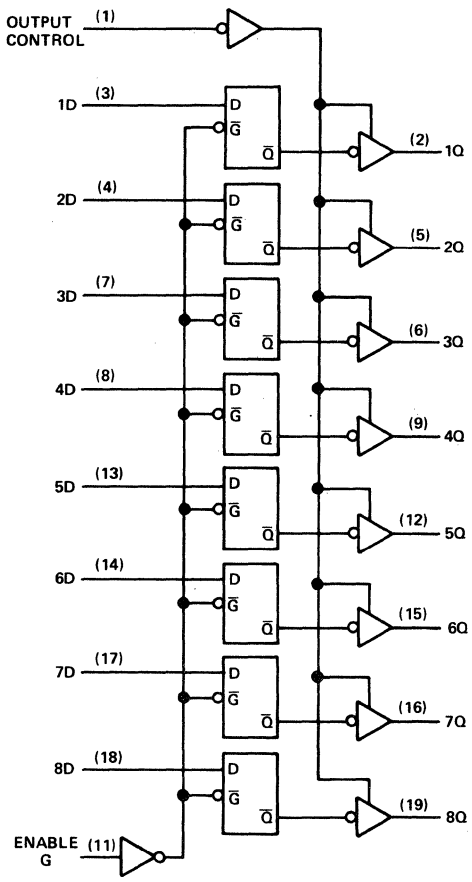
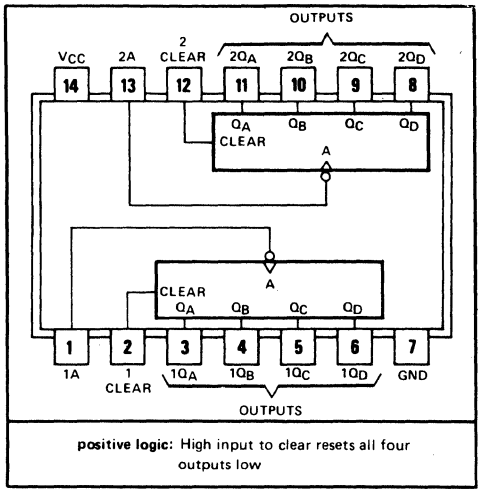


Figure 4-11. Transparent Latch Logic and Connections

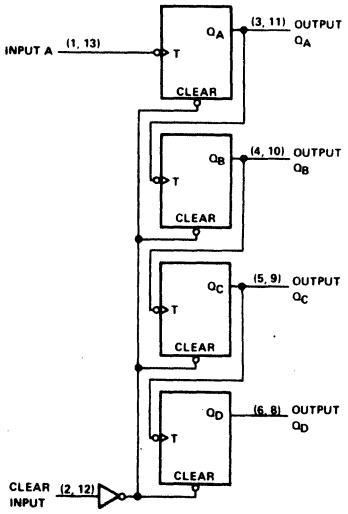
4.2.10 Dual 4-Bit Binary Counter (U102).

These devices contain eight master-slave flip-flops and additional gating to implement two individual 4-bit counters in a single package, each with a clear and clock input. Parallel outputs are available from each counter so that any submultiple of the input count frequency is available. See Figure 4-12 for logic diagram and truth table.

CONNECTION DIAGRAM



LOGIC DIAGRAM



TRUTH TABLE

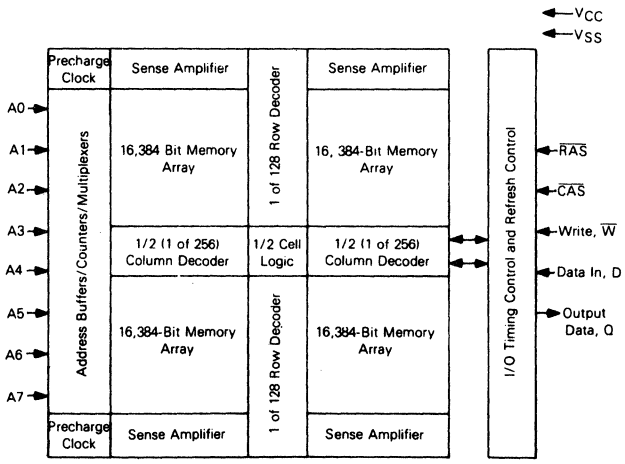
COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

Figure 4-12. 4-Bit Binary Counter Connections

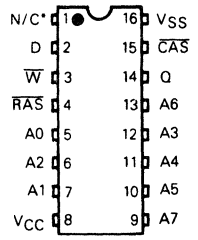
4.2.11 65,536-Bit Dynamic RAM (U7-U24, U27-U44, U47-U64, U67-U84).

THE MCM6665 is a 65,536 bit, high-speed, dynamic Random-Access Memory. Organized as 65,536 one-bit words and fabricated using HMOS high-performance N-channel silicon-gate technology. This new breed of 5-volt only dynamic RAM combines high performance with low cost and improved reliability. A functional diagram and pin connections are shown in Figure 4-13.

FUNCTION DIAGRAM



CONNECTION DIAGRAM



PIN NAMES	
A0-A7	Address Input
D	Data In
Q	Data Out
W	Read/Write Input
RAS	Row Address Strobe
CAS	Column Address Strobe
VCC	Power (+5 V)
VSS	Ground

Figure 4-13. Dynamic RAM Functional Diagram and Pin Connections

4.2.11.1 Addressing.

The 16 address bits required to decode 1 of the 65,536 cell locations within the device are multiplexed onto the 8 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks. The first clock, the Row Address Strobe (RAS), latches the 8 row address bits into the chip. The second clock, the Column Address Strobe (CAS), subsequently latches the 8 column address bits into the chip. Each of these signals, RAS and CAS, triggers a sequence of events which is controlled by different delayed internal clocks. The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the CAS clock sequence are inhibited until the occurrence of a delayed signal derived from the RAS clock chain. This "gated CAS" feature allows the CAS clock to be externally activated as soon as the Row Address Hold Time specification (tRAH) has changed from Row address to Column address information.

Note that CAS can be activated at any time after tRAH and it will have no effect on the worst case data access time (tRAC) up to the point in time when the delayed row clock no longer inhibits the remaining sequence of column clocks. Two timing endpoints result from the internal gating of CAS which are called tRCD (min) and tRCD (max). No data storage or reading errors will result if CAS is applied to the device at a point in time beyond the tRCD (max) limit. However, access time will then be determined exclusively by the access time from CAS (tCAC) rather than from RAS (tRAC), and access time from RAS will be lengthened by the amount that tRCD exceeds the tRCD (max) limit.

4.2.11.2 Data Input/Output.

Data to be written into a selected cell is latched into an on-chip register by a combination of WRITE and CAS while RAS is active. (The later of the signals (WRITE or CAS) to make its negative transition is the strobe for the Data In (DIN) register.) This permits several options in the write cycle timing. In a write cycle, if the WRITE input is brought low (active) prior to CAS, the DIN is strobed by CAS, and the set-up and hold times are referenced to CAS. If the input data is not available at CAS time or if it is desired that the cycle be a read-write cycle, the WRITE signal will be delayed until after CAS has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of WRITE rather than CAS. (To illustrate this feature, DIN is referenced to WRITE in the timing diagrams depicting the read-write and page-mode write cycles while the "early write" cycle diagram shows DIN referenced to CAS).

Data is retrieved from the memory in a read cycle by maintaining WRITE in the inactive or high state throughout the portion of the memory cycle in which CAS is active (low). Data read from the selected cell will be available at the output within the specified access time.

4.2.11.3 Data Output Control.

The normal condition of the Data Output (DOUT) of the device is the high impedance (open-circuit) state. That is to say, any time CAS is at a high level, the DOUT pin will be floating. The only time the output will turn on and contain either a logic 0 or logic 1 is at access time during a read cycle. DOUT will remain valid from access time until CAS is taken back to the inactive (high level) condition.

If the memory cycle in progress is a read, read-modify write, or a delayed write cycle, then the data output will go from the high impedance state to the active condition, and at access time will contain the data read from the selected cell. This output data is the same polarity (not inverted) as the input data.

Once having gone active, the output remains valid until CAS is taken to the precharge (logic 1) state, whether or not RAS goes into precharge.

If the cycle in progress is an "early-write" cycle (WRITE active before CAS goes active), then the output pin will maintain the high impedance state throughout the entire cycle. Note that with this type of output configuration, the user is given full control of the DOUT pin simply by controlling the placement of WRITE command during a write cycle, and the pulse width of the Column Address Strobe during read operations. Note also that even though data is not latched at the output, data can remain valid from access time until the beginning of a subsequent cycle without paying any penalty in overall memory cycle time (stretching the cycle).

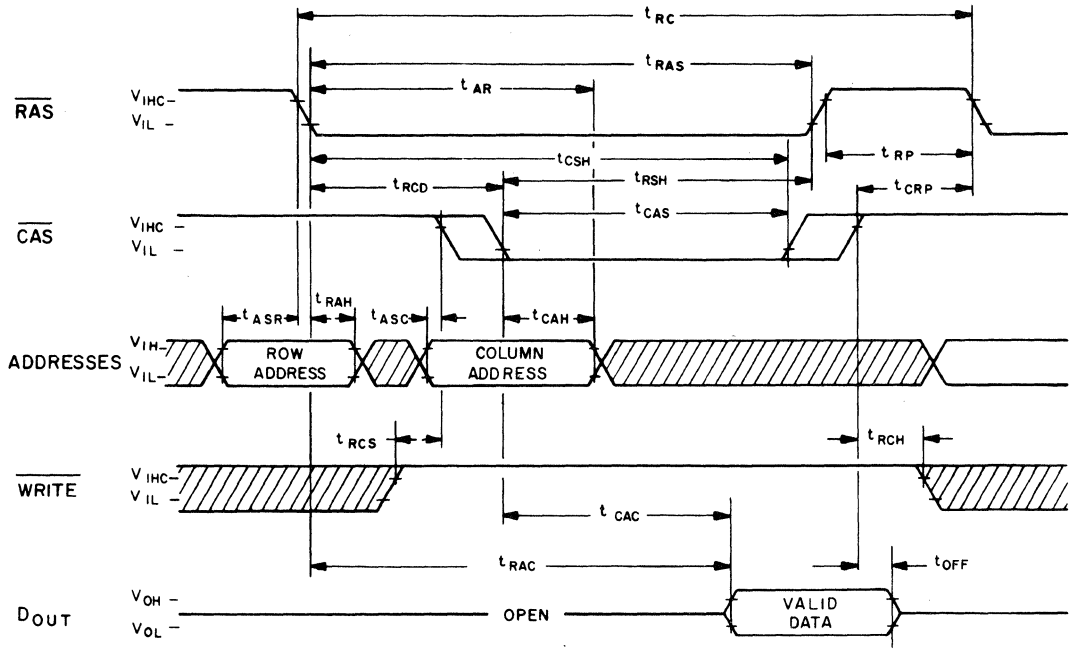
4.2.11.4 Refresh.

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 128 row addresses within each 2 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "RAS-only" cycles.

4.2.11.5 Timing.

Timing diagrams for the various cycles of operation are illustrated in Figure 4-14.

READ CYCLE



WRITE CYCLE (EARLY WRITE)

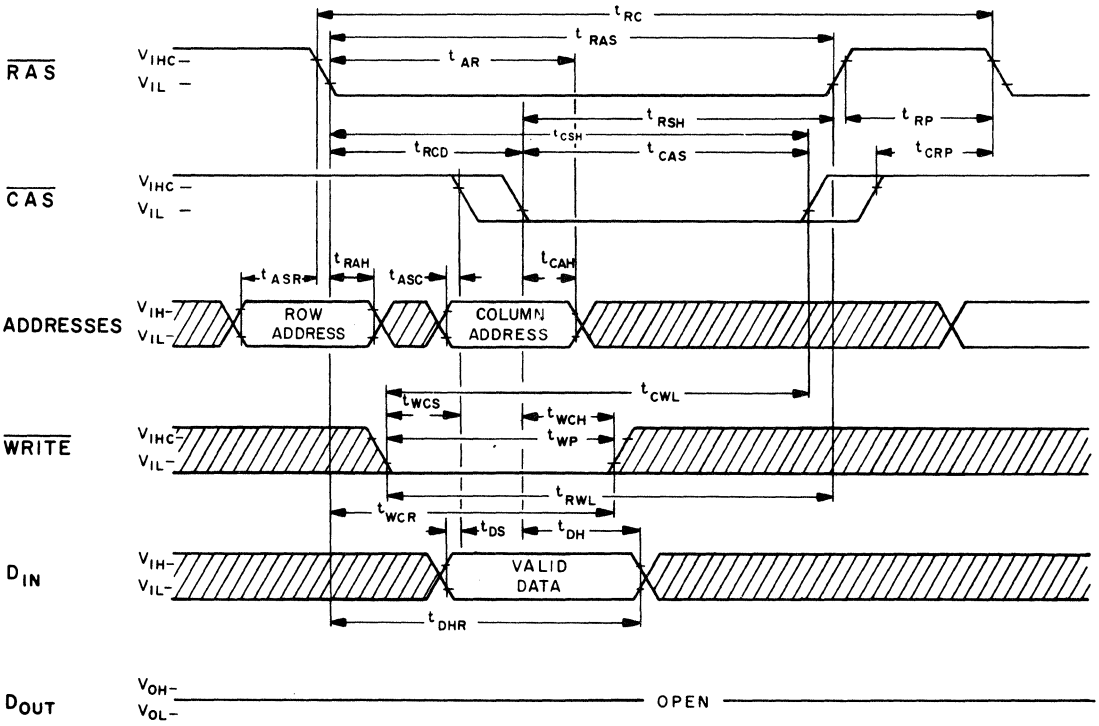
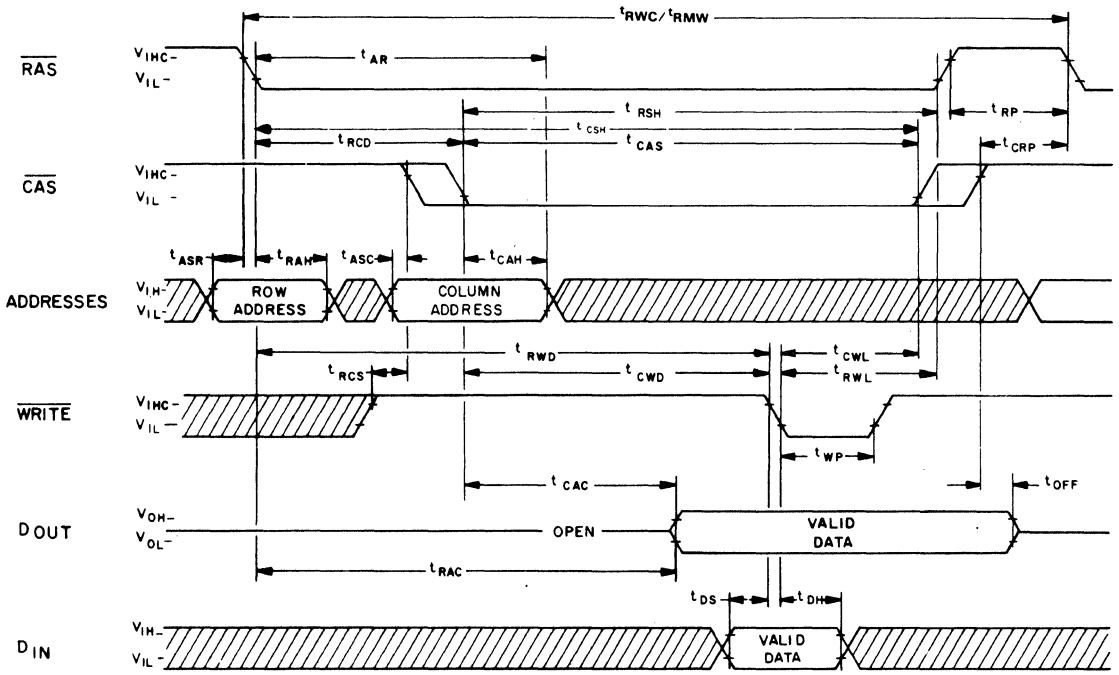


Figure 4-14. Dynamic RAM Timing (Sheet 1/2)

READ–WRITE/READ–MODIFY–WRITE CYCLE



"RAS–ONLY" REFRESH CYCLE

NOTE: CAS = V_{IHC}, WRITE = Don't Care

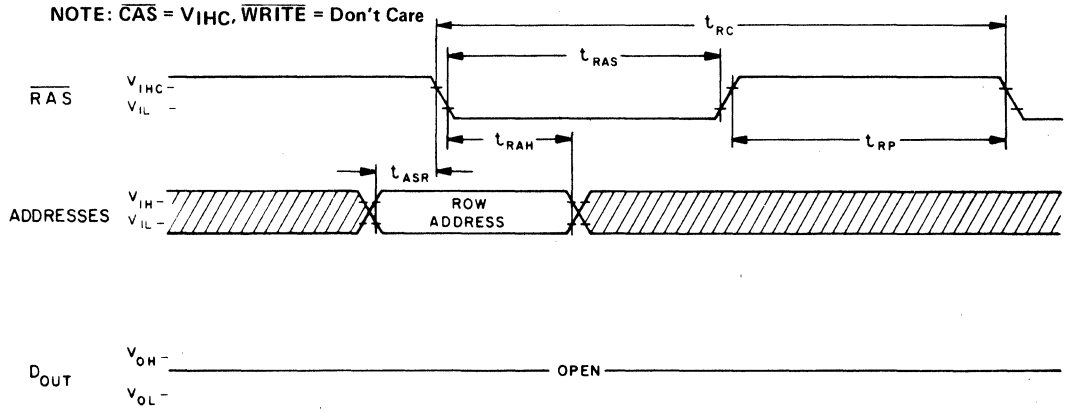


Figure 4-14. Dynamic RAM Timing (Sheet 2/2)

SECTION V

MAINTENANCE AND TROUBLESHOOTING

5.0 INTRODUCTION.

The AM-720 circuit board performs to full capability with a minimum of maintenance. This section describes maintenance and troubleshooting procedures and procedures for handling warranty returns.

5.1 CIRCUIT BOARD CHECKOUT.

The AM-720 circuit board was fully tested before it left Alpha Microsystems and will operate satisfactorily in the system if the hardware and software requirements of Sections 2 and 3 of this manual are met. Should a problem arise, use the following procedures to identify and locate the fault.

1. Check all cables for proper seating of connectors.

2. Check each of the wires at the cable connectors to ensure that each wire is properly seated in its groove.

3. Check the circuit boards for proper seating in the slot.

4. Check all power connections for correct voltages.

5. Check jumper options to ensure correctness of application. These are described in Section II of this manual.

Verify that the fault is in the AM-720 and not either in the system or in the peripherals. This can best be accomplished with substitution of a known good circuit board.

6. Perform the bank swapping scheme described in paragraph 2.3.2.1.

7. Perform the AM-720 diagnostic tests. Contact the Alpha Micro International Support/Services Group for information on diagnostic test availability.

5.2 WARRANTY PROCEDURES.

This circuit board is covered by warranty issued by Alpha Microsystems Inc., Irvine, California. Complete details of the warranty are included with the circuit board. Should a problem arise with this circuit board, call your dealer or the Alpha Micro International Support/Services Group for information.

Table 6-1. Component Cross-Reference List

REF DESIG	MFR TYPE NO.	PAR	REF DESIG	MFR TYPE NO.	PAR
U1	74LS244	4.2.5	U26	74S280	4.2.7
U2	74LS244	4.2.5	U27	4164	4.2.11
U3	74LS244	4.2.5	U28	4164	4.2.11
U4	74LS244	4.2.5	U29	4164	4.2.11
U5	74LS244	4.2.5	U30	4164	4.2.11
U6	74S280	4.2.7	U31	4164	4.2.11
U7	4164	4.2.11	U32	4164	4.2.11
U8	4164	4.2.11	U33	4164	4.2.11
U9	4164	4.2.11	U34	4164	4.2.11
U10	4164	4.2.11	U35	4164	4.2.11
U11	4164	4.2.11	U36	4164	4.2.11
U12	4164	4.2.11	U37	4164	4.2.11
U13	4164	4.2.11	U38	4164	4.2.11
U14	4164	4.2.11	U39	4164	4.2.11
U15	4164	4.2.11	U40	4164	4.2.11
U16	4164	4.2.11	U41	4164	4.2.11
U17	4164	4.2.11	U42	4164	4.2.11
U18	4164	4.2.11	U43	4164	4.2.11
U19	4164	4.2.11	U44	4164	4.2.11
U20	4164	4.2.11	U45	74S280	4.2.7
U21	4164	4.2.11	U46	74LS244	4.2.5
U22	4164	4.2.11	U47	4164	4.2.11
U23	4164	4.2.11	U48	4164	4.2.11
U24	4164	4.2.11	U49	4164	4.2.11
U25	74LS244	4.2.5	U50	4164	4.2.11

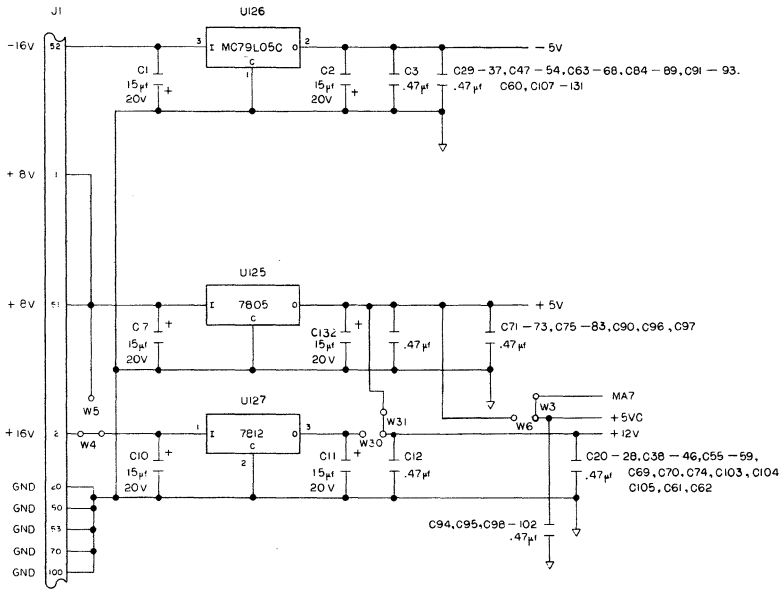
Table 6-1. (Con't) Component Cross-Reference List

REF DESIG	MFR TYPE NO.	PAR	REF DESIG	MFR TYPE NO.	PAR
U51	4164	4.2.11	U76	4164	4.2.11
U52	4164	4.2.11	U77	4164	4.2.11
U53	4164	4.2.11	U78	4164	4.2.11
U54	4164	4.2.11	U79	4164	4.2.11
U55	4164	4.2.11	U80	4164	4.2.11
U56	4164	4.2.11	U81	4164	4.2.11
U57	4164	4.2.11	U82	4164	4.2.11
U58	4164	4.2.11	U83	4164	4.2.11
U59	4164	4.2.11	U84	4164	4.2.11
U60	4164	4.2.11	U85	74S00	-
U61	4164	4.2.11	U86	74LS10	-
U62	4164	4.2.11	U87	74LS51	-
U63	4164	4.2.11	U88	74LS74	4.2.3
U64	4164	4.2.11	U89	74LS32	-
U65	74S280	4.2.7	U90	74S08	-
U66	NOT USED	-	U91	74LS74	4.2.3
U67	4164	4.2.11	U92	74LS74	4.2.3
U68	4164	4.2.11	U93	74LS20	-
U69	4164	4.2.11	U94	74LS38	-
U70	4164	4.2.11	U95	74LS74	4.2.3
U71	4164	4.2.11	U96	74LS175	4.2.4
U72	4164	4.2.11	U97	74LS123	4.2.2
U73	4164	4.2.11	U98	74S287	4.2.8
U74	4164	4.2.11	U99	74LS00	-
U75	4164	4.2.11	U100	74LS02	-

Table 6-1. (Con't) Component Cross-Reference List

REF DESIG	MFR TYPE NO.	PAR	REF DESIG	MFR TYPE NO.	PAR
U101	74LS04	-	U126	NOT USED	-
U102	74LS393	4.2.10	U127	NOT USED	-
U103	74S373	4.2.9	U128	NOT USED	-
U104	74S257	4.2.6			
U105	74S257	4.2.6			
U106	74LS244	4.2.5			
U107	74LS373	4.2.9			
U108	74LS373	4.2.9			
U109	74LS373	4.2.9			
U110	74LS10	-			
U111	74LS74	4.2.3			
U112	74LS240	-			
U113	25LS2521	4.2.1			
U114	74LS244	4.2.5			
U115	74LS244	4.2.5			
U116	25LS2521	4.2.1			
U117	74LS244	4.2.5			
U118	74LS244	4.2.5			
U119	74LS244	4.2.5			
U120	74LS244	4.2.5			
U121	74LS244	4.2.5			
U122	NOT USED	-			
U123	74LS14	-			
U124	26LS123	4.2.2			
U125	7805	-			

REVISIONS			
LTR	DATE	DESCRIPTION	APPR
A00		PROD. REL PER ENO0833	



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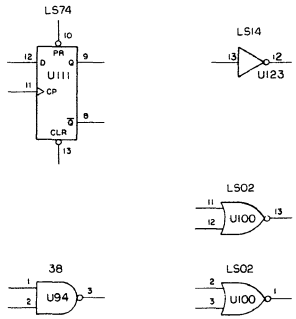


VCC AND GND. TABLE

VCC PIN NO.					GND.	I.C. NO.
+5V	+12V	-5V				
14					7	U6.26.45.65.85.86.87.88.89.90.91.92.93.94.95.99.
						U100.101.102.110.111.123
16					8	U96.97.98.104.105.124
20					10	U1.2.3.4.5.25.46.103.106.107.108.109.112.113.114.115.116.
						U117.118.119.120.121.122
9	8	1			16	U7-U24, U27-U44, U47-U64, U67-U84

REF. DES. LAST USED	REF. DES. NOT USED
U127, R42 C131, DS1 RN2, J2 W25	U66, U122 R30 THRU R32, R34 THRU R37, R40, W12 THRU W14 C8, 9, 17, 4, 5, C106.

4. FOR DWE-00710-04 CUT ETCH W20, W21, W6 THEN JUMPER A, E, W3.
3. U7-U24, U27-U44, U47-U64, U67-U84, ARE ICM-04116-02.
2. CAPACITOR VALUES ARE IN MICROFARADS ± 20%, 50V.
1. RESISTOR VALUES ARE IN OHMS, ± 5%, ¼W.

NOTE: UNLESS OTHERWISE SPECIFIED

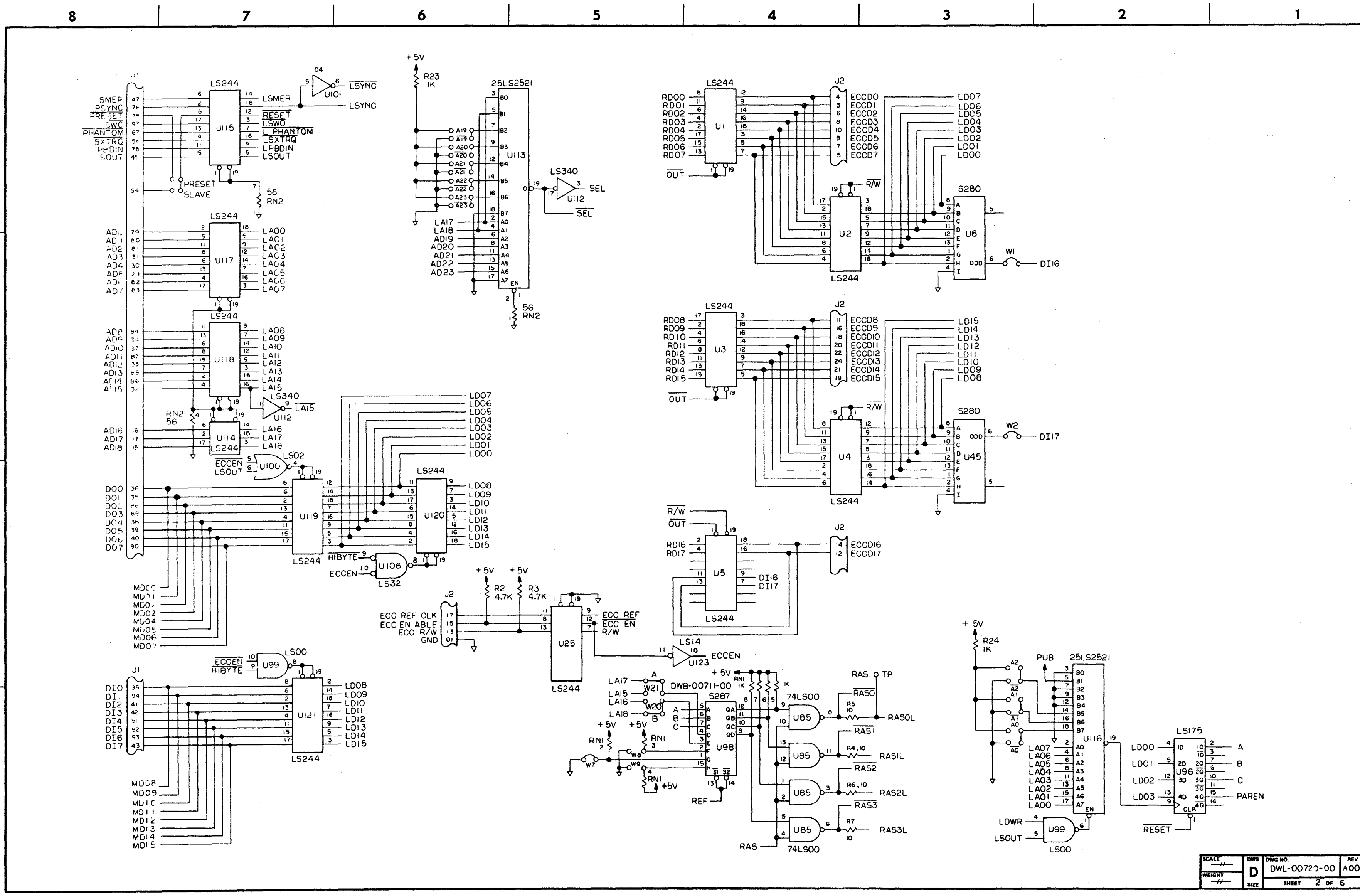
DO NOT SCALE DWG
ALL DIMS IN INCHES
TOLERANCES
X ± .1
.XX ± .03
.XXX ± .010
ANGLES ± 2°
SURFACE ✓
UNLESS OTHERWISE SPECIFIED
NEXT ASSY | USED ON
APPLICATION

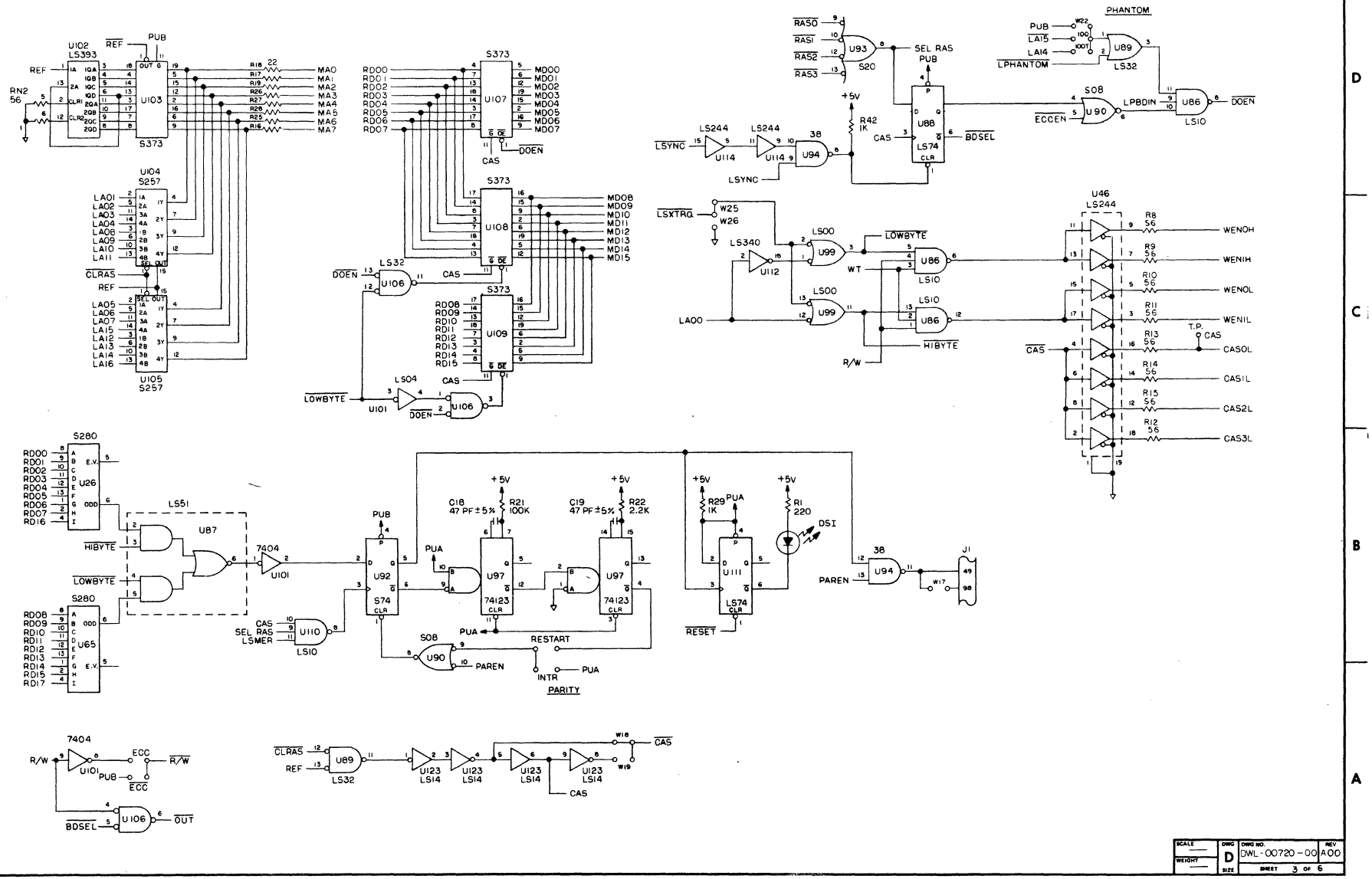
DWN Charles Nelson 6-26-81
CHK R Bailey 7-15-81
ENG
APPD
APPD

alpha micro
IRVINE, CA. 92713

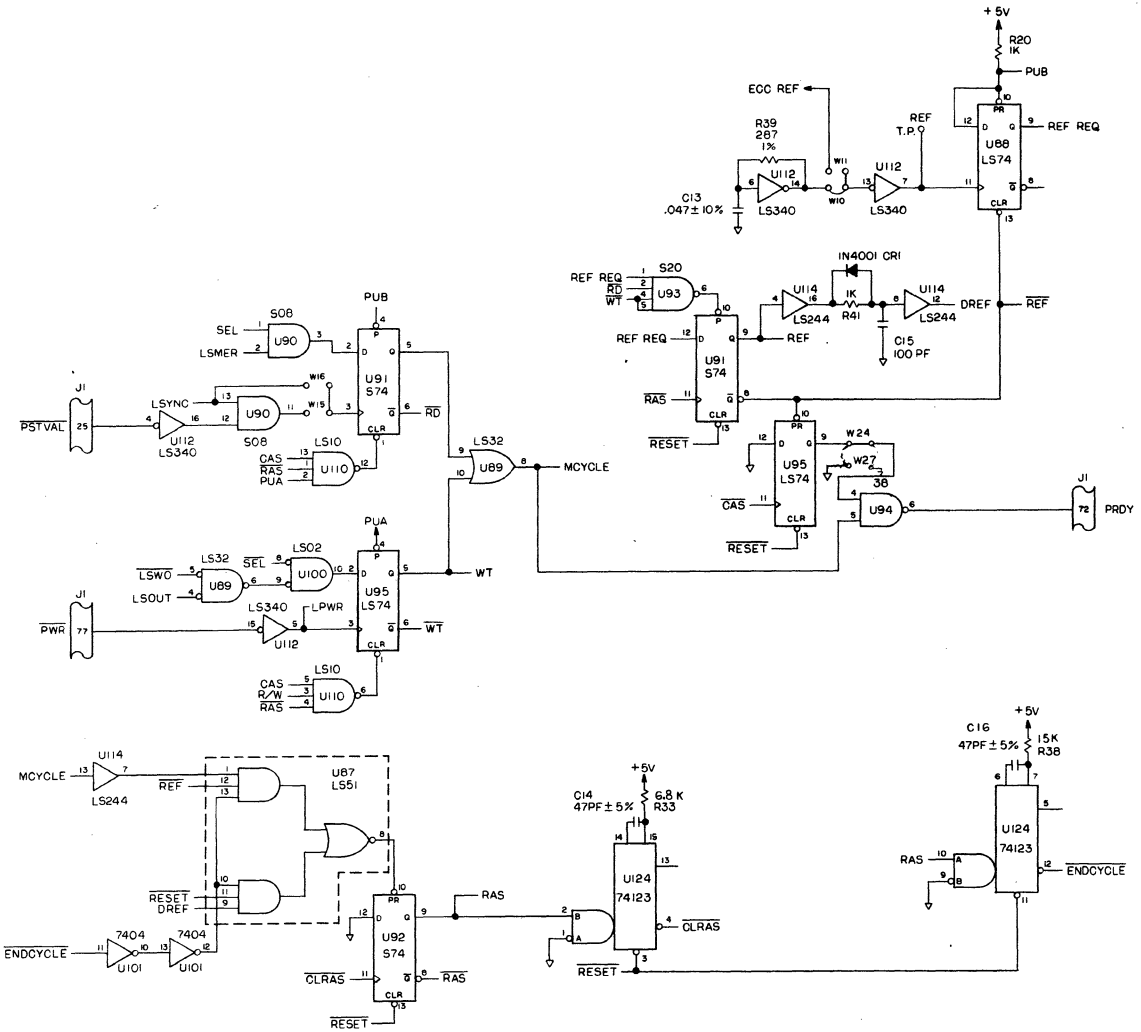
TITLE
LOGIC, MEMORY, BOARD
AM-720

SCALE —
WEIGHT —
SIZE D
DWG NO. DWL-00720-00
REV A00
SHEET 1 OF 6

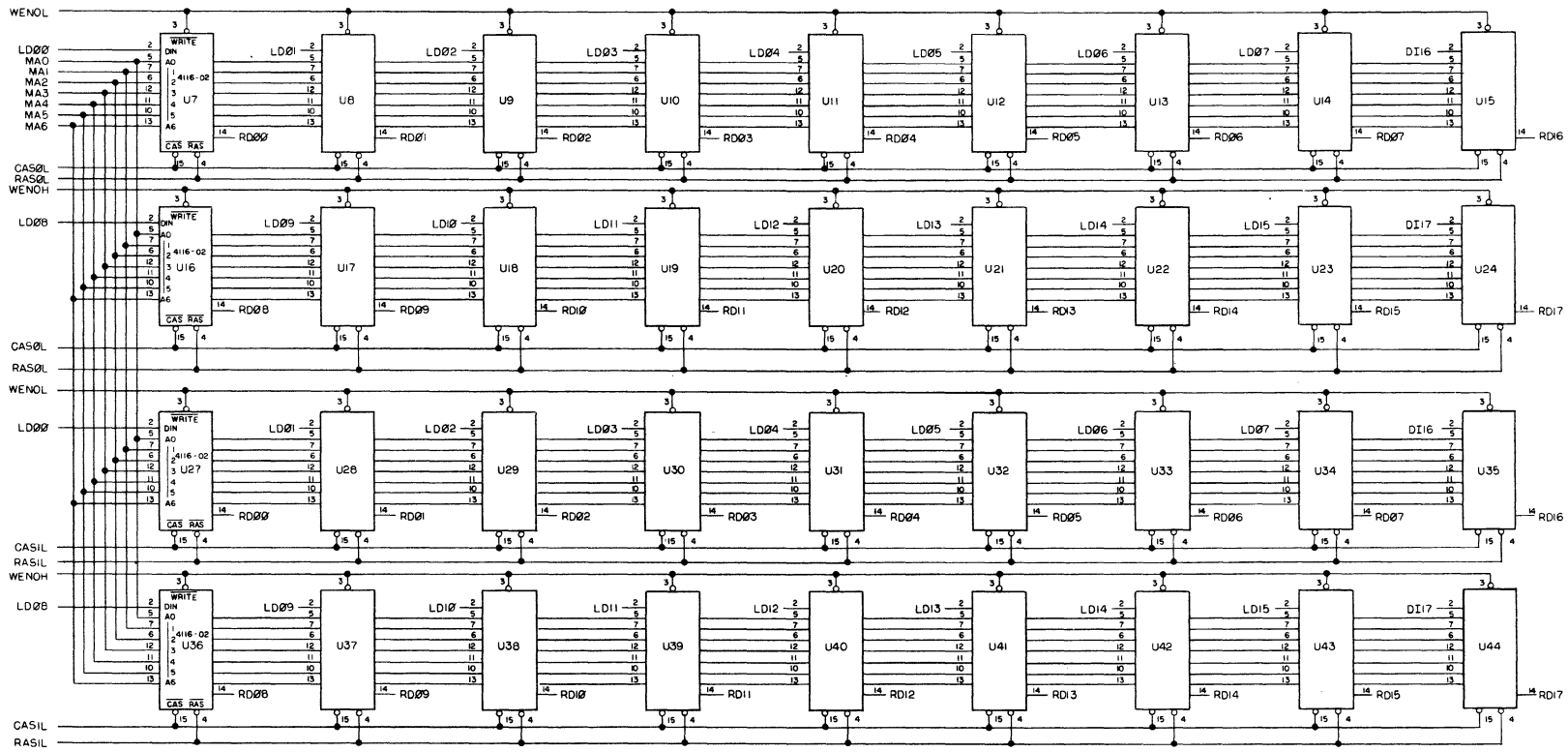

8
7
6
5
4
3
2
1
D
C
B
A
LS244
U115
SMER
PSYNC
PRESET
SWC
PHANTOM
SXTRQ
PBDIN
SOUT
LSMER
RESET
LSWO
L PHANTOM
LSXTRQ
LPBDIN
LSOUT
U101
LSYNC
PRESET
SLAVE
56
RN2
U117
LA00
LA01
LA02
LA03
LA04
LA05
LA06
LA07
U118
LA08
LA09
LA10
LA11
LA12
LA13
LA14
LA15
LS340
U112
RN2
56
U114
LS244
LA16
LA17
LA18
AD16
AD17
AD18
ECCEN
LSOUT
LS02
U100
DO0
DO1
DO2
DO3
DO4
DO5
DO6
DO7
U119
U120
LD00
LD01
LD02
LD03
LD04
LD05
LD06
LD07
LD08
LD09
LD10
LD11
LD12
LD13
LD14
LD15
HIBYTE
ECCEN
U106
LS32
MD00
MD01
MD02
MD03
MD04
MD05
MD06
MD07
U99
LS00
J1
DI0
DI1
DI2
DI3
DI4
DI5
DI6
DI7
U121
MD08
MD09
MD10
MD11
MD12
MD13
MD14
MD15
+5V
R23
1K
25LS2521
U113
A19
A20
A21
A22
A23
LA17
LA18
AD19
AD20
AD21
AD22
AD23
EN
RN2
LS340
SEL
U112
J2
ECC REF CLK
ECC EN ABLE
ECC R/W
GND
R2
4.7K
R3
4.7K
U25
ECC REF
ECC EN
R/W
LS14
U123
ECCEN
RD00
RD01
RD02
RD03
RD04
RD05
RD06
RD07
U1
OUT
ECCD0
ECCD1
ECCD2
ECCD3
ECCD4
ECCD5
ECCD6
ECCD7
U2
S280
U6
ODD
W1
DI16
RD08
RD09
RD10
RD11
RD12
RD13
RD14
RD15
U3
ECCD8
ECCD9
ECCD10
ECCD11
ECCD12
ECCD13
ECCD14
ECCD15
U4
U45
W2
DI17
RD16
RD17
U5
ECCD16
ECCD17
LAI7
LAI5
LAI6
LAI8
W21
W20
DWB-00711-00
S287
U98
RN1
1K
74LS00
U85
RAS
TP
RAS0
RAS0L
RAS1
RAS1L
RAS2
RAS2L
RAS3
RAS3L
R5
R4
R6
R7
10
W7
W8
W9
REF
+ 5V
R24
1K
PUB
25LS2521
U116
LA07
LA06
LA05
LA04
LA03
LA02
LA01
LA00
LDWR
LSOUT
U99
LS00
LS175
U96
CLR
A
B
C
PAREN
RESET
DWL-00720-00
REV
A00
SHEET 2 OF 6
SCALE
WEIGHT
SIZE
D



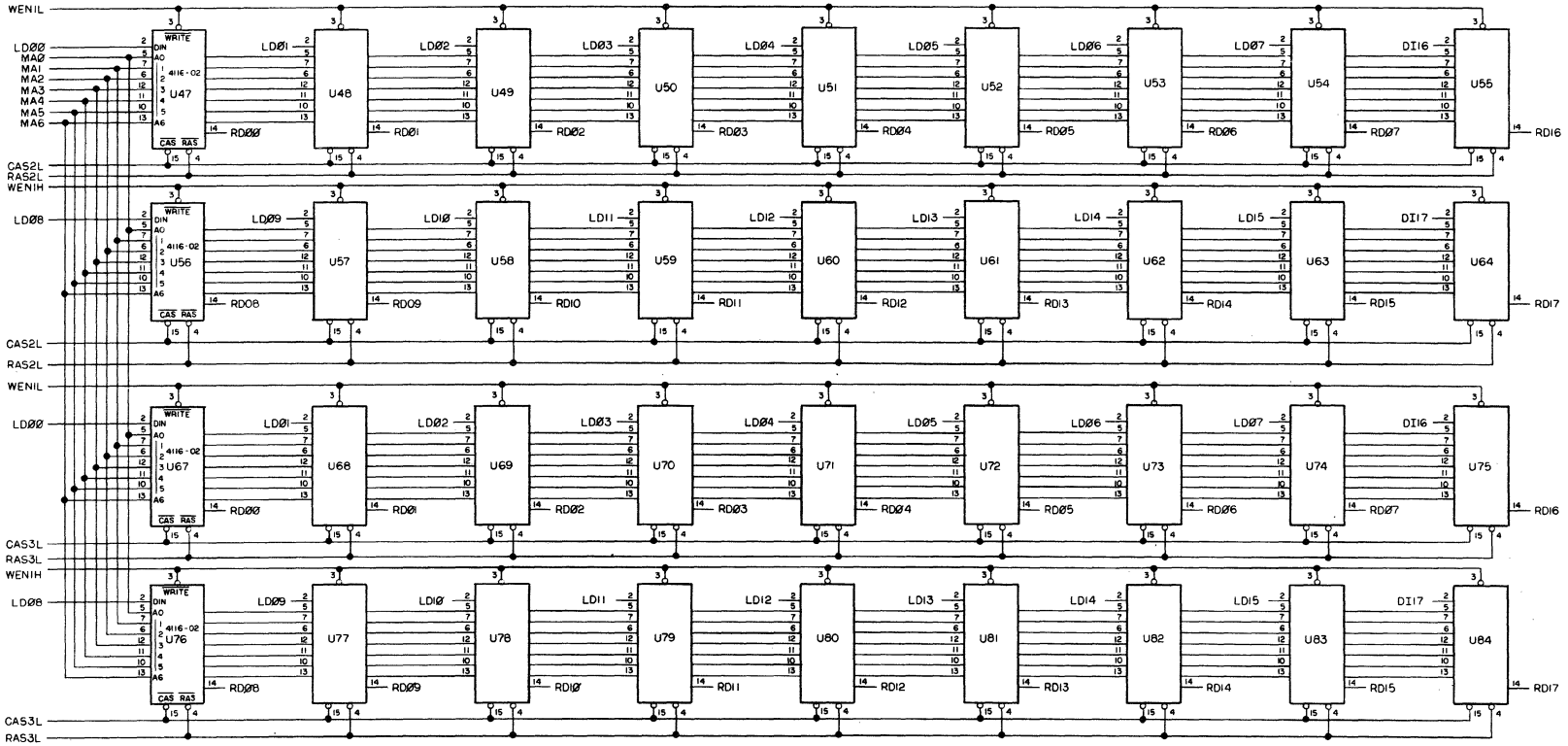
SCALE		DWG SIZE	DWG NO.	REV
WEIGHT		D	DWL-00720-00	A00
			SHEET 3 OF 6	



SCALE	DWG	DWG NO.	REV
WEIGHT	D	DWL-00720-00	A00
SIZE		SHEET 4 OF 6	



SCALE	DWG	DWG NO.	REV
WEIGHT	D	DWL-00720-00	A00
	SIZE	SHEET 5 OF 6	



SCALE	DWG	DWG NO.	REV
WEIGHT	D	DWL-00720-00	A00
	SIZE	SHEET 6 OF 6	

.....ASSEMBLY..... NUMBER	DESCRIPTION	REC#	.....COMPONENT..... NUMBER	DESCRIPTION	ASSY. BIN#	QUANTITY
DWB0072000	ASSY MEMORY BOARD .5 MB	A00				
		00001	DWF0072000	PCB DETAIL MEMORY BOARD .5 MB		1.000
		00002	CNA0009600	CONN RECEPTACLE SHORTING 2CONT BLK		17.000
		00003	CNF0003600	HEADER STRIP LINE PLUG		7.000
		00004	CNF0003800	HEADER STRIP LINE PLUG MALE		2.000
		00005	CNF0003510	ASSIGNED		1.000
		00006	CNF0003302	HEADER STRIP LINE PLUG MALE		4.000
		00008	HDS1050606	SCREW,PHMS,SS,PH RECESS, 6-32X3/8		2.000
		00009	HDN1000006	NUT HEX 6-32 KEP INT/EXT CAD STL		2.000
		00011	ICL0780501	VOLTAGE REGULATER +5V, 5 AMP, TO-3		1.000
		00014	CNF0000601	HEADER 26PIN W/O EJCT RT ANGLE UL		1.000
		00015	HDM0001200	THERMAL GREASE		0.000
		00017	CNF0003303	HEADER STRIP LINE PLUG MALE		1.000
		00018	IC10740001	IC QUAD 2 INPUT NAND GATE		2.000
		00019	IC10740201	IC QUAD 2 INPUT NOR GATE		1.000
		00020	IC10740400	IC HEX INVERTER		1.000
		00021	IC10740802	IC QUAD 2 INPUT AND GATE		1.000
		00022	IC10741001	IC TRIPLE 3 INPUT NAND GATE		2.000
		00023	IC10743201	IC QUAD 2 INPUT OR GATE		2.000
		00025	IC10743800	IC QUAD 2 INPUT NAND DRIVER OC		1.000
		00026	IC10745101	IC 74LS51 AND-OR-INVERT GATES		1.000
		00027	IC10747401	IC DUAL D FLIPFLOP		3.000
		00028	IC10747402	IC DUAL D FLIPFLOP		2.000
		00029	IC10741401	IC HEX INVERTER W/HYSTERESIS		1.000
		00030	IC17412300	IC, DUAL ONE SHOT		2.000
		00031	IC17417501	IC QUAD D FLIPFLOP		1.000
		00032	IC17424401	IC OCTAL BUS DRIVER NONINVERT		14.000
		00033	IC17425702	QUAD DATA SELECTOR 74S257		2.000
		00034	IC17428002	IC 9 BIT ODD/EVEN PARITY GENERATOR		4.000
		00035	DWB0071100	PROM ASSY, 256 X 4 (ADDR DECODER)		1.000
		00037	IC17439301	IC DUAL 4 BIT BINARY COUNTER		1.000
		00038	IC10252101	IC 8 BIT COMPARATOR		2.000
		00039	ICM0416400	IC, RAM 64K X 1 150ns DYNAMIC		72.000
		00040	CPP0015601	CAPACITOR 15 UF 20V		2.000
		00041	CPN0047401	CAPACITOR .47 UF		46.000
		00042	RS20010200	RESISTOR 1 K 1/4W 5% CAR		6.000
		00043	RS20022100	RESISTOR 220 OHM 1/4W 5% CAR		1.000
		00044	RS20047200	RESISTOR 4.7 K 1/4W 5% CAR		2.000
		00045	RSN0000800	RESISTOR NETWORK, 8 PIN SIP, 1K		1.000
		00046	RSN0001100	RESISTOR NETWORK, 8 PIN SIP, 56 OHM		1.000
		00047	RS20015300	RESISTOR 15K 1/4W 5% CAR		1.000
		00048	RS20010400	RESISTOR 100K 1/4W 5% CAR		1.000
		00049	RS20022200	RESISTOR 2.2 K 1/4W 5% CAR		1.000
		00050	RS20056000	RESISTOR, 56 OHMS 1/4W 5%		8.000
		00052	RS20068200	RESISOR 6.8K 1/4 W 5% CARBON		1.000
		00053	DI00400100	DIODE		1.000
		00054	IC17434001	IC,SCHMITT TRIGGER OCTAL DRIVER		1.000
		00055	IC10742002	IC DUAL 4 INPUT NAND GATE		1.000
		00056	CPN0047000	5% CAPACITOR 47pF (DIPPED MICA)		4.000
		00057	CPN0047301	CAPACITOR .047UF		1.000

.....ASSEMBLY..... NUMBER	DESCRIPTION	.....COMPONENT..... REC#	NUMBER	DESCRIPTION	ASSY. BIN#	QUANTITY
		00058	DID0000100	LED		1.000
		00059	RS20010000	RESISTOR 10 OHM 1/4W 5% CAR		4.000
		00060	IC17437302	IC OCTAL D FLIPFLOP		4.000
		00061	RS20287000	RESISTOR, 287 OHMS 1% 1/4 W		1.000
		00063	CPN0010101	CAPACITOR 100 PF		1.000
		00064	RS20022000	RESISTOR 22 OHM 1/4W 5% CAR		8.000
		00065	LBL0001829	LABEL, PCB SERIAL I.D. AM-720		1.000
		00066	HDM0002100	HEAT SINK 1.4 WI .5 HT 1.880L		1.000
		00067	HDW1000406	NYLON SHOULDER WASHER #6		2.000
		00068	CNF0003301	HEADER, MALE, SINGLE POST		1.000

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