TECHNICAL MANUAL

AM-420

DISK DRIVE CONTROLLER CIRCUIT BOARD

DWM-00420-00

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alpha micro

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GENERAL DESCRIPTION

1.0 INTRODUCTION

This manual provides operating and maintenance instructions for the AM-420 Winchester Disk Drive Controller circuit board manufactured by Alpha Microsystems Inc., located in Irvine, California. Circuit board description, operating and usage instructions, programming, theory of operation, and maintenance instructions are included to provide the user with the information necessary to utilize this circuit board to its full capability.

1.1 CIRCUIT BOARD DESCRIPTION

The AM-420 Wincheter Disk Drive Controller circuit board provides data processing, control and interface capability between a standard S-100 Bus system and one to four PRIAM Winchester hard disk drives. A CPU microprocessor, a DMA address generator, a Random Access Memory (RAM) with associated control logic provide the sophisticated data processing necessary for control of up to four PRIAM Winchester disk drives. A 2K Read Only Memory (ROM) is contained on the board to provide a bootstrap load program and also to contain the microcode necessary for the CPU module operation.

A simplified block diagram of the circuit board is shown in Figure 1-1. For a complete detailed description of circuit board operation, see Section IV of this manual. For programming requirements, see Section III of this manual.

1.2 APPLICATION

This circuit board provides the data processing and interface capability necessary for operation of up to four PRIAM Winchester hard disk drives. Data is transferred at an average rate of 8 MHz between the controller and drives. See Section II of this manual for wiring instructions and system interface information. For complete information on the disk drive, see the appropriate PRIAM Hardware Maintenance Manual.

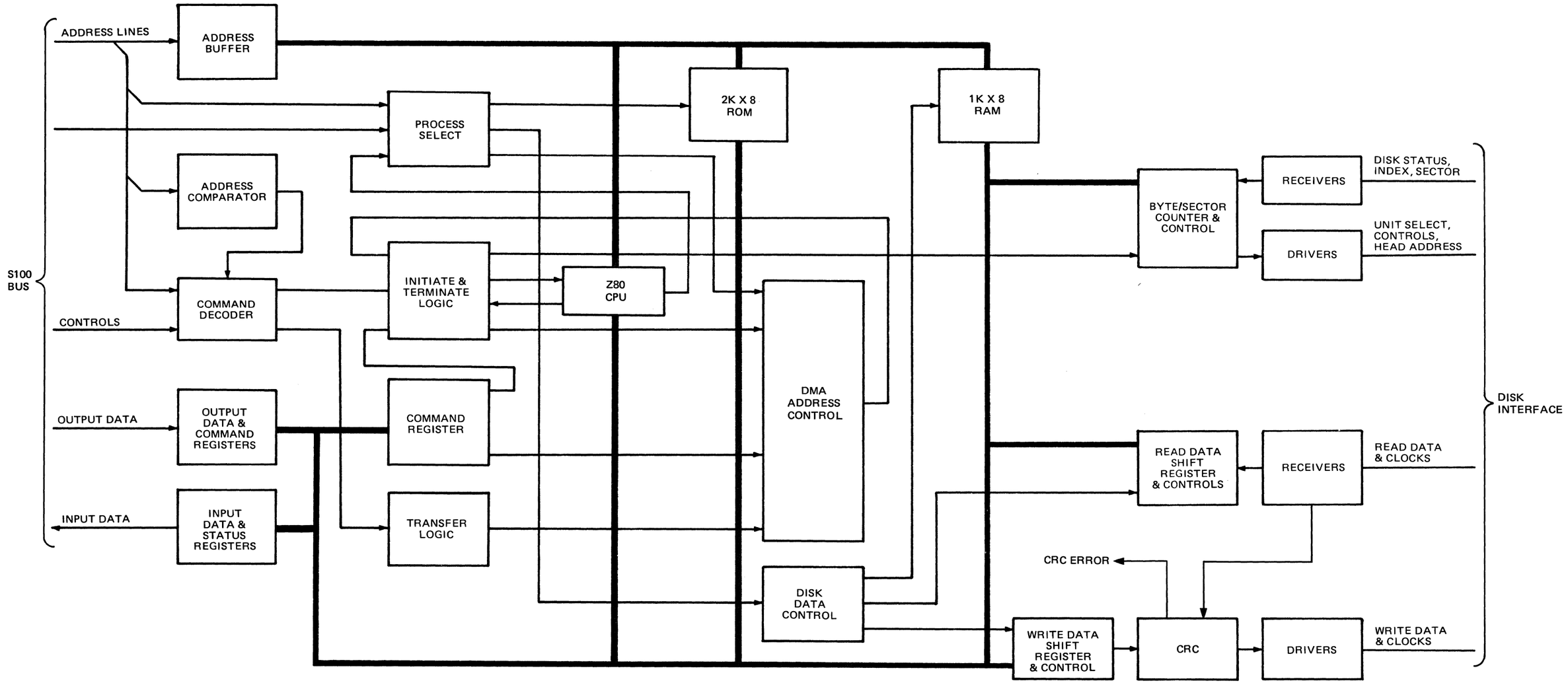


Figure 1-1. AM-420 Simplified Block Diagram

SECTION II
OPERATING DATA

2.0 INTRODUCTION

This section contains information on the use of the AM-420 Disk Controller circuit board. Capabilities, specifications, interface wiring, and user option descriptions are provided for the successful integration of the AM-420 into the user's system.

2.1 CAPABILITIES AND SPECIFICATIONS

This circuit board operates from the standard S-100 Bus structure to interface with the PRIAM Winchester hard disk drive. The board can interface with up to four disk drives. Detailed specifications are contained in Table 2-1.

Table 2-1. AM-420 Specifications

PARAMETER	SPECIFICATIONS
CPU Interface	Standard S-100 Bus
Drives per Controller	1-4
Printed Circuit Boards	1
Data Transfer Modes	Programmed Multi-Level Interrupts, Full Sector Block Transfers.
Data Transfer - Controller to Disk	Serial
Data Transfer - Controller to Computer	8-bit bytes Parallel
Data Transfer Format	512 bytes per sector, plus CRC and sentinel check bytes.
On-Board Buffer	1024 bytes
Error Checking	CRC Error Code
Input Power	+8 volts DC @2.0 amps
Interconnections	One mounting slot of an S-100 Bus chassis. One 50-pin cable to first drive (25 feet maximum cumulative length on four drives).
Dimensions	9" x 10"

Table 2-1 (Con't). AM-420 Specifications

PARAMETER	SPECIFICATIONS
Environment (operating)	
Temperature	60° to 104° F (15° to 40°C)
Humidity	10% to 80% (non-condensing)

2.2 INSTALLATION AND START-UP

When the AM-420 circuit board is received, it is ready for use. No adjustment or calibration is required for operation. The hardware requirements for installation and use are described in this section and the software requirements are described in Section III.

2.2.1 Installation

First ensure that the proper power wiring is available and that the correct voltages are connected to the disk drive and to the various pins of the circuit board as shown in Table 2-2. Connect the cables to the disk drives as shown in Figure 2-1.

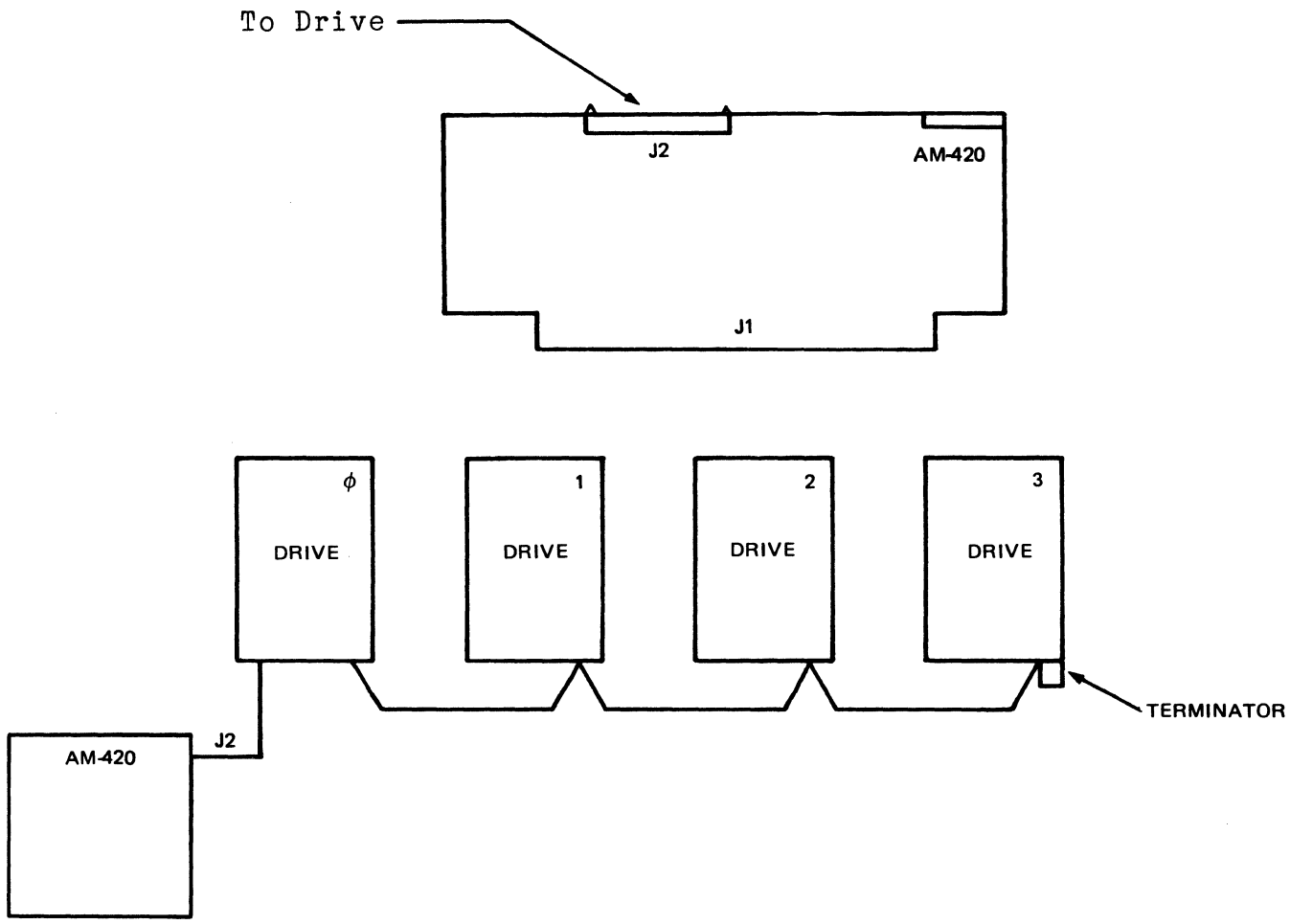


Figure 2-1. Disk Drive Interface Cabling

Table 2-2. Alpha Micro Bus Interface Signals List

MNEMONIC	NAME	PIN NO.
+7.5V	+ 7.5vdc Power	1
+16V	+ 16vdc Power	2
$\overline{\text{VI8}}$	Vectored Interrupt 8	3
$\overline{\text{VI0}}$	Vectored Interrupt 0	4
$\overline{\text{VI1}}$	Vectored Interrupt 1	5
$\overline{\text{VI2}}$	Vectored Interrupt 2	6
$\overline{\text{VI3}}$	Vectored Interrupt 3	7
$\overline{\text{VI4}}$	Vectored Interrupt 4	8
$\overline{\text{VI5}}$	Vectored Interrupt 5	9
$\overline{\text{VI6}}$	Vectored Interrupt 6	10
$\overline{\text{VI7}}$	Vectored Interrupt 7	11
RTC	Real Time Clock, 50Hz or 60Hz	12
POWFAIL	AC Power Failure Status	13
$\overline{\text{VI9}}$	Vectored Interrupt 9	14
A18	Address 18	15
A16	Address 16	16
A17	Address 17	17
$\overline{\text{STATDSB}}$	Status Disable	18
$\overline{\text{C/CDSB}}$	Command/Control Disable	19
GND	Ground	20

Table 2-2.(con't) Alpha Micro Bus Interface Signals List

MNEMONIC	NAME	PIN NO.
$\overline{\text{IODIS}}$	I/O Disable	21
$\overline{\text{ADDDSB}}$	Address Disable	22
$\overline{\text{DODSB}}$	Data Bus Disable	23
Ø2	Phase 2 Clock	24
$\overline{\text{STVAL}}$	Status and Address Valid	25
PHLDA	DMA Request Acknowledge	26
PWAIT	Processor Wait	27
N/U	Not Used	28
A5	Address 5	29
A4	Address 4	30
A3	Address 3	31
A15	Address 15	32
A12	Address 12	33
A9	Address 9	34
DOUT 1/D1	Data Bus Bit 1	35
DOUT 0/D0	Data Bus Bit 0	36
A10	Address 10	37

Table 2-2.(con't) Alpha Micro Bus Interface Signals List

MNEMONIC	NAME	PIN NO.
DOUT 4/D4	Data Bus Bit 4	38
DOUT 5/D5	Data Bus Bit 5	39
DOUT 6/D6	Data Bus Bit 6	40
DIN 2/D10	Data Bus Bit 10	41
DIN 3/D11	Data Bus Bit 11	42
DIN 7/D15	Data Bus Bit 15	43
SMI	Bus Master OP Code Fetch	44
SOUT	I/O Output Cycle	45
SINP	I/O Input Cycle	46
SMEMR	Memory Read Cycle	47
SHLTA	HLT Acknowledge	48
$\overline{\text{PERR}}$	Parity Error Pulse	49
GND	Ground	50
+7.5V	+7.5vdc Power	51
-16V	-16vdc Power	52
GND	Ground	53
$\overline{\text{SLAVECLR}}$	Reset Signal To All I/O Devices	54

Table 2-2.(con't) Alpha Micro Bus Interface Signals List

MNEMONIC	NAME	PIN NO.
$\overline{\text{DMA0}}$	DMA Controller Arbitration	55
$\overline{\text{DMA1}}$	Lines For Use With Standard	56
$\overline{\text{DMA2}}$	S-100 Bus DMA System	57
$\overline{\text{SXTRQ}}$	16 Bit Cycle	58
A19	Address 19	59
N/U	Not Used	60
A20 A21 A22 A23	Address 20 Address 21 Address 22 Address 23	61 62 63 64
$\overline{\text{ADVAL}}$	Address Valid On Data Bus	65
$\overline{\text{WRDIS}}$	Write Disable	66
$\overline{\text{PHANTOM}}$	ROM Memory Enable	67
N/U N/U	Not Used Not Used	68 69
Gnd	Ground	70
N/U	Not Used	71
PRDY	Processor Ready	72

Table 2-2.(con't) Alpha Micro Bus Interface Signals List

MNEMONIC	NAME	PIN NO.
N/U	Not Used	73
$\overline{\text{PHOLD}}$	DMA Request	74
$\overline{\text{PRESET}}$	Preset	75
PSYNC	Processor Sync, Start of Bus Cycle	76
$\overline{\text{PWR}}$	Write Strobe	77
PDBIN	Data Bus Input Command	78
A0	Address 0	79
A1	Address 1	80
A2	Address 2	81
A6	Address 6	82
A7	Address 7	83
A8	Address 8	84
A13	Address 13	85
A14	Address 14	86
A11	Address 11	87
DOUT 2/D2	Data Bus Bit 2	88
DOUT 3/D3	Data Bus Bit 3	89
DOUT 7/D7	Data Bus Bit 7	90
DIN 4/D12	Data Bus Bit 7	91
DIN 5/D13	Data Bus Bit 13	92
DIN 6/D14	Data Bus Bit 14	93
DIN 1/D9	Data Bus Bit 9	94
DIN 0/D8	Data Bus Bit 8	95

Table 2-2.(con't) Alpha Micro Bus Interface Signals List

MNEMONIC	NAME	PIN NO.
SINTA	Interrupt Acknowledge	96
$\overline{\text{SWO}}$	Bus Master Output	97
$\overline{\text{ERROR}}$	Memory Error Interrupt	98
$\overline{\text{BERR}}$	Bus Error	99
GND	Ground	100

2.3 INTERFACE DESCRIPTION

The AM-420 Disk Controller Circuit board provides interface capability between the standard S-100 Bus and the PRIAM Winchester disk drives.

2.3.1 S-100 Bus Interface

The AM-420 circuit board is fully S-100 Bus compatible. The board and its associated disk drives are addressed through the address lines and data is transferred through the standard data-in and data-out ports. The S-100 bus connections are made via the bottom edge connector and are listed in Table 2-2. For a complete description of these signals and their operation in the AM-420, see Section IV of this manual.

2.3.2 Disk Drive Interface

One AM-420 Circuit Board accommodates a maximum of four PRIAM disk drives. Interface connections are made through one cable connecting to all four drives in a daisy-chain (50 pin ribbon cable). Pin 1 on the daisy chain cable is identified by a stripe wire along one edge. Connect pin 1 of the cable to pin 1 of the connector on both the drive and the AM-420. Terminate only the last drive in sequence on the daisy-chain cable using the terminator card provided with the drive.

Interface cabling is shown in Figure 2-1. For further information on operation of the AM-420 interface, see Section IV of this manual.

2.4 USER OPTIONS

Some features of the AM-420 can be changed by selection of jumpers at the user's option. Location of the jumper pads is shown in Figure 2-2.

2.4.1 Address Code

Circuit board addressing can be selected at the user's option for any address block (in increments of four) on the address lines AD2-AD7. The standard address (C4 Hex) is contained in etch when the circuit board is manufactured. To change the address, cut the desired etch and leave open for pull up, jumper or ground to generate the desired board address.

2.4.2 Interrupt Lines

Interrupt compatibility for any S-100 bus system is provided with jumpers to any of the vectored interrupt lines VI0-VI7. Attach the jumper wire from the pad located as shown in Figure 2-2 to the desired interrupt line. The standard interrupt line is VI5 which is contained in etch. Cut this jumper to change the interrupt.

2.4.3 Boot Option

The AM-420 contains a bootstrap loader program contained in an internal PROM that the user may utilize. If the user decides to boot from another source, the boot feature must be disabled with a jumper block as shown in Figure 2-2. When using the AM-420 with the AM-100/T CPU, always disable the boot feature. Various boot PROM's exist to allow booting from various backup devices. Consult the Alpha Micro International Support/Services Group for additional details.

2.4.4 AM-100 Preparation

If the Alpha Micro AM-100 CPU is used in the system, the interrupt jumper must be added on the CPU board at VI5 for compatibility with the AM-420.

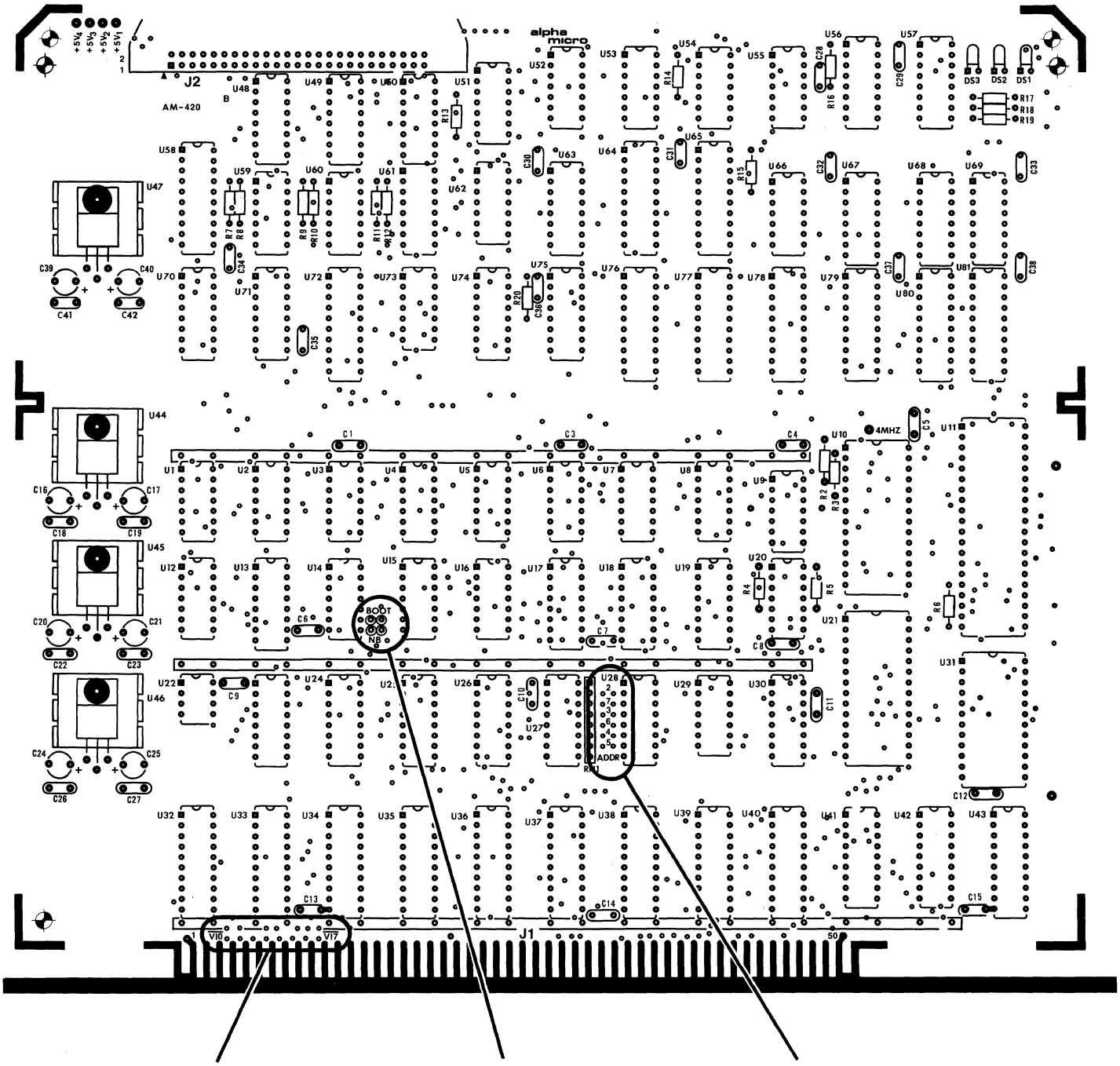


Figure 2-2. Jumper Options

SECTION III
PROGRAMMING

3.0 INTRODUCTION

This section describes the programming requirements for the AM-420 circuit board. Circuit board addressing, bootstrap loader, and AM-420 internal programming are described for complete system compatibility.

When the AM-420 circuit board is received, it is ready for use with the PRIAM disk drive as described in Section II of this manual. The bootstrap loader and the microcode contained in internal firmware is designed only for these disk drives.

3.1 UNIQUE SOFTWARE CONSIDERATIONS

One of the most important differences between the Winchester drives and lower capacity conventional drives is that the software must accept media flaws. The track and bit densities are so great with these high capacity memory disks that it is impossible to manufacture platters with no media flaws. Therefore, software consideration is made for these faulty blocks.

The technique used to detect and flag these tracks writes to and reads from every track and flags any tracks that are faulty. To accommodate this technique, a new program called "CRT420" is included. New versions of old programs have also been included.

3.2 ADDRESSING

The AM-420 and associated disk drives are addressed through the S-100 bus address lines. The circuit board address is jumper selectable by the jumpers connected to U27. Pull-ups to either +5V or ground jumpers select the board address on S-100 bus address lines AD2-AD7. Address C4 (Hex) is etched in the board to occupy I/O ports C4 and C5 (Hex).

3.3 INITIALIZATION

On initial power-up or reset, the AM-420 goes into a dormant state waiting for initialization. With the boot option enabled, the phantom signal is activated, disabling any phantom controlled memory. The S-100 bus is enabled to access the bootstrap loader contained in the AM-420 PROM.

The 2K x 8 EPROM (U31) contains both the bootstrap routine and the controller microcode. The microcode resides in the first 1K bytes, and the bootstrap routine resides in the second 1K bytes of this PROM. The current bootstrap routine is written in AM-100 code. However, other user codes may be used.

> NOTE: If the user code contained in the AM-420 EPROM is changed from the current boot routine, the microcode in the first 1K of memory must be duplicated exactly.

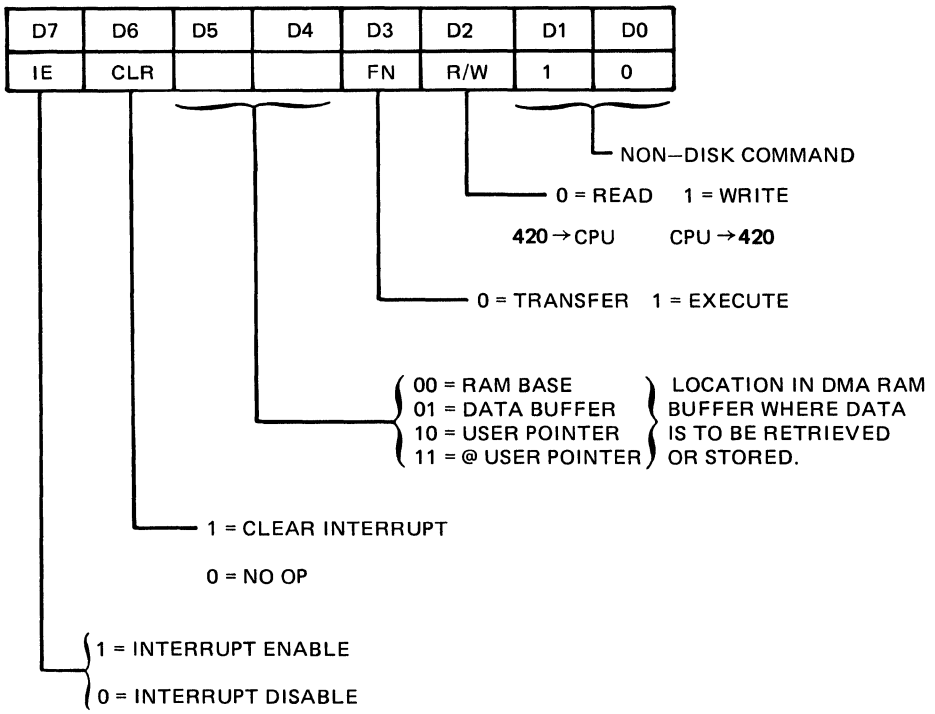
Initialization of the AM-420 is accomplished by writing a zero byte into the AM-420 command register during system initialization. The on-board CPU finishes initialization of the disk controller and releases the Phantom signal.

3.4 COMMAND REGISTER

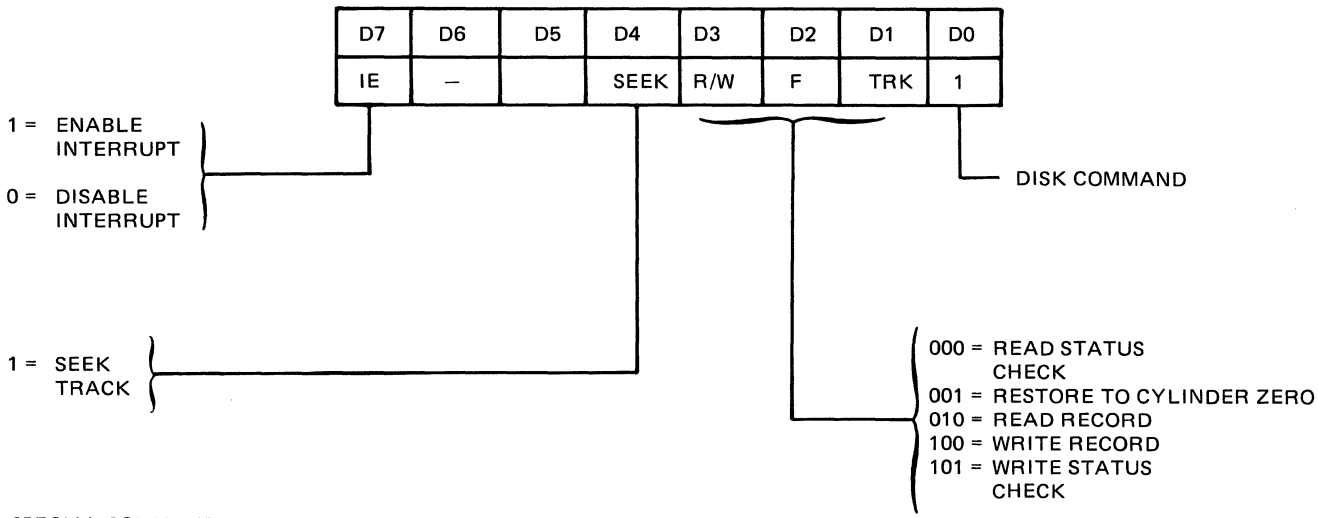
The command register receives AM-420 commands from the S-100 bus. It is accessed by writing to the selected address. The base addresses are in multiples of four from the first address FF00 (Hex) to FFFC (Hex) in increments of four. A software handshake sequence must be used for the command transfer (see paragraph 3.7). FFC4 (Hex) is the base address when it is shipped from the factory.

There are three basic types of commands used for operation of the AM-420 system; non-disk commands, disk commands and special commands. All three types are described in Figure 3-1.

NON-DISK COMMANDS:



DISK COMMANDS:



SPECIAL COMMANDS:

1. **0F HEX – READ REVISION LEVEL**
2. **1F HEX – RUN MEMORY TEST**
3. **2F HEX – SEQUENCE UP DRIVE**
4. **3F HEX – SEQUENCE DOWN DRIVE**
5. **4F HEX – RESET DRIVE**
6. **5F HEX – READ DRIVE ID**
7. **6F HEX – READ SECTOR SIZE**
8. **7F HEX – READ CURRENT CYLINDER**
9. **8F HEX – READ DRIVE STATUS**

Figure 3-1. System Commands

3.5 STATUS REGISTER

The status register is used to determine the current status of the AM-420 controller. It is accessed from the S-100 bus by reading from the user selected base address of the circuit board FFC4 (Hex). The format of the status register is described in Figure 3-2.

3.6 INTERRUPT MODE

The interrupt mode in the AM-420 can be selected by both disk and non-disk commands. If the interrupt mode is selected, the interrupt occurs at the completion of the current AM-420 command. The interrupt must be cleared by the user by setting bit 6=1 of any non-disk command.

3.7 HANDSHAKE SEQUENCE

A handshaking type interaction is required between the AM-420 circuit board and the CPU any time a command is sent to the AM-420. This handshaking is a software operation that uses bit 7 of the Status Register. Handshake operations proceed in the following sequence:

1. A command is sent from the S-100 bus to the Command Register.

2. The system software waits for bit 7 of the Status Register to become a 1 to guarantee that the AM-420 has received the command.

3. The system software writes a zero into the Command Register to clear the previous command.

4. The system software waits until bit 7 of the Status Register becomes a 0 indicating that the Command Register has been cleared and the command has been executed.

This completes the handshake operation and the program continues.

STATUS REGISTER BITS (PORT)

D7	D6	D5	D4	D3	D2	D1	D0
CR							

DISK ERROR CODES

02 (HEX) = DRIVE SEQUENCING UP
03 (HEX) = SPECIAL COMMAND ERROR (UNKNOWN SPECIAL COMMAND RECEIVED)
04 (HEX) = RAM SELF TEST ERROR
05 (HEX) = DISK NOT READY
0B (HEX) = DISK WRITE PROTECTED
0F (HEX) = DISK FAULT (THE CODE FOR THE FAULT IS LOCATED IN THE DATA REGISTER (BASE ADDRESS +1).
40 (HEX) = READ CRC ERROR

DATA REGISTER BITS FOR DISK FAULTS ONLY (PORT + 1)

D7	D6	D5	D4	D3	D2	D1	D0
CRJ	WPR	FLT	BSY	UNK	SKF	UNK	RDY

CRJ – COMMAND REJECT – A COMMAND WAS SENT TO THE DRIVE WHILE IT WAS ALREADY PROCESSING ONE

WPR – WRITE PROTECT – DRIVE IS WRITE PROTECTED

FLT – DRIVE FAULT – DRIVE FAULT

BSY – DRIVE BUSY – DRIVE IS BUSY PROCESSING COMMAND

SKF – SEEK FAULT – A DRIVE SEEK COMMAND CAUSED AN ERROR

RDY – 3-5 DRIVE READY – DRIVE IS READY

UNK – UNKNOWN – BITS MAY BE IN ANY STATE

Figure 3-2. AM-420 Status Words

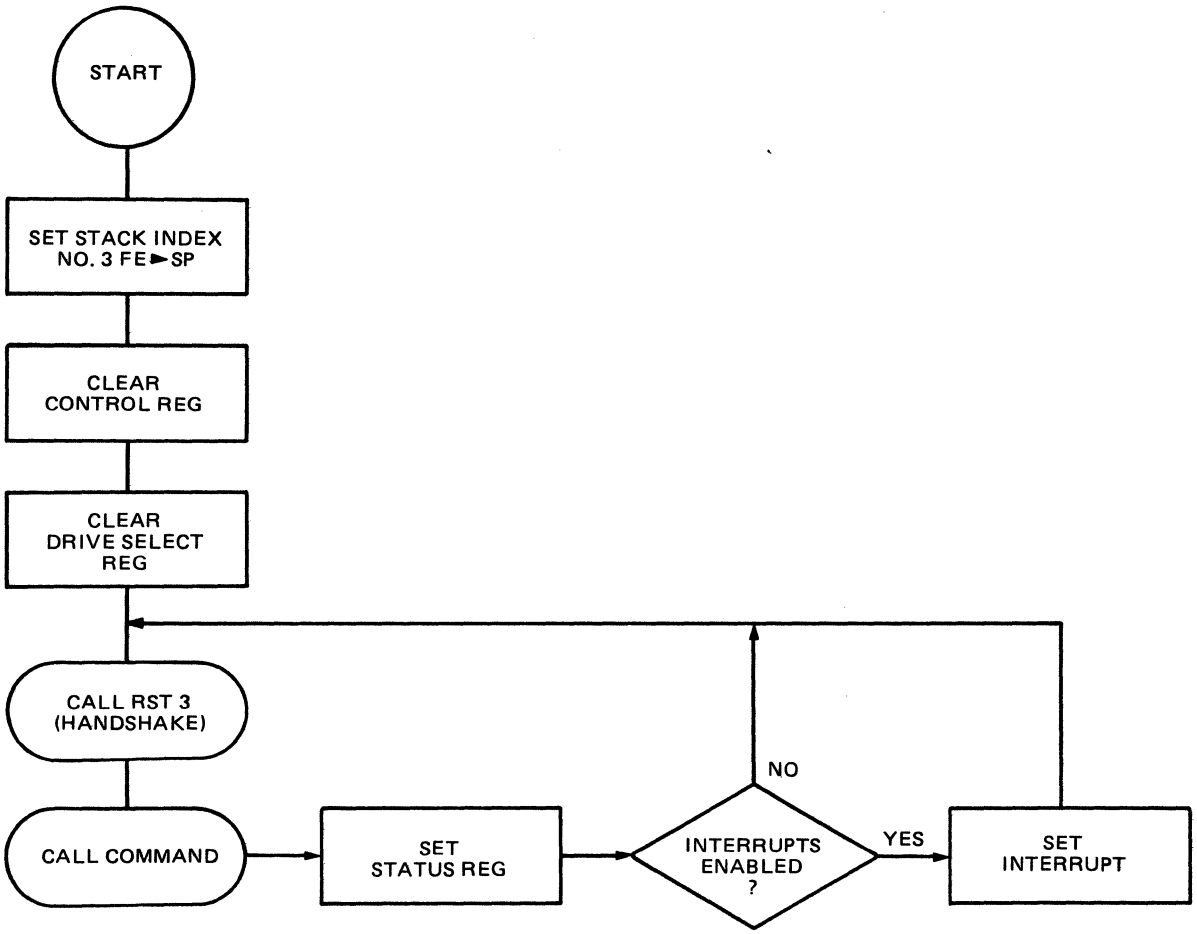


Figure 3-3. DMA Buffer Operation

3.8 DMA BUFFER

The DMA buffer is the 1K RAM in the AM-420. All data transfers to or from the disk must pass through this buffer and are handled by the DMA logic.

The DMA buffer is accessed by addressing the AM-420 base address plus one and all data between the AM-420 and the S-100 bus must pass through this single port. No DMA type operations occur between the AM-420 and system memory because they are handled on a programmed basis only. The microcode initializes the buffer and sets the DMA channels for proper operation as shown in Figure 3-3. The Handshake sequence is shown in Figure 3-4, and the data transfer sequence is shown in Figure 3-5.

The starting location within the buffer is determined by bits 4 and 5 of non-disk commands. The RAM base address (D5=0, D4=0) points to the first location in the DMA buffer. The first eight locations of this buffer are used to store information regarding retry count, drive select, and cyclinder/sector/head select.

The data buffer address (D5=0, D4=1) points to the start of 512 data bytes within the buffer and begins at the ninth byte. The user pointer address (D5=1, D4=0) points to a location within the DMA buffer which may be loaded by the user to point to other buffer memory locations for data transfer or the start of user defined microcode. The actual location is the last two bytes of the 1K RAM used for the DMA buffer. The user pointer (D5=1, D4=1) is used to make indirect data transfers or jumps to microcode using the user pointer.

3.8.1 DMA Buffer Operation For Disk Write

Transferring data to the DMA buffer and then performing disk write operations takes place as follows:

1. Send DMA write command 06 (Hex) to the AM-420 command register and perform a handshake.

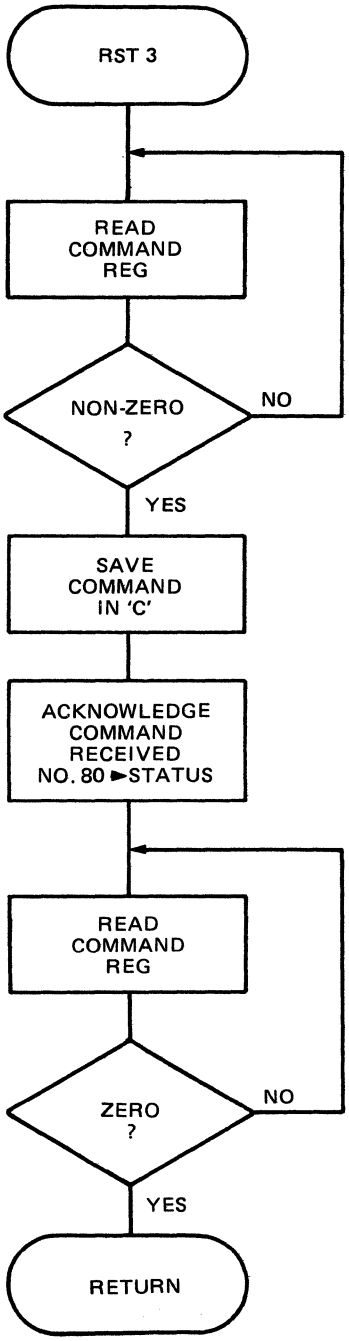


Figure 3-4. Handshake Sequence

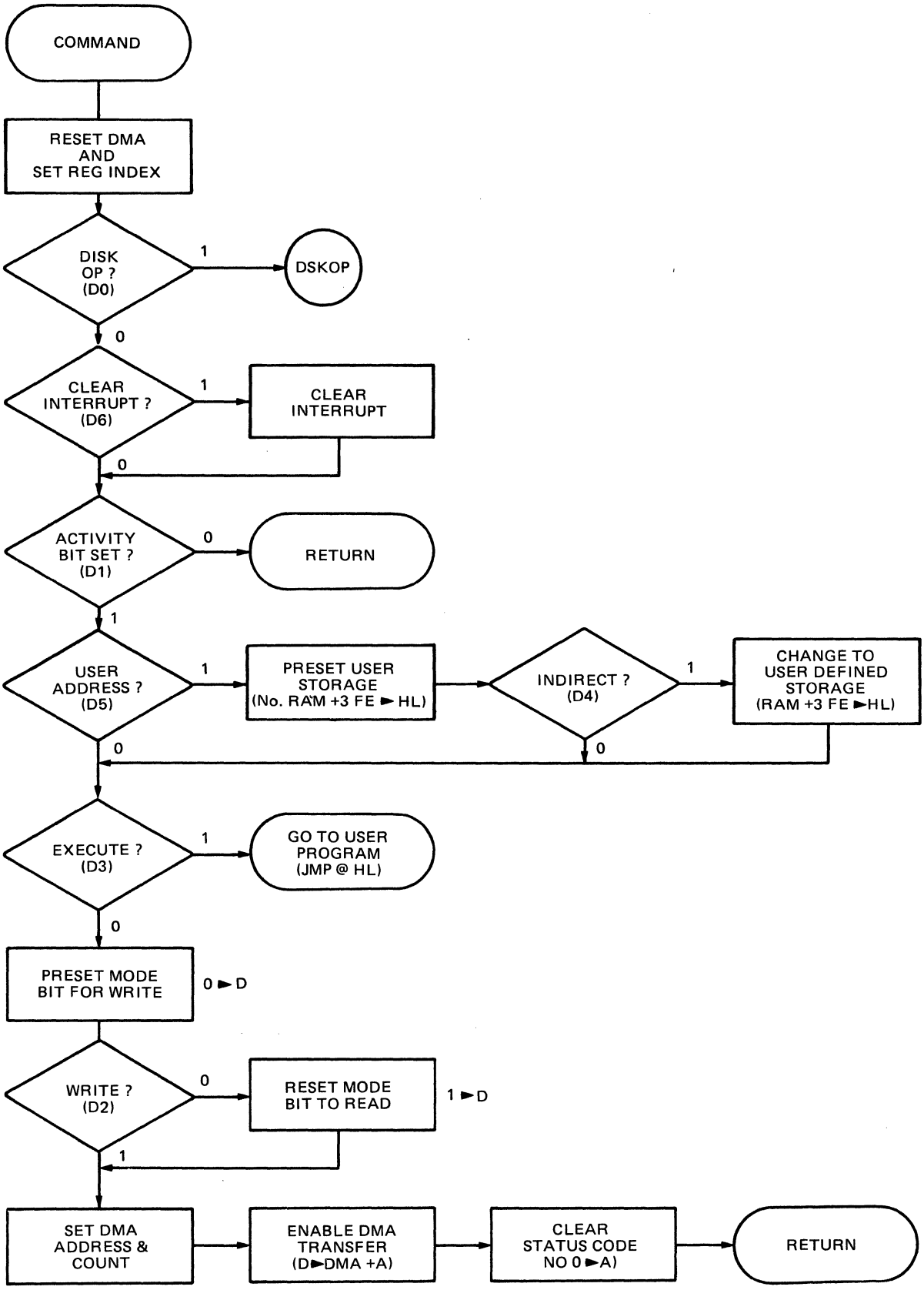


Figure 3-5. DMA Transfer Sequence

2. Send retry count to AM-420 DMA buffer (normally 8).

3. Send disk unit number (0-3) to DMA buffer (see note).

4. Write physical address plus two bytes of zeros (6 bytes total), sector, head, cylinder (2 bytes).

5. Send data (0-512 bytes) to DMA buffer.

6. Send disk write command 19 (Hex), or 99 (Hex) for interrupt, to AM-420 command register and perform a handshake.

7. Read AM-420 status register and check for zero condition indicating no error.

8. Continue with next command if no errors are detected.

NOTE: Disk unit number is sent as a radial select.
i.e. Unit 0=0001 binary
Unit 1=0010 binary
Unit 2=0100 binary
Unit 3=1000 binary

3.8.2 DMA Buffer Operation For Disk Read

Transferring data from the disk into the DMA buffer and then reading the DMA buffer is performed as follows:

1. Send a DMA write command 06 (Hex) to the AM-420 command register and perform a handshake.

2. Write retry count into the DMA buffer.

3. Write disk unit number (0-3) into the DMA buffer.

4. Write physical address plus two bytes of zeros (six bytes total), sector, head, cylinder (2 bytes).

5. Write disk read command 15 (Hex), or 95 (Hex) for interrupt, to the AM-420 command register and perform a handshake.

6. Read AM-420 status register and check for zero condition indicating that no errors have occurred.

7. Assuming that no errors occurred during the disk read, send the DMA read command 12 (Hex), or 92 (Hex) for interrupts to the AM-420 command register and perform the normal handshake.

8. Read one byte of data from the DMA buffer and discard it (the first byte is always invalid data).

9. Read the valid data (1 to 512 bytes) from the DMA buffer.

3.8.3 Physical Address

The term physical address refers to a four byte block pointing to the cylinder/sector/head within the drive. The user enters these four bytes in the following order:

1. Sector (1 byte)

2. Head (1 byte)

3. Cylinder (2 bytes)

A valid sector number is between zero and the maximum number of sectors around a disk track. A valid head number is between zero and the maximum number of heads in the drive.

A valid cylinder number is a two byte number between zero and the maximum number of cylinders within a drive.

3.9 RESTORE COMMAND

The restore command is used to reset the disk logic and force the disk head to return to track zero. The user may force a restore command with a disk command 3 (Hex), or the microcode will exercise the restore command on its own following certain errors.

If a disk fault occurs, the microcode attempts one restore and then checks the fault status again. If the fault still exists, the microcode aborts the command operation and reports an error to the CPU.

3.10 STATUS CHECK

The Read and Write Status check commands are used to access specific status information from the disk drive.

The Write Status check command is used to determine if the currently addressed disk is write protected. It does not attempt to actually write any data. If the addressed disk is write protected, error code ØB (Hex) is placed in the status register.

The Read Status check command (if SEEK bit 4 is on) seeks for the currently addressed track and then returns. Data is not read from the disk. If an error occurred, an error code is placed in the status register.

3.11 SPECIAL COMMANDS

The third class of commands are special feature commands. There are two types of these commands which will be discussed in paragraphs 3.11.1 and 3.11.2.

1. Read Microcode Revision Level - This command will return the revision level of the microcode. This is a Type II Command.

2. Execute Internal RAM Test - This command will execute an internal RAM Test. It takes about 5 seconds to run. This test is run at power up, but not at reset automatically. This is a Type II Command.

3. Sequence Up Drive - Will sequence up the selected drive (Type I Command).

4. Sequence Down Drive - Will sequence down the addressed drive (Type I Command).

5. Reset Drive - Will reset fault on selected drive.

6. Read Drive Type Command - Will return type of drive currently selected (Type II Command).

7. Read Drive Sector Size - Will return number of bytes per sector on selected drive (Type II Command)

8. Read Current Cylinder - Will return position of head on selected drive (Type II Command).

9. Read Drive Status - Returns drive status on selected drive (Type II).

3.11.1 Type I Commands

Type I commands return no information.

3.11.2 Type II Commands

Type II commands return information through both the Status Register and the on-board RAM Buffer.

A detailed listing of commands, their usage and how they return data is described in the following paragraphs.

3.11.2.1 Read Revision Level (OF hex)

1. Write a OF hex to command port.
2. Perform handshake sequence.
3. Write a 12 hex to command port.
4. Perform handshake.
5. Read one byte from the DMA buffer and discard (first byte is invalid data).
6. Read three ASCII characters from the DMA buffer. These will be the revision level of the Prom.

3.11.2.2 RAM Test (1F hex)

1. Write command and perform handshake. It will take approximately 5-6 seconds for the RAM test and the completion of the handshake. If the test failed, a 4 hex will be returned in the status register at the end of the handshake. If no error, terminate.
2. If test fails write 12 hex to command port.

3. Perform handshake.

4. Read one byte from data port and discard.

5. The next four bytes contain:

   a. Error address Lo.

   b. Error address Hi.

   c. Byte Written.

   d. Byte read.

3.11.2.3 Sequence Up Drive (2F hex)

1. Write a 6 hex to command port.

2. Perform handshake.

3. Write a zero to data port.

4. Write unit number to data port in a radial select fashion, i.e. Unit 0=01

5. Write a 2F hex to command port.

6. It is recommended that the drive status command be used to wait for the drive to become ready (see paragraph 3.1.2.9).

3.11.2.4 Sequence Down Drive (3F hex)

1. Perform steps 1-4 as in Sequence Up Drive command.
2. Write a 3F hex to command port.
3. Perform handshake.

3.11.2.5 Reset Drive (4F hex)

1. Perform steps 1-4 as in Sequence Up Drive command.
2. Write a 4F hex to command port.
3. Perform handshake.

3.11.2.6 Read Drive ID (5F hex)

1. Perform steps 1-4 as in Sequence Up Drive command.
2. Write a 5F hex to command port.
3. Perform handshake.
4. Write a 12 hex to command port.
5. Perform handshake.
6. Read one byte from data port and discard.
7. Read byte from data port, this byte is the drive ID. Refer to the manual on the particular drive to determine the drive ID.

3.11.2.7 Read Drive Sector Size (6F hex)

1. Perform steps 1-4 as in Sequence Up Drive command.

2. Write a 6F hex to command port.

3. Perform steps 3-6 of Read Drive ID. command.

4. The next two bytes read from the data port are the number of bytes per sector stored at Low byte and High byte.

3.11.2.8 Read Current Cylinder (7F hex)

1. Perform steps 1-4 as in Sequence Up Drive command.

2. Write a 7F hex to command port.

3. Perform steps 3-6 as in Read Drive ID. command.

4. The next two bytes read from the data port are the current cylinder stored Low byte, High byte.

3.11.2.9 Read Drive Status (8F hex)

1. Perform steps 1-4 as in Sequence Up Drive command.

2. Write an 8F hex to command port.

3. Perform steps 3-6 as in Read Drive ID. command.

4. Read drive status byte. Bits are as follows:

Bit 0 = Drive up to speed and ready

Bit 1 = Seek completed

Bit 2 = Seek fault

Bit 3 = Head on cylinder zero

Bit 4 = Drive processing command

Bit 5 = Drive unsafe condition

Bit 6 = Drive write protected

Bit 7 = Command received while busy

SECTION IV

FUNCTIONAL THEORY OF OPERATION

4.0 INTRODUCTION

The AM-420 Disk Controller circuit board contains integrated circuit elements for the data processing necessary for the performance of the functions described in Sections I,II and III of this manual. This section describes the functional theory of operation of the circuit board and also provides information for each of the integrated circuit elements.

4.1 CIRCUIT BOARD OPERATION

This circuit board provides control and interface capability between the S-100 bus and the PRIAM Winchester hard disk drive. The functional block diagrams of the circuit board are shown in Figures 4-1 and 4-2. The circuit board schematics, parts lists, and component cross reference lists are contained in Section VI of this manual. Table 4-1 contains a list of the signals used in these circuit boards with descriptions of their functions.

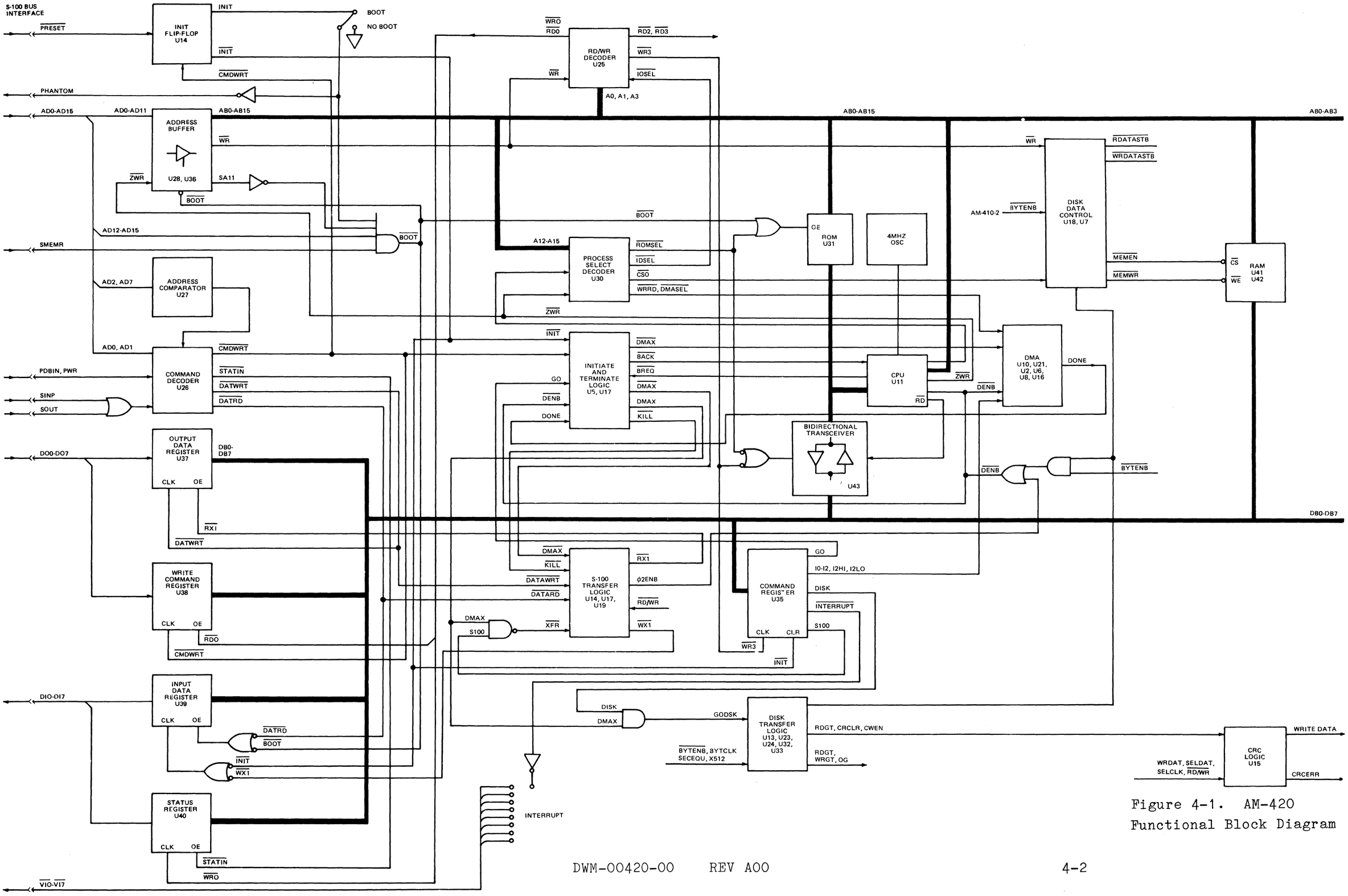


Figure 4-1. AM-420 Functional Block Diagram

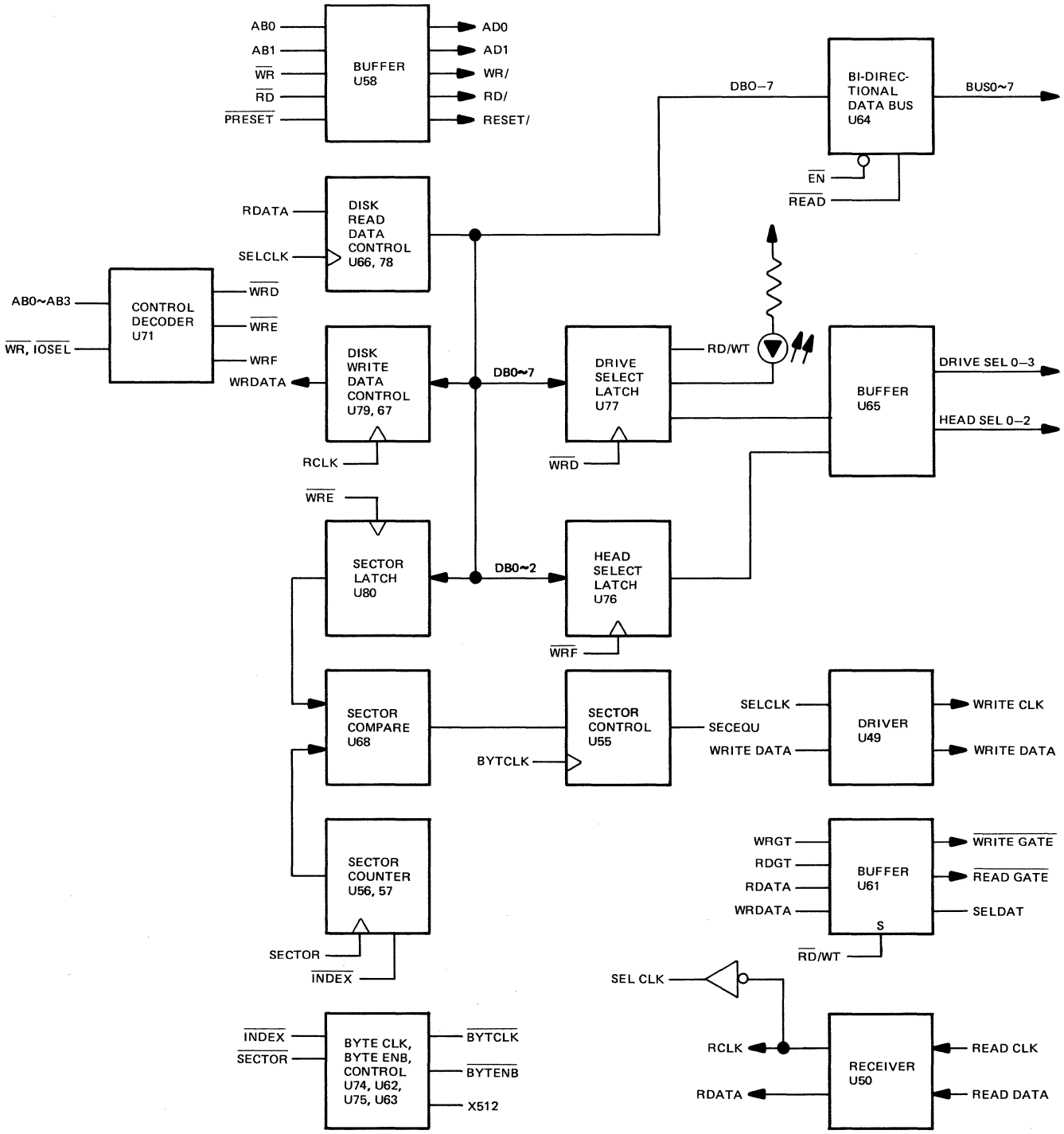


Figure 4-2. AM-420 Functional Block Diagram

Table 4-1. AM-420 Signals List

SIGNAL	NAME	SCHEM PAGE OF SOURCE	DESCRIPTION
AB0-AB15	Address Bus		16 Bit Tri-state address bus. Provides addressing for memory, data exchanges and I/O device exchanges.
$\overline{\text{BACK}}$	Bus Acknowledge	SH1	CPU module output indicating that the CPU module address bus, data bus, and tri-state control bus signals have been set to their high impedance state.
$\overline{\text{BOOT}}$	Bootstrap Load	SH1	Generated when the bootstrap program has been selected. Enables the ROM, Address Buffer and Input Data Register.
$\overline{\text{BREQ}}$	Bus Request	SH1	CPU module input requesting that the CPU module set its address bus, data bus, and tri-state control bus to the high impedance state.
BYTCLK $\overline{\text{BYTCLK}}$	Byte Clock	SH3	Generated by the Byte Clock Counter at the end of each byte of data written or read. Used to control the Shift/ Load of the write data shift register and disk transfer logic.

Table 4-1 (Con't). AM-420 Signals List

SIGNAL	NAME	SCHEM PAGE OF SOURCE	DESCRIPTION
$\overline{\text{BYTENB}}$	Byte Enable	SH3	Byte clock counter output at the same frequency as $\overline{\text{BYTCLK}}$ but twice the duration. Used by the disk transfer logic and disk data control logic.
$\overline{\text{CMDWRT}}$	Command Write	SH1	Output of the Command Decoder to clock command data into the Write Command Register and set up the initiate logic.
CRCERR	CRC Error	SH2	Output of the CRC checking module indicating an error in the data.
CRCLR	CRC Clear	SH2	Master reset input to the CRC checking module.

Table 4-1 (Con't). AM-420 Signals List

SIGNAL	NAME	SCHEM PAGE OF SOURCE	DESCRIPTION
CSO	Chip Select	SH1	Output of the process select decoder and is one of the signals that enables the RAM.
CWEN	Check Word Enable	SH2	Generates the enable signal to the CRC checker allowing the check word to be generated and written onto the disk.
$\overline{\text{DATRD}}$	Data Read	SH1	Command Decoder output to enable the Input Data Register and to generate S-100 transfer signals.
$\overline{\text{DATWRT}}$	Data Write	SH1	Command Decoder output to enable the Output Data Register and to generate S-100 transfer signals.
DENB	DMA Enable	SH2	Provides clock input to the DMA Address Generator modules. DMA enable begins each cycle of the DMA.

Table 4-1 (Con't). AM-420 Signals List

SIGNAL	NAME	SCHEM PAGE OF SOURCE	DESCRIPTION
$\overline{\text{DMASEL}}$	DMA Select	SH1	Output of the process select decoder to enable the selected DMA address generator. Used to write data into or read data from the DMA address generator.
DMAX $\overline{\text{DMAX}}$	DMA Access Grant	SH2	Indicates that the on-board CPU is off the busses and that control of those busses may now pass to the DMA logic.
DISK	Disk Command	SH2	Output of the Command Register to set up a disk operation with DMA Access Grant signal.
DONE	Process Command	SH2	Output of the DMA Address Generator indicating completion of the current operation.
D0-D7	Data Bus Bits 0-7	SH1	Internal eight-bit tri-state data bus.

Table 4-1 (Con't). AM-420 Signals List

SIGNAL	NAME	SCHEM PAGE OF SOURCE	DESCRIPTION
GO	Go	SH2	Start command output from Command Register. Initiates the transfer of bus control from the on-board CPU to the DMA logic.
GODSK	Go Disk	SH2	Initiates disk operations under DMA logic control.
IDXSEC $\overline{\text{IDXSEC}}$	Sector Reset	SH3	Reset command to byte clock counter to reset count to beginning of each sector.
INDEX	Disk Index	SH3	Index pulse from disk drive. Occurs once per revolution of the disk to define the beginning of sector zero.
INIT $\overline{\text{INIT}}$	Initialize	SH1	Internal reset signal generated from S-100 bus $\overline{\text{PRESET}}$ signal.
$\overline{\text{IOSEL}}$	I/O Select	SH1	Generated from either Read or Write output from the CPU microprocessor when address lines A14 and A15 from the internal address bus are both one.

Table 4-1 (Con't). AM-420 Signals List

SIGNAL	NAME	SCHEM PAGE OF SOURCE	DESCRIPTION
I0, I1	Instruction Codes	SH2	Instruction code inputs to the DMA Address Generator from the Command Register.
I2LO, I2HI	Instruction Codes	SH2	Instruction code to either the upper eight bits or lower eight bits of the DMA Address generator from the command register.
$\overline{\text{JAM6}}$	Preset Six	SH3	Presets byte clock counter to a count of six to synchronize the read timing.
$\overline{\text{KILL}}$	Terminate	SH2	Terminates the operation in process.
$\overline{\text{MEMEN}}$	Memory Enable	SH2	Enables the RAM for read or write operations.
$\overline{\text{MEMWR}}$	Memory Write	SH2	Controls read or write operations of the RAM. Low = write, High = read.
OG	Output Gate	SH2	Allows transfer of data into or out of the disk drive.

Table 4-1 (Con't). AM-420 Signals List

SIGNAL	NAME	SCHEM PAGE OF SOURCE	DESCRIPTION
RDATA	Read Data	SH3	The data recovered from the disk in NRZ form.
$\overline{\text{RDDATA STB}}$	Read Data Strobe	SH2	Generated by the Disk Data Control logic to transfer a byte of read data from the buffer register to the data bus DB0-DB7.
RDGATE	Read Transfer Gate	SH3	Instructs the disk drive to gate the read data onto the interface. It occurs for any disk transfer cycle (read or write).
RDGT	Read Gate	SH2	Same as RDGATE but only during a read disk transfer (gated by $\overline{\text{RD}}$/WR).
$\overline{\text{RD}}$/WR	Read/Write	SH4	Generated from bit 4 of command word to set either disk Read or Write processing.
RD0-RD3	Read 0 - Read 3	SH1	Read select outputs from the Read/Write decoder to enable read operations.

Table 4-1 (Con't). AM-420 Signals List

SIGNAL	NAME	SCHEM PAGE OF SOURCE	DESCRIPTION
$\overline{\text{ROMSEL}}$	ROM Select	SH1	Generates the output enable of the ROM.
$\overline{\text{RX1}}$	Output Data Transfer	SH2	Output from the S-100 bus Transfer logic to transfer data from the Output Data Register to the Internal data bus DB0-DB7 (logical OR of RD1 and the read pulse from the DMA logic).
SA11	S-100 Address Bit 11	SH1	Buffered S-100 address bit 11.
SDREQ $\overline{\text{SDREQ}}$	S-100 Data Request	SH2	Generated from $\overline{\text{DATWRT}}$ or $\overline{\text{DATRD}}$ for S-100 bus data transfers.
SECEQU	Sector Equal	SH3	Pulse output of the Sector Counter and Control logic when the sector counter is equal to the sector latch indicating that the requested sector is under the read/write head.

Table 4-1 (Con't). AM-420 Signals List

SIGNAL	NAME	SCHEM PAGE OF SOURCE	DESCRIPTION
SECTOR	Sector Pulse	SH3	Sector pulse that occurs at the beginning of each disk sector except sector zero which is marked by the INDEX pulse.
SELCLK	Selected Clock	SH3	Data Clock
SELDAT	Selected	SH3	Either read data or write data depending on state of read/write command.
$\overline{\text{STATIN}}$	Status In	SH1	Output of the command decoder to enable the Status Register.
S100	S-100 Select	SH2	Command Register output to enable an S-100 bus data transfer.
$\overline{\text{WR}}$	Write	SH1	Generated from on-board CPU Write (ZWR) signal.
WRDATA	Write Data	SH3	Serial write data from the shift register into the CRC generator.

Table 4-1 (Con't). AM-420 Signals List

SIGNAL	NAME	SCHEM PAGE OF SOURCE	DESCRIPTION
$\overline{\text{WRDATA STB}}$	Write Data Strobe	SH2	Generated by the Disk Data Control logic to clock the write data from the data bus DB0-DB7 into the write buffer register.
WRGT	Write Transfer Gate	SH2	Instructs the drive to write data onto the selected surface. It occurs for both read and write disk transfer cycles.
WRITE GATE	Write Gate	SH3	Same as WRGATE but only during a write disk transfer (gated by $\overline{\text{RD}}$/WR).
WRITE DATA	Disk Write Data	SH3	Disk write data from the CRC checker logic applied to the write data drivers.
$\overline{\text{WRRD}}$	Write-Read	SH1	Read pulse or write pulse from the on-board CPU.

Table 4-1 (Con't). AM-420 Signals List

SIGNAL	NAME	SCHEM PAGE OF SOURCE	DESCRIPTION
WR0-WR3 WRD-WRF	Write0-Write3 WriteD-WriteF	SH1	Write select outputs from the Read/Write decoder that enable write operations to selected latches.
WX1	Write 1	SH2	The logical OR of WR1 and the write pulse from the DMA logic.
XFER	Transfer	SH2	Generated from DMAX and S-100 to strobe the S-100 Transfer Logic to transfer data from the Input and Output Data Registers to the internal data bus.
X512	Times 512	SH1	Used by the DMA logic to indicate when all data has been written or read and that CRC data is next.
$\overline{\text{ZWR}}$	CPU Write	SH1	Indicates that the CPU Module holds valid data to be stored in the addressed memory.

Table 4-1 (Con't). AM-420 Signals List

SIGNAL	NAME	SCHEM PAGE OF SOURCE	DESCRIPTION
4 MHZ	4 MHz Clock	SH1	4 MHz clock from oscillator U9.
02ENB	S-100 Transfer	SH2	Clock signal for every cycle of the S-100 data transfer.

The major processing components of this board are the CPU microprocessor (U11) and the DMA Address Generator (U10 and U21). The ROM (U31) contains the bootstrap load routine and also contains the microcode necessary for operation of the microprocessors.

4.1.1 Power-Up Reset

On initial power-up, the circuit board is in a dormant state waiting for initialization. The PRESET signal from the S-100 bus sets the INIT flip-flop U14 to activate the PHANTOM signal to disable any main memory under phantom control and to enable the bootstrap gate. INIT generally resets logic on the circuit board to initial conditions.

4.1.2 Addressing

Address data is received from the S-100 bus on address lines AD0-AD15. This address data is transferred to the internal address bus during boot loading for use by the controllers and memories within the circuit board and is also used for direct addressing of the circuit board. Buffers on U28 and U36 gate the addresses to the internal bus when enabled by bootstrap signal BOOT.

Address lines AD2-AD7 are wired directly to comparator U27 for circuit board addressing. The other inputs come from circuit board etch or jumper wires to either +5V pull-ups or ground to produce the desired address. The output of the comparator U27 is asserted when the data from the address lines compare with the address of the AM-420. This generates read and write signals from decoder U26. The address in etch is C4 (Hex) and other addresses can be selected as described in Section II.

4.1.3 CPU Output

CPU output data is transmitted to the AM-420 for circuit board control and data transfer by the S-100 bus data and control lines. Data is received by the AM-420, by the Output Data Register U37, and the Write Command Register U38. The Input to these data registers comes from the S-100 bus data lines D00-D07 and the output, when enabled, goes to internal data bus DB0-DB7.

4.1.3.1 Command Data

Data from the S-100 bus data lines is clocked into the Write Command Register by Command Write signal CMDWRT from the Command Decoder U26. This takes place when address lines AD0 and AD1 are zero and I/O output signal SOUT from the S-100 bus is asserted. Signal CMDWRT also resets the INIT flip-flop U14 and resets the initiate logic.

When the CPU microprocessor issues a write command (ZWR) and address lines AB14 and AB15 from the internal address bus are both one, IOSEL is asserted to enable the Read/Write decoder U25. Signal ZWR is also applied to buffer U28 to generate WR which is an input to the Read/Write decoder. When address bits AB0 and AB1 from the internal bus are zero, the RD0 output from the Read/Write decoder transfers the contents of the write command register to the internal data bus.

4.1.3.2 Command Types

The non-disk commands issued to the AM-420 are used for control and operation of the logic internal to the circuit board. The bit functions are listed in Table 4-2 and the commands are listed in Table 4-3. Disk Commands are used to control the disk drive and access status information from the drive. Disk command bit functions are listed in Table 4-4, and disk command codes are listed in Table 4-5.

Table 4-2. Non-Disk Command Bits

BIT	NAME	FUNCTION
0 1	0 1	=0 Indicates non-disk command =1 Activity Bit.
2	R/W	Read/Write 0=read (AM-420 to CPU), 1= write (CPU to AM-420).
3	FN	Command Function 0=transfer 1=execute
4 5	BUF DMA	Location in DMA buffer where data is to be retrieved or stored.*
6	CLR	Clear current interrupt 0=nop 1=clear
7	IE	Interrupt Enable 0=disable 1=enable

*

Bit		Location
5	4	
0	0	RAM Base (Direct)
0	1	Data Buffer
1	0	User Pointer
1	1	@ User Pointer (Indirect)

Table 4-3. Non-Disk Command Formats

BITS 7 6 5 4 3 2 1 0	FUNCTION
0 0 0 0 0 0 0 0 X X 0 0 0 1 1 0 X X 0 1 0 1 1 0	Initialization/Boot Load Write data to DMA buffer (RAM Base) Write data to DMA buffer (Data Base)
X X 0 0 0 0 1 0 X X 0 1 0 0 1 0	Read data from DMA buffer (RAM Base) Read data from DMA buffer (Data Base)
0 1 0 0 0 0 0 0 X 1 X X X X 1 0	Clear Interrupt (Clear Only) Clear Interrupt (plus some other non-disk command)
X X 1 0 0 1 1 0	Write user microcode pointer
X X 1 1 0 1 1 0	Indirect load via user pointer
X X 1 1 1 0 1 0	Execute from users microcode pointer
X X 1 1 0 0 1 0	Indirect read via user pointer
X X 1 0 0 0 1 0	Read user microcode pointer

Table 4-4. Disk Command Bits

BIT	NAME	FUNCTION
0	DSK	Always 1 for disk type commands.
1 2		Command function comprised of bits 1, 2, and 3 taken as a whole. *
3	R/W*	0=read 1=write
4	SK	Seek
5	-	Not used
6	-	Not used
7	IE	Interrupt enable 0=disable 1=enable

* See Table 4-5

Table 4-5. Disk Command Codes

BITS			FUNCTION
3 R/W	2	1	
0	0	0	Read Status Check
0	0	1	Restore to Cylinder Zero
0	1	0	Read Record
0	1	1	Read Record
1	0	0	Write Record
1	0	1	Write Status Check

4.1.3.3 Output Data

The output data from the CPU to the AM-420 transfers from the S-100 bus data lines to the internal data bus through the Output Data Register U37. The input to the Output Data Register comes from the S-100 bus data lines D00-D07; and the output, when enabled, goes to the internal AM-420 data bus DB0-DB7.

Data from the S-100 bus data lines is clocked into the Output Data Register by data write signal $\overline{\text{DATWRT}}$. This is generated by the Command Decoder when the board is addressed and address lines AD0=1 and AD1=0 and I/O output signals SOUT and $\overline{\text{PWR}}$ from the S-100 bus are asserted. Signal $\overline{\text{DATWRT}}$ also sets flip-flops in the S-100 transfer logic to generate $\overline{\text{RX1}}$ to transfer the data from the Output Data Register to the internal bus during internal S-100 type DMA cycles.

4.1.4 CPU Input

CPU input data is transmitted from the AM-420 by the S-100 bus data and control lines. It is transmitted from the AM-420 by the Status Register (U40) and the Input Data Register (U39).

4.1.4.1 Status Register

The Status Register is used to determine the current status of AM-420 board operations and to indicate disk drive faults. The input to the Status Register comes from the internal data bus DB0-DB7; and the output, when enabled, goes to the S-100 bus data lines DI0-DI7.

Data from the internal data bus is clocked into the Status Register by signal $\overline{\text{WR0}}$ from the Read/Write Decoder (U25). This occurs when the lines AD0, AD1, and $\overline{\text{WR}}$ are all low. The contents of the Status Register are transferred to the S-100 bus data lines by the $\overline{\text{STATIN}}$ signal from the Command Decoder. This signal is issued when AB0=0 AB1=0, PDBIN is true (high) and $\overline{\text{PWR}}$ is false (high).

4.1.4.2 Status Word Formats

Status words contain information regarding the operation of the AM-420 board and associated disk drives. Status word information and formats are contained in Figure 4-3. Bit 7 is the Command Received (CR) bit (1=Received, 0=Cleared).

When the status word is received by the CPU, the data is checked for any of the four codes shown at the top of Figure 4-3. If the disk error code is found, the disk error status is accessed from the data register. Bit definitions for disk faults are shown in Figure 4-3.

4.1.4.3 Input Data Register

The Input Data Register (U39) controls the transfer of data from the internal data bus to the S-100 bus data lines. The inputs to this register come from internal data bus DB0-DB7 and the output, when enabled, goes to the S-100 bus data lines DI0-DI7.

Data from the internal bus is clocked into the register when either $\overline{\text{INIT}}$ or $\overline{\text{WX1}}$ are True. Signal $\overline{\text{INIT}}$ controls the register during a boot data transfer and Write Transfer 1 ($\overline{\text{WX1}}$) signal comes from the S-100 bus transfer logic. Signal $\overline{\text{WX1}}$ is generated in the same way as $\overline{\text{RX1}}$ described in paragraph 4.1.3.3 except $\overline{\text{RD}}$/WR input to the S-100 bus transfer is in the Write state. Data is placed on the S-100 bus data lines when in the bootstrap mode by $\overline{\text{BOOT}}$ or by the $\overline{\text{DATRD}}$ output of the Command decoder. Signal $\overline{\text{DATRD}}$ is issued when the board is addressed and AD0=1, AD1=0, Read Enable PDBIN is true (high) and Write Strobe $\overline{\text{PWR}}$ is false (high).

4.1.5 Boot Load Procedure

The AM-420 contains a bootstrap load routine stored in the ROM on U31. The microcode for internal AM-420 microprocessor operation is also contained in the first 1K of ROM memory. The bootstrap program is contained in the second 1K of ROM memory.

> NOTE: If the user code is changed from the current boot routine, the microcode in the first 1K of memory must be duplicated exactly.

BIT								FUNCTION
7*	6	5	4	3	2	1	0	
CR	0	0	0	0	0	0	0	Status OK - Function Complete
CR	0	0	0	0	0	1	0	Drive Sequencing Up - Power Up Only
CR	0	0	0	0	0	1	1	Special Command Error - Illegal Spec Command
CR	0	0	0	0	1	0	0	RAM Test Error
CR	0	0	0	0	1	0	1	Disk Not Ready
CR	0	0	0	1	0	1	1	Write Protected
CR	0	0	0	1	1	1	1	Disk Error - See Below
CR	1	0	0	0	0	0	0	CRC Error

* CR = Command Received, 0 = Cleared, 1 = Received

DATA REGISTER BITS FOR DISK FAULTS

D7	D6	D5	D4	D3	D2	D1	D0
CRJ	WPR	FLT	BSY	UNK	SKF	UNK	RDY

CRJ – COMMAND REJECT – A COMMAND WAS SENT TO THE DRIVE WHILE IT WAS ALREADY PROCESSING ONE

WPR – WRITE PROTECT – DRIVE IS WRITE PROTECTED

FLT – DRIVE FAULT – DRIVE FAULT

BSY – DRIVE BUSY – DRIVE IS BUSY PROCESSING COMMAND

SKF – SEEK FAULT – A DRIVE SEEK COMMAND CAUSED AN ERROR

RDY – 3-5 DRIVE READY – DRIVE IS READY

UNK – UNKNOWN – BITS MAY BE IN ANY STATE

Figure 4-3. Status Word Formats

The CPU reads the bootstrap load program by addressing the AM-420 board and reading from F400 (Hex) up. This address, combined with SMEMR from the S-100 bus and a high INIT signal which takes place on initial start-up, generates the $\overline{\text{BOOT}}$ signal. If the optional jumper is in the NO $\overline{\text{BOOT}}$ position, one input to the BOOT AND gate is connected to ground, disabling the bootstrap feature.

The $\overline{\text{BOOT}}$ signal enables the ROM (U31), the Address Buffer (U28 and U36), and the Input Data Register (U39). The $\overline{\text{INIT}}$ signal enables the clock input to the Input Data Register and since it is a transparent latch type register, the bootstrap program transfers from the ROM to the system.

4.1.6 Interrupts

The interrupt mode can be selected for AM-420 board operation when the software program sets bit 7 in either disk or non-disk commands. When the interrupt mode is selected, the interrupt occurs at the completion of the current AM-420 command. This is taken from the internal data bus by the command register (U35) and connected to the S-100 bus vectored interrupt lines. Any one of the seven interrupt lines ($\overline{\text{VI0}}$-$\overline{\text{VI7}}$) may be selected by a jumper as shown in Section II.

The interrupt mode may be cleared by the software program so that the interrupts do not occur. The program clears the interrupt mode by setting bit 6 in any non-disk command to a one (see Table 4-2).

4.1.7 Byte Clock Counter

The byte clock counter controls the shift registers for serial-to-parallel and parallel-to-serial conversion of read and write operations respectively. It consists of a counter on U74 with associated select and gating logic.

Signal RD/WR selects the necessary clocks and data for either read or write disk operations. During read operations, flip-flops on U62 detect the first bit (sentinel) and presets the byte counter (U74) to a count of 6 ($\overline{\text{JAM6}}$). This counter then counts the selected clock pulses until a full byte is loaded into shift register U66.

The counter output is gated (count 7) to generate the clock to load the shift register data into buffer register U78 for transfer through the internal data bus to the RAM. Write operations are similar except the counter output $\overline{\text{BYTCLK}}$ controls the shift/load control to write shift register U67.

4.1.8 Disk Transfer Logic

The disk transfer logic consists of a ROM (U33), a counter to sequence the ROM (U23 and U24), an input MUX (U13) and a D flip-flop register to buffer the ROM output (U32). This logic is common to both disk read and disk write, DMA transfer operations.

Signal $\overline{\text{BYTENB}}$, that occurs once for each byte of data transferred, provides the clock input to the ROM sequence counter. Sequencing the ROM through its program controls the transfer of data from the disk to RAM and RAM to disk.

4.1.9 Sector Counter

The sector counter logic enables the controller to read or write data in a specific sector on the selected disk. Signal $\overline{\text{WRE}}$ clocks the data from the data bus DB0-DB7 into register U80. At the disk index, signal INDEX resets counter U56,U57 to FF and it then counts disk sector pulses (SECTOR) and provides its counter output to comparator U68. The other input to the comparator is the selected sector number stored in register U80. When the sector count equals the selected count, the compare output of the comparator generates sector equal signal (SECEQU) to the disk transfer logic.

4.1.10 Data Write Logic

The data write logic provides the clock and data outputs necessary for the disk drive write circuitry. Serial write data (WRDAT), from the write shift register U67 is sent to the CRC logic (U15) for error checking. For a description of the operation of the CRC module, see paragraph 4.2.3.

The selected clock and selected data (SELCLK) and SELDAT) provide the data and clock inputs to the CRC module. The output of the CRC logic is WRITE DATA that is applied to driver U49 to operate the selected write head. The SELCLK is applied to a delay to compensate for the propagation delays inherent in the write data path. The clock is then applied to driver U49 in the same manner as the write data for operation of the selected disk drive.

4.1.10.1 Disk Drive Controls

The CONTROL/STATUS informations are bidirectional through the data bus DB0-DB7 via U64. The direction of the data flow is controlled by the control decoder from address bits AB0-AB3 and IOSEL. The unit and head select data are also taken from the data bus and stored in the buffer U76 and U77.

4.1.11 Input From Disk Drive

Read data and clocks are received from the selected drive through line receiver U50. Serial READ DATA and READ CLK are applied to shift register for serial-to-parallel conversion. The data is then clocked into the register (U78) at the end of each 8-bit byte by BYTCLK. The read data strobe RDATASTB transfers that byte of data to the data bus DB0-DB7 and into the RAM (U41 and U42).

4.1.12 AM-420 Board Operations and Timing

The following paragraphs describe the timing and sequence of operations of the AM-420 board. The numbers in parentheses refer to the numbers on the associated timing diagram.

4.1.12.1 Data Transfer Operations

The system CPU issues a command to the AM-420 to perform a data transfer type of operation (data to or from the disk, or data to or from the S-100 bus). The on-board CPU sets up the board for the kind of transfer requested (disk or S-100), sets the direction of transfer (read data into the board or write data out from the board) via the $\overline{RD}$/WR bit, and sets up the DMA chips with their required address and word counts. The CPU then issues a GO command as shown in Figure 4-4.

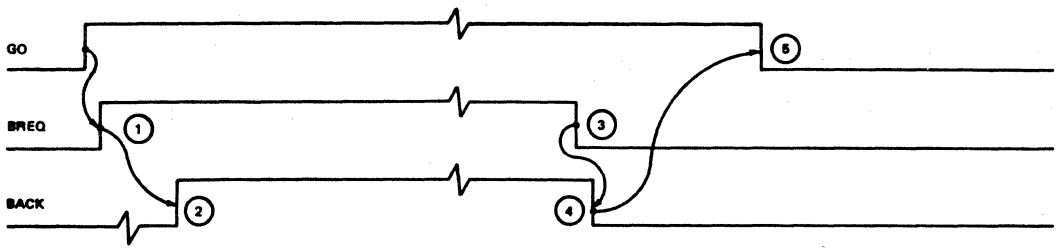


Figure 4-4. Data Transfer Timing

When the GO line goes high, it sets flip-flop U5, which causes $\overline{\text{BREQ}}$ to be asserted (1). When $\overline{\text{BREQ}}$ (Bus Request) is asserted, the on-board CPU will, at its earliest convenience, take itself off the data and address busses and issue a $\overline{\text{BACK}}$ (Bus Acknowledge) signal (2). Since $\overline{\text{BACK}}$ indicates that the on-board CPU is tri-stated, the DMA circuitry can now use the data and address busses. The DMA circuit then does its job of transferring the data. When the last byte of data is transferred, a DONE signal is issued by the DMA logic. The issuance of DONE causes $\overline{\text{BREQ}}$ to drop (3), thereby allowing the on-board CPU to reactivate itself (4), which then shuts off the GO signal (5).

4.1.12.2 Disk Transfer Operations

When the AM-420 has been issued a disk transfer command (read or write a sector), the on-board CPU checks the disk drive for error conditions and, if possible, corrects the condition. If no error exists, or it is corrected, the on-board CPU issues a GODSK command, as shown in Figure 4-5. (GODSK is the logical AND of signals GO, DISK and the CPU being tri-state, DMAX). GODSK causes the micro-engine (U13, U23, U24, U32, U33) to start up. The micro-engine then waits for the SECEQU (Sector Equals Requested Count) pulse. At this point, the micro-engine begins its sector format function, which causes the timing signals RDGATE, WRGATE, OG, CRCLR, CWEN (Read Gate, Write Gate, Output Gate, CRC Clear, Check Word Enable) to be issued at the appropriate time. The micro-engine is sequenced by the BYTCLK/$\overline{\text{BYTENB}}$ (Byte Clock, Byte Enable) signals, which are derived from the drive clock.

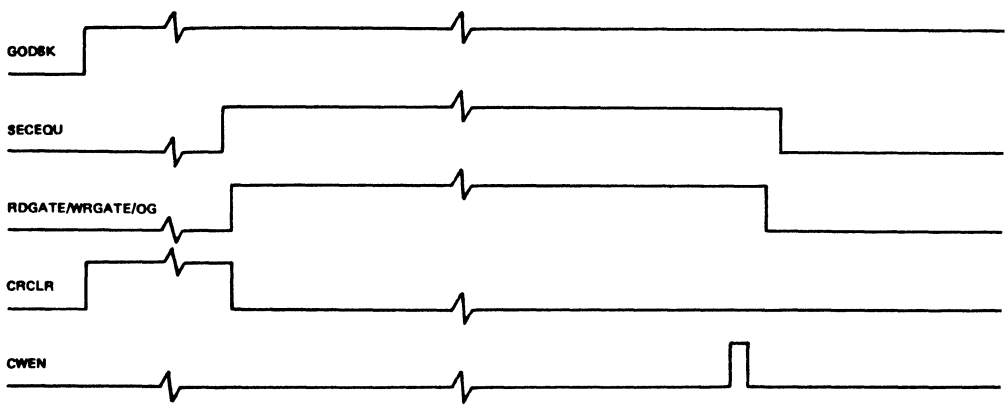


Figure 4-5. Disk Transfer Timing

4.1.12.3 Disk Read Clocks

The BYTCLK, $\overline{\text{BYTENB}}$ timing, as shown in Figure 4-6, is based on the signal READ CLOCK, which is received from the drive. Both BYTCLK and BYTENB are derived from a counter U74. The counter counts at the rising edge of SELCLK. When this count equals 7, BYTCLK is issued; When equal to 2 and 3, BYTEN is issued. When the count equals 0 (the next state) BYTCLK is dropped; when equal to 4, BYTEN is dropped. $\overline{\text{BYTENB}}$ is twice as long as BYTCLK. BYTCLK indicates when the last bit of a byte has been read or written.

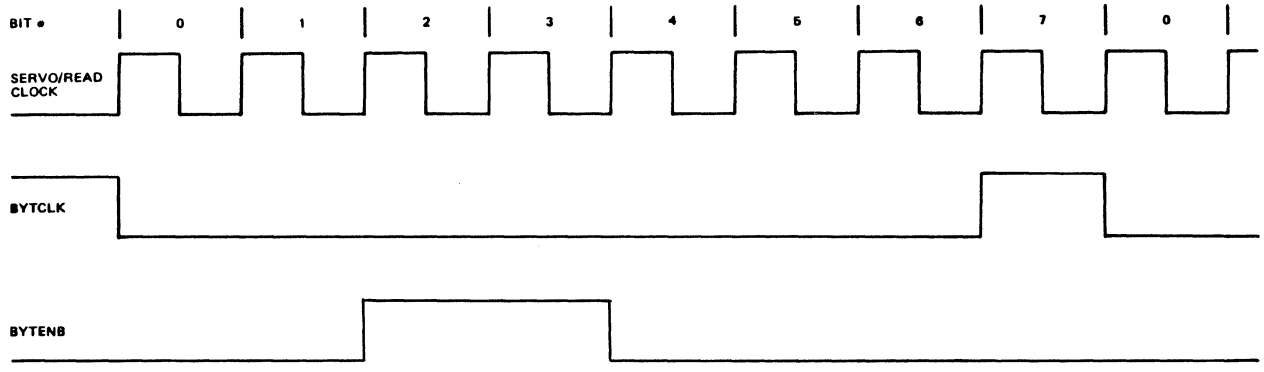


Figure 4-6. BYTCLK-BYTENB Timing

4.1.12.4 Disk Write Clocks

The SERVO CLOCK from the drive is delayed and then transmitted as the WRITE CLOCK to the drive. The delay is set to equal the propagation delay of the CRC circuit. The WRITE CLOCK signal and the WRITE DATA signal must have the relationship shown in Figure 4-7. The trailing edge of WRITE CLOCK must occur in the middle of the data cell of both the WRDATA and the CRC check word.

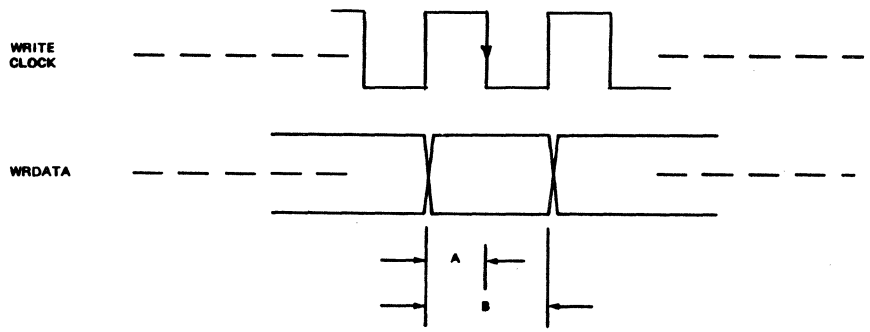


Figure 4-7. Disk Write Timing

4.1.12.5 Sector Beginning Format Operations

This timing shows in greater detail (see Figure 4-8) the relationship between the various sector format signals, as created by the micro-engine, at the beginning of the sector. Note that the micro-engine has no idea of the direction of transfer, and therefore issues timing signals for both the read and write transfers. When the sector counter equals the requested sector number, a SECEQU (Sector Equal) pulse is issued. At the next byte, the WRGATE (Write Gate) signal goes high and the CRCLR (CRC Clear) signal is dropped. One byte later the RDGATE (Read Gate) signal goes high. Twelve bytes after read gate, OG (Output Gate) is raised. This signal enables the transfer of data to/from the RAM. After OG is asserted, if it is a write operation, a "sentinel" bit is written; if it is a read, the BYTCLK is disabled until the sentinel bit is detected. The

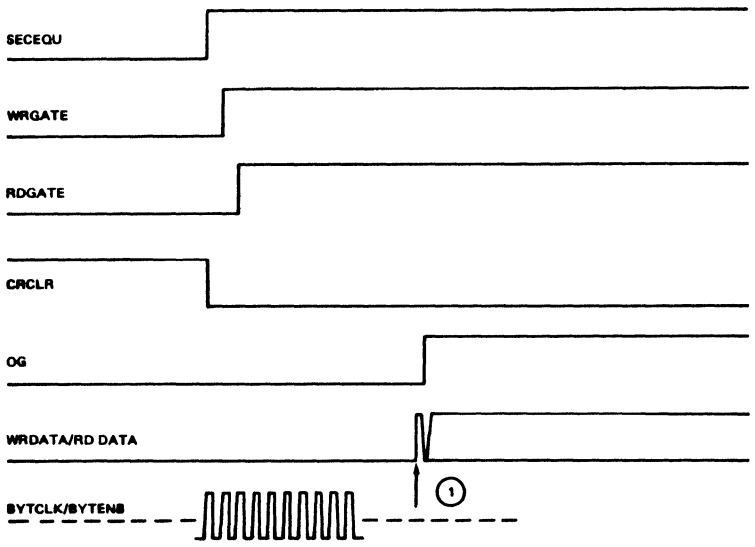


Figure 4-8. Sector Beginning Timing

sentinel bit is the indicator of the physical beginning of the sector. It is written out on the twelfth byte so that during a read, when the absolute timing from the sector pulse to the first bit of data is not known, the data bit cells can be synchronized. This means that the sentinel bit is written so that during a read the byte is synchronized such that bit 0 is interpreted as bit 0 and not as any other bit.

4.1.12.6 Sector End Format Operations

This timing shows (see Figure 4-9) in greater detail the relationship between the sector format signals at the end of a sector. After 512 bytes of data have been transferred into RAM (one per BYTCLK/$\overline{\text{BYTENB}}$) the CWEN (Check Word Enable) signal goes high causing the CRC generator to output the current check word if a write is occurring. During a read, the CWEN signal is ignored and the check word is entered into the serial data stream to be checked by the CRC chip. At the end of this time the CRC generator will issue a CRCERR (CRC Error) signal if an error in receiving occurred. A tranmsit CRC error is impossible. OG (Output Gate) drops at the end of the CRC field, shutting off further data transfers to RAM. RDGATE (Read Gate) is dropped after OG to insure that no glitches enter into the serial data stream, and WRGATE (Write Gate) drops several bytes later to insure

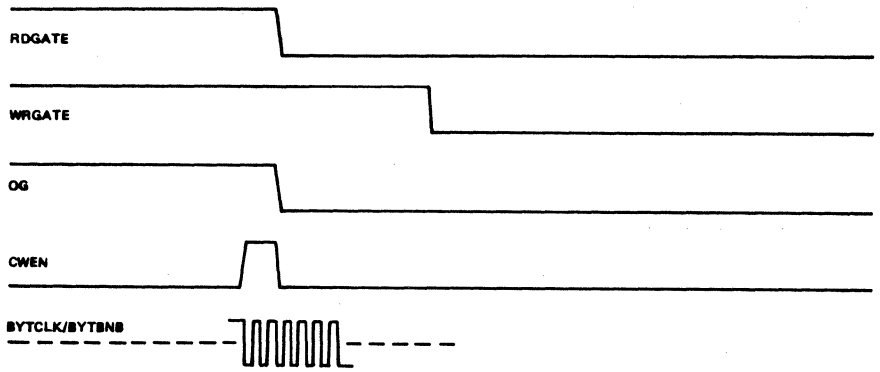


Figure 4-9. Sector End Format Timing

to insure that the data stream after the CRC check word is zero. A short while later, the next sector pulse, defining the next sector occurs and SECEQU also drops. The DONE signal will have occurred coincident with the falling edge of OG causing the DMA cycle to end and return bus control back to the on-board CPU.

4.1.12.7 DMA Transfer Operations

The whole process of transferring data to or from the RAM, to or from the board, is done as a DMA cycle. The CPU sets up the board for the transfer, sets the DMA address and word counts, sets the read/write bit for transfer into or out of the AM-420, and then sets the GO bit and either the DISK bit or the S-100 bit. These three bits, (DIS, S-100 and $\overline{RD}$/WR) cause the DMA cycle to follow the correct path. The IC's U18 and U19 steer the DMA logic to provide the requested transfer. U18 is used for a disk type transfer, while U19 is used for the S-100 type transfer. For any of the four types of transfers, RAM to S-100, S-100 to RAM, RAM to disk, or disk to RAM, the process is to set the three bits in the registers ($\overline{RD}$/WR, DISK, or S-100) and issue a GO command. The DMA hardware takes care of the rest of the process. Each byte is transferred into or out of RAM via one of two signals: BYTENB or 02ENB (phase 2 Enable). BYTENB is used for a

disk type transfer, and 02ENB is used for the S-100 type transfers. Each signal was designed to be no less than 200ns, or the access time of the RAMs. To this end the signal 02ENB is one whole cycle of the 4MHz master clock. When the system CPU reads from or writes to the AM-420 data ports, a DATRD (Data Read) or DATWRT (Data Write) pulse occurs. These signals are OR'ed to cause a SDREQ (S-100 DMA Request) which forces JK flip-flop U17 to toggle, creating 02ENB.

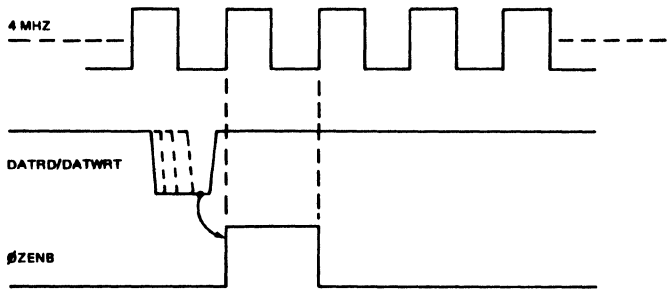


Figure 4-10. DMA Transfer Timing

4.2 CIRCUIT MODULE DESCRIPTION

This section describes the operation of the individual circuit packages (DIPS) contained on the AM-420 circuit board. Most of the processing is handled by the CPU and DMA address generator modules, so these are described in detail. The control logic and interface modules are also described with logic and connection diagrams for each one.

4.2.1 CPU Microprocessor (U11).

The CPU microprocessor is a single DIP module that handles the data processing of the AM-420 circuit board.

Figure 4-11 is a block diagram of the CPU, and Figure 4-12 details the internal register configuration which contains 208 bits of Read/Write memory that are accessible to the programmer. The registers include two sets of six general purpose registers that may be used individually as 8-bit registers or as 16-bit register pairs.

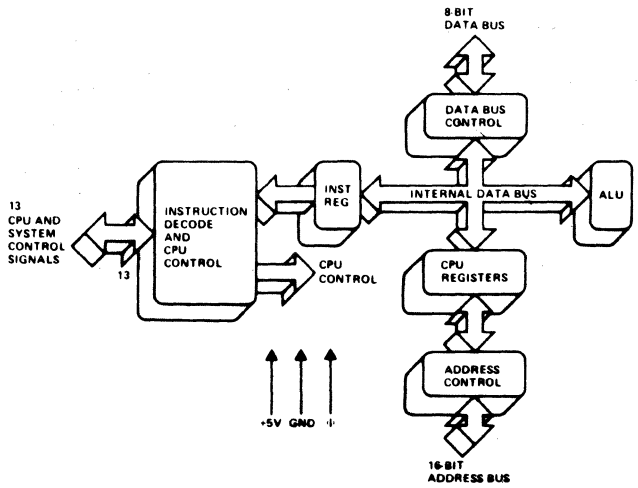


Figure 4-11. CPU Block Diagram

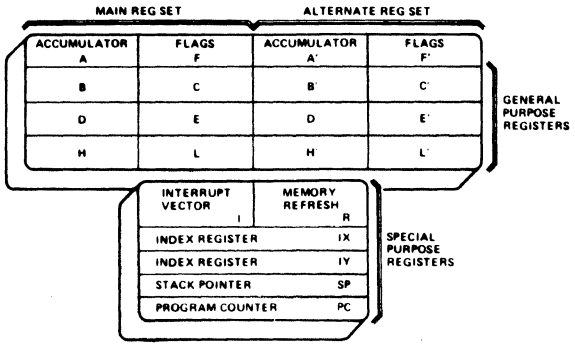


Figure 4-12. CPU Registers

Figure 4-13 shows the CPU pin in figuration and Table 4-6 contains a list of the CPU signals.

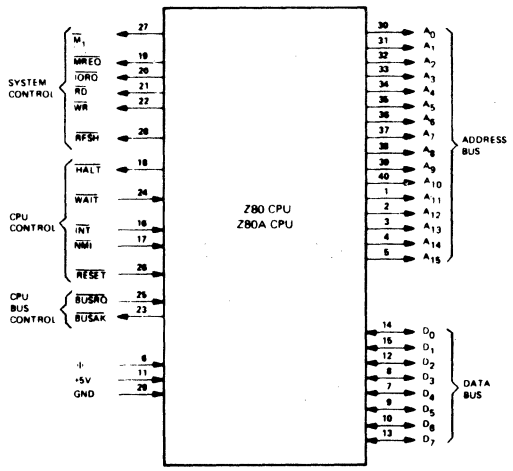


Figure 4-13. CPU Pin Configuration

Table 4-6. CPU Signal List

SIGNAL	PIN	FUNCTION
A0-15 ADDRESS BUS		Tri-state output, active high. A0-A15 constitute a 16-bit address bus. The address bus provides the address for memory (up to 64K bytes) data exchanges and for I/O device data exchanges.
D0-D7 DATA BUS		Tri-state input/output, active high. D0-D7 constitute an 8-bit bidirectional data bus. The data bus is used for data exchanges with memory and I/O devices.
$\overline{M1}$ MACHINE CYCLE ONE	27	Output, active low. $\overline{M1}$ indicates that the current machine cycle is the OP code fetch cycle of an instruction execution.
$\overline{MREQ}$ MEMORY REQUEST	19	Tri-state output, active low. The memory request signal indicates that the address bus holds a valid address for a memory read or memory write operation.
$\overline{IORQ}$ INPUT/OUTPUT REQUEST	20	Tri-state output, active low. The $\overline{IORQ}$ signal indicates that the lower half of the address bus holds a valid I/O address for an I/O read or write operation. An IORQ signal is also generated when an interrupt is being acknowledged to indicate that an interrupt response vector can be placed on the data bus.

Table 4-6 (Con't). CPU Signal List

SIGNAL	PIN	FUNCTION
$\overline{RD}$ MEMORY READ	21	Tri-state output, active low. $\overline{RD}$ indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O device or memory should use this signal to gate data onto the CPU data bus.
$\overline{WR}$ MEMORY WRITE	22	Tri-state output, active low. $\overline{WR}$ indicates that the CPU data bus holds valid data to be stored in the addressed memory or I/O device.
$\overline{RFSH}$ REFRESH	28	Output, active low. $\overline{RFSH}$ indicates that the lower 7 bits of the address bus contain a refresh address for dynamic memories and the current MREQ signal should be used to do a refresh read to all dynamic memories.
$\overline{HALT}$ HALT STATE	18	Output, active low. $\overline{HALT}$ indicates that the CPU has executed a $\overline{HALT}$ software instruction and is awaiting either a nonmaskable or a maskable interrupt (with the mask enabled) before operation can resume. While halted, the CPU executes NOP's to maintain memory refresh activity.

Table 4-6 (Con't). CPU Signal List

SIGNAL	PIN	FUNCTION
$\overline{\text{WAIT}}$ WAIT	24	Input, active low. $\overline{\text{WAIT}}$ indicates to the CPU that the addressed memory or I/O devices are not ready for a data transfer. The CPU continues to enter wait states for as long as this signal is active.
$\overline{\text{INT}}$ INTERRUPT REQUEST	16	Input, active low. The Interrupt Request signal is generated by I/O devices. A request will be honored at the end of the current instruction if the internal software controlled interrupt enable flip-flop (IFF) is enabled.
$\overline{\text{NMI}}$ NON MASKABLE INTERRUPT	17	Input, active low. The non-maskable interrupt request line has a higher priority than $\overline{\text{INT}}$ and is always recognized at the end of the status of the interrupt enable flip-flop. NMI automatically forces the CPU to restart to location 0066H.
$\overline{\text{RESET}}$	26	Input, active low. $\overline{\text{RESET}}$ initializes the CPU as follows: reset interrupt enable flip-flop, clear PC and registers I and R and set interrupt to 8080A mode. During reset time, the address and data bus go to a high impedance state and all control output signals go to the inactive state.

Table 4-6 (Con't). CPU Signal List

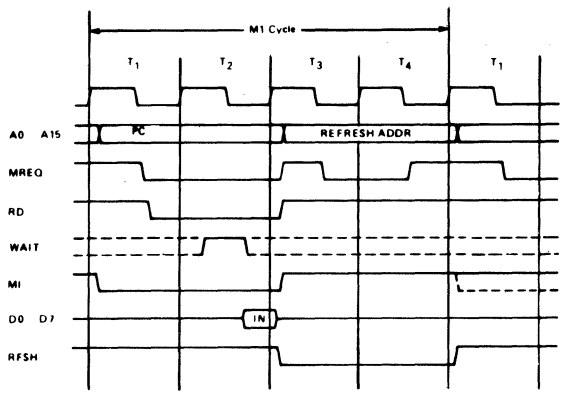
SIGNAL	PIN	FUNCTION
$\overline{\text{BUSRQ}}$ BUS REQUEST	25	Input, active low. The bus request signal has a higher priority than $\overline{\text{NMI}}$ and is always recognized at the end of the current machine cycle and is used to request the CPU address bus, data bus and tri-state output control signals to go to a high impedance state so that other devices can control these busses.
$\overline{\text{BUSAK}}$ BUS ACKNOWLEDGE	23	Output, active low. Bus acknowledge is used to indicate to the requesting device that the CPU address bus, data bus and tri-state control bus signals have been set to their high impedance state and the external device can now control these signals.

There are also two sets of accumulator and flag registers. The programmer has access to either set of main or alternate registers through a group of exchange instructions. This alternate set allows foreground/background mode of operation or may be reserved for very fast interrupt response. Each CPU also contains a 16-bit stack pointer which permits simple implementation of multiple level interrupts, unlimited subroutine nesting and simplification of many types of data handling.

The two 16-bit index registers allow tabular data manipulation and easy implementation of relocatable code. The Refresh register provides for automatic, totally transparent refresh of external dynamic memories. The I register is used in a powerful interrupt response mode to form the upper 8 bits of a pointer to an interrupt service address table, while the interrupting device supplies the lower 8 bits of the pointer. An indirect call is then made to this service address.

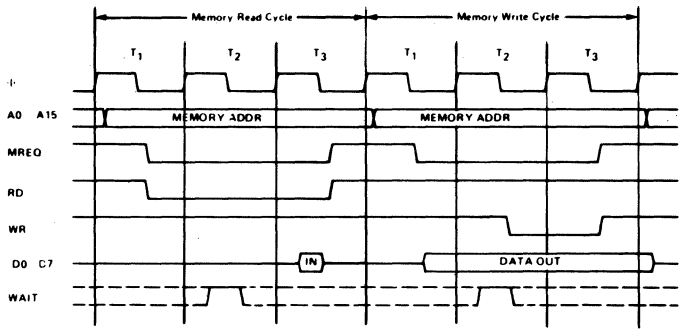
4.2.1.1 Instruction Op-Code Fetch

The program counter content (PC) is placed on the address bus immediately at the start of the cycle. One half clock time later $\overline{\text{MREQ}}$ goes active. The falling edge of $\overline{\text{MREQ}}$ can be used directly as a chip enable to dynamic memories. $\overline{\text{RD}}$ when active indicates that the memory data should be enabled onto the CPU data bus. The CPU samples data with the rising edge of the clock state T3. Clock states T3 and T4 of a fetch cycle are used to refresh dynamic memories while the CPU is internally decoding and executing the instruction. The refresh control signal $\overline{\text{RFSH}}$ indicates that a refresh read of all dynamic memories should be accomplished.



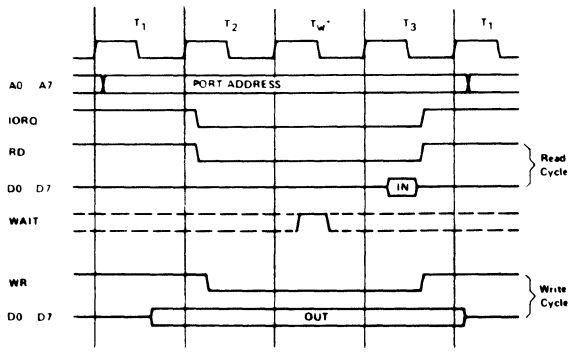
4.2.1.2 Memory Read Or Write Cycles

Illustrated here is the timing of memory read or write cycles other than an OP code fetch (M1 cycle). The $\overline{\text{MREQ}}$ and $\overline{\text{RD}}$ signals are used exactly as in the fetch cycle. In the case of a memory write cycle, the $\overline{\text{MREQ}}$ also becomes active when the address bus is stable so that it can be used directly as a chip enable for dynamic memories. The $\overline{\text{WR}}$ line is active when data on the data bus is stable so that it can be used directly as an R/W pulse to virtually any type of semiconductor memory.



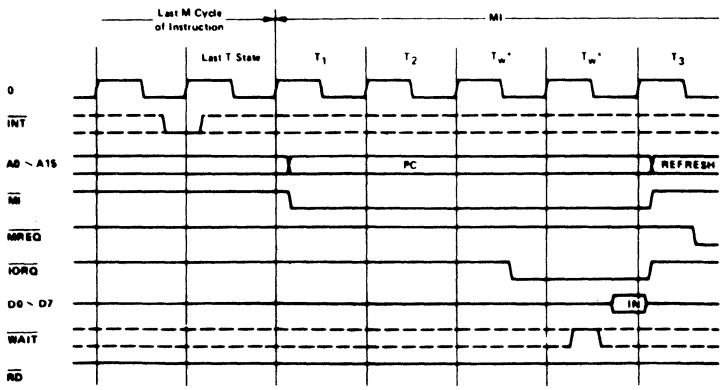
4.2.1.3 Input Or Output Cycles

Illustrated here is the timing for an I/O read or I/O write operation. Notice that during I/O operations a single wait state is automatically inserted (Tw*). The reason for this is that during I/O operations this extra state allows sufficient time for an I/O port to decode its address and activate the $\overline{WAIT}$ line if a wait is required.



4.2.1.4 Interrupt Request/Acknowledge Cycle

The interrupt signal is sampled by the CPU with the rising edge of the last clock at the end of any instruction. When an interrupt is accepted, a special M1 cycle is generated. During this M1 cycle, the $\overline{IORQ}$ signal becomes active (instead of $\overline{MREQ}$) to indicate that the interrupting device can place an 8-bit vector on the data bus. Two wait states (Tw*) are automatically added to this cycle so that a ripple priority interrupt scheme, such as the one used in the peripheral controller, can be easily implemented.



4.2.1.5 CPU Instruction Set

The following is a summary of the CPU instruction set showing the assembly language mnemonic and the symbolic operation performed by the instruction. The instructions are divided into the following categories:

- 8-bit loads
- 16-bit loads
- Exchanges
- Memory Block Moves
- Memory Block Searche
- 8-bit arithmetic andic
- 16-bit arithmetic
- General Purpose Accumulator & Flag Operations
- Miscellaneous Group
- Rotates and Shifts
- Bit Set, Reset and Test
- Input and Output
- Jumps
- Calls
- Restarts
- Returns

In Table 4-7, the following terminology is used:

- b ≡ a bit number in any 8-bit register or memory location
- cc ≡ flag condition code
  - NZ ≡ non zero
  - Z ≡ zero
  - NC ≡ non carry
  - C ≡ carry
  - PO ≡ Parity odd or no over flow
  - PE ≡ Parity even or over flow
  - P ≡ Positive
  - M ≡ Negative (minus)
- d ≡ any 8-bit destination register or memory location
- dd ≡ any 16-bit destination register or memory location
- e ≡ 8-bit signed 2's complement displacement used in relative jumps and indexed addressing
- L ≡ 8 special call locations in page zero. In decimal notation these are 0, 8, 16, 24, 32, 40, 48 and 56
- n ≡ any 8-bit binary number
- nn ≡ any 16-bit binary number
- r ≡ any 8-bit general purpose register (A, B, C, D, E, H, or L)
- s ≡ any 8-bit source register or memory location
- s_b ≡ a bit in a specific 8-bit register or memory location
- ss ≡ any 16-bit source register or memory location
- subscript "L" ≡ the low order 8 bits of a 16-bit register
- subscript "H" ≡ the high order 8 bits of a 16-bit register
- ( ) ≡ the contents within the ( ) are to be used as a pointer to a memory location or I/O port number

8-bit registers are A, B, C, D, E, H, L, I and R
16-bit register pairs are AF, BC, DE and HL
16-bit registers are SP, PC, IX and IY

Addressing Modes implemented include combinations of the following:

- Immediate
- Immediate extended
- Modified Page Zero
- Relative
- Extended
- Indexed
- Register
- Implied
- Register Indirect
- Bit

Table 4-7. CPU Instruction Set

	Mnemonic	Symbolic Operation	Comments
8-BIT LOADS	LD r, s	$r \leftarrow s$	s ≡ r, n, (HL), (IX+e), (IY+e)
	LD d, r	$d \leftarrow r$	d ≡ (HL), r (IX+e), (IY+e)
	LD d, n	$d \leftarrow n$	d ≡ (HL), (IX+e), (IY+e)
	LD A, s	$A \leftarrow s$	s ≡ (BC), (DE), (nn), I, R
	LD d, A	$d \leftarrow A$	d ≡ (BC), (DE), (nn), I, R
16-BIT LOADS	LD dd, nn	$dd \leftarrow nn$	dd ≡ BC, DE, HL, SP, IX, IY
	LD dd, (nn)	$dd \leftarrow (nn)$	dd ≡ BC, DE, HL, SP, IX, IY
	LD (nn), ss	$(nn) \leftarrow ss$	ss ≡ BC, DE, HL, SP, IX, IY
	LD SP, ss	$SP \leftarrow ss$	ss = HL, IX, IY
	PUSH ss	$(SP-1) \leftarrow ss_H$; $(SP-2) \leftarrow ss_L$	ss = BC, DE, HL, AF, IX, IY
	POP dd	$dd_L \leftarrow (SP)$; $dd_H \leftarrow (SP+1)$	dd = BC, DE, HL, AF, IX, IY
EXCHANGES	EX DE, HL	$DE \leftrightarrow HL$	
	EX AF, AF'	$AF \leftrightarrow AF'$	
	EXX	$\begin{pmatrix} BC \\ DE \\ HL \end{pmatrix} \leftrightarrow \begin{pmatrix} BC' \\ DE' \\ HL' \end{pmatrix}$	
	EX (SP), ss	$(SP) \leftrightarrow ss_L$, $(SP+1) \leftrightarrow ss_H$	ss ≡ HL, IX, IY
MEMORY BLOCK MOVES	LDI	$(DE) \leftarrow (HL)$, $DE \leftarrow DE+1$, $HL \leftarrow HL+1$, $BC \leftarrow BC-1$	
	LDIR	$(DE) \leftarrow (HL)$, $DE \leftarrow DE+1$, $HL \leftarrow HL+1$, $BC \leftarrow BC-1$, Repeat until BC = 0	
	LDD	$(DE) \leftarrow (HL)$, $DE \leftarrow DE-1$, $HL \leftarrow HL-1$, $BC \leftarrow BC-1$	
	LDDR	$(DE) \leftarrow (HL)$, $DE \leftarrow DE-1$, $HL \leftarrow HL-1$, $BC \leftarrow BC-1$, Repeat until BC = 0	

Table 4-7. (Cont.). CPU Instruction Set

	Mnemonic	Symbolic Operation	Comments
MEMORY BLOCK SEARCHES	CPI	A-(HL), HL ← HL+1 BC ← BC-1	
	CPIR	A-(HL), HL ← HL+1 BC ← BC-1, Repeat until BC = 0 or A = (HL)	A-(HL) sets the flags only. A is not affected
	CPD	A-(HL), HL ← HL-1 BC ← BC-1	
	CPDR	A-(HL), HL ← HL-1 BC ← BC-1, Repeat until BC= 0 or A = (HL)	
8-BIT ALU	ADD s	A ← A + s	
	ADC s	A ← A + s + CY	CY is the carry flag
	SUB s	A ← A - s	
	SBC s	A ← A - s - CY	s ≡ r, n, (HL) (IX+e), (IY+e)
	AND s	A ← A ∧ s	
	OR s	A ← A ∨ s	
	XOR s	A ← A ⊕ s	
	CP s	A - s	s = r, n (HL) (IX+e), (IY+e)
	INC d	d ← d + 1	d = r, (HL) (IX+e), (IY+e)
	DEC d	d ← d - 1	
16-BIT ARITHMETIC	ADD HL, ss	HL ← HL + ss	ss ≡ BC, DE HL, SP
	ADC HL, ss	HL ← HL + ss + CY	
	SBC HL, ss	HL ← HL - ss - CY	
	ADD IX, ss	IX ← IX + ss	ss ≡ BC, DE, IX, SP
	ADD IY, ss	IY ← IY + ss	ss ≡ BC, DE, IY, SP
	INC dd	dd ← dd + 1	dd ≡ BC, DE, HL, SP, IX, IY
	DEC dd	dd ← dd - 1	dd ≡ BC, DE, HL, SP, IX, IY
GP ACC. AND FLAG	DAA	Converts A contents into packed BCD following add or subtract.	Operands must be in packed BCD format
	CPL	$A \leftarrow \overline{A}$	
	NEG	A ← 00 – A	
	CCF	$CY \leftarrow \overline{CY}$	
	SCF	CY ← 1	

Table 4-7. (Cont.). CPU Instruction Set

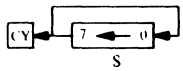
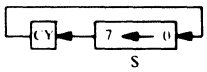
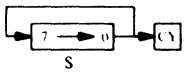
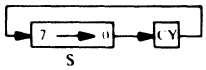
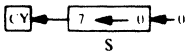
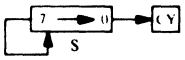
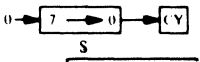
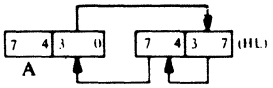
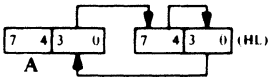
	Mnemonic	Symbolic Operation	Comments
MISCELLANEOUS	NOP	No operation	
	HALT	Halt CPU	
	DI	Disable Interrupts	
	EI	Enable Interrupts	
	IM 0	Set interrupt mode 0	8080A mode
	IM 1	Set interrupt mode 1	Call to 0038_H
	IM 2	Set interrupt mode 2	Indirect Call
ROTATES AND SHIFTS	RLC s		
	RL s		
	RRC s		
	RR s		
	SLA s		s ≡ r, (HL) (IX+e), (IY+e)
	SRA s		
	SRL s		
	RLD		
	RRD		
BITS S, R, AND T	BIT b, s	$Z \leftarrow \overline{s_b}$	Z is zero flag
	SET b, s	$s_b \leftarrow 1$	s ≡ r, (HL)
	RES b, s	$s_b \leftarrow 0$	(IX+e), (IY+e)
INPUT AND OUTPUT	IN A, (n)	A ← (n)	
	IN r, (C)	r ← (C)	Set flags
	INI	(HL) ← (C), HL ← HL + 1 B ← B - 1	
	INIR	(HL) ← (C), HL ← HL + 1 B ← B - 1 Repeat until B = 0	
	IND	(HL) ← (C), HL ← HL - 1 B ← B - 1	
	INDR	(HL) ← (C), HL ← HL - 1 B ← B - 1 Repeat until B = 0	

Table 4-7. (Cont.). CPU Instruction Set

	Mnemonic	Symbolic Operation	Comments
INPUT AND OUTPUT	OUT(n), A	(n) ← A	
	OUT(C), r	(C) ← r	
	OUTI	(C) ← (HL), HL ← HL + 1 B ← B - 1	
	OTIR	(C) ← (HL), HL ← HL + 1 B ← B - 1 Repeat until B = 0	
	OUTD	(C) ← (HL), HL ← HL - 1 B ← B - 1	
	OTDR	(C) ← (HL), HL ← HL - 1 B ← B - 1 Repeat until B = 0	
JUMPS	JP nn	PC ← nn	
	JP cc, nn	If condition cc is true PC ← nn, else continue	cc { NZ PO; Z PE; NC P; C M
	JR e	PC ← PC + e	
	JR kk, e	If condition kk is true PC ← PC + e, else continue	kk { NZ NC; Z C
	JP (ss)	PC ← ss	ss = HL, IX, IY
	DJNZ e	B ← B - 1, if B = 0 continue, else PC ← PC + e	
CALLS	CALL nn	(SP-1) ← PC_H (SP-2) ← PC_L, PC ← nn	
	CALL cc, nn	If condition cc is false continue, else same as CALL nn	cc { NZ PO; Z PE; NC P; C M
RESTARTS	RST L	(SP-1) ← PC_H (SP-2) ← PC_L, PC_H ← 0 PC_L ← L	
RETURNS	RET	PC_L ← (SP), PC_H ← (SP+1)	
	RET cc	If condition cc is false continue, else same as RET	cc { NZ PO; Z PE; NC P; C M
	RETI	Return from interrupt, same as RET	
	RETN	Return from non- maskable interrupt	

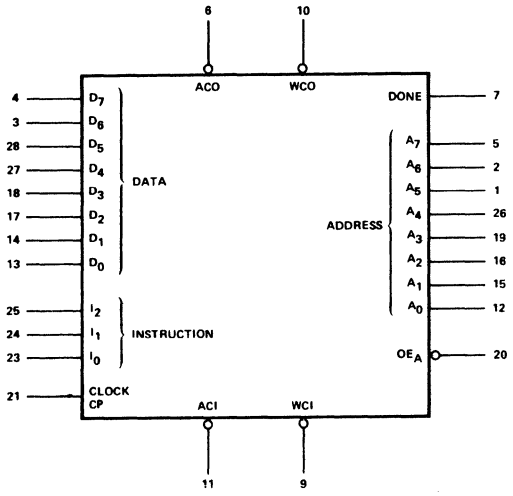
4.2.2 DMA Address Generator (U10, U21).

This device is a high-speed, 8-bit wide direct memory access address generator slice that can be cascaded to form larger addresses. Device connections are shown in Figure 4-14.

The primary function of the device is to generate sequential memory addresses for use in the sequential transfer of data to or from a memory. It also maintains a data word count and generates a DONE signal when a programmable terminal count has been reached. The device is designed for use in peripheral controllers with DMA capability or in any other system which transfers data to or from sequential locations of a memory.

The device can be programmed to increment or decrement the memory address in any of four control modes and executes eight different instructions. The initial address and word count are saved internally so that they can be restored later in order to repeat the data transfer operation.

Logic Symbol



Connection Diagram
Top View

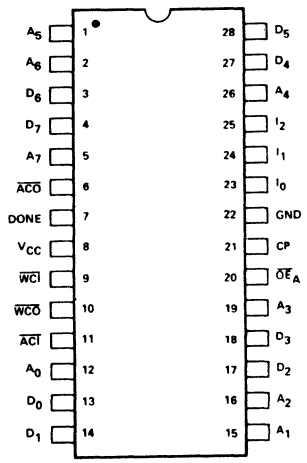


Figure 4-14. DMA Address Generator Connections

4.2.2.1 Architecture

As shown in Figure 4-15, the device consists of the following:

- A three-bit Control Register.
- An eight-bit Address Counter with input multiplexer.
- An eight-bit Address Register.
- An eight-bit Word Counter with input multiplexer.
- An eight-bit Word Count Register.
- Transfer complete circuitry.
- An eight-bit wide data multiplexer with three-state output buffers.
- Three-state address output buffers with external output enable control.
- An instruction decoder.

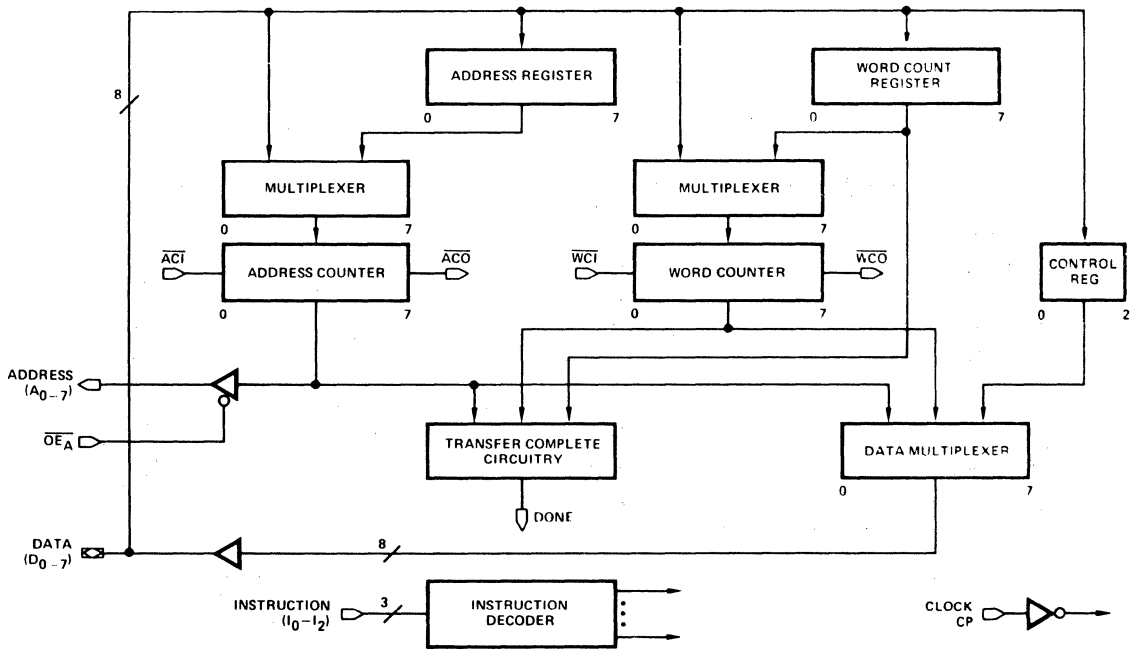


Figure 4-15. DMA Address Generator Block Diagram

Control Register. Under instruction control, the Control Register can be loaded or read from the bidirectional DATA lines DO-D7. Control Register bits 0 and 1 determine the Control Mode, and bit 2 determines whether the Address Counter increments or decrements. Figure 4-16 defines the Control Register format.

Control Register

CR_2	CR_1	CR_0

CR_1	CR_0	Control Mode Number	Control Mode Type	Word Counter	Done Output Signal
L	L	0	Word Count Equals One	Decrement	HIGH when Word Counter = 1
L	H	1	Word Count Compare	Increment	HIGH when Word Counter +1 equals Word Count Register
H	L	2	Address Compare	Hold	HIGH when Word Counter = Address Counter
H	H	3	Word Counter Carry out	Increment	Always LOW.

H = HIGH
L = LOW

CR_2	Address Counter
L	Increment
H	Decrement

Figure 4-16. Control Register Format Definition

Address Counter. The Address Counter, which provides the current memory address, is an eight-bit, binary, up/down counter with full look-ahead carry generation. The Address Carry Input (ACI) and Address Carry Output (ACO) allow cascading to accommodate larger addresses. Under instruction control, the Address Counter can be enabled, disabled, and loaded from the DATA inputs, DO-D7, or the Address Register. When enabled and the ACI input is LOW, the Address Counter increments/decrements on the LOW to HIGH transition of the CLOCK input, CP. The Address Counter output can be enabled onto the three-state ADDRESS outputs AO-A7 under control of the Output Enable input, OEA.

Address Register. The eight-bit Address Register saves the initial address so that it can be restored later in order to repeat a transfer operation. When the LOAD ADDRESS instruction is executed, the Address Register and Address Counter are simultaneously loaded from the DATA inputs, DO-D7.

Word Counter and Word Count Register. The Word Counter and Word Count Register, which maintain and save a word count, are similar in structure and operation to the Address Counter and Address Register, with the exception that the Word Counter increments in Control Modes 1 and 3, decrements in Control Mode 0, and is disabled in Control Mode 2. The LOAD WORD COUNT instruction simultaneously loads the Word Counter and Word Count Register.

Transfer Complete Circuitry. The Transfer Complete Circuitry is a combinational logic network which detects the completion of the data transfer operation in three control Modes and generates the DONE output signal. The DONE signal is an open-collector output, which can be dot-anded between chips.

Data Multiplexer. The Data Multiplexer is an eight-bit wide, 3-input multiplexer which allows the Address Counter, Word Counter, and Control Register to be read at the DATA lines, D0-D7. The Data Multiplexer and three-state Data output buffers are instruction controlled.

Address Output Buffers. The three-state Address Output Buffers allow the Address Counter output to be enabled onto the ADDRESS lines, A0-A7, under external control. When the Output Enable input, OEA, is LOW, the Address output buffers are enabled; when OEA is HIGH, the ADDRESS lines are in the high-impedance state. The address and Data Output Buffers can sink 24mA output current over the commercial operating range.

Instruction Decoder. The Instruction Decoder generates required internal control signals as a function of the INSTRUCTION inputs, I0-I2 and Control Register bits 0 and 1.

Clock. The CLOCK input, CP is used to clock the Address Register, Address Counter, Word Count Register, Word Counter, and Control Register, all on the LOW to HIGH transition of the CP signal.

4.2.2.2 Control Modes

Control Mode 0 - Word Count Equals One Mode. In this mode, the number of data words to be transferred is initially loaded into the Word Counter and Word Count Register. When the Word Counter is enabled and the Word Counter Carry-In, WCI, is LOW, the Word Counter decrements on the LOW to HIGH transition of the CLOCK input, CP. The DONE signal is generated during the last word transfer, i.e., when the Word Counter equals one.

Control Mode 1 - Word Count Compare Mode. Initially, the number of data words to be transferred is loaded into the Word Count Register and the Word Counter is cleared. When the Word Counter is enabled and the WCI input is LOW, the Word Counter increments on the LOW to HIGH transition of the CLOCK input, CP. In this mode, the Word Counter always indicates the number of data words that have been transferred. The Transfer Complete Circuitry compares the Word Counter with the Word Count Register and generates the DONE signal during the last word transfer; i.e., when the Word Counter plus one equals the Word Count Register.

Control Mode 2 - Address Compare Mode. In this mode, only an initial and final memory address need be specified. The initial Memory Address is loaded into the Address Register and Address Counter and the final memory address is loaded into the Word Count Register and Word Counter. The Word Counter is always disabled in this mode and serves as a holding register for the final memory address. When the Address Counter is enabled and the ACI input is LOW, the Address Counter increments or decrements (depending on Control Register bit 2) on the LOW to HIGH transition of the CLOCK input, CP. The Transfer Complete Circuitry compares the Address Counter with the Word Counter and generates the DONE signal during the last word transfer; i.e., when the Address Counter equals the Word Counter.

Control Mode 3 - Word Counter Carry Out Mode. For this mode of operation, the user can load the Word Count Register and Word Counter with the two's complement of the number of data words to be transferred. When the Word Counter is enabled and the WCI input is LOW, the Word Counter increments on the LOW to HIGH transition of the CLOCK input, CP. A Word Counter Carry Out signal, WCO, indicates the last data word is being transferred. The DONE signal is not required in this mode and, therefore, is always LOW.

4.2.2.3 Instructions

The instruction set consists of eight instructions. Six instructions load and read the Address Counter, Word Counter and Control Register; one instruction enables the Address and Word counters, and one instruction reinitializes the Address and Word counters. The function of the REINITIALIZE COUNTERS, LOAD WORD COUNT, and ENABLE COUNTERS instructions varies with the Control Mode being utilized. Table 4-8 defines the instructions as a function of instruction inputs I0-I2 and the four Control Modes.

Table 4-8. DMA Register Instructions

I_2 I_1 I_0	Octal Code	Function	Mnemonic	Control Mode	Word Reg.	Word Counter	Address Reg.	Address Counter	Control Register	Data D_0-D_7
L L L	0	WRITE CONTROL REGISTER	WRCR	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	D_0-D_2→CR	INPUT
L L H	1	READ CONTROL REGISTER	RDCR	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	HOLD	CR→D_0-D_2 (Note 1)
L H L	2	READ WORD COUNTER	RDWC	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	HOLD	WC→D
L H H	3	READ ADDRESS COUNTER	RDAC	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	HOLD	AC→D
H L L	4	REINITIALIZE COUNTERS	REIN	0, 2, 3	HOLD	WCR→WC	HOLD	AR→AC	HOLD	Z
				1	HOLD	ZERO→WC	HOLD	AR→AC	HOLD	Z
H L H	5	LOAD ADDRESS	LDAD	0, 1, 2, 3	HOLD	HOLD	D→AR	D→AC	HOLD	INPUT
H H L	6	LOAD WORD COUNT	LDWC	0, 2, 3	D→WR	D→WC	HOLD	HOLD	HOLD	INPUT
				1	D→WR	ZERO→WC	HOLD	HOLD	HOLD	INPUT
H H H	7	ENABLE COUNTERS	ENCT	0, 1, 3	HOLD	ENABLE COUNT	HOLD	ENABLE COUNT	HOLD	Z
				2	HOLD	HOLD	HOLD	ENABLE COUNT	HOLD	Z

CR = Control Reg. WCR = Word Count Reg. L = LOW
AR = Address Reg. WC = Word Counter H = HIGH
AC = Address Counter D = Data Z = High Impedance

Note 1:
Data Bits D_3-D_7 are high during this instruction.

The WRITE CONTROL REGISTER instruction writes DATA input D0-D2 into the Control Register; DATA inputs D3-D7 are "don't care" inputs for this instruction. The READ CONTROL REGISTER instruction gates the Control Register outputs to DATA lines, D0-D2. DATA lines D3-D7 are in the HIGH state during this instruction.

The Word Counter can be read using the READ WORD COUNTER instruction, which gates the Word Counter outputs to DATA lines D0-D7. The LOAD WORD COUNT instruction is Control Mode dependent. In Control Modes 0, 2, and 3, DATA inputs D0-D7 are written into both the Word Count Register and Word Counter. In Control Mode 1, DATA inputs D0-D7 are written into the Word Count Register and the Word Counter is cleared.

The READ ADDRESS COUNTER instruction gates the Address Counter outputs to DATA lines D0-D7, and the LOAD ADDRESS instruction writes DATA inputs D0-D7 into both the Address Register and Address Counter.

In Control Modes 0, 1, and 3, the ENABLE COUNTERS instruction enables both the Address and Word Counters; in Control Mode 2, the Address Counter is enabled and the Word Counter holds its contents. When enabled and the carry input is active, the counter increment on the LOW to HIGH transition of the CLOCK input, CP. Thus, with this instruction applied, counting can be controlled by the carry inputs.

The REINITIALIZE COUNTERS instruction also is Control Mode dependent. In Control Modes 0, 1, and 3, the contents of the Address Register and Word Count Register are transferred to the respective Address Counter and Word Counter; in Control Mode 1, the content of the Address Register is transferred to the Address Counter and the Word Counter is cleared. The REINITIALIZE COUNTERS instruction allows a data transfer operation to be repeated without reloading the address and word count from the DATA lines.

4.2.3 Cyclic Redundancy Check (CRC) Generator/Checker (U15).
Cyclic Redundancy Check (CRC) Generator/Checker is a 16-bit programmable device which operates on serial data streams and provides a means of detecting transmission errors. Cyclic encoding

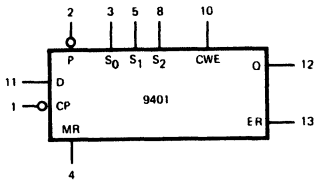
and decoding schemes for error detection are based on polynomial manipulation in modulo arithmetic. For encoding, the data stream (message polynomial) is divided by a selected polynomial. This division results in a remainder which is appended to the message as check bits. For error checking, the bit stream containing both data and check bits is divided by the same selected polynomial. If there are no detectable errors, this division results in a zero remainder. Although it is possible to choose many generating polynomials of a given degree, standards exist that specify a small number of useful polynomials. This device implements the polynomials listed in Table 4-10 by applying the appropriate logic levels to the select pin S0, S1 and S2. The CRC connections are shown in Figure 4-17.

The device consists of a 16-bit register, a Read Only Memory (ROM) and associated control circuitry as shown in the Block Diagram. The polynomial control mode presented at inputs S0, S1 and S2 is decoded by the ROM, selecting the desired polynomial by establishing shift mode operation on the register with Exclusive OR gates at appropriate inputs. To generate the check bits, the data stream is entered via the Data Inputs (D), using the HIGH to LOW transition of the Clock Input (CP). This data is gated with the most significant Output (Q) of the register, and controls the Exclusive OR gates (Figure 4-18). The Check Word Enable (CWE) must be held HIGH while the data is being entered. After the last bit is entered, the CWE is brought LOW and the check bits are shifted out of the register and appended to the data bits using external gating (Figure 4-19).

To check an incoming message for errors, both the data and check bits are entered through the D Input with the CWE Input held high. The device is not in the data path, but only monitors the message. The Error Output becomes valid after the last check bit has been entered into the device by a HIGH to LOW transition of CP. If no detectable errors have occurred during the data transmission, the resultant internal register bits are all LOW and the Error Output (ER) is LOW. If a detectable error has occurred, ER is HIGH; ER remains valid until the next HIGH to LOW transition of CP or until the device has been preset or reset.

A HIGH on the Master Reset Input (MR) asynchronously clears the register. A LOW on the Preset Input (P) asynchronously sets the entire register if the control code inputs specify a 16-bit polynomial; in the case of 12 or 8-bit check polynomials, only the most significant 12 or 8 register bits are set, and the remaining bits are cleared.

LOGIC SYMBOL

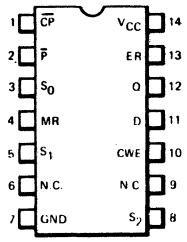


V_{CC} = Pin 14
GND = Pin 7

PIN NAMES

$S_0 - S_2$	Polynomial Select Inputs
D	Data Input
$\overline{CP}$	Clock (Operates on HIGH-to-LOW Transition) Input
CWE	Check Word Enable Input
$\overline{P}$	Preset (Active LOW) Input
MR	Master Reset (Active HIGH) Input
Q	Data Output (Note b)
ER	Error Output (Note b)

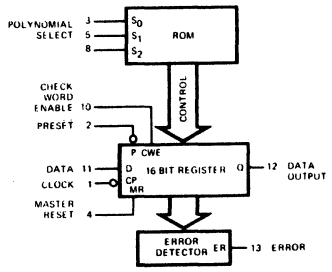
CONNECTION DIAGRAM
DIP (TOP VIEW)



Pins 6 and 9 not connected.

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

BLOCK DIAGRAM



V_{CC} = Pin 14
GND = Pin 7

Figure 4-17. CRC Checker Connections

Table 4-9. CRC Polynomial Select Codes

SELECT CODE			POLYNOMIAL	REMARKS
S_2	S_1	S_0		
L	L	L	$X^{16}+X^{15}+X^2+1$	CRC-16
L	L	H	$X^{16}+X^{14}+X+1$	CRC-16 REVERSE
L	H	L	$X^{16}+X^{15}+X^{13}+X^7+X^4+X^2+X^1+1$	
L	H	H	$X^{12}+X^{11}+X^3+X^2+X+1$	CRC-12
H	L	L	$X^8+X^7+X^5+X^4+X+1$	
H	L	H	X^8+1	LRC-8
H	H	L	$X^{16}+X^{12}+X^5+1$	CRC-CCITT
H	H	H	$X^{16}+X^{11}+X^4+1$	CRC-CCITT REVERSE

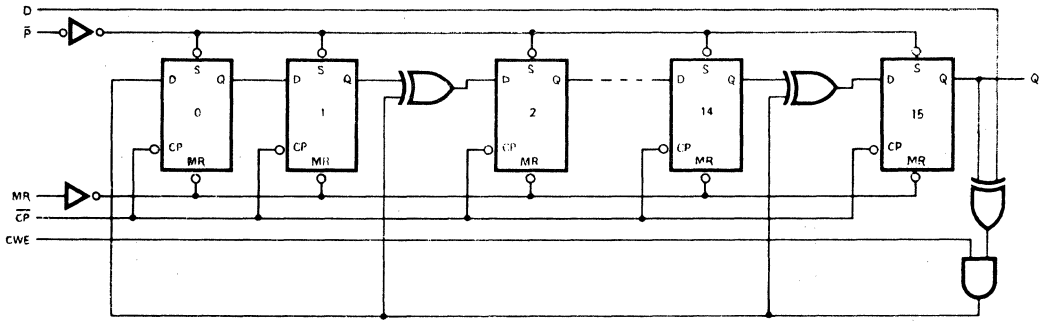
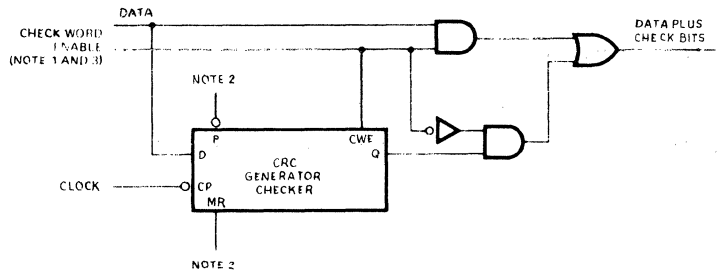


Figure 4-18. CRC Equivalent Circuit For $X^{16}+X^{15}+X^2+1$



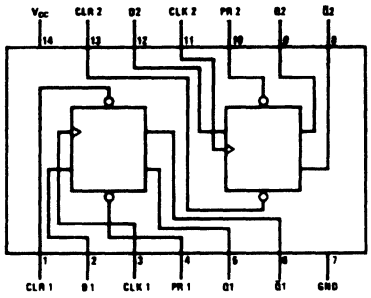
NOTES:
1. Check word Enable is HIGH while data is being clocked, LOW during transmission of check bits.
2. 9401 must be reset or preset before each computation.
3. CRC check bits are generated and appended to data bits.

Figure 4-19. CRC Check Word Generation

4.2.4 Positive-Edge-Triggered Flip-Flops with Preset and Clear (U5, U14, U53, U55, U62).

For logic and connections, see Figure 4-20.

Connection Diagram



Truth Table

INPUTS				OUTPUTS	
PR	CLR	CLK	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q0	$\bar{Q}$0

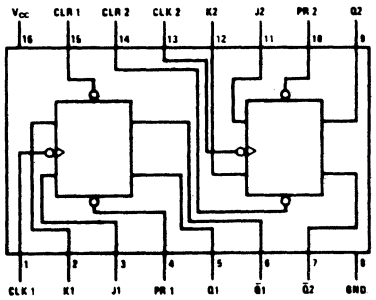
Notes. ⎍⎍ = high-level pulse; data inputs should be held constant while clock is high; data is transferred to output on the falling edge of the pulse.
Q0 = the level of Q before the indicated input conditions were established.
TOGGLE: Each output changes to the complement of its previous level on each active transition (pulse) of the clock.
*This configuration is nonstable, that is, it will not persist when preset and clear inputs return to their inactive (high) level.

Figure 4-20. Dual D Flip-Flop Connections

4.2.5 Dual J-K Negative-Edge-Triggered Flip-Flops with Preset and Clear (U17).

For device logic and connections, see Figure 4-21.

Connection Diagram



Truth Table

INPUTS					OUTPUTS	
PR	CLR	CLK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q0	$\bar{Q}$0
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q0	$\bar{Q}$0

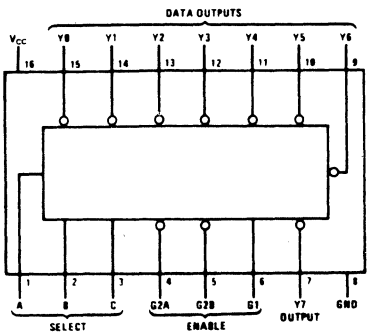
Notes. Q0 = the level of Q before the indicated input conditions were established.
TOGGLE: Each output changes to the complement of its previous level on each active transition of the clock.
*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

Figure 4-21. J-K Flip-Flop Connections

4.2.6 Decoder (U25, U26, U71).

These are Schottky-clamped circuits designed for memory-decoding or data-routing applications requiring very short propagation delay times. This DIP decodes one of eight lines based on the conditions at the three binary select inputs and the three enable inputs. For logic and connections, see Figure 4-22.

Connection and Logic Diagram



Truth Table

INPUTS					OUTPUTS							
ENABLE		SELECT										
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

*G2 = G2A + G2B

H = High level, L = low level, X = don't care

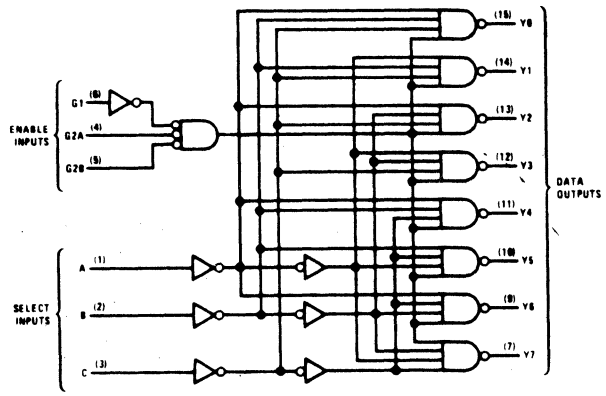
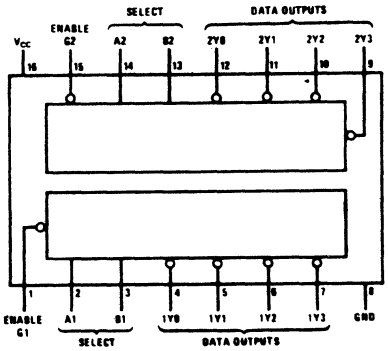


Figure 4-22. Decoder Connections

4.2.7 Decoder/Demultiplexer (U30).

These Schottky-clamped circuits are designed to be used in high performance memory decoding or data routing applications requiring very short propagation delay times. This device contains two separate two-line to four-line decoders in one package. The active-low enable input can be used as a data line in demultiplexing applications. The device features fully buffered inputs, presenting only one normalized load to its driving circuit. All inputs are clamped with high performance Schottky diodes to suppress line-ringing. For logic and connections, see Figure 4-23.

Connection Diagram



Truth Table

INPUTS			OUTPUTS			
ENABLE	SELECT					
G	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H = high level, L = low level, X = don't care

Logic Diagram

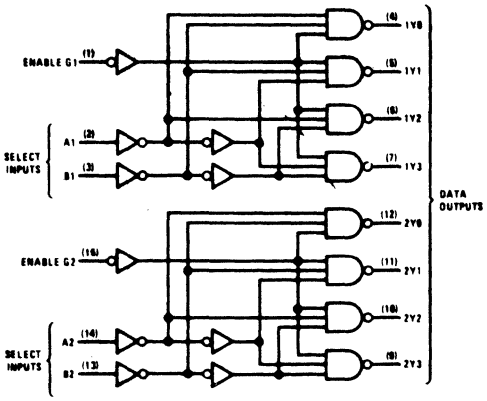
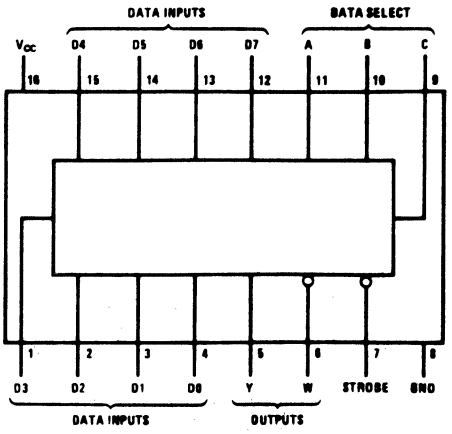


Figure 4-23. Decoder/Demultiplexer Connections

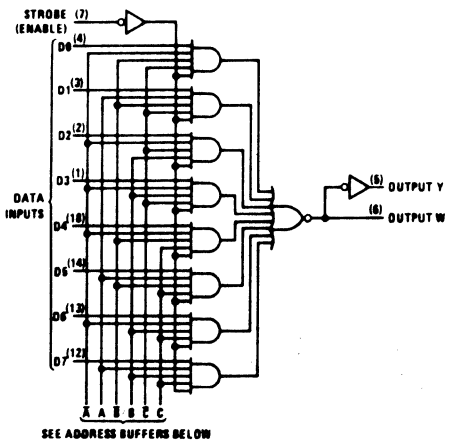
4.2.8 Data Selector/Multiplexer (U13).

This data selector/multiplexer contains full on-chip decoding to select one of eight data sources. A strobe input must be at a low logic level to enable the device. A high level at the strobe forces the W output high and the Y output low. See Figure 4-24 for logic and connections.

Connection Diagram



Logic Diagram



Truth Table

INPUTS				OUTPUTS	
SELECT			STROBE	Y	W
C	B	A	S		
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = High Level, L = Low Level, X = Don't Care

$\overline{E0}$, $\overline{E1}$ . . . $\overline{E15}$ = the complement of the level of the respective E input

D0, D1 . . . D7 = the level of the respective D input

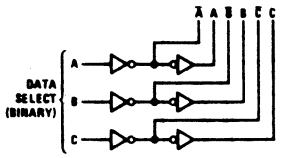
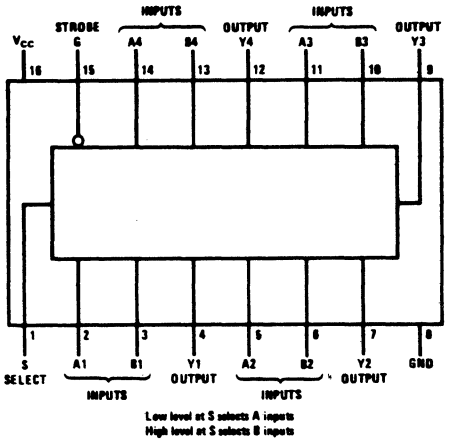


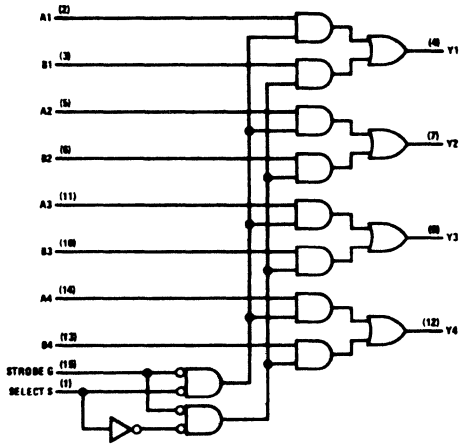
Figure 4-24. Data Selector/Multiplexer Logic and Connections

4.2.9 Quad Two-Line to One-Line Data Selector/Multiplexer (U61). This data selector/multiplexer contains drivers to supply full on-chip data selection to the four output gates. A separate strobe input is provided. A four-bit word is selected from one of two sources and is routed to the four inputs. For logic and connections see Figure 4-25.

Connection Diagram



Logic Diagram



Truth Table

INPUTS				OUTPUT Y
STROBE	SELECT	A	B	
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

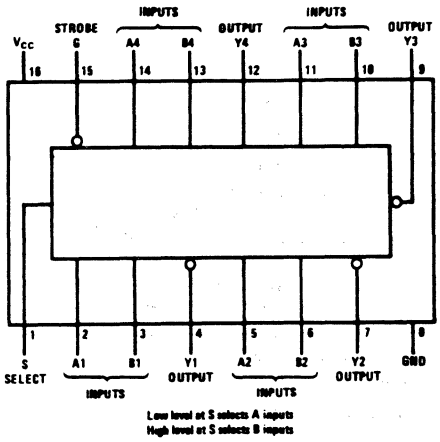
H = High Level, L = Low Level, X = Don't Care

Figure 4-25. Quad 2-Line to 1-line Data Selector/Multiplexer Connections

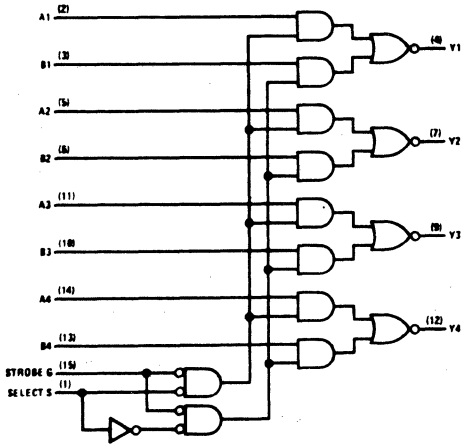
4.2.10 Quad Inverting Two-Line to One-Line Data Selector/Multiplexer (U18, U19).

This data selector/multiplexer contains inverters and drivers to supply full on-chip data selection to the four output gates. A separate strobe input is provided. A four-bit word is selected from one of two sources and is routed to the four inputs. For logic and connections see Figure 4-26.

Connection Diagram



Logic Diagram



Truth Table

INPUTS				OUTPUT Y
STROBE	SELECT	A	B	
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = High Level, L = Low Level, X = Don't Care

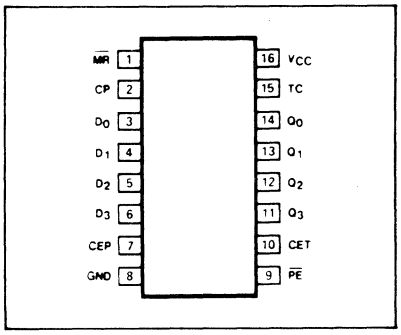
Figure 4-26. Quad Inverting 2-Line to 1-Line Data Selector/Multiplexer Connections

4.2.11 Four-Bit Binary Counter With Asynchronous Clear (U75).
This device is a synchronous, presettable, 4-bit binary counter featuring an internal carry look-ahead for applications in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the positive-going edge of the clock.

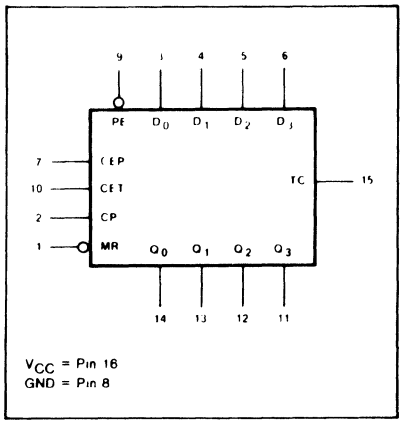
The counter is fully programmable; that is, the outputs may be preset to either level. Presetting is synchronous with the clock, and takes place regardless of the levels of the count enable inputs. A LOW level on the Parallel Enable ($\overline{PE}$) input disables the counter and causes the data at the D inputs to be loaded into the counter on the next LOW-to-HIGH transition of the clock. The reset (clear) function is asynchronous. A LOW level on the Master Reset ($\overline{MR}$) input sets all four of the flip-flop outputs LOW, regardless of the levels of the CP, $\overline{PE}$, CET, and CEP inputs.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two Count Enable inputs (CET * CEP) and a Terminal Count (TC) output. Both count enable inputs must be HIGH to count. The CET input is fed forward to enable the TC output. The TC output thus enabled, will produce a HIGH level portion of the Q output. This HIGH level TC pulse is used to enable successive cascading stages. For logic, connections, and timing, see Figure 4-27.

Pin Configuration



Logic Symbol



Logic Diagram

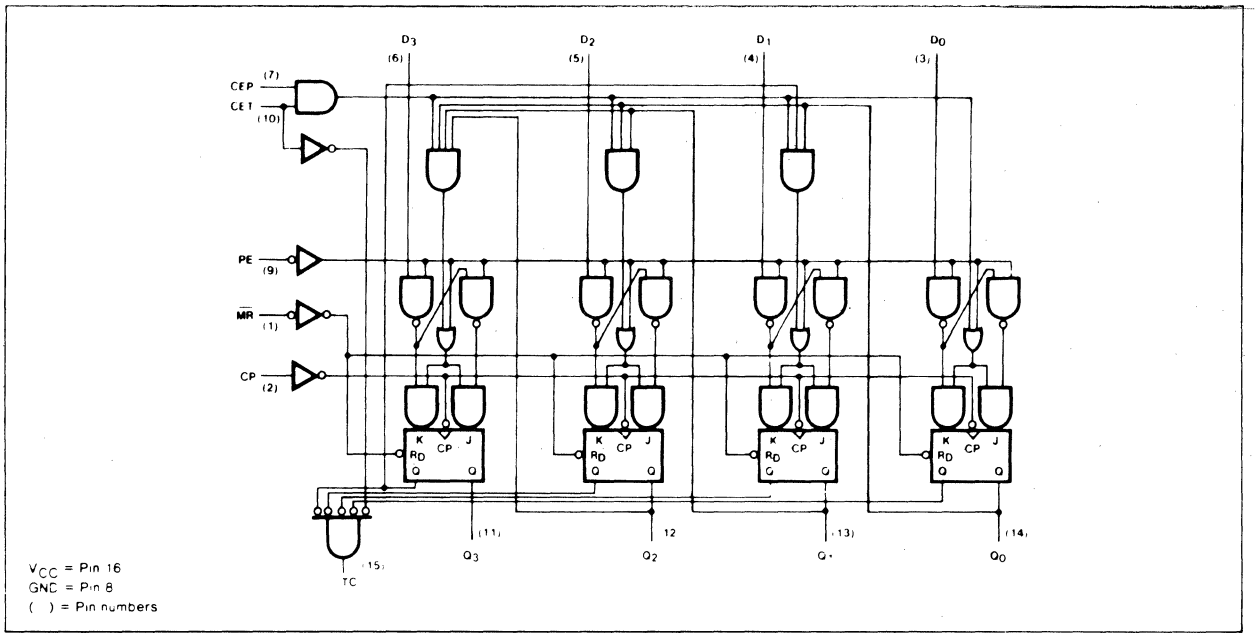


Figure 4-27 (SH1 of 2). Binary Counter with Asynchronous Clear Logic and Connections

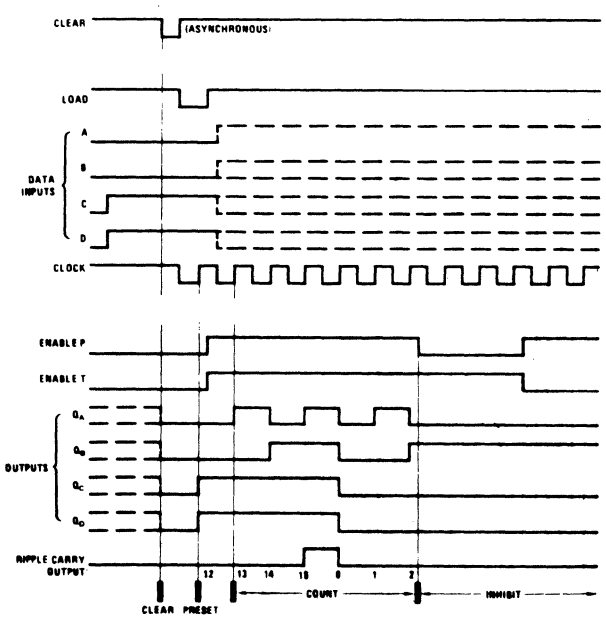
MODE SELECT - FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC
Reset (Clear)	L	X	X	X	X	X	L	L
Parallel Load	H	↑	X	X	l	l	L	L
	H	↑	X	X	l	h	H	(b)
Count	H	↑	h	h	h(d)	X	count	(b)
Hold (do nothing)	H	X	l(c)	X	h(d)	X	q_n	(b)
	H	X	X	l(c)	h(d)	X	q_n	L

H = HIGH voltage level steady state
L = LOW voltage level steady state
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition
X = Don't care
q = Lower case letters indicate the state of the referenced output prior to the LOW-to-HIGH clock transition
↑ = LOW-to-HIGH clock transition

NOTES
(b) The TC output is HIGH when CET is HIGH and the counter is at Terminal Count (HHHH for "161")
(c) The HIGH-to-LOW transition of CEP or CET on the 54/74161 should only occur while CP is HIGH for conventional operation
(d) The LOW-to-HIGH transition of $\overline{PE}$ on the 54/74161 should only occur while CP is HIGH for conventional operation

TYPICAL CLEAR, PRESET, COUNT AND INHIBIT SEQUENCES



Sequence:
(1) Clear outputs to zero
(2) Preset to binary twelve
(3) Count to thirteen, fourteen, fifteen, zero, one, and two
(4) Inhibit

Figure 4-27 (SH2 of 2). Binary Counter with Asynchronous Clear Logic and Connections

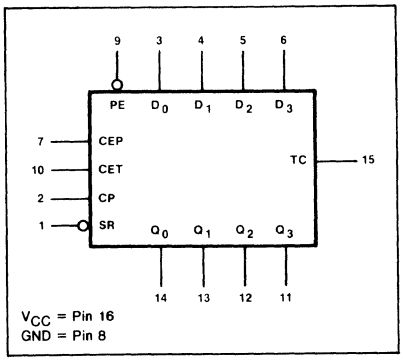
4.2.12 Four-Bit Binary Counter With Synchronous Clear (U23, U24, U74).

This device is a synchronous presettable 4-bit binary counter featuring an internal carry look-ahead for applications in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the positive-going edge of the clock.

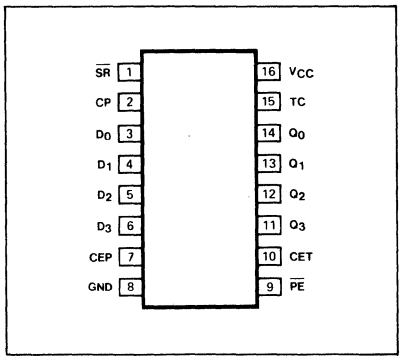
The counter is fully programmable; that is, the outputs may be preset to either level. Presetting is synchronous with the clock, and takes place regardless of the levels of the count enable inputs. A LOW level on the Parallel Enable ($\overline{PE}$) input disables the counter and causes the data at the D inputs to be loaded into the counter on the next LOW-to-HIGH transition of the clock. The reset (clear) function is synchronous with the clock. The Synchronous Reset ($\overline{SR}$), when LOW one setup time before the LOW-to-HIGH transition of the clock, overrides the CEP, CET, and $\overline{PE}$ inputs, and causes the outputs to go LOW coincident with the positive clock transition.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two Count Enable inputs (CET - CEP) and a Terminal Count (TC) output. Both count enable inputs must be HIGH to count. The CET input is fed forward to enable the TC output. The TC output thus enabled will produce a HIGH output pulse with a duration approximately equal to the HIGH level portion of the Q output. This HIGH level TC pulse is used to enable successive cascaded stages. For logic, connections and timing, see Figure 4-28.

Logic Symbol



Pin Configuration



Logic Diagram

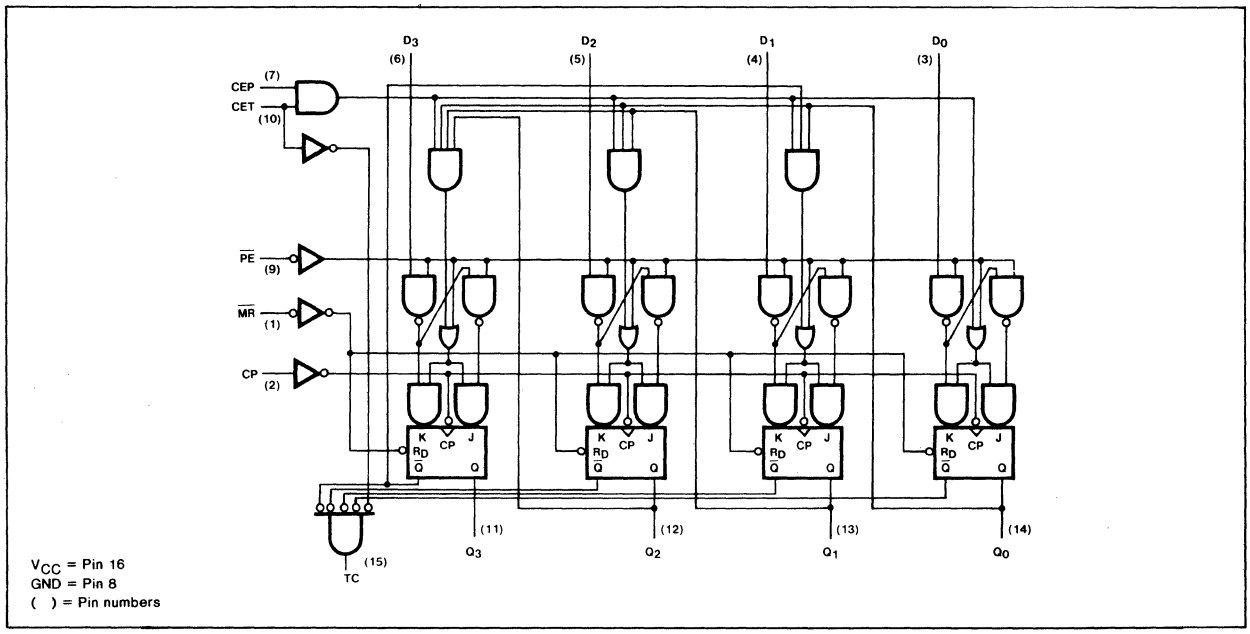


Figure 4-28 (SH1 of 2). Binary Counter with Synchronous Clear Logic and Connections

MODE SELECT - FUNCTION TABLE

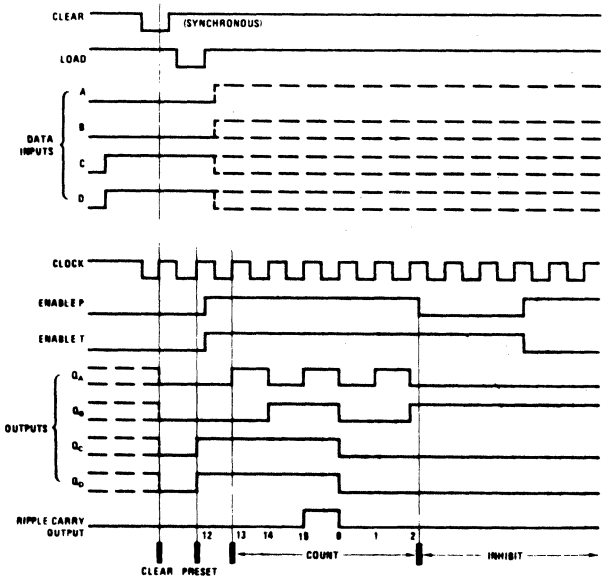
OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{SR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC
Reset (Clear)	l	↑	X	X	X	X	L	L
Parallel Load	h(d)	↑	X	X	l	l	L	L
	h(d)	↑	X	X	l	h	H	(b)
Count	h(d)	↑	h	h	h(d)	X	count	(b)
Hold (do nothing)	h(d)	X	l(c)	X	h(d)	X	q_n	(b)
	h(d)	X	X	l(c)	h(d)	X	q_n	L

H = HIGH voltage level steady state.
L = LOW voltage level steady state.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition
X = Don't care.
q = Lower case letters indicate the state of the referenced output prior to the LOW-to-HIGH clock transition.
↑ = LOW-to-HIGH clock transition

NOTES

(b) The TC output is HIGH when CET is HIGH and the counter is at Terminal Count (HHHH for "163").
(c) The HIGH-to-LOW transition of CEP or CET on the 54/74163 should only occur while CP is HIGH for conventional operation.
(d) The LOW to HIGH transition of $\overline{PE}$ or $\overline{SR}$ on the 54/74163 should only occur while CP is HIGH for conventional operation.

TYPICAL CLEAR, PRESET, COUNT AND INHIBIT SEQUENCES

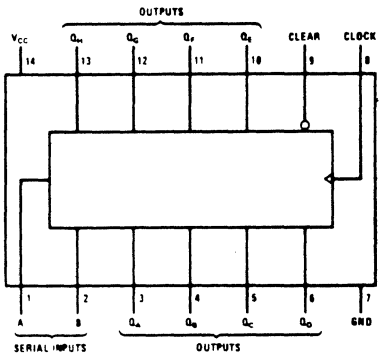


Sequence:
(1) Clear outputs to zero
(2) Preset to binary twelve
(3) Count to thirteen, fourteen, fifteen, zero, one, and two
(4) Inhibit

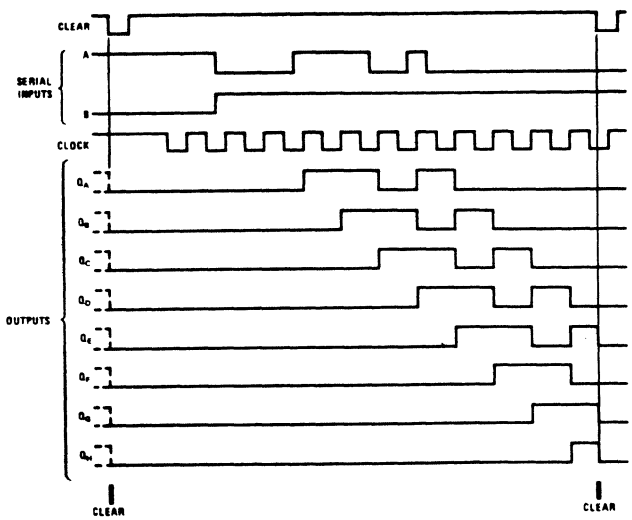
Figure 4-28 (SH2 of 2). Binary Counter with Synchronous Clear Logic and Connections

4.2.13 Eight-Bit Serial In/Parallel Out Shift Register (U66). This 8-bit shift register features gated serial inputs and an asynchronous clear. A low logic level at either input inhibits entry of the new data, and resets the first flip-flop to the low level at the next clock pulse, thus providing complete control over incoming data. A high logic level on either input enables the other input, which then determines the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the setup requirements will be entered. Clocking occurs on the low-to-high level transition of the clock input. All inputs are diode-clamped to minimize transmission-line effects. For logic and connections see Figure 4-29.

Connection Diagram



Timing Diagram



Logic Diagram

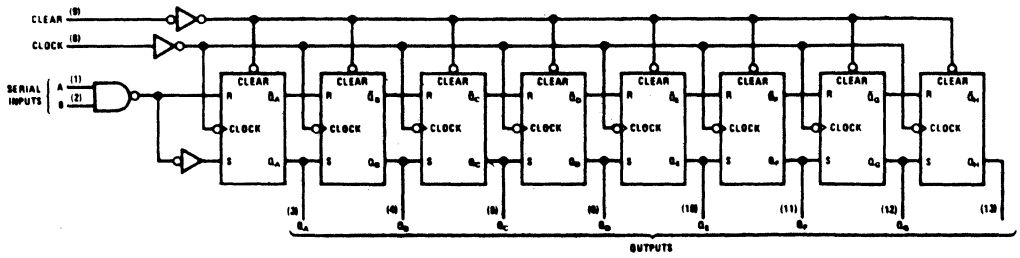
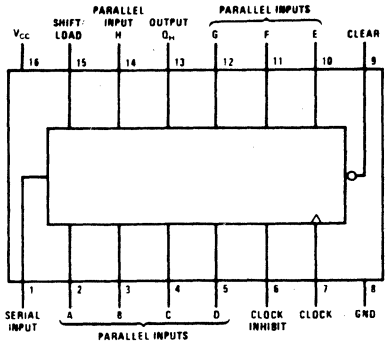


Figure 4-29. Eight-Bit Shift Register Logic and Connections

4.2.14 Eight Bit Parallel In/Serial Out Shift Register (U67). This parallel-in or serial-in, serial-out shift register features gated clock inputs and an overriding clear input. The load mode is established by the shift/load input. When high, this input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse. When low, the parallel (broadside) data inputs are enabled and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high level edge of the clock pulse through a two-input NOR gate, permitting one input to be used as a clock-enable or clock-inhibit function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input. This allows the system clock to be free-running, and the register can be stopped on command with the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. A buffered, direct clear input overrides all other inputs, including the clock, and sets all flip-flops to zero. For logic and connections see Figure 4-30.

Connection Diagram



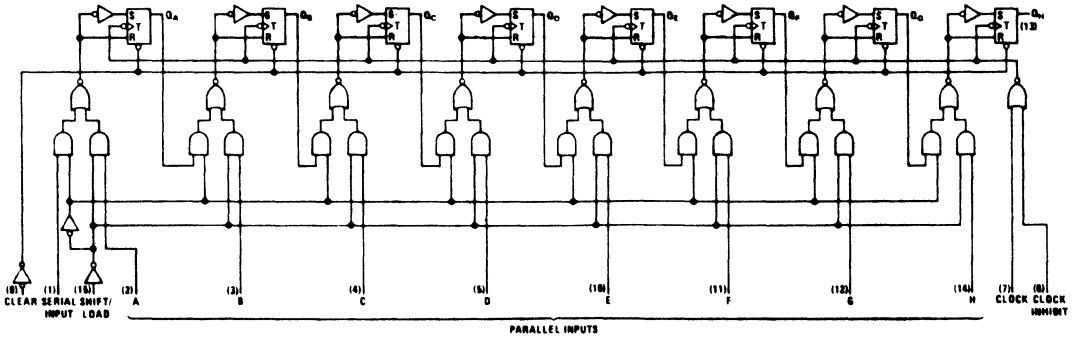
Truth Table

INPUTS						INTERNAL OUTPUTS		OUTPUT Q_H
CLEAR	SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A . . . H	Q_A	Q_B	
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	L	↑	X	a . . . h	a	b	h
H	H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	X	H	↑	X	X	Q_{A0}	Q_{B0}	Q_{H0}

H = High Level (steady state), L = Low Level (steady state)
X = Don't Care (any input, including transitions)
↑ = Transition from low to high level
a . . . h = The level of steady-state input at inputs A through H, respectively.
Q_{A0}, Q_{B0}, Q_{H0} = The level of Q_A, Q_B or Q_H, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Gn} = The level of Q_A or Q_G, respectively, before the most recent ↑ transition of the clock

Figure 4-30. Eight-Bit Parallel In/Serial Out Shift Register Logic and Connections (Sheet 1 of 2)

Logic Diagram



Timing Diagram

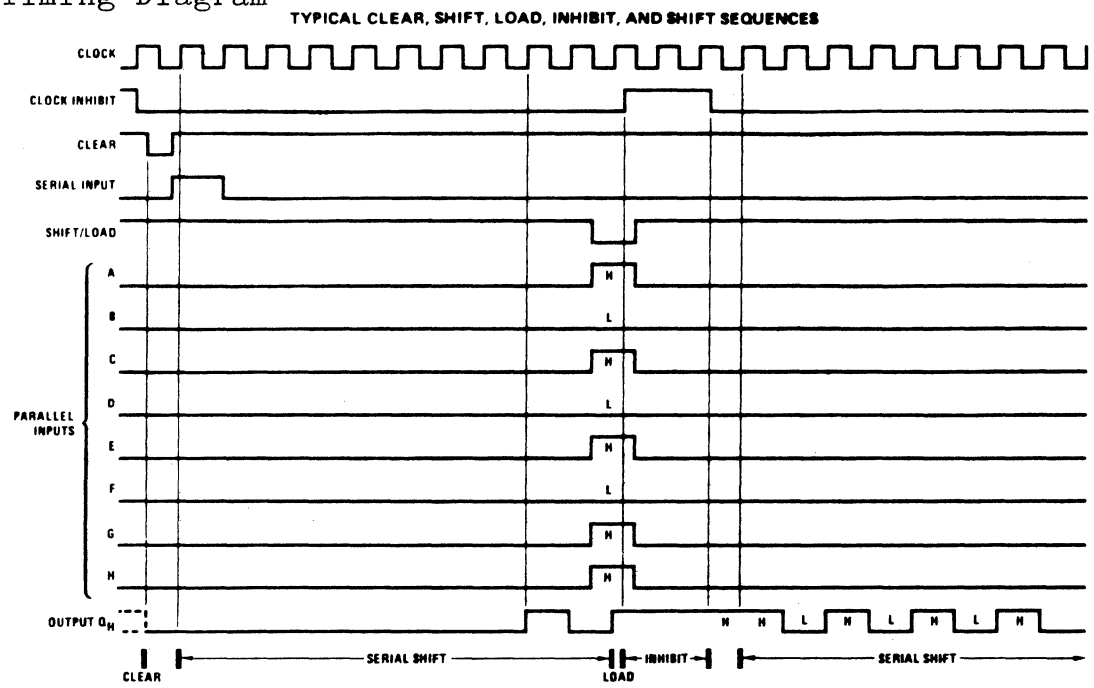
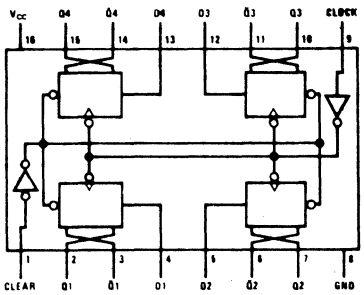


Figure 4-30. Eight-Bit Parallel In/Serial Out Shift Register Logic and Connections (Sheet 2 of 2)

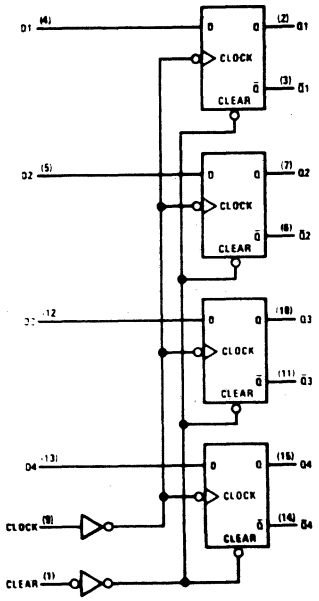
4.2.15 Quad D Flip-Flops With Clear (U63)

These positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. They feature a direct clear input and complementary outputs from each flip-flop. Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output. For logic and connections see Figure 4-31.

Connection Diagram



Logic Diagram



Truth Table

INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\bar{Q}^{\dagger}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\bar{Q}_0$

H = High Level (steady state)
L = Low Level (steady state)
X = Don't Care
↑ = Transition from low to high level
Q_0 = The level of Q before the indicated steady-state input conditions were established.
† = 175, LS175, and S175 only

Figure 4-31. Quad D Flip-Flops With Clear, Logic and Connections

4.2.16 Inverting Tri-State Buffer (U34, U65, U72).
For logic and connections see Figure 4-32.

Connection Diagram

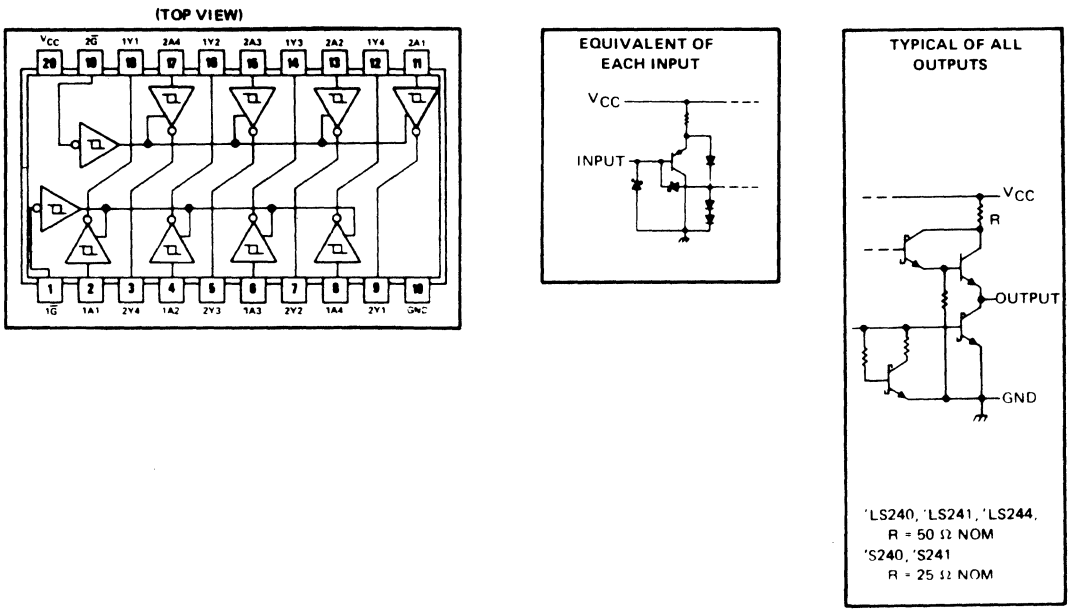
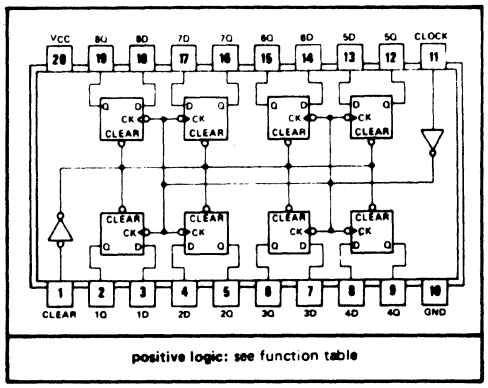


Figure 4-32. Inverting Tri-State Buffer
Logic and Connections

4.2.17 Octal D-Type Flip-Flop With Clear (U35, U79).
These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic with a direct clear input.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output. For logic and connections see Figure 4-33.

Connection Diagram



Truth Table

(EACH FLIP-FLOP)

INPUTS			OUTPUT
CLEAR	CLOCK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

Logic Diagram

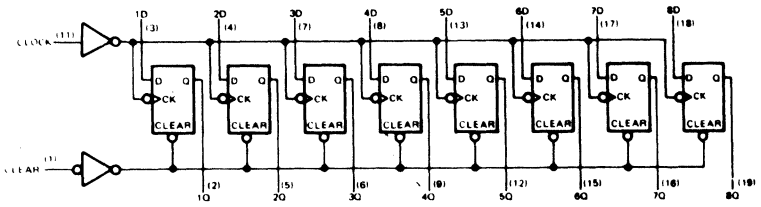
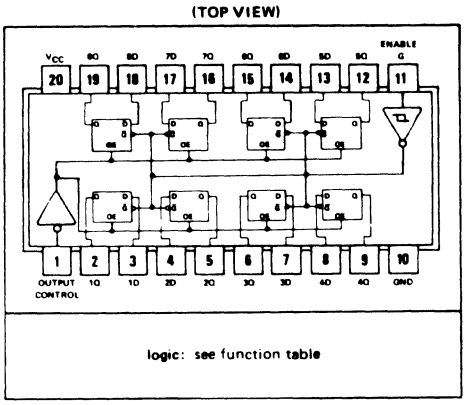


Figure 4-33. Octal D-Type Flip-Flop With Clear, Logic And Connections

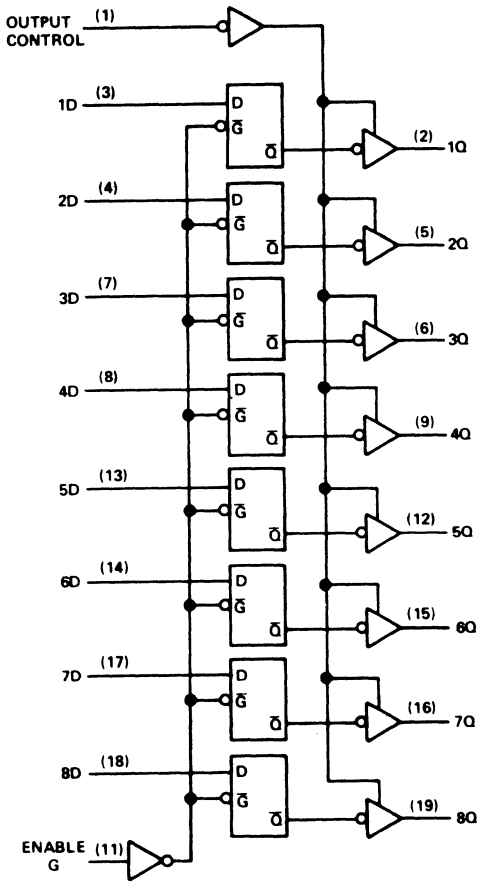
4.2.18 Octal D-Type Transparent Latch (U39).

This 8-bit register is a transparent D-type latch with three-state outputs. While the enable (G) is high, the Q outputs follow the data (D) inputs. When the enable is low, the output will be latched at the level of the data that was set up. For logic and connections see Figure 4-34.

Connection Diagram



Logic Diagram



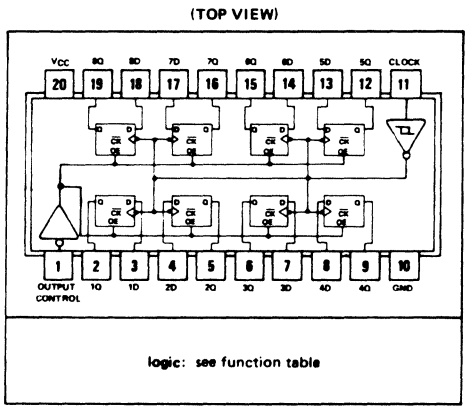
Truth Table

OUTPUT CONTROL	ENABLE G	D	OUTPUT
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

Figure 4-34. Transparent Latch Logic and Connections

4.2.19 Tri-State D Flip-Flops (U37, U38, U40, U76, U77, U80). These 3-bit registers contain D-type flip-flops with totem-pole tri-state outputs capable of driving highly capacitive or low impedance loads. When the output control is taken to a high logic level, the outputs go into the high impedance state. When a low logic level is applied to the output control, data at the D inputs are loaded into their respective flip-flops on the next positive-going transition of the clock. For logic and connections see Figure 4-35.

Connection Diagram



Truth Table

OUTPUT CONTROL	CLOCK	D	OUTPUT
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

Logic Diagram

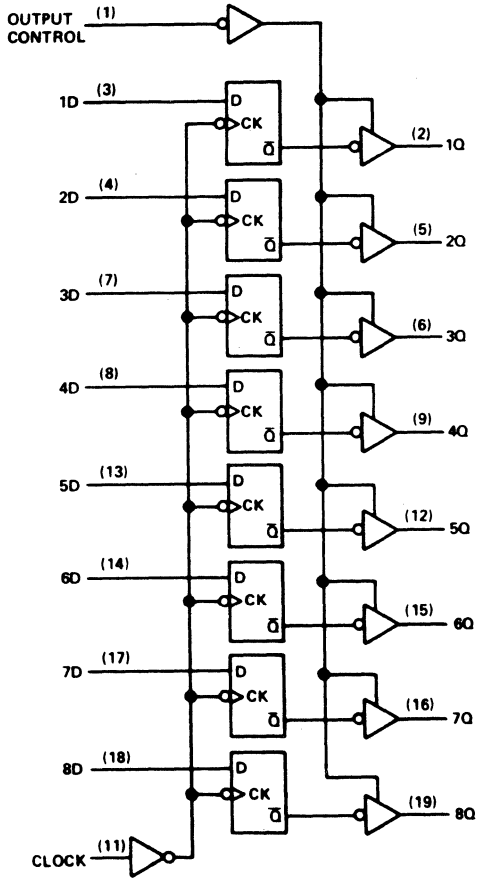
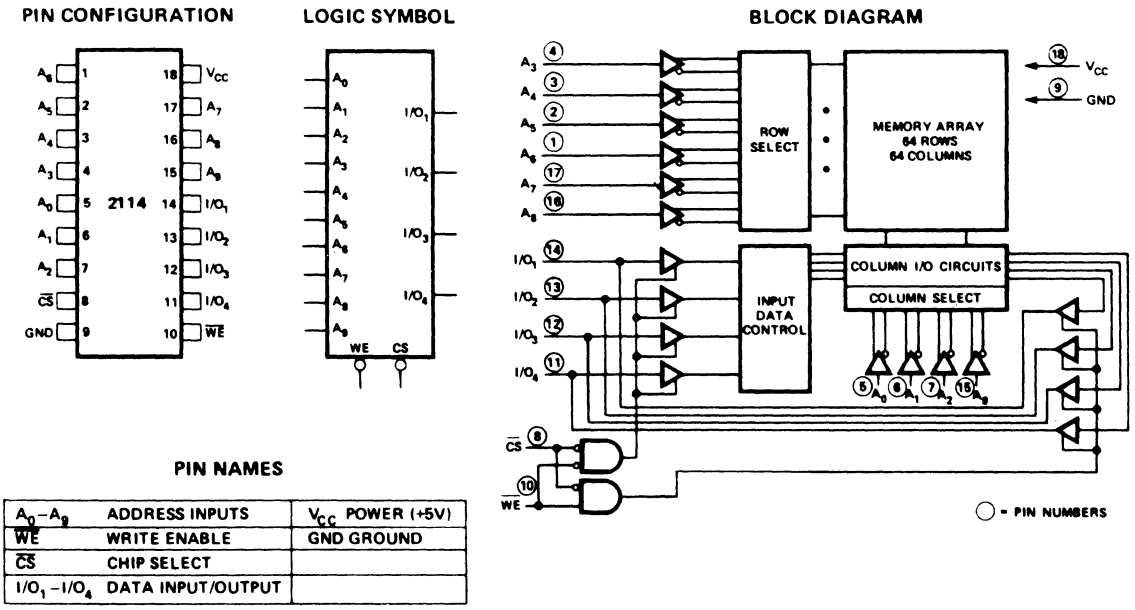


Figure 4-35. Tri-State D Flip-Flop Connections

4.2.20 1024 X 4-Bit Static Random Access Memory (U41, U42). This device is a 4096-bit static Random Access Memory organized as 1024 words by 4 bits and requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided and a separate chip select (CS) lead allows easy selection of an individual package. For logic and connections, see Figure 4-36.



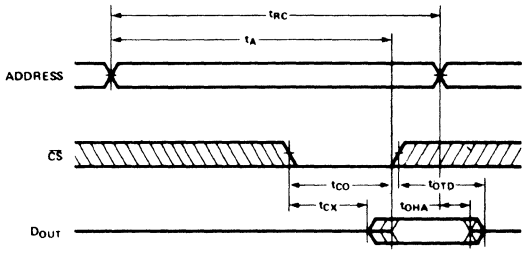
PIN NAMES

A_0–A_9	ADDRESS INPUTS	V_{CC}	POWER (+5V)
$\overline{WE}$	WRITE ENABLE	GND	GROUND
$\overline{CS}$	CHIP SELECT		
I/O_1–I/O_4	DATA INPUT/OUTPUT		

Figure 4-36. RAM Connections

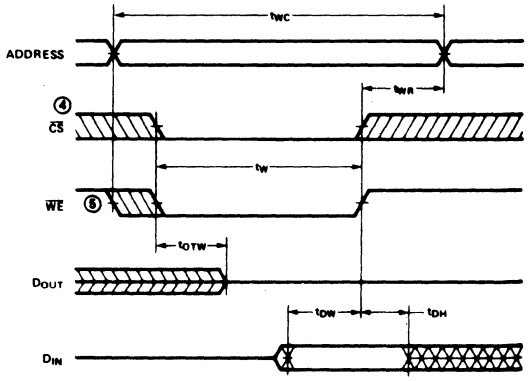
WAVEFORMS

READ CYCLE ③



NOTES:
③ $\overline{WE}$ is high for a Read Cycle.
④ If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition, the output buffers remain in a high impedance state.
⑤ $\overline{WE}$ must be high during all address transitions.

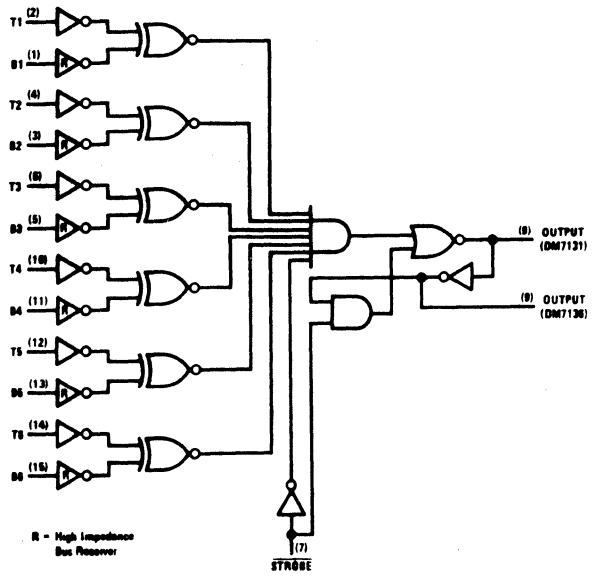
WRITE CYCLE



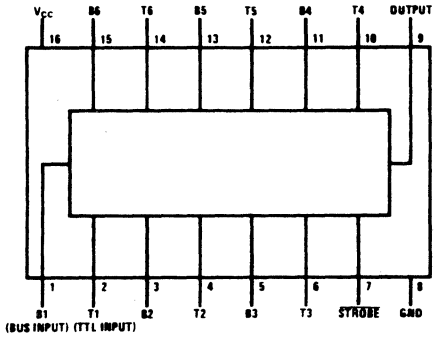
4.2.21 Bus Comparator (U27, U68).

This device compares two binary words of two to six bits in length and indicates matching (bit-for-bit) of the two words. Inputs for one word are TTL inputs, whereas inputs of the second word are high impedance receivers driven by a terminated data bus. The output has a latch that is strobe controlled. The transfer of information to the output occurs when the STROBE input goes from a logical 1 to a logical 0 state. Inputs may be changed while the STROBE is at the logical 1 level, without affecting the state of the output. For logic and connections, see Figure 4-37.

Logic Diagram



Connection Diagram



Truth Table

CONDITION	$\overline{\text{STROBE}}$	OUTPUT	
		DM71/8131	DM71/8136
T = B, T ≠ B	H	Q_{N-1} *	Q_{N-1} *
T = B	L	L	H
T ≠ B	L	H	L

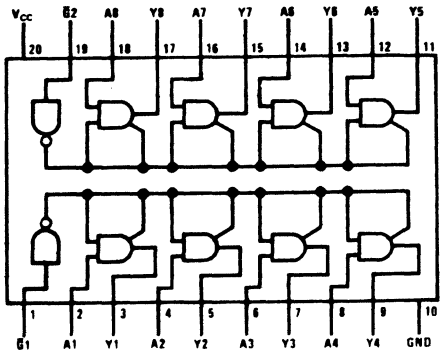
*Latched in previous state

Figure 4-37. Bus Comparator Connections

4.2.22 Tri-State Octal Buffers (U36).

This device provides eight, two-input buffers and employs Schottky TTL technology. One of the two inputs to each buffer is used as a control line to gate the output into the high impedance state, while the other input passes the data through the buffer with no inversion. Four buffers are enabled from one common line and the other four are enabled from another common line. The outputs are placed in the tri-state condition by applying a high logic level to the enable pins. For logic and connections, see Figure 4-38.

Logic and Connections



Truth Table

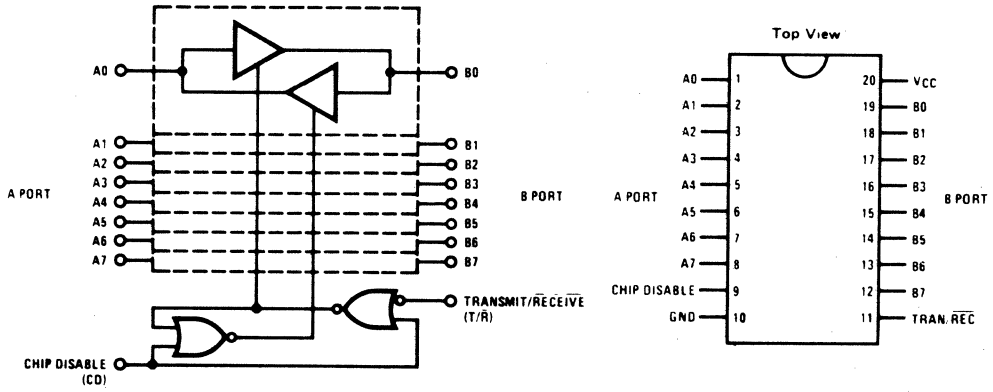
INPUTS		OUTPUT
$\overline{G}$	A	Y
H	X	Z
L	H	H
L	L	L

Figure 4-38. Tri-State Octal Buffer Logic and Connections

4.2.23 Bidirectional Transceiver (U43, U64).

This device is a Schottky device that provides bidirectional drive for bus oriented microprocessor systems. Transmit/Receive inputs determine the direction of logic signals through the device. The Chip Disable input disables both A and B ports by placing them in a tri-state condition. For logic and connections, see Figure 4-39.

Connection and Logic Diagram



Logic Table

Inputs		Resulting Conditions	
Chip Disable	Transmit/Receive	A Port	B Port
0	0	OUT	IN
0	1	IN	OUT
1	X	TRI-STATE	TRI-STATE

X = Don't Care

Figure 4-39. Bidirectional Transceiver Logic and Connections

5.0 INTRODUCTION

The AM-420 circuit board performs to full capacity with a minimum of maintenance. This section describes maintenance and troubleshooting procedures and procedures for handling warranty returns.

5.1 CIRCUIT BOARD CHECKOUT/TROUBLESHOOTING PROCEDURES

The AM-420 circuit board was fully tested before it left Alpha Microsystems and will operate satisfactorily in the system if the hardware and software requirements of Sections Two and Three of this manual are met. Should a problem arise, use the following procedures to identify and locate the fault.

1. Check the circuit boards for proper seating in the slot.

2. Check the hash totals on the latest operating system.

3. Check all power connections for correct voltages.

4. Check jumper options to ensure correctness of application. These include boot jumper and interrupt jumper on AM-100/T, or AM-100.

5. Verify that the fault is in the AM-420 and not either in the system or in the peripherals. This can best be accomplished with substitution of a known good circuit board.

6. Check the error LED's on the AM-420. They are read with the right most being the LSB.

   The errors are as follows:

   a. Read data error

b. Memory test error

c. Read CRC error

d. Drive not ready error

e. Drive Fault error

f. Restore error

g. Seeks error

7. Perform the diagnostic tests.

5.2 WARRANTY PROCEDURES

This circuit board is covered by warranty issued by Alpha Microsystems, Irvine, California. Complete details of the warranty are included with the circuit board. Should a problem arise with this circuit board, call your dealer or the Alpha Micro International Support/Services Group for information.

Table 6-1. AM-420 Component Cross-Reference List

REF DESIG	MFG TYPE NO.	PAR. NO.	REF DESIG	MFG TYPE NO.	PAR NO.
U1	74LS04	-	U24	74LS163	4.2.12
U2	74LS02	-	U25	74LS138	4.2.6
U3	74S00	-	U26	74LS138	4.2.6
U4	74LS08	-	U27	8131	4.2.21
U5	74LS74	4.2.4	U28	74LS367	4.2.18
U6	74LS08	-	U29	74LS30	-
U7	74LS11	-	U30	74LS139	4.2.7
U8	74LS00	-	U31	DWB-00422-00	-
U9	4MHz Osc.	-	U32	74S374	4.2.20
U10	2940	4.2.2	U33	DWB-00423-00	-
U11	Z80	4.2.1	U34	74LS240	4.2.16
U12	74LS08	-	U35	74LS273	4.2.17
U13	74LS151	4.2.8	U36	81LS97	4.2.22
U14	74LS74	4.2.4	U37	74LS374	4.2.19
U15	9401	4.2.3	U38	74LS374	4.2.19
U16	74LS32	-	U39	74LS373	4.2.18
U17	74LS112	4.2.5	U40	74LS374	4.2.19
U18	74LS158	4.2.10	U41	2114	4.2.20
U19	74LS158	4.2.10	U42	2114	4.2.20
U20	74LS08	-	U43	8304	4.2.23
U21	2940	4.2.2	U44	7805	-
U22	75452	-	U45	7805	-
U23	74LS163	4.2.12	U46	7805	-

Table 6-1 (Con't). AM-420 Component Cross-Reference List

REF DESIG.	MFG TYPE NO.	PAR. NO.	REF DESIG	MFG TYPE NO.	PAR NO.
U47	7805	-	U72	74LS240	4.2.16
U49	75113	-	U73	74LS10	4.2.14
U50	75115	-	U74	74LS163	4.2.12
U51	74LS08	-	U75	74LS161	4.2.11
U52	74LS00	-	U76	74LS374	4.2.19
U53	74LS74	4.2.4	U77	74LS374	4.2.19
U55	74LS74	4.2.4	U78	74S374	4.2.13
U56	74LS193	-	U79	74LS273	4.2.17
U57	74LS193	-	U80	74LS374	4.2.19
U58	74LS244	-	U81	74LS244	4.2.11
U59	74LS32				
U60	74LS14				
U61	74L157	4.2.9			
U62	74LS74	4.2.4			
U63	74LS175	4.2.15			
U64	8304	4.2.23			
U65	74LS240	4.2.16			
U66	74LS164	4.2.13			
U67	74166	4.2.14			
U68	8131	4.2.21			
U71	74LS138	4.2.6			

FBILL # DWB-00420-00

REV.B01

21 SEP,1981

DESCRIPTION 8" WINCHESTER CONTROLLER 8MB

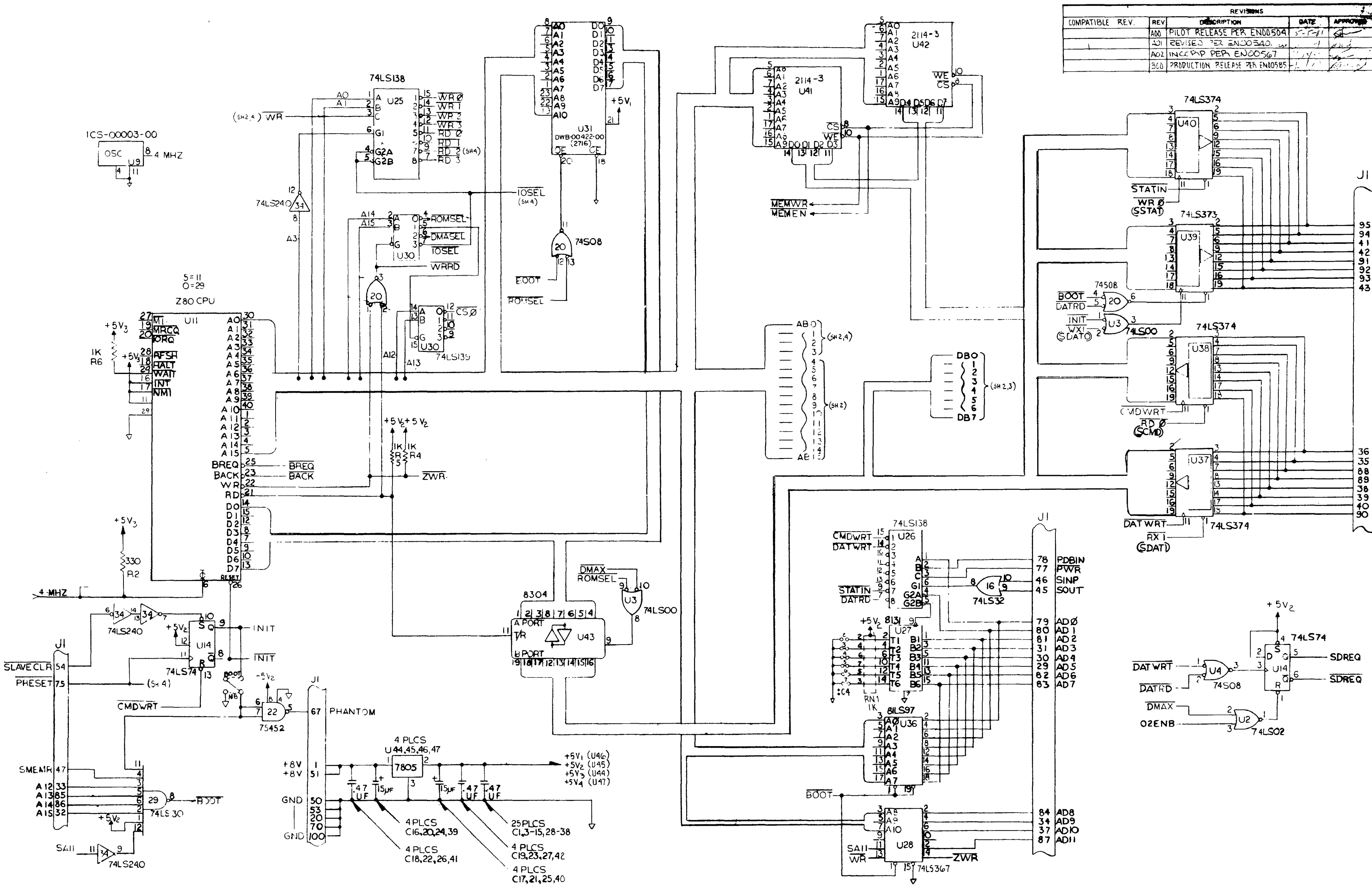
	PART NUMBER	DESCRIPTION	QTY
1	DWF-00420-00	P.C.B. DETAIL DWG, AM-420	1
2	CNA-00006-00	CONN RECEPTACLE SHORTING 2CONT BLK	1
3	CNF-00002-11	HEADER 50 PIN W/O EJC RT ANGLE	1
4	CNF-00033-02	HEADER STRIP LINE PLUG MALE	2
5	CNS-00020-00	SOCKET 20 PIN DIP	1
6	CNS-00024-00	SOCKET 24 PIN DIP	1
7	CNS-00028-00	SOCKET 28 PIN DIP	2
8	CNS-00040-00	SOCKET 40 PIN DIP	1
9	CPN-00474-01	CAPACITOR .47 UF	33
10	CPP-00156-01	CAPACITOR 15 UF 20V	8
11	DIO-00001-00	LED	3
12	DWB-00422-00	ASSY PROM PRILOD	1
13	DWB-00423-00	ASSY PROM ROM420	1
14	HDM-00003-09	BUS BAR PC MOUNT 9 POSITION	2
15	HDM-00003-11	BUS BAR PC MOUNT 11 POSITION	1
16	HDM-00007-00	HEAT SINK .750WI .375HT .750LG	4
17	HDN-10000-06	NUT HEX 6-32 KEP INT/EXT CAD STL	4
18	HDS-10506-06	SCREW,PHMS,SS,PH RECESS,6-32 X 3/8	4
19	IC1-07400-01	IC QUAD 2 INPUT NAND GATE	2
20	IC1-07400-02	IC QUAD 2 INPUT NAND GATE	1
21	IC1-07402-01	IC QUAD 2 INPUT NOR GATE	1
22	IC1-07404-01	IC HEX INVERTER	1
23	IC1-07408-01	IC QUAD 2 INPUT AND GATE	3
24	IC1-07408-02	IC QUAD 2 INPUT AND GATE	2
25	IC1-07410-01	IC TRIPLE 3 INPUT NAND GATE	1
26	IC1-07411-01	IC TRIPLE 3 INPUT AND GATE	1
27	IC1-07414-01	IC HEX INVERTER W/HYSTERESIS	1
28	IC1-07430-01	IC 8 INPUT NAND GATE	1
29	IC1-07432-01	IC QUAD 2 INPUT OR GATE	2
30	IC1-07474-01	IC DUAL D FLIPFLOP	5
31	IC1-08131-00	IC COMPARATOR 6 BIT	2
32	IC1-08197-01	IC BUFFER OCTAL	1
33	IC1-08304-00	IC TRANSCEIVER OCTAL	2
34	IC1-74112-01	IC DUAL J-K NEGATIVE FLIPFLOP	1
35	IC1-74138-01	IC DECODER 3 TO 8 LINE	3
36	IC1-74139-01	IC DECODER 2 TO 4 LINE DUAL	1
37	IC1-74151-01	IC 8 INPUT MULTIPLEXER	1

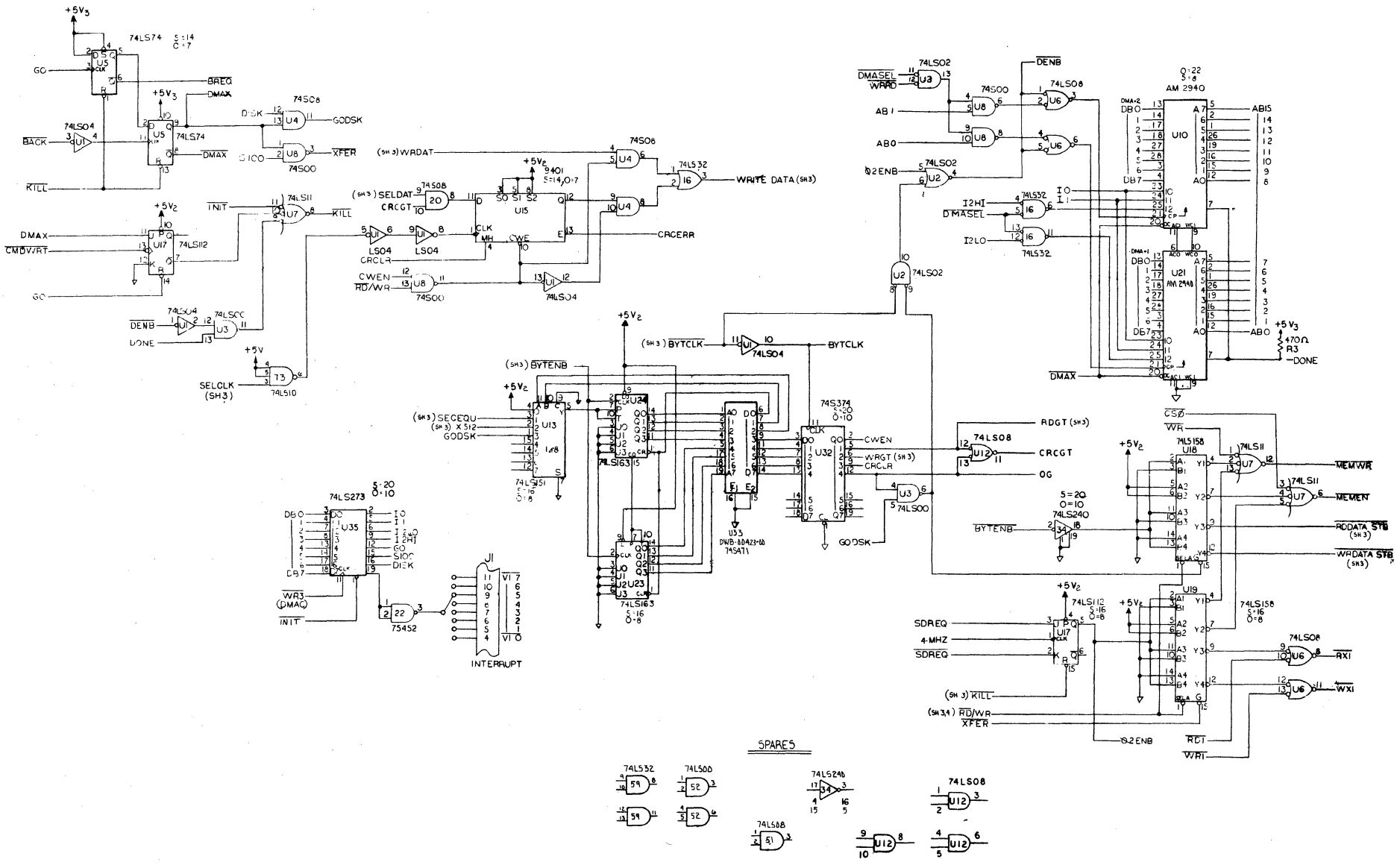
BILL # DWB-00420-00 REV.B01 DESCRIPTION 8" WINCHESTER CONTROLLER 8M

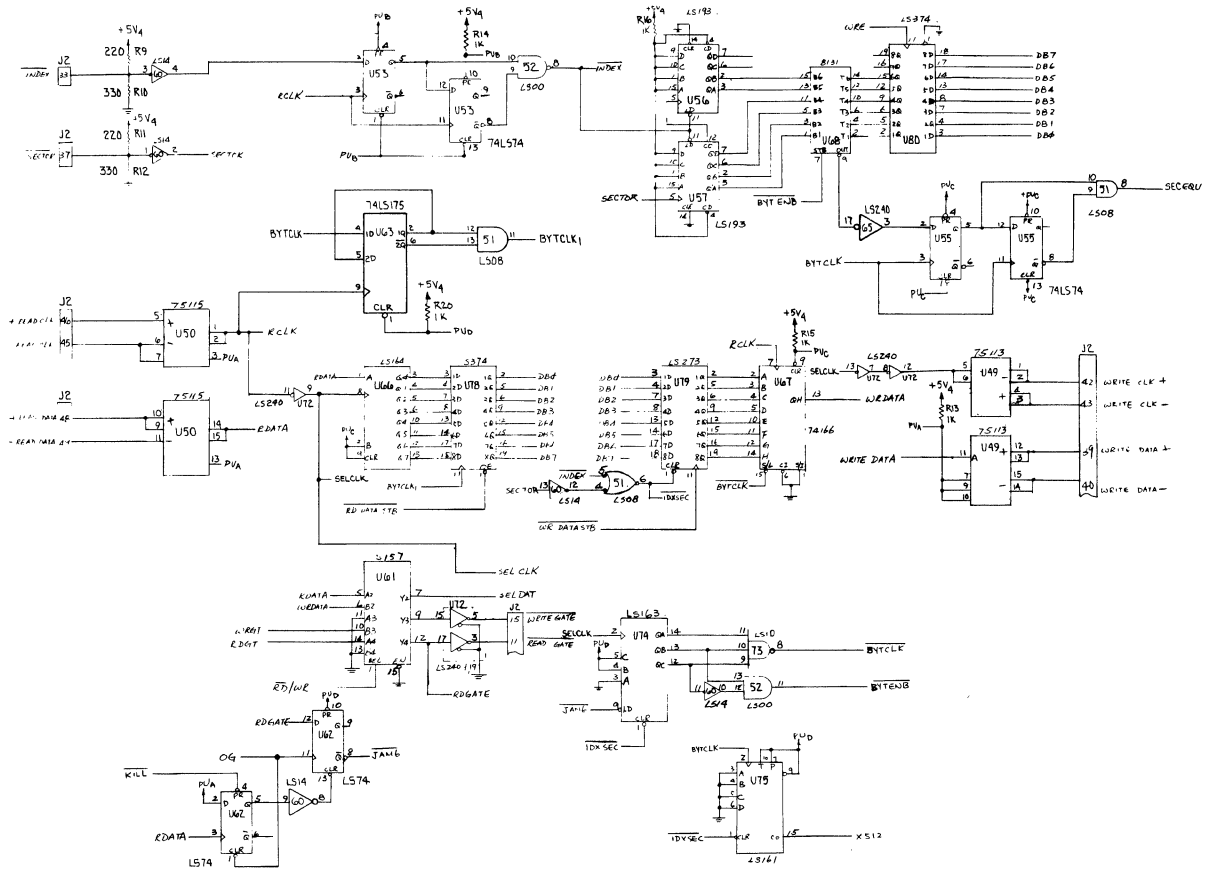
	PART NUMBER	DESCRIPTION	QTY
38	IC1-74157-02	IC QUAD 2 TO 1 DATA SELECTOR	1
39	IC1-74158-01	IC QUAD 2 TO 1 DATA SELECTOR	2
40	IC1-74161-01	IC SYNCHRONOUS 4 BIT COUNTER	1
41	IC1-74163-01	IC SYNCHRONOUS COUNTER	3
42	IC1-74164-01	IC 8 BIT SER IN PAR OUT SR	1
43	IC1-74166-00	IC 8 BIT PAR IN SER OUT SR	1
44	IC1-74193-01	IC COUNTER 4 BIT BINARY	2
45	IC1-74240-01	IC OCTAL BUS DRIVER INVERTING	3
46	IC1-74244-01	IC OCTAL BUS DRIVER NONINVERT	2
47	IC1-74273-01	IC OCTAL D REGISTER W/RESET	2
48	IC1-74367-00	IC HEX BUFFER	1
49	IC1-74373-01	IC OCTAL D FLIPFLOP	1
50	IC1-74374-01	IC OCTAL D FLIPFLOP	6
51	IC1-74374-02	IC OCTAL D FLIPFLOP	2
52	ICI-75115-00	DUAL DIFFERENTIAL RECEIVER	1
53	ICI-75452-00	IC DUAL NAND POWER DRIVER	1
54	ICL-07805-00	IC REGULATOR + 5V	4
55	ICM-02114-04	RAM 1K X 4 BIT STATIC	2
56	ICS-00003-00	IC OSCILLATOR 4MHZ	1
57	ICS-00080-00	IC MICROPROCESSOR Z-80	1
58	ICS-02940-00	IC DMA ADDRESS GENERATOR	2
59	ICS-09401-00	IC GENERATOR CRC	1
60	RS2-00102-00	RESISTOR 1 K 1/4W 5% CAR	8
61	RS2-00331-00	RESISTOR 330 OHM 1/4W 5% CAR	4
62	RS2-00471-00	RESISTOR 470 OHM 1/4W 5% CAR	1
63	RSN-00008-00	RES PACK 8 PIN SIP 1 K	1
64	ICI-75113-00	DUAL DIFFERENTIAL DRIVER	1
65	IC1-74175-01	IC QUAD D FLIPFLOP	1
66	RS2-00221-00	RESISTOR 220 OHM 1/4W 5% CAR	6
67	DWL-00420-00	* * * * RECORD NOT FOUND * * * *	0
68	CBW-00026-20	WIRE 26AWG BUS	0
69	HDM-00012-00	THERMAL GREASE	0
70	DWS-30000-04	SPEC REGULATOR MTG ASSY	0
71	LBL-00018-19	LABEL PCB SERIAL I.D. AM 420	1

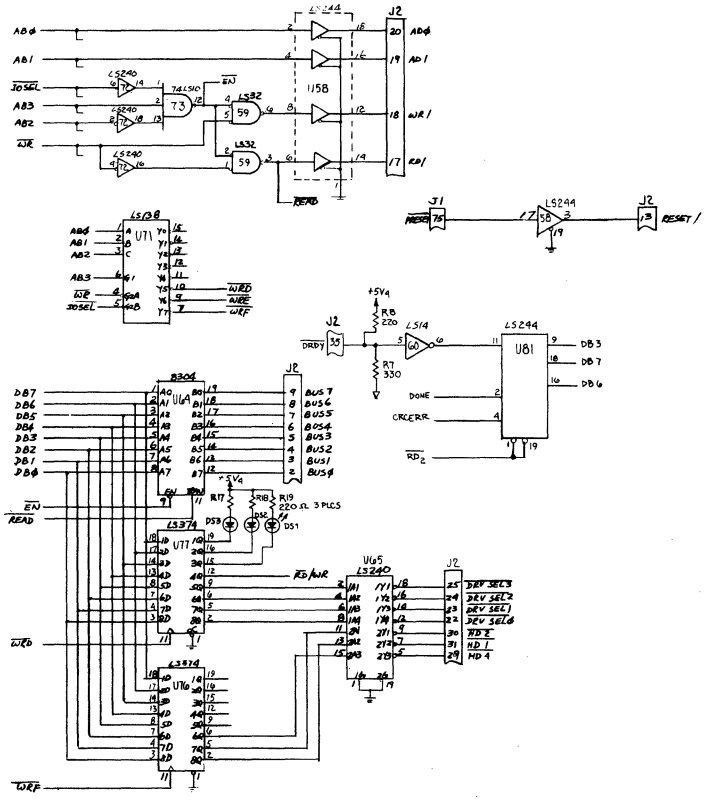
DWM-00420-00 REV. A00

		REVISIONS		
COMPATIBLE REV.	REV	DESCRIPTION	DATE	APPROVED
	A00	PILOT RELEASE PER EN00504		
	A01	REVISED PER EN00540		
	A02	INC... PER EN00567		
	3C0	PRODUCTION RELEASE PER EN00585		




+5V3
74LS74
GO
BREQ
DMAX
74LS04
BACK
74LS08
DISK
GODSK
74LS00
SIOO
XFER
KILL
+5V2
74LS11
INIT
74LS112
DMAX
CMDWRT
74LS04
74LS00
DENB
DONE
+5V
74LS10
SELCLK (SH3)
(SH3) SELDAT
CRCGT
74S08
LS04
CRCLR
CWEN
RD/WR
74S00
(SH3) WRDAT
74S08
74LS32
WRITE DATA (SH3)
CRCERR
9401
U15
74LS04
(SH3) BYTCLK
BYTCLK
(SH3) BYTENB
(SH3) SECEQU
(SH3) X512
GODSK
U13
74LS151
74LSI63
74S374
U32
CWEN
WRGT (SH3)
CRCLR
GODSK
74LS08
RDGT (SH3)
CRCGT
OG
74LS00
74LS273
U35
DB0
DB7
WR3 (DMAQ)
INIT
75452
INTERRUPT
DMASEL
WRAD
74LS02
DENB
AB1
AB0
Q2ENB
I2HI
DMASEL
I2LO
74LS32
AM 2940
U10
U21
DMA+2
DMA+1
DB0
DB7
AB15
AB0
DMAX
+5V3
470Ω
R3
DONE
74LS02
74LS240
BYTENB
CSØ
WR
74LS158
U18
MEMWR
MEMEN
RDDATA STB (SH3)
WRDATA STB (SH3)
74LS11
74LS112
U17
SDREQ
4-MHZ
SDREQ
(SH3) KILL
(SH3,4) RD/WR
XFER
74LS158
U19
74LS08
AXI
WXI
RDT
WRI
Q2ENB
SPARES
74LS32
74LS00
74LS244
74LS08
74LS08





VOLTAGE AND GROUND CHART					
+5V1	+5V2	+5V3	+5V4	GND	IC REFERENCE DESIGNATIONS
PIN 18				PIN 9	U42, U43
PIN 20				PIN 10	U32, 33, 34, 35, 36, 37, 38, 39, 40, 41
PIN 24				PIN 12	U31
	PIN 16			PIN 8	U23, 24, 26, 27, 28, 19, 30, 25, 13, 17, 18
	PIN 14			PIN 1	U12, 14, 15, 16, 20, 29
	PIN 8			PIN 22	U21
	PIN 8			PIN 4	U22
		PIN 8		PIN 22	U10
		PIN 11		PIN 29	U11
		PIN 14		PIN 7	U1, 2, 3, 4, 5, 6, 7, 8, 9
		PIN 20		PIN 10	U76, 77, 78, 79, 80, 81
			PIN 14	PIN 7	U50, 51, 52, 53, 54, 55, 59, 60, 62, 66, 73
			PIN 16	PIN 8	U48, 49, 56, 57, 61, 63, 67, 68, 69, 70, 71, 74, 75
			PIN 20	PIN 10	U58, 64, 65, 72

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