WINC-Ø5/5 & Ø5/8 TECHNICAL MANUAL

P/N 990Ø16-Ø1 REV C. 1986

COPYRIGHT

Trademarks

TABLE OF CONTENTS

FIGURES

TABLES

CHAPTER 1

INTRODUCTION & SPECIFICATIONS

Introduction

The **WINC-05/5 & 5/8** (hereafter referred to as **WINC-05** unless information is specific to a particular configuration) are disk controllers for the DEC LSI-11 CPU system. They emulate two DEC disk controllers - an RL01/02 (5.2 to 41.6 MB) and an RX02 (single/double sided, single/double density 8", **WINC-05/8**, or double density 5-1/4" floppy disks, **WINC-05/5**). They have been designed on a single dual width (5" x 8") PCB which mounts inside the CPU chassis.

The hardware is divided into four functional sections. The first is a 16 bit microprocessor which controls all other sections. Second is a serial data encoder/decoder, including a phase lock loop operating at either 5.0 MHz, 500 KHz, or 250 KHz data rates. The third section is the drive control interface. And last, the host bus interface, including control of the two command register sets plus interrupts and direct memory accesses. It should be noted that most of the traditional disk control functions are implemented in the microprocessor program, rather than in hardware.

Reference Documents

Reference documents include the following:

AED P/N	DESCRIPTION
120120-01	Logic Diagram, WINC-05 (5-1/4" floppy)
120180-01	Logic Diagram, WINC-05/5, 5/8(5-1/4" & 8" floppy)
120171-01	Logic Diagram, Signal interconnect board
900000-01	Manual, floppy diagnostic
800011-XX	Floppy Diagnostic Diskette, 5-1/4" diskette
800048-XX	Floppy Diagnostic Diskette, 8" diskette
900057-01	Manual, Winchester diagnostic
800057-XX	Winchester Diagnostic Diskette, 8" diskette

Digital Equipment Corporation

Microcomputers and Memories Peripherals Handbook
ZRXDB0 - RX02 performance excercisor
ZRLKB1 - RL02 performance excercisor
ZRLMB0 - RL02 bad block writing

Block Diagram

A block diagram of the **WINC-05** is shown in **Figure 1-1.**

Controller Architecture

A 16-bit MOS microprocessor is used to handle the primary algorithms for the **WINC-05**. These algorithms include:

- Controller command emulation
- DMA transfer support
- Drive control (SELECT, STEP, READY, etc)
- Track and sector mapping
- Header search
- Drive R/W mode control
- Drive type and format analysis
- Drive formatting
- Diagnostic aids

A bipolar microsequencer is also used in conjunction with the MOS microprocessor for serial disk data transfers whose functions are:

- Serialize/deserialize data
- Write precompensation on Winchester drives
- Phase lock oscillator control
- Clock encoding/decoding
- Address mark generation/detection
- CRC register handling

A third logical area contains the circuits used for synchronizing the host's bus interface cycles with the **WINC-05's** internal microprocessor.

Multiple Controller Operations

The **WINC-05** emulates two logical controllers by using multiprogramming techniques. When the interfaces for both the Winchester and floppy are being simultaneously operated, the Winchester interface is given a higher priority. This higher priority ensures the highest data throughput for the Winchester. The floppy interface has a guaranteed service within a set time interval to prevent it from being completely locked out.

Available Configurations

The **WINC-05** directly supports up to two physical Winchester and two floppy drives. A drive cabling board within the subsystem is used to rewire the **WINC-05** 50 pin I/O flat cable into the pin layout required by the drives.

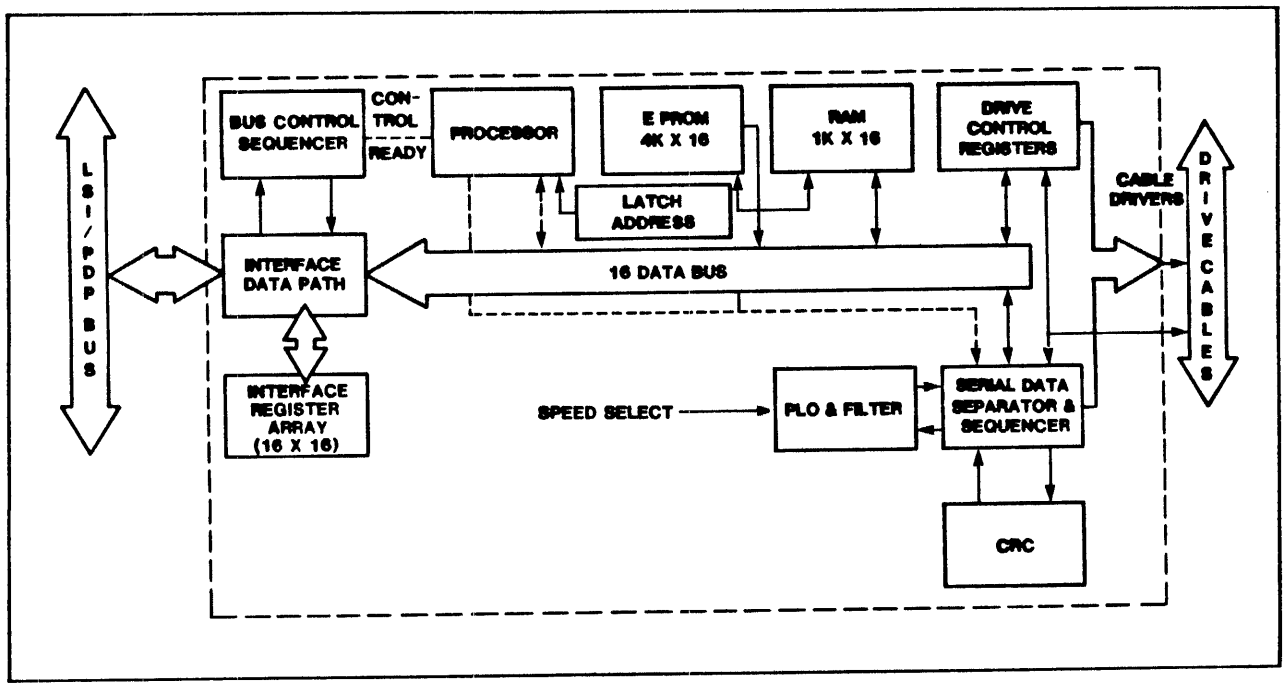


FIGURE 1.1
Block Diagram

AED system configurations which are available include:

- One or two 10.4 or 20.8 Mbyte Winchester and one 0.5 Mbyte 5-1/4" floppy or one or two 8" 1.0 MB floppy disk drives.

Figure 1.2 outlines a typical **WINC-05** configuration.

The Winchester drive control signals conform to the Seagate ST506 interface. The data rate is nominally 5 Mbits/sec. Known variations between difference disk drive manufacturers may be handled through a configuration PROM available from **AED** and installed on the controller board. (See **Appendix C**, Available Configuration PROMS).

Emulation Characteristics

The **WINC-05** is fully compatible with all DEC operating systems including RT-11, RSX-11M and RSX-11M PLUS. It is also fully compatible with DEC diagnostic programs. DEC software transparency is achieved by fundamental **WINC-05** design features such as:

- Complete emulation of DEC's RL01/02 and RX02 system
- RL01/02 compatible formats on the 5-1/4" Winchester with individual capacities of 5.2 through 41.6 Mbytes (formatted)
- RX02 compatible format on the optional 8" floppy disk drive with a capacity of 1.0 Mbytes (Fmtd.)
- The 5-1/4" floppy drive has a unique RX02 media format.

Maintenance Software

AED maintenance programs are supplied on a floppy diskette. If the **WINC-05** controller is utilized separate from the subsystem, these routines must be purchased individually from **AED** with RX02 formatting or other media. The routines include diagnostics for both the Winchester and floppy drives. See **Chapter 5** for diagnostics operation.

Controller & Subsystem Specifications

When used with Seagate ST406/412 and QUME 242 disk drives, the following are the systems specifications.

	EMULATION		
Drive Characteristics	**RL01**	**RL02**	**RX02** 8" Floppy
Capacity/drive (formatted)	5.2 Mb	10.4 Mb	1.0 Mb
Drives/controller	2	2	2
Average Access Time	93 ms	93 ms	275 ms
Minimum Seek Time	19 ms	18 ms	18 ms

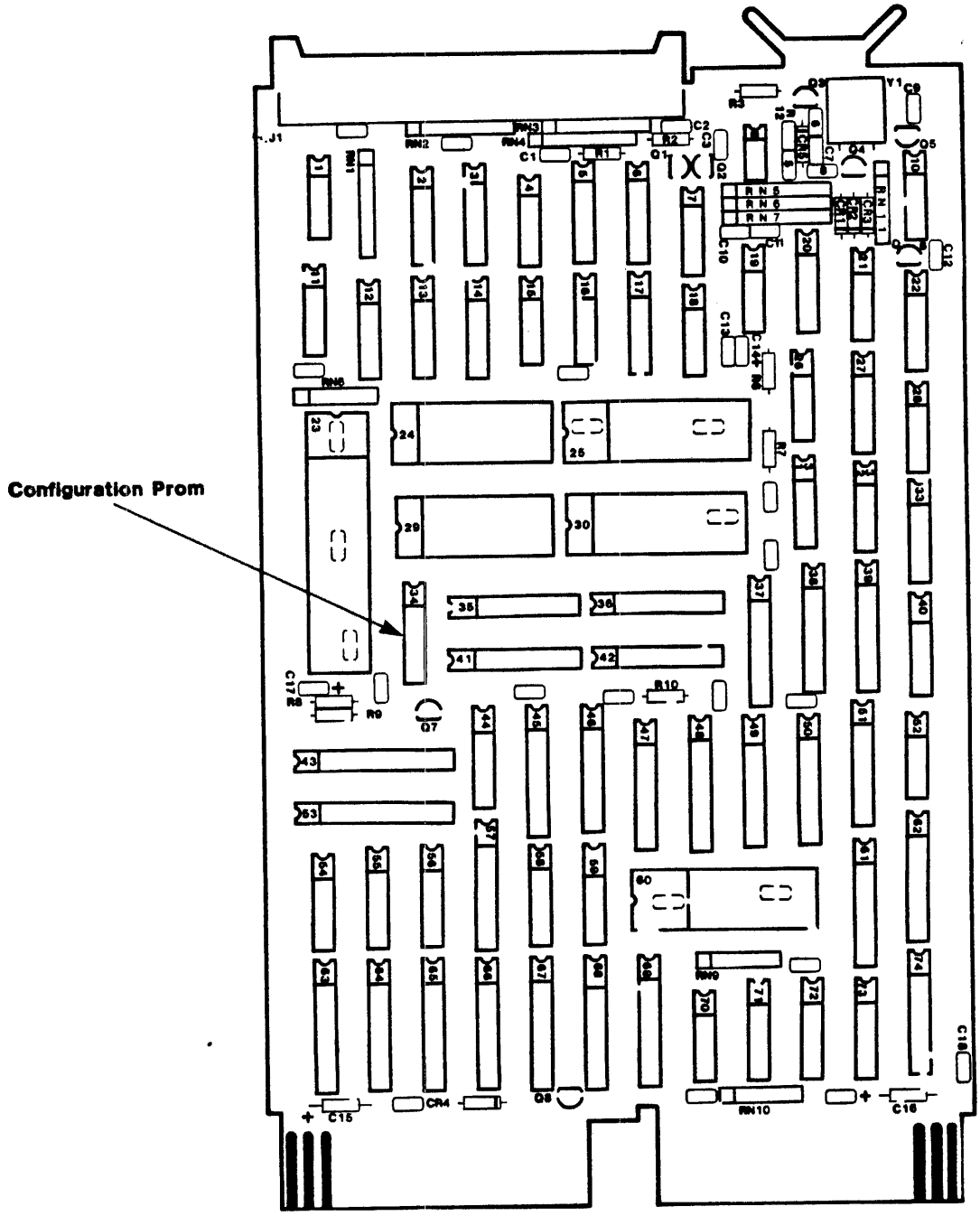


FIGURE 1.2
WINC Board Assembly

	EMULATION		
	RL01	**RL02**	**RX02**
Drive Characteristics			8" Floppy
Average Seek Time	85 ms	85 ms	91 ms
Maximum Seek Time	205 ms	205 ms	243 ms
Interleave factor	2:1	2:1	2:1
Burst transfer rate	625 Kb/sec	625 Kb/sec	62.5Kb/sec
Net transfer rate (Over entire disk, includes seeks)	259 Kb/sec	259 Kb/sec	18.3 Kb/sec
Logical Data Organization			
Heads	2	2	2
Cylinders	25	512	77
Sectors	40	40	26
Bytes per sector	256	256	256
Physical Data Organization			
Heads	2	4	2
Cylinders	306	306	77
Sectors	34	34	26
Bytes per sector	256	256	256

	EMULATION	
	RL01/02	**RX02**
Error Rates		
Hard (bits read)	1 per 10^{12}	1 per 10^{12}
Soft (bits read)	1 per 10^{10}	1 per 10^{9}
Seek (seeks)	1 per 10^{6}	1 per 10^{6}
Error control	16-bit CRC	16-bit CRC

Physical Dimensions

Subsystem Cabinet	Width: 17.6 inches (48.26 cm) Height: 5.2 inches (13.97 cm) Depth: 22.5 inches (58.42 cm) Weight: 38 lbs. (17.24 kg)

Power Requirements

Subsystem AC Power	110/115VAC ± 10%, 50/60Hz ± 0.5Hz 2.6 amps operating (max) 4.1 amps starting (max) 215/230VAC ± 10%, 50/60Hz ± 0.5Hz 1.3 amps operating (max) 2.0 amps starting (max) 300 watt maximum
Controller DC Power	+5V ± 5%, 3.8 amps typical 4.5 amps (max) +12V ± 10%, 0.1 amps (max)

CHAPTER 2

INSTALLATION

WINC-05 Controller to LSI-11 Installation

The controller will fit into the standard Q-BUS backplane. Be sure to power off the CPU before installing your card. The controller should be plugged into the next available or desired priority location dependent dual wide slot. Connect the 50-pin flat cable from the controller to the edge connector on the controller card.

NOTE

> Cable connectors are not keyed. Therefore, it is necessary to identify the Pin 1 position on both the male and female plug connectors by means of the imprinted arrow on the top edge of each connector. The flat cable also identifies Pin 1 with a red stripe. When connectoring the plugs, these arrows must be aligned to ensure correct pin and circuit connection.

System Ground

A single-point grounding scheme should be used to minimize group loop problems in a sub-system.

The common ground point, to which individual equipment grounds are connected, should be located electrically close to the building ground. The building ground is typically available at the main power distribution panel.

If the CPU is rack mounted, and if a solid electrical connection between the CPU ground and the rack mount can be ensured, then an attachment point on the sub-system chassis slide assembly may be used as the single-point ground. In such a system, all grounds should be returned to this single-point ground, thereby minimizing ground currents. The same single-point grounding system applies to a desk-top system as well.

Controller Modification Instructions

The **WINC-05** controller is supplied with the standard DEC address, vector and interrupt priority. The alternate address and vector the Winchester must be used if another RL01/02 is present in the system. The alternate address and vector for the floppy must be used if another RX02 is present in the system. Alternate address and vectors, bootstrap, and 22-bit addressing jumpers are described in **Table 2.1** (See **Figures 2.1** for jumper locations on controller card).

The bootstrap option allows the user to boot using a console device, autoboot upon power up, and disable the bootstrap.
To boot from the console device, the console must be at address 177560. Other bootstraps must be disabled or removed.

Autoboot will boot the system upon power up from DL0 without user intervention. A console device is not necessary.

If the user wishes boot from another PCB (i.e. BDVV11 or MXV11-A2), the controller's bootstrap must be disabled.

NOTE

The **WINC-05's** format routine will also be disabled.

The 22 bit addressing option must be enabled when using more than 256K bytes of memory. When using 256K bytes or less memory (18 bit addressing), this option must be disabled. See **Figure 2.4.** A pair of pliers is the recommended tool to use for removing jumpers.

Table 2-1. Device Jumper Options

	Standard	Alternate	Disable
RL01/02 (Winchester)			
PIO address	774400	775000	
Vector	160	120	No jumper on
Jumper	E4--E5	E5--E6	E4, E5, & E6
RX02 (Floppy)			
PIO address	777170	777150	
Vector	264	270	No jumper on
Jumper	E7--E8	E8--E9	E7, E8, & E9
Bootstrap			
PIO address	773000	773000	
Function	FROM TTY	AUTOBOOT	No jumper on
Jumper	E1--E2	E2--E3	E1, E2, & E3
22-Bit Addressing			
Function	Enable		
Jumper	No jumper on E10--E11		Jumper on E10-E11

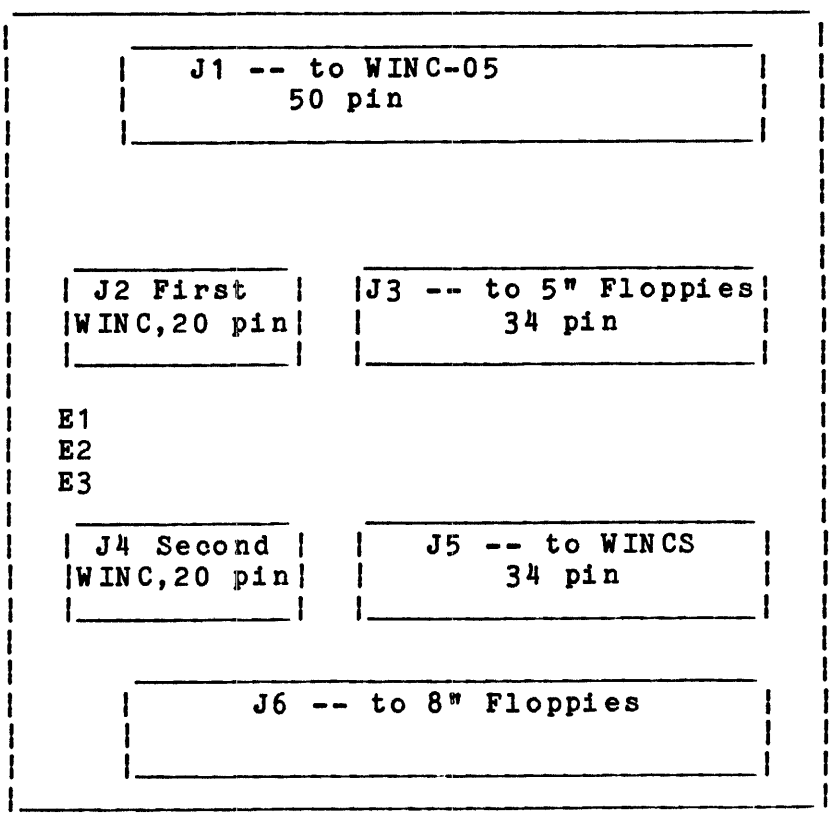
NOTE

There are three additional jumpers located on the PC board. These are for AED manufacturing tests only. <u>These jumpers should always be installed:</u>

Jumpers E12--E13, E14--E15, E16--E17

Figure 2.1

WINC-05 INTERCONNECT BOARD



Assembly Jumpering

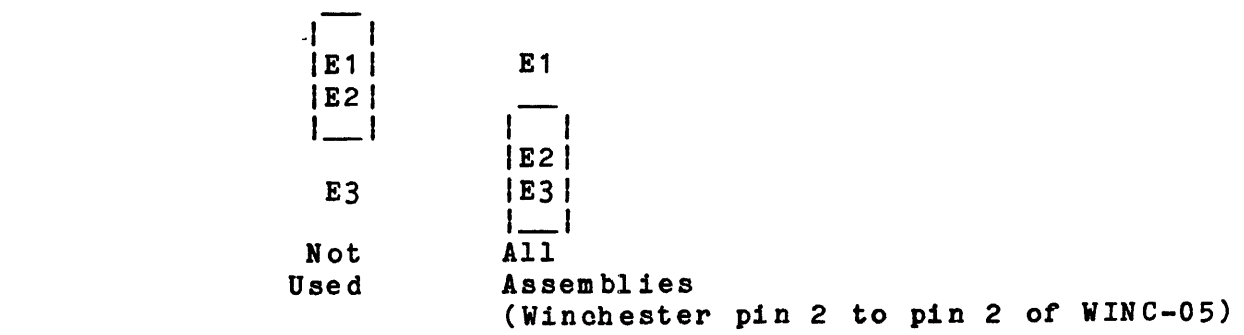


Figure 2.2

WINC-05/8/ -05/5 INTERCONNECT WIRING DIAGRAM, SINGLE DRIVE SYSTEM

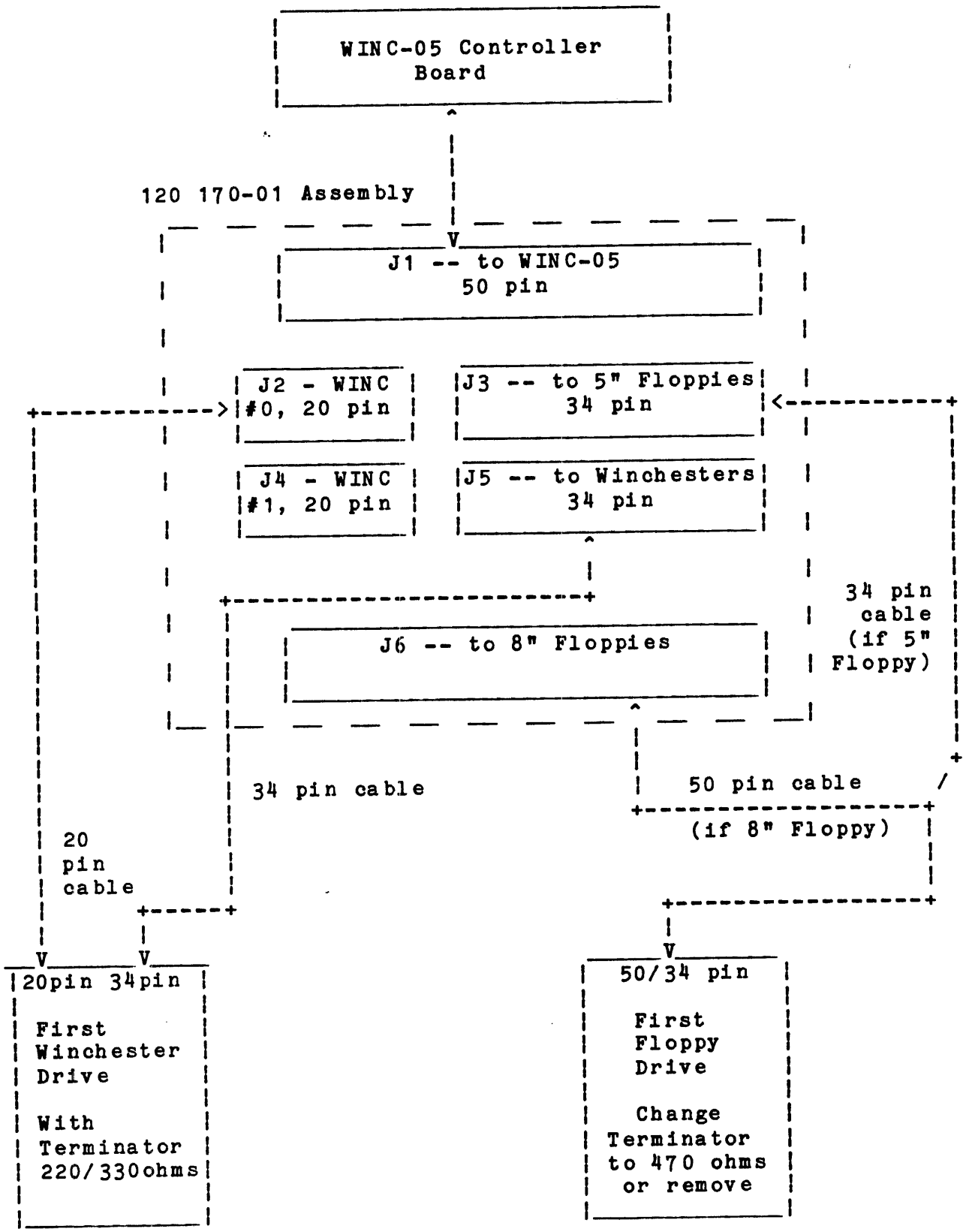


Figure 2.3

WINC-05/8/-05/5 INTERCONNECT WIRING DIAGRAM, DUAL DRIVE SYSTEM

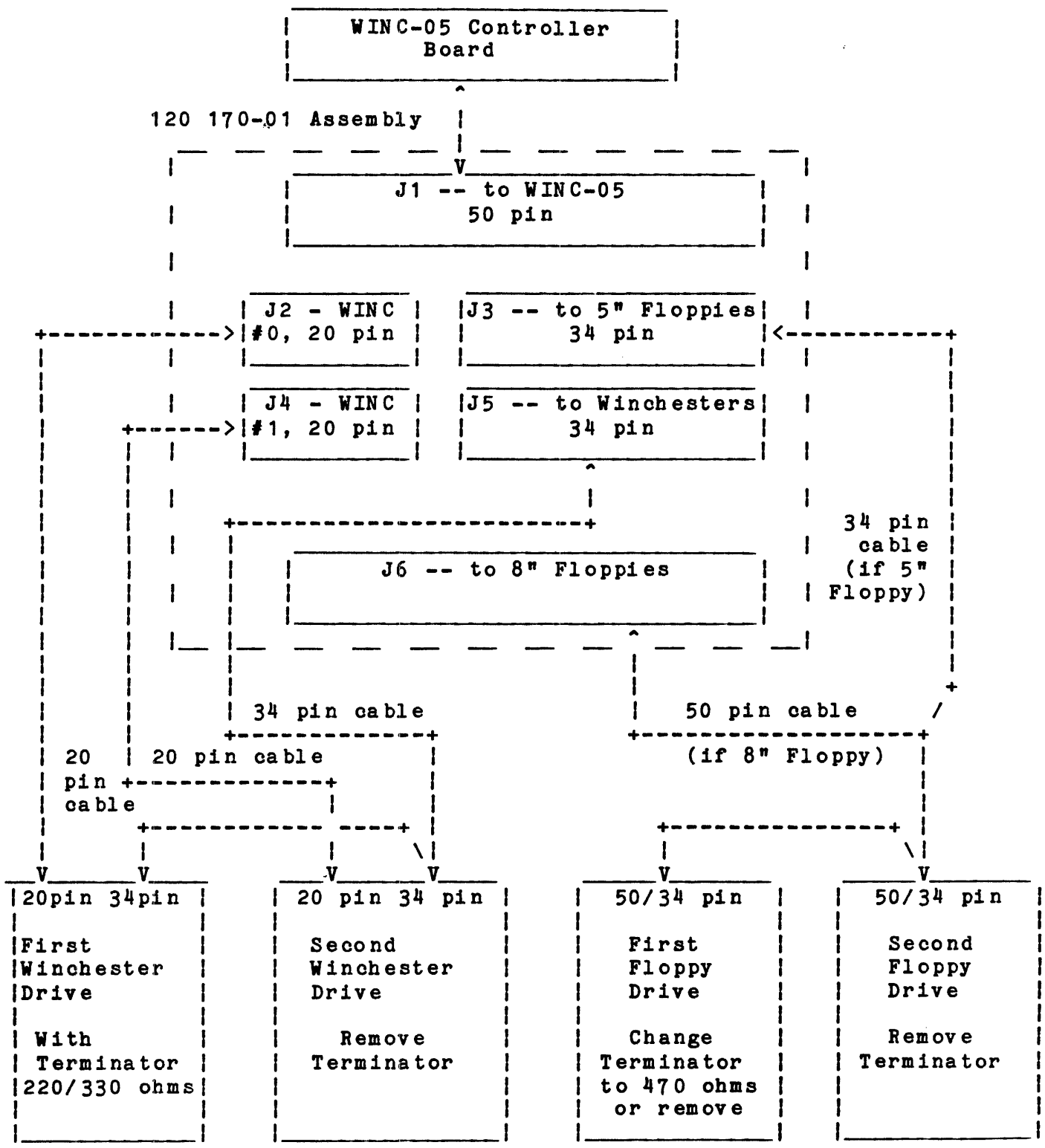
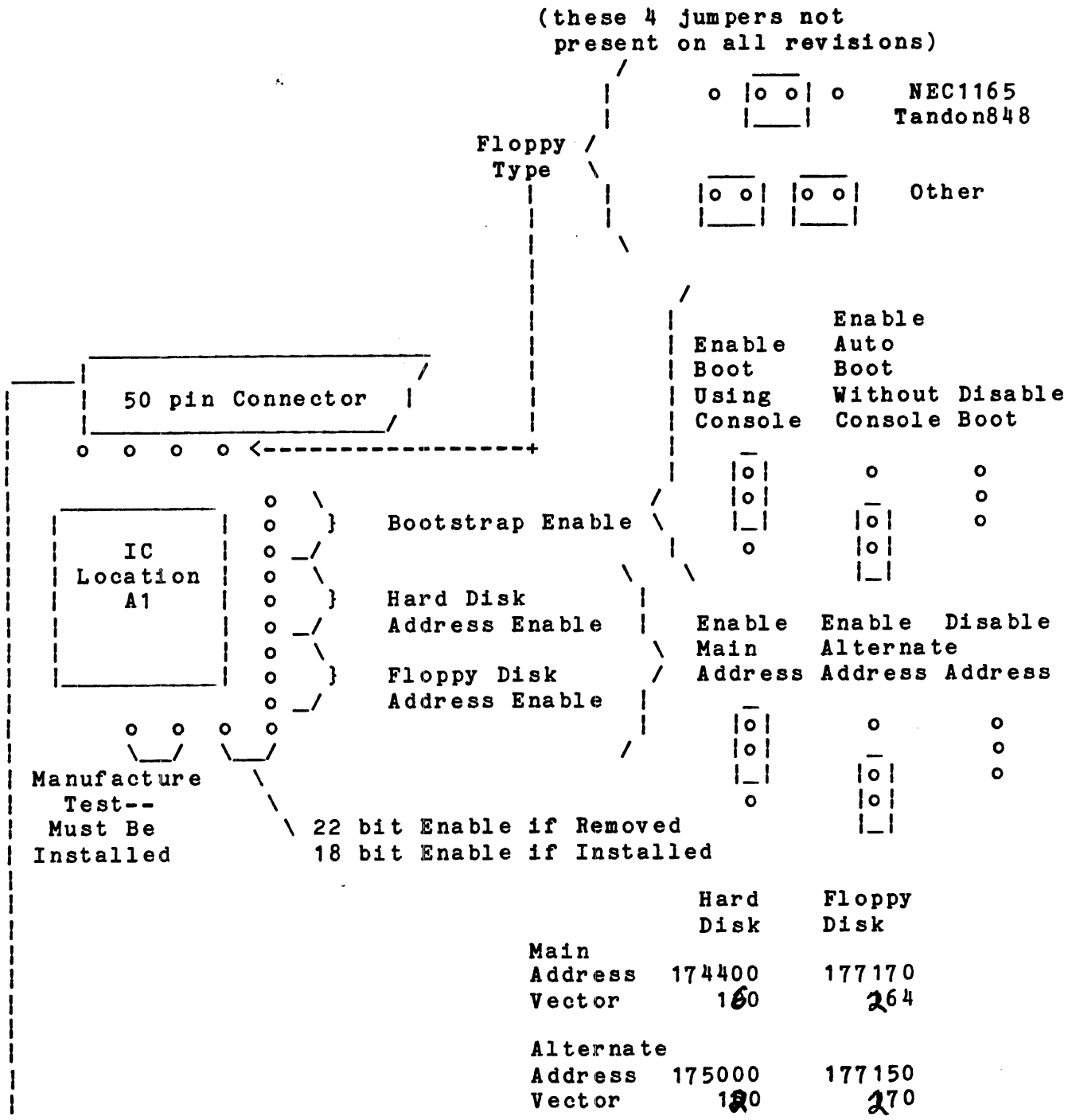


Figure 2.4

WINC-05/8, 05/5 CONTROLLER JUMPERING



	Hard Disk	Floppy Disk
Main Address	174400	177170
Vector	160	264
Alternate Address	175000	177150
Vector	120	270

CHAPTER 3

SYSTEM INTEGRATION GUIDE

Drive Specifications

The following Winchester drive specifications are assumed by the **WINC-05** with drives included in the **AED** subsystem meeting these requirements. Drives not supplied by **AED** must meet these requirements.

- Rezero with power ON is an optional specification as the **WINC-05** issues a restore command when it receives power.
- DRIVE READY must go false within 1 ms after +12V is applied. (This assumes +5V has been applied first). DRIVE READY must stay false until the drive is ready to seek, read, or write.
- SEEK COMPLETE must go false after the first step pulse and before the next step pulse is generated.
- Spindle motor speed must be within ± 2%.
- Voltage supply maximum ripple be less than 100mV RMS.

The **WINC-05** supports either the slow seek algorithm using a constant pulse interval, or the fully buffered seek algorithm (up to 25 us step interval). It does not support unique, missing pulse algorithms.

Drive to WINC-05 Interconnect Card

A PCB is used to interconnect the 50-pin flat cable to the standard Winchester 34-pin "A" cable, the 20-pin "B" cable, the 34-pin 5-1/4" floppy cable and the 50-pin 8" floppy cable. If the controller board is purchased separately, the user must supply the interconnect conversion PCB. These drive cable interconnections are defined in the following Table.

Table 3-1

Drive Cable Signals

34 Pin Cable		W05 CTR	5-1/4" WINC	5-1/4" FLOPPY	8" FLOPPY
Outputs					
DS0	drive select	26	26		1026
DS1		28	28		1228
DS2		30	30		1430
DS3		32	32		632

34 Pin Cable		W05 CTR	5-1/4" WINC	5-1/4" FLOPPY	8" FLOPPY
HS0	head select	14	14	32	14
HS1		18	18	--	--
HS2		4	4	--	--
STEP		24	24	20	36
DIRI	direction (in)	34	34	18	34
LOWC	low current	2	2	2	2
WG	write gate	6	6	24	40
Inputs					
TRK0	track 0	10	10	26	42
NDEX	index	20	20	8	20
WP	write protect/fault	12	12	28	44
RDY	drive ready	22*	22	--	--
SCPL	seek complete	8*	8		----
RDAT	floppy read data	8*	--	30	46
WDAT	floppy write data	22*	--	22	38
Outputs					
MON1	floppy motor on (8" head load)	16	--	16	18
MON2	2nd Winc motor	36	--	--	--

20 Pin Connector		W05 CTR	5-1/4" WINC	5-1/4" FLOPPY	8" FLOPPY
+RDAT0	read data -DS0	43	17		
-RDAT0		44	18		
+RDAT1	-DS1	41	17		
-RDAT1		42	18		
+RDAT2	-DS2	39	17		
-RDAT2		40	18		
+WDAT0	wrt data -DS0	47	13		
-WDAT0		48	14		
+WDAT1	-DS1,DS2	49	13		
-WDAT1		50	14		

Drive Signal Cables

All signals perform the same function as 8" floppies except where noted below.

1. **RDY** Drive ready is a function of the Winchester drive only.

2. **RDAT/WDAT** Winchester read and write data are not gated with drive select, therefore they operate as separate signals per drive. Since the writing is controlled by the write gate, two drives share one write data line. In addition, the signals are driven differently (at levels +3.5V, +0.5V).

   The floppy read and write data are driven as TTL signals. They also are time shared on signal lines used only for the Winchester drives (Seek complete, drive ready).

3. **SCPL** Seek complete. The Winchesters have a buffered seek operation where step pulses are output at a high rate (currently at 25 us per pulse) and counted by the drive. They are then issued at the stepper motor's rate. The controller then monitors seek complete to determine when the seek is done, rather than waiting for a fixed time.

4. **MON1** Motor on is used by DC motor floppy drive to turn their motors on when the signal is asserted. For AC motor drives, this signals is used as the head load control. On the DC motor drives, the heads are loaded with the motor on, with the exception of the QUME 242/YE Data YD180, which runs the motor continuously, and loads the head with the head load signal.

   MON2 (2nd Winchester) The motor on signals may also be used to sequence +12 V power for multiple drives. At motor start, the load current may be 4.6A, running current is 2.0A. Thus two drives will take 9.0A to start without sequencing, but only 6.5A with sequencing. The controller waits for the first drive to come ready (spun up), before turning on the 2nd.

5. **HS0-2** The Winchester head selection is binary, addressing one of 8 heads (4 platters). For the floppy drives, HS0 selects the 2nd side of a two-sided drive.

6. **DS0-3** The drive selects are assigned as follows:

   DS0 - 1st Winchester
   DS1 - 2nd Winchester
   DS2 - 1st floppy drive
   DS3 - 2nd floppy drive

7. Currently the **WINC-05** does not support hard sectored Winchester drives (e.g. the DMA/Memorex 5 Mby cartridge).

8. For 8" floppy drives not listed, the user should insure that the stepper power is derived from "head load/motor on", rather than from "drive select", since the controller does not delay for the stepper settling time after newly selecting the drive. For drives with a door lock, it normally is derived from "head load". This prevents opening the door during disk operations.

9. Cartridge Winchester write protect (20 pin cable, pin 5) and write fault (34 pin cable, pin 12) are collector or'ed to derive write inhibit.

10. 8" floppy two sided signal is required only for NEC floppies and must also be enable on the controller board (Jumpers 18-21). The signal is time shared on Winchester motor sequencing signal MON1.

Drive Strapping

Drives must be strapped for specific drive selection. The 5-1/4" floppy drives must also be strapped for head load control. The 8" floppy has many other options. Listed below are the strappings selection for several drive types.

The QUME 592 is similiar to the other 5-1/4" floppies including Mitsubishi M4853, Tandon TM100-4, and TEAC FD-55F. The Seagate ST4xx series is similar to other Winchesters, including the Tandom TM6xx, Syquest SQ306, Shugart SA6xx, IMI 50xxH, CMI CM5xxx, Rodime R02xx, etc.

5-1/4" Drives

Seagate ST4xx	**Qume 592**	**Shugart SA460**	**YE Data YD380**	
DS1	DS0	DS1	DS0	(install) first Winchester(DL0)
DS2	DS1	DS2	DS1	(install) second Winchester
DS3	DS2	DS3	DS2	(install) first floppy (DY0)
DS4	DS3	DS4	DS3	(install) second floppy (DY1)
MX	MX	MX	MX	remove (drive always selected)
--	HM	--	HM	install (head load = motor on)
--	HS	--	HS	remove (head load = select)
		MS		remove (motor on = select)
		SS		install (side = head select)
		SD		remove (side = direction)
		DD		don't care(door disturb)
		DO		don't care(door open)
		RI		don't care(ready = index)
		RD		don't care(ready = door closed)
		DA		remove (door lock = pin 4)
		WP		install (protect = covered notch)

Seagate ST4xx	Qume 592	Shugart SA460	YE Data YD380
			HD remove (gate out to pin 2)
			HL don't care(head load = pin 4)
			INU don't care(LED = pin 4)
			MR install (?)
			HN install (?)
			SF install (switch filter)
			ET remove (?)
			R don't care(gate out ready)
			P3 remove (? LED = off)
			P4 remove (? LED = off)
			P5 install (? LED = select)
			P6 install (? LED = blink at select)
			TD install (terminate select)
			T1 (install-last drive) terminate
			T2 (install-last drive) term. motor
			T3-T7remove (terminated on Winchester)

8" Drives

Qume DT8	Qume 242	Shugart SA810/860	Shugart 850	
DS1	DS1	DS1	DS1	remove first Winchester (DL0,..)
DS2	DS2	DS2	DS2	remove second Winchester
DS3	DS3	DS3	DS3	(install) first floppy (DY0)
DS4	DS4	DS4	DS4	(install) second floppy (DY1)
A	A	--	A	install (select = select)
B	B	--	B	remove (head load = select)
X	X	--	X	(install) second floppy (DY1)
R	R	R	R	don't care(ready status)
I	I	--	I	install (gate out index)
Z	Z	--	Z	remove (LED = select)
HL	HL	--	HL	install (step power = head load)
2S	2S	2S	2S	don't care(2 side flag)
DC	DC	DC	DC	don't care(disk change)
D	D	D	D	remove (LED = in use)
C	C	--	C	install (head load = head load)
W	--	--	--	remove (head load = in use)
Y	Y	--	Y	install (LED = head load)
DL	DL	--	--	remove (LED = in use)
DS	--	--	DS	remove (step power = select)
D1-D4	D1-D4	--	D1-D4	remove (binary select)
DDS	DDS	--	DDS	remove (binary select)
B1-B4	B1-B4	B1-B4	B1-B4	remove (head select = select)
RI	RI	--	RI	install (daisy chain index)
RR	RR	RR	RR	install (daisy chain ready)
WP	WP	WP	WP	install (enable write protect)
NP	NP	NP	NP	remove (disable write protect)
S1	S1	S1	S1	remove (side = direction)
S2	S2	S2	S2	install (side = side input)
S3	S3	S3	S3	remove (side = drive select)
HA	HA	--	--	remove (for test)
T40	T40	--	--	remove (for test)
--	SP	--	--	remove (stepper power)
--	SF	--	--	install (switch filter)
--	DLS	--	--	remove (door lock power options)
--	--	--	S	don't care(gate out sector)
--	--	--	800	install (soft sectored)
--	--	--	801	remove (hard sectored)
--	--	--	T1	(install-last drive)term. select
--	--	--	T2	(install-last drive)term. hdload
--	--	U9	T3-T6	remove (terminated on Winchester)
--	--	TR	--	don't care(true ready)
--	--	SI	--	install (internal write current)
--	--	SE	___	remove (write current = pin 2)
--	--	MS	--	remove (motor on = select)
--	--	MO	--	install (motor on = head load)
--	--	MD	--	no care 3sec delay before mot off
--	--	PD	--	remove (stepper power down)
--	--	TS	--	remove (internal data separater)

TANDON
TM848

210801	drive assembly number
-002	
210772	circuit board number
DS1	remove first Winc (DL0,..)
DS2	remove second Winc
DS3	(install) first floppy (DY0)
DS4	(install) second floppy (DY1)
--	install (select = select)
--	remove (head load = select)
--	install (head load = head load)
R	don't care(ready status)
--	install (gate out index)
--	remove (LED = select)
HL	install (step power = head load)
2S	don't care(2 side flag)
DC	don't care(disk change)
D	remove (LED = in use)
--	install (head load = head load)
--	remove (head load = flip flop)
TR	remove (true ready)
IC	remove (internal low current)
XC	install (external low current)
--	install (LED = head load)
DL	remove (LED = in use)
--	remove (step power = select)
DM	out (diagnostic mode)
B1-B4	remove (head select = select)
--	install (daisy chain index)
--	install (daisy chain ready)
WP	install (enable write protect)
NP	remove (disable write protect)
S1	out (side = direction)
S2	install (side = side output)
S3	out (side = drive select)
M1	in (select to motor on)
--	out (MCx to motor on)
M3	out (?)
M4	in (head load to motor on)
MC1	don't care(pin 4 to motor off)
MC2	don't care(pin 6 to motor off)
MC3	don't care(pin 8 to motor off)
MC4	don't care(pin 24 to motor off)
--	out (?)
--	out (+24V to +12V)
MOH	out (motor on high true)
MOL	out (motor on low true)
PS(3)	in etch (power save)
NL	don't care(non latched in use)
LL	don't care(latched in use)

Drive Termination

Drives utilize terminators for input signals. Only one drive in a system should be terminated. This termination is usually placed on the last Winchester drive, even if the floppy drives are slightly further along the cable. On drives with removeable resistor packs, **AED** will install a 450 ohm resistor pack on the last floppy drive. However, the **WINC-05** can not drive sufficient current to terminate the floppy with the standard 150 ohm value terminator.

Drive Control Algorithms

The **WINC-05** continuously monitors the drive ready signal of the first Winchester drive to determine whether cabinet power is on or off. This test is disabled if the controller has the RL interface enable jumper removed. If power is off, the controller drops the motor control signals to the second Winchester and to the floppies, to limit the current surge when the cabinet is turned on. When the first drive becomes ready (or when the spin up timeout is exhausted, normally 20 seconds), the controller turns the second drive motor on (if configured), and waits for it to come ready. It then turns on the motor to the floppy drives, testing whether a disk is inserted or not. For CPU BUS initalizations the controller skips the Winchester spin up sequencing, but tests floppy drives for disk insertion.

When a RL drive orientated command is issued, the controller first selects the drive and tests for ready and seek complete. If the command is a seek, the direction is set, and step pulses are generated. For drives with buffered seek mode, a pulse rate of 25 us is used with a pulse wide of 6 us, without a buffered seek, the pulse rate of 3.0ms is used. The head is also selected. The controller will then set an internal flag and test for seek complete in its idle loop. This will allow overlapping of RX commands. If the command is a read or write, the controller first tests if a seek is still in operation. If it is, the commands are delayed until the seek is complete, then performs the read or write operation. The controller first finds the correct sector header (except for the read data without header check command), then either reads the data sector, or asserts write gate and writes the data sector. The command continues until the word count is exhausted, sector by sector. If a logical track spans two physical tracks, a seek will automatically be performed in mid-transfer.

For formatting, the controller seeks to each track, writes a pre-index fill pattern, then waits for the index pulse from the drive and writes both sector headers and data (data = zeros). When complete, the controller finds the headers of the bad block file, and writes the data in the correct bad block file format. However, it does not locate any bad blocks on the disk. The user must run a utility program for that (i.e. DEC diagnostic program ZRLMB1, or RSX11 utility BAD).

When an RX command is issued which is drive oriented, the controller tests whether the motor is still on from a previous operation, or if the head is still loaded on drives whose motor is always on. If not, the motor is turned on (or head is loaded), and a motor on delay counter is started. This is normally 1.0 second for motor on, and 50 ms for head load. The **WINC-05** then re-enters its idle loop until the timer timeout (allowing RL commands to be executed). When the timeout occurs, the controller then seeks the drive to the proper track, normally with a 3.0 ms pulse interval, a 11 us pulse width, and a 15 ms step settling time. The read or write is then performed similarly to the RL read or write, with the exception that only one sector is transferred per command.

With the exception of index during formatting, the controller's logic does not use any status information from the floppy drive. Drive ready is determined by successfully reading a sector from the disk. Double-sided is determined by successfully reading a sector from side 2. Disk changes are handled by testing drive density before an operation, if the motor (head load) had been turned off between commands.

Formatting the floppy disk is similar to formatting the Winchester, with the exception that there is no bad block file on the disk.

Drive Mapping

The standard RL01/RL02 and RX02 have a different track and sector from the drives used on the **WINC-05**. Therefore, the controller must ascertain where the standard tracks and sectors are located on the physical drive. The following information lists the different drive structures.

	RL01	**RL02**	**RX02**	**"RX03"**
Heads	2	2	1	2
Cylinders	256	512	76	76
Sectors/Track	40	40	26	26
Bytes/Sector	256	256	256	256

	ST506	**ST412**	**ST419**	**Rodime R0204**	**Qume 592**
Cylinders/Drive	153	306	306	306	80
Tracks/Cylinder	4	4	6	8	2
Sectors/Track	34	34	34	34	16
Bytes/Sector	256	256	256	256	256

Therefore, an RL02 cylinder 0, head0, sector 0-39 would be stored on a Seagate ST412, on cylinder 0, head 0, sector 0-33 and on cylinder 0, head 1, sector 0-5. The **WINC-05** may need to do a seek while reading one RL02 track.

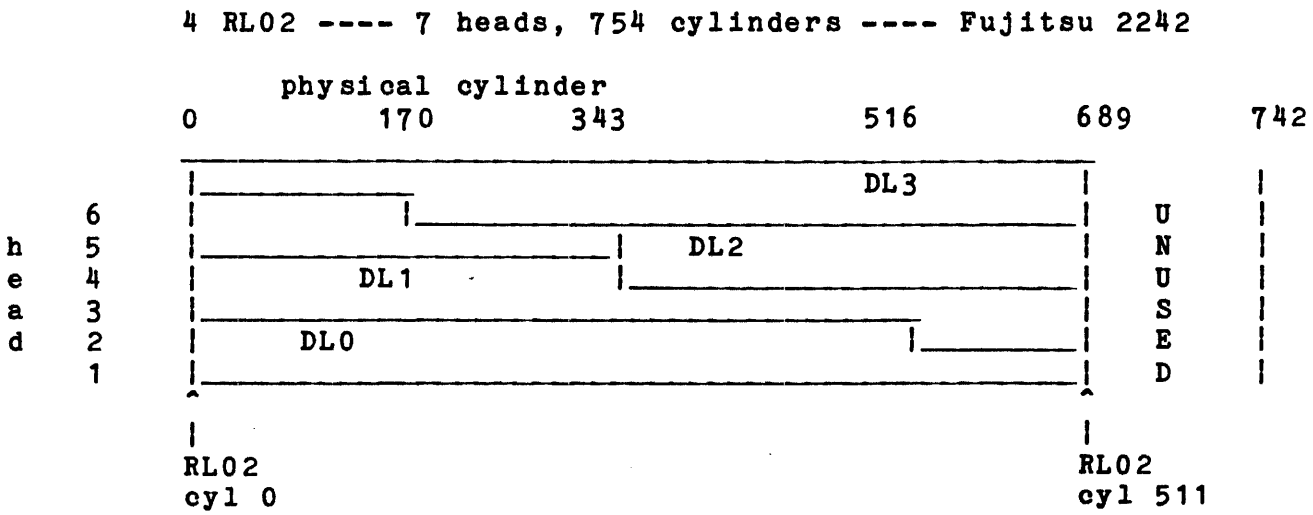
For drives containing more than one RL logical drive, the **WINC-05** formats the drive to put each RL drive on separate heads of the drive, such that logical cylinder 0 of each RL drive is on physical cylinder 0 (hence will be defect free). As an example, the Seagate 419, and the Rodime R0204 are shown.

ST419 as 3 RL01's:	DL0 = heads 0,1 DL1 = heads 2,3 DL2 = heads 4,5
ST419 as RL02 + RL01:	DL0 = heads 0-3 (RL02) DL1 = heads 4-5 (RL01)
R204 as 2 RL02's:	DL0 = heads 0-3 DL1 = heads 4-7

In addition, more than one physical drive can be supported. This second drive does not have to be the same as the first drive, however, a logical drive cannot be located on two drives. For example, using the Seagate ST419:

1st ST419	DL0 = heads 0-3 (RL02) DL1 = heads 4,5 (RL01)
2nd ST419	DL2 = heads 0-3 (RL02) DL3 = heads 4,5 (R101)

The **WINC-05/8** has the ability to to handle Winchester drives with voice coil head position actuators, which require one data surface to be dedicated to servo information rather than data. This requires that a logical RL drive must be formatted on some number of heads plus a partial head, thus storing part of two logical RL drives on a single head. An example of the resulting **WINC-05** format is as follows:



Most drive manufacturers certify that drive cylinder 0 will be error free, therefore the **WINC-05** always stores RL cylinder 0, head 0 of each logical drive on the physical cylinder 0 of the drive.

The controller access algorithm accesses all sectors per head, then all assigned heads per cylinder, through the cylinders, storing sequentially RL sectors, heads, and cylinders.

To compute formatted storage on a drive, compute the total tracks (=vendor heads multipled by vendor cylinders). Storage of a single RL01 requires 603 tracks, a single RL02 requires 1205 tracks. There typically will be some remaining formatted tracks which will not be usable due to the fixed size of the RL units.

Since each RL drive's sectors are in known locations, each RL drive may be formatted without affecting data on any other RL drive on a given physical drive.

The 5-1/4" floppy drive is designed in a less complex manner, using 2-sided disks to emulate a single sided RX02.

Track n, sector	1-16 are on track n, head 0, sector 1-16
Track n, sector	17-26 are on track n, head 1, sector 1-10 and track n, head 1, sector 11-16 are unused.

The 5-1/4" floppy disk will operate only as a single-sided, double density RX02 format.

8" disks and 5-1/4" RX50 disks are media compatible, and do not map tracks and sectors.

Configuration PROM

The configuration PROM allows for different parameters from a variety of disk drive vendors. **AED** utilizes a 256 x 4 prom equivalent to Signetics 82S129. Any prom may be used with an address access time less than 200 ns. The chip select access time should be less than 200 ns, and input and output current less than the 82S129. A standard PROM is included with the controller. A nonstandard PROM must be purchased from **AED** for drives supplied by the user, or may be generated by the user.

- Drive indentifier
- Mapped, or unmapped (unmapped for floppy)
  Starting unit number if mapped
- Starting head number
- Number of physical heads per logical drive
- Number of physical cylinders
- Cylinder for "low current" and precompensation switch
- Seek step interval
- Seek pulse width
- Drive spin up time
- Head load/Motor on delay for floppy

Exact Format of the Prom

An actual listing of a configuration PROM and comments to assist in the interpret the listing can found in **Appendix A.**

For the 8" floppy drives, two series of configuration PROMS are available. The first assumes that the motor is always running and signal "head load" only loads the head. The controller delays 50 ms before transferring data. This is used by the QUME DT8/242 and the SA850. The second assumes that the motor is started and stopped by the signal "head load". The **WINC-05** delays 1.0 second before transferring data. This is needed for the SA810/860, and the TM848. The standard configuration PROMS use a 3 ms step rate and 15 ms step settling delay, and are set for double sided operation.

Drive Power Protect

The **WINC-05** has circuits to prevent data loss during power up/down operations. The controller monitors Q-BUS signal DCOK, which states that "all power supplies in spec". This signal is received by a FET, and drives a very low saturation voltage transistor which powers down the output drives, including "write gate" and "drive select". This method provides protection when the voltage is in the range where IC's may malfunction.

This method also provides protection when the LSI-11 powers up/down independently from the drive cabinet. It should be warned that the user's system must provide this signal during the power down, as well as power up cycles. When the LSI-11's power is left on and the drive cabinet is powered down, protection is provided by the drive itself, and is part of the vendor drive specification.

Drive Power Supplies

The switching power supply which is the most common for system integrators, is also notorious for creating specific problems with disk drives. The following are the major problems seen by **AED**, along with recommendations to alleviate any potential problem.

It is apparent that some switching supplies radiate excessive EMI within a cabinet. Since the floppy disk drives do not have perfectly shielded drive heads, some will pick up the radiation in the heads and head cable. This will cause randomly located soft errors when reading from the drive. A solution for this is to provide additional shielding around the floppy drive itself. This is typical on 5-1/4" floppies, but not likely on 8" floppy disks.

Almost every Winchester drive will internally connect logic ground to their frame. Ground loops can be generated in the system, caused by the switcher's high frequency operations. This may cause random soft data errors in the Winchester (or the floppy, if common power cabling is used). Two solutions are known for this problem. The first is to isolate the Winchester's frame from the enclosure's frame. The second is to use a "common mode" line filter in the DC cables between the power supply and the drives. A common mode line filter has series inductors in the DC and DC RETURN conductors, with high frequency capacitors between DC, DC RETURN, and NEMA GROUND.

Winchester Write Protect Switch Capability

The microcode on the **WINC-05** controller allows the user to implement write protection for each logical RL drive. This implementation requires the addition of WP switches on the physical unit. See **Figure** 3. for specific current requirements necessary for switch implementation.

The WP switches will drive 4 cable status signals during that time where there is no Winchester activitiy. They are tested by the controller during the idle loop, approximately once per 50 milliseconds. Should the controller remain continuously busy, the switches will not be updated. If a WP switch is set, the controller sets that drive into a write protected mode until the switch is reset, and all write operations to that drive inhibited and a command error is posted to the software.

Logical Unit:	DL0	DL1	DL2	DL3
Signal:	-WFLT	-RDY	-TRK0	-SCPL

When (-DS0 = -DS1 = -DS2 = -DS3 = 1), a high level (not asserted) on the appropriate signal represents write enabled. A low level (asserted) represents write protection.

The controller disables all drive select signals during idle time (approximately 50 ms after the last command). The statue of all selects off can be used to generate a controller idle display. This idle display however, can only monitor the state of a physical Winchester drive, rather than each logical RL unit. This is due to the fact that only the drive select signals are available.

It should be noted that the write protect function is a microcode operation, and will not protect against hardware malfunctions. It provides only for protection against software and format write attempts.

Write protection of the floppy disk drives remains unchanged, utilizing write protect notches provided by the floppy drives.

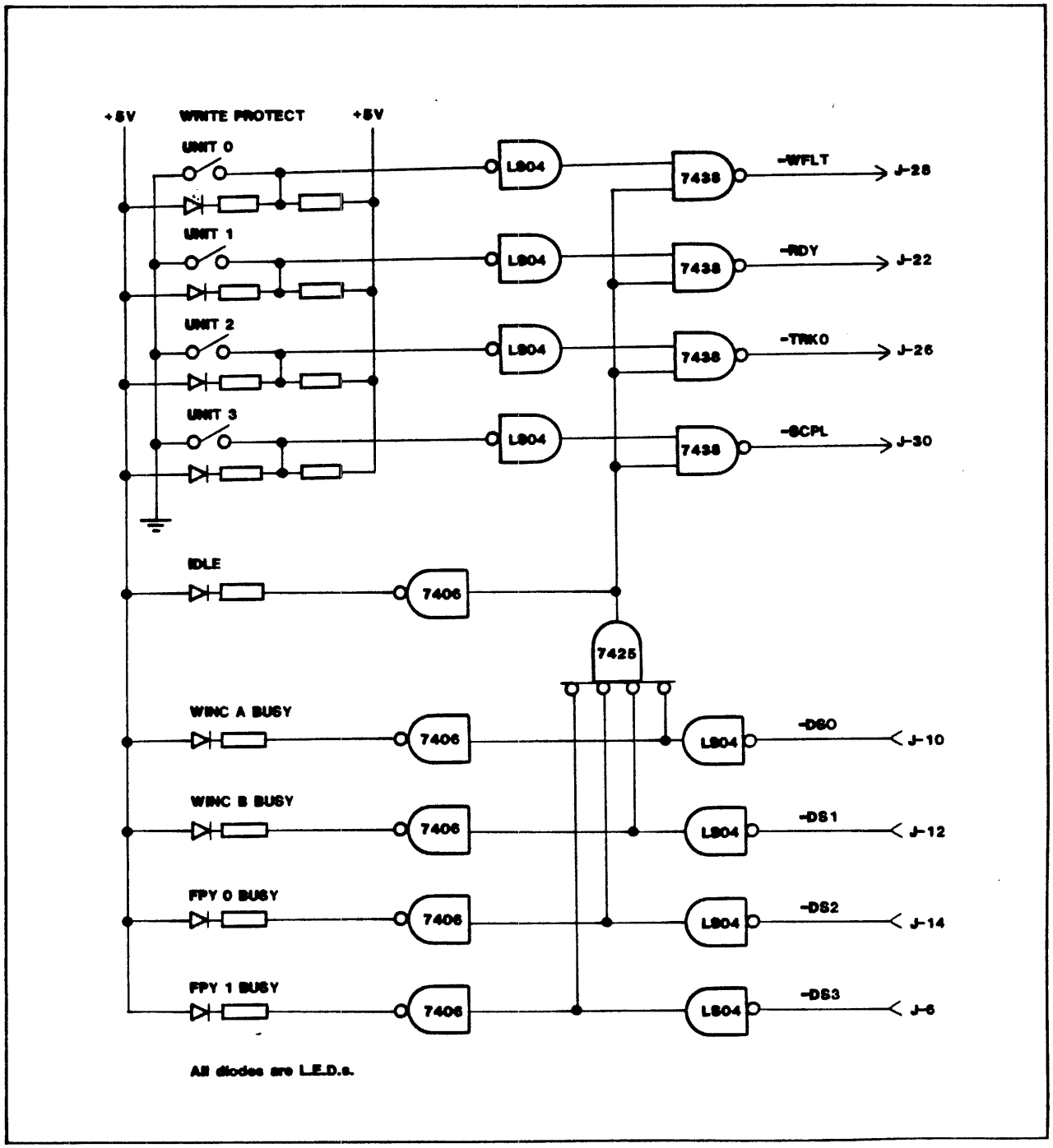


FIGURE 3.1
WRITE Protect & Drive Activity

System Level Considerations

DMA Bandwidth

The **WINC-05** with an interleave of 2:1, assumes that most of the DMA bandwidth is available to the controller. If other high bandwidth devices are on the BUS, a **WINC-05** transfer may not complete within one sector time, and will result in missed drive revolutions, slowing the transfer to one sector per revolution.

The algorithm used by the **WINC-05** for interleave of two is includes a request DMA transfer; once granted, keep control of the BUS until complete (128 words). If any other device requests a DMA cycle, relinquish the BUS, but immediately re-request a DMA cycle, so that the controller will capture control of the BUS once the other device is finished. This algorithm is usually named "self throttling" access method.

Should the competing device fail to relinquish the BUS, or if it requests enough cycles during a transfer, the **WINC-05** will not complete its transfer in time to access the next disk sector before the disk has rotated past the next sector, requiring the **WINC-05** to wait for the next revolution of the disk to read that particular sector. The total time required to transfer a sector by the **WINC-05** is 330 microseconds, the time available before the next sector is 560 microseconds (130 us spare, assuming an LSI-11/23 and MSV11D memory).

In effect, the LSI-11 is locked out for the duration of the DMA transfer, however, other DMA devices get serviced during this interval. Effectively, the **WINC-05** has the lowest DMA priority of competing DMA devices, regardless of position in the BUS priority chain. It will get at least 50% of BUS cycles if competing against a lower priority device.

The **WINC-05** with an interleave of 3:1 assumes most of the DMA bandwidth is required by other devices.

The algorithm used is to transfer one word per DMA request, then make the next request. This is the method described in the DEC LSI-11 BUS handbook.

This allows for sufficient time for other DMA devices to access the BUS without degrading the **WINC-05** to the point of missing disk revolutions. The total time required to transfer a sector by the **WINC-05** is 500 microseconds (assuming no contending DMA requests), the time available before the next sector is 960 microseconds (460 us spare, assuming an LSI-11/23 and MSV11D memory). **NOTE:** On **WINC-05** controllers delivered before 9/30/83, timing is 610 us for the transfer with 960 us available (350 us spare).

Floppy Disk DMA Operation

The **WINC-05** handles BUS cycles similar to 3:1 interleave. This provides a transfer time per word of 4.9 micro seconds (average).

DMA Performance Summary

Typical BUS requirement analysis for the **WINC-05**.

	Interleave of 2:1	**Interleave of 3:1**
DMA throughput requirements		
Time on Bus	330 us	280 us
Time off Bus	630 us	1160 us
Total per Sector	960 us	1440 us
Percent available (to LSI or other DMA)	66%	81%
DMA request latency requirements		
Transfer Time	330 us	280 us
Time until next Sector	480 us	960 us
Spare Time	150 us	680 us
Allowable competing Peak DMA time	150us/480us	680us/960us
Interference for non-missed revolutions	100 wrds/480us =210 Kwd/sec	453wrds/960us =450 Kwd/sec
Maximum LSI BUS bandwidth (assume 1.5 us/xfer)	(=667 Kwd/sec)	

Interrupt Considerations

System Interrupt Bandwidth

It must be noted that using the **WINC-05** with an interleave factor of 2:1 can affect interrupt performance. During **WINC-05** DMA cycles, the LSI will be locked out of BUS cyces for 330 microseconds each sector. Other interrupting devices with are maximum service interval less than 330 microseconds will miss interrupts. The method utilized to correct this situation is to use the **WINC-05** with a 3:1 interleave, allowing the DEC specified interrupt latency to be met.

If additional devices on the BUS interrupt the controller more than once during the on time of 300us, the system will fail. These additional devices may have a problem at 2:1 interleave are high speed D to A and A to D converters which operate on an interrupt per conversion. The quad serial line board should not experience problems, even at a 19,200 baud rate (interrupt per 570 us per line). Most other high speed devices will be using DMA data transfers, rather than interrupts.

Four Level Interrupt Support

The **WINC-05** implements the true 4 level interrupt algorithm. Therefore, the **WINC-05** can be used in the "position independent" configuation as defined in the DEC LSI-11 handbook.

For example, the **WINC-05** (at interrupt priority level 5) can be located before a priority level 6 device in order to minimize DMA request propagation delays, while allowing interrupt priority to be given the level 6 device rather than the **WINC-05**.

Note that position dependent devices must be placed after all position independent devices as defined in the DEC LSI-11 BUS handbook. Some current position dependent devices are the DEC serial interfaces (DLV11-J, DLV11-E) and the RX02 (from DEC and others). Interrupts will be services out of priority order unless the dependent devices are handled correctly.

Device Independence

The **WINC-05** implements two independent controller devices on one board. Each of these devices, (RL01 and RX02) appear to be accessed simultaneously through system software, producing results similar to two physically separate controllers. Producing simultaneous access results is derived through the access of one device (RL01) while the other, (RX02) is performing an arbitrary function. Each device will perform individual operations regardless of the state of the second device.

The **WINC-05** executes commands on a device sequentially. Therefore, upon simultaneous commands to the RX02 and RL02 devices, the first command detected by the **WINC-05** will be executed, followed by the second. While one of these devices is busy, the **WINC-05** may be accessed on the other device for any legal function. In addition, the device with a command in progress can also be accessed in legal ways, e.g. a "test for controller ready" loop, output CSR "interrupt enable = 0", output RX02 initialize function.

RX02 22-BIT Addressing Extension

With the introduction of 22 bit addressing, questions regarding the RX02 emulation which only supports 18 bits arose. Since DEC supports their 18 bit controller through system software, **AED** does not offer a non-emulating variation of the controller.

Under RSX11M, support of the 18 bit RX02 in 22 bit systems was added in revision 4.1B. RSX11M PLUS added 22 bit support of the RX02 in revision 2.1B. The drivers create an intermediate buffer (DYCOM) in the lower 18 bit of memory, then copies the data from there into locations above 256 K bytes.

For RT11, support of the 18 but RX02 in 22 bit systems under the XM monitor has not yet been added as of revision 5.0. Under the FB/SJ/BL monitor in revision 5.0, the extended memory can be accessed as a "RAM disk" with the VM driver.

CHAPTER 4

SOFTWARE INSTALLATION

The following explains the bootstrap operation and media initialization. For **WINC-05** operation, a DEC-supplied DL and DY driver must be a part of your Operating System. A System Generation is not required if a loadable DL or DY driver is used. Please refer to DEC's Operating System manual for additional details.

When power is initially applied to the **WINC-05**, a power-up built-in test will be executed to check all internal functions. Microprocessor ALU operations and conditional branches are checked, and verification of the internal buffer is done. Following this test, the controller will check to determine if the drives are powered up to their appropriate speed. If so, a rezero will be issued which will restore the drive heads to Track 0. If a drive is not ready, this operation will not be performed. The controller and drive ready bits will be posted in the CSR register upon completion of the drive spinup and rezero.

If an error is detected, an error status will be posted in the CSR register. Please refer to **Chapter 5** for Troubleshooting information.

Bootstrap/Format Monitor

The Bootstrap/Format Monitor is an integral operating program on the controller the allows you to boot from any device as well as to do off-line formatting of both Winchester and floppy drives. The **WINC-05** also allows formatting from DEC Operating System format routines. See your DEC manual for further details.

This program is designed to allow formatting the Winchester or floppy with minimal keystrokes. You have the flexiblity of selecting Winchester interleaving for your particular system application and system overhead. One logical unit may be formatted without disturbing another logical unit on the same physical drive.

Another advantage of this program is seen when formatting floppy diskettes. The Monitor is capable of formatting unformatted diskettes. You have the option of formatting either single density or double density 8" diskettes. The controller will automatically recognize single or double sided diskettes.

Format Description

Disk media must be formatted by recording header information and data field before the drives may be used. Drives received from **AED** will be pre-formatted, thereby requiring an initialization of their directory only. (i.e., INIT command). Drives not received from **AED** should be formatted using the **AED** Boostrap/Format Monitor program.

The controller's **on-line format routine** is used to write headers and data sectors, as well as initialize the bad block file on the disk media. To verify the data sectors, and to record any bad sectors in the bad block file, execute the **FORMAT** routine (verify only) for RT11, or the **BAD** routine for RSX11M.

Format Execution

The **AED** format routine is initiated by entering the Boostrap/Format Monitor. This is done by performing the following procedure, using the appropriate Winchester or floppy example.

Enter	Display
BREAK KEY	@
173000G	@173000G
--	AED>

This will return an AED> prompt. Once inside the monitor, both bootstrap and formatting can be performed.

Winchester Format Example

Enter	Display
BREAK KEY	@
173000G	@173000G
--	AED>
*XI2 (interleave factor)	AED>XI2
XU0 (Winchester unit no.)	AED>XU0
--	Format DL0 (ILV=2);
	Are your sure (Y/N)?

Y or N.

* An interleaved factor of 2 or 3 may be selected, depending upon system requirements. This selection should be determined by the host CPU speed, memory speed, and system overhead. Most systems will use an interleave factor of 2, allowing the controller to access every other sector during multiple-sector I/O operations. If the system overhead is too much for the selected interleave, the controller will miss sectors and will require extra revolutions, causing a reduction in system throughput. Should this occur, the interleave factor should be be increased to 3, which will allow additional time between sector accesses.

Floppy Disk Format Example

Enter	Display
BREAK KEY	@
173000G	@173000G
--	AED>
*XD2 (density selection)	AED>XD2
XU0 (floppy unit no.)	AED>XU0
--	Format DY0 (DEN=2);
	Are your sure (Y/N)?
Y or N.	

* Either single or double density 5-1/4" & 8" (XD1: 8" only, XD2: 5-1/4" & 8"), or RX50 (XD5: 5-1/4" only) can be selected.

The formatted drive is ready to be check for bad blocks and initialized with a directory. (i.e., INIT DL0: or INIT DY0:).

Bootstrap Procedures

The **WINC-05** features an onboard 512 byte bootstrap ROM which allows booting from either the Winchester or floppy drives. This feature makes the controller equivalent to the DEC BDV11 bootstrap PCB.

The ROM program communicates via the system console to initiate a bootstrap operation. An option on the board allows automatic unattended bootstrapping or disabling of the bootstrap function. **See Chapter 2, Table 2.1.**

Due to the architecture of the LSI-11/23 PLUS computer, **AED's** boot ROM cannot be used. Use the boot ROM located on the 11/23 PLUS board.

Boostrap Description

The controller provides bootstrap capability from the disk drives that are directly connected.

The controller bootstrap is a program residing at starting address 173000 (octal) to allow use of the standard CPU power up boot function. The bootstrap program uses the CPU console device for control. The CPU console must be at address 177560 for the bootstrap to function.

This function will load head 0, track 0, and sector 0 of the selected drive into CPU memory starting at the memory location 0. If no drive is specified, the system will default to DL0. It then loads the unit number into the CPU's register 0 and transfers control to the CPU at location 0.

The bootstrap program will load from the **WINC-05**, drive DL0, if you fail to type another function within 90 seconds after the boostrap program begins execution. To provide a bootstrap command to a device attached to the system, even at an unattended site after a power failure, a jumper selectable autoboot is available.

Autobootstrap Option

A jumper option is provided, as explained in **Table 2.1**, to automatically bootstrap from the controller drive DL0 at power up, without delay and without the necessity of a console device at address 177560. If this option is enabled, at the time the CPU performs the power up jump to address 173000, the controller will bootstrap from drive DL0. If drive DL0 is not ready, the controller will keep trying until the drive is ready, or until the CPU is manually halted.

Manual Bootstrap Methods

The **WINC-05** can also manually boot from any bootable device on the BUS. To boot from the controller when power is applied and autoboot is inhibited, and a boot has been copied to DL0, perform the following:

Enter	Display
BREAK KEY	@
173000G	@173000G
	AED>
[CR] or DL0 [CR]*	AED>[CR] or AED>DL0 [CR]

[CR] = Carriage Return
* = DL0, DL1, DL2, DL3 or DY0, DY1 may be selected

To transfer control back to the host's ODT monitor, press the BREAK KEY.

NOTE

When a **WINC-05** subsystem is received from **AED**, no boot is present. You must boot from another device until the boot can be placed onto DL0.

Boostrap Inhibit Option

A jumper option is provided to disable the bootstrap function. This will allow another bootstrap ROM to be located at address 173000. The jumper is removed to disable it.

System Software

Double-sided Floppy Operation

In order to operate the 8" floppy disks as double sided drives, a patch must be made to the software drive. This patch is available from **AED** as an autopatch module, applied to the driver after all DEC modifications are applied. This patch is available for both RT-11 ad RSX-11M Operating Systems.

Because DEC systems do not support double-sided diskettes, they can not be considered interchangeable media. However, they provide extra storage capacity within a **WINC-05** system environment, as well as being interchangeable with most other non-DEC RX02 controller vendors.

RX50 5-1/4" Floppy Operation

The **WINC-05/50** supports RX50 media compatible operation. However, this is not software compatible with DEC RX50 controllers. **AED** supplies a modification to the RX02 DY driver to operating the **WINC-05**. Disks generated on the **WINC-05/50** are interchangable with DEC RX50 systems. The patch is available for both RT-11 and RSX-11M Operating Systems. Boot operations are supported on the RX50 diskettes, but because of differences in controller commands, the diskettes can not be booted from DEC controllers without rewriting the boot area on the diskettes.

In addition, the **WINC-05/50** allows usage of the second side for the RX50 disk for additional storage, but at the cost of DEC interchangeability.

A format program is included with the RX50 modification for on line formatting of RX50 diskettes, allowing formatting of single sided diskettes for interchangeability, of formatting double sided diskettes for increases storage capacity.

CHAPTER 5

MAINTENANCE & TROUBLESHOOTING

Preventative maintenance should be performed on a regular basis. This consists primarily of cleaning the drives heads on the floppy disk drive. The procedure for cleaning the Read/Write heads is given on the package of commercially available cleaning kits. Corrective maintenance may be required if the diagnostic malfunctions.

In the event of a malfunction, review the list of possible symptons described in this Chapter and perform the suggested corrective actions. Should a malfunction persist, contact the **AED** Customer Service Department.

Troubleshooting procedures assumes availability of spare parts, tools, and skills necessary to analyze faults on a DEC system. The procedure also assumes the remaining elements of the system are performing to specifications.

If a spare controller board is available, board swapping is the quickest way to isolate the fault to the controller or subsystem.

WINC-05 Floppy Disk Diagnostics

The **AED FLEX-02** diagnostic program is designed to demonstrate the functional operability of the **FLEX-02, WINC-05/5** and **WINC-05/8** RX02 controller. The diagnostic program is a standalone program, residing on the first six tracks (Track #0-5) of the distribution diskette (single or double density). The diagnostic individual tests will use the remaining tracks for test purposes. The diagnostic will test drive #0 and 1, single or double sided diskettes, single or double density, depending on how the diagnostic is configured.

Test Requirements

A. PDP-11 or LSI-11 with console terminal
B. 8K of memory
C. AED WINC-05/5 or WINC-05/8 floppy disk
D. 800011-02 WINC-05/5 Diagnostic diskette
   800048-02 WINC-05/8 Diagnostic diskette

CPU Starting Address (octal)

A. Normal start: 200
B. Restart: 1000

Program Load Procedure

A. Place the diagnostic diskette in drive unit #0 or 1, with the diskette label facing up.

B. Enter bootstrap command:

DY(CR), DY0(CR)	BOOT FROM FLOPPY DRIVE UNIT #0
DY1(CR)	BOOT FROM FLOPPY DRIVE UNIT #1

Operator Interface

All operator input requests must be terminated by a carriage return (CR). If the input is just terminated by a (CR), the input response is treated as "NO" input response. A Control-C (CTRLC) input will cause the diagnostic to perform a restart operation.

Program ID

When the initial program load is completed, the diagnostic will type its ID, program part number, and revision levels.

-01 SINGLE DENSITY
-02 DOUBLE DENSITY

Test Configuration

The current test configuration will be displayed, and the operator prompted for configuration modifications. The default configuration is shown.

```
TEST CONFIGURATION: DRIVE=1 HEAD=SINGLE DENSITY=DOUBLE
CHANGE TEST CONFIGURATION (Y OR N)?
```

If the operator response is (Y) YES, terminated by a (CR), the configuration option change is requested. If the operator response is (N) NO, or just terminated by a (CR), the test configuration is left alone. The following is the configuration option change request:

TEST DRIVE 0/1 (Y OR NO):	Y	=	TEST DRIVE
	(CR),N	=	DON'T TEST DRIVE
SINGLE OR DOUBLE SIDED (S OR D)	S	=	SINGLE SIDED
	D	=	DOUBLE SIDED
	(CR)	=	LEAVE PARAMETER UNCHANGED
SINGLE OR DOUBLE DENSITY (S OR D)	S	=	SINGLE DENSITY
	D	=	DOUBLE DENSITY
	(CR)	=	LEAVE PARAMETER UNCHANGED

Operating Procedure

Depending upon how the diagnostic is configured, an initialized diskette should be inserted into drive 0 and/or 1, with the label up.

When the diagnostic is ready to accept command input, the following message is displayed:

ENTER

The following is a list of acceptable input commands:

SYNTAX: X(N),S or X-Y(N),S

X	=	1-6	RUN TEST #1-6 ONLY
	=	A	EXECUTE ALL TESTS
	=	(CR)	EXECUTE ALL TESTS, CONTINUE AFTER ERROR
	=	C	CHANGE TEST CONFIGURATION
	=	T	MODIFY TEST TRACKS (TEST 4-6 ONLY)
	=	W0	WRITE DIAGNOSTIC DRIVE #0
	=	W1	WRITE DIAGNOSTIC DRIVE #1
X - Y	=		EXECUTE TEST (X) THROUGH TEST (Y)
N	=		REPEAT COUNT, DEFAULT=1
S	=		STOP ON ERROR

Examples:

CR	-	Run all test once, continue after error
A,S	-	Run all tests once, stop after error
A(20),S	-	Run all tests 20 times, stop after error
3	-	Run Test #3 once, continue after error
2(10)	-	Run Test #2 10 times, continue after error
1(50),S	-	Run Test #1 50 times, stop after error
1-3(5),S	-	Run Test #1-#3 5 times, stop after error
W0	-	Write diagnostic on drive #0

NOTES:

1. If an error is discovered while typing in a command, the rubout key may be used to delete preceeding character.
2. If the program detected an error in the command string, the following error message is typed: INVALID CMD
3. Test(s) may be aborted by striking 'any' console key.
4. A Control-C (CTRLC) will cause the diagnostic to be restarted.

Description of Tests

TEST 1 - STATUS TEST

This test will primarily test basic operation of the floppy disk controller commands (except set density), and verify the posting of RXCSR and RXESR register status.

ERROR		
1	-	Controller reset comand error Initial RXCSR/ESR register status error.
2	-	Fill buffer command error RXCSR - tranfer ready (TR) RXESR - drive ready (DRY), unit select (UN)
3	-	Interrupt received when interrupt disabled, No interrupt when interrupt enabled
4	-	No interrupt on program interrupt, IE=1 GO=0
5	-	Fill buffer command error RXCSR - density (DEN) RXESR - density (DEN)
6	-	Fill buffer command error RXCSR - error (ERR) RXESR - word count overflow (OVF) Error code - 230
7	-	Empty buffer command error RXCSR - density (DEN) RXESR - denisty (DEN)
8	-	Data compare error
9	-	Empty buffer command error RXCSR - error (ERR) RXESR - word count overflow (OVF) Error code - 230
10	-	Ready drive status command error RXCSR - side selected (SID) RXESR - side selected (SID), side ready (SRY)
11	-	Read sector command error RXCSR - error (ERR) RXESR - density error (DNE) Error code - 240
12	-	Write sector command error RXCSR - error (ERR) RXESR - density error (DNE) Error code - 240
13	-	Fill buffer/write sector error
14	-	Read sector/empty buffer error
15	-	Data compare error
16	-	Read sector command error Error code - 40
17	-	Read sector command error Error code - 70
18	-	Fill buffer command error RXCSR - error (ERR) RXESR - non-existent memory (NXM)

19	-	Empty buffer command error RXCSR - error (ERR) RXESR - non-existent memory (NXM)
20	-	Write sector (deleted data mark) error RXESR - deleted data sector (DEL)
21	-	Write/read sector command RXESR - deleted data sector (DEL)

TEST 2 - RECORD SIZE

This test will verify the ability of the floppy disk controller to perform a variety of data transfers; data verification with selected data patterns, data transfer with varying word counts, and data transfers to all possible memory locations (28K maximum).

ERROR		
1	-	Fill buffer command error
2	-	Empty buffer command error
3	-	Data compare error (selected data)
4	-	Fill buffer command error
5	-	Empty buffer command error
6	-	Data compare error (varying word count)
7	-	Post fill zero's error
8	-	Fill buffer/write sector command error
9	-	Read sector/empty buffer command error
10	-	Data compare error (selected data)
11	-	Interrupt received on priority level (4,5,6,7)
12	-	Fill buffer command error
13	-	No interrupt on priority level 3
14	-	Fill buffer command error
15	-	Empty buffer command error
16	-	Data compare error (memory block)

TEST 3 - SEEK TEST

This test will read sector #0 from tracks #8-76 with a sawtooth pattern, then write/read track #8, sectors #1-26.

ERROR		
1	-	Read sector error
2	-	Write/sector error

TEST 4 - DATA RELIABILITY TEST

This test will write, read, and compare each sector (1-26) from track #10-76. A track table contains test track address. Use command function (T) to modify the track address. (DEFAULT: 10, 11, 12, 43, 44, 45, 74, 75, 76). Random data is used except for track 76 (worst case).

ERROR		
1	-	Read sector/empty buffer error
2	-	Data compare error
3	-	Incorrect track, head, sector address
4	-	Fill buffer/write sector error

TEST 5 - READY VERIFY

This is used to test drive interchangeability, read back, and compares all sectors previously written by Test 4.

ERROR		
1	-	Read sector/empty buffer eror
2	-	Data compare error
3	-	Incorrect track, head, sector address

TEST 6 - READ VERIFY TRACK 76 (WORST CASE)

This test will read track 76 and sectors 1-26 five times for worst case data read checks. Track 76 must have been written by Test 4.

ERROR		
1	-	Read sector/empty buffer error
2	-	Data compare error
3	-	Incorrect track, head, sector address

General Purpose

ERROR		
100	-	CONTROLLER RESET ERROR

Error Reporting and Recovery

Whenever an error occurs, the following general error messages are displayed:

```
TST=n ERR=n ERROR DESCRIPTION
UN=n RXCMD=xx RXCSR=xx RXESR=xx SEC=n. HD=n. TRK=n.
ERCD=xx WC=xx CTRK0=n. CTRK1=n. TTRK=n. TSEC=n. MSTS=x
BTRK=n.

TST=n ERR=n ERROR DESCRIPTION SEC=n. HD=n. TRK=n.
UN=n RXCMD=xx RXCSR=xx EXP=xx RXESR=xx EXP=xx
```

TST	=	TEST NUMBER
ERR	=	ERROR NUMBER
UN	=	UNIT NUMBER
RXCMD	=	COMMAND ISSUED
RXCSR	=	RXCSR REGISTER STATUS (COMMAND COMPLETION)
RXESR	=	RXESR REGISTER STATUS (COMMAND COMPLETION)
EXP	=	EXPECTED STATUS
SEC	=	SECTOR ADDRESS
HD	=	HEAD ADDRESS
TRK	=	TRACK ADDRESS

Full error status:

```
ERCD      =    ERROR CODE
WC        =    WORD COUNT
CTRK0     =    CURRENT TRACK, UNIT #0
CTRK1     =    CURRENT TRACK, UNIT #1
TTRK      =    TARGET TRACK, LAST ACCESS
TSEC      =    TARGET SECTOR
MSTS      =    MISCELLANEOUS STATUS BITS
BTRK      =    TRACK ADDRESS (ERROR CODE 150)
```

Generating a New Diagnostic Diskette

Proceed through the following steps to generate a new diskette.

1. Follow IPL procedure
2. Insert an initialized diskette in drive #0 or #1
3. Input command: W0 WRITE DIAGNOSTIC ON DRIVE #0
   W1 WRITE DIAGNOSTIC ON DRIVE #1

A new diskette will be generated and the diagnostic restarted. Repeat step 3 for additional diskettes.

Changing the Controller Address

To change the diagnostic's controller address, change location 400 and 402 in memory.

```
400 = 177150 (address)
402 =    270 (vector)
```

Winchester Diagnostics

The **AED WINC-05/8** diagnostic program is designed to demonstrate the functional operability of the WINC-05/8 disk controller. This stand-alone program resides on the first six tracks (#0-5) of the distribution diskette (single or double density). The diagnostic will test either RL01 or RL02 drive #0-#3.

Test Requirements

A. PDP-11 or LSI-11 with console terminal
B. 8K memory
C. AED WINC-05/5 or WINC-05/8 Winchester disk controller
D. XXXXXX-02 WINC-05/5 Diagnostic Diskette or
   800074-02 WINC-05/8 Diagnostic Diskette

CPU Starting Address

A. Normal Start: 200
B. Restart: 1000

Program Load Procedure

A. Place diagnostic diskette in Drive Unit #0, label up.
B. Enter bootstrap command. DY(CR), DY0(CR) or (CR)

Operator Interface

All operator inputs requests must be terminated by a carriage return (CR). If only a (CR) is entered, the input response is treated at a "NO" input response. A Control-C (CTRLC) input will cause the diagnostic to perform a restart operation.

Program ID

When the initial program load (IPL) is completed, the diagnostic will type its ID, program part number and revision level.

Test Configuration

The current test configuration will be displayed, and the operator prompted for configuration modifications. The default configuration is shown.

```
TEST WINC05 AT ADDRESS = 175000
DRIVE(S) TO BE TESTED:  (DRIVE)
CHANGE TEST CONFIGURATION (Y OR NO)?
```

If the response is (Y CR), YES carriage return, the configuration option change is requested. If the response is (N) NO, or (CR), the test configuration is ignored. The following is the configuration option change request.

REQUEST			RESPONSE
TEST DRIVE0 (Y OR N):	Y	=	TEST DRIVE0
	(CR), NO	=	DO NOT TEST DRIVE0
TEST DRIVE1 (Y OR N):	Y	=	TEST DRIVE1
	(CR), NO	=	DO NOT TEST DRIVE1
TEST DRIVE2 (Y OR N):	Y	=	TEST DRIVE2
	(CR), NO	=	DO NOT TEST DRIVE2
TEST DRIVE3 (Y OR N):	Y	=	TEST DRIVE3
	(CR), NO	=	DO NOT TEST DRIVE3
TEST WINC05 OR WINC08:	5	=	WINC-05
(5 OR 8)	8	=	WINC-08
NORMAL ADDRESS (174400) OR			
ALTERNATE ADDRESS (175000)	N	=	NORMAL ADDRESS
ENTER (N OR A)	A	=	ALTERNATE ADDRESS

Operating Procedure

Depending upon how the diagnostic is prepared to accept command input, the following message is displayed:

```
ENTER:
```

The following is a list of acceptable commands:

```
SYNTAX:   X(N), S or X-Y(N), S

X     = 1 - 7   Run Test #1-7 only
      = A       Execute all tests
      = (CR)    Execute all tests, continue after error
      = C       Change test configuration
      = T       Modify test tracks (Test 4-6 only)
      = F       Format drive (WINC-05 only)
      = W0      Write diagnostic into floppy drive #0
      = W1      Write diagnostic into floppy drive #1

X - Y =         Execute test (X) through test (Y)
    N =         Repeat count, default=1
    S =         Stop on error
```

Examples:

```
CR          -   Run all tests once, continue after error
A,S         -   Run all tests once, stop after error
A(20),S     -   Run all tests 20 times, stop after error
3           -   Run test #3 once, continue after error
2(10)       -   Run test #2 ten times, continue after error
1(50),S     -   Run test #1-#3 five times, stop after error
W0          -   Write diagnostic on floppy Drive #0
```

NOTES:

1. If an error is discovered while typing a command, the rubout key may be used to delete preceding characters.
2. If the program detected an error in the command string, the following error message is typed: INVALID INPUT
3. Test(s) can be aborted by striking 'any' console key.
4. A Control C (CTRLC) will restart the diagnostic.

The following list are acceptable commands to be used if a stop error is selected.

1. R - Retry
2. C - Continue
3. A - Abort test
4. L - Continue retry, report error
5. N - Continue retry, do not report error
6. D - Debug
7. ? - Help

If the format drive command is selected, the following questions will be asked.

1. Format which drive? Enter (N or 0-3)
2. Enter interleave number (2 or 3)
3. Enter format data pattern up to six digits
4. Are you sure you want to format driveX? Enter (Y or N)

NOTE: Format command is valid for WINC-05 controller only.

Description of Tests

TEST 1 - STATUS TEST

This test is designed primarily to test the basic operation of the WINC-05/8 commands, and verify the posting of RLCSR status.

ERROR

2 - interrupt time out
3 - controller ready time out
4 - read drive status command error
5 - read header command error
6 - seek command error
7 - write sector command error
8 - read sector command error
9 - write sector command error during write check operation
10 - write check command error
11 - read data without header check command error
12 - non exist memory test error
13 - word count overflow test error

TEST 2 - RECORD SIZE & INTERRUPT PRIORITY TEST

This test will verify the WINC-05/8 Read/Write operation with various word counts, and test the interrupt occurance under various CPU interrupt priorities.

ERROR

14 - write command error during record size test
15 - read command eror during record size test
16 - compare error during record size test, data under run
17 - compare error during record size test, data over run
18 - interrupt priority test error

TEST 3 - SEEK TEST

This test will seek to various tracks with a sawtooth pattern.

ERROR

19 - read drive status error during seek test
20 - read sector error during seek test
21 - write/read data error

TEST 4 - DATA RELIABILITY TEST

This test will write, read and compare each sector (0-39) from various tracks. A track table contains test track address. Use command function (T) to modify the track address. Random data is used except for the most inner track. (Track 255 for RL01 drive and track 511 for RL02 drive).

ERROR

22 - write command error, fix data pattern
23 - read command error, fix data pattern
24 - compare error, fix data pattern
25 - read drive status error
26 - write command error, random data
27 - read command error, random data
28 - compare error, random data
29 - compare error, header

TEST 5 - READ VERIFY

This test is used to test drive data reliability. It reads and compares all sectors previously written by Test 4.

ERROR

27 - read command error, random data
28 - compare error, random data
29 - compare error, header
30 - read drive status error

TEST 6 - READ VERIFY THE MOST INNER TRACK

Track 255 for RL01 drive, track 511 for RL02 drive.

ERROR

27 - read command error, random data
28 - compare error, special data pattern
29 - compare error, header
30 - read drive status error

TEST 7 - WRITE/READ ALL TRACKS AND ALL SECTORS

This test writes, reads and compares data on each sector and track of the drive.

ERROR		
26	-	write command error, random data
27	-	read command error, random data
28	-	compare error, random data
29	-	compare error, header
30	-	read drive status error

Error Reporting and Recovery

Whenever an error occurs, the following general error messages are displayed.

```
TST=n ERR=n ERROR DESCRIPTION
UN=n RLCMD=xxxxxx RLSCR=xxxxxx EXP=xxxxxx RLDSR=xxxxxx
THD=x TTRK=xxx TSEC=xx EA=xx BA=xxxxxx WC=xxx CHD=x
CTRK=xxx
TST=n ERR=n ERROR DESCRIPTION
UN=n RLCMD=xxxxxx RLCSR=xxxxxx EXP=xxxxxx RLDSR=xxxxxx
EXCEPTED: SEC=xx HD=x TRK=xxx RECEIVED SEC=xxHD=x
TRK=xxx OS=xxx DAT EXP=xxxxxx DATA REC=xxxxxx
```

TEST	=	TEST NUMBER
ERR	=	ERROR NUMBER
UN	=	UNIT NUMBER
RLCMD	=	COMMAND ISSUED
RLCSR	=	STATUS RECEIVED
EXP	=	EXPECTED STATUS
RLDSR	=	DRIVE STATUS
THD	=	TARGET HEAD
TTRK	=	TARGET TRACK ADDRESS
TSEC	=	TARGET SECTOR ADDRESS
CHD	=	CURRENT HEAD
CTRK	=	CURRENT TRACK ADDRESS
OS	=	BUFFER ADDRESS OFFSET
EA	=	BUS ADDRESS EXTENTION
BA	=	BUS ADDRESS
WC	=	WORD COUNT

NOTE: If the controller interrupt times out while reading RLDSR, the diagnostic program puts 177777 in the error report.

Generating a New Diagnostic Diskette

A new program diskette can be generated by executing the following steps.

1. Follow IPL procedure.
2. Insert an initialized diskette in floppy drive #0 (#1)
3. Input command: "W0" ("W1") write diagnostic on floppy drive #0 (#1)

A new diskette will be generated and the diagnostic restarted. Repeat Step 3 for additional diskettes.

DEC DIAGNOSTICS

The **WINC-05** is designed to use DEC-supplied diagnostics to demonstrate the performance and subsystem troubleshooting ability of the **WINC-05** disk system for customer acceptance. Refer to the DEC User's Guide for operating instructions.

RL/RX CONTROLLER TEST

- *CZRLGB0 RL controller test 1
- CZRLHB0 RL controller test 2
- *CZRLIC0 RL drive test 1
- CZRXCA0 RX utility driver
- CZRXFA1 RX function-logic test

RL/RX SYSTEM EXERCISER

- CZRLKB1 RL performance exerciser
- CZRXDB0 RX performance exerciser

RL/RX UTILITY PROGRAMS

- CZRLLB0 RL drive compatiblity
- CZRLMB0 RL bad sector file tool
- CZRXEA2 RX format program

NON-SUPPORTED PROGRAMS

- CZRLJB1 RL drive test 2
- CZRLNA0 RL drive test 3
- CZRXAE0 RX RX01 system reliability test
- CZRXBF0 RX RX01 interface test

*Program change requirements.

RX02 Dual-Head, 8-Inch Floppy Testing

For the dual-head floppy subsystem supplies with the **WINC** subsystem, a provision must be made for the second head. When running the DEC diagnostics (for example, ZRXDB0), the second head is tested as a separate unit from the first head. Testing a two-headed floppy is not explained in the DEC User's Guide.

Program Change Requirements

Due to the architectural differences between the WINC-05 and the RX02, RL01/RL02 disk subsystems, some of the low-level diagnostic subtests which are used to fault isolate a problem are not directly emulated. Below is a list of these diagnostic programs and their subtests requiring program modification for proper operation. Use the Update Program (UPD2) to change the memory locations.

CZRLGB0 Controller Test 1

Memory Location	Change From	To	Subtest	Reason
20644:	1404	404	Test 32	Read header-2nd/3rd (0,CRC) words not emulated.
23776:	1404	404	Test 43	Read header-2nd/3rd (0,CRC) words not emulated.

CZRLIC0 Drive Test 1

Memory Location	Change From	To	Subtest	Reason
36462:	1406	406	Test 14	Read header-2nd/3rd (0,CRC) words not emulated.

TABLE 5-1

Dual-Head Floppy Disk Diagnostics

Display	Enter	Comments
DS-B	Start	Start test
UNITS?	2	2 heads on 1 drive
UN1 ADRS	CR	Use default address
Vector	CR	Use default vector
Drive	0 CR	Drive 0
Expansion	0 CR	Head 0
UN2 ADRS	CR	Use default address
Vector	CR	Use default vector
Drive	0 CR	Drive 0
Expansion	1 CR	Head 1
Change Switch?	Y CR	Yes
Help?	Y CR	If desired
Exercise	3 CR	Or other; 3=write/read/compare
Data Pattern	0 CR	Or other; 0=random data
Track Sequence?	1 CR	Or other; 1=ascending order

Double Density?	Y CR	Double density
Deleted data?	CR	Default
Flags?	CR	
Track Limits	CR	Track 00-76
Sector Limits	CR	Specify limits
MIN	1 CR	Sectors 1 to 26; enter sector
MAX	26 CR	Min=1, max=1 to speed up test
Future Expansion?	Y CT	Must be answered "Y" if any unit select expansion questions were answered "1"

(Diagnostic will begin running)

Replaceable Parts

The following lists outline the list of spare parts available by part number, from **AED.**

WINC-05/5 & 5/8 SUB ASSEMBLY SPARES

PART NUMBER	DESCRIPTION
OEM Parts	
120179-XX	CONTROLLER CARD ASSEMBLY (5/8)
890063-XX	CONFIGURATION PROM (specify drive configuration)(5/8)
990016-01	WINC-05/8 MANUAL
800048-02	DIAGNOSTIC DISKETTE, 8" (5/8)
551022-100	8" DBLE-SIDED, DBLE DEN DISKETTES-10 ea.(5/8)
120119-01	WINC-05 CONTROLLER CARD (5/5)
890063-XX	CONFIGURATION PROM (specify configuration)
800111-02	DIAGNOSTIC DISKETTE, 5 1/4" (5/5)
551023-100	5 1/4" DISKETTES-10 ea. (5/5)
1020170-02	DRIVE CABLING BOARD (5/8)
Drive Subsystem - Common Parts	
580220-000	POWER CORD
580110-002	3 AMP FUSE
590100-000	RUBBER FEET (4/SET)
590602-000	CHASSIS SLIDES
180036-XX	DOCUMENTATION PACKAGE (includes manual, schematics)
Drive Subsystem - 8" Floppy System	
554712-900	5 1/4" WINCHESTER DRIVE, 10 MB (5/8)
525511-900	8" SLIM LINE FLOPPY DRIVE (5/8)
160096-01	POWER SUPPLY ASSEMBLY (includes back panel) (5/8)
150043-11	10' I/O CABLE, 50 PIN (5/8)

150098-01	DC HARNESS CABLE ASSEMBLY (5/8)
150097-01	FLOPPY DRIVE CABLE ASSEMBLY, 50 PIN (5/8)
150055-02	WINCHESTER DRIVE CABLE ASSEMBLY, 20 PIN (5/8)
150053-03	WINCHESTER DRIVE CABLE ASSEMBLY, 34 (5/8)
140231-01	TOP COVER (5/8)
140230-01	RACKMOUNT CHASSIS (5/8)
140204-01	FALSE PANEL, 8" SLIMLINE DRIVES (5/8)
140202-01	DRIVE SUPPORT BRACKET,8" SLIMLINE DRIVES (5/8)
140201-01	FALSE PANEL BRACKET (5/8)
140200-01	DRIVE COUPLER, 8" SLIMLINE DRIVE (5/8)

Drive Subsystem - 5-1/4" Floppy System

120113-01	DRIVE CABLING BOARD (5/5)
554712-900	5 1/4" WINCHESTER DRIVE, 10 MB (5/5)
552411-900	5 1/4" FLOPPY DRIVE (5/5)
160064-01	POWER SUPPLY ASSEMBLY, (incl.rear panel) (5/5)
160047-02	FAN ASSEMBLY (5/5)
150055-01	FLAT CABLE ASSEMBLY, 20 PIN (5/5)
150054-01	DC CABLE HARNESS ASSEMBLY (5/5)
150053-02	FLAT CABLE ASSEMBLY,34 PIN(14"with fold) (5/5)
150053-01	FLAT CABLE ASSEMBLY,34 PIN(9" with fold) (5/5)
150043-11	50 PIN I/O CABLE ASSEMBLY, 10' (5/5)
140142-01	RACKMOUNT CHASSIS (5/5)
140141-01	TOP COVER (5/5)
140114-01	FRONT PANEL (5/5)
140112-01	DRIVE SUPPORT BRACKET (5/5)
180025-XX	DOCUMENTATION PACKAGE (includes manual, schematics)

CONTROLLER REPLACEABLE SPARES LIST

120179-xx WINC-05/8, WINC-05/5, WINC-05/50

Loc.	Part Numbers			Function
	5/8 RX01/02	5/5 AED Format	5/50 RX50	
A25	890071-01			Z8000 main program
A30	890071-02			Z8000 main program
A34	890063-xx			Drive Config. Prom
A37	890073-01	890085-01	890085-01	Floppy phase counter
A38	890074-01	890083-01	890086-01	Serial control
A39	890075-01	890084-01	890084-01	Ser. encode/decode
A45	890064-01			Function logic unit
A46	890076-01			Function addr. decode
A47	890077-01			Instruction prom
A60	890068-01			Addr.seq. (for IP)
A57	890067-01			QBUS Addr. decoder
A50	890050-01			interrupt ack decode
A74	890080-01			DMA grant sequencer
A51	890051-01			Z8K addr.decode/rdy

120119-xx WINC-05

5-1/4" AED FLOPPY FORMAT

Location	P/N
A25	890062-01 H
A30	890062-02 H
A34	890063-xx E
A37	890044-01 A
A38	890045-01 A
A39	890046-01 A
A45	890094-01 A
same as	890064-01 A
A46	890065-01 A
A47	890066-01 A
A60	890093-01 A
same as	890068-01 A
A57	890067-01 A
A50	890050-01 C
A74	890054-01 A
A51	890051-01 A

WINC-05 Floppy Conversion 120179-xx

Installation Instructions:

1. To convert from 5" AED or RX50 floppy operation to 8" RX02 operation:

   Remove A37, A38, A39 (save for reverse conversion)

   Install prom 890073-01 in A37, 890074-01 in A38, and 890075-01 in A39.

   Replace A34 with the appropriate configuration prom.

2. To convert from 8" RX02 floppy operation to 5-1/4" AED RX02 operation:

   Remove A37, A38, A39 (save for reverse conversion)

   Install prom 890085-01 in A37, 890083-01 in A38, and 890084-01 in A39.

   Replace A34 with the appropriate configuration prom.

   To convert from 5-1/4" RX50 floppy operation to 5-1/4" AED RX02 operation:

   Remove A38 (save for reverse conversion)

NOTE: Proms at Location A25, A30 (890071-01,02) must be Revision K or later.

3. To convert from 8" RX02 floppy operation to 5-1/4" RX50 operation:

Remove A37, A38, A39 (save for reverse conversion)

Install prom 890085-01 in A37, 890086-01 in A38, and 890084-01 in A39.

Replace A34 with the appropriate configuration prom.

To convert from 5-1/4" AED floppy operation to 5-1/4" RX50 operation:

Remove A38 (save for reverse conversion)

Install prom 890086-01 in A38.

NOTE: Proms at locations A25 and A30 (890071-01,02) must be at Revision L or later.

CHAPTER 6

PROGRAMMER'S GUIDE

General

A description of the registers and commands used for emulation and maintenance mode is included in this section. For quick reference, a bit layout of the information provided is noted at the top of the particular table.

RL01 PIO Addressing

			Alternate
774400	CSR	Command/status register	(775000)
774402	BAR	Bus address register	(775002)
774404	DAR	Disk address register	(775004)
774406	MPR	Multipurpose register	(775006)
774410	BAE	Bus address extension register	(775010)
774412	---	Undefined	(775012)
160	Interrupt vector		(120)

CSR Bit Definition

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
write	0	0	0	0	0	0	DS1	DS0	0	INE	MAD	MAD	FUN	FUN	FUN	0
read	ERR	DRE	NXM	DLT	CRC	OPI	DS1	DS0	RDY	INE	MAD	MAD	FUN	FUN	FUN	DRY

ERR: Any controller error
DRE: Drive error - selected drive
NXM: Non-existant memory eror
DLT: Data late - header or data field not found
CRC: CRC error - header or data
OPI=0 & CRC=1 & RD CMD -- data CRC error
OPI=1 & CRC=1 & RD CMD -- header CRC error
OPI=0 & CRC=1 & WR CHK -- write check error
OPI: Operation incomplete in 200 ms -- header not found
DS: Drive select (DS1, DS0 selects 1 of 4 drives)
RDY: Controller ready
(GO: Command GO bit equals .NOT.RDY [i.e. write RDY=0])
INE: Interrupt enable
MAD: Extended bus address bit 17, 16
FUN: Controller function select

CODE	FUNCTION
000	no op
001	write check
010	get status
011	seek
100	read header
101	write data
110	read data
111	read data -- without header check

DRY: Drive ready (heads loaded, not seeking)

Bus Address Register

This is a 16 bit read/write bus address (BA) register. BA expansion bits 16 and 17 are contained in CSR bits 4 and 5. The contents of this 16 bit BA register plus the CSR expansion bits indicate the address of the CPU memory to be used for data transfers. The complete 18 bit address is updated at the completion of each sector. The BA is cleared with a BUS INIT, or by loading with all zeros. For 22 bit addressing, the BA extension register is found at location 774410 and contains address bit 16 through 21 in register bits 0 through 5.

```
15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
BA15 ----------------------------------------------------BA00
```

BA15-BA00: Bus Address

Disk Address Register

This read/write register is used for three different functions. These functions are comprised of:

A) DA register during a SEEK command
B) DA register during a READ/WRITE or WRITECHECK command
C) DA register during a GET STATUS command

The register is cleared by a BUS INIT or by loading with all zeros.

Seek Commands

```
15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
DF8 DF7 DF6 DF5 DF4 DF3 DF2 DF1 DF0 0   0   HED 0   DIR 0   1
```

```
DF8-DF0:    Cylinder difference
HED:        Head select
DIR:        Seek direction (DIR=1: increasing cylinder number)
```

READ/WRITE Commands

```
15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
CA8 CA7 CA6 CA5 CA4 CA3 CA2 CA1 CA0 HED SA5 SA4 SA3 SA2 SA1 SA0
```

```
CA8-CA0:    Cylinder address
HED:        Head select
SA5-SA0:    Sector address
```

Get Status Command

```
15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
0   0   0   0   0   0   0   0   0   0   0   0   RST 0   GS  1
```

```
RST:        Reset drive error registers
GS:         Get status request
```

Multipurpose Register

Get Status Command

```
15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
WDE CHE WL  SKT SPE WGE VC  DSE DT  HED CO  HO  BH  ST2 ST1 ST0
```

WDR: Write data error (no write current detected)
CHE: Write current in head without write gate asserted
WL: Drive write protect on
SKT: Seek timeout
SPE: Spin error (drive did not spinup)
WGE: Write gate error
VC: Volume check (after new head load)
DSE: Drive select error (multiple drive selections)
DT: Drive type (0=RL01, 1=RL02)
HED: Currently selected head
CO: Drive cover open
HO: Head over disk (heads loaded)
BH: Head over home area (heads loaded)
ST: Drive state

CODE	STATE
000	cartridge unloaded
001	drive spinning up
010	heads loading
011	drive seeking
100	drive seeking
101	lock on (spun up)
110	heads unloading
111	drive spinning down

Read Header Command

```
    15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
(1) CA8 CA7 CA6 CA5 A4  CA3 CA2 CA1 CA0 HED SA5 SA4 SA3 SA2 SA1 SA0
(2) 0   0   0   0   0   0   0   0   0   0   0   0   0   0   0   0
(3) CRC15 ---------------------------------------------- CRC00
```

After a read header command, the MPR acts as a 3 word FIFO. If the program reads this register 3 times in succession, the above 3 words are obtained. NOTE: The **WINC-05** does not support reading more than one word. If the programs reads the second and third word, the first word will be repeated.

READ/WRITE Commands

```
15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
1   1   1   WC12 ------------------------------------- WC00
```

WC12-WC00: Transfer word count (2's compliment)

BUS Address Extension Register

```
15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
0   0   0   0   0   0   0   0   0   0   BA21 ---------- BA16
```

This register is accessible only if the controller has 22 bit addressing enabled. Note that the CSR address bits BA17, BA16 override the BA17 and BA16 bits in this register.

Command Sequences

READ Data/WRITE Data

```
WRITE---CYL:HEAD:SECTOR----INTO DAR
WRITE---BA-----------------INTO BAR & BAE
WRITE---WC(2'S COMP)-------INTO MPR
WRITE---DRIVE:MAD:FUN------INTO CSR
```

The controller transfers data from/to the disk into/from the memory buffer. The transfer starts at the specified cylinder, head and sector, and continues until the word count is incremented to zero. Note that the command will not transfer data from more than a single cylinder and head, thus the maximum transfer is limited to 5120 (decimal) words.

Write Check

```
WRITE---CYL:HEAD:SECTOR-----INTO DAR
WRITE---BA-------------------INTO BAR & BAE
WRITE---WC(2'S COMP)---------INTO MPR
WRITE---DRIVE:MAD:FUN:-------INTO CSR
```

The controller compares data from the disk (starting at the specified cylinder, head and sector) with the data in the memory buffer. It continues the comparison until the word count is incremented to zero. Note that the command will not operate off cylinder or head boundaries.

Seek

```
WRITE---CYLDIFF:HEAD:DIR----INTO DAR
WRITE---DRIVE:FUN-----------INTO CSR
```

The controller initiates a seek to the specified cylinder on the specified drive. Note that all seeks must be explicitly commanded with a seek command. The cylinder difference is output, not the absolute cylinder address.

Read Header

```
WRITE---DRIVE:FUN-----------INTO CSR
@Interrupt:
READ----MPR (contains current CYL:HEAD:SECTOR)
```

The controller reads the next header. This command is used to locate the current track under the heads.

Get Drive Status

```
WRITE---GS----------------INTO DAR
WRITE---DRIVE:FUN---------INTO CSR
@Interrupt:
READ----CSR (contains error information)
READ----MPR (contains drive status)
```

Read Data Without Header Check

```
WRITE---BA----------------INTO BAR
WRITE---WC(2'S COMP)------INTO MPR
WRITE---DRIVE:MAD:FUN-----INTO CSR
```

This is a diagnostic command to allow data recovery when a sector's header contains a hard error.

Special Function Formation Logical Unit

```
WRITE---000364------------INTO DAR    (set maintenance mode)
WRITE---000004------------INTO CSR    (get status)
Wait for interrupt/controller ready  (error is posted)
WRITE---XXXXXX------------INTO DAR    (XXX=0: interleave of 2)
                                     (XXX=1: interleave of 3)
WRITE---YYYYYY------------INTO MPR    (YYY=format data pattern)
WRITE---000016------------INTO CSR    (read header)
                                     (000016=unit 0,000416=unit 1
                                      001016=unit 2,001416=unit 3)
Wait for interrupt/controller ready  (maintenance mode is reset)
                                     (error means format failed)
```

Volume Check Flag

At power on, the Winchester drives set cartridge change. The controller sets the drive volume check flag. It must be cleared before any drive accesses can take place. To clear, issue a get status command with the RESET bit set in the DAR.

WINC-05 Floppy Interface

PIO Addressing (Standard Assignment)

```
                                          Alternate
    777170....CSR----Command-status register  (777150)
    777172....ESR----Extended status register (777152)
    777172....DBR----Data buffer register     (777152)

       264....Interrupt vector                  (270)
```

CSR Bit Definition

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ERR	INT	MAD	MAD	1	RX5	SID	DEN	TR	INE	RDY	UN	FUN	FUN	FUN	GO
R	W	W	W	R	R/W	R/W	R/W	R	R/W	R	R/W	R/W	R/W	R/W	W

ERR: Any controller error
INT: Controller reset
MAD: Extended bus address bits 17,16
RX5: RX50 format slect (0=RX01/02, 1=RX50)
SID: Side select
DEN: Density select (0=single, 1=double)
TR: DBR transfer request
RDY: Controller ready
UN: Unit select
FUN: Controller function select

CODE	FUNCTION
000	fill buffer
001	empty buffer
010	write sector
011	read sector
100	set density
101	read drive status
110	write sector (deleted data mark)
111	read full error status

GO: Command initiate flag

NOTE: For RX50 formatted disks, the RX5 bit is set and the DEN bit is reset in the command word.

DBR Definition

The DBR is defined in the various command sequences.

WARNING: Read or write to the DBR only in the correct sequence. Failure to do so will result in an undefined failure to occur within the function in progress.

In general, the user must never write into the DBR, except when the RT bit is set in the CSR during a command sequence. The user may read from the DBR only when the controller is ready (RDY bit is set in the CSR).

ESR Bit Definitions

```
15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
0   0   RX5 5ER NXM OVF SID UN  DRY DEL DEN DNE ALO INT SRY CRC
```

RX5: RX50 format (actual)
5ER: RX50 format error (0=RX50 cmd and disk or RX02 cmd and disk) (1=RX50 cmd and RX02 disk or RX02 cmd and RX50 disk).
NXM: Non-existant memory
OVF: Word count overflow
SID: Side selected (actual)
UN: Unit selected (actual)
DRY: Drive ready (selected drive)
DEL: Deleted data sector read
DEN: Density (actual) (0=single, 1=double)
DNE: Density error
ALO: Drive cabinet AC low
INT: Controller reset done
SRY: Side 2 ready
CRC: CRC error

The ESR can be read from the DBR at the completion of any command. It may also be read in the DBR by executing a read drive status command.

Command Sequences

The following command sequences are described for operation under program control.

When manually executing commands using the console ODT, the CSR is written first, then the first and second DBR words are written. Reading the DBR does not reset the TR flag (after microcode 890071, Revision E).

Fill/Empty Buffer Functions

```
WRITE:  MAD:DEN:FUN:GO=1---INTO CSR (TYP:401/403 octal)
   or:  MAD:RX50:FUN:GO=1---INTO CSR (TYP:2001/2003 octal)
@TR=1:
WRITE:  WORD COUNT---------INTO DBR (0-200 octal/0-400 octal)
@TR=1:
WRITE:  BUS ADDRESS--------INTO DBR
```

The controller fills/empties its internal buffer from/into the CPU's memory. A fill operation will post fill the buffer with zeros should the word count be less than the max word count.

READ/WRITE/WRITE(Deleted Data) Functions

```
WRITE:  SID:DEN:UN:FUN:GO=1--INTO CSR (TYP:407/405 octal)
   or:  SID:RX50:UN:FUN:GO=1-INTO CSR (TYP:2007/2005 octal)
@TR=1:
```

```
WRITE:  SECTOR #-------------INTO DBR (1-32 octal/1-12 octal)
@TR=1:
WRITE:  TRACK #--------------INTO DBR (0-114 octal/1-120 octal)
```

The selected read/write operation to/from the disk drive is performed into/from the controller's internal buffer.

Read Drive Status

```
WRITE:  SID:UN:FUN:GO=1------INTO CSR (TYP: 013 octal)
```

Drive ready (disk inserted), disk density, and number heads are tested for the selected unit. Status is returned in the ESR.

Warning: Requires 250ms for command completion.

Set Media Density

```
WRITE:  DEN:UN:FUN:GO=1------INTO CSR (TYP: 411/011 octal)
   or:  RX50:SID:UN:FUN:GO=1--INTO CST (TYP: 2011/3011 octal)
@TR=1:
WRITE:  Keyword-------------INTO DBR (TYP: 0111 octal ['I'ascii])
```

This command will write all sectors of all tracks of all heads in the selected density. The data written are all zeros. The command will rewrite the header information.

Warning: Requires 15 sec (30 sec if two sided) for command completion. If a command is aborted before completion, an erroneous disk will remain.

Read Full Error Status

```
WRITE:  FUN:GO=1-------------INTO CSR (TYP: 017 octal)
@TR=1:
WRITE:  BUS ADDRESS----------INTO DBR
```

The controller empties the internal status registers into the CPU memory.

The CPU memory format is:

```
BA+0:<15:8> WORD COUNT.............<7:0> ERROR CODE
BA+2:<15:8> CURRENT TRACK, UN1.....<7:0> CURRENT TRACK, UN0
BA+4:<15:8> TARGET SECTOR..........<7:0> TARGET TRACK,LAST ACCESS
BA+6:<15:8> MISC STATUS BITS.......<7:0> MISC STATUS BITS
```

MISC STATUS BITS:

```
BIT 7:  Unit selected
BIT 6:  Drive Density, UN1
BIT 5:  Head load flag
BIT 4:  Drive density: UN0
BIT 3:  0
BIT 2:  0
BIT 1:  0
BIT 0:  Density (read error reg command)
```

ERROR CODES:

000	----	--
010	SEEK	Home not found (UN0) after INIT
020	SEEK	Home not found (UN1) after INIT
030	----	--
040	SYST	Access attempt to track .GT.76
050	SEEK	Home found before target track found
060	----	--
070	R/W	Target sector not found before 52 sectors past (or target sector=0, or > max sector number)
100	SYST	Write attempt on a write protected disk
110	R/W	No disk transition found on 40us (data mark found, but read fault during sector)
(120)	R/W	No preamble found (WINC-05: 130)
130	R/W	Preamble found but no head ID mark found
140	R/W	CRC error on what appears to be the header
150	SEEK	Track address not equal to target track
(160)	R/W	Too many tries for an IDAM (WINC-05: 170)
170	R/W	Data mark not found for target sector
200	CRCE	CRC data error found
210*	DENS	RX50 error (not RX50 format)
220	DIAG	R/W electronics failure
230	SYST	Word count overflow
240	DENS	Density error
250	SYST	Wrong keyword for set density command
260*	R/W	Side does not equal taget side
270*	SYST	Attempt to access side 2 of 1 sided disk

ERROR CLASSES:

SYST	Programming error
DIAG	Controller self diagnostic error
SEEK	Drive seeking error
R/W	Drive read/write error
DENS	Disk density/format discrepancy
*	AED Extention to the DEC RX02 Error Codes

CONTROLLER RESET

Either: WRITE: INT=1----------INTO CSR (at any time)

or: execute the CPU RESET instruction
or: perform an external system reset
or: turn the drive cabinet AC power on (after CPU power on)

Upon receipt of any of the following reset functions, the controller will perform the stated functions.

A) Reset the controller (except for drive cabinet power on). All error bits are cleared, ready is reset, interrupt enable is reset

B) Execute a self diagnostic program (returning status in the CSR, ESR, and via the read full error status command, wherever possible, or necessary).
C) Return both drives to the home position.
D) Read unit 0, track 0, head 0, sector 0 into the controllers internal buffer.
E) Terminate the function by asserting READY in the CSR, and initialize done in the ESR.

Drive AC Power Off

Whenever the drive AC power is off, the controller will assert the AC LOW flag in the ESR in response to any command. It will also assert a controller error status bit in the CSR in response to any drive oriented command. See the paragraph above for operation with a new power on condition.

Bootstrap Command Interface

Bootstrap Functions

The **WINC-05** controller provides the capability of bootstrapping from itself. This bootstrap is a host program, residing at the starting address of 173000 (octal), to allow use of the standard CPU power up jump function. The bootstrap program uses the CPU console device for control which must be at address 177560.

Bootstrap Commands

The bootstrap functions load head 0, track 0 and sector 1 of the selected unit (unit 0 if not unit specified) of the selected device into CPU memory starting at memory location 0. It loads the unit number into the CPU's register 0 and transfers control to the CPU at location 0.

This program will automatically bootstrap load from the controller unit 0 if the operator does not type another function within 1.5 minutes after the program begins execution. This provides automatic reloading at unattended sites after power failure.

```
DY<CR>; DY0<CR>, DY1<CR>:    BOOT FROM FLEX, UNIT 0,1
DL<CR>; DL)<CR>--DL3<CR>:    BOOT FROM WINC, UNIT 0--3
```

FORMATTING THE DRIVE

The **WINC-05** will format the drives from the console at boot up time. The commands are:

Winchester

```
XI2<CR>; XI3<CR>:                 Select drive interleave (2 or 3)
XU<CR>; XU0<CR>--XU3<CR>:         Select unit (0-3)
Format DL---ARE YOU SURE? Y<CR>   Format it
```

Floppy

```
XD1<CR>; XD2<CR>; XD5<CR>:      Select density (RX01-single,
                                RX02-double or RX50)
XU<CR>; XU0<CR>; XU1<CR>:       Select unit  (0 or 1)
Format DY---ARE YOU SURE? Y<CR> Format it
```

For RX50 format, the bootstrap program will ask how many sides the disk has.

System Test Function

This facility is enabled by a bit coded into the configuration PROM. The system test command is TE<CR>. This function will perform tests on the LSI-11 processor, DLV11J, memory, a Winchester drive read test (all configured Winchesters), and an AED graphics (parallel interface DMA and PIO cycles) test. Failures are reported to the console terminal.

A typical console printout of the diagnostic is:

```
AED>    TE<return>

Testing serial ports.......Passed No Loop
Testing Winchesters........Passed
Testing CPU................Passed 11/23 MMU FPU
Testing memory.............Passed 512KB

AED>
```

The program will print out that a particular test is beginning prior to execution. Should the system fail during the test, the operator will note which function failed.

Processor Tests

Most instructions affecting the PSW flags are exercised, and the conditional branch instruction is used to test the flags. In addition, the processor type is tested (11/2, 11/23, 11/73), and the MMU and FPU are tested for existence.

Memory Tests

Data is written/read and compared, incrementing until a nonexistant location is encountered, or until the last location of the 4 Mby address space occurs. An error is displayed if any location does not compare. The memory is then cleared to zeros.

Serial I/O Tests

This test determines if all IO registers can be accessed for each port of the DLV11J quad serial board. It then attempts to loop back ports 0-2 (non-console). If no characters are received on the loop back test, the test is skipped. If characters are received, they are compared with the sent data (an error is displayed if bad).

Winchester Disk Tests

For all drives configured, the drive is selected, rezeroed (error if fail), and RL cylinder 0--head 0--sectors - through 40 are read (error if read fails). Further error classification is posted in the RL IO registers.

Graphics DMA Tests

During this routine, it is first determined whether the IO registers respond. If they do not, the diagnostic terminates testing, assuming the interface is none existent. If the interface exists, commands are issued to reset the terminal, determine the terminal type, and set up for DMA transfers. It then will execute a write raster direct and read raster direct, comparing the data read and the data being trnsfered into the terminal screen buffer is bad. Should no command response occur, or if data is bad, an error is posted. The buffer is then cleared to color zero.

Bootstrap Inhibit Option

A jumper option is provided to disable the bootstrap function, allowing another bootstrap ROM to be located at address 173000.

Auto-Bootstrap Option

An additional jumper option is provided to automatically bootstrap from the **WINC-05** drive 0 at power up, with no delay, and without requiring a console device to be present at address 177560. If this option is enabled, as soon as the LSI-11 performs the power up jump to 173000, the **WINC-05** tries to bootstrap from drive 0. If drive 0 is not ready, the controller will keep trying until th drive has spun up and is ready, or, until the LSI-11 is manually halted.

The unit which the **WINC-05** will boot from is stored in the configuration PROM. Either the DL or DY device can be selected, and any unit number. DL0 is the default.

APPENDIX A

CONFIGURATION PROM DATA

AED encourages users to customize configuration PROMS for their specific needs. This document is provided to assist in this customization.

The configuration prom contains drive constants. For each logical drive, the following data is stored:

```
Drive identifier          (0,1,0 = RL01
    hexidecimal            0,1,8 = RL02
    3 nibbles              9,9,0 = RX02 - 5/14"
                           B,8,0 = RX02 - 8"
                           0,0,0,= nonexistant drive

Mapped, or Unmapped       (unmapped for floppy)
   Starting unit number if mapped
Starting head number      (zero if unmapped)
Number of physical heads per logical drive
Number of physical cylinders (to 4,095)
Cylinder for "low current" and precompensation switch
Seek step interval        (multiple of 2.2us - 9ms)
Seek pulse width          (multiple of 2.2us - 35us)
Drive spin up time        (multiple of 1.0ms - 64 sec)
Head load/Motor on delay for floppy
                          (multiple of 1.0ms - 4 sec)
```

In addition, the configuration PROM contains the following controller related data.

Interrupt request level (level 4 or 5) for the RL and RX
Main and Alternate interrupt vectors for the RL and RX
Default boot Device and Unit number
Special boot prompt message (other than AED>), allowing up to 6 characters plus a space after the message.

PROM Format

An actual configuration PROM listing is included. The following comments will assist you in the interpretation of this listing.

The addresses in the left column must be divided by two when using a PROM programmer to examine or alter a PROM. This step is necessary because the assembler used to generate the listing allocates two addresses per word, where the programmer uses only one address per location. The PROM itself is only 4 bits wide, therefore, parameters requiring more than 4 bits will be distributed into 4 bit nibbles, and stored in sequencial addresses, with the most significant nibble at the lower of the addresses used.

AED WINC-#5 Configuration Prom Installation

Locate the configuration prom on the controller. With either a prom extractor or small flat head screwdriver, gently remove the standard prom. Insert the new configuration prom, taking note to secure it in the correct position as indicated on the illustration below.

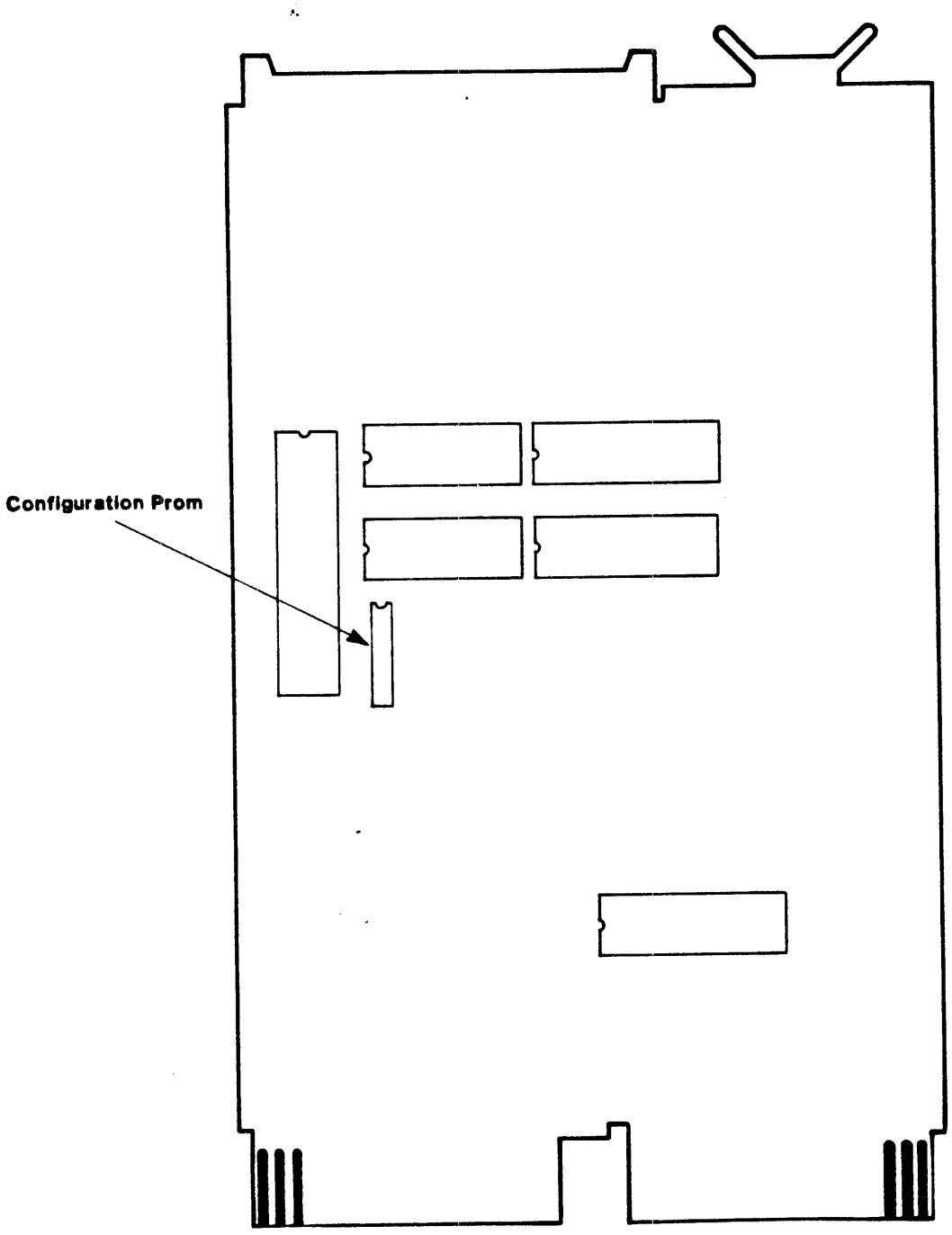


FIGURE A.1
Prom Installation

The assembler syntax used is:

WVAL - allocates a word of storage
LAND - logical and operator
SHR - logical shift right N bits
%(8), %(10),% - number radix specifier (octal, decimal, hexidecimal).

PROM Specifications

AED utilizes a 256 x 4 PROM equivalent to Signetics 82S129. Any PROM with an address access time less than 200 ns, a chip select access time less than 200 ns, and input and output currents less than the 82S129 may be used.

AED WINC-05/8 EXAMPLE CONFIGURATION PROM

Winchester:

Drive 0: AMP 27/RODIME 204 - 20MB
Drive 1: Mapped 2 10MB's
Drive 2: AMP 27/RODIME 204 - 20MB
Drive 3: Mapped 2 10MB's

Floppy:

Drive 0: Qume 242 - 8"
Drive 1: Qume 242 - 8"

SUBTTL CONFIGURATION PROM DATA

CONFIGURATION PROM DATA

```
      =0010           RADIX     16
                !SET DEFAULT CONSTANT BASE = HEX
                !CPROM definitions
                !
 =0010                  RADIX     16     !set hex radix
                !
                !DRTYPE definitions
                !
=8000           IL        EQU       08000 !interleave (not stored in
                !                             !cPROM)
                !
=4000           IHBHD     EQU       04000 !inhibit floppy head compare
                !                       =0 verify correct head
                !                       =1 inhibit, for Sigma RX02
                !                       compatability
                !
=2000           SZ8       EQU       02000 !floppy size
                !                       =0 for 5" fpy, =1 for 8" fpy
=1000           FPID      EQU       01000 !enable floppy = 1
                !
=0800           RX02      EQU       00800 !RXTYPE
                !                       =1 RX02, =0 not used
                !
=0400           CPLX      EQU       00400 !E !enable complex mapping
                !                       =0 for unmapped or stepper drives
                !                       =1 for voice coil drives
                !
                !         EQU       00200 !       unused
                !
 =0100          WCID      EQU       00100 !enable winc
                !
 =0080          RL02      EQU       00080 !RLTYPE,
 =0000          RL01      EQU       00000 !RLTYPE,
                !                       =0 for RL01, =1 for RL02
                !
 =0040          FREZ      EQU       00040 !K !fast rezero mode
                !                       =0 for 3 ms, =1 for buffered rate
                !
 =0020          DSLSL     EQU       00020 !L !for DMA360 cartridge
                !                       desel then hd switch then select
                !                       flag and skip trk 0 test
                !
                !         EQU       00010 !       unused
                !         EQU       00008 !       unused
                !
 =0006          WCMPUF    EQU       00006 !mapped drive number
                !                       =00 for vendor drive 0,
                !                       =01 for vendor drive 1,
                !                       not used if unmapped.
                !
```

```
=0001       WCMP        EQU         00001 !enable mapping of WINC
                        !                 =0 for 1 RL per vendor drive
                        !                 =1 for 2-4 RL's per vendor drive
                        !
                        ! Control Mode Definitions
                        !
=0008       GTRME       EQU         00008 !enable graphics console
                        !   bit 3         =0 for ascii console terminal
                        !                 =1 for AED graphic console terminal
                        !
                        !   EQU         00004 !       unused
                        !   bit 2         =1 must be a one.
                        !
=0006       TESTE       EQU         00006 !enable system testing
                        !   bit 1         =0 for no TE boot test command
                        !                 =1 for TE boot test command
                        !
                        !   EQU         00001 !       unused
                        !   bit 0         = unassigned

=0181       DRTYPE      EQU         WCID+RL02+(VNDRIV*2)+WCMP
                        ! Winchester RL02, mapped 2 RL's

=0000       CPROM       EQU         0
=0000       SHIFT       EQU         0
=0006       CTRL        EQU         TESTE !default control mode

=00000000   CPROM       EQU         %0
=00000000   SHIFT       EQU         %0
=00000005   INTLEV      EQU         5
=000000B4   RXMVEC      EQU         %(8)264
=000000B8   RXAVEC      EQU         %(8)270
=00000070   RLMVEC      EQU         %(8)160
=00000050   RLAVEC      EQU         %(8)120
=00000044   BTDV1       EQU         'D'
=0000004C   BTDV2       EQU         'L'
=00000000   BTUNI       EQU         0
=00000000   BTMSG1      EQU         0
=00000000   BTMSG2      EQU         0
=00000000   BTMSG3      EQU         0
=00000000   BTMSG4      EQU         0
=00000000   BTMSG5      EQU         0
=00000000   BTMSG6      EQU         0

=00000000               ORG         CPROM               !CONTROLLER
0000                PRMCTL:
                    !RL- interrupt request level = (5)
0000    000A            WVAL    ( INTLEV SHL 1)
                    !RX- interrupt request level = (5)
0001    000A            WVAL    ( INTLEV SHL 1)
                    !RL- main vector address = (160)
0002    0000            WVAL    ((RLMVEC LAND 0F00) SHR 8)
0003    0007            WVAL    ((RLMVEC LAND 00F0) SHR 4)
0004    0000            WVAL    ((RLMVEC LAND 000F) SHR 0)
```

```
                        !RX- main vector address = (264)
0005    0000                WVAL    ((RXMVEC LAND 0F00) SHR 8)
0006    000B                WVAL    ((RXMVEC LAND 00F0) SHR 4)
0007    0004                WVAL    ((RXMVEC LAND 000F) SHR 0)
                        !RL- alternate vector address = (120)
0008    0000                WVAL    ((RLAVEC LAND 0F00) SHR 8)
0009    0005                WVAL    ((RLAVEC LAND 00F0) SHR 4)
000A    0000                WVAL    ((RLAVEC LAND 000F) SHR 0)
                        !RX- alternate vector address = (270)
000B    0000                WVAL    ((RXAVEC LAND 0F00) SHR 8)
000C    000B                WVAL    ((RXAVEC LAND 00F0) SHR 4)
000D    0008                WVAL    ((RXAVEC LAND 000F) SHR 0)
                                    Control Mode
000E    0004                WVAL    (CTRL)
                        !Default boot device = (DL0)
000F    0004                WVAL    ((BTDV1 LAND 00F0) SHR 4)
0010    0004                WVAL    ((BTDV1 LAND 000F) SHR 0)
0011    0004                WVAL    ((BTDV2 LAND 00F0) SHR 4)
0012    000C                WVAL    ((BTDV2 LAND 000F) SHR 0)
0013    0000                WVAL    (BTUNI) SHL SHIFT !DEFAULT BOOT
                                    UNIT=0
                        !Special Boot prompt String
0014    0000                WVAL    ((BTMSG1 LAND 00F0) SHR 4)
0015    0000                WVAL    ((BTMSG1 LAND 000F) SHR 0)
0016    0000                WVAL    ((BTMSG2 LAND 00F0) SHR 4)
0017    0000                WVAL    ((BTMSG2 LAND 000F) SHR 0)
0018    0000                WVAL    ((BTMSG3 LAND 00F0) SHR 4)
0019    0000                WVAL    ((BTMSG3 LAND 000F) SHR 0)
001A    0000                WVAL    ((BTMSG4 LAND 00F0) SHR 4)
001B    0000                WVAL    ((BTMSG4 LAND 000F) SHR 0)
001C    0000                WVAL    ((BTMSG5 LAND 00F0) SHR 4)
001D    0000                WVAL    ((BTMSG5 LAND 000F) SHR 0)
001E    0000                WVAL    ((BTMSG6 LAND 00F0) SHR 4)
001F    0000                WVAL    ((BTMSG6 LAND 000F) SHR 0)

        =00000040       ORG         (CPROM+RMBLK)   !WINC DRIVE #0
        =00000000   UNIT            EQU     0           !INIT UNIT COUNTER
0040                    PRMRL0:
                        !for example
```

```
                    =000A                RADIX 10 !set decimal radix      !
                                !  Ampex P27 / Rodime R0204 - 20 Mby

                                     First Physical Drive - DL0
                                !
          =00000000 BSUNT       EQU       UNIT!Base unit(mapped drive)
                                !                  ! zero if unmapped
          =00000000 BSHED       EQU       0      !Starting head
          =00000004 MXHED       EQU       4      !Heads per logical drive
                                !
                                ! First logical drive
                                ! Winchester RL02, mapped 2 RL's per drive
          =0181     DRTYPE      EQU       WCID+RL02+(BSUNT*2)+WCMP
0040      0000          $10:              WVAL      0       !DRIVE ID
0042      0001                            WVAL      1       ! WINCHESTER DRIVE
0044      0008                            WVAL      8       ! RL02 TYPE
0046      0001                            WVAL      (BSUNT * 2) + 1
                                !Drive physical cylinders
0048      0001                            WVAL      ((320 LAND %0F00) SHR 08)
004A      0004                            WVAL      ((320 LAND %00F0) SHR 04)
004C      0000                            WVAL      ((320 LAND %000F) SHR 00)
                                !MAP DRIVE- starting head number (0 if unmapped)
004E      0000                            WVAL      BSHED
                                !Drive physical heads per logical drive
0050      0004                            WVAL      MXHED
                                !DRIVE LOW CURRENT/PRE-COMP CYL
0052      0000                            WVAL      ((132 LAND %0F00) SHR 08)
0054      0008                            WVAL      ((132 LAND %00F0) SHR 04)
0056      0004                            WVAL      ((132 LAND %000F) SHR 00)
                                !Seek step interval time = 24.2us
                                ! T = (( N * 2.2us ) + 4.4us + Tpw )
                                ! N = ((( T - Tpw ) - 4.4us ) / 2.2us )
```

```
0058  0000          WVAL  (((((242 - 66) - 44) / 22) LAND %0F00) SHR 8)
005A  0000          WVAL  (((((242 - 66) - 44) / 22) LAND %00F0) SHR 4)
005C  0006          WVAL  (((((242 - 66) - 44) / 22) LAND %000F) SHR 0)
                          !Seek step pulse= 6.6us
                          ! Tpw = (( N * 2.2us ) + 2.2us )
                          ! N   = (( Tpw - 2.2us) / 2.2us)
005E  0002          WVAL ((66 - 22 ) / 22) LAND %000F
                          !Drive spin up time = 20sec
                          ! T = ( N * 1.0ms )
0060  0004                    WVAL   ((20000 LAND %0F000) SHR 12)
0062  000E                    WVAL   ((20000 LAND  %0F00) SHR 8)
0064  0002                    WVAL   ((20000 LAND  %00F0) SHR 4)
0066  0000                    WVAL   ((20000 LAND  %000F) SHR 0)
            =00000078         ORG    ($10+CPBLK)              !2ND DRIVE
            =00000001 UNIT    EQU    UNIT+1
            =00000004 BSHEDEQU       BSHED+MXHED
                          !
                          ! Second logical drive - DL1
                          ! Winchester RL02, mapped 2 RL's per drive
      =0181      DRTYPE    EQU      WCID+RL02+(BSUNT*2)+WCMP
0078  0000       $20:            WVAL   0      !DRIVE ID
007A  0001                    WVAL   1      ! WINCHESTER DRIVE
007C  0008                    WVAL   8      ! RL02 TYPE
007E  0001                    WVAL   (BSUNT * 2) + 1
                          !Drive physical cylinders
0080  0001                    WVAL   ((320 LAND %0F00) SHR 08)
0082  0004                    WVAL   ((320 LAND %00F0) SHR 04)
0084  0000                    WVAL   ((320 LAND %000F) SHR 00)
                          !MAP DRIVE- starting head number (0 if unmapped)
0086  0004                    WVAL   BSHED
                          !Drive physical heads per logical drive
0088  0004                    WVAL   MXHED
                          !DRIVE LOW CURRENT/PRE-COMP CYL
008A  0000                    WVAL   ((132 LAND %0F00) SHR 08)
008C  0008                    WVAL   ((132 LAND %00F0) SHR 04)
008E  0004                    WVAL   ((132 LAND %000F) SHR 00)
                          !Seek step interval time = 24.2us
                          ! T = (( N * 2.2us ) + 4.4us + Tpw )
                          ! N = ((( T - Tpw ) - 4.4us ) / 2.2us )
0090  0000            WVAL  (((((242 - 66) - 44) / 22) LAND %0F00) SHR 8)
0092  0000            WVAL  (((((242 - 66) - 44) / 22) LAND %00F0) SHR 4)
0094  0006            WVAL  (((((242 - 66) - 44) / 22) LAND %000F) SHR 0)
                          !Seek step pulse= 6.6us
                          ! Tpw = (( N * 2.2us ) + 2.2us )
                          ! N   = (( Tpw - 2.2us) / 2.2us)
```

```
0096   0002          WVAL ((66 - 22 ) / 22) LAND %000F
                          !Drive spin up time = 20sec
                          ! T = ( N * 1.0ms )
0098   0004          WVAL ((20000 LAND %0F000) SHR 12)
009A   000E          WVAL ((20000 LAND  %0F00) SHR 8)
009C   0002          WVAL ((20000 LAND  %00F0) SHR 4)
009E   0000          WVAL ((20000 LAND  %000F) SHR 0)

               =00000002 UNIT EQU    UNIT+1                !INCR UNIT CTR
               =000000B0      ORG    (PRMRL0+(CPBLK*UNIT)) !INC DRIVE #2
00B0              PRMRL2:


               =000A            RADIX  10    !set decimal radix
                          !
                          !  Ampex P27 / Rodime R0204 - 20 Mby
                          !  Second Physical Drive - DL3
                          !
               =00000002 BSUNT   EQU UNIT !Base unit(mapped drive)
                          !                ! zero if unmapped
               =00000000 BSHED   EQU 0    !Starting head
               =00000004 MXHED   EQU 4    !Heads per logical drive
                          !
                          ! First logical drive
                          ! Winchester RL02, mapped 2 RL's per drive
          =0181      DRTYPE   EQU WCID+RL02+(BSUNT*2)+WCMP
00B0   0000          $10: WVAL 0  !DRIVE ID
00B2   0001               WVAL 1  ! WINCHESTER DRIVE
00B4   0008               WVAL 8  ! RL02 TYPE
00B6   0005               WVAL (BSUNT * 2) + 1
                     !Drive physical cylinders
00B8   0001               WVAL ((320 LAND %0F00) SHR 08)
00BA   0004               WVAL ((320 LAND %00F0) SHR 04)
00BC   0000               WVAL ((320 LAND %000F) SHR 00)
                     !MAP DRIVE- starting head number (0 if unmapped)
00BE   0000               WVAL BSHED
                     !Drive physical heads per logical drive
00C0   0004               WVAL MXHED
                     !DRIVE LOW CURRENT/PRE-COMP CYL
00C2   0000               WVAL ((132 LAND %0F00) SHR 08)
00C4   0008               WVAL ((132 LAND %00F0) SHR 04)
00C6   0004               WVAL ((132 LAND %000F) SHR 00)
                     !Seek step interval time = 24.2us
                     ! T = (( N * 2.2us ) + 4.4us + Tpw )
                     ! N = ((( T - Tpw ) - 4.4us ) / 2.2us )
00C8   0000               WVAL  (((((242 - 66) - 44) / 22) LAND %0F00) SHR 8)
00CA   0000               WVAL  (((((242 - 66) - 44) / 22) LAND %00F0) SHR 4)
00CC   0006               WVAL  (((((242 - 66) - 44) / 22) LAND %000F) SHR 0)
                     !Seek step pulse= 6.6us
                     ! Tpw = (( N * 2.2us ) + 2.2us )
                     ! N   = (( Tpw - 2.2us) / 2.2us)
00CE   0002               WVAL     ((66 - 22 ) / 22) LAND %000F
                     !Drive spin up time = 20sec
                     ! T = ( N * 1.0ms )
```

```
00D0    0004          WVAL      ((20000 LAND %0F000) SHR 12)
00D2    000E          WVAL      ((20000 LAND  %0F00) SHR 8)
00D4    0002          WVAL      ((20000 LAND  %00F0) SHR 4)
00D6    0000          WVAL      ((20000 LAND  %000F) SHR 0)

        =000000E8    ORG  ($10+CPBLK) !2ND DRIVE
        =00000003 UNIT   EQU  UNIT+1
        =00000004 BSHEDEQU    BSHED+MXHED
                  !
                  ! Second logical drive - DL4
                  ! Winchester RL02, mapped 2 RL's per drive
        =0181       DRTYPE   EQU WCID+RL02+(BSUNT*2)+WCMP
00E8    0000    $20:   WVAL   0  !DRIVE ID
00EA    0001           WVAL   1  ! WINCHESTER DRIVE
00EC    0008           WVAL   8  ! RL02 TYPE
00EE    0005           WVAL   (BSUNT * 2) + 1
                  !Drive physical cylinders
00F0    0001           WVAL   ((320 LAND %0F00) SHR 08)
00F2    0004           WVAL   ((320 LAND %00F0) SHR 04)
00F4    0000           WVAL   ((320 LAND %000F) SHR 00)
                  !MAP DRIVE- starting head number (0 if unmapped)
00F6    0004             WVAL BSHED
                  !Drive physical heads per logical drive
00F8    0004             WVAL MXHED
                  !DRIVE LOW CURRENT/PRE-COMP CYL
00FA    0000             WVAL ((132 LAND %0F00) SHR 08)
00FC    0008             WVAL ((132 LAND %00F0) SHR 04)
00FE    0004             WVAL ((132 LAND %000F) SHR 00)
                  !Seek step interval time = 24.2us
                  ! T = (( N * 2.2us ) + 4.4us + Tpw )
                  ! N = ((( T - Tpw ) - 4.4us ) / 2.2us
0100    0000        WVAL  (((((242 - 66) - 44) / 22) LAND %0F00) SHR 8)
0102    0000        WVAL  (((((242 - 66) - 44) / 22) LAND %00F0) SHR 4)
0104    0006        WVAL  (((((242 - 66) - 44) / 22) LAND %000F) SHR 0)
                  !Seek step pulse= 6.6us
                  ! Tpw = (( N * 2.2us ) + 2.2us )
                  ! N   = (( Tpw - 2.2us) / 2.2us)
0106    0002        WVAL ((66 - 22 ) / 22) LAND %000F
                  !Drive spin up time = 20sec
                  ! T = ( N * 1.0ms )
0108    0004        WVAL ((20000 LAND %0F000) SHR 12)
010A    000E        WVAL ((20000 LAND  %0F00) SHR 8)
010C    0002        WVAL ((20000 LAND  %00F0) SHR 4)
010E    0000        WVAL ((20000 LAND  %000F) SHR 0)

        =00000004 UNIT   EQU  UNIT+1        !INCR UNIT CTR
        =00000120        ORG  (PRMRL0+(CPBLK*UNIT)) !FLOPPY DRIVE #0
                  PRMRX0:
```

```
        =000A           RADIX   10  !default decimal radix
                        !
                        !  QUME 242- 8" DRIVE
                        !Drive ID= 8" drive, RX02 type - DY0
        =B800           DRTYPE.EQU   FPID+RX02+SZ8+IL
0120    000B                WVAL %0B
0122    0008                WVAL %8
0124    0000                WVAL %0
0126    0000                WVAL %0
                        !Drive physical cylinders
0128    0000                WVAL ((077 LAND %0F00) SHR 8)
012A    0004                WVAL ((077 LAND %00F0) SHR 4)
012C    000D                WVAL ((077 LAND %000F) SHR 0)
                        !Map drive- base head
012E    0000                WVAL 0
                        !Drive physical heads
0130    0002                WVAL 2
                        !Drive low current/pre-comp cyl
0132    0000                WVAL ((044 LAND %0F00) SHR 8)
0134    0002                WVAL ((044 LAND %00F0) SHR 4)
0136    000C                WVAL ((044 LAND %000F) SHR 0)
                        !Seek step interval time = 3 MS
                        ! T = (( N * 2.2us ) + 4.4us + Tpw )
0138    0005                WVAL ((((30000 - 110 - 22 ) / 22) LAND %0F00) SHR 8)
013A    0004                WVAL ((((30000 - 110 - 22 ) / 22) LAND %00F0) SHR 4)
013C    000D                WVAL ((((30000 - 110 - 22 ) / 22) LAND %000F) SHR 0)
                        !Seek step pulse= 11us
                        ! Tpw = (( N * 2.2us ) + 2.2us )
013E    0004                WVAL     ((110 - 22 ) / 22) LAND %000F
                        !Head load time = 50ms
                        ! T = ( N * 1.0ms )
0140    0000                WVAL     ((50 LAND %0F00) SHR 8)
0142    0003                WVAL     ((50 LAND %00F0) SHR 4)
0144    0002                WVAL     ((50 LAND %000F) SHR 0)
                        !Head unload time = 2sec
                        ! T = ( N * 1.0ms )
0146    0007                WVAL     ((2000 LAND %0F00) SHR 8)
0148    000D                WVAL     ((2000 LAND %00F0) SHR 4)
014A    0000                WVAL     ((2000 LAND %000F) SHR 0)

        =00000158       ORG  (PRMRX0+CPBLK)    !FLOPPY DRIVE #1
0158                PRMRX1:
```

```
          =000A      RADIX     10              !default decimal radix
                     !
                     !  QUME 242- 8" DRIVE
                     !Drive ID= 8" drive, RX02 type - DY1
          =B800      DRTYPE.EQU   FPID+RX02+SZ8+IL
0158      000B         WVAL %0B
015A      0008         WVAL %8
015C      0000         WVAL %0
                     !Mapped drive flag (=0 for floppy)
015E      0000         WVAL %0
                     !Drive physical cylinders
0160      0000         WVAL ((077 LAND %0F00) SHR 8)
0162      0004         WVAL ((077 LAND %00F0) SHR 4)
0164      000D         WVAL ((077 LAND %000F) SHR 0)
                     !Map drive- base head
0166      0000         WVAL      0
                     !Drive physical heads
0168      0002         WVAL 2
                     !Drive low current/pre-comp cyl
016A      0000         WVAL ((044 LAND %0F00) SHR 8)
016C      0002         WVAL ((044 LAND %00F0) SHR 4)
016E      000C         WVAL ((044 LAND %000F) SHR 0)
                     !Seek step interval time = 3 MS
                     ! T = (( N * 2.2us ) + 4.4us + Tpw )
0170      0005         WVAL ((((30000 - 110 - 22 ) / 22) LAND %0F00) SHR 8)
0172      0004         WVAL ((((30000 - 110 - 22 ) / 22) LAND %00F0) SHR 4)
0174      000D         WVAL ((((30000 - 110 - 22 ) / 22) LAND %000F) SHR 0)
                     !Seek step pulse= 11us
                     ! Tpw = (( N * 2.2us ) + 2.2us )
0176      0004         WVAL ((110 - 22 ) / 22) LAND %000F
                     !Head load time = 50ms
                     ! T = ( N * 1.0ms )
0178      0000         WVAL ((50 LAND %0F00) SHR 8)
017A      0003         WVAL ((50 LAND %00F0) SHR 4)
017C      0002         WVAL ((50 LAND %000F) SHR 0)
                     !Head unload time = 2sec
                     ! T = ( N * 1.0ms )
017E      0007         WVAL ((2000 LAND %0F00) SHR 8)
0180      000D         WVAL ((2000 LAND %00F0) SHR 4)
0182      0000         WVAL ((2000 LAND %000F) SHR 0)

          =00000200    ORG  (CPROM+%(10)512)  !SET END OF PROM AREA

                               END
```

No errors detected

APPENDIX B

DRIVE VENDOR STATUS REPORT

The following information outlines the various Winchester and floppy disk drives that have been verified for operation with the WIMC-05/5 and WIMC-05/8 disk controller. Configuration PROMs exist for each of these manufacturers.

Floppy Disk Drives

There are four classes of floppy drives which AED supports in a a variety of configurations.

5 1/4" Equivalent to Qume 592, i.e., a 3 ms step rate, and 1 second motor on time.

Such drives include:

Qume 592, Tandon TM100-4, YE-Data YD-280 Mitsubishi M4853.

5 1/4" Equivalent to Shugart SA460/SA350, i.e., a 6 msstep rate, and a 1 second motor on time.

8" Equivalent to Qume 242/ Shugart SA850, i.e., a 3 ms step rate, an independent head load control (50 ms head load delay), with the motor continuously spinning.

Such drives include:

Qume DT8 & 242, Shugart 850 (but NOT the SA800 due to the 8 ms step rate), YE Data YD-174 and YD-180, MPI 42, and Mitsubishi M2894-63 & M2896-63.

8" Equivalent to Shugart SA860/Tandon 848, i.e., a 3 ms step rate, and a motor on control (1 sec motor on delay) located on the "head load" pin. This also supports the 5 1/4" drives offering 8" capacity, and can also be used for the Qume 242 type described above (but with a longer head load delay).

Such drives include:

Tandon TM848-x, Shugart SA860 (8"), as well as YE Data YD-380, Mitsubishi M4854, and TEAC FD55G (5 1/4").

The Winchester drives that are supported by AED as a class are:

ST412 306 cylinders, with 2, 4, 6, or 8 heads. Either an RL01 on 2 heads, or an RL02 on 4 heads. Buffered step rate of 25 us. Write precompensation on cylinders above 128.

640 640 cylinders, with 2, 4, 6, or 8 heads, an RL02 on 2 heads. Buffered step rate of 25 us, write precompensation on all cylinders.

Larger voice coil drives will be supported upon demand.

NOTE: On 15-Sept-84, the dash numbers for the 20 Mby--306 cylinder drives was changed to include the operation of the Seagate ST425 drive, as well as other drives. The previous dash numbers are not compatible with the Seagate drive.

Configuration Prom Part Numbers Cross Reference

5 1/4" Flpy Config. #	Prom 890063 -xx	Old Prom Dash #
5P001	-01	
5P002	-45	(-02)
5P003	-04	
5P004	-15	
5P005	-46	(-10)
5P006	-16	
(5P007)	-06	(use 5P002)
(5P008)	-05	(use 5P009)
5P009	-39	(-09)
5P010	-40	(-19)
5P011	-07	
5P012	-17	
5P013	-08	
5P014	-34	
5P015	-35	
5P016	-44	
5P017	-55	
5P018	-73	

8" Flpy Config. #	Prom 890063 -xx	Old Prom Dash #
8P001	-14	
8P002	-13	
8P003	-11	
8P004	-18	
8P005	-37	(-12)
8P006	-38	(-20)
8P007	non-existant	
8P008	-21	
8P009	-42	(-23)
8P010	-24	
8P011	-25	
8P012	-26	
8P013	-27	
8P014	-41	(-28)
8P015	-29	
8P016	-30	
8P017	-31	
8P018	-32	
8P019	-33	
8P020	-36	
8P021	-43	
8P022	-47	
8P023	-48	
8P024	-49	
8P025	-50	
8P026	-51	
8P027	-52	
8P028	-53	
8P029	-54	
8P030	-56	
8P031	-57	
8P032	-58	
8P033	-59	
8P034	-60	
8P035	-66	
8P036	-62	
8P037	-63	

Configuration Prom Part Numbers Cross Reference

5 1/4" Flpy Config. #	Prom 890063 -xx	Old Prom Dash #	8" Flpy Config. #	Prom 890063 -xx	Old Prom Dash #
			8P038	-64	
			8P039	-65	
			8P040	-67	
			8P041	-68	
			8P042	-69	
			8P043	-70	
			8P044	-71	
			8P045	-72	

Seagate Standard Equivalents - 5, 10, 15, 20 Mby Drives

ST412 like, 306 cylinders	5 Mby 2 hd	10 Mby 4 hd	15 Mby 6 hd	20 Mby 8 hd	CPROM ok?	Notes
	-----	-----	-----	-----	--	---------
Standard Config. Proms	1 RL01	1 RL02	1 RL02 1 RL01	2 RL02		
1 drive	--	5P002	5P006	5P009		5 1/4" floppy
	--	--	--	--		5 1/4" (Shugart)
	--	8P003	--	8P005		8" (Qume equiv)
	--	8P004	8P017	8P009		8" (Tandon equiv)
	--	8P022	--	--		8" (1 sided)
2 drive	--	5P003	--	5P010		5 1/4" floppy
	--	5P014	--	--		5 1/4" (Shugart)
	--	8P002	--	8P006		8" (Qume equiv)
	--	8P008	--	8P014		8" (Tandon equiv)
	--	8P023	--	--		8" (1 sided)
	-----	-----	-----	-----	--	---------
		2 RL01	3 RL01			
1 drive	--	5P005	5P004	--		5 1/4" floppy
	--	--	--	--		5 1/4" (Shugart)
	--	8P001	--	--		8" (Qume equiv)
Vendor Model	--	--	--	--		8" (Tandon equiv)
& tested?	-----	-----	-----	-----	--	---------
Ampex	P7	P12	P19	P27	yes	full high
	no	yes(*)	no	yes		
CMI	5206	5412	5619	--	no,step	timing difference
	no	yes(*)	yes		AED has	some proms avail
Cogito	--	CG912	--	--	yes	1/2 high
		no				
Distron	507	514	519	D526	yes	full high
	no	no	no	no		
Fujitsu	M2231	M2233	M2234	M2235	yes	full high
	no	yes	no	yes		
	?	?	--	--	?	1/2 high
		no	no			
IMI	5006H	5012H	5018H	--	yes	full high
	no	yes(*)	no			
	2306	2312	--	--	?	1/2 high
	no	no				

ST412 like	5 Mby 2 hd	10 Mby 4 hd	15 Mby 6 hd	20 Mby 8 hd	AED CPROM ok?	Notes
Microscience	--	HH612 yes	--	--	yes	1/2 high W05,read problem
Miniscribe	2006 no	2012 no	--	--	?	full high
	3006 no	3012 no	--	--	?	1/2 high
Mitsubishi	M4863-2 no	M4863-3 no	--	--	?	full high
NEC	D5214 no	D5224 no	D5234 no	D5244 no	yes	full high
Rodime	R0201 no	R0202 no	R0203 no	R0204 yes	yes	full high
	R0351 no	R0352 yes(*)	--	--	yes	3.5", 1/2 high
Seagate	ST406 no	ST412 yes	ST419 yes	ST425 yes	yes	full high 425 = new CPROM
	--	ST212 yes(*)	--	--	yes	1/2 high
Shugart	SA607 no	SA612 no	--	--	?	full high
	SA706 no	SA712 no	--	--	yes	1/2 high
Tandon	TM501 no	TM502 yes(*)	TM503 no	--	yes	full high
	TM251 no	TM252 yes(*)	--	--	yes	1/2 high
TEAC	? no	? yes(*)	? no	--	yes	Mfg under Seagate license (avail in Japan only)

NOTES:

yes (*) was tested by a customer, not **AED**.
no has not been tested on **WINC-05**.
CPROM yes is compatible with standard **AED** configuration PROM
no is not
? is not known (spec not received)

612 cylinder standard equivalents - 10, 20, 30, 40 Mby Drives

612 cylinders	10 Mby 2 hd	20 Mby 4 hd	30 Mby 6 hd	40 Mby 8 hd	AED CPROM ok?	Notes
Standard Config Proms Available	1 RL02	2 RL02	3 RL02	4 RL02		
	--	--	--	5P015		5 1/4" floppy
	--	--	--	--		5 1/4" (Shugart)
	--	--	--	--		8" (Qume equiv)
	--	--	8P015	8P016		8" (Tandon equiv)
Vendor Model & tested?						
CMI	CM6213 no	CM6426 no	CM5640 no	---	yes	full hi 640 cyl
Miniscribe	---	---	---	5451 no	?	full hi ? cyl
Rodime	R0201E no	R0202E no	R0203E R0206 no	R0204E R0208 yes(*)	yes	full hi 640 cyl
Tulin	TL213 no	TL226 no	TL240 yes	--	yes	1/2 high 640 cyl

Notes:

yes (*) was tested by a customer, not **AED**.
no has not been tested on **WINC-05**.
CPROM yes is compatible with standard **AED** configuration PROM
NO IS NOT
? is not known (spec not received)

Configurations Available for Higher Capacity Drives

---
2 RL02 + 1 RL01 drives

CDC Wren 9415-36-5 — 36.3Mby unfmt, 5hd, 679cyl, 45ms

8P019 — with 2 x 8" floppies (Tandon equivalent)

---
3 RL02 drives

Quantum — Q540 — 42.6Mby unfmt, 8hd, 512cyl, 49ms, Production 8/84

8P024 — with 2 x 8" floppies (Tandon equivalent)
8P025 — with 2 x 8" single sided floppies (SA800/810)

Syquest — SQ338

8P039 — with 2 x 8" floppies (Tandon equivalent)

---
3 RL02 + 1 RL01 drives

Atasi 3046		46.3Mby unfmt, 7hd, 635cyl, 30ms, production 3/83
	5P018	with 2 x 5-1/4" floppies (Qume equivalent)
	8P020	with 2 x 8" floppies (Tandon equivalent)

---
4 RL02 drives

Fujitsu	M2242AS	55.0Mby unfmt, 7hd, 754cyl, 35ms, production 8/84
Priam	502	55.0Mby unfmt, 7hd, 755cyl, 32ms, production 11/83
Atasi	3051	51.0Mby unfmt, 7hd, 704 cyl
	8P026	with 2 x 8" floppies (Tandon equivalent)
Micropolis 1304		51.9Mby unfmt, 6hd, 830cyl, 30ms, production 9/83
	8P027	with 2 x 8" floppies (Qume/NEC equivilent)

Cartridge Drives - Seagate ST506 Compatible

Available Configuration Proms:

Syquest SQ306F/R 5.1 Mby Formatted (servo before index)
Western Dynex 5.1 Mby Formatted (servo on Track -1)

5P015	DL0: (RL02) Seagate ST412	DY0: (AED RX02) Qume 592
	DL1: (RL01) Syquest SQ306	DY1: (AED RX02) Qume 592
8P021	DL0: (RL02) Seagate ST412	DY0: (RX01/02) Qume type
	DL1: (RL01) Syquest SQ306	DY1: (RX01/02) Qume type
8P033	DL0: (RL02) Seagate ST425	DY0: (RX01/02) Tandon type
	DL1: (RL02) Seagate ST425	DY1: (RX01/02) Tandon type
8P032	DL0: (RL01) Syquest SQ306	DY0: (RX01/02) Tandon type
	DL1: (RL01) Second SQ306	DY1: (RX01/02) Tandon type

Syquest SQ312RD 10.2Mby formatted 612 cyl, servo before index
This drive requires PCB 120179, Microcode Revision K or later.

5P017	DL0: (RL02) Seagate ST425	DY0: (AED RX02) Qume type
	DL1: (RL02) Seagate ST425	DY1: (AED RX02) Qume type
	DL2: (RL02) Syquest SQ312	
8P028	DL0: (RL02) Seagate ST425	DY0: (RX01/02) Tandon type
	DL1: (RL02) Seagate ST425	DY1: (RX01/02) Tandon type
	DL2: (RL02) Syquest SQ312	
8P029	DL0: (RL02) Syquest SQ312	DY0: (RX01/02) Tandon type
	DL1: (RL02) Second SQ312	DY1: (RX01/02) Tandon type

DMA Systems 350 10.2Mby formatted 612 cyl, servo before index
This drive requires PCB 120179, Microcode Revision L or later.

8P031	DL0: (RL02) DMA 360	DY0: (RX01/02) Tandon type
	DL1: (RL02) Second DMA 360	DY1: (RX01/02) Tandon type

The following drives are not compatible with **WINC-05**. They are not Seagate ST506 compatible. These drives are hard sectored, servo between sectors.

DMA Systems	5.1Mby formatted, 33 sectors/track
Memorex (2nd source)	5.2Mby formatted
IOMEGA Beta-5	5.1Mby formatted, 52 sectors/track, floppy
Microstorage MS212	10Mby formatted, 1/2 high, spec not recv'd.

Additional Drives Less Than 20 Mby

The following drives need special configuration PROMS, as they differ in the number of heads & cylinders, or step rate.

CMI 5412 10.4Mby formatted

5P011	one RL02, plus one 5 1/4" floppy
5P013	two RL01, plus one 5 1/4" floppy

CMI 5619 15.6Mby formatted

5P012	three RL01, plus two 5 1/4" floppies
8P018	one RL02, one RL01, plus two 8" Tandon type floppies

Seagate ST506 5.2Mby formatted

8P045	one RL01, plus two 8" Tandon type floppies

Unless otherwise anotated, the following drives do not have configuration proms available.

Vendor	Model	
CDC	9270-6	5.2 Mby, 3.5", 2 hd- ? cyl, 117ms
"Cricket"		
Seagate	ST506	5.2 Mby formatted, 4 hd-156 cycles
Tandon	602S	5.2 Mby formatted, 4 hd-156 cyl, 153ms
(2) CMI	CM6213	10.4 Mby formatted, 2 hd-640 cyl, 40 ms
Tandon	603E	10.4 Mby formatted, 6 hd-230 cyl, 210ms
(2) Atasi	3320	15.6 Mby formatted, 3 hd-635 cyl, 30ms
(2) CDC	9415-5/21	15.6 Mby formatted, 3 hd-675 cyl, 45ms
"Wren"		
Evotec	5530	15.6 Mby formatted, 6 hd-375 cyl, 49ms
(2) Memorex	512	15.6 Mby formatted, 3 hd- ? cyl, 25ms
(3) Quantum	Q520	15.6 Mby formatted, 4 hd-512 cyl, 45ms

Notes:

(1). Requires custom configuration PROM.
(2). Requires custom configuration PROM. Supported only on 120179-xx PCB (**WINC-05/5** or **WINC-05/8**).

20 Megabyte Drives (Complete List)

			Unformatted Capacity	Heads/Cylinders	Avg Access	Avail 1st Ship
(1)	Seagate	425	25	8/306	85ms	(6/84)
	Seagate	4026	25.6	4/?	40ms	(4/85)
	Seagate	225	? 20Mbyfmt	1/2 high		
(1)	Distron	526	25.5	8/306	77ms	(N/A)
(3)	Distron	D7xx	26.9	3/?	35ms	(N/A)
	Microsci	HH725	25.5	?	80ms	
	NEC	D5244	25.8	?		
(3)	Micropo	1302	25.9	3/830	30ms	(9/83)
(1)	Fujitsu	2235	26.2	8/306	85ms	(9/83)
(2)	Tulin	TL226	26.7	4/640	75ms	(3/84)
(2)	CMI	CM6426	26.7	4/640	40ms	(8/83)
(1)	Ampex	27	27	8/320	85ms	(5/83)
(1)	Rodime	R0204	27.7	8/320	85ms	(10/82)
(2)	Rodime	R0202E	26.7	4/640	55ms	(2/84)
	Tandon	703	30.1	?	39ms	?
(3)	Vertex	V130	30.8	3/987	30ms	(10/85)
(3)	Cynthia	D530	30.8	3/987	30ms	=Vertex V130
	Tandon	TM703	31	5/?	39ms	?
	Evotec	5540	31.2	8/375	(N/A)	
(3)	Quantum	Q530	31.9	6/512	49ms	(8/84)
	Syquest	SQ325F	25.5	4/612	99ms	(5/85)
	Miniscribe	8425	--- 21.4Mbyfmt		68ms	(7/85)

Notes:

(1), (2). Standard Configuration
(3). Requires custom configuration PROM. Supported only on 120179-xx PCB (**WINC-05/5** or **WINC-05/8**).

Drives Over 20 Mby (formatted)

	Unformatted Capacity	Heads/ Cylinders	Avg Access	Availability (1st ship)
26.2 Mby - 2 X RL02 1 X RL01		**(31.24 Mby unfmt, min, or 3013 tracks)**		
(2) Fujitsu	M2241AS	31.4	4/754	35ms (8/84)
(2) Atasi	3033	33.1	5/635	(10/85)
(2) Memorex	513	39.3	5/?	25ms ?
(4) CDC	9415-5/36	36.3	5/679	45ms (10/85)
31.5 Mby - 3 X RL02		**(37.5 Mby unfmt, min, or 3615 tracks)**		
(1,3)Tulin 1/2" high	240	40.0	6/640	75ms now(4/84)
(1) CMI	5640	40.0	6/640	40ms now(8/83)
(1) Rodime	R0203E	40.0	6/640	55ms now(1/84)
(1) Rodime	R0206	40.0	6/640	55ms now(1.84)
(2) IMI	5650H	41.0	8/?	49ms now
(4) Quantum	Q540	42.6	8/512	49ms now(8/84)
(2) Micropo	1323	42.6	4/1022	25ms ?
(2) Micropo	1303	43.2	5/830	30ms now(9/83)
(2) Distron	D7xx	44.9	5/?	35ms (N/A)
Minisor ?	5338	?	?	?
(4,3)Syquest	SQ338	38.2	6/612	99ms (5/85)
36.7 Mby - 3 X RL02 1 X RL01		**(42.54 Mby unfmt, min, or 4218 tracks)**		
(4,3)Atasi	3046	46.3	7/635	now?
(2) Maxtor	?	47.8	6/918	11/83?
41.9 Mby - 4 X RL02		**(50.0 Mby unfmt, min, or 4820 tracks)**		
(2) Tandon	705	50.1	?	39ms ?
(1) Miniscri	5451	?	8/?	90ms ?
(2) Vertex	V150	51.4	5/987	30ms now?
(2) Cynthia	D550	51.4	5/987	30ms =Vertex V150
(4,3)Microp.	1304	51.9	6/830	30ms now(9/83)
(1,3)Rodime	R0204E	53.3	8/640	55ms now(1/84)
(1,3)Rodime	R0208	"	"	" "
(4) Priam	502	55.0	7/755	32ms now(11/83)
(4) Fujitsu	M2242AS	55.0	7/754	35ms now(8/84)
(2) Memorex	514	55.1	7/	25ms ?
(4) Atasi	3051	51.3	7/704	

Notes:

(1). Standard configuration.
(2). Requires custom configuration PROM. Supported only on 120179-xx PCB (**WINC-05/5** or **WINC-05/8**).
(3). Tested on **WINC-05**.
(4). See Sheet 6 for prom.
(?). Specification not received by **AED**.

5 1/4" FLOPPY DISK, 1/2 height (1.6") or full high (3.4")
(these emulate a RX02 disk on a double sided drive)

General: 2 Side, 250Kbps, 1.0Mby, 96Tpi, 80Tk,
94 ms avg access at 3 ms step

Alps	AFD222	1/2 high
Canon	MDD221	3/8 high
(1) CDC	9429	1/2 high, 3ms step,15ms settle
Epson	SD570	1/2 high
Epson	SD540	1/2 high
Hi Tech	596-10	1/2 high
1,4)Mits.	M4853	1/2 high, 3ms step,15ms settle,250ms start
(1) Philips	X3134	1/2 high, 3ms step
(1) Sangyo	FB504	1/2 high, 3ms step
(1) Qume	192	1/2 high, 3ms step,15ms settle,500ms start
Remex	RFD965	1/2 high
(1) Shugart	SA465	1/2 high, 3ms step,15ms settle,500ms start
(1) Sumitomo	FDA5300	1/2 high, 3ms step,15ms settle, n.s. start
Tandon	TM55-4	1/2 high
(1,4)TEAC	FD55F	1/2 high, 3ms step,15ms settle,400ms start
(1) TEK (NSA)	FB504	1/2 high, 3ms step
(1) YE Data	YD480	1/2 high, 3ms step
BASF	6238	2/3 high
(2) Remex	RFD960	2/3 high, 5ms step,25ms settle,200ms start
(2,4)CDC	9409T	full high,5ms step,15ms settle,50ms h.load
(2) MPI	92	full high,5ms step,25ms settle,35ms h.load
(2) Microp	1115VI	full high,6ms step
(1,4)Qume	592	full high,3ms step,15ms settle,1000ms start
(2) Remex	RFD960	full high,5ms step
(2,4)Shug	SA460	full high,6ms step,15ms settle,200ms start
(1) Tandon	TM100-4	full high,3ms step,15ms settle,250ms start
(1,4)YE Data	YD280	full high,3ms step,15ms settle,1000 ms start
(2) WST	FDD221-5	full high,5ms step

Floppy Disk -- 3.5" Diskette -- 5 1/4" Interface
(these emulate a RX02 disk on a double sided drive)

General: 2 Side, 250Kbps, 1.0Mby, 135Tpi, 80Tk, 158ms avg access

Epson	SMD180
Mitsubishi	MF353
(2,4)Shugart	SA350 1/2 high,6ms step,15ms settle,500ms start
TEAC	FD-35F

Notes:

1. Uses standard 5 1/4" configuration PROM.
2. Requires 5 1/4" (Shugart) configuration PROM.
3. Needs custom configuration PROM.
4. Tested on **WINC-05**.

5 1/4" Floppy Disk, with 8" Performance, with 5 1/4" Interface
(these use the 8" floppy configuration PROM, emulating RX01, RX02, or RX03 floppy disks), with motor on control.

General: 2 Side, 1/2 high, 500Kbps, 1.6Mby, 96Tpi, 77Tk, 91ms avg seek

(2,4)C Itoh	YD380T	1/2 high,3ms step,15ms settle,1000ms start
Epson	SD560	1/2 high
HiTech	596-16	1/2 high
Micropo	1117VI	full hi
(2) Mits	M4854	1/2 high,3ms step,15ms settle,250ms start
(2) Philips	X3138	1/2 high,3ms step
(2) Shugart	SA475	1/2 high,3ms step,15ms settle,500ms start
TEAC	FD55G	1/2 high
(2,4)YE Data	YD380	1/2 high,3ms step,15ms settle,1000ms start
Mits	M4855	1/2 high 2.0Mby
Tandon	TM102-2	full hi 2.0Mby

Floppy Disk -- 8", 1/2 height (2.3")

General: 2 Side,1/2 high, 500Kbps, 1.6Mby, 48Tpi, 77Tk,76ms avg access

BASF	6105	1/2 high
(1) MPI	42	3/8 high,3 ms step
(1) Mits	M2896-63	1/2 high,3ms step,15ms settle,35ms h.load
(1,4)NEC	FD1165	1/2 high,3ms step,15ms settle,35ms h.load
(1,4)Qume	242	1/2 high,3ms step,15ms settle,50ms h.load
(2) Shugart	SA860	1/2 high,3ms step
(2,4)Tandon	TM848e-2	1/2 high,3ms step,15ms settle,500ms start
Toshiba	ND40D	1/2 high 94ms
(1,4)YE Data	YD180	1/2 high,3ms step,15ms settle,50ms h.load

Floppy Disk -- 8", full height (4.5")

General: 2 Side,1/2 high, 500Kbps, 1.6Mby,48Tpi, 77Tk, 76ms avg access

(1) CDC	9406-4	2 side,3ms step,15ms settle,35ms hd load
(1) Decitek	8302/T	2 side,3ms step,15ms settle,35ms hd load
(1) Mits	M2894-63	2 side,3ms step,15ms settle,35ms hd load
(1) Memorex	552	2 side,3ms step,15ms settle,35ms hd load
(?) MFE	750	2 side, ? ? ?
(1) Qume	DT8	2 side,3ms step,15ms settle,35ms hd load
(1) Shugart	SA850	2 side,3ms step,15ms settle,35ms hd load
(1) YE Data	YD174D	2 side,3ms step,15ms settle,35ms hd load
(3) CDC	9404B	1 side,10ms step,15ms settle,60ms hd load
(3) Memorex	550	1 side,6ms step,15ms settle,35ms hd load
(3) Shugart	SA800/1	1 side,8ms step,8ms settle,35ms hd load
(?) Siemens	100-8	? side,3ms step,15ms settle,25ms hd load

Notes:

1. Uses either 8" configuration PROM.
2. Uses 8" (Tandon) configuration PROM.
3. Requires custom configuration PROM.
4. Tested on **WINC-05**.
5. (?) Specifications not provided to **AED**.

APPENDIX C

PROM AVAILABILITY LIST

WINC-Ø5/5, Ø5/8 Board Configurations Sorted by Type

12Ø179 PWA	89ØØ63 C PROM	Winchesters	Floppies
Type is 8" Qume 242 or Equivalent			
-Ø1	-11	1Ø Mby--one ST412	two 8" head-load floppy
-Ø4	-13	2Ø Mby--two ST412	two 8" head-load floppy
-Ø2	-12(-37)	2Ø Mby--one Ro 2Ø4 (ST425)	two 8" head-load floppy
-Ø6	-2Ø(-38)	4Ø Mby--two Ro 2Ø4 (ST425)	two 8" head-load floppy
Type is 8" Tandon or Others			
-Ø3	-18	1Ø Mby--one ST412	two 8" motor-on floppy
Type is 8" NEC Floppy			
-1Ø	-12(-37)	2Ø Mby--one Ro 2Ø4 (ST425) (currently delivered as 12Ø245-Ø1)	two 8" NEC floppy
Type is with Sigma RXØ2 double-sided floppy compatibility. 1st issue was EDAX. Also delivered as 12Ø245-Ø2 with -7Ø configuration prom.			
-11		1ØMby--one ST412	two 8" motor-on floppy
-12	-62(-7Ø)	1ØMby--one ST412	two 8"
Type is Without AED Prompt (YD 38Ø drive)			
-Ø5	-26	2Ø Mby--one Ro 2Ø4	two 8" motor-on floppy, $ prompt
-Ø7	-27	4Ø Mby--two Ro 2Ø4	two 8" motor-on floppy, $ prompt
Type is AED Format 5" Floppy			
-Ø8	-Ø2(-45)	1Ø Mby--one ST412 (same as 12Ø12Ø-Ø1 pwa)	one (two) 5" floppy
-Ø9	-Ø9(-39)	2Ø Mby--one Ro 2Ø4 (same as 12Ø119-Ø2 pwa)	two 5" floppy

General Note: Configuration PROM in parenthesis is being incorporated into the board, and adds the support listed in parenthesis.

WINC-05/5

Model Number	Part Number	Description
5P001	890063-01 E	DL0- (RL01) Seagate ST506 5.24Mby DY0- (AED RX02) 5 1/4" Qume 592
	890063-02 E	DL0- (RL02) Seagate ST412 10.48Mby DY0- (AED RX02) 5 1/4" Qume 592
5P002	890063-45 E	DL0- (RL02) Seagate ST412 10.48Mby DY0- (AED RX02) 5 1/4" Qume 592 DY0- (AED RX02) 5 1/4" Qume 592
5P003	890063-04 E	DL0- (RL02) Seagate ST412 10.48Mby DL1- (RL02) 2nd ST412 10.48Mby DY0- (AED RX02) 5 1/4" Qume 592 DY0- (AED RX02) 5 1/4" Qume 592
5P004	890063-15 E	DL0- (RL01) Seagate ST419 15.72Mby DL1- (RL01) mapped 3 RL01'S DL2- (RL01) DY0- (AED RX02) 5 1/4" Qume 592 DY1- (AED RX02) 5 1/4" Qume 592
	890063-10 E	DL0- (RL01) Seagate ST412 10.48Mby DL1- (RL01) mapped 2 RL01'S DY0- (AED RX02) 5 1/4" Qume 592
5P005	890063-46 E	DL0- (RL01) Seagate ST412 10.48Mby DL1- (RL01) mapped 2 RL01'S DY0- (AED RX02) 5 1/4" Qume 592 DY1- (AED RX02) 5 1/4" Qume 592
5P006	890063-16 E	DL0- (RL02) Seagate ST419 15.72Mby DL1- (RL01) mapped 1 RL02+ 1 RL01 DY0- (AED RX02) 5 1/4" Qume 592 DY1- (AED RX02) 5 1/4" Qume 592
5P007	890063-06 E	DL0- (RL02) AMP/Rodime 202 10.48Mby DY0- (AED RX02) 5 1/4" Qume 592
5P008	890063-05 E	DL0- (RL02) AMP/Rodime 204 20.96Mby DL1- (RL02) mapped 2 RL02'S DY0- (AED RX02) 5 1/4" Qume 592

WINC-Ø5/5

Model Number	Part Number	Description
	890063-09 E	DLØ- (RLØ2) AMP/Rodime 2Ø4 2Ø.96Mby DL1- (RLØ2) mapped 2 RLØ2'S DYØ- (AED RXØ2) 5 1/4" Qume 592 DY1- (AED RXØ2) 5 1/4" Qume 592
5PØØ9	890063-39 E	DLØ- (RLØ2) Seagate ST425 or AMP/Rodime 2Ø4 2Ø.96Mby DL1- (RLØ2) mapped 2 RLØ2'S DYØ- (AED RXØ2) 5 1/4" Qume 592 DY1- (AED RXØ2) 5 1/4" Qume 592
	890063-19 E	DLØ- (RLØ2) AMP/Rodime 2Ø4 2Ø.96Mby DL1- (RLØ2) mapped 2 RLØ2'S DL2- (RLØ2) 2nd 2Ø4 2Ø.96Mby DL3- (RLØ2) mapped 2 RLØ2'S DYØ- (AED RXØ2) 5 1/4" Qume 592 DY1- (AED RXØ2) 5 1/4" Qume 592
5PØ1Ø	890063-4Ø E	DLØ- (RLØ2) Seagate ST425 or AMP/Rodime 2Ø4 2Ø.96Mby DL1- (RLØ2) mapped 2 RLØ2'S DL2- (RLØ2) 2nd 2Ø.96Mby drive DL3- (RLØ2) mapped 2 RLØ2'S DYØ- (AED RXØ2) 5 1/4" Qume 592 DY1- (AED RXØ2) 5 1/4" Qume 592
5PØ11	890063-Ø7 E	DLØ- (RLØ2) CMI 5412 1Ø.48Mby DYØ- (AED RXØ2) 5 1/4" Qume 592
5PØ12	890063-17 E	DLØ- (RLØ1) CMI 5419 2Ø.96Mby DL1- (RLØ1) mapped 3 RLØ1'S DL2- (RLØ1) DYØ- (AED RXØ2) 5 1/4" Qume 592 DY1- (AED RXØ2) 5 1/4" Qume 592
5PØ13	890063-Ø8 E	DLØ- (RLØ1) CMI 5412 1Ø.48Mby DL1- (RLØ1) mapped 2 RLØ1'S DYØ- (AED RXØ2) 5 1/4" Qume 592
5PØ14	890063-34 E	DLØ- (RLØ2) Seagate ST412 1Ø.48Mby DL1- (RLØ2) Seagate ST412 1Ø.48Mby DYØ- (AED RXØ2) Shugart SA46Ø DY1- (AED RXØ2) Shugart SA46Ø

WINC-Ø5/5

Model Number	Part Number	Description
5PØ15	89ØØ63-35 E	DLØ- (RLØ2) Rodime 2Ø4E(2Ø8) 41.92Mby DL1- (RLØ2) mapped 4 RLØ2'S DL2- (RLØ2) DL3- (RLØ2) DYØ- (AED RXØ2) 5 1/4" Qume 592 DY1- (AED RXØ2) 5 1/4" Qume 592
5PØ16	89ØØ63-44 E	DLØ- (RLØ2) Seagate ST412 1Ø.48Mby DL1- (RLØ1) Syquest SQ3Ø6F cartridge DYØ- (AED RXØ2) 5 1/4" Qume 592 DY1- (AED RXØ2) 5 1/4" Qume 592
5PØ17	89ØØ63-55 E	DLØ- (RLØ2) Seagate ST425 or AMPEX 27/Rodime 2Ø4 2Ø.96Mby DL1- (RLØ2) mapped 2 RLØ2'S DL2- (RLØ2) Syquest SQ312 cartridge DYØ- (AED RXØ2) 5 1/4" Qume 592 DY1- (AED RXØ2) 5 1/4" Qume 592
5PØ18	89ØØ63-73 E	DLØ- (RLØ2) Atasi 3Ø46 DL1- (RLØ2) mapped 3 RLØ2's DL2- (RLØ2) and 1 RLØ1 DL3- (RLØ1) DYØ- (AED RXØ2) 5 1/4" Qume 592 DY1- (AED RXØ2) 5 1/4" Qume 592
5PØ19	89ØØ63-74 E	DLØ- (RLØ2) Seagate ST412 1Ø.48Mby DYØ- (AED RXØ2) 5 1/4" Qume 592 DY1- (AED RXØ2) 5 1/4" Qume 592 Bootstrap self test enabled. Bootstrap graphics self test enabled.
5PØ2Ø	89ØØ63-75 E	DLØ- (RLØ1) Syquest SQ3Ø6 cartridge DL1- (RLØ1) Second Syquest SQ3Ø6 DYØ- (AED RXØ2) 5 1/4" Qume 592 DY1- (AED RXØ2) 5 1/4" Qume 592 Bootstrap self test enabled.

WINC-Ø5/8

Model Number	Part Number	Description
8PØØ1	890063-14 E	DLØ- (RLØ1) Seagate ST412 1Ø.48Mby DL1- (RLØ1) mapped 2 RLØ1'S DYØ- (RXØ1/Ø2) 8" Qume 242 DY1- (RXØ1/Ø2) 8" Qume 242
8PØØ2	890063-13 E	DLØ- (RLØ2) Seagate ST412 1Ø.48Mby DL1- (RLØ2) 2nd ST412 1Ø.48Mby DYØ- (RXØ1/Ø2) 8" Qume 242 DY1- (RXØ1/Ø2) 8" Qume 242
8PØØ3	890063-11 E	DLØ- (RLØ2) Seagate ST412 1Ø.48Mby DYØ- (RXØ1/Ø2) 8" Qume 242 DY1- (RXØ1/Ø2) 8" Qume 242
8PØØ4	890063-18 E	DLØ- (RLØ2) Seagate ST412 1Ø.48Mby DYØ- (RXØ1/Ø2) YE Data YD18Ø or YD38Ø DY1- (RXØ1/Ø2) YE Data YD18Ø or YD38Ø
	890063-12 E	DLØ- (RLØ2) AMP/Rodime 2Ø4 2Ø.96Mby DL1- (RLØ2) mapped 2 RLØ2'S DYØ- (RXØ1/Ø2) 8" Qume 242 DY1- (RXØ1/Ø2) 8" Qume 242
8PØØ5	890063-37 E	DLØ- (RLØ2) Seagate ST425 2Ø.96Mby or AMPex 27/Rodime 2Ø4 DL1- (RLØ2) mapped 2 RLØ2'S DYØ- (RXØ1/Ø2) 8" Qume 242 DY1- (RXØ1/Ø2) 8" Qume 242
	890063-2Ø E	DLØ- (RLØ2) AMP/Rodime 2Ø4 2Ø.96Mby DL1- (RLØ2) mapped 2 RLØ2'S DL2- (RLØ2) 2nd 2Ø4 2Ø.96Mby DL3- (RLØ2) mapped 2 RLØ2'S DLØ- (RXØ1/Ø2) 8" Qume 242 DY1- (RXØ1/Ø2) 8" Qume 242
8PØØ6	890063-38 E	DLØ- (RLØ2) Seagate ST425 2Ø.96Mby or AMPex P27/Rodime 2Ø4 DL1- (RLØ2) mapped 2 RLØ2'S DL2- (RLØ2) 2nd 2Ø.96Mby drive DL3- (RLØ2) mapped 2 RLØ2'S DLØ- (RXØ1/Ø2) 8" Qume 242 DY1- (RXØ1/Ø2) 8" Qume 242

WINC-05/8

Model Number	Part Number	Description
8P008	890063-21 E	DL0- (RL02) Seagate ST412 10.48Mby DL1- (RL02) 2nd ST412 10.48Mby DY0- (RX01/RX02) YE Data YD180 or YD380 DY1- (RX01/RX02) YE Data YD180 or YD380
	890063-23 E	DL0- (RL02) AMP/Rodime 204 20.96Mby DL1- (RL02) mapped 2 RL02'S DY0- (RX01/RX02) YE Data YD180 or YD380 DY1- (RX01/RX02) YE Data YD180 or YD380
8P009	890063-42 E	DL0- (RL02) Seagate ST425 or AMPex 27/Rodime 204 20.96Mby DL1- (RL02) mapped 2 RL02'S DY0- (RX01/RX02) YE Data YD180 or YD380 DY1- (RX01/RX02) YE Data YD180 or YD380
8P010	890063-24 E	DL0- (RL02) Seagate ST412 10.48Mby DY0- (RX01/RX02) YE Data YD180 or YD380 DY1- (RX01/RX02) YE Data YD180 or YD380 boot prompt is '$', floppy is YD380
8P011	890063-25 E	DL0- (RL02) Seagate ST412 10.48Mby DL1- (RL02) 2nd ST412 10.48Mby DY0- (RX01/RX02) YE Data YD180 or YD380 DY1- (RX01/RX02) YE Data YD180 or YD380 boot prompt is '$', floppy is YD380
8P012	890063-26 E	DL0- (RL02) AMP/Rodime 204 20.96Mby DL1- (RL02) mapped 2 RL02'S DY0- (RX01/RX02) YE Data YD180 or YD380 DY1- (RX01/RX02) YE Data YD180 or YD380 boot prompt is '$', floppy is YD380
8P013	890063-27 E	DL0- (RL02) AMP/Rodime 204 20.96Mby DL1- (RL02) mapped 2 RL02'S DL2- (RL02) AMP/Rodime 204 20.96Mby DL3- (RL02) mapped 2 RL02'S DY0- (RX01/RX02) YE Data YD180 or YD380 DY1- (RX01/RX02) YE Data YD180 or YD380 boot prompt is '$', floppy is YD380

WINC-Ø5/8

Model Number	Part Number	Description
	890063-28 E	DLØ- (RLØ2) AMP/Rodime 204 20.96Mby DL1- (RLØ2) mapped 2 RLØ2'S DL2- (RLØ2) AMP/Rodime 204 20.96Mby DL3- (RLØ2) mapped 2 RLØ2'S DYØ- (RXØ1/RXØ2) YE Data YD18Ø or YD38Ø DY1- (RXØ1/RXØ2) YE Data YD18Ø or YD38Ø
8PØ14	890063-41 E	DLØ- (RLØ2) Seagate ST425 or AMPex 27/Rodime 204 20.96Mby DL1- (RLØ2) mapped 2 RLØ2'S DL2- (RLØ2) second 20.96Mby drive DL3- (RLØ2) mapped 2 RLØ2'S DYØ- (RXØ1/RXØ2) YE Data YD18Ø or YD38Ø DY1- (RXØ1/RXØ2) YE Data YD18Ø or YD38Ø
8PØ15	890063-29 E	DLØ- (RLØ2) Rodime 206(203E) 31.44Mby DL1- (RLØ2) mapped 3 RLØ2'S DL2- (RLØ2) DYØ- (RXØ1/RXØ2) YE Data YD18Ø or YD38Ø DY1- (RXØ1/RXØ2) YE Data YD18Ø or YD38Ø
8PØ16	890063-3Ø E	DLØ- (RLØ2) Rodime 208(204E) 41.92Mby DL1- (RLØ2) mapped 4 RLØ2'S DL2- (RLØ2) DL3- (RLØ2) DYØ- (RXØ1/RXØ2) YE Data YD18Ø or YD38Ø DY1- (RXØ1/RXØ2) YE Data YD18Ø or YD38Ø
8PØ17	890063-31 E	DLØ- (RLØ2) Seagate ST419 15.72Mby DL1- (RLØ1) mapped 1 RLØ2+ 1 RLØ1 DYØ- (RXØ1/RXØ2) YE Data YD18Ø or YD38Ø DY1- (RXØ1/RXØ2) YE Data YD18Ø or YD38Ø
8PØ18	890063-32 E	DLØ- (RLØ2) CMI 5419 15.72Mby DYØ- (RXØ1/RXØ2) YE Data YD18Ø or YD38Ø DY1- (RXØ1/RXØ2) YE Data YD18Ø or YD38Ø
8PØ19	890063-33 E	DLØ- (RLØ2) CDC9415-36-5 DL1- (RLØ2) mapped 2 RLØ2'S DL2- (RLØ1) and 1 RLØ1 DYØ- (RXØ1/RXØ2) YE Data YD18Ø or YD38Ø DY1- (RXØ1/RXØ2) YE Data YD18Ø or YD38Ø

WINC-Ø5/8

Model Number	Part Number	Description
8PØ2Ø	890063-36 E	DLØ- (RLØ2) Atasi 3Ø46 DL1- (RLØ2) mapped 3 RLØ2'S DL2- (RLØ2) and 1 RLØ1 DL3- (RLØ1) DYØ- (RXØ1/RXØ2) YE Data YD18Ø or YD38Ø DY1- (RXØ1/RXØ2) YE Data YD18Ø or YD38Ø
8PØ21	890063-43 E	DLØ- (RLØ2) Seagate ST412 1Ø.48Mby DL1- (RLØ1) Syquest SQ306F cartridge DYØ- (RXØ1/RXØ2) 8" Qume 242 DY1- (RXØ1/RXØ2) 8" Qume 242
8PØ22	890063-47 E	DLØ- (RLØ2) Seagate ST412 or Fujitsu 1Ø.48 Mby DL1- (RLØ2) mapped 2 RLØ2'S DYØ- (RXØ1/RXØ2) Shugart SA8ØØ DY1- (RXØ1/RXØ2) Shugart SA8ØØ
8PØ23	890063-48 E	DLØ- (RLØ2) Seagate ST412 or Fujitsu M2233 1Ø.48 Mby DL1- (RLØ2) Second 1Ø.48 Mby drive DYØ- (RXØ1/RXØ2) Shugart SA8ØØ 1 sided DY1- (RXØ1/RXØ2) Shugart SA8ØØ 1 sided
8PØ24	890063-49 E	DLØ- (RLØ2) Quantum Q54Ø 31.44 Mby DL1- (RLØ2) mapped 3 RLØ2's DL2- (RLØ2) DYØ- (RXØ1/RXØ2) Shugart SA86Ø DY1- (RXØ1/RXØ2) Shugart SA86Ø
8PØ25	890063-5Ø E	DLØ- (RLØ2) Quantum Q54Ø 31.44 Mby DL1- (RLØ2) mapped 3 RLØ2's DL2- (RLØ2) DYØ- (RXØ1/RXØ2) Shugart SA8ØØ 1 sided DY1- (RXØ1/RXØ2) Shugart SA8ØØ 1 sided
8PØ26	890063-51 E	DLØ- (RLØ2) Fujitsu M2242as 41.92 Mby DL1- (RLØ2) mapped 4 RLØ2's DL2- (RLØ2) DL3- (RLØ2) DYØ- (RXØ1/RXØ2) Shugart SA86Ø/YD38Ø DY1- (RXØ1/RXØ2) Shugart SA86Ø/YD38Ø
8PØ27	890063-52 E	DLØ- (RLØ2) Micropolis 13Ø4 41.92 Mby DL1- (RLØ2) mapped 4 RLØ2's DL2- (RLØ2) DL3- (RLØ2) DYØ- (RXØ1/RXØ2) Qume 242/NEC FD1165 DY1- (RXØ1/RXØ2) Qume 242/NEC FD1165

WINC-Ø5/8

Model Number	Part Number	Description
8PØ28	890063-53 E	DLØ- (RLØ2) Seagate ST425 or AMPex 27/Rodime 2Ø4 2Ø.96Mby DL1- (RLØ2) mapped 2 RLØ2'S DL2- (RLØ2) Syquest SQ312 cartridge DYØ- (RXØ1/RXØ2) YE Data YD18Ø or YD38Ø DY1- (RXØ1/RXØ2) YE Data YD18Ø or YD38Ø
8PØ29	890063-54 E	DLØ- (RLØ2) Syquest SQ312 cartridge DL1- (RLØ2) second Syquest SQ312 DYØ- (RXØ1/RXØ2) YE Data YD18Ø or YD38Ø DY1- (RXØ1/RXØ2) YE Data YD18Ø or YD38Ø
8PØ3Ø	890063-56 E	DLØ- (RLØ2) Atasi 3Ø33 DL1- (RLØ2) mapped 2 RLØ2'S DL2- (RLØ1) and 1 RLØ1 DYØ- (RXØ1/RXØ2) YE Data YD18Ø or YD38Ø DY1- (RXØ1/RXØ2) YE Data YD18Ø or YD38Ø Bootstrap self test enabled
8PØ31	890063-57 E	DLØ- (RLØ2) DMA 36Ø cartridge DL1- (RLØ2) second DMA 36Ø DYØ- (RXØ1/RXØ2) YE Data YD18Ø or YD38Ø DY1- (RXØ1/RXØ2) YE Data YD18Ø or YD38Ø Bootstrap self test enabled
8PØ32	890063-58 E	DLØ- (RLØ1) Syquest SQ3Ø6 cartridge DL1- (RLØ1) second Syquest SQ3Ø6 DYØ- (RXØ1/RXØ2) YE Data YD18Ø or YD38Ø DY1- (RXØ1/RXØ2) YE Data YD18Ø or YD38Ø Bootstrap self test enabled
8PØ33	890063-59 E	DLØ- (RLØ2) Seagate ST425 or AMPex 27/Rodime 2Ø4 2Ø.96Mby DL1- (RLØ2) mapped 2 RLØ2'S DL2- (RLØ1) Syquest SQ3Ø6 cartridge DYØ- (RXØ1/RXØ2) YE Data YD18Ø or YD38Ø DY1- (RXØ1/RXØ2) YE Data YD18Ø or YD38Ø Bootstrap self test enabled
8PØ34	890063-6ØE	DLØ- (RLØ2) Seagate ST425 or Fujitsu M2235--2Ø.96Mby DL1- (RLØ2) mapped 2 RLØ2'S DYØ- (RXØ1/RXØ2) Shugart SA8ØØ 1 sided DY1- (RXØ1/RXØ2) Shugart SA8ØØ 1 sided Bootstrap self test enabled

WINC-Ø5/8

Model Number	Part Number	Description
8PØ35	890063-66 E	DLØ- (RLØ2) Seagate ST425 2Ø.96Mby or AMPex 27/Rodime 2Ø4
	(equivalent 890063-37/12	DL1- (RLØ2) mapped 2 RLØ2'S DYØ- (RXØ1/Ø2) 8" Qume 242 DY1- (RXØ1/Ø2) 8" Qume 242 Bootstrap self test enabled Interrupt priority 4 for RL and RX
	890063-61 E	Replaced by 8PØ35
8PØ36	890063-62 E	DLØ- (RLØ2) Seagate ST412 1Ø.48Mby Floppy compatible with Sigma RXØ2 disk DYØ- (RXØ1/Ø2) 8" Shugart SA86Ø DY1- (RXØ1/Ø2) 8" Shugart SA86Ø Bootstrap self test enabled
8PØ37	890063-63 E	DLØ- (RLØ2) Quantum Q54Ø 31.44 Mby DL1- (RLØ2) mapped 3 RLØ2's DL2- (RLØ2) Floppy compatible with Sigma RXØ2 disk DYØ- (RXØ1/RXØ2) Shugart SA86Ø DY1- (RXØ1/RXØ2) Shugart SA86Ø Bootstrap self test enabled
8PØ38	890063-64 E	DLØ- (RLØ2) Rodime 2Ø2E, CMI 6426 2ØMby DL1- (RLØ2) mapped 2 RLØ2's DYØ- (RXØ1/RXØ2) YE Data YD18Ø or YD38Ø DY1- (RXØ1/RXØ2) YE Data YD18Ø or YD38Ø Bootstrap self test enabled
8PØ39	890063-65 E	DLØ- (RLØ2) Syquest SQ338 31.2Mby DL1- (RLØ2) mapped 3 RLØ2's DL2- (RLØ2) DYØ- (RXØ1/RXØ2) YE Data YD18Ø or YD38Ø DY1- (RXØ1/RXØ2) YE Data YD18Ø or YD38Ø Bootstrap self test enabled
8PØ4Ø	890063-67 E	DLØ- (RLØ2) Rodime 2Ø8(2Ø4E) 41.92Mby DL1- (RLØ2) mapped 4 RLØ2's DL2- (RLØ2)
	(equivalent 890063-3Ø)	DL3- (RLØ2) DYØ- (RXØ1/RXØ2) YE Data YD18Ø or YD38Ø DY1- (RXØ1/RXØ2) YE Data YD18Ø or YD38Ø Bootstrap self test enabled Interrupt priority is 4

Model Number	Part Number	Description
8P041	890063-68 E	DL0- (RL02) Miniscribe 10.48Mby DY0- (RX01/02) Shugart SA860 DY1- (RX01/02) Shugart SA860 Bootstrap self test enabled
8P042	890063-69 E (equivalent 890063-20/38)	DL0- (RL02) Seagate ST425 20.96Mby or Ampex P27/Rodime 204 DL1- (RL02) mapped 2 RL02's DL2- (RL02) 2nd 20.96Mby drive DL3- (RL02) mapped 2 RL02's DY0- (RX01/02) 8" Qume 242 DY1- (RX01/02) 8" Qume 242 Bootstrap self test enabled Interrupt priority is 4
8P043	890063-70 E	DL0- (RL02) Seagate ST412 10.48Mby DY0- (RX01/02) 8" Qume 242, NEC 1165 DY1- (RX01/02) 8" Qume 242, NEC 1165 Floppy compatible with Sigma RX02 disk Bootstrap self test enabled
8P044	890063-71 E	DL0- (RL02) Quantum Q540 31.44Mby DL1- (RL02) mapped 3 RL02's DL2- (RL02) DY0- (RX01/RX02) 8" Qume 242, NEC 1165 DY1- (RX01/RX02) 8" Qume 242, NEC 1165 Floppy compatible with Sigma RX02 disk Bootstrap self test enabled
8P045	890063-72 E	DL0- (RL01) Seagate SA506 5.24Mby DY0- (RX01/02) Shugart SA860 DY1- (RX01/02) Shugart SA860 Bootstrap self test enabled
8P046	890063-76	DL0- (RL02) Seagate ST4038 DL1- (RL02) or Micropolis 1304 DL2- (RL02) mapped 3 RL02's DY0- (RX01/RX02) 8" Qume 242, NEC 1165 DY1- (RX01/RX02) 8" Qume 242, NEC 1165 Bootstrap self test enabled.
8P047	890063-77 E	DL0- (RL02) Seagate St412 or DL1- (RL02) Syquest SQ312 cartridge DY0- (RX01/RX02) 8" Qume 242, NEC 1165 DY1- (RX01/RX02) 8" Qume 242, NEC 1165 Boostrap self test enabled.

Model Number	Part Number	Description
8P048	890063-78 E	DL0- (RL02) Rodime 202E, TEAC 520 20Mby DL1- (RL02) mapped 2 RL02's DL2- (RL02) Second 20Mby drive DL3- (RL02) mapped 2 RL02's DY0- (RX01/RX02) YE Data YD180 or YD380 DY1- (RX01/RX02) YE Data YD180 or YD380 Bootstrap self test enabled.
8P049	890063-79 E	DL0- (RL02) Microscience HA315 - 10Mby DL1- (RL02) Syquest SQ312 cartridge DY0- (RX01/RX02) 8" Qume 242, NEC 1165 DY1- (RX01/RX02) 8" Qume 242, NEC 1165

Prom Cross Reference (890063-XX)

New Configuration Prom Numbers

890063 -xx	Config 8" flpy	Config 5" flpy	890063 -xx	Config 8" flpy	Config 5" flpy
-01		5P001	-21	8P008	
-02	(use -45)	-22	(freeport)		
-03	(freeport)		-23	(use -42)	
-04	5P003		-24	8P010	
-05	use -09	5P008	-25	8P011	
-06		5P011	-26	8P012	
-07		5P011	-27	8P013	
-08		5P013	-28	(use -41)	
-09	use -39		-29	8P015	
-10	use -46		-30	8P016	
-11	8P003		-31	8P017	
-12	use -37		-32	8P018	
-13	8P002		-33	8P019	
-14	8P001		-34		5P014
-15		5P004	-35		5P015
-16	8P007	5P006?	-36	8P020	
-17		5P012	-37	8P005	
-18	8P004	5P018	-38	8P006	
-19	use -40	5P019	-39		5P009
-20	use -38	5P020	-40		5P010
-41	8P014		-61	8P035	
-42	8P009		-62	8P036	
-43	8P021		-63	8P037	
-44		5P016	-64	8P038	
-45		5P002	-65	8P039	
-46		5P005	-66	8P035	
-47	8P022		-67	8P040	
-48	8P023		-68	8P041	
-49	8P024		-69	8P042	
-50	8P025		-70	8P043	
-51	8P026		-71	8P044	
-52	8P027		-72	8P045	
-53	8P028		-73		5P018
-54	8P029		-74		5P019
-55		5P017	-75		5P020
-56	8P030		-76	8P046	
-57	8P031		-77	8P047	
-58	8P032		-78	8P048	
-59	8P033		-79		
-60	8P034		-80		

Boot Message from CPROM

As of Rev G on **WINC-Ø5**, a boot 6 character message other then AED> can be stored in the configuration prom. Locations 14-1F in the CPROM (28-3f on the listing) contain one nibble (4 bits) of the ASCII code in Hex for the char to be displayed. If location 14 is non-zero, the message in prom will be used otherwise the standard the AED> will be used. The **WINC-Ø5** micro code automatically places a carriage return and line feed before the user message and a space after it. As an example, to use **WINC-Ø5**:

HEX prom address	14,15	16,17	18,19	1A,1B	1C,1D	1E,1F
HEX char data	5,7	4,9	4,E	4,3	3,Ø	3,5
ASCII char	W	I	N	C	Ø	5

Each prom address is 4 bits wide so 1 ASCII character (2 Hex digits) takes 2 prom locations. To terminate a message in less than 6 characters, load a zero into the 2 prom locations following the last character in your message.

Complex Drives Support

Version 'E' on the **WINC-Ø5/8** board can support complex drives in which one plate can be participate into upto three different logic drives. (Called section 1, section 2, and section 3.) Parameters associated with each section are max cylinder number, base head number and max head number. Parameters for section 1 are stored in CPROM location same as they were before. Parameters for Section 2 and Secton 3 are stored in CPROM location 1A4 to 1F3 (word address) with ten word address for each logic drive. See CPTEST.SRC for an example of complex drive configuration.

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE IN OHMS AND ARE 1/4W UNLESS OTHERWISE SPECIFIED.

2. FOR MODULE MAP SEE SHEET 7. GATES ARE IN ORDER OF OUTPUT PIN NUMBERS AND ARE DEPICTED FROM LEFT TO RIGHT TOP TO BOTTOM ORDER.

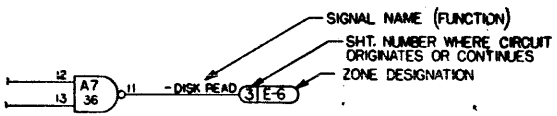
A19	← REF DESIGNATION
7438	← I.C. TYPE
4 | 4	← GATE IS LOCATED ON DESIGNATION SHEET NO.
4 |	← SPARE GATE

3. THE FOLLOWING SYMBOLS DENOTE RESISTOR NETWORK CONFIGURATIONS FOR RN NOS. 1 THRU 10.

T — RN2, 220/330 Ω. PIN 1-GND, PIN 8-Vcc.
RN10, 220/330 Ω. PIN 1-GND, PIN 6-Vcc.

I — RN3 100Ω RN6 2.7K
RN4 470Ω RN7 8.2K
RN5 470Ω RN11 1.5K

C — RN1 1K, RN8 1K, RN9 1K { PIN 1 Vcc }



REF DESIGNATION TABLE		
DESIG	HIGHEST USED	NOT USED
A	A74	——
RN	RN11	——
C	C17	C4
CR	CR5	——
R	R10	R4,5
Q	Q 8	——
Y	Y1	——

PULL UP NET TABLE	
DESIGNATION	RESISTOR
+A	RN8-3
+B	R10

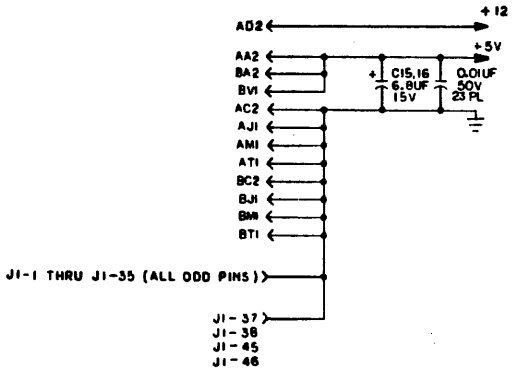
[5] R12 IS PRESELECTED AT 27K OHMS. TEST WILL DETERMINE THAT A8-3 VOLTAGE IS +4.05 VOLTS. VALUE RANGE FOR R12 STARTS AT 20K THRU 70K.

[6] -01 IS CONFIGURED FOR 890063-11.
-02 IS CONFIGURED FOR 890063-12.
-03 IS CONFIGURED FOR 890063-18.
-04 IS CONFIGURED FOR 890063-13.
-05 IS CONFIGURED FOR 890063-26
-06 IS CONFIGURED FOR 890063-20
-07 IS CONFIGURED FOR 890063-27
-08 IS CONFIGURED FOR 890063-02
-09 IS CONFIGURED FOR 890063-09
-10 IS CONFIGURED FOR 890063-12

[7]

	WINC-05	WINC-05/8
A37	890085-01	890073-01
A38	890083-01	890074-01
A39	890084-01	890075-01

[8] ALL VERSION EXCEPT -10 JUMPER E18 TO E19 AND E20 TO E21. VERSION -10 JUMPER E19 TO E20.



REVISIONS			
ISSUE	DESCRIPTION	DATE	APPROVED
A	PROD REL 2384	4/1/84	[illegible]
B	ECO 2394	4/26/84	[illegible]
C	ECO 2397	5/16/84	[illegible]
D	ECO 2399	9/4/84	[illegible]
E	ECO 2470	10/5/84	[illegible]
F	ECO 2492	4/21/85	[illegible]

QTY REQD	PART NUMBER	CAGE IDENT	DESCRIPTION	ITEM NO.
PARTS LIST				

TOLERANCE UNLESS OTHERWISE SPECIFIED
FRACTIONS ±
.XX ± .1
.XXX ± .1
ANGULAR
SURFACE
SCALE

MATERIAL
FINISH

DRAWN: B SUIT 3/18/83
CHK'D:
APP'D:
MFG:

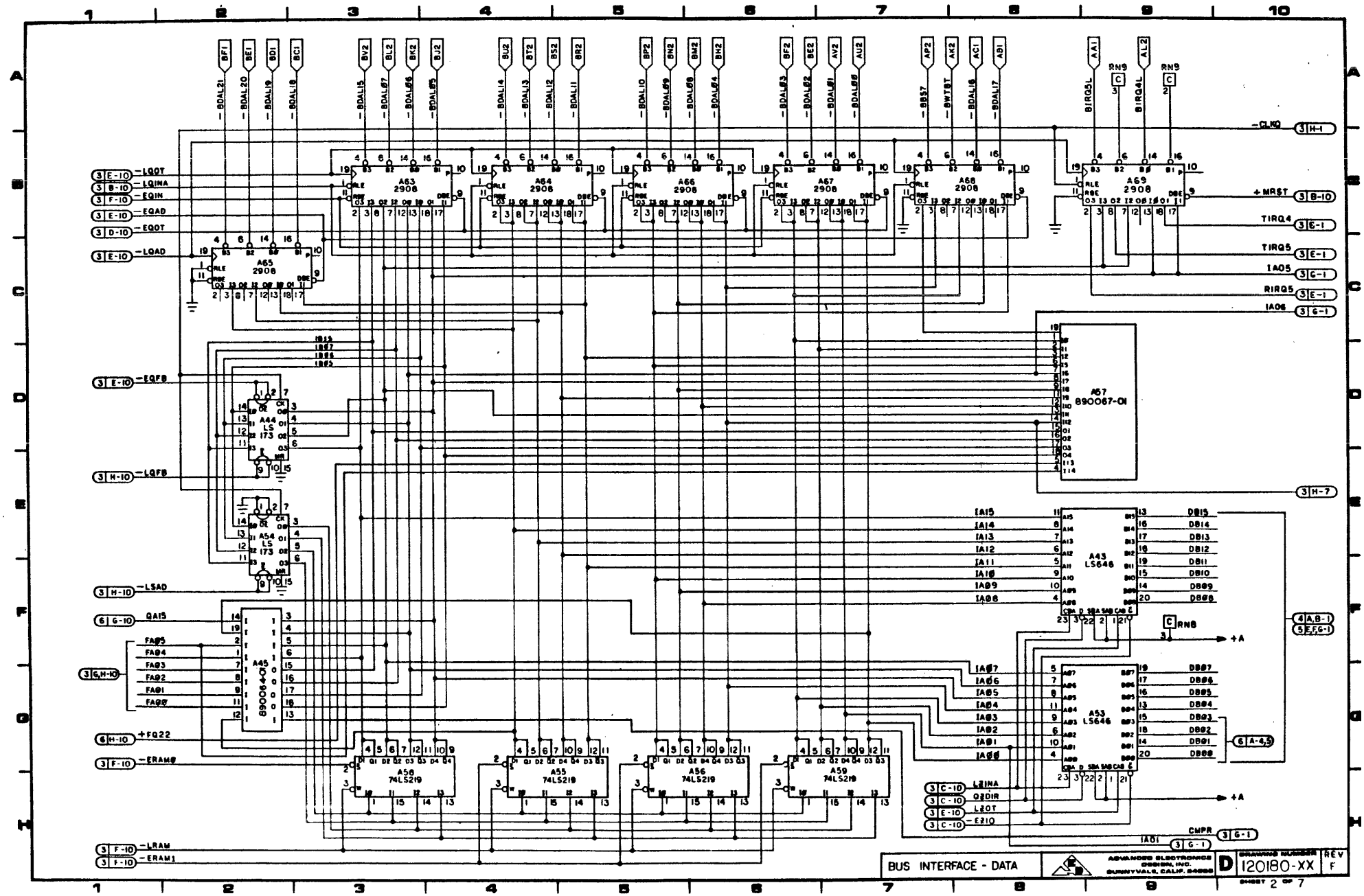
DRAWING TITLE: SCHEMATIC, WINC-05/8, WINC-05

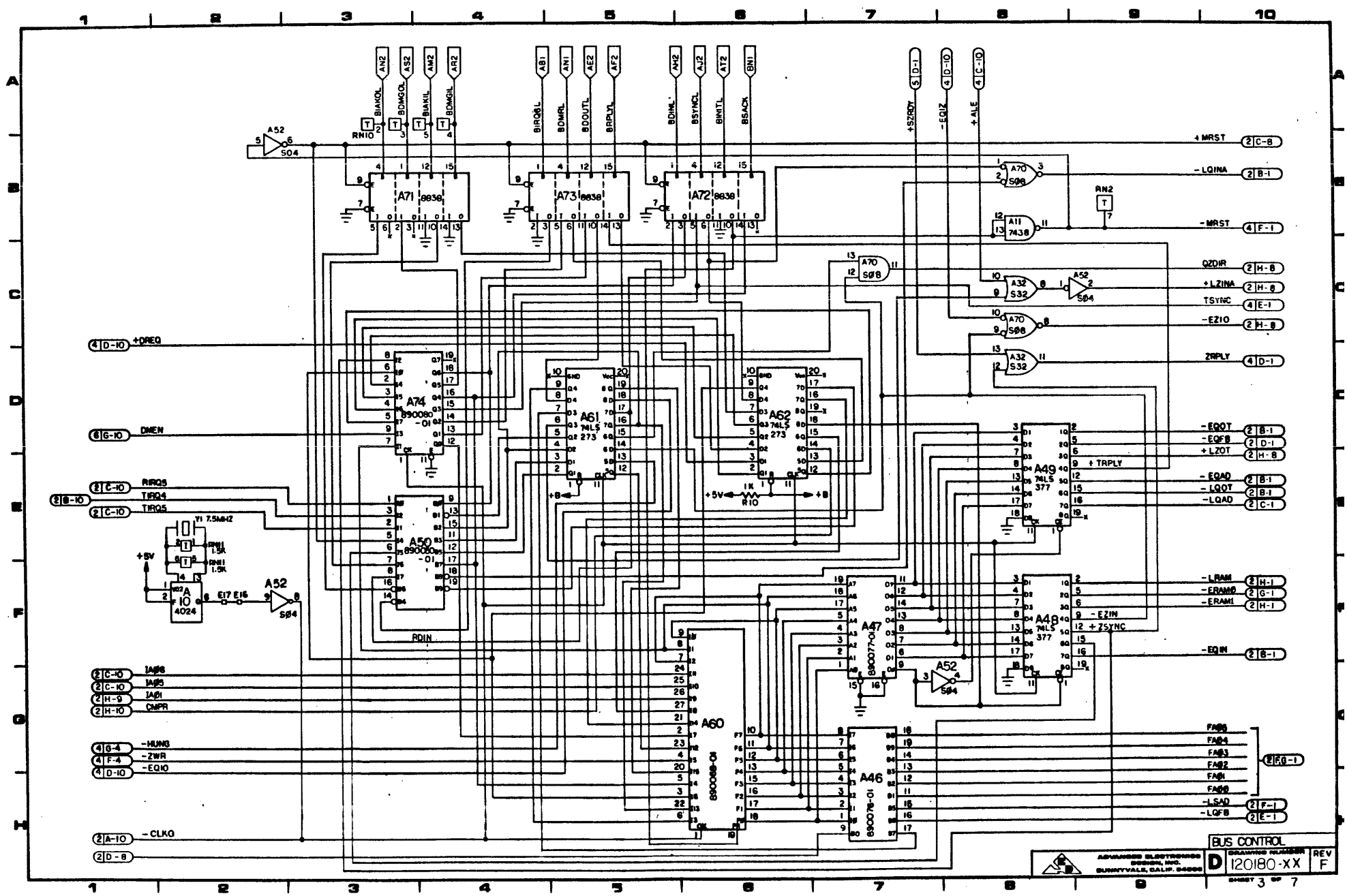
DASH NO.	NEXT ASSY	USED ON
XX	120179-XX	WINC-05/8
APPLICATION		

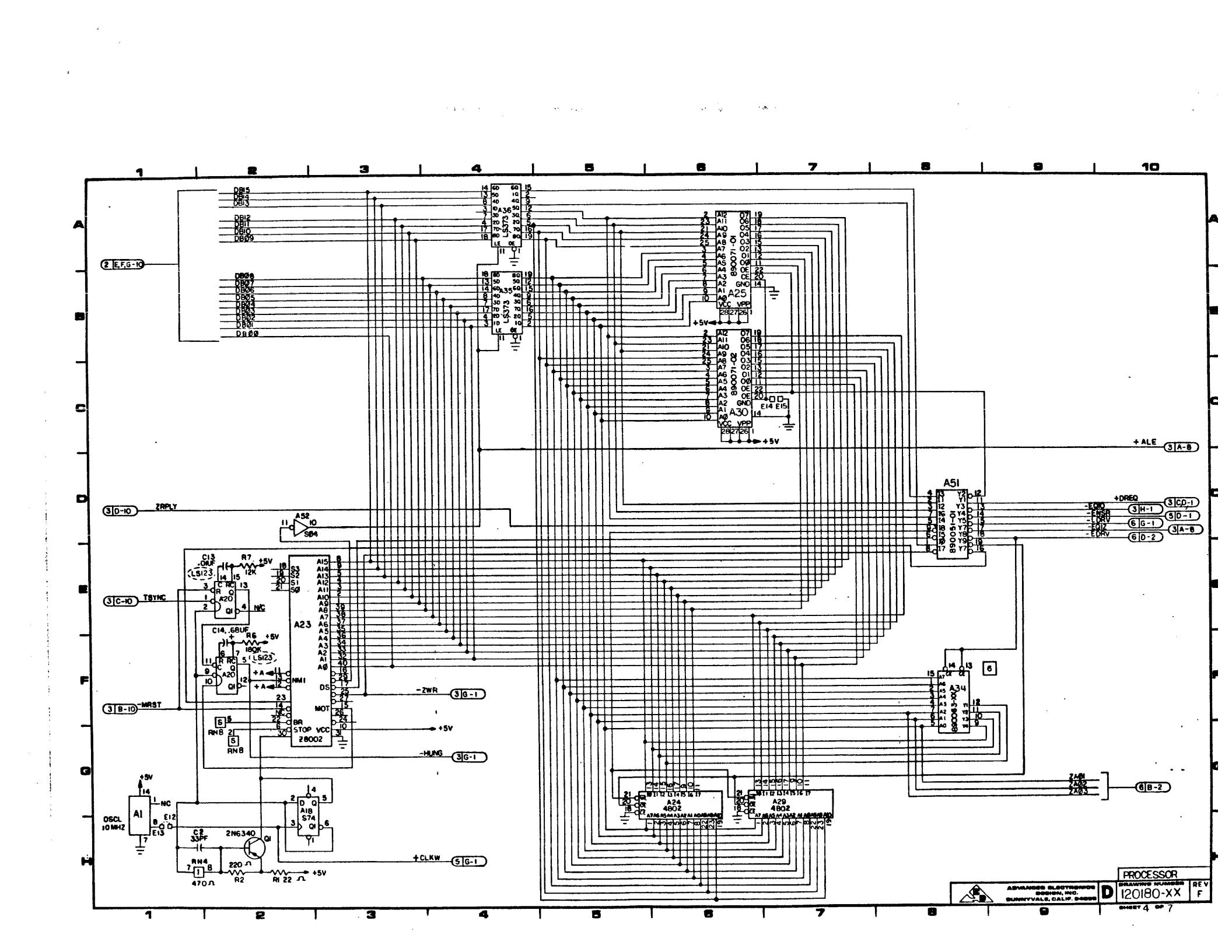
ADVANCED ELECTRONICS DESIGN, INC. SUNNYVALE, CALIF. 94086

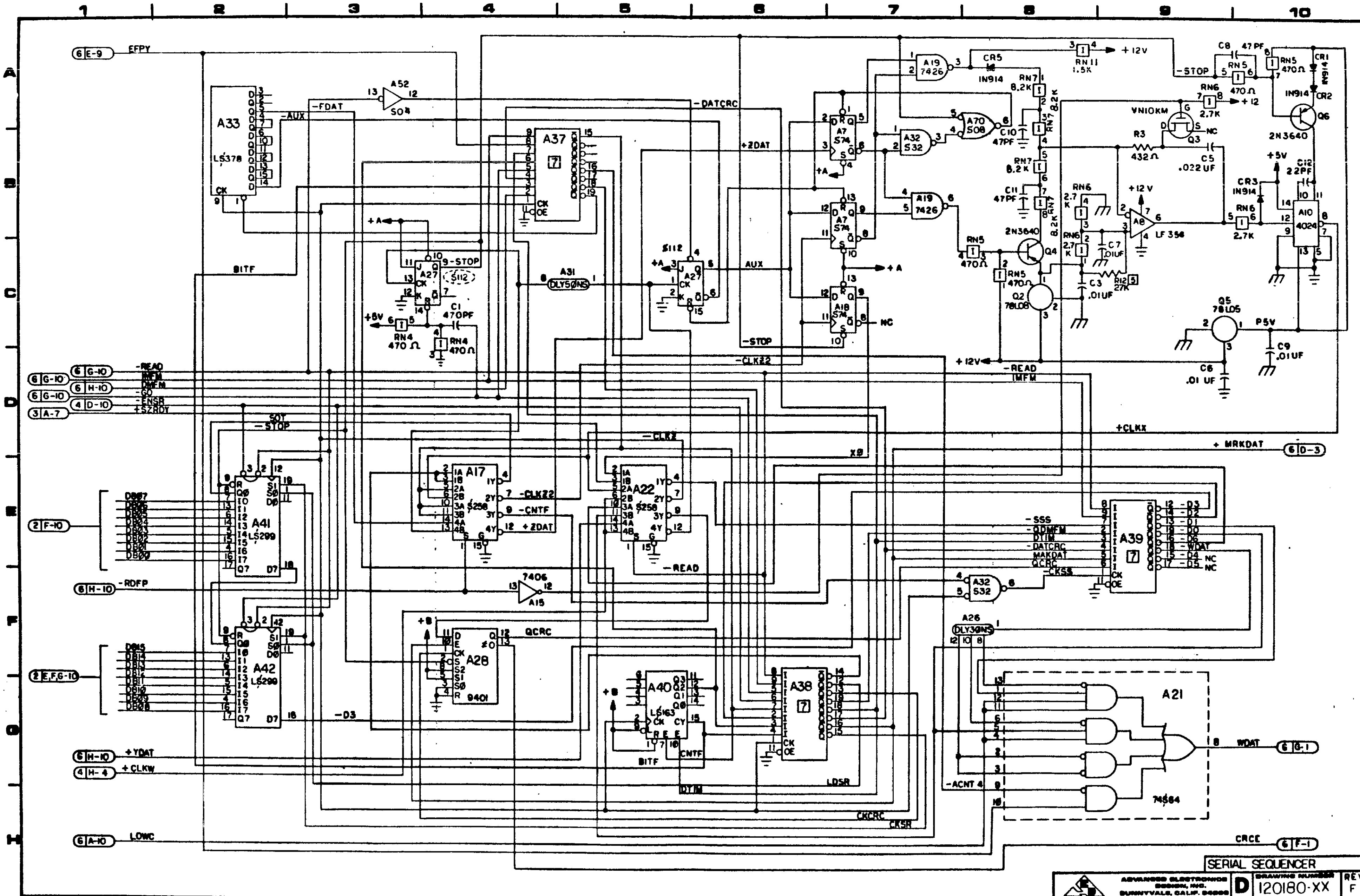
SIZE D | DRAWING NUMBER 120180-XX | REV F

SHEET 1 OF 7


BUS INTERFACE - DATA
ADVANCED ELECTRONICS DESIGN, INC. SUNNYVALE, CALIF. 94086
D
120180-XX
REV F
SHEET 2 OF 7


BUS CONTROL
D
120180-XX
REV F
SHEET 3 OF 7
A71 8838
A73 8838
A72 8838
A74 890080-01
A61 74LS 273
A62 74LS 273
A50 890050-01
A60 890068-01
A47 890077-01
A46 890078-01
A48 74LS 377
A49 74LS 377
A52 S04
A70 S08
A11 7438
A32 S32
A10 4024
RN10
RN11 1.5K
RN12 1.5K
RN2
R10 1K
Y1 7.5MHZ
+5V
+8
RDIN
BIAKOL
BOMGOL
BIAKIL
BOMGIL
BIRQ6L
BOMRL
BDOUTL
BRPLYL
BDINL
BSYNCL
BINTL
BSACK
+SZRDY
-EQIZ
+ALE
+MRST
-LQINA
-MRST
QZDIR
+LZINA
TSYNC
-EZIO
ZRPLY
+DREQ
DMEN
RIRQ5
TIRQ4
TIRQ5
IAØ6
IAØ5
IAØ1
CMPR
-HUNG
-ZWR
-EQIO
-CLKQ
-EQOT
-EQFB
+LZOT
+TRPLY
-EQAD
-LQOT
-LQAD
-LRAM
-ERAMØ
-ERAM1
-EZIN
+ZSYNC
-EQIN
FAØ5
FAØ4
FAØ3
FAØ2
FAØ1
FAØØ
-LSAD
-LQFB
ADVANCED ELECTRONICS DESIGN, INC. SUNNYVALE, CALIF. 94086


PROCESSOR
DRAWING NUMBER
120180-XX
REV
F
SHEET 4 OF 7
ADVANCED ELECTRONICS DESIGN, INC. SUNNYVALE, CALIF. 94086
+ALE
+DREQ
ZRPLY
TSYNC
MRST
-ZWR
-HLNG
+CLKW
+5V
OSCL 10 MHZ
2N6340
A23
A24
A25
A29
A30
A34
A51
A52
A35
A36
LS373
LS123
S04
S74
28002
4802
89C071-01
89C071-02
89C071-03
89C071-04
89C071-05
89C071-06
89C071-07
89C071-08
89C071-09
89C071-10
89C071-11
89C071-12
89C071-13
89C071-14
89C071-15
89C071-16
89C071-17
89C071-18
89C071-19
89C071-20
89C071-21
89C071-22
89C071-23
89C071-24
89C071-25
89C071-26
89C071-27
89C071-28
89C071-29
89C071-30
89C071-31
89C071-32
89C071-33
89C071-34
89C071-35
89C071-36
89C071-37
89C071-38
89C071-39
89C071-40
89C071-41
89C071-42
89C071-43
89C071-44
89C071-45
89C071-46
89C071-47
89C071-48
89C071-49
89C071-50
89C071-51
89C071-52
89C071-53
89C071-54
89C071-55
89C071-56
89C071-57
89C071-58
89C071-59
89C071-60
89C071-61
89C071-62
89C071-63
89C071-64
89C071-65
89C071-66
89C071-67
89C071-68
89C071-69
89C071-70
89C071-71
89C071-72
89C071-73
89C071-74
89C071-75
89C071-76
89C071-77
89C071-78
89C071-79
89C071-80
89C071-81
89C071-82
89C071-83
89C071-84
89C071-85
89C071-86
89C071-87
89C071-88
89C071-89
89C071-90
89C071-91
89C071-92
89C071-93
89C071-94
89C071-95
89C071-96
89C071-97
89C071-98
89C071-99
89C071-100
89C071-101
89C071-102
89C071-103
89C071-104
89C071-105
89C071-106
89C071-107
89C071-108
89C071-109
89C071-110
89C071-111
89C071-112
89C071-113
89C071-114
89C071-115
89C071-116
89C071-117
89C071-118
89C071-119
89C071-120
89C071-121
89C071-122
89C071-123
89C071-124
89C071-125
89C071-126
89C071-127
89C071-128
89C071-129
89C071-130
89C071-131
89C071-132
89C071-133
89C071-134
89C071-135
89C071-136
89C071-137
89C071-138
89C071-139
89C071-140
89C071-141
89C071-142
89C071-143
89C071-144
89C071-145
89C071-146
89C071-147
89C071-148
89C071-149
89C071-150
89C071-151
89C071-152
89C071-153
89C071-154
89C071-155
89C071-156
89C071-157
89C071-158
89C071-159
89C071-160
89C071-161
89C071-162
89C071-163
89C071-164
89C071-165
89C071-166
89C071-167
89C071-168
89C071-169
89C071-170
89C071-171
89C071-172
89C071-173
89C071-174
89C071-175
89C071-176
89C071-177
89C071-178
89C071-179
89C071-180
89C071-181
89C071-182
89C071-183
89C071-184
89C071-185
89C071-186
89C071-187
89C071-188
89C071-189
89C071-190
89C071-191
89C071-192
89C071-193
89C071-194
89C071-195
89C071-196
89C071-197
89C071-198
89C071-199
89C071-200
89C071-201
89C071-202
89C071-203
89C071-204
89C071-205
89C071-206
89C071-207
89C071-208
89C071-209
89C071-210
89C071-211
89C071-212
89C071-213
89C071-214
89C071-215
89C071-216
89C071-217
89C071-218
89C071-219
89C071-220
89C071-221
89C071-222
89C071-223
89C071-224
89C071-225
89C071-226
89C071-227
89C071-228
89C071-229
89C071-230
89C071-231
89C071-232
89C071-233
89C071-234
89C071-235
89C071-236
89C071-237
89C071-238
89C071-239
89C071-240
89C071-241
89C071-242
89C071-243
89C071-244
89C071-245
89C071-246
89C071-247
89C071-248
89C071-249
89C071-250
89C071-251
89C071-252
89C071-253
89C071-254
89C071-255
89C071-256
89C071-257
89C071-258
89C071-259
89C071-260
89C071-261
89C071-262
89C071-263
89C071-264
89C071-265
89C071-266
89C071-267
89C071-268
89C071-269
89C071-270
89C071-271
89C071-272
89C071-273
89C071-274
89C071-275
89C071-276
89C071-277
89C071-278
89C071-279
89C071-280
89C071-281
89C071-282
89C071-283
89C071-284
89C071-285
89C071-286
89C071-287
89C071-288
89C071-289
89C071-290
89C071-291
89C071-292
89C071-293
89C071-294
89C071-295
89C071-296
89C071-297
89C071-298
89C071-299
89C071-300
89C071-301
89C071-302
89C071-303
89C071-304
89C071-305
89C071-306
89C071-307
89C071-308
89C071-309
89C071-310
89C071-311
89C071-312
89C071-313
89C071-314
89C071-315
89C071-316
89C071-317
89C071-318
89C071-319
89C071-320
89C071-321
89C071-322
89C071-323
89C071-324
89C071-325
89C071-326
89C071-327
89C071-328
89C071-329
89C071-330
89C071-331
89C071-332
89C071-333
89C071-334
89C071-335
89C071-336
89C071-337
89C071-338
89C071-339
89C071-340
89C071-341
89C071-342
89C071-343
89C071-344
89C071-345
89C071-346
89C071-347
89C071-348
89C071-349
89C071-350
89C071-351
89C071-352
89C071-353
89C071-354
89C071-355
89C071-356
89C071-357
89C071-358
89C071-359
89C071-360
89C071-361
89C071-362
89C071-363
89C071-364
89C071-365
89C071-366
89C071-367
89C071-368
89C071-369
89C071-370
89C071-371
89C071-372
89C071-373
89C071-374
89C071-375
89C071-376
89C071-377
89C071-378
89C071-379
89C071-380
89C071-381
89C071-382
89C071-383
89C071-384
89C071-385
89C071-386
89C071-387
89C071-388
89C071-389
89C071-390
89C071-391
89C071-392
89C071-393
89C071-394
89C071-395
89C071-396
89C071-397
89C071-398
89C071-399
89C071-400
89C071-401
89C071-402
89C071-403
89C071-404
89C071-405
89C071-406
89C071-407
89C071-408
89C071-409
89C071-410
89C071-411
89C071-412
89C071-413
89C071-414
89C071-415
89C071-416
89C071-417
89C071-418
89C071-419
89C071-420
89C071-421
89C071-422
89C071-423
89C071-424
89C071-425
89C071-426
89C071-427
89C071-428
89C071-429
89C071-430
89C071-431
89C071-432
89C071-433
89C071-434
89C071-435
89C071-436
89C071-437
89C071-438
89C071-439
89C071-440
89C071-441
89C071-442
89C071-443
89C071-444
89C071-445
89C071-446
89C071-447
89C071-448
89C071-449
89C071-450
89C071-451
89C071-452
89C071-453
89C071-454
89C071-455
89C071-456
89C071-457
89C071-458
89C071-459
89C071-460
89C071-461
89C071-462
89C071-463
89C071-464
89C071-465
89C071-466
89C071-467
89C071-468
89C071-469
89C071-470
89C071-471
89C071-472
89C071-473
89C071-474
89C071-475
89C071-476
89C071-477
89C071-478
89C071-479
89C071-480
89C071-481
89C071-482
89C071-483
89C071-484
89C071-485
89C071-486
89C071-487
89C071-488
89C071-489
89C071-490
89C071-491
89C071-492
89C071-493
89C071-494
89C071-495
89C071-496
89C071-497
89C071-498
89C071-499
89C071-500
89C071-501
89C071-502
89C071-503
89C071-504
89C071-505
89C071-506
89C071-507
89C071-508
89C071-509
89C071-510
89C071-511
89C071-512
89C071-513
89C071-514
89C071-515
89C071-516
89C071-517
89C071-518
89C071-519
89C071-520
89C071-521
89C071-522
89C071-523
89C071-524
89C071-525
89C071-526
89C071-527
89C071-528
89C071-529
89C071-530
89C071-531
89C071-532
89C071-533
89C071-534
89C071-535
89C071-536
89C071-537
89C071-538
89C071-539
89C071-540
89C071-541
89C071-542
89C071-543
89C071-544
89C071-545
89C071-546
89C071-547
89C071-548
89C071-549
89C071-550
89C071-551
89C071-552
89C071-553
89C071-554
89C071-555
89C071-556
89C071-557
89C071-558
89C071-559
89C071-560
89C071-561
89C071-562
89C071-563
89C071-564
89C071-565
89C071-566
89C071-567
89C071-568
89C071-569
89C071-570
89C071-571
89C071-572
89C071-573
89C071-574
89C071-575
89C071-576
89C071-577
89C071-578
89C071-579
89C071-580
89C071-581
89C071-582
89C071-583
89C071-584
89C071-585
89C071-586
89C071-587
89C071-588
89C071-589
89C071-590
89C071-591
89C071-592
89C071-593
89C071-594
89C071-595
89C071-596
89C071-597
89C071-598
89C071-599
89C071-600
89C071-601
89C071-602
89C071-603
89C071-604
89C071-605
89C071-606
89C071-607
89C071-608
89C071-609
89C071-610
89C071-611
89C071-612
89C071-613
89C071-614
89C071-615
89C071-616
89C071-617
89C071-618
89C071-619
89C071-620
89C071-621
89C071-622
89C071-623
89C071-624
89C071-625
89C071-626
89C071-627
89C071-628
89C071-629
89C071-630
89C071-631
89C071-632
89C071-633
89C071-634
89C071-635
89C071-636
89C071-637
89C071-638
89C071-639
89C071-640
89C071-641
89C071-642
89C071-643
89C071-644
89C071-645
89C071-646
89C071-647
89C071-648
89C071-649
89C071-650
89C071-651
89C071-652
89C071-653
89C071-654
89C071-655
89C071-656
89C071-657
89C071-658
89C071-659
89C071-660
89C071-661
89C071-662
89C071-663
89C071-664
89C071-665
89C071-666
89C071-667
89C071-668
89C071-669
89C071-670
89C071-671
89C071-672
89C071-673
89C071-674
89C071-675
89C071-676
89C071-677
89C071-678
89C071-679
89C071-680
89C071-681
89C071-682
89C071-683
89C071-684
89C071-685
89C071-686
89C071-687
89C071-688
89C071-689
89C071-690
89C071-691
89C071-692
89C071-693
89C071-694
89C071-695
89C071-696
89C071-697
89C071-698
89C071-699
89C071-700
89C071-701
89C071-702
89C071-703
89C071-704
89C071-705
89C071-706
89C071-707
89C071-708
89C071-709
89C071-710
89C071-711
89C071-712
89C071-713
89C071-714
89C071-715
89C071-716
89C071-717
89C071-718
89C071-719
89C071-720
89C071-721
89C071-722
89C071-723
89C071-724
89C071-725
89C071-726
89C071-727
89C071-728
89C071-729
89C071-730
89C071-731
89C071-732
89C071-733
89C071-734
89C071-735
89C071-736
89C071-737
89C071-738
89C071-739
89C071-740
89C071-741
89C071-742
89C071-743
89C071-744
89C071-745
89C071-746
89C071-747
89C071-748
89C071-749
89C071-750
89C071-751
89C071-752
89C071-753
89C071-754
89C071-755
89C071-756
89C071-757
89C071-758
89C071-759
89C071-760
89C071-761
89C071-762
89C071-763
89C071-764
89C071-765
89C071-766
89C071-767
89C071-768
89C071-769
89C071-770
89C071-771
89C071-772
89C071-773
89C071-774
89C071-775
89C071-776
89C071-777
89C071-778
89C071-779
89C071-780
89C071-781
89C071-782
89C071-783
89C071-784
89C071-785
89C071-786
89C071-787
89C071-788
89C071-789
89C071-790
89C071-791
89C071-792
89C071-793
89C071-794
89C071-795
89C071-796
89C071-797
89C071-798
89C071-799
89C071-800
89C071-801
89C071-802
89C071-803
89C071-804
89C071-805
89C071-806
89C071-807
89C071-808
89C071-809
89C071-810
89C071-811
89C071-812
89C071-813
89C071-814
89C071-815
89C071-816
89C071-817
89C071-818
89C071-819
89C071-820
89C071-821
89C071-822
89C071-823
89C071-824
89C071-825
89C071-826
89C071-827
89C071-828
89C071-829
89C071-830
89C071-831
89C071-832
89C071-833
89C071-834
89C071-835
89C071-836
89C071-837
89C071-838
89C071-839
89C071-840
89C071-841
89C071-842
89C071-843
89C071-844
89C071-845
89C071-846
89C071-847
89C071-848
89C071-849
89C071-850
89C071-851
89C071-852
89C071-853
89C071-854
89C071-855
89C071-856
89C071-857
89C071-858
89C071-859
89C071-860
89C071-861
89C071-862
89C071-863
89C071-864
89C071-865
89C071-866
89C071-867
89C071-868
89C071-869
89C071-870
89C071-871
89C071-872
89C071-873
89C071-874
89C071-875
89C071-876
89C071-877
89C071-878
89C071-879
89C071-880
89C071-881
89C071-882
89C071-883
89C071-884
89C071-885
89C071-886
89C071-887
89C071-888
89C071-889
89C071-890
89C071-891
89C071-892
89C071-893
89C071-894
89C071-895
89C071-896
89C071-897
89C071-898
89C071-899
89C071-900
89C071-901
89C071-902
89C071-903
89C071-904
89C071-905
89C071-906
89C071-907
89C071-908
89C071-909
89C071-910
89C071-911
89C071-912
89C071-913
89C071-914
89C071-915
89C071-916
89C071-917
89C071-918
89C071-919
89C071-920
89C071-921
89C071-922
89C071-923
89C071-924
89C071-925
89C071-926
89C071-927
89C071-928
89C071-929
89C071-930
89C071-931
89C071-932
89C071-933
89C071-934
89C071-935
89C071-936
89C071-937
89C071-938
89C071-939
89C071-940
89C071-941
89C071-942
89C071-943
89C071-944
89C071-945
89C071-946
89C071-947
89C071-948
89C071-949
89C071-950
89C071-951
89C071-952
89C071-953
89C071-954
89C071-955
89C071-956
89C071-957
89C071-958
89C071-959
89C071-960
89C071-961
89C071-962
89C071-963
89C071-964
89C071-965
89C071-966
89C071-967
89C071-968
89C071-969
89C071-970
89C071-971
89C071-972
89C071-973
89C071-974
89C071-975
89C071-976
89C071-977
89C071-978
89C071-979
89C071-980
89C071-981
89C071-982
89C071-983
89C071-984
89C071-985
89C071-986
89C071-987
89C071-988
89C071-989
89C071-990
89C071-991
89C071-992
89C071-993
89C071-994
89C071-995
89C071-996
89C071-997
89C071-998
89C071-999
89C071-1000

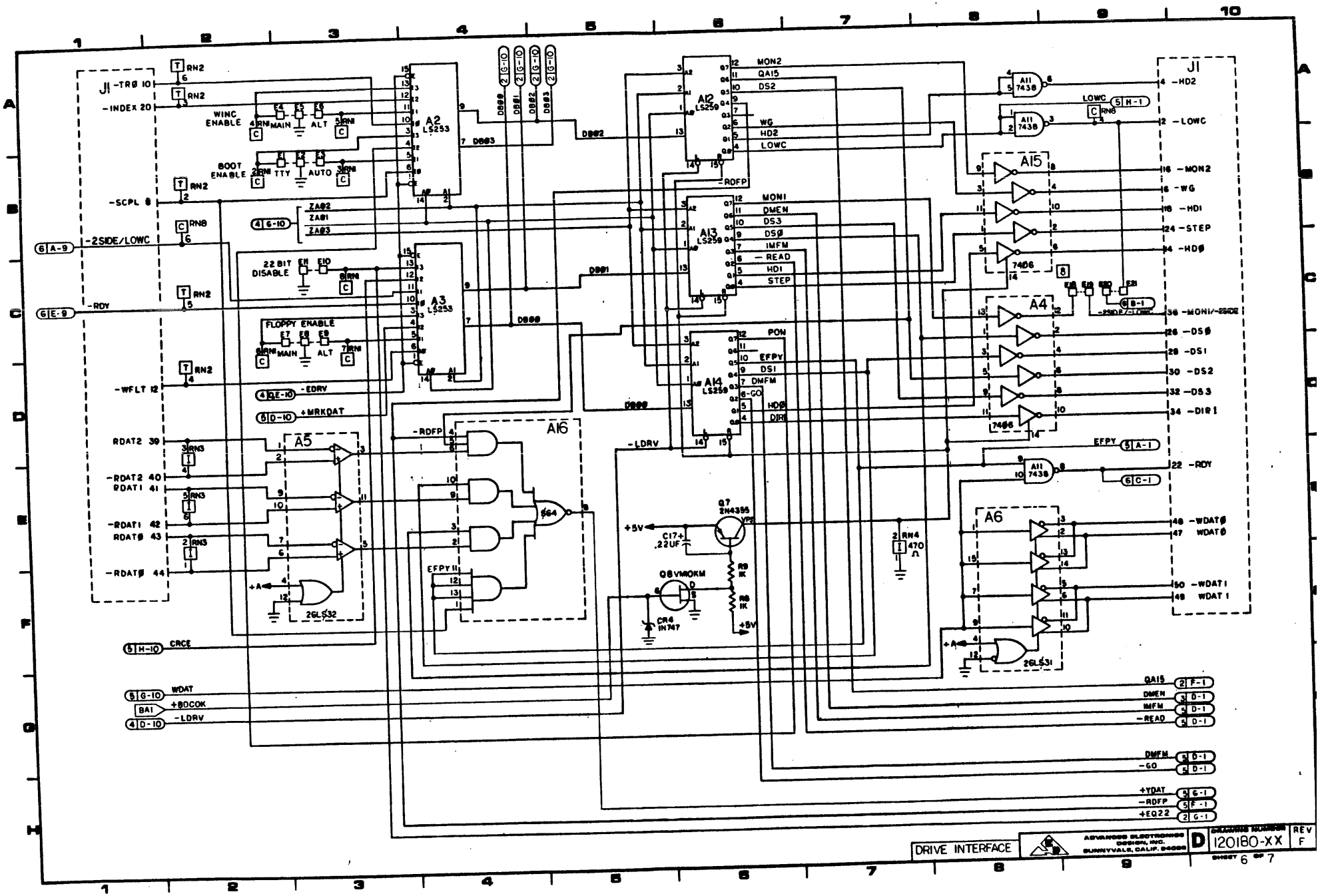


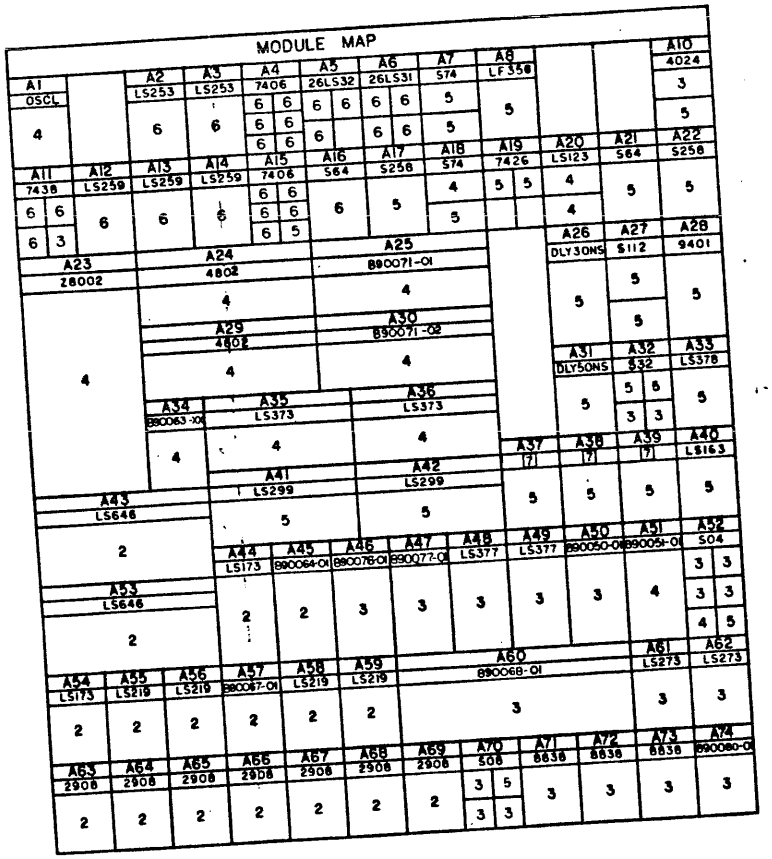
SERIAL SEQUENCER

ADVANCED ELECTRONICS DESIGN, INC.
SUNNYVALE, CALIF.

D | DRAWING NUMBER 120180-XX | REV F

SHEET 5 OF 7


DRIVE INTERFACE
ADVANCED ELECTRONICS DESIGN, INC. SUNNYVALE, CALIF. 94086
D
DRAWING NUMBER 120180-XX
REV F
SHEET 6 OF 7
J1
A2 LS253
A3 LS253
A12 LS259
A13 LS259
A14 LS259
A15
A16
A4
A5
A6
A11 7438
7406
2GLS32
2GLS31
Q7 2N4355
Q8 VM10KM
CR4 IN747
C17 .22UF
R9 1K
R8 1K
2 RN4 470Ω
-TRØ 10
-INDEX 20
-SCPL 8
-2SIDE/LOWC
-RDY
-WFLT 12
RDAT2 39
-RDAT2 40
RDAT1 41
-RDAT1 42
RDATØ 43
-RDATØ 44
WINC ENABLE
BOOT ENABLE
TTY
AUTO
MAIN
ALT
22 BIT DISABLE
FLOPPY ENABLE
ZA02
ZA01
ZA03
-EDRV
+MRKDAT
-RDFP
-LDRV
EFPY 11
+5V
+A
CRCE
WDAT
+BDCOK
MON2
QA15
DS2
WG
HD2
LOWC
MONI
DMEN
DS3
DSØ
IMFM
-READ
HDI
STEP
PON
EFPY
DSI
DMFM
-GO
HDØ
DIR
-HD2
-LOWC
-MON2
-WG
-HDI
-STEP
-HDØ
-MONI/-2SIDE
-DSØ
-DS1
-DS2
-DS3
-DIR1
-RDY
-WDATØ
WDATØ
-WDAT1
WDAT1
QA15
DMEN
IMFM
-READ
DMFM
-GO
+YDAT
-RDFP
+EQ22


MODULE MAP
A1 OSCL 4
A2 LS253 6
A3 LS253 6
A4 7406 6 6 6 6 6 6
A5 26LS32 6 6 6
A6 26LS31 6 6 6 6
A7 S74 5 5
A8 LF356 5
A10 4024 3 5
A11 7438 6 6 6 3
A12 LS259 6
A13 LS259 6
A14 LS259 6
A15 7406 6 6 6 6 6 5
A16 S64 6
A17 S258 5
A18 S74 4 5
A19 7426 5 5
A20 LS123 4 4
A21 S64 5
A22 S258 5
A23 Z8002 4
A24 4802 4
A25 890071-01 4
A26 DLY30NS 5
A27 S112 5 5
A28 9401 5
A29 4802 4
A30 890071-02 4
A31 DLY50NS 5
A32 S32 5 5 3 3
A33 LS378 5
A34 890063-XX 4
A35 LS373 4
A36 LS373 4
A37 [?] 5
A38 [?] 5
A39 [?] 5
A40 LS163 5
A41 LS299 5
A42 LS299 5
A43 LS646 2
A44 LS173 2
A45 890064-01 2
A46 890076-01 3
A47 890077-01 3
A48 LS377 3
A49 LS377 3
A50 890050-01 3
A51 890054-01 4
A52 S04 3 3 3 3 4 5
A53 LS646 2
A54 LS173 2
A55 LS219 2
A56 LS219 2
A57 890067-01 2
A58 LS219 2
A59 LS219 2
A60 890068-01 3
A61 LS273 3
A62 LS273 3
A63 2908 2
A64 2908 2
A65 2908 2
A66 2908 2
A67 2908 2
A68 2908 2
A69 2908 2
A70 S08 3 5 3 3
A71 8838 3
A72 8838 3
A73 8838 3
A74 890080-01 3