AHA-1540C Series

High-Performance Bus Master
ISA to SCSI Host Adapters

Technical Reference Manual

adaptec

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Technical Reference Manual

Including
AHA-1540C/1542C and
AHA-1540CF/1542CF

adaptec

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Adaptec, Inc.
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Milpitas, CA 95035

FCC Compliance Statement

NOTE: This equipment was tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference in residential installations. This equipment generates, uses, and can radiate radio frequency energy, and if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation.

If this equipment does cause interference to radio or television equipment reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna
- Move the equipment away from the receiver
- Plug the equipment into an outlet on a circuit different from that to which the receiver is powered
- If necessary, the user should consult the dealer or an experienced radio/television technician for additional suggestions

CAUTION: Only equipment certified to comply with Class B (computer input/output devices, terminals, printers, etc.) should be attached to this equipment, and must have shielded interface cables.

Finally, any change or modifications to the equipment by the user not expressly approved by the grantee or manufacturer could void the user's authority to operate such equipment.

Each AHA-1540C Series host adapter is equipped with an FCC compliance label which shows only the FCC Identification number. The full text of the associated label follows:

This device complies with part 15 of the FCC rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference and (2) this device must accept any interference received, including interference that may cause undesired operation.

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Preface

This Technical Reference Manual provides technical information for Adaptec's AHA-1540C Series ISA-to-SCSI host adapters. It is prepared for customer technical personnel requiring detailed information on the operation of the board at a register and command protocol level. Documentation of board schematics, integrated circuits, microcode and BIOS routines is not provided.

Programmers writing device drivers for specific peripherals are strongly advised to use the Advanced SCSI Programming Interface (ASPI) specification appropriate to the operating system chosen. This will allow flexibility across all boards complying with ASPI Manager modules and prevent obsolescence. Please contact Adaptec Corporate Communications for copies of ASPI specifications. Software managers are documented and sold separately.

The AHA-1540C Series host adapters described in this Technical Reference Manual include:

- The AHA-1540C and AHA-1542C host adapters, jointly referred to as the AHA-1540C/1542C host adapter
- The AHA-1540CF and AHA-1542CF, likewise referred to as the AHA-1540CF/1542CF host adapter

References to the AHA-1540C Series host adapter, or adapters, apply to both the AHA-1540C/1542C and AHA-1540CF/1542CF. Features particular to specific models are clearly mentioned where appropriate.

Conventions

The following typographic conventions are used throughout this Technical Reference Manual.

bold
Used for keystrokes (.. press the **Enter** key ..) and screen selection fields (.. select **Backup Device** and ..).

Helvetica
Used for operator entry that must be typed exactly as shown
(.. device=c:\cdrom\cdrom.tsd ..) and for screen messages (.. Enter Password ..).

Helvetica Italics
Used as a place holder for text you must determine and type in (.. enter *nn* for number ..).
Also used for program and file names in body text (.. the *autoexec.bat* file ..).

Italics
Used for emphasis (.. is *only* supported ..) and document reference (.. refer to Chapter Three, *Installation* ..).

ALL CAPITALS
Used for acronyms (..the SCSI device..).

Hexadecimal numbers are followed with an 'h', e.g., 330h.

The ❒ symbol marks the end of text for each chapter.

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Chapter One

Introduction

Document Scope

This manual provides the information required to program the Adaptec AHA-1540C Series Intelligent Host Adapters in ISA bus-based systems.

Product Overview

The AHA-1540C Series provides a powerful multitasking interface between the Industry Standard Architecture (ISA) bus and the Small Computer System Interface (SCSI) bus. The AHA-1540C Series are high-performance intelligent host adapters supporting a maximum asynchronous SCSI rate of 2.0 MBytes/second and synchronous transfer rates of 5 to 10 MBytes/second. The AHA-1540C Series supports multithreaded I/O operations, allowing simultaneous operations on multiple targets/LUNs. Disconnect/Reconnect support maximizes bus utilization for multiple target systems. Target Mode operation allows AHA-1540C Series host adapters to receive information from other host adapters. Scatter Gather allows high performance even in systems with fragmented memory buffers.

The Adaptec AHA-1540C Series provides a solution for system applications requiring very high performance, configuration flexibility, multithreaded I/O capability and system redundancy. The Adaptec BIOS also allows an AHA-1540C Series host adapter to be used in place of a standard fixed disk controller. The AHA-1540C and AHA-1540CF host adapters provide only the high-performance host adapter circuitry. The AHA-1542C and AHA-1542CF host adapters provide identical host adapter circuitry, but add an IBM-compatible floppy disk drive controller to the circuit board. The AHA-1540CF/1542CF host adapter provides Fast SCSI support, Floptical diskette drive support, and the AHA-1542CF provides support for an alternate floppy diskette controller I/O address.

AHA-1540C Series Family Product Features

The following are standard features for the AHA-1540C Series host adapters:

- High performance bus master DMA with selectable or programmable data rates of up to 10 MBytes/second
- Built-in SCSI*Select*™ BIOS configuration software utility
- Maximum synchronous SCSI bus transfer rate of 5.0 MBytes/second on the AHA-1540C/1542C and 10.0 MBytes/second on the AHA-1540CF/1542CF with Fast SCSI Support enabled

- Adaptec BIOS for standard fixed disk emulation
- Scatter Gather (supports up to 255 segments)
- Floptical diskette drive support on the AHA-1540CF/1542CF
- Asynchronous and synchronous peripherals supported simultaneously
- Provision for programmable AT bus burst transfer on and off time via device drivers
- Configurable DMA channel for bus arbitration (channels 0, 5, 6, 7)
- Configurable interrupt channels (IRQ 9, 10, 11, 12, 14, 15)
- True multithreaded operation supporting up to 255 tasks simultaneously
- Programmable mailbox architecture
- Switch-selectable I/O port address
- Internal and external SCSI connectors
- Initiator and Target Modes of operation fully supported
- On-board floppy disk drive controller (AHA-1542C and AHA-1542CF only)

Product Specifications

Physical Dimensions	Length	Width	Height
AHA-1540C/1542C	7.0 inches	.625 inches	4.5 inches
AHA-1540CF/1542CF	6.3 inches	.625 inches	4.5 inches
Standard ISA-compatible form factor			
Power Requirements			
+5.0 +/- 0.25 Volts at 0.51 Amps not including bus termination power			
Fuse Type: (AHA-1540C/1542C only)			
1.5 Amp, 125 Volt			
Environmental Requirements			
Temperature 0 to 55 °C (operating) -40 to 75 °C (storage)			
Reliability Information			
Mean Time Between Failures: (calculated per Mil Handbook 217E, ground benign, 40° C)			
AHA-1540C	101,637 hours	AHA-1540CF	137,399 hours
AHA-1542C	96,612 hours	AHA-1542CF	121,146 hours
Mean Time Between Failures: (calculated per Bellcore specification TRNWT000332)			
AHA-1540CF	333,200 hours	AHA-1542CF	530,786 hours

SCSI Interface

Electrical

The electrical interface conforms to the *American National Standard for information systems - Small Computer Systems Interface (SCSI),* ANSI X3.131 for single-ended operation.

Output Signals

All signals use open collector or three-state drivers. Each signal driven by a SCSI device has the following output characteristics when measured at the SCSI device's connector:

Signal	Definition	Characteristics
V_{OL}	Low-level output voltage	0.0 to 0.5 volts DC at 48 mA sinking (signal assertion)
V_{OH}	High-level output voltage	2.5 to 5.25 volts DC (signal negation)

Input Signal

SCSI inputs meet the following electrical characteristics on each signal (including both receivers and passive drivers):

Signal	Definition	Characteristics
V_{IL}	Low-level input voltage	0.0 to 0.8 volts DC (signal true)
V_{IH}	High-level input voltage	2.0 to 5.25 volts DC (signal false)
I_{IL}	Low-level input current	-0.4 to 0.0 mA at V_I = 0.5 volts DC
I_{IH}	High-level input current	0.0 to 0.1 mA at V_I = 2.7 volts DC
Minimum input hysteresis = 0.2 volts DC Maximum input capacitance = 25 pF (measured at the device connector closest to the stub, if any, within the device)		

Internal Connector

Unshrouded 50-pin header, compatible with unshielded alternative 1 connector as specified in ANSI X3.131-1986 (Figure 4-1).

Partial list of compatible connector plugs (for reference only):

Manufacturer	Model	Part Number
3-M	N.A.	3425-6000
T&B Ansley	N.A.	609-5000M

The cable for the internal SCSI connector should be good quality 50-conductor flat cable with 26- or 28-gauge conductors and a characteristic impedance (Z_0) of 100 ±10 ohms. Cable shielding is necessary if extremely noisy circuitry or extremely noise-sensitive circuitry is present inside the host computer frame.

External Connector

Shielded 50-pin high density (Alternative 1) connector as specified in the proposed ANSI standard X3T9.2/86-109 Revision 10h, Partial list of compatible connector plugs or cable assemblies (for reference only):

Manufacturer	Model	Part Number
AMP	Connector	749111-4
	Back Shell	749193-1
Fujitsu	Connector	FCN-237R050-G/F
	Back Shell	FCN-230C050-D/E or -C/E
Honda	Connector	PCS-XE50MA
	Back Shell	PCS-E50LA

Cable for external SCSI connector should be good quality 100% shielded round cable with 25 twisted pairs. *Each pair should have a characteristic impedance (Z_0) between 90 ohms and 110 ohms.* Wire gauge may be 26 or 28 AWG. All pairs should have the same impedance and should have the same delay per length of cable. Cables meeting these requirements normally operate correctly in any SCSI configuration and should normally meet all FCC requirements.

Complete cable assemblies are available from the following manufacturers:

Manufacturer	Phone
Amphenol Interconnect Products	(607) 786-4221
Quintec Interconnect Systems	(408) 272-8000
Enhance Cable Technology	(408) 293-2425

Radiation Immunity

The AHA-1540C Series meets the radiation limits specified for a Class B computing device in accordance with the specifications in Subpart J of Part 15 of FCC Rules. See FCC Compliance notes and recommendations in the *Preface* of this document.

Reference Documents

The following references may be useful when programming these Adaptec AHA-1540C Series host adapters:

- *IBM® PC-AT® Technical Reference Manual*
- *Small Computer System Interface, ANSI X3T9.2/86-109 Revision 10h,* American National Standards Institute
- Adaptec *AHA-1540C/1542C Installation Guide,*
  Adaptec *AHA-1540CF/1542CF Installation Guide,*
  Adaptec *AHA-1540C/1542C User's Manual,* and
  Adaptec *AHA-1540C Series User's Manual*
- Intel® *82077SL Floppy Disk Controller Data Sheet*

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Chapter Two

Architecture

Hardware

AHA-1540C Series hardware is based on the latest VLSI technology for maximum performance using a minimum of board space. AHA-1540C Series host adapters are assembled on multilayer printed circuit boards in Adaptec's volume manufacturing plant and subjected to a number of functional and mechanical inspections and tests. The architecture of the board is depicted in Figure 2-1.

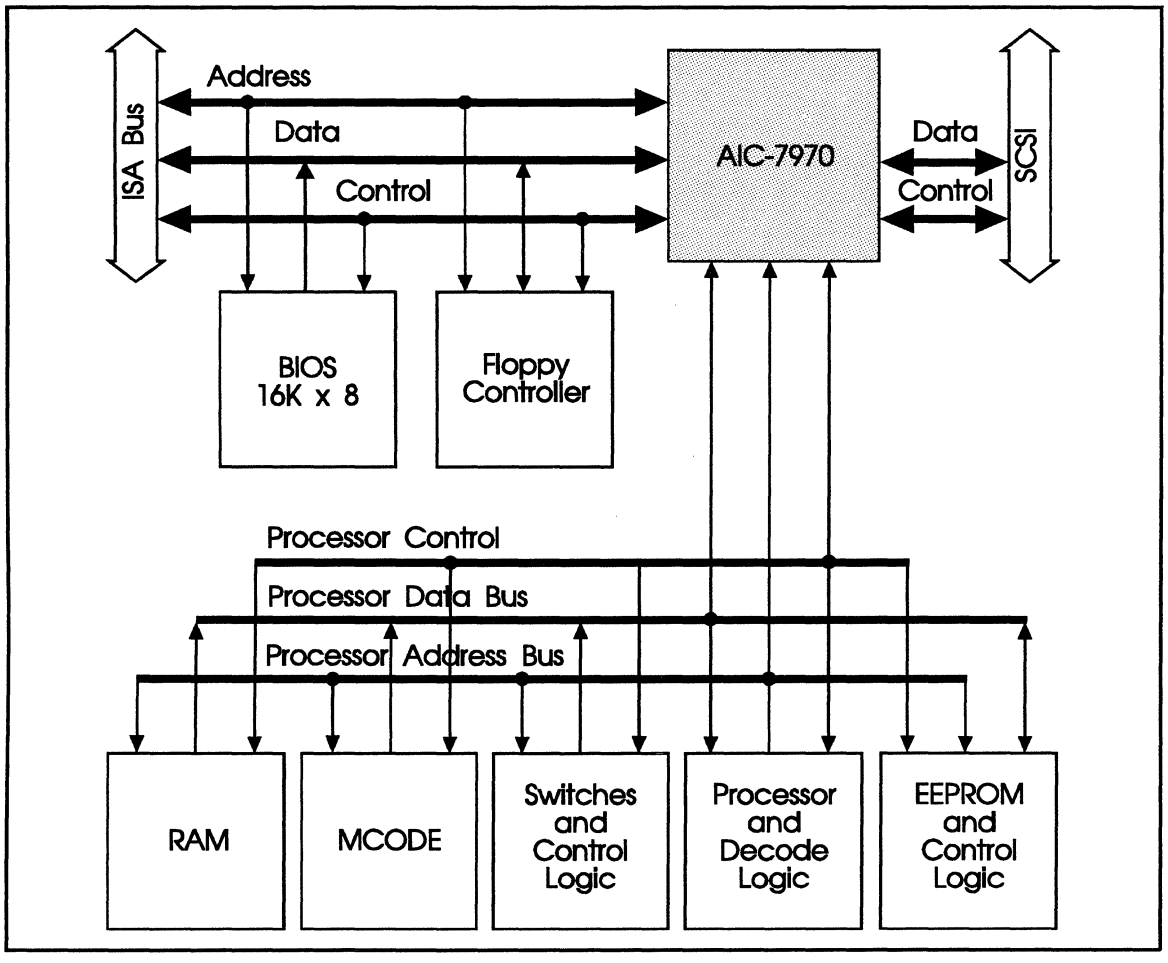

Figure 2-1. AHA-1540C Series Block Diagram

AIC-7970 ASIC

Adaptec has used its long experience in high-performance silicon design for peripheral control applications to incorporate numerous functions in a custom ASIC, the AIC-7970, which streamlines AHA-1540C Series host adapter operation. The AIC-7970 contains several functional blocks, including interface circuitry for the host CPU, BIOS EPROM and floppy disk controller interface, a two-channel bus master DMA controller, decoding logic and SCSI interface capability. Together these provide the AHA-1540C Series host adapters with the following functionality:

- Software selection of host interrupt channel
- Firmware selection and address decoding of the port address used to access the host adapter
- Firmware selection and address decoding of the on-board BIOS address
- Bus master DMA on the ISA bus
- Address decoding for blocks addressed by the on-board Z-80 microprocessor
- Programmable interrupt capability used by the on-board Z-80 microprocessor for SCSI, DMA and host CPU interface circuitry

The microprocessor interface section provides logic to interact with the dedicated processor on the host adapter. The BIOS decode logic allows the BIOS resident on the host adapter to be placed at one of six possible addresses. The floppy disk controller decode section is independent of the rest of the logic and allows the single-chip floppy disk controller (AHA-1542C and AHA-1542CF only) to provide the entire logic to handle two attached floppy disk drives. A single floppy disk I/O address is supported (3F0-3F7h). The AHA-1542CF supports an alternate I/O address (370-377h).

Current overload on the AHA-1540C/1542C is prevented in the internal circuitry of the AIC-7970 via the use of a current limiting fuse; and on the AHA-1540CF/1542CF with a self-resetting circuit breaker. This fuse or circuit breaker allows nondestructive current limiting of the terminator power supplied to the SCSI cable.

The AIC-7970 can perform asynchronous data transfers on the SCSI bus at up to 2.0 MBytes/second, and synchronous transfers at up to 5.0 MBytes/second on the AHA-1540C/1542C, and 10.0 MBytes/second on the AHA-1540CF/1542CF. Fast SCSI transfers are supported on the AHA-1540CF/1542CF. The AHA-1540C Series can operate simultaneously as both an initiator and, if this feature is enabled, as a processor target device.

Through a 16-bit interface internal to the board, the AIC-7970 reduces system bus busy time during data transfer by bursting data across the ISA bus at up to 10 MBytes/second. System bus on and off times are programmable. The AIC-7970 has separate data buses for the local microprocessor and for the host CPU and contains all registers used to communicate between the host adapter and the host CPU. This further increases the performance of the AHA-1540C Series by reducing the overhead associated with execution of SCSI commands.

Shadow RAM

The AIC-7970 contains 128 bytes of RAM which is mapped into the last 128 bytes of host adapter BIOS address space after power on. This RAM holds configuration data. It is accessed during BIOS calls in a fashion transparent to the system CPU.

Bus Master DMA

The bus master DMA capability of the AIC-7970 ASIC permits direct transfer of data to and from main system memory. Such an implementation greatly reduces host software overhead because the host CPU need not maintain the DMA channel address pointers and word counts. Bus master DMA also reduces the number of interrupts generated per I/O command.

Each of the two DMA channels has a 64-byte FIFO used during data transfer. One channel is used for commands and the other for data transfer to and from the host adapter. Only one channel can be active at a time on the ISA bus. The ISA bus DMA channel used by the AHA-1540C Series is software-selectable.

Adaptec's implementation of bus master DMA can achieve a 10 MByte/second burst data rate. This speed is especially valuable in multitasking systems in which tasks execute on a time shared basis. The AIC-7970 DMA circuitry handles both odd byte count and odd starting memory transfers with no performance degradation.

8-Bit and 16-Bit Memory and Odd Byte Data Transfers

The AHA-1540C Series automatically shifts to 8-bit or 16-bit data transfers as indicated by the control lines on the ISA bus. Between addresses 0A0000h and 0BFFFFh hex the signal line MEMCS16 on the ISA bus determines the width of the transfer. If this signal is active, 16-bit memory is assumed, and if it is inactive, 8-bit memory is assumed. Outside of this address space 16-bit memory is always assumed. This capability is provided since some memory in the I/O space, such as video RAM, is 8 bits only and transfers data only on the lower data bits (D0-D7).

Bus master DMA data transfers into 8-bit or 16-bit wide memory are fully supported. During normal DMA operations, nearly all transfers to and from memory are 16 bits wide. At the very end, or the very beginning of a transfer starting at an odd address boundary, an 8-bit transfer on the upper data bits (D8-D15) occurs as defined by the ISA bus architecture.

EEPROM

An on-board EEPROM holds configuration data for the AHA-1540C Series. This data is software configurable.

Floppy Disk Controller (AHA-1542C and AHA-1542CF only)

The floppy disk interface is implemented using an Intel 82077SL single-chip floppy disk drive controller. All drive control signals are fully decoded by this chip and have 24 mA drive capability with selectable polarity. Data and control signals from the drive are buffered by the 82077SL using input buffers that provide hysteresis and thus good noise immunity.

The 82077SL contains a microprocessor interface which is register-level compatible with the PC system. It uses a 16-byte FIFO for improved performance at the microprocessor interface. The AHA-1542C floppy disk controller interface is located at 3F0-3F7h in the PC's I/O space; this address is fixed. The AHA-1542CF supports an alternate floppy disk controller interface location at 370-377h; the default and alternate locations are software switchable. The DMA channel and interrupt channel used by the floppy controller are fixed at 2 and 6 respectively. For hardware information, turn to Appendix B, *Floppy Disk Drive Interface.*

Firmware Description

The AHA-1540C Series supports multithreaded SCSI initiator operation through a simple mailbox protocol. The firmware accepts and queues as many Command Control Blocks (up to a limit of 256 CCBs) as required and executes them from its local RAM. The firmware controls all of the SCSI activity that a task may require, including:

- Arbitration
- Selection
- Disconnection
- Reconnection
- Command completion

Using the same mailbox protocol, AHA-1540C Series host adapters can operate as a processor-type device serving as a multitasking target with respect to other initiators. This feature allows high bandwidth communication between multiple hosts.

In addition, the AHA-1540C Series firmware cooperates with the BIOS installed on the host adapter to emulate the standard DOS Int 13h (disk drive) BIOS calls directed to SCSI drives. This allows booting operations and the execution of standard DOS operations from attached SCSI disks, allowing the SCSI subsystem to completely replace the usual internal disk functions.

A multiuser, multitasking operating system issues a large number of I/O tasks in a rapid sequence. The architecture of the AHA-1540C Series makes management of this activity very easy and straight forward for the operating system and its associated I/O drivers. The next section, titled *Mailboxes*, briefly explains the interaction between the system and the AHA-1540C Series host adapter required to accomplish an I/O task.

Mailboxes

The AHA-1540C Series uses a mailbox architecture for task communication between the host and host adapter. This allows the host adapter to perform multithreaded operations with a minimum of host intervention. The mailboxes are located in main system memory. Each mailbox entry is four bytes long. After power-up sequencing, host initialization procedures, and the boot procedure are completed, the host issues an initialization command to inform the host adapter of the mailbox location. There is always an equal number of Outgoing Mailboxes (MBO) and Incoming Mailboxes (MBI). MBIs are located immediately after the MBOs. The mailbox initialization process typically occurs once after power on, although it can be done any time the host adapter is idle.

A typical mailbox structure is shown as follows:

Base Adr			
+0	CMD	CCB 4 Pointer	MBO 0
+4	CMD	CCB 2 Pointer	MBO 1
+8	00	Free Entry	MBO 2
+12	CMD	CCB 3 Pointer	MBO 3
+16	00	Free Entry	MBI 0
+20	Status	CCB 1 Pointer	MBI 1
+24	00	Free Entry	MBI 2
+28	00	Free Entry	MBI 3

In this example there are four MBOs and four MBIs. The first byte of each MBO contains the MBO Command byte. The remaining three bytes point to a Command Control Block (CCB). The CCB provides the rest of the information needed to complete a task. A physical address is used for the CCB pointer. An MBO is available to accept a new entry if the first byte is zero.

The first byte of each MBI contains the status of a completed task. The remaining three bytes point to the CCB of the completed task. An MBI is free if the Status byte is zero. Mailboxes may point to CCBs controlling initiator tasks, target tasks, or error recovery tasks.

Command Control Block

A Command Control Block provides the information required to control a SCSI command sequence. The block contains pointers to the data area to be used by the command. It contains areas for presenting status for both the host adapter and the addressed SCSI device. In addition, it contains the SCSI Command Descriptor Block defining the action to be taken by the addressed SCSI device. An error information buffer area is also provided.

A Command Control Block is also used to service an operation requested by another initiator when the AHA-1540C Series host adapter is addressed as a SCSI Processor device. The complete set of Command Control Block Opcodes is defined in the section titled *Command Block Definition* in Chapter Five, *Firmware Description.*

The following shows a typical CCB:

Byte 0	Command Control Block Opcode			
+1	Tar/Init	Data Out	Data In	LUN
+2	SCSI Command Length = m			
+3	Returned Sense Info Length = n			
+4	Data Length (MSB, MID, LSB)			
+7	Data Pointer (MSB, MID, LSB)			
+10	Link Pointer (MSB, MID, LSB)			
+13	Command Link ID			
+14	Host Status			
+15	Target Status			
+16	Reserved			
+17	Reserved			
+18	SCSI Command Bytes (m Bytes)			
18 + m	Allocated for Sense Data (n Bytes)			

Command Descriptor Block

The Command Descriptor Block (CDB), a part of the Command Control Block, is a standard format command packet that is transmitted to the addressed SCSI device. It contains all the command information required by the SCSI device to perform the desired operation. The CDB contains the command operation code followed by a Logical Unit Number (LUN), command parameters if required, and a control byte. A typical Group 0 6-byte CDB follows:

	Bit 7	6	5	4	3	2	1	0
Byte 0	Operation Code							
1	LUN			Logical Block Address (MSB)				
2	Logical Block Address							
3	Logical Block Address (LSB)							
4	Transfer Length							
5	Vendor Unique			Reserved			Flag	Link

Please refer to the *American National Standard for information systems - Small Computer Systems Interface (SCSI),* ANSI X3.131, the *Common Command Set (CCS) Revision 4B,* and the *draft proposed American National Standard for information systems - Small Computer Systems Interface - 2 (SCSI-2)* for additional information on Command Descriptor Blocks.

Principles of Operation

At power-up, the host PC must inform the SCSI host adapter of the location and number of mailboxes. To start a task, the host builds a CCB and stores its memory address in a free mailbox. A non-zero Mailbox Out command byte is then written to indicate that the mailbox entry is full and valid. The host then writes to an I/O port (see Chapter Four, *Hardware Functional Description*) to tell the host adapter to scan the MBO area. When a full MBO is found, the host adapter copies the mailbox's CCB pointer into its internal RAM and clears the mailbox entry by writing a zero to the MBO command byte. This frees the MBO so that it can be used to start another task.

After completing a task, the host adapter scans the MBI area for a free mailbox. When one is found, it is updated with the task's completion status and CCB pointer. The CCB pointer identifies the completed task. An MBI stored interrupt is generated to notify the host that a task was completed. The host scans the MBI area searching for a non zero Status byte. When one is located, the host obtains the CCB pointer and frees the MBI by writing a zero into the Status byte. The host then examines the contents of the CCB to determine that the command was successfully completed. The freed MBI can now be used to indicate the completion of another task. The host adapter fills the MBI area and scans the MBO area in a round-robin fashion. If the host saves the position of the last active MBI entry, it can determine the MBI of a new entry immediately without searching, since a new entry exists in the next MBI location.

The host adapter transmits a new MBO Available (if enabled) or MBI Full interrupt to the host whenever all non-mailbox interrupts are cleared and serviced by the host. The host should analyze the interrupts and clear them as soon as possible so that the host adapter can post any new interrupts quickly. The host adapter does not wait until an interrupt can be transmitted to the host before processing an MBO entry or creating a new MBI entry. Thus, in processing a single MBI interrupt, the host may find several MBI entries waiting by the time the interrupt processing is finished. Similarly, a later MBI interrupt for the last of the later MBI entries may find nothing to service because the MBI entry was examined and processed as a result of the first MBI Full interrupt. If the interrupts are reset quickly by the

host, the probability of an interrupt occurring when no MBI entry is available is much lower, providing an important performance improvement. If the MBI entries are emptied by the host in a round-robin order, the scan for the next full entry is very simple, since it is always the next MBI entry in the mailbox area.

Task Queuing

Multiple tasks may be started against a target/LUN or against multiple targets/Logical Units. Since only one task can be active against any one LUN at a time, all other tasks for the same LUN are queued on the host adapter. SCSI-2 style command queuing is not implemented by the AHA-1540C Series. Other LUNs may have active tasks at the same time.

The host adapter de-queues on a first in, first out (FIFO) basis for each target/LUN combination. However, due to the optimization algorithm used by the host adapter, a task may sometimes be started earlier on multiple target/LUN systems in spite of its later occurrence in the queue. Task queuing should not be used where changes in the order of command execution may cause data integrity failures.

A full description of the control block and its operation is provided in Chapter Five, *Firmware Description*.

Onboard BIOS Operation

A host adapter BIOS is provided to emulate the standard fixed disk BIOS and boot functions by intercepting Int 13h (disk drive) calls. With this BIOS, the host adapter can be used in lieu of a standard fixed disk controller on any ISA-compatible system.

During system boot, the BIOS reads configuration information from the on-board EEPROM. If this data cannot be found or correctly recognized, the BIOS will issue an error message.

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Chapter Three

Installation

Unpacking and Inspection

The carrier is responsible for damage incurred during shipment. In case of damage, have the carrier note the damage on both the delivery receipt and the freight bill, then notify your freight company representative so that the necessary insurance claims can be initiated.

After opening the shipping container, use the packing slip to verify receipt of the individual items listed on the slip. Retain the shipping container and packing material for possible later re-use should return of the equipment to the factory be necessary.

Figures 3-1 and 3-2 show the AHA-1540C Series AHA-1542C and AHA-1542CF host adapter boards, and the location of various devices on them. The AHA-1540C and AHA-1540CF boards are similar, with the exception of the floppy controller and internal floppy connector, which are not included on those models.

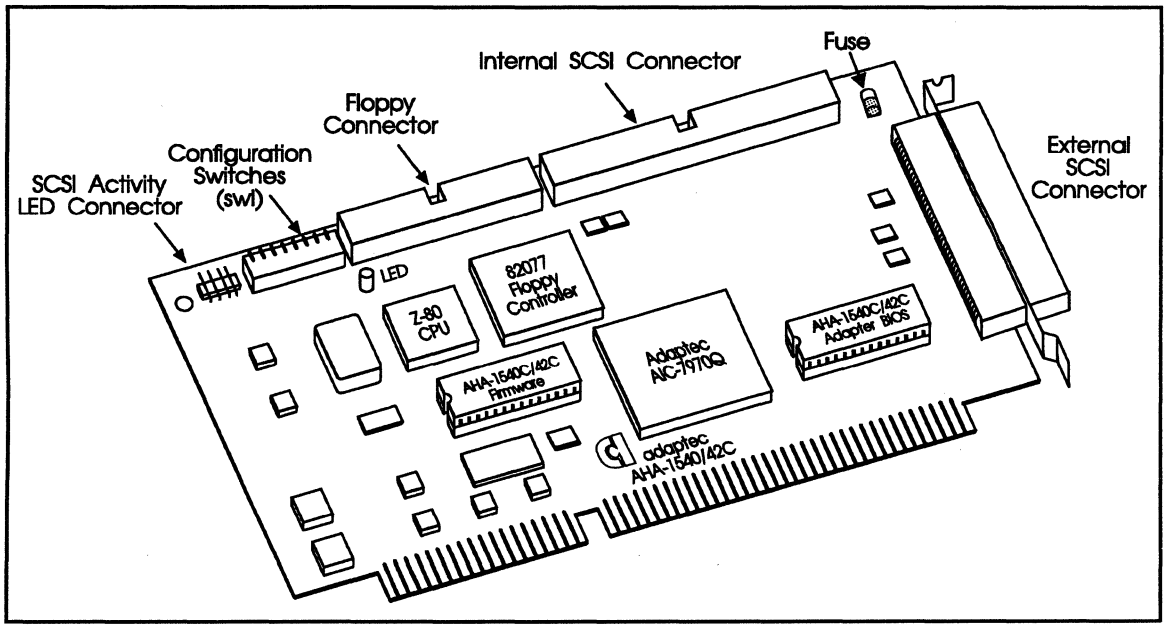

Figure 3-1. ***AHA-1540C Series*** **AHA-1542C**

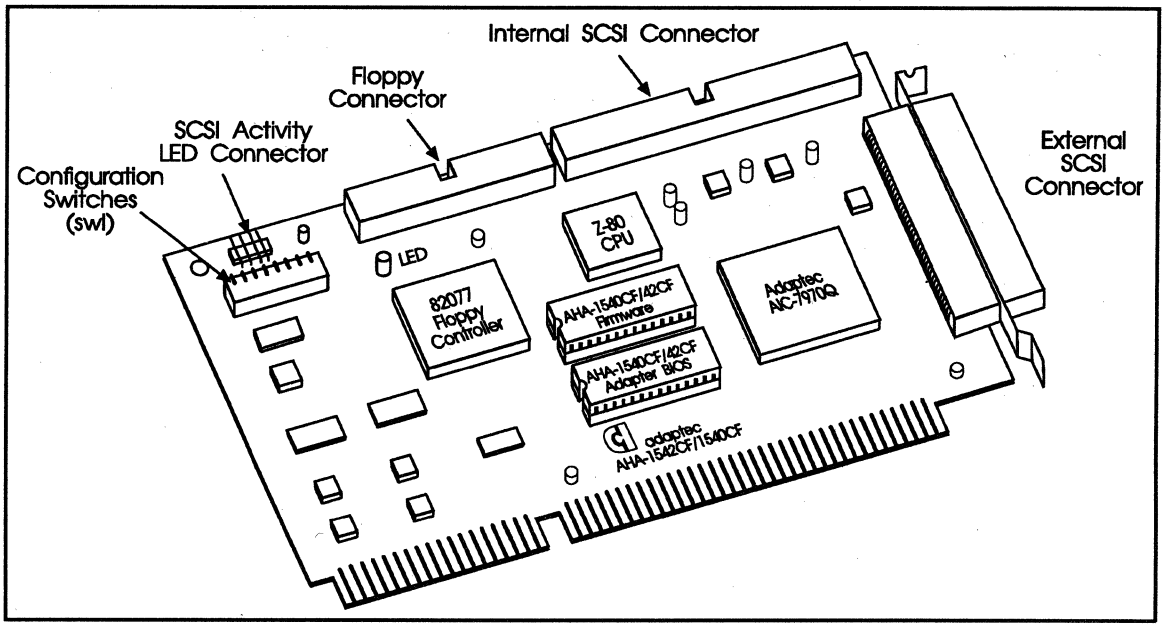

Figure 3-2. *AHA-1540C Series* AHA-1542CF

Caution

The AHA-1540C Series host adapters have been carefully designed to resist the effects of static electricity. However, unusual static discharges can damage or shorten the life of any electronic equipment. Please take the proper precautions when handling the board. Keep the board in its conductive wrapping until it is ready to be installed in your system. Be sure that the host computer and the personnel handling the board are properly grounded while installing the board.

Installation

The following section details the proper setup for the Adaptec AHA-1540C Series ISA to SCSI host adapters. The installation of the board consists of:

1. Verifying the on-board DIP switch settings
2. Preparing the SCSI devices, including installing their correct terminations
3. Inserting the board into a full-length ISA-compatible connector
4. Connecting a SCSI cable from the on-board connector to a SCSI target
5. Verifying and/or setting host adapter configuration through the ROM-based SCSI*Select*™ BIOS configuration utility (keyboard accessible at system boot)

> **Note**
> The system must be turned off during physical installation of the host adapter board.

Hardware Setup

Several preparatory steps must be taken to install the host adapter in the host computer. The AHA-1540C Series on-board DIP switch settings should be verified and adjusted if necessary. The SCSI bus terminators must be installed in the correct SCSI devices. Finally, the correct SCSI IDs must be assigned to each peripheral device.

The Adaptec AHA-1540C Series 16-bit ISA to SCSI bus host adapter is designed to operate as shipped in the majority of ISA bus computers. The host adapter's DIP switch settings should almost always remain in their original default positions. The AHA-1540C Series is shipped with the following default settings:

Setting	Default Value	How Set
SCSI ID	7	Software
SCSI Parity	Enabled	Software
SCSI Termination	Enabled	Software/Switches
Terminator Power	Supplying	Always enabled
Synchronous Negotiation	Disabled	Software
DMA Channel	5	Software
DMA Transfer Rate	5.0 MBytes/sec	Software
Interrupt Channel	11	Software
AT Port Address	330h	Switches
AT BIOS Address	DC000h	Switches
Floppy Disk Controller	Disabled (AHA-1540C, AHA-1540CF) Enabled (AHA-1542C, AHA-1542CF)	Switches
BIOS	Enabled	Switches
Floptical Drive Support	Disabled	Software

BIOS Address Selection

The BIOS base address is set by switches prior to system power up. Firmware reads the switch settings and stores them in a two-byte register in the BIOS address space at power on; if they are subsequently changed, the changes are not recognized until the system is powered up again. The first byte is a switch setting and the second byte is the 2's complement thereof to ensure checksum consistency. The following table indicates the proper BIOS base address selection and the appropriate switch settings. Note that enabling a bit requires it to be Off; when a switch is On, that bit is disabled. The default address is marked with an asterisk (*).

SW6	SW7	SW8	Address 16k x 8
Off	Off	Off	DC000h*
On	Off	Off	D8000h
Off	On	Off	D4000h
On	On	Off	D0000h
Off	Off	On	CC000h
On	Off	On	C8000h
Off	On	On	Reserved
On	On	On	BIOS Disabled

Note
All the switches are read in once upon power up. If any switch is changed during operation, it will not be recognized until the board is powered down and powered up again. In order to make switch settings effective, power down the system, change any switches and power up again.

AT I/O Port Selection

The following table shows the various AT port addresses available by setting DIP switches. The default setting is marked with an asterisk.

SW2	SW3	SW4	Address
Off	Off	Off	330h*
On	Off	Off	334h
Off	On	Off	230h
On	On	Off	234h
Off	Off	On	130h
On	Off	On	134h
Off	On	On	Reserved
On	On	On	Reserved

Floppy Controller Enabling

Floppy drive controller enabling and disabling is controlled by SW5 on the AHA-1540C Series host adapter. The Intel 82077SL is used as a floppy controller; it is located only on the AHA-1542C and AHA-1542CF host adapters. It supports 250, 300, 500 and 1000 KBits/sec transfer rates. Do not attempt to change the setting for SW5 if you have an AHA-1540C or AHA-1540CF host adapter; it should remain in the On position. Disable the AHA-1542C/AHA-1542CF floppy controller if another controller already runs your floppy drives, or disable the other floppy drive controller. Refer to your user's manual concerning disabling

your current floppy drive controller. The following settings will enable or disable the floppy disk controller for the AHA-1542C and AHA-1542CF:

SW5 Off = Enabled (default for 1542C and 1542CF)

SW5 On = Disabled (default for 1540C and 1540CF)

SCSI Termination

The SCSI bus must be terminated correctly to assure proper operation. The first and last physical SCSI devices on the SCSI cable must have terminators installed/enabled. All other SCSI devices must have terminators removed/disabled. The host adapter termination state can be controlled by the SCSI*Select* BIOS configuration utility, or by setting SW1=On. SW1=Off is the factory default setting. The relationship of the BIOS configuration utility setting and the position of SW1 is defined in the table below:

SW1 Setting	Configuration Utility Setting	Termination Status
Off	Enabled	Enabled
Off	Disabled	Disabled
On	Enabled	Enabled
On	Disabled	Enabled

The internal and external connectors on the AHA-1540C Series connect to the same SCSI bus, so both internal and external cabling must be considered in determining where terminators are installed:

- If only one cable (either internal or external) is connected to the host adapter, the host adapter terminators must remain enabled. Terminators must also be installed on the device at the farthest end of the cable from the host adapter. Terminators must be removed from, or disabled on, all other attached SCSI devices.

- If both internal and external cables are connected to the host adapter, disable termination on the host adapter and install terminators on the devices at the farthest end of each cable. Terminators must be disabled on the host adapter and removed from, or disabled on, all devices except the device at the end of each cable. The instruction manuals for each SCSI device indicate how the terminators can be removed/disabled or replaced/enabled.

SCSI ID Setting

The SCSI target address (SCSI ID) for each intended SCSI target device must be selected by setting the proper jumpers or switches on those devices. Guidelines for setting the SCSI ID are as follows:

- Each device installed on a SCSI bus must be set to a unique SCSI ID; this includes the SCSI host adapter. Devices may not share SCSI IDs.

- The host adapter's default ID is 7; it seldom needs to be changed, although the SCSI*Select* BIOS configuration utility can be used to do so.

Duplicate SCSI IDs will cause errors that are extremely difficult to identify. Any jumpers on adapters other than the AHA-1540C Series (which has no jumpers) that control operating modes must also be properly set.

Check the SCSI drive or controller to ensure that parity checking is enabled. If parity checking on the device is disabled or not supported, disable parity checking on the host adapter with the SCSI*Select* BIOS configuration utility. Parity checking should only be enabled if all SCSI devices support it.

Floptical Support (AHA-1540CF1542CF only)

If you have connected a Floptical diskette drive to the SCSI bus, BIOS Support for Floptical Drives must be enabled with SCSI*Select* BIOS configuration utility.

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Chapter Four

Hardware Functional Description

Hardware Overview

This section provides a description of the AHA-1540C Series hardware-to-PC-host-software functional interface.

DMA control logic on the AHA-1540C Series host adapters control ISA bus arbitration and data transfer handshaking. During DMA data transfers, the AHA-1540C Series become bus masters. The DMA logic supports both odd and even starting addresses. For odd starting addresses, the first transfer will be an 8-bit transfer. Thereafter, 16-bit transfers will be used to complete the data transfer. Odd-byte transfers and the last transfer of an even number of bytes to an odd address are treated in a similar manner.

The SCSI port is controlled by the AIC-7970, an Adaptec SCSI protocol device which supports arbitration, selection, and reselection with a minimum of processor intervention. This VLSI device also supports target mode and synchronous SCSI transfers.

I/O Port Interface

The I/O port interface consists of four 8-bit wide I/O ports in the PC I/O address space. They form the primary communications channel between the host CPU and the host adapter. The base port is for control and status, the second port for command and data transfer, and the third port for interrupt flags. The fourth port is used for identification of the AHA-1540C Series host adapter.

I/O Port Interface Bit Definition

Port Address = Base + 0

WRITE: Control Register		READ: Status Register	
Bit 7	Hard Reset (HRST)	Bit 7	Self Test in Progress (STST)
Bit 6	Soft Reset	Bit 6	Internal Diagnostic Failure (DIAGF)
Bit 5	Interrupt Reset (IRST)	Bit 5	Mailbox Initialization Required
Bit 4	SCSI Bus Reset (SCRST)	Bit 4	SCSI Host Adapter Idle (IDLE)
Bit 3	Reserved (0)	Bit 3	Command/Data Out Port Full (CDF)
Bit 2	Reserved (0)	Bit 2	Data In Port Full (DF)
Bit 1	Reserved (0)	Bit 1	Reserved (Undefined)
Bit 0	Reserved (0)	Bit 0	Invalid HA Command (INVDCMD)

Port Address = Base + 1

WRITE: Command/Data Out		READ: Data In	
Bit 7	Command/Data Out Bit 7	Bit 7	Data In Bit 7
Bit 6	Command/Data Out Bit 6	Bit 6	Data In Bit 6
Bit 5	Command/Data Out Bit 5	Bit 5	Data In Bit 5
Bit 4	Command/Data Out Bit 4	Bit 4	Data In Bit 4
Bit 3	Command/Data Out Bit 3	Bit 3	Data In Bit 3
Bit 2	Command/Data Out Bit 2	Bit 2	Data In Bit 2
Bit 1	Command/Data Out Bit 1	Bit 1	Data In Bit 1
Bit 0	Command/Data Out Bit 0	Bit 0	Data In Bit 0

Port Address = Base+ 2

WRITE: Reserved, do not write		READ: Interrupt Flags	
Bit 7		Bit 7	Any Interrupt
Bit 6		Bit 6	Reserved
Bit 5		Bit 5	Reserved
Bit 4		Bit 4	Reserved
Bit 3		Bit 3	SCSI Reset Detected (SCRD)
Bit 2		Bit 2	HA Command Complete (HACC)
Bit 1		Bit 1	MBO Available (MBOA)
Bit 0		Bit 0	MBI Full (MBIF)

Port Address = Base +3

WRITE: Reserved, do not write		READ: Identification Register	
Bits 7-0		Bits 7-0	When read, this register will return the first four letters identifying the manufacturer's name, ADAP (from *Adap*tec) and repeat this string endlessly in circular fashion during subsequent reads.

Control and Status Port

Writing a one to the bits of the Control Port initiates certain special host adapter operations. There is no requirement to return the bits to the zero state, since they are reset automatically after the requested operation is initiated. Read operations to the Status port address return host adapter status information.

Base+0 Port, Write: Host Adapter Control Port

Bit 7 - Hard Reset (HRST)
Setting the Hard Reset bit to one forces the host adapter into a state identical to that of normal power-on. Diagnostic functions are executed, and the status of all on-going SCSI operations are lost. A Reset Condition is generated on the SCSI bus.

While the reset is being processed, the Self Test in Progress bit (Host Adapter Status Port bit 7) is set. When the reset is complete, that bit is reset and the Mailbox Initialization Required bit (Host Adapter Status Port bit 5) and the SCSI Host Adapter Idle bit (Host Adapter Status Port bit 4) are set; these indicate that the AHA-1540C Series mailbox structure must be reinitialized and that no other operations are active on the host adapter. See the *Reset Functions* section in this chapter for a description of the overall reset structure.

Bit 6 - Soft Reset (SRST)
The Soft Reset bit clears all on-going SCSI and host adapter commands. All Command Control Blocks are abandoned and all queued commands are abandoned. Mailbox In and Mailbox Out entries must be cleared by the host. No diagnostic functions are executed. A Reset Condition is not generated on the SCSI bus. The Mailbox Initialization Required bit (Host Adapter Status Port bit 5) and the SCSI Host Adapter Idle bit (Host Adapter Status Port bit 4) are set when processing is completed. This indicates that the AHA-1540C Series mailbox structure must be reinitialized and that no other operations are active on the host adapter. See the *Reset Functions* section in this chapter for a description of the overall reset structure.

Bit 5 - Interrupt Reset (IRST)
Setting this bit clears the interrupt port of all bits that have been set and resets the interrupt line. The host adapter manages the interrupt presentation to minimize the possibility of incorrectly resetting an interrupt. MBOA (Mailbox Out Available) and MBIF (Mailbox In Full) interrupts are presented immediately unless an SCRD or HACC interrupt has not yet been cleared by the host. The SCRD (SCSI Reset Detected) or HACC (Host Adapter

Command Complete) are the only bits set after any interrupt bit has been cleared and the DF (Data In Port Full) bit is zero, indicating an operation is fully completed.

The prompt resetting of MBOA and MBIF interrupts minimizes the chance that the reset of one will also reset the other. Host programs should, however, be aware that there is a small chance of falsely resetting a new MBIF while clearing an MBOA interrupt. This can be resolved by periodically scanning the MBI entries when activity is expected on the host adapter or by not enabling the MBOA interrupt.

Bit 4 - SCSI Bus Reset (SCRST)
The setting of this bit causes a SCSI Bus Reset to be generated on the SCSI bus. The SCSI Bus Reset is triggered at the time the SCRST bit is set to one and raises the RST line on the SCSI Bus for the designated 25 microsecond period. The reset is managed as a SCSI Soft Reset and will allow partially completed operations to continue after the reset occurs. See the *Reset Functions* section in this chapter for a description of the overall reset structure.

Bits 3-0 - Reserved
Reserved bits must be set to zero to avoid compatibility problems with future extensions of the Control Register.

Base+0 Port, Read: Host Adapter Status Port

Bit 7 - Self Testing in Progress (STST)
This bit, when one, indicates that the host adapter is performing self-initialization and internal diagnostics. The bit is set after a power-on or hard reset (Control Port Bit 7 HRST = 1). When diagnostic operation is complete, the STST bit is reset to zero and bit 5 or bit 6 is set to one to indicate the successful or unsuccessful completion of the diagnostics. If bit 7 remains on, it indicates that the initialization or diagnostic could not be completed. In most cases, bit 6 (DIAGF) will be set to indicate that an internal diagnostic failure occurred.

Bit 6 - Internal Diagnostic Failure (DIAGF)
This bit, when one, indicates that the self-testing process has completed and that an error was detected. The host adapter must be reset by setting the Hard Reset bit (bit 7 of the Control Port) to clear the error. If the AHA-1540C Series host adapter again detects an error, troubleshooting procedures must be performed to identify and correct the error condition. The diagnostic LED will usually present a flash code that indicates the nature of the failure.

Bit 5 - Mailbox Initialization Required (INIT)
This bit, when one, indicates that the self-testing process has completed successfully and that the AHA-1540C Series is ready for mailbox initialization to be performed. The base memory address of the mailbox area must be established by execution of the Mailbox Initialization command. After execution of the Mailbox Initialization command and any other desired initialization operations, the AHA-1540C Series is ready for full operation.

Bit 4 - SCSI Host Adapter Idle (IDLE)
This bit, when one, indicates that the host adapter is in the idle state. The host adapter has no outstanding adapter commands or SCSI commands. The host processor must wait for the idle state before executing any adapter command except the Start SCSI (02) Command.

Bit 3 - Command/Data Out Port Full (CDF)
The host uses the CDF bit to synchronize command and data transfers to the host adapter. An adapter command byte or an outbound parameter byte can be placed in the Command/Data Out Port when the port is empty, indicated by the CDF bit being zero.

When a byte is placed in the Command/Data Out Port, the CDF bit is set to one and remains one until the host adapter has obtained and processed the byte. When the CDF bit returns to zero, the next command or parameter byte can be placed in the port.

Bit 2 - Data In Port Full (DF)
The host uses the DF bit to synchronize transfers of data from the host adapter to the host. When the DF bit is set to one, the host adapter has placed a byte in the Data In Port for the host to remove and process. When the host performs a read to the Data In Port address, the DF bit is reset to zero automatically and not set to one again until a new data byte has been placed in the Data In Port.

Bit 1 - Reserved
This bit must be reset to zero.

Bit 0 - Invalid Host Adapter Command (INVDCMD)
The Invalid Host Adapter Command bit is set to one if an invalid command or parameter byte was received in the Command/Data Out Port. After sending a command byte or data byte, the host software determines that the next byte is ready to send by waiting for the CDF bit to be reset. If the command byte or parameter byte is not valid, the command sequence will instead be terminated by the host adapter.

The host adapter always terminates a command by raising the Host Adapter Command Complete (HACC) interrupt. If the HACC interrupt is set to one and the INVDCMD bit is not set, the command terminated normally. If the INVDCMD bit is also set to one, the command or parameter bytes were determined to be invalid and the command terminated abnormally. The INVDCMD bit is only valid from the time the HACC interrupt is set until the HACC interrupt is reset. The bit's value is not predictable until a new HACC interrupt is set for a new adapter command.

Command/Data Out and Data In Port

The second I/O port address is used by the host to write adapter command bytes and accompanying host adapter data bytes to the host adapter. This port address is also used by the host adapter to send parameters back to the host device to be read.

The Command/Data Out Port is used by the host to send host adapter initialization and management commands and parameters that cannot be sent by the standard mailbox protocol. Information requested by the adapter commands is placed in the Command/Data Out Port and is then returned through the Data In Port. The host should understand the format and number of bytes to be transmitted for each command. This insures that extra invalid bytes are not passed across the interface. Bytes in addition to those required by a given command are likely to be interpreted as invalid. However, any excess bytes used with a command may errantly cause the execution of valid commands.

The host should only write to the Command/Data Out Port when CDF is zero. This allows time for the host adapter to process a previously written command or parameter byte. CDF is

automatically set to one when the host writes to the port and is reset to zero after the host adapter reads the port.

If an adapter command needs additional data bytes, the host waits until CDF is zero before writing the additional bytes to the Command/Data Out Port. Just as in the command transfer case, each parameter byte written will set CDF. The host can write additional data bytes only after CDF is again zero. The HACC interrupt indicates when the command has terminated, normally or abnormally. If INVDCMD is also set, the host adapter found either the command or data bytes to be invalid and terminated abnormally. The use of CDF as a handshaking bit is required to prevent the transfer of invalid data.

If an adapter command requires data transfer from the host adapter, the host adapter will place the data bytes in the Data In Port and set the DF bit (Status Port bit 2) to indicate that the requested parameter is ready for the host to read. When the host reads the Data port, DF is automatically reset. The host should wait until DF is again set before attempting to transfer the next parameter byte. The use of the DF bit to control the handshaking process is required to prevent the transfer of invalid data. After the last data byte has been transferred, the HACC interrupt bit will be set indicating command completion. If the adapter command was invalid, the HACC interrupt will occur before all data bytes have been transmitted and the INVDCMD bit will be set.

Interrupt Flag Port

The Interrupt Flag Port contains bits that indicate the reason that an interrupt was provided to the host from the host adapter. The host adapter uses the interrupt to notify the host that the host adapter is ready for immediate service from the host.

The Interrupt Flag Port is a read-only port. When an interrupt bit is set by the host adapter to indicate that the host should respond, the Any Interrupt bit and the interrupt line are both also set. When the host begins to examine the returned registers and mailboxes to determine the cause of the interrupt and to perform the operations needed to service the interrupt, the host will first read the Interrupt Flag Port to record which interrupts must be serviced. The host will then clear the interrupts by setting the IRST bit (Host Adapter Control Port bit 5). The host adapter presents MBOA and MBIF interrupts immediately unless there is already an SCRD (SCSI Reset Detected) or HACC interrupt present. If SCRD or HACC is present, the MBOA and/or MBIF interrupt will be posted after the SCRD or HACC interrupt is cleared by the host. An SCRD or HACC interrupt will only be presented if the Any Interrupt signal is zero and the DF signal is zero, indicating the completion of all pending interrupt presentation. It is recommended that the MBOA interrupt be enabled only when required by the host. This prevents the possible setting and resetting of MBIF interrupts before they are processed. Other reset operations will also reset the Interrupt Flag Port and the interrupt line, including the Hard Reset bit (HRST), the Soft Reset bit (SRST), and the power-on reset issued by the motherboard.

Base+2 Port, Read Only: Interrupt Flag Port

Bit 7 - Any Interrupt
This bit, when one, indicates that the interrupt to the host has been established. The interrupting condition is identified in bits 0 to 3.

Bits 6-4 - Reserved
Returned as zero.

Bit 3 - SCSI Reset Detected (SCRD)
This bit, when one, indicates that a SCSI Reset has been received on the SCSI bus. The Any Interrupt bit and the PC's interrupt signal will also be set. The host adapter supports SCSI Soft Reset (see the section titled *SCSI Soft Reset Option* in this chapter). Any on-going target or initiator activities will continue normally after first clearing the SCSI bus. In some rare cases, host intervention will be required to restart a SCSI command that was aborted by the reset operation. The host can convert the SCSI Soft Reset to a SCSI Hard Reset by setting the Control Register Soft Reset (Bit 6) to one, clearing all on-going operations in the host adapter. In this case, the host must recognize that any operations not yet completed will never be completed and must perform appropriate error recovery operations. See the section titled *Reset Functions* in this chapter which describe the overall reset protocol. The SCRD bit is not set for host-initiated SCSI Reset conditions caused by the setting of the HRST bit or the SCRST bit, since the host is already aware of the actions it has requested. If the Any Interrupt signal or DF signal is present, the SCRD interrupt will not be presented until the interrupts already present are cleared.

Bit 2 - Host Adapter Command Complete (HACC)
This bit, when one, indicates that an Adapter command has been completed, normally or abnormally. The Any Interrupt bit and the PC's interrupt signal will also be set. If the command was completed normally, only the HACC bit will be on. If the command was completed abnormally or was aborted before it was completed, the HACC bit will be one and the Invalid Command Bit (Status Register bit 5) will also be one. During parameter transfers to or from the host adapter, the HACC bit should be examined to verify that the command is still being processed and has not been ended abnormally. If the Any Interrupt signal or DF signal is set, the HACC interrupt will not be presented until the interrupts already presented are cleared.

Bit 1 - Mailbox Out Available (MBOA)
This bit, when one, indicates that an outbound mailbox entry is now available for use by the host. The Any Interrupt bit and the PC's interrupt signal will also be set. Most operating systems will choose to leave this interrupt disabled to avoid the generation of extra interrupts. The host adapter will normally empty Mailbox Out entries to its local RAM so rapidly that round-robin filling of the Mailbox Out entries will assure that a Mailbox Out entry will already be empty by the time the host is ready to fill it again.

If the host finds that all Mailbox Out entries are full, it can enable the Mailbox Out Available interrupt by executing an Enable Mailbox Out Interrupt command through the I/O Command Port. The Enable Mailbox Out Interrupt command is one of the two commands that can be executed without waiting for the IDLE state of the host adapter. As soon as any Mailbox Out entry is cleared by the host adapter, an MBOA interrupt will be generated to indicate to the host that an MBO entry is available. An MBOA interrupt is generated after that each time a Mailbox Out entry is cleared by the host adapter until an Enable Mailbox Out Interrupt command is executed to force the reporting of MBOA interrupts to be disabled. If the SCRD or HACC interrupts are present, the MBOA interrupt is not presented until they are cleared. At all other times, MBOA is presented immediately.

Bit 0 - Mailbox In Full (MBIF)
This bit, when one, indicates that an entry has been placed by the host adapter in the Mailbox In. The interrupt should be reset as soon as possible so that any subsequent interrupts can be detected. The host adapter may return information in other Mailbox In entries, so the host should check the next entry to determine if more than one set of information has been

provided. The MBI entries are filled in round-robin order, so the host should simply check the next MBI entry after the last one that was found when a new MBIF interrupt occurs.

If an MBIF interrupt is set and other Mailbox In entries are made before the interrupt is cleared, then all the entries can be scanned as found. The new MBIF interrupt will be presented if the SCRD and HACC interrupts are cleared. A new MBIF interrupt will be presented regardless of the state of the MBOA interrupt bit. It is important to clear and record each interrupt as soon as possible to avoid the possible accidental resetting of a valid interrupt. In addition, it is desirable to enable the MBOA interrupt as rarely as possible. The host system software must be ready to scan for MBI entries even if no MBIF interrupt occurred.

Reset Functions

The AHA-1540C Series provides extensive reset functions. This allows for the fullest flexibility and architectural consistency with both the SCSI and ISA (Industry Standard Architecture).

Hard Reset Operations

Resets may be generated by powering down the AHA-1540C Series Host Adapter. This is accomplished by normal system power switch cycling or the Hard Reset procedure for your system. Setting the HRST bit (bit 7 of the Host Adapter Control Port) will also force a hardware reset to the AHA-1540C Series. Regardless of the source, a Hard Reset forces the following actions on the AHA-1540C Series.

- All internal registers of the AHA-1540C Series are returned to their reset condition.
- The host adapter's microprocessor returns all internal information and parameters to their initial state.
- The host adapter performs all required internal diagnostics.
- A standard SCSI Reset condition is generated to all other attached SCSI devices.

During the Hard Reset process, the AHA-1540C Series indicates to the attached host that self-testing is in process. This is accomplished by raising the STST bit in the Host Adapter Status Port. After the Hard Reset process is complete, the AHA-1540C Series indicates that initialization parameters are required from the host by raising the initialization bit in the Host Adapter Status Port.

SCSI Reset Operations

The SCSI Reset condition is defined in the *SCSI Standard, X3.131-1986, Section 5.2.2.* A SCSI Reset condition may be forced by any SCSI device on the bus. The condition is forced by the assertion of the SCSI Reset signal.

The AHA-1540C Series has four mechanisms which may force a SCSI Reset condition. The SCSI Reset condition may be invoked from the host software if the software sets the SCRST bit (Bit 4 of the Host Adapter Control Port). In this case, the normal SCSI Reset operations

will be performed by the host adapter and the SCSI Reset signal will be asserted on the SCSI bus. In this case, the SCRD bit (Interrupt Flag Port bit 3) will not be set, since the host itself caused the reset.

The SCSI Reset is invoked if a Hard Reset is generated by cycling the system power, i.e. powering the system down and then back up by using the Reset button or the power supply ON/OFF switch.

The SCSI Reset condition may be invoked by the AHA-1540C Series as part of the recovery mechanism for a SCSI bus phase error. Bus phase errors may include detection of an invalid information transfer phase or detection of an impossible phase sequence (Command Phase after a Data Phase in the same command). In this case, the normal SCSI Reset operations will be performed and the SCSI Reset signal will be asserted on the SCSI bus. In addition, the SCRD bit (Interrupt Flag Port bit 3) will be set to indicate to the host computer that a SCSI Reset condition occurred. The setting of the SCRD bit also causes the Any Interrupt bit (Interrupt Flag Port bit 7) and the appropriate interrupt signal to be presented.

The SCSI Reset condition may be invoked by another SCSI device attached to the AHA-1540C Series as part of the other device's recovery mechanism or initialization procedure. In this case, the normal SCSI Reset operations will be performed. In addition, the SCRD bit (Interrupt Flag Port bit 3) will be set to indicate to the host computer that a SCSI Reset condition occurred. The setting of the SCRD bit also causes the Any Interrupt bit (Interrupt Flag Port bit 7) and the appropriate ISA interrupt signal to be presented.

SCSI Soft Reset Option

The SCSI Specification indicates two methods for handling normal SCSI Reset operations. The AHA-1540C Series implements the Soft Reset option, described in *Section 5.2.2.2* of the *SCSI Specification*.

The Soft Reset option is designed to allow a SCSI Reset signal to correctly clear the SCSI bus, while allowing on-going system operations to continue without major interruptions. When the SCSI Reset occurs, any activity on the SCSI bus is immediately halted and all bus lines are cleared from the bus. After the reset condition ends, any operations in progress are again allowed to start up in the normal manner. No status or pointer information is destroyed. All disconnected commands are allowed to reselect and continue in the normal manner. This Soft Reset function allows a multiple initiator system to use reset to clear certain types of bus failures without damaging on-going tasks from any initiator.

The SCSI Soft Reset option is useful in multitasking systems that cannot tolerate the overhead of a complex reconfiguration and reinitialization after a normal reset operation. For the SCSI Soft Reset option to operate correctly, all SCSI devices that communicate on the SCSI bus must support the Soft Reset option. If any SCSI devices support the Hard Reset option, it is likely that operations will be terminated without warning and the system will have to time-out and monitor the requirement to restart some activities.

SCSI Hard Reset Option

The Hard Reset option is designed to restore all attached SCSI devices, including both hosts and peripheral devices, to their power-on reset state. All system activities that have not been

recorded on a non-volatile memory device or through another SCSI path are completely lost and must be restarted. The system must be completely reinitialized. For certain types of systems that frequently do back-up or check-point their transactions, that reinitialize quickly and easily, or that infrequently do resets, the Hard Reset option is appropriate.

The AHA-1540C Series responds to a SCSI Reset condition by executing only the Soft Reset option, but it notifies the host whenever a SCSI Reset condition has been established by interrupting to the host. The host then has the option of converting the Soft Reset to a Hard Reset by forcing the host adapter to clear all the on-going operations and return to its initial state. The host requests this by raising the SRST bit (bit 6 of the Host Adapter Control Port). The host must raise the SRST bit within 300 microseconds to disable the restarting of operations, according to the rules of Soft Reset. The raising of the SRST bit causes the host adapter to abandon all CCBs and prepare itself to begin accepting new instructions from the host. No secondary SCSI Reset signals are activated. The mailbox initialization and all normal SCSI initial conditions are reset by the SRST bit, so that reinitialization is required to restart the system. Of course, the system still has the right at any time that the IDLE bit (bit 4 of the Host Adapter Status Port) is on to execute any of the adapter commands and modify the Mailbox Address or the SCSI initial conditions.

If the host requires that the SCSI bus be reset according to the SCSI Hard Reset option, the host raises the HRST bit. The host adapter will then set a SCSI Reset condition on the SCSI Bus and clear all its CCB and status information, thereby performing a SCSI Hard Reset with a single load to the Host Adapter Control Port. Reinitialization will be required.

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Chapter Five

Firmware Description

Host Adapter Command Overview

The AHA-1540C Series supports two types of commands: *SCSI* and *Adapter*. SCSI commands are issued using the mailbox protocol and a Command Control Block. When SCSI commands are used, the AHA-1540C Series is operating in true multithreading mode. In this mode of operation, the AHA-1540C Series is capable of executing multiple commands for multiple targets concurrently. The AHA-1540C Series maximizes I/O transaction throughput by managing SCSI disconnection and reconnection.

Adapter commands are issued by writing to the Command/Data Out port. Most adapter commands cannot be issued when there are outstanding SCSI commands. Adapter commands are used to initialize the host adapter and to establish control conditions within the host adapter. Adapter commands are also used to transmit the special parameters for communication between the BIOS and the host adapter for the execution of Int 13h operations.

Adapter Command Operation Codes

Below is a list of the hexadecimal host adapter command operation codes.

Code (hexadecimal)	Command
00	No Operation
01	Mailbox Initialization
02	Start SCSI Command*
03	Start PC-AT BIOS Command
04	Adapter Inquiry†
05	Enable Mailbox Out Available Interrupt
06	Set Selection Time Out
07	Set Bus-On Time
08	Set Bus-Off Time
09	Set Transfer Speed
0A	Return Installed Devices
0B	Return Configuration Data
0C	Enable Target Mode
0D	Return Setup Data†
1A	Write Adapter Channel 2 FIFO Buffer
1B	Read Adapter Channel 2 FIFO Buffer

Code (hexadecimal)	Command
1C	Write Adapter Channel 1 FIFO buffer
1D	Read Adapter Channel 1 FIFO Buffer
1F	Echo Command Data
20	Adapter Diagnostic
21	Set Host Adapter Options
22	Set EEPROM†
23	Return EEPROM†
24	Enable Shadow RAM for Read/Write†
25	Initialize BIOS Mailbox†
26	Set BIOS Bank One†
27	Set BIOS Bank Two†
28	Return Extended BIOS Information†
29	Set Mailbox Interface Enable†
82	Start BIOS SCSI Command*†

*These commands can be issued while the host adapter is executing a SCSI command.
†Not supported by or operates differently with the AHA-1540B/1542B.

All host adapter commands except Start SCSI Command (02h) and Start BIOS SCSI Command (82h) must be executed only when the IDLE bit (Status bit 4) is one or when the host adapter is idle. Many commands require additional parameter bytes which are then written to the Command/Data Out I/O port (base + 1). Before each byte is written by the host to the host adapter, the host must verify that the CDF bit (Status bit 3) is zero, indicating that the command port is ready for another byte of information. The host adapter usually clears the Command/Data Out port within 100 microseconds. Some commands require information bytes to be returned from the host adapter to the host. In this case, the host monitors the DF bit (Status bit 2) to determine when the host adapter has placed a byte in the Data In I/O port for the host to read. The DF bit is reset automatically when the host reads the byte. The format of each adapter command is strictly defined, so the host adapter and host system can always agree upon the correct number of parameter bytes to be transferred during a command.

All adapter commands except Return Installed Devices, Start SCSI Command, and Start PC-AT BIOS Command typically require less than 200 microseconds to complete. Return Installed Devices typically completes in less than 3 seconds. Start SCSI Command and Start PC-AT Command completion times vary with the SCSI device and the command issued.

No Operation (Operation Code 00h)

No host adapter action is taken, but HACC is set indicating command completion. No additional information bytes are exchanged.

Mailbox Initialization (Operation Code 01h)

This command specifies the number of mailbox locations used by the host adapter and the base memory location of the mailbox area. The host adapter requires that four bytes of outbound data follow the command byte. The definition of those four bytes is shown below:

Byte	Definition
0	Mailbox count: Must be greater than zero.
1	Mailbox physical address (MSB)
2	Mailbox physical address
3	Mailbox physical address (LSB)
1, 2, 3	Mailbox address: Location of the first byte of the mailbox area.

When the Mailbox Initialization command and parameters are received, the host adapter assumes that the specified number of Mailbox Out entries and the same number of Mailbox In entries are assigned beginning at the mailbox address. The total number of bytes reserved for the mailbox area is eight times the Mailbox Count. If the Mailbox Count is zero, the INVDCMD and HACC bits are set to indicate that the parameter is invalid.

This command can be issued any time the host adapter is idle. It is typically used once after power-on.

At command completion, HACC is set to one and INIT is reset to zero. HACC is reset as specified in the *Interrupt Flag Port* section of Chapter Four, *Hardware Functional Description*.

Start SCSI Command (Operation Code 02h)

This command indicates that the host has made at least one Mailbox Out entry and that the host adapter should begin to scan for active MBO entries. Once scanning has been started, it continues until all MBO entries have been serviced, either by beginning the requested operations or by queuing the activities for later execution. Since it is not easy for the host to determine that scanning is still taking place, the host should normally issue this command every time a Mailbox Out is filled. This command does not require additional data bytes. To avoid unnecessary interrupts, HACC is *not* set after command completion. HACC and INVDCMD are set if the mailbox was not previously initialized.

Start PC-AT BIOS Command (Operation Code 03h)

This command is used by the Adaptec host adapter BIOS to communicate with the host adapter firmware. The command is reserved for use by the Adaptec host adapter BIOS.

Adapter Inquiry (Operation Code 04h)

After receiving this command, the host adapter returns four bytes of data describing the host adapter firmware revision level. After completing the transfer of the four bytes of inbound data, the HACC interrupt is set indicating normal command completion. The bytes contain the following information:

Byte	Description	Value	Meaning
00	Board Identification (ID) The value in this byte allows software supported on both the ISA bus and on the Micro Channel to distinguish the type of supporting host adapter.	00h	Board is an AHA-1540 with 16-Head BIOS
		30h ('0' ASCII)	Board is an AHA-1540 with 64-Head BIOS
		41h ('A' ASCII)	Board is an AHA-1540/1542, 64-Head BIOS
		42h ('B' ASCII)	Board is an AHA-1640, 64-Head BIOS
		43h ('C' ASCII)	Board is an AHA-1740A/1742A/1744 (standard mode)
		44h ('D' ASCII)	Board is an AHA-1540C/1542C
		45h ('E' ASCII)	Board is an AHA-1540CF/1542CF
		All Others	Reserved
01	Special Options Identification The value in this byte indicates what special options are supported on the AHA-1540C Series Host Adapter. Other host adapters use other values in this byte.	30h ('0' ASCII)	Board is standard model
		All Others	Reserved
02	Firmware Revision Level (First byte) This value contains an ASCII value from 0-9 that is the first digit of the firmware base code revision installed in the AHA-1540C Series .	Equal to released microcode version	N/A
03	Firmware Revision Level (Second byte) This value contains an ASCII value from 0-9 that is the second digit of the firmware base code revision installed in the AHA-1540C Series .	Equal to released microcode version; subset of First byte	N/A

After completing this command HACC is asserted, indicating normal completion.

Enable Mailbox-Out Available Interrupt (Operation Code 05h)

The Enable Mailbox Out Available Interrupt command specifies that a Mailbox Out Available interrupt to the host CPU should be generated whenever a Mailbox Out entry has been cleared by the host adapter. One byte of outbound data is transmitted to indicate whether the interrupt should be enabled or disabled.

Byte	Description
0	Enable/Disable Parameter (00h or 01h) This parameter byte, if set to 00h, prevents the Mailbox Out Available interrupt from being returned. If set to 01h, the Mailbox Out Available interrupt is returned as soon as a Mailbox Out has been cleared by the host adapter.

After completing this command, HACC is *not* asserted to avoid generating additional interrupts. If the data byte is not 00h or 01h, INVDCMD is asserted indicating an invalid command which also asserts HACC.

The Mailbox Out Available Interrupt command is intended to be used by the host as an indicator that the Mailbox Out entries have been found full by the host. It should be disabled soon after being issued. If used in other ways, the interrupt may generate a large number of relatively useless interrupts that must be serviced by the host CPU.

Set Selection Time Out (Operation Code 06h)

This command sets the SCSI selection time out value. The SCSI selection time-out value is used to determine whether or not a SCSI selection was successful. If the SCSI BSY signal is not returned within the specified time-out value, the selection is terminated and an appropriate error message posted with the returned CCB. This command expects four outbound data bytes to be provided as defined below:

<table>
<tr><th>Byte</th><th colspan="2">Description</th></tr>
<tr><td>00</td><td colspan="2">Enable/Disable Selection Time Out
This parameter byte specifies whether the selection time out is used. If the byte is set to 00h, no time out is performed. If the byte is set to 01h, the time specified in bytes 02 and 03 is used as the selection time out for the SCSI bus. The default value established by the reset process is 01h, indicating the time out is enabled.</td></tr>
<tr><td>01</td><td colspan="2">Reserved (00h)
This byte must be zero.</td></tr>
<tr><td>02</td><td>Time Out Value (MSB)</td><td rowspan="2">This two-byte value specifies the time in milliseconds that is used for the selection time out. The default value is 250 milliseconds.</td></tr>
<tr><td>03</td><td>Time Out Value (LSB)</td></tr>
</table>

After completing this command, HACC is asserted, indicating normal completion. INVDCMD is asserted, indicating an invalid command, if data byte 0 is neither 00h nor 01h or if byte 1 is not 00h.

Set Bus-On Time (Operation Code 07h)

This command specifies the time that the host adapter spends on the bus when transferring data. The Bus-On duration is adjustable from 2 to 15 microseconds. The default setting is 11 microseconds. One data byte is passed out to the host adapter to indicate the Bus-On duration in microseconds.

Byte	Description
0	Bus On-Time (2-15 microseconds)

After completing this command, HACC is asserted indicating normal completion. INVDCMD is asserted, indicating an invalid command, if the value is less than 2 or greater than 15. The valid range is 2 to 15 decimal.

Set Bus-Off Time (Operation Code 08h)

This command sets the time that the host adapter spends off the bus during a data transfer. The Bus-Off duration is adjustable from 1 to 64 microseconds. The default setting is 4 microseconds. After receiving this command, the host adapter expects one byte of data which specifies the bus-off time in microseconds.

Byte	Description
0	Bus Off-Time (1-64 microseconds)

After completing this command, HACC is asserted indicating normal completion. INVDCMD is asserted, indicating an invalid command, if the value is greater than 64. The valid range is 1 to 64 decimal. The actual time implemented by the host adapter is rounded down to the next four-microsecond step at or below the specified value. The minimum value is approximately one microsecond.

Set Transfer Speed (Operation Code 09h)

This command adjusts the bus master DMA circuitry to a specified maximum ISA bus transfer speed to and from the host memory. Any of several speeds may be selected with the **AT DMA Transfer Rate** option of the SCSI*Select*™ BIOS configuration utility. The speed selected from the SCSI*Select* BIOS configuration utility can be overridden if the Set Transfer Speed host adapter command is executed.

The single data byte transmitted after the Set Transfer Speed command byte either sets the read and write speed together, or establishes separate values for each. The default setting is the value set by the configuration program. The I/O Channel Ready signal automatically slows the system further if required by the host memory.

Data Byte 0	ISA Bus Transfer Speed		
00h	5.0 MBytes/second		
01h	6.7 MBytes/second		
02h	8.0 MBytes/second		
03h	10 MBytes/second		
04h	5.7 MBytes/second		
80-FFh	**Bit**		**Custom Transfer Speed**
	7	1	
	6-4	000	Read Pulse Width (ns) = 100
		001	Read Pulse Width (ns) = 150
		010	Read Pulse Width (ns) = 200
		011	Read Pulse Width (ns) = 250
		100	Read Pulse Width (ns) = 300
		101	Read Pulse Width (ns) = 350
		110	Read Pulse Width (ns) = 400
		111	Read Pulse Width (ns) = 450
	3	0	Strobe off time = 100ns
		1	Strobe off time = 150ns
	2-0	000	Write Pulse Width (ns) = 100
		001	Write Pulse Width (ns) = 150
		010	Write Pulse Width (ns) = 200
		011	Write Pulse Width (ns) = 250
		100	Write Pulse Width (ns) = 300
		101	Write Pulse Width (ns) = 350
		110	Write Pulse Width (ns) = 400
		111	Write Pulse Width (ns) = 450
FFh	3.3 MBytes/second		

After completing this command, HACC is set indicating normal completion.

Return Installed Devices (Operation Code 0Ah)

This command returns information about which SCSI Targets and Logical Units (LUNs) are installed on the SCSI bus. The host adapter issues the SCSI Test Unit Ready command to each target/LUN combination and reports the results using eight bytes of data returned through the Data In Register. Each byte is associated with the corresponding target. Each bit within a target byte is associated with a particular Logical Unit, bit 7 indicating the presence of LUN 7 and so forth. A bit value of one indicates that the associated LUN is installed. The state of each target is determined using the SCSI Test Unit Ready command by analyzing the returned data to determine if the addressed LUN is available.

After receiving this command, the host adapter returns eight bytes of information which specify the installed configuration as shown below:

Byte	Configuration	Bit	Meaning
0	Target 0	7	LUN 7 Installed
		6	LUN 6 Installed
		5	LUN 5 Installed
		4	LUN 4 Installed
		3	LUN 3 Installed
		2	LUN 2 Installed
		1	LUN 1 Installed
		0	LUN 0 Installed
1	Target 1		See Byte 0 for description
2	Target 2		See Byte 0 for description
3	Target 3		See Byte 0 for description
4	Target 4		See Byte 0 for description
5	Target 5		See Byte 0 for description
6	Target 6		See Byte 0 for description
7	Target 7		See Byte 0 for description

If, during the execution of this command, a target reports a status of Busy, the host adapter continues to reissue the command until either the drive reports not Busy, or one minute of time elapses. Commands are reissued at 250 millisecond intervals. The byte associated with the SCSI Device Identifier of the host adapter is always zero. After completing the information transfer, the HACC bit is set to indicate normal completion.

Return Configuration Data (Operation Code 0Bh)

The DMA arbitration priority, the Interrupt channel, and the SCSI ID of the adapter are returned by this command. The three bytes of information are returned in the following format:

Byte	Description	Bit	Meaning
0	DMA Arbitration Priority	7	Channel 7
		6	Channel 6
		5	Channel 5
		4-1	Reserved (0)
		0	Channel 0

Byte	Description	Bit	Meaning
1	Interrupt channel	7	Reserved (0)
		6	Interrupt channel 15
		5	Interrupt channel 14
		4	Reserved (0)
		3	Interrupt channel 12
		2	Interrupt channel 11
		1	Interrupt channel 10
		0	Interrupt channel 9
2	SCSI Identifier	7-3	Reserved (0)
		2-0	Binary value of SCSI Identifier

After completing this command, HACC is set to indicate normal completion.

Enable Target Mode (Operation Code 0Ch)

This host adapter command enables and disables Target Mode. The host adapter requires that two bytes of outbound information follow the command byte. The information bytes contain the following information:

Byte	Description	Bit	Meaning
0	Enable/Disable Target Mode Specifies which operating modes the host adapter uses. If set to 00h, the AHA-1540C Series operates in Initiator Mode only. This is the default value after a Hard Reset, Soft Reset, or Power-on Reset. If set to 01h, the host adapter operates both as an initiator and as a processor-type target SCSI device. Any other value is invalid.		
1	Logical Unit Mask (For bit value 1, LUN treated as installed. For bit value 0, LUN treated as not installed.)	7	Corresponds to LUN 7
		6	Corresponds to LUN 6
		5	Corresponds to LUN 5
		4	Corresponds to LUN 4
		3	Corresponds to LUN 3
		2	Corresponds to LUN 2
		1	Corresponds to LUN 1
		0	Corresponds to LUN 0

If the AHA-1540C Series host adapter does not have the Target Mode feature enabled, the host adapter indicates an invalid host adapter command. If an attempt is made to change from target mode while there are still target mode CCBs being processed by the host adapter, the host adapter posts an invalid host adapter command indication.

If the command disables Target Mode, the Logical Unit Mask byte is ignored. If the command enables Target Mode, the Logical Unit Mask byte must contain at least one bit, indicating the presence of at least one Logical Unit.

The SCSI Inquiry command provides an indication to other initiators that the Logical Unit is installed or not installed in byte 1 of the returned inquiry data.

If Target Mode is not enabled, the host adapter behaves on the SCSI interface as an ordinary SCSI initiator. Any attempt to select the host adapter results in a SCSI selection time-out. Most reset operations, including Soft Reset, Hard Reset, and Power-On Reset return the AHA-1540C Series Target Mode to the disabled state. SCSI Resets, generated by the host or by other SCSI devices, do not change the previously established enabled or disabled state of Target Mode.

Return Setup Data (Operation Code 0Dh)

This command returns information describing the setup of the host adapter. The information returned reflects either the values supplied by previous host adapter commands or default values. The command is followed by an outbound data transfer and an inbound data transfer. The outbound transfer is a one-byte parameter indicating the length of the required inbound data transfer. The inbound data transfer contains from zero to 255 bytes of information describing the setup of the host adapter. The inbound information normally transferred is truncated or padded with zeros as necessary to transfer the requested number of bytes.

Byte	Description	Meaning	
Outbound Data Byte			
00h	Data In Length	The number of data bytes requested can be from 0 to 255. A value of zero is accepted and 256 bytes are returned.	
Inbound Data Summary			
00h	SDT and Parity Status	Bit 0	In the AHA-1540C Series this bit is always returned as zero.
		Bit 1	If this bit is zero, parity checking on inbound SCSI transfers has been disabled. If this bit is one, parity checking on inbound SCSI transfers is enabled.
		Bit 2-7	Reserved (0)
01h	Transfer Speed	This byte returns the value passed in to the host adapter by the Set Transfer Speed command.	
02h	Bus On Time	Indicates the Bus On Time in microseconds.	
03h	Bus Off Time	Indicates the Bus Off Time specified by the Bus Off Time Value in microseconds.	
04h	Number of Mailboxes	The number of mailboxes established by a previous Mailbox Initialization command is returned in this byte. This number is 00h if the Mailbox Initialization command has not yet been successfully completed.	
05h	Mailbox Address (MSB)	The base address of the mailbox area established by a previous Mailbox Initialization command is returned in these bytes. The Most Significant Byte is byte 5. These bytes have no meaning if Mailbox Initialization has not yet been successfully completed.	
06h	Mailbox Address		
07h	Mailbox Address (LSB)		

Byte	Description	Meaning	
08h	Synchronous Transfer Agreements Returns information about the synchronous negotiation with target 0. The byte is 00h for the address of the host adapter.	Bit 7	Set to one if synchronous transfer has been negotiated. Set to zero if negotiation has not occurred.
		Bits 6-4	These bits contain a value between 0 and 7 that defines the synchronous transfer period according to the following equation. Period = 100 + 50 (value) nanoseconds
		Bits 3-0	These bits contain the negotiated offset value. The value is normally between 1 and 7. Zero indicates asynchronous transfer.
09h	Sync Neg, Target 1 Same as byte 8, for target 1	See Byte 8 for the bit description.	
0Ah	Sync Neg, Target 2 Same as byte 8, for target 2	See Byte 8 for the bit description.	
0Bh	Sync Neg, Target 3 Same as byte 8, for target 3	See Byte 8 for the bit description.	
0Ch	Sync Neg, Target 4 Same as byte 8, for target 4	See Byte 8 for the bit description.	
0Dh	Sync Neg, Target 5 Same as byte 8, for target 5	See Byte 8 for the bit description.	
0Eh	Sync Neg, Target 6 Same as byte 8, for target 6	See Byte 8 for the bit description.	
0Fh	Sync Neg, Target 7 Same as byte 8, for target 7	See Byte 8 for the bit description.	
10h	Disconnection Option	Each bit corresponds to a SCSI device, e.g., bit 0 corresponds to the device at SCSI address 0. When set to one, the host adapter prevents the SCSI device from disconnecting.	
11-24h	Customer Banner or Information	These bytes are reserved for customer-specific data.	
25h	Auto Retry Option	In the AHA-1540C Series this byte is returned as zero.	
26h	Switches on Board	Return the settings of the AHA-1540C Series board switches. If a switch is Off, zero is returned. Switch to bit mapping is as follows: Bit 0: ISA I/O port address select bit 0 Bit 1: ISA I/O port address select bit 1 Bit 2: ISA I/O port address select bit 2 Bit 3: Floppy enable/disable Bit 4: BIOS base address select bit 0 Bit 5: BIOS base address select bit 1 Bit 6: BIOS base address select bit 2 Bit 7: EEPROM read data	
27h	Firmware checksum	MSB	
28h	Firmware checksum	LSB	
29h, 2Ah, 2Bh	BIOS mailbox address	MSB MID LSB	
2C-FFh	Reserved (00h)		

If the command completes normally, the HACC interrupt is set to one. If the mailbox area has not been properly initialized, all 17 bytes are still requested by the host. If byte 4 (Number of Mailboxes) is zero, bytes 5-7 must be ignored.

Write Adapter Channel 2 FIFO Buffer (Operation Code 1Ah)

After receiving this command, the host adapter expects three outbound information bytes to be transferred which point to an area of 64 bytes in system RAM. The area pointed to is transferred to the host adapter's Channel 2 FIFO Buffer using the host adapter's DMA circuitry. After completing the transfer of the 64 bytes from the indicated buffer area to the host adapter, the HACC interrupt is set indicating normal completion. This command is used in conjunction with the Read Channel 2 FIFO Buffer command for host adapter diagnostics. The Channel 2 FIFO Buffer is used for transmission of all information between the host adapter and the host system except the actual data fields.

Byte	Description
0	Buffer area address, MSB
1	Buffer area address, MID
2	Buffer area address, LSB

Read Adapter Channel 2 FIFO Buffer (Operation Code 1Bh)

After receiving this command, the host adapter expects three outbound information bytes to be transferred which point to an area of 64 bytes in system RAM. The area pointed to is used as a buffer to receive 64 bytes of information transferred from the host adapter's Channel 2 FIFO Buffer to the host's memory using the host adapter's DMA circuitry. After completing the transfer of the 64 bytes from the Channel 2 FIFO Buffer to the indicated buffer area from the host adapter, the HACC interrupt is set indicating normal completion. This command is used in conjunction with the Write Adapter Channel 2 FIFO Buffer command for host adapter diagnostics.

Byte	Description
0	Buffer area address, MSB
1	Buffer area address, MID
2	Buffer area address, LSB

Write Adapter Channel 1 FIFO Buffer (Operation Code 1Ch)

After receiving this command, the host adapter expects three outbound information bytes to be transferred which point to an area of 54 bytes in system RAM. The area pointed to is transferred to the host adapter's channel 1 FIFO buffer using the host adapter's DMA circuitry. After completing the transfer of the 54 bytes from the indicated buffer area to the host adapter, the HACC interrupt is set indicating normal completion. This command is used in conjunction with the Read Adapter Channel 1 FIFO Buffer command for host adapter diagnostics.

Byte	Description
0	Buffer area address, MSB
1	Buffer area address, MID
2	Buffer area address, LSB

Read Adapter Channel 1 FIFO Buffer (Operation Code 1Dh)

After receiving this command, the host adapter expects three outbound information bytes to be transferred which point to an area of 54 bytes in system RAM. The area pointed to is used as a buffer to receive 54 bytes of information transferred from the host adapter's FIFO to the host's memory using the host adapter's DMA circuitry. After completing the transfer of the 54 bytes from the channel 1 FIFO to the indicated buffer area, the HACC interrupt is set indicating normal completion. This command is used in conjunction with the Write Adapter Channel 1 FIFO Buffer command for host adapter diagnostics.

Byte	Description
0	Buffer area address, MSB
1	Buffer area address, MID
2	Buffer area address, LSB

Echo Command Data (Operation Code 1Fh)

This command is used to test the Command/Data Out port, the Data In port, and the associated control bits in the other I/O Ports. After receiving this command, the host adapter expects one byte of outbound information to be transferred through the Command/Data Out port. The host adapter then sends (echoes) the same data value back to the host through the Data In port. After the host has read the data value provided on the Data In port, the host adapter generates the HACC interrupt to indicate normal command completion.

Outbound Data Summary		Inbound Data Summary	
Byte	Description	Byte	Description
0	Outbound Echo Value	1	Returned Echo Value

Adapter Diagnostic (Operation Code 20h)

This command causes the host adapter to perform its internal self-diagnostics. A host adapter Hard Reset is also executed, but without issuing a SCSI bus reset. The host adapter must be reinitialized after this command before normal operation is resumed.

After issuing this command, the host should monitor the Host Adapter Status port (Base+0 port) for command status. The host should first wait for the deassertion of the STST bit, indicating completion of self-diagnostics, and then wait for assertion of one or more of the following bits: DIAGF, IDLE, DF. If IDLE is asserted and DIAGF is unasserted, no error occurred during the diagnostic. If DIAGF or DF is asserted, an error occurred during the

diagnostic. In this event, the host must wait for assertion of DF, then read the error code returned through the Data In port (Base+1 port). The error code equals the number of the diagnostic test that failed. If there was no error, no data byte is returned.

After the host adapter completes execution of this command, it asserts the HACC and any Interrupt bits in the Host Adapter Status port (Base+2 port).

Set Host Adapter Options (Operation Code 21h)

This command provides the host a mechanism for specifying certain host adapter configuration options. The configuration parameters are sent to the host adapter via a parameter list following the command Opcode. The format of the list is described below:

Byte	Description
0	Length of remaining parameter list, in bytes. Equals the total list length minus one.
1	Disable SCSI Disconnection Option Each bit corresponds to a SCSI device, e.g., bit 0 corresponds to the device at SCSI address 0. When set to one, the host adapter prevented the SCSI device from disconnecting. When cleared to zero, disconnection is allowed. Byte 1 is mirrored back to the host as Byte 10h of the Return Setup Data Host Adapter command.

Additional bytes may be defined in the future. Presently, additional bytes are accepted without error, but are ignored.

Set EEPROM (Operation Code 22h)

This command provides the host a mechanism for changing the host adapter configuration. The SCSI*Select* configuration utility sends this command to change all or a few bytes of the configuration in the EEPROM. The firmware then updates the EEPROM in addition to the configuration registers in the AIC-7970.

The outbound transfer starts with two parameter bytes that indicate the length of the outbound data transfer and the offset from the beginning of the EEPROM respectively. One to 32 bytes of data to be written to the EEPROM are then sent to the host adapter. If a full 32 byte transfer is not required, the number of bytes supplied is 31 minus the offset value. An offset of zero transfers 32 bytes.

Byte	Description
0	Reserved (must be zero)
1	Number of outbound data bytes. Not the offset byte. This equals bytes 3 - *n*.
2	Offset from the beginning of the EEPROM
3 - *n*	Outbound data bytes.

Return EEPROM (Operation Code 23h)

This command provides the host a mechanism for reading the host adapter configuration. The information returned reflects either default EEPROM values or values set by a previous Set EEPROM command. The command byte is followed by an outbound data transfer and then an inbound data transfer. The outbound transfer contains three parameter bytes: the flag, the length of the required inbound data transfer, and an offset from beginning of the EEPROM. The inbound data transfer contains from zero to 31 bytes of information describing the configuration of the host adapter. The number of bytes transferred depends on the offset specified in byte one. An offset of zero transfers 32 bytes.

Byte	Description
0	Flag byte 1 = Return configured options 0 = Return default options
1	Number of inbound data bytes, not including the offset byte. This equals bytes 3 through *n*.
2	Offset from the beginning of the EEPROM.
3 - *n*	Inbound data bytes

Enable Shadow RAM for Read/Write (Operation Code 24h)

This command enables and disables Shadow RAM for read/write by the host CPU. Upon power-up the Shadow RAM is disabled. A Command Complete interrupt is not generated after executing this command. The HACC bit is set in the Interrupt Flag register.

Byte	Description	Bit 1 Bit 2	Meaning
0	Enable/Disable Shadow RAM	00	The read operation reads from BIOS EPROM. The write operation is disabled
		01	The read operation reads from BIOS EPROM. The write operation is disabled
		10	The read operation reads from Shadow RAM. The write operation is disabled
		11	The read operation reads from Shadow RAM. The write operation writes to Shadow RAM.

Initialize BIOS Mailbox (Operation Code 25h)

Reserved; only for use by the Adaptec BIOS.

Set BIOS Bank One (Operation Code 26h)

This command sets the BIOS bank. Upon power-on the BIOS is mapped in the 16 KByte BIOS address space set by the switches. This command is used by the BIOS to switch itself to bank one from bank two. A Command Complete interrupt is not generated. The HACC bit is set in the Interrupt Flag register. Although the Command Complete bit is set, the Any Interrupt bit is not set.

Set BIOS Bank Two (Operation Code 27h)

This command sets the BIOS bank. Upon power-on the BIOS is mapped into the 16 KByte BIOS address space set by the switches, as defined by bank one. This command is used by the BIOS to switch itself to bank two from bank one. After it has executed, the upper 16 KBytes of BIOS are mapped into the address space set by the switches. A Command Complete interrupt is not generated. The HACC bit is set in the Interrupt Flag register. The Command Complete bit is also set.

Return Extended BIOS Information (Operation Code 28h)

The Return Extended BIOS Information and Set Mailbox Interface Enable commands are used to protect against data corruption for the following cases:

- If support for drives greater than 1 Gigabyte is enabled and device drivers are used that do not support drives larger than 1 Gigabyte
- If dynamic scanning of the SCSI bus is enabled or if BIOS support for more than two drives under DOS 5.0 or greater is enabled

If greater than 1 Gigabyte support is enabled, the AHA-1540C Series BIOS disables the host adapter's mailbox initialization by sending a Set Mailbox Interface Enable command with byte 0, bit 0 set to 1 (disable mailbox initialization), and with byte 1 set to one of the defined lock codes (see sectiom *Set Mailbox Interface Enable (Operation Code 29h)*). To subsequently enable the mailbox interface (MBO and MBI, not the BIOS mailbox), a device driver must supply a matching lock code with a Set Mailbox Interface Enable command. This matching code is determined by the device driver using a Return Extended BIOS Information command.

A similar series of events occurs for the case where dynamic scanning is enabled or greater than two drive support under DOS 5.0 is enabled. In either of these cases, byte 0, bit 0 is set to 1 (disable mailbox initialization). However, byte 1 will be set to a different lock code than for the case where greater than 1 Gigabyte is enabled without a proper device driver. See the Set Mailbox Interface Enable command in the next section for a description of byte 1 assignments.

The host adapter firmware checks the lock code and if it matches, the host adapter accepts a Mailbox Initialization command (Opcode 01h) from the host. If the lock code does not match, the host adapter firmware treats a Mailbox Initialization command from the host as an invalid command. This latter case would generally occur if a driver is loaded that does not support the aforementioned attributes when they are enabled (i.e., drives larger than

1 Gigabyte, dynamic scanning of the SCSI bus or greater than 2 drives under DOS 5.0). The driver in this case would fail to load and data corruption would not occur.

The Return Extended BIOS Information command returns two bytes to the host, which are defined as follows:

Byte	Bit	Description
0	7-4	Reserved (returns zero)
	3	Extended BIOS translation (0=disabled, 1=enabled)
	2-0	Reserved (returns zero)
1	7-0	Mailbox Lock Code If this byte is set to 0, host adapter mailbox initialization is enabled. Otherwise, mailbox initialization is disabled and the value equals the lock code previously set by the BIOS with a Set Mailbox Interface Enable command.

Set Mailbox Interface Enable (Operation Code 29h)

The BIOS or device driver sends two bytes to the host adapter. These are defined as follows:

Byte	Bit	Description
0	7-1	Reserved (must be zero)
	0	When 0, mailbox initialization is enabled. When 1, mailbox initialization is disabled.
1	7-0	Mailbox Lock Code If set to 0, host adapter mailbox initialization is enabled. Otherwise, mailbox INIT is disabled and the value equals the lock code.

The Return Extended BIOS Information and Set Mailbox Interface Enable commands are used to protect against data corruption for the following cases:

- If support for drives greater than 1 Gigabyte is enabled and device drivers are used that do not support drives larger than 1 Gigabyte
- If dynamic scanning of the SCSI bus is enabled or if BIOS support for more than two drives under DOS 5.0 or greater is enabled

The Set Mailbox Interface Enable command is used in the following two ways:

1. To set the value used when the mailbox interface (MBO and MBI) is to be controlled by a lock code and to simultaneously lock that interface.

2. To unlock the mailbox interface with the lock code supplied by the Return Extended BIOS Information command (Opcode 28h).

Set Mailbox Interface Enable is used by the BIOS or device driver to disable the mailbox interface if byte 0, bit 0 is set to one. The lock code supplied with this command (in byte 1) is stored by the host adapter for later use when the interface is unlocked.

If a subsequent Set Mailbox Interface Enable command is received by the host adapter with byte 0, bit 0 cleared to zero, the mailbox initialization is enabled if the lock value supplied in byte 1 matches the value set with an earlier Set Mailbox Interface Enable command. Otherwise the firmware ignores the command and treats a Mailbox Initialization command (Opcode 01h) as invalid.

Note that zero is an invalid lock code value; all other values are valid lock codes. A driver should not re-enable the host adapter mailbox unless the meaning of the lock code is fully understood. Only the values in the following table are currently implemented:

Byte	Description
1	The AHA-1540B/1542B or AHA-1540C Series BIOS is using an extended BIOS translation algorithm with an Int 13h disk drive interface. This interface is used with drives larger than 1 Gigabyte in size.
2	Dynamic scanning of the SCSI bus enabled or BIOS support for more than two drives under DOS 5.0 enabled.
3-FFh	Reserved.

Start BIOS SCSI Command (Operation Code 82h)

Reserved; only for use by the Adaptec BIOS.

Mailbox Overview

The AHA-1540C Series uses a mailbox architecture for task communication between the host and the host adapter when executing SCSI commands. This allows the host adapter to perform multithreaded operations with a minimum of host intervention. The mailboxes are located in main system memory. Each mailbox entry is four bytes long. At power-on, the host issues an initialization command to inform the host of the mailbox location. There are always an equal number of outgoing mailboxes (MBOs) and incoming mailboxes (MBIs). The MBIs are located immediately after the MBOs. Initiator operations and target operations use the same mailboxes. Both initiator and target operations may be in process at the same time. A typical mailbox structure is shown in the following table.

Base Addr			
+0	Command	CCB 4 Pointer	MBO 0
+4	Command	CCB 2 Pointer	MBO 1
+8	00	Free Entry	MBO 2
+12	Command	CCB 3 Pointer	MBO 3
+16	00	Free Entry	MBI 0
+20	Status	CCB 1 Pointer	MBI 1
+24	00	Free Entry	MBI 2
+28	00	Free Entry	MBI 3

In this example, there are four MBOs and four MBIs. The Mailbox Count in the Mailbox Initialization command was set to four. The base address is the address specified by the Mailbox Address field.

> Note
> The Adaptec BIOS initializes the PC's DMA controller to accommodate bus master DMA. If the host adapter BIOS is removed or disabled, the host DMA controller must be initialized, via software, for bus master DMA operation. See the section titled *Description of Host Adapter Operation* later in this chapter.

Mailbox Out Definition

The first byte of each MBO contains the Mailbox status byte. The remaining three bytes contain an address pointer (which is a physical address) to the first byte of a Command Control Block (CCB). The CCB provides additional task control information. An MBO is free if the

first byte is zero. The host can make an entry in any free MBO and indicate that it is filled out or completed by placing the proper MBO command in the first byte of the MBO. After the MBO has been examined by the host adapter and all relevant information has been obtained, the host adapter sets the MBO command byte back to zero to allow the host to fill it again. For a multitasking operating system, the number of mailboxes should be sufficient to allow at least one mailbox for each active independent task or activity.

The MBO format is described in detail in the following table:

Byte	Description	Meaning	
0	MBO Command This byte specifies the state of the MBO entry.	00h	Mailbox Out is free
		01h	SCSI or host adapter command is to be started. CCB pointer indicates location of CCB to be processed.
		02h	SCSI or host adapter command is to be aborted. CCB pointer indicates location of CCB to be terminated.
1	CCB Pointer	MSB of physical address	
2	CCB Pointer	MID of physical address	
3	CCB Pointer	LSB of physical address	

For values of byte 0 other than those listed above, the host adapter simply sets byte 0 to 00h and ignores the Mailbox Out (MBO) entry. No corresponding Mailbox In is generated.

The use of Mailbox Out (MBO) entries to pass pointers to CCBs is identical for Target and Initiator Modes. The appropriate target mode CCB may be prepared early and posted to the host adapter in preparation for an operation that is expected to happen. If a SCSI operation occurs before the CCB is prepared, the host adapter processes as much of the transaction as possible, then requests a CCB from the host through the MBI. The host is fully responsible for preparing the correct CCB from the information provided through the MBI.

In Target Mode, one CCB may be present for each unique combination of LUN, initiator and direction. If a second CCB to the same LUN and initiator with the same direction bit is sent to the AHA-1540C Series, the CCB is returned with a host status of 19h, Duplicate CCB Received command.

An initiator-type CCB may be queued for a LUN and target. The host adapter is always searching for new MBO entries in a round-robin order, beginning with the entry after the last MBO entry that was processed. By always placing the MBO entries consecutively in the MBO area, the host can assure that the SCSI commands start with the minimum scan overhead. Initiator CCB queuing must be used with caution; under some circumstances it is possible for a CCB to be executed out of order.

If the Enable Mailbox Out Available interrupt (05h) is executed, the host takes one of the following actions after each MBO entry is freed by the host adapter:

- If the Any Interrupt bit in the Interrupt Flag port is zero, indicating that there are no interrupts pending, the Mailbox Out Available interrupt and Any Interrupt bit are set to indicate a hardware interrupt to the host.

- If the Mailbox Out Available interrupt is set to 1 by the previous clearing of a Mailbox Out entry and the interrupt has not yet been cleared by the host, the host adapter does not change the MBO interrupt bit and continues to scan for other stored MBO entries.
- If interrupts other than the Mailbox Out Available interrupt are pending, the host adapter waits for the pending interrupts to be cleared before setting the Mailbox Out Available interrupt. This guarantees that the MBO Available interrupt is not cleared accidentally when the host clears another interrupt.

Mailbox In Definition

The Mailbox In entries are used to pass completion information concerning a task from the host adapter to the host. In addition, requests for Target Mode CCBs are passed to the host using MBI entries. The first byte of each MBI contains the MBI Status byte, summarizing the type of information being passed from the host adapter to the host. The remaining three bytes contain specialized data that provides more detail about the information. In the case of a CCB Completed MBI, the bytes contain a pointer to the completed CCB. In the case of a CCB Required MBI, the bytes contain the information necessary for the host to prepare an appropriate CCB. Only those MBIs with an MBI Status that is non-zero have information for the host. When the host returns the MBI Status byte to zero, the MBI Free state, the host adapter is allowed to place a new set of information in the MBI entry.

When a SCSI command completes or if a new CCB is required, the host adapter scans the first byte of an MBI entry to find a free mailbox. If one is found, the host adapter updates the MBI's Status byte with a non-zero value and updates the following bytes with the appropriate required pointers or parameters.

The valid MBI formats are defined below:

Mailbox In Format for CCB Complete

Byte	Description	Meaning	
0	MBI Status This byte specifies the state of the MBI entry.	00h	Mailbox In is free.
		01h	CCB completed without error. CCB pointer indicates location of successfully completed CCB.
		02h	CCB aborted by host. CCB pointer indicates location of CCB that was aborted.
		03h	Aborted CCB not found. CCB pointer indicates the supposed location of the CCB that was to have been aborted. It is likely that the CCB was already presented to the host before the Abort CCB MBO entry was completed.
		04h	CCB completed with error. The CCB fields indicate the details of the error condition. This code allows normal CCB completion to be processed without bothering to examine the completion codes in the CCB.
1	CCB Pointer	MSB of physical address	
2	CCB Pointer	MID of physical address	
3	CCB Pointer	LSB of physical address	

Mailbox In Format for CCB Required

Byte	Definition	Meaning	
0	MBI Status	This byte specifies the state of the MBI entry.	
		10H	SCSI target command received with no CCB available. The host must prepare an appropriate CCB and place it in the MBO to complete the SCSI command. The remaining three bytes of the MBI specify the information necessary to prepare a SCSI command.
1	Initiator and LUN	Bits 7-5	Binary address of initiator that selected the host adapter in Target Mode.
		Bit 4	The SCSI target command received was a Receive command. A CCB must be prepared to transmit data to the initiator.
		Bit 3	The SCSI target command received was a Send command. A CCB must be prepared to transmit data from the initiator.
		Bits 2-0	Binary address of the logical unit of the Target Mode host adapter that was addressed by the initiator.
2-3	Data Length	The high-order two bytes of the data length specified in the Send or Receive command. A CCB must be prepared to transmit this amount of data plus up to 256 more bytes. It is assumed that the data fields are self-defining or of a known length in such protocols.	

The CCB Required MBI entries are only generated when a command has been received by the host adapter in target mode. For these CCB Required MBI entries, byte 0 takes on a distinctive value of 10h. This value indicates that the filled MBI entry is requesting a CCB appropriate for servicing a SCSI transaction for which no CCB was available at the host adapter. Pending receipt of this CCB, the host adapter will have disconnected from the SCSI bus after receiving the initiator and LUN addresses and either a SCSI Send or Receive command.

If the LUN address is enabled by the Logical Unit Mask, the host adapter places the LUN address in bits 7-5 (initiator) and bits 2-0 (target) and sets bit 3 or bit 4 to specify receipt of a SCSI Send or Receive command respectively. The host system is then expected to prepare a CCB suitable for processing the Send or Receive command. If the LUN address received with the SCSI Send or Receive command is disabled, no MBI is presented and a check condition is posted to the initiator. A subsequent Request Sense command will return an Invalid LUN error indication.

The information in bytes 2 and 3 of the MBI entry is a copy of bytes 2 and 3 of the Send or Receive command CDB. This gives the host an approximation of the length of the requested data transfer. This length is used by the host to allocate the correct amount of buffer to accept data in a Send command or to transfer in a Receive command.

After each MBI entry is stored by the host adapter, it indicates that MBI scanning must be performed in the following manner:

- If the Any Interrupt bit is not set to one in the Interrupt Flag port, indicating that no interrupts are pending, the host adapter sets the Mailbox In Full interrupt bit, the Any Interrupt bit, and raise the hardware interrupt line to indicate that there is at least one Mailbox In entry to be examined by the host system.
- If the Mailbox In Full interrupt bit has already been set to indicate that an entry was made in the Mailbox In area and if that interrupt has not yet been cleared by the host, no further notification is provided by the host adapter.
- If interrupts other than the Mailbox In Full interrupt are pending, the host adapter waits for all pending interrupts to be cleared before setting the Mailbox In Full interrupt.

Note

Careful host Target Mode software design is necessary to prevent ambiguity in the notification process. Consider the case in which a CCB was just prepared but the MBO containing it has not yet been searched by the host adapter. If the host adapter simultaneously creates an MBI entry requesting the CCB which is already stored in an MBO entry, the host may choose to examine the MBI entry and not act on it, having already provided the needed CCB. The host should also examine the entire MBI space to be sure that any previously supplied CCBs were not already used for other previous operations posted by the host adapter but not yet serviced by the host. Proper care in host system design prevents these overlapping operations from becoming a problem.

Command Block Definition

The CCB specifies detailed information about a SCSI command. The format of a CCB is shown below. Each of the fields is separately explained following the table.

Command Control Block Format

Byte	Description	Meaning	
0	Command Control Block Operation Code	See the following section titled *Byte 0: Command Control Block Operation Codes*. Also see the note below.	
1	Address and Direction Control	Bits 7-5	CCB Opcode = 00h, 02h, 03h, 04h: SCSI Target ID CCB Opcode = 01h: SCSI Initiator ID
		Bit 4	Outbound data transfer, length is checked.
		Bit 3	Inbound data transfer, length is checked.
		Bit 2-0	Logical Unit Number
2	SCSI Command Length		
3	Request Sense Allocation Length/Disable Auto Sense		
4-6	Data Length	Byte 4 most significant	
7-9	Data Pointer	Byte 7 most significant	
10-12	Link Pointer	Byte 10 most significant	
13	Command Linking Identifier		
14	Host Adapter Status (HASTAT)		
15	Target Device Status (TARSTAT)		
16-17	Reserved (00)		
18 - 18+m	SCSI Command Descriptor Block (CDB)	Length specified by byte 2	
18+m - 18+n+m	Allocated for Sense Data	Length of reserved space in byte 3	

Note

The AHA-1540C Series host adapters use individual bits of byte 0 of the CCB as defined in the section titled *Byte 0: Command Control Block Operation Codes*. This is different from the AHA-1540B/1542B host adapters, which treat all of byte 0 as an opcode. The AHA-1540C Series is backward compatible with software written for the AHA-1540B/1542B. For a full explanation of the use of byte 0 of the CCB by the AHA-1540B/1542B, see the *AHA-1540B / 1542B Technical Reference Manual*.

The standard format of the Command Control Block is shown in the following diagram:

Byte 0	Command Control Block Opcode			
1	Tar/Init	Data Out	Data In	LUN
2	SCSI Command Length = m			
3	Request Sense Allocation = n			
4	Data Length (MSB, MID, LSB)			
7	Data Pointer (MSB, MID, LSB)			
10	Link Pointer (MSB, MID, LSB)			
13	Command Link ID			
14	Host Status			
15	Target Status			
16	Reserved			
17	Reserved			
18	SCSI Command Bytes (m Bytes)			
18+m	Allocated for Sense Data (n Bytes)			

The bytes of the CCB are defined further below.

Byte 0: Command Control Block Operation Codes

The AHA-1540B/1542B defines all of byte 0 of the CCB as an opcode. Valid Opcode values for the AHA-1540B/1542B are:

Byte	Description
00h	SCSI Initiator Command Control Block
01h	SCSI Target Command Control Block
02h	SCSI Initiator Command Control Block with scatter/gather
03h	SCSI Initiator Command, residual data length returned
04h	SCSI Initiator Command with scatter/gather, residual data length returned
81h	SCSI bus device reset

The AHA-1540C Series CCB Opcode (Byte 0) is defined as follows:

7	6	5	4	3	2	1	0
BDRST	ND	Retry	Rsvd	Rsvd	Opcode		

The valid Opcode values for the AHA-1540C Series are:

Byte	Description
00h	SCSI Initiator Command Control Block
01h	SCSI Target Command Control Block
02h	SCSI Initiator Command Control Block with scatter/gather
03h	SCSI Initiator Command, residual data length returned
04h	SCSI Initiator Command with scatter/gather, residual data length returned

The Retry bit notifies the host adapter whether or not it should perform a retry on busy. A value of 0 indicates a busy retry should be performed. A value of 1 indicates the busy status should be returned in the Target Status field of the CCB, rather than retrying on busy.

> Note
> The time delay between retries is about 700 msec and the firmware is able to handle other CCB requests during this delay, including aborts.

The AHA-1540C Series SCSI*Select* BIOS configuration utility allows you to enable/disable SCSI disconnection on a per target basis. This is also accomplished with Opcode 21, Set Host Adapters option. If a target is configured to enable SCSI disconnection, setting the No Disconnect (ND) bit to 1 forces the host adapter to prevent disconnection on a per CCB basis. An ND bit value of 0 notifies the firmware to allow disconnection based on how the host adapter is configured. The Bus Device Reset flag (BDRST) tells the host adapter to generate a SCSI Bus Device reset message on the specified target (byte 1 of CCB). All other flags are ignored.

If the operation code value is 00h or 03h, the SCSI command specified in the Command Descriptor Block field of the CCB is executed against the addressed target/LUN. The other fields of the CCB support the required initiator functions of the AHA-1540C Series. Operation codes 00h and 03h differ only in the updating of bytes 4, 5, and 6 following completion of the command.

If the operation code value is 01h, the CCB services a Send or Receive command sent to the host adapter acting as a target with respect to another initiator. The values in the other fields are used to service Target Mode operation. If an operation code of 01h is specified to a host adapter that has not had its Target Mode enabled, the host adapter returns a Host Status indication of 18h, Invalid CCB Parameter.

If the operation code value is 02h or 04h, the SCSI command specified in the Command Descriptor Block field of the CCB is executed against the addressed target/LUN. The definition of the Data Length and the Data Pointer is modified to support the scatter/gather function. Operation codes 02h and 04h differ only in the updating of bytes 4, 5, and 6 following the completion of the command.

If the opcode value is 81h, a Bus Device Reset message is sent to the addressed target. This command forces the host adapter to abort all outstanding tasks against the selected target. All remaining CCB Bytes are ignored. The host adapter generates a Bus Device Reset message out to the specified target.

Any other command value generates a Host Adapter Detected Error (Host Status byte of 16h).

Byte 1: Address and Direction Control

This byte identifies the address of the devices that are to be serviced and provides information about the expected direction of data flow.

If the CCB is an Initiator CCB, this byte identifies the target SCSI device in bits 7,6, and 5. If the CCB is a Target CCB, the byte identifies the initiator with which the CCB is associated.

Bits 4 and 3 are set to determine the direction of data transfer. For an Initiator CCB, the direction of data transfer is established by the SCSI command being executed independent of the value of bits 3 and 4. For a Target CCB, if neither bit is set or both bits are set, the CCB is returned with an indication of Invalid CCB Parameters (18h) in the Host Status field, since each Target CCB must be identified as to whether it services a Send or a Receive command. If both bits are set for an Initiator CCB, the command must perform no data transfer. If only bit 3 is active, the data transfer is from the external SCSI device to the host adapter. If the CCB is a Target CCB, the data transfer occurs during a Data Out phase, while if the CCB is an Initiator CCB, the data transfer occurs during a Data In phase. If only bit 4 is active, the data transfer is from the host adapter and to the external SCSI device. If the CCB is a Target CCB, the data transfer occurs during a Data In phase, while if the CCB is an Initiator CCB, the data transfer occurs during a Data Out phase.

If bits 3 or 4 are set for an Initiator CCB, the data length is checked. If the amount of data transferred exceeds the specified amount, the CCB Host Status field contains an indication of Data Over/Under Run (12h). For a Processor Target Mode CCB, the handling of incorrect lengths is described in the section titled *Incorrect Length Management for Target Mode Operation* in Chapter Seven, *SCSI Features.*

If a data underrun/overrun condition occurs for an operation that accesses the drive's media (Read/Write, Extended Read/Write, Write and Verify) and the direction bits are set to zero, the host adapter completes the operation without error. However, some or all of the data specified by the host may not be transferred.

Caution

The appropriate direction bit should be set for all operations that access the drive's media.

Setting the correction bit enables the host adapter to check the length of the data transfer and if a data underrun/overrun condition occurs, the CCB is returned with an indication of Data Underrun/Overrun (12H) in the Host Status field. For operations that do not access the drive's media, the direction bits should be set to zero unless transfer length checking is

desired. Setting both direction bits to one should be used only when no data transfer is expected or suppression of data transfer is desired for Read operations.

If the CCB is an Initiator CCB, bits 2, 1, and 0 define the target Logical Unit to be addressed. If the target accepts an Identify message out, the value in bits 2, 1, and 0 is provided in the LUN field of the message byte. The LUN field in the SCSI Command Descriptor Block (CDB) is expected to be zero. If the target does not accept an Identify message out, the LUN field in the SCSI CDB must contain the correct Logical Unit address. SCSI devices with conformance level 2, including Common Command Set (CCS) disk drives and all SCSI-2 devices, always accept the Identify message out. The few SCSI devices not meeting those requirements must be examined on a case-by-case basis to determine whether the Logical Unit Address should be placed in CCB Byte 1 or in the CDB.

Byte 2: SCSI Command Length

This byte specifies the length, in bytes, of the SCSI Command Descriptor Block (CDB).

Byte 3: Request Sense Allocation Length

When a SCSI device terminates an operation with Check Condition status, it means that the device has error or status information as a result of execution of the operation. The SCSI specification indicates that a Request Sense command must be executed before any other command is executed to ensure that the host initiator obtains the error information. Since the AHA-1540C Series host adapter has the capability of queuing commands for execution, the host adapter itself must take charge of generating the Request Sense command. Automatic generation of Request Sense is disabled by specifying a value of 01h for the Request Sense Allocation Length.

This byte indicates the length, in bytes, of the area reserved for information that may be obtained by a Request Sense command. A value of 00h indicates that an allocation length of 14 bytes is to be used, sufficient to capture the sense key and error code of all normal extended sense type devices. A value of 01h requests that no automatic Request Sense be executed. The values from 02h to 07h are reserved. Values from 08h to FFh are valid allocation lengths. The value is used to notify the host adapter that the specified number of bytes have been reserved at the end of the CCB to receive possible Request Sense data bytes. The Request Sense also uses the indicated allocation length as its byte count in the Command Descriptor Block generated by the host adapter.

If an operation that treats the AHA-1540C Series adapter as a Target Mode device fails and presents a Check Condition status byte, the initiator should return a Request Sense command. The AHA-1540C Series adapter returns appropriate sense information in response to the command. If the command that originally failed was a Send or a Receive command, the same Request Sense information bytes that will later be sent to the initiator are also sent to the host when the CCB is returned. The sense information is placed in the specified Request Sense Allocation area with a length not exceeding the Request Sense Allocation Length.

Bytes 4, 5, 6: Data Length

These bytes determine the length, in bytes, of the data transfer. CCB host adapter error 12h is posted if a data overrun occurs.

If the CCB specifies a scatter/gather operation, the Data Length field contains the total number of bytes in the data segment list.

If the Opcode value is 00h or 02h, these bytes remain unchanged upon completion of the command. If the Opcode value is 01h, these bytes are set by the host adapter upon completion of the command to the number of bytes actually transferred. If the Operation Code value is 03h or 04h, these bytes are set by the host adapter upon completion of the command to the difference between the original Data Length, as specified by the host, and the actual number of bytes transferred across the SCSI bus. In the event of data overrun, these bytes are set to zero. For Opcode 04h, the original Data Length is the sum of all segment Data Lengths.

Bytes 7, 8, 9 : Data Pointer

These bytes specify the real address of the first byte of the data area to be used during the data phase of the SCSI command.

If the CCB specifies a scatter/gather operation, the Data Pointer field contains a pointer to the first byte of the data segment list.

Bytes 10, 11, 12: Link Pointer

These bytes are used when a SCSI command contains a Link or Link With Flag bit in the command. When a Linked command is completed, the host adapter uses the contents of this field as a pointer to the next CCB to execute. If the Linked Flag bit is set, an interrupt is generated before the next command is started. A completed CCB is always reported back in an MBI, but MBIF interrupts are only reported if the linked set of commands is finished or if a Link with Flag message is presented. There must be enough MBI entries to receive the entire set of linked commands.

Target Mode does not support the linking function.

Byte 13 : Command Link ID

This byte is used in conjunction with linked commands. It is set by the host to identify commands in a command chain.

Linking is not supported in Target Mode.

Byte 14 : Host Adapter Status

This byte is used to report the host adapter status (HASTAT), and is defined as follows:

Value	Definition
00h	No Host Adapter Error Detected The CCB was completed normally.
11h	Selection Time Out The initiator selection or target reselection was not complete within the set SCSI selection time out period.
12h	Data Overrun/Underrun The target attempted to transfer more data than was allocated by the Data Length field or the sum of the Scatter/Gather Data Length fields.
13h	Unexpected Bus Free The target dropped the SCSI Busy line at an unexpected time.
14h	Target Bus Phase Sequence Failure An invalid bus phase or bus phase sequence was requested by the target. The host adapter generates a SCSI reset condition, notifying the host with a SCRD interrupt.
16h	Invalid CCB Operation Code The first byte of the CCB was invalid. This usually indicates a software failure.
17h	Linked CCB does not have the same LUN A subsequent CCB of a set of linked CCBs does not specify the same LUN as the first.
18h	Invalid Target Direction Received from Host The direction of a Target Mode CCB was invalid.
19h	Duplicate CCB Received in Target Mode More than one CCB was received to service data transfer between the same target LUN and initiator SCSI ID in the same direction.
1Ah	Invalid CCB or Segment List Parameter A segment list with a zero length segment or invalid segment list boundaries was received. A CCB parameter was invalid.

Byte 15: Target Device Status

For an Initiator CCB, this byte is used to return the SCSI status byte sent to the host adapter from the initiator. If a SCSI command returns with Busy status, the normal recovery process is to execute the command again. The AHA-1540C Series adapter takes that burden off the host and periodically restarts the command automatically until the command completes with a status other than Busy.

For a Target Mode CCB, this byte is used to indicate to the host what status the host adapter returned to the initiator.

Target Status may have the following values:

Byte	Description
00h	Good Status
02h	Check Status (See Request Sense byte area)
08h	LUN Busy

Bytes 16-17: Reserved (must be 0)

Bytes 18 - 18+m: SCSI Command Descriptor Block

This field holds the SCSI Command Descriptor Block (CDB) as described in the SCSI specification. The length of this command is described in byte 02h. For Initiator Mode CCBs, the CDB provided by the host is transmitted to the target. For target mode CCBs, the CDB provided from the initiator is returned to the host in this space.

Byte 18+m - 18+n+m : Allocated for Sense Data

If a Check Status condition is detected by the AHA-1540C Series as it completes an operation on the SCSI bus, the host adapter automatically executes a Request Sense command with the data length specified by Request Sense Allocation Length. The actual bytes returned, up to the maximum indicated by the Request Sense Allocation Length, are placed in the area allocated for sense data. If the Request Sense Allocation Length is 01h, no Request Sense command is executed.

If the Request Sense command completed without a Check Status condition, the Target Status is set to Check Status, and the Host Status is set to 00h. If the Request Sense command completed with Check Status, the Target Status is set to Check Status, and the Host Status is set to 14h.

If a check condition is detected by the AHA-1540C Series while it is operating in Processor Target Mode, the same information that is later recovered by the initiator that received the Check Status is also placed in the area allocated for sense data so that the host processor is also aware of the failure.

Scatter/Gather List Definition

Using the normal CCB Operation Codes of 00h and 01h (SCSI Initiator and SCSI Target CCBs), the CCB itself contains a pointer to the first byte of a contiguous area of data of a specified length. The direction of transfer with respect to the data area and the checking of the length of the data transfer to the data area are both managed by the AHA-1540C Series according to the requirements of the particular mode and control bit setup.

With a scatter/gather Operation Code of 02h or 04h, the CCB contains a pointer to a list of data segments and the length of the list of data segments. The data segment list contains

pointers to the actual location in host memory of the data segments to be transferred as well as the precise length of each data segment. Each data segment list entry contains a three-byte pointer to the location of a data segment and three-byte length value telling how long that particular data segment shall be. The data segment list is arranged in the order in which data is gathered or distributed, the first pointer in the list being used first.

A typical data segment list is shown in the following table. This sample data segment list describes 4096 bytes distributed in four separate locations within system memory. The beginning of the data segment list is indicated by the data segment list pointer. The length of the data segment list (24 bytes) is contained in the Data Segment List Length field of the CCB.

	3 Bytes	3 Bytes
	(MSB) (LSB)	(MSB) (LSB)
Data Segment List Pointer	Segment 0 L=1024	Data Segment 0 Pointer
	Segment 1 L=2	Data Segment 1 Pointer
	Segment 2 L=2046	Data Segment 2 Pointer
	Segment 3 L=1024	Data Segment 3 Pointer

A data segment list can have from one to 255 segments. A list with 0 segments or a list with more than 255 segments causes an Invalid Segment List Error to be posted in the Host Status field.

The AHA-1540C Series has no constraints with regard to the data segment address boundaries and lengths that are allowed.

Description of Host Adapter Operation

This section summarizes how the AHA-1540C Series host adapter is initialized and how it interacts with the host during normal operation.

System Power-on Initialization

Local Interface

After a power-on reset, the processor on the host adapter reads the switches. The switch information for the I/O port address is written in the host address space. After the I/O port information is written, the local processor executes an internal diagnostic to verify basic board functions and posts the results to the host.

System Interface

After power-on reset the on-board system BIOS reads the port information from the host address space. The SCSI*Select* BIOS configuration utility reads the EEPROM information. This utility verifies the configuration information from the user. Once information is verified, the BIOS sends a command to store the information in the EEPROM. After the configuration is complete, the host adapter is initialized. If an on-board BIOS is not enabled the device driver polls the I/O port address space (base address +3) for the ASCII string *ADAP*. When the device driver finds all the host adapters, the host adapters are configured into the system.

After system initialization is finished, the I/O Command port initialization commands must be executed. The Mailbox Initialization command must be executed to assign the mailbox area. The Enable Target Mode command may optionally be executed if Target Mode is to be allowed.

Execution of Initiator Mode Operations

To begin an Initiator Mode SCSI command, the host first allocates a data buffer area. A CCB is then created to perform the desired operation to the correct peripheral device and a pointer to the data buffer area is placed in the CCB. Once the CCB is completely defined, the host places a pointer to the CCB in an empty MBO location, places an MBO full status in the MBO Status byte, and transmits a Start SCSI Command to the I/O Command port. If the host adapter is not already scanning the MBO for an active MBO entry, the Start SCSI Command to the I/O port causes it to begin scanning for such an entry.

After finding an active MBO entry, the AHA-1540C Series copies the MBO Command field contents and CCB pointer into its internal RAM and clears the MBO Command byte, freeing the mailbox. Up to 16 Initiator CCBs and 16 Target CCBs can be stored in the host adapter's internal RAM concurrently. The AHA-1540C Series maximizes SCSI bus utilization by starting the next available CCB as soon as the bus is free. Disconnection and reconnection on the bus are automatically taken care of by the AHA-1540C Series. As the host adapter starts the SCSI operation, it first determines if the addressed target/LUN is busy. If the target/LUN is busy, the command is placed in the task queue to be tried again later.

Commands are removed from the queue in the order they were received, establishing a First In First Out (FIFO) command execution order. The order of task completion may vary due to the different amounts of time required to process and complete different commands. If the target/LUN is not busy, the new command is started at the next bus free phase. If Busy status is received by the AHA-1540C Series, the CCB is placed at the end of the FIFO queue to be restarted later.

If a Check Condition status is received from the target, the AHA-1540C Series issues a Request Sense command to get the sense data. The sense data is stored in the CCB after the SCSI command data. The driver software must reserve the allocated number of bytes at the end of the CCB to hold the sense data which is returned as a result of receiving a Check status. Automatic Request Sense can be optionally disabled by using a field in the CCB.

If the MBO Command tells the host adapter to abort a SCSI command, the host adapter first searches the active and queued CCBs. If the CCB containing that command is found, the task is aborted at the earliest possible moment and an MBI entry is made to indicate that

the CCB's execution was successfully terminated. If the CCB containing the command to be aborted is not found among the active or queued CCBs, the AHA-1540C Series reports that fact in the MBI Status byte. The CCB may not be found because it has previously been aborted, because an intervening reset occurred, or because the CCB was already finished normally and returned.

The AHA-1540C Series scans the MBOs in a round-robin fashion. This is to ensure that all of the mailboxes are scanned with equal probability. A host can minimize the AHA-1540C Series MBO scan time by using MBOs sequentially.

When executing a Start SCSI Command, the AHA-1540C Series does not verify that the new CCB resides in an unused memory area. Therefore, the host must not re-use a CCB location until it has been returned through a Mailbox In entry and the host has examined all the pertinent information in the CCB. CCB addresses are used by the AHA-1540C Series as task identifiers.

Execution of Target Mode Operations

Target Mode With a Prepared CCB

Typical target operation is managed in the following way by the host software. After power-on initialization is complete, the host sends an Enable Target Mode command to the host adapter to enable Processor Target Mode. The host, from previous configuration knowledge, then generates a pair of CCBs for each likely initiator and for each LUN supported by the host. One CCB is for outbound data from the initiator using the Send command, while the other is for inbound data from the target to the initiator using the Receive command. The Send command CCB defines a data buffer for the expected network type command from the initiator. The Receive command CCB defines a set of data which is known and expected by the initiator, typically a welcome or configuration type message packet. The host adapter tests to be sure that duplicate CCBs are not provided by the host.

As the initiator finishes its initialization procedure, it requests availability and configuration information using the Test Unit Ready, Request Sense, and Inquiry commands. Finally, it may choose to address Send and Receive commands to the targets it has located to transmit or request information packets.

When the initiator executes a Send or a Receive command, the target accepts the selection on the SCSI bus, accepts the command from the initiator, and executes the proper data transfer to or from the area specified by the proper CCB. When all SCSI activity is finished successfully, the CCB is posted back to the host program by an entry in the MBI. The host adapter updates the CCB byte count and CDB field contents to correctly reflect the operation performed. The host is notified that there is an entry in the MBI by an interrupt from the host adapter. The host then prepares a new CCB to control the target's next activity expected from the initiator.

Target Mode Without a Prepared CCB

Alternatively, the processor-type device may be addressed by an initiator when no CCB has yet been prepared for use by the host adapter. If the host adapter command enabling Target Mode has not yet executed, the host adapter acts like any initiator. It accepts any selection sequence and any attempts to select it by its target ID causes the initiator to detect a selection time out.

If the host adapter has been enabled as a processor target by a host adapter command, any selection to the host adapter's target address is accepted. The availability commands and identification commands (Test Unit Ready, Request Sense, and Inquiry) are executed completely and normally. If a Send or Receive command is received while a CCB is not active, the processor target accepts the selection, obtains the Identify Message Out (to determine what Logical Unit has been selected), inputs the CDB from the SCSI bus, and then disconnects. A CCB may not be active at this time either because the host has not completed its program initialization or because the host has not finished analyzing the results of previous data transfers and generated a new CCB.

The CDB received by the host adapter in Target Mode is partially interpreted so the proper MBI can be generated to notify the host that a new CCB with a certain address, direction, and data length must be generated. When the new CCB is passed to the host adapter by an MBO entry, the CCB is filled with the command information, the host adapter reconnects to the SCSI bus, and the command is completed as described above.

DMA Channel Initialization

The DMA circuitry must be set to a special state to allow the bus master operation of the AHA-1540C Series to operate correctly. This state is normally established by the BIOS during initialization so that no other activity is required. If a DMA channel other than the default channel is being used or if the DMA channel is manipulated by other programs, the circuitry must be initialized in the following way before the AHA-1540C Series can be used.

For the DMA channel being used, 2 bytes of data must be written to the DMA controller port specified to initialize the host DMA controller for bus master DMA operation. The following table specifies these values in hexadecimal:

DMA Channel	DMA Controller Port	Data
0	0B	C0
	0A	00
5	D6	C1
	D4	01
6	D6	C2
	D4	02
7	D6	C3
	D4	03

Interrupt Initialization

This setup procedure is normally completed by the BIOS during initialization so that no other activity is required. If modifications to the interrupt handler are required, this information together with the programming information provided by the host system should be sufficient to properly setup the interrupt vectors.

The host adapter will drive one of several interrupts in the PC system. The particular interrupt used must be setup on power-up initialization and be properly managed during usage. The PC interrupts of interest to the host adapter driver along with their corresponding vector locations are summarized below. All these interrupts are handled by a slave interrupt controller. The master controller handles all system interrupts such as keyboard, timer, etc., and is assumed to be correctly initialized to allow interrupts by the slave controller. Upon receiving an interrupt, the processor will be vectored to the contents of the corresponding vector location.

Hardware Interrupt	Software Interrupt Vector Location
9	71h
10	72h
11	73h
12	74h
14	76h
15	77h

The interrupt is initialized by clearing the corresponding Interrupt Mask bit in the slave controller. The mask register is a read/write register, and only the bit of interest should be cleared. The port address is A1h, and the Interrupt Mask bit definitions are as follows:

Bit	Interrupt
0	8
1	9
2	10
3	11
4	12
5	13
6	14
7	15

Host Adapter Diagnostics

The AHA-1540C Series executes self-diagnostics upon power-on. These diagnostics test host adapter CPU operation, compute a checksum for the EPROM, and checks the data transfer path on the board. If switch positions 2, 3 and 4 are On (closed), the board performs a continuous self-test until the power is turned off. The following table shows the tests that are run. If a particular test fails, the test number displays in the data register of the port address at (base address + 1). In addition, the number of the test that failed is displayed using a number of successive flashes of the on-board LED followed by a pause.

Test Number and Flash Code	Test Description
1	Microcode EPROM checksum
2	RAM test
3	AIC-7970 register
4	FIFO1 Read and Write, FIFO to/from Microprocessor
5	FIFO1 Read and Write, Microprocessor to/from SCSI
6	FIFO2 Read and Write, FIFO to/from Microprocessor
7	EEPROM test

Chapter Six

On-board BIOS Interface

BIOS Command Execution Using Int 13h

On AT-compatible systems, disk I/O requests are passed from the operating system to the BIOS through software Int 13h. CPU registers are used to pass information about the desired operation and the associated parameters.

The AHA-1540C Series BIOS provides SCSI support by intercepting each interrupt and managing the request according to the drive address. If the drive is a floppy or internally installed fixed disk, the call is managed by the motherboard BIOS with no changes. If the selected drive is a SCSI disk drive, the request is handled by the Adaptec BIOS resident on the AHA-1540C Series. The AHA-1540CF/1542CF BIOS provides additional support for Floptical diskette drives on the SCSI bus.

> Note
> For concurrent operation, only calls to drive 81h (*D*) are handled by the AHA-1540C Series BIOS. However, in cases where DOS 5.0 or above is used, the AHA-1540C Series BIOS can handle calls to multiple drives (more than one drive may be supported under DOS 5.0 or above with the AHA-1540C Series). For nonconcurrent operation, calls to both drive 80h (*C*) and 81h (*D*) are managed by the AHA-1540C Series BIOS regardless of the DOS version.

On each Int 13h call, the correct host microprocessor registers are set by the operating system program to provide the required parameters to both the Adaptec BIOS and the motherboard BIOS. Most commands use the registers as indicated in the following table:

Register	**Function**
AH	BIOS Function Code
AL	Sector Count
CH	Low Byte of Cylinder Number
CL (Bits 7,6)	High Bits of Cylinder Number
CL (Bits 5-0)	Sector Number (1-based)
DH	Head Number
DL	Drive Number
ES:BX	Data Buffer Address

If, after sending a command to the drive, the drive reports a status of Busy, the host adapter continues reissuing the command until the drive reports Not Busy. Commands are reissued indefinitely at 700 millisecond intervals.

Physical to Logical Address Translation

As shown above, the starting disk sector address for read, write and verify requests is passed as a physical address including a 10-bit Cylinder Number, an 8-bit Head Number, and a 6-bit Sector Number. SCSI devices are addressed by logical block address without regard to the physical layout of the drive. For this reason, all SCSI devices are defined as drives with 64 heads and 32 sectors per track and with the appropriate number of cylinders to provide the full capacity of the drive using this physical to logical translation. The SCSI logical address is formed by the BIOS by concatenating the values as shown below:

Logical Block Address = Cylinder (10 bits) | | Head (6 bits) | | Sector (5 bits)

Maximum capacity under DOS is therefore 1024 cylinders, 64 heads, 32 sectors/track and 512 bytes per sector. This results in a maximum capacity of 1 Gigabyte. To control drives having a capacity greater than 1 Gigabyte, extended BIOS translation is enabled, as explained in the next section.

Extended BIOS Translation

Adaptec's extended translation feature provides support under DOS for drives with capacities to 8 Gigabytes. It does so by using a 1024 cylinder, 255 head and 63 sector translation scheme with drives controlled by the BIOS on the AHA-1540C Series host adapter. To enable extended BIOS translation, use the SCSI*Select* BIOS configuration utility.

Caution

Changing translation schemes on a drive that has already been partitioned erases all of the data on that drive. Backup any data on a drive before changing the partition method used for it.

Once you have enabled extended BIOS translation, run *Fdisk* under DOS to re-partition the drive. The cylinder size is now 8 MBytes and the partition size must be an integer multiple of this size. If you request a partition size that is not an integer multiple of 8 MBytes, *Fdisk* will round up to the nearest whole multiple of 8 MBytes.

Extended BIOS translation is not required with most newer versions of UNIX or with NetWare 386. These operating systems are not subject to the 1024 cylinder limitation of DOS.

The extended BIOS translation is for use with DOS version 5.0 (or later) only. Also, do not use extended translation with drives that contain two or more partitions formatted with different operating systems. In such a configuration, use standard translation and ensure that any DOS partitions are less than 1 Gigabyte in size. UNIX or NetWare 386 partitions can still be greater than 1 Gigabyte.

Virtual to Physical Buffer Address Translation

A data buffer address is passed to the BIOS via ES:BX. This virtual address can be easily translated into the physical address needed by a bus master device when the system processor is in real mode. Because this is the case at system boot time and under normal DOS operation, simple segment arithmetic is normally used to convert ES:BX to a physical address usable by the AHA-1540C Series:

Physical address = (Segment × 16) + Offset

The 386 processor, however has given rise to a large number of software products which use the 386 memory management feature to provide virtual 8086 operation. The address passed in ES:BX still appears valid to the BIOS, but the processor is not in fact in real mode, and normal segment arithmetic does not yield the correct physical location of the data buffer. This issue has been addressed by IBM and Microsoft® in a specification known as the Virtual DMA Services (VDS). This specification provides a method to the ROM BIOS for determining the physical location of a buffer given the segment:offset as well as its layout (it may not be contiguous). The AHA-1540C Series BIOS fully supports the VDS specification so that 386 memory management programs run without a driver as long as they are VDS compliant.

BIOS Command Return Codes

The BIOS command, when complete, returns control to the requesting program at the next instruction after the software interrupt. Upon return, the Carry Flag (CF) is set and a hex status code is located in register AH for examination by the requesting program.

The return codes placed in the AH register by the BIOS after executing a command are shown below:

AH (Hex)	Definition
00h	No Error. Operation completed successfully
01h	Invalid Function Request. The Int 13h function code provided was not valid or the drive number was out of range.
02h	Unable to Read Address Mark. One of the following additional sense codes (SCSI ASC) was presented in the sense information returned by the target: 12h - No AM Found in ID Field 13h - No AM Found in Data Field 21h - Illegal Logical Block Address
03h	Write Protect Error. Returned SCSI ASC: 27h - Data Protect
04h	Read Error. Returned SCSI ASC: 14h - No Record Found 16h - Data Sync Error
10h	Uncorrectable ECC Error. Returned SCSI ASC: 10h - ID ECC Error 11h - Unrecovered Read Error

AH (Hex)	Definition
11h	ECC Corrected Data Error. Returned SCSI ASC: 17h - Recovered Read Error without ECC 18h - Recovered Read Error with ECC 1Eh - Recovered ID with ECC Correction
20h	General Controller Failure. Returned SCSI ASC: 01h 03h 05h 06h 07h 08h 09h 1Bh 1Ch 1Dh 40h 41h 42h 43h 44h 47h 48h 49h
40h	Seek Operation Failed. Returned SCSI ASC: 02h - No Seek Complete 15h - Seek Positioning Error
80h	Time-out. Host adapter or device not responding to BIOS
AAh	Device Not Ready. Returned SCSI ASC: 04h - LUN not ready 29h - Unit Attention, Power on 2Ah - Unit Attention, Mode Select Change 45h - Select/reselect command failed 46h - Unsuccessful Soft Reset
BBh	Undefined Error Occurred. A SCSI ASC other than those listed was returned by the target.
CCh	Write Fault. Not returned by AHA-1540C Series BIOS
FFh	Sense Operation Failed. An error occurred issuing the SCSI Request Sense command to the target.

BIOS Disk Commands

The commands that can be accepted from the operating system by the host adapter BIOS include all those commands required for normal DOS operation, for booting of the DOS operating system, for booting of other operating systems, and for basic maintenance and verification of normal disk operation. The command set is summarized in the following table and each command is described in more detail in the sections below:

AH Register	Meaning
00h	Reset Disk System
01h	Read Status of Last Operation
02h	Read Desired Sectors into Memory
03h	Write Desired Sectors from Memory
04h	Verify Desired Sectors
06h	Identify SCSI Devices
08h	Read Drive Parameters
09h	Initialize Drive Pair Characteristics
0Ch	Seek
0Dh	Alternate Disk Reset
10h	Test Drive Ready

AH Register	Meaning
11h	Recalibrate
15h	Read DASD Type

The Format commands (AH = 05h, 07h, and 1Ah) are not supported by the AHA-1540C Series BIOS. The format operation is performed under a special format utility installed in ROM and initiated through the Debug program.

The Diagnostic Reserved commands (AH = 0Ah, 0Bh, 0Eh, 0Fh, 12h, and 14h) are not supported by the AHA-1540C Series BIOS.

The Park Heads command (AH = 19h) is not supported by the AHA-1540C Series BIOS.

The Reserved for Diskette commands (AH = 16h, 17h, 18h) and the commands from 1Bh up through FFh are not supported by the AHA-1540C Series BIOS. An attempt to execute any of these unsupported commands is terminated by the BIOS and an error code of 01h (Invalid Function Request) is returned in the AH register.

Reset Disk System

The BIOS is requested to reset the disk subsystem. This BIOS command is then passed on to the standard BIOS so that any internally installed fixed disk and floppy disk devices can also be reset. If the BIOS is operating concurrently with an internally installed fixed disk, the drive number is decremented by the AHA-1540C Series BIOS so that the standard BIOS does not attempt to reset a drive that is not installed.

Input Parameters:	AH = 00h DL = Drive Number
Output Parameters:	AH = Status of Operation CF = Return Code

Read Status of Last Operation

The status of the last operation performed to the specified disk is returned. No SCSI activity occurs. The disk status is reset to zero.

Input Parameters:	AH = 01h DL = Drive Number
Output Parameters:	AH = Status of Operation CF = Return Code

Read Desired Sectors Into Memory

The sectors requested by the parameters are read from the disk to the system memory. The SCSI command is executed as a Read (Extended) command (SCSI operation code 28h). If the operation fails and an error is reported through the BIOS status byte, the operation should be retried one time. If an error code of 11h (ECC Corrected Data Error) is returned, the data returned has been corrected and may be used with confidence. The table that follows shows the input and output parameters.

Input Parameters:	AH = 02h DH=Head CH=Cylinder DL=Drive Number CL=High Cylinder and Sector AL=Number of Sectors to Read ES:BX=Address of Buffer Area
Output Parameters:	AH=Status of Operation CF=Return Code

Write Desired Sectors from Memory

The sectors requested by the parameters are written from the system memory to the indicated disk. The SCSI command is executed as a Write (Extended) command (SCSI operation code 2Ah). If the operation fails and an error is reported through the BIOS status byte, the operation should be retried one time.

Input Parameters:	AH=03h DL=Drive Number DH=Head CH=Cylinder CL=High Cylinder and Sector AL=Number of Sectors to Write ES:BX=Address of Buffer Area
Output Parameters:	AH=Status of Operation CF=Return Code

Verify Desired Sectors

The sectors defined by the parameters are verified to be correctly written on the SCSI disk. The SCSI command is executed as a Verify command (SCSI operation code 2F) with the Byte Check bit set to zero. If the Verify command is not supported by the selected disk, the Verify Desired Sectors performs a SCSI Read command (SCSI operation code 28h) and throws away the received data. If the operation fails and an error is reported through the BIOS status byte, the operation should be retried one time.

Input Parameters:	AH=04h DL=Drive Number DH=Head CH=Cylinder CL=High Cylinder and Sector AL=Number of Sectors to Verify
Output Parameters:	AH=Status of Operation CF=Return Code

Identify SCSI Devices

This is a special AHA-1540B/1542B and AHA-1540C Series BIOS call that is used to return the number of the first supported SCSI drive. In the nonconcurrent case (2 SCSI drives), the returned value is 80h. If only one SCSI drive is installed, an additional returned value of 81h appears. The implementation of this command for the AHA-1540B/1542B is as follows:

Input Parameters:	AH=06h DL=Drive Number (81h)
Output Parameters:	AH=Status of Operation BL=First Drive Supported 80h=Nonconcurrent Operation 81h=Concurrent Operation

For the AHA-1540C Series, the syntax of this command is different. The first five bytes of the call (bytes 0-4 under ES:BX in the table below) are inspected by the BIOS upon entry. If these bytes are different from those listed in the table below, the BIOS treats the board as an AHA-1540B/1542B host adapter. If they match those listed in the table below, the board is assumed to be an AHA-1540C Series host adapter, and the following table applies:

Input Parameters:	AH=06h DL=Drive Number CL=0C0h CH=0FFh DH=0FFh ES:BX points to the buffer as follows: Set by Caller: Byte 0='A' Byte 1='D' Byte 2='P' Byte 3='T' Byte 4=Requested length of data to receive from BIOS Returned by BIOS: Byte 5=Actual length of data sent by BIOS to caller Bytes 6-13=Host Adapter ID Byte 14=Device Target ID Byte 15=LUN Byte 16=Host Adapter Location (LSB) Byte 17=Host Adapter Location (MSB)
Output Parameters:	AH=Status of Operation CF=Return Code

If the hexadecimal status code (AH) = 00h, and the CF is clear, then the following is returned by the BIOS to the caller:

- Actual length of data sent by BIOS to caller = 12 bytes (from byte 6 to byte 17)
- Host adapter ID = "AHA-1540" (the caller must verify that the character string in these 8 returned bytes specifies the correct model of host adapter)
- Target ID = SCSI target ID of given device (DL = drive number)
- LUN = SCSI LUN of given device, set to 0 (DL = drive number)
- Host Adapter Location = base port address of the host adapter

If the CF is set, the device is *not* controlled by an AHA-1540C Series host adapter.

Read Drive Parameters

A SCSI Read Capacity command is used to determine the maximum logical block of the selected drive. This information is then used to calculate the proper number of cylinders to be returned to the host system. Unless the drive size is greater than 1 Gigabyte (and support for drives greater than 1 Gigabyte is enabled), the number of heads returned is always 64 and the number of sectors per track is always 32. In the case where the drive size is greater than 1 Gigabyte, and this attribute is enabled in the SCSI*Select* BIOS configuration utility, the number of heads returned is always 255 and the number of sectors per track is always 63. The number of drives returned includes both internally installed drives and SCSI drives.

Input Parameters:	AH=08h DL=Drive Number
Output Parameters:	AH=Status of Operation DL= Number of BIOS Accessible Drives Attached (1 or 2) DH=Maximum Value for Head Number (3Fh) CH=Maximum Value for Cylinder Range (Low Byte) CL=Maximum value for Sector, High Cylinder Bits Bits 7,6 = High Order Cylinder Bits Bits 5-0 = Sector Number Maximum Value (20h) CF=Return Code

Initialize Drive Pair Characteristics

This command performs no operation, since SCSI CCS drives are self configuring.

Input Parameters:	AH=09h DL=Drive Number
Output Parameters:	AH=Status of Operation CF=Return Code

Seek

A seek to the logical block address defined by the physical parameters is performed. The seek is performed using the Seek (Extended) command (SCSI operation code 2Bh). The Seek commands are not mandatory CCS commands and are not required for proper functioning of SCSI devices. If the addressed disk drive reports an error indicating that the Seek (Extended) command is not supported, the BIOS command completes normally anyway. Since the seek operation is performed automatically by a Read or a Write operation, there is no need to generate a separate seek operation to access data.

Input Parameters:	AH=0Ch DL=Drive Number DH=Head CH=Cylinder CL=High Cylinder. (Sector Bits = 0)
Output Parameters:	AH=Status of Operation CF=Return Code

Alternate Disk Reset

The BIOS is requested to reset the disk subsystem. This BIOS command is then passed on to the standard BIOS so that any internally installed fixed disk and floppy disk devices can also be reset. If the BIOS is operating concurrently with an internally installed fixed disk, the drive number is decremented by the AHA-1540C Series BIOS so that the standard BIOS does not attempt to reset a drive that is not installed.

Input Parameters:	AH=0Dh DL=Drive Number
Output Parameters:	AH=Status of Operation CF=Return Code

Test Drive Ready

This BIOS command determines that the specified drive is available and ready by executing a Test Unit Ready command (SCSI operation code 00h) directed toward the SCSI device. The command may have to be executed a second time if a Unit Attention condition was detected during the first execution of Test Unit Ready.

Input Parameters:	AH=10h DL=Drive Number
Output Parameters:	AH=Status of Operation CF=Return Code

Recalibrate

This BIOS command transmits a Rezero Unit command (SCSI operation code 01h) to the specified drive. Since the Rezero Unit command is not a mandatory command and is not required for proper functioning of the SCSI device, the BIOS command completes without indicating an error even if the SCSI device indicates that the command is invalid.

Input Parameters:	AH=11h DL=Drive Number
Output Parameters:	AH=Status of Operation CF=Return Code

Read DASD Type

The AHA-1540C Series BIOS executes this command by sending an Inquiry (SCSI operation code 12h) and a Read Capacity (SCSI operation code 25h) command to the selected SCSI drive. The Inquiry command is used to verify that the device is a direct access storage device. The Read Capacity command is used to determine the number of logical blocks available. A special return format is used to obtain the required information.

Input Parameters:	AH=15h DL=Drive Number
Output Parameters:	AH=Status of Operation (Special Format) 00h Drive Not Present or DL Invalid 01h Reserved 02h Reserved 03h Fixed Disk Installed CX,DX=Number of 512 Byte Blocks Available on Disk CF=Return Code

Chapter Seven

SCSI Features

Initiator Mode SCSI Description

The AHA-1540C Series provides a very high performance SCSI interface connection. The host adapter meets the requirements of *ANSI Standard X3T9.2/86-109 Revision 10c*, which describes the SCSI bus. The host adapter additionally meets conformance level 2 of the specification. More specifically, the AHA-1540C Series accepts or manages the following:

- Command Complete
- Disconnect
- Message Reject
- Identify
- Save Data Pointer
- SCSI Bus Arbitration

The following alternatives are selected for the AHA-1540C Series SCSI interface connection from those described by *X3.131-1986*:

- Single-ended SCSI driver/receivers are used.
- Termination power on the AHA-1540C/1542C is supplied through a removable fuse. Termination power on the AHA-1540CF/1542CF is supplied through a self-resetting circuit breaker.
- Parity is always generated. SCSI Parity Checking can be disabled using the SCSI*Select*™ BIOS configuration utility.
- The Soft Reset option is always performed by the AHA-1540C Series. If the user desires to execute a Hard Reset instead, an interrupt service routine that detects the SCSI Reset Detected interrupt in the Interrupt Flags port must set the Soft Reset bit in the Control Port. This bit forces the host adapter to clear all SCSI-related operations, but does not require execution of the diagnostic functions. If the Soft Reset bit has been set, the host software must reinitialize the AHA-1540C Series.
- Synchronous data transfer is supported. Negotiation for the synchronous transfer initiated by another SCSI device is accepted by the AHA-1540C Series at any time. If synchronous negotiation has been enabled using the SCSI*Select* BIOS configuration utility, the AHA-1540C Series initiates synchronous data transfer negotiation when it detects that such negotiation may be required.
- Multitasking is fully supported.
- Modify Data Pointers is supported to allow Zero Latency Read operations.

In addition to these SCSI functions, the SCSI Common Command Set at level 4B is also supported. While this document was never made a standard, it describes a widely available set

of disk drive functions which are supported by the host adapter. The host adapter BIOS commands are all mapped into SCSI CCS commands to ensure proper support of the most common SCSI disk drives. The adapter command Return Installed Devices also uses CCS commands to determine which devices are available.

The draft ANSI standard for SCSI-2 has been used as a reference for the implementation of all SCSI functions with the expectation that the host adapter is fully compatible with the final version of the SCSI-2 standard. In particular, the processor-type device command set has been selected from the SCSI-2 manual for Target Mode operation.

Linked SCSI Commands

The AHA-1540C Series supports linking of SCSI commands in initiator mode. When the link bit in the SCSI command control byte is set, the target presents either a 0Ah or 0Bh message at command completion. The AHA-1540C Series uses the link pointer in a CCB to fetch another CCB. At the same time, the completed CCB status and address are stored in an MBI. If the target returns a 0Bh or 00h message, the AHA-1540C Series generates an interrupt to inform the host of the full MBI. If the target returns a 0Ah message, the MBIF interrupt is not posted until all linked commands are completed. The linked CCBs must address the same target and LUN since the target is not reselected.

Zero Latency Read Operation

The AHA-1540C Series implements zero latency operation through the use of Modify Data Pointer messages. Zero latency can eliminate rotational latency, depending on the length of the data transfer, by supporting out-of-order data transfers.

After seeking to the target track, the drive begins reading block IDs. If the first block ID is within range of the data transfer, but not the last block of the the data transfer, the drive begins reading the subsequent blocks into its buffer. Before transferring data, the drive issues a Modify Data Pointer message to the AHA-1540C Series. This supplies a positive argument that is added to the value of the current data pointer. The drive now sends this portion of the data transfer to the host. The drive resumes reading data into its buffer as soon as the first block of the data transfer is detected. Before sending this data to the host, the drive issues a second Modify Data Pointer message to the AHA-1540C Series which supplies a negative argument. This returns the data pointer to its original position. This guarantees that a data transfer of one track or less never requires more than a single revolution since data can now be transferred out of order.

SCSI Messages

The AHA-1540C Series host adapter supports a number of special messages in addition to the messages required to meet conformance level 2. Those messages are described in detail in the *SCSI Specification, X3.131-1986*, and in this section where they are used. The messages are summarized in the following table:

Function	Message	Cause
Standard Messages	Command Complete No Operation	Normal Sequencing
Error Management	Message Reject Bus Device Reset Abort Message Parity Error Initiator Detected Error	Invalid Messages Special CCB Special MBO Parity Error on Message Parity Error on Incoming Data
Disconnect/Reconnect	Identify Disconnect Save Data Pointer Restore Pointers	Normal Sequencing Normal Sequencing Normal Sequencing Special Sequencing/ZLR
Synchronous Transfer	Synchronous Data Transfer Request	Initialization Sequencing
Zero Latency Operation	Modify Data Pointers	ZLR Sequencing
Linked Commands	Linked Command Complete, Linked Command Complete with Flag	Command Linking Command Linking

Target Mode SCSI Description

Initiator Conformance Level Requirements

Initiators that execute commands against an AHA-1540C Series operating in Target Mode are required to have the following conformance levels, as described in *Appendix E* of the *SCSI Specification, ANSI X3.131-1986*. Conformance must be present with respect to each of the following items:

- The initiator must use single-ended drivers.
- Termination power may optionally be provided by the initiator, but must meet the SCSI specification in both its overcurrent protection and its reverse current diode protection. The terminators may be installed on the AHA-1540C Series board or installed as in-line terminators at the cable connectors.
- The implementation of parity is optional, but desirable.
- The initiator may support either Hard Reset or Soft Reset. All attached devices must support the same type of reset.
- The initiator must meet the requirements of conformance level 2. In particular, all LUN addressing must be performed by the Identify message, not by the LUN field in the CDB. Disconnection and reconnection must be supported.
- The initiator and target functions have the same SCSI ID.

Synchronous Transfer Support

The AHA-1540C/1542C supports only asynchronous transfers in Processor Target Mode.

The AHA-1540CF/1542CF supports synchronous transfers in Processor Target Mode if both the Fast SCSI and Synchronous Negotiation options are enabled via the SCSI*Select* BIOS configuration utility; asynchronous transfers are supported if the options are not enabled.

SCSI Target Operation in Processor Target Mode

When the AHA-1540C Series has been set to respond in Processor Target Mode, the host adapter appears on the SCSI bus as a normal processor-type device as defined by the SCSI specification. From one to eight LUNs may be supported, depending on the LUN mask byte in the Enable Target Mode command. Five SCSI commands are accepted:

- Test Unit Ready
- Request Sense
- Inquiry
- Send
- Receive

All other commands are rejected with Check Condition status. The sense information for rejected commands indicates a Sense Key of 05h (Illegal Request) with a Sense Code of 20h (Invalid Command Operation Code).

The commands that do not perform data transfer to or from the host are handled completely by the AHA-1540C Series with no CCB communication with the host system. These commands are the Test Unit Ready, Request Sense, and Inquiry. The Send and Receive commands must have a CCB from the host with the proper direction bits, the proper initiator address, and the proper LUN number to complete the SCSI operation. The Send and Receive CCBs may be provided to the host adapter before a command is received on the SCSI or may be requested after the command is received.

Each time an initiator activates a command to the AHA-1540C Series, an internal subchannel is activated to manage the command. The subchannel is dedicated to that particular LUN-initiator transaction until all operations associated with the command are completed. Such operations include disconnection to obtain a CCB, pending error conditions, and linked operations. If all subchannels are busy, a selection to the AHA-1540C Series results in the AHA-1540C Series accepting the command and then generating Busy status immediately. If this occurs, the initiator must reissue the command later.

SCSI Test Unit Ready Command

The Test Unit Ready command follows the SCSI specification in all respects. It is defined as follows:

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	Test Unit Ready Operation Code (00h)							
1	LUN (unused = 00)			Reserved (00)				
2	Reserved (00)							
3	Reserved (00)							
4	Reserved (00)							
5	Reserved (00)						Flag	Link

If the AHA-1540C Series has been initialized by the Enable Target Mode command to the Processor Target Mode, the command finishes normally with Good status and a Command Complete message. The host adapter supports the normal definition of Unit Attention on the first operation after power-on, after a SCSI reset, or after a Bus Device Reset.

If a Test Unit Ready command is executed against an LUN which was not allowed by the Enable Target Mode command, then Check Condition status is presented with sense data of Sense Key 5 (Invalid Request) and an Error Code of 25h (Invalid LUN). In order to minimize interference with peripheral devices. Test Unit Ready commands are issued only every 250 microseconds when waiting for a device to come ready.

SCSI Request Sense Command

If the AHA-1540C Series has returned Check Condition status to a previous command, the Request Sense command obtains the sense information associated with the error. This command is coded as follows:

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	Request Sense Operation Code (03h)							
1	LUN (unused = 00)			Reserved (00)				
2	Reserved (00)							
3	Reserved (00)							
4	Allocation Length							
5	Reserved (00)						Flag	Link

The returned sense information is sent in the extended sense format according to the SCSI standard. The data format is given in the following table:

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	Error Code (70h or F0h)							
1	Reserved (0)							
2	00		ILI	0	Sense Key			
3-6	Information Bytes (Residue)							
7	Additional Sense Length (06)							
8-11	Reserved (00000000h)							
12	Additional Sense Code							
13	Additional Sense Code Qualifier (00h)							

The following errors are detected and presented by the AHA-1540C Series while operating in Processor Target Mode:

Error	Sense Key (hex)	Additional Sense Code (hex)
No Sense Data	00	00
Invalid Command Operation Code	00	20
Invalid LUN	05	25
Invalid Command Parameter	05	26
Power-Up Attention	06	29
Reset Attention	06	29
Interface Parity Error	0B	47
Initiator Detected Error	0B	48
Dumb Initiator	05	2B

One set of error data may be buffered for each initiator-LUN association possible, up to a total of 56 sets of sense data. No Contingent Allegiance or Extended Contingent Allegiance state is established. The Error Code (Byte 0) is F0h if the residue field is valid and 70h if the residue field has no information.

The Incorrect Length Indicator (ILI) is set if an incorrect data transfer length is executed as described in the section titled *Incorrect Length Management for Target Mode Operation* later in this chapter. The residue is set equal to the transfer length requested in the initiator CDB minus the target host's specified data length specified as a 4-byte, two's complement number.

SCSI Inquiry Command

The Inquiry command provides the information necessary to uniquely identify the Adaptec AHA-1540C Series as a processor-type device. It is coded as follows:

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	Inquiry Operation Code (12h)							
1	LUN (unused = 00)			Reserved (00)				
2	Reserved (00)							
3	Reserved (00)							
4	Allocation Length							
5	Reserved (00)						Flag	Link

The information returned by the Inquiry command is supplied in the SCSI-2 format. The information described in the table below is returned to any selecting initiator from any selected AHA-1540C Series logical unit.

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	Peripheral Qualifier			Processor Device Type (03h)				
1	Reserved (00)							
2	Reserved (00)					ANSI v(02)		
3	Response Data Format (02h)							
4	Additional Length (1Dh)							
5	Reserved (00)							
6	Reserved (00)							
7	0	0	0	Sync = 1	Link = 1	0	0	0
8-15	Vendor Identification (ASCII) ADAPTEC *bbb*							
16-31	Product Identification (ASCII) AHA-1540*bbbbbbbb*							
32-35	Product Revision Level (ASCII)							

If the Inquiry command is attempted against a logical unit that has not been enabled as a target, byte 0 is returned as 23h, indicating that the LUN is not installed, but would be a processor device if it were installed. The remaining bytes are returned normally. If a length shorter than the required 36 bytes is specified by the Inquiry command, the number of bytes specified by the command is transferred. If a length longer than 36 bytes is specified, the command only transmits 36 bytes.

SCSI Send Command

The Send command transfers data from the initiator to the target. It uses the following format:

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	Send Operation Code (0Ah)							
1	LUN (unused = 00)			Reserved (00)				
2	Transfer Length (MSB)							
3	Transfer Length							
4	Transfer Length (LSB)							
5	Reserved (00)						Flag	Link

The information sent by an initiator to the AHA-1540C Series (acting as a target) is placed in the area specified by the appropriate CCB. If an appropriate CCB has not already been provided to the host adapter by the host software, an MBI entry requesting the appropriate CCB is sent to the host from the host adapter. In this case, the target host adapter disconnects from the SCSI until the CCB is made available to the host adapter through the MBO protocol. An appropriate CCB must have the same initiator ID, target LUN, and direction as that required to complete the command.

The transfer length in the Send command specifies the length in bytes of data that is sent during the Data Out phase. A transfer length of zero indicates that no data is sent. Management of incorrect length transfers is described in the section titled *Incorrect Length Management for Target Mode Operation* later in this chapter.

The CDB information is included in the returned CCB so that the receiving host programming can determine whether the information transmitted by the Send command was application data or asynchronous event notification data.

SCSI Receive Command

The Receive command transfers data from the target to the initiator. It has the following format:

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	Receive Operation Code (08h)							
1	LUN (unused = 00)			Reserved (00)				
2	Allocation Length (MSB)							
3	Allocation Length							
4	Allocation Length (LSB)							
5	Reserved (00)						Flag	Link

The information transmitted by the AHA-1540C Series (acting as target) to the initiator which issued the Receive command is taken from the area specified by the appropriate CCB. If an appropriate CCB has not already been provided by the host to the host adapter, an MBI entry requesting the appropriate CCB is sent to the host from the host adapter. In this case, the target host adapter disconnects from the SCSI bus until the CCB is made available to the host adapter through the MBO protocol. An appropriate CCB must have the same initiator ID, target LUN, and direction as that specified by the initiator.

The transfer length in the Receive command specifies the length in bytes of data that is sent during the Data In phase. A transfer length of zero indicates that no data is sent. Management of incorrect length transfers is described in the next section.

Incorrect Length Management for Target Mode Operation

The messages transmitted using the Send and Receive commands are expected to have a length previously agreed to by the initiator system software and by the target system software. If the transfer length specified by the command is equal to the transfer length specified by the CCB, normal operation takes place and no errors are posted.

If the transfer length specified by the initiator's command is shorter than the space defined by the target CCB, all data bytes expected and required by the initiator are transmitted. The target AHA-1540C Series indicates Good status on the SCSI bus at the end of the transfer. The target system's software, however, must be notified that the entire area of data defined by the CCB was not transmitted. A Target Status of Good is presented in the returned CCB. At the same time, the Incorrect Length Indication bit (bit 5 of byte 2) is set in the CCB Request Sense data area. Bytes 3 through 6 of the Request Sense data area contain the residue in two's complement notation equal to the length requested in the initiator command minus the length of the data area defined by the CCB. In this case, the residue is a negative number, since the requested length was less than the area specified by the CCB. The HA status stored in the CCB is 12h, indicating a Data Over/Under Run. The MBI Status byte is set to 04h to indicate that the CCB was completed with an error.

If the transfer length specified by the initiator's command is longer than the space defined by the target CCB, only those bytes contained within the CCB's data transfer area are transmitted. The target AHA-1540C Series indicates that not all bytes were transferred by flagging an error condition to the initiator. This is done by the target AHA-1540C Series using a SCSI status of Check Condition at the end of the data transfer. The Request Sense information transmitted to the initiator as a result of a Request Sense command (which immediately follows the data transfer) indicates that an incorrect length indication is present by setting bit 5 of byte 2. Bytes 3 through 6 of the Request Sense information transmitted to the initiator contain the residue in two's complement notation of the length requested in the initiator command minus the length of the data area defined by the target CCB. In this case, the residue is a positive number, since the requested length was greater than the available area. The target system's software must also be notified that the transfer length requested by the initiator exceeded the assigned buffer area. This is done by presenting to the host a Check Condition status in the returned target CCB. A Host Status of 12h is returned indicating a data over/under run. At the same time, the information that is later posted to the initiator with a Request Sense command is posted to the target system in the CCB Request Sense data area. This includes both the incorrect length indicator and the residue. The MBI Status Byte is set to 04h to indicate that the CCB completed with an error.

Aborting Target Mode Commands

The target host may abort a command by sending an MBO command of 02h to the host adapter. If execution of the command has not already been completed, the CCB is aborted and a MBI Status of 02h is returned to the host. Otherwise, an MBI status of 03h is returned.

The initiator may also abort commands by sending an abort message to the target. All CCBs, either received by or requested for the current initiator and LUN by the target host, as well as any corresponding commands received from that initiator, are aborted in such a case. An MBI status of 03h is then supplied to the host. Any CCB provided by the target host for which a corresponding initiator command has not been received is not aborted.

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Appendix A

Connector Pinout

Internal Connector Pin Assignments

AHA-1540C Series

Signal Name	Pin	Pin	Signal Name
Ground	1	2	-DB(0)
Ground	3	4	-DB(1)
Ground	5	6	-DB(2)
Ground	7	8	-DB(3)
Ground	9	10	-DB(4)
Ground	11	12	-DB(5)
Ground	13	14	-DB(6)
Ground	15	16	-DB(7)
Ground	17	18	-DB(P)
Ground	19	20	Ground
Ground	21	22	Ground
Ground	23	24	Ground
Open	25	26	Term Power (Fused)
Ground	27	28	Ground
Ground	29	30	Ground
Ground	31	32	-ATN
Ground	33	34	Ground
Ground	35	36	-BSY
Ground	37	38	-ACK
Ground	39	40	-RST
Ground	41	42	-MSG
Ground	43	44	-SEL
Ground	45	46	-C/D
Ground	47	48	-REQ
Ground	49	50	-I/O

External Connector Pin Assignments

AHA-1540C Series

Signal Name	Pin	Pin	Signal Name
Ground	1	26	-DB(0)
Ground	2	27	-DB(1)
Ground	3	28	-DB(2)
Ground	4	29	-DB(3)
Ground	5	30	-DB(4)
Ground	6	31	-DB(5)
Ground	7	32	-DB(6)
Ground	8	33	-DB(7)
Ground	9	34	-DB(P)
Ground	10	35	Ground
Ground	11	36	Ground
Ground	12	37	Reserved
Open	13	38	Term Power (Fused)
Ground	14	39	Reserved
Ground	15	40	Ground
Ground	16	41	-ATN
Ground	17	42	Ground
Ground	18	43	-BSY
Ground	19	44	-ACK
Ground	20	45	-RST
Ground	21	46	-MSG
Ground	22	47	-SEL
Ground	23	48	-C/D
Ground	24	49	-REQ
Ground	25	50	-I/O

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Appendix B

Floppy Disk Drive Interface

Interface Signals

Driver Output Signals		
V_{OL}	0 volts minimum	0.5 volts maximum
V_{OH}	Open collector	5.25 volts maximum
I_{OL}	60 mA	
I_{OH}	0.1 mA	
Receiver Input Signals		
V_{T-}	1.0 volts maximum	
V_{T+}	1.4 volts minimum	
Tied to +5 volt supply through 150 ohm resistors. Schmidt Trigger with 0.8-volt hysteresis		

Connector

Unshrouded 34-pin header. Partial list of compatible connector plugs (for reference only):

Manufacturer	**Model**	**Part Number**
3-M	N.A.	3414-6000
T&B Ansley	N.A.	609-3400M

The cable for the floppy connector should be good quality 34 conductor flat cable with 28 gauge conductors. Addressing of the second drive may be generated by twisting connector signals 10 through 16 or by changing jumpers in the floppy disk drives.

AHA-1542C and AHA-1542CF Only

The floppy disk controller allows the attachment of any standard IBM-compatible floppy disk drive to the AHA-1542C and AHA-1542CF. The floppy disk controller is accessed by the standard IBM-compatible BIOS through the standard IBM-compatible floppy diskette interface. The floppy disk controller section of the host adapter is completely independent of the SCSI host adapter functionality.

A floppy disk drive is attached to the host adapter using a 34-pin ribbon cable connector. The pinout of the cable is described in the following table. Some systems choose to use the same

address for all floppy disk drives and to twist the cable, pins 10-16, to switch the address lines at the drive.

Signal Name	Pin	Pin	Signal Name
Ground	1	2	-LD
Ground	3	4	Reserved
Ground	5	6	Reserved
Ground	7	8	-INDEX
Ground	9	10	MOTOR ENB DRIVE A
Ground	11	12	DRIVE SELECT B
Ground	13	14	DRIVE SELECT A
Ground	15	16	MOTOR ENB DRIVE B
Ground	17	18	-DIRECTION
Ground	19	20	-STEP
Ground	21	22	-WRITE DATA
Ground	23	24	-WRITE ENABLE
Ground	25	26	-TRACK 0
Ground	27	28	-WRITE PROTECT
Ground	29	30	-READ DATA
Ground	31	32	-HEAD SELECT
Ground	33	34	-DSKCHNG

AHA-1540CF/1542CF Only

The AHA-1540CF/1542CF on-board BIOS provides Floptical diskette drive control, but resides in the host PC BIOS address area.

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Appendix C

AHA-1540CF/1542CF Floptical Drive Support

General Support Features

In addition to all the features supported by the other AHA-1540C Series host adapters, the AHA-1540CF/1542CF also provides support for Floptical diskette drives. This appendix discusses AHA-1540CF/1542CF Floptical drive support features, and general information on Floptical drive characteristics.

- Floptical drives are only supported by the DOS (v.3.0 and above) and DOS/Windows operating systems at the time of this document's publication.
- Floptical support is enabled with the built-in SCSI*Select* BIOS configuration utility. Refer to the Adaptec *AHA-1540C Series User's Manual* for complete instructions on using SCSI*Select* and enabling BIOS Support for Floptical Drives.

Floptical Installation

Follow the regular SCSI peripheral device installation instructions in Chapter Three of this manual. Flopticals are SCSI devices and are installed in the same way as other SCSI devices.

The AHA-1540CF/1542CF allows you to install Floptical drives at any available SCSI ID. Remember to enable BIOS Support for Floptical Drives with the SCSI*Select* configuration utility.

Floptical Diskettes and The Host Adapter

The AHA-1540CF/1542CF BIOS supports standard 3.5-inch VHD (Very High Density) 21 MByte Floptical diskettes, without requiring driver software. The 3.5-inch Floptical drives also support 720 KByte and 1.44 MByte diskettes.

The AHA-1540CF/1542CF host adapter supports up to four floppy drives, including SCSI Floptical drives. You may choose your own mix of standard floppy and Floptical drives, up to four drives. Additional Floptical drives installed over four are recognized by the host adapter, but not directly accessible. *Swapping Active Flopticals*, later in this chapter has instructions on how to easily switch back and forth between extra Flopticals and Flopticals installed within the limit of four.

Floppy Device Drive Assignment

Drives *A* and *B* are reserved for flexible diskette drives in the DOS environment and may be assigned to either standard diskette drives or Floptical drives.

When one Floptical drive is installed, it is recognized as the first, second, or third floppy, depending on the number of standard floppy drives installed in the system.

A Floptical drive may be configured as the bootable *A* drive, with a standard (non-SCSI) floppy drive installed as floppy *B*. This is possible only if your system CMOS Setup utility allows you to configure a standard floppy as *B* without setting a standard *A*.

When two Floptical drives are installed, they are recognized by the operating system as the first and second, second and third, or third and fourth floppy drives, depending on the number of standard floppy drives installed.

Note that when a Floptical drive is added to the system as the third or fourth floppy device, the DOS logical drive designator (*A, B, C,* etc.) assigned to the Floptical is dependent on the DOS version. In general, versions of DOS prior to 5.0 map third and fourth floppy drives *before* hard disk drives. DOS versions 5.0 and later map third and fourth floppy drives after the hard disk drives.

For example, in a system with two standard floppies, one hard disk, and one Floptical drive, drive letters are assigned as follows:

Drive	DOS 3.*x* and 4.*x*	Drive	DOS 5.0 and above
A	First Floppy	***A***	First Floppy
B	Second Floppy	***B***	Second Floppy
C	Floptical	***C***	Hard Disk
D	Hard Disk	***D***	Floptical

Giving drive-letter assignment some thought before installation can make computer operation easier. Some application programs as well as statements in your *config.sys* and *autoexec.bat* files designate source file locations with drive-letter and directory pathnames.

VHD Format

The Adaptec VHD Format utility (*vhdfmt.exe*) is a DOS application program that performs low-level format (if needed), partitioning, and high-level formatting of Floptical VHD diskettes. The *vhdfmt* program is provided because DOS 5.0 and earlier versions of DOS do not recognize VHD media.

Use your standard DOS Format utility to format 720 KByte and 1.44 MByte diskettes. *Vhdfmt.exe* is *not* intended to be used with standard non-VHD diskettes.

Enter the following at the DOS command line to see an on-screen listing of the VHD Format command line options:

```
vhdfmt /?
```

Vhdfmt.exe will be included in a future version of Adaptec EZ-SCSI software; until then, *vhdfmt* can be easily obtained from the Adaptec Technical Support BBS (electronic Bulletin Board Service). The BBS can be reached from 5:00 a.m. to midnight, every day, at: (408) 945-7727. Baud rates: 1200/2400/9600, 8 data bits, 1 stop bit, no parity.

The SCSI*Select* SCSI Disk Utilities Format Disk option may also be used to low-level format VHD diskettes.

Swapping Active Flopticals

If you have more than four floppy devices and SCSI Flopticals installed, the host adapter may not allow you to access one or more Flopticals. When you start the computer, the host adapter BIOS banner device listing will report your extra Floptical(s) with a message similar to:

SCSI ID #*x–device name*– Not attached, maximum floppy count

Ignore in BIOS Scan, in the SCSI*Select* SCSI Device Configuration menu, allows you to select the SCSI ID of any installed SCSI devices that you do not want to be attached to and controlled by the host adapter BIOS. If you use Ignore in BIOS Scan to mask a Floptical's SCSI ID, the host adapter can access one of the Flopticals previously counted as being over the limit of four.

1. Start your computer and press **Ctrl-A** at the host adapter BIOS banner. AHA-1540C/1542C users with international keyboards may have to press **Ctrl-Q** (if **Ctrl-A** does not work, try **Ctrl-Q**).

2. Select **Host Adapter Port Address** and press **Enter**. If you have only one host adapter, just press **Enter**.

3. Press **Enter** again to access Configure/View Host Adapter Settings.

4. Access **Advanced Configuration Options** and set Dynamically Scan SCSI Bus for BIOS Devices to **Enabled**.

5. Press **Esc** to return to Configure/View Host Adapter Settings.

6. Access **SCSI Device Configuration**. Move the cursor to Ignore In BIOS Scan. Select the SCSI ID of the installed Floptical to be ignored. Change the setting to **Yes**. (Make sure the ID of the Floptical to be made accessible is not set to Yes.)

7. Press **Esc** to exit. Move the cursor to **Yes** when asked to save changes. Your computer will reboot.

Note the changes when the BIOS banner appears. The Floptical previously *not attached*, will now be recognized. And, the new unattached Floptical will be the one previously recognized.

> Note
> Dynamically Scan SCSI Bus for BIOS Devices must be set to Enabled in order to use Ignore in BIOS Scan to mask SCSI IDs.

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Glossary

Adaptec EZ-SCSI
A user-friendly SCSI software installation program for the DOS and/or Windows platform. EZ-SCSI automatically installs SCSI devices such as fixed disks and CD-ROM drives. Adaptec EZ-SCSI copies the required software programs to the PC's fixed disk and edits the configuration files so the host adapter can access the devices.

Adapter Command
A command transmitted to the host adapter using the Command/Data Out port and the Data In port. The commands are sequenced using the Control port, the Status port, and the Interrupt Flag port. Abbreviated as IOCP command.

Advanced SCSI Programming Interface
See ASPI.

AEN
See Asynchronous Event Notification.

AHA-1540C/1542C
The Adaptec ISA-to-SCSI host adapter for connecting SCSI devices to the ISA (PC-AT compatible) *or* EISA bus. The AHA-1540C/1542C is an enhancement of the AHA-1540B/1542B. The AHA-1542C floppy controller allows connection of standard IBM-compatible floppy disk devices to the host adapter.

AHA-1540CF/1542CF
The AHA-1540C/1542C enhanced with the addition of BIOS support for Floptical diskette drives and Fast SCSI devices. The AHA-1542CF has an improved floppy controller and added BIOS support for an alternate floppy controller I/O address.

AHA-1740A/1742A/1744
The Adaptec SCSI-to-EISA host adapter exclusively for connection to the EISA (Extended Industry Standard Architecture) bus. The AHA-1740A/1742A/1744 works only on EISA bus computers.

ASPI
Advanced SCSI Programming Interface. A software architecture which permits device modules to migrate across different hardware by communicating with the hardware through a pass-through interface to a manager written to the specific hardware.

Asynchronous Data Transfer
Data transfer performed by the SCSI interface involving the interlocking of a signal to the initiator (REQ) and a signal to the target (ACK) such that each step of the data transfer protocol must occur before the next step can begin. Asynchronous transfers are characterized by a low data rate and independence of external timing constraints, including cable length and circuit response times.

Asynchronous Event Notification
A process by which a target can send unsolicited sense information to an initiator using the Send command in order to inform the initiator about the occurrence of an important unusual occurrence.

AT Bus
The Industry Standard Architecture (ISA) bus.

Bus Device Reset
A SCSI message that clears all activity in the target to which it is addressed.

Byte
An eight-bit unit of data. An octet. A byte is normally the smallest addressable unit of memory and the unit of transfer on the SCSI bus.

CCB
See Command Control Block

CCS
See Common Command Set

CDB
See Command Descriptor Block

Command Control Block
A software object prepared by the host microcomputer software for the host adapter to provide all the control information it needs to execute a SCSI command. Abbreviated CCB.

Command Descriptor Block
A block of information passed across the SCSI bus to provide the command, parameter, and address information necessary for the target to execute the desired functions. It is prepared by the host software and placed in the CCB to be passed to the target by the host adapter. Abbreviated CDB.

Common Command Set
A defacto standard SCSI command set for communication with fixed disk drives. The Common Command Set (CCS) is the basis for the SCSI-2 command set for all types of peripheral devices.

Configuration
The operation of configuring a device on the bus through access of registers in the device by the host. It replaces the method of using jumpers common on ISA bus devices.

Control Microprocessor
An integrated circuit computer used to execute the software that controls the host adapter's operation.

Device Driver
A program that is linked with, or attached to, an operating system to map the software interface of the operating system to the requirements of attached peripheral devices and host adapters. Under ASPI, the main component associated with the board is known as a Manager.

Differential
A term referring to the electrical characteristics of the signals used on the SCSI bus interface. Differential signals occupy two conductors with a positive (+) and negative (-) polarity signal component respectively. This minimizes the effect of common mode signal noise and allows the SCSI bus to operate reliably over greater distances at a higher speed.

Direct Memory Access
A mechanism that allows hardware control of the transfer of streams of data to or from the main memory of a computing system. The mechanism may require setup by the host software. After initialization, it automatically sequences the required data transfer and provides the necessary address information. Abbreviated DMA.

DMA
See Direct Memory Access

EEPROM
Electrically-Erasable Programmable Read Only Memory. An integrated circuit used to store the host adapter firmware, which allows both mode download and firmware upgrade while in-circuit.

EPROM
Erasable Programmable Read-Only Memory. An integrated circuit used to store the host adapter BIOS.

FIFO
First In/First Out. A queuing order in which items are removed from the queue for execution in the same order in which they are placed in the queue. This is implemented with an integrated circuit that buffers data in such a manner that each byte placed in the buffer is removed from the buffer in the same order.

Firmware
The software that controls and manages the host adapter. It is *firm* as opposed to *soft* because it is designed into the host adapter and cannot be modified by the user.

Floptical
The VHD (Very High Density) 3.5-inch diskette alternative. Floptical drives currently support 21 MByte VHD diskettes, as well as 720 KByte and 1.44 MByte standard 3.5-inch diskettes. Floptical drive heads are precisely positioned through the combined use of optical servo track positioning and magnetic read/write technology, allowing for far greater data density and lower access times than those of standard diskettes.

Host
A microcomputer in which a host adapter is installed. The host uses software to request the services of the host adapter in transferring information to and from peripheral devices attached to the SCSI bus connector of the host adapter.

Host Adapter
A hardware printed circuit board that installs in a standard microcomputer backplane and provides a SCSI bus connection so that SCSI devices can be connected to the microcomputer. A host adapter is *intelligent* if it has a simple high-level software interface to the microcomputer. A host adapter is *dumb* if the microcomputer must directly manage the SCSI protocol using the microcomputer processor.

IBM PC-AT Compatible
Any computer system that exactly emulates the IBM PC-AT and that uses an ISA backplane bus.

Industry Standard Architecture
The IBM PC-AT functions have been duplicated by a number of manufacturers. All the IBM PC-AT compatible machines use a backplane bus that very closely emulates the function of the backplane bus of the PC-AT. Because of the broad usage of this bus structure, it has become known as the Industry Standard Architecture (ISA) bus, even though there is no presently accepted standard for the bus.

Initiator
A SCSI device that requests an operation to be performed by another SCSI device (the target). The initiator provides all the command information and parameters required to perform the operation, but the details of the operation are actually sequenced by the target.

ISA
See Industry Standard Architecture

Logical Unit
A physical or virtual device addressed through a target.

Logical Unit Number
An encoded three-bit identifier for a logical unit.

LU
See Logical Unit

LUN
See Logical Unit Number

Mailbox In
An area in main memory assigned by the host microcomputer software for communication with the host adapter. The host adapter places status and pointer information in entries in the Mailbox In (MBI) to indicate to the host microcomputer what operations have been completed or what information must be obtained from the host microcomputer.

Mailbox Out
An area in main memory assigned by the host microcomputer software for communication with the host adapter. The microcomputer software places commands and pointer information in entries in the Mailbox Out (MBO) to indicate what operations should be started by the host adapter.

Manager
The component of a driver which is specific to a particular board architecture and presents a standard ASPI pass-through interface for use by the peripheral-specific component of the driver, known as a module.

MBI
See Mailbox In.

MBO
See Mailbox Out.

Multitasking Operation
The execution of commands in such a way that more than one command is in progress at the same time, allowing the system to take advantage of overlapping activities by using resources that are temporarily not required for other operations. More than one program or more than one portion of a program may be operating in parallel.

PC-AT
A family of small computers sold by IBM, also called the Personal Computer/AT family of computers.

RAM
Random Access Memory. Memory of which any byte can be accessed directly in a single memory cycle. Information can be read from and written to the memory.

SCSI
Small Computer System Interface.

SCSI ASC
SCSI Additional Sense Code. Byte 12 of the extended sense information. Provides a standardized description of the condition described by the sense information.

SCSI Device
A device attached to a Small Computer System Interface bus cable. The device may be an initiator, a target, or be capable of both types of operation. The device may be a peripheral device, a host device, or a device mixing both roles.

SCSI*Select*™ Configuration Utility
Adaptec's built-in, menu-driven SCSI host adapter configuration program. SCSI*Select* allows you to change almost all of the host adapter option settings without opening the case of your computer or handling the adapter board.

Single-Ended
A term referring to the electrical characteristics of the signals used on the SCSI bus interface. Single-ended signals occupy a single conductor and are referenced to a common ground carried on the cable between the attached SCSI components.

Single-Threaded Operation
Operation of the computing system such that only one program can be operating or active at a time. The computing system must wait until all resources are available before starting an operation and cannot start another operation until the first one is completed. No overlapping of latencies or program operation occurs.

Synchronous Data Transfer
A method of data transfer on the SCSI bus involving clocking data on to the bus with fixed-length, fixed-frequency strobe pulses. The acknowledgments may be delayed several clock periods from the data requests. Synchronous data transfer can be used only for data transmission on the SCSI bus. It is prohibited for command, message, and status transmission.

Synchronous Data Transfer Negotiation
The message exchange between the initiator and the target that allows the negotiation of the data transfer frequency and delay between requests and acknowledgments required for synchronous data transfer. Once negotiated, synchronous data transfer parameters remain unchanged until certain reinitialization activities occur.

Target
A SCSI device that performs an operation requested by an initiator. The target may be a peripheral device performing a service for an initiator. The target may also be a host adapter performing a processor-type device service for an initiator.

Word
A 2-byte (16-bit) unit of data.

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