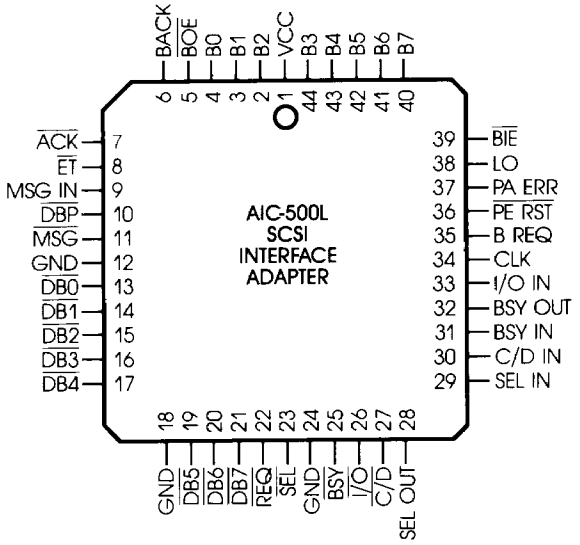
adaptec, inc.

AIC-500

SCSI Interface Adapter



- **Asynchronous Data Transfer To 1.5 Mbytes/Sec**
- **Supports Target Role**
- **Parity Generation And Checking**
- **Complements AIC-300 Arbitration And Meets SCSI Specification**
- **SCSI Bus Signals Driven Under Microprocessor Control**
- **High Current Outputs Drive SCSI Bus Directly**
- **Available in 44-Pin PLCC Package**

OVERVIEW

The AIC-500 is designed to simplify the implementation of a SCSI host interface-based disk controller. It is intended to be used in designs based around the Adaptec Programmable Storage Controller, the AIC-010; and the Adaptec Dual-Port Buffer Controller, the AIC-300. The AIC-500 comes in a 44-pin J-pack and has the high-current drivers needed to directly connect to the SCSI bus.

The AIC-010, AIC-300, AIC-500, and the buffer RAM are all that is needed to design an extremely powerful and cost effective controller which is resident o the disk drive. In most applications, the microcontroller that is directly present on the drive can be shared between the drive-related and the controller-related functions. With a dedicated processor, this same set can be used to build edxtremely hgh-performance SCSI controleIrs which connect to drive level interfaces like ST412/506, ESDI, and SMD.

PIN DESCRIPTION

SYMBOL	PIN	TYPE	NAME AND FUNCTION
			SCSI LINES
$\overline{ACK}$	7	SCSI I	ACKNOWLEDGE: Used to acknowledge data has been received or sent on SCSI bus.
$\overline{DBP}$	10	SCSI I/O	DATA BIT PARITY: SCSI bus parity bit.
$\overline{MSG}$	11	SCSI O	MESSAGE: Used to select a message phase on the SCSI bus.
$\overline{DB0}$ to $\overline{DB7}$	13-17 19-21	SCSI I/O	DATA BITS 0-7: SCSI bus data lines.
$\overline{REQ}$	22	SCSI O	REQUEST: The request for data transfer on SCSI bus.
$\overline{SEL}$	23	SCSI I/O	SELECT: Indicates a bus select status.
$\overline{BSY}$	25	SCSI I/O	BUSY: Active when any device is accessing the SCSI bus.
$\overline{I/O}$	26	SCSI O	INPUT/OUTPUT: Used to select the direction of data movement on the SCSI bus with respect to the initiator.
$\overline{C/D}$	27	SCSI O	COMMAND/DATA: Used to select command or data transfer on SCSI bus.
			CONTROLLER LINES
V_{CC}	1		+5 Volts.
B0 to B7	2-4 40-44	TTL I/O	DATA BUS 0-7: Connects to buffer RAM data pins.
$\overline{BOE}$	5	TTL I	BUS OUT ENABLE: Connects to AIC-300. Used to clock data out of internal latches for transfer onto SCSI bus.
PORT B ACK	6	TTL O	PORT B ACK: Connects to AIC-300. The acknowledge for a Port B data transfer.
$\overline{ET}$	8	TTL I	ENABLE TARGET: Connects to AIC-300. Provides microcode and hardware access to disable all drivers on the SCSI bus, except BUSY.
MSG IN	9	TTL I	Connects to I/O port which drives $\overline{MSG}$.
GND	12, 18, 24		GROUND.
SEL OUT	28	TTL I	SELECT OUTPUT: Connects to the AIC-300. Used as an input from the AIC-300 to indicate when to drive the select line on the SCSI bus.
SEL IN	29	TTL O	SELECT INPUT: Connects to the AIC-300. Used to pass the select line from the SCSI bus to the AIC-300.
C/D IN	30	TTL I	Connects to I/O port which drives $\overline{C/D}$.
BSY IN	31	TTL O	BUSY INPUT: Connects to AIC-300. Used to pass busy to the AIC-300 to indicate when other devices are actively accessing the bus.
BSY OUT	32	TTL I	BUSY OUTPUT: Connects to AIC-300.Used as an input from the AIC-300 to indicate when to drive the busy line on the SCSI bus.
I/O IN	33	TTL I	Connects to I/O port which drives $\overline{I/O}$.
CLK	34	TTL I	CLOCK: Used for clock input between 2.5 MHz and 5 MHz.

SYMBOL	PIN	TYPE	NAME AND FUNCTION
PORT B REQ	35	TTL I	PORT B REQ: Connects to AIC-300. The request for a Port B data transfer.
$\overline{\text{PE RST}}$	36	TTL I	PARITY ERROR RESET: When held high, the AIC-500 checks SCSI bus parity and indicates a parity error by setting logic 1 (high) on the PA/ERR pin. When held low, parity is passed through the AIC-500 to the controller buffer with the PA/ERR line being the parity bit.
PA/ERR	37	TTL O	PARITY ERROR: Logic 1 indicates a parity error detected on the SCSI bus when $\overline{\text{PE RST}}$ is held high. When the $\overline{\text{PE RST}}$ line is held low, parity will be passed to the controller bufffer by using the PA/ERR line as the parity bit for each byte.
LO	38	TTL I	LATCH OUT: Connects to AIC-300. Gates data into internal latches after reading data from buffer.
$\overline{\text{BIE}}$	39	TTL I	BUS IN ENABLE: Connects to AIC-300. Used to enable data from bus for writing data into buffer.

FUNCTIONAL DESCRIPTION

The AIC-500 is divided into four basic subfunctions:

- Parity Generation/Checking
- Arbitration
- SCSI Bus Drivers and Receivers
- REQ/ACK Handshake and Data Latch

PARITY GENERATION/CHECKING: The AIC-500 parity generation/checking logic will latch parity errors or pass parity through the AIC-500 in order to maintain buffer parity. The AIC-500 always generates SCSI bus parity on inbound SCSI transfers and during the selection phase.

ARBITRATION: The AIC-500 complements the AIC-300 arbitration logic to provide correct SCSI bus timing. On the SCSI interface, this provides a two-wire arbitration scheme where either $\overline{\text{SEL}}$ or $\overline{\text{BSY}}$ indicate a bus busy state.

SCSI BUS DRIVERS AND RECEIVERS: The AIC-500 has the 48 mA open-collector outputs necessary for driving the control and data line of a single-ended SCSI bus directly.

REQ/ACK HANDSHAKE AND DATA LATCH: The AIC-500 complements the AIC-300 REQ/ACK handshake timing by latching the SCSI data for an outbound data transfer before completing the transfer into the controller buffer. This speeds data transfer across the bus by reducing the REQ/ACK timing restraints for the SCSI bus transfers.

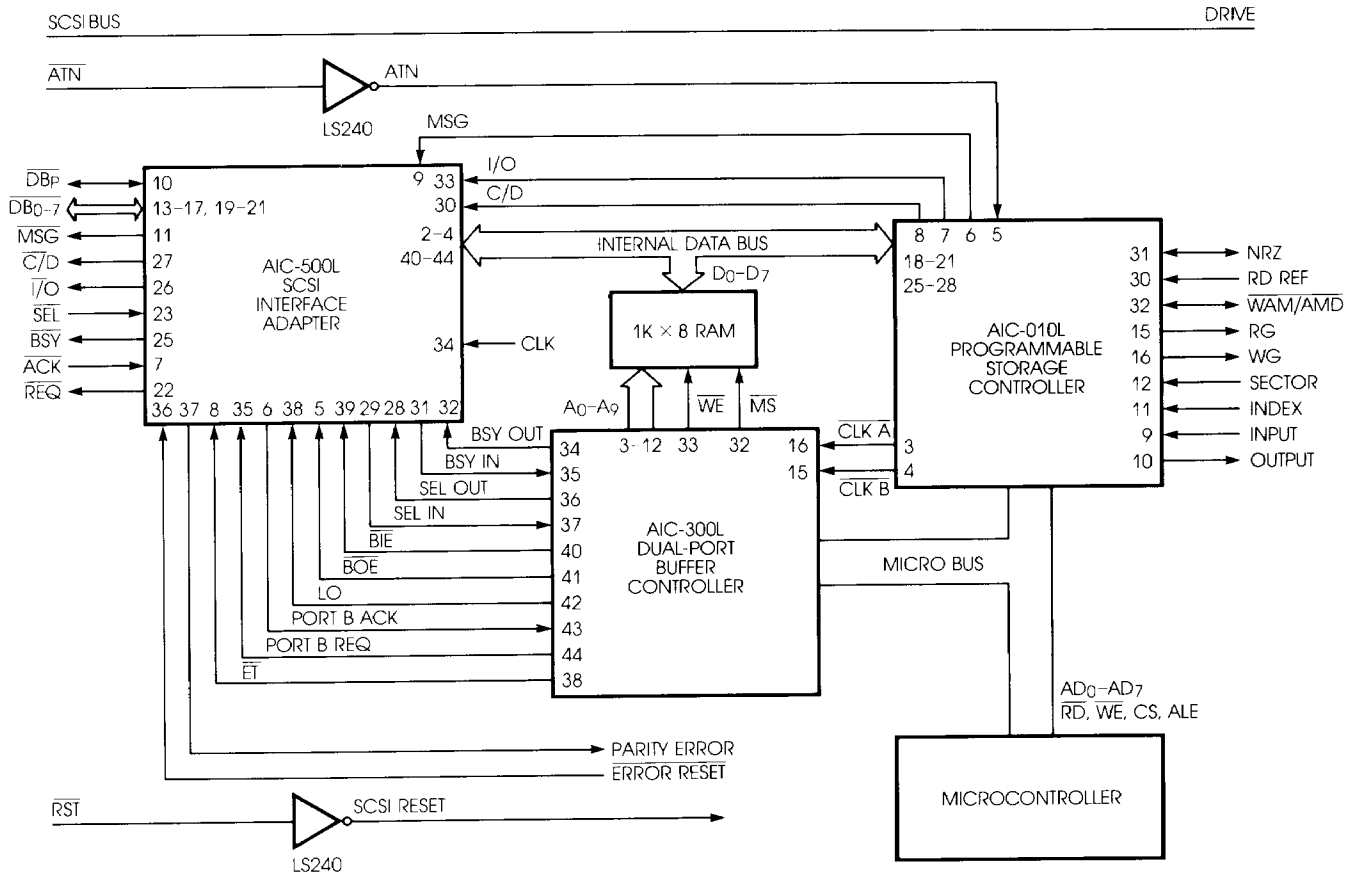


FIGURE 1. TYPICAL FULL SCSI CONTROLLER CONFIGURATION

Parity

The AIC-500 provides increased data integrity by generating and checking SCSI bus odd parity on the SCSI bus transfers. Parity may also be kept on data in the controller buffer by passing a parity bit from the AIC-500 through the buffer.

When checking SCSI bus parity, the $\overline{\text{PE RST}}$ (pin 36) line must be held high. When a parity error occurs, the PA/ERR (pin 37) line will be asserted (logic 1) and latched. To clear the error condition, the $\overline{\text{PE RST}}$ (pin 36) line must be driven to a low level. Appropriate error recovery may then take place. See Figure 2 for a block diagram demonstrating this type of operation.

To pass SCSI bus parity from the AIC-500 to the controller buffer, the $\overline{\text{PE RST}}$ (pin 36) line must be in the low state. The AIC-500 will then pass the parity bit for the data on to the controller buffer.

The AIC-500 always generates and checks SCSI bus odd parity, but the controller need not implement the parity feature. To disable parity checking by the AIC-500, the $\overline{\text{PE RST}}$ (pin 37) line should be held in a logic 1 state and the PA/ERR line may be ignored.

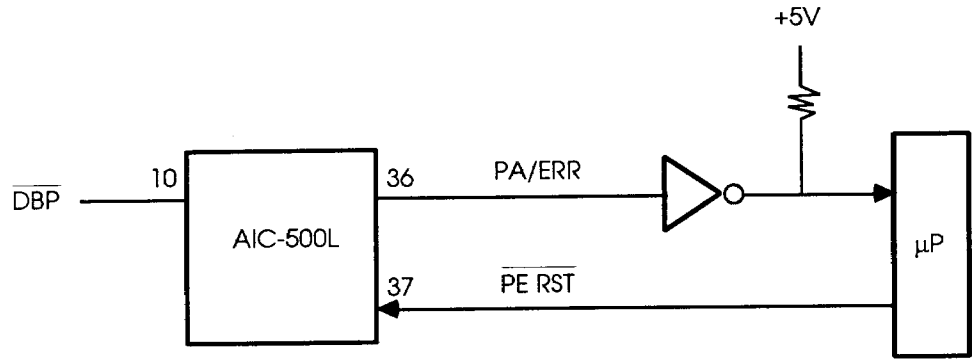


FIGURE 2. CHECKING SCSI BUS PARITY

Arbitration

The AIC-500 complements the logic of the AIC-300 to provide maximum SCSI bus performance in all phases and to ensure conformance with the SCSI specification. The AIC-300 implements the two-wire arbitration logic, waiting for a bus free state (no $\overline{BSY}$ or $\overline{SEL}$) then asserrts BSY and the correct SCSI bus ID.

See Figure 3 for a block diagram demonstrating the AIC-300 and AIC-500 interface of lines used during arbitration. The AIC-500 controls the timing of the lines being driven on the bus. The clock rate for the AIC-500 may vary between 2.5 MHz and 5 MHz. A 5 MHz clock input on pin 34 will provide maximum SCSI bus performance for the AIC-500. To calculate the timings at the SCSI interface, use the following equations:

Bus Free Delay Min = T * 3
Bus Free Delay Max = T * 4

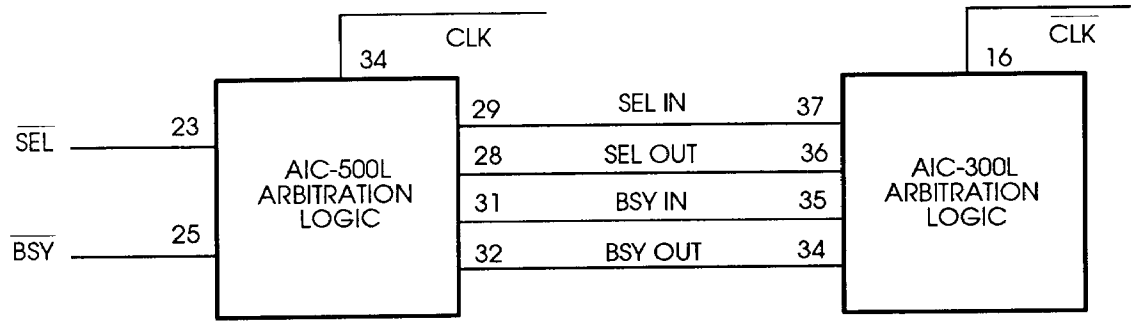


FIGURE 3. BLOCK DIAGRAM OF SCSI BUS ARBITRATION LOGIC

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature Under Bias..... 0°C to 70°C
Storage Temperature..... -55°C to 150°C
Voltage on Any Pin with Respect to Ground.....-0.3 V_{CC} to +7.0V
Power Dissipation..... 0.5 Watt
Power Supply Voltage..... 4.75 to 5.25 Volts

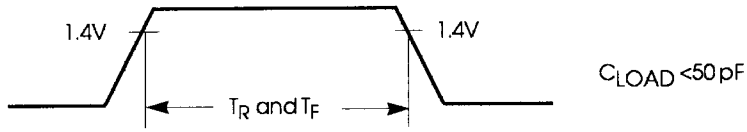
NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS (V_{CC} = 5.0V ±5%, V_{SS} = 0V, T_a = 0 ≈ +70°C)

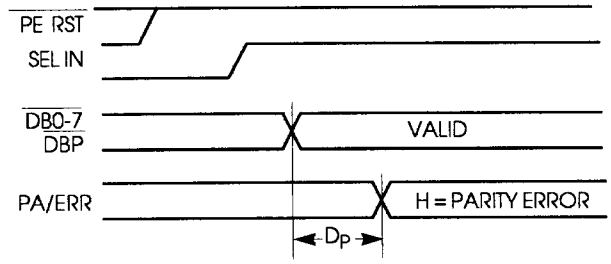
SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
V_{IL}	Input Low Voltage (All Except $\overline{ACK}$)		0.8	V	
V_{IH}	Input High Voltage (All Inputs)	2.0	V_{CC}	V	
V_{IL}	Input Low Voltage ($\overline{ACK}$)		0.6	V	
V_{OL}	Output Low Voltage (TTL Pins)		0.4	V	I_{OL} = 2 mA
V_{OL}	Output Low Voltage (SCSI Pins)		0.5	V	I_{OL} = 48 mA
V_{OH}	Output High Voltage (TTL Pins)	2.4		V	I_{OH} = -400 µA
I_{IL1}	Input Leakage (B REQ, LO, $\overline{BOE}$, $\overline{BIE}$, $\overline{ET}$, $\overline{SEL}$ OUT, $\overline{BSY}$ OUT, CD IN, IO IN, MSG IN, $\overline{PE}$ $\overline{RST}$, CLK, $\overline{ACK}$)	-10	+10	µA	0 <V_{IN} <V_{CC}
I_{OL1}	Output Leakage (B0, B1, B2, B3, B4, B5, B6, B7)	-10	+10	µA	0.45 <V_{OUT} <V_{CC}
I_{OL2}	Output Leakage (SEL, BSY, DB0, DB1, DB2, DB3, DB4, DB5, DB6, DB7, DB8)	-50	+50	µA	0.45 <V_{OUT} <V_{CC}
V_{HSY}	Hysteresis Voltage ($\overline{ACK}$ Only)	200		mV	
I_{CCS}	Standby Current		600	µA	T_a = 70°C
I_{CC}	Supply Current		30	mA	T_a = 70°C
C_{IN}	Input Capacitance		15	pF	

NOTE:
STATIC SENSITIVE DEVICE.
HANDLE WITH CARE.

A.C. TEST CONDITIONS (V_{CC} = 5.0V ±5%, V_{SS} = 0V, T_a = 0 ≈ +70°C)

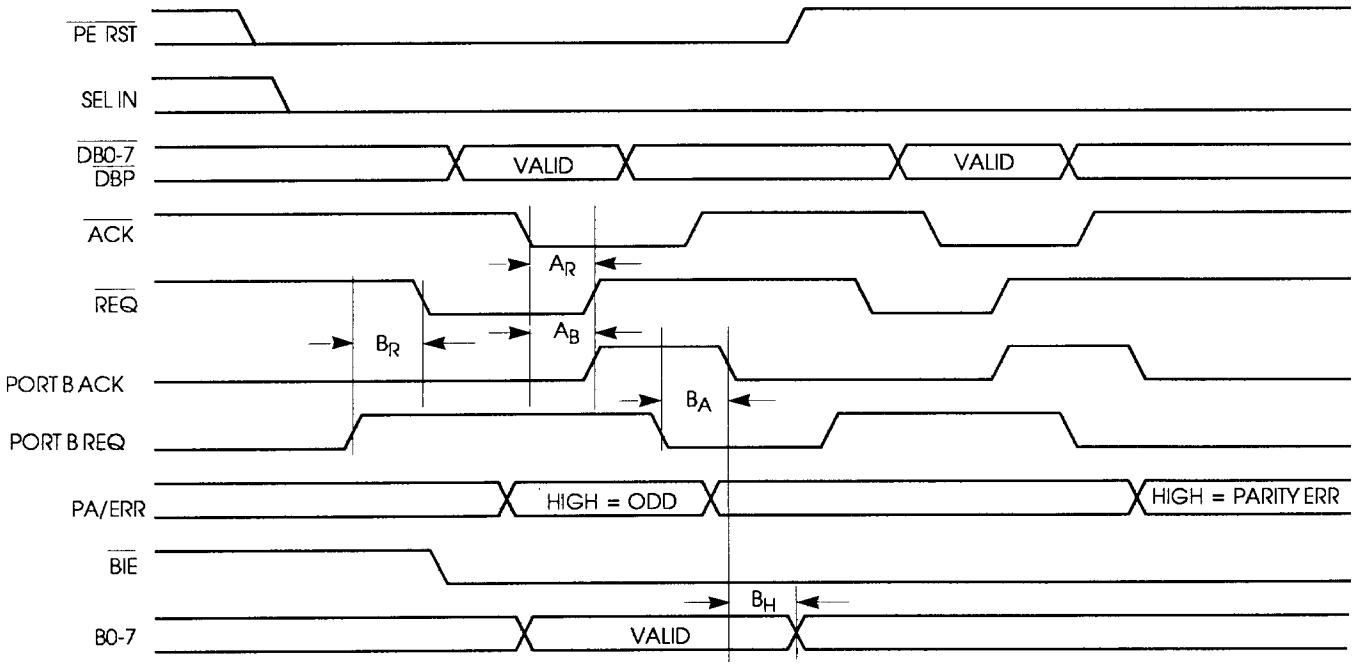


SCSI BUS PARITY TIMING



SYMBOL	PARAMETER	MIN	MAX	UNITS
D_P	Data Valid to Parity Error Detect		100	ns

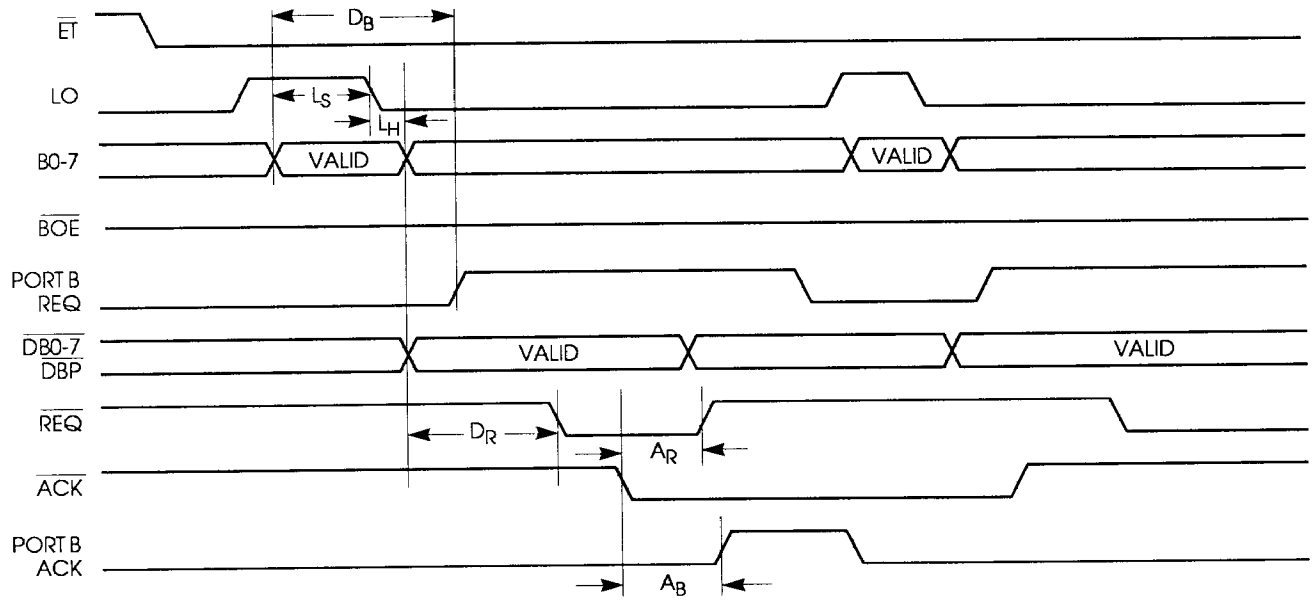
WRITE OPERATION



SYMBOL	PARAMETER	MIN	MAX	UNITS
A_R	$\overline{ACK}$ ↓ to $\overline{REQ}$ ↑	75	55	ns
A_B	$\overline{ACK}$ ↓ to PORT B ACK ↑	75	50	ns
B_R	PORT B REQ ↑ to $\overline{REQ}$ ↓	40	20	ns
B_A	PORT B REQ ↓ to PORT B ACK ↓	40	25	ns
B_H	PORT B ACK ↓ to Data Invalid	75	40	ns

The PA/ERR line in the timing diagram above shows odd parity being passed from the AIC-500 to the controller buffer when the $\overline{PE\ RST}$ line is held low, as it is during the first data transfer. During the second data transfer, the $\overline{PE\ RST}$ line is held high; therefore, the PA/ERR line indicates parity error on the SCSI bus when high.

READ OPERATION



SYMBOL	PARAMETER	MIN	MAX	UNITS
L_S	PORT B Data Valid to LO ↓	0		ns
L_H	LO ↓ to PORT B Data Invalid	25		ns
A_R	$\overline{ACK}$ ↓ to $\overline{REQ}$ ↑		80	ns
A_B	$\overline{REQ}$ ↓ to PORT B ACK ↑		80	ns
D_R	SCSI Bus Data Valid to $\overline{REQ}$ ↓	55		ns
D_B	PORT B Data Valid to PORT B REQ ↑	90		ns

$\overline{BOE}$ must be held low during data transfer from the controller to the host to ensure legal SCSI bus timing.

PACKAGING INFORMATION