SIGDA NEWSLETTER

A Quarterly Publication of the Special Interest Group on Design Automation

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Special SIGDA Officer Election Issue
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SIGDA BOARD OF ADVISORS

Nominating Committee Chair
Richard C. Smith
National Semiconductor, Inc.
2900 Semiconductor Drive, D3677
Santa Clara, California 95051
(408) 721-4794 FAX (408) 773-0978
nsc!parns!ricardo

High School Scholarship Program
Charlotte F. Acken
Sandia National Laboratories, Div. 4853
P. O. Box 969
Livermore, California 94551
(415) 294-3248 FAX (415) 294-1539
cacken@sandia.llnl.gov

Bibliography & Textbook Projects
Waldo G. Magnuson, Jr.
Lawrence Livermore National Lab.
P. O. Box 808, L-153
Livermore, California 94550
(415) 422-9950 FAX (415) 423-5080
magnuson@icdc.llnl.gov

Workshops/Conferences (except DAC)
Paul B. Weil
Nextwave Design Automation, Inc.
5339 Prospect Road, Suite 240
San Jose, California 95129
(408) 255-6458
weilcad@frith.cs.psu.edu

IEEE/CS DATC Chairman
Joanne E. DeGroat
Department of Electrical Engineering
Ohio State University
2015 Neil Avenue
Columbus, Ohio 43210-1272
(614) 292-2439 FAX (614) 292-7596
degroat@hathi.eng.ohio-state.edu

Outstanding Member Recognition
Charles E. Radke
IBM Corporation, AR1
Route 52
Hopewell Junction, New York 12533
(914) 892-2957 FAX (914) 892-3039
C.RADKE@COMPMAIL.COM

European Activities
H. Gordon Adshead
International Computers Ltd.
Wenlock Way, West Gorton
Manchester M125DR, ENGLAND
(011-44-61) 223-1301

Asian Activities
Akihiko Yamada, Chief Engineer
Information Processing Group
NEC Corporation, Daito Tamachi Bldg.
14-22 Shibaura 4-Chome, Minato-Ku
Tokyo 108, JAPAN
(011-81-3) 456-5750
FAX (011-81-3) 456-7495
a.yamada@compmail.com

Travel Grants and Library Grants
James P. Cohoon, Ph.D.
Department of Computer Science
University of Virginia, Thornton Hall
Charlottesville, Virginia 22903
(804) 982-2210 FAX (804) 982-2214
csnet: cohoon@virginia.edu
uucp: !uvacs!cohoon

Scholarships
Herschel Loomis, Jr.
Naval Postgraduate School - EE Dept.
Code 62Lm
Monterey, California 93943
(408) 646-3214
loomis@cs.nps.navy.mil

University Faculty Activities
Mary Jane Irwin
Pennsylvania State University
Department of Computer Science
University Park, Pennsylvania 16802
(814) 865-3176
mji@psuvaxl.cs.psu.edu

University Booth Project (DAC)
Martin Wong
Department of Computer Science
University of Texas
Austin, Texas 78712
(512) 471-7316
wong@cs.utexas.EDU

SIGDA OFFICERS

Chairman & ACM DAC Representative

Charles A. Shaw
Cadence Design Systems, Inc.
2455 Augustine Drive
Santa Clara, CA 95054-3082
(408) 987-5321
shaw@cadence.com

Secretary/Treasurer

Michael J. Lorenzetti
Mentor Graphics Corporation
8500 S.W. Creekside Place
Beaverton, OR 97005-7191
(503) 626-7000
mikelor@mentor.com

Vice Chairman & IEEE DATC Newsletter Coordinator

Bryan T. Preas
CADLAB
Bahnhofstrasse 32
4790 Paderborn, West Germany
011 49 52 51 28 41 02 main
011 49 52 51 60 20 67 secy
preas.@cadlab.cadlab.de
preas%cadlab.uucp@seismo.css.gov

ACM SIG Program Director

Debbie Hall
11 West 42nd Street
New York, NY 10036
(212) 869-7440
Hall@ACMVM.Bitnet

EDITOR'S NOTES

Welcome to the Winter edition of the *SIGDA Newsletter*. This will be the final edition of 1990, and it is an important one since it contains the slate of officers for SIGDA. There are two candidates for each office. Please be sure to vote. See page 23 for a listing of the candidates and related information.

This edition also contains two articles on VHDL. One is a lucid tutorial on VHDL design techniques by David Alford. David is from industry and has illustrated his article with a very comprehensive set of examples. The other article is a description of the *Keystone VHDL Design System* developed by the University of Pittsburgh and Penn State University. The authors, Alan Martello and Steven Levitan, are from the academic community, and they too have included design examples in their article. Both articles take a very practical approach to using VHDL in design. I think they will be of particular interest to those just learning about VHDL and needing explicit examples of it use.

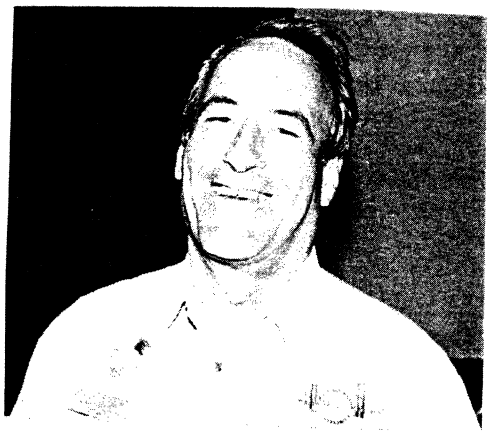
Additionally, this edition contains the minutes of two Advisory Board meetings and the Fall (ICCAD) General Membership meeting. These minutes contain good summaries of the state of the various projects of SIGDA. Also, included is the second edition of the SIGDA e-mail directory. It was drawn from the survey responses. If you want to be listed, just send in your survey form. I suspect the e-mail directory will become ever more popular.

One last note: At the recent SIG Board Meeting,a motion was passed (authored by Tom Keller, chairman of SIGMETRICS) that removes the prohibition against employment advertising in *SIGNewsletters*. The SIGDA Advisory board has not formally acted on this relative to SIGDA; however, a straw e-mail poll indicates that there is broad support for this idea. If adopted, SIGDA members could submit 'situations wanted' ads (probably for free), and DA companies could submit 'help wanted' (probably for a fee). Please don't send me your ad-copy yet since ACM-HQ must be consulted on fee structures, disclaimers, policies, etc. However, it seems likely that this new service may be added some time in 1991.

Patrick M. Hefferan - SIGDA Editor

1681 Princeton Ave.
St. Paul, MN 55105
(612)690-5451
hefferan@frith.entmoot.cs.psu.edu

LETTER FROM THE CHAIR



SIGDA has an election this Spring. In this issue, you'll find the list of nominations for our elected officers. Put together by Dick Smith, this list presents you, the members, with a selection of the most dedicated and dynamic participants in SIGDA and its activities. Dick drew on his long experience in SIGDA activities, including his position as Chair preceding me. He is uniquely qualified to head up the Nominating Committee, whose role was to put together this slate of candidates.

Should you feel that a strong candidate has been overlooked, it is not difficult to add nominations by petition. The procedure is detailed in the same section of this Newsletter.

I am not running for SIGDA office. I feel that you have had a long enough period under my leadership; it's time for a change. No organization can be healthy for the long pull if its top position isn't open, as a goal to which others in the organization can aspire. California, in the recent election, put a term limit on its state legislators - I don't want SIGDA to feel that it would need to do the same to move me out!

SIGDA has before it many exciting opportunities. It will be a pleasure, not a burden, to be elected an officer of SIGDA. There are few organizations with the financial resources of SIGDA, with such a dedicated and active group of volunteers, with such wholehearted support from its parent organization ACM, and with such a dynamic technical field of CAD as its base. The new officers will have a rich set of alternatives from which to choose.

Among these are the emergence of an integrated Europe, stretching from the Atlantic to the Soviet Union, and the chance for SIGDA to play a strong role in its conferences, workshops, universities, and industries. In Asia, the Japanese CAD-oriented conferences draw as many attendees as does DAC. Other Asian countries are ripe for a strong expansion in their CAD activities.

ACM continues to examine its structure and the services its members want to have from it. SIGDA is fortunate in having ACM as its parent - ACM has become, during my term of office, a SIG-oriented organization. SIGDA's strength gives it a leading role in ACM deliberations. The SIGDA officers are key players in ACM direction and policy decisions.

There is also the great personal satisfaction of leading an organization doing as many good things as SIGDA does. The officers you elect can feel justly proud to be elected. So choose wisely, and VOTE!

Charles A. Shaw - Chairman SIGDA
December 1990

SIGDA ADVISORY BOARD MEETING MINUTES

The SIGDA Advisory Board Meeting was called to order at 9 a.m. on **September 16, 1990** by Chairman Chuck Shaw. In attendance were Board Members Franc Brglez, Jim Cohoon, Patrick Hefferan, Mary Jane Irwin, Michael Lorenzetti, Bryan Preas, Chuck Radke, Ron Waxman, Paul Weil, and Akihiko Yamada. Also in attendance were Joe Deblasi and Debbie Hall, from ACM Headquarters and Mark Mendelbaum, Bill Greener, Meg Tuttle and Bernie Rouse from the ACM Publications Board.

A. Minutes

MOTION: *The minutes of the June 23 SIGDA Board Meeting be approved as submitted.* ***(Weil, Irwin, unanimous)***

B. Financial

Secretary/Treasurer Michael Lorenzetti reviewed the financial status of SIGDA. The fund balance is approximately $1,300,000 as of June 30, 1990. As discussed in our last meeting, our annual recurring expenses are now on the order of the revenues we realize from the Design Automation Conference (~$800,000). For fiscal year 1990, our expenses exceeded our revenues by $166,000, which indicates we are beginning to apply our massive fund balance to services for the DA profession.

C. Newsletter

Pat Hefferan reviewed the sales of proceedings, EDIF and VHDL manuals via the coupons published the Newsletter. This program provides low-cost standards manuals and proceedings to our members. He presented the following summary:

	Number	Cost
EDIF manuals	58	$3,378
VHDL manual	76	3,130
25 years of DA	35	5,100
1990 DAC proceedings	60	(w/25 Yrs)
1990 ICCAD proceedings	50	3,000
Subtotal		14,608
Postage		1,012
Labor (@$20/hr)		1,000
TOTAL		**$16,620**

Hefferan also summarized the administration cost for the Newsletter which totaled $5,544 for the year so far.

Hefferan requested that SIGDA purchase a PC and laser printer for Newsletter administration. He detailed the request as follows:

386SX PC	$2,600
HP Laser Printer	1,800
Modem	300
Software	
Ventura	500
Word	400
Communications	100
TOTAL	**$5,700**

MOTION: *Approve Pat Hefferan's request for $5700 for a PC and laser printer for Newsletter support.* ***(Weil, Cohoon, unanimous)***

D. DA Library (CD-ROM)

Kathy Preas reported that there was a great deal of enthusiasm for the DAL demos at DAC. Evaluators have been invaluable in getting feedback on the system. Many design changes have resulted. She summarized some of these.

DAL will be organized by year rather than by publication. This facilitates updates each year but makes addition of other series more difficult. ICCD proceedings have been added. The SIGDA Newsletter is included, but as page images only (this means only that it will not be searchable). The 1990 proceedings will not be included in the first release because it was not budgeted.

All text will be stored on one CD as a search device. Page images will appear on the remaining seven CDs. They plan to go back and key in tables, algorithms and other similar entries that were previously considered unkeyable. They are putting a QA plan in place. SAZTEC will do 100%

sampling of page images (some were skewed in the prototype). There will be some sampling of keyed text.

The 1989 volumes will be done as an additional pre-production evaluation version within a couple of weeks. The final version will not be available by the DAC in June. Prototype evaluation is taking longer than anticipated and there were more changes than anticipated. They expect to have ROMs pressed by July.

A discussion ensued about whether this process can be speeded up, but no solutions were found. SUN now requires purchase of CD-ROM to get software. This helps us in that drives will be installed (which is difficult).

MOTION: *Expand the DA Library budget (by approximately $110,000) to include 1990 publications, if possible.* ***(Hefferan, Lorenzetti, unanimous)***

At this point Mark Mendelbaum introduced the other ACM Publications representatives.

Bernie Rouse asked for a loan from SIGDA to ACM Publications of $110,000 to cover startup costs for CD-ROMS, to be paid back in the next fiscal year based on revenues from DAL. He reviewed the business plan.

Deblasi pointed out that we are heavily underwriting the cost. Prices can go as high as $3,500 for such a set if we were not subsidizing it. (The business plan puts the price at $599 for SIGDA members, $999 for other ACM/IEEE members and $1399 for non-members). Although SIGDA views this project as a service to the profession, a price that does not cover costs will make it tough for other SIGs to price their ROMs competitively.

After some discussion, it was agreed to leave the pricing as is, but to put a clear statement in the promotional literature that SIGDA is underwriting the cost and to what extent they are doing so.

The business plan presented assumes exclusive distribution rights for ACM because the market is too small to split between them and IEEE. The plan is to pay royalties to IEEE on a per unit sold basis. Weil requested a marketing plan from ACM for DAL.

Brglez suggested we offer a bonus to registrants at DAC and ICCAD (as part of the registration form, perhaps) to order DAL. Preas agreed to take that up with the DAC and ICCAD boards. ACM also presented a proposal for how to handle the excess revenues, should this project be wildly successful (1/3 to publications to build up CD-ROM program, 1/3 for DAL updates and 1/3 back to the SIGDA treasury).

MOTION: *Accept the tentative business plan as presented by ACM publications, including the loan from SIGDA.* ***(Cohoon, Weil, unanimous)***

The question was raised whether the loan should be a grant instead in order to leverage ACM into the CD-ROM business. After a brief discussion, it was agreed to leave it as is (as per Radke's suggestion) since we can always cancel the payback later if we so desire.

E. Formal Methods Journal

Weil reported that the proposal for a Journal on Formal Methods stands unchanged from the version presented at the DAC meeting.

The SIGDA concerns regarding scope and funding were expressed to the authors of the proposal.

MOTION: *Refer the Formal Methods Journal to the SIG Discretionary Fund for funding because it appeals to a broad based set of technical interests within ACM, not merely those of SIGDA.* ***(Lorenzetti, Irwin, 10-0-1)***

F. Email System

Mary Jane Irwin summarized costs for the 800 number used for our Email system. Installation was $341 and the total bill for February through July was $812.83. Felix Lee (flee@frith.cs.psu.edu) is the system administrator.

G. DAC Contract

Shaw reported that the three-year contract for DAC management by MPA has finally been signed. It is now time start on the next one (beginning with DAC 95) which will be done by competitive bid.

H. SIGDA University Booth

Mary Jane Irwin announced that the booth selected for the '91 DAC will be the largest so far (30' by 50'). It will contain six machines (four Suns and two DECs).

The budget is as follows:

Item	Cost
Booth Rental	$25,000
Furniture	10,000
Management	10,000
Travel	4,000
Shipping	2,000
Equipment	20,000
Total Cost	$71,000

Jim Cohoon is the organizer for 1991. It is now time to select an organizer for 1992. Several names were proposed but the decision was left up to Cohoon and Irwin. Irwin suggested that we may need an NEC machine in 1991 to encourage Asian participation.

MOTION: *Allocate $20,000 for the equipment grant for the University Booth for the 1991 organizer.* ***(Irwin, Radke, unanimous)***

Bryan Preas pointed out the DAC Executive Committee may be willing to help with public service projects such as this (that relate to DAC) and posed the question "what, if any, assistance would be beneficial?" It was pointed out that the University Booth is a high visibility area for SIGDA and is one for which we would like to retain responsibility. On the other hand, the graduate scholarship program is one that is shared with DATC (although SIGDA pays the largest share of the funding) and is generally recognized as associated with DAC. Making that program a part of the DAC budget would make the situation more equitable. Also, we could ask them to waive the registration fee for our travel grant recipients to allow our funds to go further.

Weil informed the committee that EDAC wants a University Booth for their conference. We should also consider expanding it to other areas (possibly Asia).

MOTION: *SIGDA set aside $50,000 to fund a University Booth at EDAC, contingent upon SIGDA formally becoming a sponsor or obtaining "in cooperation with" status for that conference.* ***(Weil, Radke, unanimous)***

I. Asian Activities

Akihiko Yamada reviewed a list of Asian activities related to SIGDA.

IFIP Workshop on Design and Test of ASICs. June 11-12, 1990 Hiroshima, 80 attendees. Co-sponsors IFIP WG 10.5, IPSJ

IPSJ Annual DA Workshop '90. August 30 - September 1, Hakone, Kanagawa, Japan. 108 attendees.

InfoJapan '90. International Conference on Information Technology. Commemorating IPSJ 30th anniversary. October 1-5 Keio Plaza Hotel, Tokyo, 1200 attendees expected.

IPSJ-SIGDA, IEICE-FTS Joint Workshop on Design and Test, October 8-9, Osaka, Japan.

IPSJ-SIGDA, IEICE-VLD Joint Workshop on Synthesis, December 11-12, Tokyo, Japan

Weil suggested a Pacific-Rim DA workshop somewhere between Asia and the U.S. (perhaps in Hawaii or Fiji). Yamada agreed to bring this idea up with IPSJ at their next meeting.

J. High School Scholarship

Shaw reported for Charlotte Acken. The visit by the scholarship recipients to the DAC went well. No changes in the program are anticipated for next year. We will keep the scholarship in the Bay Area and have MESA help with the screening.

Donna Couch, the current scholarship administrator, is moving from the Bay Area and will resign from her position. Two candidates have been identified to serve as her replacement. Acken proposed that we make the position a fixed fee of $6,000 per year (rather than hourly). ACM would pay the administrator directly.

The Board saw no problem with the plan and Shaw pointed out that no Board action was required, since this change is within the current scholarship budget.

Acken requested a PC, printer and software for word processing and bookkeeping for the project.

MOTION: *Approve up to $7,000 for a computer and printer for administration of the High School Scholarship program.* ***(Weil, Cohoon, 10-1-0)***

Debbie Hall of ACM requested that we collect a list of capital equipment, including price and serial number. These are necessary to depreciate the equipment and just to keep track of its location.

Lorenzetti agreed to collect the list and provide it to Hall.

Shaw presented the tentative breakdown of expenses for the fiscal year ASCEE:

Scholarship Fund	$40,000
Administrator Fee	6,000
PC, Printer & Software	10,000
Two Mentor Meetings	1,000
DAC '91 meeting expenses (travel, student luncheon, Mentor registrations at DAC, etc.)	2,500
Office supplies, phone, mail, misc. expenses	500
TOTAL	$60,000

K. Graduate scholarships

Shaw reported for Loomis that no changes are anticipated for this successful program. The current funding level is appropriate.

Waxman appointed Radke to continue as DATC representative on the Graduate Scholarship committee.

L. Video Tape

Irwin distributed comments from reviewers on Richard Newton's outline for the Introduction to Design Automation video. The comments were very positive. The budget remains at $43,000 and they hope to start production some time this fall.

Reviewer comments were also distributed on the outline of Introduction to VHDL by Jim Armstrong. This project is to be funded jointly with DATC. The anticipated total cost is approximately $38,000. They hope to have tapes ready in time for spring courses.

MOTION: *SIGDA fund 50% of the Introduction to VHDL video, up to a maximum of $20,000.* ***(Radke, Hefferan, unanimous)***

Irwin announced that they may show the video tapes at the SIGDA University Booth at DAC next year.

Irwin announced that two universities have contacted her about distributing videos that they have produced. After some discussion it was agreed that we should refer them to University Video and not get involved with distribution of tapes from other sources.

M. Discretionary Fund

Lorenzetti summarized the SIG Discretionary Fund and contributions from other SIGs (see SIGDA Newsletter, v20, number 1, page 40). The Discretionary Fund provides a means to support projects which span a wide range of technical interests, rather than those of a single SIG. SIG Board manages the fund and contributions are made by individual SIGs on a voluntary basis. For the past two years, SIGDA has worded their contribution as follows: "Subject to an absolute maximum of $200,000, SIGDA will contribute an amount equal to the maximum of the following two numbers:

(1) the largest contribution of any other single SIG,

(2) half the contribution of all other SIGs combined."

Lorenzetti reported that this wording has served to induce other SIGs to increase their contributions to the fund (most notably SIGPLAN) and prevented SIGDA from being the overwhelming majority contributor.

MOTION: *For the fiscal year 1992 Discretionary Fund contribution, apply the same conditions and amount as fiscal year 1991.* ***(Cohoon, Irwin, unanimous)***

N. Meeting at Critical Issues Conference

There are several SIG-related meetings to be held at the Critical Issues Conference in November in Washington DC. Shaw asked for suggestions as to who should represent us. Shaw and Irwin will both attend (Irwin also represents SIGARCH). Hefferan volunteered to serve as backup, should one of them be unable to make the trip.

O. Next Meeting

After some discussion, Shaw announced that the next Board Meeting will be 9 a.m. on the Sunday before ICCAD. The General Membership meeting will be held Sunday evening.

P. Conferences and Workshops

Weil summarized SIGDA conference and workshop activities. DAC is, of course, our primary conference which we co-sponsor with IEEE-CS. We are currently "in cooperation with" ICCAD, which is sponsored by the IEEE Circuits and Systems Society. They may be interested in having SIGDA as a co-sponsor. ICCAD is not a big money-maker, but is a strong technical conference and one which we already support indirectly through our Travel Grant Program. We need to be sure, however, that the current sponsors of ICCAD are in favor of such a move, so as not to damage our good working relationship with them.

MOTION: *If invited, it is the sense of the SIGDA Advisory Board that we support SIGDA co-sponsorship of ICCAD.* ***(Radke, Brglez, 9-0-2)***

Weil presented a list of 11 workshops being organized for fiscal year 1991. These included a workshop and tutorial in Leningrad, USSR, but local arrangements may be a problem, which they are now trying to resolve. Weil pointed out that over half the proposals he receives are turned down for lack of planning. There are sometimes problems with ACM organizing fees, particularly for co-sponsored workshops.

MOTION: *SIGDA will advance an $8,000 organizing fee to any workshop it sponsors (to be paid to ACM or other organizing agency) which is not included on the TMRF. If there is a surplus from the workshop, they*

must pay this amount back to SIGDA before any profit is split among the sponsors (otherwise SIGDA will absorb this cost). ***(Weil, Cohoon, 10-0-1)***

The question was raised whether, as a matter of policy, we should favor having a single sponsor per workshop and allow additional potential sponsors to have "in-cooperation with" status. Sponsorship could alternate between societies each year. Dual sponsorship is a large coordination effort between societies. No action was taken on this matter.

MOTION: *SIGDA allocate $7,000 for a computer for the workshop program.* ***(Cohoon, Hefferan, unanimous)***

Last year was the first year for the European Design Automation Conference (EDAC). They have bootstrapped themselves without sponsorship. No formal request for '91 has been made, but they are likely to request "in-cooperation with" status from SIGDA. There was support among the Board for some kind of association, but several questions must first be resolved including DAC EC's concerns about "look and feel" issues. Is there an actual sponsoring organization (or some legal entity)? Do they have liability insurance? Do they have cooperation of other European professional societies? Weil will be traveling to Europe to meet with them in the near future to discuss possible relationships between EDAC and SIGDA.

Q. Travel Grants

Cohoon announced that by not paying for meals he has been able to allow more people to participate in the grant program without causing hardship on the part of the recipients. Approximately 50% of the awards are for travel to DAC, and another 20% to ICCAD. He averages about three awards per each SIGDA sponsored workshop. He announced that they are planning on five Eastern European awards for DAC again this year. He is also trying to encourage more Asian recipients.

R. Publication Chair Search

Shaw is looking for more recommendations for a Publications Chair to serve on the Board (replacing Waldo Magnuson who recently retired). An International Journal of Design Automation is something this Board Member might consider (in addition to textbook and bibliography projects). Several names were suggested and Shaw agreed to follow up on them.

S. DATC

Ron Waxman announced that he is approaching the end of his two-year tenure as DATC chair. The new chair will be Joanne DeGroat. Waxman reported that his requested (but not yet approved) budget for the coming year is $120,000. Last year it was $45,000 (compared to the $30,000 cap of previous years).

T. Outstanding Member Awards

Radke solicited recommendations for the '91 awards. He reminded the group that no more than one of the two recipients can be current Board Members. Paul Weil suggested awards be made to workshop chairs (in addition to the outstanding member awards).

U. DAC '91

Shaw announced that the conference will take place in San Francisco in June. Relationships with U.S. companies are improving. Dates for future DACs are being pushed to earlier in June (away from end of the fiscal year). The committee is still trying to keep the dates after graduations. Mid-June seems to be the best compromise here. Next year, an Industrial Liaison position will be added to the DAC Executive Committee to

help them respond to concerns of the exhibiting companies.

This year DAC is "in cooperation with" the IEEE Circuits and Systems Society. Discussions of possible co-sponsorship are ongoing. Deblasi asked whether SIGDA feels we should encourage such a relationship.

MOTION: *The SIGDA board would like to see that SIGDA financial interest be protected and that there be a five year transition plan for additional co-sponsorship for DAC.* ***(Radke, Cohoon, DEFEATED 2-5-4)***

MOTION: *The SIGDA Board favors the inclusion of the IEEE Circuits and Systems Society as a co-sponsor of DAC provided that the distribution of funds and other matters can be worked out to the satisfaction of all parties.* ***(Radke, Lorenzetti, 10-0-1)***

V. Benchmarks

Brglez summarized the Benchmark Program. He reported that a proposal is being drafted for a benchmark session at DAC'91. He requested suggestions for a chairperson, should the session be accepted. The Board requested a report on the preparation of bibliographies of benchmark citations at the next meeting.

W. Leningrad Workshop

Weil informed us that, for the workshop in Leningrad, hotel rooms must be prepaid in order to reserve them. This money may not be refundable, should the workshop fall through for some reason.

MOTION: *Approve the expenditure of up to $50,000 to make arrangements for the Leningrad Workshop.* ***(Weil, Radke, unanimous)***

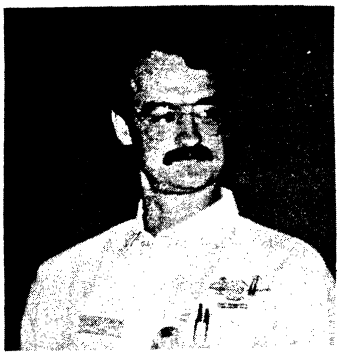
X. New Officer Elections

Shaw announced that Dick Smith is soliciting nominations for officers for next year. Recommendations for nominees should be made directly to Smith.

The meeting was adjourned at this point.

Respectfully Submitted,

Michael J. Lorenzetti
SIGDA Secretary/Treasurer



SIGDA ADVISORY BOARD MEETING MINUTES

The SIGDA Advisory Board Meeting was called to order at 9:20 a.m. on **November 11, 1990** by Chairman Chuck Shaw. In attendance were Board Members Franc Brglez, Jim Cohoon, Joanne DeGroat, Patrick Hefferan, Mary Jane Irwin, Michael Lorenzetti, Bryan Preas, Chuck Radke, Paul Weil, and Akihiko Yamada. Also in attendance were Debbie Hall from ACM Headquarters and Kathy Preas from the CD-ROM Project.

A. Minutes

MOTION: *The minutes of the September 16, 1990 SIGDA Board meeting be approved as submitted.* ***(Weil, Irwin, unanimous)***

B. Financial

Secretary/Treasurer Michael Lorenzetti reviewed the financial status of SIGDA. The fund balance is $1,078,400 as of September 30, 1990. For fiscal year 1990, our expenses exceeded our revenues by $166,000, which indicates we are beginning to apply our massive fund balance to services for the DA profession.

Lorenzetti brought up the subject of DAC sponsorship. Negotiations are in progress to add the IEEE Circuits and Systems Society as a co-sponsor of DAC. It is unclear at this point what the division of costs and surpluses will be. In case the result is an even three-way split of surplus, SIGDA should have a contingency plan for adjusting to the decrease in revenues. It was suggested that in this event we request that the DAC take over the funding of both the scholarship programs (High School and Graduate). This would remove a total of $230,000 in expenditures from our annual budget.

This led to a discussion of the larger issue of multi-sponsorship of conferences. Should we adopt a position requesting compensating influence in other conferences? The conferences of interest to the DA profession include DAC, ICCAD, EDAC, EuroDAC and, to a lesser extent, CICC, ITC and ICCD. After much discussion of the wording of such a position, the following motion was passed.

MOTION: *SIGDA requests that the Computer Society, ACM and the Circuits and Systems Society expand the discussion of sponsorship of DAC to include formulating a unified approach to sponsorship of CAD related conferences, such as ICCAD, DAC, EDAC and EuroDAC.* ***(Weil, Brglez, 10-1-0)***

The intent is that we have more cooperation among societies in conference activities and avoid an adversarial relationship, as in the case of recent EDAC activities. SIGDA wishes to work toward a unified approach to conference activity among the societies.

C. EDAC

Paul Weil brought the group up to date on the European Design Automation Conference (EDAC) situation. At this point we still have not received written evidence that the conference organizers are a legal entity. We also need evidence of insurance. EDAC continues to imply close cooperation with DAC (through use of our mail list, and by maintaining a DAC "look-and-feel") although no relationship exists.

There are coordination problems in dealing with conferences and workshops held overseas. Perhaps SIGDA should have a policy specific to such meetings. The following three guidelines for dealing with such meetings were proposed:

(1) the conference be sponsored by a professional society or government,

(2) SIGDA must be a co-sponsor (even if this is just a small percentage) with review responsibility, and

(3) the conference have a cooperative relationship with other professional activities.

(Dick Smith joined the meeting at this point). It was pointed out that the reason for criteria (2) above is to keep us involved in the decision-making process for the conference in order to avoid misunderstandings due to lack of communication. "In co-operation with" status is not adequate to do this when the conference is organized and run overseas.

MOTION: *Accept the three guidelines (outlined above) in negotiating SIGDA involvement with any international conference.* ***(Radke, Preas, unanimous)***

D. Planning and Future Meetings

Preas suggested a planning meeting like the one held in 1988, in which we would review funding levels for all projects, and discuss new project proposals. Shaw agreed to schedule a two-day meeting in early spring (March), maybe during CSC in San Antonio.

E. Newsletter

Pat Hefferan reported on the Newsletter, which continues to be published three times per year. The most recent issues were Dececember 1989, June 1990 and October 1990. The next issue (December 1990) will include an invited article on ASIC Design in VHDL. Mary Jane Irwin suggested that we solicit papers from our workshops. We could ask the organizers for the best papers from these workshops (in addition to the summary already submitted).

Hefferan went on to discuss the Membership Benefits Program - about $9,000 has been spent so far. VHDL manuals, EDIF manuals, 25 years of DAC and DAC and ICCAD proceedings are available to members at $5 per copy. Members who take advantage of these benefits are mostly students and professors, many from Pacific rim.

MOTION: *The SIGDA Board expresses its appreciation to Pat Hefferan for his efforts on the Newsletter and for the membership benefit program.* ***(Radke, Acken, unanimous)***

F. CD-ROM

Kathy Preas reported that contracts have been signed with SAZTEC and RTI. They are currently negotiating license agreements with KSC. Both single-user and multi-user licenses will be offered. Provisions will be offered for multi-users at the same time. Production test has begun. Changes have been made in capture specs and design as a result of prototype evaluation. Preas reported on delays with getting agreements with the Circuits and Systems Society. We must get their approval for Transactions on CAD. Preas is pursuing this with IEEE Press and Chuck Radke agreed to assist.

The final DA Library will be ready in October. This schedule may be moved up if quality is found to be high during evaluations. A total budget of $778K has been authorized (plus $100K for ACM support). So far, $110,000 has been spent and the remainder will be expended during the coming year. Shaw asked for ways to publicize the project and give recognition to the Preases, perhaps by presenting a paper at a publication conferences. Preas agreed to pursue this.

G. Elections

Smith reported that there is only one nomination so far. He wants to complete the slate by the end of the week and asked Board Members to come to him with suggestions. If we get it in the next Newsletter, we can avoid a special mailing. Slates must be submitted to ACM by December 3.

H. ACM HQ Costs Allocations and Budgeting Methods

Debbie Hall announced that there will be major changes in HQ allocation charges. ACM Headquarters took fiscal year 1990 HQ support amounts ($116,000 for SIGDA) and used them to calculate fees for fiscal year 1992. ACM will have a meeting in March to review and plan how this will be allocated in future years (fiscal year 1993 and beyond). SIG Board Members argued for individual charges instead of a blanket fee. HQ prefers blanket charges so they can budget in advance. SIGs prefer individual charges because they make HQ focus on the services they need most (and are willing to pay for).

Hall recommended bringing these suggestions through the Area Director and insist that he keep us informed. Shaw's motion to scrap this plan was voted down at the meeting in Washington. We could also

work to gain support of the other SIG chairs. It might be productive to propose an alternate plan. One alternative is to sign contracts for services one year in advance. Another is a minimum fee plus additional fees for individual services.

Shaw appointed a subcommittee consisting of Shaw, Lorenzetti, Weil and Irwin to pursue this actively.

I. EDAC

Jochen Jess, chairman of EDAC'91, joined the meeting at this point. He reviewed the history of the conference. It grew out of a CAVE workshop. The first conference committee consisted of many of the CAVE organizers. One goal was to demonstrate technical know-how developed in Europe. They also wanted to include U.S. papers and tutorials. They had 450 attendees at the first meeting. It was originally planned to be biennial, but changed to annual based on the success of the first one.

The flavor of the conference is a topic of discussion among their committee members. They are weighing vendor participation versus a strictly technical workshop. They want to be international with Japanese and U.S. participation. They have floor space this year for use as vendor exhibit area. EuroDAC is viewed as a competitor because they are not sure that the European market can bear two conferences.

He stated that the EDAC association is a non-profit organization "built around a bank account." Gordon Adshead is president, Jess is vice president. The sole purpose of the organization is to run the conference. There is no European-wide professional organization, which is why EDAC exists. It is considered a nucleus of such activities that may become abandoned if a larger group is formed to subsume this work. He stated that the association is established under English law as a non-profit organization.

Board Members requested a copy of the documents establishing this legal entity. They also requested a copy of the conference insurance policy and reiterated their concerns about sponsorship, insurance and cooperation among the conferences sponsored. SIGDA must abide by ACM guidelines and procedures. SIGDA is not concerned about whether EDAC has exhibits, whether the merge with EuroDAC or other organizational decisions. Board Members reviewed our position regarding sponsorship (even in as little as 5%) by SIGDA for international conferences in which we are involved. Joanne DeGroat (the DATC Chair) stated that DATC agrees with the position taken by SIGDA.

Jess summarized his understanding of the SIGDA position:

(1) documentation of non-profit legal status,

(2) evidence of insurance of the conference (not just of the sponsors),

(3) prefer sponsorship over "in-cooperation with" status.

He questioned the difference between "sponsorship" and "in-cooperation" and was informed that some participation in conference organizing and decision-making is involved in sponsorship. Jess explained that these terms are not so well defined in Europe and they have used them somewhat loosely in the past. Mary Jane Irwin provided him with a copy of the ACM procedures on "in-cooperation with" status. Cohoon agreed to send him information from the ACM procedures manual on sponsorship.

Smith pointed out the early concerns of ICCAD overlapping with DAC, which proved to be unimportant. Perhaps this will be the same with EDAC and EuroDAC. Jess responded that there are two completely different groups. EuroDAC represents the "big 12" European companies, EDAC has more membership from academia.

It was agreed that mutual cooperation was important to both SIGDA and EDAC. Jess reiterated his concerns about competition from EuroDAC.

J. Asian Activities

Yamada reviewed the Asian activities, both of IPSJ and in the area of Standards.
IPSJ - SIGDA workshop. He discussed the idea of an Asia-Pacific workshop with both groups. He introduced SIGDA activities to the IPSJ meeting (they are unfamiliar with us). He distributed copies of our brochures and Newsletters to them. There was general support, but no chairman or organization has yet been put in place. Paul Weil agreed to obtain the list of Asian recipients of manuals from Pat Hefferan and send them invitation to participate in organizing such a workshop.

InfoJapan '90 was held October 1-5. It attracted 1335 attendees and was very successful.

IPSJ sponsors several workshops: October 8-9 on Test; December 11-12 on Logic Synthesis. Weil asked whether can we publish papers or abstracts from these workshops in the Newsletter. Yamada will check this out with IPSJ, (perhaps only the abstracts since they are already in English and printing them would not prevent the authors from republishing in other journals).

EDIF - EIAJ EDIF committee met in April 1990. They will hold an EDIF forum in December 1990.

VHDL - preliminary discussions were held September 21. There is a U.S.-Japan meeting to be held here on November 15. They hope to establish a Japanese VHDL group.

K. University Booth

Cohoon announced that Japanese universities want to participate, but need NEC machines to do so. Cohoon will investigate getting them. International participation in this program would be nice. Steve Levitan has agreed to run the 1992 booth.

L. High School Scholarship

Acken announced that we have seven students attending school under our program, including students at Idaho State, UNLV, UCLA, and Berkeley. The new administrator (Susan Wills, formerly of Daisy) is working out very well. She is an excellent coordinator and meeting planner.

M. Graduate Scholarships

Loomis reported that we are again awarding ten scholarships of $12,000 each. Foreign applicants have been few, which may indicate we are not getting the word out internationally. It was pointed out that we do support many foreign students in American universities. Approximately 53 proposals were received last year.

There was some discussion of the amounts for scholarships. It was pointed out that stipends for graduate students run closer to $14,000. It was also pointed out that if we are considering asking DAC to take over funding of this program, decisions on the amount should be left to them.

MOTION: *For Chuck Shaw (the SIGDA representative on the DAC Executive Committee) to request the DAC to take over funding of the Graduate Scholarship Program.* ***(Lorenzetti, Radke, unanimous)***

Hersch Loomis pointed out that we currently include no statement on the type of DA we support in the announcement. Some proposals specify mechanical DA. Do we want to support them? It was agreed that it is Loomis' responsibility to write up the criteria and the Board suggested "topics covered by the Design Automation Conference" as a possible wording for the announcement.

N. Discretionary Fund

SIG Board is forming a group to evaluate proposals for the SIG Discretionary Fund. This group would pre-screen the proposals before they were voted on by SIG Chairs and SIG Board. Since we are such a large contributor to the Fund, we have been invited to assign a representative to the group. It is in our best interest to assign such a member to help steer the allocation of these funds, since we contribute one third of them.

MOTION: *Chuck Shaw be assigned the task of representing SIGDA on the SIG Discretionary Fund review committee.* ***(Lorenzetti, Weil, unanimous)***

O. ACM Winter Meetings

Debbie Hall reported that the bylaw amendments submitted last March have not yet been approved. She expects they will be approved by conference call in the near future.

Some controversial proposals were voted down by the Conference Board at the last meeting. One was that conference contracts would require approval of all parties (including sponsoring society chairs) and be competitive bids. This was voted down as unworkable and replaced by a simple statement that sound business practice should be employed.

A second proposal was that special discount registration fees be offered to ACM officers and Board Members when they hold a meeting at an ACM-sponsored conference. This was voted down to be only a recommendation and that the amount be large enough to cover real expenses incurred by the conference for each registrant.

P. University Booth

Weil pointed out that the motion we passed at our last meeting regarding a University Booth was specifically for EDAC and perhaps we should broaden the motion to allow it to be done

MOTION: *Up to $50,000 be budgeted for a University Booth at a European conference.* ***(Cohoon, Weil, unanimous)***

Q. Brochure

Chuck Radke announced that after the next officer election, he will print a revised version of the SIGDA Membership Brochure. He requested that Board Members send changes and corrections to him.

R. Travel Grants

Cohoon reported that the program is going well. He requested details on the recent DAC executive committee motion to fund the DAC grants for us. The question was raised whether we should require faculty approval for students to apply. No motion made on this and it was decided that the process should remain informal and requirements be left up to Cohoon.

S. Publication Chair

Shaw announced that he has several candidates for this new board post. He intends to approach them this week during ICCAD.

T. DATC

Joanne DeGroat is the new DATC representative to SIGDA. The IEEE Computer Society has changed its operating procedures. Technical Committees now propose budgets each year and the amount is not fixed as in the past. The budgets come up for approval in the next week. DATC is asking for $127,400. The scope of DATC projects for the coming year depend on the outcome of these budget decisions.

U. Outstanding Member Award

Radke has placed an announcement in the Newsletter requesting nominations for this year's Outstanding Membership Awards. We award two each year, but try to limit them to one person on the current Board. He is looking for nominations.

Shaw informed us that there are awards within ACM, such as the Turing and Grace Murray Hopper awards. SIGs should propose members from their own field to receive these awards. Radke agreed to send out a list of awards and their criteria to board members.

There has recently been a discussion of an ACM Fellows category similar to that of IEEE. This is particularly important not only to the academic community, but also for the industrial community. This came up a few

years ago but did not come about. There is a lot of support among the SIGs to get this program going. He supports it and will keep the Board informed.

V. DAC '91

Shaw reported that there is a push toward listening to the DAC exhibitors and trying to address their concerns. For example, they are trying to move away from the end of the fiscal year and DAC '91 will take place earlier in June than in recent years. These actions have been well received by the exhibitors.

The conference starts on Monday this year (instead of Sunday as in the past). The Exhibitor Technical Program will be Monday, June 17. The technical program will be Tuesday, Wednesday and Thursday and the tutorials will be on Friday.

W. Workshops

Weil reported that we supported eleven workshops this year, half of which were in Europe. He will present details at the general meeting.

X. Evening Meetings

Shaw reported that he received comments last time that our Membership Meeting was more of a lecture. He would like to make it more interactive.

After a brief discussion it was agreed to not present reports on all projects, but only selected ones with important recent activity. Following this we would solicit questions and proposals to make the meeting more interactive.

Y. Press Room Computers

Shaw announced his intention to spend $20K to purchase computers for use in the DAC press room. No action was required since this money was already budgeted for the purchase of hand-held radios for the conference. It was found to be more economical to rent the radios and this money will be used instead for PCs.

Z. Eastern European Travel Grants

Shaw informed us that we continue to receive congratulations on this program. The program was brought up in the Supreme Soviet of the USSR as an example of the benefits of *glasnost*.

We are looking for candidates for next year. Professor Marek-Sadowska has volunteered to help identify candidates in Poland. Egon worked through the scientific communities there last year, asking them to make nominations. It was agreed that we should let their professional society do the selection again this year.

a. Benchmarks

Brglez has proposed a special session for DAC to discuss benchmarks. He intends to talk to Dunlop (the DAC program chair) to get early approval of this session. Brglez is looking for nominations for a session moderator.

b. New Business

Radke has a transcript of Bill Joy's DAC keynote, for anyone who would like to review it. There was a discussion of whether we should publish it in the Newsletter. There are some holes in the transcript which need to be filled in. Radke will pursue getting the missing information from Sun.

The meeting was adjourned at this point.

Respectfully Submitted,

Michael J. Lorenzetti
SIGDA Secretary/Treasurer

SIGDA MEMBERSHIP MEETING MINUTES

The SIGDA Membership Meeting was called to order at 6:00 p.m. on November 11, 1990 by Chairman Chuck Shaw. Thirty-one members were in attendance. He announced that the format would be a brief review of some key projects and then he would solicit input on SIGDA activities. He pointed out that the SIGDA Newsletter is distributed to all ICCAD attendees and that all our activities are summarized therein.

Shaw announced that Chuck Radke is looking for award nominations for service awards from SIGDA, the Turing award and the Grace Murray Hopper award. Please make suggestions to Radke.

Mary Jane Irwin announced that DAC starts on MONDAY this year. The conference has been shifted by one day. Southern Pacific will add extra cars to travel from Silicon Valley to San Francisco.

A. High School Scholarship

Charlette Acken reviewed the purpose of the program, which is to encourage underrepresented minorities (Black, Hispanic, American Indian and women) to enter the DA profession. We have seven students in school under our program, at several universities including Idaho State, UNLV, UCLA and Berkeley. Charlotte is looking for volunteers to act as mentors for these students. Mentors must be CS or EE professionals and be a member of one of the targeted minorities.

B. Graduate Scholarships

Hersch Loomis announced we will again award ten scholarships of $12,000 each, sponsored jointly by DATC and SIGDA. These are awarded based on proposals submitted in the spring. Contact Hersch (or see the Newsletter) for more information.

C. CD-ROM

Bryan Preas reviewed the CD-ROM project. It will be a seven CD-ROM set, which includes retrieval software, and will contain all of the DAC, ICCAD, ICCD, EDAC, Transactions on CAD and the SIGDA Newsletter. It will run on the Sun SPARCstation, Mac and the IBM PC and be distributed through ACM. This project is being run in cooperation with IEEE CS DATC.

Preas gave a brief review of the history of the project. The requirements were formulated in July of 1989. Production will begin in January and distribution is scheduled for third quarter, 1991. Thus far, $110,000 has been invested in the project. The total cost will be near $750,000.

D. Workshops

Paul Weil presented list of workshops for the current fiscal year.

Workshop on Timing Issues in Specification and Synthesis (Tau90)
Vancouver, August 15, 1990
Chair Rick McGeer
Sponsor

Logic Level Modeling for ASICs
Monterey, August 12, 1990
Chair Mark Glasser
Sponsor

Workshop on EDA Frameworks
Charlottesville, November 26, 1990
Chair Ron Waxman
In Cooperation

Workshop on Formal Methods in VLSI Design
Miami, January 9, 1991
Chair P.A. Subrahmanyam [Subra]
Sponsor

Workshop on High Level Synthesis
Black Forest, March 3, 1991
Chair Raul Composano
In Cooperation

Symposium on Computer Hardware Description Languages and Applications
Marseille, April 22, 1991
Chair Dominique Borrione
In Cooperation

Workshop on Logic Synthesis
Research Triangle Park, May 7, 1991
Chair Franc Brglez
In Cooperation

Physical Design Workshop II Nemacolin
Woodlands, PA, May 20-22, 1991
Chair Antun Domic
Sponsor

Leningrad: Workshop and Tutorial
Leningrad, Russia, USSR, June 1991
Chair Jim Cohoon
Sponsor

Workshop on Theory and Practice in Physical Design
Dachstul, Saarland, (Black Forest) Germany, August 25-31, 1991
Chair Thomas Lengauer
In Cooperation

First International Workshop on the Economics of Design and Test
MCC, Texas, September 9-11, 1991
Chair Sarma Sastry
Sponsor

1991 Logic Level Modeling for ASICs
Monterey, August 11, 1991
Chair Mark Glasser
Sponsor

Weil summarized by noting we are involved in eleven workshops within a year's time. SIGDA is interested in fostering development of new workshops and provides a great deal of assistance in planning, as well as funding. Jim Cohoon elaborated on the Leningrad Workshop. It takes place June 3-4 1991. There will be four sessions with five presentations per session, mostly tutorial in nature. The goal is to promote international dissemination of DA information.

E. Elections

Shaw reported that SIGDA will conduct officer elections in the spring and that Dick Smith (Chairman of the Nominations Committee) is soliciting nominations. The nominations are due at ACM headquarters by December 3.

F. New Projects

Shaw requested that members present ideas for new projects. The Board will meet in February to discuss future directions for the organization, so get proposals to us in advance.

G. New Business

Shaw opened the floor for questions and comments at this point.

The first question was on the criteria for graduate scholarship. Loomis reviewed the criteria (from the announcement). These include quality of student, contribution for DA program at the school, and technical quality of the proposal. There were about 55 proposals last year. Members requested more feedback from the committee, particularly when proposals were turned down.

Bryan Preas asked the group whether they felt that SIGDA should publish a journal. He noted that this topic comes up periodically on the Advisory Board. It was pointed out that Transactions on CAD currently has a year and a half lag time on getting articles published, and competition with them is not a real issue. One person suggested a journal for more theoretical work (papers without practical examples or benchmark results, but strictly on theoretical aspects of DA problems). The Board agreed to consider this matter further.

H. Adjourn

Since no other topics were brought up, Shaw thanked the members for their input and adjourned the meeting.

Respectfully Submitted,

Michael J. Lorenzetti
SIGDA Secretary/Treasurer

MEMBERSHIP BENEFITS

As a special benefit to SIGDA members, certain standards manuals, proceedings, and other documents of general interest will be made available at a nominal rate. Availability of the documents may vary, so allow several weeks for delivery. Proceedings will only be issued after the conference sales have been satisfied. ***You must be a member of SIGDA to quality.***

MEMBERSHIP COUPON - DOC.

-SIGDA Membership Sponsored Manual/Proceedings -

Name _____

Address _____

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_____

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ACM Membership Number _____

SELECTIONS (please check box(es))

- ☐ EDIF 2.0.0 Standards Manual
- ☐ VHDL Language Reference Manual
- ☐ 25 Years of Electronic Design Automation
- ☐ 1990 DAC Proceedings
- ☐ 1990 ICCAD Proceedings

Please include a check for $5.00 (made out to ACM/SIGDA) to cover the cost of shipping. ($5.00 per document). Please allow several weeks for shipping and handling. DAC & ICCAD Proceedings mailed only after conference is over. Also, allow extra time for EIA EDIF Publications.

Please send coupon to:
Patrick M. Hefferan
1681 Princeton Avenue
St. Paul, MN 55105

SIGDA MEMBERSHIP SURVEY

In order to better serve the SIGDA membership, we are taking a survey of your wants and needs. Please take a few minutes to fill out the survey form on the next page and send it in. It has a preprinted address on the back, so just cut it out and fold it up with the address facing outward. Then tape (please do not staple) it shut and mail it in. You will need to provide 25 cents postage, as we cannot use our bulk mailing permit for this.

To make this more interesting and provide an incentive to get the surveys filled out, those who participate will be eligible for a drawing for a portable, electronic address book. We want to hear from you - so take a few minutes and fill it out. THANK YOU!!

PLEASE FILL OUT AND SEND IN ---------->

THE WINNER OF THE ELECTRONIC ADDRESS BOOK THIS QUARTER IS ELAINE RITCHIE FROM MARLBORO, MASSACHUSETTS!! THERE WILL BE ANOTHER WINNER ANNOUNCED IN THE NEXT SIGDA NEWSLETTER.

SIGDA SURVEY
January, 1990

This is a general membership survey.
Participants will be entered in a drawing for an electronic address book.

Name _____ EMAIL Address _____
(May we publish this address? _____)

Address _____ Company _____

_____ Occupation _____

_____ Job Function _____

Phone - Home _____ Education _____
(Highest attained)

Work _____

_____
(Signature)

How long have you worked as a DA professional? _____

Computers used in work _____

Do you have a PC at home? _____ If yes, what kind _____

Do you have a modem? _____ *At home?* _____ *At work?* _____ *Speed?* _____

Are you connected to a network (Arpa, CIC, INTERNET?) _____

In what professional societies are you a member? _____

_____

What CAD/CAE functions are you responsible for?

_____ Schematic capture	_____ Simulation	_____ Layout
_____ DRC	_____ Test	_____ Management
_____ Design	_____ Specification	_____ Evaluation
_____ Mechanical	_____ Other _____	

What additional benefits would you like from SIGDA?

_____ DAC Proceedings	_____ DAC/ICCAD Admissions
_____ ICCAD Proceedings	_____ Network Access for EMAIL/BBS
_____ Standards Manuals	_____ Continuing Education _____
_____ Tutorial Tapes	_____ Other _____
_____ CD-ROM Tapes	

Would you pay extra for them? _____ *Yes* _____ *No*

The SIGDA High School Student Mentor Program is designed to increase under-represented groups in the DA profession. The target groups for this program are: Hispanic, Black, Women (all races), Disabled, and American Indian. We are requesting that the Mentors be from the target groups. Also, for administrative purposes, the Mentors must be from the San Francisco Bay Area. For further details, contact Charlotte Acken (address on front cover).

Would you like to be a Mentor? _____ *Yes* _____ *No*

Of which target group are you a member? _____

put 25 cent
stamp here

SIGDA Membership Survey
c/o Patrick M. Hefferan
1681 Princeton Avenue
Saint Paul, Minnesota 55105

SIGDA EMAIL DIRECTORY

Listed below are the EMAIL addresses taken from the Membership Survey. Please check your address and advise us of any changes - either by an EMAIL message[1], a short note, or simply send us the Survey form with a "revised" notation at the top. Drop us a message if you would like to be included in this directory.

Acken, Charlotte ..... cacken@sandia.llnl.gov
Adams, Thomas J. ..... adams@smc.com
Adshead, H. Gordon ..... G.A.ICL@EUROKOM.IE
Baker, William I. ..... bbaker@ece.wsu.edu
Beetem, John F. ..... beetem@engr.wisc.edu
Benton, Ron ..... rrbenton@honeywell.com
Blackburn, Robert ..... rlb7h@virginia.edu
Briner, Jack V. ..... brinerj@hamlet.acc.uncg.edu
Chakravarty, Sreejit ..... sreejit@cs.buffalo.edu
Chapman, Larry ..... Chapman@hpfcla.hp.co
Chen, Kuang-Chien W. ..... kchen@cs.uiuc.edu
Chen, Liang-Gee ..... ntut034@twnmoel0.bitnet
Chen, Wei ..... chen@longs.lance.colostate.edu
Chiang, Charles ..... clc@eecs.nwu.edu
Chung, Kevin ..... chungk@eecg.toronto.edu
Cohoon, James P. ..... cohoon@virginia.edu
Crawford, Robert M. CIS76356,741
DeGroat, JoAnne E. ..... degroat@hathi.eng.ohio-state.edu
Enbody, Richard, Dr. ..... enbody@cps.msu.edu
Fendrich, John W. ..... jwf@bradley.edu
Gorman, Joe ..... jgorman@falls.cray.com
Gu, Jun ..... gu@enel.UCalgary.CA
Gupta, Anurag P. ..... anurag@ece.cmv.edu

[1] Hefferan, Patrick M. ..... hefferan@frith.entmoot.cs.psu.edu

Hemmendinger, David ..... hemmendd@tardis.union.edu
Hughes, J. Gordon ..... JGH@ES2.CO.UK
Irwin, Mary Jane ..... mji@cp.psu.edu
Jost, Allan G. ..... JOST@TUNS.CA
Kaufman, Jerry ..... gjk%hpfcla@hplabs.hp.com
Kim, Heung-Nam ..... hnkim@psuvax1.cs.psu,edu
Kim, Soohong ..... soohong@psuvax1.cs.psu.edu
Kim, Yanggon ..... KWANGMI@GONDOR.CS.PSU.EDU
Krasniewski, Andrzeg ..... ANDY@EE.ROCHESTER.EDU
Kubitz, William ..... kubitz@cs.uiuc.edu
Kukral, Dean ..... DEAN.KUKRAL@WICHITA.NCR.COM
Levitt, Marc ..... Marcl@deli.eng.sun.com
Lin, Youn-Long S. ..... ylin@twnctu01.bitnet
Lis, Joseph ..... jlis@ics.uci.edu
Lobo, Donald A. ..... Lobo@cs.ps.edu
Loomis, Herschel,Jr. ..... loomis@cs.nps.navy.mil
Lorenzetti, Michael ..... mikelor@mentor.com
Lung, Loh Wai ..... AAWAI@NUSVM.BITNET
Magnuson, Waldo G.,Jr. ..... magnuson@icdc.llnl.gov
Marwedel, Peter ..... MARWEDEL@ls12.informatik.uni-dortmund.de
Menchini, Paul ..... mench@clsi.com
Midkiff, Scott F. ..... midkiff@vtvm1.cc.vt.edu
Moh, Teng-Sheng ..... moht@iris.ucdavis.edu

SIGDA EMAIL DIRECTORY (continued)

Nelson, Victor	nelson@eng.auburn.edu
Parmar, Kirti M.	kirti@cadence.com
Preas, Bryan T.	preas@cadlab.cadlab.de
Quayle, Michael S.	quayle@ee.cornell.edu
Radke, Charles E.	C.RADKE@COMPMAIL.COM
Rajsuman, Rochit	rajsuman@alpha.ces.cwru.edu
Ravi, S. S.	ravi@cs.albany.edu
Reeves, Douglas S.	reeves@cscadm.ncsu.edu
Ritchie, Elaine K.	ritchie%hpstek.dec@decwrl.dec.com
Roy, Rabindra K.	roy@bach.csg.uiuc.edu
Rundensteiner, Elke	rundenst@ics.uci.edu
Sarma, Debabrata	sarma@chowser.rutgers.edu
Shaw, Charles A.	shaw@cadence.com
Shi, Edmond	Shi%hycad5@hacZarpa.hac.com
Smith, Richard C.	nsc!parns!ricardo
Spillinger, Ilan	ilan@techunix.bitnet
Stevenson, Carl R.	73065,270@cis.com
Szymanski, Thomas G.	tgs@research.att.com
Tanaka, Yasuhiro	tanaka@rd.nttdata.jp
Taylor, Gordon	gft@genrad.com
Tonkin, Bruce	btonkin@augean.va.oz.au
Trimberger, Steve	uunet!xitinx!steve
Tuan, T. C.	ttuan@uokmax.ecn.uoknor.edu
Walker, Duncan M.	dmw@ece.cmu.edu
Walker, Robert A.	walkerb@cs.rpi.edu
Waxman, Ron	waxman@virginia.edu
Weil, Paul B.	weilcad@frith.cs.psu.edu
Wilsey, Philip A.	paw@ueeng.uc.edu
Wong, Martin	wong@cs.utexas.EDU
Wuu, Tzyh-Yung	wuu@vlsi-cad.isi.edu
Yamada, Akihiko	a.yamada@compmail.com

SLATE OF OFFICERS

Notification of Slate for 1991 SIGDA Election

The Nominating Committee has proposed the following candidates for the SIGDA election to be held this Spring:

CHAIR

Michael Lorenzetti	Mentor Graphics Corporation
Charles E. Radke	IBM

VICE CHAIR

Susan Ayers	Alliant Computer Systems
Charlotte Acken	Sandia National Laboratories

SECRETARY/TREASURER

Patrick Hefferan	Consultant
Scott Baeder	Cadence Design Systems

In accordance with the SIGDA Bylaws, additional candidates may be placed on the ballot by petition. Individuals who wish to petition must inform ACM Headquarters (Pat Ryan), the SIGDA Area Director (Sig Treu), and the SIGDA Secretary (Patrick Hefferan) of their intent to do so by March, 15, 1991. A petition must be signed by one percent (1%) of the SIGDA membership, and must be recevied by the SIGDA Secretary no later than April 14, 1991. All candidates must be voting members of ACM and SIGDA members.

Richard Smith
Nominating Chair

Universität
Gesamthochschule Paderborn

Fachbereich 17 · Mathematik - Informatik
Thomas Lengauer
Dr. rer. nat., Ph. D.
Professor für Informatik

Universität-Gesamthochschule-Paderborn·Postf. 1621·4790 Paderborn

Zimmer Nr.: C2.335
Telefon (05251) 600 oder
Durchwahl 60 - 2066/2067
Telefax: 60 - 3836

Patrick M. Hefferan
SIGDA Editor
1681 Princeton Ave.
USA – St. Paul, MN 55105

Dear Mr. Hefferan,

my book

Combinatorial Algorithms for Integrated Circuit Layout

(overview attached) which has been published within in the Wiley-Teubner Series of "Applicable Theory in Computer Science" in August 1990 has been supported by a book grant by SIGDA over $ 10.000,–. The grant was awarded upon the suggestion of Dr. Bryan Preas (XEROX PARC) and administered by Dr. Waldo Magnuson (Lawrence Livermore Labs).

May I take this opportunity to express my sincere thanks to SIGDA and all people involved. The grant was a key to the timely completion of the book and has raised its production quality significantly. Specifically, the grant enabled me to hire a professional copy editor (Lyn Dupre from Mountain View, California) as well as to have the figures drawn professionally. In addition, I could pay proofreaders of the final version of the book. I estimate that without the grant the book would have been completed with a year's delay and contain many substantial errors, especially concerning language.

In my opinion, the book grant program by SIGDA with its special characteristics, e.g., no strings attached with respect to publishers or form, is a very effective instrument for propelling the creation of much needed textbooks for the field of design automation. Thanks for this fabulous idea.

Sincerely yours,

(Prof. Dr. T. Lengauer)

Editor'sNote: See page 113 for advertisement of the book produced by this grant

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Applied Sciences, Room 315b
Computer Engineering
University of California
Santa Cruz, CA 95064 USA

Internet: karplus@ce.ucsc.edu
(408) 459-4250
November 21, 1990

Pat Hefferan, SIGDA Editor
1681 Princeton Ave.
St. Paul, MN 55105

Dear Dr. Hefferan,

I would like to have my Internet address listed in the SIGDA e-mail listing. I am not a SIGDA member (not even an ACM member!), but I am the Local Arrangements chair for the Advanced Research in VLSI conference, which is being held here at UCSC this Spring.

The conference is a $2\frac{1}{2}$-day conference, 25–27 March 1991. This will be the thirteenth in the series of Advanced Research in VLSI conferences, but the first one at UCSC. Previous conference have been hosted by Caltech, MIT, University of North Carolina at Chapel Hill, and Stanford.

The program chair tells me that the committee has selected 22 contributed papers this year, and that we'll have four or five invited talks as well. I will send you a copy of the program as soon as we have it finalized.

Sincerely,

Kevin Karplus

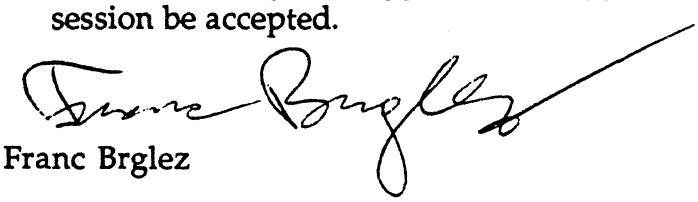
Departments

The following pages contain updates and information about various projects and activities funded by the SIGDA. Contact information (e-mail, phone, and addresses) for the individuals directing the programs can be found on the inside front cover.

Benchmarks.....Franc Brglez

Activities during July - September, 1990

- Logic Synthesis Workshop'91 announcement with "in Cooperation with ACM® SIGDA" status has been mailed out (sample attached).
- Another report on CD-ROM disk use has been e-mailed by Matt Melton, new student member from MCNC.
- European contact on benchmarking effort has been initiated and we mailed several benchmark sets recently to Grenoble, France (upon request).
- A letter has been drafted to be enclosed with every benchmark tape we distribute, acknowledging support from ACM® SIGDA (attached for board review and approval).
- We advertised for two student positions to assist in preparation, testing and and documentation of benchmarking effort. We hired two experienced graduate students from NCSU for September'90 - May'91 period (workstatements are attached).
- A draft proposal for benchmark session at DAC'91 is in progress: the session may have four major contributing teams covering high level synthesis, logic synthesis, test and verification, and layout synthesis. Each presentation will aim to select benchmarks that provide some measure of continuity with other disciplines. Ideally, the session may offer data points of individual experience that will span unique designs from highest level of specification to IC layout. I am preparing to organize the session and participate on some of the teams, but I am still looking for suggestions to approach a dynamic chairperson, should the session be accepted.



Franc Brglez

919-248-1925
brglez@mcnc.org

Student position #1: Logic Synthesis Benchmark Generation

Student: Doug Maltais, M.S. Program in ECE, NCSU, Raleigh

Project mentors: Saeyang Yang, MCNC
Franc Brglez, MCNC

Purpose

- To consolidate the existing set of benchmarks, to assist in generation of the additional set with emphasis on sequential designs, to provide a set of data points and guidelines and to prepare documentation for the 1991 set to be used in the Logic Synthesis'91 Workshop. This work will cross-reference with the benchmark set in a companion project compiled for test generation and logic verification. Both sets will contribute netlist and libraries towards the Layout Synthesis Workshop'92 benchmark set.

Background

- Prior work on benchmarks for logic synthesis has been documented in [1-3].

Proposed Milestones

- By November 7, 1990: prepare a draft outline for the proposed set, participate in the prospective DAC'91 submission.
- By January 15, 1991: prepare a beta-release of the benchmark set
- By February 28, 1991: prepare general release of the benchmark set
- By May 15, 1991: complete the last benchmark update, summarize the experience for the ACM Newsletter.

References

[1] Art De Geus, "Logic Synthesis Benchmarks", DAC'86

[2] Art De Geus, "Logic Synthesis Benchmarks", International Workshop on Logic Synthesis, MCNC, May 1987

[3] Robert Lisanke, "Logic Synthesis Benchmarks: User Guide", International Workshop on Logic Synthesis, MCNC, May 1989

Student position #2: Test and Verification Benchmark Generation

Student: Matt Melton, M.S. Program in ECE, NCSU, Raleigh

Project mentors: David Bryan, MCNC
Franc Brglez, MCNC

Purpose

- To consolidate the existing set of benchmarks, to assist in generation of the additional set with emphasis on sequential as well as bus-structured and board designs that use boundary scan. This work will cross-reference with the benchmark set in a companion project being compiled for logic synthesis. Both sets will contribute netlist and libraries towards the Layout Synthesis Workshop'92 benchmark set.

Background

- Prior work on benchmarks for test pattern generation has been documented in [1-2].

Proposed Milestones

- By November 7, 1990: prepare a draft outline for the proposed set, participate in the prospective DAC'91 submission.
- By January 15, 1991: prepare a beta-release of the benchmark set.
- By February 28, 1991: prepare general release of the benchmark set
- By May 15, 1991: complete the last benchmark update, summarize the experience for the ACM Newsletter.

References

[1] Franc Brglez, Hideo Fujiwara, "A Neutral Netlist of 10 Combinational Benchmark Circuits and a Target Translator in FORTRAN", Intl. Symp. Circuits and Systems, June 1985.

[2] Franc Brglez, David Bryan, Krzysztof Kozminski, "Combinational Profiles of Sequential Benchmark Circuits", Intl. Symp. Circuits and Systems, May 1989.

Scholarship Program .....Herschel Loomis

SIGDA-DATC DESIGN AUTOMATION GRADUATE SCHOLARSHIPS

» The ACM SIGDA and its colleagues in the IEEE DATC are sponsoring ten scholarships of $12,000 each to support graduate research and study in Design Automation, with emphasis in "electronic and computer design and test automation." These scholarships are awarded directly to a university for the Faculty Investigator to expend in accordance with the proposal.

» Scholarships can be awarded in support of new projects or for renewal of any of the previous year's grants.

» The university receiving such a scholarship is then free to use this money in direct support of one or more of its Design Automation graduate students in the manner outlined in its proposal, except that the scholarship funds shall NOT be used to support indirect costs or overhead.

» The Faculty Investigator of the project receiving a scholarship award will be expected to submit a brief report of the year's activities supported by the scholarship for publication in the *SIGDA Newsletter*. This report should be submitted at the conclusion of the year supported.

» Applications for the scholarship, either new or renewal, should be submitted by the Faculty Investigator or department chairman and should include:

a. A brief biography and transcript of the student(s) proposed for the scholarship;
b. A paragraph for each student proposed outlining his or her goals and objectives;
c. A brief proposal concerning the research to be conducted and the way in which the scholarship is to be expended;
d. A brief statement of the impact of the scholarship on the Design Automation Program at her or his institution.

» Scholarships will be awarded based on the following criteria:

a. Academic credentials of the student;
b. Quality of the proposed research;
c. Impact of the award on the DA program at the institution.

» Preference will be given to institutions which are trying to establish new DA research programs.

» Applications should be received by Monday, 1 April 1991 by:

H. H. Loomis, Jr.
Department of Electrical and Computer Engineering,
Code EC/Lm
Naval Postgraduate School
Monterey, CA 93943-5000

For further information contact Hersch Loomis at (408) 646-3214 or on MILNET at loomis@ece.nps.navy.mil. Notification of the awards will be made on 1 May 1991.

DATAPLAN PROJECT FOR SIGS ..... Lorraine Borman

CALL FOR PARTICIPANTS

1. ELECTRONIC GROUP INTERACTIVE SESSION (EGIS) WITH ACM SIG MEMBERS

2. ELECTRONIC GROUP INTERACTIVE SESSION (EGIS) WITH ACM STUDENT MEMBERS

There's a great deal of excitement within ACM lately as a result of the adoption, by ACM Council, of a "Strategic Plan for the 1990's". A summary of the plan appears in the December 1989 issue of *Communications*. The plan calls for, among other things, a major effort to gather information about the needs and desires of members (and non-members) of ACM and its sub-units in order to make ACM more responsive to the needs of these individuals and to set ACM's future directions. Information will be gathered via traditional mail surveys, face-to-face focus groups, and an experimental concept called EGIS (Electronic Group Interactive Session). An EGIS is a discussion group conducted over a period of time using electronic mail.

We are currently forming two EGIS groups made up of approximately 20-30 members each. The first group will consist of members of ACM SIGs (who may or may not be members of ACM). Please note that for this particular part of the project, we are primarily interested in SIG members who have not recently held leadership positions in their SIGs. The second group will consist of Student members of ACM. From both groups, we are interested in hearing views on current and future ACM programs, products, and services.

The questions to be discussed by the groups will primarily be in regard to the professional needs participants have and whether or not those needs are currently being met by ACM or any other organization or service.

The groups will run over a two-week period (April 2 - April 15, 1991). Selection will be based on certain criteria (e.g., location, length of membership, etc.) with the aim of having the group represent, to the extent possible, the relevant ACM population. The protocol and process for managing the groups are currently under review and will be explained in future communications. If you are interested in participating in one of the groups, (**you must be committed to using email regularly,** i.e., we expect that participants will read and respond to discussion group mail on a daily basis), please send the following information to the group's coordinator, Lorraine Borman (email is preferred, but US mail is OK; see address at the end of this memo) by **March 15, 1991.** Individuals selected to participate will be notified by March 22, 1991.

Name
Mailing Address
Telephone Number(s)
E-mail Address
EGIS in which you'd like to participate (SIG or Student members)

Please answer the following questions (to help us form a balanced group), noting the question numbers in your response.

FOR THE EGIS WITH MEMBERS OF ACM SIGS:

1. To which SIG(s) do you belong?

2. How long have you been a SIG member?

3. Do you currently hold a major office or position in the SIG (Chair, Vice-Chair, Secretary, Treasurer, Newsletter Editor, Advisory Board member) or have you held such an office or position within the past year? If so, which one?

4. Are you a member of ACM? Category? (Voting, Associate, Student)

5. Are you a member of an ACM Chapter, Student Chapter, Local SIG?

6. Are you primarily an educator? researcher? practitioner? manager? student?

FOR THE EGIS WITH STUDENT MEMBERS OF ACM:

1. Are you an undergraduate or graduate student?

2. How long have you been a student member of ACM?

3. Are you a member of ACM SIGs? Which one(s)?

4. Are you a member of an ACM Chapter, Student Chapter, Local SIG?

5. Do you currently hold a major office or position in a SIG, Chapter, Student Chapter, Local SIG (Chair, Vice-Chair, Secretary, Treasurer, Newsletter Editor, Advisory Board member) or have you held such an office or position within the past year? If so, which one?

We appreciate your interest in ACM and expect that your participation in our project will be rewarding for you as well as beneficial for ACM. It's your chance to say what you want from your computing society...and be part of an interesting process!

Thank you very much. I am looking forward to hearing from you.

Lorraine Borman
Chair, DataPlan Committee

Email: Borman.chi@xerox.com

US mail: 1865B Tanglewood Drive, Glenview, IL 60025

ASIC design in VHDL
By
David B. Alford

In the past several years, a new hardware description language has emerged as a standard in the electronic computer aided design world. Named the VHSIC Hardware Design Language(the first CAD language to have a recursive acronym), it is quickly being adopted throughout the electronics industry as the design language of choice. Two factors are driving the swift adoption of this language: many CAE vendors are supporting the language for design and simulation purposes, and hardware synthesis using the HDL has become a working reality. ASIC design in the VHSIC Hardware Description Language is proliferating throughout the electronic design world.

VHDL was originally designed by a group of people in the industry to become a standard. This group had several goals in mind. These goals are the use of the VHDL language as a design tool, a documentation tool and a simulation tool. This paper will explore these three goals in depth, as well as their impact on ASIC design.

I. VHDL as a Design Language.

Due to the nature of the paradigms of many of the simulators that were on the market at the time the VHDL standards group started their work in the

early 1980's, the group desired to have higher flexibility in defining a description language paradigm. For this reason, they specified in the VHDL standard known as the Language Reference Manual that not only would the language support data types that were typical of simulators currently available, but support for user-definable data types must be included. The data types that were typically available were bit(scalar), bit vector and integer(vector). Support for these types was included as well as data type values other than a 1, 0 or X state.

It was not adequate to just declare that user-defined data types be supported in the language, a methodology for resolving multiple driven signals of the user-defined data type, as well as the redefinition of binary and arithmetic operators available for the default data types had to be included into the standard. With these three elements, the newly defined language had a powerful capability known as a **Redefinable Paradigm** that allowed the user to completely reshape the design and simulation environment he worked under.

To resolve multiple driven signals of a user-defined type, the standard allows the declaration of resolution functions for both scalar and vector signal types. The problem with multiple driven signals, is in determining which signal overrides the drive of the other signals, or how all signals are combined and in what form to resolve the node value so that a single value for the node is derived. This can be a complex derivation, based upon what technology is being used, how the signals are being combined(wired or, wired and, wired x...) and what are the components of the signal(state and strength). In the standard specification, if the user defines their own data types, they must also define a resolution function, as well, if they plan to use multiple driven signals. The illustration in Figure 1. graphically depicts the problem of a multiple driven signal, and how a resolution function is invoked to determine the actual data value.

Resolving User Defined Data Types in the Redefinable Paradigm of VHDL.

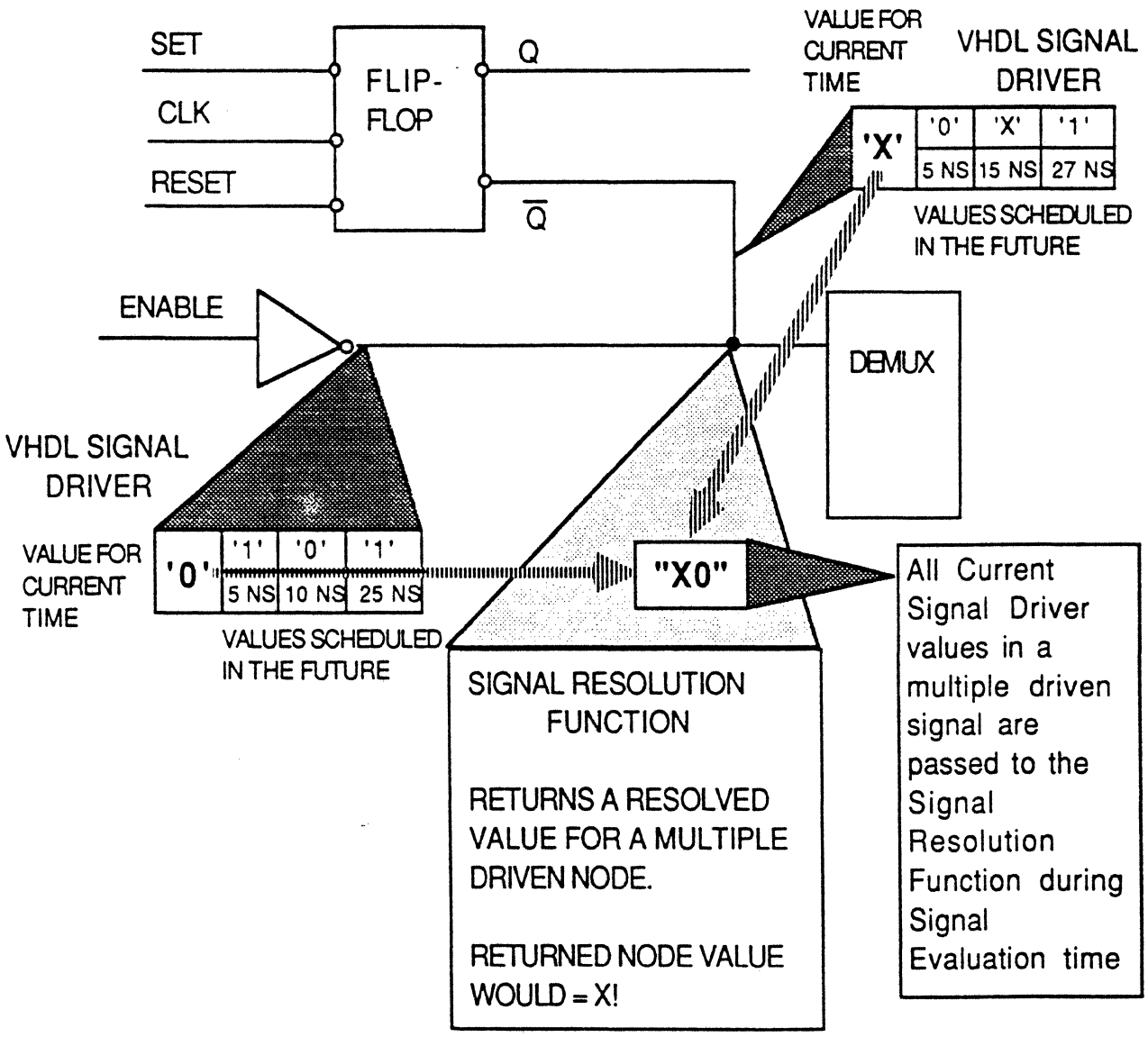


Figure 1.

Most user-defined resolution functions are driven by lookup tables that are indexed using the different values of the user-defined type. The following is an example of a user defined enumerated type, that is being advocated by a group known as the VHDL Design Exchange Group(VDEG), who are currently working toward a standard paradigm within the VHDL design community for the easy exchange of models.

MVL8 Paradigm (MVL = Multi Valued Logic)

```
Type  MVL8 is ('U',    -- Uninitialized as opposed to unknown
             'X',     -- strong X (strong unknown)
             '0',     -- strong 0 (strong low)
             '1',     -- strong 1 (strong high)
             'Z',     -- tristate X (high impedance)
             'W',    -- weak X ( weak unknown)
             'L',    -- weak 0 (weak low)
             'H');  -- weak 1 (weak high)

Type MVL8_VECTOR is array (Natural range <>) of MVL8;
```

The Wired-X lookup table to drive the resolved MVL8 type is defined as follows:

	'U'	'X'	'0'	'1'	'Z'	'W'	'L'	'H'
'U'	'U'	'U'	'U'	'U'	'U'	'U'	'U'	'U'
'X'	'U'	'X'	'X'	'X'	'X'	'X'	'X'	'X'
'0'	'U'	'X'	'0'	'X'	'0'	'0'	'0'	'0'
'1'	'U'	'X'	'X'	'1'	'1'	'1'	'1'	'1'
'Z'	'U'	'X'	'0'	'1'	'Z'	'W'	'L'	'H'
'W'	'U'	'X'	'0'	'1'	'W'	'W'	'W'	'W'
'L'	'U'	'X'	'0'	'1'	'L'	'W'	'L'	'W'
'H'	'U'	'X'	'0'	'1'	'H'	'W'	'W'	'H'

Table 1.

The use of the 'U' state differentiates a signal from an unknown or 'X' state, as opposed to an uninitialized or never touched state. The VHDL standard requires that all uninitialized signals be given a default value of the leftmost defined element of the signal data type. It is good modeling sense and style to always start a simulation at a known point with all signals at an initialized state. The inclusion of the 'U' state as the strongest strength of the 8 state paradigm facilitates the quick identification to the design engineer of uninitialized signals by always remaining in the 'U' state during a simulation.

The third element of the redefinable paradigm is the inclusion of an overloaded operator definition. The concept of the overloaded operator was first introduced in the standard software language ADA. Overloading allows the user to define how the software takes the user defined data type and operates or does functions between two variables or signals defined to be of the newly created type. The addition of two integer numbers and the exclusive-oring of two bits together are part of the default capability of the language, and are quite straight forward. However, how two MVL8 data types are exclusive-ored together must be defined, much as the signal resolution function is defined. Again, these types of functions are typically table driven, with the function defined as follows:

```
function "xor" (L, R, MVL8) return MVL8 is
    begin
            return tbl_XOR(L,R);
    end "xor";
```

The lookup table is defined as an array constant with predictable values, again indexed using the multiple values defined in the users data type. This simple yet powerful method allows redefinition or overloading of operators and functions. The **Redefinable Paradigm** is quite possibly one of the strongest points about VHDL that is currently driving its' popularity.

Another very strong point about VHDL as a design language, is its' ability to define designs at multiple abstraction levels. These design levels range from the Algorithmic/Behavioral to Data Flow/Register-Transfer down to

Primitive/Structural. VHDL easily allows mixed-mode simulation among any of these levels with a rich configuration capability. The language easily supports Top-Down, Bottom-Up, Inside-Out, or whatever kind of design methodology an engineer wishes to use.

The **Redefinable Paradigm** coupled with the ability to define designs at multiple levels gives VHDL a clear advantage as a design language over most proprietary simulators on the market today. Many ASIC foundries are beginning to adopt and support VHDL as a design language, as well as supporting the fabrication of silicon from a VHDL description.

II. VHDL as a Simulation Language.

The group defining the VHSIC Hardware Description Language standard also defined the methodology for simulating the design descriptions defined in the language. Software languages such as 'C' or Pascal are single threaded sequential languages which were inadequate for doing the multi-threaded concurrent processing need for hardware simulation. The algorithm as specified is event driven with separate signal evaluation and process execution iterations. The separation of the process execution from the signal evaluation overcomes problems inherent with single threaded sequential languages, and establishes a concurrent multiple threaded system which correctly emulates hardware.

The illustration in Figure 2 graphically depicts how the VHDL simulation algorithm works. The algorithm has two basic inner loops, signal evaluation and process executions. The outer loop serves as an iterative path from the end of the process execution loop back to the beginning of the signal evaluation loop. This implements the VHDL concept of delta time, or cycle times between the actual advancing of the simulation time clock. During delta time, signal evaluation will wake up processes, and inside of processes, new signal assignments are made, that are evaluated during the next delta time cycle. These delta time cycles continue to occur until all signal evaluations for this time cycle have been made, and all processes are blocked, waiting for time to advance. At that point, the simulator determines the next pending event by searching the signal drivers, described

in Figure 1, for the delta time to the next scheduled event. At this point the simulator increments simulation TIME by this delta to begin processing at the next event. The delta time cycles of signal evaluation loops followed by process execution loops are again repeated for the next simulation time period.

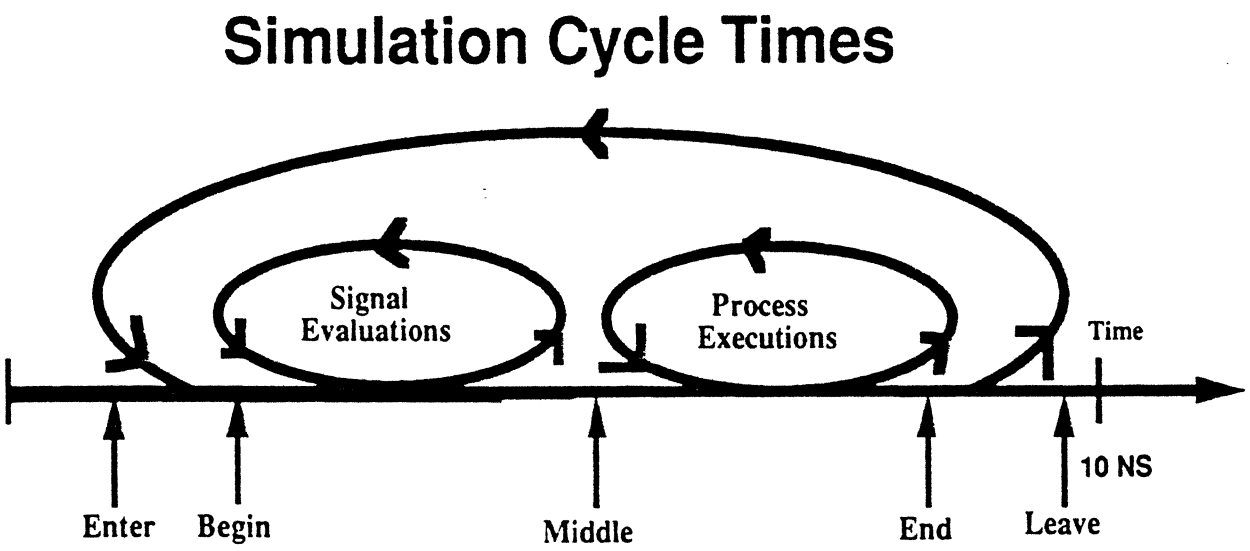


Figure 2.

All simulators that conform to the VHDL specification implement this algorithm. How they do the actual process executions, and signal evaluations varies from one implementation to another. Some vendors translate the VHDL code to 'C' or ADA, while another builds a stream of intermediate code instructions that is executed by the simulator. This intermediate code stream defines what is done during process executions loops, as well as during bus resolution and data type conversion functions in the signal assignment loops, of the delta time cycle.

Referring back to the original graphic that describes the simulation algorithm, you will see points along the time line marked as Enter, Begin, Middle, End and Leave. These points correspond to the time within the delta cycle that the simulator should be able to set and execute breakpoints, although this is not specified in the Language standard. Enter and Leave are

fairly straight forward. As you enter a time cycle or leave a time cycle, you may stop the simulation and view signal values. The Begin, Middle and End points allow stopping the simulation as a signal evaluation loop begins, or after it ends and before a process execution loop begins, or after the process execution loop is complete. This means that there could be multiple breakpoints within the delta time cycles. If there is only one signal evaluation loop, and one process execution during a delta time cycle, these breakpoints will only occur once. However, if there are multiple iterations through the signal evaluation and process execution loops then multiple breakpoints will occur. This is a very powerful debugging capability that allows the engineer to monitor signals throughout the various delta time cycles and see when they change. Race conditions are quite easily found with this type of monitoring.

The ability to simulate the specified VHDL design allows for verification of the design through the interaction of the various parts that make up the design. Functional verification, as well as pre-layout and post-layout/routing verification are all supported in the VHSIC HDL. The top-down design methodology also requires verification between different levels of design abstraction. This is also easily supported in VHDL. Using VHDL simulation for verification purposes the ASIC design engineer is assured of functioning silicon after fabrication.

III. VHDL as a Documentation Language.

The VHSIC Hardware Design Language supports multiple design libraries, as well as defining a design in a hierarchical specification. This capability allows the language to be used to document the engineers design as well as verify it. Multiple design libraries are referenced through the use of logical library specifications, which map to design library names which are bound to physical operating system directories. The mapping of logical to physical library names is implementation dependent, and differs from one simulator vendor to another. The definition of a library is done with a library statement, followed by a logical library name as follows:

```
Library YCAD;
```

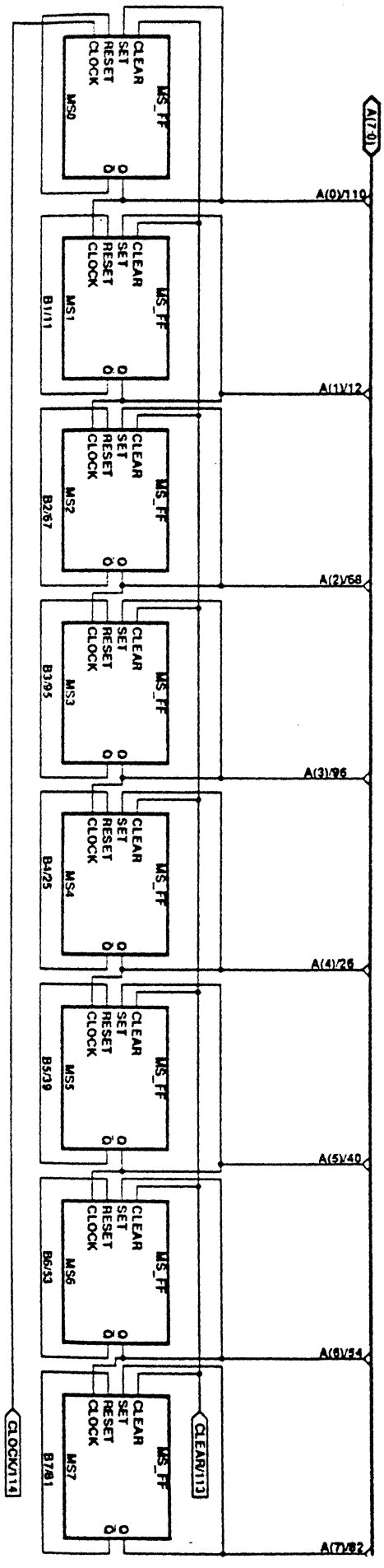
The contents of the library are accessed through a set of scope and visibility rules that when used form a document that explicitly defines what primitives are used from the declared library. The following are several examples of the usage of such rules from the previously defined logical library:

```
Use YCAD.TYPES.ALL;
Use YCAD. COMPONENTS.NOR;
Use YCAD. COMPONENTS.AND;
Use YCAD.COMPONENTS.ALL;
```

The first declaration opens a defined package called TYPES, where the ZYCAD paradigm is defined. This allows the usage of all data types, functions, overloaded operators, and signal resolution functions. The second through fourth declarations open a defined package called COMPONENTS, and specifies either individual components, or all components in the package. These are generic primitives.

A multiple hierarchy design is easily specified using VHDL as a design language, a simulation language, and a documentation language. The next 10 pages detail an 8 bit ripple counter design that is built up from a primitive library that is defined elsewhere. There are three levels of hierarchy, plus a boilerplate testbench which make up the design. Included as part of this paper are the schematic drawings of the counter, which is made up of 8 master-slave flip-flops connected to a common bus. Each MS-FF is made up of two SET-RESET flip-flops, plus additional primitive logic. Each RS-FF is modeled at a different level. The RS-FFS is modeled at the structural level, with the RS-FF modeled at a behavioral level. The RS-FFS symbol has an additional schematic underlying it, while the RS-FF has only VHDL code to describe its' behavior. Except for the RS-FF, the entire design is modeled down to the primitive gate level. All VHDL code was automatically extracted from the schematic except for the primitives which were described in a design library, and the RS-FF which was described

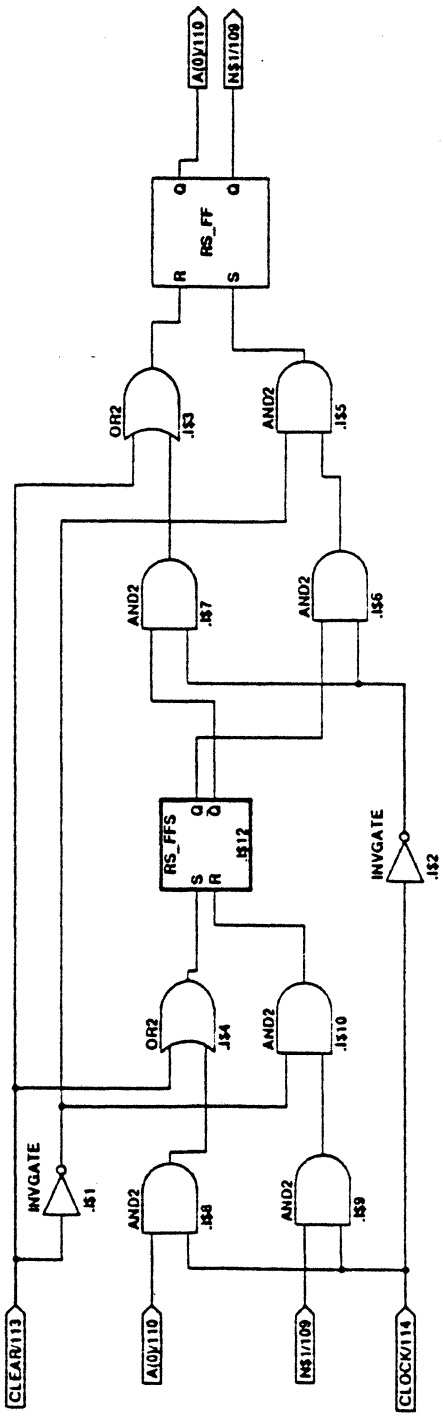
behaviorally. The two vectors necessary to drive this model (Clock and Clear) were provided within the Simulator Command Language of the simulation tool verifying the design. They can easily be moved to the boilerplate testbench to make the design totally portable. The final page shows the input vectors; Clock and Clear, as well as the output from each individual MS-FF. All signals shown in the Logic Analyzer display are scalars, except for the top signal which is the value of all the outputs of the MS flip-flops viewed as an 8 bit vector. The first 2100 NS of this simulation were plotted to verify the increasing non-overlapping count that is the output of a true ripple counter. All work was accomplished using the ZYCAD System VHDL analyzer and simulator.


A[7:0]
A(0)/110
A(1)/12
A(2)/68
A(3)/96
A(4)/26
A(5)/40
A(6)/54
A(7)/82
CLOCK/114
CLEAR/113
MS0
MS1
B1/11
MS2
B2/67
MS3
B3/95
MS4
B4/25
MS5
B5/39
MS6
B6/53
MS7
B7/81
MS_FF
CLEAR
SET
RESET
CLOCK
Q

```
-- VHDL Test Bench Created from ECS Symbol cnt8bus.sym.sym

library  YCAD;
   use  YCAD.types.all;
   use  YCAD.components.all;

entity E is
end E;

Architecture A of E is

   signal     CLEAR : DotX;
   signal     CLOCK : DotX;
   signal         A : BusX (7 downto 0);

   component CNT8BUS
      Port (    CLEAR : In    DotX;
                CLOCK : In    DotX;
                    A : InOut BusX (7 downto 0) );
   end component;

begin
   UUT : CNT8BUS
      Port Map ( CLEAR, CLOCK, A(7 downto 0) );

-- *** Test Bench - User Defined Section ***
   TB : block
   begin
   end block;
-- *** End Test Bench - User Defined Section ***

end A;

configuration CFG_TB_CNT8BUS of E is
   for A
      for UUT : CNT8BUS
         use entity WORK.CNT8BUS(SCHEMATIC);
      end for;

-- *** User Defined Configuration ***
      for TB
      end for;
-- *** End User Defined Configuration ***

   end for;
end CFG_TB_CNT8BUS;
```

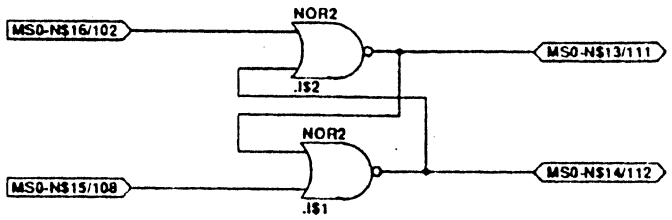
```
-- VHDL Model Created from ECS Schematic cnt8bus.sch --

library  YCAD;
   use  YCAD.types.all;
   use  YCAD.components.all;

entity CNT8BUS is
      Port (    CLEAR : In    DotX;
                CLOCK : In    DotX;
                    A : InOut BusX (7 downto 0) );
end CNT8BUS;

architecture SCHEMATIC of CNT8BUS is

   signal      N_1 : DotX ;
   signal       B1 : DotX ;
   signal       B4 : DotX ;
   signal       B3 : DotX ;
   signal       B7 : DotX ;
   signal       B2 : DotX ;
   signal       B6 : DotX ;
   signal       B5 : DotX ;

   component MS_FF
      Port (    CLEAR : In    DotX;
                  SET : In    DotX;
                RESET : In    DotX;
                CLOCK : In    DotX;
                    Q : Out   DotX;
                  b_Q : Out   DotX );
   end component;

begin

   MS0 : MS_FF
      Port Map ( CLEAR=>CLEAR, SET=>A(0), RESET=>N_1, CLOCK=>CLOCK,
                 Q=>A(0), b_Q=>N_1 );
   MS3 : MS_FF
      Port Map ( CLEAR=>CLEAR, SET=>A(3), RESET=>B3, CLOCK=>A(2),
                 Q=>A(3), b_Q=>B3 );
   MS7 : MS_FF
      Port Map ( CLEAR=>CLEAR, SET=>A(7), RESET=>B7, CLOCK=>A(6),
                 Q=>A(7), b_Q=>B7 );
   MS2 : MS_FF
      Port Map ( CLEAR=>CLEAR, SET=>A(2), RESET=>B2, CLOCK=>A(1),
                 Q=>A(2), b_Q=>B2 );
   MS6 : MS_FF
      Port Map ( CLEAR=>CLEAR, SET=>A(6), RESET=>B6, CLOCK=>A(5),
                 Q=>A(6), b_Q=>B6 );
   MS5 : MS_FF
      Port Map ( CLEAR=>CLEAR, SET=>A(5), RESET=>B5, CLOCK=>A(4),
                 Q=>A(5), b_Q=>B5 );
   MS4 : MS_FF
      Port Map ( CLEAR=>CLEAR, SET=>A(4), RESET=>B4, CLOCK=>A(3),
                 Q=>A(4), b_Q=>B4 );
```

```
   MS1 : MS_FF
      Port Map ( CLEAR=>CLEAR, SET=>A(1), RESET=>B1, CLOCK=>A(0),
                 Q=>A(1), b_Q=>B1 );

end SCHEMATIC;

configuration CFG_CNT8BUS of CNT8BUS is

   for SCHEMATIC
      for MS0, MS3, MS7, MS2, MS6, MS5, MS4, MS1: MS_FF
         use configuration WORK.CFG_MS_FF;

      end for;
   end for;

end CFG_CNT8BUS;
```


A(0)/110
N$1/109
RS_FF
R
S
Q
Q
OR2
.I53
AND2
.I55
AND2
.I57
AND2
.I56
RS_FFS
S
R
Q
Q
.I512
INVGATE
.I52
OR2
.I54
AND2
.I510
INVGATE
.I51
AND2
.I58
AND2
.I59
CLEAR/113
A(0)/110
N$1/109
CLOCK/114

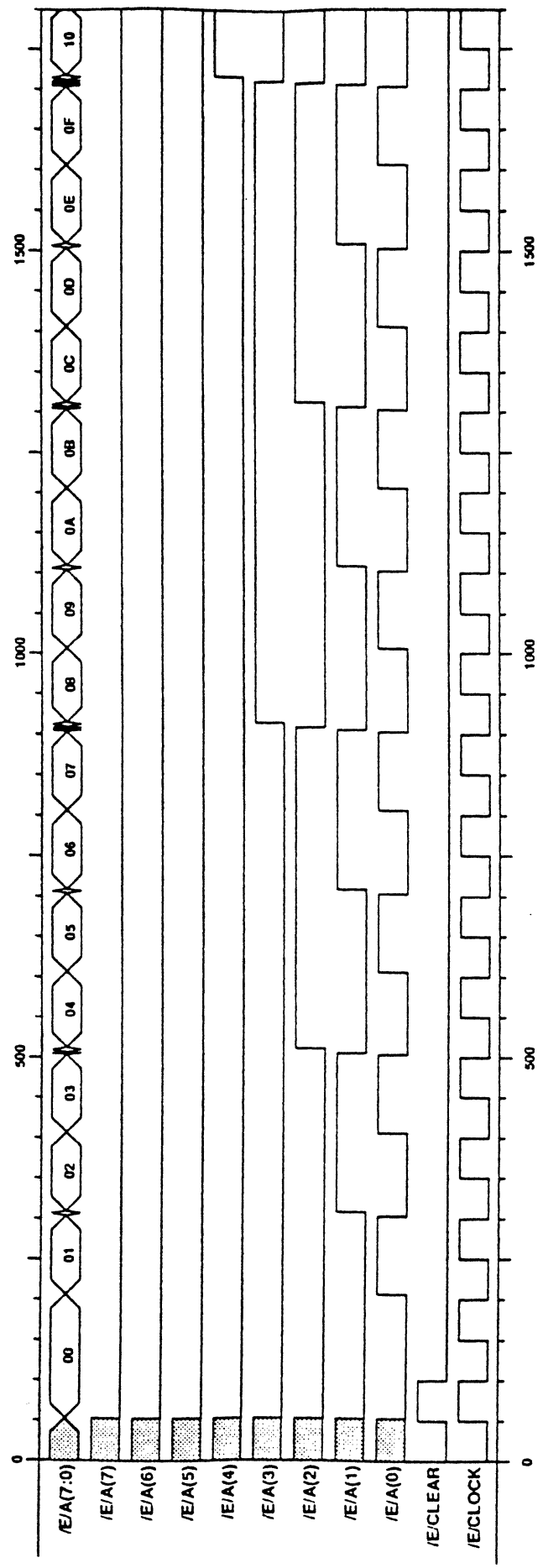
```
-- VHDL Model Created from ECS Schematic ms_ff.sch --

library  YCAD;
   use  YCAD.types.all;
   use  YCAD.components.all;

entity MS_FF is
      Port (   CLEAR : In    DotX;
                 SET : In    DotX;
               RESET : In    DotX;
               CLOCK : In    DotX;
                   Q : Out   DotX;
                 b_Q : Out   DotX );
end MS_FF;

architecture SCHEMATIC of MS_FF is

   signal     N_13 : MVL7 ;
   signal     N_14 : MVL7 ;
   signal     N_15 : MVL7 ;
   signal     N_16 : MVL7 ;
   signal     N_17 : MVL7 ;
   signal     N_18 : MVL7 ;
   signal      N_3 : MVL7 ;
   signal      N_4 : MVL7 ;
   signal      N_8 : MVL7 ;
   signal      N_9 : MVL7 ;
   signal     N_10 : MVL7 ;
   signal     N_12 : MVL7 ;

   component RS_FFS
      Port (       R : In    DotX;
                   S : In    DotX;
                   Q : InOut DotX;
                 b_Q : InOut DotX );
   end component;

   component RS_FF
      Port (       R : In    MVL7;
                   S : In    MVL7;
                 b_Q : Out   MVL7;
                   Q : Out   MVL7 );
   end component;

begin

   I_12 : RS_FFS
      Port Map ( R=>N_15, S=>N_16, Q=>N_13, b_Q=>N_14 );
   I_13 : RS_FF
      Port Map ( R=>N_18, S=>N_17, b_Q=>b_Q, Q=>Q );
   I_10 : ANDGATE
   Generic Map ( N => 2, TLH => 0 NS, THL => 0 NS, STRN => X01 )
      Port Map ( INPUT(1)=>N_8, INPUT(2)=>N_10, OUTPUT=>N_15 );
   I_9 : ANDGATE
   Generic Map ( N => 2, TLH => 0 NS, THL => 0 NS, STRN => X01 )
      Port Map ( INPUT(1)=>RESET, INPUT(2)=>CLOCK, OUTPUT=>N_10 );
```

```
    I_8 : ANDGATE
    Generic Map ( N => 2, TLH => 0 NS, THL => 0 NS, STRN => X01 )
       Port Map ( INPUT(1)=>SET, INPUT(2)=>CLOCK, OUTPUT=>N_9 );
    I_7 : ANDGATE
    Generic Map ( N => 2, TLH => 0 NS, THL => 0 NS, STRN => X01 )
       Port Map ( INPUT(1)=>N_14, INPUT(2)=>N_4, OUTPUT=>N_12 );
    I_6 : ANDGATE
    Generic Map ( N => 2, TLH => 0 NS, THL => 0 NS, STRN => X01 )
       Port Map ( INPUT(1)=>N_13, INPUT(2)=>N_4, OUTPUT=>N_3 );
    I_5 : ANDGATE


    Generic Map ( N => 2, TLH => 0 NS, THL => 0 NS, STRN => X01 )
       Port Map ( INPUT(1)=>N_8, INPUT(2)=>N_3, OUTPUT=>N_17 );
    I_4 : ORGATE
    Generic Map ( N => 2, TLH => 0 NS, THL => 0 NS, STRN => X01 )
       Port Map ( INPUT(1)=>CLEAR, INPUT(2)=>N_9, OUTPUT=>N_16 );
    I_3 : ORGATE
    Generic Map ( N => 2, TLH => 0 NS, THL => 0 NS, STRN => X01 )
       Port Map ( INPUT(1)=>CLEAR, INPUT(2)=>N_12, OUTPUT=>N_18 );
    I_2 : INVGATE
    Generic Map ( TLH => 0 NS, THL => 0 NS, STRN => X01 )
       Port Map ( INPUT=>CLOCK, OUTPUT=>N_4 );
    I_1 : INVGATE
    Generic Map ( TLH => 0 NS, THL => 0 NS, STRN => X01 )
       Port Map ( INPUT=>CLEAR, OUTPUT=>N_8 );

end SCHEMATIC;

configuration CFG_MS_FF of MS_FF is

   for SCHEMATIC
      for I_12: RS_FFS
         use entity WORK.RS_FFS(SCHEMATIC);
      end for;
      for I_13: RS_FF
         use entity WORK.RS_FF(BEHAVIORAL);
      end for;
      for I_10, I_9, I_8, I_7, I_6, I_5: ANDGATE
         use entity  YCAD.ANDGATE(BI);
      end for;
      for I_4, I_3: ORGATE
         use entity  YCAD.ORGATE(BI);
      end for;
      for I_2, I_1: INVGATE
         use entity  YCAD.INVGATE(BI);
      end for;
   end for;

end CFG_MS_FF;
```




```
-- VHDL Model Created from ECS Schematic rs_ffs.sch --

library  YCAD;
   use  YCAD.types.all;
   use  YCAD.components.all;

entity RS_FFS is
      Port (        R : In    DotX;
                    S : In    DotX;
                    Q : InOut DotX;
                  b_Q : InOut DotX );
end RS_FFS;

architecture SCHEMATIC of RS_FFS is


begin

   I_1 : NORGATE
   Generic Map ( N => 2, TLH => 0 NS, THL => 0 NS, STRN => X01 )
      Port Map ( INPUT(2)=>Q, INPUT(1)=>R, OUTPUT=>b_Q );
   I_2 : NORGATE
   Generic Map ( N => 2, TLH => 0 NS, THL => 0 NS, STRN => X01 )
      Port Map ( INPUT(2)=>S, INPUT(1)=>b_Q, OUTPUT=>Q );

end SCHEMATIC;

configuration CFG_RS_FFS of RS_FFS is

   for SCHEMATIC
      for I_1, I_2: NORGATE
         use entity  YCAD.NORGATE(BI);
      end for;
   end for;

end CFG_RS_FFS;
```

```
-- VHDL Model Created from ECS Symbol rs_ff.sym -

library  YCAD;
   use  YCAD.types.all;
   use  YCAD.components.all;

entity RS_FF is
      Port (        R : In    MVL7;
                    S : In    MVL7;
                  b_Q : Out   MVL7;
                    Q : Out   MVL7 );


end RS_FF;

architecture BEHAVIORAL of RS_FF is
        begin
              q   <= r nor b_q after 3 ns;
              b_q <= s nor q after 3 ns;
end BEHAVIORAL;

configuration CFG_RS_FF of RS_FF is
     for BEHAVIORAL
     end for;
end CFG_RS_FF;
```



August 20, 1990

A VHDL Design Environment

Alan R. Martello
Steven P. Levitan

Department of Electrical Engineering
University of Pittsburgh
Pittsburgh, PA 15261

1 Introduction

Hardware Description Languages (HDLs) provide a way to textually represent physical electronic systems [1,2]. They are used for description, documentation, and communication of digital electronic designs. More recently, they have been used for design verification, simulation, and synthesis. One language, the V(HSIC) hardware description language (VHDL) is now an IEEE standard [3]. [1]

A joint project between the University of Pittsburgh and the Pennsylvania State University has resulted in a set of software tools to help researchers and educators investigate issues in the synthesis of VLSI systems from VHDL descriptions. The tools have been developed and used extensively for the last two years at both Universities in our digital design, computer organization, and VLSI design courses. In addition the tools have been used as the basis for several ongoing research projects in VLSI architecture design and VLSI CAD.

We have chosen VHDL as the front end language in our design and synthesis system (called Keystone) for several reasons: it is a well documented standard, it is gaining popular acceptance, it supports both abstraction hierarchy and design hierarchy (with its structural and procedural constructs), and it is not tied to any one vendor's design system. Further, having the tools accept a textual representation of the design makes them more portable, running on mainframes as well as graphics workstations. This level of portability built into our VHDL tools has been welcomed by other universities as well as companies with similar research interests and we continue to distribute our VHDL tools for research and educational purposes.[2]

At the University of Pittsburgh, VHDL research has gone on since 1987. Mears [7] implemented a VHDL version 1076/B compiler and simulator. The compiler was based on work by Frauenfelder [8] on a language analyzer for an earlier version of VHDL. Frauenfelder's basic design which Mears built on was in turn based on the sample compiler described in [9]. The event driven simulator Mears implemented was capable of simulating a subset of the compiled VHDL code. This simulator was based on the RSIM work performed by Chris Terman at MIT for switch level simulation of transistors [10].

The VHDL work which Mears performed demonstrated the usefulness and established the technological feasibility of VHDL as a research tool in an academic environment. Since then we have built on Mears' work by refining those VHDL tools to produce an externally dis-

[1] This report is not meant as an introduction to VHDL; that is beyond the scope of this paper. There are a number of good books available for a description and examples of VHDL (such as [4–6]). For the complete VHDL specification, refer to the current IEEE standard document [3]. The emphasis here is to provide a brief overview of the VHDL design system as implemented at the University of Pittsburgh.

[2] Additional information regarding the VHDL tools may be obtained by sending electronic mail to vhdl@ee.pitt.edu or a written request to Dr. Steven Levitan, Dept. of Elect. Eng., 348 Benedum Hall, Univ. of Pittsburgh, Pittsburgh, PA 15261.

tributable software package for classroom and research use. A secondary goal was extending the implementation of the VHDL description and simulation constructs to meet the needs of both educators and researchers interested in synthesis [11]. This report provides an overview of the VHDL compiler and simulator.

The remainder of this discussion of the VHDL design project is organized as follows. First we discuss the concept of the VHDL design hierarchy and describe how the data structures used to implement this hierarchy are defined. Next, the method which the VHDL code is parsed and placed in the internal database is presented. This includes a general overview of the concurrent and sequential constructs which are supported. Finally, the process of creating output of the compiler from the internal compiler database is described, and an overview of the simulator is given. We must remind the reader that we implemented and are describing a *subset* of VHDL. Many of the constructs which are not supported are not discussed.

2 VHDL Design Hierarchy and Database

The basic structure within a VHDL design is the *design entity.* A single design consists of (potentially) many design entities; each entity describes a single portion of the design. Each entity has a single *entity declaration* which describes the inputs and outputs of the entity. The entity declaration does not describe how the design entity functions, it simply defines the inputs and outputs, providing an external view of the entity. Figure 1 shows a VHDL description for an 8-bit barrel shifter. The lines marked with 1 are the entity declaration.

```
    1   2   entity BARREL is
    1   2         port (data_in:   in bit_vector(7 downto 0);
    1   2               shift:     in bit_vector(2 downto 0);
    1   2               data_out:  out bit_vector(7 downto 0)
    1   2         );
    1   2   end BARREL;

        2   architecture logic of BARREL is
3       2         signal buffer_a:  bit_vector(7 downto 0);
3       2         signal buffer_b:  bit_vector(7 downto 0);
        2   begin
4       2         -- stage one, shift one bit if needed
4       2         buffer_a(7 downto 0) <=
4       2               data_in(6 downto 0) & data_in(7) when shift(0)
4       2               else data_in(7 downto 0);
4       2
4       2         -- stage two, shift two bits if needed
4       2         buffer_b(7 downto 0) <=
4       2               buffer_a(5 downto 0) & buffer_a(7 downto 6)
4       2               when shift(1) else buffer_a(7 downto 0);
4       2
4       2         -- stage three, shift four bits if needed
4       2         data_out(7 downto 0) <=
4       2               buffer_b(3 downto 0) & buffer_b(7 downto 4)
4       2               when shift(2) else buffer_b(7 downto 0);
        2   end logic;
```

Figure 1: VHDL Description of 8-Bit Tree Structured Barrel Shifter

Each design entity has at least one, but perhaps more, *architectures* associated with the entity declaration. Each architecture provides one possible way of describing the functionality of the design entity or one possible implementation of the design entity. Design entities may be hierarchically nested. This means that if one design entity is used in more than one part of the design, then it only needs to be defined once but may be referenced (or instantiated) multiple times. VHDL gives us the flexibility to describe designs while maintaining any type of hierarchical partitioning or nesting. The architecture in Figure 1 is designated by 2.

Architectures describe how a particular implementation of a design entity should function. Architectures consist of two parts: the *architecture declarations* (3 in Figure 1) and the *architecture body* (4 in Figure 1). The architecture declaration describes the various items used within the architecture body. These items include *signals* (which can be considered the same as wires) and references to other design entities which are nested inside this architecture.

Within an architecture body may appear two types of statements: concurrent statements and sequential statements. These statements are used to describe the functionality of the architecture. VHDL's concurrent and sequential statements are an attempt to describe circuits which exhibit parallel behavior and serial behavior respectively. The basic data construct within both sequential and concurrent code is the assignment construct.

3 VHDL Code → Internal Database

In the system, to internally manipulate the VHDL design, an internal database format was defined which modeled the VHDL design hierarchy described above. Although the VHDL compiler parses the entire VHDL grammar as defined in [12], it does not build the entire language into its internal database. Only those items described below are built into the internal VHDL representation.

Figure 2 shows the uppermost level of the internal VHDL database. The entire design description is composed of a list of entities. Each entity contains the information which defines its inputs and outputs. Each entity has one or more architectures which describe possible implementations of the entity. If an entity has multiple architectures (or representations) then these are chained in a list which is linked to the entity.

Within each architecture are blocks which contain the actual implementation of the architecture. Each architecture contains at least one top-level block (shown in Figure 3 as Block a. This block is a concurrent block. This block may contain other blocks nested within it (for example, Block aa and ab) and any block may contain other nested blocks (such as Block aaa and aab. This block structured nesting capability is similar to programming languages such as Pascal.

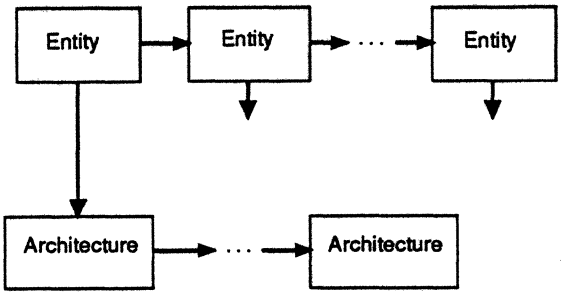


Figure 2: VHDL Compiler Entity and Architecture Structure

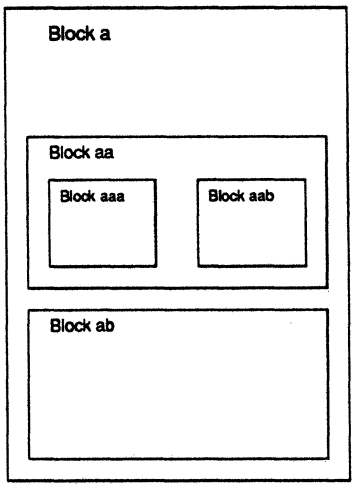


Figure 3: VHDL Compiler Block hierarchy

Each block (other than the top-level block in the architecture) is either a *process block* or a *concurrent block*. A process block contains process statements which by definition are "executed" sequentially. A concurrent block contains concurrent statements which "execute" in parallel. Concurrent blocks may contain other nested blocks (either process or concurrent) but process blocks may not contain additional hierarchy. For this reason, the top-level block in the architecture is a concurrent block.

Blocks contain two basic parts: a declaration part and a statement part. The declaration part contains definitions of local data items. A *data item* could be a signal, a variable, a constant, or a variety of other data types, depending on the type of block as defined in the VHDL Language Reference Manual [12]. Scoping rules for data items referenced in the statement part of a block are the same as in other block structured languages. If a reference to a data item within a block appears ambiguous due to multiple declarations of the same item within the block hierarchy, the reference is resolved statically by using the most recent lexically declared version of the data item.

Since the compiler performs a single pass over all input files in the process of generating output, no forward declarations are permitted. Any item (such as an entity or entity/-architecture pair) must be defined prior to being referenced by some other part of the database since support of libraries or *use/with* clauses are not implemented.

Within the statement part of a block may appear a variety of items depending of the type of block. In concurrent blocks, the following items are supported within the statement part:

- nested process blocks,
- nested concurrent blocks,
- component instantiations, and
- assignment statements.

Process blocks only support sequential control and assignment statements; no hierarchy of components or blocks are permitted within process blocks. Inside every block in the database is a list of statements which appear within the block. These statements define the functionality of the block and ultimately the entire design.

3.1 Parsing VHDL

The part of the compiler which parses the VHDL input file is automatically created from an input grammar utilizing the parser generator *bison*[13]. Parse trees for each VHDL assignment statement are created and stored in the internal database. Each node of the parse tree contains an operation to perform and pointers to the operands. These operand pointers may reference other operation nodes. This allows for arbitrarily complex expressions to be represented by the parse trees.

The primitive operations supported for both concurrent and sequential blocks are shown in Table 1. The operations common to both concurrent and sequential statements are discussed in the next section and the operations unique to concurrent and sequential statements are covered in Sections 3.3 and 3.4 respectively.

3.2 Concurrent and Sequential Operations

The Group I operations of Table 1 are common to both sequential and concurrent statements. The operations *and, or, nand, nor, xor,* and *not* are the standard logic operations. The operations *and, or,* and *xor* are multiple input single output operations; *not* is a single input operation; and *nand* and *nor* are two input operations. The *width* (or bit size) of all inputs to these operations should be identical and must match the width of the output.

The *null* operation is a single input operation and is used to represent instructions such as

Operation	Concurrent	Sequential	Group
null	√	√	I
and	√	√	
or	√	√	
nand	√	√	
nor	√	√	
xor	√	√	
not	√	√	
concat	√	√	
eq	√	√	
ne	√	√	
cond	√		II
select	√		
plus		√	III
minus		√	
lt		√	
le		√	
gt		√	
ge		√	

Table 1: Primitive Internal Operations Supported

`A <= B`. The *null* operation is also used during parsing to represent and to insert expression evaluation precedence into an expression. The input and output widths of the operands for the *null* operation should be identical.

The *eq* and *ne* operations are used to express equality and inequality operations. These are two input operations whose operands must have the same size. The result of the operation is a single bit which indicates if the operands are identical or different.

The *concat* operation performs concatenation of all its input operands into a single bit string. Each operand may be any size and the result of the operation is a bit string whose size is the summation of the sizes of all the operands.

3.3 Concurrent Blocks

Within concurrent blocks may appear component instantiations, concurrent statements, nested concurrent blocks, and process blocks. Component instantiations are used to define that a *copy* of an entity implemented by a specified architecture is present within a concurrent block. The component instantiation behaves similar to a macro definition in function (versus a procedure call) since it creates a copy of the entity and architecture within the hierarchy when the database output is generated.

When a component is instantiated, the following checks are performed.

- Any constants which are in the port specification of the instantiation must have a signal direction *in* within the instantiated entity.
- Any signals which are in the port specification of the instantiation and have a signal direction *in* must map to ports which also have a signal direction *in* within the instantiated entity.

In addition to these two instantiation checks, a check is made on each assignment statement to verify that the left-hand side of the assignment statement is not a signal which has a signal direction *in*. These three checks combined allow constants to be passed into component instantiations freely and not be corrupted within any arbitrary hierarchy.

In the database, the entity / architecture pair which refers to a component instantiation is indirectly indicated by the component instantiation statement; it is not explicitly copied. The names to use for the port mapping are stored within the instantiation for use during the database output generation phase of compilation.

The Group II operations of Table 1 are used only in concurrent statements. The operation *cond* is used to represent a conditional signal assignment as in `a <= b when c else d`. Three operands are required for this operation. The first operand (`b` in our example) is the value to be assigned when the second operand (`c`) is true. The final operand (`d`) is the value to be assigned when `c` is false. The sizes of `a`, `b`, and `d` must be the same and the size of `c` must be one (i.e. a single bit). All of `b`, `c`, and `d` may be an arbitrary expression.

The operation *select* signifies a selected signal assignment and is used to choose a single value for an assignment. The VHDL syntax for the instruction is:

$$\begin{array}{lllll} \texttt{with } b \texttt{ select } c \texttt{ <=} & x_1 & \texttt{when} & y_1, \\ & x_2 & \texttt{when} & y_2, \\ & & \vdots & \\ & x_n & \texttt{when} & y_n; \end{array}$$

This statement operates by comparing b first with y_1, then y_2, etc. and stopping when the first match is found. When this match is found, the corresponding value of x is assigned to c.

To implement this construct, a four input, single output operation is represented in the parse tree. The first operand is x, the second operand is b, the third operand points to the output of a "nested" *select* expression which represents the succeeding `when` clause, and the fourth operand is y. Because the third operand can point to another *select* operation, an arbitrary VHDL *select* instruction with n `when` clauses can be represented in the parse tree with n select operations. The sizes of the first and third operands of a *select* operation are the same size as the output; the sizes of the second and fourth operands must be identical since they are compared for equality.

The parsing of a concurrent assignment statement has four phases. The first phase is the building of the parse tree for the expression in the internal database. The second phase is a check that all operand sizes are correct depending on the operations being performed. The third phase consists of checking that the left-hand side expression of the assignment statement is not an entity input port since we never allow input ports to be modified. The final phase is the optimization of the parse tree by removing *null gates.*

During concurrent statement parsing, many *null* gates are added to disambiguate the expression and to correctly capture delay expressions within the concurrent signal assignment. After the entire statement has been parsed, some of these gates may be superfluous and can be removed. This optimization phase is performed to remove the superfluous gates.

The nesting of concurrent blocks provides for modularity within a block. Everything which may appear in the uppermost block of an architecture may also appear in any nested concurrent blocks. Static scoping rules apply to signals which are declared within nested blocks.

VHDL also allows nested concurrent blocks to have *guards* associated with them. A *guard* is an enabling signal which may be generated by an arbitrary VHDL concurrent expression. The *guard* is then used to selectively enable and disable concurrent assignment statements within the block which are *guarded.* This construct is useful for modeling buffers or entire circuit partitions which are selectively enabled and disabled by simple signal expressions.

3.4 Process Blocks

Process blocks are used within VHDL to express sequential execution. Process blocks which are encountered are stored within the database and are also translated to *C* language code for simulation. During simulation, the complex sequential code executes at native machine speeds since it is executed directly and is not interpreted. Two types of translations take place in mapping the sequential code to *C* code: translation of control constructs and translation of data constructs.

The sequential control constructs supported are similar to ones found in most high level programming languages. These control constructs may be arbitrarily nested to allow for complex sequential control description. When encountered, these sequential constructs are translated to *C* code. The translations performed are shown in Table 2.

The Group III operations of Table 1 are mathematical operations and may only be used in sequential statements. Since the sequential constructs are translated to *C* language statements, these operations are dependent on the lower-level *C* representation for their functionality. The Group III operations of *plus* and *minus* signify standard two's complement addition and subtraction. Both operations require two operands and no checking of sizes of the operands is

performed. Similarly the *lt, le, gt,* and *ge* operands perform the respective two's complement comparison operation.

All sequential data constructs are assumed to consist of a collection of bits which is not greater than the maximum size of a long integer for the host machine's *C* compiler. This size is 32 bits for VAX and SUN systems. Each data construct (*integer*, *bit vector*, *variable*, or *bit*) is mapped into a single long integer.

The advantage of utilizing this mapping is that mathematical operations have a predefined functionality on the host machine for long integers and operations such as subtraction or arithmetic comparisons are not ambiguous. A disadvantage of this approach is the limitation imposed by the length of a long integer on the host machine. This limitation effects the concurrent portion as well as the sequential portion of the compiler; thus all data objects within the VHDL design system are currently limited to a maximum length of 32 bits.

4 Generating Compiled VHDL Output

Once the input VHDL is successfully parsed and the entire database built in memory, output is generated. The output generated needs to be referenced from some uppermost point called the "top-level". This top-level of the hierarchy consists of both an entity and an architecture specification. Because the compiler performs its work in one pass, the internal database is guaranteed to have a valid hierarchy rooted at every entity / architecture pair within the database. The output generated consists of two versions of the internal database: a hierarchical version and a flattened version.

The hierarchical database maintains much of the look of the original VHDL but has the following additions:

- all expressions are fully parenthesized,
- all concurrent expressions have undergone type and size checking, and
- all signals and variables used appear in the declarations.

This portion of the database maintains the VHDL hierarchy and is useful for processing by tools which manipulate and optimize high-level or hierarchical constructs; examples of this usage of the hierarchical database are given in [11].

The hierarchical output is generated by scanning the entire database, one entity at a time, and writing all information associated with each node in the hierarchy to the output file. The top-level node is annotated in the hierarchical output and is used to limit the amount of the internal database written; only that part of the database which is referenced within the hierarchy rooted at the specified "top-level" node is written to the hierarchical database.

For example, if a design of an 8-bit ripple carry adder consisted of 8 full adders and each full adder was further described by two half adders, the design database would appear as shown in Figure 4. The hierarchical output of the design contains three major entries: one for the entire adder (top-level node), one for the full adder, and one for the half adder. The full adder is composed of two half adders and a single *or* gate. The half adder is composed of three *and* gates, two *not* gates, and one *or* gate. Each entity has multiple links within the hierarchical database as shown in Figure 4; thus ten links are present within the hierarchical representation of the adder.

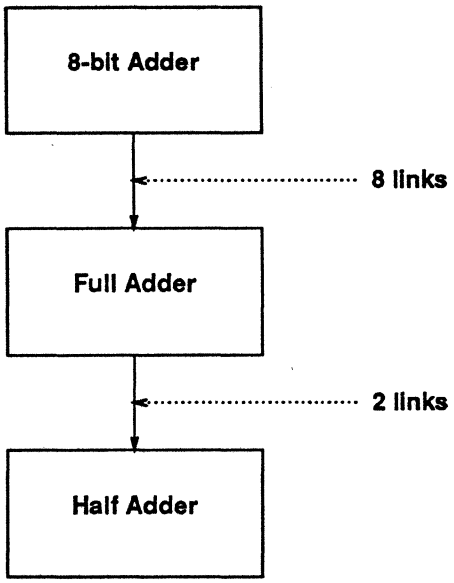


Figure 4: 8-bit Adder Hierarchy

The flattened database contains the information in the internal database in a totally expanded format. The entire hierarchy is flattened down to the operation level (also referred to at this point as the gate level). This means that the flattened database assumes operations are primitive elements. For the 8-bit adder example, the flattened representation is composed of 104 gate equations which are broken down as follows:

$$\left(\frac{\#\ \text{gates}}{\text{half adder}} \times \frac{\#\ \text{half adders}}{\text{full adder}} + \frac{1\ \textit{or}\ \text{gate}}{\text{full adder}} \right) \times \#\ \textit{full adders} = \#\ \textit{gates}$$

$$\left(\quad 6 \quad \times \quad 2 \quad + \quad 1 \quad \right) \times \quad 8 \quad = \quad 104\ \textit{gates}$$

The operation of flattening the database consists of performing a tree traversal of the entire database starting at the node specified as the top-level. The database is traversed in a depth-first manner and a gate is generated each time a leaf node in the tree is encountered.

Each operation (or gate) equation within the flattened database contains the following information:

- a unique gate name;

- the type of gate/operation;
- the delay (if any) associated with the operation;
- the type of delay (if any) associated with the operation;
- the number of inputs;
- a list of inputs;
- the number of outputs;
- the list of outputs.

In addition to removing hierarchy, the flattened database represents all multi-bit signals such as bit vectors as single data bits. Because the interconnection within the netlist is specified by name, each node within the net is labeled. This information in the flattened database was designed to be used as the input to the simulator discussed in the next section. Although specific decisions were made regarding the flattened format to accommodate our simulator, the flattened format is in a general netlist form suitable for other applications and has been used as input for automatic schematic generation [14].

5 Simulating VHDL

The VHDL simulator is an event-driven interactive simulator. It has a user friendly command line interface which supports wildcarding, command name aliases, macro expansion, and command files.

The simulator's internal structure supports two main data types which are read from the flattened database description: *nodes* and *objects*. *Nodes* are the data items represented within the simulator. *Objects* are the gates or operations represented within the simulator.

For simulation, the process blocks which have been translated to sequential code are placed in a file with a simulator specific header and footer. The header and footer allow the translated sequential code to have read and write access to the nodes. The translated process blocks are compiled and linked with a simulator library to form a VHDL model specific simulator. Once this custom simulator is created, the process blocks are not (in general) treated specially within the simulator but are simply viewed as large, multi-input, multi-output "gates" or "operations."

Since the simulator is an event driven simulator, it maintains a list of events sorted by the time at which the events should occur. The events maintained are changes of node values within the simulator. When the node associated with an event has its value updated as specified by an event and the event is removed from the event queue, and the event is said to have *fired*.

The simulator has three main modes of operation:

Initialization –	read in the netlist and initialize the nodes,
Waiting for Command –	at the command line waiting for a command from the user, and
Firing Events –	updating nodes from events on the event list which are supposed to occur up to the current time.

After the Initialization state, the simulator goes into a Wait-for-Command and Fire-Event loop. The simulator transitions from the Wait-for-Command state to the Fire-Event state when a command is issued which modifies the current time. The simulator remains in the Fire-Event state until all events which should fire up to the current time have fired or until the user interrupts event firing by typing an interrupt key; either of these conditions returns the simulator to the Wait-for-Command state.

The updating and evaluation of node values occurs in a traditional two pass method. First, new values are assigned to all nodes which should fire at time $t = now$. Next, all gates which these nodes effect are evaluated and any changes to their outputs are posted on the event queue. This update/evaluate loop continues for $t = now$ until there are no more events on the event queue to be evaluated at $t = now$. When there are no events scheduled to occur at $t = now$, time steps forward to the time for the next scheduled event. An example log file from the barrel shifter presented earlier is shown below. Our collaborators at Penn State have successfully used the simulator for their design of a signal processing architecture. In this design, they simulated a 150,000 transistor model of an ALU taking less than 3 simulator seconds per ALU clock cycle [15].

6 VHDL Design System Summary

This report has provided an introduction to the VHDL Design System developed at the University of Pittsburgh as part of the Keystone Design Environment being developed in cooperation with the Pennsylvania State University. The development of the VHDL system is ongoing and has served as the basis for two additional research projects. The first project was fault simulation and automatic test pattern generation in VHDL [16]. This work permitted injection, simulation and test vector generation for both logical stuck-at and gate delay faults.

The second project involves extending the VHDL compiler and simulator to accept a multi-valued logic algebra seamlessly into our VHDL design and synthesis semantics. The proposed multi-valued logic algebra can accurately model many characteristics of MOS and CMOS circuits including: attenuation, bi-directional pass transistors, ratioed and complementary logic, dynamic and static charge storage, busses, physical failures, delay and stuck-at faults.

```
| -->
| --> define the vector to step through
| -->
uvec shift_0 01010101 shift_1 00110011 shift_2 00001111
| -->  display the vector
uvec
|  user vector list:
|     shift_2  -  00001111
|     shift_1  -  00110011
|     shift_0  -  01010101
| -->
| --> recall the input to the shifter
| -->
node data_in_*
|  data_in_0 - 0
|  data_in_1 - 1
|  data_in_2 - 1
|  data_in_3 - 1
|  data_in_4 - 1
|  data_in_5 - 1
|  data_in_6 - 1
|  data_in_7 - 1
| -->
| --> run the barrel shifter through all 8 shift combinations
| -->
runvec
|  data_out_7 = 11111110
|  data_out_6 = 11111101
|  data_out_5 = 11111011
|  data_out_4 = 11110111
|  data_out_3 = 11101111
|  data_out_2 = 11011111
|  data_out_1 = 10111111
|  data_out_0 = 01111111
|  shift_2 = 00001111
|  shift_1 = 00110011
|  shift_0 = 01010101
```

Figure 5: Partial Simulation Log from 8-Bit Tree Structured Barrel Shifter

The modified simulator will be able to handle designs which are partitioned into abstract function blocks, gates or transistors containing timing information. The CMOS layout synthesized (with the Keystone tools) from this description will function in a manner consistent with the high-level simulation.

The Keystone Design Environment continues to evolve and with it, the VHDL Design System presented here. Over the past two years, the system has proven to be easily extensible and robust. The VHDL Design System continues to be the primary specification and design language in our project for describing designs at a high-level, testing these high-level designs with the simulator, and synthesizing CMOS layout from these high-level specifications.

VHDL Sequential Construct	*C* Construct

if *expression* **then**
sequential-statements
[**elsif** *expression* **then**
sequential-statements]*
[**else**
sequential-statements]
end if ;
	if (*expression*) {
	translated-sequential-statements
	[} **else if** (*expression*) {
	translated-sequential-statements]*
	[} **else** {
	translated-sequential-statements]
	}

case *expression* **is**
when *choices* =>
sequential-statements
[**when** *choices* =>
sequential-statements]*
end case ;
	switch (*expression*) {
	case $choice_1$: **case** $choice_2$: ...
	translated-sequential-statements
	break;
	[**case** $choice_i$: **case** $choice_{i+1}$: ...
	translated-sequential-statements
	break;]*
	}

loop
sequential-statements
end loop ;
	for (;;) {
	translated-sequential-statements
	}

while *expression* **loop**
sequential-statements
end loop ;
	while (*expression*) {
	translated-sequential-statements
	}

for *iden* **in** *range* **loop**
sequential-statements
end loop ;
	for (*iden* = *start-range* ;
	iden comparison end-range ;
	iden inc/dec) {
	translated-sequential-statements
	}

exit [**when** *expression*];	[**if** (*expression*)] **break ;**
next [**when** *expression*];	[**if** (*expression*)] **continue ;**
null ;	;

Table 2: Translations Performed from VHDL Sequential Statements to *C* Statements

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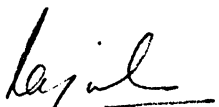
ICCAD-90

ICCAD-1990 was held at Santa Clara Convention Center from November 11 through November 15. There were three days of paper presentations and one day for eight tutorials.

I found the sessions on high-level synthesis, scheduling and allocation, and datapath synthesis very helpful to my research activities. Multi-chip partitioning problem has attracted several researchers and we saw a paper in this area. In the session on scheduling and allocation we saw graph theoretic and integer linear programming approaches for optimizing scheduling and allocation problems encountered in high-level synthesis. The datapath synthesis session had good presentations. A tool which considers low-level aspects of the design such as wiring to upgrade the quality of solutions naively obtained from high-level synthesis tools was described. A method to automatically synthesize a bus-driven architecture was described in another talk in the same session.

The panel discussion was very interesting. The topic of the panel session was "Plateaus and Dead-Ends in CAD" with testing and circuit simulation being debated as having reached a plateau and high-level synthesis being a dead-end. The debates in testing and circuit simulation brought into light some problems currently faced by the industries. Parallel algorithms and hardware accelerators for circuit simulation were emphasized. The outcome of the debate on high-level synthesis was that high-level synthesis is indeed a viable option and needs to be explored.

The conference, as in the past, was very well managed. I would like to take this opportunity to thank you and the executive committee of SIGDA for giving me the opportunity to attend the conference and to be kept upto date in the field of Design Automation.



Rajiv Jain

The 1990 ICCAD was held in Santa Clara, California, from November 11 to November 15. With the support from SIGDA I was able to attend the conference. This was my first attendance to ICCAD. I would like to take this opportunity to share the experiences with other SIGDA members.

The conference had 36 sessions with 122 papers presented. Because my primary interest is in circuit simulations, I attended most of the simulation sessions.

The paper presented by Peter Feldmann from CMU in *Accurate and Efficient Evaluation of Circuit Yield and Yield Gradients* introduced an accurate estimation method of yield and yield gradient. Instead of using conventional parametric space and performance space, disturbance space is used to characterize the process fluctuation. IC parameter's variation due to fabrication process is now represented as a function of the disturbance variables and parameters' nominal values. Yield optimization problem based on gradient method using this disturbance space becomes more efficient and accurate.

In this year's conference, it seems that the mixed-mode simulation is becoming increasingly important. As today's circuit size is getting larger and larger, efficient CAD approaches turn out to be essential. Y.C.Ju from University of Illinois presented a paper in *Mixed-Mode Incremental simulation.* A modified incremental-in-space algorithm is developed for fast circuit simulation. The boundary of the influence of a design change is dynamically determined during the incremental simulation. They also presented a concurrent fault simulation algorithm based on the mixed-mode technique.

The panel section, *Plateaus and Dead Ends in CAD*, was very helpful. It provided a wide-scope review of today's CAD development and the bottlenecks.

In summary, this year's ICCAD was a success, researchers from all over the world got together and exchanged their experiences. Thank again to SIGDA for providing me the trip grant that made my attendance possible.

Sincerely,

Tzu-wen Yao

Tzu-wen Jack Yao
SIGDA Student member.

A travel grant from SIGDA made it possible for me to attend ICCAD-90. My research interest is in High-Level Synthesis and I attended all the sessions related to synthesis. I had the opportunity to see some excellent contributions made by researchers from all over the world.

The first paper in the High-Level synthesis sessions presented an algorithm for component synthesis from functional descriptions. This approach involved recognizing functions in the control/data flow graph and mapping them on to library-specific function modules. Component mapping is formulated as a clique partitioning problem and optimally solved using branch-and-bound strategy. The second paper described pipelined synthesis with multi-cycle operations. The author showed a polynomial time solution for solving the problem. Next a paper was presented on partitioning a functional model using the Kernighan-Lin algorithm as well as the Simulated Annealing algorithm. This presentation demonstrated the importance of partitioning on the final design.

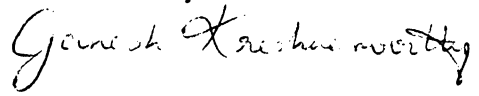
The first paper in the Scheduling and Allocation session described the application of two new kinds of graphs namely the Chordal graphs and Comparability graphs in High-Level synthesis. Many synthesis sub-tasks are formulated as clique partitioning problem which is NP complete for general graphs. The special nature of Chordal and Comparability graphs makes it easier to find cliques and thus speed up the heuristics that require finding and partitioning cliques. The next paper described an Integer-Linear programming technique to solve scheduling and allocation simultaneously. The last paper in this session presented by John Nestor (of which I was co-author) introduced a new representation for synthesis. The new representation allows scheduling freedoms in individual operators to by explored efficiently in a Simulated Annealing framework. Techniques to handle timing constraints, conditional, and subroutine call were presented.

The first paper in the Data Path synthesis sessions presented techniques to feed low level information extracted from floorplanning to guide higher level tasks of scheduling and allocation. This research recognizes the need to incorporate estimates from lower levels of design when proceeding in a top-down fashion. The second paper addressed bussing strategies to design a compact target architecture. The final presentation in this session described a method to improve allocation by successively reallocating parts of the hardware using heuristic methods.

I found several presentations in Logic synthesis and testing to be an interesting learning experience. The panel sessions helped understand where CAD research needs focus. I was glad to learn that much to my expectations High-Level Synthesis is active and alive. During the course of this trip, I had the opportunity to meet professional in the CAD community both from industry and academia with whom I could exchange ideas. I witnessed the state of the art tools for synthesis and simulation created by various CAD houses in the industry exhibit suites.

Finally, I would like to thank SIGDA for providing me the financial support to make this trip possible - a valuable experience.

Sincerely,



Ganesh Krishnamoorthy

With the help of the SIGDA travel grant, I was able to attend the International Conference on Computer-Aided Design in San Jose, California. The conference provided a good opportunity to interact with other people working in CAD and see state-of-art design tools and methodologies offered by industrial vendors.

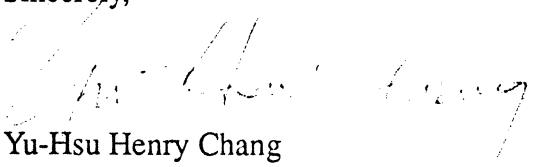
My main interest is in the development of mixed-mode simulation algorithm. Therefore, I was attracted by almost every session in circuit simulation or switch-level simulation. In the linear circuit simulation session, I found that the AWE technique is a new approach to simulate linear or linearized circuit.The AWE technique employs the Pade approximation rather than numerical integration to approximate the behavior of linear(ized) circuits. It offers one to two order of speedup against traditional SPICE-like circuit simulators, with reasonable accuracy. I found that the idea of AWE may be applicable to the modelling of logic gates for switch-level simulation.

In the switch-level simulation, a new theoretical method for assigning signal flow directions to MOS transistors was proposed by University of Southern California. The determination of the signal flow directions is one of the major issues of many computer-aided design or analysis tools. With the knowledge of signal flow directions, the speed and accuracy of these tools can be significantly improved. Therefore, the proposed new approach may be a good reference for timing verification, electrical design rule checking, or switch-level simulation.

Besides, I found the exhibitions by software vendors to be worthwhile. Many CAD software vendors presented their new integrated CAD frameworks, which integrate different CAD tools for different design phases. From the exhibitions, I learned the trend of the CAD industry , and what work I can contribute to the CAD society.

Overall, the conference was well organized with many opportunities to meet with fellow researchers. I have learned a great deal from the conference, and I am very grateful to ACM/SIGDA for making this trip possible for me.

Sincerely,



Yu-Hsu Henry Chang

DAC-90

Report on the 27th ACM/IEEE Design Automation Conference

Kyunrak Chong

Computer Science Department

University of Minnesota

Minneapolis, MN 55455 USA

I would like to thank ACM/SIGDA for providing me the travel grant to the 27th ACM/IEEE Design Automation Conference (DAC) which was held in Orlando Orange County Convention Center, Orlando, Florida from June 24 through 28, 1990. The 27th DAC consists of two parts, technical program and exhibits, and I think it was very successful.

The technical papers are organized into 43 sessions and tutorials. Each session is classified into one of four sections, synthesis, physical design, test & verification and panel. My current research interest is in developing efficient algorithms for VLSI design. I mainly attended sessions in physical design but I also attended other sections to know the research direction in other fields. It will be really helpful for my current and future research.

During the conference, the world's top CAD/CAM companies demonstrate the recently developed hardware and software available in the industry. It was the good opportunity to know about the state-of-the-art CAD systems.

I really enjoyed attending the 27th DAC and also enjoyed many Orlando's tour attractions.

Report on 1990 Design Automation Conference

Alan Martello
Department of Electrical Engineering
University of Pittsburgh
Pittsburgh, PA 15261

The 1990 Design Automation Conference was once again extremely stimulating. For me, the high points of the conference presentations were the sessions devoted to timing issues and the tutorials. The presentations which discussed timing issues were informative since my research area is timing verification. The sessions proved to be filled with the most recent research and precipitated numerous discussions throughout the conference. The tutorials, especially the one covering symbolic simulation, provided excellent introductions to unfamiliar topics.

Unlike previous years, the vendor exhibits seemed unusually "lifeless"; there did not appear to be any electricity on the exhibit floor as there had been in previous years. Many vendors were attempting to demonstrate how their design environment was "revolutionary" because it was a *unified framework.* It is true that many of the vendor products were integrated much better than in previous years. However, I find it difficult to congratulate the CAD companies for achieving a level of integration in tools and products that in many other fields would only be the minimal level of acceptance.

One significant standout on the exhibit floor was once again the University Booth. The interest in current research at universities all over the country was encouraging. Both industrial representatives and academics were found crowding around the various exhibits from across the country. I feel that the SIGDA sponsored University Booth brings a bit of realism to the inflated claims of many CAD companies and illustrates the need for stronger industrial and academic research ties.

I found the SIGDA meeting extremely informative and was pleased to see so much activity aimed at advancing the field of design automation. I would like to extend to James Cohoon and the entire SIGDA board my sincere thanks for affording me the opportunity to attend this exciting conference.

Trip Report - International Test Conference 1990

Sharad Seth
Department of Computer Science & Engineering
University of Nebraska, Lincoln, Nebraska

The conference was held at Washington, D.C., from Sept. 10 to 14. The technical program this year was better than ever before. The excellent keynote addresses by Gary Daniels of Motorola and Akihiko Yamada of NEC set the pace for the rest of the conference. Daniels' 1984 keynote address to the conference is well remembered by conference attendees for its humor and accuracy of its predictions (10 million transistors in a microprocessor device by 1994 and the need for structured approach to design and test). The current trend is towards demand for higher quality levels, shorter cycle times, and more customized products at ever decreasing costs. The challenge for the future is for the technology of design, test, and manufacturing to keep pace these customer expectations. Yamada, in his keynote address, also discussed the challenge posed by ULSI circuits to design and test community.

A new topic of much interest was *IDDQ testing* for CMOS chips. In the simplest form, this is the same as leakage current testing practiced for a long time. In its sophisticated form, however, current measurements are made after application of each test vector. The vectors are generated to detect stuck-at, stuck-on, and bridging faults within each gate *to its primary output.* This last point is significant, because in a sense, IDDQ testing allows observing each gate output independently. Another topic, *boundary scan*, maintained high interest from the previous years.

In test pattern generation, in the lead paper of the conference, Rajski and Cox outlined a 16-valued logic algorithm which obviates the need for many proposed heuristics to speed up test generation. The most entertaining presentation of the conference came from B. Krishnamurthy of Tektronix who presented a new fault-simulation algorithm for combinational circuits on behalf of his coauthors, S. Akers, S. Park, and A. Swaminathan. Their X-algorith allows quick elimination of a set of faults from consideration in fault simulation. In the area of IC defect level analysis, I enjoyed J. Savir's presentation on AC product defect level and yield loss. The novelty in this paper is its concern not only for bad chips going out but also good ones rejected due to tester/test-procedure errors. I would have preferred, however, more qualitative explanation and presentation of experimental data.

The only exhibit that I attended turned out to be most enjoyable - a presentation by Synopsis of the beta-test version of their new software called *Test Compiler.* It is a test synthesis tools that automates DFT and provides automatic test pattern generation. The tight integration of a truly hierarchical synthesis environment with test logic frees the ASIC designer to explore many alternatives for optimizing speed and area with the test logic in place. The conference also saw the entry by AT&T for the first time in the CAD market with its announcement of SYSGEN (a sequential test pattern generator) and TAP DANCE (an audit tool for design conformance to the boundary-scan standard).

Report on 1990 Design Automation Conference

Naveed A. Sherwani
Department of Computer Science
Western Michigan University
Kalamazoo, MI 49008

The 1990 Design Automation Conference (DAC) was held at the Orlando/Orange County Convention Center in Orlando, Florida from June 24 through June 28. The hundred and thirty seven technical papers presented at the conference covered all aspects of design automation.

I attended sessions related to "Physical Design". Several papers pertaining to Routing (Detailed and Global) were presented. Almost all the detailed routers presented were multi-layer routers and used the gridless approach. With channel routers reaching optimality, some over-the-cell routers were also presented. The idea is to use the 'extra' layer on the cell to route some nets thereby reducing the congestion of channel. In *General Models and Algorithms for over-the-cell routing in Standard Cell Design,* Jason Cong *et. al.* reported as much as 20% improvement over conventional channel routers. The basic idea is use a planar subset of top (resp. bottom) nets to route over the cell. They selected the nets in a way that channel height is minimized. Another approach was taken E. Katsadas *et. al.* in *A Multi-Layer Router Utilizing Over-Cell Areas.* They assume four routing layers and partition the set of nets into two sets. One set is routed using conventional channel router between the channels while remaining nets are routed over entire region. Their experiments showed significant reductions in channel height.

In summary, the DAC was both educational and enjoyable. I thank SIGDA for providing me with a travel grant to attend the conference.

ICCD

1990 International Conference on Computer Design

Naveena Nagi
Department of Electrical Engineering - Systems
University of Southern California
Los Angeles, CA 90089-0781

This year the *International Conference on Computer Design: VLSI in Computers and Processors* was held in Cambridge, Massachusetts between September 17-19, 1990. The attendees included researchers from many major computer companies and universities around the globe. The conference was multidisciplinary and brought together all the key technology elements essential in computer design. Its scope was divided into four major areas - VLSI and Technology, Architecture, Computer-Aided Design, and Design and Test. My research interests include the last two areas, and I attended the sessions in those two areas.

There were 33 paper sessions in which 107 papers were presented, along with two plenary sessions and two panel sessions. The keynote address, entitled "Increasing human/computer bandwidth", was given by Carl Caricari, Vice President of IBM's Advanced Workstation Division. He pointed out that because computational capability has progressed significantly, new, larger, and more complex problems should be addressed. Dr. J. A. Darringer, in the computer-aided design plenary session gave an overview of past and present electronic design systems and predicted significant progress in the future. Professor M. R. Mercer, in the design and test plenary, gave a very informative yet entertaining talk outlining the basic problem of design verification. He gave examples from other areas such as. hotel design, and made a strong statement regarding the increasing role of functional information in digital design and test.

There were four paper sessions related to testing. In the Design for Testability session, Lee, Irwin, and Owens of Pennsylvania State University presented results of circuits synthesized by their tool FACTOR. This tool attempts to minimize the number of connections in the circuit instead of number of

gates. The resultant circuits are of tree type with restricted reconvergent fanouts, rendering them testable. Jha and Tong of Princeton University used binary decision diagrams for designing robustly testable static CMOS parity trees.

In the session entitled *Dealing with faults*, researchers from the University of Illinois and University of Texas presented techniques for fault grading of very large digital systems using a hierarchical approach. Use of hierarchy results in savings of memory as well as CPU time. Another paper by Levitt, Roy, and Abraham showed that physical failures in BiCMOS circuits cannot be realistically modeled by stuck-at fault model. They demonstrated that some of the failures result in delay faults.

The paper entitled "Test architecture of the Motorola 68040" gave a true picture of the state-of-the-art in testing with respect to the current design capability. The philosophy of testing was a *mixed approach*, i.e. to treat each class of logic in a different manner. A different design for testability approach was used for data paths, ROM/PLA structures, embedded RAMs, random logic, and finite state machines.

The plenary session entitled, "Is there a future for ATPG?" was moderated by Tony Ambler (Brunel Univ.). The panel consisted of Gordon Robinson (GenRad), Ralph Marlett (Racal-Redac), Dave Wharton (Crosscheck), Alexander Albicki (Univ. of Rochester), and Ken Wagner (IBM). After the panelists made their presentations, an exciting series of discussions followed. The general conclusion was that ATPG is somewhat lagging behind the state of design, and further research should be continued.

It was a great opportunity and learning experience for me to be at the conference. Meeting so many active researchers, both from academia and industry, in my areas of interest was a rewarding experience.

1990 International Conference on Computer Design

Rabindra K. Roy
Center for Reliable and High-Performance Computing
Coordinated Science Laboratory
University of Illinois at Urbana-Champaign

The 1990 International Conference on Computer Design: VLSI in Computers and Processors was held in Cambridge, Massachusetts during September 17-19, 1990. This conference covers all hardware aspects of computer design, from system level to physical-design level.

The keynote speaker stressed the availability of numeric-intensive supercomputing through advanced workstations and transparent networking computing, and concluded that the problems which once defied closed solutions are now within reach through increased computational capability.

In the session entitled BIST, researchers from University of Virginia presented techniques for compacting randomly generated test sets using genetic algorithms. The discussion following the presentation raised some issues on generating patterns for *random-pattern-resistant* faults using genetic algorithms. Another paper in the same session by Brglez, Gloster, and Kedem from MCNC addressed faults that are random-pattern-resistant for uniform random patterns. They generated optimized distributions of weights that guarantee pattern coverage in a given number of random trials.

The session on High-level Design in Japan was very informative, and gave a broad perspective. The paper entitled "Rule-based Testability Rule Check Program" introduced a checking process based on a combination of symbolic simulation and violation detection.

One unique feature of this conference is that there are sessions dedicated entirely to a specific product from industry. Last year, there were sessions on *IBM Second-Generation RISC* and *Intel i486 Processor*. This year *Motorola 68040* was the topic of one such session, in which four papers were presented. The first three papers described the designs of the memory modules and bus controller, the integer module, and the floating point unit, respectively. The last paper described the testing strategy

for Motorola 68040. The complex testing problem was resolved by applying different testing techniques to different classes of logic.

It was a great opportunity and learning experience for me to be at the conference. Meeting so many active researchers, both from academia and industry, in my areas of interest was a rewarding experience.

VHDL Methods Workshop

REPORT ON THE VHDL METHODS WORKSHOP
August 13-15, 1990; UVA, Charlottesville, Virginia

By:
Zainalabedin Navabi
Electrical and Computer Engineering Department
409 Dana Building
Northeastern University
Boston, MA 02115
617-437-5413
navabi@nuhub.acs.northeastern.edu

The VHDL Methods Workshop is an annual workshop. Current research conducted on VHDL methods and applications are discussed in the workshop meetings. The 1990 workshop was organized into five sessions and included presentations on system design, verification, information management, VHDL applications, and VHDL evaluation. The author made a presentation on use of VHDL for large system design.

The topic of this presentation was A Methodology for Describing CPU-Like Structures in VHDL. A synthesizable top-down description of a 32-bit processor with over 50 instructions, an address bus, a data bus, and DMA and interrupt handling signals was presented. In the next paragraph a brief description of the method used in describing this CPU will be given.

> At the top level the CPU is separated from its I/O devices. The CPU is then partitioned into a data section and a control section. The data section is further partitioned into registers, logic units, and buses. Logic units and registers of the data section are described at the behavioral level, and their equivalent hardware has been designed. The data section itself is described at the structural level with

dataflow level handling of bussings. The data section description has a clear hardware correspondence, and its description has been designed at the gate level. The control section, on the other hand, is a large state machine, for the description of which we have used one of our previously designed synthesis subsets. The hardware correspondence of this component is also designed. All the behavioral components have also been designed at the gate level and the timings extracted from the simulations of gate level designs have been used in back-annotating the original behavioral descriptions. Interface circuits for I/O devices have also been designed. These designs are done at the dataflow abstraction level. For the description of I/O devises high level behavioral VHDL is used. File I/O constructs of VHDL are used for input and output of the I/O devices. For example a printer model writes to a file named "paper".

Although the talk was targeted for system designers that are trying to use VHDL in their design environment, interest in the system design methodology was also expressed by those involved in teaching of computer systems. As a results, we are presently working on completing the descriptions and documenting the CPU such that this CPU model and VHDL descriptions can be used in CPU design courses. Using this model, hardware concepts can be illustrated through their corresponding VHDL descriptions.

Presentations on formal verification of VHDL indicate that this is an important issue which needs a lot of attention in the coming years. Talks on analog VHDL and SPICE in VHDL were among the many interesting parers of this workshop.

Report on the VHDL Methods Workshop *

Nand Kumar
University of Cincinnati
Dept. of Electrical and Computer Engg.
Cincinnati, OH 45221-0030

September 26, 1990

The VHDL Methods Workshop was held in Charlottesville, VA from August 13–15. There were a total of five sessions:

1. System Level Modeling Methods
2. Formal Verification
3. Information Management
4. Unique Methodologies that benefit from the use of VHDL
5. Status of VHDL Evolution

The sessions that were of interest to me were the sessions on system level modeling, formal verification, and unique methodologies.

In the system level modeling session the couple of presentations that were of particular interest were the presentation on uninterpreted modeling and a methodology for describing CPU-like structures in VHDL . The latter presentation was based on the notes and resulting code from a class taught by Professor Navabi at Northeastern University in which a 32-bit CPU was described in VHDL .

In the second session all the talks were interesting. Dave Barton talked about applicative characterization of VHDL in which he proposed a new data structure in VHDL that would maintain the histories of variables. Mike Dukes talked about a generalized extraction system for VLSI . His system extracted the circuit information from MAGIC files and verified the correctness of the circuit. Alex Zamfirescu talked about model equivalences in VHDL based design.

The session on unique methodologies contained Hal Carter's SPICE in VHDL that raised some interesting questions in the use of VHDL for analog quantities, and our presentation on distributed synthesis.

The workshop was held in an informal atmosphere, with a panel of speakers entertaining questions at the end of each session. The workshop was a good learning experience and I am grateful to SIGDA for letting me have this opportunity.

Report on MICRO-23

The 23rd Annual International Symposium and Workshop on Microprogramming and Microarchitectures was held November 27-29 in Orlando, Florida.

The keynote address was given by Michael Flynn. He described experiments where the speeds of different implementations of instruction sets were compared.

Many of the papers presented at the conference addressed scheduling problems. Several papers addressed software pipelining for VLIW machines. I enjoyed the animated panel session which considered the best balance of VLIW compiling and smart run-time hardware.

There were also papers covering problems in controller synthesis and caching strategies. Among the architectures presented, I found Gocal's Prism Architecture particularly interesting.

Mavaddat described a nice formal language model for register-transfer design, and an application of this model to local microcode synthesis.

I would like to congratulate Chris Papachristou and Vicki Allan for their fine work in organizing MICRO-23, and I am very grateful to SIGDA for supporting my participation.

David Binger
University of Illinois

RECEIVED BY E-MAIL 12 December 1990

Trip Report for the Fall 1990 VHDL Users' Meeting

Joanne E. DeGroat
Ohio State University

The VHDL Users Group continues to thrive and the meetings, which are a blend of a workshop and a conference, continue to prove the interest of both users and CAD vendors in VHDL. At this Fall meeting, the presentations showed clearly that VHDL has had a profound effect on the way we think about designing digital systems. Rather than perceiving design as "pushing gates," the electronics community is demonstrating a perception that proper design begins with specification. Then, rather than implement the specification in a prototype, the specification is translated into a VHDL model for validation of the intended implementation. VHDL is viewed as useful as a specification tool, but there is interest in a language at a level of abstraction above VHDL that will enhance the design process.

Also of great interest at this meeting was the ongoing effort which will lead to the re-balloting of VHDL for a new version of the standard in 1992. At this time the requirements desired in the new version are being coalesced and documented. As part of this process the effects of implementing a given requirement are being analyzed. Implementation of requirements that would make the 1992 standard incompatible with the current standard will be implemented only after lengthy analysis. Requirements will be categorized and prioritized. The highest priority will be given to correction of ambiguities in the current standard. At the very least the new standard will clean up the existing standard and incorporate some new and desirable features into the language.

The number of requirements satisfied will depend upon how many requirements are submitted and the time available to incorporate them into the language. Those requirements which are not incorporated into the language at this time will be considered for incorporation at a later date. The realization that the standardization of VHDL is an ongoing process was not anticipated when VHDL was first standardized. The Design Automation Standards Subcommittee is learning how to maintain a "living standard." There are some obvious growing pains as the committee learns but the process is progressing well and is on track to having an improved standard in 1992.

DA Standards Activities

This section contains announcements and news reports from various standards groups and committees that impact the DA community. These include:

UDL/I Announcement
EDIF Announcement
VHDL News (VHDL User Group)
CAD Framework Initiative News(CFI)

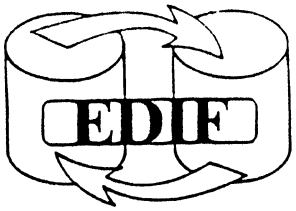
UDL/I software development awarded to Fintronic USA, Inc.

November 12, 1990
Japan Electronic Industry Development Association
UDL/I Software Development Committee

TOKYO, JAPAN, November 12, 1990 --- Japan Electronic Industry Development Association (JEIDA) announces the schedule for the first phase UDL/I software development and delivery. The main development plan, which includes the design and program development of the compiler, simulator, waveform user interface and others, has been awarded to Fintronic USA, Inc., of San Mateo, CA. This selection has been made by the UDL/I Software Development Committee (USDC) among four companies that submitted proposals: three from the USA and one from India. Recently, the detailed agreements among JEIDA, Fintronic USA and Advanced Software Technology and Mechatronics Research Institute (ASTEM), Kyoto, JAPAN, have been completed. The UDL/I Intermediate Format will be released at the end of March 1991, the beta program will be released by the end of December 1991, and the final programs will be distributed by the end of March 1992.

USDC plans to develop additional UDL/I related programs. It intends to counter-propose the development of such programs to the remaining offerors. Also, new offerors are welcome to participate, having good chances for obtaining development contracts. Further information will be available at the contact offices.

USDC opened its USA Branch office at Fintronic USA, Inc.. Dr. Alec Stanculescu, the president of Fintronic USA, Inc. is the Chair for this branch. The branch is opened to facilitate the communication between the UDL/I Software Development Committee and parties interested in UDL/I (including potential offerors of software development) that are located in the USA. The USA branch office will provide UDL/I related information to interested parties, and will collect ideas, questions, and comments related to the standardization of UDL/I. Application forms to join the USA branch of the UDL/I Software Development Committee, as well as more information regarding the USA branch of the USDC will be available at the contact offices.



CAE/CAD/CAM/CAT Engineers and Managers ...

If you're using EDIF (Electronic Design Interchange Format) in your work, you need the USA EDIF Users' Group. It offers:

- An open forum for exchanging information with experts about software applications relating to EDIF
- An annual meeting with tutorials and papers
- A newsletter
- An active platform for promoting EDIF

YOU QUALIFY FOR MEMBERSHIP ...

☐ If you are an active EDIF user ...

☐ If EDIF is in your future ...

☐ If you wish to promote EDIF ...

☐ If EDIF interests you ...

MEMBERSHIP IS FREE !!

Mail it NOW !! OR FAX Jeffrey Allison (Users' Group Chair) - 617-290-0708

Detach Page and Fold Here

Name_____ Title_____
Company_____
Mail Stop/Suite #_____
Address_____
City_____ State_____ Zip Code_____
Telephone #_____ FAX #_____
Email Address_____

Mail to:
Sally Hill, EDIF Users' Group, P.O. Box 25542, Tempe, AZ 85285-5542

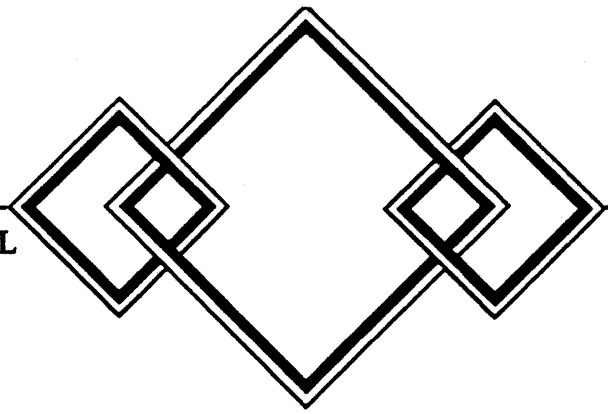
For More Information ....

Call Jeffrey Allison - 617-890-0333

VHDL NEWS

A Publication of the VHDL User's Group

Volume 4 - Number 1
November 1990



Update on Communications

Recently the number for the electronic BBS service offered by the VHDL Users' Group changed. The correct number to dial up is now (415)329-8649. The BBS can be dailed up at any baud rate (soon to expand to 9600 MNPS from 2400), parity, or start/stop bit settings.

Usenet Communcations - A Call for YOUR VOTE!!

Read on if you are familiar with Usenet and newsgroups:

As a result of the efforts of a Thomas Dettmer at the University of Dortmund in Germany, there is currently a news.groups discussion going on to establish a newsgroup called comp.lang.vhdl. In parallel, the VHDL Users' Group membership has expressed a desire to have such a notesfile, most recently at the VHDL Users' Group meeting in California. Such a newsgroup will help to increase the communication between the U.S., Europe and other countries and provide for free flowing discussion of VHDL issues.

There will be a vote taken beginning Monday, November 26th.

Please follow the process below to vote on the establishment of **comp.lang.vhdl**. A copy of the ballot is included for your review.

1. All voting begins on Monday, November 26, 1990, and continues for three weeks. Please mark your calendars!!! Your vote is important.

2. The casting of your ballot should be clearly stated in your mail header. For example, if your vote is positive, type "**Yes for comp.lang.vhdl**", or conversely "**No for comp.lang.vhdl**" This will assist us in quickly tabulating the responses.

3. Where to send your vote:

   U.S. and Canadian votes should be sent to rmr@inmet.inmet.com. If for some reason you are unable to reach Rachael Rusting, her fax is (617)868-2843.

   In Europe and geographically closer areas, votes should be sent to dettmer@saturn.ls1.informatik.uni-dortmund.de. If for some reason you are unable to reach Tom Dettmer, his fax is +49-231-755-2386.

If you have any questions, please contact Rachael Rusting at Intermetrics (617)661-1840 or rmr@inmet.inmet.com.

In order for a new newsgroup to be established, there must be at least 100 more positive votes than negative, and two thirds of the vote must be positive. Mark you calendars and **send us your vote beginning November 26th!!** Note that votes received before November 26 will not be counted.

Preview of the Ballot

Note: To review the actual ballot on November 26, refer to **news.groups**. Remember, do not post votes to the notesfile; they must be sent directly to the locations specified above to be properly recorded.

```
Preliminary version of a CALL FOR VOTES for "comp.lang.vhdl"

Please send your votes by e-mail in the time from November 26th to December
16th following the format defined at the end of this article (We need, at
minimum, 101 positive votes)

NAME/GROUP:
     comp.lang.vhdl

STATUS:
    unmoderated

CHARTER:
VHDL-1076 (VHSIC (Very High Speed Integrated Circuits) Hardware Describtion
Language) is an IEEE Standard scince 1987. It is "a formal notation intended for use in
all phases of the creation of electronic systems. ... it supports the development,
verification, synthesis, and testing of hardware designs, the communication of hardware
design data ..." [Preface to the IEEE Standard VHDL Language Reference Manual] and
especially the SIMULATION of hardware describtions. Additionally VHDL-models are a DoD
requirement for vendors.

Today simulation systems and other tools (synthesis, verification and others) based on
VHDL are available. The VHDL users community is growing fast. Several international
conferences organized by the VHDL Users Groups(s) have been held with relevant interest
Other international conferences adress the topic with growing interest as well
(Conference on Hardware Description Languages -CHDL-, [European] Design Automation
Conference -[Euro]DAC ...). More than one mailing list exists with lots of interest.

This group is a forum to discuss all problems related to VHDL Language and tools
supporting VHDL. Important topics are (without restriction to other ideas):
    Problems with the language [reference manual].
    VHDL validation suite and problems with it
    Books on VHDL
    Design example exchange.
    Available tools, their features and problems. (compilers, simulation,
        synthesis, verification ...)
    Coding conventions.
    The various groups and activities in/beside VHDL (WAVES, VASG...)
    Conferences on VHDL

An article will be posted periodially in this group, answering frequently
asked questions which did appear in the group. Thomas Dettmer (the author of this CFV)
is the volunteer for this job. Examples topics are:
   WHAT does VHDL, WAVES, ... mean
```

Where can I ftp ...
Can someone give me a list of introduction books to VHDL
and others (any help or idea is appreciated)

WHY THE NEW GROUP:
There are currently a lot of tools based on VHDL. As far as I know, they are all commercial, ranging fromm $500 (PC Version Simulator) to <unbounded>. A lot of people are working on tools and more are using the available ones. Some discussions in various groups and mailing lists prove that there is growing interest and a lot of questions/problems have to be solved. It seems that there will be enough traffic in the new group to justify the creation. A lot of other good reasons are available (thanks for all answers) but we cannot list all of them here.

SCHEDULE:

1. DISCUSSION is currently going on
   The discussion period begins on monday, october 22.
   It ends on tuesday, november 20.
   (possibly continued by email)
   send your ideas to news.groups (preferred)
   or directly to me (e-mail adress below)

2. VOTE
   Today we can see that the discussion is successfull, I'll send the call for votes on Monday, November 26 to the net and the info-vhdl mailing list. It will appear after that (delay depends on the moderator and mailing systems.) The rest of the procedure will correctly follow the rules to create new groups (see news.announce.newusers for details). The voting period ends at december 16th.

HOW TO VOTE
Your answer should be sent or forwarded by e-mail to:
dettmer@saturn.ls1.informatik.uni-dortmund.de
Put your vote in the subject of the mail. Format:
subject: YES comp.lang.vhdl or
subject: NO comp.lang.vhdl or
mail not following this format may not be counted, mail not containing a clear yes or no, without any "but we should..." is definitly not counted. Your mail MUST contain an email adress to contact you (no matter on what kind of net) - this is to enable a verification of the results by other netlanders. Votes posted to the net are not counted as well.

RESULTS
When the voting period is over, I have to wait 5 days for late answers. After that the results are published in the net and in the info-vhdl mailing list. The publication contains a short summary and the email adresses, names and votes of the voters. We need at least 101 YES votes and 2/3 of the total of valid votes must be YES to create the group. This will be done immediately after a positive result (hopefully) has been published.

tom

If you are not familiar with Usenet:

Usenet is a fairly amorphous, cooperative, informal and vast communications network. Usenet is accessible via a variety of ways. We suggest you contact your system adminstrator or your local university to see how you could be connected. While there is a commercial organization called Uunet which will connect you to Usenet for a fee, there is no requirement to use this organization to gain access to Usenet. In addition, it is ideal to find someone in your local area to act as a "feeder" to your organization, thereby saving long distance call costs.

If you have a modem, you can also access the VHDL Users' Group BBS at the number listed above.

Internet Repository and TISSS Information

There is an INTERNET repository and registered newsgroup. Mail items of interest to info-VHDL@uceng.uc.edu. Mail a request to be added to the group of registered news subscribers to info-vhdl-request@uceng.uc.edu. One can access the files online by "ftp"ing to account anonymous@uceng.uc.edu.

Similarly, information on Tester Independent Support Software System (TISSS) and the proposed IEEE Standard Waveform Vector and Exchange Specification (WAVES) can be obtained by "ftp"ing to the account anonymous@tisss.radc.af.mil (which is anonymous@131.5.3.1).

Call for Papers

The Spring VHDL Users' Group will be held in in April, 1990. The Call for Papers is attached. If you have any questions, please contact the Program Chair, Allen Dewey. Details will be mailed once location and dates are finalized.

VHDL NEWS is a publication of the VHDL User's Group. It is distributed to its members for their benefit. Those interested in receiving a copy, or in joining the VHDL User's Group, are invited to call or write the company officers.

Publisher: VHDL User's Group
3145 Geary Boulevard, Suite 123
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(415) 329-8673 (Voice information/mailbox)
(415) 329-8649 (Electronic BBS)
(415) 324-3150 (FAX)
(415) 329-0510 (Human)

Membership Information: c/o Conference Management Services
408 Waverley Street
Menlo Park, CA 94025
(415) 329-0510; (415) 324-3150 (FAX)

Editors

Rachael Rusting
Intermetrics, Inc.
733 Concord Avenue
Cambridge, MA 02138
(617) 661-1840

Fred Hinchliffe
CAD Language Systems, Inc.
15245 Shady Grove Road, Suite 310
Rockville, MD 20850
(301) 963-5200

Sponsored by the
VHDL Users' Group

CALL FOR PAPERS

Spring VHDL Users' Group

USING VHDL FOR ELECTRONIC PRODUCT DESIGN

April 1991

THE CONFERENCE

This conference is one of a biannual series of conferences on the use of VHDL in methodologies and tools in the digital electronic design environment. Practical experience on the use of VHDL in design, education, and design tool development will be emphasized.

VHDL is both a language and a complete paradigm for describing and designing electronic products. Its strength derives from its diversity and integration of levels of abstraction, and its use as both an IEEE and DoD standard by commercial tool vendors and users. There are many efforts sponsored by the IEEE, EIA, VHDL Users' Group, vendors and users looking for ways to further standardize and exploit the interchange of design information at various stages of the design and support cycles. Excitement in the industry is evidenced by the enthusiastic response at the many VHDL Users' Group Meetings over the past years.

TECHNICAL PROGRAM

Abstracts for presentation or panel discussion are invited for (but not limited to) the following topics:

- VHDL Experience
- Mixed Mode Simulation with VHDL
- Design for Synthesis and Test
- Performance Modeling with VHDL
- VHDL CASE Tools
- VHDL and the World of Test
- VHDL as a Tool to Teach Electrical Engineering Concepts
- Fault Modeling and Diagnosis with VHDL
- Integrating VHDL in the Design Environment
- Standards Updates

Proposals for half-day tutorials covering VHDL, modeling, and the use of HDL's in the design process are also invited.

PARTICIPATION

All interested parties are invited to attend and are encouraged to present issues and experience on any of the above topic areas. Participation by DoD program/contract managers, industry managers/project engineers, digital IC and system designers and tool developers is welcome. Interested speakers are requested to submit a title and an abstract for review. NOTE: If selected for presentation, a single camera-ready copy of each speaker's presentation will be required for reproduction and distribution to all attendees.

RESPONSE DATES

*COPY OF PAPERS (no more than 5 pages):	1 January 1991
NOTIFICATION OF ACCEPTANCE:	22 January 1991
FINAL PAPERS DUE:	1 March 1991

* Please note that for this conference we are asking for copies of the actual papers to be presented, *not abstracts*.

FOR MORE DETAILS

Conference Chair: Professor Hal Carter
ECE Department, ML 30
University of Cincinnati
Cincinnati, Ohio 45221
(513) 556-4781
hcarter@uceng.uc.edu

Program Chair: Dr. Allen Dewey
IBM
P.O. Box 950
Dept. G57B, Bldg. 708
Poughkeepsie, NY 12602
(914) 435-6040 FAX (914) 432-9407
adewey@pk705vmg.iinus1.ibm.com

Newsline

November 1990 *Published by: CAD Framework Initiative, Inc.* Vol. 2, Issue 3

CFI - Entering the Next Phase

Andy Graham, President
Motorola, c/o MCC

The tremendous success of the DAC '90 answered two important questions for CFI members and the viewing public: A) member EDA vendors are ready to cooperate, and B) the volunteer committee process can produce practical results in scheduled time frames. However, the DAC '90 experience also confirmed that the fulfillment of the CFI mission will require a significant effort and dedicated resources. For example, members of the Design Representation TSC worked full time to create their Procedural Interface Specification and the MCC CAD Framework Lab provided full time engineering resources, test software and facilities crucial to the project.

I believe the next questions CFI members must answer are:

1) Do we have the resources and infrastructure to accomplish our mission?

2) Will our process produce specifications that will enjoy wide commercial adoption?

3) How will CFI plan our problem-solving focus so that end users will buy the resulting vendor implementation?

As a full time assignee to the CFI, I will be working with the Board of Directors and the entire membership to bring about successful answers to these and other questions during the next two years. Although many companies are already making a strategic investment by assigning some of their best people to key CFI roles, this participation needs to be broader, especially with end users who are crucial in helping define requirements.

CFI's results to date have created high expectations for our eventual success. I believe that our anticipation of the requirements of this next phase and the continued leadership and support by all members will determine whether CFI will have its full impact on the industry.

Second Annual European CFI Meeting

Tom Rhyne, Treasurer
MCC

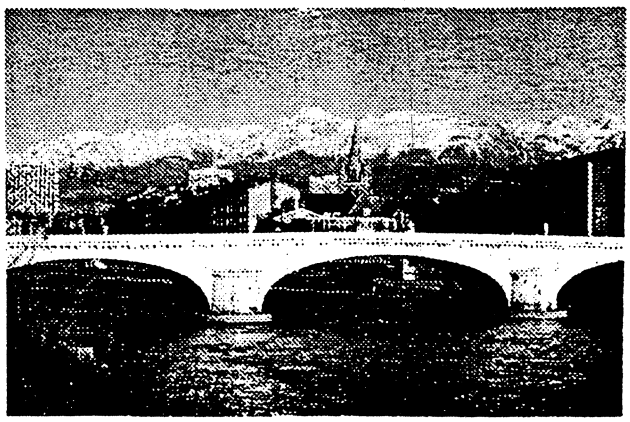
The Second European Meeting of the CFI was held in Grenoble on September 12-14, 1990. By all measures, it was a very successful meeting, a direct result of hard work and excellent planning by MP Associates, Inc. and its exemplary staff.

During the technical sessions, the TSC Chairs and their European Co-Chairs were provided opportunities to review current TSC activities and to identify activities which can be carried on independently by the European TSC members and the U.S. members. Coordination between the regional TSC memberships will then take place at the four "plenary" CFI meetings each year: the annual Business meeting, DAC, the European meeting, and ICCAD.

The Board of Directors meeting on September 12, 1990 reviewed the 1991 Integration Project, new proposals for the CFI's Technical Advisory Board, the interim progress of Earl Ecklund's "Must Kernel" committee, and a European proposal for a Benchmarking and Validation TSC. Andy Graham's offer to serve the CFI as a full-time loaned executive was accepted, and Andy presented his proposal for the "Phase-II" operation of the CFI. Details on that proposal will be worked out during the Board meeting following ICCAD.

The TCC meeting on September 13 discussed several minor revisions to the current TCC policies as well as the status of the draft proposals under consideration within each of the TSC's. The Base Standards Draft Proposal approved by the SE-TSC was also approved by the TCC.

The meeting concluded with an all-day session by the Architecture TSC.



Techincal Subcommitte UPDATES

Architecture

Noel Strader, Chair
MCC; (512) 338 - 3670

The Architecture Technical Subcommittee (A - TSC) met in San Fransisco (March 1-2, '90), Denver (April 19-20,'90), Orlando (DAC - June 29, '90), Boston (August 23-24, '90), Grenoble, France (September 14, '90) and Beaverton (Oct. 8-10, '90) since the last newsletter. At DAC, Noel Strader (MCC) was elected Chair and Bruce Malasky (Cadence) was elected Vice-Chair (renamed North American Co-Chair). The European CFI community named Leo Nabben (Philips) as European Co-Chair; an Asian Co-Chair has not yet been named. Marlow Draney (Mentor) has volunteered to obtain, assemble, and distribute minutes from A-TSC meetings.

Requirements Task Group (Paul Painter): The Users, Goals, and Objectives (UGO) part of the requirements document was approved by each TSC and then by the TCC in August 1990. The document is out for comments by CFI members. The Requirements Task Group is working to formalize the next level of detail, the requirements sections. Paul is working with the other TSC Chairs to get inputs to this section.

Architecture Task Group (Bruce Malasky): This task group is working on a framework dependencies document and on the execution model for a framework. The dependencies document is now titled "Framework Architecture." It contains a high-level view of a reference architecture. Final inputs to the first draft of this document are expected at ICCAD with a vote for TSC approved status early next year. Additional definition will be added to this document in future versions. Several execution models were presented at DAC, and execution models were discussed again in Boston. This topic was discussed at Beaverton in terms of scenarios of framework use.

Extension Language Task Group (Tim Barnes): This task group was relocated from the UI-TSC during the DAC meeting in Orlando. The task group is looking at requirements for extension languages (ELs), existing samples of ELs, and candidates for a CFI EL. Present candidate languages include C, C++, Common Lisp, and Scheme.

Specification for Specifications Task Group (Rowland Reed): A framework modeling effort was initiated by the A-TSC at the 1990 DAC. In August, the TCC created a task group, the Specification for Specifications Task Group, that subsumed the A-TSC group. The new task group has been meeting in conjunction with the A-TSC. They are working on procedural interface (PI) standards and documentation standards.

Tools Task Group: This effort has moved into the ITC-TSC.

Component Information Rules (Joseph Flanigan): This effort is in the process of defining a mission and attracting support within the CFI companies.

System Environment

Todd Scallan, Chair
IBM Corp.; (914) 385-5189

The System Environment Technical Subcommittee (SE-TSC) met four times since the last TSC update in the February 1990 CFI Newsline. New subcommittee officers were elected in June for the positions of TSC Chair (Todd Scallan, IBM) and U.S. Co-Chair (Yatin Trivedi, Sun Microsystems). Many thanks go to Keith Davis of Hewlett - Packard who served as Chair for the previous year.

A significant accomplishment for CFI was the establishment of TSC Co-Chairs for Europe and Japan. The SE-TSC Co-Chairs are Gordon Adshead (ICL) for Europe and Jouji Furui (Zuken) for Japan. The June meeting of the SE-TSC included attendees from both sides of the Atlantic and Pacific, including the newly designated Co-Chairs. This meeting represented the start of international activities for the SE-TSC on a formal basis. In an attempt to further increase international participation in the CFI process, the September working sessions were held in Grenoble, France. This meeting enabled the

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European-CFI to better understand TSC progress to date and to synchronize with current and future activities.
At the meeting in Grenoble, the SE-TSC hosted a representative from the X/Open consortium. X/Open defines guidelines that promote the portability, connectivity, and consistency of applications. Some of the work being done by X/Open overlaps with CFI, particularly in the areas of operating systems, networking, and window management. The SE-TSC intends to follow X/Open guidelines where appropriate so as to benefit from work that has already been done. In addition, the SE-TSC will attempt not to adopt guidelines that conflict with those defined by X/Open.

The SE-TSC has been making technical progress, although active participation has been low. The committee produced its first TCC - approved guideline. This guideline specifies "Base System Services" which provide the minimum functionality required for CAD frameworks and tools to execute on a hardware platform. IEEE POSIX 1003.1 is specified as the interface to these services. The SE-TSC contributed to the UI-TSC draft guideline that specifies "Basic User Interface Standards". Other draft guidelines being developed by the SE-TSC include a programming interface for a common error handling mechanism and support for ANSI C by CAD frameworks. In addition, the basis for a networking guideline is being formulated within the committee to address requirements for remote process communication and file distribution. The error handling mechanism previously mentioned is being considered for inclusion in the '91 Integration Project.

The SE-TSC approved the "CAD Framework Users, Goals, and Objectives" document that was generated by the Architecture TSC. The committee generated a list of detailed SE requirements that will be incorporated beneath the goals and objectives described in the document.

Key work activities planned for future meetings include guideline development for error handling, ANSI C support, and networking. Members of CFI are invited and encouraged to participate.

Design Methodology Management

Kenneth Fiduk, Chair
MCC; (512) 338-3518

The Design Methodology Management Technical Subcommittee (DMM-TSC) has had two meetings since the DAC CFI meetings. The TSC met on August 21 & 22 at Digital Equipment Corp., in Marlboro, MA, and on September 12 & 13, in Grenoble, France. By the time this article goes to press, a third meeting will have occurred on October 8-10, at Mentor Graphics, in Beaverton, OR.

The DMM-TSC has made significant progress in several areas over the last few meetings. The Execution Log Format guideline candidate has been distributed to the general CFI membership for review. The current, primary focus is on the development of the Tool Abstraction Specification. This guideline defines standard information necessary to aid in automating the invocation and control of individual tools. Tools execution information is divided into three categories: 1) information from the tool vendor, such as command line syntax, arguments, data requirements, etc.; 2) execution environment related information like location of tool, icon specification, performance data, etc.; and 3) methodology related information, such as pre - and post - execution requirements, tool function, etc. Some of this information is static and need only be accessed once, while some is dynamic, and must be read prior to each tool invocation. The static information can be provided in an interchange format form. Dynamic information, such as current defaults and last-used values for invocation parameters may vary from invocation to invocation, and must be accessed repeatedly. The first draft of the specification deals with the static, vendor-supplied information only, and a format for representing that information. Subsequent versions of the specification will be extended to include dynamic data and categories 2 and 3. For this information, a procedural interface will also be defined.

A tutorial paper on existing efforts in the DMM area is being drafted, expanding on the initial research done for the DMM paper presented at DAC '90. This paper identifies several classes of solution approaches, highlighting strengths and weaknesses. This paper will serve as one source of information in the development of a task and execution environment model. A taxonomy of design scenarios is also continuing to be developed to serve as validation for these models as they are developed.

The TSC has also submitted two proposals incorporating guideline activities for consideration in the CFI '91 Integration Project. Finally, elections will be held at the ICCAD CFI meetings for the TSC Chair and North American Co-Chair. Nominations will be accepted through the October meetings, both at Beaverton and the European CFI meetings in Warrington, UK. Participants will be able to vote either by mail or at the DMM-TSC meeting on November 15 after ICCAD.

Inter-Tool Communication

Ed Guy, Chair
Digital/MCC; (512) 338-3665

Since the Design Automation Conference, the Inter-Tool Communication Technical Subcommittee has held three meetings. The August meeting was hosted by Frank Cole of Westinghouse in Baltimore. At this meeting, the group worked on several areas: Joe Flanigan gave a presentation on the OSF/DCE progress; we made further progress on the ITC Architecture document and the ITC Message Dictionary. We also started an object oriented analysis of the current ITC PI.

The second meeting was held in Grenoble, France. The purpose of this meeting was to synchronize the European and North American ITC groups. At this meeting we had formal presentations by Brian Taylor on IBM's Message Server, Kim DeVilbiss on the Valid Communication Manager, and Kevin O'Leary on Tool Communication using the Computervision Design Desk Framework. There were also presentations on the updated Structural Procedural Interface (SPI) by Philippe Reyneart of Mentor/EDC, (European ITC Co-Chair) and on the SPOOK project at INESC by Helena Sarmento. We then reviewed the ITC Architecture and PI, and refined the ITC Message Server Model. Two European ITC Task Groups were also started. These groups will focus on Wide-Area Library Distribution and Inter-Simulator Communication.

The third meeting was held in Beaverton, OR at the Mentor headquarters. Again at this meeting we reviewed the ITC Procedural Interface and the ITC Architecture preparing for completion at ICCAD. The latest PI is based on the Object

Oriented message server model and is consistent with the latest CFI Specification Format. We also had a joint meeting with the User Interface and Architecture Technical Subcommittees to discuss the physical event handling mechanisms in the ITC tool interface.

ITC's next meeting will be held at the ICCAD Conference. At this meeting we plan to finish the ITC Architecture and Procedural Interface Documents. We also plan on expanding the current ITC Message Dictionary to support the CFI '91

Design Representation
Laurence Brevard, Chair
MCC; (512) 338-3567

The Design Representation TSC is defining an Informational Model (IM) and a corresponding Programming Interface (PI) through which design data can be accessed and manipulated. Recent meetings of the TSC have been in Marlborough, MA, in August, in Grenoble, France, in September, and in Beaverton, OR, in October. The next meeting will be in November 15-16, at the Sunnyvale Hilton after ICCAD.

At the 1990 Design Automation Conference, consumers were only able to read scalar netlists using a preliminary version of the interface. The next version will include non-scalar netlists and allow creation and modification as well as traversal of data.

The SIX BOX model from DAC '90 has been extended and is being described in the Express language. There is now a Base Object Model for Object, NamedObject, and Property. A Base Connectivity Model has Library, Cell, Viewtype, View, Port, Instance, Port Instance, and non-scalar Nets. The Programming Interfaces style is being refined based on lessons learned in the DAC '90 demonstration. It is moving to a simpler naming convention with fewer functions required.

A two-man team is now editing a specification to be used in the CFI '91 Integration Project with preliminary demonstrations scheduled for DAC '91. The first draft of this will be reviewed at the November meeting (after ICCAD).

User Interface
Craig Wier, Chair
Mentor Graphics, Inc.; (512) 526-4781

The User Interface Technical Subcommittee (UI-TSC) met in September and again in October. The September meeting was in Grenoble, France and was the European meeting for the CFI members. There were 11 participants, roughly evenly divided between Europeans and North Americans. The European Chair, Bill Chown (Mentor Graphics, Europe) chaired the meeting. The TSC met for a day and a half. The goal of the first half-day was to bring the European participants up to date on the activities of the TSC working groups. The UI-TSC then joined the SE-TSC to hear a presentation on internationalization by Dean Adams from X/Open. Subsequent work carried out by the committee working as a whole included the development of a list of explicit user-interface-based requirements on the Extension Language and a list of internationalization issues for the Internationalization working group to review and consolidate.

The October meeting in Beaverton, OR attracted about 18 participants. A major objective was the re-voting of the draft Basic User Interface Standard, version 1.02. The draft guidelines were approved and are now TSC-Approved Guidelines. Subsequently, a newly created Extension Language Working Group in the UI-TSC refined and added detail to the list of user-interface requirements on the extension language developed at the September meeting. The Style Guide Working Group continued working on refining of the Style Guide document. The UI-TSC also participated in a joint meeting with the ITC and ARCH TSCs to consider details of the proposed ITC mechanisms.

The next meeting of the UI-TSC will be in Santa Clara following ICCAD, November 14-16, 1990, Sunnyvale, CA.

Design Data Management
Steve Banks, Chair
Valid Logic; (408) 432-9400 ext 8656

The CFI Design Data Management TSC is currently working in three areas: Storage Management, Name Resolution, and Consistency. Storage Management is concerned with all aspects related to storage of persistent data. This is the DMM TSC's most active working group. To date they have published a Storage Management Requirements document which is up for vote by the CFI membership at the ICCAD '90 meeting, and have also produced a draft functional interface document for Storage Management which is out for initial review outside of the SM working group.

Name Resolution is concerned with issues related to identifying objects based on incomplete references, version management, and configuration management. This working group is responsible for a DMM architecture, information model, and functional interface. This group is the focus for the majority of the features related to Design Management, including checkpointing, release control, version control, project organization, library management, etc.

Consistency is concerned with issues related to identifying and maintaining consistency between various objects which combine to represent a design, and between design data and associated meta data. This last working group recently received new life when it was handed off to the European membership. While European DDM members will also be active in other working groups, this area will be managed in Europe and will be worked on primarily at European regional meetings.

The DDM TSC is also developing a glossary of terms common to design management, and supplying inputs to the CFI Requirements document.

Special Group Updates

TCAD Framework Group
Wally Dietrich, Chair
IBM Corp.; (914) 945-2073

Technology CAD (TCAD) is CAE for semiconductor device and process design, technology characterization for circuit design, and IC manufacturability. It includes modeling of fabrication process steps at the sub-micron and macro levels, and electrical simulation of small circuits. The modeling techniques used range from numerical simulation to analytic methods.

In late 1989, under SRC and DARPA sponsorship, a joint

industry-university group began to form framework guidelines for TCAD. This group joined CFI on a trial basis in June 1990, holding its first CFI meeting on June 29th. At this meeting we narrowed our focus to inter-tool communication of semiconductor wafer representations and semiconductor process representations (SWR and SPR). We also decided to create "Technology Examples" to test our draft guidelines. Alex Wong (Berkeley) and Mark Law (Univ of Florida) were chosen to head the SWR and Technology Examples working groups.

During the summer, two previously-planned SRC workshops were held to start the SWR and SPR work. These were attended by over 60 people.

The SWR working group held its first meeting on Sep 17-18 at Bell Labs. This meeting was attended by 14 people. The group decided that the representation should use a client/server and object-oriented approach, with servers for geometry, fields, and attributes.

The TCAD Framework Group will meet again on Nov. 14 (SWR only) and Nov. 15. At the 11/15 meeting, the SWR and Technology Examples working groups will make presentations to the entire group. Following the Group meeting, the SWR working group will meet again and the SPR working group will hold its first meeting.

ACCESS TO CFI PUBLICATIONS

The CFI has developed two new services to increase the availability, timeliness, and ease of access to information for its members. These services provide the ability to order paper and electronic copies of CFI publications. The available CFI publications include CFI proposals and guidelines, TSC minutes, and other CFI information.

A paper copy of CFI publications is available to **corporate members** through the CFI Office managed by MP Associates (MPA). MPA provides a quarterly index of CFI publications to CFI corporporate members and allows publications to be ordered by phone and FAX. The CFI Office can be contacted at (303) 530-4562.

Electronic access to CFI publications is available through the CFI publication server that acts as an electronic depot for CFI publications. CFI publications and a publication index can be accessed through simple electronic mail requests to the server. This service is described in the CFI publication "Electronic Access to CFI Publications" by Ed Guy and Paul Magelli (this document is available from the CFI Office). An empty electronic mail message sent to **cfi-server@etg.cad.mcc.com** will also return a description of the service. The facilities and support for electronic access to CFI publications are provided by Digital Equipment Corporation.

IMPORTANT DATES

Nov. 15-16, 1990: Sunnyvale Hilton, Sunnyvale, CA
Subcommittees will meet Thur., Nov. 15th, 8:00am to 5:00pm. Architecture subcommittee will meet Fri., Nov. 16th, 8:00am to 5:00pm. A meeting fee will be charged of $50.00 to CFI members and $80.00 to non-members.

Jan. 14-18, 1991: Hewlett - Packard, Fort Collins, CO
Subcommittees will meet on the five day schedule. 8:00am to 5:00pm.

Feb. 25-March 1, 1991: Sunnyvale Hilton, Sunnyvale CA
Annual Election Meeting
Subcommitees will meet on the five day schedule; 8:00am to 5:00pm.

May 15 - 17, 1991: Austin, TX; DAC Project Review at MCC

June 21-22, 1991: Sheraton Hotel, San Francisco, CA
Post DAC Meeting

Graham Appointed CFI's First Full-Time Executive

Boulder, Colo., Oct.8, 1990— Andrew J. Graham has been appointed the first full-time executive of the CAD Framework Initiative (CFI), an organization chartered to establish standards for electronic design automation, at a recent board of directors meeting in Grenoble, France.

Graham will serve as CFI president, a position he has held voluntarily since May 1988. His CFI salary will be paid under an assigned employee agreement with Motorola, Inc. Graham had been Manager of the Design Automation Systems Group in Motorola's ASIC Division. He will be located in Austin, Texas, where CFI will open its first headquarters next month.

Dr. Mel Slater, director of Semiconductor Systems Design Technology at Motorola, said, "CFI has proven its effectiveness by developing in just nine months a procedural interface guideline that successfully linked the design tools of more than twenty vendors in a demonstration at the 1990 Design Automation Conference. That achievement and strong worldwide support for CFI convinced Motorola to increase its own support through a loaned executive arrangement. We hope other members will follow our example by committing more of their technical and professional resources to CFI."

The CFI bylaws, adopted in 1989, provide for full-time staff. With upcoming publication of CFI's draft framework guidelines, along with planning for seven technical subcommittees and CFI's 1991 Design Automation Conference project, this is a crucial time to organize a dedicated executive staff, according to Graham.

"CFI is a truly global consortium organizing for a new phase of activities to deliver strong commercial guidelines," Graham said. "The continuity and professional management provided by a full-time staff will ensure the successful transition to this new phase."

Graham, the founding president of CFI, has been with Motorola since 1983. He was responsible for the integration of commercial and proprietary ASIC design tools as head of the Design Automation Systems Group in the ASIC Division. He holds a B.A. degree in business from the University of South Carolina.

CALL FOR PAPERS

INTERNATIONAL TEST CONFERENCE 1991
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Authors are invited to submit **original, unpublished papers** for formal presentation or **poster proposals** describing recent work and results. Submissions must include:

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- Indicate whether submission is for **paper** or **poster**
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Important Dates:

• February 4, 1991	Technical paper submissions deadline
• May 24, 1991	Notification of paper submitters.
• August 2, 1991	Poster submissions deadline
• August 16, 1991	Notification of poster submitters.
• July 19, 1991	Deadline for receipt of camera-ready manuscripts and IEEE copyright forms.

Send all submissions to:

International Test Conference, 1201 Sussex Turnpike, Suite 101, PO Box 264, Mount Freedom, NJ 07970, USA.
Telephone: (201) 895-5260, FAX: (201) 895-7265

Kenneth Mandl, Program Chair

Topics of Interest include, but are not limited to:

Design and Test Integration
Built-In Self Test
Boundary Scan
Design for Testability
Design Synthesis
Design Verification
Computer-Aided Engineering
Computer-Aided Test Generation
Testability Analysis
Fault Simulation
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Physical Defects
Fault Modeling
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AI and Expert Systems Applications
Statistical Process Control
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All papers should be suitable for a **20 minute** presentation and should not have been published previously.

Please submit 6 double-space single-sided copies of a **50-word abstract** and a more detailed summary, not to eceed either 1,000 words or six pages including figures.

Submissions should include on a separate page: the paper title, full author names and affiliations, a complete return address, telephone and Fax numbers, email address and the name of the author to whom communications should be addressed. Author(s) names and addresses should not appear on the abstract and summary.

Papers should be submitted by **April 1, 1991** to:

CCVLSI '91 Program Committee
Department of Electrical Engineering
Queen's University
Kingston, Ontario
K7L 3N6
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Notification of acceptance will be about **June 1, 1991.**

A camera-ready manuscript will be required by **July 15, 1991.**

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Authors are invited to submit 12 copies of:

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Authors of papers selected for presentation at the workshop will be asked to prepare an illustrated text for inclusion in the workshop proceedings. Selected papers from the proceedings will also be published in book form after the workshop.

IMPORTANT DATES

Deadline for Submission:
March 1, 1991
Notification of Acceptance:
May 1, 1991
Deadline for Final Version:
July 1, 1991

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International Workshop on Logic Synthesis

Research Triangle Park
North Carolina, USA

May 7-10, 1991

Sponsored by MCNC
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Return this form to:

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Name:_____ Telephone: _____
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Street/PO Box:_____ Fax/Email: _____
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Please check:

_____ I wish to preregister for the workshop
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_____ I wish to contribute to the benchmark experiment and receive more information

FIRST CALL FOR PARTICIPATION

You are invited to participate at the International Workshop on Logic Synthesis to be held at MCNC, Research Triangle Park, North Carolina, on May 7-10, 1991. Presentations will focus on recent developments in all areas of logic synthesis, including:

- multi-level minimization
- boolean and algebraic decomposition
- technology mapping and translation
- area and timing optimization
- algorithmic vs. rule-based approaches
- finite state machine synthesis
- sequential logic synthesis
- retiming
- synchronous logic synthesis
- sequential circuit optimization
- PLD/FPGA based synthesis
- synthesis and verification
- synthesis based testing
- logic-level synthesis from high-level descriptions
- logic synthesis systems
- designer experiences with synthesis tools
- standard synthesis benchmarks

Sequential logic synthesis will be emphasized.

In order to promote free and open discussion, no cameras or recording devices will be allowed. To facilitate better sharing of ideas, the workshop will be limited in size. A proceedings of accepted proposals will be compiled and distributed to all participants. All submissions are voluntary and the proceedings are issued as a service to attendees.

SUBMISSION OF PROPOSALS

Participants wishing to deliver a scheduled presentation should submit 20 copies of an extended description of their work, not exceeding 8 double-sided pages (This is the limit that will be accommodated in the proceedings.). All proposals will be reviewed by the technical program committee.

Standard Benchmarks

A unique aspect of the workshop is the presentation of benchmark results. Benchmark documentation will be available in the fall. Please contact Saeyang Yang (919-248-1800) for benchmark information.

DEADLINES

February 15, 1991	Last day to receive proposals
March 27, 1991	Notification of acceptance
April 1, 1991	Mailing of workshop program and registration
May 1, 1991	Last day to receive proposals for presentation of benchmark results
May 1, 1991	Registration due date

For further information contact:

Franc Brglez
MCNC
P.O. Box 12889
3021 Cornwallis Rd.
RTP, NC 27709
919-248-1925
brglez@mcnc.org

A. Sangiovanni-Vincentelli
UC-Berkeley
Dept. of EECS
Cory Hall
Berkeley, CA 94720
415-642-4882
alberto@ic.berkeley.edu

Saeyang Yang
MCNC
P.O. Box 12889
3021 Cornwallis Rd.
RTP, NC 27709
919-248-1800
syang@mcnc.org

Rebecca Gebuhr
MCNC
P.O. Box 12889
3021 Cornwallis Rd.
RTP, NC 27709
919-248-1841
gebuhr@mcnc.org

CALL FOR PAPERS

IEEE INTERNATIONAL CONFERENCE ON COMPUTER DESIGN: VLSI IN COMPUTERS & PROCESSORS

Sponsored by: IEEE Computer Society and IEEE Circuits and Systems Society
In Cooperation with: IEEE Electronic Devices Society

ICCD '91

Hyatt Regency Cambridge, Cambridge, Massachusetts
October 14-16, 1991

The International Conference on Computer Design: VLSI in Computers and Processors covers all aspects of the design and implementation of VLSI computer and processor systems. The multi-disciplinary nature of the conference is intended to emphasize the interactions among architecture, computer-aided design, design & test, and VLSI technology. Original papers are especially solicited in the following areas as they relate to computer and processor design:

Architecture and Algorithms: Computer Architecture: Concurrent Computers • Digital • Signal and Image Processors • Data Base Machines • Graphics Processors • Architectural Support for Operating Systems and Languages • Computer Design: Cache and Memory System Design • Processor Design • Computer Arithmetic • Computer Networks • Algorithms: Design and Analysis of Algorithms • Parallel Algorithms • Numerical Methods

Computer-Aided Design: High-Level Synthesis • Silicon Compilation • Automatic Layout: Placement and Routing • Layout Verification • Timing Analysis • Logic and Circuit Simulation • Multiprocessor and Parallel Processor • Implementation of CAD Algorithms • Dedicated CAD Hardware • Integrated CAD Systems

Design & Test: Mixed Analog/Digital Design • Design for Testability • Design for Self Test • Testing and Testability Analysis • Fault Modeling • Reliable Computing • Design for Reliability

VLSI & Technology: State of the Art System Integration • Packaging • Wafer-Scale Integration • Environmental Factors • Optical Interconnects • VLSI: CMOS • Bipolar • GaAs • Low Temperature • Mixed Technologies • Storage: Optical • Magnetic • Semiconductor

Papers are also solicited which describe innovative features of new products and the overall integration of Technology, Architecture, CAD, and Design and Test into the Computer Design Process.

Instructions to Authors

Prospective authors are invited to submit a 3-4 page, single spaced summary plus additional pages for key figures, diagrams, and references. To be considered for review, the following information must be included: (a) a clear description of the contribution and why it is important, (b) original research submissions must state what is novel about the contribution, (c) review and tutorial submissions must state the contribution to the multi-disciplinary mission of the conference. Authors should indicate the appropriate technical area for their submission: Architecture and Algorithms, Computer-Aided Design, Design and Test, or VLSI and Technology.

Submit six (6) copies of summaries, along with the authors' names, addresses, e-mail addresses and office and home telephone numbers, no later than **February 1, 1991** to the Technical Program Chair:

Dwight Hill
AT&T Bell Laboratories
3D-446
Murray Hill, NJ 07974
Telephone: 201-582-7766
E-mail: dwight@research.att.com

- Proposals for specially organized sessions are solicited. Please forward your proposals to the Technical Program Chair for review no later than **January 2, 1991.**
- Summaries to Technical Program Chair: **February 1, 1991.**
- Notification of acceptance: **March 31, 1991.**
- Final camera-ready paper due **June 15, 1991.**
- Awards will be presented to the best conference papers.

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BRAZILIAN MICROELECTRONICS SOCIETY

JULY 15-19, 1991
MINASCENTRO CONVENTION CENTER
BELO HORIZONTE - BRAZIL

CALL FOR PAPERS

THE CONFERENCE

The annual congress of the Brazilian Microelectronics Society brings together Brazilian and international specialists and researchers in several areas related to microelectronics.

The following activities are included in the conference:

- technical sessions
- invited papers
- panel discussions
- tutorial courses
- industrial exhibition

Invited international specialists participate in the activities of the congress.

New products from the industry and from the major Brazilian research centers can be seen in the industrial exhibition.

AREAS OF INTEREST

Authors are invited to submit papers in all areas of microelectronics. Topics include, but are not limited to:

- integrated circuit design
- computer aided design
- simulation, verification, and testing
- fabrication processes
- materials, devices, and circuits
- instrumentation for microelectronics

SUBMISSION OF PAPERS

Contributions will be accepted in English or in Portuguese, in either of two categories:

- full-length paper
  Up to 10 pages long, for presentation in oral sessions.
- short paper
  Report 2 pages long, for presentation in a poster session. This is a brief technical communication which suits the purpose of reporting partial or preliminary results of undergoing research and development.

Camera-ready originals plus 3 (three) copies should be sent to the address below, where additional information can be obtained.

VI SBMICRO Congress
A/C José M. Mata - Organizing Committee
Depto. de Ciência da Computação - UFMG
Caixa Postal 702
30161 Belo Horizonte, MG - Brazil
Telefone: (031) 443-4088
Telex: (031) 2308 UFMG
Fax: (031) 443-6757
E-mail: sbmicro91@lncc.bitnet

Deadline for submission of manuscripts: March 25, 1991

PAPER FORMAT

The papers have to be submitted in a camera-ready format, in double spaced A4 paper (297 x 210 mm), leaving 25 mm margins on each side. The first page should include the title, author identification, and abstract.

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Gathering Data for Planning

CALL FOR PARTICIPANTS

1. **ELECTRONIC GROUP INTERACTIVE SESSION (EGIS) WITH ACM SIG MEMBERS**

2. **ELECTRONIC GROUP INTERACTIVE SESSION (EGIS) WITH ACM STUDENT MEMBERS**

There's a great deal of excitement within ACM lately as a result of the adoption, by ACM Council, of a "Strategic Plan for the 1990's". A summary of the plan appears in the December 1989 issue of *Communications*. The plan calls for, among other things, a major effort to gather information about the needs and desires of members (and non-members) of ACM and its sub-units in order to make ACM more responsive to the needs of these individuals and to set ACM's future directions. Information will be gathered via traditional mail surveys, face-to-face focus groups, and an experimental concept called EGIS (Electronic Group Interactive Session). An EGIS is a discussion group conducted over a period of time using electronic mail.

We are currently forming two EGIS groups made up of approximately 20-30 members each. The first group will consist of members of ACM SIGs (who may or may not be members of ACM). Please note that for this particular part of the project, we are primarily interested in SIG members who have not recently held leadership positions in their SIGs. The second group will consist of Student members of ACM. From both groups, we are interested in hearing views on current and future ACM programs, products, and services.

The questions to be discussed by the groups will primarily be in regard to the professional needs participants have and whether or not those needs are currently being met by ACM or any other organization or service.

The groups will run over a two-week period (April 2 - April 15, 1991). Selection will be based on certain criteria (e.g., location, length of membership, etc.) with the aim of having the group represent, to the extent possible, the relevant ACM population. The protocol and process for managing the groups are currently under review and will be explained in future communications. If you are interested in participating in one of the groups, (**you must be committed to using email regularly,** i.e., we expect that participants will read and respond to discussion group mail on a daily basis), please send the following information to the group's coordinator, Lorraine Borman (email is preferred, but US mail is OK; see address at the end of this memo) by **March 15, 1991.** Individuals selected to participate will be notified by March 22, 1991.

Name
Mailing Address
Telephone Number(s)
E-mail Address
EGIS in which you'd like to participate (SIG or Student members)

Please answer the following questions (to help us form a balanced group), noting the question numbers in your response.

FOR THE EGIS WITH MEMBERS OF ACM SIGS:

1. To which SIG(s) do you belong?

2. How long have you been a SIG member?

3. Do you currently hold a major office or position in the SIG (Chair, Vice-Chair, Secretary, Treasurer, Newsletter Editor, Advisory Board member) or have you held such an office or position within the past year? If so, which one?

4. Are you a member of ACM? Category? (Voting, Associate, Student)

5. Are you a member of an ACM Chapter, Student Chapter, Local SIG?

6. Are you primarily an educator? researcher? practitioner? manager? student?

FOR THE EGIS WITH STUDENT MEMBERS OF ACM:

1. Are you an undergraduate or graduate student?

2. How long have you been a student member of ACM?

3. Are you a member of ACM SIGs? Which one(s)?

4. Are you a member of an ACM Chapter, Student Chapter, Local SIG?

5. Do you currently hold a major office or position in a SIG, Chapter, Student Chapter, Local SIG (Chair, Vice-Chair, Secretary, Treasurer, Newsletter Editor, Advisory Board member) or have you held such an office or position within the past year? If so, which one?

We appreciate your interest in ACM and expect that your participation in our project will be rewarding for you as well as beneficial for ACM. It's your chance to say what you want from your computing society...and be part of an interesting process!

Thank you very much. I am looking forward to hearing from you.

Lorraine Borman
Chair, DataPlan Committee

Email: Borman.chi@xerox.com

US mail: 1865B Tanglewood Drive, Glenview, IL 60025


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SCME (Stichting Centra voor Microelektronica)

and other European technical societies.

Proceedings will be published by the IEEE Computer Society Press.

CONFERENCE BRIEF SUMMARY OF ACTIVITIES

Sunday 24 February

Registration for Tutorials

Monday 25 February

Registration for Tutorials
Tutorials
Conference Registration
Vendor Exhibition
Vendor Presentations
Welcome Reception
Fringe Meetings

Tuesday 26 February

Speakers Breakfast
Conference Registration
Plenary Opening Session
Parallel Technical Sessions
Vendor Exhibition
Technical Posters
Spouses Programme
Civic Reception
Fringe Meetings

Wednesday 27 February

Speakers Breakfast
Parallel Technical Sessions
Vendor Exhibition
Technical Posters
Spouses Programme
Panel Session
Candlelight Canal Cruise

Thursday 28 February

Speakers Breakfast
Parallel Technical Sessions
Vendor Exhibition
Close of Conference

EDAC 91
Amsterdam 25-28 February 1991

REGISTRATION FORM

Please use BLOCK CAPITALS

Surname/Family Name _____ Forename _____

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TUTORIALS FEES

	Payment Received Before 1 Jan. 1991	Payment Received After 1 Jan. 1991
Authors/co-authors and members of professional organisations*	Dfl 400	Dfl 440
Delegates	Dfl 500	Dfl 550
Research Students	Dfl 250	Dfl 275

TOPIC

You may combine an A, B or C tutorial with an E, D or F. Please tick one in each category.

Morning Session (Tick one)

A: Analogue Design _____

B: Design for Testability _____

C: High Level Synthesis _____

Afternoon Session (Tick one)

D:Synthesis of Signal Processors _____

E: Floorplan Design _____

F: Logic Synthesis _____

REGISTRATION FEES

	Payment Received Before 1 Jan. 1991	Payment Received After 1 Jan. 1991
Authors/co-authors and members of professional organisations*	Dfl 800	Dfl 850
Delegates	Dfl 900	Dfl 950
Research Students **	Dfl 300	Dfl 300
Accompanying Persons	Dfl 275	Dfl 275

GRAND TOTAL Dfl _____

* Membership no: _____

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Julie Eitzer
(212) 869-7440

RELEASE DATE:

IMMEDIATE
October 5, 1990

Please include the following listing in the CALENDAR OF EVENTS section of your publication:

Second Physical Design Workshop
May 20-22,1991,
Pittsburgh, PA

Sponsored by ACM, The Association for Computing Machinery and the Special Interest Group: SIGDA

For further information contact: Mary Jane Irwin, Pennsylvania State University, Dept. of Comp. Sci., University Park, PA 16802; phone (814) 865-1802; email: mji@guardian.cs.psu.edu.

The Association for Computing Machinery plays a leading role as the representative society of the computing scientists. The majority of ACM's over 75,000 members are active participants in ACM's Special Interest Groups (SIGs), considered to be the best technical resource groups in the computing field. The SIGs focus on creating technical forums for the exchange of the latest research findings, technical notes, and other professional data, and on disseminating that information through refereed publications and technical conferences.

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7th Annual Symposium on Computational Geometry
June 10-12, 1991
Red Jacket Inn, North Conway, NH

Sponsored by ACM, The Association for Computing Machinery, the Special Interest Group ACT and GRAPH.

For further information contact: Scott Drysdale, Math and Comp. Sci., Dartmouth College, Hanover, NH 03755; (603) 646-2101; email: scot.drysdale@dartmouth.edu.

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This proceedings offers a survey of issues, techniques, and approaches for potential and current users of simulation tools and applications. Six sections: Distributed simulation; Networks/distributed computing; Multiprocessor/parallel processor systems; Artificial intelligence/simulation synergism; Analog simulation; Languages/tools. (Simultaneously published as *Simuletter*, Vol. *20*, No. 1.)
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January 1991 A publication of the
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- System Designs and Partitioning
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Dr. Ping Yang
Texas Instruments, Inc.
MS 369, P.O. Box 655621
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Phone: (214)-917-7901
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The IEEE Journal of Solid-State Circuits has been published for the past twenty-five years by the IEEE Solid-State Circuits Council on behalf of nine Groups and Societies within the IEEE. In response to an initiative from the Computer and Circuits & Systems Societies, the Council has authorized a series of special issues on microelectronic systems if the demand warrants. The intent is to establish a consistent forum for this field which unifies advances in many disciplines. Members of the sponsoring IEEE Societies may subscribe to this monthly journal for $14 per year. Contact IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08855-1331, Phone: 201-981-0060.

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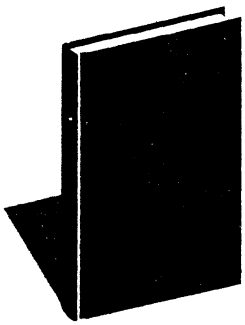

By Thomas Lengauer, Universitat Gesamthochschule Paderborn, West Germany

The last decade has brought explosive growth in the technology for manufacturing integrated circuits. The complexity of circuits is now so great that it forces the use of sophisticated mathematical techniques to optimise circuit designs with the aid of computers. Layout is an aspect of circuit design that involves a particularly large and interesting variety of difficult combinatorial problems.

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The book can be used as a text for graduate courses on circuit layout as well as on combinatorial optimisation. At the same time the book serves as a reference to experts in both fields.

CONTENTS: Part I - Background; Introduction to Circuit Layout; Optimisation Problems; Methods from Algorithmic Graph Theory; Methods from Operations Research and Statistics; Part II - Combinatorial Layout Problems; The Layout Problem; Circuit Partitioning; Placement, Assignment, Floorplanning; Global Routing and Area Routing; Detailed Routing; Compaction.

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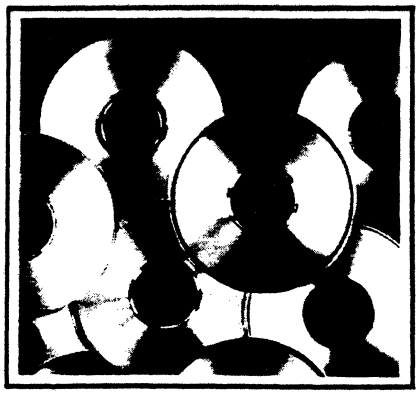

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