SIGDA NEWSLETTER

A Quarterly Publication of the Special Interest Group on Design Automation

VOLUME 20 NUMBER 2 OCTOBER 1990

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SPECIAL ICCAD CONFERENCE ISSUE
Attend the SIGDA Fall Meeting at ICCAD

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EDITOR'S NOTES

Welcome to the fall edition of the *SIGDA Newsletter*. This edition contains the minutes of both the Advisory Board meeting and the Summer General Membership meeting. These minutes contain good summaries of the state of the various projects of SIGDA. You should also note Franc Brglez' appointment as manager of the SIGDA Benchmarks project (see the Departments Section). Additionally, this issue contains the first edition of the SIGDA e-mail directory. It was drawn from the survey responses. If you want to be listed, just send in your survey form.

This edition has a collection of photos from the DAC including shots of the summer meeting, the lunch organized for the Eastern European students, Dr. Martin Wong's University Booth, our scholarship winners, and more. We are fortunate to have another article by Steve Meyer in this issue on wirability estimates. This newsletter can be a good place to publish articles and notes that would otherwise wait long periods in the queue for more formal journals. And that problem is likely to be further aggravated (read on).

Another DA publication, *High Performance Systems* (formerly - *VLSI Design*, and before that *Lambda*) folded this summer. You may have also heard that the IEEE's *Design & Test Magazine* will scale back its publishing frequency. Most certainly, this is an unpleasant trend, leaving the DA industry with an ever smaller bandwidth of interchange. We will all miss the feeling of community that *High Performance Systems* provided with its news, interviews, and editorials. And the fewer pages available in *D&T* will further slowdown the technical paper pipeline. If you have any insights on this problem (or perhaps a solution), please drop me a line. **THANK YOU...**

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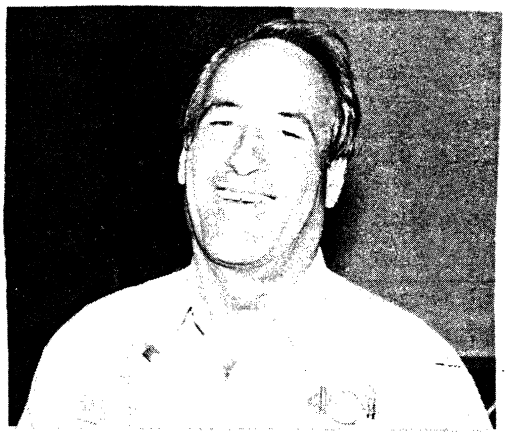
LETTER FROM THE CHAIR



SIGDA's premier event, DAC, came off in steamy Orlando last June in its usual grand style. In the opinion of most, it was the best DAC ever. Nevertheless, DAC cannot stagnate, or it will lose its preeminent position. A somewhat earlier start date, modification of its Sunday-Wednesday schedule, more tutorials, additional tracks of sessions devoted to the interests of groups other than developers are under discussion.

As one of DAC's sponsors, we put a modest amount of money each year into purchasing equipment to support DAC. Our sister organization IEEE-CS this year will purchase a UNIX computer, on which a truly effective email system can be mounted at DAC. SIGDA will purchase PCs for the press room, with different brands of word processing software familiar to the press corps. DAC itself will require the supplier of badge-making equipment to bring enough equipment on site to provide backup against the equipment failure which produced the long lines at registration this year.

The summer annual SIGDA membership meeting took place, again shared with DATC; see the minutes elsewhere. Your officers and board solicit your opinion on the format of these meetings. The range of SIGDA activities is now so large that meaningful discussions of alternatives and membership votes on directions and budgets isn't feasible. But a negative comment made to me seems valid criticism - the meeting has turned into a presentation by SIGDA's Board of its already made decisions. Give us your opinion - how do you want these meetings structured? We meet again at ICCAD - see the announcement elsewhere. Come, but also tell me or other Board members how to improve this meeting!

SIGDA's High School Scholarship program, under Charlotte Acken, draws universal praise. Eight winners are now in the program. Their entire college awards are in escrow, to be paid out as they succeed in their college programs. The program initiated in a suggestion from Pat Pistilli; its current success is due in large measure to the efforts put into it by Regina Pistilli whose salary was a donation from MP Associates. SIGDA is greatly indebted to them! We wish Regina all the success in her PhD studies.

Here is a chance for you to help this great project. Charlotte needs mentors from under-represented groups in our profession - women, hispanics, blacks, native americans, etc. SIGDA pays your expenses, we need your participation.

Bryan and Kathy Preas' CD-ROM project was a roaring success at DAC. Its demo at the University Booth was always crowded, the comments of its prototype evaluators significantly changed its format. This is SIGDA's major project, measured both in expenditure level and in our expectations of its impact on our profession. Get your CD-ROM reader plans ready for its availability next year!

The University Booth itself was thronged. Martin Wong and Mary Jane Irwin scheduled non-stop demos of university software. It was the meeting place for the whole university community. And this year its appearance was the equal of any vendor booth in its increased size, its furnishings and equipment, and of course in the large SIGDA banner. Most importantly, the research results demoed by the students were impressive; our profession shows no signs of stagnating!

To control the wide-ranging SIGDA activities, your Board now meets four times a year. SIGDA's FY91 budget is over three quarters of a million dollars, the equal of many a business. The group which gives up its weekends to control these activities deserves continued recognition. We have a vacancy now, Waldo Magnuson has retired and I am searching for a replacement to run our publications efforts. With talk of a Journal or other regular publication, this can be an important spot.

SIGDA will have elections next Spring. Dick Smith, our nominations chair, is now searching for candidates. Call him with your suggestions. Don't be modest, either, you can suggest yourself!

ACM's elections last spring produced a top level in ACM totally supportive of SIGDA and DAC. From John White down, the volunteer heads of ACM come from SIG backgrounds. At the same time, Joe Deblasi joined ACM as its executive director, and Pegotty Cooper hired Debbie Hall to handle SIG activities for the group of SIGs which includes SIGDA. Their assistance has already produced a DAC management contract renewal, breaking a long stalemate. Debbie in particular became immediately indespensible, I don't know how we ever functioned without her.

Paul Weil is a dynamo - look at the list of workshops! These include a number in Europe, and Jim Cohoon is working with Siemen's Egon Hoerbst in helping Eastern Europeans to hold one in Leningrad! Workshops are the cutting edge of technology, they complement the major conferences. Why don't you volunteer to Paul to lead a workshop? It's great for your reputation as well as being a service to our profession.

Pat Hefferan has started a new consulting business, yet he continues to provide us superlative newsletters. Look through this one - they just get better and better!

Hersh Loomis' graduate scholarship program drew an amazing number of high-quality applicants. A mailing made through Pat Hefferan to ALL graduate schools with possible candidate programs was partly responsible. Picking the winners which were announced at DAC,was a tough job. Library grants were awarded to those just missing the scholarships. One recipient was a Mainland China university. SIGDA is truly becoming world-wide.

Jim Cohoon handles an amazing number of requests for travel grants efficiently and fairly. This year, it included a project to bring potential Asian paper authors to DAC to help them understand the requirements for a paper to be accepted. His piece-de-resistance was the Eastern European project, seven CAD professionals were brought to DAC from Russia, Eastern German, Hungary, Poland and Czechoslovakia, each with a Western European companion to ease the travel and customs problems. I was thrilled to talk with them and find such dedication to a free society. Again Jim had the help of Egon Hoerbst. SIGDA thanks you!

Charles A. Shaw - Chairman SIGDA

September 1990

SIGDA ADVISORY BOARD MEETING MINUTES

The SIGDA Advisory Board Meeting was called to order by Chairman Chuck Shaw at 8:00 a.m. on June 23, 1990. Board Members in attendance were Gordon Adshead, Franc Brglez, Jim Cohoon, Pat Hefferan, Mary Jane Irwin, Michael Lorenzetti, Bryan Preas, Dick Smith, Ron Waxman, and Paul Weil. Also present were Debbie Hall (ACM), Kathy Preas (CD-ROM project manager) and Mark Mandelbaum (ACM Publications Board).

A. Welcome New Members

Chairman Chuck Shaw introduced Franc Brglez from MCNC, who is the new board member in charge of benchmarks. Chuck also introduced two visitors from ACM: Debbie Hall, who is now our liaison to headquarters and Mark Mandelbaum, who is from ACM publications and has joined the meeting to participate in the CD-ROM discussions.

B. CD-ROM

Kathy Preas presented the current status of the CD-ROM project (now called DALibrary). The prototype is now available and evaluation has begun. It runs on the IBM PC, the Apple MAC II and Sun workstation (the first database to run on all three). So far, PC problems are very minor. MAC users have a little problem getting started, but it works fairly well. The Sun version has numerous problems (the UNIX kernel must be rebuilt to use the system). Sun is working on correcting this.

The IEEE Circuits and Systems Society has given us permission to use their copyrighted material. FIZ Karlesruhe (a German interactive database company) is interested in putting our database on-line for their customers. Details are being worked out. Demos will be run in the ACM University Booths during the Design Automation Conference.

There is an evaluation meeting on Tuesday from 6-7:30 p.m. during the Conference, during which beta test users will discuss the system and suggest modifications for the production version. Some distribution issues are yet to be resolved.

The IEEE has been cooperative, receptive and encouraging, but not closely involved and have not yet committed to active involvement in distribution and support. Bryan Preas reminded the Board that he hopes to price DALibrary such that there is no return to SIGDA (this is a service to the profession). All costs, except support, are now fixed. Support costs are being worked out. The following table summarizes the costs for a single (nine CD) volume:

Pressing	$25
Packaging	$10-12
Royalties on retrieval engine	$70-100
Support	???
TOTAL	**~ $150**

Mark Mandelbaum reported on market forecasts made by ACM. Technical libraries are the biggest customers (rather than individuals). He estimates 1000-1200 sales (75% to libraries). Library grants specifically for CD-ROMs were suggested as a way to get the project going (1200 for ROM and drive). Current grant size is $1000.

MOTION** - Budget $30,000 to support library grants to universities for CD-ROM readers and ROMs, limit to one grant per university, $1500 maximum per grant.* ***(Weil, Hefferan, 10-0-1).

Bryan brought up the question of whether we can fund a person at ACM to handle support. There are often problems with installation and there are usage questions to be answered. There must be a number to call for assistance. Should this be RTI or ACM? We can fund the start-up of such a service at ACM to leverage them into the CD-ROM business. RTI is quoting $160,000 for this service. Mark has hired a full-time CD-ROM person at ACM to do marketing and support. Question is what happens if she becomes overloaded? Can we fund part-time back-up?

MOTION**: - Grant up to $100,000 to ACM as seed money for support of CD-ROM customers. **(Waxman, Weil, unanimous)

Preas presented a revised budget. Total spent so far is $696,222 (slightly over the budgeted amount of $668,000). The cost will grow to $794,222 if we add the ICCD proceedings.

MOTION** - The CD-ROM project stick with current budget and scope. **(Smith, Waxman, 9-2-0)

The Board expressed appreciation and congratulations to Bryan and Kathy Preas for a job well done.

C. DAC

Dick Smith reported that DAC pre-registration is up from last year. Some changes in format are in the works. Practical user track parallel to the regular Conference is one of the suggestions being discussed.

D. Travel Grants

Jim Cohoon reported that 110 travel grants were awarded for DAC alone. No food money was provided to recipients this year (registration, lodging and transportation only). This allowed more awards to be granted and doesn't seem to present a hardship to recipients. Jim asked for a budget increase for next year.

MOTION** - Increase Travel Grant budget from $125,000 to $150,000. **(Radke, Preas, unanimous)

Cohoon questioned whether we should require ACM membership on the part of travel grant recipients (as opposed to only SIGDA membership, as is the current policy).

MOTION** - That ACM membership be a requirement for travel grant recipients. **(Preas, Radke, 10-0-1)

E. Conferences

Paul Weil listed conferences and workshops in which SIGDA is involved. There are three conferences and seven workshops that we sponsor, co-sponsor or are "in cooperation with". Weil questioned whether we should require proceedings from our workshops. Does this stifle open interchange of ideas? After some discussion, it was decided to leave this to the discretion of workshop chairmen. However, it was agreed that a summary (for publication in the Newsletter) should include a technical overview and the workshop program.

F. New Journal

ACM Journal on Formal Methods wants $48,000 seed money to start the journal. Long term costs may be $150,000. This publication would be co-sponsored by SIGDA and SIGPLAN (who is putting in an equal amount of money). Is this too narrow of a topic to be a successful journal? Should we require a broader coverage of DA? Should ACM create a special interest group to cover this? Shaw pointed out that we need a replacement for Waldo Magnuson to manage the Textbook and Bibliography projects (under whose jurisdiction this kind of publication would fall). Shaw requested recommendations and several were made.

MOTION** - Recommend that Chairman Chuck Shaw find new board member to manage journals (along with textbooks and bibliography) and authorize up to $50,000 to initiate an ACM Journal which includes Design Automation as a topic. **(Weil, Radke, 9-0-2)

G. Benchmarks

Franc Brglez reported that FTP from MCNC works well. He presented a profile for benchmark distributions. He proposed a benchmark panel discussions at the next DAC. Franc was referred to Al Dunlop (DAC program chair) to discuss this further. Franc also reported on the MCNC International Workshop on Layout Synthesis, which was held last May. The workshop attracted over 100 attendees and a two-volume proceedings was distributed. The place and route benchmarks were enhanced and redistributed for this workshop. Next year

(1991) the topic is Logic Synthesis, 1992 will be Layout Synthesis again.

H. University Booth

Mary Jane Irwin reported that the booth is going well. Twenty universities will be demonstrating software this year, three of which are European. Five machines (three Suns and two DECstations) are in the booth. The total cost is approximately $71,000. Cohoon will be the organizer for 1991. It is time to designate a person for 1992.

I. Video Tape Project

Irwin reported that the first tape will be "An Introduction to DA" targeted at sophomore university students. Professor Richard Newton of UC Berkeley will be the speaker. The schedule calls for August production for fall course use. Adshead recommended that we provide tapes in European-compatible format. Irwin will investigate this through ACM distribution. A VHDL tutorial (joint with DATC) is also in the works. The speaker has not yet been identified. The maximum cost to SIGDA will be $20,000.

J. European Activities

Adshead reviewed the goals and policies of EDAC. They plan to continue to have an annual conference in March. This conference will have a moving European location. It is a non-profit, self-financing activity. They plan steady growth and increasing vendor presence. The intention is to act in harmony with U.S. DAC and emerging global scenario. They started with a $20,000 loan (which has since been repaid) and have netted a $35,000 profit from the 1990 conference (total cost for EDAC90 was $400,000). Paying attendance was 460. EDAC'91 will be in Amsterdam, EDAC'92 in Brussels and EDAC'93 in Paris.

K. DATC

Ron Waxman reminded the Board that the DATC Executive Committee will meet Monday evening at the Sheraton. Everyone is invited to this open meeting.

L. Publicity

Chuck Radke reported that the new brochures are included in the DAC handouts and will be available at all workshops. Shaw extended thanks on behalf of the Board.

M. Bulletin Board and Communications

Dick Smith reported that the News system is not being used. SIGDA traffic in the comp.lsi.cad newsgroup is very light How do we increase the interest in this service? DAC has had a DIN network for use by attendees in the past. This year there will also be a Sun network to do this. DAC is discussing installation of a UNIX machine to provide year-round DAC-related communications. Perhaps we can utilize this tool. No action taken.

N. DAC Contract

The DAC management contract is still in the works. Yet another final version is now ready for review. IEEE and ACM have agreed to it. It now goes back to the contract negotiation committee. Shaw pointed out that this board may need to become involved in the process if this version is not approved. (NOTE: the contract was approved and signed a few days following the meeting - MJL.)

O. Next Board Meeting

After some discussion, it was agreed to hold the next Board Meeting in conjunction with ICCD in September in Cambridge, Mass. Shaw will make arrangements and inform the committee.

At this point Chairman Shaw adjourned the meeting.

Respectfully Submitted,

Michael J. Lorenzetti
SIGDA Secretary/Treasurer

SIGDA MEMBERSHIP MEETING MINUTES

The SIGDA Membership Meeting was called to order by Chairman Chuck Shaw on June 24, 1990 at 7:10 p.m. Approximately 150 members were in attendance.

A. DA Library

Bryan Preas reviewed the project and informed attendees that they could view a prototype version at the ACM and University Booths. The final version will contain 35,000 pages on 8-9 CD-ROMs. This is the first CD-ROM database to support three different platforms (Sun, Mac and IBM PC). The final version will be available from the IEEE and ACM publication departments in early 1991.

B. University Booth

Mary Jane Irwin reviewed the University Booth Activities. This year's Booth is 30 X 45 (compared to last year's 20 X 20). Twenty universities are participating (three of which are European). There are five workstations (three Suns and two DECstations) in the booth. Jim Cohoon will be next year's university booth organizer.

C. Workshops

Paul Weil reviewed the conference and workshop schedule. The three main conferences are DAC, ICCAD and EDAC. ICCAD (the International Conference on Computer-Aided Design) is in its sixth year. Last year it attracted over 1000 attendees. A total of 124 papers have been accepted for the coming year's conference (in November), which will be in Santa Clara, California (as it has been every year).

EDAC (the European Design Automation Conference) was held "in cooperation with" SIGDA. Jochen J.A. Jess reviewed the conference. EDAC evolved from a CAVE workshop. The first conference was held in Glasgow last March. There were 450 paid attendees, and 600 participants overall. Next year it will be held in Amsterdam and they expect 700-800 participants. Seven workshops are being supported (at least partially) by SIGDA. Weil introduced representatives from each of them to tell the members about the workshops.

Rick McGeer discussed the ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (tau 90). It will be held August 15-17, 1990, in Vancouver. The workshop covers all aspects of timing. Forty-five papers have been submitted, 25 were accepted. Proceedings will be made available for attendees only. Each session will feature twenty-minute presentations followed by a panel discussion of the speakers in that session.

The Workshop on Logic Level Modeling for ASICs was discussed by Rob Mathews. It is attended by people involved in modeling, simulating and using ASICs. The first workshop was held December 3-5, 1989 and had 30 attendees. (See the June 1990 SIGDA Newsletter for the conference summary.) The next one is scheduled for August 12-14, 1990 in Monterey. It will have largely the same format. An announcement for the upcoming workshop also appears in the June 1990 Newsletter.

Ron Waxman discussed the Workshop on EDA Frameworks in Charlottesville, Virginia, November 26, 1990 (SIGDA and DATC are both working "in cooperation with" this IFIP workshop).

Waxman also talked about CHDL '91 (another IFIP workshop), which will be held in April 1991, in Marseille France, and is also "in cooperation with" SIGDA.

The workshop on Formal Methods in VLSI Design to be held January 1991 in Puerto Rico was discussed by P.A. Subrahmanian. The workshop is intended to bridge traditional CAD to those interested in formal methods.

The Workshop on High Level Synthesis was discussed by Raul Camposano. It will be held in Black Forest, West Germany, on March 3, 1991.

The International Workshop on Logic Synthesis, was discussed by Franc Brglez of MCNC. A similar workshop is held each year in Research Triangle Park, North Carolina, "in cooperation with" SIGDA (last year's topic was layout synthesis). SIGDA provides funding for benchmark development and distribution support. The next one will be held May 7-10, 1991 and will have special emphasis on sequential logic synthesis. The workshop typically attracts 100+ attendees. Weil summarized the workshop program and the support that SIGDA offers in terms of proposal development, organization (including site selection, budgets and timeline of activities leading up to the meeting). He encouraged those with ideas for other workshops to contact him at the address which appears inside the front cover of the Newsletter.

D. Newsletter

Newsletter Editor Pat Hefferan reminded members that one of the membership benefits is the reduced rate for VHDL Manuals, EDIF Manuals, 25 Years of Design Automation, Proceedings of ICCAD and DAC which are available using the coupons printed in the Newsletter. He asked members to participate in the membership survey printed on page 13 of the June issue. Preliminary results say that 81% of the respondents are US citizens, 44% are from industry, and 72% have email addresses.

E. High School Scholarship (ASCEE)

Charlotte Acken informed the members that the program is in its second year. ASCEE awards undergraduate scholarships to underepresented minorities in computer science and EE fields. Last year the program was held in Las Vegas (the site of last year's DAC). Four high school juniors were selected as finalists. Two of these (Maria Nolasco and Kim Dinks) were selected as winners of $4000/year renewable scholarships. Jon Duran received a one-time only $1000 scholarship. The fourth finalist elected not to pursue a career in the computer science or EE fields, and thereby became ineligible to receive an ASCEE award.

This year the scholarship is being conducted in the San Francisco area. It was decided that having the scholarship follow the DAC each year, as originally planned, is too cumbersome to manage effectively. San Francisco was chosen because it has a large number of DA professionals available to serve as mentors. The program will again award two $4000 per year renewable scholarships and two $1000 one-time only scholarships. The winners will be introduced at the keynote address at DAC. Charlotte expressed her thanks to Regina Pistilli for founding program.

F. Travel Grant Program

Jim Cohoon reviewed the travel grant program which has an annual budget of $125,000. This year there were 150 awards made. Roughly half of the budget goes to DAC attendees. A total of 110 students and professors traveled to DAC this year under the program. They represented 15 countries and 49 universities. Six awardees were Eastern Europeans.

G. Graduate Scholarships

Chuck Shaw reported for Herschel Loomis. A total of 10 graduate scholarships were awarded during the DAC general sessions. Library grants were awarded to all proposals which were not fully funded.

H. Awards

Charles Radke presented the SIGDA service awards for this year. The SIGDA service

awards were started in 1986 to recognize outstanding efforts of SIGDA volunteers. Two of the $500 awards are given each year and no more than one can be from the current Advisory Board. This year's recipients were Fred Hinchliffe (for instituting the travel grant program) and Bryan Preas (for the CD-ROM project and serving as vice-chairman). Radke also presented plaques to last year's recipients: Michael Lorenzetti and Scott Baeder.

I. Video Project

Mary Jane Irwin reported that the first SIGDA funded video will be Introduction to Design Automation by Richard Newton of UC Berkeley. The targeted audience is sophomore college students. The video is expected to be ready for fall distribution.

At this point the meeting was adjourned.

Respectfully Submitted,

Michael Lorenzetti
SIGDA Secretary/Treasurer

MEMBERSHIP BENEFITS

As a special benefit to SIGDA members, certain standards manuals, proceedings, and other documents of general interest will be made available at a nominal rate. Availability of the documents may vary, so allow several weeks for delivery. Proceedings will only be issued after the conference sales have been satisfied. ***You must be a member of SIGDA to quality.***

MEMBERSHIP COUPON - DOC.

-SIGDA Membership Sponsored Manual/Proceedings -

Name _____

Address _____

_____

_____

_____

ACM Membership Number _____

SELECTIONS (please check box(es))

- ☐ EDIF 2.0.0 Standards Manual
- ☐ VHDL Language Reference Manual
- ☐ 25 Years of Electronic Design Automation
- ☐ 1990 DAC Proceedings
- ☐ 1990 ICCAD Proceedings

Please include a check for $5.00 (made out to ACM/SIGDA) to cover the cost of shipping. ($5.00 per document). Please allow several weeks for shipping and handling. DAC & ICCAD Proceedings mailed only after conference is over. Also, allow extra time for EIA EDIF Publications.

Please send coupon to:
Patrick M. Hefferan
1681 Princeton Avenue
St. Paul, MN 55105

SIGDA MEMBERSHIP SURVEY

In order to better serve the SIGDA membership, we are taking a survey of your wants and needs. Please take a few minutes to fill out the survey form on the next page and send it in. It has a preprinted address on the back, so just cut it out and fold it up with the address facing outward. Then tape (please do not staple) it shut and mail it in. You will need to provide 25 cents postage, as we cannot use our bulk mailing permit for this.

To make this more interesting and provide an incentive to get the surveys filled out, those who participate will be eligible for a drawing for a portable, electronic address book. We want to hear from you - so take a few minutes and fill it out. THANK YOU!!

PLEASE FILL OUT AND SEND IN ---------->

THE WINNER OF THE ELECTRONIC ADDRESS BOOK THIS QUARTER IS DEBABRATA SARMA FROM CINCINNATI, OHIO!! THERE WILL BE ANOTHER WINNER ANNOUNCED IN THE NEXT SIGDA NEWSLETTER.

SIGDA SURVEY
January, 1990

This is a general membership survey.
Participants will be entered in a drawing for an electronic address book.

Name _____ EMAIL Address _____
(May we publish this address? _____)

Address _____ Company _____

_____ Occupation _____

_____ Job Function _____

Phone - Home _____ Education _____
(Highest attained)

Work _____

_____
(Signature)

How long have you worked as a DA professional? _____

Computers used in work _____

Do you have a PC at home? _____ If yes, what kind _____

Do you have a modem? _____ *At home?* _____ *At work?* _____ *Speed?* _____

Are you connected to a network (Arpa, CIC, INTERNET?) _____

In what professional societies are you a member? _____

_____

What CAD/CAE functions are you responsible for?

_____ Schematic capture	_____ Simulation	_____ Layout
_____ DRC	_____ Test	_____ Management
_____ Design	_____ Specification	_____ Evaluation
_____ Mechanical	_____ Other _____	

What additional benefits would you like from SIGDA?

_____ DAC Proceedings	_____ DAC/ICCAD Admissions
_____ ICCAD Proceedings	_____ Network Access for EMAIL/BBS
_____ Standards Manuals	_____ Continuing Education _____
_____ Tutorial Tapes	_____ Other _____
_____ CD-ROM Tapes	

Would you pay extra for them? _____ *Yes* _____ *No*

The SIGDA High School Student Mentor Program is designed to increase under-represented groups in the DA profession. The target groups for this program are: Hispanic, Black, Women (all races), Disabled, and American Indian. We are requesting that the Mentors be from the target groups. Also, for administrative purposes, the Mentors must be from the San Francisco Bay Area. For further details, contact Charlotte Acken (address on front cover).

Would you like to be a Mentor? _____ *Yes* _____ *No*

Of which target group are you a member? _____

put 25 cent
stamp here

SIGDA Membership Survey
c/o Patrick M. Hefferan
1681 Princeton Avenue
Saint Paul, Minnesota 55105

SIGDA EMAIL DIRECTORY

Listed below are the EMAIL addresses taken from the Membership Survey. Please check your address and advise us of any changes - either by an EMAIL message[1], a short note, or simply send us the Survey form with a "revised" notation at the top. Drop us a message if you would like to be included in this directory.

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Departments

The following pages contain updates and information about various projects and activities funded by the SIGDA. Contact information (e-mail, phone, and addresses) for the individuals directing the programs can be found on the inside front cover.

Workshops/Conferences ..... Paul B. Weil

SIGDA sponsors many Workshops and Conferences in the Electronic CAE/CAD arena. During 1990 and 1991, SIGDA will either sponsor cosponsor or work in cooperation with other professional societies on 20 professional meetings. Please watch the newsletter for announcements.

We are always developing new Professional Activities to meet the needs of our 2000+ membership. SIGDA does its utmost to assist the organizing committees through comprehensive support activities. For the smaller meetings, SIGDA funds ACM and others who provide direct assistance with: site selection, budgeting, advertisement, and registration. This leaves the organizers with time to develop a superior technical program.

If you would like to propose a Conference or Workshop, you need only to prepare a two page summary of: The Meeting's Technical Objectives, Background of this and similar meetings on this Subject, Potential Locations and Dates, Meeting Size and Format, and the Organizing Committee and brief background of Chairpersons. This should be e-mailed to the SIGDA Workshop and Conference Chair Dr. Paul Weil at *weilcad@frith.cs.psu.edu*

SIGDA SPONSORED CONFERENCES, SYMPOSIUM, AND WORKSHOPS APPROVAL PROCESS

1. PROPOSAL: Two page Summary of:

   The Meeting's Technical Objectives
   Background of this and similar meetings on this Subject
   Potential Locations and Dates
   Meeting Size and Format
   Organizing Committee and brief background of Chairpersons

2. INITIAL ORGANIZATION: ACM will assist the Committee with:

   Site Selection
   Budgets
   Timeline of Activities leading up to the Meeting

3. MEETING BETWEEN ACM/SIGDA REPRESENTATIVE AND CHAIRPERSON(s)

4. FORMAL APPROVAL BY SIGDA

5. SIGDA WILL ARRANGE FOR ACM TO PROVIDE ASSISTANCE IN:

Local Arrangements
Call of Papers/Participation
Registration
Advanced Program
Publications
Onsite Registration
Post Conference Accounting

The ACM/SIGDA encourages the organizers to consider in-cooperation or co-sponsorship with other Professional Societies (ACM/SIGDA has a close working relationship with the IEEE as well as other Electronic Engineering Societies).

AFTER THE MEETING

IMMEDIATELY FOLLOWING THE CONF/SYMP/WORKSHOP hold a meeting that will discuss future events and seek volunteers to run these events.

STATUS REPORT: Within a few days of the Meeting transmit to SIGDA a brief status report including the meeting's attendance, financials, how the meeting met its technical objectives and any outstanding problems that may have developed.

MEETING SUMMARY: Within a few Weeks of the Meeting provide a 5 to 10 page Summary (see the June 1990 Newsletter pp 129-135 for a good example) of the meeting's activities for publication in the SIGDA Newsletter along with plans for future events. Emphasize the Technical aspects of the CONF/SYMP/WORKSHOP.

COPIES OF PROCEEDINGS: Any Proceeding or Digest of the material presented at the Meeting should be available to SIGDA Members. Five copies should be mail to SIGDA as soon as they are available. Arrangements must be made to assure that a quantity of proceedings can be purchased by SIGDA Members.

Outstanding Member Recognition .....Charles A. Radke

Since January of 1971, SIGDA has been in continuous operation, and over these 15 years has steadily increased its influence on the Design Automation profession. It, therefore, appears fitting that SIGDA recognize those members who have given so much of themselves to the SIGDA organization, to the members, to its newsletter, and to the sponsored technical functions (e.g., conferences, workshops, and symposia).

The award is given annually and is presented at the Design Automation Conference. It consists of a plaque plus $500. No more than two are given in a year, and none are awarded if no appropriate candidate is felt to exist.

A committee of four including the SIGDA Advisory Board Person responsible for Outstanding Member Recognition selects the award winners from nominations received from the SIGDA membership. The nominations must be in by 3/15 with a decision by 5/15 of that same year.

The awards for the past five years were:

1986 Richard C. Smith & Charles E. Radke
1987 Robert Smith & Waldo G. Magnuson, Jr.
1988 Charles A. Shaw & Luther Abel
1989 Michael J. Lorenzetti & D. Scott Baeder
1990 Frederich Hinchcliffe & Bryan T. Preas

If you have a nomination for the upcoming 1991 year, please send it to me (my address is on the front cover). Please state the reasons for your nomination.

Benchmark Development & Distribution ..... Franc Brglez

Mr. Brglez has recently taken over the management of the SIGDA sponsored benchmark series from Michael Lorenzetti. Mr. Brglez is at the Microelectronics Center of North Carolina. His report follows:

An unknown number of benchmarks have been obtained from MCNC anonymously via ftp copies over the Unix network. Also, a total of 46 tapes and printed versions were distributed to 14 foreign countries and the US between January 1 and June of 1990. See the distribution profile below for detail.

BENCHMARK	Requests Filled
MODGEN89	1
Logic Synthesis 89	5
PNR88	2
COMPACT87	0
ISCAS85	7
ISCAS89	7
High Level Synthesis	0
Layout Synthesis90	14
All Benchmarks	10

I plan to approach the program chair of next year's DAC about having a panel session on benchmarks. Please contact me at *(919) 248-1925* or e-mail at *brglez@mcnc.org* for further details about the SIGDA sponsored benchmark program.

University Booth Project ..... Martin Wong (Mary Jane Irwin 1989)

This is the third year that the SIGDA has sponsored the University Booth at the DAC. This year's booth was the largest yet, measuring 30' x 45', and was equipped with five workstations.

Twenty universities demonstrated their research programs and work of their graduate students. Also, the SIGDA's CD-ROM prototype (running on a Sun workstation) was demonstrated at the University Booth.

James Cohoon will be taking over the University booth project for next year's DAC. Below is a schedule of the demonstrations at the 1990 DAC.

SUNDAY

TIME	Sun 4/60 **panda**	Sun 4/60 **uci_cad**	Sun 4/110 **frith**	DECstation 3100 **washoe**	DECstation 3100 **hydrus**	MISC
4:00 to 5:00	ATPG *test generation* Virginia Tech	SLAM/LES *layout synth* UC Irvine	slicer/splicer *schdl, connctvty* Penn State	BLIS *behav to logic* UC Berkeley	PEW/FABRICS *proc/device sim* CMU	
5:00 to 6:00	BTG *test generation* Virginia Tech	MILO/VSS *optmz, synth* UC Irvine	ivf2glue *machine synth* Penn State	SLIP *partitioning* UC Berkeley	COSMOS *switch level sim* CMU	
6:00 to 7:00	CHAMP *logic fault sim* Illinois	BIF/EXEL *behavioral synth* UC Irvine	SDE *o-o design env* Michigan State	VOV *design managmt* UC Berkeley	SAW *behavioral synth* CMU	

MONDAY

TIME	Sun 4/60 **panda**	Sun 4/60 **uci_cad**	Sun 4/110 **frith**	DECstation 3100 **washoe**	DECstation 3100 **hydrus**	MISC
10:00 to 11:00	ATPG *test generation* Virginia Tech	DSUI *user interface* TU Delft	ivf2glue *machine synth* Penn State	EDIF/CFI *EDIF tools* UC Berkeley	VLASIC *yield sim* CMU	GALAXY *design env* Wisconsin
11:00 to 12:00	CHAMP *logic fault sim* Illinois	DSUI *user interface* TU Delft	factorII/tvg *ml logic synth* Penn State	MIS *multilevel synth* UC Berkeley	HITEC/PROOFS *test gen, f sim* Illinois	GALAXY *design env* Wisconsin
12:00 to 1:00	ICE *incremental sim* Illinois	SLAM *layout synth* UC Irvine	artistII *layout synth* Penn State	SLIP *partitioning* UC Berkeley		GALAXY *design env* Wisconsin
1:00 to 2:00	SYLON *logic net synth* Illinois	MILO *logic optmz* UC Irvine	SDE *o-o design env* Michigan State	BOLD *X win interface* Colorado	PEW/FABRICS *proc/device sim* CMU	
2:00 to 3:00	ASYL *std cells synth* INP Grenoble	VSS *behavioral synth* UC Irvine	a.out *sizer* UC Santa Cruz	BLIS *behav to logic* UC Berkeley	MICON *SBC prototyping* CMU	
3:00 to 4:00	OESIM *high level sim* Washington	BIF/EXEL *behavioral synth* UC Irvine	a.out *sizer* UC Santa Cruz	EDIF/CFI *EDIF tools* UC Berkeley	HITEC/PROOFS *test gen, f sim* Illinois	Modeler's Asst *VHDL generator* Virginia Tech
4:00 to 5:00	WIREC *framework* Washington	UCI Tools *misc* UC Irvine	hdtv *timing verifictn* Pittsburgh	OLYMPUS *vertical synth* Stanford	SAW *behavioral synth* CMU	Modeler's Asst *VHDL generator* Virginia Tech
5:00 to 6:00	OESIM *high level sim* Washington	UCI Tools *misc* UC Irvine	TimberWolf *placemt, routing* Yale	VOV *design managmt* UC Berkeley	minTC *optimal clock* Michigan	Modeler's Asst *VHDL generator* Virginia Tech

The ACM SIGDA CD-ROM Project is also exhibited in the University Booth

27th DAC University Booth

TUESDAY

TIME	Sun 4/60 **panda**	Sun 4/60 **uci_cad**	Sun 4/110 **frith**	DECstation 3100 **washoe**	DECstation 3100 **hydrus**	MISC
10:00 to 11:00	ASYL *std cells synth* INP Grenoble	NELSIS *CAD framework* TU Delft	hdtv *timing verifictn* Pittsburgh	SIS *seq ckt synth* UC Berkeley	minTC *optimal clock* Michigan	SPARK *test gen, diagns* Case Western
11:00 to 12:00	CHAMP *logic fault sim* Illinois	NELSIS *CAD framework* TU Delft	slicer/splicer *schdl, connctvty* Penn State	OLYMPUS *vertical synth* Stanford	SAW *behavioral synth* CMU	SPARK *test gen, diagns* Case Western
12:00 to 1:00	BTG *test generation* Virginia Tech	VSS *behavioral synth* UC Irvine	ivf2glue *machine synth* Penn State	BLIS *behav to logic* UC Berkeley	PEW/FABRICS *proc/device sim* CMU	SPARK *test gen, diagns* Case Western
1:00 to 2:00	ATPG *test generation* Virginia Tech	BIF/EXEL *behavioral synth* UC Irvine	factorII/tvg *ml logic synth* Penn State	BOLD *X win interface* Colorado	VLASIC *yield sim* CMU	
2:00 to 3:00	ICE *incremental sim* Illinois	SLAM *layout synth* UC Irvine	artistII *layout synth* Penn State	VOV *design managmt* UC Berkeley	COSMOS *switch level sim* CMU	
3:00 to 4:00	BTG *test generation* Virginia Tech	BIF/EXEL *behavioral synth* UC Irvine	TimberWolf *placemt, routing* Yale	MIS *multilevel synth* UC Berkeley	Architectural Synthesis CMU	CATHEDRAL-II *DSP Si compiler* IMEC Leuven
4:00 to 5:00	ASYL *std cells synth* INP Grenoble	SPACE *3D verification* TU Delft		SIS *seq ckt synth* UC Berkeley	MICON *SBC prototyping* CMU	CATHEDRAL-II *DSP Si compiler* IMEC Leuven
5:00 to 6:00	SYLON *logic net synth* Illinois	SPACE *3D verification* TU Delft	a.out *sizer* UC Santa Cruz	OLYMPUS *vertical synth* Stanford	minTC *optimal clock* Michigan	CATHEDRAL-II *DSP Si compiler* IMEC Leuven

WEDNESDAY

TIME	Sun 4/60 **panda**	Sun 4/60 **uci_cad**	Sun 4/110 **frith**	DECstation 3100 **washoe**	DECstation 3100 **hydrus**	MISC
10:00 to 11:00	ICE *incremental sim* Illinois	UCI Tools *misc* UC Irvine	TimberWolf *placemt, routing* Yale	SLIP *partitioning* UC Berkeley	HITEC/PROOFS *test gen, f sim* Illinois	JUNE *placer, router* Minnesota
11:00 to 12:00	SYLON *logic net synth* Illinois	VSS *behavioral synth* UC Irvine	ivf2glue *machine synth* Penn State	OLYMPUS *vertical synth* Stanford	minTC *optimal clock* Michigan	JUNE *placer, router* Minnesota
12:00 to 1:00	WIREC *framework* Washington	BIF/EXEL *behavioral synth* UC Irvine	hdtv *timing verifictn* Pittsburgh	BOLD *X win interface* Colorado	Architectural Synthesis CMU	JUNE *placer, router* Minnesota
1:00 to 2:00	OESIM *high level sim* Washington	MILO/SLAM *optmz, synth* UC Irvine	factorII/tvg *ml logic synth* Penn State	EDIF/CFI *EDIF tools* UC Berkeley	MICON *SBC prototyping* CMU	
2:00 to 3:00	WIREC *framework* Washington					

The ACM SIGDA CD-ROM Project is also exhibited in the University Booth

DAC Photos

Following are photographs of the 27th DAC including the Summer SIGDA Meeting and associated activities.

Entrance to the 27th DAC Exhibit hall and Conference Rooms

Martin Wong, this year's SIGDA University Booth Manager, and Mary Jane Irwin, last year's Booth Manager, stand in front of their creation

A conference attendee talks with an exhibitor from the University of California at Irvine in the SIGDA booth.

Luncheon for SIGDA-Sponsored Eastern European Students

The SIGDA sponsored travel and DAC attendance for six students from Eastern European countries. They were paired with Western European students who acted as mentors.

Jim Cohoon organized the travel and arrangements for the Eastern Europeans, and set up a luncheon for them and their mentors.

SIGDA High School Scholarship Program

The SIGDA provides a scholarship to under-represented groups in the engineering field. The recipients were invited to the DAC in Orlando and attended the DAC functions as well as Disney World.

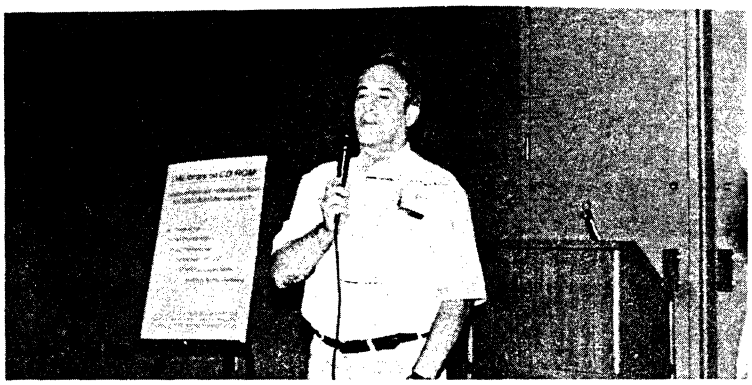
Charlotte Acken administers the SIGDA High School Scholarship program.

Maria Soledad Ochomongo and Raul Alberto Ortega, Jr.

Christopher Ray Silva and Tessa Helena Wilbert.

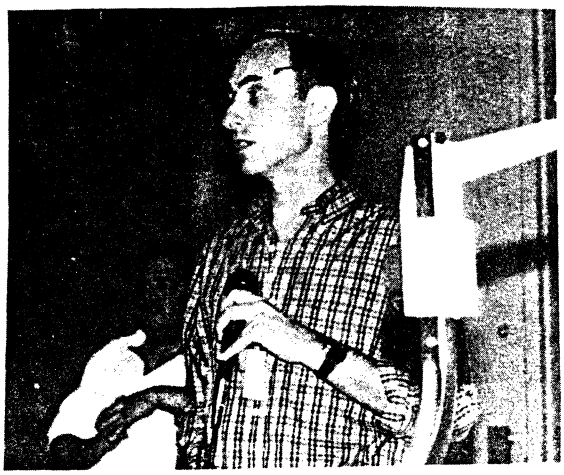
SIGDA Summer Meeting (1990)

The annual general membership meeting of the SIGDA was held at the Orlando Convention Center. Summaries of the major SIGDA projects and workshops were presented.



Chuck Shaw, Chairman of SIGDA, opens the annual summer meeting of the ACM/SIGDA

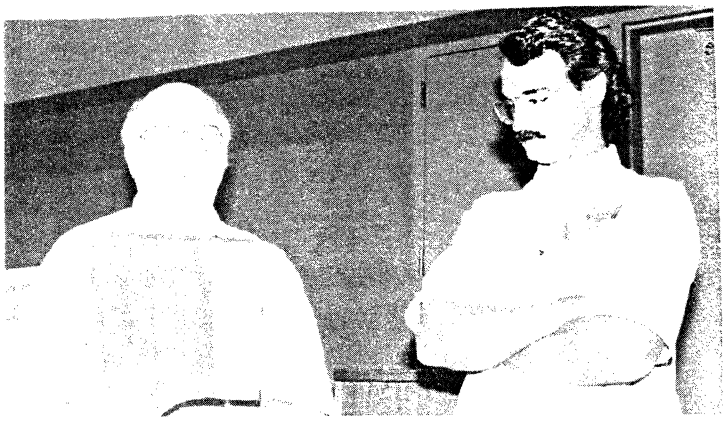
The crowd mills around the food and refreshment table before the SIGDA meeting.



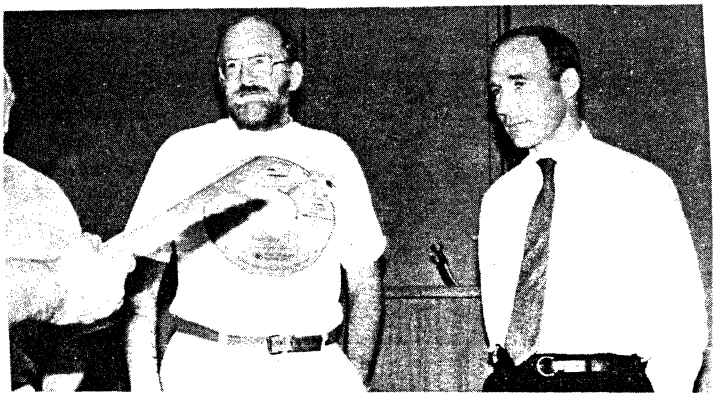
Rob Matthews reports on the successful ASIC modelling workshop held this Spring.

SIGDA Outstanding Member Awards

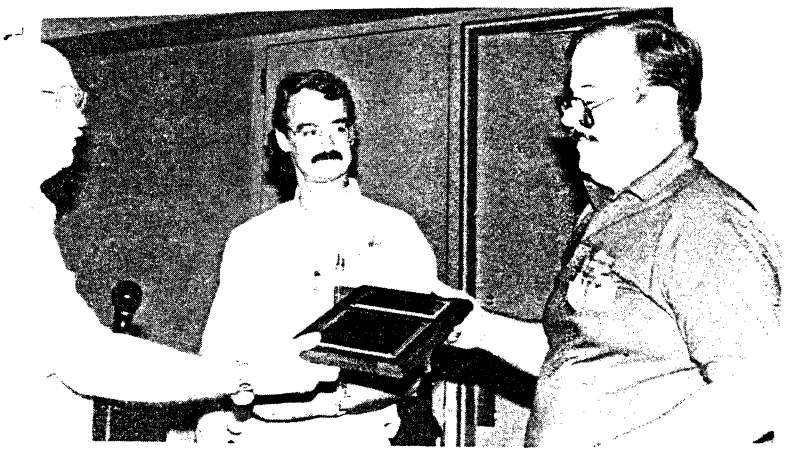
The SIGDA recognizes outstanding members who have made significant contributions to the society and the DA profession. Charles Radke is the board member in charge of this award. Awards for both 1989 and 1990 were presented at this year's DAC.



Chuck Radke presents the award to Michael Lorenzetti, SIGDA Secretary-Treasurer



Chuck presents awards to Bryan Preas, SIGDA Vice Chairman and director of the CD-ROM Project, and to Fred Hinchcliffe, the former SIGDA Travel Grants Director.



Chuck presents the award to D. Scott Baeder, the former Newsletter Editor.

A New Placement Level Wirability Estimate with Measurements

Steve Meyer

Pragmatic C Software
220 Montgomery Street, Suite 925
San Francisco, CA 94104

Abstract: An extension of the wirability estimate concept to master slice placement is presented. This estimate is usable on individual circuits, produces detailed wire requirement maps, but requires target designs to be at least partially placed. The main innovation is the discovery of an outer rectangle estimate that separates basic wire requirements from routing details. The estimate averages wires within one chip but is inapplicable to chip type wire space modeling. Steiner tree net decomposition, the half perimeter wire length estimate, and potential wire requirement reduction from a third metal layer are evaluated.

1. Introduction

Just as approximate device models are necessary during logic design, approximate wirability estimates assist in layout system development. Once the decision to improve a layout system is made, it is often difficult to identify the part of the system most in need of improvement. This paper describes a new wirability estimate usable during and after placement on master slice based semicustom ICs. A master slice based IC is either a gate array or standard cell circuit organized as fixed length cell rows separated by wiring channels with two perpendicular metal wiring layers. Vertical feed thrus are used for cross row connections [18] [29].

The estimate produces detailed chip maps that can be used to determine if congested regions are caused by the placement or by the routing part of a layout system. It can be used on automatically or manually placed designs at any placement stage. The idea behind this estimate is to compute a very simple global routing. It measures placement wire requirements independent of channel router efficiency and independent of congestion versus wire length trade offs made by global routers (see [14] for example).

Three basic estimate matrices are computed. One measures the number of horizontal wires running along each wiring channel at every wire grid. Another measures the number of vertical feed thru wires crossing every active row at every grid. The third measures the vertical wiring channel crossing wires. The three computed matrices are used to produce wire requirement maps and to compute global statistics. The estimate is called "outer rectangle" because 1/2 wire is added to the value (row or channel wire number) for all four sides of the bounding rectangle determined by each two point connection. Every signal net is decomposed into pin pairs by computing the minimum spanning tree (MST) on the complete graph corresponding to each net. The outer rectangle wire segments are treated as if every channel and every feed thru grid had "infinite" capacity.

Exact chip totals such as total substrate wiring channel track demand or total row feed thru requirements can be computed. The total is exact because even though fractional wires are used, the totals are exact after division by two. In this paper the estimate results are interchangeably called maps, the output form, arrays, the storage form, or matrices, the conceptual form.

1.1 Relation to Other Wirability Estimates

The estimate is related to standard wiring capacity demand matrices (see [2] for example) but requires only placement level circuit data base information and produces more detailed (fine grain) measurements for each placement. It is also slightly related to the placement evaluation scheme described by Shiraishi and Hirose[26], but does not use net cut crossing counts and is able to predict feed thru requirements. The outer rectangle estimate is complementary to the standard statistical chip wirability (chip type wiring space requirements) work [3] [5-6] [8] [10-11] [30-31]. It is also related to transistor area evaluation metrics [25]. Measurements from the circuit maps can be used to validate wirability models. The estimate should perhaps be called circuit or even circuit region specific wirability. Statistical validation of this estimate is meaningless since it simply measures important

layout parameters. The simplifying assumptions have proven in practice to balance accuracy against programming ease and resource utilization.

1.2 Relation to Global Routing

In a sense this estimate is an abstracted global router. However, it can be used on partial placements because data from the routing part of the circuit data base is not required. A real global router needs to know exactly which feed thru grids are blocked, and where to add extra feed thru cells for standard cell layouts. Exact horizontal channel entry points need to be determined before a standard channel router can be used. Papers by Lee [14] and Rose [23] describe global routers that also break nets into pin pairs using an MST calculation and then search for a path connecting the pin pair minimizing some evaluation function. The outer rectangle estimate introduced here uses the best routing path assuming no interference from other connections. If a one bend route is possible, it will cause the least additional congestion. This idealized estimate is preferable for placement evaluation since it is unaffected by router implementation details [20] [17].

2. Estimate Description

2.1 Matrix Dimensions

The vertical row feed thru matrix (called **vrow**[][] below) has dimension R by G+2 where R is the number of rows and G is the wire grid number per per row. Every wire connecting to or feeding thru a row is added to its grid row location. For the purpose of including signal nets connecting I/O pads to the master slice area, I/O pads are assumed to be located at the real substrate wire grid and row closest to the lower left pad corner in a "virtual" row or grid just outside the master slice area. I/O pad location is not particularly important, but it is valuable to include wire segments connecting to I/O pads that lie inside the master slice area.

The horizontal channel congestion matrix (called **hchan**[][] below) has dimension R+1 by G+2. The channel corresponding to a row is by convention immediately above it. This means an extra matrix row is needed immediately below the bottom row. Notice the channel immediately above and the channel immediately below the master slice area are included in the output map. The vertical channel feed thru matrix (called **vchan**[][] below) has dimension R+1 by G+2 and includes wires crossing a channel. Such wires may cause problems for a channel router.

2.2 Algorithm

To compute the outer rectangle matrices first decompose all nets into N-1 two point connections (assume the size of a net is N). The minimum spanning tree (MST) of the complete graph of N points is the best decomposition. See section 5 for a discussion of the various problems encountered in attempting to use one easy to compute L-shape Steiner tree decomposition method. The distance metric should be the sum of the rectilinear matrix row and column distances. When connecting to a pin from below, the pin should be treated as if it were located on the bottom of its row. When connecting from above, the pin should be treated as if it were on top.

Next add each pin pair to the three arrays in any order. Add one to each array location crossed by the wire segments required to connect the MST pin pair. The outer rectangle estimate assumes a pin pair connection is made with four wires coincident with the four rectangle sides determined by the two points. After all connections have been added to an outer rectangle array, each array value is divided by two because each pin pair is connected twice and because only one wire will actually connect the pin pair.

There are three different possible connection configurations: a connection crossing at least two wiring channels, a connection crossing exactly one wiring channel, and a connection extending horizontally along one cell row crossing no wiring channel. For each connection type both the vertical and the horizontal wire matrices must be updated (see figures 1-3). Two aspects of the updating must be treated carefully. For wires crossing at least one channel, the channels closest to the rectangle center must have their counts incremented. When both pins connect to grids along the same vertical line, the rectangle degenerates into two coincident lines. Each crossed grid and channel must be incremented by two.

3. Implementation Details

3.1 MST Pin Data Structure

Assuming a circuit is stored according to the data structure scheme described in [16], the following C Programming Language [13] pin data structure can be used to decompose one signal net into N, MST pin pairs (one pin element will be the root and have no connecting pin):

```
struct pintab_t {          /* place for one MST edge */
 struct type_pin_t *ptpin; /* the pin's type data */
 struct coord_t pt;        /* pin (grid, row) coordinates */
 int ndist;                /* current ptr to partial MST distance */
 struct pintab_t *nrnod;   /* current nearest node */
 struct coord_t nrpt;      /* nearest pin coordinates */
};
struct pintab_t pintab[MAXNETSIZE];
```

The MST is stored so that each element points only to the coordinates of its tree parent. This is sufficient to determine pin pairing since tree topology is not needed.

3.2 MST Function

The following in place implementation of Prim's algorithm [21] can be used to compute the MST for one net (pointed to by parameter **np**). It assumes the **pintab**[] array is filled and initialized for every pin in the net and assumes the **np->npnum** field contains the number of pins in the net. The **ptp->ndist** field must be initialized to the constant **FAR_DIST** that is larger than the wire grid size of the chip, and the **ptp->nrnod** field must be initialized to **NULL**. The **exchange**() function exchanges the contents of two **pintab**[] elements and the **wdist**() functions computes the rectilinear row and grid distance between **pintab**[] pin pair entries.

```
cmp_nmst(np)
 struct net_t *np;
{
 register struct pintab_t *endp, *ptp, *minp;
 int tmp, mind, edges, numtodo;

 edges = np->npnum - 1;
 for (endp = &pintab[0]; edges > 0; endp++, edges--)
  {
   mind = FAR_DIST;
   numtodo = edges;
   for (ptp = endp + 1; numtodo > 0; ptp++, numtodo--)
    {
     if ((tmp = wdist(&endp->pt, &ptp->pt)) < ptp->ndist)
      { ptp->ndist = tmp; ptp->nrnod = endp; }
     if (ptp->ndist < mind) { mind = ptp->ndist; minp = ptp; }
    }
   /* link in edge pointing to tree parent */
   minp->nrpt = minp->nrnod->pt;
   /* change pintab[] so new node will be at endp next pass */
   exchange(minp, endp + 1);
  }
}
```

This algorithm runs in $O(N^2)$ time but makes no assumption that **wdist**() uses geometric distance. See [7] or [1] for a discussion of MST algorithms. Since the real pin to pin tree edge is not needed and since **pintab**[] entries move, the nearest pin coordinates are used to represent the edge when updating the maps or wire lengths. Notice the part of the circuit data base containing mask level data can be ignored, and once data base coordinates are translated into master slice row and grid values, wire coordinates can be ignored.

3.3 Example Matrix Update Function

The following C function illustrates map update code for a decomposed MST edge with pin pairs separated by at least one row. This code assumes the points have coordinates (**grid1**, **row1**) and (**grid2**, **row2**), and that a possible exchange has been made to insure **row1** <= **row2**. **vrow**[][] in the matrix of vertical row crossing feed thru wires, **vchan**[][] is the matrix of vertical channel feed thru wires, and

hchan[][] is the horizontal wiring channel matrix. **addin_vert**() adds one to the vertical count in the given map from the first row to second row along the given grid. **addin_chan**() adds one to every horizontal grid along the channel at **hchan[row]** from **grid1** to **grid2**.

```
add_dist_conn(grid1, row1, grid2, row2)
 int grid1, row1, grid2, row2;
{
 /* know at least one row between connecting rows */
 addin_vert(vchan, grid1, row1, row2 - 1);
 addin_vert(vchan, grid2, row1, row2 - 1);
 addin_vert(vrow, grid1, row1, row2);
 addin_vert(vrow, grid2, row1, row2);

 /* channel with same row number is above row */
 addin_chan(hchan, grid1, grid2, row2 - 1);
 addin_chan(hchan, grid1, grid2, row1);
}
```

3.4 Output Format

A good output scheme rotates the maps ninety degrees. Cell rows run from top to bottom in a file or on a printed page. Maps of large circuits will be too wide for one page, but a map file can be separated into vertical segments and then joined after printing. For channel map sections see figure 4 and 5. For over row feed thru map sections see figure 6.

3.5 Run Time

The computer program to compute the estimate reads the circuit description, builds the three maps and writes the maps to a file. The run time is 38 seconds for the primary1 circuit from the cell based benchmarks [4] [20] [17]. It has 752 cells, 904 signal nets, and 81 I/O pads. The run time is 128 seconds for the primary2 benchmark circuit with 2907 internal cells, 3029 signal nets, and 107 I/O pads. The times are on a 12 Megahertz, one wait state 80286 system with a 28 ms. hard disk. The time spent filling the **pintab**[] table and computing the MSTs for the 904 primary1 nets is .9 seconds and 4.3 seconds for the 3029 primary2 nets. The MST times are computed by repeating the computation 20 times and dividing by 20. The MST computation time is negligible compared to the time it takes to input the circuit description and write out the maps.

4. Measurements

To illustrate possible estimate applications, a number of measurements using the standard primary1 and primary2 cell based benchmark circuits from various Physical Design Workshops [4] [20] [17] [22] have been made. The placements are from the Timberwolf placement system [24]. The placements measured here require somewhat larger area than the current best placements. The primary1 circuit occupies 2673 two input nand gate equivalents (one gate is three wire grids) and the placement used here was placed on a 17 row substrate with 480 grids per row. The primary2 circuit occupies 7600 gates and was placed on a substrate with 23 rows and 1005 grids per row. The benchmark circuits are representative of typical master slice circuits [15]. The substrate organization (aspect ratio) was provided as input data to the Timberwolf placer and discovered by means of trial and error.

The measurement scheme used for the benchmark circuits assumes fixed 15 wire grid wiring channels and 15 grid high rows as part of the base substrate. The circuit rows would then be moved to their correct locations before final routing. This means wire lengths assume a 30 grid row center to row center distance no matter how many tracks are actually used. Since real wire grid distances are used, I/O pad wires are longer than they should be, and primary2 vertical wires are shorter than they should be because wire channels normally require more than 15 tracks. There is more wiring in master slice area corners than there should be because most I/O pads end up in the corners of the substrate because the original physical design bench mark substrate requires more perimeter than is needed by the placed master slice core. The wire lengths below are for relative comparisons and are always computed using the same outer rectangle algorithm. This makes these small substrate inaccuracies unimportant. The combination of equal spacing for both metal layers and the 30 grid track to track distance means, in computing the MST, cross channel connections are as distant as pins five gates (15 grids) away. Connections passing thru one row along one vertical grid are as distant as pins 15 gates (45 grids) distant

along one vertical grid The distance values can be changed to increase horizontal channel wiring and to decrease vertical feed thru wires at the cost of physically longer wires.

The placements for the benchmarks were placed assuming the global router would add one grid feed thru cells where needed. The chip is normally simply stretched in the horizontal direction. If a large number of added feed thrus are needed, the track usage may be too small because wires from other rows may cause routing conflicts and require even more feed thrus and channel tracks.

4.1 Timberwolf Placement Map Discussion

The primary1 circuit is quite easy. See figure 4 for the Timberwolf primary1 placement most congested area. The values beginning with a '+' sign mean the value is really the number plus 1/2. The value +10 means 10.5. It requires 226 channel track using the outer rectangle estimate and has extra unused feed thrus in every row. The wire length is 111,000 (111k where k stands for thousand) wire grids (or 1.11×10^6 microns because both the metal layers use a 10 micron grid). 68k grids are vertical wires and 43k grids are horizontal. 61.5 percent of the wiring is vertical. The highest track usage channels need 15 or 16 tracks. It may be possible to achieve a better routing because the high track channels have adjacent low track demand channels. Pin pairs connecting along one row can possibly be moved to the adjacent wire channel with less track usage.

The larger primary2 circuit is more difficult. See figure 5 for a channel track usage map of a congested area and see figure 6 for the row feed thru requirement map of the same area. It requires 544 tracks using the outer rectangle estimate and needs to have feed thrus added by the global router in many rows. The largest number is 199 or a requirement that each row increase in length by 20 percent (see table 1). A real router may not require extra feed thrus since it can reorganize the MST pin pairs to increase the number of along channel horizontal connections. The physical wire length will be longer but channel track demand may not increase if the new horizontal segments can be location in channel sections whose requirement is less than the channel maximum. The cost may be a larger total channel track number and possibly slower circuits if the wire length of critical nets is increased. Even if feed thru requirements are not reduced the added feed thrus should cause no problem if each row has feed thrus added to make sure pins remain aligned in the vertical direction. The wire length will also be proportionally higher. The wire length if no extra feeds thrus need to be added is 468k wire grids. 306k grids are vertical wires and 162k are horizontal. 65.3 percent of the wiring is vertical, but this value will be reduced when the wiring channels are lengthened for the extra feed thrus.

The highest channel wire usage is 30 to 32 grids and most high usage channels are adjacent to other high track usage channels. This means clever wire channel assignment will probably not reduce track requirements. The total track usage is about 1/4 to 1/3 the track value predicted by [10, figure 4, p. 43], but that substrate had both horizontal and vertical wiring channels, and it is not clear the terms "circuit element" in [10] and gate as used here are the same.

4.2 Half Perimeter Net Wire Evaluation Function Test

One physical design open question involves accuracy of the net wire length part of the the placement evaluation function. Persky et. al. claim and give reasons why half perimeter wire length is a reasonable evaluation function approximation in their description of the LTX system [19]. The half perimeter wire estimate uses half the perimeter of the rectangle bounding all pins in a net. They show why it is trivially accurate for two or three pin nets. They give reasons why it is good for four or five pin nets, but they state it is probably not very accurate for nets with six or more pins [19, p. 226]. The MST estimate is more exact (up to Steiner wiring) but takes more time to compute. The outer rectangle estimate can be used to measure how much wire comes from nets with more than five pins and therefore identify nets whose wire length contribution may be inaccurately evaluated.

Because from 1/3 to 1/2 for primary1 and 1/2 to 2/3 for primary2 of the wire length, channel tracks, and feed thrus are contributed by large nets in the good Timberwolf placements, a high wire proportion is due to inaccurately evaluated nets. This suggests the half perimeter function is not sufficiently accurate. For the Timberwolf primary1 placement 30k or 27 percent of the wire grid length comes from nets with more than five pins. 105 of the 226 required tracks or 46.5 percent are contributed by large nets. Around 50 percent and sometimes as many as 8 or 9 wires out of the maximum of 15 or 16 are contributed to the channel track usage by the larger nets. Around 33 to 40 percent of the feed thru total

is contributed by greater than five pins nets.

For the Timberwolf primary2 placement 217k or 46.2 percent of the wire grid length is contributed by nets with more than five pins. 305 of the 544 required tracks or 56.5 percent are contributed by large nets. From 50 to 66 percent of the horizontal wire channel track usage is due to nets with more than five pins. The highest usage is 20 tracks. See table 1 column three for the feed thru percentage from greater than five pin nets. The large net feed thru percentages ranges from 48 to 64 with the high values in the most congested circuit regions. The larger percentage contribution from large net wires for primary2 versus primary1 may explain why primary2 is significantly more difficult to lay out than primary1.

4.3 Potential Area Reduction from a Third Metal Layer Measurements

Some experimental master slice ASIC circuits use a third metal layer (metal3). The most obvious use dedicates metal3 to long vertical cell row feed thru wires (actually feed over) that connect pins on rows separated by intervening cell rows. Long connections can be made without causing congestion in the regions they cross. The alternative to dedicating metal3 to horizontal wires suffers from the problem that the vias used to connect metal1 and metal3 horizontal wires in, for example, channel jogs block scarce vertical metal2 feed thru grids. There may be some better mixed direction metal3 use that is not considered here.

A known good placement can be used to measure the possible benefits from dedicating metal3 to vertical wires. In the measurements described here, the metal3 layer is dedicated to long vertical wires that cross at least one cell row (see figure 3). The results discussed here evaluate placements made for two layer metal to see how much track and feed thru reduction is possible with simple rewiring. The next step would possibly be to repeat this experiment using placements from a placer modified to maximize vertical wiring. But since maximizing vertical wiring causes an increase in real wire length and since the placement for primary2 already has a possible shortage of available metal2 feed thrus, the rewiring scheme used here may actually show the potential size reduction limit from the third metal layer addition.

The benchmark placements from the Timberwolf system discussed in section 5.1 have been rewired to to maximize vertical wiring. Tables 2 and 3 compare the rewired vertical feed thru numbers to the original wire estimate results that used exact physical wire length. For the three metal layer case, the metric is weighted wire length. Wire length is weighted such that a wire that connects rows separated by exactly one intervening row (see figure 3) along one vertical grid is exactly as distant as a horizontal wire connecting a pin only six grids (two gates) distant. Further vertical wire shortening leads to no horizontal wire channel height decrease at least for the benchmark circuits.

Since the primary1 circuit has sufficient available feed thrus, adding a third metal layer does not lead to much area reduction. See table 2 for primary1 possible metal3 wire usage. Columns two and three contain the number of vertical feed thru wires for two layer metal assuming exact wire distance connections. Column three contains the percentage of available (non blocked) feed thru wires that would be used assuming no feed thru were lost due to congestion problems. Column four contains the potential number of long vertical wires that could be moved to metal3. The connection pattern in figure 3 would use metal3 but the patterns in figures 1 and 2 would not. Column five gives metal3 feed thru percentages that would be used for each row. Notice that nearly two thirds of the available feed thru grids go unused over most internal rows in the three layer metal case. Global routing that makes maximum metal3 use would, at a minimum, reduce the required track count from 226 to 209 or 7.5 percent. The trade off is a 10.4 percent increase in total wire length. This assumes the bench mark system uses the same pitch for all metal layers. A better global router could reduce the required maximum channel density by reducing channel density peaks, but then the same router could probably also reduce peaks in the two layer metal case [14]

Table 6 shows the saving for the primary2 circuit. The saving here is potentially larger. If real wire length is used, it appears that some rows have an available feed thru shortage that would require widening of the entire master slice area. But a better global router may be able to convert some crossings into along channel wires that can be run along channel sections that do not require the maximum channel density. In any case, global routing that attempts to make maximum use of metal3 would, at a minimum, reduce required track number from 544 to 486 or 10.7 percent. The trade off is a

15.1 percent increase in total wire length. Column five shows that nearly two thirds of the available metal3 tracks are used over the central rows. If the master slice row lengths really needs to be increased by the 199 grids that row 17 needs, the addition of a third metal layer can reduce total area by 25 percent (1000/1200*486/544). Of course, the actual decision to add a third metal layer will be determined by manufacturing and electrical considerations in addition to area reduction.

5. L-shaped Steiner Tree Decomposition

An attempt was made to improve the net decomposition phase of the estimate by changing to Steiner tree wiring. The change has not been made since at least for one simple approach, the estimate was no better. The optimum L-shape rectilinear algorithm described at 1989 DAC [12] was implemented. It is both efficient (converting an MST to an optimum L-shape Steiner MST is linear in the worst case) and because it computes upper and lower rectangles, fits well with this estimate. The following changes were made to the estimate program:

1. The original MST algorithm (see section 3.2) was modified to compute separable MSTs.
2. The dynamic programming algorithm described in [12, p. 164] was implemented to set the best overlap values for the lower and upper rectangles.
3. The MST was traversed again using the lower-upper rectangle choices and the same rectangle overlap algorithm to find Steiner points.
4. The Steiner points were added to the net. Steiner points that did not lie on cell rows were moved to the nearest row. This movement was required only for I/O pad connections since Steiner points lie on the grid of original point intersections and all internal pins lie on rows. A net was treated from then on as a larger net with the Steiner points connecting to virtual pins.
5. The normal separable MST for the new larger net was recomputed.

The running time was still reasonable. Total running running time for primary1 was 65 seconds versus 38 and for primary2 the time was 254 seconds versus 128 on the same 12 Megahertz 80286. All of the extra time (a factor of around 25) was required by the Steiner MST algorithm, but the implementation contained some measurement and consistency checking code. Unfortunately, the measured results were not much better than the non-Steiner MST results. The wire length for primary1 was 2.85 percent less (453.8k versus 468.7k grids) and for primary2 was 3.16 percent less (453.8k versus 468.7k grids). The outer rectangle track requirement was virtually the same for primary1 (222 versus 224) and 2.9 percent less (528 versus 544) for primary2. The Steiner tree row feed through requirements were considerably higher due to the extra 194 Steiner points for primary1 and 854 Steiner points for primary2. See Table 1 column 6 for the Steiner row feed thru requirements for primary2. Notice how much larger the Steiner values are compared to the simple MST values in column 2.

There are a number of explanations for these results. The expected 10 percent wire length reduction in Steiner trees [12] is lessened because only 1/2 to 2/3 of the wire is contributed by nets that are large enough to benefit from Steiner points (see section 4.2). The improvement is further reduced because good placements avoid expensive vias by lining up pins along straight lines. The additional Steiner points tend to move wires toward the already congested central chip regions and add vias. This is an important negative factor. Except for the Steiner movement of wires to chip center, I believe the seeming extra row feed thrus are caused by implementation problems. The implementation assumes that a Steiner pin is located on a row and therefore blocks a feed thru grid when it enters a channel. Providing a channel router can process points that do not need to enter a side, this assumption is overly pessimistic. Although, there is definitely some cost associated with the Steiner points and their required via. A second reason for the extra feed thrus is that the distance metric for separable MSTs maximizes vertical edge length when distances are tied. The axis should probably be rotated by 90 degrees to reduce vertical wires but this will increase channel track demand. Use of Steiner points may well improve the outer rectangle estimate, but it is not obvious exactly how to compute it. The most obvious approach is not an improvement.

6. Discussion

It is possible to use this estimate in the placement evaluation function. When a cell is moved, all connecting nets must have their counts removed for every pin pair, and the MSTs must be recomputed. Finally, the new pin pair outer rectangles must be added back in. Incremental MST recomputation is also possible (see [9] or [27] for example). An attempt was made to use the maps described here (incrementally computed) to reduce congestion by assigning a negative weight to row positions near congested horizontal channels during the development of the program described in [15] for gate arrays. The results from a few attempted placements on a few designs was that the congested area simply moved to a new array region and was worse because the wire length increased. The more complicated schemes used in [23] [14] [28] may be required because intuitively it seems congestion avoidance should help.

The estimate can detect properties of particular circuit types that are missed by at least one statistical measure. An estimate (see [6]) derived from [5] [10] was used to predict wirability for individual circuits. Circuits implementing FIFO or LIFO queues tended to be more difficult than predicted, but the outer rectangle maps showed significant congestion. The regular structure of queues seems to not match the master slice organization. Randomly connected circuits also tend to be more difficult than predicted by simple statistical estimates due to above average total wire length. Fortunately random circuits do not correspond to electrically meaningful designs. Circuits using level sensitive logic, scan rings, or other special testing logic tend to be easier to wire than predicted because they often have simple wiring patterns using short wires. The detailed information provided by the estimate can simplify easy or difficult circuit type detection.

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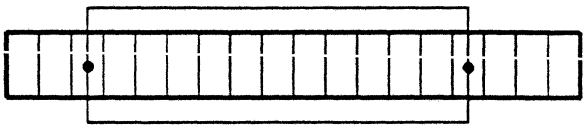

Figure 1. Along Channel Possible Connections

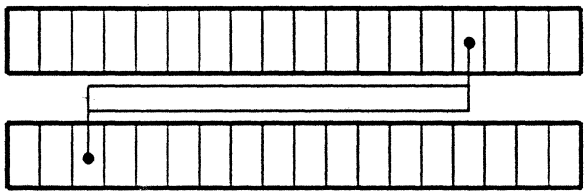

Figure 2. Cross Channel Connection

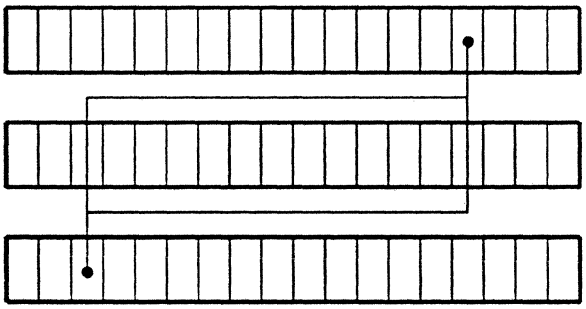

Figure 3. Cross Row One Via Possible Connections

Figure 4. Timberwolf Primary1 Horizontal Channel Track Demand Map

Timberwolf primary1 placement most congested region
Rotated map so wiring channes 0-17 (horizontal channels) run down page
Rotated map so grids 120-166 (vertical wires) run across page

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
120	+14	9	6	+8	8	+4	+6	+7	+8	+5	+11	+7	8	+7	7	4	7	8	120
121	+14	+8	+5	8	+7	+5	+6	+8	+8	+5	+11	+7	8	+7	7	5	7	8	121
122	+14	9	6	8	+6	+5	6	+9	+8	6	+11	+7	8	7	+6	+4	+6	8	122
123	+14	+9	7	+8	+6	5	5	+9	8	6	+11	7	+7	7	7	5	7	+8	123
124	+14	+9	7	+8	7	+4	4	+9	8	6	+12	8	+7	7	7	+3	+6	+8	124
125	14	+9	+7	8	+6	+4	4	+9	8	6	+12	8	+7	+7	+7	+3	+6	+8	125
126	14	+10	9	8	+6	+3	+4	8	+7	6	+12	8	+7	7	8	4	7	+8	126
127	14	10	+9	8	+6	+3	+4	+8	8	+6	+13	+8	+8	7	7	4	+7	9	127
128	14	+10	10	+8	8	+3	+5	9	8	6	+13	+9	+8	+7	+6	3	+7	9	128
129	14	+10	10	8	+7	+4	6	9	+7	+5	12	9	8	+7	+6	3	+7	9	129
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131	14	10	10	+8	7	4	6	8	7	+5	+12	+8	8	7	+6	4	8	+9	131
132	14	10	9	+8	+6	3	+5	9	7	6	13	9	+8	7	6	+3	+7	9	132
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137	+14	11	10	+8	6	+2	5	+10	7	7	+13	+8	+8	8	6	+3	+8	+9	137
138	15	11	+9	+8	+5	1	5	+10	7	7	14	9	+8	8	+6	4	9	9	138
139	+14	+10	+8	8	5	1	6	+10	+7	+7	14	9	9	+8	6	3	+8	9	139
140	+14	10	8	8	5	1	7	11	+7	7	+13	9	+9	+8	6	3	+8	9	140
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146	14	10	8	7	5	+1	+7	+10	6	+7	+14	8	+8	8	+5	4	+10	9	146
147	+13	10	+7	+6	5	+2	7	11	8	+8	14	8	+8	9	6	+4	+10	9	147
148	+13	10	+7	+6	5	+2	7	+10	+8	+8	14	8	+8	8	6	+4	10	+8	148
149	+14	10	8	7	5	2	+7	10	8	+9	14	9	8	7	+5	+4	10	+9	149
150	+14	10	+7	+6	5	2	7	+10	9	+10	13	8	8	7	+4	+4	10	+9	150
151	14	+9	+7	+6	5	+2	+7	10	+9	+10	12	8	+8	+8	5	5	+11	10	151
152	14	+9	+7	+6	6	+2	+6	+8	+9	+11	+11	8	+8	+9	6	5	10	+9	152
153	14	+9	8	+6	6	3	+6	9	10	12	+10	7	8	+9	6	5	10	+9	153
154	+14	10	7	+6	6	3	7	+9	+10	+12	+10	7	8	+9	+6	+5	10	+9	154
155	14	+9	7	+6	+6	+3	7	+9	+10	12	10	7	8	9	+6	6	10	+9	155
156	14	+9	7	+6	7	4	7	10	10	12	+9	+6	9	9	+6	6	+9	9	156
157	14	10	8	7	7	+3	+6	10	+10	+11	+9	6	+8	9	+6	6	+10	9	157
158	+14	+10	+7	+6	+7	4	+6	+9	+9	+10	9	6	+8	9	+7	+5	10	9	158
159	14	11	+7	+6	8	5	+6	+9	+9	11	9	6	+8	9	+8	+5	10	9	159
160	14	11	8	+7	+8	5	7	9	+9	+10	+8	6	+7	8	+8	+5	10	9	160
161	14	11	8	+7	+8	5	7	+8	8	10	8	6	+7	8	+8	+5	10	9	161
162	14	11	7	7	8	5	7	+8	8	+10	+8	6	+7	8	+8	5	+9	9	162
163	+13	+10	+7	+7	8	+4	+6	8	+7	+10	9	+7	+8	8	+8	5	10	+9	163
164	+13	+10	8	8	+7	5	+6	+7	7	11	9	7	8	+7	+8	5	+9	9	164
165	+13	+10	+7	7	7	5	+6	+7	8	12	9	+7	+8	8	9	5	+10	9	165
166	+13	10	8	7	+7	+5	+6	7	+7	12	8	7	8	8	9	+4	10	9	166

Note to reviewer: map will be cropped to half column for paper

Figure 5. Timberwolf Primary2 Horizontal Channel Track Demand Map

```
Timberwolf primary2 placement most congested region
Rotated map so wiring channes 0-23 (horizontal channels) run down page
Rotated map so grids 421-467 (vertical wires) run across page
```

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	
421	12	+8	+8	9	+11	16	14	21	+18	+23	+18	12	+11	+20	+19	18	+28	27	16	11	18	+18	15	+8	421
422	12	10	+8	+9	11	+14	13	+20	18	+22	+18	13	+12	+19	+18	+16	29	29	17	12	19	+18	15	+8	422
423	12	10	+7	9	+10	+14	+12	20	18	23	19	+12	12	19	+18	+15	+28	28	16	+11	+18	+19	15	+8	423
424	12	+10	8	9	+10	+15	+12	+21	+18	+22	19	+12	12	19	+18	+15	+29	+28	16	+11	+17	+19	15	+8	424
425	+11	11	+7	+8	+10	+15	+11	21	19	22	+18	+12	+12	+19	19	16	29	+29	+16	+12	17	+19	+14	+8	425
426	11	10	+6	8	10	15	+11	21	19	+21	+19	+12	12	18	+18	16	+28	29	16	+12	17	+19	14	+8	426
427	+11	+10	+6	8	10	16	12	+21	20	22	20	+12	13	+18	18	+15	30	28	16	13	+16	+19	14	+8	427
428	11	+8	6	7	+9	15	+11	+22	21	+22	+19	13	+13	19	17	14	30	29	+16	13	+15	+19	15	9	428
429	+11	9	6	7	9	+13	+12	23	+20	22	+19	13	14	19	17	14	+29	+27	+16	12	16	+19	14	+8	429
430	12	+9	6	+6	9	14	+12	+20	20	+21	+19	13	+13	+18	17	+13	29	+27	+16	+12	+16	20	14	+8	430
431	12	8	+5	+6	9	+13	+12	22	+20	+22	18	+13	14	+19	+16	13	+29	27	17	13	+16	+20	+14	+8	431
432	+12	8	+5	7	+8	+11	13	22	20	22	+18	+14	15	+20	+17	+13	28	27	+17	+12	+16	20	14	9	432
433	12	+7	+5	7	+8	13	+12	20	+19	21	+18	+14	14	+19	+17	14	+28	+27	17	12	16	+19	15	8	433
434	+12	8	+5	7	+8	+12	13	+20	20	+22	17	+14	15	+20	18	+13	+28	28	+17	+12	+16	+20	+16	+8	434
435	13	8	6	+6	8	+12	+12	19	19	23	+17	15	15	20	+18	+13	+28	+28	18	12	+17	+20	16	8	435
436	+12	6	+5	+6	8	13	+12	+17	19	+23	18	14	+13	18	17	+13	+28	29	+18	11	17	+18	+15	8	436
437	+12	6	+5	+6	8	+13	14	17	+18	+23	+16	14	14	18	+17	13	29	29	18	+11	+16	+18	16	+8	437
438	12	+5	6	7	8	13	13	+16	+18	24	17	+15	14	18	+17	12	29	+28	18	13	17	19	+16	+7	438
439	12	5	+5	8	+8	+13	13	+15	20	+24	19	+15	13	18	+18	+12	29	+28	+17	13	+16	18	16	+7	439
440	12	5	5	+7	+8	13	+12	+15	+19	23	19	15	+12	+17	+18	14	29	+28	+17	13	16	+17	16	+7	440
441	+12	+5	+5	9	+8	+13	13	16	20	23	+18	15	13	+18	18	+12	+29	29	18	+13	+17	+18	+16	+7	441
442	+12	+5	+5	9	+8	+13	13	+16	+20	23	19	+15	13	19	+18	+12	29	+28	18	14	+17	+17	16	+7	442
443	+12	+5	6	+8	+7	13	+12	+16	20	+21	19	+15	+12	+18	+17	13	+29	+28	18	14	+17	+17	16	+7	443
444	+12	+5	+5	+8	+7	13	13	+16	+20	+21	18	+15	12	+18	18	+12	+29	27	+17	14	17	18	15	+7	444
445	+12	+5	5	8	+7	+11	+12	17	21	+21	+18	+15	+11	+18	+17	+12	29	+26	+18	15	+17	+18	15	8	445
446	13	6	5	+8	7	+11	12	17	+21	+21	+18	15	11	19	18	+13	+29	28	19	+14	18	18	14	8	446
447	+13	+6	+4	8	+7	12	12	17	22	+21	19	15	10	19	18	+13	+28	+26	+19	+14	+17	+18	14	8	447
448	+13	6	+4	+8	8	+11	12	17	+22	+22	+19	+15	+10	19	+16	+13	28	+26	+19	+14	+17	19	+14	8	448
449	+13	+6	5	+8	+8	11	+11	+16	+21	22	+19	+16	11	+19	+16	+14	28	+26	20	13	+17	+18	14	+8	449
450	14	7	5	+6	+7	10	+11	17	22	21	19	+16	11	+19	16	15	+27	+25	20	+12	+16	18	13	+8	450
451	14	7	+4	7	+8	+10	12	18	22	21	19	17	12	19	16	15	+27	26	+20	13	17	+18	+13	+8	451
452	14	7	+4	7	+8	+9	12	+17	22	+21	+19	+17	13	19	16	15	+27	26	21	13	17	+19	13	+8	452
453	14	7	+4	+7	9	+8	12	+17	20	+21	+19	+17	+13	+19	16	15	+28	+25	20	+12	16	+19	+13	9	453
454	14	+7	5	+7	+10	+8	+11	+17	21	+21	19	+18	14	+20	16	15	+28	+25	+19	13	+16	18	13	+8	454
455	14	+6	+4	+6	+10	9	+11	17	21	22	+19	+18	14	21	16	15	+28	25	19	+12	17	18	13	+8	455
456	14	+6	+4	+6	10	+8	11	17	20	+21	20	+18	14	20	+15	15	28	24	+19	13	+17	18	13	+8	456
457	14	+6	+4	+5	9	+7	11	17	+20	22	20	+18	+14	+19	+15	+15	+27	24	+20	13	17	+17	+12	11	457
458	13	+6	4	5	+9	+7	11	17	+20	+22	20	+19	15	+19	+15	+15	+26	+24	22	+12	+17	17	12	+9	458
459	13	+6	4	5	+9	+7	11	+17	+20	+22	+20	20	15	+18	16	+15	+25	+25	22	+12	17	+16	+12	10	459
460	+12	+6	+4	5	+8	7	11	+17	21	23	+22	20	+15	+18	+16	+15	26	26	23	13	17	+16	+12	10	460
461	+12	6	4	5	9	+7	11	+17	+21	+23	22	+19	16	19	16	16	+25	+25	+22	+12	17	+16	13	+10	461
462	+12	6	4	5	+9	8	12	+18	+21	+22	+22	+19	16	19	+16	+16	+26	25	+21	+12	+17	16	13	+10	462
463	+12	+5	5	5	9	8	12	17	21	22	+24	+19	18	19	17	17	+26	25	22	13	+17	16	+12	+10	463
464	+12	+5	5	5	+9	+8	12	+17	22	+22	24	+18	+17	+18	16	+16	26	25	+21	14	+17	16	13	11	464
465	13	+5	+5	+4	9	+8	+12	18	+21	+22	+24	19	+17	18	16	+16	25	25	21	+13	+16	+14	12	+10	465
466	13	+5	+5	+4	+9	+8	13	18	+21	+22	26	19	+18	+18	+16	16	25	+25	21	13	+16	+14	+12	11	466
467	13	+5	+5	+4	+9	9	14	+17	22	23	+25	18	18	18	+15	+16	26	+25	20	15	16	15	14	+11	467

Note to reviewer: map will be cropped to half column for paper

Figure 6. Timberwolf Primary2 Vertical Row Grid Crossing Map

```
Timberwolf primary2 placement most congested region
Rotated map so wiring channes 1-23 (horizontal channels) run down page
Rotated map so grids 421-467 (vertical wires) run across page

    |  1|  2|  3|  4|  5|  6|  7|  8|  9| 10| 11| 12| 13| 14| 15| 16| 17| 18| 19| 20| 21| 22| 23|
----|---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+----
 421|  1=   =   =   = +2= +2= +3= +1= +1=  2=  += +1=  +=  3= +1=  2=  1=  +=  +=   =   =  1=   | 421
 422|  += +2=  += +1=   =   =  2=   =   =   =  1=  2=  1=  2=  += +2= +2=  3=  3=  2=  2=   =   | 422
 423|   =   =   =   =  1=  1=   =   =   =  2=  1=   =  2=   =  2=   =   =   =   =  1=  3=  1=   | 423
 424|  1=  1=  1=  1=  2=  2=  3=  2=   =  2=   =  2=   =  1=   =  1=  2=   =  +=  += +2= +1=  1| 424
 425| +1= +2=  += +1=  3=   = +1=  += +1=   =  += +2= +1=  3= +1= +1= +2= +1=  1=  2=   =  2=   | 425
 426|   =   =   =   =   =  1=   =   =   =  1=  1=   =  2=   =  2=  +=  += +1=  1=   =  2=   =   | 426
 427|  3=  1=  1=  1=  2=  2=  1=  1=   =  2=   =  += +2=  2= +1= +3= +1=  +=  += +1= +1=  +=   | 427
 428|   =  +=  +=  += +3=  +=  1= +2=  1= +2= +1= +2=  += +2=  +=  += +2= +1=  2=   =   =  2=  2| 428
 429|  1=   =   =  1=  += +1=  3= +3=  2= +1=  2=  3=  1=  3=  += +1=  +=  +=  +=  +=  1=   =   | 429
 430|  2=  1=   =  += +1=  4=  +=  += +1=  2=  2=   =  2=   =  2=   =  1=   =  1=   =  1=  1=   | 430
 431|   =   =   =   =  3=  2= +1= +2= +2=  1=   =  1=   =  1=   =  += +2=  += +2=   =  += +2= +1| 431
 432| +1=  +=  +=  1=  +=  +=  3= +2=  2=  += +1=  3=  2=  3=  1=   =   =  += +2=  += +1=  += +2| 432
 433|   =   =   =   =  1=  3=   =   =   =  1=  2=   =  2=   =  2=   =  1=   =   =   =   =  1=   | 433
 434|  1=   =   =  1=   = +1= +2= +2= +1=  2=   =  2=   =  3=   =  +=  1=  1=  3=  += +1= +2=  2| 434
 435| +2= +1=  +=   =   =   =  1=  1=  2=  +=  3=  4= +1= +4= +1=  += +2=  +=  2= +1= +2= +2=   | 435
 436|   =   =   =   =   =  1=   =  1=  2= +1= +2=  +=  +=  += +1=  += +2= +2=  +=   =  1=   =   | 436
 437|  1=   =   =   =   =  2=  2=   =   =  1=   =  +=  += +1= +2=  2= +1=  2= +1=  +=  +=  +=  2| 437
 438|   =  1=  1=   =   =   =  1=  1=  1=  +=  3=  1=  2=  +=   =  2=  1=   =  2=  1=  2=   =   | 438
 439|   =   =  2=  +=  += +1=   = +1= +3=  2=  3= +1=  += +2= +1=  1=  1=  2=  +=   =  1=   =   | 439
 440|   =   =   =   =   =   =   =   =   =   =  2=   =   =   =  2=  2=  1=   =   =   =   =   =   | 440
 441|  1=   =  2=   =  1=  1=   =  1=  1=   =   =  1=   =  1=   =   =  2=  +=  += +1= +2=  2=   | 441
 442|   =   =   = +2=  += +1=   = +2=  3=  1=  2= +1=  += +2=  +=   =   =  1=   =  2=   =   =   | 442
 443|   =  += +1=  +=  +=  +=  += +1=  += +1= +2=  += +1=  +=  1=  2= +1= +2=  +=  2=   =  1=   | 443
 444|   =   =  1=   =  1= +1=  +=  += +1=  +=  += +2=  += +2= +1= +1= +1=  +=  +=  +=  += +1=   | 444
 445|   =   =   =  1=   =   =  1=  1=   =   =  2=  1=   =  2=   =  1=   =  1=  1=  2=   =  2=  2| 445
 446|  +=  +=  2=   =   =   =   =  1=   =   =  2=   =  2=   = +1=  2=  3=  3=  += +2=  +=  +=  +| 446
 447| +1=  +=  +=  += +2= +1=  +=  +=  += +1=  += +1=   =  1=  1=   = +1=  +=  1=  +=  +=  +=   | 447
 448|   =   =   =  1=  2=   =  2= +1= +2=  2= +1= +2= +1=  1=  1=  1= +1=  1=  2=  1=   =  2=   | 448
 449|   =  1=  1= +1= +2=  +=   =  1=   = +1=  3=  2= +1= +1=  3=  2=  3= +3= +1= +2= +1=  += +1| 449
 450|  1=  +=  +=  +=  +=  +=  1=  1=  1= +1= +1=  += +1=  +=  += +1=   =   =   =   =   =   =   | 450
 451|   =   =   =  2=  2=   = +1= +1= +1=   =   =  1=  1=   =   =   =   =  1=  1=  1=   =  2=   | 451
 452|   =   =   =   = +1= +1=  += +1= +2=  += +1= +1=  +=   =   =   =   =  2=  2=  2=  2=  +=   | 452
 453|   =   =   =  1=   =   =  2=   =   =  1=  1=   =  1=   =   =   =  1=  +=  +=  +=  += +1=  2| 453
 454|  1=  1=  1= +1= +1=  +=  +=  3= +1= +1= +1= +2= +1=  +=   =  1=   =  1=  2=  2=   =   =   | 454
 455|   =   =   =  += +2= +1=  +=  += +2=  2=  2=  3=  1=  2=   = +1=  +=  2=  +=  += +1=   =   | 455
 456|   =   =   = +1= +2=  +=   =  1=   =  1=  1=  1=  1=   =   =  1=  +=  += +1=  1=  2=   =  1| 456
 457|   =   =  1=   =   =   =   =  1=  2=   =   =   = +1=  += +1=  2=  1= +1=  2=   =  1=   =  2| 457
 458|   =   =   =  += +1=  +=  +=  +=+2=  +=  += +2=  += +2=   =   = +1= +1= +1=   =  2=   =   | 458
 459|  1=   =   =  1=  2=   =  += +1=  1= +2=  2=  2= +1= +1= +1=  1=  1=   =   =   =   =  1|  459
 460|   =  2=  +=  +=  +=  +=  += +1=  +=  3=  3=   =  2=   =  2=  1= +1= +1= +2=   =   =   | 460
 461|   =   =   =   =  1=   =   =   = +2=  +=  +=  1= +2=  1=  +=  1=  += +1= +1=   =   =  1=  2| 461
 462|  1=   =   =   =  2=   =  2=  2=  1= +2= +1= +2=  += +1=   =  1=  1=   =   =   =  1=   =  2| 462
 463|  += +1=  +=  +=  +=  +=   =   =   =  3=  3=  3=  1=  3= +1=  +=  2=  2=  2=  +=  +=  +=  +| 463
 464|   =   =   =  1=  2=   =   =  1=  2=   =   =   =  2=   =   =  1=  2= +1= +2= +1=  +=  2=  2| 464
 465|  +=  +=  +=   =  2=   =  1=   =  1= +2= +1=  3=  1=  1=  += +1=   =   =  2=   =   =   =   | 465
 466|   =   =   =   =  1=  1=  1=   =   =  3=  3=  3=  1= +3=  +=  +=  1= +2= +1=  1=  1=   =  1| 466
 467|   =   =   =  1=   =  1= +1=  += +2=   =   =   =  2=   =   =  2=  2=   =  2=  2=  2=  1=  2| 467
```

Note to reviewer: map will be cropped to half column for paper

TABLE 1. Timberwolf Primary2 Row Feed Thru Requirements

Row	Used grids	Unused grids	unused with unc. pins	% used by >5 pin nets	Steiner used grids
1	478	271	322	61.5	488
2	633	165	203	45.8	713
3	715	78	114	49.7	798
4	700	96	130	46.0	754
5	802	22	51	42.3	897
6	833	-6	18	42.1	888
7	938	-89	-73	46.7	1008
8	896	-60	-38	49.2	944
9	923	-78	-56	49.7	1002
10	890	-61	-34	52.1	987
11	858	-41	-7	58.4	908
12	839	-37	-1	58.4	934
13	953	-138	-108	64.0	1041
14	901	-71	-43	57.8	1001
15	944	-114	-95	54.0	987
16	983	-139	-120	57.7	1024
17	1039	-199	-185	63.0	1149
18	1008	-148	-133	53.7	1085
19	929	-80	-58	49.5	1007
20	847	-17	14	51.7	916
21	821	21	51	55.4	892
22	755	67	102	48.0	814
23	549	186	217	34.9	581

TABLE 2. Primary1 Metal3 Vertical Feed Through Wires

	Real Wire Distance		Two Rows Equal Two Gates	
Cell Row	Total Crossing Wires	% of Metal2 if no Metal3	Possible Metal3 Wires	% of Metal3
1	188	57.7	33	6.9
2	243	73.3	48	10.1
3	223	70.8	68	14.1
4	286	85.5	120	25.1
5	279	84.3	144	29.9
6	283	83.4	177	36.9
7	291	88.2	195	40.5
8	324	94.1	208	43.2
9	334	95.7	192	40.0
10	307	89.7	176	36.6
11	324	94.2	153	31.8
12	284	86.3	137	28.5
13	263	82.1	119	24.8
14	252	77.2	102	21.3
15	246	74.7	78	16.2
16	227	68.8	50	10.4
17	220	67.9	24	5.0

TABLE 3. Primary2 Metal3 Vertical Feed Through Wires

	Real Wire Distance		Two Rows Equal Two Gates	
Cell Row	Total Crossing Wires	% of Metal2 if no Metal3	Possible Metal3 Wires	% of Metal3
1	478	63.9	128	12.8
2	633	79.4	221	22.0
3	715	90.2	297	29.5
4	700	88.0	346	34.4
5	802	97.4	408	40.6
6	833	100.7	430	42.7
7	938	110.5	448	44.5
8	896	107.2	500	49.8
9	923	91.7	520	51.7
10	890	107.4	535	53.2
11	858	105.0	583	58.0
12	839	104.6	560	55.7
13	953	117.0	574	57.1
14	901	108.6	558	55.5
15	944	113.7	537	53.4
16	983	116.5	553	55.0
17	1039	123.7	566	56.3
18	1008	117.2	576	57.3
19	929	109.5	535	53.2
20	847	102.1	445	44.2
21	821	97.5	359	35.7
22	755	91.8	208	20.7
23	549	74.8	94	9.4

Conference Reports

27 th Design Automation Conference

Report on the 1990 Design Automation Conference

Orlando, FL, June 24-28, 1990

Randall Brouwer

Center for Reliable and High-Performance Computing
University of Illinois, Urbana-Champaign
Urbana, IL 61801

The 1990 Design Automation Conference was held from June 24 through June 28 at the Orlando/Orange County Convention Center, Orlando, Florida. The conference was highighted by nearly 40 technical sessions, tutorials, and panel discussions, along with numerous technical exhibits.

This was my first opportunity to attend the Design Automation Conference, and I was first impressed by the size of the conference. It became immediately clear that much effort was spent in organizing the conference because everything ran so smoothly.

Along with presenting a paper on the topic of parallel global routing in Session 38, I was able to attend a number of other sessions on various topics including placement, routing, channel routing, testing, and fault simulation. The quality of the papers and the presentations was very professional.

Besides attending the technical sessions, there was time to meet people and to talk to vendors about their products. This especially gave me a better perspective on the design automation industry in general.

I would like to thank SIGDA for providing the travel grant which allowed me to attend DAC-90, and the Program Committee and my session chair for their work in organizing the sessions.

Report on 27th Design Automation Conference

Anurag P. Gupta
Electrical and Computer Engineering Department
Carnegie Mellon University, Pittsburgh, PA 15213

The 27th Design Automation Conference was held in June, 1990 in Orlando. The combination of an impressive technical program and an extensive set of industrial exhibits has made it the premier conference for the DA professional. I'd like to take this opportunity to share some of my impressions of DAC'90.

The keyword for this year, at least for the industrial exhibits, seems to have been **frameworks**. Its significance was underscored by the interest in the demonstration by the CAD Framework Initiative, innumerable number of vendor videos and presentations that used it repetitively, and even in some toys handed out by some of the vendors (e.g. Interact's "screaming-ball" which "screamed" when touched to express dismay at a no-integration scenario)! It was interesting to see that ideas as recent as those published in last year's DAC were finding their way to products; for example, DEC's PowerFrame seemed to share the tool-object concept introduced in Daniell's CADWELD system last year.

CAD tools targeted towards optimizing circuit performance are becoming increasingly significant. Of specific interest to me was the session on timing verification. Paper 7.1 by Sakallah *et al* describes a novel approach for timing analysis that can handle level-sensitive latches which had confounded most previous approaches. Paper 7.2 by Martello *et al* was interesting since it can handle circuits consisting of complex components unlike just combinational logic, flip-flops and latches addressed by previous approaches.

The SIGDA DA Library on CD-ROM project also generated a lot of interest. The project has tremendous potential and the demo of the prototype system in the SIGDA University booth convinced me of its feasibility and usefulness.

Most importantly, I think DAC provides an excellent opportunity for meeting and exchanging ideas with other members of the DA community and for finding out about the latest products and research ideas. While the industrial booths provided a lot more sales pitch than useful information, I think that they make DAC a unique well-rounded conference.

Finally, I would like to thank SIGDA for providing the travel grant to attend the conference.

Conference Report - 27th DAC- Design Automation Conference
June 24 - 28, 1990 - Orlando, Florida

Mauricio Breternitz Junior
ECE - Electrical and Computer Engineering Department
CMU - Carnegie-Mellon University

I attended the 27th Design Automation Conference with the aid of a travel grant from SIGDA. This report discusses the aspects of the conference that I found interesting, the sessions on high-level synthesis and the exhibitor's booths. Due to my research interests, this report focuses mostly on the aspects of the conference dealing with high-level and behavioral synthesis.

It was interesting to notice the progress on high-level synthesis techniques. Of particular interest to me was to observe how results from a well-established research area, such as compilation for fine-grain parallelism, may be applied to enhance design tasks. A paper by researchers from U.C.Irvine introduced DAC attendees to the VLIW (Very-Long Instruction Word) compilation techniques of Percolation Scheduling and Pipeline Scheduling. The paper described current status of VLIW compilation techniques, and illustrated their use as a scheduling technique for behavioral synthesis. In particular, loop parallelization techniques such as Software Pipelining provide a powerful mechanism, which in some situations is capable of finding optimal parallelism among loop iterations. Finding parallelism among loop iterations is a hot topic for CAD researchers, as indicated by the best papers from the previous year's DAC.

Another interesting paper introduced Path-Based scheduling, proposed by researchers at IBM. The technique schedules operations from a control-flow graph in an attempt to find a minimum number of control steps for each possible path of execution, while satisfying constraints of data dependency, resource allocation and pipelining characteristics of the operators. Experiments of the technique with High-Level Synthesis benchmarks showed its practical feasibility. I had opportunity of discussing with the researchers an interesting outgrowth of this research: its possible use as a VLIW compilation technique, due to the ability of handling pipelined operators. With this in mind, the papers mentioned above compose an interesting example of symbiosis between research areas.

I presented the paper titled "Architecture Synthesis of High-Performance Application-Specific Processors". It describes a methodology to perform (board-level) design of processors dedicated to the high-performance execution of to a single task. High-level source code for the task serves as the processor specification. High-performance VLIW compilation techniques convert the high-level code into highly parallel microcode which serves as an optimized processor specification. Efficient hardware allocation is done with the aid of graph-coloring techniques. Interesting comments from the session chair highlighted the relationship between this research and traditional techniques for board-level design. In particular, board designers use a flow-chart method to detect parallelism and manually generate microcode, a task which is automated in this methodology.

I had a good experience participating in the University Booth as an Exhibitor. The booth provided the capability of demonstrating a working version of software to other researchers in the area and industrial visitors. This made hands-on experience possible, with accurate exchange of of information. In many cases this stimulated in-depth discussion.

Most of the industrial exhibitor's booths had colorfully printed posters and professional publicity specialists making presentations. The quality of information and demonstrations was good in general. Unfortunately in my opinion, some exhibitors overly enhanced the entertainment and show-biz aspect of the displays, and thus actually restricted opportunities for appropriated technical information exchange.

Report on Participation at DAC '90

Joseph S. Lis
Dept. of Information & Computer Science
University of California, Irvine

The 27th Design Automation Conference provided me the opportunity to view the current state of the art in design automation in both industry and academia. Since my research involves high level synthesis, and in particular the use of the VHSIC Hardware Description Language (VHDL) for synthesis, I was particularly interested in the exhibits and technical talks which involved the use of VHDL.

There were several technical sessions which presented information of interest to me. Session 5: New Scheduling, Allocation and Mapping Techniques, Session 9: Data Path Optimization Algorithms, Session 25: Scheduling Algorithms for High-Level Synthesis, Session 29: Data Path Synthesis presented the application of several mathematical techniques such as linear integer programming and bipartite weighted matching to the major subtasks of high-level synthesis. Another common theme of these sessions was the simultaneous solution of the resource allocation, scheduling and resource binding design tasks so that the effects of decisions made during one phase on the other phases are considered.

Session 1: HDL Validation and Intermediate Format, Session 24: Object-Oriented Approaches and Session 28: Standards, Openness and Design Environments in Electronic Design Automation addressed the issues of frameworks for modelling the functionality of designs to be synthesized and the integrating design tools. It was interesting to learn of the methods presented to deal with the sophistication of design tools and the vast amount of data required to represent a design.

Several commercial tools for simulation and synthesis from VHDL were displayed on the exhibit floor, indicating the acceptance of VHDL as a common hardware description language. Vendors stressed the importance of a common user interface for their various design tools. In addition, the University Booth provided informative demonstrations of current work at universities such as Carnegie Mellon, USC, UC Berkeley and Irvine, Penn State and others. This booth offered the opportunity to view implementations of the ideas presented in the talks, provided exposure for some new work in progress, and allowed for interaction between peers in the academic (as well as industrial) community. I hope that SIGDA continues to support this worthwhile effort.

I would like to thank SIGDA for making it possible to attend and participate in DAC '90.

REPORT on the 27th Design Automation Conference

Andrew Lim
Computer Science Department
University of Minnesota
Minneapolis, Mn 55455

This year the 27th Design Automation Conference was held at the Orange County Convention Center in Orlando, Florida from June 24 to June 27, 1990.

This was my first conference attendance. Naturally, I got to see and learn alot. It presented me with opportunities to meet with researchers in many areas of CAD on VLSI and the chance to acquaint myself with people in the industries and their latest CAD products.

The conference was organized into 43 sessions with 125 papers. Most of the papers seemed very interesting. Since, I am in the area of physical design, most of the sessions that I attended were on physical design. Below is a brief note on some of the sessions.

Session 2, on probabilistic techniques in placement : annealing and its competitors is interesting. Since such algorithms are very much dependent on implementations and fine tuning, it is best that such programs are made available easily to anyone to facilitate fair and accurate comparisions. It will also save researchers' time in implementing algorithms of previous works.

Session 6, is on timing driven layout. Various techniques were used to do the layout inorder to minizing the longest path in the circuit. I found the paper by Ichiang Lin and H.C. Du interesting as they tried to unified timing and geometric constrains into geometric constrains.

In session 10, on issues in floorplanning, I found that the optimal algorithm obtained by Wang and Wong from Austin interesting. They presented some pruning procedures that will speed up their algorithm tremendously.

Finally, I would to thank SIGDA for awarding me the travel grant to attend the conference. I am sure that this experience will help me in many ways in my research activites, and broaden my perspective in this area.

27th DAC Trip Report
Binary Decision Diagrams in Design Automation

Karl S. Brace
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Carnegie Mellon
Pittsburgh, PA 15213

A Binary Decision Diagram (BDD) is a graph data structure which represents a Boolean function in canonical form. Although a canonical representation of a Boolean function implies a solution to many NP-hard problems, and thus must in the worst case be exponential in time, the BDD representation manages to avoid this worst case behavior for many practical applications. In many cases the formation of BDD's and operations upon them prove very fast, but memory use is still a significant concern for those functions which are not so easily represented. The identification of equal functions and tautological functions is trivial once a BDD for a set of functions is formed, and many other operations which are hard in other representations are relatively easy in a BDD.

The interest in BDD's in design automation has increased dramatically recently, as demonstrated by the growing number of papers about BDD's and many more papers which mentioned BDD's. Recent advances in design and implementation have made BDD's more practical than ever. The paper "Efficient Implementation of a BDD Package", which I wrote with Richard Rudell and Randal Bryant, described a reusable BDD package with good speed and superior memory performance, both in terms of raw memory use and in terms of user control over memory use. The paper "Shared Binary Decision Diagram with Attributed Edges for Efficient Boolean Function Manipulation" by Shinichi Minato, Nagasi Ishiura and Shuzo Yajima at Kyoto University presented experimental results of several previously untried enhancements to the basic BDD structure with good speed performance.

The manipulation of Boolean functions is a very common operation in design automation, and BDD's are being used more and more to support or replace other representations. BDD's are proving useful in applications such as logic verification after optimization transformations, formal verification of hardware using symbolic switch-level simulation, translation of high level logic constructs to hardware in logic synthesis, and almost any application which requires identification of equal Boolean functions given ordinary logic networks or sequences of logic operations. Operations which are trivial in a BDD are the identification of Boolean equivalence between 2 functions and testing a function for tautology or satisfiability. It is efficient in a BDD to test 2 functions for logical implication, which can be useful in logic optimization, and to find an assignment of variables which satisfies a function, which can be useful in test generation.

I am sure we will see this increased use of BDD's in design automation continue for some time.

Report on the 27th Design Automation Conference

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cloutier@ece.cmu.edu

July 11, 1990

I would like to thank SIGDA for the travel grant that simplified my attendance at the 27th DAC. I find the real benefit of attending conferences is the face-to-face discussions that are possible with the many other researchers who attend the conference. I found this especially true this year because I presented a paper (titled "The Combination of Scheduling Allocation and Mapping in a Single Algorithm") and so I was able to discuss my ideas with many more people that I might otherwise have met.

I think the second most important feature of attending conferences is the renewal of old contacts. It was interesting to learn the current status of research in the area of behavioral synthesis at industrial locations. Being at an university I sometimes have the impression that the current research can be quickly integrated into CAD systems. After discussions with several of the vendors and some former co-workers I found that the integration is not nearly as fast as I had originally thought.

This year I took the opportunity to attend the SIGDA business meeting on Sunday evening. If you are reading this report then you must review the SIGDA Newsletter in detail. By doing so I think that you get a very good update on current activities of the SIG. I found that much of the information presented at the meeting had also been discussed in the Newsletter. The meeting itself provided a chance to put faces with the names, and to discuss participation in future projects of the SIG.

The University booth was impressive this year, a very professional setup. Also on display was the SIGDA CD-ROM Project, while the demonstration system only contained last year's DAC proceedings it provided an introduction to the potential uses of such a system.

Report on the 27th Design Automation Conference

Kevin Chung

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I would like to thank SIGDA for the travel grant that enabled me to attend the 27th Design Automation Conference held June 24-28, 1990 in Orlando, Florida.

I was particularly interested in going to DAC-27 because I was an author of the conference paper, *Chortle: A Technology Mapping Program for Lookup Table-Based FPGAs* by Bob Francis, Jonathan Rose and myself. Attending the presentation of papers at a conference was a novel experience and it was also stimulating to meet and exchange ideas with other researchers. The presence of commercial exhibitors also provided a good opportunity to find out what was going on in the CAD industry.

I found the papers presented in the session that contained our paper (session 37 - *Decomposition and Partitioning in Logic Synthesis*) the most interesting. The most relevant paper was one entitled, *Logic Synthesis for Programmable Gate Arrays*. This paper described a tool that performed logic synthesis for Xilinx 3000 parts. This paper was interesting because Xilinx parts are lookup table based field programmable gate arrays and our paper was about a technology mapper for lookup table based architectures. The other papers in our session were *Corolla Based Circuit Partitioning and Resynthesis* and *A Unified Approach to the Decomposition and Re-Decomposition of Sequential Machines.*

The panel discussion on *The Impact and Evaluation of Competing Implementation Media for ASIC's* was interesting since it focused on programmable gate arrays.

The Birds of a Feather meeting about the CD-ROM project was constructive and interesting. I believe that the CD-ROM database will be very useful for CAD researchers and my department is fortunate enough to be an evaluator for this project.

In summary, I enjoyed the conference and am glad that I was able to go.

Report on the 27th Design Automation Conference

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chcho@vtvm1.cc.vt.edu

The 27th Design Automation Conference was held in Orlando, Florida, June 24-28, 1990. I had two things to do at the conference. First, I attended a technical session (Session 1 - HDL Validation and Intermediate Format), where the paper ("The VHDL Validation Suite") of which I am a coauthor was presented. The paper introduces a test suite which can determine whether a VHDL tool completely and correctly implements the IEEE standard VHDL language. Second, I demonstrated a CAD tool called BTG (Behavioral Test Generator) at the university booth. BTG automatically generates test vectors from behavioral VHDL descriptions of digital circuits. I would like to thank the attendees who showed great interest in it and gave me some invaluable comments which could be reflected on my dissertation. The university booth was well organized and featured an academic environment in the huge exhibition area.

Since my major interest is in VLSI testing, I attended a few related technical sessions and a panel session (Session 20 -Testing Strategies for the 1990s). It was notable that people use **binary decision diagrams**[1] in various areas (testing, verification, and boolean function implementation). The panel members were optimistic about the testing of VLSI circuits, especially of sequential circuits. Their predictions were fresh and fascinating.

I also attended many exhibitions, especially of VHDL tool vendors. The VHDL tools had the following common points:

- multi-window graphic system
- facilities for easy editing
- interface with existing simulation tools
- synthesis and test generation capability

I felt that VHDL tools would be required in every phase of VLSI design in the near future.

It was a real pleasure to attend the conference. I would like to thank SIGDA for providing me a grant to attend it.

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[1] Sheldon B. Akers, "Binary Decision Diagrams", IEEE Trans. on Computers, Vol. C-27, No. 6, pp. 509 - 516, June 1978.

DAC'90 Trip Report

Cho Woo Moon

Dept. of EECS
UC Berkeley
Berkeley, CA 94720

This year's Design Automation Conference featured a lot of papers on performance and testing issues. This is a big change from the previous years, in which area minimization was the main issue. The session on **Timing and Routing Optimization in Synthesis** had seven papers on improving the speed of synthesized logic circuits. These papers presented techniques at various levels in the design process for speeding up circuits, and showed very promising results. As for testing, two of the three best paper awards went to papers dealing with testing: one was about generating test patterns for large sequential circuits (*Sequential Test Generation at the Register-Transfer and Logic Levels*) and the other was about synthesizing a circuit which is fully testable for various testability criteria with small area overhead (*Synthesis and Optimization Procedures for Robustly Delay-Fault Testable Combinational Logic Circuits*). The trend towards performance and testing reflects the responsiveness of the present research efforts on the real needs of the industry.

Another interesting thing that I noticed was the surge of interest on logic representation called the "Binary Decision Diagram (BDD)". By using BDD's, very large functions, which could not be handled with conventional representations, can now be represented and manipulated. The verification techniques based on BDD's seem very promising for VLSI circuits.

In short, I enjoyed the conference and I thank SIGDA for making this trip possible.

Report on DAC-1990

Gani Jusuf

Department of Electrical Engineering and Computer Sciences,

Electronic Research Laboratory,

University of California, Berkeley CA 94720.

The 27th ACM/IEEE Design Automation Conference was held on June 24-28, 1990 at Orlando/Orange County Convention Center in Florida. The technical sessions were organized in four parallel sessions : physical design, test/verification, synthesis and panel discussion. A total of 125 technical papers were presented over the three day period.

I attended mainly the physical design sessions because of my research area. There were several interesting papers in floorplanning, compaction, and performance constrained routing. There was an excellent paper describing a one-dimensional compactor which simultaneously compacts the contents of all the cells of a layout hierarchy without changing the hierarchy by David Marple in session 22.2 titled "A Hierarchy Preserving Hierarchical Compactor." I also attended several selected presentations on object-oriented approaches, a tutorial on symbolic simulation and a panel discussion on the impact and evaluation of competing implementation media for ASIC's.

Because the sessions were run simultaneously, I had to select which presentations to attend. Often I found myself running from one presentation in the physical design session to another presentation in a different session. I wish I could sit and listen to many interesting papers and discussions which ran simultaneously. In addition to the technical presentation, I found the vendor exhibitions and demonstrations very interesting and useful in that it provided the appreciation of what people are doing in the industry.

Overall, my attendance at the 27th Design Automation Conference has been a very useful one. I hope the organizers can keep up their superb work for years to come. Finally, I would to thank SIGDA for providing the travel grant which made my attendance at DAC-1990 possible.

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Report on DAC-90

by

Nikolaos A. Kyrloglou

The 27th ACM/IEEE Design Automation Conference (DAC-90) was held at the Orlando/Orange County Convention Center in Orlando, Florida, from 24th to 28th June 1990. The Conference attracted attendees mainly from the USA; however other countries were also represented by researchers. More than 130 papers were presented in 3 parallel sessions. Panel sessions served as a meeting point to discuss topics of interest and debate in the field of Design Automation.

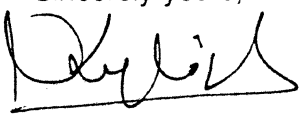
I am a Ph.D. student at the Microelectronics Laboratory of the Dept. of Electrical Engineering of the University of Patras, Greece, and my main interests include the design of CAD tools and ASICs. We have produced some module generators for specific circuits under a custom made design environment which have been accepted for publication by international journals.

Since I am from a small country, where Microelectronics recently started developing, there are few people working in similar areas as mine. It is thus inspiring to meet people from other parts of the world sharing the same research interests. Thus at the conference I made professional contacts with fellow participants working in similar areas as mine and we exchanged ideas and views on various topics. I found the areas of Synthesis and Physical Design of particular interest to me and I attended most sessions. Of great interest were also the two tutorials on Cell Synthesis and Symbolic Simulation which gave a general view of their respective topics. Some panel discussions provided an interesting aspect of how various people view a topic.

Another interesting part of the Conference was the Technical Exhibition that took place in the Conference Center. We had the opportunity to see various CAD tools and computers and to test and compare products from different companies. All this added to the excitement of being there, at this outstanding Conference.

At this point I would like to thank SIGDA one more time for providing me with a travel grant and giving me thus the chance to attend this conference.

Sincerely yours,



N. A. Kyrloglou

July 24, 1990

Patrick Hefferan
SIGDA Editor
1681 Princeton Ave.
St. Paul, MN 55105

Dear Mr. Hefferan;

Please allow me to add my congratulations to everyone who was involved in coordinating the DAC 90 Conference. Over many years I have attended a large number of conferences, and have been in charge of the program as well as proceedings for the NEC held in Chicago each year. DAC puts them all in the shade. Finest, and best organized, I have ever attended.

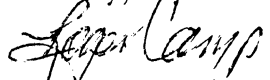
First, I would like to single out the Sunday corporate presentations as being especially important to me personally. As a neophyte in the DAC area it was an excellent way to catch up on the true state of the art, without having to expose my fundamental ignorance at each and every booth until later. I only wish that I had been able to attend at least two at a time out of the four presented. By the relative attendance at some it was possible for me to estimate their perceived importance.

Second, I have previously contacted many of the suppliers represented at DAC by mail and found most of them unwilling to provide much assistance to universities. The $40,000 price tags and up are a great deterrent to a department whose annual equipment budget is around that number. To my delight I found by visiting all booths there were plans by most of the larger suppliers to provide "university packages." This has proven by one supplier of Pspice to be an immense marketing tool, and we can all hope that others will see the same opportunity.

Third, I would like to offer the organizers of DAC 91 the support of the Computer Science Department at Cal Poly. It would be a pleasure to contribute by means of student and faculty labor at any level which might be deemed helpful. Many Computer Scientists have degrees in mathematics, and it is my plan to try to also infect many of them in my department with this DAC virus.

Without this travel grant I would have been unable to attend, and would have missed out on the largest meteor to hit the Electrical Engineering scene in many years. I hope to be a part of this and am working toward introducing this material into our undergraduate and graduate curriculum in the coming months.

Sincerely,



Roger Camp, Chairman
rcamp@calpoly.polyslo.edu

Report on DAC-90
June 24 - 28, 1990
Orlando, Florida

Wei Chen
Department of Electrical and Computer Engineering
New Jersey Institute of Technology
University Heights
Newark, NJ 07102

This year's DAC conference was held between June 24 - 28 in Orlando, Florida. The conference had 43 sessions including 5 panel sessions in which 137 papers were presented. The papers can be categorized into three major areas: logic and RTL level synthesis, VLSI physical design automation, and test and verification. My area of interests in design automation is synthesis and synthesis for testability. Therefore, I attended most of the synthesis sessions and a few of the test and verification sessions.

In comparison with the previous DACs, this year we saw a dramatic increase in the number of papers presented in the area of synthesis both at the logic level and the RTL level. There were some interesting papers dealing with scheduling and allocation algorithms. Ku and Micheli reported a scheduling algorithm that supports unbounded delays specified by users. Cloutier and Thomas presented their synthesis algorithm which combines scheduling, allocation and mapping into a single algorithm so that the interactions among these three steps are taken into account in order to reduce cost. A very interesting paper given by Potasman et al presented a new approach of synthesis based percolation. The algorithm can handle conditional jumps, loops and multicycle pipelined operations.

In the areas of testing and design for testability, an excellent panel session on testing strategies for the 1990's was organized. Although each panelist gave their own perspective on future trends in testing and design for testability, a great deal of debate surfaced again between the "traditional" testing methods, such as scan and partial scan, and methods through synthesis. Devades and Keutzer gave an excellent paper which illustrates a design method that can guarantee any chips to be fully path delay testable.

As a whole, I found this year's DAC to be very successful, particularly in providing a venue to exchange recent research results. I believe we will see a great deal of work and interesting developments in the area of high level synthesis in the future.

At the last day of the conference, I also attended a one-day tutorial on high level synthesis. It was a very well organized tutorial and clarified a number of questions I had.

Finally, I would like take this opportunity to thank SIGDA for providing me with the travel funds to attend this year's Design Automation Conference. It was certainly a very successful and worthwhile event!

27th DAC Trip Report

Robert L. Blackburn
Department of Electrical Engineering
Thornton Hall, University of Virginia
Charlottesville, VA 22903

The 27th DAC was as successful as ever. Both technical sessions and exhibitions provided useful information about the state of the art in design automation. The increased number of papers on high level (behavioral) synthesis in the technical sessions was of particular interest.

One paper of special interest was "The VHDL Validation Suite" presented by James Armstrong of Virginia Tech (page 2 of the Proceedings). The announcement that VHDL validation suite will be made available to the public in the fall of 1990 was particularly good news. Such a suite will provide tool developers such as myself a standardized means to gage the accuracy and completeness of the way in which they process VHDL specifications.

Other papers of special interest included "An Intermediate Representation for Behavioral Synthesis" (page 14) presented by Nikil Dutt and "Abstract Data Types and High-Level Synthesis" (page 680) presented by Gregory Whitcomb. These and other papers were very pertinent to my current work in synthesis and design representations.

One of the most interesting and exciting items on the exhibition side was not a CAD tool or workstation, but rather a library research tool. SIGDA and the DATC demonstrated their CD-ROM project in the University booth. The goal of the project is to record almost all relevant CAD literature on a set of CD-ROMs and create software to be used to search and read through the material. The demonstration disk included only the proceedings of the 26th DAC, but the final project is expected to include all DAC and ICCAD proceedings, all of the SIGDA newsletters, and IEEE Transactions on CAD. The demonstration was quite impressive in the searching capabilities and graphic information it provided. All material is being recorded both as page images to provide an exact replica of the original and as an ASCII text stream to provide for easy text searching. Anyone needing to research a topic in the field would benefit greatly from having such a resource at their finger tips.

I would like to express my appreciation to SIGDA for providing the funding that made my attendance possible.

Alexander Saldanha
Computer Science Division
EECS Department
207-166 Cory Hall
Berkeley CA 94720

Dr. Patrick Hefferan
1681 Princeton Ave.
St Paul, MN 55105

Dear Dr. Hefferan:

The 1990 Design Automation Conference was held in Orlando, Florida. I focussed my attention on the technical sessions in logic synthesis, verification and timing optimization.

In one of the synthesis sessions results were presented that demonstrate that Boolean methods for logic optimization allow further improvements in circuit area over what is already obtained using algebraic techniques. In another session the relationship between the testability and delay of logic circuits was explored with consideration for area as well. The author presented a paper which described an algorithm guaranteeing complete single stuck-at-fault testability without any performance penalty while another paper described synthesis approaches to completely delay-fault testable circuits.

The panel on testing strategies for the next decade provided an interesting debate on the direction for future work in the field. While it was made clear that through conventional test pattern generation approaches the testability of circuits has been enhanced a strong case was made for exploiting synthesis in obtaining highly testable circuits. A new technology for significant quality and speed improvements in testing was also claimed.

In the verification session the exciting new representation of Boolean functions by BDD's was the main focus and algorithms to manipulate and aplly these representations were described.

Delay optimization is the primary criteria in logic optimization. While in the past few years there have been significant advances made in area optimization, the progress in delay optimization has not kept pace. At the DAC, however, this trend was reversed by the extended session on timing optimization. New ideas and algorithms for reducing the delay of networks and layouts were presented.

Besides the technical sessions the highlight of the DAC was the exhibitions of the CAD industry. Clearly, the attention of a lot of the industry was focussed on high level synthesis and logic synthesis tools to aid in the VLSI design process.

Sincerely,

Alexander Saldanha

Alexander Saldanha

207-123 Cory Hall
U. C. Berkeley
Berkeley CA 94720

August 6, 1990

Dr. Patrick Hefferan
1681 Princeton Ave.
St Paul, MN 55105

Dear Dr. Hefferan:

With the help of the SIGDA travel grant I was able to attend the 27^{th} Design Automation Conference in Orlando, Florida. The conference provided a good opportunity to interact with other people working in Design Automation and to see state-of-the-art design tools and methodologies offered by industrial vendors.

I found the technical sessions on synthesis, testing and verification most interesting. The session on Timing Verification had some interesting papers. It was most illuminating to find out that precharged, unate logic families were the only ones that do not have functional hazards. The use of BDD's (Binary Decision Diagrams) for symbolic timing simulation was also an interesting idea.

From the many papers that referred to BDD's it is quite obvious that this particular data-structure used to represent circuits greatly enhances the sizes of circuits that one can analyse/optimize. A seperate session devoted to BDD's that described new techniques for efficient implementations of BDD's was a good idea. in doing so, a large audience was made aware of the potential of BDD's and will undoubtedly leed to more and diverse applications of this data-structure.

In synthesis, the two most interesting sessions were on delay optimization and testing. The session of delay optimization provided a wide variety of techniques that can be used to improve performance. All the papers dealt with some aspect of the circuit that degrades performance and tried to improve that. It will be intersting to see if some or all the approaches described can be combined to solve the pressing problem of improving circuit timing. Testing sessions and panels described new testing strategies that are very promising. It was heart warming to see synthesis techniques being developed to address testing issues. Techniques to synthesize fully delay-path-testable circuits and irredundant versions of high-performance, redundant circuits look very promising.

I am grateful to SIGDA to have made my attending this conference possible.

Sincerely,

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June 28, 1990

The 1990 Design Automation Conference was held in Orlando, Florida, from June 23 – June 28. There were many interesting papers and I found the technical discussions with other participants very informative.

My presentation was scheduled on Tuesday, June 26th and went smoothly. This was my second presentation in a conference and the experience has been very valuable to me.

Every night after the end of the sessions, researchers got together and discussed the latest advances in design automation of integrated circuits. In the area of Logic Synthesis that I am more familiar with the emphasis has shifted from area optimization to performance optimization and people are looking for methods which can do area and performance optimization at the same time. Partitioning of logic networks into parts that can be handled by logic optimization algorithms is becoming more important.

Binary Decision Diagrams (BDD's) play a key role in Logic Synthesis. One whole session was devoted to this subject. Current research in this area deals with sequential verification and combinational verification of some very hard Boolean networks like multipliers that could not be handled previously.

The combinational logic synthesis (multi-level as well two-level logic synthesis) seems to be maturing and the sequential logic synthesis/optimization seems to be an active research area now.

The panel sessions were not as controversial as I had expected but they brought to light many important issues and problems of current logic synthesis systems.

I found the Exhibit Boot very interesting. The latest software packages and hardware tools produced for design automation were at display. Different companies were advertising their latest products. It seems that a great number of transactions took place during the conference.

In summary, this was a very successful conference and I have learned a great deal from it. I am very grateful to ACM/SIGDA for making this trip possible for me.

Report on the 27th ACM/IEEE Design Automation Conference 1990

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DAC'90 was held in Orlando, Florida, USA from the 24th to 28th of June 1990. I was able to attend the conference to present a paper, with the support of a travel grant from SIGDA.

My main interest was in the use of parallel processing for speeding up CAD algorithms. Most of the papers discussed the use of shared memory multiprocessors. Hung et al. discussed parallel circuit simulation algorithms for the shared memory Cedar machine, and recorded speedups of 8.7 using 4 clusters of 4 processors. Yang discussed parallel direct method circuit simulation for the Alliant FX/80, and recorded average speedups of around 4 using 8 processors. Subramanian and Zargham discussed parallel implementations of demand driven logic simulation on a Sequent Balance multiprocessor. Brouwer and Banerjee discussed a parallel global routing algorithm implemented on the Encore Multimax that showed speedups above 6 using 8 processors. Carlson and Rutenbar discussed parallel algorithms for VLSI Mask verification on the massively parallel Connection Machine.

Bill Joy presented an interesting keynote address and predicted that user interface code would become increasingly important in the next generation of system software.

The panel discussions were well attended, and provided a good forum for the exchange of opposing points of view. I found the discussions on distributed computing and implementation media for ASICs to be the most interesting. I hope transcripts of some of the panel discussions will be printed in future SIGDA newsletters.

I found the exhibitions by software vendors to be worthwhile. I was able to get an appreciation of the directions that industry are taking in developing CAD software, which are not immediately apparent from looking at the technical papers in recent conferences and journals. The emphasis was on getting software tools and hardware platforms from different vendors to work together, through such schemes as the CAD Framework Initiative. There were some good examples of automatic synthesis software that included structures for circuit testing in the resultant circuit layout.

Overall the conference was well organized with ample opportunity to meet with fellow researchers. I would like to see name tags with larger print to help in identifying people in future years, in addition to the credit card size name tags designed to allow vendors to take an imprint for their mailing lists.

Report on the Design Automation Conference (DAC'90)

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First of all, I would like to thank the executive committee of SIGDA for providing me with a grant to attend the 27th DAC held between June 24-28 in Orlando - USA.

Besides the technical content of the conference, one of the surprising points is the very low level of European representation : according to my approximate statistics, only 10 papers were coming from Europe (USA : 92, other 25). We can compare these figures with the one obtained for EuroASIC'90 (Paris, France, May 1990) and EDAC (Glagow, Scotland, March 1990) which are two medium-size European conferences. The following figures are obtained, USA : EuroASIC = 15, EDAC = 31, Europe : EuroASIC = 69, EDAC = 79. Results seem to be more balanced in European Conference than at the DAC ; I do not have any comparative figures for the past years but this very low european representation is regrettable.

Concerning the scientific point of view, my points of interest are synthesis and test program generation, more especially from high-level specification. Moreover, I am implied in a European Esprit project about CAD tool evaluation and I am therefore interested in benchmarking.

One, among others, interesting information concerns the VHDL validation suite : this suite which will allow to check the conformity of VHDL tools to the Language Reference Manual will be completed and available in October this year.

Concerning synthesis, many sessions were devoted to both low and high level synthesis and a special session was dedicated to the problem of formal design verification ("Verification of interacting sequential machines" by Ghosh, Devadas,

Newton). Formal verification is an important research area motivated by the increasing use of complex CAD tools in the design process of both combinational and sequential circuits and the inefficiency of exhaustive simulation based approaches (mention here the tutorial on symbolic simulation techniques and applications by R. Bryant).

Concerning test generation, I am mainly interested in Automatic Test Program Generation from high-level specification and an interesting session was dedicated to this problem. One of the main problems in this area is the link between functional and structural (stuck-at) faults. Apart from some results on ATPG for controllers, we do not have a clear idea of the fault coverage resulting from test vectors obtained using ATPG from high-level specification.

The next interesting point during the DAC'90 was the possibility to demonstrate the synthesis tool developed by INPG/CSI at the university booth. We were allocated 3 hours demo times and these demonstrations gave me the opportunity to discuss and present our work to people from both university and industry. Thanks to Casey The for his support before and during the installation.

To end with, let us mention that some interesting IEEE/DASS meetings were held after the DAC and I have participated to the working group on the standardization of the WAVES language.

DATABASE SUPPORT FOR EDA APPLICATIONS: A REPORT ON THE 27th ACM/IEEE DESIGN AUTOMATION CONFERENCE

Orlando, June 24-28, 1990

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July 7, 1990

My area of specialization is the design and development of data base systems for support of non-traditional domains, such as, engineering applications. In the context of object-oriented and semantic database systems, my research has focussed on modeling and design representation problems as well as on design data management. In order to better understand the needs and requirements of design automation applications on database systems, I decided to attend DAC'90. It was my first conference in this field, and it turned out to be a very valuable experience for me.

I was interested in the opinions of both the industrial as well as the academic design automation community on database support functionalities and other enabling technology for EDA. I now believe that the community has recognized the need for such systems. In fact, there were several companies in the exhibition room that specialize in the development of object-oriented databases targeted for design automation applications. One thing that stood out to me from visiting the exhibition halls was the intensive focus on frameworks for system integration. Framework technology includes enabling technologies such as tool integration, a common data base system, easy-to-use user interfaces, and the like. I was therefore surprised about the low number of sessions devoted to enabling technology for design automation: There seemed to be a discrepancy in interest between vendors and the focus of the DA research community.

My primary research interest being in data base management systems, the sessions and panels I attended were mostly in this or related fields. There was only one technical session on this topic, namely, session 8 on *Data Management and Version Control.* A second one (session 24) devoted to vaguely related topics was titled *Object-Oriented Approaches.*

The *Data Management and Version Control* session featured interesting papers on diverse database issues. The first paper presented an automated trace system that keeps a design history of all tool activations as well as the names of the design files used as input and produced as output. This allows for "retracing" if the design data becomes updated, i.e., the time-stamp of the design data is newer than the time stamp of the tool activation in the existing trace. Retracing can be viewed as a limited form of consistency maintenance. The second and third presentations discussed aspects of the Nelsis system. The second paper focussed on the meta-data management subsystem. The authors showed how meta-data can be exploited for framework tasks, such as, concurrency control or hierarchy support. The third paper discussed the user-interface to the meta-data, in particular, a graphical browser. The proposed browser can be used to graphically formulate queries on the meta-data by selecting with the mouse the appropriate meta-objects. A textual representation of the query is then automatically generated. The fourth paper presented an Intelligent Component Database for the automatic generation of components as requested by high-level synthesis tools via a set of parameters. Such a component database is found to be more flexible than a component library typically used for this task. The fifth and last paper presented ideas on design data management in the CAD Framework Initiative (CIF).

In addition to the technical talks there were some very interesting panels, in particular, the panel (session 40) titled *Object-Oriented Databases in Electronic Design: Implementation Experiences.* Unfortunately, there were too many panelists (I recall eight), so that time allotted for the panel ran out shortly after the presentation of the position statements of the panelists. Unfortunately, this did not leave much time for discussion. There seemed to be a general consensus among the panelists that object-oriented databases have shown some success and that they have the potential to meet the needs of the electronic design community. A crucial characteristic required of databases for design, as stressed by all speakers, was *performance.* Most believe that the required level of performance will be reached by commercial database products in the near future. It was also pointed out by Larry Lai (Objectivity) that there is not just one measure of performance; instead there are several possible measures. Examples of performance issues to be considered are graceful performance degradation (working set size), support for certain classes of operations (explicit physical clustering), and the start-up time for reading into main memory only what is demanded rather than the complete design data as done in memory-based databases. This clearly shows that public benchmarks of a great variety are needed in order to fairly evaluate a database system. In addition, electronic design automation vendors suggested that in the long run the development of databases for EDA should take place within database companies rather than that they would try to develop their own in-house products. Database companies have expertise on the efficient management and access of data, and thus will outperform in-house technology. General agreement existed on the fact

that object-oriented database management systems form a solid foundation for a design framework.

I also found the panel on *Standards, Openness, and Design Environments in Electronic Design Automation* very informative. The advantages of standards for users have always been obvious to me; but I was curious about why industry would invest in these efforts. The panel addressed this and other related issues. What tool and system integration does in the small for particular design environments, general standards set for electronic design automation will do for the whole community. In particular, it will allow EDA companies to leverage of the "work" done by other. Companies can focus on the development of special-purpose tools rather than investing repeated efforts into interfacing their products with systems from other vendors. Last but not least, it will provide a foundation for a true comparison of design tool quality, as vendors can no longer hid behind their particular system configuration. Several speakers voiced that standards can get in the way of progress and innovation, if they are being forced upon a community while their understanding of the product is not mature. Most panelists believed that the community needed a few more years of experience with the object-oriented methodology in general and with object-oriented database systems in particular, before one should settle on a standard within this realm. On the other hand, domains that are well-understood, such as, data exchange, will profit from immediate standardization efforts.

I also checked out the CAD Framework Initiative project booth. CFI presented a procedural interface for access to a netlist structure specified on a simple netlist transfer format. The netlist structure was quite simple, i.e., it appeared to be read-only and without hierarchy, versioning, etc. A major accomplishment of the CFI project, however, was to get 18 different vendors to participate and to agree on such a common interface. Each of these vendors invested a couple of weeks to interface one or more of their tools to this procedural interface format. As demonstrated by CFI, successful communication of these diverse tools took place across a five heterogeneous platform network. This is definitely a milestone in setting standards.

The conference has been a rewarding learning experience for me. Many thanks to all who made it the success it was; special thanks also goes to SIGDA for providing me with the travel grant.

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July 17, 1990

Dr. James P. Cohoon
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Dear Dr. Cohoon:

This year's Design Automation Conference was characterized by the establishment of VHDL as a standard tool for both the simulation and design of VLSI circuits. Among the conference exhibitors, virtually every company involved in digital CAE claimed to have integrated VHDL into its design framework. While most of these used VHDL for simulation only, at least one company demonstrated a system for automatically synthesizing logic circuits from certain types of VHDL descriptions.

As VHDL moves into the industrial community, academic research on the language seems to be slowing. This year only three papers were presented describing academic research related to VHDL. One of these papers was strongly industry-oriented, presenting a comprehensive suite of tests for validating VHDL implementations. The other two papers described an object-oriented environment for VHDL designs and a method for performing fault simulation on behavioral VHDL descriptions.

The success of VHDL was the impetus for a "birds of a feather" meeting held Tuesday evening to discuss the definition of a hardware description language for analog circuits. This, however, seems to be a much more difficult problem than the design of VHDL. Everyone agreed that the analog design process is much more *ad hoc* and poorly understood than that of digital design. In fact, the very definition of "analog" was unclear; should a prospective language also be able to model mechanical systems, high-frequency interactions, optical effects, or even quantum-mechanical phenomena? While these questions were left unresolved, three characteristics were suggested as important parts of an analog HDL:

- A method for describing and enforcing conservation laws such as Kirchoff's laws and charge conservation.
- A method for describing the ordinary and partial differential equations that govern analog system behavior. A related issue to this is that many analog systems (e.g. optical) involve more than simple point interactions among variables; interactions that take place over surfaces and volumes should also be representable.
- Support for the hierarchical design and simulation of analog systems. This should include capabilities for top-down design, bottom-up design, and mixed-level simulation.

Thank you very much for your financial support during my attendance at DAC this year.

Sincerely,

Timothy M. Burks

Report on Attendance at the 1990 Design Automation Conference

Joanne E. DeGroat
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In general The Design Automation Conference showed a continuance of trends that have been evolving over the past years. Synthesis and verification continue to be focus areas. However, even with all the work on synthesis, there are still significant limitations on the size and complexity of circuits that may be synthesized. It was pointed out in the panel on "Testing Strategies for the 1990's" that 10,000 gates is about the limit of the best synthesis tools. It is in some ways gratifying that we have reached this point in the evolution of synthesis this quickly, but significant research is still needed if we are to eventually synthesize more than individual chips. Another interesting point that was made is that synthesis research began to mature after digital hardware description languages gained sufficient maturity.

Although not reflected in the technical papers yet, there is interest in a new area, an Analog Hardware Description Language. The presentation in the Birds of a Feather meeting was very informative. Significant thought and work has been in progress on analog HDLs. There are many issues to be resolved as pointed out in this meeting and in a presentation during the Design Automation Standards Subcommittee meetings held Thursday and Friday. One issue is the appropriate levels of abstraction for an AHDL. In the digital domain the levels of abstraction start at the gate (or even transistor) level and move through levels of abstraction to a RTL level and eventually an algorithmic specification. But what are the corresponding levels in the analog domain? An even more important issue is what should they be. In the development of VHDL there were many digital HDL to use as a basis for what to do or not to do. In the analog domain there are only a few tools to use as starting points, the most familiar being SPICE. It will be interesting and exciting to see the developments in this area over the next five years. It will also be interesting to see if the development of an AHDL stimulates the development of synthesis of analog circuits.

For those who did not see the demonstration of the CD ROM project, the prototype system looks impressive. The demonstration system covers the 1989 DAC Proceedings. Various search functions allow the information to be accessed via various keywords, via reference as the references are linked, and so forth. Once the desired article is found, a hard copy of the article as it appears in the proceedings may be printed. To have the entire history of papers in any field available on line is tremendously useful to researchers and designers. More importantly, it significantly reduces the time needed to locate and copy papers on a particular subject and trace references. It will clearly enhance design automation research. SIGDA and DATC are to be commended for this project.

And a final thanks to SIGDA for the support I have received.

1990 DAC Trip Report

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The principal purpose of our trip was to make two paper presentations. The first presentation was in Session 1 on the "VHDL Validation Suite", a set of tests that one can use to determine if a VHDL tool interprets the VHDL language properly. The suite was developed jointly by our research group at Va. Tech and a group of seven companies: CLSI,MCC,Genrad,DAZIX, Silicon Compiler Systems,Vantage, and Zycad. A presentation on the suite was also made to the IEEE DASS VASG meeting. The DASS has setup a study group to determine how best to utilize the suite. Andy Huang of Raytheon (508-858-5727) is chairing the group.

Our second paper presentation in Session 35 dealt with "Behavioral Fault Simulation In VHDL". This paper describes two programs which can be used to perform behavioral fault simulation with a conventional VHDL simulator. The first program, called the fault mapper, creates executable VHDL models with behavioral faults in them. The second program, the test bench generator, transforms a test vector set into a test bench architecture which can be used to simulate the faulty model.

At the University booth we demonstrated two pieces of software, a modeler's assistant program which provides for graphical assists to behavioral model development and a behavioral test generator which develops tests from VHDL behavioral descriptions.

REPORT ON 27th DAC

(Orlando, June 24-28 1990)

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The 27th DAC was held in Orlando, from 24 to 28 June 90. In addition to high quality technical sessions, there were exhibitor presentations and tutorials. Since I come from Europe, the SIGDA travel grant was for me the unique opportunity to attend technical talks on the several topics related to Design Automation, and to visit such an expensive exhibition of CAD tools.

My primary interest is in the topic of Formal Methods for Hardware Design Verification. Formal verification is an on-going research area which seems to be promising as an alternative to exhaustive simulation. It gives a sure framework to prove VLSI circuits, using mathematical methods. To prove a circuit means to show the equivalence between a circuit specification and a particular implementation, or between two distinct implementations given at distinct abstration levels, for all possible inputs and internal states. These last years, formal verification has gaigning acceptance in the designer community. We are working with four teams of distinct countries in Europe, on a ESPRIT BRA project called "CHARME", for Correct HArdware design MEthodology. The aim is to develop a complete CAD tool which allows circuit description in a classical HDL (such as VHDL), the translation of this description into a mathematical formalism, and then the proof using specific tautology prover or general purpose theorem prover. We also intend to define the concept of "design fo verifiability". Also, some industries, such as BULL France, believe in formal verification methods and use them during the design process of commercialized VLSI circuits.

Formal verification methods was pointed out at DAC, since there was one session reserved for test and verification, among the four parallel sessions leading every day. An interesting tutorial on "Symbolic Simulation", by Randy BRYANT, intends to convince all the attendees, even the one not specialized in this area, that formal methods are very efficient to verify combinational cicuits and certain kinds of Finite State Machines. Randy BRYANT has also emphasized that certain concepts used in formal verification, such as Binary Decision Diagrams, can be applied to synthesis or testing.

Among the sessions on formal verification, I want to report the session on Binary Decision Diagrams. These diagrams allow to encode boolean functions in an efficient way and can be used to perform formal verification as well as, for example, during synthesis process. The first paper, "Efficient implementation of a BDD Package", written by R. S. BRACE, R. L. RUDELL and R. E.

BRYANT, describes an efficient way to implement BDDs. All the boolean functions are represented as "if then else" functions and are encoded as ROBDD, using a hash-code table. ROBDD stands for "Reduced Ordered Binary Decision Diagrams": the variables that appear in BDDs are ordered and each node in the BDD represents a distinct function (if there are several identical sub-functions in an expression, they are encoded only once). The second paper, "Sequential Circuit Verification using Symbolic Model Checking", written by J.R BURCH, E. M CLARKE and K.L. Mc MILLAN, shows the use of BDD for symbolic model checking. Model checking consists in the verification of a set of circuit properties. In this paper, properties are expressed using "Computation Tree Logic"; each property and each state transition relation are represented by BDDs. This gives an effective improvement of the previous model checker. The last paper, "Shared Binary Decision Diagrams with attributed edges for efficient boolean function manipulation" written by S. MINATO, N. ISHIURA and S. YAJIMA, gives some improvements on the implementation of BDDs:
- Shared BDDs: insure that two isomorphic sub-graphs do not coexist
- variable shifters: two graphs which do not use the same variables but have the same form are identified identical
- attributed edges: only one sub-graph is represented, even if it is reached by the value 0 or 1.
Furthermore, they have defined a variable ordering based on the topological features of the circuit that gives a significant size reduction. This session was of great interest for me since it gave the state of the art on the implementation of BDDs.

Another session, "Formal methods for design verification", was less technical but illustrated some decomposition principles in order to verify VLSI designs. More specifically, the third paper, "Verification of Interacting Sequential Circuits", written by A. GHOSH, S. DEVADAS, and R. NEWTON gave some ideas about the decomposition and interaction of Finite State Machines. This paper was very interesting for me since I have verified that some problems specific to formal verification, such as the interaction of FSM, occur also in synthesis. I think that the main quality of the DAC is to bring together people involved in Design Automation, designers as well as researchers working in distinct, but complementary, domains.

I want also to mention the tutorials; they allow a non specialist to have a large knowledge on an specific topic, thanks to several talks of great quality. I attend the tutorial on "Parallel Processing for VLSI CAD Application". It was for me of great interest to have an overview of all the CAD tools, and at the same time, an overview of the parallel processing problem, since I am working on the specification and verification of parallel architectures.

I would like to thank the organizers of the conference for an outstanding work, and SIGDA for providing the travel grant. It was of a great value for me to attend this conference prior to defending my Ph. D; it has broadened my understanding of the state of the art both industrial and academic in the domain of Design Automation.

Report on the 27th ACM/IEEE Design Automation Conference held at Orlando Florida, June 24-28, 1990

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July 2, 1990

First I would like to thank SIDGA for providing me with a travel grant which enabled me to participate in the 27th Design Automation Conference and present my paper.

I have found my participation in this conference very fruitful. A number of experts in various areas of VLSI such as Synthesis, Testability, Simulation and Physical Design attended the conference. The sessions and the papers were very interesting and addressed a variety of contemporary problems. Most of the presentations were well attended; even the closing sessions on the final day of the conference were packed. I was very excited to see more than 100 attendees during the presentation of my paper in the last session of the conference.

One of the interesting features of this conference is the richness of the panel sessions. These panel sessions are very useful in that it provides the audience an opportunity to express their opinion freely on some of the contemporary and future issues. There were six panels during the entire conference on issues ranging from Women's Role in Microelectronics Industry to Embedded Software. I will provide a brief report on one of the panel sessions I attended.

The panel discussion on Testing Strategies for the 90's was organized and chaired by S. Vincentelli of University of California, Berkeley. The panel

consisted of T. Gheewala of CrossCheck Technology, S. Devadas of MIT, M. Schulz from Europe, T. Tamama from Japan, V. Agrawal of AT&T, Bell Labs and T. Williams of IBM. S. Vincentelli opened the session by introducing Fault models, Test Pattern Generation algorithms, Design For Testability and Testability Driven Synthesis as major issues of testing in the 90's. Whereas the fully observable CrossCheck architecture provides a new strategy for making the circuits more testable, asynchronous logic testing is still left as an open problem. S. Vincentelli observed that Logic Synthesis is becoming a reality and urged for the need of strong link between testability and optimality of circuits.

The panel members did not concur on a specific test methodology as a technique of the 1990's. T. Gheewala suggested that Crosscheck meets ASIC designers' test needs by provided high fault coverage and zero delay. S. Devadas argued for synthesis and concluded that synthesis will displace test pattern generation and simulation. According to him, deterministic BIST will become popular in the 1990s. M. Schulz presented the European view on Testing and also felt the need for Automated Synthesis linking synthesis and testability. T. Tamama gave the Japan's view by pointing out the need for high speed testing in the 90's. He mentioned that Japan is actively engaged in high speed and high density circuit testing and is also developing E-Beam testers navigated by Expert Systems.

V. Agrawal talked about hierarchical design for testability and addressed Area, Timing and Testability as the three facets of the testability problem in the 90's. T. Williams addressed the question: "To scan or not?". He explained Scan as a requirement and Self-Test and Well-Synthesized Test are the other methodologies of the 90's.

The audience participated very lively and asked the panel to comment on pragmatic issues of testing and the guarantees of testing for physical defects. Though some members of the panel suggested synthesis as a perfect solution to this problem, the audience was not quite satisfied with the solution. In conclusion, logic synthesis appears to be a winner in the 90's but testing complex circuits is still an open problem.

I would like to thank the SIGDA for the travel grant which allowed me to go to the recent Design Automation Conference (DAC). I present here a short report on some of my experiences.

Although my main interest lay in the technical presentations, I found the panel discussions quite interesting for a young CAD researcher, like myself. Specifically, the discussion in the panel on *Integration of Hardware and Software in Embedded System Design* to provide some insight to how professional organizations view CAD and SWE; how they use them, and some of the current problems in the "real world." This discussion of hardware and software integration was well led by W. Lattin of Logic Automation, Inc..

Of particular note was the need assented to by all parties for tools that allow designers to search that grey design space that lies in the area of hardware/software tradeoffs. As systems are developed, there seems to be a design decision very early in the design process that divides the project into two streams: Hardware design, and Software design. A miracle occurs at a stage known as "system definition" and produces this division. Later on in the design cycle, another miracle must occur at a stage called "system integration" which unifies the work done in parallel. All seemed to agree that although this process has worked in the past, due to the changing market place, this practice is becoming inadequate.

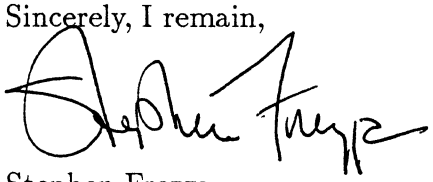
With the observation that any problems found during system integration are prohibitively expensive to repair, there was a clear call for tools to be provided that allow ties to be formed between these two design efforts. These links would be to provide a means for integration problems to be discovered and recovered from early, before recovery involved large amounts of rework. The discussion surrounding these links branched into the areas of methodology, project management, system and sub-system simulation and emulation, all aimed at providing a means of avoiding integration problems.

Another tack was also brought up - that not only should such problems be avoided as the hardware and software developments are occuring, but that there is a distinct need to be able to *predict* where such problems may occur - that is the ability to rapidly develop a system-level model with the ability to model how the system will work (or better yet, *if* their system will work) as expected. This was a call for tools that allow the designer to search the system design space, and evaluate the design under consideration. One panelist coined the phrase "Brain-Aided Engineering," that is the ability of such software to allow the designer to use their brain, and not just push documentation and specifications around, as the current generation of software engineering tools seem to.

These two calls clearly indicate a growing industry need; There are several methods through which they may be addressed, such as changes to the design and simulation methodologies used, or (of particular interest to me) is the development of new abstractions that address the design space, and how to best search it.

I wish to sincerely thank the SIGDA for providing me with the means of attending this conference, and especially Dr. Cohoon for his efforts in coordinating the travel grant program.

Sincerely, I remain,



Stephen Frezza
University of Pittsburgh
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Design Automation Conference 1990

Kaushik De

Center for Reliable and High Performance Computing

Coodinated Science Laboratory

University of Illinois at Urbana-Champaign.

The Design automation conference was held at the Orange County Convention center at Orlando, Florida, from June 24th to June 28th. 125 papers were presented in 43 sessions. Presentations were held in 3 parallel session and in the 4th session, panel discussions were held. I found the conference excellently organized.

Though I have interest in several areas of Design Automation, my area of active research is synthesis for testability and logic synthesis. I have attended the session called "Synthesis for Testability". *Best paper award* winner paper was presented in that session. The content was synthesis of delay-fault testable combinational circuit. The paper presented a method for synthesizing robust delay-fault testable circuit. A paper in the same session showed that redundancy is not necessary for reducing delay and an irredundant circuit can be synthesised from a redundant circuit always which will have delay atmost that of the original circuit.

Another interesting session was on decomposition and partitioning in logic synthesis. A paper was presented on a unified framework and associated algorithms for the optimal decomposition and re-decomposition of sequential machines. Another paper presented on logic network partitioning on the basis of analysis of reconvergence fanout. Partitioned and resynthesized circuits are reported to have fewer literal count than the original circuit. The partitioning scheme seems to improve the performance and testability of the circuit.

Session on Boolean Methods was very interesting. A new technique of boolean resubstitution with permissible functions and ordered binary decision diagram was presented in the paper from Fujitsu Limited. Use of observability and external don't cares in simplification of multi-level network is discussed in a paper. In that paper an algorithm for computing subsets of observability don't care was presented. Another interesting paper in that session reported some experimental results obtained when experimenting with entropy of the

system.

I had oppotunity to attend sesions related to probabilistic technique of placement, ideas in testing, timing and routing optimization in synthesis, testing using functional models etc. I also visited booths of some companies such as Cadence, Synopsys, Mentor Graphics, Texas Instruments, IBM, Hewlett Packard etc.

I am most pleased with the opportunity to meet with so many active researcher in the design automation community, both from industry and academia.

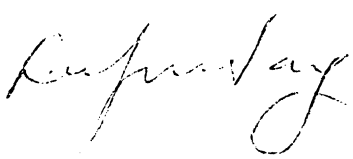
Report on DAC'90

Gueesang Lee
Department of Computer Science
The Pennsylvania University
University Park, PA16802

I would like to thank SIGDA for granting me travel funds to participate in DAC'90 in Florida. It was a good experience for me to join the University Booth and to see the exhibition and paper presentations which show the most up to date technology in VLSI design. I was quite surprised to know that the companies and the universities are very actively working on the area of computer aided VLSI design. In the paper presentations, the paper authored by S. Devadas and K. Keutzer was the most impressive one to me. My primary concern is the synthesis methodology for improved testability. I think the paper presents a good way of getting dely fault testable circuits, even though the size of the synthesized circuits may quite small to be practical. The technique presented in the paper maight be employed in other synthesis methods.

Again I appreciate that I could have an opportunity to be in DAC'90.

Sincerely,



Gueesang Lee

REPORT : The International Conference on CAD 1990

Liren Liu

Computer Science Department

University of Minnesota

MPLS, MN55455

The International Conference on CAD 1990 was held at Convention Center in Orlando, Florida, from June 24 to June 27, 1990.

There were 43 sessions and 125 papers presented. I was interested in testing and timing verification of VLSI design. Mostly, I attended Synthesis Sessions and Test & Verification Sessions.

There were four papers relevant directly to Timing Verification. K.A. Sakallah et al., from University of Michigan, presented an LP-based algorithm to obtain the optimal cycle time for latch-controlled synchronous digital circuits. A.R. Martello et al. in their paper, "Timing Verification Using HDTV", showed that a hard design timing verification provides an overview of a system design for verifying the consistency of timing specifications for digit circuits.

McGeer and Brayton derived a dynamic programming procedure to find the longest dynamically sensitizable path in a precharge/unate network and proved that the tight criterion of dynamic sensitization satisfies robustness requirement on such network. This was their further work based on the viability function which had been introduced in ICDAC 89.

The forth paper was presented by N. Ishiura et al. from Kyoto University. They encoded the cases of possible delay values of each gate by binary values and simulated all the possible combinations of the delay values by means of symbolic simulation. This technique can identify hazard, the most tough problem in timing verification and delay fault testing. It gave us accurate simulation results without pessimism .

Many new concepts and new ideals, such as Shared Binary Decision Diagram (S. Minat et al.), Floorplan Area Optimization (T.C. Wang, D.F. Wong), Robust Delay-fault Test (S. Devadas, K. Keutzer), and etc. were also interesting to me. I am going to study these papers more carefully after this Conference.

The panel sessions were very helpful too. I enjoined Session 30 about symbolic simulation presented by Prof. R.E. Bryant who brought me from the fundamental concepts up to date on this exciting field.

In exhibition booths, the major companies involved in CAD provided detailed information about their latest products and developments. Even in the bus for the Swamp Party, I learned a lot by talking with Mr. Steve Boosie, who is working for Texas Instruments currently.

I would like to thank the organizers of the Conference for their successful job, and also to thank SIGDA for providing me the student travel grant and enabling me to enjoy the meeting.

I am sure that the attendance of this Conference will help me very much in my future research activities. I am looking forward to participating 1991 ICCAD.

Liren Lin

The 27th ACM/IEEE Design Automation Conference

Larry G. Jones

Department of Computer Science
University of Illinois at Urbana–Champaign
Urbana, Illinois 61801

Having a joint trade show and technical conference makes the DAC a very informative and diverse conference. The opportunity for interaction between industrial and academic researchers clearly enriches both worlds, keeping all of us in contact with real problems, current successful approaches, and directions for new solutions.

Organization, participation, and interest in the University Booth has improved each year. This year there was a marked improvement in the size of the booth, the hardware available, and the position on the trade show floor, giving researchers, including myself, excellent exposure to the design automation community. Many universities demonstrated their ongoing research, giving us a taste of the future of design automation. Demonstrations of the SIGDA CD–ROM project at the University Booth clearly showed the progress made and the potential benefits of having an online database of DA research papers.

The DAC was highlighted by a wide variety in the technical sessions and panel discussions. Of particular interest to me were the sessions devoted to symbolic simulation and the Binary Decision Diagram (BDD) representation.

I would like to thank all those involved in the organization of the University booth for doing such a splendid job. I would also like to thank SIGDA for providing me with a travel grant and making my participation possible.

27^{th} Design Automation Conference - 1990

Kayhan Küçükçakar
Department of Electrical Engineering – Systems
University of Southern California
Los Angeles, CA 90089-0781

27^{th} Design Automation Conference was held in Orlando, Florida during June 24-28, 1990. I had the privilege of attending DAC-90 as an author. I'd like to thank SIGDA for the award of a travel grant to attend DAC-90. DAC was a good combination of technical sessions with 125 papers, more than 120 vendor exhibits, panel sessions and tutorials. DAC-90 provided a unique environment for information exchange between the professionals in the field.

There were 6 sessions devoted to behavioral synthesis. Papers showed overall improvements in the quality of automated designs as well as drastic reductions in run-times of algorithms presented. In traditional high-level synthesis, smaller design tasks used to be sequentially executed, mainly due to the high complexity of the overall problem. This year, efficient methods were presented to concurrently perform some of these design tasks by neither exploding the run-time complexity nor lowering the design quality.

Another important aspect of presentations was that there was more emphasis on timing constraints in layout generation as well as higher levels.

The DAC Conference

It was an interesting experience attending the DAC conference from June 25th through June 27th in Orlando. The keynote address by Bill Joy of Sun Microsystems gave a glimpse of the future of workstations and the immense power that will be available to individuals from the workstations of the future. The comments on open systems were also well taken. The point was that, open systems allow small groups of ingenious individuals to add significantly to the advances in technology, and that new ideas frequently come from the inspirations of single individuals or small groups. Therefore, the concept of open systems is inherently useful in achieving rapid technological advance.

The displays by the various exhibitors were fascinating, to say the least. They could not be covered in a single afternoon, and the interchange of ideas was very useful. There was a wide variety of hardware and software presented by numerous vendors. Several new work stations were on display for trial use. There were numerous demonstration programs running, as well as experimental displays on various subjects, such as superconductivity.

Difficult choices had to be made in determining which sessions to attend. The sessions on timing verification and electrical simulation were particularly interesting. The talks were well presented and gave a good insight into the speaker's work. Sitting through the sessions stimulated the formation of new ideas and new approaches to existing problems.

In several ways the conference was an event not to be missed. It was a very useful platform for the interchange of ideas and the stimulation of the minds of those who attended. It was a place to meet and speak with new people as well as with old friends. It was a place to see the latest in hardware and software. Those who were responsible for putting on the conference are to be commended for its high quality.

Finally, to top off the event, my University and myself were fortunate to receive one of the SIGDA scholarships given at the opening session. For this honor, I would like to thank the members of the ACM SIGDA. The award is greatly appreciated.

Donald A. Joy
Dept. of Elect. and Comp. Engr.
University of Massachusetts
Amherst, Massachusetts

27th Design Automation Conference - Trip Report

Yen-Chuen Wei

Department of Computer Science and Engineering
Mail Code - C014
University of California, San Diego
La Jolla, CA 92093

The 27th Design Automation Conference (DAC-90) was held from June 24 to 27, 1990 in Orlando, Florida. There were about 125 technical papers presented during the three day period. In addition to the technical papers, there were several panel discussions and tutorials.

My research interest is mainly on placement and routing algorithm. In the conference, I went to several technical sessions of Physical Design. From these sessions, I found out that one major emphasis of this year's program was the use of CAD to increase the performance of the circuits. For example, one session was Probabilistic Techniques in Placement. Simulated annealing was challenged by its competitors, such as simulated evolution and other stochastic methods. The objective is to find better partitioning and/or placement results to improve the system performance. Another session was Timing Driven Layout Techniques. These techniques aimed for high speed VLSI designs, including placement, floorplanning, and global routing considerations.

I also participated a very interesting panel: Standards, Openness, and Design Environments in Electrical Design Automation, chairmaned by A. R. Newton, with panelists from the CEOs of major CAD tool design companies. In order to remove the barriers of tool integration, they all agreed on developing a standard interface so that many related tools provided by different vendors in different workstations can work together.

The most successful feature of every annual Design Automation Conference is to combine technical sessions with industrial exhibition. There was no exception this year. Over 100 exhibitors introduced their major products and latest developments. The exhibition provided us up-to-date information and new trend in Design Automation industry.

I would like to thank SIGDA for providing the travel grant that made my attendance at DAC-90 possible. It was a great opportunity and valuable learning experience for me.

Trip Report: 1990 Design Automation Conference

Sreejit Chakravarty
Dept. Of Computer Science
State University of New York
Buffalo, NY

I just returned after attending the 1990 IEEE/ACM Design Automation Conference where I presented part of my work on "synthesizing/designing and identifying stuck-open testable CMOS combinational circuits". I am grateful to the SIGDA executive committee for supporting this trip of mine and I would like to thank them for the support. In what follows I will try to summarize my perspective of the conference.

As is usually the case there were both technical and commercial exhibits sessions. I am academically minded and therefore spent most of my time attending the technical sessions. However, I did spend about half a day visiting the booths set up by the various vendors and found it very useful.

So far as the technical sessions were concerned most of the papers seemed to be have been from four areas: Synthesis for Testability; Testing; High Level Synthesis; and Physical Design. Over the years the number of testing related sessions in DAC has been on the increase and this year there were more testing related sessions than in the previous years. The number of papers on physical design is definitely on the decrease. I wonder if this reflects industry trends or is merely a function of the composition of the program committee.

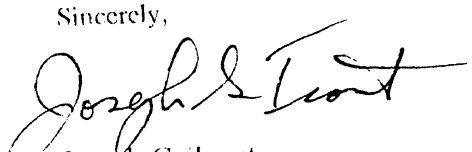
My primary area of interest is VLSI testing and I attended a number of sessions containing testing related papers. Most of these papers were very interesting and were more of a pragmatic nature. There was also a panel discussion on "Testing in the 1990's". A number of "distinguished" panel members voiced their opinions on testing trends for the future. The opinions ranged from being very "bizzarre" to being very "learned". The more "flippant" among the panelist promised to solve all testing related problems in a couple of years. The rest merely expressed more optimism. I agreed with some and disagreed with others. However, I was disturbed with the fact that proponents of some of the new ideas in testing were not included in the pnel.

There was a very good "swamp party" on Tuesday. I did enjoy the very lively music. There was an abundance of "exotic" food. For those that enjoy "frog's leg", "alligators tail" etc. the "swamp party" was the place to be. I certainly did not enjoy the "alligator show". I have always been against such treatment of animals. I know not many of you will agree with me. But, I hope the DAC executive committee can do better than this in future DAC parties.

Being a university faculty member, I consider one of the most important aspects of the DAC to be the blend of research papers with the exhibits of real-world commercial products. Having this mixture of presentations allows the academic attendee to contribute to and actively participate in the research paper sessions and at the same time visit the exhibit areas to learn what the state-of-the-art is in the commercial world. It gives the academician the ability to learn how his/her research might be affecting the real-world and also provides information that can be brought back to the classroom to be shared with the students. On the other hand it also gives the industry user a chance to contribute to the research process by attending the paper sessions.

For the second year in a row, I noticed that one of the big buzz words on the exhibits floor was VHDL. Many vendors are supporting and marketing products that involve the use of the VHSIC Hardware Description Language (VHDL). This standardized language is propagating into EE and CS curricula and it is very gratifying to see that there is an ever growing base of industry support. In my opinion, expanded and structured use of VHDL will aid the digital system design process immensely.

Sincerely,



Joseph G. Tront
Assoc. Professor

Trip Report
International Workshop on Layout Synthesis

Dannie Durand

May 14, 1990

This report describes the International Workshop on Layout Synthesis held at the Microelectronics Center of North Carolina (MCNC) in Research Triangle Park from May 8th to May 11th. 1990. The purpose of the workshop was to describe advances in routing and placement technology in the last two years and to compare layout systems through the use of benchmarks.

A comparison of this year's workshop with the International Workshop on Placement and Routing of two years ago gives a sense of how fast things are changing in the layout field. It also indicates the direction in which current research is moving. Two years ago. the emphasis was primarily on standard and macro cells, although one session was devoted to sea-of-gates layout. An entire session was devoted to improving cooling schedules in simulated annealing algorithms. Another session was devoted to combined routing and placement systems. Detailed routing meant primarily channel routing, although one paper on switchblock routing was presented. Very little attention was given to compaction.

This year there was still a lot of interest in standard cell placement and on systems for macro cell layout. However, two layout systems were reported which dealt with designs which combine macro and standard cells. In addition to a session on channel routing, a paper on routing field programmable gate arrays was presented as well as a paper on a system which could be used to route a number of different design styles such integrated circuits, printed circuit boards and multi-chip modules. Global routing was discussed for macro cells, standard cells and sea-of-gates. The session on floorplanning indicates that the emphasis in layout is shifting more and more towards attacking placement and routing as an integrated problem instead of addressing each of these problems individually. Unlike the workshop of two years ago. this year an entire session was devoted to symbolic layout and compaction. There were two talks on simulated annealing-based placement implementations and two on parallel simulated annealing algorithms. However this year there seemed to be more emphasis in the systems in which simulated annealing was used than in simulated annealing itself. In general, the trend seems to be towards systems which can handle designs which have less regularity, giving the designer increased flexibility. This can be seen in the systems which combine standard and macro cells as well as the systems which attempt to address the layout problem for several different technologies. There is also a movement, typified by field programmable gate arrays, towards technologies which reduce the time and cost required to layout a chip, although with a possible reduction in area/time efficiency.

The change in technologies was also reflected in the set of benchmarks used this year. These were compiled and presented by Krysztof Kozminski. A movement is afoot to use two formats as standards: Yet Another Language (YAL) and Vanilla Place and Route (VPNR). Parsers for these languages are available from MCNC through anonymous FTP. Only two of the standard cell benchmarks used two years ago were repeated in this years benchmark set: Primary1 and Primary2. These are considered out of date because they include many feedthroughs and have a lot of areas in which no routing is permitted at all. Nowadays most cells have one or at most two feedthroughs. However, because the use of Primary1 and Primary2 is widespread they were included again this year. A variety of other benchmarks were included to test different aspects of a layout system. One of these is Struct, which is a 16 bit multiplier. This benchmark is of interest because it is a highly structured, hierarchical design. Another is Biomed, a benchmark which will be difficult for any system which computes optimal steiner trees. This is because it includes large number of high cardinality nets. Industry1 tests over-the-cell routing. Industry2 and Industry3 have many feedthroughs in each cell and relatively few signal connections to each cell. As a result, in these designs vertical routing is relatively cheap.

In addition to Ami33 and Xerox, the macro cell benchmarks from two years ago, three new macro cell benchmarks have been added: Ami49, Hp and Apte. Three mixed standard cell/macro cell benchmarks are also available now: G2, A3 and T1. Unfortunately, these have a relatively low ratio of standard cells to macro blocks and so do not test some aspects of mixed layout systems adequately. More mixed benchmarks are needed with higher cell to block ratios. More benchmarks are needed in the following areas as well: compaction (large examples), sea-of-gates, and performance-oriented layout to test critical paths and clock distribution. Some people in the layout community have expressed an interest in benchmarks to test placement only and routing only, but others feel it is difficult to interpret the results when only one of these problems is addressed in isolation. All of these benchmarks are available from MCNC through anonymous FTP.

Report on the
IFIP Working Conference on Logic and Architecture Synthesis

Tadeusz Łuba
Warsaw University of Technology
Institute of Telecommunications
00-665 WARSAW, Nowowiejska 15/19

The IFIP Working Conference on Logic and Architecture Synthesis was held at Palais des Congres, a very interesting venue of Paris, particularly intended for making conferences and congresses. Together with this conference there was held the EuroASIC conference for which the two sessions of Logic and Architecture Synthesis Conference was held commonly. This two common sessions were sacrificed especially to the area of logic synthesis, which as prof. G. Saucier said, became to play a major role in VLSI designing. The invited paper was of prof. E.J.McCluskey, who presented a very interesting "Half a Century of Logic Synthesis".

The conference offered me the possibility to meet international experts in the field of logic synthesis both from U.S.A. and Europe. Particularly I was enjoyed to meet all of these specialists whose books and papers I have been read and whose I could treat as my "teachers of logic synthesis".

There were a number of interesting talks on logic synthesis. Some particularly interesting papers were concerned with the CAD tools for logic synthesis on PALs and such the key problems as state assignment and minimization of sequential machines. The most interesting papers were presented by G. Saucier, R. Brayton and G. de Micheli.

My talk on *Combining Serial Decomposition with Topological Partitioning for Effective Multi-Level PLA Implementations* was concerned with PAL based synthesis as well as general method of logic decomposition problem. A number of new approaches to logic decomposition problem I have mentioned during the conference will be very useful in development of our CAD system. Besides the technical talks, the conference provided a good exhibition of new commercial products from the industry. It is an excellent opportunity to communicate with persons from the industry. Attending the IFIP Conference helped me to learn the latest developments in research on CAD systems for VLSI.

I am grateful to SIGDA for supporting my visit in Paris through their travel grant and thus making it possible for me to be part of the show. I would like also to thank prof. G.Saucier for waiving me from conference duty.

Report on 1990 International Workshop on Layout Synthesis

Mitsuru Igusa

Department of Electrical Engineering,
University of California, Berkeley

The 1990 International Workshop on Layout Synthesis was held at the Microelectronics Center of North Carolina (MCNC) in Research Triangle Park in May. There were approximately 90 attendees at the conference primarily from U.S., with several people from Canada, Europe and Japan. Most of the attendees were from universities and research organizations, and less than 20 attendees were from industry.

There were 3 days of technical talks, concentrating on placement, floorplanning, routing and compaction. I thought the following talks were interesting:

• "An Optimal Algorithm for Floorplan Area Optimization" by T. Wang and D. Wong
This is a practical extension of the Stockmeyer's shape fitting algorithm commonly used in floorplanning. The extension handles L-shaped blocks and a class of non-sliceable placements in an optimal manner using a fast and novel search space pruning algorithm.

• "Permissible Error in Parallel Simulated Annealing" by M. Durand
A formal model of how multiple processors interact when synchonization is reduced when applied to parallel simulated annealing is presented. The model is used to analyze worst case bounds on the effect of error (caused by the reduced synchronization) on the final solution quality. This theoretical model explains why worse results are usually obtained from distributed memory compared to shared memory paralled processors.

• "A New Area-Based Figure of Merit for Layout Synthesis" by A. Rajanala and A. Tyagi
Empirical fomulas are presented that estimate the area of a variety of n-bit data path modules such as parallel-prefix adders and barrel shifters. The formulas are a function of n, and experimentally shown to be fairly accurate in estimating area for a wide range of sizes (n ranging from 4 to 128).

There was also a placement and routing benchmark session. The benchmarks consisted of several small gate-array, standard-cell and macro-cell chip layout examples. There were several universities, and one company from industry that participated in doing the benchmarks. In general the results were better and more consistent than the results from an earlier workshop (1988 MCNC Workshop on Placement and Routing). This indicated that the exiting algorithms are becoming more mature and good competetive results are more easily obtainable.

I would like to thank ACM SIGDA for providing the travel grant.

Report for the 1990 ISCAS Conference

Michael A. B. Jackson

Department of Electrical Engineering and Computer Sciences

University of California, Berkeley, California 94720

June 1, 1990

The 1990 International Symposium on Circuits and Systems (ISCAS) was held in New Orleans, Louisiana between May 1 and May 3 at the Sheraton Hotel. I attended as an invited author for the session on "Layout for High Performance Circuits" where I presented my paper entitled "Estimating and Optimizing RC Interconnect Delay during Physical Design." I found the conference to be an interesting blend of technical presentations, tutorial level panel discussions, one-day technical courses and vendor product demonstations.

One of the unique experiences that ISCAS offers as a conference is the diversity of the program schedule. Topics ranged from "Multidimensional Digital Signal Processing" to "Technological Challenges Facing the High-Volume Analog Circuit Designer." I found myself spending most of my time attending a tutorial level panel discussion on neural network chips, and sessions devoted to IC design. Some of these sessions included: layout for high performance ICs, electronics packaging, the pervasiveness of BICMOS technology, and circuit layout.

In general, IC performance optimization of integrated circuits seemed to be well represented by several papers from the areas of logic synthesis, physical design, and transistor sizing. I would say that the area which garnered the most interest and was represented best in terms of program time was the research in neural networks.

I would like to thank ACM SIGDA for their generous support in providing me with a travel grant. Not only did the ISCAS conference present an opportunity for me to broaden my technical horizons, but it also provided me with the opportunity to visit and experience one of America's most interesting cities.

Report for the 1990 ISCAS

Department of Electrical Engineering and Computer Sciences

University of California, Berkeley, California 94720

May 15, 1990

Shen Lin

The 1990 International Symposium on Circuits and Systems was held in sunny New Orleans, Louisiana, between May 1 and May 3 at the New Orleans Sheraton hotel. I attended the conference as a speaker and found the conference to be an enlightening blend of technical presentations covering topics from analog integrated circuits, neural networks, to, digital signal processing, and computer aided circuit designs.

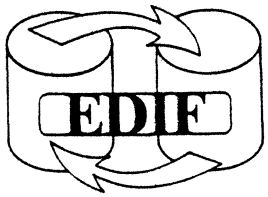
I presented a paper about an efficient and accurate timing verifier in the section of high performance layout. I think the feedback is positive. I got some very useful comments from the audience. Nowadays, the high performance layout is a very hot topic in circuit design. In that section, many valuable ideas were brought out by experts. From the discussion with them during a short break, I definitely resolve some questions in my research at this field.

I found myself spending most of my time attending the panel discussions about the analog implementation of neural networks. These were given by experts in industry and academy. Their experience can lead me a correct point of view about this so far still controversial topic.

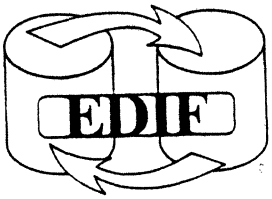
Because the ISCAS covers very broad range of fields, I got chance to hear some interesting topics about image processing, efficient device models, and behavior synthesis techniques. This presious chance to ISCAS truly broaden my eye sights on all these technologies.

DA Standards Activities

See also **Conference Announcements** Section for other standards-related activities.



Department of Computer Science
University of Manchester



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ENGLAND

CALENDAR OF EVENTS

Below is a list of upcoming DA events prepared by Dr. Sunil Das of the University of Ottawa. Dr. Das is also editor of the IEEE *VLSI Technical Bulletin.* He is an associate editor of the SIGDA Newsletter

Sunil Das

Second International Conference on Microelectronics (Arab School of Science and Technology), October 13-15, 1990, Damascus, Syria.

Contact : M. I. Elmasry, VLSI Research Group, University of Waterloo, Waterloo, Ontario N2L 3G1, Canada. *Phone* : (519)885-1211, *ext.* 3753.

AIPR 19, Workshop on Applied Imagery Pattern Recognition (Society of Photooptical Instrumentation Engineers, Rome Air Development Center), October 17-19, 1990, McLean, VA.

Contact : Brian Mitchell, ERIM, PO Box 8618, Ann Arbor, MI 48106. *Phone* : (313)994-1200, *ext.* 2713.

OOPSLA 90, Fifth Conference on Object-Oriented Programming Systems, Languages, and Applications (ACM), October 21-25, 1990, Ottawa, Ontario, Canada.

Contact : Association for Computing Machinery, 11 West 42nd Street, New York, NY 10036. *Phone* : (212)869-7440.

FOCS, 31st Foundations of Computer Science (IEEE Computer Society), October 22-24, 1990, St. Louis, MO.

Contact : Christos Papadimitriou, Computer Science Department, University of California at San Diego, La Jolla, CA 92093. *Phone* : (619)534-2086.

JCIT 5, Fifth Jerusalem Conference on Information Technology (IEEE Computer Society, Information Processing Association of Israel), October 22-25, 1990, Jerusalem, Israel.

Contact : Abraham Peled, IBM T. J. Watson Research Center, PO Box 704, Yorktown Heights, NY 10598.

ESORICS 90, European Symposium on Research in Computer Security (AFCET), October 24-26, 1990, Toulouse, France.

Contact : Martin Gilles, 16 Para de Diane, 78350 Jouy eu Josas, Toulouse Cedex, France.

NACLP 90, 1990 North American Conference on Logic Programming (IEEE Computer Society), October 28-November 1, 1990, Austin, TX. *Cosponsor* : ACM.

Contact : Carlo Zaniolo, MCC, 3500 West Balcones Center Drive, Austin, TX 78759. *Phone* : (512)338-3442.

Compsac 90, 14th International Computer Software and Applications Conference (IEEE Computer Society), October 31-November 2, 1990, Chicago, IL.

Contact : Ifay F. Chang, Room 1B28, IBM T. J. Watson Research Center, PO Box 714, Yorktown Heights, NY 10598. *Phone* : (914)789-7825. *Fax* : (914)784-6211.

1990 IFIP-IEEE International Workshop on Defect and Fault Tolerance in VLSI Systems (IEEE Computer Society), November 5-7, 1990, Grenoble, France.

Contact : Gabriel Saucier, Institut National Polytechnique de Grenoble/CSI, 46 avenue Felix Viallet, 38031 Grenoble Cedex, France. *Phone* : (33)76-57-46-87. *Fax* : (33)76-50-23-21 ; or Tulin E. Mangir, TRW, 1 Space Park, R2/2036, Redondo Beach, CA 90278. *Phone* : (213)813-3894. *Fax* : (213)813-3709.

24th Asilomar Conference on Signals, Systems, and Computers (Naval Postgraduate School *et al.*), November 5-7, 1990, Pacific Grove, CA.

Contact : George M. Dillard, Naval Ocean Systems Center, San Diego, CA 92152-5000. *Phone* : (619)553-2478.

ICCC 90, 10th International Conference on Computer Communication (International Council on Computer Communication), November 5-9, 1990, New Delhi, India.

Contact : Saroj Chowla or P. P. Gupta, ICCC 90, CMC Limited, A-5 Ring Road, South Extension Part I, New Delhi 110 049, India. *Phone* : 91(11)626-807. *Fax* : 91(11)684-4652.

IEEE Workshop on the Management of Replicated Data (IEEE Computer Society, IEEE Computer Society Technical Committee on Operating Systems), November 7-9, 1990, Houston, TX.

Contact : Luis-Felipe Cabrera, IBM Almaden Research Center, 650 Harry Road, MC K55/803, San Jose, CA 95120-6099. *Phone* : (408)927-1838.

ICCAD 90, IEEE International Conference on Computer-Aided Design (IEEE Computer Society), November 11-15, 1990, Santa Clara, CA. *Cosponsor* : IEEE Circuits and Systems Society.

Contact : Pat Pistilli, MP Associates, 7490 Clubhouse Road, Suite 102, Boulder, CO 80301. *Phone* : (303)530-4562.

AIDA 90, Sixth Conference on Artificial Intelligence and Ada (George Mason University *et al.*), November 15-16, 1990, Reston, VA.

Contact : AIDA 90, George Mason University, 4400 University Drive, Fairfax, VA 22030. *Phone* : (703)323-2713. *Fax* : (703)323-2630. *E-mail* : aida@gmuvax.gmu.edu.

IFIP Workshop on Electronic Design Automation Frameworks (IEEE Computer Society, International Federation for Information Processing), November 26-28, 1990, Charlottesville, VA.

Contact : Ron Waxman, University of Virginia, Thornton Hall, Charlottesville, VA 22903. *Phone* : (804)924-6086.

IEEE 1990 Conference on Software Maintenance (IEEE Computer Society), November 26-29, 1990, San Diego, CA.

Contact : Thomas M. Pigoski, USN, NSGD Pensacola, Corry Station, Pensacola, FL 32511. *Phone* : (904)452-6399.

Micro 23, 23rd Symposium and Workshop on Microprogramming and Microarchitecture (IEEE Computer Society), November 27-29, 1990, Orlando, FL. *Cosponsor* : ACM.

Contact : Chris Papachristou, Case Western Reserve University, Computer Engineering and Science Department, Cleveland, OH 44106. *Phone* : (216)368-5277. *E-mail* : cap@alpha.ces.cwru.edu.

First International Symposium on Uncertainty and Analysis : Fuzzy Reasoning, Probabilistic Methods, and Risk Management (IEEE Computer Society, University of Maryland *et al.*), December 3-5, 1990, College Park, MD.

Contact : Bilal M. Ayyub, Civil Engineering Department, University of Maryland, College Park, MD 20742.

ICCV 90, Third International Conference on Computer Vision (IEEE Computer Society), December 4-7, 1990, Osaka, Japan.

Contact : ICCV 90, IEEE Computer Society, 1730 Massachusetts Avenue, N.W., Washington, D.C. 20036-1903. *Phone* : (202)371-1013.

11th Real-Time Systems Symposium (IEEE Computer Society, IEEE Computer Society Technical Committee on Real-Time Computing), December 5-7, 1990, Orlando, FL.

Contact : Doug Locke, IBM - MS 409, Systems Integration Division, 6600 Rockledge Drive, Bethesda, MD 20817. *Phone* : (301)493-1496. *E-mail* : cdl@cs.cmu.edu.

CASE 90, Fourth International Workshop on Computer-Aided Software Engineering (IEEE Computer Society), December 5-8, 1990, Irvine, CA.

Contact : Elliott J. Chikofsky, Radius Systems, 75 Lexington Street, Burlington, MA 01803. *Phone* : (617)494-8200.

10th Conference on Foundations of Software Technology and Theoretical Computer Science, December 17-19, 1990, Bangalore, India.

Contact : Y. N. Srikant, Indian Institute of Science, Bangalore 560 012, India. *Phone* : 91(812)334-411.

Seventh Israeli Conference on Artificial Intelligence and Computer Vision, December 26-27, 1990, Tel Aviv, Israel.

Contact : A. Bruckstein, Faculty of Computer Science, Technion, 32000 Haifa, Israel. *E-mail* : freddy@techsel.bitnet ; or Shmuel Peleg, David Sarnoff Research Center, CN 5300, Princeton, NJ 08543-5300. *Phone* : (609)734-2284. *E-mail* : peleg@vision.sarnoff.com.

Fourth CSI/IEEE International Symposium on VLSI Design (IEEE Computer Society, Computer Society of India *et al.*), January 5-8, 1991, New Delhi, India.

Contact : Yashwant K. Malaiya, Computer Science Department, Colorado State University, Fort Collins, CO 80523. *Phone* : (303)491-7031. *Fax* : (303)491-2293. *E-mail* : malaiya@ravi.cs.colostate.edu ; or D. Roy Chowdhury, Gateway Design Automation, SDF # A-1, Noida Export Processing Zone, PO NEPZ, Noida 201 305, India. *Phone* : 91(05736)62342. *Fax* : 91(05736)62343.

IEEE International Conference on Wafer Scale Integration (IEEE Computer Society), January 29-31, 1991, San Francisco, CA. *Cosponsors* : IEEE Components, Hybrids, and Manufacturing Technology Society.

Contact : Terry Chappell, 730 Encino Drive, Aptos, CA 95003. *Phone* : (408)662-1936 ; or R. Mike Lea, Brunel University, Uxbridge UB8 3PH, U.K. *Phone* : (44)895-74000, *ext.* 2821. *Fax* : (44)895-58728. *E-mail* : mike.lea@brunel.ac.uk.

EDAC 91, European Design Automation Conference (IEEE Computer Society, Institution of Electrical Engineers), February 25-28, 1991, Amsterdam, The Netherlands.

Contact : Secretariat, EDAC 91, CEP Consultants, 26-28 Albany Street, Edinburgh EH1 3QH, Scotland. *Phone* : 44(31)557-2478. *Fax* : 44(31)557-5749.

(Prepared by Associate Editor Sunil R. Das, Department of Electrical Engineering, University of Ottawa, Ottawa, Ontario K1N 6N5, Canada)

SIGDA FALL MEETING
at ICCAD-90

Sunday Evening, November 11
Look for Placards at the Santa Clara Convention Center

Food and beverages (alcoholic and non-alcoholic) will be served

CALL FOR PAPERS

28TH ACM/IEEE DESIGN AUTOMATION CONFERENCE®

SAN FRANCISCO MOSCONE CENTER • JUNE 17-21, 1991

DAC is the premier conference devoted solely to the field of Design Automation. All aspects of the use of computers as aids to the design process, from conceptual design through to manufacturing, are included. Four session types are included: regular paper sessions, short paper sessions, panels, and tutorials.

REQUIREMENTS FOR SUBMISSION OF PAPERS

Authors should submit their papers to the Program Chair no later than November 7, 1990. Each submission should include one cover page and eight stapled copies of the complete manuscript.

The one cover page should include:

- •Name, affiliation, and complete address for each author
- •A designated contact person including fax (if available), and telephone number
- •A designated presenter, should the paper be accepted
- •The following signed statement: "All appropriate organizational approvals for the publication of this paper have been obtained. If accepted, the author(s) will prepare the final manuscript in time for inclusion in the Conference proceedings and will present the paper at the Conference."

The eight copies of the complete manuscript should each include:

- • Title of paper, 60 word abstract indicating significance of contribution, and a list of category numbers (given below), **ordered by relevancy,** most closely matching the content of the paper. **To permit a blind review, do not include name(s) of author(s).**
- •The complete text of the paper in English, including all illustrations and references, not exceeding 5000 words. The length of the paper is considered in the review process.

Notice of acceptance will be mailed to the contact person by February 15, 1991. Authors of accepted papers must sign a copyright release form.

TOPICS OF INTEREST

Authors are invited to submit original technical papers describing recent and novel research or engineering developments in all areas of Design Automation. Topics include, but are not limited to:

1.1 Electrical Simulation
1.2 Discrete Simulation
1.3 Timing Verification
2.1 Test Validation and Testability Analysis
2.2 Test Pattern Generation and Design-for-Test
2.3 Formal Methods for Design Verification
3.1 Floorplanning and Placement
3.2 Global and Detailed Routing
3.3 Physical Module Generation
3.4 Symbolic Layout and Compaction
3.5 Complete Layout Systems
3.6 Layout Verification (DRC, ERC)
4.1 Logic Synthesis and Optimization
4.2 Register-Level Synthesis and Optimization
4.3 Behavioral Synthesis and System-Level Design Aids
5.1 Behavioral and Hardware Description Languages
5.2 Design Systems and Databases
6.1 DA for IC Fabrication
6.2 Computer Aids for Manufacturing
7.1 DA for Analog Circuits
7.2 High Speed Systems and Microwave DA
7.3 DA for Electronic Packaging
8.1 Human Factors in DA
8.2 Frameworks and Software Engineering in DA

PANELS, TUTORIALS, SPECIAL TOPIC SESSIONS

Proposals for topics of Panels, Tutorial Sessions, and Full-Day Tutorials should be submitted to the Program Chair no later than November 7, 1990. Each proposal should not exceed two pages in length and should include a description of the topic, structure of the session or tutorial, and a list of participants. Contact should be made with all participants in advance.

Special Topic Sessions may be either independent papers with a common theme or a set of closely related papers describing an overall system. In both cases, independent reviews of each paper and evaluation of the session as a whole will be used to select sessions. Proposals for Special Topic Sessions should be submitted along with the papers to be included in the session and should describe the theme of the session. These proposals and papers must be submitted by November 7, 1990 to allow for a complete review.

Birds of a Feather meetings are informal groups to discuss technical items of common interest. These very informal noncommercial meetings are held after normal Conference hours. Submissions should be one paragraph in length.

PROGRAM CHAIR

MP Associates, Inc.
ATTN: Alfred E. Dunlop
Program Chair, 28th DAC
7490 Clubhouse Rd., Suite 102
Boulder, Colorado, 80301
For information call: (303) 530-4333

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INTERNATIONAL CONFERENCE ON COMPUTER-AIDED DESIGN

ICCAD-90

A CONFERENCE FOR THE EE/CAD PROFESSIONAL

November 11-15, 1990
Convention Center
Santa Clara, California

ADVANCE PROGRAM

sponsored by

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ADVANCE REGISTRATION FORM
ICCAD-90

November 11-15, 1990
Santa Clara, CA USA

Make checks payable to: **ICCAD-90**

Please mail registration form and check to:

MP ASSOCIATES, INC.
REGISTRATION DESK
7490 CLUBHOUSE ROAD, SUITE 102
BOULDER, CO 80301
(303) 530-4562 (for information only)

All advance registration must be received before October 12, 1990. On-site Conference payments must be made by check or cash. **NO CREDIT CARDS ACCEPTED!** No refunds unless cancellation is received before October 12, 1990. All refunds are subject to a $15.00 fee.

PLEASE TYPE OR PRINT CLEARLY.

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	Before Oct. 12	After Oct. 12	Amount
IEEE/ACM Members	$160.00	$200.00	_____
Non-members	$200.00	$250.00	_____
Students	$50.00	$50.00	_____
One day only	$100.00	$125.00	_____

Select day: ☐ Mon. ☐ Tues. ☐ Wed.

TUTORIAL FEES

IEEE/ACM Member 1/2 Day	$130.00	$130.00	_____
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Non-member 1/2 Day	$160.00	$160.00	_____
Non-member Full Day	$320.00	$ 320.00	_____

TOTAL AMOUNT: *(sum of conference & tutorial fees)* _____

TUTORIAL REGISTRATION

(See page 36, item 6 for details)

Attendance is limited for ICCAD-90 tutorials. To increase your chances of reserving a seat in the tutorial of your choice, register before the October 12 advance registration deadline. Tutorial registration fee includes breakfast and tutorial materials.

Tutorial Selection: *please indicate first (1) and second (2) choices. If registering for a full day, check both an A.M. and a P.M. tutorial.*

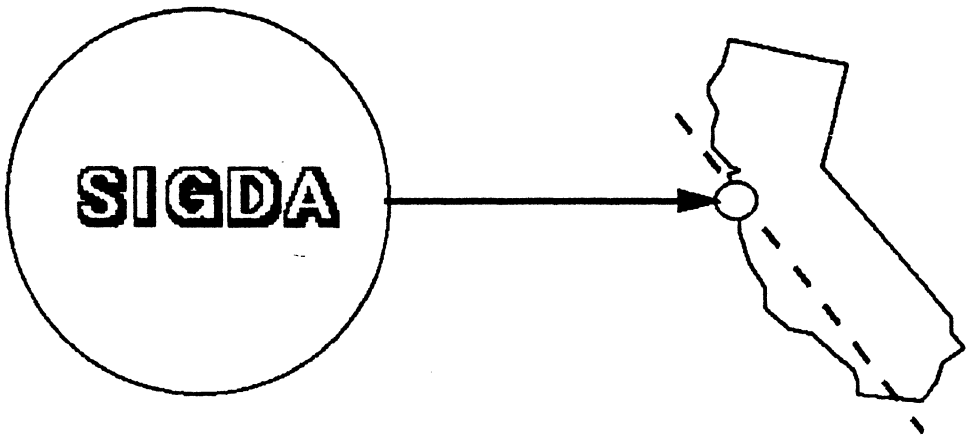
MORNING:

_____ Formal Verification of Hardware Designs
_____ Multi-Level Logic Synthesis
_____ What's New in VLSI/CAD: A Manager's Crystal Ball
_____ Electrical Modeling of Chip and Package Interconnects

AFTERNOON:

_____ High-level Logic Synthesis
_____ Synthesis for Testability
_____ Sequential Synthesis
_____ Mixed Analog/Digital Simulation

The Silicon Valley Chapter of



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First Tuesday of the Month
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St James Infirmary
390 Moffett Blvd.
Mountain View
12:00 noon

For further information contact Paul Weil:
weilcad.frith.cs.psu.edu


EDAC
The European Design Automation Conference
Amsterdam
25-28 February 1991
EDAC 91 Secretariat
CEP Consultants Ltd
26-28 Albany Street
EDINBURGH
EH1 3QH
UK

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Formal Verification and Specification	Luc Claesen IMEC vzw, Heverlee, B
Layout Synthesis	Günther Koetzle IBM Laboratorium, Boeblingen, FRG
Layout Verification	Pierro Capocelli SGS-ATES, Milan, I
Simulation	Louis Vidigal INESC, Lisbon, P
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VHDL Users' Group
IEEE Computer Society

In Cooperation with the Electronic Industries Association

CALL FOR PAPERS

Fall VHDL User's Group

VHDL: A SYSTEMS DESIGN PERSPECTIVE

October 14-17, 1990
Claremont Resort
Oakland, California

The fall VHDL User's Group Meeting will be held in the beautiful Claremont Resort in Oakland, California. Our theme this fall will be the use of VHDL in designing large systems. The technical presentations for this User's Group Meeting will focus on the different ways of using VHDL in designing systems. Any presentations concerning the use of VHDL in designing, modeling, and/or documenting systems at a high level of abstraction are welcome. Presentations concerning the synthesis of systems level descriptions from gate level VHDL descriptions are especially encouraged.

Areas of interest include, but are not limited to:

Abstract Modeling	Behavioral Specifications
Verifying System Models	Validating Behavioral Models
Tools for Systems Modeling	Validating Systems Models
Formal Methods	Large Team VHDL Models
Transition to Other Tools	Testing Systems Models
Standards for Systems Models	High-Level Synthesis
Sample Systems Models	Actual Uses of VHDL for Systems

Important dates:

Abstracts Due:	July 1, 1990
Acceptance Notification:	July 15, 1990
Presentations Due:	September 1, 1990

Abstracts may be sent to the program co-chairs:

David Barton
Intermetrics, Inc.
4733 Bethesda Ave.
Bethesda, MD 20814
(301) 657-3775
(301) 657-9290(fax)
barton@i2wash.com

Doug Perry
Synopsys, Inc.
1098 Alta Ave.
Mountain View, CA 94043
(415) 962-5000
(415) 965-8637(fax)

CALL FOR PARTICIPATION

University of Virginia

Center for Semicustom Integrated Systems

Second International IFIP WG 10.2 Workshop on Electronic Design Automation Frameworks

Organized in cooperation with

GI FA 3.5 and ITG FA 5.2,
IEEE Computer Society (Design Automation Technical Committee),
ACM (Special Interest Group on Design Automation)
and the
University of Virginia Center for Semicustom Integrated Systems

Location and Date:

The workshop will be held in Charlottesville, Virginia, USA, **November 26 through 28, 1990.**

Theme: The Advent of Standards and their Effect on Design Environments for the 90s.

Scope:

The IFIP WG 10.2 Workshop on **EDA Frameworks** will explore how the entry of new standards such as VHDL, EDIF, STEP/PDES, and CFI, and efforts to create a harmonious framework for the application of these standards, will effect the design environment during the 90s. What is the role of specialized languages for specific environments, given this new impetus? How can the user community help standards to evolve and meet changing needs as the technology changes? Topics include, but are not limited to:

- Common data bases
- Design frameworks
- Tool integration strategies
- Application of AI-techniques
- LANs/WANs
- Version management
- Exchange formats
- Standardization of interfaces
- Conceptual schemata
- Combined hardware/software design
- Design management tools
- Documentation control

Framework Demonstrations:

One afternoon during the workshop will be devoted exclusively to demonstrations of running frameworks.

IEEE COMPUTER SOCIETY DATC

acm SIGDA

CHDL 91
Call for Papers

IEEE COMPUTER SOCIETY DATC

SIGDA

IFIP
Tenth International Symposium on Computer Hardware Description Languages and their Applications

April 22-24, 1991 Marseille, France

Theme: The Synergistic Relationship Between CHDLs and The Design Environment
The goal of this symposium is to bring together, from industry and academia, the leading researchers and the best work in digital systems design aids based upon description languages (CHDLs). Each session will present a view of the challenges and their impact on future CHDLs.

The workshop will be followed by a meeting of the "VHDL Forum for CAD in Europe." A common session between the two events is planned.

Scope
Authors are invited to submit original scientific papers describing recent research, new developments or practical experience on significant design projects, in all areas of CHDLs and their application in the design environment. Topics include, but are not limited to:

- VHDL
- Frameworks
- Application driven Semantics of CHDL's
- Very High Level System Specification
- Test Oriented CHDL's
- Synthesis from a High Level Description
- Formal Verification: Techniques and Applications
- Automatic Finite State Machine Verification
- New concepts in Design Environments: User Interfaces, Design Representations, Tool Integration, Special Purpose Hardware

Paper submission for 30 minute regular presentations
One cover page and five stapled copies of the full length manuscript in English, should be sent to the program chairman to arrive no later than September 15, 1990. The one cover page should include:

- Title of paper
- Name(s), affiliation(s), complete address(es) of author(s).
- Identification of principal author, with telephone, telefax and e-mail indications
- The following signed statement:

  "All appropriate organizational approvals for the publication of this paper have been obtained. If accepted, the author(s) will prepare the final manuscript in time for inclusion in the conference proceedings, and will present the paper at the conference".

The five copies of the full manuscript should each include the title of paper, list of authors, topic(s) from the list above that most closely match the content of the paper, abstract, and complete text including all illustrations and references, not exceeding 20 double-spaced typewritten pages. Refereeing will be carried out by the program committee. Authors of accepted papers will be notified by January 1, 1991. The final camera-ready version of accepted papers is due by February 15, 1991. A selection of the conference papers will be considered for publication in an international journal (approval pending). A cash prize will be given for the best paper presented. The program committee reserves the right to accept for a poster session a submission for regular presentation, and to request the author(s) to shorten the submitted manuscript.

CALL FOR PAPERS
IEEE JOURNAL OF SOLID-STATE CIRCUITS
FIRST SPECIAL ISSUE
on
MICROELECTRONIC SYSTEMS

Microelectronic systems must be specified at every level of abstraction including the system, behavioral, register, logic, circuit, transistor and process levels. To address this growing area, a series of special issues is being planned as a forum for original papers which emphasize the *interactions* among the various aspects of microelectronic systems including interactions among system design, logic circuit design, memory design, architecture, CAD tools, testing, physical design, VLSI technology and semiconductor processes. Thus, its scope will include all aspects of the design and implementation of microelectronic systems. Topics of interest include, but are not strictly limited to, the following:

- Partitioning Designs over Multiple Levels of Packaging
- Economical Architectures for Wafer Scale Integration
- Interactions Between Architecture and Process Technology
- Analog Neural Networks Using Subthreshold CMOS
- Area, Time, I/O and Energy Tradeoffs of VLSI Systems

Prospective authors are requested to submit five copies of the complete manuscript of 7 to 15 double-spaced typewritten pages, plus up to 10 pages of figures. Shorter papers of 6 or less pages and up to 3 pages of figures will be considered for publication as correspondence. To be considered for the May, 1991 special issue, manuscripts should be sent by **September 15, 1990** to the Guest Editor:

Prof. Donald W. Bouldin
Electrical & Computer Engineering
University of Tennessee
Knoxville, TN 37996-2100

Phone: (615)-974-5444
FAX: (615)-974-5492
Email: bouldin@sun1.engr.utk.edu
or bouldin@utkvx.bitnet

The IEEE Journal of Solid-State Circuits has been published for the past twenty-five years by the IEEE Solid-State Circuits Council on behalf of nine Groups and Societies within the IEEE. In response to an initiative from the Computer and Circuits & Systems Societies, the Council has authorized a series of special issues on microelectronic systems if the demand warrants. The intent is to establish a consistent forum for this field which unifies advances in many disciplines. Members of the sponsoring IEEE Societies may subscribe to this journal for $14 per year which will be published *monthly* beginning in 1991. Contact IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08855-1331, Phone: 201-981-0060.

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INTERNATIONAL JOURNAL IN COMPUTER SIMULATION

The **International Journal in Computer Simulation** will present state-of-the-art research and development in the area of modeling methodologies; discrete event, parallel discrete event, continuous, dynamic, military, agricultural, and economic simulations; simulation of manufacturing and production environments; simulation as a design tool; and simulation related topics.

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Full manuscripts and outlines of proposed articles should be sent to:

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Guidelines for Authors can be obtained from either the Editor or Ablex Publishing Corporation, 355 Chestnut St., Norwood, NJ 07648.

International Journal of Computer Simulation

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Areas of Primary Interest:

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Logic Level Modeling for ASICs
Monterey Beach Hotel, Monterey, California
August 12-14, 1990
Fee: $420 (includes Registration, Hotel, and meals)
Sponsored by SIGDA of ACM
in cooperation with IEEE Circuits and Systems Society

CALL FOR PARTICIPATION

The Logic Level Modeling for ASICs Workshop will provide an interchange of ideas between people working on ASIC logic level models. The workshop will include people from ASIC foundries, CAE companies, Universities, and System designers (ie ASIC users.) There will be three major technical sessions, and two lighter evening sessions. Each technical session with be discussion oriented rather than presentations. Specific topics include:

-TIMING MODELS FOR ASICS
-SIGNAL REPRESENTATIONS
-TESTING ISSUES
-MODELING LARGE CELLS
-ACCURACY/ROBUSTNESS/PERFORMANCE/FEATURES
-AUTOMATION OF MODEL GENERATION (SYNTHESIS)

To maintain the workshop atmosphere and to encourage open discussions no recorders or cameras will be allowed. However, notes will be taken and a workshop report will be published in the SIGDA newsletter. The attendance will be strictly limited to 40 people, based upon first paid, first served basis with a limit of 2 attendees per company. In case of over subscription attendance preference will be given to those actively working in the field and willing to make a significant technical contribution to the workshop. Each attendee is expected to participate actively in the workshop and will be assigned some questions to be answered before the workshop, and the results will be presented during the sessions. The Sunday evening session includes a light supper, discussions, and an opportunity to meet the participants.

For more information please contact any member of the Workshop Committee:

Workshop Chair	Program Chair	Arrangements Chair
Mark Glasser	Steve Bush	Colleen Matteis
Valid	VLSI Technology	
(408) 998-2430	(408)944-4811	(408)434-7624
Session Chair	**Assistant Lexicographer**	**Lexicographer**
Dr. Robert Mathews	Dr. John M. Acken	Bill Hobson
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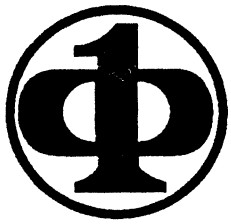
SIGDA

IEEE Circuits and Systems Society

Logic Level Modeling for ASICs Workshop 1990



CALL FOR PAPERS

Third IEEE Conference On Computer Workstations: Accomplishments And Challenges

Sponsored by the IEEE Technical Committee on Operating Systems

The Sea Crest Resort, Falmouth, Cape Cod (Massachusetts)
May 15–17, 1991

As we enter the 1990's, changes in technology will require rethinking the role of the workstation in the computing environment. Gigabit communication, desktop parallel computing, and multimedia applications are now emerging. The key to effective computing in this new world is the interface between the user and the computing environment: the workstation. What challenges must be overcome to make effective use of emerging technologies? CCW '91 seeks to foster dialogue between builders of workstation-based applications and technological innovators. Papers may focus on experiences with ambitious applications as well as on research topics. Topics include:

- Design of workstation computing environments
- Workstation and system architecture
- Application and system management
- User interface technologies
- Exploiting parallelism and massive memory
- Network support for high performance distributed computing
- Computer-aided software engineering
- Information management systems
- Real-time sensing and control
- Issues of scale
- Innovative ideas and technologies

Papers should be no longer than about 5000 words (20 double-spaced pages), and must be received by September 15, 1990. Authors will be notified of acceptance by December 1, 1990, and final camera–ready copy is due by January 15, 1991. Both technical and case-study papers are solicited; case studies should describe existing systems and include performance or operational data where practical.

The conference will also include a poster session for discussing work in progress. Individuals with a specific interest in participating in the poster session are invited to submit a one-page abstract describing their project. In addition, the program committee will invite the authors of some of the submitted papers to present their work in the poster session.

Send five copies of each submission to:

Prof. Keith Marzullo
Program co-chair, CCW '91
Department of Computer Science, Upson Hall
Cornell University
Ithaca NY 14853

Important dates:

Submissions due	September 15, 1990
Notification of acceptance	December 1, 1990
Camera-ready copies due	January 15, 1991

INTERNATIONAL WORKSHOP ON FORMAL METHODS IN VLSI DESIGN

Miami, Florida
January 9 - 11, 1991

Sponsored by ACM SIGDA
in cooperation with IFIP WG10.2, IEEE TC VLSI

Background

There is increasing interest, both in academia and industry, in the application of formally-based design techniques to the design of integrated systems. Some of this interest has been motivated by the urgency of improving the reliability, testability and the robustness of designs. The aim of this series of workshops is to bring together researchers interested in the application of formal techniques to the hardware design process. The emphasis of this year's meeting is to provide an opportunity for synergistic interaction between researchers in "traditional" CAD areas and those interested in formal approaches to design.

Workshop Format

The workshop will consist of overviews of major topics by leading researchers, submitted and invited papers, poster sessions, and discussion sessions.

Focus

The session topics will include:

- Practical Experiences with Verification and Synthesis Systems
- Integration of traditional CAD systems and Verification
- Synthesis and Verification of Delay Insensitive Circuits
- Timing Specification and Verification
- Transformation based Design
- Design transformations for Testability
- Applications of higher Order Logic and Theorem Proving
- Finite State Machine Synthesis and Verification
- Applications of temporal logic and model checking
- VHDL based design systems and Communicating Sequential Processes
- Applications of Binary Decision Diagrams
- Process Algebras
- Specification and Design of Systolic Arrays

The intent of the workshop (and its format) is intended to encourage in-depth informal discussions among participants.

Prior Workshops

This workshop is intended as a series in North America to complement a corresponding series held in Europe. The latter series has been organized within the scope of IFIP WG10.2 (System Description and Design Tools) and LIFIP WG10.5 (Very Large Scale Integration); the latest of these workshops was held at Houthalen, Belgium in November 1989.

Hotel Registration

The Workshop will be held at the Omni International Hotel overlooking Biscayne Bay. A reduced winter hotel rate of $92 has been negotiated for Workshop participants. To make your hotel reservations call the Omni at 305-374-0000 and refer to ACM/VLSI '90.

For Workshop Registration Contact:

Marcela Brathwaite at 212-869-7440 Extension 347, e-mail: Marcela@acmvm.bitnet

Advanced Research in VLSI *Conference*

March 25 - 27, 1991

University of California, Santa Cruz

(co-sponsored by UC Berkeley)

This conference is the thirteenth in a series that has been held at CalTech, MIT, University of North Carolina, and Stanford. As in the past, the main goal of the conference is to promote interaction among researchers in the various disciplines.

VLSI (Very Large Scale Integration) involves the design, manufacture, and use of systems constructed from complex integrated circuits. It includes semiconductor devices and processing, circuit and system design, computer-aided tools and design automation, and systems architecture.

Systems Design and Integration is the special focus of the 1991 conference. Original research papers are especially welcome on

- **Systems:** Architecture using characteristics of VLSI technology and packaging, systems on a chip; systems integration issues: partitioning, interfaces, clocking, and synchronization; fault tolerance, simulation, testing, and formal verification methods.
- **Theory:** Models of computation for VLSI; massively parallel algorithms; metrics for evaluating the complexity of algorithms or systems.
- **Tools:** Systems modeling tools for experimenting with architectures; languages to specify or describe interfaces; methods and tools for behavioral synthesis; design data bases and data management frameworks.
- **Technology:** Sensor and actuator devices and circuits; integration of analog and digital circuits; power consumption, distribution, and cooling; wafer-scale integration and packaging.

As always, papers are welcome on all VLSI fields, especially on new ideas outside specific categories. The conference is not a showcase for established systems and CAD tools, but a forum for new ideas. Papers presented must have enough background to reach novices and enough new material to please experts.

Program Committee
Chair: Carlo Séquin, UCB, Berkeley

Academia

Don Bouldin, U. of Tennessee, Knoxville
William Dally, MIT, Cambridge
Carl Ebeling, U. of Washington, Seattle
Tracy Larrabee, UCSC, Santa Cruz
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Dick Lyon, Apple Computer, Cupertino
Al Marston, Sun Microsystems, Mountain View
Osamu Tomisawa, Mitsubishi, Itami, Japan
John Wharton, Applications Research, Sunnyvale

The FIRM deadline for submission of papers is October 15, 1990.
Authors will be notified by November 26, 1990.
Camera-ready manuscripts are due December 29, 1990.

Send 5 copies of draft papers (not to exceed 15 pages) by October 15, 1990 to:

Professor Carlo H. Séquin
University of California
CS Division, Evans Hall
Berkeley, CA 94720

Circuit Simulation and Process Simulation and Modeling Workshops

MCNC will conduct concurrent workshops covering the areas of circuit simulation and verification and the modeling and simulation of silicon processes. The purpose of these workshops is to draw together people who are model developers, users, programmers, and designers, as well as people who are doing measurement and characterization.

The task of developing usable simulation tools is enormous! Success requires an interdisciplinary effort. The MCNC research program in modeling and simulation is based on this concept and includes research in numerical techniques, models, measurements, and software. The simulation tools CAzM and PREDICT have been developed in an environment of aggressive VLSI/ULSI design and fabrication. It is hoped that the MCNC workshops will help broaden the involvement of workers nationally who have similar goals and interests - for the good of all concerned.

Invited speakers will present information on topics including process models, process characterization/measurement, circuit simulation issues, and process/device modeling issues in the 90s.

The one day workshops will be held **November 6, 1990** at MCNC, 3021 Cornwallis Road, Research Triangle Park, NC 27709. Registration will begin at 8am.

Accommodations: Rooms will be set aside at the Holiday Inn in Research Triangle Park. Attendees will be responsible for contacting the hotel directly to make reservations (919-941-6000). Transportation will be provided from the airport. In addition, MCNC will provide free shuttle service between the center and the hotel.

Pre-registration: Attendance will be by pre-registration. The workshop will be limited in size to guarantee maximum effectiveness. Reservations will be accepted on a first-come, first-serve basis.

Registration Fees:

Before Oct. 22	
Registration fee	25.00
Student fee	10.00
After Oct. 22	
Registration fee	35.00
Student fee	20.00

The registration fee for the workshop includes attendance, lunch, refreshment breaks, and necessary supplies. Payment for all registration fees is required in advance.

Registration Form

Please mail this form along with your check (payable to MCNC) to:

Rebecca Gebuhr
MCNC
P.O. Box 12889
Research Triangle Park, NC 27709-2889

Name: _____

Address: _____

Street/PO: _____

City _____ State: _____ E-mail: _____

Please indicate special dietary considerations: (ie. vegetarian) _____

International Workshop on Logic Synthesis

FIRST CALL FOR PARTICIPATION

You are invited to participate at the International Workshop on Logic Synthesis to be held at MCNC, Research Triangle Park, North Carolina, on May 7-10, 1991. Presentations will focus on recent developments in all areas of logic synthesis, including:

- multi-level minimization
- boolean and algebraic decomposition
- technology mapping and translation
- area and timing optimization
- algorithmic vs. rule-based approaches
- finite state machine synthesis
- sequential logic synthesis
- retiming
- synchronous logic synthesis
- sequential circuit optimization
- PLD/FPGA based synthesis
- synthesis and verification
- synthesis based testing
- logic-level synthesis from high-level descriptions
- logic synthesis systems
- designer experiences with synthesis tools
- standard synthesis benchmarks

Sequential logic synthesis will be emphasized.

In order to promote free and open discussion, no cameras or recording devices will be allowed. To facilitate better sharing of ideas, the workshop will be limited in size. A proceedings of accepted proposals will be compiled and distributed to all participants. All submissions are voluntary and the proceedings are issued as a service to attendees.

SUBMISSION OF PROPOSALS

Participants wishing to deliver a scheduled presentation should submit 20 copies of an extended description of their work, not exceeding 8 double-sided pages (This is the limit that will be accommodated in the proceedings.). All proposals will be reviewed by the technical program committee.

Standard Benchmarks

A unique aspect of the workshop is the presentation of benchmark results. Benchmark documentation will be available in the fall. Please contact Saeyang Yang (919-248-1800) for benchmark information.

DEADLINES

February 15, 1991	Last day to receive proposals
March 27, 1991	Notification of acceptance
April 1, 1991	Mailing of workshop program and registration
May 1, 1991	Last day to receive proposals for presentation of benchmark results
May 1, 1991	Registration due date

For further information contact:

Franc Brglez
MCNC
P.O. Box 12889
3021 Cornwallis Rd.
RTP, NC 27709
919-248-1925
brglez@mcnc.org

A. Sangiovanni-Vincentelli
UC-Berkeley
Dept. of EECS
Cory Hall
Berkeley, CA 94720
415-642-4882
alberto@ic.berkeley.edu

Saeyang Yang
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P.O. Box 12889
3021 Cornwallis Rd.
RTP, NC 27709
919-248-1800
syang@mcnc.org

Rebecca Gebuhr
MCNC
P.O. Box 12889
3021 Cornwallis Rd.
RTP, NC 27709
919-248-1841
gebuhr@mcnc.org

Return this form to:

Rebecca Gebuhr
International Workshop on Logic Synthesis
MCNC
P.O. Box 12889
3021 Cornwallis Road
Research Triangle Park, NC 27709-2889

(Please print clearly)

Name:_____ Telephone: _____
Affiliation:_____
Street/PO Box:_____ Fax/Email: _____
City:_____ State/Country:_____

Please check:

_____ I wish to preregister for the workshop
_____ I wish to be added to the mailing to receive additional information
_____ I wish to contribute to the benchmark experiment and receive more information

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Statement of Publication Frequency

The *SIGDA Newsletter* is the official publication of the ACM's Special Interest Group in Design Automation. It is published three times per year; Summer, Fall, and Winter. It contains the minutes of the SIGDA advisory board as well as the minutes of the Summer (DAC) and Winter (ICCAD) general membership meetings. The *Newsletter* welcomes opinions, articles, and letters from its membership.

CALL FOR PAPERS

FIRST INTERNATIONAL WORKSHOP ON THE ECONOMICS OF DESIGN AND TEST

September 23 - 25, 1991
MCC, Austin, Texas

Sponsored by ACM SIGDA

in cooperation with IFIP WG10.5, MCC, Austin Chapter of the IEEE Computer Society

PURPOSE

The purpose of this workshop is to provide a friendly forum for discussing and exploring current and future test trends and how they are driven by the economics of delivering ever-increasing complex microelectronic systems. The primary focus will be on the economical ($) impact of test decisions directly associated with the design, manufacturing, or field maintenance of integrated circuits, boards, or systems.

AREAS OF INTEREST

Specific topics of interest include but are not limited to:

- Economics of ATE, e.g., mainframe testers, vs. verification testers
- Economics of DFT, e.g., scan vs BIST vs CrossCheck
- The relationship between design, test, and quality
- Quality and reliability effects on maintenance costs
- Cost effectiveness of BIST, full scan, partial scan, etc
- Concurrent engineering methodologies supporting testability and reliability
- CAD tools for analyzing design and test economics
- Expert systems for testability analysis, and synthesis
- Gate-array Test vs Standard Cell vs Full Custom
- Testability impact on time-to-market
- Physical defect and failure mode analysis
- Mathematical models for testability assessment
- Mixed analog/digital testing
- Multi-chip module testing
- Test standards
- New Test and Design methodologies

AUTHOR INFORMATION

Authors are invited to submit 12 copies of:

1) One page abstract containing 50-80 words, the title of the paper, author names, affiliations, addresses, fax numbers, telephones, and the person who will represent the work if the paper is accepted.
2) Either a summary of at least 500 words or a full paper.

For U.S. Authors Send To:
Dr. Magdy Abadir
MCC CAD Program
3500 West Balcones Center Dr
Austin, TX 78759
Tel: (512) 338-3611
Fax: (512) 338-3600

For Non-U.S. Authors Send To:
Prof. A.P. Ambler
Brunel University
Dept. of Elect. Eng. and Electronics
Uxbridge, Middx
UB8 3PH, UK
Tel: +44 895 74000 Fax: +44 895 58728

Authors of papers selected for presentation at the workshop will be asked to prepare an illustrated text for inclusion in the workshop proceedings. Selected papers from the proceedings will also be published in book form after the workshop.

IMPORTANT DATES

Deadline for Submission:
March 1, 1991
Notification of Acceptance:
May 1, 1991
Deadline for Final Version:
July 1, 1991

WORKSHOP ORGANIZING COMMITTEE

General Chair
Prof. S. Sastry, USC, CA

Program Chairs
Prof. A.P. Ambler, Brunel Univ , UK
Dr. M.S. Abadir, MCC, TX

PROGRAM COMMITTEE

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Prof. Melvin Breuer (US)
Dr. Serge Demidenko(USSR)
Colin Maunder (UK)
Prof. Will Moore (UK)
Prof. Bill Rogers (UK)
Prof. Gabriel Saucier (France)

SECOND PHYSICAL DESIGN WORKSHOP

Module Generation and Silicon Compilation

Nemacolin Woodlands, Laurel Highlands, Pennsylvania, USA

May 20-22, 1991

Sponsored by ACM's SIGDA

FIRST CALL FOR PARTICIPATION

You are invited to participate in the Second Physical Design Workshop to be held at The Nemacolin Woodlands Conference Center in the Laurel Highlands outside Pittsburgh, Pennsylvania on May 20-22, 1991. Presentations will focus in IC physical design with emphasis on recent developments in module generation and silicon compilation including:

- layout from netlists
- layout to/from schematics
- layout from behavioral HDL's
- performance driven layout
- experiences with silicon compilation
- layout benchmark results

The workshop will be limited in the number of attendees.

To facilitate comparison of results a set of standard benchmark circuits will be distributed by December 1990. Please contact the Benchmark Chair to obtain more information about the benchmarks for the workshop.

Participants wishing to deliver a presentation should submit 14 copies of a manuscript whose length does not exceed 3000 words, apart from figures, indicating the status of the work and significant results. Proposals will be reviewed by the Technical Program Committee. Proceedings will be published and distributed at the workshop. **The submission deadline is January 7, 1991.**

WORKSHOP DEADLINES

Jan. 7, 1991	Last day to receive proposals
Feb. 11, 1991	Notification of acceptance
March 11, 1991	Camera-ready copy due
May 1, 1991	Last day to receive proposals for presentation of benchmark results

For further information contact:

Workshop Chair
Antun Domic
HLO2-3/J3
DEC
77 Reed Rd.
Hudson, MA 01749
domic@cadsys.dec.com

Program Chair
Mary Jane Irwin
333 Whitmore Lab
Dept. of Cmp. Science
Penn State Univ.
Univ. Park, PA 16802
mji@cs.psu.edu

Benchmark Chair
Dwight Hill
AT&T Bell Labs
600 Mountain Ave.
Murray Hill, NJ 07974
dwight@allegra.att.com

Arrangements Chair
Steven Levitan
348 Benedum Hall
Dept. of Elec. Engr.
Univ. of Pittsburgh
Pittsburgh, PA 15261
levitan@ee.pitt.edu

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Please state your major professional field: _____

☐ **SUBSCRIPTION TO SIGDA NEWSLETTER ONLY:** Enclosed is payment of $5.00 for annual subscription. *(Note: Subscription is included with membership dues.)*

☐ Please send information on ACM Membership.

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* For ACM members renewing within the next three months, do not use this application. Simply add this SIG to your renewal invoice when you receive it and return with the appropriate additional payment.

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