acm SIGDA NEWSLETTER

SPECIAL INTEREST GROUP ON DESIGN AUTOMATION

Contents:

*Presented at 13th Design Automation Conference

SIGDA

ACM Special Interest Group on Design Automation

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MEMBERSHIP

SIGDA dues are $3.00 for ACM members and $5.00 for non-ACM members. Checks should be made payable to the ACM and may be mailed to the SIGDA Secretary/ Treasurer listed at left, or to SIGDA, ACM Headquarters, 1133 Avenue of Americas, New York, N.Y. 10036. Please enclose your preferred mailing address and ACM Number (if ACM member).

SIG/SIC ACTIVITIES

1) Informal technical meetings at NCC.

2) Formal meeting during National ACM meeting + DA Workshop.

3) Joint sponsorship of annual Design Automation Workshop.

4) Quarterly newsletter.

5) Panel and/or technical sessions at other National meetings.

FIELD OF INTEREST OF SIGDA MEMBERS

Theoretic, analytic, and heuristic methods for;

   1) performing design tasks,

   2) assisting in design tasks,

   3) optimizing designs through the use of computer techniques, algorithms and programs to:

   1) facilitate communications between designers and design tasks,

   2) provide design documentation,

   3) evaluate design through simulation,

   4) control manufacturing processes.

CHAIRMAN'S MESSAGE

The 13th Design Automation Conference in San Francisco was an outstanding event. The technical program contained a number of significant presentations, the tutorials were very helpful and well presented, and the arrangements, as usual, were top notch. Thanks and congratulations to Don Humcke and the rest of the committe for their hard work and dedication.

SIGDA held a business meeting at the conference which was attended by 18 persons of which 14 were SIGDA members. The meeting was scheduled opposite several "birds of a feather" informal technical sessions, and so I am not disappointed with the turnout.

General discussions revolved around our somewhat loose association with ACM which resulted in a consensus that since our group is strong and enthusiastically supports the Design Automation Conferences, our lack of participation in traditional ACM conferences (ACM National and NCC) while unfortunate, is not a cause for concern.

Luther Abel presented a financial report which indicated that we are financially healthy SIG, and that our surplus derives primarily from conference and proceeding profits. These are soft funds, and with the exception of the Design Automation Conferences, they lose money at least as often as they make it. The discussion then focused on the assessment for non-ACM SIG members.

The issues, as I have discussed in previous chairman's messages are: non-ACM SIGDA members are assessed $7.50 yearly for "data processing" and $1.50 head tax. This means that, in addition to the usual costs of newsletter mailing, etc., we are charged $9.00 for these members while they pay only $5.00 in dues. ACM SIGDA members office costs amount to approximately $5.00 yearly while dues are $3.00. It has been the feeling of your executive committee and board of directors that the degree to which non-ACM members are subsidized is out of line and that their dues should be raised.

This feeling was supported by the meeting attendees.

The next problem discussed dealt with the provisions in the bylaws for charging dues. I outlined this problem to you in my last message and proposed a solution. The attendees felt that while the executive committee with the advice and counsel of the directors should be able to set the dues, removing all limits on dues from the bylaws was not appropriate.

An alternative was proposed and strongly backed which 1) remains responsive to the need for dues revisions in response to ACM Headquarters assessment changes without continued revision of the bylaws, and 2) retains a limiting function to prevent the dues from being increased excessively by an irresponsible administration. Briefly, the proposal is to set the dues floor at $4.00 for members and $8.00 for non-members (providing a $1.00 subsidy for both classes currently) and to allow an increase of not more than $2.00 per year to be

imposed by the executive committee with the advice and counsel of the directors. Under this scheme, the rate of dues increase is controlled and the time constant for substantial increases will allow members to effect the increases by exercising their rights of officer selection and/or bylaw revision if a dues increase pattern is felt to be excessive or unnecessary.

In a straw vote of the attendees the alternative received unanimous support, and it is my intention to submit it to you in the form of an amendment to Article III. Section C of the Bylaws in accordance with Article VIII of the Bylaws and the rules of ACM. Which states that:

A. An amendment to these bylaws may be proposed by a resolution adopted by the Executive Committee or by a petition signed by at least 10 members.

B. Within 60 days after receipt by the Secretary-Treasurer of the proposal of an amendment, the Secretary-Treasurer shall conduct a mail vote on the amendment. The proposed amendment shall be reviewed by the Chairman of the Committee on Special Interest Groups and Committees prior to the mail vote on the amendment. Ballots shall be mailed to all members of the Group and shall state the last day for receipt of a voted ballot by the Secretary-Treasurer. This date shall be 30 to 60 days after the last ballots are mailed. The amendment shall become effective if it receives a majority vote of one-fourth of the Group membership, with the effective date falling 60 days after the final receipt date stated on the amendment ballots.

SIGDA will hold elections next spring for Chairperson, Vice Chairperson, and Secretary-Treasurer to take office on 1 July 1977. I will soon be appointing a nominating committee in accordance with ACM rules. The chairperson of this committee will be announced in the December Newsletter. In the meantime, if any of you are interested in running or wish to place another's name in nomination, please call or write me. The jobs require people who care about SIGDA and its future, but the work load is really minimal. Please consider running for an office!

Bill Van Cleempt is doing a great job organizing the Symposium on Design Automation and Microprocessors to be held 24-25 February 1977. Read the call for paper elsewhere in the Newsletter and contribute!

1

A DATA STRUCTURE
FOR THE DESCRIPTION AND THE HANDLING
OF ENGINEERING DRAWINGS

by

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1. Introduction

The specifications of a data structure are essentially linked to the model which it is wished to represent, to the functional links which it is wished to obtain amongst the various data and the action which it is wished to take on such structure. [1, 2]

An engineering drawing is the two-dimensional representation obtained according to precise accepted standards of three-dimensional objects.

Thus the data structure representing an engineering drawing will surely contain all the connections among the two-dimensional graphic elements of which same is composed and should contain a complete description of the three-dimensional object represented, so as to allow action on same at any level whatsoever through its two-dimensional representation.

On the other hand, by analyzing the various phases of the design process which lead to the production of final working drawings, it is to be noted that the three-dimensional model of the mechanical part becomes increasingly detailed and complex, as are the drawings used to illustrate same.

Moreover, the quantity of drawings which accompany the various phases of the design process is ever greater and the types of action to be taken on such drawings refer to an ever greater extent to details which do not substantially alter the piece from a functional point of view, but which complicate its shape to an appreciable degree.

Furthermore, at such a level, the drawing contains a large amount of data of a technological and constructive nature which are also continually changed or amended.

The use of computer aided drafting systems is justified where large numbers of considerably complex drawings are involved.

In the field of mechanics, this occurs as may be seen, during the final stage of design where the manner of action taken as to the object represented essentially concerns details (from the point of view of the shape of the piece); it would not therefore seem reasonable at this level to use for the storage of the drawing, a data structure which contains a complete and faithful representation of the illustrated mechanical part given its great complexity. [3]

It will therefore be sufficient for the data structure for the handling of the drawings to contain only those functional links which are of interest at the detailing design stage.

2. Analysis Of Engineering Drawings

An engineering drawing, as mentioned in the introduction above, is the final document resulting from all the phases of design, and thus constitutes the specifications for production, hence containing a complete series of data which are not limited to a graphic description of the shape of the piece illustrated according to traditional standards, but refer to the technological processing specifications such as dimensions and dimensional tolerances, surface roughness and manufacturing methods.

It may therefore be seen that engineering drawings may be considered as being a graphic structure divided logically and functionally into two parts: the graphic structure representing the shape of the piece and the graphic structure representing all other data.

These two different structures may be thought of as being arranged on two separate sheets, superimposed one over the other, taking into account, however, the fact that there exist certain connections between the said two sheets. More precisely, the graphic structures which represent dimensions or symbols are coupled to points or lines of the graphic structure representing the shape of the piece.

In many kinds of non engineering applications, a drawing is composed of a more or less numerous series of repeated graphic elements (symbols, diagrams, etc.). A typical example is that of electric or electronic circuits, plant drawings, etc..

The data structure of a drawing of this kind may be suitably organized in a hierarchical fashion by establishing basic patterns used as primitives and more complex figures, built up by means of such primitives, which may in turn be appropriately repeated in generating the final drawing. [4]

In the case of mechanical engineering drawings, it is not possible to identify any basic primitives which may then be suitably introduced into a hierarchical structure, and hence the drawing will be structured at the lower graphic level namely, that of points, segments and arcs. [5] [6]

The objects illustrated in engineering drawings are three-dimensional, finite bodies which are thus defined in space by finite and contiguous surfaces.

Each of these projected finite surfaces gives rise to a closed polygonal. From this point of view, an engineering drawing may be thought of as being read in the form of a series of closed polygonals, each of which represents the projection of a surface of the piece.

This would always be true were it not for the fact that for reasons of clarity in the drawing, the hidden lines (that is, those polygonals or parts thereof covered by other surfaces to be found between such polygonals and the projection point) are eliminated.

The visible parts of the partially hidden polygonals, may be seen as open polygonals whose ends are determined and hence coupled to those polygonals which define anteriorly arranged outlines.

An engineering piece, moreover, is not univocally characterized by a pure geometrical form, there being functional links existing between the various surfaces which define same; there exist, that is, surfaces which are functionally dependent upon others.

This dependency may be maintained in the drawing by having recourse to open polygonals which in fact create a hierarchical link among the polygonals themselves.

Moreover, in such a way it is possible to eliminate all those parts which would be duplicated since they belong to contiguous polygonals.

The coupling points of the open polygonals which will only be those at the beginning and the end, may be at the turning point of other polygonals.
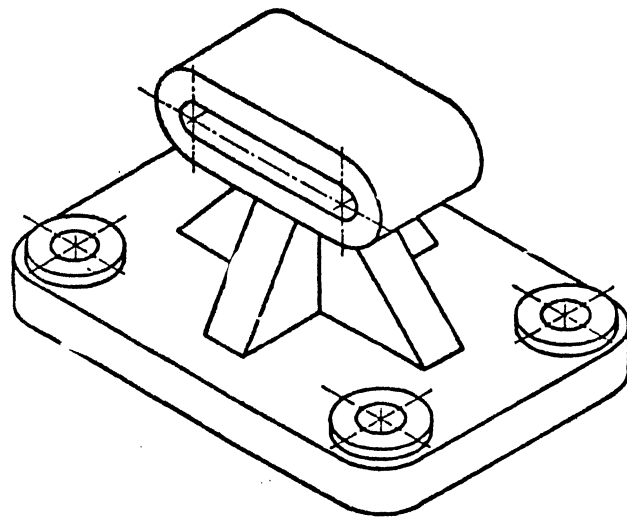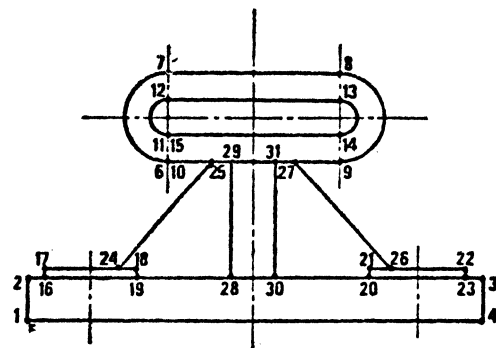

Figure 1.

In the case of side coupling, the point will be conventionally referred to with the term "half hinge". In Figure 1, it is possible to identify as closed polygonals, the turning point sequences 1-2-3-4-5, 6-7-8-9-10 and 11-12-13-14-15; whilst open polygonals may be identified in 16-17-18-19, 20-21-22-23, 24-25, 26-27, 28-29 and 30-31.

The points 16 and 19, 20 and 23, 24 and 25, 26 and 27, 28 and 29, 30 and 31 are half hinges. Again, by continuing in the analysis of an engineering drawing, it may be seen that there exist local details such as fillets and chamfers, that it would serve no purpose to introduce explicitly into the structure illustrated in the drawing. For example, the end of the shaft shown in Figure 2A is to be taken, and therefore stored, as a perfectly cylindrical section with local variations as indicated schematically in Figure 2B.
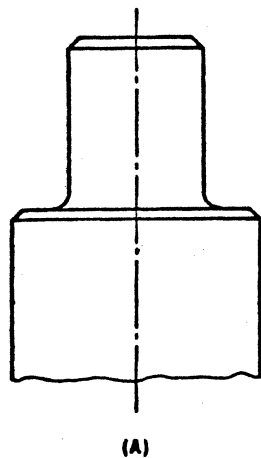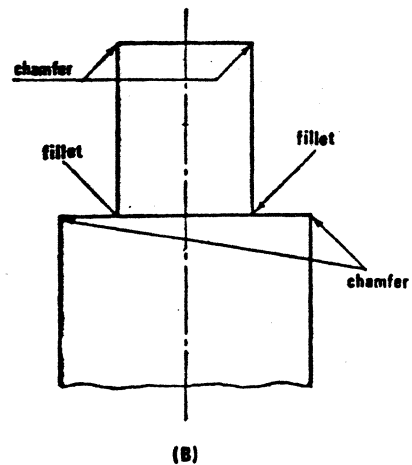
3

Figure 2.

(A)   (B)

2.2 Technological Data (Sheet 2)

As regards the technological and dimensional data, same are indicated in a conventional manner in the drawing, using standardized and therefore ripetitive graphic structures and a series of alphanumerical symbols, varied from time to time.

In this case, the use of graphic primitives may therefore be considered in order to introduce this information into the data structure representing the engineering drawing, which allow the generation of:

- linear dimensions

- circumference dimensions

- arc dimensions

- angle dimensions

- symbols relating to the surface condition

- special notes.

The single technological data could be obtained by characterizing each of these primitives by means of a series of free parameters associated with a string of alphanumerical symbols, containging the relative information.

3. Modification

The types of action taken with regard to modifying a drawing, in addition to additions or erasure of parts, are essentially of two kinds:

- change in the shape of the piece

- change in the technological data.

In the former of these cases, the change in shape consequently leads to the adjustment of all the relative technological data. This means cancellation of all the information related to parts which have been taken away and up-dating of the data relating to those parts of the drawing which have been modified.

The second type of action only concerns the technological data and is therefore limited to merely changing the relative alphanumerical data, or to modifications as to formats or references. In all events, none of these operations may be such as to affect the representation of the shape of the piece.

4. Proposed Data Structure

From the analysis of an engineering drawing and the types of action which may be taken as regards same, a schematizable data structure as shown in Figure 3 may be derived. As may be seen, the drawing as a whole is subdivided into various independent "drawings" which represent its various views and sectional views, and thus have no other connection if not that of reciprocal position.

In each of these drawings, it is possible to identify, as has been seen, two different levels of graphic information: one containing only the representation of the piece and the other containing all its technological and dimensional data.

In conformity with the analysis carried out, the level representing the shape alone is composed of a series of open and closed polygonals, and the level representing the technological and dimensional data is composed of three different categories of graphic structures representing, respectively:

- dimensions

- symbols

- notes.

The single technological and dimensional data are stored in the data structure by means of single alphanumerical strings and the free parameters which represent the corresponding primitives.

Between the level of the technological data and that of the shape of the piece, exist, as has been seen, a number of connections in the sense that the technological and dimensional
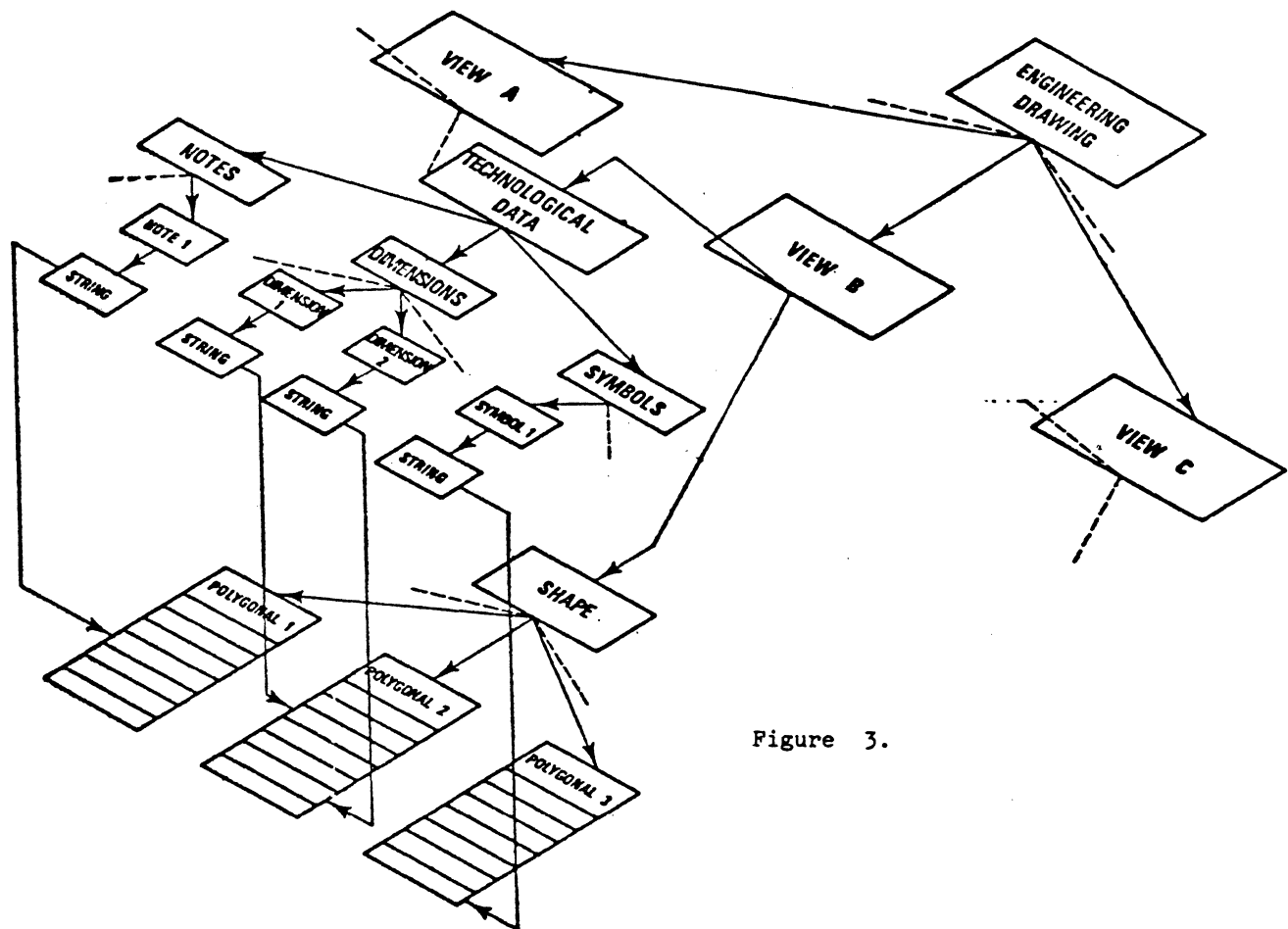
4

Figure 3.

data are coupled to particular elements of the shape, being dependent upon same.

In the data structure which will be illustrated hereinbelow, reference will be made to a single drawing (that is, to only one view or sectional view) since the only link existing between the single views or sectional views is that of reciprocal position.

4.1 Data Structure Relating To Shape (Level 1)

The shape of the piece is stored by means of a series of lists connected one with the other, each of which represents a polygonal.

Each element of the list is structured in such a way as to contain the following information:

- x, y coordinates of point

- code indicating type of line (blank, solid, dashed)

- function code indicating which kind of curve joins the point

In cases other than that of a straight line, same is replaced by a table pointer

setting forth all the parameters which characterize the sections of the curve:

- pointer at next point of polygonal

- pointer at possible points of coincidence

- pointer of connection in the event of point being a half hinge

In such a case, the pointer points to the initial point of the side of the polygonal to which the half hinge is coupled.

- code of local variation used for chamfers and fillets

In the event of there being a chamfer or fillet corresponding to the point, it points to a table containing a code of variation (chamfer or fillet) and the relative numerical value.

- chamfer pointer   This pointer serves the purpose of connecting up with the other point defining the chamfer (in fact, this point does not necessarily have to be contiguous).

An element of the list will therefore be structured as shown in Figure 4.

X Y	· - coordinates of the point
L	- line code
F	- function code
PC	- coincidence pointer
PH	- half hinge pointer
PV	- local variation pointer
PC	- chamfer pointer
PN	- pointer to next point

Figure 4.

4.2 Data Structure Relating To Technological Data

The technological data are defined by means of the primitives established from time to time by a series of parameters. In all the primitives, the following types of parameters may be identified:

- coupling pointers to elements of the structure which describe the shape of the piece

- format code

- parameters of position on plane. These parameters are the coordinates of a characteristic point used both for the positioning of the technological data and for the recognition thereof

- string pointer. Since the alphanumerical strings relating to each set of technological data may have very differing lengths, easily put to editing, same are stored in a suitable structure. It therefore becomes necessary to have a pointer to said structure for each set of technological data.

More precisely:

- Linear dimensions

XR YR	- Coordinates of point for positioning and recognition
F	- Format code
PS	- Pointer to string
P1	
P2	- Coupling pointers to two points of the structure describing shape.

- Circumference dimensions

XR YR	- Coordinates of point for positioning and recognition
F	- Format code
PS	- Pointer to string
PC	- Coupling pointers to circumference centre.

- Arc dimensions

XR YR	- Coordinates of point for positioning and recognition
F	- Format code
PS	- Pointer to string
P1	- Coupling pointer to the second point of the arc.

- Angle dimensions

XR YR	- Coordinates of point for positioning and recognition
F	- Format code
PS	- Pointer to string
P1	
P2	
P3	- Coupling pointers to four points of the structure describing shape.
P4	

- Notes

XR YR	- Coordinates of point for positioning and recognition
F	- Format code
PS	- Pointer to string
XS YS	- Coordinates of point used for positioning string
P1	- Coupling pointer to shape.

- Symbols

XR YR	- Coordinates of point for positioning and recognition
F	- Format code
PS	- Pointer to string
P1	- Coupling pointer to shape.

Figures 5 and 6 show by way of example, a drawing and its corresponding structure.
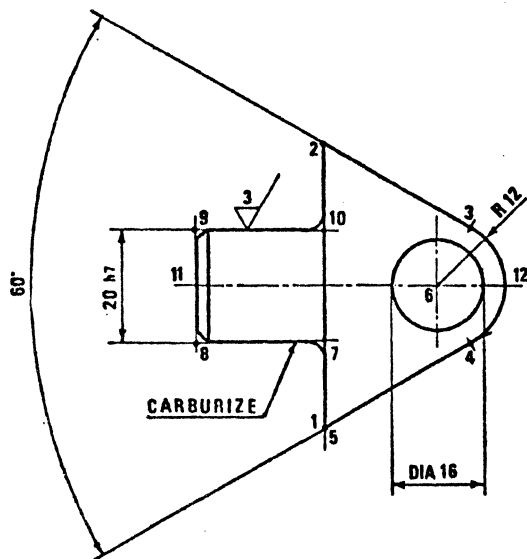

Figure 5.

6

Figure 6.

5. Possible Modification Operations

According to the schematization introduced, a distinction will be made between action regarding the graphic structure corresponding to the shape of the piece and action as to the structure corresponding to all the other data. Taking into account the fact that there exists a connection between the two structures and that the graphic data are subject to the shape of the piece and not vice versa.

5.1 Modification Of The Shape Of The Piece

Action as to the shape of the piece may be taken at two levels:

- modification which will be termed "dimensional", which does not involve the sequence of graphic elements making up the polygonals, but merely changes their numerical values (coordinates, length, etc.)

- modification which will be termed "functional" which does affect the sequence of graphic elements (erasure, replacement, insertion of parts).

5.1.1 Dimensional Modification.
As far as the dimensional modification of the shape is concerned, the following possibilities have been identified:

- change in the coordinates of a point common to two consecutive segments of a straight line (this leads to a variation in the length of the two segments concurrent at such point). See Figure 7/1.

- translation of a segment of a straight line comprised between two other segments (translation occurs in an orthogonal direction to the segment itself and its extremities are bound to lie on the straight lines defined between the previous and following segments). See Figure 7/2.

- rotation of a segment of a straight line around its extreme point (the other point being bound to belong to the polygonal section contiguous at such point). See Figure 7/3.

- variation of the centre and/or radius of a circumference. See Figure 7/4.

- variation of a centre and/or radius of an arc of a circumference extending between two segments maintaining the tangency at its extremes. See Figures 7/5, 7/5 and 7/7.

- variation of the centre and/or radius of an arc without the conditions of tangency at its extremes. In this case the initial and end points of the arc are determined by fixing their belonging to the polygonal sections before and after same. See Figures 7/8, 7/9 and 7/10.

- variation in the characteristic value of chamfers and fillets. See Figure 7/11.

In all these cases any information of a technological nature which refers to pieces which have undergone functional modifications is automatically adjusted to the new values.
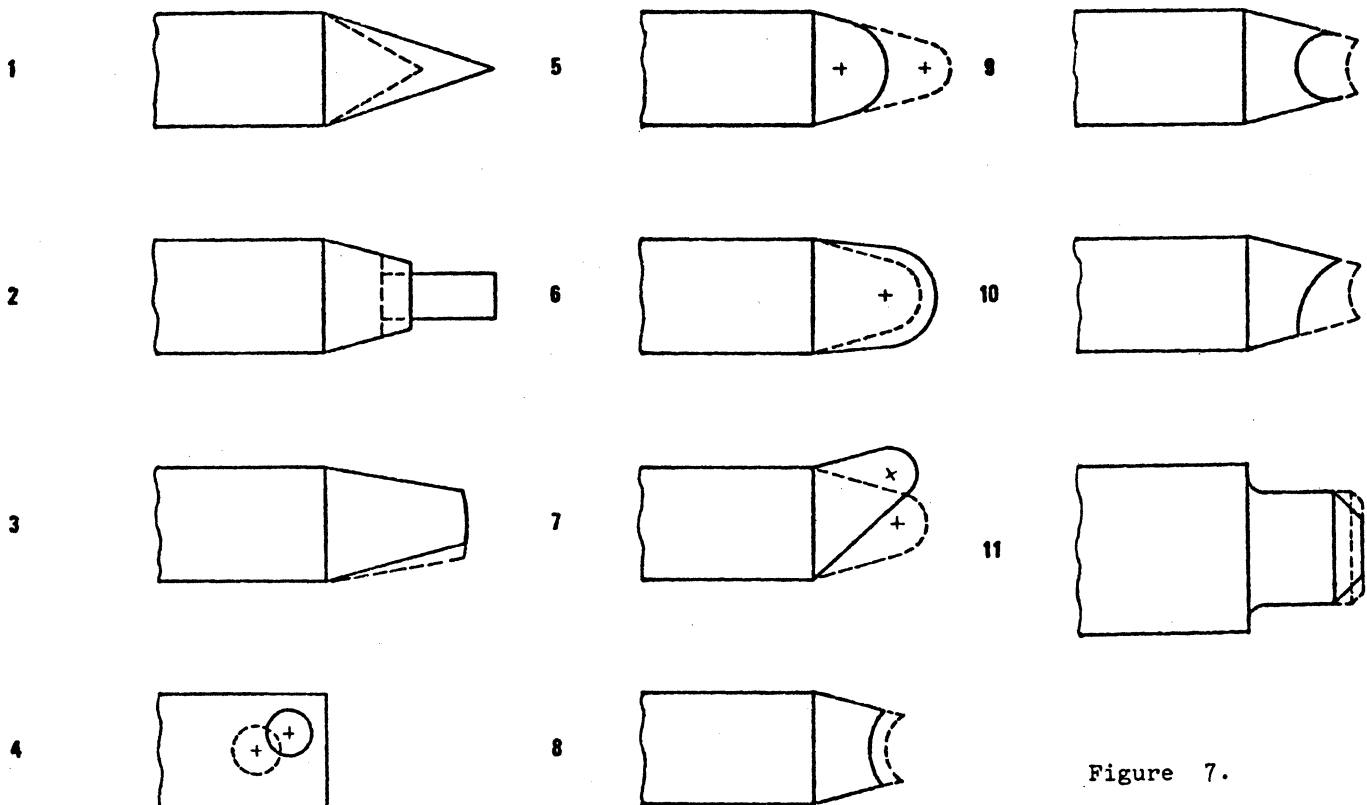

Figure 7.

3.1.2 Functional Modification.

As regards the functional modification of the shape, the following possibilities have been identified:

- erasure of an entire open or closed polygonal

- append of a new open or closed polygonal

- replacement of a part of a polygonal; that is, erasure of the sides of the polygonal included between two points and insertion between same of a new sequence.

The half hinges which are attached to the sides of the polygonal are cancelled or transformed into the extreme points of an open polygonal which may either be erased or completed.

Any technological information having points of connection with the erased parts is automatically cancelled.

3.2 Modification Of Technological Information

The technological information, whilst having points of connection to the shape of the piece, has some degree of freedom as regards its positioning on the plane of the drawing.

A diagram of the various types of graphic information evidencing these points of connection and their possibilities of displacement, is given in Figure 8.

As regards the modification of these graphic structures, the following possibilities have been identified:

- displacement of the graphic structure according to its degree of freedom

- variation in format of dimensions

- editing of relative alphanumerical string

- erasure of one or more graphic structures

- addition of new graphic structures.

6. Comments And Conclusions

The illustrated data structure centres upon the open and closed polygonal concept: this makes it possible to express in terms of structural links the relations of both a functional and positioning nature relating to the various surfaces defining the illustrated piece.

Moreover, the implicit sequentiality of each single polygonal, in addition to expressing the continuity of the surfaces defining the piece in terms of structural links, also optimizes the efficiency of the data structure.

In fact, when used for loading the structure, either entirely by means of digitalization or making use of graphic systems for generation of drawings, same compacts the storage of the points which define the drawing, reducing to a minimum, the duplication of the stored points. This is important because clearly the response time for any action as to the structure, same being based on lists, is proportional to the number of stored points.

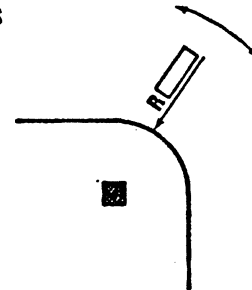It is moreover clear that also the output phases are optimized since blank paths are reduced to a minimum.
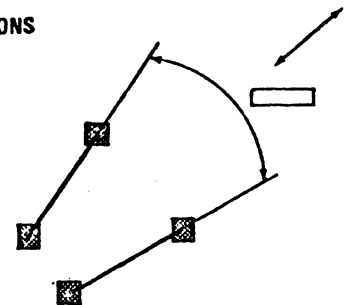

LINEAR DIMENSIONS
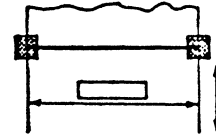
CIRCUMFERENCE DIMENSIONS
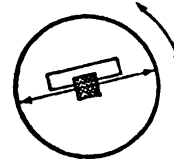
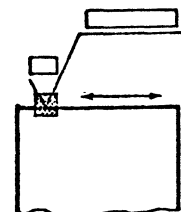**ARC DIMENSIONS**

ANGLE DIMENSIONS

NOTES AND SYMBOLS

Figure 8.

This type of approach also implicity proposes a description and reading methodology for engineering drawings, given the fact that it makes it possible to identify the links existing between the outlines of the piece based on its relative positioning or on its functional dependancy.

If the data structure is loaded with a sequentiality which does not reflect the continuity of the engineering drawing examined, whilst loosing in efficiency it causes an increase in the number of stored points, but maintains all its possibilities.

The quantitative data relating to overall dimensions and response times as a function of the complexity of the drawing and the loading procedures of the structure will be available upon conclusion of the implementation presently being carried out on a Hewlett-Packand 2100 System,(16K core, disc, magnetic tape) to which are connected a graphic terminal, namely, Tektronix 4010, and a graphic tablet, namely, the Tektronix 4954.

7. Acknowledgements

8. References

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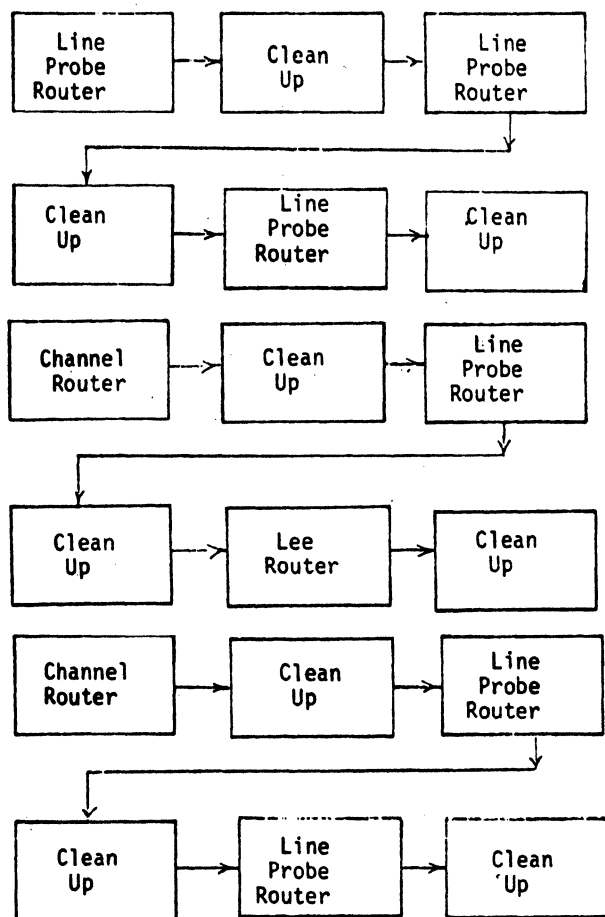
Figure 9. Blocked Access to Edge Connector Pads.

Figure 8. Typical Cleanup Processing Sequences Being Evaluated.

PRODUCTIONS'S INTEREST IS IN ITS ECONOMICS

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System Description

CAD for LSI design means a total package from basic circuit analysis up to programs which generate tapes for numerical controlled pattern generators and testing equipment.
The flow of such a system is given in Fig. 1. It shows the usual diagram of circuit analysis, cell library, logic simulation, functional and d.c. parametric test generation and an automatic layout system.

COMPUTER AIDED DESIGN SYSTEM

FOR DIGITAL IC's IN LOCMOS
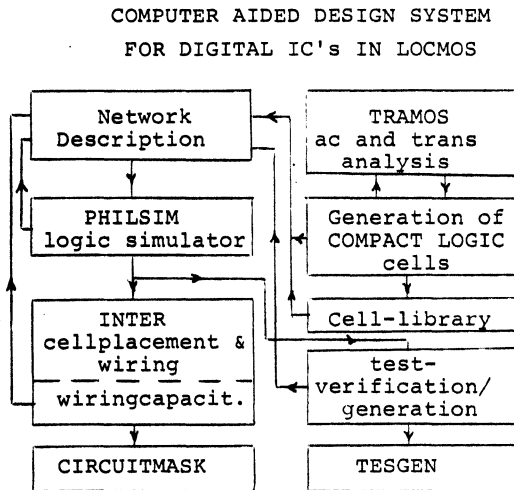
fig. 1.

The cells in the cell library range from simple gates and flipflops to more complex functions up to nine input variables; also ROM- and RAM bit cells are available. An example of a cell structure is given in Fig. 2. Each cell has a constant height and variable width. The in- and output signals can be reached both from the top and the bottom of the cell.
The library contains about 120 items which are all characterized with respect to layout as well as electrical and logical behaviour, including time delay factors.
Custom designs and LSI's in general often need something special. If a CAD system is not capable of handling these specialties without losing its efficiency or without becoming difficult to handle, users are not willing to accept that system as a tool. To bypass this problem a library is developed which contains so-called "primitives", examples of which are shown in Fig. 3.

COMPACT LOGIC CELL

$$F = \overline{(C1+C2) \cdot B1 + A1 \cdot A2}$$

fig. 2

fig. 3

With these basic items, which are related to the single process steps, the designer is able to develop all kinds of specials, which will not only satisfy the customer specification but also will fit into the rest of the system.

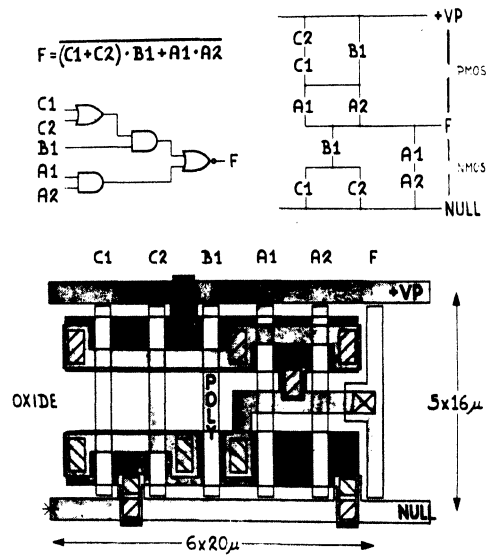The first step after the acceptance of the development of a design is to convert it into functions provided by the library. If necessary a special building block is developed. For this purpose the analysis program is used to check the electrical properties. A correlation has been established between the calculated values and the diffusion product with an accuracy of about ten percent.

When all building blocks are available, the network is coded for the computer, where macro facilities, parameter descriptions, etc. are available to reduce the amount of work. (see Fig. 4.)

fig. 4

To check the logic behaviour against the original specification a time dependent logic simulator is used. The designer "feeds" his circuits by describing the input pulses and he gets back the response of the circuit as calculated by the computer. (See Fig. 5.)

A loop of checking and changing the logic set-up is started until the specifications are met.

At this moment the description is fixed and this one will be used by each consequent step.

It is very nice to have a functional working circuit, but it is useless if it cannot be tested. One has to make sure that not only testing can be done, but that it can be performed on a production basis, which means on a standard automatic tester in a short time. For this purpose the test engineer works with a logic test verifier which deals with logic stuck at one/zero defects and a program that generat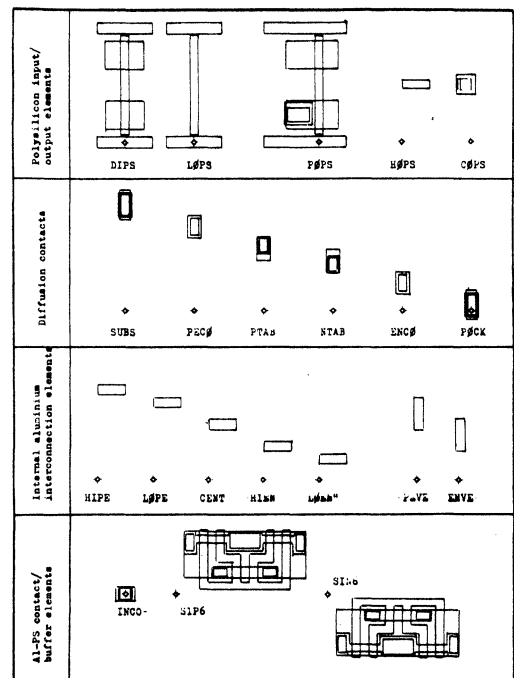es the d.c. parametric tests. With these aids he is informed about the defects which can or cannot be detected, how efficient the test sequence is, etc. (See Fig. 6.). As LSI test equipment is not cheap, this is an important step which, if not carefully handled, will cost a lot of money afterwards.

fig. 5

fig. 6

Once the logic has been designed and it has been proven that testing is not a problem, the layout phase can be entered. As all information to generate the layout is available this is not a large problem.
Because of the constant height of the cells it is obvious that they are placed in rows. This is in our system done by hand as we have seen sofar that in general the designer can come up with a starting solution which is even as good as one produced by a computer program, but at far less costs.
The placement information is added to the original network description and also stored in the computer. As both the interconnection scheme (derived from the network and placement) and the cell layout (retrieved from the library) are known, an automatic wiring routine is able to generate a double layer interconnection pattern. The outcome is presented to the designer (see Fig. 7), and as the first shot in placement never is 100 % good as well as the wiring algorithms, which do not take years, are not 100 % optimal a loop starts of iterative and partly interactive man-machine work.
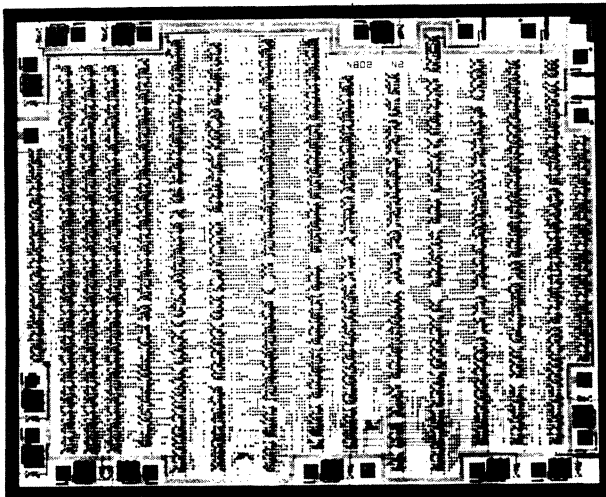

fig. 7

The program calculates the contribution of the wiring to the circuit delay and this is fed back into the network. This enables the designer to make a final check of his logic with the actual final layout data.
After this is accomplished we end up with two magnetic tapes, one is driving the mask pattern generator and the other is to control the automatic tester.

Production requirements

The system as described above is not new in its set-up but several systems like this have never come further than the research buildings although they are only worthwhile to develop if they are used for production purposes because here is where cycle time, hit rate and design efficiency are directly related to money or market position.
A CAD system for production purposes has to cope with several aspects which seem to be contradictory.
You have to design faster, but chip area may not grow.
You have to be advanced but the failure rate must be lower.
You are forced to standardise, but flexibility for specialties and design freedom may not be cut down to zero.
The way of operation in the design cycle has changed drastically, but it must be easy to learn for existing designers, etc.
So more factors are involved than just that the system produces a good chip.
Searching for acceptable compromises the following starting conditions were formulated:

- Develop the system not in research but in the middle of the users, step by step, not starting from a complete specification, because full specifications of a really new approach tend to contain more wishfull thinking and utopia's than realistic thoughts about tools for daily use. The constant feedback of users gives better information of what is really needed next.
- Do not use initially high professional programmers because they do not understand the design world nor do designers speak programmers slang.
- Use a small computer to do the job, so one is not invited by the hardware to be wasteful, minicomputers are becoming cheaper, no large system-overhead costs have to be paid and one can schedule the machine without being pushed off by accounting-, salary-, sales- and management programs which have always higher priority. Designers need fast turnaround.
- Do not try to make the computer "creative" because per definition she is not, and simulating that costs a lot of dollars.
- Do not give a designer more information than he is asking for because either he does not want it or he is not yet susceptible for it; in both cases it is a waste of effort, paper and money.
- Put more emphasis on the fact that the algorithms are 100 % safe rather than 100 % optimal and allow adjustment by the designer.
- A circuit should only be described once during the design cycle, to avoid translation errors, and double checking.
- Make the system transparent to future users, not a magic black box.

Hardware and algorithms

Keeping these things in mind the LOCMOS design system is developed on a small 64 K/16 bit word oriented computer, disc and magnetic tape backing store, a tektronix storage display and a plotter.
As in the first place the aim was to be safe the algorithms in use are reasonably well established.

The model in the circuit analysis has been kept simple and the number of nodes that can be calculated in one run has been kept to maximum 100. The reason is that if one has to do circuit analysis in detail on a complete LSI to get the last nano-second

out, the production never will be able to
make such a product with reasonable yield.
So for the normal applications a cross
check between model and production was made.
The time delays as function of the fanout
were calculated and these factors are auto-
matically produced when the network is en-
tered in the computer.

The simulator/verifier uses a slightly mo-
dified version of the look ahead algorithm
as described by Ulrich [1].
Here a lot of attention has been paid to
features which are not absolutely necessary
but which make it easier to detect errors,
make sure everything has been excercised,
warm starts, etc.

In the layout phase the partitioning, if
necessary, and the placement of the cells
is done by hand. Here the knowledge of the
designer who has struggled with his product
during the logic set-up is used, rather
than to excercise with an algorithm. This
has two reasons. In the first place the
computerprograms are not yet so extremely
clever, that they beat the designers'
brains evidently and second, because of the
reason just mentioned the man still has to
make himself thoroughly acquainted with the
computer placement to be able to do the
final optimisation and this costs as much
time as doing it himself right from the be-
ginning and he is more involved.
For the wiring a combination is used of
the algorithms described by Lee [2] and the
one mentioned by Schweickert [3].
It is a routine, for two layer wiring, con-
sisting of aluminum and polysilicon.
The algorithms used do not give in all ca-
ses the optimum solution, as they are also
dependent upon the placement.
For this reason the possibility has been
built for the designer to interact with the
machine in front of a storage tube display.
He may shift, replace or add cells in a row,
as well as change the wiring which is pro-
duced between rows. All changes are con-
trolled and checked against the original
network.
Although we are rather confident that the
existing program is error-free, we still
do a cross check at the end. Having the
wiring and the cell placement, we generate
via a separate procedure a network and com-
pare that with the original one. In this
way we are absolutely sure that the cir-
cuit on the slice is the circuit we de-
veloped.
When special blocks have to be incorporated,
like large output stages, a complete ROM,
etc., not only the logic connection is
checked, but also whether these items and
connections, as they have to be brought in
by hand, fulfill the process design rules.
To generate a ROM we have a special pro-
gram that produces the layout starting from
an adress-content table. The complete ROM
is then placed in the reserved area in the
total circuit.
To check the layout when cells are generated
and when larger portions are glued together
a program is available with extensive fea-
tures on design rule checking and pattern
manipulation both in batch and interactive
mode.

System Failures

Up to now about one hundred circuits have
been developed with the LOCMOS design system.
Their complexity ranges from 700 to 1800
gates, plus ROMs and RAMs with chip areas up
to 22 mm^2. Two of them did not meet the ori-
ginal specification. On the first one it
turned out that a part of the function never
was correctly simulated and by consequence
failed. On the second the program had not
given adequate information about the delay
added by the wiring.
The total amount was given but the long de-
lay line effect that came together with it
was not taken into account. So one is to
blame the system, for the others the first
shot was correct.

Design Cycle

Development of the network, special cells,
if needed, and logic simulation until check-
ed circuitry takes 2 - 3 man-months depen-
ding on the complexity.
Generating an adequate and efficient test-
sequence requires about 4 - 6 weeks.
The designer needs 3 - 6 weeks to generate
the layout. In this period he is able to
change his philosophy regarding the place-
ment a couple of times completely and to do
optimisation on each of them.

When the specification of an existing design
changes, all information is still available
and if just a couple of gates have to be
changed, only a few computer runs are neces-
sary. When a larger part is altered some
weeks may be involved.

Hand-versus Machine layout

A couple of designs, made by hand, have
been taken and reworked with the help of
the machine. It turned out that the designer
working with the system, generates the lay-
out on the same chip area with a factor
varying from six to nine gaining in time.
The most important point was however,
that the hand-layouts contained errors which
indicate that it is nearly impossible to
make a circuit of up to 8000 transistors of
mostly wild logic, error-free in the first
go.
The reason for this result is that the cells
themselves are made without sacrificing area
to the fact that they have to fit into a
system. That is why they are called COMPACT
LOGIC cells. Also the fact that the wiring
can approach a cell from both sides has the
advantages that the algorithms can be kept
simple and that no extra area is lost by
going across or around a cell.

Education and Transfer

Both a company like Philips, which comprises
several design centres, and the LSI-design
field itself, with its large variety of cus-
tomers, require that a CAD system can be
learned easily.
When it takes half a year or more before a
man is able to use CAD, the benefit is alrea-
dy doubtfull and it will be very difficult
to get such a system accepted as a tool for

day to day use.
Besides, a manufacturer never can have all
the knowledge of the different fields of
technology as e.g. computer industry, tele-
phone equipment, consumer electronics,
military developments etc. So it must be
possible to teach a customer how to use the
system and to be sure that the product he
designs with it works according to specifi-
cation.
Both for internal and external customers a
course is given of one week and in the week
following some guidance is offered when they
start their designs. After that they work
on their own, also outside customers, which
may be illustrated by the fact that one
customer designed a 15000 gate system di-
vided over 12 chips after following the
course by sending carddecks and inspecting
the computer outputs which were sent back.
We as a manufacturer do not know the con-
tents of the chips with respect to the lo-
gic functions but we produce and test the
parts and we have seen the final system
working.

As several centres must be able to use the
system and not all have the same computer
equipment, machine language could not be
used. This may be considered as a draw-
back because programs written in high level
language tend to take more core and some
more run time but the advantages are more
important. The programs can be transfered
easily, which is impossible when machine
code is used. Coding and debugging costs
less money and more people are able to un-
derstand what is coded so the system does
not die when the programmer leaves.

Summary

The LOCMOS design system is in use comple-
tely in five different centres and partly
in another four. A group of 3 programmers
is available to maintain an expand the
program possibilities.

As testprogram- and layout- generation go
in parallel the typical turnaround time
for a circuit of 1200 gates from start to
tapes for mask and tester is four months.
The computer expenses amount to about
$ 3500.--.
So in half a years time it is possible to
make parts which are correct in the ini-
tial version and that is exactly what the
product manager is looking for.

1. E.G.Ulrich Communications of ACM Vol 12/2

2. C.Y.Lee IRE Transactions on electronic
            computers Vol EC-10

3. D.Schweikert e.a. Proceedings of the 10th
            design automation workshop.

FROM THE EDITOR

This issue is almost entirely devoted to material from
the recent 13th Design Automation Conference held in
San Francisco June 28-30. It is being sent (comple-
ments of SIGDA) to all attendees, in the hope that non-
members of SIGDA will decide to join the group. All
of the papers included here are ones which were
refereed for and presented at the 13th DAC, so the
material should be of interest to a wide audience.
Hope you benefit from it!

The next (December) issue copy deadline is October 27;
once more I encourage your contributions to this
Newsletter.

Rob Smith
8/20/76

P.S. Join SIGDA -- if you're not now a member!

Errata for 13th DA Proc. (Jones/Nelsen paper) page 349:
Table 5: line 2: change "10,000,000" to read
"1,000,000".

CLUSTERING METHODS AS PARTIAL SOLUTIONS
TO THE SPACE ALLOCATION PROBLEM

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Abstract

The paper presents a three phase approach to the space allocation problem. The first phase is to identify the activities that can be considered as members of component groups by classification methods. Secondly to find organizational form for each of the groups and to locate the members into the layout. Thirdly to find organizational form for the whole system and to locate the groups in the system.

Introduction

A survey of space allocation procedures will produce many hundred procedures. From early work by Whitehead and Elder and by Buffa and Armour procedures have been generated from many different viewpoints. The problem presented by Whitehead and Elder was to find the optimum layout for an operating floor of a hospital given (a) the activities that had to be located, (b) the personnel and their relative salaries, and (c) the frequency of movement between activities by different personnel groups. The criteria used in this work was to minimize travel cost computed as the distance x frequency x personnel salary (by group). In general the space allocation problem is one of finding the spatial configuration and the allocation of specific activities to the configuration, given a criterion function.

Existing Methods

It is not intended in this paper to cover all of the methods that are available for space allocation, but rather to illustrate a few recent developments. The methods can be considered as (1) heuristic (2) enumerative (3) dissections and (4) classification.

Heuristic

Until recently all of the approaches were heuristic. In the majority of cases the procedure is to select an activity, locate it and then select another and locate it in the best location relative to the first, and so on until all activities were located. ALDEP and CRAFT are examples of this approach. The problem of this approach is in the selection of the first activity to place, and to establish the order of the activities. A solution to this problem was presented at the DAC Conference in 1971 in Dallas by the author. The solution used a classification method to find the ordering of the elements, thus increasing the probability that an optimum could be reached.

Enumeration

In "The Animals of Architecture" by the author[1]

a list of the enumeration of polyominos (configuration of connected squares) was reported from research carried out by Read[2] and Lunnon[3]. In a further article by Matela and March entitled "The Animals of Architecture, A Census"[4] the enumerations were analysed to identify coefficients that would reduce the set of polyominos to a manageable size, given different criteria for the coefficient. The advantage of enumeration is that once a complete set of configurations exists, then it is only necessary to look through a catalogue to find the one configuration that is needed in the specific case. The disadvantage is in finding a coefficient that is able to discriminate and also be relevant to the different design problems that are encountered. An interesting offshoot of this work is the enumeration of bridges or cutsets that are possible within a polyomino. This work will be useful in arriving at layouts for houses given that there is a need for a certain number of component groups and a total number of activities. For example, in a house with nine activities in three groups the scanning procedure would simply find all nine cell configurations with two bridges or cutsets. Further analysis would determine which layout to select. Future work in this area will be useful in building design problems when coefficients can be generated to reflect the design criteria.

Dissections

Recent work by Steadman[5] and Mitchell[6] is based on the graph theoretic work of Tutte[7]. The work on dissections is a subset of the general space allocation problem. In dissection enumeration there is the constraint that each configuration must be contained by a simple rectangle. Mitchell[8], in recent work has produced a design system using the dissection enumeration; the system searches the catalogue of dissections to find all those that match the graph properties given by the user. By means of a non-linear program the dissection is adapted to specific dimensions. The application of this system would seem to be constrained to the level of complexity of a house. The computation necessary to dimension a configuration greater that three cells in depth becomes unreasonable due to the amount of computation time. The advantages of this enumeration are similar to the enumeration of polyominos; however, the design system by Mitchell[9] shows the usefulness of the theoretic development.

Classification

Classification methods were first generated by biologists who needed to separate different animals or cells into classes or families or species. The work in biology developed by Sokal and Sneath[10] has been applied in a design system by Mitchell[11]. The same functional operation of classification can be found in electrical engineering. By the operation of cutset analysis a set of component groups in a system can be found. This work has been applied to design by Tabor[12]; the classification is represented in the form of a dendrogram which illustrates how the system is broken down into its components. Work in the social sciences on factor analysis methods by Horst[13] and Harman[14] can also be considered as a classification method. This work has been applied to design by the author[15].

In previous work, classification methods have been used as a partial solution to the allocation problem. Let us consider the allocation of 9 cells. If we classify the data matrix given to relate the 9 cells and find that three groups of 3 cells are formed, then only approximately 200 solutions exist for any one configuration. If on the other hand we had to allocate each cell to a location in any one configuration, then approximately 360,000 solutions would be

possible. By classifying the data we are reducing the selection to one in 200 from one in 360,000. For a complete reference to the methods associated with classification and the disciplines from which they come refer to Ball[16].

The development from heuristics to enumerations would seem to have been generated by a need on the part of the researchers to develop a theoretic framework for the subject. This would appear to have been achieved.

Although it is important to develop such a theory it also seems important to find the correct relationship between the environment of the problem and the methods involved. In early work on the subject it was assumed that there was significance in using travel cost as a criteria; however, it is obvious that this is not significant at the building scale. In house design it is possible to use the travel cost criteria indirectly to find the optimal layout to give privacy in the different sections of the house, the objective being to minimize the amount of internal partitions. Outside of these two specific problems, and those that are only economic in nature such as the factory, the space allocation problem is not one of optimization. The problem is to find the level of building organization that is appropriate to the use of the building.

The Environment Of The Problem

The type of problem to which this method can be applied is one where there is a large number of different activities. It is increasingly common to find that large organizations have a diversified network of administrative control and that it is difficult to find one person who can identify the needs for a new building. Universities and research facilities are typical of this type. The groups that can be identified in such situations may be classified as follows; a control group consisting of the personnel in administrative control ie. Presidents and Vice-Presidents in a research group or the Dean and Department Chairmen in a university group. The second group is composed of all the personnel who have a particular functional unit in the organization under their control. This could be the director of a lab or an individual who is conducting a specific project. The design analysis that is carried out is based on information collected from the individuals described in the second group and presented to the control group for verification. The process that developes between the designers, control group, and researchers is one that clarifies the needs of all three groups. The method to be described is the method that the designers would use to arrive at the spatial allocations for each itteration of the method.

The Method

The method of space allocation has three distinct phases. The first phase is to find by classification the component groups of the system. The component group in a research facility could be the group of individual research activities that cluster together because of common service requirements or because of the free exchange of ideas between researchers. The second phase of the method is the analysis of the component groups to find out if there are characteristics of the group that would help in the selection of a spatial organization. The selection of a spatial organization for each of the component groups is also part of this phase. The third phase is to find a spatial organization that will be used to organize the component groups into a total system. As Allen has described "the gatekeeper" in communication terms, we will use the same term to refer to those activities in a building that organizes the component groups and in themselves form a network with other gatekeepers to organize the complete system.

Phase 1

The first phase is to classify the elements, or activities, into their component groups. The information collected for the analysis can vary considerably, refer Frew[17]. In different building types different criteria will be important. In Allen the criteria has to do with where personnel found their ideas for research. The resultant classification identified the personnel type known as "the gatekeeper." From an operational standpoint, the matrix that is most useful in space allocation is the one where the matrix represents all of the criteria that can be used to determine a physical connection between two elements. or where it is advantageous to minimize the distance between two elements. The information is represented in the form of a matrix D where the elements of the matrix represent the connection or lack of connection of the elements of the system.

For any two rows in the matrix a distinction must be made between $D_{ij} = D_{ji}$ (direct relation)

and $D_{ij} \neq D_{ji}$ (associative relation). Any resultant classification must keep the direct relation $\geqslant$ the associative relation as the direct relationship is a given condition. Consequently, the comparison of rows will produce an intercorrelation matrix I which, when combined with the distance matrix D, will produce a matrix R which will have the characteristic as follows.

It will have the elements in the same rank order as D and have the further discrimination of the inter-correlation matrix I. The values of the elements of the R matrix indicates the strength of connection between the members represented in the element. To find the component groups, firstly order the elements in R from strongest to weakest, then sort each element of the matrix from the strongest down into different groups, each time checking to make sure that neither member of the element is present in a previous group. If either member is present, then that element becomes part of that group. The process continues until all members of the system have been accounted and the exact composition and number of component groups established.

Phase 2

From existing algorythms this phase would be to find the pattern that is the best fit to the data matrix that was originally generated. One weakness of these algorythms is that they use data that is either in distance terms or in terms of required boundaries; consequently, the process used generates patterns that are normally free form and with numerous cells that are completely enclosed by other cells. The determination of the closed packed pattern or the open pattern is a function of the scale used in the original data matrix. Similar problems occur in cellular assembly and rectangular dissection programs. At the level of 10 cells the foregoing programs are adequate. At the level of 100 cells they are not. The 100 cell case is typically a hospital or research facility. In these cases the phase, after finding the component groups, is to find the organization of paths that will be used to connect the cells or activities ie. corridors.

Let us look for a moment at the number of possible organizations of paths that exist. At a fundamental level it is the author's contention that there are not more than five types that can be assembled in combination with other types to create the building form. The types are:

1) Centralized Activity. Where one activity

such as a waiting room is isolated as the activity to organize all other activities in the component group. The qualities that
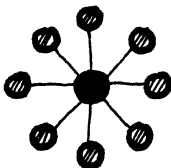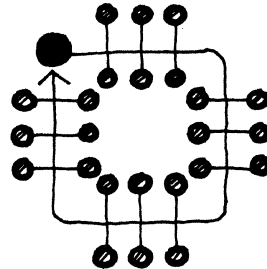
are apparent in this type are:

minimum distance between cells,
minimum privacy,
greater potential for an informal environment.

2) The Street. Where an additional element is added such as a corridor or, if expanded in scale, an activity can be a street or meeting place. If the street is only entered from one side, then one is able to design an environment that is controlled and secure.
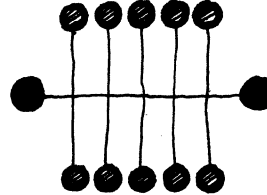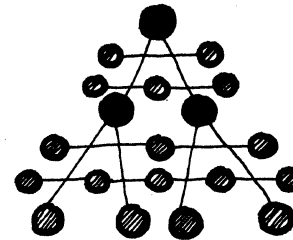

3) The Circuit or Loop. This type is sometimes known as a court-yard form due to the negative space created by the circuit form of the layout. It is more common in low rise buildings, although it is found as the top or top two stories of large bulk buildings such as Place Bonaventure in Montreal. This form gives the designer the ability to create a secure environment and gives maximum distance between cells.

4) The Tree. The tree is a hierarchial organization of cells where the user is guided to his destination by a sequence of decision points or branches. This form gives the opportunity to clearly identify the levels of authority in an organization if they exist. It is a system where the user must be given information at each branch. Control and security can be designed as required and each cell will have a different level of privacy depending on the location of the cell in the system.

5) The Cell as a Path. Each cell can be considered as having a path as part of its function. A house is often considered as this especially among the daytime activities. The qualities that one can obtain from such an organization are to minimize any set of distance requirements and also to minimize the degree of privacy that is possible in each cell.
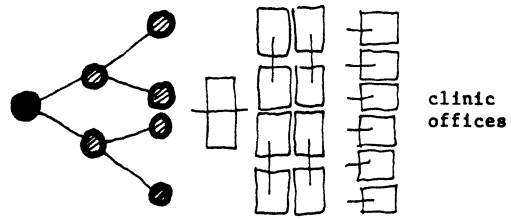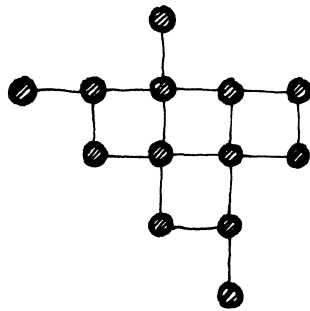
Organization Diagram for Multi-Cellular Structure

clinic
offices
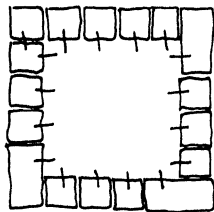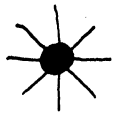
public building
research lab
gallery
school

Organization
Diagram.

Typical
Plan
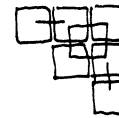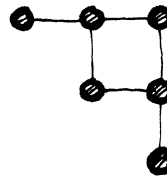
the house
research labs

Program Sequence

EXAMPLE OF
CELLULAR
ORGANIZATION
TO THE
GRAPHS

1) Select organizational type
2) Determine number of cells
3) Distribution of cell areas
4) Dimensional constraints
5) Allocate names to cells
6) Evaluate
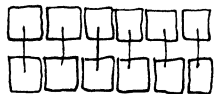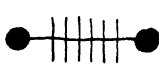
offices
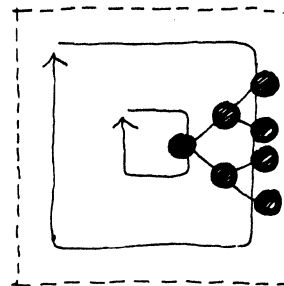
Medical Clinic

Three organizations
are interlinked.
a) circuit for
patients, b) circuit
for medical staff,
c) tree for patient
to consult medical
staff.
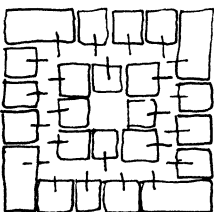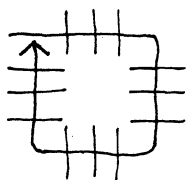
offices
research labs
shops
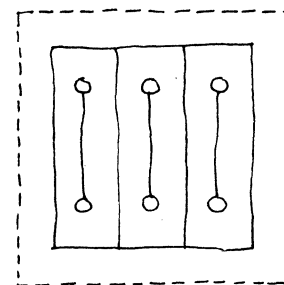
Shopping Mall

Three interlocking
circuits that form
the public circula-
tion with three
streets to service
the stores connect-
ing vertically to
vehicular traffic.

19
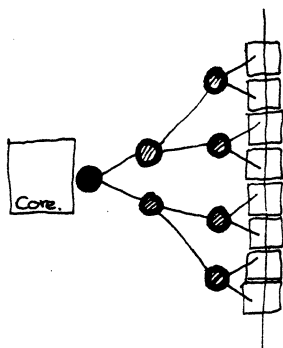
Offices

Simple tree structure to provide pedestrian access with the private offices organized as a circuit on the outside face of the building.

COMBINATION OF FUNDAMENTAL

ORGANIZATIONAL FORMS

Although the subject has been limited to the organization of activities to facilitate human usage, it is also possible to apply the organizational forms to the sub-systems of a building. In applying them to the sub-systems the objective would be to identify the design problems that would arise from the overlap or intersection of the sub-systems.

To select one of the five organizational forms for the component group is not an obvious process. It would seem that the most rational way to do this would be to analyze the original matrix and determine the best fit between pattern and matrix and thereby select the best. On consultation with graph theorists, it would seem that there is not at present a method for making such a selection. Since there can be only five space allocations for each component group, it is suggested that all five be produced or that the obviously unfeasible solutions be dropped and only those that meet the higher level qualities described against each type be continued. For example, a component group that requires maximum privacy for each cell would not consider a centralized activity type as feasible. The selection procedure is one of excluding the unfeasible types and carrying all others to the next phase.

Phase 3

The organization of the component groups can be determined by analysis of the qualities of the individual groups. From the original data matrix one can determine a ratio between the number of elements that define the internal cohesion of the group and the number of elements that define the connections of the members of the group to the other members of the system. In a recent study of the requirements for an expansion to a research facility it was found that the chemical group had a very high ratio. Almost 100 percent of the connections were internal, whereas the design group had a very low ratio indicating a need for central location and easy access to other groups. In this particular example the existing facility determined the allocation at this level. If this had not been the case, then the ratio could be used as a simple gravity measure. In addition, the summation of the values of the connections between the groups can be used to locate the groups relative to each other.

On closer analysis of the component groups, one may find that there are one or two cells that have greater connection to the whole system than to the particular group. Such cells are known as "gatekeepers" and can be used to represent the group in arriving at the space layout for the whole system. The method of finding the layout at this level is the same as previously described ie. by carrying out a space lay-

out for each of the organizational types. As can be seen in the clinic example there is a need for exploration of overlaping types which puts a demand on the computer system for greater user input which can be provided through interactive graphics with large computation and storage ability.

Conclusion

As Eastman[18] has described in data base design for building design problems, there are three levels of information that must be stored. They are:
  a) topological information of the elements
  b) dimensions
  c) location in the particular instance
In this paper it is also recommended that the computerized process of considering the arrangement of rooms in a building be as follows:
  a) identify the component groups
  b) select topological organization types for groups
  c) locate groups and identify system organization.
  d) give dimension to the elements
    In conclusion, it would appear that too much attention has been given to establishing theoretical framework to look at the space allocation problem which has now developed to the point where application in computer aided design is unlikely, although contributions have been made to the original graph theoretic issues raised by Read, Tutte, and Harary. It is the environment of the problem, ie. the nature of the design process and existing buildings, that create the criteria for generation of computer aided design systems. The system described in this paper is in a preliminary stage; computer programs are not complete but will be developed in the next year.

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Second International Conference on Computers in
Engineering and Building Design

ABSTRACTS OF PAPERS

ON BUILDING DESIGN

DATABASES FOR PHYSICAL SYSTEM DESIGN: A SURVEY OF U.S. EFFORTS

CHARLES M. EASTMAN
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A perspective is introduced regarding database systems for physical system design, with special emphasis on building systems. This perspective focuses on the relation of data to analysis programs, whether the data incorporates redundancy, methods of describing shape information, and alternative implementation strategies for design database systems. This perspective is super-imposed on three design database efforts now ongoing in the United States: CADANCE at General Motors: COMRADE at the Naval Ship Research and Development Center and BDS at the Institute of Physical Planning, Carnegie-Mellon University.

COMPUTER-AIDED HANDLING OF BRIEFING AND DESIGN INFORMATION FOR BUILDING PROJECTS

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1-4 Yarmouth Place, Piccadilly, London W1Y 8JQ.

The architectural design process involves the collection, storage, retrieval, analysis and presentation of information about a building project.

Manual data handling can be tedious, error prone, time-consuming and expensive on a project of any appreciable size or complexity.

Automated data handling, utilizing computer-based techniques, can sometimes offer an alternative method of working with the potential for greater accuracy, saving of time, cost savings and greater job satisfaction.

This paper examines some of the factors that need to be taken into account in adopting a computer-aided approach to the handling of briefing and design information for building projects; it presents an outline of such a computer-based system currently in use together with examples of its cost, advantages and disadvantages.

THE USE OF 3D INTERACTIVE GRAPHICS TO AID THE DESIGN AND LAYOUT OF EQUIPMENT

C. JOHNSON, P. PURCELL and P. SAMPSON
Department of Design Research, Royal College of
Art, Kensington Gore, London SW7 2EU, U.K.

The paper addresses the potential for using 3D graphics as an aid to equipment design and layout. Several inter-related issues are examined, namely:

The problem of controlling the graphic image and of manipulating the internal computer model of the design.

The relative merits of wire-line diagrams (with or without hidden line removal) and tonal pictures are discussed.

The use of computer modelling aids to assist the designer in the layout of equipment in various work environments.

The value of perspectives from arbitrary viewpoints as opposed to conventional two-dimensional plans and perspectives.

THE INTER-RELATIONSHIP OF DESIGN AND PERFORMANCE VARIABLES

ALAN H. BRIDGES
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Glasgow, U.K., G4 0NG.

This paper discusses the use of computer-aided building appraisal programs, showing how they can help the designer by providing facilities to search the solution space for feasible designs, and giving information on the multivariate and temporal aspects of design. The use of the programs to establish the relationsnips between those variables which the designer may manipulate and the characteristics measured by the computer program are described, indicating how the information obtained may provide general design rules and also be incorporated in future programs as a further design aid.

DYNAMIC PROGRAMMING IN THE CAD OF BUILDINGS

JOHN S. GERO
Department of Architectural Science, University
of Sydney, Sydney, NSW, 2006, Australia.

Dynamic programming is an especially useful optimization technique when nonlinearities and increments are found in conjunction with combinatorics as often occur in various problems in the CAD of buildings. This paper presents the formulation as dynamic programs of three different problems: site development economic feasibility studies, normalization in building design, and sky lobby and lift zoning in tall buildings. The emphasis is on a standard formulation for this class of problem. The paper concludes with comments on potential applications of dynamic programming to building design and mentions some extensions being developed including forward feed systems, non-serial representations and fuzzy set evaluators.

CEDAR3: BASIC SOFTWARE FOR COMPUTER-AIDED DESIGN

D. CHARLESWORTH and G. WEBSTER
Property Service Agency, Directorate of Building
Developments, Cedar Project, Room 1610, Lunar
House, 40 Wellesley Road, Croydon CR9 2EL, England.

A justification of the concept of basic software is given in the context of the history of CEDAR. The current applications area is described. A simple but logical description of basic software is developed in stages, each stage being functionally dependent on the previous stage. At each stage design decisions are argued. Finally, possible lines of future development are considered.

NEW DEVELOPMENTS IN THE OXSYS SYSTEM

PAUL RICHENS
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Cambridge, England.

The OXSYS system for computer-aided building design contained a number of software techniques capable of wider use. When it was reimplemented on a minicomputer, it was decided to develop it, as separate levels applicable to multi-function interactive data orientated systems in general, to buildings in general, and to a particular type of building. The lowest level, forming a nucleus of great generality contains three sections. The Programming System provides an overlay generator, control routines and diagnostic facilities. The User Interface provides batch and interactive I/O, device independence, and graphics. The Data Management System handles the security, access and structuring of large random-access databases.

COMPUTER AIDS FOR A DEPARTMENT OF ARCHITECTURE IN LOCAL GOVERNMENT

ROBIN TH'NG
Department of Architectural and Related Services,
Strathclyde Regional Council, Scotland.

This paper is concerned primarily with computer aids for architectural design. It records the areas in which the computer can play a role in design offices in Local Government. It is, however, too early to predict the success of such techniques for real design problems.

A GRAPHICS SYSTEM FOR BUILDING DESIGN IN THE CANADIAN GOVERNMENT

J. KIRK ROBERTSON
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Development Branch, Department of Public Works,
Sir Charles Tupper Building, Riverside Drive,
Ottawa, Ontario K1A 0M2, Canada.

The Department of Public Works of the Government of Canada has embarked on a five-year programme to develop computer-aided design tools for its building design and maintenance operations. The paper describes the principle features of the thoroughly integrated design graphics system developed, outlining the hardware, language and programs which have been selected and developed to meet the requirements of the programme.

EXPERIENCE OF THE USE OF COMPUTER PROGRAMS IN THE DESIGN OF THE HEATING, WATER SUPPLY AND AIR CONDITIONING OF A PUBLIC OFFICE BUILDING

MATTI HÄKKILÄ
Insinooritoimisto Olof Granlund Antii Oksanen,
skol, Engineering Consultants, Liisankatu 19 A 5,
00170 Helsinki 17, Finland.

The subject of discussion is the largest public office building in Finland, the Pasila Administration Centre. The design and construction of the building is supervised by the National Board of Building.

Computer programs were used to analyze the effects of various factors on the indoor climate of the building. The heating and cooling requirements of the building were calculated as well as the heating, water supply and cooling water systems.

The experience has been of a purely positive nature. Both the designers and the supervisor have been kept up-to-date with respect to the consequences arising from the various design possibilities.

LUMPS - LAND USE MASTER PLAN SUBSTITUTE

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** Computer Applications Group, Technical
  Policy Division, Department of Architecture
  and Civic Design, Greater London Council,
  Room 462 North Block, County Hall, London SE1.*

*** Thamesmead Master Plan Group, Special Works
  Branch, Department of Architecture and Civic
  Design, Greater London Council, Room 372
  North Block, County Hall, London SE1, England.*

The LUMPS system is a set of computer aids to
various processes within the physical planning
activity. It is impossible to gain insight into
the nature and applicability of LUMPS without
first understanding its general relationship to
the planning process, and Section 1 of the paper
attempts to clarify this. It also defines its
relationship with the Thamesmead Development and
the objectives which were thought important to the
evolution of the system.

Section 2 describes the basic structure of LUMPS
as it is apparent to the user, describing each
of its component subsystems and their uses in turn.

Section 3 outlines the processes involved in the
implementation of the system and some of the
problems encountered.

USER ASPECTS OF SAR 70, AN INTERACTIVE SYSTEM FOR THE GENERATION OF ALTERNATIVE DWELLING LAYOUTS

*J.H.A.E. AMKREUTZ and P.J.M. DINJENS
Department of Architecture Building and Planning,
University of Technology, Postbus 513, Eindhoven,
Netherlands.*

In this paper some of the problems in using the
SAR 70 system as it is now, are discussed. It is
shown, that these practical aspects touch deeper
and more general problems in CAD; From this
some guidelines are suggested, that the authors
used to solve these problems in the design of an
improved version of the SAR 70 system now under
development.

DATA-STRUCTURES FOR FUNCTION AND GEOMETRICAL DESCRIPTION OF BUILDINGS

*K. AGGER
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8000 Aarhus C, Denmark.*

To meet the demand for a single total and
general computer system for problem solving and
communication in planning and production of
buildings, the object of this project is the
creation of a data-structure for the functional
and geometrical description of buildings.

In implementation of the data-structure, the
greatest importance is attached to the geometrical
data. Therefore, those algorithms implemented so
far only allow the user to model a three-
dimensional description of a building, on-line on
a graphical data-screen and look at the creation
in various scales, projection modes and on any
projection-plane.

13th DESIGN AUTOMATION CONFERENCE REVIEW

David Hightower
Texas Instruments, Inc.

Unlucky 13 turned out to be lucky 13 for the 13th Design Automation Conference at the Jack Tar Hotel in San Francisco, June 28-30. By any measure the conference was a success.

The 375 registered participants were treated to three full days packed with 17 technical sessions in which 71 papers from 9 countries were presented.

There were three tutorials this year: Interconnection, Interactive Graphics and Applied Data Base Techniques, and Program Verification. Although the hour-long talks are called tutorials they really present current state-of-the-art techniques. The attendance was excellent with more than 200 people showing up at the 8:00 am talks.

Technical sessions began at 1:30 on Monday. The DA "standards" were well received with usually more than 130 people attending. These included interactive graphics, interconnection, placement and routing, design rule verification, and IC layout.

The interconnection session chaired by Roland Mattison of GTE, played to a full house. The conference committee and the hotel staff had to move chairs into the lecture hall during the talk to accommodate the overflow crowd in excess of 200.

Jim Allen of Bell Labs presented a modification of Lee's algorithm. Schmidt of Bell Labs and Wu of Vanderbilt presented a router which first assigns paths from a fixed set of path types, then assigns the path segments to tracks using an interesting assignment algorithm. During the question-answer session following the talks, participants expressed concern about choosing algorithms for minicmoputers and for large batch applications.

More than 100 people attended the IC Layout session chaired by Rob Smith of Lawrence Livermore Lab. The session focused on the features of working systems. Four papers discussed the placement and routing algorithms incorporated in the Bell Lab's LTX system. The system exploits interactive operator inputs to improve performance of automated layout processes. An unusual symbolic layout problem modeling approach was described by Steve Nance of American Microsystems. In the last paper, Bill Van Cleemput discussed some interesting implications of a topological approach to IC layout.

The session on Design Rule Verification chaired by Herb Wall of GTE was also well attended with approximately 175 persons. There were four papers that dealt with the following problems in IC mask preparation: tolerance checking, design rule verification, element recognition, and circuit analysis done by examining the mask. The authors were Lindsay, Preas, and Gwyn of Sandia Labs; Dobes and Byrd of Macrodata, and Ikemoto, et al, of Hitachi. Dave Hightower attacked the tolerance checking problems of printed wiring boards.

The interactive graphics session, chaired by R. Williams of IBM, described three working interaction DA systems. As always, the questions were these: refresh vs. storage scopes, and minicomputers vs. the power of a TSO system. Horbst, Prechtl, and Will of Siemens presented a paper on a system which emphasizes the importance of the man-machine dialogue, and the importance of hardware independence. Marks of Martin Marietta Corp. presented a paper describing a total DA system implemented on TSO which reduces design time by 50% over a partially automated DA system. The partially automated system, which has been in use for the past 6 years, was described by Lerman.

The session on routing and placement, chaired by Steve Pardee of Bell Labs, contained six papers: Hanan, Wolff, and Agule of IBM presented a paper on the results of applying six different iterative improvement algorithms and a constructive initial placement algorithm to six problems. A new force-directed pairwise relaxation algorithm came out the winner. Ramakrishna Rau of Stanford described a more integrated approach to the interconnection problem. He criticized the need for the disjoint steps of: wire list determination, layering, ordering, and routing. He suggested an approach which does many of these things on the fly with the goal of equal distribution of wire density. Lesk and Goldstein of Bell Labs described a technique for discrete optimization which makes use of "blocks" appearing in many suboptimal solutions. Blocks are identified and then optimal solutions to the block arrangement problem may be found. The result is a near optimal solution. Kamikawai, Kishida, Osawa, Yasuda, and Chiba of Hitachi described a DA system called "Master-Slice" employing automatic routing and placement. Wilson and Smith of Lawrence Livermore Lab presented several models and a technique for evaluating automatic router capabilities. Patterson and Phillips of GE of England described a complete CAD system for PWB design which has been implemented on a minicomputer.

Other mainline DA sessions were: digital logic simulations, testing and testers, fault tolerant DA, and data bases, chaired (respectively) by: Losleben of NSA, Corriea of IBM, Hassler of TI, and Williams of Bell Labs. Space does not permit abstracting the papers in these sessions, but there was considerable interest in all four sessions. The session on data bases contained a paper not listed in the program. It was presented by Carl Shinn of Bell Labs, who described the data base behind BLUE, an interactive editor for modifying and auditing circuit masks.

The sessions on structural, mechanical, and architectural DA were well attended, and there will be an effort next year to strengthen those areas, particularly architectural DA. Jean-Marie Comeau of Carleton University was the architectural DA session chairman, and Chuck Radke of IBM chaired the session on Structural and Mechanical DA.

There were three sessions on software engineering and reliability chaired by D. Nelson, an independent contractor, and R. T. Yeh of the University of Texas. These sessions dealt with software design and development methodology. Their place in the DA conference was based on the importance of software in design automation rather than on the extent to which the design and development of software has itself been automated.

Other sessions were Computer Aided Doumentation chaired by Bob Hitchcock of IBM, and Mature DA Systems reviewed by Dan Schweikert of Bell Labs.

The Design Automation Conference has always been for hard workers. The average attendee starts with a tutorial at 8:00 am, followed by talks from 9:00 until 12:00 and 1:30 until 5:30. A cocktail hour from 5:30-6:30 permits the attendee to mingle and talk DA with people from other companies (and countries). At 6:30 there are common interest meetings where groups of people with a common problem, interconnection for example, can get together and talk about their pet problems and solutions.

If you liked us in San Francisco, you'll love us in New Orleans for DAC '77.

SYSTEMS • SOFTWARE • HARDWARE • PRACTICAL RESULTS • RESEARCH

1977 International Symposium on Fault-Tolerant Computing FTCS-7

University Hilton Hotel (Adjacent to the USC campus)
LOS ANGELES, CALIFORNIA   JUNE 28-30, 1977

CALL FOR PAPERS

This is the seventh annual international symposium sponsored by the Technical Committee on Fault-Tolerant Computing of the IEEE Computer Society.

Papers are solicited on any subject dealing with the general topic of fault-tolerant computing. A list of the topics considered relevant to the theme of this symposium is given below.

- *Fault-Tolerant System Architecture*
- *Operating Systems for Fault-Tolerant Systems*
- *Fault Diagnosis, Reconfiguration, and Recovery*
- *Fault-Tolerant Software Systems*
- *Error Control in Computers and Computer Networks*
- *Measures of Availability, Reliability, and Fault Tolerance*
- *System Testing and Diagnosis*
- *Applications of Error Coding Techniques*
- *Modeling of Fault-Tolerant Systems*
- *Verification of Hardware/Firmware/Software Design*
- *Analysis of Test Generation Methods*

Four copies of a complete paper of digest length (4000 words maximum) should be sent so as to be received by the Program Chairman no later than December 1, 1976. Each paper should include an abstract of no more than one page.

Authors will be notified of the disposition of their papers by March 1, 1977.

GENERAL CHAIRMAN
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Los Angeles, CA 90007

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University of Southern California
Los Angeles, CA 90007

WORKSHOP ON DESIGN AUTOMATION AND
MICROPROCESSORS

Call for Participation

The IEEE Technical Committee on Design Automation and the ACM Special Interest Group on Design Automation plan to organize a workshop on Design Aids for the Design of Microprocessors and Microprocessor-based Systems.

This 2 or 3-day workshop is tentatively scheduled for February 1977 on the West Coast. The intention is to hold the workshop as close as possible to the COMPCON 77 Spring Meeting.

The workshop will have a formal part with refereed contributions and invited talks. These will be published in the proceedings of the Workshop. There will be a number of informal sessions. In order to stimulate open discussion these will **not** be part of the proceedings and no taperecorders or cameras will be allowed during these sessions.

Since this is intended to be a workshop (or a working conference) the number of attendance will be strictly limited. If you intend to participate by submitting a paper, by talking at an informal session or just by attending, please indicate by notifying W. M. Van Cleemput, Digital Systems Laboratory, Stanford University, Stanford, California 94305.
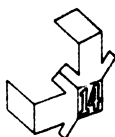
SOME IMPORTANT DEADLINES: Refereed papers due:
October 1, 1976; Notice of acceptance sent:
November 15, 1976; Final manuscripts due:
December 31, 1976; Participation in informal
sessions: December 15, 1976.

14TH DESIGN AUTOMATION CONFERENCE

REQUIREMENTS FOR SUBMITTING PAPERS

If you plan to submit a paper, you should send three copies of the paper (rough drafts are acceptable) to the program chairman no later than December, 1976. Please include a title for the paper plus an abstract (less than 25 words)

Accompanying the draft should be the full name, affiliation address, and telephone number of the principal author, with whom all further direct communication will be conducted.

Notification of acceptance will be sent to you during the first week of March 1976. After notification of acceptance, you will receive detailed instructions on the format to be observed in typing the final copy. To insure the availability of Proceedings at the Workshop, your final manuscript will be due April 20, 1977.

Final papers should be no longer than 5000 words, and the presentation should be limited to 20 minutes. Projection equipment for 35mm slides and viewgraph (overhead projector) foils will be available for every talk. Please indicate what, if any, additional audio-visual aids you require.

Rough drafts are to be sent to the Program Chairman:

Program Chairman   David W. Hightower
Texas Instruments, Inc.
P.O. Box 5012 MS907
Dallas, Texas 75222 -
214-238-3492

General Chairman   Judy G. Brinsfield
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Sponsors

The sponsors of the Design Automation Workshop are the ACM (Association for Computing Machinery) Special Interest Group on Design Automation and IEEE (Institute of Electrical and Electronics Engineers) Computer Society Design Automation Technical Committee.

Design Automation

Design Automation implies the use of computers as aids to the design process.

In the broadest sense, the design process includes everything from specifying the characteristics of a product to meet a marketing objective to enumerating the details of how it is to be manufactured and tested.

Thus design automation embraces applications from one end of the design process to the other.

Site of the 14th DAC   International Hotel
300 Canal Street
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June 20, 21, 22, 1977

TOPICS OF INTEREST

TECHNIQUES
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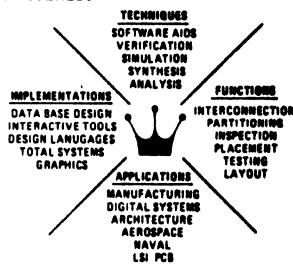
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2909 CORONADO
SANTA CLARA, CALIFORNIA   95051

BRAUNE, D
BELL LABS
WARRENVILLE-NAPERVILLE ROAD
NAPERVILLE, ILL   60540

BREVER, M
UNIVERSITY OF SO. CALIFORNIA
POWELL HALL 412
LOS ANGELES, CALIFORNIA   90007

BRUCE, E
DIGITAL EQUIPMENT
146 MAIN ST
MAYNARD, MASS   01754

BREWER, H E
CALCOMP
2411 W LA PALMA AVE
ANAHEIM, CALIFORNIA   92801

BRINSFIELD, J G
BELL LABS
WHIPPANY ROAD
WHIPPANY, N J   07981

BUCKLES, M L
MAGNAVOX
4624 EXECUTIVE BLVD
FORT WAYNE, IND   46808

BURKLEY, R
IBM
1930 CENT PK W
LOS ANGELES, CALIFORNIA   90067

BURCH, W F
COMSAT LABORATORIES
P O BOX 115 CLARKSBURG, MD   20734

BURD, W
SANDIA LAB
ORG 9624
ALBUQUERQUE, N M   87115

BURGIN, L
COMPUTER VISION
19 COACH ROAD
BILIERICA, MASS   01821

BURTON, M
MCDONNELL AIRCRAFT
LAMBERT FIELD BOX 516
ST LOUIS, MO   63166

BYRD, R
6728 RANDIWOOD LANE
WEST HILLS, CALIFORNIA   91307

CAGE, W
LAWRENCE LIVERMORE LABS
BOX 808 L-156
LIVERMORE, CALIFORNIA   94550

CAIRNS, J
TRW SYSTEMS
4205 W 230TH PL
TORRANCE, CALIFORNIA   90505

CANCILLA, E
AMER MICRO SYS
3800 HOMESTEAD ROAD
SANTA CLARA, CALIFORNIA   95051

CARNEY, A
AIR FORCE AVIONICS LABS
AFAL MICRO ELECTRONICS BRANCH
WRIGHT-PATTERSON AFB
DAYTON, OHIO   45433

CARROLL, B D
AUBURN UNIVERSITY
AUBURN, ALA   36830

CASE, G
SANDIA CORP
ALBUQUERQUE, N M   87115

CAVAGNA, C
POLITECHNICO DI MILANO
MILANO, ITALY

CHAPPELL, S G
BELL LABS
WARRENVILLE-NAPERVILLE ROAD
NAPERVILLE, ILL   60540

CHAWLA, B R
BELL LABS
600 MOUNTAIN AVE
MURRAY HILL, N J   07974

CHURCH, J
ADAGE INC
2555 E CHAPMAN AVE
FULLERTON, CALIFORNIA   92631

CIAMPI, P
RAYTHEON
HARTWELL ROAD S2-68
BEDFORD, MASS   01730

CLAIRORNE, J
INTEL CORP
3065 BOWERS AVE
SANTA CLARA, CALIFORNIA   95051

CLARY, D
AMERICAN MICRO SYSTEMS
3800 HOMESTEAD ROAD
SANTA CLARA, CALIFORNIA   95051

COFFINBERRY, R
BURROUGHS CORP
BOX 235
DOWNINGTOWN, PA   19335

COMEAU, J
GOMT OF CANADA, DSS, BMC
365 LAURIER WEST
OTTAWA, ONTARIO, CANADA   KINGY1

CONGER, R
BURROUGHS CORP
P O BOX 517
PAOLI, PA   19301

CONWAY, L
XEROX CORP
PALO ALTO RESEARCH CTR
PALO ALTO, CALIFORNIA   94306

COOK, M R
GTE AUTO ELE LABS
400 N WOLFF ROAD
NORTHLAKE, ILL   60164

COOLO, L H
MICROTECHNOLOGY
22069 WALLACE DRIVE
CUPERTINA, CALIFORNIA   95014

COOLEY, H E
IBM
1000 WESTCHESTER AVE
WHITE PALINS, N Y   10604

CORREIA, M
IBM
E FISHKILL RT 52
HOPEWELL JUNCTION
NEW YORK, N Y   12533

CRAWFORD, B J
AMER MICRO SYSTEMS
3800 HOMESTEAD RD
SANTA CLARA, CALIFORNIA   95051

CROWLEY, J
TEXAS INSTRUMENTS
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DALLAS, TEXAS   75222

CRAFT, L C
SIGNETICS
811 E ARQUES
SUNNYVALE, CALIFORNIA   94086

CURD, W H, JR
HONEYWELL
BCX 26159
PHOENIX, ARIZONA   85068

CYTRYN, A
SLS-ENVIRONETICS
600 MADISON AVE
NEW YORK, N Y   10022

DAAE, H
TANDBERGS RADIOFABRIKK
OSLO, NORWAY

DANKERS, K
TRW
ONE SPACE PARK R6-1380
REDONDO BEACH, CALIFORNIA   90278

DARAM, S B
ROCKWELL INTERNATIONAL
201 E CHAPMAN #72B
PLACENTIA, CALIFORNIA   92670

DAVIES, A D
VIRGINIA COMM UNIV
1015 FLOYD AVE
RICHMOND, VIRGINIA   23226

DAY, F W
BELL LABORATORIES
600 MOUNTAIN AVE
MURRAY HILL, N J   07974

DEARDORFF, L H
GTE AUTO ELEC LABS
400 N WOLFF RD
NORTHLAKE, ILL   60164

DEUTSCH, D N
BELL LABS
600 MOUNTAIN AVE
MURRAY HILL, N J   07974

DIAZ, R A
LAAS OHM CNRS
FOW OHN COLONEL ROCHE
37400 BULOUSE, FRANCE

DIEGLER, A
BELL LABS
6200 EAST BROAD ST
COLUMBUS, OHIO   43213

DIERK, KARSTEN
SINGER
150 TOTOWA RD
WAYNE, N J   07424

DONELSON, W C
MIT
77 MASS AVE
CAMBRIDGE, MASS   02139

DONOVON, A
RAYTHEON
HARTWELL ROAD
BEDFORD, MASS   01730

DROBISH, W
SILICON SYSTEMS, INC
2913 DAIMLER ST
SANTA ANA, CALIFORNIA   92705

DRUMMOND, E
SJSV
22038 HUTCHINSON ROAD
LOS GATOS, LA   95030

DYE, J
EURTEK, INC
7041 E 15
TULSA, OKLAHOMA   74112

EISENBERG, B
NCR
CAMBRIDGE, OHIO   45409

EMMOTT, J T
BELL LABS
555 UNION BLVD
ALLENTOWN, PA   18103

ENCARNACAO, J
TECHNISCHE HOCHSCHULE
STEUBENPLATZ 12
6100 DARMSTADT
W GERMANY

EVANS, R
BURROUGHS CORP
25725 JERONIMO
MISSION VIEJO, CALIF   92675

EVERITT, F
GTE AUTO ELEC LABS
400 N WOLFF ROAD
NORTHLAKE, ILL   60164

FAIRBAIRN, D
XEROX
3333 COYOTE HILL ROAD
PALO ALTO, CALIF   94304

FALVEY, J P
COMSAT
COMSAT DRIVE
CLARKSBURG, MD   20734

FARAH, J J, JR
GENRAD INC
BAKER AVE
CONCORD, MASS   01773

FELSENSTEIN, M A
HEWLETT PACKARD
5301 STEVENS CREEK BLVD
SANTA CLARA, CALIF   95050

FELLER, A
RCA CORP
CAMDEN, N J   08102

FELTON, P
RAYTHEON CO
BOX 360
PORTSMOUTH, R I   02871

FINKELMAN, L F
SINGER COMPANY
833 SONORA AVE
GLENDALE, CALIF   92101

FISHER, R S
GTE LABS
40 SYLVAN ROAD
WALTHAM, MASS   02154

FLETCHER, R F
BELL LABS
6200 E BROAD ST
COLUMBUS, OHIO   43213

FLOMENHOFT, M
INTEL
3065 BOWERS AVE
SANTA CLARA, CALIF   95051

FORD, F C
BURROUGHS CORP
PAOLI, PA   19301

FOURNIER, S
YALE UNIVERSITY
SCHOOL OF ARCHITECTURE
NEW HAVEN, CONN   06520

FRIBERG, T
ERICSSON
STOCKHOLM, SWEDEN

FRIEDMAN, A
UNIV OF SO CALIF
4566 POE AVE
WOODLAWD HILLS, CALIF   91364

FRYKLUND, J
MILNE HALL
OREGON STATE UNIVERSITY
CORVALLIS, OREGON   97331

FUKUSHIMA, H
MIRCOTECHNOLOGY CORPORATION
224 NORTH WOLFE ROAD
SUNNYVALE, CALIF   94086

GEE, L
HEWLETT PACKARD CO
5301 STEVENS CREEK BLVD
SANTA CLARA, CALIF   95050

GIBSON, D
AMER MICRO SYSTEMS
3800 HOMESTEAD ROAD
SANTA CLARA, CALIF   95051

GIBSON, W M
IBM
NEIGHBORHOOD ROAD
KINGSTRON, N Y   12401

GIELICZ, K P
TRW SYSTEMS
ONE SPACE PARK R6/1176
REDWOOD BEACH, CALIF   90278

GINGERICH, J
TEKTRONIX INC
P O BOX 500
BEAVERTON, OREGON   97005

GOLDSTEIN, A J
BELL LABS
6 CORPORATE PLACE
PISCATAWAY, N J   08854

GORMAN, J L
SPERRY UNIVAC
ROSEVILLE, MINNESOTA   55112

GOSTA, L
ELLEMTEL UTVERKLINKS
FACK
S 125 20 ALUSSO
SWEDEN

GOTO, S
UNIV OF CALIF
2109 CEDAR #A
BERKELEY, CALIF   94709

GOUNDAN, A
UNIV OF SOUTH CAL
UNIVERSITY PARK
LOS ANGELES, CALIF   90007

GRANT, P
DANIEL, MAWN, JOHNSON
3250 WILSHIRE BLVD
LOS ANGELES, CALIF   90010

GRIFFIN, B
AMER MICRO SYS
3800 HOMESTEAD RD
SANTA CLARA, CALIF   95008

GRINTHAL, E T
BELL LABS
600 MOUNTAIN AVE
MURRAY HILL, N J   07974

GRUSS, R P
DEPT OF DEFENSE
91 AB CALIF TERR
GAMBRILLS, MD   21054

GULLEDGE, B
NORTH ELECTRIC CO
553 SOUTH MARKET
GALION, OHIO   44833

GUMMELL, H K
BELL LABS
600 MOUNTAIN AVE
MURRAY HILL, N J   07974

GWYN, C
SANDIA LABS
DIV 2142
ALBUQUERQUE, N M   87115

HAGERMAN, R J
BELL LABS
11900 N PECOS ST
DENVER, COLORADO   80234

HANAN, M
IBM CORP
T J WATSON RES CENT
YORKTOWN HEIGHTS, N Y   10598

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HUGHES
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FULLERTON, CALIF   92634

HASS, B
RAYTHEON - MJD
HARTWELL ROAD
BEDFORD, MASS   01730

HASSLER, E
TEXAS INSTRUMENTS
P O BOX 5012 MS 907
DALLAS, TEXAS   75222

HATTON, D P
IBM
6300 DIAGONAL HIGH
BOULDER, COLORADO   80301

HAYES, J P
UNIV SOUTHERN CAL
DEPT OF EE
LOS ANGELES, CALIF   90007

HELLER, B
RAYTHEON CO
528 BOSTON POST RD
SUDBURY, MASS   01776

HEMBROUGH, F
RAYTHEON CO
HARTWELL ROAD
BEDFORD, MASS   01730

HENINGER, A
AMER MICRO SYSTEMS
3800 HOMESTEAD RD
SANTA CLARA, CALIF   95051

HERCOG, D
UNIV OF LJUBLJANA
YUGOSLAVIA

HEROT, C
MIT
RM 9-512
CAMBRIDGE, MASS   02139

HERRICK, W
GTE
77 "A" ST
NEEDHAM, MASS   02194

HIGHTOWER, D W
TEXAS INSTRUMENTS INC
P O BOX 5012 MS907
DALLAS, TEXAS   75222

HILIANI
ICL
WENLOCK WAY - WEST GORDON
MANCHESTER, ENGLAND

HITCHOCK, R B
IBM CORP
BOX 6
ENDICOTT, N Y   13760

HO, P K
GIBBS & HILL INC
393 SEVENTH AVE
NEW YORI, N Y   10001

HOLOMAN, S B
BELL LABS
CRAWFORDS CORNER ROAD
HOLMDEL, N J   07733

HOFFMAN, S
GTE SYLVANIA
BOX 188
MOUNTAIN VIEW, CALIF   94042

HOLSINGER, JR, C E
VIRGINIA COMMONWEALTH UNIV
1501 FLOYD AVE
RICHMOND, VIRGINIA   23220

HORBST, E, JR
SIEMENS AG
FL SYST 252 D8000
MUNICH, HOFMASTER
W GERMANY

HSIEH, E P DR
IBM
E FISHKILL - RT 52
HOPEWELL JUNCTION, N Y   12533

HUBBARD, R
SPERRY UNIVAC
P O BOX 500
BLUE BELL, PA   19422

HUDSON, C
AMER MICRO SYS
3800 HOMESTEAD RD
SANTA CLARA, CALIF   95051

HULSOOR, S
GTE SYLVANIA
NEEDHAM, MASS   02194

HUM, R
BELL NORTHERN
P O BOX 3511 STA 'C'
OTTAWA, ONTARIO, CANADA K1Y4H7

HUMCKE, D
BELL LABS
CRAWFORDS CORNER ROAD
HOLMDEL, N J   07733

IKEMOTO, Y
HITACHI LTD
TOKYO, JAPAN

IOSUPOVICZ, A
CALIF STATE UNIV
18111 NORDHOFF ST
NORTHRIDGE, CALIF   91324

IVEY, R
MC CONNELL DOUGLAS
700 ROYAL OAKS DR
MONROVIA, CALIF   91016

JAKIELA, A
BELL LABS
WARRENVILLE-NAPERVILLE ROAD
NAPERVILLE, ILL   60540

JARVELA, R
IBM
12 MALONEY DR
WAPPINGERS FALLS, N Y   12590

JENNINGS, D
AMER MICRO SYS
3800 HOMESTEAD RD
SANTA CLARA, CALIF   95051

JODOIN, N
BELL NORTHERN RESEARCH
CRYSTAL BEACH
OTTAWA, CANADA, ONTARIO

JOHNSON, D W
MC DONNELL DOUGLAS
700 ROYAL OAKS DR
MONROVIA, CALIF   91016

JOHNSON, J A
LOS ALAMOS SCIEN LAB
BOX 1663
LOS ALAMOS, N M   87545

JCHNSON, S E
OREGON STATE UNIVERSITY
3415 S W CHINTINNINI AVE
CORVALLIS, OREGON   97330

JCHNSON, W
TEXAS INSTRUMENTS
BOX 5012 MS 907
DALLAS, TEXAS   75222

JONES, E
FAIRCHILD MOS
BOX 303
LOS ALTOS, CALIF   94022

JONES, G W
IPC SCIENCE & TECHNOLOGY PRESS
IPC HOUSE, 32 HIGH ST
GUILDFORD, SURREY, ENGLAND GU1 3EW

KALLA, G
UNIVAC
UNIVAC PARK
ST PAUL, MINN   55165

KADAKIA, V
XERCX CORP
702 S AVIATION BLVD
EL SEGUNDO, CALIF   90245

KAMIKAWAI, R
HITACHI LTD
1-280 HIGASHI KORGAKUSO
KOKUBUNJJ, TOKYO, JAPAN

KANE, J
IBM
600 HARVARD ST
VESTAL, N Y   13850

KATO, S
NEC SYSTEMS
C/O HONEYWELL
PHOENIX, ARIZ   85005

KATZ, W M
SCIENTIFIC CALCUL INC
110 ALLENS CREEK RD
ROCHESTER, N Y   14618

KAUFMAN, R E, DR
MIT
1-112 MECH ENG DEPT
CAMBRIDGE, MASS   02139

KELLER, D S
UNIV OF CALIF
817 CALIF ST #4
SANTA CRUZ, CALIF   95060

KELLY, M
LAWRENCE LIVERMORE LABS
LIVERMORE, CALIF   94550

KENNEDY, E M
GENERAL ELECTRIC
BOX 237
DETROIT, MICHIGAN   48221

KENNICOTT, P
GENERAL ELEC CO
BOX 8
SCHENECTADY, N Y   12301

KERR, R W
GTE AUTO ELEC
400 N WOLFF ROAD
NORTHLAKE, ILL   601614

KESLER, J R
GENERAL ELECTRIC
283 HARTS DRIVE
NEW HARTFORD, N Y   13413

KING, G E
VARIAN DATA MACHINES
2722 MICHELSON DR
IRVINE, CALIF   92713

KLEMCZAK, R
IBM
D153K BLD 906
EAST FISHKILL, N Y   12601

KLOMP, J G M
PHILIPS
OUDE MOLLE MUTSEWEG 105
NYMEGEN, NETHERLANDS

KLOTZ, C
WESTERN ELECTRIC CO
SUITE 113 502 EARTH CITY
EARTH CITY, MO   63045

KORENJAK, A
RCA
RT 1
PRINCETON, N J   08540

KOSMAN, R A
BELL LABS
WARRENVILLE-NAPERVILLE RD
NAPERVILLE, ILL   60540

KOVIJANIC
SPERRY UNIVAC
621 SILVER LAKE RD
NEW BRIGHTON, MINN   55112

KOZAK, P
BELL LABS
600 MOUNTAIN AVE
MURRAY HILL, N J   07974

KRULEE, R L
GTE SYLVANIA
P O BOX 188
MT VIEW, CALIF   94042

KUH, E S
UNIV OF CALIF
COLLEGE OF ENGINEERING
BERKELEY, CALIF   94720

KUSILE, B
DIGITAL EQUIP CORP
146 MAIN ST
MAYNARD, MASS   01754

KUWAHARA, Y
HITACHI, LTD
2672 BAYSHORE FRONTAGE RD
MT VIEW, CALIF   94043

LANGLET, T
BURROUGHS CORP
25725 JERONIMO
MISSION VIEJO, CALIF   92675

LARSON, J F
IBM - POUGHKEEPSIE
BLDG 951
POUGHKEEPSIE, N Y   12602

LARVELA, J N
OSU COMPUTER CENTER
OREGON ST UNIVERSITY
CORWALLIS, OREGON   97331

LA SHOMB, J
SPERRY UNIVAC
2276 HIGHCREST DRIVE
ROSEVILLE, MINN   55113

LATUS, P
IBM
P O BOX 600
HOPEWELL JCT, N Y   12533

LEIF, C
ELLEMTEL UTVECKLINGS
FACK
S-125 20 ALUSJO
SWEDEN

LERMAN, H N
MARTIN-MARIETTA CORP
P O BOX 5837 MP 198
ORLANDO, FLA   32805

LEVIN, S
UNIV OF CALIF
DEPT OF COMP SCIENCE
IRVINE, CALIF   92717

LEWIS, T M
SINGER CORP
833 SONORA AVE
GLENDALE, CALIF   91201

LEYKING, L
BURROUGHS CORP
25725 JERONIMO
MISSION VIEJO, CALIF   92675

LIEBERT, T A
BELL LABS
CRAWFORD CORNERS ROAD
HOLMDEL, N J   07733

LINDERS, J
UNIVERSITY OF WATERLOO
WATERLOO, ONT   NZL 3G1

LINDSAY, B
SANDIA LABS
DIV 2142
ALEUQUERQUE, N M   87115

LOCK, K
BURROUGHS
16701 W BERNARDO
SAN DIEGO, CALIF   92127

LOSLEBEN, P
NSA
R154
FT MEADE, MD   20755

LUCAS, W J
SPERRY FLIGHT SYSTEMS
21111 N 19TH AVE
PHOENIX, ARIZONA   85027

LUCY, T
AUTOMATED SYSTEMS
999 N SEPULVEDA
EL SEGUNDO, CALIF   90245

LUND, J
HONEYWELL
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PHOENIX, ARIZ   85005

MC ARDLE, M
NCR
16550 W BERNARDO DR
SAN DIEGO, CALIF   92127

MC CORMICK, D
DEPT OF DEFENSE
9800 SAVAGE RD
FT MEADE, MD   20755

MC CREIGHT, E
XEROX
3333 COYOTE HILL RD
PALO ALTO, CALIF   94304

MC CULLOUGH, B B, JR
TEXAS INSTRUMENTS
13500 N CENTRAL EXPRESSWAY
DALLAS, TEXAS   75222

MC FARLAND, B
TRW SYSTEMS
ONE SPACE PARK
REDONDO BEACH, CALIF   90278

MAGNUSON, W
LAWRENCE LIVERMORE LABS
LIVERMORE, CALIF   94550

MARKS, L
MARTIN MARIETTA
ORIANDO, FLA   32805

MARLETT, R D
WESTINGHOUSE
BALTIMORE, MD   20203

MARTELLOTTO, N A
BELL LABS
WARRENVILLE-NAPERVILLE ROAD
NAPERVILLE, ILL   60540

MARTINEZ, P
NAT SAVINGS / LOAN OF VENE
APARTADO 6760 CARMEL 101
CARACAS, VENEZUELA

MATTHEWS, A
ADAGE INC
1079 COMMONWEALTH
BOSTON, MAINE   02215

MATTISON, R
GTE LABS
WALTHAM, MASS   02154

MAY, G
TEXAS INSTRUMENTS
DALLAS, TEXAS   75062

MAYFIELD, J P
TELEDYNE RYAN AERO
2701 HARBOR DR
SAN DIEGO, CALIF   92127

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IBM
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POUGHKEEPSIE, N Y   12602

MENCN, P R
BELL LABS
WARRENVILLE-NAPERVILLE ROAD
NAPERVILLE, ILL   60540

MEYER, G
BELL LABS
CRAWFORD CORNER ROAD
HOLMDEL, N J   07733

MICHAELS, P A
BENDIX RESEARCH
27734 LYNDON
LIVONIA, MICH   48154

MILICI, A K
SPERRY FLIGHT SYSTEMS
21111 NORTH 19TH AVE
PHOENIX, ARIZONA   85027

MILLER, D
INTEL CORP
3065 BOWERS AVE
SANTA CLARA, CALIF   95051

MISRA, J
UNIV OF TEXAS
DERY OF COMP SCIENCES
AUSTIN, TEXAS   78712

MISSEN, R
IBM
P O BOX 600
HOPEWELL JUNCT, N Y   12533

MOREL, A
THOMSON-CSF
3 AVENUE CENTRALE
92700 COLOMBES, FRANCE

MORZENTI, O J
BELL LABS
600 MOUNTAIN AVE
MURRAY HILL, N J   07974

MURPHY, B
NAVAL AVIONICS FACILITY
6000 E 21ST
INDIANAPOLIS, INDIANA   46218

NANCE, S
AMERICAN MICROSYSTEMS
3800 HOMESTEAD RD
SANTA CLARA, CALIF   95051

NASH, J D
RAYTHEON
HARTWELL RD 32-68
BEDFORD, MASS   01730

NELSON, D
INDEPENDENT CONTRACTOR
3401 MARKET ST - RM 250
PHILADELPHIA, PA   19104

NELSON, W B
LOS ALAMOS SCIENTIFIC LAB
BOX 1663 GROUP C-6
LOS ALAMOS, N M   87545

NICHOLSON, J O
INTERNATIONAL HARVESTER CO
7 S 600 COUNTY LINE RD
HINSDALE, ILL   60521

NIN, A
IVIC-LAB COMPUTACION
APARTADO 1827 CARMELITAB 101
CARACAS, VENEZUELA

NOPPEN, RUDI
GESELLSCHAFT FUR KERN
PCSTFACH 3640
7500 KARLSRUBE
GERMANY

ODHNER, V
BURROUGHS
CSG/T SWEDESFORD RD
PAOLI, PA   19301

OLILA, J S
SIGNETICS
811 E ARQUES
SUNNYVALE, CALIF   94086

CRNSTEIN, S M
XEROX PARC
COYOTE HILL RD
PALO ALTO, CALIF   94304

OSUNA, J
INTEL CORP
3065 BOWERS AVE
SANTA CLARA, CALIF   95051

OZGA, R
GTE AUTO ELEC LABS
400 N WOLFF RD
NORTHLAKE, ILL   60164

PADDOCK, S
GTE SYLVANIA
BCX 188
MOUNTAINVIEW, CALIF   94042

PARASCH, G J
IEM CORP
1701 NORTH ST
ENDICOTT, N Y   13760

PARDEE, S
BELL LABS
WHIPPANY RD
WHIPPANY, N J   07981

PARIS, J
IBM
BODLE HILL RD
OSWEGO, N Y   13827

PATTERSON, G L
GEC TELECOMMUNICATIONS
P C BOX 53 TELE WORKS
COVENTRY, ENGLAND CV31HJ

PODERSON, D
HEWLETT PACKARD
PALO ALTO, CALIF   94304

PEGRAM, D W, JR
BELL LABS
11900 N PECOS ST
DENVER, COLO   80234

PELLEGRIN, J
BELL LABS
WARRENVILLE-NAPERVILLE ROAD
NAPERVILLE, ILL   60540

PERSKY, G
BELL LABS
600 MOUNTAIN AVE
MURRAY HILL, N J   07974

PETERSON, D L
LEAR SIEGLER, INC
4141 EASTERN AVE S E
GRAND RAPIDS, MICH   49508

PETERSON, D P
SANDIA LABS
ALBUQUERQUE, N M   87115

PFISTER, G F
IBM BLDG 985
ROUTE 55
POUGHKEEPSIE, N Y   12601

PIERCE, A R
VIRGINIA POLY INS
BACKSBURG, VA   24061

PISCATELLI, R N
SANDERS ASSOC
DANIEL WEBSTER HWY
SOUTH NASHUA, N H   03060

PISTILLI, P O
BELL LABS
11900 N PECOS ST
DENVER, COLORADO   80234

POCHA, MICHAEL
LAWRENCE LIVERMORE LABS
LIVERMORE, CALIF   94550

POND, E W
BELL LABS
WARRENVILLE-NAPERVILLE ROAD
NAPERVILLE, ILL   60540

PREAS, B
SANDIA LABS
DIV 2142
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AUTOMATIC PC BOARD ROUTING CLEANUP PROCEDURES*

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ABSTRACT

Automatic routing programs produce layouts which contain features that could be improved. This paper describes straightforward techniques for layout improvement that are routing algorithm independent.

INTRODUCTION

Automatic routing programs frequently attempt to produce interconnections consistent with algorithmic implementations, but which lack certain attributes readily observable by human evaluators. Specific router behavioral patterns are highly dependent on interaction of a particular router with a particular layout problem, but certain classes of "less than optimal" behavior can be observed over a wide variety of such combinations.

We suggest in this paper that some of the most common types of undesirable wiring paths can be improved by a router-independent automatic cleanup procedure, and show how cleanup might be accomplished. The utilization of cleanup processing as board layout progresses will also be explored, and results obtained through use of a local implementation will be presented.

For discussion purposes, we define cleanup as revision of a PC board layout which preserves realized interconnections while improving the esthetic appearance, fabrication characteristics, or realization of as yet unrouted connections. In many environments, cleanup is performed manually or with the assistance of computer-aided interactive graphics systems. However, under certain circumstances it becomes desirable to completely automate the process. Indeed, certain types of cleanup or layout revision are often incorporated directly into the programs which perform PC board layout.

We have noticed, however, that some of the most relevant cleanup requirements (see below) are necessary regardless of the routing algorithm used. Thus, to build cleanup facilities into each router program might lead to redundant effort when multiple algorithms are to be employed. Furthermore, the circumstances under which cleanup is preformed for a single router may greatly influence the strategies to be followed: cleanup procedures invoked after routing 50%, 70% and 90% of all point-to-point connections might be different from each other, and wouldn't be the same as the procedure used after all possible connections have been made.

The cleanup procedure is therefore required to operate independent of any particular routing algorithm, with behavior drastically modifiable under control of several parameters supplied at each invocation. The software which realizes our cleanup process also provides for later extension of the subsystem to include other types of cleanup strategies. The PCB cleanup subsystem is intended to eliminate obviously undesirable choices made in local areas of the board, with relative undesirability of significant features expressed as control parameter values. Cleanup behavior may be drastically modified by changing combinations of these parameters.

The definitions which follow explain terms frequently used in the remainder of this paper:

segment - a straight piece of wire or conducting foil.

fromto - a pair of points on a PC board between which a wired connection is to be made.

node - a fixed point on a board to which a wired connection is to be made (usually a device or connector pin).

junction point - point of intersection (end-to-end) of three or more wire segments.

crossover junction point - point where the center-lines of two or more wires segments cross.

proximity junction point - a junction point created by the extension of one or more existing wire segments.

via - a conducting path through the board from one layer to the next.

chain - a continuous string of wire segments which is terminated on both ends by nodes and/or junction points.

signal set - a collection of nodes and wire segments that are (or should be) connected together.

preferred direction - It is often useful to restrict wire orientation to a single direction on a given board layer. This direction is the preferred direction for that layer.

TYPICAL CLEANUP SITUATIONS

Routers that consider a single point-to-point connection at a time may produce situations similar to that shown in Figure 1a. Two connections have been made for a signal set, and the wires cross (on the same or different layers). For a wide range of objective functions, such layouts can be improved.

Another frequently encountered situation is illustrated in Figure 1b. A path meanders unnecessarily, with the more direct route perhaps being preferable. In 1c, a pair of feed-thru vias can be eliminated by moving a wire segment to another board layer. In 1d, two paths may be combined to yield a more economical interconnection. In 1e, an area of the board is unnecessarily fragmented, resulting perhaps in less than optimal utilization of potential path areas.

These examples, while oversimplified, represent similar situations encountered in the layouts produced by a number of routing algorithms. The following material describes an economical procedure for improving such layouts.

THE CLEANUP ENVIRONMENT

The environment in which our cleanup procedure functions is shown in Figure 2. The cleanup monitor routine supervises all cleanup activity. It determines the order in which processes are invoked, what options are selected, and controls communication between the cleanup section and the remainder of the PCB layout system. The monitor is organized to accommodate the addition of new cleanup processor sections and revisions to existing processors. The general approach is to define one data area containing all pertinent PCB layout information. Each cleanup processor communicates with this data area. Functionally the cleanup monitor operates as a controller, invoking subsidary "working" routines in a meaningful sequence. (Although the monitor supports many cleanup processes, this paper will focus on techniques related to junction point cleanup.) The board model initializer is the first section to be invoked when beginning the cleanup process. It retrieves necessary information about the board and the routed paths, converting this data into the form used for route cleanup. This process in effect builds a model of the board, which is used by the various processors in route cleanup.

In order to monitor cleanup operation for testing and analysis purposes, a data output module is provided to format several reports listing board data as stored in the cleanup data area. It was also found useful to add a capability to produce relatively crude checkprint pictures. (The board illustrations which accompany this paper were produced using the checkprint routines.)

When cleanup operations are finished the revised board layout description must be communicated to the remainder of the system. A module which converts the cleanup board model data back to the layout representation is invoked just prior to completion of board cleanup.

The remainder of the modules called by the cleanup monitor are drivers for specific types of

cleanup operations. To provide maximum flexibility, these communicate via the cleanup data area, function independently from each other, and need not be invoked in any particular sequence.

The cleanup processors have a similar organization to that of the cleanup monitor. Each contains a local data area, a data retriever (which builds the functional data model for that particular section), a data report generation section, a data update section and the functional modules which perform a step of the algorithm for each particular cleanup process. In most cases, a function-specific is as the basis for local data. This allows each processor to work with a data structure which is best suited for the operations being performed by that particular process, thus not forcing each individual processor to conform to a potentially inappropriate standard. This relaxes constraints on additional processors that may eventually b- added, keeping the system as modular as possible. There is also a module which updates the cleanup board model with revised layout information.

Each algorithm is partitioned into a series of relatively independent modules which are executed in sequential order. The communication within each cleanup processor is via the data common area for that particular processor. Each processor section also has access to the cleanup board data and may refer to it at any time. In general any module has access to any data area which is available to any of the modules found closer to the "root" of the hierarchical system tree structure.

CLEANUP MONITOR DATA STRUCTURES

The data structure used by the cleanup monitor provides a convenient and flexible means of describing the dimension, location, and type of each of the elements of area on the board. The dimension of each area (such as a signal path) is needed for checking for clearance when adding or changing signal paths. Four types of areas must be described:

1. Signal paths
2. Feedthrough vias
3. Unroutable areas (barriers)
4. Connection and test point pads.

The barriers, connections and test point pads are specified in the problem definition and are not changed by the cleanup section. The signal paths and feedthrough vias are the only areas that may be altered by the cleanup section.

Each such area is modeled as a rectangle, with the lower left and upper right corner coordinates of each rectangle stored with 15 bit integer precision in the board model data structure. For areas which are not rectangular (e.g. circular pads, etc.) the coordinates for the rectangle which encompasses the area are stored. Our current interpretation of coordinates gives a .001" resolution for cleanup processing. This method is flexible and can easily represent signal paths of different widths and irregularly shaped areas in a concise form.

Each element of area is assigned a location in a linked list. Each location descriptor specifies the lower left and upper right corner coordinates, the signal set which the rectangular entity belongs, and a pointer to the next link in that particular list. A separate list is used for each layer of the circuit board plus one for areas which occupy all layers of the board (e.g. feedthrough vias). This approach speeds testing for clearance during addition of new segments to a layout, since only a subset of the rectangular barriers must be examined. A header for each list has a pointer to the first and last links of each list and a count of the number of rectangles in the list.

The data structure used within the junction point cleanup processor section is quite different from that of the cleanup monitor. The data structure is a representation of only one signal set of the board; since each signal set is processed individually, only one net needs be represented at a time. The wire segments used to interconnect the signal set are described by the coordinates of the centerline endpoints for each straightline segment. A centerline representation is sufficient here since junction point cleanup deals only with interconnection paths instead of the total area each path actually uses. When checking for clearance during the addition of cleanup segments, actual path width is used to determine potential conflicts with the rest of the board model in the cleanup monitor. (The cen-

terline representation is stored in the junction point cleanup signal set data if clearance is confirmed).

Four basic types of signal path elements must be represented in this model. These are:

1. Wire segments
2. Feedthrough vias
3. Connection node points
4. Intersection points

Each signal path (wire segment) is described by its centerline end coordinates. The feedthrough vias are stored as a signal wire segment from one layer to another. Connection node points and intersection points are represented by a single set of coordinates stored in a point list.

A wire segment is any straight line portion of a connection path. (If a connection path were in the shape of an "L" between two points, it would require one wire segment for each leg of the "L".) A feedthrough via, being represented as a wire segment, is dealt with as a straight line portion of a connection path from one layer to the other.

The connection node points and intersection points are indistinguishable except for a type indicator. A node point is a location that must be electrically connected to the final network, whereas the intersection points need not be so connected. An intersection point is a location where three or more wire segments end. The connection requirement used in junction point cleanup thus becomes: find a minimal centerline length connection of all node points (which may or may not include paths connected to intersection points).

The actual connection between two points (intersection points or node points) is composed of a set of serially connected wire path segments. This set of serially connected segments is called a wire segment chain; a list is used to accumulate information describing each chain. One wire segment chain is used for each connection path between two points. Thus no (node or junction) points lie in the middle of a wire segment chain and any valid connection is composed of a combination of a subset of all defined wire segment chains.

This data structure is therefore composed of

three lists (see Figure 3): the segment list, the wire segment chain list, and the point list. The segment list stores with the end coordinates of each segment (x, y, and z), a pointer to the previous and next segments in the wire segment chain (chain end points if end of chain), the type of each segment end (point or bend) and a status indicator used by the algorithm. The point list contains the coordinates of each node or intersection point, the type of point, a status indicator, and a pointer to each wire segment chain which has this point as an end. The wire segment chain list contains a pointer to the first and last segment of the chain, the first and last points of the chain, the length of the chain, and a status indicator for use by the processing sections.

This organization of multiply linked lists allows convenient implementation of the cleanup algorithm and speeds access to desired data. As will be seen, this data structure also lends itself to other types of cleanup processing thus reducing the effort necessary to implement new cleanup processes.

THE JUNCTION POINT CLEANUP ALGORITHM

Given the descriptions of the nodes, barriers, and wire segments belonging to a particular signal set, the junction point cleanup routines establish a point list (consisting of nodes and junction points), and a segment list. The next operation is growing chains of wire segments: consider a series of wire segments beginning at a point in the point list and continuing segment by segment to another point in the point list. Any segment belonging to an unfinished chain (a series of segments which does not begin and end in the point list) is eliminated. After all chains have been grown, we are prepared to select those chains of shortest collective length that connect all of the nodes. The description of the PC board may then be altered to include only those wire segments which belong to the shortest net of chains. The process is then repeated for the next signal set. An overview block diagram of the basic junction point cleanup procedure is shown in Figure 4.

As an example, consider the layout shown in Figure 5. There are three nodes in the signal

set shown; they are connected in such a way that there is one redundant path between node 3 and the junction point. In this example, chain 1 connects node 1 to the junction, chain 2 connects node 2 to the junction, chain 3 is the shortest chain connecting node 3 to the junction, and chain 4 is the longest chain connecting node 3 to the junction. Having grown the chains, the collection (or net) of chains of shortest collective length is chosen. Thus, chain 4 is eliminated.

In the above example, we have implied a weighting of the wire segments that is proportional to their lengths. A more complicated weighting function significantly extends the capabilities of the algorithm. For instance, if we wish to penalize wire segments that cut across the preferred direction of the board layer, we could weight as follows:

> preferred direction - weight = 1* length
> across preferred direction - weight = N* length

where N is greater than one. With this weighting, path length would not be the sole criterion for choosing one chain over another: wire segment orientation would also influence the choice. Similarly, vias can be discouraged by assigning a large weight to them. A chain containing a via would then appear to be less desirable than a chain without a via.

If there is only one chain connecting a pair of points, the weighting scheme has no bearing on the selection. The effectiveness of the weights (and of the entire procedure) in eliminating layout problems depends upon the existence of alternate paths between points. As the following example will show, there is a definite advantage to adding carefully selected wire segments to establish alternate paths.

Consider the open loop of wire shown in Figure 6. The extension of one of the wire segments, from point A to point B, will result in a proximity junction point at B. The trial extension is termed a proximity junction point probe, and it is added by the cleanup routines to the signal set if wiring rules are not violated. Recall that chains of wire segments connect nodes and/or junction points. In this example, there are two chains connecting junction points A and B.

A weighting based on length is used to score these alternate paths and the loop is eliminated. The proximity junction point probes are added before the chains of wire segments are grown.

Similarly, pairs of vias may be eliminated by the addition of a wire segment between them. We have found that care must be taken when using this type of via elimination, since the layer 2 segment may fragment space when moved to layer 1. This secondary effect could be counterproductive to further efforts by a router. Therefore, this type of via elimination might be best done at the final cleanup stage.

PERFORMANCE AND CURRENT WORK

The junction point cleanup procedure described above is being used to improve the quality of layouts produced by several PCB interconnection routers in use at LLL. Several modes of utilization have been found worthwhile. In one application, a relatively unsophisticated line probe router was interrupted during the layout of a number of small, medium density boards. During each interruption, cleanup processing was applied in an attempt to improve the likelihood of completing unattempted and/or previously failed point-to-point connections. Figure 7 shows the layout improvement realized on one example board when the line probe router was interrupted (for the first time) after routing 50% of the connections. Table I shows the results of similar experiments involving a number of other boards.

We are now in the process of evaluating the performance of a layout system which combines junction point cleanup processing with several other routing algorithms. Figure 8 shows some of the processing sequences being investigated. Preliminary results of these experiments indicate that certain of the multiple algorithm approaches shown may be more powerful than any single algorithm with cleanup. It has also become obvious that the junction point algorithm does not deal with certain classes of easily corrected layout problems.

One of the most serious unresolved cleanup requirements concerns unnecessarily restricted access to nodes to which later connections must be made. Figure 9 shows an occurance of a representative situation. A path to edge connector

H blocks access to nearby connectors J and K. Since the blocking wire segment is parallel to the preferred direction, a relocation to the alternate site shown involves extension of an existing segment perpendicular to the preferred direction.

Recombination of unnecessarily fragmented open board area is another cleanup process not presently implemented. Junction point processing frequently contributes to open space recovery, but is not specifically oriented toward this objective. We feel that this capability could significantly improve router connection yield if used during the interrupted routing cleanups.

The additional cleanup processing suggested above represents a significant investment in software development for our small group. We have therefore decided to focus efforts on a manual layout revision facility which will allow evaluation of the merits of automating blockage removal and space recombination. It should be pointed out that the LLL PCB layout system is used primarily to design custom boards with extremely small production runs (1 to 6 units, typically), so that reduction of design labor and development schedule times are extremely important factors.

CONCLUSION

A router-independent PCB layout cleanup procedure has been described. The implementation discussed is extremely flexible and has been shown to improve the performance of routers with which it is used.

a. Redundant Paths.

b. Unnecessary Meandering.

c. Via Elimination

d. Combining Portions of Two Connections.

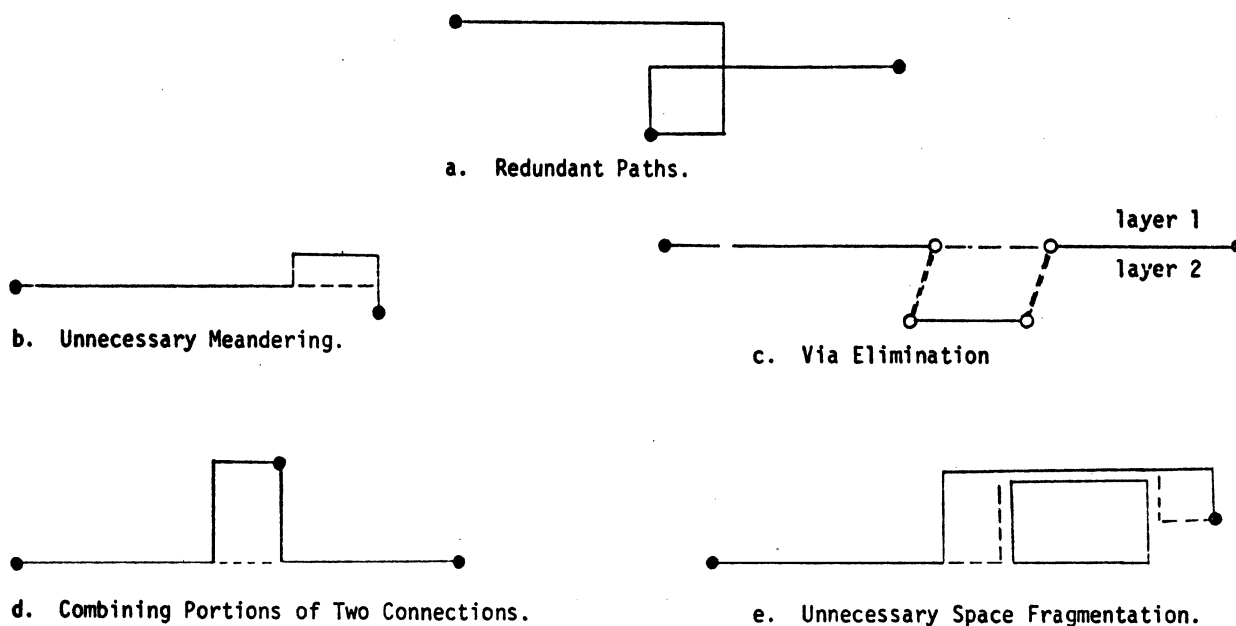e. Unnecessary Space Fragmentation.

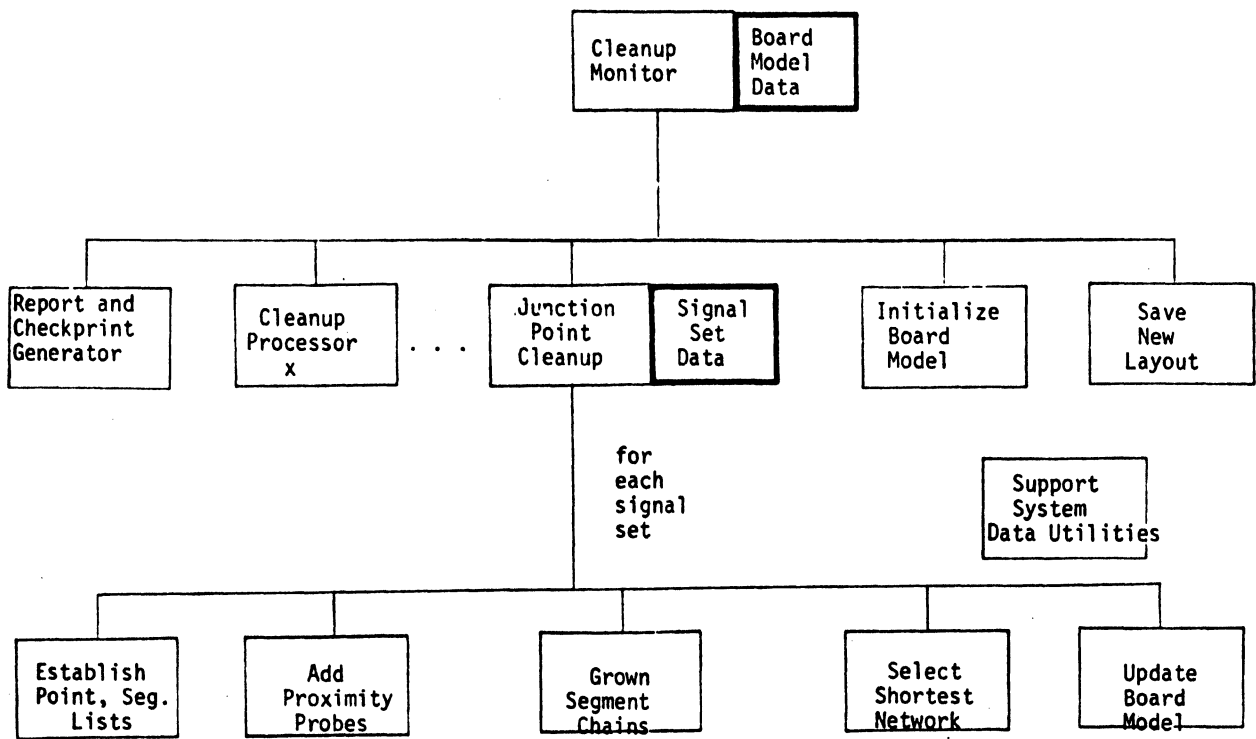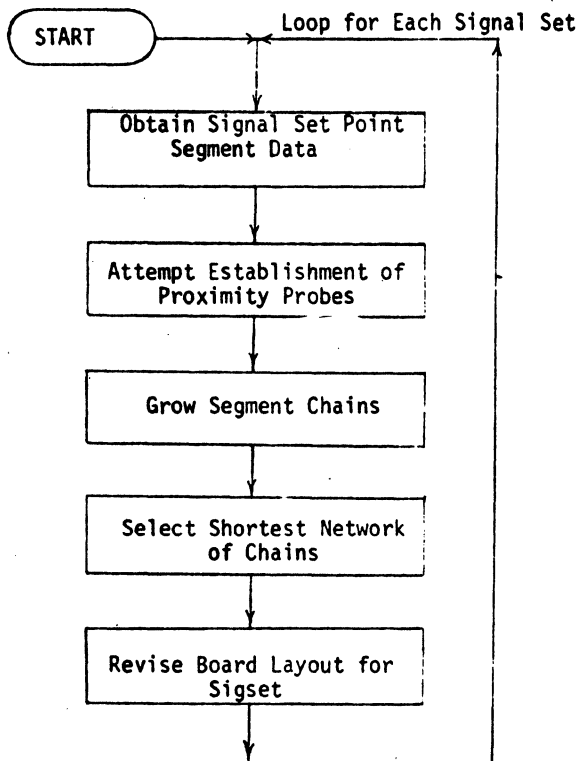Figure 1. Typical Cleanup Situations.
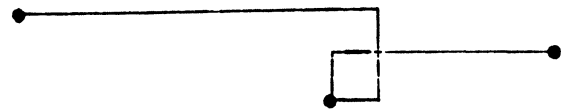
Figure 2. The Cleanup Subsystem.

Figure 4. The Junction Point
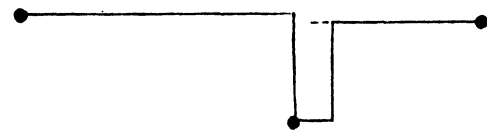Cleanup Process.

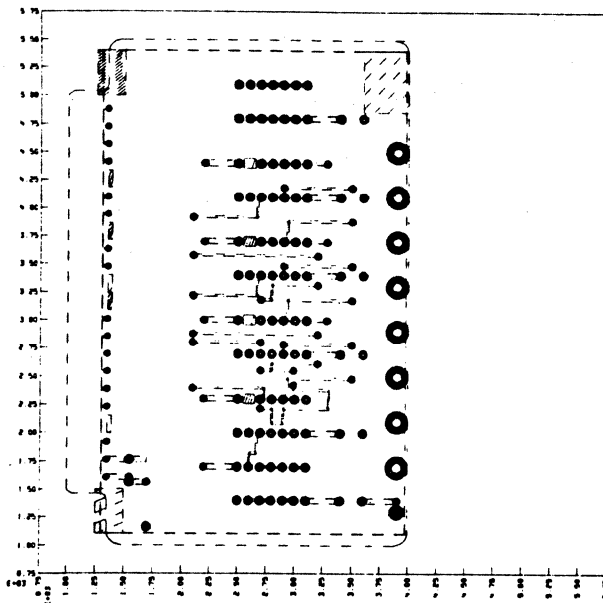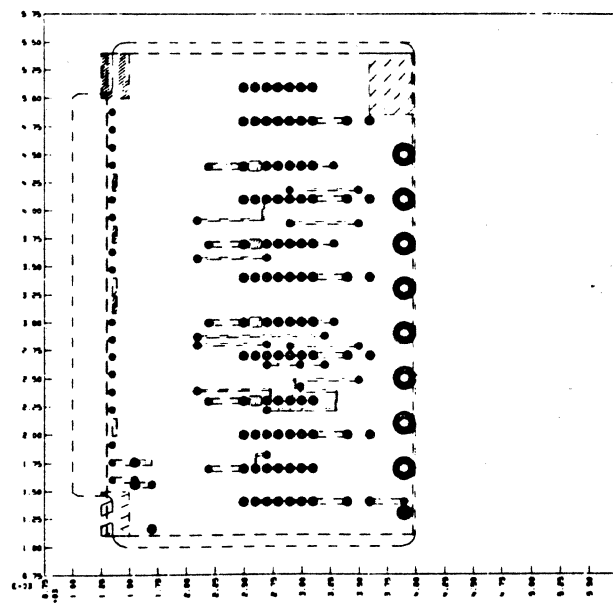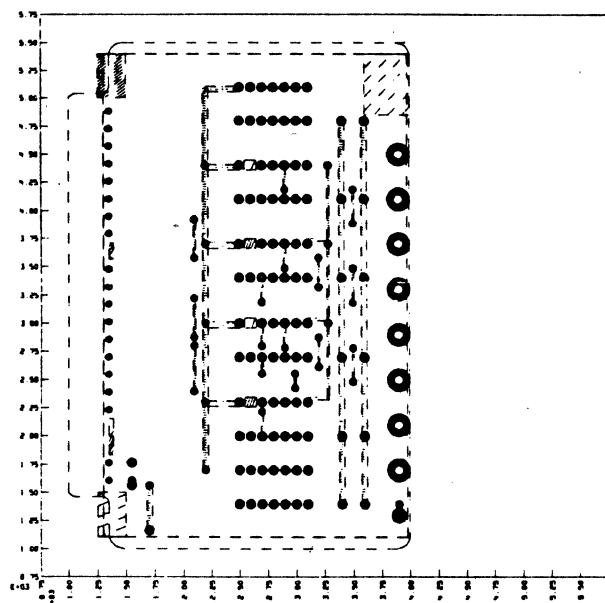Figure 5. A Junction Point
Cleanup Example.

Figure 6. Discovery of a Proximity
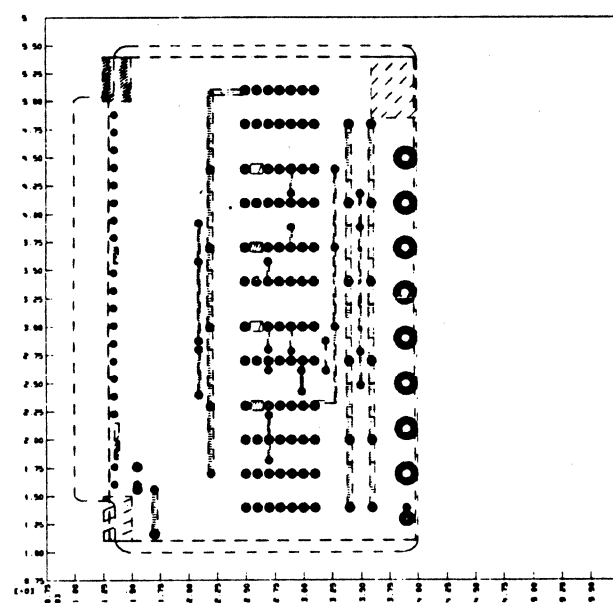Junction Point Pair.

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CLI BOARD LAYER 1.

CLI BOARD LAYER 1.

CLI BOARD LAYER 2.

CLI BOARD LAYER 2.

a. Before Cleanup

b. After Cleanup

Figure 7. A Cleanup Example.

[The last 2 illustrations from this paper appear on page 10 of this Newsletter. - ed.]

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