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SIGDA NEWSLETTER

SPECIAL INTEREST GROUP ON DESIGN AUTOMATION

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Contents:

SIGDA

ACM Special Interest Group on Design Automation

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SIG/SIC ACTIVITIES

1) Informal technical meetings at NCC.

2) Formal meeting during National ACM meeting + DA Workshop.

3) Joint sponsorship of annual Design Automation Workshop.

4) Quarterly newsletter.

5) Panel and/or technical sessions at other National meetings.

FIELD OF INTEREST OF SIGDA MEMBERS

Theoretic, analytic, and heuristic methods for:

1) performing design tasks,

2) assisting in design tasks,

3) optimizing designs through the use of computer techniques, algorithms and programs to:

1) facilitate communications between designers and design tasks,

2) provide design documentation,

3) evaluate design through simulation,

4) control manufacturing processes.

FROM THE EDITOR

I refuse to accept responsibility for the late arrival of the last issue. It left Livermore 12/4/76 and has not begun arriving through the mails as of 2/9/76. Undoubtedly the Christmas holidays were related to some of the delay but I agree with you--this is unreasonable!

Once more I would like to ask for contributions to this newsletter--I have had limited input for this issue, as you'll soon discover. How about some volunteers to write session summaries for the upcoming DA workshop? How about book and paper reviews? Deadlines for copy arrival at my address (front inside cover) for the next few issues are:

June (Vol. 6, #2)	5/1/76
Sept. (Vol. 6, #3)	7/15/76
Dec. (Vol. 6, #4)	10/1/76

I would like to thank Waldo Magnuson, now one of my co-workers at LLL, for permission to publish his recent report on European DA. Due to the length of the paper, we decided to divide it into two sections. The concluding portion will appear in the June Newsletter.

Several issues of the Proceedings for early DA Workshops are no longer available. I have received several inquiries concerning papers published in them, and wonder if any readers would like to see specific papers reprinted in this Newsletter? Call or write, if you have inputs.

I received one response to my Steiner tree challenge: Mr. Yuk Y. Yang of Burroughs found several problems with our solution. His suggestions were appreciated, and it's back to the drawing boards!

The notice reproduced below may be of interest to readers on other continents.

SIG/SIC NEWSLETTERS BEING AIRSHIPPED TO EUROPE FOR FASTER DISTRIBUTION OVERSEAS

Since July, those SIG/SIC Newsletters which are mailed from Headquarters have been airshipped via KLM to Amsterdam for delivery to all countries outside the North American continent. Because of the fast Dutch mail service leaving Amsterdam, we are able to achieve the following time savings with little increase in postal cost over standard U.S. surface printed matter rates:

	OLD WAY	NEW WAY
Europe	4- 8 weeks	1-2 weeks
No. Africa	6-10 weeks	2-3 weeks
Rest of World	8-12 weeks	3-4 weeks

See you at the 1976 Design Automation Conference in Palo Alto!

Rob

R. J. Smith

2/17/76

Dear Mr. Smith:

I read with much interest your article (co-author C.V. Cao) titled "Generation of Steiner Tree Connections in a Barrier-Free Environment" appearing in the current issue of ACM SIGDA Newsletter.

I was first introduced to the Steiner's problem back in 1970 while a graduate student at Columbia University. I have spent a fair amount of time on this problem but was not able to come up with a computationally feasible algorithm for its optimal solution. After I left Columbia, my interest on this problem is still strong, and I have tried to keep up with all published results on this topic.

While reading the article in the Newsletter, I tried, as you suggested, to improve the solution of the 26-point example. However, after carefully counting the tree lengths, it seems that the total length of the Steiner Tree as shown in Figure 3 is 199, instead of 192. Moreover, the Steiner Tree in Figure 3 can be improved quite easily to one with total length of only 196. I am enclosing a copy of the improved Steiner Tree for your reference.

To conclude this letter, I would be very grateful if you could send me a copy of LLL Report UCRL-76982, titled "Construction of Steiner Tree using the method of variable shortest connecting networks."

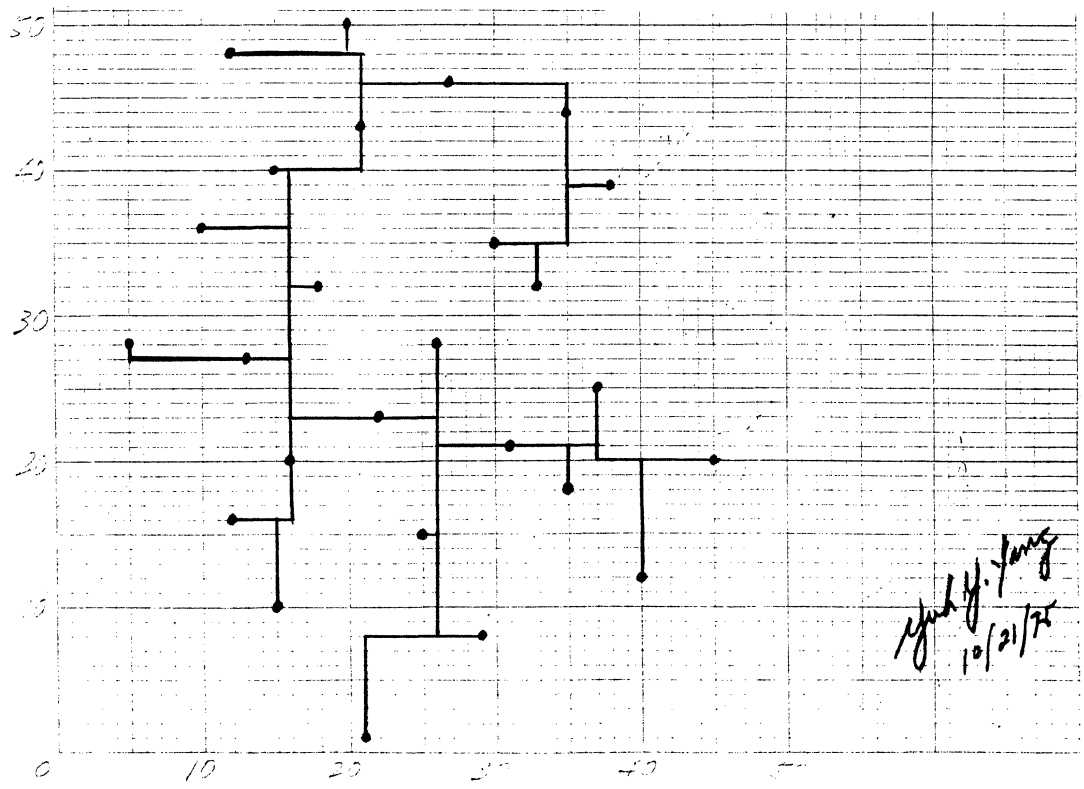
Thank you very much.

Yours sincerely,

Yuk Y. Yang
Project Engineer
Burroughs Corporation

YYY/ah

Enclosure



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COMPUTER AIDED DESIGN AND DESIGN AUTOMATION IN EUROPE

WALDO G. MAGNUSON, JR.

20 OCTOBER 1975

UNITED STATES OF AMERICA

I. INTRODUCTION

This report is a summary of computer aided design (CAD) and design automation (DA) stemming from a series of visits to universities, research laboratories, industrial companies and conferences during the past twelve months. In arranging these visits the primary contacts were with people engaged in applying digital computers as both an engineering aid and as a manufacturing tool in designing and building electronic systems and subassemblies. The visits were made throughout western Europe, with the United Kingdom, the Scandinavian countries, Germany and Italy receiving the greatest attention.

In Section II, I have given a rather superficial account of the development of CAD and DA, a brief description of the logic design process, and an indication of the trends in DA. The presentation is brief, because to do it properly would require hundreds of pages rather than just a few. Also, it is short because the principal purpose of this report is to describe the status of CAD and DA in Europe. Although the emphasis is on design automation of digital systems, I have included research in CAD (network analysis, network sensitivity and optimization, etc.) in several places in the report.

Each of the sections following Section II begins with a brief summary of how I see the state-of-the-art in computer aided design (CAD) and design automation (DA) in the different countries. Following these summaries are brief abstracts (almost keyword descriptions) of the main thrust of CAD and DA at the different establishments I visited. Then following these abstracts are longer reports. Many of these longer reports have appeared as European Scientific Notes articles during the past year, but most have been re-edited and, in some cases, have had details added for this report.

II. COMPUTER AIDED DESIGN AND DESIGN AUTOMATION

A. The Development of CAD and DA

One of the earliest applications of digital computers in electrical engineering was in the area of building computers. The repetition and sheer bulk of the design descriptions for digital systems led people early in the game to use computers to keep track of items such as parts lists, wiring procedures, documentation, cross reference lists, etc. The use of computers in the design and fabrication of digital systems has become known as computer-aided design (CAD) and design automation (DA).

For this report, a CAD system will be taken as a collection of software programs and the computers they run on that are utilized in the design of electronic systems; a DA system will imply software systems that participate in the translation of a design to a hardware environment; and a CAM system (computer aided manufacturing) as those software aids which generate output directly used in the fabrication of hardware. For example, the analysis of a metal-oxide semiconductor (MOS) chip geometry to obtain a time-domain response would be CAD; the automatic routing of connection paths on a printed circuit board would be DA; and the generation and use of a punched-paper tape for driving an automatic wiring machine would be CAM. The boundaries between CAD, DA, and CAM are rather diffuse, however, and often the terms are used with much overlap in meaning.

With the production of bulk quantities of transistors with controlled parameters and their subsequent use in the second generation of digital computers in the mid-1950's, came the parallel entry and use of DA and CAD systems. The major computer manufacturers were, by the mid and late 1950's, already using computers in the design of computers. These early programs usually were limited to checking input data fields, physical layout (making sure two packages didn't occupy the same position), fan-out (overloading), and logic design rules, and generally were interfaced (via punched cards or paper tape) to automatic wire-wrap machines.

As the market for computers grew and production increased, design errors and changes became more expensive. Increased attention turned to logic simulation to verify correct operation and to test sequence generation, i.e., the generation of input tests to detect and locate faults in hardware during the checkout process.

Superimposed on the pressures to design larger, faster, and more reliable digital computers, came the development of the Planar semiconductor process in the early 1960's. The Planar process promised integrated functions on a chip. With the arrival of large scale integration (LSI) in the hands of designers in the late 1960's the expense of design changes reached the point where full computer-simulation of integrated circuit (IC) chips became a necessity. Simulators, mask layout programs, and test and diagnostic programs have become essential to the IC industry.

As the size of systems being designed and built grew, the magnitude of the design automation programming problems increased many fold. Not only was storage (memory) capacity troublesome but the combinational aspects of many of the DA algorithms also caused problems.

B. The Logic Design Process and DA

The design of digital systems can be partitioned into three phases: pre-construction design, hardware and packaging implementation, and final testing and error diagnosis.

Prior to any construction of hardware the designer should have at hand items from the DA system such as a computer-generated logic schematic a report of design exceptions (possible errors), and an evaluation of the design via a simulator. Once he is satisfied with the correctness of the design, the next task is to specify the physical layout of the logic.

Several tasks are required by the packaging programs; first, the logic must be partitioned into subsets for assignment to standard IC modules. In this process several constraints must be satisfied; for example, one objective function is certainly to minimize the cost (fewest number of components, lowest cost components, etc.), but in addition maintenance considerations are often equally important. Connector-pin count is usually a fundamental consideration. In the partitioning process the design should be assigned to standard printed-circuit boards (PCB) and to standard IC modules.

Once the design has been partitioned and assigned to cards, these cards must be placed in connectior positions within a card cage or similar hardware. Placement criteria could be based on wire buildup, signal crosstalk, heat dissipation, ease of wiring, neatness, and so on.

In designing both PCB's and IC's, the wire routing to interconnect signals continues to be a problem. Interaction graphics often are used to provide heuristics to solve routing problems, although considerable progress has been made in automatic routing algorithms.

When a new system is still in the design phase (pre-implementation), it can be tested for correctness by using a simulator program. In an analogous way we would like to test a system for correctness of operation after it is realized in hardware. To determine whether a digital system is performing properly, a sequence of inputs is applied and the outputs are observed and checked against the logic function intended. To overcome the combinatorial problem associated with testing all possible situations, schemes (algorithms) have been developed for efficient yet adequate testing. Test sequence generation continues to remain a problem, however, as technology develops in digital systems.

C. Trends in DA

Considerable progress has been made in logic simulation, test sequence generation, placement, routing and in the use and development of high level description languages. Part of this progress is a result of the large increase in computer power and part is due to greater complexity in the systems being built.

Many algorithms and much of the theory for the above processes have not been able to keep pace with the complexity growth. Thus, interactive graphics have often been adapted to use human decision-making rather than an algorithmic approach to a solution.

More effective change control procedures are needed. For example, after spending 100 hours of computer time generating a test pattern-sequence tape, let us suppose a minor change in the design is made. How should the fault tape be changed? Is it necessary to repeat the entire process? Similarly, the translation from specification to design details (synthesis) finds practical solutions elusive.

For the past few years it has been apparent that the correct approach is towards describing and analyzing systems at a higher level. The pay-offs in using high-level programming languages have been repeatedly illustrated. In a similar way the specification and design of digital systems have been moving towards a higher level of description. With architectures for array, parallel, and associative processors becoming increasingly common, we can expect the trend towards higher level descriptions and automatic translation into hardware to continue.

III. CAD AND DA IN GREAT BRITAIN

A. Summary

British universities and industries have had a rather long association with CAD, but its present-day use is characterized by some good research at a few universities and limited use by industry. In my opinion, industrial CAD utilization as compared to that in the US generally lags by several years. Computer access, particularly convenient time-sharing terminals, is often quite limited. Commitment to using and developing new CAD techniques and DA facilities is limited to high pay-off areas (principally PCB layout), and little support is given for efforts towards developing DA systems for new technologies. As bright spots in universities, I would list the work of Bennetts at Southampton on test generation, Spence at Imperial College on interactive sensitivity analysis and optimization, Grey at Edinburgh on interactive integrated circuit (IC) layout, and Lewin at Brunel on simulation and high level logic description languages.

B. Great Britain Short Reports

Imperial College, University of London (Dr. R. Spence)
CAD work in computer graphics, particularly in studying human factors as they apply to interactive circuit design. Considerable work in sensitivity analysis and optimization going on.

ICL, Manchester (Mr. G. Adshead)
DA work is primarily aimed at production of multi-layer PCB's. Also there is CAD work in test sequence generation, layout, routing, simulation, etc.

University of Edinburgh, Edinburgh, Scotland (Dr. J. Grey)
Several CAD and DA research projects are in progress. Past work has been in PCB layout, routing, digital logic simulation, DA languages.

University of Southampton, Southampton, Hants. (Prof. K. Nichols)
CAD work in electronic circuit analysis. Special techniques developed for using CAD programs on small computers. Emphasis on automatic test generation for digital networks.

Mullard Ltd., Southampton, Hants. (Mr. D. Jarvis)
Emphasis has been on development of CAD programs for IC mask layout with supporting programs for circuit analysis, logic simulation, and test generation.

Post Office Research Department, Ipswich (Mr. K. Clark)
Uses CAD programs for PCB layout. Past work with programs for analysis and digital logic simulation.

Heriot-Watt University, Edinburgh (Prof. F. Heath)
Digital system design using interactive graphics system. Work based to a large extent on the LOGOS system.

Brunel University, Uxbridge (Prof. D. Lewin)
Research in digital system design automation, particularly high level simulation and testing.

General Instruments, Glenrothes, Scotland
"Turn key" operation of Applicon IC mask layout system. Additional CAD work in program development for logic simulation and MOS device modeling.

Loughborough Univ. of Technology, Loughborough (Dr. M. E. Woodward).
Logic synthesis via stored program methods. Decomposition and redundancy effects in logic implementation.

Royal Radar Establishment, Great Malvern (Dr. F. E. Withers)
DA system in operation with logic diagram drawing, design rules checking, logic simulation and PCB layout. No current CAD research or development underway.

Portsmouth Polytechnic, Portsmouth (Mr . A. H. Evans)
Hardware construction oriented DA system for digital logic wire wrap boards. Input language, circuit diagram, layout documentation, card and backpanel wiring, and design error checking plus the data base, comprise the principal features of the system.

Sperry Gyroscope Co., Bracknell (Mr. A. Bayfield)
PCB oriented CAD aids. Wire-wrap and design information program being expanded and logic simulation program being developed. Minicomputer interactive graphics system for drawing and PCB being planned.

Plessey Telecommunications Research Laboratory, Poole (Mr. W. Brown)
CAD work is directed towards digital systems, and emphasis is on PCB layout (both manual digitizer program aids and interactive computer graphics) and increasingly on logic simulation with corresponding application to test sequence generation.

C. Great Britain CAD and DA Reports

Design Automation at Brunel University

The stated objective of computer aided design (CAD) research in the Department of Electrical Engineering and Electronics at Brunel University is: "The group as a whole are concerned with the conceptual design, verification, testing and fault diagnosis of complex logical systems." Three academic staff, two support people (programmers) and approximately ten graduate students have been directing their research work towards developing computer programs to assist in the design of digital logic systems - a sizable group in terms of university CAD research.

At the present time, there are two systems of programs that members of the group have developed for computer assisted logic design. They are the HILO and the CALD systems. The HILO development, directed by

G. Musgrave, has been designed to simulate digital logic at both the high level (HI) and the low level (LO) of system description. At the high level, logic is specified at a system level in terms of information flow between the functional blocks making up the logic. For example, at the high level, registers and arithmetic functions (e.g., adder, multiplier) are available, and combinational logic may be described as Boolean expressions, encoders or decoders or truth tables. Low level descriptions include all of the basic gates and flip-flops. In addition, parallel datapaths up to 24 bits wide can be described by simple input statements.

Part of the motivation in the design of the simulator was to be able to simulate large digital systems (40,000 logic gates or about equivalent to a minicomputer in size) in a concise way. By using procedures like partial truth-table descriptions, the behavior of devices like encoders could be specified in two input statements rather than 40 to 50 lines of input that would be required if a gate level description were used.

The logic simulator allows gate propagation delays to be specified for single elements and for groups of elements. This control for delays allows the mixing of fast and slow logic families in the same simulation. HILO also allows initial logic levels to be specified for signals and signal buses. Before starting a simulation, HILO forces the network into some stable state which is consistent with the specified initial values and the network inputs.

In designing HILO, not only were the requirements for good simulation considered but, and just as important, the area of testing, both for fault-cover verification and diagnostic dictionary compilation was considered. Testing of digital systems and subsystems is extremely important and often difficult and costly. Automatic test equipment (ATE) is available for testing digital equipment quickly and accurately, but there is still the problem of what tests to apply. However, writing and checking a test program is expensive and time-consuming.

At Brunel, three approaches have been studied to generate test sequence patterns for detecting digital logic faults. They are manual, automatic and interactive test generation. The current emphasis is on the latter two methods. They hope to get something like 60% test coverage automatically for digital systems. So far they have been working only at the chip level in applications (they are closely working with industry in the development of the simulator) and have been getting about 85% fault coverage for 4000 gate LSI chips. Two approaches to automatic fault checking are being taken: Path sensitizing (D-algorithm) and a heuristic search technique. In the interactive test generation the emphasis at Brunel has been on fault detection and not on fault location. First, a test sequence is manually constructed which detects a fault. The D-simulator algorithm is used to aid and check this process. Faults are introduced in parallel to speed the process.

Next, starting with the Manually specified sequence, the user selects a fault, and the test generation routine tries to devise a set of input waveforms which will render the fault detectable at the network outputs. This process is repeated until most or all of the faults have been covered. Provisions also exist for allowing the system to take on inconsistent logic states so that sequences may be obtained for difficult faults by allowing the designer to make use of prior knowledge of the functional behavior of the logic system.

In comparison to other high-level system description languages, HILO is not a pure registered-transfer level language. Although the system can describe registers, at Brunel they are not trying to use it as a design language but rather in a design verification (simulation) role. HILO differs from most other gate level simulators in that it allows a much wider range of primitive logic blocks. This, of course, makes it potentially more efficient in simulating a large system if portions of that system are described by such blocks.

Over the past four years Prof. D. Lewin has led a team who have produced a set of programs called CALD (Computer Assisted Logic Design). This work began while Lewin was at Southampton University and has continued at Brunel. The CALD software, based on fundamental switching theory, provides synthesis and minimization for combinational circuits and state-table reduction and assignment for sequential logic circuits for up to 20 switching variables.

The early work has been expanded to investigate the development of interactive techniques (using graphic and teletype terminals) for description and evaluation of logic systems. The group are investigating aspects of extending the input specification language to CALD. They are presently considering the Iverson register transfer language, the PMS (Processor-Memory-Switch) and ISP (Instruction Set Processor) languages and such graph theoretics as Petri nets. The CALD system will produce a logic design implemented in transistor-transistor logic (TTL). They are currently adding provisions for implementations in programmed logic arrays (PLA). Within a year they hope to be able to describe a system using either a language or a flow-chart via an interactive CRT.

An ultimate object is to marry the CALD and HILO systems to provide a complete synthesis, simulation and test sequence generation design automation system.

MINNIE - AN INTERACTIVE GRAPHICS CAD PROJECT AT IMPERIAL COLLEGE

Between 1968 and 1971 a small experimental interactive graphics project for electrical circuit design was initiated by Dr. R. Spence of the Electrical Engineering Department, Imperial College, University of London. The objective was to gain experience in interactive graphics and man-machine communication and to move away from the batch-made attitude in engineering use of computers.

As a result of this early study, the Science Research Council (SRC) provided Spence funding to study circuit design via interactive graphics. This research grant (1971-1974) was directed at two closely-linked topics: (1) man-computer dialogue and (2) circuit analysis algorithms. The most obvious end result during this three-year period was the development of an interactive graphics circuit design facility called MINNIE (the name stems from the fact that a mini-computer, a Digital Equipment Corporation PDP-15, is being used in the project). The MINNIE system comprises a graphical input for discrete-component electrical networks, and a frequency-domain analysis which includes both large- and small-change sensitivities.

The SRC made a continuation three-year award (1 July 1974) for approximately £90,000 ($216,000) to Spence to support research on "Dynamic Graphical Interaction in Electrical Circuit Design and Modelling." The grant provides for the acquisition of a new computer system (a PDP-15/76, VT-15 interactive display, and cartridge disk system was purchased) and four full-time personnel.

The directions and objectives for the project remain much the same as before:

(1) The development of concepts and techniques for interactive graphic display, and of algorithms for network analysis.

(2) Research in psychological, ergonomic and perceptual aspects of the interactive-graphic man-computer dialogue.

(3) Development and evaluation of techniques to enable easier use of computers.

Most of the effort to date has been in items (1) and (3). Some work has been done on (2), but an emphasis on it awaits the appointment of a human factors specialist.

The first version of MINNIE was "frozen" in early 1974 to permit the software to be installed at six different locations. Since early 1974 the second version has been developing, and early this year it was also "frozen." The new version of the program had the following improvements:

(a) A new command dialogue - which has been designed to have a "skeleton structure" by providing a simplified display with particular emphasis on preventing users from entering blind alleys when selecting options.

(b) The ability to define a circuit property of interest - which builds in a flexibility by allowing users to define element relationships.

(c) The acceptance of response specifications - that is by allowing the input of a frequency domain behavior specification.

(d) Tracking-sensitivity analysis - which allows global variables (temperature, process parameter, radiation, etc.) to be changed without an analysis for each new value. This is particularly useful for integrated circuit design.

(e) Increased node and branch capacity - where the system now accommodates 25 nodes and 50 branches, it is to be expanded even further through sparse matrix techniques in a future program version.

(f) Model pessimization - which indicates to the user those parts of a device model which do not contribute significantly to the output parameter being viewed.

(g) Comprehensive graph display facilities - permits, for example, a superposition of graphs, the definition of symbols, interrogation of graph values, etc.

(h) Enhancement of existing facilities - in which an additional number of minor features will make the MINNIE system more stable, easier to use, and more computationally efficient.

Considerable progress has been made in the development of new algorithms or refinement of existing ones for linear circuit analysis and design. Statistical sensitivity, differential sensitivity for large component changes, optimization and component tolerance assignment are just a few of the design features being actively developed by Spence and his team. From the beginning, the project has held the human-factors aspect of interactive graphics as equally important as the circuit analysis aspect. As part of the effort along this avenue, a seminar was sponsored by the group about a year ago (ESN-28-8; 285) on "Man-computer diologues for effective circuit design." The progress has not been as rapid as hoped in this phase of the project primarily due to the difficulty in obtaining a person trained in human factors and integrating that person into the project.

The MINNIE project of Spence and colleagues is probably the most intensive research project in interactive graphics in Europe. The dual emphasis on circuit analysis and ergonomics is being meaningfully attacked by the group with reasonable success.

On two points I feel the research program could be improved. The first would be to develop the programs in a less machine-dependent environment. Often they resort to assembly language coding and to using system-dependent features which tie the program to the PDP-15 system more than is necessary. The other short-coming is the recent decision to view the research in a more commercial light, which will greatly restrict the distribution of the program and thus limit to some extent the research results. This second feature is in keeping, however, with the attitude towards software development done under government and university sponsorship in Great Britain.

COMPUTER AIDED DESIGN PROJECT - UNIVERSITY OF EDINBURGH

Dr. J. V. Oldfield has been director of the Computer Aided Design Project of the Computer Science Department, University of Edinburgh for several years. In August Oldfield left the University after 14 years for the position of second Chair of Electrical Engineering at the University College of Swansea, Wales, and Dr. J. P. Gray became Director of the Project. My host for a visit in mid-July was Oldfield, and it was a very informative visit, indeed. My visit follows an earlier ONRL visit in 1972 by Franklin F. Kuo (ONRL-R-11-72), and I will attempt to describe the current research emphasis and the accomplishments since 1972.

Funding for the Project is primarily from the Science Research Council, and approximately $960,000 has been expended since its inception in 1966. The average number of people on the Project has been about ten including staff, research students and visitors. They have been quite fortunate in having their own PDP-10 time-sharing system together with a coupled PDP-7 computer driving a DEC-340 display, as well as Tektronix T-4010 and T-4002 storage tube displays. In early 1973 a conflict arose concerning the possible sharing of the PDP-10 between the CAD group and the School of Artificial Intelligence. Over the objections of the CAD group, the conflict was resolved by expanding the PDP-10, placing the machine under a separate management (outside the CAD group) and having it serve both projects. The added load on the computer has had an adverse effect on the system response for interactive computer graphics. For example, in one demonstration of a printed-wiring-board layout program that I observed, the response times (PDP-7 to PDP-10 connection) were as long as 40 seconds; clearly interactiveness was severely limited.

At present the CAD group efforts are centered about two activities. John Gray is engaged in the development of register transfer design automation programs and John Eades, Jeff Philips and Nigel Rose are primarily emphasizing the further development of layout programs. The work of Gray and his students has resulted in a suite of programs which form an aid for design when using DEC PDP-16 register transfer modules. The program suite (named ARTHUR) checks for logical errors, checks the operation of algorithms, produces a list of specific modules and the interconnections necessary to build hardware, and can produce flowcharts for a complete design. Gray anticipates further work in this area, particularly in looking at higher language levels for describing digital systems.

In the past the group has had a strong effort in printed-circuit-board layout. An early development (N. A. Rose and J. V. Oldfield, "Printed-wiring-board layout by computer," Electronics and Power, October 1971) used an abstract topological model of the circuit in which first a planar graph was constructed after which a pseudoplanar graph was built in an attempt to both place and route (one side) a discrete component electrical circuit.

A more recent project (July 1973) by A. K. Hope has involved the application of interactive computer techniques and graph-theoretic methods to printed-wiring-board design. This has led to the development of a two-sided digital integrated circuit board program in which graph partitioning is used in the automatic component placement and a stepping aperture approach is used for conductor routing. Both the placement and the routing phases have provisions for interacting via the graphic console.

Another recent project (PhD thesis work by B. Dervisoglu) concerned computer aided design techniques applied to digital logic design. Basically, the work consisted of describing the logic components which realize the required operations, making connections between their terminals (via a graphics screen), and then using a simulator to test the design. The method used in the design philosophy divides the operations to be performed by the target machine (the digital system) into two types, data and control, and components are defined to realize both parts. At this time it's not clear that work will be continued along the lines started by Dervisoglu.

The Computer Aided Design Project has, in the past, maintained good contacts with industry. A collection of programs to assist in the design of integrated circuit layout is the result of one such relationship. The system, GAELIC, allows a user to specify integrated circuit layouts either by means of a launguage or via a digitizer and a rough sketch. He can then interact with the data structure by means of a storage tube presentation. For example, a user can move or delete an instance of a shape, he can repeat instances, he can define new shapes, etc. The ultimate products are production masks for integrated circuits. This is currently one of the most active projects.

The strength of the Computer Aided Project has been in good facilities, good people and a continuation of leadership. Perhaps in the past printed-circuit-board layout has been emphasized a little too much, but the recent projects in higher level digital description languages and interactive integrated circuit mask generation have addressed themselves to useful, real-life problems.

COMPUTER AIDED DESIGN AT THE UNIVERSITY OF SOUTHAMPTON

The computer aided design (CAD) effort in the Department of Electronics, University of Southampton is led by Mr. K. G. Nichols and Dr. R. G. Bennetts. Nichols has been engaged in using computers in engineering design for several years and presently is overseeing the development of linear and non-linear electrical network analysis programs. Bennetts has been involved with computer assisted logic design in cooperation with Prof. D.W. Lewin of Brunel University. Bennetts' primary emphasis currently is in the automatic test sequence generation for testing complex digital networks.

The computer-aided circuit analysis work at Southampton has been done for the most part on a small computer. The turn to a small machine was prompted by rather severe problems of access and turn-around time on the University's central computing facility (an ICL 1907 with 96K words

of core). Nichols is of the opinion that even when adequate large computing facilities are available, there is still a case to be made for providing some analysis and design programs on a small machine. Because of the emphasis on small machines, Nichols and his associates have devised a program development philosophy which can be summarized as follows: 1) All main analysis programs are written in FORTRAN II (for small machine compiler efficiency). 2) The main analysis programs each fit into 16K work of 16 bit store. 3) The main analysis programs are highly modular and hierarchical with exhaustive documentation. 4) Each main analysis program has a specific input program, and 5) All input is by means of a simple commands with free-format fields. The computer they are using is a Honeywell DDP-516 with 16K of 16 bit words for memory and a 1M word fixed-head disk backing store.

Two fully developed network analysis programs have been used for several years by a number of undergraduate and postgraduate students in connection with a variety of projects. The two programs are ICAP which is a small-signal ac analysis program and ITAP which is a non-linear dc and transient analysis program (K.G. Nichols, "Computer-aided analysis of electronic circuits on a small machine," AGARD Conference Proceedings No. 130, Lyngby, Denmark, 21-25 May 1973). The primary distinction of the two programs is the fact they are operational on a small computer and in doing so, the programming has used some very clever storage compacting techniques, all within FORTRAN. The group are working further on sparce matrix schemes with regard to computational speed and accuracy in a small machine environment. Nichols, at this point, feels that sparce matrix storage will save little in storage with the problems they are working with, but the potential gains will be in speed. In all of the analysis program developments, the emphasis has been on economic use of the programs in the sense of efficient algorithms for a restricted set of problems.

Past work under Nichols' supervision has been in automated pattern drawing for generating integrated circuit masks, automatic layout of printed-circuit board, and automatic circuit synthesis procedures.

The automated pattern drawing work involved the simultaneous development of hardward vector generators to control a laser mask-making machine and the development of a high-level mnemonic-language for describing mask patterns. The first language (LASMASK) was rather conventional in that commands for lines, rectangles, step-and-repeat of patterns, etc., were incorporated. More recent program development has been towards a program (PATTERN-MASTER) that retains the principal features of LASMASK but also provides extended features with applications such as printed-circuit board and electronic circuit schematics in mind.

The recent work in printed-circuit board layout is similar to the directions being taken by others who are developing layout programs - namely, making the programs more interactive by means of visual display units. The basis of the Southampton layout program is a topological representation of the interconnections and components (dual in-line integrated circuit packages) in the form of a graph. Rather than a full software approach to a placement and routing, they are pursuing a development which allows the designer to use his experience in component ordering as a means of reducing computing time and memory requirements.

The work in design automation by Bennetts and his students is leading-edge research in test sequence generation for testing logically complex digital networks. Bennetts believes that the gap between the test sequence generation (tsg) theoreticians and the tsg practitioners is due to the "opaqueness" of some of the papers, i.e., these papers are not solving the major problems as seen by the practitioner, rather the papers are concerned with more esoteric and academic problems. He feels that the way to solve the problem of developing an algorithmic tsg for large networks is to partition the networks. A modular approach (R.G. Bennetts, et al, "A modular approach to test sequence generation for large digital networks," Digital Processes 1, No. 1, 1974) to tsg is probably the principal research emphasis of the group. Bennetts states that technically, the modular approach, may be said to be an application, at the system's level, of the sensitive patch concept. Basically, the method consists of (1) partitioning a large network into separate sub-networks, (2) then by using existing algorithms, determining the tests for each module, and finally (3) matching the test outputs from one module with test inputs until "forward" matching reaches an observable output and "backward" matching reaches actual inputs. They have written programs for the second and third steps

and are evaluating the software. They have yet to identify the criteria for partitioning networks into a suitable set of modules, feeling that the range of applicability of the inter-module test chaining must be evaluated first. Their early examples have been very promising for the method. They feel that the modular approach has the potential for overcoming many of the problems that have beset automated tsg.

Bennetts is also involved with a program of research to study the relationship between circuit design procedures, final implementation structures, and final testability. In particular they are looking at hoped for solutions to the following: 1) What features contribute to a circuit that is testable? 2) How may these features be included in design algorithms? 3) What extra logic, if any, will enhance the circuits testability?

Most of the computer work by Bennetts and his associates has been on the University's central ICL 1907 computer. Some work is also being performed on a Varian 620/L minicomputer system.

The University of Southampton is scheduled for one of the ICL New Range computers sometime during the next year (a 2970 (P3) system). Bennetts anticipates a lot of his work will be done on the new machine. Nichols has accomplished much within the confines of the small and slow Honeywell computer, however, I believe the work could be profitably extended to encompass a much wider set of problems by moving to a larger and faster machine. It was not clear whether or not Nichols is going to move his work onto the ICL 2970 system when it becomes available.

My general impression of the research at Southampton in both the digital and analog CAD is very favorable. They maintain close contacts with both industry and other universities. In addition, their attitude is to tackle problems which are problems to practictioners rather than to theoreticians.

DESIGN AUTOMATION AT LOUGHBOROUGH UNIVERSITY OF TECHNOLOGY

Dr. M. E. Woodward of the Department of Electrical Engineering is investigating switching circuit design at the sub-system level. Woodward and his research students have been studying stored program implementation of switching functions rather than implementation by means of discrete logic gates. Their investigations can roughly be divided into the main areas of: basic theoretical design concepts using stored program modules, computer-aided design techniques, and applications to arithmetic functions and digital filtering. The advent of semiconductor read-only memories (ROM) has given rise to the economical realization of sequential machines as stored-program switching systems. However, theory has not kept pace with the hardware technology. Most all of the established design techniques for the design of switching systems (minimization, assignment, etc.) are applicable only to discrete gate level digital design and are not appropriate to system or sub-system level design. Woodward and his associates are studying techniques for the decomposition of stored-program sequential machines into non-loopfree structures. The techniques they have developed yield near uniform structures with little redundancy in storage requirements ("Realization of stored-program sequential machines," Electron Lett. 10, 246, 13 June 1974). They have developed a computer program which generates the set of all closed partitions of the states of a sequential switching system (Electron. Lett., to be published). They have also extended the application of these techniques to the hardware implementation of digital filters using stored program modules. Another problem they are currently investigating is the effect of redundancy on ROM storage, that is, how ROM storage bits is a function of the way a system is decomposed; for example, in some cases a parallel partitioning leads to the minimum structure, whereas in other cases, a serial decomposition is minimal.

DESIGN AUTOMATION AT INTERNATIONAL COMPUTERS LIMITED

Design Automation (DA) at International Computers Limited (ICL) is spread across the three main design facilities located at Manchester, Kidsgrove, and Stevenage. Approximately 150 people are engaged in DA out of some 30,000 employed by ICL. The 150 are split among engineering application programmers (25%), technicians (43%) and computer operators (32%). At Manchester 25 engineers and programmers, 15 technicians and 20 computer operators are in the DA sector. The technicians are principally used for the coding of input, checking runs, and providing programmer assistance, and the operators run the five computers that are dedicated to DA work. Mr. H. G. Adshead is manager of the DA sector within ICL and his responsibility encompasses all three facilities. Adshead was my host on a recent visit to Manchester and provided a full, informative and very worthwhile visit.

A rough breakdown of the types of DA work at the three facilities is as follows:

Manchester - Design of large central processors. There is a precision multilayer printed circuit board plant, and DA is concerned mostly with multilayer boards and backplanes with some microcircuit and LSI work. Two computers (ICL 1906A and ICL 1906F) are operated by the DA people.

Kidsgrove - Design of terminals, disk controllers, etc. There is a multilayer plant and machine assembly facilities. An ICL 1903S is operated by the DA group, with most DA work devoted to multilayer board design.

Stevenage - Design of small processors, peripheral controllers, etc., but no manufacturing. Two ICL 1903S computers are used mostly for multilayer board design and layout.

As perhaps gathered already, by far the major effort and emphasis of the DA work centers itself on the design of multilayer printed circuit boards. The current DA system (known as SYSTEM 71) consists of approximately two million instructions (almost entirely in assembly language) and represents an investment of approximately $4.5 M. About six boards a day are currently being designed at the Manchester facility. Typical boards have 16 layers and up to 2400 wires, and the rate of uncompleted paths on a board is less than 1.5%, with over 60% of the boards resulting in 100% completed inter-connections. For the most part ICL design is being used, and the routing programs perform the appropriate transmission-line design rule checking.

For an accepted design, several items of production data output are produced including NC tapes for art-work, drilling and assembly operations, full production documentation, testing tapes for continuity and functional testing, logic drawings, modification instructions, tapes for diagnosis and documents for production control and forward ordering. Over 4000 magnetic tapes are stored on past completed designs, and the program implements design changes in a way so as to minimize modifications.

The present utilization of DA at ICL is very closely tied to production payoff, and consequently, of the many processes that could lend themselves to automation, tracking has received the bulk of attention. Over the past eight years a succession of tracking (≡ routing) algorithms have been implemented. They found from early studies that heuristics rarely achieve a success greater than 70%, Lee's algorithm with Acker's modification yield tracking successes of about 95%, while cellular wiring (first reported by Hitchcock in 1969) averages 99.6% and has proven the most successful of the tracking algorithms implemented by ICL. Channel assignment, line search, stepping aperture and other techniques have not appeared attractive, although up to 98.5% tracking successes have been achieved (see H. G. Adshead, "Optimizing Automatic Tracking of Multilayer Boards," AGARD Conference Proceedings No. 130, Copenhagen, May 1973).

In looking to the future, Adshead sees the next possible development in DA at ICL in the area of logic system simulation, particularly coupled to test pattern generation.

ICL has a considerable investment, extensive commitment and a strong group in design automation. If they have a weakness, it is perhaps, that their development of techniques is too closely coupled to immediate payoffs without enough research on future DA investigations. This is not completely surprising in view of the financial position of ICL which has not been especially strong, even though they are number two in size in the digital computer field.

MICROCIRCUIT DESIGN AT GENERAL INSTRUMENT, GLENROTHES, SCOTLAND

The General Instrument Microelectronics Group (GI) at Glenrothes, Scotland, is one of three GI integrated-circuit MOS plants (the others being located in New York and Naples) and has capability for applications engineering, design, mask making, diffusion; assembly, test and quality control.

Currently, GI is taking a rather pessimistic attitude towards custom integrated circuit (IC) design. Before a custom design is started, the predicted sales must be greater than 200 K items for the first two years. This is in contrast to the trend in Europe and UK where IC manufacturers have been moving towards more custom work after finding the competition with US semiconductor houses tough in standard product lines. Perhaps GI knows something the other manufacturers don't. It was disclosed, however, that new product developments must have the approval from company headquarters in New York.

I was particularly interested in the use of computer aids at Glenrothes for two reasons: With the parent company in the US, would the UK concern simply use computer aids developed in the US, or would they develop their own aids, and additionally, on what scale would computer aids be used in a relatively small company (approximately 20 engineers of 300 employees are actually engaged in MOS IC design)?

GI uses mostly US developed software, although they do have a few people working in this area. They have written a logic simulation program which is interesting in that the simulator has a direct relationship with the transistors which are described in terms of IC chips layout geometries as opposed to most simulators which make use of logic gate descriptions. Furthermore, the simulator is operational on a company-owned minicomputer (a Digital Equipment Corporation PDP-11/05). Also available on the minicomputer is a MOS P-channel transient analysis program. This program uses the physical dimensions of active device models and the geometry layout to include the effects of stray capacitance in calculating the time response. The use of geometry descriptions for active devices appears to be the general trend in transient analysis programs for MOS design as opposed to discrete component descriptions which has been the rule in past network analysis programs. Because of the computer's speed and size, the circuits must be partitioned into 20 to 30 transistor subgroups for analysis by this program. Whereas the simulator program has been designed and programmed by the people at Glenrothes, the transient analysis program (named CIRC) was developed at the University of Utah under a contract between the University and the Xerox Company (from whom GI obtained the program).

The IC layout is designed on a purchased "turn-key" graphics system also developed in the US. The Applicon Design Assistant System was purchased approximately one year ago by GI. The heart of the Applicon System is the PDP-11/05 computer. (Applicon did about $6 M of business last year and have installed over 800 systems since their first delivery in 1970.) General Instruments have sent a programmer through the Applicon software school, and they intend to do their own program maintenance, program extensions, and future program developments.

After the layout is completed, further programs developed at Glenrothes do design rule checking (mask overlapping, spacing between conductors, loading) and write the individual mask layer patterns onto magnetic tape cassettes. Up to 16 mask layers can be handled although only five to seven are usually used. The cassettes are then used to drive a Gyrex Photo-head plotter to produce the master masks.

Future computer-aided design plans at Glenrothes are aimed at providing more design documentation and to further develop their logic simulator.

The design of MOS chips at General Instruments is centered about, and completely dependent on their computer aids. Although they have a small force maintaining and developing software, their designs appear to go smoothly through the facility, and they seem to have the flexibility to match computer design aids to design and production requirements.

INTEGRATED CIRCUIT DESIGN AUTOMATION AT MULLARD SOUTHAMPTON

The Integrated Circuit (IC) Development Division at Mullard Southampton is comprised of four sections: The MOS group, the Bipolar Transistor Design group, the Consumer group, and the Computer Aided Design (CAD) group. Mr. D. B. Jarvis is leader of the CAD group which consists of ten men and operates a medium-size ICL 4130 computer. Although the plant produces components (resistors and capacitors), tran-

sistors, diodes, vacuum tubes, and LSI chips, the effort by Jarvis and his group is primarily in support of the metal oxide semiconductor integrated circuit (MOS IC) effort, particularly MOS memories. Until a year ago the principal effort was in transistor-transistor logic (TTL) designs, but since then, a majority of the new designs have been in MOS memory devices. I was told by Jarvis that the Southampton plant is the main diffusion facility in the UK for semiconductors.

The philosophy in the development of CAD IC techniques at Mullard has been to aid the designer rather than to replace him with fully automated programs. Often, according to Jarvis, CAD systems have been developed which try to re-structure the design problem so as to reduce the number of degrees-of-freedom, and thus, to make possible the use of exhaustive search algorithms. In doing so, the programs often tend to be tied to a particular technology, which shortens their useful lifetimes. Frequently they also tend to be inferior in performance to algorithms allowing human judgment. Mullard has placed the emphasis on allowing free intervention by the designers.

Their work has developed along six lines: (1) Mask design and fabrication, (2) Electronic circuit analysis, (3) Digital logic simulation, (4) Test sequence generation, (5) Test data analysis, and (6) Large logic circuit design system. In using the mask design program, a design can be described with an input language, can be digitized directly, or can be input using a graphics display. All three of these methods of program input are in general use by other companies who make IC masks, but Mullard is perhaps unique in having all three in one program with easy transferability among the three. Their circuit analysis is accomplished using two programs: CAMOS and PHILPAC. The CAMOS program can compute the dc and transient response for MOS circuits (p or n channel and enhancement or depletion devices). The transistors are described by the geometries of the diffusion masks, and the program calculates capacitance by using the geometries of the nodes (conductors). Networks with up to 100 MOS devices can be accommodated on the ICL 1430 computer being used by the CAD group. The PHILPAC program is a development of Philips Inc., Eindhoven (Mullard is a UK subsidiary of Philips), and is used at Southampton via a teletype and telephone line to the Philips IBM 370/195 computer. The present limits for the program are 200 network nodes, 170 components, and 50 transistors which is similar to other programs (CIRCUS,SPICE, ASTAP) with much the same analysis capabilities. PHILPAC can perform non-linear dc, linearized ac, and non-linear transient analyses. The non-linearities are limited to the transistor and diode models and to the input sources. The program is considered proprietary and is not expected to be released to users outside the Philips family.

Logic simulation and test sequence generation is via a program (LSTV) written by Mullard Southampton. The logic simulator can deal with both static and dynamic logic and can be run in two modes. The time mode of simulation gives the most detail about circuit response. Each gate is modeled as an ideal logic element followed by a delay whose value depends on the signal transition direction. All changes in logic value are assumed to occur instantaneously, but the delays make it possible to model propagation of signals, spike generation (glitches) and race conditions. For efficiency, new values at gate outputs are computed only when changes at inputs occur. Undetermined states are also dealt with, so network initialization can be handled without problems.

The other simulator mode, the code mode, simulates 10-20 times faster than the time mode but only gives the network equilibrium values following each input change. The program converts the network description into an equivalent set of Boolean equations which are solved for each set of inputs. Gate delays are ignored. Program provisions avoid recursion of bistable loops but allow the modeling of internally generated pulses. A limitation of the code simulation mode is that undetermined states cannot be dealt with. The simulator can accommodate up to 3000 gates, but most problems run on it at Southampton are in the range of 50-500 gates.

Functional test sequence generation is done with the aid of LSTV simulation program. Engineers prepare proposed test sequences, and logic output values are computed by simulation. The test verification portion of the simulator next automatically adds single faults and resimulates the network. Stuck-at-one and stuck-at-zero faults for each gate input and output are introduced, and a defect is noted in each case where the faulted network output is different from the unfaulted. Output from LSTV is a list of defects not detected for the pattern under consideration.

The test generation portion is rather straightforward with no strategies for automatically generating test patterns and nothing, for example, like parallel simulation for checking several sequences simultaneously. Consequently, the test generation probably will not be able to accommodate large systems in either a simulation or test sequence pattern checking modes.

Another program developed at Mullard Southampton is for designing intergrated injection logic chip mask patterns. The program, DAISY (Design Automation for Integrated SYstems), is normally used in conjunction with the logic simulator and the circuitmask program. DSAISY was designed with emphasis placed on producing small area-efficient chips. In test, the program utilizes about 10% more area than a fully optimized manual layout. The interconnections are specified for DAISY in the same network description as for the LSTV simulation program. The use of DAISY for layout is basically a manual process of placement and routing, but a fully interactive display system is operational with the ICL 4130 computer system. An important function of DAISY is the check made against design rules such as interconnection capacitance to insure the layout conforms to the logic network. It is anticipated that DAISY will be extended to the design of MOS devices.

With the system of programs in use at Mullard Southampton, a high level of confidence in designs is achieved. Good design coordination is provided by the fact that one engineer takes a design through the complete cycle. About two to four designs are started each week, although less than 100 go into production in a year's time. Records are kept on the final device tests, and a statistical data reduction is run on the ICL 4130 to aid in process control, design verification, and model parameter determination.

DESIGN AUTOMATION AT PLESSEY, POOLE, DORSET

Four years ago the computer aided design (CAD) activity at Plessey Telecommunications Research Laboratory, Poole, Dorset, was visited by F. F. Kuo from this office. At that time the CAD work centered on extending the CALD system (ESN-29-6; 268), developing a high level input processor language and on interactive computer graphics. Today, the CAD effort is principally concerned with two problems: printed circuit board (PCB) layout and PCB testing.

In PCB design they use three methods for the layout of approximately 150 new board designs each year. Besides the continued use of manual layout, they use a combination of manual-digitizer layout in which several digitizers are time-shared on a minicomputer. The digitizer makes use of a rather complete menu of layout patterns held internally in the computer. The computer also provides a fair amount of feedback in the way of messages during the placement and routing phases. PCB's are also designed using the Redac PCB system on a PDP-15 computer equipped with a graphic console. They have had the Redac program for a little over a year and are finding that new and larger board designs are pushing both the computer and software. They are seriously looking at modifying the software and may be forced into doing future board designs on their larger ICL 1906A computer.

Coupled with increasing larger and more complex PC boards, the problem of testing the boards is becoming of serious concern. Mr. W. Brown, leader of the digital CAD activity, said they have been particularly worried with the testing problem and are placing an expanding effort in developing CAD aids for test generation. To this end, they have developed two digital logic simulators; one a three-level simulator capable of accommodating networks up to 1000 gates (too small for their newer PCB's) and the other a two-level parallel simulator. They are also concurrently investigating algorithms for test generation to be used with the parallel simulator plus further developing and extending the simulator itself.

Although considerable earlier cooperation existed between the CAD activities at Brunel University and the University of Southampton and Plessey, they now appear to have considerably less joint cooperation. As a consequence, I feel they have not progressed as rapidly in the simulation and testing areas as they would have with a continued close association. Likewise, the work in interactive graphics, while at one

time quite active and advanced, now is absent (at least in CAD). It didn't appear that interactive CAD, with the exception of the Redac system, is likely to become an active project soon.

Brown sees a continued emphasis on PCB layout and testing but does not see Plessey developing digital design aids for logic synthesis, assignment, or partitioning. Similarly, because they find computer costs expensive (and hence simulation of logic expensive), he believes that prototype construction will remain the primary mode of design at Plessey.

IV. CAD AND DA IN SCANDINAVIA

A. Summary

The most striking feature of CAD and DA in Denmark, Finland, Norway and Sweden is the enthusiasm and attention companies are giving this field. Electronics technology is receiving considerable emphasis in all four countries with quite visible signs of new buildings, equipment, and computing facilities. At most companies a small but determined CAD effort exists. Usually these are directed at aspects of automation closely coupled to manufacturing and production (PCB and test sequence generation (TSG)). For the most part, there is a heavy reliance on software developed outside Scandinavia (for example the British Redac PCB system and the US TEGAS TSG system). Thus, in general, industry here lags in comparison to U. CAD usage by several years. However, it is moving much faster than Great Britain in this field and I believe will surpass it in a few years. University relationships with industry are very good. Tordhol at the University of Trondheim, Kjelkerud at the Royal Institute of Technology, Stockholm, and Lindberg at the Technical University of Denmark all have excellent CAD and DA research projects which would compare favorably with US university research.

I found a very high degree of cooperation among universities and companies in regard to CAD planning and sharing of programs. This was particularly true in Norway as well as in Finland and Denmark but not so prevalent in Sweden. This cooperative effort was not nearly as obvious elsewhere in Europe, and in fact, universities in Britain seem to be viewing software development with an eye towards commercial exploitation.

B. Scandinavia Short Reports

SWEDEN

LM Ericsson, Stockholm (Dr. C. Jacobaeus)
Several programs for filter synthesis, analysis, and optimization. Current work directed towards PCB layout and testing.

ASEO-HAFO, Vallingby (Mr. H. Berg)
CAD and DA programs for custom MOS-LSI design include circuit analysis, logic simulation, and MOS artwork layout.

SAAB-Scania, Linkoeping (Mr. B. Magnhagen)
CAD/CAM system exists for digital electronics and includes application programs for wire list and NC tape production, logic diagrams, PCB layout, and logic simulation.

Philips Teleindustri, Jarfalla (Mr. L. Fransson)
CAD work is currently limited to interactive graphics PCB layout and evaluation of digital test pattern generation programs.

Royal Institute of Technology, Stockholm (Dr. E. Kjelkerud)
Primary CAD research on logic simulation, fault simulation, models, and test generation for digital circuits. Current emphasis on parallel fault simulation and testing.

FINLAND

Nokia Electronics, Helsinki (Dr. P. E. Ahonen)
CAD being used in filter design and PCB layout and in microprogram simulation, logic simulation, wirewrap production and test generation for ATE.

Technical Research Center of Finland, Helsinki
Just beginning a survey of CAD program availability and suitability for Finland's industry.

Helsinki University of Technology, Otaniemi (Prof. V. Porra)
Extensive CAD program development for microstrip circuit development. Transistor modeling, circuit optimization, transmission line analysis, stability analysis and hybrid circuit layout programs have been developed.

DENMARK

Elektronikcentralen, Horsholm (Mr. P. Stangerup)
Analog circuit analysis program development, also some work in filter analysis and reliability modeling by computer.

Technical University of Denmark, Lyngby (Prof. E. Lindberg)
Linear and nonlinear circuit analysis program research with emphasis on sparse matrix techniques and fast integration methods. DA work in interactive (storage tube) PCB layout and logic simulation.

NORWAY

Kongsberg Våpenfabrikk, Kongsberg (Mr. P. A. Arneberg)
Printed circuit board program development (both interactive graphics and automatic placement and routing), projects in digital logic simulation and test sequence generation for ATE. Some work in data base development for DA.

Norwegian Defense Research Establishment, Kjeller (Mr. H. Schiøtz)
Digital logic simulation program development. Microprocessor simulation at system level (instruction simulation), gate level, and also cross-assembler development. Some program development for wire-list generation and PCB layout.

Electronics Research Laboratory, Univ. of Trondheim, Trondheim (Mr. H. Tordhol)
Digital logic simulation and test generation studies (TEGAS program), PCB layout including placement and routing, and high level system simulation.

Central Institute for Industrial Research, Oslo (Mr. A. Landmark)
Current work is directed to developing a comprehensive data base for digital logic DA.

C. Scandinavia CAD and DA Reports

COMPUTER AIDED DESIGN IN KONGSBERG, NORWAY

Although the translation of A/S Kongsberg Våpenfabrikk (KV) is "Kongsberg Small-arms Factory"(Kongsberg is a small town 53 miles southwest of Oslo), the company is diversified and serves both civilian and military markets. Administratively, it has five product divisions: defense products, automobile parts, gas turbines, electronic systems, and computers. A little over 6800 people are employed by KV.

The company has maintained a strong development capability, and to aid this, a Technology Section was established a few years ago. Per A. Arneberg heads this section, which evaluates new technology and brings it to the attention of other groups within KV. However, the primary emphasis of their work is in computer-aided design (CAD). Arneberg has divided his people into three groups: 1) a CAD group which mostly does printed-circuit-board (PCB) layout, 2) a prototype PCB group and 3) a development group for CAD problems.

Up until a year and a half ago, KV had an on-site IBM 360/40 computer. Since that system left, a computer-service company in Oslo has been the source of computer time. An IBM 370/158 and a Univac 1110 system are both available through a remote batch terminal. The present arrangement is awkward in developing a CAD capability, and Arneberg stated that he believes they will soon have a local computer.

Arneberg does most of the initial coordination in new technology transfer within the company, and a recent example is their experience in testing of printed-circuit boards (PCB's). They made a 12-month projection of the number of PCB's that would need to be tested. In 1974, about 20,000 boards were tested, comprising about 150 to 200 different types. If testing were to be done the same way as in the past, KV would have to hire 5 to 15 new people just to write test programs. In the past and currently, the PCB's in use at KV have contained 30-35 dual in-line integrated circuit (IC) packages. There is a very marked trend towards using larger boards (up to 150 IC's). It is an almost inhuman task to write test sequences manually for testing 150 module boards, hence a new method was needed at KV.

A project was started in conjunction with the Royal Council on Scientific and Technical Research (NTNF) to find out what is available in the world today for generating test patterns more efficiently. The study concerned only computer programs for test generation and did not include a study of test equipment. The principal programs which were evaluated included the following: CAPS (General Radio), FLASH (Membrain), FLOG (Time-Sharing Ltd.), FAIRTEST (Fairchild Semiconductor), TESTAID (Telpar) and TEGAS (Comprehensive Computing Systems and Services). The net result of the investigation was that NTNF and a group of Norwegian concerns (including KV) acquired the TEGAS (Test Generation and Simulation) program marketed by CCSS, a company based in Texas. According to Arneberg, this program was chosen, for several reasons, among them being the fact that TEGAS has one of the most advanced and fastest simulators available and additionally it does test-pattern checking in a parallel fault simulation mode. This parallel simulation means a speed gain in checking patterns equivalent to the word-size of the computer on which the program is being run (a factor of 32 for an IBM 360 or 370 system for example). The program is written entirely in FORTRAN and has several simulation and testing modes. It also has provision for describing digital systems at different levels (gate level to complex functional module level) (S. A. Szygenda, "TEGAS2 -- Anatomy of a general purpose test generation and simulation system for digital logic," Proceedings of the Design Automation Workshop, Dallas, Texas, June 1972).

The TEGAS program has been operational on the IBM 370/158 in Oslo since December 1974, and at mid-January only a medium-complexity test program had been run. The program used 76 seconds to analyze 40 input test patterns yielding an 80% fault coverage for the 27 IC (150 gate) network. The real fault coverage for the hand-generated patterns for the same network was not known at the time of my visit, but was the next item to be checked. It is a recognized fact that rarely is the fault coverage known for hand-generated test patterns.

Although the move towards automatic test pattern generation represents the next step in CAD at KV, there are two areas that are constantly used at the present time. So far, the distinct CAD steps have been in: 1) PCB layout and 2) Computer produced tapes for semi-automatic wiring machines. If wire-wrap technology is being used in a design, the engineer collects the data and writes the wiring list for the LIST program. The program, which is run on the Univac 1110 computer in Oslo, produces the punched paper tape to control the wiring machine and a wiring schedule printout for system documentation. This program has been in use for several years, and because it neither interfaces with a data base nor provides the engineer with design information, it has not had much effect on the design process.

The PCB layout system has had more of an impact. KV purchased the Redac Software Ltd., Tewkesbury, England software and a PDP-15 computer system from Digital Equipment Corporation. To date, the system has kept pace with PCB layout requirements, but as with the requirement for test pattern, Arneberg is faced with increasing this capability by a factor of three.

About two and a half years ago, KV started a project in which they evaluated the potential for using a computer system for electronic circuit schematic drawing. They defined specifications for what they would like to see in such a system, but the analysis showed such a system would not be economic compared to their manual drafting process. During the specification process, they started some cooperative work with Redac which, however, was discontinued at an early stage. Redac continued the development of the software and have recently announced the availability of a logic schematic program which is used in conjunction with their PCB software system. At this time, according to Arneberg, KV does not intend to acquire the software, because of the more pressing problems of testing and PCB layout.

In the process of technology evaluation, KV has been conducting both a time and cost study and an operational analysis on the electronic design of digital products. The purpose of these studies is to look for priority areas in which to take the next steps in using computers in design. Certainly one area under consideration is to connect the CAD steps for schematic drawing (now manual), PCB layout (on the PDP-15), test pattern generation (TEGAS program), wirelist generation (on the Univac 1110) and simulation (TEGAS program). At present, each of these programs has separate input descriptions and data procedures, and there is no feeding of information from one process to another. Arneberg believes the central part to tie these together is a data base. To this end KV has been looking at acquiring a CAD system (data base system) rather than continuing with the development or purchasing of single unconnected programs. They will probably evaluate what is available in CAD data bases as the next step in CAD system development. Arneberg feels that the adoption of such a system will radically change the design process. Where now each designer works in a step-by-step way with little effect on other stages of the design, a data base will force an interdependence. Designers will have to get much more involved with computers, and will probably have to do a lot of the data preparation themselves.

KV is taking an aggressive attitude towards incorporating CAD technology into their design process. They are doing it in cooperation with other Norwegian concerns, thus being one of the few united efforts in European countries in this respect.

ELECTRICAL ENGINEERING AT THE NORWEGIAN DEFENCE RESEARCH ESTABLISHMENT

The Norwegian Defence Research Establishment (NDRE) is located fifteen miles east of Oslo in the small town of Kjeller. The facility reports to the Defence Ministry and is engaged primarily in development and research activities for the military forces. The establishment is organized along several technological lines including electronics, weapons and materials, toxicology, explosives and underwater acoustics. Approximately 400 people are employed at NDRE and the largest division is electronics with 150. This Division is probably Norway's most significant effort in military electronics R&D. Even so, much of its work is unclassified and is generally made available to official visitors.

The Electronics Division has groups working in general circuit design, software development, computer design, electro-optics, communications and radar. I visited H. Schiøtz who is engaged in digital hardware design and is leader of the digital design group of ten persons. About half o this group have university degrees and the remaining have technical training They both support and do engineering design.

Schiøtz also has been closely coupled to NDRE's use of computers in electronic design. The computer aided design (CAD) work is not a formal laboratory effort nor is it being done by any particular group, but rather, computer aids are developed in conjunction with normal research projects. Schiøtz became interested in CAD while on a fellowship leave at National Semiconductor, Incorporated, California, about three years ago. While there he designed and programmed an initial version of a digital logic simulator. A revision of the program, called LOGSIM, was made when he returned to NDRE and a user's manual was written. Subsequently, a software company in Oslo obtained marketing rights to the program and has offered it on their computer network to subscribers. Data SAAB in Sweden is one foreign user of the program. Some problems with the second version of the simulator remained, however, in both storage and run inefficiency, and in general, the users at NDRE could solve only a subset of their problems. A decision to revise the simulator was made and about one year ago an engineer programmer at NDRE was assigned the task of completely rewriting the program. Special attention was given to speeding up the simulation mode and in economizing the storage of data. The newest version became operational on the NDRE computer in January, 1975, and Schiøtz finished the accompanying user manual in late February.

Basically the program is a two-level (true-false), gate-level logic simulator. The program makes use of a library which contains physically available integrated circuits. At present, the library contains descriptions

for about 60 of the TTL logic family devices (7400, 7474, 74193, etc.), a few 10,000 series ECL logic devices and a rapidly growing number of CMOS integrated circuit modules. Read-only-memory elements are treated like any other logic element. During use the stored pattern is specified. When modules are added to the library, rather than describing them at a logic gate level, they are generally expressed as FORTRAN functions (subroutines). The simulator program is written in FORTRAN, and the use of FORTRAN expressions to describe the function of a logic module is very efficient at program run time. The manual supplies enough information so a user can write and add to the library for his particular run.

Input to the program is relatively simple with essentially two pieces of information required: (1) The end connections between all pins in the circuit listed in the format: module type, module serial number, pin number; and (2) The input signals with their level as a function of time (standard pulse generators are a part of the library). This input is generally prepared on punched cards and read through a remote batch-energy station onto disk at the computer center. Some checking, although not extensive, is done for syntax and semantic errors for the input data.

When CMOS logic devices are employed, the program uses the supply voltage specified by the engineer (or 5 V by default) to calculate the nominal gate delays for individual devices. Another interesting and useful feature available during run time is the ability to set flags sensitive to simulated logic levels. These flags can be used like an oscilloscope sweep trigger to start printout action or to printout when a specified condition occurs. Normally, thirty channels of output are displayed (listed) in a multi-column fashion. When the number of requested outputs exceeds thirty, the program automatically goes to a single column format and sixty output signals can be accommodated. If sixty is exceeded, there is automatic switching to a tabular format.

The size of a design description is limited by the amount of computer memory available, of course; but because each signal string is equivalenced to the same memory location, relatively large designs can be accommodated. Fifty memory locations are used for each signal string (electrical node). For most circuits this results in a module count of approximately one-third the number of module pins, or expressed in another way, a 1000 gate network will require about 50,000 storage positions.

Two other simulators have been developed at NDRE, and their integration into a design project is worthy of mention. A register transfer language (RTL) simulator and microprocessor (μP) system simulator were written. Both simulator programs were specifically for aiding in the design of a μP developed at the Establishment. The RTL simulator was written explicitly to test the operation code set of the μP after it had been fully simulated at a gate level by the LOGSIM program. Different instructions (for example, the hardware multiply and divide) were exercised to insure correct operation. After the architecture of the μP was fixed, a higher level simulator was designed which effectively simulates the μP as a component in a system. This program, MICPROC, and the μP component (a FORTRAN subroutine) is used to develop systems in which the μP is used (e.g., a radar control system). On a Control Data Corporation Cyber-74 computer system, simulation ratio for MICPROC is 70:1.

The μP itself is rather interesting. Design objectives were most heavily influenced by the high speeds required by the applications for which the μP was intended. For example, some specifications include:

250 nsec instruction cycle time
75 instructions
16 bit word length
memory up to 64K
hardware multiply and divide
optional index register

The unit consists of four TTL logic LSI modules which were designed at NDRE. The μP is available as a commercial product (by ACUS, Oslo) together with an assembler and a high level language compiler (written in SIMULA). The assembler is in FORTRAN and is running on a Cyber-74, a Univac 1108, and IBM 360-70, and a Honeywell 6000. The μP is currently being incorporated in several NDRE projects as well as being used by the Norwegian Research Council and SAAB, Sweden, in the Viggen fighter.

The other effort at NDRE in computer aids for electronic design has been the development of a wire-list program based on the standard wire-wrap cards and bin system in use at the Establishment. The wirelist program is operational on a Kongsberg Vapenfabrikk SM3 computer, and the program is rather conventional in that module, or card, positions are first specified and then signal strings are specified. The program computes the end coordinates for every wire and groups the wires according to length but does no optimization of wiring path. Very little design information is provided as output by the program.

At present, printed circuit boards are laid out manually and then digitized. They are limited to two-sided boards with plated-though holes; although they anticipate going to multi-layer boards soon. At present though, no program development for multilayer boards is planned.

They have a few network analysis programs operational on their Cyber-74 (CIRCUS and ECAP are two programs available), but these are used very little. The design methods have been moving very rapidly away from discrete component designs to digital designs using LSI logic modules. There will probably be no CAD group set up at NDRE, but rather program developments will continue to be done by interested individuals. The Norwegian Council for Industrial Research (NCIR) does have a project in which the CAD effort is being coordinated in Norwegian industry by means of a committee which meets on a regular basis. NCIR has a small number of people and funding and is taking early steps towards developing and exchanging CAD programs.

ELEKTRONIKCENTRALEN - HØRSHOLM, DENMARK

Elektronikcentralen (Danish Research Center for Applied Electronics) is an independent non-profit organization under the auspices of the Danish Academy of Technical Sciences and was established in 1966 by the fusion of three electronics-oriented research institutes that date back some 30 years. Funding is both from the Danish Scientifc and Technical Research Council and from contract project work on an individual and multi-client basis. The staff numbers about 80, of whom approximately 30 to 35 are graduate electronic engineers. The main areas that the Center is engaged in are: systems engineering and circuit design, electro-magnetic noise and interference engineering, reliability studies and environmental testing, and component and materials technology and development.

The purpose of a recent visit was to assess the Center's use of computers in engineering design. My contact for the visit was Mr. P. Stangerup, who is principally involved with the development of programs for computer-aided design of analog circuits at the Center. The computing resources at the Center take two forms--via a rather recently acquired Digital Equipment Corporation PDP-11 minicomputer and via a telephone link to the Copenhagen-based GE Mark I timesharing service. To date, most program development has been in BASIC on the Ge system, but currently the programs are being rewritten in FORTRAN and transferred to the PDP-11 computer. Stangerup has developed several small linear analysis programs for filter design and amplifier response calculations. One of the more interesting recent programs he has developed is one that uses y- and s-parameters as the basis for the mathematical models for transistors. This work is reported in AGARD Conference Proceedings No. 130 on Computer Aided Design for Electronic Circuits, Lyngby, Denmark, 21-27 May 1973 ("Linear Transistor Models in HF Network Analysis. Adaptation Between Measurements and Analysis by Computers," by P. Stangerup, p. 10-1 to 10-22).

Another very interesting program Stangerup has recently worked with has concerned the thermal design of satellite NiCd batteries for the European Space Research Organization. From a modeling of the electrical, physical (dimensional), and heat transfer properties, Stangerup calculates the temperature profiles as a function of electrical load and time. A resistor-capacitor network analog is used in which the cross-sectional area is modeled by a mesh of resistors and capacitors. With the program, battery failure modes and reliability have been analyzed, and several potential design weaknesses have been uncovered and design modifications suggested.

The use of computer-aided engineering design at the Center has involved mostly small-signal linear network analysis programs. The success in the use of these programs has come about because of their application to well-defined problems and to problems of immediate concern. To date, they have not used any computer aids in the design or fabrication of the digital system they build. It was surprising to see that all of their digital system backpanels were being wired entirely by hand and without any aids from the computer such as wire-lists, signal cross-reference lists, parts lists, etc. because this has been one area where there has been a demonstrated economic payoff.

COMPUTER-AIDED CIRCUIT ANALYSIS AT THE TECHNICAL UNIVERSITY OF DENMARK

Computer-aided circuit analysis has been an active research area in the Laboratory of Circuit Theory, Technical University of Denmark (DTH), Lyngby, Denmark, since 1963 when Prof. E. V. Sorensen developed a program for ac analysis of linear networks. Presently Prof. Erik Lindberg has the responsibility for analog circuit analysis program development. Both Sorensen and Lindberg were my hosts on a recent visit to the Institute of Circuit Theory and Telecommunication at the University. The Lyngby campus is a modern appearing attractive university located a short 15 minute train ride north of Copenhagen. There are approximately 3000 students, 600 scientific staff members, 140 post-graduate students and 700 assistants on the single campus at Lyngby.

Since 1969 special courses in computer-aided circuit analysis have been arranged as a postgraduate course in cooperation with private firms and engineering societies in Denmark. In addition each year such a course is offered as an optional graduate course within the Laboratory of Circuit Theory. Two circuit analysis programs (ANP3 and NAP2) are being used the heaviest, each over 1000 times per month, and have been added to the Lyngby IBM-370/165 monitor system due to their heavy use. Besides the ANP3 and NAP2 programs, users also have several analysis programs available that have been developed elsewhere. These programs include CORNAP, ECAP, ECAP II, GOSPEL, LEANS, LISA, NASAP, and SNAP plus ANP2 and NAP1--a very wide selection of programs indeed.

The first program developed by Sorensen in 1963 (ANP1) and its successor (ANP2) were based on the topological tree expansion method. These two programs, although excellent for teaching network topology theory, were too slow for analyzing networks of larger than modest size ($\gtrsim$15-20 nodes). Consequently, ANP3 (Analytical Network Program) was developed.

ANP3 is designed for the frequency analysis of active RLC single-input single-output circuits. The first version was coded in ALGOL IV for the Danish GIER computer, then recoded in ALGOL V for the RC4000 system, and finally in FORTRAN IV for first the IBM-360/75 computer and the now current IBM-370/165 system. ANP3 is based on a two-sets-of-eigenvalues approach. The circuit specified is transformed into an equivalent active RC network by gyrator simulation of all inductances, and the indefinite admittance matrix is formed. From this matrix the network transfer function is derived. An extension of the program finds the first and second order sensitivity functions and worst case network values.

The other analysis program in heavy use is the Nonlinear Analysis Program NAP2 similarly developed at DTH. At present the program performs a DC and Transient analysis of systems in which diodes, bipolar transistors, and field effect transistors are modeled by nonlinear built-in models. Nonlinearities can be specified by means of tables, built-in functions or FORTRAN subroutines. In addition the user is allowed to build his own multilevel nested subcircuit models. NAP2 is coded in FORTRAN IV and is based on a hybrid formulation of the network equations and on sparse matrix techniques. For nonlinear circuits the Newton-Raphson iteration method is followed by a variable-order, variable-step implicit integration scheme. Besides the dc operating point and large-signal time response, the following types of outputs are available: Any driving -point response or transfer function, auto-scaled tables and lineprinter plots, histograms of Fourier analysis, noise analysis and specified combinations of response.

In designing both the ANP3 and NAP2 programs, special attention has been given to making the programs very efficient. For example, an analysis by ANP3 of an equalizer circuit with 23 nodes and 47 elements took 1.66 seconds of IBM-370/165 time. An analysis (DC and TR) by NAP2 of a 741

op-amplifier (19 transistors, 13 resistors, 1 capacitor and 3 sources) required 38.20 seconds of computer time.

Both of the analysis programs represent well-designed and extensively debugged systems. They are both available for a handling charge only, and the authors are ready to discuss problems concerning the implementation on other computers.

I also visited the Laboratory for Pulse and Digital Techniques while at DTH and talked to Prof. Ole Lading concerning the Laboratory's use of computer aids in digital design. In the 1960's they had a layout-simulator program running on a Danish GIER computer, but solution times were very long (12 hours or more for the layout of a 32 integrated circuit board) and the programs were never used very much. In the past couple of years a different approach has been taken for layout. An interactive scheme has been developed using a Tektronix 4012 storage tube display connected to a Texas Instrument TI-960A minicomputer which is, in turn, coupled to a RC4000 multi-programming system. Via a keyboard input, stored patterns and language, they are able to place and route a printed circuit board. Post processing by the RC4000 computer produces documentation and control paper tapes for layout and drilling. They next plan to add automatic routing using a modified algorithm for the initial layout. Following that, they anticipate developing a logic simulator based on a functional description. Lading and the staff and students working with him are developing computer aids in support of a research computer being designed and built in the Laboratory. The programming tasks are aimed at real problems, and they appear to be taking a well-thought out approach to software development.

CUSTOM LSI SEMICONDUCTOR DESIGN IN SWEDEN

The major producers of large scale integrated (LSI) semiconductor circuits have progressively moved towards large-volume quantities and standard product lines. Consequently it has been increasingly more difficult to obtain custom LSI designs for low-volume special applications. Thus, it was interesting to find a company, HAFO in Vällingby, Sweden, which is offering a custom metal-oxide semiconductor (MOS) LSI design service.

HAFO (Instituet för Halvledarforsking AB, i.e., The Institute of Semiconductor Research Inc.), after being a purely research and development company since its foundation in 1954, announced in 1969 that it was to become a producing company with the manufacturing of thick film circuits and electro-optic components. In 1972, under licence from RCA, a production capability in MOS processing was established. Sweden, which up to 1972 had been completely dependent on foreign semiconductors manufacturers, now not only has its own, but one offering a custom service - a service difficult to obtain nowadays.

The basis for successful MOS LSI design is a computer-aided design (CAD) system. Mr. Helge Berg joined HAFO in 1969 and has been in charge of the CAD development and of the circuit design. About 15 engineers are engaged in MOS circuit design and two to four in CAD software development. The heart of the CAD system is a Digital Equipment Corporation (DEC) PDP-15 computer system with 56 K word corestore, floating point hardware processor and two 260 K word DEC disks plus various peripherals (magnetic tapes, graphical display, printer, etc.).

Running on this computer system (24 hours a day, seven days a week) are several CAD programs, the most important being:

1) dc and transient nonlinear network analysis
2) sequential and combinatorial logic simulator
3) MOS artwork layout
4) MOS layout rules check

By means of the dc and transient analysis programs, the nonlinear behavior of MOS transistor cells can be studied in terms of impurity concentrations, oxide thickness, diffusion profiles, dimensions, temperature, etc., for single transistors. The transient behavior for MOS and bipolar integrated circuits for circuit sizes up to 100 network nodes, can also be obtained. In this case the active device models are nonlinear four-pole models. A state-space analysis is used together with a variable-step integration method. Emphasis has been placed on convenient input and output provisions as is the case for similar programs elsewhere.

To complement the design, the simulation of the logic behavior is achieved with a program having basic building blocks of AND, OR, NAND, NOR gates and provisions for grouping these blocks into subcircuits (flip-flops, adders, etc.), to any number of levels. The limit for the program is 600 gates which is rather restrictive for MOS designs which typically may contain 2000 gates and are heading towards 10,000 gates on a chip.

The MOS artwork layout relies on a simple high level language in which the geometrical dimensions of rectangles and polygons are specified. Patterns may be stored and later recalled, and the usual provisions for grouping, rotating, mirroring and dimensioning exist. Berg stated that although they have the Redac interactive MOS layout system, they have found that the language approach using plotter output and a batch system has been more successful. They have been doing about ten designs per year in this way. They do use the Redac software for printed circuit board layout. About 100 two-layer boards are designed per year using this system.

Berg said their biggest current problem is the lack of computer time for the number of designs they are doing. For the future he hopes to replace the PDP-15 with the more powerful PDP-10 computer. In terms of software development, he has been looking at automatic placement and routing, as these operations presently require the most design time.

Berg and his group have developed, in the past five years, a rather simple and straightforward but comprehensive set of CAD programs for MOS design and layout. They rely on manual intervention and translation between steps, contrary to that of most other systems that use a data base to bridge operations. They have concentrated on CMOS and PMOS but are presently extending their efforts to include integrated injection logic. As the only semiconductor design and fabrication facility in Sweden, HAFO is building an important service for their country's electronics industry and they are doing it well.

The remainder of Waldo Magnuson's comprehensive report will be coming to you in Vol. 6, Number 2 of the SIGDA Newsletter.

- Editor

RECENT PUBLICATIONS.

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Distributed Computing in Engineering Design Processes (F.A. Hess and D.K. Egel).
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Yours sincerely,

JWB/bp

J.W. Bandler
Professor of Electrical Engineering
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	10	Fault Mechanisms and Fault Tolerant Design	3
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NEWS RELEASE

The Sixth International Symposium on Multiple-valued Logic will be held at Utah State University, Logan, Utah, during May 25-28, 1976. The Symposium will feature tutorial, invited and research papers as well as panel and informal discussions. Invited speakers include Dr. G.J. Massey, Y.H. Pao, and L.A. Zadeh.

Engineering, logical, mathematical and philosophical aspects of multiple-valued logic and its applications as well as related areas will be covered in the Symposium. The Symposium is co-sponsored by the IEEE Co puter Society, ACM, The Office of Naval Research and Utah State University.

After the Symposium, there will be sightseeing tours in the national parks during the Memorial Day weekend.

"Since the technology has moved into MSI and LSI areas, we are facing the pin limitation problems," said Dr. Stephen Su, the Symposium Chairman. "For the same amount of information transfer, multiple-valued logic allows us to use less pins. Furthermore, the concept of multi-valued logic has recently been found to have applications in many areas such as design of digital systems, software, artificial intelligence, etc. As a result, increasing interest and attention have been given to this area."

Everyone is invited to attend the Symposium. The deadline for submitting abstracts to the Chairman is April 15, 1976. Further information can be obtained from Dr. Su in the Electrical Engineering Department, Utah State University, Logan, Utah 84322. Telephone number is (801)-752-4100 extension 7806.

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