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SIGDA NEWSLETTER

SPECIAL INTEREST GROUP ON DESIGN AUTOMATION

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Contents:

SIGDA

ACM Special Interest Group on Design Automation

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MEMBERSHIP

SIGDA dues are $3.00 for ACM members and $5.00 for non-ACM members. Checks should be made payable to the ACM and may be mailed to the SIGDA Secretary/Treasurer listed at left, or to SIGDA, ACM Headquarters, 1133 Avenue of Americas, New York, N.Y. 10036. Please enclose your preferred mailing address and ACM Number (if ACM member).

SIG/SIC ACTIVITIES

1) Informal technical meetings at NCC.
2) Formal meeting during National ACM meeting + DA Workshop.
3) Joint sponsorship of annual Design Automation Workshop.
4) Quarterly newsletter.
5) Panel and/or technical sessions at other National meetings.

FIELD OF INTEREST OF SIGDA MEMBERS

Theoretic, analytic, and heuristic methods for:

1) performing design tasks,
2) assisting in design tasks,
3) optimizing designs through the use of computer techniques, algorithms and programs to:

1) facilitate communications between designers and design tasks,
2) provide design documentation,
3) evaluate design through simulation,
4) control manufacturing processes.

CHAIRMAN'S MESSAGE

CHARLES W. ROSE

As I write this, my first of eight (8) "Chairman's Messages," SIGDA has a steadily increasing membership of nearly 500, a healthy bank balance, and is sponsoring an active technical program. When one considers that just a little more than 4 years ago, SIGDA faced dissolution for lack of interest, the change is remarkable. This change is the result of extremely hard work on the part of Chuck Radke, his officers, and board of directors during that period. I would like to take this opportunity to thank Chuck and his team on behalf of the entire membership of SIGDA for their inspired leadership and dedication.

SIGDA held a spirited business meeting at the DA Conference in June. Principal items of discussion were broadening the technical and membership basis of SIGDA, possible workshop and technical session topics, and means of encouraging contributions to the Newsletter.

We are in the process of assigning committee responsibilities and recruiting a new Board of Directors. I am happy to announce that Bill Van Cleemput currently of the University of Waterloo (soon to be at Stanford) has agreed to head up our membership efforts. He and Vice Chairperson Judith Brinsfield will work together in the area of foreign contacts and members.

Judith has also agreed to work with me in broadening the technical scope of SIGDA. Rob Smith, who has done a superb job as editor of the Newsletter, will also continue. The Newsletter does need your support also, however; Rob has a number of ideas for new features which he'll be writing about soon.

By the time you read this, the Joint-Waterloo Workshop will be history. We hope that it was but the first of several joint ventures with other SIG's/SIC's which will foster technology exchange and exposure to new ideas and techniques.

If you see a need for such a program, either as a workshop or conference session, please contact either Judith Brinsfield or me and we will try to work something out.

Speaking of conference sessions, don't forget the SIGDA session at ACM-75 in October. It will focus on "Human Factors Engineering Issues in Design Automation Systems."

Finally, Judith, Luther and I thank you for your support and hope that you will help us to continue to move SIGDA ahead in the next two years.

C. W. Rose

FROM THE EDITOR

Several outstanding contributions make this an unusual issue. Hopefully, its bulk will restore the confidence of those readers who thought the June issue was a bit thin. The first two papers were to have appeared in the Proceedings of the 12th Design Automation Workshop, but missed the publication deadline due to international mail delays. The third paper has been in existence for about two years, but apparently isn't very well known. Its refreshingly open style and practical orientation should be of interest to those of you who are in the PCB routing business. The bad news for routing people comes in the paper by James Lynch, who sheds some light on the inherent difficulties of PCB layout.

I've included a short note with a challenge for those who might care to relax with a Steiner tree some evening: I hope to publish in future issues some of the correspondence received in response to the Steiner tree remarks.

If you find this issue to be worthwhile, there are at least two ways you can help. First, send me material for future issues. Working papers, informal notes, student papers, conference rejections (unless they're awful!), suggestions for reprints, and similar material are all welcome. How about a list of recent publications in design automation by authors in your organization? [I will do so if at least two others send in lists for publication.]

We have also noticed that many design automation people do not belong to SIGDA. Encourage such people to join (its cheap) and contribute to the Newsletter (become famous -- or infamous).

In closing, please note that many of the names and addresses on the inside cover have changed (including mine):

NOTE ADDRESS CHANGES!

Rob Smith

COMPUTER AIDED PLANT LAYOUT DESIGN

F. Ciaffi

FIAT - DIREZIONE CENTRALE RICERCA
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Torino, Italy

INTRODUCTION

Plant layout is of fundamental importance for the arrangement and allocation of internal plant-areas an essential and frequent operation for large industrial installations.
The traditional work method involves:

- the physical positioning of machine shapes on a board representing the rough map of the factory;
- the reproduction on paper and the completion of the detailed map.

A first step towards the design automation has been completed with the development of a computer-aided drafting system which has been fully operational in the production environment since June '74.
The main features of the system are:

- dedicated hardware [1]: the Design Centre is composed of a medium sized computer linked to a storage C.R.T. and to an intelligent terminal with refresh C.R.T., a digitizer and a high-speed precision plotter;
- highly specialized software for the Data Base [2]: it performs archive and data management, memory virtualization, drawing structuring; future enlargements of the Data Base are taken into account;
- rich set of application and utility programs for the designers, draftsmen, Data Base manager and operators of the Centre;
- wide use of the graphic interaction as the best means of dialogue between the designer and the computer.

The second step, now in a phase of detailed specification, concerns the development of C.A.D. techniques optimizing equipment allocation and area planning.
This paper first illustrates the nature of the plant layout problem with a description of the conventional approach followed in the design offices of FIAT's Automobile Group.
Then some introductory notes are given referring to FIAT's background in C.A.D. activities and to the configuration of the hardware-software system on which the Plant Layout programs run. A Data Base description follows illustrating the wide set of managed entities and their relationships. The Data Base is presented as the nucleus of the overall system. More detail is given to the main phases related to the layout design: the maintenance of the graphic libraries performed by draftsmen through both on-line and off-line programs, and the actual layout activity performed by the designer interactively.
The paper closes with a description of the current developments: an increasing availability of computer access by means of several remote graphic terminals, and the integration of the interactive program with algorithms automatically performing portions of the conceptual design work.

CONVENTIONAL APPROACH TO THE PLANT LAYOUT DESIGN

The purpose of a plant layout design is to find the best arrangement of the production equipment in a given space. When the design activity is performed in a manual way it is entirely based on the experience of a few persons and on a quantity of data that the designer himself must collect. The following data is considered by the designer: drawings of the building in which the layout is to be developed; characteristics of that building concerning clearances, maximum allowable loads, location of supporting columns, service installations (steam, water, gas, compressed air, electric power, waste conduits); production process description; and finally machinery and auxiliary equipments with their patterns, dimensions, weights, inputs and outputs.
Sometimes the designer himself goes to the plant to obtain data on actual location of machinery, obstructions, feeding points, conveyors, storage areas, etc. He may also make reference to previous solutions for similar work arrangements through search and study of the old drawings stored in traditional paper archives.
There are four major phases of work.
The first is the preparation of a rough schematic drawing to be used for a preliminary study of the layout.
On the basis of the first rough study, a second phase is started to prepare a wooden panel with the tracing of mesh areas over which, subsequently, work areas will be defined. In the meantime two-dimensional shapes of machinery and furniture are cut from cardboard.
The third phase is the actual design phase: the patterns are placed, by repeated trials, on the work areas. Several tentative solutions of the layout are achieved, presented and discussed with the interested people in order to arrive at the final solution to be implemented. Each solution seeks the best arrangement with various criteria of safety, comfort for machine operators, greater efficiency in the routing and handling of materials, ease in isolating hazardous processes, and

proper use of existing space and service equipment already installed.
The last phase consists of transferring the location and shape of each physical element that has been entered in the design to the map, and providing all auxiliary information for each element such as labels, numbers, dimensions, tables, etc. Copies of the drawings are sent to the various users (other designers, workshop heads) and to the archives. Any feedback from the users must be considered and may cause iterations through some phases of the design process.

C.A.D. WITH INTERACTIVE GRAPHICS AT FIAT

The background of the Plant Layout Design System consists of the experience gained in several years of studies, tests and implementations in the field of interactive graphics for C.A.D.. The hardware used ranges from the UNIVAC 1557/1558 System, through various Tektronix storage tube terminals up to the ADAGE Advanced Graphic Terminals. The following computer facilities were used: UNIVAC 1106/1108, DIGITAL PDP-11, DIGITAL PDP-15. Home-built software includes base and service software. Application software has been developed mainly in the areas of curve and surface fitting (for car bodies and die design) of mechanical drafting and of electrical schematic layout[3].
Minor implementations include: interactive storage-retrival of technical data, a program for turbine blade design, and an interactive and graphic version of a transfer machine simulator.
The first experiments emphasized two very important facts. Firts, that good system performance may be obtained only on dedicated computer facilities (or dedicated to technical services only). Second, that a very effective graphic interaction needs some special hardware features such as a high density of lines on the screen, a wide set of interaction facilities, all handled by a processor in a fast way, and a wide screen surface.
As far as the software is concerned our prior experience in the development of an electrical schematic layout system revealed the important role played by the Data Base in an integrated design system. The Data Base for this system, which was the largest interactive application at FIAT before the Plant Layout design tool, included software for virtual memory facility and complex structure handling.
Both systems are run on the "Interactive Design Centre" hardware configuration which is described in the next section.

THE "INTERACTIVE DESIGN CENTRE"

The following description reflects the concepts currently utilized in the 1st generation FIAT's Interactive Design Centres. The details refer to the particular configuration on which the Plant Layout System is running.
The Interactive Design Centre is based on two processors linked with a parallel high speed line (50 k words/sec).
The main processor is a DIGITAL PDP-15, 48 k words (18 bits), with 3 diskpack units (10 Mw each), two compatible magnetic tape units and such peripherals as a line printer, a card reader, and a Tektronix T4002A graphic terminal.
The special purpose graphic processor is an ADAGE AGT/130, 32 k words (30 bits), driving a large, round, flat surface screen, and some devices for the interaction: a tablet with pen, an alphanumeric keyboard, a set of 16 function switches and a set of six potentiometers.
The work load is distributed as follows: the PDP-15 executes the application programs, manages the Data Base and supplies the ADAGE (which has no mass memory resource) with the overlays of programs running on it; the ADAGE performs two types of activities: the management of the structured display list and the execution of the operators for the graphic interaction.
There are some general purpose software modules, which run on this hardware and may be considered an integral part of the system concept; they are: most of the graphic interaction operators, the management of a generalized display list, the communication software and a package to virtualize the memory (which helps in implementing special Data Bases for technical purpose with very effective response times).
Compatible graphic operators exists to work on the Tektronix T4002A storage tube terminal.
The Interactive Design Centre typically offers a plotting service. The plotting facility for Plant Layout consists of a XYNETICS 1100 Drafting Table driven off-line by a PDP-11 which interprets the information written on a magnetic tape by the PDP-15 interpreting the drawing structures.

THE DATA BASE FOR THE PLANT LAYOUT SYSTEM

The Data Base is the structured archive containing all the information related to the Plant Layout design activity. The Data Base software performs the mass-memory and virtual-memory management, the data assignment to various entity types, the maintenance of hierarchical and non-hierarchical links between all the types of entities, the assignment of codes and identifying names to the entities.
The description of the Data Base is itself a description of the nucleus of the Plant Layout System. All the programs make use of it, by reading and writing on it, during all the activities they perform: the library-building programs use the structuring and archiving capabilities; the layout program makes also library references; the plotting programs follow directives recorded on a drawing structure and, of course, interprets library references and contents; the programs for the system manager allow him to list the Data Base directories and contents, to modify them and to widen the limits initially defined.
The information contained in the Data Base is organized in two main categories, Administrative and Graphic. The first category is used as an access to the graphic category. See Fig. 1.
The Administrative entities are: the FIAT Divisions, the factories of a Division, the buildings of a factory, the workshops of a factory, the classification labels of machines, equipment, installations, and the drawings.
Each Administrative entity is principally classified with a code and a name. It is linked to higher and lower level entities and to the related graphic entities, if existing.
The Graphic entities are: the shapes of machinery, equipment, auxiliary tools, furniture, the symbols for supply connections, the shapes of fixed elements on the building (mainly the pillars), the detailed plans of the buildings and the technological maps of work areas. The graphic entities are grouped by type, and stored into "libraries". They

contain all the information useful to their graphic representation and are subjected to continuous updating and expansion. Such information is, in turn, subdivided in elementary blocks, to allow speedy, efficient, non-redundant operations such as modifications, additions, deletions.
Two examples follow to describe some relations between the entities.
Example 1:when the designer starts, he types the workshop number. From this number the Division, the factory and the building are identified. The Data Base opens the library of the machine shapes and the library of the drawings, related to that factory, and the library of the work areas related to that building.
Example 2: typically there are more samples of the same machinery which have the same shape, but different labels. The Data Base records only one graphic shape and creates the proper links with the administrative labels. When the designer calls for one label, he gets from the library a copy of the machine shape.
A list of the maximum number of allowable entries follows (the limits to which an expansion is possible are in parentheses):
Divisions: 9 (15)
Factories in each Division: 9 (30)
Buildings in each Division: 30
Workshops in each Factory: 99 (120)
Labels: 30000 (no virtual limits)
Machine Shapes in each Factory: 5000 (7000)
Plans for each Building: 4000 (7000)
Work Areas in each Building: 4000 (9000)
Layout Drawings: 5000 (no virtual limits).
The recording needs for those entities easily exceed millions of computer words. Magnetic disk packs provide the necessary physical storage with short access times. An estimate indicates that one disk pack will contain all the machine libraries, buildings, work areas and drawings of one Division for two to three years of activity. The libraries of the work areas are the main cause of increasing storage requirements.
The magnetic tapes provide the space needed to store the less recent studies. They are interfaced, in a transparent way, by the Data Base software. If the designer asks to have an old drawing on the screen (both for a simple examination or for extracting useful subsets), the Data Base asks the operator to mount the proper tape. The drawing structure and the work area structures will be fetched from this tape and the only difference, from the user's viewpoint,is a longer wait time.

THE MAINTENANCE OF THE LIBRARIES

During the layout design process it is assumed that all the shapes of machinery, auxiliary equipment and buildings needed to develop a layout are available from the libraries. This means that the activity of preparing graphic shapes is separated from the design activity. Time and resources have been allocated for the maintenance of the libraries and most of the programs are devoted to this important activity. Some of them are exclusively used by the Data Base manager. Their function is to initialize new entities, mainly in the administrative sets, to perform inter-factory transfers, to make dumps and patches into the libraries, to list the library contents with different orders, to save-restore the libraries on the mass-storage devices and to enlarge the limits initially set at certain values. Five programs are used by the library draftsmen, four for machinery shapes description and one for buildings description.

Machinery shapes

For the machinery shapes description there are interactive programs and non-interactive programs. The common purpose is to allow the loading of the structure of the shapes. The shape structure (maintained by a subset of the Data Base software) is a set of data cells properly linked between them and to a library index. The header of a shape structure is a cell pointing to some rings of cells as illustrated in Fig. 2. There are graphic-type rings (G-rings), whose cells contain graphic information, and instance-type rings, (I-rings),whose cells contain reference to library items.
The most important graphic information is the set of lines describing the machine form. In the overall system a graphic form is described in a unique way - a set of blocks (arcs or polygons) with their own attributes (line width and line type) and coordinates. A coordinate is stored in integer form, each bit representing one centimeter.
The first G-ring of a shape structure contains the so-called "Simple Graphic Form" (S.G.F.), as opposed to the "Complex Graphic Form" (C.G.F.), contained in the second G-ring. The S.G.F. is used for the drawings shown on the screens because all the graphics terminals with refresh C.R.T. have a limit on the number of lines drawn, either for the display list limited area in the refresh memory, or for the flicker arising when a complex image is not completely refreshed in the proper time period. The library draftsmen must draw the S.G.F. with the minimum amount of lines useful to acknowledge the shape and his special points, if any (inputs, outputs, workplace).
The needs of a more detailed drawing, as required by the users of the final layout, are satisfied with the C.G.F.. The C.G.F.,considered only by the plotting programs, may be composed of many more lines than the S.G.F., though no special limit exists for both of them, and both share the same internal structure.
Each cell of the third G-ring describes a shaded area and contains the coordinates of a closed path and the parameters of the shading (the coordinates of three points giving the angle of the lines and the distance between the lines).
The cell in the fourth G-ring contains the identification label description. The only purpose of this description is to assign the area where the label must be written. The true label contents is assigned when the shape is called (through one of the identifiers) to be used in a layout.
The fifth G-ring is made of cells for description labels. Each cell has alphanumeric contents, the area assignment (as previously described) and the parameters for the characters (height and width).
The sixth G-ring contains (in up to 4 cells) a list of all the identification labels of the physical machines having that shape in common.
There is only one I-ring for the instances of symbols representing the supply connections for the machinery. These symbols are drawn with the same critera explained above,and are stored into a "common library". Other common libraries refer to the pillars (shapes to be used in the building struc-

ture), to the furniture and to the machinery not pertaining to any factory.
The non-interactive programs accept input on punched cards or on punched tape produced by a digitizer, and allow the creation of new entities. A simple language is used through which it is possible to describe the various items of the structure. The cards allow a full precision and require less input hardware.
The digitizer is a very helpful tool when big drawings of complex machines are available.
The interactive programs allow both the creation of new entities and the modification of the existing ones, directly on the screen of a graphic terminal.
One program runs on the Tektronix 4002A storage tube terminal. The keyboard is used for alphanumeric and functional input and the joystick (combined with the cross on the screen) for geometrical input. The screen is the obvious soft output However a hardcopy output unit, directly linked and controlled by the terminal, is also available. The rectangular screen is divided into two areas - a square on the left for the drawing, and a vertical strip on the right for messages, menus and coordinate values.
The program structure is hierarchical. The various levels of activity, library selection, general and special activity selection, are reached by menu. There are some phases such as drawing, writing, and moving shapes which are performed by the "operators". The main operators are the graphic operator, the "instance" operator and the "edit" operator. The graphic operator allows the user to work on a graphic form, structured as previously explained, by adding, deleting, modifying each information block. In the case of new shapes the operator begins to work on the empty entity. The operations are performed by keying in some characters, with the cross positioned in the meaningful positions. Among the facilities offered to the users are: grid and subgrids, drawing area enlargement up to a 2.6 Km square; coordinate reading; loading of coordinates by cross, or by keying in the values, or with reference to some other point; zooming of a portion of the drawing area to full screen; and refreshing of the actual image at any time.
The "instance" operator allows the user to work on the set of instances of symbols (in the I-ring). Those symbols may be added (called from the library by number), moved, rotated, duplicated, set in a row and/or equally spaced, deleted, simply by keying in some characters with the cross properly positioned.
The "edit" operator allows the user to work on sets of labels of the same category. In this case, on the identification label or, independently, on the description labels.
Labels may be created or deleted. During the creation both contents and parameters may be given - parameters by means of the "control" keys.
Another interactive program runs on the Adage Graphic Terminal. Functional input is performed through 16 pushbuttons and two foot-pedals. The geometric input is performed through a tablet with the cross as a feedback on the screen. An analog-type, general purpose input is given by means of six potentiometers. The alphanumeric keyboard completes the set of tools for the interaction.
The structure is similar to the interactive program which uses the Tektronix terminal.
The main differences are due to the performances of the operators sometimes by virtue of the updating in real time of the image, sometimes due to an overall major complexity. For example, the graphic operator offers many facilities to the user such as the sub-image definition an recall, and the real-time display of measures, angles, coordinates. The "instance" operator offers a better feedback in moving and rotating the instances of symbols. The "edit" operator is very complete for string editing and gives effective feedback for the real area occupied on the drawing, depending on the character size and string rotation.

Buildings

For the building shapes description there is an interactive program running on the Tektronix terminal. Almost all the description phases can be performed through interaction, but the draftsmen are strongly advised to follow a suggested procedure. They must describe the building shape with the non-interactive language, the same used for machinery shapes, enriched with the descriptors of the grids of pillars. The card input allows the user to write the exact coordinates, as taken from engineering drawings of the building, and to easily create many pillar instances, with exact positions and identifiers. An homogeneous matrix (or grid) of pillars is described by three cards: the reference to the common library of pillars and rotation, the characteristics in the X-direction and in the Y-direction (coordinates of the extremes and rules for creating the identifiers in each direction).
The card deck is read in through a menu command of the interactive program. The draftsmen can immediately check the correctness of the input and is free to perform interactive changes though the suggested way is to change the input deck.
Each building (the single administrative entity) may have more graphic versions. In the Data Base these versions are identified as the old ones, the one valid at the current time, and the "studies" (with the modifications or the enlargements of that building not yet existing). The layout designer can select the version on which he intends to develop his design, even if the layout program initially displays the "current" version of the building.

Library references

For both machinery and building shapes there are plotting programs which generate sets of drawings. Those drawings are used together with the administrative printed lists as a reference during the designer's work.

THE PLANT LAYOUT DESIGN ACTIVITY

Forewords

When the designer sits at the Adage Graphics Terminal (see Fig. 3) to develop a Layout, he works on the basis of data such as: a set of technical information, the machining cycles (coming from the methods offices), the knowledge of similar solutions developed in the past and his own experience.
The computer system may support him in two ways: it is able to retrieve and show to him the old solutions, and it helps him to quickly develop some new solutions. Each trial may be materialized

in tens of minutes. After a few hours the designer can bring out some preliminary drawings and discuss them whith his colleagues. This is true if all the needed machine shapes are already in the libraries. However, even if they are not in the libraries (as in completely new studies), it is easy to use the shape of similar machines. The library drawings and the library lists will help during the search, and the program permits calls from the libraries "by similarity".
The design evolves through multiple iterations both in the traditional and in the computer-aided method (the same will be true with the automated programs now in a specification phase). With the second method each iteration is shorter and easier and the times between iterations are substantially reduced. Thus, the designer's efforts may be exclusively devoted to the real design problems.

The interactive program

The Layout program is divided into phases to be performed in sequence.
The first phase introduces the activity. By means of the workshop number keyed in by the designer, the proper libraries are identified and retrieved from the library-pack. Together with the common libraries, they are stored in the virtual area for fast access. In the second phase the designer is asked to specify a drawing number if the activity refers to an existing drawing. Otherwise the activity is assumed to be a new one. In the first case the drawing characteristics are read in the drawing archive. The area information is used to show the contents with the same display parameters in effect at the last "store". In the second case some subphases follow to specify the area and the contents of the new study. First, the region in the building where the study is to be developed must be specified. This is done through the pillar identifier or with reference to the displayed image. A default specification exactly frames the drawing contents on the screen. Another specification refers to the building version. The program automatically displays the current version (see Fig. 4), but the designer can select a different one from a list of versions. The last specification must provide the drawing contents. It may be performed through one or more selections in a list of the work areas defined in that building, or by entering a date to obtain the real configuration at that date (the actual building and the actual work areas). For this purpose the work areas, as well as the buildings, are stored with the study, activity and end-of-activity dates. A null contents selection implies that the designer will start a completely new study, with no reference to an existing situation.
At the end of this second phase the main drawing characteristics are known-the drawing area is mapped on the screen, the proper building portion is displayed and the work areas are shown with their outlines and names (see Fig. 5).
The third phase is the most complex one. It is hierarchically structured and starts from the general type of activity related to the work area choice. For definition of a new work area, for modification or for deletion of a work area existing on the screen. In the first two cases the layout activity for a work area is started. The work area has been selected as a unit logically complete from the designer's view point (see Fig. 6).

It is also the best dimensioned entity to be handled on a screen; typically it ranges from fifty to a few hundred machines. The work area has the structure of all the other graphic entities-header cell with pointers to rings of graphic cells and pointers to rings of instance cells. Five G-rings describe the outline of the area, the identifier label, the generic lines drawn directly in the work area, the description labels and the shaded areas (as for the machinery shapes) belonging to the work area. Five I-rings describe the machinery instances, the furniture instances and the networks of special lines, by means of three entity types: the node instances, the logical links between nodes, and the graphic path of each logical link.
All the items of this structure are created, modified, deleted only through graphic interaction. By menu selection the needed operators are called. The graphic and the "edit" operators have already been described. Two others are very important for the layout activity-a complex "instance" operator and a "network" operator. The instance op. is used to position the machinery shapes. The main functions are: to call shapes from the library by keying in the identifiers, to delete one or more of them, to handle them in several ways. The machinery shapes are normally displayed with the Simple Graphic Form (S.G.F.) and the identification label. Each time a shape is called in from the library or picked for handling, the description labels and the supply connection symbols are also displayed. All the machine shape details may be added, deleted, modified both in the contents and in the relative position, excepting the identification number.
The complete shape as a whole, in turn, may be moved and rotated. More complete shapes may be jointly moved, rotated, set in a row and/or equally spaced. Repeated duplications are allowed only on the furniture shapes, or on the machinery shapes called from the libraries as "similar".
In each phase of the operation some aids are available to the designer: grids, immediate magnifications of sub-areas (see Figs. 7 and 8), real-time update of selected distances (between points or from a point to a line) of coordinates (either absolute, with reference to the building origin, or relative to a newly set origin) and absolute angles.
The "network" operator is used to describe lines with special graphic forms, typically the network of transporters and the conveyors superimposed on the work areas.
Any number of networks may be described on the work area. Each of them is made of any number of nodes and connections between them, and has such attributes as path type and turn-radius.
Nodes and connections may be easily created, deleted and modified. The designer must only describe the paths (through a subset of the graphic operator) while the detailed drawing is performed by the plotting program.
Other facilities are available to simplify interaction on a given layout.
Entire sub-areas may be submitted to the same operation. The designer encloses sub-areas within a line and all the internal items of any type are uniformly translated, or deleted. Each work area may be repeatedly divided in two work areas. Alternatively the contents of a work area may be added to the current work area.

The fourth phase is reached when the designer, after some iterations on the phases 2 and 3, wants to momentarily or permanently interrupt his activity on the current drawing and proceed to the plotting specifications. First, he selects the sheet format and the scale. An outline of the sheet, or sheets, needed to contain all the drawing area is displayed on the screen so that the designer can move it for the best framing of the contents. Then, he fills the drawing identification form to be plotted on the lower right side of sheet. After these operations the drawing structure is complete. It may be stored as an official drawing or as a new study. If it has been retrieved from an archive of studies it may also directly replace the old one, or assume a new version number. In all cases the given identification number is written on the screen for the designer's reference.

The plotted output

A Layout plotting program accepts as input one or more drawing identifiers. For each drawing and for each sheet, the drawing structure is analyzed. Each item is retrieved from the libraries and expanded to elementary plot commands (see Fig. 9). There are some predefined detail levels selected by the designer to satisfy different requirements.For example a drawing may be plotted for intermediate test, for reference or for production needs.
For the lower detail level some items are plotted in their simpler form, others are not considered at all. Other requirements refer to the drawing accuracy that is determined at plotting time through the use of one or more pens, ball-point or ink pens, and by setting different plotting speeds. In conclusion, the plotting time for a standard size sheet (59.4 x 84.1 cm) of average complexity ranges from a few minutes to a few tens of minutes.

CURRENT DEVELOPMENTS

Apart from a few easily implemented developments useful to conveyor designers and the factory plans draftsmen, there are two main developments that will improve the effectiveness of the overall system. The first one should satisfy the need of distributing the computer support to many design offices located in remote areas. The present hardware configuration can't easily manage more concurrent programs, and is not able to handle communications with remote stations. The solution comes with the use of a more powerful host computer with efficient communications and multiprogramming capabilities. A sharable Data Base will be an important characteristic of the new system.
Also the remote stations will evolve through more updated concepts such as local multiprogramming to share the resources during the design activity, local intelligence, and compatibility with both refresh and storage tube terminals.The remote stations will be tailored on the real needs of the offices, following the asserted philosophy of the FIAT's S.T.U. (Generalized remote station)[4].
The second development refers to a natural evolution of the application software. Today the designer's work is easier and faster, but no conceptual help comes from the computer. Two problems have been specified: to find the best layout solution with given criteria and to compare or evaluate many layout solutions. The first problem deals with such cases as the completely new layout with or without space constraints and the revised layout due to changes in flow processes or due to the introduction or removal of machinery. The proposed algorithms implie multiple iterations with the designer's intervention. The graphic interaction will increase the system performance to very high levels. A result will be immediately shown on the screen in a format very familiar to the designer. New suggestions and constraints will be easily introduced. The process will be restarted and an improved solution together with some parameters for evaluation will be submitted to the designer for a new iteration.
Much more information, such as worker space, overrun of moving members, individual buffers, maintenance accessibility, entry and exit points, must be inserted in the machinery libraries. Free rings have been reserved in the structure for this purpose. Original data such as machine to machine flow and transporter selection parameters must be given for each study. As a counterpart it is expected that a new study in which the outer conditions are fixed may be completed in a few hours time.

ACKNOWLEDGEMENTS

Many individuals contributed substantially to the system described in this paper. In particular the author would like to acknowledge the contribution of V.Fazi for his efforts in hardware integration, R.Marello for developing the Data Base, N.Todisco for programming the graphic terminal and G.Villani for assisting in user training.
The author would like to thank F.Plevna for his valuable assistance in specifying user oriented system characteristics and coordinating the activities during the system development.

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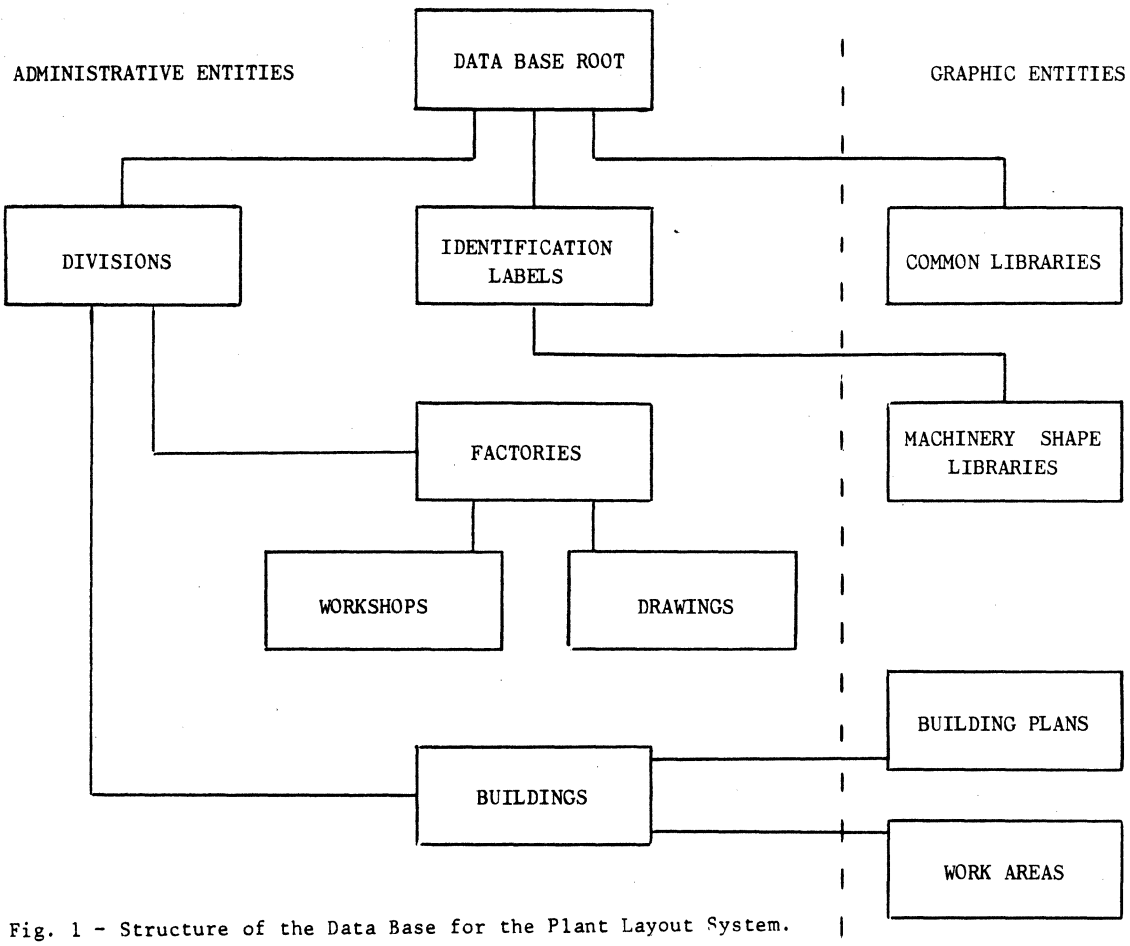

Fig. 1 - Structure of the Data Base for the Plant Layout System.

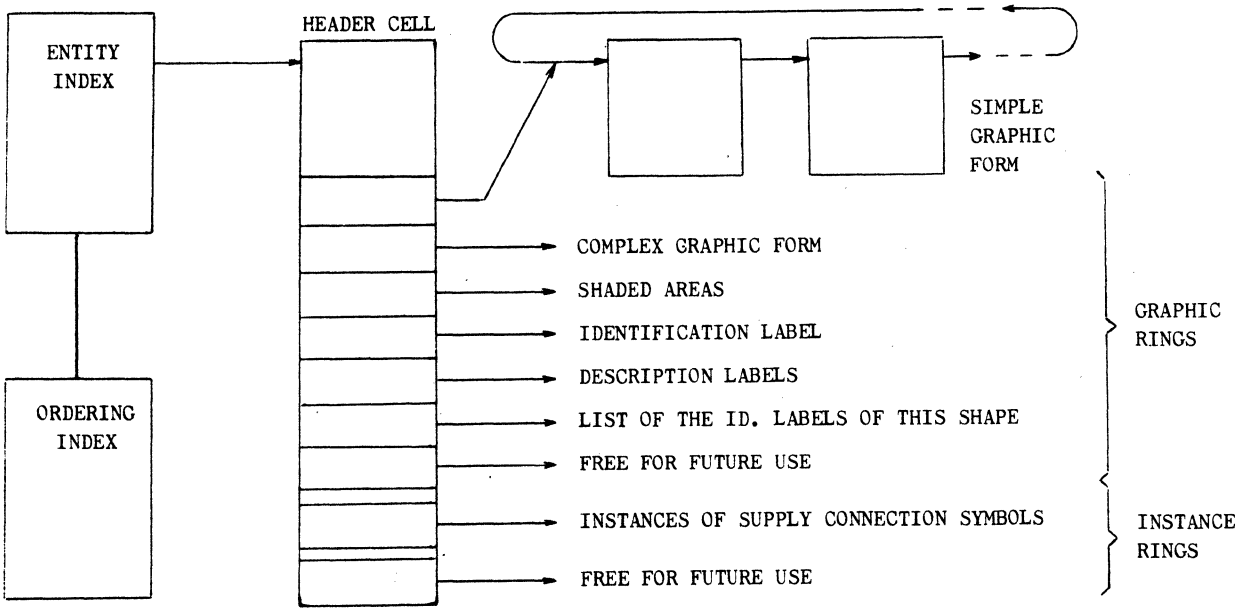

Fig. 2 - Structure of a machinery shape.

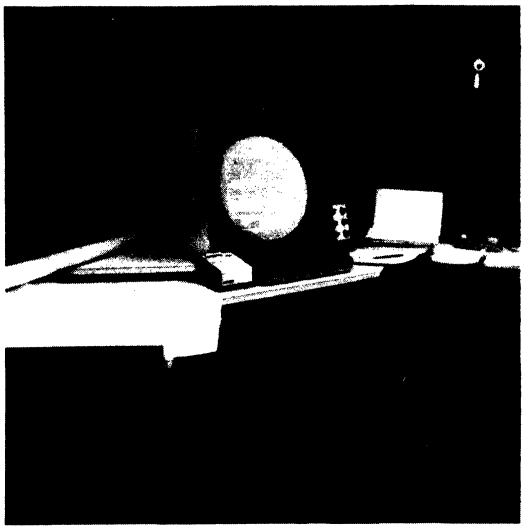

Fig. 3 - High performance graphic terminal.

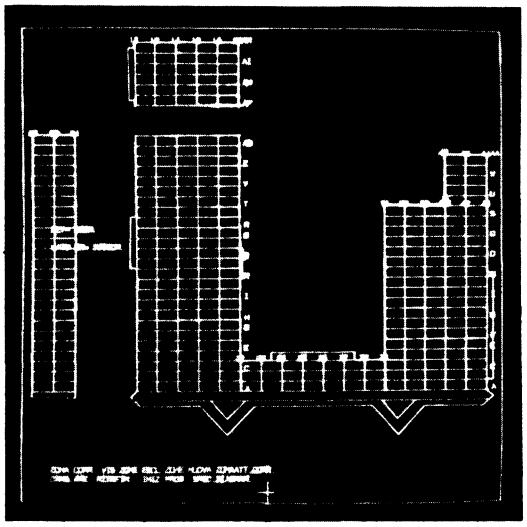

Fig. 4 - Overview of plant.

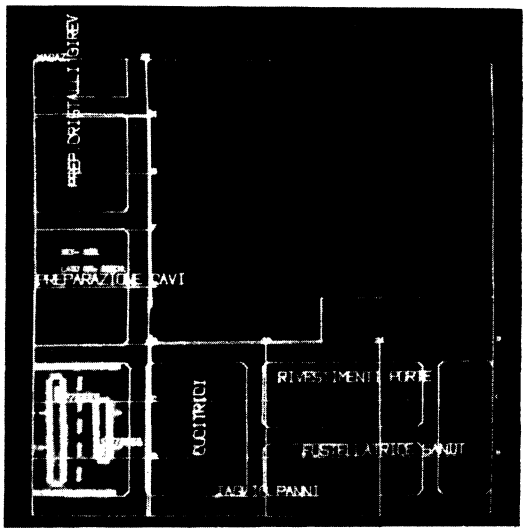

Fig. 5 - Partial layout of work areas.

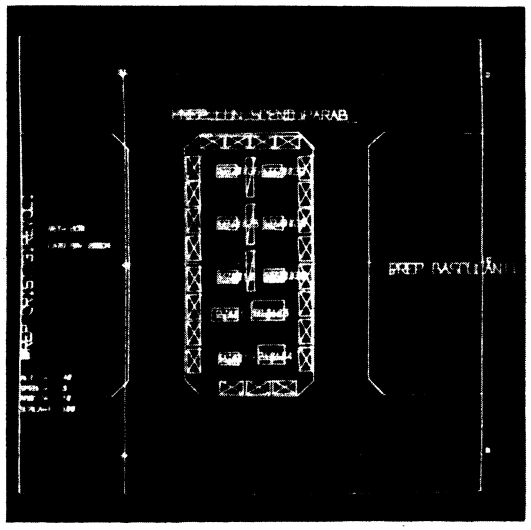

Fig. 6 - Layout of a work area.

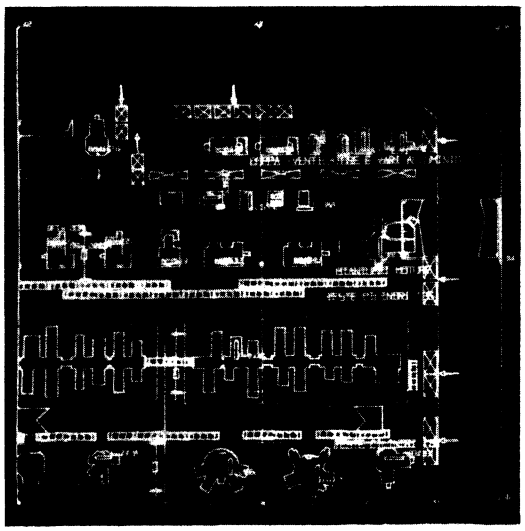

Fig. 7 - Detail of a work area.

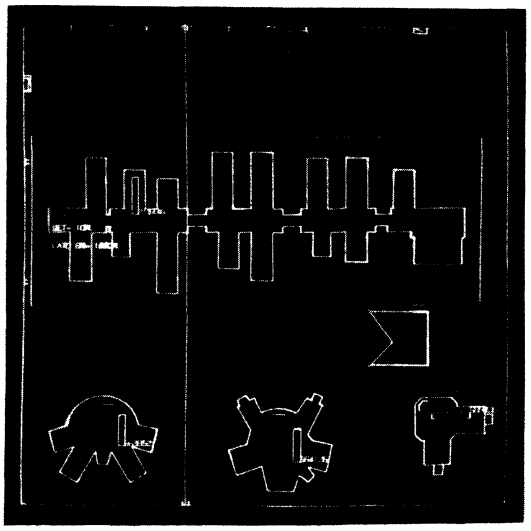

Fig. 8 - Detail of machines in a work area.

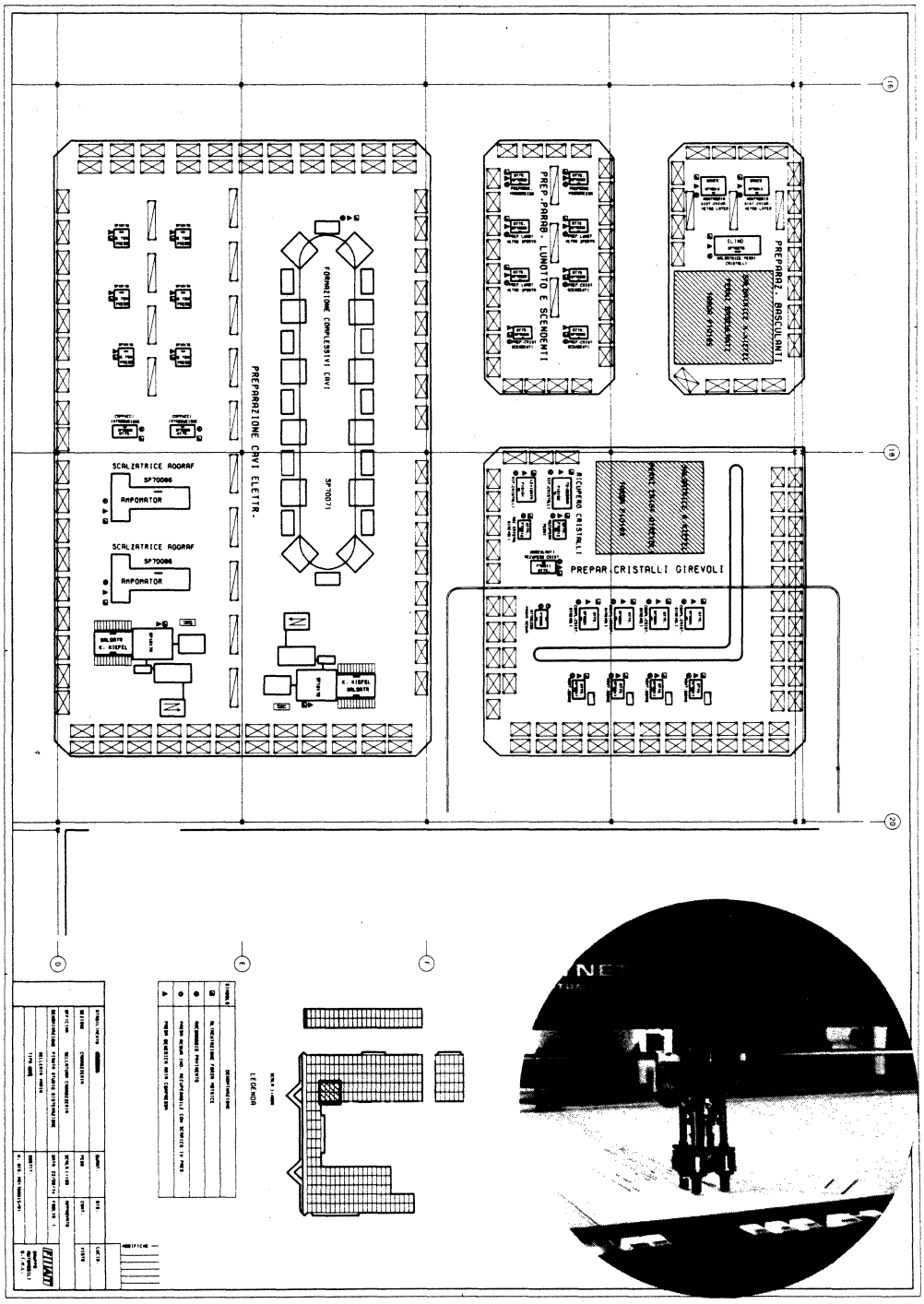

Fig. 9 - Example of final plant layout drawn by the high speed plotter.

SET OF PROGRAMS FOR AUTOMATED DIGITAL SYSTEMS DESIGN

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Current trend of a computer development is characterized especially by large changes on a field of technology, which offers new logical solutions of a computer design. To follow that trend is necessary to use a computer equipped by appropriate problem oriented software for verifying and realizing a new design. Getting out of that fact was some years ago in the Research Institute for Mathematical Machines in Prague started a long-termed plan called "Automation of Digital Systems Design". Nowadays is realized the first part of this plan, consisting of tasks of the technical design. In the area of a logical design was created the program system for coding and testing of microprograms used for computer EC 1021 and now it is generalized for other devices. In the area of a system design we begin to use a language for the multilevel description of a computer structure, followed by programs for computer description processing and simulation. In this paper is described a set of programs for the technical design and for the design of microprograms.

The program system for the design automation is based on a uniform definition of a circuit diagrams description. Information from such descriptions is processed and stored in a data base called the Master Information File (MIF). Except of the MIF are used during processing other files containing informations in a form of a catalogue, like descriptions of used logic and functional elements, constructions of PCBs and other components, diagnostic tests, drawings, rules of interconnecting etc.

The input for automated design programs is described by data oriented languages. There are used languages for description of functional circuit diagrams, logic diagrams, elements placing, constructions, routing of printed connections and wire routing, tests, interconnections of PCBs and as output languages are used operation codes for plotter and tester.

Amount of programs is represented by 2.5 MB core storage. Set of programs or individual program can be used also without data base MIF. In this case is omitted complex program for data base protection. In the MIF is stored the last state of a project but is also possible to regenerate any of previous states. Processing of a task is controlled by control cards into which is punched control language text. Input information for a task is a sequence of system control cards, sequence of control cards for automated design and input data of a task. By the set of programs are solved following tasks:

1) design of PCBs including components placement and assignment of logic elements to integrated circuits,

2) simulation of logic circuits on PCBs on a gate level,
3) test generation for PCBs,
4) making out the drawings of functional and logic diagrams,
5) placing of PCBs in cases,
6) interconnection of PCBs,
7) evaluation of assembly rules for PCBs interconnections,
8) compiling of microprograms into machine code including addressing of microinstructions,
9) microprogram simulation on a functional level.

The main point of an automated design is the data base MIF. This Master Information File contains informations about one designed device. Informations are obtained and used during logical and technical design. The MIF is organized as a sequence of records, each of ones corresponds to one contact in a device. In each record is stored a characteristic of a contact. Summary informations in the MIF contain complete informations about logical relations at a logic or functional level, about electrical interconnection, construction addresses of elements and construction nodes, characteristics of signals and connections, relations to drawings of diagrams and necessary information for the file maintenance. The MIF structure is created in such a way, that updating the file during machine design is possible. The MIF is maintened by special program, which also protects the file against destroying.

Other files can be devided into three groups. The first one consists of logic and functional elements, the second one of construction and technological data and the third one of output files like diagrams drawings and diagnostic tests.

Priority in program coding was given to FORTRAN for its simplicity and efficiency of a compiled program and for advantages offered by compiler during debugging the programs. For time or storage exacting tasks was used ASSEMBLER. Exceptionally was used COBOL and macrolanguage MLl. As output languages were used operation codes of plotters and tester. Input languages can be characterized in the following way, circuit diagram at any level is described by elements, logical, functional or components of a circuit, one by another. Each element description contains list of inputs, outputs, signals and type of element and its identifier.

Programs are draft in such a way, that is possible to change or correct partial results and so influence the whole solution. For these purposes was developed a set of languages, which allow to make such changes.

Set of programs for automated PCB design consists of four basic programs. By the simplest one is possible with use of a geometric figures library to create any figures and to convert them into graphic output language. Input data describes configuration of basic figures only and dynamically loaded figures. The program is used for IC design, for hybrid circuits design and in all cases, where the highest degree of universality is desired. Other two programs realize interconnections of geometric figures, which represented by electric components on a board. One of this programs accomplishes automatic interconnecting, the other one enables to make manually changes in automatic design or to influence the automatic solution. These programs are universal in that sense they are independent of PCB construction. Parameters of a PCB are limited only by a used main storage. The designed board can vary from 1 to 14 layers with any proportions, components and connectors. The last

program from this set performs besides the automatic interconnecting also assignment of logic elements to integrated circuits, placement ICs on a board and pin assignment. This set of programs allows to include other programs for coding different graphical output devices like plotters for drawing a PCB or numeric controlled drillers.

Diagnostic programs for PCB

Testing of a PCB is usually passing following four stages.

a) Test generation
b) Test correctness and completness verification
c) Creation a control program for a tester
d) Testing on a tester - and in case the tests fail follows fault location procedure.

Each of these stages may be realized in different ways, manually, on a computer or on an automatic test equipment (ATE). Processing is then rather itterative than sequential only.

Instead of developing a complicated ATE we prefered to use a computer for stages a) to c). This tasks were realized in reversial order starting from point c), creation a control program for tester, through correctness and completness verification to test generation.

Control program for tester is punched into paper tape or stored on a magnetic tape by program, which compiles a diagnostic language text and translates it into tester code.

Test verification is done by simulation program. This program creates from circuit description a model in main storage. In the case the model would be too large is possible to have a part of the model in the main storage and the rest on a disk. Tests are simulated on this model in an asynchronous way. Simulation program enables also simulate stuck faults. Results of fault simulation are processed in form of fault dictionaries used later in fault location procedures. Test generation is restricted on circuits without feed back loops or with single loops. Algorithm used in program is similar to D-algorithm.

Diagram drawing program

There is one program for drawing of functional as well as logic diagrams, where the type of diagram is given as a parameter. Another parameters are format of drawing (normalized formats in metrical system A3 and larger) and output device (line printer or different kinds of plotters).

Besides diagram description are used in this program another two files stored on a disk pack or on a magnetic tape. There are library of graphic images for each element used in a diagram and library of diagram formats. Graphic images of elements must correspond to current valid norms.

Diagram drawing program consists of five basic parts:

a) reading in and processing the input data (diagram description),
b) partitioning of diagrams into pages, following parts are done in a cycle for all pages,
c) placing of element images on a page,
d) interconnecting of elements,
e) output in the form appropriate to a chosen output device.

The parts a) to d) are independent on used output device and data transfer to part e) is done in a form of special language, which contains all means necessary for storing a graphical information.

OPTIMISING AUTOMATIC TRACKING OF MULTILAYER BOARDS

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SUMMARY

The paper commences with a brief but critical appreciation of some known automatic tracking techniques for multilayer printed circuit boards, viz. Maze-Running, Line-Search and Channel-Allocation. The purpose here is to bring out their inherent similarity and to propound their specific superiority under different combinations of controlling criteria dictated by technological constraints. Consideration is given to the prohibitive core and time requirement for a real life environment involving an approximately 500 x 500 track matrix associated with the request for orthogonally connecting about 2500 pin-pairs, on each board. The paper then proceeds to discuss in detail the evolution of an effective algorithm and list-structure capable of successfully handling this problem. Finally several side issues of major significance are introduced. The efficient pre-sorting of the order in which wires are submitted to the main algorithm has been found to make a significant contribution to the efficiency of the entire system. Profile analysis is developed as a technique for comparing the relative merits of various topological placements of the logic network. The importance of the basic board layout and its relation to the algorithm employed is stressed.

Acknowledgements

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1. INTRODUCTION

Design Automation is a discipline devoted to the utilisation of digital computers in the design process.

1.1 Background

At the Manchester factory of ICL, Design Automation techniques have been employed since 1958 in the field of the design, engineering and manufacture of large digital computers. The current suite of programs (known as SYSTEM 71) consists of 1.3 million instructions developed over the past 7 years, and represents a fairly large investment (ADSHEAD, 72). Three medium scale computers are employed six days a week (totalling over 400 hours). Each week up to 5000 jobs for 100 design engineers are processed, producing up to 1 million digits of NC tape and 500 master logic drawings. Designs for many types of computer system and technology are stored on over 4000 magnetic tapes. The design operations for any type of logic assembly follows the general pattern shown in Figure 1.

1.2 Computer Design Process

Basically the design process involves the decomposition of the planning specification into a system structure (Figure 2). The information explosion in the process may be from 10K characters of product specification into about 200 M characters of NC, production, test and maintenance information. DA efforts are primarily aimed at achieving increased scale, efficiency and economy in the processes of Synthesis, Partitioning, Checking, Placement, Tracking, Testing and Modification of large logical networks.

1.3 Tracking

The need for the automated tracking process increases as we move from wire wrap techniques to the sophistication of orthogonal interconnections automatically etched on multilayer printed circuit boards (Figure 3). As the number of interconnections increased to several thousands the need for automatic tracking becomes essential, especially when a design rate of 2 - 5 per week is required. The human sense of associative perception is no longer very helpful. The problems are so enormous in their sheer bulk that tracking of one multilayer board would require many man weeks of effort, without any guarantee of an acceptable solution. It is relevant to observe that the whole justification for major investment in a DA system probably rests on the existence of a good tracking algorithm and the subsequent generation of NC tapes. However, as the programs are Software Engineered into a reliable system used on a daily basis, the actual instructions in the algorithms represent less than 1 per cent of the total problem.

1.4 The Basic Problem

The process of "routing" is defined (AKERS, 72) as that of formally defining the precise conductor paths necessary to properly interconnect the elements of the computer. 4 main subdivisions have been identified (BRUER, 72), namely, wire list determination from the logic file; layering; ordering; and wire layout. The purpose of this paper is to endeavour to highlight some more of the problem areas and suggest the basic outlines of a successful approach, currently employed as an integral part of a live Design Automation system for Multilayer Boards.

1.5 Total Technology

It cannot be overemphasised that the design algorithms and the product must be developed together. This is particularly true in the case of the basic design of the multilayer board itself. Section 10 indicates some of the design parameters that must be considered when developing a successful interconnection technology.

2. DEFINITIONS

Routing: The process of determining the sequence in which the several points are to be interconnected.

Ordering: Sorting: The process of sequencing the order in which wires should be presented to the tracking process.

Layering: The process of allocating various wires to a particular plane in the multilayer board.

Tracking: The process of precise path determination for each wire.

Profile Analysis: A study of tracking density in an orthogonal direction for each channel.

Board Layout: The basic design of a board before tracks are added.

Plane: A layer containing either horizontal or vertical tracks. These coexist as plane-pairs.

Pins: A point on a board which forms either a source or target for a wire interconnection.

Through hole: (Via): A position on a board (other than a pin) which allows the union of X or Y tracks through a Z directed link.

Space: An area of a board which extends from one edge to the other and may be of any desired width.

Channel: One of the possible parallel lanes in which the tracks in a space may be laid.

Track: (Track Segment): A wholly horizontal or vertical section of a wire.

Wire: (Pin-Pair): The interconnection between 2 points consisting of one or more interlinked tracks.

Cross Over: A link between adjacent tracks in parallel channels implemented without using opposite plane.

Target Cross: The cross formed by the potential tracks surrounding a target pin.

Map: The core space or list structure devoted to defining the track on a plane pair.

Pin Block: The situation where all ways out of a pin are blocked by previous tracks.

Excess Length: The amount by which the actual tracked wire length differs from the minimum (Manhattan) length.

Handwire: A wire which cannot be tracked automatically.

Minimum Rectangle: The smallest rectangle that includes the source and target pins.

Bounding Rectangle: A larger rectangle bounding the channels which may be used to link a pin-pair.

Tracking Success: The ratio of the number of wires successfully tracked to the total number of wires requesting linkage. This is usually expressed as an average over many boards.

Channel Utilisation Co-efficient: The ratio of total track length to total channel length for each channel.

Track Density: The ratio of used track to total available channels for a whole board.

Profile Demand: The ratio of tracks attempting to cross a cross section to the total number of channels available.

3. REVIEW OF TRACKING TECHNIQUES

Historically there have been a number of approaches to the tracking problems.

3.1 Heuristics

Early tracking attempts were based on heuristic approaches e.g. look for one, two or three through-hole paths. In our experience these rarely achieved a Tracking Success greater than 70%.

3.2 Lee's Algorithm

Lee proposed a method that was exhaustive and could be made to find the best path between two points in a maze if one existed. (LEE, 61). Several variations (ACKERS, 67) have been incorporated and in 1966 the group developed a program to handle 1500 wires on a 40 x 40 cm board (Figure 4) with its own variation of data structure (Figure 6). The programs were used to produce a family of 200 platters and achieved a Tracking Success of about 95% in about 80 minutes of machine time. The program suffered from basic weaknesses:-

a. Large store for every matrix point (200,000 x 3 bits)
b. Large store for list of trial points (200,000 words of Drum Space)
c. Time-consuming back-tracking

3.3 Cellular Wiring

The group in 1968 independently developed a cellular storage approach similar to that reported (HITCHCOCK, 69). These programs are still running successfully for 15 x 20 cm macros containing 400 wires (Figure 5). The highly compressed data structure for each cell (Figure 7) fits into one computer word of 24 bits and tracking takes 1 minute of machine time as 3 paths are explored simultaneously with a variant of Lee's Algorithm. (In fact 10 solutions are generated in 10 minutes). Tracking success is 99.6%, averaged over a few thousand board designs. This tracking technique forms an essential component of a highly successful interconnection technology. Macro boards are totally designed at the rate of 6 per day.

3.4 Channel Assignment and other Techniques

Several other algorithms have been proposed (FISK, 67 and GINSBERG, 69), including the stepping aperture technique (LASS, 69). So far the group has not encountered design problems where these approaches appeared attractive. A Channel assignment technique that was developed separately assigns wires to spaces and then finally to channels in that space (HASHIMATO, 71). This method splits up wires into sets of wire segments free to move sideways within the boundaries if a given space and also from one space to another if overcrowded. Finally track segments are assigned without overlapping in a manner so as to minimise channel demand. The group developed a program on these lines which proved less successful on multilayer boards and came to the conclusion that the main potential for this technique lies in the LSI and hybrid micro-circuit fields.

3.5 Line Search

An inversion of Lee's approach was proposed (MIKAMI, 68) that involved storing track data in the form of track segments and searching for intersection line by line instead of point by point. This algorithm was very attractive from the point of view of core reduction, but does not reduce run time for difficult wires. An early prototype program (HEATH, 69) developed by the group confirmed this. A heuristic extension to this basic scheme (HIGHTOWER, 69) was based on the concept of "covers" and "escape points". The group independently developed and extended the line-search algorithm in an exhaustive manner in 1970. Currently 40 x 40 cm platters (Figure 9) containing 2500 wires are being tracked in around 10 minutes machine time with a tracking success of 98.5 per cent.
This paper aims mainly to discuss the various aspects of this approach.

4. CONSTRAINTS and OPTIONS IN TRACKING

4.1 Wire Listing (Routing)

In the group's environment of high speed ECL logic and matched transmission lines there is no question of employing Steiner nets to interconnect several pins. For this reason and in order to provide ability for modification, the transmission lines are routed in the logical sense while the logic file is being constructed and modified. The tracking problem begins then with the extraction from the logic file of wires (or pin-pairs) to be fitted into the board. The order in which these wires are sorted is highly critical to the success of the Algorithm and is further discussed in Section 7.

4.2 Constraints

There are a number of parameters that are usually fixed with the basic board layout and are not left as a dynamic option during the tracking process. However, it is good practice to construct the program such that all these parameters can be altered on a table look-up basis.

a. Size of the multilayer boards
b. Number of X-Y plane pairs
c. Distribution and spacing of track segments
d. Distribution and number of available through holes
e. Ability or otherwise to employ adjacent through holes
f. The use or otherwise of 45 degree lines
g. The number of ways out of a pin
h. The use or otherwise of crossovers
j. The degree of parallel tracks allowed (to minimise cross talk).

4.3 Optimisation Criteria

There are a number of features or goals (some of which are actually contradictory) which have to be balanced when establishing a tracking algorithm as a systems engineered program, viz.

a. Purpose built software for maximum speed and cost-effectiveness
b. Generalised (modular) system for flexibility to cope with fast changing techniques
c. Minimum computer run time (or design cost)
d. Maximum production yield (or min. production cost)
e. Minimum total track length (or circuit delay)
f. Minimum number of through holes
g. Minimum number of hand wires

In short, the programs should be capable of generating a reliable, cheap and modifiable design quickly and cheaply. In addition they must be capable of extracting wires from the Data Bases of different Projects and must generate output data in a controlled, reliable and reproducible form directly utilisable for controlling NC production machines.

4.4 Degrees of Freedom

In general if one allows more choices, or ways of meandering across or through the board (degress of freedom), then design is potentially eased but production is correspondingly complicated. Paradoxically increasing the degrees of freedom considerably slows down any exhaustive tracking algorithm and hence should be introduced with caution.

4.5 Layering

Some board layouts (or shortage of core), demand a preassignment of wires to individual planes of a multilayer board. (e.g. predominantly horizontal or predominantly vertical etc.,). The adoption of line-search techniques has rendered this process absolete as all maps may be held in core simultaneously.

4.6 Parallel Tracks

In high speed logic, parallel tracks are a potential source of cross-talk. Histograms of parallelism in designs tracked, showed a remarkably low incidence of this effect above a quarter wave length. However, the adoption of board designs with only 2 tracks per space immediately halves the voltage significance of this effect. Thus the group has so far been able to avoid the algorithmic complications of this problem.

4.7 Graphics or Manual Additions

In the large computer design environment, we have a high design volume and modification rate in proportion to the production volume and hence it is uneconomical to include graphical interaction to force in any handwires. For example there is a net increase of 33% in design costs to remove 2 handwires. All boards are designed to be simply modifyable and hence the 2 or so initial handwires can be simply soldered on the back. 60% of all boards designed on a totally automatic basis contain no handwires.

5. FEATURES OF THE ALGORITHM

There are a number of features in the algorithm developed, implemented and integrated in the DA system, that distinguish the group's approach (Figure 10) from that of Mikami or Hightower.

The basic algorithm is as follows:-

a. develop the primary trial lines (track possibilities) that leave each of the 2 pins
b. select the longer of these as the target cross. Store the source trial lines in the map list.
c. take each source trial line in turn and:-
d. take each point in turn and attempt an orthogonal radiation, i.e. develop further secondary trial lines. If this new line intersects the target cross then a path has been found, else store the trial line in the map list and continue with steps d and c.
e. if the list of trial lines becomes exhausted before intersection is achieved, then there is no possible path between the 2 points.

5.1 List Structure

The basic unit of storage is a track segment. This may be an existing track from a previous wire or a trial line during the search phase. All these segments are chained together in one common list structure (Figure 8) in a manner that allows dynamic expansion of work space and allows optimum analysis of track intersection or interference. The maps for all layers are mixed up in one common storage area. Trial lines are easily and rapidly created by chaining into the front of the list for each channel. They are deleted after each tracking attempt in one rapid garbage collection process. The choice of storage format for the trial line units allows rapid unpacking and generation of further trial lines without unduly hindering the back tracking operation after intersection has been achieved. An interesting feature is that if the number of layers is increased then the core store used actually decreases owing to the reduced use of through holes.

5.2 Blocked-Off Areas

All practical board designs contain regions that are unavailable for tracking. These arise from bolt holes drilled through the board, power connections or other surface irregularities. The unavailable track segments are blocked-off as dummy segments already utilised before commencement of any real tracking. As these blocks tend to be common to all layers, only one storage area is used and chained into the end of each map list.

5.3 Failures

A very significant single motivation arises from the understanding that it is better to optimise the algorithm around the near failures rather than the easy wires.

Consider some rather rough estimates:-

	No. of Vias	Percentage of total pin pairs	Percentage of total computer run time
Simple Cases	0-1	55%	10%
	2-3	25%	25%
Complex Cases	4-7	15%	30%
	8+	3%	15%
	Handwires	2%	20%

It is tempting to add heuristics or logical short cuts to speed up the majority of simple cases but the extra programming is entirely wasted on the difficult wires. Hence the whole philosophy is geared round the detection of reject cases, thereby both simplifying and speeding up the programs. Mikami advocated radiation from both Source and Target Pins simultaneously. It is better to determine a single Target Cross (the largest) and then radiate from the Source only.

5.4 Map Swapping

There are a number of advantages from holding all layers in store simultaneously. There is no need to pre-layer the wires and tracking is attempted on each map cyclically with increasing relaxation of excess length constraints (Figure 11). In this way each map ends up with a similar track density and a good balance is achieved between the tendency for the line search algorithm to find longer paths (excess length) with less through holes in preference to more direct tracks.

5.5 Software Engineering

A considerable degree of flexibility and modularity has been achieved to cater for varying board layouts. All programming is done with the aid of a segmented modular programming system employing macro generation and a low level assembly language. All track programs are used in 2 modes:-

a. Tentative Tracking where evidence of a solution is fed back to the logic engineer and

b. Production Tracking where a particular solution is selected and frozen in a controlled, safe and reproducible manner suitable for the generation and supply or production information.

The whole algorithm is thereby included in a totally integrated design system approach. Logic design processes are directly linked with production output via a common data base.

6. WIRE ORDERING

A key problem was the criteria for sorting the pin pairs prior to presenting them to the tracking algorithm. Clearly once a wire has been tracked it is a potential source of blockage to many subsequent wires. There are a number of general considerations, viz.

a. The length of wire. A short wire is less likely to block a long wire than vice versa. Paradoxically this approach ought to be inverted on electrical grounds, since a lot of short handwires (although more expensive to produce) will create less cross-talk problems than a few long handwires.

b. The area of minimum rectangle gives a measure of potential via availability.

c. The shape of the minimum rectangle. Meandering is more likely to be necessary in long thin rectangles.

d. Wires to critical regions of the board (e.g. edge pins).

e. Fast or critical signals should take priority over slow monitoring or handkey wires. It is rarely practical to expect logic engineers to indicate which are fast or slow signals, but certain information may sometimes be generated from the logic design process itself.

f. Local variations in track density can have a profound effect in causing pin blocks. Surprisingly a profile sorting order based on the probability of dense regions did not prove a great success.

For the large platters a heuristic function composed of the above variables was developed which was fairly simple to compute and still found very satisfactory in giving a high tracking success.

For the smaller macros ten or so different sorting functions combined with variations in bounding rectangles are tried. One function stands out as a clear best in 50% of the boards. However, there are many cases where each of the other functions is significantly better. It is possible for the handwire count to range from 0 to 10% depending on the choice of sorting function.

7. POST PROCESSING

The inner tracking algorithm must assume the standard design tolerances. However, after all wires have been tracked there usually remains considerable scope for improving the design to increase production yields.

a. Deletion of through holes: Any track segment, say in X plane, that does not in fact overlap any Y track segments may be implemented on the Y side of the plane thereby saving up to 2 through holes.

b. Track centering: If only one track segment occupies a channel it is implemented centrally thereby increasing track to pad spacing.

c. Track flipping: Track segments are further spread out by flipping them into adjacent vacant channels.

d. Track hooking: Tracks that lie totally under components are slightly extended (or hooked) such that they may be cut if necessary during modification.

All these above processes have to be used with discretion. The act of improving circuit etching and drilling yield can in fact cause problems for flow soldering or modification and may increase cross-talk.

8. PROFILE ANALYSIS

Tracking of large multilayer boards aimed at 100% tracking success is a relatively demanding process. A technique capable of quickly warning about low probability cases or comparing the trackability of various topological placements of the same logic network is usually most welcome. 'Profile Analysis' is basically an attempt to predict the orthogonal trackability of any multilayer board without actually attempting 'tracking'. (Figure 12)

Assuming predetermined design parameters and tracking algorithm, the two major factors influencing the tracking success may be identified as partitioning and placement.

8.1 Effects of Partitioning

Packing the maximum logic on any multilayer board is very attractive for reducing the number of boards and thereby reducing the total production and yields costs. But excessive packing usually increases track-demand (and therefore the channel utilisation coefficient) and may make complete tracking success impossible. Strictly the number of internal links (pin-pairs demanding tracking) will influence the tracking problem more than the actual amount of logic assigned to the board.

8.2 Effect of Placement

Placement has an even greater effect on the tracking success level. Poor placement can make the profile highly fluctuating by unevenly distributing track demands over various channels. It can also increase the track density by placing highly connected units farther apart and vice versa. The latter will actually lower the threshold packing density, upsetting the advantages of optimal partitioning.

8.3 Profile Analysis

The profile of a multilayer board looks at its channel utilisation from an orthogonal direction. The curve therefore is the join of all the points representing the channel occupancy at every channel on the plane.

Profile demand (say DYi) is the total of horizontal theoretical tracks requesting permission to cross the vertical channel (x=i). The X-Profile (Figure 13), will then be the curve joining all the points (i, DYi) on the graph.

The critical channel utilisation coefficient and therefore the track density (being the integral of either profile demand or channel utilisation over suitable range), will usually be a function of the design parameters and the efficiency of the tracking algorithm and will have to be determined statistically.

The following conclusions can be derived from profile analysis. (Figure 12)

a. If the minimal track density (integral of profile demand) exceeds the critical track density (integral of critical channel utilisation), the board certainly needs replacing or even re-partitioning.

b. If not so, but several local maxima cross the critical occupancy curve, replacement is indicated to improve tracking success.

c. Any placement which reduces the tracking density and/or the smoothness of profile (keeping it below the critical profile curve everywhere) is to be preferred.

9. DESIGN OF BOARD

As has been pointed out in previous sections of this paper, the tracking algorithm very much depends on the Basic Board Layout and vice versa. There are of course other factors that also affect the choice of board design such as automatic testing, assembly and monitoring, (LUTTMER, 68 and MARSH 70). However, the main tracking considerations are:-

a. The distribution of pins and vias

b. Access to edge pins

c. The handling of power distribution and power logic strap-offs

d. Ability to modify

e. The expected number of wires per pin, which varies with the type of logic

f. The expected average wire length

Within the above it is advisable to base the original estimates on random wiring (parabolic profile) and allow a 70% meander factor.

The final choice of layout could well be influenced by the design/production volume relationships since the objects of the algorithm are to balance problems of design with those of production.

10. ANALYSIS AND CONCLUSIONS

There are no universal requirements, constraints or criteria for optimising the orthogonal tracking problem.

These typical average figures will give some idea of the efficiency of the algorithm:-

Physical size of board	40 x 40 cm
Number of tracking layers	4
Number of channel rows	300 (not pin rows)
Number of channel columns	300 (not pin rows)
Number of potential vias	100K
Number of available vias	50K
Track density	70%
Number of wires	2000
Ratio of excess to minimum track length	10%
Number of vias used per wire	1.5
Percentage of hand wires	< 1.5%
Core (including all maps)	20K words (24 bits)
Time CPU per board	10 mins. 1905F (roughly equivalent to 360/50).

Extreme care should invariably be devoted to the systems development phase including the finer details of the algorithm and board design. In spite of the necessity of surviving the crushing pressures of the highly competitive modern technology and commerce demanding a system 'yesterday rather than tomorrow', the tracking suite was developed as a highly robust, sophisticated and integrated software system. And most significantly the emphasis was on 'Optimising the complex cases (which devour resources with very little to show) rather than the simple cases (for which virtually any algorithm or implementation would be good enough)'.

The main achievement is felt to be the actual implementation of a thoroughly integrated system capable of automatically extracting its essential information from the design automation logic files and ultimately providing complete information for driving the numerically controlled machines needed for production of these multilayer boards.

It is felt that the wire ordering and map swapping techniques correctly compliment each other.

Another relevant aspect of the system is the profile analysis, which not only provides a fairly quick and accurate estimate of the automatic trackability of any board (without actually tracking it - something which may be highly core and time demanding) but also points out strongly the areas on the board which are liable to produce handwires. This allows an off line interaction by the logic designer.

Over the past 7 years the group have advanced the local state of the art considerably in that current boards are designed several times more cheaply and faster and yet are also cheaper and easier to produce than before.

As we move closer towards employing LSI and hybrid microcircuits these techniques prove to be a sure foundation for exploiting the "technologies of tomorrow".

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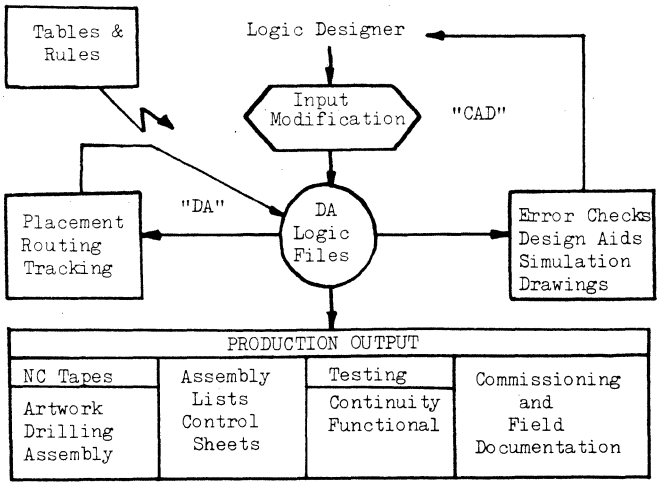

Figure 1. BASIC DESIGN SYSTEM FOR LOGIC SUB-ASSEMBLIES

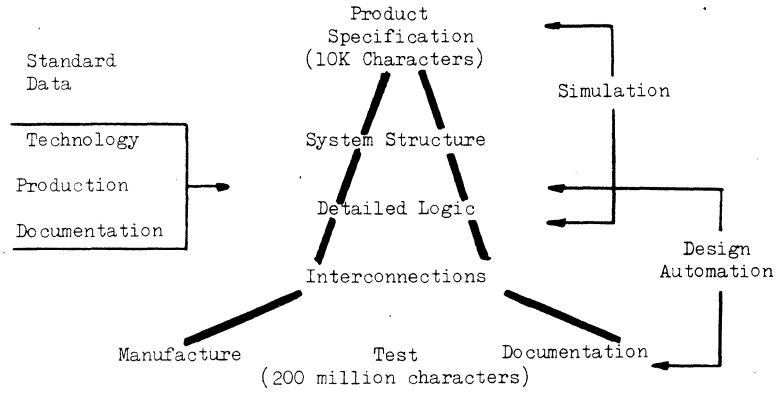

Figure 2. THE COMPUTER DESIGN PROCESS - EXPANSION

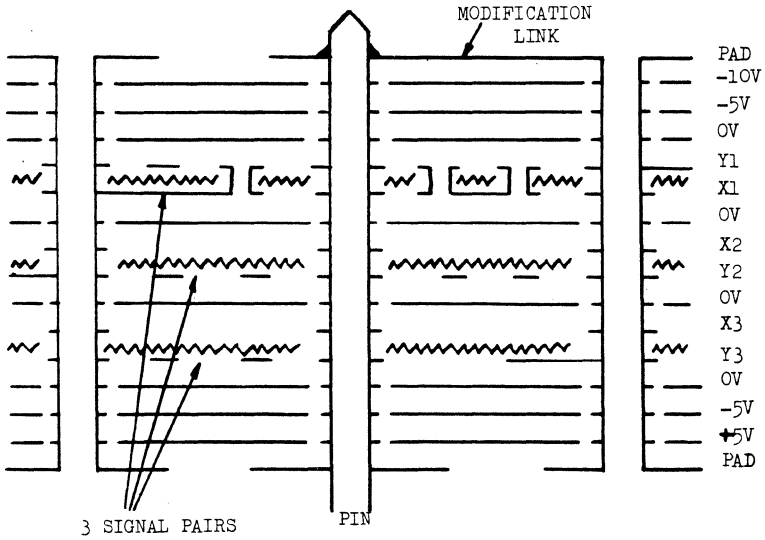

Figure 3. CROSS SECTION OF 16 LAYER PLATTER

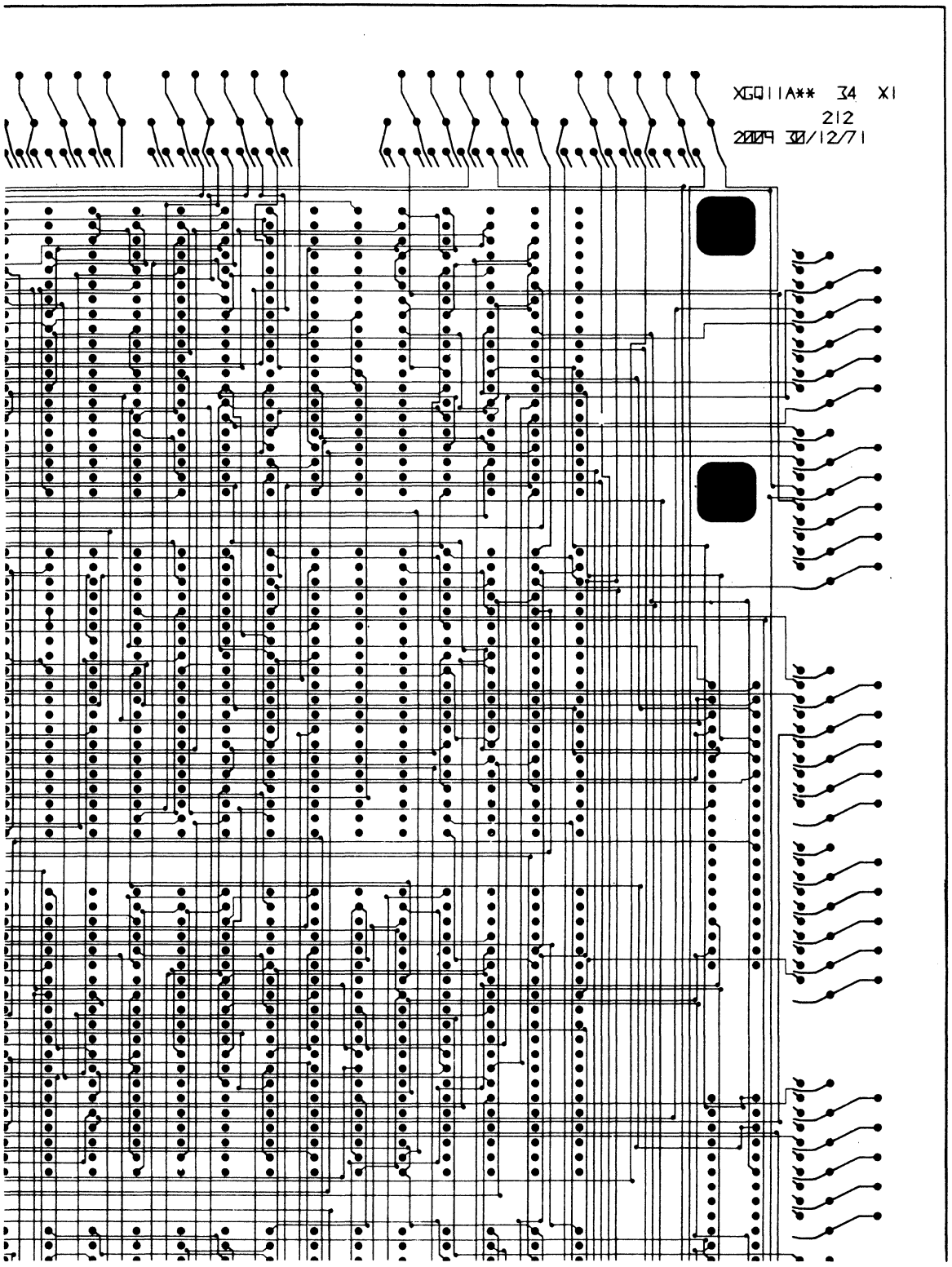

Figure 4. PART OF 1966 PLATTER - LEE'S ALGORITHM

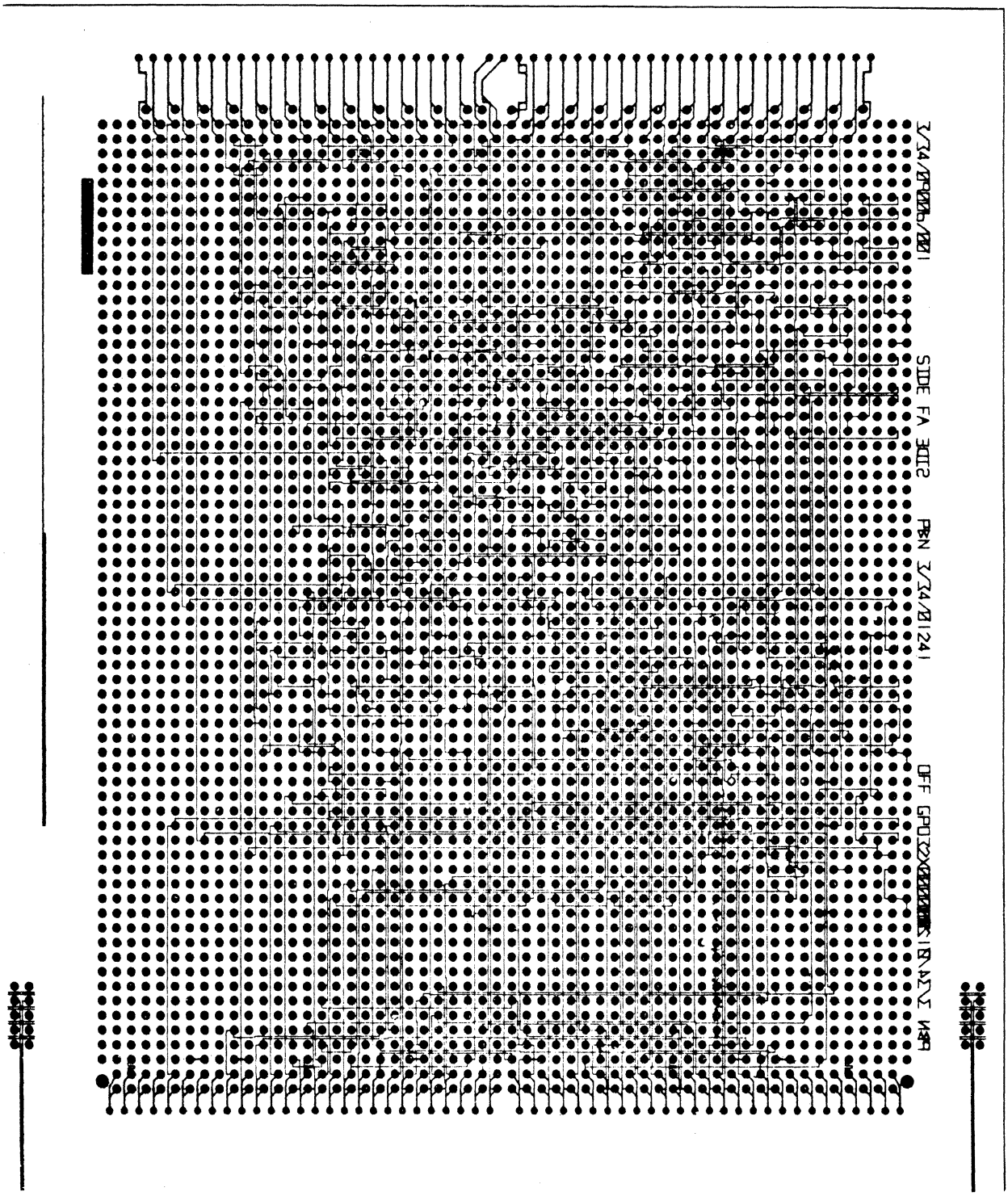

Figure 5. 1968 MACRO - CELLULAR LEE ALGORITHM

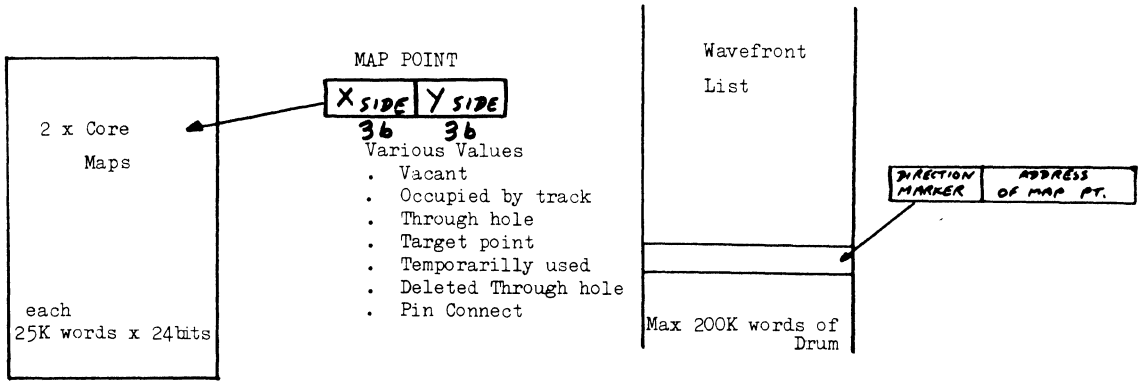

Figure 6. 1966 PLATTER DATA STRUCTURE - LEE'S ALGORITHM

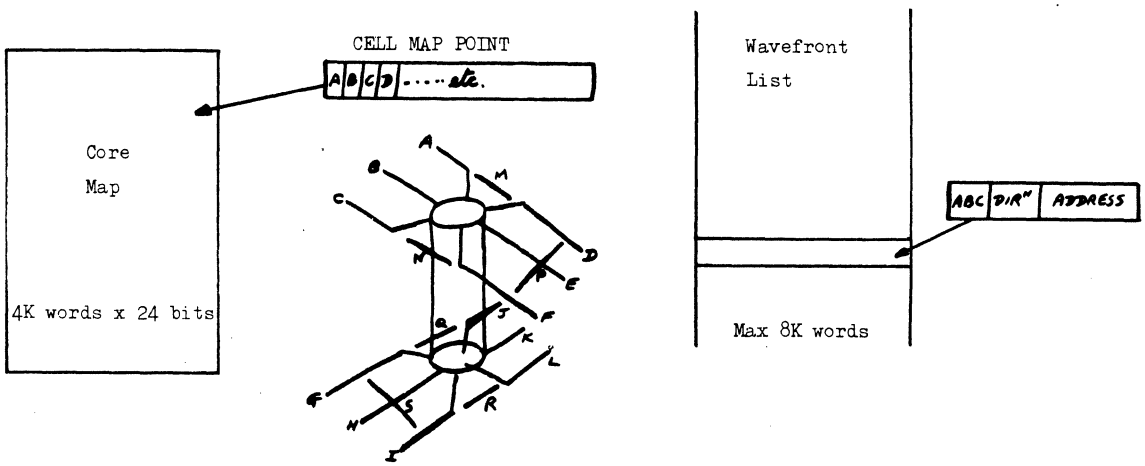

Figure 7. 1968 MACRO DATA STRUCTURE -- CELLULAR LEE ALGORITHM

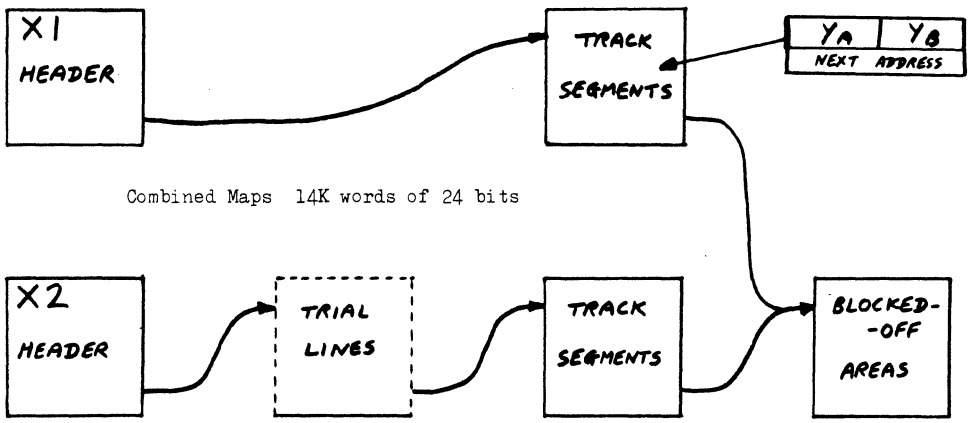

Figure 8. 1970 PLATTER LIST STRUCTURE - LINE SEARCH

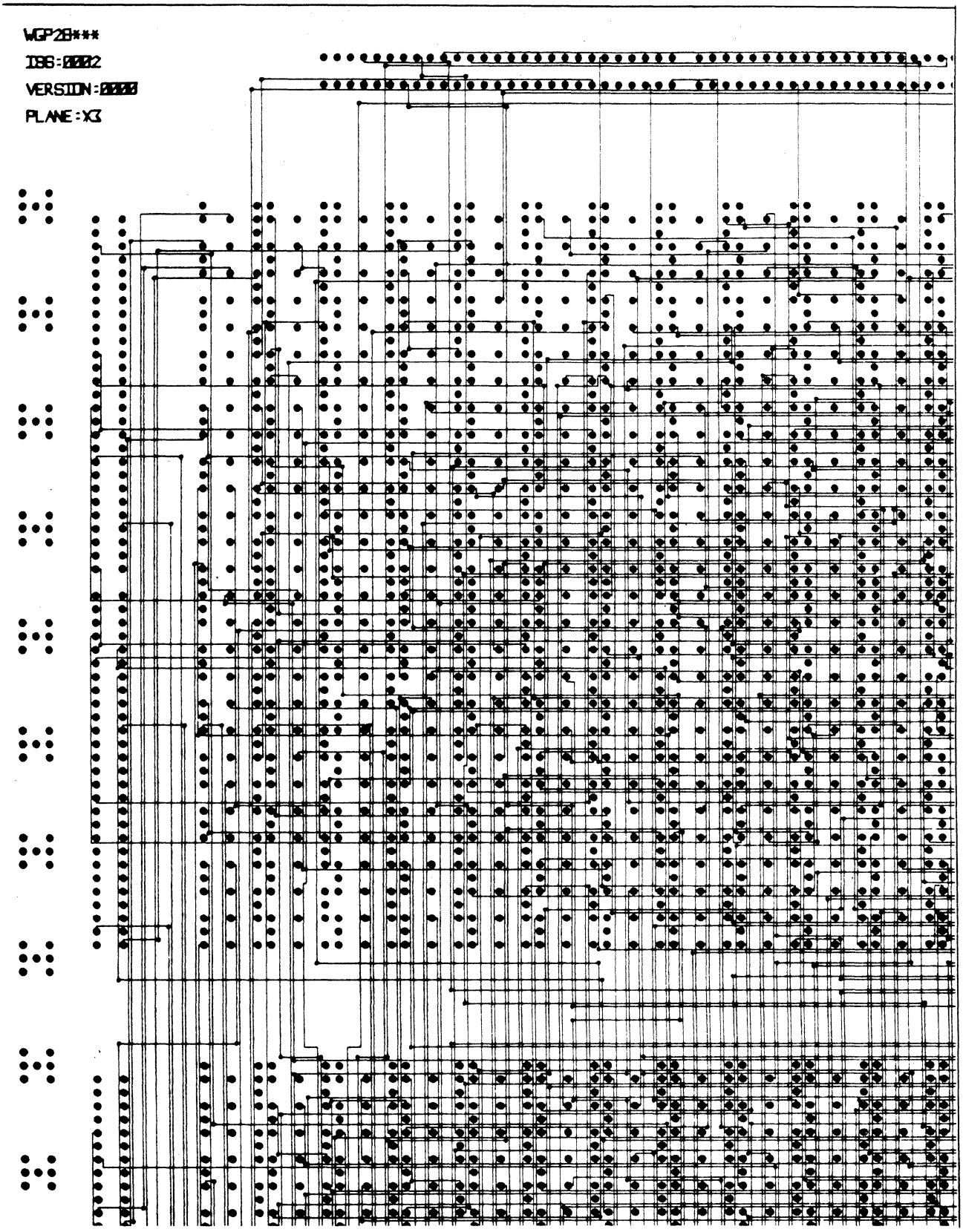

Figure 9. 1970 PLATTER - LINE SEARCH ALGORITHM

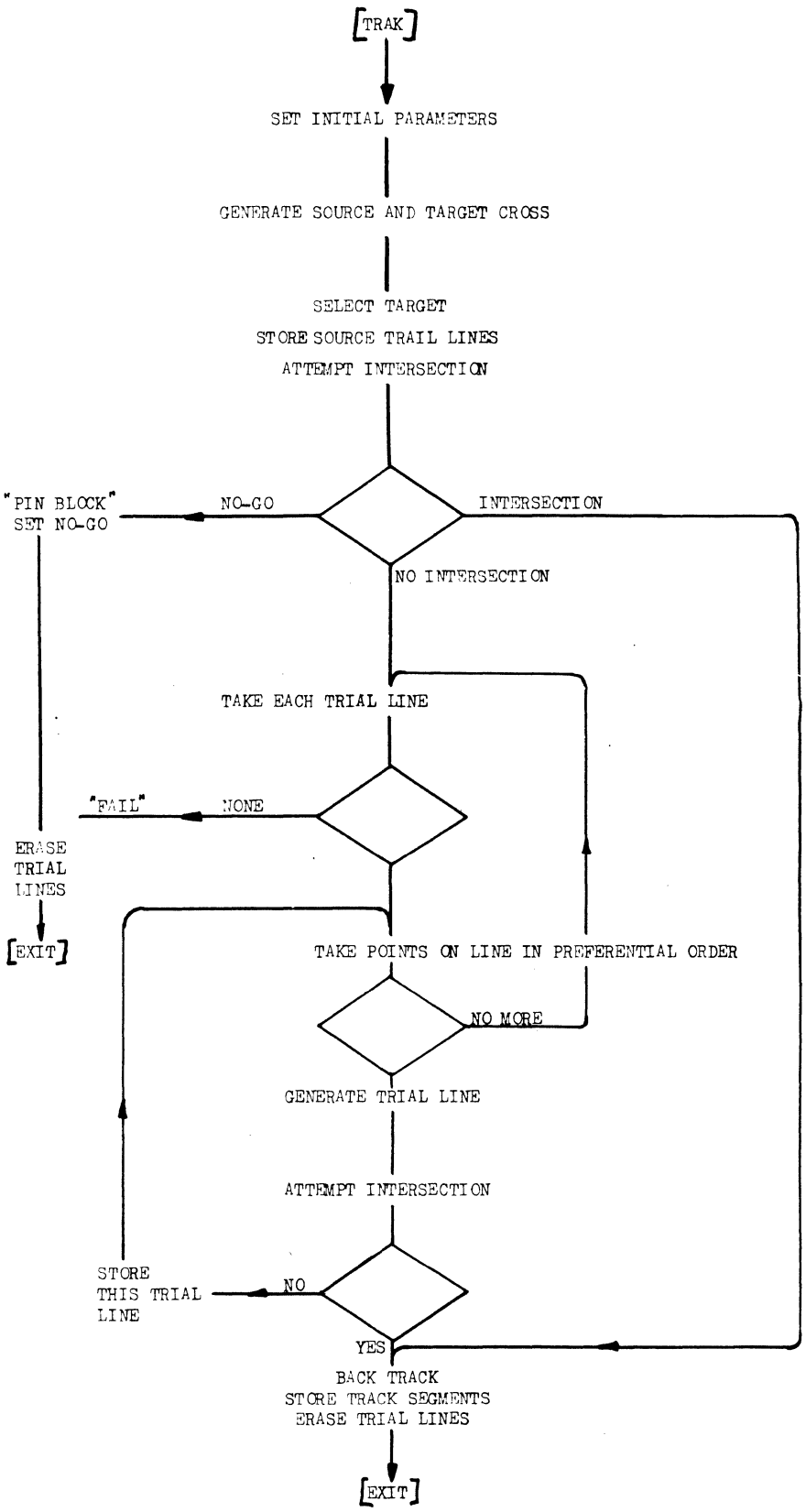

Figure 10. BASIC LINE-SEARCH ALGORITHM

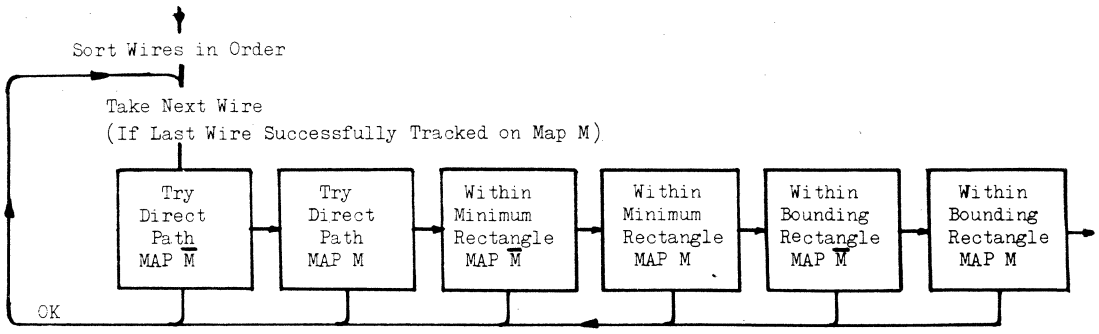

Figure 11. MAP SWAPPING STRATEGY

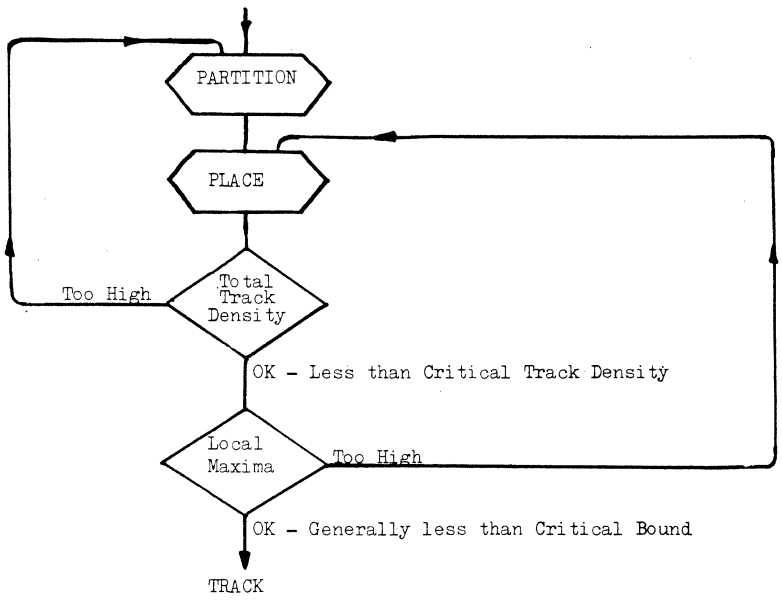

Figure 12. EMPLOYMENT OF PROFILE ANALYSIS

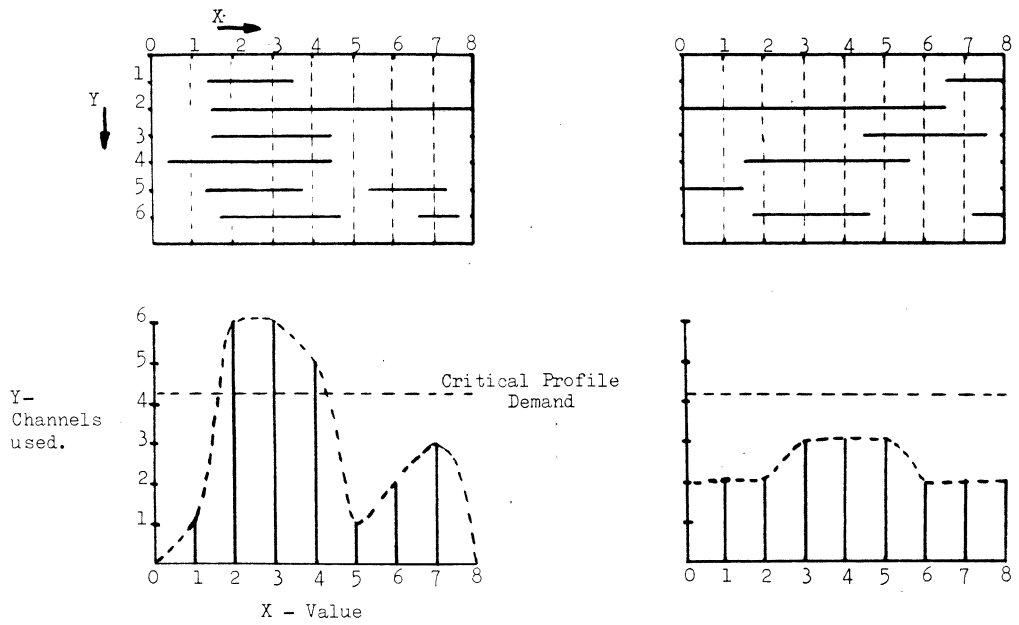

Figure 13. PROFILE ANALYSIS - EXAMPLE OF 2 DIFFERENT PLACEMENTS

GENERATION OF STEINER TREE CONNECTIONS IN A BARRIER-FREE ENVIRONMENT*

by

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We have recently developed an algorithm for the generation of Steiner trees in a barrier-free environment. The algorithm and related mathematical material appear elsewhere (1); the purpose of this note is to informally describe the concepts underlying our approach, and to demonstrate the computational feasibility of the method. Our problem model consists of a two-dimensional rectilinear grid containing nodes which must be connected by orthogonal line segments. The objective is to connect the set of nodes with a collection of lines having minimum total length. As will be demonstrated, our technique may be manually applied to problems of 25-50 points; much larger problems could be solved by utilizing computer processing. While the algorithm has not yet been proven to produce minimum length trees, we maintain that typical results are at least very nearly minimal. We hope to stimulate critical reactions to the following material by presenting it informally in this Newsletter.

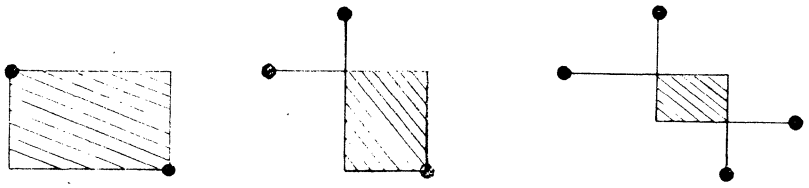
The Steiner tree algorithm is based on the concept of a minimum variable connection, which implicitly records all minimum length rectilinear paths between two points. Figure 1a shows a minimum variable connection (MVC) between two points; figure 1b portrays a MVC for 3 points.

In 1c, this concept is extended to four points: note that, as the partial network is extended to include additional points, the "variability" of the connection (indicated by the shaded area) may be reduced. We hypothesize that the "add a point to the network" operation can in general be expressed as an algorithm which impacts the variability of the evolving minimum length interconnection, but preserves the minimum total length property of the growing network.

An algorithm for producing Steiner trees based on this idea is more formally developed in material available elsewhere (1); this illustrative note continues by describing a tree connecting 26 randomly generated points. Figure 2 lists the coordinates for nodes of this example network. Our algorithm was manually applied to this problem, yielding the network shown in Figure 3. While we have been unable to prove that the 192 unit distance network is a minimum solution, we challenge readers to suggest shorter solutions! Obviously, if the proposed solution to this example is not minimal, the current algorithm is flawed. However, we believe that the minimum variable connection concept is a useful tool, and could be applied to more practical design automation problems.

For example, in a very general PC board cellular router (2) one might depict each cell as a square which contains a number of rectilinear entities representing intracellular connections to points on the cell periphery. Track segments (conductor paths plus 1/2 minimum separation on each side) could be modeled as rectangles, with minimum variable connections recorded as larger rectangular areas. The propagation of probe "wavefronts" through such cells and/or the imposition of additional connections through them could be expressed algorithmically as variable connection operations on the cell contents. An example is shown in Figure 4.

A wavefront foreward trace enters the cell area E1. Since the cell is empty (4a), a proposed wire path may leave the cell anywhere else on the cell periphery. Suppose the router later chooses boundary area X1 as the path exit point. Note that a minimum length path E1 to X1 is free to



a. b. c.

FIGURE 1. MINIMUM VARIABLE CONNECTIONS.

*This work was performed under the auspices of the U.S. Energy Research and Development Administration.

C_i, i =	Location x	y	C_i, i =	Location x	y
1	21	1	16	33	32
2	15	10	17	30	35
3	29	8	18	10	36
4	40	12	19	15	40
5	25	15	20	38	39
6	12	16	21	21	43
7	35	18	22	35	44
8	16	20	23	27	46
9	31	21	24	12	48
10	22	23	25	20	50
11	37	25	26	45	20
12	13	27			
13	26	28			
14	5	28			
15	18	32			

FIGURE 2. AN EXAMPLE PROBLEM CONTAINING 26 RANDOMLY GENERATED POINTS.

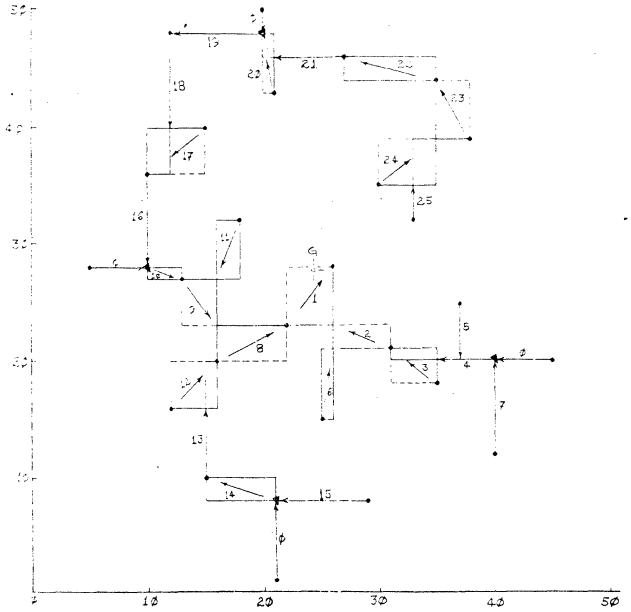


FIGURE 3. RESULTS FOR THE 26 POINT EXAMPLE: TOTAL LENGTH = 192.

traverse any area of the cell interior, which represents a minimum variable connection for signal 1.

Consider in 4b the propagation of a second signal through the cell. If the wavefront enters at E2 then the heavy darkened area of the cell is reachable for exit of path 2. This portion of the periphery can be calculated by considering the maximum variability of E2 to the remaining cell boundary, reducing all other variable connections as required (while maintaining a path, of course). Assume that X2 is chosen for the exit area of signal 2. 4c shows the resulting model of cell contents. Note that some arbitrary decisions have been made in developing this version of the model. (Shaded areas represent variable connections.)

The center region of the cell could be assigned to either connection 1 or 2, with an arbitrary choice having potential impact on later attempts to route through this cell.

If the number of paths through a cell is kept low, this "variability fragmentation" problem may not become serious. Choice of variability assignment might also be influenced by accessability status of regions bounding the area of contention.

These illustrations are not arguments to support construction of a cellular router based on similar ideas. It is quite probable that others have attempted to use this model in earlier work. We have however, not discovered published accounts of similar ideas. Suggestions, anyone?

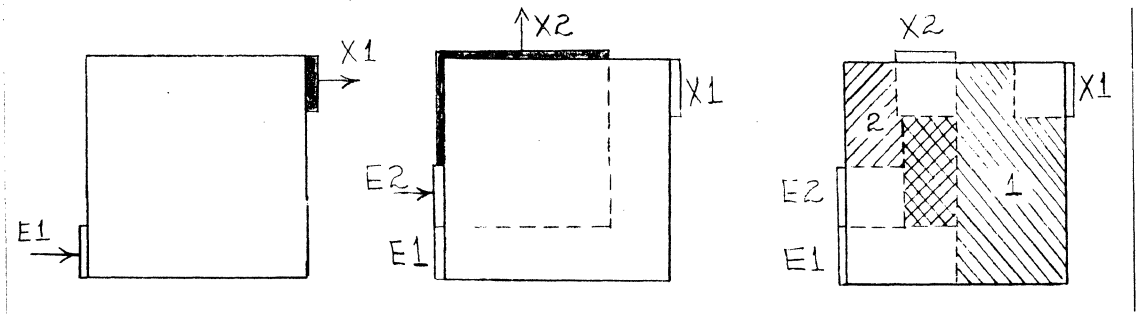


FIGURE 4. AN INTRACELLULAR MODEL USING MINIMUM VARIABLE CONNECTIONS.

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THE EQUIVALENCE OF THEOREM PROVING AND THE INTERCONNECTION PROBLEM

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ABSTRACT

A simple method of converting statements in mathematical logic to equivalent interconnection problems is demonstrated. This shows that if there exists a practical method for solving interconnection problems, then there exists a practical proof procedure for statements in mathematical logic. (In the terminology of Cook [1] and Karp [4], the interconnection problem is NP-complete.) Since such a procedure has been sought for without success for almost 100 years, we should not expect the interconnection problem to be any easier. This holds equally true for finding a method which will route a given percentage of wires.

I. INTRODUCTION

We shall phrase the interconnection prob in graph theoretic terminology. $G = \langle N,E \rangle$ will represent an undirected graph with node set N and edge set E. Individual edges will be denoted by two element sets giving the nodes they connect.

The graph theoretic model of the interconnection problem is as follows. Given a graph $G = \langle N,E \rangle$ and disjoint subsets $S_1,\ldots,S_k$ of N, find disjoint connected subsets $T_1,\ldots,T_k$ of N such that $S_i \subseteq T_i$ for $i = 1,\ldots,k$. Here G represents the circuit board with N the set of possible endpoints of wires on the board and E the set of allowable pathways between points. The sets $S_1,\ldots,S_k$ are the endpoints of nets 1 through k respectively, and the sets $T_1,\ldots,T_k$ are the points in a routing of nets 1 through k.

This formalization of the interconnection problem will be related to statements in the propositional calculus, i.e., boolean formulas of variables. A basic problem with such formulas is determining whether a given formula is satisfiable, i.e., whether there exists an assignment of True or False (1 or 0) to the variables such that the formula is True (takes on the value 1) for that assignment.

The problem of finding a practical procedure for de-

termining satisfiability of a formula in propositional calculus (or the dual problem of proving a formula is a tautology) has been studied as far back as Frege [2] in the 1870's, and it appears to be unsolvable. We shall show how, given a formula in propositional calculus, it can be recoded into an interconnection problem such that the formula is satisfiable if and only if the interconnection problem is solvable. Thus, if there were a practical method for solving the interconnection problem, there would be a practical method for solving the satisfiability problem. This should cast serious doubt on the existence of a good interconnection algorithm, even, as we shall see, one which merely routes a given percentage of the wires.

II. ENCODING FORMULAS INTO GRAPHS

We begin by showing how to encode a formula into an interconnection problem on a graph.

Theorem I. Given a formula σ of the propositional calculus, there is a graph with an interconnection problem which is solvable if and only if σ is satisfiable.

Proof. By a result of Cook [1] σ can easily be converted to conjunctive normal form (CNF); thus we may assume $\sigma = C_1 \wedge \ldots \wedge C_m$, and for $i=1,\ldots,m$ $C_i = w_{i1} \vee \ldots \vee w_{in_i}$ where each w_{ij} is a literal, i.e., a variable or the negation of a variable. The remainder of the proof shows how to convert σ, given that it is in CNF, into an interconnection problem.

We construct $G = \langle N,E \rangle$ as follows. Let σ be as above, with $v_1,\ldots,v_n$ the distinct variables occurring in σ. (Refer to Figure 1.) N will consist partly of the following nodes: nodes C_i and C_i' for each clause C_i, and nodes v_j and v_j' for each variable v_j. There will be exactly two paths between each v_j and v_j', called the high and low paths. The remaining nodes will be on these paths.

Now consider each clause C_i and the variables occurring in it. If v_j is a literal in C_i (occurring without the negation sign), place the node n_{ij1} on the low path from v_j to v_j', add it to N, and add the edges $\{C_i,n_{ij1}\}$ and $\{C_i',n_{ij1}\}$ to E. If $\bar{v}_j$ (negation of v_j) is in C_i, place n_{ij0} on the high path from v_j to v_j', add it to N, and add $\{C_i,n_{ij0}\}$, $\{C_i',n_{ij0}\}$ to E. Finally, add edges to E to explicitly form all the high and low paths.

We must now specify the subsets S_i of N which are to be connected.

$S_i = \{C_i,C_i'\}$ for $i = 1,..,m$ and

$S_{m+j} = \{v_j,v_j'\}$ for $j = 1,..,n$.

Assuming σ is satisfiable, we must show the existence of $T_1,\ldots,T_{m+n}$. Let $f: \{v_1,\ldots,v_n\} \to \{0,1\}$ be the satisfying assignment of the variables. For $j = 1,\ldots n$ let T_{m+j} be the high path between v_j and v_j' if $f(v_j) = 1$, and let it be the low path if $f(v_j) = 0$.

To construct T_i for $i = 1,\ldots,m$ note that since σ is satisfied by f, C_i contains some literal which takes on the value 1, i.e., at least one of the following cases holds:

(1) for some j, v_j occurs as a literal in C_i and $f(v_j) = 1$

(2) for some j, $\bar{v}_j$ occurs as a literal in C_i and $f(v_j) = 0$

If case (1) holds, let $T_i = \{C_i, n_{ij1}, C_i'\}$. Then $T_i \cap T_{m+j} = \emptyset$ since T_{m+j} is the high path and n_{ij1} is on the low path. By similar reasoning, if case (2) holds, let $T_i = \{C_i, n_{ij0}, C'_i\}$.

By the construction of G, all the T_i's are connected and pairwise disjoint, and $S_i \subseteq T_i$ for $i = 1, \ldots,m+n$. Thus the existence of a satisfying assignment for σ implies the existence of $T_1,\ldots,T_{m+n}$ with the the desired properties.

Conversely, given $T_1,\ldots,T_{m+n}$ define

$f(v_j) = 1$ if T_{m+j} is the high path

$= 0$ if T_{m+j} is the low path

for $j = 1,\ldots,n$.

Then it is easy to see that (1) or (2) above holds for each clause C_i. Therefore σ is satisfiable.

This completes the proof.

It is interesting to note that the graph G of the theorem can be embedded in a two layer circuit board where each layer is a rectangular grid. Thus, it is conceivable that there are circuit boards in existence that "prove" fairly nontrivial theorems in the propositional calculus.

III. FURTHER RESULTS

It is even possible that there are one layer circuit boards that are encodings of difficult problems in mathematical logic. This is contained in the following theorem.

Theorem II. Given a formula σ of the propositional calculus, there is an interconnection problem on a planar graph which is solvable if and only if σ is satisfiable.

Proof. To avoid tedious details we proceed informally, using the example of Figure 1. Basically we will show how to remove nonplanar parts of the graph

while retaining the property that the graph is routable if and only if the formula ϕ is satisfiable.

One type of nonplanarity is illustrated in Figure 1, where a path from C_1 to C_1' crosses over the high and low paths from v_1 to v_1'.

Figure 2 shows how the nonplanarity is removed. The set $S_1 = \{v_1, v_1'\}$ is also replaced by the sets $\{v_1, x_1\}$, $\{x_2, x_3\}$, and $\{x_4, v_1'\}$. These additional nodes and edges permit a connection to be made from C_1 to C_1' while insuring that the same type of path (high or low) is taken at v_1 and v_1'.

The other type of nonplanarity is also illustrated in Figure 1, where a path from C_1 to C_1' intersects the high path from v_2 to v_2' but crosses over the low path. This may be removed in a manner very similar to the method described above.

When all nonplanarities have been removed, we have a planar graph G' which is routable if and only if G is satisfiable, thus completing the informal proof.

Again, note that G' is embeddable in a rectangular grid.

We have shown that completely routing a circuit board is a very difficult problem, but one may still believe that routing only a certain number or percentage of the connections might be much easier. This is not the case, however. Garey, Johnson, and Stockmeyer [3] have shown that the problem of satisfying a given number of clauses in a formula in CNF is essentially the same problem as satisfying all the clauses, i.e., satisfying the formula. A slight modification of our proof carries the result over to the interconnection problem, showing that routing a given percentage of the wires is still very difficult.

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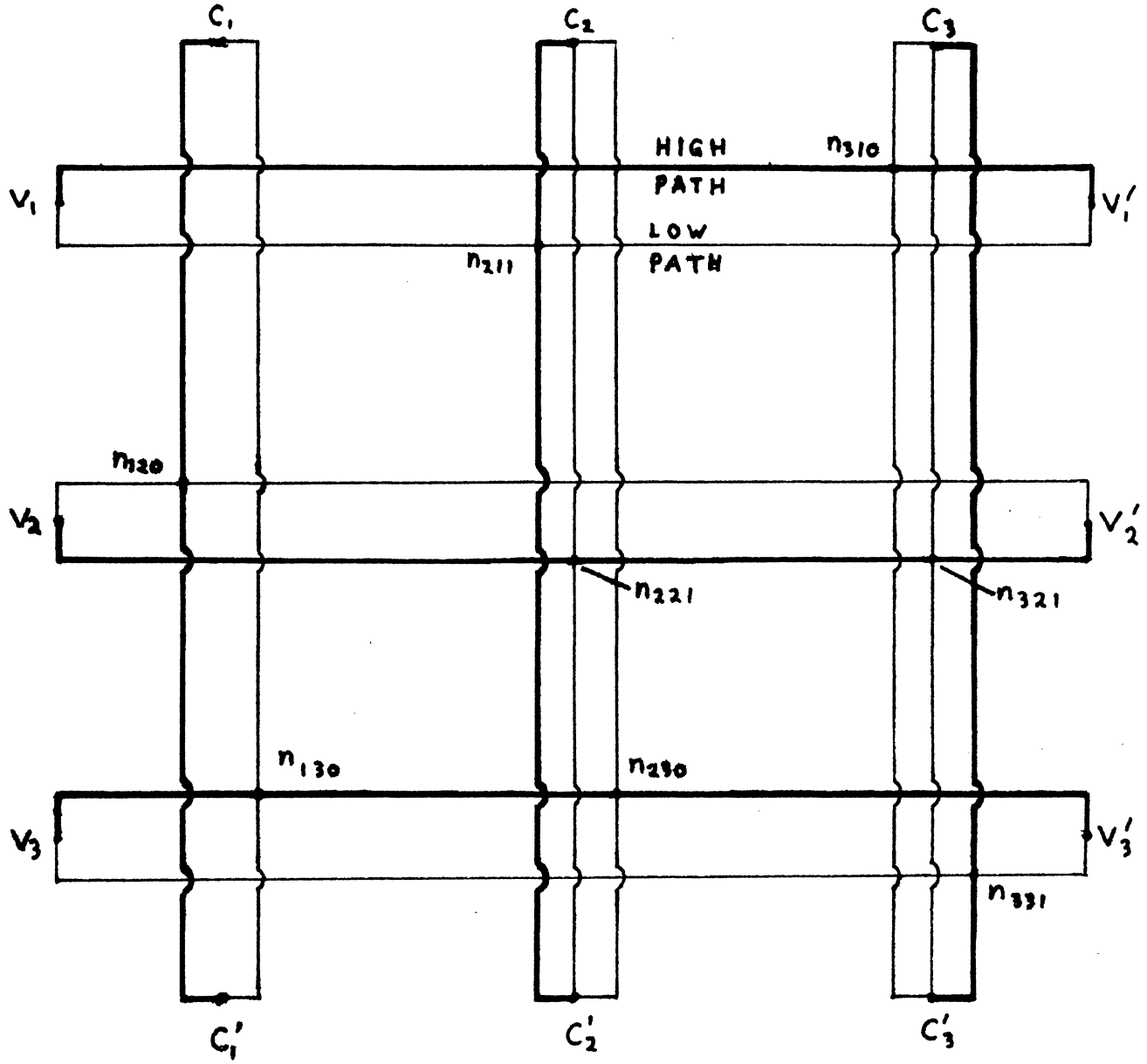

$\sigma = C_1\, C_2\, C_3$, satisfying assignment

$C_1 = \bar{v}_2 V \bar{v}_3$ $\quad f(v_1) = 1$

$C_2 = v_1 V v_2 V \bar{v}_3$ $\quad f(v_2) = 0$

$C_3 = \bar{v}_1 V v_2 V v_3$ $\quad f(v_3) = 1$

Figure 1.

Example of a formula σ and its encoding as a graph. The heavy lines connect the sets $T_1,\ldots,T_6$ resulting from the satisfying assignment.

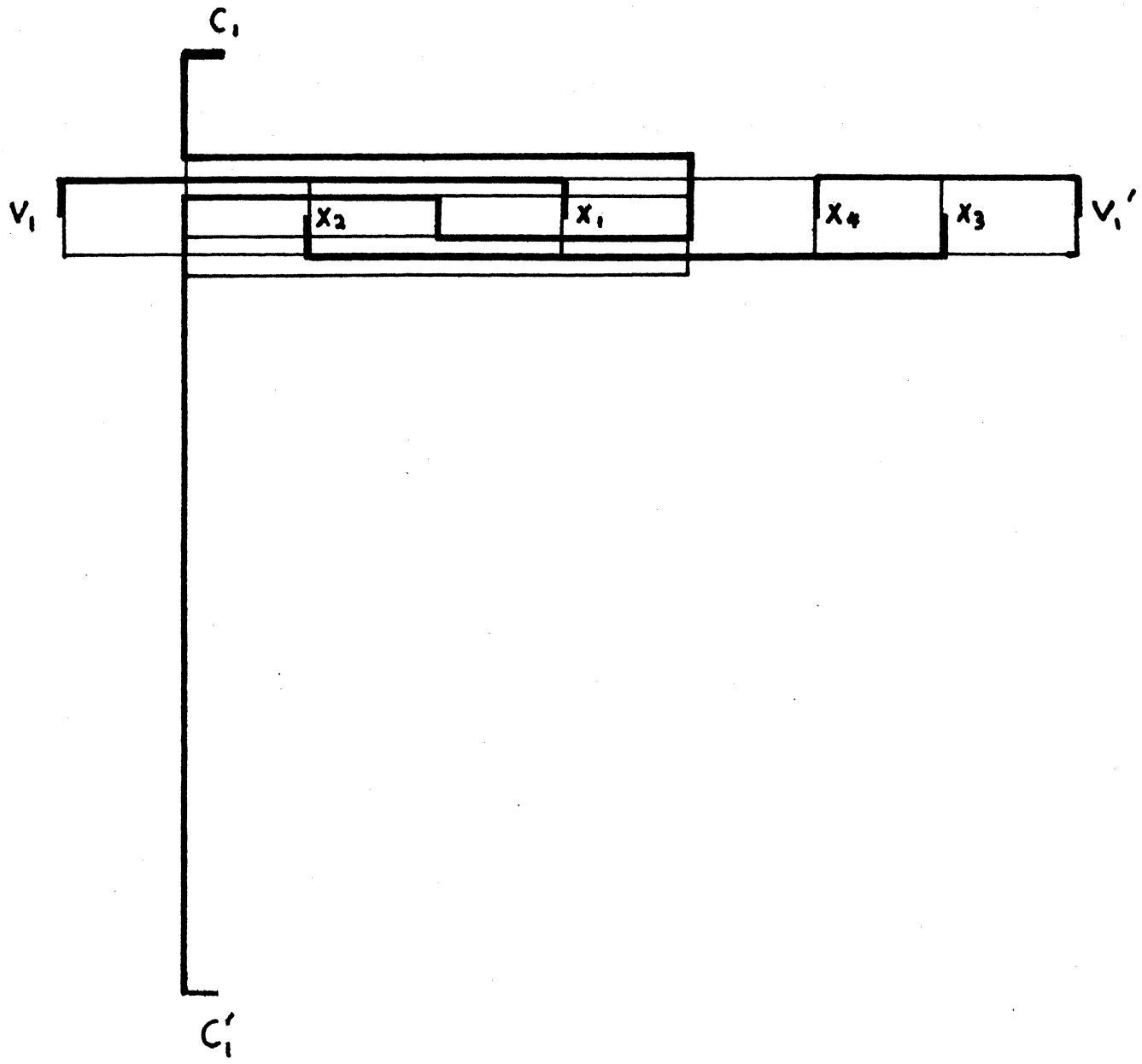

Figure 2.

Removal of nonplanarity from Figure 1. The heavy lines show the high path taken at v_1 and v_1' and the path between C_1 and C_1'.

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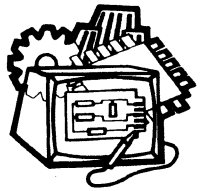
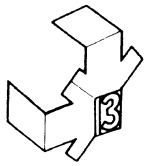
ENDICOTT, NY
13760



CALL FOR PAPERS CALL

13TH DESIGN AUTOMATION CONFERENCE



REQUIREMENTS FOR SUBMITTING PAPERS

If you plan to submit a paper, you should send three copies of the paper (rough drafts are acceptable) to the program chairman no later than December 12, 1975. Please include a title for the paper plus an abstract (less than 25 words)

Accompanying the draft should be the full name, affiliation address, and telephone number of the principal author, with whom all further direct communication will be conducted.

Notification of acceptance will be sent to you during the first week of February, 1976. After notification of acceptance, you will receive detailed instructions on the format to be observed in typing the final copy. To insure the availability of Proceedings at the Conference, your final manuscript will be due April 20, 1976.

Final papers should be no longer than 5000 words, and the presentation should be limited to 20 minutes. Projection equipment for 35mm slides and viewgraph (overhead projector) foils will be available for every talk. Please indicate what, if any, additional audio-visual aids you require.

Rough drafts are to be sent to the Program Chairman:

Program Chairman — S. A. Szygenda
The University of Texas
Electrical Engineering Dept. (ENS515)
Austin, Texas 78712
512-471-7365

General Chairman — Donald J. Humcke
Bell Laboratories
Building 1F-222
Holmdel, New Jersey 07733
201-949-6253

Design Automation

Design Automation implies the use of computers as aids to the design process.

In the broadest sense, the design process includes everything from specifying the characteristics of a product to meet a marketing objective to enumerating the details of how it is to be manufactured and tested.

Thus design automation embraces applications from one end of the design process to the other.

Site of the 13th DAC — Rickey's Hyatt House
4219 El Camino Real
Palo Alto, California
June 27, 28, 29, 1976

TOPICS OF INTEREST			
TECHNIQUES	FUNCTIONS	APPLICATIONS	IMPLEMENTATIONS
SOFTWARE ENGRG	INTERCONNECTION	MANUFACTURING	DATA BASE DESIGN
VERIFICATION	PARTITIONING	DIGITAL SYSTEMS	INTERACTIVE TOOLS
SIMULATION	INSPECTION	ARCHITECTURE	DESIGN LANGUAGES
SYNTHESIS	PLACEMENT	AEROSPACE	TOTAL SYSTEMS
ANALYSIS	TESTING	NAVAL	GRAPHICS
PROGMR PRODUCTIVITY	LAYOUT	LSI PCB	

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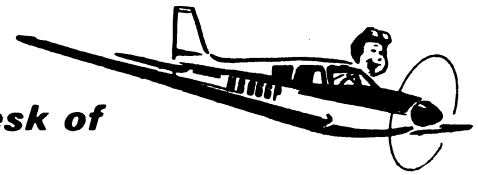


From the desk of

Donald J. Humcke

Call for Speakers

Workshop on Methods of Verification in Design Automation or Is the Design Correct?

October 8 - 10, 1975

Michigan State University, East Lansing, Michigan

Co-sponsored by IEEE Computer Society Technical Committees on Design Automation and Fault Tolerant Computing

The rapidly increasing complexity of digital technology has made it mandatory to verify the correctness of a design before committing to manufacturing. This need has, in turn, placed new demands on design automation. Thus, this year's workshop will focus on new methods of verification which have been or are being developed. The following sessions are planned:

Architecture and Logic Verification - Functional simulation, gate level simulation, Boolean comparison, architecture (RTL) - to - logic verification, etc. (Chairman: Steve Chappell, Bell Laboratories)

Microprogramming - Symbolic verification of microcode, interactive debugging/testing systems, verification via comparison to specification, etc. (Chairmen: William Carter, IBM and George Leeman, IBM)

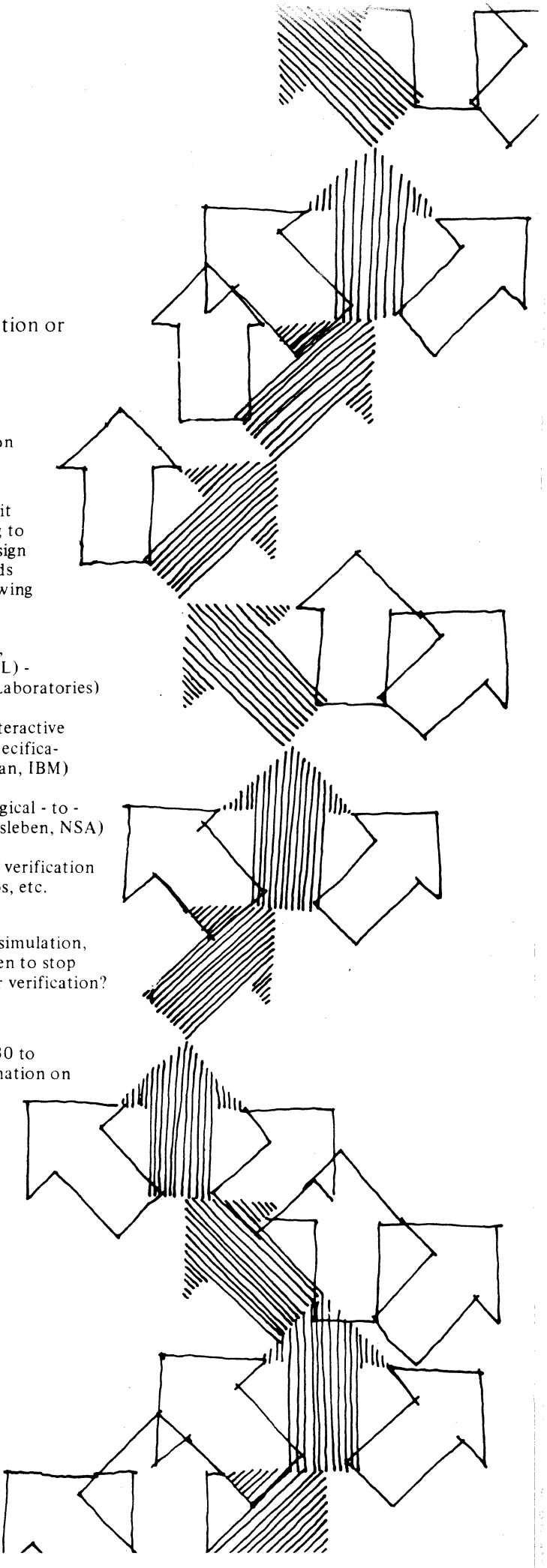
Implementation Verification - Delay and Timing analysis, logical - to - physical checking, shapes checking, etc. (Chairman: Paul Losleben, NSA)

Manufacturing Verification – Testing - DC Tests, AC Tests, verification of manually generated test patterns, testing of arrays, macros, etc. (Chairman: Gernot Metze, University of Illinois)

User Session - How are the programs actually used; e.g., for simulation, how are input patterns determined, how does one know when to stop simulating, etc.? What are the future requirements on DA for verification? (Chairman: Eckhard Schulz, Itek)

Speakers are asked to give a prepared but informal talk of about 30 to 45 minutes length, but a written paper is not required. For information on speaking or attending, contact:

Dr. Roy L. Russo
IBM T.J. Watson Research Center
Post Office Box 218
Yorktown Heights, New York 10598
Tel: 914- 945- 1643



UNIVERSITY OF WATERLOO

ACM - SIGDA / SIGGRAPH / SIGMOD

SEPTEMBER 15 - 17, 1975.

WORKSHOP ON DATA BASES FOR INTERACTIVE DESIGN.

AT THE WATERLOO MOTOR INN, WATERLOO, ONTARIO, CANADA.

Many computer-aided design systems operate on large volumes of graphical and non-graphical data. Special consideration must be given to data base management systems and working data subsets. A need exists for standardization in data base organization for business and scientific applications.

In this spirit SIGDA, SIGGRAPH, and SIGMOD (the special interst groups of the ASSOCIATION FOR COMPUTING MACHINERY for Design automation, Graphics, and Management of Data) in co-operation with the University of WAterloo are jointly sponsoring a workshop which will bring together designers who use large quantities of data and computer scientists who develop interactive data base and graphics systems. The Workshop is intended to explore mutual areas of interest and to promote an understanding of interrelated problems.

TOPICS
- Data Base Management Systems and their potential application in computer assisted design.
- Interactive computer graphics systems including data base support.
- Design Automation involving large volumes of data.
- Data distribution in design applications (intelligent satelites, data networks).

OBJECTIVES
- Stimulate the development of data base technology and its potential applications in design.
- Examine the role of interactive graphics in the design data base environment.
- Provide a forum for interaction between computer scientists and those involved in the design process.

TENTATIVE TECHNICAL PROGRAM

Monday, September 15, 1975.

INVITED SPEAKERS

"Evolving Concepts of Graphics Data Bases in Design-aids Systems"
C. W. Rosenthal and L. Rosler
Bell Laboratories, Murray Hill, N.J.

Title to be announced
J. Fry
University of Michigan
Ann Arbor

SESSION 1 - DATA BASES FOR COMPUTER AIDED DESIGN

Chairman : J. Paterson, Bell Northern Research, Ottawa, Canada.

"Enhancements to the DBGT Model for Computer-aided Ship Design"
A.E. Bandurski, D.K. Jefferson
Naval Ship Research & Development Center, Annapolis, MD

"An Environment of the Interactive Evaluation of Scientific Data and its Application in Computer Aided Design"
M. Bergen
IBM, Heidelberg Scientific Center, Germany

"Personalized Management and Graphical Display of Data: An Extensible System Approach"
L. Borman, W.D. Dominick, R. Hay, Jr., P. Kron, B. Mittman
Northwestern University, Evanston, Ill.

SESSION 2 - ARCHITECTURE AND URBAN MANAGEMENT

Chairman : C.E. Radke
IBM Corporation, Poughkeepsie, N.Y.

"Database Features for a Design Information System"
C.M. Eastman
Carnegie Mellon University, Pittsburgh, PA

"Data Base Management Facilities for Interactive Graphics"
D.F. Barnard
University of Edinburgh, Scotland

"An Approach to Implementing a Geo-data System"
A. Go, M. Stonebraker, C. Williams
University of California, Berkeley, CA

Tuesday, September 16, 1975.

INVITED SPEAKERS

"Graphics and Data-base Considerations"
R. Williams
IBM Research, San Jose, CA 95193

Title to be announced
W. McGee
IBM, Palo Alto Scientific Center
(tentative)

SESSION 3 - DATA BASE MANAGEMENT SYSTEMS FOR ENGINEERING DESIGN AND AUTOMATION

Chairman : W.D. Little
Dept of Electrical Engineering
University of Waterloo, Waterloo, Ontario, Canada

"A Data-base Design for Digital Design Automation"
M.N. Matelan, R.J. Smith, II
Lawrence Livermore Laboratory, Livermore, CA

"Integration of Data Base Management and Project Control for Engineering Design"
S.J. Fenves
Carnegie-Mellon University, Pittsburgh, PA

"VDAM- A Virtual Data Access Manager for Computer Aided Design"
D.R. Warn
General Motors Research, Detroit, Michigan

SESSION 4 - DRAFTING AND AUTOMATED DESIGN

Chairman : W.M. vanCleemput
Dept of Computer Science
University of Waterloo, Waterloo, Ontario, Canada

"A Fundamental Approach to Data-base Implementation for Design Automation"
G.S. Melanson, S.A. Spurlin
Harris Corporation, Melbourne, Florida

"Computer Assisted Cartography and Geographic Data"
J. Linders
University of Waterloo, Waterloo, Ontario, Canada

"A Data Base for Editing Printed Circuit Artwork on an Interactive CRT"
R.D. Wrigley
Bell Laboratories, Holmdel, N.J.

"A Numerical Geometry System"
K. Johnson, G. Silverman
IBM, L.A. Scientific Center, Los Angeles, CA

SESSION 5- OPEN SESSION FOR SHORT TALKS BY ATTENDEES

Chairman : R. Williams
IBM Corporation, San Jose, CA 95193

"Interactive Design and Engineering Automatic System"
D. Yelton
Digital Equipment Corporation, Maynard, Mass.

Plus other not yet confirmed.

GENERAL INFORMATION.

Registration Fees

ACM members :
Preregistration (before September 1) $ 45
after Septmber 1 $ 55

Non members
Preregistration (before September 1) $ 55
after September 1 $ 65

Students (full time, with ID) $ 25

The registration fee includes one copy of the conference proceedings, 2 lunches and the banquet.

Lodging

A block of rooms has been reserved at the Waterloo Motor Inn (475 King Street N., Waterloo, Ont., Canada - (519) 884 0220) for the duration of the conference. Rates $ 16 for a single room, $ 25 for a double.

Transportation

Kitchener - Waterloo is located on Highway 401 between Toronto and Detroit. Ground transportation from Toronto International Airport is provided by Lishman Coach Services, directly to the hotel. A reservation is desirable.
Write to Lishman Airport Transportation Service
41 Fair way Road South
Kitchener, Ontario, Canada
(519) 578 0110.

For a copy of the final program and registration forms, please contact :
W.M. vanCleemput
Dept of Computer Science
University of Waterloo
Waterloo, Ontario
Canada N2L3G1

1975 INTERNATIONAL SYMPOSIUM ON COMPUTER HARDWARE DESCRIPTION LANGUAGES AND THEIR APPLICATIONS

September 3-5, 1975
Graduate Center
City University of New York
33 West 42nd Street
New York City

This Symposium is co-sponsored by CUNY, IEEE Computer Society Technical Committee on Computer Architecture, ACM SIGDA and SIGARCH in cooperation with Utah State University.

The Symposium objective is to bring together experts in CHDL (Computer Hardware Description Languages) and people who are interested in using CHDL for describing, documenting, simulating and synthesizing digital systems with the aid of a computer. The program contains tutorial and research papers with each paper reviewed by at least two referees. There are also two sessions for presenting the most recent results and new concepts which are not fully developed.

Tuesday, September 2

7-9 P.M. Registration and Get-Acquainted Hour

Wednesday, September 3

8:20-8:30 INTRODUCTION S.Y.H. Su, Symposium Chairman
WELCOME R. E. Marshak, President of CCNY

8:30-9:10 KEYNOTE SPEECH K. E. Iverson, IBM Fellow

Session I: Tutorial - STRUCTURES DIGITAL SYSTEMS
Chairman: R. E. Miller, IBM Watson Research, IEEE Fellow

9:10-9:50 "Structured Approach to Digital Systems"
S. PATIL, Project MAC, MIT

9:50-10:10 Coffee Break

10:10-10:50 "A Directed Graph Model for Hardware/Software Design"
F. T. BRASHAW, Case Western Reserve University

10:50-11:30 "Comparison of Graph Models for Parallel Computation and Their Extension"
S. Y. FOU and G. MUSGRAVE, Brunel University, England

Session II: Tutorial - DESIGN LANGUAGE
Chairman: H. Ofek, IBM Watson Research

1-1:30 "Updated AHPL (A Hardware Programming Language)
F. J. HILL, University of Arizona

Session III: RECENT RESULTS
Chairman: J. G. Linders, Univ. of Waterloo

1:30-2:30

Session IV: WHERE DO WE GO FROM HERE?
Chairman: Y. Chu, University of Maryland

3:00-4:30 Panelists: J.A.N. Lee, R. McClure, F.J. Mowle, R. Piloty, E. Stabler, J.G. Vaucher

4:30-5:30 Planning Session for Future Symposium

5:30-7:00 Social Hour and Informal Discussions

Thursday, September 4

Session V: NEW COMPUTER HARDWARE DESCRIPTION LANGUAGES
Chairman: S.Y.H. Su, Utah State University, Logan, Utah

8:00-8:30 "A Model Approach to the Description of Hardware Systems"
E. W. VOGEL, Generaldirektion PTT, Bern, Switzerland

8:30-9:00 "Digitest II: An Integrated Structural and Behavioral Language"
F.J. RAMMIG, Universität Dortmund, Germany

9:00-9:30 "APL*DS: A Hardware Description Language for Design and Simulation"
W.R. FRANTA and W.K. GILOT, University of Minnesota, Minnesota, Minneapolis, MINN.

9:30-10:00 Coffee Break

Session VI: CHDLs IN DESIGN AUTOMATION SYSTEMS
Chairman: J.P. Hayes, University of Southern California

10:00-10:30 "The Model/Linda Design Automation System"
I. LEWIS and A.M. PESKIN, Brookhaven National Laboratory, Upton, N.Y.

10:30-11:00 "A Hardware Compiler for Interactive Realization of Logical Systems Described in Cassandre"
Y. BRESSY, B. DAVID, Y. FANTINO, J. MERMET, Universite Scientifique et Medicale de Grenoble, Grenoble Cedex, France

11:00-11:30 "Applications of an ISP Compiler in a Design Automation Laboratory"
M.R. BARBACCI and D. SIEWIOREK, Carnegie-Mellon University, Pittsburgh, Pa.

11:30-1:00 Lunch

Session VII: NEW APPLICATIONS OF CHDLs
Chairman: J.L. Houle, University of Montreal, Canada

1:00-1:30 "The Use of Two CHDL Systems, PMS and DIDL, in the Design of a Fourier Transform Processor"
A.M. DESPAIN, Utah State University, Logan, Utah

1:30-2:00 "A Language for the Specification of Digital Interfacing Problems"
A.C. PARKER and J.W. GAULT, North Carolina State University, Raleigh, N.C.

2:00-2:30 "Fault Test Generation Using a Design Language"
B.M. HUEY and F.J. HILL, University of Arizona, Tucson, Arizona

2:30-3:00 Coffee Break

Session VIII: Panel discussion: "USING CHDL AS AN INPUT TO DESIGN AUTOMATION SYSTEMS"
3:00-4:30 Chairman: J.F. Lund, Honeywell, Phoenix, Arizona
Panelists: M. Barbacci, M.D. Breuer, N. Garaffa, R.L. Hasterlik, D.P. Siewiorek

4:30-6:30 Social Hour and Informal Discussions

7:00-10:00 10 course Chinese Banquet

Banquet speaker - H. Fleisher, IBM Fellow, IEEE Fellow
Subject - "Science and Technology in the Academic and Industrial Worlds"

Friday, September 5

Session IX: EXTENSIONS OF CDL
Chairman: R.W. Hartenstein, University of Karlsruhe, Germany

8:00-8:30 "A CDL Compiler for Designing and Simulating Digital Systems at the Register Level"
J. BARA and R. BORN, Michigan Technological University, Houghton, Michigan

8:30-9:00 "A Position Paper on Extensions to the Computer Design Language"
L.R. STINE and F.J. MOWLE, Purdue University, W. Lafayette, Indiana

9:00-9:30 "Segmentation Constructs for RTS III, a Computer Hardware Description Language Based on CDL"
R. Piloty, Technische Hochschule Darmstadt, Darmstadt, W. Germany

9:30-10:00 Coffee Break

Session X: CHDL DRIVEN SIMULATION
Chairman: D.L. Dietmeyer, University of Wisconsin

10:00-10:30 "Simulation of Switching Circuits by SSM - a New Hardware Simulation Language"
W. GOERKE and H.J. HOFFMANN, Universität Karlsruhe, Karlsruhe, Germany

10:30-11:00 "The Hilo Logic Simulation Language"
P.L. FLAKE, G. MUSGRAVE and M. SHORLAND, Brunel University, Middlesex, England

11:00-11:30 "LASCAR: A Language for Simulation of Computer Architecture"
D. BORRIONE, ENSIMAG, Grenoble Cedex, France

11:30-1:00 Lunch

Session XI: STRUCTURE DESCRIPTION
Chairman: B.J. Smith, University of Colorado

1:00-1:30 "Computer Structure Language (CSL)"
J.A. HARRIS and D.R. SMITH, SUNY, Stony Brook, N.Y.

1:30-2:00 "A Structural Modeling Language for Architecture of Computer Systems"
R.I. GARDNER, JR., G. ESTRIN and H. POTASH, University of California, Los Angeles

2:00-2:30 "OSM - Microprogrammed Hardware Structure Description Language"
R.W. MARCZYNSKI, W.T. PULCZYN, J.M. SOCKACKI, Polish Academy of Sciences, Warsaw, Poland

2:30-3:00 Coffee Break

Session XII: RECENT RESULTS
Chairman: G.J. Lopovski, University of Florida

3:00-5:00

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*S. Su will be in Taiwan during July 10 - August 31.
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