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VLSI SYSTEMS DESIGN

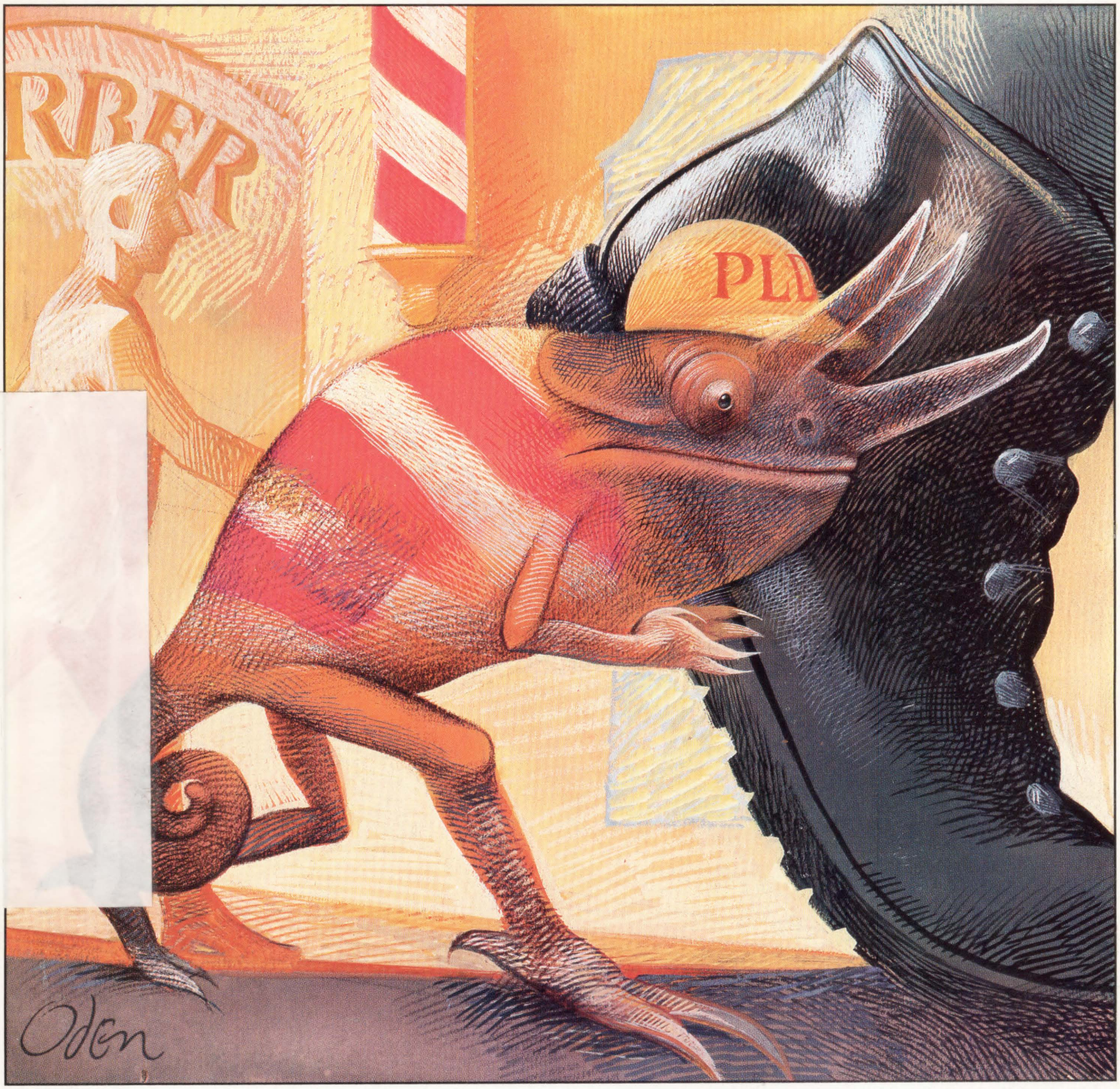
APRIL 1988

David Hightower on the floorplanner of the future

Layout software for large sea-of-gates designs

Special Report: VLSI in Japan

The Magazine for Systems Design Using VLSI Technology



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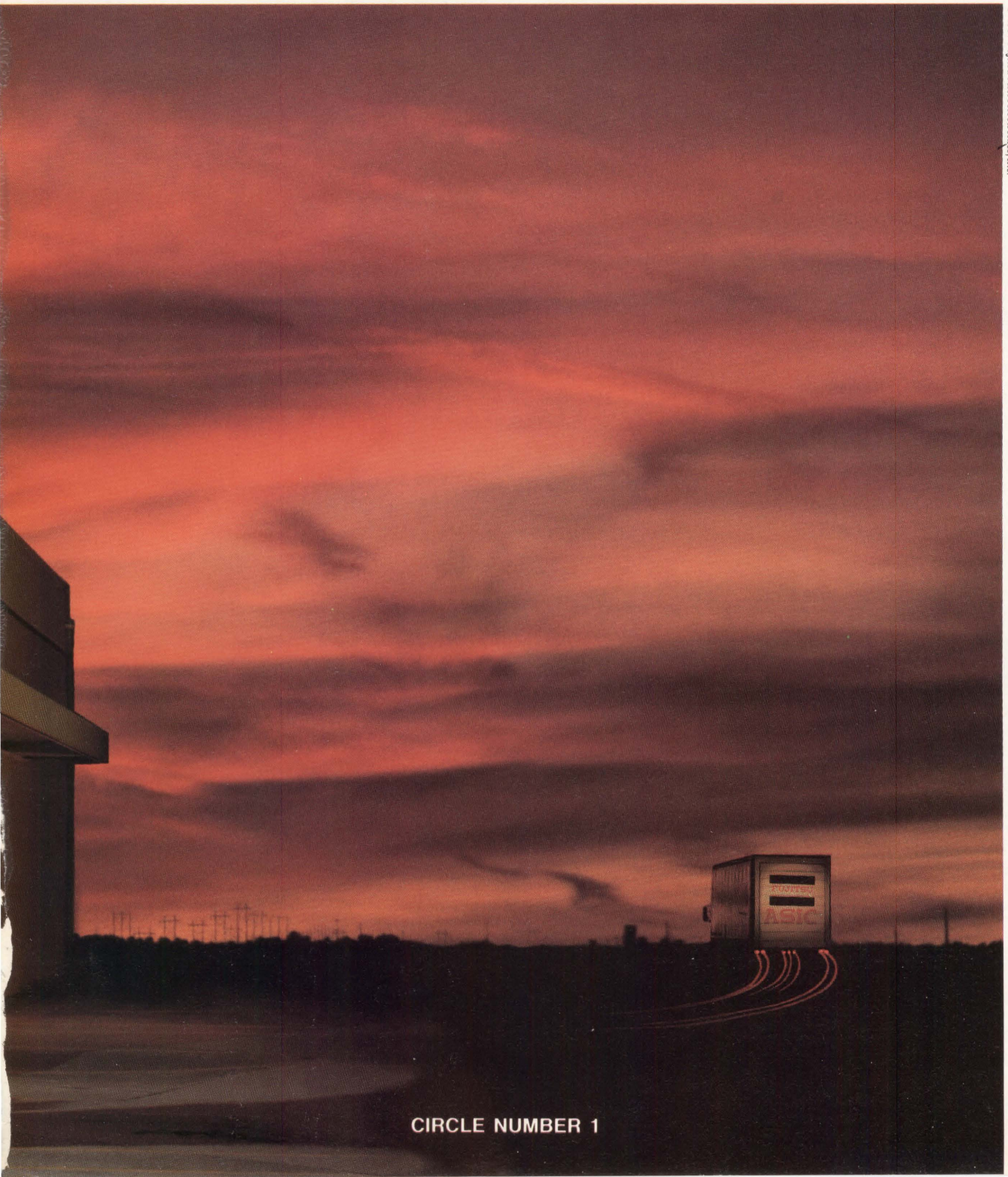

CIRCLE NUMBER 1

Publisher
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VLSI SYSTEMS DESIGN was founded to explore, expand, and define the interrelations between very-large-scale integrated circuits (VLSI) and computer architecture, design strategies, costs, and aids, as well as the electronics industry as a whole. VLSI SYSTEMS DESIGN is unique in that it is written by and for the participants in this dynamic field. VLSI SYSTEMS DESIGN intends to be the communication focus of a new VLSI design community, encourage its development, and help define its directions.

Over 41,000 copies of this issue printed.

VLSI

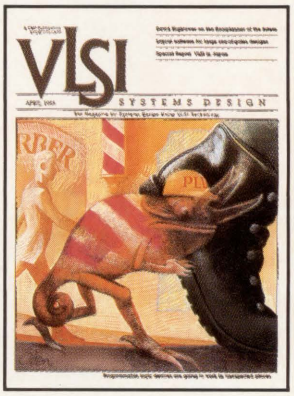
Volume IX, No. 4, April 1988

SYSTEMS DESIGN

The Magazine for Systems Design Using VLSI Technology

Cover

Chameleonlike, the latest round of programmable logic devices are adapting to new and unusual applications, thanks to architectures that give them more flexibility than earlier devices. Cover illustration by Dick Oden, Laguna Beach, CA.



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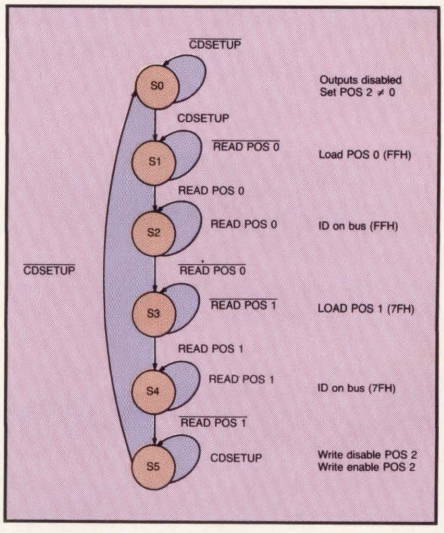

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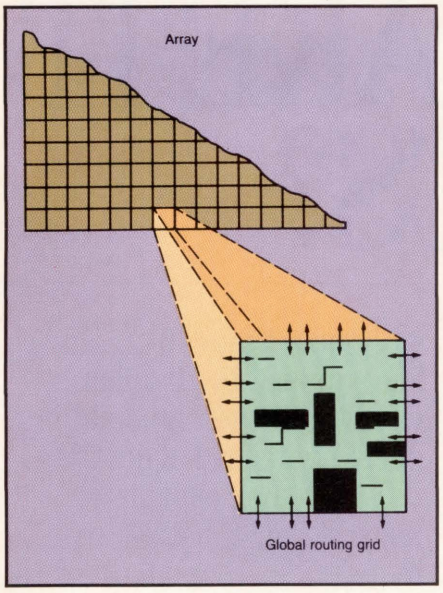

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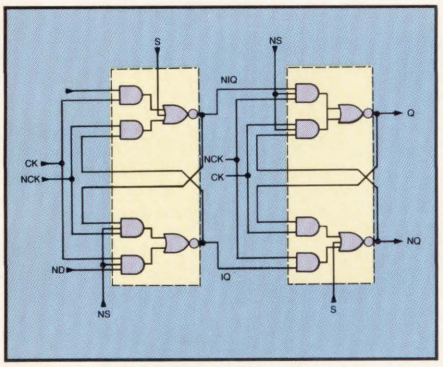

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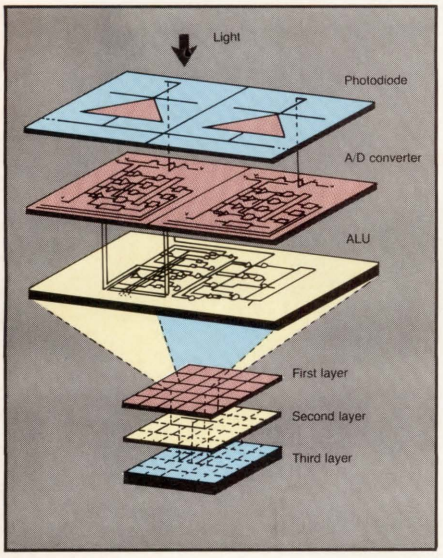

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Articles

DO YOU HAVE WHAT IT TAKES TO MAKE IT BIG IN ASICS?

Not long ago, designing ASICs wasn't even part of your job. Now it's the part everyone's counting on.

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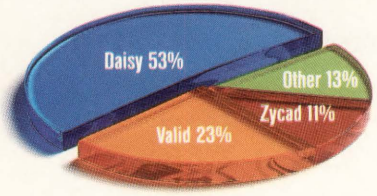

Simulation accelerator market share. Source: Prime Data, 1985 and 1986 unit shipments.

For example, our MegaLOGICIAN™ simulation accelerator is seamlessly integrated with the schematic, so you can locate and correct design problems interactively. That means faster debugging and more time to improve the quality of your design. Plus no other accelerator is as well supported, with more than 170 design kits supplied by 70 different vendors. So you can build productivity instead of libraries.

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*Based on minimum 10x performance improvement compared to 32-bit workstations. Source for design kit estimates: VLSI Systems Design's Semicustom Design Guide, 1987.

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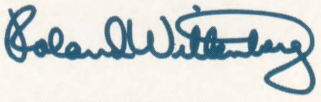
Are We Still Playing Games?

It's almost 20 years since the UNIX operating system was developed by Ken Thompson at Bell Laboratories. It was originally created for an experimental computer game. However, during the past 19 years, AT&T has revised, enhanced, and expanded the system so that it now has a robust suite of features. The University of California at Berkeley also got involved with the system in the late '70s and added many of its own enhancements and extensions such as the BSD 4.x versions.

In recent years UNIX has become one of the most popular de facto standards in the design automation industry. As a result, more and more design systems and tools are being ported to UNIX operating systems. This trend could bode well for the computer-aided engineering community. A strong, universally accepted operating system would help designers in picking and choosing a set of tools, from a variety of vendors, that was best suited to their particular applications. Unfortunately, a number of dark clouds have been looming on the UNIX horizon. One such cloud is the proliferation of different UNIX or "UNIX-like" systems. There's System V, BSD 4.3, AIX, DNIX, HP-UX, and ULTRIX, and the list keeps growing. Also, there have been numerous efforts to standardize on one unified system. Just recently AT&T and Sun Microsystems announced a long-range joint effort to develop a unified UNIX that incorporates the best features of System V and BSD 4.3. Additionally, the IEEE POSIX (portable operating system) committee has received conditional approval for a UNIX user-interface standard (IEEE-1003.1). But both System V and BSD 4.3 will require some rework to meet this standard.

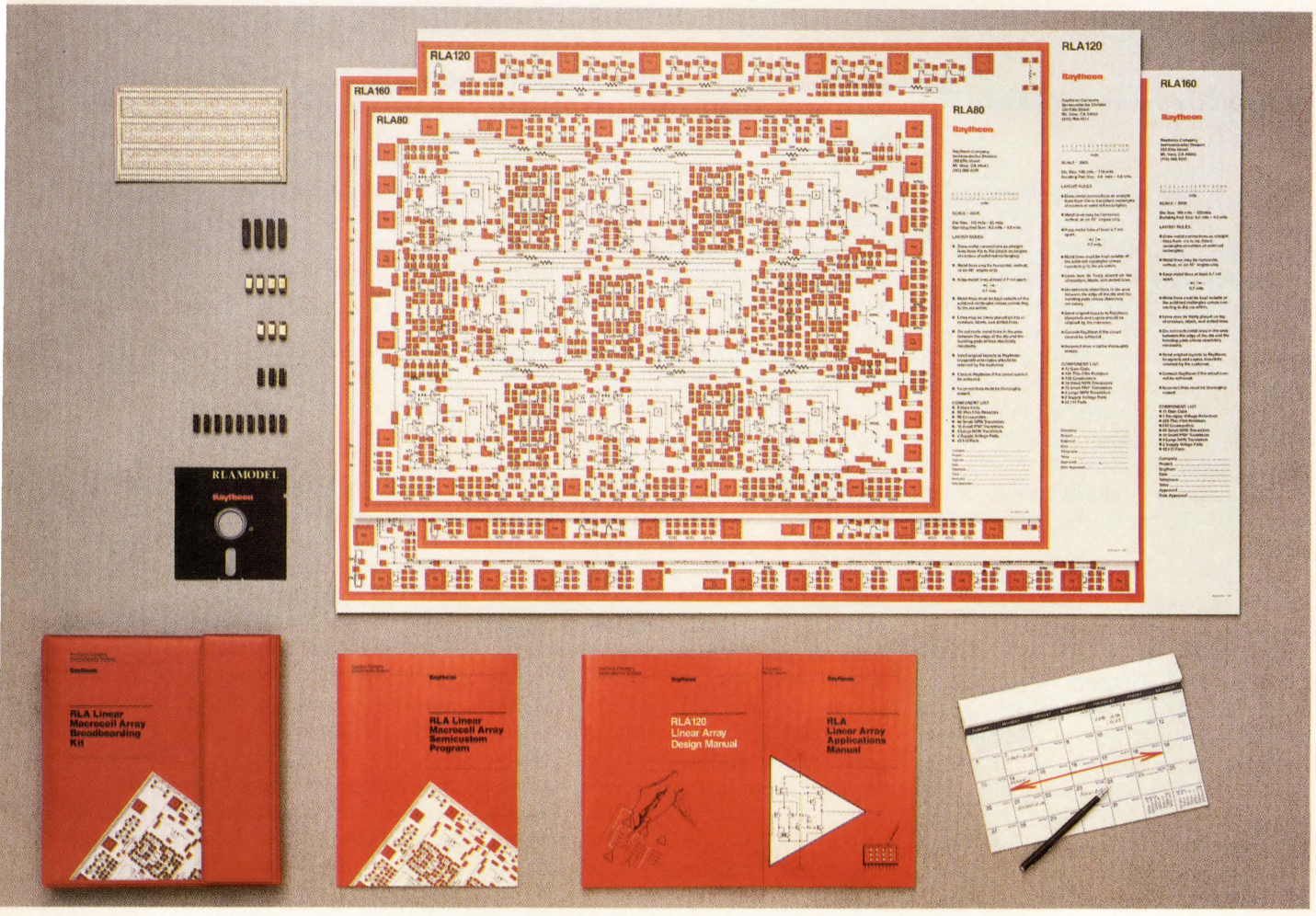
A second storm cloud appeared a few months ago when AT&T announced a buy-in at Sun. That event, together with the AT&T-Sun program for determining the future directions of UNIX, triggered a much publicized dispute between AT&T and a large group of prominent UNIX licensees. Despite AT&T's assurances to the contrary, the licensees fear that the new UNIX will end up with a built-in bias toward the Sun and AT&T workstation architectures. In addition, there are still some shortcomings to the present versions of UNIX—even though a number of independent groups from both academia and industry are hard at work on the solutions. For instance, a group at Carnegie-Mellon University has already developed a MACH kernel for UNIX that solves many of the problems of extending UNIX to networked uniprocessor and multiprocessor systems.

I doubt that UNIX will ever be the answer to every designer's prayers—and systems with large installed bases like MS-DOS and VMS won't be abandoned—but a good operating-system standard could ease and accelerate the transition of many reluctant system engineers into the world of design automation. Such a speedup can't help but benefit the entire U.S. electronics industry. So let's stop playing games with industry standards and get the various industry groups together to try to work out a solution agreeable to all parties. Perhaps a cooperative industry-university program like the X Window program now operating at MIT with industry sponsorship is the answer. We've already got a head start, since many of the university enhancements and developments for UNIX were funded with U.S. tax dollars and are now in the public domain.



Roland C. Wittenberg
Executive Editor

The One Week Analog ASIC.



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[1]PSPICE is a trademark of MicroSim Corporation.
[2]SPICE developed by University of California.

Access to the right technology

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CIRCLE NUMBER 2

A Poorly Executed Benchmark?

Dear Editor:

I must question the article "Benchmarking Schematic Entry Systems" published in your 1988 *User's Guide to Design Automation*. The article is a poorly executed product evaluation that suffers from several very serious flaws, including inaccuracy. The caveatin the concluding paragraph does not begin to cover the extent of variables unaccounted for. Here are some examples of the flaws in the article:

- The author did not solicit the current version of the products under evaluation.
- The author failed to learn about and develop a consistent methodology for evaluating the four products.

An apt example of poor methodology is that the author did not enlist users of equal proficiency even though ease of use was considered to be an important factor in the evaluation. As a consequence, a given schematic editor was judged more favorably if Ms. Filseth had access tc a proficient user of that editor. In fact, in counting keystrokes, she substituted short-cut procedures developed by proficient users, if available. That reduced the number of keystrokes for some editors and not for others.

The Daisy product did not benefit by reduced keystroke counts because, according to Ms. Filseth, the Daisy user was familiar only with DED, the precursor to ACE,and ACE was substituted at the last minute as the Daisy product in the evaluation. That helps to explain her poor rating of ACE.

It is clear that neither Ms. Filseth nor her users had much experience with the functionality of ACE. Otherwise, she would have known that ACE does indeed have an *undo* command. In fact, it is probably the only editor that has has an infinite undo/redo capability, which can be used on multiple files independently.

She also would have known that ACE can delete not only a rectangular area but any selection or group of selections the user defines. In fact, Ms. Filseth was completely unaware that ACE offers the user the ability to select and group objects so that operations may be performed on them later. This Macintosh-like feature actually reduces the required number of keystrokes.

- The author provided insufficient information about the design and published the schematic for only one editor. This lack of information is particularly disappointing because readers would have been better able to judge the contents of the article if they had access to all the critical information. For example, judging by the design shown for LSED, the times for all four schematic editors seem tremendously high. At the 1986 Design Automation Conference, Daisy conducted a "race for productivity" in which attendees were invited to use ACE to create a design similar to the one shown in the article. Nearly all of these participants, who had never used ACE before, were able to complete the schematic in under 6 minutes. Perhaps if the actual schematic created by Ms. Filseth's ACE users had been shown, readers would have been able to evaluate why such a seemingly simple design required a reported 260 minutes to complete. Showing all the schematics would also have allowed readers to evaluate the "aesthetic" problems Ms. Filseth reported.

In addition, better information about the design would have illustrated whether problems with the schematic were indeed a function of the schematic editor or the user or whether the design Ms. Filseth selected was more suited to one vendor's modeling system than that of another.

David A. Stamm
Executive Vice President
Daisy Systems Corp.
Mountain View, CA

Dear Editor:

In the article entitled "Benchmarking Schematic Entry Systems," which appeared in the 1988 *User's Guide to Design Automation*, a benchmark is performed using the Apollo DN420, a platform that has been made obsolete for over two years by two subsequent generations of computers, and by Mentor Graphics' software release 5.1 for NETED/SYMED, which in fact has been upgraded by three new software versions over the past two years. I believe that the other competitive products in this article were also far from current offerings.

The caveat at the end of her article that "software is in constant flux" cannot excuse a review of products that were replaced over two years ago.

Frank Costa
Vice President and General Manager
Design and Analysis Division
Mentor Graphics Corp.
Beaverton, OR

The author replies: *Let me start with the criticism that both Mentor Graphics and Daisy make, that systems benchmarked were not the latest offerings from the four vendors.*

Mr. Costa's complaints that the benchmark was performed on an obsolete Mentor platform using an outdated software release are valid, and I certainly share Mentor's frustration over the difficulty of keeping studies of this kind current with vendor releases.

First, I must point out that there was an excessively long lead time on this article. I initially gathered information for the study in September, 1986, and submitted it to VLSI Systems Design *for consideration in early 1987.* VLSI *accepted the article for publication in late spring but asked that I substitute Daisy Systems' new product, ACE, for DED/CED. I performed that benchmark in mid-1987. The published article finally emerged in early 1988. As a result, none of the products in this article were "current offerings."*

Secondly, recognizing the futility of playing perpetual "catch-up" with constant new product releases, I simply reported which versions I used; furthermore, I did use the most current versions available to me.

This article began as a term project in a class at San Jose State University. When I embarked upon this project in the fall of 1986, I submitted letters of inquiry to all of the vendors involved. In those letters, I described the proposed study as a student "technical report" and noted that I hoped eventually to get the paper published in a trade journal. I asked for information about recent prod-

uct releases, upcoming demonstrations, and equipment availability. Noting that my research would be incomplete were I unable to include data about these vendors' products, I asked for "any information [they] might be able to provide toward a more accurate comparison of [their] product to the other editors."

Of the four vendors in this study, Mentor Graphics alone did not respond to my letter. A follow-up call also was ignored, an my phone calls were not returned.

As for Daisy, it is certainly true that the study was originally completed with DED/CED as a prominent player and that ACE was only later substituted for its outdated precursor.

Let me now turn to Mr. Stamm's other criticisms.

• Poor methodology. *The reference to "short-cut procedures" was included because NETED/SYMED is a more reconfigurable editor than the others in this study. Ignoring this characteristic would have made it impossible to give a clear picture of that editor's real-world usefulness. If ACE also has such capabilities, I am sorry that I wasn't aware of them.*

Secondly, proficiency is a subjective quality and one difficult to measure. I enlisted engineers whose daily work required them to use the respective editors in similar capacities. All the engineers participating in this study believed themselves to be proficient users.

• Unfamiliarity with ACE. *I did not say that the Daisy user was familiar only with DED/CED, ACE's predecessor. What I said was that the same engineer who entered the DED/CED design for the original comparison also entered the ACE design. Presumably, many ACE users were once DED/CED users; I did not regard proficiency in both systems to be an unlikely prospect. It is true the ACE user was less experienced with ACE than the other users with their editors, but that is hardly surprising, since ACE is a newer product than its competition in this study.*

• Inexperience with ACE. *It is true that ACE offers the attractive features mentioned in Mr. Stamm's letter, and I am sorry I missed them. In retrospect, it seems unwise to have moved so quickly through an evaluation of ACE in a futile attempt to keep the article timely. For whatever inconvenience these mistakes may have caused Daisy, its clients, and* VLSI Systems Design, *I apologize.*

The select-and-group-for-later-recall capability he describes reduces the required number of keystrokes for group operations slightly. Since I don't know how this feature works on ACE, I will not attempt to revise my keystroke estimate.

While I strongly regret overlooking

Continued on page 66

CICC '88
May 16-19, 1988
Rochester Riverside Convention Center/Holiday Inn-Genesee Plaza
Rochester, NY

CICC '88 is sponsored by the IEEE Electron Devices Society and the IEEE Solid State Circuits Council and co-sponsored by the IEEE Rochester Section. Its goal is to bring together designers and manufacturers of circuits and systems and users of custom ICs to discuss new developments and future trends in custom integrated circuits. Session topics will include application-specific memories, circuit and logic simulation, drivers and interfaces, layout analysis and generation, analog circuit techniques, targeted silicon compilers, user-programmable logic devices, testers and testability, high-performance fabrication technology, packaging and systems interconnection, cell-based designs, telecom circuits, and reliability. For additional information, contact Mrs. Roberta Kaspar, Executive Secretary, CICC '88, 20 Ledgewood Dr., Rochester, NY 14615. (716) 865-7164.

15th Annual Symposium on Computer Architecture
May 30-June 2, 1988
Ilikai Hotel
Honolulu, HI

This annual symposium is sponsored by the Computer Society of the Institute of Electrical and Electronics Engineers and the Association for Computing Machinery. It will feature presentations that include language-oriented architectures, distributed and parallel architectures, performance evaluation and measurement, advanced devices, architectures for transaction-based systems, memory systems, architectures for artificial intelligence applications, interconnection networks, the impact of VLSI on architecture, novel computing techniques, operating-systems-oriented architectures, and tools and methods for architecture design and description. Additional information about the symposium may be obtained by contacting H.J. Siegel, General Chair, Supercomputing Research Center, 4380 Forbes Blvd., Lanham, MD 20706.

Design Automation Conference '88
June 12-15, 1988
Anaheim Convention Center
Anaheim, CA

DAC '88, which is sponsored by the IEEE Computer Society and the Association for Computing Machinery, is devoted solely to the field of design automation. This year's conference will offer tutorials, panel discussions, and technical presentations. General session topics will include electrical and discrete simulation, timing verification, testing and diagnosis, formal verification techniques, IC layout and silicon compilation, layout verification, logic and register-level synthesis, design systems and databases, behavioral and hardware description languages, design automation for integrated-circuit fabrication and for analog circuits, high-speed systems and microwave design automation, and system-level design aids. Additional information may be obtained by contacting Pat Pistilli, MP Associates Inc., 7490 Clubhouse Road, Suite 102, Boulder, CO 80301. (303) 530-4333.

ICCAD-88
November 7-10, 1988
Santa Clara Convention Center
Santa Clara, CA

This international conference, sponsored by the IEEE Computer Society and the IEEE Circuits and Systems Society, in cooperation with the IEEE Electron Devices Society and the ACM Special Interest Group on Design Automation, is oriented toward the electrical engineering CAD professional. Original papers are invited for 25-minute presentations on these topics: simulation, layout, layout verification/extraction, testing, database/CAD systems, and design synthesis. Twelve copies of both a one-paragraph abstract and a detailed 1500-word description, which are due April 29, should be sent to ICCAD-88 Secretary, Electrical and Computer Engineering Dept., Carnegie Mellon University, Pittsburgh, PA 15213, (412) 268-3546. For more details, contact MP Associates Inc., 7490 Clubhouse Road, Suite 102, Boulder, CO 80301. (303) 530-4562.

IEEE International Conference on Wafer-Scale Integration
January 3-5, 1989
Fairmont Hotel
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This conference will present a balanced program of all the aspects of monolithic wafer-scale integration, including theory, technology, applications, and products. The program will feature contributed papers, poster presentations,, and panel discussions and will cover topics such as WSI reliability, yield modeling, wafer-scale CAD systems, packaging, power/ground distribution, signal and image processors, and wafer-scale memory. Interested authors should submit, by May 1, three copies of a summarized proposal to Joe Brewer, Westinghouse Electric Corp., Box 746, M/S 5240, Baltimore, MD 21203. For more information, contact Patty Patterson, TRW Defense Systems Group, 1 Space Park (R2/2076), Redondo Beach, CA 90278. (213) 812-0788. □

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CIRCLE NUMBER 4

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Sea-of-Gates Array Technology

Shedding its quiet image, Silvar Lisco (Menlo Park, CA), pushes into the forefront of semicustom IC design with a new gate array design system, AVANT GARDS. The new software places and routes sea-of-gates designs having as many as 150,000 gates. Arrays with two or three routing layers can be implemented. Automatic and interactive placement and routing algorithms allow the tools to use between 80% and 90% of the available gates on an three-layer-metal array, according to Silvar Lisco.

AVANT GARDS is approximately comparable to the other new sea-of-gates layout system, TANGATE from Tangent Systems Corp. (see p. 22). Although TANGATE specifies a larger potential design size, we imagine that 100,000 gates is sufficient for most gate array users.

TANGATE is still available only to Tangent's technology partners. It will not be available commercially for two months. In contrast, Silvar Lisco has taken pains to make AVANT GARDS an immediately applicable product, with features we may see in the commercial version of TANGATE. AVANT GARDS can lay out designs for any foundry or process technology. It can automatically develop a model of an array and its cell libraries from physical designs in the GDS II format, and it can lay out designated nets to keep propagation delays below a user-specified maximum. Nets can also be prioritized.

AVANT GARDS contains an automatic program that produces a rough initial floorplan according to hierarchy in the logic design. Automatic placement tools improve the initial placement through hierarchical, min-cut, and seed-based placement algorithms. Routing is accomplished with line search and exhaustive maze routing algorithms. During any step, interactive placement and routing editors allow designers to preplace and alter macros and routes.

The product can, with customer input, route arrays with channels and "islands" as handily as it does sea-of-gates ICs. It is available for VAX computers for $325,000; workstations from Apollo Computer and Sun Microsystems will be supported later this year.

SGS-Thomson Microelectronics (Carrollton, TX) has already incorporated the tool into the design suite for its ISB12000 Continuous Array family.

VLSI Technology Inc. (San Jose, CA) has announced its second sea-of-gates arrays, called the VGT200 series, which join its VGT100 products. The new series has a unique "bent-contact" structure that allows the transistors to be packed more tightly, resulting in not only higher density but also lower parasitic capacitances. Like the VGT100 chips, the VGT200 arrays use gate isolation to isolate macrocells from one another, a feature that increases the flexibility of the placement tools during layout.

The total gates in the seven arrays in the series range from 30,752 to 187,300. With the denser transistor layout, utilization efficiency falls to 35% (from 75% for the VGT100 series), allowing the VGT200 arrays to implement designs as large as 10,000 gates for the smallest array and 65,000 gates for the largest. Although the total number of usable gates has not increased much from that of the VGT100 series (which accommodates 50,000 maximum usable gates), the real benefit of the new architecture is in performance. The typical gate propagation delay for the VGT200 arrays is 0.560, 70% that of the VGT100 arrays.

Both the VGT100 and VGT200 series can implement designs created from VLSI Technology's "portable libraries," which include macrocells and compilers for RAMs, state machines, and datapaths. The designs can also be implemented in cell-based ICs. NRE for the VGT200 arrays ranges from $40,000 to $150,000.

Finally, Toshiba America Inc. (Sunnyvale, CA) has shrunk its TC110G sea-of-gates arrays from 1.5- to 1.0-μm CMOS technology, resulting in the TC120G series. The new technology reduces propagation delays 33%, offering typical gate delays of 400 ps. Like its predecessor, the TC120G series uses two layers of interconnect and has array sizes ranging up to 129,042 available gates. Although Toshiba uses the TANGATE layout tools, two-layer-metal technology limits the gate utilization of the TC120G arrays to between 30% and 50%. Toshiba is accepting designs this month.

ECL Array

Raytheon Co.'s Semiconductor Division (Mountain View, CA) has rolled out its latest ECL gate array, the CGA1ME12. This low-power, high-speed array is based on the BIT1 ECL process developed by Bipolar Integrated Technology Inc., and features a typical access time of 3.5 ns. It contains 4584 equivalent gates, 1280 bits of RAM, and 120 I/O cells. The core gates are laid in 12 contiguous rows with 18 first-metal routing tracks between each row. There are 1,320 transistors and an equal number of resistors in each row. At the end of each row there are bias cells that provide reference voltages and constant current sources for the internal logic. Gate transition times are approximately 300 ps/gate, and power runs at 300 μW/gate. Commercial versions of the new gate array start at $150, with typical NRE charges running from $40,000 to $60,000.

New RISC Machines

Apollo Computer Inc. (Chelmsford, MA) is attempting to leapfrog competitors like Sun Microsystems and Hewlett-Packard by building the Series 10000 family of RISC-based computers with multiprocessing capabilities. Called the parallel reduced-instruction-set multiprocessing, or PRISM, architecture, the new design is based on co-equal integer and floating-point processors sitting on a 64-bit CPU bus. Large register files, a 128-kilobyte instruction cache and a 64-kilobyte data cache help maintain single-cycle execution of all instructions, except for floating-point division, floating-point square-root calculations, and integer division. The result is a RISC CPU board that, according to Apollo, executes between 15 and 30 VAX MIPS.

By combining one to four processors on a 150-megabyte/s, 64-bit "X-bus," Apollo will create four workstations and four servers with a peak estimated processing power of 100 VAX MIPS for the four-processor systems. Users can plug as many as 128 MB of system memory into the X-bus, as well as disk drives and an eight-plane graphics system. The X-bus also has an interface to resident VMEbus and PC AT–compatible bus slots, so that the Series 10000 systems

ARRAY FOR BiCMOS!

180 MHz with low power.

It's cause for celebration. AMCC extends its lead as the high performance/low power semi-custom leader with three exciting, new BiCMOS logic arrays that optimize performance where today's designs need it most. In throughput (up to three times faster than 1.5µ CMOS).

Today, system designers look at speed, power and density. For good reasons. As CMOS gate arrays become larger and faster, designers can't meet their critical paths due to fanout and interconnect delay. As Bipolar arrays become larger and faster, power consumption becomes unmanageable. So AMCC designed a BiCMOS logic array family that merges the advantages of CMOS's low power and higher densities with the high speed and drive capability of advanced Bipolar technology. Without the disadvantages of either.

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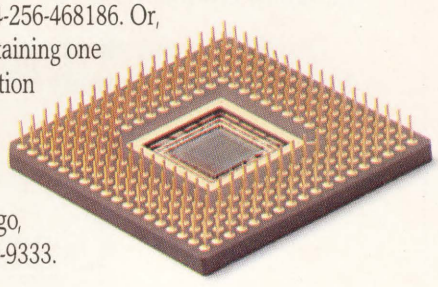
Q14000 SERIES

	Q2100B	Q9100B	Q14000B†
Equivalent Gates	2160	9072	13440
Gate Delay* (ns)	.7	.7	.7
Maximum I/O Frequency (MHz)	180	180	180
Utilization	95%	95%	95%
Power Dissipation (W)	1.8	4.0	4.4
I/O	80	160	226
Temperature Range	COM, MIL	COM, MIL	COM, MIL

*(2 loads, 2 mm of metal) †Available soon



A Better BiCMOS Array is Here.

AMCC

CIRCLE NUMBER 5

can support the same peripherals as Apollo's other computers.

The Series 10000 depends heavily on semicustom VLSI chips for its high performance. The RISC CPU chip set was designed by Integrated CMOS Technology Inc. (ICS), and the chips are being fabricated in the California foundries of VLSI Technology and the Japanese foundries of Toshiba Corp. Implemented with gate arrays having up to 256 pins and 40,000 gates, the chips use CMOS technology for the integer processor, floating-point register files, and memory management units. The floating-point multiplier and floating-point ALU are standard bipolar ECL chips from BIT.

The workstations will be "source-code–compatible" with Apollo's 68020-based platforms, meaning Apollo-based application software must be recompiled to run on the DN10000. For that purpose, Apollo has developed compilers that use data-flow techniques to exploit the parallel operation of the components in the architecture.

Entry-level prices for the servers range from $69,000 to $129,900; prices for the workstations are $10,000 more than the servers. Shipments of completed systems are expected in the third quarter of this year.

MIPS Computer Systems Inc. (Sunnyvale, CA) has unveiled its next generation of RISC chips, which could form the heart of PRISM-class computers. The new R3000 CPU, built with 1.5-μm CMOS technology, runs at 25 MHz and is specified at a sustained execution rate of 20 VAX MIPS. Its companion floating-point accelerator, the R3010, performs 7 MFLOPS for single-precision arithmetic and 4 MFLOPS for double-precision arithmetic, according to the Linpack benchmarks.

MIPS and its semiconductor partners, LSI Logic, Integrated Device Technology, and Performance Semiconductor, will be offering the chips by the end of the second quarter of this year. Applications of the new chips will benefit from an AT&T-blessed Applications Binary Interface (ABI), which will ensure that all R3000-based UNIX systems will be able to run the same software.

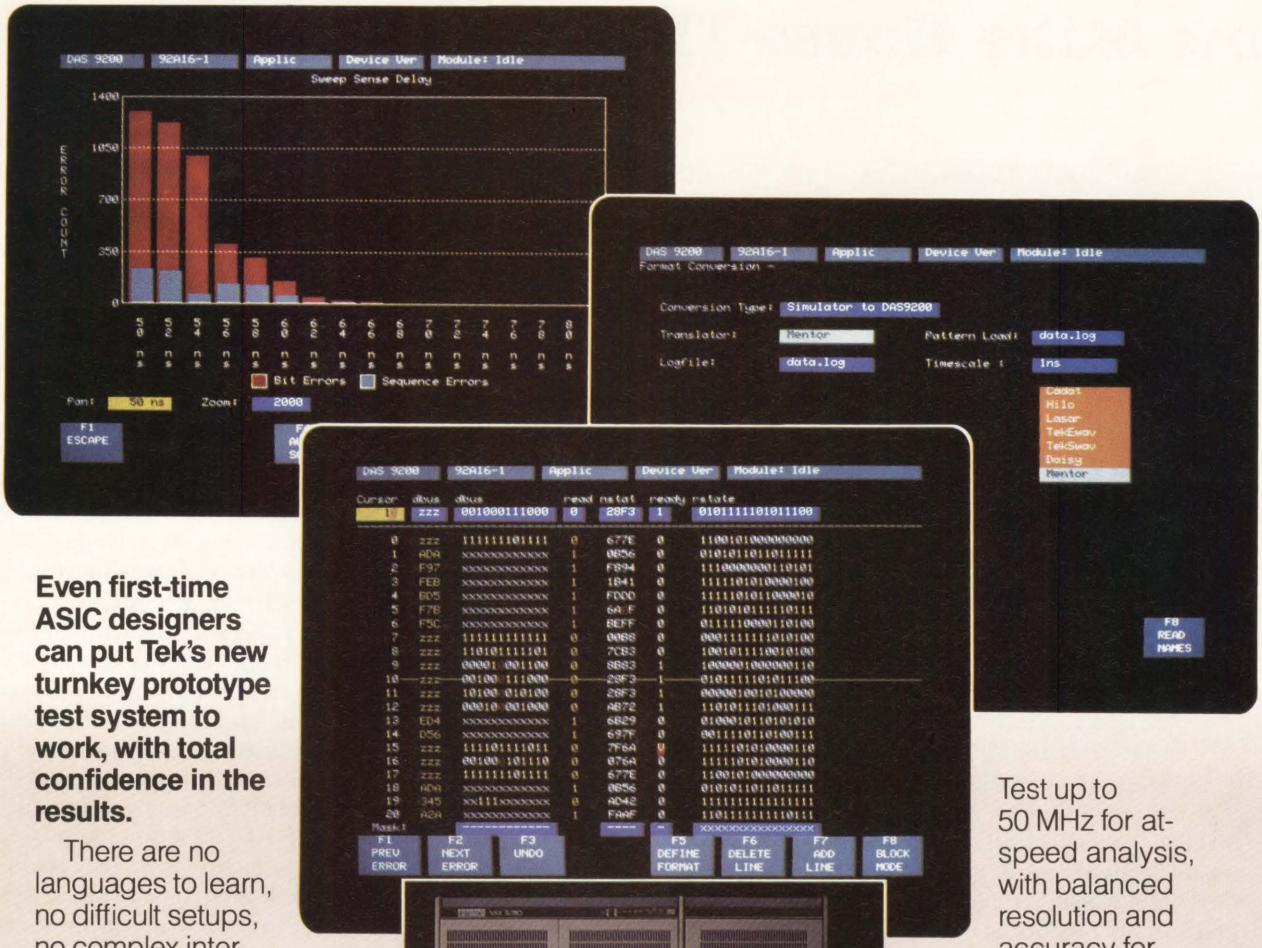
LSI Logic Inc. (Milpitas, CA) is positioning itself as the primary source for semicustom RISC machines by licensing the SPARC CPU from Sun Microsystems. As it is doing with MIPS's RISC products, LSI Logic will develop support chips and unique coprocessors for the SPARC architecture, as well as offering the CPU as a standard product and a "building-block" cell. The SPARC products will be available by midyear.

Two 64-bit FPUs

The WTL 3364 and WTL 3164 floating-

Continued on page 66

HOW TO SUCCEED IN ASIC PROTOTYPE VERIFICATION. FIRST TIME. EVERY TIME.



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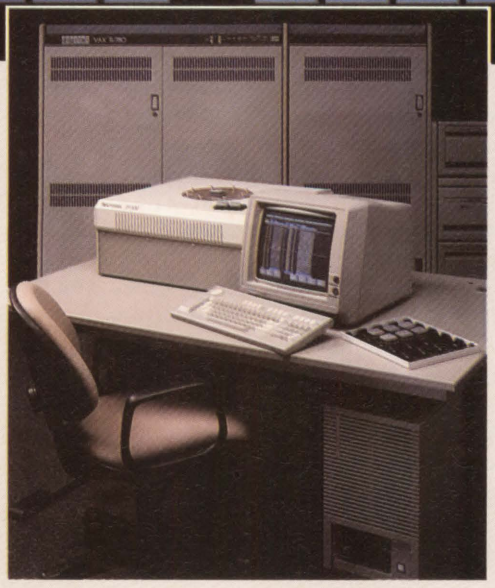

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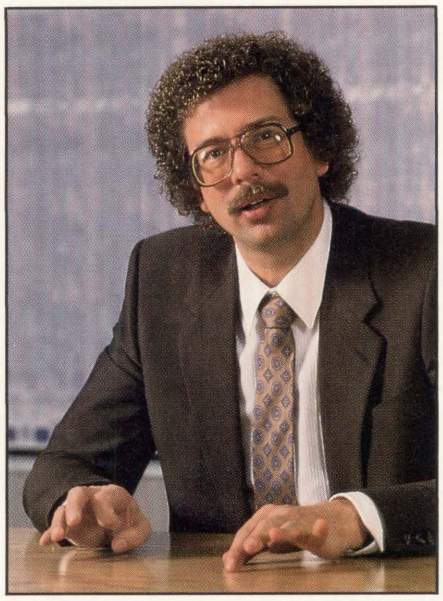
CIRCLE NUMBER 7

This Is the House That Ross Built



Ross Freeman started Xilinx Inc. to have a good place to work. A Silicon Valley veteran, he was looking for a place to hang his hat, to find some basic values: employee loyalty; a good, useful product; and pride in a job well done.

To keep Xilinx a nice place to work, Ross and the other managers interview prospective employees to find those who are "philosophically compatible." Certain types of people will flourish in the atmosphere, but not the "fast-buck types." He explains that "high-driving people who scream and bang the table wouldn't fit here."

Ross describes himself as a team player, serious about hard work, company pride, and the close knot of employees he calls "the tribe." He wants to keep the atmosphere within Xilinx pretty calm.

The strategy pays off, by the way. None of the technical staff, and only a handful of people in the whole company, have left in its four years of existence. This record gives Xilinx more continuity than most Silicon Valley companies and reduces the amount of recruiting effort needed. It also makes Ross Freeman proud.

He seems to be a man with broad ideals and high aspirations. As a physics student, he was interested in cosmology, including general relativity and the evolution of the universe. He received a bachelor's degree in physics from Michigan State University and a master of science degree in physics from the University of Illinois. As he approached his PhD thesis, though, he realized there was only a handful of jobs for those of his bent. Rather than start all over again in a new field, Ross decided to track his own path. The path led him, by way of the Peace Corps and West Africa, to a career in electronics.

Drawing on his experience with electronic equipment as a research assistant, Ross first worked at Teletype Corp. He moved to Zilog Inc., where he designed an enormously successful peripheral for the Z80 microprocessor—the serial I/O device, or SIO. He also helped design another popular peripheral, the serial communications controller (SCC). On the strength of such achievements, he worked his way up to director of IC engineering.

Ross found that he was not fulfilled by his rapid rise at Zilog. Although those times were heady ones at the company, technical management of 200 people didn't suit him. "When you have 200 people to manage, you're clearly not doing any useful work."

He began to consider alternatives. Consulting was one possibility, but he didn't like being drawn into sorting out other people's problems. "Whether you succeed or not, you don't get emotional benefit from it," he says. He decided that starting the right kind of company would give him the best work environment as well as long-term satisfaction.

At Xilinx, he has designed a product, the Logic Cell array (LCA), that he hopes will be as universally successful as his Z80 peripherals. The LCA, also referred to as a programmable gate array, reflects Ross's belief that one off-the-shelf product, if it does many things for many people, is better than a product that must be customized. "I'm an incorrigible standard-products person" he says.

Ross, Bernie Vonderschmitt, and Jim Barnett—all from Zilog—started Xilinx with only a concept and faith. They had a clear idea that something could be done and enough IC design experience to be sure they could make such a device. They didn't know exactly what type of part would emerge; "we just wanted to be the best company in the field of programmable gate arrays."

Ross also knew that he wanted to stay in the technical area. He didn't want to do the business-oriented tasks that other founders excel at. "I don't enjoy talking to the financial community," he says. "It takes a different mind set."

The part that resulted from his efforts used, for the first time, static RAM cells as the programmable elements in a user-programmable logic device. SRAM technology was chosen because it generally leads EPROM or EEPROM technology by a full generation. However, Ross points out that Xilinx is a gate array company, not a CMOS gate array company. It will use more appropriate technology when one becomes available.

The LCA itself was not the only challenge. The design software required more engineering than the hardware. In fact, the first three engineers hired were software engineers. Xilinx is as much or more a software company as it is an IC company, because, as Ross puts it, "what good is the most wonderful IC in the world if you can't design with it?"

Despite his faith in his ideas, Ross claims he's not very good at predicting the future. For now, he's quite delighted to do technical work and management. With his tendencies toward hard work, loyalty, pride, and faith, he should enjoy his coming days in the house that he helped build. *—David Smith*

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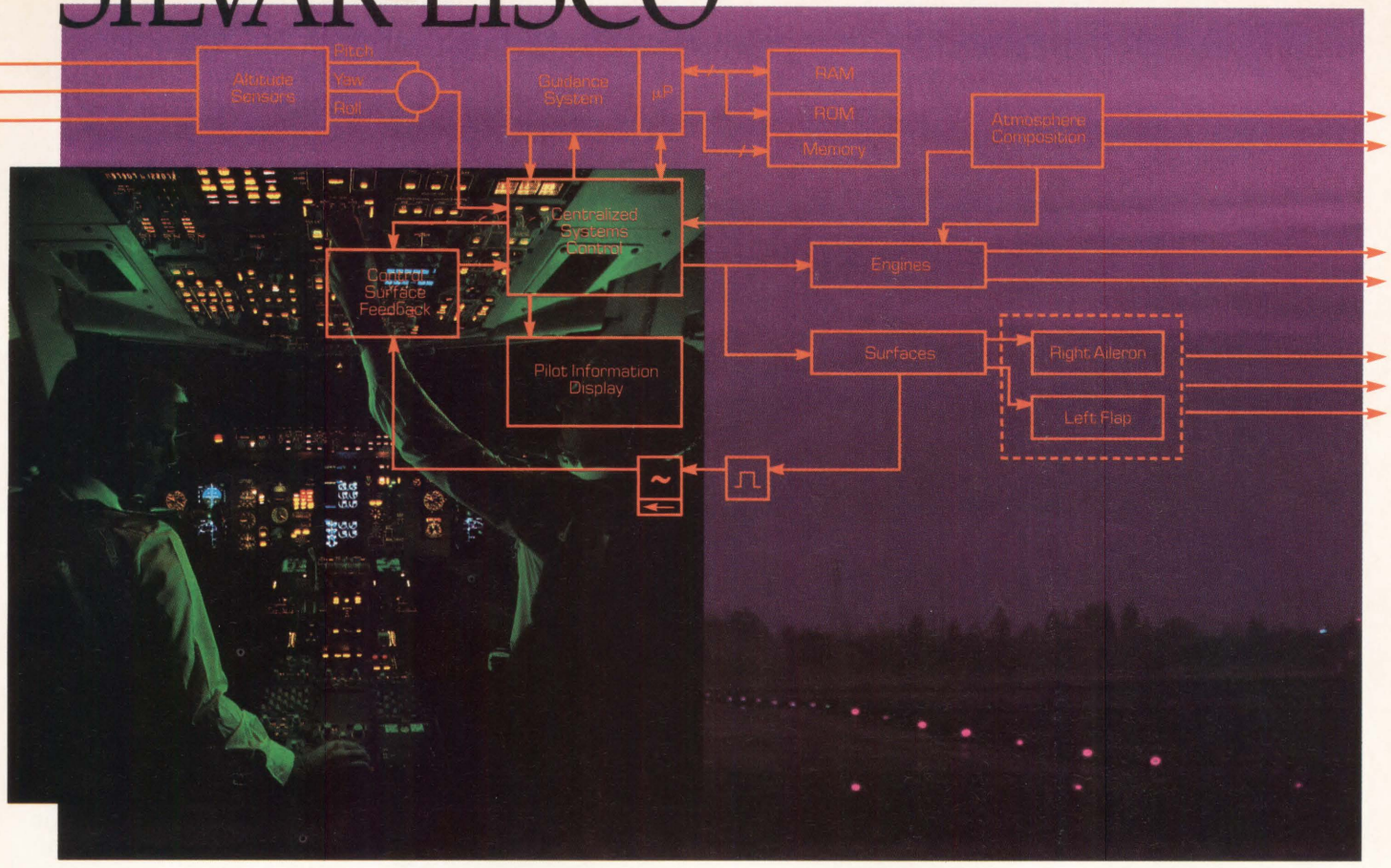

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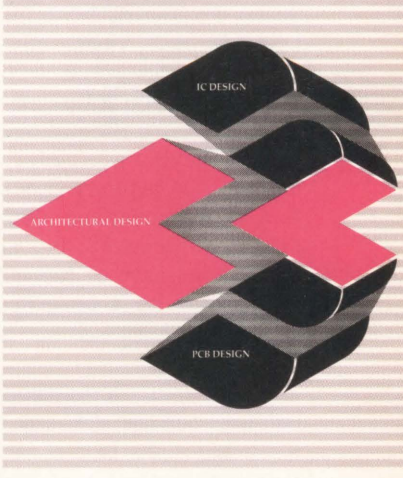

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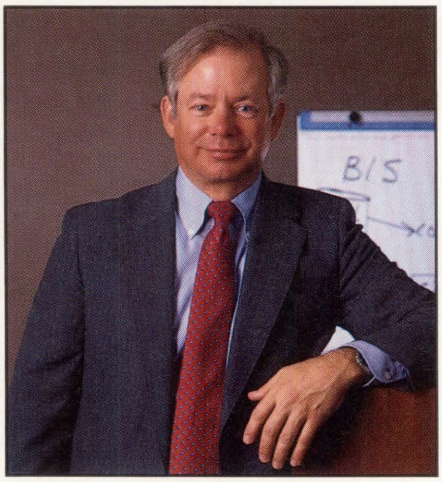
CIRCLE NUMBER 12

Floorplanning for the Future

Dave Hightower, Calma Co., Santa Clara, CA



In the next-generation layout system, the floorplanner may well be the most important tool on the designer's workbench. The reasons for this are many: the geometric increase in integration; block-style layout in full-custom chips, standard cells, and gate arrays; and the typically poor performance of block placement tools.

We know that the level of integration (number of gates per die) increases exponentially, roughly doubling every two years. I know of 1.5-million transistor chips currently in the design stage; by 1990, therefore, our technology will permit 1 billion transistors on a single chip. With such high levels of integration, achieving acceptable performance and die size requires very careful attention to placement and routing at all levels of the hierarchy. For integrated circuits in the range of 160,000 to 250,000 square mils, an increase in size of 5% to 10% is at least serious and probably unacceptable.

A powerful floorplanner is vital in helping control die size. Even with smaller designs having large blocks, a good planning tool used at the beginning of the design and at each level of the hierarchy can have a significant impact on die size, performance, and cost.

More and more full-custom chips are designed using hierarchy and block layout styles. The engineers designing these chips would like to have access to good automatic layout; however, since fully automatic block placement probably lags all the rest of CAD technology in effectiveness, at least some manual intervention is required in the beginning of the design process. Furthermore, this manual intervention also includes analysis of performance, I/O assignment, power consumption, and bus routing. For manually designed blocks, the designer has an additional degree of freedom—the aspect ratio. With a good floorplanner, the designer can analyze trade-offs intelligently, before committing himself to a particular layout.

Although hands-off standard-cell and gate array designs are routine, some designs require careful placement of certain structures to perform correctly or, in many cases, to attain successful routing. Many standard-cell designs today have microprocessor parts, large memory blocks, or other large structures. These blocks are difficult to handle well automatically. Furthermore, there is increasing demand for implementing a portion of the design as one or more custom blocks and the rest as standard cells; I believe this design style will become more prevalent within a few years. All these design styles may need careful placement and analysis to achieve the target cost and performance goals.

Even with large gate arrays, where typically we think of hands-off layout, a floorplanner can help predict exactly which gate array size is appropriate for a particular design. A few hours on a floorplanner can save a gate array designer from having to go to the next larger size of gate array, resulting in a significant reduction in recurring cost.

For all these reasons, a sophisticated, highly interactive floorplanner is required. Even the "automatic" placement tool in the floorplanner should be interactive; that is, it should have a "human subroutine" through which it calls the operator from time to time to solve some local problem and then continues searching for the global solution.

A "super"-floorplanner will have other features as well. Recursive block size and die size estimation will permit progressive improvement of a layout. Naturally, the tool should permit both interactive and automatic I/O and block terminal assignment. There should also be interactive and automatic "routing" for adding the area needed for bus communication between the large blocks.

We can foresee more advanced capabilities than are commonly available in current floorplanning systems. One possibility is a "hierarchy rearranger," to optimize the input hierarchy before layout is begun. Traditionally, the arrangement of hierarchy in the floorplanner is fixed; attempts to automate hierarchical definition have so far been mostly unsuccessful. There should also be suitability measures for channel generation or slicability. The designer could then participate in creating the most optimal hierarchy and routing arrangement. At present, the designer has no assistance in these areas.

Conventional tools should be included at the back end of the design suite, including automatic or semi-automatic placement tools; block movement tools; standard-cell movement tools; a prerouting congestion analysis program; and placement evaluation tools, with wiring length estimates tied to delay analysis.

Consequently, the next-generation floorplanner will be an extremely important analytic tool. It will no doubt be integrated with many other analytic tools, to provide a vital front-end analysis tool set that will virtually guarantee a successful layout. □

David Hightower has been the manager of advanced systems development at Calma since October, 1986. He has been involved in IC CAD since 1966.

Conference Preview

The 1988 Custom Integrated Circuits Conference

The Custom Integrated Circuits Conference (CICC) comes home to Rochester, NY, this month for its tenth anniversary. Fittingly for this occasion, the keynote address is "From Childhood to Adolescence—The ASIC Industry Comes of Age," to be given by Douglas Fairbairn, vice president of VLSI Technology Inc. and general manager of its ASIC division. ASICs, which were just finding their way into leading-edge applications at the beginning of this decade, are now considered a necessity for almost every new product. Would any self-respecting company announce a new workstation or graphics engine in today's market without also touting the number and complexity of the custom chips that make the product's breakthrough performance possible?

This year's CICC will offer a record-setting 168 papers covered in 25 technical sessions, plus four evening panel sessions and a repeat of last year's successful "New Product Announcements" session. The panels will cover some provocative topics such as the Davids versus the Goliaths in the ASIC business, the pros and cons of fast turnaround for ASICs, various trade associations and groups tied to the semiconductor industry, and the good and the bad of different semiconductor technologies. The new product session will be held Monday evening and feature eight companies, each with 15 minutes to unveil its latest offering.

First and foremost, though, the CICC will continue to emphasize its traditional role as the conference of record for application-specific ICs. A total of 19 of the sessions will be devoted to ASICs and the tools for designing them: 7 are pegged for design automation tools and 12 for the actual custom and semicustom ICs. Four of the remaining 6 sessions are devoted to manufacturing, testing, and packaging issues. In addition, reliability will have its own session, and a hot new topic, neural networks, will debut this year.

Chips and More Chips

The Thursday morning session devoted to high-density, high-performance gate arrays will cover devices with up to 12,000 gates for bipolar ECL technologies and up to 237,000 gates for CMOS designs. A. Hui et al. of LSI Logic Corp. will describe a compacted sea-of-gates array fabricated in a 1-μm HCMOS technology. The 237,000-gate array occupies a 1.5-cm^2 die and delivers 400-ps gate delays.

Also scheduled for the same session is a presentation by K. Sawada et al. of Toshiba Corp.'s Semiconductor Device Engineering Laboratory that should elicit much interest. Their paper will describe a sea-of-gates chip the same size as LSI Logic's but with only 72,000 gates. However, the gates occupy only two thirds of the chip's real estate, and the remaining third of the chip sports a complete 1-megabit dynamic RAM. The typical delay time for the gate array is 400 ps and the worst-case access time for the DRAM is 60 ns.

On the bipolar front, B. Coy et al. of Applied MicroCircuits Corp. will talk about their 12,000-gate ECL/TTL gate array with 100-ps gate delays. The chip uses three-layer metallization and a sea-of-gates architecture to achieve over 95% cell utilization. The power dissipation is less than 10 W.

"Application Specific Memories," a Tuesday morning session, will cover such topics as consumer EPROMs and RAMs, large EEPROMs for ASICs, and a unique 2-bit-per-cell dynamic RAM. Also at the session, T. Maruyama et al. of Toshiba will discuss a low-power EPROM with a wide operating-voltage range for consumer products, particularly battery-powered systems. A demonstration microcontroller running at 32 kHz and 3 V and incorporating the new EPROM structure consumes only 90 μW.

A dynamic RAM targeted at TV and other video applications will be described in a paper by Y. Murakami et al. of Sharp Corp. The 185K × 6-bit RAM stores one NTSC TV field with 6-bit quantitization. The 1.2-μm dual-metal CMOS device has a 60-ns cycle time.

National Semiconductor Corp. has developed an 8-bit parallel EEPROM megacell suitable for large EEPROM arrays, and B. Carney et al. will discuss some examples of the use of the cell in a variety of ASIC applications. A four-level dynamic RAM cell that stores 2 bits per cell will be described by T. Furuyama et al. of Toshiba. They will also describe an experimental 1-Mb array composed of 512K cells with a 170-ns access time that demonstrates the new technology.

Also on the agenda for Tuesday morning is a session entitled "Drivers and Interfaces" that covers everything from a smart biCMOS driver for 400-dot-per-inch thermal printing heads to an NMOS driver capable of modulating laser diodes at up to a 1.7-gigabit/second rate. The laser driver paper, written by K.R. Shastri et al. of AT&T Bell Laboratories, will also describe the 0.75-μm NMOS technology used to fabricate this driver. The chip can deliver adjustable constant amplitude-modulation current pulses of up to 50 mA with rise and fall times of 200 to 300 ps over a wide range of supply and input voltages as well as operating temperatures.

K. Tsubone et al. of Oki Electric Industry Co. will talk about the thermal printer driver chip that consists of a 128-bit shift register, a dot-history control circuit (DHCC), and a 128-

Custom Integrated Circuits Conference

Rochester Riverside Convention Center/ Holiday Inn-Genesee Plaza Rochester, NY, May 16-19, 1988

Key:
- Design tools
- Chips and circuits
- Manufacturing and test

Time	Holiday Hall (Holiday Inn)	Windsor Room (Holiday Inn)	101 Meeting Rooms (Convention Center)	Lilac Ballroom North (Convention Center)	Lilac Ballroom South (Convention Center)
Tuesday 8:30 a.m.	Welcome/Opening Remarks, Technical Program, Keynote Address	—	—	—	—
9:45 a.m.	**VLSI Design Environments & Synthesis** Chairman: Samuel N. Stevens Co-Chairman: Ronald T. Jerdonek	—	**Advances in Simulation Methods & Tools** Chairman: Gregory W. Ledenbach Co-Chairman: John Barnes	**Application Specific Memories** Chairman: K. Venkateswaran Co-Chairman: Ken Au	**Drivers & Interfaces** Chairman: Jagdish C. Tandon Co-Chairman: Wesley A. Vincent
Tuesday afternoon	**Circuit & Logic Simulation** Chairman: Resve Saleh Co-Chairman: Larry Bashaw	—	**Layout Analysis & Generation** Chairman: H-F. Stephen Law Co-Chairman: Constantine Anagnostopoulos	**Multidimensional Signal Processing & Graphics** Chairman: Lauren Christopher Co-Chairman: David Brown	**Data Acquisition & Phase-Lock Techniques** Chairman: David M. Lewis Co-Chairman: Douglas Barber
Wednesday morning	**Neural Networks & Speech Recognition** Chairman: Fathy Yassa Co-Chairman: David Brown	—	**Automatic Place & Route** Chairman: Daniel Daly Co-Chairman: Gerald Buurma	**Analog Circuit Techniques** Chairman: David Wayne Co-Chairman: Alan B. Grebene	**Device, Process & Statistical Modeling** Chairman: Peter M. Zeitzoff Co-Chairman: Hoda Abdel-Aty-Zohdy
Wednesday afternoon	**Targeted Silicon Compilers** Chairman: James Lipman Co-Chairman: Richard W. Bryant	**Data Conversion Circuits** Chairman: Douglas Barber Co-Chairman: Hae-Seung Lee	**User Programmable Logic Devices** Chairman: William S. Carter Co-Chairman: Sun H. Chiao	**Testers & Testability** Chairman: Allan L. Goodman Co-Chairman: Don L. Black	**High Speed Circuits** Chairman: Mark Horowitz Co-Chairman: Terry Sideris
Wednesday evening (Panels)	**Large Merchant Vendors vs. The Little Guys—Who Will Win the ASIC Business?** Moderator: D.E. Brown	—	**Fast Turnaround: Design to System—If It Can't Be Done In a Timely Fashion, Then Don't Bother Doing It At All** Moderator: J. Lipman	**Research Consortiums, Cooperatives, & Industry Associations** Moderator: T.M. Kelly	**CMOS, BiCMOS, Bipolar—The ASIC Technology Puzzle** Moderator: Mike Hollabaugh Co-Moderator: Mike King
Thursday morning	**High Density, High Performance Gate Arrays** Chairman: Rick Rasmussen Co-Chairman: Harold Scalf	—	**Telecommunication Network IC Applications** Chairman: David Embree Co-Chairman: Shya Hao	**High Performance Fabrication Technology** Chairman: Morgan Pope Co-Chairman: Marc Hartranft	**Packaging & System Interconnect** Chairman: Andras I. Lakatos Co-Chairman: Aris K. Silzars
Thursday afternoon	**Cell-Based Designs** Chairman: George Sporzynski Co-Chairman: Terry Sideris	—	**High Performance CMOS Processes** Chairman: Mike King Co-Chairman: Susumu Kohyama	**Telecom Circuits** Chairman: Charles Jungo Co-Chairman: David A. Wayne	**Reliability** Chairman: Thomas M. Kelly Co-Chairman: Stephen R. Quigley

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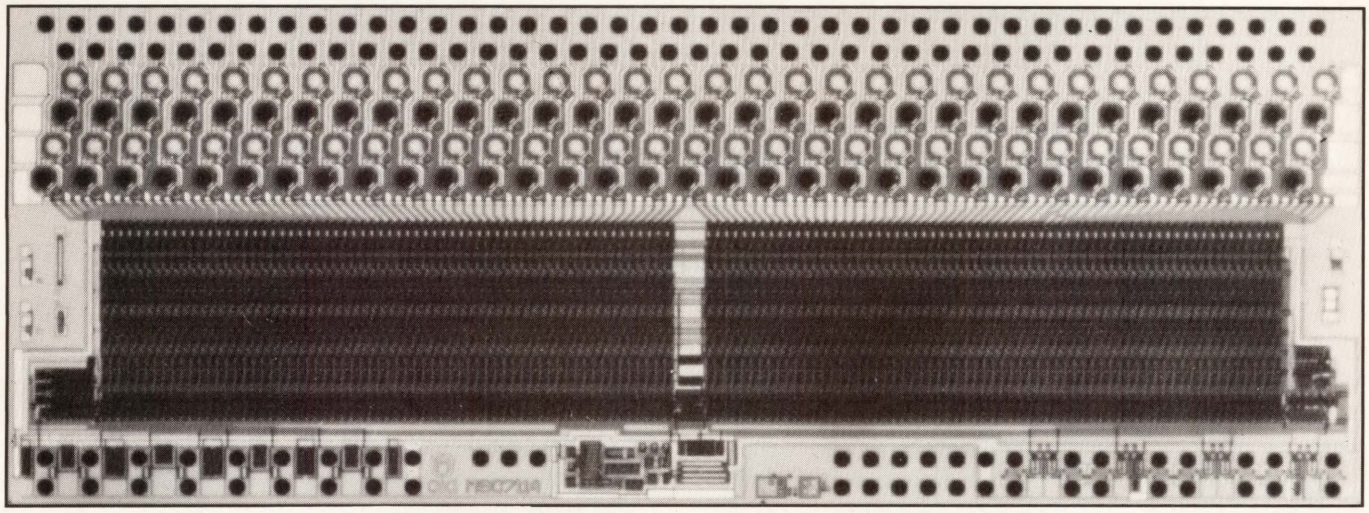

FIGURE 1. Oki Electric used biCMOS technology to develop a 128-bit smart driver for a high-speed 400-dot-per-inch thermal printer head.

bit output driver. The output drivers are implemented in bipolar technology, and the other two circuits in CMOS. The DHCC stores the drive bit and the data for the two previous bits to compensate for the heating memory of the thermal printing head. The chip (see Figure 1) is capable of driving a 400-dpi head at printing speeds of up to 1000 lines/second.

The Wednesday afternoon session entitled "High Speed Circuits" is expected to deliver just that—a variety of application-specific chips that tackle many of today's speed barriers. The applications will run from DSPs through multiplexers to arithmetic blocks. The chips use bipolar, CMOS, and GaAs technologies. The DSP application will detail an 8-bit shift register and 4-bit ALU operating at 2 GHz. The IC, implemented in GaAs by ITT, will be described in a paper by H.P. Singh et al. Also running in the 2-GHz region is the 16/8-bit multiplexer-demultiplexer pair implemented with ECL-compatible GaAs standard cells. It will be described in a paper given by B.W. Cheney et al. of TriQuint Semiconductor Inc.

If you are looking for megaFLOPS, don't fail to hear the presentation by S. Tibbitts et al. of National Semiconductor Corp. The company's latest 14×54-bit multiplier megacell clocks at 4.5 ns, and two cells can be cascaded to form a double-precision circuit with 100 MFLOPS of throughput.

Data Acquisition and Conversion

Data acquisition and data conversion chips and circuits will get plenty of attention at CICC, with high-speed analog-to-digital and digital-to-analog converters grabbing the limelight. The Tuesday afternoon session titled "Data Acquisition & Phase-Lock Techniques" leads off with a paper by F. Thomas et al. from France's Thomson Hybrides & Microndes describing 1-GHz A/D building blocks implemented in ECL-compatible GaAs. The session also will have presentations on medical data acquisition chips by G. McGlinchey et al. of S&W Medico Teknik A/S (Denmark) and a multichannel acquisition system with on-chip DSP by S.E. Noujaim et al. of General Electric Co.

"Data Conversion Circuits" on Wednesday afternoon features a paper by J.-T. Wu et al. of Stanford University that will describe a CMOS comparator for flash A/D converters that clock at 100 MHz and use pipelined cascaded regenerative sense amplifiers. On the same program is a 667-ns two-step flash A/D converter that sports 12-bit resolution. The presentation will be by D.A. Kerth et al. of Crystal Semiconductor Corp.

Design Tools

Design automation tools will still have a prominent position on the CICC agenda. At "VLSI Design Environments & Synthesis" on Tuesday morning, D.A. Pierce et al. of AT&T Bell Laboratories will provide details of a design system with many automatic features that allows the designer to move from the concept to the layout in record time.

"Advances in Simulation Methods & Tools" is also on the agenda for Tuesday morning. At this session, T.M. Kelessoglou et al. of the University of California at Berkeley will talk about the application of artificial intelligence to SPICE. The new knowledge-based SPICE environment, called NECTAR, improves the operation of SPICE with respect to its convergence properties, its ability to recognize input file errors, its user interface, and its speed of execution. One particularly nice feature of NECTAR is that it does not alter SPICE, but treats it as a black box.

At this same session and in sessions on Wednesday and Thursday, analog and mixed analog-digital CAE/CAD tools are very prominent. Typical of the mixed-mode tools is the analog-digital simulation technique described by E.S. Lee et al. of AT&T Bell Laboratories. Two specialized simulators are tightly coupled into a single computing environment with a common user interface. At the same session, R.Sparkes et al. of Tektronix Inc. give details on their approach to implementing digital macros on an analog simulator.

These are a small sampling of the papers on the varied menu that the CICC Technical Program Committee has served up. In addition, there are two sessions devoted to telecommunications circuits and applications. Codecs, modems, ISDN chips, and high-speed LANs all are covered. Also, the Thursday morning session devoted to packaging and system interconnects is expected to draw large crowds. So whatever your special interests may be, the 1988 CICC agenda is sure to whet your appetite. —*Roland C. Wittenberg*

Automating the Layout of Very Large Gate Arrays

Aki Fujimura, Tangent Systems Corp., Santa Clara, CA

System designers are placing demands on ASIC suppliers to produce gate arrays with greater capacity. Demands for 100,000 or more used gates on a single device are forcing changes in gate array architectures and computer-aided layout tools. To make efficient use of the resources of such large arrays, the tools must support large designs and be able to utilize as much of the array's gates as possible.

The sheer size of these designs and the need for fully automatic layout introduces a new set of CAD problems. These designs often have three or more routing layers and no wiring channels. Many contain RAM, ROM, and other large blocks. In addition, there are special requirements for power distribution and clock skew management. A new generation of CAD tools is required to address these problems.

The TANGATE system has been designed specifically to complete the layout of both large sea-of-gates arrays and conventional channeled gate arrays. This integrated set of tools contains unique placement and routing algorithms to lay out large arrays automatically with zero unconnected routes.

The Layout Process

The layout process begins with data entry and ends with design verification (see Figure 1). User-written C programs or netlists in standard formats or in Tangent's own proprietary text format enter library and design information into the database. The library data include array topology and existing metal routing within the base array. Design information includes the netlist; net priority, or "weight"; special-net routing instructions; macro preplacements; and macro grouping requirements. These data are verified to ensure that they are valid for the design tools before the system proceeds to the automatic layout steps.

Placement is the first layout step. Macros, including random logic, functional blocks, and I/O, of arbitrary height and width, are placed automatically in the same placement step. Legal locations for blocks and macros are automatically calculated as part of the placement process. Special-net routing steps route any special interconnections in the design before the general routing steps. Power grids using wires of multiple widths and dynamically sized vias are adjusted automatically for the presence of large blocks and to pins that fall off of the routing grid.

"Clock-tree synthesis" examines the placement of clock pins to optimize skew while minimizing the impact on routability. The program automatically inserts clock buffers to maintain even skew across the clock network. Because clock tree synthesis examines the actual placement and must insert buffers into that placement, it must be integrated with the layout steps.

Global routing and final routing steps follow special-net routing. Fully automatic results with no umcompleted connections are achieved even in very large and dense designs. Design verification completes the design process. Even though all automatic and interactive operations are correct by construction, interactive user design requires that the design rules and electrical rules be rechecked based on technology specifications in the library. All violations are graphically highlighted for fast location and correction.

TANGATE supports designs that are organized in logical and physical hierarchies. One unique capability, however, is that it can place and route large designs without hierarchical organization. Laying out a flat design is often preferable because simultaneous optimization of all areas of a design can maximizes utilization. TANGATE incorporates new placement and routing algorithms and new database technologies to allow simultaneous optimization at design complexities exceeding 50,000 nets.

Placement

Gate array layout, as opposed to full-custom or cell-based layout, must work within the constraints of a fixed die area. The placement algorithm must optimize macro placement to ensure the maximum usable routing area. This optimization is accomplished by distributing macros across the entire array, using all available space.

Iterative improvement techniques work to cluster high-connectivity components into distinct areas within the array. Special attention is paid in the algorithm, however, to reduce the tendency to pull all clusters of high-connectivity components into the middle of the array. To this end, routing congestion, an optimization criterion, tends to force component placement toward the edges and corners of the array. Net length, another optimization criterion, prevents the placement tools from sacrificing timing performance. The result is balanced routing across an array, rather than extreme routing congestion in the center, a problem with more traditional gate array layout systems.

In TANGATE, both placement and floorplanning are completed in the same step. Blocks of any rectilinear shape (even **L**- or **I**-shaped blocks), I/O buffers, and random logic macros are placed automatically during the same layout step. Electrically equivalent alternatives (with the same speed and func-

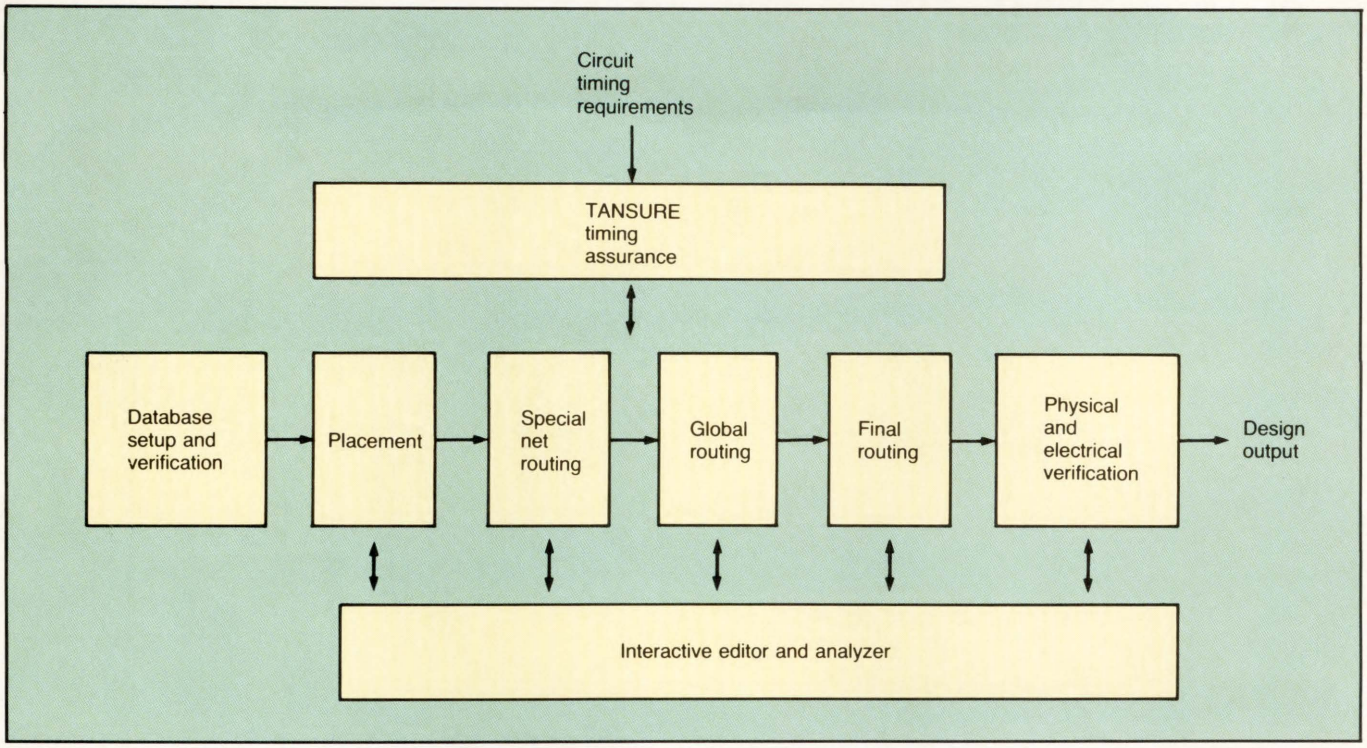

FIGURE 1. Layout process flow for the TANGATE layout system.

tion) and orientations of each block and macro are tried to determine the best placement. The user defines equivalences among macrocells and among functional blocks in the library.

Floorplanning is accomplished through the placement tool's ability to recognize area restrictions entered by the designer. A "keep in area" feature enables the designer to incorporate logical partitions of the circuit design in placement constraints in the physical placement space. The design text file lists the components in a logical partition, as determined by the designer. The placement tools keep these components within the area constraint while optimizing net length and balancing routing congestion across the array.

Routing

Automatically completing a large design with high gate utilization and zero uncompleted routing connections requires a unique routing methodology. Traditional routing techniques do not perform well in large sea-of-gates or three-layer designs. Channel routers, for example, can severely constrain the topology of the design by imposing reserved routing channels. High gate utilization in triple-layer-metal gate array designs, however, produces routing areas without distinguishable channels. Channel restrictions would waste space and thus reduce gate utilization within the array. Another approach, routing the entire array at once with a maze router, entails a prohibitive memory space and run time.

Instead of using either of these approaches, the routing process in TANGATE is broken into two steps: global routing and final routing. The global router produces a coarse routing solution for the entire chip, and the final router automatically completes routing within subregions, routing the most congested ones first.

Global routing breaks the array space into global routing cells. The global router determines for every net which cells

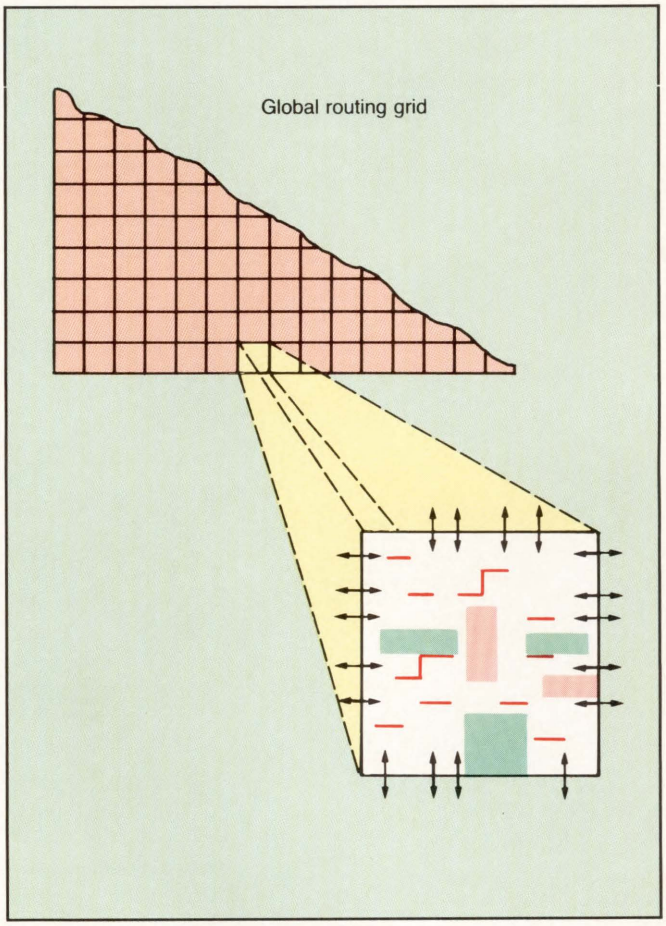

FIGURE 2. Obstructions along a global routing cell.

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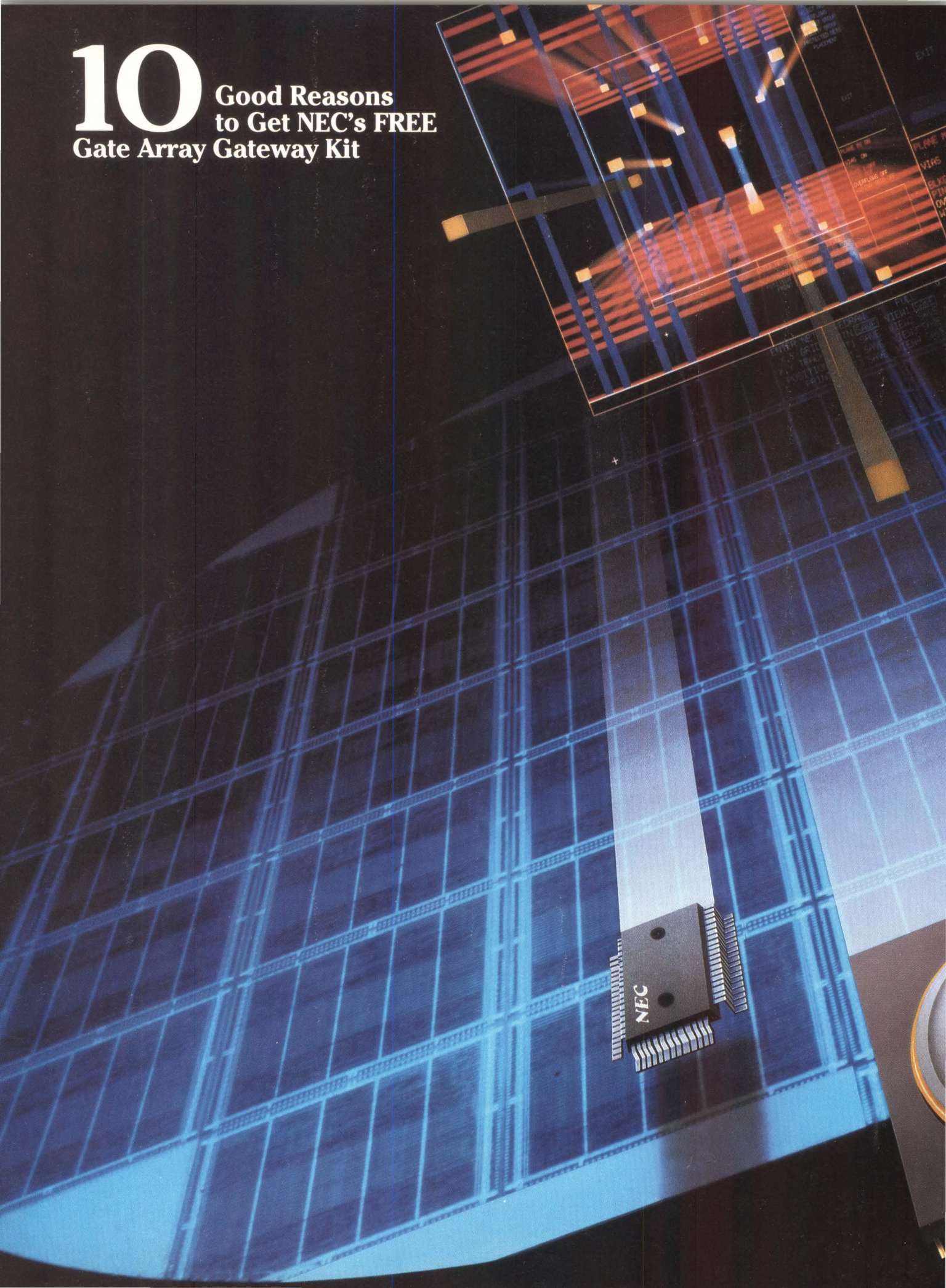

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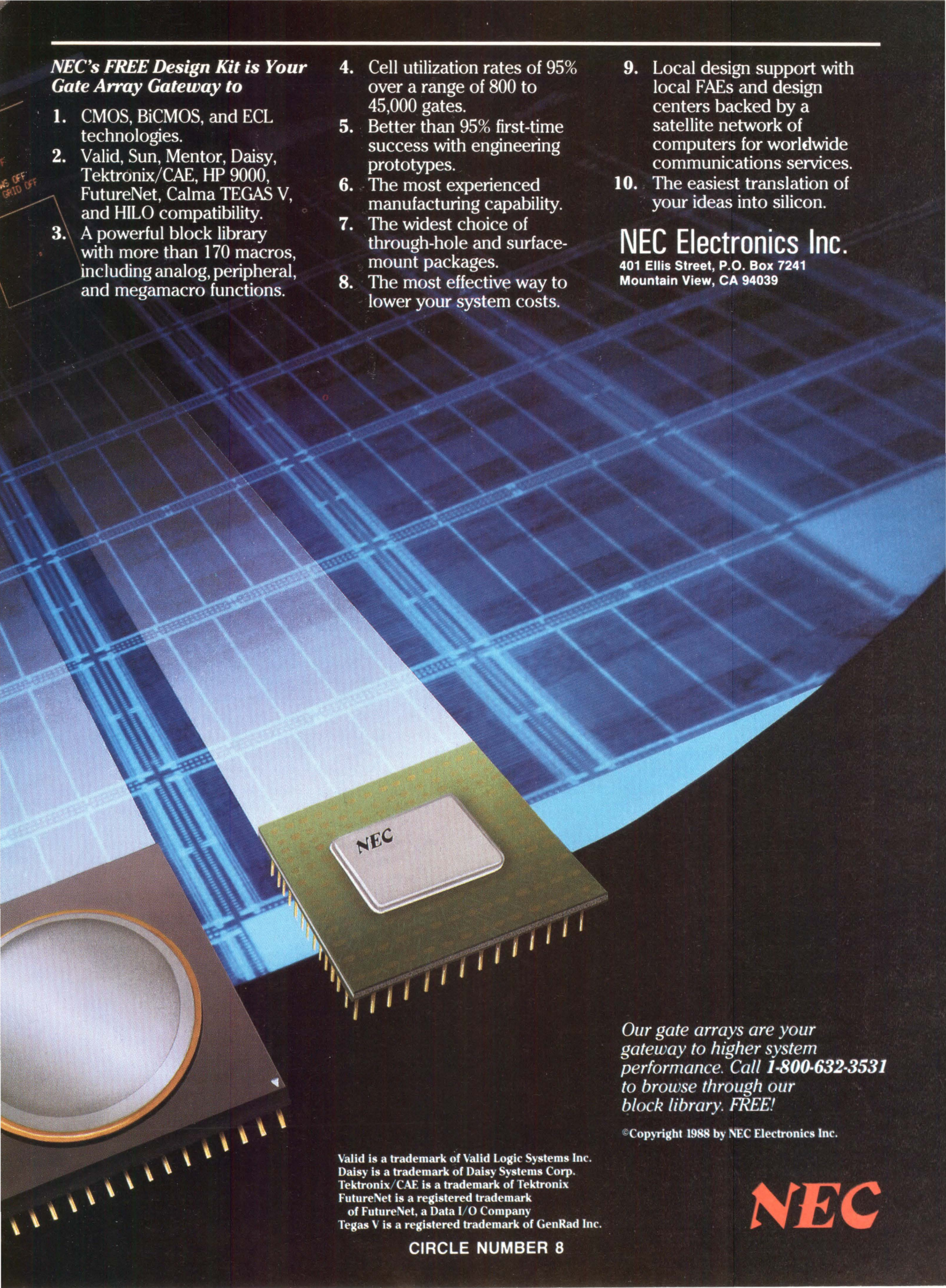

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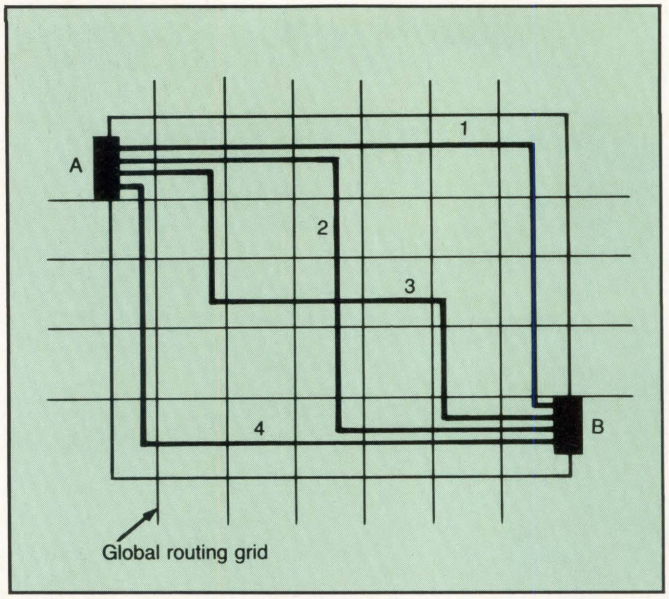

FIGURE 3 A variety of routing alternatives from A to B give rise to different global routing alternatives, all of equal net lengths.

are used to route that net. Each cell consists of boundary edges, connection pins within the boundary, and routing obstructions within the region (see Figure 2). Cell size is determined by the array technology (macro size, spacing rules, and such). The global router optimizes the flow of interconnections across these boundary edges.

As noted, routing congestion and wire length are the primary criteria used in measuring the merit of a routing solution. Reducing the congestion increases the probability of 100% completed connections. Controlling the wire length ensures that the routable design meets timing performance requirements. Timing Assurance, an upcoming option to the system, gives the tools greater flexibility in relieving routing congestion. The Timing Assurance tools tell the router which signals have critical timing parameters and need to be short and which signals can be allowed to meander to reduce routing congestion.

Many different paths of minimal length can exist between any two connection points in a design (see Figure 3). Hence it is important to explore fully all the paths of minimal length to minimize congestion. Poor distribution of interconnects during global routing will lead to potential routing incompletions during final routing. TANGATE's global router uses iterative improvement techniques to attain minimal congestion while maintaining minimum wire lengths.

Final routing works by routing a sequence of small regions, each consisting of multiple global routing cells. These regions may contain pins, routing obstructions, and preroutes in arbitrary locations and on arbitrary layers. Further, pins and obstructions may be of arbitrary shape and may also be noncontiguous. All global routing assigned to the region is final-routed. The resulting final routing is stitched back into the global routing at the region boundary. The final router's goal is to complete all interconnections while minimizing vias and optimizing wire length.

Via minimization results from the tools' freedom to select among multiple connection points along a pin and from the

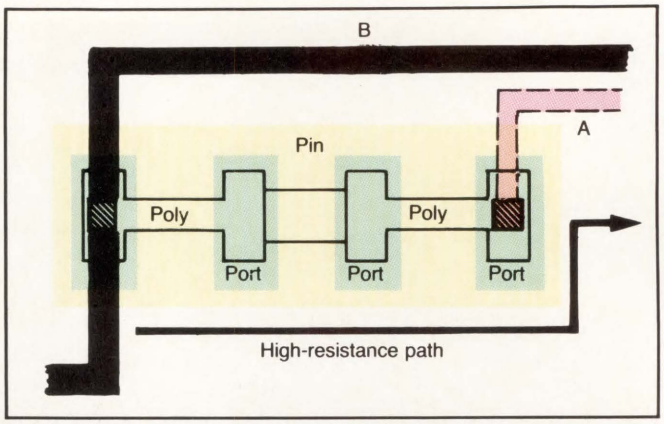

FIGURE 4. General "pin-port" modeling prevents the selection of a high-resistance path A over the higher-performance path B.

router's ability to make short routing jogs without changing routing layers. The final router selects the best connection point on a pin based primarily on routing congestion and net length. The routes can change direction in the same layer to connect to a pin or to avoid a routing obstruction.

Increased circuit performance results from the ability of the TANGATE software to select between connection points on a pin. A "pin-port" model enables the user to specify distinct, mutually exclusive portions of the pin to be used for connections. Like the pins themselves, the ports may be of arbitrary shape and may be noncontiguous, connected within the cell. TANGATE will use only one of these ports in making connections.

In Figure 4, for example, a pin is defined in the macro library to consist of two ports: the left port and the right port. A signal route that enters a pin at the leftmost point could exit the pin at the rightmost point, on line A, by using the polysilicon path through the pin. This option could produce the shortest overall connection. The polysilicon path, however, has significantly higher resistance and so would increase interconnect timing delays. In this case, the routers would connect to only the leftmost port and continue from that port, on line B, without using polysilicon in the routing path.

The final routing process uses similar improvement techniques to those of the global routing. Initially, the final router produces a route for each net. Improvements are made by trying other routing paths, under the control of an iterative improvement system. The choice of a new routing path depends on previous improvement attempts and their associated costs. Iterative improvement refines the routing, producing high gate utilization while maintaining 100% connections.

Although fully automatic, the layout tools keep the designer informed of the progress of the layout. Early feedback of routing congestion can warn the designer of potentially overconstrained designs. A routing congestion map graphically shows him where the global router has found areas of high routing congestion. Additionally, the timing analyzer in the Timing Assurance package will give early feedback of potentially overconstrained timing conditions in a design. Interconnect delay data, back-annotated to simulators, can uncover timing race conditions or other timing-related circuit malfunctions.

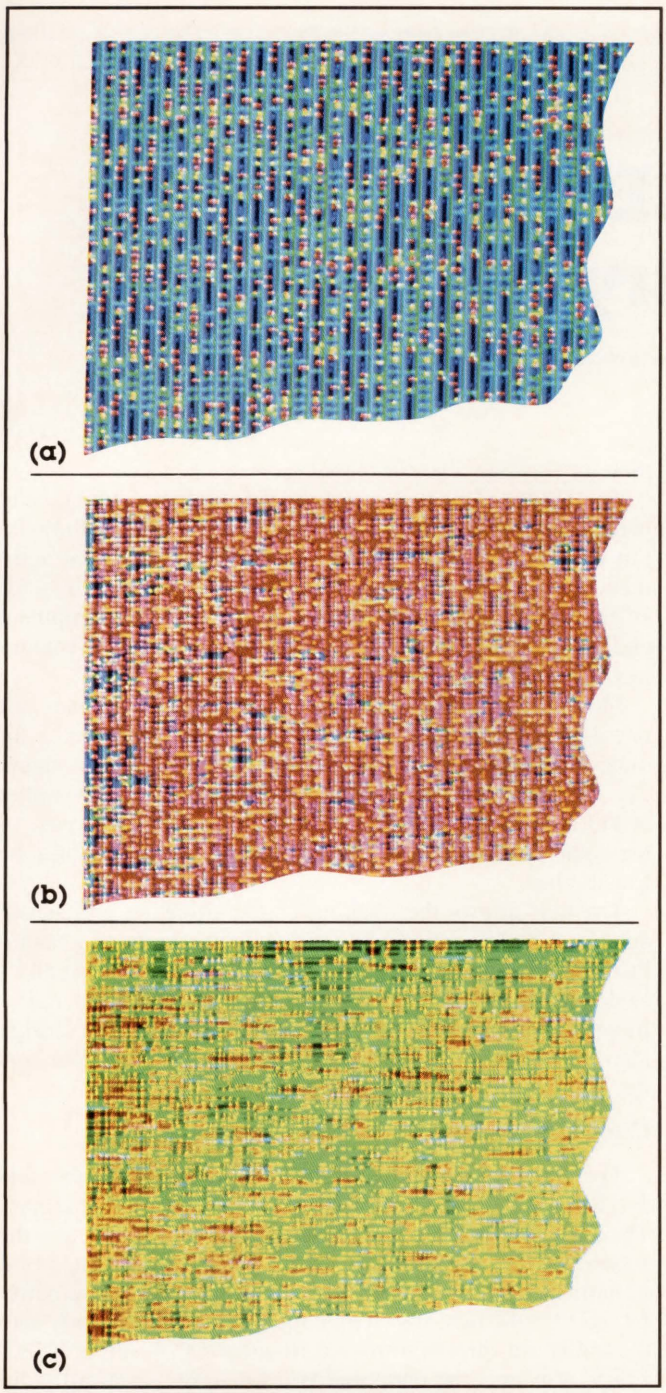

FIGURE 5. Uniform routing in the first layer (a), the first two layers (b), and all three layers (c) of a three-layer design.

A layout system devised for large designs must have a database structure that can be accessed quickly and efficiently by the layout and verification tools. Because access from disk storage is significantly slower than access from memory, a compact database that keeps much of the design information in memory is more efficient. Further, any database must be organized to minimize the number of disk accesses. Even when all of the database can fit in memory, special structures are necessary to allow fast access to blocks of data. The speed of access determines the speed of graphical display, which is fundamental to performing efficient interactive analysis and to editing very large designs.

A Compact Database

TANGATE incorporates a compact database that includes special data structures for fast graphics. One technique used to achieve compactness is in the representation of wires, which account for a major portion of the database. TANGATE achieves compact wire representation by using two distinct representations. In large designs, more than 99.9% of the wires and vias in the design share common attributes. Most have the same widths per layer, use the same vias, and contain no routing loops. TANGATE employs a highly compact representation of these nets to take advantage of these features. The remaining 0.1%, however, demand a high degree of flexibility in widths, via generation, and routing patterns. The database represents these nets to allow the variations, but less compactly, and provides utilities to translate between the two representations.

The special structures for graphics are important for interactive response, as well as for the efficiency of the automatic layout tools. TANGATE allows fast interactive analysis and editing of very large designs on standard engineering workstations without the use of special hardware. Because the structures are embedded within the database, there is no need to convert data. As an example of how the special structures aid efficiency, when the final router routes a subregionthe database interaction is highly optimized, because the database access is similar to that required for graphics.

Results

Over two dozen designs in a variety of technologies, including CMOS, bipolar, and ECL, have been completed using the TANGATE layout system. These designs have ranged from a conventional 1000-gate array in double-layer metal to beyond 100,000 used gates on a triple-layer-metal CMOS sea-of-gates array. Utilization rates vary greatly depending on array architecture, macro design, and netlist. In all cases, the designs have been completed fully automatically with no uncompleted connections at previously unattainable utilizations. Even for designs that contain only random logic, customer benchmarks have produced greater than 60% utilization for double-layer metal and 100% utilization for triple-layer metal. (Utilization rates are of course generally highest for those designs with RAM, ROM, or other high-density functional blocks.) □

Acknowledgments

I would like to acknowledge the special contributions made to the development of this system by the TANGATE team in particular and by the people of Tangent Systems, Toshiba Corp., and Motorola Inc. The architecture of the TANGATE system was designed by Thomas Kronmiller, Eric Nequist, Steven Teig, and Aki Fujimura. The original version of this article was written by John Seaton.

About the Author

Aki Fujimura is the engineering and marketing product manager of TANGATE. Previously, he was at Trilogy Systems and at Honeywell Information Systems. He received a BS in computer science and an MS in electrical engineering and computer science from the Massachusettes Institute of Technology in 1982.

Multilevel EEPLD Implements Biotelemetry System

Erich Goetting, Mikael Hakansson, and Steven Peterson, Exel Microelectronics Inc., San Jose, CA

In the past, to implement a system like the one to be described here, logic designers used PLDs to reduce the number of TTL devices needed as glue logic. But the two-level PLD AND-OR architecture posed significant limitations.

Conventional PLDs could provide only limited logic complexity between an input and an output pin because they were restricted to a level of AND gates followed by a level of OR gates to generate user-programmable functions. Fortunately, new PLDs offer multilevel logic that can include registers, PLAs, ROMs, random logic, and other system building blocks, which can be cascaded to form relatively complex subsystems.

Greater Flexibility

Though most multilevel PLDs are not as dense as gate arrays, their flexibility allows the user to define complex logic using either gate array or standard PLD design techniques. Furthermore, a user can compile, test, and program the chip in less than three minutes with a PC-based development system.

Thanks to chip-packing algorithms in PLD design software and the inherent flexibility of multilevel logic, the new PLDs use on-chip gates efficiently. In contrast, fixed-AND PLDs have a fixed number of gates available for each output pin and if one does not use all the gates for a particular logic function, they are simply wasted.

When these new PLDs are implemented in electrically erasable technology, as is the case with Erasic devices, their gates can be programmed, tested, and reprogrammed up to 10,000 times, and each design can be customized for a specific application without requiring a new test procedure. This flexibility is useful for adding security features, configuration information, and serial numbers in inventory applications.

Counting Livestock

Figure 1 shows the block diagram for a remote data transmitter, the key element of a fairly complex and unconventional application—tracking livestock—that exploits the advantages of the Erasic CMOS PLD. A rancher could track tens of thousands of cattle carrying biotelemetry systems built around the transmitter. As the cattle pass a certain gate, for example, the rancher can identify each animal from the serial number it transmits, and he can remotely check each animal's body temperature and pulse. Such automated checks can dramatically improve inventory control and veterinary care, thereby slashing livestock losses.

The ability to read a remote serial number automatically greatly speeds inventory control and adds other capabilities. For example, if units moving along a conveyor could automatically transmit serial numbers to a stationary data recorder, this information could be used in a record of the shipment and it could be added to a database to update inventory records automatically.

Most of the tracking and monitoring system fits into just one 24-pin Erasic device supported by two serial analog-to-digital converters and a few passive components (see Figure 2). The heart of the system, the remote data transmitter (RDT), does not resemble a traditional PLD design because of the significant amount of internal logic cascading within the Erasic chip.

The RDT allows the tracking of identification and sensor data from mobile objects like railroad cars, parts on a manufacturing line, or in this case livestock. Powered by a small rf-to-dc converter on the animal, the RDT transmits radio-frequency–encoded digital data to a receiver. The design identifies each animal and, with the aid of sensors, monitors the animal's temperature and pulse.

Checking Pulses

The RDT on each animal transmits one 32-bit number and two 8-bit numbers. The 32-bit number identifies the animal. The first 8-bit number represents body temperature; and the second, pulse. A transmitted 64-bit word includes the 32-bit ID number, the 8-bit temperature, the 8-bit heart rate, a parity bit, and 11 idle bits, which give the receiver time to lock onto the middle of three transmitted frequencies. A single 78C800 Erasic transmits the data, and two low-cost, serial A/D converters digitize the body temperature and pulse.

The system on the animal comprises a power converter, the two A/D converters, a single Erasic PLD, and two sensors. The Erasic includes a 32×1-bit EEPROM, a data multiplexer, a parity generator, a clock generator, a sequencer, an rf transmitter, and control and interface logic for the converters.

Operation begins when a radio beam, focused from a hand-held receiver/transmitter no more than 5 feet away, powers the circuit. The focused radio beam strikes a small coil in the rf-to-dc converter on the animal. The signal from the coil is rectified and regulated. The coil in the converter and the coil in the hand-held rf transmitter act together like a loosely coupled transformer.

The converter's dc output powers the Erasic and the A/D

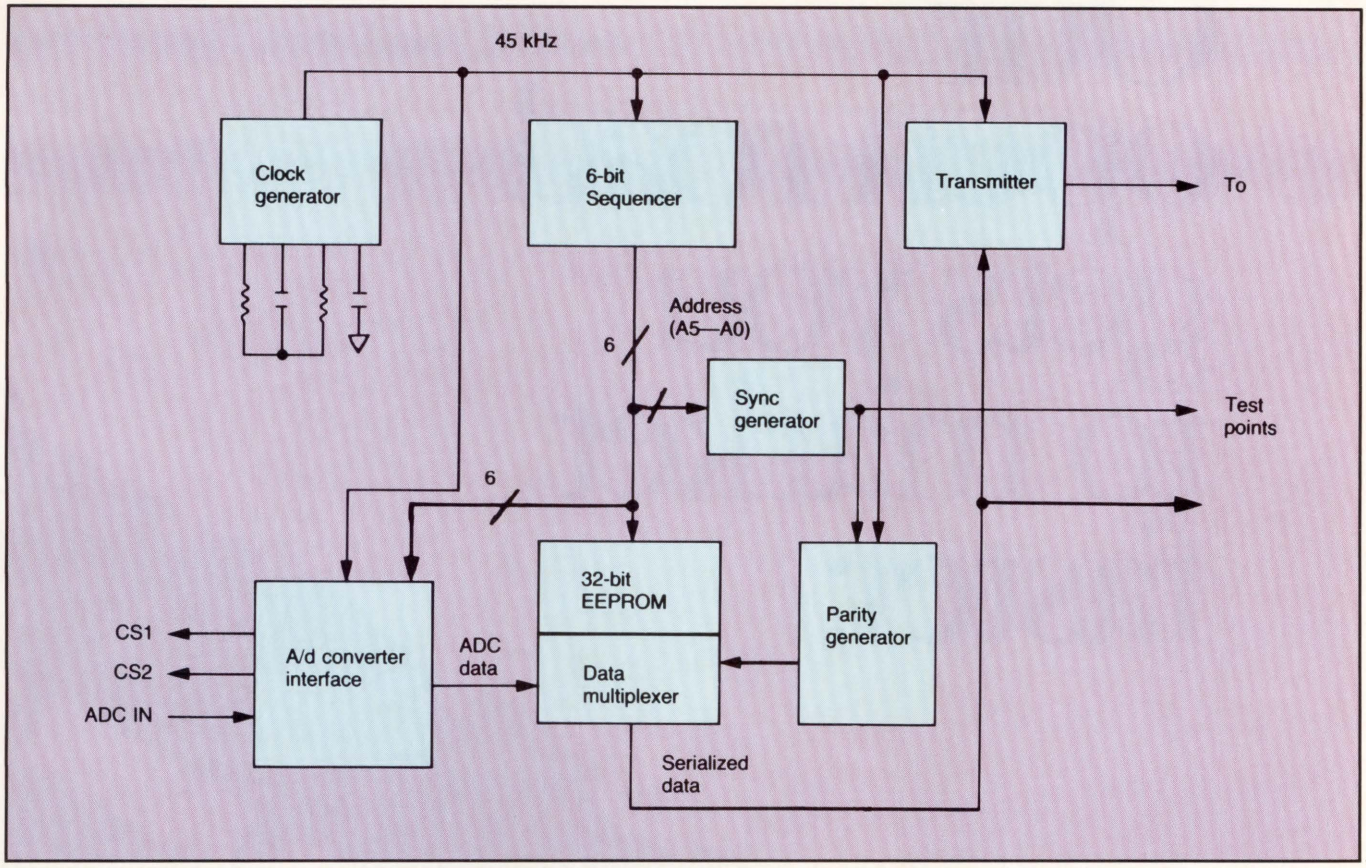

FIGURE 1. Block diagram of the remote data transmitter circuit, implemented with an Erasic PLD.

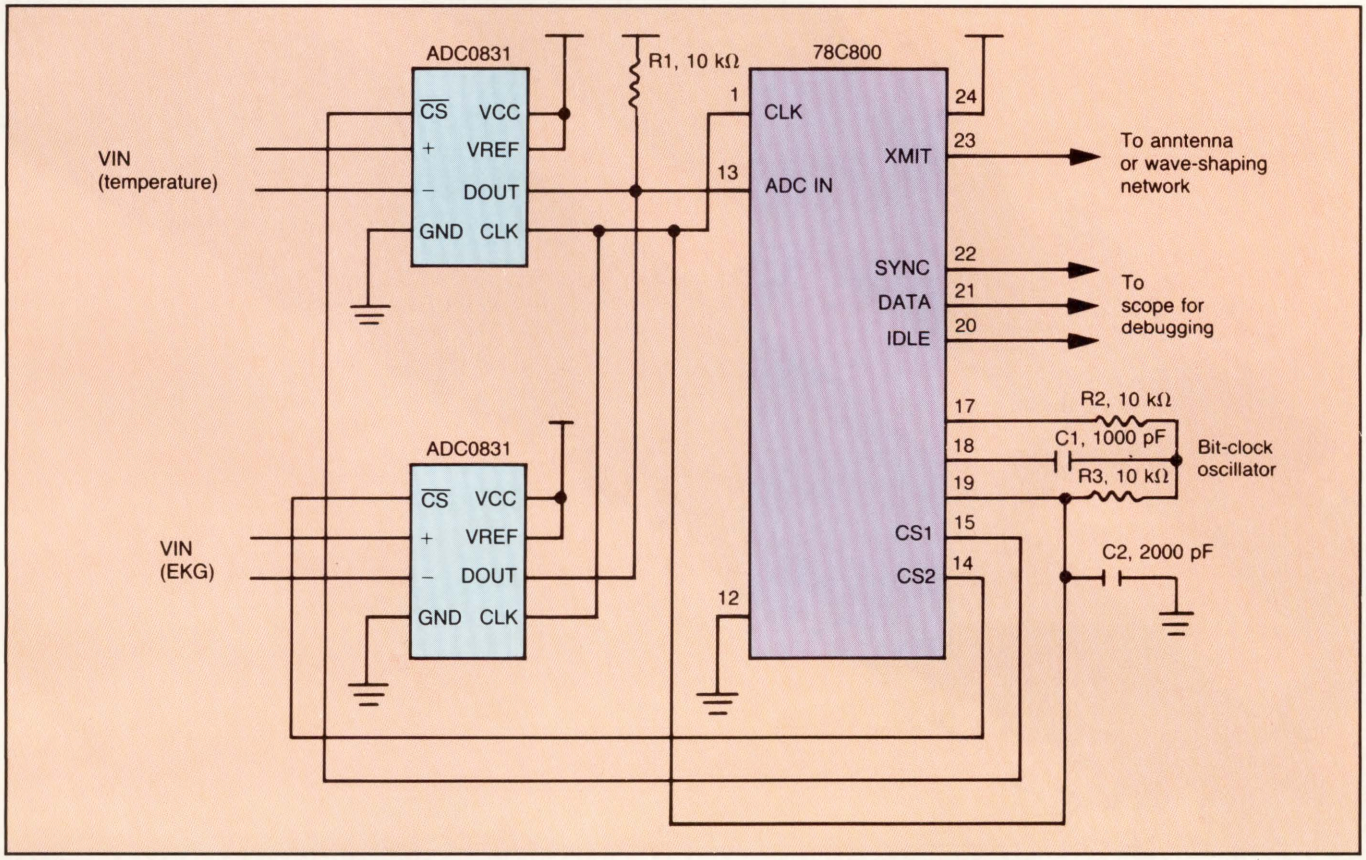

FIGURE 2. The heart of the inventory and biotelemetry system uses one Erasic and two converters.

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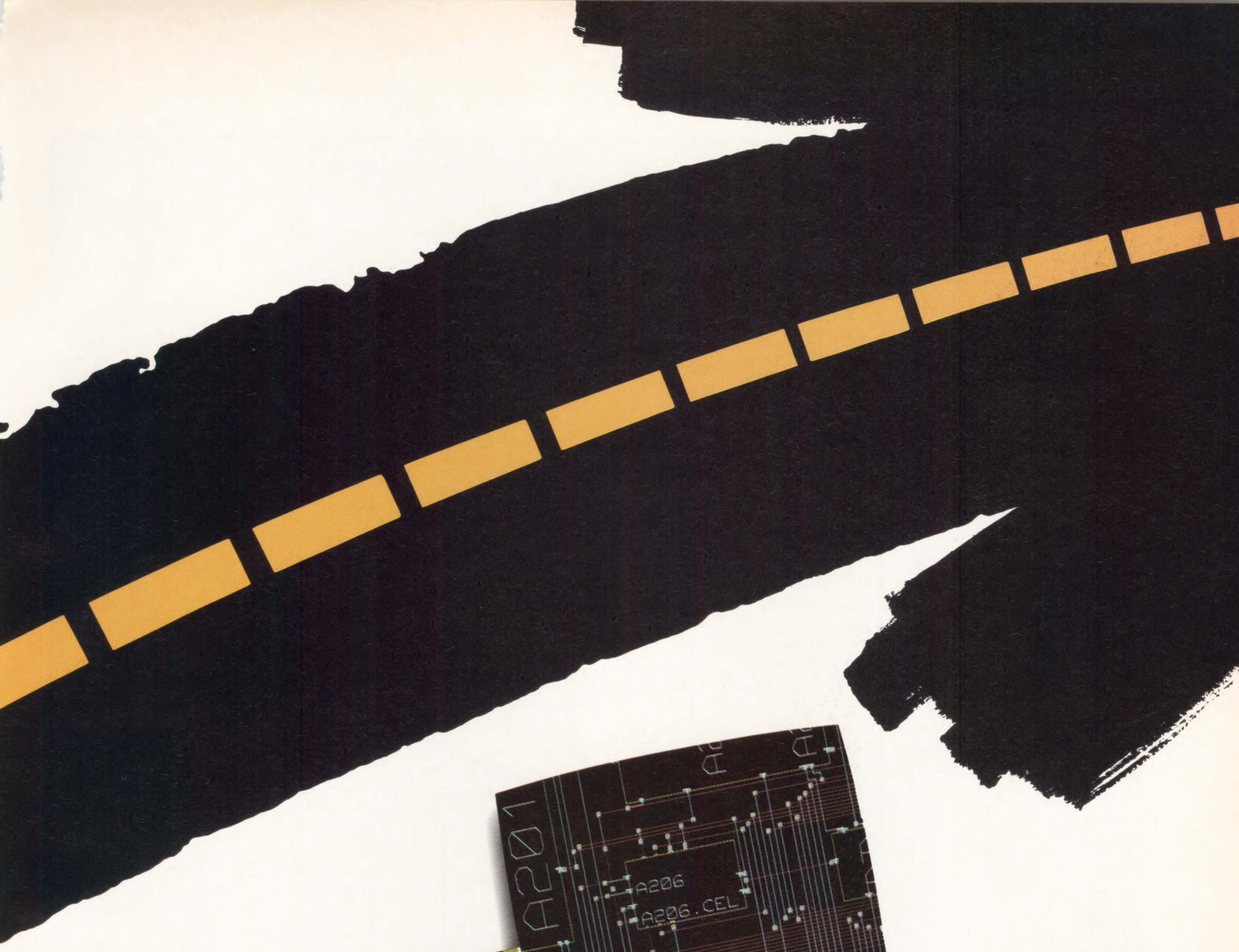

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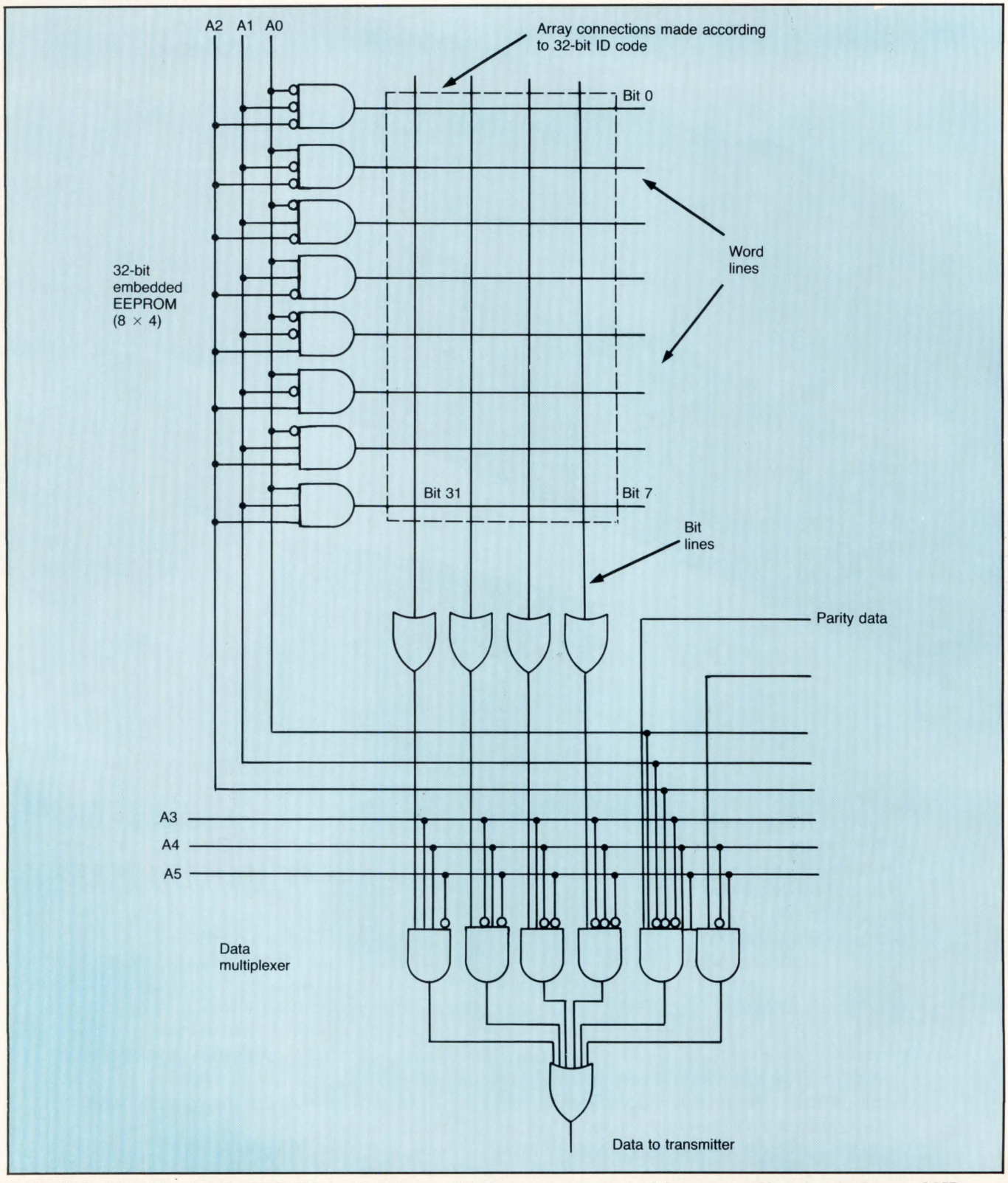


FIGURE 3. The 32 × 1-bit EEPROM and data multiplexer are created by cascading logic in an AND-OR-AND-OR sequence.

converters. In total, they consume no more than about 75 mW. When the power turns on, the clock starts running and the sequencer begins counting. The transmitter sends a bit to the receiver for each clock cycle.

The first information transmitted is the 32-bit ID number, which is stored in the EEPROM (see Figure 3). The ID number moves to the transmitter through the data multiplexer one bit at a time. (The ID number in the EEPROM is specified by eight

hexadecimal characters either at compilation time or during device programming.)

The Transmission Sequence

After the ID number is transmitted, the sequencer selects the first A/D converter, which digitizes body temperature; then the second, which encodes the pulse rate. After these data have been transmitted, the sequencer addresses the multiplexer, which sends an even-parity check bit, after which the transmitter sends out a reference frequency for 14 clock cycles. Then the 64-bit sequence begins again with the transmission of the ID code. This sequence is repeated until the animal passes from the range of the radio beam or the rancher selects another animal.

The data multiplexer selects the source of bits to go to the transmitter based on addresses it receives from the sequencer. The sequencer also controls the timing of the A/D converter interface and the transmitter. The data multiplexer and EEPROM are cascaded directly, without any intermediate pins. The two in tandem look like an AND plane going into an OR plane feeding directly into another AND plane, finally multiplexed down through an OR gate.

Parity generation is accomplished with a buried JK flip-flop that toggles every time a 1 goes to the transmitter. An even number of 1s toggles the JK flip-flop to a 0 state; an odd number toggles it to a 1 state. The parity generator is reset at the end of each 64-bit sequence.

The JK flip-flop is efficient for building counters because it has both toggle and hold modes in addition to set 0 and set 1 modes. Its use also simplifies the design of sequencers and state machines in general. To achieve the same results, PLDs with only D flip-flops (the vast majority) require valuable array logic to implement toggle and hold modes.

Spending Money to Save

The Erasic's transmitter uses three ring oscillators. Because their frequency varies with temperature and voltage, ring oscillators are seldom used for data transmission. But in this application, the driving factor is cost and transmitter size, so that it pays to spend more on a few hundred receivers in order to save lots of money on tens of thousands of transmitters.

The ring oscillator is an extremely low-cost transmitter. Its natural frequency variations are tracked by the phase-locked loop circuitry in the receiver. Conventional LC or quartz oscillators, though more stable, would add unacceptable cost and size.

At any one time, the transmitter transmits one of three frequencies. A 1 is transmitted when the medium frequency (nominally 20.8 MHz) is followed by a high frequency (nominally 41.7 MHz). A 0 is transmitted when the medium frequency is followed by a low frequency (nominally 13.9 MHz). The data output bit rate is 45 kHz, and data sequences are transmitted 700 times per second.

The transmitting antenna is a 4-inch piece of wire connected to an output pin on the Erasic. The receiving antenna is in the hand-held transmitter/receiver. In field tests, the transmission range extended to about 20 feet.

The interface with the A/D converters is defined using ABEL's set operations and their relationships. The inputs to the converters are edge-sensitive, so that flip-flop sync circuits ensure that the outputs will be free of glitches during sequencer transitions.

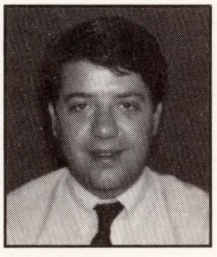
Three additional pins on the Erasic are used for testing and debugging.

It is relatively easy to create ASIC circuits using Erasics with Data I/O's ABEL. MultiMap and MultiSim software from Exel Microelectronics enhance ABEL to allow it to handle multilevel logic compilation, device mapping, and simulation. These programs are completely transparent to ABEL users.

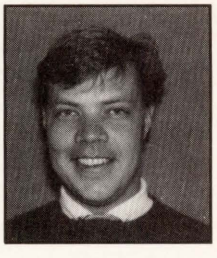
By taking advantage of traditional design software, an engineer can use conventional PLD design techniques. This means that users of traditional AND-OR PLDs can easily add multilevel logic to their repertoire by cascading logic structures within the ABEL design file. These structures can include Boolean equations, state diagrams, truth tables, set operations, and macros. In addition, designers familiar with TTL or gate-level schematic design can use Exel's TTL macro library and Data I/O's schematic capture. Captured schematics are compiled into ABEL equations and subsequently mapped into the Erasic chip.

Regardless of the design methodology, as the logic is compiled into the device, it is streamlined with logic packing algorithms that eliminate unnecessary and unused logic. For example, if the designer specifies an up/down counter but uses it only as an up counter, the logic associated with the down counter is automatically eliminated. Consequently, an engineer can design efficiently without having to worry about every last gate. □

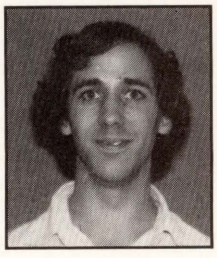
About the Authors



Erich Goetting manages the EEPLD program at Exel Microelectronics, where he is responsible for PLD architecture, device design, design tools, and customer support. His areas of interest include high-density, high-speed circuit design techniques and the interaction between PLD architectures and software tools. Erich holds a BS in applied science and a BS in finance form the University of Pennsylvania and an MS in computer science from the University of Southern California.



Mikael Hakansson is a senior systems engineer, responsible for research and development of EEPLD design tools. His areas of interest are logic synthesis and algorithm design for logic optimization and simulation. He holds an MSEE from Lund University of Technology, Sweden.



Steven Peterson is an associate systems engineer, working on EEPLD applications and design methodology, Steve's interests include the application of cell library techniques to EEPLD design, EEPLD programming, and test methodologies. He holds an associate science degree from Sierra College.

The Integration of Fiber Optics into Network Systems

Mark Stansberry, Cypress Information Resources, Los Gatos, CA

System designers considering the inclusion of network nodes within their application have a number of evolving technical issues to contend with: the arrival of very high speed gallium arsenide ICs, the dawning of the fiber optics age, and the globalization and standardization of a world information network. Designers should be familiar with not only the fundamentals of network node design, but also the dynamically changing standards and technology, including optoelectronics and the evolution of integrated electronics for fiber-optic networks.

The requirements for networks are becoming more stringent. Throughput requirements are increasing because of high-speed superworkstations and the file-transfer–intensive software applications that run on them. Network nodes must also become compatible with other networks, such as in telecommunications. Specifically, network nodes must incorporate optoelectronics to hook up to fiber-optic cabling.

Central to the issues cited above are the type of standard IC building blocks available for network nodes. Advanced Micro Devices Inc. (Sunnyvale, CA) has developed fiber-optic network node ICs whose applications range from impervious high-security networks to futuristic, "all-in-one" local-area networks that combine video, graphics, data, and voice communications. Additionally, Siemens Semiconductor (Santa Clara, CA) is making IC components for plastic fiber-optic LANs for emerging automobile and trucking network applications. Rockwell International Corp. (Newport Beach, CA) and Honeywell Inc. (Colorado Springs, CO) are developing revolutionary GaAs chips that employ optical detectors and receivers as replacements for I/Os on VLSI chips. These optical devices reduce chip power, increase fan-out capability, and connect directly to fiber-optic cable. These forthcoming ICs point to a future where light will be the medium of interconnection from the system level down to the internal, chip level.

Network Node Design

When building a network node in a system, the medium or media, topology, and protocol all must be considered so that the node will meet users' needs. For example, industrial, military, and medical applications often require token-passing protocols, whereas office applications can often suffice with carrier-sense multiple-access (CSMA) protocols. The first set of applications requires access to the network bus within a fixed amount of time. On the other hand, the minor inconvenience of having to retransmit data on a small office LAN might not justify the added cost of a token-passing scheme. However, adding more nodes in the future may make the office LAN so inefficient that it will be virtually useless.

When designing a network node, the following parameters must be considered: the number of nodes in the network, the frequency of transmission, the average length of the data packet, the propagation delay through the network, the need for guaranteed access to the network bus, the desired rate of data transmission and throughput efficiency, the maximum distance between nodes, the maximum cabling distance of the entire network, the tolerated data error rate, the LAN's operating environment, the need to support multiple standards, the procedures for handling network faults, transformation into a optical cabling system, the efficiency of the transmission, the cabling costs for the network, and the ease of redesign for new standards.

The specification of those parameters will limit the choice of network node designs for the proposed target application. Table 1 summarizes the various network node choices for different standards and protocols.

Fiber-Optic Networks

The medium used for the network is also a concern. The cabling dictates the delay and associated jitter, which affect the error rate and system throughput. Proper cabling, therefore, simplifies the hardware and protocol requirements. All networks except for optical networks use twisted-pair or coaxial cabling, with different limitations on length, noise protection, and cost.

As the price of fiber-optic cabling drops toward the cost of copper wire cabling, the medium will find increased use because of its small size and the benefits of using light as the carrier. For example, fiber-optic cable is about 50 times lighter, and much smaller, than coaxial cable for a given bandwidth. Fiber optics also offers these advantages: high immunity from crosstalk and interference; nonconductivity: low attenuation; low propagation delay; and low bit-error rates.

Fiber-optic cable also is superior to coaxial cable because it does not suffer from ground loop problems or emit electromagnetic energy. It also requires only tens of milliwatts to drive a fiber-optic cable, whereas a transceiver for an Ethernet coaxial cable dissipates about 100 mW.

Fiber optics is becoming the preferred medium of network designers. The onslaught of new system-level products is pushing new implementations. Several workstation compa-

	Protocol	Data rate (Mb/s)	Maximum number of nodes	Maximum network length	Maximum node-to-node distance	Number of data field bytes
Ethernet	CSMA/CD	10	1024	2.5 km	500 m	1518
Cheapernet	CSMA/CD	10	120	925 m	185 m	1518
Starlan	CSMA/CD	1	40	2.5 km	250 m	1518
PCNet	CSMA/CD	2	72/1000*	1000 ft/5 km*‡	Not available	1518
FDDI	Token	100/200	500	100 km	2 km	4500
Token bus	Token	5/10	32	10 km	700 m	8191
Token ring	Token	4	250	1 km^2	300 m	Unlimited
Intel	CSMA/DCR	20	63	2.5 km	2.5 km	1518

* With IBM PCNet translator unit
‡ Radius

TABLE 1. A comparison of network standards.

nies like Sun Microsystems Inc. (Mountain View, CA) and Apollo Computer Inc. (Chelmsford, MA), are planning fiber-optic interfaces for their systems. Du Pont Connector Systems (New Cumberland, PA) has developed a fiber-optic network for Apple's Macintosh computers. The System Finex from Fibronics International Inc. (Hyannis, MA) offers a fiber-optic LAN built around the Fiber Distributed Data Interface (FDDI) standard (see Figure 1).

FDDI has gained considerable support from IC vendors. It uses a dual-ring structure, with a 100-Mb/s data bandwidth, a 100-km maximum ring cable length, a 2-km station-to-station cable distance, and as many as 500 network nodes.

The dual counterrotating ring topology, using primary and secondary rings, provides fault protection and a 200-Mb/s peak data transfer rate. The standard also allows expansion of the ring network to support both front-end and back-end branches off the main ring. In this configuration, the branches can operate independently or be patched, through an optical switch, into the main ring upon request.

The components of an FDDI system node include an optical transceiver link to the fiber-optic cable, a receiver and transmitter, a media access controller, a data buffer controller, a datapath controller, and the fiber-optic cable. A fiber-optic network in a ring configuration is economical because it requires no repeaters. Each node is regenerative; it receives the data and retransmits it to the next node over economical "multimode" fiber-optic cable.

A fiber-optic network includes several design components such as the IC node electronics, the interconnects, and the links to the fiber. When designing the network, one must allow for the losses in the interconnects.

Basic fiber-optic physical-medium components that affect the losses are the optical transmitter, the optical receiver, the T coupler, the star coupler, the optical switch, and finally the source and detector connectors. The transmitter determines the starting power for the fiber-optic cable and connectors. The LED transmitter (an LED with driver circuitry) has a typical power level of 100 to 1000 μW (−20 to 0 dBm). Losses range from 0.5 to 1 dB for the splices to 16 to 18 dB for the star coupler, plus, for medium-grade "multimode" cable, between 1 and 5 dB/km.

For a rough power analysis, all of the losses must be subtracted from the transmitter's output and compared with the receiver's sensitivity. In addition, losses from the aging of the components should be considered for reliability. When the losses become too large, they affect the signal-to-noise ratio enough to increase the bit-error rate, reducing system throughput.

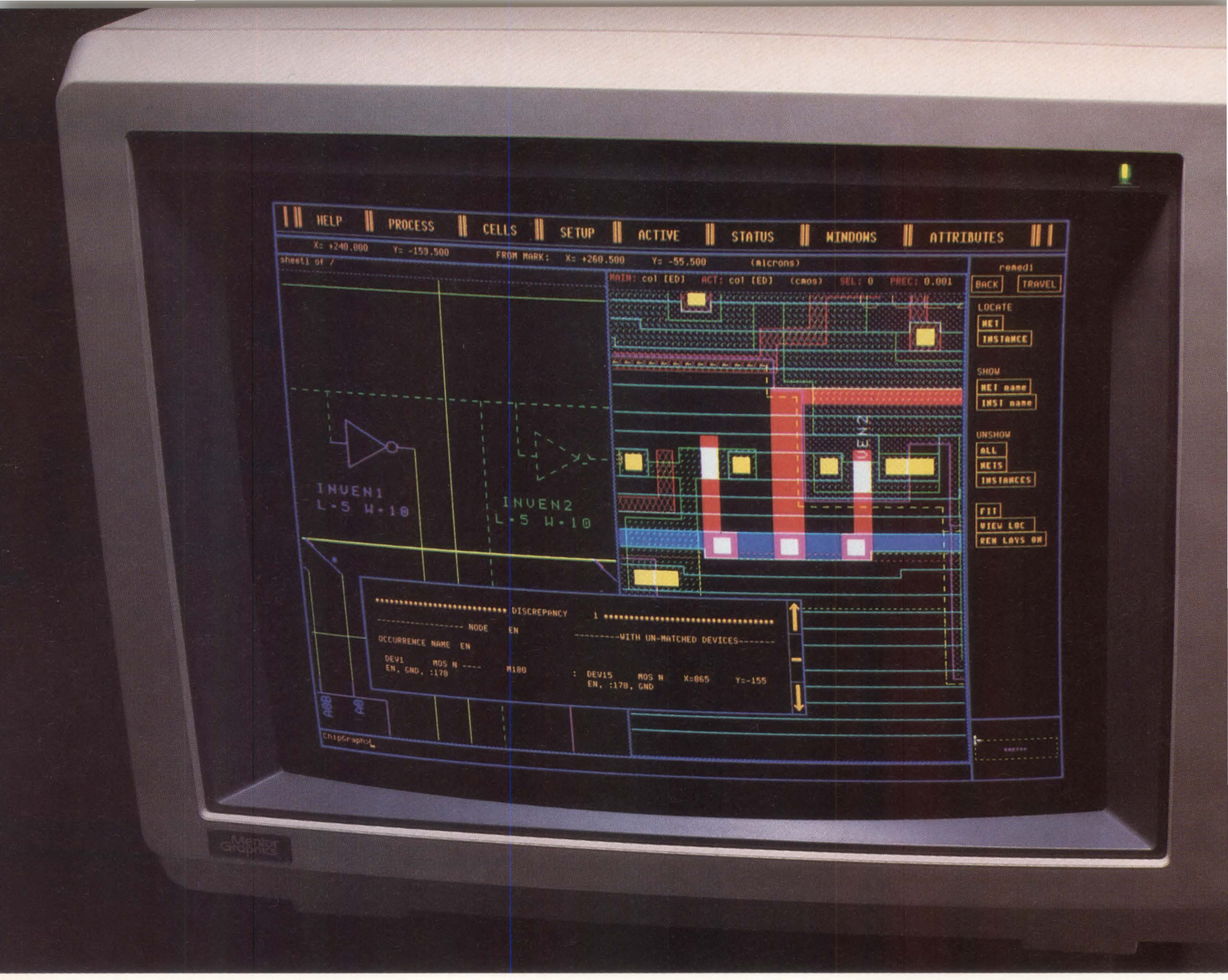
Fiber-Optic ICs

New ICs for the fiber-optic LANs are under development at Honeywell, Rockwell, and the Defense Advanced Research Projects Agency (DARPA). These GaAs ICs incorporate standard electronic components such as multiplexers, demultiplexers, error correction units, and optical detectors and receivers that can be directly connected to fiber-optic cable or to waveguides. Optical switches, both 32 × 32 and 256 × 256, also are under development.

Fiber-optic ICs are already offered by AMD (its FDDI chip set), GigaBit Logic Inc. of Newbury Park, CA (the 16G040 clock and data recovery circuit), and Signetics Inc. of Sunnyvale, CA (the NE5212 receiver). AT&T Technology Systems (Berkeley Heights, NJ) offers an LED-based lightwave data link, the ODL200, which is an FDDI transceiver with a transmission rate of 40 to 220 Mb/s. Crystal Semiconductor Corp. (Austin, TX) has a fiber-optic transmitter and receiver (1.544 Mb/s), which incorporates an encoding and decoding scheme as well as clock and data recovery.

AMD's five-chip set includes the Am7984 ENDEC transmitter, the Am7985 ENDEC receiver, the Am79C83 FORMAC (fiber-optic ring media-access controller), and the Am79C81 RAM buffer controller (see Figure 2).

The operation of the chip set in a dual-ring structure requires two transmitter and receiver chips. The ENDEC transmitter chip performs parallel-to-serial conversion and encoding for transmission. Conversely, the ENDEC receiver



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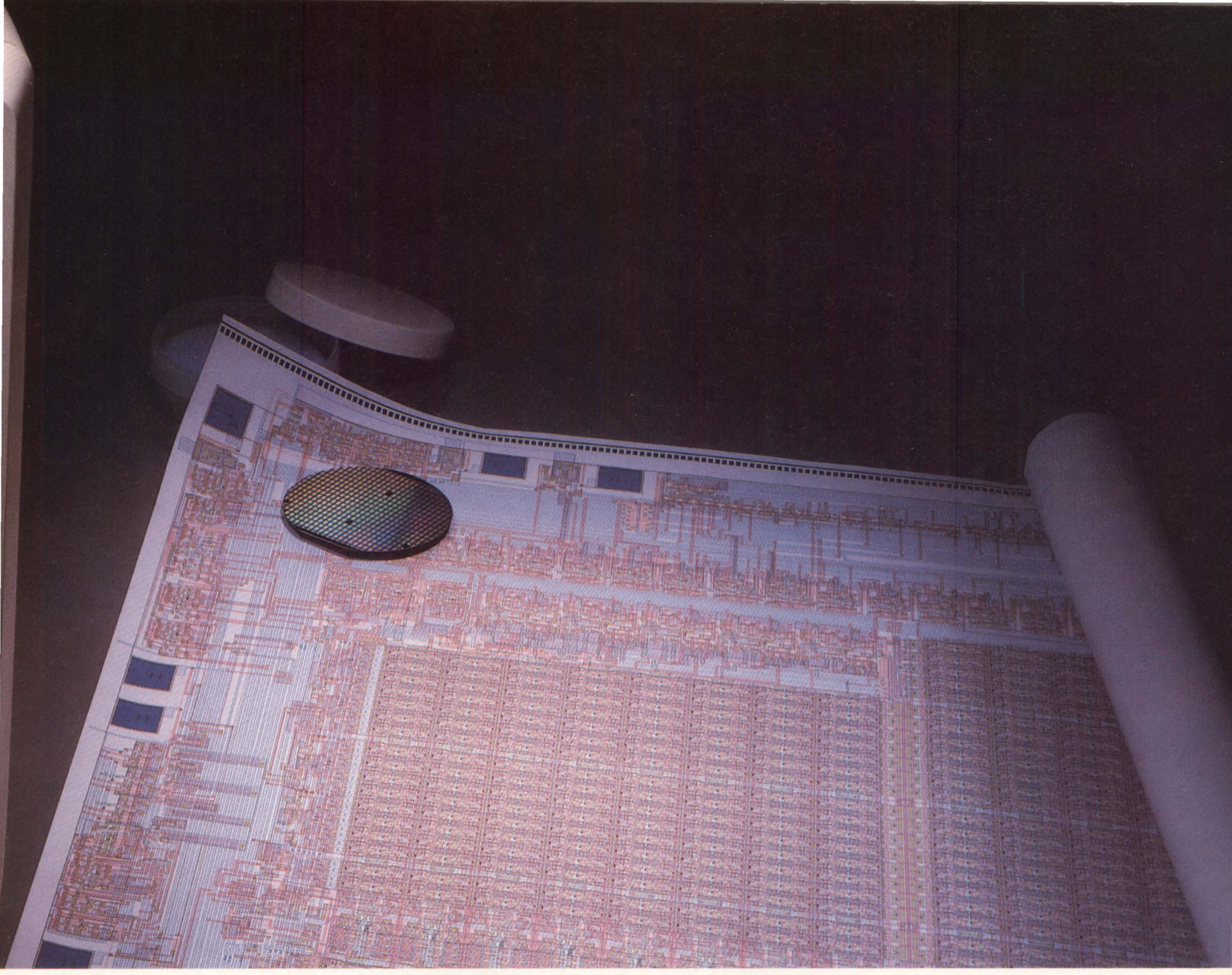

Structured Chip Design (SCD), a hierarchical approach to physical layout, removes much of the unnecessary and confusing mask data, while retaining correct functionality and interfaces.

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performs decoding of the serial data stream from the fiber-optic cable, serial-to-parallel conversion, and clock and data recovery. It has an elasticity buffer for retiming of the incoming data, because FDDI uses a distributed clocking system.

The FORMAC chip performs packet reception and transmission, removal of the the packet from the ring, address recognition, frame-check sequence generation, and network and frame status handling.

The RAM buffer controller supports the overall throughput of the system by controlling transfers between the datapath controller and local memory while simulataneously permitting transmission and reception of data to and from the link. The local memory allows the node to assemble and disassemble packets locally during the transmission and reception of packets to or from the network bus. The RAM buffer controller can transfer a 32-bit word every 160 ns.

The datapath controller converts 8-bit words received from the receiver into a 32-bit-word format. It also converts 32-bit words sent by the RAM buffer controller into 8-bit words that are then sent to the transmitter for serialization and encoding.

The chip set employs a "list" packet memory system, with a maximum memory size of 256K × 36 bits that allows for the transmission of more than one packet at a time. The external buffer memory is divided into three logical areas; one area supports synchronous transmissions data, another holds asynchronous transmission data, and the third is for packet reception.

Asynchronous transmission is the primary mode of data transfer in a fiber-optic system. Asynchronous data can be sent nonsequentially: A packet that is a portion of a larger file can be sent and transmission stopped while another node transmits; then transmission of remaining packets of the file is initiated. Synchronous data, on the other hand, cannot afford this luxury. The reason is that synchronous data is voice or video data, which must be continuous for telephone and CATV applications.

The FORMAC chip oversees access to the ring through three timers—the token ring timer, the token-holding timer, and the transmission-valid timer. The token ring timer holds the token rotation time, which is determined on ring initialization. During ring initialization, the network determines which node will need to transmit most often and then determines an average token rotation time so that the most demanding node in the network will be able to transmit whenever it has data to send. In other words, an average token rotation time is determined and a timing algorithm is set up so that the token will rotate around the ring fast enough to meet the requirements of the most active node. The token-holding timer sets the time allowed for asynchronous transmission of each node while the transmission valid timer sets a maximum limit on the time to transmit.

After the initialization process, the token circulates around the ring until a station has a request for transmission. When the station that needs to transmit receives the token, it appends to it a data packet, a frame-check sequence field, and other bits such as the preamble, the source address and destination address. It sends this data frame and immediately afterward releases the token to the ring (as opposed to waiting for the data frame to return all the way around the ring as with the token-ring standard).

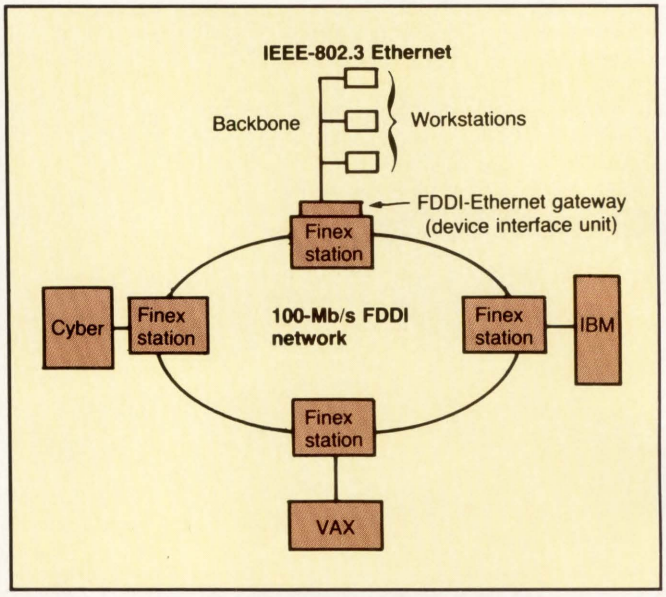

FIGURE 1. The System Finex optical LAN.

Also, at the time the token is received by the station, the time in the token rotation timer (that is, the time since it last received a token) is loaded into the token-holding timer and the token rotation timer is reset to zero and begins counting again. The data frame circulates around the ring until it reaches the original transmitting station, where it is then stripped off. At this point, the token is passed to the next station.

Applying Fiber-Optic LANs

One of the main challenges for system designers is the conversion of copper-cable LANs to fiber-optic LANs. Ring networks are a natural for fiber-optic conversion because they can use regenerative optical links in their nodes and do not require repeaters. Bus and tree topologies, because they require a T coupler for network branches, produce inordinate loss when implemented in fiber, so that they require the use of expensive repeaters.

For Ethernet conversion, star topologies are possible for fiber implementation. There are four basic approaches being examined for fiber-optic Ethernet networks. These include a passive star with collision detection by signal analysis, a passive star with collision detection by time-domain analysis techniques, an active star that offers 100% collision detection, and a complex hybrid star (Rowarth, 1987). At this time it appears that the active star configuration will be employed because its 100% collision detection does not entail undue network complexity. Currently, BICC Data Networks (Hemel Hempstead, Herts., UK) offers a system (Isolan) that converts Ethernets to optical-fiber cabling systems.

Another application of fiber optics is to connect peripherals like disk drives or printers to host computers. For such applications, AMD's Taxi chip set converts parallel data into serial form and provides an interface with the optical link. At the other end, it converts the serial data into parallel and temporarily stores them. This application allows for 100-Mb/s direct serial interconnection of point-to-point disk drives and printers to host computers, replacing parallel transmission through copper wire.

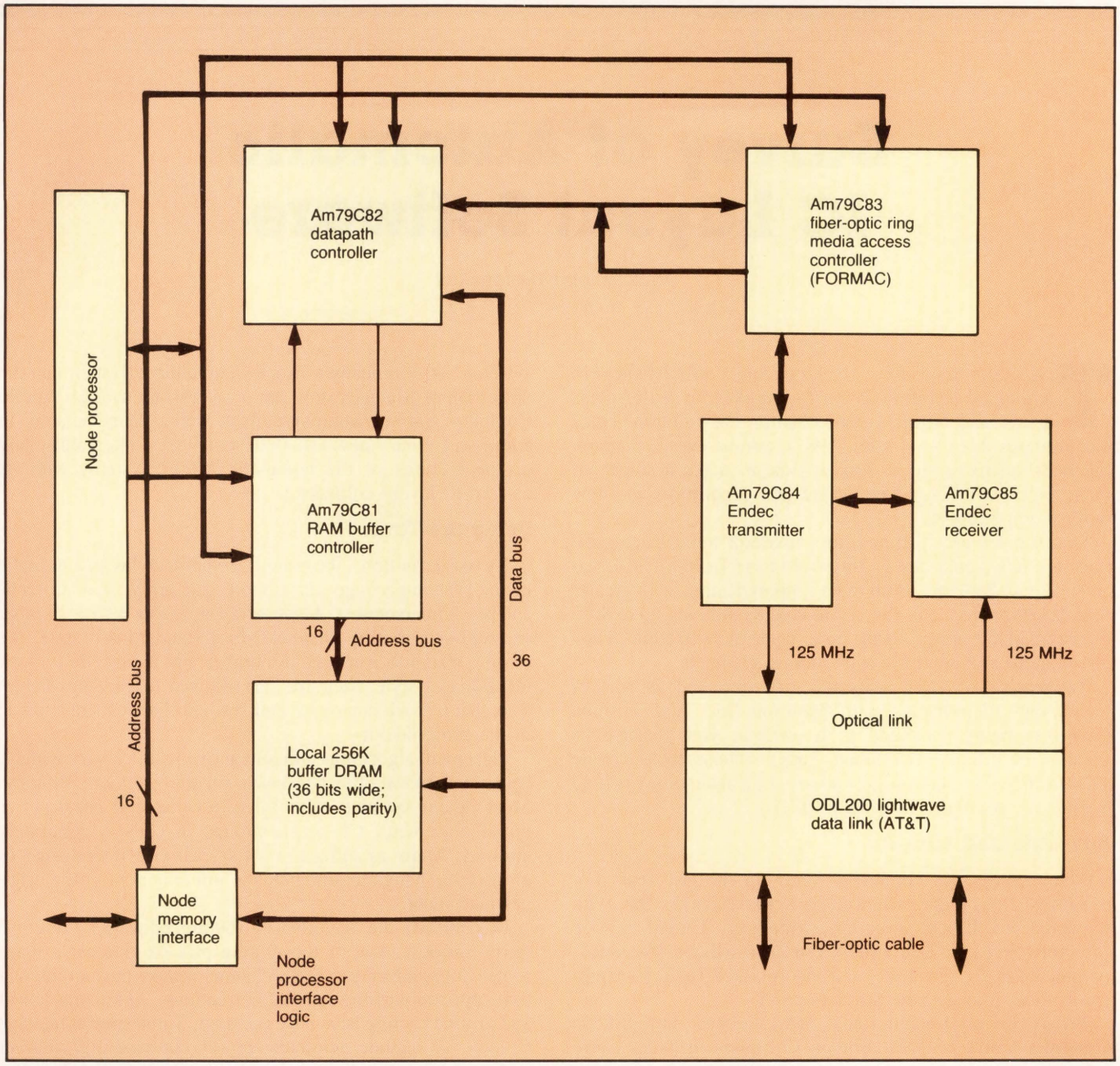

FIGURE 2. The basic setup for an FDDI network using AMD's fiber-optic chip set.

One of the significant applications of the fiber-optic medium is in machinery that generates high voltage and current transients, such as in automobiles, appliances and industrial equipment. Plastic fiber-optic cable with fiber-optic LED sources and receivers (such as Siemens's SFH 750 transmitter and SFH 250 receiver) may be employed in such equipment to link microprocessor equipment with local machinery. Plastic fiber-optic cable is preferable to copper cable in this application because it will not spark when cut, it will not transmit high voltage and current transients to sensitive VLSI circuits (a major problem with automobile electronics), and it offers high noise immunity as well. Plastic fiber-optic cable, however, suffers from high attenuation (>200 dB/km), but it is inexpensive and can be used effectively to transmit data at 1-MHz rates at distances on the order of tens of meters. □

Reference

Rowarth, D., and N. Howe. 1987. "Isolan: A Fibre-Optic Ethernet," *Electronics and Wireless World,* August 1987.

About the Author

Mark Stansberry took his BSEE at San Jose State University, then joined Fairchild Semiconductor as a test engineer. He moved to Exar Integrated Systems as an applications engineer and later to National Semiconductor as an ASIC applications engineer. In 1986, he founded Cypress Information Resources, a consulting company specializing in technical literature, market research, and product design.

Survey of Automatic IC Layout Software

VLSI Systems Design Staff

Two major trends have emerged from a turbulent year in automatic layout tools for ICs: support for sea-of-gates arrays and business consolidation. In addition, since our previous directory (April, 1987), almost every company has been restructuring its product line to make it stand out from the crowd. They have added new algorithms and new workstation support.

Sea-of-gates architectures, an important trend in gate arrays, are now supported by improved tools from Silvar Lisco and Tangent Systems. Both tools support designs with greater than 100,000 gates and can create layouts utilizing up to 80% of the available gates, using three-layer metallization. They also handle architectures with routing channels.

Tangent's TANGATE software, first revealed as part of technology parternships with Motorola Inc. and Toshiba Corp., is being packaged as a product. But because its features are still in development, Tangent chose not to include TANGATE in these tables. (For a look at the technology behind TANGATE, see the article on p. 22.)

Buy-Outs and Mergers

Many companies combined forces in the last year. For example, CAECO Inc. acquired DeNeis Resources Inc. with its respected Blocks program. Similarly, United Silicon Structures Inc., the U.S. arm of European Silicon Structures, bought Lattice Logic Ltd., and incorporated Lattice's Chipsmith tools into its new SOLO tool set.

When Silicon Design Labs (SDL) merged with Silicon Compiler Corp. to form Silicon Compiler Systems Corp. (SCS), the two product lines were strengthened by: satisfying the needs of both the professional IC designers (SDL's customers) and the ASIC users (Silicon Compiler's customers). SDL's tools are being used to enhance SCS's Genesil compiler.

SDA Systems and ECAD Inc. are now one company. However, the name and product line of the combined company is as yet unannounced. But the details of the product line integration are expected to be unveiled at the Design Automation Conference in June.

We welcome GE Solid State into this year's directory. Its acquisition of RCA brought GE the VITAL design tool set, which was developed by RCA for its ASIC line. VITAL usersdesign gate arrays and standard-cell ICs built from macros in GE's libraries, include the Advancell standard-cell libraries. Also, VITAL, with its focus on ASICs, does not compete directly with GE's Calma product line.

As for Calma, there's good news for users of its layout systems. The company's Block Interconnect System and the newer Block Manager now run on workstations from Apollo Computer and Sun Microsystems as well as Data General. In addition, Calma's new EDS III design system integrates many of the features of the automatic layout systems with its custom-IC layout software.

Using the Tools

By our definitions, there are three basic styles an automatic layout system package can support: gate array, standard-cell, and block interconnect. A gate array style uses a fixed number of fixed-size routing channels. In a standard-cell style, the routing channels can vary in number and in size. In a block interconnect style, they are also allowed to vary in orientation; that is, both horizontal and vertical channels are allowed in the same layout.

Placement algorithms and interactive features vary widely, because there is little consensus on the optimum strategy. Most layout systems offer force-directed and constructive initial placement. Clustering groups of cells is commonly allowed. Many systems also offer pairwise interchange or group interchange to automate the improvement of the original placement.

In contrast, the majority of routing packages present a fairly uniform view of the routing process. Expect a maze router, a global router, and a channel router, plus an interactive editor to perform manual corrections. Automatic power and ground routing is usually standard. Some special features to look for include automatic power bus tapering, contour routing, and routing based on delay analysis. Some packages are set up so that you can manually edit routes and compact as you go. We are also beginning to see, within products like Valid Logic Systems' Compose and ECAD's SYMBAD, the ability for the user to write routines that control the execution of layout programs—in effect, to encode the designers' practices in the product.

Automatic layout systems must receive their netlists from one source and deliver completed designs to another. Interfaces for standard input and output formats are increasing, as companies learn that proprietary formats discourage user acceptance rather than enhance product loyalty. This year some companies, such as SCS, Silvar Lisco, SDA Systems, and Mentor Graphics, expect to offer EDIF interfaces, primarily for reading netlists and writing back-annotations. The exchange of artwork information usually proceeds in either the GDS II or CIF format.

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Directory of Automatic IC Placement and Routing Software

Company and contact	Product and cost	Hosts	Layout styles	Placement algorithms and interactive features	Routing algorithms and interactive features
CAECO Inc. 2945 Oakmead Village Court, Sunnyvale, CA 95045 Mark Miller, Director of Marketing, (408) 988-0128	**CAECO Blocks** $50k	Sun-3, Sun-4, Apollo, MicroVAX, Data General, Valid SCALDstar	• Row-based standard-cell • Rectilinear block • Mixed standard-cell and block • 2, 2.5, and 3 routing layers	• Force-directed • Simulated annealing • Group interchange • Blocks and cells can be repositioned; routing channels are defined and redefined by the user	• Global • Channel • Automatic power/ground • Optimization command for cell repositioning; signal prerouting; multiple power and grounds; prerouting and editing power and ground
Calma Co. 501 Sycamore Dr., Milpitas, CA 95035 Bob Kosobucki, IC Product Manager, (408) 943-5192	**Block Interconnect System (BIS)** $50k **Block Manager** $60k	Data General, Sun, Apollo	• Standard-cell • Block interconnect	• Constructive initial placement • Pairwise interchange • User has numerous grouping and preplacement options (can do complete interactive preplacement)	• Maze • Global • Channel • Switch-box • Wires (including power/ground) may be prerouted interactively with no restrictions on the size of the wires
Control Data Corp. 2900 Old Shakopee Road, PO Box 0, Minneapolis, MN 55440 Dale Brothanek, Marketing Communications, (612) 853-3197	**MIDAS** $170k–$750k (total package); $100k–$435k (layout only)	CDC, Apollo, Orcatech, Daisy	• Gate array—2 metal layers and 1 via layer; fixed cell locations; fixed routing channels	• Interactive placer on both Apollo and Orcatech features density maps (horizontal, vertical, and combined), rat's nest (interconnect map), pre- and post-placement statistics, recalling of the placement from a previous revision of the part	• Maze • Channel • Automatic power/ground • Priority routing in batch mode; rerouting of selected nets
Daisy Systems Corp. 700 Middlefield Road, PO Box 7006, Mountain View, CA 94039 Nancy Morrison, Manager, Public Relations, (415) 960-6591	**GATEMASTER** $20k (IBM PC AT)	IBM PC AT, Logician, MegaLogician	• Gate array—channeled and sea-of-gates; 1 and 2 routing layers	• Simulated annealing • Supports 100% automatic placement and routing as well as interactive editing	• Maze • Global • Channel • Automatic power/ground • Supports automatic and interactive editing with correct-by-construction control; routing to internal pins; pushbutton layout—calls maze, channel, rip-and-retry routers automatically
ECAD Inc. 2455 Augustine Dr., Santa Clara, CA 95054 Peter Lee, Product Manager, (408) 727-0264	**SYMBAD** $50k–$100k	VAX, MicroVAX, Apollo, Sun, Tektronix	• Standard-cell • Block interconnect • Gridless algorithms • Symbolic	• Clustering, partitioning, geometric fitting • Fully automatic pad and terminal placement options; full floorplanner; interactive placement commands include align terminal, align cell, flyline (rat's nest)	• Global • Channel • Switch-box • Automatic power/ground • Power and ground sizing; "selective automation"—combined manual and automatic routing; bus routing; rip-up and retry

Other layout capabilities	Netlists in	Netlists out	Artwork in	Artwork out	Geometry editor	• ERC • DRC	Other tools or system features
• Automatic compaction • 45° routing • Contour routing • Hierarchical operation • Multiple standard-cell classes • Integrated with CAECO layout editor	SILOS	—	CAECO Layout, CAECO Layout Synthesis, GDS II, CIF	CAECO Layout, GDS II, CIF	CAECO Layout	• CAECO Checker • DRACULA II	CAECO Schematic, CAECO Layout, CAECO Waveform, CAECO Layout Synthesis
• No restrictions on power and ground routing, pad placement, and prewiring • Rectilinear blocks	TDL, Calma, Mentor	Calma Netlist Driven Layout (NDL—from a Custom Plus layout)	GDS II stream	GDS II stream, GDS II libraries	GDS II Custom Plus, symbolic editor; EDS III editor	• On-line Custom Plus, NDL • Batch-SPACER II	Placement and routing are tightly coupled to the GDS II Custom Plus editor (they use the GDS II internal data structures as the interface instead of stream); plotting/CAM
—	Proprietary format	—	Proprietary format	GDS II stream, PG tapes	None	DRACULA	Integrated system; automatic back annotation after layout
• Supports automatic delay calculation and back annotation for simulation • Correct-by-construction editing	Daisy, EDIF, ASIC vendor-specific	—	EDIF	GDS II, modified GDS II (as delivered by ASIC vendor)	MAX (option)	• Correct by construction • Yes	—
• Contour compaction • User can manually edit and recompact • Fully user-intervenable and re-entrant (manual edits are preserved upon re-use of automatic tools) • Symbolic edits permit overconstraints, which are resolved by compactor	SILOS, TEGAS, SYMBAD, Mentor	SPICE, SILOS, TEGAS, SYMBAD	GDS II, Applicon, SYMBAD ASCII file	GDS II, Applicon, SYMBAD ASCII file, DRACULA, PG, E beam	Polygon Editor (PED)	• LVS, ERC, LPE • Yes	Symbolic layout and compaction (OED), automatic floorplanner (FP), programming language for database access and technology portability (SPL)

Directory of Automatic IC Placement and Routing Software (continued)

Company and contact	Product and cost	Hosts	Layout styles	Placement algorithms and interactive features	Routing algorithms and interactive features
GE Solid State Route 202, Somerville, NJ 08876 Phyllis Orlando, Software Marketing, (201) 685-6585	**VITAL** $70k	IBM, VAX; Sun and Apollo (soon)	• Standard-cell and macrocell in arbitrary combinations • Gate array • 2 or 3 routing layers	• Fully automatic floorplanner (simultaneous placement of standard cells, arbitrary blocks, and I/O pads) • Partitioning-based algorithms • Pairwise interchange • Simulated annealing and channel-density–based standard-cell placement algorithms • Complete and partial preplacement options	• Global • Channel • Maze • Automatic routing and sizing of power and ground buses optional • User-specified control over power/ground routing • Mixed digital-analog routing (soon)
LSI Logic Corp. 1551 McCarthy Blvd., Milpitas, CA 95035 Van Lewing, Director, Software Marketing, (408) 433-8000	**LDS3 LAYOUT** $300k	Sun-3, Sun-4, IBM, VAX; Silicon Graphics graphics workstations	• Gate array—channeled and sea-of-gates • Standard-cell • Block interconnect	• Force-directed • Constructive initial placement • Pairwise interchange • Simulated annealing • Cells may be preplaced using the graphics editor, and the remaining cells are automatically placed	• Maze • Global • Channel • Switch-box • Automatic power/ground • Wires may be interactively inserted using the graphics editor, and the remaining wires are automatically routed • Clock routing
Mentor Graphics Corp. 8500 SW Creekside Place, Beaverton, OR 97005 Fred Cohen, Director of Marketing, IC Layout Tools, (503) 626-7000	**Gate Station** $51.4k–$100.4k **Cell Station** $62.4k–$110.4k	Apollo 3000, 4000	• Gate array • Standard-cell • 2 routing layers	• Constructive initial placement • Pairwise interchange • Fully interactive correct-by-construction editor (floorplanning, placement, power and signal routing); preplacement information transferred from schematic or interactively	• Maze • Channel • Global • Line probe • Automatic power/ground • Full-function interactive correct-by-construction power and signal routing
SDA Systems 555 River Oaks Pkwy., San Jose, CA 95134 Bob Wiederhold, Product Marketing Director, (408) 943-1234	**Place and Route** $57k	Sun, Apollo, VAX, MicroVAX	• Standard-cell • Block interconnect • 3 routing layers maximum	• Clustered placement • Interactive placement editor; placement through a text file; placement analysis utilities; critical-net optimization; floorplanning utilities; automatic feed-through insertion	• Global • Channel • Automatic power/ground • Automatic feed-through assignment; interactive global router; critical-net optimization

Other layout capabilities	Netlists in	Netlists out	Artwork in	Artwork out	Geometry editor	• ERC • DRC	Other tools or system features
• Iterative row-balancing techniques to generate compact layouts • Automatic back annotation of chip parasitics • Critical-path delay optimization • Stand-alone module generator • Multiple module definition to aid floorplanning • Chip-aspect ratio control • Execution time option • Automatic multiple-pass placement	CADL, TEGAS (TDL)	—	DFL, GDS II, Apple	CIF, GDS II, Calcomp, Applicon (soon), EDIF (soon), ASCII file, DFL	Calma, Mentor	• ENLAVE and CONCERT (conductivity verification programs), DRACULA II • DRACULA II	
• Automatic wire sizing of clock and power nets • Channel compaction	Compiled LSI Logic network description language (NDL)	NDL	GDS II	GDS II, IGL	DICE	• — • Graphics editor, rule driver	Automatic clock routing; automatic floorplanning using LPACE
• Routing squeeze to optimize channel utilization • Obstacle avoidance for overcell routing	DDF (Mentor format)	DDF, EDIF (gate arrays only)	GDS II, Applicon, CIF, Gate Lister, Cell Lister procedural access	DDF, GDS II stream, Applicon, EDIF (gate arrays only), Gate Lister and Cell Lister procedural access	ChipGraph (available as option to Gate and Cell Stations)	• — • Correct by construction	Automatic library generation; wire length extraction for delay calculation
• Automatic power bus tapering • Automatic support of multiple power bus topologies • Automatic compaction • Automatic, gridless, 100% completion, contour routing (90° and 45°) • Via minimization	EDIF, MIF, SDL	HILO, SILOS, SPICE, HSPICE, SCOAP, timing analysis, other user-definable formats	EDIF, GDS II	GDS II	Layout	• PDCompare, PDExtract • PDCheck	Supports hierarchical design; supports multiple technologies (CMOS, nMOS, bipolar, GaAs); customizable through use of high-level programming language (SKILL)

Directory of Automatic IC Placement and Routing Software (continued)

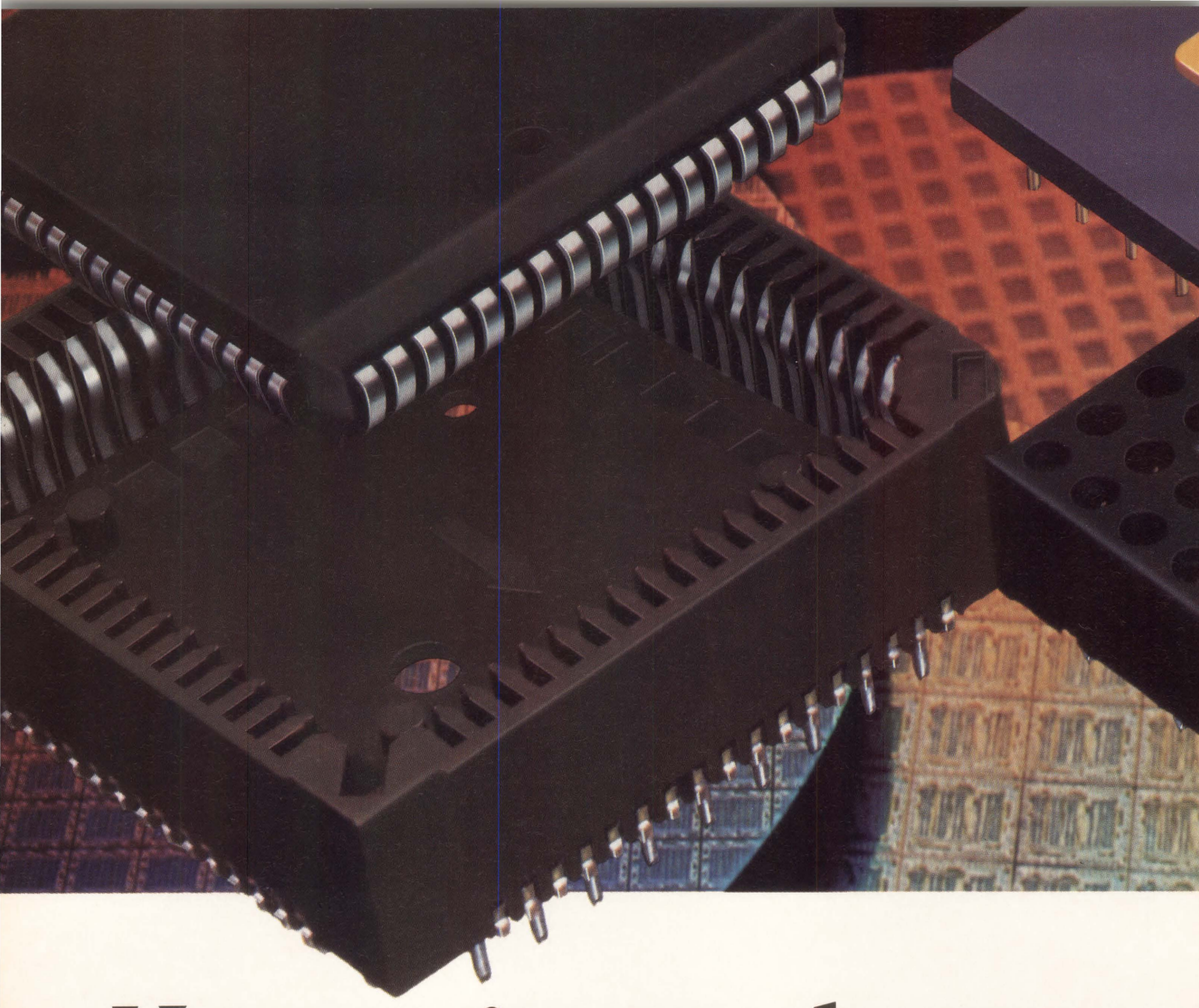
Company and contact	Product and cost	Hosts	Layout styles	Placement algorithms and interactive features	Routing algorithms and interactive features
Seattle Silicon Corp. 3075 112th Ave. NE, Bellevue, WA 98004 Larry Morrell, Director of Strategic Marketing, (206) 828-4422	**SuperGlue** $70k-150k	Apollo, Valid SCALDSTAR	• Standard-cell • Block interconnect • 1 or 2 routing layers (CMOS)	• Constructive initial placement • Interactive placement; automatic channel definition	• Global • Channel • Automatic power/ground • Interactive manual routing; interactive editing of automatic routing
Silicon Compiler Systems Corp. 2045 Hamilton Ave., San Jose, CA 95125 Jim Griffeth, Product Marketing Manager, (201) 580-0102	**GDT** $88k	Apollo, Sun, MicroVAX	• Full-custom/symbolic • Module generation (microprocessor to ROM, RAM, PLA cores) • Standard-cell • Block interconnect • 2 or 3 routing layers	• Constructive initial placement • Pairwise interchange • Simulated annealing • Min-cut partitioning • Special handling for clocks; user-defined placement of external terminals; interactive access from the system's graphics editor • User-defined algorithms	• Global • Channel • Switch-box • Automatic power/ground • Interactive block placement and floorplanning from the system's graphics editor • Manual wire editing • Automatic feedthrough assignment and alignment • Uncommitted feedthroughs
Silvar-Lisco 1080 Marsh Road, Menlo Park, CA 94025 Dirk Wauters, Director, Product Marketing, (415) 324-0700	**GARDS, GARDS-XL, AVANT GARDS** $60k+ (includes schematic capture)	Apollo, Digital, Sun, IBM	• Gate array—channeled, sea-of-gates, VLSI sea-of-gates; row, column, island • Mixed block and any size cell • 3 routing layers maximum	• Automatic and manual floorplanning • Min-cut • Constructive initial placement • Force-directed • 1- or 2-dimensional congestion • Timing-driven layout; interactive placement editor	• Line-search and maze clean-up routing • Interactive, semi-automatic, or automatic routing • Programmable and fixed contacts; routing over, through, into cells; routing editor with automatic routing; conditional routing
	CALMP $57k+ (includes schematic capture)		• Standard- cell • Block interconnect with unlimited hierarchy • Mixed block and any size cell • 3 routing layers maximum	• Interactive floorplanning • Cluster-based initial placement • Force-directed • Critical-net optimization; interactive placement editor	• Global • Channel • Automatic and hierarchical power/ground • Routing over, through, and into cells; conditional routing
Tangent Systems 2840 San Tomas Expwy., Suite. 101, Santa Clara, CA 95051 David Evans, Vice President of Marketing, (408) 980-0600	**TANCELL** $55k (workstation), $120k (VAX-11/785)	VAX, MicroVAX; Intergraph InterPro 32C, 32; Apollo; Sun	• Standard-cell • Block interconnect • 3 routing layers	• Constructive initial placement • Simulated annealing • Timing-driven placement; placement by cell type, cell groups; interactive placement editing	• Maze • Global • Channel • Automatic power/ground • Wire editing; delay analysis

Other layout capabilities	Netlists in	Netlists out	Artwork in	Artwork out	Geometry editor	• ERC • DRC	Other tools or system features
• Automatic sizing of power and ground wiring • Optional flattening of the routing hierarchy	Mentor Graphics NETED, Valid Logic ValidGED, text specification	—	GDS II	GDS II, CIF	None	• — • Yes	Integrated with the Concorde VLSI compiler
• Contour routing • Procedural layout • Rat's nest • Slicing • Automatic internet parasitic extraction • Automatic netlist extraction • Automatic compaction	L language and SPICE, Lsim, Lpar, EDIF (4Q)	SPICE, Lsim, Lpar, L language	GDS II	GDS II	Led; graphical and schematic editor; generation of router netlist from graphical entry; manual routing editor; executive for automatic compaction rule checking and routing	Lrc and Ldbi for hierarchical user-defined electrical and geometrical checking programs	L procedural design language for developing reconfigurable circuit compiler programs; Lsim analog and digital mixed-mode, fault simulator; behavioral modeling; Ltime static timing analysis and critical-path optimization; Lcompilers (RAM, ROM, PLA); microprocessor cores; CRT controller
• Contour routing, 90° and 45° • ECO capability • Multiple physical types for every logical type • RC delay analysis, capacitance extraction, back annotation for postlay-out simulation	SDL, MDL, EDIF (2H'88)	SDL, TDL, SPICE, HILO-3, SILOS, MDL	GDS II, Applicon 860, CV, CIF	GDS II, Applicon 860, CV, CIF	PRINCESS	• Full ERC, EPC, netlist comparison vs. layout, hierarchical ERC/NCC • Full hierarchical DRC	Physical foundry libraries; schematic capture; mixed analog-digital simulator; switched-capacitor simulator; behavioral simulator; logic simulator; SPICE/SDL netlist extraction; printed circuit board layout system; design verification and mask data preparation software; technology independence (CMOS, NMOS, bipolar, biCMOS, GaAs)
• Schematic-driven placement for easy floorplanning • Hierarchical layout • Multiple physical types for every logical type • RC delay analysis, capacitance extraction, back annotation for postlayout simulation							
• Channel compaction • Timing-driven routing • 100% routing completion	EDIF, HILO-3, TDL, ILOGS/SILOS	EDIF, HILO-3, ILOGS/SILOS	GDS II	GDS II	None	• Open, shorts, and floating topologies; stubs • Placement, interconnect width and spacing, netlist	TANSURE timing-driven layout; TANTEST automatic design for testability

Directory of Automatic IC Placement and Routing Software (continued)

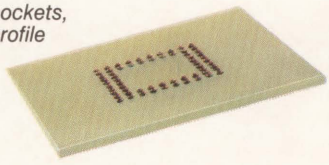
Company and contact	Product and cost	Hosts	Layout styles	Placement algorithms and interactive features	Routing algorithms and interactive features
Tektronix Inc. CAE Systems Division PO Box 4600, Beaverton, OR 97076 Bob Harrison, Product Marketing Manager, (503) 629-1630	**MERLYN-G** $50k (MicroVAX)	IBM, VAX, Cray, Apollo, MicroVAX; Tektronix graphics terminals	• Gate array—channeled and sea-of-gates • Virtually no restrictions on array size or number of macros	• Force-directed • Constructive initial placement • Pairwise interchange • Quadratic/least-squares • Interactive graphical placement editing	• Maze • Global • Channel • Automatic rip-up and retry • Interactive graphical wire editing
	MERLYN-S $50k (MicroVAX)	VAX, MicroVAX; Tektronix graphics terminals	• Standard-cell • Block interconnect • Virtually no restrictions on circuit size or number of devices	• Force-directed • Constructive initial placement • Pairwise interchange • Quadratic/least-squares • Graphical placement of cells, blocks, and I/O pads during preplacement; interactive graphical placement editing; graphical floorplanning includes chip-size estimator	• Global • Channel • Automatic power/ground • Interactive graphical wire editing; graphical wiring of timing-critical nets to achieve minimal delay
United Silicon Structures Inc. (US2) 1971 Concourse Dr., San Jose, CA 95131 Steven Eliscu, Product Marketing, (408) 435-1366	**SOLO family** $25k–$50k	Sun, Apollo, VAX, IBM PC AT	• Compiled logic • Standard-cell • Block interconnect	• Force-directed • User can force physical logic groupings using the netlist hierarchy • User can force pad placement	• Channel • Automatic power/ground • User can tag critical nets
Valid Logic Systems Inc. 2820 Orchard Pkwy., San Jose, CA 95134 Donna Rigali, Product Marketing Manager, (408) 432-9400	**Compose** $25k	Sun	• Standard-cell • Full-custom blocks • Compiled • No restrictions on circuit size • 2.5 layers visible; unlimited number of layers supported	• Constructive placement • Automatic cell orientation • Pairwise interchange • Interactive graphical control • User-specified I/O placement • Net and component weighting	• Global • Maze • Automatic power/ground planar • Manual prerouting • Re-entrant router • Netlist-driven • Handles ECOs incrementally • Rules-driven user-specified maximum length and capacitance, layer and width specification
VLSI Technology Inc. 1109 McKay Dr., San Jose, CA 95131 Bill Murray, Software Marketing Manager, (408) 434-7660	**VLSI Logic Compiler** $140k	VAX, Apollo, Sun, MicroVAX, HP; Tektronix, AED graphics terminals	• Standard-cell • Block interconnect • 2 routing layers	• Min-cut • Proprietary • Interactive floorplanning for standard cells and multiple arbitrary blocks	• Maze • Global • Channel • Automatic power/ground • Interactive global routing guidance to control power and critical nets • Channel compaction

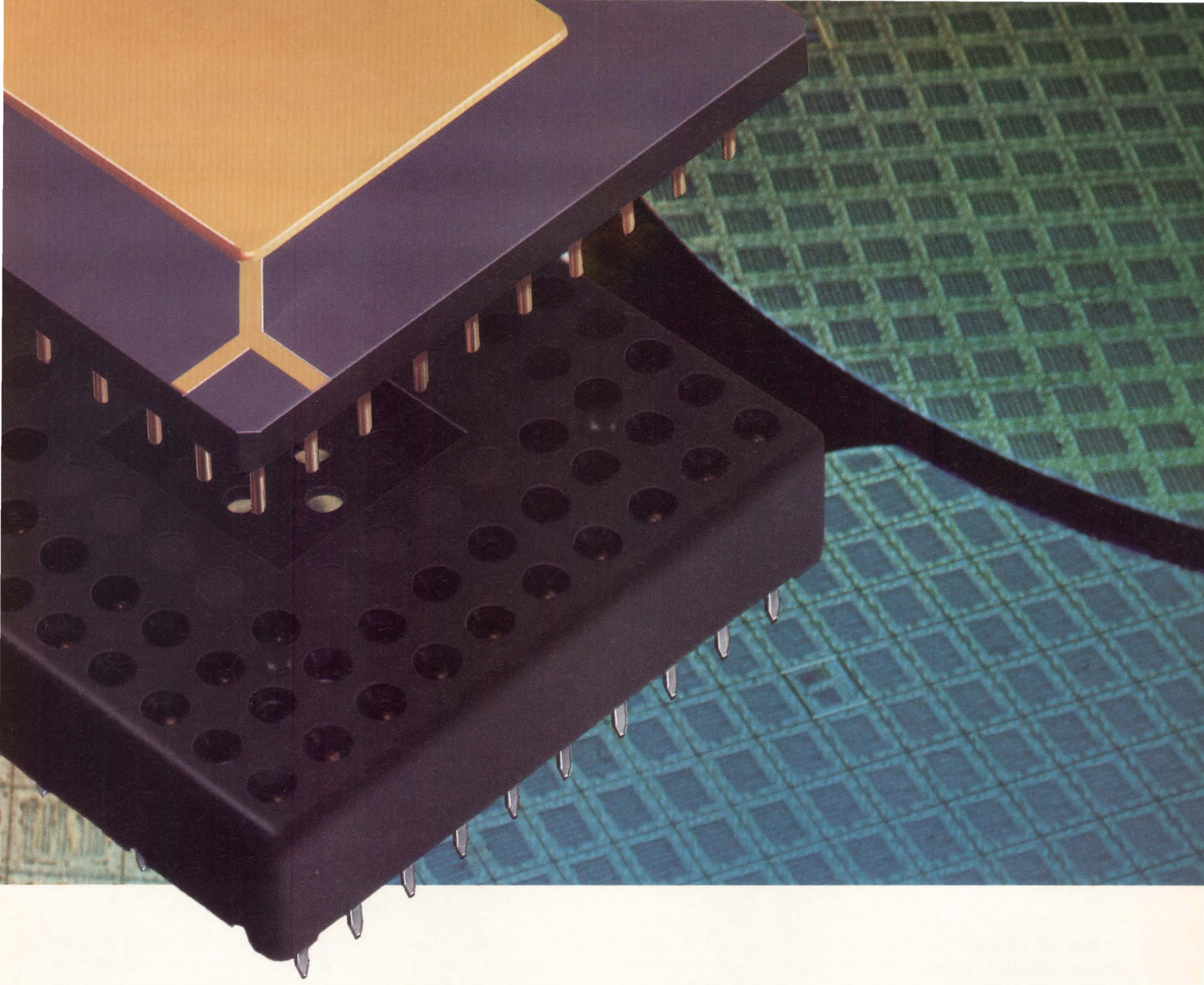
Other layout capabilities	Netlists in	Netlists out	Artwork in	Artwork out	Geometry editor	• ERC • DRC	Other tools or system features
—	Consult factory	—	Consult factory	GDS II	None	• — • DRC	Graphical database creation and maintenance; TURNCHIP ASIC layout modules provide foundry-endorsed customer-performed fully automatic layout for specific array families; foundry-certified symbol, simulation, and physical libraries provided
• Automatic channel compaction provided • Gridless routing is supported	Consult factory	—	Consult factory	GDS II	None	• — • Yes	Graphical database creation and maintenance
• Pad placement to minimize wire length	IDL (Intermediate Design Language)	IDL	CIF, GDS II	CIF	None	• Correct by design • —	DRAW produces CIF and a load file for back-annotated simulation; ARTVIEW is a graphical plotting utility
• Separate automatic compactor • Via minimization • Automatic jogging • Tapered power routing • Hierarchical • Variable-size wires • Automatic generation of pad ring	SPICE, ASCII netlist from ValidGED schematic capture	TIME-MILL, SPICE, ValidGED	GDS II stream, ValidGED, EDIF, CIF	CIF, GDS II stream, ValidLED, EDIF	ValidLED	• ValidCOMPARE • ValidDRC	Automatically generates library cell definitions from the layout
• Automatic generation of pad ring structures • Compaction • Variable-size wires	Daisy, Mentor, TEGAS, proprietary	Proprietary, SPICE, HILO, Daisy back annotation, Mentor back annotation	CIF, GDS II	CIF, GDS II	VTIlayout or VTIcompose	• VTInetcompare • VTIdrc	Symbolic manual or automatic routing in VTIcompose; integrated with silicon compilation system



How we've made sure the chip's locked in, but you're not.

ZIF and LIF PGA sockets, plus our minimal profile spring sockets in PGA footprint.





Whichever direction you take in microprocessor technology, AMP makes sure you have the socketing options you need to make it pay off.

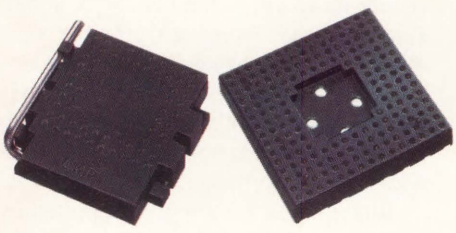
Our high pressure tin sockets for plastic leaded packages come with an exclusive Positive Lock retention system that keeps chips secure during handling and shipping. Ceramic chip carrier sockets feature duplex plated contacts and snap-on covers that accommodate heat sinks. Both are available in standard and surface-mount versions.

AMP offers you more: high-speed, surface-mount sockets on .020″ centers. Gold-plated plastic carriers and sockets. For pin grid arrays, sockets in ZIF and LIF styles, plus custom VHSIC capability.

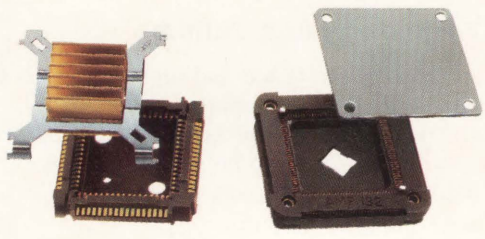
Choose your technology. AMP makes it easy to implement, with full socketing support.

Call 1-800-522-6752 for more information on AMP sockets. AMP Incorporated, Harrisburg, PA 17105-3608.

AMP Interconnecting ideas



Low-height sockets in all standard sizes (JEDEC A, B, D), with duplex-plated contacts for sure performance. High-speed, surface-mount sockets feature 0.5pF, 1.4nH contact characteristics.



CIRCLE NUMBER 10

VLSI in Japan

Japanese Engineering Girds for the Future

Stan Baker, Editor-at-Large

Japan's electronics engineers are feeling the pressure because Japan's electronics industry is no longer the challenger. The goal of Japanese laboratories is to keep Japan one step ahead by forging new generations of systems that are smarter and higher performers than those produced by worldwide competitors.

Japanese engineering is undergoing significant changes—in the development and configuration of tools rather than in the style of managing technology. Integrated design automation that brings semiconductor logic and silicon design together is being avidly sought throughout Japanese engineering organizations. That has forced much indigenous CAD software development. Design automation software that spurred a huge industry in the United States does not appear to fit well within Japanese engineering organizations. Even those tools that do fit are being integrated and augmented with the human interface and documentation features that match the Japanese language and style. Overall, engineering managers throughout Japan are confident in their country's engineering prowess and can be sometimes heard making critical remarks about foreign engineering.

Technology and Culture

They have a tested and highly disciplined product development culture and see that as absolutely essential to success. They obviously do not understand why foreign competitors so seldom operate the way they do.

The critical question, though, is whether the Japanese can meld design automation within their engineering culture or whether the competitive necessity of using design automation will impose fundamental organizational changes. Developing and integrating the best design automation tools has therefore become the central effort at Japanese semiconductor companies.

The Japanese are fully cognizant that the design automation bridge from silicon to systems is already established. In the United States and Europe, essentially all the new computer systems have been developed with extensive use of simulation. But in Japan large VLSI projects are still developed from definition to end products by the same design group, with dependable but poorly integrated tools.

This concern is expressed by Hajime Yasuda, department manager for strategic planning and 32-bit microcomputer development at Hitachi Ltd. After shepherding the H series microprocessors and microcontrollers through development for several years, Yasuda is looking forward eagerly to a better design environment. "We must use a hierarchical design system with macro simulations, rather than design on one level only." He points out that chips are getting too large for any one person to manage in detail.

The integrated hierarchical computer-based environment is needed because "VLSI designers are becoming similar to software designers." There are "many tens of engineers on projects now and many workstations," he explains. But there is still "no good tool for macro descriptions. The hierarchical system is not easy to make."

At Hitachi's Musashi Works several hundred terminals work off a Hitachi supercomputer. The design automation environment being built around that processing power uses proprietary software. "We will consider outside packages," Yasuda says, "but compatibility is a big problem."

Lagging Software

Many CAE/CAD development projects exist within the research and product laboratories of Japanese semiconductor companies. But most have not come into broad use for product design, says Koji Sato, manager of the layout design aids group in the IC CAD development department of Mitsubishi Electric Corp. He characterizes these developments as being too specialized and indicates that they are incomplete largely because they are so costly. Also, not enough software design talent has been available to make them of general use or to integrate them.

It costs less to purchase design software tools from U.S. vendors, says Sato, and so Mitsubishi's strategy is to develop only the unique tools it needs. Sato seems more committed to getting outside software wherever possible than other Japanese managers. But other Japanese engineering managers say they have found currently available tools difficult to integrate and lacking in functions and performance.

That attitude is strongly supported by

Hajime Sasaki, vice president of NEC Corp. and manager of the semiconductor group. NEC's division-wide design automation environment "will be all of our own developments. I don't think the performance of commercial products is good enough for our needs."

At NEC's Central Research Laboratories in Kawasaki, Satoshi Goto is responsible for the development of much of the in-house design automation tools that Sasaki is waiting for. "The most important problem is the integration of tools," he says, and he will develop those tools in NEC labs. Outside tools "don't have enough functions. That is essential for NEC, and we have our own methodologies, especially for chip design. For ASICs, however, we can do with commercial tools."

ASIC Alliances

The same attitute was echoed at Toshiba Corp. by Mitsuhiro Koike, manager of the design automation development group in the CAE and CAT engineering Department at the company's Semiconductor System Engineering Center. Although Toshiba will depend on LSI Logic, Tangent, SDA, and others to provide the ASIC design tools, it is developing its own tools for proprietary chips. Toshiba is also depending on its alliance with Siemens and General Electric for cell development.

Japanese managers are looking for future generations of design automation systems that have the ability to handle such tasks as examining complex three-dimensional structures rapidly, in large groups of devices or one at a time, as well as in layer-by-layer detail. They also must be able to simulate electrical, mechanical, optical, and thermal action in a broad overview or in the minutest detail. Furthermore, the designer must be able to get answers to complex queries in moments, not hours or days.

Optimizing designs requires fast turnaround for hypothesizing and testing the hypotheses, and then iterating the process as many times as necessary to arrive at a final solution.

But speed is not enough. "It's necessary to introduce artificial intelligence," NEC's Sasaki says. As an example, he points to signal delay analysis in laying out ICs. "Expert knowledge is needed for optimizing placement and layout. Realizing such expert systems is mostly an idea now," he continues. "It needs dedicated AI engines. Present-day computer architectures don't work and we may need non–von Neumann processors."

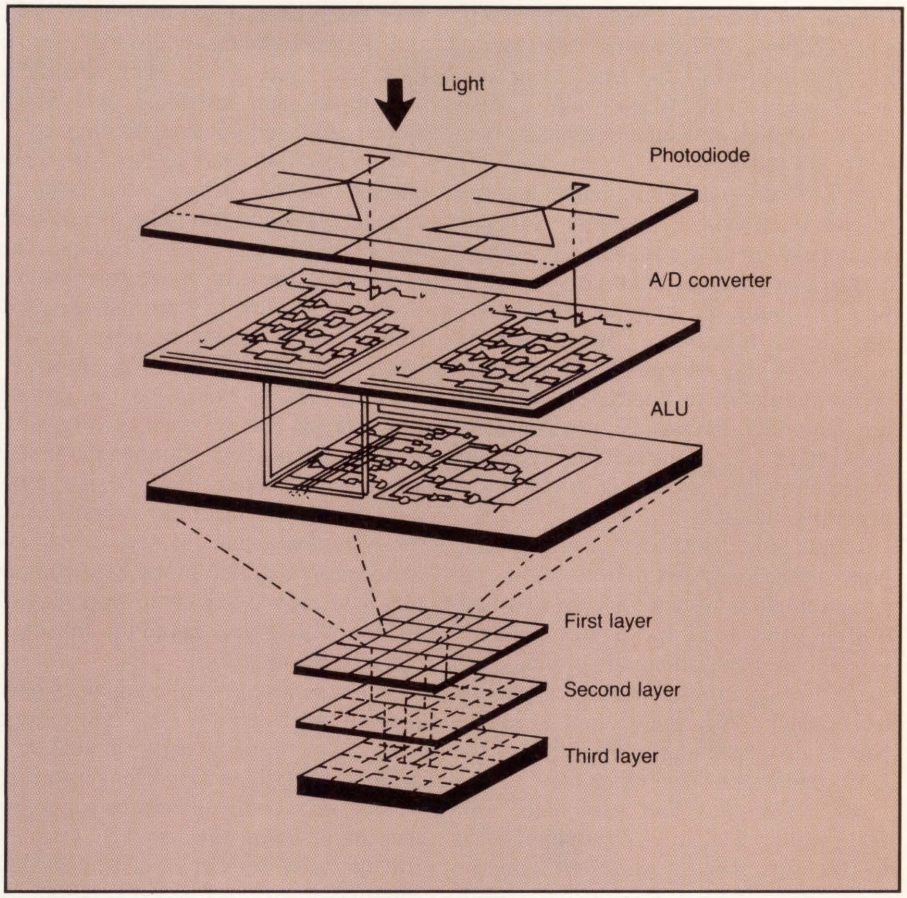


FIGURE 1. Mitsubishi has made demonstration prototypes of a three-layer image-processing subsystem that it predicts will be more than 5,000 times faster than a typical pipelined processor.

Expert Systems and Supercomputers

NEC's research labs, like those of its competitors, are working on logic synthesis with expert systems and artificial intelligence. The goal is to go automatically from functional description to logic. Sasaki sees the results of that effort being deployed in his engineering labs in the early 1990s.

Fast simulation with expert-system guidance can bring about fully interactive engineering and is therefore as critical a goal as any other feature of design tools. Simulating the action of millions of transistors quickly will require supercomputers. So will a full-featured analysis of individual device structures. Simulations necessary for the development of new processes, and research to increase the understanding of materials, will also require huge computing resources. System engineering must be concerned with the whole scope of hardware, from base materials to the end product and its lifetime maintenance.

Supercomputing performance—up to thousands of MIPS—is the key to satisfactory simulation. Japan's Ministry of International Trade and Industry has been guiding a cooperative supercomputing initiative since 1981. The target date for completion is 1990, but the results of the cooperative effort are already finding their way into in-house systems.

Party to MITI's program are Fujitsu,

Hitachi, Mitsubishi, NEC, NTT, Oki, and Toshiba. Meanwhile, Matsushita Electric Industrial Co. Ltd.is working with Kyoto University to develop a massively parallel minisupercomputer, one with 300 CPUs.

In addition to supercomputers and artificial intelligence, Japanese planners are depending on a new wave of sophisticated workstations and high-speed networks to build the integrated engineering systems they need. Early models of supercomputers are being used to develop the simulation technologies for studying materials, processes, devices, circuits, packaging, and systems. The big supercomputers are likely to be used primarily internally.

In late 1985, NEC began using HAL, a high-speed logic simulation engine. It can simulate a system with up to a half million gates and 2 megabytes of memory. It can debug the total system: CPU, main memory, cache memory, and control storage. The first system available had 32 processors and was intended for large mainframe development.

NEC's Goto has built a simulator with 100 parallel CPUs and a throughput of 90 to 100 MIPS. The CPUs use 68020 microprocessors. The system now being built has 256 processors that Goto says will achieve over 200 MIPs. Goto refers to the entire environment for VLSI design as a "silicon brain." Its primary elements will be artificial intelligence techniques, hardware engines for accelerating specific tasks, new man-machine interfaces, silicon compilers, and networking. The graphics must be fast and processing on complex problems must be done in 3 minutes maximum, Goto estimates.

It will be several years before supercomputing and optical token-ring networks are driving highly integrated in-house design systems. Meanwhile, Japanese semiconductor companies continue to struggle with the issues of interfacing with their ASIC customers' needs.

Compartments

The well-ordered and -disciplined operations of Japanese electronics companies could be described as "compartmentalized." Each compartment or cell has its own set of responsibilities. Projects are broken down into basic tasks and assigned to the appropriate cells. Each team gets a full set of specifications, costs, and schedules, over which there is little or no renegotiating.

This discipline has fostered the contracting out of many of the tasks, a siuation that occurs more frequently here than in the United States or Europe. The contractors are treated like internal cell teams. Many times, these outsiders are chip design houses that become involved in chip designs critical to the project.

These design houses are a driving factor in the development of ASIC CAD systems and have been among the first to adopt workstations. The design tools must match the Japanese system, since the system will change only very slowly to accommodate the tools. U.S. companies have moved quickly to workstations and are willing to adapt to the software, but not the Japanese.

The Japanese system companies have not invested heavily in VLSI design tools. Also, until recently, almost 90% of the ASIC designs have been performed by the semiconductor houses supplying the chips. Even now, experts estimate that the total number of ASIC packages supplied by the semiconductor houses represents over 80% of the ASIC volume in Japan. The aggressive efforts of semiconductor houses to supply these complete packages has not encouraged the system vendors to invest in their own design automation tools.

ASIC Designers: A Short Supply

The pressure is on systems engineers to become involved in the configuration of circuits on silicon. Observers of these trends in Japan expect that the semiconductor houses will gradually push most of the ASIC design tasks into the system houses. They have to: There simply are not enough semiconductor engineers to meet the demand.

As testimonial to this growing demand for ASIC designs, Toshiba has recently built an 11-story ASIC design center in Kawasaki with at least 60 design booths dedicated to specific customers. "We plan to port Toshiba CAD to customers' systems," says Kenji Yoshida, senior manager of the CAD and CAT engineering department at the company's Semiconductor System Engineering Center. Toshiba is providing the libraries and interfaces for its mainframes. Layout tools for 1.5- and 2.0-μm gate arrays are also offered for customers' workstations.

Over at Hitachi, IC designers use their own MCDA system to take them from the logic level through simulation down to the physical layout. They can work at the chip, block, or cell level, and a cell generator is being developed. Blocks are now placed manually but routed automatically. The system can handle an entire chip if it runs on a mainframe with sufficient memory.

The cell generator will operate independently of design rules. The logic is entered, along with the design rules. The pattern emerges automatically, but "this is not near perfection," says Shojiru Asai, directing manager of Hitachi's ULSI Research Center at the Central Research Laboratory. "Human beings have layout habits," Asai continues. "They use certain personal rules, and the results should incorporate these rules."

Hitachi is also developing an automatic logic generator, timing simulators, and automatic test pattern generators. These are the main areas of work, Asai adds.

MCDA was a primary tool in developing the H series microprocessors. "We are very confident of it," Yasuda says. Therefore MCDA is being expanded not only with these new capabilities, but to more engineers. However, "MCDA is mainframe-oriented and can't be ported to workstations easily," Yasuda admits. Nevertheless, the porting is under way. What's more, he says, Hitachi is thinking of buying Suns to bring it to more engineers on local workstations.

The mainframes will be used for general-purpose accelerators, Asai projects. The 35-MIPS 6080H mainframe at Hitachi routed the company's H32 32-bit microprocessor design in 10 hours.

However, at NEC, Sasaki's expectation is that mainframes will become limited mostly to powerful communication controllers and database processors on the high-performing networks that will be required for the next-generation IC design automation systems. Special

accelerators will be tailored to maximize the performance of specific tasks.

In Japan, the newest and fastest technologies have usually bowed first in large computers, where the extra expense can be more easily justified. Nevertheless, consumer systems have been a major driving factor for the Japanese engineers—similar to the role played by computers and communications systems for U.S. and European engineers.

Consumer products, formerly mostly analog, have rapidly moved into the digital domain, with memory and digital signal-processing functions leading the pack. For example, some experts predict that high-definition TVs will soon use over 100 megabits of DRAM.

The Need for Speed: DSP, Not RISC

With leading-edge memory technology well in hand, Japan is now making increased efforts in DSP. The current state of DSP development offers a 50-ns processing cycle time for 32-bit systems. But the target is 20 ns at prices consistent with consumer markets. NEC's Sasaki expects that DSP cycle times of 25 ns will be achieved by 1990, with 15-ns chips available by 1995. "beyond 15 ns, it's not possible to see," he says.

Demonstrating the current state of the art, Hitachi has an image processor with a 50-ns cycle time now being readied for market. It processes a 512×512-pixel screen in under 0.2 second and uses micro- and "pico"-levels of coding. Aimed at image telecommunication systems, compressing X-ray photos in medical laboratories, robotics, and office automation, it has 430,000 transistors fabricated in 1.3-μm MOS. The application software is under development, with plans to market the product this year.

The DSP blocks are now standard products, but in the future they will be offered as cores, Sasaki says. Products will change rapidly, but in their features rather than in the essential functions. The essential-function cores will allow upgrading of the peripheral functions to keep up with changing market trends. Sasaki emphasizes the high priority of the core concept.

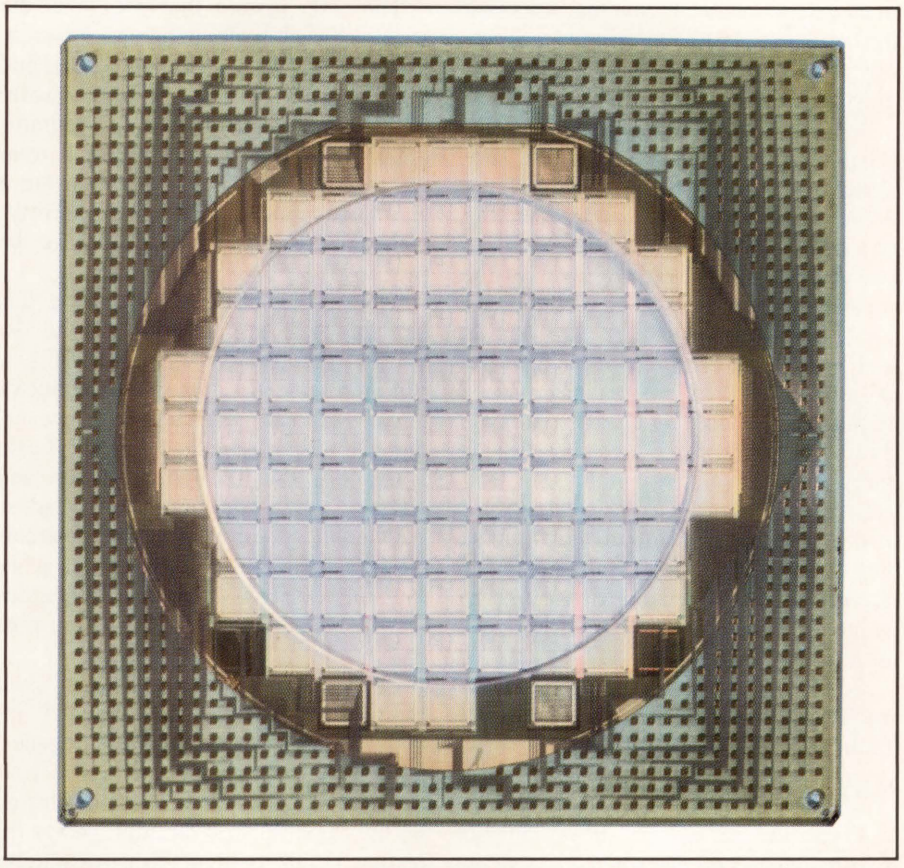


FIGURE 2. Fujitsu claims solid progress toward the practical use of wafer-scale technology. One example is this wafer comprising multiple 170,000-gate FFT processors with built-in test circuits.

What about RISC as a path to higher performance? NEC and other Japanese companies deny they are involved in RISC projects. Their microprocessor programs are CISC-oriented, and the companies are tightly involved with TRON, which uses one of the strongest CISC approaches.

Sasaki admits that the workstation makers are not satisfied with CISC and are asking for RISC, stating his personal feeling that NEC should also be involved in RISC but is not at present. Other product programs take precedence, and "I don't think we can have a general-purpose RISC chip." NEC is willing to design custom RISC chips, but so far no customers have signed up.

(Fujitsu is of course involved with RISC, fabricating both Intergraph's Clipper and Sun Microsystems' SPARC. Clipper is a full-custom chip set, and SPARC has so far been implemented by the company as a custom gate array.)

The quest for greater density, higher performance, and lower cost per function are tied together, as they have been since the dawn of the IC era. Seeking to put Japan in the lead in this search, MITI launched its future electron devices program in 1984. That program has focused on three-dimensional structures, superlattices, radiation-hardened devices, and bioelectronics.

More Dimensions

The 3D IC portion of the program has four years to go. Its target is the fabrication of five layers of circuitry on a silicon substrate with typical processing methods and with essentially the same device densities (per layer) obtainable with single-level fabrication.

Mitsubishi is spearheading the project, which is supported by several other Japanese semiconductor companies, at its LSI Research and Developmant Lab in Itami City, near Osaka. The general

manager, Kyoichi Shibayama, says that the target date for the multilayer technology is 1995, with simple designs beginning in 1993.

Mitsubishi has demonstrated prototypes of a basic image-processing subsystem (see Figure 1). This three-layer device includes a 5x5 light-detecting photodiode array on the top layer; an analog-to-digital converter layer in the middle; and a group of ALU circuits on the bottom layer. There is a conversion and processing channel for each of the 25 diodes, and the processing proceeds in parallel, channel by channel. When a 512×512-pixel three-level system is fabricated, Mitsubishi predicts, it will process a full frame in 5 μs, compared with 26 ms for a typical pipelined image processor. The paralleling factor is 5,200 for this enhanced density technique. The company, though, has said little about cost projections.

So far, the biggest problem is the quality of each layer, since one layer failure ruins all five layers of circuitry.

Technology Paths

From the processing developments seen in Japan and elsewhere, it is obvious that the simple linear progress of IC technology, based on planar shrinking, is due for some rude alterations. There is definite progress in wafer-scale integration and 3D device structures.

Fujitsu, for example, has finally made what it believes is solid progress toward the practical use of wafer-scale technology. Its researchers in Atsugi have fabricated single-wafer FFT processors with built-in test circuits, and composed of some 170,000 gates (see Figure 2).

Fujitsu uses conventional lithography to make identical repeated blocks of logic that are compatible with current processing equipment. Built-in self-testing of the processor blocks and interconnects is a must.

Many identical wafers are fabricated and tested. Then the good dice and interconnection paths are identified for each wafer. Fujitsu has created a program that automatically designs a unique mask for the top metal layer to provide the desired interconnects. But since the yield patterns vary from wafer to wafer, this mask is good for only one wafer.

The CAD system that programs the wiring of each wafer generates a pattern for contact holes between the second and third metal layers. After getting a wafer failure map, the CAD system programs the logical position and physical relationships for each good block, using a simulated annealing algorithm. Forty-eight good blocks are used to make the processor.

The biggest problem in making this technology fully practical is still the low yields, according to Shinpei Hijiya, senior researcher at the semiconductor devices laboratory in Atsugi. However, damage from mechanical probing is also a major problem. Interconnection and isolation are still problems, too, he adds.

One FFT system his team has fabricated includes 88 16-bit multiplier-accumulators (MACs), each with 2900 gates and 25 I/O pads. Power dissipation runs about 5 W on the 4-inch wafer.

Each block is tested using its own built-in 700-gate test circuit which includes a pseudorandom pattern generator, a pattern compressor, and a test-controller. The interconnects are tested by the same self-test circuits. Power for testing is fed to each block separately. Also, by using internal switches, the blocks can be switched in and out of strings of blocks and isolated, and facilitating troubleshooting.

Hijiya says one possible use of the new methodology is in combining next-generation SRAMs into wafer-scale memory boards. Because the technology is limited to systems where many blocks of one type are needed, logic systems would have to be implemented as parallel systems that use repeatable building blocks.

Is there a large market possible? "Maybe," Hijiya says, but "we must use the most up-to-date technology to be competitive, and it will remain a technology mainly used for special purposes. It's not almighty." But Fujitsu is now studying applications for the technology.

Mitsubishi has made an interesting analysis of the role of different VLSI structures. In the 1990s Mitsubishi researchers expect 3D circuits to have very broad application in high-speed and high-density systems. Microfabrication, putting chips together at the micron interconnect dimensional levels, will push circuits to new heights of functional density. And wafer-scale integration will be the path to take to the next level, ultra-large-scale integration.

Packaging: Another Revolution

The broad developments in IC processes, structures, and devices are the glamorous high-profile pursuits of this industry. But the art and science of assembling and interconnecting the dice on substrates and across fiberglass boards have also contributed heavily to the increasing performance of systems—and also to the cost picture.

In Kyoto, at Kyocera Corp., the message was that new packaging technologies are bringing IC and package designers together, making packages part of the devices, as well as components of the system and opening new opportunities for enhancing speed, size, cost, and reliability.

The package makers have traditionally followed the directions of the die designers. But now the trend is changing.

In the opinion of Yoshihiko Nishikawa, engineering manager of Kyocera's laminate package operation, a primary route to flexibility, speed, and reliability is with multilayer, multidie ceramic packaging. This technology is coming close to the processing of the dice themselves, now using deposited thin-film wires with minimum features of about 1 mil. The packages offer improved performance and complete protection for the dice, Nishikawa says.

The packaging has been used for special circuit combinations in the heart of processors by computer companies for over five years. But Kyocera sees interest developing in other areas and also at some semiconductor companies. These other areas were just "not ready for it till now," Nishikawa says. There have been mechanical problems with bond attaching and mismatched thermal coefficients between the die and substrate. But such problems have been solved. Beyond that, laser adhering of lead frames is being researched, promising a capability that will allow even more automation of the assembly operation. □

A High-Speed, Low-Power Josephson-Junction RAM

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In a Josephson-junction computer, a cache and main memory hierarchy is indispensable for parallel processing, and many types of Josephson-junction logic and memory circuits have been developed to demonstrate their feasibility in such an application. Josephson devices have been fabricated with both fast switching elements and very low power consumption. However, the cache memory must work at the same speed as the processing unit. Unfortunately, previously reported cache memories did not work fast enough to satisfy the system requirements. Therefore, a successful high-speed, low-power Josephson computing system depends critically on the development of a high-speed Josephson RAM.

One problem is the complicated timing control required for resetting the peripheral circuitry. This control has been an obstacle to decreased memory access time. The peripheral circuit gates (which work on dc power) have to be reset to the initial condition after the logic operations are completed. Also, to prevent the circuit from latching up during the reset period, the gate circuit must be controlled with a reasonable timing margin. This margin prevents decreasing the circuit operating time.

We propose a resistor-coupled Josephson logic (RCJL) decoder, which works on ac power. RCJL eliminates the need for complicated timing control signals, since the decoder is reset when the ac current passes through zero.

Another goal of NEC's high-speed RAM development program was to deliver a subnanosecond RAM with wide operating margins. The RCJL decoder and sense circuits, plus a nondestructive-read-out (NDRO) memory cell, all of which were developed to work on ac power, have succeeded in meeting this wide operating margin requirement. The memory cells and cell array drive lines were designed so that bidirectional signal currents could be used. The three-junction superconducting quantum interference device (SQUID) read and write gates in the memory cells and the cell array drive lines are designed to read the correct data from each cell independent of the polarity of the powering current.

A 1-kilobit high-speed Josephson-junction RAM has been developed as the first in a series of Josephson LSI devices. The 1K × 1-bit memory was integrated into a 4.4-mm × 4.4-mm working area with NDRO cells using a 3-μm niobium planarization process. Approximately 10,000 $Nb/AlO_x/Nb$ junctions with critical current densities of approximately 1000 A/cm^2 were designed in a variety of physical sizes in order to decrease the number of junctions required for implementing the RAM. The critical current density is limited by the available minimum junction size.

The RAM consists of X and Y decoders with address buffers and inverters (see Figure 1); a 32 × 32-bit cell array; X, Y, and D drivers; a sense circuit; and X, Y, and S reset circuits. All the peripheral circuits except the D line drivers work on ac power. The ac powering scheme eliminates the control signals, such as set, reset, or start. Ten-bit address and a read/write select signal, along with their complements, are decoded in three-stage AND circuits. The number of decoding stages is decreased by introducing a parallel decoding technique with high-drive-capability AND circuits in order to reduce the decoding time. Each NDRO memory cell can store 3 flux quanta. The cells are symmetrically arranged in a 2.08-mm × 2.08-mm area of the chip, allowing direct connections to the signal lines running between adjacent cells. The smallest line widths and spacings are 3 and 2 μm, respectively.

The memory cell is selected by X and Y line currents for the write mode and by X and D line currents for the read mode. The D line current determines whether a logic 1 or a logic 0 is stored in the cell's storage loop. The X lines are reversed every two cells to control the current direction at the gates. Read data from the cell array, selected by the 32 AND gates in the sense circuitry and driven by the decoder output circuitry, is collated with two-stage OR gates.

The chip, including an access-time–measuring circuit, was fabricated using a four-layer Nb planarization process. A lift-off technique was used for the interconnecting wiring, and a polystyrene etch-back technique for the junctions. The contacts were manufactured using a tapered etching technique.

The memory consists of connecting leads made up of three layers of Nb, 300 or 400 nm thick; planarized $Nb/AlO_x/Nb$ junctions; 60-nm-thick Mo resistors; and silicon dioxide insulators. The $Nb/AlO_x/Nb$ junctions were designed in 11 different sizes ranging from 3.3 μm × 3.4 μm to 7.0 μm × 10.7 μm as a means of obtaining a high packing density.

The basic NDRO cell occupies a 65 × 65-μm^2 area with Josephson-junction current densities of 1,030 A/cm^2. The interconnecting paths for the decoder and sense circuits are 4 μm wide.

The memory function was statically verified with a "marching" test pattern from a standard LSI tester. Forty percent of the bits operated within a ±18% bias current margin.

The access time is the measured difference in delay time between the reference path and the 1K RAM path. It is equal to the sum of the decoding time

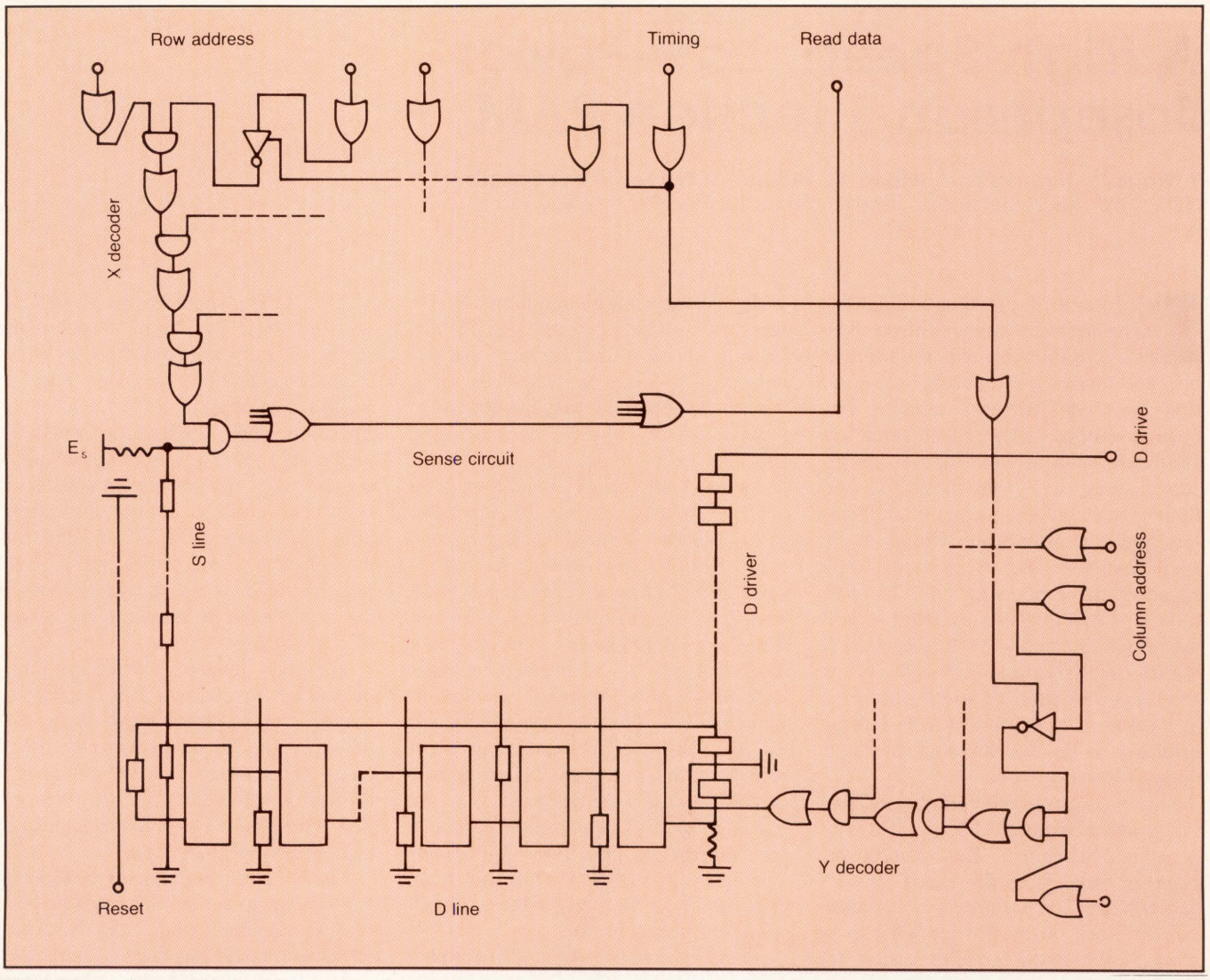

FIGURE 1. Simplified diagram showing the critical paths for reading the data from the 32 × 32-bit Josephson-junction RAM cell array.

(including two OR-buffer gate times and one inverter circuit switching time), the D line current rise time, the cell operation time, the S line current fall time, and the AND-OR sense circuit operation time. The measured access time is a function of the bias and driver current amplitudes. Over a 93% to 65% bias current range for the Y decoder, the access time varied from 640 to 1150 ps. The D line current was a nominal 0.8 mA, and the S line current was 78% of its 0.2-mA design value for these measurements.

The access time showed similar decreases as a function of increasing D line current, with a maximum time difference between the cells of 60 ps. A minimum access time of 570 ps was obtained for the nearest cell in the array with a 0.187-mA S line current, a 0.88-mA D line current, and a 95% decoder bias condition. The measured times correlated well with the times derived from an ECAP circuit simulation.

Most of the 13 mW dissipated in the RAM is concentrated in the current-regulating resistors in the OR gates of the decoders and in the drivers. This low-power, 570-ps RAM is expected to accelerate the opening of the door to the implementation of a high-performance computer based on Josephson-junction technology. □

Acknowledgments

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A Single-Chip SQUID Magnetometer

N. Fujimaki, H. Tamura, T. Imamura, and S. Hasuo, Fujitsu Laboratories Ltd., Atsugi, Japan

Many applications in biomagnetism and geophysics require sensitive magnetometers that can measure extremely low level magnetic fields. For example, the biomagnetic outputs of the human heart are in the range of 10^{-10} Teslas/$\sqrt{\text{Hz}}$, and the magnetic fields from brain waves are even lower. The most sensitive magnetometers are those based on a SQUID, or superconducting quantum interference device. A typical SQUID magnetometer uses superconducting Josephson junctions that require temperatures close to absolute zero.

The SQUID we have developed operates at 4.2K, which requires the use of a liquid helium bath or other expensive means. Despite this drawback, it does allow us to measure magnetic fields down to 3.3×10^{-12} T/$\sqrt{\text{Hz}}$—a major improvement over most Hall-effect, flux gate, and other types of magnetometers.

For the most sensitive magnetic measurements, a null-balancing circuit is used. With this method, known levels of magnetic quanta are fed back to balance out the field under measurement. However, previous magnetometers based on these techniques suffered from two major drawbacks. The first was the physical bulk of the complex analog feedback circuits, which often used lock-in amplifiers and other large components. The second was the room-temperature operation of the feedback circuit, which necessitated separation from the SQUID sensor's cryogenic environment. In the past, this requirement led to problems in shielding both the feedback circuits and the connecting cables from stray electric and magnetic fields. Furthermore, this situation was exacerbated for multichannel magnetometer systems, where crosstalk between channels added significant problems.

Converting the feedback circuitry to digital technology reduced the noise problems, but we still felt that integrating the loop feedback onto the SQUID sensor chip was the best method of overcoming these problems. However, a single chip dictated the use of superconducting technology for the feedback circuit.

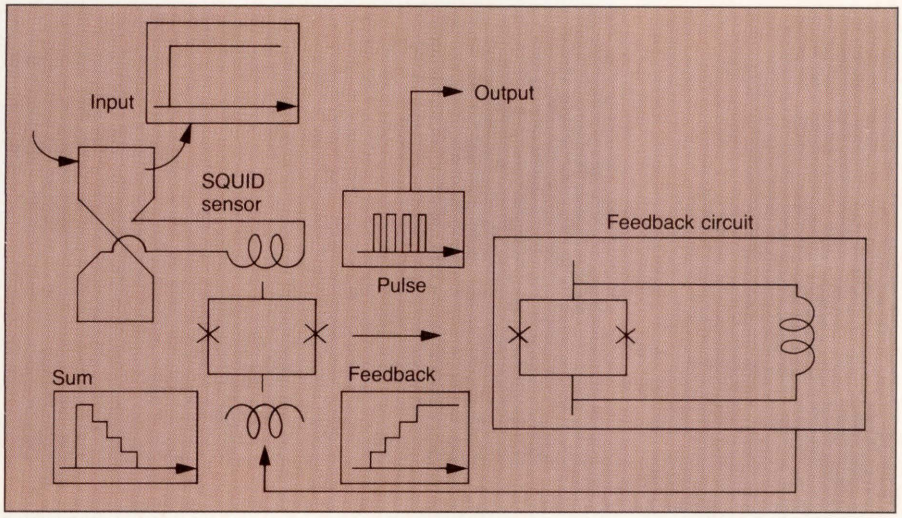


FIGURE 1. Simplified schematic of a magnetometer based on a superconducting quantum interference device (SQUID).

With these goals in mind, we first considered a relatively complex Josephson digital circuit for the feedback loop. However, a large, complex digital circuit on the same chip as the SQUID sensor could easily add to the noise problems. The final design capitalized on the fact that the magnetic flux in a superconducting loop is quantized in integral increments of the basic flux quantum (2.07×10^{-15} Webers), and since a superconducting loop has no electrical loss, the sensed flux quanta can be easily stored. And if write gates are included in the Josephson circuit, flux quanta can be added or subtracted from the quanta stored in the superconducting loop.

The magnetic field to be measured by the SQUID magnetometer is captured by an on-chip 20-turn figure-eight pickup coil (see Figure 1). The output from this pickup coil couples flux to the SQUID sensor. The flux in the superconducting storage loop is also coupled to the SQUID sensor, but with a polarity that allows the SQUID to sense only the difference between the two magnetic flux levels.

The SQUID has been designed for ac bias operation at 600 kHz. This ac operation produces positive output pulses when the net field at the sensor is positive and negative output pulses when the field is negative. The write gate circuitry has been designed to add 1 flux quantum into the loop whenever it receives a positive input pulse, and conversely subtract 1 quantum for each negative pulse.

In normal operation the magnetic field at the sensor produces a series of pulses at the bias frequency. These pulses drive the write gate to introduce flux quanta (1 quantum per pulse) into the superconducting loop, which functions as both an up/down counter and a digital-to-analog converter. The total stored flux quanta in the loop is equal to the total number of positive pulses minus the total number of negative pulses driving the write gates.

The "counted" and stored flux quanta in the loop continue to increase until they null out the field at the sensor. At

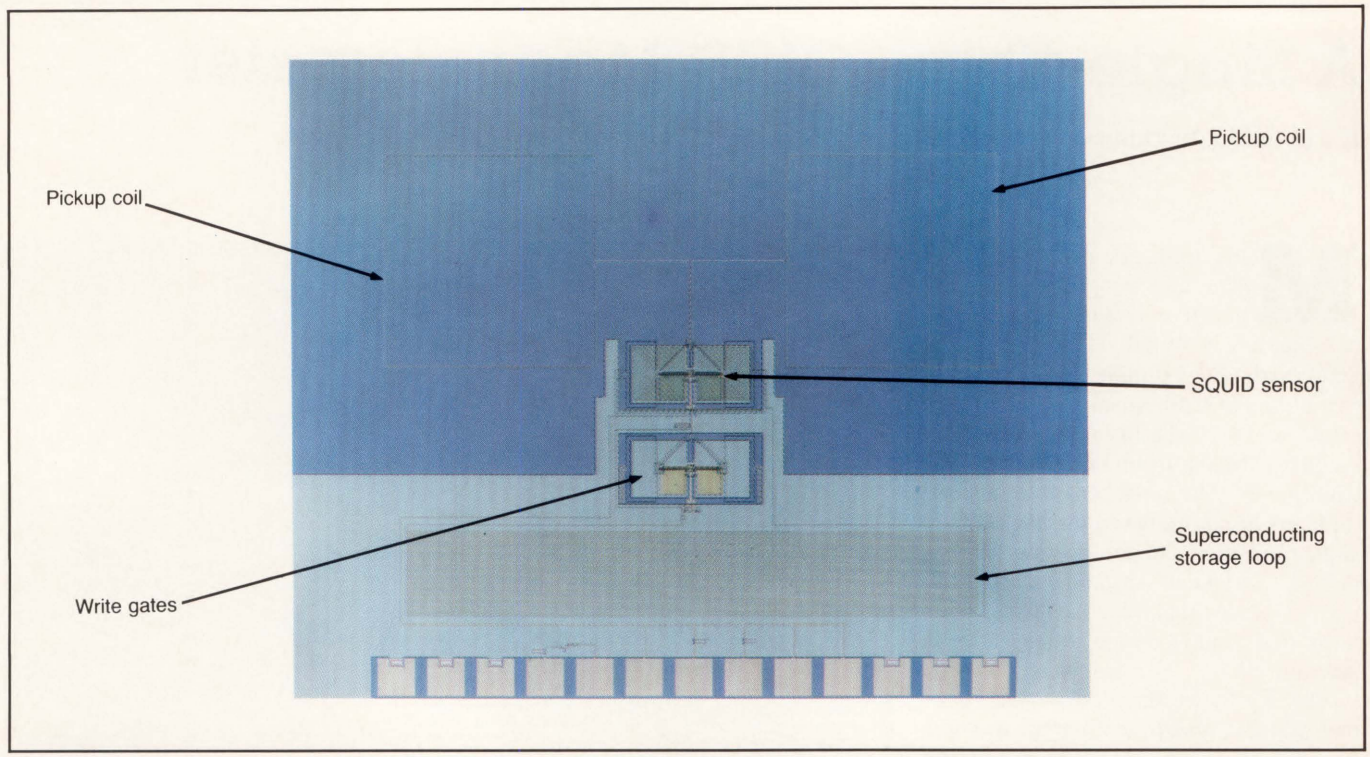


FIGURE 2. The complete SQUID magnetometer is implemented on a single chip.

this point, the sensor ceases to produce output pulses. The final stored count is then equal to the number of quanta coupled to the sensor from the pickup coils. For example, if it takes four pulses to balance out the magnetic field at the SQUID sensor, the field at the sensor is equal to four times the basic flux quantum. The actual magnetic field is then proportional to this count. The scaling factor depends on the size and number of the pickup coils and the percentage of the pickup flux coupled to the sensor. In the present design, the SQUID sensor operates over a range of approximately ± 200 times the basic quantum.

The integration of a complete SQUID sensor circuit and feedback circuit together with the necessary pickup coils on a single superconducting chip has produced a magnetometer that operates in a single cryogenic environment and only requires connections for the ac input bias and output pulses. This highly sensitive magnetometer not only eliminates most externally introduced noise problems, but also provides a high degree of immunity to crosstalk in multichannel systems.

Furthermore, the simplicity of the chip's design should ease the fabrication of multichip magnetometers for sensitive applications such as magnetocardiograms. Also, it should be possible to move the basic design rapidly and easily to the latest "high-temperature" superconducting materials that can operate in a low-cost liquid nitrogen environment rather than the considerably more expensive liquid helium required by the present design. Indeed, the magnetometer could be one of the first practical applications of these new "high-temperature" superconducting materials.

The final design includes the pickup coil, SQUID sensor, write gate, and superconducting storage loop on a 3.0-mm $\times$ 3.3-mm chip (see Figure 2). It was fabricated using niobium thin films, molybdenum resistors, and silicon dioxide layers for insulation. Eight masks were used. The layout was accomplished with a conventional commercially available CAD system. The simulation of the circuit, including the Josephson junctions, was performed with a SPICE program running on a mainframe computer. Some of the sensor and write gate characteristics were mathematically derived to provide circuit parameters that could be used in the simulation. The program, which included the Newton-Raphson method, was written in FORTRAN. □

The High-Temperature SQUID Is Here

In the present superconducting technology race, Japanese and U.S. scientists have taken turns leapfrogging ahead of each other. However, just recently, scientists at the National Bureau of Standards laboratories in Boulder, CO, have grabbed the lead by demonstrating the first practical superconducting device to operate at 81K—a temperature high enough to maintain easily with a liquid nitrogen environment (77K). The superconducting quantum intreference device, or SQUID, was designed and constructed by James E. Zimmerman, a retired NBS physicist now working as a guest researcher at the labs. The basic superconducting material, yttrium barium copper oxide, was made at NBS's Center for Electronics and Electrical Engineering by Ronald Ono and James Beall. *—Roland C. Wittenberg*

Putting PS/2 POS in the 5AC312 EPLD

Pedro Vargas, Intel Corp., Folsom, CA

The introduction of the IBM PS/2 (Personal System 2) models and their innovative Micro Channel bus has provided numerous opportunities to develop creative interface solutions. Although the interface requirements are new, the designer is faced with making a familiar choice: using discrete SSI/MSI chips, incorporating a PLD, or going for a custom IC solution.

In the past, using TTL on the PC, PC XT, and PC AT expansion boards was often a good choice, but the smaller size of the PS/2 "plug-in" adapters makes area dramatically more important. The custom-chip solution is probably the best for companies that have a well-defined product and large volumes and can afford the cost of the chip development. The other choice, using a PLD, is one that has not been popular in PC bus interfacing owing to the limited function and performance of most PLDs.

Programmable Option Select

The PS/2 models use software instead of hardware for adapter configuration. This feature, called Programmable Option Select (POS), eliminates the need for switches on the motherboard and adapters by replacing them with programmable registers.

The motherboard and each connector on the Micro Channel has a unique signal called $\overline{\text{CD SETUP}}$ that initiates a setup mode when it is active. Only one connector at a time can be in the setup mode, thus providing an organized way to perform initialization.

Each adapter must implement POS with eight registers. Depending on the adapter function, not all of them need to be used. The first three (POS registers 0, 1, and 2) are required because they provide the adapter ID and the adapter enable/disable function necessary during setup and error checking. The other five (POS 3 through 7) hold Option Select and Address Extension bytes that identify what sort of device drivers the operating system should apply to the board. The IBM Technical Reference Manual (1987) provides a table for suggested ID bytes arranged by adapter type.

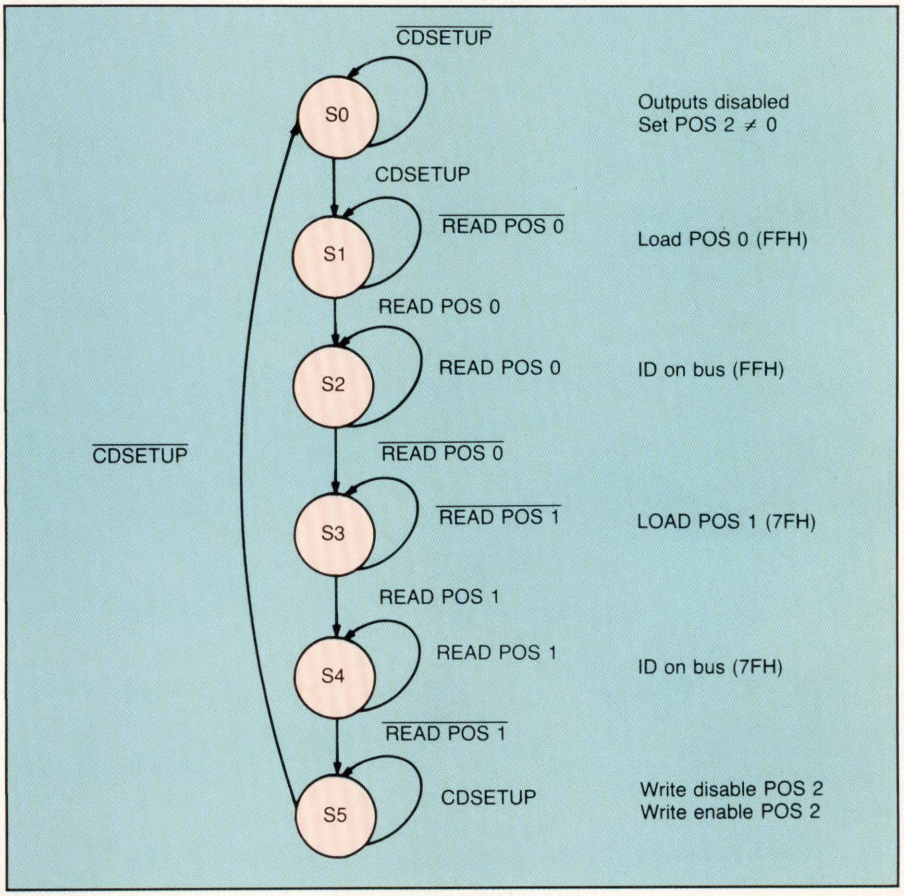


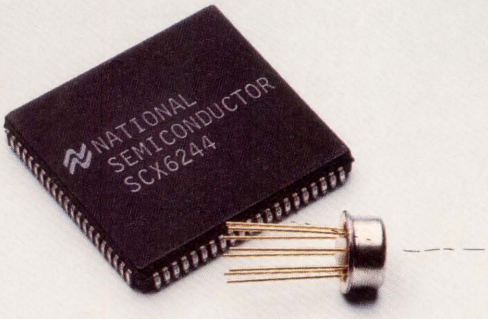
FIGURE 1. State diagram for a PS/2 POS implementation.

In brief, the system uses POS thus:

1. The system selects the adapter to be placed in setup mode by driving its $\overline{\text{CD SETUP}}$ signal active.
2. The adapter is identified by reading two ID bytes from POS 0 and POS 1 (hexadecimal 100 and 101).
3. The adapter is disabled by writing a logic 0 to POS 2 (hex 102).
4. If implemented, Option Select Data is written to POS 3, 4, and 5.
5. The adapter is enabled by writing a logic 1 to POS 2.
6. $\overline{\text{CD SETUP}}$ goes inactive and the adapter is out of the setup mode.

The POS bytes (hex 103, 104, and 105) are used with multifunction adapters that reside in a system with similar adapters. The design example in this article was actually engineered for an Intel single-function card that incorporates four modems with an 80C186 acting as a controller. Since the adapter performs only one function, there was no need to implement the Option Select bytes. In this case, the only requirements were to provide the ID bytes and the enable/disable features, which are

National Semiconductor



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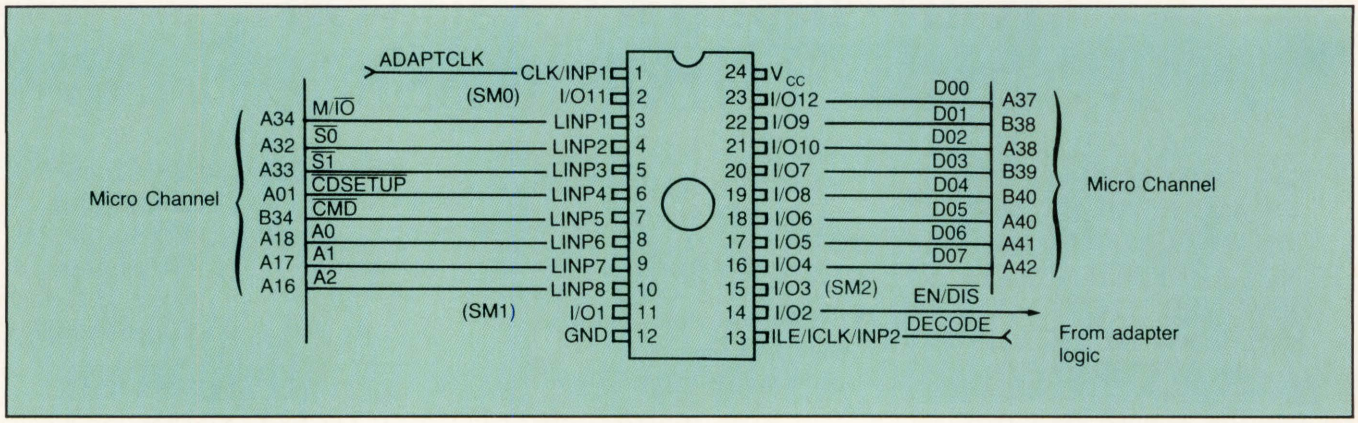


FIGURE 2. Pin-out for a 5AC312 Micro Channel interface.

done with POS registers 0, 1, and 2.

The modem card falls under the category of storage device, so 7FFFH was chosen. IBM has assigned unique IDs for its own cards, but the third-party choices are up for grabs. Thus more than one company could assign the same ID to their cards. In that case, companies that implement the POS function in discrete TTL or a custom IC will have to redo the design or cut and jumper the board. Using an erasable PLD for this application minimizes the risk of conflicting IDs, since all that is needed is to burn another EPLD with the appropriate bytes.

A State Machine for POS

Figure 1 shows the state diagram for a state-machine implementation of POS. During S0 (state 0), the machine idles until CD SETUP is driven active. The adapter must already be disabled and POS 2 must be zero during power-up and reset. When CD SETUP is driven active, the machine goes to state S1 and loads the least significant ID byte (FFH). It remains in S1 while waiting for a READ POS 0 command. As soon as POS 0 is read, the machine cycles to state S2 and issues FFH. Once READ POS 0 is inactive, the machine cycles to state S3, during which it loads the second ID byte (7FH) and waits for the READ POS 1 command. The last ID byte is put on the bus when READ POS 1 comes and the machine goes to state S4. Since we know that the next two setup operations are I/O writes, the machine remains in S5 while POS 2 is disabled and enabled per the Micro Channel bus specification.

The POS requirements placed on our modem adapter are easily met by putting a 5AC312 to some creative use. In terms of performance, the 25-ns propagation delay is more than adequate for the system requirements during the setup mode. POS registers 0, 1, and 2 can easily be accommodated by the 12 macrocells. Eight macrocells are used to load and send the ID bytes from POS 0 and 1. One macrocell is used as the LSB of POS 2. The remaining three macrocells make up a state machine that internally sequences through the setup mode.

At power-up and reset, the chip registers come up as 0, in accordance with the design requirements. Inputs and outputs are registered in the 5AC312, enabling the bus inputs to be synchronized and clean output signals to be generated.

A device enable signal is generated by CD SETUP and the appropriate port select address (indicated by CDEN). This function requires 11 product terms. With conventional PLD architectures, this requirement would almost invariably result in the use of two macrocells to obtain the requisite product-term width. With the 5AC312, if a design has more than eight product terms, four additional product terms can be "borrowed" from the adjacent macrocells. Product terms are reallocated in such a manner for the device enable signal. Without this variable product-term allocation, the POS function would not have fit in one chip.

The output enable control signal needs two p-terms for each macrocell. Again, without the 5AC312 some workaround would have been needed.

The final state machine operation entails that the 5AC312 remain in S5 while POS 2 is consecutively enabled and disabled. This is a bit-write of a register and is easily done by using the 5AC312's dual feedback capability. Though bit 0 of POS 2 uses the D00 line, internally it is routed to a separate register. Without dual feedback, this internal transceiver function would be impossible to implement.

Figure 2 shows the pin-out for this POS implementation. The definition of the signals is given in the IBM literature.

Conclusion

Using a 5AC312 enables the designer to place the entire function in one EPLD (transceivers may still be required). This modem adapter POS implementation was easily done in one 5AC312 device. An equivalent implementation in 16R8s would have required two devices.

Adding other Micro Channel interface features like arbitration or interrupt sharing would certainly be too much for this one device. Since this adapter did not have those requirements, it was not a problem. However, a complete POS implementation with Option Select bytes and other features could be done with the 5AC312's future family members.□

Acknowledgments

Many thanks to Thom Bowns and Dan Smith for their help with this article.

References

IBM Corp. 1987. *IBM Personal System 2, Model 80, Technical Reference.*

IBM Corp. 1987. *IBM Personal System 2, Hardware Maintenance Reference.*

Intel Corp. 1988. *Intel 5AC312 EPLD Data Sheet.*

GaAs Standard Cells Use SCFL Logic for 2-GHz Toggle Frequencies

Users of gallium arsenide can usually be characterized as those requiring the ultimate in high-frequency performance or those not pushing the upper frequency limits, albeit still requiring hundreds of megahertz, but wanting lower power consumption. TriQuint Semiconductor attempts to satisfy both groups with its QLSI standard-cell family, the first cell-based GaAs product to use enhancement/depletion-mode technology.

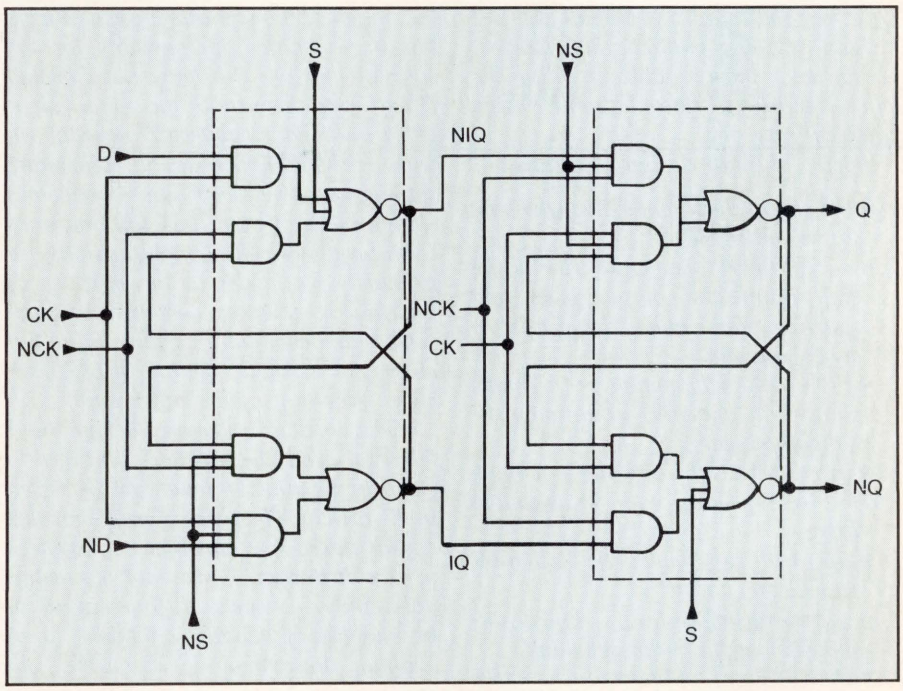
The QLSI family consists of two types of logic: zero-diode FET logic (ZFL) and source-coupled FET logic (SCFL). The SCFL logic is a new development, and the ZFL cells are lifted directly from TriQuint's TQ3000 gate array. The family includes logic cells as complex as full adders, as well as latches and flip-flops.

The SCFL cells use differential signals, much like ECL. SCFL devices use each signal and its complement to switch cell currents with small voltage swings (see the figure). This scheme provides similar benefits to ECL, particularly high operating frequencies—a 2-GHz toggle rate for the SCFL cells—and high common-mode rejection. However, maintaining differential currents results in higher power consumption.

ZFL operates at lower operating frequencies—1 GHz—but requires much lower power: 2.4 mW per cell, versus 8 mW for SCFL gates. Also, ZFL requires only half the interconnects of differential logic, improving the chip density.

There are some drawbacks: A ZFL flip-flop requires four cells, while only two SCFL cells form a flip-flop, and one cell forms a latch (as shown in the figure). The delay-power product for ZFL circuitry is therefore half that of the SCFL for logic gates, but roughly equivalent for latches and registers.

TriQuint is also developing lower-power SCFL cells for such applications as cellular radios and beepers. It is also working on shrinking the size of the ZFL cells to allow denser designs requiring even less power.



A source-coupled FET logic (SCFL) master-slave flip-flop cell.

ZFL and SCFL cells can be mixed in the same design. One side of the SCFL's differential output can be used to drive ZFL cells directly, and if required, TriQuint can make ZFL cells drive SCFL cells by assigning the proper supply voltages to the ZFL circuits.

All cells need a 5-V power supply range, although the SCFL cells operate from 0 to −5 V. Two supply voltages are necessary if the SCFL designs have to drive CMOS, TTL, or pseudo-ECL (+5-V) signal levels. A +5-V SCFL family of cells is also under development.

Users can specify TriQuint design kits containing logic symbols and digital models that run on Mentor Graphics' workstations. Kits for operation on workstations from Tektronix's CAE Systems Division and Daisy Systems are expected in June. The design manuals and kits cost $995. NRE charges start at $60,000. Designs as large as 6,000 gates can be accomodated.

TriQuint also offers Multi-Project Chips (MPCs) that contain dice from several customers. By designing to the fixed die size of the MPC, customers can get fabricated dice for only $22,000 or tested dice for $35,000. This service, however, does not include production masks. MPCs are run approximately three times annually.

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Letters continued from page 9

these important features of ACE, I don't feel that my mistakes significantly affected the overall results. It was predominantly ACE's slow response time, coupled with its inability to replicate parts, that led to its relatively poor showing.

• Insufficient information about the design. *Of course the schematic shown in the* User's Guide *did not require 260 minutes to complete. That schematic represented only one level of the benchmark design. I did not submit the full design to* VLSI *for publication because it would have been unable to allot the space required to reproduce the design in its entirety.*

Briefly, the full design contained:

- *the main-level schematic (the one shown on p. 36)*
- *a chip-level schematic (including chip input and output pads and showing the main level as a subcomponent)*
- *the CNTRL subcomponent (a small, finite-state machine containing 14 subcomponents)*
- *the ENGRG subcomponent (a bank of 16 flip-flops with load-enable logic)*
- *the SUB subcomponent (a 16-bit subtracter)*
- *the 16-bit multiplexers shown (unlabeled) in the main schematic*
- *the OR gate, composed of a NAND gate and two inverters*

Each of these components included both a network and a symbol. I have sent Daisy and Mentor a copy of the entire design; and I am certainly willing to supply additional copies to others who request them. Perhaps seeing the entire design will make ACE's total entry time seem more plausible to Daisy.

It should be noted that the entry time I reported for ACE did not include either the time that the engineer spent modifying the "nested file" ACE requires for a design re-using hierarchical subcomponents or the time spent in repairing the schematic damaged by the diagonal-wire bug reported on p. 33. Both of these obstacles cost the user considerable time, but they were not held against ACE in my evaluation of its overall performance.

• Not showing all the schematics. *I did supply* VLSI Systems Design *with a figure that showed the same schematic produced by all four editors. Because of space requirements,* VLSI *did not publish it.*

I would also like to point out that the schematic published on p. 36 and represented as having been entered on LSED appears to have been somewhat modified by VLSI *during the process of readying the piece for publication. In particular, much of the text attached to objects has been omitted, presumably for the sake of clarity. This may have misled Daisy as to the ease of the panel. Also, LSED does not provide arrowheads on wires resembling those the schematic shows; nor do the off-page connectors shown in the figure look like the ones LSED produces. These modifications are primarily irrelevant to the purpose of this figure, however, which was to describe the benchmark circuit, not to acclaim the aesthetic quality of LSED designs over that of the other editors.*

• The design. *I selected a design that I felt exercised the editors' abilities to perform the kinds of functions discussed in the article. The types of problems this circuit posed are common occurrences in circuit design. It was not unreasonable either to expect all four editors to be capable of dealing with them or to evaluate the manner in which they did so.*

I agree that providing the complete design, had space permitted, would have benefitted the reader enormously; however, I do not think the design in any way favored one editor over another. I hope that Daisy, upon reviewing the design, will agree that it is not extraordinary in nature.

In summary, I tried to create a study evaluating the usefulness of these schematic editors to the engineers actually using them. Specifically, I wanted to measure their ease of use for the everyday designer, not simply to record responses within the ideal-world parameters of vendor-provided demos. Unfortunately, as Daisy aptly points out, it is impossible to guarantee equality of user proficiency in a study such as this one. The results of this comparison are, therefore, to be considered approximate and preliminary.

News continued from page 14

point processors from Weitek Corp. (Sunnyvale, CA) each contain a 64-bit multiplier, a 64-bit ALU, a circuit block that performs division and square-root calculations, a 32 × 64-bit six-port register file, and status and control logic. At their highest clock rate of 10 MHz, they are capable, through concurrent operation of their constituent functional blocks, of a peak execution rate of 20 MFLOPS.

The 168-pin WTL 3364 has three 32-bit ports: one bidirectional, one input, and one output. The three buses can be configured as one 64-bit bidirectional bus. The 144-pin WTL 3164 has a single bidirectional 32-bit bus. It is more appropriate as a coprocessor in microprocessor systems, whereas the WTL 3364 is better where high I/O bandwidth is critical.

Functionally, the two chips are identical. Their multipliers, ALUs, and divide/square-root units are independently controlled, so that they can execute instructions concurrently. All multiplier and ALU instructions require a single cycle to complete; double-precision division and square-root operations require 17 and 30 cycles, respectively.

Weitek has been suppling samples to beta-site customers since January, and production volume is scheduled for July. The WTL 3164 in 10-piece sample quantities sells for $829.

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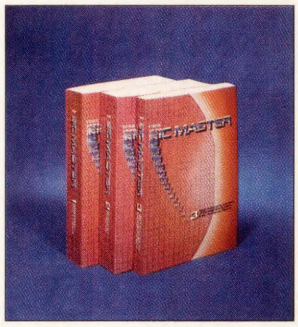

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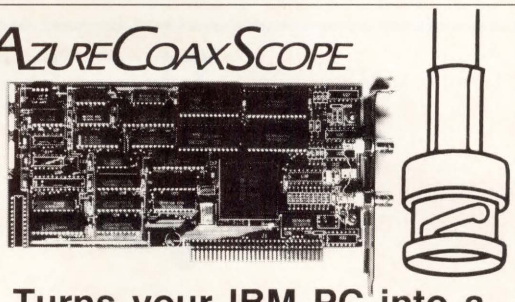

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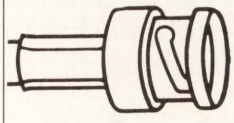

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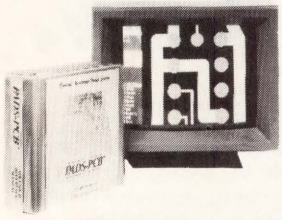

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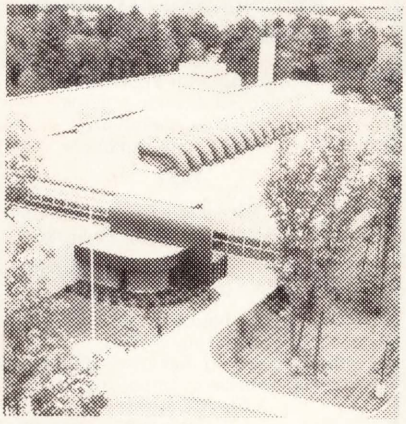

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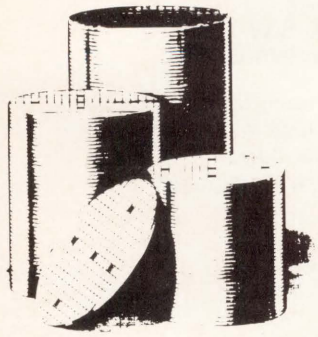

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Responsible for technical strategy and operations to manage vendor, technology and device selection, specification, qualification and production support for standard VLSI business. Requires BS in engineering or computer science and MBA with at least 10 years' technical and business operations experience in computer/ semiconductor industry.

PRODUCT ENGINEERING SUPERVISOR

Provide technical leadership of a group responsible for the technical aspects of non-volatile memory devices (PROM, EPROM, EEPROM). Interface with IC vendors, design engineering, and manufacturing. Requires BS in physics or equivalent and at least 5 years' semiconductor technology with supervisory experience.

For the preceding positons, please contact: Jerry Temple, Department 0401 8825, Digital Equipment Corporation, 111 Locke Drive, Box 1006, Marlboro, MA 01752-9106.

To cash in on these blue chip opportunities with a $9.4-billion computer company, please contact the appropriate person listed above.

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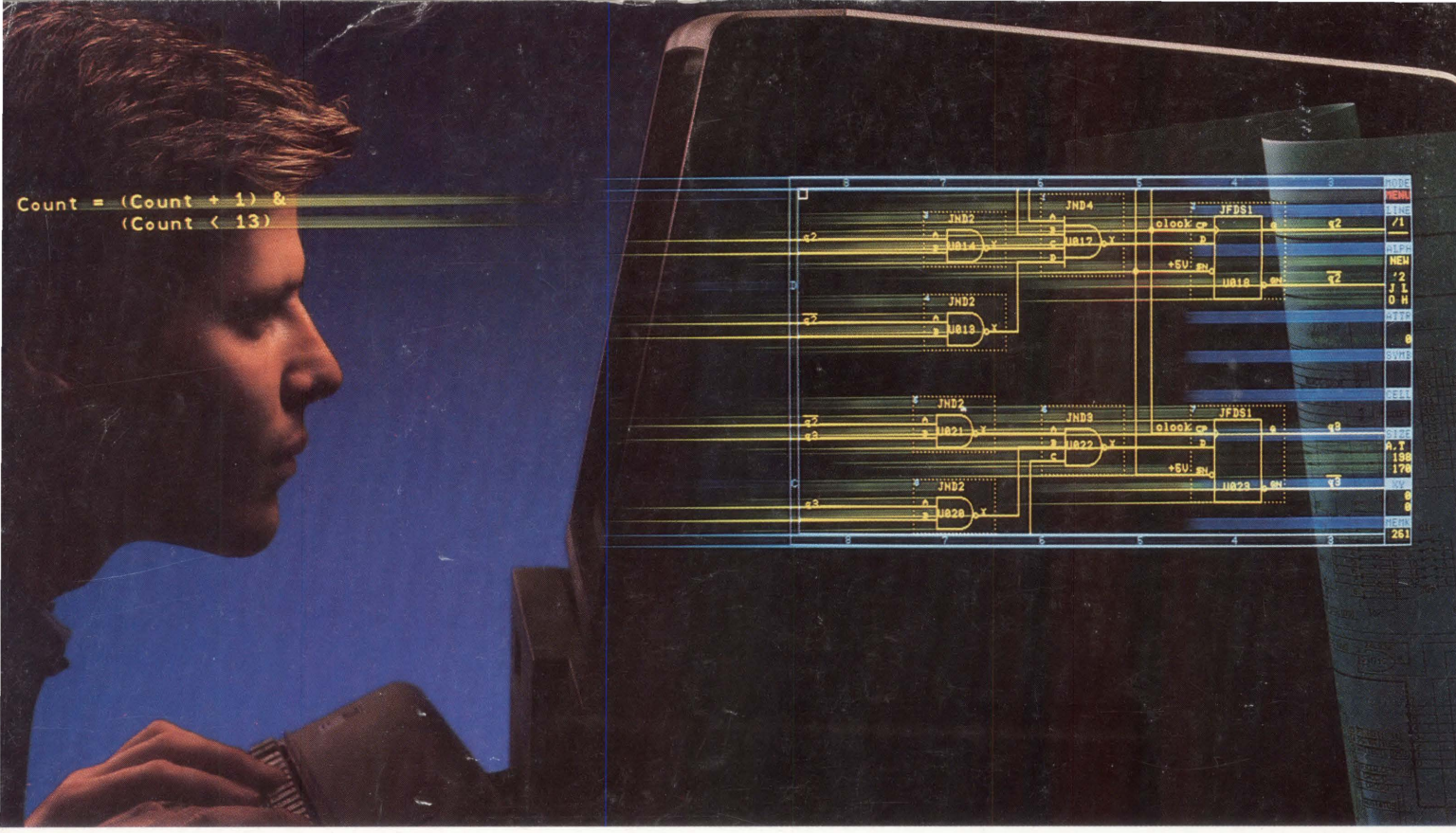

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