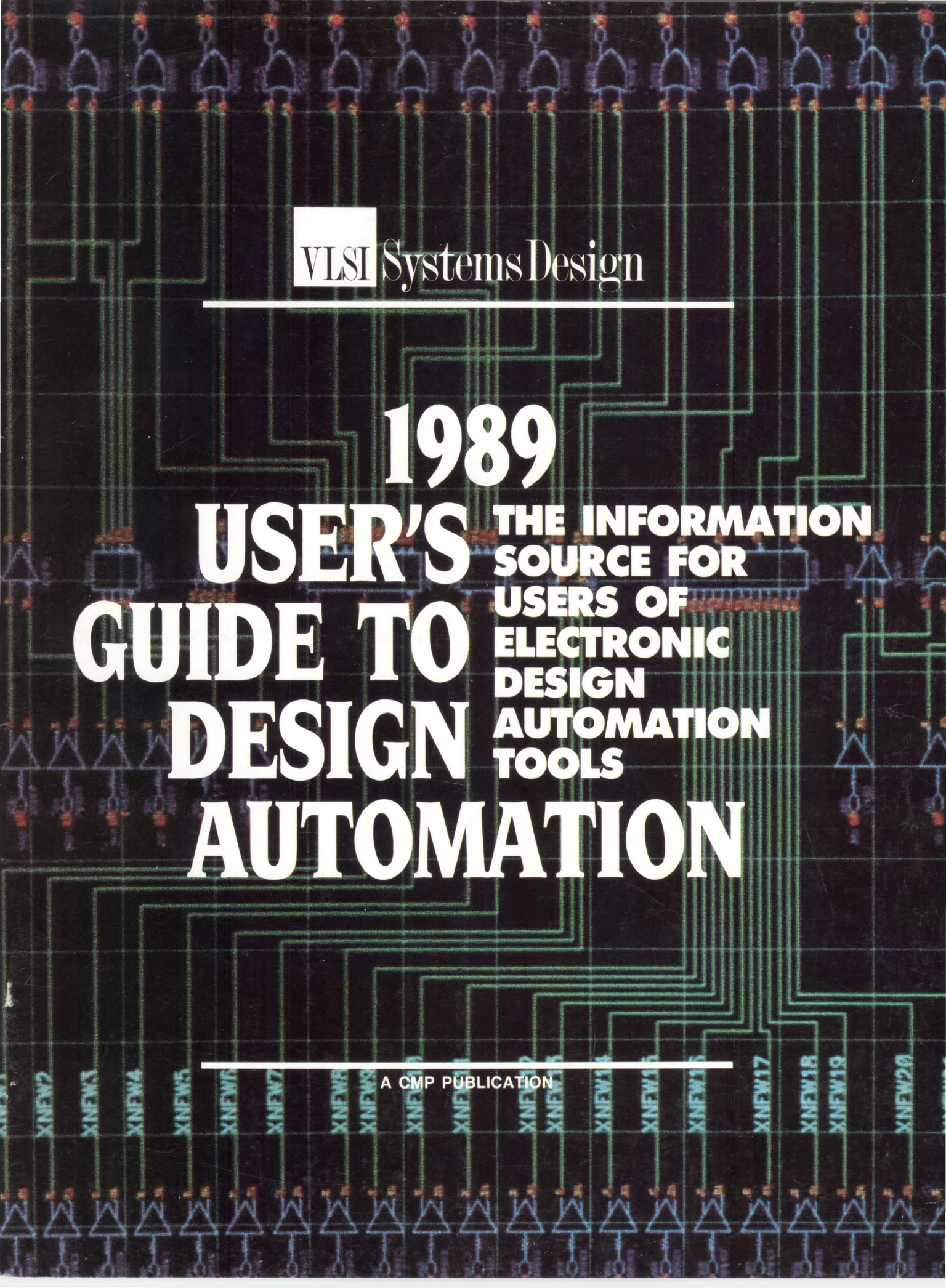


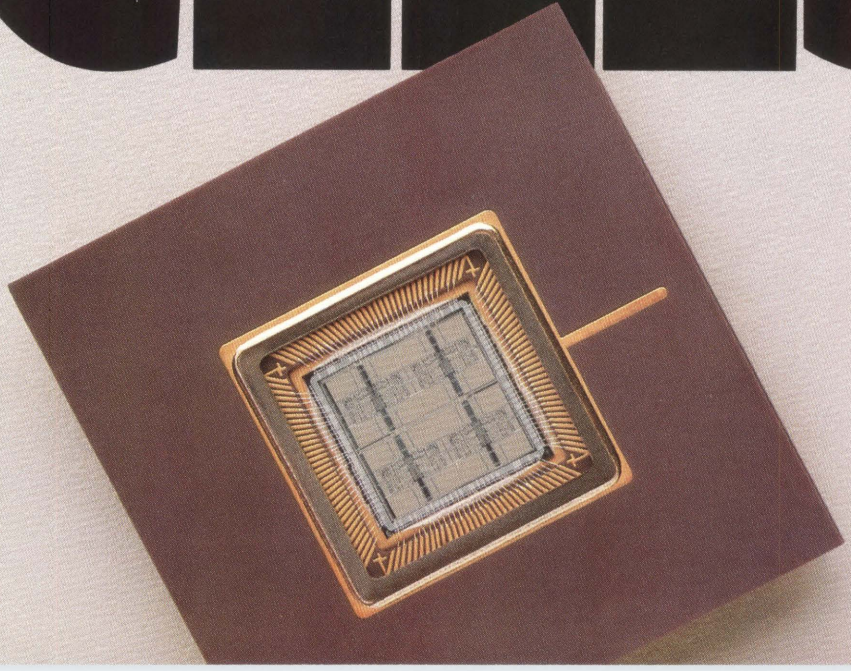
VLSI Systems Design

1989 USER'S GUIDE TO DESIGN AUTOMATION

THE INFORMATION SOURCE FOR USERS OF ELECTRONIC DESIGN AUTOMATION TOOLS

A CMP PUBLICATION

BUILD KILLER CELLS.



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A cell design with 200,000 gates. More than 1000 library elements. 2MB of memory. And sub-micron HCMOS technology.

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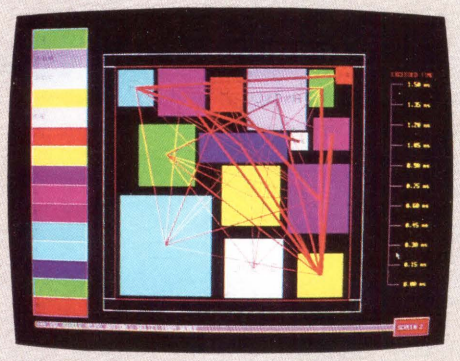

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CIRCLE NUMBER 1

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VLSI Systems Design

A CMP Publication

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FEATURES

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INTRODUCTION TO THE GUIDE

The past five years have witnessed the maturing of the design automation industry and its products. These products started as relatively crude tools for IC design that were not only difficult to operate, but also difficult to use without an extensive background in IC technology. However, today's tools have reached out to the system designer and other designers who are not necessarily knowledgeable in the IC arena, and who may be primarily interested in taking advantage of ASICs and standard VLSI chips without being required to learn their technologies in detail.

The tools continue to reach out for these system designers. Even the PCB-CAD tools, which predated the IC-CAD tools by many years, have moved from a relatively independent, design/manufacturing-based tool set to an integrated design environment that is more closely aligned with the systems engineer's requirements. The most touted benefit of today's design automation tools has been the ability of these tools to free up designers from many of the details of design. This fosters the designer's ability to quickly optimize their designs with many iterations of the overall system or any of its parts. For instance, electrical rule checking has freed the designer from the tedious and time-consuming task of checking thousands of gates for such rules as fan-in, fan-out, proper load terminations, and grounding of unused inputs. Design rule checking performs a similar function for the physical layout of the integrated chip or printed-circuit board.

Functions such as these are included in most of today's tools. In addition, this trend toward the embedment of more intelligence in tools over the past few years has encouraged an increased use of artificial intelligence and expert systems by design tool vendors. Two articles covering these topics have been included in this issue of our *User's Guide to Design Automation*. They both provide an overview of knowledge-based design environments and discuss such topics as logic synthesis and expert systems, but each author provides an overview that is based on his own company's (Texas Instruments or NCR Microelectronics) particular design environment.

As in the past, *VLSI's* guide has been designed to serve as a reference for both the ASIC designer and the systems engineer. The guide has complete and updated directories that list most of the design automation tools now available (together with their vendors) for three categories of products: CAE entry and analysis systems; integrated circuit layout systems; and printed circuit board layout systems.

— Roland Wittenberg

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CIRCLE NUMBER 2

LOGIC SYNTHESIS AS A FRONT-END TOOL IN AN ASIC DESIGN ENVIRONMENT

Bryan Bell and Glenn Woppman, Texas Instruments Inc., Dallas, Texas

Logic synthesis has become somewhat of an industry buzzword—conjuring up visions of high-level designs automatically converted into optimized gate-level implementations. Rather than an esoteric design tool, synthesis is a key bridge between logic design and *ASIC* physical implementation.

Logic synthesis brings a set of key capabilities to *ASIC* logic design. It relieves systems engineers of implementation drudgery, permitting them to concentrate on design functionality. It also automatically provides logic minimization, gate optimization, and design-rule enforcement. Relieving engineers of these time-consuming tasks cuts design-turnaround time, and enables engineers to get products out the door faster while still maintaining quality control.

Logic synthesis also provides an interactive design front end to *ASIC* designers. One logic synthesis tool—the Logic Consultant from Trimeter Inc. (Pittsburgh, Pa.)—will serve as a front-end design tool for engineers working with *TI*'s *ASIC*s. Since early 1988, *TI* designers have been working with Logic Consultant. This tool has given *TI* engineers a fast, reliable method to optimize its *ASIC* gate array and standard cell designs.

TI has developed two knowledge bases necessary for the Logic Consultant to serve as a design front end (Figure 1). One knowledge base accommodates the TGC100 Series 1-micron gate array family; the other serves the TSC500 1-micron standard cell family.

This software should solve one of today's major design problems—the conversion of *PLD*-based designs into *VLSI* logic. With the Trimeter Logic Consultant front end, engineers can directly convert *PLA*-based designs into *ASIC* gate-level designs that will be optimized for area, power, or speed constraints. This capability permits engineers to use *PAL*s for prototypes and more efficient *ASIC* chips for production.

Designers will also be able to work at higher levels of abstraction. Instead of working at the gate or *ASIC* logic-function level, they will be able to use logic equations, *PAL* equations, finite state machines, or truth tables to specify designs and improve productivity (Figure 2).

Thus, the system designer can now concentrate on design functionality, passing off much of the implementation details to a software assistant such as the Logic Consultant. With this new tool, designers can try different design choices or rework a design automatically to meet different timing and area constraints.

LOGIC CONSULTANT

The idea behind logic-synthesis software such as Trimeter's Logic Consultant is straight-forward: Designs are converted into an intermediate generic form that can be logically minimized. This minimal form is then mapped onto a given *ASIC* technology library.

For design analysis, the Logic Consultant includes a schematic analyzer. With it, the designer can interactively specify and examine highlighted critical paths in a design. These paths can be chosen based on minimum pin-to-pin signal transitions.

A designer can try different tactics and then examine the results interactively for key critical signal paths. Additionally, the designer can also print out a schematic of the gate-level design for documentation or further analysis.

KNOWLEDGE BASES

Libraries are a collection point for design information. *TI*'s 1-micron *ASIC* library has more than 461 elements in it, and *TI* is working on an additional 71 complex functions. Many of the library's elements have been added at the request of *TI* customers. This library forms a common knowledge pool, permitting designers to benefit from the experience of other engineers doing diverse designs.

To allow system designers to maximize their use of the *ASIC* library, *TI* has developed two knowledge bases (*KB*s) to supplement the Logic Consultant. The TSC500 Series *KB* is developed from *TI*'s 1-micron standard-cell family while the TGC100 Series *KB* was developed from *TI*'s 1-

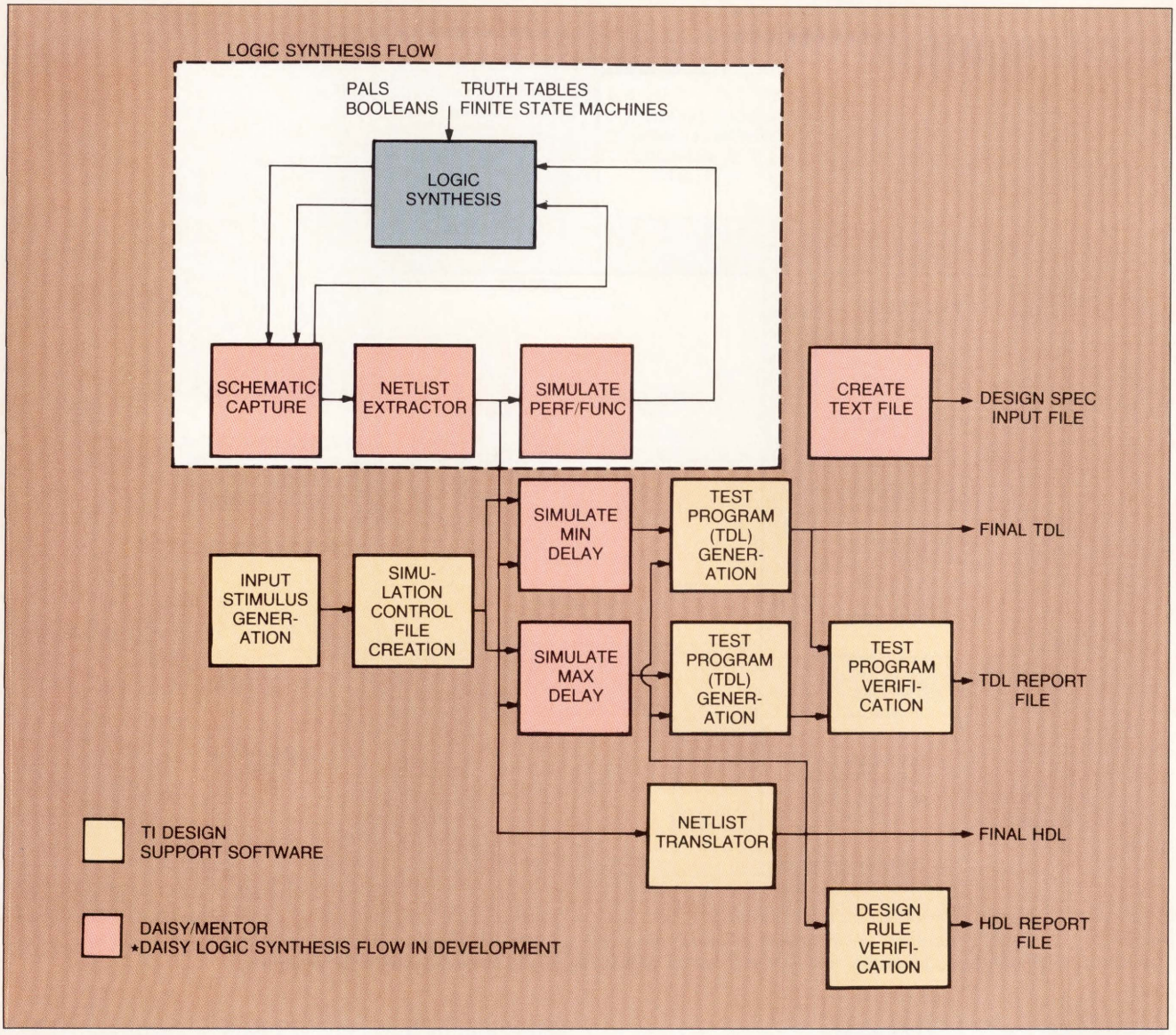


Figure 1. The TI logic-synthesis design environment is shown here with its basic parts. The logic-synthesis function front end accepts inputs in most of the forms a design engineer would use—PALs, Booleans, truth tables, and finite state machines.

micron gate array family. The two knowledge bases comprise all the functionality that is offered in the corresponding *ASIC* libraries.

These knowledge bases form the technology platform for mapping generic designs into the given *TI* gate array or standard cell implementation. Engineers can enter their designs in a higher level form—such as logic equations, truth tables, or *PLD* equations—for conversion into *ASIC* gates. Alternatively, they can use standard schematics that will be converted into an intermediate form and then synthesized.

Logic synthesis allows engineers to design using generic gate types. The software design can be counted upon to optimize such a design by selecting more suitable library logic functions to meet area, timing, or power constraints. Done this way, design can become more of a two-step process—doing the top-level design, and then the technology-dependent implementation.

This approach will make it easier to move designs between different circuit technologies. The logic synthesizer is then responsible for implementing the design into a *TI* gate array or standard cell.

A final library advantage to using logic synthesis is that the designer is now freed up from the restrictions of the library itself. In effect, the designer can define his own soft macro elements or logic modules, and be secure in knowing that they are optimized for the given *ASIC* technology.

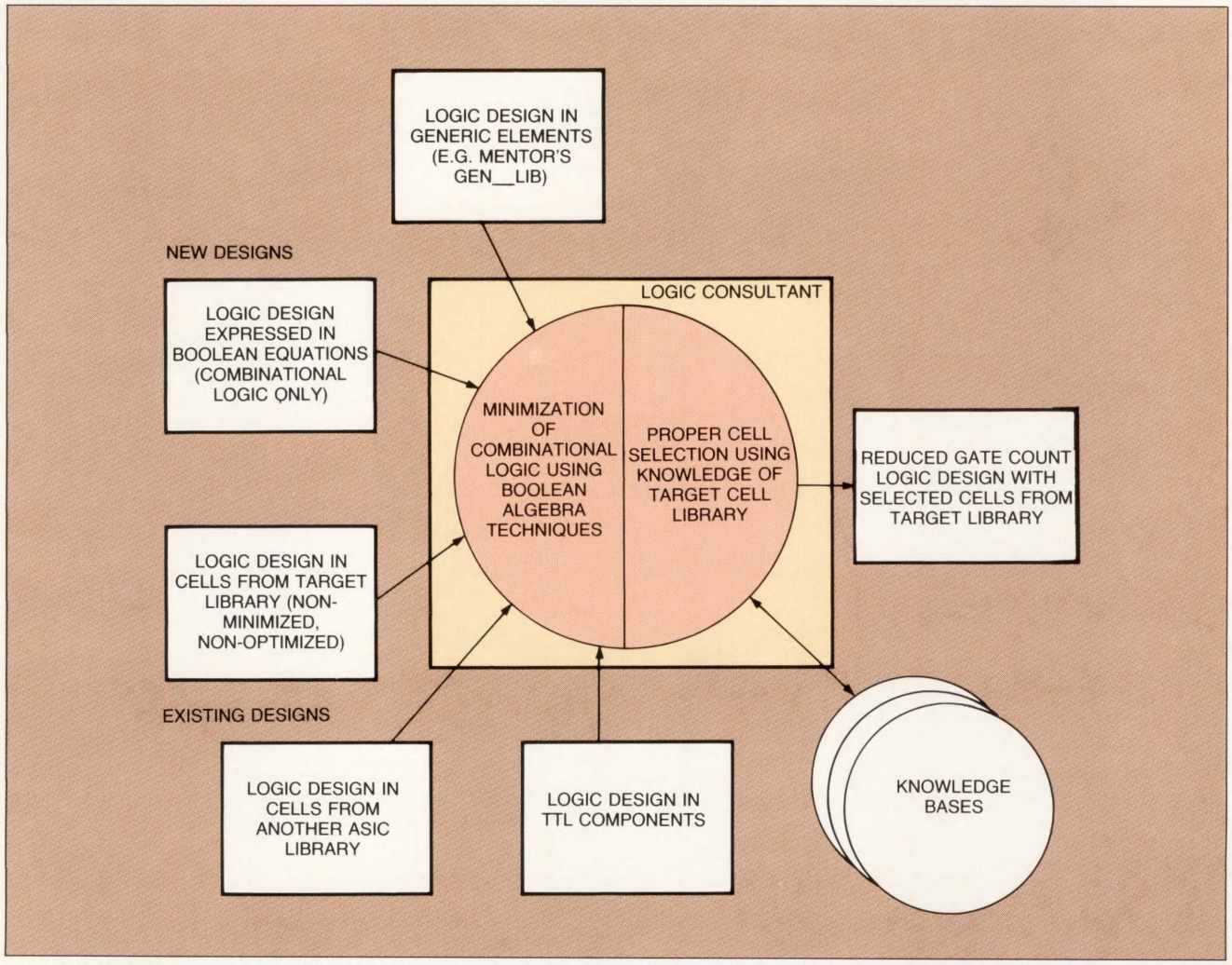


Figure 2. The Logic Consultant environment is shown here with its various possible inputs. Knowledge bases built around TI's TSC500 Series standard cell family and TGC100 Series gate array family are available to the designer.

THE PAYOFF—PAL CONVERSION

Few high-performance designs use discrete logic anymore. Instead, they tend to use either *VLSI* or *PLD*s. For example, the new Series 10000 workstation from Apollo Computer Inc. (*VLSI* Systems Design, August 1988, pg. 60) has almost no discretes.

In fact, many board-level designers find themselves using a *PAL*- or *PLD*-based design to test-market or prototype a product. With logic synthesis to handle the implementation details, they can easily shift their designs to more efficient, cost-effective gate arrays or standard cells when the product or design is stable.

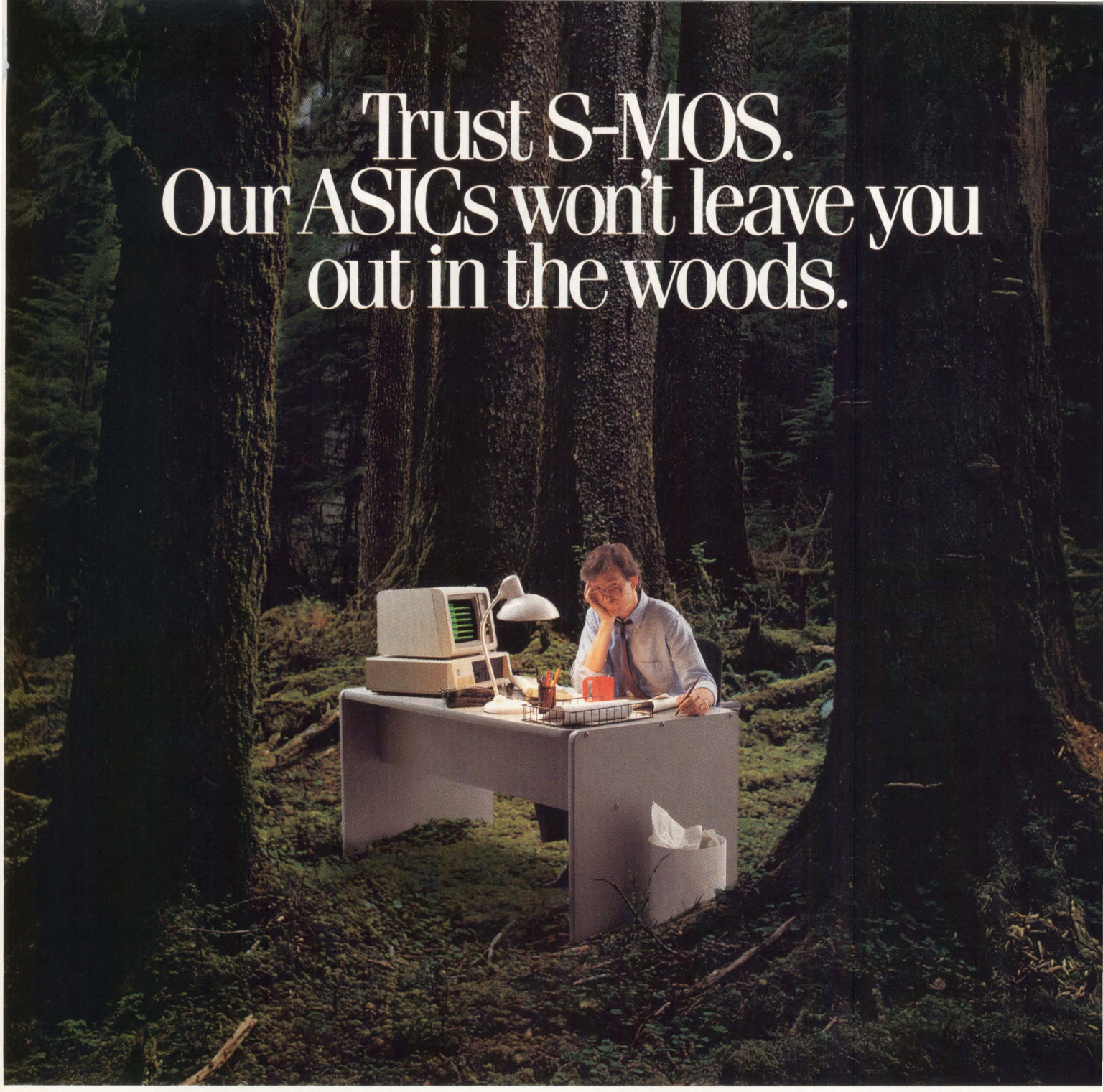
However, the conversion of a *PAL* to an *ASIC* is not a trivial task. *PAL*s simplify design by providing a large number of sum-of-product terms to be handled in a minimal number of logic levels—two or three. Doing this with standard logic gates in *VLSI* can deepen the number of logic levels, increasing both the circuit area and the delay time in traversing the logic.

A large function library, however, can minimize this effect by furnishing enough specialized circuits to avoid deepening the chain. Unfortunately, most designers are forced to do this conversion by hand. Such a conversion typically takes three to seven days for relatively simple *PLD*s, and longer for complex circuits.

Logic synthesis offers a perfect way out of this dilemma. For one thing, the software accepts high-level circuit descriptions; for another, it performs the lower level implementations automatically. And finally, it allows the designer to control the final implementation by specifying timing and area constraints.

PAL DESIGN EXAMPLES

TI regional technology centers have already been using the Logic Consultant to handle *PAL* conversions. In one system design, a *PAL* circuit (10-ns *TIBPAL* 16L8-10CN)



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CIRCLE NUMBER 5

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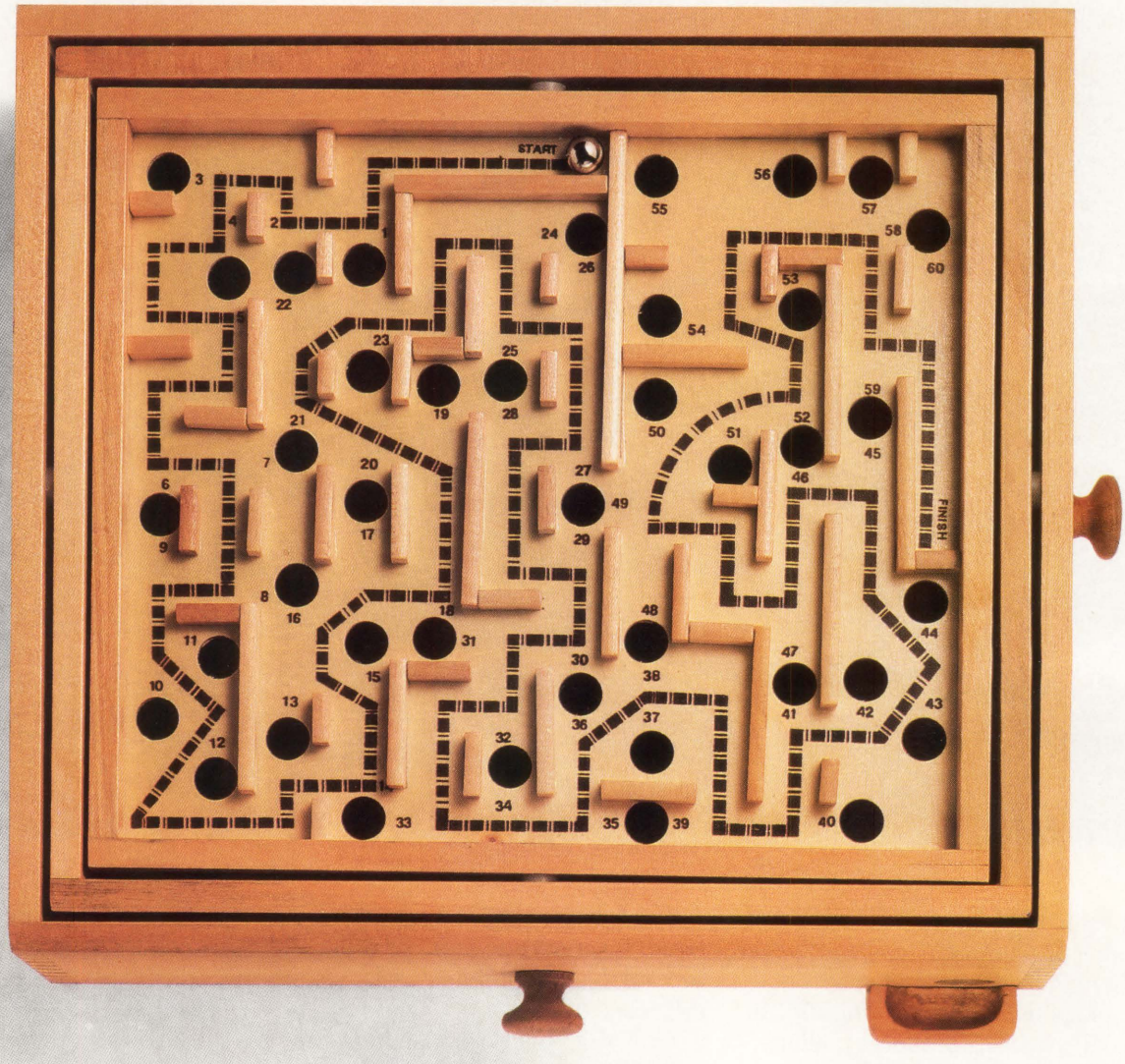

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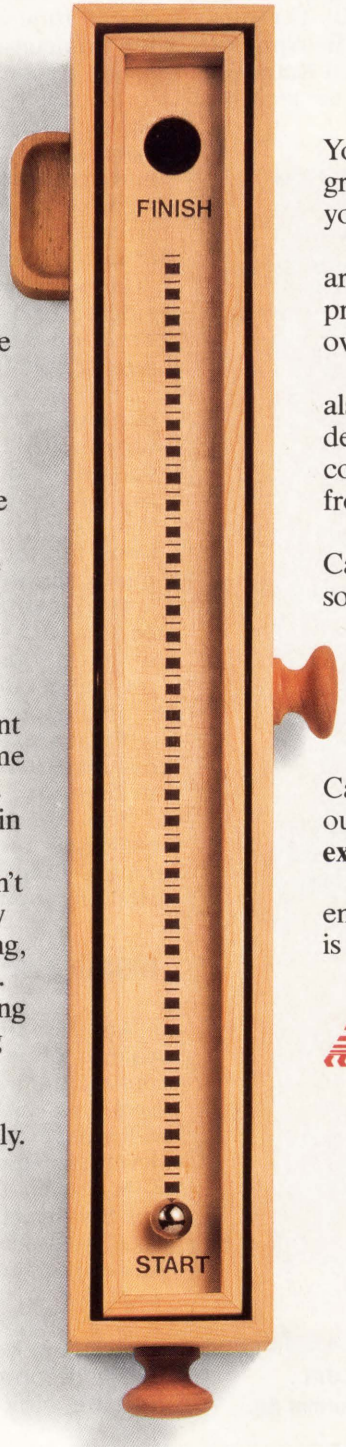

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CIRCLE NUMBER 3

was converted into *ASIC* gate logic using the Logic Consultant in less than 20 minutes—from *CUPL* file source-file input to schematic output. In contrast, it usually takes an *ASIC* designer a week to convert a single *PAL*, including quality control checks. Thus, by hand, the job would have been equivalent to some 40 man-weeks of engineering effort. Moreover, the logic synthesis process was efficient enough to replace 10-ns *PAL*s, keep the overall timing, and still minimize the gate count.

In this case, the *CUPL* logic equation (Figure 3a) was converted into the Trimeter form (Figure 3b). The implementation was then performed running the equations against the *TI* TSC500 Series standard-cell Knowledge Base. The converted logic was minimized for area, and the end-result was an automatically partitioned schematic.

In another design, a multiple *PAL* memory-management unit was converted into *ASIC* gates. The design supported multiple *TI* TMS320C25 *DSP* processors, each with local high-speed memory. Initially, the design had 11 *PAL*s, mainly 16R4s and some 16L8s. The design was converted into *ASIC* logic and took up only about 350 gates.

In this case, the full conversion took three days. Most of that time was used to convert the *PAL* equations into the Trimeter input form. Additional time was needed to create a schematic representing all the converted *PAL*s.

In a step-by-step process, each *PAL* was converted into equations and then synthesized. Next, the hierarchy of synthesized *PAL*s, now converted to gates, was flattened and synthesized again into an integrated minimal design. The last synthesis step served to optimize the total circuit, eliminating redundancies and taking advantage of any shared equation paths.

For simpler *PAL*s, the general conversion rule is that a single *PAL* takes about 50 gates to represent it in an *ASIC*. Thus, an 8,000-gate array can pinch-hit for up to 160 *PAL*s, a significant savings in real estate.

Helping to reduce this *PAL*-to-*ASIC* gate count, as well as minimize delay time, is the use of the complex gate functions in the *TI* Library. These complex functions can substitute for multiple gates, and provide special drive capabilities as well as minimize delay. For example, *TI*'s TSC500 Series library has 51 complex Boolean functions for the synthesis software to build an optimal implementation.

The potential savings with optimized gate choices can be seen with the *TI* BF0035 logic function—a 7-input *AND-OR-AND-NOR* gate with a worse case delay of 8.3 ns. It takes up real estate equivalent to 2.25 gates. Yet the same function, done in random logic, would require 8.5 gates with far greater delay (19.6 ns). Thus, when the BF0035 can map into a circuit, it can result in significant saving in both area and delay.

This circuit can be made up from plain gates or from a collection of subfunctions. The Logic Compiler has "rules" that will map such circuit occurrences into the BF0035 should conditions warrant it.

```
/** INPUTS **/
PIN 1  = LOGIC1E ;
PIN 2  = !GROUP5 ;
PIN 3  = LOGIC1G ;
PIN 4  = !GROUP6 ;
PIN 5  = I__INSTB__21 ;
PIN 6  = !GROUP10 ;
PIN 7  = I__INSTB__04 ;
PIN 8  = !GROUP11 ;
PIN 9  = I__INSTB__26 ;
PIN 11 = !GROUP12 ;
PIN 18 = LOGIC1M ;
PIN 17 = !GROUP16 ;
PIN 16 = LOGIC1L ;
PIN 15 = !EBKCK ;

/** OUTPUTS **/
PIN 19 = !FWI8__2 ;
  FWI8__2 = LOGIC1E & GROUP5
  LOGIC1G & GROUP6
  I__INSTB__21 & GROUP10
  I__INSTB__04 & GROUP11
  I__INSTB__26 & GROUP12
  LOGIC1M & GROUP16
  LOGIC1L & EBKCK ;
  END;
```

[A]

```
INPUT LOGIC1E , ZGROUP5 , LOGIC1G , ZGROUP6 ,
  I__INSTB__21 , ZGROUP10 , I__INSTB__04 , ZGR
  I__INSTB__26 , ZGROUP12 , LOGIC1M , ZGROUP16 ,
  LOGIC1L , ZEBKCK ;
OUTPUT ZFWI8__2 ;
GROUP5  = ~ZGROUP5 ;
GROUP6  = ~ZGROUP6 ;
GROUP10 = ~ZGROUP10 ;
GROUP11 = ~ZGROUP11 ;
GROUP12 = ~ZGROUP12 ;
GROUP16 = ~ZGROUP16 ;
EBKCK   = ~ZEBKCK ;

  FWI8 2 = LOGIC1E & GROUP5
   + LOGIC1G & GROUP6
   + I__INSTB__21 & GROUP10
   + I__INSTB__04 & GROUP11
   + I__INSTB__26 & GROUP12
   + LOGIC1M & GROUP16
   + LOGIC1L & EBKCK ;

ZFWI8__2 = ~FWI8__2 ;
```

[B]

Figure 3. Part (a) of this figure shows the PAL CUPL specification before it is converted to Trimeter format (b).

HIGHER LEVEL

Another advantage to a logic synthesis front end is that it gives the systems designer the ability to re-optimize at a higher level. Optimized design modules, or sections, can be re-optimized as they are joined to take advantage of common terms or redundancies. At each level of integration, design optimization can be ensured.

Moreover, the design constraints can be re-explored for further optimizations. Critical signal paths can be evaluated across major portions of the design, and re-done interactively.

This is an important aspect to the use of logic synthesis, because most of today's logic designs are not completely new designs. Instead, they are extensions of existing designs, or new products that try to make use of existing circuits.

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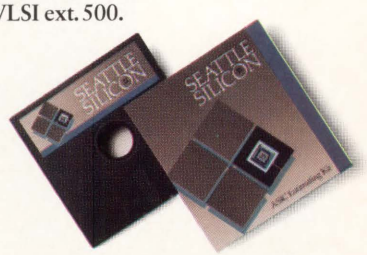

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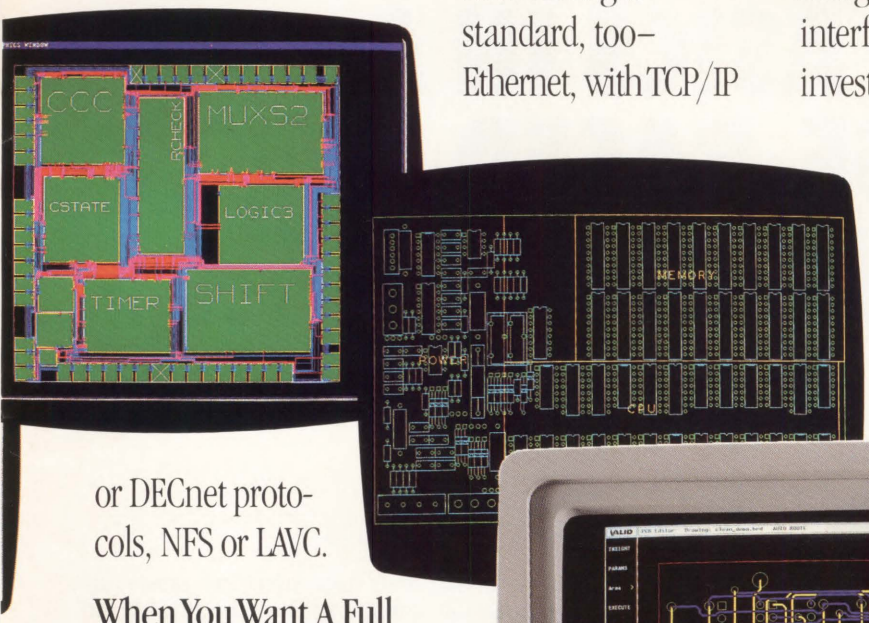

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VALID

CIRCLE NUMBER 4

DESIGNING ASICS IN A KNOWLEDGE-BASED ENVIRONMENT

Earl Reinkensmeyer, NCR Microelectronics, Fort Collins, Colo.

Now that acceptable first-pass success rates have been realized, other *ASIC* success issues need to be addressed. These issues include design optimization, cost-effectiveness, design creativity, productivity, quality, and reliability. The key element essential to meeting these additional criteria is increasing the amount of knowledge and expertise available to the designer. This goal can best be achieved by working in a knowledge-based engineering environment based on artificial intelligence (*AI*) concepts.

Knowledge comes in three forms: 1) rules-based knowledge that can be automatically (algorithmically) applied to complete sequential analytical tasks such as chip partitioning, timing analysis, *DRC*, and *ERC*; 2) embedded-function-based knowledge that is implicit in *ASIC* macrocell libraries and cell compilers; and 3) reasoning-based knowledge that is accumulated through years of design experience and knowledge "capture," and is inferentially applied. We will consider the application of each kind of knowledge to *ASIC* design, explore commercially available tools that utilize that knowledge, and provide illustrative design examples.

LOGIC SYNTHESIS

Rules-based knowledge and embedded-function-based knowledge can be combined to perform logic synthesis in the *ASIC* environment. Logic synthesis allows designers to input designs using a high-level design description language. It then applies expert knowledge to automatically generate the optimal logic implementation. This gives the designer unprecedented levels of design creativity while managing the cumbersome details necessary to ensure total specification-to-logic congruence.

Design synthesis tools free designers to take a more global and strategic approach to *ASIC* design. The heart of the design synthesis concept is the use of a high-level hardware description language (*HDL*) that allows the designer to take a more conceptual approach to *ASIC* design. The design synthesis tool then automatically handles implementation, ensuring that the final, optimized logic precisely matches the initial behavioral specification.

Early investigations in the use of high-level language descriptions were performed in universities and advanced development laboratories. In the late 1970s, Metalogic experimented with its Metasyn synthesis language, the first and perhaps only "pure" commercially available synthesis system generally considered to have been conceptually ahead of its time.

Following this early work came the development of the N. system-level design automation language from Endot Inc. (Cleveland, Ohio). Endot was recently acquired by Zycad Inc. (Minneapolis,' Minn). This language allows register-transfer-level specification and simulation. Several similar commercial offerings have appeared.

The U.S. government also supports work in this area, most notably with its *VHSIC* hardware description language (*VHDL*). *VHDL* lays the framework for defining, simulating, and documenting digital designs, particularly those originating in *DOD*'s *VHSIC* program. The government's primary thrust here is not to mandate how design occurs but rather how it is documented, to allow multiple sourcing, re-engineering, technology sharing, and maintenance.

COMPARING LOGIC SYNTHESIS TOOLS

With any of the new generation of logic synthesis tools, designers do not have to manually place and interconnect hundreds or even thousands of high-level schematic symbols. They are free to take a more conceptual approach to *ASIC* design. They can explore design alternatives at the architectural level, rather than have to generate the actual logic-level schematic symbols to see if their ideas are feasible.

Using logic synthesis, functional descriptions can take several hours and a couple of pages of data to generate rather than the many weeks and many pages of

data required for interconnecting schematic symbols. This doesn't count the schematic entry and verification that is also generally required for traditional *ASIC* design. This ability to enhance creativity early in the design process promises to have a significant impact on both chip- and system-level productivity.

A number of logic synthesis tools have recently been introduced. For example, the Genesil LogicCompiler from Silicon Compiler Systems (San Jose, Calif.) uses heuristic techniques. The techniques provide the user with the capability to configure combinational logic and optimize for either speed, gate count, or area by specification or circuit substitution. LogicCompiler can accept input from a netlist. It optimizes the design by automatically compiling the functionally optimized circuit into standard cells. These are not ordinary standard cells; they are fully parameterized, and they are tuned to maximum density for the specific fabrication process. Each cell is available in two basic configurations (minimum area or maximum drive), and each configuration has four performance-level choices. Using timing analysis, transistors can be individually sized along the critical path for further performance optimization. Automatic place and route algorithms then provide for maximum density by laying out the cells in horizontal rows and routing between them. The aspect ratio of the compiled cell can also be adjusted for best fit. These compiled parameterized cells can be combined with structured compiled functions within the Genesil design environment.

Synopsis Inc. (Mountain View, Calif.) recently added an *HDL* compiler to its Design Compiler logic synthesis system. This system uses the Verilog language from Gateway Design Automation (Westford, Mass.) to input hardware descriptions, or utilize netlist, equation, *PLA*, or truth table inputs. It is expected, however, that Synopsis will support additional *HDLs*. Circuits may be combinational or sequential, and may be specified in a hierarchical structure; the Design Compiler translates them automatically into gate-level circuit descriptions that are optimized for a particular vendor's library. The optimization process is controlled by the user through a design constraint control file (e.g. clock rate, maximum area, set-up time, hold time, loading, process, temperature, and voltage) that enables the user to trade-off circuit speed for area. Keep-out areas can be specified so that Design Compiler does not attempt to further optimize user-selected portions of the design. Synopsis embeds the transformation rules within the tool.

The Logic Synthesizer from *VLSI* Technology Inc. (San Jose, Calif.) provides output in a form that can be implemented as an optimized programmable logic array (*PLA*) structure within an *ASIC*, as well as in a netlist form for implementation as either a gate array or cell-based device. The Logic Synthesizer also offers automatic state assignment and optimization. Those two features can produce greater silicon efficiency and improved performance by making state assignments based on logic adjacency, reducing the time required to optimize and minimize the size of the logic produced. Logic Synthesizer automatically generates high-fault-coverage test vectors for the logic generated. It lets engineers specify *IC* designs in a high-level state transition language that includes Boolean equations as input.

The Logic Consultant from Trimeter Technology Corp. (Pittsburgh, Pa.) uses both algorithmic and expert system technology for logic design optimization of gate arrays and standard cells. Logic Consultant first performs two-level and multilevel logic minimization on an input design, then considers a variety of alternative cell and macrocell selections and combinations for more efficient logic design implementation. After selecting the optimal combination of cells and macrocells that meet the design's timing and area requirements, the tool generates an output schematic for viewing and editing on the existing *CAE* system. Logic Consultant accepts five types of inputs: an initial logic schematic expressed in specific library component symbols, simulated to verify functional correctness; a set of Boolean equations representing combinational logic specifications; a verified logic schematic expressed in generic primitives; and a logic schematic implemented in *TTL* components.

FLEXIBLE SYNTHESIS TOOL

NCR's Design Synthesis tool is based on technology developed by Silc Technologies Inc. (Burlington, Mass.). Silc's system, called SilcSyn, is not limited to any particular design type or style, which makes it very flexible for an *ASIC* environment. It supports combinational and sequential logic as well as synchronous and asynchronous design requirements. When integrated with an *ASIC* library and design tools, it gives the engineer design flexibility while significantly increasing productivity.

With Design Synthesis, once the micro-architectural description has been completed using the high-level language, it is then simulated at the conceptual level until the designer is satisfied with the design's functionality. The iteration loop at this point is very tight: the designer simply changes the description and resimulates. This is considerably more efficient than the conventional schematic capture, netlist extraction, logic simulation, and edit schematic loop.

When the designer is satisfied with design functionality, the description is automatically synthesized into structural resources such as registers, adders, and multiplexers. *NCR*'s Design Synthesis automatically minimizes these resources algorithmically (using mathematical procedures) and heuristically (using "rules of thumb") to help achieve an efficient implementation. At this point, the design is both library- and technology-independent.

After the design has been synthesized and minimized into generic, technology-independent logic elements, it must be mapped into a specific library that has been built in the specific technology of the *ASIC* vendor. In Design Synthesis, this "builder" incorporates knowledge-based rules entered by *NCR* to guide it in optimizing the mapping for several *NCR* libraries and technologies, including the 2.0- and 1.5-micron *CMOS* cell libraries. Some of these "good design practice" rules were taken from *NCR*'s Design Advisor. Another round of minimization is included in the mapping process, including replacement of certain logic configurations with more

complex cells to improve speed and density.

NCR's builder also allows the designer to guide the synthesis and mapping task by specifying maximum logic depths for all or part of the design. Other rules incorporated into *NCR*'s builder minimize delays, and balance the loading of critical signals by name or by type. The designer can also specify various special input and output pad configurations required for their design by name or by type.

After the design has been implemented in a given library, schematic creation files are automatically generated to interface with standard schematic capture tools. The interface partitions the schematic based on the design architecture, schematic sheet size, and density requirements specified by the user.

```
THIS FIFO CONTROLLER PERFORMS THE FOLLOWING
FUNCTION:

WHEN FIFO-REQUEST (F__REQ) IS ASSERTED, DATA IS READ
FROM THE FIFO IF THE FIFO IS NOT EMPTY. THE READ RE-
SPONSE IS TO SET FIFO-READ (F__READ) AND PULSE DATA-
STROBE (D__STROBE). WHEN THE FIFO IS EMPTY THE FIFO-
EMPTY (F__EMPTY) SIGNAL IS SET.

WHENEVER THE FIFO IS NOT FULL AND DATA-AVAILABLE
(D__AVAIL) IS SET THE READING OF 10 ADDRESS LOCA-
TIONS WITH A COMPANION PULSE ON FIFO-WRITE
(F__WRITE).

CONDITIONING ON PHASE, ALLOWING FOR SET-UP, ETC.
COULD BE HANDLED WITH PHASE VALID OUTPUT ASSER-
TIONS, DELAYING THE PULSE OCCURANCES, ETC. SINCE
THIS WAS A FICTITIOUS SPEC, THOSE DETAILS WERE NOT
ADDRESSED.
```

Figure 1. A plain-English description of a FIFO controller.

SYNTHESIZING A FIFO CONTROLLER

To illustrate the logic synthesis process, a *FIFO* controller example is presented in Figure 1 where a plain-English description is given. This is followed by its functional description in high-level hardware description language (Figure 2). Finally, a synthesized schematic representation is made. First the design is partitioned into functional blocks; for example, write-loop, input, reset, read-loop, and output. Second, the logic synthesizer then automatically generates a schematic-level implementation of each of the functional blocks.

NCR's Design Synthesis can be used to create major blocks of a design. The blocks can then be combined with other functions including analog, high-level functions such as core microprocessors, or compiled functions such as memory, using traditional schematic capture. Blocks designed using synthesis can be combined with other functions and simulated as an entire chip or system to ensure compliance with functional specifications.

```
;;;
;;; FIFO__CONTROL.DESIGN
;;; COPYRIGHT 1988 NCR CORPORATION
;;;
(CHIP FIFO CONTROL


    (DECLARE ;;; INPUT, OUTPUT PADS, VARIABLES
        ($SET BIT__LEN 16)
        (WORD-LENGTH $BIT__LEN)
        ($SET BIT__DOUBLE ($TIMES $BIT__LEN 2))
        (PAD *F__EMPTY* (INPUT F__EMPTY FLOW-
          THROUGH))
      (PAD *F__FULL* (INPUT F__FULL FLOW-THROUGH))
        (PAD *D__VALID* (INPUT D__VALID RESET-BY RST))
        (PAD *CLOCK* (INPUT CLK-IN NOT-CLOCKED))
        (CLOCK CLK INTERNAL-DATA-AVAILABLE RISING-
          EDGE SOURCE CLK-IN CHIP-DEFAULT)
        (PAD *RST* (INPUT RST-IN NOT-CLOCKED))
        (RESET RST FLOW-THROUGH SOURCE RST-IN)
        (PAD *RD__SEL* WORD-LENGTH 4 (OUTPUT
          RD__SEL STORED RESET-BY RST))
        (PAD *D__AVAIL* (OUTPUT D__AVAIL STORED
          RESET-BY RST))
        (PAD *D__STROBE* (OUTPUT D__STROBE
          UNSTORED))
        (PAD *F__READ* (OUTPUT F__READ UNSTORED))
      (PAD *F__WRITE* (OUTPUT F__WRITE UNSTORED))
      (PAD *F__REQ* (INPUT F__REQ FLOW-THROUGH))
  );;; END OF GLOBAL DECLARATION


;;; DCM READ LOOP
;;; F__REQUEST CAUSES F__READ/DATA STROBE PULSE
;;; UNLESS FIFO IS EMPTY, THEN IT WAITS UNTIL NOT
;;; EMPTY AND REQUEST ACTIVE.
;;; WHEN FIFO GOES EMPTY, CLEAR DATA AVAILABLE
      (DCM READ__LOOP
        (DECLARE (RESET-BY RST))
        (PAR
            (IF (AND (NOT F__EMPTY) F__REQ)
            (PAR (SET F__READ 1)
            (SET D__STROBE 1)))
          (IF F__EMPTY (SET D__AVAIL 0)))
        (SET D__STROBE 0)
      );;;END OF DCM READ__LOOP


;;; DCM WRITE LOOP
;;; WHEN DATA__VALID GOES HIGH, WRITE SEQUENCE
;;; OF 10 BYTES TO FIFO UNLESS FIFO FULL
;;; WHEN COMPLETE, SET D__AVAIL HIGH
      (DCM WRITE__LOOP
          (DECLARE (RESET-BY RST))
              ($LOOP
                FOR ADDRESS
                FROM 0 TO 9 BY 1
                DO
              (WHILE (OR F__FULL (NOT D__VALID))
                (WAIT))
                    (PAR
                (SET RD__SEL $ADDRESS)
                (SET F__WRITE 1))
              (SET F__WRITE 0)
          )
          (SET D__AVAIL 1)
      ) ;;END OF DCM WRITE__LOOP
) ;;; END OF CHIP
```

Figure 2. A functional description—in a high-level hardware description language—for the FIFO controller.

BENEFITS OF LOGIC SYNTHESIS

Ultimately, the biggest benefit of logic synthesis is the separation of conceptual design from actual structural implementation. This separation helps protect the design investment and provide migration to new or alternate implementations.

The logic synthesis concept also promotes reuse of design blocks within multiple designs and technologies. Customers can design proprietary macro functions or "standard part" equivalents not available from an *ASIC* vendor.

Training and experience will help users become even more comfortable with logic synthesis as they gain an understanding of the physical implications of a particular high-level language description. With this comfort will come quantifiable increases in design productivity, a higher percentage of first-pass success rates, and significantly reduced *ASIC* time-to-market schedules, along with intangible benefits of unprecedented levels of creative design freedom.

APPLYING REASONING-BASED KNOWLEDGE

We have seen how rule-based knowledge and embedded-function-based knowledge can be combined to perform logic synthesis in the *ASIC* environment. We will now consider how reasoning-based knowledge, accumulated through years of design experience and knowledge capture, is inferentially applied to provide design advice.

In discussing *ASIC* design success, reference is often made to "first pass success." Many *CAE/CAD* tool suites provided by semicustom *IC* vendors provide very high first-pass success rates "as designed." This means that the tools themselves accurately predict device function and performance, and rarely introduce errors. There is, however, still opportunity for the design engineer to introduce errors through misinterpretation, or misuse of the tools and their reports. It is also possible to have marginal areas in the design that the designer's *CAE/CAD* tool methodology does not detect, or for the engineer to use design practices that increase the likelihood of problems. Design advice tools address such pitfalls so that first-pass success is redefined as an *ASIC* that works as intended in the target system. This bottom line criterion is the key to the ultimate successful application of semicustom *IC* technology.

There are relatively few design advice tools on the market today, so it is difficult to make generalizations about their capabilities. However, in general, they automate design review, offer new opportunities to improve designs, and help solve problems that other *CAD* tools are not designed to detect.

Some design advice/optimization tools provide a framework for developing a design advice database, while others actually provide the knowledge-base itself. For example, Knowledge Consultant from Trimeter Technology Corp. (Pittsburgh, Pa.) takes the first approach, allowing you to incorporate your own design expertise into a knowledge base used by Trimeter's Logic Consultant for logic design optimization. To build or enhance an *ASIC* logic-design knowledge-base, Knowledge Consultant is used to draw an "antecedent circuit." This is a pattern of cells and macrocells that commonly appear in logic designs for the chip, using foundry-specific library component symbols. The designer then draws a "consequent circuit," a less obvious but faster or denser implementation of the antecedent circuit. Knowledge Consultant is then used to define any additional selection criteria that aid in determining the applicability of substituting the consequent circuit for the antecedent circuit. While Knowledge Consultant swaps cells based upon "captured knowledge," and therefore improves even pre-existing designs, it does not reason inferentially.

VLSI Technology Inc.'s Technology Design Assistant addresses the partitioning of logic and functions among *ASIC* chips. It applies algorithmic rules for optimum partitioning for power consumption, and aids the user in selecting between compiled cell, standard cell, or gate array methodologies. Information on packaging alternatives is provided. The design advice is based upon algorithmic calculation, not inferencing.

NCR's Design Advisor provides a comprehensive knowledge base together with inferencing capability. It combines an artificial-intelligence inference engine with knowledge derived from extensive *NCR* design experience and textbook knowledge. The resulting tool can be used by both junior-level and sophisticated circuit designers to optimize designs, avoid costly errors, simplify the design process, and broaden the designer's own knowledge. In many cases it may contribute to a saving of weeks or months in the design cycle.

The *NCR* Design Advisor can be used to perform regular automated design reviews, and can provide expert design advice at any point in the design process. The automation provided by the system also assists in managing the large number of details in creating highly complex designs, ensures all accepted design advice is applied consistently throughout the design, and allows "what-if" scenarios to be pursued and analyzed. Input to the system consists of a circuit description, which can be accessed at any point when an important portion of a design has been completed. This allows the designer to partition the design and apply the Design Advisor to either specific modules or the entire design.

Unlike traditional *CAD* tools that apply algorithmic solutions to numeric data, the Design Advisor behaves more like a human expert, performing heuristic processing on symbolic information. The system combines a database of design knowledge with an underlying multiparadigm reasoning system that allows it to analyze and recommend action related to generally accepted logic design principles, testability, timing analysis, cost effectiveness, and buffering and system interface requirements.

The inference engine used in the Design Advisor is based on the *PROTEUS* hybrid expert-system development tool created by the Microelectronics and Computer Technology Corp. (*MCC*) of Austin, Texas, a private-sector cooperative research venture of which *NCR* is a member.

PROTEUS employs a logic-based truth maintenance system combined with a sophisticated framework for knowledge representation. This results in a powerful inference engine, on top of which *NCR* has built an extensive knowledge base. The knowledge base is derived from the collective human experience of circuit designers at both *NCR* and some of the company's customers. The *NCR* Design Advisor is the first commercial application of the *MCC PROTEUS* technology.

The Design Advisor knowledge base currently encompasses the domains of chip timing, synchronicity, testability, performance and *I/O*, in addition to other areas of overall design quality and manufacturability. A hierarchy of design attributes serves as a framework for the system's recommendations. It was compiled by analyzing typical mistakes that had caused unsatisfactory silicon prototypes in designs done by both junior and expert designers over the past several years. Additionally, *NCR* has incorporated knowledge related to the actual thought process of typical design engineers, as learned from a lengthy interview process. Each participant was asked to think aloud so that the logic train and approach could be recorded. From this information rules were formulated and critiqued by experts.

Based on *NCR* studies, almost two-thirds of the design problems generally found at the prototype stage will be detected by Design Advisor while they can still be easily remedied. As much as 70 percent of all timing-related problems were detected in the studies, and this often subtle area accounted for the majority of the observed problems missed by design engineers.

Design Advisor analyzes the design within the context of the knowledge base. When it identifies an error or the opportunity for a more optimal design implementation, it provides an error message and general guidelines for solving the problem. Also, unlike standard design rule checkers that simply flag errors, it features an explanation utility that shows the train of logic and the design occurrences that led to the suggestion. This allows the designer to learn from his errors and reduces the likelihood of repetition.

Design Advisor also checks the design for compliance with fundamental, successful design techniques, including rules for maintaining synchronous circuitry, and warns against hazardous timing practices. Additionally, suggestions for simple ways to minimize die size help the designer keep costs in line for when the product is in high-volume production.

CONTRADICTING AND OPPOSING ADVICE

The designer may not agree with the advice given. Advice delivered by Design Advisor can be rebutted in two ways. It can either be "contradicted" or "opposed."

The advice might be contradicted by the user because he does not agree with the reasoning that led to the advice that was delivered. The capability to contradict the system enables the designer to reason with the system regarding possible new information that may not have been initially available to the system. The system will reason with the designer—to the extent of the depth of knowledge relating to the rule that the system has tried to impose. The additional data, or knowledge, given by the designer during this dialog usually resolves the contradiction and adjusts the state of the knowledge base for that session. In the event that the designer himself has knowledge that the system does not have, and he is unable to resolve the contradiction logically by opposing the system, then the advice may simply be opposed by the user. Under this condition, the system accepts that the question has been resolved by information that was not explicitly available.

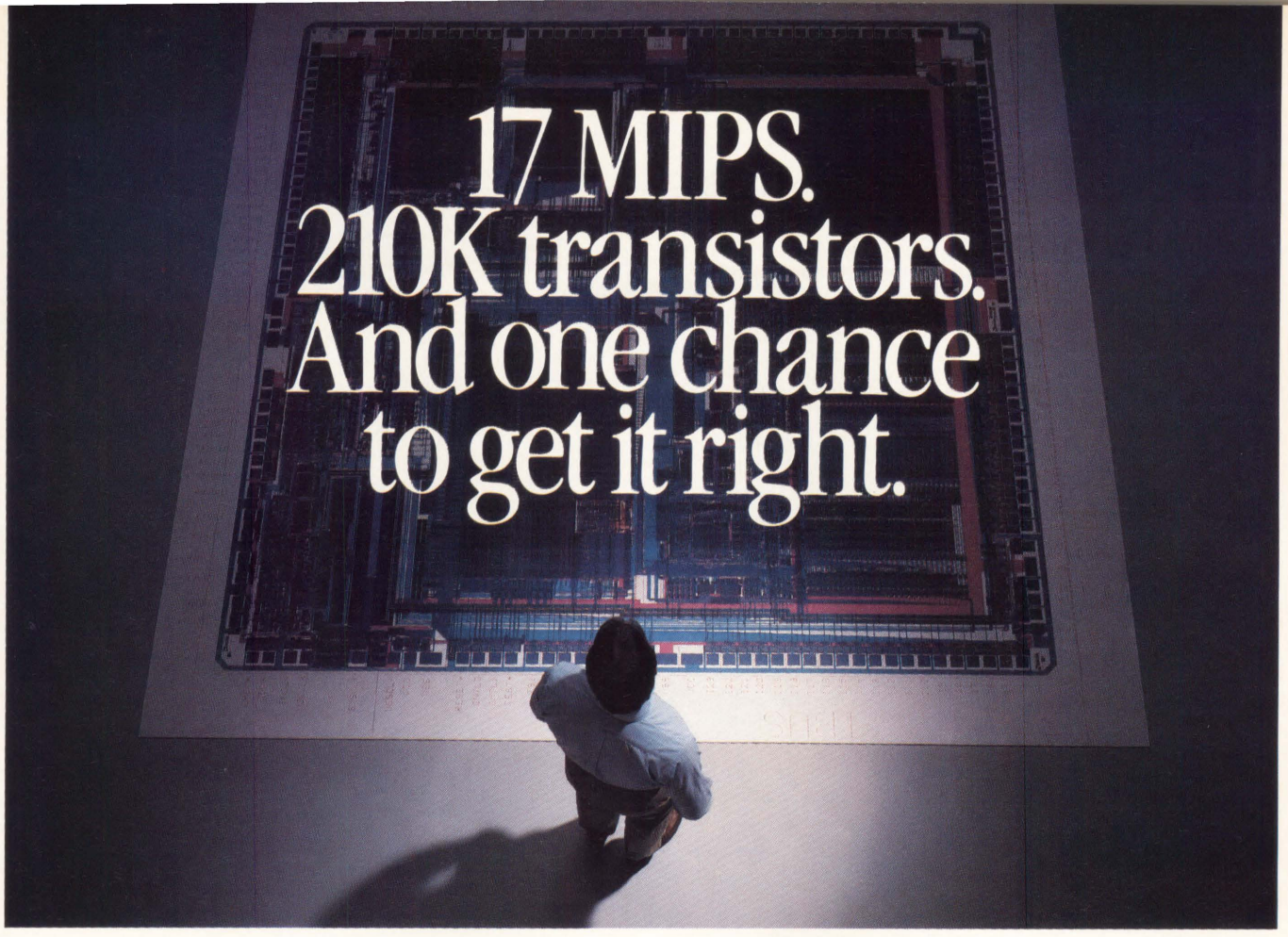
The system prompts the user to document reasons for opposing or contradicting the advice. The designer is expected to provide an explanation for his reasoning. This serves as valuable documentation to other designers using the system on the same design. Records of contradicted and opposed advice may also be brought to the attention of the expert team members who conduct the final design review. This offers two potential benefits. It will help the team to understand what problems were handled by the designer. It will also bring to the committee's attention advice that was delivered inappropriately by the system, or areas of the system's knowledge base, that can be effectively extended by applying this designer's method of dealing with the problem.

TESTING AND UPDATING THE KNOWLEDGE BASE

A tool that gives advice is no better than the rules it attempts to enforce. Its knowledge base must be tested and updated. Presently, the testing methodology for rules within an expert system is the subject of considerable research in artificial intelligence. Clear methodologies have not been established that are applicable to all cases. The testing activities for Design Advisor include some similarities to the testing that goes on for much conventional software. Namely, the system is run on cases designed so that every rule within the system will "fire," i.e. every element of knowledge will become active. Additional examples are generated to verify the proper interaction of one element of knowledge with another.

Who should update the knowledge base? Machine learning in artificial intelligence is another area of active, ongoing basic research. However, many of the problems involved with commercially fielding such systems have not been addressed. The Design Advisor learns through a controlled growth of the knowledge base in the hands of the developers at *NCR*. This assures that the knowledge is verified and relevant, and maintains consistency across all installations of the tool. The growth of the knowledge base does include information derived from customer experience.

Knowledge-based tools have finally arrived. They are available across a wide range of functions, from front-end to back-end, from circuit partitioning, to logic synthesis, to design advisement. Provided by a growing number of suppliers they will continue to impact *ASIC* design by improving engineering productivity, shortening time-to-market schedules, and lowering costs. They will free the engineer from drudgery to do what he does best: design creatively.



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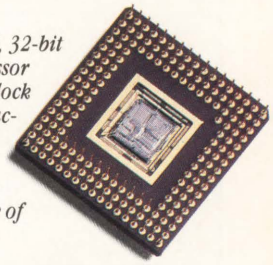

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CADAM Inc. 1935 N. Buena Vista St. Burbank, Calif. 91504 Alan Cohen Marketing Manager for CADAM Electrical Products (818) 841-9470	**Interactive Design System** $65k—$170k, software only IBM 4331 and up (VM/CMS, MVS, or VS1) **Micro CADAM** $8k, software only **Micro CADAM Cornerstone** $2995 software only PC AT (MS-DOS)	None	CADEX	None	2000 SSI/MSI TTL and ECL; 700 memory parts; 8000 schematic and PCB design symbols
Cadence Design Systems Inc. 555 River Oaks Pkwy. San Jose, Calif. 95134 L. Siegel Manager, Public Relations (408) 943-1234	**CAE/CAT Tools** $13k, software only Apollo, Sun, DEC, UNIX, Ethernet, TCP/IP	None	Schematic capture	None	Standard logic gates for IC design
CAD Group Inc. 3911 Portola Dr. Santa Cruz, Calif. 95062 Gena Haas Marketing Communications Manager (408) 475-5800	**SALT** Software only: $3.5k, all DOS operating systems; $15k workstations; $40k–$60k, mainframes; $80k–120k, supermini and supercomputers PC/XT, AT (DOS); MicroVAX to VAX 8800 (VMS, UNIX); Cyber and Cray (NOS, COS, UNICOS, CTSS); Sun (UNIX); Apollo (AEGIS, DOMAIN IX)	IBM AT accelerator package includes both hardware and software 5-MIPs performance	Interfaces to Scientific Calculations; Case Technology; OrCAD; CAECO	SALT Hardware Description Language (SHDL, an enhanced register-transfer language)	1500 SSI/MSI TTL and ECL; 72 LSI and VLSI; 100+ generic behavioral models
Cadnetix Corp. 5757 Central Ave. Boulder, Colo. 80302 Steve Sherwood Marketing Communications Manager (303) 444-8075	**CDX-3000 PC schematic entry system** $4950 PC ATs and compatibles (standard DOS, Ethernet, PC NFS), optical mouse **CDX-95xx and CDX-96xx Capture and Management Workstations** $14.9k Sun 3/50 and 3/60 (UNIX, Ethernet TCP/IP, NFS) **CDX-95xx and CDX-96xx Digital and/or Analog Design Workstations** $32.9k Sun 3/50 and 3/60 (UNIX, Ethernet TCP/IP, NFS) **CDX-81xx Design Capture and Management, Digital Design, Analog Design Environments** $10.8k	CATS dynamic hardware modeler (network resource for simulation and physical modeling)	Hierarchical schematic capture	CADAT behavioral description language (BDL)	2000 SSI/MSI TTL and ECL; 100 PLDs; 400 miscellaneous (primitives, CMOS); 1000 analog device models; hardware models: ASIC, ECL, TTL, CMOS, advanced functions

N/s = Not Supplied By Vendor N/a = Not Available

Design analysis		Design transfer		Additional capabilities	
Simulators and capabilities	**Timing analysis**	**Netlist outputs**	**Test vector outputs**	**IC/PCB layout**	**Other tools, comments**
Susie simulator $995	Susie/Tim simulator $2490 Timing to 101 ns	ASCII, Tango, P-CAD, Calay, Racal, Applicon	N/s	Tango-PCB ($595) Tango Route ($495)	N/s
Max+Plus Interactive Functional Simulator; Waveform Entry for specification of simulation VECTORS; Virtual Logic Analyzer to specify breakpoints and display output waveforms	Critical Path delay predictor	Altera design format	None	None	Design tools for MicroChannel interface; translation and optimization of designs with knowledge-based processing engine.
SimuKit Simulator integration kit for access to user's own in-house simulators **SPICE 2G.6** **SPICE PLUS** (enhanced SPICE 3) Circuit simulation, including time- and frequency-domain analysis **SABER Behavioral Simulator** **mwSPICE Microwave Simulator**	None	ASCII format	Not applicable	None	Parameter entry with subcircuits and a symbol editor; function generator and oscilloscope; frequency sweeper and network analyzer; dc meter; spectrum analyzer; statistical analysis; parametric plotting; power design module; stress analysis; IC design, power design, circuit design, and test development tool kits.
PSPICE (MicroSim) Circuit simulator	None	GDSII; SCICARDS; TEGAS; SILOS; ILOGS; LOGIS; SPICE	Not applicable	ICD-ONE, RGRAPH, and CRITERION II IC and PCB layout tools	None
CADAM CADAT (enhanced CADAT) Switch-level, gate, fault, and behavioral simulator **CATS** (HHB Systems) Physical model simulation	None	CADAM; CADAT	None	Interactive Prance Cadam PCB layout	PCB thermal analysis; IPC350B output; 3D and solid model interface
SILOS and HILO Logic and fault simulator **SAGE** Circuit simulator **SCOAP** Testability analyzer **SPICE and HSPICE** Circuit simulator interface Verilog netlist capability	Timing analysis (Cadence)	EDIF	Sentry; GenRad; Advantest	IC layout design, automatic IC layout, IC floorplanning; design verification (DRC, ERC, LVS)	Module compilation; generalized simulation/test language; electrical rule checking; open simulation system
SALT Switch, gate/functional, and behavioral simulator; concurrent timing verification/analysis; analog/digital mixed mode **SHDL** Behavioral model simulator	In SALT; dynamic timing analysis	SALT; SCICARDS; standard ASCII format	Sentry	None	Critical path analysis; transfers from other simulators to SALT; custom models; many interactive features
CADAT Logic, switch-level, worst-case, behavioral, and fault simulator **SABER** Analog circuit simulation	CADAT: nominal and worst-case simulation incorporating set-up hold, pulse width, spike and race condition analysis	SPICE; CADAT; TEGAS; SCICARDS; EDIF 2.0; Verilog	Zehntel; GenRad; Factron; Marconi; HP	CDX-56000SP PCB layout stations; CDX-75000XP Route Engine III	User has access to all network resources

Directory of CAE Systems (continued)

Vendor Contact	System overview		Design entry		
	Product name, cost, and host	Applications hardware	Schematics	HDLs	Standard libraries
Control Data Corp. 8100 34 Ave. S. PO Box 0 Minneapolis, Minn. 55440 R.L. Biggs Marketing Manager (612) 853-5255	**MIDAS** $600k+, turnkey; $75k+, software only CDC Cyber 180 (NOS, NOS/VE, HASP, X.25, Kermit)	Interface to Zycad logic and fault accelerators	Daisy; Mentor	N.2	Gate array families and standard glue logic
	Electronics Designer $6k, software only PC/XT or AT with Hercules or EGA graphics boards; VAX; IBM; Cyber 800 or Cyber 205; any LAN	None	Electronics Designer (Case Technology)	VERILOG	2000 MIL-SPEC-1000 parts, (including TTL, CMOS, ECL, and microprocessors)
Daisy Systems Corp. 700 Middlefield Rd. PO Box 7006 Mountain View, Calif. 94039 Rich Dickerson Director of Corporate Communications (415) 960-6674	**Advansys Series** $24k–$89k Sun 386i; UNIX; NFS; Ethernet; TCP/IP; X Window System	MegaLOGICIAN, Personal MegaLOGICIAN, GigaLOGICIAN simulation accelerators; PMX (Physical Modeling Extension)	ACE	Daisy Behavioral Language (DABL)	4400 digital components: TTL, CMOS, ECL, memory, PLD, microprocessor; Mil-Spec library; 175 vendor-supplied ASIC libraries, 1215 analog devices
Data I/O Corp. FutureNet Division 10525 Willows Rd. NE Redmond, Wash. 98052 Michael Radovich Public Relations Manager Data I/O Corp. (206) 881-6444	**FutureNet FutureDesigner** $7.9k Mixed-mode design entry and logic synthesis: Sun; PC AT, PS/2 **FutureNet DASH Schematic Designer** $3850 Schematic capture: Sun; PC AT, PS/2 **ABEL** $1745 PLD design tool: Sun, PC, PS/2, VAX (VMS and UNIX), Apollo	Interfaces to CATS hardware modeler (HHB Systems), Zycad/SSC accelerators	DASH; schematic translators for Analog Design Tools, Computervision, Mentor, CBDS	ABEL/Gates	2300+ symbols, including TTL, ECL, CMOS, Intel, Motorola, discrete; libraries for 40+ ASIC vendors also are available
Electronics Software Products 18013 Sky Park Circle Irvine, Calif. 92714 Behrooz Shariati Western Technical Manager (714) 261-1777	**USPICE; PC-USPICE** **CADAT** **LOGNET** Software only; contact company for costs VAX (VMS, UNIX); IBM (MVS); Sun (UNIX); Apollo (AEGIS)	None	LOGNET (VLSI Automation)	None	7400/5400 TTL; MECL; 10K
EPIC Design Technology Inc. 2900 Lakeside Dr. Suite 205 Santa Clara, Calif. 95050 David Squires Director of Technical Marketing (408) 988-2944	**TIMEMILL** $5k–$20k, software only Sun; Apollo (UNIX); MicroVAX and VAX 8600 (Ultrix, VMS); Valid SCALDStar; PC-386; HP workstation **PATHMILL** $4k–$15k, software only Sun; Apollo (UNIX); MicroVAX and VAX 8600 (Ultrix, VMS); Valid SCALDStar; PC-386; HP workstation **VERIMILL** $30k, software only Sun; Apollo (UNIX)	None	GED (Valid Logic Systems) ECS (CAD/CAM Group) CapFast (Phase Three Logic); NETED (Mentor); netlist interfaces to HSPICE, SILOS, VERILOG, TEGAS, HILO	C and TIMEMILL HDL (a superset of C)	7400 HCMOS, ALS, AS, FAST; LSI Logic 7k: 100; Raytheon ECL: 100; generic RAM, ROM, PLA

N/s = Not Supplied By Vendor N/a = Not Available

Design analysis		Design transfer		Additional capabilities	
Simulators and capabilities	**Timing analysis**	**Netlist outputs**	**Test vector outputs**	**IC/PCB layout**	**Other tools, comments**
ASSIST Logic and behavioral simulator (including timing) **BEV** (Boolean evaluator) Zero-delay logic and behavioral simulator **AFS** (automatic fault simulator) Fault simulation and test vector gen. **STAFAN** (Statistical Fault Analysis) Probabilistic fault detection	PATH-TRACE	SYSCAP II.5; SPICE 2G6	Neutral format with post-processors for Sentry, Teradyne, Takeda-Raiken, and GenRad	LLS semicustom IC layout	Model generation; testability metric; routability metric; integrated database with configuration management; testability analysis tools supporting built-in test
SALT (CAD Group) Switch- and gate-level simulator, dynamic timing analysis **VERILOG** (Gateway Design Automation) Behavioral simulator **ASPEC** Circuit simulator **PREDICTOR** (MSI) Reliability analysis (MIL-SPEC-217)	SCALD (with Case)	Netlist and drawing transfer to Mentor, and Prime Computervision	Fairchild Sentry; GenRad; others	PCB layout editor with links to host-based Vectron for automatic placement and routing	Job creation language ("JCL") generators; auto-dial and log-in; and auto-submit to network (Cyber 205, Cray); all analysis tools also on in-house host
DSPICE (based on Berkeley SPICE) Circuit simulator **Daisy Logic Simulator (DLS)** Switch/gate/functional/physical modeling all integrated in one logic simulator MDLS (accelerated version of DLS) **Megafault (concurrent)** Fault simulation accelerator **A/D Lab** Analog-digital design environment	Daisy Timing Verifier (DTV)	TEGAS (Calma)	Sentry Series 7; Factron 800 series; GenRad GR160, GR180	Chipmaster full custom editor; Gatemaster automatic gate array placement and routing; Boardmaster PCB layout	PLDMaster with ABEL or LOG/IC compilers for PLD design and simulation; FrameMaker technical documentation software
Interface to: SPICE, CADAT, Analog Design Tools, TEGAS	None	ABEL; Applicon; CADAM; Computer-vision; EDIF; Racal-Redac; SCICARDS; SPICE; TEGAS; Xilinx; over 50 others	Sentry; GenRad; IMS; Tektronix; over 10 others; PLDtest automatic test vectors for PLDs	Interfaces to CADAM, CBDS Applicon, Computervision, REDAC, Xilinx	PLDtest (automatic test-vector generation)
USPICE, PC-USPICE Circuit Simulator **CADAT** (HHB Systems) Logic simulator, fault simulator, behavioral simulator, timing, worst-case	None	None	Sentry; GenRad	Edge IC graphics layout (NCA)	Wirewrap support
TIMEMILL Mixed level simulator - switch (including layout extracted capacitance), gate, and functional	TIMEMILL: dynamic timing verifier for set-up, hold, edge-to-edge and pulse width verification; PATHMILL: mixed level critical path analyzer - switch (including layout extracted capacitance), gate, and functional; VERIMILL: static timing verifier, allows multiple clock cycles, cycle sharing and min-max analysis	N/s	Sentry	None	Netlist-compatible across all tools

Directory of CAE Systems (continued)

Vendor Contact	System overview		Design entry		
	Product name, cost, and host	Applications hardware	Schematics	HDLs	Standard libraries
Gateway Design Automation Corp. 2 Lowell Research Center Dr. Lowell, Mass. 01852 Pete Johnson Marketing Manager (508) 458-1900	**VERILOG** $25k **VERILOG-XL** $35k **VERIFAULT-XL** $35k Software only VAX and MicroVAX (VMS); IBM (VM/CMS); Sun (UNIX); Apollo (AEGIS, UNIX); MIPS (UNIX)	None	Netlist interfaces to Daisy; Mentor; TDL; Valid; NDL; others supported by schematic vendor	VERILOG C-based behavioral language; VHDL	7400/5400 TTL; various ASIC libraries
Harris Semiconductor Custom IC Division P.O. Box 883 Melbourne, Fla. 32901 John Reeser Manager, Business Development (407) 729-5390	**HARRIS ARCHITECT** CMOS Digital Design Package Bipolar Analog Design Package CMOS Analog Design Package Cadence Design Framework Sun now, other UNIX workstations planned; software only or turnkey	Interface to CADAT accelerator	EDIF netlist, Daisy and Mentor interface schematics	CADAT BDL; VHDL being developed	HSC1000 library; HSC1000RH Rad Hard Library; 200 primitive and macrocell functions, RAM and ROM module compilers
GenRad Inc. Design Automation Products 510 Cottonwood Dr. Milpitas, Calif. 95035 Peter Denyer Marketing Manager (408) 432-1000	**System HILO Logic Simulation Toolkit** Software from approximately $15k upwards depending on platform Computers supported include: VAX (VMS, Ultrix, or BSD 4.2); Sun (UNIX); Apollo (Aegis); HP-9000 (Unix); InterPro (UNIX); IBM - CMS (mainframe), AUX (RT-PC); Harris (UNIX); Cray (UNICOS)	HICHIP (Physical device modeling system); Interface to ZyCAD accelerators (via ZyCAD)	Interfaces available from most schematic capture systems including Cadence, Case Technology, Computervision, Daisy, FutureNet, Hewlett-Packard, IBM, Intergraph, Mentor, P-CAD, Phase Three Logic, Racal-Redac, Silvar Lisco, Valid Logic, Viewlogic	GHDL (GenRad hardware description language)	Over 5000 TTL, ECL, CMOS, and VLSI components; over 20 semicustom libraries from various manufacturers; HIGEN ASIC library modeling tool; HI-LIB - PLD (PLD model characterization tool)
Hewlett-Packard Co. 19310 Pruneridge Ave. Building 49AV Cupertino, Calif. 95014 Customer Information Center (800) 752-0900	**HP Electronic Design System** Design capture, $8200–$17,850 (hw + sw) Design verification, $15k–$41k (hw + sw) HP 9000 series 300 workstations (HP-UX) and networking services	Interface to HI-CHIP hardware modeling system (GenRad)	Design Capture System (HP's Salt Lake City Operation)	Functional Modeling Language (FML—GenRad) and harware description language (HDL for HICHIP)	›3000 digital parts: TTL, MOS, ECL, microprocessors, PLDs; 3500 analog symbols
HHB Systems 1000 Wyckoff Ave. Mahwah, N.J. 07430 Todd Westerhoff Marketing Manager (201) 848-8000	**CADAT** $3k–$100k+, software only VAX (UNIX, VMS); Sun (UNIX, NFS); Apollo (DOMAIN IX); IBM (MVS, DOS); Masscomp (UNIX); HP9000/series 300 (UNIX); Ethernet TCP/IP **INTELLIGEN automated test generation** Up to $190k, software only Sun (UNIX, NFS); VAX (VMS, ULTRIX, Ethernet TCP/IP)	CATS logic/concurrent fault acceleration systems; OEM of Mach 1000 accelerator (ZyCAD); CATS hardware modeler models 6000, 8000, 10,000	Interfaces to Mentor; EDIF; TEGAS; FutureNet; Case Technology; PCAD; Cadnetix; Zuken; Computervision; Racal-Redac	Behavioral Description Language (BDL)	2500 SSI/MSI TTL and ECL; LSI Logic, SMC, VLSI Technology cell libraries; Fairchild, NEC gate arrays; Quadtree VLSI libraries; all Future Net libraries; Gould
Integrated Silicon Design Pty Ltd. 230 North Terrace Adelaide SA 5000 Australia A.R. Grasso Technical Manager +61-8-223 5802	**PHASE ONE** **PHASE TWO** **PHASE THREE** Prices not specified VAX (VMS, UNIX), MicroVAX (VMS, Ultrix); Apollo 3000/4000 (DOMAIN IX); Sun 3/4 (UNIX); PC AT with EGA (MS-DOS, XENIX)	None	None	Integrated system specification language, used in the system simulator	None

N/s = Not Supplied By Vendor N/a = Not Available

Design analysis		Design transfer		Additional capabilities	
Simulators and capabilities	**Timing analysis**	**Netlist outputs**	**Test vector outputs**	**IC/PCB layout**	**Other tools, comments**
VERILOG Behavioral, functional, gate, and switch simulator **VERILOG-XL** Accelerated gate and switch simulator (plus all VERILOG capability) **VERIFAULT-XL** Concurrent and distributed fault simulation	None	None specified	Through Test Systems Strategies	None	TESTSCAN (ATPG and fault simulation for scan design systems); BITGRADE (fault simulation for BIST designs); VHDL support; remote graphics
SLICE Circuit simulator **CADAT** (HHB Systems) Switch, gate, behavioral simulator **TA** (Cadence) Timing analyzer **CADAT** (HHB Systems) Fault and logic simulator **CADAT** (HHB Systems) Hardware modeler	TA timing analyzer provided by Cadence (worst-case delays, timing diagrams for selected nets may be displayed, auto-model generation is provided)	EDIF input, GDS II output	Sentry	IC layout from Cadence accepts Cadence and HDL inputs; capable of adding custom cells and macroblocks to design; generates routing parasitics	Automatic sizing of bipolar transistors; logic optimization for area or speed; synthesis of logic circuits from Boolean expressions; schematic creation from netlist; VGH200RH Rad Hard gate array and Rad Hard library from Silicon Compiler Systems
HISIM Design verification simulator **HITIME** Dynamic timing analysis software **HIFAULT** High-performance fault simulation **HITEST** Computer-assisted test generation suite	Integral in HISIM Integral in HITIME Integral in HIFAULT	ASCII text files	To GenRad board test systems via HIPOST; to other test systems via Test Systems Strategies Inc. (TSSI)	None	EDIF 2.0 netlist reader; VHDL support
Analog Workbench (Analog Design Tools) Circuit simulation, virtual instruments, and analysis **HILO-3 Logic Simulator** (GenRad) Behavioral, functional, gate, and switch simulation; logic and fault simulator; HICHIP physical modeler	In HILO-3	HP-generic; user-definable; SCICARDS; Racal-Redac RINF; Calay; Computervision, EDIF, HP printed circuit design system	HP 82000 IC verification system; HP3065 board testers; HP16500A logic analysis system	Graphics editors, IC layout analysis, IC symbolic layout and compaction (VTI and SDA Systems); automatic IC layout (VTI); CR 2000 hybrid IC design software (Zuken); Printed Circuit Design System (Hewlett-Packard)	Bundled design database language provides database access; bidirectional link with HP PLD design system; software link to transfer HP 64000 data to HILO-3 memory and microprocessor models
CADAT 7.0 Behavioral, functional, gate, and switch simulator; hardware modeling; concurrent fault simulator; simulation acceleration	Worst-case timing simulation through CADAT	Mentor; EDIF; TEGAS; FutureNet; Case; PCAD; Cadnetix; Zuken	Standard interface to CADAT binary databases; Factron; ITG/CADIF; IMS	None	PALGEN PAL model generation; INTELLIGEN testability analysis and test generation for sequential scan or nonscan designs
PROBE Circuit simulator **SYSMOD** Functional simulator using specification language	SYSMOD system simulation and timing analysis	SPICE; SIM (Berkeley); ISDL (internal format)	None	PLAN IC geometric editor; SYSGEN symbolic layout; SYMEDIT symbolic layout; SYSPLAN floorplanner; CHECK, NET, ELEC, SYSCHECK layout analysis	None

Directory of CAE Systems (continued)

Vendor Contact	System overview		Design entry		
	Product name, cost, and host	Applications hardware	Schematics	HDLs	Standard libraries
Intergraph Corp. 1 Madison Industrial Pk. Huntsville, Ala. 35805 Beverly Staley Electronics Marketing Engineer (205) 772-2000	**Design Engineer** $21k+, turnkey Intergraph Clipper-based standalone workstation (UNIX V 5.3.1; XNS/Ethernet TCP/IP) tied to a VAX host **Design Engineer PC** $3k, software only IBM/AT or compatible (PC-DOS 3.3)	Design Engineer interface to Zy-CAD's Mach 1000 hardware accelerator and IKOS 800 or 1900 hardware simulator and GenRad's HI-CHIP physical modeler	Design Engineer Design Engineer PC	Design Engineer: IKOS' TDL and system HILO HDL	Design Engineer and Design Engineer PC 4000 TTL, ECL, CMOS, memory, microprocessors, peripherals, discrete devices, major ASIC vendor libraries
LSI Logic Corp. 1551 McCarthy Blvd. Milpitas, Calif. 95035 Van Lewing Director of Software Marketing (408) 433-7204	**System Integrator** $75k+, software only Sun 3, Sun 4 (UNIX, NFS); IBM 30xx (VM/CMS-compatible); VAX, MicroVAX (VMS, DECnet); Apollo 3000, DN570, DN580, 4000 (DOMAIN IX)	Interfaces to LSI Logic accelerators; ZyCAD LE and FE accelerators	LSED	Network description language (NDL); hierarchical network description language (HNDL); Behavioral Specification Language (BSL)	Gate-model libraries; behavioral libraries in development
	Silicon Integrator From $75k, software only Sun 3, Sun 4 (UNIX); IBM 30xx (VM/CMS-compatible); VAX, MicroVAX (VMS); Apollo 3000 DN570, DN580, 4000 (DOMAIN IX); vendor-supplied networks	Interfaces to LSI Logic accelerators (ACCELSI) for logic and/or fault simulation, ZyCAD LE and FE accelerators	LSED		
	Logic Integrator $75k+, software only Sun 3 (UNIX); vendor-supplied networks	None			
Matra Design Semiconductor 2895 Northwestern Pkwy. Santa Clara, Calif. 95051 Pradip Madan Vice President of Marketing and Sales (408) 986-9000	**GATEAID PLUS/PC** $945, software only Compaq 386, PC/XT, AT; Telenet X.25 connection to MDS host	None	DRAFT (adapted from OrCAD)	Boolean equation language and translator	Standard cells: TTL, CMOS SSI/MSI; PLDs
	GATEAID II gate array design system $25k+, software only MicroVAX, VAX (VMS)	None	GED graphics editor	FML (GenRad)	Standard cells: TTL, CMOS SSI/MSI; bit-slice LSI; RAM blocks; multiplier; UART
	LSIntegrator (Silicon Compiler Systems Corp.) Price not specified Sun (UNIX)	None	LED graphics editor	L-Language	Standard cells: ALU; sequencer; RAM; datapath elements
Mentor Graphics Corp. 8500 S.W. Creekside Place Beaverton, Ore. 97005 Mohan Nair Marketing Director (503) 626-7000	**Entry Station** $1995, software only PC/XT, AT **Capture Station** $12.5k, turnkey **Design Station** $23.7k, turnkey **Idea Station** $33.7k, turnkey Apollo (AEGIS, UNIX; Domain, Ethernet TCP/IP, HASP, 3270, X.25)	HML hardware modeling system; Compute Engine accelerator; XSIM interface to ZyCAD	NETED/SYMED	Behavioral language models (extension of C and Pascal); VHDL product available first half 1989	1239 TTL; 123 ECL; 571 CMOS, 70 PLDs; 146 memory; 1800 analog; 85 HML; 109 generic library

N/s = Not Supplied By Vendor N/a = Not Available

Design analysis		Design transfer		Additional capabilities	
Simulators and capabilities	**Timing analysis**	**Netlist outputs**	**Test vector outputs**	**IC/PCB layout**	**Other tools, comments**
Design Engineer **CSPICE** Analog circuit simulator with virtual test instrument interface and pole zero, statistical, worst-case, Monte Carlo, time domain, frequency domain, DC, temperature, noise, distortion, spectrum, and sensitivity analysis **SYSTEM HILO** **HISIM** Fault-free simulator **HITIME** Dynamic timing analysis simulator **HIFAULT** Fault simulator **HICHIP** Hardware modeler **HITEST** Test vector generator **IKOS** ASIC logic analyzer, logic simulation and fault simulation	Design Engineer System HILO - HITIME	Design Engineer HILO; user-reformatable ASCII netlist; Mitsubishi; SMOS and EDIF 2 0 0; FutureNet; Design Engineer PC CSPICE; HILO-3, Intergraph, Xilinx	Design Engineer and Design Engineer PC HIPOST (GenRAD 2270 series); Factron 303, 323, 330, 333; HP 3065; ESP model 7100; Marconi system 80	PCB Engineer, package libraries DIPs, SIPs, SMDs, automatic placement, automatic routing with blind/buried vias, on-line DRC and CAM; Tancell (Tangent Systems) automatic timing-driven cell-based IC layout	Hybrid Engineer for hybrid layout form thick/thin film hybrid circuits, Optronics, Gerber, and HP plotters
Multichip gate-level simulator; multichip mixed behavioral/gate simulator **ACCELSI** Hardware-accelerated gate simulator	Path timing analyzer for multichip timing analysis	Network description language (NDL)	None	None	
LDS Single-chip gate simulator **BSIM** Single-chip behavioral/gate simulator All simulators handle detailed delay prediction; back annotation is supported for delay prediction for distributed delay values	Path timing analyzer for single-chip timing analysis	Network description language (NDL); hierarchical network description language (HNDL)	Ando; Sentry; Trillium	Layout integrator	Power analysis; automatic schematic generation from NDL netlist; logic synthesis; PAL synthesis; logic compilers; multiplier compilers; memory compilers; TESTLSI automatic test pattern generation
None	None	None	None	None	None
ARCIS Gate simulator	ARCIS timing analyzer; spike analyzer; WAVE waveform analyzer	ARCIS	Fairchild; ARCOP testability analyzer for 100% testability analysis	Proprietary	Bulletin board for data transfer and support
HILO-3 (GenRad) Gate simulator	ARCIS timing analyzer; in HILO-3	ARCIS; HILO-3 format			
LSIM (Silicon Compiler Systems) Behavioral, gate, switch, and timing simulator	In L-SIM	None			
MSIMON MOS circuit simulator **MSPICE** Circuit simulator **QUICKSIM** Behavioral, functional, gate, and switch simulator **QUICKFAULT** Fault simulator New analog simulator and library available first half 1989	TVER; QUICKPATH (graphical critical path analyzer)	TDL; EDIF 200; SPICE; Computervision; ILOGS; NCA; SCICARDS; Racal-Redac; MASKAP; Valid; LOGCAP; GDS II and many other netlist outputs available	HP; GenRad; Advantest; Ando; Marconi; Sentry; Teradyne; ASIX; IMS; STS; Tektronix; Trillium; ASC II (through Test System Strategies Inc.)	Gate array layout; standard-cell layout; full-custom IC layout; PCB layout	PLD synthesis capability; ASIC vendor-independent designer; electronic packaging and thermal analysis; CASE tools; documentation

Directory of CAE Systems (continued)

Vendor Contact	System overview		Design entry		
	Product name, cost, and host	Applications hardware	Schematics	HDLs	Standard libraries
MIETEC Raketstraat 62 1130 Brussels, Belgium J.Y. Peigne Communications Director (32) 2-728-1811	**MIETEC design system** Price not specified DAS 9100	None	SDS (Silvar-Lisco)	DAML	Standard-cell libraries, mixed digital-analog; CMOS; BiMOS
Motorola Inc., Semicustom Division 1300 North Alma School Rd. Chandler, Ariz. 85224 Andy Graham DASG Manager (602) 821-4180	**Design Verification Module** $7.5k, software only Mentor Idea Station, Daisy Logician, Personal Logician, Valid CAE **Open Architecture CAD System** $50k+, software only Apollo 3xxx, 4xxx, Sun 3, Sun 4, VAX	None	Supports Mentor (NETED); Daisy (DED and GED); Valid	Verilog HDL hardware description language	Motorola gate array libraries; 2-micron HCA62A series; HDC series of high-density CMOS arrays
Omation Inc. 1210 East Campbell Rd. Richardson, Tex. 75081 John Hoskins Vice President of Marketing (214) 231-5167	**SCHEMA II+** $495, software only **SCHEMA-PCB** integrated PCB layout $975, software only **SCHEMA-ROUTE** autorouter $750, software only IBM PC and compatibles (DOS)	None	SCHEMA II SCHEMA II+	None	Over 4000 unique symbols: standard TTL SSI/MSI; memory; PALs; microprocessors; analog; discrete; CMOS; ECL; analog
OrCAD Systems Corp. 1049 SW Baseline St. Suite 500 Hillsboro, Ore. 97123 Jim Edgerton Marketing Communications Manager (503) 640-9488	**OrCAD/SDT III** $495, software only **OrCAD/VST** $995, software only **OrCAD/PCB** $1495, software only **OrCAD/PLD** $495, software only **OrCAD/MOD** $495, software only PC/XT, AT, PS/2 (MS-DOS)	None	OrCAD/SDT III (schematic capture); OrCAD/PLD (PLD documentation to SDT III)	OrCAD/PLD (procedural language for state machines)	3700 parts including 1700 TTL, 335 CMOS, 184 ECL, 300 microprocessors and peripherals, 660 PALs and memory, 320 discrete, 235 analog
Personal CAD Systems Inc. 1290 Parkmoor Ave. San Jose, Calif. 95126 Terry Zimmerman Vice President, Marketing (408) 971-1300	**Master Schematic** $1.5k, software only PC/XT, AT (DOS); HP Vectra; Olivetti; TI Professional; NEC PC-98XA; Ethernet, Novell software, 3Com	None	PCCAPS hierarchical schematic capture	None	More than 6000 parts including TTL, CMOS, ECL, microprocessors, memory, analog
Phase Three Logic Inc. 1600 NW 167 Pl. Beaverton, Ore. 97006 Karen Beall Director, Graphics CAE/CAD Systems (503) 645-0313	**CFx000** $395, software only (except for CF3550) PC AT or PS/2 with EGA/VGA card (MS-DOS, TCP/IP); Sun 3 (NFS, TCP/IP), Sun 4, Sun 386i, color or monochrome	Interfaces to HILO-3 (GenRad); ZyCAD accelerators; HI-CHIP hardware modeling system (GenRad)	SCHEDIT schematic editor	HILO-3 (GenRad)	2000+ parts in symbol library, including TTL, CMOS, ECL, microprocessors, support chips; GenRad simulation model libraries; HILO models for MMI PALs
Prime Computervision Division 100 Crosby Dr. Bedford, Mass. 01730 Product Marketing Manager (617) 275-1800	**CADDStation** $55.3k, turnkey 68020-based workstations (UNIX, Ethernet, TCP/IP, NFS) **Personal Engineer** $3.5k, software only IBM PC and compatibles (PC-DOS) **Personal Engineer/CV386** $11.5k, turnkey 80386-based PCs (MS-DOS 3.2)	CATS hardware modeling system (HHB Systems)	Schedit/Symed	HDL (GenRad); CADAT, BMI (HHB Systems) HDL	3000 TTL/ECL parts; 15 PLDs; 40 memory; 40 LSWLSI; 800 analog parts; 300 primitives for CADAT and Saber modeling; same libraries on Personal Engineer
Quantic Laboratories Inc. Suite 200 281 McDermot Ave Winnipeg, Manitoba Canada R3B OS9 Richard Facia Marketing Manager (204) 943-2552 (800) 665-0235 (in U.S.)	**GREENFIELD** $35k US and up, software only Sun 3 (UNIX); Apollo (Aegis, Domain); HP 9000/320, 350, 360 (HP UX); MicroVAX (VMS); VAX (VMS); Prime (Primos); Cray (Unicos)	None	Schematic capture	None	None

N/s = Not Supplied By Vendor N/a = Not Available

Design analysis		Design transfer		Additional capabilities	
Simulators and capabilities	**Timing analysis**	**Netlist outputs**	**Test vector outputs**	**IC/PCB layout**	**Other tools, comments**
ANASIM Circuit simulator **DIGSIM** Functional and gate simulator **DAML** Behavioral simulator **FLTSIM** Fault simulator **MIXSIM** Mixed-mode (digital/analog) simulator	Under development	SDL (Silvar-Lisco); Daisy; Valid; Mentor	Sentry VII, 20, 21; Teradyne 300 series; NTDF (ITT-Alcatel)	IC layout (Calma and Computervision); DRC, ERC, CPA (MASKAP, ECAD); automatic IC layout (Silvar-Lisco)	Silicon compilers; PLA, RAM, ROM module generators; switched-capacitor filter compiler
QUICKSIM (Mentor) Behavioral/gate simulator **DLS** (Daisy) Gate-level simulator **Verilog XL** Behavioral, gate, switch, simulator	MTA timing analysis; (NCR) Critical path trace static timing analysis	TDL; Logcap; EDIF 2.0	Tester-independent code	TANGATE sea of gates array layout (Tangent Systems); MERILYN-G gate array layout (Tektronix)	None
Netlist to PSPICE, SPICE, Susic, P/C SILOS and others; Schema-silos to be released in early 1989	None	Cadnetix; Calay; Computervision; DataCon; FutureNet; Intergraph; PADS PCB; P-CAD; Racal-Redac; SCICARDS; SPICE; Tango-PCB; Telesis; Salt; and others	None	Schema-PCB and route plus interfaces to several other programs	Xilinix XACT and Intel IPLDs II interfaces; backward and forward annotation with full error checking, on-line ports browsing, real-time object editor, unlimited levels of hierarchy
OrCAD/VST Functional gate simulator **OrCAD/MOD** PLD description module for VST SPICE shell is built into schematic capture package	In OrCAD/VST and OrCAD/MOD	Applicon Bravo and Leap; Algorex; Calay; Cadnetix; Computervision; DXF; EDIF; FutureNet; Intergraph; MultiWire; PCAD; Salt; SPICE; SCICARDS; Racal-Redac; Telesis; Vectron; PADS; TANGO	None	OrCAD/PCB (printed circuit board layout with autorouter) Interface to Applicon; Algorex; Calay; Cadnetix; Computervision; FutureNet; Intergraph; PCAD; PADS; SCICARDS; Racal-Redac; Telesis; TANGO; Vectron	PLD programming tools, many library interfaces from third-party vendors, scalable text and objects, hierarchy, object editor, DeMorgan conversion, part rotation, on-line part browsing, keyboard macros, A through E size work sheets, SMT support on PCB layout
PC-LOGS Behavioral, gate, and switch simulator **P-SPICE** Analog circuit simulator	None	EDIF; TEGAS; HILO; SPICE; CADAT; SCICARDS; Computervision; CBDS; Calay; Racal-Redac	None	SMT and thru-hole PCB layout; automatic PCB layout; CAM output; Gerber output; ECO; entry level and advanced packages	Hierarchy; on-line design rule checking; thermal analysis; extensive schematic features
Berkeley SPICE (for Sun) PSPICE (for IBM PC AT) (MicroSim) Circuit simulator **HILO-3** (GenRad) Behavioral, functional, and gate simulator; fault simulator	in HILO-3	Computervision Cadds4X and Cadds3; Racal-Redac; SCICARDS, PADS	HIPOST (GenRad)	CF/PCB integrated schematic design and PCB layout system	Symbol editor, compiler; programmable netlist library extraction; interactive waveform grapher; plotting program
SPICE 2G.6 Circuit simulator **HILO** (GenRad) Logic and fault simulator **SABER** (Analogy Inc.) Circuit simulator **CADAT 6** (HHB Systems) Behavioral, functional, logic, and switch simulator	DTV (Dynamic Timing Verifier)	CADDS 4X; HILO-3, SPICE 2G6, ELF; EDIF 2.0; PNL interface tools; Silvar Lisco GARDS	HILO-3 ATG (GenRad); CADAT 6	Autoboard SMT on the CADDStation system, production drafting, military specification drafting; PCB thermal analysis (Pacific Numerix)	Simulation grapher; programmable logic device design software; load checking routines; bill of materials generator; model generator design checker (rules based verifier)
PHYLLIS Analog simulation of digital circuits SPICE compatible (SPICE not included)	None	ASCII format; SPICE files; EDIF 2.0; IGES	N/a	None	Magnetic and electric field analysis, field plots, SPICE input, board, cable, connector, hybrid, IC packaging analysis

Directory of CAE Systems (continued)

Vendor Contact	System overview		Design entry		
	Product name, cost, and host	Applications hardware	Schematics	HDLs	Standard libraries
Racal-Redac Inc. 238 Littleton Rd. Westford, Mass. 01886 Dave DeMaria Director of Technical Marketing (508) 692-4900	**VISULA CAE** $26k, software only **VISULA CAE/CAD** $60k, software only VAXstation II (VMS); Apollo (UNIX); Sun (UNIX) **MAXI/PC** $995 **CADSTAR** $4850 software only Integrated Logic Capture/PCB Design Compaq 386, IBM PC AT or compatible, IBM PS/2 (MS DOS) with EGA and high resolution graphics; Ungerman-Bass; Fox Research 10-Net; Excellon	CATS hardware modeler and simulation accelerator (HHB Systems) None	VISULA SCM hierarchical schematic capture REDLOG	In CADAT (HHB Systems) None	2000 models (TTL, CMOS) up to LSI complexity; 200+ behavioral and hardware models Variable
Royal Digital Systems Inc. 2855 Kifer Rd. Santa Clara, Calif. 95050 Ray U'ren Vice President (408) 980-9492	**SCEPTER** $19,999/$29,999, software only Sun (UNIX); Silicon Graphics	None	Intergraph; Case; SCICARDS, V.L FIN, OrCAD, P-CAD	None	2200, including TTL, LSTTL, CMOS, microprocessors and peripherals, ECL, discrete, passive, analog
Schlumberger CAD/CAM 2833 Junction Ave. Suite 200 San Jose, Calif. 95134 Brian Gardner Product Manager (408) 433-4880	**BRAVO 3 Electronic Design** $10k–$50k VAX (VMS), Sun (UNIX)	Interface to hardware modeler	Schematic capture	None	Numerous catalogs, including TI TTL, Motorola STTL, Motorola HCMOS, and Fairchild FAST
Scientific Calculations Inc. 7796 Victor-Mendon Rd. P.O. Box H Fishers, N.Y. 14453 Douglas Spice Director of Marketing Services (716) 924-9303	**SCIDESIGN** $3k **CADAT** PC/XT, AT MicroVAX/GPX (DOS 2.1; Kermit, DECnet-DOS communications)	CATS hardware modeler and simulation accelerator (HHB Systems)	SCIDESIGN	In CADAT	+500 SSI/MSI TTL and ECL; generic PLA, RAM, and ROM models; 68000 and 2900 families
Seattle Silicon Corp. 3075 112th Ave. NE Bellevue, Wash. 98004 Richard Ahlquist Marketing Manager (206) 828-4422	**ChipCrafter ASIC Design System** $59k, software only Mentor Idea series (Apollo 3000, 4000) **ChipCrafter ASIC Expert Option** $49k, software only Mentor Idea series (Apollo 3000, 4000) **ChipCrafter IC Expert Option** $41k, software only Mentor Idea series (Apollo 3000, 4000)	Simulation accelerators (Mentor, ZyCAD)	Design entry through Mentor NETED	Joint development with JRS Research for VHDL interface	Standard cells; configurable SSI, MSI, PLA, RAM, ROM, FIFO, I/O; datapath compiler; logic synthesis for state machines and random logic
Silicon Compiler Systems Corp. 2045 Hamilton Ave. San Jose, Calif. 95125 Jeff Elias Marketing Manager (408) 371-2900 Richard Gordon Marketing Manager (201) 580-0102	**GENESIL** $125k, software only VAX, MicroVAX (ULTRIX); Apollo (DOMAIN IX); Sun (UNIX); Ethernet TCP/IP **Logic Compiler** $23.5k, software only **ATG** $49.5k, software only **GDT** $88k, software only **Lsim** $49.5k, software only **Ltime** $40k, software only Apollo (DOMAIN IX); DEC (ULTRIX); Sun (UNIX)	Interfaces to Mach 1000 logic/fault accelerator None	Interfaces to Mentor Led interactive schematic and layout editor	None L language for VLSI; M language for behavioral description	Library of CMOS compilers; datapath, multiplier Lcompilers generator libraries include standard cells, PLA, RAM, ROM, datapath, memory, CRT controller, core microprocessor

N/s = Not Supplied By Vendor N/a = Not Available

Design analysis		Design transfer		Additional capabilities	
Simulators and capabilities	**Timing analysis**	**Netlist outputs**	**Test vector outputs**	**IC/PCB layout**	**Other tools, comments**
SPICE (Berkeley Version 2G6) Circuit simulator **SABER 2.1** Analog system simulator **CADAT 6.1** (HHB Systems) Behavioral, gate, and switch simulator; concurrent fault simulator	in CADAT in SABER	CADAT 5.1; HILO; SPICE	Eaton Model 800; Sentry	VISULA PCB automatic layout	VISULA SCM on-line electrical rule checking; REDLOG/REDCAD waveform analysis
Interfaces to Personal CADAT Interfaces to PACSIM, PSPICE circuit simulators	In P-CADAT	Racal-Redac; HHB Systems	None	CADSTAR MAXI/PC Geometry editor; layout analysis; automatic placement and routing	REDSOFT customer support/software maintenance product
N/s	N/s	AutoMate; SCICARDS; Calay; Cadnetics; Valid; Daisy; Mentor; FutureNet; Racal-Redac; Case	None	Automatic PCB layout, including SMD	Expert board, auto placement, auto-routing
Logic Analysis (enhanced CADAT) Functional, logic, behavioral, and fault simulator	Timing simulation in CADAT	CADAT; SPICE; template to reformat for others	Factron; Sentry; GenRad	BRAVO 3 VLSI geometry editor; ECAD layout analysis; BRAVO 3 PCB layout editor; automatic placement and routing (Algorex)	PG and E-beam interfaces; photoplot, drill, insertion, mechanical 3D design, and analysis of PCBs
SPICE Circuit simulator **CADAT 6.1** Behavioral, gate, and switch; concurrent fault simulation	In CADAT	SCIDESIGN ASCII netlist data; CV3; SPICE; CADAT	Sentry	SCICARDS PCB geometry editor and automatic placement and routing	Complete database extraction and reformatting tools
Interface to Mentor QUICKSIM	SSC static timing analyzer	Mentor; SILOS	Sentry	ChipCrafter ASIC Design System: Automatic place and route; layout view; automatic buffer sizing; automatic variable layout for different manufacturing processes ChipCrafter ASIC Expert Option: Adds foreign module integration; interactive layout; manual override of buffer sizing; polygon-level geometry view Chipcrafter IC Expert Option: Adds bidirectional translators for GDSII and CIF formats; LVS analysis tools; interfaces to Mentor ChipGraph and DRACULA DRC	ASIC operations provides verification, fabrication, packaging, test for prototypes and production volumes
In GENESIL Functional logic simulator with switch-level option; interface to Mentor QUICKSIM	GENESIL timing analyzer	Mentor	N/s	Interactive and automatic IC layout tools; LogicCompiler: automatic layout of logically optimized standard cells	ATG: Automatic test pattern generation
Lsim Behavioral, functional/gate, and switch simulation integrated with ADEPT circuit simulation; fault simulation (both serial and probabilistic); Lspice analog simulation	Ltime Timing Analyzer (in house); RC tree-based switch-level timing analysis	SPICE; EDIF	IMS; Sentry 7, 8, 20, 21; Advantest	Led IC layout, geometry editing, mask-level symbolic layout compaction, procedural layout, floorplanning; LRC electrical and design rule checking; Lextract database extraction routines; Lpar automatic placement and routing of standard cells and blocks	L Database Interface (Ldbi)

Directory of CAE Systems (continued)

Vendor Contact	System overview		Design entry		
	Product name, cost, and host	Applications hardware	Schematics	HDLs	Standard libraries
Silvar-Lisco 1080 Marsh Rd. Menlo Park, Calif. 94025 Tony Wainwright (415) 324-0700	**Design Entry** $6k+ **Logic Design System** $25k+ **System Design** $40k+ **Mixed Analog/Digital Simulation System** $25k+ **Switched Capacitor Simulation System** $23k+ MicroVAX, VAX (VMS); PC AT, 43xx, 9370, 30xx (MS-DOS, VM/CMS); Apollo (AEGIS); Sun (UNIX); DECnet, Ethernet, Domain	Interface to HHB Systems simulation accelerator	Schematic Design System (SDS)	HELIX HHDL	4000 SSI/MSI TTL; 328 PLDs; 162 memory; 120+ LSI/VLSI (available through Quadtree); 70 miscellaneous CMOS; additional simulation libraries from Quadtree Corp.
Spectrum Software 1021 S. Wolfe Rd. Sunnyvale, Calif. 94086 Karen Burchfiel Customer Service Representative (408) 738-4387	**MICRO-CAP II** Electronic Circuit Analysis Program $895 **MICRO-CAP III** Electronic Circuit Analysis Program $1495 **MICRO-LOGIC II** Digital Circuit Simulation Program $895 IBM PC/XT, AT or IBM PS/2 or fully compatible (DOS 3.0 and above)	None	Micro-Cap II, Micro-Cap III, and Micro-Logic II schematic capture	None	›200 for Micro-Cap II and Micro-Cap III; 200 elements for Micro-Logic II
Tanner Research 128 W. Del Mar Blvd. Pasadena, Calif. 91105 David Lipin Product Manager (818) 795-1696	**Gatesim** $950, software only PC, XT, AT, 386, PS/2, or compatible **Netlist Package** $200, software only PC, XT, AT, 386, PS/2, or compatible	N/s	Interface to OrCAD schematic capture	None	1200 cell vendor-independent schematic library Mapping libraries available separately ($200 each) for ASIC vendors: GE Solid State, National, NCR, Oki, TI, and customer owned standard cell layout library for customer-owned layout
Teradyne Inc. 321 Harrison Ave. Boston, Mass. 02118 Daryl Layzer Marketing Services Manager (LASER Version 6) (617) 482-2700 x2808	**LASAR Version 6 Simulation Software** $15k+, software only VAX (VMS), Sun (UNIX); DECnet; NFS	DATASource hardware modeling system	N/s	TML register-transfer language; LABEL behavioral language	3800 SSI/MSI TTL, ECL; generators for memory; 200+ LSI/VLSI; 40+ VLSI hardware models; gate array macrocells
Teradyne EDA 5155 Old Ironsides Dr. Santa Clara, Calif. 95054 Georgia Marszalek Director of Marketing Communications (408) 980-5200	**AIDA Design System** $140k, turnkey Apollo (UNIX, Domain, Domain gateways: SNA, VAX, Ethernet, etc.); Sun 3 (UNIX, NFS) **Vanguard CAE Design System** $5k–$25k, software only **Vanguard Stellar CAE Design System** $5k–$80k, software only PC/XT, AT (PC-DOS); VAX (VMS, DECnet); Sun (UNIX, NFS, PC NFS); Ethernet TCP/IP	AIDA simulator accelerators; interface to D300 hardware modeler Interface to Teradyne D300 hardware modeler	Vanguard Schematic Design System Vanguard Schematic Design System	AIDA Design Language SCALD design language (Lawrence Livermore National Lab)	Advanced CMOS gate array libraries: 100+ parts each 5000+ parts: TTL, ECL, CMOS, PLDs, ASICs, and microprocessor families

N/s = Not Supplied By Vendor N/a = Not Available

Design analysis		Design transfer		Additional capabilities	
Simulators and capabilities	**Timing analysis**	**Netlist outputs**	**Test vector outputs**	**IC/PCB layout**	**Other tools, comments**
HELIX Behavioral simulator **CADAT** (HHB Systems) Functional/gate simulator **ANDI** Switch simulator (mixed analog analysis) **SWAP** Switched-capacitor filter analysis	Simulation libraries for HELIX contain "intelligent" behavioral models that also perform timing checks; also timing analysis in CADAT	CADAT; SPICE; HILO; LOGCAP; TEGAS; SILOS; CBDS; SCICARDS; Racal-Redac; SUPER-COMPACT; SECMAI/OPTIMA	Sentry; GenRad; Advantest; Teradyne; IMS (through Test Systems Strategies Inc.)	Automatic gate-array and standard-cell layout; IC layout design; layout analysis; PCB placement and routing; (GARDS, Avant Gards, SCII, DVP, Princess, CAL-PC)	Design databases (both netlist and schematic) are portable between supported brands of hardware; EDIF support
Micro-Cap II Analog circuit simulator **Micro-Cap III** Analog circuit simulator **Micro-Logic II** Logic circuit simulator	Micro-Cap II: transient, ac, dc and Fourier, worst case, temperature stepping; Micro-Cap III: transient, ac, dc, and Fourier, worst case, monte carlo, parameter stepping, temperature stepping; Micro-Logic II: timing analysis	Micro-CAP II and Micro-Logic II: ASCII output; Micro-Cap III: ASCII output and output to SPICE netlist	Micro-Logic II: ASCII format	None	Notepad and built-in calculator included with Micro-Cap III; mouse support for Micro-Logic II and Micro-Cap III
GateSim Gate level timing simulator with automatic fault grading capability	Static timing analysis in GateSim	Flexible format translator produces HILO, TEGAS, and others (user-defined)	Flexible format translator produces HILO, TEGAS, and others (user-defined)	L-Edit hierarchical layout editor for ICs and PCBs; DRC and standard-cell place and route packages available for L-Edit	Tool set supports vendor independent design style with automatic mapping to any of several commercial ASIC vendors or to your own layout
LASAR Version 6 Behavioral, functional, and gate simulator; hardware modeling; fault simulator; automatic test pattern generation; interface to DATASource hardware modeling system	True worst-case timing analysis with common ambiguity removal	N/s	Teradyne L1xx, L2xx, J9xx; Computer Automation 4700, 4900, Marathon; GenRad 197x, 2225, 2235; Hewlett-Packard DTS70; Sentry 7–21; also supported by Test System Strategies Inc.'s TDS system	None	CircuitMaker and CircuitBreaker for PLD modeling and ATPG
AIDA Transient Analysis Program Circuit simulator **AIDA Logic Simulator** Logic simulator with optional accelerators **AIDA Fault Simulator and AIDA Fault Inferencer** Fault simulators with optional accelerators **Case/AIDA** (AIDA) Logic and fault simulator **CASE/LASAR** Logic simulator **Case/SPICE** (Meta-Software, MicroSim) Circuit simulator **Case/SILOS** (SimuCAD) IC simulator Other simulator interfaces available	AIDA Timing Verifier Timing Verifier	TEGAS Design Language (TDL); foundry-specific (contact company) EDIF, TEGAS; SCICARDS; Racal-Redac; Telesis; CV-CADDS4X; CBDS; Cadnetix; Calay; Mentor; HP; Applicon SPICE; CADAT; LSI Logic; SILOS; SALT; ZyCAD; HILO	Foundry-specific (contact company) See Teradyne LASAR description	None Interfaces to Cadnetix, Racal-Redac, Calay, SCICARDS, Academi	AIDA automatic test pattern generator Documentation interfaces to Interleaf and Ventura Publishing; interfaces to ASK's MANMAN manufacturing software; programmable electrical rule checker; graphics framework interface to third party tools; automatic PCB autorouter

Directory of CAE Systems (continued)

Vendor Contact	System overview		Design entry		
	Product name, cost, and host	Applications hardware	Schematics	HDLs	Standard libraries
Valid Logic Systems Inc. 2820 Orchard Pkwy. San Jose, Calif. 95134 Nancy Madison Director Product Marketing (CAE/IC CAD) (408) 432-9400	**Design Entry System** $5.9k+ **Logic Design System** $9.9k+ **Design Validation System** $17.5k+ **ADvantage Analog Design System** $21.7k+ **RapidTEST Fault Simulation System** $17.5k VAX, VAXstation (VMS); Sun (UNIX); PC AT (UNIX); SCALDsystem (UNIX); Ethernet TCP/IP, DECnet, VAXcluster (LAVC)	Realchip hardware modeler; Networked Realchip; Realmodel hardware modeler; Realfast simulation accelerator, Realchip II	ValidGED; Transcribe	UCP C-based behavioral modeling language	4000+ TTL, ECL; 30+ PLDs; 60+ memory; 100+ LSI/VLSI; 100+ ASIC design kits; behavioral models from Logic Automation and Quadtree; analog libraries
Vamp Inc. 6753 Selma Ave. P.O. Box 411 Los Angeles, Calif. 90028 John Soluk Manager of Marketing (213) 466-5533	**McCAD Schematics** $495, software only **McCAD DACS** $295, software only Apple Macintosh 512, Macintosh Plus, Macintosh SE, Macintosh II; Apple Network	None	McCAD Schematics	None	200+ TTL; 100 discrete; 250 CMOS
Viewlogic Systems Inc. 313 Boston Post Rd. West Marlboro, Mass. 01752 Sri Sriram Vice President of Marketing (508) 480-0881	**Workview Series Software** for ASIC, system, analog design 1000 series (80286), $6k+; 2000 series (80286 "native mode"), $6.3k+; 3000 series (80386 "native mode"), $7.5k+; 5000 series (Sun), $10k+; 7000 series (VAX), $10k+	LM1000 hardware modeler; interface to ZyCAD	Viewdraw	VHDL	2000+ TTL; 100+ ECL; 100+ PLDs; 100+ memory; 50+ LSI/VLSI; 600+ analog; semicustom libraries from more than 12 vendors including LSI Logic Corp., and VLSI Technology Inc.
Visionics Corp. 3032 Bunker Hill Lane Suite 201 Santa Clara, Calif. 95050 Alex Wellins Public Relations Manager (800) 553-1177	**EE Designer I** $895 **EE Designer II** $1995 **EE Designer III** $3995 **EE Designer III/Extended** $5995 All are software only and all include autorouters; PC/XT, AT, PS/2, and compatibles	None	EE DESIGNER; ASCII, OrCAD; Schema; FutureNet	None	1000: TTL, CMOS, SMT, microprocessor, discretes, analog
VLSI Technology Inc. 1109 McKay Dr. San Jose, Calif. 95131 Bill Murray Tactical Marketing Manager (408) 434-3000	**VLSI Express Systems** $30k–$195k VAX (VMS); Apollo (AEGIS); HP series 9000, model 350 (UNIX); Sun 3 (UNIX), Sun 4	None	VTIschematic	Hierarchical Net List (HNL)	Portable gate array and standard-cell-compiler libraries for datapath logic synthesis, RAM, ROM, PLA
Xerox 475 Oakmead Pkwy. Sunnyvale, Calif. 94086 Petros Xides CAE Product Division Manager (408) 737-4307	**Expert Designer** $7k–$12k Xerox 6085; Ethernet; XNS; TCP/IP	None	Expert Schematics (new hierarchical schematics for systems design; drafting parts importation)	XDDL	1200 TTL, CMOS, and ECL symbols in schematic symbol library; 200 models in simulation model library
ZyCAD Corp. Endot Products 1380 Willow Rd. Menlo Park, Calif. 94025 Susan Runowicz-Smith Product Marketing Manager (415) 321-8574	**N.2 System Design Environment** $200k, software only MicroVAX to VAX 8800 (VMS, UNIX); Apollo (AEGIS), Sun (UNIX); CDC (NOS/VE); PC AT (GENIX); Ethernet TCP/IP	Interface to ZyCAD logic accelerators	Netlist interface to Mentor	ISP'; HDL; ISP' to VHDL; translator	Custom library support for system and subsystem entities through interfaces to workstations

N/s = Not Supplied By Vendor N/a = Not Available

Design analysis		Design transfer		Additional capabilities	
Simulators and capabilities	**Timing analysis**	**Netlist outputs**	**Test vector outputs**	**IC/PCB layout**	**Other tools, comments**
ValidSPICE PRECISE circuit simulator (Electrical Engineering Software) **ValidSIM** Behavioral, logic, and switch simulator with timing analysis **TIMEMILL** (EPIC Design Technology) Mixed-level timing simulator and critical path analyzer **RapidTEST** Fault simulator	ValidTIME; TIMEMILL (EPIC Design Technology)	HDL; HILO-3; LOGCAP; MCLDL; SPICE; TEGAS5; CADDS; Calay; CBDS; Paragon; Racal-Redac; SCICARDS; Wirewrap; ILOGS; LIL; FAIRLOGS; CPP; CADAM; SEL; SDL; SDIF; Applicon; LASAR	Teradyne; HP; GenRad; Zehntel; TSSI interfaces	IC layout editor; IC layout analysis; full-custom and standard-cell IC layout; Compose chip architecture environment; ALLEGRO interactive and automatic PCB layout	ValidPLD—automatic generation of timing and logic models; ValidEZLIB—creates new library components by modifying existing ones; DIAL—programming language for custom interface creation; Transcribe production documentation environment, plus netlist-driven schematic generation
McCAD DACS Circuit, logic, and behavioral simulator	In McCAD DACS	Computervision; Calay; Gerber; SCICARDS; McCAD	None	McCAD PCB-1, PCB-ST, and automatic routing tools	McCAD-to-Gerber translator module
VIEWSIM For behavioral, RTL, logic, switch, analog-level with timing **VIEWSIM/AD (enhanced PSPICE)** Mixed analog/digital simulator **HILO** (GenRad); **TEGAS** (Calma); **LASAR** (Teradyne); **SILOS** (SimuCAD); **ZILOS** (ZyCAD); **PSPICE** (MicroSim); **SPICE** (UC Berkeley); **HSPICE** (Meta-Software); **IG-SPICE** (A.B. Associates); **PRECISE** (EEsof); **ALLSPICE** (Acotech); **Touchstone** (EESof)	None	*CAE/CAD graphics:* Computervision CADDs 4, 4X, CADDSTATION; Daisy; Mentor; Metheus; Prime EDMS; Valid *PCB:* Redac (Redboards, Cadet, Maxi, Mini); Redac (DSM6); Academi; Applicon; CADES; Cadnetix; Calay; CBDS; Computervision; EDIF; Intergraph; MERLYN; OmniCad; P-CAD; PRANCE; Redac RINF (Visula); SCICARDS; Valid/Telesis *Simulators:* Bolt; CADAT; Computervision; MDL; Silvar-Lisco; SDL *PLD:* Altera, MMI, Xilinx *IC layout:* Cadence	None	Configurable design rule checker; VIEWPLACE for critical placement; layout interface to CAD	Document processor merges text and graphics; electronic mail system; data management; 80386 simulation tools to support ASIC design beyond 30,000 gates; Pre-CAD PCB placement for PCB design; analog stress/manufacturability analysis; CAE interfaces
5 simulators: Logic, timing, ac, dc, transient analysis	Included in all products	ASCII	None	Direct translation from netlist to layout, DRC, connectivity check, autoplacement, fab drawings	Gerber, N/C drill, printers, plotters, high-resolution graphics
VTIsim Behavioral, gate, and transistor simulator **VLSI Qsim** Behavioral and gate **VTISPICE** Circuit simulator	Timing Verifier	HNL netlist format	Sentry 10, 20	Sticks symbolic IC editor; automatic IC layout; cell compiler; datapath compiler; state machine compiler	None
Expert Logic Simulator Switch-level and logic simulation	None	LASAR; Computervision; Racal-Redac; SCICARDS; CADAT, HILO; EDIF; SPICE; user-definable data extractor	None	Expert PCB System board layout tools with SMD capability	Interfaces to VIEWPOINT (Xerox office automation system); IGES translator, it runs in the new environment as an application to Xerox VIEWPOINT; new tools for symbol creation
N.2 Mixed behavior/functional, register-transfer, gate simulator; software system simulator	None	Topology file in-house	User-created; test coverage tool	None	Stochastic performance analyzer; N.2 analysis environment; meta-assembler and retargetable linking loader; C behaviors, programs, and models can be linked; build tool for updating changes to models

Directory of Printed Circuit Board Layout Systems

Vendor Contact	System name, typical cost	Mainframe	Workstation	Software only	Hardware environment • System support • Memory support • Graphics support	• Design entry • Simulation	• ERC • DRC • Extraction	Output formats • Printer/plotter • Assembler • Tester; other
Academi Systems Inc. 2418 Armstrong St. Livermore, Calif. 94539 (415) 449-3294 Cynthia Peddie Vice President	**Academi 56000** $62.5k **Academi 54000** $39.8k	—	•	•	• DEC with attached processors • 1-MB main memory • Tablet input; 19″ display with 640×512 resolution	• Case, FutureNet interfaces • —	• — • Layout rule checker (batch) • CAE interface for circuit extractor	• Calcomp, DEC, HI, HP • Generic NC interface • —
Accel Technologies Inc. 7358 Trade St. San Diego, Calif. 92121 (619) 695-2000 Ray Schnorr Vice President of Marketing	**Tango-PCB** $600 **Tango-Route** $500 $1k if bought together	—	—	•	• PC/XT, AT, PS/2 (DOS 2.X); local-area network • 640-KB main memory and 2 disk drives • Mouse input; CGA, EGA, VGA, Hercules, 640×480, 800×600, 1024×768, 16 color	• Tango-Schematic; Omation, OrCAD, interfaces • —	• Electrical rule checker with Tango-PCB and Schematic • Design rule checker by Tango-Route • —	• HP-GL, DM-PL, Calcomp, IBM, Epson, Okidata, Toshiba printers, Gerber • Excellon • —
Aptos Systems Corp. 5274 Scotts Valley Dr. Scotts Valley, Calif. 95066 (408) 438-2199 John Roth President	**CRITERION** $995 **RGRAPH** (with graphics coprocessor) $6.7k	—	—	•	• PC AT, 80386-based PC; local-area-network • 640-KB main memory and hard disk • Mouse or digitizer input; 13″ monitor with EGA (CRITERION); 19″ monitor with 1024×768 resolution (RGRAPH)	• Aptos schematic capture; FutureNet, OrCAD, PCAD interfaces • TEGAS and PSPICE interfaces	• Common node checker • Layout rule checker • —	• Calcomp, Epson FX series, Gerber, HI, HP, Zeta • Excellon • —
Automated Systems Inc. 4105 Sorrento Valley Blvd. San Diego, Calif. 92121 (619) 546-0024 Andy Chmielinski Manager, PranceGT Product Marketing	**PranceGT** $90k	—	—	•	• DEC VAXstation 3500; ULTRIX/X windows; (no accelerators) • 16-32-MB main memory and 280-MB hard disk • Keyboard, mouse input; 19″ color monitor; 8 plane graphics (GPX)	• Netlist from most popular schematic capture/CAE systems • User interface based on X-windows standard utilizing pop-ups, pulldowns, dialogue boxes, etc.	• On-line • On-line and post-route • —	• HPGL, Gerber • — • Excellon, Trudrill
Cadam Inc. 1935 N. Buena Vista St. Burbank, Calif. 91504 (818) 841-9470 Alan Cohen Electrical Products Marketing	**IPC** (Interactive Prance CADAM) $116k per CPU	•	—	—	• Any IBM mainframe or compatibles (VM or MVS) • Standard memory • Mouse or tablet input; IBM 5080 scopes or compatibles	• Interface through CADEX • CADAT; two-way netlist translation	• Tolerance checker (batch and on-line) • Layout rule checker • CADEX circuit extractor; thermal analysis	• Benson, Calcomp, Gerber, HP, Versatec • Generic NC interface; APT Data; generic assembly interface • Generic ATE interface
Cadisys Corp. 624 E. Evelyn Ave. Sunnyvale, Calif. 94086 (408) 732-1832 Paul Ling Customer Support Manager	**AutoPCB** $1.5k–$7.5k	—	—	•	• PC AT; PC-based network systems; Sun 3/386i (UNIX) • 640-KB main memory and 10-MB hard disk • Mouse or digitizer input; 15″/19″ monitor with EGA, VGA	• AutoSCHEMA (Cadisys); generic interface • CADAT; SPICE; thermal analysis	• Electrical rule checker • Design rule checker • Circuit extractor	• AutoCAD-supported graphics, printers, and plotters • Excellon drill • —

N/s = Not Supplied By Vendor N/a = Not Available

• Initial placement tools • Placement improvement tools	Routing tools	• Max board size • Layer count • Grid sizes	• Schematic libraries • Library support • Package libraries	Surface-mount design support
• Manual and automatic initial preplacement; rat's-nest display • Automatic component, pin, and gate swapping	Signal prerouting; priority, channel routing; compaction; re-entrant; 45°; keep-out zones	• 32″ × 32″ • 64 • Any in 1-mil increments	• CAE interface • New parts can be defined in metric units and mils; new library entries are formed for each package of each device • All typical package types needed for basic design are included.	Flip-flop screen; flip components between sides instantaneously; blind and buried vias
• Manual preplacement; rat's-nest display • Manual reconnection	Signal prerouting; proprietary routing algorithm; re-entrant; 45° routing; keep-out zones; maze routing	• 32″ × 32″ • Now 19 layers: 6 signal, 1 power, 1 ground, 2 silkscreen, 2 assembly, 2 solder mask, 1 keep-out, 1 board outline, 1 connection, 1 title layer, 1 drill drawing • Any in 1-mil increments	• Analog, 1500 schematic symbols; digital, 1675 schematic symbols (in 15 libraries) • New physical parts can be defined graphically; parts can be defined in mils only; new library entries are formed for each package of each device • All typical packages needed, both thru-hole and surface-mount devices	Large SMD library: flip components, dual silkscreen, assembly and solder masks layers
• Manual placement; rat's-nest display • —	Signal prerouting; priority, channel, maze, expert system routing; keep-out zones for wires	• 64″ × 64″ • 50 • 25, 50, 100 mils; fineline; microline; staggered	• Schematic symbols: TTL, 107; ECL, 77; CMOS, 130; analog, 71; discretes, 84; microprocessors, 84 • New physical parts can be defined in metric units and mils; new library entries are formed for each package of each device • Package options: passives, 2; DIPs, 256; SIPs, 256	129 surface-mount schematic symbols and packages (J-lead and gull); blind and buried vias
• Floor planning; dual-sided; minimal crossing count; connectivity; minimum spanning; Z-axis swapping; rubberbanding rat's nest; flexible placement matrices; component orientation; component type differentiation • Interactive and automatic swapping; Z-axis crossing minimization; component alignment	Interactive and automatic maze search with optional display; interactive and automatic squeeze through/shove; auto-stringers; component/connector head start; pattern recognition; interactive and automatic rip-up/re-entrant reroute; intelligent diagonalization; via minimization and manufacturing cleanup; signal prerouting; keep-out zones; copper fill; ECL/high-speed rule adherence; layer polarization; simultaneous multilayer	• 64″ × 64″ • 64 • Any uniform, variable or non-uniform	• Standard packaging • User-extensible multi-user relational DBMS containing electrical, physical and geometric part attributes • Standard package options (pin, gate)	Dual-sided boards with extensive placement, editing, and viewing controls; ASI design service bureau database compatibility and design support
• Min-cut preplacement with user-specified restrictions; rat's-nest display and histograms • Interactive and automatic component, pin, and gate swapping	Signal prerouting; priority, maze, channel re-entrant router on any grid and 1–20 layers; compaction; rip-up; ECL design rules supported; keep-out zones	• Board size function of grid (50″ × 50″ board with 50-mil grid) • 20+ up to 99 signal planes • Any in 1-mil increments	• Schematic symbols: discrete, 6500; digital, 2800; ANSI, 1200 • New physical parts can be defined in metric units and mils; schematic and physical libraries are separate • Package options: DIPs, 30; SMDs, 30; analog, 60	Blind and buried vias; front and back surface mount; interactive swapping of components between sides
• Interactive; rat's-nest display; prompting under three strategies • —	Manual and automatic signal prerouting; memory bus router; hybrid channel/maze router; daisy-chain routing for ECL; compaction; re-entrant; 45° routing; keep-out zones for wires and vias	• 60″ × 60″ • No specified limit (24 auto routing plus 5 power) • Gridless system, 1 mil increments	• Schematic symbols: TTL, 3700; CMOS, 300; ECL, 350; analog, 400; PALs, 25; microprocessors, 35; connectors, 130 • New physical parts can be defined in English or metric units; some physical parts may be defined in the library • Package options: DIPs, 13; TOs, 10; DOs, 10; SMDs, 10; connectors, 130; cases, 5	SMD footprints; blind and buried vias; components both sides of PCB

Directory of Printed Circuit Board Layout Systems (continued)

Vendor Contact	System name, typical cost	Mainframe	Workstation	Software only	Hardware environment • System support • Memory support • Graphics support	• Design entry • Simulation	• ERC • DRC • Extraction	Output formats • Printer/plotter • Assembler • Tester; other
Cadnetix Corp. 5757 Central Ave. Boulder, Colo. 80301 (303) 444-8075 Greg Skomp Manager of Marketing and Communications	**CDX-50,000S** $69.9k **CDX-5000S** $54k **CDX-56,000SP** $89.9k	—	•	•	• Sun (UNIX); Ethernet • 4-24-MB main memory and 141-327-MB formatted hard disk • Mouse, keyboard input; bit-slice graphics processor; 19″ color monitor with 1024 × 800 resolution	• Mentor, Scicards, Valid, FutureNet interfaces, and EDIF • CDX digital design environment; enhanced SABER circuit simulator; simulation accelerator; physical modelor	• Electrical rule checker (on-line and batch) • Design rule checker (on-line with ECL applications) • Complete board fabrication outputs, netlist	• Calcomp, Gerber, HI, HP-GL • Excellon; Amistar, Dynapert, Universal; EDIF, IGES, IPC-350, DQL • Ditmco, Factron, GenRad, Integr-Test, Marconi, ATG interfaces, HP 3065
CAD Software Inc. Box 1142 Suite 6 Littleton, Mass. 01460 (617) 486-9521 N. Marsh	**PADS-PCB** $1k–$2.9k	—	—	•	• PC AT, 386, PS/2 • 512–640-KB main memory and 10–20-MB hard disk • Mouse input; 12″ or 19″ display with EGA or GEM	• PADS-CAE • —	• Schematic vs. layout, Air Gap • Batch design rule checker • —	• Gerber, HI, HP, and generic matrix plotter interface • Excellon • —
Calay Systems Inc. 16842 Von Karman Rd. Suite 100 Irvine, Calif. 92714 (714) 863-1700 Nancy J. Nykanen Marcomm Manager	**PRISMA** Contact Vendor for cost	—	•	—	• Sun Microsystems • 327-MB • 8-MB	• Case, Daisy, FutureNet, Mentor, PCAD, Viewlogic interfaces • PACIFIC NUMERIX	• On-line electrical rule checker • Batch design rule checker; ECL checker • —	• Calcomp CC907, Gerber 4000, HP-GL • Excellon, Trudrill, generic drill interface; Fuji, Panasonic pick-and-place; Dynapert, Universal interfaces • GenRad, Zehntel interfaces
Computamation Systems Ltd. 40 Lake St. Leighton Buzzard Bedfordshire LU7 8RX England Phone: (0525) 378939 J. Yelland	**VUTRAX** $280–$6k	—	—	•	• PC AT, 386, PS/2 • 512–640-KB main memory and 10–20-MB hard disk • Mouse or digitizer input; single or dual screen; EGA, Metheus, Galaxy, CCG graphics	• VULTRAX SCH. • 1/F to PSPICE.	• — • Logical and physical-design rule checker • —	• Gerber, DMP, HP-GL, HI • Roland Emma, HP Laser, Excellon • —
Computervision Corp. 100 Crosby Dr. Bedford, Mass. 01734 (617) 275-1800 Barry Heller Manager, Electronic Product Marketing	**Autoboard SMT CADDstation System** $52.9k	—	•	—	•68020 (UNIX); Ethernet TCP/IP, NFS • 8–32-MB main memory, 170-MB hard disks, and 280-MB 8″ SMD drive • Mouse, keyboard; 19″ display size with 1152 × 900 × 8 resolution	• Schematic Design (Computervision) • CADAT logic simulation (HHB Systems); SABER circuit simulation (Analogy Inc.); thermal analysis (Pacific Numerix); HILO-3 (GenRad); SPICE 2G.6	• On-line ERC • On-line/batch DRC • Keep in/keep out zones supported	• Gerber, Quest, Benson, Calcomp, Versatec, Hewlett-Packard • Excellon, Posalaz, Siemens • Marconi, Panasonic, Universal
Control Data Corp. 8100 34th Ave. South P.O. Box 0 Minneapolis, Minn. 55440 (612) 853-8390 John W. Barnes	**ICEM Electronics** $14k–$75k	•	•	•	• PC/XT, (MS-DOS); Cyber 910, (UNIX); TCP/IP • 640-KB main memory and 4-MB hard disk (PC XT); 30-MB main memory and 70-MB hard disk (Cyber) • Mouse input; 12″/17″ monitor with 1024 × 700 × 8 resolution	• ED-Schematics, ICEM DDN (CDC) • SALT (The CAD Group); ASPEC (CDC); SYSCAP (CDC)	• Batch electrical rule checker (CDC) • On-line and batch layout rule checker (CDC); keep-out zones supported • Two way transfer to 3D drafting for packaging and mechanical analysis (fit, stress, thermal)	• Calcomp, Gerber, HP, Versatec • Excellon drill; generic NC format • Fairchild, GenRad

N/s = Not Supplied By Vendor N/a = Not Available

• Initial placement • Placement improvement	Routing tools	• Max board size • Layer count • Grid sizes	• Schematic libraries • Library support • Package libraries	Surface-mount design support
• Constructive and min-cut preplacement, netlist-driven; rat's-nest display • Simulated annealing; component, pin, and gate swapping; automatic decoupling capacitor assignment	Signal prerouting; priority, maze, heuristic (for memory arrays), re-entrant router with up to 8 layers on any grid; rip-up; SMT; high-speed layout rule adherence; 45° routing; keep-out zones	• 36″ × 48″ • 24 trace, 24 draft • Any combination of grids on "plastic grid"	• Schematic library: basic, 83 pads, 248 components, 298 shapes; CAE, 699; CAD, 2255 components; 74 TTL, 789; 54 TTL, 791 components; commercial CMOS, 235; military CMOS, 224 components; ECL, 75; advanced functions, 89; physical modeling, 55; ASIC libraries (LSI Logic, VLSI Technology, NEC Electronics, TI, Motorola, Hitachi, NCR, National Semiconductor) • New physical parts can be defined in metric units and mils; separate library entry not required for each package option of each function. • Package options: capacitors, 35; connectors, 23; discretes, 45; DIPs, 21; SIPs, 7; PGAs, 6	Blind and buried vias; alternate shapes, automatic breakout generation
• Matrix; force-directed; rat's-nest display • Component, pin, and gate swapping	Signal prerouting; priority, maze re-entrant multilayer router with 1, 5, 10, 20, 25, or 50 grids; 45° routing; keep-out zones	• 32″ × 32″ • 30 layers • 1–1000 mils in 1-mil increments	• — • Physical parts can be defined • Approximately 1000 parts in 8-128 pins, DIPs, SMDs, and pin-grid arrays	Blind and buried vias; standard and micro-size vias
• Force-directed; min-cut; constructive; proportional-space gridless algorithm; rat's-nest display • —	Optional Hardware acceleration	• 32″ × 32″ • 256 • .00001	• Schematic library: TTL, 1000; memory, 500; device, 250; analog, 350; ECL, 500; Intel, 200; Motorola, 200 • New physical parts can be defined in metric units and mils; new library entries are formed for each package of each device • Package options: rectangular, 28 or 32 pins; small- outline, 8, 14, 16, 20, 24; DIPs, 8, 14, 16, 20, 24, 28, 40; PLCCs, 44 or 68; zigzag, 16 or 20; various discretes, through-holes and connectors	Flip-flip screen; double-sided boards; blind and buried vias, although not automatically
• Initial rat's-nest display • Automatic placement; pin and gate swap facility	Any signal priority multilayer auto router; any grid, 45° routing, keep-out zones, track necking	• 32 × 32 • 16 layer • 1-952 mils in 1-mil increments	• Supplied • Schematic and physical libraries can be defined in mil or metric • DIPs: 4, 8, 16, 20, 22, 24, 28, 40; PLCC: any, SMSO/SMSO2 4-254, any outline user-definable for through or surface mount	Double-sided, solder paste and resist for front and backside, blind and buried vias
• Constructive • Pairwise swapping; automatic pin and gate swapping	Single-layer, layer-pair, and simultaneous multilayer grids are supported; prerouting of signals; re-entrant maze router with extensions to reposition traces and vias; 45° routing; keep-out zones at board and component level	• 39″ × 39″ (999 mm × 999 mm) • 20 signal; 10 power and ground • 1 mil	• — • New physical parts can be defined graphically or in ASCII; parts can be defined in metric units and mils; physical parts are attributes of the schematic or library entries that are formed for each package of each device—hierarchical within library (many components can use same package information) • —	Blind and buried vias, dual-sided design capabilities
• Fully automatic, optimized to minimize congestion and/or force-directed; rat's-nest display • Simulated annealing; automatic component, pin, and gate swapping	Signal prerouting; priority, channel, maze re-entrant layer-pair router; compaction; keep-out zones	• 36″ × 36″ • 20 signal, 40 power ground • 0.1 mil and up	• Schematic libraries: TTL, 1200; CMOS, 500; ECL, 200; Intel/AMD, 200 • New physical parts can be defined in metric units and mils; new library entries are formed for each package of each type • Package options: DIPs, 50; discretes, 100; others, 100	Blind and buried vias

Directory of Printed Circuit Board Layout Systems (continued)

Vendor Contact	System name, typical cost	Mainframe	Workstation	Software only	Hardware environment • System support • Memory support • Graphics support	• Design entry • Simulation	• ERC • DRC • Extraction	Output formats • Printer/plotter • Assembler • Tester; other
Daisy Systems Corp. 700 Middlefield Rd. Mountain View, Calif. 94039 (415) 960-0123 Jerry Harvel Marketing Manager	**Boardmaster STAR Router** $22.5k–$28.5k	Vax	•	•	• 80286, 80386/DNIX, UNIXEthernet, TCP/IP, NFS, Sun 386i • 4–16-MB main memory and 85–475-MB hard disks • Mouse, tablet input; Daisy hardware, bit-map graphics; 15″/19″ monitor with 1024 × 832 × 8 resolution	• DED II, ACE (Daisy) • DLS, MDLS, DSPICE, ADLAB, VLAB (Daisy)	• BoardMaster on-line and batch; layout schematic vs. consistency checker • BoardMaster on-line and batch; keep-out areas • Procedural interface	• Gerber, HP, Printronix, Versatec, Laser • Excellon, Trudrill drill • MultiWire interface, auto assy, ATE
Douglas Electronics Inc. 718 Marina San Leandro, Calif. 94577 (415) 483-8770 Dana Dotson Marketing Manager	**Douglas CAD/CAM** $3k (Also available from Bishop Graphics)	—	—	•	• Apple Macintosh Plus/SE, Mac II; Apple Talk local-area network • 1-MB main memory; 400-KB disk drive; hard disk optional • Keyboard, tablet, mouse input; Apple monitor	• Schematic • Digital simulation included	• — • — • —	• Gerber; HI; HP-GL; ImageWriter, Laser-Writer • Excellon • —
Hewlett-Packard Co. 19310 Pruneridge Ave. Bldg. 49AV Cupertino, Calif. 95104-9826 (800) 752-0900 Customer Information Center	**HP Printed Circuit Design System (HP PCDS)** $59k–$95.5k	—	•	—	• HP300 + HP-UX; HP800 Server; IEEE-802.3 LAN • 8-MB main memory and 152–571-MB hard disk • Mouse and tablet input; bit-mapped video bit-slice accelerator; 16″, 19″ monitor with 1280 × 1024 × 8 resolution	• Design Capture System (HP) • Design Verification System, fault simulator, HICHIP hardware modeling system (HP)	• On-line and batch electrical rule checker (HP) • Design rule checker (HP) • —	• HP-GL • Excellon, Trudrill, generic drill interfaces; generic pick and place interfaces; ACI • HP3065 board test family; EDIF, IGES, GERBER interfaces
IBM Corp. 1503 LBJ Freeway 6th Floor Dallas, Tex. 75234 (214) 406-7518 C.W. Liles CAD/CAM/CAE Marketing Programs Manager	**Circuit Board Design System (CBDS)** $22k–$27.3k (software only)	•	•	•	• System 370 architecture (9370, 43XX, 30XX) and RT System • System 370: 8-MB main memory and 50-MB user hard disk; RT System: 8–16-MB main memory and 70-MB user hard disk • Mouse, keyboard input; 5080 monitor (1024 × 1024)	• LOKI, netlist inputs • HILO-3, HSPICE	• — • On-line design rule checker • Netlist extraction	• Gerber G7000E • Excellon, Neutral, Trudrill, standard insertion • Fairchild, GenRad interfaces
Interactive CAD Systems 2352 Rambo Court Santa Clara, Calif. 95054 (408) 970-0852 Eddy Ozomaro President	**PROCAD Xtra** $600–$1.5k	—	—	•	• PC/XT, AT • 640-KB main memory • Mouse, digitizer, joystick input; 19″ monitor with 2048 × 2048 resolution	• Schematic capture included • SILOS, MDL; SPICE, HSPICE, LVS, FutureNet	• ECAD, NCA software • Layout rule checker • —	• Epson, Gerber, HI, HP Laser-Jet, HP-PL, Toshiba • — • —
Intergraph Corp. 1 Madison Industrial Park Huntsville, Ala. 35807 (205) 772-2000 Randy Anderson Product Marketing Manager	**PCB Engineer** $35k–$70k	—	•	—	• Intergraph 100, 200, 300 UNIX workstations, Ethernet network • 6–80-MB main memory and 156-MB–4-GB hard disk • Mouse, digitizer input; 15″/19″ monitor with 1184 × 884 resolution	• Design Engineer or Design Engineer PC • HILO-3; CSPICE, Zycad Mach 1000, and Ikos	• On-line and batch • On-line and batch • EDIF	• Optronics, Gerber, HP, Cal-Comp, and Versatec • Bridgeport, Dynapert, Excellon, Philips, Posalux, Sieb and Meyer, TDK, Trudrill, and Universal • GenRad, Factron/Schlumberger, HP, Marconi, Zehntel, and ES*P; interfaces to wire wrap

N/s = Not Supplied By Vendor N/a = Not Available

• Initial placement • Placement improvement	Routing tools	• Max board size • Layer count • Grid sizes	• Schematic libraries • Library support • Package libraries	Surface-mount design support
• Force-directed; density and/or Manhattan distance is user-definable; fixed-pre-placement; rat's-nest display • Pairwise swapping and multiple swaps with same shape (package), spread and improve	Signal prerouting; priority, costed-maze re-entrant router on up to 16 layers; ECL layout rule adherence; on-line 45° routing; keep-out zones for wires and vias; 45° rip-up and reroute any grid	• 32″ × 32″ • 255 (BoardMaster); 16 signal, 16 power (Star) • Gridless (BoardMaster); 10, 20, 25, 50, 42-16-42, 40-20-40, 40-10-10-40, 42-8-8-42, 38-12-12-38 (Star)	• Schematic symbols: 74TTL, 398; 54TTL, 398; 4000C, 194; 74HC, 203; 54HC, 175; ECL 10K/10KH/100K, 279/215/118; memory, 360; PLAs/PALs, 64; microprocessors, 232; semicustom devices, 54; basic library, 93 • New physical parts can be defined in metric units and mils; new library entries are formed for each package using information extracted from the schematics. • Package options: DIPs, 6–64 pins; SIPs, 8–12; pin-grid arrays, 68–132; discretes, 2–8; all through-hole and SMT	SMT configurations same library as through-hole, blind and buried vias, auto via fan out for SMT
• Manual only, rat's-nest display • —	—	• 32″ × 32″ • 16 routing layers • 1–1000 mils in 1-mil increments	• Schematic libraries: TTL, CMOS, ECL, discrete • New physical parts can be defined in mils only • User-created	Blind and buried vias; user-definable surface-mount devices, placement on both sides of board
• Constructive; force-directed placement by device classification; rat's-nest display, mixed-size placement; two-sided placement; automatic placement grid generation • Force-directed pairwise relaxation; automatic pin and gate swapping	Signal prerouting; maze re-entrant router on 4 layers; 45° routing; keep-out zones for wires and vias; rip-up and re-try routing; adaptive grid routing; autoconnect to buried planes (whole or split)	• 45″ × 45″ (.01 mil resolution), 450 cm × 450 cm (.001 mm resolution) • 128 layers (99 copper) • User-defined grids	• Schematic libraries: TTL, 2698; MOS, 576; ECL, 160; microprocessors and PLDs, 163 • New physical parts can be defined; new library entries are formed for each package of each device • Package options: 9000 total devices including DIPs, SIPs, SOICs, PLDs, discretes	Blind and buried vias; SMD discrete device library; auto-connect to buried planes (whole or split); pad entry specification; primary, secondary board view (flip-screen); placement on both sides of board simul-taneously; routing to off-grid parts; support of metric or English units
• Constructive; force-directed placement with user-specified weights; rat's-nest display • Automatic and interactive component, gate, and pin swapping across windows	Signal prerouting; priority, channel re-entrant router on 4 layers; 45° routing; keep-out zones for wires and vias	• 60″ × 60″ board • 99 layers • 1 mil up	• Schematic symbols: 10,000 elements • New physical parts can be defined in mils only; each symbol requires only one symbol in the database and multiple package versions are defined for it • Package options: DIPs, SIPs, axial, radial, mechanical, pin-grid arrays, SMDs, TAB	Flip-flip screen; double-sided boards; hidden and buried via support; SMD, TAB package libraries; SMT CAM file interfaces and hybrid support
• Manual placement; step and repeat (fixed placement); rat's-nest display with optimization • Pin swapping	Signal prerouting; priority, channel, look-out re-entrant router on up to 25-layer pairs; compaction; some ECL compatibility; 45° routing; keep-out zones	• 64″ × 64″ • Unlimited • 1-mil resolution	• Schematic libraries: TTL, 500; CMOS, 150; linear, 150; other, 50; microprocessors, 300; memories/PLD, 200 • New physical parts can be defined in metric units and mils; new library entries are formed for each package of each device • Package options: DIPs, 20; SIPs, 10; through-hole, 10	Blind and buried vias
• CIP (Constructive Initial Placement) includes "what if" algorithms, force-directed; min-cut with autoplacement on both sides of the board; rat's-nest display generated for minimum length or ECL • Component, pin, gate swapping, and histro-gram	Signal prerouting; priority, channel, maze multilayer; memory; compaction; rip-up and re-route; ECL layout rule; 45° routing from pins and bends; 60° routing for memory	• 64″ × 64″ • 16 • 1/10 mil (.0001)	• 5000 plus TTL, CMOS, ECL, and analog • Physical parts can be defined in metric or mil units; each device may refer to a single physical description • DIPs, SIPs, SMDs, axial; radial; chip carriers	Blind and buried vias; automatic placement on both sides of the board; automatic fan-outs; hybrid support

Directory of Printed Circuit Board Layout Systems (continued)

Vendor Contact	System name, typical cost	Mainframe	Workstation	Software only	Hardware environment • System support • Memory support • Graphics support	• Design entry • Simulation	• ERC • DRC • Extraction	Output formats • Printer/plotter • Assembler • Tester; other
Mentor Graphics Corp. 1940 Zanker Rd. San Jose, Calif. 95112 (408) 436-1500 Jim Behrens Director, PCB Marketing	**BoardStation** $59.7k	—	•	•	• Apollo 3500, 4500 and 10,000 multiprocessor (AEGIS and UNIX); Compute Engine global accelerator; Domain/Idea series DBMS • 4–128-MB main memory and 155–348-MB hard disk • Keyboard, mouse input; 19″ monitor with 1024 × 1280 × 4 resolution	• NETED (Mentor) • QUICKSIM, MSPICE, MSIMON, mixed-mode simulator (Mentor)	• On-line electrical rule checker • On-line design rule checker • Circuit extractor with hierarchical expander; two-way open ASCII database	• Calcomp, Gerber, HP, Versatec • Excellon and Trudrill interfaces • GenRad 227X, Zehntel 850 interfaces
Omation Inc. 1210 East Campbell Rd. Suite 100 Richardson, Tex. 75081 (800) 553-9119 (214) 231-5167 Jackie Williams Marketing Analyst	**SCHEMA-PCB** $975–$2575 **SCHEMA II+** $495	—	—	•	• PC/XT, AT, 386, PS/2 and compatibles; COMPAQ; AT&T and Zenith • 512-640k main memory; 576k expanded memory (LIM); 10/20-MB hard disk • M/S compatible mouse; IBM EGA and VGA NEC GB-1, Video 7, Genoa and Super Genoa, and Paradise	• SCHEMA II+ • SCHEMA-SILOS	• — • Schematic design rule checking before the netlist is loaded to PCB: Floating inputs, nets with no driving source, nets with multiple driving sources, nets with more than one label, nets with a single pin, reference designators used two or more times; PCB DRC: Air Gap and electrical connectivity DRC • —	• Gerber, HI, HP, matrix printers: IBM (5152, proprinter, Pro-XL24), Brother, EPSON (FX, MX, LQ), Okidata (M92, M93, M192, M193, M292, M293), C.ITOH 1550, Toshiba (PS321 and PS341) • Excellon • —
Personal CAD Systems Inc. (P-CAD) 1290 Parkmoor Ave. San Jose, Calif. 95126 (408) 971-1300 Sales Desk	**Master Designer** $8.5k–$14k **Associate Designer** $3.9k–$9.9k	•	—	•	• PC AT (MS-DOS 2.0+) • 640-KB main memory and 20-MB secondary storage. 2-MB LIM • Mouse, digitizer, keyboard inputs; 13″/19″ monitor with CGA, EGA	• PC-CAPS (P-CAD) • LOGS II (P-CAD)	• On-line electrical rule checker • On-line/batch design rule checker • Netlist/circuit extractor	• Bruning, Calcomp, C.Itoh, Epson, HI, HP, IBM-GTCO, Interleaf, Muto, Okidata, Seiko, TI, Gerber, more • Component insertion • NC drill
Racal-Redac Inc. 238 Littleton Rd. Westford, Mass. 01886 (508) 692-4900 Susan Cook Marketing Communications Manager	**VISULA PLUS** $12k–$60k	—	•	•	• Apollo; DEC; Sun; MIPS; Domain, Ethernet, DECnet, NFS • Hardware platform dependent, 4 MB-32 MB • Mouse or keyboard input; 15″/19″ monitor; resolution h/w dependent	• VISULA PLUS design entry • CADAT; SPICE; SABER • Pacific Numerix thermal analysis	• On-line and batch electrical rule checker • On-line batch design rule checker and manufacturing checker • —	• Calcomp, Ferranti, Gerber, HP, Versatec • Universal; Dynapert; Fuji; Excellon • GenRad, Marconi, Zehntel; user-definable outputs
Royal Digital Systems Inc. 2855 Kifer Rd. Santa Clara, Calif. 95050 (408) 970-0909 A.V. Seshadri Vice President, Sales	**Royal Digital Scepter Systems** $25k–$40k	—	•	•	• Silicon Graphics workstations, Sun microsystems workstations, desktop, and file savers • Depends on platform • Depends on platform	• Flexible—supports many popular schematic capture packages • P-SILOS; CADAT; P-SPICE; timing verifier	• On-line and batch electrical rule checker • Design rule checker • Circuit extractor	• Gerber; ASCII; Calcomp pen plotters, HPGL formats • Excellon; Universal; ASCII • Fairchild; Zehntel; Everett Charles; ASCII interface

N/s = Not Supplied By Vendor N/a = Not Available

• Initial placement • Placement improvement	Routing tools	• Max board size • Layer count • Grid sizes	• Schematic libraries • Library support • Package libraries	Surface-mount design support
• Random; constructive; force-directed; two-sided; rat's-nest display • Automatic and interactive component, gate and pin swapping; full automatic analog support; associative placement by area, device or from schematic	Signal prerouting; priority, channel, maze, memory re-entrant layer pair router; compaction simulated through cost controls; ECL layout rule adherence; 45° routing; keep-outs for components, wires, and vias; automatic routing multiple wire widths, shove aside and combination grids	• 100″ × 100″ • 255 layers • Automatic generation of grid from design rules, with 0.1 mil minimum in variable grid range; no limit to pin count or pins per net	• Schematic symbols: 54TTL, 74TTL, 74HC, 54HC, HCT, ECL 10K and 100K, memory, PLDs, PALs, PLAs—3000 • New physical parts can be defined in metric units and mils; symbols are automatically packaged during layout • Package options: 90	Blind and buried vias; user-definable surface-mount package and land-pattern libraries; simultaneous two-sided placement
• Matrix; force-directed; rat's-nest display • Component, pin, and gate swapping; auto placement	Minimum manual routing 1 mil; 10, 20, 25, 50 autorouting grids; 4 autorouting algorithms (memory, power/ground, horizontal vertical, maze/search algorithm with 8 passes with each pass handling connections in increasing difficulty with the last pass doing via reduce	• 32″ × 32″ • 30 layers • 1-1000 mils in 1-mil increments	• 4800 total; TTL (54 and 74); CMOS (4000 and 7000); ECL (10K and 100K); memory; analog; microprocessors (Intel, Motorola, Zilog, and VLSI); discrete, graphical, IEEE • New physical parts can be generated to the users specifications in both packages. • 3500 parts: 8-128 pin DIPs, SMD, and pin grid array, SIPs	The parts can be placed on the top or bottom layer with the pads distinguished with different colors; blind and buried vias in standard or micro sizes
• Constructive (user-defined lattices); Kernighan-Mathaea min-cut; rat's-nest display, force vectors • Simulated annealing; component and gate swapping, pin swapping	Signal prerouting; priority, maze re-entrant all-layer router; 45° routing; keep-out zones, fine line, analog, interstitial vias, trace hugging	• 64″ × 64″ • 100 layers (including graphics and signal layers) • 1 mil up, 1-mil increments	• Schematic symbols: TTL; CMOS; linear; discrete; electromechanical; Intel microprocessors; Motorola microprocessors; SMT; 6000 + parts • New physical parts can be defined in metric units and mils; physical parts are separate entries • Package options: DIPs, SOICs, SMDs, SIPs, more	Predefined footprints; blind and buried vias; extensive library; two-sided CAM interfaces
• Constructive; force-directed; min-cut; rat's-nest display; placement aids for both sides of board • Simulated annealing; automatic gate and pin swapping	Signal prerouting; 45% memory router; rip-up and retry push-aside router; keep-out areas; high-speed logic router; interactive autorouter	• 5 meters × 5 meters • 50 electrical layers, 200 documentation • User definable in 1/100th-micron increments	• Schematic symbols: TTL, CMOS, ECL, analog, PALS, microprocessors, connectors • New parts can be defined in metric units and mils • Package options: DIPs, SIPs, PGAs, SMDs, axial lead, hybrid dyes, user-definable	User-definable pads; blind and buried vias; auto component mirror; SMT CAM interfaces; auto-placement on both sides; fine-line routing
• Constructive; user-directed; rat's-nest display; expert system derives placement from knowledge base of 100 designs; automatic placement on both sides of board • Component, gate, and pin swapping	Signal prerouting; channel router; finishing router with user-defined window; strategic compaction; ECL layout by net; re-entrant; 45° routing; keep-out zones; post process clearance and circuit verification available	• 32″ × 32″ • 20 signal layers; 256 documentation layers • 1 mil and up in 1-mil increments (76.2 million grids in both X and Y direction), grids can be shown as points or lines in user-specified colors	• Schematic symbols: TTL, 600; LSTTL, 300; CMOS, 700; ECL, 100; analog, 250; LSI, 600; nonpackageable symbol type • New physical parts can be defined in metric units and mils; new library entries are formed for each package of each device • Package options: DIPs, SIPs, SMDs, pin-grid arrays, axial, chip-on-board, hybrids	Surface-mount packages and land-pattern libraries; blind and buried vias; open file format for SMT CAM file interfaces; automatic via depth control; hybrid design support

Directory of Printed Circuit Board Layout Systems (continued)

Vendor Contact	System name, typical cost	Mainframe	Workstation	Software only	Hardware environment • System support • Memory support • Graphics support	• Design entry • Simulation	• ERC • DRC • Extraction	Output formats • Printer/plotter • Assembler • Tester; other
Schlumberger CAD/CAM 4251 Plymouth Rd. P.O. Box 986 Ann Arbor, Mich. 48106 (313) 995-6000 Brian F. Barton Director of Electronics	**Bravo 3** $40k	•	•	•	• VAX (VMS); Sun (UNIX); Applicon Graphicstations; Ethernet, DECNet • 5-MB main memory and 350-MB hard disk • Mouse, tablet input; 19″ Applicon monitor with up to 1536 × 1197 × 8 resolution	• Applicon design capture • CADAT; SPICE	• High-speed electrical rule checker (batch) • Design rule checker • Circuit extractor	• Generic plotter interface • Generic assembly equipment interface • Generic tester interface
Scientific Calculations Inc. 7796 Victor-Mendon Rd. Fishers, N.Y. 14453 (716) 924-9303 Douglas W. Spice Director, Marketing Services	**SCICARDS** $25k–$45k	•	•	•	• VAX (VMS); SC Design Station (UNIX); Ethernet, DECnet; Sun (UNIX) • 6-MB main memory • Mouse, keyboard input; 19″ monitor with up to 1024 × 1024 resolution	• SCIDesign schematic capture • CADAT simulation	• On-line electrical rule checker • On-line design rule checker • —	• Benson, Calcomp, HP, Versatec • Excellon; Universal • GenRad, HP, Tektronix interfaces
Shared Resources Inc. 3047 Orchard Park San Jose, Calif. 95134 (408) 434-0444 Robert Wong Executive Vice President	**Koloa PCB Design System** $50k–$100k	—	—	•	• Elxsi; Multiflow; Prime; IBM 43xx; Apollo; Sun; VAX • 2–4-MB main memory and 70-MB hard disk • Mouse, keyboard input; 15″/19″ monitor with 1280 × 1024 × 4 resolution	• Generic CAE interface • Direct link to AIDA simulator	• On-line and batch electrical rule checker • Correct-by-construction layout	• Calcomp; Gerber; Versatec • Excellon, Trudrill; Universal • Faultfinder; GenRad; HP; Teradyne; Zehntel; Trace, most bare-board testers; Wirewrap
Tanner Research 128 W. Del Mar Blvd. Pasadena, Calif. 91105 (818) 795-1696 David Lipin Product Manager	**L-Edit** $495 **DRC Module** $400	—	—	•	• PC, XT, AT, 386, PS/2, or compatible • 640k • EGA, mouse input	• N/s • N/s	• — • Optional design rule check module • —	• Epson dot matrix, HP-GL, postscript printers and phototypesetters, Gerber • — • —
Teradyne EDA 2141 Landings Dr. Mountain View, Calif. 94043 (415) 962-1440 Steve Chidester PCB Product Manager	(Case Technology) **Vanguard PCB Design System** $5k–$30k	—	•	•	• IBM PC 286, 386, and compatibles; Sun 3/260; MicroVAX 2000/GPX; Ethernet • 4–16-MB main memory and 30–140-MB hard disk • Mouse, keyboard input; EGA; Microfield Graphics monitor with 1280 × 1024 × 8 resolution	• Vanguard (Case) • CADAT; SILOS; SALT; HILO; HSPICE; IG-SPICE; Touchstone; PSPICE; LDS; timing verifier	• Electrical rule checker from menu • Consistency, keep-out checker, parameterizable design rule checker (Case) • —	• Gerber, HP • Excellon drill; Universal pick-and-place; Techno insertion • Zehntel interface

N/s = Not Supplied By Vendor N/a = Not Available

• Initial placement • Placement improvement	Routing tools	• Max board size • Layer count • Grid sizes	• Schematic libraries • Library support • Package libraries	Surface-mount design support
• Constructive and force-directed initial placement; rat's-nest display • Component, pin, and gate swapping	Signal prerouting; channel, maze, priority multilayer router on 5-, 10-, 20-, 25-, 50-, or 100-mil grid; compaction; rip-up; 45° routing; keep-out zones	• Any board size • 32 layers • Manual routing grid on any grid size	• Schematic library: TI TTL, 1882; Motorola STTL, 280; Motorola HCMOS, 99; Intel microprocessors, 92 • New physical parts can be defined in metric units and mils; new library entries are formed for each package of each device • Package options: DIPs, 15; also flat packs, transistors, can-type ICs	User-defined surface-mount land patterns; board can be viewed from any angle; double-sided boards; blind and buried vias
• Force-directed; rat's-nest display • Simulated annealing; component, gate, and pin swapping	Signal prerouting (all sizes); priority, channel, maze re-entrant router; ECL layout rule adherence; 45° routing; keep-out zones; 100% rip-up and retry	• 60″ × 60″ • 32 signal layers • Any from 1 mil up	• Schematic library: user-defined • New physical parts can be defined in metric units and mils • Package options: user-defined	User-defined library for packaging and surface-mount land patterns; blind and buried vias; double-sided boards; SMT CAM file interfaces
• Manual preplacement; rat's-nest display • Placement aids	Priority routing with tuning; channel-like router; automatic trace centering; complete transmission line management; re-entrant; 45° routing; keep-out zones for wires and vias	• 100″ × 100″ • Essentially unlimited • Any grid from 1 μm to 1″; up to 10 wires between pins	• — • New physical parts can be defined in metric units and mils; all attributes come from package library • Package options: all TTL, ECL, and standard VLSI packaging; surface-mount packaging and surface-mount land patterns for most standard components	Flip-flip screen; double-sided boards; hidden and buried via support
• Manual placement; step and repeat; hierarchical design editing • —	N/s	• 65″ by 65″ depending on grid size selected • 65,000 layers • User-defined	• DIP pad library supplied, hierarchical editor makes package library maintenance and generation easy • — • —	N/s
• Ordered by connectivity and user filter; rat's-nest display • —	Signal prerouting; priority, channel, maze multilayer re-entrant router; compaction; rip-up; 45° routing; keep-out zones	• 32″ × 32″ • 20 layers simultaneous in router (it can do 256 layers) • Variable in 1-mil increments	• Schematic symbols: digital, 4000; analog, 500; other, 500 • New physical parts can be defined in mils; new library entries are formed for each package of each device (normally parts are attributes) • Package options: DIPs, SIPs, SMD, analog	Blind and buried vias

Directory of Printed Circuit Board Layout Systems (continued)

Vendor Contact	System name, typical cost	Mainframe	Workstation	Software only	Hardware environment • System support • Memory support • Graphics support	• Design entry • Simulation	• ERC • DRC • Extraction	Output formats • Printer/plotter • Assembler • Tester; other
Valid Logic Systems Inc. 2 Omni Way Chelmsford, Mass. 01824 (508) 256-2300 Katherine Gambino Director, Product Marketing, PCB Division	**ALLEGRO** From $20k	—	—	•	• Sun 3/60, 3/110, 3/260, 4/110, 4/260; No special graphics hardware required; 8-MB memory (min.); 32-MB memory (max.); 19″ color or mono monitor with 1152 × 900 resolution • DEC 3200, 2000, or GPXII workstations running under VMS; 8-MB memory (min.); 32-MB memory (max.) • Ethernet, DECnet networking support; NFS support	• — • ValidSPICE PRECISE circuit simulator (Electrical Engineering Software); ValidSIM behavioral, logic, and switch simulator with timing analysis; TIMEMILL (EPIC Design Technology) mixed-level timing simulator and critical path analyzer; RapidTEST fault simulator	• Electrical continuity checker • Physical design rule checker • Electrical analysis calculator to measure net impedance, capacitance, propagation delay, inductance and resistance on board layouts; wire delay extractor for input to digital simulation; SPICE model extractor for input to analog simulation	• Calcomp; HP; Versatec; Gerber and laser photoplot • Excellon NC drill/route; universal inserters; generic ASCII interfaces can be modified by the user to create other post-processors • CV CADDS 4X mechanical; SDRC IDEAS mechanical; PCB interfaces from SCICARDS, Calay, Redac Maxi, Cadnetix, Calma, Computervision; Intelligent Gerber-in
	ALLEGRO-REVIEW $10k	—	—	•	• Sun 3/60; Sun 4/110; 8-MB memory (min.) • DEC 3200 (VMS) or GPXII; 8-MB memory (min.) • Color or mono	• Same as ALLEGRO	• Continuity checker • Physical design rule checker • Same as ALLEGRO	• Calcomp; HP; Versatec plotter support • — • —
	ALLEGRO-ENGINEER $22k	—	—	•	• Same as ALLEGRO REVIEW	• Same as ALLEGRO	• Same as ALLEGRO REVIEW, plus thermal analysis of PCB layouts; reliability rates of individual components and boards; noise margins and voltage/-temperature threshold shifts	
Vamp Inc. 6753 Selma Ave. Los Angeles, Calif. 90028 (213) 466-5533 J. Soluk Marketing Director	**McCAD EDS-1** $1.5k	—	—	•	• Macintosh, Appletalk • 1–2-MB main memory and 20-MB hard disk • Mouse, digitizer input; 19″ monitor with 1024 × 780 × 8 resolution	• McCAD schematics • McCAD DSIM; circuit simulation under development	• — • — • —	• Apple; HI; HP • Excellon; Allied Linotronic interface • —
Visionics Corp. 343 Gibraltar Dr. Sunnyvale, Calif. 94089 (408) 745-1551 Alex Wellins Director of Marketing	**EE Designer III** $4k	—	—	•	• PC/XT, AT, PS/2 • 640-KB main memory up to 2 MB • Mouse or digitizer input; CGA or EGA monitor, VGA, 1024 × 768, 1280 × 1024	• Visionics schematic capture; interfaces to OrCAD and Omation • Visionics logic and circuit simulation; interfaces to OrCAD and Omation	• Electrical rule checker • Design rule checker • Circuit extractor	• DM-PL; Epson; Gerber; HP-GL, Calcomp • Excellon • —
Wintek Corp. 1801 South St. Lafayette, Ind. 47904 (317) 742-8428 Marcia Borton CAD Sales	**smARTWORK** $2k	—	—	•	• PC/XT, AT (DOS 2.0+) • 512-KB main memory • Mouse input; CGA, EGA, VGA monitor	• Wintek schematic capture • —	• Layout vs. schematic consistency checker • On-line design rule checker • Circuit extractors	• Epson; Gerber; IBM; HI; HP • Excellon; DAC; IPC-NC/349 • —

N/s = Not Supplied By Vendor N/a = Not Available

• Initial placement • Placement improvement	Routing tools	• Max board size • Layer count • Grid sizes	• Schematic libraries • Library support • Package libraries	Surface-mount design support
• Board floorplanning feature supports layout partitioning and better control of placement of critical components; three different placement algorithms are optimized for IC, discrete, and gate array placements; DRC for auto-insertion clearances and height restrictions • Pin and gate swapping	An expert routing system utilizes costed maze, rip-up and retry, and push/shove routines to achieve high completion rates without requiring a hardware accelerator; special routing features are provided for ECL or high-speed nets, including automatic signal scheduling, automatic terminator assignment, and priority, daisy chain routing; routing supports 45° angles and a range of glossing features including trace centering between pins, via minimization, and jog elimination	• Boards as large as 6.8 miles on each side at 1 mil resolution can be supported in a single database • 50 routing layers and unlimited data/drafting layers • Database resolution down to 0.00001 mil; metric and English unit support; regular and non uniform grids supported in any user defined size	• 4000+ TTL, ECL; 30+ PLDs; 60+ memory; 100+ LSI/VLSI; 100+ ASIC design kits; behavioral models from Logic Automation and Quadtree; analog libraries • New physical parts can be defined in metric units and mils; a single device definition can be used for multiple package descriptions • Symbol library contains over 100 package options: DIP, 8–64 pins; SIPs, 6–12; SOICs, 8–24; PLCCs, 20–68; pin-grid arrays, 68–172, 1/4–1-W resistors; capacitors; many connectors	Double-sided boards; automatic blind and buried via selection by router; automatic pin escape generation; automatic test pad insertion for SMD devices; dual sided autoplacement
• Board floorplanning tools allow the engineer to partition the layout; automatic and interactive placement features permit complete or partial placement of critical components • Pin and gate swapping provide for optimization of initial placement	Critical signals can be interactively connected by the engineer, then fixed to prevent changes by the autorouter or layout designer using a complete ALLEGRO design system; after routing, any trace can be electrically analyzed or edited by the engineer using ALLEGRO-REVIEW	• Boards as large as 6.8 miles on each side at 1 mil resolution can be supported in a single database • 50 routing layers and unlimited data/drafting layers • Database resolution down to 0.00001 mil; metric and English units support; regular and nonuniform grids supported in any user-defined size	• 4000+ TTL, ECL; 30+ PLDs; 60+ memory; 100+ LSI/VLSI; 100+ ASIC design kits; behavioral models from Logic Automation and Quadtree; analog libraries • New physical parts can be defined in metric units and mils; a single device definition can be used for multiple package descriptions • Symbol library contains over 100 package options: DIP, 8–64 pins; SIPs, 6–12; SOICs, 8–24; PLCCs, 20–68; pin-grid arrays, 68–172, 1/4–1-W resistors; capacitors; many connectors	Dual-sided automatic placement; blind and buried via support
• Manual only • Rubber banding and rat's-nest display	Signal prerouting; priority routing; compaction; rip-up under development; re-entrant; 45° routing; keep-out zones	• 32″×32″ (manual); 16″×16″ (automatic) • 32 layers • 10, 20, 25, 50, 100, 125, 150, 156, and 200 mils	• Schematic symbols: basic set, optional additional libraries • New physical parts can be defined in metric units and mils; physical parts are attributes of the schematic • Package options: 3000	Double-sided SMT boards; user-definable footprints
• Autoplacement based on board size, density, and routing requirements; rat's-nest display (partial or complete) • Manual component, gate, and pin swapping only	Signal prerouting; priority, channel, maze multilayer router; keep-out zones; 45° routing; window options	• 32″×32″ • 36 layers • 1 mil	• Schematic symbols: TTL, CMOS, ROM, RAM, EPROM, PROM, analog, 200; additional 200-part library available • New physical parts can be defined in metric units and mils • Package types: DIPs, 2; SIPs, 1; discrete, 3; SMD, 1	Surface-mount package included; component mirror, place on any layer
• Manual placement only • —	Signal prerouting; maze layer-pair router; re-entrant; 45° routing; keep-out zones	• 10″×16″ • 2 signal layers, 2 soldermask layers, 1 silkscreen layer • 50-mil grid	• Schematic symbols: TTL, 294; CMOS, 148; ECL, 55; microprocessors, 144; miscellaneous, 74; ladders, 86; borders, 19 • New physical parts can be defined in mils only • Package options: footprints created individually	—

Directory of IC Layout Systems

Company Contact	System name and configuration	Typical cost	Hardware configuration				
			CPU (operating system)	Main memory secondary storage	Graphics processor and memory	Display resolution size	Local-area network
Andrew Tickle Associates 1222 Richardson Ave. Los Altos, Calif. 94022 (415) 965-9540 Andrew Tickle President	**TURBO-CAD** (software only)	$30k– $50k	VAX, PC AT, Silicon Graphics, Sun 3, Sun 4, 386i	Standard host configuration	Standard OEM	Standard OEM	Ethernet
Aptos Systems Corp. 5274 Scotts Valley Dr. Scotts Valley, Calif. 95066 (408) 438-2199 John Roth Product Manager	**ICD One** (software and graphics card) **DeskTop Cell Pro** (software only)	$5200 $750	IBM or Compaq 286, 386 or compatibles	640 KB 20-MB disk minimum 9-track tape	Artist I series controller card EGA	1024 × 768 × 4 19″ EGA monitor	3Com; GDS II interface via PC serial interface or Ethernet
Cadence Design Systems Inc. 555 River Oaks Pkwy. San Jose, Calif. 95134 (408) 943-1234 L. Siegel Manager, Public Relations	**Dracula** (stand-alone workstation or host with attached stations)	$35k– $150k	MicroVAX with VMS or Ultrix; Apollo; Sun; MIPS	16 MB 300 MB plus disk	Apollo, DEC, Sun	1024 × 1024 × 4 1024 × 1024 × 8 15″–19″	Domain, DecNet, Ethernet, TCP/IP
	EDGE: layout, PDV (Physical Design Verification), compactor, place and route SYMBAD: OED, PED, LVS, BPR, FP, SBB	$25k– $150k	DEC (Ultrix, VMS) Apollo (Domain) Sun (UNIX)	8 MB minimum 130 MB plus disk	DEC GPX 8-plane graphics Standard color graphics	864 × 1024 1024 × 1024 910 × 1152	Ethernet, DECnet Ethernet, Domain Ethernet
Control Data Corp. 8100 34th Ave. South Minneapolis, Minn. 55440 (612) 853-5255 R.L. Biggs Marketing Manager	**MIDAS/LAYOUT** (host or cluster controller with attached workstations or graphics terminals)	$250k (soft-ware)	CDC CYBER-180 series (NOS)	8–16 MB 200 MB on line	Apollo processors and/or Orcatech 2000 processor 1 MB	512 × 512, 1024 × 1024 9″–14″	Domain
Daisy Systems Corp. 700 Middlefield Rd. Mountain View, Calif. 94039 (415) 960-6586 Tom Flannery ChipMaster Product Manager	**ChipMaster** (stand-alone workstation) **Advansys ChipMaster System** (stand-alone)	$52k– $64k $56k– $67k	80386/287 (DNIX: UNIX 4.2 BSD enhanced) Sun 386i (UNIX)	8–16 MB, 140–327 MB disk, 60 MB QIC tape (on Sun 386i)	Am29116 bit-slice display controller X-window system on standard graphics h/w	1024 × 832 (× 4 or × 8) 15″ or 19″ 1152 × 900 × 8 19″	Ethernet, TCP/IP, NFS
EEsof Inc. 5795 Lindero Canyon Rd. Westlake Village, Calif. 91362 (818) 991-7530 Sandra Rochowansky Manager of Marketing Communications	**MiCAD II** (software only)	$6.7k– $11k	PC/XT, AT, or compatibles (MS-DOS 3.1) Apollo (Domain IX) Sun (Sun OS) HP (HP-UX) VAX (VMS)	640K plus 2 MB above board 4 Mbyte	CGA, EGA 16 KB for CGA, 128 KB minimum EGA	320 × 200 × 2 (CGA); 640 × 350 × 4 (EGA) 1280 × 1024 × 1 1024 × 800 × 4	Ethernet

N/s = Not Supplied By Vendor N/a = Not Available

I/O formats							Artwork database operations								
GDS I	GDS II	APL 860	APL 870	CIF	PG	EBES	Sizing	Scaling	Boolean	Design-rule checking	Extraction	ERC	Netlist compare	Front-end design tools	Symbolic layout and compaction; module generators
○	●	○	○	●	○	○	○	○	●	GDS I and CIF I/O; batch, on-line	Output during layout synthesis as SPICE netlist with parisitics included	○	●	Logic and circuit synthesis; CMOS transistor-level netlist generation; Silvar-Lisco SDS and CAL-MP interface	Automatic self-compacting layout; cell generation; pad layout; RAM generator; netlist comparison
○	●	○	○	○	○	○	●	●	○	Batch	Connectivity; R and C parameters with circuit elements	●	●	CRITERION I schematic capture; PSPICE circuit simulator	None
○	●	●	○	●	●	●	●	○	●	Batch, incremental, on-line, hierarchical	MOS, bipolar, CMOS connectivity with R and C parameters	●	●	SILOS and HILO (logic and fault simulator), SAGE (circuit simulator), SCOAP (testability analyzer), SPICE and HSPICE (circuit simulator interface), Verilog netlist capability	None
○	●	●	○	●	○	○	●	●	●	Batch, incremental, on-line, hierarchical pattern recognition	Connectivity transistor, R, and C parameters	●	●	Same as above	Full-function polygon editor with symbolic compactor, parameterized cells, procedural language and multiwindow editing
○	●	○	○	○	●	●	○	○	○	Batch, incremental, on-line	Capacitance parameters	●	○	Schematic capture; MIDAS and other logic simulators; SPICE, ASPEC circuit simulators; Gateway test tools	None
○	●	●	○	●	●	●	●	●	●	On-line DRC; batch Dracula II	Connectivity; transistor, R, and C parameters Automatic parameter insertion to simulator	●	●	DED II, ACE schematic capture; DLS logic simulator; DSPICE circuit simulator	None
○	●	○	○	○	○	○	●	●	○	None	Pad patterns for chip and package-mounted devices, thin-film resistors, netlists to layout	○	●	TOUCHSTONE, Libra, and MWSPICE circuit simulators	Automated netlist to layout translation

Directory of IC Layout Systems (continued)

Company Contact	System name and configuration	Typical cost	Hardware configuration				
			CPU (operating system)	Main memory secondary storage	Graphics processor and memory	Display resolution size	Local-area network
Emerald Design Systems Inc. 1043 N. Shoreline Mountain View, Calif. 94043 (415) 965-3300 Bob Greene Sales Manager	**GEMstation SAPPHIRE TURBO-CAD** (stand-alone workstation, host, or cluster controller with attached workstations or graphics terminals, or software only)	$38k (system with software), $45k (RISC system with software)	68020 MIPS, "RISC" UNIX V.3	4–32 MB 72 MB–1.1 GB disk 170 MB–9.6 GB	Silicon Graphics' proprietary Geometry Pipeline Hitachi	1280 × 1024 × 32 1024 × 768 × 32 19″	Ethernet TCP/IP, NFS, XNS
IC Editors Inc. P.O. Box 5938 San Jose, Calif. 95150 (408) 971-2422 Donald Brandshaft President	**ICED** (software only)	$995	PC/XT, AT, or compatible with mouse (MS-DOS 3.X)	640K, uses its own paging ICED pages to disk or EMS memory allowing up to 16 Mbytes to be used	EGA card with 128 KB or more RAM	640 × 350 × 8 11″–17″	GDS II and CIF interface via PC serial interface
Integrated Silicon Design Pty. Ltd. 230 North Terrace Adelaide, SA 5000 Australia 61-8-223-5802 A.R. Grasso Technical Manager	**Phase One VLSI Software Suite** (software only) **Phase Two VLSI Software Suite** (software only) **Phase Three VLSI Software Suite** (software only)	Not specified	VAX, MicroVAX, Sun 3/4, Apollo 3000/6000, Hewlett-Packard 9000–300 PC AT/EGA	Not specified	Not specified	Not specified	Not specified
Integrated Silicon Systems Inc. (ISS) P.O. Box 13665 Research Triangle Park, N.C. 27709 (919) 361-5814 Jim Poitras President Roger McPherson Denver, Colo., office (303) 666-0619 Lynda Muns Santa Clara, Calif., office (408) 562-6154	**LTL-100/386** **LTL-100/Sun**	$20k–$30k $20k–$40k	386 Sun	4–16 MB 40–300 MB 8–16 MB 140–560 MB	Proprietary and standard Standard OEM	1024 × 1024 × 4 19″ 1100 × 900 × 8 19″	3COM, Ethernet, Sun, NFS
Intergraph Corp. 1 Madison Industrial Pk. Huntsville, Ala. 35805 (205) 772-2000 Gary Staley Electronics Marketing Engineer	**TANCELL** (stand-alone workstation, or host or cluster controller with attached workstations or graphics terminals)	$65k (work station)	Intergraph's Clipper-based stand-alone workstations (UNIX)	16 MB 150 MB	InterPro 32c 4 MB	1184 × 884 15″, 19″	IEEE-802.3 (Ethernet)

N/s = Not Supplied By Vendor N/a = Not Available

I/O formats							Artwork database operations								
GDS I	GDS II	APL 860	APL 870	CIF	PG	EBES	Sizing	Scaling	Boolean	Design-rule checking	Extraction	ERC	Netlist compare	Front-end design tools	Symbolic layout and compaction; module generators
●	●	●	○	●	●	●	●	●	●	JADE "Instant Batch"	Output during layout synthesis as SPICE netlist with parisitics included (TURBO-CAD)	○	●	PC-based schematic capture; logic synthesis; circuit synthesis; CMOS transistor-level netlist generation; timing analysis; support for Silvar-Lisco's SDS and Cal-MP formats	Automatic, self-compacting layout, design-rule-driven; cell generation from Boolean or transistor descriptions; automatic pad layout; RAM generator; symbolic editor; netlist comparison
○	●	○	○	●	○	○	○	●	○	1st quarter '89 Batch	None	○	○	None	None
○	○	○	○	●	○	○	●	●	○	Interactive; batch (whole design or on a window)	Connectivity, substrate connection, length, width, area of drain and source, perimeter of drain and sources; capacitance: active layers to substrate	●	○	Probe (in-house) full-voltage-current circuit simulation; system simulation and specification	Sticks editor; compaction; cell compilation from netlist
○	●	●	●	●	●	●	●	●	●	Interactive; batch (whole design on an open structure)	Available through C interface	●	●	None	CMOS cell compiler
○	●	○	○	○	○	○	○	○	○	Batch, incremental, on-line	R/C tree interconnect delay analysis, back annotation	●	●	Schematic capture: Intergraph Design Engineer, EDIF; logic simulation: HILO-3, TEGAS (TDL), ILOGS/SILOS	Compactor type: batch and interactive

Directory of IC Layout Systems (continued)

Company Contact	System name and configuration	Typical cost	Hardware configuration: CPU (operating system)	Main memory / secondary storage	Graphics processor and memory	Display resolution / size	Local-area network
Matra Design Semiconductor 2895 Northwestern Pkwy. Santa Clara, Calif. 95051 (408) 986-9000 Pradip Madan Vice President, Marketing and Sales	**GATEAID PLUS/PC** (software only)	$945	PC/XT, AT, 386	640 KB min. Hard disk recommended	EGA, CGA, Hercules	640 × 480	None
	GATEAID II (software only)	$95k	VAX 8600, 8650, 11/750, 11/780, or MicroVAX II (VMS)	2 MB (minimum recommended) 200-MB disk	Tektronix 41XX series (or compatible)	640 × 480 × 4	None
Mentor Graphics Corp. 8500 S.W. Creekside Pl. Beaverton, Ore. 97005 (503) 626-7000 Brain Kiernan Director of Corporate Communications	**Chip Station** (stand-alone workstation) **Cell Station** (stand-alone workstation) **Gate Station** (stand-alone workstation)	$50k+	68020/68881 (12–33 MHz) (AEGIS or UNIX BSD 4.2/ System V)	4–32 MB 170-380 MB, 60-MB cartridge tape	Apollo Domain Series or Matrox Enhanced Graphics	1024 × 800 × 4 (DN3000); 1024 × 800 × 8 (DN3500/-DN4500); 1280 × 800 × 8 (Enhanced Graphics)	Domain or Ethernet TCP/IP
MIETEC Raketstraat 62 1130 Brussels, Belgium (32) 2-728-1811 J.Y. Peigne Communications Director	**Made** (host or cluster controller with attached workstations or graphics terminals)	$20k+	VAX 8530, VAX 750, MicroVAX II, VAXStation 2000 (VMS)	5+ MB 140+ MB	GPX, VAXstation 2000, Tektronix	480 × 640 1000 × 1200 19″	LAVC, Ethernet
Schlumberger CAD/CAM 2833 Junction Ave. Suite 200 San Jose, Calif. 95134 (408) 433-4880 Brian Gardner Product Manager	**Bravo 3 VLSI** (stand-alone workstation or host with attached stations)	$115k; $15k (software); $65k (workstation)	VAX (VMS), Sun (UNIX)	Standard VAX and Sun configurations	Proprietary and standard supported	Up to 1536 × 1157 color 19″	DECnet, Ethernet
Scientific Calculations Inc. 7796 Victor-Mendon Rd. P.O. Box H Fishers, N.Y. 14453 (716) 924-9303 David Marini Vice President of Sales	**MEDS** (host with attached stations or software only)	$50k (software)	VAX 11/780, 11/785, 8600, (VMS) MicroVAX II (VMS)	6 MB 500-MB disk 9 MB 213-MB disk	Megatek 7250 and VT100 64 KB	512 × 512 × 4 19″	Ethernet
Silicon Compiler Systems Corp. 2045 Hamilton Ave. San Jose, Calif. 95125 (408) 371-2900 Richard Gordon Marketing Manager (201) 580-0102	**GDT** (software only)	$88k software only	Sun (UNIX); Apollo (Domain IX); DEC (Ultrix)	4 MB minimum 12 MB for a 112K transistor design	Not specified 4 and 8 planes	1152 × 900 1280 × 1024 or 1024 × 864; 8-bit planes Varies; typically 13″, 15″, or 19″	Ethernet, Domain
	Layout	$30k software only	Sun (UNIX); Apollo (Domain IX); DEC (Ultirx)	4–32 MB 70-, 130-, and 474-MB disks 9-track and 20- or 40-MB ¼″ tape	Standard OEM graphics	1024 × 1024 × 8 1024 × 1024 × 4	Ethernet, TCP/IP, Domain

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I/O formats							Artwork database operations								
GDS I	GDS II	APL 860	APL 870	CIF	PG	EBES	Sizing	Scaling	Boolean	Design-rule checking	Extraction	ERC	Netlist compare	Front-end design tools	Symbolic layout and compaction; module generators
○	●	○	○	○	●	○	○	○	●	Batch, on-line (limited)	R and C parameters	●	●	Schematic capture; logic simulation; graphical analyzer; layout extractor; testability program; fault simulator	Sticks editor; user-defined SRAM compilers
○	●	●	○	●	●	●	●	●	●	Batch via Dracula II or III, interactive via Remedi	Transistor type, size, and connectivity: Dracula, R, and C parameters via Dracula	●	●	Schematic capture is NETED; QUICKSIM logic simulator; MSPICE, MSIMON circuit simulators	Device-level editing (Chip Station); connectivity-based editing and compaction (Cell Station); procedural access toolkit for module generation
●	●	○	○	○	○	○	●	●	●	MASKAP; ECAD, batch, on-line	Transistor type, size, and connectivity: MASKAP; ECAD; capacitance	●	●	SDS, ACE, GED schematic capture; logic simulation; circuit simulation; mixed-mode multilevel simulator	PLA, ROM, resistor, RAM, switched-capacitor filter compilers
●	●	●	●	○	●	●	●	●	●	Interactive; ECAD, batch, incremental, hierarchical	Connectivity; transistor, R, and C parameters	●	●	Design capture; logic analysis (based on CADAT); circuit analysis (based on SPICE)	Cell generator runs off a netlist from a schematic
●	●	○	○	○	●	●	○	●	○	(Correct-by-construction approach)	Connectivity	○	○	(User interface)	Interactive symbol editor
○	●	○	○	○	○	○	●	●	○	Batch, on-line, hierarchical	Transistor type, size, connectivity, capacitance, resistance stored in the L database—no extraction necessary	●	○	Interactive schematic and layout editor; mixed-mode analog and digital logic simulator; behavioral-simulation; fault simulation; timing analysis; test vector translation for Sentry and IMS	Mask-level symbolic layout; constraint graph compaction; datapath compiler; CRT controller, core microprocessor; RAM, ROM, PLA, random logic compilers
○	●	○	○	○	○	○	●	●	●	Batch, incremental, on-line, hierarchical	Connectivity; transistor, R, and C parameters	●	●	Schematic capture; mixed-mode simulation including behavioral, gate, switch, circuit, analog	Symbolic layout; automatic layout from circuit constraint graph and vitual grid compaction

Directory of IC Layout Systems (continued)

Company Contact	System name and configuration	Typical cost	Hardware configuration				
			CPU (operating system)	Main memory secondary storage	Graphics processor and memory	Display resolution size	Local-area network
Silvar-Lisco 1080 Marsh Rd. Menlo Park, Calif. 94025 (415) 324-0700 Tony Wainwright Vice President, Marketing	**GARDS** **SCII** **PRINCESS** **DVP** (All: stand-alone workstation, host or cluster controller with attached workstations or graphics terminals, or software only)	\$60k \$60k \$22k \$38k	VAXstation (VMS), IBM (VM/CMS), Apollo (AEGIS), Sun (UNIX)	4–16 MB 70–300-MB disk	Digital GPX and 4125, IBM 5080, Apollo, Sun	1024×1024 910×1152 (Sun) 19″	DECnet, Ethernet, Domain
Tangent Systems Corp. 2840 San Tomas Expwy. Suite 200 Santa Clara, Calif. 95051 (408) 980-0600 Rod Dudzinski Product Manager	**TANCELL** (stand-alone workstation, host or cluster controller with attached workstations or graphics terminals, or software only) **TANGATE** (stand-alone workstation, host or cluster controller with attached workstations or graphics terminals, or software only)	\$65k (work station) N/s	Apollo (Domain), Intergraph InterPro 32C, 220 (UNIX); VAX, GPX (VMS); Sun (UNIX) Intergraph InterPro 32C, 220 (UNIX); VAX, VAXstation (VMS); Sun (UNIX)	16 MB 150 MB 16 MB 150–300 MB	Intergraph InterPro 32C, 220; Apollo DN5xx, DN3000, DN4000; Sun 3, Sun 4 Intergraph InterPro 32C, 220; Apollo DN5xx, DN3000, DN4000; Sun 4	1280×1024 1024×1024 1024×800 1152×900 1280×1024 1024×1024 1024×800 1152×900	Ethernet, Domain, DecNet, TCP/IP Ethernet, Domain, TCP/IP, DecNet
Tanner Research 128 W. Del Mar Blvd. Pasadena, Calif. 91105 (818) 795-1696 David Lipin Product Manager	**L-Edit** **DRC module** **SCPAR module** **CMOS library** Total (software only)	\$495 \$400 \$400 \$100 --- \$1395	PC/XT, AT 386 machine PS/2 or compatible (MS-DOS)	640K	Standard EGA with 256K	EGA 640×380	Any PC board network (e.g. Ethernet, Tops)
Valid Logic Systems Inc. 2820 Orchard Pkwy. San Jose, Calif. 95134 (408) 432-9400 Dirk Wauters Director, IC Product Marketing	**Mask Design System, IC Design System, EDS-111** (stand-alone workstation or software only) **GDSII/3200** (stand-alone workstation)	\$25k+ \$84k	VAXstation II (VMS) Sun (UNIX) Data General MV7800 (ADS/VS)	5 MB 71 MB 5–8 MB 280 MB 4–14 MB 160–320 MB	GPX Sun graphics processor Proprietary bit-slice	1025×864 color 19″ 1152×900 color 19″ 1280×1024×4 19″	DECnet, LAVC, Ethernet TCP/IP NFS, Ethernet TCP/IP Ethernet
VLSI Technology Inc. 1109 McKay Dr. San Jose, Calif. 95131 (408) 434-3000 Bill Murray Tactical Marketing Manager	**VTItools**	\$20k–\$140k	VAX 760-8800, MicroVAX (VMS) Apollo (AEGIS) Sun 3, Sun 4 (UNIX)	16 MB 100 MB	AED or Tektronix 4115, 4125 Standard configurations Standard configurations	1280×767 1280×1024 1024×800 1280×1024 1152×910	DECnet, Ethernet TCP/IP, Domain

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I/O formats							Artwork database operations								
GDS I	GDS II	APL 860	APL 870	CIF	PG	EBES	Sizing	Scaling	Boolean	Design-rule checking	Extraction	ERC	Netlist compare	Front-end design tools	Symbolic layout and compaction; module generators
●	●	●	●	●	●	●	●	●	●	Batch, incremental, on-line, hierarchical	Connectivity; transistor, R, and C parameters	●	●	SDS schematic capture; HELIX (behavioral) and ANDI/SWAP (mixed-mode) simulators; interface to CADAT, HILO, SPICE, and TSSI	Procedural language for module generation (e.g., ROM, RAM, PLA)
○	●	○	○	○	○	○	○	○	○	Batch, incremental, on-line	Full parameter extraction of final routing	●	●	Netlist interface to HILO-3, TEGAS (TDL), SILOS logic simulators, plus EDIF	None
○	●	○	○	○	○	○	○	○	○	Batch, incremental, on-line	Full parameter extraction of interconnect	●	●	Netlist interface LEF; library interface DEF, GDSII	None
○	○	○	○	●	○	○	●	●	●	N/s	N/s	○	○	OrCAD schematic capture	Automatic standard-cell place and route; pad frame generation; pad routing; CMOS standard-cell layout library
●	●	○	●	●	●	●	●	●	●	Batch, incremental, on-line, hierarchical	Connectivity; transistor, R, and C parameters	●	●	ValidGED schematic capture; ValidSIM logic simulator; PRECISE circuit simulator; TIMEMILL switch-level simulator and critical path analyzer	Symbolic interconnect editor, compactor, and floorplanner; placement and routing; MSI/SSI, FIFO, PLA, RAM, ROM, datapath, and other compilers
○	●	○	○	●	○	○	○	○	○	Batch, on-line	Connectivity; transistor and C parameters	●	●	VTIschematic; VTIsim mixed-mode simulator; VLSI Qsim, Daisy and Mentor interfaces	Sticks, composition, autorouting, compaction; RAM, ROM, PLA, multiplier, datapath, and other compilers

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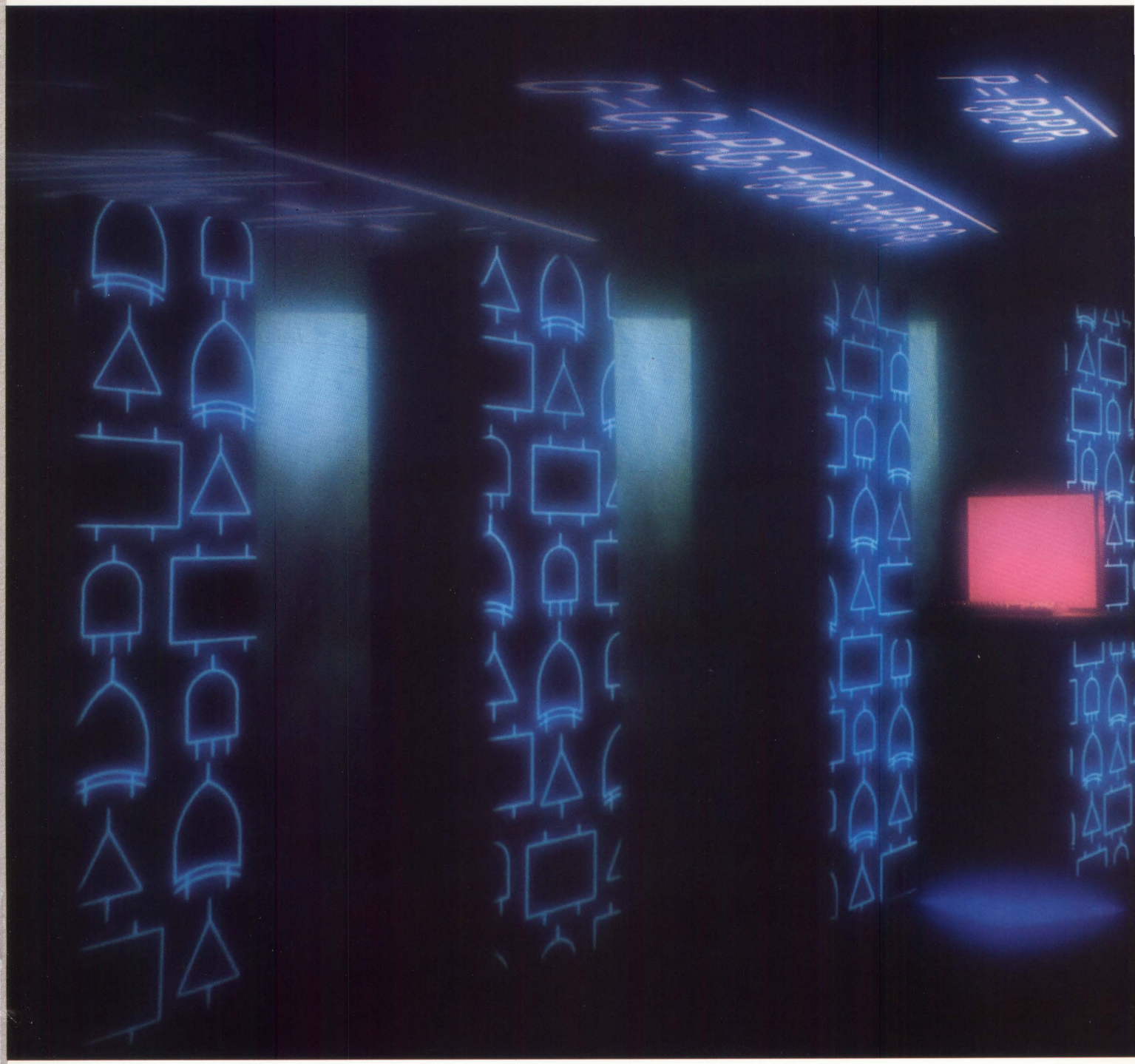

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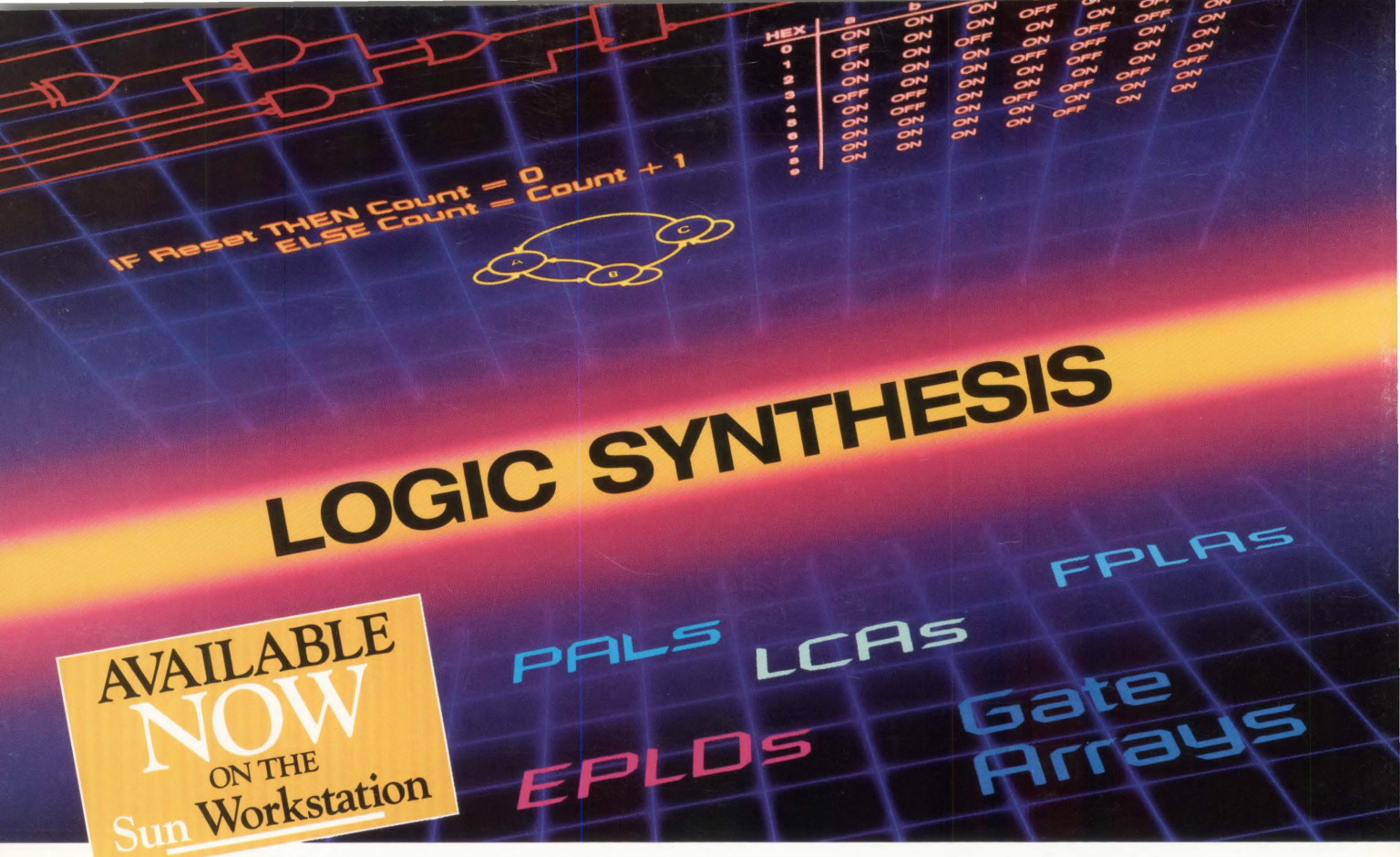

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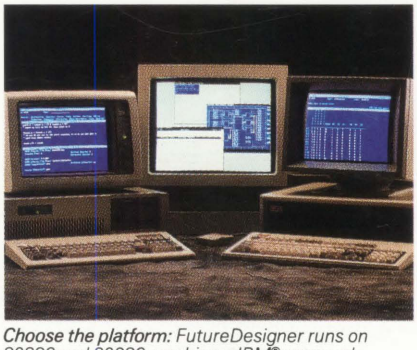

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