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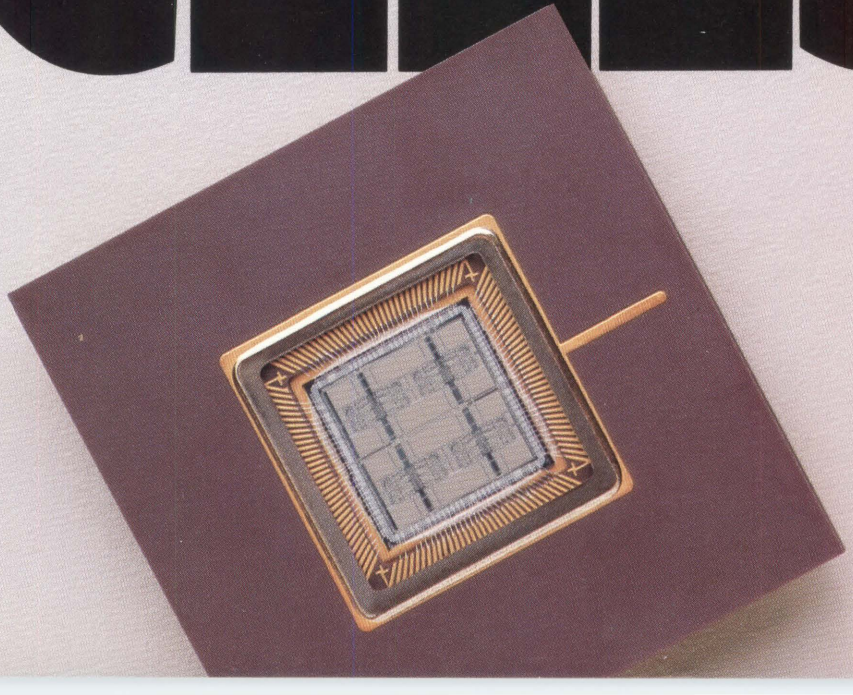

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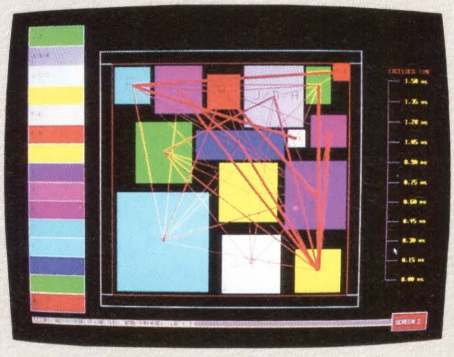

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INTRODUCTION TO THE GUIDE

With the third annual *Semicustom Design Guide*, we continue to provide in-depth technical articles on the range of semicustom IC technologies and the CAE tools and methodologies required to exploit fully those technologies. Backing up the articles are extensive and detailed listings of semicustom vendors, products, and design centers.

Leading off the *Guide* are two articles on state-of-the-art aspects of gate arrays. Next comes an article that approaches the question of semicustom from the point of view of a particular application area—digital signal processing; it argues that, for now, designers are best served by a hybrid approach that includes DSP cores, standard cells, logic synthesis, and silicon compilation (module generation). Then an update covers the recent

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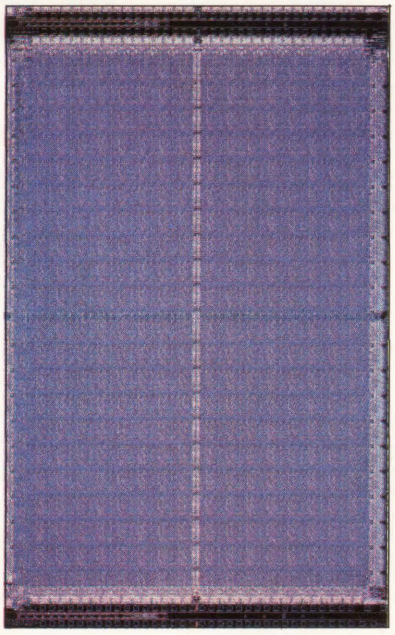
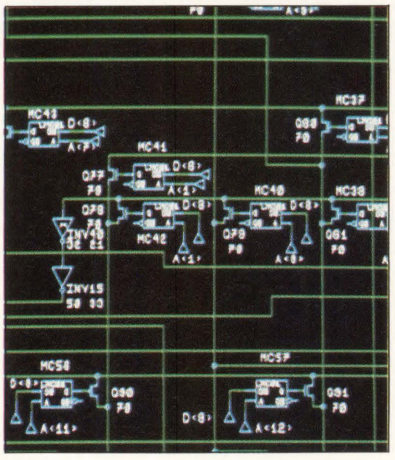
flurry of developments in programmable logic, including "user-programmable gate arrays."

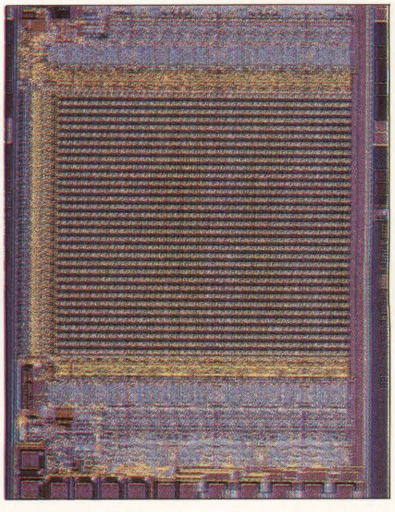
On the tools side, probably nothing has been hotter this year than logic synthesis and VHDL. Section II starts with a consideration of logic synthesis technology embedded in a silicon compilation design system (something that is also touched on in the DSP design article) and a description of the use of VHDL for behavioral description and verification. The following article addresses the need for more accurate timing models for logic simulation, and the last one tackles the problem of developing tests for verifying ASIC prototypes.

We conclude with our set of directories and the 1987 subject index to *VLSI Systems Design*.

— Mike Robinson







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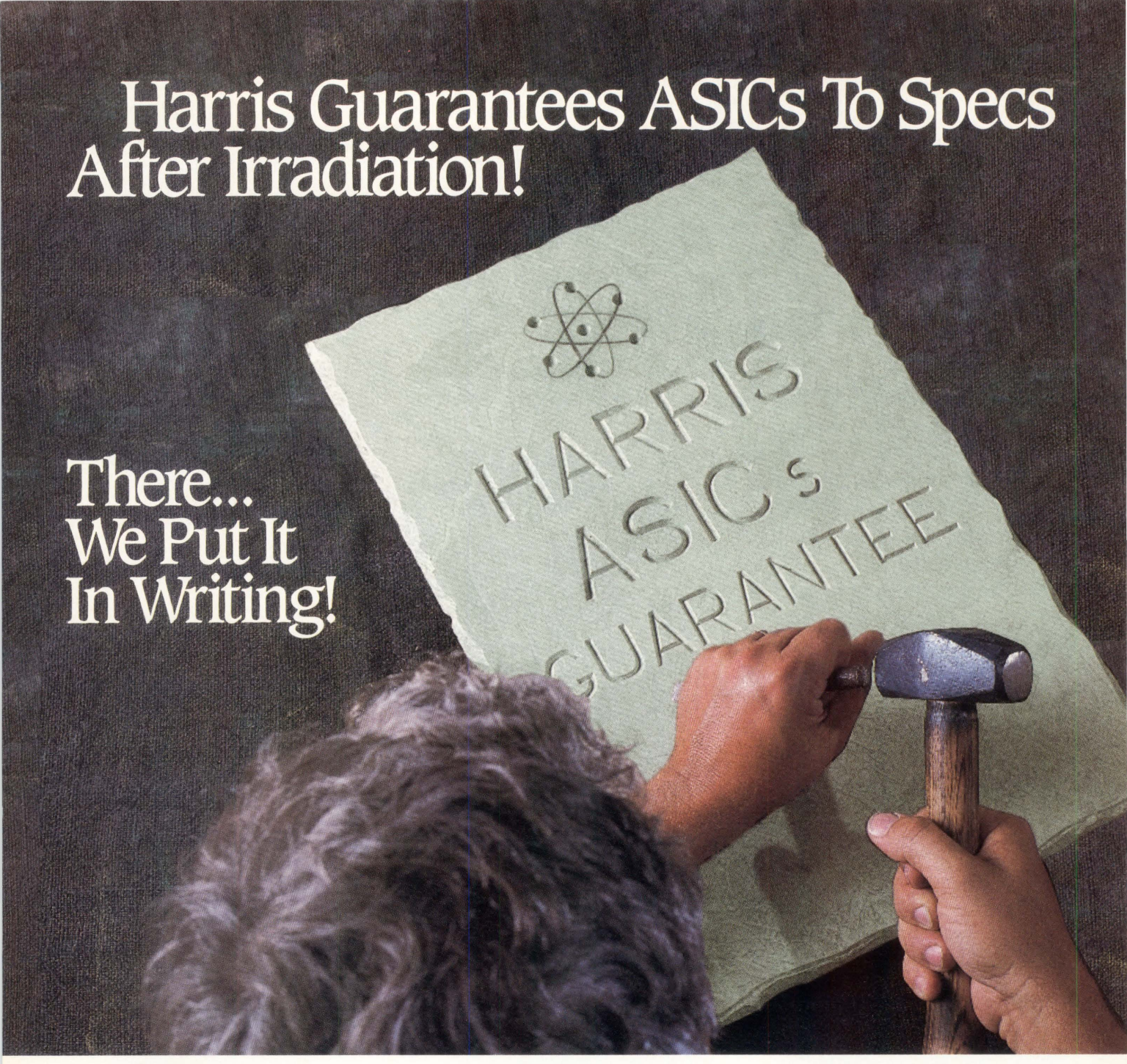

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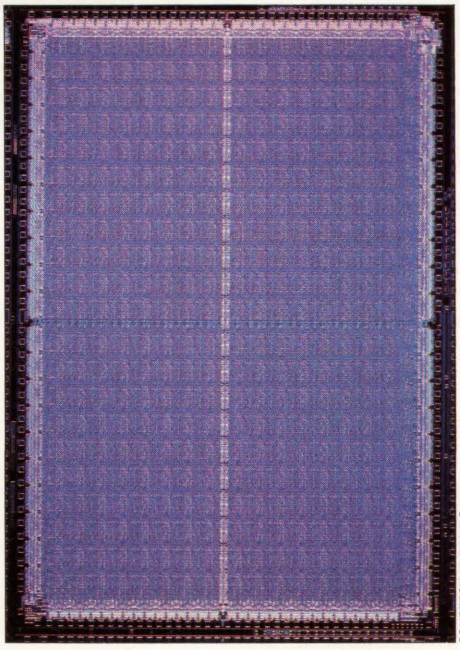

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8 GARNERING THE GATES IN HIGH-DENSITY ARRAYS

Ernest L. Meyer

Changes in gate array technology have opened up new vistas for systems designers who seek high performance and high levels of integration without incurring exorbitant engineering expenses.

24 HIGH-SPEED GATE ARRAYS: CONSIDERING THE OPTIONS

Ron Cates, Vitesse Semiconductor Corp.

To meet the needs of high-performance systems, semicustom designers now have a choice of silicon-based ECL and gallium arsenide, and GaAs has stepped up to enhancement/depletion-mode technology.

32 A HYBRID APPROACH TO APPLICATION-SPECIFIC DSP DESIGN

Howard Moscovitz, AT&T Bell Laboratories

Designers of application-specific DSP integrated circuits have a variety of design alternatives available to them, from traditional schematic capture and standard-cell design to logic synthesis, module generators, data path compilers, and DSP CPU cores. No single tool satisfactorily handles all the applications.

42 PROGRAMMABLE LOGIC UPDATE

Ernest L. Meyer

Recently, a wave of new, improved, and faster programmable logic chips, includer user-programmable gate arrays, were introduced, promising to expand the usefulness of programmable logic technology.

GARNERING THE GATES IN HIGH-DENSITY ARRAYS

Ernest L. Meyer, Campbell, Calif.

The past decade has seen a virtual implosion of IC functionality. Even a gate array can now hold 100,000 two-input NAND gate equivalents—10 times as much integration as was possible even three years ago—and the manufacturing and design innovations for high-density arrays are increasingly counterbalancing the area, performance, and cost barriers traditionally associated with gate array implementation. In addition, those innovations are applicable to all array sizes and are expected to "trickle down."

Two particular techniques are especially significant: the use of triple-level metal (TLM) and the omission of empty wiring channels from the die (channelless, channel-free, or sea-of-gates arrays). With TLM, wires account for proportionally less area and transistor density increases. Parasitic delays are not only smaller on average, but also more predictable. When applied to sea-of-gates array architectures, TLM is yielding utilizations of 90% and higher. However, computer-aided design is not coping easily with these newer technologies. In particular, the increased density and large gate counts intensify the problems of power distribution and critical path constraints. New techniques for placement and routing are being tried out on these very large gate arrays.

TRACKING DOWN THE PROBLEM

Having chosen a semicustom approach, most of the arguments cited against gate arrays arise from their size. Wasted silicon area results from the use of one common base for a number of different functions. Not only might the die size influence final package cost, but also a larger chip will slow down the logic. The less dense the chip, the longer the average wire length. Longer wires add capacitive delays that introduce severe design problems; these problems center not so much on the longest delay, but rather on the range of delays. The impact of die size on performance is particularly strong in gate arrays, where a computer decides the transistor and wire arrangement with algorithms that solve the topological wiring problem, not necessarily the electrical performance problem.

Net lengths display a "right-biased" distribution, with the average net length exceeding the median. Also, the average net length deviates further from the median on the high side as fan-out increases. This distribution poses grim problems for the designer. Simulating with a worst-case delay is highly unrealistic, as only a small number of nets have that delay figure. Especially for high fan-outs, simulating with an average delay may not be much better, because the distribution is skewed to the right. Using a median delay will not allow for the worst-case paths—on one out of ten occasions, approximately, the actual delay will be more than three times the median delay.

High-density arrays are therefore attractive mostly for their advantageous wire delay distribution. The transistors may have much the same speed and the average wire delay may not be much smaller. Even halving the average wire delay does not typically increase speed by more than 10%. However, if the chips are smaller, there are fewer critical paths (whether anticipated or not). Because the longest possible path is now also shorter, there also are fewer restrictions on gate placement and routing. Layout software therefore struggles less to complete the design within the same constraints. In fact, according to manufacturers, the computer time required to complete a high-density array layout is reduced and that reduction more than offsets the costs incurred by the lower yield of a larger die. At the same time, the wiring delays are more predictable, making the technology more attractive to users.

SHRINKING

Shrinking the fabrication process design rules is the most obvious way to reduce a chip's size. However, as transistors shrink below 1.25 μm, the impact of minimum feature size on gate array density becomes much less important. More significant are the minimum wire width and the isolation distance between adjacent wires. Adding these two numbers gives the metal pitch, the minimum possible distance between the centers of two adjacent wires. The pitch can never be as small as the minimum feature size: the transistors and polysilicon wires under the metal track make the surface too bumpy for an even deposition of metal on top (Gulett, 1985)

More recent IC processes use planarization to smooth the surface between each deposited layer. In planarized

processes, the wafers are heated up between metal depositions so that the deposited intermetal dielectric flows and tends to "soften" abrupt steps in the underlying layers, providing a smoother surface for subsequent layers.

Planarized processes make it possible to forge much narrower wires, but if the wires are too small, electromigration can fuse out the metal. In metal migration, excessively high current density causes a gradually accelerating movement of the metal atoms in the direction of the current, until the wire wears out.

Metal migration places a lower limit on metal track width. The dangerous current density for aluminum is about 2 mA/μm^2 of the wire's cross-section. Wires cannot be more than 0.5 μm thick without making the surface too irregular. A typical high-speed process, with a 200-MHz toggle frequency and a 2.5-μA/MHz gate transient current, creates a 0.5-mA drive. A pure aluminum signal wire thus cannot be less than 1 μm wide without self-destructing.

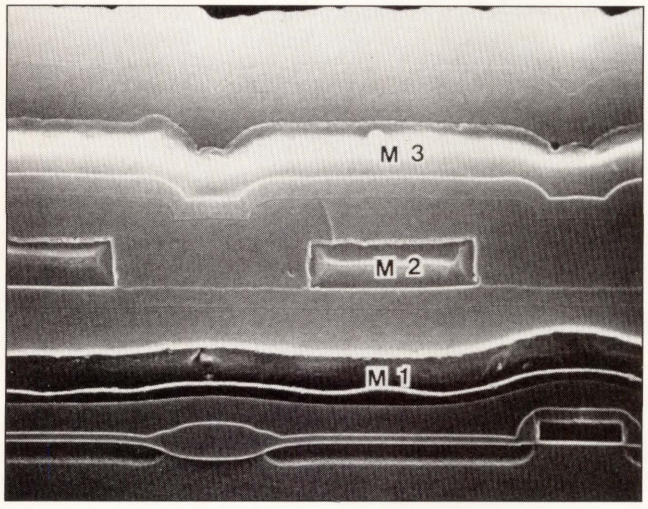

FIGURE 1. The quality of the planarization is shown in a cross section of a Motorola triple-level-metal (TLM) die.

Since it is not possible to compact wires any further in the horizontal direction, vendors are applying the skyscraper principle and going up. Three-level metal (TLM) has been used for power distribution in a number of bipolar processes, in which the pitch of the third metal level has to be much wider than those of the first two levels, because the third metal level is deposited on a surface with even more irregularities.

Fujitsu was the first company to apply the same principle to a CMOS gate array family, using a 4.5-μm pitch on first metal and a 9-μm pitch on the third metal layer with a 1.5-μm process. Fujitsu has been shipping TLM CMOS since 1985.

Shortly after, Hughes Aircraft extended its planarized process to permit the use of 4-μm-wide wires on all three metal layers. In such planarized processes, the reduced metal pitch that is possible on the second and third levels allows even the third level to be used for signal distribution. At about the same time, Toshiba started shipping TLM arrays. Recently, NEC started shipping TLM arrays, with maximums of about 40,000 and 75,000 available gates.

At the time of writing, Motorola has TLM arrays at least in prototype, and Hitachi and LSI Logic are reported to have TLM prototypes. All three companies may have production-quantity TLM arrays by the fourth quarter of this year; Motorola's highly planarized TLM process is shown in Figure 1 . Some other companies, including SGS-Thomson, Texas Instruments, and VLSI Technology, are likely to follow suit.

CHANNELED ARCHITECTURES

Traditionally, gate array bases have been built with separate transistor and wiring areas. In these "channeled" arrays, an empty channel of silicon separates one or two unwired p-n transistor row pairs. The gate array macrocell library then wires up the transistor rows into gates, flip-flops, and larger functions: first-level metal joins up the uncommitted transistors in custom metal patterns over the p-n transistor row diffusion regions. These gates and multigate functions, called hard macros, are the smallest building blocks used by the system designer.

On the same metal level used to wire the uncommitted transistors in the base into hard macros, the hard macros are wired into functions. With a channeled architecture, horizontal wires between the gates are run in first-level metal in the wiring channels between the transistor rows. Vertical wire tracks then run over the horizontal wire channels and p-n transistor rows, on second-level metal. By adding a third metal layer, it is possible to move some of the horizontal wiring tracks from the first metal level to the third, permitting the rows of macros to be moved closer together and thus achieving higher density.

With two layers of metal, it is not feasible to obtain high utilization on a channeled array having more than 20,000 gates. The channels must be increased in width so much that the wire loads become too big. NEC uses three layers of metal to obtain 90% utilization with a channeled array of 40,000 equivalent gates.

SEA-OF-GATES ARRAYS

Whereas TLM attacks the problem of increasing gate density, channelless or sea-of-gates arrays are employed to increase absolute gate counts past the 20,000-gate mark. In these array types, all the wiring channels are removed from the array base. By covering the array base totally with a "sea" of cells or transistors, it is possible to obtain utilizations in excess of 90% for designs with a lot of regular structures (RAM, ROM, and PLA). Array bases that strive for these high gate counts and high utilizations, sometimes called "brick wall" or "puzzle fit" arrays, may be the wave of the future. To obtain the highest utilizations with irregular logic, however, triple-level metal is mandatory.

For example, Tangent Systems laid out an experimental TLM array from Texas Instruments and is reported to have obtained a 99% utilization—without any manual intervention—of over 100,000 gates. Vendors now offering TLM sea-of-gates arrays do not generally quote utilizations as high as sported by TI's CAD benchmark. Hughes does offer 100% utilization for up to 20,000 gates (Hsu et al., 1986), but utilization falls steeply for arrays beyond this level, and in fact Hughes does not sell larger arrays on the commer-

cial market. Motorola is claiming 75% utilization for a prototype 100,000-gate array. Other TLM vendors fall below the half-way mark on utilization; Toshiba, for example, quotes less than 50% (Sawada et al., 1988).

Of course, it is not necessary to have TLM in order to use a sea-of-gates architecture. Sea-of-gates arrays were first introduced in 1982 by California Devices (Lipp, 1983), using double-level metal (DLM). (California Devices has recently been liquidated.)

DLM sea-of-gates CMOS arrays are now available from many vendors, including LSI Logic, SGS-Thomson, S-MOS, and VLSI Technology, as well as from most of the vendors supplying TLM arrays. Note that DLM sea-of-gates arrays that were introduced this year are already obtaining utilizations as high as those of current TLM channelless arrays. For example, SGS-Thomson claims a 60% utilization; VLSI Technology, about a 45% utilization; and LSI Logic, a 40% utilization (T. Wong et al., 1986).

THE UTILIZATION ISSUE

Utilization is one of the hottest issues in array design and is especially so with sea-of-gates architectures. Manufacturers typically indicate the size of an array by the number of two-input NAND gates the array will hold. The size of all other functions is then measured by the number of such gates that could fit in the same area.

This metric introduces the first level of confusion. Macrocells from different vendors can have different numbers of equivalent gates for the same function. The confusion is compounded by whether the equivalence is based on the number of used transistors or on the number of used *cells* (grouped transistors that are electrically isolated from their neighbors). Not all the transistors in a cell may be usable with some functions, and therefore if the quoted figure is for cell utilization, it will be higher than it would be for transistor utilization.

Whatever the case, it is rarely possible to use all the available transistors or cells, even in a channeled array. Leaving some cells unused will reduce wiring congestion. The effect of so-called "depopulated regions" on routability varies from one array (and the CAD system employed for it) to the next. With sea-of-gates arrays and double-level metal, some transistor sites *must* be "depopulated" for the horizontal wiring. Leaving every other row depopulated will reduce the maximum possible utilization to 50%. Vendors quoting a 40%–50% utilization are probably using this technique. Vendors with 30%–40% utilization are probably depopulating *two* rows of gate cells for each macro row used.

One may wonder, why use a sea-of-gates architecture at all if macro rows are regularly depopulated anyway? The answer lies in the use of solid multirow blocks (with no depopulated rows) for regular functions such as RAM, ROM, multipliers, and PLAs. Because these functions are very regular, it is possible to hand-craft building-block modules so that the signal, power, and control port locations directly abut neighboring building blocks. If the constituent building blocks use all the available active devices in the sea of transistors over which they lie, then utilization can be 100% in these areas.

Typical designs usually contain a varying mixture of regular and random logic functions. With a 40% utilization of random logic and a 100% utilization in the regular structures, the final utilization depends heavily on the balance between regular and irregular functions in the specific design.

This discrepancy decreases as more and more rows are populated with logic functionality. The developers of more recent DLM sea-of-gates technologies have concentrated their efforts on designing base gate cells and developing CAD tools that can permit higher utilization, rather than on improving the process and manufacturing technology. SGS-Thomson, for example, is moving toward the depopulation of every third cell row only, allowing a peak 67% utilization for irregular functions. However, this higher utilization is obtained by slightly loosening the cell layout.

A low utilization now does not mean that the array is doomed for all time. The utilization may be low because the array and its library have been designed to be shifted to new processes as they become available. For example, the recent DLM arrays from SGS-Thomson, S-MOS, and VLSI Technology cited above all were designed to yield higher utilization when ported to TLM processes.

Moreover, utilization does not necessarily reflect an array's actual transistor density (number of usable transistors per square mil). Some arrays use base cells that are more spread out, so that the utilization will be higher but the number of transistors per square mil is lower.

BASE CELL DESIGN

The number of rows that must be depopulated to permit routing with the available metal resources depends partly on the base cell design. Transistors can be arranged in various ways inside the transistor rows and can vary in size, isolation technique, shape, and proportion.

Fujitsu, for example, uses two big p-type, two big n-type, and four small n-type transistors in its base cell (Takahashi et al., 1985), as shown in Figure 2a. With logic functions, the four small n-type transistors are not used at all; instead, the space over them is used for wiring channels, yielding a "pseudochanneled" structure with about 13 first-level metal wiring channels between each gate. When the cell is used for RAM, all eight transistors are employed for a single memory bit. This approach yields a high density for RAM but a lower density for logic functions. Fujitsu does not quote utilization figures for its arrays, which is just as well, because any percentage would need to be qualified by the proportions of RAM and logic considered.

Figure 2b shows a more typical base cell design, with all transistors exactly the same size. This particular diagram shows the proportions used in the Hughes arrays. Figure 2c shows a very similar base array cell structure, this one from Motorola, with the transistors wired into a NAND gate. Both these arrays use a basic isolated cell of eight transistors: four p and four n types.

Higher transistor counts can be obtained by removing the dielectric isolation between neighboring cells. Transistors are then tied to the power rails at both ends ("dead" transistors) to provide electrical isolation between neighboring functions. This scheme uses up more area than

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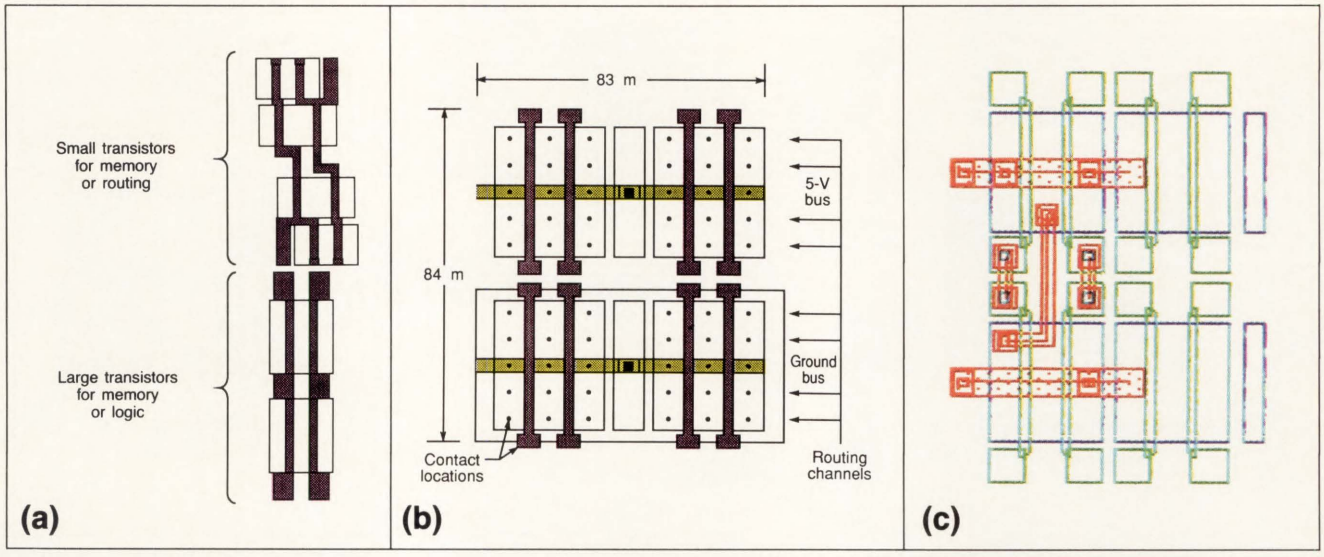

FIGURE 2. Fujitsu's heterogeneous cell (a): the small transistors are either used for ROM or are not used in logic macros, freeing more first-level metal for horizontal wiring. Also shown are standard straight-transistor dielectrically isolated cells, one from Hughes (b) and one configured as a NAND gate, from Motorola's library (c).

conventional dielectric isolation for a single gate, but since it provides flexibility as to where isolation may occur, it can save space when used with large functions. Technically speaking, arrays based on these cell types are true "sea-of-transistor" arrays—sometimes called "continuous" arrays, because each row has a continuous well diffusion; arrays with dielectric isolation are properly "sea-of-gates" arrays. However, these terms are used somewhat loosely. Figure 3 shows a D flip-flop implemented on a continuous array by VLSI Technology.

Note that some vendors include the transistors used for isolation as "utilized" transistors, and some do not. With continuous arrays, therefore, it is worth checking what any particular utilization number really means.

The continuous array example exhibits two further aspects of array cell design: p-n size ratio adjustment and bent (versus straight) gates. The balance between low-to-high and high-to-low transitions is controlled by the ratio of p- to n-transistor sizes. "Transition balancing" is preferable because it makes logic design much simpler.

Bending the gate means that the source, gate, and drain contacts for any one transistor all lie in one column. This innovation by Lipp (1983) facilitates wiring. If the gates are not bent, as in the arrays in Figures 2b and 2c, the gate contact is in a different column from the one containing the source and drain. Therefore, half as many gates can fit in the same number of columns. On the other hand, straight-gate columns are narrower than bent-gate ones, because there is no area wasted in making the wire bend. Straight gates end up slightly wider and slightly shorter.

Since horizontal wiring is the crucial resource, it makes sense to use bent gates for sea-of-gates arrays. Bent gates could be why the DLM arrays from VLSI Technology and SGS-Thomson obtain high utilizations compared with the TLM arrays, which currently all use straight gates.

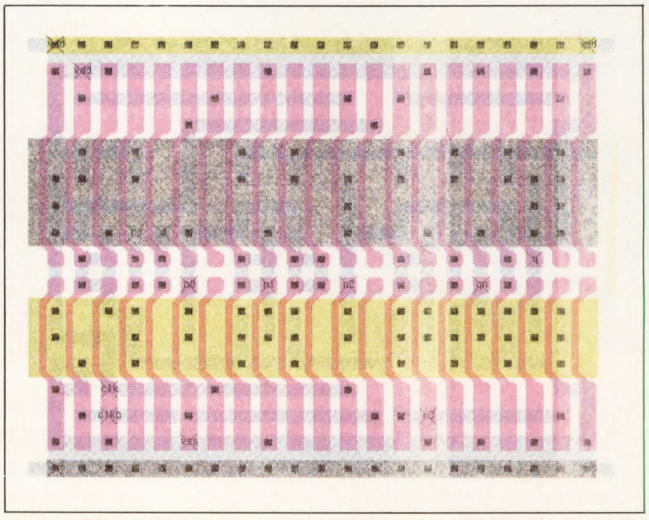

FIGURE 3. A D-type latch in stacked logic from VLSI Technology. Stacked logic and wider base cells permit more horizontal wiring on first-level metal over populated cell sites.

POWER DISTRIBUTION

Power distribution becomes critical as density increases. More transistors are packed into the same area, which means that the power lines may pick up more noise. Most arrays use a fixed power distribution grid (SGS-Thomson's grid is described by Blumberg and Waggoner, 1988). The grid must provide adequate clearance for routing to the underlying macrocells.

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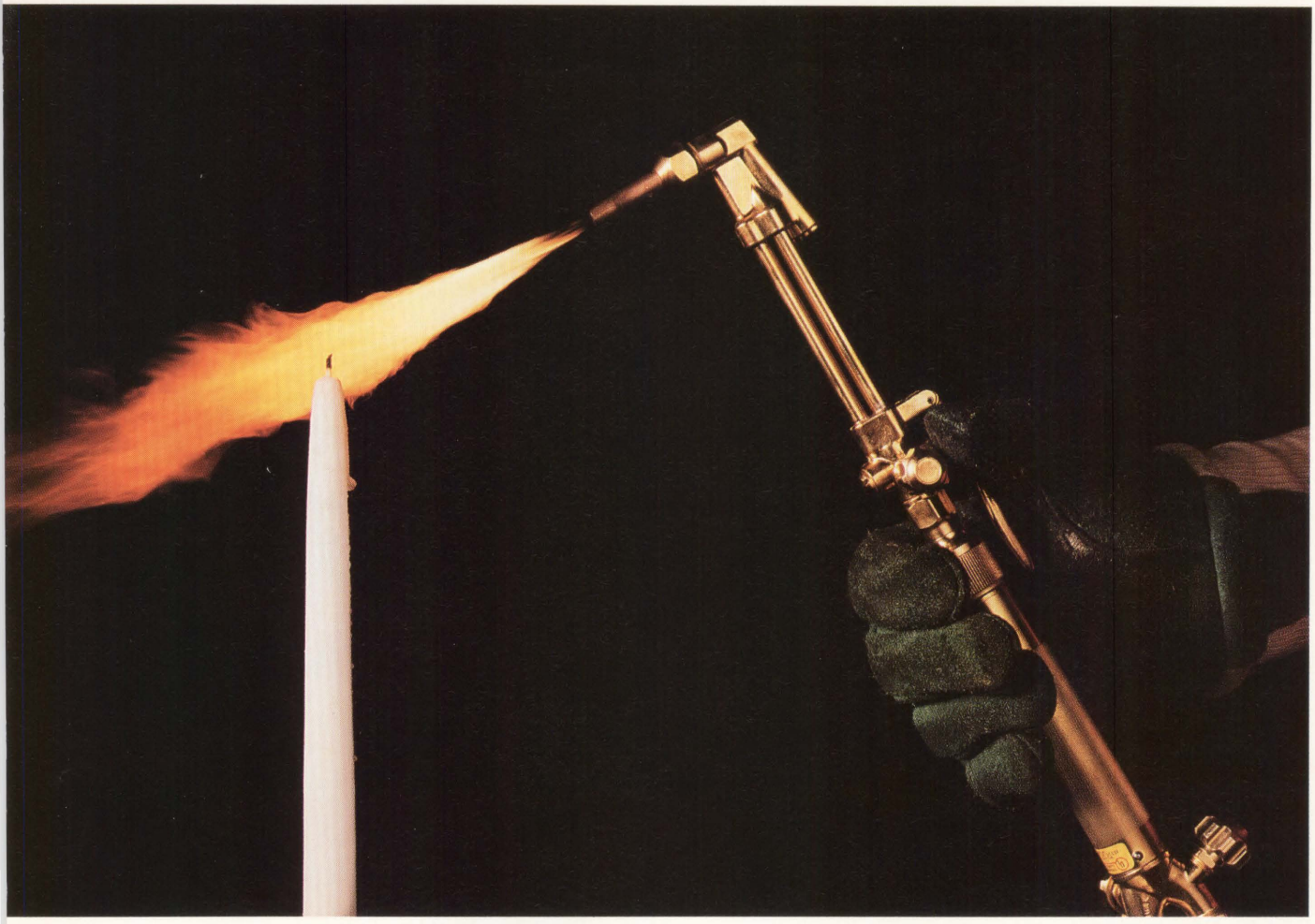

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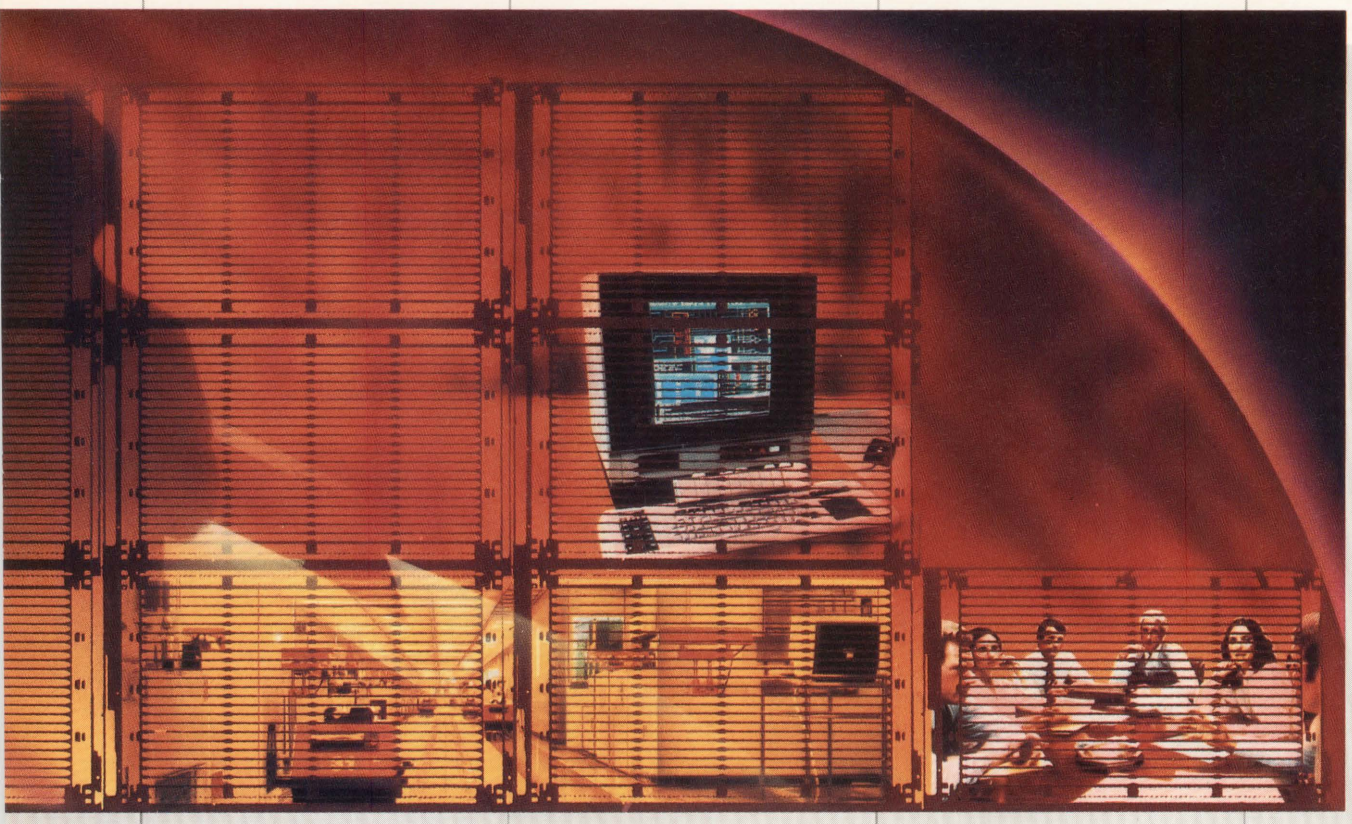

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CIRCLE NUMBER 5

two methods. Some arrays restrict macro placement so that the macro wiring ports do not fall under the power lines, but this approach lowers utilization. Alternatively, cells can be designed with more than one contact location, called "antennas," for each signal port in the macro, but they introduce additional wiring congestion.

The alternative to both methods is to use a flexible power distribution scheme, as advocated by VLSI Technology. This approach is desirable, but it presents a far greater burden on the CAD software, and most current routing systems are not up to the task.

GLOBAL SIGNALS

Heavily loaded paths (clocks and global signals such as resets) are handled in various manners. Hughes, for example, recommends the use of the output driver in an I/O buffer to drive such critical signals into the chip core. This approach yields a high fan-out capability, but the signal source is on the edge of the array, resulting in more clock skew between one side of the array and the other. Balanced clock trees are therefore preferable if more than 20,000 gates are used. On the other hand, tree balancing can use up an appreciable number of gates and is not simple.

LAYOUT

As array size grows beyond about 20,000 gates, further problems are thus imposed on the layout software by the increasingly complex power distribution and critical path constraints. Indeed, as Dan Skilken, product marketing manager, ASIC strategic marketing, at VLSI Technology, says, "The array architecture is built around the router, and not the other way around."

The routing software used for high-density arrays is under continual development by all parties involved and cannot be fairly evaluated by benchmarks. Only three third-party CAD suppliers (Descartes Automation, Silvar-Lisco, and Tangent Systems) are supplying solutions for TLM and channelless arrays.

Descartes Automation is not selling a product but rather advocating a design philosophy and customizing tools in terms of it. "Treating layout software as a standard product does not make sense, because each array has its own characteristics," says Antek Szepieniec, the company's executive vice president. Descartes's experience is that flattened designs lay out better than hierarchical designs. "It is not always the case that hierarchy coming either from the netlist or from min cuts actually groups critical paths together. On the other hand, logical clustering or min cut is difficult to outsmart!" Szepieniec says.

To overcome this problem, placement and routing should take place concurrently. "While performing a placement using an arbitrary partitioning scheme with seeded critical elements, we manipulate the global routing data for wires that cross the partition. This information helps the evaluation of final performance, and if critical lengths are likely to be exceeded, we can reroute these nets at the global level," he explains.

Each block, as it and the routing within it are defined at the global level, is then fully placed and routed. The resulting postlayout wiring delay data for each completed block are then used to create more accurate delay estimates for the remaining design. According to Descartes' experience, this incremental process is very efficient.

Silvar-Lisco is selling a product that uses hierarchy for initial placement. Routing, however, is a back-end process, rather than integrated into the early stages of detailed placement; a conventional min-cut algorithm is used to define the blocks. Critical paths are not confined within block boundaries and so additional placement processing must be performed.

In Silvar-Lisco's scheme, overlapping partitions are used to optimize the placement of critical gates after initial min-cut partitioning. With overlapping partitions, gates placed within the overlap can move anywhere into a neighboring block. Critical gates can therefore move to their optimal position and are not constrained to the block in which they are first placed. Silvar-Lisco's approach can handle up to about 75,000 utilized gates. SGS-Thomson and Digital Equipment use the Silvar-Lisco tools.

Tangent Systems aims to provide a totally automatic solution and 100% routing completion. Placement can be flat, or hierarchy can be used, with "fuzzy" blocks resulting (block size and shape can be changed after initial placement, and functional density within the block can be specified by the system to permit more or less through-block routing as needed). Unlike the case with all other systems, the routing algorithm is not a channel router; instead, it sees "obstructions" in the Manhattan path (a connection with only one corner) and finds the best route around them. Obstructions may comprise existing or predicted routing congestion, as well as elements that are already placed.

The router is also loaded with additional features, such as smart power routing and automatic clock-tree balancing. If power grids are used, they can be automatically altered in type, depending on whether the grid runs over irregular logic or over a modular function such as RAM or ROM. Individual power wires can also be widened automatically when there is no signal wire obstruction.

The automatic clock-tree balancing ensures that the loads are even on each side of the the clock tree by dynamically adding gates during routing.

Tangent's software is being used by, among others, Motorola, S-MOS, and Toshiba. Its present maximum capacity is a quarter of a million gates.

STRUCTURED GATE ARRAYS

Before sea-of-gates arrays acquired their viselike grip on the semicustom market, a number of manufacturers introduced arrays that put a fixed block of memory, a certain-sized multiplier, or a small microcontoller core on the edge of a channelled gate array. This approach, pioneered by IBM and marketed first by LSI Logic as structured gate arrays, can yield greater density improvements for the highly regular functions than sea-of-gates arrays, and the embedded hard macros can be customized for speed.

However, the user is committed to the actual function sizes that are supplied. If anything other than the supplied function size is required, such arrays actually waste space for a small performance improvement. As a result, they

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BIPOLAR

DESCRIPTION	F_t	EMITTER WIDTH	METAL LAYERS
Industry standard	400MHz	14μm	1
High voltage	400MHz	20μm	1
High speed linear	4.5GHz	4μm	2
High speed digital	6GHz	3μm	2
Ultra-high speed	14GHz	0.6μm	3

MOS

PROCESS FAMILY	fCLOCK	MINIMUM FEATURE	VSUPPLY
KC Industry standard CMOS	20MHz	4μm	3-10V
JG Double SiGate NMOS	10MHz	6μm	9-18V
VB High speed CMOS	40MHz	2μm	3-5V
VJ Very fast CMOS	50MHz	1.5μm	3-5V
VQ Ultra fast CMOS	75MHz	1.2μm	3-5V
MH/MA SiGate CMOS	30MHz	4μm	3-15V

BIPOLAR (CDI)

PROCESS	EMITTER WIDTH/ FEATURE SIZE	GRID PITCH	MAX. SPEED	MAX. POWER	MIN. POWER
ORIGINAL CDI	5μm				
CDI FAB I	3.75μm	11.5μm	10ns	2.4pJ	1.5pJ
CDI FAB IIa	2.5μm	8μm	4ns	1.2pJ	0.8pJ
Geometry change (utilizing multi-level differential logic-DML)					
CDI FAB IIb	2.5μm	8μm	800ps	0.8pJ	0.54pJ
CDI FAB III	1.5μm	6μm	400ps	0.4pJ	0.27pJ
CDI FAB IV	1.2μm	4.5μm	200ps	0.2pJ	0.14pJ

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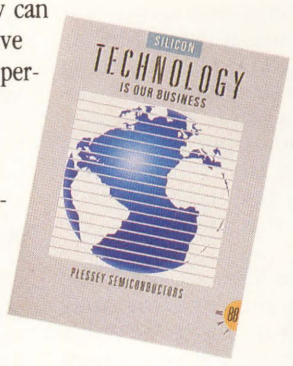

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PLESSEY

Number 1 for ASICs

CIRCLE NUMBER 6

have largely fallen out of favor.

However, with the continuing progression in memory density, structured arrays could be on the way back. An unusual chip from Toshiba integrates a sea-of-gates array with high-density DRAM (Sawada et al., 1988). The chip clocks in with about 30,000 gates available for logic and a whole megabit of 60-ns DRAM. This capacity is two orders of magnitude more memory than offered by any previous structured array and a lot of gates!

To use this phenomenal fusion of function, not more than about 5,000 gates and 32 output drivers can switch at once. As long as these limits are not exceeded, the chip is reported to be fully hardened against noise disturbance.

The combination of sea-of-gates arrays with various high-density memory functions may in fact lead to specialized chips appearing for graphics control, BITBLT processing, cache and memory management, and digital signal processing.

THE FUTURE?

We can expect further improvements in density and the adoption of sea-of-gates techniques in other technologies besides CMOS. LSI Logic has now presented technical data on the first BiCMOS sea-of-gates array, which may be available for prototyping over the next six months (A. Wong et al., 1988). The array will support up to 123,000 gates and departs from the fully integrated BiCMOS array used by Applied Micro Circuits Corp. (Lin and Spehn, 1987). Instead, bipolar drivers are lined up on one edge of the array and used to drive high-fan-out signals into the pure CMOS core. This setup permits adoption of the buffer clock driver technique advocated by Hughes, with less clock skew. At the same time, cells developed for the company's established sea-of-gates arrays can be directly used in the identical CMOS core.

BiCMOS is an important step in part because it permits the integration of analog circuitry with sea-of-gates architectures. Analog circuitry could be used for on-chip power regulation to reduce the switching noise problem. As a result, the arrays could use a lower power supply (perhaps 2.5 or 3 V), which would lower the current density in the metal interconnections, reduce migration effects, and permit the use of submicron-wide wires in planarized DLM processes.

AMCC, which introduced BiCMOS channeled arrays last year, is now developing the first sea-of-gates bipolar array (Coy, Mai, and Yuen, 1988). The chip is being produced using Plessey's HE1 process. Bipolar transistors are more difficult to embed in a sea-of-gates architecture, particularly because of the larger amount of wiring space that must be used to distribute power. Furthermore, the reduction in chip size made possible with sea-of-gates architectures has less impact on performance and predictability for bipolar than for CMOS technology, because wire lengths are less critical. Thus AMCC's movement to a sea of gates for bipolar arrays may be an indication that layout techniques for these chips are generally superior to those offered for traditional channeled approaches, even if only for the savings in chip real estate.

CONCLUSIONS

The advent of high-density arrays heralds the increased feasibility of gate arrays in many applications where before only hand-crafted or standard-cell designs were viable. Of course, triple-level metal and sea-of-gates layout will before long be applied to cell-based design; the implications of those developments are left to future articles. □

Acknowledgments

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About the Author

Ernest Meyer is a free-lance writer and editorial consultant, as well as a contributing writer and columnist for *Supercomputing Review* and *Embedded Systems Programming.* Previously, he was an editor at *VLSI Systems Design.* He has worked on the design of various electronic systems, including an Apple-compatible microcomputer and a music synthesizer.

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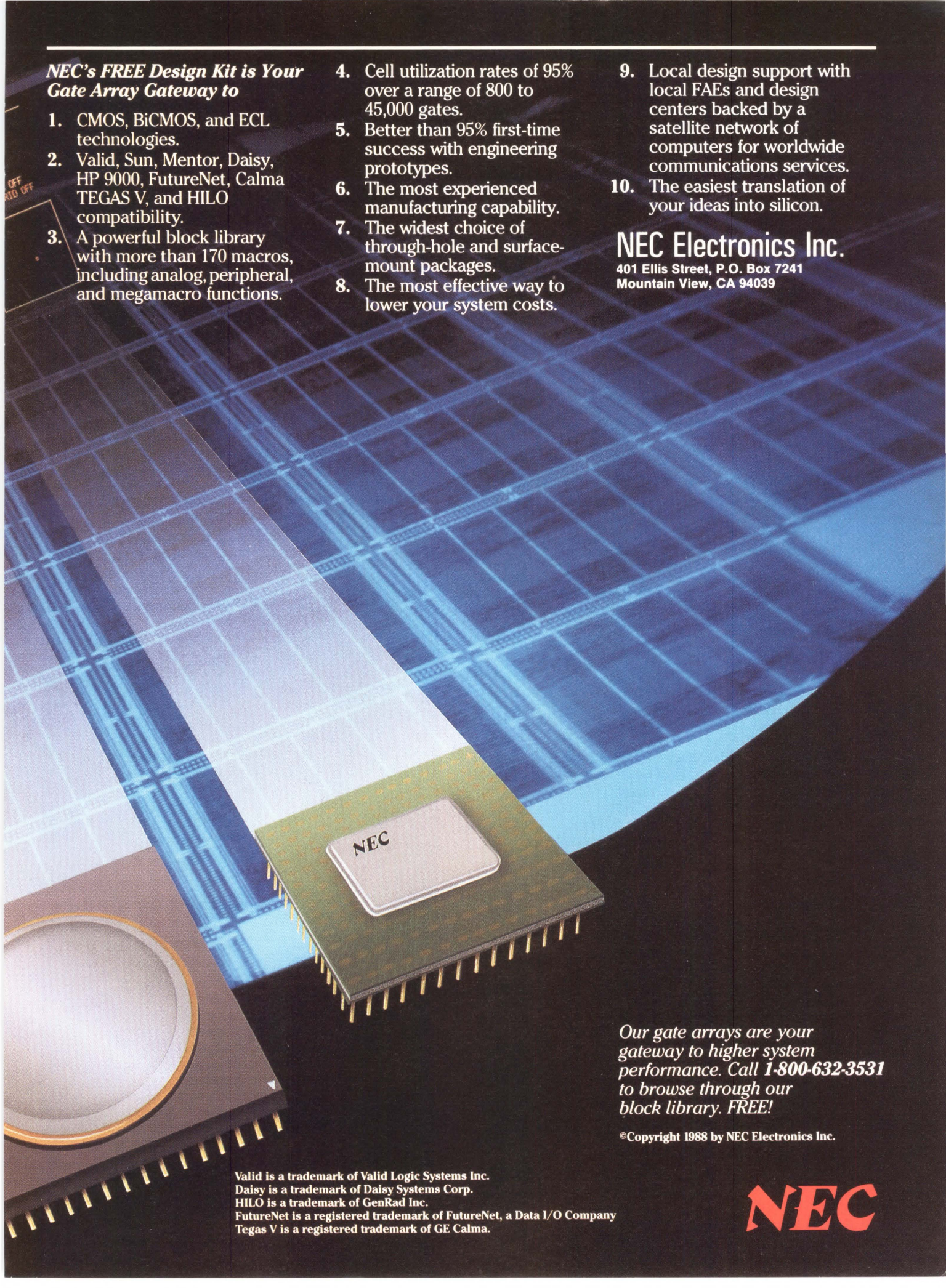

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HIGH-SPEED GATE ARRAYS: CONSIDERING THE OPTIONS

Ron Cates, Vitesse Semiconductor Corp., Camarillo, Calif.

High power dissipation has traditionally been part and parcel of every fast-clocking system, and in many cases it sets the upper bound on the practical density of an integrated circuit. For ICs clocked at less than 50 MHz, CMOS is the obvious choice. It offers an unparalleled combination of circuit complexity and low power dissipation. Digital circuits that operate beyond 50 MHz, however, are needed for many applications—high-performance workstations and computers, telecommunications, and automated test equipment, to name a few. CMOS just does not have the performance for such settings.

Typically, designers turn to bipolar ECL circuits when higher performance is essential. Recently, though, system designers have been given a viable alternative technology for high-speed digital circuits—enhancement/depletion-mode gallium aresenide, or E/D GaAs.

Gate arrays have become a dominant approach to implementing high-performance systems. They offer an opportunity to create a custom component that can meet performance criteria and that involves a minimum of design time and risk. Advanced software tools, usually running on engineering workstations, make it possible to enter the schematic and accurately simulate logic and timing before committing to silicon.

DIFFERENT TOPOLOGIES

To understand the differences between ECL silicon and E/D GaAs, it is useful to review the basic circuit topologies of each. Central to the operation of a typical ECL NOR gate (Figure 1) is the main differential pair (Q_1 and Q_2). V_{REFA} is set at a voltage halfway between a valid logic high and logic low. When digital signals arrive at the base of Q_2 or Q_3, the active device in the differential pair switches state, resulting in a change of voltage across the load resistor (R). Emitter-follower Q_4 shifts the level of that voltage change and buffers it. Q_5 and Q_6, along with their corresponding resistors, act as active current sinks.

The majority of the current consumed by an ECL gate passes through the emitter-follower to drive the interconnect capacitance. To reduce power consumption, advanced ECL gate arrays use a special power supply to supply power to the emitter-followers. Since V_{EF} is typically set at −3.3 V, this approach saves power when compared with gate arrays that tie the emitter-followers to V_{EE}, which is set at −5.2 V.

The simple ECL NOR gate requires six transistors and three resistors, as well as several voltage references that set currents or provide the reference voltage to the differential pair. Typically, these reference generators are shared among several gates. Unfortunately, the metal buses that distribute the reference voltages can increase the size of

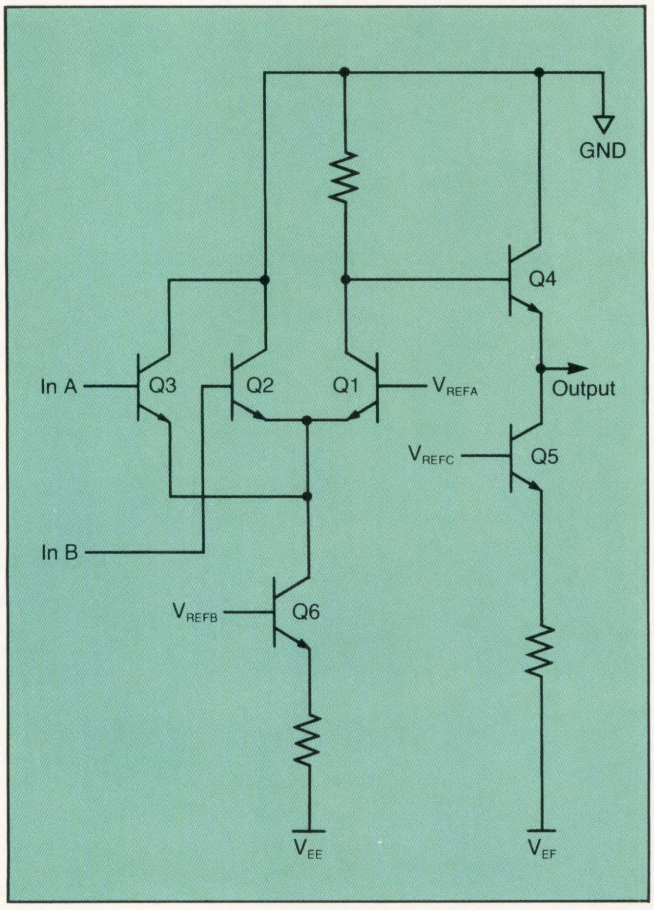

FIGURE 1. A typical two-input ECL NOR gate requires six transistors, three resistors, and several voltage references.

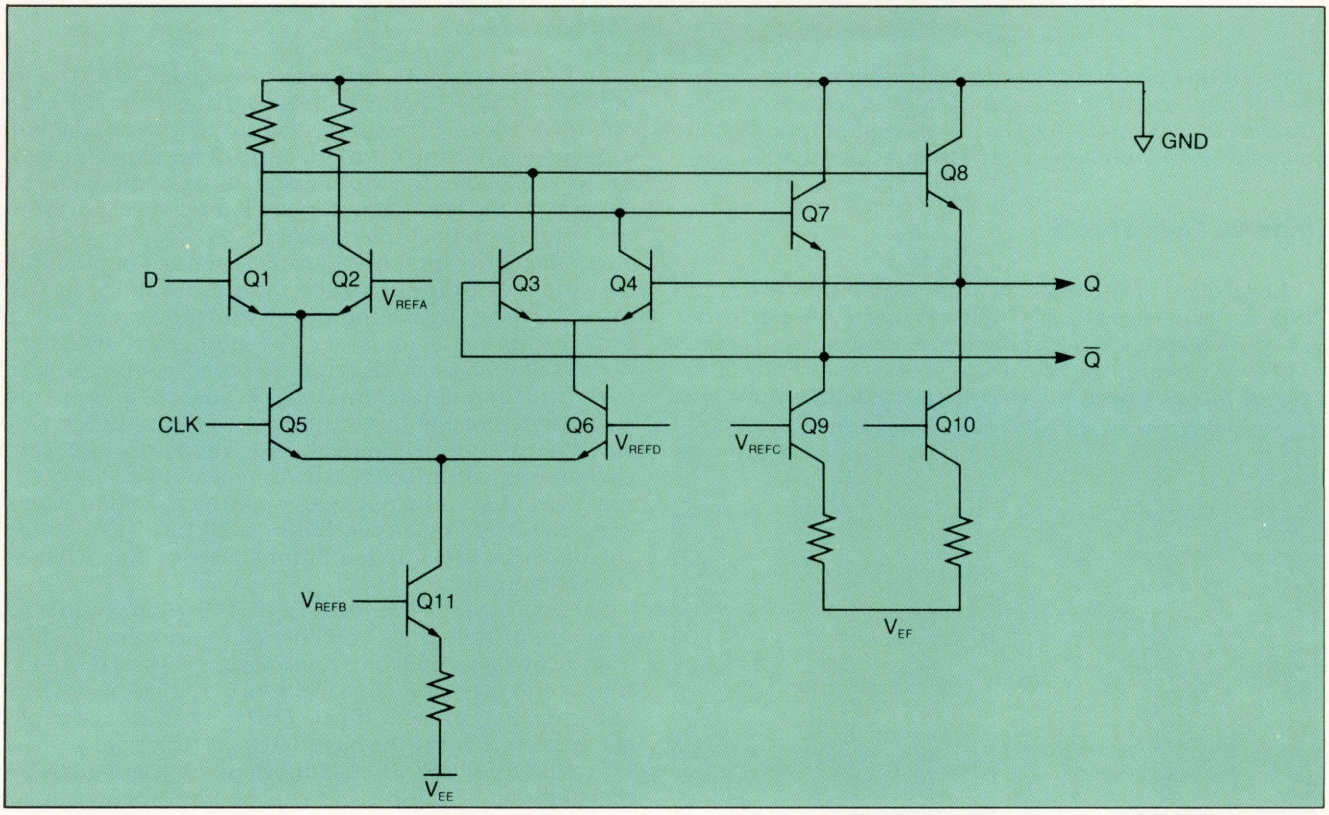

FIGURE 2. Adding "clocking pair" (Q_5 and Q_6) and a "latching pair" (Q_3 and Q_4) to the circuit shown in Figure 1 creates a data latch. Cascading two of these structures results in a D-type edge-triggered flip-flop.

the gate and consume routing resources.

Although the ECL gate looks complex, slight modifications to the basic structure make it configurable to a variety of logic primitives. A data latch is created (Figure 2) by adding a clocking differential pair (Q_5 and Q_6) and a regenerative pair (Q_3 and Q_4). When the clock is high, the input transistor pair amplifies the data input; when the clock is low, the regenerative pair is active, latching the data through feedback from the outputs. Other structures that are similar to this latch use the regenerative transistor pair for logic inputs and capitalize on the vertical gating structure to implement such functions as a 2:1 multiplexer or an exclusive-OR gate. Cascading two latches and cross-wiring the clock inputs creates an edge-triggered D flip-flop.

When compared with the ECL structure, the E/D GaAs gate is very simple. A two-input NOR gate (Figure 3) uses only three transistors and needs no resistors. It uses a depletion-type MESFET (Q_1) as an active-load pull-up device and two enhancement-type MESFETs (Q_2 and Q_3) as pull-down switches. The GaAs gate operates identically to equivalent silicon NMOS structures. Q_2 and Q_3 are large enough so that if one or the other is on, or if both are on, it or they can sink all of the current from Q_1 and provide a small V_{vDS} for a logic-low output. When both enhancement transistors are off, the pull-up current is forced into the forward-biased gate-source junction of the driven gate, providing a logic high.

In the E/D GaAs configuration presented here, the power dissipation of the gate is independent of the logic state that it is in. Because the current on the power supply buses is constant, self-generated noise on the signal and internal

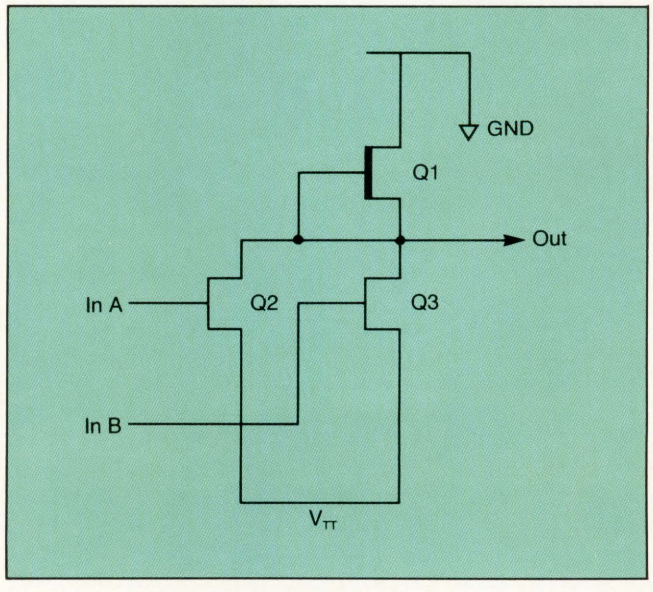

FIGURE 3. A simple two-input E/D GaAs NOR gate uses only three transistors and needs no resistors and no voltage references; it requires a single −2-V power supply.

power buses is virtually eliminated, reducing the need for artificially large noise margins. Reduced voltage swings—such as the 500 mV for E/D GaAs—also simplify high-speed switching and reduce current-drive requirements.

DRIVING CAPACITANCE

Regardless of the material from which they are made, bipolar transistors have a higher transconductance than FETs. As a result, ECL circuits drive long capacitive lines fairly well, exhibiting 50 to 60 ps of delay for every millimeter of interconnect. Driving long capacitive lines with some E/D GaAs circuits, however, is inefficient because the pull-down transistors grow in proportion to the size of the pull-up driver and, therefore, may not provide an adequate capacitive buffering ratio (the ratio of the capacitance of the driven load to the input capacitance of the buffer). If the ratio is too low, the buffer itself introduces excessive capacitance on the input signal.

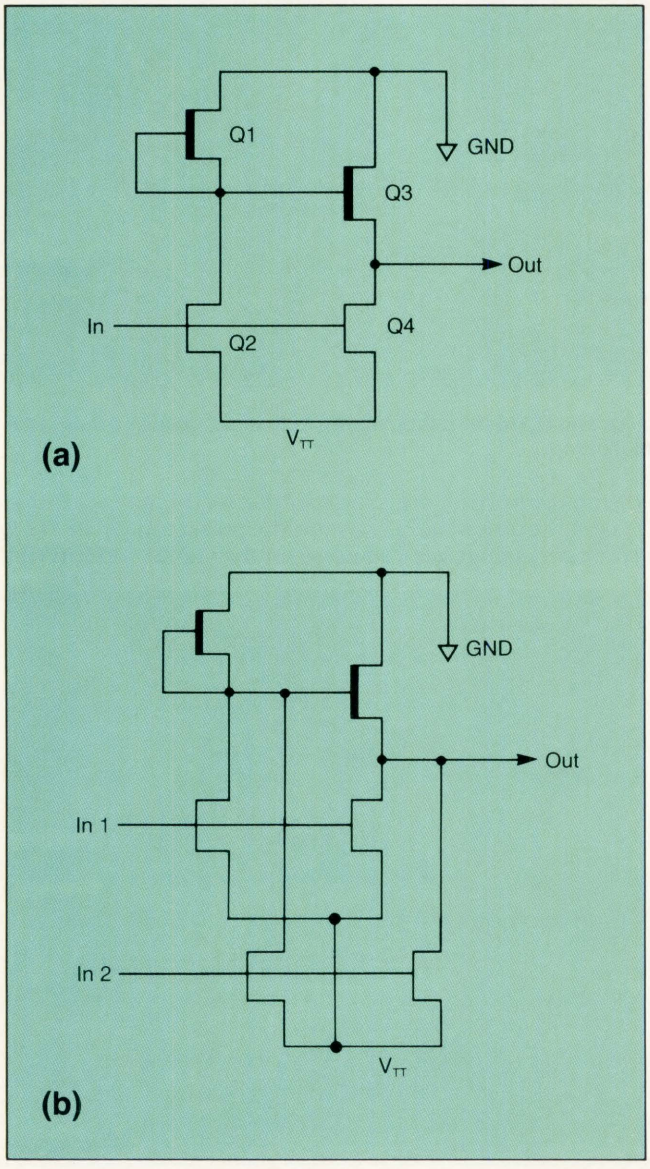

FIGURE 4. An E/D buffer with a push-pull stage (a) can drive a millimeter of wire in 50 ps. Adding a set of pull-down devices converts the buffer into a NOR gate (b).

A buffer skirts this limitation (Figure 4a). The push-pull operation of its output stage enhances its ability to drive capacitive loads by placing a positive bias on the gate of the output pull-up transistor. The pull-down transistor doesn't have to be made larger in order to sink the extra current of the pull-up transistor, because the pull-up transistor's current is enhanced only when the input voltage is low. When the input is high, the gate and source of Q_3 are at the same potential, so that the transistor has a lower current drive. The buffer is capable of driving a millimeter of metal in 50 ps. Logic operations can be incorporated into the buffer by providing additional sets of pull-down devices (Figure 4b).

E/D GaAs is similar to NMOS in that flip-flop circuits are created with NOR gates. Consider two posssible D flip-flops (Figure 5): one would be a typical edge-triggered version; the second uses differential clocks to reduce both set-up and propagation-delay times. Both rely on cross-coupled NOR gates to achieve the basic latching function.

In general, simple digital functions such as logic gates, registers, and multiplexers can be implemented in E/D GaAs with fewer transistors than they would need in ECL. As shown, a flip-flop requires 19 transistors in E/D GaAs but 22 transistors and 10 resistors in an ECL implementation. As a result, much less real estate is required to implement a given function in E/D GaAs. Since they don't require area-consuming resistors, E/D GaAs circuits can achieve densities equivalent to NMOS circuits. A two-input NOR gate, for example, occupies only 100 μm^2.

This density has strong implications for gate arrays. E/D GaAs arrays occupy about one half the area of ECL arrays of equivalent compexity. Metal routes, therefore, are shorter for E/D gate arrays: statistical analysis on automatically routed arrays shows an average route length of 0.3 mm per fan-out load in an E/D GaAs array (from Vitesse's design manual), much shorter than the 0.8 mm per fan-out load in an ECL device (according to Raytheon's *ECL Family Design Manual*).

POWER CONCERNS

No discussion of high-performance circuits would be complete without a careful consideration of power dissipation. High power dissipation has traditionally been associated with every fast-clocking system and, in many cases, it limits the density of an integrated circuit.

ECL circuits have dramatically improved their power dissipation for a given function over the levels of early SSI devices. Today, typical ECL gate power falls between 1 and 4 mW, depending on the speed option that the designer selects. Even at such low values, new 10,000- and 12,000-gate ECL arrays can dissipate as much as 30 W when their

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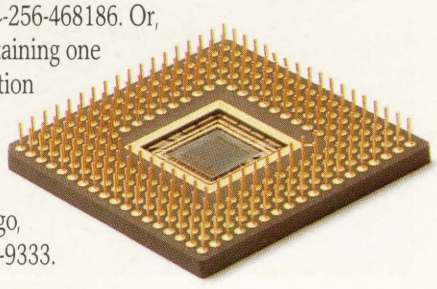

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resources are fully used. Some ECL arrays have low-power options that drop the total power of a 10,000-gate device to less than 10 W by reducing performance. The designer must be careful to ensure that these devices still meet speed requirements.

The primary improvement that E/D GaAs technology brings to the high-performance market is reduced power dissipation. By operating from a single −2-V power supply, E/D GaAs can offer performance comparable to that of ECL circuits while consuming one fourth the power. For example, the VSC4500 gate array from Vitesse Semiconductor (Figure 6) can integrate as many as 4,000 NOR gates and has a typical power dissipation of only 1.5 W.

E/D GaAs and ECL silicon circuits have very similar speed parameters. Typical gate delays for both technologies are on the order of 200 ps, and flip-flop delays, from clock input to data output, are approximately 700 ps for lightly loaded outputs. Exercising high-power options on an ECL array can result in higher performance than that possible with an E/D GaAs array, but these options can increase power consumption to the point where the device becomes unsuitable for air- or conduction-cooled systems. GaAs has an analogous technology—D-mode MESFET—that trades low power consumption for operating frequencies in excess of 3 GHz.

E/D GaAs has a slight edge over ECL silicon in terms of the bandwidth of I/O buffers. Typical ECL devices have I/O bandwidths of approximately 600 MHz, whereas E/D GaAs devices can reach 1 GHz. This bandwidth is achievable despite the fact that the E/D GaAs devices use non-ECL logic

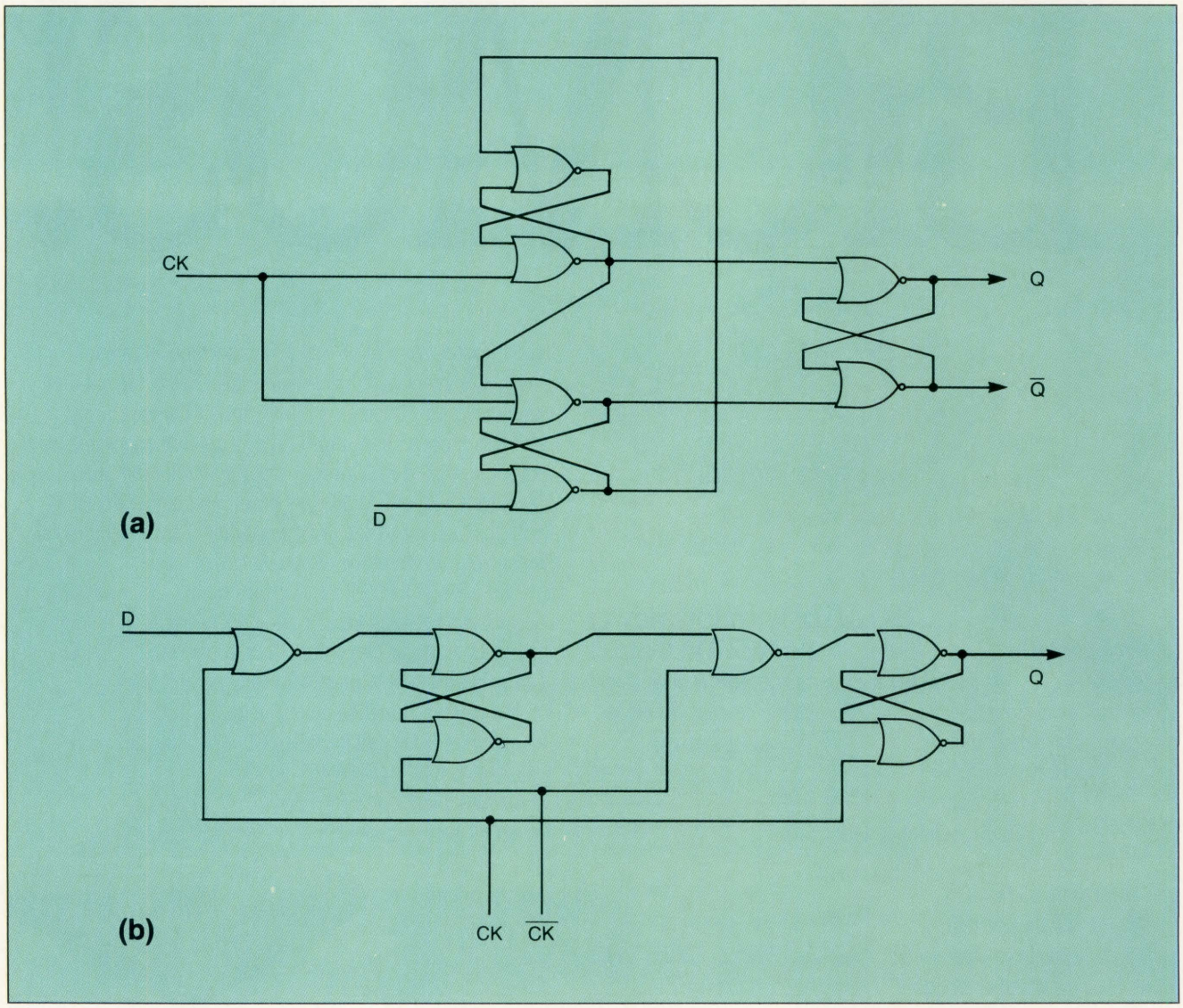

FIGURE 5. Similar to NMOS, E/D GaAs technology uses cross-coupled NOR gates to create a D-type edge-triggered flip-flop (a). A version that uses a differential clock signal (b) has better setup and delay propagation characteristics.

levels internally that must be translated into ECL levels (and vice versa) at the I/O circuits. Higher bandwidths are possible for GaAs if those internal logic levels could be extended between GaAs devices. No standards have been set for GaAs logic levels, however, so that E/D GaAs arrays are built to be compatible with ECL signal levels. The availability of E/D GaAs devices that communicate with GaAs logic levels is likely to occur within a year.

PACKAGING

Packaging technology has evolved to keep up with the requirements of high-performance gate arrays. The typical package, whether it houses a GaAs or an ECL device, is usually a multilayer ceramic package with transmission line interconnects and ground and power planes. The transmission lines serve to maintain an environment free of discontinuities from the chip pads to the package pins. The ground and power planes in the package minimize the inductance of the power distribution system and reduce transients that are caused by switching outputs. The packages are usually available in either a pin-grid array (PGA) or leaded chip carrier (LDCC).

Heat removal is critical to the proper operation of ECL devices. Package thermal resistance ranges between 1°C and 5°C per watt dissipated by the device. For chips dissipating in excess of 20 W, liquid cooling may be needed to maintain junction temperatures in operational ranges. For devices dissipating less power, a heat sink with hundreds of linear feet per minute of air cooling is adequate.

E/D GaAs devices require less severe cooling measures because they dissipate much less power. A typical 4,000-gate chip can usually operate without a heat sink if it resides in a ceramic package with a built-in copper heat spreader.

In terms of cost, E/D GaAs arrays compete head to head with ECL devices. Although GaAs wafers are more expensive than silicon ones, MESFET technology requires substantially fewer fabrication steps than bipolar ECL technology, primarily because MESFETs are planar devices whereas ECL uses more complex vertical device structures. The E/D GaAs process contains only nine masks, even though both enhancement and depletion transistors are produced; one industry-standard ECL process uses 24 mask steps. Because most major processing steps and materials are identical to those used in silicon MOS processing, fabrication errors should not be a substantial source of yield limitations. GaAs wafer defect density still lags behind that of silicon, but excellent progress has been made in the past year. As demonstrated by existing products chips with between 4,000 and 6,000 gates can be fabricated with acceptable yields. We project that in two years chips with between 10,000 and 20,000 gates will be commercially viable.

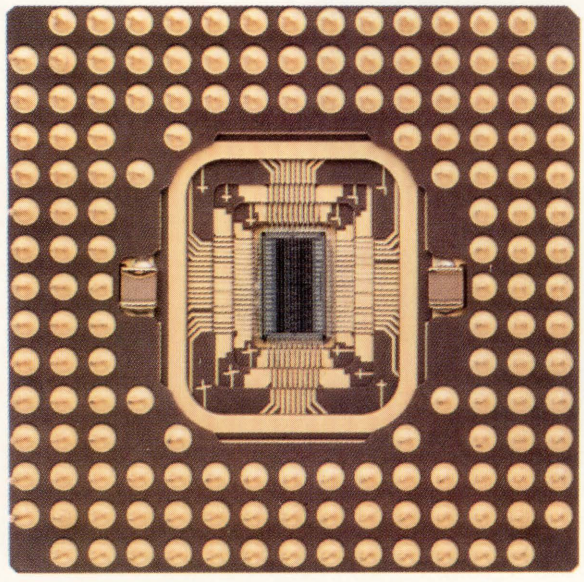

FIGURE 6. The low power and small cell size of E/D GaAs makes possible this 4,000-gate array, Vitesse's VSC4500.

DESIGN GUIDELINES

In the design of a gate array for high-speed synchronous systems, clock distribution is particularly critical. The designer must ensure that all clock signals arrive within specified limits; designs with intentional race conditions are discouraged. The designer should also examine back-annotated layout parasitics to determine the actual differences in clock route lengths and corresponding signal delays.

Maintaining clock duty cycles is particulary important in E/D GaAs arrays because their logic structures produce signal rise times that are slower than the fall times. "Pulse swallowing" can become a concern for high-speed clock signals that have short high-level or low-level durations. Alternating inverting buffers can help to cancel the magnitude of pulse distortion effects. Pulse distortion is also a concern within ECL arrays, although rise and fall time differences are less pronounced in those devices.

Manual placement of logic macros is recommended for all critical paths in a high-speed device. Hand placement seems to have a more pronounced effect on performance than hand routing. Several ECL and GaAs vendors provide their customers with software that allows them to place a portion of an array manually and thereby minimize interconnect parasitics in critical paths. □

ABOUT THE AUTHOR

Ron Cates is the technical marketing manager for Vitesse Semiconductor, where he is responsible for strategic product planning and runs the company's applications engineering department. He also has served as a section manager at TRW's Electronic Systems Group and as a designer at Hughes Aircraft. He holds BS and MS degrees in electrical engineering from the University of California at Los Angeles.

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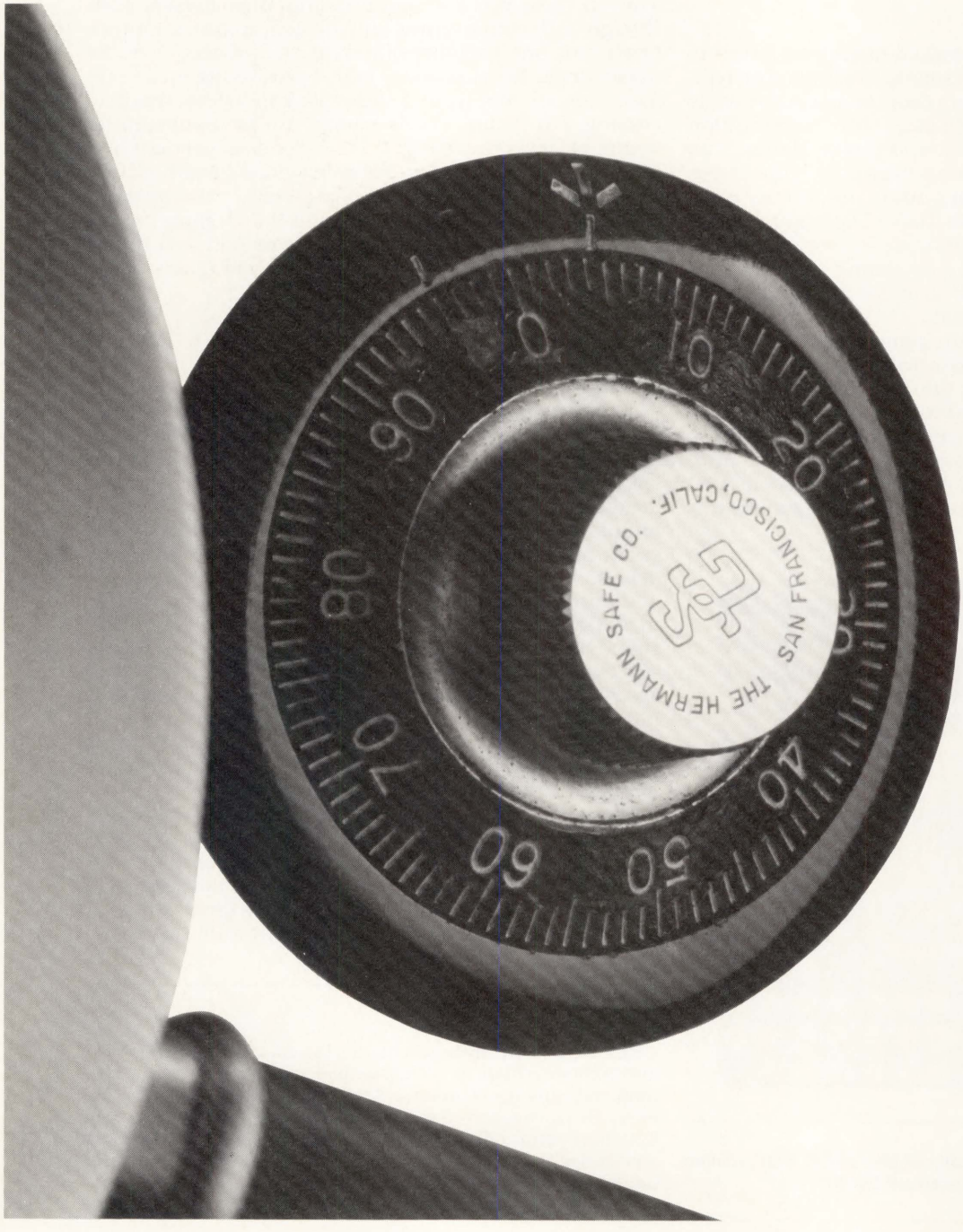

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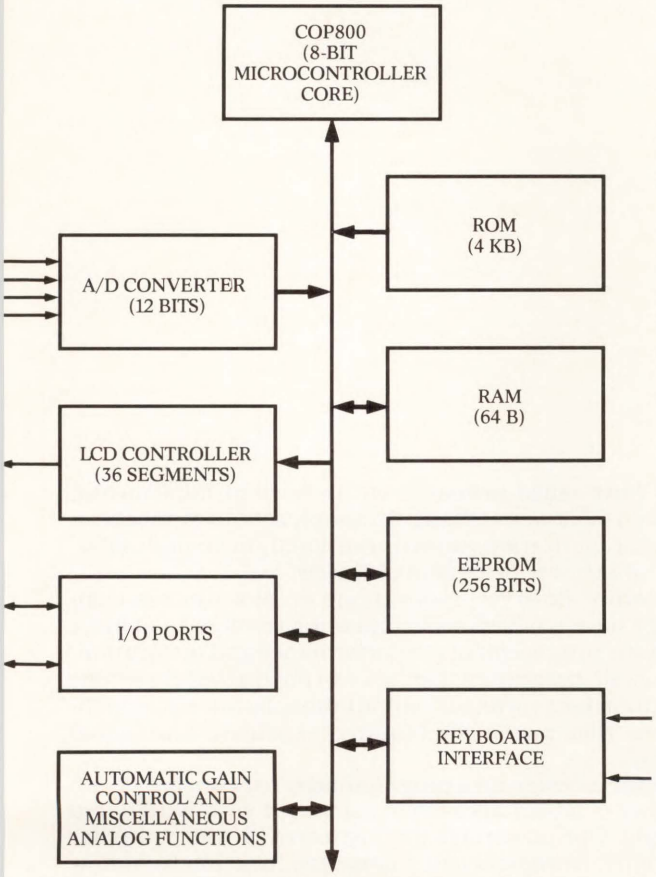

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CIRCLE NUMBER 8

A HYBRID APPROACH TO APPLICATION-SPECIFIC DSP DESIGN

Howard Moscovitz, AT&T Bell Laboratories, Allentown, Pa.

Designers of application-specific integrated circuits for digital signal processing have a variety of design alternatives available to them, from traditional schematic capture and standard-cell design to logic synthesis, module generators, data path compilers, and DSP CPU cores. At present, however, no individual methodology provides an optimal solution for a wide range of DSP applications. Consequently, rather than relying on a single tool to handle all of their applications, what designers need is a hybrid methodology that enables them to take advantage of multiple design approaches.

With such a system (Figure 1), designers can partition their DSP ASIC designs and apply the most appropriate methodology for each subsystem or module. The system-level interaction of each subsystem can later be verified through mixed-mode simulation and a multifaceted test strategy. By automating these processes as much as possible, a hybrid system enables the designer to both maximize performance and minimize design time.

PROGRAMMABLE DSPs

One design methodology that is rapidly gaining popularity is the use of programmable DSP cores in conjunction with customized peripheral and I/O functions. Using this approach, the designer combines the core CPU with such functions as additional arithmetic units, memories, I/O ports, registers, data conversion circuits, and other combinatorial logic.

Traditionally, because DSP applications have been performance-bound, designers of special-purpose DSP circuits have relied primarily on hard-wired implementations. In most cases, designers simply could not shoehorn complex applications into conventional single-multiplier, general-purpose programmable DSPs.

Recently, however, innovations in CMOS process technology have enabled semiconductor vendors to achieve dramatic improvements in performance and integration. As a result, programmable DSPs can now provide real-time execution for a variety of computationally intensive applications that previously required expensive hard-wired designs.

Basing a design on a programmable DSP core provides a number of advantages when compared with hard-wired designs. One advantage that DSP cores provide is higher flexibility. Designers can change the function by simply changing the program that's stored in ROM (as they can with standard DSP chips); they can also select the exact amount of on-chip memory that is needed for the application.

Another advantage is that the applications are easier to simulate, test, and debug, since high-level simulation models and development systems are available for DSP cores. Furthermore, because semiconductor vendors typically build testability into their cores, the task of developing complex test programs is simplified. Designers can even build hardware breadboard prototypes, using a stand-alone version of the off-the-shelf DSP in conjunction with the appropriate memory and logic elements.

Probably the chief advantage of using a programmable DSP is the ease of software development. In addition to providing a standard assembler, many vendors are offering advanced software tools, such as application libraries,

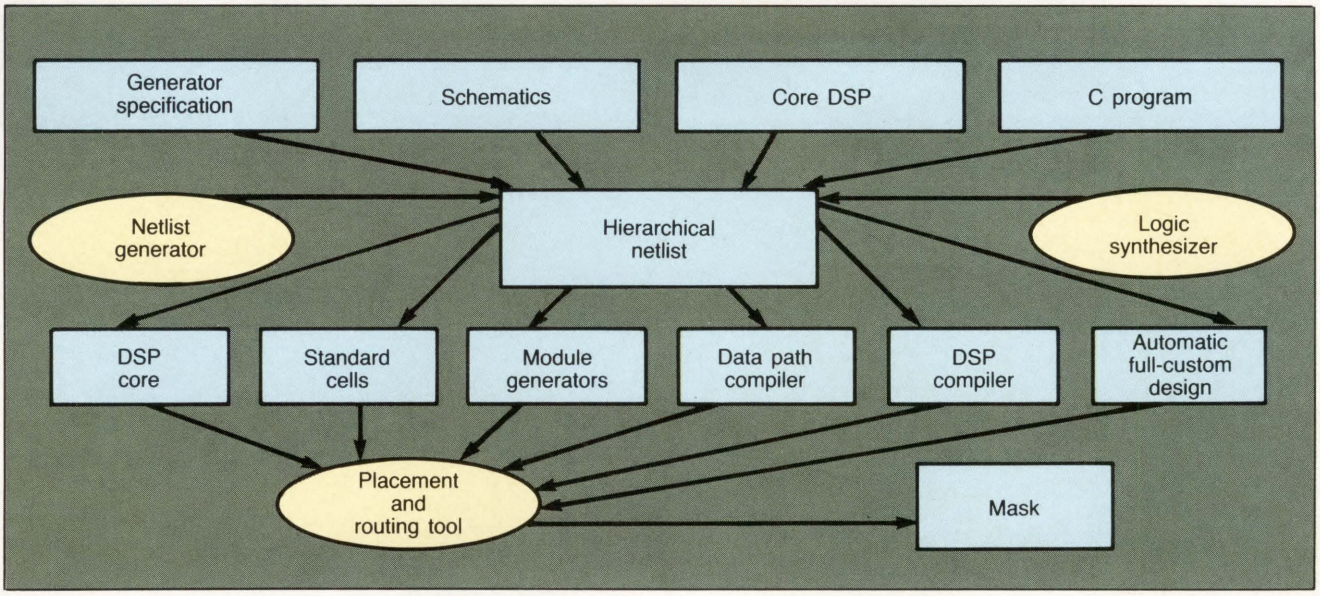

FIGURE 1. Hybrid system for DSP design.

debuggers, and compilers. With AT&T's DSP32C, Texas Instruments' 320, and Motorola's 56000, for example, designers can use combinations of C and assembler, coding the bulk of their programs in C and the speed-critical portions in assembler. Third-party vendors also are contributing, providing menu-driven development packages that enable non-DSP experts to experiment with DSP functions and construct programs without requiring an understanding of DSP architectures or conventional programming languages.

HIGH PERFORMANCE DEMANDS DESIGN DIVERSITY

With the speed of at least one DSP core (the DSP16A) now exceeding 30 MHz, designing peripheral logic that can keep up with the CPU core is becoming more difficult. Although a standard-cell methodology provides sufficient speed for many applications, in some cases standard library components may not prove sufficiently fast.

Here, a hybrid design system provides an excellent alternative. With it, designers implement each section of their circuit using the most productive design methodology that meets the system's minimum performance requirements. Once designers have partitioned their circuits, they select the appropriate method for each module and obtain an optimized netlist for the entire chip. Preferably, as needed, they would be able to further optimize the speed or power consumption of individual modules by taking advantage of an automated full-custom layout capability with automatic transistor sizing.

DATA PATH COMPILERS

Certain portions of a special-purpose DSP lend themselves better to different approaches. For the critical data path elements of such circuits as sequencers, address generators and arithmetic units, a bit-slice approach is often employed, with schematic capture generally used for design entry. With a data path compiler, the designer can obtain an automatic custom layout for the data path by specifying the components in the data path and their relative locations.

For regular structures, such as RAMS, ROMS, PLAS, multipliers, and register files, designers can invoke a library of module generators (also known as layout compilers). These generators produce a custom design for such components based on user-supplied parameters like the multiplier precision or RAM word length. Often, a number of generators are available for a particular function to optimize it for a specific applications (such as Wallace tree, parallel array, and shift-add for multipliers).

LOGIC SYNTHESIS FROM C

For less common DSP functions or for random logic functions that don't map well to the DSP generators, designers can take advantage of general-purpose logic synthesis tools, which produce a netlist based on a Boolean or other functional description. With AT&T's logic synthesis tool, known as Cones, designers describe their logic using a C language functional description that specifies the circuit's state transitions at the bit or register level.

Cones uses a three-step process to generate a netlist. First, it takes a C description and generates a Boolean equation (sum of products) for each bit in the circuit (output or flip-flop) description. Next, it generates a netlist. If the target design is an IC, Cones develops the netlist using an optimal combination of the logic elements contained in the standard-cell library. If the target is one or more PLDS (which might be used for prototype development), Cones partitions the design and generates a netlist using an optimal combination of PLDS.

In the final stage, whether the target device is an IC or one

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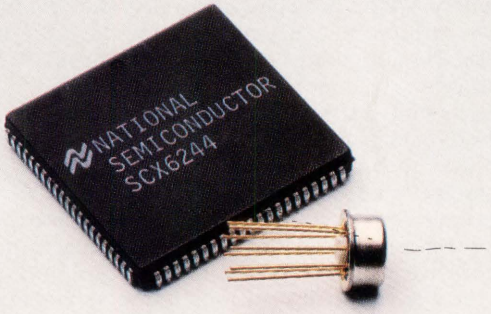

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or more PLDs, Cones looks for common circuitry, forms a single occurrence of this circuitry, and updates the netlist. (For example, each bit in a register may have decoding and chip select circuitry in common).

Limitations of the logic synthesis approach

In most cases, Cones can generate a netlist whose efficiency is comparable to that which can be obtained in a hand design. Still, logic synthesizers, Cones included, have many limitations, particularly for implementing critical arithmetic and data path elements. Multipliers are a case in point. When a logic synthesis tool encounters the expression $A = B \times C$, it may not recognize that specialized generators are available to implement that function. As a result, it may try to implement it using standard combinatorial and sequential logic.

Although this approach is generally efficient for handling random logic, it can't match the custom design that a multiplier generator provides. Furthermore, logic synthesis tools can't yet select appropriate DSP architectures, such as bit-serial, bit-parallel, or serial-parallel.

Another limitation is a lack of support for design modifications. Because the compiler handles the entire design, the designer will be unfamiliar with the circuit topology. Consequently, if the resulting circuit doesn't meet all the design specifications, it is difficult for the designer to identify the problem and effect a change.

In addition, logic synthesis tools sometimes don't adequately address the design-for-test issue. Some vendors approach the problem by applying a single test method, like scan path design. However, a practical system must apply a test methodology or combination of methodologies that match the particular function. Scan methodologies, for example, prove ineffective for circuits with large numbers of registers or large amounts of memory. In both cases, because the register and memory elements must be configured as a serial shift chain, the time required to shift data in and out of the chain proves prohibitive. Built-in self-testing provides an effective alternative in many cases. However, this capability is more difficult to provide, as it must be incorporated into the generator or compiler and must be customized for every circuit that is developed.

DSP-SPECIFIC SILICON COMPILERS

A high-performance alternative to general-purpose logic synthesis tools is DSP-specific compilers, which are actually an extension of the generator technology used to implement components such as multipliers. These new tools—for example, Cathedral from Imec in Belgium and Lager, developed at the university of California at Berkeley—design entire DSP modules by converting a programming language or other high-level specification of a DSP algorithm into a series of calls to special, architecture-specific layout generators. The circuits produced by these generators are wired together to form the desired function (Figure 1).

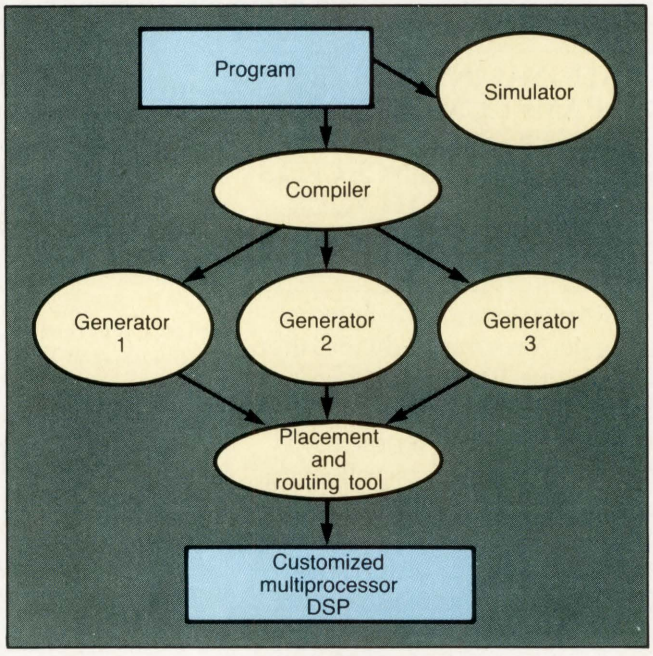

FIGURE 2. Generator-based DSP compiler.

AT&T has designed such a generator system, for internal use, for implementing nth order, m-bit FIR (finite-impulse-response) filters. The system uses a library of parameterized, hierarchical layout generators. It selects and configures these generators based on user-specified parameters like filter length, window type (rectangular, Kaiser, etc.), filter type (low-pass, bandpass, etc.), and filter cut-off frequency.

An FIR filter calculates the sum of products for pairs of data—one corresponding to a signal, $x(n)$, and the other to a coefficient, $h(i)$—according to the following equation:

$$y(n) = \sum_{i=0}^{n} h(i) \times (n-1)$$

This equation is implemented by multiplexing a single shift/add multiplier-accumulator.

The FIR generator system calculates the filter coefficients based on the user's inputs. It then passes the following parameters down for layout synthesis: the order, n, of the filter; the number of bits, m, of precision; the filter coefficients; the number of vertical buses (used as feedthroughs at higher levels of the hierarchy); the transfer protocol for serial data output; and the output drive requirements. The FIR filter consists of the following subblocks: an input serial-to-parallel buffer, an output parallel-to-serial buffer, signal and coefficient registers, a multiplier, and an accumulator (Figure 3).

The subblocks are created hierarchically (Figure 4). A separate generator implements each of the subblocks

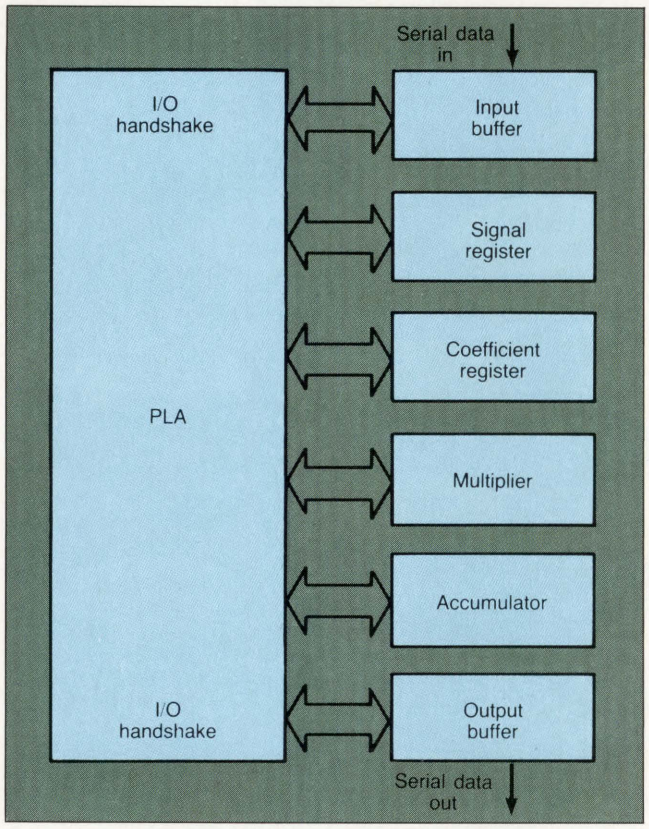

FIGURE 3. Functional blocks of an FIR filter.

based on the compiled parameters and technology information that it obtains from a technology base. Each subblock generator makes calls to a number of subgenerators. At the lowest level in the hierarchy, leaf cell generators handle electrical, physical, and behavioral properties. The hierarchical symbolic layout is then assembled into a fixed-grid layout by a module assembler tool called Panda (which is for internal use).

LIMITED FLEXIBILITY

DSP-specific compilers offer considerable promise for implementing a wide range of DSP functions. At present, however, their chief limitation is inflexibility. The generator methodology works satisfactorily only when a given application maps well to the supported architecture; these compilers may be completely ineffective or unusable for nontargeted applications.

Another problem is the large amount of support software (such as simulation models, fault models, and test vectors) that must be developed to support these generators. Unless there is a significant opportunity to reuse these generators, they may not be cost-effective.

A HYBRID APPROACH

Although advanced tools such as compilers and logic synthesizers greatly simplify the development of high-performance DSP ASICs, designers must recognize their limitations. By adopting a hybrid design methodology, designers can take advantages of the relative strengths of a variety of tools.

AT&T Bell Laboratories uses such a hybrid system to design many of its application-specific DSP circuits (Figure 5). The entry point to the system, which consists of tools designed for internal use, is a hierarchical netlist that can be derived from a variety sources. These include DSP cores, netlist generators (programmable macrocells), transistor- and logic-level schematics, and the Cones logic synthesizer.

One of the advantages of using an open hybrid methodology is the ability to take advantage of new developments in automatic full-custom layout capabilities, which are invaluable in the performance-driven DSP arena. Whereas conventional standard-cell methodologies use macrocells with fixed cell layouts, a custom-layout approach enables designers to maximize speed/power by optimizing transistor sizing.

AUTOMATED OPTIMIZATION OF TRANSISTOR SIZES

AT&T simplifies the design of full-custom circuits through automation. Once designers have obtained a transistor netlist (through logic synthesis, a standard-cell approach, or custom design), they can invoke another internal tool, Tilos, which uses iterative static timing analysis to optimize all critical circuit paths based on user-supplied timing requirements and estimated circuit parasitics.

Tilos doesn't simply choose cells from a library; it optimizes each transistor in each cell. By sizing transistors with Tilos, designers can often develop circuits that operate at twice the frequency of an equivalent standard-cell design using the same technology. Moreover, Tilos enables designers to optimize either performance or power dissipation by providing a set of control parameters. In contrast, a standard-cell approach typically provides a limited set of performance options. Thus designers don't have as much freedom to optimize their circuits by making performance/power trade-offs.

AUTOMATIC FULL-CUSTOM LAYOUT

Once an optimized hierarchical netlist is generated by Tilos, it is passed to a layout supervisor tool called Impala, which creates a customized, hierarchical, row-oriented symbolic layout. To do so, Impala calls a CMOS symbolic layout cell compiler (known as SC2) for each cell in the module. SC2 can create symbolic layouts for any CMOS circuit form: conventional complementary static, dynam-

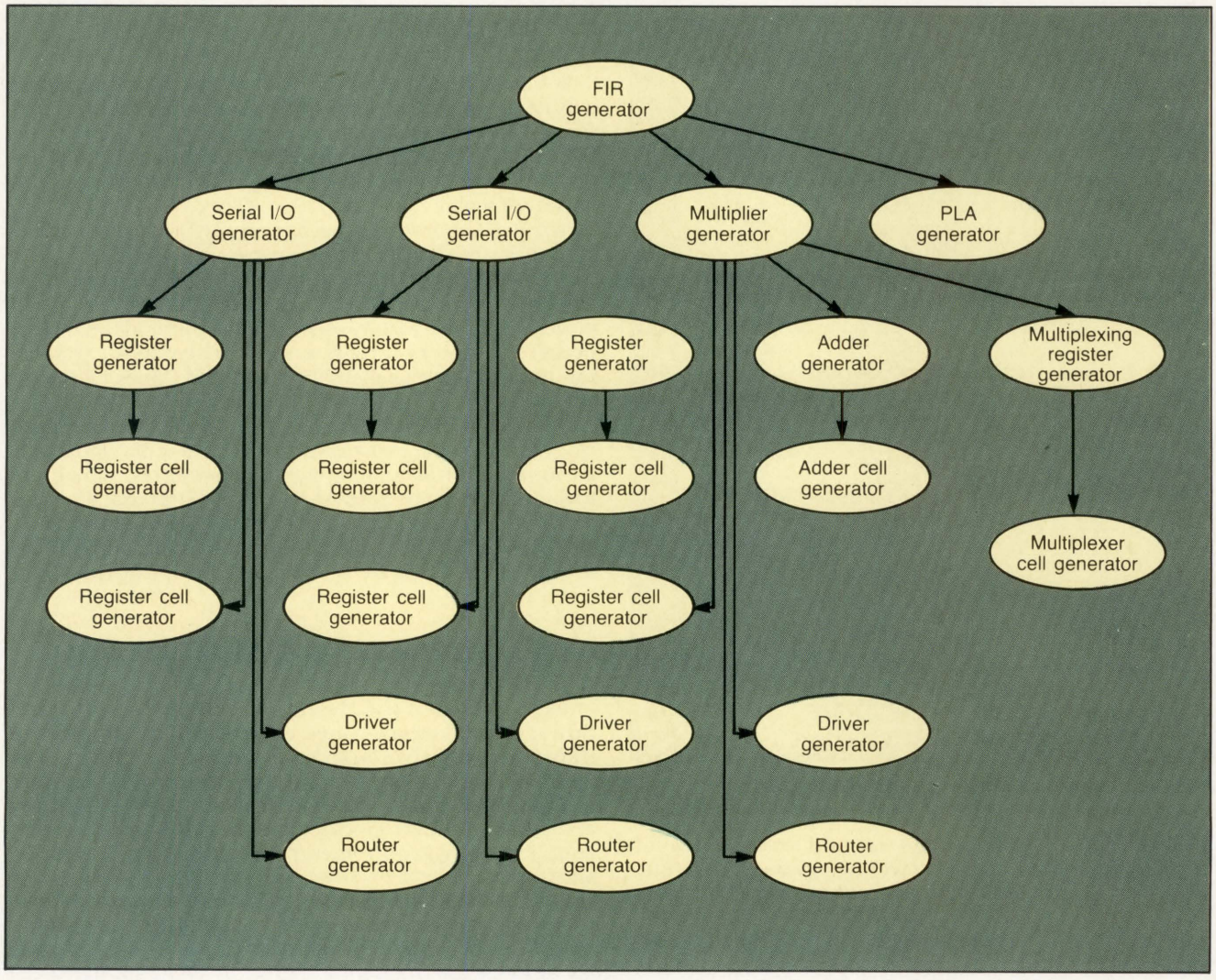

FIGURE 4. Layout generator hierarchy for FIR filters.

ic, domino, zipper, and so on. Since most cell compilers are effective for cells containing only about 200 transistors, Impala creates hierarchical modules that contain many compiled cells.

The resulting symbolic layout is converted into a technology-specific manufacturable mask by a hierarchical module assembler program called Panda. The entire transistor sizing and layout loop can be repeated by extracting more accurate parasitics and supplying them to Tilos. However, since the automatic layout process is very consistent and predictable, a prelayout parasitic estimator (appropriately called Paranoid) has been developed to minimize the need for additional iterations. Once all the chip's modules have been designed, they are connected to the chip's I/O pads using a standard-cell placement and routing tool known as LTX2.

SYMBOLIC LAYOUT PROVIDES DESIGN UPDATABILITY

Because all the programs in the tool set employ symbolic layout, designs are, to a great extent, independent of design rules. With symbolic layout, transistors, wires, contacts, and cells are placed on a virtual grid in terms of their relative location. Once the the layout is complete, a user-supplied technology file is referred to adapt, or bind, the design to a specific fabrication process.

By employing symbolic layout, AT&T is able to more easily

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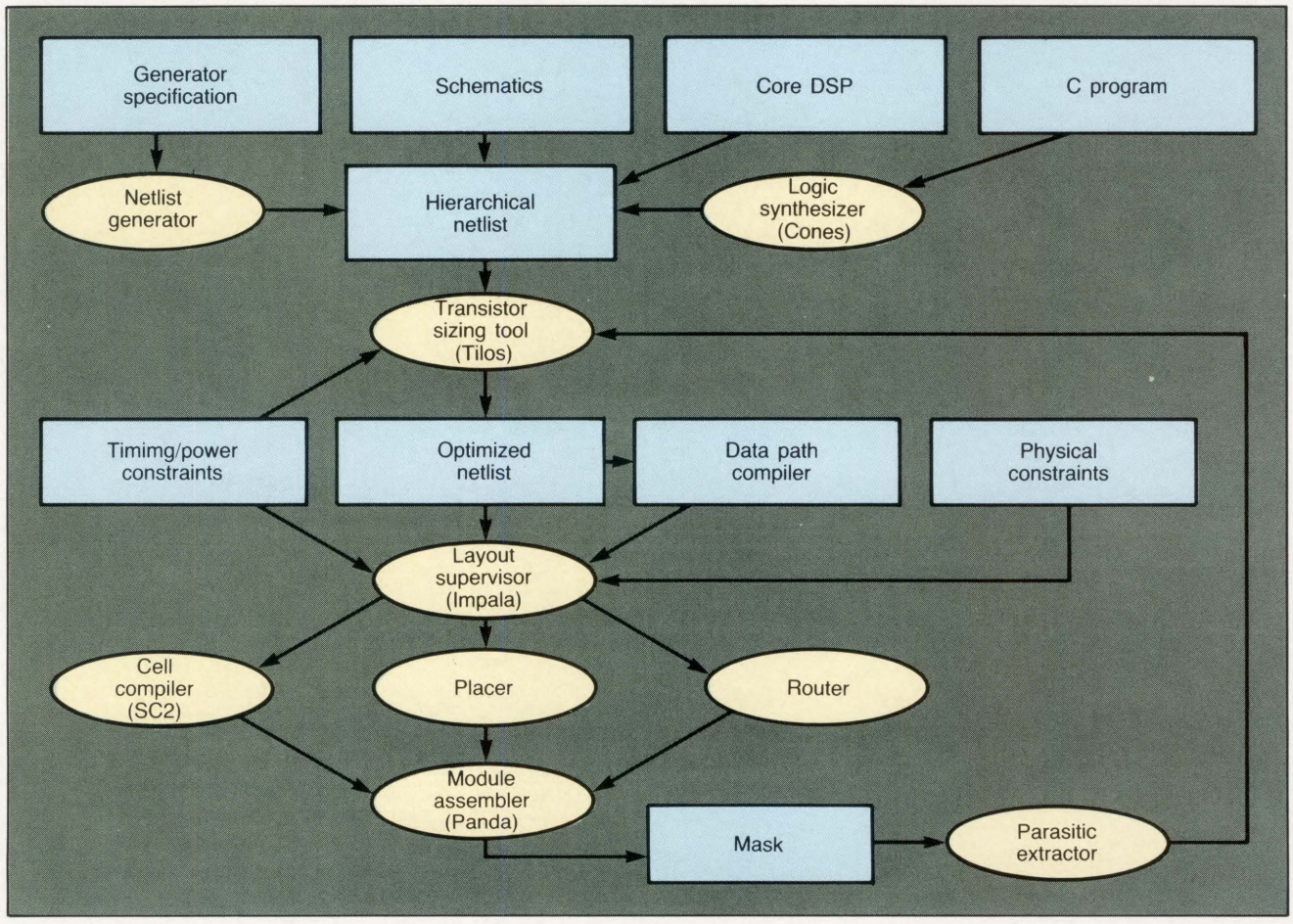


FIGURE 5. The hybrid automatic full-custom DSP design system at AT&T.

migrate to new technologies. At the same time, because designers don't have to be concerned with the design rules of a particular process, the design of new generators is greatly simplified, thus improving productivity. Designers can concentrate on the design of new generators, rather than on updating existing ones for new technologies.

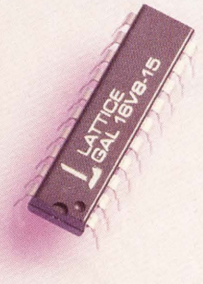
FULLY AUTOMATIC DESIGN—STILL IN THE FUTURE

The ultimate goal in CAE/CAD development is to produce a decision-making system that can automatically partition a circuit and apply the best methodology for each module. Such a tool will also have to provide mixed-mode simulation and apply the most effective test methodology.

At this point, however, the individual capabilities of each methodology are evolving so fast that updating the decision-making software is a formidable task. For the foreseeable future, therefore, designers will have to assume this task themselves. With a versatile enough tool kit, however, they can significantly reduce the design cycle for application-specific DSPs without compromising circuit performance. □

ABOUT THE AUTHOR

Howard Moscovitz is the supervisor of AT&T Bell Laboratories' DSP design methodology group, which also does research on DSP architectures, and the technical chairman of the IEEE VLSI for Signal Processing Workshop, to be held in Monterey, Calif., in November. He received an MFA degree in electronic music and recording media from Mills College in Oakland, Calif., in 1972 and was the director of Electronic Music Associates in the same city from 1972 to 1981. That year he earned an MS degree in electrical engineering at the University of California at Berkeley and joined AT&T Bell Labs.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PROGRAMMABLE LOGIC UPDATE

Ernest L. Meyer, Campbell, Calif.

Last year, programmable logic device architectures were evolving in three essentially different directions: some chips were replacing the AND/OR plane with unorthodox programmable structures; some were combining programmable structures with standard-part functions; and some were enhancing conventional structures with more advanced macrocell capabilities. Recently, a fourth trend has rapidly emerged: some PLDs are just getting faster.

DEVELOPMENT SYSTEMS

At first blush, programmable chip architectures might seem irrelevant to the current-day system designer. With the actual advent of "universal" programming systems, designers could define a circuit at an abstract functional level and then hit the "compile" button for different PLDs until the circuit fit into one. Unfortunately, device support by universal programming systems typically follows a chip's introduction by about six to nine months. In the interim, designers must use device-specific development systems from the component manufacturers.

Since a competitive edge can be gained by implementing a PLD before its support by universal programming systems arrives, it may seem attractive to jump for a new part and get the development system for it. However, it is more time-consuming to evaluate alternative implementations with device-specific development systems: the design must be entered on each system separately. Performance comparisons are not simple, and so designers may instead opt to choose a part before schematic capture and simulation. It is therefore advantageous to understand the available architectures, to know what the best chip is for a particular requirement.

Universal programming systems continue to be useful in this process, since established PLDs are often the best choice anyway. At this stage, many of the devices that were reported on last October (Meyer, 1987) are now supported by the leading universal programming system, from Data I/O. For example, the company now supports the Xilinx family (for schematic capture and simulation, anyway), as well as the PLX448, the 29M16, the 5C032, the GAL39V18 (now renamed the GAL6001), and the EP1800.

Data I/O is also now distributing the ABEL and PLDtest design software on additional platforms besides the IBM PC: on Intergraph's Clipper and the Sun-3 hardware, as well as on hardware running under the VMS and Unix operating systems.

ARCHITECTURAL VARIATIONS

Choosing the right part for a particular application is becoming an increasingly complex problem. There are now hundreds of PLD parts in thousands of versions. As was stated earlier, the more innovative PLD architectures are evolving in three essentially different directions. Orthodox PLD structures have been entirely abandoned in some chip families, to be supplanted by radically different interconnection strategies. Other chips have melded conventional PLD architectures with standard-part functions into programmable "integrated subsystems." Then, too, some chips have supplemented the traditional architectures with grander macrocell capabilities.

ESOTERIC ARCHITECTURES

In the first of these categories, we noted previously two chip families that represent a distinct departure from traditional PLD architectures: the Erasic family from Exel and the LCA devices, or "programmable gate arrays," from Xilinx. Both have been very successful.

Exel's Erasic family forsakes the traditional AND-OR plane architecture in favor of a single folded programmable NOR array. The XL78C800 offers two combinatorial inputs, two sets of four latched inputs, and 10 registered outputs.

Folded NOR architectures lend themselves to multilevel logic: the XL78C800 can contain a phenomenal 42 logic levels, with 32 buried NOR product terms that can be cascaded combinatorially or combined to form additional registers. A commercial 25-ns version is now available for $14 per hundred, with a 45-ns version for $7.25. Mil-spec parts are $92 and $75 for the respective speed grades.

Exel is currently porting the Erasic family to a 1.2-μm process and will shortly be offering 15-ns parts in commercial grades. The company is also readying its next-generation part, the XL78C1800, which boasts 1,800 gate equivalents in a 40-pin DIP and a 44-pin PLCC.

The Erasic's NOR architecture permits somewhat higher performance for many functions but cannot be designed with a standard programming system alone. Exel offers a transparent preprocessor for Data I/O's ABEL system so that designers can work with a familiar design system. The fuse map preprocessor, simulator preprocessor, and TTL library are under $400.

Xilinx is even more radical. In the XC3020, it embeds 64 macrocells in a grid of dynamically reprogrammable (SRAM) interconnections. Each macrocell contains two flip-flops; in addition, each macrocell may be used for either two four-input or one five-input combinatorial function. The XC3020 also contains 64 I/O macrocells on the periphery, each of which contains two more flip-flops that may be used for a registered input and output or within a counter chain. Thus the chip contains 128 macrocells in total, with 256 flip-flops.

Since this time last year, Xilinx has also introduced the XC3090. This programmable Hercules contains 320 internal macrocells and 144 I/O, yielding an estimated 9,000 equivalent gates and 928 flip-flops. At present, this device is the only programmable logic chip that is conceivably large enough for a full 16-bit microprocessor.

Military-grade versions in 175-pin ceramic PGAs are available in 50-MHz speeds for $346.50 in 100-piece quantities. The XC3020 has dropped to $51.65 for 70 MHz; the old 2064 (with 256 flip-flops) is now a bargain at $32.50. The company will be releasing intermediate parts between the 3020 and 3090 in 84-pin PLCCs and ceramic quad flat packs over the coming year.

Xilinx has expanded its front-end design system line to include design and simulation tool support for almost two dozen vendors, including Data I/O, Mentor, Daisy, Valid, Case Technology, Viewlogic, and Omation. Actual wire delays can be back-annotated from the Xilinx layout software into these systems for postlayout simulation.

An additional vendor has entered into the "esoteric" category: Actel Corp. has introduced a user-programmable gate array that employs antifuse technology for densities up to 6,000 estimated gate equivalents with a 1.2-μm process (Mohsen, 1988). The architecture closely resembles an actual gate array rather than any current form of PLD. Actel's Act1 family may prelude a new generation of design capabilities, with 70-MHz toggle frequencies for any combination of sequential and combinatorial functionality. The first chip contains almost 200,000 antifuses, providing sufficient interconnections to simulate fully a gate array architecture, but increasing the programming time (and, presumably, the fallout) compared with a conventional fuse-link PLD.

As an alternative to gate arrays, the Act1 part is certainly attractive, especially since NREs are practically nonexistent, there is no wait for wafer turnaround, and revisions are pretty much instantaneous.

Programming is one distinction between the two families. The Act1 chip requires about 10 minutes to program. On the other hand, the Xilinx parts can be programmed in milliseconds, although they must be reprogrammed from PROM each time the system is turned on. Xilinx supplies an 8-pin skinnyDIP PROM with enough internal space—64 kilobits—to program its largest array, if no other PROM space is available on board. Some have cited the extra chip and boot time as a disadvantage, but Xilinx points out that the boot time is only milliseconds long and that their skinny-DIP, if it is necessary, is smaller than a fingernail.

'HYBRID' ARCHITECTURES

"Hybridization" of standard-part functions with programmable AND/OR planes can yield higher equivalent-gate counts in smaller chips.

Recently, Atmel has announced the first line of programmable analog/digital devices (PADDs). These devices combine standard analog functions with programmable function control and memory. They will include programmable delay lines, programmable filters, and video DACs, employing nonvolatile memory to store delay-line control codes, filter settings, and color look-up tables.

On the strictly digital front, hybrid architectures currently fall into two categories: programmable sequencers and programmable bus interfaces.

Programmable Sequencers

PROSE and SAM were the first two families of programmable sequencers, both of which combine branch control logic (in a PAL form) with an EPROM- or PROM-based microsequencer and an output register. To these we can now add the TIBPSG507 from Texas Instruments and two parts from Cypress Semiconductor.

SAM, from Altera, contains 768 product terms in a programmable AND plane with eight true and complemented inputs from input pins and eight inputs carrying the micro-address; a 448 × 36-bit EPROM, of which 8 lines feed back to the AND plane; a 15-byte stack; an 8-bit loop counter; and a 32-bit register that pipes into 16 outputs horizontally or vertically. A design system is available from Altera for about $2,000, which includes a microcode assembler, a functional simulator with graphical output, and a programmer. Commercial-grade 20-MHz SAMs are $25 to $30, and a 30-MHz version is being readied.

PROSE, from Advanced Micro Devices, contains up to 16 product terms in a programmable AND array with 14 complementary inputs and 2 outputs; 128 product terms in a 128 × 21-bit PROM and with 8 bit lines connected to registered outputs, 5 bit lines folded back into the PROM array, 2 bit lines XORed with the inputs from the PAL array, and 6 bit lines for condition selection (feeding into the PAL array). Design support is supplied by PALASM 2, and Data I/O supports PROSE programming. PROSE devices are available from stock for $15.

Designers may wonder why these particular dimensions have been chosen for these single-chip sequencers and when a programmable sequencer is preferable to a standard-part implementation. According to Altera, SAM reduces unit cost by about $15, between the component cost, board area savings, and system-level savings over an equivalent 20-MHz system implemented with discrete devices. As for PROSE, Monolithic Memories says that the architecture was established by customer demand.

Texas Instruments' TIBPSG507 is less complicated than PROSE and SAM (despite its longer name). It is in fact similar to the familiar 82S105 from Signetics. However, whereas Signetics's FPLS (field-programmable logic sequencer) contains 16 straight inputs, 8 nonbidirectional

latched outputs, and 6 buried latches, the TIBPSG507 contains 12 straight inputs, 8 bypassable nonbidirectional latched outputs, and 8 buried registers.

Moreover, the TIBPSG507 includes a 6-bit counter as well. The counter can be programmed to stop and start again with product terms, and the clear function can be programmed also. Counter hold and clear functions may be registered or combinational, permitting both external and internal complex count function control. By appearance, then, the TIBPSG507 is simpler to use but less versatile than PROSE and SAM.

Data I/O supports programming for the chip. In 1,000-piece quantities, it costs $15.89 in a 24-pin plastic DIP and $16.24 in a 28-pin PLCC.

Cypress Semiconductor also based its state machine parts on standard PLD architectures. Although these parts do not actually contain counters or sequencers, they *are* specially designed for state machine applications.

There are two parts, one for synchronous and one for asynchronous machines. The CY7C330 is the synchronous state machine PLD. It contains both input and output registers, and runs at 50 MHz. There are 11 registered inputs, which can be programmed to clock on either of two input clocks, allowing two-phase or customized pulse response. There are also 12 output registers and 4 dedicated buried registers, controlled by a separate output "state clock." The user can bury up to 6 output registers without sacrificing input pins, yielding up to 10 buried registers. The device comes in 50-MHz and 33-MHz versions, in windowed ceramic 28-pin slimDIPs for $30.60 and $23.55, respectively, in 100-piece quantities. Plastic windowless packages will soon be available for $24.70 and $19.40.

The CY7C331 is a registered PLD specially tailored for asynchronous state functions. It contains 12 registered bidirectional macrocells and 13 nonregistered inputs. The macrocells can provide registered, transparent, or combinationial input or output; and the set, reset, and clock all are controlled by product terms. The part comes in a 28-pin windowed ceramic package and costs $21.40 and $16.45 for 25-ns and 35-ns versions, respectively.

Cypress is working on a new state machine architecture with 125-MHz speed, destined for availability in the second quarter of 1989. This part will use both rising and falling clock edges to double synchronous throughput and will probably use the same 0.8-μm drawn-feature design rules (0.65 μm *l* effective) as currently used for the '331 and '332. Incidentally, Cypress currently has the smallest feature sizes of all PLD vendors. Cypress is also a technology partner in the forthcoming MAX chip from Altera (described below) and will be shipping the part 90 days after Altera's introduction of the part.

Programmable Bus Interfaces

Harris, which invented the fuse in the first place, was the first company to combine standard-part functions and fuses. The 82C339, which has been available for about four years, contains an octal multiplexed input for interfacing with 8088-type buses and a programmable comparator to generate up to four control signals at user-programmed addresses, making the device ideal for direct memory-mapped applications.

Last year, three further bus-oriented devices emerged: the BIC, the Buster, and the PLX448.

The BIC, from Intel, combines three octal latched transceivers with a standard PAL architecture. The transceivers can be clocked in any one of eight modes, with a special macrocell dedicated to each I/O pin. A further four buried macrocells are included. BICs are shipping for $17.50.

The Buster, from Altera, contains one transceiver, with a 24-mA drive capability, which makes it compatible with IBM's Micro Channel bus. Also, there are two registered inputs, 7 buried macrocells, and 20 I/O macrocells. Buster is now being sampled in commercial 25-MHz grades for just under $25. A development system with programmer goes for some $2,500.

PLX Technology is now shipping the PLX448. This part contains a standard internal PAL architecture with 10 inputs and 8 doubly folded bidirectional outputs. However, the I/O macrocells meet the IEEE-448 standard, with 4 outputs driving 48-mA loads and 4 outputs driving 24-mA loads on a separate clock.

PLX Technology is now also offering preprogrammed versions of the PLX448 for standard bus interface functions. These preprogrammed devices perform common VMEbus, VSB (VME subsystem bus), and Micro Channel protocol functions. VSB masters and slaves are $24 to $26; VMEbus masters and slaves costs $28 to $52; and VMEbus interrupt generators, $26. A Micro Channel master is currently being sampled for $26.

IMPROVING ON THE STANDARD ARCHITECTURE

Most parts that provide embellishments on standard PLD architectures do so by supplying enhanced macrocell capabilities. Macrocells can restrict the actual usefulness of a device if they are not flexible enough. On the other hand, an overcomplex macrocell can be wasteful when just a simple macrocell will do.

Features to check for in "fully featured" macrocells include varying sum-of-product-term distributions; programmable register bypass, feedback, and preloading; individually programmable clock and output three-stating; programmable polarity; sequential diagnostic capability; bidirectional I/O; configurability as a D or JK flip-flop or latch; and an additional feedback path so that the macrocell pin can be used as an input at the same time as the register is buried ("dual foldback").

Four part families sport major variations on the standard architecture. Announced some time ago are the 29M16 and the 29MA16, a planned family from Advanced Micro Devices. In this family, a whole 16 fully featured I/O macrocells are crammed into a 24-pin chip. How? Simply enough, by replacing dedicated inputs by I/O macrocells. These parts lead one to wonder why PLD vendors hadn't dreamed up replacing all the dedicated inputs by programmable I/O macrocells before this.

The 29M16 and 29MA16 differ essentially in their product-term distribution. Between 4 and 12 product terms are assigned to each macrocell, with the distribution different for different groups of pins in the two parts (a trick pioneered by Cypress Semiconductor). Advanced Micro Devices may sample the 29M16 toward the end of the year.

The 5AC312 EPLD, from Intel, contains 8 registered inputs and 12 fully featured I/O macrocells. Of particular

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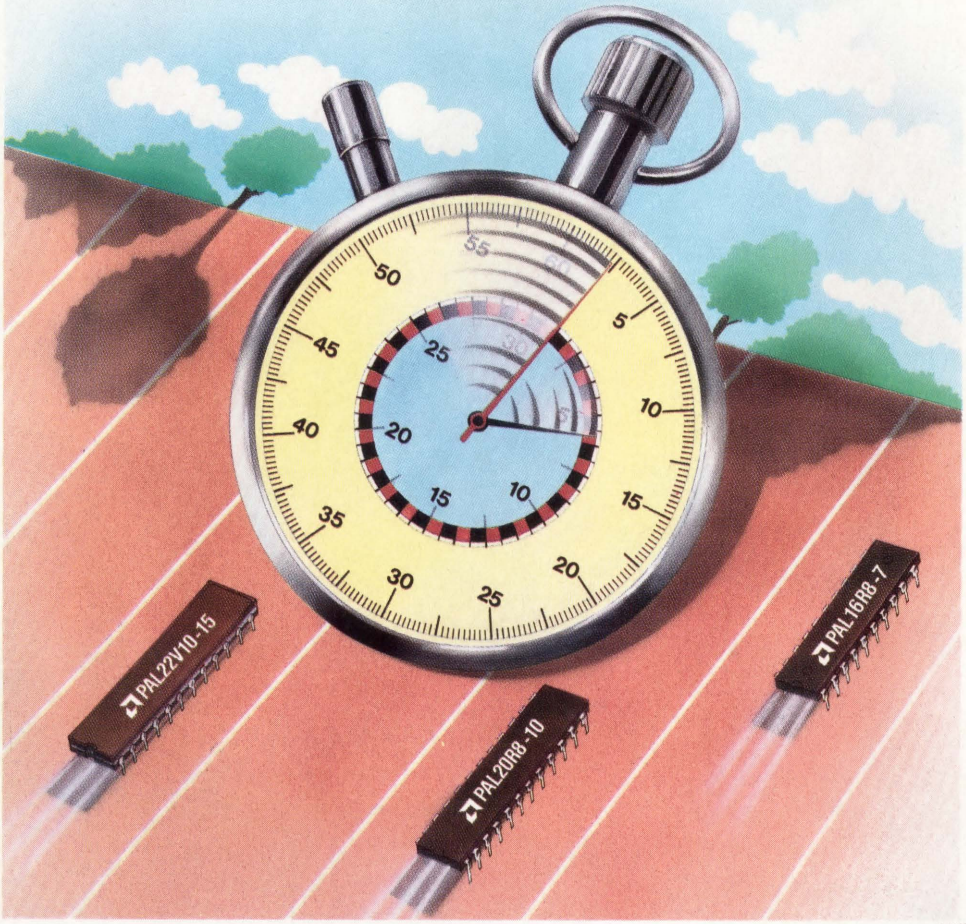

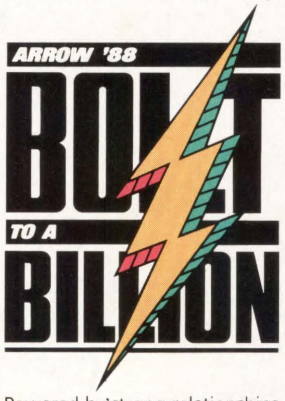

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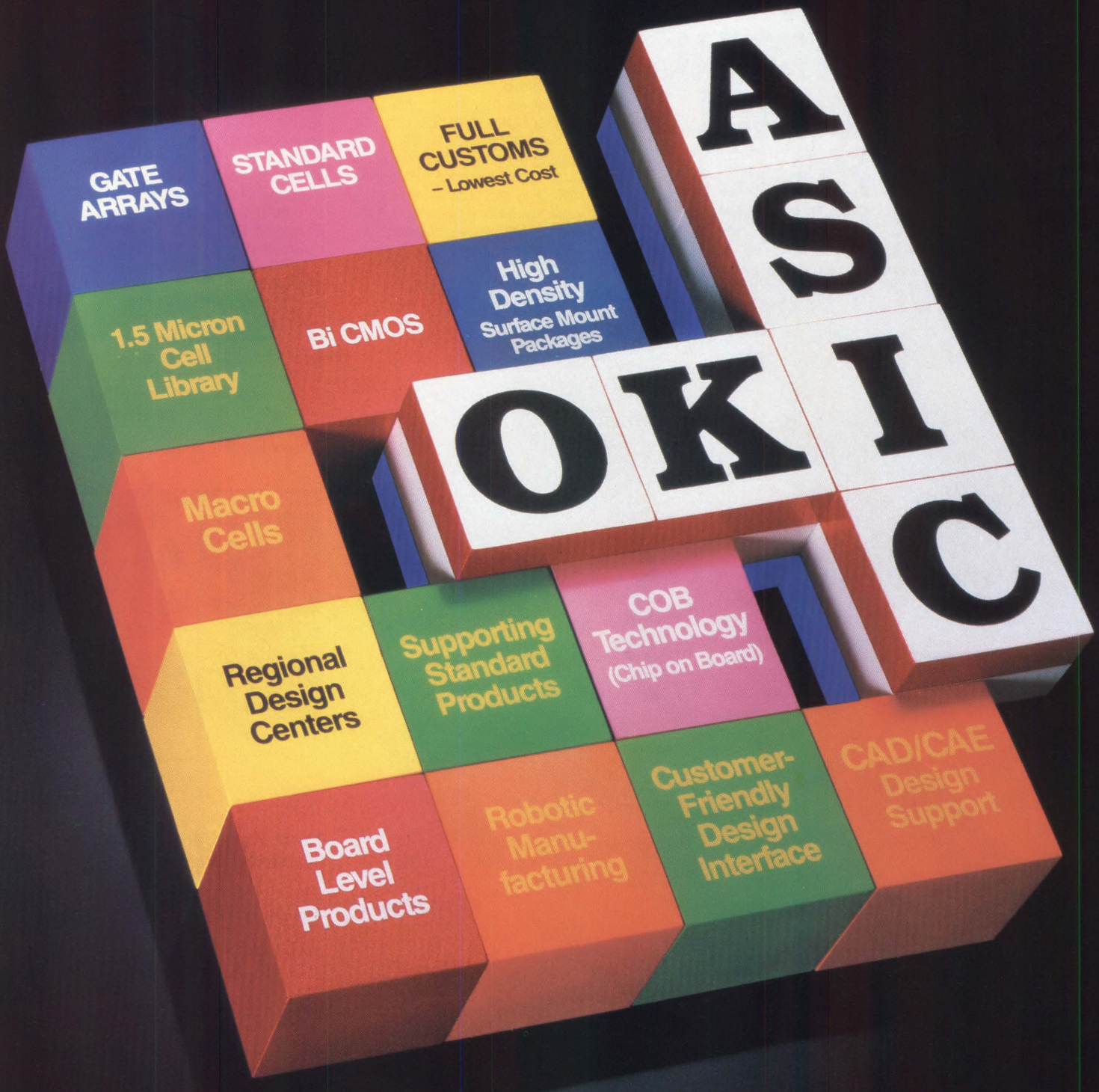
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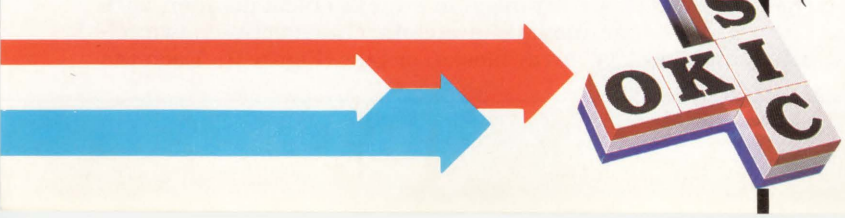

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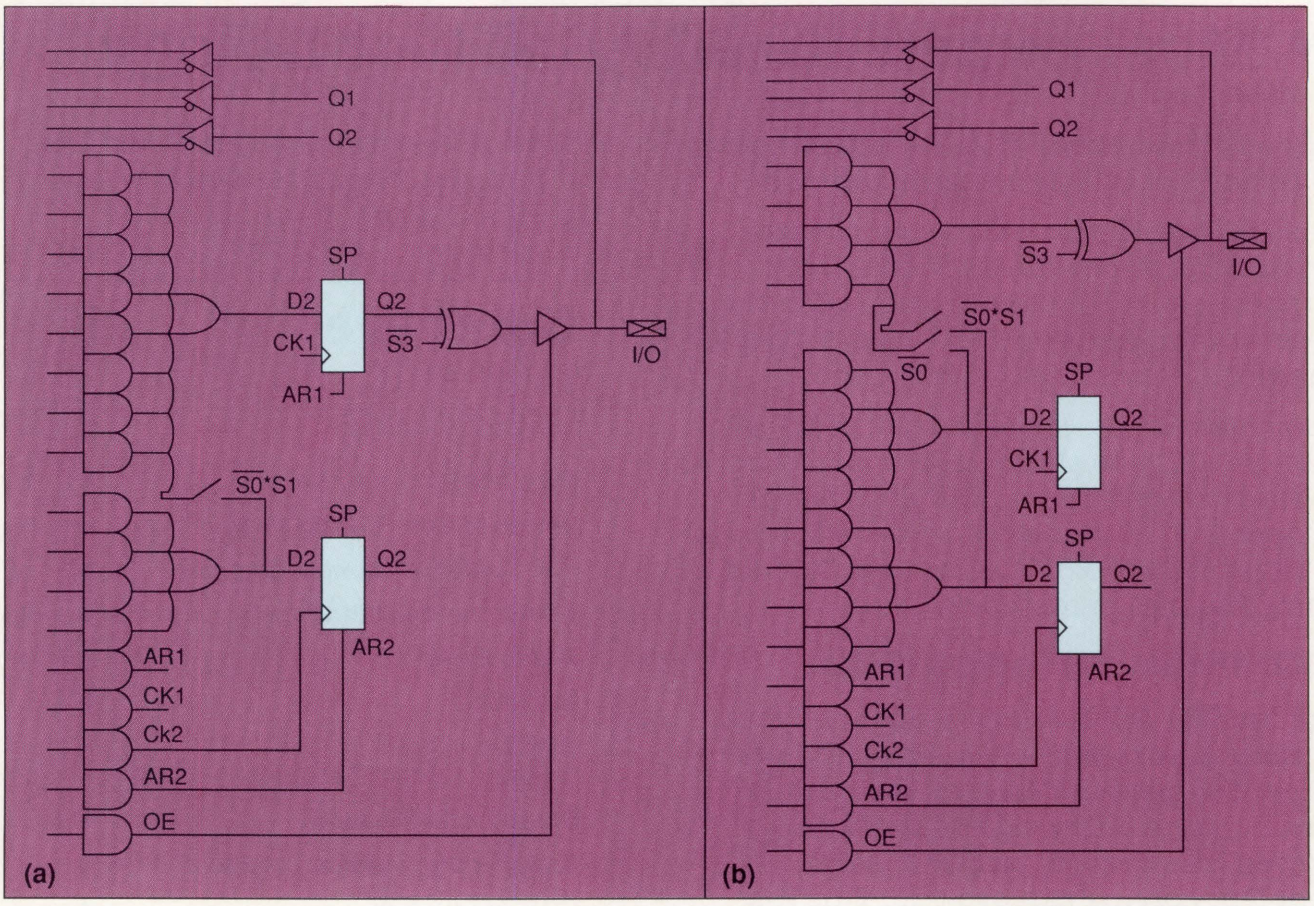

FIGURE 1. In Atmel's "Jumbo Logic Array, each I/O macrocell, registered (a) and combinatorial (b), contains two flip-flops, both of which may be buried.

note: product-term allocation between adjacent macrocells is user-programmable. Each macrocell is normally fed by 8 ORed product terms; however, 4 additional product terms may be reassigned to each macrocell from each of the two adjacent macrocells by programming the appropriate interconnections. Thus a macrocell can be fed by 12 product terms, and one of its neighbors by 4; or a macrocell may be fed by 16 product terms, and each of both of its neighbors by 4. This flexibility makes the part particularly suitable for medium-scale irregular decoding functions.

Now reduced in price to $17.50, the '312 has met with good favor, and Intel will be introducing an additional member for the family by the end of the year. The new part will have twice the density of the '312 and the same features. Intel will also introduce software and programming hardware at the same time, as well as simulation support for the whole family. The new software and hardware will allow engineers to use state machine, schematic design, or netlist entry, as well as detailed timing simulation. The design system for all Intel products will be $3,450. Data I/O already supports the existing parts.

The 30-ns GAL6001 (as noted, previously designated the GAL39V18), from Lattice Semiconductor, has 10 registered inputs and 10 fully featured I/O macrocells. The inputs for the I/O macrocells have separate registers, permitting the I/O macrocells to be buried and the inputs registered simultaneously. The chip also contains 8 buried registers. Supported by a proprietary development system costing less than $800, it is second-sourced by National Semiconductor and SGS Semiconductor.

Also on the density front, consider the "Jumbo" from Atmel and Altera's MAX. Atmel's so-called "Jumbo Logic Array," the ATV2500, contains 14 standard inputs and 24 I/O macrocells in a 40-pin PLCC. Unlike any other part, it contains two doubly folded registers in each I/O macrocell (Figure 1), making it possible to bury 48 registers. Note that the register clocks are driven by product terms, making the part suitable for asynchronous state machines. The macrocells also contain three sum terms that may be allocated to the flip-flops or to a combinational output in a flexible manner (the part can thus emulate Intel's flexible product term allocation).

The MAX is the next offering from Altera and will start shipping next quarter. It uses hierarchical AND planes to reduce the number of fuses and increase the equivalent gate count. True system clock rates of 40 MHz are promised for the family, which will offer 16 to 128 macrocells. The macrocells are arranged in a hierarchical manner, with global programmable interconnections between two columns of logic array blocks, or LABs (Figure 2). Each LAB

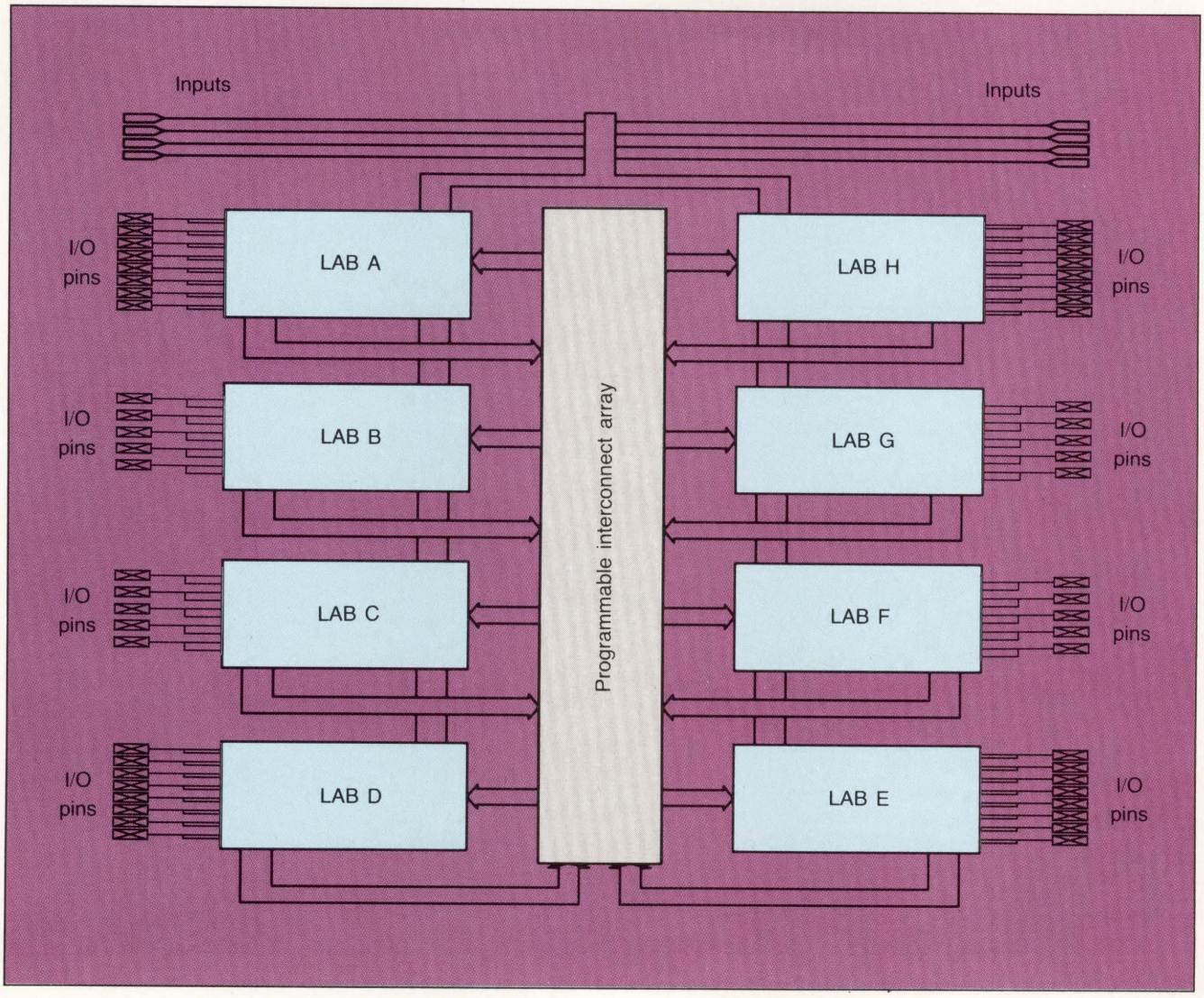

FIGURE 2. The MAX, from Altera, uses a novel structure containing two columns of logic array blocks (LABs), each containing its own product-term matrix, to expand the globally available signals into a larger submatrix.

contains its own product-term matrix to expand the globally available signals into a larger submatrix, as well as 16 to 32 I/O macrocells. The MAX will be supported by its own PC AT–based development system; pricing is not yet announced. As previously mentioned, Cypress is a technology partner and will second-source the part next year; Texas Instruments, Intel, and WaferScale Integration also second-source Altera EPLDs and so will probably be second sources later on.

GETTING FASTER AND FASTER

On the speed front, a number of vendors are closing in on the sub-10-ns region. At the time of writing, Texas Instruments is leading the TTL fray with a specially designed programmable address decoder (PAD). The device moves in the opposite direction from all the architectures described above, focusing on simplicity (Figure 3). The architecture is optimized for decoding: there is only one product sum for each output, but instead of one common output enable line, there is a separate high-impedance control for each pin. The PAD rushes along with a 7-ns maximum delay and a conservative current drain of 180 mA. PADs are available immediately for $9.39 per 1,000 pieces. Data I/O and Digital Media both support PAD programming.

TI is also offering a 6-ns ECL PAL in a ceramic DIP for less than $20. The TIEPAL10H16P8 conforms to the 10KH logic levels and is said to demonstrate 99% yields.

AMD is hot on TI's heels with "standard" TTL PALs rather than new architectures. AMD's 16R8, 16R6, 16L8, and 16R4 are now available in 7.5-ns versions, a mere 0.5 ns slower than the PAD. The parts draw 180 mA maximum (140 to 150 mA typical) and are being distributed at $10.45 per 100. It is worth noting that these parts are the commonest programmable devices in use and so are likely to be

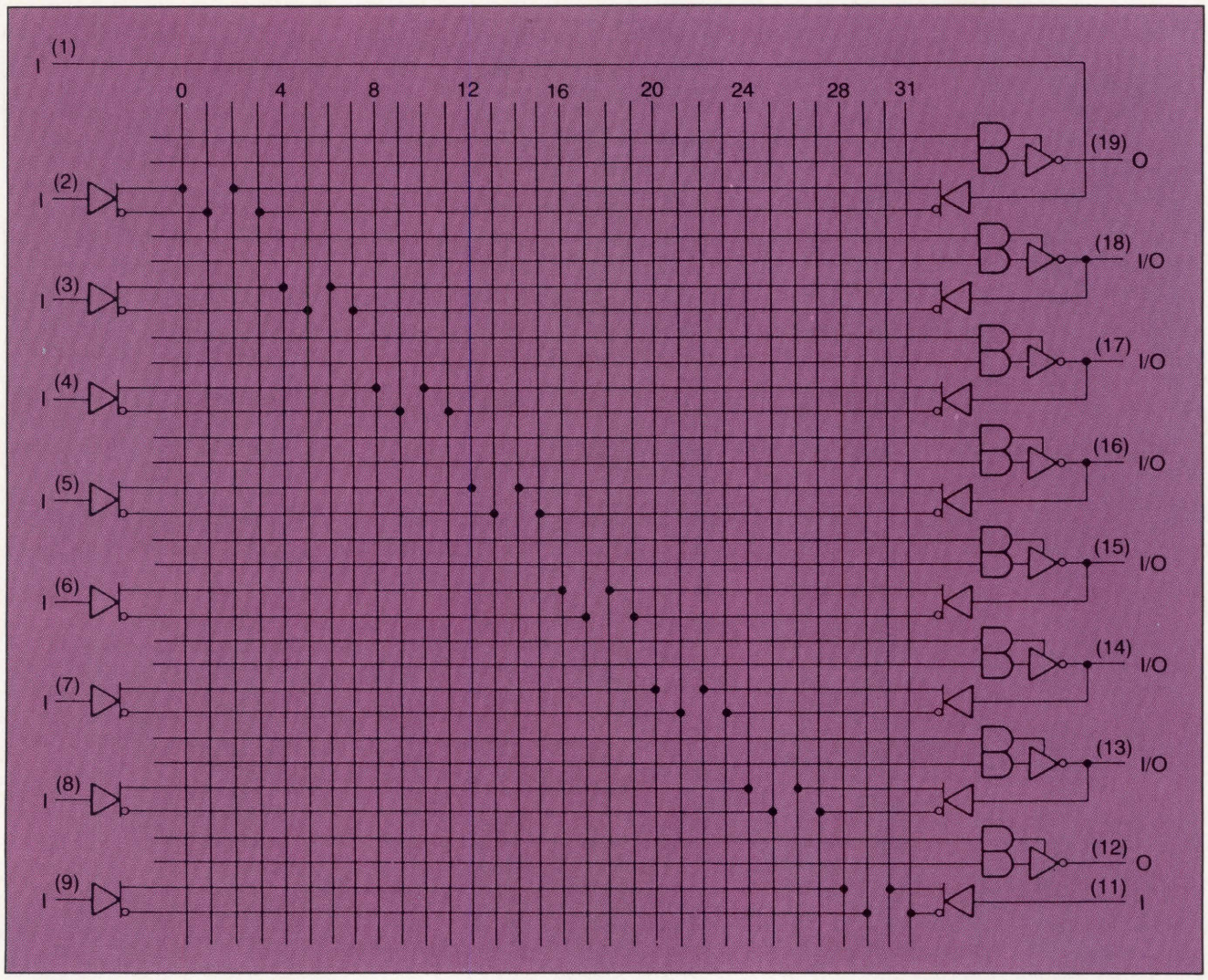

FIGURE 3. Opting for simplicity, Texas Instruments' programmable address decoder (PAD) achieves a maximum delay of 7 ns.

preferred by many. AMD is also offering the 22V10 in a 15-ns grade at $16.45 per 100.

Lattice Semiconductor is selling the fastest EEPLDs at present, clocking in with a 12-ns maximum delay. The GAL16V8A-12 and GAL20V8A-12 are priced at $8.32 and $9.51 each, respectively, for 100 units in plastic DIPs. Lattice is not currently offering a high-speed-grade version of the 22V10.

Gazelle Microcircuits has shaved 5 ns off AMD's high-speed 22V10 version by casting the chip in gallium arsenide. However, its 10-ns GA22V10 is about $50 and must be laser-programmed by the manufacturer. The chip has nevertheless already achieved popularity in the high-end PC market, where it is being used in 25-MHz 80386 machines for cache control.

Gazelle's speed advantage will be difficult to maintain. For smaller functions, chips in TTL are already available that are faster than that offered by Gazelle in GaAs. However, GaAs performance is more stable with temperature variations, and power dissipation is lower.

In fact, the war over power dissipation is just starting. Over the next year, we may well see a narrowing in the speed margins between the different product offerings and, at the same time, a greater focus on power dissipation per gate equivalent. □

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ABOUT THE AUTHOR

Ernest Meyer is a free-lance writer and editorial consultant, as well as a contributing writer and columnist for *Supercomputing Review* and *Embedded Systems Programming.* Previously, he was an editor at *VLSI Systems Design.* He has worked on the design of various electronic systems, including an Apple-compatible microcomputer and a music synthesizer.

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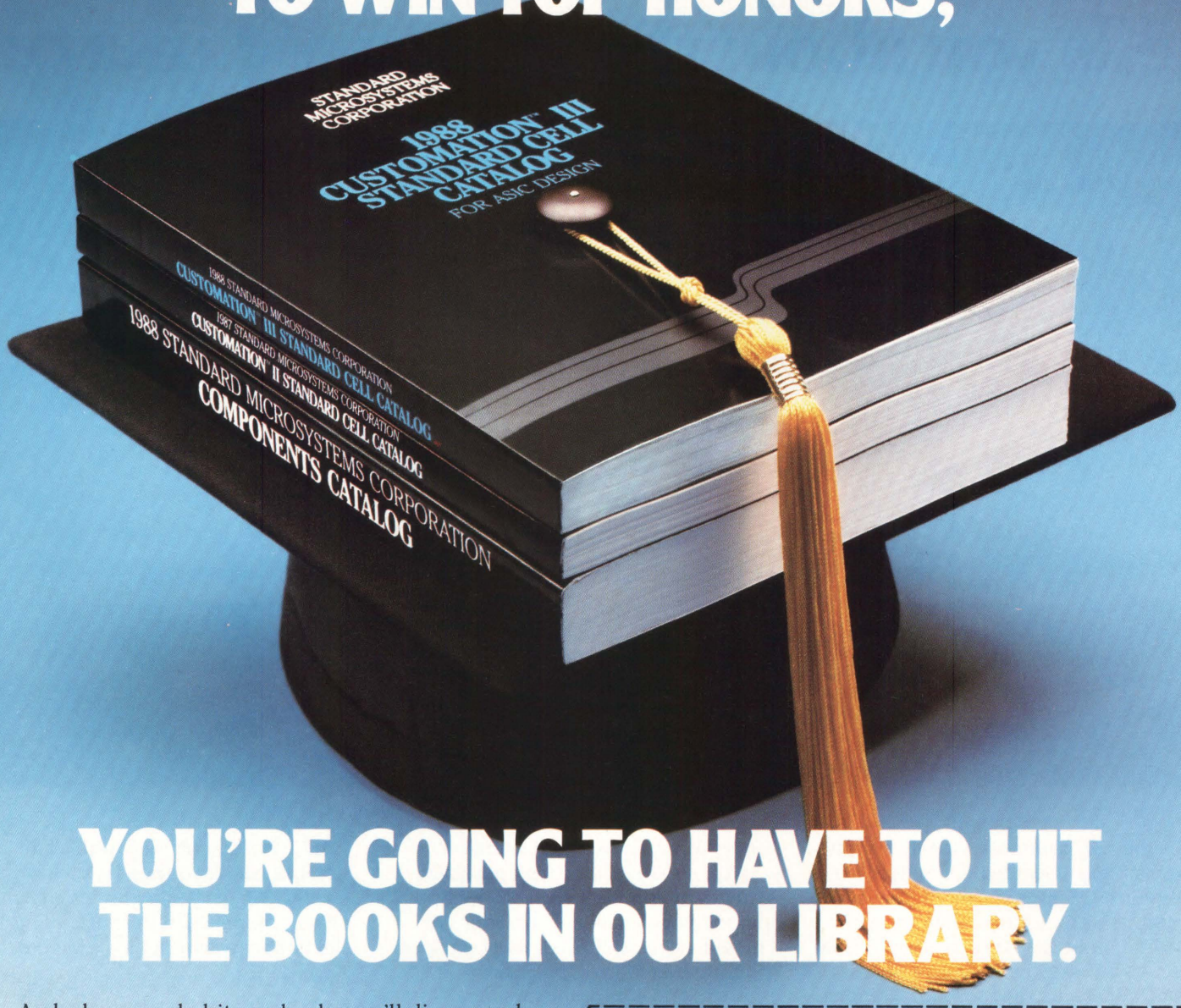

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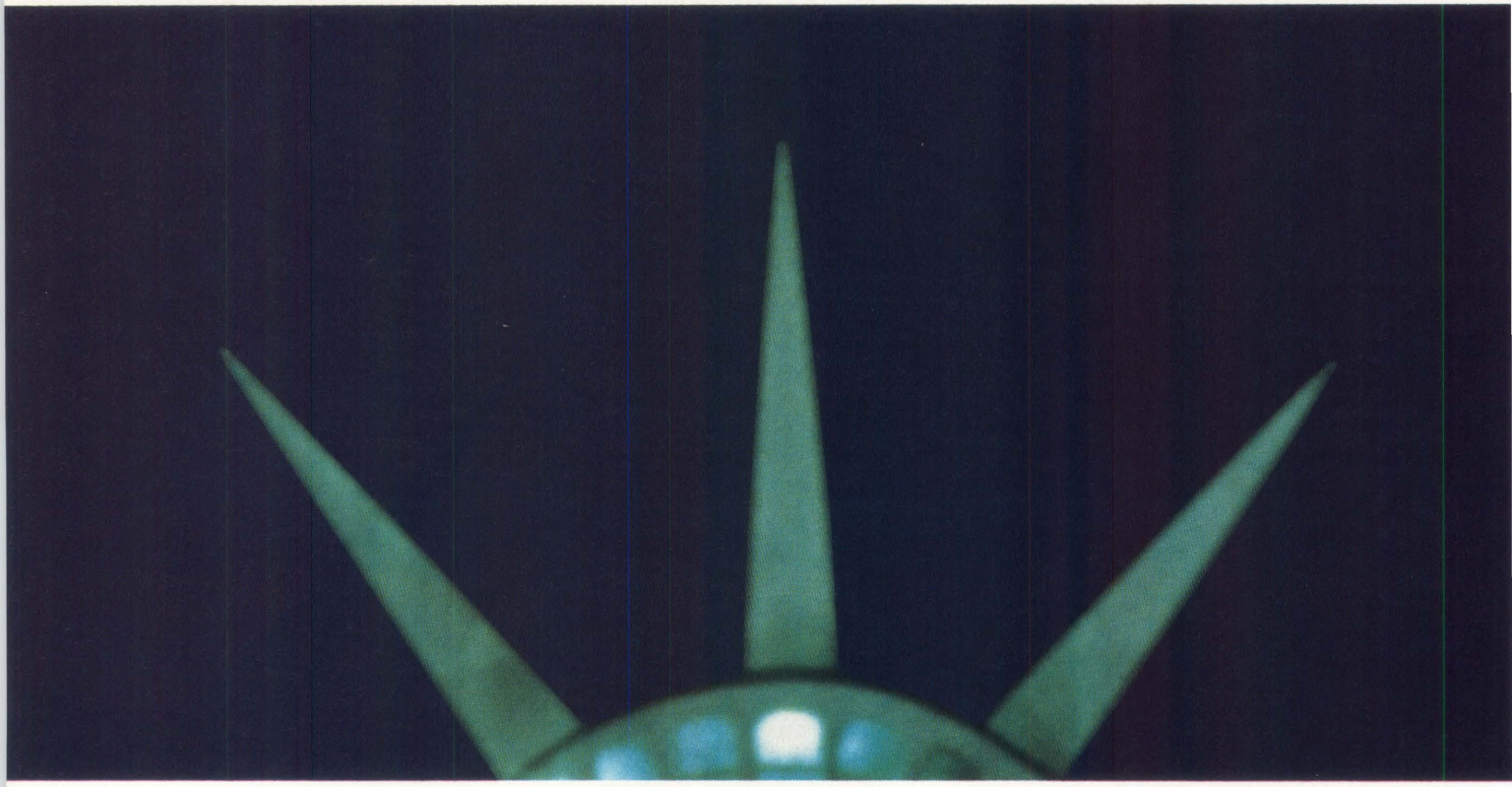

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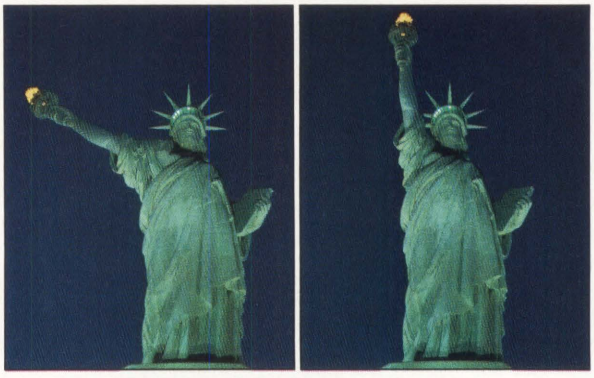

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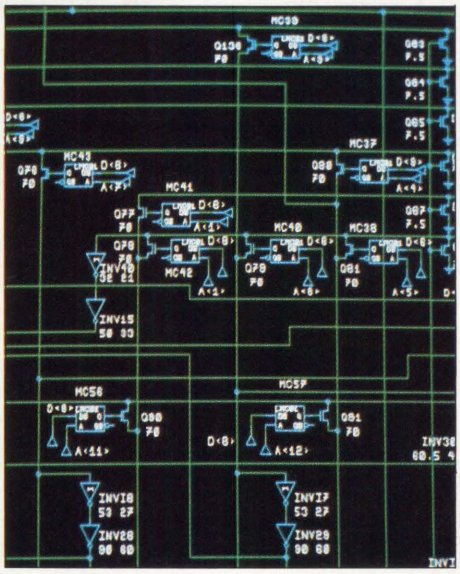
II DESIGN TOOLS & METHODOLOGIES



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56 THE ROLE OF LOGIC SYNTHESIS IN SILICON COMPILATION

Misha R. Burich, Silicon Compiler Systems Corp.

Logic synthesis's key role will be as a consistent piece of a design environment that includes design capture, simulation, logical design analysis, and manufacturing support, the author maintains.

64 VHDL FOR ASIC DESIGN AND VERIFICATION

Rick Sullivan and Lisa R. Asher, Viewlogic Systems Inc.

Starting in October 1988, all ASIC designs submitted to the Department of Defense must be accompanied by behavioral and structural descriptions written in VHDL. The authors present a top-down design verification methodology for large ASICs, using the appropriate subset of VHDL.

74 ADVANCED MODELING TECHNOLOGIES FOR LOGIC SIMULATION

William B. Fazakerly and Robert P. Smith, Ikos Systems Inc.

Smaller device geometries increase the need for more accurate timing models for logic simulation. Table look-ups and linear interpolation techniques deliver a high degree of accuracy.

86 LINKING DESIGN AND TEST FOR ASIC PROTOTYPE TEST DEVELOPMENT

Eric Archambeau, Teresa Butzerin, and Dave Roth, VLSI Technology Inc.

Developing test programs for ASIC prototypes is still a major bottleneck in the semicustom development cycle. The test vector generation methodology descibed guarantees that test vectors will always convert to the cycle-based world of testers, while guarding against race conditions and other hazards.


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THE ROLE OF LOGIC SYNTHESIS IN SILICON COMPILATION

Misha R. Burich, Silicon Compiler Systems Corp., San Jose, Calif.

Logic synthesis converts register- and logic-level design descriptions into detailed logic implementations. In so doing, it frees designers of both application-specific ICs and standard ICs from dependence on a specific technology. At the same time, it delivers a high-level design paradigm and makes possible global optimizations of designs that are too complex to be done by hand. Because silicon compilation delivers some of the same benefits, logic synthesis has become part of silicon compilation products, and it will play an even more important role in future products.

Logic synthesis software attempts to create an implementation that is efficient whether the design is realized as a gate array, a standard-cell IC, or a custom, compiled chip. To meet that goal, it must be integrated with design capture, analysis, verification, and test generation tools. Thus at some companies, including Silicon Compiler Systems (SCS), logic synthesis is seen as part of a design environment that includes simulation, logical analysis, and manufacturing support (for example, test vectors and netlist database).

SILICON COMPILATION IN IC DESIGN

ASIC and IC design automation is helping engineers construct increasingly complex ICs. Today, chip designs with tens of thousands of gates are becoming very common, and size and complexity will continue to grow. Furthermore, IC process technology can handle hundreds of thousands of gates. Consequently, the design automation tools—for both the front and back ends—must keep pace with the capabilities of process technology.

The front end of the design process comprises design capture and verification of the architecture, detailed logic implementation of the architectural components, and simulation and timing verification of the logic implementation. Logic synthesis plays a role in automating the logic implementation of some or all of the architectural components.

The back end of the design process completes the physical layout, verifies functionality and performance, and checks for design rule violations. Further, the libraries of models used in the design are as critical as the verification tools because they tie the front and back ends together, allowing the entire process to be optimized. Silicon compilation can supply all the requisite elements of both ends of design (Figure 1).

Silicon compilation has become a leading IC design automation discipline because its rapid iterations make it the most productive methodology for both cell-based ASICs and standard parts. To get an idea of its range, note that

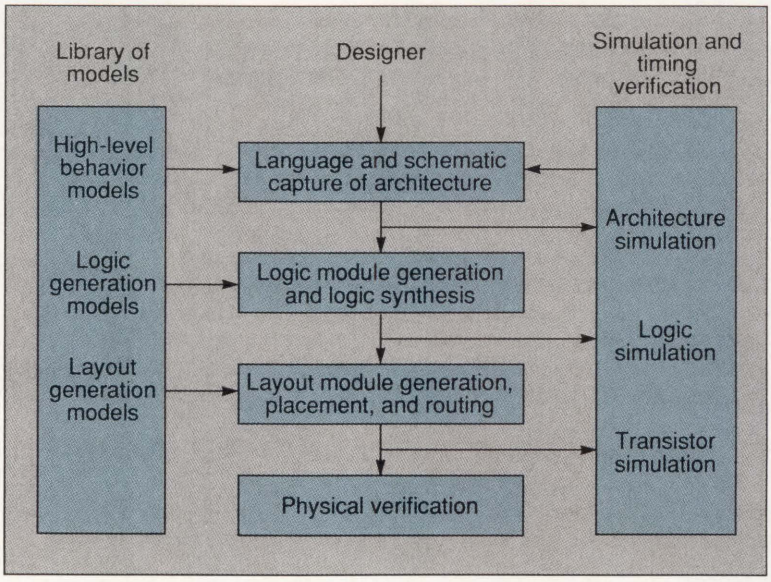

FIGURE 1. The design flow of a silicon compilation system includes logic synthesis to generate unstructured blocks of logic that are not efficiently designed with logic modules.

silicon compilation was used to design the CPU chip set for Tandem's CLX workstation as custom ASICs and the Motorola 88000 RISC chip set as standard parts. Indeed, silicon compilation is especially suited for complex ASICs and multichip designs ranging in density from 10,000 to over 200,000 gates.

Silicon compilation yields rapid iterations at any level of the design process, a capability essential for building complex systems. It improves productivity by integrating into a unified environment some key technologies: design capture, logic synthesis, mixed-mode simulation, timing analysis, test vector generation, cell and module compilation, and placement and routing. Related technologies like computer graphics, high-level languages, and design database management complete the environment.

LOGIC SYNTHESIS JOINS COMPILATION

Logic synthesis is one of the latest additions to the set of silicon compilation tools. In our view, logic synthesis is a subset of high-level behavioral synthesis. Behavioral synthesis itself begins with a functional description of a system—simply put, what the system does. It results in a structural description of the design, consisting of high-level logic elements, like registers and memories. These specifications can take several forms: logic equations, state machine descriptions, truth tables, or descriptions in a structural language.

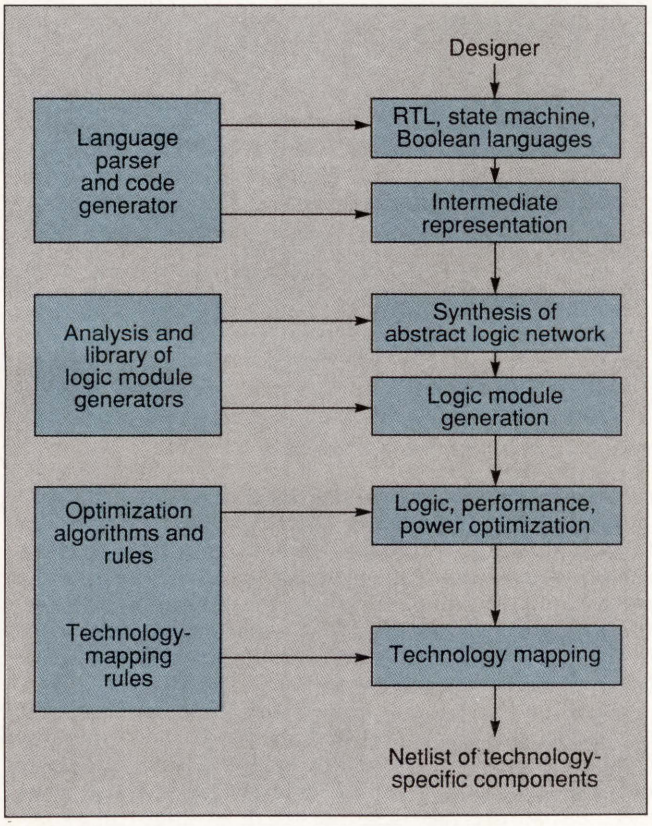

FIGURE 2. The flow of logic synthesis includes several tools and representations of the design.

Logic synthesis converts such high-level logic specifications into detailed logic descriptions. These final descriptions contain the primitives in a particular cell-based technology. In the case of gate arrays and standard cells, the library of primitives consists of specific gates, such as AND gates and flip-flops. More advanced libraries, as found in silicon compilation systems, include higher-level components like adders, ALUs, multipliers, RAM, ROM, and PLAs.

Logic synthesis systems run through a series of steps that include language parsing of the design input, logic module generation, logic optimization, power consumption optimization, and technology mapping (Figure 2). The element first entered into a system is the logic specification (which, as noted above, may take several forms). The input is processed by a parser, which constructs an intermediate representation that can be analyzed by the software tools, which convert it into an abstract logic network.

A logic network can also be arrived at through schematic capture and then entered into a logic synthesis system. One of the benefits of silicon compilation is that it allows a user to capture designs that contain high-level, parameterizable cells (Figure 3). The resultant network consists of generalized logic functions, arithmetic functions, and memory elements.

Synthesis then proceeds to generate the logic modules for all of the higher-level functions. (Logic module generation is a very important aspect of synthesis and is discussed later in more detail.)

At this point, the logic synthesis tool optimizes the logic, performance, and power consumption. This important step creates a schematic of the synthesized logic that minimizes the composite-cost function while attempting to satisfy the performance constraints specified by the user. (Figure 4 shows a portion of an automatically generated schematic of the logic that was synthesized from the input in Figure 3.)

The final step is the technology mapping. This procedure begins with the derived logic network and updates it with components from the chosen implementation technology—bipolar or CMOS gate arrays, standard cells, or compiled-cell libraries. Some logic synthesizers combine optimization and technology mapping in a single step.

PARSERS AND GENERATORS

The input for logic synthesis systems contains register-transfer-level (RTL) languages and finite state machine descriptions. Boolean equations are a subset of these descriptions. VHDL is one of the many languages that fall into this category; in fact, it is emerging as a standard language for synthesis, in addition to its role as a behavioral modeling language. The input languages describe how a circuit functions. A parameterized ALU description in the SCS logic description language, for instance, would show several aspects of a specification. For example, the functional description could take the form of a list of parameters, say, the width of the ALU (Figure 5). Therefore, this functional description can be used for ALUs with any num-

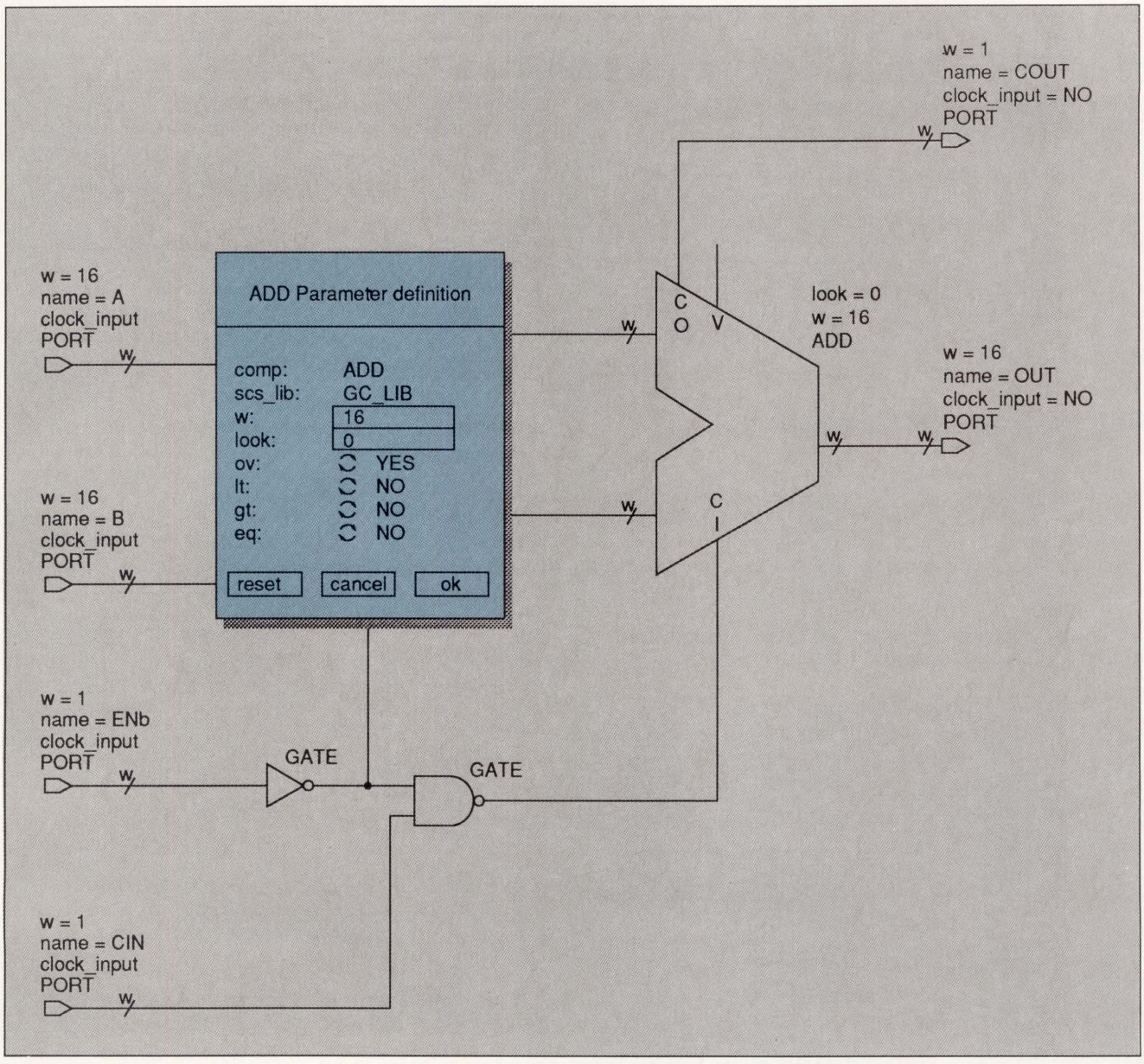

FIGURE 3. Schematic capture within the compilation system combines logic gates with parameterized cells.

ber of bits.

In addition to the data types ("int," "struct," and "list") traditionally found in programming languages, a logic description language supports the data types for externally visible signals ("ports") and internal signals ("sig"). In this example, the op-code signal "OP" controls the function of the ALU. The add op code is 0; the subtract op codes are 1 and 2. The result is latched into an output D latch on CLK.

Such logic descriptions are processed by a parser, which constructs the intermediate parse-tree description that unlike the language description, can be read by the logic synthesis tools. These tools analyze the parse tree and create a network of abstract gates, latches, adders, shifters, and other arithmetic functions. Logic synthesis then continues, generating the logic modules.

A logic module generator (also known as a module or block compiler) is a program that takes a high-level description and from it generates all necessary views of the module for the designer: layout view, simulation view, timing analysis view, and a schematic symbol view for design capture. Module generators can be constructed to produce logic netlists as well.

Logic module generators are very important for logic synthesis. They can represent very-high-level functions and contain user-specified parameters. These generators are developed by expert IC and logic designers whose prowess they capture. ASIC designers then leverage this expertise when capturing the design.

The following example of a multiplier logic-module gen-

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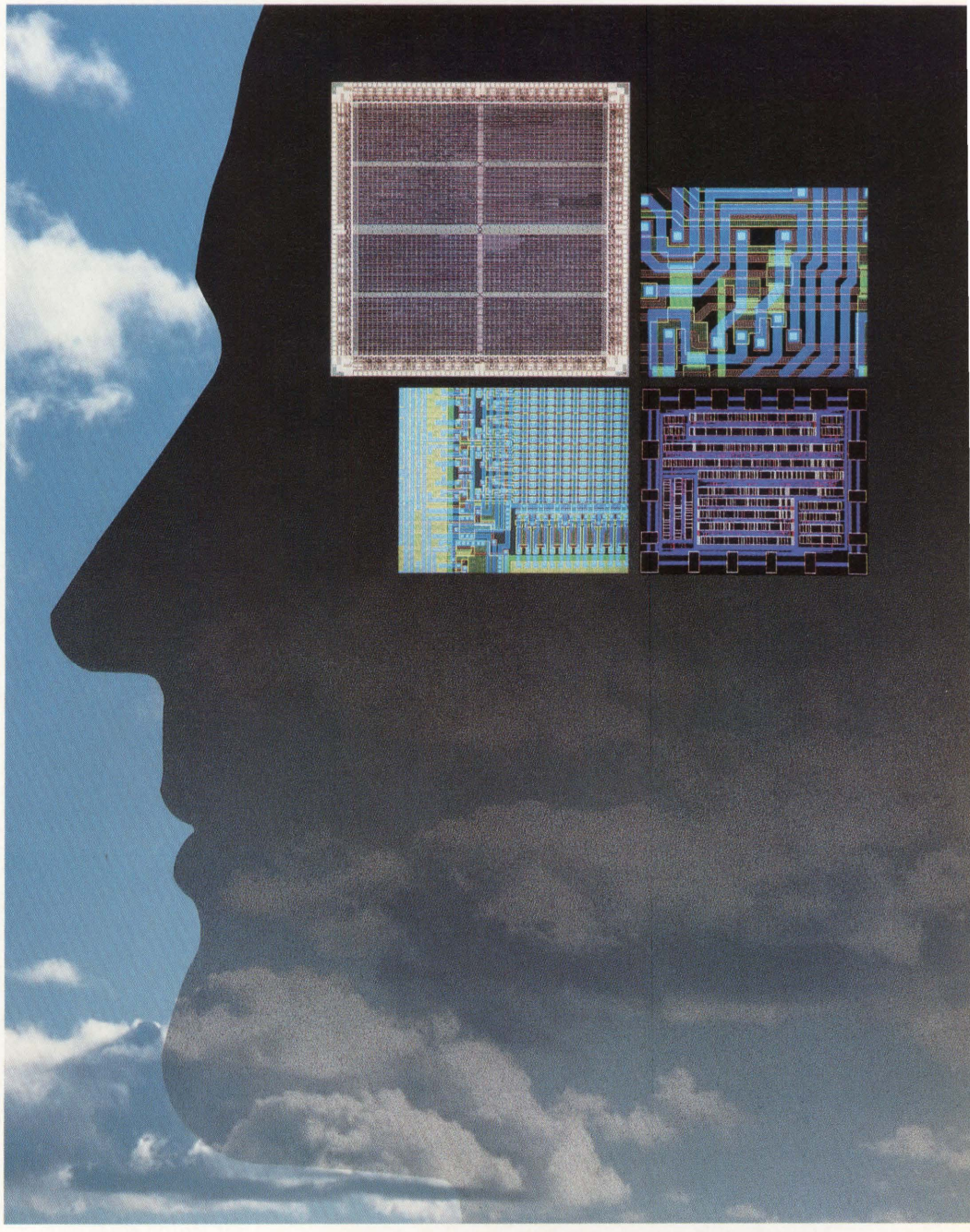

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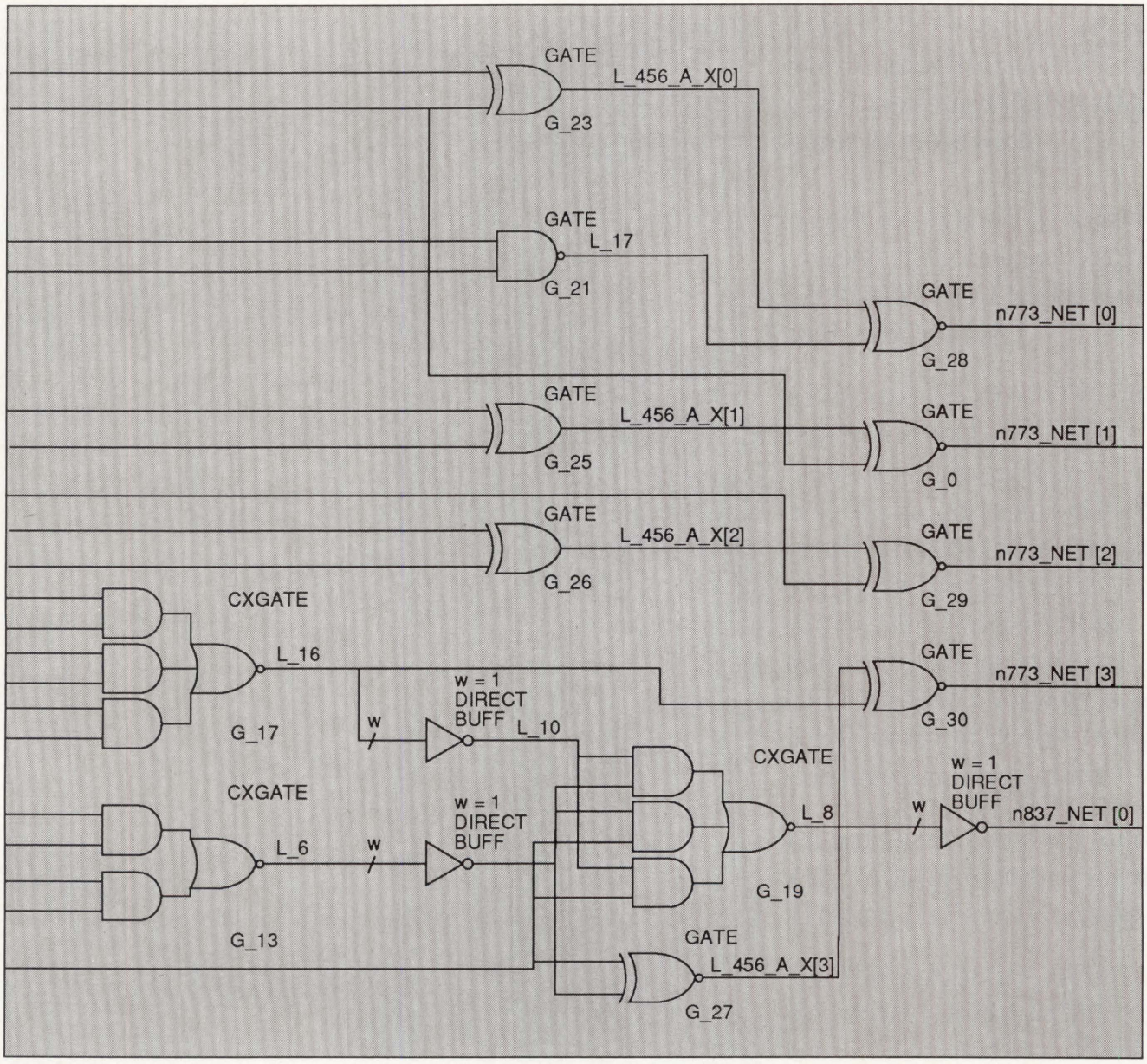

FIGURE 4. The logic synthesizer created this logic from the schematic input in Figure 3. Only a portion is shown.

erator incorporates several user-specified parameters:

```
Func Multiplier (n_bits, m_bits, accumulator)
    int n_bits; /* number of bits for multiplier */
    int m_bits; /* number of bits for multiplicand */
    int accumulator; /* optional accumulator*/
```

This generator creates $n \times m$-bit multipliers with optional accumulators for summing up. It produces a gate-level description of a multiplier with any specific set of parameters, which may range from 2 bits to 64 bits.

Module generator libraries contain parameterized system components like logic gates, adders, counters, data paths, RAM, ROM, PLAs, multipliers, and core microprocessors. The tools for developing module generators consist of interactive graphics editors, specialized languages, simulation and characterization programs, and behavioral- and functional-modeling tools. In particular, logic module generators are best developed by ASIC CAD departments, in a structural modeling language. Such a language has to support all traditional language constructs but must also support logic parameterization and netlist connectivity.

OPTIMIZATION AND MAPPING

Logic and performance optimization takes place once the logic network is constructed from the language parsing and logic module generated. Most optimization techniques are based on algebraic or rule-based methods. Some of them combine the two. The traditional optimi-

```
func alu (width)
    int width;/*inputparameter is the ALU width*/
{
  port CC;              /*carry in*/
  port CLK CLK;         /*clock*/
  port R R[width];      /*input R of variable width*/
  port S S [width];     /*input S of variable width*/
  port Y Y [width];     /*output Y of variable width*/
  port OP OP [3];       /*input op-code for the ALU function*/
  sig Yunl [width];     /*internal unlatched result*/
    /*op-code specification, output is set to one of the cases*/
    Yun) = (select OP'{
        case ): (R + S + C); /* add with carry */
        case 1: ((S − R) − C; /* subtract R from S 8/
        case 2: ((R − S) − C; /* subtract S from R */
        case 3: (R | S); /* logic or */
        case 4: (R & S); /* logic or */
        case 5: (R << 1); /* shift R left */
        case 6: (R∧S); /* exclusive or */
        case 7: (R >> 1); /* shift R right */
    })
    Y = diff( Yunl, CLK ); /* latch result */
}
```

FIGURE 5. The language specification for an ALU shows the use of parameters (width) and data types for I/O signals ("ports") and internal signals ("sig").

zation algorithms, used primarily for PLA and PLD optimization, operate only on two-level logic networks. Multilevel optimization methods are more useful because they can improve sequential circuits as well as combinatorial ones.

Performance optimization is essential for a logic synthesis system. The user wants to specify critical paths to be optimized, timing constraints among signals, and clock cycle duration. To do so, the logic synthesis system must contain a built-in critical-path analyzer that evaluates possible approaches.

Technology mapping produces the final implementation of the desired function in the form of a network of specific library components. For example, the design can be mapped into a bipolar or CMOS gate array, standard cells, or a compiled-cell library. Each of these libraries may contain different logic and memory primitives. Between the libraries, the primitives may have different timing delays, loading constraints, and interconnect constraints. For this reason, a logic synthesis system should combine logic and performance optimization with the technology-mapping information and rules.

SYNTHESIZING LAYOUT

Logic synthesis is a technology for transforming and optimizing a high-level description of a complex function into a netlist of primitive logic gates. Logic synthesis has become important to silicon compilation because it provides an additional mechanism for synthesizing layout for parts of a chip or for an entire chip. This mechanism applies standard-cell placement and routing software to the optimized gate-level netlist. By combining logic synthesis and layout tools in one environment, silicon compilation tools provide a tighter link to layout and allow the designer to leverage the logic optimization in the layout and vice versa.

One example of a combined logic synthesis and standard-cell layout system is SCS's LogicCompiler, a rule-driven system combined with parameterized, standard-cell layout.

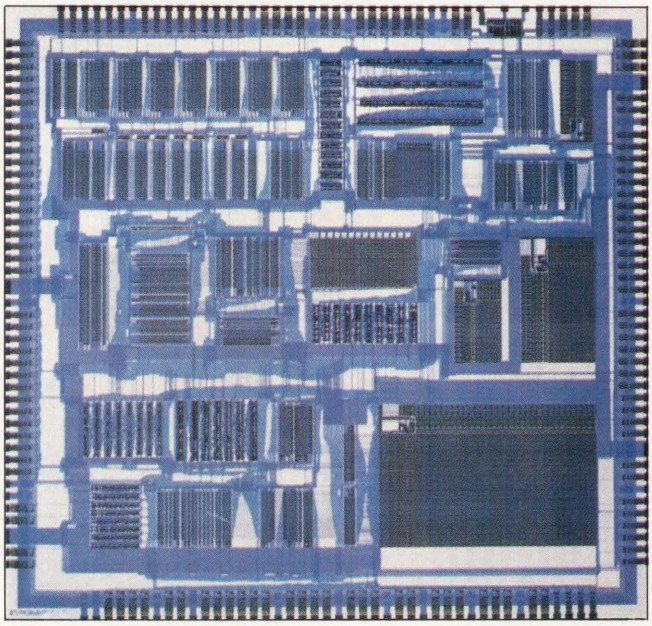

FIGURE 6. This 100,000-transistor RISC processor contains 16 major blocks, 6 built from logic synthesis tools and 10 created by module generators.

The compiler accepts input descriptions in many forms: logic equations, state equations, schematic diagrams, netlists, structural descriptions, and module-generator parameters. Its primary application is those parts of a design that are not inherently highly structured. Random logic, control logic, and smaller arrays can often be significantly reduced in size by efficient optimization.

An illustration of the power of logic synthesis within silicon compilation can be seen in a design that was run through LogicCompiler (Figure 6). Six of the 16 major blocks were prepared with the compiler. The others were designed using specific module generators. This custom RISC processor has about 100,000 transistors. □

ABOUT THE AUTHOR

Misha R. Burich has been vice president of engineering at Silicon Compiler Systems (SCS) since April 1987. He was a cofounder of Silicon Design Labs in Warren, N.J., and its vice president of engineering from January 1984 until it merged with Silicon Compilers Inc. to form SCS. He has been responsible for managing product development. Earlier, Burich taught and worked at Bell Laboratories. He obtained his MS and PhD degrees from the University of Minnesota and his Dipl. Ing. from the University of Belgrade, Yugoslavia, all in electrical engineering.

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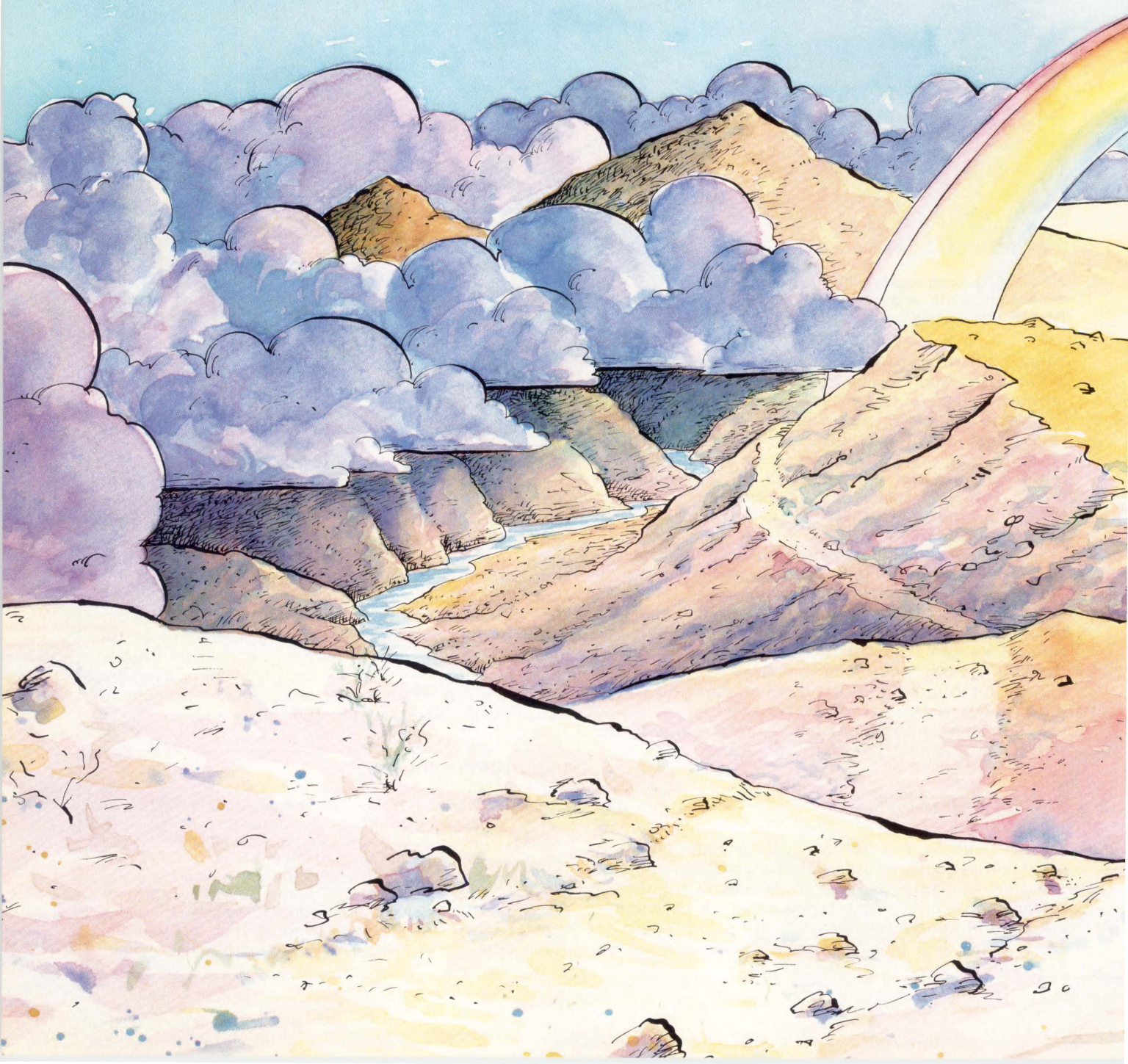

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CIRCLE NUMBER 18

VHDL FOR ASIC DESIGN AND VERIFICATION

Rick Sullivan and Lisa R. Asher, Viewlogic Systems Inc., Marlboro, Mass.

Owing in part to its recent ratification as IEEE Standard 1076–1987, VHDL (VHSIC Hardware Description Language) is rapidly gaining momentum as an industry-standard hardware description language. Its usage will be further accelerated by the recent Department of Defense mandate that all ASIC designs submitted under contract must be accompanied by VHDL models. This mandate is encompassed within Military Standard 454, which states that "ASICs designed after September 30, 1988, shall be documented by means of structural and behavioral VHDL descriptions."

This article describes a rigorous top-down design methodology for ASICs, employing a behavioral subset of VHDL. The goal of this methodology is to enable the production of higher-quality chips with fewer postfabrication design changes. As a by-product, it will produce the behavioral and structural VHDL modules required by Mil-Std-454.

The main benefits of the method are:

- Simplified project planning, achieved by splitting the problem into smaller, independent problems
- The creation of rigorous design specs (VHDL behavioral models), prior to implementation, which can clarify design requirements and lead to cleaner designs
- Identification of design flaws early in the design cycle, when the cost to fix problems is minimal
- The creation of VHDL behavioral models that can be used in system simulations before the ASIC has been designed.

Certain CAE tools are required for this design method. These tools are collectively referred to as the "host CAE system." A good schematic editor is assumed. Other features specific to this design method are highlighted and discussed below; particularly important is the ability to simulate behavioral VHDL models within the ASIC design cycle, as opposed to once at the end of the design.

As an illustration, we will use a circuit that implements a parallel hardware sorting algorithm. This circuit would occupy about 11,000 gates in a typical gate array. Its basic function is to shift in a stream of up to 256 sixteen-bit unsigned integers and shift them out in ascending order.

VHDL SUBSET FOR BEHAVIORAL MODELING

VHDL includes constructs that support diverse design styles (Lipsett, Marschner, and Shahdad, 1986; Barton, 1988 and June 1988), allowing designers to specify structural, data-flow, and behavioral models. This broad coverage of methodologies is necessary because VHDL models must serve as self-contained specifications for design transfer. However, when using VHDL as a design tool, users find that a particular design style employs only a subset of VHDL's features. In fact, when required by contract or design methodology to produce models at a specific level, users must restrict themselves to a defined subset of the language. The VHDL subset described here applies to behavioral modeling. Tools that implement this subset adequately support modeling at the behavioral level, and users who adhere to this subset can be confident that their models lie within the behavioral domain of VHDL.

In general, a VHDL model has two parts: an *entity* declaration and one or more alternative *architecture* bodies. The entity declaration defines a device's external interface, and each architecture body describes one implementation of the entity. An architecture body can include instances of other components and define their logical interconnections, specifying the internal structure of the entity; or it can contain behavioral process statements, defining an algorithm that produces new values for the entity's outputs. Architecture bodies can also contain concurrent signal assignments, which are data-flow constructs that specify new values of output signals as a function of input signal values. These statements, as well as two other kinds of concurrent statements, concurrent assertion statements and concurrent procedure calls, can be represented as semantically equivalent process statements (IEEE, 1988).

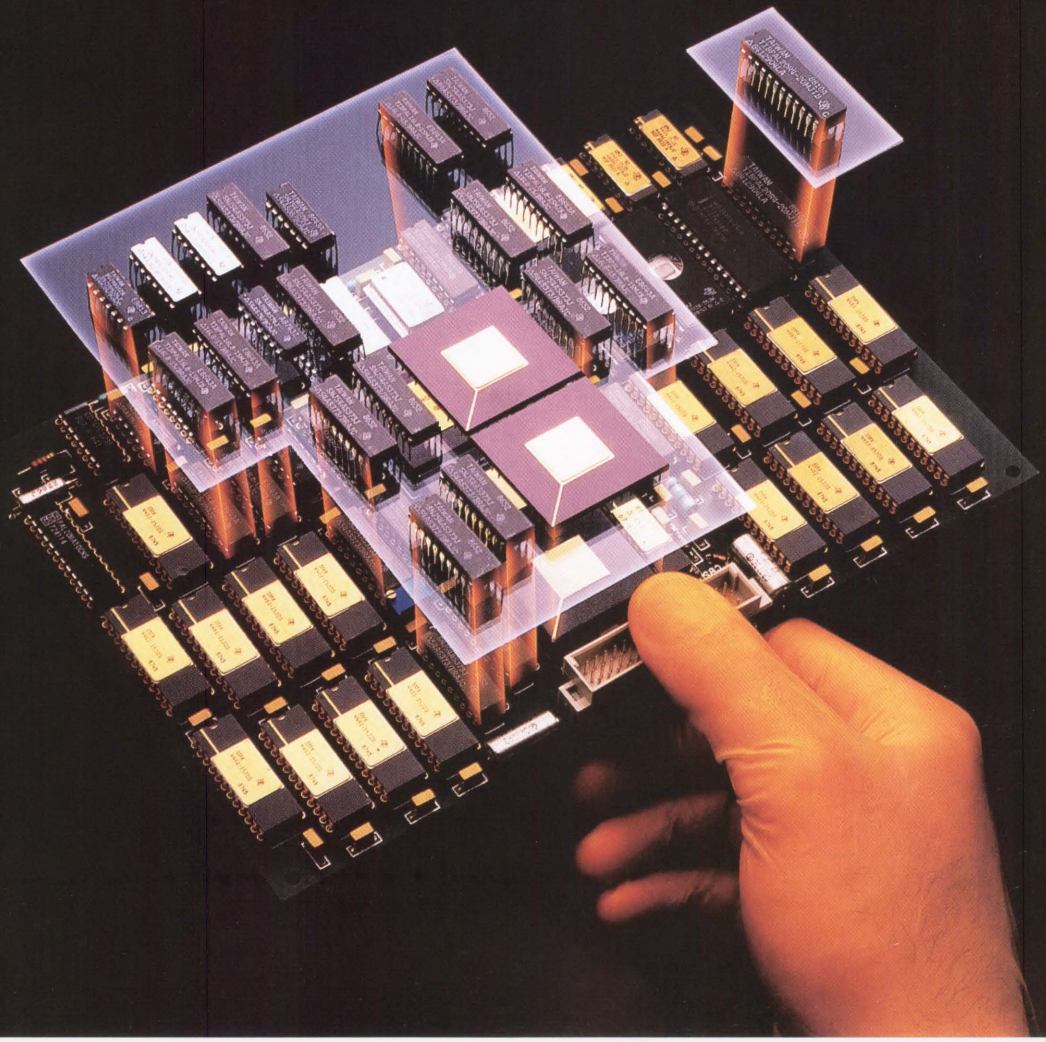
An architecture body may contain these three construct types in any combination. However, a purely behavioral architecture body specifies none of the internal structure of a device; instead, it captures the device's externally visible function, or behavior, at its top level (IEEE, 1988; Barton, June 1988). Since IEEE–1076 stipulates that a behavioral architecture body does not instantiate lower-level

TEXAS INSTRUMENTS REPORTS ON

SYSTEMS LOGIC

IN THE ERA OF

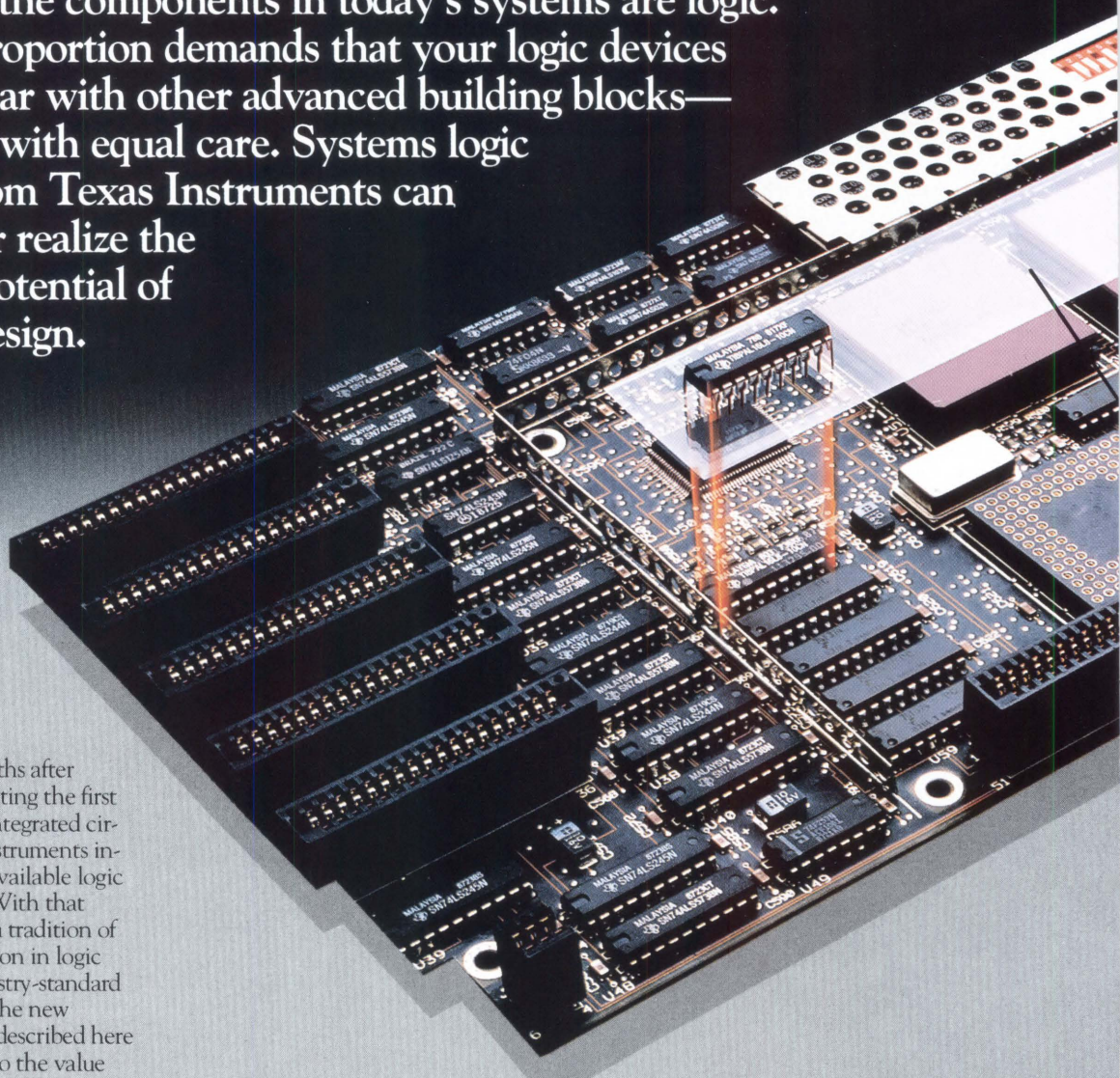
MegaChip TECHNOLOGIES



Systems logic in the Era of MegaChip Technologies:

No system should ever be limited by its to help your design perform at its best.

Up to 65% of the components in today's systems are logic. Such a large proportion demands that your logic devices perform on a par with other advanced building blocks—and be chosen with equal care. Systems logic alternatives from Texas Instruments can help you better realize the performance potential of your system design.



Within months after demonstrating the first working integrated circuit 30 years ago, Texas Instruments introduced a commercially available logic function, an RS flip-flop. With that beginning, TI established a tradition of development and innovation in logic that encompasses the industry-standard SN54/74 Series TTL and the new families of advanced logic described here that can add significantly to the value and performance of your overall system.

For example, for systems that require off-the-shelf flexibility with a degree of customization, TI's Programmable Logic Devices (PLDs) include popular 10-ns PAL® ICs available in high volume. And, to keep pace with today's high-speed microprocessors, TI plans to continue to drive PLD performance to sub-10-ns speeds.

TI's Advanced CMOS Logic (ACL) supports the design goal of high performance combined with low-power operation, while TI's new BiCMOS bus-interface family delivers very high drive current at very low power compared to bipolar circuits.

For systems requiring moderate densities and fast prototype cycle times, TI offers a new series of one-micron CMOS gate arrays. When you need higher levels of integration plus increased design flexibility, TI's one-micron CMOS standard cells provide the means for system consolidation.

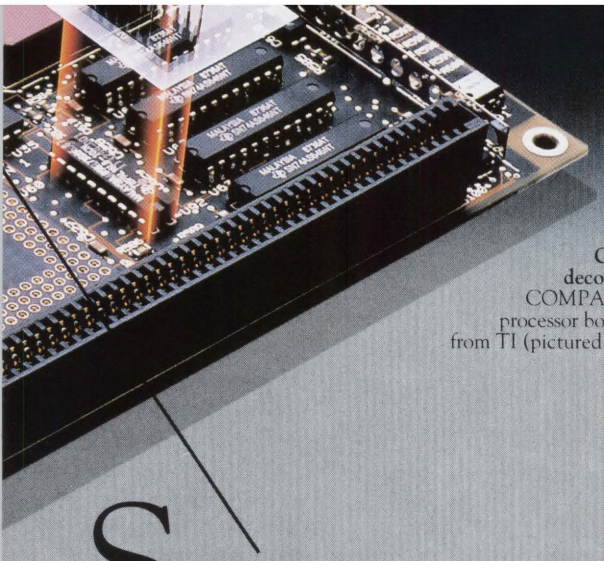
And for military applications, TI offers a wide choice of high-reliability logic functions.

On the following pages are details of what you can expect from TI's range of logic options:

ON THE COVER: Suspended above the board, provided by Rockwell International, Missile Systems Division, are military versions of TI advanced logic devices.

TI's MegaChip Technologies

Our emphasis on high-density memories is the catalyst for ongoing advances in how we design, process, and manufacture semiconductors and in how we serve our customers. These are our MegaChip™ Technologies, and they are the means by which we can help you and your company get to market faster with better products.



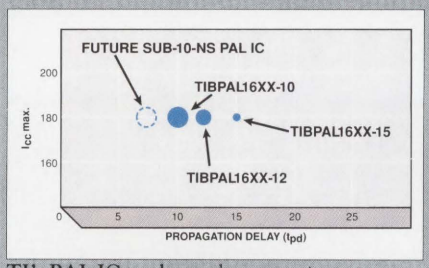
Contributing significantly to fast address decoding in speed-critical paths of the COMPAQ DESKPRO 386/20™ personal computer processor board are two TIBPAL16L8-10 PAL circuits from TI (pictured above a segment of the board).

Speed your system to market with TI's superfast PLDs.

PLDs are a functional alternative to standard logic ICs and gate arrays or standard cells.

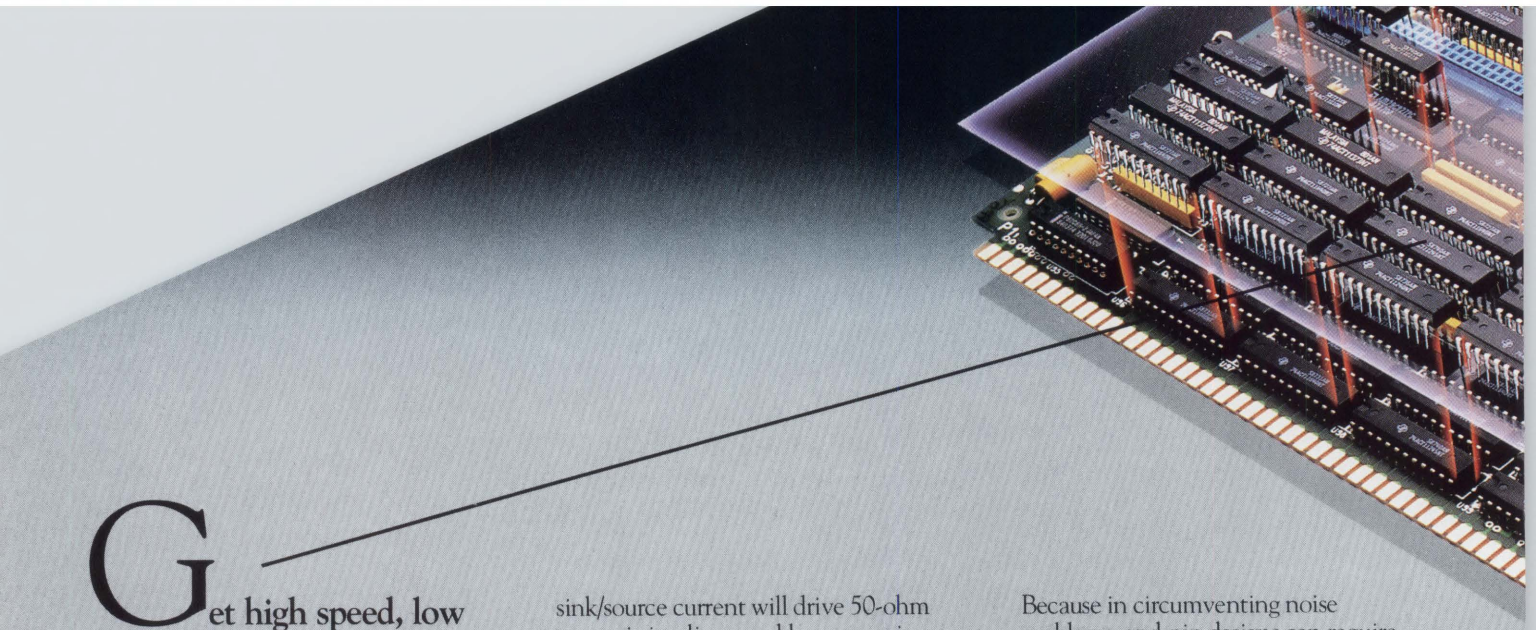
Because TI's PLDs are off-the-shelf items you program yourself, you avoid the longer design cycle times of custom ICs and move on to market faster. These PLDs offer very attractive performance advantages. Consider these:

- **TIBPAL16XX-10 PAL ICs** from TI deliver a 10-ns propagation delay and are available in quantity. Clock-to-Q time is 8 ns, and output-registered toggle frequency is 62.5 MHz. IMPACT-X™ technology gives these PAL ICs their superior speed; they are well suited for use with high-speed processors such as the Motorola 68030, the Intel 80386, and RISC-based architectures. The 10-ns performance brings a higher level of integration to speed-critical paths.
- **TI's TIEPAL10H16P8-6 IMPACT™ ECL PAL circuit** delivers even faster operation: 6-ns propagation delay max. You can now streamline conventional ECL designs by consolidating several discrete components into a single custom function.
- **TI's new 7-ns Programmable Address Decoder** is intended to help you squeeze more performance out of memory interface systems. By performing address decoding much faster than conventional PAL architectures—in 7 ns—the TIBPAD16N8-7 allows you to take advantage of the new processors to increase overall system performance.
- **TI's 50-MHz Programmable State Machines (PSMs),** TIB825S105B (16 x 48 x 8) and '167B (14 x 48 x 6), are ideal for use in high-performance computing, memory interface, telecommunications, and graphics. These PSMs may be used to implement custom sequential logic designs such as peripheral I/O controllers and video-blanking controllers.
- **The TIBPAL22VP10-20,** with a 20-ns delay, is 20% faster than the competition's "A" version and much more flexible. A programmable output macrocell allows two extra, exclusive output configurations, for a total of six.
- **TI's TICPAL16XX Series 20-pin CMOS PAL ICs** are the cure for power problems. They operate at virtually zero standby power and are reliable, high-performance replacements for conventional TTL and HCMOS logic. The devices can be erased and reprogrammed repeatedly.



TI's PAL IC road map shows consistent power and consistently higher speeds, with even faster versions on the way.

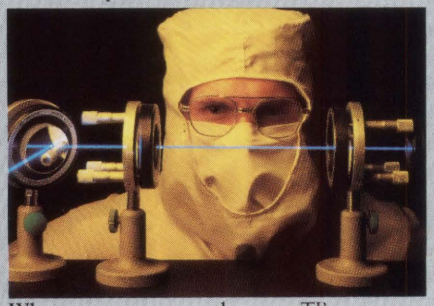
Turn page for more information



Get high speed, low power, and low noise with TI's broad ACL family.

It's an extensive family that includes gates, flip-flops, latches, registers, drivers, and transceivers. It's a readily available family in DIP and SOIC packages. It's TI's high-performance EPIC™ ACL family, bringing with it an important bonus—major reductions in noise.

Family speed is comparable to advanced bipolar 54/74F; 24 mA of sink/source current will drive 50-ohm transmission lines; and low power is characteristic of TI's EPIC technology. All this with "ground bounce" substantially reduced compared with end-pin ACL. The reasons are innovative packaging and a circuit-design technique called OEC™ (Output Edge Control) which softens the transition states that cause simultaneous switching noise. In fact, EPIC ACL noise levels are typically 10% less than those of bipolar devices.



When every nanosecond counts, TI's new high-performance ACL family can help you significantly improve system speed.

The rapidly increasing customer acceptance of TI's ACL family confirms its noise-reduction advantages and its ease of use.

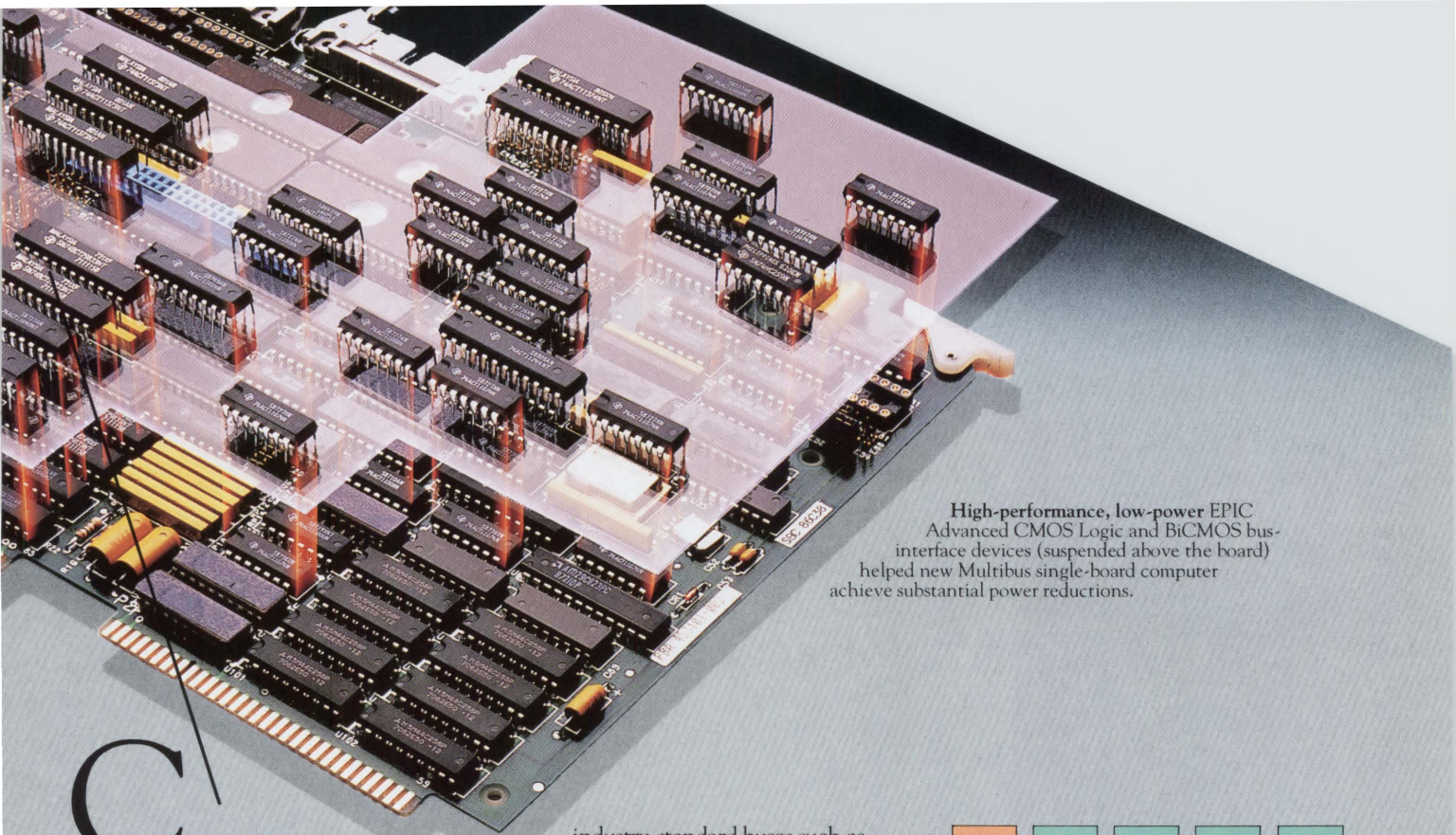
System design advantages

A unique "flow-through architecture" simplifies board design, layout, and troubleshooting. Inputs surround power pins on one side, outputs on the other, and control pins are strategically located at the package ends.

From a systems perspective, TI's arrangement offers the lowest-cost design when compared to end-pin ACL. Because in circumventing noise problems, end-pin designs can require additional components that take up to 32% more board area and slow system performance.

There are 146 functions, in both AC and ACT versions, currently announced in TI's ACL family, including such innovative, highly complex functions as advanced transceivers, line drivers, latches, feedback registers, multiplexers, and counters.

This ACL family, developed in cooperation with and supported by Philips/Signetics, fully meets JEDEC industry-standard No. 20 specifications for Advanced CMOS Logic.



High-performance, low-power EPIC Advanced CMOS Logic and BiCMOS bus-interface devices (suspended above the board) helped new Multibus single-board computer achieve substantial power reductions.

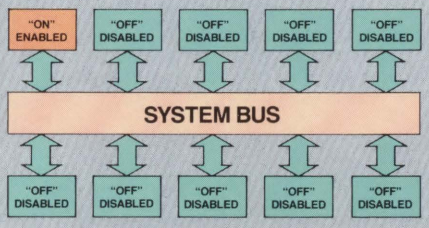
Cut power, not speed or drive, with TI's BiCMOS bus-interface ICs.

This new family is a simple, effective means to reduce system power consumption without compromising advanced performance.

As the BiCMOS name implies, TI combines bipolar IMPACT and CMOS processing to achieve switching speeds comparable to advanced bipolar products and provide the 48/64-mA drive current needed for high-capacitive loads and backplanes. In particular, family members meet the drive requirements of industry-standard buses such as Multibus® and VMEbus™

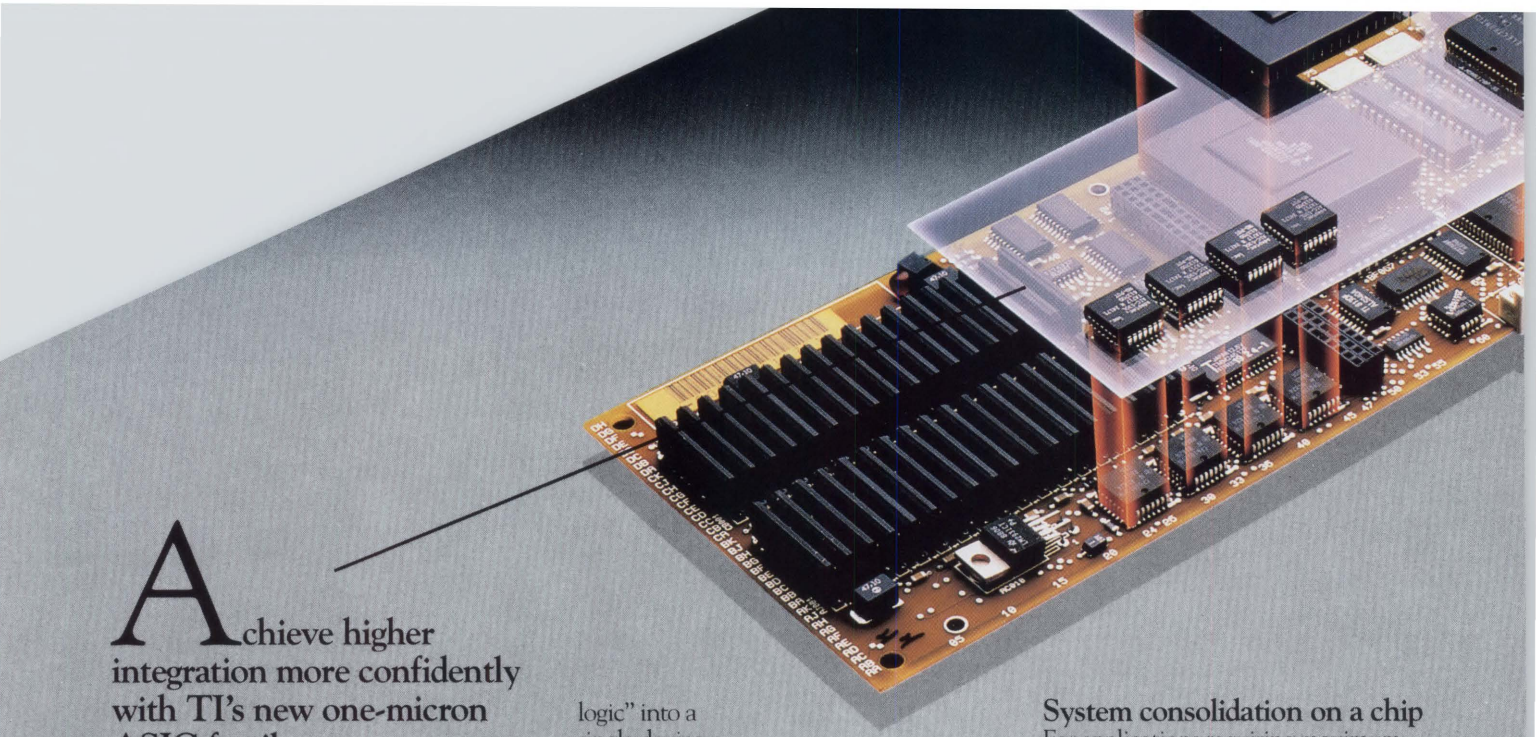
In addition, TI's BiCMOS devices can reduce disabled currents by 95% and active currents by 50%-80% compared to bipolar equivalents. Result: System IC power savings can be more than 25%.

There are more than 60 functions comprising TI's BiCMOS bus-interface family. Included are 8-, 9-, and 10-bit latches, buffers, drivers, and transceivers—a wide choice that means you can easily find what you need to implement high-performance bus-interface designs.



An innovative circuit design in TI's BiCMOS bus-interface logic helps lower disabled currents. This is key to overall power savings because in a typical bus network only one device is enabled at a time.

Turn page for more information



Achieve higher integration more confidently with TI's new one-micron ASIC family.

Now, you can integrate more of your systems logic using TI's new one-micron CMOS ASIC (application-specific integrated circuit) family—the TGC100 Series gate arrays and the TSC500 Series standard cells. Each offers different degrees of design flexibility and system integration. The result is significantly reduced component count which cuts board size and system cost while improving reliability and performance.

And TI is supporting the family with comprehensive kits that help minimize design cost, risk, and time by providing a comfortable, easy-to-use design environment.

Efficient logic consolidation

Using TI's new TGC100 Series gate arrays, you can sweep major chunks of "glue logic" into a single device while realizing fast design and prototype cycle times. Array densities currently range to more than 8K usable gates and 142 bond pads; the Series will be extended to more than 16K usable gates and 216 bond pads in a major production release planned for late 1988. Prototype delivery is typically two to three weeks from approval of postlayout simulation results.

The TGC100 Series Design Kit gives you complete autonomy and control over the design process. It is a comprehensive set of the tools required for successful gate-array design and validation *(see last page for details)*.

Standard packages for the TGC100 Series range from 28-pin DIPs to 84-pin PLCCs, with optional packages up to 144 pins.

System consolidation on a chip

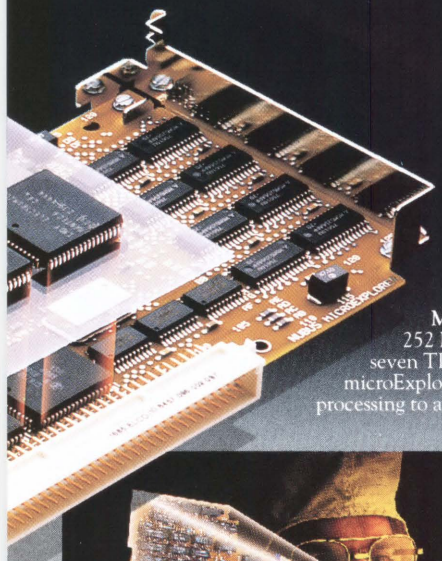
For applications requiring maximum design flexibility and higher levels of integration, TI has disclosed its third-generation standard-cell family, the TSC500 Series.

Complex system designs can be implemented using a growing core of basic SSI/MSI functions, as well as scan cells for testability and MegaModule™ building blocks such as register files. FIFOs, bit-slice family functions, RAM, and ROM are other aids to implementation. Output cells with drive capability up to 64 mA are available.

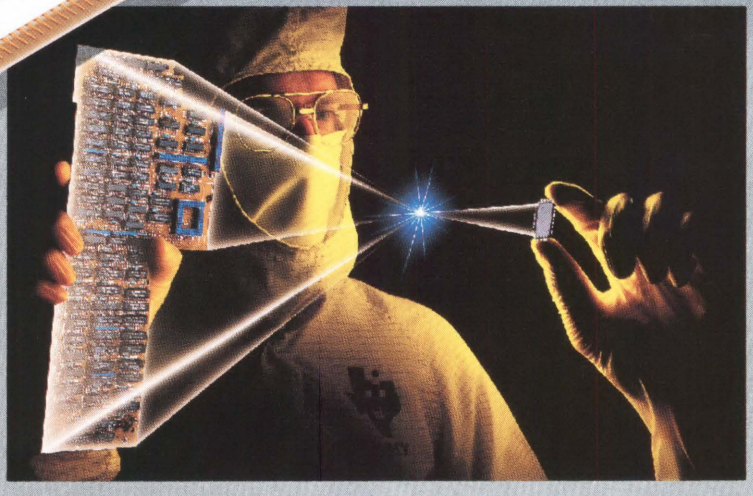
Package options include conventional through-hole DIPs, surface-mount PLCCs, and plastic quad flatpacks (QFPs) in both JEDEC and EIAJ standards, as well as high-pin-count plastic pin-grid arrays.

Both the TGC100 and TSC500 Series have a typical propagation gate delay of

logic. TI offers advanced logic families



Major logic consolidation, the equivalent of 252 MSI and LSI devices, was possible using the seven TI ASIC functions shown above the microExplorer™ board which brings symbolic processing to a MacIntosh II® desktop computer.



480 ps for a two-input NAND gate with a fanout of three; flip-flop toggle rates range up to 208 MHz. Both series offer output and bidirectional buffers with variable slew-rate control. And both series are fabricated in TI's high-performance EPIC process.

Apply TI's advanced logic to improve the performance of military systems.

Among TI's broad selection of logic devices produced to military requirements is a large PAL family. Propagation delays as fast as 15 ns are available over the military temperature range. The introduction of a 12-ns, 20-pin PAL circuit is planned, as well as military versions of the TIB825S105B and '167B Programmable State Machines.

TI is offering military counterparts selected from its ACL family, as well as 54F functions. Soon to come will be the BiCMOS family of bus-interface functions.

Included among TI's lineup of military ASICs are versions of the one-micron TGC100 Series gate arrays discussed at left, as well as two-micron standard cells.

TI's logic devices are among the more than 800 military functions offered compliant to MIL-STD-883C, Class B. Of this total, TI provides more than 200 to DESC-standard military drawings and is qualified to supply 285 JM38510 Class B devices (QPL 75).

THIRTIETH ANNIVERSARY
1958 1988
INVENTION OF INTEGRATED CIRCUIT

Milestones in Innovation

TI's tradition for milestone innovations extends from the infancy of semiconductor technology into the MegaChip Era. Among the major highlights:

- First commercial silicon transistor (1954)
- First commercially produced transistor radio (1954)
- First integrated circuit (1958)
- First integrated-circuit computer (1961)
- First hand-held calculator (1967)
- First single-chip microprocessor (1970)
- First single-chip microcomputer (1970)
- First single-chip speech synthesizer (1978)
- First advanced single-chip digital signal processor (1982)
- First video RAM (1984)
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TEXAS INSTRUMENTS

components but is composed of process statements and concurrent statements with equivalent process statements, a VHDL subset that applies to behavioral modeling includes process statements to capture component behavior, architecture bodies to enclose process statements, and entity declarations to define interfaces between behavioral models and the surrounding structure.

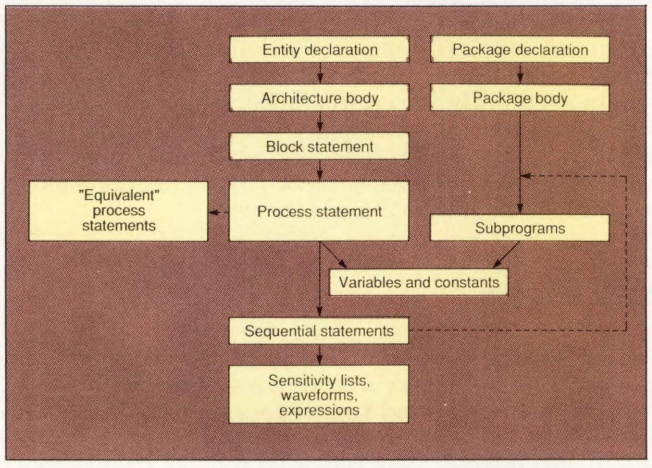


FIGURE 1. Grammar tree for the behavioral subset of VHDL.

The subset presented here is derived from the VHDL grammar (IEEE, 1988) by extracting the process statement and its components, plus all enclosing constructs necessary to build a complete design entity description (Figure 1.) Traversing the grammar tree down from the process statement to its leaves, we include sequential statements and constant and variable declarations. Traversing the tree up from the process statement to the root, we extract architecture bodies and entity declarations. Signal declarations are included to allow communication between processes and between behavioral models and enclosing structure. For convenient packaging of commonly used algorithms, subprograms and packages also are added.

Within this subset, a behavioral model consists of an entity declaration and one behavioral architecture body.

For the sorting chip, the entity declaration declares the model's name, "sorter," and its input and output pins, or ports (Figure 2). This model has two 16-bit data buses, "din" and "dout"; two clock lines, "phi1" and "phi2"; and four control lines.

The architecture body of such a behavioral model consists of a set of one or more process statements. These processes execute concurrently, suspending and resuming execution in response to events on signals and conditions within the simulation.

Each process statement defines a sequential algorithm that calculates new values of its output signals as a function of the values of its input signals over time. This algorithm is represented by a series of executable statements, including *wait* statements; *if*, *case*, and *loop* statements; procedure calls; assertion statements; and variable and signal assignments.

The architecture body for the sorter ASIC contains two concurrent statements (Figure 3). The first, labeled "check," is a concurrent assertion statement that monitors the control signal "newword" and flags any attempt to use a feature that has not yet been implemented. This

```
entity sorter is
  port (din:      in vlbit_1d(15 downto 0);     -- data in
        dout:     out vlbit_1d(15 downto 0);    -- data out
        phi1, phi2,                             -- clocks 1 and 2
        reset,                                  -- reset control signal
        read,                                   -- sort dir'n ctl signal
        double,                                 -- double-word ctl signal
        newword: in vlbit);                     -- word boundary ctl signal
end;
```

FIGURE 2. Entity declaration for the sorter ASIC.

```
architecture behavior of sorter is
  constant width:      integer := 16;  -- width of words to sort
  constant length:     integer := 265; -- number of words to sort
begin
--
--concurrent assertion statement:
--flag attempt to use unimplemented feature after initialization:
  check: assert not (double = '1' and now > 0ns)
                  report "Double-word sorting is not implemented.";
--
--main sorting process:
--insert each new word in order in data bank and emit sorted words:
  main: process
    variable data:      vlbit_2d(0 to length - 1, 0 to width - 1);
                        --data words in process of sort
    variable inwix,
      outwix:integer := 0;-- word indices for input, output
  begin
wait until newword = '1';-- wait for new word boundary
    for clockperiod in 1 to width - 1 loop
      wait until phi1 = '1'; wait until phi2 = '1';
    end loop;                           -- wait for last clock period
    wait until phi1 = '1';              -- wait for start of clock period
    dout <= data (outwix);              -- emit next data word
    wait until phi2 = '1';              -- wait for second phase
    if reset = '1' then
      init: for wix in 0 to length - 1 loop
        data (wix) := X"FFFF";          -- initialize data bank
      end loop;
      inwix := 0;                       -- initialize data indices
      outwix := 0;
    else
      if read = '1' then                -- increment input index and
        inwix := (inwix + 1) rem length;
        insert (data, inwix, din);      -- insert next data word in order
      else                              -- increment output index
        outwix := (outwix + 1) rem length;
      end if;
    end if;
  end process;                          -- return to top of process
end behavior;
```

FIGURE 3. Behavioral architecture body for the sorter ASIC.

concurrent statement is equivalent to a process statement consisting of one sequential assertion statement; it becomes active whenever the signal "double" changes and then suspends until another change occurs. The second concurrent statement, labeled "main," is a process statement that implements the ASIC's sorting function. In response to events on the model's input control signals, this process loads data words from the input data bus and returns the numbers in sorted order on request.

The sorter chip requires a rising edge on its "newword" signal, followed by one clock cycle for each bit of its data lines, to load or emit one data word; this scheme allows the data to be converted internally into a serial bit stream. Since a behavioral model of this chip need not mimic its internal operation, it can handle data bits in parallel.

The main process watches the clock and "newword" signals, waiting for the final clock period following the rising edge of "newword." At this point, it emits the least number in its "data" array. Then, if a reset has been requested, it initializes its data array and input and output indices. Otherwise, if the "read" line is high, it inserts the number on its data input line, in sorted order, into the "data" array; if the "read" line is low, the process increments its current output index to address the next-greatest data word.

As the design evolves, more accurate timing information may be added to the model, as well as checks for input timing and data errors.

Process statements may invoke subprograms, which may be declared within packages and shared by behavioral models. Subprograms contain the same sequential statements as are allowed within processes. The behavioral model "sorter" calls a procedure named "insert" (Figure 4), to insert a number into its data array.

This model of the sorter ASIC accurately captures its behavior without specifying its structural implementation. The use of high-level programming constructs to describe its operation allows a brief and straightforward specification of its function.

Although debugging a behavioral model of a complex ASIC is not a trivial task, it is easier than verifing an equivalent structural model. Designers can detect and correct functional design flaws at this stage, before expending the considerable effort required to specify a full structural implementation. To facilitate verification of behavioral models, a VHDL simulator should provide an accessible debugging environment, in which users can interactively control simulation, set breakpoints, display and modify variables and signals within models, and so on.

After verification, a behavioral VHDL model can be used as a standard to verify subsequent structural implementations created during the process of top-down design. It can also be used as a high-performance library component for board- and system-level designs that include an ASIC even before the chip is completely designed. Finally, since it is written in VHDL, it serves as a portable simulation model and functional specification of the ASIC.

```
procedure insert     (variable data:     inout    vlbit_2d(0 to
                                                  255, 0 to 15);
                     constant size:      in       integer;
                     constant din:       in       vlbit_vector) is
  variable wix:          integer;
begin
  -- find location for new data word, shifting greater words up:
  wix := size - 1;
  while wix /= 0 and data(wix - 1) > din loop
    data(wix) := data(wix - 1);
    wix := wix - 1;
  end loop;
  -- insert new data word in correct location:
  data (wix) := din;
end insert;
```

FIGURE 4. Insert procedure for the behavioral model of the sorter ASIC.

VHDL TEST BED

After the top-level behavioral model is written and debugged, the next step is to create a test bed—essentially a set of input patterns and expected output responses. Test beds are usually written in the stimulus language of the simulator; the DOD, however, will probably require that they be written in VHDL (U.S. Government, 1998).

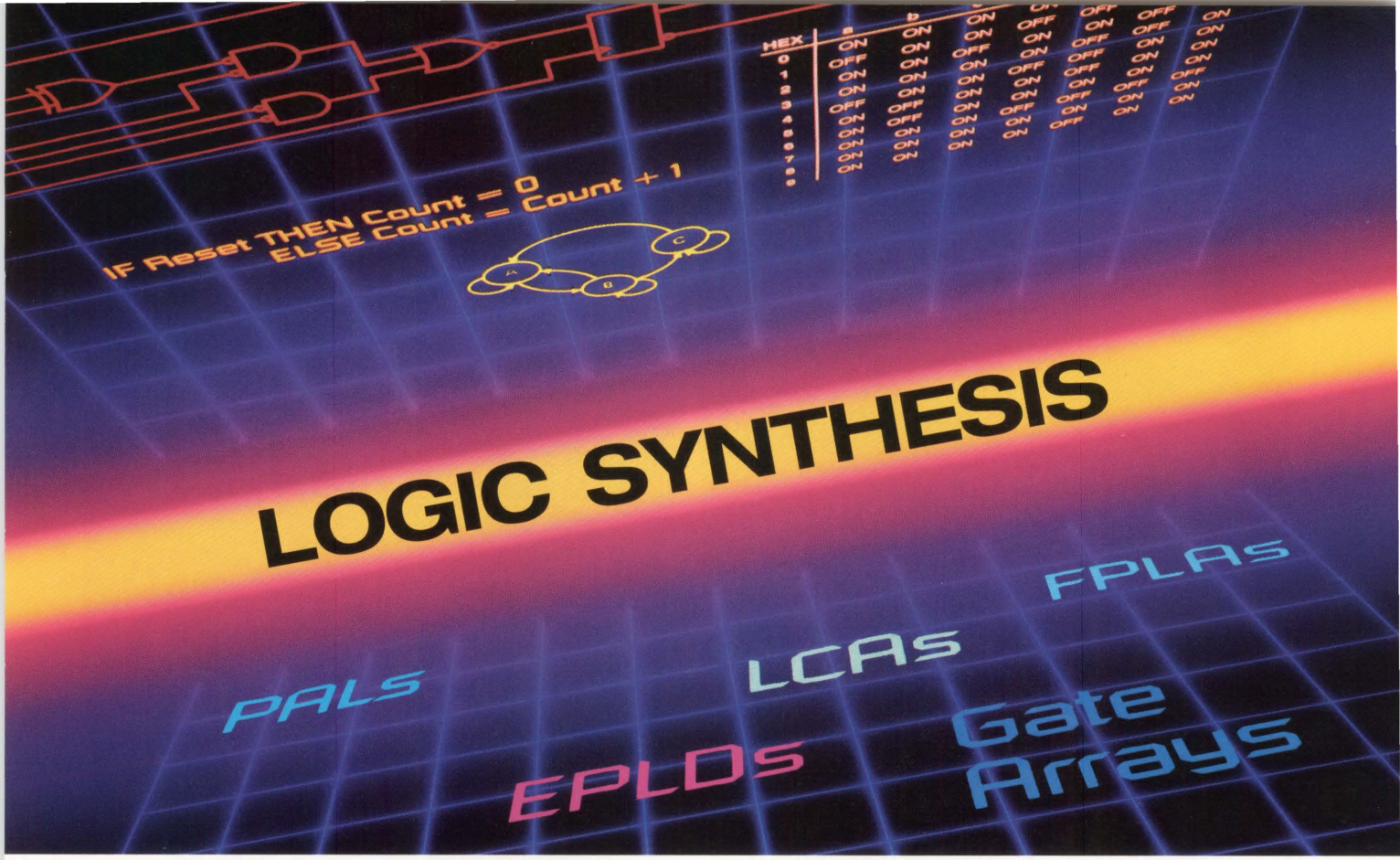
Besides inherent portability, there is another benefit of coding test patterns in VHDL: it is a powerful language for generating and interpreting timed data. For example, few simulators allow the conditional application of input stimuli based on current or previous output values. This capability to perform "handshaking" with the circuit under test is easily implemented in VHDL and is important for tests that drive asynchronous devices—for instance, bus or peripheral controllers.

Another illustration of the flexibility of VHDL as a test language is its ability to represent timing relationships parametrically. An example of this is illustrated by the sorter chip timing diagram (Figure 5). The two nonoverlapping clocks, "phi1" and "phi2," are characterized by the period, "P," and the positive-going pulse width, "PHI_PW." The phase relationship between the pulses, "PHASE," is specified as a fraction of the period. A third nonoverlapping pulse, "NEWWORD," appears at the beginning of every sixteenth period and marks the start of a shift-in or shift-out operation. This pulse is characterized by its delay from the start of the period "NEWWORD_DLY" and by its pulse width, "NEWWORD_PW." The period of the "NEWWORD" pulse is a function of the clock period, "P."

These timing relationships are defined in the VHDL test bed for the sorter circuit (Figure 6). The independent timing variables "P," "PHI_PW," and "NEWWORD_PW" are defined as constants of type "time." The concurrent statements in the "timing" block generate the signals shown in Figure 5.

The exact timing of the waveforms can be changed by modifying the constants without changing the expressed relationships. For example, the frequency can be changed easily without affecting the phase relationship between "phi1," "phi2," and "newword."

The remainder of the sorter test bed is coded in the "test" process of Figure 6. The three steps are initializing the circuit, shifting in the words to be sorted, and shifting out and checking the sorted data.



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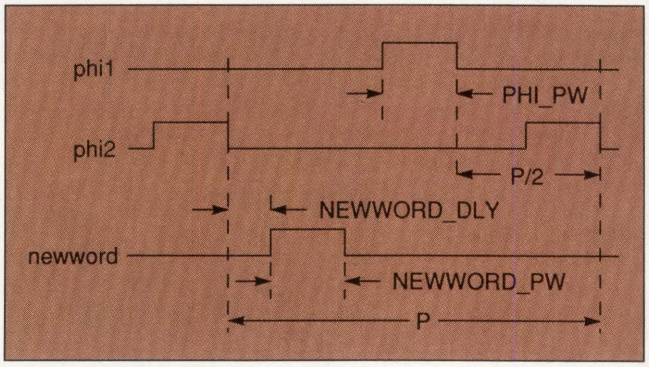

FIGURE 5. Timing diagram for the sorter's clocking sceme.

Initialization consists of asserting the "reset" and "read" lines and waiting for 16 cycles ("NBITS" * "P"). This procedure sets all internal register values to hexadecimal FFFF (see Figure 2 again).

During the shift-in operation, words are presented to the sorter at the start of every sixteenth cycle. This cycle is marked by the "newword" pulse, which indicates that a new word is available for shifting in. The *for* loop iterates through the 256 words ("NWORDS") to be sorted. Each word is retrieved by the "getval" procedure and applied to the "din" data inputs. The *wait* within the loop ensures that each word is presented on a 16-cycle boundary.

The "getval" procedure can be implemented in a variety of different ways. One obvious approach is to read data values from a file.

To enter the shift-out mode, the "read" line is reset and another *for* loop is entered. Each iteration of the *for* loop waits 16 cycles for a full word to be shifted out. It then calls the "checkval" routine to compare the sorter output, "dout," with the expected output. If a discrepancy is found, an error message is printed.

The existence of a good test bed greatly simplifies subsequent design iterations, because each major refinement can be tested against the original test bed. If errors are introduced, the test bed will automatically flag them.

There are several steps remaining in the top-down design methodology (Figure 7). The first design refinement consists of drawing a block-level schematic. This block diagram identifies major components or subsections of the design and interconnections. Design teams can now be formed to work independently on various subsections.

To avoid unintended departures from the original design spec (that is, the top-level behavioral VHDL model), each design team must regularly simulate design refinements against the test bed. Furthermore, design teams must be able to do so without interfering with each other. For example, if design team 1 introduces a major bug into its portion of the design, design team 2 should not be prevented from simulating its own design refinements against the test bed.

To achieve this degree of independence, each design team must write a behavioral VHDL model for its own portion of the ASIC. These models are tied together with the block-level schematic and simulated against the test bed. If the test bed detects discrepancies, the bugs must be isolated and fixed. To do that quickly, the host CAE system should support a good interactive debugging environ-

```
architecture action of driver is
  constant PHI_PW:          time    := 100ns;
  constant P:               time    := 400ns;
  constant PHASE:           time    := P/2;
  constant NEWWORD_DLY:     time    := (P - SKEW -
                                        PHI_PW)/3;
  constant NEWWORD_PW:      time    := 30ns;
  constant NBITS:           integer := 16;
  constant NWORDS:          integer := 256;
begin
--
--
  timing: block
    begin
    phi1        '0' after PHI_PW when phi1 = '1' else
                '1' after P - PHI_PW when phi1 = '0' else
                '1' after P - SKEW - PHI_PW;
    phi2        '0' after SKEW when phi1 = '0' else
                '1' after SKEW when phi1 = '1' else
                '0';
    newword     '0' after NEWWORD_PW when newword = '1' else
                '1' after NBITS * P - NEWWORD_PW
                    when newword = '0' else
                '1' after NEWWORD_DLY;
  end block timing;
--
-- setup test
--
  test: process
    begin
--
-- initialization
--
    reset <= '1';
    read <= '1';
    double <= '0';
    din <= b"0000000000000000";
    wait for NBITS * P;
--
-- load initial data
--
    reset <= '0';
    for nword in 1 to NWORDS loop
      nextval(nword, din);
      wait for NBITS * P;
      end loop;
--
-- shift out data
--
    read <= '0';
    for nword in 1 to NWORDS loop
      wait for NBITS * P;
      checkval(nword, dout);
      end loop;
    wait;
  end process init;
end action;
```

FIGURE 6. Test bed for the sorter ASIC.

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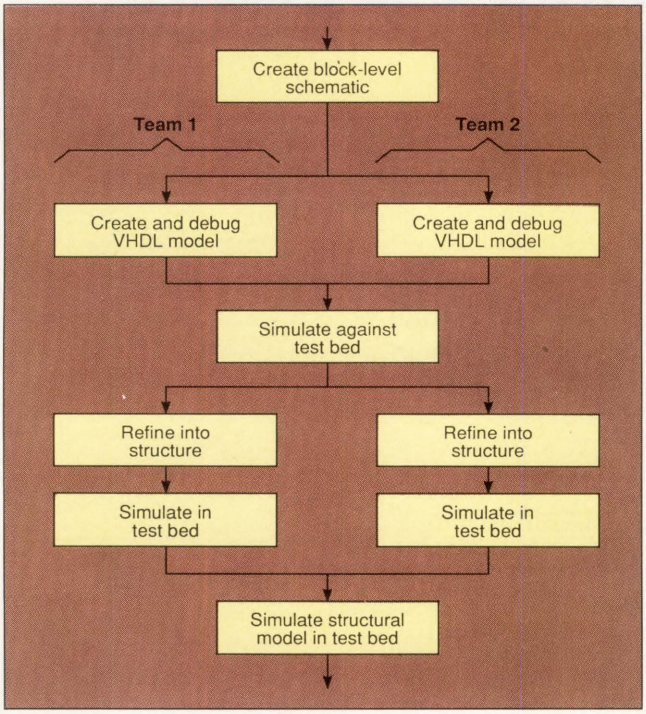

FIGURE 7. Top-down design verification flow.

ment with graphical presentation of the output data.

Once each design team has working behavioral models in place, it can begin to refine its portion of the design into a more detailed structure without affecting other design teams. Each team simulates its own design refinements within the context of the test bed and the verified VHDL models produced by the other teams. Thus each team simulates its own design at a detailed level, while the remainder of the design is simulated behaviorally.

Each team produces a schematic depicting a full structural implementation of the design in terms of the target foundry's ASIC cell library. If the design team has followed the methodology, the schematic is guaranteed to simulate correctly within the context of the test bed and the validated VHDL models from other teams.

STRUCTURAL SIMULATION

The next step is to integrate the structural models and simulate the entire chip at the foundry-cell level. To support this step, the host CAE system must be capable of substituting structural models for the VHDL models in the top-level schematic (see Figure 5 again). Substitution should be a simple matter of changing an attribute or property on the schematic.

At this point, a full structural simulation of the ASIC should not reveal any gross design errors, since they would have been detected earlier (assuming a thorough test bed). Timing errors will be the most common type of problem. Many timing problems will not be detected during behavioral simulations unless the behavioral VHDL models contain accurate checks for timing constraint violations. Such checks are difficult to code in advance, since timing constraints depend heavily on the topology of the final implementation and layout, and neither of those is known when the model is first written. Estimated timing can be used, but final implementation may deviate significantly from the estimate, resulting in errors.

To effectively flush out these timing problems, the host CAE system must be capable of back-annotating accurate prelayout and postlayout delays. These delays should then be reflected back into the top-level behavioral model for later use in board-level simulations. One way to facilitate back annotation of delays to the top-level model is to code the behavioral VHDL model in such a way that all delays are retrieved through function calls. These functions can then be defined in a VHDL *package*, which can be modified for different delay values.

When structural simulations have been completed, netlist, schematic, and test pattern data can be sent to the foundry to manufacture the part.

The test bed and the top-level behavioral model are coded directly by ASIC designers. The structural VHDL model of the ASIC must be generated from the hierarchical schematics. To handle this step automatically, the host CAE system must be capable of converting schematics into a structural VHDL model. □

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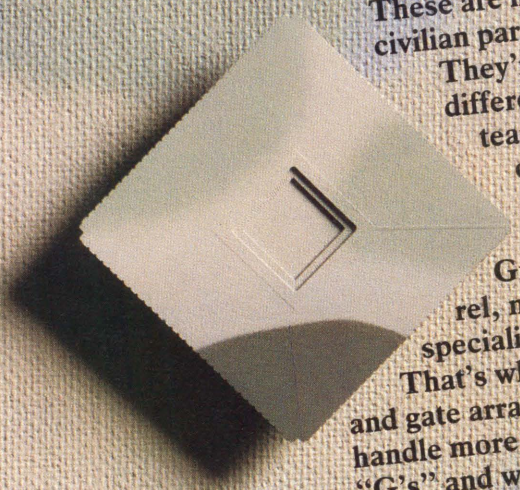

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ADVANCED MODELING TECHNIQUES FOR LOGIC SIMULATION

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Over the last five years, the number of new application-specific IC designs started each year has increased by well over fourfold. This huge jump in ASIC usage is the result of the shift from full-custom designs, implemented by skilled IC designers, to gate array and standard-cell designs implemented by system design engineers.

Full-custom ASIC design allows the designer to achieve the optimum cost/performance for a given integrated circuit process technology. However, it requires transistor-circuit simulation (for example, SPICE) to predict the circuit behavior, before masks are made and prototypes fabricated. Unfortunately, such simulation is extremely costly and time-consuming. In fact, it is virtually impossible to simulate a complete ASIC with SPICE-type simulators.

Gate array and standard-cell design approaches address this problem through the creation of a library of precharacterized logic building blocks (macrocells). By carefully precharacterizing the logical and timing behavior of each macrocell, it is possible to eliminate the need for SPICE simulation of the complete ASIC design. The system design engineer can use the precharacterized macrocell models together with a logic simulator to predict the exact functional and timing behavior of the circuit. In addition, based on the results of the logic simulation, the ASIC vendor can guarantee the performance of the proposed design before mask making and prototype fabrication.

Precharacterization is the process of developing a computationally simple timing model that approximates the actual voltage-versus-time behavior of the macrocell. The simple timing model must accurately map the detailed transistor-level behavior to 0-to-1 and 1-to-0 propagation delay times. The input-to-output propagation delays are based on extensive SPICE simulations of each macrocell, performed over a wide range of possible operating conditions (voltage, temperature, input waveform, and load capacitance). Obviously, the success of the design approach depends on the accuracy of the simple timing model used to predict the behavior of each macrocell: Overoptimistic modeling can result in prototype circuits that do not work in the target system. Excessive conservatism, on the other hand, prevents the system design engineer from exploiting the full potential of the IC process technology and may render his system design uncompetitive.

LINEAR DELAY PREDICTION

To explore how simple macrocell timing models are developed, consider the transistor-level schematic of a simple two-input NAND gate implemented in CMOS technology (Figure 1). The effects of multiple macrocell loads are represented by a lumped capacitance, C_L. For our first approximation, we will model the behavior of the MOS transistors as switched resistors. If the A input is high and we apply a step-function input to the B input, the output of the NAND gate will transition from 1 to 0.

The output transition can be broken into two phases. rst phase is the time required to turn off the p-channel transistor and turn on the n-channel transistor connected to B. During this time, the output voltage of the NAND gate will not change. This time is not dependent on the output load capacitance, C_L. Once the n-channel pull-down device has turned on, the C_L will be discharged to ground through two n-channel transistors in series. The time required for the output voltage of the NAND gate to reach 50% of the supply voltage will be proportional to the value of C_L.

From this simple analysis, we can derive a straightforward slope-intercept timing model for the behavior of the NAND gate (Pilling, Ordnung, and Heald, 1972). The rising and falling delay times for the NAND gate can be approximated with the following formulas:

$$T_d(rise) = T_{plh} + (K_{lh} \times C_L)$$
$$T_d(fall) = T_{phl} + (K_{hl} \times C_L)$$

Besides C_L in picofarads, the parameters required for the model are:

- T_{plh}: the fixed 0-to-1 delay (ns)
- T_{phl}: the fixed 1-to-0 delay (ns)
- K_{lh}: the 0-to-1 load-dependent output slew rate (ns/pF)
- K_{hl}: the 1-to-0 load-dependent output slew rate (ns/pF)

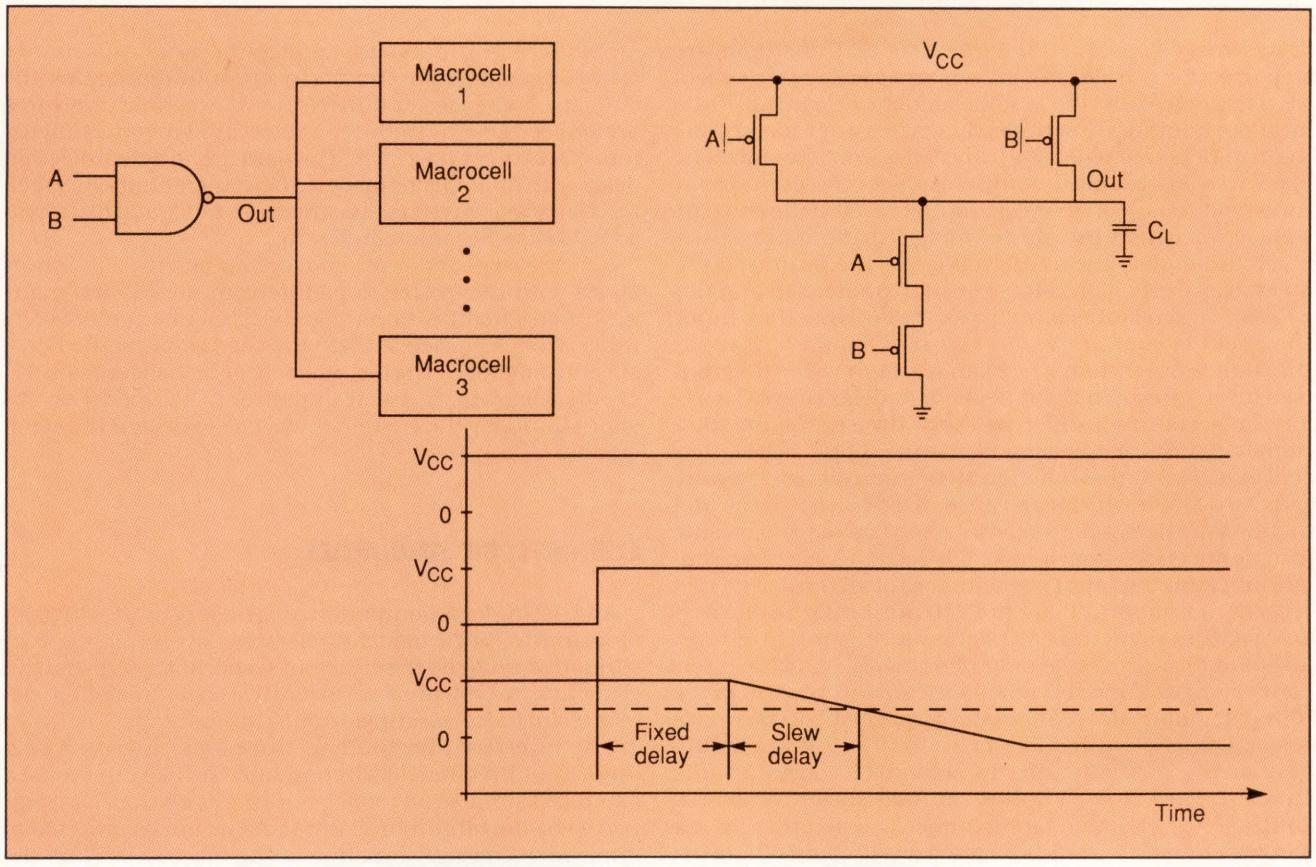

FIGURE 1. Derivation of a simple timing model for a two-input CMOS NAND gate macrocell.

The exact values of T_{plh}, T_{phl}, K_{lh}, and K_{hl} are determined from multiple SPICE simulations of the NAND gate under various output loading conditions. The value of C_L is calculated by summing the input capacitances of all the macrocells driven by the NAND gate together with the parasitic interconnection capacitance.

Unfortunately, the simple slope-intercept timing model has several basic flaws which can lead to substantial inaccuracies in the predicted macrocell delay times (Chang, Chen, and Subramaniam, 1988). These flaws are exacerbated by the rapid improvements in IC processing that allow smaller and smaller device geometries.

One major inaccuracy in the simple slope-intercept timing model is caused by the assumption of a step-function input to the macrocell. Of course, in the actual circuit, the input waveform is far from a step function. A slowly changing input signal causes additional delay, since the transistors in the macrocell will not turn on or off as quickly as if the input were a step function. The effect of noninfinite input signal slew rates is to add delay to each input of the macrocell. This additional delay is a complex function of the input slew rate and the output drive characteristics of the macrocell. The importance of input slew rate increases as the device geometries get smaller.

Figure 2 shows the ratio of load-dependent (slew rate) delay to total gate delay for increasing fan-out loading (two-input NAND gate equivalent loads). The data is based on published data book information for both 2-μm and 1.5-μm gate array technology from a major semicustom vendor and is normalized for a 6,000-gate array. The ratio of slew rate delay to total delay is much greater for the newer 1.5-μm process, so that the simple slope-intercept timing model will be less so accurate.

A second inaccuracy in the simple slope-intercept model is caused by using $V_{CC}/2$ to measure the load-dependent

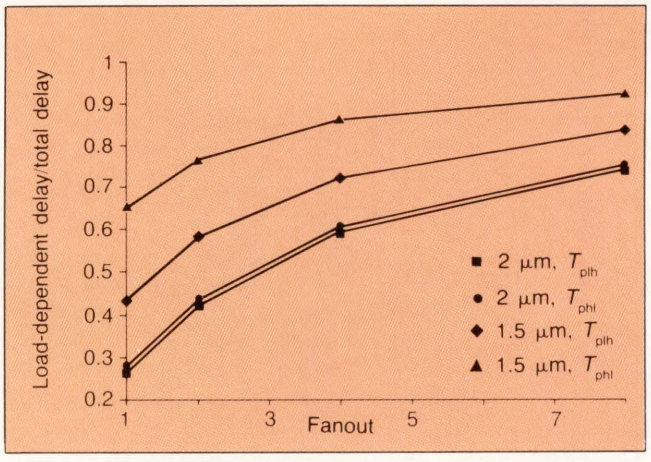

FIGURE 2. Effect of geometry on the input slew rate (for a two-input NAND gate).

delay time. Of course, if the input signal transitions are step functions, it doesn't matter what voltage threshold we use to measure the load-dependent delay. But if the inputs are not step functions, the correct way to determine the load-dependent delay is to measure from the end of the fixed delay to the time the output voltage crosses the input threshold voltage of the receiving macrocell, defined as the voltage for which the static voltage at the input of the macrocell equals the static voltage at the output of the macrocell (unity-gain voltage). Unfortunately, in practice it is very difficult to design all macrocells so that their input threshold is equal to $V_{CC}/2$. Figure 3 shows how input thresholds other than $V_{CC}/2$ can result in vastly different measurements of the load-dependent delay times. Therefore, to account for different input thresholds, an additional delay factor must be added to the simple slope-intercept model which is a function of the input signal slew rate.

A third factor which can cause inaccuracies in the predictions of the simple slope-intercept model is parasitic interconnection capacitance. It is relatively easy to calculate and sum the input capacitances of all the driven macrocells. It is more difficult to calculate the parasitic interconnection capacitance; particularly prior to circuit layout and, as process geometries shrink, parasitic interconnect capacitance becomes a greater proportion of the total capacitance load. For example, published data from a major semicustom vendor shows that for a 2-μm 6,000-gate array, the estimated interconnect capacitance is equal to approximately 50% of the total capacitive load. In contrast, the estimated interconnect capacitance for the same vendor's 1.5-μm 6,000-gate array is about 60% of the total capacitive load.

Furthermore, parasitic interconnection capacitance grows as semicustom circuits incorporate more gates (the chip size increases and therefore interconnecting wires are longer). Also, as the interconnecting wires on semicustom circuits get narrower, the parasitic interconnection delays can no longer be modeled by a single lumped capacitor. Narrower wires mean higher resistance and distributed RC delays become significant.

Nearly every vendor of semicustom macrocell libraries starts with the simple slope-intercept model, and many have made modifications to account for one or more of its inherent inaccuracies. Once the vendor has settled on a specific macrocell timing model that he believes is sufficiently accurate, he must implement that model on the logic simulator the customer will use to design the semicustom circuit.

EXISTING LOGIC SIMULATORS

All existing logic simulation programs operate with a set of "primitive" logic modeling elements. Every circuit to be simulated must be described in terms of these primitive elements. A typical set of primitive logic modeling elements includes multiple-input AND, OR, NOR, and NAND gates, inverters and buffers, three-state inverters and buffers, bidirectional switches, and the like. To create a macrocell simulation model, one or more primitives supported by the target simulator must be interconnected to implement the logic function of the macrocell. Thus the simulation model for a two-input NAND gate macrocell usu-

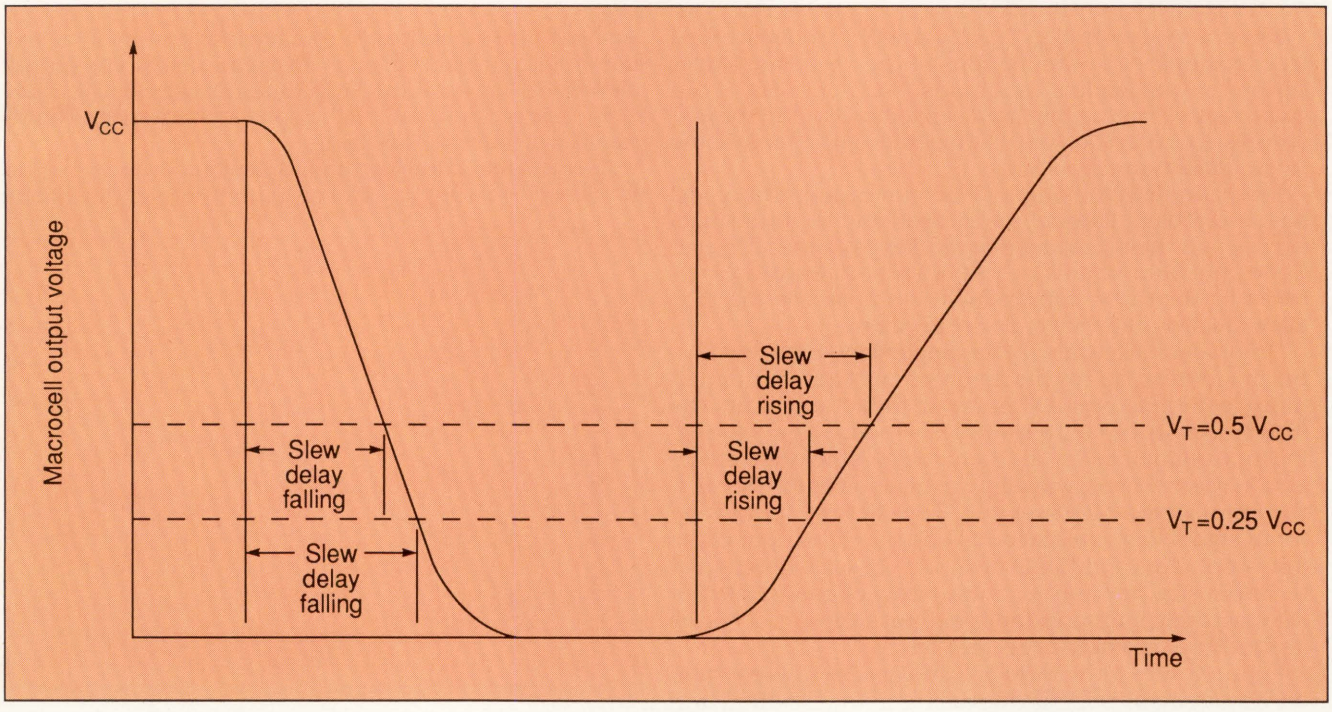

FIGURE 3. Effect of nonsymmetrical threshold voltage on slew rate delay.

ally requires only one two-input NAND primitive modeling element, whereas a counter macrocell requires the interconnection of many primitive elements.

Most existing logic simulation programs sold by third-party CAE software vendors allow the user to assign a unique rise and fall delay for every primitive modeling element used in the simulation. The developer of a macrocell simulation library must therefore use the appropriate macrocell timing model to calculate the input-to-output macrocell delays and distribute these delays properly among the primitive elements that make up the simulation model. Traditionally, this work has been done by the semicustom vendor.

Unfortunately, this is a relatively inefficient way to develop macrocell simulation libraries, since the interconnectivity of the macrocells must usually be determined twice—once in building the database of primitives and again in distributing delay values among the primitives. First, the logic simulation software must use the macrocell netlist to determine the interconnectivity of macrocells, substitute the appropriate primitive element simulation model, and create a simulation database consisting only of primitive elements. Then, the semicustom vendor must write a program that redetermines the macrocell interconnectivity and calculates the input-to-output delays based on the fan-out loading for each macrocell. The program must also correctly assign these delays to each primitive modeling element in the simulation database. Thus carefully predicting macrocell time delays generally involves significant additional circuit compilation overhead. Since each new simulation library requires writing a new timing prediction and primitive delay assignment program, semicustom vendors are reluctant to support multiple logic simulation programs.

Another disadvantage of the rise/fall-delay-per-primitive approach is the difficulty of implementing macrocell timing modeling that goes beyond the simple slope-intercept prediction. In recognition of this difficulty, several semicustom vendors have written their own logic simulation programs (Schaefer, 1985; Chawla, Gummel, and Kozak, 1975). These programs implement more complex, and therefore more accurate, macrocell timing models and free the semicustom vendor from supporting multiple simulators. However, vendor-specific logic simulation programs require the user to either commit himself to buying circuits from a single vendor or pay for and learn to use logic simulation programs supplied by multiple vendors.

An alternative approach is to develop a logic simulation system that can accurately model macrocell libraries from many different semicustom vendors. Such a system needs to be flexible enough to be able to support differing modeling requirements from different vendors and it needs to be powerful enough to provide a high degree of modeling accuracy.

NONLINEAR DEPENDENCE OF OUTPUT DELAY ON CAPACITIVE LOAD

As discussed earlier, the simple slope-intercept model does not provide the accuracy needed to model input slew rate effects on device delays. As the total output loading on a gate increases, the slope (1/slew rate) of any transitions on the output decreases. Depending on the slope, there is a measurable time between the time that the gate output voltage reaches the threshold voltage, V_T, and the time it reaches V_{CC} (see Figure 3 again). The gate inputs that see this transition incur additional delay because of the time it takes the input voltage to rise from V_T to V_{CC}.

One approach to modeling the effect of input slew rate on macrocell inputs is to assume that all macrocells will be affected equally by a given input slew rate. With this assumption it is possible to lump together the effect of input slew rate on each driven macrocell add an incremental delay to the output of the driving macrocell. The incremental delay is a function of the output slew rate of the driving macrocell. Since the output slew rate is a function of the capacitive load on the output of the macrocell, C_L, the input-to-output delays for a macrocell can be modeled with the following equations:

$$T_d(rise) = T_{plh} + (K_{lh} \times C_L) + f_r(C_L)$$
$$T_d(fall) = T_{phl} + (K_{hl} \times C_L) + f_f(C_L)$$

where f_f and f_r are functions (generally nonlinear and different for rising and falling transitions) that model the effect of input slew rate on macrocell delay. This approach therefore yields a nonlinear dependence of macrocell delay on the output capacitive load.

A flexible yet powerful way to implement these equations in a logic simulator is to use a table-driven look-up scheme. In this type of approach, any function can be approximated by a piecewise linear model; the breakpoints and slope multipliers for each portion of the model are stored in a table and used to calculate the delay for different total output load capacitances. The advantage of this table-driven approach is that it is fast and flexible; any arbitrary curve can be easily modeled.

Figure 4 shows a typical curve of delay versus total output capacitance and how the Ikos simulator models it using piecewise linear approximation. (The simulator allows the definition of up to five piecewise linear segments.) The curve is determined by specifying RBK, the nonlinear load breakpoint, the load multipliers (constants X0–X4), and a slope multiplier for each segment. Tables for generating both rising and falling nonlinear load-dependent delay times are provided.

For some macrocells, it is necessary to specify different output load-dependent delays for different input paths to the same output. Consider, for example, a three-input AND-OR-INVERT macrocell, consisting of a two-input AND gate whose output drives one input of a two-input NOR gate and a third input tied directly to the remaining input of the two-input NOR gate (Figure 5). If both inputs to the AND gate are high, the output is pulled low by two n-channel transistors in series. However, if the direct input to the NOR gate is high, the output is pulled low by a single n-channel transistor. Obviously, for a given capacitive load, the falling slew delay from either AND input to the output will be longer than from the direct NOR input to the output. In this case, the simulator allows different tables to be specified, depending on which input is being evaluated. This approach

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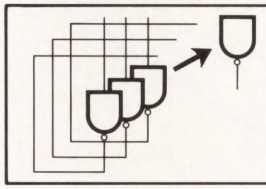

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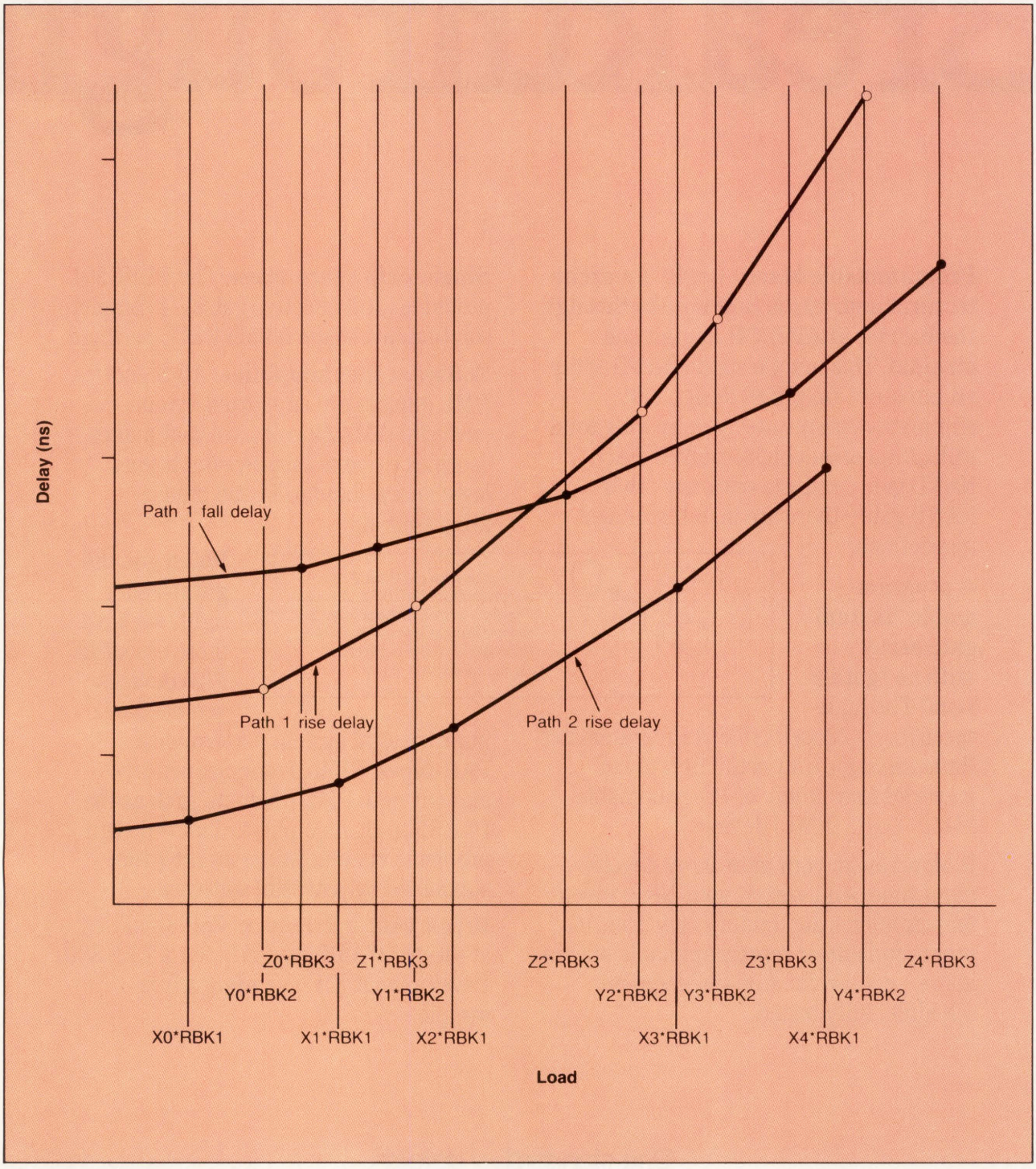

FIGURE 4. Piecewise linear delay curves.

allows for more accurate timing modeling than simply assuming that the output delay equations are the same for all paths to the same output.

One advantage of this simple approach to modeling slew rate effects is that timing problems can be more easily debugged. Excessive signal delay can easily be traced back to the "slow" gate. If the signal delay is due to output loading, the output drive of the gate can be increased (or an output buffer added). If the simulator adds the delay to the input of the driven gate, it might lead the designer to conclude that the problem was caused by excessive load on the driven gate rather than from the driving gate. He would then erroneously beef up the drive capability of the driven gate, which would not mitigate the problem.

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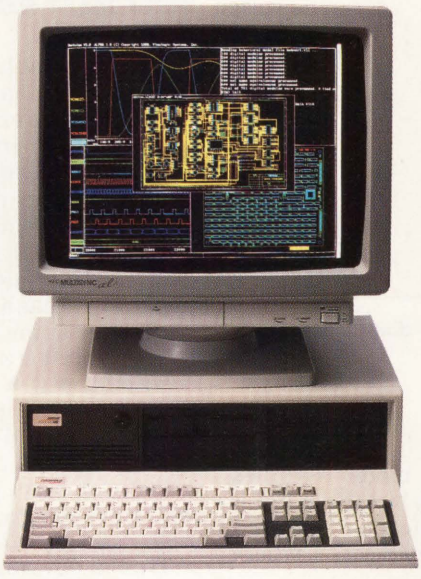

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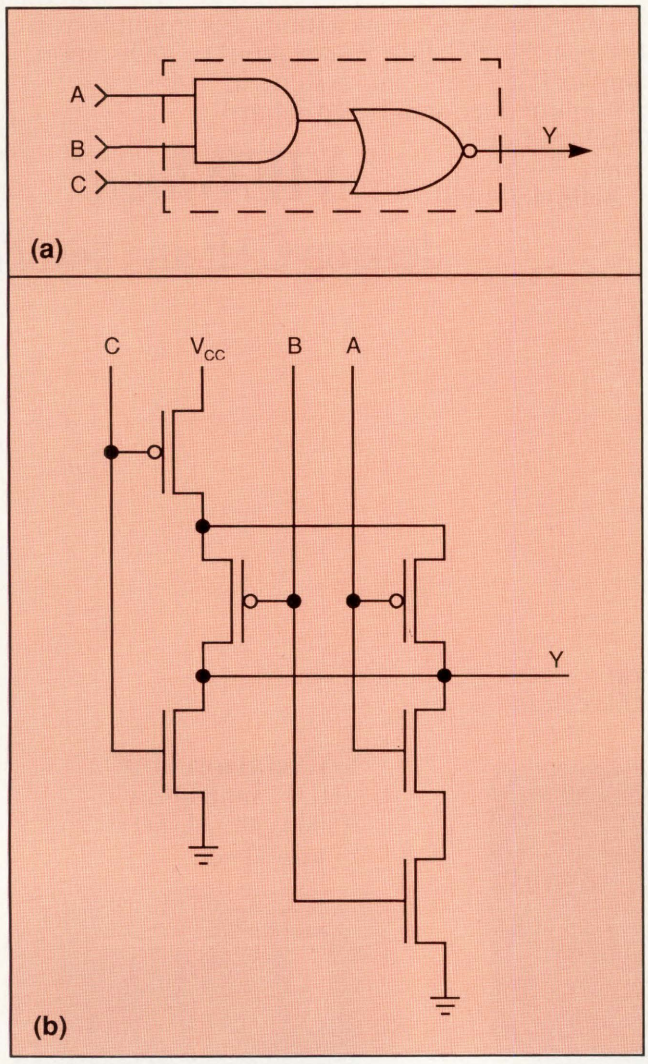

FIGURE 5. AND-OR-INVERT macrocell: logic diagram (a) and schematic (b).

SLEW RATE MODELING

The nonlinear load-dependent delay model assumes that all gates are affected in the same way by a given input slew rate. In practice, this assumption leads to reduced accuracy, particularly for small-geometry devices, where slew rate effects can be substantial.

It is possible to model slew rate effects more accurately by adding a separate slew-rate-dependent delay to the input of every macrocell model. Studies have shown that the additional input delay must be a function of both the slew rate of the transitioning input and the slew rate of the transitioning output (or, equivalently, the capacitive loading on the output) (Matson, 1985). With this approach, the input-to-output delay equations for a macrocell become:

$$T_d(rise) = f_r(ST_x, C_L) + T_{plh} + K_{lh} \times C_L$$
$$T_d(fall) = f_f(ST_x, C_L) + T_{phl} + K_{hl} \times C_L$$

where ST_x is the input slew time of the appropriate polarity (for instance, rising transition on input leads to rising transition on output). Note that ST_x is given by the $K_x \times C_L$ product of the driving macrocell.

Since these delay terms are a function of two variables (input slew rate and output load) a table look-up scheme is again the most flexible and practical way to model these curves. In the Ikos simulation system, a 5×5 matrix is used, allowing the specification of an input delay for up to 25 combinations of input slew rate and output capacitance. The discrete slew rate and output load points define a piecewise linear surface in three-dimensional space (Figure 6). Two-dimensional interpolation is used to locate points on the surface that are not defined by the discrete points in the 5×5 matrix. The interpolated delay is then added as an input delay to the driven gate.

The Ikos simulation system allows the entry of up to 16 different three-dimensional tables for each macrocell. With this capability, it is possible to model input slew rate effects differently for each macrocell input pin. The use of multiple input slew rate tables also allows the input slew rate model to be different for rising and falling input transitions. It is therefore possible to employ the input slew rate tables to model the asymmetrical effect of macrocell threshold voltages that are not equal to $V_{CC}/2$.

INPUT DELAY MODELING

The Ikos simulation system supports separate rise and fall delays from each simulation primitive input pin to the output of the simulation primitive. Input delays generated from three-dimensional slew rate tables can therefore be added into the path delay of appropriate simulation primitive. There is an inherent problem with this scheme, however, that is common to all event-driven simulation algorithms. In the simple case shown in Figure 7, a 10-ns input delay has been added to input A and a 2-ns delay to input B, and the gate has a falling delay (input to falling output) of 2 ns. Now, assume that input A transitions high and that 1 ns later input B transitions high. What happens?

When input A transitions, a gate evaluation is performed. Since input B is still low, no event is scheduled. One nanosecond later, input B transitions high and another gate evaluation is performed. This time an event is scheduled, since both A and B are now high. The output will be scheduled to transition low 4 ns after input B goes high (2 ns input delay + 2 ns gate delay).

This is obviously not correct. The output should not transition low until 12 ns after input A goes high (10 ns input delay + 2 ns gate delay). Because the transition on input A preceded the transition on input B, an output event was not scheduled, and the input delay on input A is effectively ignored.

Fortunately, there is a way to overcome this problem. Figure 7 shows the addition of buffers to the gate inputs. The input delays are added to the buffers; since any transition on the input to the buffer will cause an output event to be scheduled, the correct delays are presented to the NAND gate inputs. The only drawback to this approach is that it

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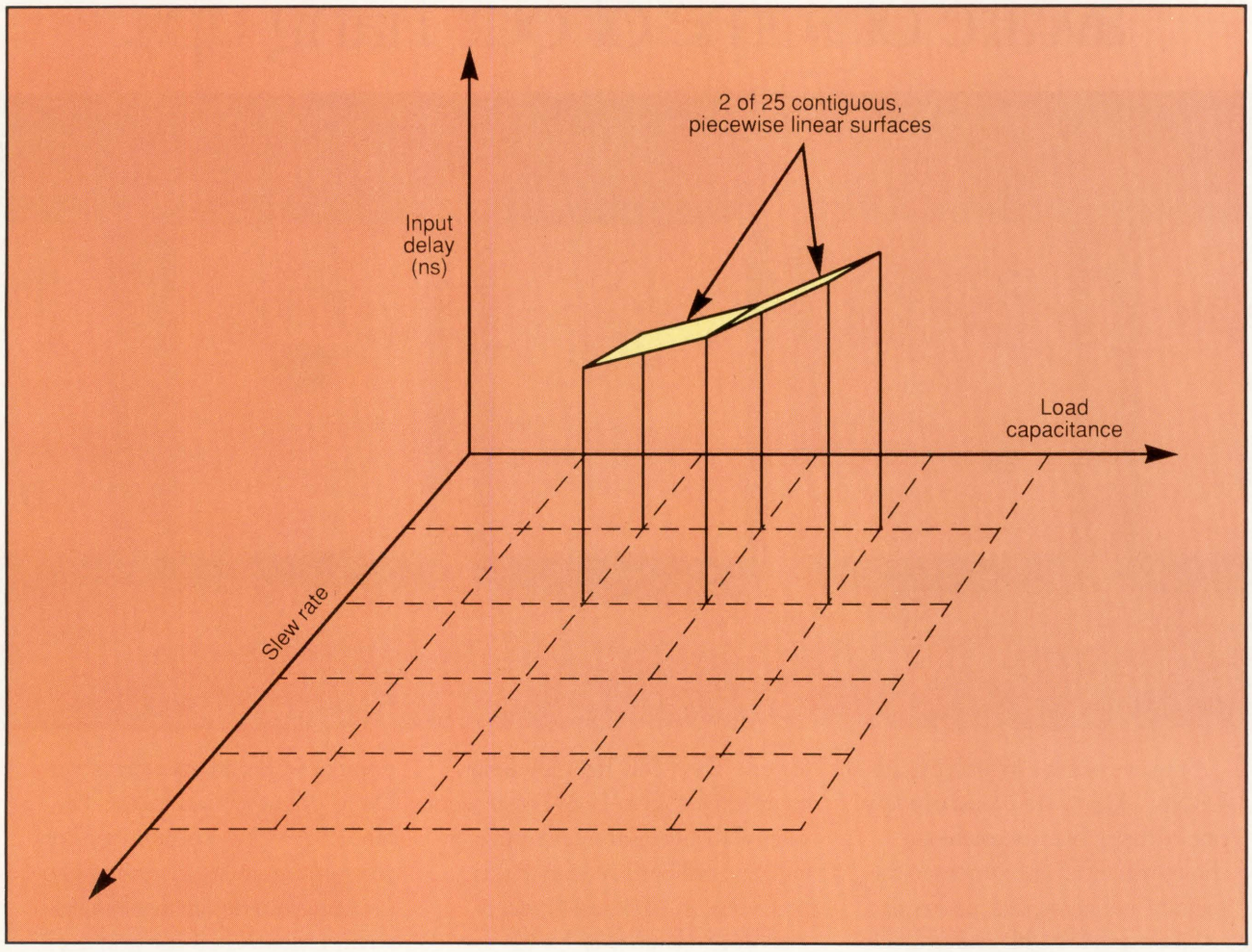

FIGURE 6. Piecewise linear surface model of slew rate delay.

requires the consumption of more primitives and increases the complexity and time required by the netlist processing step prior to simulation.

We have taken a novel approach to overcome these drawbacks. In the Ikos simulator, a differential threshold is set. If the difference between the input delays is less than the threshold, the input delays are added directly to the cell inputs. If the difference exceeds the threshold, input buffers are added to the gate inputs and the delays are assigned to the buffer inputs. This technique is applied to the slew rate table-driven delays. It is also used to back-annotate RC wiring delays derived from the actual layout. This approach produces an optimal balance between accuracy, efficient primitive utilization, and processing speed.

ESTIMATING HIERARCHICAL WIRE CAPACITANCE

As noted earlier, parasitic interconnection capacitance becomes of relatively greater importance as device geometries shrink. Estimating the parasitic interconnection capacitance before device layout is therefore becoming more and more critical to accurate macrocell timing modeling. One way to improve interconnect capacitance estimation is to take advantage of hierarchy in the macrocell netlist description. This technique assumes that hierarchical nodes in the netlist will ultimately be placed and routed as "blocks." Interconnections between these blocks will then be made globally across the chip.

Figure 8 shows four levels of hierarchy that make up a design. The wire interconnects within blocks likely to be much shorter than the wires that connect the blocks together at the next higher level. In this case, the simulator should assign a smaller estimated wire capacitance value to interconnects within a certain level and a higher estimated value to the interconnects running between levels. Since the physical placement and routing of the chip is also derived from the hierarchy, this technique yields a close approximation to the actual wiring capacitances.

In practice, a table-driven approach is again the most efficient way to develop the wiring interconnect models. The Ikos system supports up to 256 tables of estimated wire capacitance per ASIC library. Each table has 32 entries of wire capacitance that are ordered by fan-out number. In

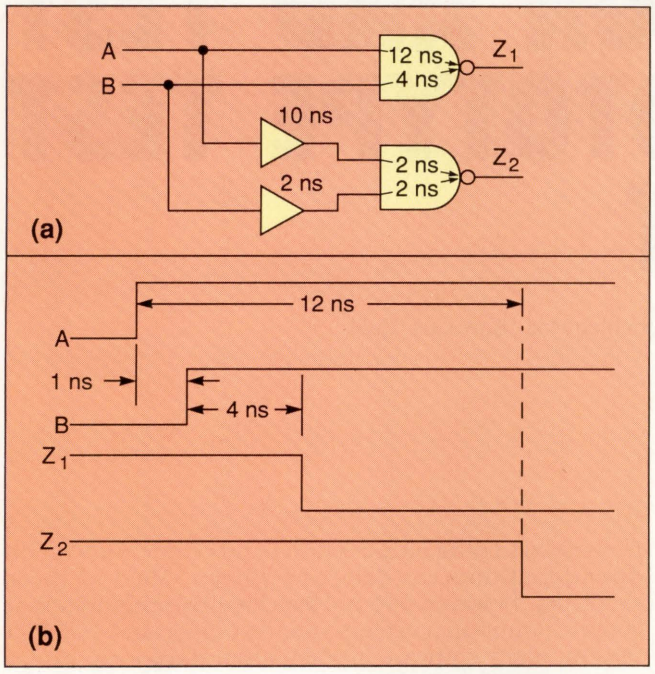

FIGURE 7. The use of input buffers to ensure correct delay assignment: logic diagram (a) and timing diagram (b).

use, the fan-out number is derived by totaling the number of cell and block inputs and outputs on the net at a particular level in the design hierarchy (with the exclusion of the output of the driving element).

The 256 tables are assigned to different ASICs within a family and to different levels of the design hierarchy. Within a given ASIC family, there are usually a number of different parts differentiated by gate count. Each unique part number is assigned its own set of wiring tables. These tables are subdivided into unique tables for each level of the design hierarchy. In the Ikos system, tables are designated for main levels and subsidiary levels.

Main tables are used for estimating wiring capacitance between cells and subblocks at the highest level of a particular net's routing path. The subsidiary tables are used for estimating capacitance for cells and subblocks at levels lower than the particular net's top level. In the case of either table, linear interpolation is used to select the correct wiring capacitance value based on the fan-out number. This approach makes possible to estimate very accurately the prelayout interconnect capacitance.

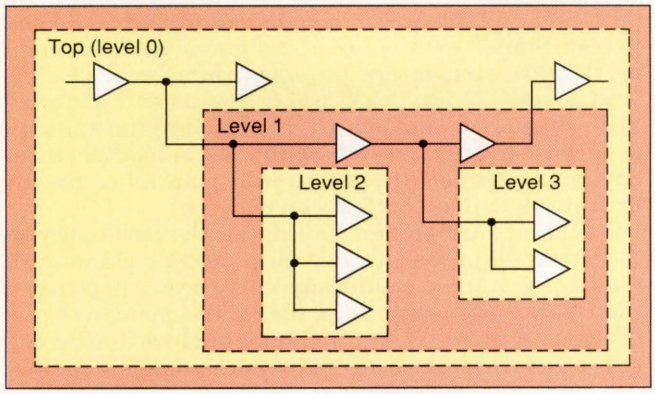

FIGURE 8. Interconnectivity in a hierarchical design.

SUMMARY

Accurate simulation of today's small-geometry ASICs puts added requirements on simulators. Since each ASIC vendor develops its own unique specifications, simulation vendors are faced with the task of having to accommodate complex modeling schemes yet retain flexibility so that many different ASIC libraries may be supported. The table-driven approach to approximating complex functions provides this flexibility. With table look-ups and linear interpolation techniques, complex functions and curves can easily be represented with a high degree of accuracy. Not only is table look-up fast, but also changes and updates can be made quickly and easily, easing the development of accurate ASIC simulation libraries. □

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LINKING DESIGN AND TEST FOR ASIC PROTOTYPE TEST DEVELOPMENT

Eric Archambeau, Teresa Butzerin, and Dave Roth, VLSI Technology Inc., San Jose, Calif.

Testing is often the major obstacle to achieving a fast turnaround for application-specific ICs. Computer-aided tools and advanced processing equipment are now available to perform quick, error-free design and fast manufacturing of ASIC prototypes. However, developing test programs for delivering tested ASIC prototypes is still a major bottleneck. A prototype device may fail the test program even if the device passes the customer's "incoming inspection," which often consists of plugging the device into his system. This paper describes an integrated test vector development environment for the fast and reliable generation of ASIC prototype test programs.

PROTOTYPE TEST ISSUES

The alternative to ASIC prototype testing is called "cut-and-go": no functional test is performed. This technique is clearly inferior in terms of costs and quality for both the manufacturer and the customer. However, since the time required to debug functional test vectors can be as long as several weeks, ASIC customers are usually willing to accept cut-and-go as a trade-off for fast-turnaround prototypes.

The principal cause for prototype test difficulties comes from the way design data is transferred to the test floor. Typically, ASIC prototype tests are derived from the simulation runs done during the design verification phase; these simulation vectors are then converted into a given tester language. If the test fails to perform correctly, the burden of correcting the problems is passed on to a test engineer. But since the test engineer has very little knowledge about the design, he must resort either to reviewing the original schematics and simulations himself or to consulting with the designer. In either case, correction is a very time-consuming and tedious process that also results in a loss of valuable tester time to debugging procedures.

There are many reasons why a test program might not work (that is, not match the silicon behavior), even if the silicon works in the customer's application. For example there might be race conditions, either internal or pattern-induced; uninitializable circuitry; noise due to simultaneously switching outputs (SSOs); bus contention on bidirectional pins; or defective silicon. Most of these problems, however, are not detected by programs that convert simulation vectors into test programs. For that reason, many software products that purport to bridge design verification and testing in reality only guarantee to generate a compilable test program, not necessarily a working test program.

THE 'TEST HOSPITAL' EXPERIMENT

The problem of automatically developing prototype test programs is particularly critical for VLSI Technology Inc., since ASIC foundry service, including prototyping, is a very important part of our business. Moreover, whereas the design and fabrication turnaround time for gate arrays and cell-based designs has been decreasing over the last few years, test development time has not followed the same path. Additionally, the number of prototypes to be processed has been going up, thus increasing the burden on test engineering.

The search for a solution to this problem was given to a special task force, whose charter was to debug test programs for ASICs, systematically research test program problems, and make recommendations in all areas related to test. Staffed with a mix of designers, software engineers, and test engineers, the organization was called the "test hospital," since "sick" test programs were admitted to be "diagnosed" and treated. The test hospital was supplied with an STS 120 tester (Sentry 20–compatible) in an environment isolated from the test floor but linked directly to the workstation-based design network.

Whenever a test program failed to work immediately on the tester, the precise cause of the problem was analyzed. As of this writing, over 90 designs have been submitted to the test hospital—only a fraction of the company's ASIC designs. Of these, 41 required some analysis and debugging other than simple test program recompilation. Silicon fabrication failures represented only a negligible percentage of the cases (see the table).

Conversion software errors	Internal race conditions
Dubious simulation practices	Initialization problems
External race conditions	Dubious design practices
Test hardware problems	Simultaneously switching outputs and other noise sources

Test program failure mechanisms.

The information collected enabled us to design a test vector generation environment that guarantees that test vectors will always convert to the cycle-based world of testers while guarding against race conditions and other hazards. By developing simulation guidelines, improving model and vector conversion software, establishing standard test procedures, and providing a reliable automatic test program generation procedure, we have been able to dramatically reduce the average time required to develop a prototype test. Although this experiment was originally run on gate array designs, it has been extended to cell-based devices.

As this prototype test program development environment was installed, the percentage of test programs that worked successfully on first try increased by a factor of 12. Meanwhile, the average number of man-hours per test program debugging decreased by a factor of 7. Since the latter number is directly related to the time spent by the average ASIC designer to develop his or her own prototype test in the same test generation environment, it affects all ASIC designers.

A NEW APPROACH TO PROTOTYPE TESTING

Lessons learned from the test hospital experiment have helped us formulate a new approach to prototype testing. Users of ASICs need to realize that the link between simulation, testers, and silicon is not automatic and that they should require that their ASIC vendors provide them with tools and guidelines to bridge the gaps between these three worlds of IC testing (Figure 1).

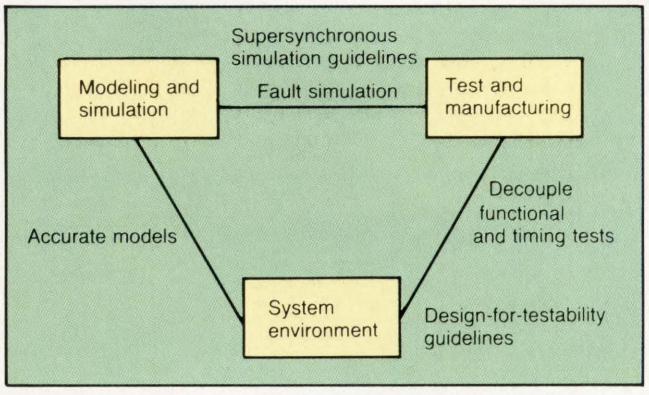

FIGURE 1. Linking the three worlds of testing.

Although these three environments have large overlaps, there are of missing bridges between them. For example:

- Simulation can display the behavior of internal nodes, but testers can only probe I/O pins.
- Millions of vectors can be used to simulate a circuit in the intended system, but such large numbers of vectors are not practical for testers.
- Two-micron gates can switch at 40 MHZ in a system, but many testers can only test at speeds of up to 20 MHZ.
- Noninitialized counters may work in a system but cause unknown states in the simulation and become untestable because of unpredictable output values.
- A single simulation cannot verify the timing for both the best and worst cases that may exist in an actual system.

The problem of creating "working" test programs automatically needs to be solved in several realms. To address all aspects of the test generation problem, the methodology we adopted is based on five important principles:

1. Provide design-for-testability guidelines during the logic definition phase
2. Decouple the functional and timing elements of test programs
3. Require "test-orientated" simulation
4. Provide extremely accurate modeling and simulation
5. Provide fault simulation

DESIGN FOR TESTABILITY

Because prototype tests must be able to weed out any defective silicon, prototype test programs must guarantee adequate fault coverage. Since typical testers impose limits on test length, high fault coverage must be accomplished with relatively few patterns. That can be achieved only if a high level of controllability and observability is provided for imbedded functional blocks. Design-for-testability (DFT) techniques (Williams, 1983) must be applied from the beginning of the design cycle to achieve these results. Even if high fault coverage is perceived as an issue only for production testing, DFT features should already by incorporated at the prototype level so that DFT will impose a minimum overhead on the overall design cycle time.

The testability of a circuit can be measured early in the design cycle (Archambeau, 1985) to detect areas of poor controllability and observability before committing the design to silicon. The use of testability features might imply an area penalty, design constraints, and even performance deterioration. On the other hand, increased testability usually reduces simulation, test vector generation, and actual test time, as well as overall testing costs. The testability trade-offs must therefore be fully evaluated before committing a design to silicon.

Our experience with the test hospital confirmed the well-known fact that some of the worst problems with failing test programs are a result of design problems. In some cases in which a test program fails because of illegal initialization or "internal" race conditions, the problem is virtually impossible to solve without redesigning the circuit. Remember, though, that a device can function perfectly in its intended system and still be virtually untesta-

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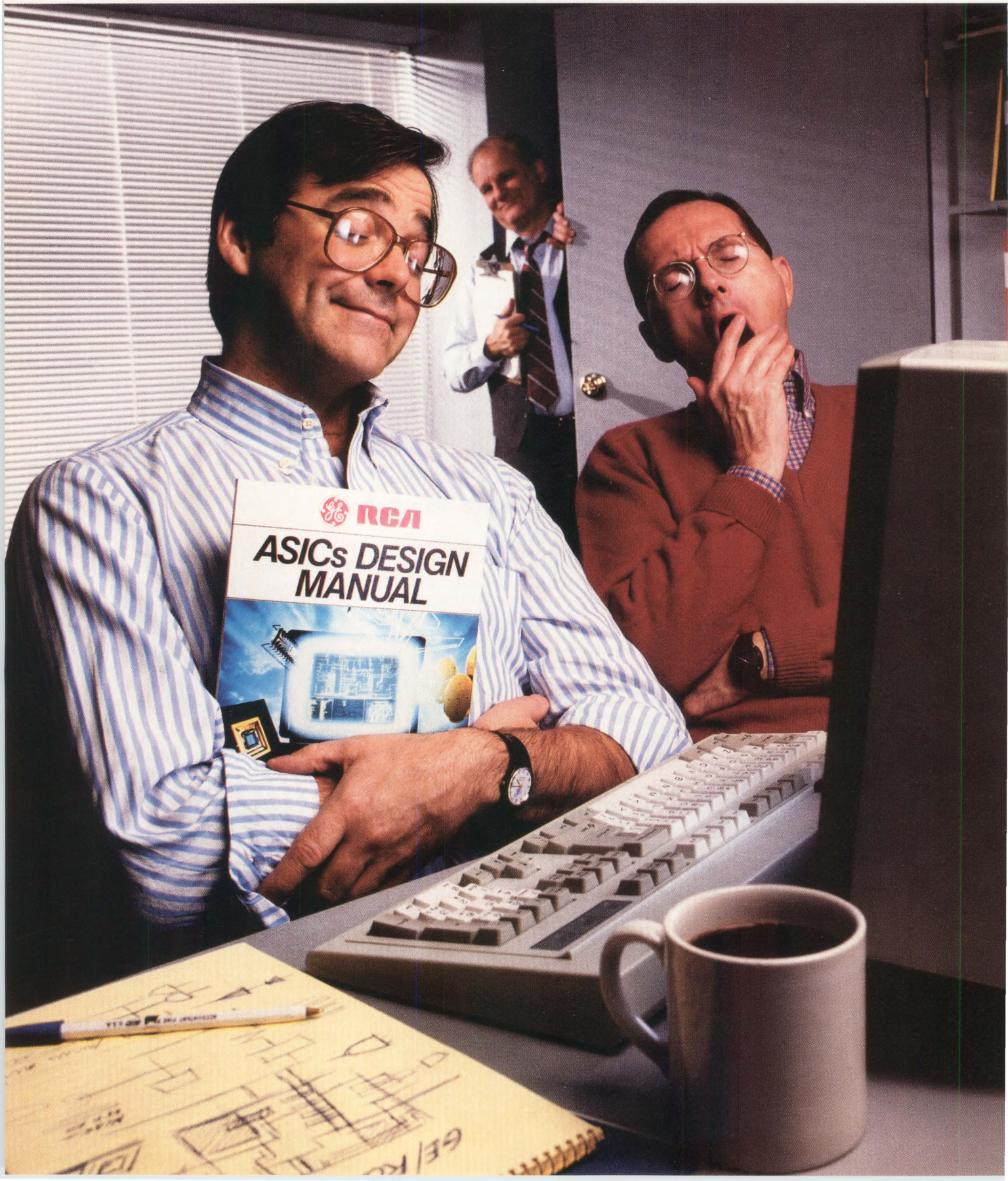

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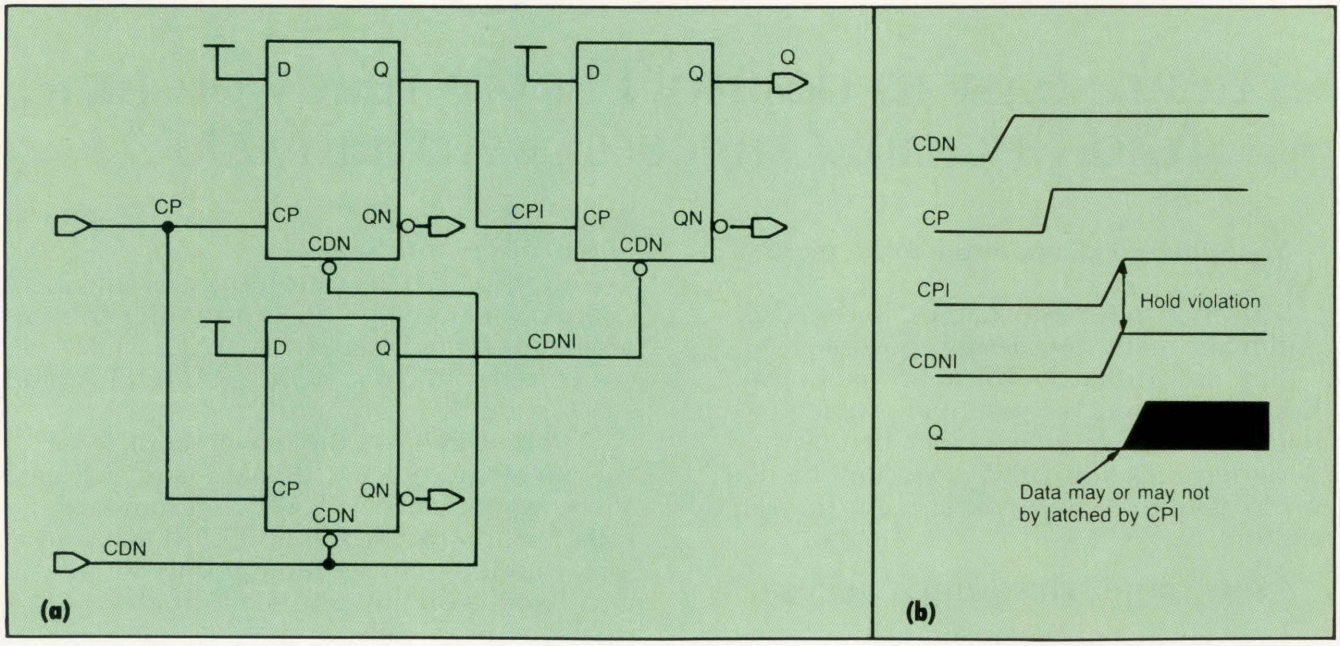

FIGURE 2. Internal race condition: circuit (a) and waveforms (b).

ble, because it was not designed with testability considerations in mind.

Illegal initialization. It is critical that all latches and storage elements in a circuit be designed such that they can be initialized to a known state during system initialization. If a circuit cannot be initialized easily, generating a reliable test program can be extremely difficult. Most testers have a "match" mode that can be used to clock a circuit until it proceeds to a recognized state, but it is often very difficult (and sometimes impossible) to ascertain an identifiable sequence.

Internal race conditions. An internal race condition can occur when inputs to a latch transition as a direct result of a common internal transition. Figure 2 shows an example of a race condition between a flip-flop's Clock and Clear pins, resulting from a common signal transition. Even when such a race condition does not affect the final system operation, it might result in test problems. For example, if a latch's data is sampled asynchronously, even if it does not matter which clock edge catches the data for system operation, the tester, which expects completely predictable behavior, might fail good devices.

Internal race conditions are much more serious than external (pattern-induced) race conditions because they cannot be corrected by modifying the vector timing.

DECOUPLING TEST ISSUES

As a first step toward simplifying the test problem for prototype test programs, we propose here to decouple the different aspects of tests, which previously have been bundled together:

1. *Parametrics test.* A parametrics test checks for overall process variations and validates the modeling hypothesis used during design verification simulation runs.
2. *Functional test.* The test frequency can be different from the system operation frequency, since functional test vectors should be used not as additional simulation vectors, but rather to validate further the design verification hypothesis and to check for silicon faults.
3. *Speed test.* Speed specifications are checked for by measuring critical paths, a sufficient test for race-free designs.

At-speed testing of all parts is no longer necessary when:

- Simulation takes into account frequency-related phenomena (for example, heat dissipation due to high-frequency operation and setup and hold time temperature variations)
- High-fault-coverage, low-speed test vectors check for process defects (localized manufacturing flaws) while validating functional simulation results
- Parametric tests check for global manufacturing deviations and thus validate the accuracy of the system timing verification
- Actual chip maximum utilization frequency is measured by user-specified critical path checks

Decoupling of speed and functional checking permits the use of the normal operation zone of any target tester for prototype testing without trying to push the test equipment to its limits. That reduces the need for an experienced test engineer's time.

The first implication of this decoupling is that the designer must develop a test-oriented simulation distinct from his system simulation—a reasonable expectation,

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since it is not always possible to exactly replicate the actual operating conditions of a circuit on a tester. VLSI Technology's "supersynchronous" simulation guidelines are tester-independent and test-oriented and facilitate this "new" design step.

SUPERSYNCHRONOUS SIMULATION GUIDELINES

Supersynchronous guidelines were established to maximize the probability that the test generation simulation can be converted into a working test program. They are not intended to provide the designer with maximum design verification flexibility or to address the problem of developing high-speed, customized test programs. They *are* intended to decrease the test development time and shorten the prototyping cycle. In VLSI Technology's design environment, adherence to the guidelines is checked by a vector screener. Customers normally submit a set of "supersynchronous" simulation vectors along with their netlist to one of VLSI's design centers. Customers requiring more flexibility can use the company's Special Test Services at additional cost and with longer development time.

Some of the major aspects of these simulation guidelines follow:

- *Simulation timing must be tester-compatible.* All input timing in a test-oriented simulation must adhere to the synchronous, cycle-oriented timing constraints of a tester. The simulation must be "cycle-based," with all inputs changing at regular edge times relative to the beginning of a cycle. Inputs must be assigned one of the standard tester input formats: NRZ (non–return to zero—one edge time), RTZ (return to zero—two edge times), or RTO (return to one—two edge times). All input transitions must occur at the prescribed input edge time, and the edge time assignments must remain constant throughout the test (Figure 3). Multiple edge time definitions are permitted because restricting all inputs to change at a single edge time can introduce "artificial" pattern-induced race conditions—that is, race conditions occurring only at test time, not during normal systems operation.

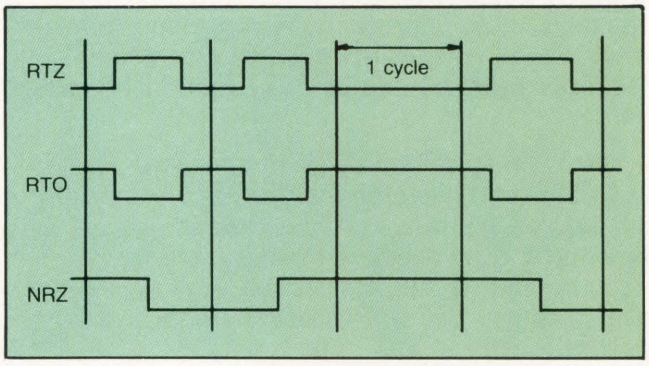

FIGURE 3. Supersynchronous input rules.

- *Test generation simulation need not be at system speed.* The purpose of the test generation simulation is to generate functional test patterns, not to verify the system timing constraints. Outputs may be strobed only once per cycle, and they should be strobed only when the circuit is entirely stable, so that the speed at which the test-oriented simulation may be done is limited by the maximum delay of the longest internal path.
- *Assign input edge times to avoid race conditions.* Input timing generators should be assigned to avoid pattern-induced, or external, race conditions. An external race condition can occur when inputs to a latch transition as a direct result of I/O input transitions. An example would be a flip-lop with both data and clock driven from I/Os and assigned to the same edge time (Figure 4).

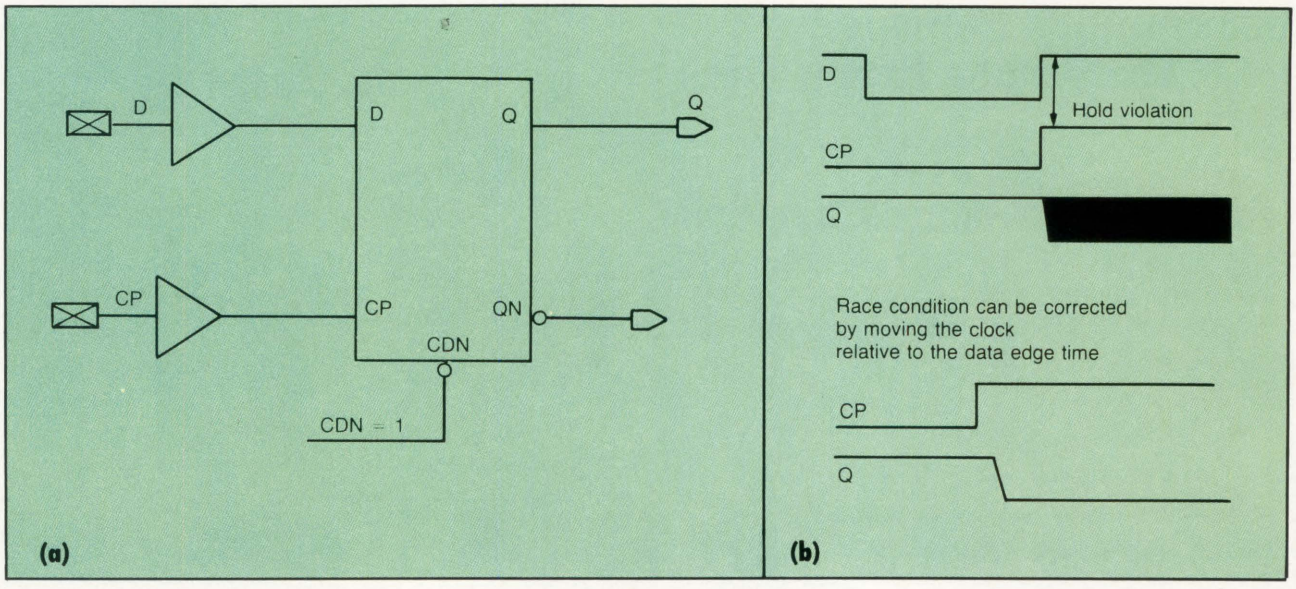

FIGURE 4. External race condition: circuit (a) and waveforms (b).

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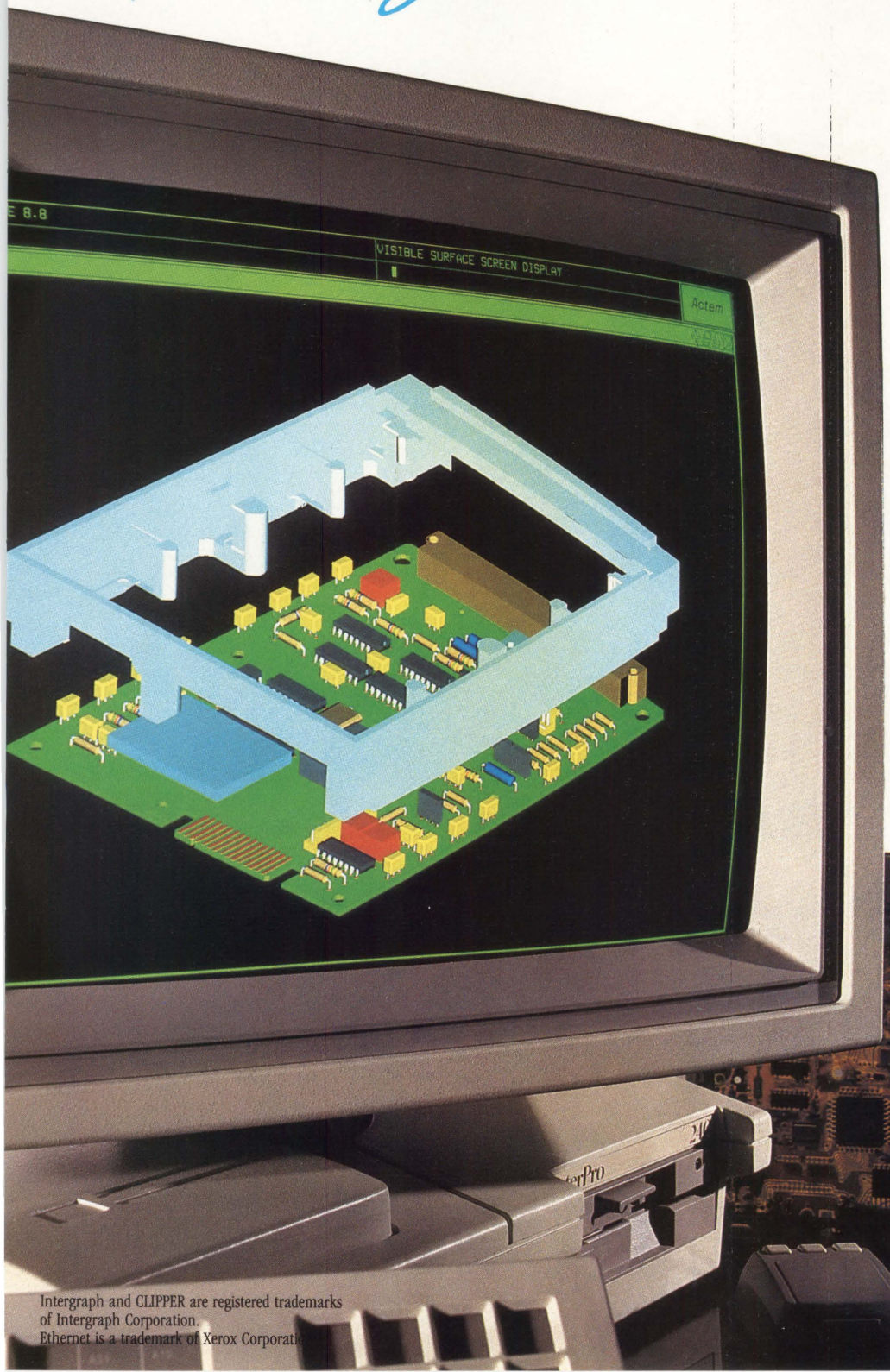

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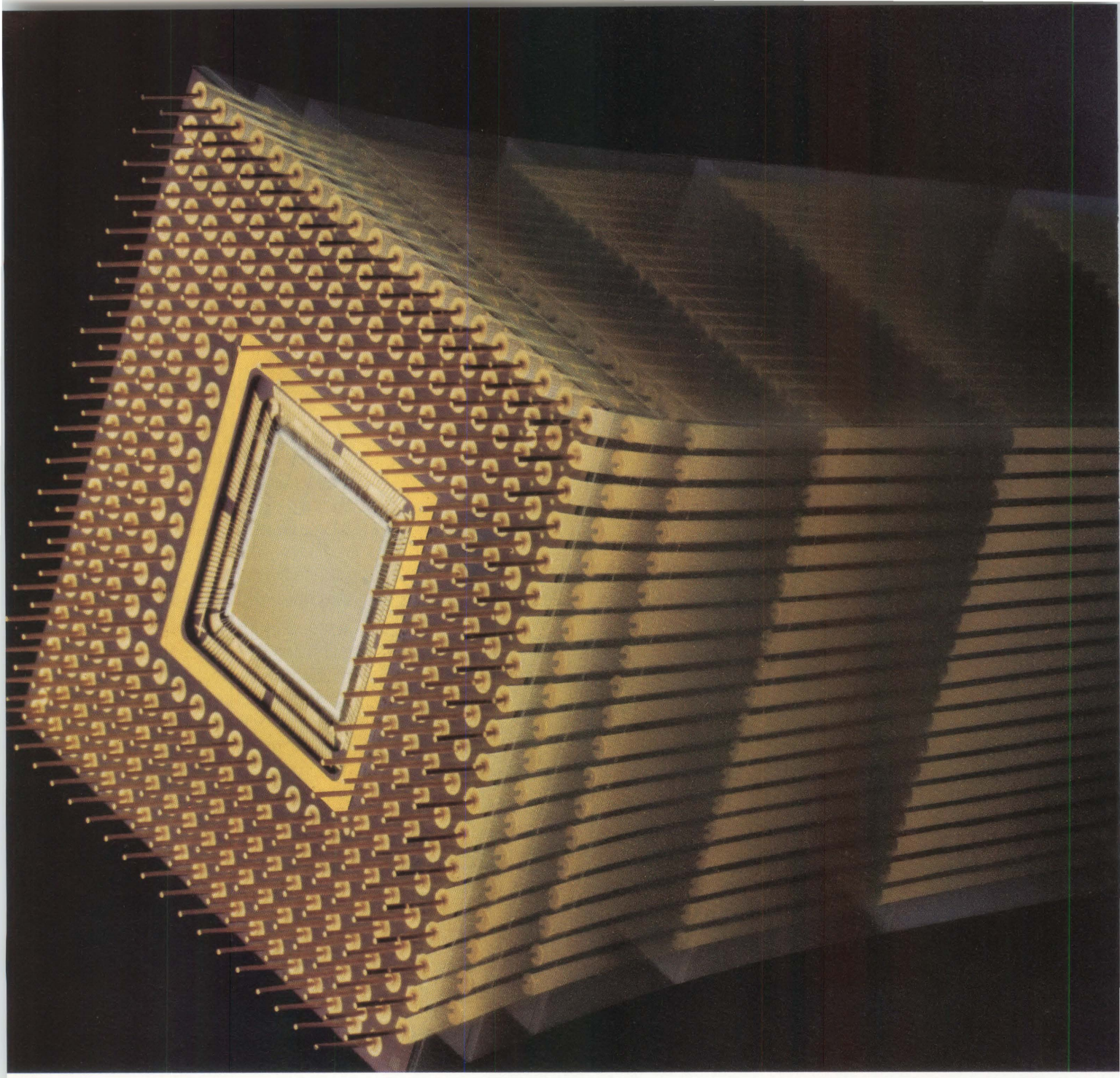

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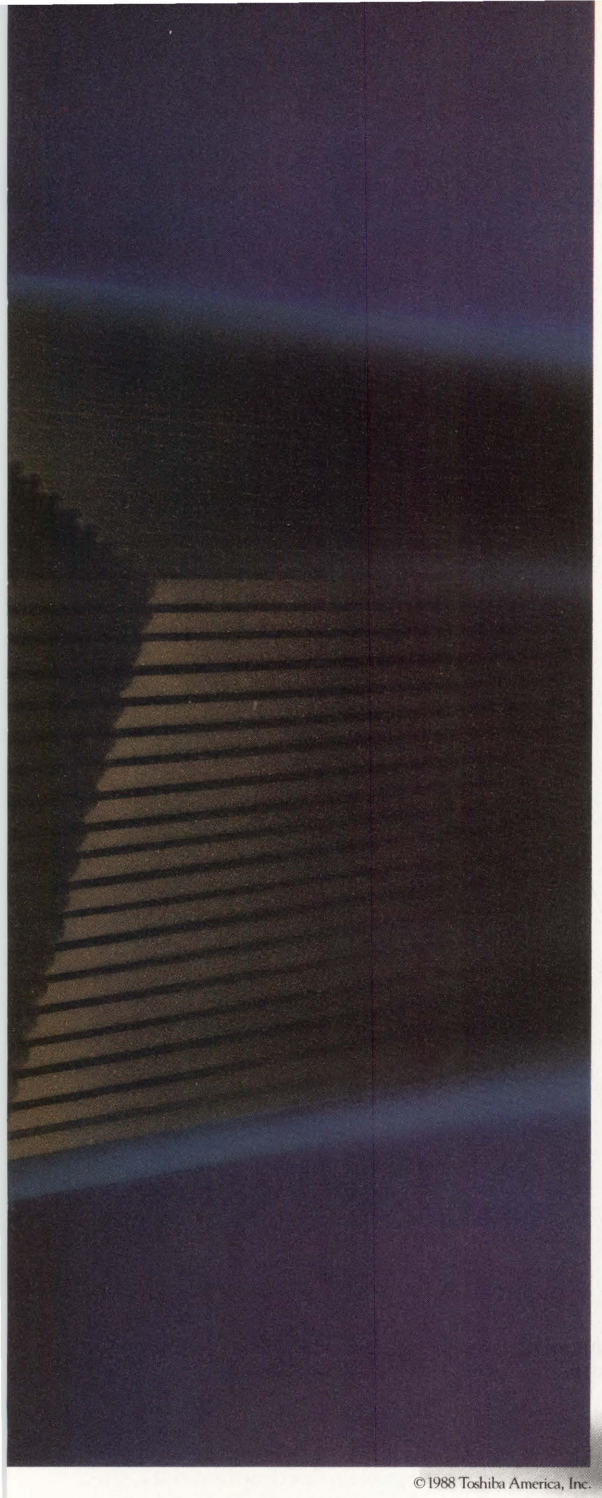

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For this reason, supersynchronous guidelines require that edge times be separated by *N* nanoseconds, where *N* is greater than the longest possible delay in the circuit. Defining large delays between edge times helps prevent pattern-induced race conditions: Providing for discrete time intervals in which signals can settle precludes the tester's timing generators from triggering simultaneous transitions from different edge times.

- *Two timing generators cannot be assigned the same edge time.* The tester might skew two different timing generators by a few nanoseconds relative to each other, and the skew could possibly lead to race conditions or yield problems, depending on the particular circuit and simulation conditions (Figure 5). Consequently, this very important rule prevents unreproduceable race conditions caused by timing generator skews from happening.

Note that the supersynchronous rules prevent tester-induced and pattern-induced race conditions from occurring: the remaining internal race conditions between transitions triggered by the same timing generator are detected by the models during simulation or timing verification, or both.

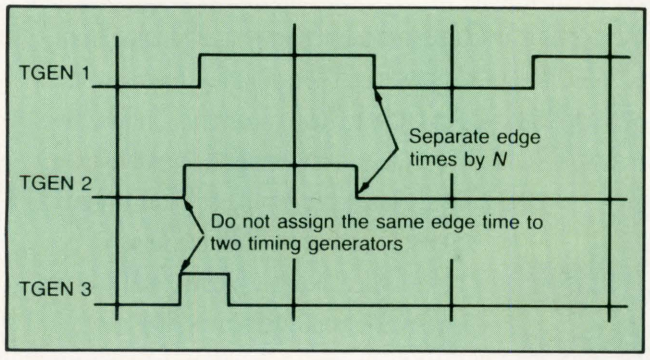

FIGURE 5. Supersynchronous rules for edge time definition.

- *Bidirectional contention must be avoided.* Supersynchronous bidirectional rules require that the control signal of every bidirectional circuit be "watched" in the trace file. The bidirectional control signal determines whether a bidirectional pin is driven or sensed during a particular cycle. The following supersychronous guidelines refer to bidirectional circuits:

  - There should be only one transition per period on any bidirectional node.
  - There should be only one transition per period on any control signal (bidirectional or three-state).
  - If a transition occurs on both the bidirectional node and its control in a cycle, the control transition must occur before the node transitions.

If a bidirectional pin is driven as an input by the tester while the circuit is driving the node as an output, current spikes can appear on the power or ground lines. The supersynchronous guidelines (see Figure 6) prevent this hazardous situation, which could cause permanent circuit damage.

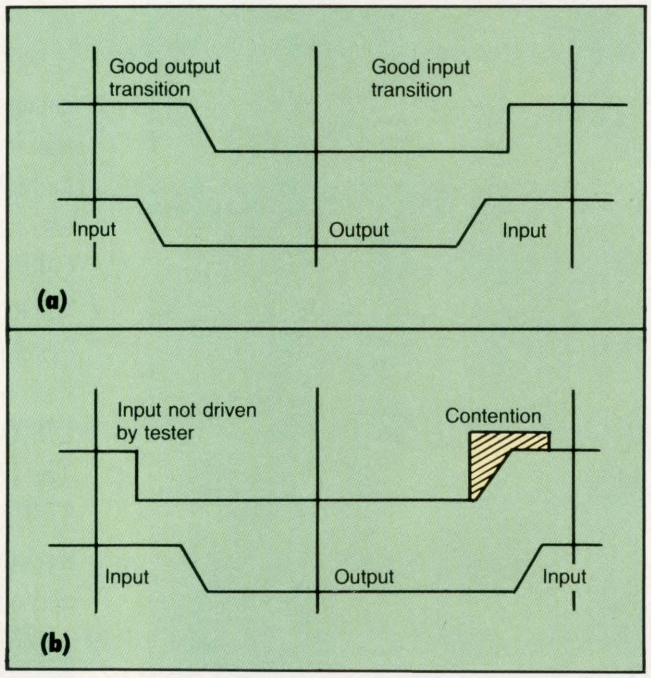

FIGURE 6. Supersynchronous bidirectional guideline: good (a) and bad (b) control.

- *Test modes must be specified.* Test mode initialization sequences must be provided for cell-based designs; for circuits incorporating megacells or compiled cells, the designer must provide and specify test modes during which supersynchronous predefined vectors can be applied to each functional block.

MODELING AND SIMULATION ISSUES

Prototype test programs must be generated directly from simulation trace files, and they therefore rely on very accurate logic and timing simulation. Despite continuous progress in simulation accuracy, many effects, like those of current switching, and input level problems cannot be handled by most logic simulators. Capacitive loading effects for complicated models like unbuffered flip-flops (where the capacitive load on $\overline{Q}$ may effect the timing on Q)

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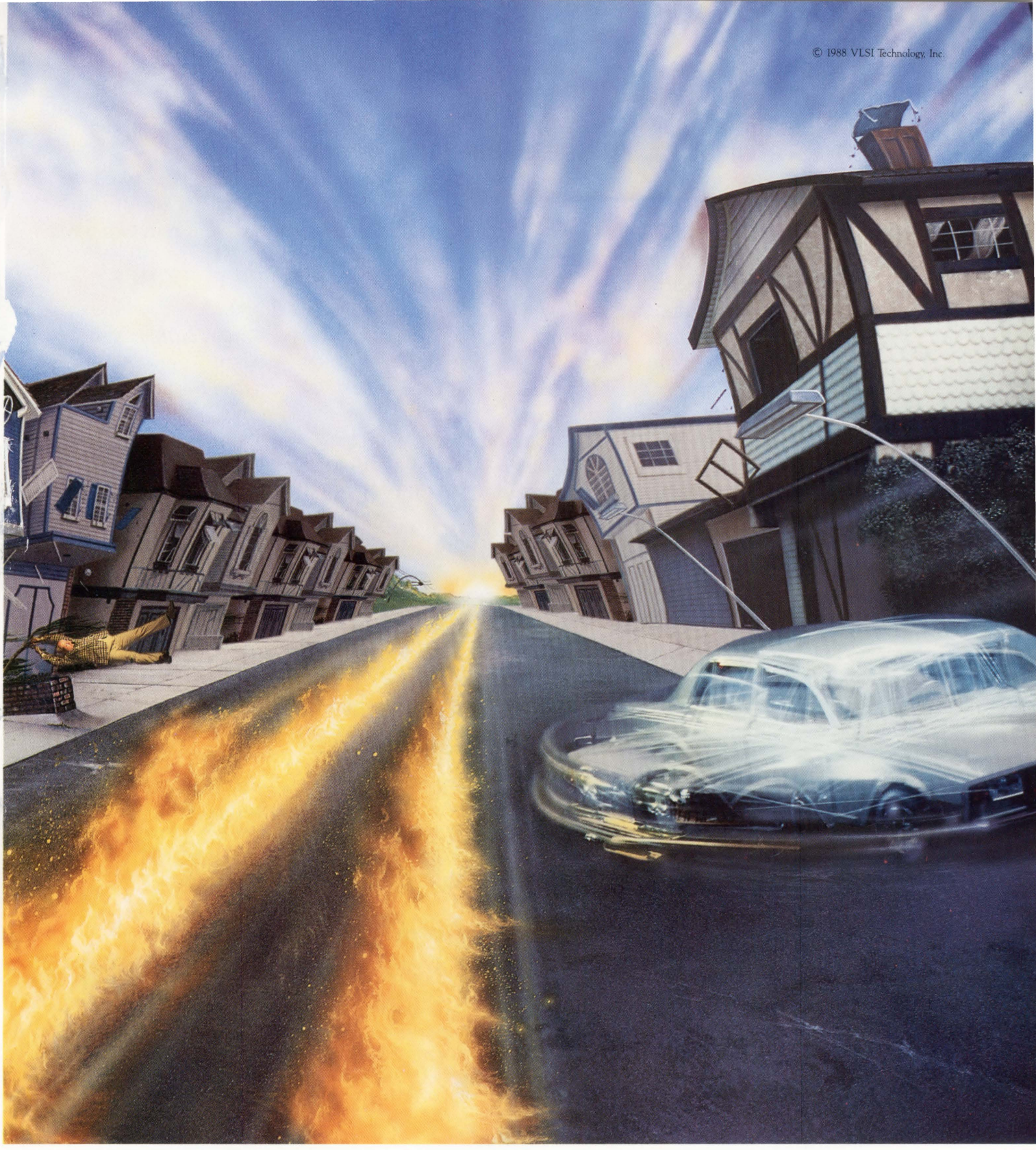

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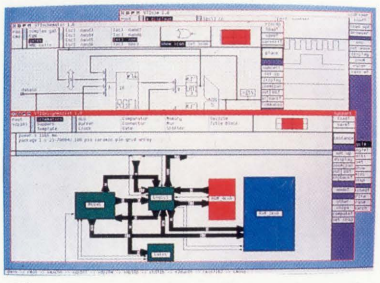
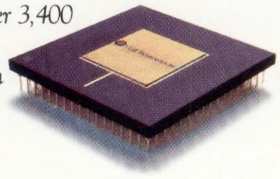


The Concept Express Design System's highly productive logic tools and silicon compilers were used to develop this very-large-scale ASIC. It incorporates a 2901 datapath, RAM, ROM, and over 3,400 gates of random logic.



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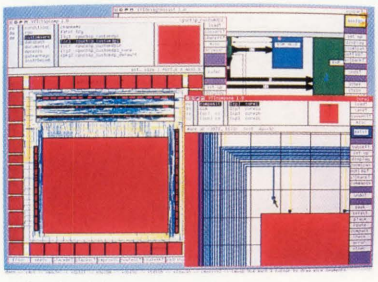
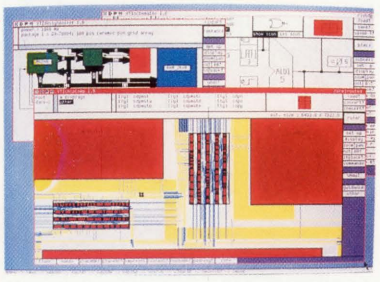
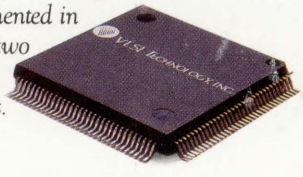


This highly-integrated design combines control logic, a register file, a refresh counter, and five peripheral chips onto a die size of 275x315 mils. The logic design, layout, and verification were completed in only 12 weeks.

SILICON EXPRESS™:



This design integrates all the peripheral chips for an AT computer with six megacells and control logic. Using the Silicon Express Design System, logic and physical designs like these can be implemented in under two man months.



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are likewise nearly impossible to model completely accurately. Finally, "error conditions," such as setup and hold violations, clock violations, and minimum pulse width violations, are often difficult to characterize.

Our experience with the test hospital was instrumental in identifying certain modeling problems and understanding model limitations. Here are a few things users need to understand about IC models, especially in regard to test program generation:

- *Models must initialize "conservatively."* Models must be as conservative as necessary in handling unknown nodes, to ensure that model outputs become asserted only when a circuit is correctly initialized. This requirement may call for the designer to add some extra circuitry or extra vectors to rigorously initialize the circuit.

- *Models must report all timing violations.* All timing relationships in logic blocks must be characterized, and error messages must be heeded by the user. Setup and hold violations on Clear and Set inputs, clock skew errors, or minimum pulse violations all can cause serious logic ambiguities. In all cases, the user must be notified by the model. Model violations cannot be tolerated during test-oriented simulation because even if the designer is aware of a model timing error and is sure it does not affect the system performance, it could very likely affect the test program.

- *A single simulation cannot represent best- and worst-case timing.* A single simulation run can verify timing at only one point in the performance spectrum (best-case, typical, worst-case). Since process performance scales linearly, this limitation is usually not too serious. Very difficult critical paths or possible race conditions, however, should be analyzed at both ends of the performance spectrum.

- *Noise and current effects cannot be simulated.* Since the simulator cannot consider noise, the designer must subscribe to design and simulation guidelines to avoid noise problems (for example, the maximum number of simultaneously switching outputs per power pair, the maximum number of outputs between grounds pads, no ground at corner of DIPs). VLSI Technology provides a comprehensive list of these requirements in its design and test guidelines.

FAULT SIMULATION ISSUES

Given the considerations above, prototype test vectors should be fault-graded. Several fault simulation techniques are available to perform the task (Goel and Moorby, 1984). For prototype test programs, probabilistic fault simulation can be used to obtain good estimates of their efficiency (Agrawal and Jain, 1985) at minimal cost, as test-oriented fault-free simulations are required anyway. A benefit of high-quality prototype tests is that production tests having very high fault coverage can be derived quickly from the existing prototype tests. Reciprocally, one does not need to wait until high production volumes to ensure high-quality shipments. □

ACKNOWLEDGMENTS

None of this work would have been possible without the initial leadership and continuing guidance of Bob Shur of VLSI Technology's design technology group. The authors also wish to thank Jim Althoff and Atiq Raza of VLSI Technology for their continuing support throughout the test hospital experiment.

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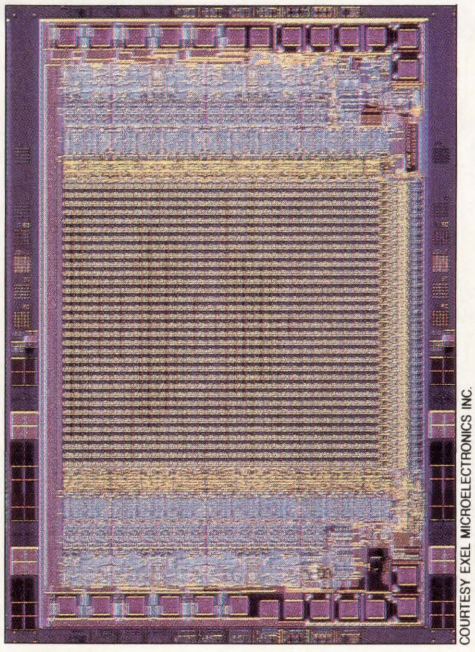
III DIRECTORIES



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GUIDE TO THE DIRECTORIES

This section of the *Guide* is a listing of gate array, cell library and PLD vendors and product lines and regional design centers. "Gate Array and Cell Library Vendor Profiles" gives customer interface (design data media), CAD system access, and price and deliveries. For the five media format choices, a bullet (•) shows company preference, an open bullet (○) means the company allows it, and a dash means the format is unacceptable.

A *functional* specification defines an architecture in terms of major function blocks, primary I/Os, and expected behavior. If the design is expressed with standard logic primitives, a *generic* logic schematic can be submitted. Working from a vendor's known library of macros can result in a *converted* logic schematic. If the vendor allows access to its CAD system or supports its libraries, a verified *netlist* can be submitted. Further, with access to the layout outlines of the library elements, graphical editing tools, and layout analysis programs, the design may be done by the customer, who hands over a verified *layout*.

The columns on CAD systems show the host computers on which the system runs. Whether customers can use the tools at the company *(on-site)*, from remote terminals *(remote)*, or on their own machines *(off-site)* is indicated with a bullet. A dash means access is not available. The final column lists the workstations, simulators, and layout systems the vendor supports.

In the NRE category, approximate development costs for a 3,000-gate digital IC are given. Vendors of GaAs, linear, and certain special ICs list cost estimates of typical devices. Turnaround time is measured from submission of a verified netlist to delivery of packaged tested prototypes. (Note: "n/s" means "not specified.")

In the "Directory of Gate Arrays," the number of array types (sizes) for each family is shown in parentheses next to the series name. Below the family name is the technology and the line width of this process. The column *programmable layers* lists the poly ("P") and metal ("M") layers available for customization, followed by the pitch of the wiring, where available. The "Directory of Cell Libraries" follow a similar format.

For arrays, we list the numbers of components available (spanning the smallest to the largest product in the family). The number of gates is for digital arrays or combined analog-digital arrays, and the number of active components is for linear arrays or array portions. We also list both digital I/Os and dedicated analog I/Os .

The listings in the "Directory of Programmable Logic Devices" are self-explanatory.

A separate listing, "ASIC Vendor Contacts," contains, for gate array and cell library vendors, the names, addresses, and phone numbers of all the companies and, in almost every case, a contact person for obtaining more information. In "Directory of ASIC Design Centers," vendor-owned and third-party design centers are listed by location under the manufacturer's contact information. Distributor contacts, on the other hand, are grouped at the end of the section.

Missing this year from the directories are Harris Semiconductor, Hitachi America, Interconics, McDonnell Douglas, SGS-Thompson, Supertex, Telmos, and Universal Semiconductor. Unfortunatley, these companies were unable to supply the necessary information in time for inclusion. Also not included is K-MOS Systems.

Gate Array and Cell Library Vendor Profiles

Company	Products	Customer interface					CAD system access					Nonrecurring expense ($K)		Turnaround (weeks)		Minimum production contract
		Functional	Generic	Converted	Netlist	Layout	CAD system hardware	On-site	Remote	Off-site	Workstations, simulators, and layout supported	GA	SC	GA	SC	
ABB HAFO	CMOS cell library	○	○	○	•	○	MicroVAX VAX	•	•	•	Daisy Mentor P-CAD Tektronix	n/s	40+	n/s	12-16	None
Actel	CMOS gate arrays	—	—	—	—	—	IBM PC 386	—	—	•	PC-386 Viewsim	n/s	n/a	2 hours	n/a	None
Adams Russell Semiconductor	GaAs D-MESFET cell library	•	—	—	—	•	VAX/Micro-VAX/IBM	•	—	•	None	n/a	35-40	n/a	8-10	4-wafer lot
Advanced Micro Devices	Bipolar gate arrays	•	•	•	•	○	IBM, VAX, Apollo	•	•	•	Mentor	Varies	n/s	8-9	n/s	None
Applied Micro Circuits	Bipolar and BiCMOS gate arrays and cell libraries	○	○	•	•	•	Apollo MicroVAX VAX Sun	•	•	•	Daisy Mentor Valid Lasar 6	25-95	n/s	7-12	n/s	None

Gate Array and Cell Library Vendor Profiles (continued)

Company	Products	Customer interface					CAD system access					Nonrecurring expense ($K)		Turnaround (weeks)		Minimum production contract
		Functional	Generic	Converted	Netlist	Layout	CAD system hardware	On-site	Remote	Off-site	Work-stations, sim-ulators, and layout supported	GA	SC	GA	SC	
Arrow Electronics	CMOS gate arrays and cell libraries	○	●	●	○	○	VAX Apollo	●	●	●	Daisy Mentor	n/s	n/s	4-8	6-12	None
AT&T Technologies	CMOS cell libraries; digital bipolar gate arrays	○	○	○	●	—	Apollo AT&T IBM MicroVAX VAX Sun	●	●	●	Daisy Mentor Valid	45	≥50	8	8-12	None
Barvon BiCMOS Technology	BiCMOS gate array; CMOS and BICMOS cell libraries	○	●	●	●	○	Apollo VAX MicroVAX	●	—	●	Mentor Silvar-Lisco	n/s	n/s	n/s	n/s	None
California Micro Devices	CMOS gate arrays and cell libraries	○	●	●	●	○	MicroVAX VAX	●	—	●	Daisy Mentor Viewlogic Tektronix	10-25	40-50	4-6	6-8	None
Cherry Semiconductor	Bipolar gate arrays	○	○	●	○	○	IBM PC	●	—	—	Applicon	27	—	12	—	None
Control Data	CMOS gate array; and cell libraries	—	—	●	●	—	Cyber 800 Apollo	●	●	●	Daisy Mentor	38	80	12	12	$100k/year (SC)
Custom Arrays	Linear bipolar gate arrays and cell library	●	●	●	●	●	IBM PC	●	●	●	Analog Design Tools PC AT PC-386	5-50	20-70	3	12-28	None
Custom Silicon	CMOS and bipolar gate arrays; CMOS cell libraries	●	○	○	○	—	MicroVAX IBM PC Apollo Sun	●	●	●	Mentor Daisy FutureNet Viewlogic	12	25	3	5-7	None
Data Linear	Bipolar analog arrays, and cell library	○	—	●	●	●	IBM PC MicroVAX VAX	●	●	●	Daisy Mentor Valid ADT Via	25-30 15-20 analog array	25-50	6-8	10-12	500 units/year
Design Devices	CMOS gate array and cell library	●	○	○	○	—	MicroVAX IBM PC Apollo	●	●	—	Mentor Valid	26	39	9-11	14-17	None
Electronic Technology	CMOS gate arrays; bipolar linear arrays; CMOS cell libraries	●	●	○	○	○	VAX SCS-40	—	—	—	Daisy Via	15	25	12	16	None
Exar	Bipolar linear arrays and cell library; CMOS gate arrays and cell library	○	●	●	●	○	VAX IBM PC (Linear) Apollo (digital)	●	●	●	Mentor	n/s	30	n/s	13	None
Ford Micro-electronics	GaAs E/D MESFET gate array	○	○	○	—	●	VAX 11/78X or 8600	●	—	●	Daisy	Ap-prox-imate-ly 75	Not yet avail-able	13	n/s	5 wafer units/year (GA)
Fujitsu Micro-electronics	CMOS, BiCMOS, and bipolar gate arrays; CMOS cell libraries	—	○	●	●	○	VAX MicroVAX IBM PC Apollo Sun Fujitsu Amdahl	●	●	●	Daisy HP Mentor Valid Tektronix	20	40	4	8	None

Gate Array and Cell Library Vendor Profiles (continued)

Company	Products	Customer interface					CAD system access					Nonrecurring expense ($K)		Turnaround (weeks)		Minimum production contract
		Functional	Generic	Converted	Netlist	Layout	CAD system hardware	On-site	Remote	Off-site	Work-stations, sim-ulators, and layout supported	GA	SC	GA	SC	
Gain Electronics	GaAs E/D MESFET gate array	○	○	●	●	—	IBM PC Apollo	●	—	●	Mentor Viewlogic	55	n/s	14	n/s	n/s
GE Micro-electronics Center	Si-gate CMOS gate array and cell library (CMOS/SOS gate array and cell library also available)	—	○	○	●	○	VAX 11/78X or 8600 MicroVAX Apollo Sun	●	●	●	Valid Mentor FutureNet	35	50	5	9	None
Genesis Microchip	CMOS gate array and cell library	o	●	○	○	—	IBM 30XX or 43XX IBM PC Apollo Sun	●	●	●	Mentor FutureNet Daisy	n/s	De-pends on con-tent	6	10	n/s
Gennum	Bipolar and digital linear arrays	●	○	○	○	●	IBM PC	—	—	●	Computer-Vision	6.9-40	n/a	8-12	n/a	None
GE Solid State	CMOS and SOS gate arrays and cell libraries	○	○	●	●	○	MicroVAX VAX Sun	●	●	●	Daisy FutureNet Mentor PCAD Valid	15-75	25-125	5	8	None
GigaBit Logic	GaAs cell library	○	○	○	●	○	VAX MicroVAX IBM PC	●	—	●	Daisy Mentor	—	75	—	16	None
Gould Semiconductor	CMOS gate arrays and cell library	○	●	●	●	●	Apollo IBM PC Prime Symbolics VAX	●	●	●	Daisy FutureNet Mentor P-CAD	14-19	21-26	6	8	Negotiable
Hamilton/Avnet	CMOS, bipolar, BiMOS, ECL, and SOS gate arrays; CMOS cell libraries.	—	○	●	●	●	MicroVAX IBM PC Sun	●	●	●	FutureNet Faircad LDS III Ikos MDE	30	40-60	8-12	10-16	None
Holt Integrated Circuits	CMOS analog and combo array; CMOS cell library	●	●	●	○	●	VAX	●	●	●	Calma	—	35-45	—	12-16	Negotiable
Honeywell Solid State Electronics Division	CMOS, bipolar, and rad-hard gate arrays	○	○	●	●	○	Apollo Elxsi Daisy	●	●	●	Daisy Mentor	30-100	—	4-6	—	None
Hughes Aircraft	CMOS gate arrays and cell libraries	○	○	●	●	●	VAX Apollo	●	—	—	Daisy Mentor	30-50	40-75	4-6	8-10	100 units/year (GA); 1,000 units/year (SC)
ICI Array Technology	CMOS gate array and cell library; bipolar ECL	○	●	●	○	—	Apollo	●	—	—	Mentor	15	30	6-10	12-16	None
Integrated Circuit Systems	CMOS gate arrays and cell libraries; GaAs cell libraries	○	●	○	○	○	Apollo IBM PC VAX	●	●	●	Daisy Mentor Calma	23	39	6	10	500k units and $12k/year (GA); 1k units and $25k/year (SC)

Company	Products	Customer interface					CAD system access					Nonrecurring expense ($K)		Turnaround (weeks)		Minimum production contract
		Functional	Generic	Converted	Netlist	Layout	CAD system hardware	On-site	Remote	Off-site	Work-stations, simulators, and layout supported	GA	SC	GA	SC	
Integrated Logic Systems	CMOS gate arrays and cell libraries	○	●	●	●	—	VAX	●	—	●	Daisy OrCAD Mentor	10-50	—	8-12	—	None
Intel	CMOS cell library	○	○	○	●	—	MicroVAX VAX	●	—	●	Daisy Mentor	—	Negotiable	—	8-12	Negotiable
International Microcircuits	CMOS gate arrays and cell libraries	—	●	●	●	○	Apollo VAX	●	—	●	Daisy Mentor	16.8	44.8	6	16	None
International Microelectronic Products	CMOS standard cells	○	●	●	●	●	IBM PC MicroVAX Sun	●	●	●	SST SCS Viewlogic Mentor	n/a	30-50	n/a	12	None
LSI Logic	CMOS/BiCMOS gate arrays and cell libraries	—	○	○	●	—	Apollo IBM MicroVAX Sun-3 Sun-4 VAX	●	●	●	Daisy Mentor Valid	n/s	n/s	2	6	None
Marconi Electronic Devices	CMOS and SOS gate arrays; CMOS and SOS cell libraries	○	○	○	●	○	Apollo VAX MicroVAX	●	●	●	Daisy Mentor	—	—	—	—	None
Matra Design Semiconductor	CMOS gate arrays	○	●	●	●	—	IBM PC MicroVAX VAX	●	●	●	Daisy Mentor Valid HP	5-40	—	3-6	—	None
MCE Semiconductor	CMOS and bipolar gate arrays and cell libraries	○	○	●	●	●	IBM PC	●	—	●	Calma	5	10	5-7	6-10	None
Micro Linear	Bipolar linear arrays	●	●	●	●	●	IBM PC Sun	●	●	●	ADT Calma Daisy Viewlogic	15-30	—	10-16	—	Negotiable
Micro LSI	CMOS gate array and cell library	●	●	○	○	○	Prime	●	—	—	Daisy	15-25	35-45	10	14	n/s
Micro-Rel	CMOS and bipolar cell library	●	○	○	●	●	Data General/MV Apollo	—	—	—	Calma Daisy Mentor	—	n/s	—	13	$100k/year (SC)
Mietec	CMOS and bipolar gate arrays and cell libraries	○	○	○	●	●	VAX MicroVAX	●	●	●	Daisy Valid	—	40	—	6	30k units per year and $100k/year (SC)
Mitsubishi Electronics America	CMOS gate arrays and cell library	—	○	●	●	○	IBM IBM PC Apollo Sun	●	●	●	Valid Mentor Daisy Intergraph HP Ikos Orchard FutureNet	10-30	30-60	4	10	$100K/year (SC)
Motorola	CMOS, BiMOS and bipolar gate arrays	—	○	●	●	○	IBM VAX Apollo Sun MicroVAX	●	●	●	Daisy FutureNet Mentor Valid	20	25-30	5	—	Negotiable

Gate Array and Cell Library Vendor Profiles (continued)

Company	Products	Customer interface					CAD system access					Nonrecurring expense ($K)		Turnaround (weeks)		Minimum production contract
		Functional	Generic	Converted	Netlist	Layout	CAD system hardware	On-site	Remote	Off-site	Work-stations, simulators, and layout supported	GA	SC	GA	SC	
National Semiconductor	CMOS and ECL gate arrays; CMOS and ECL cell libraries	—	○	●	●	○	IBM VAX MicroVAX	●	●	●	Daisy FutureNet Mentor Valid Sun	Negotiable	Negotiable	3-4	7-9	None
NCM	CMOS gate arrays and cell libraries	○	○	○	○	○	Silicon Graphics	—	—	—	GEM	8-16	25-30	4	10	None
NCR Microelectronics	CMOS gate arrays and cell libraries	○	○	○	●	○	VAX	●	●	●	Cadnetix Daisy Mentor Valid FutureNet	12-20	30-50	3-5	8-10	None
NEC Electronics	CMOS, BiCMOS, and bipolar gate arrays; CMOS cell library	○	○	●	●	○	NEC-Acos VAX Sun	●	●	●	Cadnetix Daisy FutureNet HP Mentor Valid	Negotiable	Negotiable	4-7	7-10	Negotiable
Oki Semiconductor	CMOS gate arrays, and cell libraries	—	●	●	●	●	IBM Amdahl VAX	●	●	●	Daisy Mentor Valid Sun FutureNet	20-22	35	4	8	10 units–100 units
Panasonic	CMOS gate arrays and cell libraries	—	○	●	●	—	VAX MicroVAX Fujitsu	●	—	●	Daisy Mentor	18	35	3-4	6-10	None
Plessey Semiconductor	Bipolar and CMOS linear arrays, gate arrays, and cell libraries	○	●	●	●	●	Apollo IBM PC Sun VAX MicroVAX	●	●	●	ADT Daisy Mentor Valid FutureNet	5-50	25-80	6-10	8-16	$50K per year (GA); $80K per year (SC)
Polycore Electronics	Bipolar linear arrays	●	●	●	●	●	IBM PC	—	—	—	IBM PC-ICED	5	—	6	—	None
Raytheon Semiconductor	Bipolar and CMOS gate arrays	●	○	●	●	●	VAX Amdahl	●	●	●	Daisy Mentor Valid	15-75	—	8-12	—	Program-dependent
Seattle Silicon Corp.	CMOS cell libraries	○	○	●	●	○	Apollo	●	—	●	Mentor	n/a	35	n/a	8	None
Sierra Semiconductor	CMOS cell library	○	○	●	●	●	Apollo Elxsi VAX Sun	●	—	●	Daisy Mentor	—	30	—	12	None
Signetics/Philips	CMOS cell libraries	●	○	○	●	○	Apollo VAX IBM PC	●	●	●	Mentor OrCAD Daisy Valid	—	30-50	—	10-14	$100k per year
Siliconix	CMOS gate arrays	○	○	○	○	—	IBM IBM PC VAX	●	—	●	Case Daisy FutureNet Mentor	10	—	6	—	None
Silicon Systems	Bipolar gate arrays; bipolar and CMOS linear arrays; CMOS cell libraries	●	●	○	○	○	Apollo VAX MicroVAX	—	—	●	—	20-40	35-75	6-10	8-12	1k units/year or $50k/year (GA); 10k units/year or $100k/year (SC)

Company	Products	Customer interface					CAD system access					Nonrecurring expense ($K)		Turnaround (weeks)		Minimum production contract
		Functional	Generic	Converted	Netlist	Layout	CAD system hardware	On-site	Remote	Off-site	Work-stations, sim-ulators, and layout supported	GA	SC	GA	SC	
Silicon West	CMOS gate arrays and cell library	●	●	○	○	—	Apollo VAX	—	—	—	Mentor	30	40	6-8	8-10	None
S-MOS Systems	CMOS gate arrays and cell library	—	○	●	●	●	MicroVAX IBM IBM PC Apollo Sun	●	—	●	Daisy Mentor FutureNet OrCAD Viewlogic	18	36	5-7	11-14	5k units/year (GA); 10k units/year (SC)
Standard Microsystems	CMOS cell libraries	○	●	●	●	●	Apollo IBM PC MicroVAX VAX	●	—	●	Daisy Mentor Metheus-CV Valid Viewlogic	—	15-35	—	6-10	$50k/year (SC)
Tachonics	GaAs D-MESFET cell library	—	○	○	●	●	Apollo	●	—	●	VLSI Technology Mentor	—	75	—	10	None
Tektronix	Bipolar linear and digital arrays	○	○	●	○	○	MicroVAX VAX	●	—	●	Tektronix	60	—	6	—	None
Texas Instruments	CMOS gate arrays and cell libraries	●	●	●	●	○	Apollo IBM	●	●	●	Daisy Mentor Valid	15-25	30-40	2-3	3-6	None
TLSI	CMOS gate arrays; CMOS and nMOS cell libraries	●	●	●	○	●	IBM PC MicroVAX	●	—	—	Calma Daisy	20	35	8	12	None
Toshiba America	CMOS gate arrays and cell libraries	●	●	○	○	●	IBM/VAX	●	●	●	Daisy FutureNet Mentor Valid Viewlogic HP Aida P-CAD	9-90	15-50	2.5-4	7-12	None
TriQuint Semiconductor	GaAs D-MESFET standard cell, E/D-MESFET gate arrays and cell libraries	○	○	○	●	●	Daisy Logician Apollo VAX MicroVAX	●	—	—	Daisy Mentor	45-60	60-120	10	14	None
Unicorn Micro-electronics	CMOS gate arrays and cell library	●	●	●	●	●	MicroVAX VAX	●	●	●	Daisy	5-20	25-45	4-8	12-16	None
United Silicon Structures (US2)	CMOS cell library	○	○	○	○	●	VAX 11/78X or 8600 MicroVAX IBM PC Apollo Sun	●	—	●	Sun-3 Apollo DN3000, DN4000 DEC VAX station	n/a	15	n/a	6	One unit/year (SC)
United Technologies Micro-electronics Center	CMOS and rad-hard CMOS gate arrays and cell libraries	○	○	●	●	●	MicroVAX VAX	●	●	●	Daisy Mentor Valid	30	50	6-8	8-12	None
Vitesse Semiconductor	GaAs E/D-MESFET gate arrays and cell library; mixed D and E/D-MESFET gate arrays	○	○	○	●	○	VAX 11/78X or 8600 MicroVAX Apollo, Sun Daisy	●	●	●	Daisy Mentor Merlyn-G VLSI Tools	Con-tact factory	Con-tact factory	8-10	n/s	Contact factory

Gate Array and Cell Library Vendor Profiles

Company	Products	Customer interface					CAD system access					Nonrecurring expense ($K)		Turnaround (weeks)		Minimum production contract
		Functional	Generic	Converted	Netlist	Layout	CAD system hardware	On-site	Remote	Off-site	Work-stations, simulators, and layout supported	GA	SC	GA	SC	
VLSI Technology	CMOS gate arrays and cell libraries	○	○	●	●	●	Apollo Elxsi HP MicroVAX Sun VAX	●	●	●	HP Daisy Mentor FutureNet	16-150	n/s	3	5-6	Contact sales
VTC	CMOS and bipolar gate arrays and cell libraries	○	○	●	●	○	Apollo IBM PC	●	●	●	Mentor Daisy	25	50	6	12	None
WaferScale Integration	CMOS cell library	●	●	●	●	○	VAX	●	●	●	Daisy Intergraph	—	60	—	16	Contact sales
Xerox Microelectronics Center	CMOS and ECL gate arrays; CMOS and ECL cell libraries	●	●	○	○	—	VAX-11/78x or 8600 (some software), Xerox 6085 workstations	●	●	—	Xerox 6085	20-35	40-55	4-10	6-12	None
Xilinx	CMOS gate arrays	○	●	●	n/a	n/a	IBM PC Apollo Sun Daisy	n/a	n/a	n/a	Daisy Mentor IDEA Valid PC	—	n/a	—	n/s	None
Zymos	CMOS cell libraries	○	●	●	●	—	IBM PC Prime	●	●	●	Case	n/a	Contact sales	n/a	Varies	Contact sales

Directory of Gate Arrays

Company	Product Technology Line width	Program-mable Layers	Typical Parameters			Components		Interface levels[4]			Temp. ranges[5]			Second Sources
			MHz[1]	mW[2]	ns[3]	Gates	I/Os	C	T	ECL	C	I	M	
Actel Corp.	Act1 (2) Si-gate CMOS 2 μm	M1 6 μm M2 7 μm	70	n/s	2.7	1200-2000	57-69	●	●		●			None
Advanced Micro Devices	Am3500 Bipolar OI (ECL) 1.5 μm	M1 6 μm M2 9 μm	650	1-4	0.4-0.6	4988	134			10K, 100K	●			None
	Am3525 Bipolar OI (ECL) 1.5 μm	M1 6 μm M2 9 μm	650	1–4	0.4–0.6	3718 + 1152 bits RAM	135			10K, 100K	●			None
	Am3550 (5) Bipolar OI (TTL, STTL, ECL) 1.5μm	M1 6 μm M2 9 μm	560	2	0.4	1568–5228	48–124		●	10KH, 100K	●			None
	Am3530 Bipolar OI (TTL, STTL, ECL) 1.5 μm	M1 6 μm M2 9 μm	560	2	0.4	410	20		●	10KH, 100K	●			None

1. Flip-flop toggle rate. 2. Gate power at frequency. 3. 2-in NAND delay, FO = 2, 1 mm wire. 4. C = CMOS, T = TTL. 5. C = commercial, I = industrial, M = military.

Directory of Gate Arrays (continued)

Company	Product Technology Line width	Programmable Layers	Typical Parameters			Components		Interface levels[4]			Temp. ranges[5]			Second Sources
			MHz[1]	mW[2]	ns[3]	Gates	I/Os	C	T	ECL	C	I	M	
Applied Micro Circuits	Q5000 (5) Bipolar OI (TTL, STTL, ECL) 2 μm	M1 5.6 μm M2 8.0 μm M3 (only on Q5000T)	800	0.9	0.35	1300–5000	76–160		•	10K, 100K	•	•	•	Signetics/-Philips
	Q14000 (4) Si-gate CMOS and bipolar OI (TTL, ECL) 1.5 μm	M1 4.5 μm M2 4.5 μm M3 6 μm	240	0.02	0.67	2100–14,000	80–226	•	•	10K, 100K	•	•	•	S-MOS
	Q20000 (3) Bipolar trench isolation 1 μm	M1 4 μm M2 5 μm M3 7 μm	1.5 GHz	0.5	0.09	2000-16,000	244		•	•	•	•	•	Plessey
AT&T Microelectronics	ALA-200 Bipolar JI (IIV) 1.5 μm	M1 5 μm M2 10 μm	4.5 GHz	n/a	n/a	111-222 active 501-998 passive	36-48		•	•	•	•	•	None
	ALA-300 Bipolar JI (90V) 8 μm	M1 10 μm M2 10 μm	250	n/a	n/a	29-116 active 111-444 passive	30-32		•	•	•	•	•	None
	ALA-400 Bipolar JI (30 V) 4 μm	M1 8 μm M2 8 μm	250	n/a	n/a	122-208 active 417-670 passive	38-42	•	•	•	•	•	•	None
	DBIC gate array (TTL, ECL)	M1 5 μm M2 5 μm	600	1.25	0.2	2000-6000	72-120			10K				n/s
Barvon BiCMOS Technology	BC9000 (1) BiCMOS (bipolar and Si-gate CMOS) 2 μm	M1 M2	100	n/s	1.5	2000 gates 18 analog 900 passive	68 total	•	•		•	•	•	None
California Micro Devices	C3000 (4) Si-gate CMOS 3.5 μm	P1 7 μm M1 7 μm	15	0.44	2.1	500–2000	40–80	•	•		•	•	•	None
	C2000 (8) Si-gate CMOS 2 μm	M1 4.5 μm M2 5.5 μm	30	0.8	1.2	1500–10,000	72–250	•	•		•	•	•	None
Cherry Semiconductor	1200, 1300, 1400 Bipolar JI (I^2L) 4 μm	M1 16 μm	3	0.7	50	192–288 gates 50–106 active	24–28 2–6 analog	•	•	•	•	•		Exar
	Genesis (4) Bipolar JI (I^2L) 4 μm	M1 16 μm	3	0.4	50	64–256 gates 143–69 active 345–200 passive	10—18 16–22 analog	•	•		•	•	•	Exar
Commodore Semiconductor	4100 Series Si-gate CMOS 2 μm	M1 5 μm M2 7 μm	80	1	1.2	500–6000	40–152	•	•		•			None
Control Data	VLSI-6200 Si-gate CMOS 2 μm	M1 5.5 μm M2 7 μm	40	0.24	0.85	8500	154	•	•		•	•	•	National, VTC
	VLSI-6100 Si-gate CMOS 1.25 μm	M1 3.5 μm M2 4.5 μm	40	0.2	0.8	8500	154	•	•		•	•	•	National, VTC
	VLSI-7000 Si-gate CMOS 1.25 μm	M1 2.5 μm M2 2.5 μm	75	0.2	0.5	20,000	238	•	•		•	•	•	Honeywell Digital Products
Custom Arrays	MM 20 V bipolar (9) Bipolar JI 6 μm	M1	n/s	n/s	n/s	45–280 active 100–1150 passive	14–46		•	•	•	•	•	Ferranti Interdesign
	MV 40 V bipolar (5) Bipolar JI 6 μm	M1	n/s	n/s	n/s	68–340 active 360–1400 passive	20-44		•	•	•	•	•	Ferranti Interdesign

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Directory of Gate Arrays (continued)

Company	Product Technology Line width	Programmable Layers	Typical Parameters			Components		Interface levels[4]			Temp. ranges[5]			Second Sources
			MHz[1]	mW[2]	ns[3]	Gates	I/Os	C	T	ECL	C	I	M	
Custom Silicon	SLA-8000 (10) Si-gate CMOS 1.2 μm	M1 3.5 μm M2 5 μm	120	1.45	.52	5000-130,000	86-308	•	•		•	•	•	Seiko
	HCA 62A00 (8) Si-gate CMOS 2 μm	M1 5.25 μm M2 6 μm	50	1	1.5	648-8568	44–168	•	•		•	•	•	Motorola, NCR
	MH–15 Volt (8) Si-gate CMOS 4 μm	M1 8 μm	40	n/s	Depends on voltage	70-1600 gates 8-84 active	18-84	•	•		•	•	•	Plessey
	SLA–1.5 Volt (6) Si-gate CMOS 2 μm	M1 M2	10 @ 3 V 1 @ 1.5 V	2.2	8.5 @ 1.5 V	1632–8000	78–178	•	•		•	•	•	Seiko
	HDC 100 (10) Si-gate CMOS 1 μm	M1 3.6 μm M2 4 μm M3 4 μm	175	1	0.45	5670-104,832	99-512	•	•		•			Motorola
	MM–15 Volt (9) Bipolar JI 5 μm	M1 18 μm	350[6]	n/s	n/s	41-276 active 50-369 passive	14-46 analog I/O	•	•	all	•	•	•	Plessey
	MV-40 Volt (5) Bipolar JI 5 μm	M1	n/s	n/s	n/s	58-203 active 216-924 passive	16-36 analog I/O	•	•	all	•	•	•	Plessey
Data Linear	DL104–650 analog arrays (5) Bipolar DI 5 μm	M1 15 μm	0.5–1 GHz[6]	n/s	2	56–347 active 28–173 passive	14–34 analog	•	•	10K, 100K	•	•	•	None
	SP1104 Bipolar DI 4 μm	M1 7 μm M2 15 μm	npn, 1 GHz; pnp, 0.6 GHz	20 V; 35 V	n/s	444 active NiCr 800 KΩ Pinch 1.2 MΩ 14 MOS caps 6 zeners	24	•	•		•	•	•	None
	SP1204 Bipolar DI with JFETS 4 μm	M1 7 μm M2 15 μm	npn, 1 GHz; pnp, 0.6 GHz	20 V 35 V	n/s	440 active 16 JFETS 2 zeners pinch 400 KΩ NiCr 800 kΩ or SiCr 6 MΩ	40	•	•	•	•	•	•	None
Design Devices	CMOS gate arrays Si-gate CMOS 2 μm	M1 6 μm M2 9 μm	50	1.05	1.75	300–13,500	44–200	•	•		•	•	•	None
	Si-gate CMOS 1.5 μm	M1 5.6 μm M2 6 μm	150	0.14	0.7	5300-129,000	70-370	•	•		•	•		None
Electronic Technology	A5S (13) Bipolar OI (TTL) 5 μm	M1 10 μm	1	4	n/s	37–298 active	14–40	•	•		•	•	•	Exar
	D2D, D3D, D5S (6) Si-gate CMOS	M1 M2	65	0.56	0.9/1.4	600–5000	44–124	•	•		•	•	•	Motorola, NCR, Gould
	Bipolar linear (15) Bipolar JI 7 μm	n/s	n/s	n/s	n/s	n/s	14–40		n/s		•	•	•	Exar
Exar	Flexar Bipolar (analog) 3 μm	M1 M2	1 GHz[6]	n/s	n/s	800	48	•	•	•	•	•	•	Rohm
Ford Microelectronics	Gate array (1) GaAs E/D MESFET (proprietary Ford logic) 1.5 μm	M1 5 μm M2 4 μm	1 GHz	0.6	170 ps	3000	68			100K	•			n/s

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Company	Product Technology Line width	Programmable Layers	Typical Parameters			Components		Interface levels[4]			Temp. ranges[5]			Second Sources
			MHz[1]	mW[2]	ns[3]	Gates	I/Os	C	T	ECL	C	I	M	
Fujitsu Microelectronics	ET-H ECL (1) Bipolar ECL 0.5 μm	M1 4.5 μm M2 4.5 μm M3 4.5 μm	1000	1.62	.100	9856	200			10K, 100K	•			None
	ET ECL (5) Bipolar OI (ECL) 1 μm	M1 <5 μm M2 5 μm	800	1.83	0.22	1056–6160	64–136		•	10K, 100K	•			None
	ETM ECL (2) Bipolar OI (ECL) 1 μm	M1 <5 μm M2 5 μm	800	1.83	0.25	2640–3960 4.6–9.2K RAM	136		•	10K, 100K	•			None
	BC-H (1) BiCMOS 1 μm	M1 4 μm M2 4 μm M3 4 μm	250	4.5	.57	11968	200		•	•	•			None
	BiCMOS (4) Si-gate CMOS and bipolar JI 1.5 μm	M1 <6 μm M2 6 μm	180	4.5	0.65	645–3240	52–112		•		•	•		None
	HB-LSTTL (2) Bipolar JI (STTL) 2 μm	M1 6 μm M2 9 μm	70	0.8	2.4	528–1080	60–88		•		•	•		None
	H-LSTTL (5) Bipolar JI (STTL) 2 μm	M1 6 μm M2 9 μm	150	0.8	1.25	360–3162	40–112		•		•	•	•	Texas Instruments
	AV CMOS (5) Si-gate CMOS 1.8 μm	M1 6 μm M2 9 μm	85	2.2	1.4	2600–8000	106–160	•	•		•	•	•	None
	AVB CMOS (6) Si-gate CMOS 1.8 μm	M1 6 μm M2 8 μm	85	2.2	1.4	350–2000	42–92	•	•		•	•	•	None
	AVM CMOS (3) Si-gate CMOS 1.8 μm	M1 6 μm M2 8 μm	85	2.2	1.4	1500–4000 2K RAM	114–127	•	•		•	•	•	None
	UH CMOS (1) Si-gate CMOS 1.5 μm	M1 4.5 μm M2 6 μm M3 9 μm	105	2.1	1.0	20,000	220	•	•		•	•		None
	UHB CMOS (11) Si-gate CMOS 1.5 μm	M1 4.5 μm M2 6 μm M3 9 μm	115	2.3	0.9	330–12,000	60–220	•	•		•	•		None
	UM CMOS (2) Si-gate CMOS 1.5 μm	M1 4.5 μm M2 6 μm M3 9 μm	105	2.1	1.0	10,000–15,000 6–12K RAM	219	•	•		•	•		None
	AU CMOS (5) Si-gate CMOS 1.2 μm	M1 3.5 μm M2 5 μm M3 7 μm	120	2.4	0.7	30,000–100,000	200–350	•	•		•	•		None
	AVL CMOS (6) Si-gate CMOS 2.3 μm	M1 6 μm M2 8 μm	10	n/s	10.8	350–2000	42–92	•			•	•		None
Gain Electronics	GFL2000, GFL4000, GFL7000 (3) GaAs E/D MESFET (GFL patent pending) 1 μm	M1 M2	1000	1.2	247	2000-7000	80-176		•	10K	•			n/s
GE Microelectronics Center	GEGATEAGC-40000/ TAGC40000 CMOS and megarad version "T" (CMOS/SOSrad-hard process also available) 1.25 μm	M1 3 μm M2 4 μm	40	0.5	0.7	1700-13,500	60-172	•	•				•	None
Genesis Microchip	SCX6B (9) Si-gate CMOS 1.5 μm	M1 M2	100	n/s	0.6	400-15,000	28-200	•	•		•	•	•	National

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Directory of Gate Arrays (continued)

Company	Product Technology Line width	Program-mable Layers	Typical Parameters			Components		Interface levels[4]			Temp. ranges[5]			Second Sources
			MHz[1]	mW[2]	ns[3]	Gates	I/Os	C	T	ECL	C	I	M	
Gennum	LA250 (3) Bipolar JI (analog) 8 μm	M1 8 μm	20	n/a	20	96–207 active 38–132 passive	24–40	•	•	•	•	•	•	Polycore
	LA200 (3) Bipolar JI (analog) 8 μm	M1 8 μm	20	n/a	20	37–122 active 26–58 passive	14–24	•	•	•	•	•	•	Polycore
	GA900 Bipolar (analog) 4 μm	M1 4 μm	200	n/a	2	140-280 active 110 passive	28-48	•	•	•	•	•	•	None
GE Solid State	PA60,000 (2) Si-gate SOS 4 μm	M1 10 μm	10	0.15	2	650–1200	78–106	•			•	•	•	None
	PA40,000 (6) Si-gate CMOS 3 μm	M1 10 μm	10	0.2	2.5	250–1200	76–106	•	•		•	•	•	None
	PA50,000 (6) Si-gate CMOS 3 μm	M1 10 μm M2 13 μm	15	0.3	2.5	680–6000	74–180	•	•		•	•	•	LSI Logic
	CGA10 (6) Si-gate CMOS 2 μm	M1 5.8 μm M2 7.5 μm	50	20	1.1	960-8000	56-140	•	•		•	•	•	VLSI Tech-nology
	CGA200 (13) Si-gate CMOS 1.5 μm	M1 4.8 μm M2 6.2 μm	250	1.5	0.8	960-54,000	48-348	•	•		•	•	•	VLSI Tech-nology
Gould Semi-conductor	B (7) Si-gate CMOS 2 μm	M1 5 μm M2 7 μm	50	2	1.3	1000–10,000	68–208	•	•		•	•		Contact company
	Si-gate CMOS 1.25 μm	M1 M3	100	n/s	0.6	2000–14,000	52–152	•	•		•	•		Contact company
Holt Integrated Circuits	HI 5100 (1) Si-gate CMOS 3 μm	M1 8 μm	20	0.2	6	73 gates 254 active 255 passive	12 40 analog	•	•		•	•	•	None
	HI 5300 Si-gate CMOS 3 μm	M1 8 μm	20	0.2	6	178 gates op amps, comparators, current source, 86 passive, 1 bipolar transmitter	64	•	•		•	•	•	None
Honeywell Solid State Electronics Division	HCT5000 Si-gate CMOS 1.2 μm	M1 M2	40	0.24	0.3	5000	96	•	•		•	•	•	None
	HCT15000 Si-gate CMOS 1.2 μm	M1 M2	40	0.24	0.3	15,000	144	•	•		•	•	•	None
	HC20000 Si-gate CMOS 1.2 μm	M1 M2	50	0.30	0.3	20,000	238	•	•		•	•	•	None
	HC40000 Si-gate CMOS 1.2 μm	M1 M2	50	0.30	0.3	40,000	300	•	•		•	•	•	None
	HCS15000 Si-gate CMOS 1.2 μm	M1 M2	25	0.30	0.4	12,000	144	•	•				•	None
	HM3500 Bipolar OI 2.5 μm	M1 M2	500	2.0	0.3	3500	120		•	•	•	•	•	None
	HVM10000 Bipolar OI 1.2 μm	M1 M2	300	0.4	0.2	10,000	256		•	•	•	•	•	None
	HE12000 Bipolar OI 1.2 μm	M1 M2	600	0	0.1	12,000	256		•	•	•			None

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Company	Product Technology Line width	Programmable Layers	Typical Parameters			Components		Interface levels[4]			Temp. ranges[5]			Second Sources
			MHz[1]	mW[2]	ns[3]	Gates	I/Os	C	T	ECL	C	I	M	
Hughes Aircraft	U series (11) Si-gate CMOS 2 μm	M1 5 μm M2 7 μm	200	1.2	1.2	1000–41,000	40–248	•	•		•	•	•	None
	HL5000 (8) Si-gate CMOS 3 μm	M1 M2	n/s	0.02/ MHz	2.4	504–6000	52–180	•	•		•	•	•	LSI Logic
	HL7000 (8) Si-gate CMOS 2 μm	M1 M2	n/s	0.02/ MHz	1.4	880–10,013	68–232	•	•		•	•	•	LSI Logic
	HL9000 (8) Si-gate CMOS 1.5 μm	M1 M2	n/s	0.02/ MHz	1.0	880–10,013	68–232	•	•		•	•	•	LSI Logic
	HL10,000 (4) Si-gate CMOS 1.5 μm	M1 M2	n/s	0.01/ MHz	0.7	50,000–129,000	120– 256	•	•		•	•	•	LSI Logic
ICI Array Technology	DHS (10), HCD (3) Si-gate CMOS 1.5, 2, and 3 μm	P1 M1 1.5, 2, 3 μm	40	0.07	2	150–2650	38–86	•	•		•			None
Integrated Circuit Systems	VGT10 Si-gate CMOS 2 μm	M1 6μm M2 6μm	70	0.2	1.0	800–10,000	40–140	•	•		•	•	•	VLSI Technology
	VGT100 Si-gate CMOS 1.5 μm	M1 6μm M2 6μm	85	0.13	0.7	3700–66,000	84–384	•	•		•	•	•	VLSI Technology
	SCX Si-gate CMOS 2 μm	M1 6μm M2 6μm	66	0.2	1.0	600–8,700	40–155	•	•		•	•	•	National Semiconuctor
Integrated Logic Systems	CA15 (6) Si-gate CMOS 1.5 μm	M1 7 μm M2 7 μm	150	1	0.7	1960-41,568	48–194	•	•		•	•	•	None
	15GH (5) Si-gate CMOS 1.5 μm	M1 6 μm M2 6 μm	150	1	0.7	30,400–100,512	146– 260	•	•		•	•	•	None
International MicroCircuits	G4000 (8) Me-gate CMOS 8 μm	M1	2.0	0.015	70	75–600	23–53	•	•		•	•	•	S-MOS Systems
	G70000 Si-gate CMOS 3.5 μm	P1 M1	42	0.42	3.3	135–2535	28–88	•	•		•	•	•	S-MOS Systems
	IMI6000 (7) Si-gate CMOS 2 μm	P1 M1 M2	60	0.6	1.4	820–6204	60–158	•	•		•	•	•	S-MOS Systems
	IMI7000 Si-gate CMOS 1.5 μm	P1 M1 M2	100	n/s	0.75	1632-8000	70-170	•	•		•	•	•	S-MOS Systems
International Micro-Electronic Products	Si-gate CMOS (5) 1.2 μm	M1 4 μm M2 4.5 μm	40	1.4	1	800–15,000	40–110	•	•		•	•		National Semiconductor, VLSI Technology
LSI Logic	LCA100K (3) Si-gate CMOS 0.7 μm	M1 M2 M3	n/s	0.01/ MHz	0.46	50,000–100,000	316-418	•	•		•	•	•	Contact company

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Directory of Gate Arrays (continued)

Company	Product Technology Line width	Programmable Layers	Typical Parameters			Components		Interface levels[4]			Temp. ranges[5]			Second Sources
			MHz[1]	mW[2]	ns[3]	Gates	I/Os	C	T	ECL	C	I	M	
LSI Logic	LMA9000 (10) Si-gate CMOS 1.5 μm	M1 M2	n/s	0.012/ MHz	0.57	700–15,000	41–174	•	•		•	•	•	Contact company
	LCA10000 (6) Si-gate CMOS 1.5 μm	M1 M2 M3	n/s	0.012/ MHz	0.57	10,000– 50,000	76–256	•	•		•	•	•	Contact company
	LSA1500 (4) Si-gate CMOS 1.5 μm	M1 M2	n/s	0.012/ MHz	0.57	22,000– 38,000 18K-32K RAM	234	•	•		•	•	•	Contact company
	LL9000 (8) Si-gate CMOS 1.5 μm	M1 M2	n/s	0.018/ MHz	1.0	880-10,013	68-232	•	•		•	•	•	Contact company
	LL7000 (8) Si-gate CMOS 2 μm	M1 M2	n/s	0.018/ MHz	1.4	880-10,013	68-232	•	•		•	•	•	Contact company
	LSA2000 (11) Si-gate CMOS 2 μm	M1 M2	n/s	0.018/ MHz	1.4	4000-6900 2K-9K RAM	190	•	•		•	•	•	Contact company
	LDD10000 (6) Si-gate BiCMOS 1.5 μm	M1 M2	n/s	0.012/ MHz	0.57	8000-43,500 CMOS 375-1330 biCMOS	144-256	•	•		•	•	•	Contact company
Marconi Electronic Devices	MA2000A (5) Si-gate CMOS 3 μm	M1 8 μm M2 8 μm	60	0.18	1.6	1120–6864	48–128	•	•		•	•	•	None
	MA9000 (3) Si-gate CMOS/SOS 2.5 μm	M1 8 μm M2 8 μm	60	0.1	1.2	748–4048	48–106	•	•		•	•	•	None
	MA8304 (1) Si-gate CMOS 3 μm	P1 6 μm M1 6.5 μm	35	0.11	3	392	26	•	•		•	•	•	United Micro-electronics
	MA4000 (4) Si-gate CMOS 2 μm	M1 6 μm M2 6 μm	100	0.2	0.9	3904– 10,044	96–160	•	•		•	•	•	None
Matra Design Semi-conductor	MA (4) Si-gate CMOS 2.5 μm	P1 6.5 μm M1 10 μm	25	0.018/ MHz	2	228–1139	32–62	•	•		•	•	•	None
	MB (9) Si-gate CMOS 2 μm	P1 4 μm M1 6 μm M2 9 μm	45	0.015/ MHz	1	810–7500	73–191	•	•		•	•	•	Plessey
MCE Semi-conductor	MCE Uniray Bipolar JI (analog) 5 μm	M1 11 μm	50	20	15	38–220 71–592 active	n/s	•	•	•	•	•	•	Ferranti Inter-design
	MCE MGC (7) Me-gate CMOS 5 μm	M1 10 μm	5	2	16	75–984	22–68	•	•		•	•	•	Master Logic
Micro Linear	FB900 (6) Bipolar JI (analog) 5 μm	M1 20 μm	30	n/s	10	50–205 active 120–607 passive	18–28	•	•	10K	•	•	•	Cherry, Exar, Ferranti Inter-design, MCE
	FB300 (5) Bipolar JI (analog/digital) 4 μm	M1 16 μm M2 22 μm	100	n/a	4	120 gates 252–319 active 741–907 passive	22 digital 24–44 analog	•	•	10K	•	•	•	None
	FB3600 (3) Bipolar JI (analog/digital)	M1 14 μm M2 22 μm	100	n/a	4	256–720 active 678–1816 passive	24–44 digital or analog	•	•	10K	•	•	•	None
	FB3400 (2) Bipolar JI (analog)	M1 20 μm M2 22 μm	30	n/a	10	200–540 active 508–1362 passive	28–44 analog or digital	•	•	10K	•	•	•	None

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Company	Product Technology Line width	Programmable layers	Typical parameters			Components		Interface levels[4]			Temp. ranges[5]			Second sources
			MHz[1]	mW[2]	ns[3]	Gates	I/Os	C	T	ECL	C	I	M	
Micro LSI	µGA Si-Gate CMOS 3 µm	P1 5 µm M1 7 µm	90	3.5	1.1	200–3500	120	•	•		•	•		None
	ULSI 20 Si-gate CMOS 2 µm	M1 6 µm M2 8 µm	90	3.5	1.1	200	26 10% analog	•	•			•		None
Mietec	MTC CMOS Si-gate CMOS 2.4 µm	P1 4.8 µm P2 4.8 µm M1 5.6 µm M2 4.2 µm	60	0.2	2.0	n/s	n/s	•	•		•	•	•	Inter-metall (Frei-bourg)
	MTC biMOS Bipolar JI + CMOS 3 µm	P1 7 µm M1 8 µm M2 9 µm	40	0.2	4.5	n/s	n/s	•	•		•	•	•	None
Mitsubishi Electronics America	M6001x (9) Si-gate CMOS 2 µm	M1 4 µm M2 7.5 µm	100	0.015	1.4	500–8100	54–190	•	•		•	•		None
	M6002x (6) Si-gate CMOS 1.3 µm	M1 4 µm M2 6 µm	175	0.01	0.9	200–2400	22–72	•	•		•	•		None
	M6003x (6) Si-gate CMOS 1.3 µm	M1 4 µm M2 6 µm	175	0.01	0.9	3200– 20,000	88–256	•	•		•	•		None
	M6004x (2) Si-gate CMOS 1.3 µm	M1 4 µm M2 6 µm	175	0.01	0.9	4100-6300	182-222 (for high I/O pin count)	•	•		•	•		None
Motorola	MCA I ECL (2) Bipolar OI (ECL) 3 µm	M1 8 µm M2 16 µm	>250	3.3	0.8	625–1192	46–60			10K, 10KH	•			None
	MCA II ECL (3) Bipolar OI (ECL) 2 µm	M1 6 µm M2 10 µm (M3 fixed)	>770	3.2	0.25	902–2760 1K RAM	54–120			10K, 10KH, 100K	•			None
	MCA I ALS (2) Bipolar OI (STTL) 3 µm	M1 8 µm M2 16 µm	>80	1.0	1.4	533–1280	57–75		•		•			None
	MCA II ALS (2) Bipolar OI (STTL) 2 µm	M1 6 µm M2 10 µm (M3 fixed)	>150	1.2	0.7	1800–2860 16×8 RAM	120		•		•			None
	HCA 62A00 (8) Si-gate CMOS 2 µm	M1 5.4 µm M2 6 µm	>85	1.0	1.5	648–8568	44–168	•	•		•	•	•	NCR
	MCA III ECL (2) Bipolar OI (ECL) 1.5 µm	M1 4 µm M2 6 µm (M3 fixed)	>1000	1.0-3.0, pro- gram- mable	0.1	1500–10,332	108– 256			10K, 10KH, 100K	•			None
	BiMOS (3) Si-gate CMOS and bipolar OI (STTL) 1.5 µm	M1 4 µm M2 5 µm	>150	0.022/ MHz	0.6	704–6144	44–228	•	•	10K, 10KH, 100K	•			None
	HDC series (5) Si-gate CMOS 1 µm	M1 3.6 µm M2 4 µm M3 4 µm	>150	0.006/ MHz	0.4	8208-104,832	100-267	•	•		•	•	•	None
National Semi-conductor	SCX 6200 (2) Si-gate CMOS 2 µm	M1 4.75 µm M2 6.25 µm	>100	2.75	0.9	600–8736	49-155	•	•		•	•	•	IMP
	10K VHSIC Si-gate CMOS 1.25 µm	M1 3 µm M2 4 µm	200	0.12	0.4	10,000	152	•	•				•	Westing-house
	SCX6Bxx (1) Si-gate CMOS 1.5 µm	M1 3.5 µm M2 4.75 µm	>150	3	0.65	400-15,000	28-200	•	•		•	•	•	None
	FGE (5) Bipolar OI (ECL) 1.5 µm	M1 5 µm M2 9 µm M3 13 µm	1000	4.5	0.23	100-6300	21-220		•	10K, 100K	•	•	•	Honeywell
	FGA (3) Bipolar OI (ECL) 1.5 µm	M1 5 µm M2 5 µm M3 9 µm	1800	3.7	0.12	1300-15,000	72-300		•	•	•	•	•	None

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Directory of Gate Arrays (continued)

Company	Product Technology Line width	Programmable layers	Typical parameters			Components		Interface levels[4]			Temp. ranges[5]			Second sources
			MHz[1]	mW[2]	ns[3]	Gates	I/Os	C	T	ECL	C	I	M	
NCM	3000 (3) Me-gate CMOS 7 μm	M1 12.5 μm	5	n/s	18	235–500	38–48	•	•		•	•	•	None
	7300, 7500 Si-gate CMOS 3, 5 μm	P1 10 μm M1 10 μm	18, 12	n/s	5, 8	780 gates 8 active	62	•	•		•	•	•	None
	5000 Bipolar JI 5 μm	M1 12.5 μm	40	n/s	3	78–132 active 227–296 passive	18–24		•	•	•	•	•	Exar, Ferranti Inter-design
NCR Micro-Electronics	62A00 (8) Si-gate CMOS 2 μm	M1 M2	85	1.6	1.5	600–8500	44–168	•	•		•	•	•	Motorola
NEC Electronics	CMOS-5/5A (13) Si-gate CMOS 1.2 μm	M1 3.6 μm M2 4.6 μm M3 7.2 μm	250	3.0	0.52	2000–45,000	88–334	•	•		•	•		None
	CMOS-4/4A/4R (16) Si-gate CMOS 1.5 μm	M1 5.4 μm M2 7 μm	140	2.1	0.9	320–19,551	54–266	•	•		•	•		None
	CMOS-4L (6) Si-gate CMOS 1.5 μm	M1 5.4 μm M2 7 μm	25	0.08	7	860-5600	62-138	•			•			None
	BiCMOS-5 (5) Si-gate CMOS 1.3 μm Bipolar 1.2 μm	M1 M2	300	5.4	0.45	5000–20,000	148-280	•	•	10KH, 100K	•	•		None
	BiCMOS-4/4A (6) Si-gate CMOS 1.5 μm Bipolar 2 μm	M1 5.4 μm M2 7 μm	200	3.6	0.67	600–10,000	64–228	•	•		•	•		None
	ECL-4A (5) Bipolar (ECL) 1.2 μm	M1 M2 M3 (power)	1200	4.85	0.15	2400-35,000	108-236		•	10KH, 100K	•			None
	ECL-4 (2) Bipolar (ECL) 1.2 μm	M1 M2 M3 (power)	1700	6.75	0.14	600-4400	56–108			10KH, 100K	•			None
	ECL-3A/3B (5) Bipolar (ECL) 1.4 μm	M1 M2 M3 (power)	450	4.35	0.5	2400-9600	120-172		•	10KH, 100K	•			None
	ECL-3 (3) Bipolar (ECL) 3 μm	M1 8 μm M2 M3 (power)	300	1.1	0.7	1200-3000	48-180			10K	•			None
	ECL-2 (3) Bipolar (ECL) 3 μm	M1 8 μm M2 M3 (power)	450-750	4.5	0.05	300-2000	28-108			100K	•			None
Oki Semi-conductor	MSM7H000 CMOS 2 μm drawn	M1 8 μm M2 11 μm	40	6	1.8	301-10,008	32-188 4-18 mA 48 mA max	•	•		•	•		None
	MSM7nV000 CMOS 1.5 μm drawn	M1 5 μm M2 7.5 μm	50	5	1	700-10,008	74-188 4-8 mA 24 mA max	•	•		•	•		None
	MSM10V000 CMOS 1.5 μm drawn	M1 5 μm M2 7.5 μm	65	4.5	0.8	5500-100,500	74-188 4-12 mA 24 mA max	•	•		•	•		None
	MSM7U000 CMOS 1.2 μm drawn	M1 4.5 μm M2 6 μm	80	4	0.5	1632-30,384 cells (6 transistors)	60-252 +8 power 4-12 mA 24 mA max	•	•		•	•		None
Panasonic	MN 51000 (8) Si-gate CMOS 2.5 μm	M1 3.6 μm M2 5 μm	120	0.025	1.9	312–4000	46–164	•	•		•	•		None
	MN 52000 (5) Si-gate CMOS 2 μm	M1 2.7 μm M2 3.8 μm	160	0.02	1.4	2014–10,000	94–234	•	•		•	•		None
	MN 53000 (13) Si-gate CMOS 1.5 μm	M1 2.4 μm M2 2.8 μm	200	0.015	1	315–20,064	42-256	•	•		•	•		None

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Company	Product Technology Line width	Programmable layers	Typical parameters			Components		Interface levels[4]			Temp. ranges[5]			Second sources
			MHz[1]	mW[2]	ns[3]	Gates	I/Os	C	T	ECL	C	I	M	
Plessey Semiconductor	CLA 5000 (8) Si-gate CMOS 2 μm	M1 6 μm M2 6 μm	100	0.35	1.2	640–10,044	44–176	•	•		•	•	•	Matra-Harris
	ELA60000 (4) Bipolar (ECL) 1.5 μm	M1 5 μm M2 5 μm M3 7 μm (power only)	2000	7	0.3	600–4500	48–120	•	•	10K, 100K	•	•	•	None
	MVX (5) Bipolar JI (analog) 10 μm	M1 18 μm	n/s	n/s	n/s	62–213 active	20–44	•	•	•	•	•	•	Custom Arrays
	MFX (5) Bipolar JI 4 μm	M1 18 μm	n/s	n/s	n/s	100–170 gates 160–650 active	16–48	•	•	•	•	•	•	None
	MMX (9) Bipolar JI 10 μm	M1 18 μm	n/s	n/s	n/s	36–434 active	14–48	•	•	•	•	•	•	Custom Arrays
	ULA Digilin G (7) Bipolar CDI 4 μm	M1 8 μm	0.66	0.002	230	30–578 gates 124–436 active	10–36	•	•		•	•	•	None
	ULA Digilin P Bipolar CDI (10) 3 μm	M1 8 μm	4.8	0.001	40	128–1152 gates 444–1088 active	16–44	•	•		•	•	•	None
	ULA R (28) Bipolar CDI 2.5 μm	M1 8 μm	65	350	2.2	130–2000	20–72	•	•		•	•	•	None
	ULA DS (30) Bipolar CDI 1.5 μm	M1 6 μm	250	0.33	1.0	630–10,000	32–138	•	•		•	•	•	None
	MLX (2) Me-gate CMOS 7 μm	n/s	n/s	n/s	n/s	64 gates 312–842 active	30–42	•	•		•	•	•	None
	MC (7) Me-gate CMOS 6 μm	M1 10 μm	18	0.125	15	140–800	29–58	•	•		•	•	•	MCE, Master Logic, Hytek
	MH (8) Si-gate CMOS 4 μm	M1 8 μm	40	0.1	n/s	70–1600	18–84	•	•		•	•	•	None
Polycore Electronics	Maxi chip (8) Bipolar JI (analog) 5 μm	M1 15 μm	n/s	n/s	n/s	17–165 active 24–280 passive	10–40		•	all	•			Gennum
Raytheon Semiconductor	CGA 300 Bipolar JI (STTL) 5 μm	M1 15 μm M2 15 μm	25	5	6	300	48		•		•	•	•	None
	CGA 800-2500 Bipolar JI (ISL) 3 μm	M1 10 μm M2 15 μm	100	0.4	2.2	800–2400	48–84		•		•	•	•	None
	CGA 3,500, 5,000 Bipolar OI (ISL) 2 μm	M1 6 μm M2 9 μm	150	0.16	1.2	3500, 5000	120, 150		•		•	•	•	None
	CGA70E18 Bipolar (ECL) 2 μm	M1 4 μm M2 4 μm	1000	300	0.3	12,800	176	•	•	10KH, 100K	•	•	•	None
	RL 7000 series Si-gate CMOS 2 μm	M1 7 μm M2 9 μm	40	0.72	1.4	880–10,013	68–232	•	•		•	•	•	LSI Logic
	CGA40E12 Bipolar (ECL) 2 μm	M1 4 μm M2 4 μm	1000	300	.3	7752	120		•	10KH, 000053	•	•	•	None
	CGA1ME12 Bipolar (ECL) 2 μm	M1 4 μm M2 4 μm	1000	300	.3	4584 1280 bits of RAM	120		•	10KH, 100K	•	•	•	None
	RL1050–H1200 NCMOS 1.25 μm	M1 4 μm M2 6 μm	250	8 mW/ MHz/ gate	0.95	5670–20, 440–160	90	•	•		•	•	•	None
Siliconix	ISO5 (9) Si-gate CMOS 4.8 μm	M1 10 μm	10	0.09	2.8	180–2400	30–90	•	•		•	•	•	Universal

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			MHz[1]	mW[2]	ns[3]	Gates	I/Os	C	T	ECL	C	I	M	
Silicon Systems	SSI 6600 (6) Si-gate CMOS and bipolar JI (CML) 3 μm	P1 6 μm M1 8 μm	25	n/s	5	0–545 179–294 active 224–712 passive	28–62 analog	•	•		•	•	•	None
	BK MSA6900 Bipolar JI (STTL) 3 μm	M1 8.8 μm M2 12 μm	>100	n/s	1.5	n/s	n/s	•	•	•	•	•	•	None
	MSA6700 (4) Si-gate CMOS 3.8 μm	P1 M1	20	0.01/ MHz	<5	80–600 gates 190–601 active 600–1200 passive	32–52 8–12 analog	•	•		•	•		None
	SSI 6900 (4) Bipolar JI (STTL, ECL, CMI) 2.5 μm	M1 8 μm M2 14 μm	>100	n/s	n/s	20–80 gates 144–168 active 24–56 passive	16–32 8 analog	•	•	•	•	•		Ferranti Inter-design
Silicon West	SWI 1000 (4) Si-gate CMOS 2 μm	M1 M2	100	0.6	1.2	360–10,000	40–161	•	•		•	•		None
S-MOS Systems	SLA 6000 (10) Si-gate CMOS 2 μm	M1 7 μm M2 9.8 μm	70	0.8	1.7	513–6206	60–154	•	•		•			IMI
	SLA 7000 (5) Si-gate CMOS 1.5 μm	M1 5.2 μm M2 7.4 μm	100	1.2	0.9	2232–16,250	90–188	•	•		•			IMI
	SLA 8000 (6) Si-gate CMOS 1.2 μm	M1 3.5 μm M2 5 μm	120	1.45	0.7	5904–38,550	82–218	•	•		•			None
Tektronix	QuickChip 4 Bipolar JI (ECL, CML) 4 μm	M1 7 μm M2 7 μm	500	1	0.4	300	n/s			all	•	•		None
Texas Instruments	TGC100 series Si-gate CMOS 1 μm	M1 4.8 μm M2 5.4 μm	150	0.018/ MHz	0.5	3200–18620	84–216	•	•		•	•	•	None
TLSI	TA CMOS (6) Si-gate CMOS 5 μm	M1 10 μm	10	n/s	6	300–1260	37–75	•	•		•	•	•	
	TA CMOSII (5) Si-gate CMOS 3 μm	M1 7 μm	36	n/s	3	540–2500	37–81	•	•		•	•	•	Gould
	TA CMOSIID (4) Si-gate CMOS 3 μm	M1 7 μm M2 8 μm	40	n/s	2.5	1000–4012	61–117	•	•		•	•	•	Gould
Toshiba America	TC110G Si-gate CMOS 1.5 μm	M1 5.6 μm M2 6 μm	150	0.14	0.6	3498–129,000	68–368	•	•		•	•		LSI Logic
	TC120G Si-gate CMOS 1 μm	M1 5.6 μm M2 6 μm	200	Contact company	0.4	37,932-129,042	19–368	•	•			n/s		None
TriQuint Semi-conductor	TQ3000 GaAs E/D-MESFET 1 μm	M1 2 μm M2 3 μm	1000	2.5	0.18	2000-4200	84	•	•	all	•	•	•	None
Unicorn Micro-electronics	UM1200 (4) Si-gate CMOS 3 μm	M1 P1	20	0.4	3.0	200–910 gates 36–68 passive	28–58	•	•		•	•		United Micro-elec-tronics
	UM1300 (4) Si-gate CMOS 2 μm	P1 M1 M2	30	0.9	2	1320–3060 gates 58–102 passive	54–92	•	•		•	•		United Micro-elec-tronics
United Technologies Micro-electronics Center	UTB (5) Si-gate CMOS 3 μm	M1 7.5 μm M2 7.5 μm	115	2.25	2.2	1000–7600	40–144	•	•				•	None
	UTD (4) Si-gate CMOS 1.5 μm	M1 6 μm M2 6 μm	250	7.5	0.63	3400–11,000	116–212	•	•				•	None

1. Flip-flop toggle rate. 2. Gate power at frequency. 3. 2-in NAND delay, FO = 2, 1 mm wire. 4. C = CMOS, T = TTL. 5. C = commercial, I = industrial, M = military.

Company	Product Technology Line width	Programmable Layers	Typical Parameters			Components		Interface levels[4]			Temp. ranges[5]			Second Sources
			MHz[1]	mW[2]	ns[3]	Gates	I/Os	C	T	ECL	C	I	M	
Vitesse Semiconductor	VSC4500 (1) GaAs E/D-MESFET (DCFL) 1.2 μm	M1 4 μm M2 8 μm	600 single-ended, 850 differential	6.2	0.240	4000	120		•	10K, 100K	•	•	•	None
	VSC1500 (1) Mixed D-and E/D-MESFET (DCFL; source- coupled FET logic) 1.2 μm	M1 4 μm M2 8 μm	2000	DCFL 0.42, SCFL 0.23[6]	DCFL 0.545, SCFL 0.235[6]	1500	35			10K, 100K	•	•	•	None
VLSI Technology	VGT200 (13) Si-gate CMOS 1.5 μm	M1 4 μm M2 5.6 μm	250	15	0.560	960–54,000	48–348	•	•		•	•	•	Philips, GE
	VGT-100 (13) Si-gate CMOS 1.5 μm	M1 4 μm M2 5.6 μm	175	3.5	0.8	1600–66,500	56–348	•	•		•	•	•	GE
	VGT10 (6) Si-gate CMOS 2 μm	M1 6 μm M2 6 μm	120	2.4	1.2	1600–10,648	56–140	•	•		•	•	•	GE
VTC	VJ800 (4) Bipolar JI 3 μm	M1 8 μm M2 12 μm	50	2.25	2	50 28–40	28–68 active		•	10K, CML	•	•	•	None
	Si-gate CMOS 1 μm	M1 4 μm M2 6 μm	200	n/s	0.7	6000	n/s	•	•		•	•	•	Motorola
	VG6000 Si-gate CMOS 1.6 μm	M1 M2	200	n/s	1	6000	172	•	•		•	•	•	National
	VJ900 (3) Bipolar OI 2 μm	M1 8 μm M2 12 μm	250	2.25	0.42	30–572	16–68		•	10K	•	•	•	None
Xerox Microelectronics Center	SCX 6200 (2) Si-gate CMOS 2 μm	M1 4.75 μm M2 6.25 μm	>100	2.75	0.9	600–8736	49-155	•	•		•	•	•	IMP
	10K VHSIC Si-gate CMOS 1.25 μm	M1 3 μm M2 4 μm	200	0.12	0.4	10,000	152	•	•				•	Westinghouse
	SCX6Bxx (1) Si-gate CMOS 1.5 μm	M1 3.5 μm M2 4.75 μm	>150	3	0.65	400-15,000	28-200	•	•		•	•	•	None
	FGE (5) Bipolar OI (ECL) 1.5 μm	M1 5 μm M2 9 μm M3 13 μm	1000	4.5	0.23	100-6300	21-220		•	10K, 100K	•	•	•	Honeywell
	FGA (3) Bipolar OI (ECL) 1.5 μm	M1 5 μm M2 5 μm M3 9 μm	1800	3.7	0.12	1300-15,000	72-300		•	•	•	•	•	None
Xilinx	XC2000/XC3000 (7) Si-gate CMOS 1.2 μm	n/a	70	1.0	2	1200-9000	58-144	•	•		•	•	•	AMD

1. Flip-flop toggle rate. 2. Gate power at frequency. 3. 2-in NAND delay, FO = 2, 1 mm wire. 4. C = CMOS, T = TTL. 5. C = commercial, I = industrial, M = military. 6. For a 2-in NOR gate.

Directory of Cell Libraries

Company	Product Technology Line width	Wiring layers	Typical parameters			Cells		Interface levels[4]			Temp. ranges[5]			Second sources
			MHz[1]	mW[2]	ns[3]	Simple	Complex	C	T	ECL	C	I	M	
ABB HAFO	MEG 6 Me-gate CMOS 5 μm	M1 10 μm	10	0.5	10	55 gates 10 MSI 15 analog 20 I/O	RAM, ROM, PLA	•	•		•	•	•	GE
	SOS3 Si-gate SOS 4 μm	P1 8 μm M1 8 μm	35	0.1	2.5	55 gates 10 MSI 10 I/O	RAM, ROM, PLA	•	•		•	•	•	GE

1. Flip-flop toggle rate. 2. Gate power at frequency. 3. 2-in NAND delay, FO = 2, 1-mm wire. 4. C = CMOS, T = TTL. 5. C = commercial, I = industrial, M = military.

Company	Product Technology Line width	Wiring layers	Typical parameters			Cells		Interface levels[4]			Temp. ranges[5]			Second sources
			MHz[1]	mW[2]	ns[3]	Simple	Complex	C	T	ECL	C	I	M	
ABB HAFO	SOS4 Si-gate SOS 2 μm	P1 4.5 μm M1 6 μm M2 9 μm	150	n/s	1.2	55 gates 10 MSI 10 I/O	RAM, ROM, PLA	•	•		•	•	•	None
	SIGI Si-gate CMOS 3 μm	P1 6 μm M1 6 μm	35	n/s	3	55 gates 10 MSI 10 analog 10 I/O	RAM, ROM, PLA, multiplier	•	•		•	•	•	GE
	SIG2 Si-gate CMOS 2 μm	P1 4.5 μm M1 6 μm M2 7 μm	110	n/s	2	55 gates 10 MSI 10 analog 10 I/O	RAM, ROM, PLA	•	•		•	•	•	GE
Adams Russell	GaAs D-MESFET 1 and 0.5 μm	n/s	n/s	n/s	n/s	>50 analog	Interpolation of cells in the library		n/s		•	•	•	None
AT&T Technologies	1.25 μm library Si-gate CMOS 1 μm	P1 2.5 μm M1 3.5 μm M2 4.5 μm	170	1.9	0.8	165 gates >70 MSI 14 analog 55 I/O	RAM, ROM, PLA, cell compiler, function compiler	•	•		•	•	•	None
	GaAs high-voltage E/D-FET 1 μm	M1 2 μm M2 2 μm	n/s	0.5	0.1	30	10		n/s		•	•	•	None
Barvon BiCMOS Technology	Si-gate CMOS and biCMOS 2.5 μm	M1 M2	75	n/s	3	>350 MSI 80 analog 14 I/O	RAM, ROM; 10-bit DAC and ADC; AGC, ALU, filters	•	•		•	•	•	None
	Si-gate CMOS 2 μm	M1 M2	150	n/s	1.2	as above	as above	•	•		•	•	•	None
	Si-gate CMOS 1.5 μm	M1 M2	200	n/s	0.9	as above	as above	•	•		•	•	•	None
	BC1000 BiCMOS 2 μm	M1 M2	100	n/s	1.5	150 MSI 30 analog 15 I/O	RAM, ROM; ADC, DAC, bandgap reference, differentiator, peak detector, filters	•	•		•	•	•	None
	BC4000 Si-gate CMOS 2 μm	M1 M2	150	n/s	1.3	150 MSI 30 analog 15 I/O	as above	•	•		•	•	•	None
California Micro Devices	Si-gate CMOS 1.5 μm	M1 4.5 μm M2 5 μm	150	3	0.7	70 gates 40 MSI 30 I/O	RAM, ROM, PLA	•	•		•	•	•	None
Commodore Semiconductor	4500 series Si-gate CMOS 2 μm	P1 4 μm M1 4.5 μm M2 5.5 μm	80	0.5	1	50 gates 15 MSI 15 I/O	RAM, ROM, PLA; 65C02	•	•		•			None
Control Data	VL 5000 Si-gate CMOS 1.2 μm	M1 3.3 μm M2 3.6 μm	166	0.9	0.58	86 MSI	Register file, 2901, stackable register and multiplexer cells	•	•		•	•	•	VTC
Custom Arrays	MM macrocells Bipolar JI 6 μm	M1	n/s	n/s	n/s	30 analog	Op amps, voltage regulators, oscillators, band-gap references, comparators	•	•	•	•	•	•	Ferranti Inter-design
	MV macrocells Bipolar JI 6 μm	M1	n/s	n/s	n/s	30 analog	Op amps, voltage regulators, oscillators, bandgap references, comparators		•	•	•	•	•	Ferranti Inter-design
Custom Silicon	VS 3000 Si-gate CMOS 3 μm	P1 2.7 μm M1 2.2 μm M2 4.95	50	0.25	1.8	50 gates 20 MSI 20 analog 30 I/O	RAM, ROM, ALU, multiplexers, 275 MicroBlocks, 29xx bit-slice processors, 65CX02, multiport RAMS	•	•		•	•	•	NCR, Motorola
	VS 2000 Si-gate CMOS 2 μm	M1 3.75 μm M2 4.25 μm	85	0.28	1.1	58 gates 103 MSI 6 analog 34 I/O	RAM, ROM, PLA, EEPROM; SRAM, D-RAM, 275 MicroBlocks, 29xx bit-slice processors, 65CX02, SCSI, and CRT controller, 68C05, multiports RAMS	•	•		•	•	•	NCR, Motorola
	VS-1500 Si-gate CMOS 1.5 μm	M1 3 μm M2	110	0.14	0.5	57 gates 105 MSI 20 analog 34 I/O	RAM, ROM, ALU, MUX, 275 MicroBlocks, 29xx bit-slice processors, 65CX02, SCSI, and CRT controllers, 68C05, multiport RAMS	•	•		•	•	•	NCR
Data Linear	DL-104/187/357/650 Bipolar DI (analog) 5 μm	M1 15 μm	0.5-1 GHz[6]	n/s	2	13 analog	Any arrangement of simple cells		•	10K, 100K	•	•	•	None
	SP1204 Bipolar DI (20, 35 V) (analog and interface cells	M1 7 μm M2 15 μm	1 GHz[6]	n/a	n/a	Many simple analog and logic interfacing cells	10 basic macrocells	•	•	•	•	•	•	None

1. Flip-flop toggle rate. 2. Gate power at frequency. 3. 2-in NAND delay, FO = 2, 1-mm wire. 4. C = CMOS, T = TTL 5. C = commercial, I = industrial, M = military 6. f_T.

Company	Product Technology Line width	Wiring layers	Typical parameters			Cells		Interface levels[4]			Temp. ranges[5]			Second sources
			MHz[1]	mW[2]	ns[3]	Simple	Complex	C	T	ECL	C	I	M	
Design Devices	Si-gate CMOS 2 μm	M1 6 μm M2 9 μm	50	1.5	1.75	54 MSI 40 I/O	RAM, ROM, 2901 family	•	•		•	•	•	None
	Si-gate CMOS 1.5 μm	M1 5.6 μm M2 6 μm	150	1.8	1	115 gates 45 MSI 20 I/O	RAM, ROM, PLA, 74xx logic, mulipliers	•	•		•	•	•	None
Electronic Technology	ETC Si-gate CMOS 2 and 3 μm	P1 or M1 7.5 μm	50	0.65	2.15	52 gates 7 MSI 14 analog 15 I/O	RAM, ROM; 65CX02	•	•		•	•	•	Gould, Motor,ola, NCR
	STDC Si-gate CMOS 3 μm	M1 M2	40	0.35	1.7	25 gates 2 MSI 6 analog 16 I/O	RAM, ROM, CPU/timer; 65Cx02, 6512×8 RAM, 62H×8 ROM	•	•		•			Motor,ola, NCR, Gould
	STDC Si-gate CMOS 2 μm	M1 M2	75	0.35	1.1	46 gates 14 MSI 26 I/O	RAM, ROM, 65HC05	•	•		•	•	•	NCR, Motor,ola, Gould
Exar	P3000 Si-gate CMOS 3 μm	M1 6 μm M2 7 μm	35	0.19	2–3	50 gates 15 analog 10 I/O	Analog cells can be parameterized based on operating conditions	•	•		•	•	•	Rohm
	N2000 Si-gate CMOS 2 μm	M1 7 μm M2 8 μm	100	0.19	1	50 gates 75 MSI 25 analog 32 I/O	RAM, ROM, EEPROM; analog and switched- capacitor filters	•	•		•	•	•	Rohm
Fujitsu Micro-electronics	AV-OEBB Si-gate CMOS 1.8 μm	P1 6 μm M1 7 μm M2 9 μm	100	n/s	1.2	140 digital	RAM, ROM, PLA, multipliers, ALU	•	•		•	•	•	None
	AU-AEBB Si-gate CMOS 1.2 μm	P1 3 μm M1 4.5 μm M2 6 μm M3 9 μm	120	n/s	0.85	100 gates 28 MSI 40 I/O	RAM, ROM, PLA; multipliers, ALU; 8200-type logic	•	•		•	•	•	None
GE Micro-electronics Center	GECELL Si-gate CMOS (CMOS/SOS available) 1.2 μm	M1 3 μm M2 4 μm	40	0.32	0.7	100 gates 50 MSI 70 I/O	None	•	•				•	None
Genesis Microchip	M² CMOS Si-gate CMOS 2 μm	M1 M2	85	n/s	0.9	100 gates 104 MSI 12 analog 78 I/O	RAM, ROM, EEPROM, COP888, HPC 16- bit controller, SM8250, 2901	•	•		•	•	•	National
GE Solid State	SC2500 Si-gate CMOS 3 μm	M1 9 μm M2 11 μm	15	0.3	2.5	63 MSI 8 I/O	RAM, ROM, PLA, compilable cells as hard macros	•	•		•	•	•	None
	SC2000 Si-gate CMOS 3 μm	P1 11 μm M1 9 μm	10	0.2	2.5	63 MSI 8 I/O	Compilable cells as hard macros	•	•		•	•	•	Silicon Systems
	SC2800 Si-gate SOS 3 μm	P1 6 μm M1 10 μm	15	0.2	1.5	45 MSI 11 I/O	Compilable cells as hard macros	•	•		•	•	•	None
	SC3000 Si-gate CMOS 2 μm	M1 6 μm M2 8 μm	20	0.3	1.8	63 MSI 8 I/O	RAM, ROM, PLA, compilable cells as hard macros	•	•		•	•	•	VLSI Tech-nology
	SC4000 (Advancell) Si-gate CMOS 1.5 μm	M1 3.5 μm M2 4.8 μm	100	0.5	0.8	167 gates 10 MSI 5 analog 84 I/O	RAM, ROM, PLA, 2900 family bit slice	•	•		•	•	•	Toshiba, Siemens
	SC3500 Si-gate CMOS 1.6 μm	M1 4.8 μm M2 6.4 μm	26	0.3	1.5	63 MSI 13 I/O	RAM, ROM, PLA, compilable cells as hard macros	•	•		•	•	•	VLSI
	SC2500E Si-gate CMOS (12 V) 3 μm	M1 9 μm M2 11 μm	15	0.3	2.5	63 MSI 13 I/O	RAM, ROM, PLA, compilable cells as hard macros	•	•		•	•	•	None
GigaBit Logic	SC5000 GaAs D-MESFET (CDFL) 0.8 μm	M1 4 μm M2 4 μm	2300	2.4	0.18	15 gates 13 MSI 7 I/O	None	•	•	10K, 100K	•	•	•	Tachonics
	SC10000 GaAs E/D-MESFET (CDFL/SCFL) 0.8 μm	M1 4 μm M2 4 μm M3 4 μm	3000	1.5	0.15	12 gates 13 MSI 6 I/O	RAM, ROM	•	•	10K, 100K	•	•	•	None
Gould Semi-conductor	Si-gate CMOS 2 μm	M1 5 μm M2 7 μm	100	2.4	0.6	516 gates 200 MSI 24 I/O	RAM, ROM, PLA; multipliers, 2901 family; barrel, pipeline shifters			n/s	•	•	•	Contact company
	Si-gate CMOS 3 μm	M1 M2	50	n/s	2.5	212 gates 200 MSI 24 I/O	ADC, DAC, filters, op amps, analog, megacells			n/s	•	•	•	Contact company

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Directory of Cell Libraries (continued)

Company	Product Technology Line width	Wiring layers	Typical parameters			Cells		Interface levels[4]			Temp. ranges[5]			Second sources
			MHz[1]	mW[2]	ns[3]	Simple	Complex	C	T	ECL	C	I	M	
Holt Integrated Circuits	Si-gate CMOS 3 μm	P1 7 μm M1 8 μm	15	0.2	6	40 gates 10 MSI 20 analog 25 I/O	RAM, ROM; ADC, DAC, display drivers, controllers	•	•		•	•	•	None
	Si-gate CMOS 3 μm	P1 7 μm P2 8 μm M1 8 μm	15	0.2	6	40 gates 10 MSI 25 analog 25 I/O	RAM, ROM, A/D, D/A display drivers, controllers	•	•		•	•	•	None
Hughes Aircraft	Si-gate CMOS 3 μm	P1 10 μm M1 9 μm	30	0.45	2	100 gates 15 MSI 25 analog 10 I/O	n/s	•	•		•	•	•	None
	U series Si-gate CMOS 2 μm	P1 2 μm P2 2 μm M1 5 μm M2 5 μm	30–50	0.8	1.5	50 gates 20 MSI 100 I/O	RAM, ROM, PLA, EEPROM, 2903, 2910	•	•		•	•	•	None
Integrated Circuit Systems	Si-gate CMOS 3 μm	P1 6 μm M1 9 μm	80	0.02	1.2	65 gates 35 MSI 20 analog 18 I/O	RAM, ROM, PLA, PLL, VCO	•	•		•	•	•	NCR, VTI, Motorola
	Si-gate CMOS 2 μm	M1 M2	80	.014	1.2	36 gates 18 MSI 18 analog 12 I/O	RAM, ROM, PLA, 65C02	•	•		•	•	•	NCR, VLSI Technology, Motorola, NSC
	VTI Si-gate CMOS 2 μm	M1 M2	80	.015	1.2	44 gates 16 MSI 12 I/O	RAM, ROM, PLA, Intel peripheral chips	•	•		•	•	•	None
Intel	Si-gate CMOS 1.5 μm	M1 3.84 μm M2 5.12 μm	65	0.02	0.7	41 gates 47 MSI 24 I/O	RAM, ROM, PLA, 80C51, 8086 peripherals, counters, adders, analog	•	•		•			None
International Microcircuits	G4000 Me-gate CMOS 8 μm	M1	2	0.01	70	n/s	n/s	•	•		•	•	•	S-MOS
	G70000 Si-gate CMOS 3.5 μm	P1 M1	42	0.42	3.3	24 gates 9 MSI 8 I/O	n/s	•	•		•	•	•	S-MOS
	IMI6000 Si-gate CMOS 2 μm	P1 M1 M2	60	0.6	1.4	101 gates 50 MSI 18 I/O	n/s	•	•		•	•	•	S-MOS
	IMI 7000 Si-gate CMOS 1.5 μm	P1 M1 M2	100	n/s	0.75	1632-8000	70-170	•	•		•	•	•	S-MOS
International Microelectronic Products	ACL3/DCL3 Si-gate CMOS 3 μm	P1 8 μm M1 8 μm	50	0.15	3	45 gates 35 analog 21 I/O	RAM, ROM	•	•		•			Contact company
	ACL2/DCL2 Si-gate CMOS 2 μm	M1 6 μm M2 8 μm	80	0.3	1	45 gates 10 analog 21 I/O	RAM, ROM	•	•		•			Contact company
	DCL1.2 Si-gate CMOS 1.2 μm	n/s	n/s	n/s	n/s	45 gates 21 I/O	n/s			n/s			n/s	n/s
LSI Logic	LST20/LSC20 Si-gate CMOS 2 μm	P1 M1 M2	n/s	0.02/MHz	1.4	>400 gates >300 MSI >100 I/O	Mutipliers, barrel shifters, 6845, 8251, 2901 family, RAM, ROM, PLA (LSC20)	•	•		•	•	•	Contact company
	LCB 15 Si-gate CMOS 1.5 μm	P1 M1 M2	n/s	0.01/MHz	0.5	>400 gates >300 MSI >200 I/O	RAM, ROM, PLA, EPROM, multiport RAM, FIFO, LIFO, CAM; 29xx, 82xx, 6845	•	•	10K, 100K	•	•	•	Contact company
Marconi Electronic Devices	CELLMOS Si-gate CMOS 5 μm	P1 10 μm M1 10 μm	20	0.1	8	55 gates 6 MSI 9 analog 6 I/O	RAM, ROM, "stretchable" buffer	•	•		•	•	•	None
	CELLMOS Si-gate CMOS 3 μm	P1 6 μm M1 6 μm	40	0.12	3	55 gates 6 MSI 9 analog 6 I/O	RAM, ROM, "stretchable" buffer	•	•		•	•	•	None
	CELLSOS Si-gate SOS 5 μm	P1 10 μm M1 10 μm	25	0.08	5	56 gates 11 I/O	RAM, ROM, "stretchable" buffer	•	•		•	•	•	None
	MacroSOS1 Si-gate CMOS/SOS 2.5 μm	M1 6 μm M2 6 μm	70	0.003	1.2	38 gates 22 MSI 21 I/O	RAM, ROM, counters, adders, shift registers	•	•		•	•	•	n/s
	MacroMOS1 Si-gate CMOS 3 μm	P1 8 μm P2 8 μm M1 8 μm M2 8 μm	60	0.6	1.6	42 gates 38 MSI 27 analog 26 I/O	RAM, ROM, counters, adders, shift registers, ADC, DAC	•	•		•	•	•	n/s

1. Flip-flop toggle rate. 2. Gate power at frequency. 3. 2-in NAND delay, FO = 2, 1-mm wire. 4. C = CMOS, T = TTL. 5. C = commercial, I = industrial, M = military.

Company	Product Technology Line width	Wiring layers	Typical parameters			Cells		Interface levels[4]			Temp. ranges[5]			Second sources
			MHz[1]	mW[2]	ns[3]	Simple	Complex	C	T	ECL	C	I	M	
Matra Design Semiconductor	GATELIB/MA Si-gate CMOS 2.5 μm	P1 6.5 μm M1 10 μm	25	0.02/ MHz	2	86 gates 25 MSI 1 analog 40 I/O	None	•	•		•	•	•	None
	GATELIB/MB Si-gate CMOS 1.5 μm	P1 4 μm M1 6 μm M2 9 μm	45	0.02/ MHz	1	70 gates 20 MSI 3 analog 33 I/O	RAM, multipliers, ALU, UART, 2901 family	•	•		•	•	•	Plessey
MCE Semiconductors	MCE Unicell Bipolar JI 5 μm	M1	50	20	7	10 I/O	Op amps, comparators, references	•	•	•	•	•	•	None
	MCE MGA Me-gate CMOS 5 μm	M1 10 μm	5	3	10	21 gates 38 MSI 11 analog 43 I/O	Bias generator, comparator, op amp	•	•		•	•	•	None
	MCE SGA Si-gate CMOS 4 μm	P1 8 μm M1 8 μm	10	1	5	15 gates 13 MSI 11 analog 21 I/O	Comparator, op amp bias generator	•						None
Micro LSI	μCell library Si-gate CMOS 2 and 3 μm	P1 M1	90	1.1	3.5	70 gates 10 MSI 10 I/O	RAM, ROM	•	•		•	•		None
	ULSI 20 Si-gate CMOS 2 μm	M1 6 μm M2 8 μm	90	3.5	1.1	70 gates 25 MSI 16 I/O	RAM, ROM	•	•		•	•		None
Micro-Rel	D5 library Si-gate CMOS 5 μm	P1 10 μm M1 10 μm	1	0.12	1.0	108 gates 28 analog 17 I/O	RAM, ROM	•	•		•	•	•	None
	D3 library Si-gate CMOS 3 μm	P1 6 μm M1 7 μm M2 10 μm	25	1	5	n/s	RAM, ROM	•	•		•	•	•	None
	Si-gate CMOS 3.5 μm	P1 3.5 μm M1 3.5 μm	n/s	n/s	n/s	85 gates 25 analog	Op amp, comparators, reference, bias generator, oscillator	•	•		•	•	•	None
	Bipolar JI, OI, DI (TTL) 8 μm	P1 8 μm M1 8 μm	n/s	n/s	n/s	10 gates 20 analog	—		•		•	•	•	None
	BiMOS 3 μm	P1 3 μm	25	1	5	85 gates 25 analog	Op amps, comparators, reference bias generator, OSC	•	•		•	•	•	None
Mietec	CMOS 2.4 μm Si-gate CMOS 2.4 μm	P1 4.8 μm P2 4.8 μm M1 5.6 μm M2 7.2 μm	60	0.2	2	34 gates 32 MSI 42 analog 48 I/O	RAM, ROM, PLA; switched- capacitor filter compiler	•	•		•	•	•	None
	Bipolar JI and Si-gate CMOS 3 μm	P1 7 μm M1 8 μm M2 9 μm	40	0.2	4.5	20 gates 10 MSI 20 analog 2 I/O	RAM, ROM, PLA; switched- capacitor filter compiler	•	•		•	•	•	None
Mitsubishi Electronics America	Si-gate CMOS 2 μm	n/s	100	0.015	0.9	85 cells 175 functions 9 I/O	Configurable RAM, ROM	•	•		•	•		None
National Semiconductor	Micro CMOS Si-gate CMOS 2 μm	M1 4.75 μm M2 6.25 μm	110	2.75	1	90 gates 98 MSI 10 analog 170 I/O	RAM, ROM, PLA, EEPROM, UARTs, 2901, 2911; 16-bit controller; comparators, opamps, voltage reference, analog switch, ADC configurable I/O drivers	•	•		•	•	•	IMP
NCM	20 series Me-gate CMOS 7 μm	M1 13 μm	5	n/s	16	20 gates 18 MSI 8 analog 6 I/O	PLA, ROM	•	•		•	•	•	None
	9000 series Si-gate CMOS 3 μm	P1 10 μm M1 12 μm	18	n/s	3	40 gates 7 MSI 3 analog 9 I/O	ROM, PLA	•	•		•	•	•	None
NCR Microelectronics	VS2000 Si-gate CMOS 2 μm	M1 M2	85	0.28	1.1	58 gates 38 MSI >20 analog 34 I/O	RAM, ROM, dual-port RAM, PLASCSI controller CRT 45; 68C05, ALU, 8200 series; shift register, multiplexers, 65Cx02, SRAM, EEPROM	•	•		•	•	•	Motorola
	VS1500 Si-gate CMOS 1.5 μm	M1 M2	120	0.28	0.8	76 gates 38 MSI >20 analog 39 I/O 14 special functions	RAM, ROM, multipliers (8×8, 16×16), dual-port RAM, ALU, counter, shift register, and multiplexer generators 7400 series, 8200 series, SRAM	•	•		•	•	•	None

1. Flip-flop toggle rate. 2. Gate power at frequency. 3. 2-in NAND delay, FO = 2, 1-mm wire. 4. C = CMOS, T = TTL. 5. C = commercial, I = industrial, M = military.

Directory of Cell Libraries (continued)

Company	Product Technology Line width	Wiring layers	Typical parameters			Cells		Interface levels[4]			Temp. ranges[5]			Second sources
			MHz[1]	mW[2]	ns[3]	Simple	Complex	C	T	ECL	C	I	M	
NEC Electronics	SC5; μpD92xxx Si-gate CMOS 1.2 μm	M1 3.6 μm M2 4.6 μm M3 7.2 μm	250	3	0.52	74 gates 70 MSI 150 I/O 91 74LS	RAM, ROM, 8200 peripherals, analog cells, ALU, etc.	•	•		•	•		None
	SC4 μpD91xxx Si-gate CMOS 1.5 μm	M1 5.4 μm M2 7 μm	140	2.1	0.9	50 gates 70 MSI 40 I/O 84 74LS	RAM, ROM, 8200 peripherals, analog cells, ALU, etc.	•	•		•	•		None
Oki Semiconductor	MSM91H000 CMOS 2 μm drawn	2	40	8	1.8	150	300, plus 80C51, RAM, ROM, PLA	•	•		•	•		None
	MSM91V000 CMOS 1.5 μm drawn	2	50	5	1.0	150	300, plus 80C51, RAM, ROM, PLA	•	•		•	•		None
	MSM91U000 CMOS 1.2 μm drawn	2	80	4	0.6	150	300, plus 32K RAM, ROM, PLA	•	•		•	•		None
Panasonic	MN71000 series Si-gate CMOS 2.5 μm	P1 M1 M2	n/s	n/s	1.9	200 gates 32 I/O	RAM, ROM, PLA	•	•		•	•		None
	MN72000 Si-gate CMOS 2 μm	M1 3 μm M2 3 μm	160	0.02	1.4	182 gates 18 I/O	RAM, ROM, PLA	•	•		•	•		None
	MN73000 Si-gate CMOS 1.5 μm	M1 2.3 μm M2 2.3 μm	200	0.02	1	182 gates 18 I/O	RAM, ROM, PLA	•	•		•	•		None
Plessey Semiconductor	MVA 5000 Si-gate CMOS 2 μm	M1 6 μm M2 6 μm	100	0.35	1.2	86 gates 65 MSI 10 analog 22 I/O	RAM, ROM, PLA, barrel shifters, (user-defined paracells)	•	•		•	•	•	Matra-Harris
	Macrochip (MM, MV, MF) Bipolar JI	n/s	n/s	n/s	n/s	45 analog	Cells can be redefined by the user	•	•	All	•	•	•	Custom Arrays
	MH Si-gate CMOS 4 μm	P1 M1	20	0.3	8	50 MSI 5–10 analog 20 I/O	RAM, ROM	•	•	All	•	•	•	None
	Compiled ASIC FABIII Bipolar JI (CML) 1.5 μm	M1 6 μm M2 6 μm	250	0.42	1	48 gates 51 MSI 18 analog 21 I/O	RAM, ROM, 16- bit multipliers, SCSI controller; ADC, VCO, user-definable analog	•	•	10K, 100K	•	•		None
Seattle Silicon	ChipCrafter Si-gate CMOS 1.2 μm	M1 3.1 μm M2 3.9 μm	400	2	0.6	24 gates (6 drive options) 12 MSI (plus user- definable) 6 analog 12 I/O (variable drive)	RAM, ROM, PLA, FIFO, multiplier-all cells are parameterized	•	•		•	•		None
	ChipCrafter Si-gate CMOS 1.5 μm	M1 4 μm M2 4.5 μm	350	1.7	0.75	24 gates (6 drive options) 12 MSI (many user- definable options) 6 analog 12 I/O (variable drive)	RAM, ROM, PLA, FIFO, multiplier-all cells are parameterized	•	•		•	•		None
	ChipCrafter Si-gate CMOS 2 μm	M1 4.95 μm M2 5.5 μm	210	1	1.2	24 gates (6 drive options) 12 MSI (many options) 6 analog 12 I/O (variable drive)	RAM, ROM, PLA, FIFO, multiplier-all cells are parameterized	•	•		•	•		None
Sierra Semiconductor	Si-gate CMOS 2 μm	P1 4 μm M1 5 μm M2 7 μm	70	0.2	1.5	70 gates 150 MSI 50 analog 40 I/O	RAM, ROM, PLA, EEPROM, μP, ADC, DAC, compiled cells, megacells	•	•		•	•	•	VLSI Technology
	Si-gate CMOS 1.5 μm	P1 3 μm M1 4 μm M2 5.5 μm	120	0.5	1	70 gates 150 MSI 50 analog 40 I/O	RAM, ROM, PLA, EEPROM, μP, ADC, DAC, compiled cells, megacells	•	•		•	•	•	VLSI Technology
Signetics/ Philips	SystemCell Si-gate CMOS 3 μm	P1 9 μm M1 9 μm	25	n/s	4	250 gates 53 MSI 62 I/O	n/s	•	•		•	•	•	Texas Instruments
	SystemCell Si-gate CMOS 2 μm	P1 3 μm M1 8 μm M2 8 μm	60	n/s	1.4	250 gates 53 MSI 62 I/O	RAM, ROM, PLA, 2900 family, SCSI bus initiator	•	•		•	•	•	Texas Instruments
	SystemCell II Si-gate CMOS 1.5 μm	P1 M1 6.4 μm M2 6.4 μm	60 max	n/s	1.3	131 gates 46 MSI 38 I/O 5 oscillators	Data-path elements, RAM, ROM, PLA, parametric blocks, megacells	•	•		•	•	•	Philips

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Company	Product Technology Line width	Wiring layers	Typical parameters			Cells		Interface levels[4]			Temp. ranges[5]			Second sources
			MHz[1]	mW[2]	ns[3]	Simple	Complex	C	T	ECL	C	I	M	
Silicon Systems	CC Si-gate CMOS 3 μm	P1 M1	25	n/s	3	40 gates 10 MSI 20 analog 23 I/O	RAM, ROM, PLA	•	•		•	•		RCA
	SSi 6600 Si-gate CMOS 3 μm	M1 12 μm	25+	n/s	<5	40 gates 10 MSI 20 analog 23 I/O	RAM, ROM, PLA	•	•		•	•	•	None
Silicon West	SWI 1000 Si-gate CMOS 2 μm	M1 M2	100	0.6	1.2	50 gates 25 MSI 8 I/O	RAM, ROM, PLA	•	•		•	•		LSI Logic VLSI Tech-nology
	SWI 2000 Si-gate CMOS 2 μm	P1 4 μm M1 6 μm M2 8 μm	100	0.6	1.2	50 gates 25 MSI 2 analog 8 I/O	RAM, ROM, PLA	•	•		•	•		None
S-MOS Systems	SSC 1000 Si-gate CMOS 1.8 μm	M1 7 μm M2 10 μm	70	1.2	0.9	131 MSI 192 I/O	RAM, ROM, PLA	•	•		•			None
Standard Micro-systems	Customation II Si-gate CMOS 3 μm	P1 6.3 μm M1 8.1 μm	24	0.25	1.8	71 gates 87 MSI 26 analog 21 I/O	RAM, ROM, PLA; UARTs, ADC, DAC, DTMF, 555, 8250, Manchester encoder-decoder, data separator, SCSI, 65CX02, timer, VCO	•	•		•	•	•	NCR
	Customation III Si-gate CMOS 1.6 μm	M1 5.5 μm M2 7.5 μm	60	0.28	1.1	71 gates 87 MSI 26 analog 23 I/O	RAM, ROM, PLA; UARTs, Manchester encoder-decoder, data separator, SCSI, 8259, ADC, timer, CRT controller	•	•		•	•	•	NCR
Tachonics	TCPM GaAs D-MESFET (SCFL) 1 μm	M1 6 μm M2 8 μm	1500	5	0.09	20 gates 6 MSI 1 analog 4 I/O	Designed to be integrated with MMIC functions	•	•	10KH	•	•	•	None
	SC5000 GaAs D-MESFET (CDFL) 0.8 μm	M1 4 μm M2 4 μm	2300	2.4	0.18	12 gates 13 MSI 6 I/O	10 analog and MMIC cells	•	•	10K, 100K	•	•	•	GigaBit Logic
Texas Instruments	SystemCell Si-gate CMOS 2 μm	M1 7.2 μm M2 5.4 μm	66	0.03/ MHz	1.2	114 gates 95 MSI 55 analog	13 special functions, SRAM, ROM, PLA, pipeline test register	•	•		•		•	Signetics/ Philips
	TSC500 series Si-gate CMOS 1 μm	M1 4.8 μm M2 4.8 μm	150	0.014 MHz	0.5	160 gates 77 MSI 166 I/O	22 special functions, SRAM, ROM, PLA, register files, FIFOs, 2901/02/04/10	•	•		•		•	None
TLSI	Si-gate CMOS 5 μm	P1 10 μm P2 12 μm M1 10 μm	10	0.35	6	5 gates 60 MSI 36 analog 15 I/O	RAM, ROM; bi-quads, PLL, V ref	•	•		•	•	•	Gould, GTE, Mitel, IMP
	Si-gate CMOS 3 μm	P1 7 μm M1 7 μm M2 8 μm	35	n/s	2.5	5 gates 60 MSI 25 analog 15 I/O	RAM, ROM; amplifiers, PLL bi-quads, V ref	•	•		•	•	•	Gould, IMP, Micrel
	Si-gate nMOS 4 μm	P1 9 μm M1 9 μm	8	n/s	8	5 gates 24 MSI 5 analog 12 I/O	RAM, ROM	•	•		•	•	•	Gould, Micro-Rel, Citel
Toshiba America	TC22SC Si-gate CMOS 2 μm	M1 5 μm M2 6 μm	100	n/s	1.5	100 gates 78 MSI	RAM, ROM, PLA; MSI functions are soft macros only	•	•		•	•		None
	TC23SC Si-gate CMOS 1.5 μm	M1 5.6 μm M2 6 μm	150	1.8	1	115 gates 45 MSI 412 I/O	RAM, ROM, PLA, 74XX logic, multipliers	•	•		•	•		GE, and Siemens

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Directory of Cell Libraries (continued)

Company	Product Technology Line width	Wiring layers	Typical parameters			Cells		Interface levels[4]			Temp. ranges[5]			Second sources
			MHz[1]	mW[2]	ns[3]	Simple	Complex	C	T	ECL	C	I	M	
TriQuint Semiconductor	Q-LOGIC GaAs D-MESFET 1 μm	M1 3 μm M2 4 μm	2500	4, 11, 45	1 0.3 0.08	70 gates 130 MSI 15 I/O	n/s	•	•	All	•	•	•	None
	QLSI GaAs E/D- MESFET 1 μm	M1 2 μm M2 3 μm	3000	2.5, 8	0.18, 0.12	19 gates 30 MSI 13 I/O	Custom digital/analog	•	•	All	•	•	•	None
Unicorn Microelectronics	Compile Si-gate CMOS 1.5 μm	M1 4.0 μm M2 4.4 μm	60	0.1	0.75	100 gates 50 MSI 20 I/O	RAM, ROM, PLA; datapath blocks, FIFO	•	•		•	•		Seiko, United Microelectronics
United Silicon Structures	US2 Solo library Si-gate CMOS 15 μm	P1 4.5 μm M1 6 μm M2 6.5 μm	130	.56	.85	51 gates 51 MSI 27 analog 58 I/O	RAM, ROM, PLA, 2901, multiplier; any user-defined cell is available through hardware description language	•			•	•	•	European Silicon Structures
United Technologies Microelectronics Center	UTBS Si-gate CMOS 3 μm	M1 7.5 μm M2 7.5 μm	190	2.25	1.54	49 gates 29 MSI 12 I/O	RAM, ROM; 1553 bus controllers, 1750 processors	•	•				•	None
	UTDS Si-gate CMOS 1.5 μm	M1 6 μm M2 6 μm	345	8	0.65	49 gates 29 MSI 12 I/O	RAM, ROM; 1553 bus controllers; 1750 processors	•	•				•	None
Vitesse Semiconductor	PGUSC-100 GaAs E/D-MESFET (DCFL, SCFL) 1.2 μm	M1 6 μm M2 6 μm M3 15 μm (power only)	2500	0.4	0.2	30 gates 25 MSI 10 I/O	RAM, PLA, 2900 bit-slice family in GaAs		•	•	•		•	Ford Microelectronics
VLSI Technology	VSC10 Si-gate CMOS 2 μm	M1 5 μm M2 7 μm	130	1.2	0.93	65 gates 110 MSI 85 I/O	RAM, ROM, PLA, multiplier; 82CXX peripherals; 68C45 CRT controller, Z80 CPU plus peripherals; 85C30; datapath compiler, logic synthesizer, high speed RAM	•	•		•	•	•	Rockwell
	VSC100 Si-gate CMOS 1.5 μm	M1 3.2 μm M2 4.5 μm	180	1.2	0.74	As above	As above	•	•		•	•	•	Rockwell
VTC	VL1000 Bipolar JI 3 μm	M1 8 μm M2 12 μm	50	2.25	2	9 SSI gates 15 MSI 64 analog 9 I/O	RAM, ROM, data converters, amplifiers		•	10K	•	•	•	None
	VL2000/3000 Bipolar OI 2 μm	M1 8 μm M2 12 μm	250	2.25	0.42	22 SSI gates 38 MSI 16 I/O	RAM, ALU, PLL, DAC		•	10K, 10KH	•	•	•	None
	VL5000 Si-gate CMOS 1 μm	M1 M2	200	n/s	0.5	50 gates 20 MSI 10 I/O	RAM, ROM, PLA; 2901, 2910, multiplier	•	•		•	•	•	None
WaferScale Integration	Modular Cell Si-gate CMOS 0.8 μm	P1 3.4 μm P2 2.6 μm M1 4.2 μm M2 4.8 μm	180	1.25	0.55	15 gates 45 MSI 20 I/O	RAM, ROM, PLA, EPROM, bit slice, multipliers, FIFOs, barrel shifters	•	•		•	•	•	GE
Xerox Microelectronics Center	Micro CMOS Si-gate CMOS 2 μm	M1 4.75 μm M2 6.25 μm	110	2.75	1	90 gates 98 MSI 10 analog 170 I/O	RAM, ROM, PLA, EEPROM; UARTs, 2901, 2911; 16-bit controller; comparators, opamps, voltage reference, analog switch, ADC configurable I/O drivers	•	•		•	•	•	IMP
Zymos	Zy60000 Si-gate CMOS 1.8 μm	M1 6 μm M2 6 μm	100	n/s	0.9	170 gates 205 MSI 40 I/O	RAM, ROM, PLA; Z2901 bit slice; Intel family peripherals (Z80C49, Z8237, Z8259, Z8254, Z8284, Z82284, Z82288); Z6818, Z74612	•	•		•	•		None

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Directory of Programmable Logic Products

Company and contact	Product or product family	Technology	Maximum/standby current consumption (mA)	Registered/-nonregistered propagation delay (ns)	Second sources	Design tools and programmers	Package types
Advanced Micro Devices Inc./ Monolithic Memories 901 Thompson Pl. PO Box 3453 Sunnyvale, CA 94088-3453 (800) 538-8450 Andy Robin Director of Marketing, Programmable Logic	**Am2064** **Am2018** **Am3020** **Am3030** **Am3042** **Am3064** **Am3090** **AmHCLA**	CMOS (R) CMOS (R) CMOS (R) CMOS (R) CMOS (R) CMOS (R) CMOS (R) CMOS	f[1]/5, 10 f[1]/5, 10 f[1]/1, 10 f[1]/1, 10 f[1]/1, 10 f[1]/1, 10 f[1]/1, 10 f[1]/1	6–12[2]/10–20[3] 6–12[2]/10–20[3] 5–8[2]/9–14[3] 5–8[2]/9–14[3] 5–8[2]/9–14[3] 5–8[2]/9–14[3] 5–8[2]/9–14[3] 5–8[2]/9–14[3]	Xilinx Xilinx Xilinx Xilinx Xilinx Xilinx Xilinx Xilinx	XACT, OrCAD, Daisy, FutureNet, Mentor	DIP, PLCC, PGA
	PALC20RA10Z **PALC29M16H** **PALC29MA16H** **PALC16L8Z** **16R4,6,8Z** **PALC20L8Z** **20R4,6,8Z** **PALC18U8Q** **PALC16L8Q** **16R4,6,8Q** **PALC22V10H** **PAL10H20EV8** **PAL10H20EG8** **PAL16L8-7** **16R4,6,8-7** **PAL16L8H** **16R4,6,8H** **PAL16L8** **16R4,6,8** **PAL20L8-10** **20R4,6,8-10** **PAL20L8** **20R4,6,8** **PAL22V10-15** **PAL22V10** **PAL22IP6** **PAL20RA10** **PAL16RA8** **PAL18P8** **PAL22P10** **PAL6L16/8L14** **PAL20L10** **20X4,8,10** **PAL20S10** **20RS4,8,10** **PAL32R16** **PAL32VX10** **PAL23S8** **PMS14R21** **PLS105** **PLS167** **PLS168**	CMOS (EE) CMOS (EE) CMOS (EE) CMOS (E) CMOS (E) CMOS (E) CMOS (E) CMOS (E) CMOS (E) CMOS (E) CMOS (E) ECL ECL TTL TTL TTL TTL TTL TTL TTL TTL TTL TTL TTL TTL TTL TTL TTL TTL TTL TTL TTL TTL TTL TTL TTL TTL TTL TTL TTL TTL TTL TTL	90/0.15 120 120 90/0.1 90/0.1 70/0.1 70/0.1 55 45 45 90 220, 280 220,280 180 180 90 90 55–180 55–180 210 210 105–210 105–210 180 180 210 200 170 90–180 105, 210 90 105–210 180 240 240 280 180 210 210 200 160 160	40,45/40,45 15/25 15/25 —/35 15/35 —/40, 45 20, 25/40, 45 15, 25/25,35 —/25 15/25 15, 25/25, 35 3.5/6 3.5/6 —/7.5 6.5/7.5 —/15 12/15 —/10–35 7–25/10–35 10 8/10 15–35 12–25/15–35 10/15 15, 25/25, 35 35/35 20, 30/20, 30 30/30 —/15–35 —/15, 25 —/40 —/15–30 15/30 —/35 17/35 25/40 15/25, 30 13, 15/20, 25 12, 20/— 10/— 13/— 15/—	Seeq Cypress Cypress Cypress NSC, TI NSC, TI NSC, TI NSC, TI TI NSC NSC NSC NSC	PALASM 2 (AMD), PLPL (AMD), ABEL (Data I/O), CUPL (Logical Devices), PLDesigner (Minc)	Windowed ceramic DIP, ceramic and plastic DIP, PLCC, LCC
	Am29CPL141 **Am29PL141** **Am29LPL141** **Am29PL142**	CMOS (E) TTL TTL TTL	105 450 315 500	13, 15/— 15/— 25/— 20/—		ASM14X, SIM14X (AMD)	Windowed ceramic DIP, ceramic and plastic DIP, PLCC, LCC
	Am2971	TTL	310, 425	22, 23/—		PEGPDS (AMD)	Ceramic DIP, flatpack, LCC
Altera Corp. 3525 Monroe St. Santa Clara, CA 95051 (408) 984-2800 David Laws Vice President, Marketing	**EP 310** **EP 320** **EP 600** **EP 900** **EP 1210** **EP 1800** **EPB 1400** **EPS 448** **EPB 2001** **EPB 2002** **EPM 5016** **EPM 5024** **EPM 5032** **EPM 5064** **EPM 5127** **EPM 5128**	CMOS (E) CMOS (E) CMOS (E) CMOS (E) CMOS (E) CMOS (E) CMOS (E) CMOS (E) CMOS (E) CMOS (E) CMOS (E) CMOS (E) CMOS (E) CMOS (E) CMOS (E) CMOS (E)	40/15 20/0.01 15/0.01 30/0.01 25/3 60/0.01 100/60 100/60	15-35/25-75 15-35/25-75 15-35/25-75 15-35/25-75 15-35/25-75 15-35/25-75 40 50/33	Intel, Cypress, TI, WSI	PLDS2, PLCAD4 (Altera), PCCAD-Supreme, PLDS-SAM; many third-party programmers, including Data I/O and Stag, PLDs—McMAP, PLDs—MAX	Ceramic DIP, ceramic LCC, windowed PGA, plastic LCC, plastic DIP (one-time programmable)
Atmel Corp. 2095 Ringwood Dr. San Jose, CA 95131 (408) 434-9201 Jack Peckham Vice President of Sales	**AT-22V10** **AT-22V10L** **AT-V750** **AT-V2500**	CMOS (E) CMOS (E) CMOS (E) CMOS (E)	100/100 15/12 120/120 15/5	15-25/25-40 15-25/25-40 25-35/30-40 35-45/35-45	Many for 22V10	ABEL (Data I/O); CUPL (P-CAD); Log/ic (ISDATA)	DIP, JLCC—plastic and ceramic
Cypress Semiconductor 3901 North First St. San Jose, CA 95134 (408) 943-2600 Al Graff Programmable Logic Product Manager	**PALC20 series**	CMOS (E)	70 mA, commercial; 70 mA, military	15–25/20–40	AMD, TI, NSC, Lattice	Data I/O ABEL, ISDATA Logic, Minc PLDesigner, CUPL, Cypress PLD Tool Kit; Data I/O, Stag, Kontron, Logical Devices, Digelec, Cypress QuickPro	20 pins: windowed DIP, ceramic DIP, plastic DIP, plastic SOJ, ceramic LCC
	PLDC18G8	CMOS (E)	80	10–15/12–20	Lattice, AMD, TI, NSC, Signetics	Data I/O ABEL, ISDATA Logic, Minc PLD Designer, CUPL, Cypress PLD Tool Kit; Cypress QuickPro	20 pins: windowed DIP, ceramic DIP, plastic DIP, plastic SOJ, PLCC, ceramic LCC

1. The maximum is a function of density and frequency. 2. Internal register setup time. 3. Internal logic delay block.

Directory of Programmable Logic Products (continued)

Company and contact	Product or product family	Technology	Maximum/standby current consumption (mA)	Registered/-nonregistered propagation delay (ns)	Second sources	Design tools and programmers	Package types
Cypress Semiconductor Corp. 3901 North First St. San Jose, CA 95134 (408) 943-2600 Al Graff Programmable Logic Product Manager	**PLDC20G10**	CMOS (E)	70, commercial 100, military	10–25/15–40	AMD, TI, NSC, Lattice	Data I/O ABEL, ISDATA Logic, Minc PLD Designer, CUPL, Cypress PLD Tool Kit; Data I/O, Cypress QuickPro	24pins: windowed DIP, ceramic DIP, plastic DIP, ceramic LCC; 28-pin PLCC
	PALC22V10	CMOS (E)	90 mA, commercial 120 mA, military	10–25/15–40	AMD, TI	Data I/O ABEL, ISDATA Logic, Minc PLD Designer, CUPL, Cypress PLD Tool Kit; Data I/O, Stag, Kontron, Logical Devices, Digelec, Cypress QuickPro	24 pins: windowed DIP, ceramic DIP, plastic DIP, ceramic LCC; 28 pins: windowed LCC, PLCC
	PLDC20RA10	CMOS (E)	80 mA, commercial 100 mA, military	20–35/20–35	AMD	Data I/O ABEL, ISDATA Logic, Minc PLD Designer, CUPL, Cypress PLD Tool Kit; Cypress QuickPro	24 pins: windowed DIP, ceramic DIP, plastic DIP, ceramic LCC; 28 pins: windowed LCC, PLCC
	CY7C330	CMOS (E)	120 mA, commercial 150 mA, military	15–25/n/a 50 MHz max,commercial; 40 MHz, military	—	Data I/O ABEL, Cypress PLD Tool Kit; Data I/O, Cypress QuickPro	28 pins: PLCC, windowed DIP, ceramic DIP, plastic DIP, ceramic LCC
	CY7C331	CMOS (E)	120 mA, commercial 150 mA, military	25–40/25–40	—	Data I/O ABEL, Cypress PLD Tool Kit; Data I/O, Cypress QuickPro	28 pins: windowed DIP, ceramic DIP, plastic DIP, PLCC, ceramic LCC
	CY7C332	CMOS (E)	120 mA, commercial 150 mA, military	20–35/20–35	—	Data I/O ABEL, Cypress PLD Tool Kit; Data I/O, Cypress QuickPro	28 pins: windowed DIP, ceramic DIP, plastic DIP, PLCC, ceramic LCC
Exel Microelectronics Inc. 2150 Commerce Dr. San Jose, CA 95131 (408) 432-0500 Patrick Frain Product Marketing Manager	**XL78C800-25** **XL78C800-35**	CMOS (EE) CMOS (EE)	35/17 30/15	25/25 35/35	—	ABEL (Data I/O); Multimap and Multisim (in-house enhancements to ABEL); Data I/O; Stag Microsystems; Inlab; SMS; Logical Devices	Skinny plastic DIP or ceramic DIP, LCC, PLCC
Gazelle Microcircuits Inc. 2300 Owen St. Santa Clara, CA 95054 (408) 982-0900 Robert Gunn Product Marketing Manager	**GA22V10-10** **GA22V10-7** **GA22VP10-7**	GaAs	210/210 220/220	7.5/10 6/7.5	n/s	All of Gazelle's devices are laser-programmed at the factory	Ceramic side-brazed DIP
Gould Inc. **Semiconductor Division** 2300 Buckskin Rd. Pocatello, ID 83201 (208) 233-4690 Jerry Homstad Vice President, Engineering	**PEEL 18CV8** **PEEL 153** **PEEL 173** **PEEL 253** **PEEL 273**	CMOS (EE) CMOS (EE) CMOS (EE) CMOS (EE) CMOS (EE)	25, 35/15, 25 45 45 45 45	18/25 30 30 30 30	International CMOS Technology	Data I/O, Structured Design, Stag, Valley Data Sciences, Varix, P-CAD Systems	Plastic DIP, ceramic DIP, CerDIP
Intel Corp. 1900 Prairie City Rd. FM 1-76 Folsom, CA 95630 (916) 351-6290 Karl H. Weigl Product Line Manager	**5C031,32** **5C060** **5C090** **5C121** **5C180** **5CBIC**	CMOS (E) CMOS (E) CMOS (E) CMOS (E) CMOS (E) CMOS (E)	40,25/30,0.1 30/0.1 35/0.1 100/30 50/0.15 110/0.1	30,15/40,30 20/45 20/50 35/65 30/70 30/70	Altera	iPLDs II, Schema II, iState state machines (Intel); interfaces to FutureNet, P-CAD	Plastic DIP (5C032, 060, 090); CerDIP window (031, 032, 060, 090, 121), PLCC (060, 090, 180, CBIC)
International CMOS Technology Inc. 2125 Lundy Ave. San Jose, CA 95131 (408) 434-0678 Greg Lara Product Marketing Engineer	**PEEL153, 173** **PEEL253, 273** **PEEL18CV8** **PEEL20CG10** **PEEL22CV10** **PEEL22CV10Z**	CMOS (EE) CMOS (EE) CMOS (EE) CMOS (EE) CMOS (EE) CMOS (EE)	35 + 1/MHz 35 + 1/MHz 20 + 0.7/MHz 45 + 0.5/MHz/45 45 + 0.5/MHz/45 45 + 0.5/MHz/.1	—/40,35,30 —/40,35,30 20–12/35–15 20,15/35,25 20,15/35,25 20,15/35,25	Gould Semiconductor	APEEL Logic Assembler (ICT), PDS-1 PEEL Development System (ICT), ABEL (Data I/O), CUPL (P-CAD), Data I/O, Digelec, Kontron, Logical Devices, Stag Microsystems, Advin Systems, BP Microsystems, Adams-MacDonald, and others	Plastic DIP, ceramic DIP, PLCC
Lattice **Semiconductor Corp.** PO Box 2500 Portland, OR 97208 (503) 681-0118 Bill Wiley Smith Director of Marketing	**GAL16V8A** **GAL16V8** **GAL20V8A** **GAL20V8** **GAL6001** **ispGAL16Z8**	CMOS (EE) CMOS (EE) CMOS (EE) CMOS (EE) CMOS (EE) CMOS (EE)	115/75 45/35, 90/70 115/75 45/35, 90/70 150/90 90/70	10/12 12/15 10/12 12/15 15/30 15/25	NSC, SGS-Thomson	Software: ABEL (Data I/O); CUPL (Logical Devices); PLDesigner (MINC); Programmable Logic Technology; Qwerty Inc.; Hardware: Data I/O; Stag; Logical Devices; Programmable Logic Technology; Qwerty Inc.; One-D; Advin Systes; and other programmers	Ceramic DIP, plastic DIP, PLCC, LCC, ceramic side-brazed DIP

Company and contact	Product or product family	Technology	Maximum/standby current consumption (mA)	Registered/-nonregistered propagation delay (ns)	Second sources	Design tools and programmers	Package types
National Semiconductor Corp. 2900 Semiconductor Dr. Santa Clara, CA 95051 (408) 721-6053 Bien Irace Product Marketing	**PAL1016P8** **10016P8** **1016RD8** **10016RD8** **1016P4A** **10016P4A** **1012C4A** **10012C4A** **1016RM4A** **10016RM4A**	ECL ECL ECL ECL ECL ECL ECL ECL ECL ECL	240 240 280 280 220 220 220 220 240 240	—/8 —/8 3/6 3/6 —/4 —/4 —/4 —/4 2/3 2/3	n/s	PLAN (NSC), ABEL (Data I/O) CUPL (P-CAD), Unisite (Data I/O), IQ-180/280 (Digital Media), ECL-1 and ECL-2 (IMS), Pallprox (Logical Devices)	Ceramic DIP, quad cerpack
	GAL16V8 **20V8**	CMOS (EE) CMOS (EE)	45–90/35–70 45–90/35–70	25–12/35–15 25–12/35–15	Lattice Lattice	PLAN (NSC), ABEL (Data I/O), GOA, Unisite (Data I/O), Logic Lab, Owerty	Plastic DIP, ceramic DIP, PLCC
	PAL10H8 **12H6** **14H4** **16H2** **10L8** **12L6** **14L4** **16L2** **16C1**	TTL TTL TTL TTL TTL TTL TTL TTL TTL	45–90 45–90 45–90 45–90 45–90 45–90 45–90 45–90 45–90	—/35–25 —/35–25 —/35–25 —/35–25 —/35–25 —/35–25 —/35–25 —/35–25 —/35–25	AMD AMD AMD AMD AMD AMD AMD AMD AMD	PLAN (NSC), ABEL (Data I/O), CUPL (P-CAD), PALASM (AMD), 303A-011 and 60A, Unisite (Data I/O), Allpno (Logical Devices), Stag ZL30A	Plastic DIP, ceramic DIP, PLCC
	PAL16L8 **16R4** **16R6** **16R8** **PAL12L10** **14L8** **16L6** **18L4** **20L2** **20C1** **PAL20L8** **20R4** **20R6** **20R8** **PAL20L10** **20X4** **20X6** **20X8** **PAL20P8** **20RP4** **20RP6** **20RP8** **PAL16RA8** **PAL20RA10**	TTL TTL TTL TTL TTL TTL TTL TTL TTL TTL TTL TTL TTL TTL TTL TTL TTL TTL TTL TTL TTL TTL TTL TTL	90–180 90–180 90–180 90–180 100 100 100 100 100 100 210 210 210 210 165 180 180 180 210 210 210 210 170 200	—/35–10 15–8/25–10 15–8/25–10 15–8/25–10 —/40 —/40 —/40 —/40 —/40 —/40 —/25–15 15–12/25–15 15–12/25–15 15–12/25–15 —/50–30 30–15/50–30 30–15/50–30 30–15/50–30 —/15 12/15 12/15 12/15 30/35 30/35	AMD, TI — AMD, TI AMD, TI AMD AMD AMD AMD AMD AMD AMD, TI AMD, TI AMD, TI AMD, TI AMD, TI AMD, TI AMD, TI AMD, TI AMD AMD AMD AMD AMD AMD	FAIM, Unisite (Data I/O), Digelec 803, Stag 30A800	n/s
PLX Technology Inc. 625 Clyde Ave. Mountain View, CA 94043 (415) 960-0448 Don Etzbach Sales Manager	**PLX448**	CMOS (E)	80/80	25/35	n/s	ABEL version 3.0 (Data I/O), CUPL (P-CAD), PET100 (PistoHI Tools), Data I/O, Digelec, Logical Devices, OAE; PistoHI Tools, Stag Microsystems, Sunrise	Plastic DIP, windowed ceramic DIP, LCC
Samsung Semiconductor Inc. 3725 North First St. San Jose, CA 95134 (408) 434-5561	**CPL (CMOS Programmable Logic)** **16R8** **16R6** **16R4** **16L8** **20R8** **20R6** **20R4** **20L8** **20L10** **22V10** **16V8**	CMOS (E)	80/45, 105/70	15, 25/25, 35	Cypress, AMD	Data I/O, Digelec, Digital Media, Kontron, Oliver Advanced Engineering, Stag, Varix	Plastic DIP, ceramic windowed DIP
Signetics Corp. 811 E. Arques Ave. Sunnyvale, CA 94086 (408) 991-5390 Joel Rosenberg PLD Marketing Manager	**PLS100** **PLC153** **PLS153** **PLS153A** **PLHS153** **PLUS153B** **PLUS153D** **PLS173** **PLUS173B** **PLUS173D** **PLC473-60**	TTL CMOS (E) and TTL TTL TTL TTL TTL TTL TTL TTL TTL CMOS (E) and TTL	170 60 155 155 155 200 200 170 200 200 45, 60	—/50 —/45 —/40 —/30 —/20 —/15 —/12 —/30 —/15 —/12 —/60	NSC, International CMOS Technology — — — — — — — — —	Amaze (Signetics), ABEL (Data I/O), CUPL (P-CAD); Data I/O model 298, 60, Unisite 40; Stag model ZL30/30A, PPZ2200	Commercial: plastic and ceramic DIP, windowed ceramic DIP, plastic PLCC. Military: ceramic DIP, windowed ceramic DIP, flat pack, LCC

Directory of Programmable Logic Products (continued)

Company and contact	Product or product family	Technology	Maximum/standby current consumption (mA)	Registered/-nonregistered propagation delay (ns)	Second sources	Design tools and programmers	Package types
Signetics Corp. 811 E. Arques Ave. Sunnyvale, CA 94086 (408) 991-5390 Joel Rosenberg PLD Marketing Manager	**PLHS473**	TTL	155	—/22	—	See previous page	See previous page
	PLHS18P8A	TTL	155	—/20	AMD		
	PLHS18P8B	TTL	155	—/15	AMD		
	PLHS16L8A	TTL	155	—/20	AMD, TI, NSC		
	PLHS16L8B	TTL	155	—/15	AMD, TI, NSC		
	PLUS16L8D	TTL	180	—/10	AMD, TI		
	PLUS16R8D	TTL	180	18/10	AMD, TI		
	PLUS16R6D	TTL	180	18/10	AMD, TI		
	PLUS16R4D	TTL	180	18/10	AMD, TI		
	PLUS20L8D	TTL	210	—/10	AMD		
	PLUS20R8D	TTL	210	18/10	AMD		
	PLUS20R6D	TTL	210	18/10	AMD		
	PLUS20R4D	TTL	210	18/10	AMD		
	PLC16V8	CMOS (E) and TTL	50, 90	55/35	Lattice, NSC		
	PLC20V8	CMOS (E) and TTL	50, 90	55/35	Lattice, NSC		
	PLS105	TTL	180	72/—	AMD, TI		
	PLS105A	TTL	180	50/—	AMD, TI		
	PLUS405	TTL	225	30/—	—		
	PLS155	TTL	190	70/50	—		
	PLS157	TTL	190	70/50	—		
	PLS159A	TTL	190	55/35	—		
	PLS167	TTL	180	72/—	AMD, TI		
	PLS167A	TTL	180	50/—	AMD, TI		
	PLS168	TTL	180	72/—	AMD, TI		
	PLS168A	TTL	180	50/—	AMD, TI		
	PLS179	TTL	210	55/35	—		
	PLHS501	TTL	295	—/22	—		
	PLHS502	TTL	370	—/20	—		
Texas Instruments Inc. P.O. Box 655012 Dallas, TX 75265 (800) 232-3200 Tim Schnettler Strategic Marketing Manager, Programmable Logic Products	**TIBPAL16L8**	TTL	100,180,200	25,15,10,7.5,12	MMI, AMD, NSC	ABEL (Data I/O); Digital Media; CUPL (Personal CAD Systems)	Commercial: plastic DIP, SMD. Military: ceramic DIP, LCC
	16R4,6,8	TTL	100,180,200	25,15,10,7.5,12			
	PAL16L8A/A-2	TTL	90,180	35,25	MMI, AMD, NSC		
	16R4,6,8A/A-2	TTL	90,180	35,25	MMI, AMD, NSC		
	TIBPAD16N8	TTL	180	7	—		
	TIBPAL20L8	TTL	105,180	25,15	MMI		
	20R4,6,8	TTL	105,180	25,15	MMI		
	PAL20L8A	TTL	210	25	MMI, AMD, NSC		
	20R4,6,8A	TTL	210	25	MMI, AMD, NSC		
	TIBPALT19L8	TTL	210	25	—		
	T19R4,6,8	TTL	210	25	—		
	R19L8	TTL	210	25	—		
	R19R4,6,8	TTL	210	25	—		
	20L10	TTL	165	20,30	MMI, NSC		
	20X4,8,10	TTL	165	20,30	MMI, NSC		
	TIB82S105B	TTL	180	15	Signetics		
	82S167B	TTL	160	15	Signetics		
	TIBPAL22V10A	TTL	180	25	AMD		
	22VP10	TTL	210	20	—		
	TIFPLA839	TTL	180	20	—		
	840	TTL	180	25	—		
	TICHAL16L8	CMOS	0.1	35	—		
	16R4,6,8	CMOS	0.1	35	—		
	TICPAL16L8	CMOS	0.1	55	—		
	16R4,R6, R8	CMOS	0.1	55	—		
	TICPAL18V8Z	CMOS	0.1	25	IDT		
	TICPAL22V10Z	CMOS	0.1	35	AMD, MMI, Cypress NSC		
	TIEPAL10H16P8	ECL	240	6	NSC		
	TIEPAL10016P8	ECL	240	6			
Xilinx Inc. 2069 Hamilton Ave. San Jose, CA 95125 (408) 559-7778	**XC2064**	CMOS	25–50 max	17/10[1]	AMD	PC-based: Schema, FutureNet, OrCAD, P-CAD, Case, Viewlogic. Workstation: Daisy, Mentor, Valid, Xilinx Xact	Plastic DIP, PLCC, PGA, CQFP
	XC2018	CMOS	50–75 max	17/10[1]			
	XC3020	CMOS	50–75 max	16/9[1]			
	XC3030	CMOS	75–100 max	16/9[1]			
	XC3042	CMOS	100–150 max	16/9[1]			
	XC3064	CMOS	175–250 max	16/9[1]			
	XC3090	CMOS	250–350 max	16/9[1]			

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Toshiba America Inc.
1220 Midas Way
Sunnyvale, CA 94086
(408) 733-3223
Allan Cox
Director of Marketing
Semicustom Products
MOS IC Division

TriQuint Semiconductor
P.O. Box 4935, Group 700
Beaverton, OR 97075
(503) 644-3535
Louis Pengue
Product Marketing Manager

Unicorn Microelectronics Corp.
99 Tasman Dr.
San Jose, CA 95134
(408) 433-3388
H.Y. Liu
Sales Manager

United Silicon Structures (US2)
1971 Concourse Dr.
San Jose, CA 95131
(408) 435-1366
Steven Eliscu
Product Marketing

United Technologies Microelectronics Center
1575 Garden of the Gods Rd.
Colorado Springs, CO 80907
(719) 594-8124
Ronald Hehr
Manager, Semicustom Products

Vitesse Semiconductor
741 Calle Plano
Camarillo, CA 93010
(805) 388-3700
Joe Welsh
ASIC Product Marketing Manager

VLSI Technology Inc.
1109 McKay Dr.
San Jose, CA 95131
(408) 434-3100
Bill Murray
Tactical Marketing Manager

VTC Inc.
2401 E. 86th St.
Bloomington, MN 55425
(612) 851-5200
John S. Monson
ASIC Product Marketing Engineer

WaferScale Integration Inc.
47280 Kato Rd.
Fremont, CA 94538
(415) 656-5400
Rich Talburt
Manager, CSD Design

Wyle Laboratories Electronics Marketing Group
18910 Teller Ave.
Irvine, CA 92715
(714) 851-9953
(408) 727-2500
Rick Timmins
Vice President of Semicustom ICs

Xerox Microelectronics Center
701 S. Aviation Blvd.
El Segundo, CA 90245
(213) 333-7701
Gary Petrov
Manager, Regional Design Support Centers

Xilinx Inc.
2069 Hamilton Ave.
San Jose, CA 95125
(408) 559-7778
Lee Farrell
Product Marketing Director

ZyMOS Corp.
477 N. Mathilda Ave.
Sunnyvale, CA 94088
(408) 730-5400
Vic Pasini
Tactical Marketing Director

Directory of ASIC Design Centers

ABB HAFO Inc.
11501 Rancho Bernardo Rd., Suite 200
San Diego, CA 92127

Kay Baird
Marketing Administrator
(619) 485-8200

San Diego, CA: 5 engineers; 1 VAX-11/780; Tektronix graphic terminals; Racal-Redac system
Stockholm, Sweden: 30 engineers; 2 VAX 8530s ; 4 VAX-11/780s; Tektronix graphics terminals; Racal-Redac systems; ZyCAD logic evaluator; Daisy, Mentor, Tektronix, and P-CAD workstations.

Communications are available via 1,200-baud dial-up modems and dedicated-line X.25 networks. Customized training classes are offered at the company's or the customer's facilities.

Advanced Micro Devices Inc.
5900 E. Ben White Blvd., M/S 538
Austin, TX 78741

Bruce Smith
Product Marketing Manager
(512) 462-5667

Boston, MA: 1 engineer; 1 workstation
Sunnyvale, CA: 1 engineer; 1 workstation

Communications at 9,600 bps; one-on-one training.

Applied Micro Circuits Corp.
6195 Lusk Blvd.
San Diego, CA 92121

Allyn Pon
Product Marketing Manager
(619) 450-9333

San Diego, CA: 10 engineers; 7 computers/workstations
Milan, Italy (ACSIS): 6 engineers; 1 computer/workstation
Tokyo, Japan (Teksel Co. Ltd.): 2 engineers; 1 computer/workstation
Stockholm, Sweden (Sattco): 4 engineers; 1 computer/workstation
Cambridge, UK (Hi-Tek Distribution): 3 engineers; 3 computers/workstations
Breisach, West Germany (Bacher GmbH): 2 engineers; 1 computer/workstation

Training offered includes a two-part class: 3 days on design methodology followed by 1.5 lab days on engineering workstations; full documentation including note set and design manual; 1 instructor per 14 (maximum class size); 1–2 students per EWS.

Arrow Electronics
25 Hub Dr.
Melville, NY 11747

Mel Kutzin
Semicustom Design Services
(516) 391-1300

Sunnyvale, CA: 4 engineers; Daisy MegaLogician, 1 Mentor (Apollo DN3000)
Baltimore, MD: 5 engineers; 1 Mentor (DN3000), Daisy Personal Logician; 2 terminals

Design centers for National Semiconductor, Texas Instruments, and VLSI Technology products. Dial-up modems at 1,200/2,400 baud; dedicated lines, East Coast, at 9,600 baud; Ethernet; direct access to Arrow mainframes, hardware accelerators, and workstations; tie-in to TI regional design centers. Hands-on one-day courses in schematic capture and simulation at the workstations. IC and workstation vendor training manuals and data books available. One instructor for 3–5 students; 1–2 students per workstation. Buy or lease CAD tools from Arrow. (Mil-Std-883 screening available for ASIC products.)

ASIC Northwest Inc.
405 114th Ave. SE #205
Bellevue, WA 98004

John L. Barney
President
(206) 451-9335

Bellevue, WA: 1 engineer; 1 Mentor (DN3000)

Dial-up communication available at 2,400 baud. Customer and turnkey designs for NCR standard cells and gate arrays, US2 standard cells, and KMOS Semicustom Designs mixed analog/digital arrays.

AT&T Technologies Inc.
1 Oak Way
Berkeley Heights, NJ 07922

(800) 372-2447

Sunnyvale, CA: 14 engineers; 1 VAX-11/785; 2 Daisy, 2 Mentor, 4 AT&T workstations; 10 terminals
London, England: 5 engineers; 2 MicroVAXes, 1 Mentor; 5 terminals
Madrid, Spain: 5 engineers; 1 VAX-11/785, 1 MicroVAX, 1 AT&T 3B2/400, 7 AT&T workstations; 12 terminals.
Munich, West Germany: 15 engineers; 1 VAX-11/785; 2 Daisy, 2 Mentor, 2 Valid, 4 AT&T workstations; 15 terminals
Singapore: 7 engineers; 1 VAX-11/785; 12 terminals.

Dedicated 56-kilobaud data links hook up to an IBM 3081, located in AT&T's research center in Allentown, PA. In Allentown, courses on design techniques and AT&T CAD tools are given every two months; at the design centers, they occur on an as-needed basis. There is one student per terminal; the ratio of students to instructors is 5:1.

Barvon BiCMOS Technology Inc.
1992 Tarob Ct.
Milpitas, CA 95035

Sales Department
(408) 262-8368

Milpitas, CA: 7 engineers; 1 Mentor, 1 Apollo, 1 P-CAD; 5 terminals

Barvon offers several classes in design methodology, electrical design, placement/routing and simulation for digital, mixed analog and digital, and analog designs using gate arrays and standard cells. Training is available from established outlines or tailored to satisfy individual needs.

California Micro Devices
215 Topaz St.
Milpitas, CA 95035

Matt Townsend
Marketing Manager
(602) 921-4641

Cherry Semiconductor Corp.
2000 S. County Trail
East Greenwich, RI 02818

Bob Maigret
Manager of Semicustom Products
(401) 885-3600

Coherent Design
275 Saratoga, Suite 200
Santa Clara, CA 95050

Roger Biros
President
(408) 296-3710

Santa Clara, CA: 7 engineers, 2 support

Coherent Design serves as a turnkey, systems level design team, working from customer specifications to produce schematics, netlist and test vectors for CMOS gate arrays and cell libraries. Coherent design provides quick-turn prototypes (Xilinx) and fix-mode ASICs from a common database. All designs are vendor independent. ASIC vendors supported include National Semiconductor, LSI Logic, VLSI Technology, Sanyo Semiconductor, S-MOS Systems, Xilinx, and Plessey Semiconductors. Complete simulation and test facilities available.

Control Data Corp.
8100 34th Ave. South
Minneapolis, MN 55440

Robert L. Biggs
Marketing Manager
(612) 853-3117

Plymouth, MN: 12 engineers; 5 Mentor, 1 Daisy

Communications are via HASP 4,800 baud; X.25, 4,800 baud; Kermit 9,600 baud; and dial-up modems with support for workstations. A one-week design class includes a complete set of manuals and covers workstation usage, design verification, and testability analysis. There are 5–10 students per class; 1–2 students per Mentor workstation. Additional services include multichip, multiboard system simulation, IC characterization, and PCB manufacturing/assembly facilities.

Custom Arrays Corp.
525 Del Rey Ave.
Sunnyvale, CA 94086

George N. Krautner
Vice President, Marketing
(408) 749-1166

Complete CAE/CAD design methodology using PC AT or PC386 platform. Liberty proprietary software addresses schematic capture; SPICE simulation; symbolic layout; and layout verification, consisting of design

rule checking, electrical rule checking, layout vs. schematic, postlayout SPICE netlist extraction, and schematic back annotation. Half-day training on PC AT–based workstation is usually sufficient, and all manuals are included. Students each have their own workstation. Additional services include full-custom design of linear circuits, and mixed analog and digital design using bipolar and CMOS technology.

Custom Silicon Inc.
600 Suffolk St.
Lowell, MA 01854

David W. Guinther
Vice President
(508) 454-4600

Lowell, MA: 8 engineers; 4 Apollo, 4 Viewlogic, 2 FutureNet, 1 Daisy; 11 terminals

Communications exist via 1,200- and 4,800-baud modem connections. Design manuals and data books are included with all classes. Classes are structured with one instructor and workstation to no more than two students. CSI offers full turnkey, joint development, and customer-designed IC programs for NCR standard cells, Motorola gate arrays, and Plessey bipolar linear arrays. CSI software products include generic libraries and design kits for Viewlogic and Mentor workstations.

Design Devices
20301 Century Blvd., MS A-23
Germantown, MD 20874

Steve Becraft
Department Manager
(301) 428-6660

Germantown, MD: 3 engineers; Mentor, Valid, MicroVAX II, PC AT; 2 terminals, 1 hardware accelerator

Dial-up communications are available at 2,400 baud. Introduction to ASIC Design is the training class offered, and it includes class notes and vendor-specific literature. One instructor is provided for every four students and one workstation for every two students.

Design Engineering Inc.
1900 13th St., Suite 304
Boulder, CO 80302

Stephen L. Davis
President
(303) 440-7997

Saratoga, CA: 1 engineer; 1 Cadnetix
Boulder, CO: 4 engineers; 3 Daisy, 1 Mentor
Roswell, GA: 2 engineers; 2 Mentor
Plano, TX: 2 engineers; 2 Mentor

Dial-up 2,400-baud communications at each site. Sale of ASIC designer productivity enhancement tools: Sim-P/L, simulation pattern generation language compiler; ORCMNT, OrCAD-to-Mentor schematic translator.

Exar Corp.
2222 Qume Dr.
San Jose, CA 95131

Shyam Dujari
Digital Products Marketing Manager
(408) 434-6400

San Jose, CA: 12 engineers; Mentor systems, VAX 8600

Dial-up communications at 1,200 baud. Training on the N2000 standard-cell library and design manuals on Exar's technologies are offered. Workstations available for customer design use. Full-custom analog cell development available.

Fujitsu Microelectronics Inc.
3545 North First St.
San Jose, CA 95134

(408) 922-9000

San Jose, CA: 15 engineers; Fujitsu, Amdahl, Sun, Apollo, Valid, Daisy; Ikos hardware accelerator
Atlanta, GA: 5 engineers; Sun, Daisy
Chicago, IL: 4 engineers; Sun, Valid
Boston, MA: 8 engineers; Sun, Daisy, Valid
Dallas, TX: 6 engineers; Sun, Daisy, Valid

Design systems at these centers include LCAD, ViewCAD, Daisy, Mentor, Valid. Fujitsu has dial-up and dedicated lines available; dedicated lines run at 19 kbps to San Jose host.

GE Microelectronics Center
1 Micron Dr.
PO Box 13049
RTP, NC 27709

D.J. Blackley
Manager, Program Acquisition
(919) 549-3100

Research Triangle Park, NC

Dial-up communications at 9,600 baud. Equipment and services include Mentor, Valid, FutureNet systems; VAX/VMS-based Lasar; engineering design assistance; application engineering assistance (at RTP only).

Genesis Microchip Inc.
2900 John St.
Markham, Ontario L3R 5G3

Bill White
Vice President of Sales
(416) 470-2742

Logic simulation accelerator

Gennum Corp.
P.O. Box 489, Station A
Burlington, Ontario
Canada L7R 3Y3

Adrian Gheron
Senior Applications Engineer
(416) 632-2996
(800) 263-9353

Yardley, PA (Carpenter Electronic Associates Inc.)
Burlington, Ontario: 14 engineers; Computervision, PC AT, Compaq/386, VAX
Tokyo, Japan (Gennum Corp)
Chateaubourg, France (Sorep)
Delft, the Netherlands (Catena Microelectronics BV)
Tucson, AZ (Production Services Inc.)

Customers who have commitments to Gennum are invited to join the staff of the design centers for a seminar on linear design. The company also offers a one-day seminar on an as-needed basis at the customer's location. It uses a semicustom design manual and sells a $99 kit that has a CAD tape of the six Gennum chips for routing. Gennum offers a range of services from prototyping based on the customer's design to design from customer application information.

GE Solid State
724 Route 202
P.O. Box 591
Somerville, NJ 08876

Phyllis Orlando
Marketing Communications
(201) 685-6585

Brussels, Belgium (SDM)
Brussels, Belgium: 6 engineers; VAX 6220, MicroVAX, 3 Daisy
San Jose, CA: 5 engineers; VAX 8600, 4 Daisy, 1 Mentor, 1 silicon compiler
Boulder, CO (Integrated Silicon Systems): 1 engineer; 1 Mentor
Paris, France: 2 engineers; 2 Daisy
Hamburg, West Germany: 1 engineer; 1 Daisy
Munich, West Germany: 1 engineer; 1 Daisy
Hong Kong: 1 engineer; VAX-11/750, 1 Daisy, 1 P-CAD
Tel Aviv, Israel (Aviv)
Ancona, Italy (Iselqui)
Boston, MA: 1 engineer; 1 Daisy, 1 P-CAD
Somerville, NJ: 5 engineers; VAX 8800, VAX 8830, 1 MicroVAX, 8 Daisy, 1 Mentor, 1 Valid, 1 P-CAD, 1 FutureNet, 1 silicon compiler
Durham, NC: 5 engineers; 1 MicroVAX, 3 Daisy, 1 Sun
Research Triangle Park, NC (Integrated Silicon Systems): 12 engineers; 1 Daisy, 2 Mentor, 2 P-CAD, 2 FutureNet, 4 LTL100 layout systems
Oslo, Norway (Nordic)
Singapore (NTI)
Madrid, Spain (Lober): 1 MicroVAX
Dallas, TX: 2 engineers; 2 Daisy, 1 P-CAD
Camberley, UK: 1 engineer; 1 Daisy

GE Solid State has customer dial-up service at 2,400 baud, and ISS has 1,200-baud modems. GE offers a three-day training course in Somerville, San Jose, and Brussels, with one engineer at a workstation. The course is designed to teach an engineer to design semicustom circuits with standard cell and gate arrays using GE's Fastrack ASIC Design Management System. All data books and training manuals are included.

GigaBit Logic Inc.
1908 Oak Terrace La.
Newbury Park, CA 91320

Anthony Conoscenti
Product Marketing Engineer
(805) 499-0610

Los Angeles, CA: 10 engineers; 3 Daisy, 3 VAX, 2 Calma, 1 Mentor, 1 Sun; 2 Tektronix layout terminals
Woodland Hills, CA (Navasys): 4 engineers; 2 Daisy
S. Portland, ME (QSI Corp.): 10 engineers; 5 Computervision, 1 Sun; 1 terminal

A custom IC training seminar that runs 1–6 days is offered at GigaBit, 4- and 1-day standard-cell training seminars are offered at customers' locations. Each seminar is taught to a single customer at a time and includes design manuals. Additionally, SPICE simulation, DRC, ERC, and LVS are available. In Japan, the distributor Tel (Tokyo) supports GigaBit products with design centers in Yokohama, Yamanashi, Kyushu, Tohoku, and Osaka.

Gould Inc.
Semiconductor Division
2300 Buckskin Rd.
Pocatello, Idaho 83201

Jerry Homstad
Vice President, Engineering
(208) 233-4690

Cupertino, CA: 2 engineers; Mentor, IBM PCs
Altamonte Springs, FL: 1 engineer; Mentor, Daisy, IBM PC
Jericho, NY: 1 engineer; Mentor, Daisy, IBM PC
Edina, MN: 1 engineer; IBM PC

Two-day gate array and standard-cell design training, provided by field application engineers, includes a user's guide to workstations. The student-to-instructor ratio is 1:4, and the student-to-workstation ratio is 1:1 or 2:1. Gate array and standard-cell design manuals are given out; subscribers automatically receive updated library sheets from Gould.

Hall-Mark Electronics Corp.
11333 Pagemill Rd.
Dallas, TX 75243

Wayne Howse
ASIC/USIC Program Manager
(214) 343-5923

Tampa/St. Petersburg, FL: 1 engineer; Sun-3/160C, PC AT
Atlanta, GA (Norcross): 1 engineer; Sun-3/160C, PC AT
Boston, MA: 1 engineer; Sun 3/160C, PC AT
Baltimore, MD: 2 engineers; Daisy MegaLogician, Personal Logicians (4 workstations, 1 PC AT, 6 terminals; Sun-3/160C); Sun-3/260
Austin, TX: 1 engineer; Daisy Personal Logician

The design centers offer LSI Logic and Motorola products. Baltimore has dedicated and dial-up lines for remote communications; Austin, Atlanta, and Tampa/St. Pete have dial-up only. A 5-day class offers 3 days of lecture and lab plus 2 days of design. Macrocell library and design manuals are provided. One instructor trains 10 students; pairs of students share a terminal.

Hamilton/Avnet Electronics
1175 Bordeaux Dr.
Sunnyvale, CA 94089

Robert M. Gardner
Vice President/General Manager
(408) 743-3001

Chandler, AZ: 4 engineers
Chatsworth, CA: 3 engineers
Costa Mesa, CA: 3 engineer
Gardena, CA: 1 engineers
Sunnyvale, CA: 5 engineers
Boston, MA: 4 engineers
Baltimore, MD: 1 engineer

Hamilton/Avnet has dial-up communications and offers training courses for its customers. Additional equipment includes Ikos hardware accelerator.

Honeywell Inc.
1150 E. Cheyenne Mountain Blvd.
Colorado Springs, CO 80906

David Wick
ASIC Product Line Manager
(719) 540-3580

Colorado Springs, CO: 10 engineers; Elxsi 6400, 5 Mentor, 4 Daisy; 5 terminals
Minneapolis, MN: 9 engineers; VAX-11/78x, 2 Mentor, 1 Daisy; 3 terminals

Communications available include dial-up at 1,200 baud and dedicated at 9,600 baud. There is a five-day training course for designing CMOS, bipolar, and rad-hard arrays. The course examines Honeywell's array technology and macro library, as well as the full gate array development sequence from system feasibility and partitioning through physical layout and test program generation. A design manual and course materials are included. There is one instructor per four students and one workstation per two students. Honeywell also has Teradyne's Lasar 6 simulation provided on a VAX, Merlyn-G layout tools on Elxsi, MSPICE on VAX and Apollo, and applications engineering support.

Hughes Aircraft Co.
Microelectronics Center
500 Superior Ave.
Newport Beach, CA 92658-8903

Mike Friedman
Applications Manager
(714) 759-2727

Communications are linked via telephone to Hughes's VAX. Training available includes a 2-day course on using library and timing analysis tools on a workstation.

Integrated Circuit Systems Inc.
2626 Van Buren Ave.
PO Box 968
Valley Forge, PA 19482-0968

Faye Jeffries-Cirino
Sales/Marketing Coordinator
(215) 666-1900

King of Prussia, PA: 18 engineers; 2 Daisy, 2 Mentor, 1 VAX-11/780, 2 Calma GDS II; 24 terminals

Dial-up communications at 1,200 and 9,600 baud are available. Training is tailored to the customer, usually with a ratio of one instructor to two or three students. Instruction may use Mentor, Daisy, PC, or VAX systems, depending on the customer's needs. Full-custom layout for minimum production cost, maximum performance, or unique function also is available.

Integrated Circuit Technology Inc.
22691 Lambert St.
Suite 514
El Toro, CA 92630

Akhtar Ali
Vice President, Engineering
(714) 581-7195

El Toro, CA: 2 engineer assistants, 3 engineers; 2 Apollo (DN4000, DN3000); HP plotter

ICT has developed an efficient automatic custom layout methodology that reduces the time spent on custom IC designs by about 50%. The company provides low-cost design services and, besides its own software, has a complete set of design tools, including schematic capture, logic and circuit simulators, and back-end verification, resident on a network of Apollo workstations (DN4000/3000).

Intel Corp.
3065 Bowers Ave.
Santa Clara, CA 95051

Mike Fister
Design Center Operations Manager
(602) 961-8172

Santa Clara, CA
Swindon, England
Paris, France
Tsukuba, Japan
Boston, MA

Communications are via a 9,600-baud dedicated line. Customer education consists of a set of modular courses (including manuals) for teaching gate array, standard-cell, and microprocessor/peripheral core classes. One instructor teaches a maximum of 8 students; 2 students share a workstation. Workstations are Daisy, Mentor, and MicroVAX II. Design assistance, turnkey services, and hot-line support also are available through the the design centers.

International Microcircuits Inc.
3350 Scott Blvd.
Santa Clara, CA 95054

Nasser Abdollahi
Product Marketing
(408) 727-2280

Santa Clara, CA: 19 engineers
Basingstoke, England (IMI UK Ltd.): 4 engineers; 2 Daisy, 2 Mentor
Paris, France (Sagem): 12 engineers; 6 Mentor
Herzelia, Israel (AST): 2 engineers; 1 Daisy, 1 Mentor

Dial-up communications are available. IMI offers an Easygate user's training course in which students bring in their circuit and test requirements. Easygate is customer interface software that uses production test vectors to generate the stimuli for design simulation to guarantee design testability. Instruction is one on one, with one workstation per student.

International Microelectronic Products Inc.
2830 N. First St.
San Jose, CA 95134

Thomas Flageollet
Marketing Manager
(408) 434-1362

San Jose, CA: 50 engineers; 2 Prime 9950s, 2 VAX 750s, 4 Sun-3/280s, 6 Sun 3/160s; 60 terminals
Swindon, England: 3 engineers; Mentor, Sun

Communications exist via dial-up 2,400-baud modems and X.25 Telenet service. Training is tailored to individual customers' needs with reference to schematic capture, logic simulation, and design verification. IMP provides automatic translation of foreign netlists with its universal netlist translator software.

LSI Logic Corp.
1551 McCarthy Blvd., MS D102
Milpitas, CA 95035

Susan Josephson
Marketing Communications
(408) 433-8000

Milpitas, CA	**Irvine, CA**	**Sherman Oaks, CA**
Boca Raton, FL	**Itasca, IL**	**Bethesda, MD**
Waltham, MA	**Minneapolis, MN**	**Edison, NJ**
Dallas, TX	**Bellevue, WA**	**Vienna, Austria**
Calgary, Canada	**Edmonton, Canada**	**Burnaby, Canada**
Kanata, Canada	**Toronto, Canada**	**Pointe Claire, Canada**
Paris, France	**Ramat Hasharon, Israel**	**Milan, Italy**
Tokyo, Japan	**Tsukuba, Japan**	**Osaka, Japan**
Seoul, Korea	**Oss, the Netherlands**	**Livingstone, Scotland**
Biel, Switzerland	**Bracknell, England**	**Berlin, West Germany**
Dusseldorf, West Germany	**Stuttgart, West Germany**	**Munich, West Germany**
Isernhagen, West Germany	**Luebeck, West Germany**	

(See also distributors Wyle Electronics Laboratories, Hamilton/Avnet, and Hall-Mark Electronics)

Two to 30 applications engineers per LSI Logic design resource center are available to assist with designs. Main computer centers are located at Milpitas, Waltham, Bracknell, Munich, Paris, and Tokyo. All others are tied in through direct 9,600-baud lines. All design centers offer training classes on the company's Modular Design Environment (MDE) ASIC software tools (including advanced simulation, schematic capture, and floorplanning), workstations, and array and cell-based design.

Marconi Electronic Devices Inc.
45 Davids Dr.
Hauppauge, NY 11788

Dale Wilson
Vice President of Sales and Marketing
(516) 231-7710

Hauppauge, NY: Daisy and Mentor workstations available for customer usage
Wembley, England: 18 engineers; 2 VAX 7850, 4 Mentor, 2 Applicon
Lincoln, England: 18 engineers; 2 Daisy, 7 Mentor, 2 VAX 7850

Communications via dial-up or leased line up to 9,600 baud. Training courses in Hilo. Marconi trains engineers in digital design, simulation, test generation, layout, and other design skills. Manuals are provided. Typically, there is a 6:1 ratio of students to instructors and a 2:1 ratio of students to workstations. One-on-one as well as group (three students) training can be arranged. Training classes at Wembley, England.

Matra Design Semiconductor
2840-100 San Tomas Expwy.
Santa Clara, CA 95051

Pradip Madan
Vice President, Marketing and Sales
(408) 986-9000

Santa Clara, CA: 10 engineers; IBM PCs, VAX; IBM PC terminals
Paris, France: 12 engineers; MicroVAX, VAX, Daisy, Mentor, IBM PCs; Tektronix and IBM PC terminals
Munich, West Germany: 5 engineers; Tektronix and IBM PC terminals
Milan, Italy: 1 engineer; Tektronix and IBM PC terminals
Stockholm, Sweden: 1 engineer; Tektronix and IBM PC terminals
Bracknell, UK: 2 engineers; Tektronix and IBM PC terminals

Communications are via a 4,800- and 9,600-baud dedicated line. Training courses are offered on the average of one per week or as needed, with one instructor for every 3–6 students and one workstation for every 1–2 students. The training at the design center focuses on gate array design guidelines, using MDS design tools, integrating PALs efficiently into gate arrays, implementing RAM on the MB series, packaging options, and testability issues. Design manuals, users' software manuals, and cell library information are provided. Design software is available on a PC that provides complete support for the customer for remote designs, from schematic capture through simulated netlist transfer for layout.

MCE Semiconductor Inc.
1111 Fairfield Dr.
West Palm Beach, FL 33407

Richard McCargar
Vice President
(407) 845-2837

Prototype and evaluation capability using the MCE UniDES System. MCE's design aids and tools include layout worksheets, instructions on how to interconnect the components by specifing the final interconnecting pattern metal mask, kit parts, and data sheets.

Micro LSI
2065 Martin Ave., Suite 101
Santa Clara, CA 95050

Dusty Duistermars
Chief Engineer
(408) 727-7987

Santa Clara, CA: 2 engineers; 2 Daisy

Dial-up modem lines at 1,200 baud are available for file transfer. One-on-one instruction of 2 students per instructor and per workstation is provided.

Mietec
Westerring 15
9700 Oudenaarde
Belgium

J.Y. Peigne
Communications Director
055-33-22-11

Paris, France: 1 engineer; MicroVAX; 2 terminals
Bracknell, UK: 1 engineer; MicroVAX; 2 terminals
Munich, West Germany: 1 engineer; MicroVAX; 2 terminals

Communications via dedicated line 19.2 kbaud. Training classes are offered for each point of the company's CAD system, MADE (Mietec Analog and Digital Engineering system). Private customer offices are available 24 hours a day, 7 days a week. Full plotting services, telefax, telex, and telephone facilities are provided for customer services.

Mitsubishi Electronics America Inc.
1050 E. Arques Ave.
Sunnyvale, CA 94086

Thomas Liao
Product Manager
(408) 730-5900

Sunnyvale, CA: 8 engineers; 2 Mentor, 2 FutureNet, 1 Daisy, 2 Valid, 1 Intergraph; 1 Ikos
Durham, NC: 12 engineers; 2 Daisy, 3 FutureNet, 2 Valid, 4 Mentor, IBM 4381/3270

Communications are available via dial-up lines at 1,200/2,400 baud and a dedicated line at 9,600 baud; remote access is also available via IBM-net. Classes can be scheduled at customers' locations for five or more students.

Motorola Inc.
1300 N. Alma School Rd., CH-180
Chandler, AZ 85224

Michael Ponzo
Tactical Marketing
(602) 821-4219

All centers listed below have similar staff and equipment: 1–3 engineers; Daisy or Mentor workstations for CAE tools.

Los Angeles, CA	**San Jose, CA**	**Washington, DC**
Orlando, FL	**Chicago, IL**	**Boston, MA**
Dallas, TX	**Sydney, Australia**	**Toronto, Canada**
Aylesburry, England	**Taipei, Taiwan**	**Hong Kong**
Tel Aviv, Israel	**Tokyo, Japan**	**Seoul, South Korea**
Singapore	**Solna, Sweden**	**Munich, West Germany**

Independent Design Centers:
Lowell, MA (Custom Silicon Inc.)
Research Triangle Park, NC (Integrated Silicon Systems)
(See also the distributors Hamilton/Avnet, Schweber Electronics, Hall-Mark Electronics, and Wyle Laboratories)

All centers have dial-up communications at up to 10 kbps or datacomm network at up to 2,400 bps. Design centers offer Daisy or Mentor workstations plus a high-speed link to Motorola's mainframe computer for verification and release.

National Semiconductor Corp.
2900 Semiconductor Dr.
Santa Clara, CA 95052

Tom Wong
Strategic Marketing Manager
(408) 721-5884

Hong Kong, BCC: 2 engineers; Daisy, FutureNet; IBM terminal
Santa Clara, CA: 14 engineers; 3 VAX-11/780s, Daisy, Mentor, FutureNet; IBM terminal; 1 Tektronix graphics terminal
Tustin, CA: 3 engineers; MicroVAX, Daisy, FutureNet; 5 IBM terminals
London, England: 2 engineers; Daisy, FutureNet; IBM terminal
Reading, England: 5 enginers; VAX-11/780, 8600; 6 terminals
Paris, France: 2 engineers; Daisy, FutureNet; IBM terminal
Munich, West Germany: 6 engineers; Daisy, Valid, FutureNet; IBM terminal
Milan, Italy: 1 engineer; Daisy; IBM terminal
Tokyo, Japan: 4 engineers; VAX-11/785; 6 terminals
Boston, MA: 4 engineers; Daisy, FutureNet; IBM terminal
Bloomington, MN: 3 engineers; MicroVAX II; 5 terminals
Stockholm, Sweden: 1 engineer; Daisy; IBM terminal
Richardson, TX: 3 engineers; MicroVAX II; 4 terminals
Taiwan and South Korea (third party)
(See also the distributor Hamilton/Avnet)

Communications exist via a dedicated SNA network at 14.4 kbaud. Three- to five-day workstation-based training is tailored to the user's experience, with several instructors for up to six students per session. Training manuals and free use of an individual workstation and mainframe are included. National offers extensive consulting for customers doing joint design and accepts turnkey designs (circuit schematic as input). It holds a one-week course on the DA4 (VMS/Unix) design automation system, a one-day class on Aspect gate arrays, and a two-day ECL hardware design course, with complete documentation.

NCM Corp.
1500 Wyatt Dr.
Santa Clara, CA 95054

(408) 496-0290

Santa Clara, CA: 3 engineers; Silicon Graphics 3030; Silicon Graphics and Televideo terminals

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NCR Microelectronics
2001 Danfield Ct.
Fort Collins, CO 80525

Lyle Wallis
Commercial ASICs
Earl Reinkensmeyer
Software Products
(303) 226-9500
(800) 334-5454

NCR Microelectronics
1635 Aeroplaza Dr.
Colorado Springs, CO 80916

Ted Lunacek
Military ASICs
Michael Moursi
Automotive ASICs
(719) 596-5795
(800) 525-2252

Arcadia, CA (NAVAsys ASIC Design Services): 3 engineers; 3 Daisy
Calabas, CA (Guidon, McLean and Easton): 3 engineers; 2 Daisy
Laguna Hills, CA (Micronix): 5 engineers; 4 Mentor Graphics
Santa Clara, CA (NCR) 2 engineers; 2 Mentor, 2 Daisy
Boulder, CO (Design Engineering Inc.): 4 engineers; 3 Daisy, 1 Mentor
Breckinridge, CO (VLSI Microsystems Inc.): 4 engineers; 2 Daisy
Colorado Springs, CO (NCR): 7 engineers; 10 Mentor, 4 Daisy, 1 VAX 8700, 1 VAX 785
Orlando, FL (Micro Devices): 4 engineers; 3 Mentor
Roswell, GA (Design Engineering Inc.): 2 engineers; 2 Mentor
Munich, West Germany (NCR): 2 engineers; 2 Mentor
Kawasaki City, Japan (Japan Macnics Corp.): 2 engineers; 1 Mentor
Lowell, MA (Custom Silicon Inc.): 11 engineers; 5 Viewlogic, 4 Mentor, 2 FutureNet, 1 Daisy
Woburn, MA (NCR): 3 engineers; 2 Mentor
Farmington Hills, MI (Automotive Systems Laboratory Inc.): 4 engineers; 1 Mentor
Research Triangle Park, NC (Integrated Silicon Systems Inc.): 12 engineers; 3 Mentor, 2 FutureNet, 1 Daisy
Rochester, NY (RIT Research Corp.): 1 engineer; 1 Daisy
West Chester, PA (ASIC Designs Inc.): 1 engineer; 2 Daisy
El Paso, TX (Sherwood Design Center): 2 engineers; 1 Daisy
Plano, TX (Design Engineering Inc.): 2 engineers; 2 Mentor
Berkshire, UK (Manhattan Skyline): 2 engineers; 1 Daisy, 1 Mentor
Salt Lake City, UT (Systronix Inc.): 2 engineers; 1 Daisy
Bellevue, WA (ASIC Northwest): 1 engineer; Mentor

All NCR-affiliated design centers will perform turnkey design or support customers' designers in the design center. Some design centers will go into the customer's facility to assist with design; some will do system-level as well as device design. All regional NCR offices have FAEs available to assist customers with design planning and design support. Every month, NCR holds a three-day semicustom design training session at one of its facilities for customers who are new users. In addition, training on NCR software tools is available. Training will be scheduled off site if requested. For more information, call (303) 226-9500.

Nebula Corp.
33 Lyman St.
Westboro, MA 01581

Jim Gobes
Vice President, Sales
(508) 366-6558

Westboro, MA: 7 engineers; 1 MicroVAX, 1 Daisy, 4 PC ATs; fault simulation engine

Nebula is an independent design center that provides system-level semicustom design services using commercially available CAE tools. Its engineers can work at the customer's site or can provide full turnkey solutions, working with and producing designs for the ASIC vendor of the customer's choice. Nebula offers a free "solution evaluation" of customer systems that includes system partitioning; CAE tool strategy; and selection of vendors that meet the technology, packaging, and cost criteria. Customization of customer-owned CAE tools and fault grading services for any design also are provided.

NEC Electronics
401 Ellis St.
P.O. Box 7241
Mountain View, CA 94039

Grant Hulse
Strategic Marketing Manager
(415) 965-6333

Santa Ana, CA	**Mountain View, CA**
Natick, MA	**Raleigh, NC**
Portland, OR	**Dallas, TX**
Chicago, IL	

All of the locations above have major engineering workstations and VAX machines networked with the Mountain View, CA, NEC computer center via 9.6- to 48-kbps communications . Design training is available as requested by the customer, with one instructor per student and one student per workstation. Workstation manuals, data sheets, design manuals, block library, and EWS design kits are included with the hands-on training. Additionally, NEC provides seminars and technical presentations.

Oki Semiconductor Inc.
785 North Mary Ave.,
Sunnyvale, CA 94086

Clifford Vaughan
ASIC Marketing Manager
(408) 720-1900

Sunnyvale, CA: 30 engineers; 5 Daisy, 2 Mentor, Valid, FutureNet, Sun, VAX, IBM, Amdahl; 20 terminals networked to mainframe
Stoneham, MA: 3 engineers; Daisy, Mentor, Sun, VAX; 2 terminals networked to mainframe in Sunnyvale

Dial-up link at 9,600 baud. Direct satelite link between design centers and manufacturing sites. Design training and hands-on workstation instruction available at all design centers.

Ontario Research Foundation
Microelectronics Development Centre
Systems Engineering
2395 Speakman Dr.
Mississauga, Ontario
Canada L5K 1B3

John Paterson
Marketing Manager
(416) 822-4111

Toronto, Ontario: 5 engineers; 5 Mentor, 1 PC AT; 2 terminals

Dial-up lines are available at 300, 1,200, and 2,400 baud. Training is provided on a one-to-one basis to client engineers, with one workstation for the client. Group sessions also are provided to a group of six or eight engineers, with two instructors for the group and two engineers to a workstation. The center offers turnkey design services or facility rental. It supports more than a dozen foundries and maintains a generic cell library that is convertible to foundry specifications. Digital, analog, and analog/digital ICs are supported.

Panasonic Industrial Co.
1610 McCandless Dr.
Milpitas, CA 95035

Terry Toyooka
Resident Engineer
(408) 946-4311

San Jose, CA: 3 engineers; 2 Daisy Logicians, 2 Mentor Idea 1000s, 1 VAX

Pioneer Technologies Group
9100 Gaither Rd.
Gaithersburg, MD 20877

R. F. Hammett
Vice President, Systems Marketing
(301) 921-0660

Gaithersburg, MD: 2 engineers; 1 VAX, 1 Mentor

Design center for Plessey and National Semiconductor product lines.

Plessey Semiconductor
1500 Green Hills Rd.
Scotts Valley, CA 95066

Phillip Pollok
Director of Marketing
(408) 438-2900

Santa Clara, CA: 2 engineers; 1 MicroVAX II; 6 terminals
Scotts Valley, CA: 25 engineers; 1 VAX-11/780, 1 VAX-11/730, 30 terminals; 2 MicroVAX IIs, 10 terminals; 2 Emerald VLSI Design Stations, 3 Mentor, 1 Calma GDS II system, 2 Analog Design Tool Stations (Sun), 4 IBM PC ATs
Encinitas, CA (Analog Solutions): 1 engineer; 1 IBM PC XT
Ottawa, Ontario (Ontario Centre for Microelectronics): 10 engineers; 3 Mentor, 8 Valid, 10 IBM PC ATs
Toronto, Ontario (Microelectronics Development Centre): 4 engineers; 4 Mentors, 1 PC AT;
Boulder, CO (Analog Solutions): 1 engineer; 1 PC AT
North Palm Beach, FL (Silicon Beach Enterprises): 2 engineers; 3 PC ATs
Boston, MA: 2 engineers; 1 MicroVAX II; 6 terminals
Timonium, MD (Microcom): 7 engineers; 7 PC ATs
Marlton, NJ: 2 engineers; 1 MicroVAX II; 6 terminals
Dallas, TX: 2 engineers; 1 MicroVAX II; 6 terminals
(See also the distributor Pioneer)

Communications are provided via a 1,200-baud Tymnet connection for all technology centers. All Plessey technology centers offer 2- to 5-day hands-on training courses tailored to the experience level of the students. The courses cover gate array and cell-based design methodologies using PDS2 and Megacell layout editor software. CLA5000 and Megacell design manuals are included. Ratios are six students for one instructor and one student per terminal. Additional services include feasibility studies, product definition, design engineering support, packaging, and test and evaluation support. Workstation support is offered for MicroVAX, Daisy, Mentor, Valid, FutureNet and Tektronix CAE. Full training is offered at Scotts Valley. There are also full CAD and design manuals available for training.

Schweber Electronics Corp.
CB 1032 Jericho Tpk.
Westbury, NY 11590

Mimi Shokraie
Technical Marketing Business Manager
(516) 334-7555

Irvine, CA **San Jose, CA**
Norcross, GA **Bedford, MA**

Schweber has over 50 man-years of semicustom design experience. It offers leading logic consolidation products and services supporting VLSI Technology, Motorola, Altera, AMD/MMI, TI, and Signetics. Centers are equipped with Mentor Graphics (DN3000/DN4000) and Sun-3/260 workstations. The company specializes in design consulting, equipment leasing, and 24-hour design center accessibility.

Semiconductor Specialists Inc.
195 Spangler Ave.
Elmhurst, IL 60126

P. Jeffrey Carroll
Director of Marketing
(312) 279-1000

West Drayton, UK (Semiconductor Specialists [UK] Ltd.): 2 engineers

The London-area design center handles the ASIC product lines of Plessey Semiconductor, Siliconix, Raytheon Semiconductor, and Ferranti.

Sierra Semiconductor Corp.
2075 N. Capitol Ave.
San Jose, CA 95132

Don MacLennan
Director, Custom Marketing
(408) 263-9300

San Jose, CA: 21 engineers; 2 Valid, 10 Apollos, 1 Daisy, 3 Mentor; 22 AED terminals connected to Elxsi, 2 Sun terminals
Burlington, MA: 1 engineer; 1 Apollo
Oakbrook, IL: 1 engineer; 1 Apollo
's-Hertogenbosch, the Netherlands: 7 engineers; 1 Mentor, 1 Daisy; 4 AED terminals connected to a VAX 8650

Communications are via 1,200-baud dial-up lines. Individual training is available at all design centers. Each student has a workstation for his exclusive use during design training. Sierra offers custom cell design, custom consulting, and system consulting, particularly in analog and EEPROM design.

Siliconix Inc.
2201 Laurelwood Rd.
Santa Clara, CA 95054

Joe Baranowski
IC Marketing Manager
(800) 554-5565 x1900

Santa Clara, CA: 10 engineers; 1 VAX-11/780, 5 Daisy, 3 Mentor, 5 FutureNet; 15 terminals
Boston, MA: 2 engineers; 1 FutureNet, 1 Daisy Personal Logician
Swansea, Wales: 8 engineers; 1 VAX-11/780, IBM, FutureNet, 2 Daisy; 7 terminals
Hong Kong: 2 engineers; 4 Daisy; 4 terminals
Munich, West Germany: 2 engineers; FutureNet, Daisy; 3 terminals
(See also the distributor Pioneer)

Communications are available via 1,200-baud modem links. Training is given one on one for customers, who also are allowed free use of the facilities. Manuals on cell libraries, design, and workstations are provided. Software, now available on a time-shared basis, uses the GE network.

Silicon West Inc.
5470 Anaheim Rd.
Long Beach, CA 90815

Edward Evans
President
(213) 494-4588

Signal Hill, CA: 6 engineers; 1 VAX, 2 Apollos, 2 PC/XTs

Communications are via a 1,200-baud modem. Special training classes are available only by customer request. Special custom cells will be designed at the customer's request.

Sipex Corp.
Data Linear Division
491 Fariview Way
Milpitas, CA 95035

Valentino Liva
ASIC Marketing and Applications
(408) 945-9080

Milpitas, CA: 11 engineers; VAX, MicroVAX, IBM PCs, complete Daisy CAE/CAD systems (Chipmasters and Personal Logicians for schematic capture)
Paris, France: 1 engineer; 1 Daisy, ADT

Dial-up communications are available at 2,400 baud. One-on-one instruction is used for semicustom analog training in dielectric isolation technology. Design manuals are available. The company provides one workstation per student.

SIS Microelectronics Inc.
1500 Kansas Ave., Bldg. 1D
PO Box 1432
Longmont, CO 80502

William D. Burkard
President
(303) 776-1667

Longmont, CO: 2 DN570 Turbos (one with Mentor software), 1 DN4000, 1 DN3500, 3 DN3000, 1 DN660 (with Mentor software); Ikos simulation system; complete VLSI Technology Inc. design system, FutureNet design system, Mentor; 7 IBM PC data entry stations

SIS is a VLSI Technology authorized design center (ADC), with training provided by VLSI Technology. SIS specializes in system-level design support that includes multichip and mixed-technology implementations. In addition to the VLSI Technology design system, SIS has developed proprietary software interfaces to FutureNet and Mentor TTL libraries, as well as PALASM and ABEL translators for PAL equations.

S-MOS Systems Inc.
2460 N. First St.
San Jose, CA 95131

Joel Silverman
Director of Marketing
(408) 922-0200

San Jose, CA: 15 engineers; IBM PC, Mentor, Daisy, IBM and VAX mainframes; 6 terminals
Boston, MA: 1 engineer; PC AT
Baltimore, MD (Dibec)

Types of communications available are dial-up and dedicated lines with SNA, RJE, and asynchronous protocols at 1,200 to 9,600 baud. Classes are three days for inexperienced users; otherwise, training is done by students on their own workstations under the guidance of one instructor per student. Training also includes user's guides. Each design center has provision for secure areas.

Standard Microsystems Corp.
35 Marcus Blvd.
Hauppauge, NY 11788

Brian Cayton
Director of Marketing
(516) 273-3100

Campbell, CA (VLSI Design Associates): 11 engineers; 2 Mentor, 3 Calma, 1 VAX; 6 terminals
Irvine, CA (Turk Enterprises): 2 engineers; 2 Viewlogic (IBM PC)
Nashua, NH: 2 engineers; 2 Viewlogic (IBM PC)
Hauppauge, NY: 27 engineers; 3 Mentor, 3 Daisy, 2 Valid, 11 Metheus-CV, 4 VAX-11/785s, 18 Viewlogic (IBM PC); 25 terminals
Lewisville, TX (Mike McConnell & Assoc.): 2 engineers; 2 Viewlogic (IBM PC)
Paris, France (Maxcell): 7 engineers; 2 Daisy Megalogician, 3 Personal Logicians
Munich, West Germany: 2 engineers; 2 Viewlogic (IBM PC)
Solna, Sweden (Naxab): 3 engineers; Daisy

SMC offers both 3- and 5-day training courses that cover the use of the library, software tools, and supercells. The courses are available on an as-needed basis, and manuals following the course work and giving details on all tools, hardware, and cell performance are provided. Typically, there is one instructor and one workstation for each two students.

Tachonics Corp.
107 Morgan Lane
Plainsboro, NJ 08536

Michael Zyla
Marketing Manager
(609) 275-2504

Plainsboro, NJ: 6 engineers; 3 Mentor, 3 VLSI Technology

The company offers a one- and a two-day seminar on the use of standard-cell libraries at customers' locations and at Tachonics' headquarters. The course includes design manuals. Extensive consultation with MMIC, analog, and digital designers is available, which is especially important for designs based on the company's mixed-mode analog and digital cell libraries. Circuit design and logic design capability is offered, in addition to basic standard-cell placement, routing, and fabrication.

Texas Instruments Inc.
8390 LBJ Expwy.
P.O. Box 655303, M/S 3670
Dallas, TX 75265

Jerry Koontz
ASIC Marketing Communications Manager
(214) 997-2031

All design centers have Daisy and Mentor workstations and IBM 3279s.

Santa Clara, CA	**Irvine, CA**	**Atlanta, GA**
Chicago, IL	**Boston, MA**	**Dallas, TX**
Ottawa, Ontario	**Bedford, England**	**Paris, France**
Hanover, West Germany	**Milan, Italy**	**Rieti, Italy**
Stockholm, Sweden	**Tokyo, Japan**	**Hong Kong**

(See also the distributors Arrow and Wyle)

TI provides both evaluation and design assistance to its customers. A one-day workshop for designers familiar with basic workstation operation is offered and focuses on such aspects of design as partitioning, designing for testability, optimizing performance, analyzing power/ground pin requirements, and guidelines for simulation and test pattern generation. The course can be modified for special customer needs on site. The design staff is available for project-oriented consultation on topics like library installation, design partitioning, and project planning. TI provides a hot line and on-location help for work on in-house CAE equipment. The staff also performs turnkey and special design projects, such as design translations, schematic capture, test pattern generation, and fault grading. Selected centers provide clients who lack workstations secure use of either Daisy Megalogician or Apollo DN660 workstations. These centers offer advanced capabilities that include local design layout and preparation of postlayout delay and back annotation data files.

Toshiba America Inc.
1220 Midas Way
Sunnyvale, CA 94086

Allan Cox
Director Marketing
Semicustom Products, MOS IC Division
(408) 733-3223

Redhill, CA: 2–5 engineers; FutureNet, Viewlogic; 4 terminals
Sunnyvale, CA: 16 engineers; Daisy, Mentor, FutureNet, Aida, HP, Valid, Viewlogic; 18 terminals
Atlanta, GA: 2–5 engineers; FutureNet, Viewlogic; 6 terminals
Boston, MA: 9 engineers; Daisy, Mentor, Valid, FutureNet, Viewlogic; 12 terminals and a mainframe
Dallas, TX: 4 engineers; Daisy, FutureNet, Mentor, Viewlogic; Ikos; 6 terminals

Communications are via high-speed dedicated lines. Training is included with the design contract on a one-to-one basis. Design manuals and cell library are provided. Services range from specification, netlist extraction, and simulation to design libraries.

TriQuint Semiconductor Inc.
PO 4935, Group 700
Beaverton, OR 97075

Louis Pengue
Product Marketing Manager
(503) 644-3535

Beaverton, OR: 15 engineers; Daisy, Mentor; MicroVAX engineering design network

The company offers one-on-one instruction for designing GaAs gate arrays and standard-cell devices. Custom and semicustom design classes with actual fabrication of customers' designs are available. Also avaialble are evaluation kits for prototype development, using TriQuint standard components and semicustom or full-custom devices.

Unicorn Microelectronics Corp.
99 Tasman Dr.
San Jose, CA 95134

H. Y. Liu
Sales Manager
(408) 433-3388

United Silicon Structures (US2)
1971 Concourse Dr.
San Jose, CA 95131

Steven Eliscu
Product Marketing
(408) 435-1366

San Jose, CA: 5 engineers; Sun, Apollo, DEC, PC; 10 terminals
San Jose, CA (ATS)
San Jose, CA (CIT)
Los Angeles, CA (SDC)
Seattle, WA (ANW)

Courses are offered in Solo design, design methodology, and design for testability. A set of manuals is provided with each course. The ratio of instructors to students is 1:4, and the ratio of workstations to students is 1:1. US2 can create fully customized cells to meet specific requirements and can provide turnkey design services.

United Technologies
Microelectronics Center
1575 Garden of the Gods Rd.
Colorado Springs, CO 80907

Ronald Hehr
Manager, Semicustom Products
(719) 594-8124
(800) MIL-UTMC x8124

Laguna Hills, CA: 2 engineers; 1 MicroVAX, 3 IBM PCs running Valid; 5 terminals
Waltham, MA: 2 engineers; 1 MicroVAX, 3 IBM PCs running Valid; 5 terminals

UTMC has dial-up lines and a 9600-baud dedicated line to its factory. Training is given on an individual basis at the design centers. Access to a Zycad simulation accelerator is provided through a dedicated line to the factory.

Vitesse Semiconductor Corp.
741 Calle Plano
Camarillo, CA 93010

Joe Welsh
ASIC Product Marketing Manager
(805) 388-3700

Greenbelt, MD (Atlantic)

For information, contact Atlantic, (301) 220-1501.

VLSI Technology Inc.
1109 McKay Dr.
San Jose, CA 95131

Peter Bagnall
Vice President, ASIC Marketing
(408) 434-3000

Santa Ana, CA: 2 engineers; 5 computers/workstations
San Jose, CA: 26 engineers; 46 computers/workstations
Canada (Microtel Pacific Research)
Longmont, CO (SIS)
Ft. Lauderdale, FL: 2 engineers; 5 computers/workstations
Chicago, IL: 2 engineers; 5 computers/workstations
Boston, MA: 12 engineers; 18 computers/workstations
South Portland, ME (Qadic Systems Inc.)
Princeton, NJ: 4 engineers; 8 computers/workstations
Dallas, TX: 5 engineers; 9 computers/workstations
King of Prussia, PA (Integrated Circuit Systems Inc.)
London, England: 2 engineers; 4 computers/ workstations
Paris, France: 3 engineers; 6 computers/workstations
High Wycombe Bucks, Ireland (Axiom Electronics Ltd.)
Tokyo, Japan: 6 engineers; 9 computers/workstations
Soina, Sweden (Nordisk Arraytekuik AB)
Munich, West Germany: 10 engineers; 18 computers/workstations

Communications is via dedicated lines at 9,600 baud for small centers (fewer than 6 engineers) and satellilte links at 50 kbaud for large centers (6 engineers or more). For the training, there are 10 students per instructor and one workstation per student; courses on VLSI design methodology and the use of the company's tool set are offered. Additionally, computing resources, physical design, and system partitioning are available.

VTC Inc.
2401 E. 86 St.
Bloomington, MN 55425

Gary Heyes
ASIC Product Manager
(800) VTC-ASIC

Phoenix, AZ (Circuit Design Group)
Laguna Hills, CA (Micronix): 5 engineers; 3 Mentor, 3 PC/XTs; 5 terminals
South Portland, ME (Quadic Systems): 6 engineers; 3 Metheus-CV 3721E, 2 PC-based systems
Kanata, Ontario (Calmos Systems): 10 engineers; 3 Valid; 6 terminals

Calmos trains on an individual basis with the charge built into the cost of the design; otherwise, the fee is $500 per day for consulting. Quadic has the manuals for the standard-cell package data sheets; it costs about $200 for the digital standard-cell library.

Wyle Laboratories
Electronics Marketing Group
18910 Teller Ave.
Irvine, CA 92715

Rick Timmins
Vice President of Semicustom ICs
(714) 851-9953 or (408) 727-2500

Calabassas, CA: 1 engineer; Daisy Personal Logician, MicroVAX, FutureNet, Altera
Irvine, CA: 5 engineers; Daisy MegaLogician, 3 Personal Logicians, MicroVAX, FutureNet, Altera; Ikos
San Diego, CA: 1 engineer; Daisy Personal Logician, MicroVAX, FutureNet, Altera
Santa Clara, CA: 5 engineers; Daisy MegaLogician, 3 Personal Logicians, MicroVAX, FutureNet, Altera; Ikos
Denver, CO: 3 engineers; Daisy MegaLogician, 3 Personal Logicians, MicroVAX, FutureNet, Altera
Portland, OR: 1 engineer; Daisy Logician, MicroVAX, FutureNet, Altera
Dallas, TX: 1 engineer; Daisy Personal Logicians, MicroVAX, FutureNet, Altera

All 13 Wyle locations have direct lines to LSI Logic's mainframe. Wyle also handles the ASIC products of Texas Instruments, LSI Logic, and Motorola as well as the programmable logic families of Altera, Intel, Signetics/Philips, Advanced Micro Devices, and TI. The Irvine, Santa Clara, and Denver facilities include PLD design, programming, and text centers. Wyle provides the LSI Logic, Motorola, and Texas Instruments libraries and design software and has franchises for Daisy, FutureNet, and Ikos design systems. All of the centers except for Santa Clara and San Fernando (Calabasas) have 24-hour customer access.

Xerox Microelectronics Center
701 S. Aviation Blvd.
El Segundo, CA 90245

Gary Petrov
Manager, Regional Design Support Centers
(213) 333-7701

El Segundo, CA: 3 engineers; 5 Xerox 6085s, 1 Sun; Ikos
Santa Clara, CA: 2 engineers; 5 Xerox 6085s, 1 Sun; Ikos
Webster, NY: 3 engineers; 5 Xerox 6085s, 1 Sun; Ikos
Dallas, TX: 2 engineers; 5 Xerox 6085s, 1 Sun
Welwyn Garden City, UK: 1 engineer; 5 Xerox 6085s, 1 Sun; Ikos

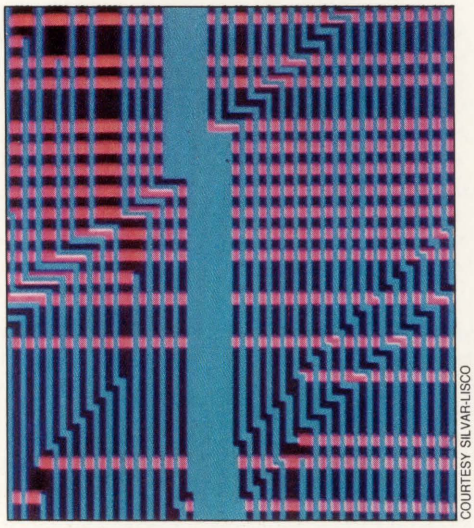
Dial-up and Ethernet communications are available at 9,600 baud. Two-day semicustom design course are available, with design and CAD manuals. The ratio of instructors to students is 1:4, and the ratio of workstations to students is 1:2. Additional services include fault grading, design assessments, design services from block diagrams, access to the mainframe in California, and fabrication support.

ZyMOS Corp.
477 N. Mathilda Ave.
Sunnyvale, CA 94088

Vic Pasini
Tactical Marketing Director
(408) 730-5400

ZyMOS is concentrating on higher levels of microprocessor peripheral integration targeting the 80X86 series of peripheral circuits.

IV REFERENCES



COURTESY SILVAR-LISCO

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PRELIMINARY
DEVICE SPECIFICATION

AMCC®

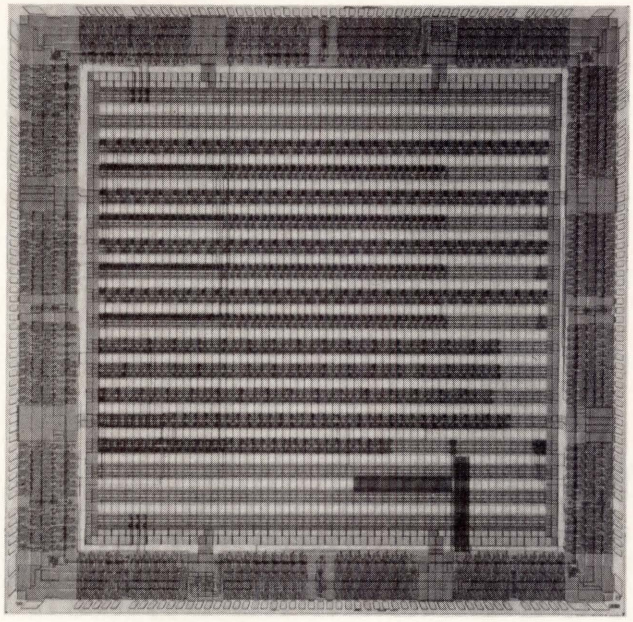
Q14000 SERIES BiCMOS LOGIC ARRAYS

DESCRIPTION

The AMCC Q14000 Series of BiCMOS logic arrays is presently comprised of two products with densities of 2160 and 9072 equivalent gates, respectively. The series is optimized to provide CMOS densities with bipolar performance for today's sophisticated semicustom applications.

The Q14000 Series combines 1.5-micron CMOS features with an advanced 1.5-micron oxide-isolated bipolar process on a single silicon chip. The BiCMOS process uses an N-type epitaxial layer as the foundation for both the NPN bipolar and CMOS devices. The CMOS transistors are used for logic implementation only and therefore utilize devices sized smaller than those required for a pure CMOS array. Because there are no large metal interconnects to drive, the high intrinsic speed and low power advantages of CMOS are preserved even as the densities are increased.

Bipolar totem-pole device pairs are used to provide the needed drive capability between logic cells. In addition, bipolar I/O cells provide an interface to ECL 10K, ECL 100K, TTL or mixed ECL/TTL systems.



PERFORMANCE SUMMARY	
PARAMETER	VALUE
Typical internal gate delay	
1 load, no metal	.61 ns
2 loads, 2mm of metal	.70 ns
Typical internal F/F toggle frequency	240 MHz
Typical input delay	
ECL–	2.2 ns
TTL–	4.0 ns
Typical output delay	
ECL–	1.2 ns
TTL–(15 pf)	4.0 ns
ECL compatible output drive	25 Ω, 50 Ω
TTL compatible output drive	20 mA
Average cell utilization	95%

TABLE 1

An extensive library of SSI and MSI logic macros is available in conjunction with AMCC's MacroMatrix® design kit. MacroMatrix is available for use in conjunction with most popular engineering workstations (EWS).

FEATURES

- 1.5-Micron Mixed Bipolar/CMOS Technology
- 2160 and 9072 Equivalent Gates
- Speed/Power Programmable I/O Macros
- ECL, TTL, or Mixed ECL/TTL
- Full Military Screening Available
- Operate over −55°C Ambient to +125°C Case

PRODUCT SUMMARY		
DESCRIPTION	Q2100B	Q9100B
Equivalent gates	2160	9072
Internal logic cells	540	2268
I/O pads	80	160
Fixed power/ground pads	28	56
Total pads	108	216
Typical power[1]	1.8 W	4.0 W

TABLE 2

NOTES:

1 4.5 Volts supply @ 25°C, 50% inputs/50% outputs; 40 MHz with 20% of internal gates switching.

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Q14000 SERIES ARRAY ORGANIZATION

BICMOS PROCESS CROSS SECTION

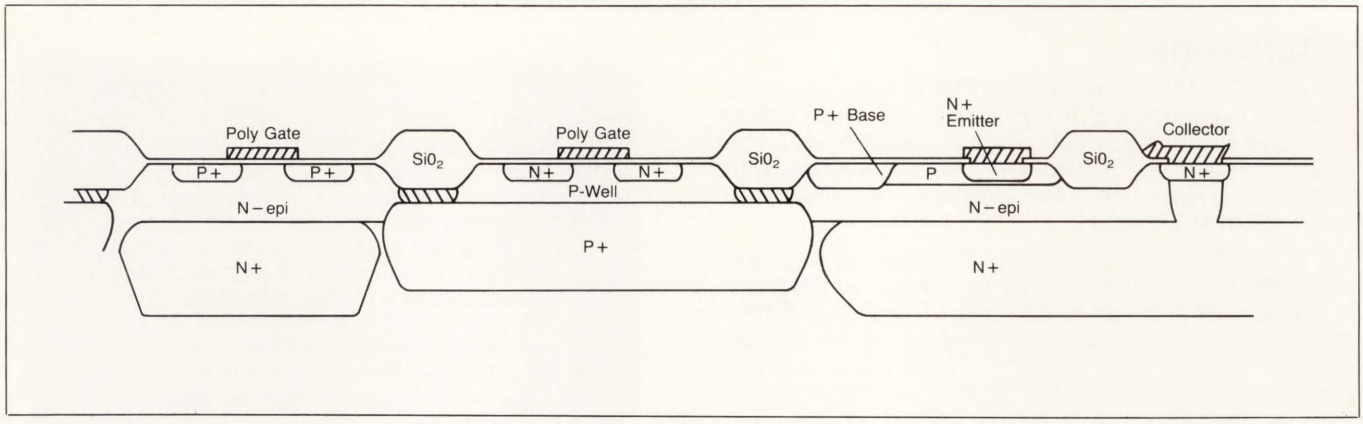


FIGURE 1

ARRAY ARCHITECTURE

The Q14000 Series logic arrays are comprised of repeated structures, or logic cells, containing bipolar and CMOS transistors and resistors. Macros, which serve as the basic elements for logic design, are built by the interconnection of the components contained in one or more cells.

The Q14000 Series arrays employ two types of cells – logic and I/O, along with overhead circuitry such as voltage references and voltage regulators. While the overhead circuitry is predefined by AMCC, I/O and logic functions which can be assigned to uncommitted cells are found in the Q14000 Series macro library.

I/O cells are located around the perimeter of each array. On three sides of the array, the I/O cells can be used to implement unidirectional input or output interfaces. I/O cells, found on the remaining side of the die, can perform bidirectional or unidirectional I/O functions. All I/O cells can implement ECL 10K, ECL 100K or TTL interfaces.

BiCMOS 2-INPUT NAND

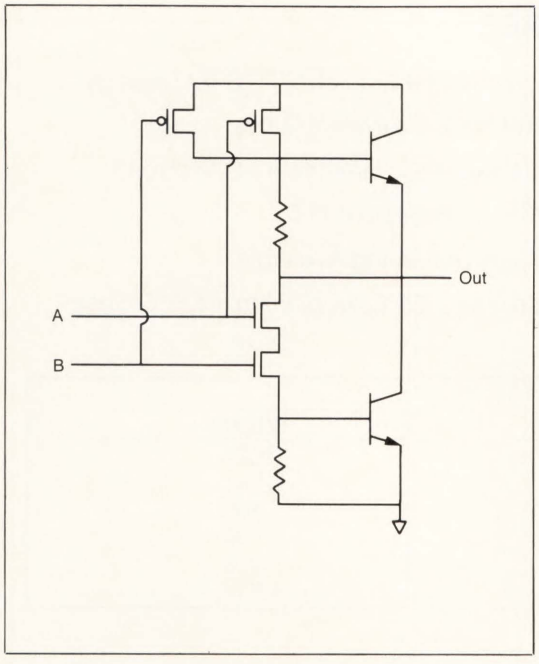


FIGURE 2

Q9100B DIE LAYOUT

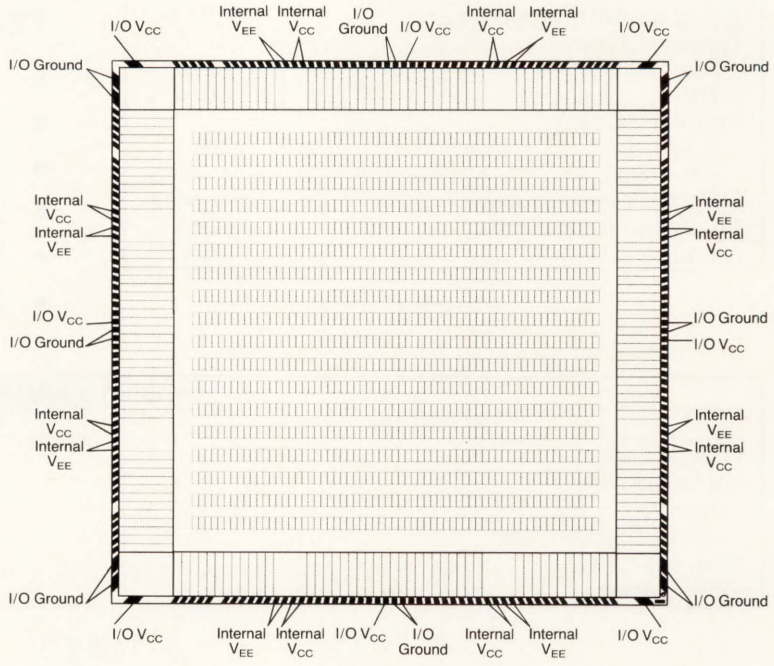
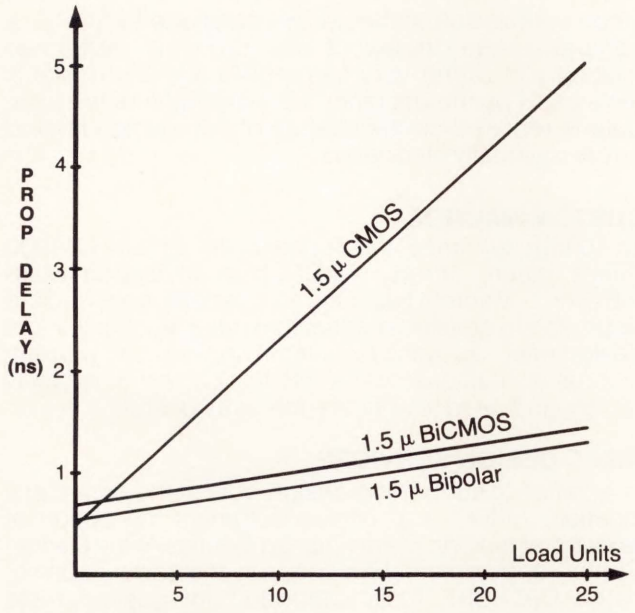


FIGURE 3

BICMOS CELL STRUCTURE

The Q14000 Series basic cell utilizes both CMOS and bipolar devices. The CMOS devices are used for logic implementation while the bipolar devices provide the necessary drive capability. The performance of an internal macro is directly related to the drive, or K-factor, associated with the macro. Since the bipolar transistors used in the Q14000 Series basic cell yield K-factors 5 to 10 times lower than those of comparable CMOS transistors, BiCMOS macros experience minimum performance degradation as fanout loads are increased.

FANOUT DEGRADATION COMPARISON



Typical Delay of 2-input NOR Gate as Function of Loading

FIGURE 4

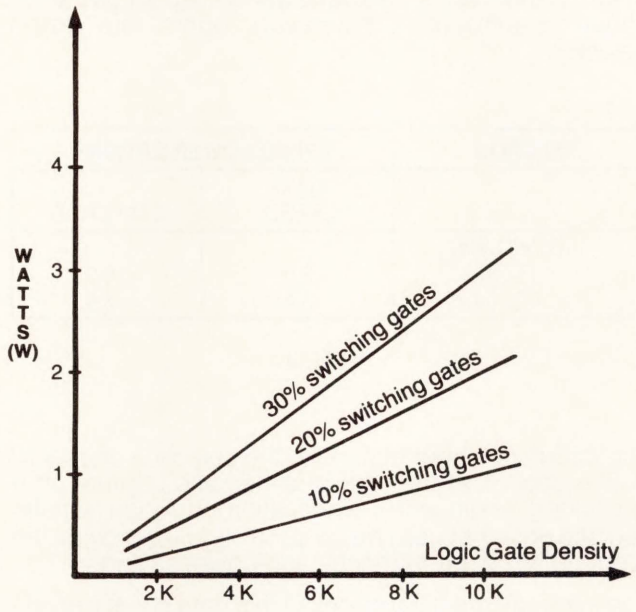
POWER CONSIDERATIONS

AMCC's Q14000 Series arrays have the optimum combination for high performance while maintaining low power dissipation. The power consumption of the internal core of a BiCMOS array is directly proportional to the number of gates switching simultaneously during a clock cycle and the operating frequency. Internal power consumption for Q14000 Series BiCMOS arrays is approximately 20 μW/gate-MHz for active gates switching during the clock cycle. The core area consumes no DC power. Figure 5 plots internal power versus the percentage of simultaneously switching gates.

I/O cell power is determined by the interface mode selected and the particular macro selected. Power consumption for representative I/O macros is defined in the ECL and TTL Interface sections of this data sheet.

The total power dissipation for a Q14000 Series array is given by: Total Power = core power + I/O power + overhead power where the overhead power is associated with the internal reference voltage generators and is specified in the Q14000 Series Design Manual.

TYPICAL CORE POWER DISSIPATION AT 50 MHZ



Internal Power as Functions of Logic Gate Density and Percentage of Simultaneously Switching Gates
(Clock Freq. = 50 MHz)

FIGURE 5

PACKAGING

The Q14000 Series logic arrays are available in a range of standard packages including surface-mountable chip carriers and pin grid arrays. For complete details consult the AMCC Packaging Guide.

PACKAGE	Q2100B	Q9100B
68 pin PGA	•	
84 pin LDFP	•	
84 pin PGA	•	
100 pin LDCC	•	
100 pin PGA	•	
132 pin LDCC		•
196 pin LDCC		•
224 pin PGA		•

TABLE 3

LDCC – Leaded Chip Carrier
LDFP – Leaded Flat Pack
PGA – Pin Grid Array

HIGH SPEED/LOW POWER MACROS

The Q14000 Series macro library offers maximum flexibility in the optimization of circuit performance and power consumption. I/O macros are offered with standard and high-speed options. The high speed options require somewhat more power than standard, but provide a significant improvement in performance.

Table 4 illustrates the effects of speed/power selections on I/O pair delays. As the table indicates the overall macro performance versus power consumption can be varied significantly depending upon the option selected.

MACROS	SPEED/POWER OPTIONS	
	HIGH SPEED	STANDARD
I/O Pair Delay		
TTL (ns)	8.0	10.0
ECL (ns)	3.4	3.9

TABLE 4

The circuit designer can make the selection of speed/power options at the time of schematic capture on a supported engineering workstation. Through simulation, the designer can fine-tune the circuit to provide the required mix of performance and power savings.

The interface macro sections of this data sheet provide additional information on speed/power trade-offs.

FLEXIBLE I/O STRUCTURE

The Q14000 Series I/O cells are configurable to provide a wide range of interface options.

INPUT	BI-DIRECTIONAL	OUTPUT
TTL	TTL transceiver	TTL totem pole
ECL 10K	ECL 10K transceiver	TTL 3-state
ECL 100K	ECL 100K transceiver	TTL open collector
		ECL 10K
		ECL 100K

TABLE 5

The Q14000 Series arrays also offer the following special options to support unique interface requirements such as high speed and +5V, single-supply ECL and TTL I/O (see Table 4).

The mixed ECL/TTL capabilities allow the interface to both technologies on a single chip without the use of external translators.

The +5V single supply ECL allows a high-speed TTL system to be partitioned using multiple AMCC devices which provide ECL I/O speeds with TTL system compatibility.

DESIGN INTERFACE

AMCC has structured its circuit design interface to provide maximum flexibility without compromising design correctness. For implementations using an engineering workstation, AMCC provides MacroMatrix software. MacroMatrix works in conjunction with the popular, commercial workstations to provide the following capabilities:

- Schematic Capture
- Logic Simulation
- Pre-Layout Delay Estimation
- Array and Technology-Specific Rules Checks
- Estimated Power Computation
- Layout Netlist Generation
- Post-Layout Timing Verification

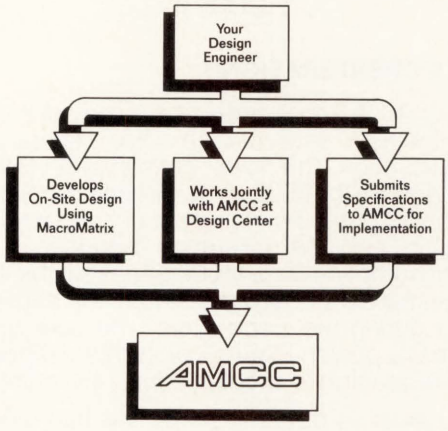
Upon submission of the design database to AMCC, a comprehensive review of the circuit is performed making use of the very same EWS and MacroMatrix tools used by the designer. No translation of the logic data is required so the chance of non design-related errors is virtually eliminated.

CUSTOM MACROS

To further enhance the functionality of the Q14000 Series macro library, AMCC has developed MacroEditor™. MacroEditor uses a correct-by-construction approach to develop macros that meet all the pertinent design rules. As individual circuit applications warrant, macros with unique characteristics can be developed rapidly and used to optimize the array design.

AMCC DESIGN SERVICES

In addition to supporting design work at the designer's location, AMCC also offers customers the option of working at the San Diego Design Center. At the Design Center, engineers have access to the same sophisticated CAD/CAE tools supported for customer-site designs plus direct contact with a dedicated applications engineer to assist with the array implementation.



AMCC also provides a number of additional support services including:

- Full Design Implementation Service
- Local and Factory Applications Engineering Support
- Comprehensive Training Courses
- Complete Design Documentation

ECL INTERFACE

The Q14000 Series BiCMOS arrays can interface to standard ECL 10K and ECL 100K levels. All ECL inputs are buffered and can enter the array from any I/O cell.

ECL outputs can leave the arrays from any I/O cell. Different configurations of the I/O cells provide for a 50 ohm or 25 ohm output drive. Some 50 ohm output macros incorporate simple logic functions within the I/O cell effectively providing added density. 25 ohm outputs require two I/O cells.

Bidirectional ECL operation is available using one-quarter of the available I/O cells. 20 and 40 ECL transceiver macros are located along one side of the Q2100B and Q9100B arrays, respectively.

I/O POWER SUPPLY CONFIGURATION

I/O	V_{EE}	V_{TTL}
ECL 100K	−4.2 to −4.8V	—
ECL 10K	−4.7 to −5.7V	—
ECL 100K/TTL	−4.2 to −4.8V	5V
ECL 10K/TTL	−4.7 to −5.7V	5V
TTL	—	5V
ECL/TTL Single Supply	4.5 to 5.5V	5V

TABLE 7

REPRESENTATIVE ECL INTERFACE MACROS

DESCRIPTION	CELLS	TYPICAL DELAY (ns)[1]		TYPICAL POWER (mW)[2]	
		STANDARD OPTIONS	HIGH SPEED OPTIONS	STANDARD OPTIONS	HIGH SPEED OPTIONS
ECL 10K/100K INPUTS					
Noninvert	1	2.7	2.2	9.7	12.6
2 input OR/NOR*					
ECL 10K/100K OUTPUTS					
2 input OR	1	1.2	—	28.4	—
25Ω Driver*	2	1.2	—	56.8	—
Bidirect	1	1.5	—	38.3	—

* Under development

TABLE 6

TTL INTERFACE

TTL signals can enter the Q14000 Series arrays from any I/O cell. Once on-chip, TTL signals are automatically converted to internal operating levels for logic operations.

Signals leaving the array are subjected to level translation in the I/O cell. Following this translation, TTL outputs are available in totem pole or 3-state configurations.

TTL and ECL I/O can be mixed on each array yielding four basic configurations: TTL-only, ECL-only, mixed ECL/TTL (dual supply) and mixed ECL/TTL (single supply). Power supply requirements for each mode of operation are shown in Table 7. Representative TTL and TTLMIX I/O configurations are summarized in Table 8.

One quarter of the I/O cells on each Q14000 Series array can be configured to allow bidirectional TTL operation. All bidirecctional I/O cells are located along a single side of each array.

REPRESENTATIVE TTL INTERFACE MACROS

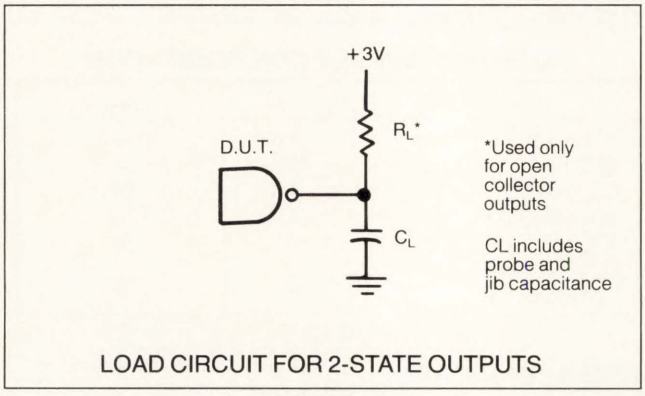
	DESCRIPTION	CELLS	TYPICAL DELAY (ns)[3]		TYPICAL POWER (mW)[4]	
			STANDARD OPTIONS	HIGH SPEED OPTIONS	STANDARD OPTIONS	HIGH SPEED OPTIONS
SINGLE SUPPLY	INPUTS					
	Non-Inverting	1	5.0	4.0	15.0	17.5
	OUTPUTS					
	2 input OR	1	5.0	4.0	10.5	17.0
	3-state	1	5.0	4.0	17.0	23.5
	Bi-directional*	1	5.0	4.0	32.0	41.0
DUAL SUPPLY	INPUTS					
	2 input OR/NOR	1	5.0	—	24.3	—
	OUTPUTS					
	2 input OR	1	5.0	—	26.4	—
	3-state	1	5.0	—	49.8	—
	Bi-directional*	1	5.0	—	71.0	—

*Under development

TABLE 8

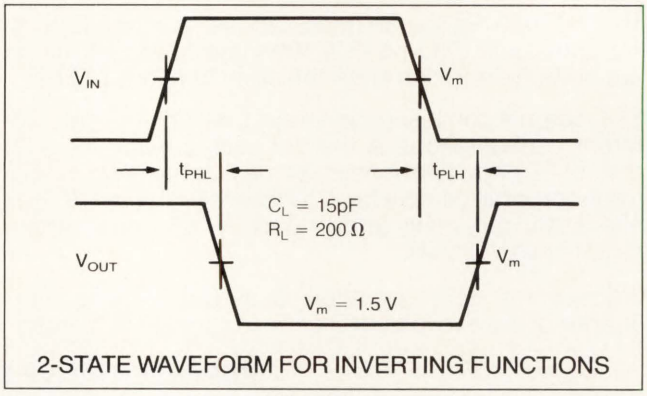
NOTES:
1 Prop Delays are for fastest path. $V_{EE} = -4.5V$. Inputs specified driving 3 load units, outputs specified driving 15 pf
2 At $V_{EE} = -4.5V$. Does not include I_{EOF}
3 Prop Delays are for fastest path. $V_{CC} = .5V$, $T_J = 25°C$. Inputs specified driving 3 load units, outputs specified driving 15 pf
4 At $V_{CC} = 5.0V$. Does not include I_{EOF}

Q14000 SERIES TTL TEST LOAD CIRCUITS



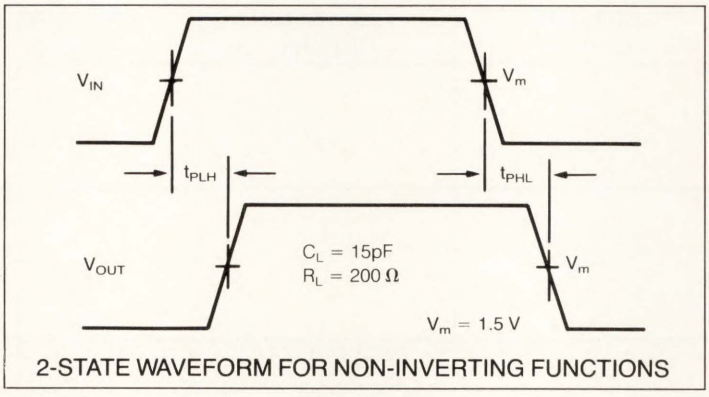
LOAD CIRCUIT FOR 2-STATE OUTPUTS

FIGURE 6



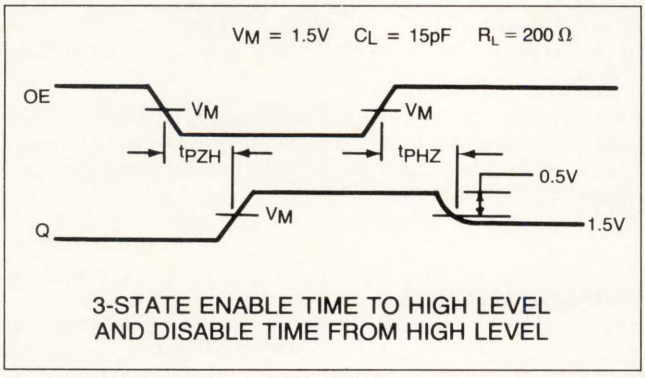
2-STATE WAVEFORM FOR INVERTING FUNCTIONS

FIGURE 7



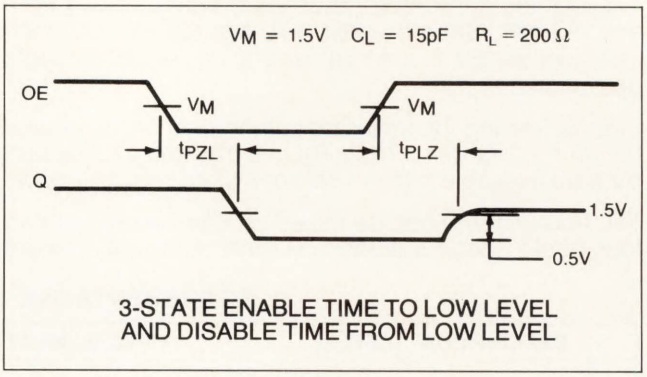
2-STATE WAVEFORM FOR NON-INVERTING FUNCTIONS

FIGURE 8



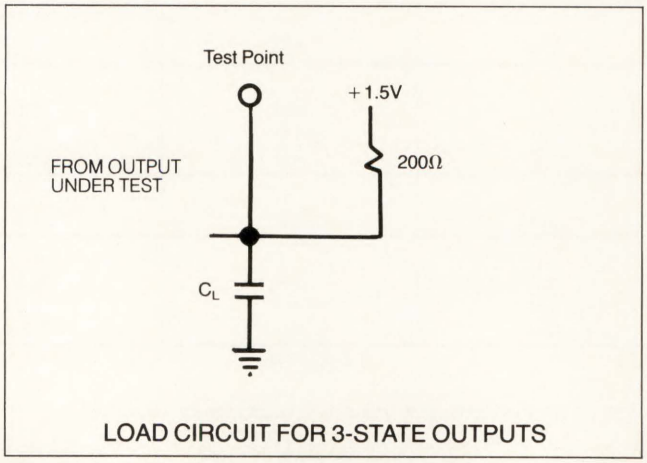
3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL

FIGURE 9



3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL

FIGURE 10



LOAD CIRCUIT FOR 3-STATE OUTPUTS

FIGURE 11

INTERNAL LOGIC CELL CAPABILITIES

The Q14000 Series internal logic cells are all identical in structure and are positioned in uniform columns across the arrays. Each cell contains 16 CMOS and 4 bipolar uncommitted transistors along with 4 resistors. The cells are individually configurable to provide a variety of logic functions through the use of the Q14000 Series macro library. The macro library provides SSI, MSI and some basic LSI functions. The higher level macros provide the advantages of higher speed, lower power and increased circuit density over a logically equivalent SSI macro implementation.

Table 9 lists parameters for a number of representative Q14000 Series internal macros.

REPRESENTATIVE INTERNAL MACROS

DESCRIPTION	NUMBER OF CELLS	TYPICAL DELAY (ns)[1]	LOADED DELAY (ns)[2]
2-input NAND (DUAL)	1	0.70	0.84
3-input NAND	1	1.12	1.26
4-input NAND	1	1.30	1.44
2-input NOR (DUAL)	1	0.95	1.09
3-input NOR	1	1.25	1.39
4-input NOR	1	1.87	2.01
Exclusive OR	1	2.10	2.24
Exclusive NOR	1	2.10	2.24
2-wide 2-2 input AND-OR-Inv.	1	1.92	2.10
Latch with Reset			
C→Q	1	2.97	3.11
C→$\overline{Q}$		3.67	3.81
R→Q		1.00	1.14
R→$\overline{Q}$		1.70	1.84
Set/Scan DFF with Reset			
C→Q	3	2.92	3.06
C→$\overline{Q}$		3.62	3.76
R→Q		2.13	2.97
R→$\overline{Q}$		2.83	2.97
4 : 1 Mux			
Data→Y	2	2.43	2.57
Select→Y		2.83	2.97

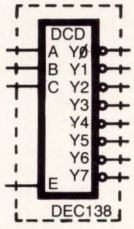
NOTES:
1 Driving 2 loads plus 2 mm of metal
2 Driving 5 loads plus 4 mm of metal

TABLE 9

HARD MSI MACROS

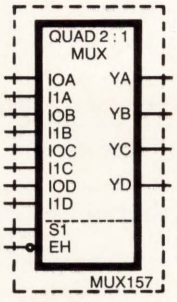
In addition to basic macros, the Q14000 Series incorporates hard MSI macros for faster, more efficient designs. MSI macros can decrease design time by using large building-blocks rather than one-cell macros. Hard MSI macros are customized transistor level implementation of complex functions as opposed to "soft macros," which are gate-level implementation through logic equivalence. AMCC's hard macros, which employ a proprietary routing scheme, have a distinct advantage over "soft macros" by 1) improving density in utilizing more transistors per cell 2) up to 40% performance improvement due to optimized metal interconnect and 3) predictable delay characteristics from pre-determined layout constraints.

TYPICAL MSI MACROS



3 : 8 DECODER WITH ENABLE

TYPICAL DELAY	F.O. = 2 2mm of metal	F.O. = 5 4mm of metal
A,B,C→Y	3.44 ns	3.58 ns
Enable→Y	2.84 ns	2.98 ns



QUAD 2 : 1 MUX

TYPICAL DELAY	F.O. = 2 2mm of metal	F.O. = 5 4mm of metal
I0,I1→Y	2.03	2.17
S1→Y	3.04	3.18

Q14000 SERIES OPERATING CONDITIONS

RECOMMENDED OPERATING CONDITIONS – COMMERCIAL

PARAMETER	MIN	NOM	MAX	UNITS
ECL Supply Voltage (V_{EE})V_{CC} = 0				
10K Mode	−4.94	−5.2	−5.45	V
100K Mode	−4.2	−4.5	−4.8*	V
ECL Input Signal Rise/Fall Time	–	1.5	5.0	ns
TTL Supply Voltage (V_{CC})	4.75	5.0	5.25	V
TTL Output Current Low (I_{OL})			20	mA
Operating Temperature	0 (ambient)		70 (ambient)	°C
Junction Temperature			130	°C

RECOMMENDED OPERATING CONDITIONS – MILITARY

PARAMETER	MIN	NOM	MAX	UNITS
ECL Supply Voltage (V_{EE})V_{CC} = 0				
10K Mode	−4.7	−5.2	−5.7	V
100K Mode	−4.2	−4.5	−4.8*	V
ECL Input Signal Rise/Fall Time	–	1.5	5.0	ns
TTL Supply Voltage (V_{CC})	4.5	5.0	5.5	V
TTL Output Current Low (I_{OL})			20	mA
Operating Temperature	−55 (ambient)		125 (case)	°C
Junction Temperature			150	°C

* −5.7V is possible. Consult AMCC for ECL 100K DC parametrics operating at this voltage.

ABSOLUTE MAXIMUM RATINGS

ECL Supply Voltage V_{EE} (V_{CC} = 0)	−8.0 VDC
ECL Input Voltage (V_{CC} = 0)	GND to V_{EE}
ECL Output Source Current (continuous)	−50 mA DC
TTL Supply Voltage V_{CC} (V_{EE} = 0)	7.0 V
TTL Input Voltage (V_{EE} = 0)	5.5 V
Operating Temperature	−55°C (ambient) to +125°C (case)
Operating Junction Temperature T_j	+150°C
Storage Temperature	−65°C to +150°C

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	COM 0°/+70°C			MIL −55°/+125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{IPD} − ECL	ECL Input Propagation Delay Including Buffer	Standard	3 loads		2.7	3.7		2.7	4.0	ns
		High Speed	3 loads		2.2	3.0		2.2	3.2	ns
t_{IPD} − TTL	TTL Input Propagation Delay Including Buffer	Standard	3 loads		5.0	6.8		5.0	7.3	ns
		High Speed	3 loads		4.0	5.4		4.0	5.8	ns
t_{OPD} − ECL	ECL Output Propagation Delay				1.2	1.6		1.2	1.7	ns
t_{OPD} − TTL	TTL Output Propagation Delay	Standard	15 pf		5.0	6.8		5.0	7.3	ns
		High Speed	15 pf		4.0	5.4		4.0	5.8	ns
t_{FPD}	Internal Equivalent Gate Delay		2 loads +2mm of metal		0.7	1.05		0.7	1.30	ns
F_{maxt}	Maximum Internal F/F Toggle Frequency				240	180		240	165	MHz
F_{in} − ECL	ECL Input Frequency at Package Pin	Standard	3 loads		150	110		150	105	MHz
		High Speed	3 loads		240	180		240	165	MHz
F_{out} − ECL	ECL Output Frequency at Package Pin		50 Ω		240	180		240	165	MHz
F_{in} − TTL	TTL Input Frequency at Package Pin	Standard	3 loads		90	65		90	60	MHz
		High Speed	3 loads		120	90		120	85	MHz
F_{out} − TTL	TTL Output Frequency at Package Pin		15 pf		90	65		90	60	MHz
t_{PZH}	Enable time to high level		Fig. 9		9	12.3		9	13.0	ns
t_{PZL}	Enable time to low level		Fig. 10		9	12.3		9	13.0	ns
t_{PHZ}	Disable time from high level		Fig. 9		9	12.3		9	13.0	ns
t_{PLZ}	Disable time from low level		Fig. 10		9	12.3		9	13.0	ns

Q14000 SERIES OPERATING CONDITIONS

ECL 10K INPUT/OUTPUT DC CHARACTERISTICS $V_{EE} = -5.2V$[1]

	$T_{ambient}$				T_{case}	
	−55°C	0°C	25°C	75°C	125°C	UNIT
$V_{OH\,max}$	V_{CC}− 850	V_{CC}− 770	V_{CC}− 730	V_{CC}− 650	V_{CC}− 575	mV
$V_{IH\,max}$	V_{CC}− 800	V_{CC}− 720	V_{CC}− 680	V_{CC}− 600	V_{CC}− 525	mV
$V_{OH\,min}$	V_{CC}−1080	V_{CC}−1000	V_{CC}− 980	V_{CC}− 920	V_{CC}− 850	mV
$V_{IH\,min}$	V_{CC}−1255	V_{CC}−1145	V_{CC}−1105	V_{CC}−1045	V_{CC}−1000	mV
$V_{IL\,max}$	V_{CC}−1510	V_{CC}−1490	V_{CC}−1475	V_{CC}−1450	V_{CC}−1400	mV
$V_{OL\,max}$	V_{CC}−1655	V_{CC}−1625	V_{CC}−1620	V_{CC}−1585	V_{CC}−1545	mV
$V_{OL\,min}$	V_{CC}−1980	V_{CC}−1980	V_{CC}−1980	V_{CC}−1980	V_{CC}−1980	mV
$V_{IL\,min}$	V_{CC}−2000	V_{CC}−2000	V_{CC}−2000	V_{CC}−2000	V_{CC}−2000	mV
$I_{in}H\,max$[2]	30	30	30	30	30	µA
$I_{in}L\,max$[2]	−.5	−.5	−.5	−.5	−.5	µA

ECL 100K INPUT/OUTPUT DC CHARACTERISTICS $V_{EE} = -4.5V$[3]

SYMBOL	PARAMETER	TEST DC CONDITIONS	COMM 0°/+70°C V_{EE} = −4.2V to −4.8V			MIL −55°/+125°C V_{EE} = −4.2V to −4.8V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	Output Voltage HIGH	Loading is 50 Ohms to −2V	V_{CC}-1035		V_{CC}- 850	V_{CC}-1080		V_{CC}- 835	mV
V_{OL}	Output Voltage LOW	Loading is 50 Ohms to −2V	V_{CC}-1830		V_{CC}-1605	V_{CC}-1880		V_{CC}-1595	mV
$V_{IH\,min}$	Input Voltage HIGH	Maximum input voltage HIGH	V_{CC}-1145		V_{CC}- 800	V_{CC}-1145		V_{CC}- 800	mV
$V_{IL\,max}$	Input Voltage LOW	Maximum input voltage LOW	V_{CC}-1950		V_{CC}-1475	V_{CC}-1950		V_{CC}-1475	mV
I_{INH}[2]	Input Current HIGH	$V_{IN} = V_{IH\,max}$			30			30	µA
I_{INL}[2]	Input Current LOW	$V_{IN} = V_{IL\,min}$			−.5			−.5	µA

TTL INPUT/OUTPUT DC CHARACTERISTICS

SYMBOL	PARAMETER	TEST DC CONDITIONS		COMM 0°/+70°C			MIL −55°/+125°C			UNIT
				MIN	TYP[4]	MAX	MIN	TYP[4]	MAX	
V_{IL}[5]	Input HIGH Voltage	Guaranteed input HIGH voltage for all inputs		2.0			2.0			V
V_{IH}[5]	Input LOW Voltage	Guaranteed input LOW voltage for all inputs				0.8			0.8	V
V_{IK}	Input clamp diode voltage	V_{CC} − Min, I_{IN} = −18mA			−.8	−1.2		−.8	−1.2	V
V_{OH}	Output HIGH Voltage	V_{CC} − Min, I_{OH} = −1mA		2.7	3.4		2.4	3.4		V
V_{OL}	Output LOW voltage	V_{CC} = Min	I_{OL} = 4mA			0.4			0.4	V
			I_{OL} = 20mA			0.5			0.5	V
I_{OZH}	Output "off" current HIGH (3-state)	V_{CC} = Max, V_{OUT} = 2.4V		−50		50	−50		50	µA
I_{OZL}	Output "off" current LOW (3-state)	V_{CC} = Max, V_{OUT} = 0.4V		−50		50	−50		50	µA
I_{IH}	Input HIGH current	V_{CC} = Max, V_{IN} = 2.7V				50			50	µA
I_I	Input HIGH current at Max.	V_{CC} = Max, V_{IN} = 5.5V				1			1	mA
I_{IL}	Input LOW current	V_{CC} = Max, V_{IN} = 0.5V				50			50	µA
I_{OS}	Output short circuit current	V_{CC} = Max, V_{OUT} = 0V		−25		−100	−25		−100	µA

1 Data measured with $V_{EE} = -5.2 \pm .1V$ (or $V_{CC} = 5.0 \pm .1V$ for +5V ref. ECL 10K) assuming a +50°C rise between ambient (T_a) and junction temperature (T_J) for −55°C, 0°C, +25°C, and +70°C, and a +25°C rise for +125°C. Specifications will vary based upon T_J. See AMCC Packaging and Design Guides concerning V_{OH} and V_{OL} adjustments associated with T_J for packages and operating conditions.

2 Per fan-in.

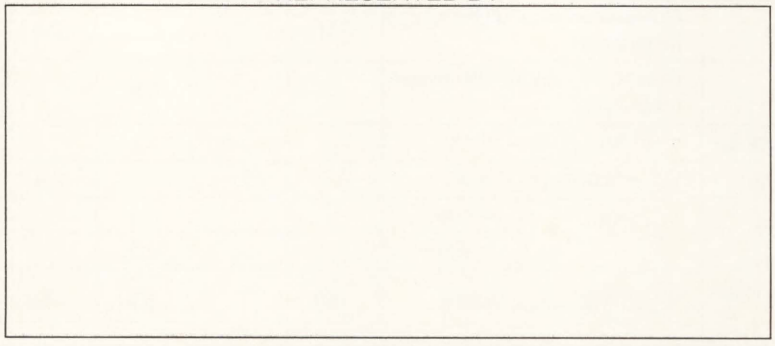
3 Data measured at thermal equilibrium, with maximum T_J not to exceed recommended limits. See AMCC Packaging Guide to compute T_J for specific package and operating conditions. For +5V ref. ECL 100K, V_{OH} and V_{OL} specifications will vary based upon power supply. See AMCC Design Guide for adjustment factors.

4 Typical limits are at 25°C, V_{CC} = 5.0V.

5a These input levels provide zero noise immunity and should only be tested in a static, noise-free environment.

5b Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMCC recommends using $V_{IL} \leq 0.4V$ and $V_{IH} \geq 2.4V$ for functional and AC tests.

REPRESENTED BY



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Of course, AT&T can accept a customer's logic diagram and electrical specifications, and our designers will perform the complete design cycle, thus requiring minimal customer interaction at appropriate review intervals prior to prototype mask commitment.

The process outlined above is capable of producing highly complex standard cell designs with a first-time silicon success rate approaching 100%. Our ASIC offering is differentiated by the following features:

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- A Versatile Functional Design System
- Parameterized Macroblock Compilers
- Total Commitment to Technology Advancement
- Superior CMOS Performance
- Powerful CAD Tools Designed to Eliminate Risk
- Full Testing Capability and Quality Assurance
- Complete IC Design Support and CAD Tool Training

Cell Libraries

AT&T's standard cells are predesigned and precharacterized logic elements providing an extensive choice of logic functions as well as speed/size tradeoffs to accommodate a wide range of requirements. The library includes combinatorial cells, sequential elements, linear functions, input/output buffers and level shifters. In each technology, we supply two versions of our cell library. In one version, cells are area-optimized to minimize chip size. In the other version, cells are larger to maximize performance. The two libraries can be combined on the same chip if necessary.

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Complex VLSI circuits, however, are made up of more than just simple logic elements. The capability to easily create complex functions is essential to the fast development of any design. That is why AT&T's comprehensive Functional Design System (FDS) meets this need. Following simple interactive procedures, a customer can quickly synthesize or compile complex logic functions from simple functional specifications. The functionally synthesized elements available include:

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- Comparators
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- Multipliers
- Parity generators
- Universal registers
- Combinatorial cells
- Finite state machines

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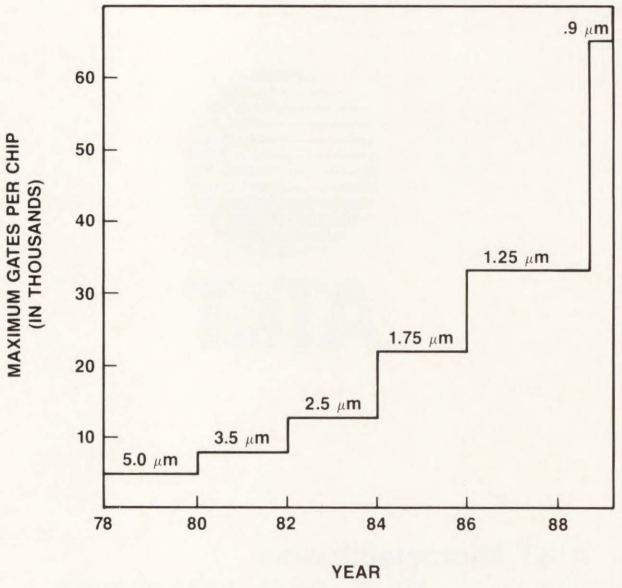
At AT&T, we're constantly shrinking design rules to bring ever greater complexity and performance within the reach of our customers. Our current mainstream VLSI technology is 1.25 μm CMOS. And you can bet we're not stopping there! But aggressive technology development means nothing if the finished part won't work. So, to ensure the manufacturability of all of our customers' designs, we process initial prototypes on the same fabrication line that will supply production requirements.



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Our high-volume CMOS processes utilize twin-tub epitaxial structures. This enables us to optimize both NMOS and PMOS transistor characteristics for superior circuit performance.

CMOS Speed Performance

Gate	Average Gate Delay (ns)
	1.25 μm (1.0 μL′)
Inverter	0.8
2-input NAND	1.0
f-f setup	0.7
f-f clk to out	1.6
Input buffer	1.0
Output buffer (50 pF load)	3.5

(Nominal process, 5 V power supply, 25°C, fanout = 3, 2.5 mm wire.)

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(34-1-) 404-6263, 403-4114

Custom

ASIC CMOS Standard Cell Library Generation

AT&T has developed a fast, error-free method of generating standard-cell mask layouts and associated models that is unique in the standard-cell custom IC industry. The method allows standard-cell users to incorporate the latest technology into their designs. The process consists of standard-cell support library generation and is illustrated in Figure 1. The VTGEN computer program generates all standard-cell mask layouts and stores them in a library. The HCAP tool then extracts the simultation models from the mask layouts and stores these models in support libraries to be accessed by other CAD systems such as ADVICE, MOTIS3, and LTX2.

Mask Layout Generation

VTGEN combines two files to create the mask layouts for the library elements: a cell-description file and a technology file. The cell description file is obtained from a library of technology-independent standard cell descriptions, where each cell description defines a function in terms of its logic definition and transistor-level connectivity. The technology file contains information about the cell layout style and also provides technology-dependent design rules such as window size and spacing, metal pitch, and other tolerances. VTGEN uses the cell description file and the technology file to automatically generate a file containing the mask layout of every standard cell. Each mask layout will perform the function specified by its cell description, and will conform to the design rules for a specified technology. The mask layouts become part of the library.

Simulation Model Generation

HCAP extracts the simulation models directly from the mask layouts in the library. Two input files are required by HCAP: the file of standard cell mask layouts from the library and a second technology-dependent file containing performance-determining parameters. HCAP uses these two files to automatically generate a symbolic layout description and a transistor-level model. Two files (one for ADVICE and MOTIS3, and one for LTX2) are created and added to the library. Once the simulation models are available, a table of gate delays for different output loads is determined by simulation and published in the standard-cell catalog.

New Standard Cells

If a new cell type is needed for a specific application, AT&T's Standard Cell group will create the required cell description, and VTGEN will generate the mask layout using the appropriate technology file. HCAP then will extract the simulation models and the symbolic layout description, and append them to the library. In most cases, this entire process is easily completed in less than one day.

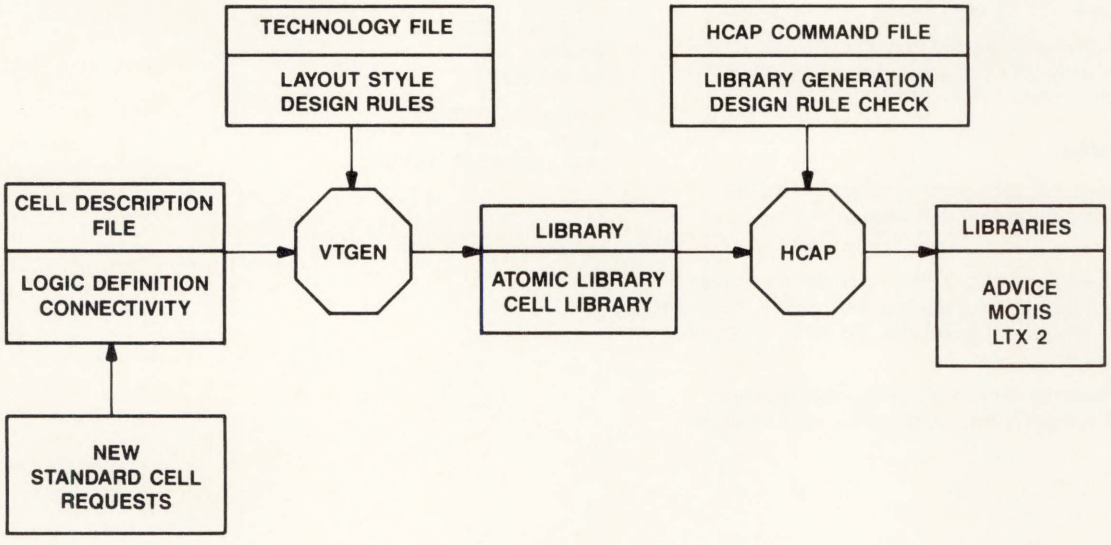
Design System

AT&T provides a system of integrated Computer Aided Design tools to assist designers in each phase of IC development. Designers are freed from the time-consuming and error-prone task of data conversion, since these tools are integrated by a common interface, which makes all the tools compatible—from schematic capture to layout verification.

The schematic capture tool is flexible, easy-to-use, and offers the powerful features needed for complex VLSI circuits. Several auditing features provide early detection of circuit problems, thereby shortening the design cycle. The simulator provides the ability to quickly and accurately verify both the logic and timing requirements. The design-for-testability tools alleviate the usual laborious task of generating high-fault coverage vectors. The layout tool handles both standard cells and higher-level blocks. Automatic placement and routing assure that even the most complex circuits are properly interconnected.

The AT&T system has demonstrated a very high first-time success rate on custom standard-cell designs. The tools facilitate the design of circuits that push the limits of technology, both in gate count and performance.

Figure 1. Standard-Cell Support Library Generation.



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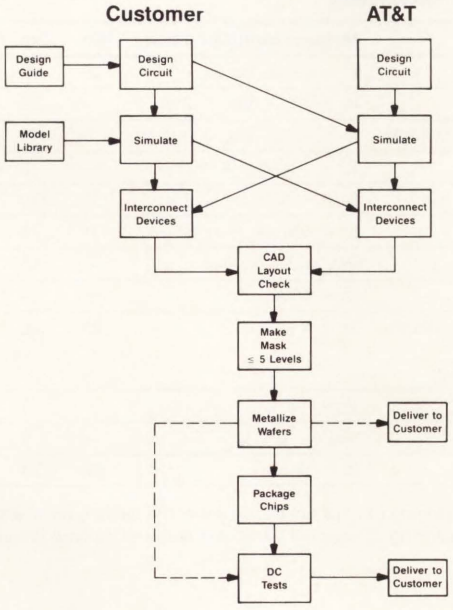
☐ AT&T Microelectronics, Dept. 51AL230230, 555 Union Boulevard, Allentown, PA 18103 **1-800-372-2447** (In Canada, **1-800-553-2448)**

AT&T's Semicustom Alternative

Flexible Design Options



1-800-372-2447

AT&T semicustom linear arrays are the cost-effective alternative to custom design. The semicustom approach is the most economical route to satisfy production requirements for less than 50,000 devices. Semicustom development costs are significantly lower than those for a full-custom IC development, with prototypes available within six to eight weeks of design verification. A semicustom design can also be the first step in the two-step design process that leads to a full-custom integrated circuit. The semicustom design allows initial low-volume production to begin, and can be replaced with a full-custom design for high-volume production.

Linear Array Capabilities

AT&T's family of CBIC linear arrays has been designed to fulfill a wide range of applications using a complementary vertical NPN and PNP transistor technology. Our linear arrays satisfy circuit design requirements ranging for dc to VHF, and 5 to 90 volt applications. In addition, some linear arrays combine analog and digital circuitry on the same chip. AT&T linear array applications are limited only by your imagination.

From design through manufacture, AT&T can assist you with all your design needs. In fact, our sales account managers and support engineers are just a phone call away. We invite you to join us in discovering the benefits of semicustom linear arrays.

Package Type	Pin Counts
Through-Hole Technology	
DIP — Plastic	8, 16, 18, 20, 24, 28, 32, 40
Surface Mount Technology	
Chip Carriers — Plastic	44
Plastic SOJ (J Leads)	16, 20, 28
Plastic SOIC (Gull Wing)	
Wide Body	16, 20, 28

AT&T Microelectronics
555 Union Blvd., Dept. 51AL230230
Allentown, PA 18103

AT&T

Description

The ALA201/202 UHF Linear Arrays are semi-custom integrated circuits consisting of vertical NPN and PNP transistors, programmable and fixed capacitors, and implanted boron resistors. Designed on a regular grid system, the array provides easy interconnection for the designer. The ALA201/202 UHF Linear Arrays are fabricated in a complementary bipolar integrated circuit (CBIC) process that offers the advantages of similar NPN and PNP transistor characteristics at very high speeds. Typical f_T of 4.5 GHz for the NPN and 3.75 GHz for the PNP transistors (V_{CE} = 6 volts and I_C = 3 mA) with high current drive capability (8 mA for the NPN and PNP 1X transistors) is unique to these linear arrays.

Dual-layer and thick metal are typically used for most applications; however, single-layer metal may be used upon special request. The bottom and top metal layers have a low sheet resistance of about 0.03 ohm/sq. and a current capacity of 2 mA/μm of metal width. The standard 6 μm bottom and 10 μm top metal linewidths are capable of carrying a maximum of 12 and 20 mA dc current, respectively. For cases where high-current must be carried, a thicker gold layer called "thick metal" is available with a sheet resistance of about 0.004 ohms/sq. and a current capacity of 14 mA/μm of metal width. The ALA201 device is divided into 6 modules consisting of 5 standard and 1 power module. The ALA202 device is divided into 12 modules consisting of 9 standard, 2 power, and 1 input module. All modules are symmetrically located within the array for easy layout. The modules, being on a regular grid system, allow the user to interconnect components by drawing lines on a clearly defined grid marked on a layout sheet.

For more detailed information regarding ordering procedures, design kits, and packaging for the ALA201/202 UHF Linear Arrays, refer to the Semi-Custom Linear Array brochure.

Features

- Quick design turnaround
- Custom circuitry at low cost
- High performance
- Design proprietorship
- High probability of success
- High reliability

Electrical Characteristics

T_A = 25°C unless otherwise specified

NPN dc Parameters

Symbol	Measurement/Condition	Min	Typ	Max	Unit
h_{FE}*	I_C = 1 mA, V_{CE} = 2 V	80	110	—	—
f_T	I_C = 1 mA, V_{CE} = 2 V	—	3.5	—	GHz
V_A (early voltage)	I_C = 1 mA, V_{CE} = 2, 4 V	20	40	—	V
$V_{CE\ (sat)}$	I_C = 1 mA, I_B = 100 μA	—	.13	.35	V
V_{BE}**	I_E = 1 mA, V_{CE} = 2 V	.720	.775	.820	V
BV_{CEX}	I_C = 100 μA, I_B = 0.1 μA	12	18	—	V
I_{EBO}	V_{EB} = 2 V, I_C = 0	—	.02	1	μA
BV_{CBO}	I_C = 1 μA	20	30	—	V
BV_{CSO} (collector substrate breakdown)	I_C = 1 μA	20	60	—	V
I_{CES}	V_{CE} = 5 V	—	1	—	nA
I_{CBO}	V_{CB} = 10 V, I_E = 0	—	1	—	nA
BV_{EBO}	I_E = 10 μA	4.7	5.3	5.9	V

PNP dc Parameters

Symbol	Measurement/Condition	Min	Typ	Max	Unit
h_{FE}*	I_C = 1 mA, V_{CE} = 2 V	25	40	—	—
f_T	I_C = 1 mA, V_{CE} = 2 V	—	2.5	—	GHz
V_A (early voltage)	I_C = 1 mA, V_{CE} = 2, 4 V	8	11	—	V
$V_{CE\ (sat)}$	I_C = 1 mA, I_B = 100 μA	—	.13	.35	V
V_{BE}**	I_E = 1 mA, V_{CE} = 2 V	.730	.780	.830	V
BV_{CEX}	I_C = 100 μA, I_B = 0.1 μA	11	14	—	V
I_{EBO}	V_{EB} = 2 V, I_C = 0	—	.01	1	μA
BV_{CBO}	I_C = 1 μA	16	19	—	V
BV_{CSO} (collector substrate breakdown)	I_C = 1 μA	20	40	—	V
I_{CES}	V_{CE} = 5 V	—	1	—	nA
I_{CBO}	V_{CB} = 10 V, I_E = 0	—	1	—	nA
BV_{EBO}	I_E = 10 μA	5.0	5.4	6.7	V

* h_{FE} matching of adjacent transistors of the same type is within ±5%.
** V_{BE} matching of adjacent transistors of the same type is within ±1.5 mV.

For additional information, contact your AT&T Account Manager, or call:
☐ AT&T Microelectronics, Dept. 51AL230230, 555 Union Boulevard, Allentown, PA 18103 **1-800-372-2447** (In Canada, **1-800-553-2448)**

Resistor Data (ALA201) T_A = 25°C

Value (Ω)	Tol (%)	Type	TCR PPM/°C	Total
50	±20	BI*	+1300	40
100	±20	BI*	+1300	240
200	±20	BI*	+1300	40
1000	±20	BI**	+1100	20
2000	±20	BI**	+1100	120
4000	±20	BI**	+1100	20

Capacitor Data (ALA201)

Type	Cap (pF)	Tol (%)	Total
Programmable	0.75 to 3.35	±20	5
Fixed	1.0	±20	10
Programmable	1.0 to 32	±20	6

Component Totals (ALA201)

Component	Type	Total	Standard	Power
Transistors				
NPN	1X	47	9	2
NPN	2X	12	2	2
NPN	5X	7	1	2
NPN	15X	2	—	2
PNP	1X	27	5	2
PNP	2X	12	2	2
PNP	5X	2	—	2
PNP	15X	2	—	2
Resistors*	50 Ω	40	8	—
	100 Ω	240	40	40
	200 Ω	40	8	—
Resistors**	1000 Ω	20	4	—
	2000 Ω	120	20	20
	4000 Ω	20	4	—
Capacitors	0.75 to 3.35 pF	5	1	—
	1.0 pF	10	2	—
	1.0 to 32 pF†	6	—	—
Bonding Pads	—	36	—	—

* Denotes a 50 ohm/sq. implanted boron resistor.
** Denotes a 1080 ohm/sq. implanted boron resistor.
† These capacitors are located on the border of the overall die.

Note: Matching of adjacent resistors of similar type is within ±1%.

Resistor Data (ALA202) T_A = 25°C

Value (Ω)	Tol (%)	Type	TCR PPM/°C	Total
50	±20	BI*	+1300	80
100	±20	BI*	+1300	480
200	±20	BI*	+1300	80
1000	±20	BI**	+1100	40
2000	±20	BI**	+1100	240
4000	±20	BI**	+1100	40

Capacitor Data (ALA202)

Type	Cap (pF)	Tol (%)	Total
Programmable	0.75 to 3.35	±20	10
Fixed	1.0	±20	20
Programmable	1.0 to 32	±20	8

Component Totals (ALA202)

Component	Type	Total	Standard	Input	Power
Transistors					
NPN	1/3X	2	—	2	—
NPN	1X	92	9	7	2
NPN	2X	24	2	2	2
NPN	5X	14	1	1	2
NPN	15X	4	—	—	2
PNP	1/3X	2	—	2	—
PNP	1X	52	5	3	2
PNP	2X	24	2	2	2
PNP	5X	4	—	—	2
PNP	15X	4	—	—	2
Resistors*	50 Ω	80	8	8	—
	100 Ω	480	40	40	40
	200 Ω	80	8	8	—
Resistors**	1000 Ω	40	4	4	—
	2000 Ω	240	20	20	20
	4000 Ω	40	4	4	—
Capacitors	0.75 to 3.35 pF	10	1	1	—
	1.0 pF	20	2	2	—
	1.0 to 32 pF†	8	—	—	—
Bonding Pads	—	48	—	—	—

* Denotes a 50 ohm/sq. implanted boron resistor.
** Denotes a 1080 ohm/sq. implanted boron resistor.
† These capacitors are located on the border of the overall die.

Note: Matching of adjacent resistors of similar type is within ±1%.

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ANALOG

ALA400/401 Linear Array Family

Description

The ALA400/401 Linear Array Family is fabricated using the complementary bipolar integrated circuit (CBIC) process that offers the advantages of vertical NPN and vertical PNP transistors. CBIC technology offers the advantage of designing high-performance circuits with less design complexity. A minimum collector-to-emitter, reverse breakdown voltage of 33 volts is guaranteed for both transistors.

Typical peak f_T of 350 MHz for NPN and 300 MHz for PNP transistors and 2 mA current drive capability for the 1 X transistors are unique for these linear arrays. Current drive capability for the other on-chip transistors is linear, e.g., 2 X = 4 mA, 3 X = 6 mA, etc. Pinch-off voltage for JFETs is 1 to 2 volts. I_{DSS} is about 1.0 mA.

The ALA400 Linear Array is divided into 16 modules, consisting of 12 standard, 2 power and 2 JFET modules. The ALA401 Linear Array is divided into 9 modules, consisting of 7 standard and 2 power modules. All modules are symmetrically located within the array for ease of design layout. Because the modules are on a regular grid system, the user interconnects components by drawing lines on a clearly defined grid, marked on a layout sheet.

Two-level metal is used for interconnections. Upon request, a thick-metal interconnect is also available to provide higher current capacity. The top metal layer has a low sheet resistance of <0.03 Ω/sq. and a current capacity of 2.0 mA/micron metal width. The bottom metal layer has a sheet resistance of <1.0 Ω/sq. and a current capacity of 200 μA/micron of metal width. The thicker metal interconnect has a sheet resistance of <0.003 Ω/sq. and a current capacity of 20 mA/micron of metal width.

Features

- High-frequency performance, typical f_T of 350 MHz for NPN and 300 MHz for PNP transistors
- 33 volt capability
- Low development costs
- Quick design turnaround, typically six to eight weeks from design approval
- Complementary vertical NPN and PNP transistors
- Two-level metal interconnect
- All I/O ESD protected

Component Totals (ALA400)

Component	Type	Total	Standard	JFET	Power
NPN	1 X	70	5	5	—
NPN	2 X	12	1	—	—
NPN	3 X	16	1	—	2
NPN	38 X	4	—	—	2
PNP	1 X	70	5	5	—
PNP	2 X	12	1	—	—
PNP	3 X	16	1	—	2
PNP	63 X	4	—	—	2
Resistors*	500 Ω	104	8	4	—
	1 kΩ	168	12	12	—
Resistors**	5 kΩ	216	16	8	4
	10 kΩ	168	12	12	—
Capacitors	—	14	1	1	—
JFETs	—	4	—	2	—
Bonding Pads	—	44	—	—	—

* Denotes a 200 ohm/sq. implanted boron resistor.
** Denotes a 2000 ohm/sq. implanted boron resistor.

Component Totals (ALA401)

Component	Type	Total	Standard	Power
NPN	1 X	43	5	4
NPN	3 X	16	2	1
NPN	38 X	2	—	1
PNP	1 X	43	5	4
PNP	3 X	16	2	1
PNP	63 X	2	—	1
Resistors*	100 Ω	42	6	—
	500 Ω	72	8	8
	1 kΩ	64	8	4
Resistors**	5 kΩ	132	16	10
	10 kΩ	100	12	8
Capacitors	—	7	1	—
Bonding Pads	—	38	—	—

* Denotes a 200 ohm/sq. implanted boron resistor.
** Denotes a 2000 ohm/sq. implanted boron resistor.

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Electrical Characteristics $T_A = 25°C$

NPN1X Transistor

Symbol	Measurement Condition	Min	Typ	Max	Unit
h_{FE}*	I_C = 1 mA, V_{CE} = 2.5 V	40	85	250	—
I_C	80% of peak h_{FE}	—	2	—	mA
BV_{CEO}	I_C = 1 mA	33	38	—	V
BV_{CBO}	I_C = 10 μA	33	50	—	V
BV_{EBO}	I_C = 10 μA	7.7	8.2	8.7	V
V_{BE}**	I_E = 100 μA	—	743	—	mV
R_{sat}	h_{FE} = 2	—	37	—	Ω
$V_{CE\ (sat)}$	I_C = 1 mA, h_{FE} = 2	—	70	150	mV
V_A (early voltage)	I_C = 500 μA	65	225	—	V
f_T	V_{CE} = 10 V	—	350	—	MHz

* h_{FE} match of same type adjacent transistors is within 5%.
** V_{BE} match of same type adjacent transistors is within 1.5 mV.

PNP1X Transistor

Symbol	Measurement Condition	Min	Typ	Max	Unit
h_{FE}*	I_C = 1 mA, V_{CE} = 2.5 V	40	110	250	—
I_C	80% of peak h_{FE}	—	800	—	μA
BV_{CEO}	I_C = 1 mA	33	47	—	V
BV_{CBO}	I_C = 10 μA	33	48	—	V
BV_{EBO}	I_C = 10 μA	7.7	8.2	8.7	V
V_{BE}**	I_E = 100 μA	—	748	—	mV
R_{sat}	h_{FE} = 2	—	127	—	Ω
$V_{CE\ (sat)}$	I_C = 1 mA, h_{FE} = 2	—	140	250	mV
V_A (early voltage)	I_C = 500 μA	45	60	—	V
f_T	V_{CE} = 10 V	—	300	—	MHz

* h_{FE} match of same type adjacent transistors is within 5%.
** V_{BE} match of same type adjacent transistors is within 1.5 mV.

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ANALOG

ATE-Series Digital Bipolar Gate Arrays

AT&T Microelectronics is introducing a new series to the family of existing custom gate arrays. The customized high-speed TTL-ECL gate arrays are designed using Scaled-Fast Oxide-Isolated Logic (SFOXIL) bipolar technology which offers higher operating speeds. The new gate arrays are the ATE6000, ATE3000, and ATE1000 and will be available at the end of 1Q88, 2Q88, and 3Q88 respectively.

Product Features

- Several internal speed and power options available:

Speed	*Power*
500 ps	1.25 mW/gate
300 ps	2.5 mW/gate
200 ps	5.0 mW/gate

- Internal clock frequency of 500—800 MHz
- ECL and TTL buffers for optimum speed/power combinations:
  ECL buffer input: 300 ps
  ECL buffer output: 600 ps

  TTL buffer input: 500 ps
  TTL buffer output: 2400 ps
- ECL outputs that drive 50 Ω loads
- Fast turnaround time of 6 weeks from t = 0
- ECL and TTL input/outputs available
- Highly integrated SSI/MSI macro library available

CAD Features

- Schematic capture
- Multiple-delay logic simulation
- Automatic placement and routing
- Design verification
- Test program generation

Product Matrix

Gate Array Code	Maximum No. of Equivalent Gates	Total No. of Inputs, Outputs, and Input/Outputs	Package Type
ATE1000	1,000	To be determined	To be determined
ATE3000	3,000	To be determined	To be determined
ATE6000	6,000	120	149-pin PGA

For additional information, contact your AT&T Account Manager, or call:
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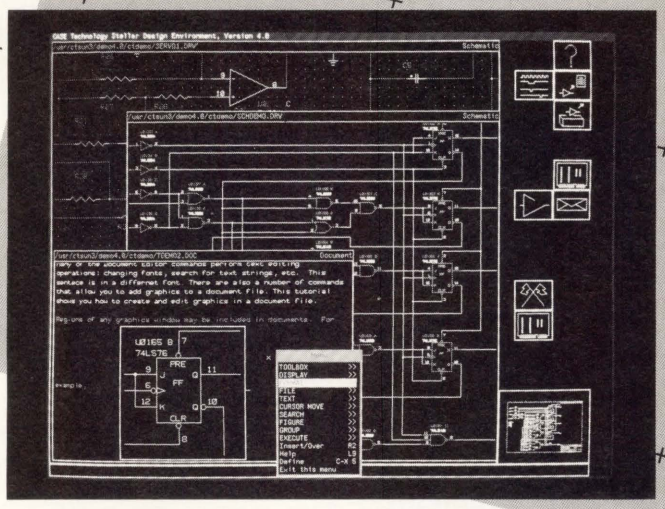
CASE Technology Vanguard Graphics Framework

- **Simplifies user integration of third-party software**
- **Platform-independent file formats and user interface**
- **Powerful window system consistent with workstation standards (SunView, UIS)**
- **Configurable inter-process communication**
- **Common simulator data format (CSDF)**
- **User-definable hierarchical menus**
- **Simple powerful macro language**
- **Redefinable keystroke definition**
- **User-definable context-sensitive help facility**



In today's modular engineering tool environment, design engineers require comprehensive tools linked to a framework. And the Vanguard Graphics Framework provides a complete symbolic toolset to link major application tools with a system independent language. With the Vanguard Graphics Framework designers can integrate third-party software or customer-specific functions quickly and easily.

Platform Independence

Software can be easily integrated on any of the supported platforms (Sun, VAX, PC). The integration mechanism is platform-independent, allowing the user to develop one set of menus and macros that will be on any supported platform.

Window System

The native window system is supported on Sun and VAX, allowing third-party graphic programs to run simultaneously with the Vanguard Design System in their own windows. The windows live within the Sun and VAX window systems, and a consistent multi-window capability is provided on the PC.

Multi-Processing

An inter-process communication mechanism allows multiple asynchronous processes to execute while the software is executing, and to communicate with the Vanguard software using standard workstation mechanisms.

Simulator Integration

The Common Simulator Data Format (CSDF) provides a standard data format for expression of analog or digital waveform data, supported by simulator vendors today. This simple format can be generated by third-party programs to allow configurable display of waveform data within the graphic framework environment.

Menus

The graphics environment provides hierarchical user-configurable menus. Up to five levels of nesting are supported, and the user can bind arbitrary commands, macros, or external functions to the menu items. Menus are also configurable per window, and are context-sensitive depending on the selected object.

Macros

The Vanguard macro language allows the user to quickly define special functions which operate on system data types and communicate with the file system and external programs through simple commands. The macro language is based on simple user commands which can be recorded automatically by the macro processor, providing a "rehearsal mode" command creation capability.

Speed Keys

Keyboard bindings can be redefined or augmented to meet specific customer needs. Common commands or macros can be bound directly to specific keys for quick access.

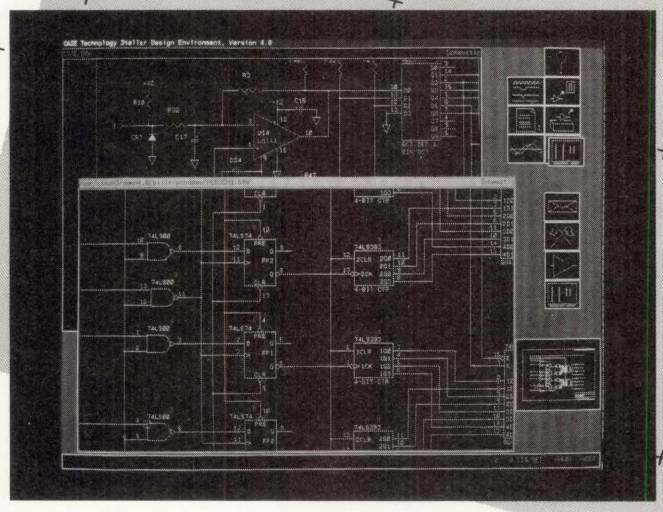
Help

The user-definable help facility allows specific help information to be provided for any command.

TERADYNE

Teradyne EDA
5155 Old Ironsides Drive
Santa Clara, California 95054
408/980-5200

CASE Technology Vanguard Design Capture System



The Vanguard Design Capture System provides the most powerful tool in the industry for creating and editing schematics.

The schemetic design system incorporates pop-up menuing and windowing capabilities allowing designers to work or view multiple schematic pages simultaneously without leaving the CASE environment.

Product Highlights:

- **Display and edit multiple schematic sheets**
- **Hierarchical desgn**
- **Intelligent rubberbanding lines**
- **Closet-point line drawing**
- **Automatic text placement**
- **Ability to rotate all text fields in 90 degree increments.**
- **Fast and powerful SCALD Hardware compiler complies large designs in minutes.**
- **User definable keystroke macros.**
- **Automatic pan and multiple zoom levels.**

Configurable User Interface

The Schematic Design System also gives the designer many choices in configuring the user interface. One option is the split screen with a schematic drawing on the left and a hierarchial menu on the right. This option is beneficial for first time users allowing them to easily learn the system.

Context-Sensitive Menu Capability

Allows the user to invoke the help function from any position within the pop-up menus or windows, and receive detailed information about the operation of a particular command in the pop-up menu or window where the cursor is located.

Multi-Window Structure

To keep information and functions easily accessible, the system employs several different windows, all accessible with single keystrokes. The window environment allows the user to display multiple schematics with a layout window simultaneously, as well as digital and analog waveform and document windows. This permits direct interactions between the schematic, layout and simulation. In addition, the Schematic Design System also supports graphic icons for its windows for a shorter learning curve and optimum use of screen space.

Windows include the schematic reference window, the library window for access to parts libraries, the component description window, and a color layer window just to name a few.

Database Management:

In contrast to many CAE systems, the Vanguard CAE Design System keeps the database compact. This is an important consideration in memory-limited systems and avoids performance degradation associated with "thrashing" in virtual memory-based systems. The compact database is achieved through the use of a frame-based method of storing component and graphics information.

ASCII File Interface:

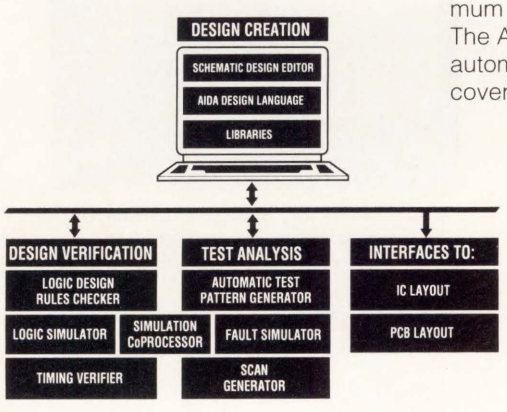
Even with the compact database structure used in the Schematic Design System, data remains in an easily accessible form. All files are documented ASCII formats allowing simple transfer between platforms and easing user creation of special purpose analysis or conversion programs. This also allows the designer to integrate the Vanguard Design System easily with internal or third-party design tools.

TERADYNE

Teradyne EDA
5155 Old Ironsides Drive
Santa Clara, California 95054
408/980-5200

AIDA TESTABILITY TOOLS

The AIDA Testability Tools provide integrated test evaluation and pattern generation for designers of large systems using ASICs. Each test vector created by the AIDA ATPG is evaluated by the AIDA Fault Simulator to eliminate additional faults. The AIDA Scan Ring Generator automatically implements scan rings for device or system test.



The AIDA Design System

Highlights

- **Automatic Test Pattern Generator (ATPG)**
- **Automatic Scan Ring Generator (SCANGEN)**
- **Accelerated Fault Simulator (FLTSIM)**
- **100% testability for scan designs using ASICs**
- **All tools operate as shared engineering resources**
- **All tools accept designs created on other systems**
- **Integrated tools work together to create optimized test pattern set**

The AIDA testability tools provide users with fast, accurate test pattern generation, fault grading, and automatic test path synthesis for large ASIC and system level designs. Designers can achieve 100% fault coverage of single stuck-at faults, using ATPG patterns alone or in combination with their own test vectors. The AIDA Scan Ring Generator speeds production testing by automatically creating an advanced test methodology. And because the tools are integrated, the AIDA Fault Simulator checks the coverage of each ATPG pattern to ensure maximum coverage with minimum vectors. The AIDA Testability Tools provide automatic test analysis and fault coverage for large system designs.

Importance of Testability

As designs become more complex and expensive to produce, they become increasingly difficult to test for manufacturing defects. Because the manufacturing yields of IC processes are low compared to established PCB manufacturing lines, using the same level of test pattern coverage allows more defective parts to ship to end users. And the cost in terms of money, time, and customer goodwill of discovering defects after manufacturing and assembly follows the same escalating trend.

Manually creating a set of patterns which exercises design functionality is no longer an acceptable solution. As chips push 100K gates, no designer can write vectors that will achieve the necessary fault coverage. Because the cost of allowing defective parts to pass into manufacturing increases with the complexity of the chip, extremely high coverage is required. Manufacturers who cannot efficiently test chips and systems will not be able to compete.

Designing for Testability

Most available fault grading tools perform toggle tests or probabilistic fault grading. Because toggle tests provide no comparison of correct vs. incorrect results, they are nearly useless as test tools. Similarly, probabilistic fault grading shows only statistical results, providing no guidance for improving test coverage. As chips get larger and gate counts increase, these problems increase. One effective solution for these problems is to design testability into the system from the start.

TERADYNE

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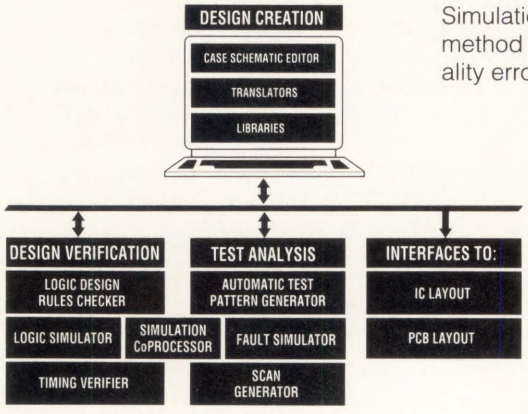
AIDA MEMORY & LOGIC COSIMULATOR ACCELERATORS

(CoSim/ML)

Very large, multi-chip, multi-board system designs can be evaluated cost-effectively at the gate level with the AIDA Memory & Logic CoSimulator accelerator. The CoSim/ML Processor simulates up to 8 million gates at 10 million evaluations per second. CoSim/ML is a standalone accelerator which functions as a network resource with both Apollo and Sun workstations.



The AIDA Design System

Highlights

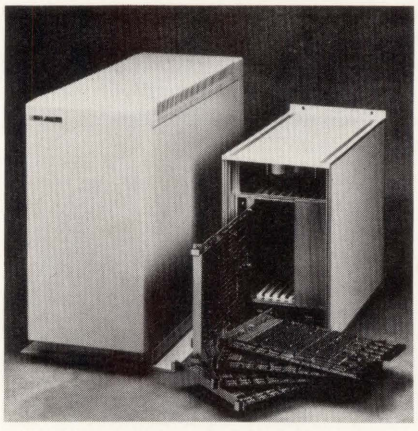
- **Simulates up to 7 million bits of RAM and ROM using on-board emulation**
- **Up to 10 million gate evaluations per second**
- **Handles tristate drivers, bi-directional ports, bus transceivers**
- **Accelerates Levelized Compiled Code (LCC) operation of AIDA Logic and Fault Simulators**
- **Very large capacity for gate-level simulation of large systems using ASICs**

The AIDA Memory & Logic CoSimulator Accelerator (CoSim/ML) provides designers of large complex systems with fast, accurate simulation of entire multi-chip, multi-board systems. Using the CoSim/ML from their own workstation over a network, designers can quickly and easily simulate large systems designs using ASICs. The AIDA CoSim/ML accelerator enables designers to verify the function and debug the operation of complete systems of up to 8 million gates on their own workstation.

Challenges of Multi-chip, Multi-board, Mixed-technology Simulation

Simulation turn-around is a key method for detecting design functionality errors, and has become the gating item for many systems design projects. Large portions of chips and chip sets must be simulated several times a day with useful and understandable results in order for a design team to maintain tight development schedules. Systems incorporating chips with mixed technologies and ASICs from multiple foundries require accelerated system level simulation for accurate design.

Many logic simulators fail to take into consideration the realities of large systems design. Few simulators provide sufficient capacity. They often flood users with data, producing tens of thousands of lines of simulation data. While some of this data is simply irrelevant, much of the rest requires analysis which can take many days. Once different technologies and different modeling levels are added to the picture, designers are often left drowning in a sea of unmanageable data with no way to discover whether their design is performing correctly.



The AIDA Memory & Logic CoSimulator Processor (Dimensions 26"x13"x24")

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5155 Old Ironsides Drive
Santa Clara, CA 95054
408/980-5200

FUJITSU

FUJITSU ASIC PRODUCT GUIDE

Fujitsu is the world's largest producer of ASIC products. Since 1974, we have taken over 9,000 design-starts through volume production; the longest proven track record in the industry. Today, Fujitsu continues to make the world's largest commitment of human, technical, and financial resources to the ASIC business.

Select from our complete line of CMOS, ECL and BiCMOS gate arrays and standard cells. From our state-of-the-art 1.2 micron CMOS gate arrays and standard cells to our industry-leading 10,000 gate ECL gate arrays — Fujitsu is the ASIC partner you've been looking for.

FUJITSU BIPOLAR TECHNOLOGY — GATE ARRAYS

ET Series ECL Gate Arrays	Part Number	Basic Logic Cells	Equivalent Gates*	I/O Count & Special Functions
1.0μ ECL 220 ps/800 MHz ECL, TTL, or Mixed Interface	ET750	192 Cells	1,056 Gates	64 I/O, 48 ECL Outputs
	ET1500	384 Cells	2,112 Gates	88 I/O, 64 ECL Outputs
	ET3000	768 Cells	4,224 Gates	120 I/O, 72 ECL Outputs
	ET4500	1,120 Cells	6,160 Gates	136 I/O, 84 ECL Outputs
	ET2004M	480 Cells	2,640 Gates	120 I/O,** 4.6Kbit RAM @ 3.2ns t_{AA}†
	ET2009M	480 Cells	2,640 Gates	120 I/O,** 9.2Kbit RAM @ 4ns t_{AA}†
	ET3004M	720 Cells	3,960 Gates	120 I/O,** 4.6Kbit RAM @ 4ns t_{AA}†
ET-H Series ECL Gate Arrays				
0.5μ ECL 100 ps/1GHz ECL or Mixed ECL/TTL Interface	ET10000H	1,792 Cells	9,856 Gates	200 I/O, 120 ECL outputs ††
	E10000H	1,792 Cells	9,856 Gates	300 I/O, 150 ECL outputs

* Full Adder = 11 Gates ** 136 I/O Optional † Typical †† Mixed TTL/ECL interface available

ET Series BiCMOS Gate Arrays	Part Number	Basic Logic Cells*	Equivalent Gates**	I/O Count
1.5μ, 0.8 ns/180 MHz	BC400	430 Cells	645 Gates	52 @ 24mA
	BC800	812 Cells	1,218 Gates	72 @ 24mA
	BC1200	1,248 Cells	1,872 Gates	96 @ 24mA
	BC2000	2,160 Cells	3,240 Gates	112 @ 24mA

* Three input gates ** Two input gates

ET Series LSTTL Gate Arrays	Part Number	Basic Logic Cells*	Equivalent Gates**	I/O Count
1.25 ns/150 MHz	B240	240 Cells	360 Gates	40 @ 24mA
1.25 ns/150 MHz	B350	360 Cells	540 Gates	40 @ 24mA
2.4 ns/70 MHz	B350B	352 Cells	528 Gates	44, 16 @ 48mA
1.25 ns/150 MHz	B600	616 Cells	924 Gates	64 @ 24mA
2.4 ns/70 MHz	B700B	720 Cells	1,080 Gates	64, 24 @ 48mA
1.25 ns/150 MHz	B1100	1,120 Cells	1,680 Gates	88 @ 24mA

* Three input gates ** Two input gates

Note: I/O gate count is not included in Basic Logic Cell or Equivalent Gate density numbers. LSTTL and BICMOS cells have three (3) logic inputs.

FUJITSU CMOS TECHNOLOGY — STANDARD CELLS

AU Series Standard Cell	Compiliable Cells	Super Macros	Basic Logic Cells (2 Input Gate)	Performance
1.2μ CMOS 2- & 3-Layer Metal	32K RAM, 128K ROM PLAs, Registers, Multipliers, ALU	Standard LSI equivalent functions (29xx, 68xx, 82xx)	>60K Gates 2-Input gate equivalent	<0.8 ns typ. <1.3 ns worst case
AV Series Standard Cell				
1.8μ CMOS 2-Layer Metal	16K RAM, 64K ROM, PLAs, Registers	Standard LSI equivalent functions	>13K Gates 2-input gate equivalent	<1.4 ns typ. <2.2 ns worst case

FUJITSU ASIC PRODUCT GUIDE

FUJITSU CMOS TECHNOLOGY — GATE ARRAYS

UHB Series Gate Arrays	Part Number	Basic Logic Cells	I/O Count	Special Functions
	C12000UHB	12,734 Gates	220	
	C8700UHB	8,768 Gates	188	
	C6000UHB	6,000 Gates	163	
	C4100UHB	4,174 Gates	163	Output current options:
0.9 ns typ./1.4 ns max.	C3000UHB	3,066 Gates	149	3.2 mA, 12 mA, and 24 mA
12 mA Balanced Output	C2200UHB	2,220 Gates	123	Absolute number of outputs will
1.5μ Dual-Well CMOS	C1700UHB	1,724 Gates	108	be determined by the output
2-Layer Metal	C1200UHB	1,233 Gates	92	current option.
	C830UHB	830 Gates	76	
	C530UHB	530 Gates	66	
	C330UHB	336 Gates	60	
UH Series Gate Arrays				
1.0 ns typ./1.5 ns max.	C20000UH	20,160 Gates	220 w/Optional	Internal Clock Drivers,
1.5μ Dual-Well CMOS			Output Drive:	Scan Test, Auto-Test
3-Layer Metal			3.2 mA/6.3 mA	Program Generation
UM Series Gate Arrays				
	C15006UM	15,120 Gates + RAM	219 w/Optional	6,144 bits RAM
			Output Drive:	4 x (24 x 64) Single Port
1.0 ns typ./1.5 ns max.			3.2 mA/6.4 mA	4 x (18 x 64) Dual Port
1.5μ Dual-Well CMOS				
3-Layer Metal	C10012UM	10,080 Gates + RAM	219 w/Optional	12,288 bits RAM
			Output Drive:	2 ea. 4 x (24 x 64) Single Port
			3.2 mA/6.4 mA	2 ea. 4 x (24 x 64) Dual Port

AV Series Gate Arrays	Part Number	Basic Cells	I/O Count	Special Functions
	C8000AV	8,000 Gates	160	
1.4 ns typ. 2.2 ns. max.	C660AV	6,664 Gates	160	Standard I/O options include
1.8μ CMOS	C5000AV	5,022 Gates	142	TTL compatible, Schmitt trigger,
2-Layer Metal	C3900AV	3,900 Gates	127	and tri-state functions.
	C2600AV	2,640 Gates	106	
AVB Series Gate Arrays				
	C2000AVB	2,052 Gates	92	
1.4 ns typ./2.2 ns max.	C1600AVB	1,674 Gates	76	All AVB outputs have buffered
10 mA Buffered Output	C1200AVB	1,245 Gates	68	high output current options.
1.8μ CMOS	C850AVB	852 Gates	60	
2-Layer Metal	C540AVB	549 Gates	50	*Special low voltage AVL
Low Voltage Option	C350AVB	357 Gates	42	versions are available
AVM Series Gate Arrays				
1.4 ns typ./2.2 ns max.	C4002AVM	4,087 Gates + RAM	146	2,304 Bits RAM or 4,608 Bits ROM
1.8μ CMOS	C2301AVM	2,375 Gates + RAM	124	1,024 Bits RAM or 2,048 Bits ROM
2-Layer Metal	C1502AVM	1,564 Gates + RAM	114	2,304 Bits RAM or 4,608 Bits ROM

AU Series Gate Arrays	Part Number	Basic Cells	I/O Count	Special Functions
0.7 ns Typ./1.1 ns max.	C100kAU	102,144 Gates	332	
Enhanced Sea-of-Gates	C30kAU	31,500 Gates	178	Output current options:
12 mA Output Capability	C75kAU	75,140 Gates	300	3.2 mA and 12 mA
1.2μ Dual-Well CMOS	C50kAU	52,164 Gates	257	16K RAM (single and multi-port),
3-Layer Metal	C40kAU	41,184 Gates	220	64K ROM, registers available

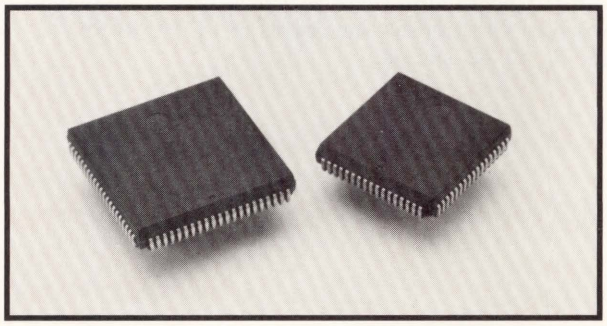
FUJITSU ASIC PACKAGING

CURRENT FUJITSU PACKAGES

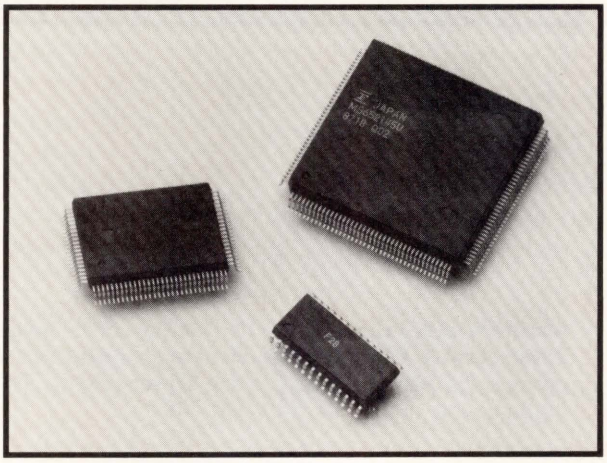
We provide you with the industry's widest range of state-of-the-art plastic and ceramic packages for ASICs. Our packages are all designed internally so Fujitsu can offer you the packaging technology that is unparalleled in the ASIC world. Choose from our selection of surface mount and thru-hole PGAs, LCCs, FPTs, and DIPs for your ASICs — it's ready for you today.

Our broad selection of packages was developed specifically to meet your ASIC needs. Fujitsu is the industry leader in packages for both surface mount and thru-hole technologies. These packages represent our committment in providing you with the best that is available today.

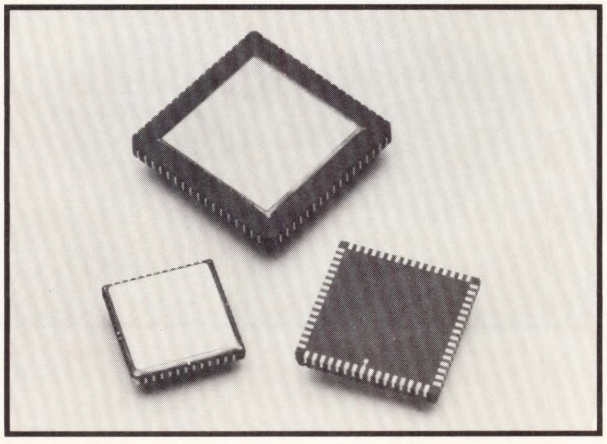
FUJITSU, THE LEADER IN SURFACE MOUNT PACKAGES



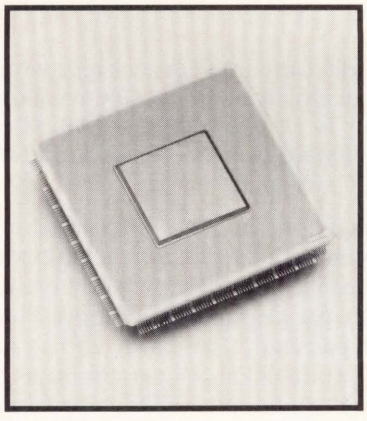
Plastic Leaded Chip Carriers offer flexibility of being able to be surface mounted or socketed. Available in pin counts of 28, 44, 68, and 84.



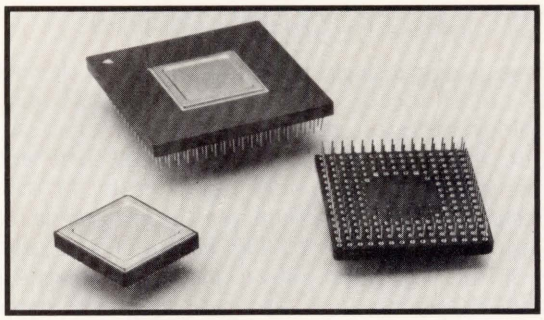
Plastic Flat Packages feature high pin densities for surface mounting with ease of lead inspection. Available in pin counts of 16, 20, 24, 28, 44, 48, 64, 70, 80, 100, 120, and 160.



Ceramic Leadless Chip Carriers offer capability for hermetically sealed surface mounting. Available in pin counts of 28, 48, 64, 68, and 84.



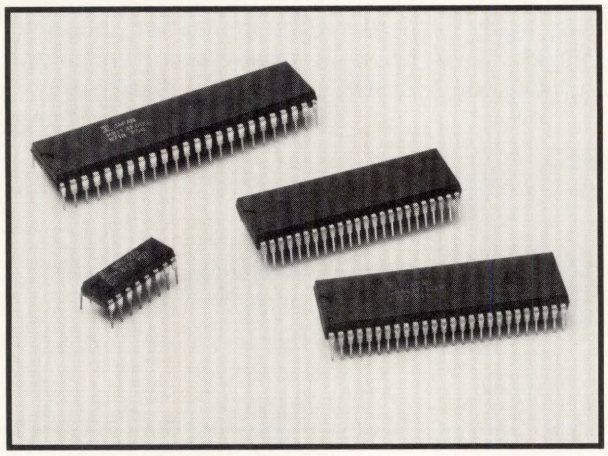
Ceramic Flat Packages offer high pin densities with complete hermetic seal. They have high power dissipation capability that makes this package useable for both CMOS and ECL applications. Available in pin counts of 48, 80, 100, 120, 160, 164, and 260.



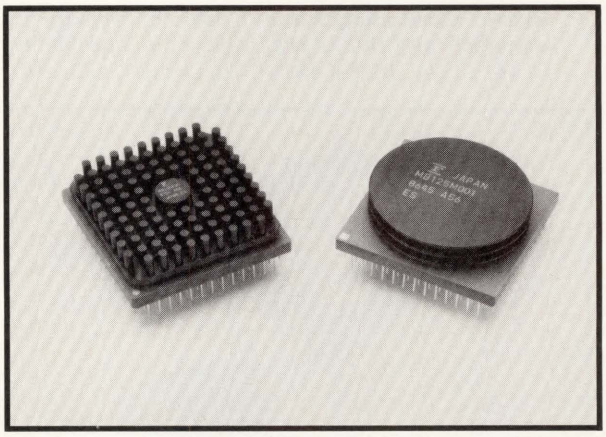
Plastic and Ceramic Pin Grid Arrays with both thru-hole and surface mount capability are available. They feature high pin counts and reliability with available pin counts of 64, 88, 107, 135, 149, 179, 208, and 256.

FUJITSU ASIC PACKAGING

FUJITSU'S THRU-HOLE PACKAGES



Plastic and Ceramic Dual In-line-Packages are the least expensive and most flexible for thru-hole designs. They are offered in standard form factor as well as shrink and skinny form factors with available pin counts of 14, 16, 18, 20, 22, 24, 28, 40, 42, 48, and 64.



Standard ECL Packages are used in thru-hole applications. These ceramic PGA packages offer two standard heat sink options: Pin Fin (left) and Cooling Tower (right). Available in pin counts of 88, 121, 149, and 208.

FUTURE ASIC PACKAGING TRENDS

Fujitsu is aggressively pursuing long-term development efforts on advanced semiconductor and ASIC packaging technology. Areas of concentration are in high lead count ceramic quad-flat packages; fine-pitch, surface mount ceramic pin-grid arrays; very high density plastic quad-flat packages; high pin count plastic pin-grid arrays; and tape automated bonding (TAB). Fujitsu is currently developing 25-mil lead pitch plastic quad-flat packages in both 200-and 240-pin versions. Also in development are ceramic quad-flat packages with 12.5-mil lead pitch and lead counts of well over 300.

A major development program is under way to enhance our current line of surface mounted ceramic pin-grid array packages. A ceramic surface mount PGA package (with over 400 pins on 50-mil spacing) is in an accelerated development program. Fujitsu is also developing TAB assembly technology to accommodate over 500 leads for advanced CMOS and bipolar ASIC products.

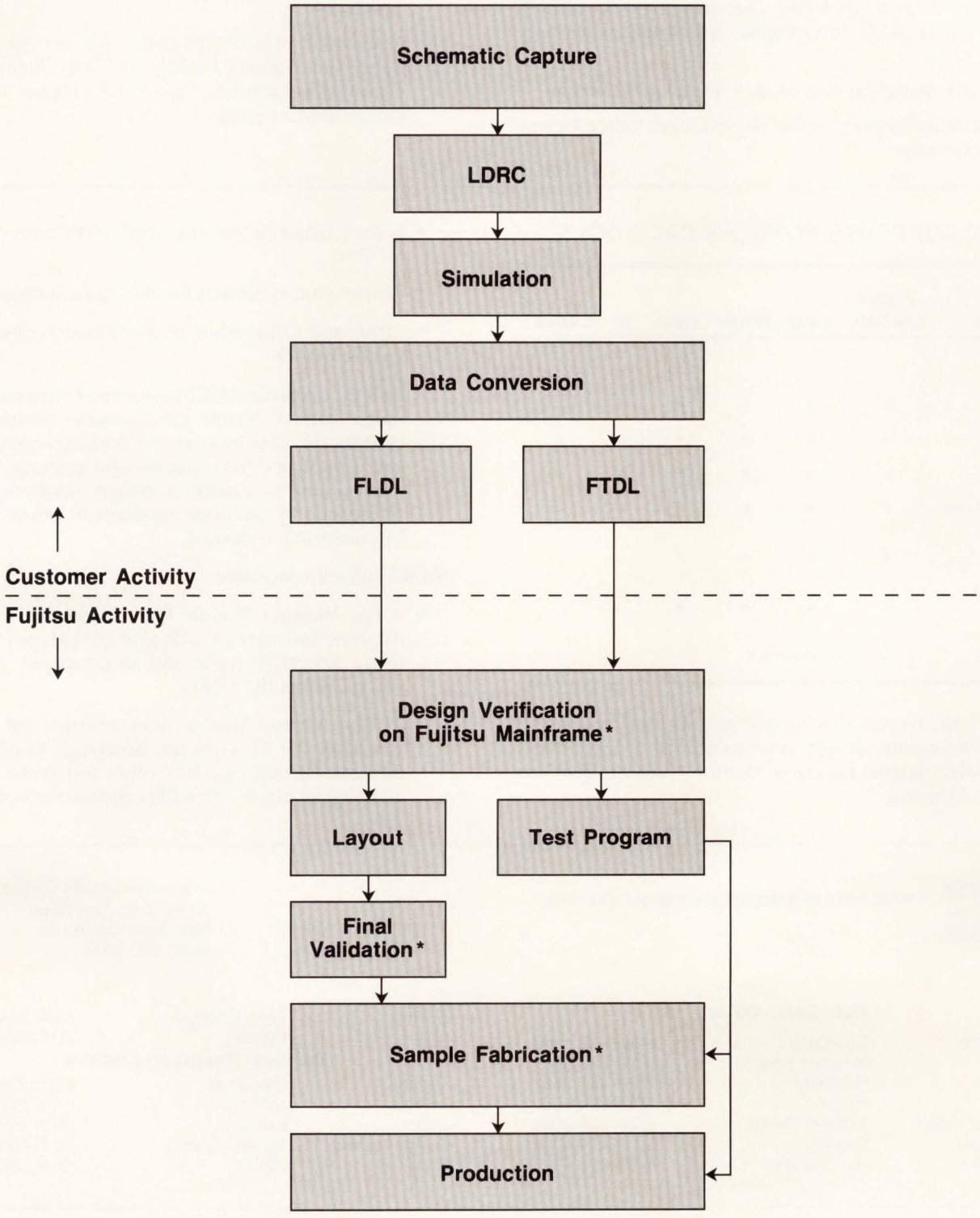
This advanced packaging technology is required to take advantage of future generations of ASIC semiconductor devices whose performance would be severely limited by existing conventional packaging technology. Fujitsu's extensive and broad packaging research efforts assure timely availability of reliable and cost-effective packaging for all future high pin-count or high performance requirements.

FUJITSU

FUJITSU ASIC DESIGN FLOW

for

ViewCAD™ and Popular Workstations



*Requires customer approval of output.

FUJITSU ASIC DESIGN SUPPORT

Fujitsu provides design support for all its ASIC technologies and architectures with both **ViewCAD** software and Fujitsu ASIC Design Kits.

ViewCAD is Fujitsu's comprehensive computer-aided-design software written in "C" and developed by Fujitsu for use on UNIX™ platforms that support XWindow™. **ViewCAD** is available from Fujitsu Microelectronics, Inc. and it includes:

- A Schematic Capture Module utilizing XWindow
- A Timing Diagram or Waveform Entry Module for test vector entry.
- A Logic Design Rule Check Module (LDRC) that screens for design violations such as fanout and drive, gate count, I/O requirements, etc.
- An Interactive Simulation Module that replicates the Fujitsu mainframe for both functional and timing simulation.
- Conversion Modules to define the net list and test vectors in Fujitsu's formats of FLDL (Fujitsu Logic Description Language) and FTDL (Fujitsu Test Data Description Language).

FUJITSU SUPPORTS POPULAR CAD TOOLS

Technology	*Fujitsu ViewCAD™*	*Daisy*	*Mentor*	*Valid*	*HP*	*LASAR™*
CMOS						
AU 1.2μ	•	•	•	•	•	—
UH 1.5μ	•	•	•	•	—	•
UHB 1.5μ	•	•	•	•	•	•
Standard Cell	•	•	•	•	•	—
ECL	•	•	•	•	—	—
BiCMOS	•	•	•	•	—	—

• Available — Under development

Fujitsu ASIC Design Kits are available for designers using some of the popular design tools on generic workstations. The kits offer support for Daisy, Mentor, Valid and HP (see Table) and include:

- Fujitsu Libraries for the tool's Schematic Capture Module
- Fujitsu Timing Models for the tool's simulator
- LDRC and Conversion Modules as described above for **ViewCAD**
- **FAME**™ (Fujitsu's ASIC Management Environment), a menu driven design management program that enables the user to select technology, approximate gate count and I/O, pinout and package requirements, and to create a design database that is referenced by the other modules to assure correct-by-construction designs.

FAME software includes:

- A File Manager Module that checks the schematic database and timing models for consistency with the menu selections made and automatically compiles and performs the LDRC.
- A Test Vector Module that creates test vectors automatically for complex functions, assists in defining test groupings, cycle times and strobe settings, and checks created test files against restrictions.

FUJITSU **FUJITSU MICROELECTRONICS, INC.**

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HARRIS Technology Overview

The Harris Semiconductor Custom Integrated Circuits Division (CICD) develops and manufactures custom and semicustom integrated circuits for use in the Strategic, Tactical and Space environments. Particular emphasis is placed on Radiation Hardened, High Performance, High Reliability and Classified applications. CICD capabilities include Bipolar, Digital and Analog, CMOS Digital and Analog and combinations of these technologies on the same integrated circuit, all of which are offered as standard products, custom and semicustom design and production capabilities, and foundry services.

The technologies offered by CICD are summarized below:

CICD Process Technologies

- MOS Process Technologies
  - ➤ Silicon Gate CMOS and PMOS
  - ➤ Metal Gate CMOS and PMOS
  - ➤ MNOS (Non-volatile Memory Element)
- Bipolar Digital Capabilities
  - ➤ Dielectric and Junction Isolation Technologies
  - ➤ Advanced Low Power Schottky Logic Family
  - ➤ Schottky Transistor Logic Family
- Analog Capabilities
  - ➤ Complementary Bipolar Dielectric Isolation
  - ➤ CMOS and JFETs Added to Bipolar Processes
  - ➤ Laser Trimmed Precision Thin Film Resistors
  - ➤ Analog CMOS
- Gallium Arsenide
  - ➤ Discrete Gain and Power GaAs FETs
  - ➤ Digital MSI and SSI Logic Functions
  - ➤ Monolithic Microwave Integrated Circuits (MMICs)
  - ➤ Microwave Amplifiers
  - ➤ Semicustom Logic Arrays

Harris processes are summarized in the table below. Note that Harris CMOS processes are Self Aligned gate, Junction Isolated processes, hence the names SAJI I, IV, etc.

HARRIS CICD PROCESS FEATURE SIZE SUMMARY

Process	Minimum Feature Size (Drawn Microns)	Rad Tol/Rad-Hard	Levels of Metal
MOS			
PMOS	7.5		1
MGCMOS (metal gate)	7.5		1
SAJI I	5.0	RT/RH	1
SAJI IV	3.0	RT/RH	1
Scaled SAJI IV	2.5	RT/RH	1
SAJI IVA (A/D)	3.0		1
SAJI VH	2.0	RH	2
RH-7 (VHSIC-LIKE) (A/D)	1.2	RH	2
L7.5	1.5	RT	2
Gamma III	1.2	RH	2
S7	1.2	RT	2
BIPOLAR			
High Freq. Process (HFP)	5.0	RH	1
BIMOS*	2.0		1
Advanced Low Power Schottky	4.0	RH	1
Linear ALPS	4.0	RH	1
High Current Linear (HCL)	5.0	RH	1
Very High Freq. Process (VHFP)	4.0	RH	2
GaAs			
DIGI-1,-11	1.0		
MMIC	.5		

SEMICONDUCTOR PRODUCTS DIVISION

Harris Semiconductor offers a wide selection of standard analog and digital circuits through its Semiconductor Products Division. This includes a large selection of Standard Radiation-Hardened data sheet products.

HARRIS SEMICONDUCTOR • P.O. Box 883 • Melbourne, Florida 32902-0883 • (407) 724-7872

* Available end of CY '89

HARRIS

HSC1000

SEMICUSTOM

August 1988

Dual Level Metal CMOS Standard Cell Library

Features

- **Low Power CMOS Process**
- **1.5 Micron Channel Lengths (1.0 Micron Effective)**
- **Dual Level Metal Interconnect**
- **800ps Typical 2-Input Nand Gate Delay with a Fanout = 2**
- **100MHz Flip-Flop Toggle Frequency**
- **Supports Gate Counts to 25K**
- **Over 200 Primitive and Macrocell Functions**
- **Complex Function Megacells**
- **RAM and ROM Module Compilers**
- **Supported on Harris Architect™, Daisy™ and Mentor Graphics® Design Systems**
- **CMOS/TTL Compatible I/O's**
- **Commercial-Industrial-Military Temperature Ranges**
- **Proven Reliable and Manufacturable Process**
- **Extensive Packaging Options**
- **Screening and Qualification to Mil-Std-883C Method 5004/5005, Class B**
- **Function Compatible with the HSC1000RH Radiation Hardened Library**

Description

The Harris HSC1000 Standard Cell Library is a family of high performance 1.5 micron dual level metal, silicon gate standard cells. The library consists of a family of variable width primitive cells with which a large number of MSI and complex function megacells have been implemented. RAM and ROM compilers are available which allow the user to implement exact configuration of RAM and ROM for a particular application. The HSC cell library meets all military requirements and is forward compatible with other Harris cell libraries. Designs implemented with the HSC1000 library may be ported to the HSC1000RH library for radiation hardened requirements.

The library is supported on Harris Architect™, Daisy™ and Mentor Graphics®. A complete set of design tools allows the designer to capture, simulate, and verify that the design goals are met. The layout software organizes the chip as rows of cells separated by the exact number of routing channels required for interconnection of the cells. This approach minimizes chip area for cost efficient, high performance designs.

The HSC primitives are a group of 110 custom designed cells that represent the basic design functions most commonly used by a chip designer. These cells are the lowest level at which the designer may work. They include basic gates such as nands, nors, and inverters as well as flip flops and latches. These cells have been optimized for area and performance. Each cell is designed such that rise and fall propagation times have been matched to minimize skew.

The 74XX functions are offered for those designers who feel more comfortable designing with a standard logic family. All of the 74XX functions are soft coded cells implemented with the HSC primitives. The functionality of the 74XX family has been preserved and matches that of the HCMOS family.

The complex function megacells are a family of highly integrated functions which allow the designer to more efficiently implement commonly used LSI functions.

The I/O cells offer the designer fast on and off chip propagation times. High output drive is offered allowing the chip to drive 100pF loads in minimum time

Packaging

Harris Semiconductor offers a wide variety of plastic and ceramic dual-in-line packages, leadless and leaded chip carriers, flatpacks and pin grid arrays. The table illustrates the types of packages and pin count options available. For additonal information or packaging requirements not shown in this table, please contact a factory representative.

PACKAGING	PIN COUNT
Plastic DIP	14 - 48
Ceramic DIP	14 - 64
Plastic Leaded Chip Carrier	20 - 84
Ceramic Leaded Chip Carrier	14 - 164
Ceramic Leadless Chip Carrier	18 - 84
Ceramic PGA	68 - 180

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

HARRIS

HSC1000RH

SEMICUSTOM

August 1988

Radiation Hardened Dual Level Metal CMOS Standard Cell Library

Features

- Low Power CMOS Process
- 2.0 Micron Channel Lengths (1.25 Micron Effective)
- Dual Level Metal Interconnect
- Guaranteed Hardened Against Radiation
  - Total Dose ..... $>2 \times 10^5$ Rad-Si
  - Data Upset ..... $>1 \times 10^9$ Rad-Si/s
  - Latch-Up Free to ..... $>1 \times 10^{12}$ Rad-Si/s
  - Functional After 10^6 Total Dose Radiation
- 800ps Typical 2-Input Nand Gate Delay with a Fanout = 2
- 100MHz Flip-Flop Toggle Frequency
- Supports Gate Counts to 13K
- Over 200 Primitive and Macrocell Functions
- Complex Function Megacells
- Supported on Harris Architect™, Daisy™ and Mentor Graphics® Design Systems
- CMOS/TTL Compatible I/O's
- Military Temperature Ranges
- Proven Reliable and Manufacturable Process
- Extensive Packaging Options
- Screening and Qualification to Mil-Std-883C Method 5004/5005, Class B
- Function Compatible with the HSC1000 Non-Radiation Hardened Library

Description

The Harris HSC1000RH Standard Cell Library is a family of high performance 2.0 micron dual level metal, radiation hardened, silicon gate standard cells. The library consists of a family of variable width primitive cells with which a large number of MSI and complex function megacells have been implemented. The HSC cell library meets all military requirements and is forward compatible with other Harris cell libraries.

The library is supported on Harris Architect™, Daisy™ and Mentor Graphics® platforms. A complete set of design tools allows the designer to capture, simulate, and verify that the design goals are met. The layout software organizes the chip as rows of cells separated by the exact number of routing channels required for interconnection of the cells. This approach minimizes chip area for cost efficient, high performance designs.

The HSC primitives are a group of 110 custom designed cells that represent the basic design functions most commonly used by a chip designer. These cells are the lowest level at which the designer may work. They include basic gates such as nands, nors, and inverters as well as flip flops and latches. These cells have been optimized for area and performance. Each cell is designed such that rise and fall propagation times have been matched to minimize skew.

The 74XX functions are offered for those designers who feel more comfortable designing with a standard logic family. All of the 74XX functions are soft coded cells implemented with the HSC primitives. The functionality of the 74XX family has been preserved and matches that of the HCMOS family.

The complex function megacells are a family of highly integrated functions which allow the designer to more efficiently implement commonly used LSI functions.

The I/O cells offer the designer fast on and off chip propagation times. High output drive is offered allowing the chip to drive 100pF loads in minimum time.

Packaging

Harris Semiconductor offers a wide variety of plastic and ceramic dual-in-line packages, leadless and leaded chip carriers, flatpacks and pin grid arrays. The table illustrates the types of packages and pin count options available. For additonal information or packaging requirements not shown in this table, please contact a factory representative.

PACKAGING	PIN COUNT
Plastic DIP	14 - 48
Ceramic DIP	14 - 64
Plastic Leaded Chip Carrier	20 - 84
Ceramic Leaded Chip Carrier	14 - 164
Ceramic Leadless Chip Carrier	18 - 84
Ceramic PGA	68 - 180

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

HARRIS Digital Architect™

SEMICUSTOM

August 1988

Design System

Features

- **Supports Harris Standard Cell, Gate Array* and Compiled Functions***
- **Schematic Capture and Simulation for SSI, MSI, LSI Macrofunctions and RAM/ROM Compilers Available Now**
- **Complete System including Place and Route and Layout Verification Planned for 1989**
- **Based on the CADENCE Design Framework™, Providing Consistent, Menu-driven Interfaces for All Tools**
- **1.5 Micron Non-rad-hard (HSC1000) and Two Micron Rad Hard (HSC1000RH) Libraries Are Available Today**
- **CADAT™ Logic and Fault Simulation Capabilities Include Min/Typ/Max Delays for All Functions. Post Radiation Simulation Supported for HSC1000RH**
- **Back Annotation of Fanout and Routed Delays**
- **Harris-Customized CADENCE Design Framework™ Allows Use on Most UNIX Platforms**
- **Scheduled for QML (Generic Qualification) in Calendar Year 1990**
- **Supports EDIF Netlist Input**

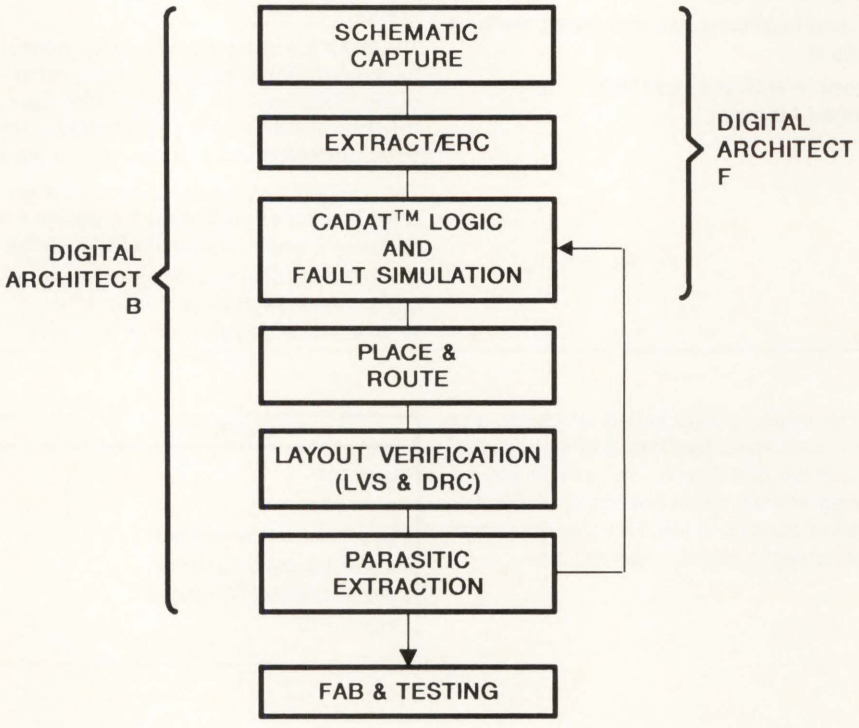
Description

The Harris Digital Architect Design System provides schematic capture, design verification and place and route capability for Harris HSC cell families. This toolkit is based on the CADENCE Design Framework™ and has been used successfully for many HSC cell-based designs. The Harris Digital Architect Design System is the toolset that Harris uses internally to design standard products and to process customer designs captured on other workstations such as Daisy or Mentor.

After placement and routing, parasitics are back-annotated to the CADAT simulator for a final simulation and critical paths are identified, evaluated and modified if necessary. The Harris Digital Architect Design System supports the entire design process from design capture through PG tape generation.

Two versions of the Harris Digital Architect Design System are available; a schematic capture and design verification system called Digital Architect F, and a complete front to back system, Digital Architect B.

Design Flowchart



Additional Information is Available in the Harris Digital Architect Design System Users Guide.

Digital Architect™ is a Trademark of Harris Corporation

*Gate Array Support Planned for Q2, 1989, Compiler Support Provided as a Harris Custom Service.

CADENCE Design Framework™ is a Trademark of CADENCE Systems, CADAT™ is a Trademark of HHB Systems

HARRIS

Bipolar Analog Architect™

August 1988

Design System

Features

- Full Custom Bipolar Transistor-Level Analog IC Design Capability
- Runs on Industry Standard Workstation Platforms
- Menu-Driven Interface
- Hierarchical Schematic Capture
- Coupled Electrical and Physical Design Features
- Electrical Design Rules Checking and Layout vs. Schematic Checking
- Continuously Variable Diffused and Thin Film Resistors
- Automatic Device Model Parameter Determination
- Self-Contained Statistical Process/Device Data Bases
- A Variety of High Performance Bipolar Analog Processes
- Continuously Variable Transistor Geometries
- Based on the CADENCE Design Framework™
- Powerful Electrical Statistical Simulation Capability
- Automatic Layout Generation
- Layout Modifications and Parasitics Automatically Back Annotated to Schematics

Shippable Product Forms

- Unprobed Wafers With Untested Packaged Prototypes
- Tested Dice
- Tested Packaged Parts
- All Wafers Delivered in Unprobed Circuit Form Are Probed For Conformance to Process/Device Parameter Limits

Description

The Bipolar Analog Architect Design System is a comprehensive, self-contained software system for the full custom design of analog circuits using bipolar technology. This package contains all tools necessary to perform both the electrical and physical design of an analog IC using Harris proprietary wafer fabrication processing. The package also contains a complete statistical description of the process being used, allowing a comprehensive statistical analysis of circuit performance using built-in Monte Carlo procedures.

In this system, no structural geometries are predetermined. The geometry of transistors and other circuit elements is determined by the user, according to the individual application, using built-in software.

The electrical design system includes software tools for design capture, device design, electrical simulation, and data analysis. The physical design system provides tools for layout graphics editing, layout to schematic checking, layout groundrule checking, and parasitic extraction.

A variety of wafer fabrication processes will eventually be incorporated into the system, allowing the designer to use various combinations of Bipolar, JFET, analog switching CMOS and digital CMOS technology in the solution of system design problems. These will be continuously augmented as new processes are developed at Harris, assuring the user continued access to state-of-the-art technology.

General Purpose Process

Features

- Dielectrically Isolated
- Complementary Vertical Bipolar Transistors
- P Channel JFET
- Various Diffused Resistors
- Laser Trimmable NiCr Resistors
- High Quality Capacitor

TYPICAL DEVICE CHARACTERISTICS

	NPN	PNP
BVCEO	40V	40V
HFE	250	125
F_T	750MHz	400MHz

High Frequency Process

Features

- Dielectrically Isolated
- Complementary Vertical Bipolar Transistors
- Double Level Metal Interconnect
- P Channel JFET
- Various Diffused Resistors
- Laser Trimmable NiCr Resistors
- High Quality Capacitor

TYPICAL DEVICE CHARACTERISTICS

	NPN	PNP
BVCEO	20V	20V
HFE	150	125
F_T	1.2GHz	1.0GHz

HARRIS

CMOS Analog Architect™

August 1988

Design System

Features

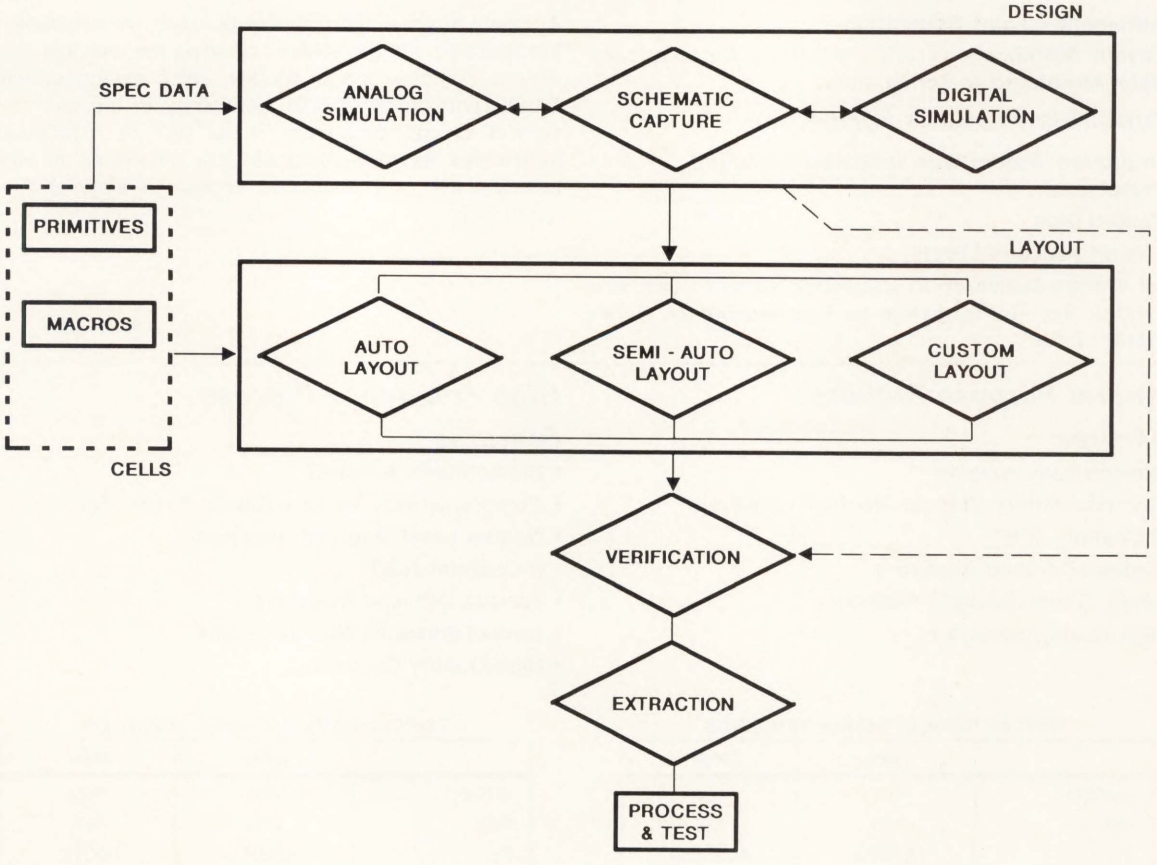
- **Provides a Path to Quick-turn, High Confidence Analog ASICs**
- **Supports Switched Capacitor Design Techniques Allowing a Wide Range of Analog Functions**
- **Supported by the Harris HCAD 10-Volt Analog and Digital Cell Family**
- **SWITCAP™ and SLICE* Simulations Allow Accurate Prediction of Final Circuit Performance**
- **Typical Level of Integration is 50 Op-Amps**
- **Available as a Harris Custom Capability**
- **Harris-Customized CADENCE Design Framework™ Allows Use on Most UNIX Platforms**

Description

The Harris CMOS Analog Architect Design System provides schematic capture, design verification, netlisting and place and route capability for the Harris HCAD analog/digital cell family. These tools are supported on a Harris-modified CADENCE Design Framework™ and have been used successfully for several HCAD cell-based designs. At the present time the CMOS Analog Architect Design System is used internally to perform designs to a customer specification.

The primary library is composed of a full set of analog primitive cells optimized for sampled data design methods. Also available are higher level macros (filter structures and programmable amplifiers for example) which help reduce design cycle time through the use of interactive auto place and route techniques.

Design Flow



Additional Information is Available in the CMOS Analog Architect Users Guide and HCAD Library Datasheet From Harris.

Lattice Semiconductor Corporation™

GAL®16V8A

Ultra High-Speed E²CMOS™ Generic Array Logic

FEATURES

- **HIGH PERFORMANCE E²CMOS™ TECHNOLOGY**
  - 12 ns Maximum Propagation Delay
  - Fmax = 62.5 MHz
  - 10 ns Maximum from Clock Input to Data Output
  - TTL Compatible 24 mA Outputs
  - UltraMOS® III Advanced CMOS Technology
- **50% REDUCTION IN POWER**
  - 75mA Typ I_{cc}
- **E² CELL TECHNOLOGY**
  - Reconfigurable Logic
  - Reprogrammable Cells
  - 100% Tested/Guaranteed 100% Yields
  - High Speed Electrical Erasure (<50ms)
  - 20 Year Data Retention
- **EIGHT OUTPUT LOGIC MACROCELLS**
  - Maximum Flexibility for Complex Logic Designs
  - Programmable Output Polarity
  - Also Emulates 20-pin PAL® Devices with Full Function/Fuse Map/Parametric Compatibility
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
  - 100% Functional Testability
- **APPLICATIONS INCLUDE:**
  - DMA Control
  - State Machine Control
  - High Speed Graphics Processing
  - Standard Logic Speed Upgrade
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

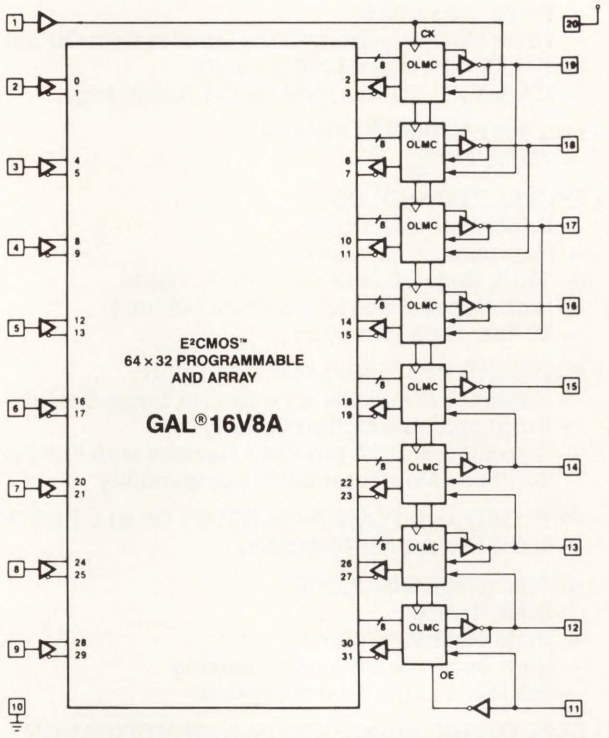
DESCRIPTION

The GAL®16V8A, at 12 ns maximum propagation delay time, combines a high performance CMOS process with Electrically Erasable (E^2) floating gate technology to provide the highest speed performance available in the PLD market. CMOS circuitry allows the GAL®16V8A to consume just 75ma typical I_{cc} which represents a 50% savings in power when compared to its bipolar counterparts. The E^2 technology offers high speed (50ms) erase times providing the ability to reprogram or reconfigure the devices quickly and efficiently.

The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. An important subset of the many architecture configurations possible with the GAL®16V8A are the PAL® architectures listed in the table on the right. The GAL®16V8A is capable of emulating any of these PAL® architectures with full function/fuse map/parametric compatibility.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. Therefore, LATTICE guarantees 100% field programmability and functionality of all GAL® products. LATTICE also guarantees 100 erase/rewrite cycles and that data retention exceeds 20 years.

FUNCTIONAL BLOCK DIAGRAM



GAL®/PAL COMPARISON—12/15ns DEVICES

PART TYPE	GAL®16V8A ARCHITECTURE EMULATION 115ma	PAL®16xx AVAILABILITY 115ma	PAL®16xx AVAILABILITY 180ma
16L8	✔		✔
16H8	✔		
16R8	✔		✔
16R6	✔		✔
16R4	✔		✔
16P8	✔		
16RP8	✔		
16RP6	✔		
16RP4	✔		
10L8	✔		
12L6	✔		
14L4	✔		
16L2	✔		
10H8	✔		
12H6	✔		
14H4	✔		
16H2	✔		
10P8	✔		
12P6	✔		
14P4	✔		
16P2	✔		
16V8	✔		

LATTICE SEMICONDUCTOR CORP., PO BOX 2500, PORTLAND, OREGON 97208-2500, U.S.A.
Tel. (503) 681-0118; 1-800-FASTGAL
0888/WCP/5K/EC

August 1988

Lattice Semiconductor Corporation™

GAL®20V8A

Ultra High-Speed E²CMOS™ Generic Array Logic

FEATURES

- **HIGH PERFORMANCE E²CMOS™ TECHNOLOGY**
  - — 12 ns Maximum Propagation Delay
  - — Fmax = 62.5 MHz
  - — 10 ns Maximum from Clock Input to Data Output
  - — TTL Compatible 24 mA Outputs
  - — UltraMOS® III Advanced CMOS Technology
- **50% REDUCTION IN POWER**
  - — 75mA Typ I_{cc}
- **E² CELL TECHNOLOGY**
  - — Reconfigurable Logic
  - — Reprogrammable Cells
  - — 100% Tested/Guaranteed 100% Yields
  - — High Speed Electrical Erasure (<50ms)
  - — 20 Year Data Retention
- **EIGHT OUTPUT LOGIC MACROCELLS**
  - — Maximum Flexibility for Complex Logic Designs
  - — Programmable Output Polarity
  - — Also Emulates 24-pin PAL® Devices with Full Function/Fuse Map/Parametric Compatibility
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
  - — 100% Functional Testability
- **APPLICATIONS INCLUDE:**
  - — DMA Control
  - — State Machine Control
  - — High Speed Graphics Processing
  - — Standard Logic Speed Upgrade
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

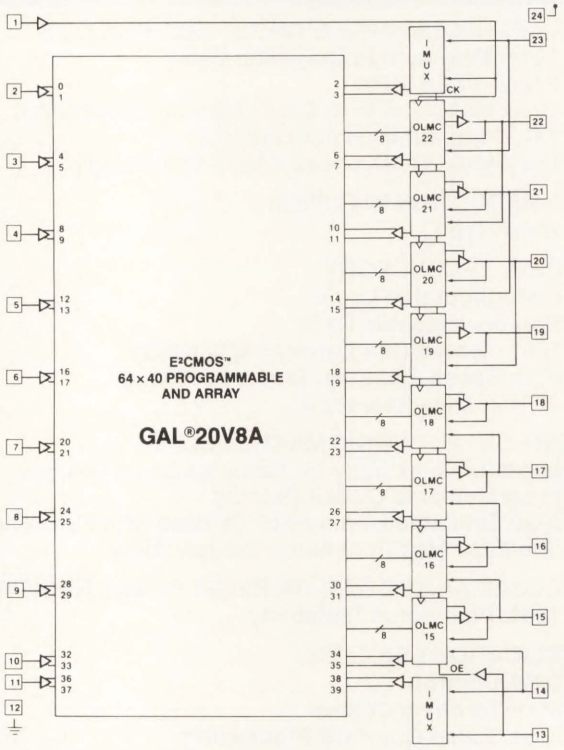
DESCRIPTION

The GAL®20V8A, at 12 ns maximum propagation delay time, combines a high performance CMOS process with Electrically Erasable (E^2) floating gate technology to provide the highest speed performance available in the PLD market. CMOS circuitry allows the GAL®20V8A to consume just 75ma typical I_{cc} which represents a 50% savings in power when compared to its bipolar counterparts. The E^2 technology offers high speed (50ms) erase times providing the ability to reprogram or reconfigure the devices quickly and efficiently.

The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. An important subset of the many architecture configurations possible with the GAL®20V8A are the PAL® architectures listed in the table on the right. The GAL®20V8A is capable of emulating any of these PAL® architectures with full function/fuse map/parametric compatibility.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. Therefore, LATTICE guarantees 100% field programmability and functionality of all GAL® products. LATTICE also guarantees 100 erase/rewrite cycles and that data retention exceeds 20 years.

FUNCTIONAL BLOCK DIAGRAM



GAL®/PAL COMPARISON—12/15ns DEVICES

PART TYPE	GAL®20V8A ARCHITECTURE EMULATION 115ma	PAL®20xx AVAILABILITY 115ma	180ma
20L8	✔		✔
20H8	✔		
20R8	✔		✔
20R6	✔		✔
20R4	✔		✔
20P8	✔		
20RP8	✔		
20RP6	✔		
20RP4	✔		
14L8	✔		
16L6	✔		
18L4	✔		
20L2	✔		
14H8	✔		
16H6	✔		
18H4	✔		
20H2	✔		
14P8	✔		
16P6	✔		
18P4	✔		
20P2	✔		
20V8A	✔		

LATTICE SEMICONDUCTOR CORP., PO BOX 2500, PORTLAND, OREGON 97208-2500 U.S.A.
Tel. (503) 681-0118 or 1-800-FASTGAL; FAX (503) 681-3037

August 1988

Lattice Semiconductor Corporation

GAL®6001

Generic Array Logic

PRELIMINARY

FEATURES

- **ELECTRICALLY ERASABLE CELL TECHNOLOGY**
  - **— Instantly Reconfigurable Logic**
  - **— Instantly Reprogrammable Cells**
  - **— Guaranteed 100% Yields**
- **HIGH PERFORMANCE E²CMOS™ TECHNOLOGY**
  - **— Low Power: 90mA Typical**
  - **— High Speed: 15ns Max. Clock to Output Delay**
    25ns Max. Setup Time
    30ns Max. Propagation Delay
- **TTL COMPATIBLE INPUTS AND OUTPUTS**
- **UNPRECEDENTED FUNCTIONAL DENSITY**
  - **— 10 Output Logic Macro Cells**
  - **— 8 State Logic Macro Cells**
  - **— 20 Input and I/O Logic Macro Cells**
- **HIGH-LEVEL DESIGN FLEXIBILITY**
  - **— 78 x 64 x 36 FPLA Architecture**
  - **— Separate State Register and Input Clock Pins**
  - **— Functionally Supersets Existing 24-pin PAL® and IFL™ Devices**
  - **— Asynchronous Clocking**
- **SPACE SAVING 24-PIN, 300-MIL DIP**
- **HIGH SPEED PROGRAMMING ALGORITHM**
- **20-YEAR DATA RETENTION**

DESCRIPTION

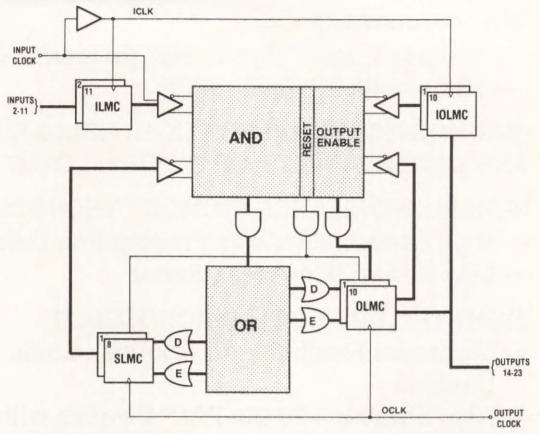
Using a high performance E²CMOS™ technology, Lattice Semiconductor has produced a next-generation programmable logic device, the GAL®6001. Having an FPLA architecture, known for its superior flexibility in state-machine design, the GAL®6001 offers the highest degree of functional integration, flexibility, and speed currently available in a 24-pin, 300-mil package.

The GAL®6001 has 10 programmable Output Logic Macrocells (OLMC) and 8 programmable "buried" State Logic Macrocells (SLMC). In addition, there are 10 input Logic Macrocells (ILMC) and 10 I/O Logic Macrocells (IOLMC). Two clock inputs are provided for independent control of the input and output macrocells.

Advanced features that simplify programming and reduce test time, coupled with E²CMOS™ reprogrammable cells, enable 100% AC, DC, programmability, and functionality testing of each GAL®6001 during manufacture. This allows Lattice to guarantee 100% performance to specifications. In addition, data retention of 20 years and a minimum of 100 erase/write cycles are guaranteed.

Programming is accomplished using standard hardware and software tools. In addition, an Electronic Signature word is available for storage of user specified data, and a security cell is provided to protect proprietary designs.

FUNCTIONAL BLOCK DIAGRAM



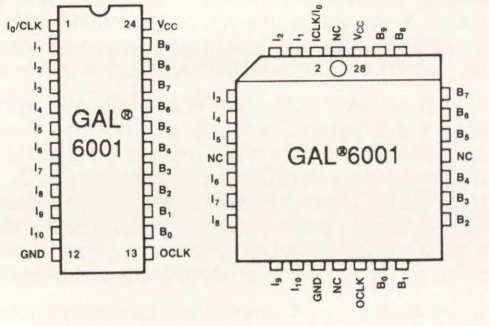
MACRO CELL NAMES

ILMC	INPUT LOGIC MACRO CELL
IOLMC	I/O LOGIC MACRO CELL
SLMC	STATE LOGIC MACRO CELL
OLMC	OUTPUT LOGIC MACRO CELL

PIN NAMES

I_0-I_{10}	INPUT	B_0-B_9	BIDIRECTIONAL
ICLK	INPUT CLOCK	V_{CC}	POWER (+5)
OCLK	OUTPUT CLOCK	GND	GROUND

PIN CONFIGURATION



JUNE 1988

LATTICE SEMICONDUCTOR CORP. P.O. BOX 2500, PORTLAND, OR 97208

APPLICATIONS HOTLINE: 1-800-FASTGAL

Lattice Semiconductor Corporation

ispGAL™ 16Z8

In-System re-Programmable
GENERIC ARRAY LOGIC

ADVANCED INFORMATION

FEATURES

- **IN-SYSTEM RECONFIGURABLE—5-VOLT ONLY PROGRAMMING**
  - **— Change Logic "On the Fly" (in less than 1 s)**
  - **— Nonvolatile E² Technology**
- **DIAGNOSTICS MODE FOR CONTROLLABILITY AND OBSERVABILITY OF SYSTEM LOGIC**
- **HIGH PERFORMANCE E²CMOS™ TECHNOLOGY**
  - **— High Speed: 25ns Max Propagation Delay**
  - **— Low Power: 90mA Max Active**
- **EIGHT OUTPUT LOGIC MACROCELLS**
  - **— Maximum Flexibility for Complex Logic Designs**
  - **— Also Emulates 20-pin PAL® Devices with Full Function/Fuse Map/Parametric Compatibility**
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
  - **— 100% Functional Testability**
- **SPACE SAVING 24-PIN, 300-MIL DIP**
- **MINIMUM 10,000 ERASE/WRITE CYCLES**
- **DATA RETENTION EXCEEDS 10 YEARS**
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**
- **APPLICATIONS INCLUDE:**
  - **— Reconfigurable Interfaces**
  - **— Copy Protection and Security Schemes**
    - **— erasable hardware**
    - **— password systems**
    - **— proprietary hardware/software interlocks**

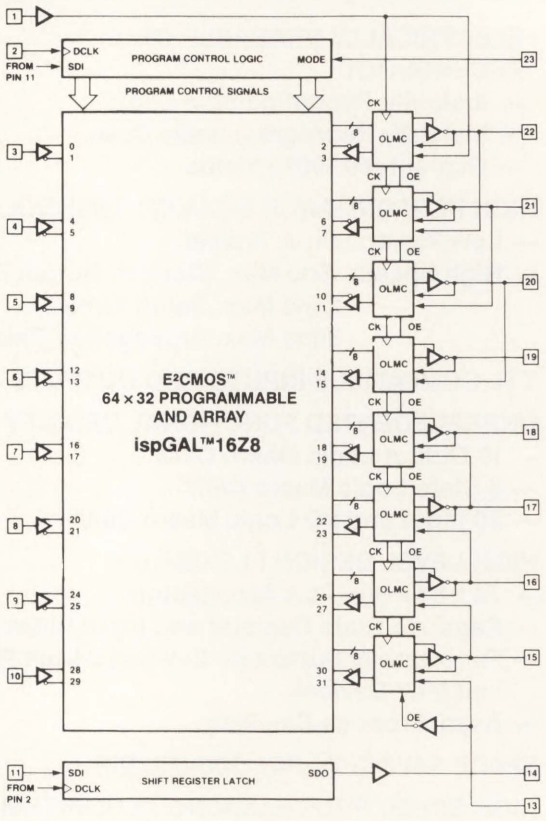
DESCRIPTION

The LATTICE ispGAL™16Z8 is a revolutionary programmable logic device featuring 5-volt only in-system reprogrammability and real time, in-system diagnostic capabilities. This is made possible by on-chip circuitry which generates and shapes the necessary high voltage internal programming control signals. Using LATTICE UltraMOS® technology, this device provides true bipolar performance at significantly reduced power levels.

The 24-pin ispGAL™16Z8 is architecturally and parametrically identical to the 20-pin GAL®16V8, but includes 4 extra pins to control in-system programming. These extra pins are: data clock (DCLK), serial data in (SDI), serial data out (SDO), and mode control (MODE). These pins are not associated with normal logic functions and are used only during programming. Additionally, this 4-pin interface allows an unlimited number of devices to be cascaded to form a serial programming and diagnostics loop.

Advanced features that simplify programming and reduce test time, coupled with E²CMOS™ reprogrammable cells, enable complete AC, DC, programmability, and functionality testing of each ispGAL™16Z8 during manufacturing and allows LATTICE to guarantee 100% performance to all specifications.

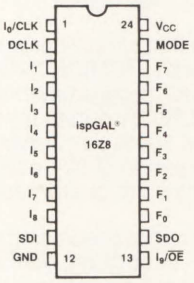
FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

I_0-I_{15}	INPUT	MODE	MODE CONTROL
CLK	CLOCK INPUT	DCLK	DATA CLOCK
B_0-B_5	BI-DIRECTIONAL	SDI	SERIAL DATA IN
F_0-F_7	OUTPUT	SDO	SERIAL DATA OUT
$\overline{G}(\overline{OE})$	OUTPUT ENABLE	V_{CC}	POWER (+5V)
GND	GROUND		

PIN CONFIGURATION



FEBRUARY, 1988

LATTICE SEMICONDUCTOR CORP. P.O. BOX 2500, PORTLAND, OR 97208
APPLICATIONS HOTLINE: 1-800-FASTGAL

Mitsubishi CMOS Gate Arrays

SOLID SEMICONDUCTOR FOUNDATION

Mitsubishi Electric Corporation markets and sells semiconductor products in the United States and Canada through Mitsubishi Electronics America, Inc.-Semiconductor Division with headquarters in Sunnyvale, California.

According to Dataquest, Mitsubishi Electric is among the top ten semiconductor suppliers in the world, offering a broad line of semiconductor products. Additionally, Mitsubishi companies are diversified into areas including heavy industry, chemicals and consumer products marketed worldwide.

A sister company to Mitsubishi Electronics America, Inc., Mitsubishi Semiconductor America, Inc. in Durham, North Carolina provides U.S. assembly of DRAMs. Major design centers for gate arrays and standard cells are also located at Mitsubishi companies in Sunnyvale and in Durham.

Mitsubishi is a major worldwide DRAM supplier. Current development of 4 and 16 megabit DRAM products will provide advanced technology for ASIC design.

In 1987, Mitsubishi Semiconductor America, Inc. broke ground for an ASIC fabrication facility. Development and production of 1.3 μm and 1.0 μm CMOS gate arrays and standard cells for U.S. customers is slated to start at this facility in early 1989.

FEATURES

- 1.3 μm (M6002X, M6003X, M6004X) and 2 μm (M6001X) CMOS processes.
- Broad density range: 200–20,000 useable gates
- Extensive variety of packages:
  - — PLCC
  - — QFP
  - — DIP
  - — SOP
  - — Shrink DIP
  - — Ceramic PGA
  - — Tape-Automated Bonding Pin-Grid-Array (TAB PGA)
  - — Mounted Pin-Grid-Array (MPGA)*
- High quality and reliability
  - — 100% burn-in
  - — 100% electrical (AC and DC) and functional testing
- Mitsubishi's patented gate isolation structure** allows 15% faster performance and 20% higher gate density than conventional oxide isolation.
- Variable Track Master (VTM) architecture provides effective implementation of memory on chip.
- Flexible design support with a library of over 280 macros.
- All popular engineering workstations are supported: Mentor Graphics,® Valid Logic,™ Daisy,™ Hewlett Packard,® IKOS,™ Intergraph,™ FutureNet® and OrCAD.™

DESCRIPTION

Mitsubishi offers four families of CMOS gate arrays with an extensive selection of packages and gate capacities.

1.3μm CMOS Gate Arrays

M6002X Series — A family of conventional channeled architecture arrays with sizes from 224 to 2,400 useable gates.

M6003X Series — A family of large gate arrays, in sizes of 3,200 to 20,000 useable gates. These arrays use Mitsubishi's Variable Track Masterslice (VTM) architecture which provides variable size routing channels and efficient use of gates for flexible RAM and ROM cells.

M6004X Series — Two array sizes from the M6003X family are offered in TAB (Tape-Automated-Bonding) packaging for a high I/O count. Sizes now available are 4,100 gates (182 I/Os) and 6,300 gates (220 I/Os).

2.0μm CMOS Gate Arrays

M6001X Series — A family of conventional architecture arrays using the 2 μm CMOS process in sizes ranging from 500 to 8,000 gates.

1.0 μm CMOS Gate Arrays

Mitsubishi will offer 1.0μm gate arrays by the end of 1988. Sizes will include 15,000, 25,000, 35,000 and 50,000 useable gates. These arrays are designed with Variable Track Masterslice architecture and will use the same library cells and CAD tools available for other Mitsubishi gate array families.

*Available end of 1988.
**U.S. Patent No. 4,562,453.

REGIONAL SALES OFFICES

NORTHWEST
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15612 Highway 7, #243
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800 N. Bierman Circle
Mt. Prospect, IL 60056
Phone: 312-298-9223

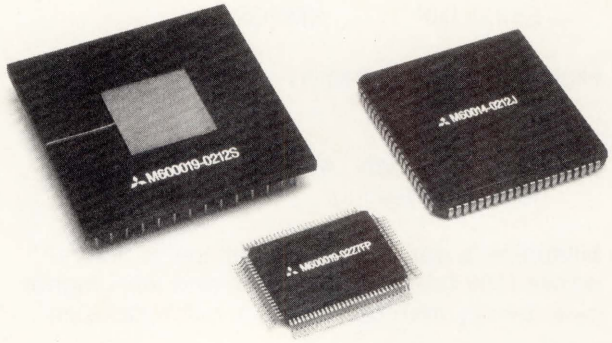
MITSUBISHI ELECTRONICS

Mitsubishi 1.3μm CMOS GATE ARRAYS
M6002X, M6003X, and M6004X Series

Part Number[1][2]			M60020	M60021	M60022	M60023	M60024	M60025	M60030	M60031	M60032	M60034	M60035	M60037	M60041	M60042
Number of Gates			224	507	800	1104	1773	2400	4788	7308	10836	20412	25200	47376	7308	10836
Number of Equivalent Gates			—	—	—	—	—	—	3200	4100	6300	8400	11000	20000	4100	6300
Maximum I/O Ports			22	32	42	48	62	72	88	110	132	180	196	256	182	220
Maximum Number Pin Pairs[3]			390	630	930	1200	1750	2190	2790	3650	5910	7045	9450	17180	3650	5910
Total Number Basic Cells[4]			672	1521	2400	3312	5319	7200	9600	12300	18900	25200	33000	60000	12300	18900
Maximum Number Useable Basic Cells[5]			570	1292	2040	2815	4522	6120	8160	9840	15120	20160	26400	48000	9840	15120
Package Type	**Lead Spacing**	**Pins**														
Plastic DIP	100 mil	16[6]	•													
		20[6]	•	•	•											
		28[7]	•	•	•	•										
Plastic Shrink DIP	70 mil	42		•	•	•	•	•	•							
		52			•	•	•	•	•							
		64						•	•	•	•	•				
Small Outline Package (SOP)	50 mil	24	•	•	•											
		36		•	•											
Plastic Flat Package (FP)	1.0mm	44			•	•	•	•								
	1.0mm	64				•	•	•	•	•						
	0.8mm	80					•	•	•	•	•	•				
	0.65mm	100							•	•	•	•	•			
	0.8mm	128								•	•	•	•			
	0.65mm	160										•	•			
Plastic Leaded Chip Carrier (PLCC)	50 mil	44		•	•	•	•	•								
		52				•	•	•	•							
		68					•	•	•	•	•	•				
		84						•	•	•	•	•	•			
Tape-Automated-Bonding Pin-Grid-Array (TAB PGA)	100 mil	208													•	•
		256														•
Ceramic Pin-Grid-Array (PGA)	100 mil	177														
		209											•			
		281												•		

(1) M60002X Series is conventional (channel) architecture.
(2) M60003X Series is Variable Track Masterslice (VTM) architecture.
(3) A pin pair is a cell-to-cell interconnect. The total number of pin pairs is limited for each gate array. Exceeding this limit means the automatic routing of the interconnect may be difficult.
(4) A basic cell is the pair of corresponding p and n transistors from which the array is constructed. Three basic cells are equivalent to a 2-input NAND gate.
(5) Maximum utilization with random logic.
(6) 300 mil body only available.
(7) 600 mil body only available.

The dots shown in this chart indicate packages now in production. Please contact your local Mitsubishi sales office for information on additional package/array combinations.



Mitsubishi CMOS Gate Arrays

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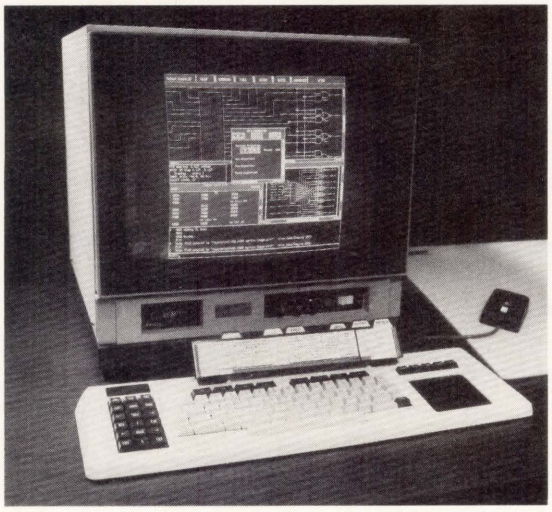
Mitsubishi 2μm CMOS GATE ARRAYS
M6001X Series

Part Number			M60011	M60012	M60013	M60014	M60015	M60016	M60017	M60018	M60019
Number of Gates			500	810	1100	1680	2666	3608	4814	6233	8096
Maximum I/O Ports			64	82	96	116	132	148	176	178	190
Maximum Number Pin Pairs(1)			720	980	1220	1660	2380	3210	4120	5820	7000
Total Number Basic Cells(2)			1500	2431	3300	5040	8000	10824	14442	18700	24288
Maximum Number Useable Basic Cells			1275	2066	2805	4284	6800	9200	12275	14960	19066
Package Type	**Lead Spacing**	**Pins**									
Plastic DIP	100 mil	16(3)	•								
		18(3)	•								
		20(3)	•								
		24(5)	•	•	•	•	•	•	•		
		28(4)	•	•	•	•	•	•	•		
		40(4)	•	•	•	•	•	•	•		
		42(4)	•	•	•	•	•	•	•		
Plastic Shrink DIP	70 mil	42	•	•	•	•	•	•	•		
		52	•	•	•	•	•	•	•		
		64	•	•	•	•	•	•	•	•	•
Ceramic Pin-Grid-Array (PGA)	100 mil	124						•	•	•	•
		209						•	•		•
Plastic Flat Package (FP)	1.0mm	44	•	•	•	•					
	1.0mm	64	•	•	•	•	•	•			
	0.8mm	80	•	•	•	•	•	•	•	•	•
	0.65mm	100		•	•	•	•	•	•	•	•
	0.8mm	128					•	•	•	•	•
	0.65mm	160								•	•
Plastic Leaded Chip Carrier (PLCC)	50 mil	44	•	•	•						
		52	•	•	•	•	•				
		68		•	•	•	•	•	•		
		84		•	•	•	•	•	•	•	•

(1) A pin pair is a cell-to-cell interconnect. The total number of pin pairs is limited for each gate array. Exceeding this limit means the automatic routing of the interconnect may be difficult.
(2) A basic cell is the pair of corresponding p and n transistors from which the array is constructed. Three basic cells are equivalent to a 2-input NAND gate.
(3) 300 mil body only available.
(4) 600 mil body only available.
(5) 600 and 300 mil available.

The dots shown in this chart indicate packages now in production. Please contact your local Mitsubishi sales office for information on additional package/array combinations.



CAD Workstation for Gate Array Designs

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NORTHWEST
1050 East Arques Avenue
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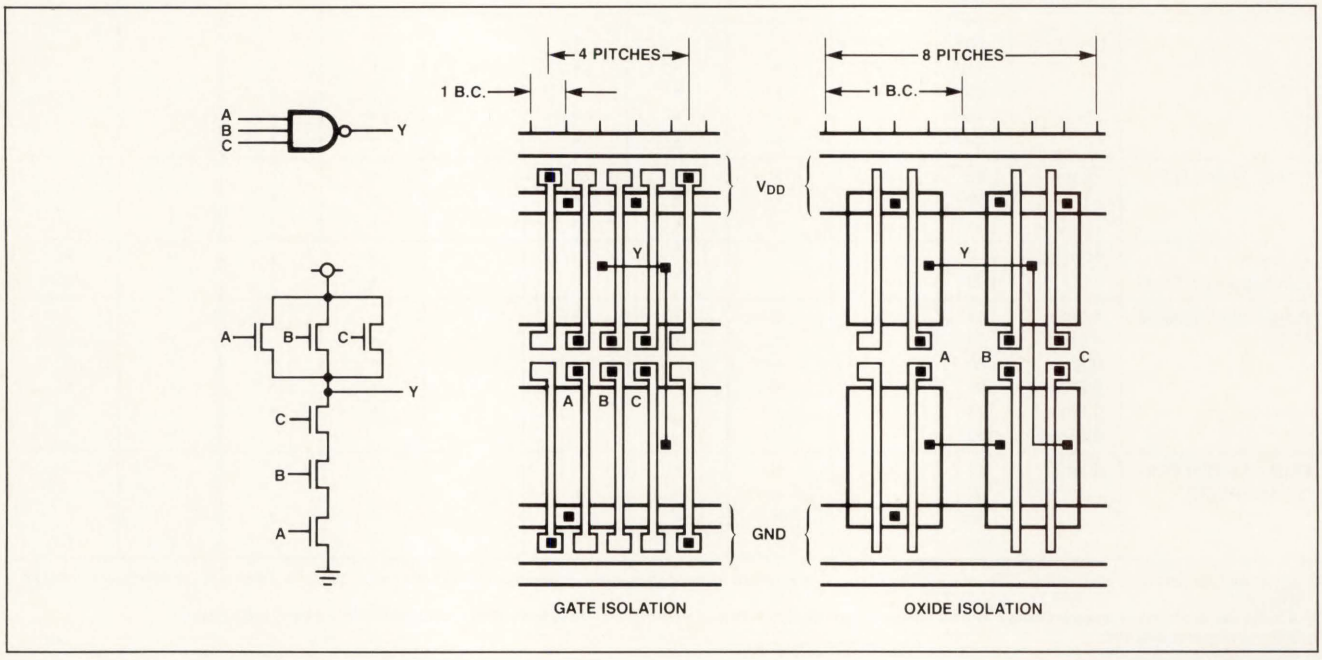
DESIGN INNOVATION

Gate Isolation

Mitsubishi gate arrays are designed using a patented* gate isolation structure developed at Mitsubishi's LSI Labs.

The layout drawing of a three-input NAND, shown below, shows the benefits of this process. Gate isolation is achieved in four "pitches" as compared to the eight required for the conventional oxide-isolation process. The ability to use individual "basic cells" (pairs of N– and P– transistors), rather than groups of two-input NAND gates results in higher gate utilization.

Overall, gate isolation results in a more compact design, and lower interconnect capacitance so that circuit performance is better than the conventional oxide isolation process. The example of the three input NAND gate shows a 50% improvement in density. Other cells average about 30% density increase. Performance improvements *of 10 to 20%* are also realized as a result of shorter interconnect lines.

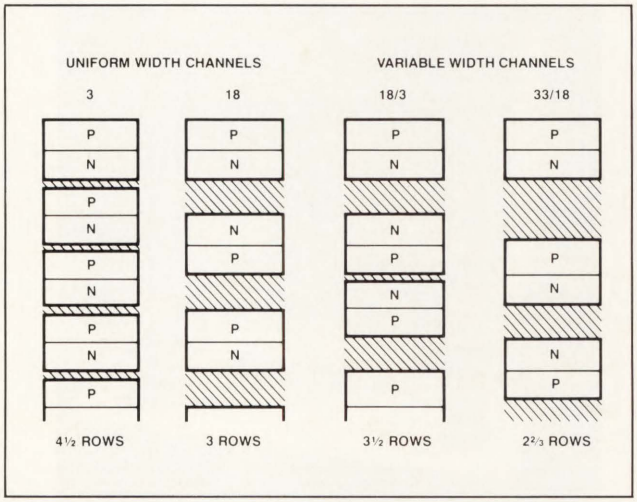


Variable Track Masterslice (VTM)

The M6003X family uses the variable track masterslice (VTM) architecture developed by Mitsubishi. This architecture provides flexible width routing channels by allowing a tradeoff between rows of transistors and routing space.

The array leaves room for three lines between transistor rows which is sufficient for the row and column lines of a memory cell. As more routing is needed, rows of n– or p– transistors are sacrificed for interconnect. The place and route software can make variable sizes of routing channels, depending upon need.

The largest array in Mitsubishi's VTM family has about 300,000 transistors, which is equivalent to 50,000 gates. Utilization depends on the mix of random-logic and repetitive functions, such as memory/shift registers. Random logic can achieve at least 40% utilization of the array while ROM or RAM can achieve 100% utilization.



*U.S. Patent No. 4,562,453.

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QUALITY AND RELIABILITY

Data from the high volume process used for Mitsubishi's static RAMs assures tight process control and high quality/reliability for ASIC products.

All Mitsubishi gate array products (except prototypes) undergo a high temperature (125°C), high voltage (7 volts), static burn-in. The duration of burn-in is varied according to the maturity of the product and product line.

All products, including prototypes, are 100% tested functionally and to AC and DC specifications.

Mitsubishi uses proprietary I/O protection techniques to enhance ESD and latch-up immunity. When tested with 1500 ohms of series resistance, Mitsubishi's gate arrays withstand discharges of over +2000 volts from a 100pF capacitor. Current surges of 200mA on the power pin can be tolerated without latch-up.

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Symbol	Parameter	Limits		Unit
		Min	Max	
V_{DD}	Supply Voltage	$V_{SS}-0.3$	7.0	V
V_I	Input Voltage	$V_{SS}-0.3$	$V_{DD}+0.3$	V
V_O	Output Voltage	$V_{SS}-0.3$	$V_{DD}+0.3$	V
I_O	Output Current(1)		10	mA
I_O	Output Current(2)		20	mA
I_O (T)	Total Output Current		100	mA
Topr	Operating Temperature	−20	75	°C
Tstg	Storage Temperature	−55	150	°C
	Electrostatic Discharge(3)	−2000	2000	V

Recommended Operating Conditions

Symbol	Parameter	Limits		Unit
		Min	Max	
V_{DD}	Supply Voltage	4.5	5.5	V
Topr	Operating Temperature	−20	75	°C
V_I	Input Voltage	0	V_{DD}	V
V_O	Output Voltage	0	V_{DD}	V
I_O	Output Current per Output(1)		7	mA
I_O	Output Current per Output(2)		14	mA
C_L	Output Load Capacitance		50	pF
I_O (T)	Total Output Sink Current		80	mA
I_O (T)	Total Output Source Current		40	mA

DC Characteristics

Symbol	Parameter	Test Conditions	Limits		Unit
			Min	Max	
V_{IL}	Input Voltage (TTL Interface)	$V_{DD}=4.5V$	0	0.8	V
V_{IH}		$V_{DD}=5.5V$	2.2	5.5	
V_{IL}	Input Voltage (CMOS Interface)	$V_{DD}=4.5V$	0	1.35	V
V_{IH}		$V_{DD}=5.5V$	3.85	5.5	
VT−	Input Voltage Schmitt Trigger (TTL Interface)	$V_{DD}=5V$	0.7	1.65	V
VT+			1.3	2.1	
VH			0.3	1.2	
VT−	Input Voltage Schmitt Trigger (CMOS Interface)	$V_{DD}=5V$	0.85	2.5	V
VT+			2.3	3.7	
VH			0.5	1.6	
V_{OL}	Output Voltage	$V_{DD}=5V$, $I_O=0mA$		0.1	V
V_{OH}			4.9		
I_{OL}	Output Current(1)	$V_{OL}=0.4V$, $V_{DD}=4.5V$	6		mA
I_{OH}		$V_{OH}=4.1V$, $V_{DD}=4.5V$	−2		
I_{OL}	Output Current(2)	$V_{OL}=0.4V$, $V_{DD}=4.5V$	14		mA
I_{OH}		$V_{OH}=4.1V$, $V_{DD}=4.5V$	−5		
I_I	Input Leakage Current	$V_I=V_{DD}$, V_{SS}	−1	+1	μA
I_{OZ}	Output Leakage Current	$V_O=V_{DD}$, V_{SS}	−1	+1	μA
RU	Pull-up Resistor(1)	$V_{DD}=5V$, $V_I=0V$	50	500	kΩ
RD	Pull-down Resistor(1)	$V_{DD}=5V$, $V_I=5V$	50	500	kΩ
RU	Pull-up Resistor(2)	$V_{DD}=5V$, $V_I=0V$	23	230	kΩ
RD	Pull-down Resistor(2)	$V_{DD}=5V$, $V_I=5V$	16	160	kΩ

(1) M6001X Series
(2) M6002X, M6003X and M6004X Series
(3) Electrostatic discharge is measured from a 100pF capacitor through 1500Ω.

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Minnetonka, MN 55345
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800 N. Bierman Circle
Mt. Prospect, IL 60056
Phone: 312-298-9223

Typical AC Characteristics (V_{DD} = 5V, T_{opr} = 25°C, Fanout = 2, Metal = 1.0mm)

Parameter	Test Conditions	1.3μm (M6002X, M6003X)	2μm (M6001X)	Unit
2-Input NAND Gate Delay		0.9	1.4	nsec
Input Buffer Delay		1.2	1.4	nsec
Output Buffer Delay	Load: 20pF	3.5	5.5	nsec
	Load: 50pF	4.8	7.7	
	Load: 100pF	7	11.9	
Power Dissipation/Output Buffer	Load: 25pF	0.6	0.6	mW/MHz
	Load: 50pF	1.3	1.3	
	Load: 100pF	2.5	2.5	
Toggle Rate		175	100	MHz
Power Dissipation per Gate		10	15	μW/MHz
Input Pin Capacitance	f = 1MHz	8	8	pF
Output Pin Capacitance		8	8	
Bidirectional Pin Capacitance		8	8	

User Friendly CAD System for Error-Free Design

Mitsubishi offers a highly flexible system of design interface options. Starting with a schematic, we'll implement a design from schematic capture, simulation and timing verification through manufacturing and testing of prototypes. Designers can use Mentor Graphics,® Daisy,™ Valid Logic,™ FutureNet,™ Hewlett Packard,® Intergraph,™ IKOS,™ or OrCAD™ workstations with the powerful and user-friendly Mitsubishi CAD system to direct their own design. In addition, modem hook-ups using a terminal or PC with IBM® 3270 emulation are available. Mainframe access for simulation is also available via IBM-IN.® This provides for flexible remote access to the Mitsubishi CAD system for circuit design.

No matter how customers choose to interface, Mitsubishi will provide guidance as needed. There are design centers in Sunnyvale, California and Durham, North Carolina offering mainframe computer capability for development. Additional design support is offered at Mitsubishi regional office technical centers.

MITSUBISHI FLEXIBLE DESIGN INTERFACE

Mitsubishi Engineering Workstation Support

	Schematic Entry	Functional Simulation	Delay Simulation	Circuit Conversion	Test Pattern Conversion
Mentor "IDEA 1000®"	•	•	•	•	•
Daisy "LOGICIAN™"	•	•	•	•	•
Valid "SCALD™"	•	•	•	•	•
FutureNet "DASH/CADAT®"	•	•		•	•
Hewlett Packard®	•	•	•	•	•
Intergraph™	•	•	•	•	•
IKOS™		•	•	•	•
OrCAD™	•			•	

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THE MITSUBISHI GATE ARRAY CELL LIBRARY

Mitsubishi continues to expand its extensive cell library for easy development of a wide range of logic applications. The large number of TTL-compatible cells in Mitsubishi's library are ideally suited for applications where development of designs using TTL logic components, or conversion of existing TTL systems are required. Unique cells, such as ROM and RAM, provide even more flexibility for integrating functions which previously had to be implemented off-chip. ROM cells are not shown, since gate array ROM is created by a ROM compiler for the size needed.

The current library offers over 105 TTL-equivalent macrofunctions (soft macros) and over 175 hard macro cells.

On-Chip Configurable RAM and ROM

With Mitsubishi gate arrays, designers can configure various sizes of memory on-chip. Only the number of cells necessary to achieve the required word-length is used, leaving unused cells free to implement other logic. There is less wasted space, plus designers save the I/Os and access delays involved in interfacing off-chip. Mitsubishi's memory cells have typical access times of 20ns to 25ns for the 2μm family, and 15ns to 20ns for the 1.3μm family.

MACRO FUNCTIONS

Cell Name	LSTTL Equiv	Description	Basic Cells (1)	Pin Pairs (2)
T04200SA	LS42	BCD: Decimal Decoder	66	48
T04800SA	LS48	BCD: 7 Segment Decoder/Driver	146	95
T07500WA	LS75	4-Bit Through Latch	64	10
T08300WB	LS83	4-Bit Full Adder	137	74
T08301WA	LS83	4-Bit Full Adder	137	74
T08500WB	LS85	4-Bit Magnitude Comparator	194	113
T09000WA	LS90	Decade Counter	157	33
T09100SA	LS91	8-Bit Shift Register	171	22
T09101SA	LS91	8-Bit Shift Register	190	31
T09200WA	LS92	Divide-by-12 Counter	132	21
T09300SA	LS93	4-Bit Binary Counter	103	13
T09500WA	LS95	4-Bit Parallel Register	135	40
T09600WA	LS96	5-Bit Shift Register	157	33
T13700SA	LS137	3:8 Decoder/Demux with Latch	95	57
T13800SA	LS138	3:8 Decoder/Demux	60	42
T13800WA	LS138	3:8 Decoder/Demux	130	58
T13900SA	LS139	2:4 Decoder/Demux	54	34
T13901SA	LS139	2:4 Decoder/Demux	26	17
T14700WB	LS147	10-Dec: 4-BCD Priority Encoder	115	64
T14800WB	LS148	8:3 Priority Encoder	163	86
T15100WA	LS151	8:1 Data Selector/Mux	77	54
T15300WA	LS153	4:1 Data Selector/Mux	82	50
T15301SB	LS153	4:1 Data Selector/Mux	35	25
T15500SA	LS155	2-Bit Binary: 4-Dec Demux with Strobe	56	35
T15700SA	LS157	2:1 Data Selector/Mux	40	27
T15700WA	LS157	2:1 Data Selector/Mux	49	23
T15800WA	LS158	2:1 Data Selector/Mux	53	27
T16000WA	LS160	Synchronous Presettable Decade Counter with Reset	225	86
T16100WB	LS161	Synchronous Presettable 4-Bit Counter with Reset	212	80
T16200WA	LS162	Fully Synchronous Presettable Decade Counter	194	79
T16300WA	LS163	Synchronous 4-Bit Binary Counter	199	62
T16400SA	LS164	8-Bit Serial-In/Parallel-Out Shift Register	211	35
T16500WA	LS165	8-Bit Parallel-In/Serial-Out Shift Register	268	77
T16600WA	LS166	8-Bit Shift Register	247	71
T17300WA	LS173	4-Bit D-Type Register with 3-State Output	172	47
T17400SA	LS174	Hex D Flip-Flop with Reset	151	22
T17500SA	LS175	Quad D Flip-Flop with Reset	100	14
T18100SB	LS181	ALU/Function Generator	341	165
T18200SB	LS182	Look-Ahead Carry Generator	95	66
T19000WA	LS190	Synchronous Presettable Up-Down Decade Counter	288	106

MACRO FUNCTIONS

Cell Name	LSTTL Equiv	Description	Basic Cells (1)	Pin Pairs (2)
T19100WA	LS191	Synchronous Presettable Up-Down 4-Bit Counter	278	94
T19200WA	LS192	Synchronous Presettable Up-Down Decade Counter	230	230
T19300WA	LS193	Synchronous Presettable Up-Down 4-Bit Counter	229	89
T19400WB	LS194	4-Bit Bidirectional Universal Shift Register	208	86
T19500WA	LS195	Parallel Access Shift Register with Reset	176	47
T19600WA	LS196	Presettable Decade Counter/Latch	222	73
T19700SA	LS197	Presettable 4-Bit Binary Counter/Latch	192	59
T24800WA	LS248	BCD: 7-Segment Decoder/Driver	157	99
T25100WA	LS251	8:1 Data Selector/Mux with 3-State Output	100	52
T25700WA	LS257	2:1 Data Selector/Mux with 3-State Output	84	27
T25800WA	LS258	Quad 2:1 Data Selector/Mux with 3-State Output	71	27
T27300WA	LS273	Octal Positive Edge-Triggered D Flip-Flop with Reset	202	26
T28000WB	LS280	9-Bit Odd/Even Parity Generator/Checker	159	106
T28001WA	LS280	9-Bit Even Parity Generator/Checker	72	16
T28002WA	LS280	9-Bit Odd Parity Generator/Checker	72	16
T29500WA	LS295	4-Bit Shift Register with 3-State Output	162	40
T29800WA	LS298	Quad 2-Input Mux with Storage	122	31
T35200WA	LS352	Dual 4:1 Data Selector/Mux with Strobe	74	48
T35300WA	LS353	Dual 4:1 Data Selector/Mux with 3-State Output	94	52
T36700WA	LS367	Hex Bus Driver with 3-State Output	72	14
T36800WA	LS368	Hex Bus Driver with 3-State Output (Inverter)	84	20
T37300WA	LS373	Octal Positive Edge D Flip-Flop with 3-State Output	193	35
T37400WA	LS374	Octal Positive Edge D Flip-Flop with 3-State Output	287	42
T37700WA	LS377	Octal Positive Edge D Flip-Flop with Enable	244	61
T39000WA	LS390	Dual Decade Counter	135	23
T39300SA	LS393	Dual 4-Bit Binary Counter	214	44
T39500WA	LS395	4-Bit Cascadable Shift Register	179	48
T49000WA	LS490	Dual 4-Bit Decade Counter	165	35
T59500WA	LS595	8-Bit Shift Register/Latch with 3-State Output	451	66
T66800WA	LS668	Synchronous Presettable Up-Down Counter	285	110
T66900WB	LS669	Synchronous 4-Bit Up-Down Counter	261	111
T67001WB	LS670	4 x 4 Register Files with 3-State Output	505	113
T68401WA	LS684	8-Bit Magnitude Comparator	224	99
T68801WA	LS688	8-Bit Magnitude Comparator with Enable	130	46
M00100WB		16-Word x 32-Bit RAM	3123	650
M00200WB		32-Word x 32-Bit RAM	5461	1234
M00300WB		64-Word x 16-Bit RAM	5573	1338
M00400WB		128-Word x 8-Bit RAM	5643	1330

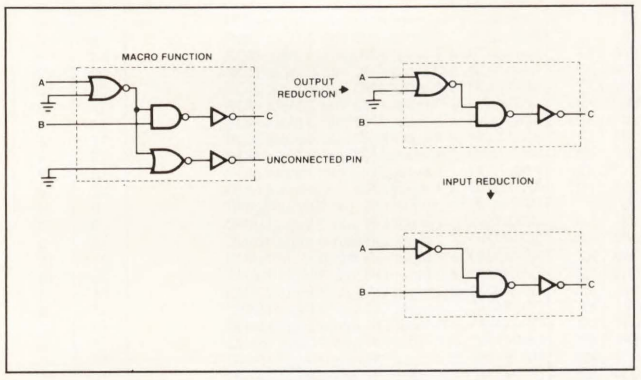
(1) A basic cell is the pair of corresponding p and n transistors from which the array is constructed. Three basic cells are equivalent to a 2-input NAND gate.
(2) A pin pair is a cell-to-cell interconnect. The total number of pin pairs is limited for each gate array. Exceeding this limit means the automatic routing of the interconnect may be difficult.

Automatic Logic Reduction

Mitsubishi's CAD system automatically implements logic reduction by eliminating unused cells from partially used macrofunctions.

The example below illustrates typical reduction resulting from unused inputs and outputs, which can be accomplished by our CAD system.

Logic Reduction: Example Using Mitsubishi's CAD System



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NORTH CENTRAL
800 N. Bierman Circle
Mt. Prospect, IL 60056
Phone: 312-298-9223

MACRO CELLS

Cell Name	Drive	Description	Basic Cells (1)	Pin Pairs (2)
V01S		Inverter	2	1
V01W	X2	Inverter	3	1
V01Q	X4	Inverter	5	1
KH1S		Driver, 3-State, Active High	7	2
KH4S		Driver, 3-State, Active High, 4-Bit	19	5
K0ZW	X2	Driver, 3-State, Active High	11	2
KL1S		Driver, 3-State, Active Low	7	2
KL4S		Driver, 3-State, Active Low, 4-Bit	19	5
K1ZW	X2	Driver, 3-State, Active Low	11	2
K1NS		Driver, Clock Line	3	1
K1NW	X2	Driver, Clock Line	4	1
K1NQ	X4	Driver, Clock Line	6	1
K2GW	X2	Driver, Clock Line, Gated	5	2
N02S		NAND, 2-Input	3	2
N02W	X2	NAND, 2-Input	7	2
N03S		NAND, 3-Input	4	3
N03W	X2	NAND, 3-Input	8	3
N04S		NAND, 4-Input	5	4
N04W	X2	NAND, 4-Input	9	4
N05S		NAND, 5-Input	6	5
N06W	X2	NAND, 6-Input	12	6
N08W	X2	NAND, 8-Input	14	8
N09W	X2	NAND, 9-Input	16	9
N12W	X2	NAND, 12-Input	19	12
N16W	X2	NAND, 16-Input	25	16
AN2S		AND, 2-Input	4	2
AN3S		AND, 3-Input	5	3
AN3W	X2	AND, 3-Input	6	3
AN4S		AND, 4-Input	6	4
AN4W	X2	AND, 4-Input	7	4
R02S		NOR, 2-Input	3	2
R02W	X2	NOR, 2-Input	7	2
R03S		NOR, 3-Input	4	3
R03W	X2	NOR, 3-Input	8	3
R04S		NOR, 4-Input	5	4
R04W	X2	NOR, 4-Input	9	4
R06W	X2	NOR, 6-Input	12	6
R08W	X2	NOR, 8-Input	14	8
R09W	X2	NOR, 9-Input	16	9
R12W	X2	NOR, 12 Input	19	12
R16W	X2	NOR, 16-Input	25	16
OR2S		OR, 2-Input	4	2
OR2W	X2	OR, 2-Input	5	2
OR3S		OR, 3-Input	5	3
OR3W	X2	OR, 3-Input	6	3
OR4S		OR, 4-Input	6	4
OR4W	X2	OR, 4-Input	7	4
XNOS		Exclusive NOR, 2-Input	6	2
XNOW	X2	Exclusive NOR, 2-Input	9	2
XORS		Exclusive OR, 2-Input	6	2
XORW	X2	Exclusive OR, 2-Input	9	2
S12S		Selector, 1 to 2	6	3
D12S		Selector, 1 to 2, Dual	10	4
S21B		Selector, 2 to 1	7	4
S21S		Selector, 2 to 1	5	4
D21S		Selector, 2 to 1, Dual	9	6
S24S		Selector, 2 to 1, 4-Bit	37	10
S34W	X2	Selector, 3 to 1, 4-Bit	41	14
S44W	X2	Selector, 4 to 1, 4-Bit	52	18
S41S		Selector, 4 to 1	17	10
A23S		AND-NOR, 2-Input AND into 2-Input NOR	4	3
A34S		AND-NOR, 3-Input AND into 2-Input NOR	5	4
A24S		AND-NOR, 2-Input AND into 3-Input NOR	5	4
A01S		OR-AND-NOR, 2-Input OR into 2-Input AND into 2-Input NOR	5	4
O23S		OR-NAND, 2-Input OR into 2-Input NAND	4	3
O34S		OR-NAND, 3-Input OR into 2-Input NAND	5	4
O24S		OR-NAND, 2-Input OR into 3-Input NAND	5	4
O01S		AND-OR-NAND, 2-Input AND into 2-Input OR into 2-Input NAND	5	4
T24S		AND-NOR, 2 2-Input AND into 2-Input NOR	5	4
T26S		AND-NOR, 3 2-Input AND into 3-Input NOR	8	6
T28W	X2	AND-NOR, 4 2-Input AND into 4-Input NOR	14	8
T2CW	X2	AND-NOR, 6 2-Input AND into 6-Input NOR	20	12
T2GW	X2	AND-NOR, 8 2-Input AND into 8-Input NOR	25	16
T36W	X2	AND-NOR, 2 3-Input AND into 2-Input NOR	11	6
T39W	X2	AND-NOR, 3 3-Input AND into 3-Input NOR	14	9
T3CW	X2	AND-NOR, 4 3-Input AND into 4-Input NOR	17	12
T48W	X2	AND-NOR, 2 4-Input AND into 2-Input NOR	13	8
T4CW	X2	AND-NOR, 3 4-Input AND into 3-Input NOR	18	12
T4GW	X2	AND-NOR, 4 4-Input AND into 4-Input NOR	22	16
U24S		OR-NAND, 2 2-Input OR into 2-Input NAND	5	4
U26S		OR-NAND, 3 2-Input OR into 3-Input NAND	8	6
U28W	X2	OR-NAND, 4 2-Input OR into 4-Input NAND	14	8
U2CW	X2	OR-NAND, 6 2-Input OR into 6-Input NAND	21	12
U2GW	X2	OR-NAND, 8 2-Input OR into 8-Input NAND	25	16
U36W	X2	OR-NAND, 2 3-Input OR into 2-Input NAND	11	6
U39W	X2	OR-NAND, 3 3-Input OR into 3-Input NAND	14	9
U3CW	X2	OR-NAND, 4 3-Input OR into 4-Input NAND	17	12
U48W	X2	OR-NAND, 2 4-Input OR into 2-Input NAND	13	8
U4CW	X2	OR-NAND, 3 4-Input OR into 3-Input NAND	17	12
U4GW	X2	OR-NAND, 4 4-Input OR into 4-Input NAND	22	16
LM1W	X2	AND-OR, 2 2-Input AND into 2-Input OR	8	4
LM2W	X2	AND-OR, 3 and 2-Input AND into 2-Input OR	9	5
FD1S		D Flip-Flop	19	2
FDBS		D Flip-Flop	18	2
FD1W	X2	D Flip-Flop	21	2
FD2S		D Flip-Flop, with Set	21	3
FDCS		D Flip-Flop, with Set	20	3
FD2W	X2	D Flip-Flop, with Set	23	3
FD3S		D Flip-Flop, with Reset	21	3
FDDS		D Flip-Flop, with Reset	20	3
FD3W	X2	D Flip-Flop, with Reset	23	3
FD4S		D Flip-Flop, with Set and Reset	23	4
FDES		D Flip-Flop, with Set and Reset	22	4
FD4W	X2	D Flip-Flop, with Set and Reset	25	4
FD7S		D Flip-Flop, with Reset, Positive Edge Triggered	23	3
FD7W	X2	D Flip-Flop, with Reset, Positive Edge Triggered	24	3
FD8W	X2	D Flip-Flop, with Set and Reset, Positive Edge Triggered	26	4
FDRS		D Flip-Flop, 4-Bit	63	5
FDSS		D Flip-Flop, 4-Bit, with Reset	75	6
FDQS		D Flip-Flop, 4-Bit, with Reset	85	5
FDFS		D Flip-Flop and Latch	22	3
FJBS		JK Flip-Flop	25	3
FJ3W	X2	JK Flip-Flop, with Reset, Master-Slave	28	4
FJ4W	X2	JK Flip-Flop, with Set and Reset, Master-Slave	30	5
FJAS		JK Flip-Flop, with Set and Reset, Positive Edge Triggered	32	4
FJ7W	X2	JK Flip-Flop, with Reset, Positive Edge Triggered	29	4
FDAS		D Latch, NAND Type	12	2
HL0S		D Latch, With Reset Active High, Inverted Output	12	3
HLAS		D Latch, With Reset Active Low	12	3
HLBS		D Latch	11	2
LF1S		D Latch, Hazard Free	12	2
LF1W	X2	D Latch, Hazard Free	14	2
LF4S		D Latch, 4-Bit, Hazard Free	52	5
LFAS		D Latch, 4-Bit	39	5
LFBS		D Latch, 4-Bit	40	5
FLAS		RS Latch, NAND Type	8	2
FLOS		RS Latch, NOR Type	8	2
FR1S		Shift Register, 4-Bit, Serial-In Parallel-Out	61	2
FR2S		Shift Register, 4-Bit, Serial-In Parallel-Out, with Synchronous Load	97	7
FR3S		Shift Register, 4-Bit Serial-In Parallel-Out, with Synchronous Load	82	7
SHAS		Adder, Half, 1-Bit	9	2
SFAS		Adder, Full, 1-Bit	18	3
SA2S		Adder, Full, 2-Bit	49	5
SA3S		Adder, Full, 2-Bit	41	5
FT7S		Counter, 1-Bit, with Set and Reset, Positive Edge Triggered	28	4
CA1S		Counter, 1-Bit, with Set and Reset, Positive Edge Triggered	23	4
CA2S		Counter, 1-Bit	20	2
FC1S		Counter, 4-Bit, Binary, Asynchronous	70	3
D2GS		Decoder, 2 to 4	24	2
D3GS		Decoder, 3 to 8	51	3
D4GS		Decoder, 4 to 16	97	4
PGN1		Edge Sensitive Pulse Generator	23	1
PGN2		Edge Sensitive Pulse Generator	34	1
PGN3		Edge Sensitive Pulse Generator	45	1
PGN4		Edge Sensitive Pulse Generator	56	1
PGN5		Edge Sensitive Pulse Generator	67	1
PGN6		Edge Sensitive Pulse Generator	78	1
PGR1		Edge Sensitive Pulse Generator	23	1
PGR2		Edge Sensitive Pulse Generator	34	1
PGR3		Edge Sensitive Pulse Generator	45	1
PGR4		Edge Sensitive Pulse Generator	56	1
PGR5		Edge Sensitive Pulse Generator	67	1
PGR6		Edge Sensitive Pulse Generator	78	1
BOSN		Buffer, Oscillator	4	1
BI1N		Buffer, Input, TTL	0	0
BK1N		Buffer, INput, Clock Line, TTL	5	1
BC1N		Buffer, Input, CMOS	0	0
BS1N		Buffer, Input, TTL, Schmitt Trigger	14	1
BCSN		Buffer, Input, CMOS, Schmitt Trigger	12	1
BPUN		Buffer, Input, TTL, with Resistor Pull-Up	0	0
BPDN		Buffer, Input, TTL, with Resistor Pull-Down	0	0
BO1N		Buffer, Output	0	1
BZ1N		Buffer, Output, 3-State	12	2
BPON		Buffer, Output, Source-Only	0	1
BNON		Buffer, Output, Sink-Only	0	1
BR1N		Buffer, Input/Output, 3-State, TTL Input	12	2
BQ1N		Buffer, Input/Output, 3-State, CMOS Input	12	2
BSDT		Buffer, Input, TTL Schmitt In, Pull-Down	14	0
BSUT		Buffer, Input, TTL Schmitt In, Pull-Up	14	0
BUCN		Buffer, Input, CMOS Input, Pull-Up	0	0
BDCN		Buffer, Input, CMOS Input, Pull-Down	0	0
BSUC		Buffer, Input, CMOS Schmitt In, Pull-Up	12	0
BSDC		Buffer, Input, CMOS Schmitt In, Pull-Down	12	0
BSRN		Buffer, Input/Output, 3-State, TTL Schmitt In	26	2
BSQN		Buffer, Input/Output, 3-State, CMOS Schmitt In	24	2
ZLLL		Ground	1	0
ZHHH		VDD	1	0

(1) A basic cell is the pair of corresponding p and n transistors from which the array is constructed. Three basic cells are equivalent to a 2-input NAND gate.

(2) A pin pair is a cell-to-cell interconnect. The total number of pin pairs is limited for each gate array. Exceeding this limit means the automatic routing of the interconnect may be difficult.

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MITSUBISHI PACKAGING AND PRODUCTION

Extensive Packaging Options

Mitsubishi offers a broad range of industry-standard and proprietary packaging options. A leadership foundation in high pin count surface-mount packages includes quad flat packages (QFP), now available with up to 160 leads. Mitsubishi's high pin-count, tape-automated-bonding pin-grid-array (TAB PGA) packaging offers significant advantages in applications requiring large numbers of I/Os.

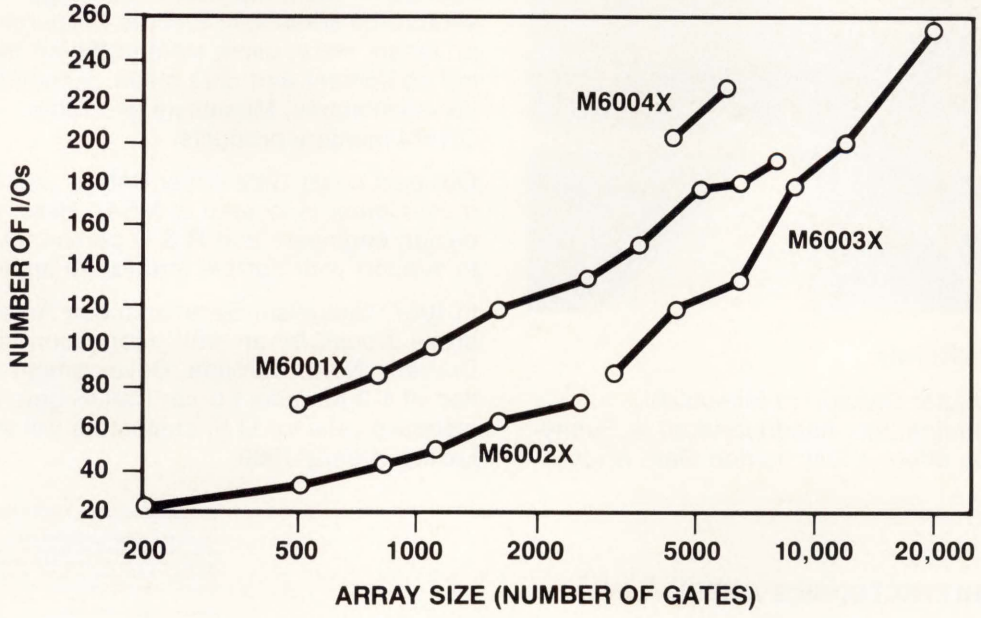
By the end of 1988, Mitsubishi will offer a cost-effective, higher reliability alternative to plastic pin-grid-array packages. This new mounted pin-grid-array package (MPGA) consists of a quad flat package (QFP) mounted on a PC board adaptor and can withstand the flexing that occurs during insertion, soldering and handling of printed circuit boards.

Mitsubishi continues to enhance its leadership position in surface mount technology with extensive R&D efforts for higher I/O devices.

		Number of Pins																					
		16	18	20	24	28	36	40	42	44	52	64	68	80	84	100	124	128	160	177	208	209	256	281
Through-Hole Devices	Plastic Standard DIP	•	•	•	•	•		•	•															
	Plastic Shrink DIP								•		•	•												
	Ceramic Pin-Grid-Array (PGA)																•			•		•		•
	Tape-Automated-Bonding Pin-Grid-Array (TAB PGA)																				•		•	
Surface Mount Devices	Plastic Small Outline Package (SOP)				•		•																	
	Plastic Quad Flat Package (QFP)									•		•		•		•		•	•					
	Plastic Leaded Chip-Carrier (PLCC)									•	•		•		•									

Large Number of I/Os

For designers who have high I/O requirements with low gate counts, the large number of I/Os in Mitsubishi's M60000 family is ideal. Integration options are wide open, from 200 gates and 26 I/Os, up to 20,000 useable gates and 256 I/Os. Our high utilization lets designers use a smaller array with a larger number of I/O ports. This I/O capacity is ideal for applications requiring parallel bus structures and reduction of "glue" logic or miscellaneous gates into a single component.



Mitsubishi CMOS Gate Arrays

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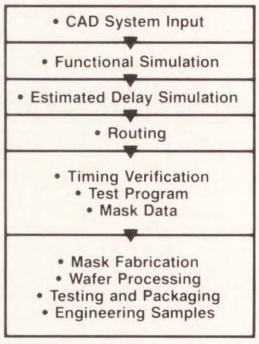
MITSUBISHI ELECTRONICS

Fast Turnaround

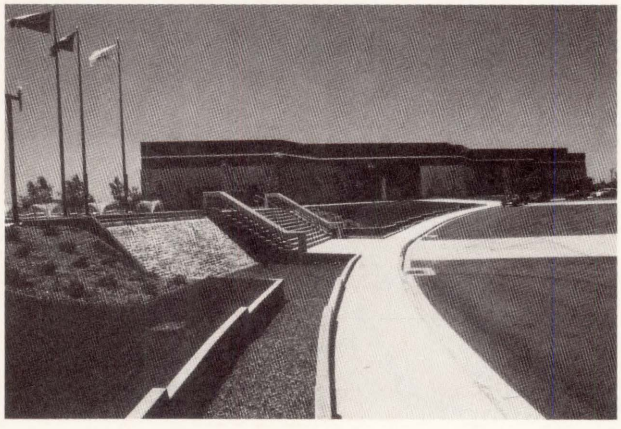
With Mitsubishi's production capabilities and short design cycle from schematic diagram to fully tested prototypes, designers can get products to market fast. Our fully characterized, high volume production process helps assure that the final product will closely match the performance verified at simulation, and that it will meet specifications the first time.

Development Milestones



U.S. Design Center Network

Mitsubishi's gate array service network offers design assistance from coast to coast. Design centers in Sunnyvale, California and Durham, North Carolina are linked by satellite to Mitsubishi's automated gate array production facilities in Kita Itami and Kumamoto, Japan.



Sunnyvale, California

The Semiconductor Division of Mitsubishi Electronics America, Inc. headquartered in Sunnyvale, California, offers a fully staffed Gate Array Design and Development Center. Extensive test and analysis equipment back Mitsubishi's reputation for excellence in quality, reliability and customer service.

Years of engineering and manufacturing experience in electronic equipment markets allow Mitsubishi to provide an unparalleled breadth of semiconductor products. From memories and microprocessors to optical devices, gate arrays and logic, Mitsubishi's leading-edge technologies include 1 Megabit DRAMs, EPROMs and SRAMs, as well as 2 MByte memory cards. The approaching generation of Mitsubishi capabilites includes 4 Megabit DRAMs, 1.3 μm laser diodes, and advanced BiCMOS and ECL ASIC solutions.

Durham, North Carolina

Mitsubishi Semiconductor America, Inc. (MSAI), opened in 1983, represents the largest investment venture by Mitsubishi Electric Corporation outside of Japan. Here, using state-of-the-art manufacturing equipment and ultra-clean, automated production techniques, Mitsubishi assembles advanced DRAM memory products.

Our east coast Gate Array Design and Development Center is located at MSAI. Here, a staff of design engineers and R & D personnel is available to support your current and future applications.

In 1987, Mitsubishi Semiconductor America, Inc. broke ground for an ASIC fabrication facility in Durham, North Carolina. Development and production of 1.3 μm and 1.0 μm CMOS gate arrays and standard cells for U.S. customers will start in this facility in early 1989.

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SEMICUSTOM

Application Specific Integrated Circuits (ASICs)

Macrocell Arrays
- High Speed ECL
- High Density CMOS
- BiMOS
- CMOS
- ALS TTL

Design Software

Design Support Locations

In Brief . . .

Macrocell Arrays

Customize Your Products — Cost-Effectively

Even as the demand for Standard (discrete) Logic forms continues to increase, the era of custom and semi-custom VLSI circuit implementation has arrived. Brought into focus by the economies of computer-aided design and manufacturing (CAD/CAM), Application-Specific Integrated Circuits (ASICs) have become cost effective even in applications with moderate volume requirements. Gate (Macrocell) Array technology has reduced both the time penalty and the cost premium for customized VLSI circuit implementation to virtually zero.

Motorola is in the forefront of this rapidly expanding field. Based on advanced processing competence developed for a broad line of standard products, both bipolar and MOS, it offers an extensive library of logic cells, a proven in-place CAD/CAM capability, and a customer training and assistance program that will turn even a first-time effort into a first-time success.

THE ASIC PHILOSOPHY

"We're supplying a foundation that allows our customers to produce an end product which comes out competitive and *stays that way* through several generations. We get the design cycle working for them, so their products don't fizzle as soon as newer parts come out. It's the difference between a product that performs on paper and one that performs in the marketplace."

Macrocell Arrays

The Right Process for the System Needs . . . The Right Size for Efficient Utilization

Motorola Macrocell Arrays offer the designer the same choice of process technologies that is available for discrete logic designs.

Selected arrays are offered for both commercial and military applications.

- For very high speeds — **State-of-the-art ECL Arrays** offer subnanosecond gate delays.
- For advanced TTL applications — **ALS-TTL Arrays** provide higher speed and lower power consumption at conventional TTL prices.
- For low power consumption with high drive at high frequencies — **BiMOS** blends the best bipolar and CMOS technologies on the same chip.
- For applications demanding very low power consumption, and low cost — **Advanced 2-micron silicon-gate CMOS Arrays;** now available to MIL-STD-883C specifications.
- For system level integration — **High Density 1.0 micron CMOS Arrays** can achieve over 75,000 usable gates on a channelless architecture of minimum dimensions.

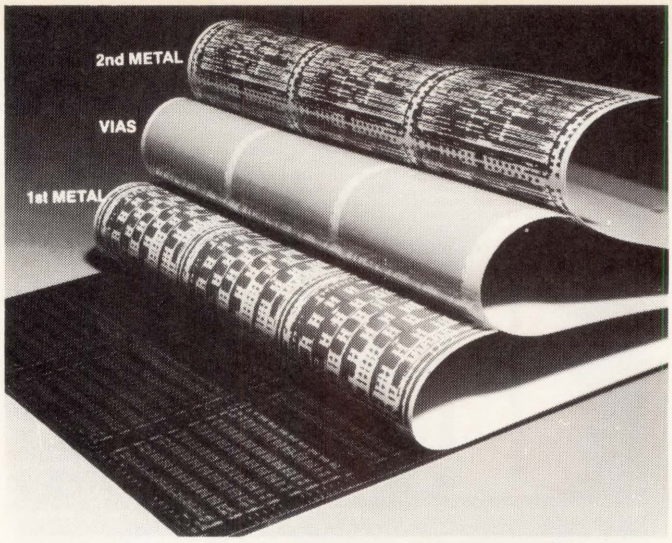
To permit cost-effective implementation, Macrocell arrays are stocked in a variety of prediffused array sizes, that permit optimized utilization of die space for varying VLSI circuit complexities.

About Motorola Macrocell Arrays

Motorola's Macrocell technology is an extension of the gate-array concept. Each cell in the Macrocell array consists of a number of uncommitted components. Stored within a computer library are the specifications for creating interconnecting patterns that transform the unconnected components into SSI/MSI logic functions called macros. These macros yield standard logic elements such as flip-flops, adders, latches and numerous other high performance, space-efficient, predefined functions.

Generating a semicustom circuit design is simply a matter of selecting the required macrocells from the library and describing the interconnect network for implementing the desired results. Motorola's CAD interface provides automatic cell placement and interconnect routing as well as extensive design rule checks. It also performs ac delay simulation, generation of test tapes and customized metalization patterns required to perform the IC processing sequence.

Compared with the conventional approach to custom circuit design, the Macrocell approach offers a tremendous reduction in design and delivery time. Compared with equivalent systems constructed of discrete logic building blocks, the high packing density of array-based components can provide a reduction of system component count approaching several orders of magnitude.



Customized metal patterns overlay predefined component arrays to shorten circuit development time.

High-Speed ECL Arrays

MCA10000ECL Array Sets New Standards

- **Gate Delays As Low As 100 ps (TYP.)**
- **Power Dissipation As Low As 1 mW/gate**
- **10,000 Equivalent-Gate Density**
- **256 I/O Signal Ports**

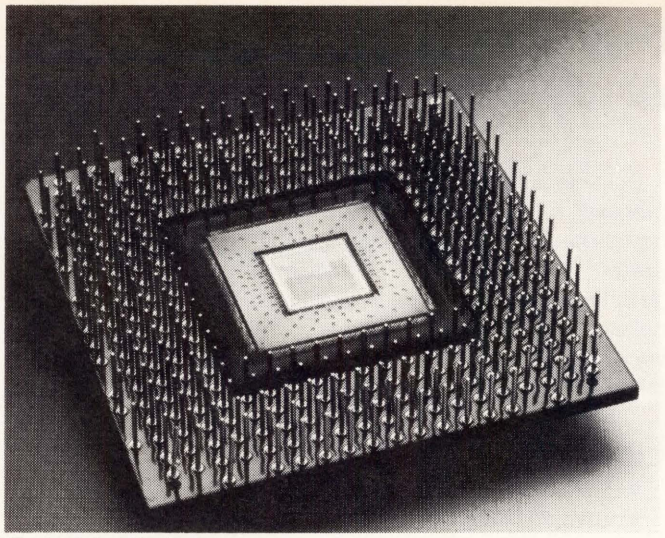
These are the vital statistics of Motorola's third generation ECL Macrocell Array. Compared with second generation products, it represents four times the maximum available gate count and one third the gate delay time.

But the performance improvements don't stop with the statistics alone. With the new array, the designer can program speed-power system performance to match critical system requirements. By means of Motorola's CAD system you can select either a high or low power base array. The designer can then individually program logic switch currents and internal output drive levels. These options yield a performance range from 0.3 ns maximum gate delays with 1.0 mW dissipation to 0.15 ns maximum delay with 3.0 mW per gate.

On-Chip 1K RAM Enhances ECL Array Functions

With approximately 1500 equivalent logic gates this new Motorola (MCA1500M) ECL Macrocell Array can satisfy a wide variety of design options while its four on-chip blocks of 32 x 9 user-configurable RAM simplify system implementation and reduce manufacturing costs.

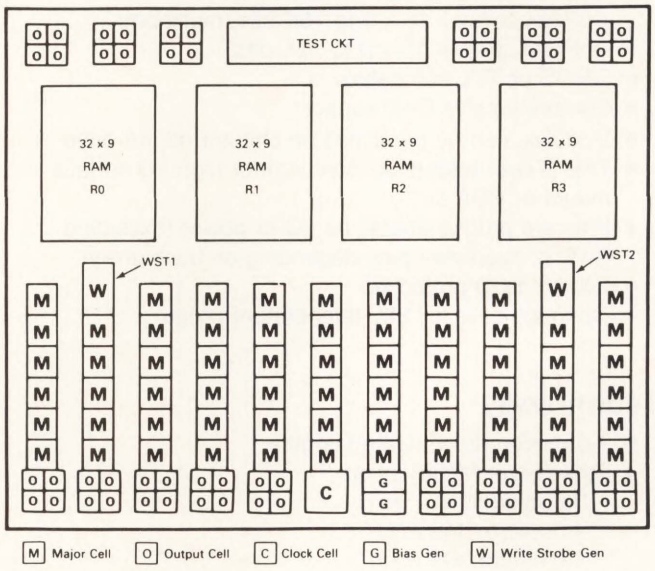
Performancewise, this array is among the fastest and most versatile available. Internal gate delays of 0.3 ns and output gate delays of 0.75 ns offer state-of-the-art throughput, while its density packs the equivalent of up to 50 discrete SSI/MSI logic functions into a single package. With a power dissipation of 8 W (typical) per array, system power dissipation can be reduced by as much as 12 to 1 compared with an equivalent circuit board housing discrete circuits.



Typical Applications:

- **State of the art CPU/FPU designs**
- **>750 MHz Telecommunications**
- **High Speed VLSI testers**

MCA1500M Macrocell Array Layout



The Motorola ECL Array Series

The following table describes the range of capabilities for designs implemented with Motorola ECL arrays.

Features \ Array	MCA 600ECL	MCA 1200ECL	MCA 800ECL	MCA 1500M	MCA 2500ECL	MCA* 1500ECL	MCA 10000ECL
Technology	MOSAIC I		MOSAIC II			MOSAIC III	
Max Gate Equivalent	652	1192	902	1708 + RAM	2760	1500	10332
Internal (Major) Cells	24	48	36	64	110	68	414
I/O Ports	46	60	54	120	120	108	256
Input/Interface Cells	25	32	—	—	—	96	224
Output (O) Cells	18	26	22	60	68	96	200
Max Gate Delay (ns)	1.2	1.2	0.5	0.5	0.5	0.175	0.175
Max Toggle Frequency (MHz)	250	250	770	770	770	1200	1200
Typ Power Dissipation (W)	2.5	4.0	2.5	8.0	8.0	3–6	10–30

*Under Development

MOTOROLA

MOTOROLA APPLICATION SPECIFIC INTEGRATED CIRCUITS

High Density CMOS Array Series

Built on a 1.0 micron, triple layer metal (TRIM) CMOS process the HDC series of arrays represents a significant advancement in microchip technology. By utilizing three layers of metal for routing in addition to power distribution, designers can achieve over 75,000 usable gates on a channelless architecture of minimum dimensions. The result is very high performance (subnanosecond loaded gates) combined with unprecedented I/O flexibility and density.

Features

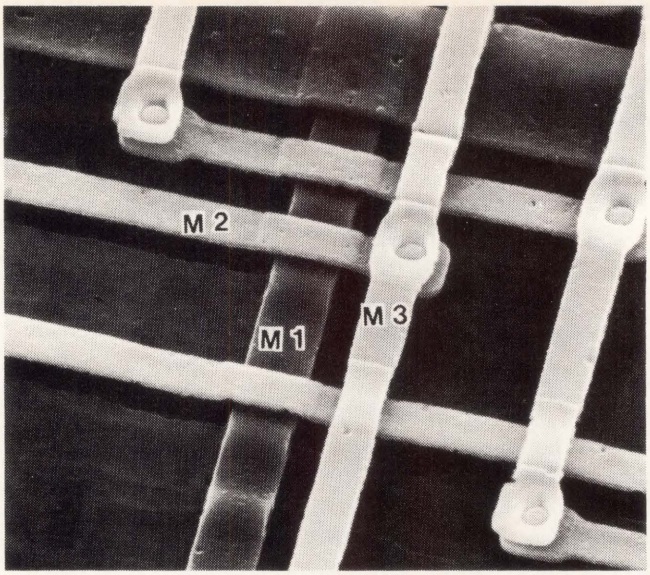
- 5,000 to 100,000 available gates
- Over 75% utilization
- Channelless sea of cells architecture
- 1.0 micron drawn gate length CMOS process
- Triple layer metal routing and power distribution
- 8 transistor fully utilizable primary cell, oxide isolated
- 250 picosecond typical gate delay (F.O. = 1)
- Efficient memory implementation
  — RAM cells — 16 x 9 to 16K bits, multiports
  — ROM cells — 16 x 9 to 32K bits
- CMOS or TTL compatible I/O
- Comprehensive CAD support
- I/O Cells can be paralleled on chip for 48 mA drive
- TAB (Tape Automated Bonding) for high I/O surface mount or PGA's
- Pins are programmable as I/O or power (excluding 8/16/32 fixed pwr. pins depending on base array)
- 2000 V ESD protection
- Operates over full MIL temperature range

Technology

- 1.0 micron drawn Gate Lengths
- Three-layer Metallization
  3.6 micron M1 Pitch
  4.0 micron M2 Pitch
  4.0 micron M3 Pitch

CAD Support

- **Automatic placement and routing of three level metal signals and power at high utilization levels**
- **Support for Daisy and Mentor schematic capture and native simulators**
- **Back annotation of capacitance information on to workstation**
- **Integrated with the MDS (Modular Design System)**



Triple layer metal routing improves utilization to over 75% on sea of cells architecture.

The HDC Series High Density Arrays

Array	# of Gates	Max # of Pads		# of I/O Cells	Die Size mils/side
		TAB	Wire Bond		
HDC006*	5,670	120	96	120	159
HDC008	8,208	140	108	144	179
HDC011*	11,208	160	120	168	199
HDC016	16,416	188	136	204	226
HDC026*	26,112	232	168	256	271
HDC031	31,290	252	244	280	291
HDC047*	47,214	304	212	344	344
HDC064	63,900	348	240	400	391
HDC080*	80,304	388	264	448	430
HDC105	104,832	444	412	512	486

*Under Development

HDC Series Planned Package Offering

Package Type	Array				
	8K	16K	31K	64K	105K
28 PLCC	X				
44 PLCC	X				
68 PLCC	X	X	X		
84 PLCC	X	X	X		
64 QFP	X	X			
80 QFP	X	X	X		
100 QFP		X	X		
120 QFP		X	X		
68 LPGA			X		
84 LPGA			X		
100 LPGA			X		
120 LPGA			X		
144 LPGA				X	
84 PGA				X	
145 PGA (CD)		X			
181 PGA (CD)			X		
299 PGA (CD)					X

CD = Cavity Down

MOTOROLA

MOTOROLA APPLICATION SPECIFIC INTEGRATED CIRCUITS

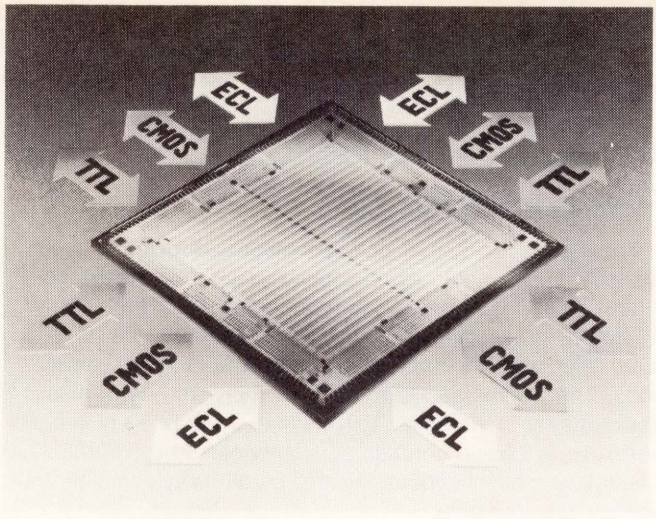
BCA Series BiMOS Arrays

Narrowing the Performance Gap Between Semicustom and Custom Designs

True custom circuit design involves using bipolar technology for those portions of a system requiring very high speed and CMOS technology where more relaxed specifications permit very low power dissipation and very high component densities. Now, BiMOS technology permits blending the two technologies on a single chip, resulting in an array capability that merges the best of both worlds.

Motorola's 1.5-micron BiMOS array family communicates efficiently with ECL, TTL and CMOS without separate interface chips and without a compromise in performance. Its I/O pins can be designated as either CMOS, ECL or TTL input or output and its Internal Cells offer bipolar drive with CMOS-like power consumption.

The accompanying table summarizes the technical story and the graph provides performance comparison with standard CMOS technology. Clearly, the unique capabilities of BiMOS offer a new potential for innovative designs.



"Unique I/O flexibility in a high performance array"

BiMOS Vital Statistics

Transistor Technology —
Polysilicon-Gate CMOS/Walled Emitter NPN Bipolar

Receiver Input Delays —
0.8 ns Typ CMOS
1.2 ns Typ TTL
3.0 ns Typ ECL (1.4 ns option)*

Driver Output Delays —
2.4 ns Typ CMOS (50 pF)
3.5 ns Typ TTL (sinking 12 mA @ 50 pF load)
1.1 ns Typ ECL (50 Ω)

Internal Gate Delay —
0.6 ns Typ (2-input NAND) with F.O. = 1

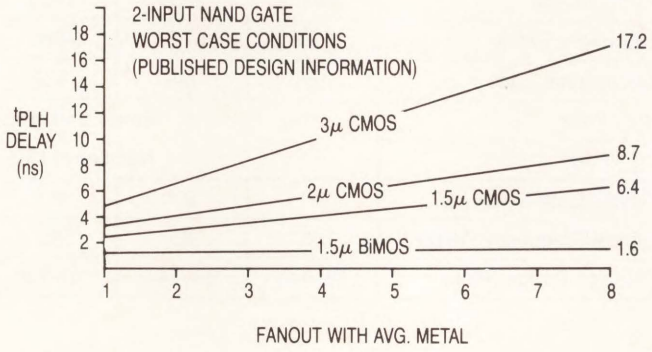
I/O Compatibility —
CMOS, MECL 10K/10KH, ECL 100K, Pseudo ECL, TTL

Power Dissipation Typ per active gate —
0.022 mW/MHz, loaded (F.O. = 3 plus 120 mils metal)

Packages PDIP, PPGA, PGA, PLCC AND PQFP

*Under Development

Performance Comparison BiMOS versus CMOS



BCA Series 1.5-Micron BiMOS Arrays

Features	BCA 700ETL	BCA 1800ETL	BCA 6000ETL
Max Gate Equivalent	704	1792	6144
Internal Cells	352	896	3072
Input/Output Cells	44	92	202
I/O Ports*	44	88	202
Max Gate Delay (ns)	1.1	1.1	1.1
Max Toggle Frequency (MHz)	200	200	200
Output Drive (mA)	12 to 72	12 to 72	12 to 72
I/O Compatibility	TTL-CMOS-ECL-PSEUDO ECL		
Power Dissipation	Low power — varies with array utilization and output loading.		
Die Size (Mils)	180 x 180	250 x 250	396 x 396

*Specific Input/Output configurations vary greatly based on package selection

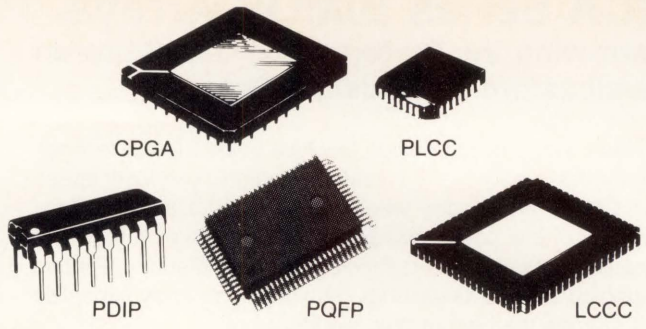
MOTOROLA

MOTOROLA APPLICATION SPECIFIC INTEGRATED CIRCUITS

HCA62A Series — CMOS Arrays Meet Military Requirements

The Motorola HCA62A series of macrocell arrays is implemented in silicon gate technology, with 2-micron drawn gate length, dual-layer metal interconnection and high-speed (HCMOS) processing. Equivalent gate counts from 600 to 8500 offer cost-effective arrays for a wide range of applications. The Series is available in an extensive line of plastic packages for commercial applications. An equivalent line of hermetically sealed ceramic packages plus MIL-STD-883C, Class B compliant processing makes all arrays suitable for military requirements.

Functionally, the Series features full I/O flexibility and completely flexible power and ground inputs. The uncommitted I/O buffers contain N- and P-channel transistors which may be configured into any of 27 different input buffers, 16 different bidirectional buffers or three different output buffers which may be paralleled for up to 24 mA of driving current. Power and ground pads may be placed at any buffer location around the array.



Sampling of available array packages. Range of packages includes everything from 16-pin DIP to 144-pin PGAs in plastic and ceramic.

HCA62A Series 2-Micron CMOS Macrocell Arrays

Features	HCA62A85	HCA62A67	HCA62A50	HCA62A36	HCA62A25	HCA62A17	HCA62A10	HCA62A06
Primary Cells	2856	2236	1658	1200	816	546	319	216
Equivalent Gates	8568	6708	4860	3600	2448	1638	957	648
Bidirectional Pads	168	146	124	102	84	68	54	44
V_{DD} Pads	Power and ground pins are programmable to any package pin.							
V_{SS} Pads	Number of pins varies with array utilization and output loading.							
Typical Gate Delay (ns)	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1
Typical Frequency (MHz)	85	85	85	85	85	85	85	85
Package Range (Pins)	68–144	68–144	40–120	40–100	40–84	28–80	24–52	16–48

The ALS TTL Array Series

Schottky clamped TTL has become the most pervasive form of digital logic in current use. The popularity of these TTL families (LS, ALS and FAST) stems from their ease of use, low cost, medium-to-high speed operation and good output drive capability. For its macrocell array line, Motorola has selected the MOSAIC (oxide-isolated) process.

The ALSTTL array family differs from FAST in that it provides a 50% reduction in power dissipation and improved speed (frequency) characteristics. Yet, it is I/O compatible with its more pervasive (in discrete logic form) LSTTL building blocks. Thus, ALS macrocell arrays offer the performance advantages of this Advanced family for the development of VLSI circuits while maximizing interface capability with the large assortment of discrete LS functions.

Motorola currently offers three array sizes ranging from 500 to 2800 equivalent gates per chip, plus an additional 2800-gate array featuring on-board memory (RAM). The characteristics of the available arrays are described in the following table:

Features	MCA 500ALS	MCA 1300ALS	MCA 2800ALS	MCA 2800RAM
Max Gate Equivalent	533	1280	2860	1800 + RAM
Internal (M) Cells	24	60	130	74
I/O Ports	57	75	120	120
Input Cells	26	40	120	120
Output Cells	27	40	120	120
Max Gate Delay (ns)	4.0	4.0	1.1	1.1
Max Toggle Freq. (MHz)	80	80	150	150
Power Diss. (W)	1.0	1.4	3.5	3.0

Design Software for Application Specific Circuits

A **Modular Design System** consisting of ASIC design software for Engineering workstations is available from Motorola. The first two modules, the **Design Verification Module** and the **Design Capture Module,** are currently available. These CAD software modules support Daisy and Mentor Graphics engineering workstations. Support for Valid Logic Systems is under development.

The Modular Design System provides engineers with a technology independent tool box that will handle today's gate array and cell based designs and tomorrow's technologies as they become available. It allows design capture using Motorola's symbol libraries to simulate the design behavior over, commercial, industrial, automotive and military temperature ranges, resimulate the actual performance of the design after physical layout, and perform rigorous timing checks and testability analysis prior to releasing a design.

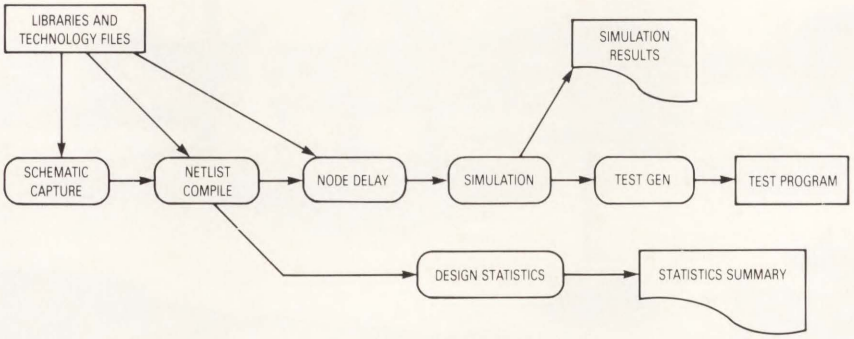
The Design Verification Module includes:

- 62A Series Gate Array
- Netlister with Electrical Rules Checking
- Design Statistics Package
- Selectable Simulation Delays

Modular CAE for Silicon Design

- Post Simulation Timing Analysis Tools with back annotation
- Installation and Verification Utilities

The Design Capture Module includes the above-listed Netlister, Cell Count and Communications only.



LIBRARIES AND TECHNOLOGY FILES

Includes CMOS Array Libraries

- Compatible with Daisy, Mentor, and Valid Workstations Typical/Best/Worst Case Technology Models

NETLIST COMPILE

Netlist Compiler and Diagnostics

- Electrical Rules and Syntax Checks
- Produces TDL, Logcap, and EDIF 2.0 Netlist

NODE DELAY

Node Delay Calculation and Back Annotation

- Sophisticated Node Delay Calculation Equation
  a. Selected Temperature, Voltage, and Process Variation
  b. Estimated or Actual Wirelength Capacitance
  c. RC Tree Analysis
  d. Delay = Intrinsic + Rise/Fall Effects + Output Load
  e. User Specified Output Loading
- Accurate Pin-to-Pin Multipath Delay Modeling (Mentor)

DESIGN STATISTICS

Design Statistics Package

- Gate and I/O Pad Utilization
- Design Rules Check
- Interconnect Analysis

TEST GEN

Test Generation and Timing Analysis

- Extracts and Verifies Tester Input Stimulus
- Checks for Bus Contention (Mentor) and Consistent Timing
- Generates Composite Best/Worst Case Simulation File
- Checks Output Timing Response for Testability
- Extensive Stimulus Diagnostics

A Look Ahead

Motorola is dedicated to servicing the application specific market with CMOS, bipolar and merged technology products. The continuing evolution of processing improvements is clearly destined to yield rapidly expanding capabilities. Please consider the following list of products already in the process of introduction or slated for early implementation.

- Expanded line of 1.0 micron CMOS arrays with triple layer metal.
- High density BiMOS arrays with CMOS power/density at bipolar speeds and on-board RAM.
- 30,000 equivalent gate ECL arrays with less than 100 picoseconds speeds and with imbedded 1.5 ns RAM.
- Open Architecture CAD System based on high performance non-proprietary tools supporting the total design process from design entry to PG tape generation in the user's environment.
- 444 pad arrays in printed-circuit board type PGA packages, or on tape with T.A.B. for multichip applications.

Regional ASIC Design Support Locations

U.S.A.

Alabama, Huntsville . . . . . (205) 830-1050
California, Los Angeles . . . . (714) 634-2844
California, San Jose. . . . . (408) 749-0510
Colorado, Denver . . . . . (303) 337-3434
DC/Maryland, Washington . . (301) 381-1570
Florida, Maitland . . . . . (305) 628-2636
Florida, Ft. Lauderdale . . . . (305) 486-9775
Georgia, Norcross. . . . . (404) 449-0493
Illinois, Chicago . . . . . (312) 576-7800
Massachusetts, Woburn. . . . (617) 932-9700
Michigan, Livonia . . . . . (313) 261-6200
Minnesota, Minneapolis . . . . (612) 941-6800
N.J., Hackensack . . . . . (201) 488-1200
N.Y., Fairport . . . . . (716) 425-4000
North Carolina, Raleigh . . . . (919) 876-6025
Pennsylvania, Philadephia . . (215) 443-9400
Texas, Dallas/Ft. Worth . . . . (214) 550-0770

INTERNATIONAL

Australia, Melbourne . . . . . (03) 887-0711
Canada, Ontario, North York . (416) 497-8181
England, Aylesbury/Bucks. . . . (0296) 395252
Germany, Munich . . . . . (089) 92720
France, Vanves . . . . . (01) 47360199
Hong Kong, Kwai Chung . . . . . (0) 223111
Israel, Tel Aviv 3-7538-222
Italy, Milan. . . . . (02) 82201
Japan, Tokyo . . . . . (03) 440-3311
Korea, Seoul . . . . . (02) 554-5118-21
Singapore 65-294-5438
Sweden, Solna . . . . . (08) 830200
Switzerland, Geneva . . . . . (022) 991-111
Taiwan, Taipei. . . . . (02) 717-7089

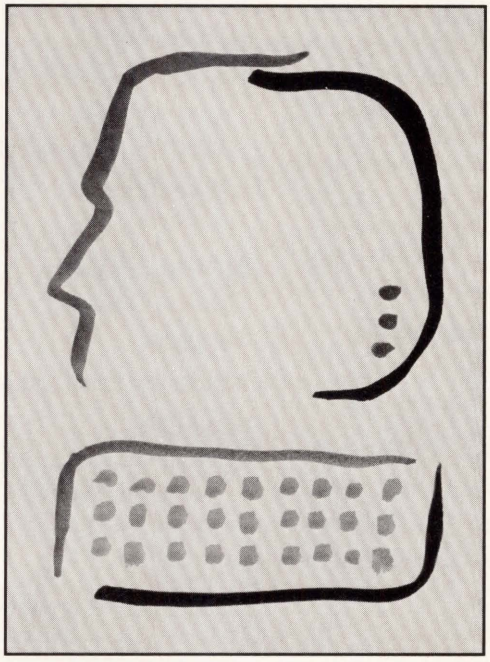
MOTOROLA

MOTOROLA APPLICATION SPECIFIC INTEGRATED CIRCUITS

KE² ASICs

The Knowledge-based
Engineering Environment

NCR



Libraries and Tools

- Standard Cells/Analog/Gate Arrays/Supercells
  Compiled Functions/Core Microprocessors
- Commercial/Automotive/Military
- 1.5 and 2.0-micron DLM CMOS
- KE² Workstation tools including Design Synthesis,
  Design Advisor, ViTat and ViSys Tool Set

Creating value

KE² Overview

Libraries and Design Tools

NCR's Knowledge-based Engineering Environment (KE²) provides design and engineering knowledge in both libraries and design tools. This gives customers the level of integration necessary to find the optimal solution to today's design requirements.

NCR's knowledge combined with the customer's collective applications knowledge make this high-level design integration possible. And the NCR KE² tools make it happen on-time and on budget.

KE² Libraries

- Commercial, Automotive and Military Temperature Ranges
- Standard Cell Libraries in 1.5- and 2.0-micron DLM CMOS
- Analog Cell Libraries in 1.5- and 2.0-micron DLM CMOS
- Gate Arrays in 2.0 micron DLM CMOS
- Compiled functions
- 68C05 and 65CX02 Cores
- 2901/2910
- 82XX Family of Peripheral Macros
- 7400 Family of Functions
- Configurable RAM, ROM, EEPROM, PLA, ALU, Shift Registers, Counter, Dual-port RAM and Multiplexers

KE² Tools on a Workstation

- Design Synthesis™, High-level Language Design Input
- Design Advisor™, Expert Design Advice and Evaluation
- ViTat™, Static Timing Analysis
- ViGen™, Function Compiler
- ViTest™, Test Generation Family
- ViSys™, Design System
- ViTa™, Design Verification

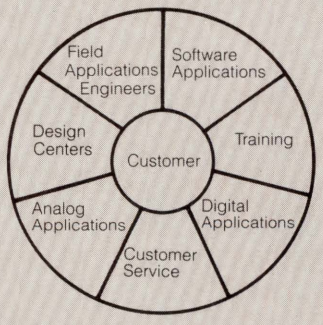
NCR's Customer Design Support Network

- Independent design centers
- Three NCR design centers in the U.S.
- European Design Center
- Far East Design Center
- Field Applications Engineers within easy geographic reach

NCR's strengths and commitment to the customer are in:

- Support of cells for high-level integration and design tools that promote designer productivity and design quality
- Support of analog/digital applications
- Customer-specific analog cells
- Digital design and customer-specific cell enhancements
- Training on libraries, software design tools and applications

NCR's Network of Customer Support



ASICs

NCR's multiple standard cell libraries allow designers to match their exact requirements with the technology that allows for the most effective level of integration and price-performance.

Our 2-micron DLM library is the mainstream choice for most designs. This technology offers excellent cost/performance tradeoffs with an extensive family of analog, EEPROM and compiler functions.

The 1.5-micron DLM library of digital and analog cells is NCR's newest and most advanced. It features double-level-metalization, very high density, and high-speed cells for greater silicon utilization and improved system performance.

Extensive I/O options are provided by NCR's I/O cell family. Mix and match output drive from 2mA to 48mA. Or input switch points and hysterisis. Add pull-ups, pull-downs, open-drain or tri-state outputs. All on one chip.

Power-on reset, oscillators and a wide range of Schmitt Triggers are standard offerings in the NCR cell libraries.

High-Rel ASICs

MIL ASICs

The Military products group is dedicated to supplying standard ICs, cell-based devices, and gate arrays screened to military requirements. This corps of Mil-Spec specialists implements a comprehensive quality system based on MIL-Q-9858A. Devices can also be screened and qualified to MIL-STD-883C, Method 5004/5005 on a stand-alone basis.

Silicon Compilers

NCR has an "ASIC alliance" with Silicon Compiler Systems Inc. (SCS) to provide design verification and foundry services for Genesil/GDT designs. Customers will receive design verification, prototype development, and production silicon all from NCR. This service also includes all of NCR's testing, packaging and applications assistance as normally provided. There is no need to establish separate business interfaces for verification/prototypes and for production silicon.

Automotive ASICs

There is a separate, dedicated Automotive ASIC Group within the Microelectronics Division. This highly focused engineering and marketing resource has no other task than to meet the special needs of automotive manufacturers.

Today, NCR is a certified supplier of automotive parts to the major U.S. automotive corporations, having successfully completed programs involving initial design to high volume production including "Just In Time" delivery and "dock to stock" quality insurance. In addition to the "big three", NCR also serves the small-to-medium automotive companies, working with engineers on a one-to-one basis.

Typical Cell Delays	1.5μm DLM	2μm DLM	3μm SLM
INV, Small Inverter	.4	.6	1.3
NAN2, 2-Input NAND	.5	.7	1.2
AND8, 8-Input AND	1.6	2.3	3.4
NOR2, 2-Input NOR	.6	.9	1.6
OR8, 8-Input OR	1.8	2.6	4.3
DFFRP, D Flip-Flop with Reset, Clock to Q	2.5	3.7	4.3
DFFRPF,* D Flip-Flop with Reset, Clock to Q	1.1	–	–

Delay values are in nanoseconds at 25°C, V_{DD}5.0 volts, and for a fanout of one typical load. *Denotes high-speed cell.

Gate Arrays

NCR offers a complete line of 2-micron, Double-Level-Metal (DLM), CMOS gate arrays to suit a wide range of applications. Through the use of Double-Level-Metal interconnects and advanced auto-routers, utilizations of 85% to 95% are typical.

The NCR building block, or "macro" cell approach, results in substantially improved circuit performance, greater circuit density and shorter design cycles.

All of NCR's gate array products are fully supported by the NCR ViSys™ Design System, the CAD system common to both gate array and cell-based products. This allows NCR gate arrays to be economically migrated to standard cells.

Packaging

NCR offers a broad range of packages for ASIC applications including plastic packages to support cost-sensitive applications as well as ceramic packages to support military, automotive and other high reliability applications.

NCR offers an extensive line of leaded and leadless surface mount options to complement a variety of through-hole mounted packages. Choices include DIPs, SOICs, PLCCs, PPGAs and Plastic Flat Packs (PFPs). NCR also supports EIAJ and JEDEC standard pinouts.

NCR 2μm DLM Gate Arrays								
Available Gates	648	957	1638	2448	3600	4968	6750	8568
Major/Primary Cells	216	319	546	816	1200	1656	2250	2856
Available I/O	44	52	68	84	100	124	146	168
Max. Gate Delay	1.6 ns (Typical)							
Max. Clock Speed	50 MHz							
Flip-Flop Toggle Freq.	85 MHz (Typical)							

Standard Cells

The following is just a sample of NCR's extensive cell library listing. Contact your NCR sales representive for a complete listing.

SSI Functions

- Buffers and inverters—output drive/tri-state options
- NAND and NOR—available with 2, 3, and 4 inputs
- AND and OR — up to 8 inputs
- EXOR, AOI and OAI "combinational" logic cells—for denser and faster devices
- Delay cells
- Clock drivers

Flip-Flop/Latches

- Cross-coupled latches—both NOR and NAND
- Level-sensitive transparent— both with or without reset and clock drivers
- Edge triggered D and JK Flip-Flops—with or without Reset, Set and Reset clock driver
- High-speed cells to meet critical path requirements.

MSI Functions

- Single-bit cascadable shift register with serial or parallel in and serial out—with or without clock driver
- Single-bit cascadable, loadable, up-down counter with Reset and Enable, carry in and carry out
- Full and Half Adders
- 74XX Library

Input/Output Pads and Buffers

- Options to give optimal size pad-limited designs
- Levels are directly TTL, LSTTL and CMOS compatible
- Input cells—choice of standard TTL or variety of Schmitt trigger levels
- Output cells—variety of drive options, open drain, pull-up/pull-down options, up to 48mA drive
- Tri-state—combination of I/O options
- Oscillators

Function Compilers

Today, NCR offers the power of some of the industry's most advanced silicon compilation technology within the framework of our existing CAD system. This capability is in the form of function compilers which allow designers to "customize" a compiled function to their specifications. NCR functions are compiled on engineering workstations eliminating costly and time consuming remote mainframe compilation. This feature gives the designer direct access to silicon compiler technology within the friendly ViSys Design System on a workstation.

Compiled Functions

- ROM
- Low-power RAM
- Fast SRAM
- EEPROM
- ALU
- Dual-port RAM
- Shift Registers
- Multiplexers
- Counters
- FIFO
- Multiplier/Accumulator

NCR CMOS Supercells

In terms of system integration, NCR's supercells open new horizons. Supercells are function blocks which were once only available as standard ICs. But NCR has taken these complex functions such as microprocessor cores, peripheral ICs, 82XX, SCSI, and CRT45 and added them to our Supercell libraries. With this advanced capability, the system-on-a-chip concept can be a reality today.

Supercells

- 65CX02 MPU Core
- 68C05 MPU Core
- D to A Converters
- A to D Converters
- SCSI Controller
- Sound Generators
- Counter/Timer
- 2901 Microprocessor
- 2910 Controller
- 15530 Encoder/Decoder
- CRT45 Controller
- 82C37A
- 82C50
- 82C53
- 82C54
- 82C55
- 82C59
- 82C84
- 82C88
- 8X8 Multiplier
- 16X16 Multiplier

NCR Analog Libraries Extend Functionality.

Analog Features

- Choice of 1.5 or 2-micron
- Low-power
- Power-down mode
- Low supply voltage operation
- Internal or peripheral placement
- 10K ECL-compatible input interface
- Analog I/O pad cells
- Kit parts

NCR's analog cell library has been an industry leader for more than five years. Functions as simple as operational amplifiers and as complex as analog-to-digital converters are available in commercial, industrial, automotive and military temperature ranges to take your NCR cell-based device well beyond the realm of normal ASIC technology.

Many complex system functions which used to require multiple analog and digital ICs can often be accomodated on a single chip. If you need a complex analog function to meet system requirements, NCR can design and build the function to your specifications using digital cells or analog cells in 1.5 or 2μm.

Analog Cells

- Op Amps
- Comparators
- Analog Switches
- Bandgap Voltage References
- Bias Generators
- Logic Level Shifter
- Power-On-Reset
- Oscillators
- VCOs
- DACs
- ADCs

NCR 1.5-micron Analog Cells currently available:

- Analog Switch
- Bandgap Voltage Reference
- General Purpose Comparator
- ECL Input Interface
- Analog Input Pad
- Analog Output Pad
- General Purpose Operational Amplifier
- Matched Resistors Using Standard Building Blocks
- Custom Resistors

VS1500 Analog Kit Parts are available for all cells listed above.

NCR 2-micron Analog Cells currently available:

- Analog Switch
- Bandgap Voltage Reference
- Custom Capacitors
- General Purpose Comparator
- ECL Input Interface
- Analog Input Pad
- Analog Output Pad
- General Purpose Operational Amplifier
- Matched Resistors Using Standard Building Blocks
- Custom Resistors

VS2000 Analog Kit Parts are available for all cells listed above.

Additional 2-micron cells under development and scheduled for release 4Q 1988.

- 8 bit, 5 MHz ADC
- 10 bit Dual Slope ADC
- 8 bit, 2 MHz DAC
- Low Current Op Amp
- High Speed Comparator
- 5 to 30 MHz Voltage Controlled Oscillator

NCR can also develop custom analog cells to meet your unique specifications. Please contact NCR for further information.

VS1500 General Purpose Operational Amplifier

Features

- 1.5-micron CMOS
- Low input offset voltage
- Low leakage CMOS inputs
- Internally compensated
- Full power-down via logic level inputs
- Low power
- Internally biased
- High output voltage swing
- Bias current and compensation options available
- Operates at supply voltages as low as 3.0 V
- Uses the standard digital process (no additional masks required)

The OA5001 is a general purpose operational amplifier cell with an input common-mode voltage range which includes V_{SS}. It is internally compensated for unity gain stability and can drive loads up to 20kΩ, 20 pF. For higher values of load capacitance, the phase margin will be less than the specified value and could result in instability. Load resistance of less than 20kΩ will result in reduced output voltage swing and open loop gain. All required bias currents are generated internal to the cell for ease of use and elimination of cross-talk between op amps which can occur with a common current reference. The OA5001 cell incorporates full power-down (PD) via logic level inputs. For normal operation, PD should be V_{SS} potential and PDB at V_{SS} potential.

Test Circuits

The OA5001 operational amplifier cell has been fully characterized over the commercial, automotive and military temperature ranges. The dc tests were done using an Analog Devices LTS-2015 analog tester configured with an op amp family board. The tester uses a standard op amp test loop to measure open-loop dc parameters. A simplified schematic of the test loop is shown in Figure 1.

The input offset voltage of the op amp appears at the output of the loop, multiplied by about 500. The DUT output voltage is set using V_{th}. The DUT common-mode voltage is set by using split supplies with the inputs always referenced to ground and programming V+ and V- to the appropriate values. DUT open-loop parameters are measured by changing the DUT voltage level of interest (e.g. output voltage, common-mode voltage or power supply voltage) and measuring the resulting change in offset voltage.

The output high and low voltage tests specified with V_{ID} = 0.1V are done by breaking the feedback loop and applying a 0.1V source between the op amp plus and minus inputs and directly measuring the resulting DUT output voltages.

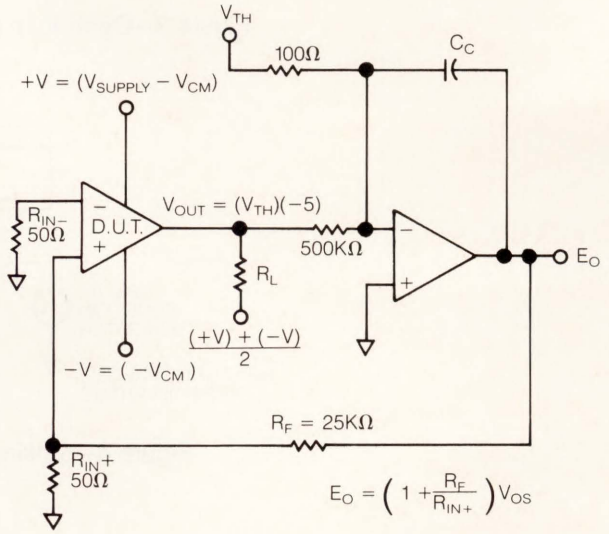


Figure 1–Simplified op amp test loop

Theory of Operation

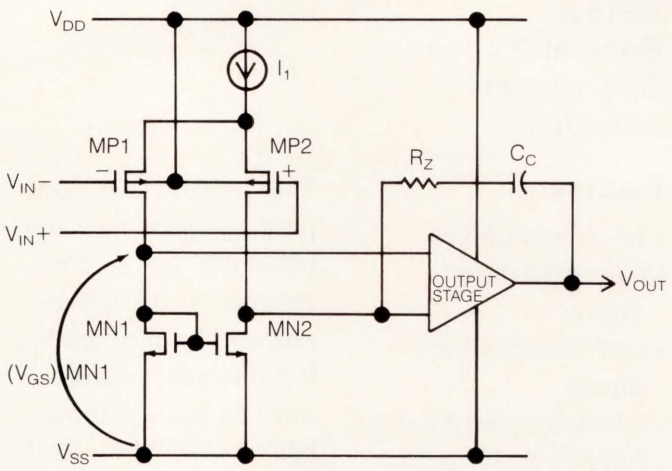
An equivalent circuit of the OA5001 operational amplifier is shown in Figure 2.

V_{IN+} and V_{IN-} are compared by the p-channel differential pair MP_1, MP_2 producing a differential output current which is converted to a single-ended output voltage by current mirror pair MN_1, MN_2. Bias current for the first stage is supplied by current source I_1. The output of the first stage is coupled to the differential pair input quasi-push-pull output stage. This output stage provides double the output source current and higher transconductance than a conventional class A output stage with the same idle current. Dominant pole frequency compensation for unity gain stability is accomplished by the addition of compensating capacitor C_C and feed-forward zero nulling resistor R_Z.

OA5001 ac parameters are measured using the test circuits in Figures 3 and 4.

The Figure 3 test circuit is used for measuring gain-bandwidth product and phase margin.
The Figure 4 test circuit is used to measure settling time, slew rate and unity gain follower frequency response.

Optional load capacitance consists of the sum of probe, package and test fixture capacitance.



$(V_{IN})_{MIN} = (V_{TN} - V_{TP}) + (\Delta V_{GS})_{MN1}$

WHERE:

V_{TN} = THRESHOLD VOLTAGE OF MN1 – MN2

V_{TP} = THRESHOLD VOLTAGE OF MP1 – MP2

$(\Delta V_{GS})_{MN1} = (V_{GS})_{MN1} - V_{TP}$

AND

V_{TP} AND V_{TN} ARE TAKEN TO BE POSITIVE VALUES.

Figure 2–0A5001 equivalent circuit

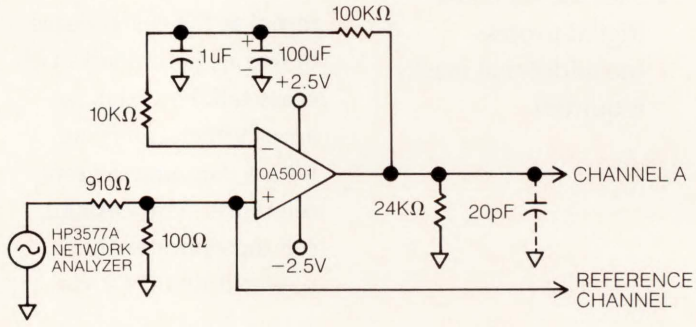


Figure 3–Open-loop gain/phase response test circuit

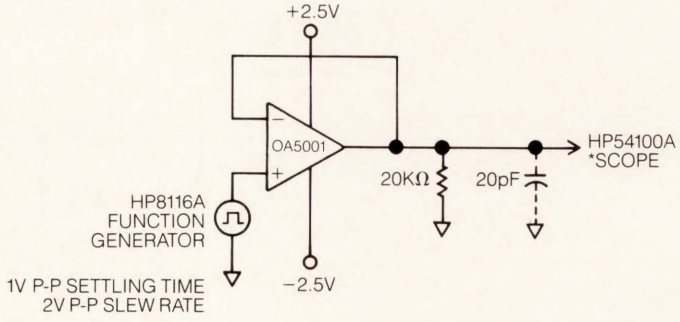


Figure 4–Settling time/slew rate test circuit

OA 5001 DC Specifications (V_{DD}–V_{SS}) = 5.0 V± 10%

Parameters	Min	Typical @ 25° C	Max	Unit	Operating Temp. Range °C	Comments/ Conditions
Input Common-Mode Voltage Range	V_{SS} V_{SS} V_{SS} V_{SS}	V_{SS}–0.2 to V_{DD}–1.5	V_{DD}–1.5 V_{DD}–1.5 V_{DD}–1.5 V_{DD}–1.5	V	25 0 to 70 –40 to 85 –40 to 125 –55 to 125	Test Circuit Figure 1
Open Loop Voltage Gain (Avol) 0 < V_{CM} < V_{DD}–1.5	64 63 60 60	70		dB	25 0 to 70 –40 to 85 –40 to 125 –55 to 125	R_L = 20K Ω Test Circuit Figure 1
Open Loop Voltage Gain (Avol) 1.0 < V_{CM} < V_{DD}–1.5	67 66 63 63	74		dB	25 0 to 70 –40 to 85 –40 to 125 –55 to 125	R_L = 20K Ω Test Circuit Figure 1
Open Loop Voltage Gain (Avol)		68 82		dB	25 25	R_L = 10K Ω R_L = 50K Ω
Initial Input Offset Voltage (V_{OS})	–5 –5 –5 –5	±1.5	+5 +5 +5 +5	mV	25 0 to 70 –40 to 85 –40 to 125 –55 to 125	Test Circuit Figure 1
Input Offset Voltage Temperature Coefficient		±5		µV/°C		Test Circuit Figure 1
Output Low Voltage V_{OUT} - V_{SS}		30	70 75 100 100	mV	25 0 to 70 –40 to 85 –40 to 125 –55 to 125	R_L = 20K Ω V_{ID} = –0.1 V V_{CM} = $V_{DD/2}$ Test Circuit Figure 1
Output High Voltage V_{DD} - V_{OUT}		150	275 300 550 550	mV	25 0 to 70 –40 to 85 –40 to 125 –55 to 125	R_L = 20K Ω V_{ID} = –0.1 V V_{CM} = $V_{DD/2}$ Test Circuit Figure 1
Supply Current		270	475 600 600 675	µA	25 0 to 70 –40 to 85 –40 to 125 –55 to 125	Test Circuit Figure 1
Supply Current Power Down Mode		.001	1.0 1.0 1.0 1.0	µA	25 0 to 70 –40 to 85 –40 to 125 –55 to 125	Test Circuit Figure 1
DC Common-Mode Rejection Ratio	60 60 60 60	85		dB	25 0 to 70 –40 to 85 –40 to 125 –55 to 125	Test Circuit Figure 1
DC Power-Supply Rejection Ratio	64 64 64 64	85		dB	25 0 to 70 –40 to 85 –40 to 125 –55 to 125	Test Circuit Figure 1

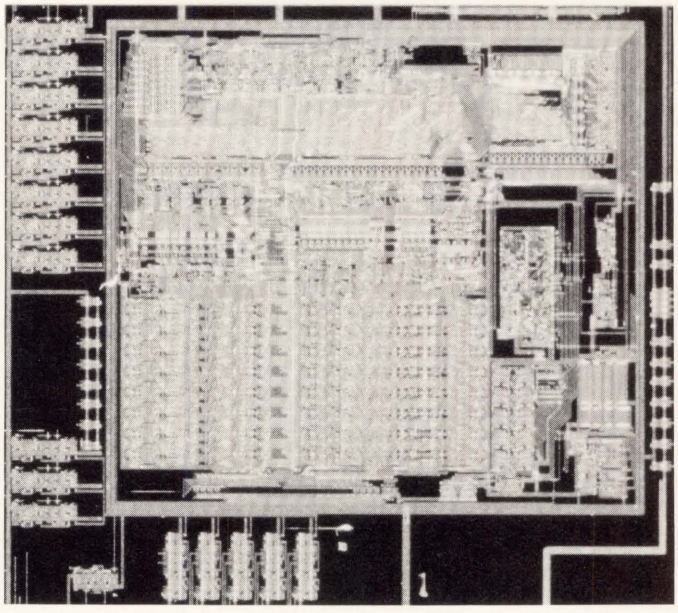
AC Specifications (V_{DD}–V_{SS}) = 5.0 V, V_{CM} = (V_{DD}–V_{SS})/2

Parameters	Unit	Typical @ 25° C	Comments/ Conditions
Gain-Bandwidth Product	MHz	2.9	R_L = 20K Ω C_L = 20 pF Test Circuit Figure 3
Phase Margin Unity Gain Feedback	deg.	35	R_L = 20K Ω C_L = 20 pF Test Circuit Figure 3
Positive Going Output Slew Rate	V/µS	5.7	R_L = 20K Ω C_L = 20 pF Test Circuit Figure 4
Negative Going Output Slew Rate	V/µS	7.8	R_L = 20K Ω C_L = 20 pF Test Circuit Figure 4
1% Settling Time (1V Step)	µS	0.6	Unity Gain R_L = 20K Ω C_L = 20 pF Test Circuit Figure 4

NCR 68C05 Core Microprocessor

Features

- 2-micron CMOS DLM technology
- 6805 8-bit MPU core functionality
- Executes identical instruction set as standard 68C05
- 8 MHz external clock; 4 MHz internal bus speed
- Enhanced 16-bit address bus
- 8-bit by 8-bit unsigned multiply instruction
- 4 uncommitted interrupt lines
- Memory mapped
- Power-saver standby feature
- Behavioral Language model aids in design and test.
- Emulator Board available



Description

The NCR68C05 core supercell is functionally identical to the industry standard MPU68C05 part. It is configured to provide a core supercell and microprocessor for NCR cell-based 2-micron devices. The core contains enhancements to improve performance and testability in the cell-based VLSI circuit environment.

Designing with the 68C05 Core

The NCR ViSys Design System libraries and tools provide a powerful Mentor Graphics workstation-based design environment to aid you in designing your device around the NCR68C05 core.

The NCR VS2000 Standard Cell Libraries (both digital and analog) and ViGen compilers for configurable memory, peripheral and interface functions provide the 2-micron cell functions to meet the requirements of a cell-based device in any commercial, automotive or military application.

In general, the 68C05 core is appropriate for any application that currently utilizes the standard 6805 CPU or for any system application that requires a CPU.

Test Considerations

A behaviorial language model (BLM) of the NCR68C05 core is available initially on the Mentor Graphics IDEA™ Series workstations. The BLM permits full simulation of the design as well as an efficient means of capturing simulation vectors for conversion to test vectors.

Test coverage of the NCR68C05 core-based design is greatly enhanced through direct testing of the functional blocks in the design, including the core. The core's internal 8-bit bus provides easy testing access and can be isolated from the external bus when testing the core.

NCR will supply a set of 68C05 test vectors as a drop-in core test for production devices which utilize direct testing. It is also possible to build self diagnostics for the core into an on-chip ROM, permitting immediate determination of full chip functionality. NCR's ViTest family of test generation tools will aid the development of a complete test program for your device.

KE²: The Knowledge-based Engineering Environment

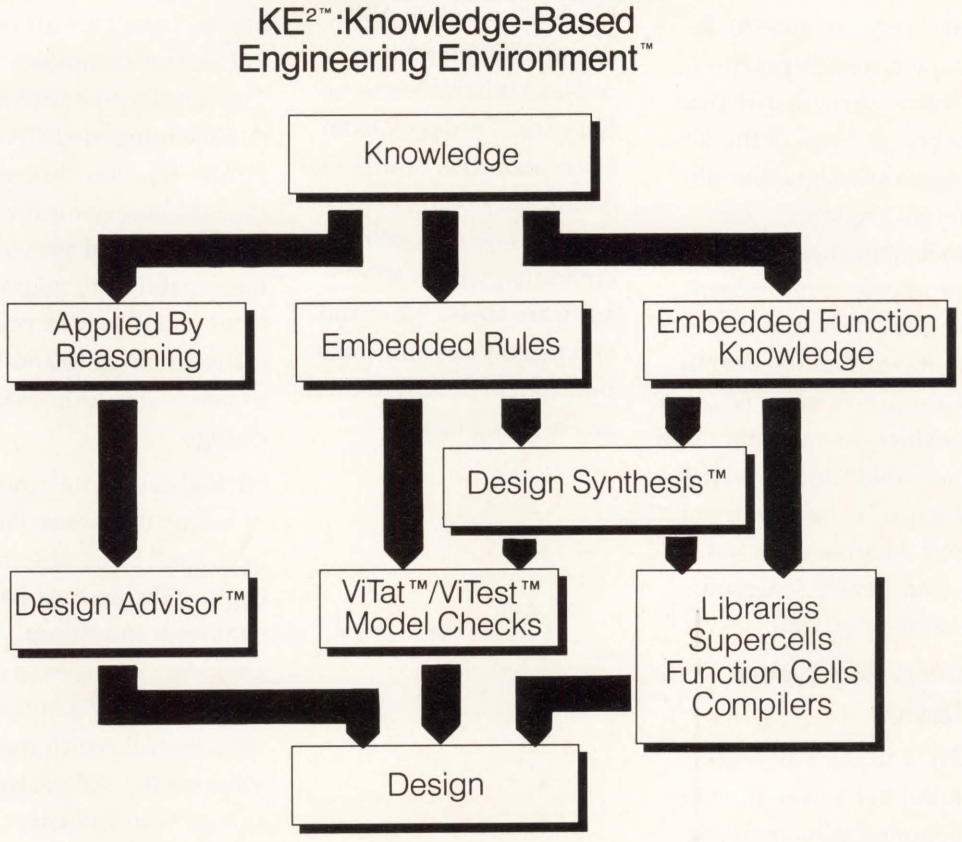
NCR is making sophisticated ASIC design available to all customers through the Knowledge-based Engineering Environment. The knowledge base is provided by years of good design experience captured in software and available to designers who use NCR's expert tools.

Productivity Improvements

KE² shortens the design cycle for designers at all experience levels. Even the most adept designer's productivity is enhanced when designs are performed at a higher level using NCR Design Synthesis and the advanced NCR function libraries and compilers.

NCR's expert ASIC design tool, Design Advisor, applies extensive expertise to evaluate the design and provide advice, even tutoring designers less familiar with ASICs.

ViTat speeds timing analysis. ViTest and probabilistic fault grading accelerate and promote tester compatibility and efficient test program production.



The KE² tools also can be used to improve design performance and logic area(cost). What-if explorations, including architectural tradeoffs with a high level language, further increasing the designer's ability to create more optimal designs.

Design Quality Engineering

Design Quality is improved by a number of KE² tools.

Improved design margins and identification of problem-prone implementations are provided by ViTat and Design Advisor. Design Advisor also reviews for conformance to good design practices.

Testability is enhanced by Design Advisor and efficient fault grading analysis.

Design Synthesis gives correct-by-construction results, including testability.

NCR's ASIC function libraries have already been through this scrutiny, assuring that you are designing with sound building blocks.

In the end, better design margins and more "bulletproof" designs result in better system manufacturing yields and reliability.

Design Management

Increasingly complex designs demand meticulous, consistent review and conformance to accepted design practices. This is particularily true when sections of the design are assigned to different engineers. KE² meets this need. It also promotes well-defined specification and documentation of the design. Design Synthesis not only enables documentation of intended functions with a high-level language but self documents its synthesized library schematic implementation.

Integrated System Design

The tools of KE² work hand in hand with many commercially available design products to support system-level design. These third-party tools include multi-chip simulation, simulation models for "standard" ICs, hardware modeling, fault grading and advice on chip interfaces. All logic simulators certified for use within KE² also have ties to PC board place and route tools.

Expanding the Knowledge Base

With NCR's migration capability between ASIC libraries and the ability to capture function descriptions in a high-level language for implementation in any library, the user's knowledge relating to a particular function block or complete ASIC design is retained for reuse in other designs or libraries. Feedback from users and other sources is continually being added to the knowledge already embodied within KE² software tools. New and enhanced tools and capabilities will be added on an on-going basis.

ViSys Design System Tools

NCR's ViSys Design System supports all NCR libraries from gate arrays to function compilers. This single, powerful and flexible integrated CAD system lets you choose the best library for the application and provides the capability to migrate from one library or process technology to another as needs and technology change.

NCR also offers a range of Software License Packages from basic design capture through AI-based synthesis and design analysis. You choose and expand the level of design control which meets your needs. All packages run on your industry-standard engineering workstation.

Design Synthesis

Knowledge-based Design Synthesis automatically generates correct and efficient designs in the target ASIC library from high-level language descriptions. Simulation can also be performed at the function language level before synthesis to quickly examine architectural tradeoffs. The system generates both sequential and combinational functions within complex asynchronous and synchronous logic blocks.

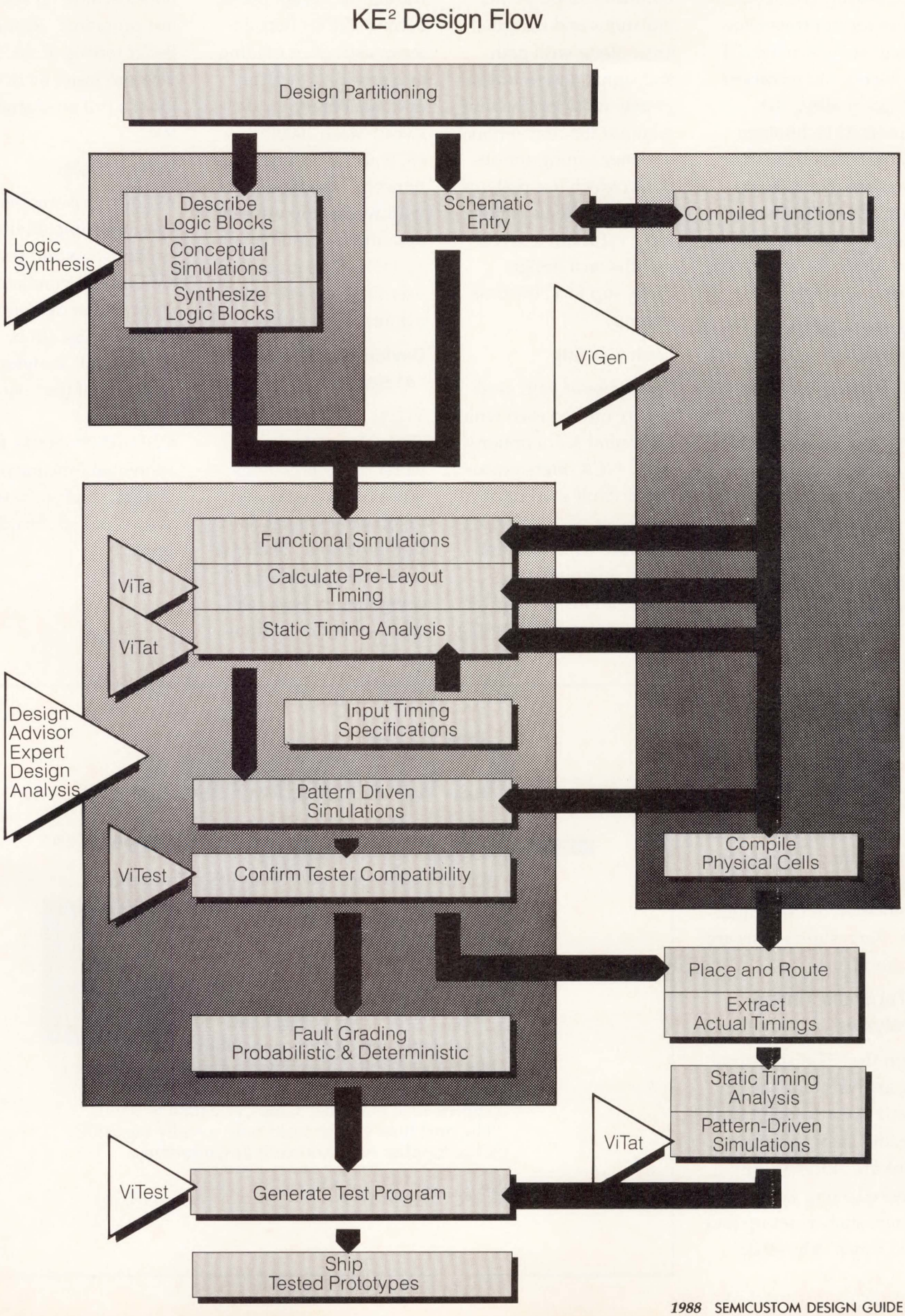
ViGen Function Compilation

Today, NCR offers the power of some of the industry's most advanced silicon compilation technology within the framework of our existing ViSys system. This capability is in the form of cell compilers which allow designers to "customize" a compiled cell to their specifications by selecting from a menu of options.

The ViGen compiler automatically generates symbols for design capture and models for simulation and timing analysis of the compiled functions. Functions such as ALU, RAM, ROM, Counter and Multiplexer, Dual-port RAM and Shift Registers can be parameterized for physical layout "on-the fly" while in the schematic entry mode. A complete simulation capability is available on the workstation. No resimulation is required.

Design Advisor

With Design Advisor, expertise in many areas relating to ASIC technology is available to automatically review the de-


KE² Design Flow
Design Partitioning
Describe Logic Blocks
Conceptual Simulations
Synthesize Logic Blocks
Logic Synthesis
Schematic Entry
Compiled Functions
ViGen
Functional Simulations
Calculate Pre-Layout Timing
Static Timing Analysis
ViTa
ViTat
Input Timing Specifications
Design Advisor Expert Design Analysis
Pattern Driven Simulations
Compile Physical Cells
ViTest
Confirm Tester Compatibility
Place and Route
Extract Actual Timings
Fault Grading Probabilistic & Deterministic
Static Timing Analysis
Pattern-Driven Simulations
ViTat
ViTest
Generate Test Program
Ship Tested Prototypes

sign at any time. Its advice concerning opportunities for improvement brings to light potential problems and enhances design quality. Advanced AI technology enables Design Advisor to reason about the design, allows the user to dialogue with the system and tutors the less experienced designer.

Accurate Timing Analysis.

ViTa timing analysis and verification tool, available since 1983, is now in its fourth generation of excellence.

ViTa supports multipath delays using actual values from the layout. First it estimates best/worst case timings and pre-layout delays and then calculates post-layout timings using distributed resistance/capacitance tree analysis.

ViTa also takes into account the effects of signal degradation. ViSys software tools support back annotation to the simulator. No resimulations are required.

ViTat Static Timing Analysis

With the ViTat static timing analysis tool, the user's point-to-point timing and skew specifications are automatically checked along with parameters such as set-up and hold times. The static operation executes in minutes and pinpoints violations and marginal areas along with path and signal descriptions, greatly reducing the time required for conventional dynamic timing simulations (which use patterns to drive the logic simulator). ViTat often saves months on a design cycle—up to a 50% time savings.

Fault Grading

Two types of fault grading are offered each with a different set of options. First, NCR offers probabilistic fault grading as a service or with optional software which runs on popular engineering workstations. This gives the user fast-turn grading and diagnostic guidance during the design phase. Second, NCR offers deterministic fault grading as a service or with an optional library for the Zycad Mach 1000™. NCR also is adding to its libraries' compatibility with workstation-driven deterministic fault analysis tools. This gives the user final accurate grading and diagnostics.

Device Test Programs "At Speed"

ViTest Test Generation Tools merge the best/worst case simulations into a common file and report on potential design problems. Then patterns are screened for compatibility with real-world tester limitations so that "at speed" simulations become "at speed" test programs. Result? Better testing of the device and faster availability of a full production test.

ViTest Tools:

- ViPac™ assures test pattern compatibility with real world testers.
- ViComp™ combines best/worst case simulations for test strobe placement analysis and creation of the final test program.
- ViStrobe™ checks for potential functional errors, valid stobe windows and strobe margins.

Quality Overview

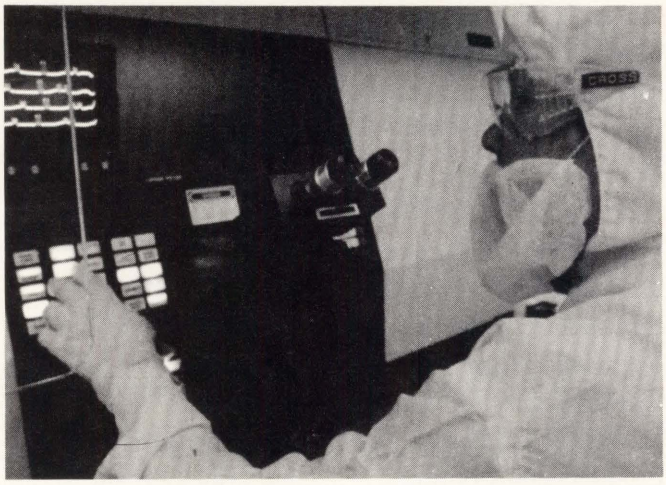
Each of NCR Microelectronics' standard products, cell libraries and processes has been extensively characterized and qualified. Our quality assurance engineers work closely with standard product, standard cell and gate array IC designers, as well as computer-aided design software engineers and process engineers to assure that long-term product quality is an integral part of every NCR standard or ASIC device.

At NCR we have learned that not only must each and every element of the design and manufacturing process be fully validated, but that they must also be validated as an entire system—from workstation simulations to processing. For example, in the design process, strict design rules with carefully controlled margining requirements are used to insure that products meet or exceed customer quality and reliability requirements. In the fabrication and assembly operation, Statistical Process Control (SPC) is the key to maintaining a high level of confidence.

Of course each ASIC device receives full screening, testing and qualification prior to shipment, but without built-in quality attributes, long term reliability could not be ensured. And at NCR quality is measured not only by the number of devices shipped to our customers, but also the reliability of the devices over the long haul.

Additionally, NCR supports a program of continuous quality improvement. This includes working closely with customers to help insure that applications are consistent with the intended use of the product. If problems are encountered, NCR maintains a closed loop corrective action system to insure that problems are resolved and corrected in a timely manner.

All of this attention to quality and reliability has paid off—for NCR and our customers. NCR has a zero-defects policy which means that every part provided to a customer is guaranteed to be defect free. This significantly reduces the customer's cost of ownership on receipt of parts, during product assembly and in the field.



Facilities

Today, NCR's Microelectronics Division operates two modern manufacturing facilities located in Fort Collins and Colorado Springs, Colorado.

The Fort Collins facility is headquarters for NCR's commercial/industrial Application Specific IC (ASIC), Customer Owned Tooling (COT), Software Products and Communications Products Business Units.

The Fort Collins location also houses volume wafer fabrication and test facilities and a complete small-volume/fast-turn assembly capability to package prototypes.

Colorado Springs is home for NCR's Military ASICs, Automotive ASICs and Logic Products Business Units.

The Colorado Springs facility is also the site of NCR's newest advanced wafer fab. Currently, this fab is running production 1.5µm and 2µm CMOS with 1.0µm and sub-micron CMOS in prototype development.

Design Centers

To serve the ASIC markets, NCR supports a network of Value Added Design Centers™ (VADC) and operates three internal Design Centers.

VADC's provide local customer service and were chosen for their special expertise and experience in ASIC design.

NCR Design Centers provide "factory-level" support to the VADCs.

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Communications Products
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Military ASIC Product Group
Automotive ASIC Product Group
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Los Angeles, CA 90067
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North Central Sales
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South Barrington, Il 60010
(312) 426-4600

South Central Sales
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5 859 6888

NEC

NEC Electronics Inc.

BiCMOS-4A ADVANCED PROCESS BiCMOS GATE ARRAYS

September 1988

Description

The BiCMOS-4A gate arrays feature the high speed of bipolar arrays and the low power dissipation of CMOS devices. NEC has achieved this combination on the same chip, plus latchup-free operation, by utilizing a 1.5-micron silicon gate CMOS technology and an advanced bipolar process.

The gate array chip (figure 1) is divided into internal and external cell areas. The I/O (interface) cells are in the external cell area. Each internal cell consists of one resistor and 14 transistors: eight n-channel, four p-channel, and two bipolar npn. The internal cell is equivalent to two gates; the external cell is equivalent to one gate.

These application-specific integrated circuits (ASICs) have part numbers in the μPD67000 series. They are available in two sizes (6372 and 10,348 gates) and a variety of packages, including low-cost plastic.

Gate arrays are intended for customers seeking cost-effective alternatives for VLSI designs. With gate arrays, designers can decrease system form factors by reducing component count and board size while increasing the reliability of their final design.

NEC's gate array program allows a semicustom IC to be developed quickly and reliably at a small fraction of the cost of a full-custom device.

NEC supports its ASIC products with a comprehensive CAD system that significantly reduces the time and expense usually associated with the development of semicustom devices. Advanced CAD tools—such as delay simulation before and after layout, racing check programs, automatic placement and routing, and test program generation—ensure accurate error-free designs.

Master Slice Data

T_A = 0 to +85 °C

	μPD67060	μPD67100
Gate count	6372	10,348
Internal cell count	3096	5060
I/O cell count	180	228
Internal gate delay (typ)	0.67 ns (2-input NAND; F/O = 2, L = 1 mm)	
Input buffer delay (typ)	1.1 ns (F/O = 2, L = 1 mm)	
Output buffer delay (typ)	3.0 ns (C_L = 15 pF)	

Features

- ☐ High speed
  - — Internal gate: 0.67 ns (2-input NAND, F/O = 2, L = 1 mm)
  - — Output buffer: 3.0 ns (C_L = 15 pF, I_{OL} = 24 mA)
  - — Input buffer: 1.1 ns (F/O = 2, L = 1 mm)
  - — Toggle frequency: 120 MHz (worst case, F/O = 3, L = 3 mm)
- ☐ Low power
  - — Internal cell: 18 μW/MHz
  - — Output buffer:
    0.541 mW/MHz (C_L = 15 pF, I_{OL} = 24 mA)
    8.35 mW (standby)
  - — Input buffer:
    26 μW/MHz
    0.77 mW (standby)
- ☐ High-drive output blocks
  - — Buffers and inverters
  - — Logic functions (D-F/F, latch, AND, OR, etc)
  - — 24 mA standard
  - — 48 mA high-current version (two external cells)
  - — Bidirectional
  - — Open-collector
  - — Three-state
  - — Optional pullup or pulldown resistor
- ☐ Input buffers
  - — CMOS level
  - — TTL level
  - — Schmitt trigger
  - — Optional pull-up resistor
- ☐ Large variety of packages
  - — PPGA, CPGA, plastic flatpack, PLCC
  - — 68 to 280 pins
- ☐ Quick turnaround time for prototypes
- ☐ Simple interface to customer's logic diagram and test patterns
- ☐ Advanced CAD tools
  - — Delay simulation
  - — Racing check
  - — Automatic placement and routing
  - — Back annotation from layout (post-layout simulation)
  - — Test program generation
- ☐ Direct access to NEC design centers. Each design center is fully equipped with the latest CAD tools and an experienced staff committed to service.

NEC

NEC Electronics Inc.

CMOS-5 1.2-MICRON CMOS GATE ARRAYS

September 1988

Description

The CMOS-5 gate arrays are low-power, high-speed integrated circuits featuring 1.2-micron silicon-gate CMOS technology. The basic cell on the gate array chip consists of six transistors, three p-channel and three n-channel. See figures 1 and 2.

These application-specific integrated circuits (ASICs) have part numbers in the μPD65000 series. They are available in a variety of sizes (2,000 to 45,000 gates) and packages.

Other NEC publications associated with this data sheet are listed below.

General Design Manual (stock no. 700210)
1.2-Micron CMOS Design Manual (in process)
1.2-Micron CMOS Block Library (in process)
ASIC Package Drawings (stock no. 700348)

Features

- ☐ Technology: 1.2-micron, silicon-gate CMOS; tv or three metal layers
- ☐ High speed
  - — Input buffer: 1.2 ns (F/O = 1, L = 0 mm)
  - — Internal gate: 1 ns (F/O = 3, L = 3 mm)
  - — Power gate: 0.7 ns (F/O = 3, L = 3 mm)
  - — Output buffer: 2.5 ns (C_L = 15 pF)
- ☐ Low power
  - — Internal cell: 12 μW/MHz
  - — Output buffer: 1.5 mW/MHz (C_L = 15 pF)
- ☐ Output current: 3, 6, 12 or 17.5 mA
- ☐ Single + 5-volt power supply
  - — CMOS level: 4.5 to 5.5 V
  - — TTL level: 4.75 to 5.25 V
- ☐ Ambient temperature:
  - — CMOS level: −40 to +85°C
  - — TTL level: 0 to +70°C
- ☐ Block library with more than 140 macros
- ☐ Input buffers
  - — CMOS level
  - — TTL level
  - — Schmitt trigger
  - — With pull-up or pull-down resistor
- ☐ Output buffers
  - — Normal
  - — Open-drain
  - — Three-state
  - — Bidirectional
- ☐ I/O interface: CMOS or TTL compatible
- ☐ Packages
  - — Plastic DIP: 24- to 64-pin
  - — Plastic flatpack: 44- to 160-pin
  - — Plastic LCC: 24- to 84-pin
  - — Plastic PGA: 72- to 280-pin
  - — Ceramic PGA: 72- to 280-pin
- ☐ Supported by advanced CAD tools
  - — Schematic capture
  - — Design rule check
  - — Logic and timing simulation before and after placement and routing
  - — Racing check, setup and hold time check, before and after placement and routing
  - — Automatic placement and routing
  - — Test vector generation if NEC scan path design methodology is used
  - — Test program generation
- ☐ Direct access to NEC design centers through communication network or telephone dial-up
- ☐ Quick turnaround time

Gate Array Sizes

μPD	Gates	Cells	Signal Pads
65025	2016	1344	88
65032	3366	2244	106
65044	4440	2960	120
65051	5292	3528	132
65061	6348	4232	144
65071	7500	5000	156
65082	8748	5832	164
65103	10,800	7200	180
65140	14,256	9504	212
65180	18,144	12,096	244
65240	24,000	16,000	284
65300	30,600	20,400	280
65450	45,012	30,008	334

Notes:

(1) Each signal pad can be used as an input, output, bidirectional, or three-state port.

(2) μPD65300 and μPD65450 have three metal layers.

For literature, call toll-free 8 a.m. to 4 p.m. Pacific time: **1-800-632-3531**

SIERRA SEMICONDUCTOR

Presents

The Industry's Most Comprehensive Standard Cell Solution for CMOS ASIC Designs

- ❑ A Triple Technology™ Process—Integrating Analog, Digital, and EEPROM On a Single Chip
- ❑ The Largest Analog Standard Cell Library in the Industry
- ❑ The Most Extensive EEPROM Library in the Industry
- ❑ A Superior Mixed Analog/Digital Simulation Program–MIXsim
- ❑ Rapid Design Cycles
- ❑ Reduced Development Costs
- ❑ Continuous Software Support
- ❑ Total Responsiveness to Customer Requirements

Find out now if the Sierra solution can economically solve your ASIC design requirements

Simply follow the die size and pin-count calculation procedure in this presentation and you can quickly determine the cost of producing your chip design. All Standard Cells in the enclosed Sierra Library are 2 micron, all-layer CMOS. And of course, Sierra's breakthrough "Triple Technology Process" allows you to integrate Analog, Digital and EEPROM all on a single chip.

Contents

- ☐ An overview of Sierra Semiconductor
- ☐ Cost Calculation Procedure
- ☐ Standard Cell Library
- ☐ The Mentor Connection
- ☐ Presenting MIXsim
- ☐ Applications
- ☐ Plants, Sales Offices, Representatives

SIERRA SEMICONDUCTOR

All About Sierra Semiconductor

■ Company Overview

Sierra Semiconductor is a supplier of CMOS all-layer semicustom application-specific integrated circuits (ASICs) with a complementary portfolio of standard products. The company's cell-based ASIC devices serve a wide base of applications, while the standard products take aim at data communications and telecommunications markets.

The ASIC and standard product lines both take advantage of Sierra's Triple Technology process, which permits the combined integration of analog, digital and EEPROM (electrically erasable and programmable read-only memory) technologies on the same chip. The semicustom devices are fully supported on multiple industry-standard platforms and universal design tools.

Sierra's products are sold primarily to original equipment manufacturers (OEMs) serving the computer, computer peripheral, instrumentation, telecommunications, data communications and business machine markets. The company's products are sold through manufacturers' representatives and distributors in North America, Japan and Southeast Asia. In Europe the company's sales are through Sierra Semiconductor, B.V. headquartered in the Netherlands. Sierra Semiconductor, B.V. also employs manufacturers' representatives.

■ Standard *and* Semicustom

Currently, Sierra's sales are split almost evenly between standard products and semicustom products. Although excellent growth is projected for standard products, the extremely rapid growth of the semicustom market is expected to result in an increasingly higher percentage of the company's total revenues being in semicustom product sales.

Products based on Sierra's standard-cell based ASICs can be designed by either Sierra or its customers exclusively, or jointly. They can be designed at Sierra's four design centers located in San Jose, Boston, Chicago and Europe (Holland). The company will continue to establish additional design centers. As a leading supplier of multiple-technology ASIC devices, Sierra's advantage stems from two disciplines: process innovations and design software.

■ Technology Advantage

The company's Triple Technology process is an advanced CMOS process that permits the integration of digital, analog, and EEPROM non-volatile memory on the same chip. Because most systems employ both analog and digital circuitry, a true "system on a chip" isn't possible unless the digital and analog technologies can be merged. The inclusion of EE memory permits the customer to further customize his products. Sierra's present semicustom standard-cell ASIC library utilizes a 2.0-micron process.

Design software has emerged as a crucial technology in the design of ASIC products. The Company's proprietary Sierra Custom Design System (SCDS) and its Mixed Analog/Digital Simulation software, MIXsim, permits efficient schematic capture, simulation and layout of standard cells, compiled cells, megacells and custom cells. The MIXsim simulator permits the simulation of both digital and analog circuitry—together on the same chip.

Prior to the development of MIXsim, analog and digital circuitry was simulated separately. Predicting the performance of the integrated product was both painstaking and uncertain. The newly introduced MIXsim greatly simplifies the design and simulation effort. Further, it is expected to result in more designs being performed independently by Sierra's customers.

■ Products

Semicustom Products

Sierra's 2.0 micron, all-CMOS product offering consists of a library of over 225 digital, over 50 analog and 25 EEPROM cells. The analog library is both the largest and most advanced library in the industry. The EEPROM library was the industry's first and is the most extensive offered.

Standard Products

The company's standard products are predominantly data communications and telecommunications circuits. The company's Triple Technology™ process is particularly well suited for the manufacture of communication circuits.

The Company's data communications line is anchored by its 1200 BPS modem (the market share leader). The company's year old 2400 BPS modem offerings are expected to emerge strongly in this rapidly developing market. Aggressive development efforts will further broaden the data communications market base served.

The Company's telecommunication product line includes DTMF receivers and transceivers, CODECs, progammable gain/loss circuits, a transcoder, cross point switch, loop back circuit and line equalizer. This rapidly growing line consists of 20+ products, placing it among the broadest in the industry.

■ Manufacturing

Sierra Semiconductor's manufacturing needs are being served by its U.S. wafer fabrication facility, a Far East facility that is currently under construction and through independent foundries.

The company's Calif.-based wafer fabrication and test facility has a capacity of 1,500 5-inch wafers per month. All production-level wafers currently utilize a 2.0-micron CMOS design process. A 1.5-micron library is in prototype and a 1.2-micron process is in development. Ultimately this facility will be used exclusively for engineering development and fast turnaround, small quantity production.

Chartered Semiconductor in Singapore is a wafer facility jointly established by Sierra, National Semiconductor Corporation and Singapore Technology Corporation. This wafer fabrication and test facility, now under construction, will house a Class 1 clean room and will be capable of producing 5,000, 6-inch, sub-micron geometry wafers per month. Sierra will install its Triple Technology process and equip, staff and manage the operation. Chartered Semiconductor will be dedicated to producing high-volume, low-cost, state-of-the-art products for Sierra and other firms (see joint ventures).

■ Facilities

Sierra Semiconductor corporate headquarters are located at 2075 North Capitol Ave., San Jose, Calif. The 115,000-sq. foot facility houses the firm's research, development, engineering, marketing, manufacturing, administration and financial operations, as well as one of its Design Centers. Additional U.S. design centers are located in Chicago, Illinois and Burlington, Massachusetts.

European headquarters are located at the Sierra Semiconductor, B.V. facility in Holland. This facility houses a design center, the product distribution center and a marketing and engineering staff.

■ Alliances

The complexity and capital intensive nature of the semiconductor business virtually dictates that companies either seek out strategic partners or perish. Thus, Sierra is constantly in pursuit of relationships that will strengthen its position. Strategic alliances and joint ventures have figured prominently in the company's successes to date. The company sees no diminution of such relationships in the future.

National Semiconductor Corporation

Since the company's inception, numerous alliances have been consummated with National Semiconductor Corporation. These agreements involved technology exchanges, shared R & D (joint development projects), and a host of other business transactions.

VLSI Technology, Inc

An alliance with VLSI Technology, Inc. has been highly beneficial to both companies—even though the two companies are direct competitors in certain areas. The two companies co-developed a set of design tools and act as second sources to one another.

SIERRA SEMICONDUCTOR

■ Joint Ventures

Three joint ventures, all recent, will have great bearing on Sierra's future.

Sierra Semiconductor, B.V.

In the first quarter of 1987, Sierra Semiconductor, B.V. was formed as a venture capital funded European company located in Holland. It is an independent company in which Sierra owns an 81% equity interest. Financing ($12 million) came from European sources. For Sierra's equity share, the company contributed its technology and granted European marketing rights for Sierra products to the new entity. The joint venture maintains a European design center, a European distribution center, and serves as the European headquarters for Sierra, providing complete technical support for European customers.

Chartered Semiconductor Pte, Ltd.

In November 1987, Chartered Semiconductor Pte, Ltd. was formed as a joint venture between Singapore Technology Corporation, Sierra Semiconductor and National Semiconductor. Chartered Semiconductor is a semiconductor manufacturing company with capacity for fabrication and test of 5,000, 6-inch, sub-micron wafers per month. This entity is scheduled for first wafer production starts in early 1989. Sierra Semiconductor is responsible for installing its Triple Technology process and managing the operation. Over half the output of Chartered Semiconductor is committed to Sierra Semiconductor. The balance is committed to National Semiconductor and Chartered-Sierra.

The ownership of Chartered Semiconductor is:

Singapore Technology Corp.	74%
Sierra Semiconductor Corp.	17%
National Semiconductor Corp.	9%
Total:	100%

The bulk of the approximately $50 million in financing is being provided by Singapore. Sierra contributes technology, training, and management for its share. National contributes technology and technical assistance for its share.

Chartered-Sierra Pte, Ltd.

Also in November, 1987, Chartered-Sierra Pte, Ltd. was formed as a joint venture between Sierra Semiconductor and Singapore Technology Corporation. Chartered-Sierra will consist of a design center and a marketing and design staff to serve and support the very fast growing Southeast Asian Market. Chartered-Sierra will be staffed by Singaporean design engineers who have been trained at Sierra's San Jose, Calif. facility. (Over 15 have been in training since late 1986).

The Standard-Cell Solution to ASIC Design

■ An hour of your time can save you thousands of dollars

■ Follow this easy calculation procedure. Call Sierra with the results — get a price!

You can quickly find out how much it would cost to convert your existing analog/digital design into a Sierra Semicustom chip. You can then compare the cost of the Sierra solution to the cost of producing your circuit as you do now, and see for yourself whether our system-on-a-chip technology makes sense for your designs.

The cost of an ASIC depends primarily on the amount of chip area it takes. Therefore, the calculation described here determines the chip area, or die size, your design will require. When you have calculated this area, a call to Sierra gives you the approximate cost of the final chip. You are under no obligation; we simply give you a price for our service and you make up your own mind. If you've ever wondered how much it would cost to move your complete analog/digital design onto one chip, now is the time to find out.

To do this calculation, you need:

- ❑ The information provided in this insert.
- ❑ Information about your design.

The die size required for your design depends on two primary factors: the amount of circuitry you have and the number of pins needed for signals going to and from the chip. If your design has a lot of circuitry and only a few I/O pins, the amount of circuitry will determine the die size. However, if your design requires a relatively large number of I/O pins, this factor could be more important in determining the die size.

Many designs cannot be 100% implemented with the Standard Cell Library, which will require some custom work by Sierra. After you calculate die size, define to Sierra the circuitry that requires custom work. Die Sizes up to 250 mils are usually very economical. 250 to 500 mils are typically expensive. Over 500 mils are normally impractical.

The calculations that follow are thus in two steps. In the first step, you calculate the chip area your circuitry alone (without I/O pins) will occupy on the chip. This area is known as the core area. Then in the second step, you determine how much chip area you need for I/O pins. By adding the I/O pin area to the core area, you obtain the total die size.

■ STEP 1 Determine the Core Area

To calculate the core area of your design, you begin by finding your design criteria in the Sierra Standard Call library (immediately following this calculation procedure). For the digital functions in your circuit, you replace the digital functions with the Sierra gate equivalents listed in the library.

There are many types of functions in the library, including digital, analog and EEPROM. When you replace these types of components in your circuit with the Sierra library counterparts, you will find specific information needed for the die size calculation.

■ STEP 1
(CONTINUED)

■ **The Number of Gates:** This applies to digital SSI/MSI functions and rugged EE Logic. Every digital function in the Sierra library is implemented using a specific number of gate equivalents. These gate equivalents are given in the library listing in this insert. Because each gate equivalent takes up a certain amount of die area, you must determine the total *Number of Gates* needed to implement the digital parts of your design.

■ **The ICF Area:** This is the "interconnect factor" for your circuit, which is the amount of interconnection between your circuit's components. The more components you have, the more area is required for interconnections. To approximate the amount of *ICF area* your circuit will need, consult the following table, noting that this ICF value applies only to digital functions:

Number of Gates	ICF	Number of Gates	ICF
0 - 1000	1.75	4000 - 6000	3.0
1000 - 2000	2.0	6000 - up	3.5
2000 - 4000	2.5		

■ **The Analog Area.** This applies to all the analog functions. The library listings give the die area required for each analog function you need to implement your circuit. You must determine the total **Analog Area** occupied by all your analog circuitry.

■ **The EEPROM Area.** This is the total area occupied by any EEPROM arrays and power supplies in the circuit. The library listings give specific areas for different EEPROM array sizes.

■ **The Compiled Area.** Any RAM, ROM, Multipliers, 2901 Data Paths or PLAs in your circuit area are implemented using a compiler, a software tool that creates any array configuration you want. The area required for RAM and ROM can be found from the tables provided. The area for multipliers, C2901 Data Paths and PLAs can be calculated using the formulas provided.

Once you get these area figures, you feed them into the following equation:

Core Area = [(Number of Gates * 2.1 * ICF) + (Analog Area + EEPROM Area + Compiled Area) * 1.35]

The 2.1 constant in this equation represents the die area required for each gate equivalent. Thus, the first parenthetical term calculates the area taken up by your digital circuitry, including the interconnect factor for the analog and memory blocks.

Once you have filled in all the variables and done the calculations, you get your core area in square mils. You must then convert the *Core Area* into a measure of the *Core Edge*: the length of one side of the *Core Area*. Because the *Core Area* is a square, you find the *Core Edge* by taking the square root of the *Core Area*:

Core Edge = $\sqrt{\text{Core Area}}$

■ STEP 2 Determine the Total Die Size

The *Core Edge* value is needed to calculate the I/O pin area in Step 2.

To complete the die size calculation, you need two pieces of information:

■ **The core edge** value calculated in Step 1.

■ **The number of pads** required for your design; that is, the number of I/O pins needed. (Each I/O pin connects to a pad area on the edge of your chip, so the chip must provide enough edge space to accommodate all the pads.) Now, calculate the number of *pads per side,* which equals the total *Number of Pads* divided by 4, then rounded up to an even number.

Using this information, perform the following test:

If **Core Edge** +10 > **(Pads Per Side)**(12.5)-13 then your design is core limited, and your final die size equals the greater of the following calculations:

Core Edge + 43

or

(Pads Per Side *12.5) + 33

If the test is not true for your circuit, then your design is probably pad limited, and your final Die Size equals the greater of the following calculations:

Core Edge + 43

or

(Pads Per Side - 2) * 7.5 + 47

The calculations in Step 2 include several factors dealing with the layout of semicustom chip. The test performed at the beginning of Step 2 is to determine whether the die size of your design is dependent on the size of your core (core limited) or the number of pads you must fit onto the chip (pad limited). The constant 10 in this test represents the power and ground routing area of the core; 12.5 is the width of the row of core-limited pads along the chip's edge; and 13 is a factor representing the grey area between a pad limited and a core limited design.

The two choices given for calculating die size for pin-limited and pad-limited cases help ensure the most accurate results. The second choice in each case (the calculation involving the **Pads Per Side**) represents a chip that is not clearly core or pad limited. By taking the greater of the two choices, you get a conservative estimate of die size. Note that you can also use the calculations for the different cases as a way of guiding tradeoffs between gates and pads, which helps you achieve the smallest die size.

Most of the constants in the calculations (43, 33, and 47) represent areas that are present in every chip. As for other constants, the 7.5 represents that pitch between pad-limited pads; 2 is subtracted from the **Pads Per Side** value because two pads can be placed in the chips corners.

Once you have calculated the die size for your design, call Sierra Custom Marketing at (408) 263-9300 to get a quote on how much your chip would cost. You might be amazed at how much our system-on-a-chip ASICs can save you.

Sierra SCDS™ 2-Micron CMOS Cell Library

■ Analog Cell Library

All analog specifications are typical, 5V, 25°C, and use a single 5V supply, unless otherwise indicated.

ANALOG-to-DIGITAL CONVERTERS

NAME	DESCRIPTION	CONVERSION TIME	NON-LINEARITY INTEGRAL	NON-LINEARITY DIFFERENTIAL	SIZE SQ. MILS
ADC4BT	4-bit flash	300 nsec	0.25 LSB	0.25 LSB	1589
ADC8BT	8-bit successive approximation	3 µsec	0.5 LSB	0.5 LSB	2833
ADC10B	10-bit successive approximation	10 µsec	0.5 LSB	0.5 LSB	2671
ADC12B	12-bit dual slope	100msec	0.5 LSB	0.2 LSB	1743
HADC8B	8-bit high speed	500 nsec	0.5 LSB	0.5 LSB	4800

DIGITAL-to-ANALOG CONVERTERS

NAME	DESCRIPTION	SETTLING TIME	NON-LINEARITY INTEGRAL	NON-LINEARITY DIFFERENTIAL	SIZE SQ. MILS
DAC4BT	4-bit flash, current output	30nsec	0.1 LSB	0.1 LSB	603
DAC8BT	8-bit resistor string, voltage output	1.5µsec	0.5 LSB	0.1 LSB	2036
DAC10B	10-bit charge integration	5µsec	0.5 LSB	0.5 LSB	2450
FDAC8B	8-bit flash, current output	20nsec	0.5 LSB	0.5 LSB	3780

OPERATIONAL AMPLIFIERS

NAME	GAIN	BAND-WIDTH	PHASE MARGIN	SLEW RATE	POWER	P-P VOLTS	LOAD	SIZE SQ. MILS
OP02IB	89DB	2.8MHz	67	4V/µsec	4.6mW	4.2V	2k/100pF	378
OP10IB	90dB	3.5MHz	70	4V/µsec	2.1mW	4.4V	10k/50pF	286
OP20IB	90dB	2.9MHz	65	4V/µsec	1.7mW	4.4V	20k/50pF	276
OP02EB	89dB	2.8MHz	67	4V/µsec	4.6mW	4.2V	2k/100pF	506
OP10EB	90dB	3.5MHz	70	4V/µsec	2.1mW	4.4V	10k/50pF	368
OP20EB	90dB	2.9MHz	65	4V/µsec	1.7mW	4.4V	20k/50pF	353
OP10ID	66dB	2.5MHz	75	7V/µsec	3.2mW	3.5V	10k/50pF	153
OP20ID	69dB	3.0MHz	65	9V/µsec	2.5mW	3.5V	20k/30pF	133
OP10ED	66dB	2.5MHz	75	7V/µsec	3.2mW	3.5V	10k/50pF	256
OP20ED	69dB	3.0MHz	65	9V/µsec	2.5mW	3.5V	20k/30pF	240

1. The suffix "I" or "E" in the cell name means internal and external, respectively. "E" type op amps drive off-chip loads.
2. Output current is specified driving minimum Resistive and maximum Capacitive Loads. The R value is indicated by the number in the Op Amp's cell name, and has units in kΩ. Typical input current is negligible. Input offset voltage < 10mV.
3. P-P Volts = peak-to-peak output Voltage swing.

ANALOG MULTIPLEXERS/SWITCHES

NAME	FUNCTION	RDS ON*	SIZE SQ. MILS	NAME	FUNCTION	RDS ON*	SIZE SQ. MILS
M21200	2:1 ANALOG MUX	200Ω	229	M4110K	4:1 ANALOG MUX	10000Ω	133
M2101K	2:1 ANALOG MUX	1000Ω	143	ASW200	ANALOG SWITCH	200Ω	153
M2110K	2:1 ANALOG MUX	10000Ω	123	ASW01K	ANALOG SWITCH	1000Ω	97
M41200	4:1 ANALOG MUX	200Ω	358	ASW10K	ANALOG SWITCH	10000Ω	87
M4101K	4:1 ANALOG MUX	1000Ω	235				

*RDS ON = peaks on resistance (worst case: 4.5-5.5V, 0-70°C)

POWER-ON-RESET/LOW VOLTAGE DETECT

NAME	DESCRIPTION	Vtrip-*	Vtrip+*	Vhyst	SIZE SQ. MILS
PORID1	Threshold reference POR	1.5V	3.8V	0.7V	163
LVDET1	Band Gap reference POR	3.7V	4.5V	0.2V	736

*Worst case: 4.5-5.5V, 0-70°C

VCO/RC OSCILLATORS/PLL

NAME	MAX. FREQUENCY	FREQUENCY ACCURACY	VCO LINEARITY	POWER	SIZE SQ. MILS
OSCHEB	500kHz	10%	0.5%	5.0mW	399
OSCLEB	50kHz	10%	0.7%	3.5mW	342
PLL34M	34MHz Phase lock subsystem	5%	2.0%	200mW	3224

■ Analog Cell Library (CONTINUED)

CRYSTAL OSCILLATORS

NAME	FREQUENCY	NAME	FREQUENCY	
OSC32K	32-100kHz	OSC16B	12-20MHz	
OSC04B	2-6MHz	OSC25B	20-30MHz	These are Bonding-Pad Cells
OSC08B	6-12MHz	OSC45B	30-50MHz	

VOLTAGE COMPARATORS

NAME	GAIN	RESPONSE TIME†	INPUT RANGE††	POWER	Vos	SIZE SQ. MILS
CPHSIB	120dB	80ns	3.5V	3.0mW	5.0mV	97
CPLSIB	106dB	350ns	3.2V	1.0mW	5.0mV	51
CPVHS1	60dB	15ns	2.5V	2.0mW	10mV	61
CPVLO1	80dB	500ns	5.0V	1.0mW	0.5mV	220
CPVLP1	80dB	5µs	3.7V	75µW	5.0mV	75

† For ±10mV input overdrive (except CPVHSI with ±300mV).

†† Input Range = common mode.

RS422 TYPE DRIVER/RECEIVER

		SIZE SQ. MILS
RSRCVR	RS422 TYPE DIFFERENTIAL RECEIVER	185
RSDRVR	RS422 TYPE DIFFERENTIAL DRIVER	114

ANALOG-REFERENCE-AMPLIFIER

		SIZE SQ. MILS
REFAMP	Unity gain op-amp used to buffer a mid-supply analog ground reference. Power = 4mW	174

VOLTAGE-TO-CURRENT CONVERTER

NAME	INPUT RANGE	OUTPUT RANGE	POWER	SIZE SQ. MILS
VTCCEI	0 - 2.5V	0 - 50µA	2.0mW	189

■ Non-volatile Library

RUGGED EELOGIC†

NAME	DESCRIPTION	WRITE CYCLE	GATES
EEDFF1	1-BIT EE D-FLIP FLOP	10ms	32
EEDLTH	1-BIT EE DATA LATCH	10ms	27
EESRLT	1-BIT EE SET-RESET LATCH	10ms	26
EEDFFC	4-BIT EE D REGISTER WITH CLEAR	10ms	86
EEDFSC	4-BIT EE D REGISTER WITH CLEAR, PRESET	10ms	103
EEDFST	4-BIT EE D REGISTER	10ms	103
EENLAC	4-BIT EE LATCH WITH CLEAR	10ms	74
EETFST	4-BIT EE COUNTER WITH PARALLEL LOAD	10ms	98

† Rugged EE is a failure tolerant, redundant dual-transistor cell design that facilitates simple application and testing. The term "EE" is for electrically eraseable; all EELOGIC devices are electrically eraseable and programmable.

RUGGED EEPROM†

NAME	TOTAL†† BITS	DESCRIPTION	WRITE CYCLE	ACCESS TIME	SIZE SQ. MILS
EEARRY	16	16 x 1 EEPROM ARRAY	10ms	125ns	800
	32	32 x 1 EEPROM ARRAY	10ms	125ns	1000
	64	64 x 1,16 x 4, 8 x 8 EEPROM ARRAY	10ms	125ns	1500
	128	128 x 1, 32 x 4, 16 x 8, 8 x 16 EEPROM ARRAY	10ms	125ns	2300
	256	64 x 4, 32 x 8, 16 x 16 EEPROM ARRAY	10ms	125ns	3100

† Rugged EE is a failure tolerant, redundant dual transistor cell design which facilitates simple application and testing.

†† Larger arrays are available on a custom basis; consult factory.

PROGRAMMING SUPPLIES

NAME	DESCRIPTION	MAX BITS	SIZE SQ. MILS
EEHVP1	PORT FOR CONTROLLED EXTERNAL VPP	4096	36
EEHVI2	CONTROLLER FOR EXTERNAL VPP	4096	550
EEHVS2	INTERNAL VPP GENERATOR	256	1070

Programming supply operation is 4.5V to 5.5V Tj = 0° to 85°C, unless otherwise indicated.

BUFFERS

NAME	DESCRIPTION	SPEED	EQUIVALENT GATES
CK01D1	NON-INVERTING CLOCK BUFFER, 1X DRIVE	3.3	1
CK01D2	NON-INVERTING CLOCK BUFFER, 2X DRIVE	2.2	2
CK01D3	NON-INVERTING CLOCK BUFFER, 3X DRIVE	2.0	3
CK02D1	INVERTING CLOCK BUFFER, 1X DRIVE	2.3	1
CK02D2	INVERTING CLOCK BUFFER, 2X DRIVE	1.7	2
CK02D3	INVERTING CLOCK BUFFER, 3X DRIVE	1.5	3
IN01D1	INVERTING BUFFER, 1X DRIVE	1.4	1
IN01D2	INVERTING BUFFER, 2X DRIVE	1.4	1
IN01D3	INVERTING BUFFER, 3X DRIVE	0.7	2
IT01D1	INVERTING 3-STATE BUFFER WITH OE, 1X DRIVE	2.0	2
IT01D2	INVERTING 3-STATE BUFFER WITH OE, 2X DRIVE	2.0	2
IT01D3	INVERTING 3-STATE BUFFER WITH OE, 3X DRIVE	2.0	3
IT02D1	INVERTING 3-STATE BUFFER WITH OEN, 1X DRIVE	2.2	2
IT02D2	INVERTING 3-STATE BUFFER WITH OEN, 2X DRIVE	2.0	3
IT02D3	INVERTING 3-STATE BUFFER WITH OEN, 3X DRIVE	2.0	3
NI01D1	NON-INVERTING BUFFER, 1X DRIVE	3.0	1
NI01D2	NON-INVERTING BUFFER, 2X DRIVE	1.8	2
NI01D3	NON-INVERTING BUFFER, 3X DRIVE	2.3	2
NT01D1	NON-INVERTING 3-STATE BUFFER WITH OE, 1X DRIVE	2.0	2
NT01D2	NON-INVERTING 3-STATE BUFFER WITH OE, 2X DRIVE	2.0	3
NT01D3	NON-INVERTING 3-STATE BUFFER WITH OE, 3X DRIVE	2.2	4
NT02D1	NON-INVERTING 3-STATE BUFFER WITH OEN, 1X DRIVE	5.1	2
NT02D2	NON-INVERTING 3-STATE BUFFER WITH OEN, 2X DRIVE	2.3	3
NT02D3	NON-INVERTING 3-STATE BUFFER WITH OEN, 3X DRIVE	2.3	4

GATES

NAME	DESCRIPTION	SPEED	EQUIVALENT GATES
AN02D1	2-INPUT AND	2.3	2
AN03D1	3-INPUT AND	3.5	2
AN04D1	4-INPUT AND	2.5	3
AN05D1	5-INPUT AND	2.5	3
AN06D1	6-INPUT AND	3.1	4
AN07D1	7-INPUT AND	3.6	4
AN08D1	8-INPUT AND	3.6	5
AO01D1	2/2 AND-OR-INVERT	2.9	2
AO02D1	3/3 AND-OR-INVERT	3.2	3
AO03D1	2/2/1 AND-OR-INVERT	3.6	3
AO04D1	2/1 AND-OR-INVERT	2.6	2
AO05D1	2/1/1 AND-OR-INVERT	4.0	2
ND02D1	2-INPUT NAND	1.5	1
ND03D1	3-INPUT NAND	2.5	2
ND04D1	4-INPUT NAND	3.0	2
ND05D1	5-INPUT NAND	3.3	3
ND06D1	6-INPUT NAND	4.4	3
ND07D1	7-INPUT NAND	4.5	4
ND08D1	8-INPUT NAND	6.6	4
NR02D1	2-INPUT NOR	2.8	1
NR03D1	3-INPUT NOR	3.5	2
NR04D1	4-INPUT NOR	4.2	2
NR05D1	5-INPUT NOR	5.7	3
NR06D1	6-INPUT NOR	7.7	3
NR07D1	7-INPUT NOR	8.8	4
NR08D1	8-INPUT NOR	11.7	4
OA01D1	2/2 OR-AND-INVERT	2.9	2
OA02D1	3/3 OR-AND-INVERT	5.6	3
OA03D1	2/2/1 OR-AND-INVERT	3.3	3
OA04D1	2/1 OR-AND-INVERT	2.8	2
OA05D1	2/1/1 OR-AND-INVERT	3.1	2
OR02D1	2-INPUT OR	2.6	2
OR03D1	3-INPUT OR	3.6	2
OR04D1	4-INPUT OR	4.7	3
OR05D1	5-INPUT OR	4.2	3
OR06D1	6-INPUT OR	4.7	4
OR07D1	7-INPUT OR	5.5	4
OR08D1	8-INPUT OR	5.4	5
XN02D1	2-INPUT EXCLUSIVE NOR	2.7	3
XO02D1	2-INPUT EXCLUSIVE OR	3.9	3

DECODERS/MULTIPLEXERS

NAME	DESCRIPTION	SPEED	EQUIVALENT GATES
DC24D1	2-TO-4 LINE DECODER	14.1	5
DC38D1	3-TO-8 LINE DECODER	5.3	14
DE24D1	2-TO-4 LINE DECODER WITH ENABLE	6.2	8
ME41D1	4-TO-1 MULTIPLEXER WITH ENABLE	8.9	9
MX21D1	2-TO-1 MULTIPLEXER	4.1	3
MX41D1	4-TO-1 MULTIPLEXER	5.8	7
MX81D1	8-TO-1 MULTIPLEXER	10.3	16

ARITHMETIC FUNCTIONS

NAME	DESCRIPTION	SPEED	EQUIVALENT GATES
AD01D1	1-BIT FULL ADDER	10.4	10
AD02D1	2-BIT FULL ADDER	11.9	18
AS01D1	1-BIT ADDER/SUBTRACTOR	10.4	12
AS02D1	2-BIT ADDER/SUBTRACTOR	11.9	23

FLIP-FLOPS/LATCHES

NAME	DESCRIPTION	SPEED	EQUIVALENT GATES
DFBNNB	D FLIP-FLOP WITH CLEAR, PRESET, BUFFERED OUTPUTS	63	8
DFBNNN	D FLIP-FLOP WITH CLEAR, PRESET	72	7
DFBNNT	D FLIP-FLOP WITH CLEAR, PRESET, 3-STATE OUTPUT	63	10
DFBTNB	BUFFERED D FLIP-FLOP WITH CLEAR, PRESET	56	9
DFBTNN	D FLIP-FLOP WITH CLEAR, PRESET, BUFFERED CLOCK	55	9
DFBTNT	BUFFERED D FLIP-FLOP WITH CLEAR, PRESET, 3-STATE OUTPUT	55	11
DFCNNB	D FLIP-FLOP WITH CLEAR, BUFFERED OUTPUTS	69	7
DFCNNN	D FLIP-FLOP WITH CLEAR	77	6
DFCNNT	D FLIP-FLOP WITH CLEAR, 3-STATE OUTPUT	69	9
DFCTNB	BUFFERED D FLIP-FLOP WITH CLEAR	58	8
DFCTNN	D FLIP-FLOP WITH CLEAR, BUFFERED CLOCK	—	7
DFCTNT	BUFFERED D FLIP-FLOP WITH CLEAR, 3-STATE OUTPUT	58	10
DFNNNB	D FLIP-FLOP WITH BUFFERED OUTPUTS	73	6
DFNNNN	D FLIP-FLOP	26	5
DFNNNT	D FLIP-FLOP WITH 3-STATE OUTPUT	67	8
DFNTNB	BUFFERED D FLIP-FLOP	61	7
DFNTNN	D FLIP-FLOP WITH BUFFERED CLOCK	—	6
DFNTNT	BUFFERED D FLIP-FLOP WITH 3-STATE OUTPUT	61	9
DFPNNB	D FLIP-FLOP WITH PRESET, BUFFERED OUTPUTS	61	7
DFPNNN	D FLIP-FLOP WITH PRESET	83	6
DFPNNT	D FLIP-FLOP WITH PRESET, 3-STATE OUTPUT	56	9
DFPTNB	BUFFERED D FLIP-FLOP WITH PRESET	51	8
DFPTNN	D FLIP-FLOP WITH PRESET, BUFFERED CLOCK	—	7
DFPTNT	BUFFERED D FLIP-FLOP WITH PRESET, 3-STATE OUTPUT	51	10
JKBNNB	JK FLIP-FLOP WITH CLEAR, PRESET, BUFFERED OUTPUTS	57	11
JKBNNN	JK FLIP-FLOP WITH CLEAR, PRESET	59	10
JKBNNT	JK FLIP-FLOP WITH CLEAR, PRESET, 3-STATE OUTPUT	48	12
JKBTNB	BUFFERED JK FLIP-FLOP WITH CLEAR, PRESET	43	12
JKBTNN	JK FLIP-FLOP WITH CLEAR, PRESET, BUFFERED CLOCK	—	11
JKBTNT	BUFFERED JK FLIP-FLOP WITH CLEAR, PRESET, 3-STATE OUTPUT	44	13
JKCNNB	JK FLIP-FLOP WITH CLEAR, BUFFERED OUTPUTS	63	10
JKCNNN	JK FLIP-FLOP WITH CLEAR	63	9
JKCTNB	BUFFERED JK FLIP-FLOP WITH CLEAR	50	11
JKCTNN	JK FLIP-FLOP WITH CLEAR, BUFFERED CLOCK	—	10
JKNNNB	JK FLIP-FLOP WITH BUFFERED OUTPUTS	46	9
JKNNNN	JK FLIP-FLOP	60	8
JKNTNB	BUFFERED JK FLIP-FLOP	46	10
JKNTNN	JK FLIP-FLOP WITH BUFFERED CLOCK	—	9
LABFNB	BUFFERED LATCH WITH CLEAR, PRESET	63	6
LABFNN	LATCH WITH CLEAR, PRESET, BUFFERED CLOCK	—	6
LABFNT	BUFFERED LATCH WITH CLEAR, PRESET, 3-STATE OUTPUT	63	8
LABNNB	LATCH WITH CLEAR, PRESET, BUFFERED OUTPUTS	71	5
LABNNN	LATCH WITH CLEAR, PRESET	88	4
LABNNT	LATCH WITH CLEAR, PRESET, 3-STATE OUTPUT	71	7
LACFNB	BUFFERED LATCH WITH CLEAR	51	5
LACFNN	LATCH WITH CLEAR, BUFFERED CLOCK	—	4
LACFNT	BUFFERED LATCH WITH CLEAR, 3-STATE OUTPUT	48	7
LACNNB	LATCH WITH CLEAR, BUFFERED OUTPUTS	63	4
LACNNN	LATCH WITH CLEAR	84	3
LACNNT	LATCH WITH CLEAR, 3-STATE OUTPUT	63	6

■ Digital Cell Library (CONTINUED)

FLIP-FLOPS/LATCHES (CONTINUED)

LACTNN	LATCH WITH CLEAR, ACTIVE HIGH BUFFERED CLOCK	—	4
LANFNB	BUFFERED LATCH	58	5
LANFNN	LATCH WITH BUFFERED CLOCK	—	6
LANFNT	BUFFERED LATCH WITH 3-STATE OUTPUT	56	6
LANNNB	LATCH WITH BUFFERED OUTPUTS	70	4
LANNNN	LATCH	113	3
LANNNT	LATCH WITH 3-STATE OUTPUT	71	5
LANTNB	BUFFERED LATCH, ACTIVE HIGH BUFFERED CLOCK	—	5
LANTNN	LATCH WITH ACTIVE HIGH BUFFERED CLOCK	—	4
LAPFNB	BUFFERED LATCH WITH PRESET	77	6
LAPFNN	LATCH WITH CLEAR, PRESET, BUFFERED CLOCK	—	5
LAPFNT	BUFFERED LATCH WITH PRESET, 3-STATE OUTPUT	77	7
LAPNNB	LATCH WITH PRESET, BUFFERED OUTPUTS	83	5
LAPNNN	LATCH WITH PRESET	45	4
LAPNNT	LATCH WITH PRESET, 3-STATE OUTPUT	83	6
MFBTNB	BUFFERED MUX FLIP-FLOP WITH CLEAR, PRESET	55	11
MFBTNT	BUFFERED MUX FLIP-FLOP WITH CLEAR, PRESET, 3-STATE OUTPUT	55	13
MFCTNB	BUFFERED MUX FLIP-FLOP WITH CLEAR, BUFFERED CLOCK, BUFFERED O/P	51	11
SCBNNB	SYNCHRONOUS COUNTER WITH CLEAR, PRESET, BUFFERED OUTPUTS	53	11
SCBNNN	SYNCHRONOUS COUNTER WITH CLEAR, PRESET	53	10
SCBNNT	SYNCHRONOUS COUNTER WITH CLEAR, PRESET, 3-STATE OUTPUTS	48	13
SCBTNB	BUFFERED SYNCHRONOUS COUNTER WITH CLEAR, PRESET	40	12
SCBTNN	SYNCHRONOUS COUNTER WITH CLEAR, PRESET, BUFFERED CLOCK	—	11
SCBTNT	BUFFERED SYNCHRONOUS COUNTER WITH CLEAR, PRESET, 3-STATE O/P	40	14
SCCNNB	SYNCHRONOUS COUNTER WITH CLEAR, BUFFERED OUTPUTS	63	10
SCCNNN	SYNCHRONOUS COUNTER WITH CLEAR	63	9
SCCNNT	SYNCHRONOUS COUNTER WITH CLEAR, 3-STATE OUTPUT	48	12
SCCTNB	BUFFERED SYNCHRONOUS COUNTER WITH CLEAR	37	11
SCCTNN	SYNCHRONOUS COUNTER WITH CLEAR, BUFFERED CLOCK	—	10
SCCTNT	BUFFERED SYNCHRONOUS COUNTER WITH CLEAR, 3-STATE OUTPUT	38	13
TFBNNB	T FLIP-FLOP WITH CLEAR, PRESET, BUFFERED OUTPUTS	63	8
TFBNNN	T FLIP-FLOP WITH CLEAR, PRESET	74	7
TFBNNT	T FLIP-FLOP WITH CLEAR, PRESET, 3-STATE OUTPUT	63	10
TFBTNB	T FLIP-FLOP WITH CLEAR, PRESET	53	9
TFCNNB	T FLIP-FLOP WITH CLEAR, BUFFERED OUTPUTS	74	7
TFCNNN	T FLIP-FLOP WITH CLEAR	88	6
TFCTNB	T FLIP-FLOP WITH CLEAR	62	8
TFPNNB	T FLIP-FLOP WITH PRESET, BUFFERED OUTPUTS	69	7
TFPNNN	T FLIP-FLOP WITH PRESET	72	6

■ Pads, Pad Drivers, Level Shifters

POWER PADS

NAME	DESCRIPTION	NAME	DESCRIPTION
PCVSS1	Vss PAD FOR CORE	PCVDD1	VDD PAD FOR CORE
PCVSS2	Vss PAD FOR I/O CELLS	PCVDD2	VDD PAD FOR I/O CELLS
PCVSS3	Vss PAD FOR BOTH (tied at pad)	PCVDD3	VDD PAD FOR BOTH (tied at pad)

OUTPUT PADS

PC7O01	OUTPUT PAD (2mA)	PD8OB3	OUTPUT PAD (24mA)
PC7O02	OUTPUT PAD (4mA)	PD8OB5	OUTPUT PAD (40mA)
PC7O03	OUTPUT PAD (8mA)	PD8OB6	OUTPUT PAD (48mA)

OUTPUT PADS WITH INPUT LEVEL-SHIFTER BUFFERS

PC7T01	OUTPUT PAD WITH TTL INPUT (2mA)	PC7C01	OUTPUT PAD WITH CMOS INPUT (2mA)
PC7T02	OUTPUT PAD WITH TTL INPUT (4mA)	PC7C02	OUTPUT PAD WITH CMOS INPUT (4mA)
PC7T03	OUTPUT PAD WITH TTL INPUT (8mA)	PC7C03	OUTPUT PAD WITH CMOS INPUT (8mA)

INPUT LEVEL-SHIFTERS

NAME	DESCRIPTION	EQUIVALENT GATES	NAME	DESCRIPTION	EQUIVALENT GATES
PC7T00	TTL INPUT PAD and BUFFER	2	SCH01T	SCHMITT TTL INPUT BUFFER	3
PC7C00	CMOS INPUT PAD and BUFFER	2	SCH01C	SCHMITT CMOS INPUT BUFFER	3

PAD DRIVERS

NAME	DESCRIPTION	EQUIVALENT GATES	NAME	DESCRIPTION	EQUIVALENT GATES
PT01D1	NON-INVERTING WITH OE	7	PT04D1	INVERTING WITH OEN	7
PT02D1	NON-INVERTING WITH OEN	8	PT05D1	INVERTING	5
PT03D1	INVERTING WITH OE	7	PT06D1	NON-INVERTING	6

■ Digital Cell Library (CONTINUED)

COP800 CORE MICROCONTROLLER FAMILY

NAME	DESCRIPTION	SIZE SQ. MILS
COP800	8-BIT BASE CORE MICROCONTROLLER	4330

NAME	DESCRIPTION	SIZE SQ. MILS	DESCRIPTION	SIZE SQ. MILS
MEMORY	1K-BYTE ROM	+1674	64-BYTE RAM	+1768
ADDER	2K-BYTE ROM	+2594	128-BYTE RAM	+3002
	4K-BYTE ROM	+4446	192-BYTE RAM	+4236
	8K-BYTE ROM	+8136		

SOFT MACRO PERIPHERALS

NAME	DESCRIPTION	EQUIVALENT GATES
COPLCD	36-SEGMENT TRIPLEX LCD CONTROLLER	950
COPIP8	8-BIT INPUT PORT	70
COPOP8	8-BIT OUTPUT PORT	120
COPBP8	8-BIT INPUT/OUTPUT PORT	200
COPRTC	REAL TIME CLOCK (EQUIVALENT TO NSC 58174)	1848

CUSTOM SOFT MACRO PERIPHERALS

KEYBOARD ENCODER WATCHDOG TIMER UART (8250 SUBSET)

COPS is a trademark of National Semiconductor Corporation

■ Compiler Library

COMPILERS

NAME	TOTAL BITS	ORGANIZATION	MAXIMUM ACCESS TIME	SIZE SQ. MILS
RAM	512	64 × 8, 128 × 4	30ns	2025
	1024	128 × 8, 256 × 4	31ns	3015
	2048	128 × 16, 256 × 8, 512 × 4	33ns	4891
	4096	128 × 32, 256 × 16, 512 × 8, 1024 × 4	35ns	8176
	8192	256 × 32, 512 × 16, 1024 × 8, 2048 × 4	39ns	14560
	16384	512 × 32, 1024 × 16, 2048 × 8, 4096 × 4	43ns	26130

			SIZE (SQUARE MILS)			
NAME	WORDS	NUMBER OF OUTPUTS:	4	8	16	32
ROM	64		867	1173	1786	2093
	128		967	1302	1972	3312
	256		1183	1575	2358	3925
	512		1156	2062	3073	5095
	1024		—	3077	4543	7476
	2048		—	5058	7435	12189

NAME	SIZE CALCULATION
2901 Data Path	(Nram × 2.83 + 54)(Nbit × 4.00 + 16) = Size (Square Mils) Nram = No. of RAM words (2,3,4,...16); Nbit = No. of bits per word (2,3,4,...80)
N × M Multiplier	For N < 20, Size is: [(N + 1) × 6.57 + 21.1] [(M/2 - 2) × 12.76 + 31.26] = Size (Square Mils) For N > 20, Size is: [(N + 1) × 6.57 + 29.23] [(M/2 - 2) × 12.76 + 31.26] = Size (Square Mils) N = Width of 1st word (8,10,12...32); M = Width of 2nd word (8,10,12...32)
PLA	(0.65 Inputs + .33 Outputs + 13.25) × (.66Minterms + 10.57) = Size (Square Mils) Inputs are 1,2,3,...50 Outputs are 4,8,12,...52 Minterms are 4,8,12,...200

Sierra's Unique Mentor Mixed Analog-Digital Design Methodology

Sierra Semiconductor's Mentor Design Kit allows designers the methodology, cell library, and software to design complex Triple Technology circuits. The Sierra Mentor Design Kit includes the following features:

- ❑ Over 50 analog symbols
- ❑ Over 25 EEPROM symbols and simulation models
- ❑ Over 225 digital symbols and simulation models
- ❑ A mixed analog-digital netlist screener
- ❑ Analog interface models
- ❑ Easy transfer to MIXsim
- ❑ Analog ASIC design consultation

■ Netlist Screener

Sierra's netlist screener checks circuit designs for common digital and analog errors. This allows designers to catch common mistakes in both the analog and digital portions of the circuit. This includes such things as connectivity, fan outs, and checking for shorts.

■ Analog Interface Models

Analog interface models allow designers to do a functional verification of the digital portion of the circuit, to assure that the interface to the analog portion of the circuit is correct. So before circuits are submitted to Sierra for final MIXsim verification, the designer is assured that key timing and interface criteria are met. The interface models are not a substitute for MIXsim verification but allow designers to verify the interface between analog and digital blocks, assure correct signal polarity, and minimize the debugging required once MIXsim circuit simulation is done.

■ Easy Transfer to MIXsim

Once the design has been verified on Sierra's Mentor Design Kit the circuit is transferred to the Sierra Design Center for verification using Sierra's proprietary mixed analog-digital simulator MIXsim. The circuit is then reviewed by Sierra's analog design engineering staff before and after layout.

■ Engineering Support

To assist circuit designers in the idiosyncracies of analog cell based ASIC design, Sierra provides consulting services to it's customers. This assures that a smooth transition to the Sierra foundry will occur.

Presenting MIXsim

■ Sierra Semiconductor's Mixed Analog-and-Digital Simulator

Digital semicustom IC design owes much of its current popularity to the rise of reliable, easy-to-use, digital simulators, which assure designers that their silicon will work the first time. These simulators mimic circuit behavior, instead of modeling every last component, and their use transforms logic designers into de facto chip designers who have no need to master the transistor-level intricacies of IC design. As the software is relatively inexpensive and runs on low-cost workstations, the development has encouraged hundreds of companies to reap the benefits of VLSI.

Designers of mixed analog-and-digital semicustom ICs have not been so lucky. The Spice-based simulation tools they use are largely to blame. Spice simulates analog circuits at the transistor level, rather than the functional level. At LSI and VLSI densities, that approach entails endless complexity, piece-meal simulation of only part of a circuit at a time, and huge chunks of computer time. Nor was Spice designed to combine with behavioral, event-driven digital simulators, so its shortcomings in this respect are enormous.

New Methodology

Sierra Semiconductor's mixed analog-and-digital simulator pioneers a new methodology. It is the first commercially available behavioral simulator to allow complex ICs incorporating both analog and digital functions to be fully, quickly, and correctly simulated.

In MIXsim, as with digital-only simulators, each analog or digital function is represented by a model. This model could represent any analog function, such as an op amp of voltage-controlled oscillator, or any digital function—say, an inverter.

During a simulation, though, MIXsim does not deal with analog models separately from digital models. Instead, it simulates the entire mixed circuit at one and the same time. In the process, each analog model is independently informed of changes at its terminals. Thus, an analog or mixed analog-and-digital signal propagates through the simulated circuit by a sequence of model interactions. The interaction sequence is controlled in an event-driven manner, much as digital behavioral simulators operate.

This type of behavioral, event-driven approach differs markedly from Spice-like mixed analog and digital simulators. In order for Spice to simulate a circuit, a set of equations must be developed to describe the entire analog circuit, and those equations must then be solved simultaneously for each time increment. Simulation time therefore increases out of all proportion to the complexity of the circuit. Spice undoubtably excels at the cell level, where transistors number less than, say, 100, but it is inordinately time-consuming and soon becomes ineffective for systems of cells or for a whole chip.

Major Benefits

The MIXsim approach to circuit simulation has substantial benefits, especially for designs that are based on standard cells. In these cell-based designs, the transistor-level details have already been worked out, and the behavior of the overall system is all the designer need worry about. After all, an engineer looking for true system integration requires a simulator that can analyze the entire circuit and the performance of each function within the circuit—there is no need to know the performance of each transistor.

MIXsim's most notable benefit is that it verifies a complete chip. Accordingly, it is concerned with timing, connectivity, the proper application of cells, and assurance that cell specifications are not being violated. Circuit designers using it can quickly examine the performance of the circuit as a whole to flag any problem in these four areas.

MIXsim's success in simulating an entire analog and digital circuit stems from the accuracy with which it can monitor the interactions between the analog and digital sections. Current Spice-based mixed mode methodology, on the other hand, commonly employs separate analog and digital simulations and does not even attempt to simulate the entire circuit at once. Instead, it first simulates the analog portion, or parts of the analog portion, of the circuit, and then connects to a digital simulation for the digital portion. Finally, it tries to combine the two simulation results. This last step lets entire classes of design errors go undetected at the analog-to-digital interface.

A second benefit of MIXsim is that intelligence is built into the analog models. When an analog function exceeds the desired specifications, error messages are displayed that state explicitly what type of error has been made. Since the simulator uses cell-level behavioral models, the errors flagged generally concern the application of the function within the circuit; they never refer to the resistors, transistors, and other components that perform the function. This feature is impossible with Spice, which has no way of knowing what the circuit is supposed to do and so can neither report nor detect errors.

MIXsim accommodates both the standard digital functions and a wide variety of analog and mixed analog-and-digital functions. These include the likes of op amps, analog switches, multiplexers, comparators, oscillators, power-on reset circuits, current sources, and of course A/D and D/A converters. The simulator can also handle other analog circuit elements, like resistors and capacitors. Should a special function be required, the simulation algorithm permits the user to create it. It is also possible to encapsulate several analog functions in a higher-level model in order to simplify the simulations.

In sum, MIXsim's combination of highly characterized and predictable analog standard cells and behavioral simulation techniques gives the user the power to simulate mixed analog-and-digital circuits with the same relative case with which all-digital circuits are simulated. Working silicon can and has been obtained the first time by designers using this simulation software.

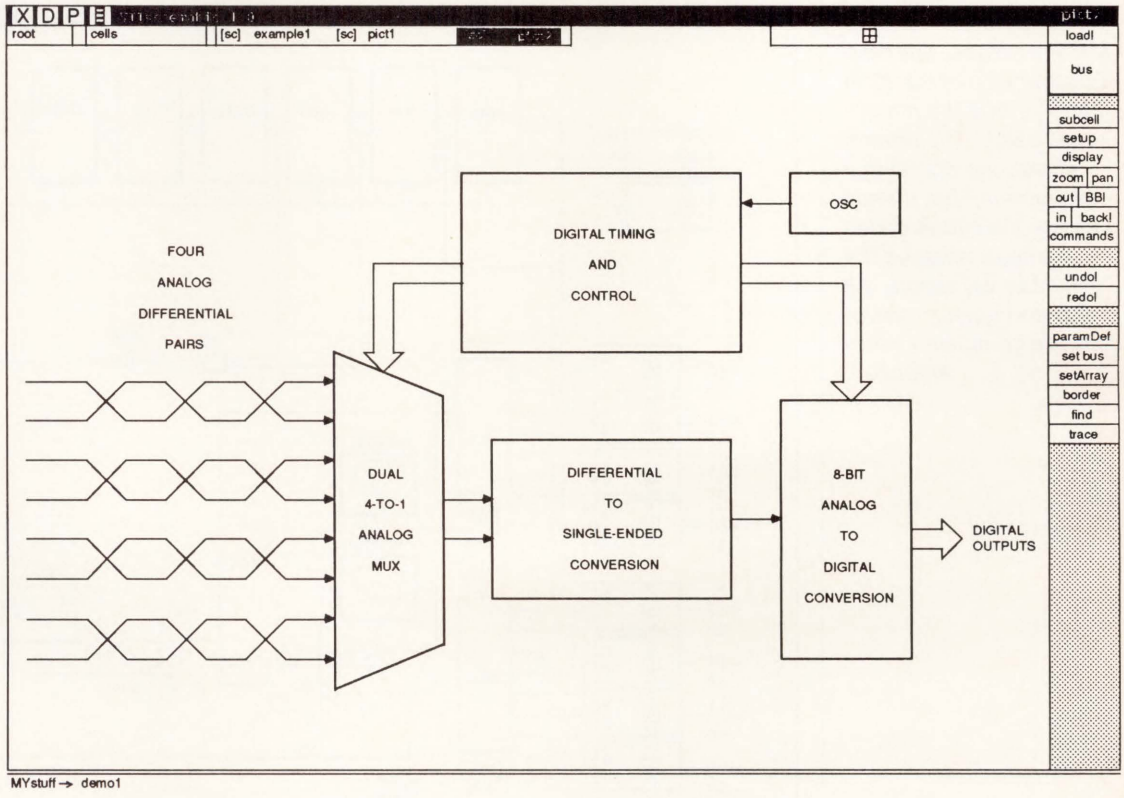


Figure 1. *MIXsim's simulation abilities apply to an IC incorporating mixed analog-and-digital circuitry. The circuit shown here digitizes differential analog inputs entering from four twisted pairs.*

To fully appreciate the difference between a Spice-based analog simulator, consider the circuit shown in Fig. 1. The design employs cells from Sierra's 2-µm standard- cell library.

In this example, the analog signal path consists of four analog differential-input signals. These pass through an analog multiplexer and are first converted into single-ended signals and then digitized by an 8-bit A/D converter. The digital portion of the circuit involves timing and control logic that selects the differential analog signals and starts the A/D conversion.

The actual schematic and macrocells are shown in Fig. 2. These macrocells are the lowest-level function that the software of the circuit designer has to work with when using MIXsim. As with any digital design, the analog functions are completely characterized and called up from the standard-cell library. (All MIXsim models are exhaustively characterized to take into account variations in process parameters, power supply voltage, and ambient temperature.)

Notice that meters are placed on the outputs of MX_{1OUT}, MX_{2OUT}, and GB_{2OUT} to monitor analog activity. The control file is like the control file used in digital simulation (see Fig. 3).

With regard to the file called Set Up Clocks, X_1 and X_2 refer to the two inputs to the oscillator. These two inputs are out of phase, so initially 0 (2,000) refers to X_1 being held at logic 0 for 2,000 ns. After the 2,000 ns has elapsed, both inputs are toggled every 200 ns, and are 180° out of phase. Note that a complete clock cycle is 400 ns long and thus corresponds to a clock frequency of 2.5 MHz. The A/D conversion time is 16 clock periods, or 6,400 ns.

The simulation is first run for 32 clock cycles. The output indicates the voltages at both the analog and digital circuit nodes (see Fig. 4), and three errors have been flagged.

The first and second errors appear 0.3 ns into the logic simulation and were uncovered by

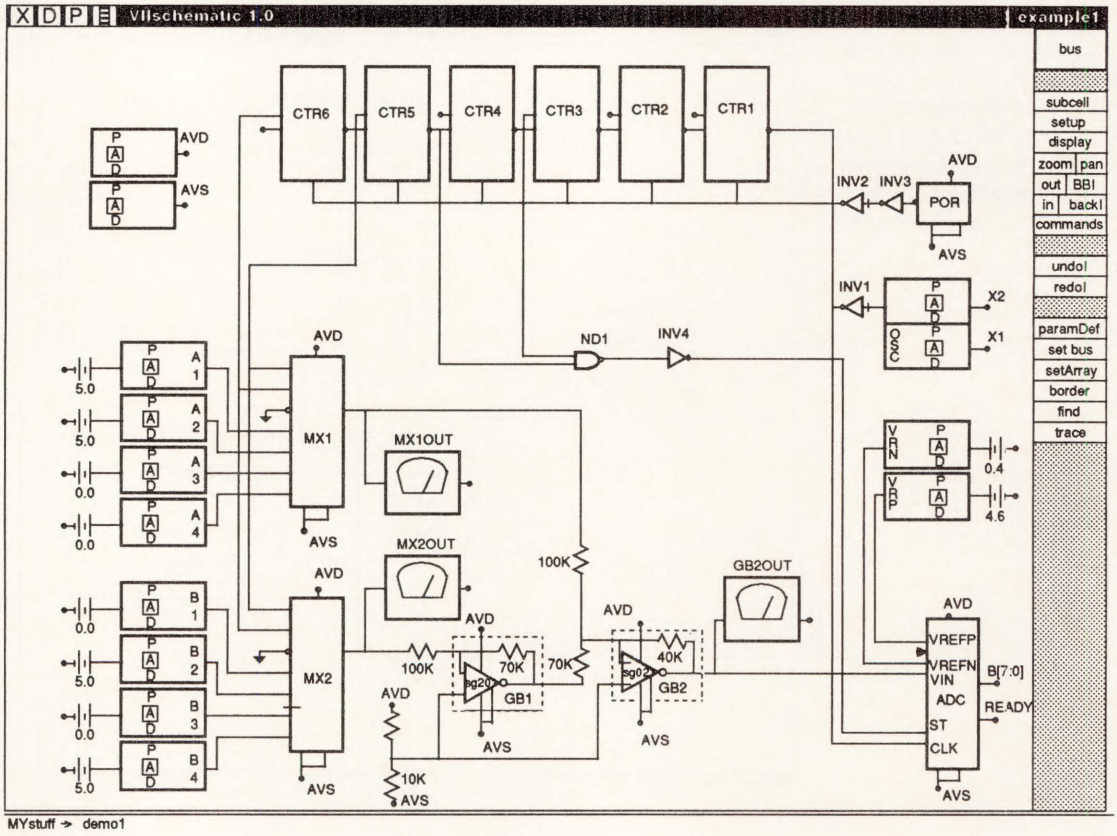


Figure 2. *From the MIXsim screen, this first-cut schematic of the IC in Fig. 1 shows the macrocells used. The meters shown are not "virtual voltometers," but merely indicate the circuit nodes whose voltages the simulator will report. All digital and analog macrocells are completely characterized.*

```
          ***********************************
          ***** SIMULATION CONTROL FILE *****
          ***********************************

      LOAD THE SCHEMATIC
      ******************
load [sc]example1
load opts

      SET UP CLOCKS
      *************
set clock (primary, report) x1 0(2000) ; 1(200) 0(200)
set clock                   x2 1(2000) ; 0(200) 1(200)

      DECLARE EXTERNAL NODES
      **********************
set ext out ctr1.q ctr2.q ctr3.q ctr4.q ctr6.qn mx1out.v mx2out.v
set ext out gb2out.v ready b[7] b[6] b[5] b[4] b[3] b[2] b[1] b[0]

      SET DISPLAY FORMAT
      ******************
set  trace mode tabular 10 200 1 ff
load timestuff

      LIST NODES TO BE "WATCHED"
      **************************
watch           ctr6.q ctr5.q
watch           mx1out.v mx2out.v
watch (display) adc.st ready
watch           gb2out.v
watch           b[7] b[6] b[5] b[4] b[3] b[2] b[1] b[0]

      RUN 32 CLOCKS
      *************
```

Figure 3. *This MIXsim control file sets up and runs a simulation. It closely resembles the control file of a purely digital simulator.*

initial connectivity and usage checks. The first error appears on gain block 2 (GB_2). It shows that the capacitive load of the gain block exceeds 30 pF, the maximum that the amplifier can drive. A check of the Sierra Semiconductor Triple Technology Standard Cell Data Book confirms that, while the input capacitance of the A/D converter is 60 pF, the Sg20id op amp cell can indeed drive only 30 pF. The problem can be quickly solved by substituting another op amp, one with greater drive capability, from the standard cell library.

The second error is the omitted connection to the positive terminal of GB_1. The fix here is simply to connect the terminal to the circuit node to which the other op amp's positive terminal is connected.

The third and last error uncovered by the simulation is the fact that GB_1's common-mode range has been exceeded. But the positive input to GB_1 is not connected, so this error may be ignored for now.

Also, notice that the MIXsim simulator takes into account resistive drops along the analog path. Each pad has 70 Ω of resistance. In addition, the analog multiplexer has about 1 kΩ of series resistance. This comes to approximately a 25-mV voltage differential between the input pad and the multiplexer output. Examination of MUX_{1OUT} and MUX_{2OUT} shows these voltage drops have been accounted for.

Once these errors have been corrected, MIXsim is rerun, again for 32 clock cycles. This next simulation reveals two errors that were previously masked (see Fig. 5). (Note that the common-mode error that appeared in the first simulation has now vanished.) The simulator explicitly flags the output of GB_2 as being clipped and the input of the A/D converter, V_{IN}, as varying by more than 1 *least significant bit* (LSB) during sampling.

Closer examination of the differential-input pairs shows that they are selected in the following order: A_1 and B_1, A_2 and B_2, A_3 and B_3, and A_4 and B_4. Thus, the inputs of the differential to single-ended signal converter are sequencing through the following voltages: 0 and 0 V, to 0 and 5V, to 5 and 0 V, to 5 and 5 V. When the differential input swings from 0 and 5V to 5 and 0 V, there are very large voltage swings in the op amps. It is at this point that the simulator shows that the input voltage to the A/D converter (V_{IN}) has not settled and is varying by 1 LSB or more during the conversion cycle.

Final Corrections

A simple change to the logic circuitry is enough to correct the settling problem at the input of the converter. The alteration adds about four clock cycles to the time between the change in the multiplexer control inputs and the start of the conversion. The longer interval gives GB_2 more time to settle.

Figure 4. The reults of the first simulation of the circuit in Fig. 2 indicate the presence of three errors. Note the inclusion of analog voltages.

```
      t              C C M          M          A R G          B B B B B B B B
      i              T T X          X          D E B          [ [ [ [ [ [ [ [
      m              R R 1          2          C A 2          7 6 5 4 3 2 1 0
      e              6 5 O          O          . D O          ] ] ] ] ] ] ] ]
      .              . . U          U          s Y U          : : : : : : : :
      n              Q Q T          T          t : T          : : : : : : : :
      s              : : .          .          : : .          : : : : : : : :
      :              : : v          v          : : v          : : : : : : : :
GB2:     [.3ns]
   WARNING:  Capacitive load at "vout" exceeds maximum of 30 pf.
GB1:     [.3ns]
   No analog source is connected to "pos"
  1:1  ...2000.0ns  0 0  +0.0264.v   +0.0187.v  0 u  UNCERTAIN  u u u u u u u u
  5:2  ...3600.0ns  0 0  +0.0264.v   +0.0187.v  1 0  UNCERTAIN  u u u u u u u u
  7:1  ...4200.0ns  0 0  +0.0264.v   +0.0187.v  1 0  +3.30...v  u u u u u u u u
  9:2  ...5200.0ns  0 0  +0.0264.v   +0.0187.v  0 0  +3.30...v  u u u u u u u u
GB1:     [8315.6ns]
   WARNING:  Common mode input voltage exceeds maximum of 3 volts.
 17:2  ...8400.0ns  0 1  +0.0241.v   +4.98...v  0 0  UNCERTAIN  u u u u u u u u
 18:1  ...8600.0ns  0 1  +0.0264.v   +4.98...v  0 0  UNCERTAIN  u u u u u u u u
 20:1  ...9400.0ns  0 1  +0.0264.v   +4.98...v  0 0  UNCERTAIN  1 0 1 1 0 0 1 1
 20:2  ...9600.0ns  0 1  +0.0264.v   +4.98...v  0 1  UNCERTAIN  1 0 1 1 0 0 1 1
 21:2  ..10000.0ns  0 1  +0.0264.v   +4.98...v  1 0  UNCERTAIN  1 0 1 1 0 0 1 1
 23:1  ..10600.0ns  0 1  +0.0264.v   +4.98...v  1 0  +3.61...v  1 0 1 1 0 0 1 1
 25:2  ..11600.0ns  0 1  +0.0264.v   +4.98...v  0 0  +3.61...v  1 0 1 1 0 0 1 1
```

Figure 5. Minor circuit redesigns to clear up the errors noted in Fig. 4 give these simulation results. An op amp clipping problem has now been uncovered. Also, the input voltage of the A/D converter is varying by more than 1 LSB during sampling.

```
      t              C C M          M          A R G          B B B B B B B B
      i              T T X          X          D E B          [ [ [ [ [ [ [ [
      m              R R 1          2          C A 2          7 6 5 4 3 2 1 0
      e              6 5 O          O          . D O          ] ] ] ] ] ] ] ]
      .              . . U          U          s Y U          : : : : : : : :
      n              Q Q T          T          t : T          : : : : : : : :
      s              : : .          .          : : .          : : : : : : : :
      :              : : v          v          : : v          : : : : : : : :
  1:1  ...2000.0ns  0 0  +0.0265.v   +0.0265.v  0 u  UNCERTAIN  u u u u u u u u
  2:2  ...2400.0ns  0 0  +0.0265.v   +0.0265.v  0 u  +2.50...v  u u u u u u u u
  5:2  ...3600.0ns  0 0  +0.0265.v   +0.0265.v  1 0  +2.50...v  u u u u u u u u
  9:2  ...5200.0ns  0 0  +0.0265.v   +0.0265.v  0 0  +2.50...v  u u u u u u u u
 17:2  ...8400.0ns  0 1  +0.0244.v   +4.99...v  0 0  UNCERTAIN  u u u u u u u u
 18:1  ...8600.0ns  0 1  +0.0255.v   +4.99...v  0 0  UNCERTAIN  u u u u u u u u
 18:2  ...8800.0ns  0 1  +0.0250.v   +4.98...v  0 0  UNCERTAIN  u u u u u u u u
 19:1  ...9000.0ns  0 1  +0.0255.v   +4.98...v  0 0  UNCERTAIN  u u u u u u u u
 19:2  ...9200.0ns  0 1  +0.0256.v   +4.98...v  0 0  UNCERTAIN  u u u u u u u u
 20:1  ...9400.0ns  0 1  +0.0264.v   +4.98...v  0 0  UNCERTAIN  1 0 0 0 0 0 0 0
 20:2  ...9600.0ns  0 1  +0.0264.v   +4.98...v  0 1  UNCERTAIN  1 0 0 0 0 0 0 0
GB2:     [9645.1ns]
   WARNING:  "vout" clipping at 4.6 volts.
 21:1  ...9800.0ns  0 1  +0.0258.v   +4.97...v  0 1  UNCERTAIN  1 0 0 0 0 0 0 0
 21:2  ..10000.0ns  0 1  +0.0258.v   +4.97...v  1 0  +4.60...v  1 0 0 0 0 0 0 0
 22:1  ..10200.0ns  0 1  +0.0259.v   +4.97...v  1 0  +4.61...v  1 0 0 0 0 0 0 0
ADC:     [10407.4ns]
   WARNING:  "vin" exceeds "vrefp" during sampling of "vin".
 23:1  ..10600.0ns  0 1  +0.0258.v   +4.97...v  1 0  +4.60...v  1 0 0 0 0 0 0 0
 24:1  ..11000.0ns  0 1  +0.0259.v   +4.97...v  1 0  +4.61...v  1 0 0 0 0 0 0 0
 25:2  ..11600.0ns  0 1  +0.0259.v   +4.97...v  0 0  +4.61...v  1 0 0 0 0 0 0 0
GB2:     [14672.7ns]
   "vout" no longer clipped at 4.6 volts.
 33:2  ..14800.0ns  1 0  +4.98...v   +0.00773v  0 0  UNCERTAIN  1 0 0 0 0 0 0 0
 34:1  ..15000.0ns  1 0  +4.98...v   +0.0117.v  0 0  UNCERTAIN  1 0 0 0 0 0 0 0
 34:2  ..15200.0ns  1 0  +4.98...v   +0.0149.v  0 0  UNCERTAIN  1 0 0 0 0 0 0 0
 35:1  ..15400.0ns  1 0  +4.98...v   +0.0196.v  0 0  UNCERTAIN  1 0 0 0 0 0 0 0
 35:2  ..15600.0ns  1 0  +4.98...v   +0.0228.v  0 0  UNCERTAIN  1 0 0 0 0 0 0 0
 36:1  ..15800.0ns  1 0  +4.98...v   +0.0234.v  0 0  UNCERTAIN  1 1 1 1 1 1 1 1
 36:2  ..16000.0ns  1 0  +4.98...v   +0.0250.v  0 1  UNCERTAIN  1 1 1 1 1 1 1 1
GB2:     [16072.6ns]
   WARNING:  "vout" clipping at .4 volts.
 37:1  ..16200.0ns  1 0  +4.98...v   +0.0265.v  0 1  UNCERTAIN  1 1 1 1 1 1 1 1
 37:2  ..16400.0ns  1 0  +4.98...v   +0.0265.v  1 0  UNCERTAIN  1 1 1 1 1 1 1 1
 38:2  ..16800.0ns  1 0  +4.97...v   +0.0265.v  1 0  UNCERTAIN  1 1 1 1 1 1 1 1
   WARNING:  "vin" varies by one LSB or more during sampling.
 40:1  ..17400.0ns  1 0  +4.97...v   +0.0265.v  1 0  +0.410..v  1 1 1 1 1 1 1 1
 41:2  ..18000.0ns  1 0  +4.97...v   +0.0265.v  0 0  +0.410..v  1 1 1 1 1 1 1 1
GB2:     [21067.8ns]
   "vout" no longer clipped at .4 volts.
 49:2  ..21200.0ns  1 1  +4.97...v   +4.99...v  0 0  UNCERTAIN  1 1 1 1 1 1 1 1
 50:2  ..21600.0ns  1 1  +4.97...v   +4.98...v  0 0  UNCERTAIN  1 1 1 1 1 1 1 1
```

To correct the clipping of GB_2's output, the gain should be reduced —an easy job. The value of the gain block's feedback resistor is simply lowered from 45 to 40 kΩ.

All the changes that have been made to the original circuit are highlighted in Fig. 6.

At this point a third simulation is run, but this time for 80 clock cycles to give the op amp more time to settle, and so on. The results show that the circuit now runs entirely without errors, indicating that the previous connectivity, dynamic range, and timing problems have been solved. Also, as indicated on Fig. 6, control registers 5 and 6 (CTR_5 and CTR_6) have cycled the input multiplexers through all four channels.

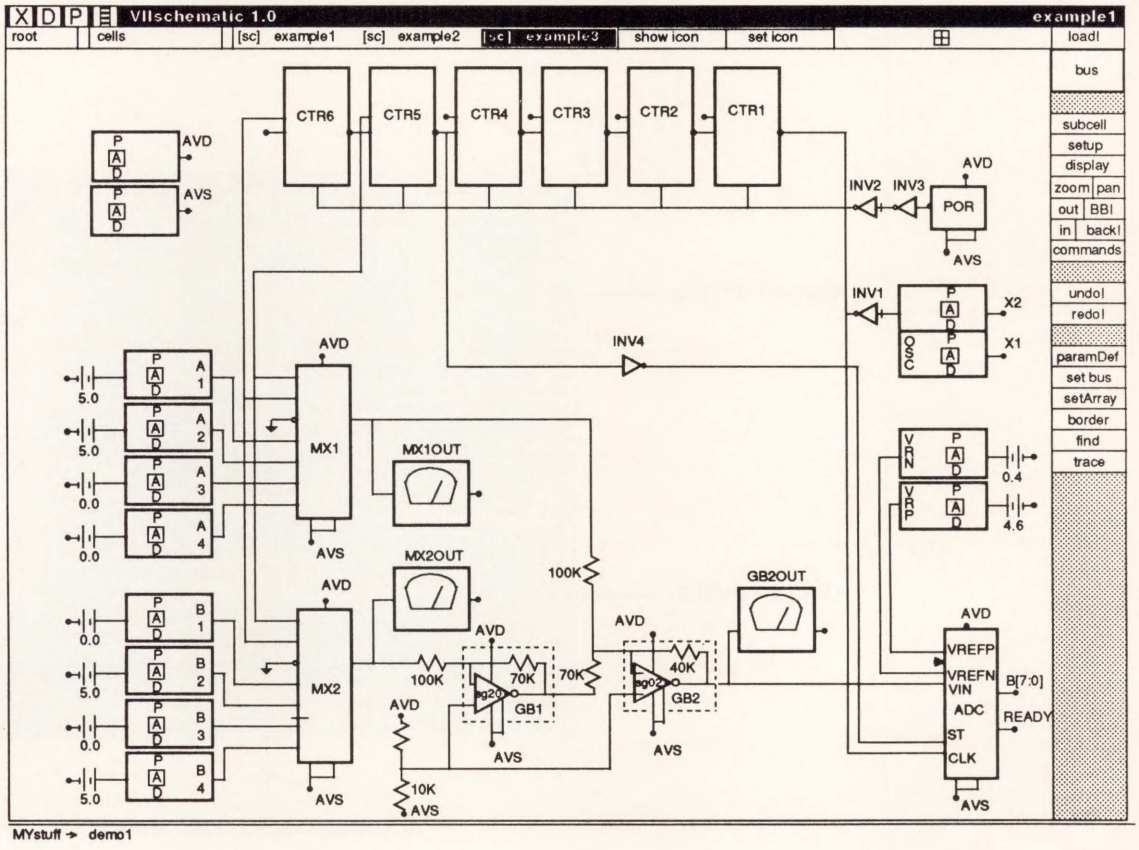
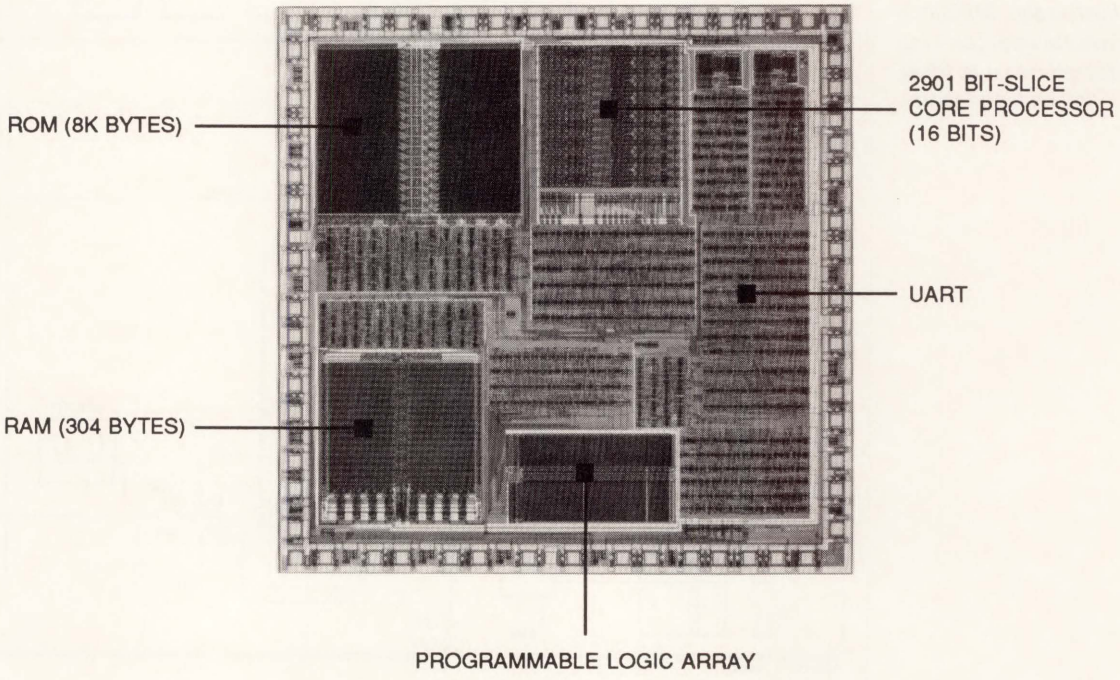


Figure 6. *After implementing all the changes highlighted, the circuit was again simulated—this time flawlessly. MIXsim's behavioral approach cut this design down to three quick simulations.*

Applications

■ Modem Advanced Coprocessor (MAC)
Sierra
Standard Product

This ASIC, designed using Sierra's 2-micron Standard Cell Library, is a specialized controller used to build a 2400 bps full duplex intelligent modem. The MAC uses a 2901 bit slice core processor to perform the digital signal processing (DSP) and the control functions. Its instruction set is a subset of Intel 8096 instruction set but operates faster than 8096. MAC is designed to interface to a parallel system bus and an RS232 port as well.



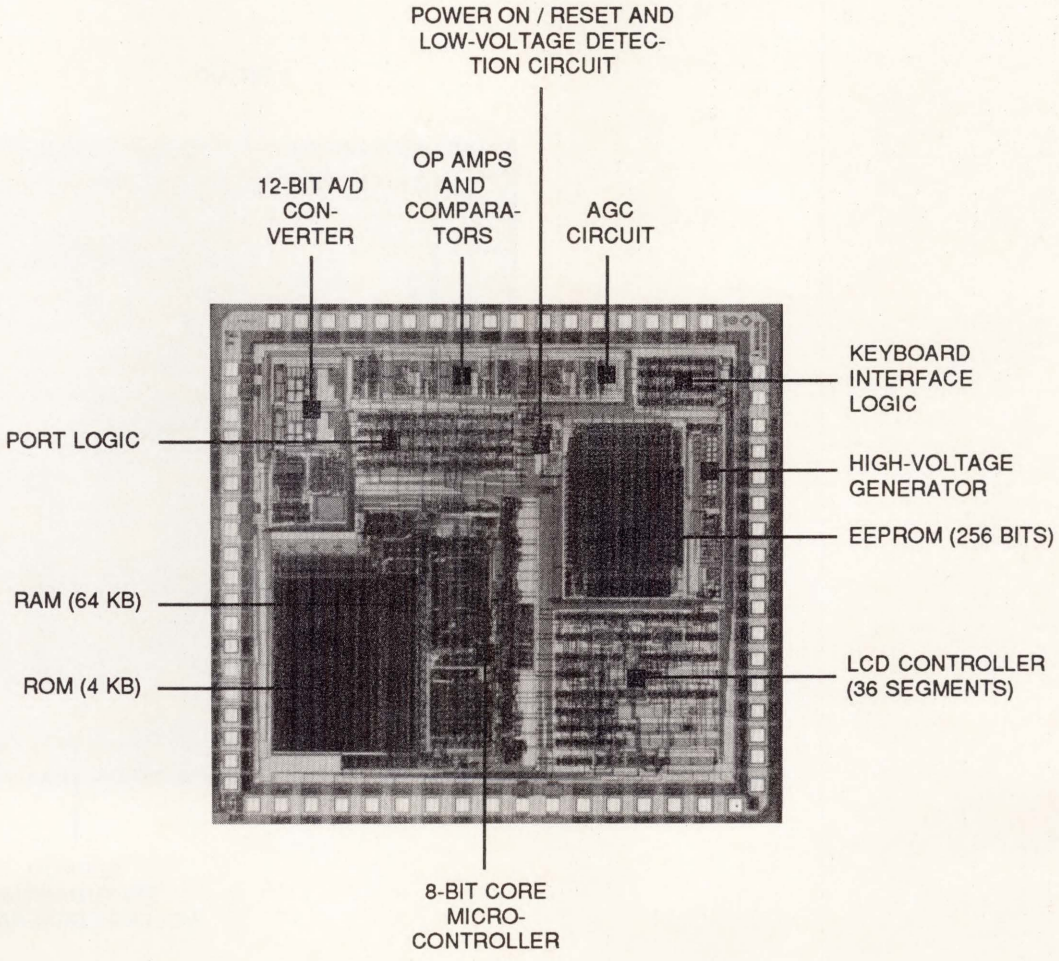
SIERRA SEMICONDUCTOR

Applications

■ Single Chip Medical Measurement and Control System

Courtesy, MIT Development Corporation

This hand-held medical instrument design utilizes an 8-bit core microcontroller standard cell along with a variety of digital, analog and EEPROM functions from Sierra's 2-micron CMOS Standard Cell Library. The 12-bit A/D converter reads the characteristics of an inserted sample and the information is transferred to the core microcontroller to compute an analysis of the sample, and display the results on an LCD. The EEPROM stores calibration values and the results of the users' test.



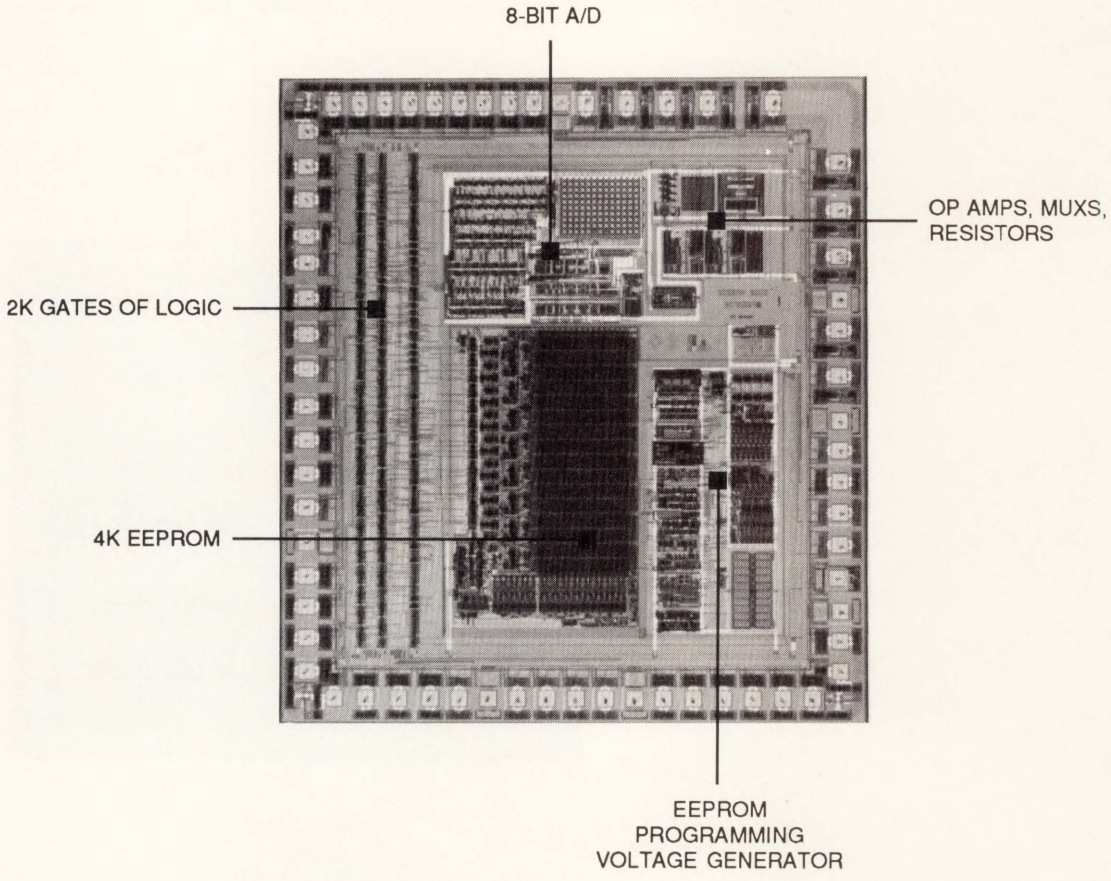
Applications

■ Distributed Environmental Controller

Courtesy, ASI Controls Corporation

This Triple Technology ASIC is used in a distributed environmental controller that can control the cooling and heating of areas in an office complex or school. The EEPROM can be programmed for each controller to provide the correct air volume flow for each combination of room size, number of vents, etc. In addition, the EEPROM is used to trim the analog circuits used to read temperature, servo motor position, etc.

The random logic was designed by Sierra's customer and integrated with the Analog and EEPROM megacells at Sierra's Design Center in San Jose.



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Signetics

PLUS405
Field-Programmable Logic Sequencer (16 × 64 × 8)

Signetics Programmable Logic
Product Specification

Application Specific Products
- **Series 28**

DESCRIPTION

The PLUS405 is a bipolar, programmable state machine of the Mealy type. Both the AND and the OR array are user-programmable. All 64 AND gates are connected to the 16 external dedicated inputs ($I_0 - I_{15}$) and to the feedback paths of the 8 on-chip State Registers ($Q_{P0} - Q_{P7}$). Complement transition terms can be generated via optional use of the two internal Complement Arrays (input variables C_0, C_1).

All state transition terms can include True, False and Don't Care states of the controlling state variables. All AND gates are merged into the programmable OR array to issue the next-state and next-output commands to their respective registers. Because the OR array is programmable, any one or all of the 64 transition terms can be connected to any or all of the State and Output Registers.

All state ($Q_{P0} - Q_{P7}$) and output ($Q_{F0} - Q_{F7}$) registers are edge-triggered, clocked J-K flip-flops, with Asynchronous Preset and Reset options. The PLUS405 architecture provides the added flexibility of the J-K toggle function which is indeterminate on S-R flip-flops. Each register may be individually programmed such that a specific Preset-Reset pattern is initialized when the initialization pin is raised to a logic level "1". This feature allows the state machine to be asynchronously initialized to known internal state and output conditions prior to proceeding through a sequence of state transitions. Upon power-up, all registers are unconditionally preset to "1". If desired, the initialization input pin (INIT) can be converted to an Output Enable ($\overline{OE}$) function as an additional user-programmable feature.

Availability of two user-programmable clocks allows the user to design two independently clocked state machine functions consisting of four state and four output bits each.

Order codes are listed in the Ordering Information Table.

FEATURES

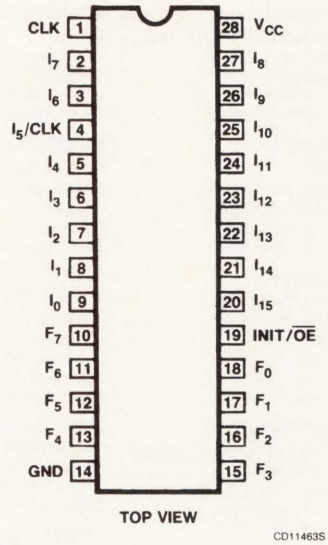
- **Functional superset of PLS105/105A**
- **50MHz clock rate**
- **f_{MAX} = 33MHz ($1/(t_{IS} + t_{CKO}) = f_{MAX}$)**
- **Field-programmable (Ti-W fusible link)**
- **16 input variables**
- **8 output functions**
- **64 transition terms**
- **8-bit State Register**
- **8-bit Output Register**
- **2 transition Complement Array terms**
- **Multiple clocks**
- **Programmable Asynchronous Initialization or Output Enable**
- **Power-on preset of all registers to "1"**
- **950mW power dissipation (typ.)**
- **TTL compatible**
- **J-K or S-R flip-flop functions**
- **3-State outputs**

APPLICATIONS

- **Interface protocols**
- **Sequence detectors**
- **Peripheral controllers**
- **Timing generators**
- **Sequential circuits**
- **Elevator controllers**
- **Security locking systems**
- **Counters**
- **Shift registers**

PIN CONFIGURATIONS

N Package

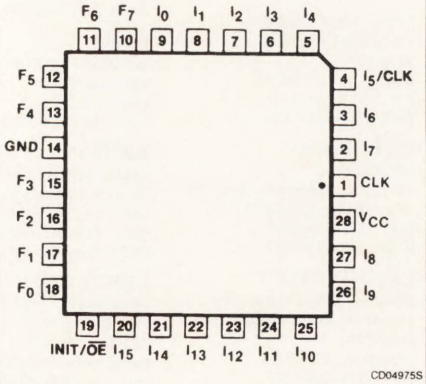


TOP VIEW

CD11463S

NOTE:
N = Plastic

A Package



CD04975S

NOTE:
A = Plastic Leaded Chip Carrier

Signetics

PLUS173D
Field-Programmable Logic Array (22 × 42 × 10)

Signetics Programmable Logic
Product Specification

Application Specific Products
- **Series 24**

DESCRIPTION

The PLUS173D is a 12ns version of the PLS173 FPLA architecture. The Signetics state-of-the-art Oxide Isolated Bipolar fabrication process is employed to produce performance levels not yet achieved in devices of this complexity.

The PLUS173D is a two-level logic element consisting of 42 AND gates and 10 OR gates with fusible link connections for programming I/O polarity and direction.

All AND gates are linked to 12 inputs (I) and 10 bidirectional I/O lines (B). These yield variable I/O gate configurations via 10 direction control gates (D), ranging from 22 inputs to 10 outputs.

On chip T/C buffers couple either True (I, B) or Complement ($\overline{I}$, $\overline{B}$) input polarities to all AND gates, whose outputs can be optionally linked to all OR gates. Their output polarity, in turn, is individually programmable through a set of Ex-OR gates for implementing AND/OR or AND/NOR logic functions.

The PLUS173D is field-programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

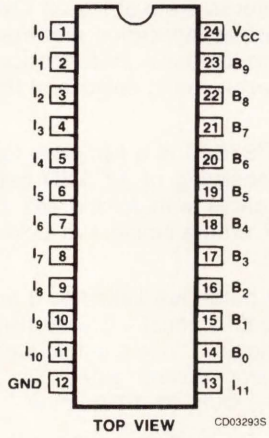
Order codes are listed in the Ordering Information Table.

FEATURES

- **Field-Programmable (Ti-W links)**
- **Functionally identical to, and pin-for-pin compatible with, the PLS173 and the PLUS173B**
- **12 inputs**
- **42 AND gates**
- **10 OR gates**
- **10 bidirectional I/O lines**
- **Programmable output polarity**
  - **active-High or -Low outputs**
- **42 product terms:**
  - **32 logic terms**
  - **10 control terms**
- **I/O propagation delay: 12ns (max.)**
- **Input loading: −100μA (max.)**
- **Power dissipation: 750mW (typ.)**
- **3-State outputs**
- **TTL compatible**
- **Security fuse**

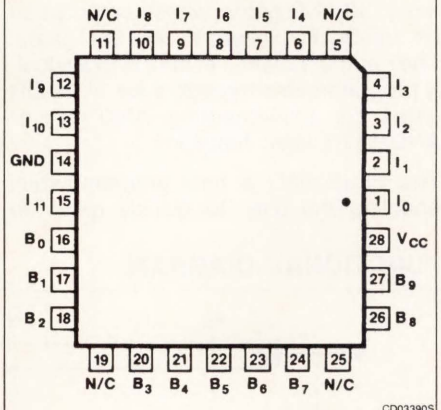
PIN CONFIGURATIONS

N Package



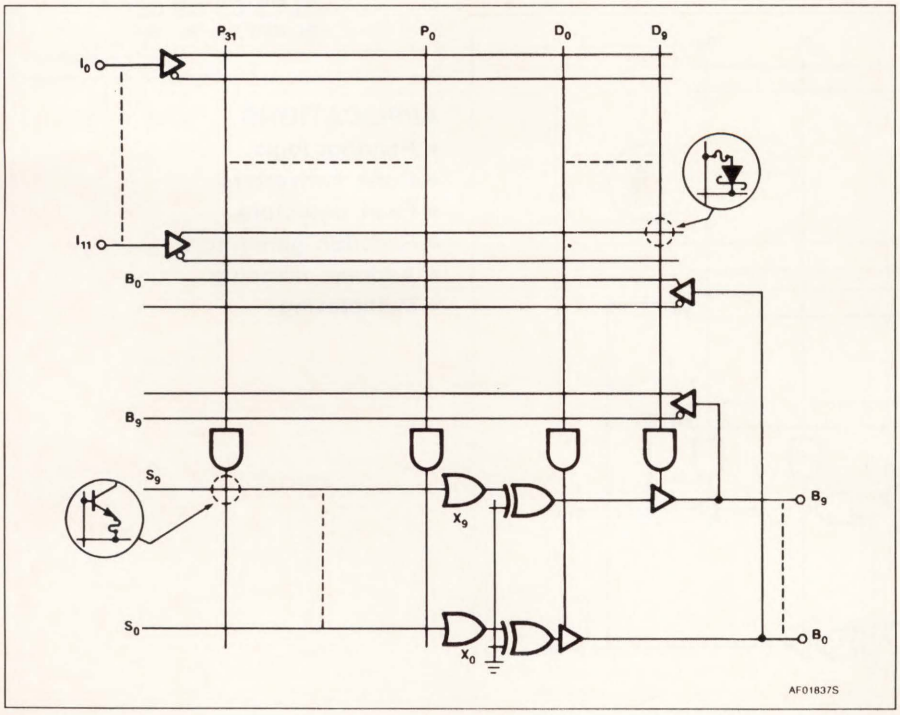
TOP VIEW CD03293S

A Package



CD03390S

FUNCTIONAL DIAGRAM



APPLICATIONS

- **Random logic**
- **Code converters**
- **Fault detectors**
- **Function generators**
- **Address mapping**
- **Multiplexing**

Signetics

PLUS153D
Field-Programmable Logic Array (18 × 42 × 10)

Signetics Programmable Logic
Product Specification

Application Specific Products
- **Series 20**

DESCRIPTION

The PLUS153D is a 12ns version of the Signetics PLS153 FPLA architecture. The Signetics state-of-the-art Oxide Isolated Bipolar fabrication process is employed to produce performance levels not yet achieved in devices of this complexity.

The PLUS153D is a two-level logic element, consisting of 42 AND gates and 10 OR gates with fusible link connections for programming I/O polarity and direction.

All AND gates are linked to 8 inputs (I) and 10 bidirectional I/O lines (B). These yield variable I/O gate configurations via 10 direction control gates (D), ranging from 18 inputs to 10 outputs.

On-chip T/C buffers couple either True (I, B) or Complement ($\bar{I}$, $\bar{B}$) input polarities to all AND gates, whose outputs can be optionally linked to all OR gates. Their output polarity, in turn, is individually programmable through a set of Ex-OR gates for implementing AND/OR or AND/NOR logic functions.

The PLUS153D is field programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

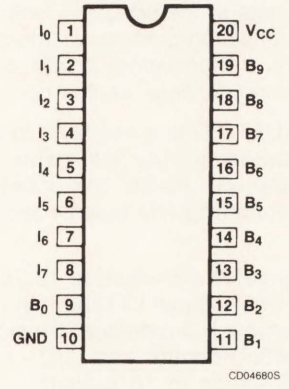
Order codes are listed in the Ordering Information Table.

FEATURES

- **Field-Programmable (Ti-W links)**
- **Functionally identical to, and pin-for-pin compatible with, the PLS153/153A, PLHS153 and PLUS153B**
- **8 inputs**
- **42 AND gates**
- **10 OR gates**
- **10 bidirectional I/O lines**
- **Programmable output polarity**
  - **active-High or -Low outputs**
- **42 product terms:**
  - **32 logic terms**
  - **10 control terms**
- **I/O propagation delay: 12ns (max.)**
- **Input loading: −100μA (max.)**
- **Power dissipation: 750mW (typ.)**
- **3-State outputs**
- **TTL compatible**
- **Security fuse**

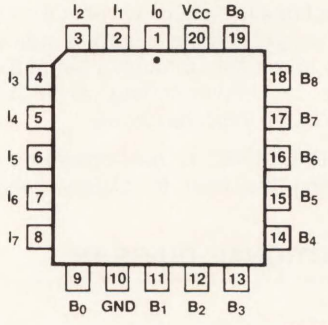
PIN CONFIGURATIONS

N Package

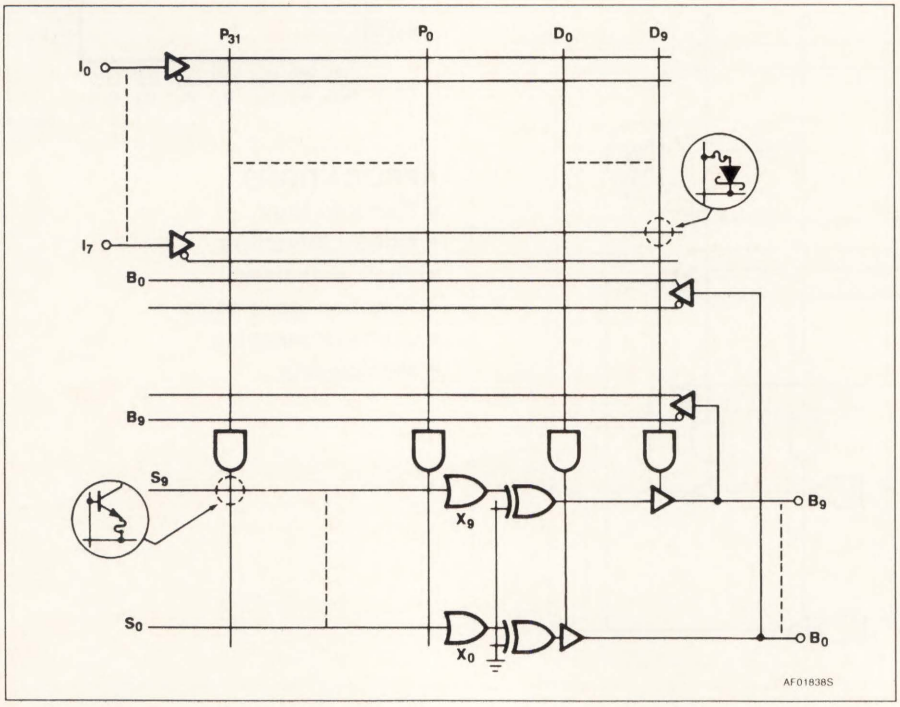


TOP VIEW

A Package



FUNCTIONAL DIAGRAM



APPLICATIONS

- **Random logic**
- **Code converters**
- **Fault detectors**
- **Function generators**
- **Address mapping**
- **Multiplexing**

Signetics

PLUS20R8D
PAL®-Type Devices Series

Signetics Programmable Logic
Preliminary Specification

Application Specific Products
- **Series 24**

FEATURES
- **Ultra high-speed:**
  - **t_{PD} = 10ns**
  - **f_{MAX} = 55.5MHz (with feedback)**
  - **t_{IS} = 10ns (worst case)**
  - **t_{CKO} = 8ns (worst case)**
- **100% functionally and pin-for-pin compatible with industry standard 24-pin PAL ICs**
- **Power-up reset function to enhance state machine design and testability**
- **Design support provided via AMAZE and other CAD tools for Series 24 PAL devices**
- **Field-programmable on industry standard programmers**
- **Security fuse**
- **Individual 3-State control of all outputs**

DESCRIPTION
The Signetics PLUS20XXD family is an ultra high-speed 10ns version of existing Series 24 PAL devices.

The PLUS20XXD family is 100% functional and pin-compatible with the 20L8, 20R8, 20R6, and 20R4 Series devices.

The sum of products (AND-OR) architecture is comprised of 64 AND gates and 8 OR gates. Multiple bidirectional pins provide variable input/output pin ratios. Individual 3-State control of all outputs and registers with feedback (R8, R6, R4) is also provided.

The PLUS20R8D, R6D, and R4D have D-type flip-flops which are loaded on the Low-to-High transition of the clock input.

In order to facilitate state machine design and testing, a power-up reset function has been incorporated into these devices to reset all internal registers to active-Low after a specific period of time.

The Signetics State-of-the-Art oxide isolation Bipolar fabrication process is employed to achieve high-performance operation.

The PLUS20XXD family of devices are field programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

DEVICE NUMBER	DEDICATED INPUTS	COMBINATORIAL OUTPUTS	REGISTERED OUTPUTS	t_{PD}	I_{CC}	f_{MAX} WITHOUT FEEDBACK	f_{MAX} WITH FEEDBACK
PLUS20L8D	14	8(6 I/O)	0	10ns	210mA		
PLUS20R8D	12	0	8		210mA	62.5MHz	55.5MHz
PLUS20R6D	12	2 I/O	6	10ns	210mA	62.5MHz	55.5MHz
PLUS20R4D	12	4 I/O	4	10ns	210mA	62.5MHz	55.5MHz

Signetics

PLUS16R8D
PAL®-Type Devices Series

Signetics Programmable Logic
Preliminary Specification

Application Specific Products
- **Series 20**

FEATURES
- **Ultra high-speed:**
  - **t_{PD} = 10ns**
  - **f_{MAX} = 55.5MHz (with feedback)**
  - **t_{IS} = 10ns (worst case)**
  - **t_{CKO} = 8ns (worst case)**
- **100% functionally and pin-for-pin compatible with industry standard 20-pin PAL ICs**
- **Power-up reset function to enhance state machine design and testability**
- **Design support provided via AMAZE and other CAD tools for Series 20 PAL devices**
- **Field-programmable on industry standard programmers**
- **Security fuse**
- **Individual 3-State control of all outputs**

DESCRIPTION
The Signetics PLUS16XXD family is an ultra high-speed 10ns version of existing Series 20 PAL devices.

The PLUS16XXD family is 100% functional and pin-compatible with the 16L8, 16R8, 16R6, and 16R4 Series devices.

The sum of products (AND/OR) architecture is comprised of 64 AND gates and 8 OR gates. Multiple bidirectional pins provide variable input/output pin ratios. Individual 3-State control of all outputs and registers with feedback (R8, R6, R4) is also provided.

The PLUS16R8D, R6D, and R4D have D-type flip-flops which are loaded on the Low-to-High transition of the clock input.

In order to facilitate state machine design and testing, a power-up reset function has been incorporated into these devices to reset all internal registers to active-Low after a specific period of time.

The Signetics State-of-the-Art oxide isolation Bipolar fabrication process is employed to achieve high-performance operation.

The PLUS16XXD family of devices are field programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

DEVICE NUMBER	DEDICATED INPUTS	COMBINATORIAL OUTPUTS	REGISTERED OUTPUTS	t_{PD}	I_{CC}	f_{MAX} WITHOUT FEEDBACK	f_{MAX} WITH FEEDBACK
PLUS16L8D	10	8(6 I/O)	0	10ns	180mA		
PLUS16R8D	8	0	8		180mA	62.5MHz	55.5MHz
PLUS16R6D	8	2 I/O	6	10ns	180mA	62.5MHz	55.5MHz
PLUS16R4D	8	4 I/O	4	10ns	180mA	62.5MHz	55.5MHz

Signetics

PLHS16L8B
Programmable AND Array Logic (16 × 64 × 8)

Signetics Programmable Logic
Product Specification

Application Specific Products
- **Series 20**

DESCRIPTION

The PLHS16L8B is a very high-speed "B" version PAL®-type device. The sum of products (AND-OR) architecture is comprised of 64 AND gates and 8 OR gates. The Signetics PLHS16L8B offers 100% functional compatibility with other PAL 16L8 devices. Specified at 155mA I_{CC} (maximum), the PLHS16L8B consumes 20% less power than other "B" version PAL 16L8 devices.

All AND gates are linked to 10 dedicated inputs, 6 bidirectional I/O and 2 dedicated outputs. On-chip buffers couple either true (I, B) or complement (I, B) input polarities to all AND gates. The 64 AND gates are separated into eight groups of eight product terms each. Within each group, seven of the AND terms are OR'ed together, while the eighth is used to control the 3-State function of the bidirectional I/O. All outputs (bidirectional and dedicated) are inverting.

In the virgin state, the AND array fuses are back-to-back CB-EB diode pairs which act as open connections. Current is avalanched across individual diode pairs during fusing, which essentially short circuits the EB diode and provides the connection for the associated product term.

The PLHS16L8B is field-programmable, allowing the user to quickly generate custom patterns using standard programming equipment.

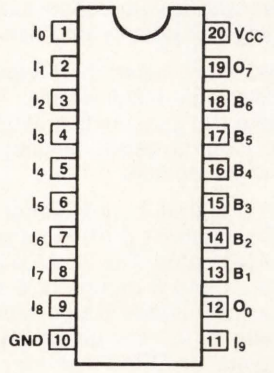
Order codes are listed in the Ordering Information Table.

FEATURES

- **Consumes 20% less power than other "B" version PAL devices**
  - **155mA I_{CC} (worst-case)**
- **I/O propagation delay: 15ns (MAX)**
- **100% functionally and pin-for-pin compatible with AmPAL16L8B, MMI PAL16L8B, TIBPAL16L8-15 and NSC PAL16L8B devices**
- **Field-programmable**
- **10 dedicated inputs**
- **8 outputs**
  - **6 bidirectional I/O**
  - **2 dedicated outputs**
- **Individual 3-State control of all outputs**
- **64 AND gates/product terms**
- **Security Fuse**

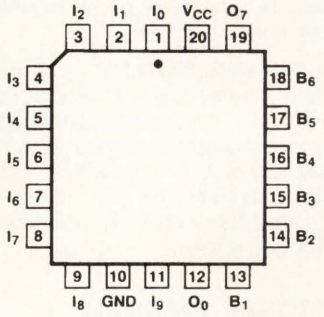
PIN CONFIGURATIONS

N Package



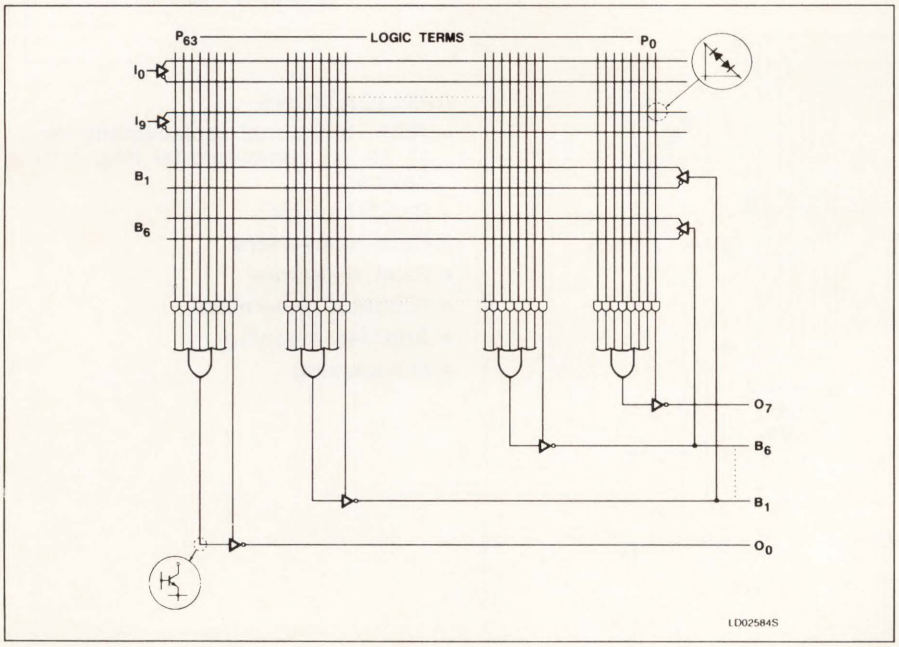
CD05323S

A Package



CD05339S

FUNCTIONAL DIAGRAM



LD02584S

APPLICATIONS

- **100% functional replacement for 20-pin 16L8 combinatorial PAL devices**
- **Random logic**
- **Code converters**
- **Fault detectors**
- **Function generators**
- **Address mapping/decoding**
- **Multiplexing**

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Signetics

PLHS18P8B
Programmable AND Array Logic (18 × 72 × 8)

Signetics Programmable Logic
Product Specification

Application Specific Products
- **Series 20**

DESCRIPTION

The PLHS18P8B is a two-level logic element consisting of 72 AND gates and 8 OR gates with fusible connections for programming I/O polarity and direction.

All AND gates are linked to 10 inputs (I) and 8 bidirectional I/O lines (B). These yield variable I/O gate configurations via 8 direction control gates, ranging from 18 inputs to 8 outputs.

On-chip T/C buffers couple either True (I, B) or Complement ($\bar{I}$, $\bar{B}$) input polarities to all AND gates. The 72 AND gates are separated into 8 groups of 9 each. Each group of 9 is associated with one bidirectional pin. In each group, eight of the AND terms are ORed together, while the ninth is used to establish I/O direction. All outputs are individually programmable via an Ex-OR gate to allow implementation of AND/OR or NAND/NOR logic functions.

In the virgin state, the AND array fuses are back-to-back CB-EB diode pairs which will act as open connections. Current is avalanched across individual diode pairs during fusing, which essentially short circuits the EB diode and provides the connection for the associated product term.

The PLHS18P8B is field-programmable, allowing the user to quickly generate custom pattern using standard programming equipment.

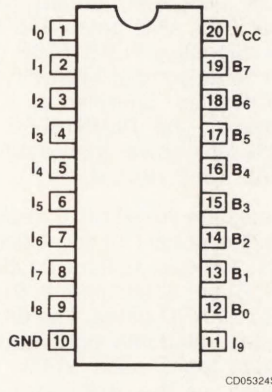
Order codes are listed in the Ordering Information Table.

FEATURES

- **100% functionally compatible with AmPAL18P8B and all 16L8, 16P8, 16H8, 16L2, 16H2, 14L4, 14H4, 12L6, 12H6, 10L8, 10H8, 16LD8 and 16HD8 PAL type products**
- **Field-Programmable**
- **10 inputs**
- **8 bidirectional I/O lines**
- **72 AND gates/product terms**
  - **configured into eight groups of nine**
- **Programmable output polarity (3-State output)**
- **I/O propagation delay: 15ns (max)**
- **Power dissipation: 500mW (typ)**
- **TTL compatible**
- **Security Fuse**

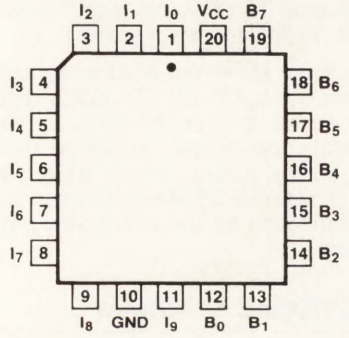
PIN CONFIGURATIONS

N Package



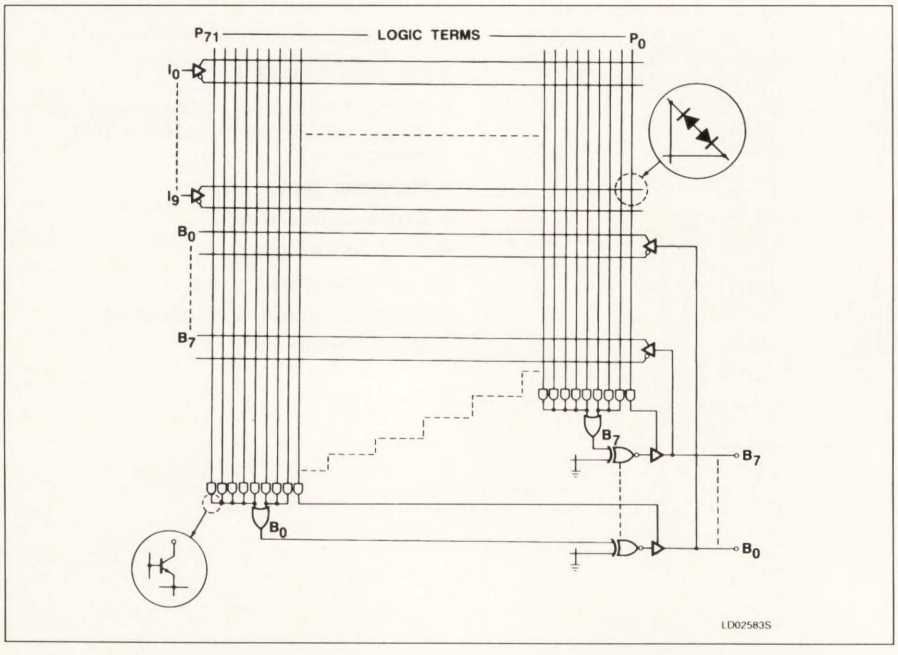
CD05324S

A Package



CD05330S

FUNCTIONAL DIAGRAM



LD02583S

APPLICATIONS

- **100% functional replacement for all 20-pin combinatorial PAL devices**
- **Random logic**
- **Code converters**
- **Fault detectors**
- **Function generators**
- **Address mapping**
- **Multiplexing**

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PLC16V8 Series
Erasable and OTP Programmable Array Logic (16 × 72 × 8)

Application Specific Products
- **Series 20**

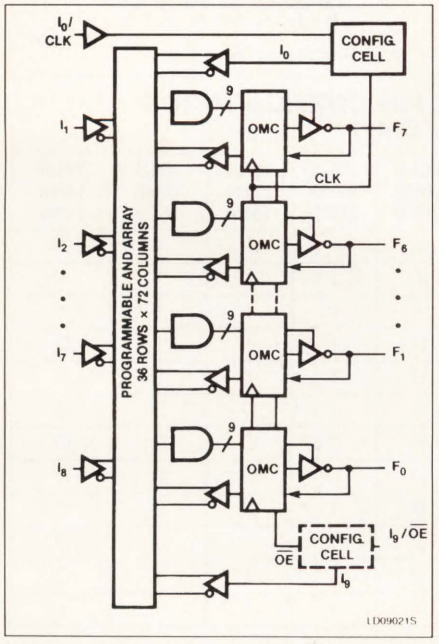
Signetics Programmable Logic
Product Specification

DESCRIPTION

The PLC16V8 Programmable Array Logic device is a 20-pin CMOS PLD designed to replace full-power as well as quarter-power and half-power Series 20 PAL® devices. Available in four speed/power configurations, the generic PLC16V8 device can be configured to emulate 22 different PAL devices in multiple speed/power configurations. The more complex AND/OR logic functions can be easily implemented with the PLC16V8 because of the flexibility inherent to its generic Output Macro Cell architecture.

The PLC16V8 is a two-level logic element comprised of 10 inputs, 72 AND gates and 8 Output Macro Cells (OMC). Each Output Macro Cell can be individually configured as a dedicated input, a dedicated output, a bidirectional I/O or as a registered output with feedback. This generic architecture provides a means of reducing documentation, inventory and manufacturing related costs. Furthermore, the PLC16V8 series devices are designed to accept both TTL and CMOS input levels to facilitate logic integration in almost any system environment.

FUNCTIONAL DIAGRAM



FEATURES

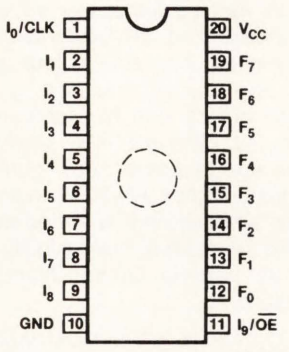
- **100% functional replacement for Series 20 PAL devices**
  $-I_{OL}$ = 24mA
- **Low power performance:**
  50 and 90mA max
  - **All inputs and outputs switching at 15MHz**
- **Equivalent bipolar performance**
  - **35 and 45ns t_{PD}**
  - **28.5 and 22.2MHz f_{MAX} (async)**
- **EPROM cell technology**
  - **Erasable**
  - **100% testable**
  - **Reconfigurable (quartz window package only)**
- **TTL and CMOS compatible**
- **Security fuse**
- **Available in 300mil-wide DIP with quartz window, plastic DIP (OTP), or PLCC (OTP)**

PIN LABEL DESCRIPTIONS

I	Dedicated input
B	Bidirectional input/output
O	Dedicated output
D	Registered output (D-type flip-flop)

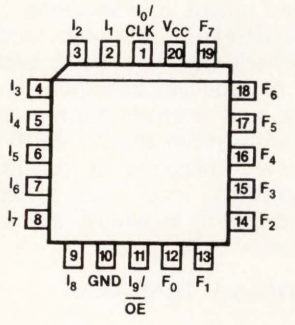
PIN CONFIGURATIONS

N and FA Packages



N = Plastic
FA = Ceramic with Quartz Window

A Package



A = Plastic Leaded Chip Carrier

PAL DEVICE TO PLC16V8 OUTPUT PIN CONFIGURATION CROSS REFERENCE

PIN NO.	PLC 16V8	16L8 16H8 16P8 18P8	16R4 16RP4	16R6 16RP6	16R8 16RP8	16L2 16H2 16P2	14L4 14H4 14P4	12L6 12H6 12P6	10L8 10H8 10P8
1	I_0/CLK	I	CLK	CLK	CLK	I	I	I	I
19	F7	B	B	B	D	I	I	I	O
18	F6	B	B	D	D	I	I	O	O
17	F5	B	D	D	D	I	O	O	O
16	F4	B	D	D	D	O	O	O	O
15	F3	B	D	D	D	O	O	O	O
14	F2	B	D	D	D	I	O	O	O
13	F1	B	B	D	D	I	I	O	O
12	F0	B	B	B	D	I	I	I	O
11	$I_9/\overline{OE}$	I	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	I	I	I	I

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Signetics

PLC20V8 Series
Erasable and OTP Programmable Array Logic (20 × 72 × 8)

Application Specific Products
- **Series 24**

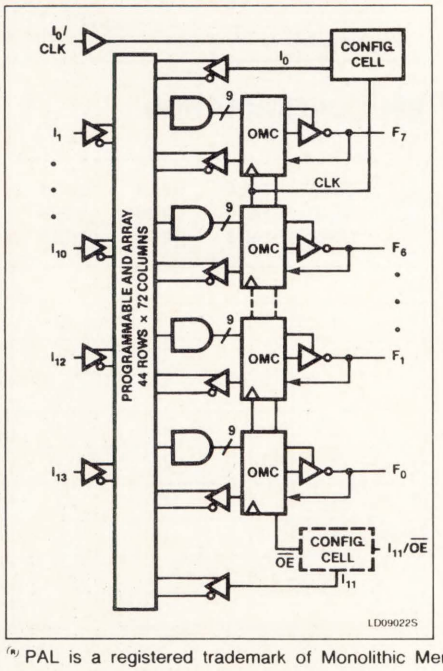
Signetics Programmable Logic
Product Specification

DESCRIPTION

The PLC20V8 Programmable Array Logic device is a 24-pin CMOS PLD designed to replace full-power as well as quarter-power and half-power Series 24 PAL® devices. Available in four speed/power configurations, the generic PLC20V8 device can be configured to emulate 21 different PAL devices in multiple speed/power configurations. The more complex AND-OR logic functions can be easily implemented with the PLC20V8 because of the flexibility inherent to its generic Output Macro Cell architecture.

The PLC20V8 is a two-level logic element comprised of 14 inputs, 72 AND gates and 8 Output Macro Cells (OMC). Each Output Macro Cell can be individually configured as a dedicated input, a dedicated output, a bidirectional I/O or as a registered output with feedback. This generic architecture provides a means of reducing documentation, inventory and manufacturing related costs. Furthermore, the PLC20V8 series devices are designed to accept both TTL and CMOS input levels to facilitate logic integration in almost any system environment.

FUNCTIONAL DIAGRAM



FEATURES

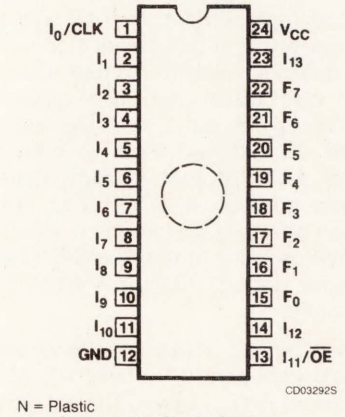
- **100% functional replacement for Series 24 PAL devices**
  $-I_{OL}$ = 24mA
- **Low power performance:**
  50 and 90mA max
  - **All inputs and outputs switching at 15MHz**
- **Equivalent bipolar performance**
  - **35 and 45ns t_{PD}**
  - **28.5 and 22.2MHz f_{MAX} (async)**
- **EPROM cell technology**
  - **Erasable**
  - **100% testable**
  - **Reconfigurable (quartz window package only)**
- **TTL and CMOS compatible**
- **Security fuse**
- **Available in 300mil-wide DIP with quartz window, plastic DIP (OTP), or PLCC (OTP)**

PIN LABEL DESCRIPTIONS

I	Dedicated input
B	Bidirectional input/output
O	Dedicated output
D	Registered output (D-type flip-flop)

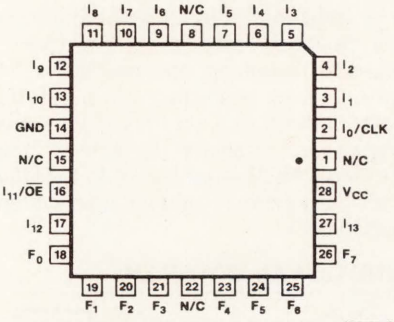
PIN CONFIGURATIONS

N Package



N = Plastic
FA = Ceramic with Quartz Window

A Package



A = Plastic Leaded Chip Carrier

PAL DEVICE TO PLC20V8 OUTPUT PIN CONFIGURATION CROSS REFERENCE (DIP Packages Only)

PIN NO.	PLC 20V8	20R8 20RP8	20R6 20RP6	20R4 20RP4	20L8 20H8 20P8	20L2 20H2 20P2	18L4 18H4 18P4	16L6 16H6 16P6	14L8 14H8 14P8
1	I_0/CLK	CLK	CLK	CLK	I	I	I	I	I
13	$I_{11}/\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	I	I	I	I	I
14	I_{12}	I	I	I	I	I	I	I	I
15	F0	D	B	B	O	I	I	I	O
16	F1	D	D	B	B	I	I	O	O
17	F2	D	D	D	B	I	O	O	O
18	F3	D	D	D	B	O	O	O	O
19	F4	D	D	D	B	O	O	O	O
20	F5	D	D	D	B	I	O	O	O
21	F6	D	D	B	B	I	I	O	O
22	F7	D	B	B	O	I	I	I	O
23	I13	I	I	I	I	I	I	I	I

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Signetics

PLS179
Field-Programmable Logic Sequencer (20 X 45 X 12)

Signetics Programmable Logic
Product Specification

Application Specific Products
- **Series 24**

DESCRIPTION

The PLS179 is a 3-State output, registered logic element combining AND/OR gate arrays with clocked J-K flip-flops. These J-K flip-flops are dynamically convertible to D-type via a "foldback" inverting buffer and control gate F_C. It features 8 registered I/O outputs (F) in conjunction with 4 bidirectional I/O lines (B). There are 8 dedicated inputs. These yield variable I/O gate and register configurations via control gates (D, L) ranging from 20 inputs to 12 outputs.

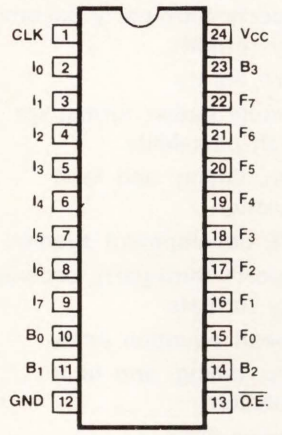
The AND/OR arrays consist of 32 logic AND gates, 13 control AND gates, and 21 OR gates with fusible link connections for programming I/O polarity and direction. All AND gates are linked to 8 inputs (I), bidirectional I/O lines (B), internal flip-flop outputs (Q), and Complement Array output ($\overline{C}$). The Complement Array consists of a NOR gate optionally linked to all AND gates for generating and propagating complementary AND terms.

FEATURES

- **f_{MAX} = 18.2MHz**
  - **25MHz clock rate**
- **Field-Programmable (Ni-Cr link)**
- **8 dedicated inputs**
- **13 control gates**
- **32 AND gates**
- **21 OR gates**
- **45 product terms:**
  - **32 logic terms**
  - **13 control terms**
- **4 bidirectional I/O lines**
- **8 bidirectional registers**
- **J/K, T, or D-type flip-flops**
- **Asynchronous Preset/Reset**
- **Complement Array**
- **Active-High or -Low outputs**
- **Programmable $\overline{OE}$ control**
- **Positive edge-triggered clock**
- **Power-on reset on flip-flop (F_n = "1")**
- **Input loading: PLS179: – 100μA (max.)**
- **Power dissipation: 750mW (typ.)**
- **TTL compatible**
- **3-State option**

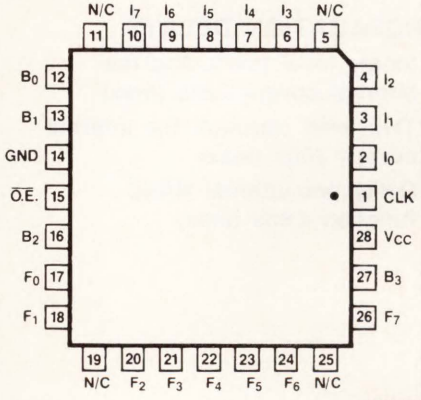
PIN CONFIGURATIONS

N Package



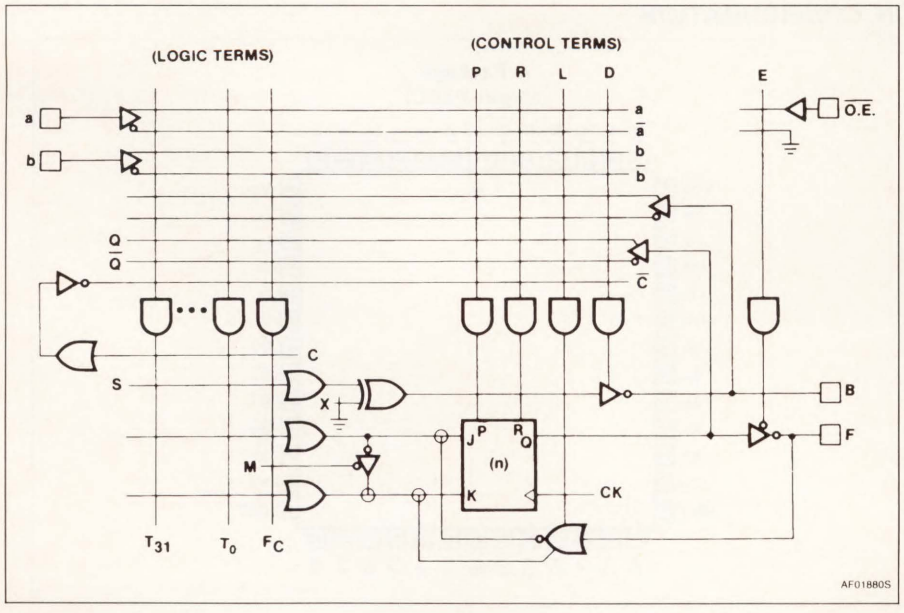
CD04521S

A Package*



CD04530S

FUNCTIONAL DIAGRAM



AF01880S

APPLICATIONS

- **Random sequential logic**
- **Synchronous up/down counters**
- **Shift registers**
- **Bidirectional data buffers**
- **Timing function generators**
- **System controllers/synchronizers**
- **Priority encoder/registers**

5

Signetics

PLHS501
Programmable Macro Logic

Product Specification

Applied Specific Application Products • PML Series

FEATURES

- Programmable instant gate array
- SNAP development system:
  - Supports third-party schematic entry formats
  - Macro library
  - Versatile netlist format for design portability
  - Logic, timing, and fault simulation
- AMAZE development system:
  - Supports third-party schematic entry formats
  - Boolean equation entry
  - Logic, timing, and fault simulation
- TTL compatible
- Power dissipation = 1.12W (typ.)

PROPAGATION DELAYS

- Single level (excluding the internal core) = 22ns (max)
- Two level (through the internal core) = 30ns (max)
- Delay per internal NAND function = 8ns (max)

STRUCTURE

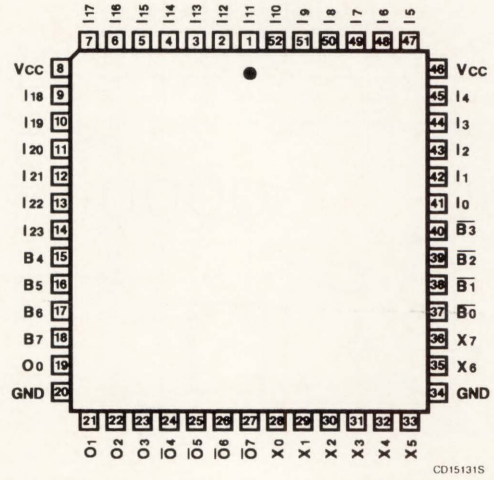
- NAND gate based architecture:
  - 72 foldback NAND terms
- 24 dedicated inputs (I0 – I23)
- 8 bidirectional I/Os with individual 3-State enable:
  - 4 active-High (B4 – B7)
  - 4 active-Low (/B0 – /B3)
- 16 dedicated outputs:
  - 4 active-High outputs:
    O0, O1 with common 3-State enable
    O2, O3 with common 3-State enable
  - 4 active-Low outputs:
    $\overline{O4}$, $\overline{O5}$ with common 3-State enable
    $\overline{O6}$, $\overline{O7}$ with common 3-State enable
  - 8 Exclusive-OR outputs:
    X0 – X3 with common 3-State enable
    X4 – X7 with common 3-State enable
- Security fuse allows protection of proprietary designs
- Testable in unprogrammed state

DESCRIPTION

The PLHS501 is a high-density Bipolar Programmable Macro Logic device. PML incorporates a programmable NAND structure. The NAND architecture is an efficient method for implementing any logic function. The SNAP software development system provides a user friendly environment for design entry. SNAP eliminates the need for a detailed understanding of the PLHS501 architecture and makes it transparent to the user. PLHS501 is also supported on the Signetics AMAZE software development system.

PIN CONFIGURATION

A Package
(52-pin PLCC)



Signetics

PML1500
Programmable Macro Logic

Preliminary Specification

Application Specific Products

FEATURES
- Programmable instant gate array
- SNAP development system
  - Supports third-party schematic entry formats
  - Macro library
  - Versatile netlist format for design portability
  - Logic, timing, and fault simulation
- TTL compatible
- Power dissipation = 1.25W (typ.)

PROPAGATION DELAYS
- Single level (excluding the internal core) = 22ns (max)
- Two level (through the internal core) = 30ns (max)
- Delay per internal NAND function = 8ns (max)
- Maximum operating frequency = 50MHz (internal flip-flop)

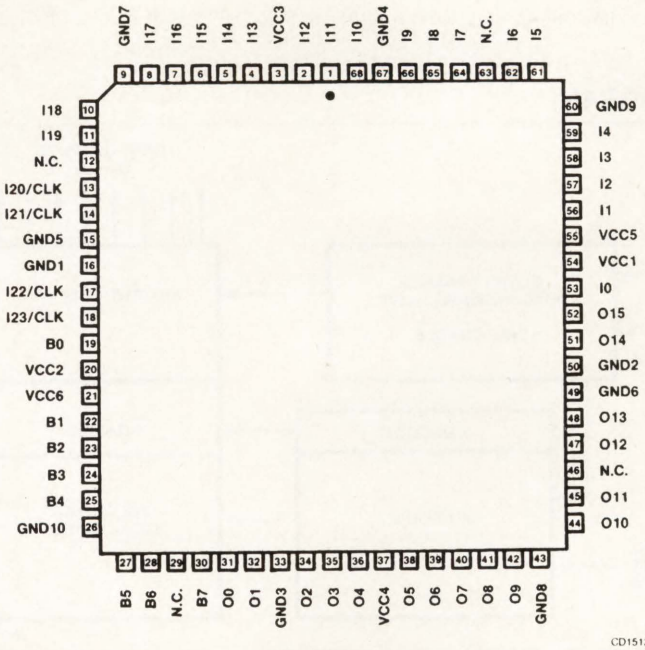
STRUCTURE
- NAND gate based architecture
  - 64 foldback NAND terms
- 20 dedicated inputs
- 4 programmable input/clock inputs
- 8 independent clocks
  - 4 from input/clock pins
  - 4 from NAND array
- 8 bidirectional I/Os
- 16 dedicated outputs
  - 8 active-High outputs
  - 4 outputs with programmable polarity
  - 4 3-State outputs with programmable polarity
- 16 buried flip-flops
  - 8 D type
  - 8 S-R type
- Security fuse allows protection of proprietary designs
- Testable in unprogrammed state

DESCRIPTION
The PML1500 is a high-density Bipolar Programmable Macro Logic device. PML incorporates a programmable NAND structure. The NAND architecture is an efficient method for implementing any logic function. The SNAP software development system provides a user friendly environment for design entry. SNAP eliminates the need for a detailed understanding of the PML1500 architecture and makes it transparent to the user.

6

PIN CONFIGURATION

A Package
(68-pin PLCC)



Signetics

27C256 O.T.P.
One Time Programmable 256K (32K × 8) EPROMs

Product Specification

Application Specific Products

DESCRIPTION

Signetics 27C256 CMOS O.T.P. EPROM is a 256K-bit 5V only memory organized as 32,768 words of 8 bits each. It employs advanced CMOS circuitry for systems requiring low power, high-performance speeds, and immunity to noise. The 27C256 has a non-multiplexed addressing interface and is plug-compatible with the industry standard 27256.

The 27C256 O.T.P. is offered in plastic DIP and plastic leaded chip carrier (PLCC) packages. Plastic EPROMs provide optimum cost effectiveness in production environments. Quick-pulse programming is employed on plastic devices which may speed up programming by as much as one hundred times.

FEATURES

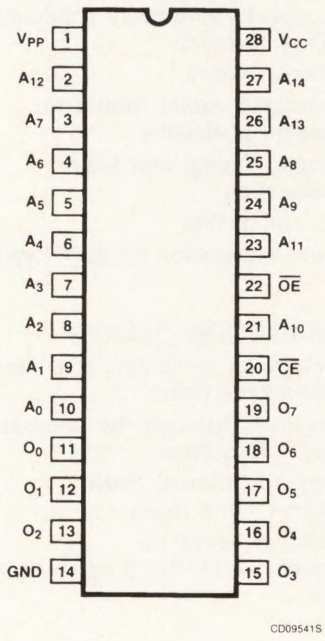
- **Low power consumption**
  - **100μA maximum CMOS standby current**
- **Quick-pulse programming algorithm for high-speed production programming**
- **High-performance speeds**
  - **27C256-15: 150ns maximum access time**
  - **27C256-17: 170ns maximum access time**
- **Noise immunity features**
  - **± 10% V_{CC} tolerance**
  - **Maximum latch-up immunity through epitaxial processing**

PIN DESCRIPTION

$A_0 - A_{14}$	Addresses
$O_0 - O_7$	Outputs
$\overline{OE}$	Output enable
$\overline{CE}$	Chip enable
N.C.	No connection
GND	Ground
V_{PP}	Program voltage
V_{CC}	Power supply
DU	Don't use

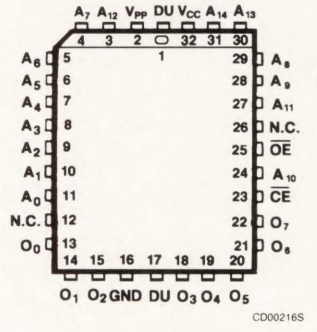
PIN CONFIGURATIONS

N Package



CD09541S

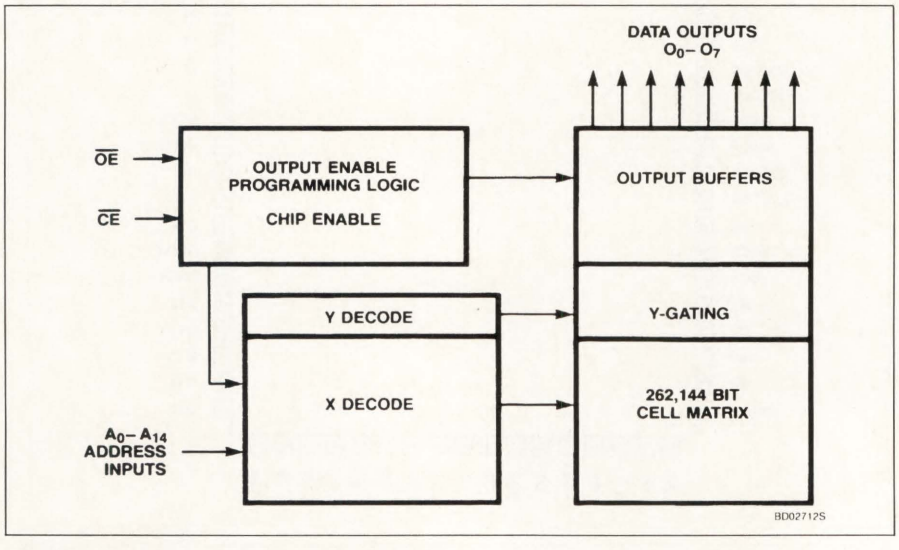
A Package



CD00216S

TOP VIEW

BLOCK DIAGRAM



BD02712S

Signetics

27C256 U.V. Erasable 256K (32K × 8) EPROMs

Product Specification

Application Specific Products

DESCRIPTION

Signetics 27C256 CMOS EPROM is a 256K-bit 5V only memory organized as 32,768 words of 8 bits each. It employs advanced CMOS circuitry for systems requiring low power, high-performance speeds, and immunity to noise. The 27C256 has a non-multiplexed addressing interface and is plug-compatible with the industry standard 27256.

The 27C256 available in a ceramic DIP package, achieves both high performance and low power consumption, making it ideal for high-performance, portable equipment. This device can be programmed with standard EPROM programmers.

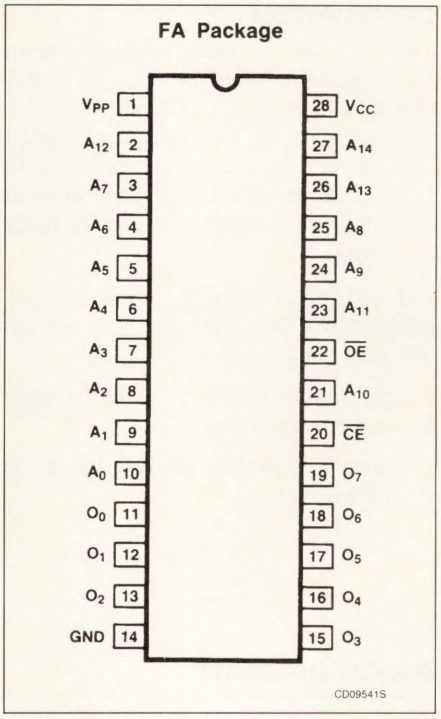
FEATURES

- **Low power consumption**
  - **100μA maximum CMOS standby current**
- **Quick pluse programming algorithm for high-speed production programming**
- **High-performance speeds**
  - **27C256-15: 150ns maximum access time**
  - **27C256-17: 170ns maximum access time**
- **Noise immunity features**
  - **± 10% V_{CC} tolerance**
  - **Maximum latch-up immunity through epitaxial processing**

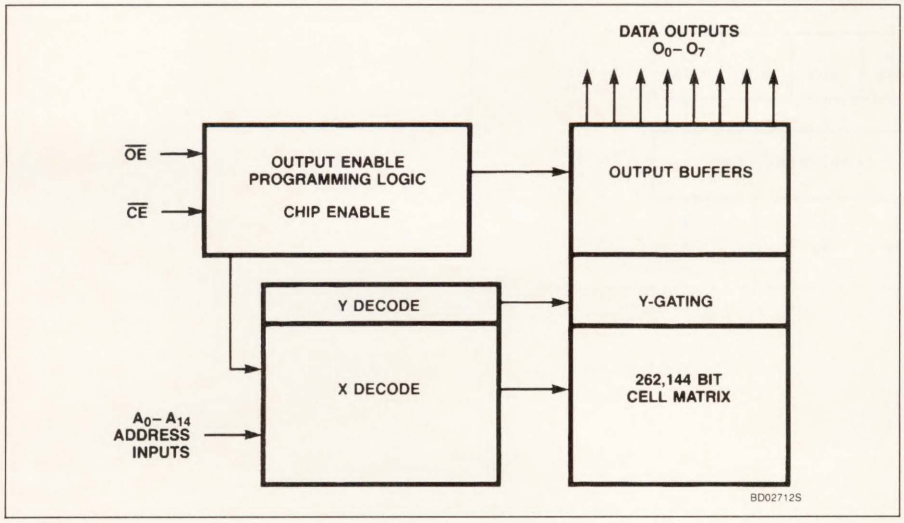
PIN DESCRIPTION

$A_0 - A_{14}$	Addresses
$O_0 - O_7$	Outputs
$\overline{OE}$	Output enable
$\overline{CE}$	Chip enable
GND	Ground
V_{PP}	Program voltage
V_{CC}	Power supply

PIN CONFIGURATION



BLOCK DIAGRAM



Signetics

10149A
1K-Bit ECL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 10149A is field programmable, meaning that custom patterns are immediately available by following the ECL fusing procedure. The device is supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

The 10149A is suitable for use in high-performance ECL systems. The outputs are capable of driving 50Ω loads.

A Chip Enable input is provided for ease of memory expansion.

Ordering information can be found on the following page.

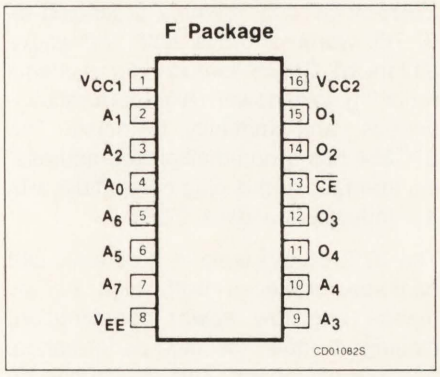
FEATURES

- **Address access time: 10ns max**
- **Power dissipation: 0.66mW/bit typ**
- **High impedance inputs (50kΩ pulldown)**
- **One Chip Enable input**
- **Open Emitter outputs (50Ω drive)**
- **On-chip address decoding**
- **No separate fusing pins**
- **Fully compatible with ECL 10K series**

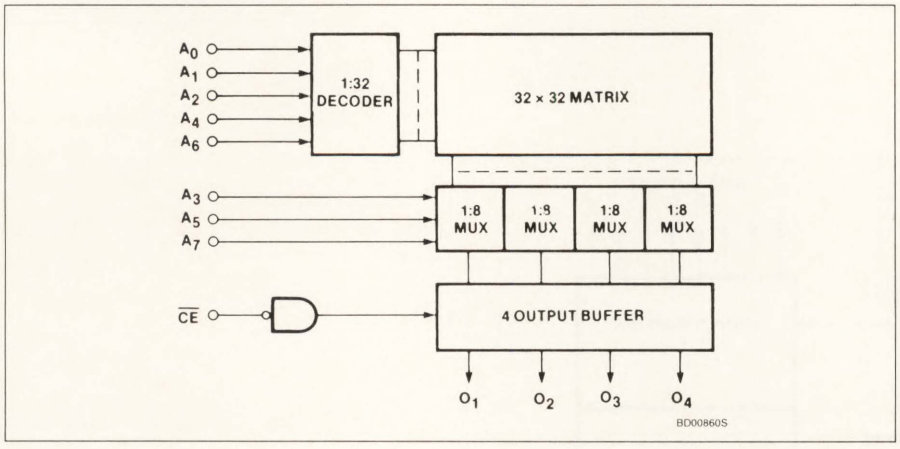
APPLICATIONS

- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION



BLOCK DIAGRAM



Signetics

27HC641
65,536-Bit UV Erasable CMOS PROM (8K × 8)

Product Specification

Application Specific Products

DESCRIPTION

The 27HC641 is a CMOS, high-speed ultraviolet light erasable electrically programmable Read Only Memory. It is organized as 8192 words of 8 bits and operates from a single 5V ± 10% power supply. All outputs offer 3-State operation and are fully TTL-compatible.

The 27HC641 uses advanced CMOS circuitry which allows operation at bipolar PROM speeds while consuming lower power. The highest degree of protection against latch-up is achieved through epitaxial processing, simplifying the design of electronic equipment which is subject to high noise environments.

The 27HC641 is available in an industry standard 24-pin dual in-line package with the same pinout as most 64K bipolar PROMs. This makes it easy to upgrade systems currently using bipolar PROMs and provide a lower power memory system solution.

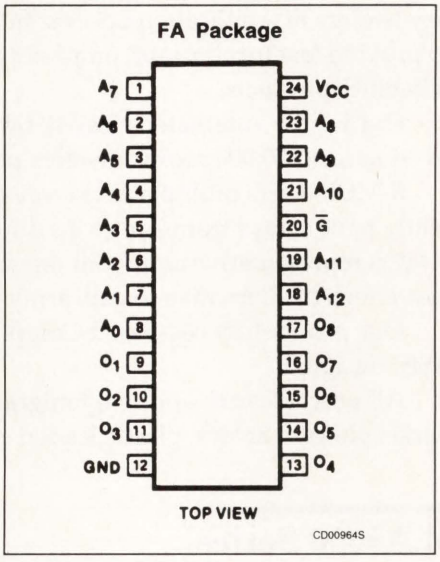
FEATURES

- **Address access time:**
  - **27HC641-55 55ns max**
  - **27HC641-45 45ns max**
  - **27HC641-35 35ns max**
- **Operating I_{CC}: 110mA max**
- **3-State outputs**
- **JEDEC standard 24-pin DIP package**
- **Direct replacement for standard 64K TTL PROMs**
- **Fully TTL-compatible**

APPLICATIONS

- **Prototyping and volume production**
- **High-performance mini- and microcomputers**
- **High-speed program store and look-up tables**

PIN CONFIGURATION



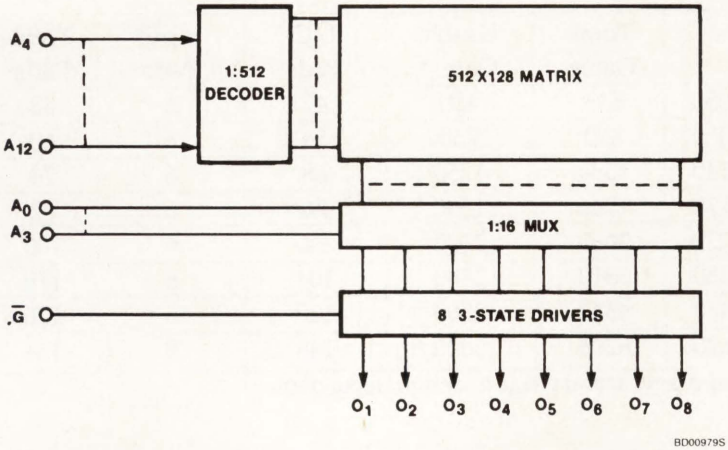
PIN NAMES

$A_0 - A_{12}$	Address inputs
$O_1 - O_8$	Data outputs
$\overline{G}$	Output Enable
V_{CC}	Supply voltage
GND	Ground (V_{SS})

ORDERING INFORMATION

PACKAGE DESCRIPTION	ORDER CODE		
	35ns	45ns	55ns
24-pin ceramic DIP with quartz window 600mil-wide	27HC641-35 FA	27HC641-45 FA	27HC641-55 FA

BLOCK DIAGRAM



March 6, 1987

S-MOS SYSTEMS

ASIC Product Overview

S-MOS Systems, Inc. and our affiliate, Seiko Epson Corporation, form a team that is one of the world's technology leaders in Application Specific Integrated Circuits. Advanced design and manufacturing capabilities enable us to provide fast turn-around on prototypes and quickly ramp to volume production with high-performance, high-reliability products.

Our highly automated class-10 fab lines have a remarkable capacity to produce over 40,000 four-inch, 20,000 five-inch and 20,000 six-inch wafers per month.

S-MOS offers multiple gate array families so you can choose the one that best suits your application. We currently have arrays from 2 microns down to 1.2 micron drawn feature sizes and complexities to 38,550 gates. Ask an S-MOS representative about our latest developments. The S-MOS ASIC program also includes standard cells as a cost-effective alternative to gate arrays for high-volume needs.

Our proprietary cell-based Compiled Cell Custom is yet another option for executing complex and high-volume ASIC designs.

All processes are upwardly migratable with automatic conversion. Most devices are available in plastic quad flat packs, pin grid arrays, plastic leaded chip carriers, small outline packages and plastic dual-in-line packages.

SLA6000 Series

- **High Speed CMOS Gate Arrays**
- **2 Micron Drawn (1.7 micron effective) Channel Length**
- **Typical Gate Delays of 1.43 ns Driving Two Internal Loads**

Product Description

The SLA6000 Series consists of a group of 8 CMOS Gate Arrays with gate counts from 513 to 6206 total gates. The series is fabricated utilizing our 2 micron high speed CMOS silicon gate technology to achieve propagation delays of 1.43 ns for a 2-input NAND gate driving two internal loads. All I/O buffers are TTL and CMOS compatible which makes this series an ideal choice for replacing existing discrete logic as well as for new designs.

A wide variety of packages is available including Plastic DIP, SOP, PLCC, Low Cost PGA, Ceramic PGA and our advanced high density flat packages for surface mounting.

SLA6000 CMOS Gate Arrays

Array	Total Gates	Usable Gates*	I/O Pads	Input Pads	Total Pads
SLA6050	513	480	42	6	48
SLA6080	820	750	54	6	60
SLA6140	1394	1250	68	6	74
SLA6170	1746	1530	76	6	82
SLA6270	2667	2300	94	6	100
SLA6330	3312	2780	104	6	110
SLA6430	4342	3560	120	6	126
SLA6620	6206	5000	146	8	154

*Typical usage; actual usage is design dependent.

S-MOS Systems, Inc., 2460 North First Street, San Jose, CA 95131 (408) 922-0200

SLA7000 Series

- **Very High Speed CMOS Gate Arrays**
- **1.5 Micron Drawn (1.2 micron effective) Channel Length**
- **Typical Gate Delays 0f 830 Picoseconds Driving Two Internal Loads**

Product Description

The SLA7000 Series consists of a group of 6 channeled arrays and 3 channelless arrays with up to 16,250 total gates. The series is fabricated utilizing our 1.5 micron very high speed CMOS silicon gate technology to achieve propagation delays of 830 ps for a 2-input NAND gate driving two internal loads.

All S-MOS/Seiko gate arrays are produced in one of the largest dedicated CMOS facilities in the world and tested at speeds up to 40MHz assuring quality, volume production.

A wide variety of package types is available including DIP, SOP, PLCC, Low Cost PGA, Ceramic PGA, and our advanced high density flat packages to 196 pins, for surface mounting.

SLA7000 CMOS Gate Arrays

Array	Total Gates	Usable Gates*	I/O Pads	Input Pads	Total Pads
SLA7160	1632	1500	70	8	78
SLA7220	2232	2000	82	8	90
SLA7340	3432	2950	104	8	112
SLA7490	4900	4100	128	8	136
SLA7620	6210	4900	150	8	158
SLA760S	11040	5500	150	8	158
SLA7800	8000	6000	170	8	178
SLA775S	13500	6800	168	8	176
SLA790S	16250	8000	170	8	178

*Typical usage; actual usage is design dependent.

SLA700B Series

- **High Output Drive CMOS Gate Array**
- **Selectable IOL to 24mA**
- **1.5 Micron Drawn (1.2 micron effective) Channel Length**

Product Description

The SLA700B Series consists of 4 CMOS gate arrays with special high drive output cells. These arrays are perfectly suited for high current busses, SCSI interfacing, or any other application which requires up to 48 mA. The outputs are designed to deliver the rated current over temperature, voltage, and process extremes at VOL = 0.4 volts.

The internal gate delays are very fast (830 ps), and each device is tested at your system clock speed up to 40 MHz.

A wide variety of package types is available including DIP, SOP, PLCC, Low Cost PGA, Ceramic PGA, and advanced flat packages for surface mounting.

SLA700B CMOS Gate Arrays

Array	Total Gates	Usable Gates*	I/O Pads	Input Pads	Total Pads
SLA708B	825	780	84	8	92
SLA715B	1500	1350	100	8	108
SLA724B	2482	2200	122	8	130
SLA738B	3792	3300	148	8	156

*Typical usage; actual usage is design dependent.

SLA100L Series

- **Operating Voltage of 0.9V to 6.0V**
- **Typical Gate Delays of 1.14 ns at 5 Volts**
- **Ideal for Battery Operated Devices**

Product Description

The SLA100L Series consists of a group of 6 CMOS Gate Arrays with up to 8000 available gates. The arrays are fabricated utilizing our proprietary low voltage CMOS technology based on years of experience making watches and other items requiring low voltage operation. The SLA100L Series is perfectly suited for any battery operation such as 1.5V or 3V. An important feature is that its wide voltage operation (0.9Volts to 6.0 Volts) is achieved by using our special low voltage process, not by screening, thus assuring that the design will work through the required voltage range.

SLA100L Low Voltage CMOS Gate Arrays

Array	Total Gates	Usable Gates*	I/O Pads	Input Pads	Total Pads
SLA116L	1632	1500	70	8	78
SLA122L	2232	2000	82	8	90
SLA134L	3432	2950	104	8	112
SLA149L	4900	4100	128	8	136
SLA162L	6210	4900	150	8	158
SLA180L	8000	6000	170	8	178

*Typical usage; actual usage is design dependent.

SLA8000 Series

- **Very High Speed/ High Density CMOS Gate Arrays**
- **1.2 Micron Drawn (1.05 micron effective) Channel Length**
- **Typical Gate Delays of 640 Picoseconds Driving Two Internal Loads**

Complete Data Sheet Follows

Product Description

The SLA8000 Series consists of a group of 7 CMOS gate arrays with gate counts from 5304 to 38,550 available gates. The series is fabricated utilizing our state-of-the-art, 1.2 micron, very high speed silicon gate technology.

Every macrocell included in our library has been fully characterized in silicon. The propagation delay values come from actual measurements of performance rather than SPICE simulations. Futhermore, all delay figures are specified at 3 sigma limits over process, temperature, and voltage, virtually guaranteeing that your production part will meet your simulation results.

The SLA8000 Series is manufactured on our highly automated six inch line and tested at speeds up to 40 MHz. It is available in a wide variety of packages including DIP, SOP, PLCC, Low Cost PGA, Ceramic PGA, and our advanced high density flat packages to 196 pins, for surface mounting.

SLA8000 CMOS Gate Arrays

Array	Total Gates	Usable Gates*	I/O Pads	Input Pads	Total Pads
SLA827S	5304	2900	82	4	86
SLA847S	9416	5100	108	4	112
SLA872S	14336	7700	136	4	140
SLA890S	18300	9700	152	4	156
SLA8B3S	22680	11800	168	4	172
SLA8F0S	30000	15000	194	4	198
SLA8J0S	38550	19000	222	4	226

*Typical usage; actual usage is design dependent.

SSC1000 Series

- **High Density Standard Cells**
- **1.8 Micron Drawn (1.25 micron effective) Channel Length**
- **Typical Gate Delays of 910 Picoseconds Driving Two Internal Loads**
- **Output Drive to 24mA IOL**

Product Description

The SSC1000 Series is a high density standard cell family with usable gate counts to 15,000 gates and I/O to 192 pads. It is ideally suited for high volume applications since it is denser than equivalent gate arrays allowing for a lower cost per gate. There are currently over 300 fully characterized cells in the library with propagation delays specified at 3 sigma limits for process, voltage, and temperature.

S-MOS/Seiko has one of the most stringent quality control programs in the industry. We have shipped millions of SSC1000 parts with an electrical defect rate of less than .0001% to date (less than 1ppm AOQL), making this series an ideal choice for very high quality/volume production requirements.

The SSC1000 Series is available in a wide variety of packages including DIP, SOP, PLCC, Low Cost PGA, Ceramic PGA, and our advanced flat packages to 196 pins, for surface mounting. Many packages are also available in Tape and Reel for high speed auto insertion equipment.

SSC3000 Series

- **Very High Density Standard Cells**
- **1.2 Micron Drawn (1.05 micron effective) Channel Length**
- **Typical Gate Delays of 610 Picoseconds Driving Two Internal Loads**
- **Output Drive to 24mA IOL**

Product Description

The SSC3000 Series is a high density standard cell family with usable gate counts to 20,000 gates and I/O to 192 pads. It is ideally suited for high volume applications since it is denser than equivalent gate arrays allowing for a lower cost per gate. There are currently over 300 fully characterized cells in the library with propagation delays specified at 3 sigma limits for process, voltage, and temperature. The series is fabricated utilizing our state-of-the-art, 1.2 micron, very high speed silicon gate technology.

The SSC3000 Series is available in a wide variety of packages including DIP, SOP, PLCC, Low Cost PGA, Ceramic PGA, and our advanced flat packages to 196 pins, for surface mounting.

Compiled Cell Custom

Product Description

CC Custom is S-MOS' proprietary cell-based custom design process that is faster and more cost-effective than full custom. With this system, S-MOS engineers can develop large, functional custom blocks for customers, then implement them, along with logic, on a single chip.

The logic can be captured and simulated at your own site with S-MOS' LADS software. The logic is then combined with the custom blocks and routed using our timing-driven place-and-router. This software simulates the entire circuit, place-and-routes it, resimulates, and re-place-and-routes. This process continues until all paths meet the original pre-route timing.

The entire process through PG-tape is complete at our facility in San Jose, California. Process technology includes our 1.8, 1.5 and 1.2 micron drawn CMOS processes.

The S-MOS CC Custom cell library is continually expanding and currently includes microprocessor core cells, peripheral cells, and RAM and ROM blocks.

S-MOS SYSTEMS

SLA8000 Series

VERY HIGH SPEED CHANNELLESS CMOS GATE ARRAYS

Description

The SLA8000 Series consists of a group of seven very high-speed, sea-of-gates CMOS gate arrays. The series is fabricated utilizing our state-of-the-art 1.2 micron silicon gate technology. Gate counts range from 5K to 38K available gates with pinouts to 226 pads.

Features

- 1.2 micron drawn (0.9 micron effective) channel length.
- Very high speed: t_{pd} (typ) = .6ns/gate
- Seven configurations
- 24mA Iol using three pads
- RAM and ROM blocks available
- Megacell compatible
- Fully migratable to S-MOS standard cells.

Product Configuration

ARRAY	TOTAL GATES	USABLE GATES*	I/O PADS	POWER PADS	TOTAL PADS
SLA827S	5304	3000	82	4	86
SLA847S	9416	5000	108	4	112
SLA872S	14336	8000	136	4	140
SLA890S	18300	10000	152	4	156
SLA8B3S	22680	12000	168	4	172
SLA8F0S	30000	16000	194	4	198
SLA8J3S	38550	21000	222	4	226

*Typical usage; actual usage is design dependent.

S-MOS Systems, Inc., 2460 North First Street, San Jose, CA 95131 (408) 922-0200

Absolute Maximum Ratings

Parameter	Symbol	Limits	Units
DC supply voltage	V_{DD}	V_{SS}-0.3 to 7.0	Volts
Input voltage	V_{IN}	V_{SS}-0.3 to V_{DD}+0.3	Volts
Output voltage	V_{OUT}	V_{SS}-0.3 to V_{DD}+0.3	Volts
Storage temp.	T_{STG}	-65 to +150	°C

Recommended Operating Conditions (commercial)

VSS = OV

Parameter	Symbol	MIN	TYP	MAX	UNITS
DC supply voltage	V_{DD}	4.75	5.0	5.25	Volts
Input voltage	V_{IN}	V_{SS}		V_{DD}	Volts
Operating temp.	T_{OPR}	0		70	°C

V_{DD} range of +,-10% and extended temperature range available upon request.

DC Characteristics

Symbol	Parameter	Conditions	VDD	MIN	TYP	MAX	UNITS
V_{IL}	Low level input voltage						
	CMOS Level		4.75			1.0	V
	TTL Level		4.75			0.8	V
V_{IH}	High level input voltage						
	CMOS level		5.25	3.5			V
	TTL Level		5.25	2.0			V
V_{T+}	Positive going threshold voltage						
	CMOS Schmitt Trigger		5.25			4.0	V
	TTL Schmitt Trigger		5.25			3.0	V
V_{T-}	Negative going threshold voltage						
	CMOS Schmitt Trigger		4.75	0.8			V
	TTL Schmitt Trigger		4.75	0.6			V
V_H	Hysteresis voltage						
	CMOS Schmitt Trigger		5.0	0.3			V
	TTL Schmitt Trigger		5.0	0.1			V
I_{IL}	Low level input current	$V_{IN}=V_{SS}$					
		No pull-up	5.25			1.0	uA
		Pull-up	5.25			100	uA
I_{IH}	High level input current	$V_{IN}=V_{DD}$					
		No pull-up	5.25			1.0	uA
		Pull-up	5.25			100	uA
V_{OL}	Low level output voltage						
	LOT + OSC	I_{OL}=50uA	4.75			0.4	V
	Type 1	I_{OL}=2mA	4.75			0.4	V
	Type 2	I_{OL}=6mA	4.75			0.4	V
	Type 3	I_{OL}=6mA	4.75			0.4	V
	Type W*	I_{OL}=12mA	4.75			0.4	V
	Type Q*	I_{OL}=24mA	4.75			0.4	V
V_{OH}	High level output voltage						
	LOT+OSC	I_{OH}=-50uA	4.75	V_{DD} -.4V			V
	Type 1	I_{OH}=-1mA	4.75	V_{DD} -.4V			V
	Type 2	I_{OH}=-1mA	4.75	V_{DD} -.4V			V
	Type 3	I_{OH}=-3mA	4.75	V_{DD} -.4V			V
	Type W*	I_{OH}=-6mA	4.75	V_{DD} -.4V			V
	Type Q*	I_{OH}=-6mA	4.75	V_{DD} -.4V			V
R_{PU}	Pull up resistor		5.0	50		500	KΩ
R_{PD}	Pull down resistor		5.0	50		500	KΩ
I_{OZ}	Tri-state leakage current		5.25			10	uA
C_{IN}	Input capacitance				4		pF
C_{OUT}	Output capacitance				6		pF
C_{BID}	Bidirectionl pad capacitance				10		pF

*Limited use

Function	Cell Name	Gates
SIMPLE GATES		
2-INPUT NAND GATE	NA2	1
3-INPUT NAND GATE	NA3	2
4-INPUT NAND GATE	NA4	2
2-INPUT NOR GATE	NO2	1
3-INPUT NOR GATE	NO3	2
4-INPUT NOR GATE	NO4	2
3-INPUT AND GATE	A3	2
6-INPUT AND GATE	A6	4
8-INPUT AND GATE	A8	5
3-INPUT OR GATE	O3	2
6-INPUT OR GATE	O6	4
8-INPUT OR GATE	O8	5
EXCLUSIVE OR GATE	EXO	3
EXCLUSIVE NOR GATE	EXN	3
COMPLEX GATES		
2-AND 2-WIDE 3-INPUT NOR GATE	AN23	2
3-AND 2-WIDE 4-INPUT NOR GATE	AN14	2
2-AND 2-WIDE 4-INPUT NOR GATE	AN24	2
2-AND 3-WIDE 4-INPUT NOR GATE	AN44	2
2-AND 3-WIDE 6-INPUT NOR GATE	AN36	5
2-AND 2-WIDE 3-INPUT NOR GATE	AO23	2
3-AND 2-WIDE 6-INPUT NOR GATE	AO26	4
4-AND 2-WIDE 8-INPUT NOR GATE	AO28	5
2-AND 4-WIDE 8-INPUT NOR GATE	AO48	5
2-OR 2-WIDE 3-INPUT NAND GATE	ON23	2
3-OR 2-WIDE 4-INPUT NAND GATE	ON14	2
2-OR 2-WIDE 4-INPUT NAND GATE	ON24	2
2-OR 3-WIDE 4-INPUT NAND GATE	ON34	2
2-AND 2-OR 2-WIDE 4-INPUT NAND GATE	ON44	2
2-OR 3-WIDE 6-INPUT NAND GATE	ON36	5
2-OR 2-WIDE 3-INPUT ANND GATE	OA23	2
3-OR 2-WIDE 6-INPUT NAND GATE	OA26	4
4-OR 2-WIDE 8-INPUT NAND GATE	OA28	5
2-OR 4-WIDE 8-INPUT NAND GATE	OA48	5
INVERTERS/BUFFERS		
NORMAL INVERTER	IN1	1
POWER INVERTER	IN2	1
POWER INVERTER	IN4	2
NORMAL BUFFER	BUF1	1
FLIP-FLOPS		
LATCH	LF	4
LATCH WITH RESET	LFR	5
LATCH WITH SET	LFP	5
D-FF	DF	6
D-FF WITH RESET	DFR	7
D-FF WITH SET	DFS	7
D-FF WITH SET AND RESET	DFSR	8
JK-FF WITH RESET	JKR	10
JK-FF WITH SET AND RESET	JKSR	11
ADDERS		
CARRY SAVE FULL ADDER	T183	9
COMPARATORS		
4-BIT MAGNITUDE COMPARATOR	T085	39
8-BIT MAGNITUDE COMPARATOR	T688	26
COUNTERS		
SYNCHRONOUS 4-BIT BINARY UP COUNTER WITH RESET, LOAD AND ENABLE	A161	57
SYNCHRONOUS 4-BIT BINARY UP COUNTER WITH RESET AND LOAD	T161E	51
SYNCHRONOUS 2-BIT BINARY UP COUNTER WITH RESET, LOAD AND ENABLE	A161H	29
SYNCHRONOUS 4-BIT BINARY UP COUNTER WITH RESET AND ENABLE	A161L	46
SYNCHRONOUS 4-BIT BINARY UP COUNTER WITH RESET	A161LE	40
SYNCHRONOUS 4-BIT BINARY UP COUNTER WITH LOAD AND ENABLE	A161R	52
SYNCHRONOUS 4-BIT BINARY UP COUNTER WITH LOAD	T161RE	46
FULLY SYNCHRONOUS 4-BIT BINARY UP COUNTER WITH RESET, LOAD AND ENABLE	A163	54
FULLY SYNCHRONOUS 4-BIT BINARY UP COUNTER WITH RESET AND LOAD	A163E	48
PRESETABLE 4-BIT BINARY UP COUNTER/LATCH WITH RESET AND LOAD	T177	39
PRESETABLE 2-BIT BINARY UP COUNTER/LATCH WITH RESET AND LOAD	T177H	21
PRESETABLE 4-BIT BINARY UP COUNTER/LATCH WITH LOAD	T177R	38
PRESETABLE 4-BIT BINARY DOWN COUNTER/LATCH WITH SET AND LOAD	T177V	39
PRESETABLE 2-BIT BINARY DOWN COUNTER/LATCH WITH SET AND LOAD	T177HV	20
PRESETABLE 4-BIT BINARY DOWN COUNTER/LATCH WITH LOAD	T177VR	38
SYNCHRONOUS 4-BIT UP/DOWN COUNTER WITH LOAD AND ENABLE	A191	70
SYNCHRONOUS 4-BIT UP/DOWN COUNTER WITH RESET	A191CE	47
SYNCHRONOUS 4-BIT UP/DOWN COUNTER WITH LOAD	A191E	63
SYNCHRONOUS 2-BIT UP/DOWN COUNTER WITH LOAD AND ENABLE	A191H	35
SYNCHRONOUS 4-BIT UP/DOWN COUNTER WITH RESET	A191LE	51
SYNCHRONOUS 4-BIT DUAL CLOCK BINARY UP/DOWN COUNTER WITH RESET AND LOAD	A193	69
SYNCHRONOUS 4-BIT DUAL CLOCK BINARY UP/DOWN COUNTER WITH RESET	A193L	53
SYNCHRONOUS 2-BIT DUAL CLOCK BINARY UP/DOWN COUNTER WITH RESET AND LOAD	A193H	36
SYNCHRONOUS 2-BIT DUAL CLOCK BINARY UP/DOWN COUNTER WITH RESET	A193HL	27
DECADE COUNTER WITH RESET	A390	32
4-BIT BINARY UP COUNTER WITH RESET	T393	25
4-BIT BINARY DOWN COUNTER WITH SET	T393V	25
DECODERS/DEMULTIPLEXERS		
BCD-TO-DECIMAL DECODER	T042	29
3-LINE TO 8-LINE DECODER/ DEMULTIPLEXER WITH ENABLE G	A138G2	18
2-LINE TO 4-LINE DECODER/ DEMULTIPLEXER WITH ENABLE G	A139	9
2-LINE TO 4-LINE DECODER/ DEMULTIPLEXER	A139G	6
DFFS/LATCHES		
4-BIT LATCH WITH RESET	T116	17
QUADRUPLE DFF WITH RESET	T175	27
QUADRUPLE DFF WITH Q, XQ	T175R	22
QUADRUPLE DFF WITH Q	T175RX	22
OCTAL DFF WITH RESET	T175W	54
OCTAL DFF	T175WR	44
OCTAL D-TYPE TRANSPARENT LATCH WITH ENABLE	T373T	26
SELECTORS/MULTIPLEXERS		
4-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH STROBE G	T153	12
4-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER	T153G	10
QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH STROBE G	T157	13
QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER	T175G	11
OCTAL 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH STROBE G	T157W	25
OCTAL 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER	T157WG	21
SHIFT REGISTERS		
8-BIT PARALLEL-OUT SERIAL SHIFT REGISTER WITH RESET	T164	55
8-BIT SHIFT REGISTER WITH RESET, LOAD AND ENABLE	T166	65
4-BIT SHIFT REGISTER WITH RESET, LOAD AND ENABLE	T166H	34

Internal Tristates

S-MOS supports the use of internal tristate buses with the following macro library:

Name	Function	Gates
BLT1	Bus Latch	1
BLT4	Quad Bus Latch	2
BLT8	Octal Bus Latch	3
TSB	Tristate Buffer	4
TSV	Tristate Inverting Buffer	5
T240	Octal Inverting Tristate Buffer	30
T240H	Quad Inverting Tristate Buffer	15

Name	Function	Gates
T244	Octal Tristate Buffer	26
T244H	Quad Tristate Buffer	13
T373	Octal Latch with Tristates	50
T373H	Quad Latch with Tristates	25
T374	Octal DFF with Tristates	72
T374H	Quad DFF with Tristates	36

Note: In order to insure design quality, S-MOS Systems requires the use of certain design patterns when using internal tristate cells. Please consult S-MOS Systems for more information(see back page for contact information).

Package Matrix

PACKAGE TYPE	NO. OF PINS	SLA 827S	SLA 847S	SLA 872S	SLA 890S	SLA 8B3S	SLA 8F0S	SLA 8J3S
PLASTIC DIP	28	X	X	X				
	40	X	X	X				
	42	X	X	X				
PLASTIC SHRINK DIP	64	X	X	X	X	X		
PLASTIC FLAT	44	X	X					
FP-2	60	X	X	X	X	X		
FP-5	60	X	X	X				
	80	X	X	X	X	X		
	100	X	X	X	X	X	X	
FP-8	120			X	X	X	X	
	128			X	X	X	X	
	144			X	X	X	X	X
	160				X	X	X	X
FP-9	196					X	X	X
(under development)	230						X	X
PLCC	44	X	X					
	68	X	X	X	X	X		
	84	X	X	X	X	X	X	X
PLASTIC PGA	89	X	X	X				
	132		X	X	X	X	X	
	176				X	X	X	X
	208						X	X
	240							X
CERAMIC PGA	132	X	X	X	X	X	X	X
	176				X	X	X	X
	208						X	X
	240							X

Process Technology

The SLA8000 Series is fabricated on our highly automated 6" fabrication line located in Fujimi, Japan. The process is similar to that used for our high-volume 256K SRAM which has been in production since 1986.

N-channel length is 1.2 micron drawn (0.9 micron effective) and P-channel length is 1.4 micron drawn (1.1 micron effective). M1 width is 1.7um and spacing is 1.8um. M2 width is 2.7um and spacing is 2.1um.

Propagation delay times

The propagation delay values printed in our cell libraries and used in simulation are derived from actual measurements of silicon, not spice simulations. The measured coefficient parameters for V_{DD}=5V +,- 5% and Ta = 0° to 70°C (25°C typical) are:

	MIN	TYP	MAX
Voltage	0.96	1.0	1.07
Temperature	0.93	1.0	1.17
Process	0.88	1.0	1.12
Margin	0.96	1.0	1.05
Actual factor	0.75	1.0	1.50
Additional guardband	0.80	1.0	1.20
Approx. simulation/cell library factor	0.60	1.0	1.80

The additional guardband used by S-MOS virtually guarantees the silicon will meet your simulations.

Propagation delays of selected macros

BEST CASE	WORST CASE
Temperature = 0^0C Ambient	Temperature = 70^0C Ambient
Supply voltage = 5.25 V	Supply voltage = 4.75V
Process = best case	Process = worst case

Name	Function	From	To	Best case		Worst case		Loads
				tplh	tphl	tplh	tphl	
NA2	2-INPUT NAND	IN	OUT	0.1	0.1	0.5	0.5	0
				.19	.22	.77	.84	1
				.28	.32	1.04	1.18	2
NO2	2-INPUT NOR	IN	OUT	0.2	0.1	0.9	0.4	0
				.64	.18	1.34	.63	1
				1.08	.26	1.78	.86	2
IN1	1 X INVERTER	IN	OUT	0.1	0.1	0.4	0.3	0
				1.00	.18	.67	.53	1
				1.9	.26	.94	.76	2
IN4	4 X INVERTER	IN	OUT	0.1	0.1	0.3	0.2	0
				.13	.12	.39	.27	1
				.16	.14	.48	.34	2
DF	D FLIP FLOP	CLK	Q	1.3	1.4	3.7	4.0	0
				1.39	1.48	3.97	4.23	1
				1.48	1.56	4.24	4.46	2
IKB	INPUT CLOCK BUFFER	IN	OUT	2.1	1.4	5.8	3.9	0
				2.3	1.5	6.5	4.5	10
				2.5	1.6	7.2	5.1	20
OB1	2mA OUTPUT DRIVER	IN	PAD	1.68	2.09	4.78	5.80	10pF
				4.0	7.25	11.10	19.80	50pF
				6.9	13.70	19.00	37.30	100pF
OB3	6mA OUTPUT DRIVER	IN	PAD	2.66	2.65	7.34	7.43	10pF
				3.30	4.45	9.10	12.35	50pF
				4.10	6.70	11.30	18.50	100pF

Workstation Support

Schematic capture, electrical rule checking, design rule checking, simulation and timing verification are supported on Daisy, Mentor and Intergraph workstations. In addition, our proprietary LADS software, used with OrCAD or FutureNet, is available for IBM PCs and compatibles.

LADS includes ERC, DRC, logic simulation and timing verification up to 7000 gates in PCs with 640K of memory or up to 20,000 gates in PCs equipped with a ZAIAZ co-processor board.

Standard Cell Migration

The SLA8000 Series can be easily migrated to SSC3000 Series 1.2um standard cells. This is made possible by the identical processing and compatible design tools shared by the two design methodologies. As such, the gate array macro library is a subset of the standard cell macro library.

Megacells

Due to the channelless design of the SLA8000 Series, fully routed and characterized megacells can be implemented effectively along side of random logic. Megacells currently under development include microprocessors, peripheral interface devices and controllers.

RAM And ROM Blocks

RAM and ROM may be implemented efficiently in small-to-medium sizes on chip. The following tables describe the available range and gate counts of popular configurations. When necessary, individual blocks may be combined to create larger sizes. Since RAM and ROM are routed as blocks, their gate count is subtracted from the total available gates in an array, not the usable gate count. The remaining number of usable gates is then recalculated from the remaining available gates.

RAM
Words: 2 to 256
Bits/word: 1 to 32
Max block size: 4096 bits

ROM
Words: 4 to 64
Bits/word: 1 to 8
Max block size: 512 bits

Typical RAM configurations

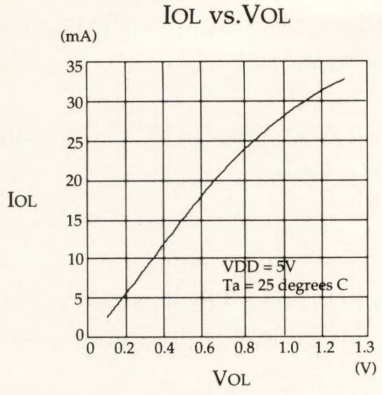
Words	Gates				
	1 Bit	4 Bits	8 Bits	9 Bits	16 Bits
16	177	361	593	651	1,057
32	276	652	1,706	1,182	1,924
64	475	1,159	2,043	2,239	3,659
128	862	2,122	3,802	4,222	7,090
256	1,637	4,049	7,265	8,069	13,697

Typical ROM configurations

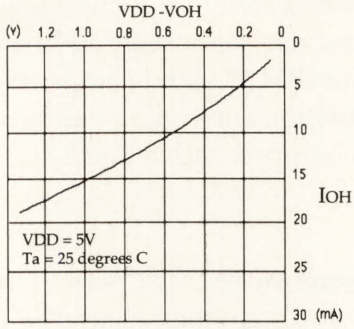
Words	Gates				
	1 Bit	2 Bits	4 Bits	6 Bits	8 Bits
16	38	48	68	88	108
32	74	92	128	164	200
64	134	168	236	304	372

Output Current (Type 2 Output Buffer)

IOL vs. VOL

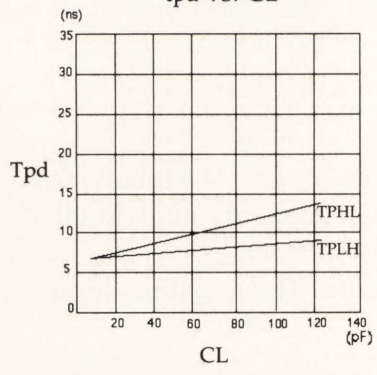


IOH vs. (VDD - VOH)

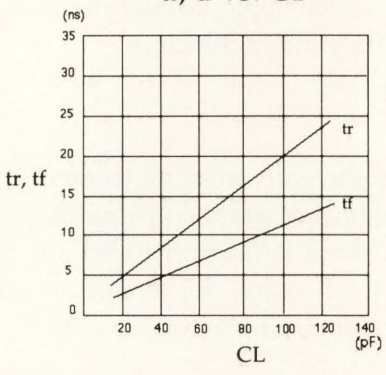


Type 2 Output Buffer Delay Characteristics

tpd vs. CL

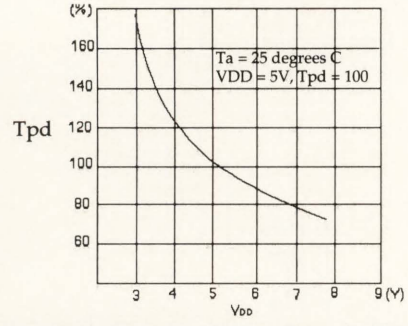


tr, tf vs. CL

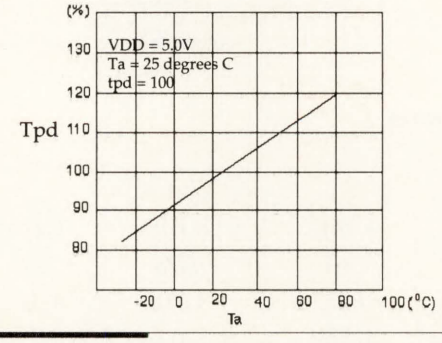


Propagation Delay Characteristics

tpd vs. VDD



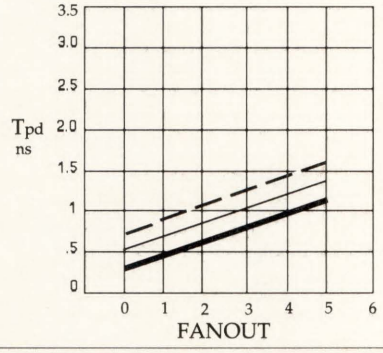
tpd vs. Ta



Propagation Delay Including Interconnect

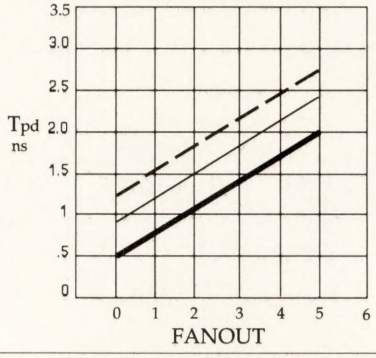
Typical Propagation Delay

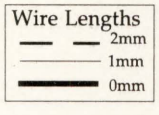
25 degrees C Ambient, 5 volts



Worst Case Propagation Delay

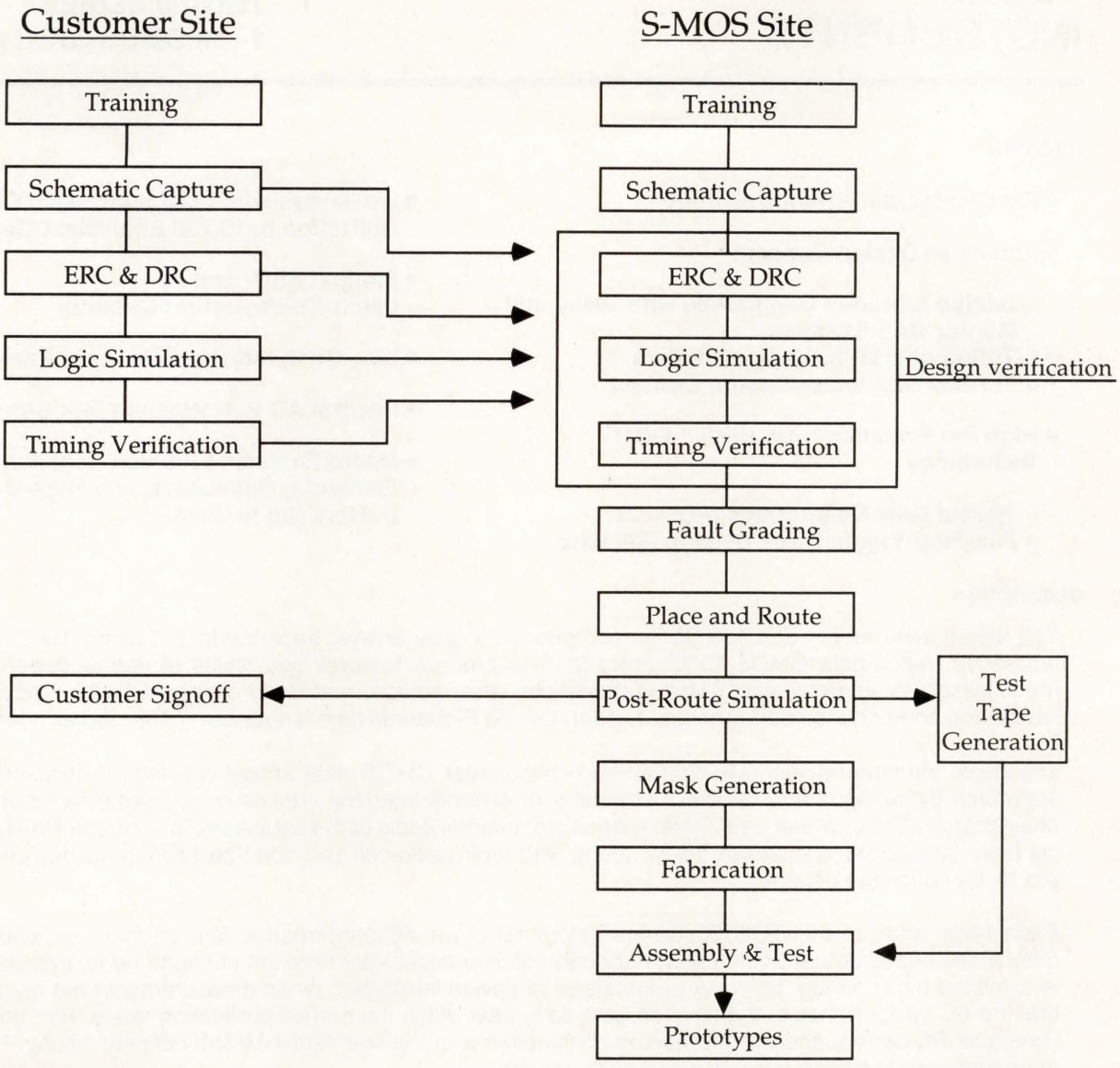
70 degrees C Ambient, 4.75 volts





2-input NAND gate

S-MOS Systems ASIC Design Flow



S-MOS Customer Engineering

In order to help customers implement their designs in S-MOS ASICs, S-MOS offers training at its design centers and at customer sites when required.

When a design is started, an S-MOS engineer is assigned to the project and will remain with the project through its completion. Our engineers will work with the customer on design, software and other technical issues. When the design files are transferred to S-MOS, that same engineer will verify the design's integrity and prepare it for place and route.

S-MOS' Customer Engineering Group provides all technical customer-support services including:

- Pre-sale technical support
- Customer training
- Design assistance
- Workstation support
- Place-and-route
- Software documentation
- Simulation support
- Turnkey designs
- Design verification

S-MOS Systems, Incorporated
2460 North First Street
San Jose, CA 95131-1002
408-922-0200
FAX 408-922-0238

TEXAS INSTRUMENTS

TGC100 SERIES
1-μm CMOS GATE ARRAYS

features

- **Fast Prototype Turnaround Time**
- **Extensive Design Support**
  - **Design Libraries Compatible with Daisy and Mentor CAE Systems**
  - **TI Regional ASIC Design Centers**
  - **TI ASIC Distributor Design Centers**
- **High Performance 1-μm EPIC™ CMOS Technology**
  - **Typical Gate Delay 500ps (FO = 3)**
  - **Flip-Flop Toggle Rates of 95 to 208 MHz**
- **Six Arrays with Maximum Basic Cell Utilization to 16,758 Equivalent Gates**
- **Integral ESD- and Latch-Up-Protection Circuitry**
- **Low-Cost, Industry-Standard Packages**
- **Integral AC Performance Test Structure**
- **Macro Functions Include Register Files, Delay Elements, Oscillators, and High-Drive Output Buffers (up to 20 mA)**

description

The Texas Instruments TGC100 Series comprises six gate arrays, each fabricated using TI's 1-micrometer advanced silicon-gate CMOS EPIC process. The process features two levels of copper-doped-aluminum metallization for interconnect. Silicided polysilicon gate, source, and drain elements further reduce internal resistance and enhance performance. N-channel and P-channel gate lengths are patterned at 1.0 micrometer.

The basic structure of the TGC100 Series 1-micrometer CMOS gate arrays consists of basic-cell columns separated by wiring channels with a perimeter of external interface macros configurable as inputs, outputs, bidirectional I/Os, or power pins. Each 4-transistor internal basic cell is equivalent to a 2-input NAND gate. The six base gate arrays are shown below, along with their basic-cell and bond-pad configurations and standard production package options.

Each base array in the TGC100 Series incorporates an AC-performance test structure embedded in an otherwise unused corner of the array. Although not user-accessible from the I/O bond pads, this test structure is activated by TI during the wafer-probe stage of device fabrication when measurements are made to verify that the AC performance of the finished gate array falls within the normal production range. For most applications, this AC performance verification, in conjunction with the standard 1-MHz functional testing, is sufficient to ensure correct device operation and performance.

library functions

The TGC100 Series gate array library includes basic gate and buffer macros and MSI-level macros. Of the 213 macros offered, 186 are hardwired and 27 are software macros. The hardwired macros provide a broad selection of predesigned, fully characterized functions. The software macros provide popular TTL/CMOS-type MSI functions that can be used as designed or modified at your workstation to suit your design requirements. Additional user-defined software macros can be created using the TGC100 library macros. Library release 2.0 contains the following classes of macros:

- 38 MSI Internal Software Macros
- 74 External Input, Output, and Bidirectional Buffer Macros
- 37 Internal Register, Flip-Flop, and Latch Macros
- 64 SSI Internal Gate and Bus Macros

A complete TGC100 Series Design Kit, available for the Daisy or Mentor CAE systems, includes the following:

- TGC100 Series Data Manual
- CMOS Gate Array Design Manual
- Design Support Software User's Manual
- TGC100 Series Design Library

The Design Kit is arranged to accommodate new material as it is issued.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage†	TTL-compatible inputs	2			V
		CMOS-compatible inputs	$0.7V_{CC}$			V
V_{IL}	Low-level input voltage†	TTL-compatible inputs			0.8	V
		CMOS-compatible inputs			$0.2V_{CC}$	V
V_I	Input voltage†		0		V_{CC}	V
t_t	Input transition (rise and fall times)†		0		100	ns
V_O	Output voltage‡		0		V_{CC}	V
I_{OH}	High-level output current‡		As specified on data sheets			mA
I_{OL}	Low-level output current‡					
T_A	Operating temperature range		0		70	°C

† Applies for external input and bidirectional input buffers.

‡ Applies for external bidirectional and output buffers.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
I_{CC} Supply Current	TGC103	$V_I = V_{CC}$ or 0 (See Note below)		350	μA
	TGC105			550	
	TGC108			850	
	TGC112			See macro data sheets	
	TGC115			See macro data sheets	
	TGC118			See macro data sheets	

Note: For external inputs and bidirectional I/O buffers with pullup source $V_I = V_{CC}$ and for external inputs and bidirectional I/O buffers with pulldown source $V_I = 0$.

The remaining electrical and switching characteristics are specified on the individual macro data sheets.

mechanical data

Production quantities of the TGC100 family of fast prototype gate array designs are available in the industry-standard plastic packages shown below.

ARRAY ORGANIZATIONS AND PACKAGES

GATE ARRAY TYPE	BASIC CELLS		TOTAL BOND PADS	PACKAGE SELECTION												
				DIP		PLCC				QFP			PPGA			
	TOTAL AVAILABLE	MAXIMUM USABLE		28 PIN	40 PIN	28 PIN	44 PIN	68 PIN	84 PIN	120 PIN	132 PIN	160 PIN	120 PIN	144 PIN	180 PIN	208 PIN
TGC103	3,200	2,880	84	X	X	X	X	X	X							
TGC105	5,376	4,838	118	X	X		X	X	X							
TGC108	8,896	8,006	142	X	X		X	X	X							
TGC112	12,654	11,389	196						X	X	X	X	X	X	X	X
TGC115	15,580	14,022	216							X	X	X		X	X	X
TGC118	18,620	16,758	216							X	X	X		X	X	X

♦ Prototypes are supplied in a socket/footprint-compatible ceramic package.

military applications

TI also offers gate array designs processed in compliance with MIL-STD-883, Method 5004/5005 or Method 5010. Production facilities are fully DESC and JAN certified.

FOR MORE INFORMATION ON THE TGC100 SERIES, PLEASE WRITE:

Texas Instruments Incorporated
Department SRY113VG8
Dallas, Texas 75380-9066

TEXAS INSTRUMENTS

TEXAS INSTRUMENTS

TSC500 SERIES
1-μm CMOS STANDARD CELLS

features

- **High-Performance 1-μm EPIC™ CMOS Technology**
  - **Typical Gate Delay 490ps (FO = 3)**
  - **Flip-Flop Toggle Rates to 185 MHz**
- **Extensive Design Library (>350 Elements)**
  - **SSI, MSI, and I/O Functions**
  - **LSI/VLSI MegaModule™ Building Blocks**
- **Through-Hole/Surface-Mount Packaging Offering (DIP/SOIC/PLCC/PGA/QFP)**
- **User-Configurable High-Density SRAM**
- **Extensive Design Support**
  - **Design Libraries Compatible with Daisy and Mentor CAE Systems**
  - **TI Regional ASIC Design Centers**
  - **Comprehensive Design Kit Support**
- **Specified Over Full Commercial and Military Temperature Range**

description

The Texas Instruments TSC500 Series comprises an extensive offering of SSI, MSI, and I/O functions and a growing library of LSI/VLSI building blocks, each fabricated using TI's 1-micrometer advanced silicon-gate CMOS EPIC process. The process features two levels of copper-doped-aluminum metallization for interconnect. Silicided polysilicon gate, source, and drain elements further reduce internal resistance and enhance performance. N-channel and P-channel gate lengths are patterned at 1.0 micrometer.

library functions

The TSC500 Series cell library includes basic gate, buffer, and MSI-level macros. Of the 426 cells offered, 376 are hardwired and 50 are software macros. The hardwired macros provide a broad selection of predesigned, fully characterized functions. The software macros provide popular TTL/CMOS-type MSI functions that can be used as designed or modified at your workstation to suit your design requirements. Additional user-defined software macros can be created using the TSC500 Series library. Library release 1.0 contains the following classes of macros:

- 50 Internal MSI Software Macros
- 23 Internal MSI Scan Flip-Flops/Latches, Delay Elements, and Oscillator Macros
- 166 External Input, Output, and Bidirectional Buffer Cells
- 46 Internal Register, Flip-Flop, Counter, and Latch Macros
- 156 Internal SSI Gate, Bus Buffers, and Input/Output Terminators
- 22 Memory Functions (SRAM, FIFO, Register File)

A complete TSC500 Series Design Kit, available for the Daisy and Mentor CAE systems, includes the following:

- TSC500 Series Data Manual
- CMOS Standard Cell Design Manual
- Design Support Software User's Manual
- TSC500 Series Design Library

The Design Kit is arranged to accommodate new material as it is issued.

STANDARD-CELL PACKAGE OPTIONS															
Type	Number of Pins														
	16	20	24	28	40	44	48	68	84	100	120	132	144	180	208
DIP	C	C	C	C/M	C/M		C/M								
SOIC	C														
LCC				C/M		C/M		C/M	C/M						
QFP										C/M	C	M			
PGA								M	M	C/M	C/M	C/M	C/M	C/M	M

C = Commercial M = Military

military applications

TI also offers standard-cell designs processed in compliance with MIL-STD-883, Method 5004/5005 or Method 5010. Production facilities are fully DESC and JAN certified.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage†	TTL-compatible inputs	2			V
		CMOS-compatible inputs	$0.7V_{CC}$			V
V_{IL}	Low-level input voltage†	TTL-compatible inputs			0.8	V
		CMOS-compatible inputs			$0.2V_{CC}$	V
V_I	Input voltage†		0		V_{CC}	V
t_t	Input transition (rise and fall times)†		0		100	ns
V_O	Output voltage‡		0		V_{CC}	V
I_{OH}	High-level output current‡		As specified on data sheets			mA
I_{OL}	Low-level output current‡					
T_A	Operating temperature range	Military	−55		125	°C
		Commercial	0		70	°C

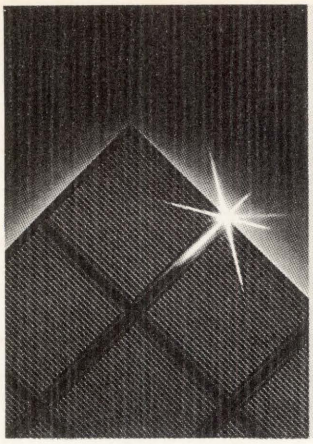
† Applies for external input and bidirectional input buffers.

‡ Applies for external bidirectional and output buffers.

FOR MORE INFORMATION ON THE TSC500 SERIES, PLEASE WRITE:

Texas Instruments Incorporated
Department SRY103VG8
Dallas, Texas 75380-9066

TEXAS INSTRUMENTS



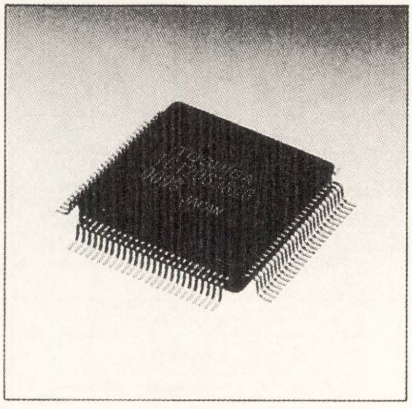
TOSHIBA

CMOS ASIC
New Product Release
TC120G SERIES GATE ARRAY

Toshiba Corporation has introduced a series of gate arrays that use a 1.0-micron CMOS process to reduce gate delays by 35%. Applications include consolidating high-speed circuits into a single package, especially in high-performance systems.

Toshiba will be accepting designs starting in April of this year.

1-Micron Process Cuts Delays of Toshiba Gate Arrays by 35%

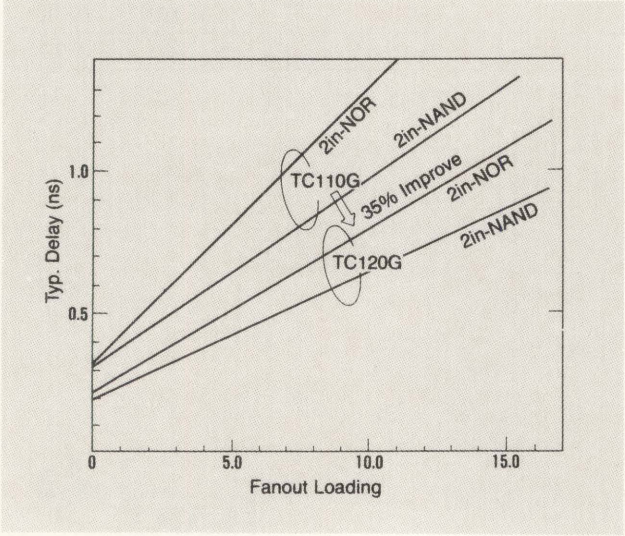


The TC120G Series, which offers typical gate delays of 400 picoseconds, (note 1), is currently available in 5 master array sizes, with gate complexities ranging from 37,392 to 129,042 raw gates. By applying a variable channel width architecture, the devices use all of the area available on a silicon die, instead of grouping gates in areas separated by wire-routing tracks. As a result, silicon utilization is improved.

The TC120G is compatible with Toshiba's TC110G Series Arrays, which use a 1.5-micron CMOS process. The TC110G Series is available in 14 master arrays, from 3,498 to 129,042 raw gates.

Both TC120G and TC110G Series are supported by compatible computer aided design (CAD) tools. Toshiba's VL-CAD system has been designed for easy migration of TC110G designs to the TC120G technology.

Performance Advantage of TC120G over TC110G



Product Specifications

	TC120G series
Process technology	HC²MOS Si-gate double layer metal
	1.0μm
Gate speed (inner gate, typ.)	0.4ns
Maximum toggle frequency	200MHz
Supply voltage	5V
Application	ECL

TC120G Series Gate Arrays

	Raw Gates	Usable[2] Gates	Pads[3]	I/Os[4]
TC120GC9	129,042	~50,000	368	256
TC120GA0	100,182	~40,000	326	256
TC120G75	74,970	~30,000	282	256
TC120G51	50,904	~20,000	234	226
TC120G38	37,932	~15,000	204	196

Notes: 1) 2 input NAND Gate with a fanout of 2 and 2mm of interconnect metal.
2) Assuming 40% gate utilization.
3) Additional I/O pads may be configured as V_{DD}/V_{SS}.
4) Tester limitation (256 maximum I/O signals)

New Product Release
TC120G SERIES GATE ARRAY

Toshiba Original CAD System for ASIC's

VL-CAD contains layout software tools which were jointly developed by Toshiba and Tangent Systems Corporation, and are being applied to both TC110G and TC120G Series Gate Arrays.

VL-CAD Features

- Integrated Hierarchical Design System
- Logic Simulator (VL-CAD) + Layout (TLAY)*
- Toshiba ASIC Families (Gate Arrays, Standard Cells and Super Integrations)
- Maximum Circuit Size 60K Gates
- Compatible Languages (TDL, TSTL)
- Workstation Interface Capabilities

*Jointly developed by Toshiba and Tangent Systems Corporation.

TC110G and 120G Series Library

Macrocells
- TC17G Series Compatible
- Performance Optimization (Standard/High Drive)

Macro Functions
- Equivalent to 74xx Series

Metal Configurable Memory
- Single/Triple Port RAM (Max. 4.5K)
- ROM (Max. 16K)

Logic/Arithmetic Cells
- ALU, CLA, MPY, Barrel Shifter, FIFO

2900 Bit Slice Compatible Cells

CPU Peripheral Cells

Package Selections

As of Mar. 1988

Package		Part Number	TC120G 38	TC120G 51	TC120G 75	TC120G A0	TC120G C9
PGA		64	A	A			
		68	A	A			
		84	A	A			
		100	A	A			
		120	A	A			
		135	A	A			
		144	A	A			
		180	A	A			
		224		A			
Cavity Down PGA		95	P	P	P		
		155	P	P	P	P	P
		223	D	D	D	D	D
		299				D	D
PLCC		44					
		68	D	P			
		84	D	P			
PFP	Square	μ44					
		44					
		60					
		100A[1)]					
		100[1)]	D	D			
		144	D	D			
		184		P			
	Rectangular	64					
		80					
		100					
CFP		100[1)]	A	A			
		144	A	A	P	P	P
		184		P	P	P	P

A: Adaptable,
D: Check with Toshiba for availability (Under development)
P: Check with Toshiba for availability (Under planning)

Notes: 1) Flat Package 100 pin is classified into 2 types determined by number of inner leads available: 100A—84 inner leads. 100—100 inner leads.
2) Please refer to "Package Selector Guide" (Document I.D. SEMI-E-S 1001) for further information in detail.

Design and specifications are subject to change without notice.

TOSHIBA
TOSHIBA AMERICA, INC.

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(408) 733-3223

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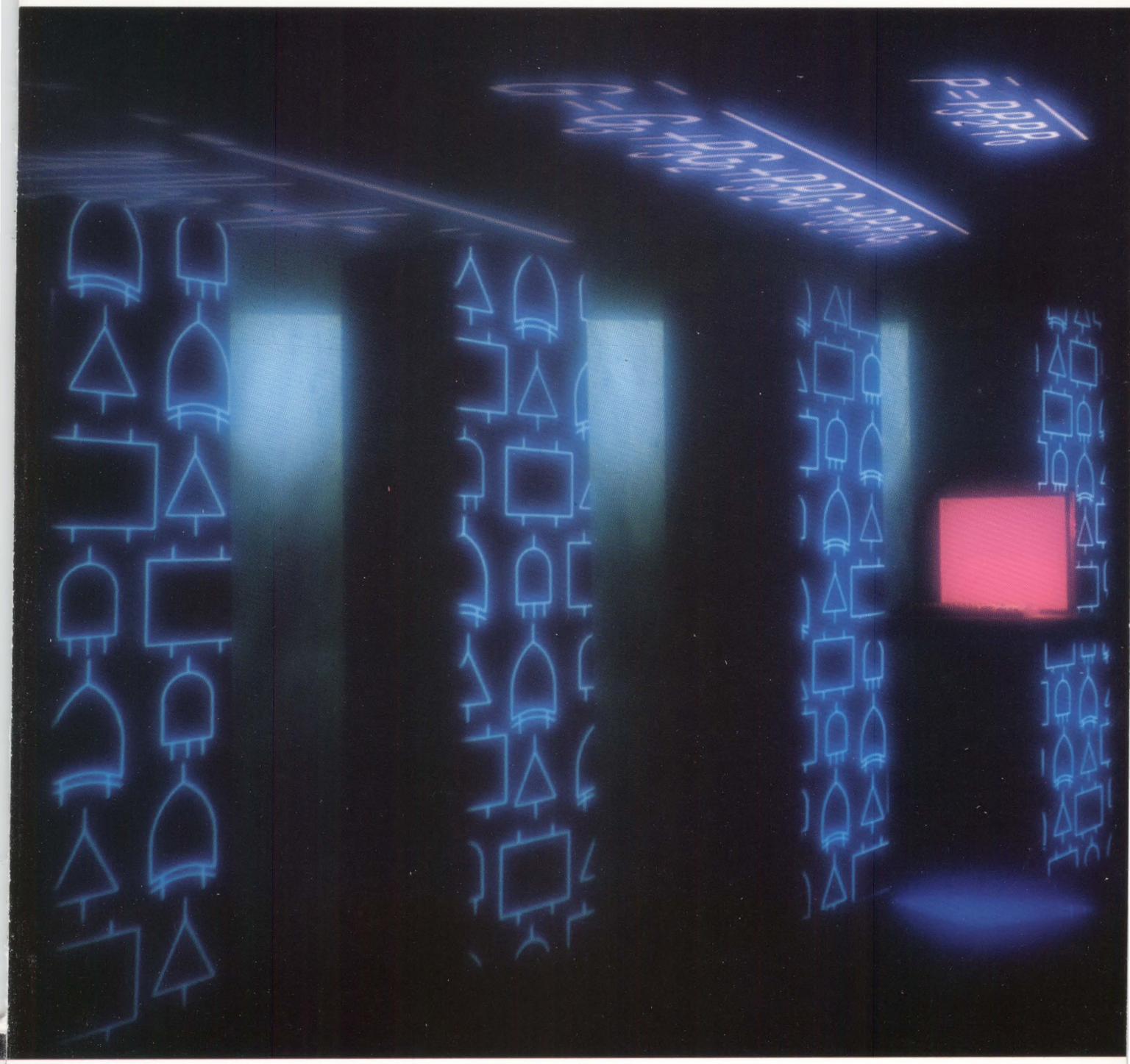
For additional information on the Knowledge-based Engineering Environment, call the NCR Hotline **1-800-334-5454**. Or write, NCR Microelectronics, 2001 Danfield Court, Ft. Collins, CO 80525.

Engineering Environment.™



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