# MULT-USER OPERATING SYSTEMS 

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## and more

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## the CP/M* and S-100 user's journal MHROSYSIEMS

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## Called "MP/M II ${ }^{\text {TM }}$ "

MP/M II, the multiuser extension of our CP/M operating system, answers the lucrative business community demand for small scale distributed processing. Smart OEM's, language companies and application programmers are enthusiastically extending their offerings to satisfy this "new" market.

## MP/M II Features

Record locking and file
locking ensure data base validity when multiple users access the same data.
With 32 megabyte file capacity, you can daisy-chain 16 state-of-the-art disk drives, at 512 megabytes each. This gives you on-line storage of 8 gigabytes!
Fast performance is a certainty. Dispatch time between users requires as little as 600 microseconds.
Encrypted passwords provide security for user files and directories.
Time and date stamps indicate your last update of an application file and either last access or file creation.

Additional features provide increased performance with exceptionally low system overhead through streamlined housekeeping plus 30 refined utilities. 400 K bytes of RAM are supported. And MP/M II is upward compatible with CP/M.

## Substantial

 Capabilities IncludedMajor utilities in the MP/M II package include our RMAC ${ }^{\text {m }}$ assembler, LINK-80, ${ }^{\text {m }}$ LIB- $80^{\text {m }}$ run time library manager, and RDT ${ }^{\text {TM }}$ debugger.

Network capability: Your product's growth to CP/NET ${ }^{\text {m }}$ is provided in MP/M II.


## To Language \&

 Application Companies:You're seizing the timeperishable market advantages of MP/M II. Its five manuals help extend your products to multiuser status, with accuracy and speed. LINK-80's overlay facilities help produce a higher quality. LINK-80, RMAC and RDT are powerful development aidswhich don't cost you a thing.

## Compatible software

 accelerates your entry into the multiuser market. Most programs running under $\mathrm{CP} / \mathrm{M}$ will run under MP/M II with little or no modification. Couple that with a built-in growth path, and you're protecting the future of your business with MP/M II.

# Extend CP/M to Multiuser Systems: Extend Your Profits 

## To Hardware OEM's: <br> The profitable impact

of multiuser contigurations is profound. Compare your sum-of-the-boxes pricing: Multiuser vs. single user. No question about it. Your next move will be to re-forecast sales quotas and profit margins. MP/M II is the key. With the market demand you read about, the act of extending your systems to MP/M II will bear handsome rewards. Your next step is equally clear. Have our marketing group expedite the MP/M II data sheet, OEM price list and contract. Here's an even more positive approach. Why not call our marketing group as your first priority?

These 14 companies are extending 24 languages to run under MP/M II:
Compiler Systems, Inc.
Control-C Software, Inc.

## Digital Research

Ellis Computing
Laboratory Microsystems
Micro-Ap
Micro Focus, Inc.
Microsoft
MT Microsystems, Inc.
Ryan-McFarland Corp.
Sorcim Corporation
SuperSoft Associates
Tarbell Electronics Timin Engineering Co.

## To Dealers, Distributors, System Houses:

It takes less effort to make more money by selling multiuser systems. Selling an upgrade path is easier than moving dead end, dedicated systems. MP/M II means hard disks, multiple printers and terminals -add-ons right through full networking environments. One sale can truly generate cash for an extended period. So call your OEM for delivery of MP/M II based systems.

Every new market has its share of easy sales. For a while, somebody will take those orders hand over fist. Your share of that business will probably depend on a single factor: Your ability to get product first.

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Over 250,000 microcom-
puters use our operating systems. Over 300 OEM's and 400 independent software vendors (ISV's) use our products as the basis of thousands of applications. These are listed in our CP/M Compatible Catalog. Over 25,000 copies, per edition, generate ISV's sales. FORUM, published quarterly, and ISV seminars provide technical


## Multiuser Demand

Multiuser demand is more than a trend. The MP/M II market is a fact of business life. It elevates the microcomputer with larger scale capabilities, and a larger dollar/sale market base. You only get one chance to make a good first (market) impression. Now is the time. We're here to help. Call (408) 649-3896, or write: Digital Research, P.O. Box 579, Pacific Grove, CA 93950. Europe: Vector, Intl., Leuven, Belgium, 32(16)202496 Far East: Microsoftware Assoc. Tokyo, Japan, 03-403-2120



EDITOR'S PAGE

In my column in the November/ December 1981 issue of Microsystems, the following appeared:

As editor of Microsystems, I have on a few occasions rejected an article that I really would have liked to publish. The problem was that the article included source code that would have taken up an entire issue, and sometimes more than an entire issue. It was with deep regret that I rejected these articles.

Although the magazine has nearly doubled in size from the first issue published less than two years ago, editorial space in the magazine is still at a premium. We have only a certain number of pages allocated in each issue for articles.

Therefore, I am seriously considering omitting source code listings from the magazine when such listings are more than two or three pages long. Instead we would refer the reader to the author to obtain the source code on disk. After all, who really wants to key in a lot of code with its attendant entry problems? Personally, I certainly would be willing to pay a reasonable sum to save the time and entry problems. Also it would free up editorial space in the magazine so that we could include more articles.

Before making such a radical change, I would like to hear from Microsystems readers and authors. Are you in favor, or opposed to the change? What do you feel is a reasonable charge for the source code? Please let me hear from you.
I received almost fifty responses from readers. It is indeed gratifying to see that so many people feel strongly
enough about it to sit down and write to me. I wish to thank them all. I regret that we do not have the space to print the letters in the magazine. All were most complimentary about the magazine, and about 70\% of the writers indicated that they were in favor of dropping lengthy source listings from the magazine. Of the $30 \%$ who were not in favor, most seemed to be either foreign subscribers or subscribers with non-standard disk systems.

Several subscribers suggested making the programs available on the CompuServe MicroNET, via the database of the CP/M Special Interest Group (CPMIG). I must confess that although I have been aware of this service for some time, I have never tried it. With all the free RIBBS and ARPANET facilities available to me, I trust that Microsystems' readers will excuse the oversight. I do intend to investigate the CompuServe CPMIG at the earliest opportunity.

Hence, we will continue to publish shorter listings as well as listings we judge to have broad interest. All authors of software, both published and not, will be encouraged to place their software into the SIG/M public domain software library. I have selected SIG/M because I feel that it has the widest distribution; its volumes are being distributed by over a hundred clubs, CPMUG and about a dozen RIBBS systems. I am also sure that someone will copy the SIG/M volumes to CompuServe, if this is not already being done. Furthermore, SIG/M does make their software available, on special order, for such non-standard disk formats as: TRS-80 I-III, Micropolis 5-1/4", NorthStar and Apple II. I will also ask each
author to make source code printouts and disk copies available at a nominal charge.

I feel that this decision will work to the advantage of all our readers.

## Articles Wanted

We are seeking articles on the following topics for inclusion in Microsystems during the second half of this year. If you would like to discuss such an article with me, feel free to call me any evening or weekend at (201)5229347, or send the article to me at: Box 1192, Mountainside, NJ 07092. We have a free author's guide available.

- Reviews of Unix-like micro operating system packages for $\mathrm{CP} / \mathrm{M}$ systems.
- Reviews of CP/M system development languages for micros (e.g., Ada, C, Pascal, etc.).
- Local network implementations on MP/M and S-100 systems.
- Interfacing CP/M and S-100 systems to the IEEE-488 bus, LSI-11 bus, etc.
- S-100 construction articles (e.g., 16-bit CPU, etc.).


## Microsystems Show Schedule

Microsystems is represented at most major consumer and trade shows. We saw many of you at the Consumer Electronics Show in Las Vegas and the Which Computer Show in Birmingham, England earlier this year. Coming up, we'll be at the West Coast Computer Faire, San Francisco, March 19-21; Trenton Computer Festival, April 17, 18; National Computer Conference, June 7-10, Houston and the Consumer Electronics Show, June 6-9, Chicago. See you there!

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ADA is a trademark of the U.S. Department of Defense
by Sol Libes

## Trenton Computer Festival Here Again

On Saturday and Sunday, April 17 and 18th, several thousand computer hobbyists will gather at Trenton State College, Trenton, New Jersey for the 7th annual Trenton Computer Festival (TCF). TCF has the largest personal computer flea market in the country. Last year it covered an outdoor area of about seven acres, and over 6,000 hobbyists flocked from all across the United States to the event. Sellers lined up for the choice spots in the wee hours of the morning, long before the gates opened. The outdoor flea market featured everything from complete computer systems to tiny electronic parts... from used TRS-80, S-100 and Apple computers to disk drives and hard-tofind parts.
TCF also features an indoor commercial exhibitor area with ninety booths, and speaker and user group sessions.
TCF is operated by the Amateur Computer Group of New Jersey, the Philadelphia Area Computer Society and the Trenton State Computer Society. The funds raised help support these nonprofit organizations and their activities. For information call (609)7712487, or write TCF-82, Trenton State College, Trenton, NJ 08625.

## How Many S-100 Systems Are There?

The January 1982 issue of Interface Age contained an interesting article on business systems. Of special interest
was a list of 116 business-oriented microcomputers. Forty of the systems use the S-100 bus, six use multibus, 56 use proprietary buses, three use the SS-50 bus, eleven use no system bus and one uses the DEC Q-bus.
Another notable feature of the article was a listing of systems shipped. The article listed the following S-100 manufacturers and units shipped:

Archives Inc.
1,500
California Computer Systems 500
Compa
700+
Dynabyte
Exidy Systems Inc.
4,500+
Findex
IMS International
15,000

Ithaca InterSystems
900
,000
Micromation Inc.
2,000
North Star Computers Inc.
1,000
Polymorphic Systems
8,000
TEI Inc.
2,500+
The total is 69,000 systems. This list does not include several of the largest manufacturers of S-100 systems (e.g., Cromemco, Vector Graphic, Systems Group, Godbout Electronics, Morrow Designs, MicroDaSys, AlphaMicro, Lomas Data Products, Seattle Computer, Tarbell Electronics, Tecmar, Dual Systems, Quasar Data Products, etc.).

Further, when one adds to the list the S-100 systems in operation one must include MITS, Imsai, TDL, Processor Technology and the many other smaller S-100 manufacturers who are no longer with us. It therefore seems reasonable to estimate that there are now well over 300,000 S-100 systems
in operation and that $40-50,000 \mathrm{~S}-100$ systems are being sold annually.

## CP/M-86 Goes Into Silicon

Intel has announced that it will soon provide a silicon version of the CP/M86 operating system. The IC will operate with both the 8086 and 8088 , and allow diskless operation, making it ideal for remote computers interconnected in a local distributed network sharing a large-capacity disk drive. The device is a 16 K ROM plus timers and other logic, and will bear the part number 8086-E3. It should be available by midyear.

In another development, Intel announced that it has signed OEM distribution agreements with Digital Research to provide custom versions of CP/M and MP/M for Intel's boards and systems.

## SIG/M \& CPMUG News

The SIG/M group has announced the release of twelve more volumes of public domain CP/M software bringing the total number of volumes up to 55. SIG/M has also released a printed 12page catalog listing all of the software in their library and a listing of the SIG/M distribution points. The Catalog is $\$ 1.50$ (U.S. first class) or $\$ 2.00$ (foreign air mail; checks must be made in U.S. funds drawn on U.S. bank). Write: SIG/M, Box 97, Iselin, NJ 08830.

The CPMUG group has announced the release of ten more volumes of software, bringing their total up to 75 volumes. However, it should be noted

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## News \& Views, continued...

that their volumes 55 through 75 are reissues of the old SIG/M volumes 1 through 20. Hence, it you already have the SIG/M disks then you also have the CPMUG volumes 55-75. CPMUG is distributing the SIG/M disks in order to give them wider distribution. Unfortunately, CPMUG has put their own volume numbers on the disks, and has not clearly identified that they are the same as the original SIG/M disks.

## Cromemco Releases 68000 Products

Cromemco Inc., of Mountain View CA, will soon start shipping its 68000 products which I first announced in the Sep/Oct 1981 issue of Microsystems There are three S-100 boards: The DPU dual processor board containing both 68000 and Z80 microprocessors (\$995), the MCU memory controller board ( $\$ 495$ ) and the 256MSU 256K RAM board (\$1995). A 512K RAM card is in the works.

The DPU can execute $\mathbf{Z 8 0}$ and 68000 instructions interchangeably, so that until a meaningful supply of 68000 software is available you can run $\mathrm{Z80}$ software. Each CMU can serve as a memory manager for up to eight RAM cards. The 256MSU uses dynamic RAM chips and includes error detection, correction and logging capability that is transparent to the user. The user can consult a file to determine which RAM chips might be a little "soft" and need replacement.

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Signature

## LETTERS

 TO THE EDITORDMA Operations With SD Systems? Dear Editor:
I certainly have enjoyed Microsystems since the first issue. Thanks for starting a magazine for the $\mathrm{S}-100$ user.

I have a few questions to ask you - I hope you can help me with them.
I have a complete SD Systems set-up, consisting of the SBC200, Expandoram II, Versafloppy II, and VDB8024. I use the SDDS control program and SD Systems DDBIOS Prom. My problem is that while the SD Systems literature indicates that DMA operation is supported, the SDOS or the BIOS doesn't implement it.
Can you tell me of any source of information available and/or software support that would allow me to implement DMA using these boards?
I also have a suggestion for three articles I feel would be appropriate for Microsystems readers like myself. (l am a home computer enthusiast.)

1. An article on SDOS similar to those Microsystems often runs on CP/M.
2. An article on implementing DMA using the SD Systems boards and SDOS as above (if it can be done).
3. Finally, an article on how to use the Godbout CPU-Z to replace an existing Z-80 board, so as to be able to address more than 64 K of memory. This article would explain the programming techniques required to use the extended 24 -bit addresses, and how to combine existing memory with additional memory for more than 64 K .
Thank you for any information you may be able to provide me.
R.W. Watts

18738 LeMarsh St.
Northridge, CA
Dear Robert: I do not own any SD Sales products and have not really had any contact with them. However, it has become apparent
from letters and conversations that I have had from owners of SDS equipment that SDS has gone their own way. They do not appear to be interested in complying with the IEEE-696/S-100 standard nor interfacing their versafloppy disk controller to CP/M. Hence, purchasers of their equipment should be warned that there is a likelihood that they will encounter problems when using SD equipment with other S-100 products. It should be pointed out that the SIG/M library contains some versafloppy driver software. Further, we would be interested in publishing an article or two on coping with SDS interfacing problems. -Editor.

## Information On Jade Big-Z CPU Card

## Dear Editor:

I notice that you are planning language issues. Languages are important, but Microsystems could well leave them to Byte and concentrate on S-100/CP/M with more hardware articles. Don't emulate Byte, except in volume!
I have a Jade Big-Z cpu board which I can't get to operate properly. The symptoms are that on RESET it displays the initial message of my 2708 monitor, and then takes off into the unknown. It will occasionally go into the monitor properly, functioning properly until another RESET. It seems to be connected with JP(ix) with which the print routine ends. Do you know anyone who has had trouble with this board with whom I might correspond? Incidentally, the monitor itself might be of interest to Microsystems at a later date. The Big-Z board was bought "assembled and tested" but has never worked; initially it was found to have an i.c. with a bent-under pin and did not work at all. It now goes occasionally. Letters to Jade have produced no reply as of yet. I would appreciate feedback from any Micro-
systems' readers who could shed some light on this problem.
P.F. Ridler

Professor/Computer Science
University of Zimbabue
P.O. Box M.P. 167

Mount Pleasant
Salisbury, Zimbabue

## More Coverage Of Disk-Related Problems Dear Editor:

I own a Dynabyte DB8/2 (quad 5") and have been using it for about two years, mostly for word processing (Word Star) and keyword retrieval (Information Master, Island Cybernetics). Recently, I bought Microsoft Basic and finally am beginning to learn it, but still am a member of a minority group, understanding little about computers or language but using my own micro (I was one of the people noted in the recent Writers Digest pieces, dealing with the uses of micros for writing).
What I would like to see is a piece in your journal about disc drives, diskettes and errors; I am certain it would become a much sought about piece and be reprinted. I would like to know about the problems generated within drives and by various kinds of external things, e.g., whether poorly handled diskettes can not only give error messages but transmit them, how to analyze and deal with sources of errors. Something with charts would be much appreciated. Such a piece could probably become an expanded separate publication. Most people I have spoken to around here have had inscrutable problems with this area.
Another disk related problem deals with how individuals with, for example, 5 " quad densities can use software available on other types.
Ben Singer
London, Canada


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source programs so it will have to use parameter substitution as follows:

$$
\begin{array}{ll}
\text { F80 }=\$ 1 & \text { \# compile source program } \\
\text { L80 } \$ 1, \text { FORLIB/S, } \$ 1 / \mathrm{N} / \mathrm{E} \# \text { link object modules }
\end{array}
$$

The dollar-sign (\$) is a signal to SUBMIT that a formal parameter is being specified. Here we use one formal parameter, $\$ 1$. The formal parameters are replaced by values at the time SUBMIT is executed. If "N" parameters are used in a given SUBMIT file, then execution proceeds as follows:

SUBMIT SUB-FILE P1 P2 P3 ... PN
where $\mathrm{P} 1 \ldots \mathrm{PN}$ replace the formal parameters $\$ 1$... $\$ \mathrm{~N}$. Therefore, if the above Fortran batch process is in a file FORT.SUB, we could compile and link the Fortran program TEST.FOR as follows:

SUBMIT FORT TEST
Here the formal parameter \$1 is replaced by TEST, and the actual SUBMIT job run is:

```
F80 =TEST
# compile source program
L80 TEST,FORLIB/S,TEST/N/E # link object modules
```

Finally, to place a literal "\$" character in a SUBMIT file, the sequence $\$ \$$ is used.

## Control Characters

It is sometimes necessary to have control characters on command lines within a SUBMIT file. SUBMIT recognizes this need by performing substitutions of the form * $<\mathrm{CHAR}>$ by the control character represent by this two letter ASCII sequence.
In my version of CP/M 2.2 (for Micropolis, by Lifeboat Associates), the SUBMIT program has a bug which made it impossible to use the control character replacement feature. For some reason, this version expected a lower case character instead of an upper case character when specifying the sequence ${ }^{*}<\mathrm{CHAR}>$. This is corrected by changing location 442 H of a memory image from 61 H to 41 H using DDT or a similar facility (e.g., ZDM). Since SUBMIT is a standard feature of CP/M, the bug may well be present in other CP/M 2.2 distributions as well.

## Use Of The 'Zero Program'

In some instances, batch processes will include repetitious execution of the same transient command (e.g., PIP). In cases where these transients are re-executable, the zero program technique may be employed to save disk access time. The zero program is a null length .COM file which allows the previously run program to be run again. The concept of the zero program was introduced in my article "GO: A Utility Program Under CP/M" (Dr. Dobb's Journal \#41) and is also described in the CP/M Bus column found in Microsystems, Vol. 2, No. 2. It should be noted that some programs do not re-execute correctly. However, standard utilities including PIP do work correctly when re-executed. Thus, we could imagine performing several copy operations within a batch process as follows:

```
: PIP.SUB 11/81
PIP B:=A:*.ASM # copy all .ASM files
@ B:=A:*.BAS # copy all.BAS files (@.COM is the
@ A:=C:123*.* # copy some files from C: to A:
STAT A: # status of A: drive
@ B: # and B: drive
```


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## CP/M Bus, continued...

While STAT 1.4 works correctly when re-executed, the STAT usr: feature of STAT 2.x does not work correctly upon re-execution. This is only a minor inconvenience.

## Comments In SUBMIT Files

Comments are possible in SUBMIT files and are often useful for the sake of documentation. Both the semicolon and colon characters initiate comments. However, as described by D. E. Cortesi in "Doctor Dobb's Clinic" (Dr. Dobb's Journal \#57, p. 40), Digital Research supports the colon (:) character as the legitimate comment delimiter. Comments are used in several of the examples presented in this column. Here is an additional example:

```
: file: DIR.SUB created 11/81
: purpose: list directory of current
: disk. List all .COM, .REL, .OVR files
: present
DIR *.COM : list command files
DIR *.REL : list relocatable object modules
DIR *.OVR : list overlay files
: done
```

Some commands will tolerate comments at the end of their command line (e.g., DIR). However, it is generally best to keep comments on separate lines. Note also that comments delimited by "\#" characters in various examples are strictly explanatory and would not actually be included in a SUBMIT file.

## Chaining SUBMIT Jobs

SUBMIT jobs may be chained in a limited fashion. The last command of any SUBMIT job may be another SUBMIT specification. Such an operation would be done as follows:

## SUBMIT NEW-JOB \# submit operations

(PARAMETER-LIST> \# new submit job
Note that SUBMIT deletes any current \$\$\$.SUB, so SUBMIT jobs may not be nested but only chained as shown here. The public domain program, Supersub, which will be discussed in the next issue, allows chaining of SUBMIT jobs.

## The XSUB Facility

It is often necessary to run interactive programs in a batch processing environment. This is not easily done with CP/M 1.4 and its predecessors. However, CP/M2 provides a new utility, called XSUB, which makes this possible to some extent. XSUB is applicable to programs which use the BDOS function 10 (line input) for their input operations. When used, it will take input from the SUBMIT file instead of the console as is normally done. Imagine that we have the following SUBMIT file:

```
: file : Enter EDIT.SUB
```

```
: enter line of input to the file $l
```

: enter line of input to the file \$l
XSUB : provide for input re-direction
XSUB : provide for input re-direction
ED \$1 \# edit file
ED \$1 \# edit file
I\$2 \# insert second argument into
I\$2 \# insert second argument into

# \#file

# \#file

E \# ed exit command...
E \# ed exit command...
:\mp@code{done}
:\mp@code{done}

# etc.

```
# etc.
```

The XSUB at the beginning alters the SUBMIT environment so that subsequent calls to BDOS function 10 will be provided with input directly from EDIT.SUB.

## Conclusion

In this installment, we have discussed the features of the SUBMIT utility program. With proper use of SUBMIT, powerful and convenient batch processing may be performed in the CP/M environment.

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# Software Product Review 

## A Look At MP/M-80 II

by Kelly Smith

## Getting It Going

Having already "brought-up" MP/M versions 1.0 and 1.1 , I was surprised at how little effort was needed for the required changes to my existing software for the Loader Basic Input/Output System (LDRBIOS) and the system dependent Resident Extended Input/ Output System (RESXIOS). The only changes required were to edit out the RESXIOS initial jump vector for COLDSTART, and in its place insert a JMP COMMONBASE (to terminate a running process). The routine COMMONBASE is nothing more than:

| COMMONBASE: | JMP | COLDSTART |
| :--- | :--- | :--- |
| ; |  |  |
| SWTUSER: | JMP | $\$-\$$ |
| SWTSYS: | JMP | $\$-\$$ |
| PDISP: | JMP | $\$-\$$ |
| XDOS: | JMP | $\$-\$$ |
| SYSDAT: | DW |  |
| ; |  |  |
| COLDSTART: |  |  |
| WBOOT: |  |  |
| ; |  |  |
|  |  | MVI |
|  | C,0; terminateprocess |  |
|  |  | XDOS |

The changes to the LDRBIOS were more for cosmetic effect at sign-on time (and also a 'bug'!), than changes actually required for upgrade to MP/M-80 II from the two earlier releases. The signon messages were for user familiarity only, to let the user know from what and where he or she had control of the system. The user would see:

```
MP/M-Net (tm), System #l
>> Multi-user Software Access <<
```

    [USER 1]
    Enter USER $0<c r>$, if you require
access to other MP/M facilities.
$==============================$
$M P / M$ is a registered trademark
of
Digital Research
================================

Booting MP/M-80 Version II now...
Kelly Smith, 3055 Waco St., Simi Valley, CA 93063.

# The Newest Release of Digital <br> Research's Multi-user, Multi-Tasking OS 

This demonstrates a customized signon message that can be sent to each user (in this case, USER 1) prior to actually booting MP/M into the system. This is easily added to your LDRBIOS by modifying the initial 'JMP 322' at location 100H of MPMLDR.COM to the base of your LDRBIOS (1700H), outputting the data to each console in the system, and then returning control to the MPMLDR by THEN DOING the 'JMP 322':.
This is a nice way to let each user know that he or she is loved, and that the system is "coming up." If you do not do this, there is an agonizing pause as the MPMLDR brings in the system.

## MP/M-80 II System Generation

Once you have produced your RESXIOS.SPR file (page relocatable RESXIOS) with RMAC and LINK, you are ready to generate your MP/M. This
is perhaps the easiest part of the whole process of getting MP/M up and running. The GENSYS program guides you through the entire configuration of your system, including default values if you care to accept them, with just a simple carriage return. For an idea of how it works refer to Figure 1. Figure 1A maps the MP/M memory system as generated by the co-efforts of GENSYS and myself.

As you can see, the Common Memory area takes up from 13 to 16 K , to be shared by all users. The Banked Memory (Bank 0) area takes 48 to 51 K bytes. These "sizes" are totally dependent upon the number of extras that you want added to your system at GENSYS time. If you can add bankswitched memory, do so. Keep in mind however, that even if you add more memory no one user can access more than 48 K . This can be a very limiting system for certain applications requiring

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$\$ 6550$
hardware
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Real-Time Clock with Battery Back-up, Interrupt Controller, 3 Timers, and 4MHZ 9511 Type Math Processor
3 Serial I/O Ports or 2 Serial and 3 Parallel I/O Ports Dual Density DMA Floppy Disk Controller Desktop or Rack Mount Enclosure with CV Power Supply
28 -inch Shugart Floppy Disk Drives (1.2 Mbytes) Desk or Rack Mount

## SOFTWARE

CPIM 2.2 and CP/M 86 from Digital Research WORDSTAR word processor from MicroPro ACT80, ACT86, and TRANS86 from Sorcim XLT86 optimizing CP/M 80 to CP/M 86 translator from Digital Research.
Scientific, Business and Word Processing Systems also available.

## ADDITIONAL OPTIONS

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DIABLO, EPSON and TEXAS INSTRUMENTS printers 300 to 1200 baud modems for telecommunications COMPUPRO-complete line of CompuPro hardware MORROW DESIGNS hard disk drives, 10, 20, and 26 megabytes
ATTRACTIVE WOODEN CUBE for rack moun equipment

SOFTWARE
MICROSOFT FORTRAN with 9511 support routines MICROSOFT BASIC, PASCAL and COBOL
SUPERCLAC financial planning and forecasting
ACT80 and ACT86-macro cross assemblers fo 8080, 8085, Z80, 6502, 6800, 8086, and 8088 TRANS86-converts 8080/8085/Z80 source into 8086/ 8088 source
dBASE II-data base manager from Ashton Tate XLT86-from Digital Research, translates and optimizes 8080 source into $8086 / 8088$ source. Converts CP/M 2.2 BDOS calls to CP/M 86 calls.
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All these systems are FAST, and you can run them even faster by adding a WARP DRIVE'm WARP DRIVE ${ }^{\text {m }}$ is extended address RAM memory configured with CP/M to look like a disk drive. But it runs over 35 times faster!
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## G8G <br> -

 (415) 895-0798CompuPro is a tradernark of Godbout Electronics CPIM is a trademark of Digital Researc WORDSTAR is a trademark of MicroPro

## Figure 1.

```
A0>gensys<cr> <--- envoke MP/M-80 II GENSYS.COM file
```

MP/M II V2.0 System Generation
Copyright (C) 1981, Digital Research

Default entries are shown in（parens）．
Default base is Hex，precede entry with \＃for decimal
Use SYSTEM．DAT for defaults（Y）？n＜cr＞＜－－－no，want to＂roll－my－own＂ Top page of operating system（FF）？ef＜cr＞＜－－－I have 60 K to work with Number of TMPs（system consoles）（\＃4）？2〈cr〉＜－－－only two terminals Number of Printers（\＃1）？＜cr＞＜－－if this was Mike Karas，it would be 4！ Breakpoint RST（06）？05＜cr＞＜－－－let＇s use RST 5 instead Add system call user stacks（Y）？＜cr＞＜－－－definitely，to run＇．com＇files 280 CPU（Y）？n＜cr＞＜－－－still using that same old IMSAI 8080 card．
Number of ticks／second（ $\ddagger 60$ ）？ $40<c \mathrm{cr}\rangle<--40$＇ticks＇（1ittle＇bugs＇？ System Drive（A：）？〈cr＞＜－－－it works better than my flakey B：drive Temporary file drive（A：）？＜cr＞＜－－this is where SUBMIT will be． Maximum locked records／process（\＃16）？＜cr＞＜－－－reasonable value Total locked records／system（\＃32）？＜cr＞＜－－－maximum things going on Maximum open files／process（\＃16）？＜cr＞＜－－－sure，why not？ Total open files／system（\＃32）？＜cr＞＜－－－use this，but be warned that this will block other files，
when things get really busy！

Bank switched memory（Y）？ n ＜cr＞＜－－－just a meager 60 K system．．．sob！ Number of user memory segments（\＃3）？ $2\langle\mathrm{cr}\rangle\langle--$ three is company，too
much company in 60K！

Dayfile logging at console（Y）？＜cr＞＜－－－show me time and file executing every possible chance．

| RESERVED | FOOOH | 1000 H | ＜－－－chuga＇ka chuga．．．GENSYS building up the |  |
| :--- | :--- | :--- | :--- | :--- |
| SYSTEM DAT | EFOOH | 0100 H | MP／M system，for＇round one＇． |  |
| TMPD | DAT | EEOOH | 0100 H |  |
| USERSYS STK | EDOOH | 0100 H |  |  |
| XIOSJMP TBE | ECOOH | 0100 H |  |  |

Accept new system data page entries（Y）？y＜cr＞＜－－－acceptable locations！

| RESBDOS | SPR | E 000 H | 0 COOH | （－－－＇round two＇．．． |
| :--- | :--- | :--- | :--- | :--- |
| XDOS | SPR | BEOOH | 2200 H |  |

Select Resident and Banked System Processes：
ABORT RSP $(N)$ ？$y\langle c r\rangle\langle--$ short of＇pulling－the－plug＇，this may be
theonlyway toexitfromsome processes．
MPMSTAT RSP（N）？y＜cr＞＜－－－yah，nifty to see what the other user is doing．
$\begin{array}{lll}\text { SCHED } & \text { RSP } & (N) \text { ？} \mathrm{Y}\langle\mathrm{Cr}\rangle<-- \text { sure，cute way to demo a task on the＇} Q \text {＇} \\ \text { SPOOL } & \text { RSP（N）？} \mathrm{y}\langle\mathrm{cr}\rangle \text {＜－－let the printer work in the background．}\end{array}$
ABORT RSP BDOOH 0100 H ＜－－－＇round three＇
MPMSTAT RSP
SCHED RSOOH 0100 H
RBOOH 0100 H （did you ever notice，that in the
SPOOL RSP BAOOH 0100H movies there are always dramatic
RESXIOS SPR B500H 0500H was blinking and flashing（？）．
$\begin{array}{llll}\text { BNKBDOS SPR } & 9200 \mathrm{H} & 2300 \mathrm{H} & \text { All I ever hear working at home，} \\ \text { BNKXDOS SPR } & 9000 \mathrm{H} & 0200 \mathrm{H} & \text { is the sound of bad spindle beari }\end{array}$

MPMSTAT BRS 7EOOH OEOOH my acoustic modem！）
$\begin{array}{llll}\text { SCHED } & \text { BRS } & 7900 \mathrm{H} & 0500 \mathrm{H} \\ \text { SPOOL } & \text { BRS } & 7100 \mathrm{H} & 0800 \mathrm{H}\end{array}$
LCKLSTS DAT 6E00H 0300H
CONSOLE DAT 6 COOH 0200 H ＜－－－Gads！My available memory is
being consumed before my very VERY WISE choices as to WHO gets HOW MUCH remaining memory！

Enter memory segment table：＜－－－and here＇s my chance．．．
Base，size，attrib（6C，94，80）？＜cr＞＜－－－MP／M gets ALL of this．
Base，size，attrib $(00, \mathrm{c} 0,00)$ ？ $50, \mathrm{ff}, 00<\mathrm{cr}\rangle<---$ USER 1 starts at 5000 ， and goes for all the
＊＊＊Memory conflict－segment trimmed＊＊＊＜－－－the＇ff＇forced it！
Base，size，attrib $(50,1 \mathrm{C}, 00)$ ？＜cr〉＜－－－accept what we can get（7K！） Base，size，attrib $(00, C 0,00) ? 00,50,00<c r\rangle<--$ USER 0 gets 20 K remaining
MP／M II Sys $6 \mathrm{COOH} 9400 \mathrm{H}<---\mathrm{MP} / \mathrm{M}$ takes up 40 K bytes．
Memseg USr $5000 \mathrm{H} \quad 1 \mathrm{COOH}$＿－－USER 1 gets a meager 7 K bytes．
Memseg Usr 0000 H 5000 H －－－USER 0 gets to run SDIR（an 18 K file！）．
Accept new memory segment table entries $(Y)$ ？$y\langle c r\rangle\langle---$ do $I$ have any choice？
＊＊GENSYS DONE＊＊＜－－－whoopie．．．now we can boot＇er up with MPMLDR，and play！

## Figure 1A．

```
BAOO to EFFF - Common Memory Area; BDOS, XDOS, XIOS, DATA areas,
    and Resident System Processes.
6C00 to B9FF - Banked portions of the BDOS, XDOS, XIOS, DATA areas,
    TMP (consoles) and Banked Resident System Processes.
5000 to 6BFF - USER l's play-ground (about the size of a 'cat box'!).
0000 to 4FFF - USER O's play-ground (just enough to run SDIR for a demo!)
```


## MP／M－80 II Review，continued．．．

lots of memory（such as UCSD Pascal， which requires 56 K to compile pro－ grams）－so keep your applications memory requirements in mind before deciding to use MP／M，or you may be sorely disappointed to find out that it just will not fit！
Well，the moment is almost at hand to see if it actually works．I took the option of SYSGENing a normal CP／M 2.2 diskette，which autoloaded the MPMLDR．COM file at cold boot time． This allowed me the ability to debug the MP／M loader with the Dynamic Debugging Tool（DDT）under control of $C P / M$ ，if I ran into trouble．So，insert the diskette in the A：drive，hit reset， and watch the lights blink on the front of my old Imsai 8080 system．Yes，all seems to be ready－I set this MP／M system up so that a remote caller initiates the system boot when my modem＂hears＂ring－detect．So，time to give it a call．I fire－up my Osborne－I with a communications program I wrote called＂RCPMLINK＂and．．．I get the customized sign－on message，then the booting message，and．．．amazing！Here comes the MP／M II Loader（Figure 2）， just as Digital Research promised．I am astounded；this is the first time that I had any version of MP／M come up the first try．I then proceeded to set the time of day clock using the TOD．PRL program．

## Figure 2.

MP／M II V2． 0 Loader
Copyright（C）1981，Digital Research Nmb of consoles
$=2$
$\begin{array}{ll}\text { Nmb of consoles } & =5\end{array}$
Breakpoint RST \＃$=$
Memory Segment Table：
SYSTEM DAT EFOOH O100H
TMPD DAT EEOOH Ol00H
USERSYS STK EDOOH 0100 H
XIOSJMP TBL ECOOH 0100H
RESBDOS SPR EOOOH OCOOH
XDOS SPR BEOOH 2200 H
$\begin{array}{llll}\text { ABORT } & \text { RSP BDOOH } 0100 \mathrm{H} \\ \text { MPMSTAT } & \text { RSP } & \text { BCOOH } & 0100 \mathrm{H}\end{array}$
$\begin{array}{llll}\text { MPMSTAT } & \text { RSP } & \text { BCOOH } & 0100 \mathrm{H} \\ \text { Sched } & \text { RSP } & \text { BBOOH } & 0100 \mathrm{H}\end{array}$
Spool RSP BAOOH 0100H
BNKXIOS SPR B50OH 0500H
BNKBDOS SPR $9200 \mathrm{H} \quad 2300 \mathrm{H}$
BNKXDOS SPR $9000 \mathrm{H} \quad 0200 \mathrm{H}$
TMP SPR $8 \mathrm{COOH} \quad 0400 \mathrm{H}$
$\begin{array}{llll}\text { Mpmstat } & \text { BRS } & 7 \mathrm{EOOH} & \text { OEOOH } \\ \text { Sched } & \text { BRS } & 7900 \mathrm{H} & 0500 \mathrm{H}\end{array}$
$\begin{array}{llll}\text { Spool } & \text { BRS } & 7100 \mathrm{H} & 0800 \mathrm{H} \\ \text { LCKLSTS } & \text { DAT } & 6 \mathrm{E} 00 \mathrm{H} & 0300 \mathrm{H}\end{array}$
CONSOLE DAT 6COOH 0200H
MP／M II Sys 6 COOH 9400 H
Memseg Usr $5000 \mathrm{H} \quad 1 \mathrm{COOH}$
Memseg Usr $0000 \mathrm{H} \quad 5000 \mathrm{H}$
MF／M II V2．0
Copyright（C）1981，Digital Research
1A＞
1A＞tod $12 / 24 / 81 \quad 09: 36: 00\langle c r\rangle$
00：00：31 A：TOD ．PRL
Strike key to set time〈cr＞
Thu $12 / 24 / 81$ 09：36：00


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8086 FORTH................................................... $\$ 100.00$
8086 FORTH with software floating point arithmetic ...... $\mathbf{\$ 2 0 0 . 0 0}$
8086 FORTH with AMD 9511 support routines. ............ $\mathbf{\$ 2 0 0 . 0 0}$
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System requirements: Z-80 microcomputer with 48 kbytes RAM and Digital Research CP/M 2.2 or MP/M 1.1 operating system; 8086/8088 microcomputer with 64 kbytes RAM and Digital Research CP/M-86 operating system.
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## MP/M-80 II Review, continued...

Here is a sample directory display (Figure 3), first from USER 1's directory, then USER O's directory. Notice the "DAYFILE" display at the user invocation of the DIR command.

An impressive array of programs are available, but notice all the .PRL that have some very familiar CP/M names such as REN, ERA, DIR and TYPE. They are the same commands you have been using with one big differencethey are disk resident, not "built-in" commands to MP/M, and they take up valuable disk space (especially valuable if you are using 8 " single density floppys). Let's face it, MP/M was not meant to run on 8" SD floppys (look at the SDIR display further on this article, for the amount of remaining disk space). However, they will do for an example until I get around to installing it on my 20Mbyte hard disk. The average hacker has at least that much storage just laying around waiting for MP/M, right? WRONG! But then MP/M-80 II is for the "big boys" anyway (on a big budget!), so I guess that I can't complain. But please, do not be misled into thinking that you will put MP/M up on your dinky 5 " disk and have MP/M run. It won't.

## New Utillties And Features: SDIR, SHOW, SET WIth HELP Displays

One nice, new feature added to release 2.0 for MP/M-80 is that some of the system utilities have built-in HELP summaries that give examples of various ways to invoke them. I wonder, however, if it might have made sense to have the HELP portions of the files as overlays that could be deleted from the directory (and take up less memory and disk) after the USER(s) were familiar with all of the command options. Refer to Figure 4 for an example.

The utility SDIR needs 18 K of the system to be able to run. I was forced to GENSYS a 20 K area for USER 0 , just to see what it did, leaving only 7 K for USER 1. It would have been nice to allow an equal amount of memory allocation for each user...oh well, on with the show!
After re-GENSYSing for a 20K USER 0 memory allocation, I am able to get SDIR to run. Let's try SDIR with HELP first (Figure 5).
Refer to the directory (Figure 6) to find the next file of interest, SHOW,

Figure 3.
file:
1A>dir<cr>
06:40:09 A:DIR .PRL
Directory for User 1:
A: USER PRL : DIR
<--- display the Directory for USER 1

PRL <--- files I knew I would need here, and initially put them here with Bruce Ratoff's 'DUPUSER' utility

1A>user $0<c r>$
06:40:19 A: USER
. PRL
User Number $=0$
$0 A>$ dir $\langle c r>$
<-- display the Directory for USER 0
06:40:27 A:DIR .PRL
Directory for User 0 : A: BNKBDOS SPR : BNKXDOS

SPR : RESBDOS SPR : TMP SPR
A: SPOOL RSP : MPMSTAT
A: ABORT PRL : ASM
A: DSKRESET PRL : DUMP
A: ERAQ PRL : MPMSTAT
$\begin{array}{ll}\text { A: PRLCOM } & \text { PRL : RDT } \\ \text { A: SDIR } & \text { PRL : SET }\end{array}$
A: STAT PRL : STOPSPLR
A: TYPE PRL: USER PRL : MPMMIT
A: GENMOD COM : GENSYS
RSP : MPMSTAT
BRS : SCHED
PRL : CONSOLE
PRL : ED
PRL : PIP
PRL: REN
PRL : SHOW
PRL : SUBMIT
PRL : MPMLDR
COM: LOAD

RSP : SCHED
RSP
BRS : SPOOL BRS
PRL : DIR PRL

PRL : ERA PRL
PRL : PRINTER
PRL
PRL
PRL
PRL : SCHED PRL
PRL : SPOOL
$\begin{array}{lll}\text { PRL : TOD } & \text { PRL } \\ \text { COM : GENHEX } & \text { COM } \\ \text { COM : MPM } & \text { SYS }\end{array}$
A: RESXIOS SPR : SYSTEM
DAT: LOAD

## Figure 4.

OA>sdir *.*<cr> <--- let's look at the Sorted Directory display.
06:54:23
Reloc seg not free <-- oops... whats wrong? Relocation Segment Not Free?
NOTE: This bit of ignorance on my part that follows was prior to GENSYSing for a 20K user 0 memory allocation-just thought I would let you see what happens:


## Figure 5.

0A>sdir [help]<cr> <--- give me some HELP with SDIR.
09:30:42 A:SDIR .PRL
. PRL
sdir file.one
SDIR EXAMPLES
sdir file.one (find a file on current user and default driv
sdir *.com d:*.pli (find matching files on default and d: drive)
sdir [rw] (find files that are read/write)
sdir [ro dir sys] (same for read/only, directory, system)
sdir [xfcb]
(find files with XFCB's)
sdir [nonxfcb]
sdir [exclude] *.com
(find files without $X F C B^{\prime} s$ )
sdir [exclude] .com (find files that don't end in 'com'
sdir [nosort] (don't sort the files)
sdir [full]
(show all file information)
sdir [size]
sdir [short] (show just the file names)
sdir [drive $=$ all]
(show just the file names)
(search all logged in drives)
sdir [drive $=(a, b, p)]$
(search specified drives, 'disk' is synonym)
sdir [user $=$ all]
(find files with any user number)
sdir [user $=(0,1,15)]$
(find files with specified user number)
sdir [length $=\mathrm{n}$ ]
(print headers every $n$ lines)
sdir [ff]
(print form feeds between headers)
sdir [message user=all]
(show user/drive areas with no files)
(show this message)
sdir [dir sys rw ro sort xfcb nonxfcb full] d:*.* (defaults)

## Figure 7.

0A>show [help]<cr> <--- give me some HELP with SHOW.
09:30:20 A:SHOW .PRL
Drive status : SHOW DRIVE: SHOW d:DRIVE:
User Status : SHOW USERS: SHOW d:USERS:
Directory Label : SHOW LABEL: SHOW d:LABEL:
Free Disk Space : SHOW SPACE: SHOW d:SPACE:

Figure 6.

```
0A>sdir<cr> <--- displaytheSortedDirectoryandfile attributes.
00:00:26 A:SDIR .PRL
Directory For Drive A: User 0
```

| Name |  | Bytes | Recs | Attributes | Name |  | Bytes | Recs | Attribute |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ABORT | PRL | 1 k | 5 | Dir RW | ABORT | RSP | 1 k | 5 | Dir R | RW |
| ASM | PRL | 10k | 74 | Dir RW | BNKBDOS | SPR | 11k | 81 | Dir R | RW |
| BNKXDOS | SPR | 1 k | 7 | Dir RW | CONSOLE | PRL | 1 k | 4 | Dir R | RW |
| DDT | COM | 5 k | 38 | Dir RW | DIR | PRL | 2 k | 14 | Dir R | RW |
| DSKRESET | PRL | 1 k | 5 | Dir RW | DUMP | PRL | 1 k | 6 | Dir R | RW |
| ED | PRL | 9 k | 68 | Dir RW | ERA | PRL | 2 k | 15 | Dir R | RW |
| ERAQ | PRL | 4 k | 29 | Dir RW | GENHEX | COM | 1 k | 6 | Dir RW | RW |
| GENMOD | COM | 2 k | 10 | Dir RW | GENSYS | COM | 9 k | 68 | Dir R | RW |
| LOAD | COM | 2 k | 14 | Dir RW | MPM | SYS | 32k | 254 | Dir RW | RW |
| MPMLDR | COM | 7 k | 54 | Dir RW | MPMSTAT | BRS | 5 k | 33 | Dir RW | RW |
| MPMSTAT | PRL | 5 k | 33 | Dir RW | MPMSTAT | RSP | 1 k | 3 | Dir R | RW |
| PIP | PRL | 10k | 77 | Dir RW | PRINTER | PRL | 1 k | 8 | Dir RW | RW |
| PRLCOM | PRL | 3k | 21 | Dir RW | RDT | PRL | 7k | 50 | Dir RW | RW |
| REN | PRL | 3 k | 19 | Dir RW | RESBDOS | SPR | 4 k | 29 | Dir R | RW |
| RESXIOS | SPR | 2 k | 13 | Dir RW | SCHED | BRS | 2 k | 12 | Dir R | RW |
| SCHED | PRL | 3 k | 20 | Dir RW | SCHED | RSP | 1 k | 3 | Dir R | RW |
| SDIR | PRL | 18 k | 137 | Dir RW | SET | PRL | 8 k | 60 | Dir R | RW |
| SHOW | PRL | 8 k | 60 | Dir RW | SPOOL | BRS | 3 k | 20 | Dir R | RW |
| SPOOL | PRL | 3 k | 17 | Dir RW | SPOOL | RSP | 1 k | 5 | Dir R | RW |
| Stat | PRL | 10 k | 78 | Dir RW | STOPSPLR | PRL | 1 k | 5 | Dir RW | RW |
| SUBMIT | PRL | 6 k | 42 | Dir RW | SYSTEM | DAT | 1 k | 2 | Dir R | RW |
| TMP | SPR | 2 k | 11 | Dir RW | TOD | PRL | 3 k | 20 | Dir R | RW |
| TYPE | PRL | 2 k | 11 | Dir RW | USER | PRL | 1 k | 8 | Dir F | RW |
| XDOS | SPR | 10k | 79 | Dir RW |  |  |  |  |  |  |
| Total Byt |  | = | 226 k | Total Record | $s=16$ |  | Files F | und $=$ | 47 |  |
| Total lk | Bloc | ks | 226 | Used/Max Dir | Entries | For | Drive A | $52 /$ | 64 |  |

Figure 7 A.
0A>show drive<cr> <--- SHOW the Drive Characteristics
06:52:24 A:SHOW .PRL

```
    A: Drive Characteristics
    1,944: 128 Byte Record Capacity
    243: Kilobyte Drive Capacity
    64: 32 Byte Directory Entries
    64: Checked Directory Entries
    128: Records / Directory Entry
        8: Records / Block
        26: Sectors / Track
        2: Reserved Tracks
```

OA>show users<cr> <--- SHOW the USER and ACTIVE files.
06:52:47 A:SHOW .PRL
A: Active User : 0
A: Active Files: 01
0A>show space<cr> <--- sHow the remaining disk SPACE.
06:53:04 A:SHOW .PRL
$\mathrm{A}: \mathrm{RW}$, Space: 14 k

Figure 8.
0A>set [help]<cr> <--- give me some HELP with SET. 09:31:56 A:SET
.PRL

SET EXAMPLES
FOR FILES

| set *.asm [rw, dir] | (File Attributes) |
| :--- | :--- |
| set *.prl [ro, sys] |  |
| set *.dat [archive $=o n, f 1=o f f, f 2=o n, f 3=o n]$ |  |
| set *.asm [time] | (Time Stamping on ASM files) |
| set *.asm [password $=$ xyz] | (Password Protection) |
| set *.asm [protect $=$ read] | (read, write, delete or none) |

FOR DRIVES

| set [password $=\mathrm{xyz}]$ | (Label Password) |
| :--- | :--- |
| set [protect $=$ on] | (Password Protection) |
| set [update $=$ on] | (Update Time Stamps on or off) |
| set [create $=$ on] | (Creation Time Stamps on or off) |
| set [access $=o n]$ | (Access Time Stamps on or off) |
| set [make $=o n]$ | (Make XFCBs - on or off) |
| set [default $=x y z]$ | (Default Password) |
| set a:[rw], b:[ro] | (Drive Status) |

which is also an upgrade of the CP/M STAT utility. SHOW's HELP options are displayed in Figure 7.

So let's try a few. To see what happens look at Figure 7A.

Finally, the SET utility (Figure 8) contains some of the features of $C P / M$ 's STAT utility for setting various file or disk attributes, but goes beyond the simple \$R/O or \$R/W and \$SYS or \$DIR attributes of STAT.

It's worth noting that the MP/M II User's Guide describes a disk attribute control called NAME (see Section 7.4.5 Naming Disks, page 63)..."SET [NAME =labelname.type] does not appear in the HELP display and, if attempted, gives the following response:

```
A>set [name=mp/m-net.sys]
09:48:49 A:SET .PRL
ERROR: ?
Invalid Value, Use ON or OFF
```

It is curious that Digital Research describes this feature in the SET documentation, while it does not appear to work-is this a "bug"?

Next try the time-stamping features that were described in the SET HELP command (Figure 9.) Note that timestamping also works on CREATE and UPDATE when new files are created, or when a file is modified.

## A User Application: SEND-MSG For Intra-User Communication

I though it might be interesting to be able to communicate between multiple users as a "message drop" for posted mail (posted on the 'Q', and visible to other users via MPMSTAT as a pending message if they care to read it). Such as it is, this does demonstrate what can be done for intra-user communication in a common user system environment-nothing fancy, but it gets the job done, allowing up to 80 characters in a message string. To see if you have any "mail," just enter MPMSTAT<cr $>$ to see if a SENDMSG is attached to your console from another user. If so, just enter ControlD to attach SEND-MSG to your console, and to finish the execution of the pending message from MP/M's CLI (Control Line Interpreter) buffer storage. If you want to send a message (say to USER 0, from USER 1), just enter:
Al>send-msg 0 Hello whats your
Well, that's how it works in theory. To see what happens, look at Figure 10.

## PRIORITY ONE ELECTRONICS

## S-100 CPU



CPU-Z -GODBOUT
PART NO. $2 / 4 \mathrm{MHZ} \mathrm{Z8O}$ DPSU 24 Bit Addressing
SDGBT 160A A \& T .................... $\$ 295.00 \ldots$... $\$ 199.00$ SDGBT 160C CSC 3-6 MHZ. ............. $\$ 395.00 \ldots .$. . $\$ 375.00$

DUAL PROCESSOR 8085-8088 - GODBOUT
6 or 8 MZ Provides true 16 Bit Power with a standard 8
SDGBT 1612A A\&T bit S-100 bus.
SDGBT 1612C CSC SOLID STATE DISK DRIVE, 3500\% FASTER! Not Really, But the Next Best Thing For Godbout 8085/88 Users. Call for Details on M-Drive. See Page 340 of November BYTE
SDGBT MD 128K
\$1,550.00
SDGBT MD 256K
2810 Z80 CPU-CA. COMP. SYST
2/4 MHZ Z80A CPU with RS232C Serial I/O Port complete with Monitor PROM for 2422 Disk Controller SDCCS 2810A A \& T ................... $\$ 350.00 \ldots .$. . $\$ 280.00$

## CB2 Z80 CPU - S.S.M.

2/4 MHZ will accept 2716, or 2732, or RAM RUN/STOP and single step switches
SDSSMCB2K Kit
SDSSMZ80M
SSMZ8O Monitor
\$344.00 \$2.... \$260.00
sDSSMZ80M SSMZ80 Monitor
S.M

8080 CPU, 1K RAM, Holds 12708 ,
1 Bit parallel input port.
SDSSMCBIK Kit..
$\$ 183.00$
SOSSMCBIA A \& T
$\$ 252.00$ $\$ 225.00$

## S-100 I/O BOARDS <br> SYSTEM SUPPORT 1-GODBOUT

Serial port (software prog baud), 4 K EPROM OR RAM provision, 15 levels of interrupt, real time clock, optional math processor SDGBTI62A DESCRIPTION LIST PRICE OUR PRIC Assembled \& Tested $\$ 399.00$ \$360.00 SDGBTiG2C CSC $\$ 495.00$ \$460.00
sofir8231 Math Chip
SDGBT8232 Math Chip
S0abTi62AM1 A\&T with 8231 Math Chip
SDGBT162AM2 A\&T with 8232 Math Chip
SDGBT162CM2 CSC with 8232 Math Chip
MPX CHANNEL BOARD - GODBOUT
I/O Multiplexer, using 8085A-2 CPU on board
SDGBT166A A \& T: $\$ 495.00$ \$450.00 SDGBT166C CSC . \$595.00 \$550.00 INTERFACER I - GODBOUT Two Serial I/O
SDGBT133A
SDGBTI33C $\begin{array}{lr}\text { A \& T } & \$ 249.00 \\ \text { CSC } & \$ 324.00\end{array}$ $\$ 219.00$ $\begin{array}{ll}\text { SOGBTIB3C } & \text { CSC } \\ & \text { INTERFACER II - GODBOUT }\end{array}$
sagbilisua Three parallel, one serial I/O board
$\begin{array}{lll}\text { SDGBTI50C CSC } & \$ 249.00 \\ & \$ 324.00\end{array}$ $\$ 219.00$ INTERFACER III - GODBOUT
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SDGBTI748C CSC 200 hr . Burn in $\$ 849.00$ $\$ 629.00$ INTERFACER 3 WITH 5 SERIAL PORTS
$\begin{array}{lll}\text { SDGBT1745A } & \text { A \& } T & \$ 599.00 \\ \text { SDGBTI745C } & \text { CSC } 200 \mathrm{hr}\end{array}$ MULTI I/O - MORROW DESIGNS
Sompsmb3200 A \& T
SWITCHBOARD - MORROW DESIGNS Two serial I/O, four parallel I/O, one status port, one strobe port
SDMDSSB2411
$\$ 299.00$
$\$ 269.00$
Two serial I/O, two parallel I/O

SDSSMI04K Kit
SDSSMIO4A A \& $T$
SDSSMI04A A\&T $\quad$ I/O 5.SSM $\$ 290.00 \quad \$ 260.00$
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2 Serial, 3 Parallel including 1 Centronics
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1/O $8 \cdot$ SSM
8 Port Serial I/O with Timer A\&
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4 Full handshaking RS232 ports and optional 2 K ROM SDCCS271001 A \& T $\quad \$ 360.00$
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S-100 10 MHZ STATIC RAM NEW LOW PRICES!
RAM 20-32K SALE $\$ 299.00$


32K STATIC RAM - GODBOUT
RAM 2010 MHZ , 4K byte block disable, bank select

 \begin{tabular}{lllr}
\& SDABTI64AAB \& $8 K$ A\&T \& LST PRICE <br>
\& $\$ 210.00$ \& OUR PRICE <br>
\hline

 SDGBT164AC8 8 K CSC $\$ 280.00$ \$260.00 SDGBT164AA16 16K A\&T, $\$ 285.00$ \$260.00 SDEBT164AC16 16K CSC $\quad \$ 355.00 \quad \$ 325.00$ 

SOGBT164AA24 \& $24 K$ \& A\&T <br>
SDGBT164AC24 \& $24 K$ \& CSC <br>
$\$ 355.00$ \& $\$ 325.00$ <br>
\hline
\end{tabular} $\begin{array}{lll}\text { SOGBT164AC24 } & \text { 24K CSC } & \$ 425.00 \\ \text { SDGBT164AA32 } & \text { 32K A\&T } & \$ 385.00 \\ & \$ 425.00 & \$ 299.00\end{array}$ SDGBT164AC32 32K CSC $\quad \$ 495.00 \quad \$ 2950.00$

## CMOS STATIC RAM

For a complete analysis of the advantages of CMOS memory, see the "Product Description"on page 416 of the January Issue of BYTE

64K CMOS STATIC RAM - GODBOUT
RAM 17, $10 \mathrm{MHZ}, 2$ Watt, DMA Compatable 24 Bit Addressing

$\begin{array}{llll}\text { SDGBT175A48 } & 48 \text { K A\&T } & \$ 650.00 & \$ 619.00\end{array}$ SDGBT175C48 48 K CSC 200hr. $\$ 750.00$ \$710.00 | SDGBT175A64 | $64 K$ A\&T | $\$ 795.00$ | $\$ 755.00$ |
| :--- | :--- | :--- | :--- | SDGBT175C64 64K CSC 200hr. $\$ 895.00$ \$80 $\$ 850.00$ NEW! 32K $\times 16$ BIT CMOS STATIC RAM - GOD

RAM $1610 \mathrm{MHZ}, 32 \mathrm{~K} \times 16$ or $64 \mathrm{~K} \times 8$

IEEE/696 16 BIT 2 Watt, 24 Bit Addressing
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$\$ 425.00$
SDSSMVB3A24 $80 \times 24$ A\&T $\$ 499.00 \quad \$ 440.00$ SDSSMVB3UP $80 \times 50$ Line Upgrade
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I/O Mapped Video Board, with Parallel Keyboard port sussmvb2k Kit $64 \times 16$ $\$ 199.00$
SDSSMVB2A A \&
$\$ 269.00$
$\$ 229.00$
Memory Mapped Video Board $64 \times 16$ character display or $64 \times 16$ graphics display

## sossmvbik Kit

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SDGBT153A
SDGBTI53C SDGBTI53C SDGBT154A SDGBTI54C SDGBT155A

Active termination, 6-12-20 slot
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## S-100 DYNAMIC RAM



## THEE EXPANDABLE 1

## PRIORITY 1 ELECTRONICS

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SDCCS2422A |  | $\$ 475.00$ | $\$ 375.00$ |
| ---: | ---: | ---: |

DISK JOCKEY 2D - MORROW
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SDSYOvM6013 35 lbs
4 character
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| PART NO. | DESCRIPTION | LIST PRICE OUR PRICE |
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## S-100 SYSTEMS

## SUPERSDXIEEN - GODBOUT

## HERE IS WHAT EACH PACKAGE INCLUDES:

 socetibiva 6 MHz 8085/8088 Dual Processor Board sobetilia high Speed DMA Disk ControllerSDEBT162A System Support 1 Multi-Function Board
Socsina interfacer 1 Dual Serial I/O
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SDABTCP/M 8616 Bit Operating System Ready to Load \& Go Cables and Documentation Three interfacer cables one disk I/O cable, complete documentator for all hardware, and manuals for both CP/M operating systems.
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PART NO.
DESCRIPTION (Switch Selectable)
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## S-100 MAINFRAMES



## S-100 MICROFRAME - TEI

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PRIORITY 1 has delayed the 8\% TEI
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## TEI S-100 FRAMES

## 3-5" DISK CUTOUTS

$\pm 8 \mathrm{~V}$ @ $17 \pm 16 \mathrm{~V} @ 1.2 \mathrm{~A}$, Internal Cables
$\begin{array}{lll} & & 12 \text { Slot desk } \\ \text { SDTEITF12 } & \text { 109.24 } \\ \$ 675.00 \\ \$ 625.00 \\ \$ 580.00\end{array}$ SOTEIRF12 12 Slot Rackmount $\$ 795.00 \$ 715.00$ \$665.00 Shipping Weight: On 12 Slot Desk 40 lbs . On 12 Slot Rackmount 45 lbs.
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$+24 V$ @ $1.5 A+5 V @ 1.0 A-5 V @ .25 A$
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Due to UPS shipping regulations, disk drives will be shipped separately from the cabinet. Don't forget to include shipping for each drive. (Shipping Weight, 16 lbs each.)

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110 V 60 HZ CVT Mainframe uses famous 20 slot GODBOUT Motherboard. 55 lbs .
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GODBOUT Mainframe, Less Motherboard \& Power Supply-Kit. 23 lbs.
SDGBTBOX DESK
Desk Top Main Frame
$\$ 289.00$ $\begin{array}{lll}\text { SDGBTBOX RACK } \quad \text { Rack Mount Main Frame } & \$ 329.00\end{array}$

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12-slot motherboard with removable termination card Snccs220001 Office Cream $35 \mathrm{lbs} \quad \$ 575.00 \$ 535.00$ siccsz20002 Blue
$35 \mathrm{lbs} \quad \$ 575.00 \$ 535.00$

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All software is supplied on 8 " Single Density IBM 3740 CP/M Compatable Diskettes

WORDSTAR
Screen-Oriented, integrated word processing system specifically designed for non-technical personnel
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MAIL MERGE WORD STAR OPTION

MAI. MERGE WORD STAR OPTI
Powerful file merging tool
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Exactly one-half the height of any other model.
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|  | Manual for DT-8 | \$ 10.0 |
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## PRIORITY ONE

## MP／M－80 II Review，continued．．．

You can continue stacking as many SEND－MSG＇s as your user memory allocation allows（I obviously didn＇t have enough memory！）．The＂Send Message＂ program（Figure 11）may be assembled with RMAC and LINK，or as RELO and REL1＇．HEX＇files using GENMOD．

## Conclusion

Digital Research＇s user docu－ mentation is perhaps the best that you could desire，including a comprehensive User＇s Guide，Programmer＇s Guide，and System Guide，all with complete glos－ saries and indexes，and even an acronyms and conventions list．This is a far cry from the original（terrible）CP／M 1.4 documentation．Also included are manuals for the LINK－80 linkage－editor， and MAC（as a reference document to the RMAC relocating macro assembler facilitfies．Incidentally，LINK－80，RMAC （and LIB－80 as well as XREF）are well worth the price of the diskette without MP／M－80 II！

MP／M－80 II is not for everyone， especially the casual user on a tight budget．In the hands of a good systems－ type programmer，and given the hard－ ware resources to properly support all of the features of MP／M，this is the multi－user／multi－tasking operating system to be using for running the myriad of CP／M－compatible applications programs that are available．I strongly recommend that you purchase both the＂MP／M II User＇s Guide＂and＂MP／M－ II System Guide＂manuals before pur－ chasing the MP／M diskettes them－ selves－you really need to get an overall view to make the best possible choice in applying MP／M to a particular appli－ cation environment．

MP／M，MP／M II，RMAC and LINK－80 are trademarks of Digital Research．

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 engineer／programmer with Pertec Computer Corporation，developing diagnostic software for systems and system peripherals．He is the vice－ president of the Valley Computer Club （Burbank，CA）and system operator of the CP／M－Net Remote CP／M System，in addition to editor and publisher of the CP／M－Net News．Activities and interests include contributing software to the SIG／M User Group library and West Coast SIG／M software distributor via modem．Figure 9.


0A＞dir stat．＊＜cr＞＜－－－access DIR as an experiment for time stamp 09：46：52 A：DIR PRL
Directory for User 0：
A：STAT PRL
OA＞stat＜cr＞
09：47：12 A：STAT－－－－also access STAT for time stamping．
A：RW，Space：$\quad 24 \mathrm{k}$
0A＞sdir＊．prl＜cr＞＜－－－SDIR should tell us if the two files were＇stamped＇！
09：47：36 A：SDIR ．PRL
Directory For Drive A：User 0


Figure 10.
OA＞send－msg 1 Hello from USER 0．．．．Whats up？＜cr＞＜－－－set－up lst message 09：37：45 A：SEND－MSG．PRL
$0 A\rangle$ send－msg 1 I hope you got my message，BYE！〈cr〉＜－－－set－up 2nd message
09：38：11 A：SEND－MSG．PRL
OA＞mpmstat＜cr＞＜－－－let＇s see if the messages are＇posted＇
09：38：20 Msg Qued
＜－－－I removed some info from MPMSTAT for brevity！
Process（es）Attached to Consoles：
［0］－Tmp0
Process（es）Waiting for Consoles：
［1］－Tmp1［1］SEND－MSG［1］SEND－MSG［1］＜－－－there they are！
Memory Allocation：
$\begin{array}{ll}\text { Base }=6 \mathrm{COOH} & \text { Size }=9400 \mathrm{H} \\ \text { Base } & =5000 \mathrm{H} \text { Allocated to } \mathrm{MP} / \mathrm{M}-80[0]\end{array}$
Base $=5000 \mathrm{H}$ Size $=1 \mathrm{COOH}$ Allocated to SEND－MSG［1］
Base $=0000 \mathrm{H}$ Size $=5000 \mathrm{H}$ Allocated to SEND－MSG［1］＜－－－2nd message
0A〉user $1<c r\rangle\langle---$ switch to USER 1.
09：39：04
Reloc seg not free＜－－oops．．．no room to execute USER．PRL file！
OA＞＜－－can＇t see it，but this is a Control－D to＇GET＇the messages
Attach：SEND－MSG
This message is from console number： 1
HELLO FROM USER O．．．WHATS UP？
＜－－another Control－D to get the remaining message
Attach：Tmpl
Attach：SEND－MSG
This message is from console number： 1
I HOPE YOU GOT MY MESSAGE，BYE！
Attach：Tmpl
$0 A>$ user $1<c r\rangle\langle---$ now that message are＇flushed＇this should work！
09：39： 29 A：USER ．PRL
User Number $=1<---$ and it does！

Figure 11.


S-100 Boards from S. C. Digital


64K DYNAMIC RAM 'Uniselect: 2'
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## Model 64KUS

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32K Static Ram 'Uniselect: 3'
features:

## Model 32KUS

- Fully Static using 2 k by 8 NMOS chips. - 16 or 24 bit address. - 8/16 bit wide data. - Bank Select by port and bit in 32 K block. Two 16 K block addressing with window capability in 2 k increments. - EPROM can be mixed with RAM. - Fast access - 250 nsec from address valid -will run with 280,28000 to $4 \mathrm{mhz}, 8080,8085,8088,8086$ or 68000 to 8 mhz without Wait States. - Provision for Battery Backup using NMOS or CMOS.


I/O, Memory Interface 'Interface: 1' features: Model 3SPC

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Z80 CPU Board Model CPUI-Z80
features: - 2 or 4 mhz clock. - Jump on Reset 2 K of EPROM (not supplied). - 8 levels of prioritized vectored interrupts.

## 16K Static Ram 'Uniselect: 1'

features: Model 16KUS

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## Software/Hardware Product Review

# The OASIS Multi-User Operating System 

by Michael J. Karas

Is this just another operating system?<br>And, a brief look at an S-100 multi-user hardware system.

The dictionary defines an "oasis" as a green, growing area in a desert or as a welcome change from the usual pace of life. "OASIS" is also the name of a microcomputer operating system that has gained a significant foothold in the microcomputer software marketplace. One has to wonder why a software product such as this was named OASIS. The microcomputer business is far from a desert. The hardware and software aspects are growing so rapidly that it is virtually impossible to keep ahead of new developments. As soon as products become available, we hear of new application areas for microprocessor hardware and software systems. The new needs then tend to foster development in a seemingly never-ending cycle. Thus, considering the state of the micro-marketplace, it must be that the OASIS operating system was introduced not as "green spot in the desert," but as a welcome change from the way things have been done. In the next few pages I will try to show why the OASIS operating system may very well be a new approach to the way microcomputer operating systems function.

As a first time user, I had never seen OASIS in operation. To become familiar with this product (or any other software product, for that matter) I had to use it, and compare it with other products in the marketplace performing a similar function. I am professionally involved in the systems end of the microprocessor business. My field of comparison for OASIS was to contrast the operational characteristics, human interface aspects, development tools, and end-

[^0]user application possibilities. Access to an appropriate hardware system and the OASIS software was obtained such that I could "setup" the system to my specific requirements much as an end-user would in purchasing a microcomputer system for use in a business, scientific, or educational application.

## An OASIS Hardware Configuration

The system hardware upon which the operating system evaluation was performed was the SYSTEM 80W, an S100 machine produced by NNC Electronics. This high quality hardware product is a unitized computer/mass storage system measuring approximately 18 inches wide, 11 inches high, and 19 inches deep. The SYSTEM 80W is based upon the IEEE/S-100 Bus Standard with a 4 MHz Z-80A CPU card and two 64K dynamic RAM boards providing a total of 128 K of memory in a bank-switched configuration. The primary data storage is provided by a Shugart SA1004 Winchester Disk, with 8.4 Megabyte formatted data storage capacity in conjunction with the companion XCOMP Winchester disk controller. File backup and loading convenience is included via a Shugart 801R 8" double density and double-sided floppy disk drive. The drive, including features of AC motor on/off and a door lock, is controlled by an OEM version of the CCS floppy disk controller.

Peripheral I/O was via three RS-232 serial I/O ports accessible on the rear panel of the computer. Optional hardware can include parallel ports or more serial ports. The internal card cage could also accomodate user-

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## OASIS Review, continued...

specified hardware such as a modem board for communication or additional memory cards. This system is available from the manufacturer: NNC Electronics, 15631 Computer Lane, Huntington Beach, CA 92649; (714)8958000, for $\$ 8,799$ and $\$ 850$ for OASIS.

## Obtaining The Software

The system software, the latest Multi-user Version 5.5A of OASIS, was provided in a format properly configured for the NNC Electronics hardware through the courtesy of the product distributor, Phase One Systems, and NNC Electronics. The evaluation package included all system functional modules and others such as a Basic Interpreter/ Compiler, Macro Assembler/Linker package, plus an impressive array of compatible utility packages that handle system maintenance and configuration chores. Complete documentation on the OASIS System was also provided. The OASIS product was written by a talented and enterprising fellow by the name of Timothy S. Williams, and is distributed and supported by Phase One Systems, Inc., 7700 Edgewater Drive, Suite 830, Oakland, CA 94621; (415)562-8085. OASIS is $\$ 850$, and includes all the software described in this article.

## Initial Observations

Once I had the system and software in place, the evaluation really began. My goal was to attach a Televideo 912 CRT as the system console at one serial port, (this was to be straightforward since the standard NNC configuration also utilizes a Televideo terminal), configure a second terminal for user two on another serial port, and connect a serial interface printer as the system hard copy device. The terminal for user two was a DEC VT100 and the printer a TI 820 dot matrix line printer. A review of the documentation was needed to learn how to go about the peripheral attachment process.

## OASIS Documentation

The OASIS documentation consists of a well-organized set of manuals describing every aspect of the operation of the software. The first is a general system reference guide that led me by the hand through the OASIS philosophy, command entry formats, and command definitions. Each system command that may be used at the Command String Interpreter (CSI) control level has a complete section of description, option definition and examples!

Another feature of the manual (and all other OASIS documentation) that I have found extremely useful is the fact that commands, each in a separate chapter, are presented in alphabetical order with a topical index marker printed in the lower outside corner of each page. On the first trip through the documentation, the value of this index was not realized. It was only later at the "try and learn" phase when I would say "How did SHOW work?", that I realized the value of this indexing. "SHOW" was easily found in alphabetic order between "SHARE" and "SPOLLER."
Only one comment need be made on the physical attributes of the manual. There is a great deal of paper in the binder with only a limited binder size. The paper is very thin and could easily have been torn from the three
binder rings. Printing of each manual in a separate softbound format would allow heavier paper to be used, and would probably allow the system documentaion to survive through months of use. Since the OASIS is generally intended to be multiuser, the three ring binder documention format might limit the "stay-in-one-piece" life-as many people require its use to learn system operation
The documentation package also includes complete operational and example-filled paperwork to describe the Basic, Macro Assembler, Linker, Executive Language and so on. Each manual has had the same care taken in its presentation to the user. The topics are presented and indexed for easy information access.

Another impressive feature of the system is an on-line help system. A file on the system disk contains a quick summary of the command formats and possible options for each OASIS command. Just in case the user needs a quick review on how to use a command such as BACKUP, he or she need only type the following:

```
>HELP BACKUP<Cr>
```

and a screen full of information pops up to tell you how to use the BACKUP program. Many of the command programs that have their own operator prompt mode, such as the DEBUG program debugger, support an internal access mode to the help file. Such utility packages permit the word HELP to be typed at the command prompt for immediate display of the command options available for that utility.

## Setting Up Terminal Two

As the system was made available, the default mode of operation for the system terminal was a "Class 7 " console, meaning a Televideo. (A TVI-912 in my case.) In OASIS, all user console devices are driven by an appropriate assembly language driver package. An integral part of this driver package is the function of translating an internal "OASIS Standard" set of terminal controls to the actual control functions required by the user's terminal. As each user console is put on-line by the default parameters specified either at system generation time or at the time it is "ATTACH"ed via a system utility, the translation information is indicated by reference to one of several available "SYSTEM.CLASSnn" files. These files (on system disk) are each specified for a given class of terminals. In my case, the terminal I desired to attach as the second user console was a DEC VT-100.

None of the standard class code files supplied with the system matched the translation characteristics of the VT100 or VT-52. (Note that the VT-100 may be configured to respond to the DEC VT-52 screen control codes. This subsequent control code set is more typical of the screen commands used by other terminals.) It is possible to use a terminal that appears as a TTY-like device, but many system functions, like the editor, console listing functions, and certain applications programs, work better with screen erase and cursor positioning capabilities. Thus I elected to get a taste of using the OASIS text editor and macro assembler by making up a new class code file for the VT52 mode of the terminal. As seems to be normal for the OASIS documention, the process of setting up the class code file for a new terminal type was clearly explained.

The class code file was entered in source code format using the OASIS "EDIT" utility. This editor is a line mode editor in the sense that text is generally processed one line at a time. Entry of text proceeded in a fairly typical manner for this kind of utility. The surprising differences were that default tab stops in the input mode are designed for assembly language format (a pleasant surprise), and certain columns are default to upper case characters for the opcode field. Another feature that had taken the human element into account was the line modification mode. Once text is entered it may be modified, a line at a time, by invoking the line edit mode. The line of text is displayed on screen with the cursor at the beginning of the line. Certain command codes move the cursor, insert or delete a character, or split one line into two. The modification operation is very similar to a full video mode editor except that only one line is the field of control. The result is a powerful text editor that does not require the memorization of 59 screen control functions before editing can begin. I was successfully entering and modifying text in my class code source file in less than twenty minutes.
The following listing is the class code file which I used to configure the OASIS system to the VT-100 terminal. The listing also includes several features of the OASIS Macro Assembler.

```
==>Fille CLASS52.ASSEMBLE
    TITLE 'CLASS CODE 52 (DFC VT 52 MODE OF VT 100)'
    ENTRY PARAMETERS:
        (A) - Control Character to Translate
        (B) - Console Device Number
        (C) - same as (A)
        (H) - Cursor address column counter
        (L) - Cursor address line number
```



```
    INIT
    DCA
    LD 
        A,01FH
        C,A
        A,C1FH ;Cursor position bias again
        A,ClFH ;Cursor position bias again
        C,A
                            ;Setup direct cursor address
                    ; entry poin
                    ;Send cursor position leadin
                            ;Send cur pos code func letter
                            ;Cursor position bias
                            ;Send the ROW code out to device
                            HOME,ESC,'H',O8CH
                            HOME,ESC,'H',O8CH
        CLEAR,ESC,'H',ESC
        EOS,ESC,'J',08C
        EOL,ESC,'K',08CH
        LEFT,ESC,'D'
        RIGHT, ESC,'C'
        RIGHT,ESC
        UP,ESC,'
        EU ;Not available
        ;Not available
        ;Not available
                            ;Not available
                            ; Not available
                            ;Not avallable
                            ;Not available
                            ;Not available
                            ;Not available
                    Not available
                            ;Not available
                            -Not available
    END
i...+++END OF FILE CLASS52.ASSEMBLE
```

The assembly language native to the OASIS system and processed by the Macro Assembler is a Z-80 utilizing ZILOG mnemonics. Notice from the listing that the assembler knows the values for control codes such as "ESC" and "LF." Also, the procedure of making a system
call involves a simple macro invocation like "SC 64." This translates into a system call type 64 that sends the character in (C) to the device addressed by the (B) register. (For documentation purposes only, the PON, POFF, .... ULOFF are macro invocation parameters for control sequences not available on the VT-52 terminal. Typical controls possible via these codes, provided the terminal can interpret them, are underline on/off and reverse video on/off.)
The program file described above was converted to the appropriate relocatable object file by using the Macro Assembler and Linker programs. An interesting capability provided with the OASIS system is a command file "ASM.EXEC", a program similar to a job submittal function on other operating systems. In this case, "ASM.EXEC" is a command file that successively invokes the macro assembler and linker. To get all of the CLASS52 file put into the proper format, all I had to type was:

```
>ASM CLASS52<cr>
```

The executive command processor did the rest by calling in the assembler and linker in turn. The similarity of OASIS EXEC to job submittal functions on other microcomputer operating system ends at the capability to process predetermined sequences of operator commands. In the OASIS environment, the EXEC processor more closely resembles the JCL language that I used some years ago on an IBM 370 system. The EXEC processor will execute an ASCII command file in a somewhat interpretive mode. The command file may contain direct CSI commands and internal calculations based upon EXEC variables and system codes returned from the last executed program. Command statements include looping possibilities with "WHILE" and "UNTIL" constructs, direct console/printer I/O and operator parameter input query. Another feature includes the possibility of passing parameters from the EXEC command processing level to the next executing transient applications package. This feature allows for the passage of information between programs without having to write it to a disk file.

The process of making the VT 52 mode of the DEC terminal work was completed with shining success. I was immediately able to get the system to bring up the second console, using the system utility commands to define a second memory partition and start active execution of a second user. Attachment of the printer was also easy since the physical device drivers that allow connection of printer devices support a number of printer "BUFFER FULL" determination mechanisms. I chose to use the "Data Set Ready" hardware handshake mechanization due to the simple nature of getting it going. The NNC hardware implementation of all serial ports includes the data set ready input on pin 20 of the rear panel DB25 RS232 connector. The TI 820 printer may conveniently be configured to assert a "reverse channel handshake" buffer full on a specific line. All I had to do was wire this line to the SYSTEM 80W connector pin 20, and the printer was up and going. The process took less than a third of the time typically expended in attaching a printer to an S-100 computer using another popular operating system.

## Multiuser Processing

With the two consoles configured to the system, I was ready to try the multiuser aspects of OASIS. The multi-

## CASIS Review, continued...

processing scheme of OASIS is based upon an internal real-time repeative interrupt that forces a system execution entry every few milliseconds. This interrupt interval, or multiples of it, create time slices during which alternating tasks are allowed to execute. If I booted up the system and didn't attach a second user, the system would then allocate every time slice to the main console, causing the system to appear to be single user. When I attached the second user, the system allocated every other time slot to alternate consoles and programs being run from those consoles.

The default time slice allocates 30 milliseconds to each user at a time. I found this time span to be adequate for most of my purposes. I did note, however, that a shorter time slice improved multiple terminal performance somewhat-if one user was creating a printout at the same time as another was doing a large amount of screenoriented output. The OASIS system permits an easy means of dynamically changing the time slice to a value that optimizes system performance for a given execution environment with a simple command like:

```
>SET SLICE=nn<cr> .. where nn is the tifue slice length
    in milliseconds.
```

A time slice of ten milliseconds was found to give the best performance for program executions requiring huge amounts of serial I/O via the three serial ports. If the processing was generally CPU speed bound, then the time slice factor had little effect on the speed of program execution.
The table below shows representative numbers for program execution times in various modes to give an indication of system performance in the multi-user mode versus single-user mode. The example mode used was primarily CPU speed bound. I took the previously presented class code definition file, and made two copies of it names USER1TST.ASSEMBLE and USER2TST.ASSEMBLE. The Macro Assembler executive command file "ASM" was used at both user consoles to assemble the two identical programs. Note that the two assembly processors shared hard disk resources for source input, object output,

Figure 1: Assembly Time Comparisons on OASIS 7 using class code file as input.

| Condition of Assembly | Time |
| :---: | :---: |
| Assemble from User 1 with User 2 idle in CSI Input wait. Both users logged to SYSTEM account. | $1 \mathrm{~min} / 7 \mathrm{sec}$ |
| Assemble from User 2 with User 1 idle in CSI Input wait. Both users logged to SYSTEM account. | $1 \mathrm{~min} / 6 \mathrm{sec}$ |
| Both users do same task at same time while logged to SYSTEM account. |  |
| USER 1 USER 2 | $\begin{aligned} & 2 \mathrm{~min} / 6 \mathrm{sec} \\ & 2 \mathrm{~min} / 7 \mathrm{sec} \end{aligned}$ |
| Assemble from console 1 with no active user 2 defined. Immediate system mode not logged to an account. | $1 \mathrm{~min} / 4 \mathrm{sec}$ |

and print file output. Also shared were the included macro file "CLASS", the assembler command file, and the linker command file.
In the examples, both users were running at a file access priviledge level of six (6) and had consoles at 9600 baud. The system time slice was at the default 30 millisecond value. The start time indicated was measured from depression of the carriage return key after the user's CSI command had already been typed in. Time measurements were made using a digital wrist watch with a one second resolution time.
The assembly times in Figure 1 are obviously limited by processing time. For two users to perform the same task, the execution time is almost exactly twice as long. Note that the last example was run to show that singleuser operation of the system is very slightly lowered by having an attached and idle second user console.

## Looking at OASIS Basic

The OASIS system includes a complete Basic language programming system that has some unique features. The Basic package is both an interpreter and a compiler. The interactive interpreter may be used for program development and debug, while the compiled mode may be invoked to produce a program that executes without needing the overhead of having the whole interpreter/compiler resident in the memory of the active user area. Also included with the system is a re-entrant version of the Basic that may be loaded such that multiple users may access the same image, from multiple active user areas. In reviewing the memory requirements to have Basic resident for each user versus having one re-entrant copy for all users, it appears that on a three-user system, more program memory space would be available for the second and third users than would be available on a two-user system, each with his own copy of Basic. This estimate was based upon the 128 K memory configuration of the NNC SYSTEM 80 W .
The functional capability of the OASIS Basic is roughly equivalent to other popular Basics from Compiler Systems or Microsoft. A number of special capabilities available appear to be due to the presence of the powerful host operating system file manager and real-time capabilities. Command functions within the language may include any valid system CSI level command, right in the middle of the Basic program! This allows full use of separately developed programs (in any language) to enhance the operation of a Basic program. (Couple this with the parameter-passing capability of the EXEC processor, and you have an extremely powerful vehicle upon which to develop sophisticated turn-key application packages.)

Direct Indexed file I/O is possible within the Basic, as this file format is directly supported by the operating system. For multi-user processing of files under the Basic (or other programs, if properly written), automatic file access record lockout is a feature that will guarantee data base integrity if multiple programs (users) are using the same data files. Many other systems do not provide this capability intrinsic to the operating system. Thus, incredible programming games must be played to achieve the same level of data access integrity.

A few other comments related to the Basic and its operation are in order here. During program development,


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## OASIS Review, continued...

the program syntax is checked (and can be corrected) as the statements are entered, not as they are executed. In addition, since syntax checking need not be done at interpretation/execution time, the user will see some improvement in execution speed. Another feature discovered in the Basic manual was something I had not seen in a high level computer language since I programmed on a main-frame computer. That feature is the capability of the Basic programmer to access the time and date routines of the system. I have illustrated the use of the time function in the Basic program listing that follows.

The program listing below shows a short program written to exercise the system execution times, as I did with the class file assembly times, using the system clock to time the program execution. Recall that the Basic interpreter was running on a $4 \mathrm{MHz} \mathrm{Z}-80$, should the reader desire to compare execution time of this program against that of another Basic. The system time slice during these tests was at the default 30 millisecond value.

```
=> Execution Time Test BASIC Program (USES SQUARE ROOT FUNC)
    10 PRINT "START TIME ",TIMES (0)
    20 FOR I% = 1 TO 10000
    30 J = SQR(I)
```



```
    50 PRINT "END TIME ",TIMES(0)
    60 END
```

| Execution Condition | Time |
| :---: | :---: |
| Executed by User 1 with attached printer in console echo mode. User 2 in prompt mode of Basic. | $0 \mathrm{~min} / 43 \mathrm{sec}$ |
| Executed by User 2 with no attached devices. User 1 in Basic prompt mode with attached printer. | $0 \mathrm{~min} / 53 \mathrm{sec}$ |
| Executed by User 1 with attached printer but no print echo on. User 2 in prompt mode of Basic. | $0 \mathrm{~min} / 43 \mathrm{sec}$ |
| Executed by both users at same time with no printer echo on at User 1. Device still attached. |  |
| USER 1: <br> USER 2: | $\begin{aligned} & 1 \mathrm{~min} / 26 \mathrm{sec} \\ & 1 \mathrm{~min} / 26 \mathrm{sec} \end{aligned}$ |
| Executed by both users at same time with printer echo on at User 1. User 2 startup delay due to User 1 printing. |  |
| USER 1: <br> USER 2: | $\begin{aligned} & 1 \mathrm{~min} / 25 \mathrm{sec} \\ & 1 \mathrm{~min} / 25 \mathrm{sec} \end{aligned}$ |

## Random Comments

Other items of interest relate primarily to several of the utility packages furnished with OASIS. For a systems person such as myself, I feel that the Z-80 program debugger is a particularly nice package. Direct assembly/ disassembly is permitted in complete ZILOG mnemonics. The on-line assembler does immediate syntax checking and program listing-just like an assembler output.
A disk backup utility furnished with the system called "ARCHIVE" makes the file backup process a breeze. One feature of OASIS is the direct indexed file format supported by the host file manager. As an applications
program data base is built in a file of this type, much of the file may contain blanks in filling out records fields. Many records may also be inactive because of delete status, or may never have been allocated as active records. This leads to the situation where ARCHIVE is an especially powerful backup utility. The backup from an active system work disk (such as the hard disk) to floppy compacts the data files as they are transferred. This allows random access direct files larger than a whole floppy to be brought into reasonable backup storage size. Other features of the ARCHIVE system are backup of files by selected wild card names, by range of creation dates, or by range of most recent access dates. Multi-volume diskette ARCHIVE backup is also possible with operator prompting for insertion of the proper diskette(s).

The hardware configuration utilized for the evaluation also deserves a final comment here. During the 45 day period that the NNC SYSTEM 80W was tested, it performed flawlessly. The reliability of the floppy system was evident in that no floppy read/write problems were encountered. The double density media conformance to IBM standard format compatibility was checked via format interchangeability with another computer system. No interchange problem was found despite the fact that the computers used entirely different types of floppy disk controllers. The SHUGART SA1004 8" Winchester disk system with the XCOMP controller seems to provide more than adequate media access speed and reliability for a multiuser system. Note from the previous assembly time tests (Figure 1) that two users building files at the same time in different areas of the hard disk did not degrade performance at all. The two-user assembly process took less than twice as long as one user, indicating that disk access performance is not generally a problem with multiple users on the NNC hardware configuration.

## Conclusion

OASIS is an absolutely fresh approach to the way that 8 -bit microcomputer operating systems have typically been implemented. The quality of the product is evident in several important areas:

- The quality of documentation allows anyone modestly serious about using a computer in professional applications to get into a productive mode of operation.
- Consistency of the operator interface at all levels of system usage provides for an easily learned system. - Run-time error checking, error reporting, and the availability of the on-line HELP system make it almost impossible for the user to "mess up the system."
- Development tools that are standard with OASIS and optional packages available from the same source provide an OEM software development environment for sophisticated applications not found on other systems with "standard" operating systems.
No, Oasis is not just another operating system. And as a person just introduced to this system, all I can say is that I am impressed at the possibilities. Just for the record, OASIS 16, the 16 -bit version, written in " $C$," will be in distribution by the time you read this evaluation. It promises to be everything that I've said to be true of the 8-bit Z-80 version-and more. Watch for it!

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[^1]
# Enhancing CP/M 2.2 

by Ralph J. Jannelli

## Enhance the performance of CP/M 2.2 in multi-user applications by setting up multiple-user directories.

Several enhancements have been made to CP/M since version 1.4. One of these enhancements, found in version 2.2, is the ability to have multiple user directories-an obvious lead-in to MP/M. However, as implemented, it offers little advantage to the user. In CP/M 2.2 each directory must contain all files that need to be accessed by that user. This is a colossal waste of disk space! Imagine having four or five users each using Basic and/or a word processor and the normal CP/M utility files (STAT, DDT, ASM, etc.). These files must be duplicated for each user on the disk. If each user had his own diskette there would be no need for separate user directories. User directories provide their greatest utility in hard disk environments, which are becoming more prevalent in today's micros. Although a hard disk has many times the capacity of a floppy, why waste disk space?

This article describes a modification to CP/M which may be made to the CCP (Console Command Processor) module, allowing any user to access all the files in user directory 0 . Directory 0 (zero) can now be considered a utility or system directory. Only user specific files will need to be included in the user directory. Example: If I am user 5 and I want to run my Basic application program "SORT.BAS", I simply enter the CP/M command "BASIC SORT". CP/M, under control of the CCP, will search my user directory for BASIC.COM which, however, does not exist in my directory. Normally CP/M would return an error. By intercepting this error and interrogating the current user number a decision can be made. If the current user number is 0 , then no other directory is searched for the requested file; control is therefore passed back to the CCP and the resulting error is sent to the user. If the current user number is not 0 , the current user number is saved, the user number is changed to 0 and the search is re-initiated. If as a result of searching the
user 0 directory the file is still not found, the user number is restored to its previous value and control is passed back to the CCP with the normal "file not found" error as a result. If the file is found in user directory 0 , the file is loaded. After the file is loaded the user number is restored. Control is now passed to the CCP which in turn passes control to the program just loaded, in this case the Basic interpreter. Now the Basic interpreter will utilize the BDOS (Basic Disk Operating System) module of CP/M to search for the applications program SORT.BAS. If the Basic interpreter does not find the file under the current user directory it will return an error message. Note that only files invoked under control of the CCP will cause a search in both the user directory and directory 0.

A further modification to the CCP provides a much more convenient prompt for a multi-user environment. Normally the CCP prompt identifies only the currently logged disk drive (i.e., A> for disk A), but gives no indication of the current user directory. The modification will cause the prompt to be the user number followed by the normal prompt (i.e., 5A > for user 5 disk A).
These changes are implemented by modifying the BIOS (Basic I/O System) module of CP/M. I chose to implement my changes in the BIOS, rather than in the CCP module, because CP/M documentation normally includes a source listing or disk file of the BIOS program, whereas a source listing of the CCP module is not available to the system user. Three jump instructions in the CCP need to be patched, but are not modified until the GOCPM routine of

[^2]Ralph J. Janneili, 101 Cottonwood Dr., Jamestown, NC 27282.

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## Enhancing CP/M 2.2, continued..

the BIOS is executed. The GOCPM routine is executed on both warm and cold boot operations. (Remember that BIOS itself is not reloaded except on a cold boot operation.) The patches are accomplished by loading the new jump address into the HL register and storing HL at the given
location for each of the three patches. The equate statements at the beginning of the program are calculated from the MSIZE given at the beginning of the normal system BIOS program, allowing appropriate relocation of the patched addresses according to the system memory size.


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# The Unbanker 

by Bob Weidemann

## Increasing the system memory space on a two-user system.

Why is it that the solutions to nine of every ten computer dilemmas fall outside the system restraints? While installing an MP/M system into my S-100 system, I discovered that I had a BDOS (Basic Disk Operation System) $161 / 2$ Kbytes long logically, with only 16 Kbytes available physically. Simple arithmetic showed me to be 512 bytes short. My solution is simple and should be of interest to anyone who finds himself a little low on memory, whether he's using MP/M, or CP/M or any other operating systems.

## Background

In a two-user MP/M system, each user has his own bank of memory. The maximum contiguous memory available to each user simultaneously or individually is 48 K . To achieve this, one simply buys two 64 K memory cards and leaves 16 K of chips off each card. Each card is addressed by the 16 address lines of the CPU, and by one more bit supplied by an output port (typically port 40H). The eight bits of the port should only have one bit on at a time, so that only one board (out of a maximum of eight) is on at a time.

The nice part of the scheme is that the I/O port bit is latched, so that you only have to change the bank bit occasionally, such as when the processor services a different user.

The 48 K available to each user is roughly equivalent to a CP/M 56 K environment since the CP/M system would have a BDOS-BIOS area included in it; whereas MP/M's 48 Kbyte is separate from the BDOS-XIOS (as it is called in MP/M environments).

The typical 8-bit microprocessor can address up to 64 K of memory. 16 K remains after we subtract the 48 K in

[^3]either bank. This 16 K is special. It contains the MP/M operating system, and must be available to the processor no matter which bank is currently being used. This 16 K is not banked; it doesn't look at the output port at all. Its physical address is the top 16 K of memory, no matter which bank is on. The other two boards are located in the bottom 48 K of memory and are turned on or off by flipping the bits in the port.

A simple way to implement this 16 K is to use two old 8 K cards that don't have bank select, or that have the bank select disabled. (By the way, most of those old 8K cards will work at 4 MHz even if you did not pay for "high speed" chips-so don't give them away!) Since you're not using bank select, this 16K of memory will always be addressable, regardless of which bank is on.

A better way to implement this 16 K is to put 16 K of chips back onto one of the two banked boards. But this 16 K must be removed from the banking scheme, so that it is always selected.

## The Problem

Remember when you first got CP/M and you decided to improve on the BIOS? Naturally, adding just one more little routine increased your BIOS size, so that you had to decrease your TPA (Transient Program Area). Typically, you did that by pretending your total memory was 1 K less than it actually was, when you constructed (used MOVCPM) your CP/M system. Now suppose you are working with MP/M and your BDOS-XIOS goes just over 16K long. How can you keep a $16+\mathrm{K}$ system in your non-banked memory when you've only got 16 K available? Remember that the SYSTEM must always be in memory, no matter which bank (or user) is on. If you use a portion of the banked memory, you would lose part of your operating system when the "other" user comes on.

After studying the MP/M manual, I realized that others must have the same problem since MP/M provides for a "banked BDOS." This feature allows you to increase your system to over 16 Kbytes. MP/M does this by transferring the overage from bank to bank everytime you change banks. This feature may not be worth implementing because of the CPU time lost in doing the transfers. I did attempt to implement this feature, and suffered increased time delays. I might even have lived with this problem for a while, except that MP/M did not work properly when I invoked the "banked-BDOS" option. Only one user's bank worked correctly. The other bank did not get updated properly. I believe it to be a bug in the MP/M implementation, but I felt that this direction wasn't worth wasting time on.

## My solution

Adding a half-K memory card that is always in the base page of memory (does not bank) deselects (phantoms out) any other memory cards whenever it is addressed. Also, MP/M allows a user to increase his non-banked system area, at the expense of losing that area from every user's memory space. So, the cost of my solution is the loss of one-half Kbyte from the TPA of each user, which is why I am not using the entire 1 K available to me from this board.
It took six chips to implement what I call my "Unbanker" circuit, shown in Figure 1. I had two choices of memory to use, static or dynamic. For this small amount of memory, dynamic would increase the chip count (due to refresh requirements) and would otherwise complicate things unnecessarily. Ideally, I wanted a $512 \times 8$ bit chip. Second
choice would be a $1024 \times 8$ bit chip. Neither of these were readily available, so I was forced to use two very common 2114's ( $1024 \times 4$ ); but I have extra memory for future expansion.
The memory is located from BEOO to BFFF hex. An 8 input NAND gate is used as an address decoder.

## Editor's Note:

Although the circuitry shown works in the author's system, it may present some problems in other S-100 systems. Note the following:

1) If there is another device which can enable the Phantom line (67) then a tri-state gate should be used to generate the Phantom signal. The input to the gate should be grounded and the WRITE* signal used to enable the gate.
2) If memory read problems are encountered due to critical CPU read timing then the READ* signal should be generated by NANDing pDBIN (78), sMEMR (47) and MEM SELECT*

BOB WEIDEMANN is totally immersed in computers. During the day he teaches programming at LaGuardia Community College; in the evening (ever since Altair sold the first S-100 computers) Bob's quest has been to develop the "perfect" $S$-100 system. He has put all this experience to good use by assisting many small businesses with the purchase and installation of microcomputers.

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## Unbanker, continued...

Figure 1.


# Interfacing a Winchester Disk To MP/M 

by Ira Gordon And Karl Wacker

With many manufacturers now advertising hard disks, we could not resist the temptation of interfacing one to an S-100 computer system. We priced the available units, and found that IMI (International Memories Inc.) was offering a 5-1/4", 6.7 Mbyte unit (unformatted), complete with intelligent controller, power supply, and cable set, for $\$ 1,900$. This is the same disk system that Corvus uses in their Constellation System, so we felt it had reached a level of product maturity.

The price was justified because of the hard disk's cost effectiveness over multiple 8" quad density floppy disks yielding equivalent storage. The use of a multi-tasking, multi-user operating system, such as Digital Research's MP/M or Phase One's Oasis, would provide additional cost justification.
The IMI-5000's specifications were very impressive. The rotational speed of the twin platters is 4800 RPM compared to the Seagate ST-506's 3600. The byte transfer rate from drive to controller is 960,000 bytes/second and from controller to CPU is 500,000 bytes/second.
The IMI-5000's intelligent controller also performs automatic sector blocking/de-blocking and track sparing of the disk media. We expected to see at least a four- to five-fold increase in performance over a single density floppy disk drive environment.
We were interfacing the hard disk to a development system using Digital Research's MP/M version 1.1. Application programs were to be written in Pascal MT+ and Z80 assembly language.
The development system hardware consisted of:

- Zobex 4MHz, Z80A CPU.
- Zobex single density floppy disk controller.
- Two SD Systems 64K ExpandoRAM II cards.
- Three Shugart SA800 floppy disk drives.
- Electronic Control Technology Ten Slot S-100 rack mount S-100 chassis with power supply.
- Two ADDS Viewpoint CRT terminals, 9600 baud.
- Power one CP-1 floppy disk power supply.
- Diablo 1355 Daisy Wheel printer with parallel interface.
- S-100 IMI controller interface card. Circuit schematic furnished by IMI.

[^4]- IMI 5007 5-1/4" Winchester drive, with IMI 5000 controller, and IMI power supply module.

The MP/M Extended Input/Output System (XIOS) for the single density floppy-based system was developed by Frank MacLachlan of San Diego, CA under contract to Zobex. The XIOS.SPR, when gensysed with MP/M, came up instantly and performed perfectly.
Additional modifications were made to the floppy-based XIOS to include a list driver routine for the Diablo printer. Separate polling modules were implemented to test the status of the platten, carriage, and wheel signals. This polling technique greatly improved the printer's performance

## Hardware Considerations

The MP/M implementation utilized bank-switched memory. The two SD Expandoram II memory cards, each set up for 48K byte memory partitions, performed perfectly. The Bank-O memory card contained a non-bank switched memory partition located from COOOH to FFFFH. This partition contained the MP/M operation system.

Our desire was to have the entire O/S, including the hard disk drivers, contained in this 16 K byte partitionrather than use the banked BDOS file manager which would reduce system performance

The SD Expandoram II memory cards also required that the XIOS be modified to use port FFH as the bank switch port. Outputting a selected bank number to port FFH would cause that bank to be selected. The Expandoram II has a dip switch which allows for the setting of unique bank addresses.
The Zobex Z80 S-100 CPU card was utilized to support the MP/M environment. It has a built-in prom monitor, located at FOOOH , which contained a debug monitor and disk bootstrap routine. The CPU card, in addition, has the following standard features:

```
- Zilog CTC-used to generate MP/M interrupt
clock.
- Two Zilog darts - 4 ASYNC Serial I/O channels.
- Phantom prom monitor.
- AM9519 interrupt controller.
- Intel 8255 parallel port interface.
- 2 or 4 MHz operation.
```

The Zobex CPU, after executing the MP/M boot program, would phantom the prom monitor and allow the entire

## Winchester Disks, continued...

16 Kbyte memory partition ( COOOH to FFFFH) to be utilized for the MP/M System.

The S-100 interface schematic supplied by IMI (see Figure 1) was found to have three deficiencies. First, the interface would not supply an I/O generated reset signal long enough to properly rest the IMI controller. Second, the IMI design did not use one address line in decoding the I/O address space. Third, separate I/O addresses were used for the four functions of the interface (data to controller, data from controller, status from controller and controller reset).

The first problem was solved by adding a one-shot (74123) and a buffer gate as a pulse stretcher. The second required the addition of another gate to the address decoding logic. The third problem was not serious in this application, and was not implemented.

The IMI 5007 drive has several major differences from other 5-1/4" Winchester drives:

- It rotates at 4800 rpm instead of 3600.
- It has a formatted capacity of 5.73 Mbytes instead of 5.01 Mbytes.
- It has the data separator, the most important part of the read/write logic, on the drive instead of on the controller.
- It uses plated media instead of conventional oxidecoated media.

The IMI 5000 controller operates the drives with 512 byte sectors, but allows you to operate as if you have 128 or 256 byte sectors (this was used to avoid the buffer space needed to do external blocking/deblocking). It also permits you to access the drives by several different methods-including absolute cylinder, head and sector numbering or, as was done in this application, by way of logical sector number. In addition, the drive does automatic track sparing for defective tracks. If the drive develops a bad track, a command sequence is provided to instruct the controller to spare that track. The controller maintains this information on the first track of the drive, using all the records on the track for maximum redundancy. The controller has a useful set of self-test features that help verify that the controller/drive combination is functionally independent of your interface.

A note of caution is in order; the drive, just like any Winchester unit, is sensitive to shock, because the heads rest on the media when the unit is powered down. For this reason, keep the drive in the shipping foam until you have shock mounted it in your system. The drive should be mounted with the disks in a vertical plane, so that if your system is bumped during transport, the heads will not clatter against the media. (IMI has a shock detector inside the drive, and the warranty is void if this has been tripped due to mishandling of the drive.)

The controller responds to the same command set as the IMI controller for the larger 8" drives, except it can only operate two drives instead of eight. The IMI power supply has sufficient capacity to operate both the controller and one 5-1/4" drive.

## Software Considerations

Due to various external factors, the drive was brought up on an MP/M system, which proved to be a blessing in
disguise, as it allowed one user to use DDT to debug the driver software while the other user did normal system operations to test the drive and software.

The S-100 interface and controller were initially tested with DDT. When they performed properly, the driver software was written and incorporated into the operating system.

The actual software consisted of several sections:

- The parameter tables needed by CP/M and MP/M to define the logical characteristics of the drive.
- The software driver for the controller.
- The intercept interface to the existing floppy driver.

The parameter tables were generated first and verified by using the STAT command.

The intercept interface was then written to test for the IMI drive number in the select routine. Then instead of returning to the floppy driver, it jumped to the IMI driver routine.

The IMI software driver did several sub-functions:

- Translation of the sector/track information generated by the operating system into a logical sector number for use by the controller.
- Verified the controller was in a known state by doing a null command, and reset the controller if necessary.
- Load the command block into the controller.
- If doing a write then load the write data.
- Wait for the controller to do the command.
- Verify completion status of the command and do error retries.
- Read in the data if it was a read command.

The actual data transfer was done using the block input and output instructions of the Z80. This type of transfer was not time critical with the interrupts enabled, and proved to be very useful in a real-time environment.

The parameter tables for standard 8" single density floppies and for the IMI are listed below for reference:

| .Floppy |  |  |
| :---: | :---: | :---: |
| defw | 26 | ; \# sectors/track |
| defb | 3 | ; block shift factor |
| defb | 7 | ; block mask |
| $d \in f b$ | 0 | ; extent mask |
| defw | 242 | ; disk size - 1 |
| defw | 53 | ; \# directorty entries - 1 |
| defb | 0 coh | ;alloc 0 |
| $\mathrm{d} \in \mathrm{fb}$ | 000h | ;alloc 1 |
| defw | 16 | ; check size |
| defw | 2 | ; \# reserved tracks (for boot, etc) |
| . IM I |  |  |
| defw | 192 | ; ${ }^{\text {a }}$ pseudo-sectors/pseudo-track |
| defb | 6 | ;block shift factor |
| defb | 63 | ; block mask |
| defb | 3 | ; extent mask |
| defw | 674 | ; disk size - 1 |
| defw | 255 | ; \# directory entries - 1 |
| defb | 080h | ;alloc 0 |
| cefb | 000 h | ;alloc 1 |
| defw | 0 | ;check size |
| defw | 0 | ; \# reserved tracks |

The following is the software listing for the IMI hard disk driver:





Upon completion of the hardware interface and software driver design efforts, we reassembled the XIOS and performed the required genmod and gensys sequences.
The MP/M system was bootstrapped and the following load map appeared on the CRT screen:
$\mathrm{NP} / \mathrm{M} \quad 1.1 \quad$ Loader
$===============$

| Number of consoles | $=2$ |
| :--- | :--- |
| Breakpoint RST | $=5$ |
| 280 CPU Memory | $=$ FFFFH |
| Top of Memory |  |


| Memory Segment Table: |  |  |  |
| :---: | :---: | :---: | :---: |
| SYSTEM | DAT | FFOOH | 01 OOH |
| CONSOLE | DAT | FDOOH | 0200 H |
| USERSYS | STK | FCOOH | 0100H |
| XIOS | SPR | F 300 H | 0900H |
| BDOS | SPR | DFOOH | 1400 H |
| XDOS | SPR | COOOH | JFOOH |

Memseg Usr 0000 H COOOH Bank 01H
Memseg Usr 0000 H COOOH Bank 00 H
The entire MP/M nucleus just fit into the 16Kbyte memory partition on the Bank-O memory card.
The hard disk was assigned as the "D:" drive select, and responded correctly when selected. We proceeded to do a STAT DSK: operation on the hard disk and observed the following:

| 43200 | $:$ | 128 byte record capacity |
| ---: | :--- | :--- |
| 5400 | $:$ | Kilobyte drive capacity |
| 256 | $:$ | 32 byte directory entries |
| 0 | $:$ | Checked directory entries |
| 512 | $:$ | Records/extent |
| 64 | $:$ | Records/block |
| 192 | $:$ | Sector/track |
| 0 | $:$ | Reserved tracks |

The next step in our testing phase required that we write and then read files to and from the hard disk. The PIP program was used to perform this operation. We copied most of the files (assembler, source, DDT, etc.) from the floppy drives. This worked correctly. The final test came when we assembled the XIOS directly on the hard disk itself. All was indeed well. STAT was used to verify that the storage space on the disk decreased or increased correctly when files were created and deleted.
The performance that was observed when we assembled the XIOS on the hard disk as compared to doing it on the floppy was approximately a 5 to 1 speed improvement.
Complete software details and listings for interfacing the IMI hard disk to the Zobex single or double density systems are available on 8 " media from the author; 6 Lenox Road, Farmingdale, New York 11735.

# The Best Boards SD Prices Slashed ! ! 

4 MHz Z-80A CPU, 64 K RAM, serial I/O port, parallel I/O port, double-density disk controller, CP/M 2.2 disk and manuals, system monitor, control and diagnostic software.
-All boards are assembled and tested-

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Extensive application notes concerning how to operate the ExpandoRAM III with Cromemco, Intersystems, and other popular $4 \mathrm{MHz} \mathrm{Z}-80$ systems are contained in the manual.
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$\$ 495.00$ MEM-65128A 128 K A \& $T$ MEM-65192A $192 \mathrm{~K} A$ \& $T$ MEM-65256A 256 K A \& $T$ $\$ 639.95$ LM-65256A $256 K$ A \& $T \ldots \ldots \ldots$. $\$ 879.95$

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SBC-200, 256K ExpandoRAM III, Versafloppy II, MPC-4 COSMOS Multi-User Operating System, C BASIC II

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 ports with independently programmable baud rates and vectored interrupts, parallel input port, parallel output port, 8 counter/timer channels, real time clock, single and double sided/single or double density disk controller for $51 / 4^{\prime \prime}$ and $8^{\prime \prime}$ drives, up to 36 K of on-board ROM, CP/M 2.2 compatible COSMOS interrupt driven multi-user disk operating system, allows up to 8 users to run independent jobs concurrently, C BASIC II, control and diagnostic software in PROM included.-All boards are assembled and tested-
MPC-4
Intelligent communications interface


- Four buffered serial I/O ports - On-board Z80A processor - Four CTC channels Independently programmable baud rates • Vectored interrupt capability - Up to 4 K of onboard PROM - Up to 2 K of on-board RAM • Onboard firmware
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# 㓌101コ Computer Products 

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# Digiac CT-810 Multi-User Support Module 

by Dennis Thovson

What capabilities and features should you look for in an I/O board? The answer to that question depends on your application. For example: How many peripheral devices (printers, terminals, modems, etc.) are required? Which of these devices require serial ports? Parallel ports? Do any of these peripherals require handshake signals such as RTS/CTS? Do you require interrupt capability, or is the program I/O sufficient? Is software control of parameters such as baud rate necessary? Any or all of these features and more can be obtained with I/O boards readily available today-for a price. Which brings us to the Digiac CT-810 Multi-User Support Module, an S-100 board designed expressly for systems running under Digital Research's MP/M operating system. This board provides the essential I/O features required by MP/M, plus some convenience operations that make life a little easier for the user.

First the basics. The board provides four RS-232C serial ports ( $75-19,200$ baud) plus one input and one output parallel port. In addition, the board contains a clock which can be programmed to provide an interrupt every 16.7 milliseconds (or optionally, 33 milliseconds) as required by MP/M for task-switching and time-of-day functions. Also available are provisions for an on-board EPROM (2708 or 2716) and the necessary circuitry to jump-on-reset to the EPROM. Extended address capability is provided through an output port which controls address bits A16-A19. Now let's look at each of these major functions in a little more detail.
This is a hardware-configurable board with no provision for software control of the serial ports. All options are selected by jumpers on the board. Of the many options

[^5]available, most are preselected on the board as received from the factory-except the baud rate for each serial port which must be selected by the user. (An advantage of hardware optioning such as used on this board is that no software initialization of the UARTS is required on power-up.) The port addresses on the board as delivered occupy a block from 80 H through 87 H . The block of port addresses can be changed to occupy any eight consecutive ports starting on either an X0 or X8 hex boundary ( $\mathrm{X}=0$ OFH). There are essentially no provisions for any RS-

> The Digiac CT-810 provides the essential I/O features required by MP/M, plus some convenience options that make life a little easier for the user.

[^6]This is the only interrupt generated by this board-the I/O ports do not generate interrupts. The interrupt rate can be selected to provide either 60 Hz ( 16.7 msec .) or $30 \mathrm{~Hz}(33.3 \mathrm{msec}$.) interrupt intervals. In either the 8080 mode or the Z80 mode two interrupts can be used with the clock. The board also contains a counter which counts the unacknowledged interrupts. This provides a method for MP/M to keep its time-of-day clock accurate when a high priority interrupt, such as a disk operation, prevents acknowledging the clock interrupt for a few "ticks." The MP/M XIOS clock routine simply reads the counter (which automatically resets it to zero) and corrects the tick count accordingly.

The on-board EPROM, which is not provided, is normally addressed at 0FCOOH (optionally OF400H) for a 2708. The board contains a jump on reset to this location. Main system memory at 0 and that which may overlap the EPROM address space must respond to a Phantom signal from the board for these features to work properly. The EPROM can be made to disappear from the system address space by an output to port 87 , and will remain out of the address space until the next system reset. Options are provided to change the EPROM address to 0 FOOOH or OF800H to accommodate a 2 K 2716 (the jump on reset address can also be changed). Or, the EPROM and jump on reset can be permanently disabled if desired.
The CT-810 provides the features required by MP/M which may, in other implementations, require multiple boards (e.g., clock and extended addressing). It is an ideal board for systems which can be set to a given
configuration at installation, and not require the flexibility provided by software control of its I/O functions. This is probably true of the majority of business systems in which MP/M is used.
Physically, the board appears to be well laid out and of good quality. The only minor complaint I have is that all option jumpers require soldering, although it looks like there is enough space available on the board to have provided some other method of optioning, particularly the baud rate selection. I have used the board in a Z80 system running a 4 MHz for about one month with no problems. It does everything it is advertised to do without fuss or bother. I did not use the extended address capability of the board, but I have every reason to expect it works as stated. The unacknowledged interrupt counter is a simple but clever way to get around the annoyance of the time-of-day clock running late, as in a typical MP/M system which disables interrupts during disk read and write activity. It worked nicely in my system. The manual furnished with the CT-810 is complete and relatively good. However, it appears to have been written by an engineer for an engineer (which may be appropriate for a hardware products such as this). This is a definitely not a manual for someone unfamiliar with microcomputer hardware.

The CT-810 is available from the Digiac Corporation for $\$ 319$ assembled and tested. Digiac also makes a full line of S-100 boards-CPU, memory, disk controllers, etc.-as well as complete systems that are ready to run. They are located at 175 Engineers Road, Hauppauge, NY 11788, telephone: (516)273-8600.
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## Hardware Product Review

# The CompuTime/QT Clock Boards 

by Leo Biese and Emilio Iannuccillo


#### Abstract

At last fall's Boston Computer show we picked up what surely seemed a good bargain-a couple of QT "S100Clock/Calendar+" kits (List \$100 a kit/\$150 A/T). Unfortunately, it turned out that the bargain boards did not quite work as implied by the designation " $\mathrm{S}-100$," since they don't work with an 8080 CPU that meets the IEEE696 standard! A letter to Don Smith, President of Q.T. Computer Systems, Inc. went unanswered for nearly one and a half months and, when received, indicated that he was unaware of this problem and would be interested in hearing about our fix. By this time the present review was underway and we did not follow-up his letter. While we were waiting for an answer we had noted the external similarity of the CompuTime ComputerWatch (their name is also on the QT board in small print, a point which we missed the first time around) and contacted them for further information. CompuTime president Gail Beaver was most helpful and kindly supplied their current board (marked S-100 880 REV B) for evaluation. CompuTime turned out to be the manufacturer of both boards and was well aware of the incompatibility problem, having revised the whole board some time ago. We will discuss the incompatability in this review, since many of the earlier versions are still around.


## The Board

This full-function clock board is remarkably simple and requires only a backup battery and few support chips for the OKI MSM5832 monolithic "Microprocessor RealTime Clock/Calendar" chip. This 18 -lead CMOS integrated circuit contains its own oscillator and divider chain, 13 four-bit I/O registers for the seconds, minutes, hours, day-of-the-week, date, and year as well as the required chip-select, read, write, and test circuits and a $+/-30$ sec. correction feature we use programatically. A "hold" input maintains the time while preventing rollover of the clock during a read. Leap year correction is automatic, and

[^7]either 12-or 24 -hour time format can be selected. Details of the registers are covered in the documentation and need not be discusssed here. The board requires four consecutive I/O ports which can conveniently be selected by a DIP switch over the entire range of $0-255$.

> This full-function clock board is remarkably simple and requires only a backup battery and few support chips for the OKI MSM5832 monolithic "Microprocessor Real-Time Clock/Calendar" chip.

[^8]have been a considerable enhancement to have the board designed so that the alternate power sources were more closely matched. One of the boards tested lost about ten seconds per day despite repeated "tweaking" of the variable capacitor. The second board lost over an hour when it was removed from the computer for about two months.

A significant design flaw is the use of a horizontal access trimmer capacitor. Since the oscillator must be touched-up daily over a period of a week or more to maintain accuracy, the board has to reside atop an extender board until this is done. A top-mounted capacitor would have been better.

> In addition to the basic clock/calendar function of the 5832 chip, the CompuTime/QT boards provide four hardware interrupt times at one hour, one minute, one second, and one millisecond (approximately) which are potentially useful in real-time process control if the board is kept activated.

In addition to the basic clock/calendar function of the 5832 chip, the CompuTime/QT boards provide four hardware interrupt times at one hour, one minute, one second, and one millisecond (approximately) which are potentially useful in real-time process control if the board is kept activated. As long as the computer is turned on, the accuracy is very good; not a single second was lost during a six hour session with the National Bureau of Standards (WWV) time signals coming into the computer room. Accuracy suffers only when the computer is turned off and the board goes into the 3.6 volt stand-by mode.
The board as supplied is clean, solder-masked, silkscreened and quite up to current manufacturing standards. There is plenty of kludge area available for your own special projects. The 35 page manual supplied is, if anything, too simply written and redundant-the register descriptions are presented in the theory of operation, in the programming section, and again in the appendix. The schematic is poorly done, but usable. Potential users would benefit by obtaining the OKI MSM5832 data sheet which is not supplied. Board-level manufacturers should follow the lead of the disc-controller providers and include the data sheets for "uncommon" chips with their documentation, since these can sometime be very difficult to obtain.
Several redundant sample programs in Basic are provided in the manual to set and read the clock, but we prefer our own version given in Listing 1. The program, "SETCLOCK," allows the clock to be synchronized with the national standard when accurate time measurements are needed. The U.S. National Bureau of Standards broadcasts time signals continuously on the 2.5, 5, 10
and 15 MHz shortwave frequencies that are readily received by even the most simple receiver anywhere in the continental U.S. (station WWV) and in the Pacific (station WWVH in Hawaii). In addition, the Canadian government also broadcasts universal time signals over its CHU channels on $3.33,7.335$ and 14.67 Hz . The details of the format for these signals can be found in any one of the many amateur radio or shortwave listener's handbooks. Essentially, the world-wide time standard is kept very accurately and announced by a distinctive tone on the second, and by a voice on the minute. SETCLOCK is selfprompting, and makes use of the $+/-30$ second adjust input (pin 15) provided on the clock chip. When pulsed high, this pin zeroes the seconds counter and, if over 30 seconds are on the clock, also adds one minute. First you must set the Year, Month, Day/Date, and Hours according to a menu selection, you are then advised to set the clock ahead at least one minute. Unlike the programs supplied with the board, the time is always visible on the screen (by using the direct cursor addressing of the ADM3a and similar terminals) while entries are being made. At this point you simply wait for the minute mark and hit the return key. We use a compiled version of this program. The delay (Line 1490) can be adjusted so that Line 950 rings the terminal bell synchronously with the time signals.
The main use we have for this board is to print the date on program listings and runs, thereby getting rid of some of the confusion we have been living with over the years (since we never can remember when anything was printed). While the Basic programs provided are adequate, we


## CompuTime/QT Clock Boards, continued...

also wanted this facility for assembly language listings and developed the program PTIME as a CP/M transient command given in Listing 2. Constant paranoia about whether or not the clock was correct led to a nearly identical program, directed to the console, which we incorporated into our CPM as an auto-load program (See cf. James J. Franz, "Turn-key CP/M Systems," Creative Computing, December 1979). With this modification, the time and the date is printed right below the $\mathrm{CP} / \mathrm{M}$ sign-on message each time the system is brought up, and whenever a warm start is done. This allows, for example, correcting the clock if we have been on vacation and would have forgotten to reset it before printing.

## Problems

The inability of this " $\mathrm{S}-100$ " board to work with many 8080 CPUs reminds us again that if the manufacturer doesn't say the board conforms to the IEEE-696 standard, it almost certainly doesn't and the potential user should proceed with caution.

Refer to this quote from the standard:
"2.2.3 Status Bus. The status bus consists of eight lines which identify the nature of the bus cycle in progress, and qualify the nature of the address on the address bus."

One of the the status signals is sOUT. This signal, according to the standard, indicates the type of I/O in progress. Nowhere in the standard does sOUT 'time' the type of I/O.

Another excerpt from the standard:
"2.7.5.2 The Write Strobe. The generalized write strobe, $\mathrm{pWR}^{\star}$, is used to write data from the data bus into the addressed bus slave..... Data out on the data bus must be guaranteed valid for a specified period both before and after the activation of the write strobe. Hence, either the leading or the trailing edge of the write strobe may be used to strobe data into the addressed slave."

Herein lies the problem with the QT board (and the earlier CompuTime version). The design completely ignored the IEEE standard relating to the pWR* strobe, and does not even have that signal coming into the board. Instead, it uses the sOUT signal not only to indicate an OUT operation to the board, but also (and improperly) to time the data onto the board. Consequently an 8080, such as the Imsai which produces valid IEEE signals, cannot strobe the power data into the clock board. The 8080 needs both pWR* and sOUT to operate properly. The sOUT signal is latched by the 8212 (on the CPU board) from long before until long after the data is valid, but the pWR * signal is needed to indicate the period when the data is valid.

These timing problems should be obvious from the diagrams supplied by the IEEE standard and the CPU manufacturers. (We will not reproduce them here.) The pWR * signal is active for a much shorter time than sOUT. The clock board latches trigger on the release of sOUT; by this time pWR* has already gone away and the data is no longer stable. (For the non-hardware types, this means
that you set the clock correctly, and the next day, it reads something ridiculous like: "December 66, 1999 18:48:91 PM"-because the data wasn't caught, or latched, at the proper time in the CPU cycle.)

So why does it work with the Z80? It just so happens that the sOUT signal from the $Z 80$ occurs at just about the same time as the pWR * signal. The $\mathrm{Z80}$ has both signals and they look about the same. The Z80, however, does not latch the sOUT signal - in fact, the Z80 does not need to latch any signals, reminding us that while it may run 8080 code, the $Z 80$ is an entirely different chip!

Note: This problem does not apply to the "Revision B" board supplied by CompuTime. They have added an extra chip (U12) to pick up pWR* in a manner very similar to our Mod-2 below; the difference being that they AND pWR* with sOUT one step later. In addition they have provided pads for connection to the bus interrupt lines.

## Modifications

There are several ways to modify the board to make it IEEE compatible. (Note: while this article was in progress a board fix, without comment, was published by Zoso in Lifelines Vol.1, No.10. It is rather cryptic to say the least.)

Figure 1: Modification \#1; This requires no additional components but sacrifices the interrupt timers.


MOD \#1 (Figure 1): We had no need of the interrupt features, so the fix was quite easy, mainly because we then had $1 / 2$ of U3 (7421) available as well as all of U2 (7401) and a section of U9 (7404).

1. Cut the trace from Bus \#45 (sOUT) to U6 $(11,13)$.
2. Cut the trace leading to U9 (5) at the chip.
3. Cut the traces to $\cup 2$ (9) on both the top and bottom of the board next to the chip.
4. Run a wire from Bus \#77 (pWR*) to U9 (5).
5. Connect Bus \#45 (sOUT) to U2 (9).
6. Connect pad $C$ to U9 (1).
7. Connect U9 (2) to U6 $(11,13)$.


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## CompuTime/QT Clock Boards, continued...

MOD \#2 (Figure 2): If you desire to keep all functions of the board intact you will have to add a gate. We used a 72 LSO 2 and called it U12.

1. Tie $\cup 12$ (14) to +5 volts and ( 8 ) to ground.
2. Cut the trace from $\mathrm{U} 6(2)$ to $\mathrm{U6}(3)$ on the solder side of the board.
3. Cut the trace from U 6 (10) to U 6 (4). This trace is on the component side under the socket. It must be done before assembly or the socket will have to be removed.
4. Tie U12 (2) to Bus \#77 (pWR*).
5. Tie U12 (3) to U1 (9).
6. Tie U12 (1) to U6 (10 and 2).

Figure 2: Modification \#2; All functions of the original board can be retained by adding a gate (U12).


## Summary

To reemphasize, the modifications pertain to the QT and earlier CompuTime boards only; the current CompuTime revision B works perfectly as is. Despite the problems we encountered, we consider each of the boards to be a bargain and a valuable addition to the system. After approximately six months of use, it is hard to think of using a computer without them. The assembled and tested boards are the same price but you can save $\$ 25$ by getting the QT kit and making the changes suggested here.

For real-time process control the boards are highly accurate and it seeems hard to justify some of the other clock boards currently on the market for several hundred dollars. Indeed, Gail Beaver at CompuTime tells us that this is a major use of their board; for everything from timing rides at amusement parks to controlling grain elevators in Australia!

As a simple time/data board, it is a 'must' for every S100 bus computer. Any sort of billing or reporting use of the microcomputer, such as a professional practice, requires the addition of at least a date-and many types of reports also require a time entry as well. This facility has long been standard on virtually all mini- and mainframe computers and is now available for the micro user at a reasonable cost.

For more information contact:
Compu/Time, P.O. Box 5343, Huntington Beach, CA 92646; (714)536-5000.

QT Computer Systems, Inc., 15620 Inglewood Ave., Lawndale, CA 90260; (800)421-5150.

OKI Semiconductor, 1333 Lawrence Expressway, Suite 104, Santa Clara, CA 95051.


```
00 'SETCLOCK: Program to set the parameters of the Computime/QT
100
10',
30 'Programed in Microsoft 5.2 BASIC by E.D.I and L.P.B. based
140 'on the manuals supplied (November 1980)
150, 2/01/81 Revised for better screen presentation and a more rapid
70 ; keyboard scan approximating realtime seconds. (LPB)
90. 2/14/81 Input for 'seconds' correction eliminated since BASIC
    2/14/81 Input for 'seconds' correction eliminated since BA
    is not fast enough
' 6/06/81 Universal time 'SYNC' revised with added prompting (LPB)
l========= SET PARAMETERS AND STORE TEXT FOR OUTPUT
CLEAR.SCREENS=CHR$(26) 'Clear ADM3a screen code
RING.BELL$=CHR$(7) 'Ring ADM3a terminal bell
ADDR=130 
290 KEYBOARD=17 'System (MITS 2SIO) port
300 DIM DAY$(6),MONTH$(12),PROMPT$(13),T(13),T$(13),US(13)
310 FOR I=0 TO 6: READ DAY$(I): NEXT
2@ FOR I=1 TO 12: READ MONTH$ (I): NEXT
340 DATA SUNDAY,MONDAY,TUESDAY,WEDNESDAY,THURSDAY,FRIDAY,SATURDAY
30 DATA JANUARY,FEBRUARY,MARCH,APRIL,MAY,JUNE,JULY,AUGUST
360 DATA SEPTEMBER,OCTOBER,NOVEMBER,DECEMBER
70 DATA MINUTE UNITS,MINUTE TENS,HOUR UNITS,HOUR TENS
380 DATA DAY OF THE WEEK {Sunday=g Monday=1 Sat=6}
9\emptyset DATA DAY UNITS,DAY TENS,MONTH UNITS,MONTH TENS
O@ DATA YEAR UNITS,YEAR TENS
4 1 0
2Ø PRINT CLEAR.SCREEN
430 PRINT TAB(12);
440 PRINT" -------
450 PRINT TAB(12); ;
470 PRINT TAB(12);
80 PRINT"
90 PRINT TAB(12); MINUTES #3 för DAYS #5 for YEARS |"
```



```
20 PRINT"। #2 for HOURS #4 for MONTHS #5 to SYNC
540 PRINT"!
550 PRINT TAB(12);
560 PRINT"|
50 PRINT TAB(12);
50 PRINT"
590 PRINT TAB(12); |"
6@\varnothing PRINT"। Do NOT use CTR/C to end as it may stop the clock |"
610 PRINT TAB(12);
620 PRINT
630 PRINT TAB PRINT TAB(12);STRINGS(54,"=")
650 '================== READ THE CLOCK REGISTERS ==========================
6 6 0 ~ ' T h e ~ c l o c k ~ r e g i s t e r s ~ c a n ~ b e ~ r e a d ~ d i r e c t l y , ~ u n f o r t u n a t l y ~ w e ~ n e e d ~
70 'to change them to ASCII text for the printout. Converting puts
80 'in an obligatory leading blank (the implied sign) which must be
90 'stripped off.
700 ',
710 :'Variables used:
750, T$(x) = ASCII string values of the registers for printout
760
\begin{tabular}{|c|c|c|}
\hline 780 OUT & DAT, 16 & 'Stop the clock \\
\hline 790 I=ø & & 'Set Register counter \\
\hline 800 FOR & \(\mathrm{D}=32\) TO 44 & 'For all registers \\
\hline 810 & OUT ADDR, D & ', point to register \\
\hline 820 & \(\mathrm{T}(\mathrm{I})=\mathrm{INP}(\mathrm{ADDR})\) & , read it \\
\hline 830 & \(\mathrm{I}=\mathrm{I}+1\) & - bump the counter \\
\hline 840 & NEXT D & ' and get the next \\
\hline 850 OUT & DAT, 0 & 'Now restart the clock \\
\hline \[
860 \text { '- }
\] & Each pass thru the read routine checks and the \(12 / 24\) hour format request & for a leap year flag \\
\hline 876 IF & T(8)>3 \(\mathrm{THEN} \mathrm{T}(8)=\mathrm{T}(8)-4\) & 'Adjust for FEB 29 \\
\hline
\end{tabular}
```

940 PRINT CHR (27) +CHR (61) + CHRS (43) + CHR\$(53) 'set cursor
950 PRINT RING. BELL\$ 'Tick seconds
960 PRINT
976 PRINT TAB(14)"today is "; DAY§(T(6));" ";

1010 PRINT
1月2』 PRINT TAB(12);STRING\$(54," =")
1030 PRINT
1040 $1=================$ CHANGE THE CLOCK REGISTERS $=====================$
1050 '--- Check keyboard for input
$1060 x=$ INP (KEYBOARD)
$1070 \mathrm{X}=\mathrm{X}$ AND $127-48$
$1080 \mathrm{IF} \mathrm{X}\langle>6$ THEN 1100
$1090 \operatorname{PRINT}$ TAB(12)"SYNC: Hit return just BEFORE zero tone ";:GOTO 1480
1160 PRINT TAB(12)"Enter function \#
1110 ON X GOTO $1140,1150,1190,1230,1240,1480,1520$
1120 GOTO $780 \quad$ 'Reprint clock till keypressed
1130 '--- Response to keboard entry:
$1140 \mathrm{X}=3$ : PRINT: PRINT TAB(7);:GOTO 1260
'Get minutes
1150 PRINT

$\begin{array}{lll}1170 & \text { IF PM }=\text { "PM" } & \text { THEN } P M=-1 \text { ELSE PM= } \\ 1180 & \text { GOTO } 1260 & \end{array}$
1190 PRINT: PRINT
$1200 \mathrm{X}=8:$ INPUT"
1200
1210 $\quad$ IS THIS LEAPYEAR "; LEAPS
$1220 \begin{array}{ll}\text { ELSE LEAP }=\varnothing & \text { GOTO 1260 } \\ & \text { Flag it }\end{array}$
$1230 \mathrm{X}=10$ : GOTO 126の 'Get month
$1240 \mathrm{X}=12:$ GOTO 1260 'Get year

910 ＇－－－Change numeric register data to string and strip off the

$\qquad$

1250 ＇－－－－－－－Data input for the clock registers
1260 PRINT：PRINT TAB（8）；PROMPT $\$(\mathrm{X})$ ；
1276 INPUT $Y$
1280 IF $X=5$ AND PM THEN $y=y+4$
1290 IF $X=8$ AND LEAP THEN $y=y+4$
1290 IF $X=8$ AND LEAP THEN $Y=Y+4 \quad$＇Send it
1300 GOSUB 1400
1310 ＇－－－Return and get the next register．We load them backwards
ie．tens and then units
$1320 \mathrm{X}=\mathrm{X}-1$
1330 PRINT TAB（8）；PROMPT $\$(x)$ ；
1340 INPUT Y
1350 GOSUB 1400
＇Send it
1360 IF $X=7$ THEN GOTO $132 \emptyset$
$137 \emptyset$ OUT DAT，$\varnothing$
＇User wants to synch the clock
1380 GOTO $42 \varnothing$

［LOG：JULY 13，1981 11：34：67 PM］
－PTIME：Prints time and calendar on the CP／M console（ADM3a）
；and lister（Diablo 164ø）using the Computime／QT clock board
；By Emilio D．Iannuccillo， 825 Hope St，Bristol，R．I． 62809 January 1981
；Restructured by L．P．Biese，Hill，N．H． 03243 May 24， 1981

；INITALIZE．Program begin here．Save old CPM stack for
；re－entry to system at conclusion of the program

| ORG | 100H | ；beginning of CPM TPA area |
| :--- | :--- | :--- |
| LXI | H， | ；clear HL |
| DAD | SP | ；load with CPM stack pointer |
| SHLD | RETURNSTACK | ；and save it． |
| LXI | SP，STACK | iset up our own stack |

；RAISE CLOCK HOLD LINE to stop the clock from advancing

| MVI | A，HOLD |
| :--- | :--- |
| OUT | ； |
| CLOCKDATA | ；and send it |

－READ Clock data．set up a loop to latch the clock ；addresss，read the data and save

L1：

| MVI | B，32 | ；Set B for 0 ，the first <br> ；clock register＋ 32 （for read） |
| :---: | :---: | :---: |
| MVI | C， 13 | ； n umber of registers |
| LXI | h，TIMETABLE | ；Area to store raw data |
| MOV | A，B | ；Start of the read loop |
| OUT | CLOCKADDRESS | ；Output \＆latch register wanted |
| PUSH | PSW | ；Need 6 microsec delay at 2 mh for |
| POP | PSW | ；clock chip to catch up |
| IN | CLOCKDATA | ；Read the register |
| MOV | M，A | ；Store it |
| INX | H | ；Bump storage location |
| INR | B | ；Bump to next register address |
| DCR | C | ；One less to go！ |
| JNZ | L1 | ；Get the next one |
| XRA | A | ；Done． |
| OUT | CLOCKDATA | ；Restart clock |

；CONVERT raw data just read into asci and stuff it
；into a print buffer for later output to devices

|  | LXI | h，Timetable | ；Start of raw data |
| :---: | :---: | :---: | :---: |
|  | MOV | A，M | ；Pick up seconds |
|  | ORI | 30 H | ；Convert to ascii |
|  | STA | S1 | ；Store at proper point in |
|  | INX | H | ；print buffer |
|  | MOV | A，M | ；Pick up tens digit of seconds |
|  | ORI | 30 H | ；Convert to ascii |
|  | STA | S10 | ；Store in print buffer |
|  | INX | H | ；Advance to minute units |
|  | MOV | A，M | ；Get it |
|  | ORI | 30 H | ；Convert it |
|  | STA | M1 | ；Store it |
|  | INX | H | ；minute tens |
|  | MOV | A，M | ；Repeat |
|  | ORI | 30 H | ；for |
|  | STA | M10 | ；minute tens digit |
|  | INX | H | ；oh，hum |
|  | MOV | A，M |  |
|  | ORI | 30 H |  |
|  | STA | H1 |  |
|  | INX | H | ；ah，hour tens，a little |
|  | MOV | A，M | ；more interesting because it |
|  | ANI | 3 | ；contains am／pm or 24 hr flag |
|  | ORI | 30 H | ；First set to ascii and |
|  | CPI | 30 H | ；Check to see if it is a 0 |
|  | JNZ | OVER6 | ；Go forward if not a 0，else |
|  | XRA | A | ；wipeout $\emptyset$ for sake of print looks |
| OVER6： | STA | H2 | ；Store it |
|  | MOV | A，M | ；Get hour tens data again |
|  | ANI | 8 | ；check if 24 hr time |
|  | J2 | NOT 24 HR | ；Go forward if not 24 hr ， |
|  | XRA | A | ；else if it is 24 hr format |
|  | STA | AMSPM | ；then wipe out $A M$ in the print |

CompuTime/QT Clock Boards, continued.


# Dual Systems Clock/Calendar Board 

by Ray Duncan

The CLK-24 from Dual Systems Control Corp. (1825 Eastshore Highway, Berkeley, CA 94710, 415-549-3854) is an S-100 board which can be interrogated by the computer to obtain month, day, year, day of the week, hours, minutes, and seconds. It can also generate vectored interrupts on every 0.97 msec , second, or hour. The board is I/O mapped and occupies two port addresses which are switch-selectable.
The board, which costs $\$ 250$, is cleanly laid out and well constructed. The CLK-24 is based on the OKO Semiconductor MSM5832 CMOS chip, a derivative of the circuits used in digital watches. The clock interface is very simple, consisting of eleven integrated circuits, a few discrete components and a crystal oscillator. A particularly nice feature of the board is an on-board battery backup. Two penlight batteries continue to supply power to the clock chip when the microcomputer is turned off.

Setting and reading the clock is straightforward from either assembly language or Basic. Detailed examples in Basic are provided in the user manual which, when implemented, proved to work correctly without modification.

The manual consists of nine photocopied pages (including diagrams), and gives intelligible and well-organized

[^9]guidance on the use of the board. Unfortunately, it does not include any technical information or a schematic.

My field is microprocessor applications for laboratory and medical environments, and many of them need a reliable time base for data collection. I have tried most of the advertised S-100 clock and calendar boards and found them to be erratic to various degrees. In contrast, the

> The CLK-24 board has been reliable, accurate, and easy to use. It has weathered all sorts of power fluctuations and interruptions without ever losing or altering the time and date.

CLK-24 board has been reliable, accurate, and easy to use. It has weathered all sorts of power fluctuations and interruptions without ever losing or altering the time and date. I would recommend this module to Microsystems' readers without any reservation.

## A Timestamp For CP/M

by Chris Terry

## A low-cost S-100 clock/calendar circuit and CP/M BIOS driver software.

## Introduction

Although this article covers some of the same material as Fred Deadrick's clock/calendar article in the July/August 1981 issue of Microsystems, it breaks new ground in three areas:

- Discussion of generalized I/O ports circuitry.
- Alternative (and somewhat lower cost) interfacing to the MSM5832 clock/calendar chip.
- Modification of the CP/M BIOS to produce a date and time upon cold boot. The routine for this can be accessed by application programs.
Fred Deadrick's article describes an interface dedicated to one particular peripheral. The chip count is low and it presents no problems in construction. However, the 8131 magnitude comparator is becoming difficult to find; I have not seen this or the 8833 bus driver/receiver quoted in any advertisement anywhere in the last few months. Also, it has been my experience that a wire-wrap board, once purchased, gets used for a number of different interfaces, some of which become a permanent part of the system. Others are purely experimental and are removed (or at least disabled) when the experiment is finished. Thus, it is an advantage for as much of the circuitry as possible to be shared among the I/O ports, to avoid duplication.

In this article I shall therefore present the basic address decoding and strobe circuits for eight input and eight output ports. All of the chips are readily available at prices between 25 cents and $\$ 1.50$ from mail order houses such as Digi-Key or Jameco. Once the logic is understood, it can be implemented with chips other than those specified. None of these circuits are new-in one form or another, they can be found on almost any S-100 interface board on the market. However, it has been some time since any general article on interfacing has appeared, and I hope that newcomers to the S-100/IEEE-696 bus may benefit from the ideas and go on to bigger and better hardware experiments. Those who are already expert interfacers can skip right to the logic diagrams and software description.

## Interface Circultry

A complete interface can be functionally divided into three parts: the computer side, the peripheral side and the software. The computer side consists of the address decoding and strobe generation circuits. These are identical in form, regardless of the type of peripheral, and can therefore be common to all I/O ports on the board. The peripheral side consists of data and control registers for input and output; the number and timing of these depends on the requirements of each individual peripheral. Some peripherals may also require signal level converters to


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## Timestamp For CP/M, continued...

be interposed between the registers and the device (e.g., TTL/RS232 drivers and receivers). As an illustration of the device side, I shall describe an assembly of flip-flops and tri-state buffers to control and read the MSM5832 clock/calendar chip. As an illustration of the software required, I shall describe a routine for incorporation into the CP/M BIOS so that the sign-on message (at cold boot) contains the current date and time, and a corresponding transient program for setting the date and time.

## Address Decoding

Since we are considering a block of eight consecutively numbered ports, the common address circuitry should decode the upper five address lines (A7 through A3) to generate a board ENABLE signal. The three low-order address lines are decoded by strobe generation circuits to produce an input or output strobe for each of the eight ports. Conceptually, the simplest way to generate an ENABLE* is to wire the address lines (directly or through inverters) to five inputs of a 74LS30 8-input NOR gate (see Figure 1). However, changing the address of the first block of the port is then a problem, because DIP switches cannot be used-they are single-pole, singlethrow switches that are either on or off. The scheme of Figure 1 requires jumpers from the gate inputs to the direct or inverted address lines. And while jumpers are feasible, they are inconvenient. With the jumpers shown, the port addresses are from 60 H through 67 H .
A more convenient method of decoding is to use a magnitude comparator such as the DM8131 (see Figure 2). This chip compares six bits. The level on the $B$ inputs is set by the switches and pull-up resistors; an open switch allows the associated resistor to pull the corresponding B input high. The chip produces an active-low ENABLE* signal if-and only if-the bit pattern on the address lines matches the pattern set into the switches (again, 60 H through 67 H ). Since we are only applying five address lines to the $A$ input, the $A 6$ and $B 6$ inputs are both tied to ground so that they always match. (They could also both be tied to +5 V .)
As mentioned above, you may not be able to obtain the DM8131. One alternative is to cascade two 4 -bit magnitude comparators such as the 74LS85; another is to use exclusive-NOR gates such as the 74LS266 or 74L288 with open-collector outputs wired together (see Figure 3). Each section of the chip produces a low output if the two input lines are at different levels. If both inputs are high or both are low, the output of the chip is high. Since all five chip section outputs are hard-wired together, a line/switch mismatch on any one address line pulls the common output line low; the ENABLE line is high only if the bit pattern on the address lines matches the pattern set into the switches. Again, an open switch matches a high address line. The open-collector chip is preferred over the standard totem-pole chip for applications in which gate oútputs are to be wired together, because the internal impedance of the totem-pole may be too high to pull several gate outputs below the 0.8 V logic 0 threshold reliably. If an active-low ENABLE* signal is required, another section of chip G2 can be used as an inverter, as shown, or a spare section of a 74LS04 hex inverter chip may be used instead.

Figure 1: Address Decoding with Gate.


Figure 2: Address Decoding with Magnitude= Comparator.


Figure 3: Address Decoding with Switched Exclusive NOR Gates (Open Collector).


## 64K STATIC RAM BOARD FOR S-100 BUS \$470



## Timestamp For CP/M, continued...



## I/O Strobe Generation

A convenient method of generating I/O strobes is shown in Figure 4. A strobe is a pulse that can be used to open a set of gates for a limited time, or to load a register with data. This register may be a single flag bit that is set or reset to indicate some condition, or it may have multiple bits to hold some pattern such as a binary number or an ASCII character. In this particular article, we shall be considering an input strobe as a means of opening gates to transfer several bits of data from the peripheral (the clock chip) to the S-100/IEEE-696 DATA IN bus; and an output strobe as a means of loading a register with several bits of command or time-of-day data, which will continue to affect the peripheral (the clock chip) long after the bit pattern has vanished from the DATA OUT bus.
This definition tells us something about the conditions under which a strobe is generated. First, we are going to output commands, so we shall do so through an output port, using the OUT instruction with an address. Second, we are going to send data to the clock chip (to initialize or correct it if it runs fast or slow) and also read data from the clock chip. An I/O port at a given address can be used either for input or for output (though not both at the same

time); since we are going to output both commands and time-of-day data, but to different parts of the clock chip, we had better use two separate ports-one for commands, the other for data. We could use either port for input from the clock chip; however, the chip has only four data lines, which are used for both input and output, depending on the current command. It therefore makes more sense to use one of our ports solely for outputting 8-bit commands, and the other for input and output of 4-bit time-of-day data. A common convention is to use the even-numbered port of a pair for status input and common output, and the odd-numbered port for data input and output. We shall therefore enable the board for addresses 60 H through 67 H , and use port 60 H for command output and port 61 H for data input and output.

The ENABLE* signal is generated by the five highorder bits of any one of these addresses. The lower three bits, which select one particular address out of the block of eight are applied to the A, B, and C address inputs of two 74LS138 3-to-8 line decoders. The ENABLE* signal is applied to the G2B enabling input line on both chips, and the G1 enabling input of each chip is tied to +5 V . When the third enabling input (G2A) of either chip is pulled low, one of the eight output lines (selected by the three address bits) also goes low. Thus, if we activate the G2A input of one 74LS138 during an output instruction,
and the G2A line of the other chip during an input instruction, we have a means of generating either an output strobe or an input strobe for each of the eight port addresses.

The timing of the strobe is important. It should be active only when the processor has placed valid data on the DATA OUT bus during an ouptut instruction, or when the processor is ready to accept data on the DATA IN bus during an input instruction. Fortunately, the S-100/IEEE696 bus has signals from which we can derive the I/O READ* or I/O WRITE* signal to be applied to the G2A multiplexer inputs, and thereby ensure that the output pulses have proper timing and duration. Execution of the OUT instruction causes the processor to generate a status signal called sOUT; execution of the IN instruction produces a similar signal called sINP. Each is active high and appears when the address is stable on the address bus and before any data is transferred. These signals allow us to distinguish I/O instructions from memory read/write instructions. Likewise, when the processor has placed data from the A register on the DATA OUT bus, and it is stable, the processor generates the active-low pWR* signal. This signal in effect says "I've put data on the bus for you; take it now." When the processor is ready to accept data from a peripheral via the DATA IN bus, it generates the active-high signal pDBIN which says "I'm ready to take

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## Timestamp For CP/M, continued...

your data; put it on the bus now." Most microprocessors strobe the data into the A register of the CPU on the rising edge of Bus State 3 of the System Clock signal ( $\Phi$ ), which occurs toward the end of the pDBIN pulse.

By gating together the sINP and pDBIN signals to produce I/O READ*, which completes the activation of one 74LS138, we ensure that the input strobe line selected by the three low-order address bits goes low only during an input instruction, at a time and for a period that exactly corresponds to the pDBIN pulse. Likewise, by gating together sOUT and pWR (inverted pWR*) to generate I/O WRITE*, which completes the activation of the other 74LS138, we cause the selected output strobe line to go low at a time and for a period corresponding to the pWR* pulse, and thereby load data from the DATA OUT bus into a register located either on the interface or in the peripheral itself.

Simple peripherals that operate at TTL levels, such as the MSM5832 clock chip, require no other signals. We shall use the IS1* strobe directly for opening tri-state gates to connect the clock data lines to the DATA IN bus. We shall invert the OSO* and OS1* strobes and use the rising edge of the pulse to load data from the DATA OUT bus into commmand and data registers.

## The Clock And I/O Registers

The clock chip and I/O registers are shown in Figure 5. The command lines (Hold, Read, Write, and 30 -second ADJust) are connected to the four high-order bits of a 74LS374 command register; the four address lines, which select the internal clock register to be accessed, are connected to the four low-order bits of the register. This register is an MSI chip containing eight edge-trigged, D-
type flip-flops. Data applied from the DATA OUT bus to the eight input terminals D0 through D7 is loaded into the register by the rising edge of a clock pulse; here we use the OSO* output strobe inverted. Thus, data on the bus is clocked into the register by the leading edge of OSO* (which corresponds also to the leading edge of pDBIN) during an output to port 60 H .
The clock data lines D0 through D3 are bidirectional. With HOLD and READ high, DO through D3 carry a BCD (binary-coded decimal) number obtained from the internal register selected by register address lines AO through A3. This number is gated onto DATA IN lines DIO through DI3 by tri-state buffers which are enabled for the duration of the IS1* strobe generated by an input instruction addressing port 61H. DATA IN lines DI4 through DI7 are left unconnected, and the random data on them should be masked out by the software-additional tri-state buffers could be used to ground these lines, but it is hardly worth the effort of putting in the additional wiring.
With HOLD and WRITE high, the selected internal register is set to the value placed on the data lines from DATA OUT lines DO0 through DO4 via half of another 74LS374 register. This register is loaded by the leading edge of pulse OS1* (inverted) during an output to port 61 H . Note that the outputs of this register are tri-stated by the READ command; this is necessary to prevent the contents of the register interfering with the clock data.

## Software

The software consists of a set of subroutines for reading the date and time, which form part of the CP/M CBIOS. A separate transient program is provided for initializing or resetting data and time; this program is resident on the



## Timestamp For CP/M, continued...

diskette as a .COM file and is invoked from the CCP in the usual manner by giving the command:

## A) CLKSET

The clock read routines are invoked by a CALL inserted into the cold boot portion of the CBIOS, or from application programs via an extra JMP instruction added to the end of the standard CP/M jump vector (after the jump to SECTRAN in CP/M 2.2, or after the jump to WRITE in $C P / M$ 1.4). These routines first read the clock registers into a 13-byte numeric array; the BCD digits are then converted to ASCII code and transferred to a string array for printing. The formatting of the string is done by the transfer routine.

## Reading the Clock Register

The CALL instruction at ODABBH in the cold boot transfers control to the main clock subroutine called CLKRD at ODCE4H in Listing 1. The first instruction in CLKRD is another subroutine RDCLK at ODD1DH. To read the thirteen registers, at clock addresses 0 through $C$ (see Figure 6), the HOLD line must first be asserted for at least 150 microseconds. This delay is produced by calling the DELAY subroutine. For a system with a 4 MHz clock, the delay constant NDELY should be increased from 15 H to 30 H or more. Upon return from the DELAY subroutine, register reading begins. For each digit, an OUT instruction to port 60 H loads the command register with READ, HOLD, and a 4-bit block register address. Data from the currently addressed internal register appears on clock data lines D0 through D3 six microseconds later, and is read by an IN instruction to port 61 H .

The addressing sequence of the clock registers is shown at the top of Figure 6. The obvious procedure would be to read the registers in ascending address sequence, but each pair of digits is then the reverse of the normal printing sequence-e.g., the year appears as 18 instead of 81 . The LOOP1 portion of RDCLK therefore reads the registers into the CLKTB array in descending register address order, so that upon completion of the RDCLK subroutine the array will contain the digit pairs in the more convenient printing sequence. The Year/Month/Day sequence is usually reformatted for printing, but is convenient for application programs that sort records into date order. The Day of Week digit at TBUF3 can be directly used as entry into a table of day names. Note that at TBUF4, containing the tens-of-hours digit, bit 3 is set to indicate 24 -hr format. This is later removed by subtracting 8 to obtain the true value.

## Building The Timestamp String

CLKRD sets a pointer (in HL ) to the start of the character array STRING2, and then makes repeated calls to the GET2 subroutine at ODD3EH. GET2 fetches a pair of digits from $\mathrm{M}(\mathrm{BC})$ in the CLKTB array, adds 30 H to convert them to the equivalent ASCII code, and deposits them at $M(H L)$ in the string array starting at STRING2. The pointers are updated after each fetch and deposit. The sequence in which digit pairs are fetched can be changed by setting $B C$ to point to the desired pair before each call to GET2. CLKRD inserts a delimiter between each digit pair ('/' between date pairs, ' $:$ ' between time pairs, and spaces between the end of the date and the start of the time).

## Using The Timestamp String

Listing 1 represents fragments of the CBIOS for a 56 K CP/M 2.2 system using a Tarbell controller. The subroutine CALL to CLKRD is inserted into the cold boot routine at ODABBH. The null terminator at the end of the sign-on message (SMSG at 0DC95H) is removed, and two further portions of message are added: "Logged on" at STRING (ODCB7H), and the STRING2 array, pre-initialized. CLKRD overwrites the string. The null terminator is placed at the end of STRING2. Thus, when the cold boot calls its printing routine PMSG, the timestamp is printed as part of the sign-on message (see Figure 7).

Figure 7: Log-On Message.

```
Tarbell 56K CPM 2.2 of 17-6-80
Logged on 09/23/81 14:36:53
A>
```

Care must be taken to keep the CLKTB array and STRING2 within the body of the CBIOS. If these items are included in the data area at the end of the CBIOS, they may be overwritten by BDOS.

Application programs may call CLKRD via an extra entry in the standard jump vector (placed after the jump to SECTRAN), and then copy either the BCD data or the string into a local data area for processing or printing. However, STRING2 does not end with a ' $\$$ '. It is therefore better to include the clock reading routines and arrays in the application source code and reassemble. This procedure allows greater freedom in formatting and permits printing via a standard BDOS call to Write Buffer function.

## Initializing and Adjusting the Clock

The CLOCKSET program is seldom used once the oscillator frequency has been correctly adjusted by means of the variable capacitor. However, a means of resetting the time is required when there is a change from summer to winter time and vice versa. CLOCKSET is therefore set up as a disk-resident utility executed in the TPA as and when required. As for the read, HOLD is raised for 150 microseconds to prepare the chip. WRITE is then raised, and eleven successive commands are issued, each consisting of HOLD, WRITE, and a register address. Each command is directly followed by a data transfer of the digit to be placed in that address. The command/data sequence takes place in writing loop WRLO: at 162 H in Listing 2. The data are entered via the keyboard into a buffer, from which they are transferred to the clock when the space bar is hit on a time signal. The routine is given in Listing 2, and the prompts are shown in Figure 8.

[^11]

O Listing 2.
FILE: CLKSET .PRN
PAGE 001


0156211 A 02
0159
061 C

017 B
AF
017 C
017 D 60
$017 \mathrm{E} 1 \mathrm{C1E1}$
0181 C 30000


$\begin{array}{lll}\text {; } & & \\ \text { BELAY: } & \text { MVI } & \text { C, NDELY ; Wait } 150 \text { usec. } \\ \text { WAIT } & \text { DCR } & \begin{array}{l}\text { C } \\ \text { WAIT }\end{array} \\ & \text { JNZ } & \text { WAI }\end{array}$
${ }^{;}{ }_{; * * * *}$
018B 436C6F636BMSG1: MESSAGE AREA
01AA

021A
0227

On
Enter Date, day of week, \& time under prompt marks:
YYMMDD HHM , ODH .

## ; *****

$* * * * * * * * * * * * * *$
CLOCK BUFFER
DS 13
ND $\quad 100 \mathrm{H}$

Figure 8: Clock Initialization and subsequent Time Request.

A>CLKSET
Clock-Calendar Initialization
Enter Date, da
YYMMDD
810923
3 2145 $\qquad$ Operator entry terminated by a Return
When ready, press Space to initialize clock
A>


A>TIME
09/23/81 21:45:11


## NORTHSTAR USERS

```
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- number.
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Software Systems


# Speed Up Your Diablo Printer 

by Gary Sabot

## Increase the speed of a Diablo printer by 50\% by using the ETX/ACK protocol.

One of the most widespread applications for microcomputers today is word processing. A word processing program, such as the Electric Pencil or Word Star, allows text to be written, added to, deleted from, and hammered into shape on a video display. The text may then be printed out. Word processing systems often include a daisy wheel printer, such as the Diablo, because of the excellent print quality that these printers offer. However, many of the systems that use the Diablo are not making efficient use of the Diablo's capabilities. This article will show how the speed of a Diablo may be increased by $50 \%$, using a method described in the Diablo manual.

## How the Diablo Operates

The Diablo is capable of receiving 120 CPS (characters per second) from a computer. These characters are stored by the Diablo, which then proceeds to print them at 45 CPS. As a result of the discrepancy between these rates, the Diablo must store any characters which it is not yet ready to print. The storage area is called the print buffer. The Diablo 1610/1620 is capable of storing 158 characters. If too many characters are sent to the Diablo too quickly, a buffer overflow will occur. The last 158 characters sent to the printer (being stored in the print buffer) are erased; and not printed. The computer is not informed of such a buffer overflow. Thus, an overflow can result, as in the loss of the middle of paragraph in a paper, or by wreaking havoc in a computer that is printing out bills or checks.

As you can see, a computer that is operating the Diablo at full speed must take precautions to prevent a print buffer overflow. The computer cannnot constantly transmit to the printer at 120 CPS-it must allow time for the printer to "catch up."

The method used by many computer vendors to prevent buffer overflow is to run the printer at only 30 CPS . This means that the computer can send a maximum of thirty characters per second to the printer. The reason that this

Gary Sabot, 38 Woodlawn Rd., Roslyn, NY 11576.
method is used in many systems utilizing the Diablo is that it is so simple. Because the computer is transmitting characters at a rate slower than the printing rate of the Diablo, there is no way that a buffer overflow can occur. However, this method wastes the Diablo's high speed capability, since it operates the Diablo at two-thirds of its full speed.

One of the best methods of preventing the buffer from overflowing is called ETX/ACK proctol. In this method, a program transmits the information to be printed in fixed length, 158 characters long, "messages." The reason for this specific message length is that the print buffer in the Diablo (the place where messages to be printed are stored) is capable of holding a maximum of 158 characters. Each of these messages must end up with a special character called ETX. ETX is a character, just like any letter or number. ETX stand for "End of Transmission." When the Diablo receives an ETX, it does not print out "ETX"-ETX is not a "printing character." Rather, it transmits a character called ACK back to the computer. ACK stands for "Acknowledge"-the printer is informing the computer that it received the message sent to it and has finished printing it. The computer may now send the next message to be printed.
The computer does not have to send the 158 characters of a message consecutively. For example, it may send thirty characters, then three characters, then eighty characters, and so on. So long as the computer transmits ETX after every 157th character and waits for receipt of ACK, the print buffer in the Diablo cannot overflow. As you can see, this method is independent of the baud rate-it does not matter how fast characters are being sent to the printer. The print buffer never overflows, yet the Diablo can be operated at its maximum rate.

## The Hardware Modifications

To utilize the Diablo at its full speed, two hardware modifications must be made. One is made in the Diablo, the other is made within the computer. First, I will describe the change that must be made in the Diablo.

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## The

 classic computer game$\qquad$

## 

Diablo Printer, continued...
Initially, the Diablo must be "informed" that it will be receiving characters at 1200 CPS. If you own a Diablo 1640/1650, this is quite easy to do. Remove the front panel with the label on it. Immediately below, there are several rows of DIP switches. Turn on the switch adjacent to the caption " 1200 Baud" and turn off any other baud rate switch, such as " 300 Baud."
If you happen to own the older Diablo 1610/1620, this change will be more difficult. The entire top of the Diablo must be taken off and a specific circuit board removed. A jumper must then be installed and the Diablo reassembled. Because the exact location of the jumper will vary depending on how old your Diablo is (older models have the jumper in a different location), I suggest that you refer to your Diablo manual for specifics. Section 5.5.2, "Jumper Installation/Removal," explains how to open the Diablo and gain access to the circuit boards, and section 5.5.2.1, "1200 Baud," indicates the proper location for the jumper. In my Diablo, the jumper location is on the left-front circuit board (see Figure 1). I used a short piece of bare wire as a jumper and taped it into place instead of soldering; consequently, I can easily remove the jumper at a future time. If you prefer, you can order a jumperplug, Diablo part no. 10634, instead of making your own.
The second hardware change is made inside your computer. You must change the baud rate of the serial interface that is connected to the Diablo to 1200 Baud. The procedure used to make this change is different for each computer. In some computers, it is done by changing

Figure 1. Jumper location on Diablo circuit board.


Figure 2. DIP location on North Star Motherboard.

the position of DIP switches within the computer, while the others require jumpers to be soldered. Unless you own a NorthStar Horizon (for which I will detail the required procedure), you will have to refer to your computer's manuals. A local computer store, or your computer's manufacturer, should be able to offer assistance if you run into problems in this area.
In my computer, the NorthStar Horizon, the baud rates of each of the two built-in serial ports are controlled by a "DIP header" that may be found at location 2D. (See Figure 2.) Some of the wires on the DIP header control the baud rate of the left serial interface (the one closest to the left side of the computer, away from the disk drives) and others control the baud rate of the right serial interface (the one closest to the disk drives). (See Figure 3.)


If you are using a video terminal, such as the Hazeltine 1500, then it will probably be connected to the left serial port and the Diablo will be connected to the right serial port. However, if you are using a memory-mapped video board rather than a video terminal, then the Diablo will probably be connected to the left serial port (the right serial port may not even be installed!). Follow the cable that connects the Diablo to your computer to determine which port is connected to the Diablo in your system. Then, remove the DIP header from the location 2D in the computer.

If the Diablo is connected to the left port, remove (desolder) the wire which presently connects pins 3, 4, and 11 . Solder in a new wire connecting pins 3, 4, and 13. Return the DIP to the Horizon.

If the Diablo is connected to the right serial port, remove (desolder) the wire which presently connects pins 5, 6, and 11. Solder in a new wire connecting pins 5, 6 and 13. Return the DIP to the Horizon.

## The Software Modifications

If you use the Electric Pencil for word processing, then your system is now ready. ETX/ATX protocol is automatically used by all of the Diablo versions of the Electric


Pencil. If you wish to use Word Star (another word processing program), you must first run the INSTALL program that comes with Word Star, and when INSTALL shows its "Communications Protocol Menu," select choice "E," for ETX/ACK protocol. Then, a routine that can input characters from the printer must be patched into Word Star-the required procedure is described in the Word Star Manual.

The preceeding paragraph indicated how to modify two word processing programs so that they use ETX/ACK protocol. If word processing is the sole use of your system, then no further changes need be made. If, however, other programs will be using the printer (i.e., MBasic, which may send program listing to the printer), then the Input/Output routines (BIOS) within CP/M itself must be modified so that they use ETX/ACK protocol. This is easier than attempting to separately modify each of the programs that your system may run. Remember that this modified CP/M should be used only with programs that do not already incorporate ETX/ACK protocol (i.e., do not use it with Electric Pencil).


The first step in modifying the BIOS is to obtain an assembly language listing for the BIOS of your particular $C P / M$. Then, where the printer output routine appears (such as the sample in Figure 4), substitute a routine like the one contained in Figure 5, which incorporated ETX/ACK protocol. Remember to substitute the correct port numbers for your system (the sample has been set up for the Horizon's left serial port). Now, assemble the new BIOS and insert into your CP/M. The exact method for "inserting" the BIOS into CP/M may be found in the CP/M manual and the CP/M user's notes for your system. If you are not familiar with $\mathrm{CP} / \mathrm{M}$ or machine language programming, you should be able to receive help in this last modification from the store that originally configured CP/M for your systom.
Although the modifications that I have detailed may seem complicated, they are actually not difficult to implement. The end product, a printer that runs at least $50 \%$ faster, is a joy to work with and a pleasure to behold.

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# Little-Ada* (Part IV) 

by Ralph E. Kenyon, Jr.


#### Abstract

Editor's Note: In this installment, the last in a four-part series, the author presents the Little-Ada compiler and object code. Parts I, II, and III were published in the Sep/Oct 1981, Nov/Dec 1981, and Jan/Feb 1982 issues, in that order. Refer to Part I for introductory reading on Little-Ada, Part II for a discussion of the run-time interpreter and compiler, and Part III for the presentation of Little-Ada's run-time interpreter and source code.


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[^12]

While serving as a lieutenant in the U.S. Navy, RALPH KENYON completed Master's Degrees in both Human Resources Management and Computer Science. With interests ranging from artificial intelligence through Zen, and as a self-styled "extrapolator," he believes that more "generalists" are needed to successfully coordinate and compassionately use man's knowledge.

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10 CO

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Little-Ada, continued.
 11190
11190 1NABO
1DCO 1 LILDO 1IIEO 1 DFO 0083
$1 E 00$
$1 E 10$
$1 E 20$
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$1 E C O$
$1 E L E O$
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0084
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$1 F 50$
$1 F 60$
$1 F 60$
$1 F 70$
$1 F 80$
$1 F 90$
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$1 F B 0$
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# Printer Control With CP/M And MBasic 

by Leo P. Biese and Emillio lannuccillo

While CP/M and the various versions of Microsoft Basic are undoubtedly the most widely used operating system and language available for the microcomputer today, the printer facilities in both can be very frustrating. Consider the following practical problem: You have just made a minor change in your master file copy of CBIOS and want to print only page fourteen. Not a chance! You can do a control-P and TYPE the whole thing. If you try to use 'TYPE' to go through the first thirteen pages on the screen and stop the listing with control-S, you are in for trouble. As soon you hit control- $P$ to switch to the printer, $\mathrm{CP} / \mathrm{M}$ thinks you are negating the previous control-S and promptly dumps the remainder of the program on the screen. A related problem occurs when you are printing a listing and want to stop before the bottom of the page. At 300 baud and up, human dexterity is just not fast enough to hit that control-S at the end of a line.

You usually end up leaving off the last few letters or printing out the first few letters of the following line, both of which end in curses, wasted paper and starting over. A friend of ours thought he had this problem licked by adding forty wait states after a carriage return. This gave a nice usable pause, but he was somewhat chagrined to learn that the lines were indeed printed out at the specified 300 baud, while the overall throughput was about 10 baud!

With Microsoft Basic the problem is even worse. Back in the "good old days" (1978) Microsoft had a CONSOLE statement that for some inexplicable reason was left out of later versions. Even this was only a partial solution at best. Several recently published schemes for implementing printer control involve POKEing the CP/M IOBYTE and retrieving the CONSOLE statement. This is a valuable help when you have a program that you may wish to direct to the printer one time and the screen the next. This solution is of no help when you have to debug a long program that you will eventually want to go to the printer. This was forcibly illustrated during the recent development of an accounting system requiring many lengthy reports. Each change in the program required printing out four or more identical pages while the next page was being "cleaned." One alternative was to write the whole thing in

[^13]PRINT statements and then go back and change them to LPRINTS. Another solution was to go back to school, learn structured programming, buy a compiler and do it right the first time. Neither seemed very attractive.

All these problems were quite easily solved with two minor changes to the BIOS. Simply alter the BIOS to recognize front panel switch \#8 (arbitrary) to toggle the printer only at the end of the current line being printed. These changes simply involve sandwiching six lines into CP/M's character output routine, forcing it to first look at the front panel, and if switch \#8 is on, to send output to the assigned Console and Lister devices simultaneously. Once this is accomplished the lister routine must look at panel switch \#9 and, if on, halt temporarily at the first carriage return encountered.


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Figure 1: Circuit to replace front-panel switches \#8-15 on the S-100 Bus.


Listing 2: Additions to the $C P / M$ BIOS to force ${ }^{7}$ the Lister device to look at front panel switch \#9 and halt at the first carriage return if TRUE.


The additions are given in Listings 1 and 2, and are indicated by a [**] in the remarks column. The unmarked code is as received in the Tarbell version of CP/M CBIOS Version 1.4 with all labels preserved.

## No Front Panel?

The software alteration has been eminently satisfactory for the past two years. Recently, however, we acquired an S-100 machine without a front panel and trashed our "Impossible Dream" [the Imsai front panel] after years of arbitrary problems. After most of the difficulties were solved, or at least accepted, it developed the curious habit of halting the CPU for no apparent reason. Plus, it almost always stopped just before the operator could save a long program. The front panel was replaced with a clean, brushed aluminum one and a Z-80 CPU was installed along with a monitor with a monitor program in ROM that did everything the panel did-better and faster. After living without printer control for a few months, the situation became unbearable and the hardware modification shown in Figure 1 was constructed.

This substitute for front panel switches is a simple, oneevening project (with readily available parts), and can be constructed on a blank S-100 prototype board or a small perf-board attached directly to the front panel, which is probably why we never got around to it! A much better solution is to kludge it onto an existing board and steal the power and bus signals, thus obviating the installation of yet another board, five-volt regulators, etc. We attached a 10-pin strip connector to the top of the board and, as can be seen from the diagram, switches \#8 to \#15 can be implemented provided you have enough sections to spare in an available hex-driver. Since only three chips are needed, it will easily fit on an Imsai or MITS CPU or I/O board and many others. Our "easy" solution developed when we acquired several QT Computer Systems Clock/ Calendar boards which have enough room left to add the whole computer. If you wish to go this route, check your existing CPU, CLOCK, I/O, D/A converter, or other boards, as there are often unused chip sections available and the hex-driver (U14) may not even be needed.

LEO P. BIESE, M.D. is a pathologist and medical director of New England Clinical Laboratories, Inc., a reference laboratory located in New Hampshire. He also serves as software editor and vice-chairman of the College of American Pathologists Microcomputer Committee and its Software Exchange. His principal interests are in the application of microcomputers to the clinical laboratory, computer-assisted interpretive reporting and teaching programming to laboratory scientists.

EMILIO D. IANNUCCILLO is an attorney with a private practice in Rhode Island. He is Town Solicitor for Bristol, and specializes in municipal-law, commercial-law and realty-law. His interests are in systems software for the legal profession and municipal government, data retrieval, and legal application programming.

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# Interfacing To S-100/IEEE 696 Microcomputers 

by Chrıs Terry


#### Abstract

Interfacing To S-100/IEEE 696 Microcomputers, by S. Libes and M. Garetz. Osborne/McGraw-Hill, 321 pp, \$15.00 1981.


This book is a "must" for anyone who wishes to construct a custom interface between an S-100 microcomputer and almost any type of peripheral device. It is a goldmine of useful information new and old, much of which has never before been collected in one place. The writing is a model of what such manuals should be but seldom are; the authors say exactly what they mean-simply, understandably, and with no ambiguity. An enormous amount of hard work must have gone into not only mastering the subject matter, but also into communicating it so admirably; yet they make it look easy and read so well. In the sense that "art is the concealment of art," the authors are artists as well as technologists.

The material falls into two main classes:

- Description of the S-100 Bus.
- Applications-How to use the bus features.

Each chapter has a short but useful bibliography of further information sources, and there is an excellent index.

## Description Of The S-100 Bus

The proposed IEEE-696 Standard, reprinted from the July, 1979 issue of Computer, is included as an appendix and provides the technical definition of the current S-100 Bus. The average reader, however, will be far more enlightened by the discussions of the bus contained in Chapters 2 through 4.

Chapter 2 contains a brief history of the S-100 bus, the mechanical description of the circuit boards and motherboard, a description of the signal groups of the bus, and power supply considerations. This chapter also introduces the important concepts of a Bus Master, which has absolute control of the bus, and a Slave, which uses the bus only at the behest of the Master. The Master is normally the CPU board, but it may release control of the bus to Temporary Masters.

Chapters 3 and 4 provide the essentials for understanding the S-100 bus. Chapter 3 gives detailed description of each of the signals, grouped by function. Particular attention is paid to the differences between the original MITS

[^14]version of the bus and the new IEEE-696 definition. Chapter 4 describes the timing relationships of the bus. In particular, it contains a beautifully clear description of the bus cycle, consisting of several bus states, and the purpose of each state. There is a detailed analysis of what occurs on the bus during each state of a read cycle and a write cycle, and a discussion of how a bus cycle can be extended by wait states.

> This book is a "must" for anyone who wishes to construct a custom interface between an S-100 microcomputer and almost any type of peripheral device.

The book would be well worth its price for these chapters alone. After reading them, I felt that for the first time I understood not only what takes place on the bus, but why. It is impossible for the average user to get this kind of understanding from manufacturers' documentation and timing diagrams.

## Applications

Chapters 5 through 16 contain a compendium of circuits, device driver routines and useful information for interfacing a wide variety of devices. If you want to connect a special device to your system, look through the table of contents of this book before you start reinventing the wheel. There is almost certain to be a circuit that you can use or adapt.

Chapter 5 deals with decoding, buffering, and wait state generation. Chapter 6 is a comprehensive interfacing guide for static RAM and EPROM-useful if you want to add, say, 1 K of workspace for a PROM monitor. Dynamic RAM is not discussed; the authors point out that timing problems are horrendous and are affected by board layout, so that a wire-wrapped dynamic RAM board would be unreliable-if it worked at all.

Chapter 7 discusses the general principles of I/O ports, handshaking, and I/O channels (a combination of ports to handle status, commands and data for one peripheral). Programmable I/O port IC's, which combine all functions for one or more channels into a single chip, are briefly

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## Book Review, continued...

discussed with specific reference to the Intel 8255 PPI (Programmed Peripheral Interface) and the Motorola 6820 PIA (Peripheral Interface Adaptor). Chapter 8 gives specific examples of simple parallel interfaces with and without handshaking, and typical software drivers for them. In both chapters there are brief discussions of memorymapped I/O, in which an I/O port occupies a location in the memory space. This type of I/O is used exclusively by 6502 and 680X microprocessors which must use memory reference instructions to perform I/O; it is an alternative mode in the Z80/808X microprocessors, though here one must consider the trade-off between the improved I/O speed and the loss of addressable memory space entailed by memory-mapped I/O.

Chapters 9 and 10 are called "Interfacing to the Real World," and cover input from keyboards and various kinds of sensors, and control of lamps, motors, sound generators, and other non-digital devices.

Chapter 11 is a brief, though excellent discussion of serial interfaces, with specific reference to some commonly used serializer/deserializer chips: the AY-5-1013 and 8250 UARTs, and the 8251A and 2651 USARTs. Since microcomputer software generally assumes asynchronous transmission over communication networks, there is no discussion of the synchronous transmission features of the USARTs; however, the bibliography cites sources for such information.

Chapter 12 covers the basics of interfacing to digital/ analog and analog/digitel converters. Chapter 13 is a full and very helpful discussion of interrupts and how to use them. Chapter 14 deals with programmable timer/counters (specifically the 8253) and their applications.

Chapter 15, on TMA (Temporary Master Access), deserves special mention. Its topic is the release of the bus by the primary Bus Master (usually the CPU) to some other device which becomes a Temporary Bus Master. This is a technique which in minicomputers used to be called DMA (Direct Memory Access), though that term is not appropriate on the $\mathrm{S}-100$ bus. The object is to allow the Temporary Bus Master to take control of the bus for a limited time or specific task. Applications include highspeed data transfers between memory and a peripheral (such as a disk controller), or transfer of control to a different CPU (as on the Godbout 8085/8088 dual processor). The timing considerations and special requirements of TMA circuits are clearly explained, and logic diagrams illustrate several implementations for various purposes.

The last two chapters describe miscellaneous but useful interface circuits (such as a jump-on-reset circuit), and justify the deliberate omission of several types of interface. The grounds for omission were mainly complexity of the device side of the interface (e.g., video and disk controllers), software complexity (e.g., non S-100 computers), or irrelevance to the S-100 context (e.g., cassettes).

[^15]

Over 150,000 computer owners and novices attended the 1981 National Computer Shows and Office Equipment Expositions, and more than a quarter of a million are expected to be at the 1982 shows.
Each show features hundreds of companies using thousands of square feet of display space to showcase and sell millions of dollars worth of micro and mini computers, data and word processing equipment, peripherals, accessories, supplies and software.

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Washington, DC DC Armory/Starplex
Across from RFK Stadium Thursday-Sunday October 28-31, 1982 11 AM to 6 PM Daily DIRECTIONS: 2001 E. CAPITOL ST. SE
(E. CAPITOL ST. EXIT OFF I-295 - KENILWORTH FRWY)

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 510

Minneapolis Minn. Auditorium \& Convention Hall Third Avenue Thursday-Sunday September 16-19, 1982 11 AM to 6 PM Daily DIRECTIONS: HWY 94 to 11th St. Exit to Third Ave.

[^16]Program Name: Jools
Hardware System: CP/M 8" SD or NorthStar DD
Minimum Memory Size: 48K
Language: Machine Code
Description: UNIX-style software tools specially adapted for the CP/M environment. The sixteen tools include VSORT-highspeed internal/external sorting on either fixed- or variable-length fields; SELECT-line extraction from a file based on the values of fixed- or variable-length fields; FIND and REPLACE--search for and replace text within files based on regular expression patterns; and REARRANG - reorder fields of a line to a user-specified format. Jools provides a modular problem-solving facility for the CP/M programmer without requiring special programming. The manual details how Jools can maintain mailing lists and biliographic databases, generate permuted indexes, and monitor changes made to a file.
Release: December 1981
Price: $\$ 95.00$ (manual only, $\$ 20.00$ )
Included with price: One 8" IBM SD or two 5-1/4" NorthStar DD diskettes, 66-page manual and quick reference guide.
Where to purchase it:
Pluto Research Group
P.O. Box 50444

Palo Alto, CA 94303-0444
(415)323-5654

Program Name: Solomon Series II
Hardware System: Z-80 with CP/M
Minimum Memory Size: 64 RAM, 1 Mb of disk storage minimium.
Description: General Accounting with Job Management. A fully integrated system utilizing a single database manager. Includes General Ledger, Accounts Receivable, Accounts Payable, Payroll, Invoicing, Cash

Receipts/Disbursements, Fixed Assets (depreciation), Address maintenance (mailing list), and Job Costing
Release: December 1981
Price: $\$ 3,495$
Included with price: Compiled PL/I code in executable form, and user reference manual. Where to purchase it:
TLB ASSOCIATES, INC
P.O. Box 414

Findlay, Ohio 45840
(419)424-0422

## Program Name: REFORMATTER CP/M-

 IBM File Conversion ProgramHardware System: Multi-drive CP/M-based system
Minimum Memory Size: 24 K
Language: Assembly Language (8080)
Description: REFORMATTER is an intelligent bi-directional file conversion program. Reads and writes IBM 3740 formatted disks (IBM Diskette 1, Basic Data Exchange Format) and gives CP/M users the ability to exchange data on floppy disk with IBM equipment, or any equipment accepting an IBM 3740 disk. Handles all conversion functions such as file reorganization and ASCII to EBCDIC character translation. Gives CP/M user access to all IBM diskette file attributes and provides facilities for examining and altering all data areas, directory entries, and fields within each IBM data set label.

## Release: June 1978

Price: \$195.00
Included with price: $8^{\prime \prime}$ disk, manual, and telephone consultation if required.

## Where to purchase it:

MicroTech Exports, Inc.
467 Hamilton Avenue
Palo Alto, CA 94301
(415)324-9114

Program Name: PASS System
Hardware System: NorthStar system, 2-DD

## or QD drives

Minimum Memory Size: 32K
Description: Assembly language program development system. Includes: PASS assembler with interactive input editing, built in cross reference listing and macro capability, improved mnemonics and syntax, e.g., "STM $\mathrm{A}, \mathrm{HL}$ " instead of "LD(HL),A"; STEP, debugging trace, with capability to set displays to field changes and echo to printer. And BLDMACRO to assist in adding macros to provided macro library.
Release: November 1981
Price: $\$ 40.00$
Included with price: Object code and manual (and program to print manual) on 5-1/4" DD or QD, ten hard sector disks. Source code \$160 extra, \$200 total, requires signed agreement.
Where to purchase it:
PASS
P.O. Box 1382

Lafayette, CA 94549
(415)945-7911

## Program Name: Solomon 1

Hardware System: Z-80 with CP/M
Minimum Memory Size: 64K RAM, 1 Mbyte of disk storage min.
Language: PL/I
Description: The Solomon I is an accounting package designed around the MDBS database management system. It includes several accountinng modules which access the same database. The result is increased ease of use-there are no sorts to run, batches of transactions to post and all functions are available from a single master menu. Solomon I includes General Ledger, Payroll, Accounts Payable, Invoicing, Accounts Receivable,

## Software Directory, continued...

Fixed Assets, and Address Maintenance.
Release: October 1981
Price: \$2,595
Included with price: Compiled PL/I code and user reference manual.
Where to purchase it:
TLB Associates, Inc.
1120 Commmerce Parkway
P.O. Box 414

Findlay, OH 45840
(419)424-0422

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Program Name: Spellbinder Hardware System: CP/M-compatible systems
Minimum Memory Size: 32K
Language: Machine Language
Description: Offers both the novice and experienced user complete word processing and office management capabilities. Includes a hierarchy of Macro commands for such tasks as que and zip sorting, mail merge, forms generation, and line numbering. Operates in two modes: edit mode and command mode. Extremely simple to learn.
Release: July 1981
Price: $\$ 450$
Included with price: Disk and special Spellbinder keytops
Where to purchase it:
Data Technology Industries
700 Whitney Street
San Leandro, CA 94577
(415)638-1206

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Price is $\$ 1125.00$; available from Advanced Micro Digital Corp., 7201 Garden Grove Blvd., Suite \#E Garden Grove, CA 92641 (714)891-4004.

## Winchester Disk System For S-100

Tarbell Electronics has introduced a new series of S-100 Winchester subsystems allowing expansion from 10 to over 200 Mb . Their ATTACH program provides a way to get up-and-running quickly. Users can start with a small system, then add up to three additional drives of any capacity. All Tarbell hard-disk subsystems 33Mbytes and above use a voice-coil actuator which provides an
average access time of 50 milliseconds. Data comes off the disk into the deblocking

buffer at the maximum possible speed of $1 \mathrm{Mb} / \mathrm{Sec}$, meaning that a 24 K file can be loaded into memory in about one second! Additional features of the subsystems include on-board CRC performed data, automatic alternate sector assignment, 512-byte onboard deblock buffer and the use of only one S-100 board slot. The subsystem includes S-100 interface, drive cabinet, power supply, cables, software and all documentation. Tarbell Electronics, 950 Dovlen Place, Suite B, Carson, CA 90746; (213)538-4251.

## 64K S-100 Static RAM Board

SSM Microcomputer Products Inc., has announced a new high performance, low power 64 K static RAM memory board, the MB64. It operates at up to 6 MHz offering two 32 K blocks, and up to 8 K of EPROM. It also includes extended addressing of up to 16 Mb of memory. Power consumption is typically less than 600 MA.
Price is less than $\$ 850$; contact SSM Microcomputer Products Inc., 2190 Paragon Dr., San Jose, CA 95131; (408)946-7400.

## S-100 Mainframe

Para Dynamics Corp., has announces the PRONTO mainframe/disk in a free-standing $26^{\prime \prime} \mathrm{H} \times 20^{\prime \prime} \mathrm{D} \times 18^{\prime \prime} \mathrm{W}$ with casters. It will hold up to two $8^{\prime \prime}$ floppy disk drives plus one $8^{\prime \prime}$ rigid disk drive, or one $8^{\prime \prime}$ floppy
disk, one $8 "$ rigid disk and streamer tape backup. The power supply allows changing input and output voltages. The IEEE Standard S -100 motherboard uses high quality goldplated edge card connections and accomodates up to 18 cards, including the new 10 " $\times 10$ " cards.


The motherboard compartment is cooled with a forced air filtered system that funnels air evenly and effectively over and through the PC cards. Other features include motherboard jumpers so that the 220 ohm load termination on various signal lines may be grounded, left open or made high with the installation of a 7805 voltage regulator in the position provided on the motherboard. The unit also includes a double pole circuit breaker, a dual AC convenience outlet on the rear of the cabinet, a double-bitted on/off key switch and a power "on" indicator and "reset."
Para Dynamics, 7740 E. Redfield Rd. Scottsdale, AZ 85260, (602)991-1600.


If you are a CP/M user, on any system -S100, Apple, TRS-80, Heath, Ohio Scientific, Onyx, Durango, Intel MDS, Mostek MDX, etc-after all CP/M is the Disk Operating System that has been implemented on more computer systems than any other DOS-then Microsystems magazine is the "only" magazine published specifically for you!

Or, if you use an S-100/IEEE-696 based computer-and the most sophisticated microcomputer systems available use the S-100/IEEE-696 hardware bus-then Microsystems magazine is the "only" magazine published specifically for you!
We started publishing Microsystems almost two years ago to fill the void in the microcomputer field. There were magazines catering exclusively to the TRS-80, Apple, Pet, Heath, etc. system users. There were also broad based publications that cover the entire field but no one system in depth. But no magazine existed for CP/M users-nor did one exist for S-100 users.

## The why and what of a software bus

First of all what is a "bus?" And why do we cali CP/M "the software bus?"

A "bus" is a technique used to interface many different modules. Examples are the "S-100/IEEE-696 Bus" and the "IEEE-488 Bus." These are hardware buses that permit a user to plug a bus-compatible device into the bus without having to make any other hardware modifications and expect the device to operate with little or no modification.

CP/M is a Disk Operating System (DOS). It was first introduced in 1974 and is now the oldest and most mature DOS for microcomputer systems. CP/M has now been implemented on over 250 different computer systems. It has been implemented on hard disk systems as well as floppy disk systems. It is supported by two user groups (CP/MUG and SIG/M-UG) that have released over 80 volumes containing over 2,000 public domain programs that can be loaded and run on systems using the CP/M DOS. Add to this another 1,500 commercially available

CP/M software packages and you have the largest applications software base in existence.

CP/M is the only DOS for micros that has stood the test of time (seven years) with the highest level of compatibility from version to version. And over the years this compatibility has been maintained as new features have been added.

This is why we say "CP/M is the software bus" and why Microsystems magazine is vital to providing CP/M users with technical information on using $\mathrm{CP} / \mathrm{M}$, interfacing to CP/M, new CP/M compatible products and for $\mathrm{CP} / \mathrm{M}$ users to exchange ideas.

## Why support the $\mathrm{S}-100$ bus?

S-100 is currently the most widely used microcomputer hardware bus. It offers advantages not available with any other microcomputer system. Here are a few of the advantages:
$S-100$ is processor independent. There are already thirty different S-100 CPU cards that can be plugged into an S-100 bus computer. Nine 8 -bit microprocessors are available: 6502, 6800, 6802, 6809, 2650, F8, 8080, 8085 and Z80. Eight 16 -bit microprocessors are available: $8086,8088,9900$, Z8000, 68000, Pascal Microengine, Alpha Micro (similar to LSI-11) and even the AMD2901 bit slice processor. Take your pick from the incredible offerings.

S-100 has the greatest microcomputer power. What other microcomputer system has direct addressing of up to 16 megabytes of memory, up to $65,536 \mathrm{I} / \mathrm{O}$ ports, up to 10 vectored interrupts, up to 16 masters on the bus (with priority) and up to 10 Mhz data transfer rate? You will have to go a long way to use up that computing power.

S-100 is standardized. The S-100 bus has been standardized by the IEEE (Institute of Electrical and Electronic Engineers) assuring the highest degree of compatibility among plug-in boards from different manufacturers. And, Microsystems has published the complete IEEE S-100/696 standard (all 26 pages).

S-100 has the greatest hardware support. There are now over sixty different manufacturers of about 400 different plug-in S-100 boards. Far greater than any other microcomputer system.

With all these advantages is it any wonder that S-100 systems are so popular with microcomputer users who want to do more than just play games?

## For the serious computer user.

Each issue of Microsystems brings you the latest in the CP/M and S-100 world. Articles on applications, tutorials, software development, product reviews, and lots more, to keep you on top of the ever changing microcomputer scene.
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## Bring the flavor of Unix To your $\mathbf{Z 8 0}$-based CP/M system with Unica

"Unicum: a thing unique in its kind, especially an example of writing. Unica: the plural of unicum."

The Unica: a unique collection of programs supporting many features of the Unix operating system never before available under $\mathrm{CP} / \mathrm{M}$. The Unica are more than software tools; they are finely crafted instruments of surgical quality. Some of the Unica are:

```
bc - binary file compare
cat - catenate files
cp - copy one or more files
dm - disk map and statistics
hc - horizontal file catenation
In - create file links (aliases)
ls - directory lister
mv - move (rename) files, even across users
mv - move (renam
rm - remove files 
sc - source file compare, w
sr - search multiple files for a pattern
sp - spelling error detector, with 20,000 word dictionary
```

Each Unicum understands several flags ("options" or"switches") which control program alternatives. No special"shell" is needed; Unica commands are typed to the standard CP/M command interpreter. The Unica package supports several Unix-like facilities, like preter. The Unica pack
filename user numbers:
sc data.bas; 2 data.bas; 3
(compares files belonging to user 2 and user 3 ); Wildcard patterns:
rm *tmp* -v
(types each filename containing the letters TMP and asks whether to delete the file);
I/O redirection:
ls $-\mathrm{a}>$ list
(writes a directory listing of all files to file"list");
Pipes:
cat chap* ! sp ! srt $>$ lst:
(concatenates each file whose name starts with"chap", makes a list of mispelled words, sorts the list, and prints it on the listing device).

The Unica are written in XM-80, a low level language which combines rigorously checked procedure definition and invocation with the versatility of Z 80 assembly language. XM-80 includes a language translator which turns XM-80 programs into source code for MACRO-80, the industry standard assembler from Microsoft. It also includes a MACRO-80 object library with over forty "software components", subroutine packages which are called to perform services such as piping, wildcard matching, output formatting, and deviceindependent $I / O$ with buffers of any size from 1 to 64 k bytes.

The source code for each Unicum main program (but not for the software component library) is provided. With the Unica and XM-80, you can customize each utility to your installation, and write your own applications quickly and efficiently. Programs which you write using XM-80 components are not subject to any licensing fee.

Extensive documentation includes tutorials, reference manuals, individual spec sheets for each component, and thorough descriptions of each Unicum.

Update policy: each Unica owner is informed when new Unica or components become available. At any time, and as often as you like, you can return the distribution disk with a $\$ 10$ handling fee and get the current versions of the Unica and XM-80, with documentation for all new or changed software.

The Unica and XM-80 (which requires MACRO-80) are priced at $\$ 195$, or $\$ 25$ for the documentation. The Unica alone are supplied as -COM executable files and are priced at $\$ 95$ for the set, or $\$ 15$ for the documentation. Software is distributed on 8" floppy disks for $\mathbf{Z 8 0}$ $C P / M$ version 2 systems.

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[^1]:    See our catalog for many other fine S-100 and Apple Boards including: - Analog to Digital Converters (16-256 channe/s; 12, 14, or 16 bit accuracy; $30,40,100$, or 125 KHz ; programmable gain; timer/counters) - Digital to Analog Converters (12 bit accuracy, 3 microsecond conversion) - 8086 CPU Board - I/O Boards - 16K Static RAM - Real-time Video Digitizer and Display.

    CP/M MP/M CP/M-86 and MP/M-86 are trademarks of Digital Research Inc. BASIC-86, MS FORTRAN and MS-PASCAL are trademarks of MicroSoft Inc.

[^2]:    RALPH J. JANNELLI holds a B.S.E.E. from New Jersey Institute of Technology. He has spent nine years designing hardware and software for calculators and office products systems with Monroe Systems for Business. He is currently working for Gilbarco Inc. as a Sr. Systems Engineer in the field of Retall Data Systems.

[^3]:    Bob Weidemann, 5 Bondsburry Lane, Melville, NY 11747.

[^4]:    Ira Gordon, 6 Lenox Rd., Farmingdale, NY 11735.
    Karl Wacker, 100 Rockaway St., Islip Terrace, NY 11752
    Software copyright ${ }^{\circ} 1981$ by K-Wacker, Inc., Islip Terrace, NY.

[^5]:    Dennis Thovson, 243 McMane Ave., Berkeley Hts., NJ 07922.

[^6]:    232C handshake signals for the serial ports. (There are instructions in the manual for adding a handshake signal to one of the serial ports with some simple external circuitry.) By contrast, the input and output parallel ports can be configured to accommodate full handshake with the connected peripheral device. In addition, these ports provide or accept strobe pulses associated with the transmitted or received data respectively.

    The clock circuit provides the timed interrupt required by MP/M for task scheduling and time-of-day functions.

[^7]:    Biese/lannuccillo, RFD1 Murray Hill Rd., Hill, NH 03243.

[^8]:    The very low power dissipation of this chip ( 90 micro Watts @ 3V) allows safe battery backup for several months with as little as 2.2 volts, in this case supplied by a 3.6 volt G.E. "Data Sentry" miniature Ni-Cad battery with on-chip automatic power-loss switching. The oscillator is driven by an external 32.768 Hz crystal (about the size of a $1 / 8$ watt resister!!; and a trimming capacitor is provided to "pull" the oscillator frequency. The frequency stability for the 5832 crystal oscillator is given as $+/-2$ ppm for an approximate two-fold change in operating temperature or a voltage drop to as low as two volts from the nominal five volts. This is an order of magnitude of only about one second per week, so obviously there are factors that effect the clock stability other than oscillator frequency. Since the chip runs at five volts (from the standard 7805 regulator) and is warmer when on-line; and then drops to 3.6 volts and a cooler environment when on standby, the accuracy of the clock is significantly affected. This is not a real problem with our use, dating print-outs, but it would

[^9]:    Ray Duncan, 4147 Beethoven St., Los Angeles, CA 90066.

[^10]:    Lightning One trademark of Lomas Data Products, Inc. *CP/M-86 and MP/M-86 trademark of Digital Research. ${ }^{* *}$ MS-DOS trademark of Microsoft Inc.

[^11]:    CHRIS TERRY was educated in England as a linguist, with an M.A. from the University of Cambridge and technical training in the Royal Corps of Signals during WWII. He came to the USA in 1958, and has worked as a technical writer for various publishing houses and digital equipment manufacturers. Chris has been with the Systems Development division of Dun \& Bradstreet, Inc. since 1974.

[^12]:    Ralph E. Kenyon, Jr., 1686 West Main Rd., Portsmouth, RI 02871
    *Ada is a trademark of the U.S. Department of Defense (Ada Joint Program Office).
    The DOD does not recognize dialects of the Ada language, whether by supersetting or subsetting.

[^13]:    Leo P. Biese and Emillio lannuccillo, RFD \#1 Murray Hill Road, Hill, NH, 03243.

[^14]:    Chris Terry, 324 E. 35th St., New York, NY 10016.

[^15]:    CHRIS TERRY became involved with micros when he built an Altair 8800 in 1975; he still uses this, mainly for word processing. He is fascinated with the potential of the micro as a tool for living (and as the greatest toy in the world!). Other interests include the Arthurian legends, science fiction, and both classical and electronic music.

[^16]:    The National Computer Shows are produced by Northeast Expositions Inc. who also produce Electronica - shows featuring home entertainment equipment and personal electronics - which are held annually in major US cities. NEI also produces the Applefest Shows. For more information about any of these events call us at $617-739-2000$ or write to the above address.

[^17]:    CompuPro is a division of Godbout Electronics, Oakland Airport, CA 94614 -0355 $\quad 415-562$-0636

