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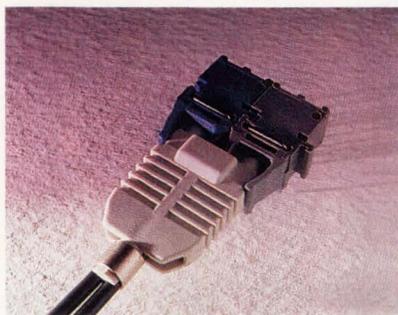
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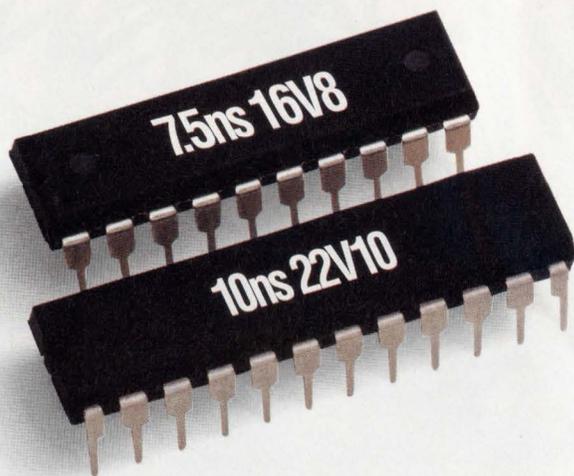
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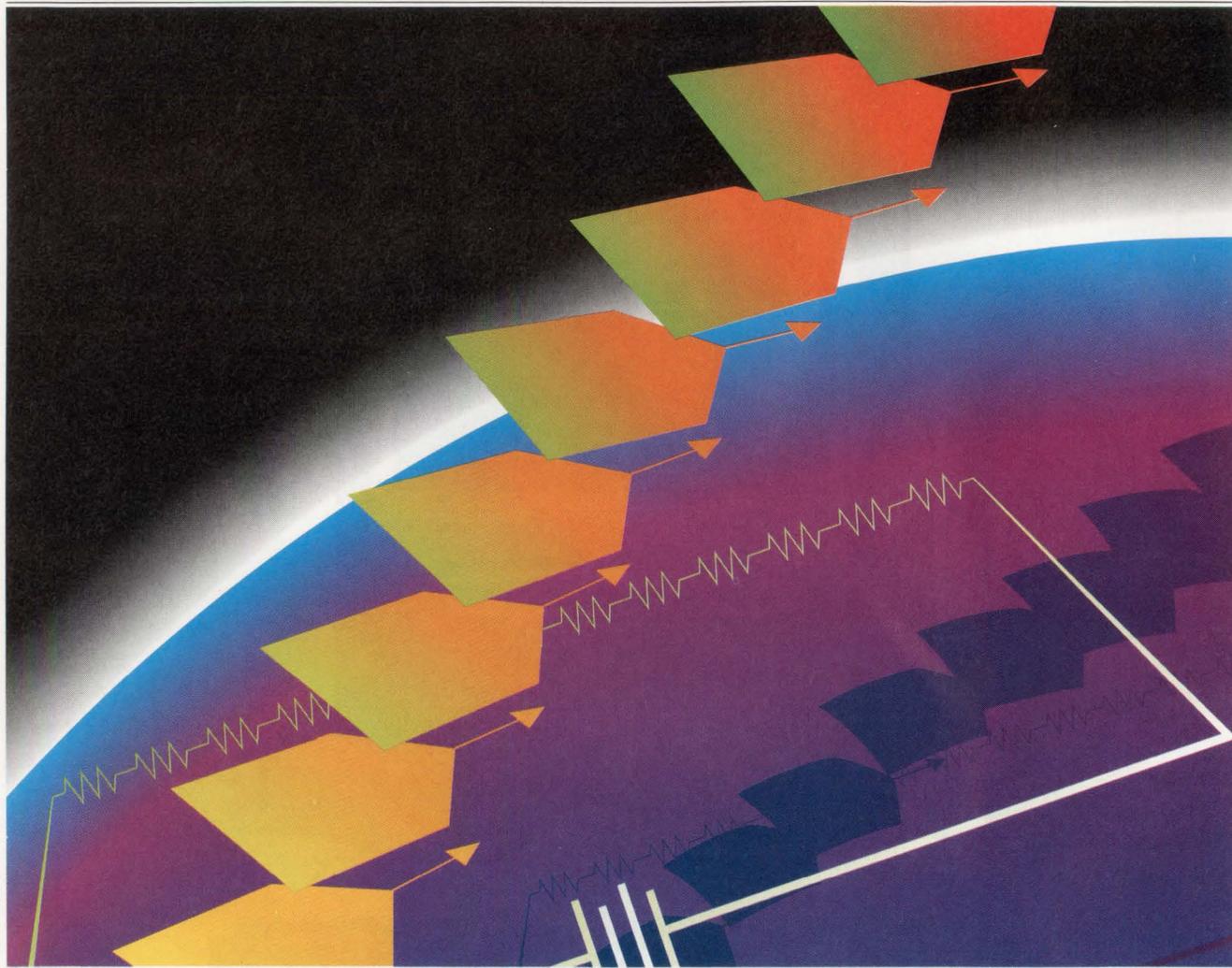
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ELECTRONIC DESIGN



**TECHNOLOGY
ANALYSIS**

41 CICC '92 BRINGS OUT THE BEST IN NEW IC DESIGNS

The technical program sheds light on advances in digital, analog, and communications ICs, as well as EDA software and mixed-signal testing.

**COVER
FEATURE**

85 IC'S 8, 14-BIT DACS SHARE RESISTOR LADDER FOR MSBS

Eight 14-bit voltage-output DACs squeeze into a single 28-pin SOIC, saving 20 to 30 active devices per octal DAC package.

**PRODUCT
INNOVATIONS**

101 FUNCTION BLOCKS SPEED UP CHIP DEVELOPMENT

Designers can select parts from a library of blocks to assemble high-performance ICs for many volume applications.

110 PC-BOARD TOOLS SIDESTEP HIGH-SPEED DESIGN SNAGS

Intelligent software helps engineers build high-speed boards and MCMs that are correct the first time through.

114 SILICON INTERCONNECTS RENDER BREADBOARDS PASSÉ

A 1024-pin land-grid array lifts prototyping into the realm of totally programmable hardware systems.

14 EDITORIAL

18 TECHNOLOGY BRIEFING

Europe creates new patent

23 TECHNOLOGY NEWSLETTER

- Thin-film foundry offers superconductors
- See the latest in EDA technology for free
- 8-bit microcontrollers hold 2.25-kbyte RAM
- Smart disk-drive spindle motor coming
- VHDL meeting stresses real-world design use
- HBT silicon transistor operates up to 53 GHz
- Enhanced architecture ups FPGAs to 20k gates
- Model approach improves lossy-line simulation

30 TECHNOLOGY ADVANCES

- Multilevel pipeline and 1-kbyte cache let 16-bit-bus 486 deliver high throughput
- Interactive trackball relies on force-feedback sensing
- Test-synthesis approach for ICs incorporates partial-scan technology
- Josephson-junction flip-flop toggles at a record 144 GHz



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 1972 Certificate of Merit
 1975 Two Certificates of Merit
 1976 Certificate of Merit
 1978 Certificate of Merit
 1980 Certificate of Merit
 1986 First Place Award
 1989 Certificate of Merit
 1992 Certificate of Merit

91 IDEAS FOR DESIGN

- 3-A dc-dc converter needs no heat sink
- Tester finds shorts on loaded boards
- Bootstrap circuit cuts distortion

96 QUICK LOOK

- PC add-on card gives software some sound
- European cellular phone market should stay strong
- Doing me-too-with-a-twist products
- What lower interest rates mean for engineering investors

97 PEASE PORRIDGE

What's all this vice-versa stuff, anyhow?

NEW PRODUCTS

- 116 Digital ICs**
ASIC families pack up to 600,000 gates thanks to 0.6- μ m features
- 117 Digital ICs**
486 workalike retains 386SX bus, pinout for notebook PCs
- 118 Computers & Peripherals**
- 119 Software**
- 120 Instruments**
- 122 Components**
- 123 Computer Boards**

125 INDEX OF ADVERTISERS

129 READER SERVICE CARD

COMING NEXT ISSUE

- Special Report: The floodgates open for multimedia products
- First details on a new multimedia graphics chip
- New mixed-signal software integrates design and test
- 32-bit microcontroller eases programming with on-chip flash EPROM
- A preview of the upcoming Electro show
- PLUS:
Ideas for Design
Pease Porridge
Technology Advances
Quick Look

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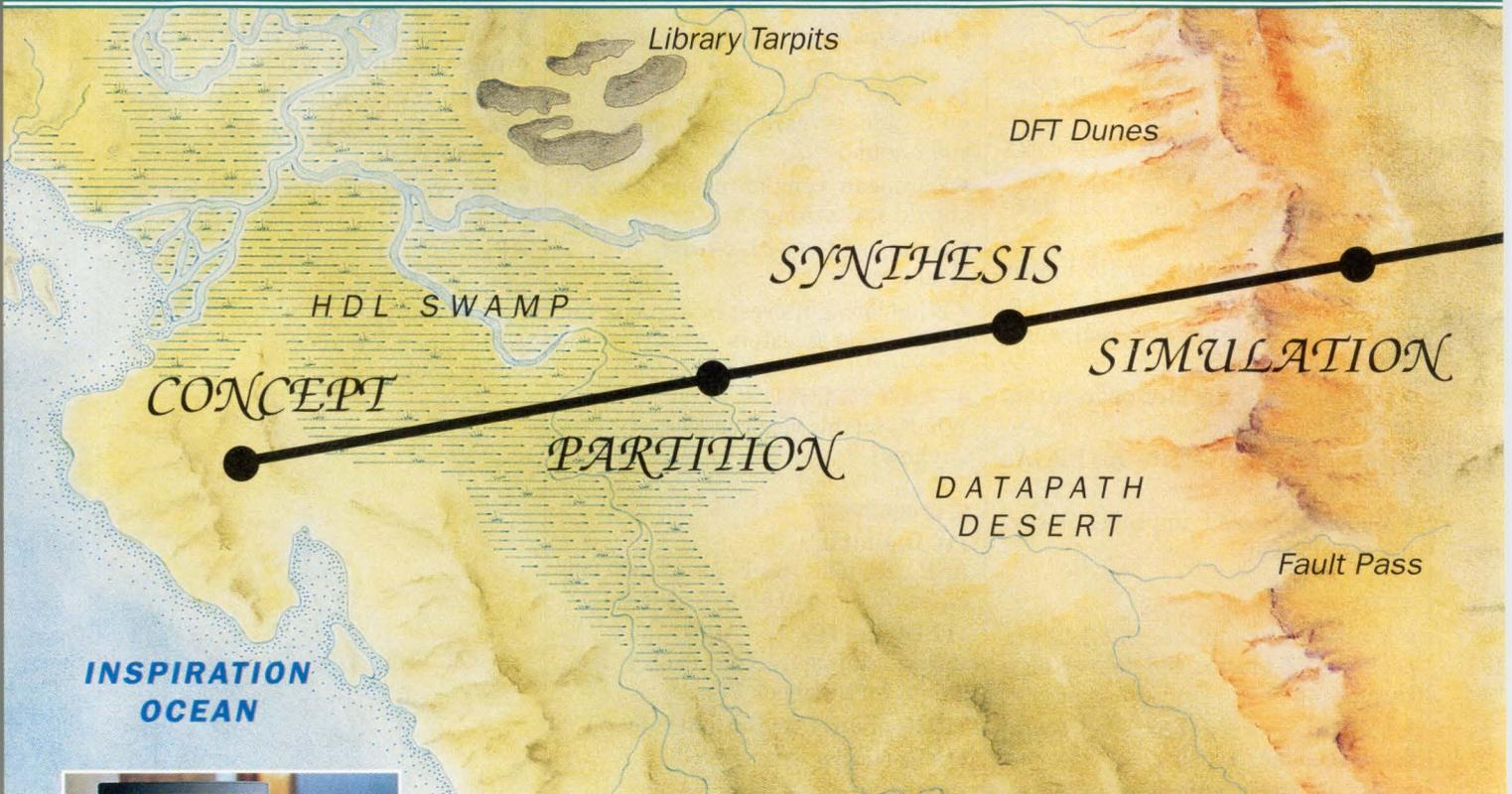
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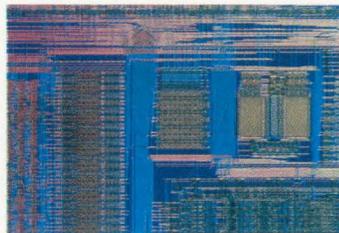
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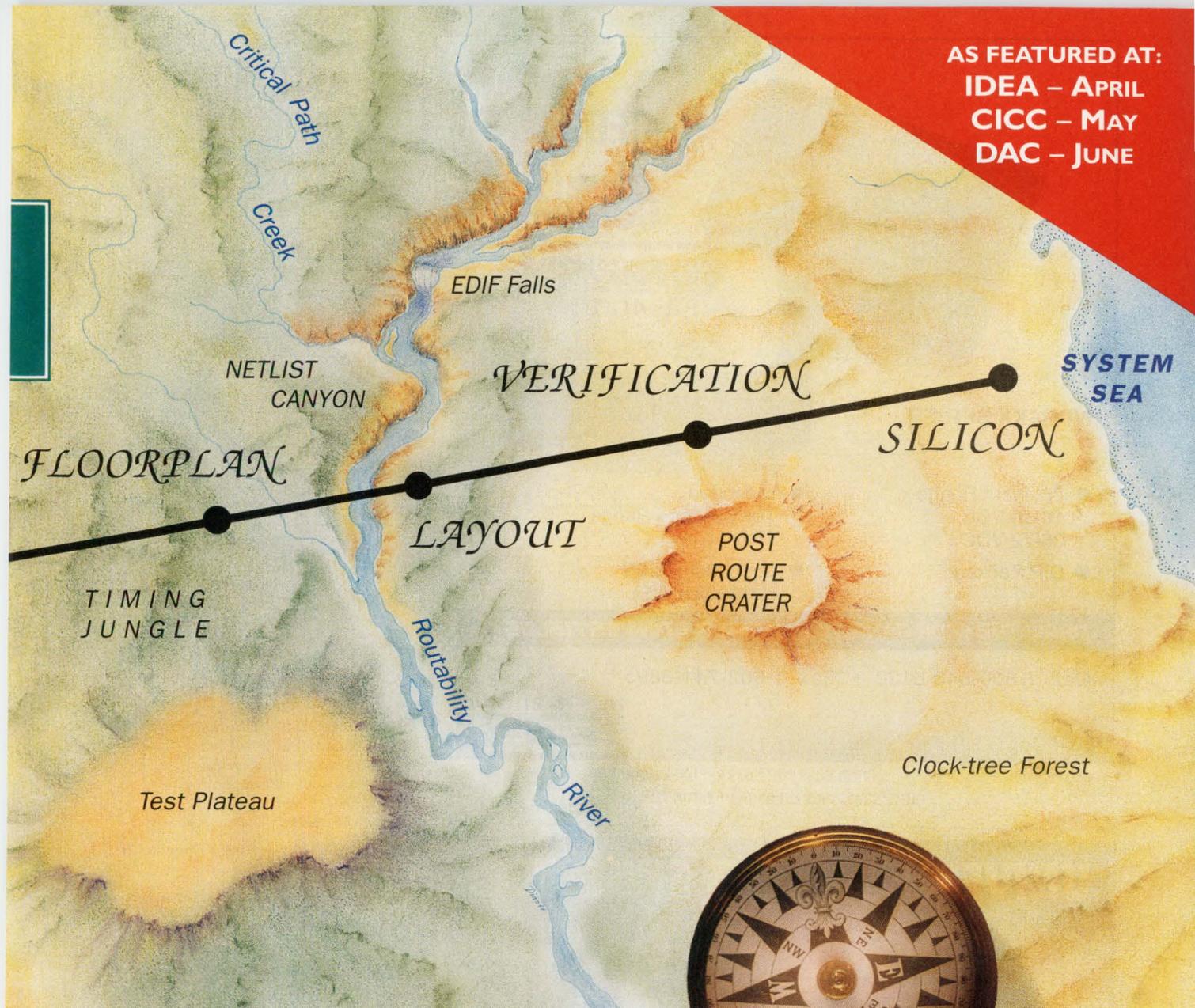
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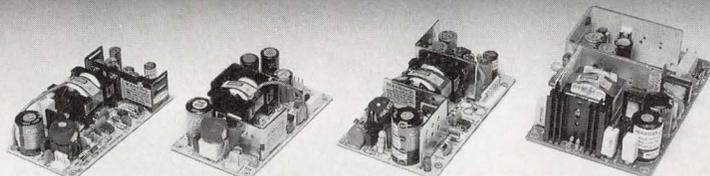
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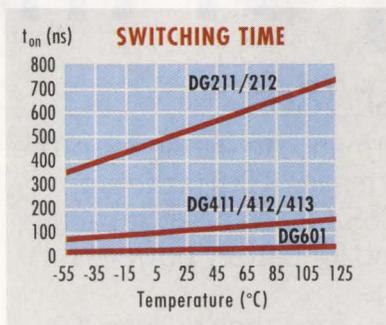
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EDITORIAL

CONGRESS MEETS THE NSF

The mid-1980's study conducted by the National Science Foundation — yes, the one that insidiously predicted a looming engineering shortage — has prompted an investigation by Congress of that organization. Hearings initiated by the House of Representatives' Subcommittee on Investigations and Oversight, part of the Science, Space, and Technology Committee, began in early April. For that hearing, the president of the American Engineering Association, Billy E. Reed, submitted written testimony that included the statement, "I do not know of a working-level engineer who believes the National Science Foundation is a friend of the engineering community." Here we have a U.S. government agency, the NSF, that is not "a friend of the engineering community," but rather has done harm to all engineers doing their part to improve the country's competitive technology stance.

According to an article in the San Jose Mercury News, "The National Science Foundation official who did the study, Peter House, defended it by telling the panel that he sought to depict a hypothetical situation. He said the study was never intended as a forecast of what might happen in the real world." Unfortunately, in that real world, real engineers have to practice their profession and earn their salaries.

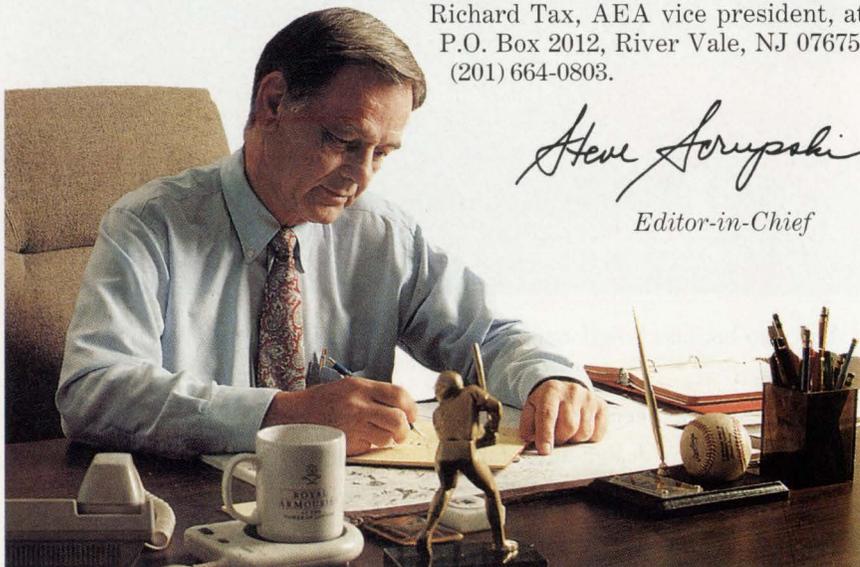
In his written testimony, AEA's Reed notes: "NSF itself has a vested interest in having a shortage. With a projected shortage, NSF is in a better position for additional funding, which keeps the bureaucracy expanding. The only loser is the working-level engineer who has no representation in the process."

Reed concludes with six recommendations: "Require any study or survey to be reviewed by an independent, neutral body before being released or 'leaked' to the public or press. This body should be representative of the engineering workforce...Require the effects of current market conditions to be considered as part of the overall study or survey as a leveling mechanism...Require NSF to spend as much resources and effort in 'recalling' a faulted report as is spent in publicizing the release of the report...Stop NSF from lobbying Congress on such issues as immigration, etc. It's one thing to testify on credible, scientific evidence, but quite another to spend taxpayer money to lobby for the NSF point of view...Place working-level engineers in areas of responsibility within this process...Stop funding ESP—engineering shortage propaganda. This money could be better spent to create jobs for engineers." Amen.

The American Engineering Association states its aims as being dedicated to enhancing the engineering profession and U.S. engineering capabilities. For

further information about AEA, contact Richard Tax, AEA vice president, at P.O. Box 2012, River Vale, NJ 07675; (201) 664-0803.

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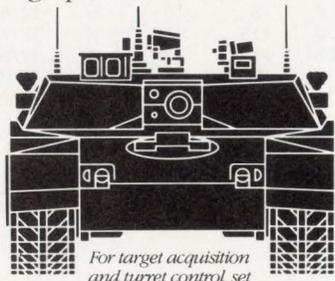


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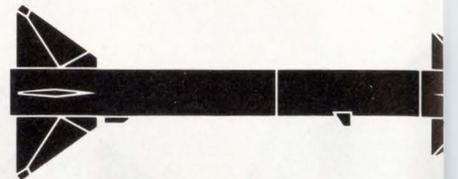
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Simple Switchers™ can drive a 1A load at 88% efficiency for one-fifth the cost of a DC-to-DC power converter. With just four external parts.

In fact, our LM1575K family of regulators — ideal for MIL-STD-704D/1275A systems — is easily customized in 30 minutes with our free software kit and three-step design procedure.



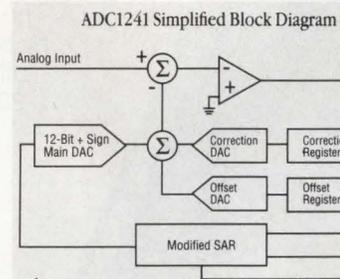
For target acquisition and turret control, set your sights on our self-calibrating ADC1241.



#24 12-Bit Plus Sign ADCs

SELF-CALIBRATION over time and temperature.

A dynamic feature that reduces parametric drifts,



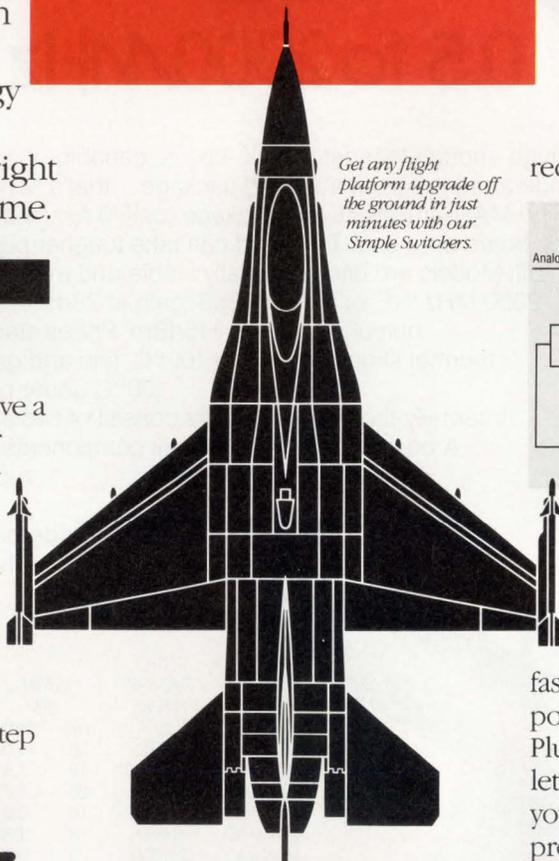
improves linearity and zero errors, and eliminates the need for external adjustments.

The ADC1241 is also fast (7.7 μ s) and extremely power conscious (40mW). Plus, its ± 5 V power supply lets you tap into the power of your existing logic and micro-processor supplies.

#49 Low-Noise CMOS Logic

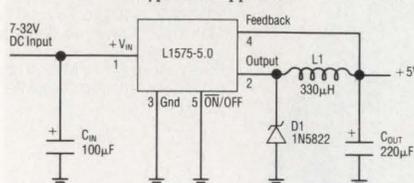
SILENT yet swift.

FACT Quiet Series™ cuts through device noise with guaranteed specs for dynamic



Get any flight platform upgrade off the ground in just minutes with our Simple Switchers.

Typical 5V Application



MIL/AERO UPGRADES

#63 #82

Launch your air-to-air missile upgrade with the precision of our 725MHz op amp.



threshold, undershoot, and ground bounce. And at speeds 15% faster than standard FACT™

No other logic can match

FACT QS 54ACTQ244 Specifications

	V _{OLP}	V _{OLV}	V _{IHD} *	V _{ILD} *	T _{skew}	ESD	Latchup
Max	1.5V	-1.2V	2.2V	0.8V	1.0ns	4,000V/min	300mA
Typical	1.0V	-0.5V	1.8V	1.4V	0.5ns	6,000V	1.0A

*V_{IHD}—Dynamic Input threshold high. *V_{ILD}—Dynamic Input threshold low.

the low noise, high speed, and low power of FACT QS, which is now available to Standard Military Drawings in CDIPs, Flatpaks, and LCCs.

Which means increased speed and accuracy for mission-critical upgrades in a single (LM6161/2/4, LM6165) or dual (LM6118) op amp. And increased stability too, because it drives large capacitive loads without oscillating.

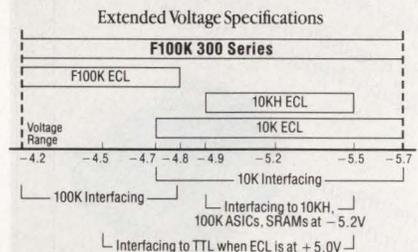
#82 Low-Power ECL Logic

LOW POWER that diets on picoseconds.

The performance and radiation tolerance (10⁶) of our ECL logic is out of this world.



voltage range allows easy upgrades in mil/aero systems that mix 10KH and/or TTL logic.



In sum, we bring more to your upgrades than sheer strength in numbers. We deliver bold new solutions with unmatched service and support. Not just now, but for the life of your design.

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Backed tomorrow.

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#63 High-Speed Op Amps

LIGHTNING FAST precision.

All AC parameters are 100% tested over the mil-temp range to guarantee hyper speeds (up to 725MHz) and pinpoint precision (offset of 1mV).

Now low power can co-exist with searing speeds. Without coolants.

300 Series' power consumption is ≤ 10KH and < TTL and CMOS at 50MHz and above. And with no fans in sight.

What's more, its extended



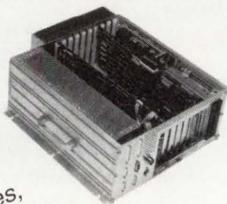
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TECHNOLOGY BRIEFING

EUROPE INITIATES NEW PATENT

American innovators – if you want to protect your invention, your intellectual property, in Europe, something new is looming on the horizon: the Community Patent. The patent will be issued on the basis of a single application and a common grant procedure, yet it will protect an invention in all countries belonging to the EC, the 12-nation European Community. It will also be valid in non-EC countries if they have ratified the European Patent Convention.

The new patent complements the European Patent that has been around for nearly 14 years. The latter is effectively a national patent in each country for which it's granted, and the protection it confers is limited to that country's territory. The Community Patent, by contrast, will be a truly supranational industrial property right, offering uniform protection in all member countries and transferable or revocable only unitarily.

By and large, patent experts at European electronics companies and American firms active in Europe welcome the new patent because it offers three basic advantages: simplicity, economy, and legal safety. It's simplicity is rooted in the fact that a single application in only one language can open the way to a patent that's valid virtually throughout Western Europe. It's economical because getting a Community Patent granted will cost less than seeking patent protection in, for example, three countries separately. And it's legally safe since the new patent is granted only after an extensive and thorough search of a data bank that presently contains more than 26 million documents (today, some countries issue national patents after only a cursory search, and all too often it turns out that these patents don't suit markets other than their home market).

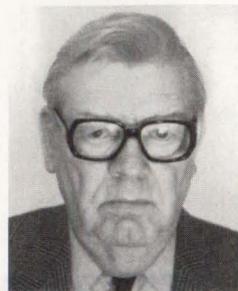
The only body to process applications and grant Community patents will be the European Patent Office (EPO) in Munich, Germany, and its sub-agencies. This means that applicants will deal with one authority instead of several national patent offices, says Rainer Osterwalder, spokesman for the EPO. There will also be a central European patents court, the Community Patents Appeals Court, which will decide litigation on infringements and validity of Community Patents and ensure that all provisions are uniformly applied.

Besides procedural simplification and the other advantages, the Community Patent and the EPO should also provide what Osterwalder calls a "fall-out" benefit. The unitary patent information policy and the EPO's big resources in data processing will help reduce the duplication of development efforts at companies. According to EC sources, re-inventions cost Europe's industry up to \$24 billion a year – an obvious waste of resources.

The Community Patent doesn't mean inventors can no longer seek "established" patents. There are still three other options. First, firms can apply for a national patent in any European country where they wish to do business. Second, they can seek an international patent in any of the 49 countries (including those in Europe) that are members of the Patent Cooperation Treaty. And third, as during the past 14 years, companies can apply for the European Patent.

The procedure for filing a Community Patent application is identical to that for the older European Patent. First, of course, the patent to be registered must meet basic criteria. It must constitute a novelty; it must reveal an inventive step or new principle (one that's not obvious to the skilled person); and it must be industrially applicable. The application must be filed in one of the EPO's three official languages – English, French, or German. The applicant needs to designate only one of the countries that ratified the European Patent Convention to have the patent treated as a Community Patent valid in all member countries.

For more information on the Community Patent, contact Rainer Osterwalder, European Patent Office, Erhardstrasse 27, D-8000 Munich 2, Germany. Phone: (0049)89-23990; fax: (0049)89-2399-2850.



JOHN GOSCH
FIELD EDITOR

Data Acquisition and Control System

Status Panel

Temperature

23.14

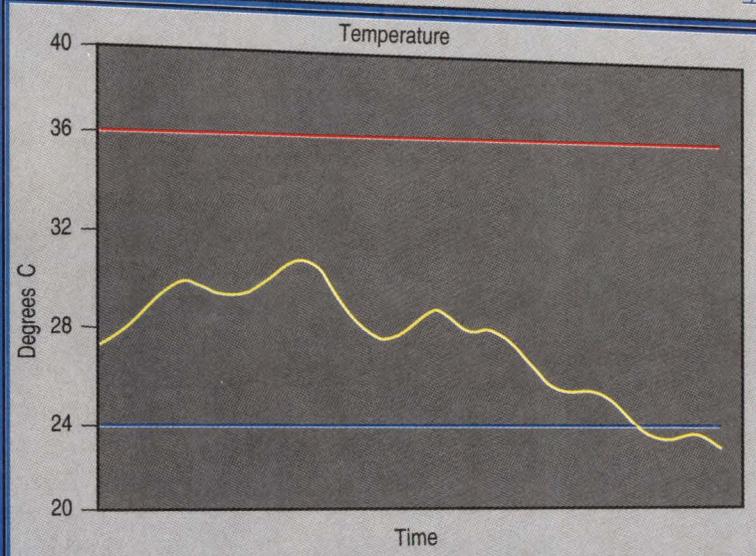
Flow Rate

64.21

Pressure

31.07

System: Active
 Valve Status:
 Valve#1: Open
 Valve#2: Open
 Overflow: Closed
 Heating Unit Status:
 Unit#1: 72%
 Unit#2: 76%
 Unit#3: 66%
 Data Logging: Active



Control Panel

Limits

36

Alarms

Upper

24

Lower

Display

Emergency System Shutdown

On

Off



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2. Turn on Computer
3. Launch LabWindows

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lowpass, highpass, bandpass

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low pass, Plug-in, dc to 1200MHz

Model No.	Passband MHz loss < 1dB	Stopband, MHz loss > 20dB	loss > 40dB	Model No.	Passband MHz loss < 1dB	Stopband, MHz loss > 20dB	loss > 40dB
PLP-5	DC-5	8-10	10-200	PLP-250	DC-225	320-400	400-1200
PLP-10.7	DC-11	19-24	24-200	PLP-300	DC-270	410-550	550-1200
PLP-21.4	DC-22	32-41	41-200	PLP-450	DC-400	580-750	750-1800
PLP-30	DC-32	47-61	61-200	PLP-550	DC-520	750-920	920-2000
PLP-50	DC-48	70-90	90-200	PLP-600	DC-680	840-1120	1120-2000
PLP-70	DC-60	90-117	117-300	PLP-750	DC-700	1000-1300	1300-2000
PLP-90	DC-81	121-137	167-400	PLP-800	DC-720	1080-1400	1400-2000
PLP-100	DC-98	146-189	189-400	PLP-850	DC-760	1100-1400	1400-2000
PLP-150	DC-140	210-300	300-600	PLP-1000	DC-900	1340-1750	1750-2000
PLP-200	DC-190	290-390	390-800	PLP-1200	DC-1000	1620-2100	2100-2500

Price, (1-9 qty), all models: plug-in \$14.95, BNC \$32.95, SMA \$34.95, Type N \$35.95

Surface-mount, dc to 570MHz

Model No.	Passband MHz loss < 1dB	Stopband, MHz loss > 20dB	loss > 40dB	Model No.	Passband MHz loss < 1dB	Stopband, MHz loss > 20dB	loss > 40dB
SCLF-21.4	DC-22	32-41	41-200	SCLF-190	DC-190	290-390	390-800
SCLF-30	DC-30	47-61	61-200	SCLF-380	DC-380	580-750	750-1800
SCLF-45	DC-45	70-90	90-200	SCLF-420	DC-420	750-920	920-2000
SCLF-135	DC-135	210-300	300-600				

Price, (1-9 qty), all models: \$11.45

Flat Time Delay, dc to 1870MHz

Model No.	Passband MHz loss < 1.2dB	Stopband MHz loss > 10dB	loss > 20dB	VSWR Freq. Range, DC thru 0.2fco	DC thru 0.6fco	Group Delay Variations, ns Freq. Range, DC thru	fco	2fco	2.67fco
PBPL-39	DC-23	78-117	117	1.3:1	2.3:1	0.7	4.0	5.0	
PBPL-117	DC-65	234-312	312	1.3:1	2.4:1	0.35	1.4	1.9	
PBPL-156	DC-94	312-416	416	0.3:1	1.1:1	0.3	1.1	1.5	
PBPL-200	DC-120	400-534	534	1.6:1	1.9:1	0.4	1.3	1.6	
PBPL-300	DC-180	600-801	801	1.25:1	2.2:1	0.2	0.6	0.8	
PBPL-467	DC-280	934-1246	1246	1.25:1	2.2:1	0.15	0.4	0.55	
▲BPL-933	DC-560	1866-2490	2490	1.3:1	2.2:1	0.09	0.2	0.28	
▲BPL-1870	DC-850	3740-6000	5000	1.45:1	2.9:1	0.05	0.1	0.15	

Price, (1-9 qty), all models: plug-in \$19.95, BNC \$36.95, SMA \$38.95, Type N \$39.95

NOTE: ▲ - 933 and -1870 only with connectors, at additional \$2 above other connector models.

high pass, Plug-in, 27.5 to 2200MHz

Model No.	Stopband MHz loss < 40dB	loss < 20dB	Passband MHz loss < 1dB	VSWR Pass-band Typ.	Model No.	Stopband MHz loss < 40dB	loss < 20dB	Passband MHz loss < 1dB	VSWR Pass-band Typ.
PHP-25	DC-13	13-19	27.5-200	1.8:1	PHP-400	DC-210	210-290	395-1600	1.7:1
PHP-50	DC-20	20-26	41-200	1.5:1	PHP-500	DC-280	280-365	500-1600	1.8:1
PHP-100	DC-40	40-55	90-400	1.8:1	PHP-600	DC-350	350-440	600-1600	2.0:1
PHP-150	DC-70	70-95	133-600	1.8:1	PHP-700	DC-400	400-520	700-1800	1.6:1
PHP-175	DC-70	70-105	160-800	1.5:1	PHP-800	DC-445	445-570	780-2000	2.1:1
PHP-200	DC-90	90-116	185-800	1.6:1	PHP-900	DC-520	520-660	910-2100	1.8:1
PHP-250	DC-100	100-150	225-1200	1.3:1	PHP-1000	DC-550	550-720	1000-2200	1.9:1
PHP-300	DC-145	145-170	290-1200	1.7:1					

Price, (1-9 qty), all models: plug-in \$14.95, BNC \$36.95, SMA \$38.95, Type N \$39.95

bandpass, Elliptic Response, 10.7 to 70MHz

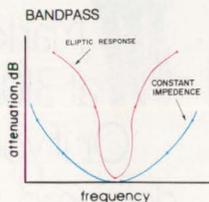
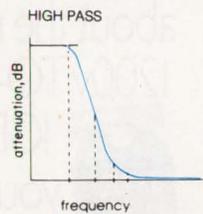
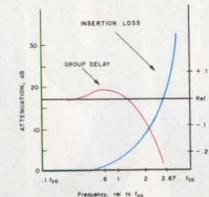
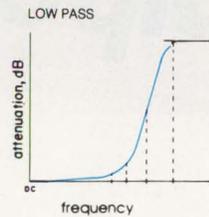
Model No.	Center Freq. (MHz)	Passband i.L. 1.5 dB Max (MHz)	3 dB Bandwidth Typ. (MHz)	Stopbands i.L. > 20dB at MHz	i.L. > 35dB at MHz
PBP-10.7	10.7	9.6-11.5	8.9-12.7	7.5 & 15	0.6 & 50-1000
PBP-21.4	21.4	19.2-23.6	17.9-25.3	15.5 & 29	3.0 & 80-1000
PBP-30	30.0	27.0-33.0	25-35	22 & 40	3.2 & 99-1000
PBP-60	60.0	55.0-67.0	49.5-70.5	44 & 79	4.6 & 190-1000
PBP-70	70.0	63.0-77.0	68.0-82.0	51 & 94	6.0 & 193-1000

Price, (1-9 qty), all models: plug-in \$18.95, BNC \$40.95, SMA \$42.95, Type N \$43.95

Constant Impedance, 21.4 to 70MHz

Model No.	Center Freq. MHz	Passband MHz loss < 1dB	Stopband loss > 20dB at MHz	VSWR 1.3:1 Total Band MHz
PIF-21.4	21.4	18-25	1.3 & 150	DC-220
PIF-30	30	25-35	1.9 & 210	DC-330
PIF-40	42	35-49	2.6 & 300	DC-400
PIF-50	50	41-58	3.1 & 350	DC-440
PIF-60	60	50-70	3.8 & 400	DC-500
PIF-70	70	58-82	4.4 & 490	DC-550

Price, (1-9 qty), all models: plug-in \$14.95, BNC \$36.95, SMA \$38.95, Type N \$39.95



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THIN-FILM FOUNDRY OFFERS SUPERCONDUCTORS

Stepping out of research papers and into reality, a first-of-its-kind foundry now offers thin-film high-temperature superconductor films. Superconductor Technologies Inc., Santa Barbara, Calif., will fabricate these films on 2-in. wafers. The company implemented various functions, such as a microwave phase shifter that demonstrates linear performance up to 36 W (developed as part of a contract with the Electronic Warfare division of Wright Laboratory at the Wright-Patterson Air Force Base). To handle the high power, the firm created a novel conductor configuration that prevents damage to the thin films. Other devices fabricated with the 77K thin films include a Schiffman phase detector and delay lines. The phase shifter demonstrated an $86^\circ \pm 2^\circ$ phase effect over a 2.4-GHz bandwidth at 6.5 GHz, and its insertion loss is less than 0.1 dB at 77K. The superconducting thin films consist of thallium compounds on a lanthium-aluminum-oxide (LaAlO_3) substrate. Foundry services can create 0.01- or 0.02-in.-thick films. Prices range from \$175 for a 1-cm² gold film, to over \$11,000 for a 2-in. double-sided wafer with the thallium thin films. Custom fabrication services like patterning start at \$250 for a 1-cm² chip. Design kits containing substrates and even a cold test fixture are available as well. Off-the-shelf resonators with frequencies of 2.3 or 5 GHz and Qs of greater than 10,000 or 8000, respectively, are available for evaluation and sell for \$1500 each. Contact Jim Bybokas at (805) 683-7646. *DB*

SEE THE LATEST IN EDA TECHNOLOGY FOR FREE

Free passes to the opening day of the Design Automation Conference (DAC) make it easier than ever for engineers to see the latest in EDA technology. Attendees will find valuable information at this year's DAC, which takes place June 8-12 in Anaheim, Calif. The conference features more than 125 exhibits that showcase the latest in EDA technology. Technical sessions will focus on user problems and solutions, including obstacles encountered with frameworks, standards, and tools. High-level executive sessions cover such topics as "Directions to watch in design technology," and "Why data models will become the fastest-growing segment of the EDA market." In addition to the first-day free passes, "exhibits only" admission can be purchased at the door at any time for \$35. For a "Free Monday" pass, call (800) 321-4573 no later than May 15. *LM*

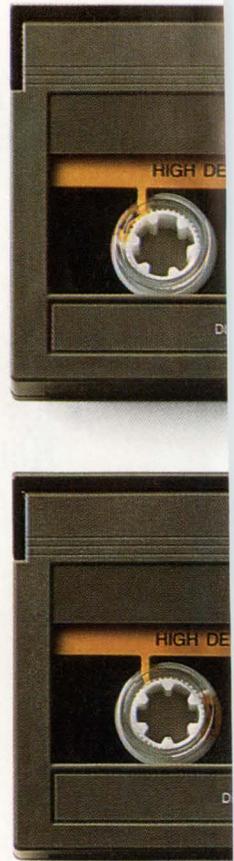
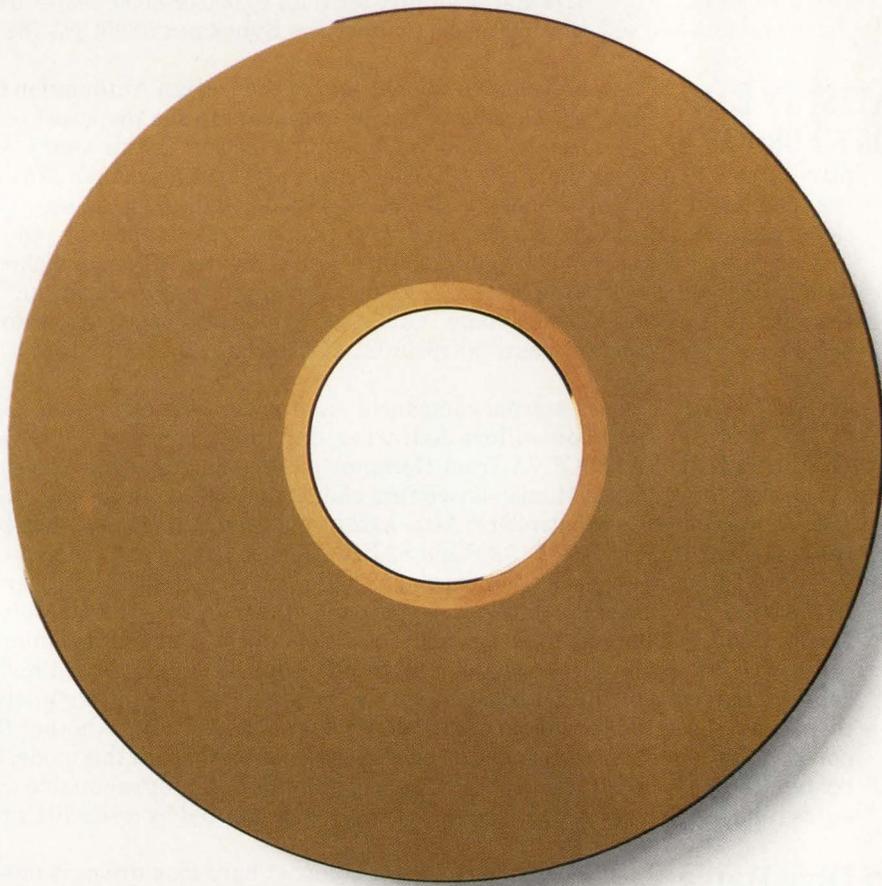
8-BIT MICROCONTROLLERS HOLD 2.25-KBYTE RAM

Fewer external components and lower cost can be achieved with two 8-bit microcontrollers featuring expanded memory. The SAB80C515A and SAB80C517A from Germany's Siemens AG offer 1.25 and 2.25 kbytes of RAM, respectively. The Munich-based firm claims that they contain more memory than other 8051-compatible microcontrollers. Also, a 32-kbyte program memory has been integrated in the corresponding SAB83C515A-5 and SAB83C517A-5 ROM versions. Now available, the devices use a maximum clock frequency of 18 MHz, which increases CPU performance by 50%. In the 80C517A, fast computation is supported by the integrated 32-bit multiply/divide unit—two 32- and 16-bit operands can be divided in 4 μs —and by eight data pointers. The controllers come with intelligent and powerful integrated peripheral modules. A 10-bit analog-to-digital converter offers a resolution of about 5 mV with either 8 or 12 input channels. The 80C515A incorporates three 16-bit-wide timers for digital-signal generation. Another first is a hardware power-down mode that's switched on and off via a control line. In this mode, the ports go to the tristate condition to further reduce power consumption. A programmable watchdog timer ensures reliable CPU operation. The clock supply is monitored by an oscillator watchdog. *JG*

SMART DISK-DRIVE SPINDLE MOTOR COMING

A smart spindle motor for compact hard-disk drives is one goal of an agreement between the Italian-Franco firm SGS-Thomson Microelectronics of Milan and Paris, and Nippon Densan Co. (Nidec), Kyoto, Japan. SGS-Thomson will furnish a specially developed power IC that doesn't need external components, and Nidec will design, manufacture, and market a miniature brushless motor unit using this IC. The new spindle motor is expected to become available later this year. The smart motor consists of a small three-phase sensorless, brushless motor containing a smart IC physically integrated with the motor body. The new device offers many benefits to disk-drive designers. For example, Nidec's proprietary sensorless double-step startup is built into the unit, guaranteeing high reliability in startup. SGS-Thomson's smart-power technology ensures that the chip operates at high efficiency and works on 3-to-5-V supplies, consuming little current. Other benefits include savings in board space and reduced design time. Applications for the new disk drives are not only seen in laptop, notebook, and palmtop computers, but because they're inexpensive, they're also looking toward fax machines and high-capacity removable cartridges. The chip's bipolar-CMOS-DMOS technology allows any mix of control and power circuits to be housed on one IC, with power dissipation so low that no special packaging is needed. *JG*

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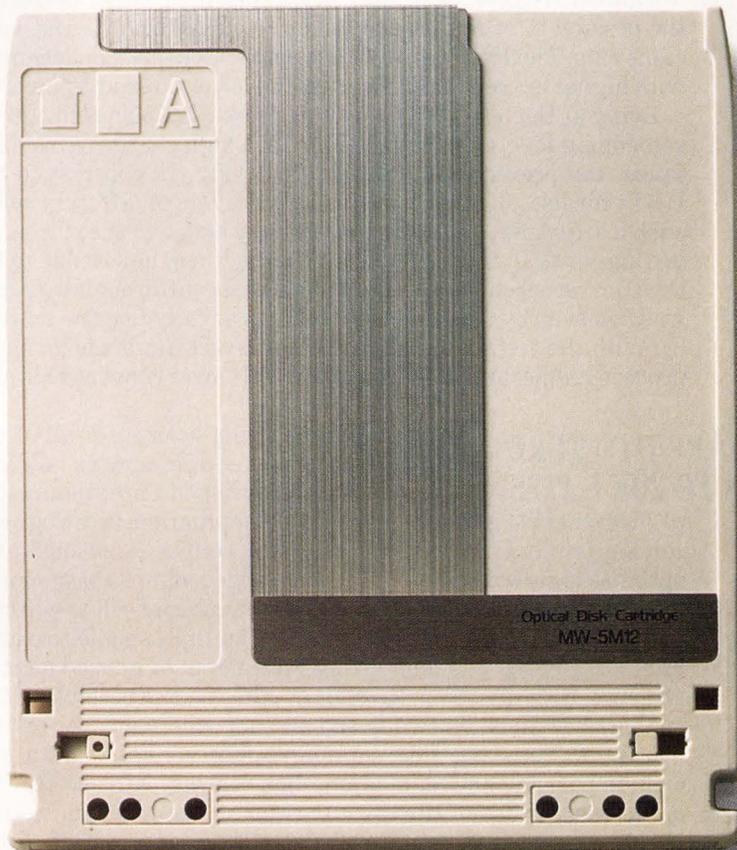
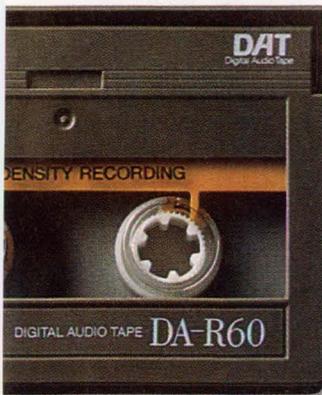
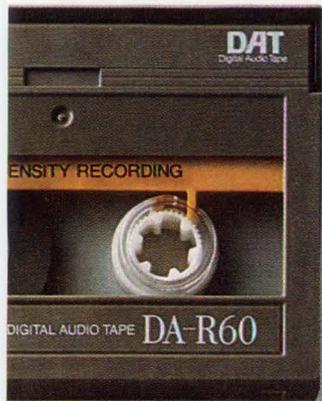
In fact, the pitter-patter of smaller footprints has encouraged us to build a considerable library of packaging options for newer areas such as VSOP, QFP and Chip-on-Flex.

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VHDL MEETING STRESSES REAL-WORLD DESIGN USE

The VHDL International Users' Forum, taking place May 3-6 in Scottsdale, Ariz., will provide a comprehensive, technical update of industry, academic, government, and international-related VHDL efforts designed to benefit all levels of VHDL users and developers. The technical program has 12 sessions focused on the research efforts currently underway within the industry, as well as the drive to better understand uses for VHDL in system design, test, and manufacturing. Forum papers will include such topics as synthesis, acceleration techniques, analog and back annotation, and the use of VHDL in ASIC and FPGA design. In addition, four tutorial programs will be offered for both novice and experienced VHDL users, and users can gain hands-on experience with the latest tools in the supplier suites. For more information on the show, call (800) 554-2550. *LM*

HBT SILICON TRANSISTOR OPERATES UP TO 53 GHZ

A silicon-based heterojunction bipolar transistor (HBT) that can handle frequencies up to 53 GHz has been developed by the Daimler-Benz Research Laboratories, the Ulm-based research facilities of the major German producer of Mercedes-Benz cars and trucks. According to the company, only IBM Research Labs in Yorktown Heights, N.Y., has attained similar speed performance. This development leaves the possibility of integrating high-frequency devices and conventional silicon circuits on the same chip. The HBT outperforms conventional silicon technologies not only in speed, but also with higher current amplification and lower noise and power consumption.

Lying at the heart of the new transistor is a 50-nm silicon-germanium base layer. High boron doping levels are responsible for a high charge carrier density. This creates a low resistance, the prerequisite for fast switching. In contrast to conventional silicon transistors, HBTs consist not just of silicon, but of layers of different semiconducting material. To obtain such a structure, germanium is usually added to the silicon. Even though germanium atoms are bigger than those of silicon, making them impossible to fit into the silicon crystal lattice, the Ulm researchers managed to make the different layers monocrystalline throughout. This was achieved by using molecular-beam epitaxy to grow extremely thin layers atop one another. With the technique, all transistor layers are made in one process. HBTs also offer lower process temperatures—typically 550°C—over conventional silicon structures. *JG*

ENHANCED ARCHITECTURE UPS FPGAS TO 20K GATES

Taking advantage of its license for all of the Xilinx patents on the RAM-based programmable-logic arrays, AT&T Microelectronics, Berkeley Heights, N.J., has developed a proprietary architecture that hosts from 3000 to 20,000 usable gates. Dubbed ORCA (optimized, reconfigurable cell architecture), the forthcoming family of arrays includes 64-bit configurable lookup tables in each logic block to help optimize logic utilizations. With the large lookup tables, more logic can be combined into one programmable logic cell, reducing the number of cell-to-cell critical paths. The same lookup tables can also be configured to perform multiple smaller functions, reducing the need for large numbers of cells and minimizing the amount of unused logic. Three major types of functions are supported by the arrays: data path, user-accessible SRAM, and glue logic. Data paths enable operations on two bused signals, whether 4-, 8-, or 16-bits wide, and perform nibble-wide operations at a time—a unique feature. For routing resources, the ORCA family will include passive, active, and long-line routing paths so that the automatic routing tools can optimize their use of the resources for short-, medium-, and long-distance routes. The initial family member will contain 3000 usable gates and pack 120 I/O pads; the largest will have 20,000 usable gates and offer 288 I/O lines. Contact Ajay Shingal at (215) 439-6004. *DB*

MODEL APPROACH IMPROVES LOSSY-LINE SIMULATION

By using a distributed-model approach rather than the traditional lumped-model approach, the PSpice software can simulate lossy transmission lines in significantly less time while producing a more accurate approximation of the line's behavior. The distributed model, developed by MicroSim Corp., Irvine, Calif., simulates a continuous line that's specified by electrical length and resistance, inductance, capacitance, and conductance distributed along its entire length. From this, the line's behavior is computed using impulse responses. This technique avoids the overhead introduced by the lumped-model approach that describes the lossy line as a string of line segments, and has each segment modeled with discrete passive components. Moreover, the lumped-model approach produces oscillations at points where abrupt changes occur in the signal traveling along the transmission line. In PSpice, these frequency artifacts are eliminated by modeling lossy lines as continuous lines. Call MicroSim at (800) 245-3022 or (714) 770-3022 for more information. *LM*

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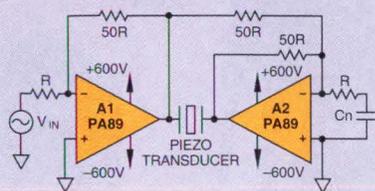
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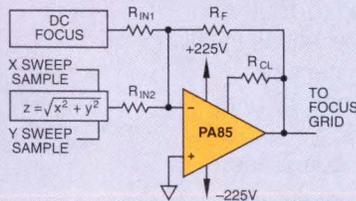
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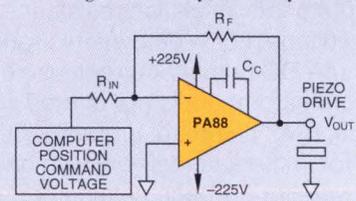
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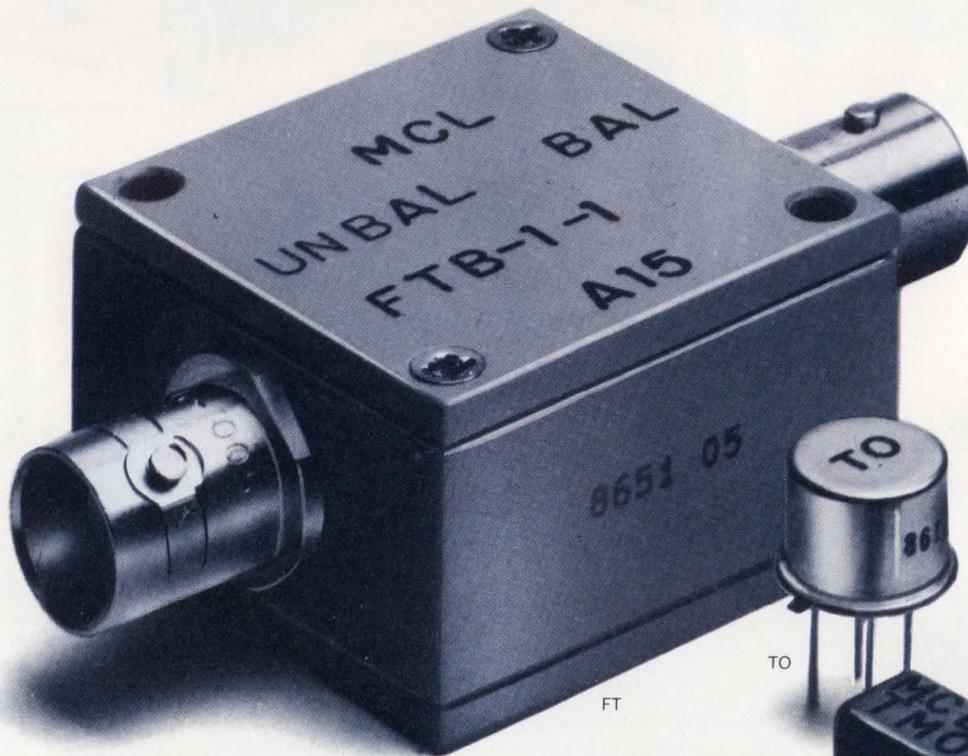
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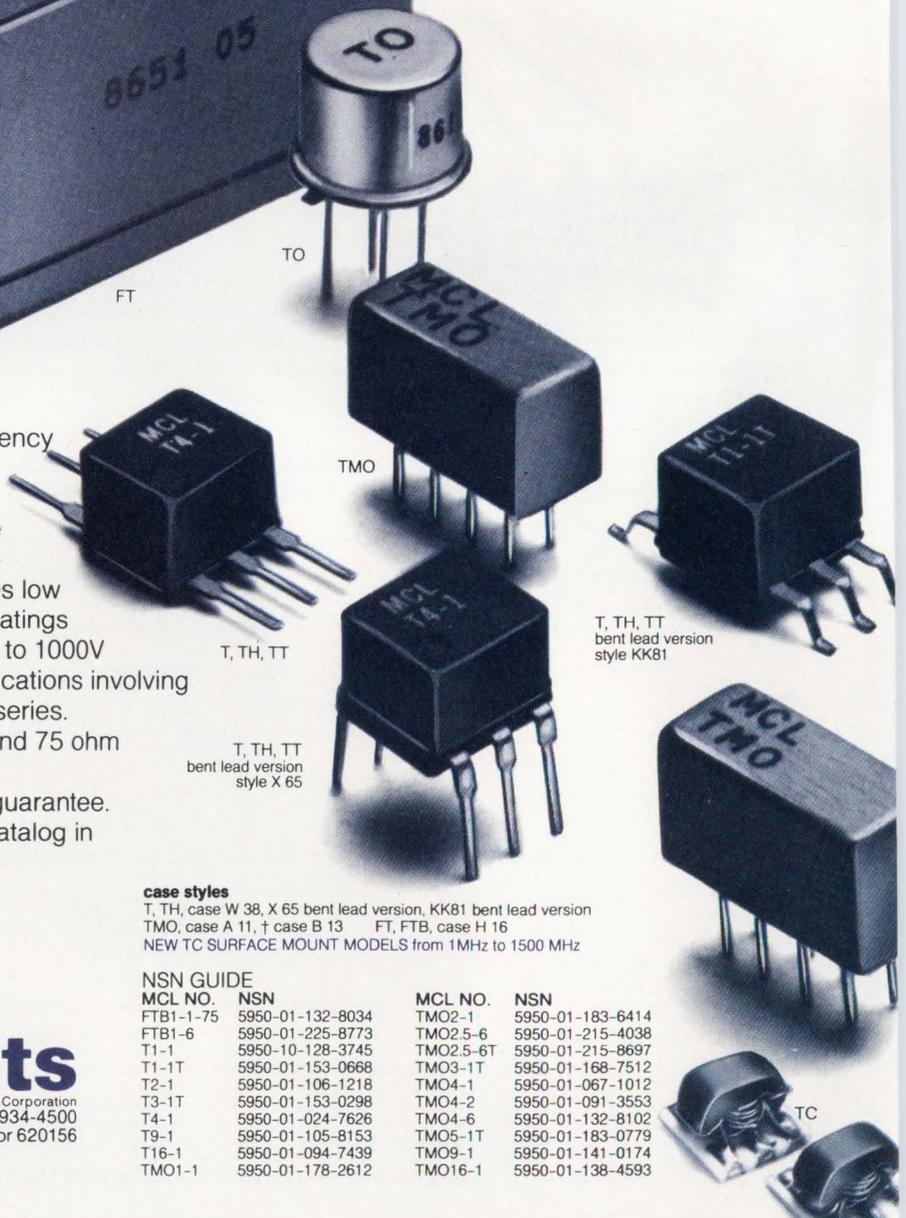


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case styles

T, TH, case W 38, X 65 bent lead version, KK81 bent lead version
TMO, case A 11, † case B 13 FT, FTB, case H 16
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NSN GUIDE

MCL NO.	NSN	MCL NO.	NSN
FTB1-1-75	5950-01-132-8034	TMO2-1	5950-01-183-6414
FTB1-6	5950-01-225-8773	TMO2.5-6	5950-01-215-4038
T1-1	5950-10-128-3745	TMO2.5-6T	5950-01-215-8697
T1-1T	5950-01-153-0668	TMO3-1T	5950-01-168-7512
T2-1	5950-01-106-1218	TMO4-1	5950-01-067-1012
T3-1T	5950-01-153-0298	TMO4-2	5950-01-091-3553
T4-1	5950-01-024-7626	TMO4-6	5950-01-132-8102
T9-1	5950-01-105-8153	TMO5-1T	5950-01-183-0779
T16-1	5950-01-094-7439	TMO9-1	5950-01-141-0174
TMO1-1	5950-01-178-2612	TMO16-1	5950-01-138-4593

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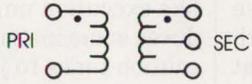
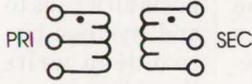
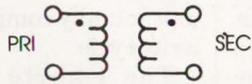
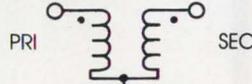
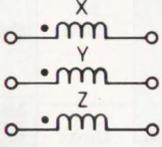
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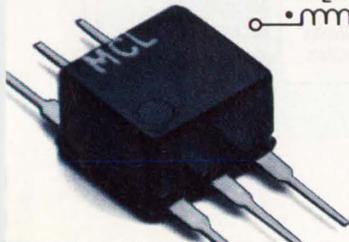
case style number see opposite page	MODEL NO.	Ω RATIO	FREQUENCY MHz	INSERTION LOSS			PRICE \$ Qty. (1-9)		
				3dB MHz	2dB MHz	1dB MHz			
A* 	T	T1-1T	1	05-200	05-200	08-150	2-80	4.45	
		T1-6T	1	003-300	003-300	01-150	02-50	6.95	
		T2-1T	2	07-200	07-200	1-100	5-50	4.95	
		T2.5-6T	2.5	01-100	01-100	02-50	50-20	4.95	
		T3-1T	3	05-250	05-200	1-200	5-70	4.95	
		T4-1	4	2-350	2-350	35-300	2-100	3.25	
		T4-6T	4	02-250	02-250	05-150	0.1-100	4.45	
		T5-1T	5	3-300	3-300	6-200	5-100	4.95	
		T8-1T	8	03-140	03-140	10-90	1-60	7.95	
		T13-1T	13	3-120	3-120	7-80	5-20	4.95	
		T16-6T	16	03-75	03-75	06-30	1-20	5.65	
		T4-1H	4	10-350	10-350	15-300	25-200	5.95	
		TH	TMO1-1T	1	05-200	05-200	08-150	2-80	7.95
			TMO2-1T	2	07-200	07-200	1-100	5-50	8.45
			†TMO2.5-6T	2.5	01-100	01-100	02-50	05-20	8.45
			†TMO3-1T	3	05-250	05-250	1-200	5-70	7.95
			TMO4-1	4	2-350	2-350	35-300	2-100	6.25
TMO	TMO5-1T	5	3-300	3-300	6-200	5-100	8.45		
	TMO13-1T	13	3-120	3-120	7-80	5-20	8.45		
B* 	TT	TT1-6	1	004-500	004-500	02-200	1-50	6.95	
		TT1.5-1	1.5	075-500	075-500	2-100	1-50	5.95	
		TT2.5-6	2.5	01-50	01-50	025-25	05-10	6.45	
		TT4-1	3	05-200	2-50	2-50	1-30	5.95	
		TT4-1A	4	0.1-300	0.1-300	0.2-250	0.3-180	6.95	
		TT25-1	25	02-30	02-30	05-20	1-10	9.95	
		TTMO	TTMO25-1	25	02-30	02-30	05-20	1-10	11.95
			TTMO1-1	1	005-100	005-100	01-75	05-40	11.45
			TTMO4-1A	4	0.1-300	0.1-300	0.2-250	0.3-180	13.95
		C 	T	T1-1	1	15-400	15-400	35-200	2-50
T1.18-3	1.18			0.01-250	0.01-250	0.02-200	0.03-50	5.65	
T1-6	1			01-150	01-150	02-100	05-50	5.65	
T1.5-1	1.5			1-300	1-300	2-150	5-80	4.45	
T1.5-6	1.5			02-100	02-100	05-50	0.1-25	5.65	
T2.5-6	2.5			01-100	01-100	02-50	05-20	4.45	
T4-6	4			02-200	02-200	05-150	1-100	4.45	
T9-1	9			15-200	15-200	3-150	2-40	3.95	
T16-1	16			3-120	3-120	7-80	5-20	4.45	
T36-1	36			03-20	03-20	05-10	1-5	6.95	
TO	TO-75			1	10-500	—	10-500	40-250	6.95
	T1-1H			1	8-300	8-300	10-200	25-100	5.95
	T9-1H			9	2-90	2-90	3-75	6-50	6.45
TH	T16-H			16	7-85	7-85	10-65	15-40	6.45
	TMO								
	TMO1-02			1	1-800	1-800	2-500	—	9.45
TMO1-1	1			15-400	15-400	35-200	2-50	6.25	
TMO1.5-1	1.5			1-300	1-300	2-150	5-8	8.45	
†TMO2.5-6	2.5			01-100	01-100	02-50	05-20	7.95	
†TMO4-6	4			02-200	02-200	05-150	1-100	7.95	
TMO6-1	6	3-200	3-200	5-150	5-50	7.95			
TMO9-1	9	15-200	15-200	3-150	2-40	7.95			
TMO16-1	16	3-120	3-120	7-80	5-20	7.95			
D 	T	T2-1	2	050-600	050-600	1-400	5-200	3.95	
		T3-1	3	5-800	5-800	2-400	—	4.45	
		T4-2	4	2-600	2-600	5-500	2-250	3.95	
		T8-1	8	15-250	15-250	25-200	2-100	3.95	
		T14-1	14	2-150	2-150	5-100	2-50	4.95	
		TMO	TMO2-1	2	050-600	050-600	1-400	5-200	7.95
			TMO3-1	3	5-800	5-800	2-400	—	8.45
			TMO4-2	4	2-600	2-600	5-500	2-250	7.95
			TMO8-1	8	15-250	15-250	25-200	2-100	7.95
		FT	TMO14-1	14	2-150	2-150	5-100	2-50	8.45
FT1.22-1	1.22		005-100	005-100	01-50	05-25	35.95		
FT1.5-1	1.5	1-400	1-400	5-200	1-100	35.95			
E 	FTB	FTB-1	1	2-500	2-500	5-300	1-100	36.95	
		FTB1-6	1	01-125	01-125	05-50	1-25	36.95	
		■FTB-1-75	1	5-500	5-500	5-300	10-100	36.95	
F 	T	T-622	1	0.1-200	0.1-200	0.5-100	5-80	3.25	
		T626	1	0.01-10	0.01-10	0.2-5	0.4-2	3.95	

■ Denotes 75 ohm models

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C72-2 REV. B

MULTILEVEL PIPELINE AND 1-KBYTE CACHE LET 16-BIT-BUS 486 DELIVER HIGH THROUGHPUT

Developing an 80486-instruction-compatible CPU might be considered a difficult-enough task, but redesigning the CPU to deliver high throughput while restricting the external bus to just 16 bits could be viewed as masochistic. However, designers at Cyrix Corp., Richardson, Texas, went to that extreme. They put a 486-software compatible CPU into a low-cost 80386SX 100-lead plastic quad-sided flat package. The result is a chip that delivers close to 486SX performance at a price competitive with the 80386SX or SL microprocessor (see "486 workalike retains 386SX bus, pinout for notebook PCs," p. 117).

Engineers applied a unique design methodology to the Cx486SLC, which they feel will guarantee compatibility while leaving

room for innovation. The approach employs a proprietary algorithm that allows the company to model any kind of programmable chip. The behavioral model then develops the logic design. Before committing the design to silicon, it's subjected to extensive simulations, both behavioral and logic.

With compatibility guaranteed by the design methodology, the designers of the new chip were able to innovate on the chip's architecture. The Cx486SLC achieves 486-level performance by employing an optimized variable-length pipeline combined with a RISC-like execution unit, a 1-kbyte integrated instruction and data cache, and an on-chip 16-bit hardware multiplier (see the diagram).

The execution path consists of five pipeline stages

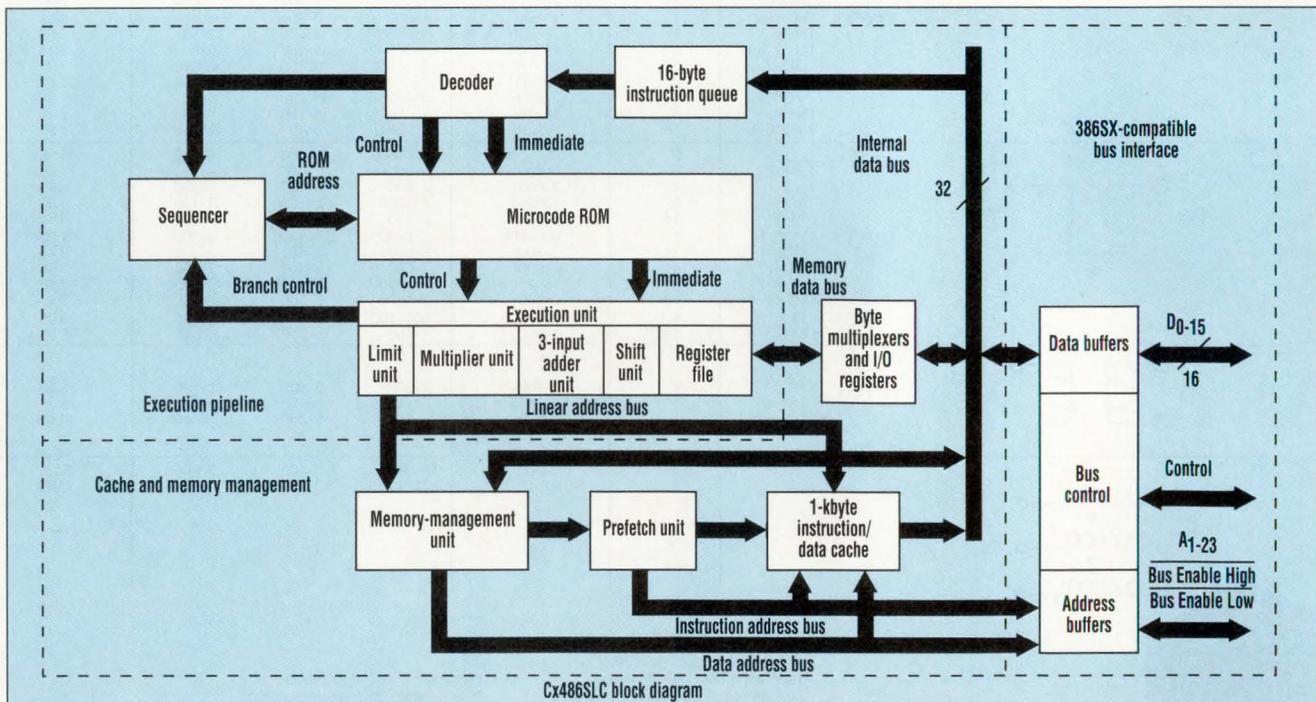
that allow successive instruction overlap, which results in minimal instruction cycle times. The five stages are: code fetch, instruction decode, microcode ROM access, execution, and memory/register file write back. These stages were designed with hardware interlocks that permit successive instruction-execution overlap. Furthermore, a number of the instructions were reduced to single-cycle execution, improving overall CPU efficiency.

A 16-byte instruction prefetch queue fetches code in advance and prepares it for decoding, helping minimize overall execution time. The instruction decoder then decodes four bytes of instructions per clock, eliminating the need for a queue of decoded instructions. Sequential instructions are decoded

quickly and given to the microcode. Non-sequential operations needn't wait for a queue of decoded instructions to be flushed and refilled before execution continues. As a result, both sequential and non-sequential instruction times are minimized.

The execution stage takes advantage of a RISC-like execution unit that reduces some instruction execution times to just a single cycle, and a 16-bit hardware multiplier that accelerates integer multiplications. A write-back cache algorithm provides single-cycle 32-bit access to the on-chip cache and posts all writes to the cache and system bus using a two-deep write buffer. Posted writes enable the execution unit to proceed with program execution while the bus-interface unit actually completes the write cycle.

The 1-kbyte on-chip cache maximizes overall performance by quickly



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supplying instructions and data to the internal execution pipeline. Although external data accesses are 16 bits, the internal cache reassembles the half-words into 32-bit words; all internal buses on the chip are 32 bits wide. An external memory access takes a minimum of two clock cycles (zero wait states). For cache hits, the new CPU eliminates these two clock cycles by overlapping cache accesses with normal-execution pipeline activity.

The combined pipeline-and-cache architecture allows cache accesses to run in parallel with normal-execution pipeline activity, resulting in cache hits that are two clock cycles faster than typical zero-wait-state external bus accesses. Additional bus bandwidth is gained by presenting instructions and data to the execution pipeline up to 32 bits at a time, compared with 16 bits per cycle for an external memory access.

The cache is a write-through unified-instruction-and-data cache. Lines are allocated only during memory read cycles. The cache can be configured as direct mapped or two-way set associative. The direct-mapped organization is a single set of 256 four-byte lines. When configured as two-way set-associative, the cache organization consists of two sets of 128 four-byte lines and employs a least-recently-used (LRU) replacement algorithm.

The 16-bit hardware multiplier added to the architecture speeds integer multiplies by as much as eight times over the shift-add multiply function in other 386 or 486 CPUs. A

faster multiply enhances the CPU's performance in such applications as graphics control and handwriting recognition. The hardware multiplier shows a 2X video-performance increase over 386 and 486 CPUs at the same clock speed, according to popular video benchmarks like Power Meter Aggregate Video.

In addition, by placing the display controller (for example, a VGA chip) on a local-bus interface rather than on the slow, 8-MHz AT bus, designers can eliminate the performance bottleneck of the AT bus and perform 16-bit transfers at the full CPU clock speed. That speeds up video performance by two- to six-fold over standard VGA. Handwriting recognition can also be accelerated without additional support logic, such as DSP chips.

During the early stages of chip development, the tests performed on the logic simulation are, of necessity, a subset of those that can be performed on the first silicon. However, by simulating thoroughly, the company was confident that the circuit would work the first time, eliminating the need for multiple chip iterations. In the case of the Cx486SLC, Kevin McDonough, vice president of engineering, said that only a few minor bugs were found in the first silicon. All of them were correctable by making changes only in the metallization mask. By not having to change all of the diffusion masks and create a second iteration of the silicon, Cyrix can deliver fully functional devices just weeks after receiving the

first samples.

The Cx486SLC CPU is the third product family developed by Cyrix using its proprietary design methodology. The other two families were math co-

processors: The first consists of the FasMath 83D87, 83S87, and 82S87; the second set includes the 87SLC and 87DLC.

JON CAMPBELL AND
DAVE BURSKY

INTERACTIVE TRACKBALL RELIES ON FORCE-FEEDBACK SENSING

The ubiquitous mouse and similar computer input devices haven't become artifacts in a museum yet, but that's where some may wind up if a new interactive man-machine interface reaches maturity and becomes a commercial product.

Under development at the Institute for Perception Research in Eindhoven, the Netherlands, the new device is a trackball that works with tactile feedback: Turning the ball with the finger or thumb, the user moves the cursor across the screen. If the cursor moves in an inappropriate direction, the ball, and hence the user, senses a resistive force. On the other hand, there's no such sensation or even a stimulating force if the cursor moves in the proper direction, which depends on the application.

Today's input devices, such as the mouse, touch screen, or the conventional trackball, are good but far from ideal. With the mouse, the cursor is made to shift across the screen by moving the whole device. The drawback is that the user must move the hand and the lower arm. What's more, the mouse and the arm movements take up much desk space.

In terms of eye-hand coordination, the directness

of data input for the touch screen is unsurpassed. But the user must lift the arm, and that obscures part of the screen. Also, in the long run, lifting the arm becomes tiresome.

As for the conventional trackball, it remains stationary and the cursor can be controlled even from an easy chair. The ball just needs to be moved with the fingers and the cursor will move with it. But there's no simple relationship between the ball's movement and that of the cursor. Because the straight cursor movements must be related to curved finger tracks across the ball, the cursor will easily shoot off in the wrong direction.

That's not the case with the new tactile-feedback trackball: The user, upon sensing the feedback force, will be guided to move the ball in another "proper" direction. Combining user comfort with directness of manipulation, the new device also diminishes the visual load, or eye strain, because the user goes by mostly what he or she feels.

The Dutch device makes for more user comfort principally because unnecessary cursor detours are avoided. Therefore, reaction is quicker to what's seen on the screen. Perception experts have found

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Since the FS700 receives the ground wave from the LORAN transmitter, reception is unaffected by atmospheric changes, with no possibility of missing cycles, a common occurrence with WWV due to discontinuous changes in the position of the ionosphere layer. Cesium and rubidium standards, in addition to being expensive initially, require periodic refurbishment, another costly item.

The FS700 system includes a remote active 8-foot whip antenna, capable of driving up to 1000 feet of cable. The receiver contains six adjustable notch filters and a frequency output which may be set from 0.01 Hz to 10 MHz in a 1-2-5 sequence. A Phase detector is used to measure the phase shift between this output and another front panel input, allowing quick calibration of other timebases. An analog output with a range of ± 360 degrees, provides a voltage proportional to this phase difference for driving strip chart recorders, thus permitting continuous monitoring of long-term frequency stability or phase locking of other sources.



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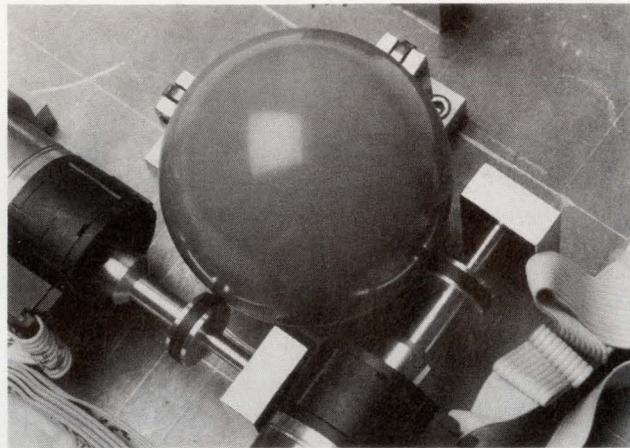
that regular eye-hand reaction time is an average 175 ms. With the force-feedback trackball it's about 30% less.

Just when the resistive force is generated depends on the application and on the screen display. For example, the trackball may be programmed so that the cursor easily moves within preferred, say, white areas on the screen, but triggers the force feedback when the user tries to move the cursor across darker, or non-preferred, areas.

The team of researchers at the institute (the institute is a joint venture of the Philips Research Laboratories and the Eindhoven University of Technology) have implemented the force-feedback principle in a demonstration system consisting of two optical position sensors and two servo motors (*see the photo*). One sensor-motor combination handles cursor position and tactile feedback along the X axis and the other does the same along the Y axis.

Computer experts and other people have already shown interest in the new device, says Jos van Itegem, a member of the research team. He thinks that if a company started to develop the device now, it could come out with a marketable force-feedback trackball "within little time." The development time would depend on the application.

According to van Itegem, many interactive applications could benefit from the new trackball. Among them are text and graphics editors in the office environment, arm-chair control of TV and CD-I (compact-disc-interac-



tive) systems, and computer-aided design.

The trackball with feedback should particularly suit users working with input devices for long peri-

ods of time, such as air-traffic controllers. The device should also prove its worth in applications where speed and accuracy of operation is important,

such as in looking at medical computer images during surgery.

Having a feedback trackball would also be handy where the user must perform two tasks at the same time—for instance, car drivers who want to operate the radio in the dashboard while keeping their eyes on the road. With the trackball at, say, the center of the steering wheel, the driver could control the ball and thus manipulate the car-radio's tuning system by sensing the resistive forces in the ball. At the same time, the driver could be keeping an eye on surrounding traffic.

JOHN GOSCH

TEST-SYNTHESIS APPROACH FOR ICs INCORPORATES PARTIAL-SCAN TECHNOLOGY

A new test-synthesis approach creates ICs with partial-scan technology, yet it still meets timing and area constraints. The synthesis technology, developed by Synopsys Inc., Mountain View, Calif., includes constraint-based scan selection and sequential automatic test-pattern generation (ATPG).

Partial scan is a test methodology that works by transforming some sequential elements in an IC into scan registers. Scan registers are controllable and observable elements. Partial-scan testing is actually a variation on full-scan testing, where all of the sequential elements are turned into scan registers.

In contrast to traditional partial-scan approaches, the Synopsys method leverages synthesis technology to treat testability as

an additional constraint along with area and timing. Consequently, the software optimizes the circuit in all three directions without compromising design time. Emphasis is placed on maintaining predictable, high-quality fault coverage with minimal design impact.

The partial-scan technology works from a top-down approach: Scan as many sequential elements as possible without impacting area and timing goals, and use sequential ATPG to generate test patterns. This approach typically requires scanning 40 to 60% of the sequential elements, and is attractive because it offers good results without numerous design iterations.

Designers use the software by inputting an IC net list. The software performs structural, timing, and area analyses on the design. Structural analysis

determines sequential scan elements that improve testability by reducing the pattern sequence needed to observe and control internal nodes in the circuit. Timing and area analyses calculates how many elements can be scanned based on their respective constraints.

The partial-scan software then uses these analyses to automatically select the scan registers, yielding optimal fault-coverage results. For example, the partial-scan technology will choose sequential elements that reduce a circuit's sequential depth. Automating the selection of scan registers based on the user's constraints removes the need for designers to become involved in the scan-architecture selection, and minimizes the impact of partial scan on a design.

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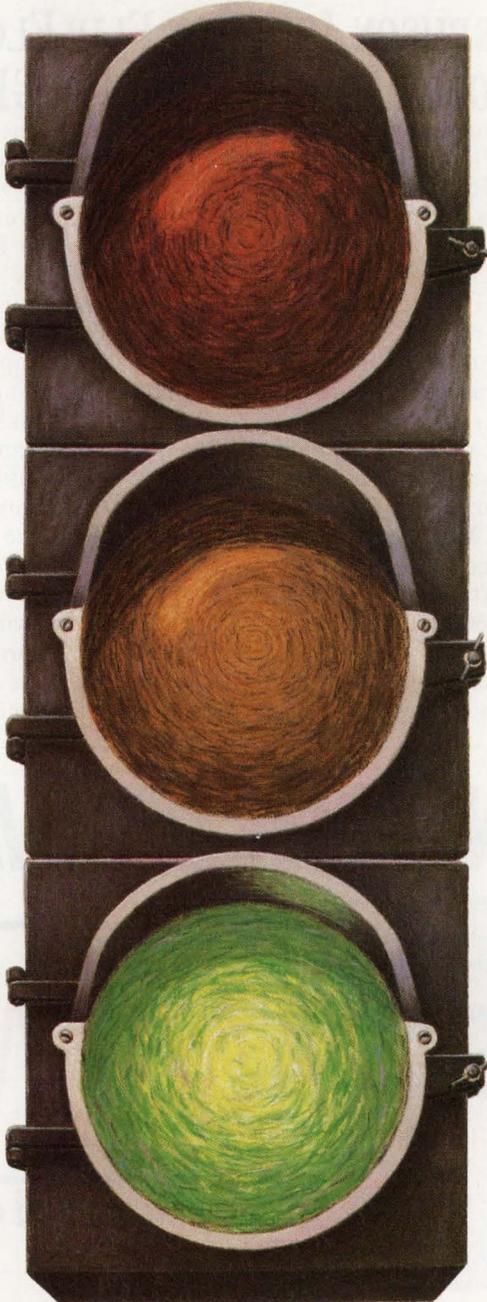
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performed once a partial-scan architecture is selected. Then, sequential ATPG generates patterns to work with the partial-scan architecture, so that the non-scannable elements can be controlled and observed, and faults can be detected in the design. Synopsys' sequential-ATPG technology consists of proprietary algorithms based on such techniques as time-reverse processing and the D algorithm.

Partial-scan technology will be incorporated into a future Synopsys product that's compatible with Test Compiler, Synopsys' existing test-synthesis product. For more information, call Synopsys at (415) 962-5000.

LISA MALINIAK

JOSEPHSON-JUNCTION FLIP-FLOP TOGGLES AT A RECORD 144 GHz

A recently developed flip-flop, based on Josephson-junction technology, toggles at a record-breaking speed of 144 GHz. The device, demonstrated by Hypres Inc., Elmsford, N.Y., works at a temperature of 4.2K, the temperature of liquid helium.

Built on a 3.5- μ m niobium process, the flip-flop is a power miser, using just 1.6 μ W. Moreover, it's been cascaded to build 4- and 32-bit shift registers operating at 60 and 45 GHz, respectively.

The complete 32-bit register doesn't require much

power either. It needs a mere 100 μ W of power (see the photo next page).

These results were obtained using the RSFQ (Rapid Single-Flux Quantum) superconducting logic family. The concept of RSFQ was developed at Russia's Moscow University by Konstantin Likharev, V.K. Semenov, Sergei Rylov, and Oleg Mukhanov (Likharev and Semenov are currently at the State University of New York at Stony Brook; Rylov and Mukhanov now work at Hypres Inc.). It represents logic ones and zeros as the presence or absence of a

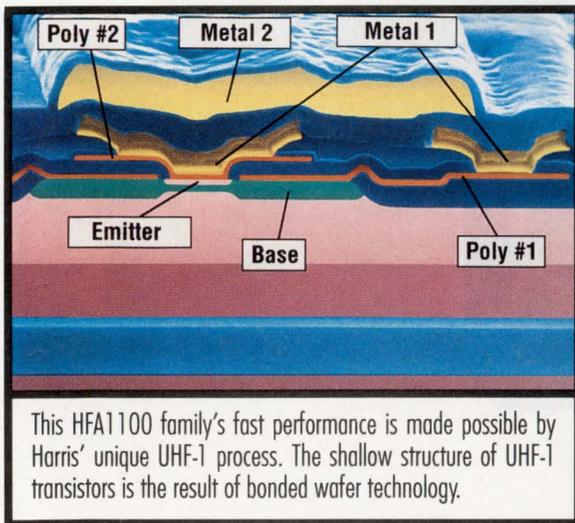
quantized magnetic fluxon.

The fluxon takes the form of a voltage pulse with an amplitude of 1 mV and a width of 2 ns. Nonlatching Josephson junctions generate, transmit, and logically combine these ultra-short pulses. The nonlatching junctions are 30 times faster and require 1/10 the power of the previously used latching designs.

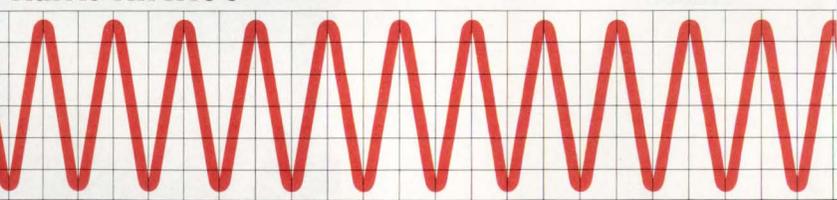
The technology also combines the advantages of low power dissipation with natural self-timing as well as insensitivity to power-supply voltage changes.

The nonlatching junctions have been successfully fabricated using newer

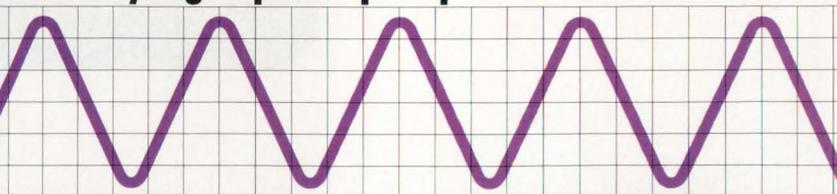
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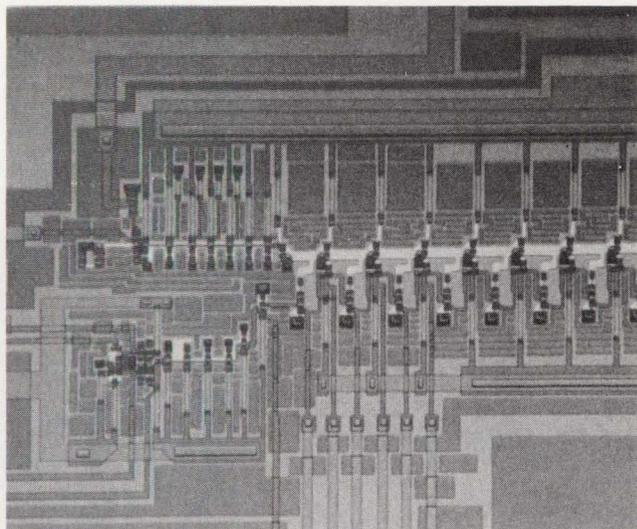
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high-temperature superconducting (HTS) materials, allowing designers to build RFSQ logic circuits that can operate at the temperature of liquid nitro-

gen.

The toggle flip-flop or prescaler circuit—the fastest RFSQ cell—represents the key component for most of the family's logic-

gate designs. As a result, the operating frequency of the toggle flip-flop circuit is critical for projecting the performance of arbitrary RFSQ-based circuits.

Because it's said to be simple to test and is easily expandable to high gate-density levels, the shift register is being offered as an ideal circuit to "prove the technology." There are many applications for the circuit. These include transient digitizers, low-power satellite correlation receivers, and digital-signal processors.

The extremely fast switching speeds of the RFSQ cells and their short aperture times suit them well in analog-to-digital converters. Here, the short

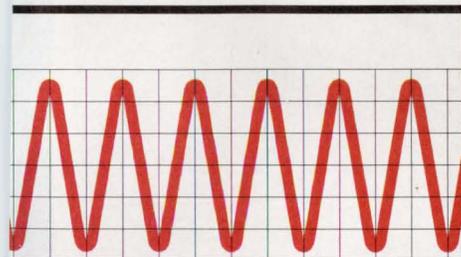
aperture time can be traded off for an ADC design with either a higher accuracy or a larger signal frequency band.

Two types of RFSQ Josephson-junction ADCs have been developed over the last decade: parallel-input and serial-input types. Though the parallel-input RFSQ Josephson-junction ADCs deliver the highest-frequency performance, they do require a simultaneous delivery of ultrafast input sampling waveforms.

For additional information about these RFSQ Josephson-junction developments, call Edwin Stebbins at Hypres Inc. at (914) 592-1190.

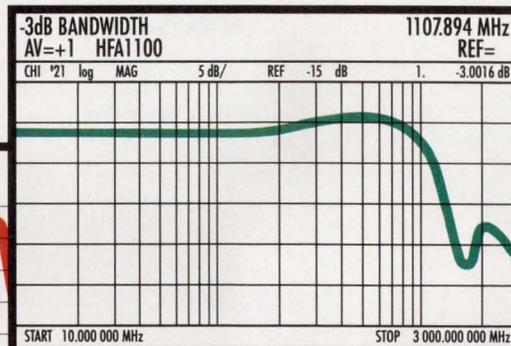
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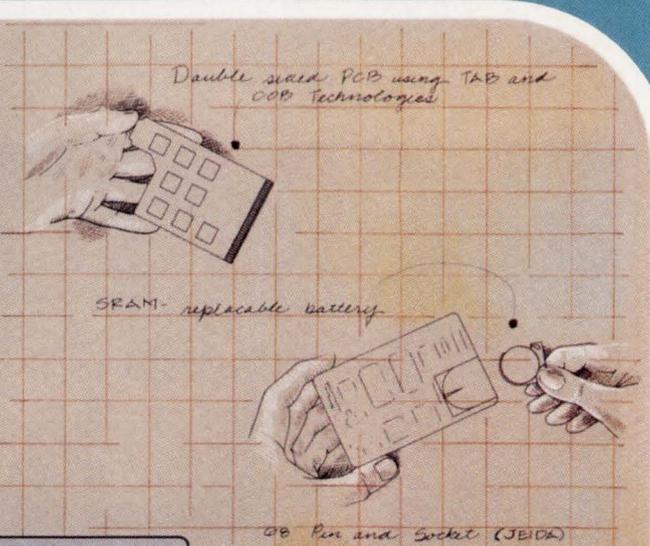
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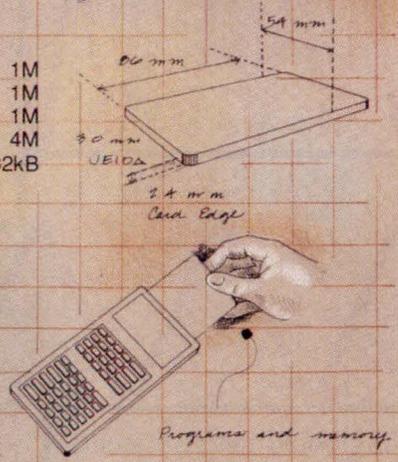
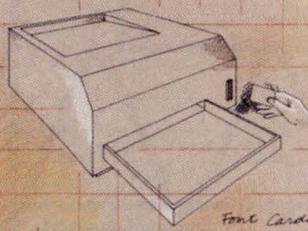
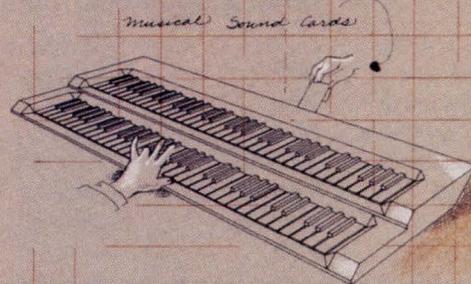
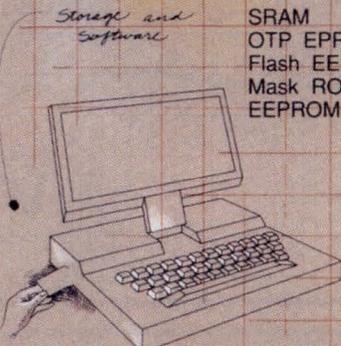
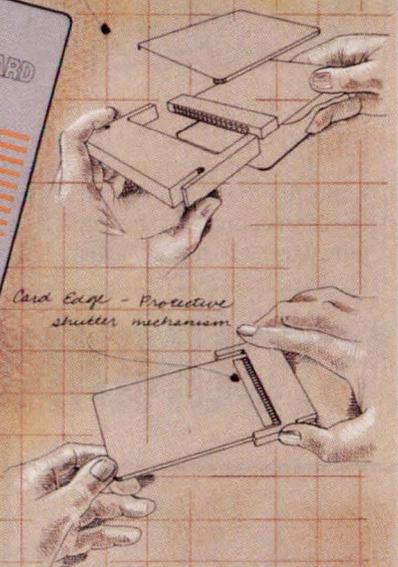


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latest in testing technologies for mixed-signal and analog ICs, as well as data-compaction and boundary-scan testing techniques. In addition, a wealth of advanced communication-IC designs using a variety of CMOS, biCMOS, bipolar, and gallium-arsenide processes highlight the conference's technical program in at least three sessions.

1992 CICC TECHNICAL PROGRAM

Session 1	Session 2	Session 3	Session 4	Session 5
PLDs and gate arrays	High-performance devices and test methodologies	Yield estimation and optimization	Programmable devices and architecture	Design partitioning and formal verification
Session 6	Session 7	Session 8	Session 9	Session 10
Graphics and parallel processors	Embedded memories and ECL circuits	Synthesis techniques for analog and digital circuits	Fabrication technology	Global wireless communications
Session 11	Session 12	Session 13	Session 14	Session 15
Physical design automation	Analog behavioral modeling and simulation	Test I	Broadband communications	Device modeling and interconnect simulation
Session 16	Session 17	Session 18	Session 19	Session 20
Data conversion	Test II	Reliability	Digital filtering and processing applications	"Engineering skills for the year 2000: What are they?"
Session 21	Session 22	Session 23	Session 24	Session 25
"Multichip modules—dream or reality?"	"Intellectual property: How smart is it?"	Interface circuits, sensors and packaging technology	Analog stuff	High-performance-circuit design techniques
Session 26	Session 27	Session 28	Session 29	Session 30
Video and speech processing	Gate-array architectures	Performance-driven layout-design automation	Communications circuits	Computation-intensive processors

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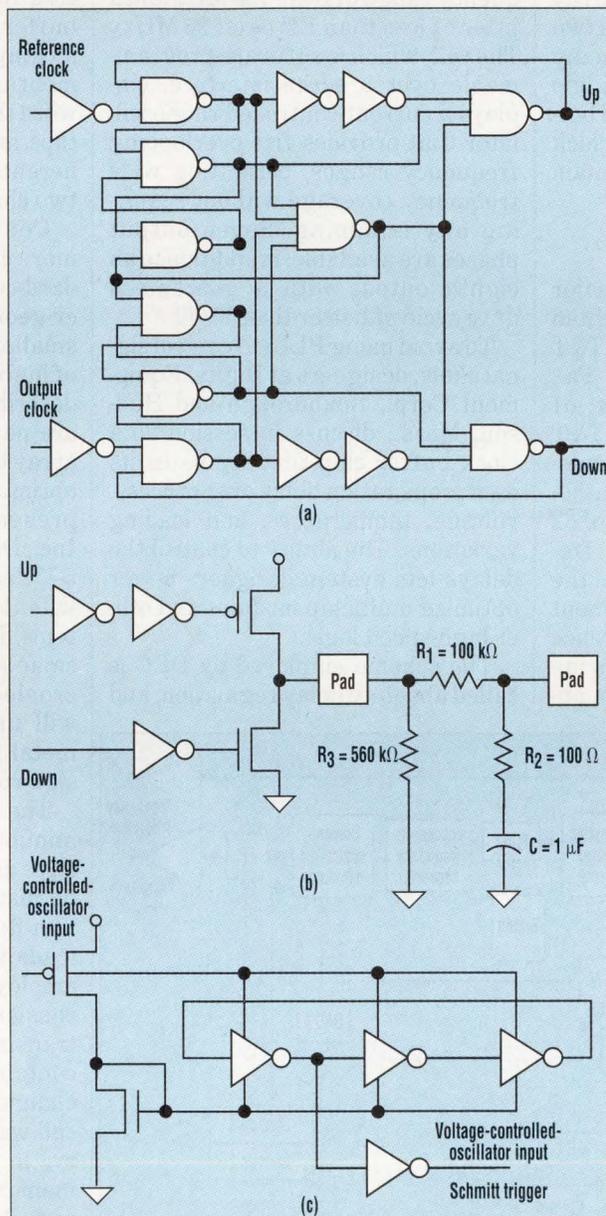
Fast and dense digital chips extend the performance curve at the CICC

Reaching new highs in density, CMOS and biCMOS chips open new opportunities. **BY DAVE BURSKY**

Taking center stage at next week's CICC are a number of new techniques for phase locking, advanced biCMOS logic, and on-chip parallelism that will push CMOS operating frequencies to several-hundred megahertz. Most of the digital technology papers fall into two categories: developments related to gate-array and standard-cell structures and macrocells, and discussions of advanced processors like math chips, digital-signal processors, Prolog execution engines, and so on. Of course, many other papers are on tap, covering such topics as mixed-signal and analog circuits, design software, circuit modeling, and testing.

To accelerate circuits, designers are applying synchronous circuit schemes that require minimal clock skew either from chip-to-chip or across one chip. Minimizing skew in turn requires better clocking and clock-distribution techniques. One example of this is a 240-MHz, phase-locked-loop macrocell developed by the Integrated Circuits Div. of Siemens Corp., Santa Clara, Calif. (described in session 25). The SCxD4 family device can be placed anywhere in the array core of a sea-of-gates (SOG) family of 1- μm gate arrays. This gives users much more design flexibility than with previous approaches that embed one or two PLLs in either the periphery or at strategic locations in the array core.

The PLL can be used for clock-tree skew manage-



1. A DIGITAL phase-locked-loop macrocell, on Siemens' family of gate arrays, performs the phase detection between reference and output clocks with a relatively simple circuit of NAND gates and some inverters (a). Phase-detector up and down outputs feed the charge pump and low-pass filter (b). The low-pass filter's output controls the PLL's VCO, made up of a ring of inverters with a Schmitt-trigger-based output tap (c).

ment, the synthesis of multiple frequencies from one reference, and other applications that require stable frequency inputs. It consists of three major sections: a phase detector on the input stage, a charge-pump and low-pass filter in the middle, and a voltage-controlled oscillator that delivers the output (Fig. 1). Just 60 gates are required to implement each PLL. However, the two resistors and a capacitor needed for each low-pass filter are external components and they must be mounted close to the packaged array.

The VCO, employing a three-stage ring oscillator and a Schmitt trigger, has a frequency range of 5 to 240 MHz with a duty cycle of about 50%. The Schmitt trigger in the VCO's output buffer helps to even up the duty cycle. For lower-frequency operation, the VCO can be slowed by inserting additional inverter stages in the ring. PLL jitter for the worst-case situation—the system clock is driven by an external, non-synchronous source—is less than 3 ns pk-pk when the VCO runs at 50 MHz, and drops to about 2 ns pk-pk at around 190 MHz.

Mitsubishi Electric Corp., Itami, Japan, is also banking on PLLs for high-speed clock distribution in its SOG array family detailed in session 27. The company was able to keep clock skew to less than 400 ps on a family of 0.6- μm CMOS SOG arrays. Unlike the Siemens approach, Mits-

bishi designers dedicated two analog PLLs in the silicon so that automatic layout tools can take care of the clock distribution while achieving up to 156-MHz operation. The lock-in range of the PLLs ranges from about 13.8 to 172 MHz when the chip is powered by a 3.3-V supply.

A clock-distribution network for each of the two PLLs on the array chips consists of five vertical and two horizontal main trunks and many smaller branch lines. Two main line drivers are placed on the top and bottom of the array and send the clock signals to all flip-flops via the main trunks and the branch lines.

SYNTHESIZE THE CLOCKS

Clock synthesis, another major use of PLL techniques, is spotlighted in two session 24 papers from AT&T Bell Laboratories, Allentown, Pa., and the Microelectronics Div. of NCR Corp., Ft. Collins, Colo. AT&T employs a low-jitter PLL to implement a 5-to-180-MHz clock-synthesizer chip that can generate any of 32 software-programmable clock frequencies. All PLL circuitry is on the chip. The only external component needed is a crystal for the reference clock (Fig. 2). The synthesizer is initially targeted at video-graphics ap-

plications for PCs and workstations, and can be used to replace the multiple crystal oscillators now used. The circuit, with an area of just 8.9 mm², can also be used as a macrocell in more complex circuits, such as an all-in VGA controller.

NCR's synthesizer, a standard-cell building block, has an output frequency range of 30 to 128 MHz and a jitter of less than 125 ps (at 96 MHz). The cell, which is software-programmable over a serial interface, employs a current-controlled ring oscillator that provides five overlapping frequency ranges, permitting wide frequency coverage without requiring any trimming. Seven output phases are available, in addition to an eighth output with a guaranteed duty cycle of better than 60/40.

To avoid using PLLs to control signal skew, designers at Digital Equipment Corp., Boxborough and Hudson, Mass., discuss in session 25 a clock buffer chip that regulates its own propagation delay over process, voltage, temperature, and loading variations. The ability to control the delays lets system designers better optimize multichip modules and other high-speed logic.

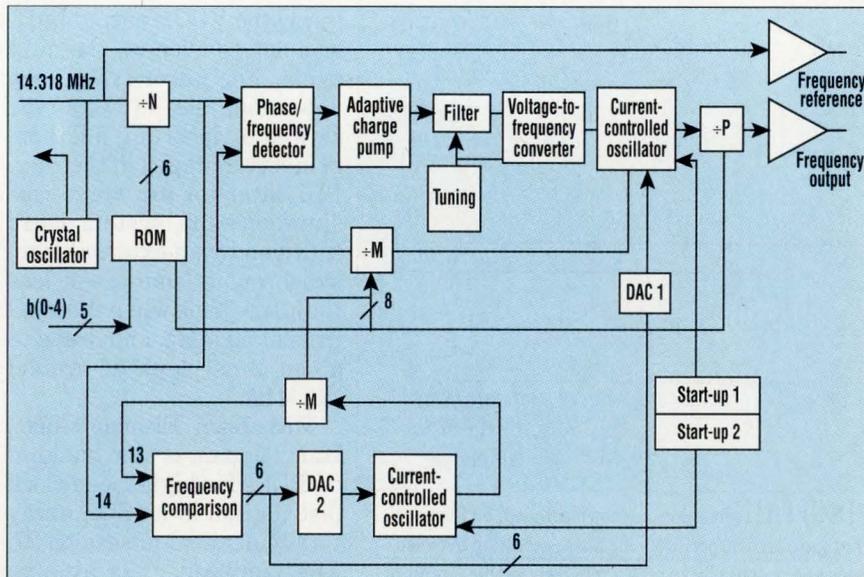
The scheme employed by DEC is called absolute delay regulation, and

consists of a circuit comprising a 144-bit data path, a state-machine controller, and a replica loop. The regulator operates synchronously to one phase, but can regulate two clock phases. Periodically, the chip generates and drives a precise measurement pulse through the on-chip replica loop, which contains a representative input receiver, output clock buffer, and overhead logic. By using a delay line and latch, the measurement pulse is captured as a parallel word that expresses how many delay taps must be added to the chip's inherent propagation delay to insert two clock periods of latency.

Controlling skew has become more critical as gate-array and standard-cell-based circuits employ finer-geometry devices to achieve ever-smaller gate arrays. The latest crop of high-performance arrays and cells described at this year's conference are no exception. A full CMOS test array that packs 154,000 gates and is optimized for 3-V operation will be presented by Texas Instruments Inc., Dallas, in session 27. A standard 5-V design offering a denser layout will also be detailed by SMOS Systems Inc., San Jose, Calif., in the same session. And SGS-Thomson Microelectronics, Carrollton, Texas, will unveil a family of triple-level metal CMOS arrays with 0.7- μ m design rules in session 9.

The TI array employs 0.65- μ m minimum features. The basic gates have an average power consumption of just 1 μ W/gate/MHz. Propagation delay for an inverter with two loads is just 325 ps. The test array employs a novel base-cell design that consists of four large and four small transistors, with each group of four containing two n-channel and two p-channel transistors. The base gate cell was optimized for use as memory, improving the performance of memory cells implemented in the array. Read access times of a single-port static RAM created with a compiler are comparable to those of an all-level custom SRAM described at last year's conference.

Squeezed onto a chip measuring just 11.7 mm on a side, the 154,000 gates are interconnected with three



2. THIS SYNTHESIZER developed by AT&T Microelectronics delivers clock signals as high as 180 MHz and includes all of the components needed to generate the clock signals, except for the crystal used for the reference signal. The programmable counters (blocks marked ÷N or ÷M) allow the circuit to supply any of 32 frequencies.

levels of metal for a gate utilization of up to 87%. Peripheral buffers are tightly spaced—they have a pitch of only 102 μm —so that tape-automated bonding can deliver the densest packaging. The tight spacing permits about 25% more I/O pads than if standard wire bonding was used.

BACK TO BASICS

TI also provides details on a new base cell for a high-density gate array in session 27. The cell includes both high- and low-channel conductivity transistors, yet imposes no area or wireability penalty (*Fig. 3a*). By tapping the same gate contact but selecting different source and drain points, the same region yields both high- and low-conductivity transistors. When the transistors are interconnected, three configurations are possible, with each best suiting a particular circuit application (*Fig. 3b*). The type 1 scheme is best for high-speed logic, while type 2 provides a low-conductance gate that does well in single-port SRAMs. Type 3 seems to be tailored for multiport SRAMs.

The SMOS presentation in session 27 also involves a new base cell. The company claims the cell permits chip utilizations of over 90% for designs employing more than 10,000 gates. The new structure starts with four transistors in the basic cell and interleaves the three legs of the two gate electrodes from each pair. That permits any source, drain, or gate to be connected to any other source, drain, or gate using only straight-line metal interconnections. Furthermore, neighboring basic cells can be connected on the top or bottom by just using an extension of the same single straight metal lines (*ELECTRONIC DESIGN, Feb. 20, p. 30*).

SGS-Thomson will describe in session 9 a 0.7- μm twin-well CMOS process that incorporates aluminum plugs in the contact holes between metal layers, and titanium/tin contact barrier layers to prevent aluminum spiking in the contact regions. The large, 220,000- mil^2 chip can be manufactured with yields of greater than 30% thanks to planar surfaces underneath the metal layers and an

aluminum-plug process.

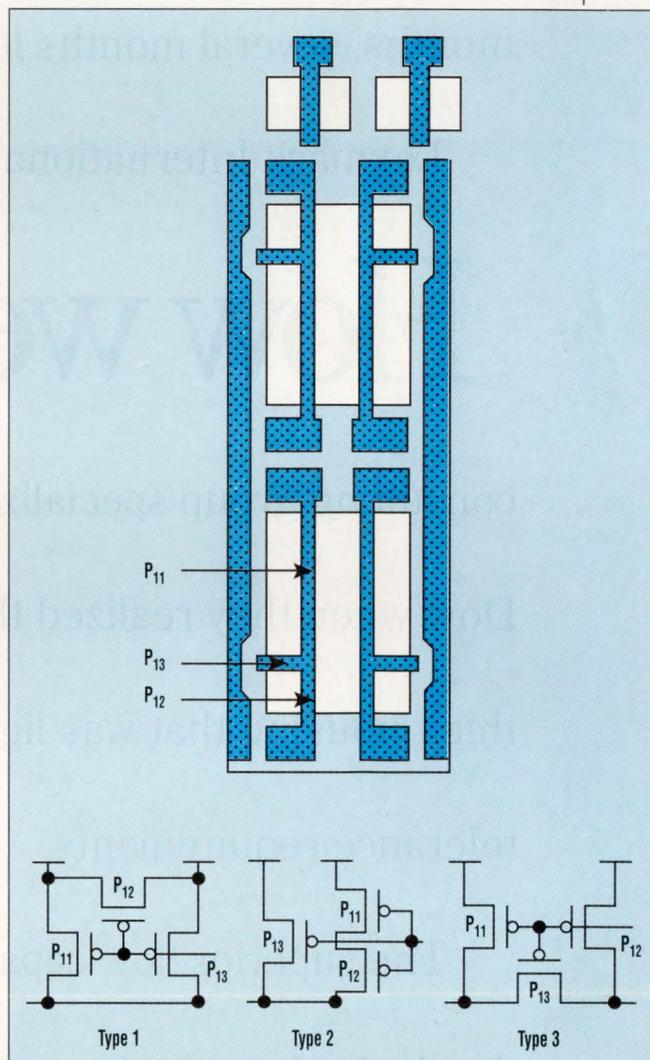
Focusing its attention on biCMOS for shorter propagation delays and very-high-performance gate arrays, the General Technology Div. of IBM Corp., Essex Junction, Vt., in cooperation with the Application Systems Div., Rochester, Minn., created a 220,000-gate chip that employs four levels of metal. Described in session 27, the chip is based on 0.8- μm minimum features. The biCMOS array has 180-ps propagation delays for a two-input NAND gate with 2 mm of wire driving a load of two, which is about half the delay of the gates in the all-CMOS array detailed by TI in the same session.

The IBM approach, however, allows biCMOS, biNMOS, and CMOS circuits to coexist on the same chip with either gate-array or standard-cell design approaches. The biCMOS process starts with the CMOS process employed by IBM for its 300K logic family of CMOS devices, then adds process steps to form the sub-collector, base, and emitter regions.

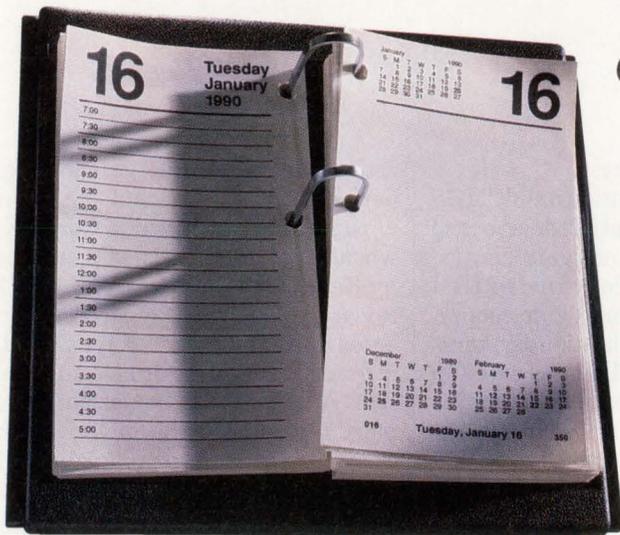
To prevent dc current in cascaded circuits, biCMOS and biNMOS circuits contain full-swing CMOS output-voltage levels. However, some multistage circuits can employ a biNMOS internal stage and a large CMOS buffer as an output stage. To allow the different circuits to work together and still maintain accurate chip timing, IBM developed a timing scheme that converts the different waveforms into an area-based equivalent "standard" waveform, with all timing rules based on the standard waveform.

BiCMOS standard-cell activities are also in-

creasing as companies gain more experience with the technology. Several papers, one by Toshiba Corp., Kawasaki, Japan, in session 2; another by Bell Northern Research Ltd., Ottawa, Canada, and Bayview Technologies Inc., Constance Bay, Canada, in session 7; and a third by Motorola Inc., Austin, Texas, in session 9, explore high-density biCMOS circuits. Toshiba's 0.5- μm standard-cell library is based on a three-level metal process that permits up to 300 k gates and 1 Mbit of SRAM to be integrated on one chip. That chip can have as



3. BY CREATING three transistors that employ a common-gate electrode (top), designers at Texas Instruments can interconnect the devices in several ways to form logic building blocks types 1, 2, and 3 (bottom). The building blocks are optimized for use as general logic, static memories, and multiport memories, respectively.



START

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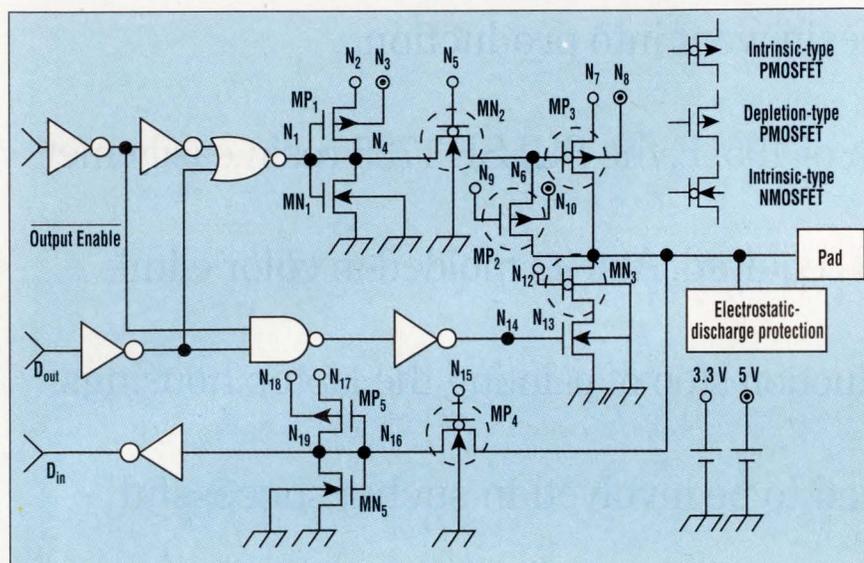
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FINISH

CIRCLE 208 FOR U.S. RESPONSE

CIRCLE 209 FOR RESPONSE OUTSIDE THE U.S.



4. WITHOUT RESORTING TO THICK OXIDES, this I/O buffer circuit developed on a 3.3-V process can handle standard TTL and 5-V levels. To enhance the circuit's ability to handle the 5-V levels, several new transistors (dotted circles) were added to the I/O buffer circuits to reduce the voltage stress.

many as 820 leads when it is housed in a surface-mounted pin-grid-array package.

Employing similar 0.5- μm features, Motorola has applied its biCMOS technology to a test chip—a version of the 68030 microprocessor. The chip places the biCMOS structures in the speed-critical paths to take advantage of the high-performance npn transistors that offer f_t s of more than 20 GHz. The resulting CPU was able to run at clock speeds 50% higher than the CMOS version and operate with supply voltages as low as 2.5 V.

Working with 0.8- μm features, BNR and Bayview created a family of synchronous self-timed SRAMs that have nominal access and cycle times of 5 ns for 64-kbit blocks of 1, 2, and 4-port SRAMs. With that short access time, designers can build chips operating at system clock speeds as high as 200 MHz. The technology also allows the companies to implement dynamic RAMs that use four-transistor memory cells.

A simpler bipolar-MOS approach that merges lateral pnp bipolar devices with MOS pull-up transistors considerably reduces the number of process steps over a full biCMOS implementation. The combination of a

high-gain lateral pnp transistor and a PMOS pull-up device allows biN-MOS circuit structures to be made in a standard CMOS process, keeping the production cost the same as CMOS. Furthermore, using the pnp device to handle highly-capacitive loads lets the circuit maintain top speeds without any substantial area penalty. For instance, a biN-MOS buffer with a 10-pF load is twice as fast as a CMOS buffer and 1.6 times faster than a biCMOS device, yet it requires just 38% more chip area than a CMOS buffer.

BRIDGING TWO WORLDS

As minimum chip features shrink, many companies reduce the chip operating voltage to 3.3 V or lower to avoid breakdowns due to electric-field stress. However, until all circuits operate at 3.3 V, interfacing 3.3-V and 5-V systems presents a challenge to many designers. To minimize the hassles, Toshiba developed a 3.3/5-V-compatible I/O circuit, which is discussed in session 23. The circuit avoids using thick oxides that typically prevent structural breakdowns caused by high field stress.

In the new circuit, extra transistors (MN3 and MN4) help reduce the V_{GS} and V_{DS} potentials of the other

MOSFETs, thus improving reliability (Fig. 4). Transistor MP4 is inserted to lessen the V_{GS} potential of transistors MP5 and MN5. Furthermore, leakage current that might flow through MP2 when 5-V signals are present is cut off thanks to three threshold-voltage controls and the 3-V gate voltage on MN2.

When lead times of several months are practical, gate arrays and standard-cell-based solutions deliver the functionality and density needed. However, when lead times turn to weeks or days, the latest generation field-programmable gate arrays offer potential solutions to get the first prototype systems ready. In session 1, a pair of presentations by Altera Corp., San Jose, Calif., and Concurrent Logic Inc., Sunnyvale, Calif., show off two of the latest architectures.

The Altera MAX7000 series is based on an EEPROM cell and 0.8- μm minimum feature sizes to achieve minimum input-to-output delays of just 11 ns. The family will offer devices with high pin counts—up to 288 pins—and in-system operating frequencies of up to 70 MHz. The high operating speed stems from a new internal programmable-interconnect array that has a series of AND gates feeding an OR function, instead of having the gates control an EPROM transistor as in the MAX5000 EPLDs (ELECTRONIC DESIGN, Jan. 23, p. 135).

A high-density array employing SRAM-based control cells, developed jointly by Concurrent Logic Inc., Sunnyvale, Calif., and National Semiconductor Corp., Santa Clara, Calif., can implement complex functions, such as 16-bit synchronous loadable counters that run at over 50 MHz. The first version of the array, described in session 1, will pack about 3136 logic cells. Each cell implements 35 different states, which gives the chip a very high degree of flexibility.

Other FPGA architectures unveiled in session 4 include Crosspoint Solutions' 0.8- μm antifuse-based logic arrays. The arrays allow transistor-level programming, enabling designers to employ the same meth-

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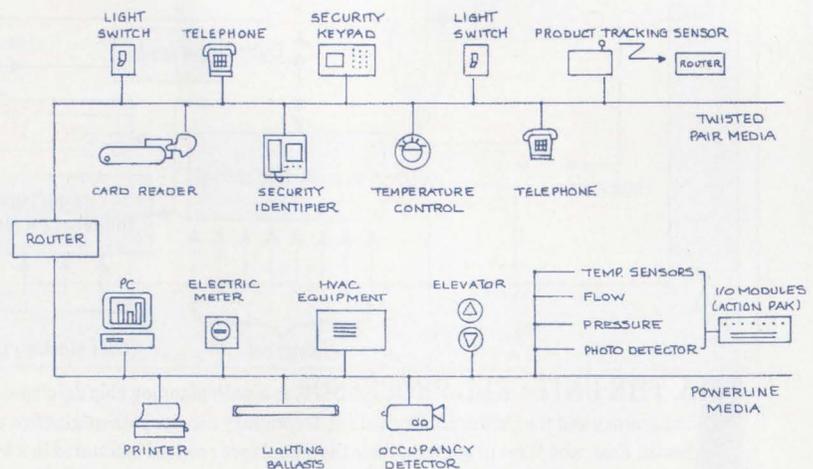
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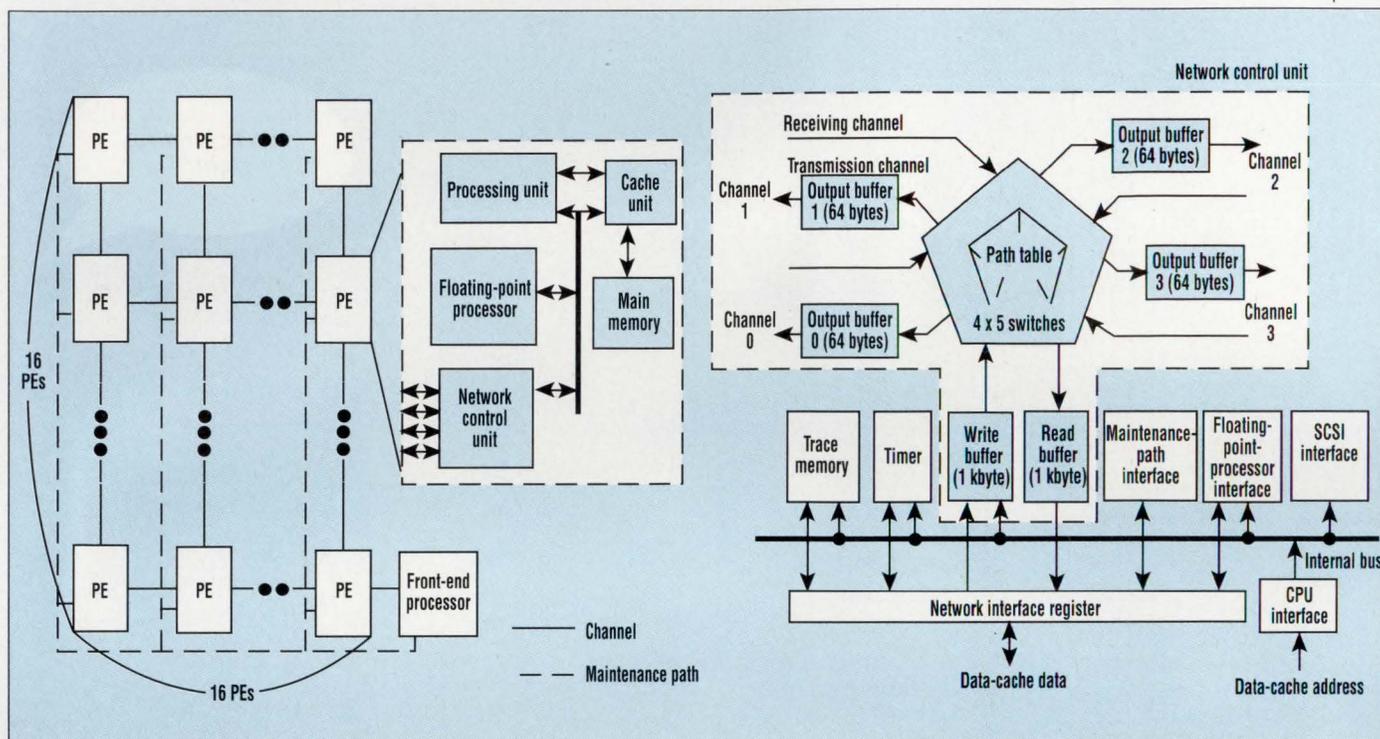
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6. EACH ELEMENT of any array of processing elements (PEs) for a large-scale parallel inference machine contains a CPU, cache controller, floating-point coprocessor, some local main memory, and a network control circuit (left). The network controller chip developed by Mitsubishi Electric has four communication channels that tie into the four nearest-neighbor PEs, and a fifth port that communicates through read and write buffers with the current PE and the rest of the system resources (right).

1 kbyte of data cache, a graphics coprocessor, a video controller, and a bus-interface unit with DRAM/video RAM and I/O control. The graphics coprocessor consists of a bit-block-transfer (bitBLT) processor and dedicated DMA channels, while the video controller chip includes a video FIFO memory and associated DMA logic.

The coprocessor's bitBLT data path consists of a four-deep source-word FIFO buffer, a previous-source register, a skew multiplexer, and a barrel shifter that extracts and aligns pixels on word boundaries. A color expander that expands a monochrome bit map to a 2-, 4-, 8-, 16-, or 32-bit/pixel bit map is also included in the bitBLT subsection. Packing about a half-million transistors, the 14-mm² chip contains most of the functions required for a low-chip-count X-terminal.

A programmable lossless data-compression coprocessor that ties into X-terminal, laptop computers and other systems which utilize data

compression will be detailed in session 1 by Infochip Systems Inc., Santa Clara, Calif. The chip includes a programmable PC/AT bus interface and a DMA controller that can be used in either a standalone mode or cascaded to one of the channels in a higher-level DMA controller. The circuit is dynamically configurable under program control and can compress and decompress data at rates of 2 Mbytes/s and 4 Mbytes/s, respectively.

WORKING IN PARALLEL

In computationally intensive processors, high degrees of parallelism are key in attaining maximum throughput. Just such an approach will be detailed in session 6 by the Jet Propulsion Laboratory in conjunction with the California Institute of Technology, both in Pasadena, Calif. On one chip, the companies integrated an array of 24 by 25 processor cells. Each processor contains a pair of 4-bit latches, an 8-bit counter, several gates, and decoding logic (Fig.

5). This chip, intended for path planning in battlefield situations, can aid in time-critical problems. For instance, during battlefield action in wartime, it can compute the shortest path to traverse a given terrain—a key factor when quick response is needed during enemy fire.

Loading the chip requires just under 0.3 ms (for a 600-pixel map). However, that time can probably be considerably improved if a submicron multilevel metal CMOS process is used for the chip, rather than the moderate-performance 2- μ m single-metal process. The chip takes just milliseconds (for arrays up to 512 by 512 points) to compute the fastest path between any points on the terrain that's mapped into the chip. In comparison, to get the same information from a software-based computation would typically require three orders of magnitude more time. As a result, improved computational efficiency is useful in battlefield situations, as well as in such applications as autonomous-vehicle

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navigation, evacuation and rescue planning, and police and transportation dispatching.

A multichip parallel execution approach applied by Mitsubishi led to the development of a large-scale parallel inference machine that can perform a maximum of 128 million reductions/s—15 times the throughput of the company's previous implementation. Described in session 30 is the parallel core of the system, which contains a maximum of 256 processor elements (PEs) set up in a simple X-Y grid. To support the parallel array of PE blocks, designers at Mitsubishi created a network control chip to coordinate array activities, a master-processing unit (CPU, address generators, etc.), a floating-point processor, and a cache-memory support circuit (Fig. 6, left). Each of those chips is replicated in every PE, and each PE also contains some local main memory.

The network chip, which handles the chip-to-chip and system-to-host communications control, has five pairs of channels: four are used for the adjacent PE cells while the fifth ties into the PE's own processor chip (Fig. 6, right). The channels that tie into the buses have 1024-by-9-bit read-buffer memories and similar-sized write-buffer memories. Each of the four transmission channels packs a 64-word-by-10-bit FIFO buffer that minimizes the chance of network choking. All of the processor

units are interconnected through a 5-by-4 switch circuit, and each receiving channel has its own path table that's used to determine the channel to transmit the packet.

A late-news paper in the same session may harbor the ultimate in parallel processing—a computational RAM. Developed at the University of Toronto, Canada, the memory chip includes single-instruction-path, multiple-data-path (SIMD) processors embedded in the memory's sense amplifiers. Consequently, the memory chip is a hybrid of a RAM and an SIMD computer. Each processor element is only 1 bit wide and arithmetic is performed in a bit-serial sequence.

The ALU performs an arbitrary function on three inputs (the memory and two registers). That ALU is actually implemented as a multiplexer with the data input coming from off-chip. Therefore, the tight-pitch layout is compatible with the memory cell grid on the chip. The registers also double as shift registers, providing communication between adjacent processor elements.

A proof-of-concept 8-kbit computational RAM was fabricated by the University of Toronto, with their ultimate goal being to implement the concept in a commercial, 4-Mbit DRAM architecture. Although the DRAM is slower than the SRAM prototype, a 32-Mbyte array could perform 13 billion 32-bit additions/s, or

10 billion multiply-accumulates/s (8-bit multiplication by a constant, 16-bit accumulation). One major application proposed by the university involves applying the concept to video-signal processing to execute discrete-cosine transforms right in the memory (an 8-by-8 transform for 1 million pixels would require just 3.9 ms to be done).

Developed as a possible coprocessor for a workstation, the Proxima Prolog execution engine that SGS-Thomson Microelectronics, Agrate, Italy, and the Politecnico di Torino, Torino, Italy, built employs parallel operation to speed the execution of Warren code. As described in session 30, the processor consists of two chips that implement the Warren abstract machine to execute Prolog programs at a rate of 500,000 logical inferences/s when clocked at a frequency of 20 MHz.

By employing a Harvard architecture with fully independent ports for code and data, the Prolog engine will minimize the memory-access bottleneck that the execution of logical inferences imposes: One inference requires 40 accesses to data memory and 16 to code memory. One of the two chips implements the instruction processor while the second chip contains the data-processing unit—a microprogrammed engine built around a 32-bit tagged data path that efficiently handles the Prolog data types and primitives. □

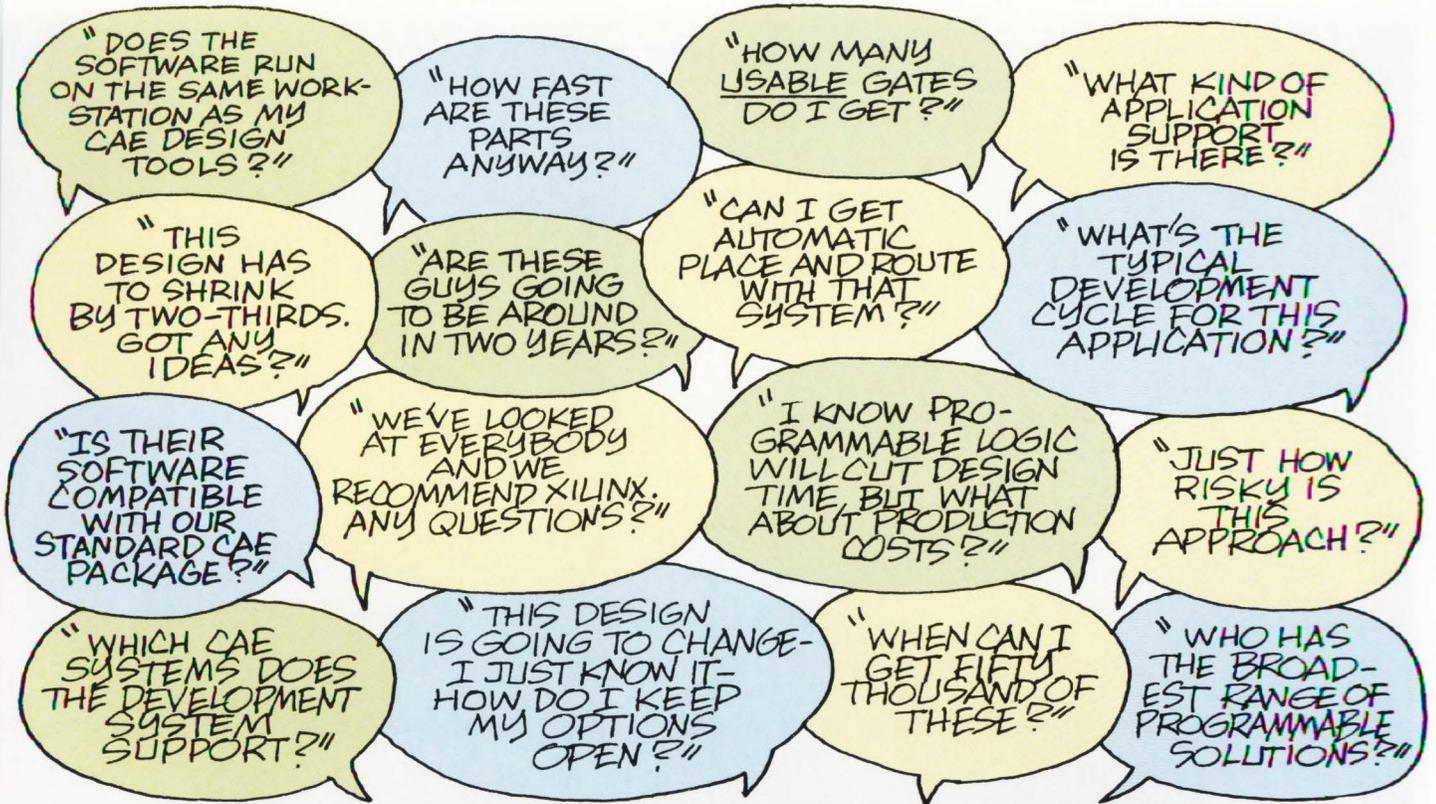
CMOS now dominates analog, mixed-signal IC designs

ICs run the gamut from systems on a chip that manage utility power and complete hearing aids to 1.2-GHz PLLs. **BY FRANK GOODENOUGH**

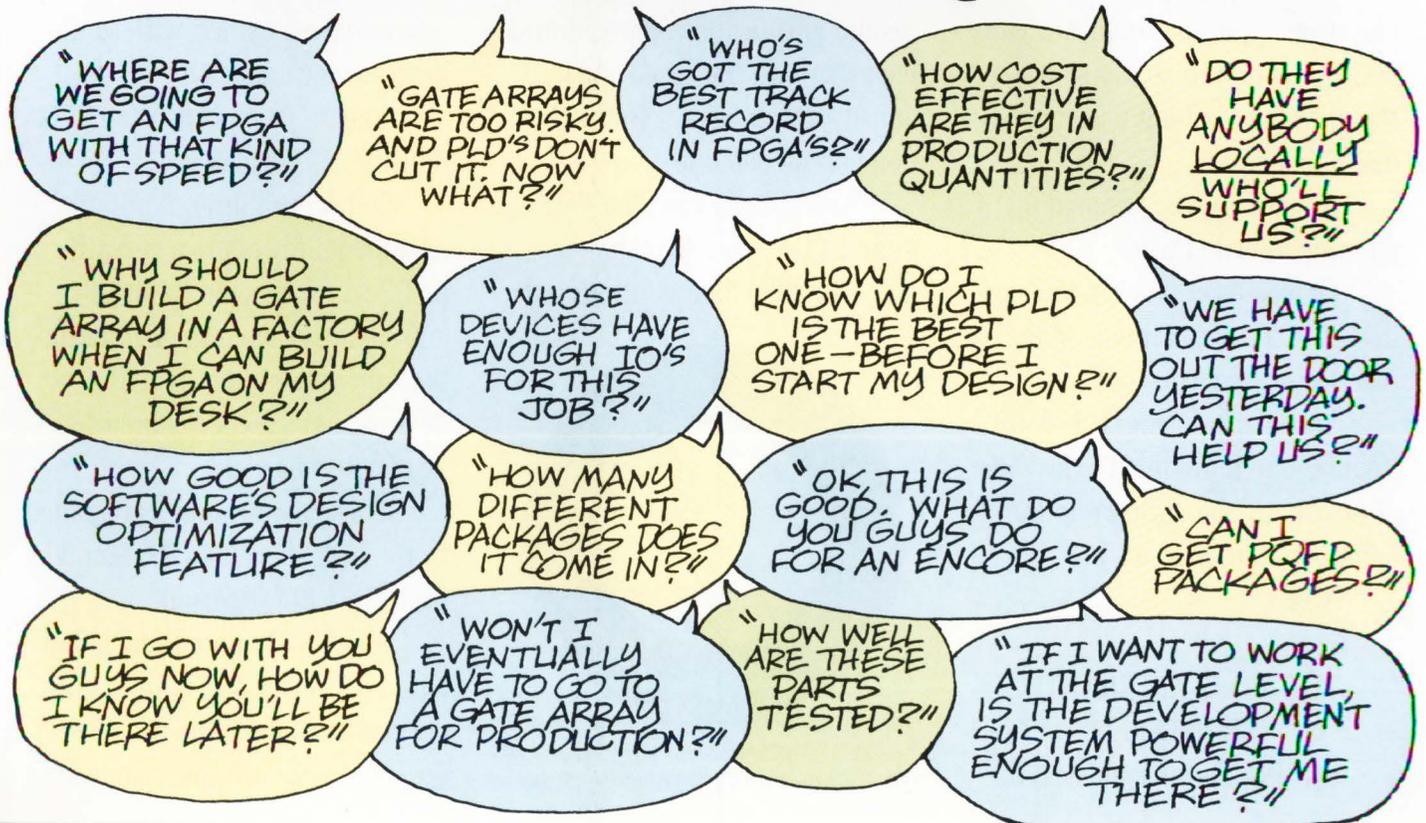
Bipolar mixed-signal ICs at this year's CICC were, with few exceptions, conspicuous by their absence. Even biCMOS devices were few and far between. In fact, most IC designs described at CICC were made on "standard" digital CMOS processes,

a trend that's quite distinct from the action in standard-product analog and mixed-signal developments. Moreover, it's quite different from what many companies say is their present, or will be their future, technology of choice for analog and

mixed-signal semicustom and custom ICs—namely complementary bipolar biCMOS processes (ELECTRONIC DESIGN, Jan. 9, p. 59). One clear trend is the move to current-mode circuit techniques to increase the speed-power product of analog ICs.



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WITHOUT ASKING A FEW QUESTIONS.**





On that great highway of electronic system design, are you still trying to lumber along in the slow lane behind a load of discrete logic?

Are you maybe jammed up by a bunch of little PLDs?

Or worse yet, stuck in the parking lot of the gate array foundry, wondering how you got there?

Well, just consider this your invitation to move into the fast lane of programmable logic. From the company that owns it.

Xilinx.

THE MOST ALTERNATE ROUTES.

Our FPGAs offer the best of

both worlds: the flexibility and instant gratification of programmable logic, with the speed and density of gate arrays. But with none of the penalties.

And nobody can offer you more FPGAs than we can.

Our 2000 family, introduced



By rolling out constant improvements in speed and density, Xilinx can give your designs more mileage.

in 1985, has been cruising down the cost curve ever since, with some devices now under \$10.

The 3000 family boosted FPGA density to 9,000 gates.

Today, our third generation XC4000 family offers a versatile architecture, on-chip RAM, fully automatic design implementation, built-in system functions, and devices that'll someday break the 20,000 gate barrier.

These powerhouses are joined by the high speed XC7200 family from our EPLD division.

Along with more than 250 different packaging and temperature options to support the broadest possible range of applications.



NOW THAT YOU CAN GO THIS FAST, HOW FAR WOULD YOU LIKE TO GO?

Speed in MHz	1992			1993		
	3000	4000	7200	3000	4000	7200
16 bit Counter	95	105	40	115	125	50
16 bit L/U/D Counter	25	30	40	30	36	50
24 bit Accumulator	16	31	17	20	29	20
24 bit Adder	16	31	17	20	29	20
16 ch, 32 bit DMA	na	20	na	na	25	na

Feel the need for speed? We're just getting revved up.

THERE IS NO SPEED LIMIT.

Today, with system speeds up to 50 MHz, and densities up to 10,000 gates, there are very few limits to what you can do with Xilinx programmable logic.

A variety of improvements help us deliver this performance boost: integrated system features

on chip, for instance, and a sub-micron manufacturing process are just two.

How much faster can you get? Just hang on and see.

GO A LOT FARTHER, FOR A LOT LESS, WITH XILINX.

High volume production does wonders for the price of our devices.

Considering we ship ten times more FPGAs than all our competition combined, it's no shock that we're the lowest cost FPGA producer. And those prices are only going to get better.

We also save you money by offering the broadest workstation platform support, and the broadest CAE system compatibility. So you can go with us without having



Besides pushing speed, density and costs, we're also driving advancements in packaging, including the first programmable logic in QFPs.

to reinvent, or reinvest in, a new set of wheels.

It's all part of a company-wide plan to make Xilinx your programmable logic company. And put you in the driver's seat.



Design and production schedules have never been tighter. Systems have never been more complex. You need more options for creativity, and more forgiveness in the design cycle, without paying the usual time or cost penalties.

Time has become so compressed, hardware and software are being engineered concurrently. Often, there isn't even time for a prototype. What do you do? Just keep reading.

LOGIC FOR THE 90'S. AND BEYOND.

The programmable logic solutions from Xilinx were made for the way you have to design logic today. And down the road.

For starters, there's no NRE. Your costs going in are low, and they

are going to get lower every day.

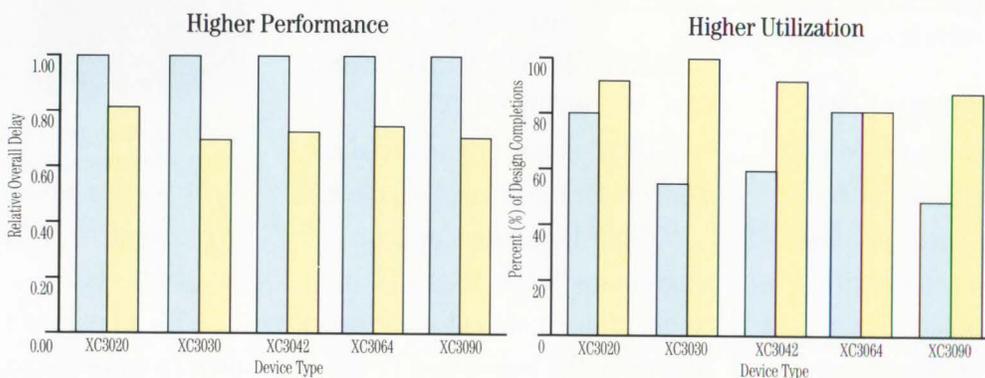
Our devices are infinitely reprogrammable, even in the system, so you can refine your design until it hums.

Later on, adding new capabilities is just as easy.

And with our short develop-

ment cycle (at least 15 weeks shorter than a gate array), you're not waiting for production quantities.

You can get them as fast as you like.



We tested our new ADI place-and-route software, v.3.2, on 153 of our customers' toughest designs. These benchmarks document the improvements you can look forward to, automatically, with Xilinx.

WHICH WAY IS THE BEST WAY TO GET THERE?

Don't worry about your inventory, either. Our devices are standard parts, fully tested (so you don't have to write test vector number one), and they'll keep until you're ready.

And our pin-compatible Hardware Gate Array makes migrating to high volumes automatic—no test vectors, no waiting, no pain.

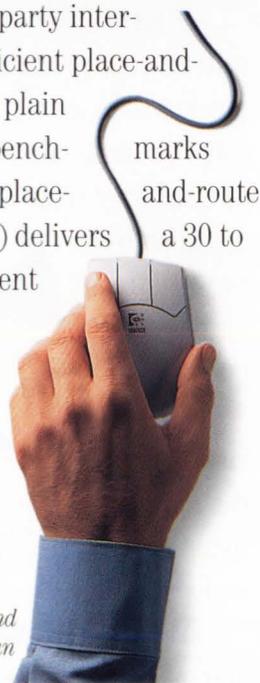
XILINX, THE SOFTWARE COMPANY.

Our XACT development system never stops getting better.

It's push-button-automatic, sure, but it's also powerful, so you can go as deep into your design as you care to.

We've also added more libraries, ABEL support, more user control, user-defined hard macros, more new 3rd party interfaces, more efficient place-and-route, and just plain more. In fact, benchmarks show our new place-software (v.3.2) delivers a 30 to 40% improvement in device utilization.

Our XACT software is so automatic, the difference between last year's model and this year's model can be just one button.



And a 25% improvement in performance.

All of which make our XACT system easier than ever to live with. But we don't intend to rest on our disks. We're building more intelligence into the system everyday, with powerful new features like deadline timing, a floor planner, and a hot, very smart design manager on the way.

You see, our goal is to build a development system that practically runs itself, and produces perfect designs in record time.

That alone is reason enough to go with us. (The fact we're driving this industry doesn't hurt either.)



The value of timely market entry is no longer incalculable.

Research on the subject shows that a six-month delay in getting to market reduces product profitability by a third over its life cycle.

As if that weren't daunting enough, consider this.

Rapidly evolving technologies reward quick product development, but tend to accelerate product obsolescence. So how do you achieve the first without getting bumped off by the second?

**GET TO MARKET FIRST,
THEN STAY THERE.**

The old saying is, "the view only changes for the lead dog."

Well, when you put your logic on a Xilinx device, here's what the leader's view looks like.

First of all, no one can help you roll out your product quicker than we can. Our hardware and software were designed from the beginning for just that purpose.

Once you're out in the market, then the fun really starts.

You can respond to changing market conditions and customer's

needs almost as soon as you learn about them.

For example, our FPGAs are even reprogrammable in the system, so you can produce new models with different feature sets just by modifying the design—

a task our software makes virtually automatic—and reloading via EPROM, disk, or telephone. And what new models they can be.



Since our PLDs are standard parts we can knock them out in ever higher volumes. So they arrive at your shipping dock fully tested, and dropping in price. Sweet deal.

**OUR IMPROVEMENTS,
YOUR INNOVATIONS.**

We're continually pushing to deliver denser, faster, smaller,

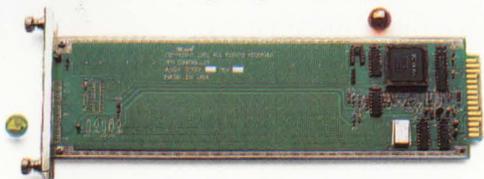
HOW MUCH IS IT WORTH TO GET THERE FIRST?

more highly integrated devices.

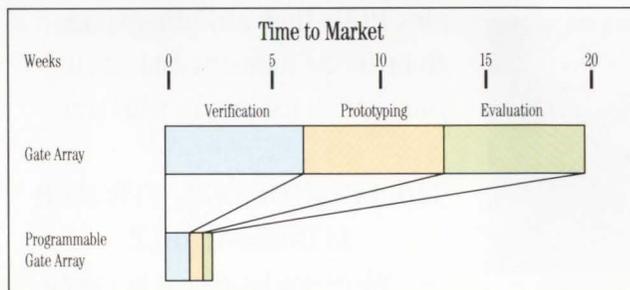
Likewise, our software gives you more and more efficient device utilization, and as a result, better performance.

Together they let you build new systems that are smaller, lighter, faster, more reliable, and yet pack more features than previous models.

And still hold the line on costs. With all that going for you, you



Before Xilinx, this board was crawling with chips. We reduced chip count by 80%, power consumption by 75%, and cut out two board layers. That's what we call a good shrink.



You may not be able to buy time, but you can certainly do the next best thing. You can buy Xilinx and save time. Almost four months worth, compared to using a conventional gate array.

won't just get to market. You'll *be* the market.

**GO WITH
SOMEONE WHO CAN
HELP YOU GET THERE.**

Because no one has a broader product line, you can get the right part, at the right time, build the

right design, and refine it without risk.

What's more, you'll find our prices will continue to drop as our volume continues to increase. Which it does everyday, as more and more

companies discover the benefits of our approach.

An approach that includes the benefits of lower costs, better integration, more speed, and less risk, all from one source.

Xilinx.

There's too much at stake to go any other way.



**AFTER ALL,
YOU'RE NOT JUST
BUYING A
LOGIC DEVICE,
YOU'RE BUYING
A HEAD START.**

When you go with Xilinx, what do you get?

Software so automated it can shrink a development cycle to less than a starting employee's



The most valuable thing in a horse race? A good lead. As the leader in programmable logic, we can help you get one. And keep it.

vacation. The fastest, densest, most cost-efficient devices. And support from the league-leader in programmable logic.

THE MOST EXPERIENCED PROGRAMMABLE LOGIC.

In all modesty, we know more about FPGAs than anybody.

After all, we invented them.

We've also sold more than 13 million devices, and more than 12,000 development systems.

So our staff of FAEs have more experience designing with complex PLDs than any other single group in the industry. And when you go with us, they're with you.

THE LOGIC OF OUR APPROACH IS INESCAPABLE.

We're not burdened by expensive fabs, so we can invest where it really counts: in device improvements.

We have the largest software team in programmable logic—half of our total R&D staff. Our goal is to automate even the toughest

designs, till the process becomes as quick and painless as possible.

We'll also continue to push the industry in device speed and density.

After all, we're in the best position to do that—our R&D budget is bigger than most of our competitor's revenues.

So find out how much we can help. Call our 24-hour information hotline at **800-231-3386** for the latest product literature and the name of the Xilinx representative nearest you. We'll take it from there. But do it soon. Because these days, getting ahead is the only way to go.



The Programmable Logic Company.SM
2100 Logic Drive, San Jose, CA 95124
(408) 559-7778

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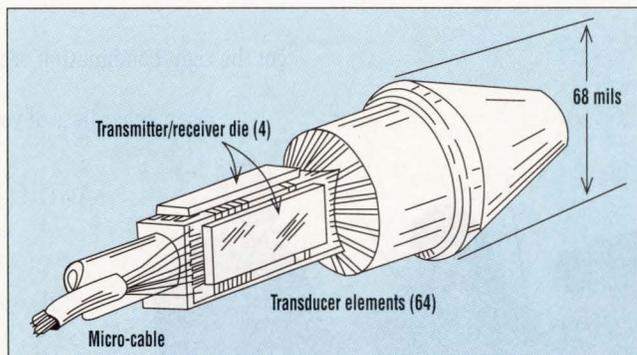
A notable example is a pair of current-mode ICs, which perform sampled-data and continuous-time filtering of 5- and 40-MHz signals.

The most interesting papers at each year's CICC are always those describing complete (or almost complete) analog or mixed-signal "systems on a chip." This year is no exception. One such IC is a four-chip circular assembly designed for insertion in human blood vessels to diagnose clogged arteries. Less than 72 mils in diameter, it contains 64 ultrasound transducers. Other systems on a chip include a single-chip hearing aid that works off 1.1 V; a digital-signal processor with eight on-board delta-sigma analog-to-digital converters designed to monitor and control three-phase power; and an 8-bit, current-mode analog-signal-processing fax subsystem.

Data converters are well represented at the CICC with a total of six CMOS ADCs and a CMOS delta-sigma digital-to-analog converter. The ADCs include a 6-bit 125-MHz flash device, a 50-MHz 10-bit multistep design, and four delta-sigma units. Several of the delta-sigma designs handle signals above 100 kHz. Three CMOS and one biCMOS frequency synthesizer for handling frequencies from 5 MHz to 1.2 GHz are also included in the technical program. On the other hand, analog arrays, which at one time dominated the CICC analog papers, were limited to just one representation: The array is built on a complementary process that provides 5-GHz npn and 3-GHz pnp transistors.

HAVE A HEART

Hope is on the way for those in need of triple bypasses to unclog arteries in the form of an "invasive" ultrasonic artery scanner described by Endosonics, Rancho Cordova, Calif. Described in session 23, the probe, which is in volume manufacture, is a joint development with Northern Design, Golden Valley, Minn. It contains 64 20-MHz piezo-



1. THIS ULTRASONIC transducer array, just 76 mils in diameter, can be inserted in human arteries to check for plaque buildup. Its echoes range off the sides of the blood vessel, providing data for a CRT display of the artery, which can be correlated with a display of the actual condition of the artery.

electric transducers connected to four transmitter-receiver ICs. The tiny probe fits in an artery-invading catheter with an outside diameter of just 72 mils (*Fig. 1*).

The transducers create a narrow, rotating beam of 20-MHz acoustic energy, which is transmitted, perpendicular to the axis of the catheter, to and through any accumulated plaque as well as the artery wall. The echoes returning to the transducers from the plaque and artery wall are amplified and passed down a multiple-conductor, several-meter-long, micro-coaxial cable running through the catheter lumen. At the end of the cable, the amplified signal is sampled, digitized at 400 MHz, and processed, producing a 360° cross-sectional image of the artery, which is applied to a CRT display. A trained observer can differentiate between a normal and a diseased artery.

Each of the four identical, 33-by-64-mil, 3- μ m, CMOS die handles 16 of the transducers. One of them, connected to the cable, acts as a master controller, while the other three act as slaves. The ICs sequentially drive the transducers with 10-V, 20-ns pulses. Each receiver amplifier, which has a current gain on the order of 60 dB, recovers from the transmit pulse to the noise level (<1.5 pA $\sqrt{\text{Hz}}$) in under 300 ns, to handle weak, near-field reflections. The current gains of the 64 amplifiers match within better than 1 dB. Total power dissipation for the four chips is less

than 100 mW.

While hearing aids work well in environments with low background noise, their recipients have trouble understanding speech in a noisy environment. It was found that adaptive high-pass filtering reduces the most disturbing noise, that with a spectral content dominated by low-frequency energy. The adaptive filter reduces background noise automatically by reducing low- and mid-frequency gain as a function of input-signal level. However, modern hearing aids, which are inserted in the ear, must also handle an "insertion loss" in the 2-to-5-kHz range because they negate the gain provided by the "unaided" ear canal.

A design team from the Micro-Rel division of Medtronic Inc., Tempe, Ariz., and Argosy Electronics Inc., Eden Prairie, Minn., describe in session 7 a one-chip hearing aid they created to handle these problems (*Fig. 2*).

The use of a biCMOS process for the chip provides CMOS for logic and switched-capacitor filters and bipolar transistors for low-noise preamplifiers and good output drive. In the chip, a low-noise circuit amplifies the input from the microphone and drives the adaptive filter, which also performs an AGC function limiting maximum signal amplitude to prevent over-driving subsequent stages. This g_m/C continuous-time filter provides a fourth-order, high-pass, Butterworth response with a corner frequency that increases from approximately 200 Hz at low-signal levels to about 2 kHz at high-signal levels.

The output of the adaptive filter drives a second-order 12-kHz, low-pass anti-aliasing filter prior to sampling and processing by the three, fourth-order switched-capacitor filters, which take care of the mid-band insertion loss. External potentiometers "weight" the outputs of these high-pass, band-pass, and low-pass filters. Their corner frequency can be changed by changing the clock frequency, which permits tuning

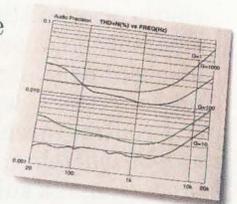
One loud part can ruin the perf

got the right combination of specifications, performance and price, regardless of your design needs.

AUDIO DESIGNERS SHOULD LISTEN TO THIS.

If you're designing audio components and want superb transient response, ambience, clarity and dynamic range, our products will be music to your ears.

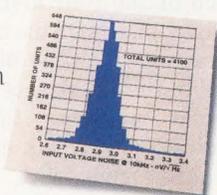
The SSM-2017 microphone preamp has impressive noise performance (950 pV/ $\sqrt{\text{Hz}}$) and ultralow THD (<0.01% @ G = 100), while the new dual OP-275 has



great sonic characteristics, low noise (6 nV/ $\sqrt{\text{Hz}}$) and low power requirements. And the dual AD712, which has a low offset voltage of 0.30 mV, drift of 7 $\mu\text{V}/^\circ\text{C}$ and a 16 V/ μs min slew rate, delivers high performance at a low price.

THIS WILL MAKE MEDICAL EQUIPMENT DESIGNERS FEEL BETTER.

Major medical applications, such as CT scanners, digital X-ray and fluid analysis, require low noise and pA bias currents. And we've got just the right prescription.



For those who want low voltage noise,

but not at the expense of current noise, the AD743 and the

The Analog family



A system that isn't working in harmony is a system bound for failure. Particularly if the part acting up is your low noise op amp.

Whether it's current noise or voltage noise you're concerned about, there's a simple way to make sure your system keeps humming along. Get your low noise op amps from Analog Devices.

With the broadest line of low noise op amps around, we've

Performance of your entire system.

higher speed AD745 offer the best combination of specs — 3.2 nV/ $\sqrt{\text{Hz}}$ and 6.9 fA/ $\sqrt{\text{Hz}}$. If your emphasis is vice versa, then the AD645 has the specs you want — 0.6 fA/ $\sqrt{\text{Hz}}$ for current noise, and 9 nV/ $\sqrt{\text{Hz}}$ for voltage noise.

OP AMPS THAT ARE INSTRUMENTAL FOR INSTRUMENTATION.

If you're working in instrumentation applications, our op amps could prove to be instrumental in your design.

The world's lowest current noise (0.11 fA/ $\sqrt{\text{Hz}}$) monolithic op amp, the AD549, has 60 fA of input bias current — which is ideal for interfacing with very high

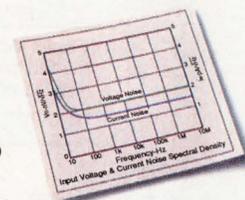
Model	Voltage Noise nV/ $\sqrt{\text{Hz}}$ @ 1 kHz typ	Current Noise fA/ $\sqrt{\text{Hz}}$ @ 1 kHz typ	Vos mV max	Supply Current mA typ	Input Bias Current max	SR V/ μs typ
AD829	2.0	1.5	0.5	5	7 μA	230
OP27/OP-37	3.0	400	.025	3	40 nA	2.8/17
AD743/745	3.2	6.9	0.5	8	250 pA	2.8/12.5
OP-275 (dual)	6	1500	1	4	350 nA	22
AD645	9	0.6	0.25	3	1.5 pA	2.0
AD712 (dual)	18	0.01	0.7	5	75 pA	20
AD548/648 (dual)	30	1.8	0.25/0.3	.34	10 pA	1.8
AD549	35	0.11	0.5	.60	60 fA	3

impedance sources. The AD548 (single) and AD648 (dual) deliver low bias current (10 pA), extremely low current noise (1.8 fA/ $\sqrt{\text{Hz}}$) and low power consumption at a highly attractive price. And the industry-standard OP-27 and OP-37 offer ultralow noise (3 nV/ $\sqrt{\text{Hz}}$ at 1 kHz) and precision dc performance.

of low noise op amps.

THE FASTEST LOW NOISE OP AMP AROUND.

If you need low noise but don't want to give up speed, then consider the extremely versatile AD829. It has low voltage and current noise (2 nV/ $\sqrt{\text{Hz}}$ and 1.5 pA/ $\sqrt{\text{Hz}}$, respectively), high speed (230 V/ μs slew rate) and excellent video performance (0.02% differential gain and 0.04° differential phase). Making it perfect for a range of applications including office automation, imaging and data acquisition systems.



GIVE US A SHOUT IF YOU NEED HELP.

Since all of these op amps are specifically designed for applications where low noise is critical, you can just drop them into your design and virtually forget about them.

Should you ever have a question, you'll be glad to hear that our products are backed by the most responsive applications support staff in the industry.



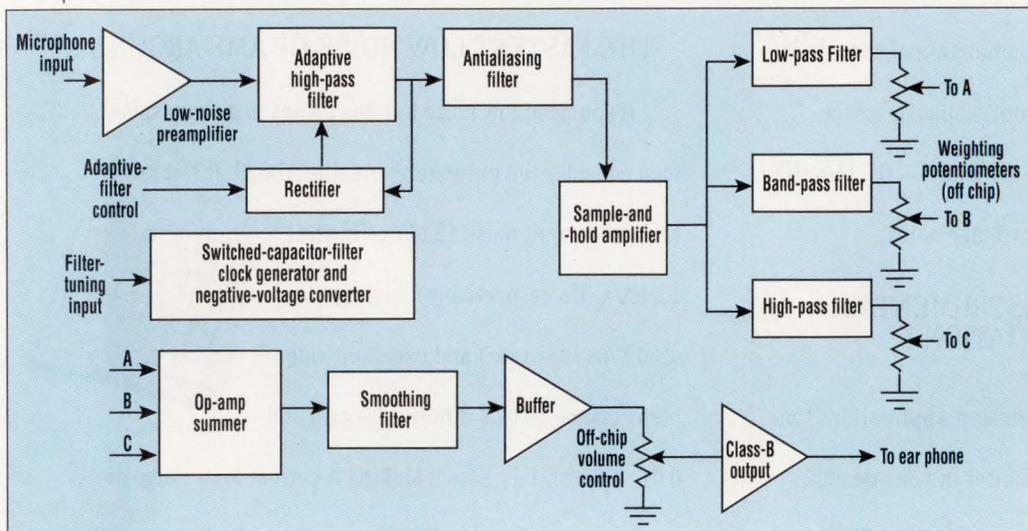
How responsive? Give us a shout at 1-800-262-5643 and see for yourself. We'll answer any questions you've got on choosing the right low noise op amp, plus send you a free low noise op amp selection guide and SPICE model library.

Or for more information on our low noise op amps, write to Analog Devices, P.O. Box 9106, Norwood, MA 02062-9106.



CIRCLE 84 FOR U.S. RESPONSE

CIRCLE 85 FOR RESPONSE OUTSIDE THE U.S.



2. TO REDUCE BACKGROUND NOISE for hearing-aid users, an adaptive high-pass filter is added in the signal path. This fourth-order continuous-time g_m/C filter reduces low- and mid-frequency gain as the signal level increases.

them to meet the unique needs of each patient. The weighted outputs are summed and smoothed by a second 12-kHz low-pass filter. The smoothing-filter's output is buffered, fed to a volume control, and then fed next to the hearing-aid's power amplifier.

Because the IC must operate from battery voltages as low as 1.1 V, a charge-pump develops a negative rail and clock drivers for the switched-capacitor circuits that swing beyond both rails. The 126-by-154-mil die uses less than 3 mA. It's built on a 3- μ m biCMOS process that also allows the building of thin-film resistors and non-voltage-sensitive MOS capacitors.

POWER PLAY

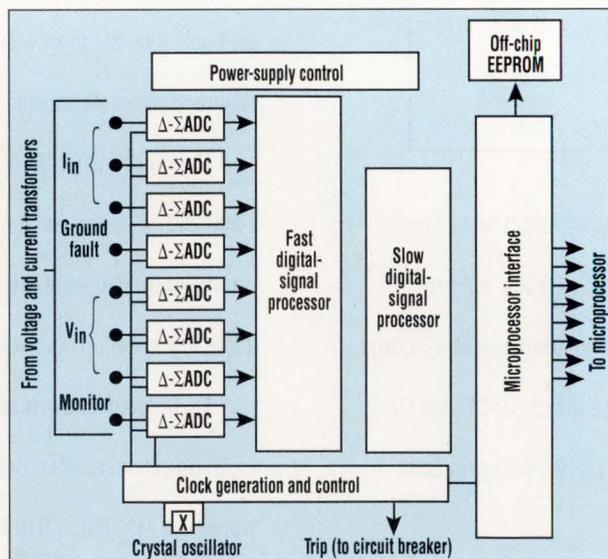
For the third CICC in a row, a design team sponsored by General Electric Corp., Schenectady, N.Y., and this year with participation by the University of Pennsylvania in Philadelphia, developed a mixed-signal IC to measure and manage three-phase ac power which they describe in session 19. Using multiple delta-sigma ADCs and a pair of bit-serial digital-signal pro-

cessors, this year's IC acquires and digitizes data from the three-phase power line and performs the calculations required for over-current protection, over and under-voltage protection, power metering, and frequency measurement. It transmits the results to a host via an asynchronous microprocessor interface and stores constants in an off-chip EEPROM.

entered from the EEPROM at power-up. To eliminate the effects of noise, tripping circuit breakers take two consecutive samples that exceed the threshold.

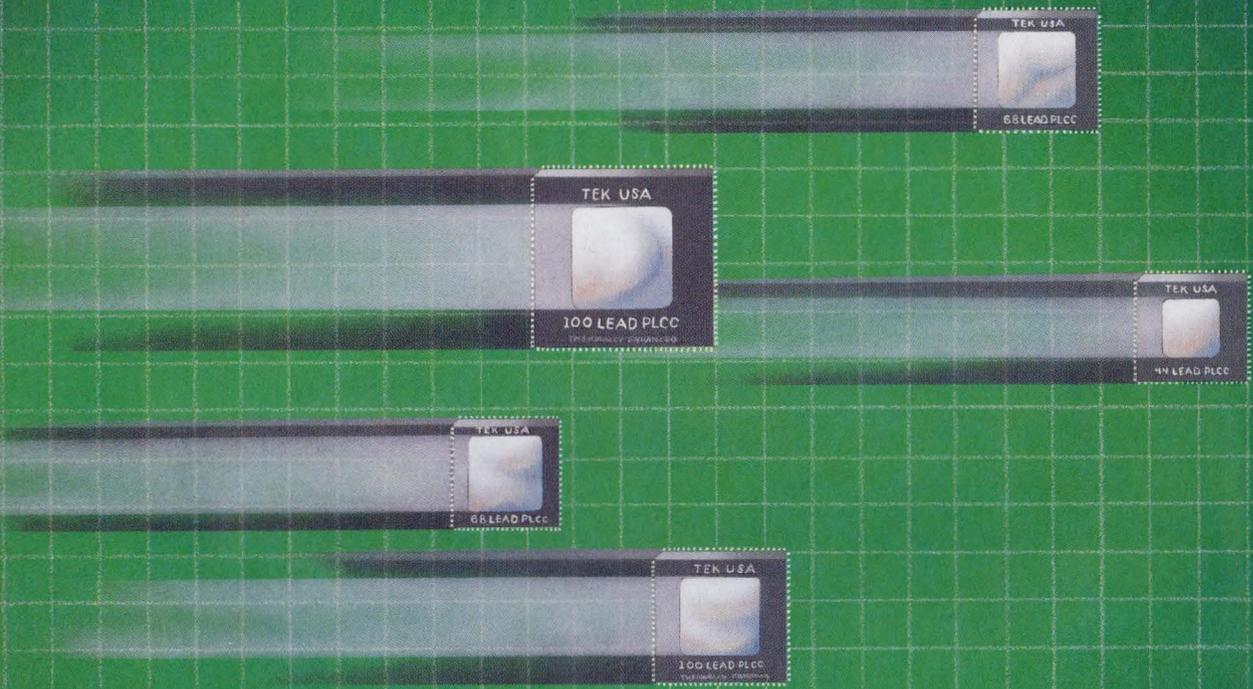
Data from the fast digital-signal processor is fed to the slow (1-MHz) digital-signal processor, which calculates frequency by counting the number of samples between zero crossings. Its first order digital high-pass filter can eliminate all dc offsets (without fear of destroying data) because transformers provide all the analog input signals. After filtering, a multiply accumulator calculates power for all three phases by multiplying voltage times current. Measurements indicate system accuracy is better than 1% for input levels within the metering range. The chip is built on a 1.5 μ m digital CMOS process.

While some of the faxes you receive may still be unreadable, sophisticated analog signal processing must be performed on signals from a fax-machine's scanning sensors to create a picture with 64 gray levels and 8-bit resolution. A CMOS IC from National Semiconductor, Herz-



3. EIGHT DELTA-SIGMA modulators in this IC monitor three-phase power-line voltage and current signals from transformers. The signals are fed to a pair of digital-signal processors, which calculate line power and fault conditions, tripping circuit breakers if necessary.

When Time Is Money ... Tektronix QuickCustom™ ASICs



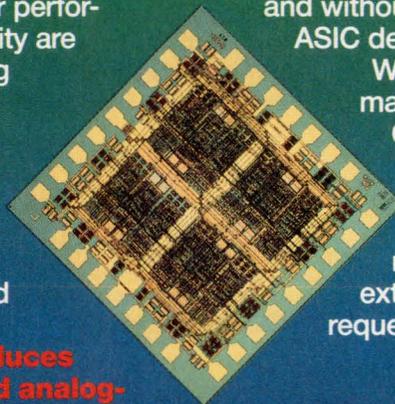
QuickCustom™ ASIC design methods from Tektronix provide convenient access to high performance bipolar technology. There are three effective design methods offered on the SHPi process with 8.5 GHz NPNs, Schottky diodes, JFETs, thin-film resistors, and PNPs. ♦ **QuickChip™ 6** semicustom analog arrays offer the fastest, lowest risk route between concept and finished product. ♦ Higher performance and greater flexibility are possible using the building block approach of **QuickTiles™**. Integration of mixed signal ASICs is fast using the digital cell library. ♦ **Full custom** design provides optimum performance and minimum die size.

Tektronix now introduces the QuickChip™ 7 mixed analog-digital array using a new, higher performance technology, GST-1. This high-density, 12 GHz process is Tektronix'

most advanced bipolar technology. Fiber optic telecommunications transceivers and high-speed mixed-signal applications are quickly implemented on the QuickChip 7 semicustom array.

QuickCustom design methods from Tektronix include the specialized design tools, accurate device modeling and experienced technical support necessary to develop ASICs quickly and without error. Even first time ASIC designers are successful.

When time and performance are critical, choose QuickCustom from Tektronix. For more information, please circle the reader number, call 800-835-9433 extension "100," or FAX your request to 503-627-5560.



Tektronix

Test and Measurement
CIRCLE 164 FOR U.S. RESPONSE

CIRCLE 165 FOR RESPONSE OUTSIDE THE U.S.

While you've been pushing the limits of digital devices,



HP's specially designed per-pin architecture makes high-performance testing an economic reality.

The HP 83000 Model F660 Digital Test System uses specially designed multi-chip modules to give you the performance you need to fully characterize designs on anything from GaAs to CMOS. With 50 ps accuracy. Speeds to 660 MHz. And up to 1024 chan-



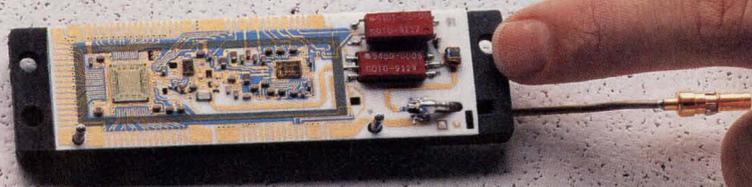
The HP 83000 Digital Test System for both engineering and production applications.

nels with true tester-per-pin architecture.

CAE links, automatic test functions, and software tools make test set up fast and characterization thorough. And there's one PMU for every 16 channels, for faster dc testing and greater throughput.

Yet, the HP 83000's highly integrated, modular electronics bring you all this performance at a cost that's less than tradi-

we've been pushing
the limits of testing.



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tional ATE systems. And since they make the footprint smaller and upgrading easier, cost of ownership is lower, too. In fact, every technical aspect of the HP 83000 system was designed with the best combination of performance and cost efficiency in mind.

So, if you're pushing the performance of digital devices, call **1-800-452-4844***. Ask for **Ext. 2898**, and we'll send you infor-

mation that explains how the HP 83000 lets you test them to their limits.

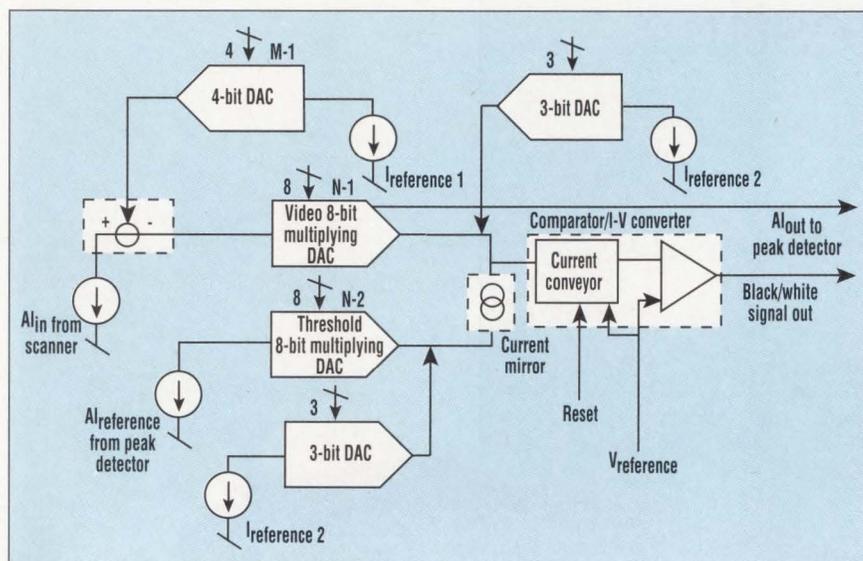
There is a better way.



* In Canada call 1-800-387-3867, Dept. 432.

CIRCLE 184 FOR U.S. RESPONSE

CIRCLE 185 FOR RESPONSE OUTSIDE THE U.S.



4. USING CURRENT-MODE analog circuit techniques, this IC processes the signals from a fax's CCD scanner, pixel-by-pixel, to provide a black/white output signal.

liya, Israel, which will ultimately be the analog portion of a fax system on a chip, performs this processing using current-mode circuits (Fig. 4).

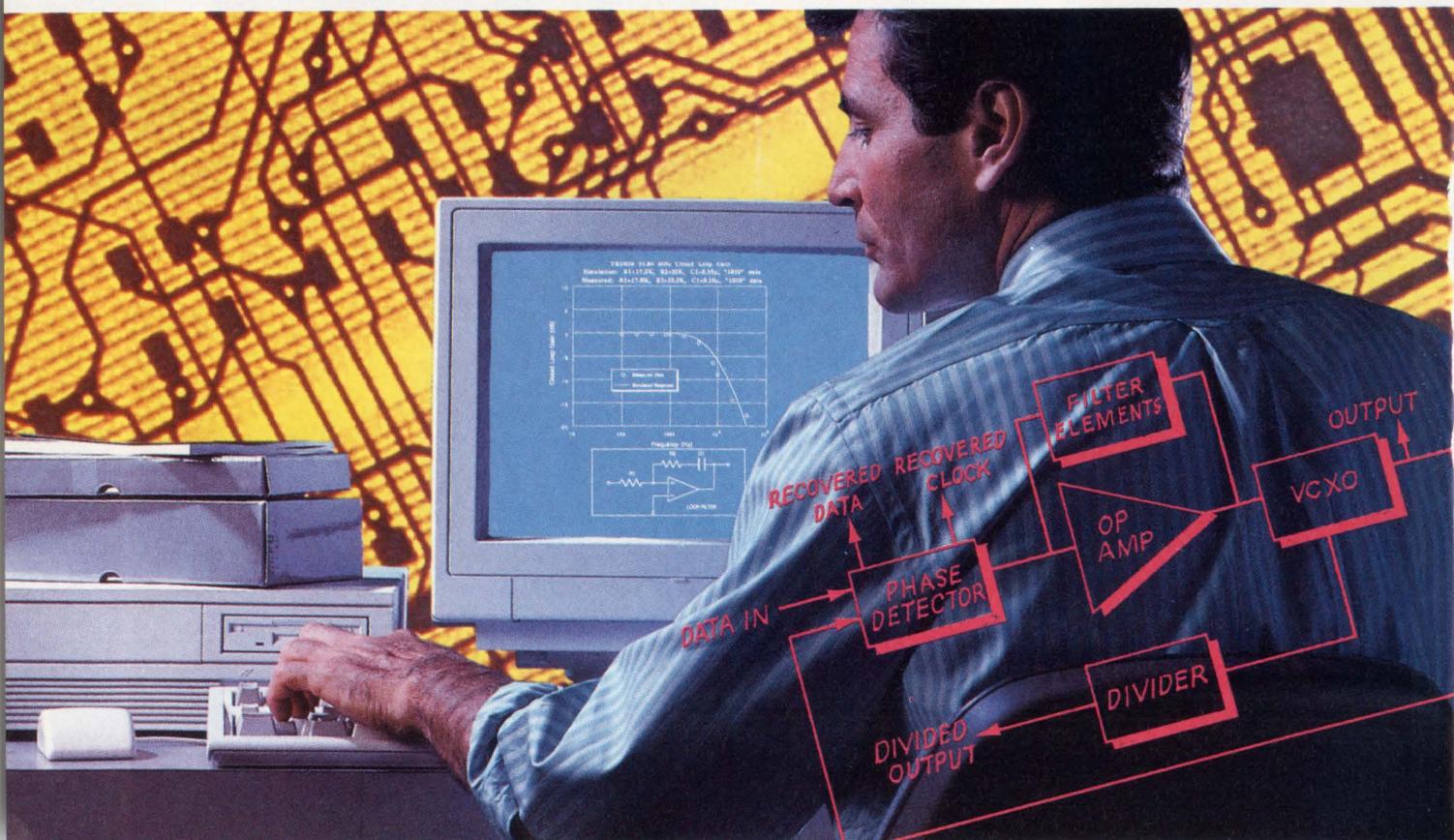
It's described in session 24.

The analog signal from the scanner, which is sampled at 2 MHz, is converted to a 0-4 mA current

source, A_{in} , which in turn feeds the analog input of an 8-bit, current-steering, video, multiplying DAC. During a calibration and offset-cancellation phase, which precedes every new page scan, a unique 8-bit code (N-1) is assigned to each of the scanner's pixels to bring them all to a common white level. This procedure takes advantage of the internal current comparator and is controlled by software. A 5-bit subsystem consisting of a 4-bit DAC, and a current mirror to reverse the direction of the correction current, cancels offset currents introduced by the external input circuitry, including that of the scanner. An internal current source supplies the reference for the 4-bit DAC and other system bias currents.

The video DAC has two identical current outputs. The first is compared with a reference value to produce one digital bit stating whether the pixel current is black or white. The second output is used by a peak-

Designing a "drop-in & power-up"

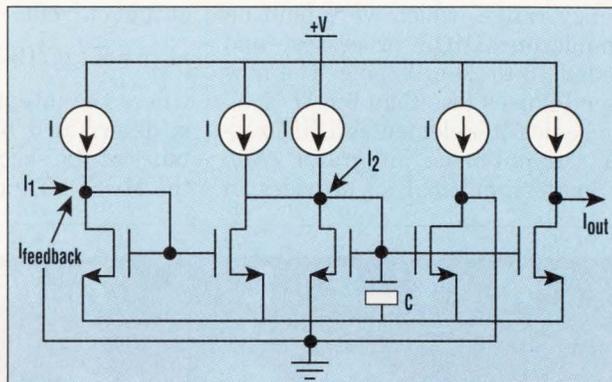


detector window (not shown) to produce a background referenced-current level, which is fed into the analog input of the threshold multiplying DAC. To create the 64-level gray scale, an 8-bit digital word from a Bayer matrix dithers the digital input of the threshold DAC. A current conveyor converts the difference in current from the two 8-bit DACs to a voltage level, which in turn is fed to the comparator (which finally makes the one-bit decision as to whether the pixel is black or white). The 3-bit DACs connected to the outputs of the 8-bit DACs cancel comparator offsets. The chip is built on a 1- μm double-metal CMOS process and uses 150 mW of power.

All things being equal, both sampled and continuous current-mode circuits, which are coming into their own for analog-signal processing, are faster than voltage-mode equivalents. A paper in session 24 from Philips Research Laboratories, Red-

hill, Surrey, England, describes a switched-current analog delay line with 10 taps, which provide a bandwidth of 5 MHz running with a clock frequency of 13.3 MHz. White noise is less than -50 dB, total harmonic distortion on a 665-kHz sine wave is below -40 dB (80% modulation) and clock noise is likewise under -40 dB. The chip was built on a conventional, 1- μm , digital CMOS process.

A joint team from Exar Integrated Systems Inc., San Jose, Calif., and Carnegie Mellon University, Pittsburgh, used current-mode techniques to build a continuous-time, fifth-order low-pass filter with a 3-dB



5. THIS CONTINUOUS-TIME low-pass filter circuit uses a current-mode g_m/C architecture to achieve a 40-MHz, 3-dB frequency while using less than 6 mW/pole.

bandwidth of 40 MHz. The filter is also described in session 24. The team adapted the g_m/C architecture, now being used for special-purpose disk-drive read-channel filters, to current-mode techniques, to build a general-purpose filter on a 2- μm digital CMOS process. That's in contrast with earlier g_m/C filters in this fre-

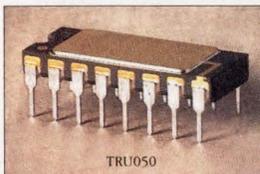
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quency range, which were built on sub-micron CMOS processes, and needed 15 to 20 mW/pole. The new filter IC uses less than 6 mW/pole. The basic filter element is a differential, current-mode integrator (Fig. 5). Small-signal analysis provides an

output current:

$$-I_{out} = K (g_m/C)(I_{in} - I_2)$$

where the integrator time constant is determined by the transconductance of the second stage divided by the MOSFET gate capacitance. The

cutoff frequency varies from 24 to 42 MHz by changing the bias current of the stage. An on-chip polysilicon resistor converts the input voltage to the current I_1 .

In session 2, a mask-programmable analog/mixed-signal array developed at Raytheon, Mountain View, Calif., represents one of the few bipolar ICs described at this year's CICC. The tile array is built on Raytheon's recently developed high-speed complementary bipolar process that provides npn transistors with an f_t of 5 GHz and pnp transistors with an f_t of 3 GHz. The chip's 30-odd analog and 50 digital macros can process analog signals to 200 MHz while providing ECL logic functions. Its 16 tiles contain over 300 transistors (ELECTRONIC DESIGN, Mar. 19, p. 143).

Future minimum-cost mixed-signal ASICs and custom ICs must depend on digital CMOS processes, while their high-performance kin must have bipolar devices, with EEPROMs providing "icing on the cake." With that concept in mind, a team at National Semiconductor, Santa Clara, Calif., developed a 1- μ m biCMOS process, described in session 9, with EEPROMs and an interpoly capacitor. The process' npn transistors provide an f_t of 5 GHz with a beta (current gain) of better than 75. The CMOS provides high-speed logic and analog switches while the npn transistors provide input circuits for low-noise op amps and fast comparators, ECL circuits, and output drive for both analog and digital circuits. The capacitors can be used to build switched-capacitor circuits and transconductance/capacitance filters. EEPROMs let the IC designer trim data converters, op amps, and smart sensors. The modular process with 12 to 22 mask steps allows the IC designer to ask for only the devices that are needed.

PAPER CLIPS AND ADCs

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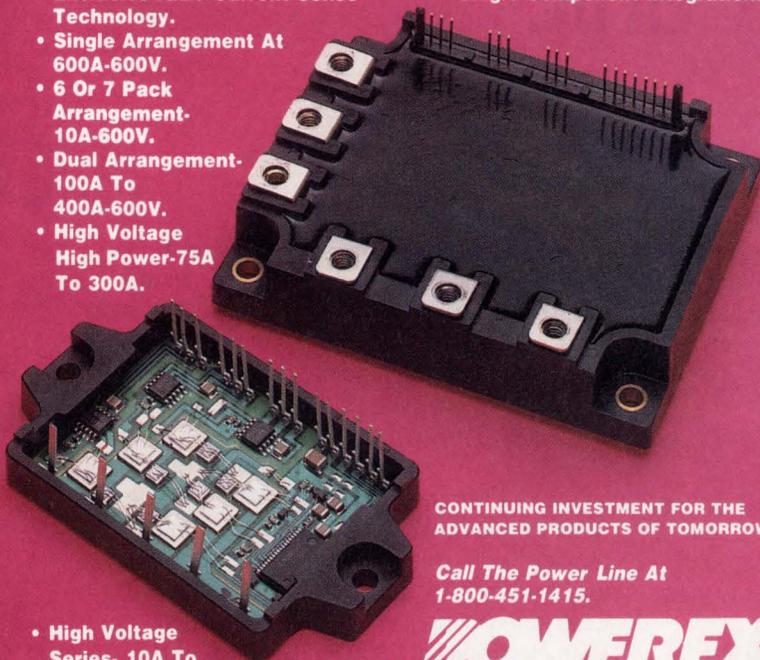
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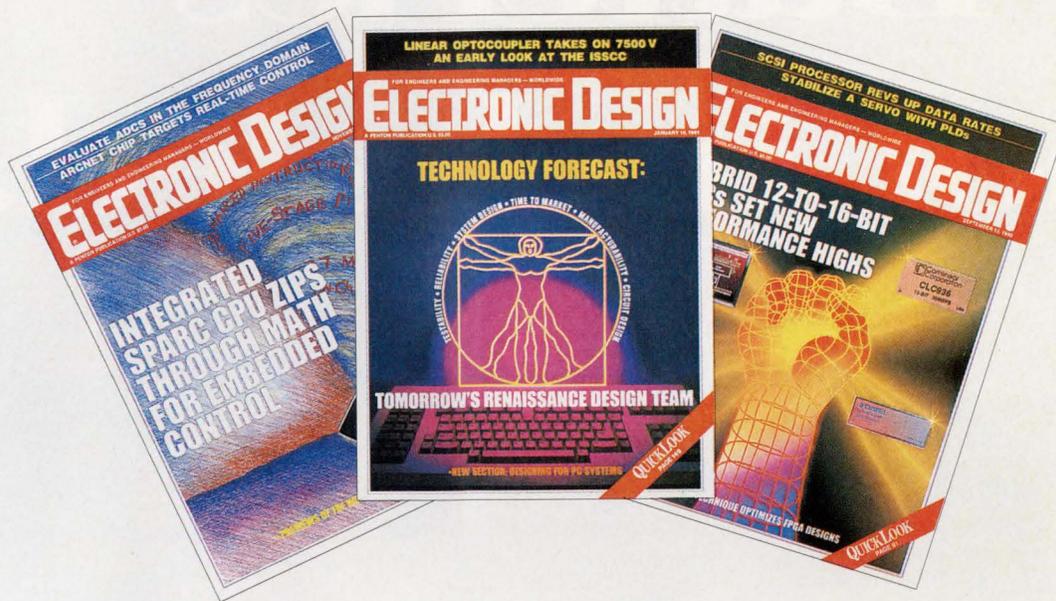
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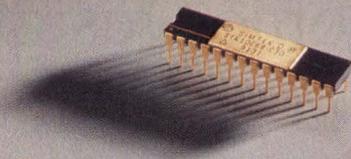
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same question in every analog designer's head. Developed at Micro Networks, Worcester, Mass., the ADC described in session 16 does not auto-zero its comparators prior to every conversion. Until now, the sampling rate of CMOS flash ICs was limited to about 50 MHz because time is taken for an auto-zero cycle between each conversion. The auto-zero cycle also increases power dissipation significantly, and corrupts the input signal as it interrupts the comparator's tracking of the input. In this converter, the comparators are only zeroed when required—for example at power-up, after every so many conversions, after a certain amount of time, randomly, or if the temperature of its environment has changed by more than a few degrees. At 125 MHz, the converter dissipates under 200 mW. Differential non-linearity error is under 1/2 LSB.

To many experts, the delta-sigma ADC is a "low-frequency" tool with its effective signal bandwidth topping out well below 100 kHz. However, some IC designers ignore the experts. A pair of teams, one from the Tampere University of Technology, Tampere, Finland, and the other a joint team from the University of Toronto in Canada and Analog Devices, Norwood, Mass., didn't get the word. As described in session 16, the teams developed higher-frequency, fourth-order delta-sigma modulators—they left the digital filtering for others. Tampere's 1.2- μ m CMOS modulator samples 100-kHz sine waves at 50 MHz, achieving 16-bit signal-to-quantization noise, and 9 effective bits of resolution (56 dB) while sampling 781 kHz.

The University of Toronto/Analog Devices group built a modulator with quite different noise-shaping characteristics: Rather than nulling the quantization noise at low frequencies close to dc, they created a switched-capacitor modulator designed to convert signals centered at a frequency of 455 kHz (AM broadcast IF band) with a bandwidth of 10 kHz. Simulations indicate 14-bit performance sampling at 1.82 MHz. Measured results are expected to be provided at the conference. □

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EDA-software advances abound for analog, synthesis areas

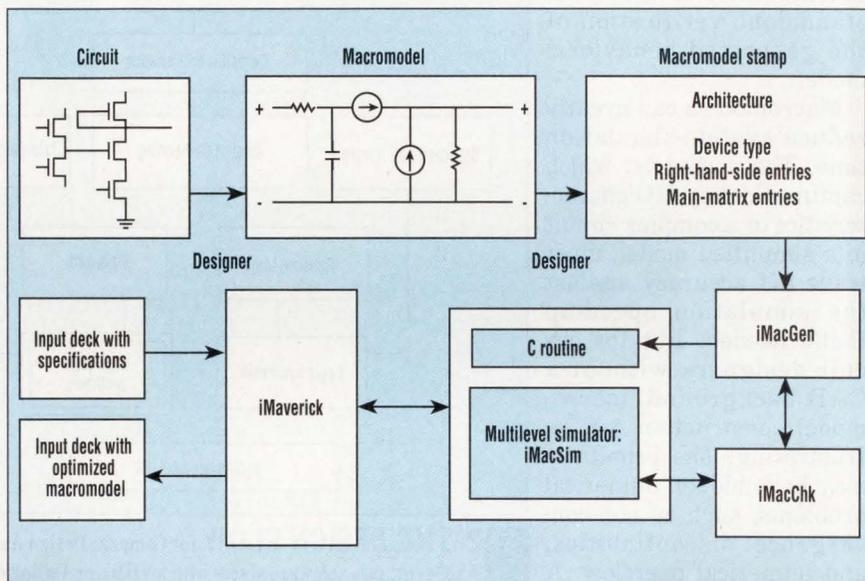
Engineers look to design analog circuits at a higher level, and synthesize more of their designs. **BY LISA MALINIAK**

Although electronic design automation (EDA) has matured for much of the industry, some areas of EDA can stand significant improvement. At this year's CICC, many of the design-automation papers focus on two of those trouble spots: analog and mixed-signal design, and analog and digital synthesis.

In session 8, a paper from the University of Calif. at Berkeley explains a top-down, constraint-driven design methodology with five key points for analog ICs. The first is that the methodology must be a top-down hierarchical process starting from the behavioral level based on early verification and constraint propagation. It must also have both bottom-up accurate extraction and verification, and automatic and interactive synthesis of components with specification constraint-driven layout design tools. The fourth point is that the methodology must include maximum support for automatic synthesis tools to accommodate users of different levels of expertise, but it shouldn't force these tools upon users. This isn't an automatic synthesis process. Lastly, the methodology must consider testability at all design stages.

The top-down process implies a well-defined behavioral description of the analog function. Characterizing analog-circuit behavior is quite different than characterizing digital circuits. Analog characterization must account not only for the function that the circuit will perform, but also for the second-order nonidealities intrinsic to analog operation.

To shorten the design cycle, it's essential that design problems be discovered early on. That's why behavioral simulation is so important to any methodology. Simulation can help select the correct architecture



1. AN ANALOG MODELING AND SIMULATION environment developed at the University of Illinois provides rapid prototyping of primitives (iMacGen), automatic numerical-consistency checking (iMacChk), macromodel optimization (iMaverick), and simulation (iMacSim).

with which to implement the analog function, while staying within the nonidealities that a given set of system specifications will permit.

Another paper on analog design addresses the automatic generation of analog models for behavioral simulation. Vanderbilt Univ., Nashville, Tenn., and AT&T Bell Laboratories, Allentown, Pa., join forces in session 12 to explain the automatic generation of transient simulation models for AT&T's mixed-mode behavioral simulator. The models are generated from higher-level transfer-function specifications in the s and z domains. Behavioral models can be defined at varying levels of abstraction. They can be defined in terms of state-space models, algebraic expressions, and mixed algebraic and differential equations. The individual simulation models, which are written in the Analog Behavior Circuit Description

Language (ABCDL); represent the subsystems that are linked to simulate the functional behavior of an entire system.

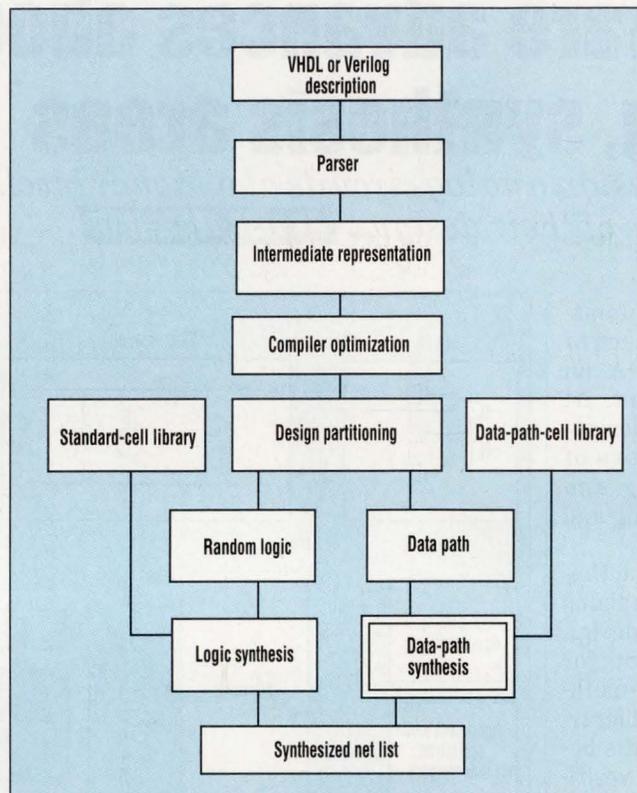
A large class of analog systems, such as filters, can be represented at a behavioral level in terms of s-domain or z-domain transfer functions. The behavioral transient simulation models for these systems are based on differential equations or state variables. Manually generating such models entails the derivation of the state-variable model, and encoding the state-variable model into the behavioral description language. The manual procedure, however, can be difficult and error-prone.

The automatic model-generation programs gensims (s-domain) and gensimz (z-domain) derive appropriate state-variable models from transfer-function specifications using the phase-variable technique.

These model generators create an ABCDL behavioral model for an analog subsystem described by a higher-level transfer function. Also generated are the model connectivity definition to interface with other simulation models, as well as a set of test vectors or signals for standalone verification of the generated behavioral model.

Macromodels can greatly reduce system-simulation time. These models, which capture the key I/O characteristics of a complex circuit in a simplified model, must trade off accuracy against the simulation speed-up that's needed. But for circuit designers without a CAD background, macromodel construction can be frustrating. The primitives may have hidden numerical problems, such as non-convergence, discontinuities, and numerical overflow. A paper from the Coordinated Science Laboratory (CSL) of the University of Illinois, Urbana-Champaign, in session 12, describes a set of tools that can create, simulate, and optimize analog macromodels. (Fig. 1).

To use the system, the engineer first identifies the circuit block to be replaced by a macromodel. Then a macromodel is constructed using primitives. Primitives that don't already exist can be added to the simulator in an AHDL-like format. The first program, iMacGen, checks the syntax of the AHDL description of a new primitive, translates it into a C file, compiles it, and links it to the iMacSim macromodel simulator. Once the primitive is created, its numerical integrity must be checked before it can be safely used. A tool called iMacChk enables the primitive-debugging mechanism, and simulates the primitives in the user-specified region of operation. Simulation is under extreme conditions to ensure that the primitives have no hidden numerical problems.



2. THE DESIGN FLOW for Compass Design Automation's ASIC-synthesis software starts with a VHDL or Verilog description that's eventually partitioned into random-logic and data-path sections. The sections are synthesized with two compilers, resulting in data paths with better speed and area performance.

After all of the primitives are entered and debugged, a macromodel with a given set of parameters can be constructed. Designers use iMaverick to optimize the macromodel parameters to their specification. After optimization, the macromodel is employed in iMacSim—a multilevel analog simulator that allows behavioral, macromodel, and circuit-level descriptions to be specified in one input file—as part of a larger simulation. The simulator combines the different algorithms needed for each type of simulation, and further reduces run time by event-driven techniques.

With mixed-signal ICs growing more complex, mixed-mode simulators are springing up to aid in their development. Until now, the designer has been responsible for choosing the levels of simulation for a given circuit. But this is a tedious and error-prone task, because the designer may not be familiar with the underlying

algorithms used in the mixed-mode simulator. The CSL of the University of Illinois, Urbana-Champaign, describes a program in session 12 called iSplit that automatically recognizes collections of transistors as higher-level blocks. Thus, the iSplice3 mixed-mode simulator receives a circuit description that's broken down into its analog and digital portions—difficult and time-consuming manually.

The iSplit program reads in a transistor net list in iSplice format and generates a new net list containing higher-level models that are recognized in the transistor network. Initially, the transistor circuit is divided into strongly connected components (SCCs) based on transistors connected at the sources and drains. Then the program makes two passes to identify higher-level blocks in each of the SCCs. In the first pass, the program recognizes any complex CMOS gates. In the second, it attempts to recognize user-defined cells that are kept

in a library file. This process continues until each of the circuit's high-level blocks are recognized.

It should be noted, however, that using higher-level models isn't always appropriate. That's because several existing conditions can cause the logic elements to give incorrect partitioning results. Examples include situations where an input of a gate assumes a voltage in the invalid region between V_{IL} and V_{IH} , or if two gates are driving the same node, as in a wired-OR connection. If any such situations occur, the higher-level model can't be used. But a modified iSplice3 simulator that supports a dynamic approach can solve the problem. It stores a logic model and a complete transistor description for each gate. If it detects a situation that could cause the gate-level model to give a wrong result, the transistor-level description is switched in

and is used from that point on.

Another approach for mixed-mode simulation involves using general building blocks to simulate sampled-data systems (SDSs). In session 12, Analogy Inc., Beaverton, Ore., describes its efforts to use such blocks to model a sigma-delta analog-to-digital converter. The blocks, known as SDS templates, have analog states as their inputs and outputs. The transfer functions of the SDS templates are specified in the *z* or *s* domains. Interface templates to make connections between three types of signals (continuous analog, analog state, and digital state) have also been developed. These interface templates allow a mixed-mode system of mixtures of analog, SDS, and digital parts to be simulated.

In using the approach to model a triple-state sigma-delta ADC, it was found that using SDS templates had a number of advantages. One is that they can mix three types of signals.

Another is the ability to specify transfer functions in either the *z* or *s* domains, depending on the designer's convention. A third is the speed and convenience of the approach. With the templates, an SDS could be simulated at the system level to verify the system's specification before designing at the transistor level.

By partitioning a VHDL description of a digital system into datapath and random-logic blocks, a new method of synthesizing high-density bit-slice data paths creates layouts that are faster and smaller than standard-cell-based random-logic designs. In one technology, the approach yielded a high-speed, 16-bit-datapath adder that was about 40% smaller and 40% faster than a similar standard-cell adder. Compass Design Automation, San Jose, Calif., has determined in session 5 that partitioning a high-performance ASIC design in this fashion eliminates the suboptimal data paths that result

from using register-transfer-level synthesis tools. These tools map data-path operations into a gate-level random-logic description, which is then implemented in standard cells.

In the new approach, after the VHDL description is translated into an intermediate representation (IR), the IR is optimized using compiler-optimization techniques, such as the elimination of common subexpressions. The IR is then partitioned into two parts. The first part is synthesized in random logic, and the second is synthesized using cells from a data-path library (*Fig. 2*). The library contains such cells as adders, subtractors, and ALUs. It also contains various cells for area and speed trade-off, such as high-speed (large-area) and high-density (low-speed) adders. With these cells, the tool tries to create the smallest design that meets a given timing constraint by selecting the appropriate cells and resource sharing. □

Mixed-signal, analog testing covered in CICC sessions

The two hot topics join subjects like data compaction and boundary-scan techniques. **BY JOHN NOVELLINO**

With the increasing complexity of ICs, the importance of concurrent engineering and design for testability cannot be overemphasized. Test engineers must get involved in the design process as early as possible. Even then, without the appropriate tools, the team will find that test development takes more time than circuit design. Recognizing this need, the CICC includes two technical sessions devoted to test. Two more CICC sessions are titled "High-performance devices and test methodologies" and "Design partitioning and formal verification".

Mixed-signal devices are proliferating, but few tools exist to help generate test programs for mixed-signal testers. A paper in session 2 by William H. Kao and Jean Xia of Cadence Design Systems, Santa Clara, Calif.,

and Tom Boydston of Teradyne, Boston, describes such tools. The authors show how designers or test engineers can use the new tools to capture test information during the design phase, then automatically create test programs for test modules, order and prioritize the tests, and create the final test program.

Tester-required information and other test data, in the form of test-module schematics, is captured during the design phase using a schematic editor. The editor also captures the full test schematic, which includes tester resources, loadboard components, and a symbolic abstraction of the device under test. On the test schematic, graphic icons or symbols represent every tester resource. The symbols may be considered generic, but the underlying properties

are tester-specific.

Next, a test sequencer allows the engineer to graphically arrange the order of the specific tests. Users can change the order as their needs change. Finally, the source-code generator takes the information supplied by the full test schematic and the sequencer tool, and automatically creates code needed for the requested tests. The code is written in the language of the target tester.

Another subject that's becoming more common, analog ICs, is discussed in two papers. In a paper in session 17, E. Paul Ratazzi of the Rome Laboratory at Griffiss Air Force Base, Rome, N.Y., describes an attempt to find a way to measure the fault-detection coverage that a test sequence provides for a specific analog device. Ratazzi notes that

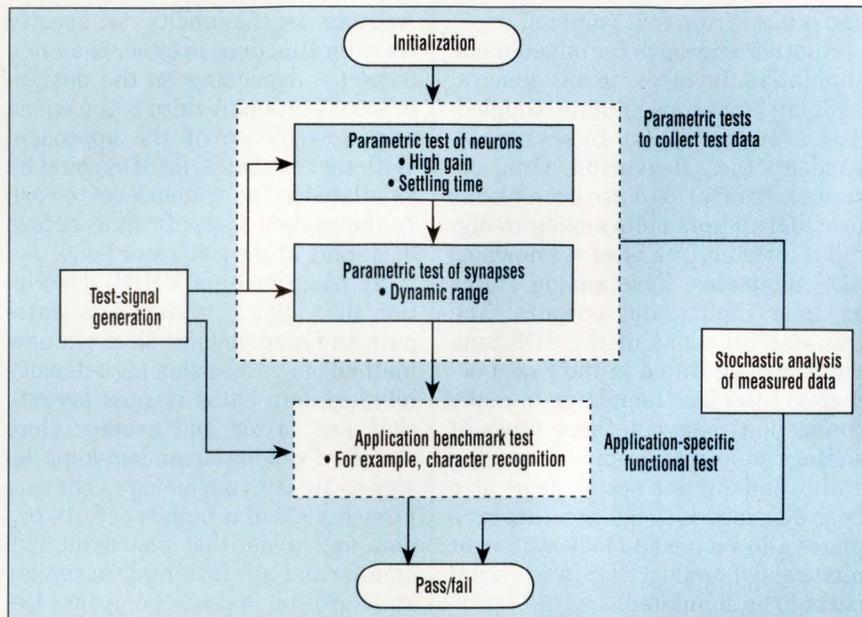
measuring fault coverage is important in the design of complex digital devices. Analog designers, however, have been unable to quantify fault coverage, mainly due to the non-deterministic nature of analog circuits.

The first step in the effort was to sponsor the development of techniques for defining a fault dictionary for a circuit. To do this, faults can be inserted, one at a time, into the device under test, whose output is then recorded in the fault dictionary. Many iterations are needed to account for the circuit's nominal component variations. Data representing an unknown circuit condition is presented to the resulting measurement tool. Using the fault dictionary, the tool makes a statistically based decision to determine a circuit fault. Consistently incorrect results indicate a fault that the test circuit doesn't propagate to its output, a fault not covered by the test sequence.

Experiments have turned up many faults that are detected by one type of test but not by another type, says Ratazzi. The paper concludes that a number of concerns must be addressed before the techniques being investigated are deemed useful.

Analog circuitry is also the subject of a paper in session 17 by Sudhir M. Gowda, Bing J. Sheu, and Joongho Choi of the University of Southern California at Los Angeles. The authors show how to test electronic neural-network chips, which consist of large arrays of several thousand synapse cells interconnecting input and output neuron arrays.

The test sequence used was to first test the input and output neurons, next test the synapse array, and then compare achieved performance to a benchmark application (Fig. 1). A fault's effect on network operation depends on the design style used to build the network, so the test method must exploit the behavior of circuit elements in a specific implementation. The authors describe a detailed measurement setup and results of tests on two types of network chips. The parametric test of the neurons involves measuring dc and transient characteristics of



1. HELP IN TESTING ANALOG neural-network processors is available in the form of a systematic test procedure. The procedure includes a comparison of results against an appropriate benchmark application.

single neurons. The parametric tests of the synapse array determines the dynamic range and linearity of individual synapse cells.

Results are presented in the form of a histogram to which a Gaussian curve was fitted and normalized. Curve characteristics, such as the mean and standard deviation, were used to evaluate the circuit's ability to run error-free. The authors note that a benchmark application can help determine the tolerable mean and standard deviation.

Two authors from AT&T Bell Laboratories, Princeton, N.J., note that the massive amounts of test data generated by today's ICs make test-data compaction an important issue. In their paper, presented in session 13, Eleanor Wu and Marsha Ramer Moskowitz describe a real-time compaction scheme that uses multiple input shift registers (MISRs) in a type of signature analysis. They say their technique can save 65% in hardware costs compared to other schemes while adding only 1% to the error-escape probability.

In the new technique, several outputs are space-compacted by a pattern recognizer (Fig. 2). In effect, the values of several outputs are coded

into a 0 or a 1, depending on the occurrence of a particular pattern. The pattern-recognizer's output goes to one of the MISR cells for time compaction.

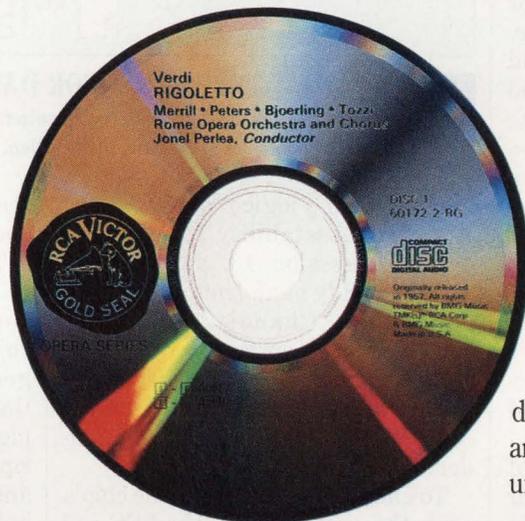
Because the technique uses space compaction, the error-escape probability depends on which outputs are grouped together. Wu and Moskowitz ran experiments on several circuits using randomly-selected groups of four, five, and eight outputs. The experiments were then run with groups of the same size but selected in a way that minimized overlap among the outputs.

In one circuit, the error-escape probability went from 9% for randomly selected groups of eight to 1.1% for groups of eight with minimal overlap. In another experimental circuit, the probability dropped from 1.3% to only 0.2% for a four-to-one space compaction.

The new scheme is easy to implement, according to the paper. Engineers first select the outputs for space compaction using a straightforward bin-packing algorithm and a specified amount of overlap. They then choose the pattern for the recognizer. Tests showed that the pattern that most often occurred in true-



The difference between AVX tantalum capacitors and the competition is just as noteworthy.



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4-50V	4-50V	6.3-50V	6.3-50V	4-50V	2-20V	2-50V	2-50V	2-50V

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CIRCLE 175 FOR RESPONSE OUTSIDE THE U.S.

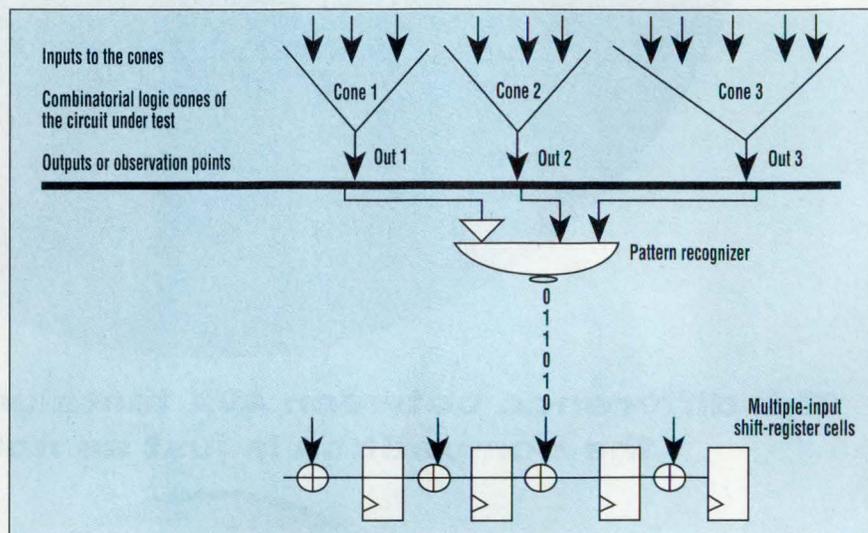
value simulation can be used.

Signature analysis and data compression are also the subjects of a paper in session 13 by D. Jani, B. Cohen, and J.M. Acken of Intel Corp., Santa Clara, Calif. The authors present two scenarios involving a design with built-in self test (BIST) based on linear-feedback shift registers (LFSRs). In the first, test patterns are repeatedly applied to the LFSR-based signature analyzer. In the second, a circuit under test with k outputs is connected to a MISR with r stages, where k is less than r .

The authors analyze two practical design issues: The effect on error masking and aliasing of applying repeated test patterns to an LFSR, and the effect on error masking and aliasing of tap-point selection on the MISR. According to the paper, the length of the LFSR should be chosen to meet the minimum-acceptable level of aliasing. And when the circuit under test has fewer outputs than the MISR has stages, the selection of the tap point affects both aliasing and error masking. The engineer's goal is to ensure that the tap selection maintains the distribution of possible MISR input sequences.

Included in the paper is a review of the standard calculations for error masking in LFSR-based BIST. The paper also covers the error calculations for optimum tap selection when an MISR is used.

Boundary-scan techniques have been well accepted since their adoption as a formal standard two years ago (IEEE-1149.1). But designers can still use some help in implement-



2. IN A NEW TECHNIQUE FOR DATA COMPACTION, several outputs are first space-compacted by a pattern recognizer. The recognizer's output then goes to a multiple-input shift register for time compaction.

ing the on-chip logic required by the design-for-testability standard. A paper in session 13, authored by Madhu Reddy et al. from Motorola's ASIC Div., Chandler, Ariz., describes how the company created the test-access port and boundary-scan chain (BSC) logic on the H4C family of 0.8- μ m, three-layer metal high-density CMOS gate arrays.

To ensure easy access to the chip's core, the authors note, the BSC cell devices are laid out on the top of the I/O buffer, with BSC signal lines running through the buffer between the top row and the bottom row of the BSC devices. When the BSC of other I/O cells are on adjacent I/O sites, the signal lines are connected by abutment. At an unused I/O site,

the lines are continued by means of a special "wire cell."

The H4C implementation offers a number of advantages including compactness, 100% usage in the chip's periphery, less routing congestion in the core area, less delay in the signal path because the multiplexer in the path is also in the periphery, and the elimination of race and hold problems because the skew between clock signals for adjacent BSC cells is minimal. The design also allowed a high BSC clock speed, use of power/ground and unconnected I/O sites for BSC logic, and electrical isolation of the BSC logic from noise. A test chip has been manufactured, and the test logic has been operated at over 25 MHz. □

CICC unfurls an array of advanced ICs for communications

Various semiconductor processes are being explored for smaller, faster, and lower-power ICs. **BY MILT LEONARD**

Advanced concepts in VLSI IC design at this year's CICC are promising dramatic improvements across the broad spectrum of communications technology. Chip designers are

pulling out all the stops in applying CMOS, biCMOS, silicon bipolar, and gallium-arsenide processing technologies to produce smaller, faster, and lower-cost semiconductors with

mixed-signal capability. These chips will implement a wide variety of communications standards, protocols, and signal-processing algorithms. Hoping to reap the benefits of these

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developments are systems ranging from personal-communications terminals, internetworked computers and peripherals, and high-performance TV.

The Cellular Telecommunications Industry Association announced that last year saw the number of cellular-telephone subscribers in the U.S. jump 43% to a total of 7.6 million. In Europe, 15 to 20 million people are expected to use the Digital European Cordless Telecommunication (DECT) system by 1999. Semiconductor companies are answering the demands of the portable and mobile communications market by producing highly integrated, cost-effective analog and digital circuits that operate at higher frequencies and with lower voltages and less current.

This trend is apparent in session 1 covering global wireless communications. In this session, Qualcomm Inc., San Diego, Calif., overviews the code-division, multiple-access (CDMA) system being proposed as a North American digital-cellular system standard. Over-the-air specifications, system implementation, and

end-to-end spread-spectrum system functions are examined.

A second Qualcomm presentation describes a single-chip mobile-station modem that supports both the existing analog cellular standard and the proposed new digital standard. Built on a 0.8- μm double-metal CMOS process, the modem integrates an original 3-chip set onto one ASIC containing about 350,000 transistors and 24 kbits of static RAM. The circuit includes most of the hardware functions required in the subscriber unit.

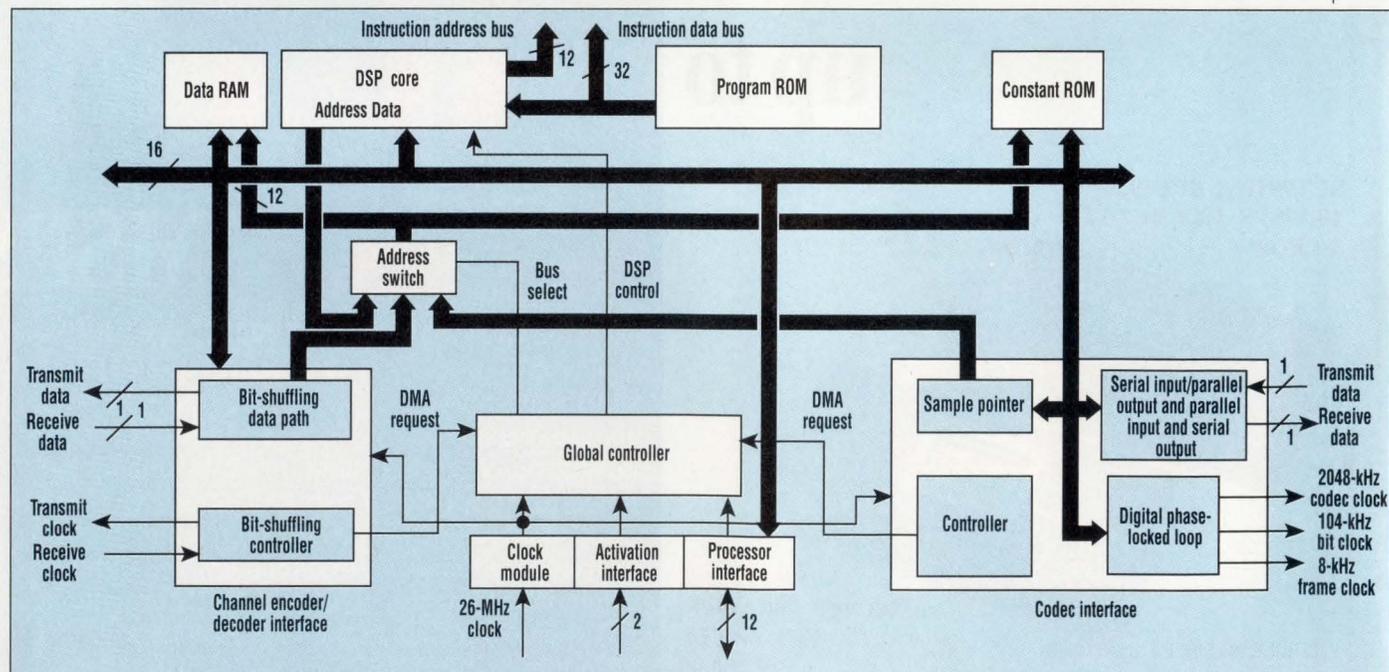
In session 10, Philips Kommunikations Industrie AG, Nuremberg, Germany, reports on its ASIC approach to building a single-chip DSP core. The ASIC integrates the functions required in a 900-MHz GSM handheld terminal (GSM is the European standard for digital mobile cellular-radio systems). Called the KISS-16V12, the ASIC includes 11-kwords-by-16-bits of ROM, 2.5-kwords-by-16-bits of RAM, a 16-by-16-bit multiplier, and 13 independent interrupt sources. The 1- μm CMOS device operates with an instruction

cycle time of 50 ns.

In the same session, GSM devices are also the subject of two joint papers from Alcatel Bell Telephone, Antwerp, Belgium, and Alcatel Radiotelephone, Colombes, France. The first device is an 85-mm², 1.2- μm CMOS DSP core used at the transmitting and receiving ends of a GSM communications link (Fig. 1). At the transmitter side of the circuit, the device converts a 104-kbit/s digitized voice signal into a 13-kbit/s stream, using an algorithm that's based on regular pulse excitation, long-term prediction, and linear-predictive coding. The reverse operation is performed on the receiver side.

Alcatel's second paper describes a baseband transceiver chip for a handheld GSM portable station. The 38- μm^2 , mixed-signal CMOS device supports the various ASICs in a radio subassembly for a GSM handheld terminal by providing channel filtering, controlling mismatches between the I and Q channels, and supporting predictive AGC.

Another development in session 10 comes from National Semiconductor



1. THE DISTRIBUTED-PROCESSING ARCHITECTURE of Alcatel's voice encoder/decoder chip ties the data bus and central data memory to the DSP core, the channel encoder/decoder interface, and the codec interface through a DMA mechanism. The DSP core handles all computationally intensive tasks, and the channel encoder/decoder performs real-time bit shuffling and reordering. Synchronizing speech-related tasks is done by the activation section of the two-part control interface. The codec interface uses a pointer function to store and retrieve samples to and from the buffer memory.



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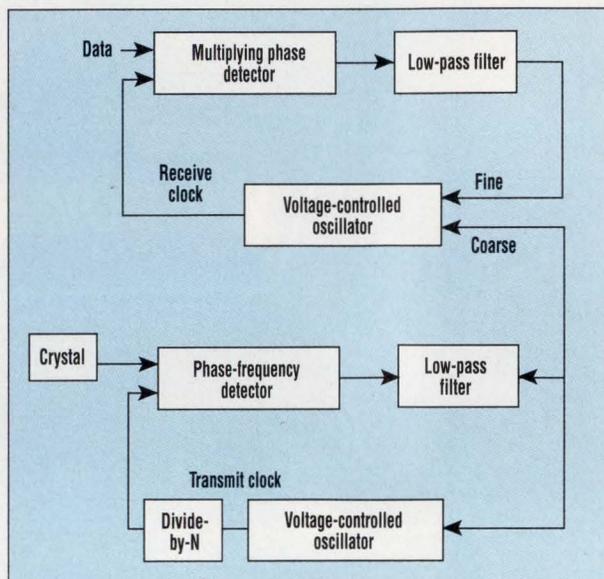
Corp., Santa Clara, Calif. The company created an experimental transceiver chip set for 1.9-GHz DECT (Digital European Cordless Telecommunication) systems. Fabricated with a 0.8- μm biCMOS process that has a 15-GHz f_t , the chip set consists of a down/up converter, a quadrature receiver, and a quadrature transmitter.

Communication ICs that operate on just a trickle of power are described by Toshiba Corp., Kawasaki, Japan, in session 10. The company has developed a 0.8- μm^2 , GaAs dual-modulus prescaler for single-cell battery operation. Implementing 60/64 and 120/128 frequency dividers, the 1-GHz prescaler chip draws 5.5 mA from a 0.8-V source and is functional down to 0.65 V.

A similar trend is exhibited in session 24 where engineers from Motorola Inc., Austin, Texas, and Mesa, Ariz., discuss a biCMOS frequency synthesizer for portable telephones. This device operates from 2.7 V drawing 7.6 mA at a 1.2-GHz input.

Several sessions offer technical papers involving optical-fiber data links. In session 1, Applied Micro Circuits Corp., San Diego, Calif., introduces a 1.0625-GHz transmitter-receiver chip set that can be used with 200- to 1244-MHz fiber-based digital-interface applications. The chips are implemented with mixed-signal ECL/TTL logic arrays fabricated with a 1- μm bipolar process. A custom phase-locked loop (PLL) is integrated on the chips. Customizing the logic cells creates transceiver designs for popular data-communications and telecommunications applications, such as SONET, HIPPI (high-performance parallel interface) serial, and Scalable Coherent Interface.

A biCMOS implementation of a related device is the subject of a session 29 presentation by the Massachusetts Institute of Technology,



2. IN THE DUAL-LOOP ARCHITECTURE of MIT's transmit/receive IC, the transmit frequency-synthesis loop (bottom) consists of a voltage-controlled oscillator (VCO), a prescaler, phase-frequency detector, and a loop filter to generate the transmit clock from a reference frequency. With an identical VCO, phase detector, and loop filter, the receive loop (top) uses the transmit-loop control voltage as a coarse adjustment to its VCO. Feedback for this loop is through a fine adjustment to the VCO to ensure that the loop center frequency is within the VCO mismatch of the input data rate.

Cambridge, Mass. The crux of the paper involves a transceiver chip set fabricated in a 1.2- μm process. The devices use PLLs for frequency synthesis and clock recovery in a master-slave architecture. The frequency reference is employed so that the transmit loop can set the center frequency of the receiver loop (Fig. 2). The circuits consume 750 mW from a 5-V supply.

Multiplexers and demultiplexers are key components in high-speed optical communication systems. For SONET applications, National Semiconductor reports on a 0.8- μm gate array with 700 ECL gates and 2000 biCMOS gates for implementing a SONET 2.4-Gbit/s multiplexer or demultiplexer. In addition to circuit operations, this session 1 presentation describes in detail the unique design of the 68-pin leaded chip carrier that houses the array. For high-frequency operation, the package uses short leads and has seven different planes to handle 2.4-GHz inputs and out-

puts, as well as mixed ECL, TTL, and CMOS signal pins.

Similar chips are described in another session 29 presentation, this by Hewlett-Packard Co., Palo Alto, Calif. On tap are an 8:1 retimed multiplexer and a 1:8 demultiplexer that operate at 10 Gbits/s. The multiplexer and demultiplexer are fabricated with a 0.8- μm silicon bipolar process and dissipate 3.8 and 4.3 W, respectively. Each chip measures 2.5 by 1.6 mm.

Session 29 also introduces a chip set from NEC Corp., Kawasaki, Japan, that teams an 8:1 multiplexer with a laser-diode driver. The multiplexer operates with ECL-level inputs. The laser-diode driver provides up to 90 mA of drive current. For use in SDH (Synchronous Digital Hierarchy) equipment, the chips are made in a 0.8- μm CMOS process and operate at up to 750 Mbits/s. The chips' designers report a jitter of under 400 ps.

Two session 14 papers also address SDH and SONET devices. AT&T Bell Laboratories, Allentown, Pa., has developed two 30-kgate, 0.9- μm CMOS chips. They interface the European 140-Mbit/s CEPT-4 network with 156-Mbit/s SDH-based networks for 2.5-Gbit/s transmission over SONET. One chip converts incoming CEPT-4 signals into STM-1 (Synchronous Transfer Mode) signals. The other device performs the reverse operation. A second SONET-related paper by Transwitch Corp., Shelton, Conn., introduces a single-chip overhead terminator that provides universal access to SONET/SDH signals. The 1- μm CMOS device contains 220,000 transistors and measures 430 by 430 mils.

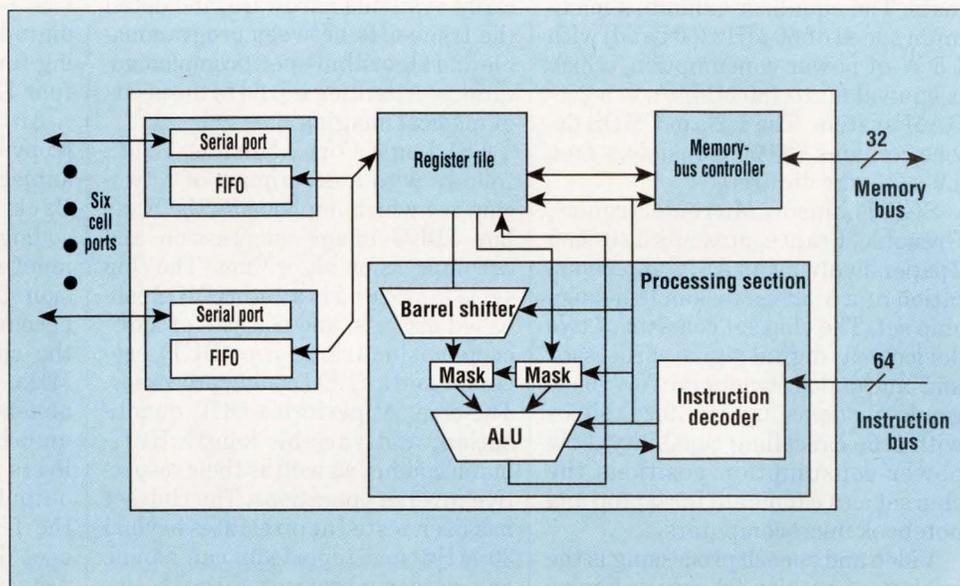
Yet another STM signal-handling device is describe in session 29 by Swindon Silicon Systems Ltd., Swindon, England. The company developed a silicon bipolar three-chip set for multiplexing, demultiplexing, and routing STM 16 data channels at 2.5 Gbits/s, per CCITT Recommendation 709. The chip set consists of a

16:1 multiplexer, a demultiplexer functioning as a 16-bit serial-to-parallel converter, and a 12-by-12 crosspoint switch. This session also includes a report on a single-chip ISDN U-interface transceiver, jointly developed by AT&T Bell Laboratories engineers from facilities in Murray Hill, N.J.; Naperville, Ill.; and Whippany, N.J. The 44.4-mm², 0.9- μ m CMOS chip can drive five miles of AWG 26 cable with 260 mW.

Two session 23 papers describe devices used at the physical fiber interface. Stanford Univ., Stanford, Calif., reports on an integrated 16-GHz GaAs and silicon bipolar optical receiver with an equivalent input noise of less than 3 pA/ $\sqrt{\text{Hz}}$. The presentation focuses on device-processing sequences used to integrate the GaAs and silicon bipolar structures. In the same session, researchers at Katholieke Univ., Leuven, Belgium, describe an integrated 150-Mbit/s LED driver and p-i-n receiver for optical communication. The 0.8- μ m CMOS chip exhibits a 10⁴ ratio between the 60-mA LED-driver modulation current and the 10- μ A p-i-n-receiver modulation current. The 1.3-by-0.6-mm chip draws 27 mA from a 5-V supply.

Most papers in session 14 apply to broadband communications systems employing ATM (Asynchronous Transfer Mode) packet switching. A joint presentation by AT&T Bell Labs, Holmdel, N.J., and Silicon Design Experts, Lakewood, N.J., reveals a 32-by-32, 200-MHz Batcher-banyan fabric chip for ATM switching. The 0.9- μ m CMOS device processes 11 million packets/s, performs 2.6 trillion bit manipulations/s, and has a total data throughput of over 5 Gbits/s. The 12-by-12-mm die contains 380,000 devices and dissipates 7.5 W at 200 MHz.

Designers at Centro Studi e Laborati Telecomunicazioni, Torino, Italy, introduce a 4-by-4 shared-memory ATM switching element that operates on four incoming 622-Mbit/s



3. THE DATA PATH of Bellcore's ATM processor for B-channel ISDN service is optimized for bit-field processing. A single instruction allows shift and mask operations on two source operands. The destination is written through a write-enable bit mask. Separate instruction and memory buses decouple the memory-bus controller from the execution of instructions. Memory can be loaded without blocking the processor until a result is needed. This allows a 53-byte ATM cell to be processed in 2 μ s.

ATM data streams. Output data is delivered through four 8-bit parallel ports at the same speed, for a total throughput of 5.8 Gbits/s. The 9.2-by-9.2-mm device contains 350,000 transistors, dissipates 1 W at a frequency of 90 MHz, and operates on a 90.68-MHz clock.

Future B-channel ISDN systems must support a range of services, from high-bit-rate, delay-critical (such as HDTV) to low-rate, delay-insensitive (such as telemetry). Researchers at Telecom Australia Laboratories, Clayton and Melbourne, Australia, have devised an experimental three-chip set. Detailed in session 14, the set consists of a sorter chip, an Omega switch, and an output-queue controller chip. The three chips form the core of a 32-by-32, 50-Mbit/s output-buffered, self-routing ATM switch fabric with multiple levels of cell delay and discard priority. The 2- μ m CMOS chip set operates at a rate of 50 Mbits/s for a throughput of 1.6 Gbits/s.

B-channel ISDN service is also the target application for a 50-MIPS cell processor divulged by Bellcore, Morristown, N.J., in the same session. This device is a RISC processor with

a custom instruction set for performing admission control, header processing, and other ATM cell-processing functions (Fig. 3). Fabricated with a 1- μ m, double-metal CMOS process, the 9-by-9.5-mm die contains 180,000 transistors. All instructions are performed in a single cycle of 20-ns minimum duration.

In session 14, a joint presentation by BNR Europe, Harlow, U.K., and SGS-Thomson, Milan, Italy, describes a prototype internetworking ASIC for protocol conversion between SDH-based networks and ATM networks. Operating on a 19.44-MHz clock, the 1.2- μ m CMOS chip with 300,000 transistors has an 8-bit parallel architecture. With a built-in cell-based protocol, data and control cells can share the same transmission media. The chip measures 11.07 by 11.85 mm.

In session 29, the University of California at Los Angeles, describes an interesting development for modem applications. Its decision-feedback equalizer chip can be programmed to equalize QPSK (quadrature phase-shift keying), 16-QAM (quadrature amplitude modulation), 64-QAM, or 256-QAM signal for-

mats. The equalizer exhibits a maximum speed of 60 MHz (60 baud) with 1.5 W of power consumption, which is equivalent to 480 Mbits/s in a 256-QAM system. The 1.2- μ m CMOS device contains 70,000 transistors on a 4.9-x-7.0-mm die area.

SGS-Thomson Microelectronics, Grenoble, France, presents a session 2 paper involving an ASIC implementation of a V.32bis/facsimile modem chip set. The chip set consists of two devices: a digital-signal processor and an analog front-end for voice-grade modems up to 19.2 kbits/s with echo-cancelling capability. Low power consumption positions the chip set as a candidate for laptop and notebook microcomputers.

Video and speech processing is the subject of session 26, which begins with a review of video-compression options by General Electric, Schenectady, N.Y. The authors survey standards, algorithms, and commer-

cially available hardware, and detail the trade-offs between programmable and algorithm-specific implementations. Attention is paid to the needs of medical imaging.

LSI Logic Corp., Milpitas, Calif., follows with a description of a two-chip set which implements the baseline JPEG image-compression and decompression algorithms. The chip set is fabricated in a 1- μ m CMOS cell-based process, and consists of a discrete-cosine-transform (DCT) processor and a JPEG coding processor. The chip set performs DCT, quantization, and variable-length Huffman coding, as well as their respective inverse operations. The chip set has been tested at pixel rates beyond 30 MHz, and reportedly can handle any data-compression ratio. A second LSI Logic paper describes a 31,000-gate inverse-DCT processor for HDTV applications. Operating at 40 MHz, the CMOS array-based de-

vice performs the 8-by-8 IDCT for digital HDTV decoders by converting four 14-bit DCT coefficients into four 11-bit pixel values every cycle.

An experimental high-speed entropy decoder chip for HDTV is the subject of a paper by Bellcore, Red Bank, N.J., in session 26. Entropy coding exploits the statistics of the input data to get lossless compression. Consisting of a variable-length decoder and a run-length decoder, the chip has been simulated at 75 MHz. At this frequency, the variable-length decoder handles a maximum input rate of 1.2 Gbits/s and delivers a constant 600 Mbits/s at the output. Developed to demonstrate the feasibility of real-time entropy decoding at HDTV rates, it will be used in a 52-MHz research prototype HDTV codec.

Session 26 also offers a simplified solution for cancelling video ghost images, as presented in a joint paper from TLW Inc., Burlington, Mass., and Philips Laboratories, Briarcliff Manor, N.Y. Where prior filter solutions required up to ten VLSI chips, the authors describe a 450,000-transistor CMOS chip that contains a configurable IIR and FIR filter. A compact digital-filter stage operating at a 14.32-MHz pixel rate contains 180 programmable taps. The 56.25-mm² chip operates from both 3.3- and 5-V supplies, and consumes 1 W at 3.3 V.

Another paper in this session describes a VLSI chip set for Chinese speech recognition. Researchers at the National Taiwan Univ., Taipei, have designed a 25-MHz, 1.2- μ m CMOS two-chip set that implements a Viterbi processor and a linear-predictive-coding processor. These two parts, which perform the computational-intensive tasks required for speech-syllable recognition, are teamed with a tone recognizer implemented with a Texas Instruments TMS320C25 digital-signal processor. The intended application is in a PC add-on circuit board. □

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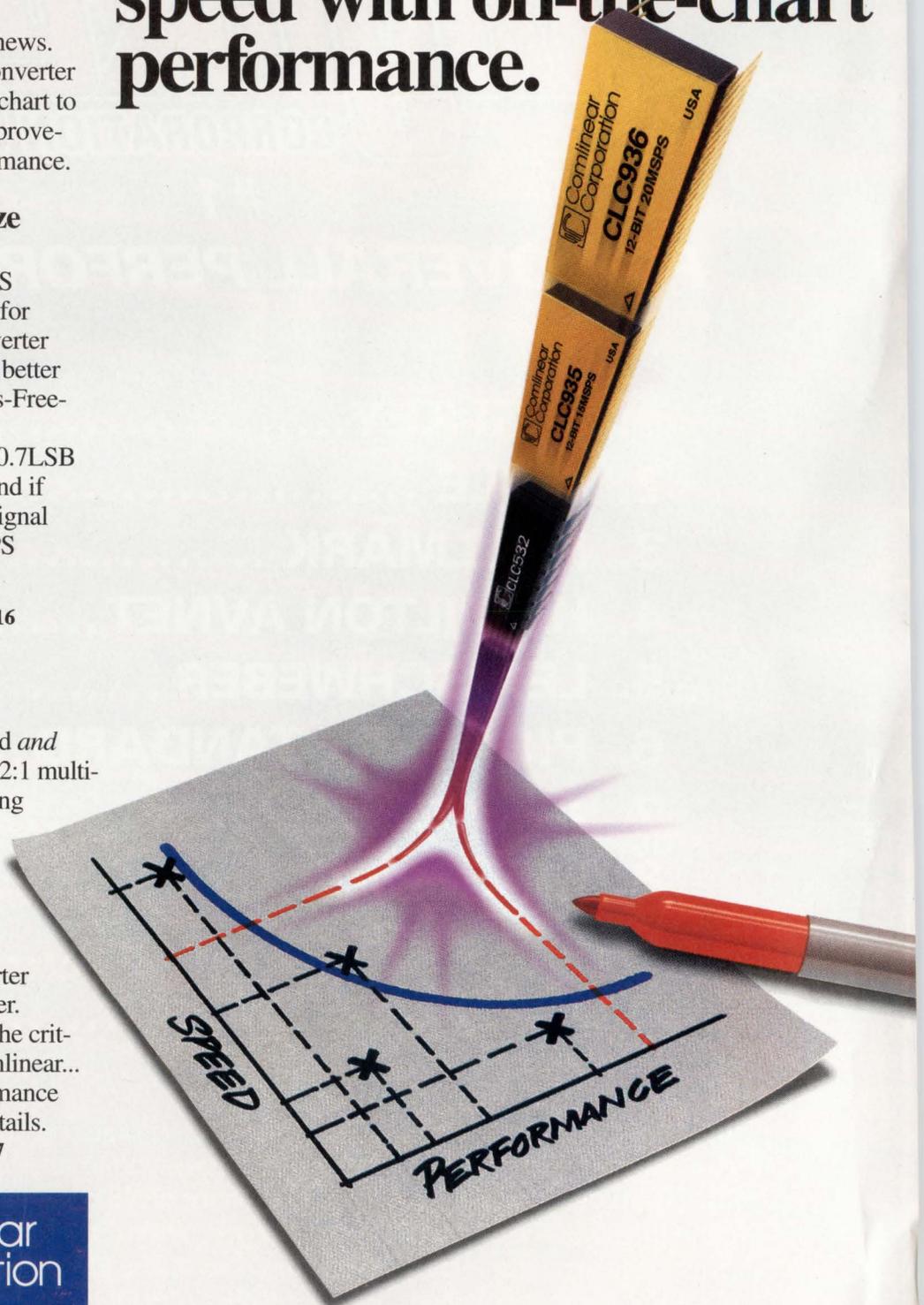
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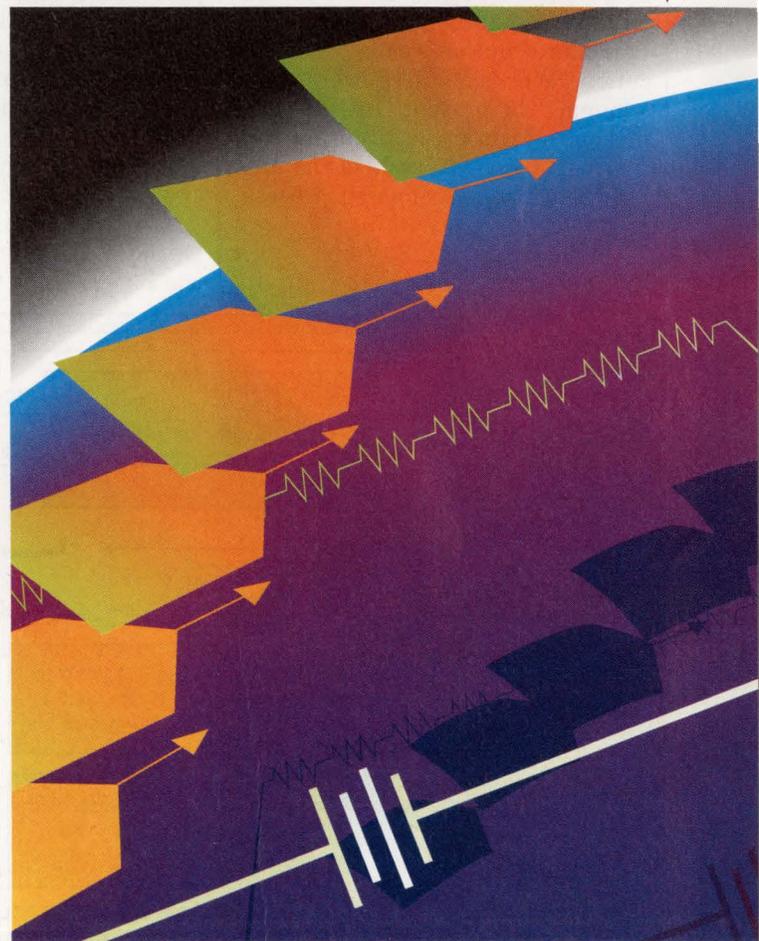
IC'S 8, 14-BIT DACs SHARE RESISTOR LADDER FOR MSBs

FRANK GOODENOUGH

Any analog IC or system circuit designer who has tried to design a digital-to-analog converter is in for a surprise upon examining the MP7610/MP7611 DACs from Micro Power Systems. Multiple DACs sharing a single resistor network for one or more most-significant bits is, at first glance, "obvious." In Micro Power's converters, the eight, 14-bit DACs on each IC share a 15-tap resistor ladder to create the four MSBs. That is, a 15-channel analog multiplexer, functionally in the analog section of each DAC, can select the voltage at any one of the ladder's 15 taps. If each DAC receives the same word, all will be tied to the same tap. A separate 10-bit, R-2R DAC provides the remaining 10 least-significant bits for each of the eight DACs (*Fig. 1*). In many applications, the single IC can replace over 20 active devices. However, its concept is anything but obvious.

Both the MP7610 and the MP7611 contain eight, 14-bit voltage-output DACs. The former employs a serial digital I/O, and is squeezed into a 28-pin DIP or a wide-body SOIC. The latter has a 14-bit parallel I/O that takes additional pins, hence it comes in a 44-pin PQFP or PGA. Both use a pair of octal 12-bit DACs, the MP7612 and MP7613, in their architectures. These 12-bit DACs also use a common ladder for the four MSBs, but only 8 bits are required for the R-2R DACs. All four ICs are built on a proprietary 3- μ m, refractory-metal-gate biCMOS process that incorporates laser-trimmable thin-film resistors.

Applications for these ICs are numerous, including pin electronics for IC, pc-board, and system automatic test equipment. The de-



vices can trim and calibrate systems and subsystems of all kinds, as well as create set points in process-control systems. The serial I/O devices in particular lend themselves to process-control and other industrial systems, as they simplify the job of creating an optically isolated digital interface.

The company prefers to walk a little before running with their specifications because these ICs represent a completely new design.

OCTAL 14-BIT VOLTAGE-OUTPUT DACs

The firm specifies just 12-bit accuracy. In other words, typical integral and differential nonlinearity (INL and DNL) of the 14- and 12-bit DACs are specified as ± 4 and ± 2 LSB, respectively. However, the DACs are better than 12-bit monotonic. Though laser-trimmable, the resistor networks in these first devices haven't been trimmed. The company believes 13-bit accuracy is possible (at room temperature) and is currently working on a trimming routine. In addition, if a demand is seen from customers (or potential customers), 14-bit-accurate devices will be developed. Moreover, the company believes extending the technique to 16-bit resolution is a matter of execution. When Micro Power starts trimming the present DACs, having just one network trim all eight DACs will increase yields and cut the time required for the trimming process, thus reducing costs.

Operating from ± 12 -V rails with a 5-V external reference, the outputs

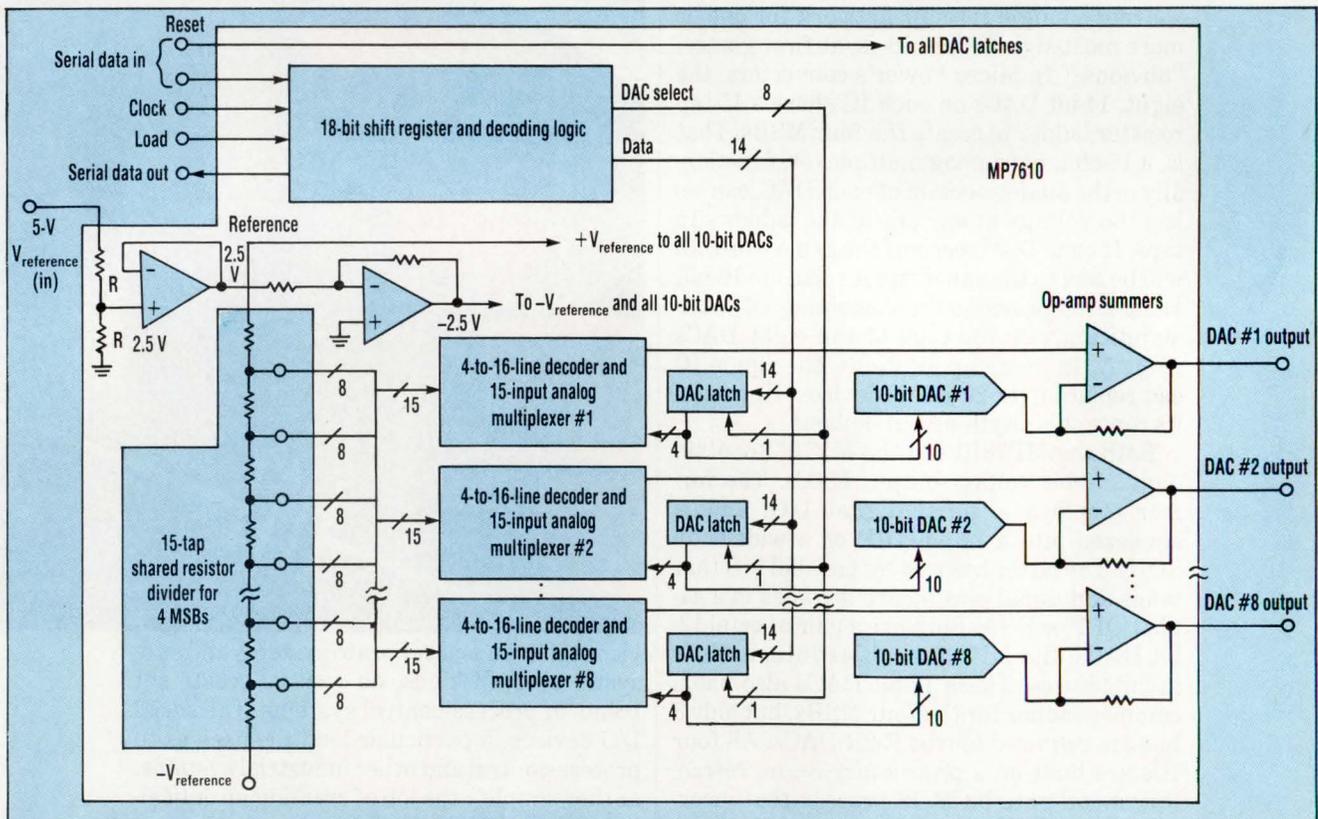
of all four DACs swing ± 10 V while sourcing and sinking 2 mA. To conserve power consumption, which is typically 320 mW, full-scale output settling time to within $\pm 1/2$ LSB has been set at a conservative 30 μ s. But that specification may well drop to 15 μ s. The eight DACs' common resistor network provides them with an uncommon feature: inherent matching of INL, DNL, and gain. While DAC-to-DAC matching is specified as 0.05% of full scale, significantly better performance has been obtained. And like settling time, the specification can be expected to improve. Matching reduces the calibration time, as well as calibration-circuit complexity, of any multi-DAC application employing system or DAC calibration. One calibration does the job for all eight DACs. A lookup-table memory is reduced in size by a factor of eight.

A major application for these DACs is in systems that currently use a single DAC to continuously up-

date eight sample-and-hold amplifiers (SHAs) with inputs from a host processor. The octal DACs eliminate SHA errors, such as pedestal, droop, and digital control-signal feedthrough. In addition, the chip's analog and digital ground lines are completely isolated from each other, virtually eliminating the possibility of digital noise getting into the analog circuits.

DAISY CHAINS

The MP7610 is equipped with a standard, three-wire, serial microprocessor interface with Data, Clock, and Load command lines (Fig. 1, again). A serial-data-out (SDO) pin is provided so that multiple MP7610s can be daisy-chained. In a system using multiple MP7610s, the SDO signal is fed to the serial-data-in (SDI) pin of the next IC in the chain. The SDO pin of the last MP7610 in the chain can be fed back to the processor for error checking before the Load command is transmitted. The



1. THE MOST-SIGNIFICANT BITS in the MP7610 octal DAC are derived from the 4 bits of the 14-bit data word that are fed to each of the 8 DACs. The 4 bits select one of the 15 taps on the resistive voltage divider. The multiplexer's output is summed in an op amp with the output of a 10-bit DAC that provides the LSBs.

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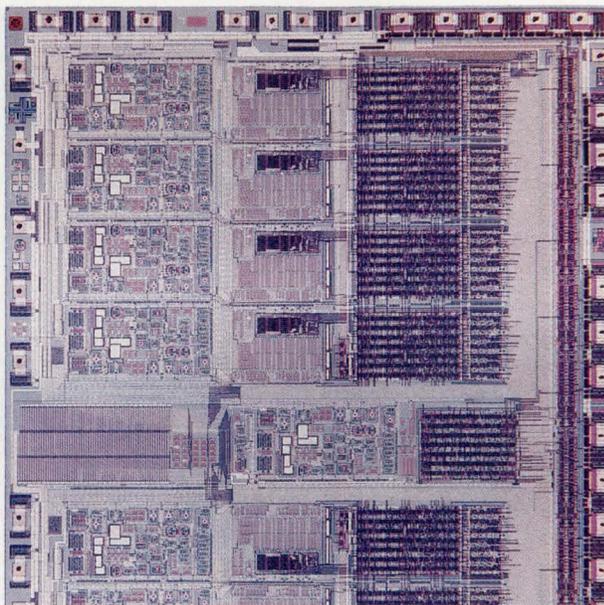
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OCTAL 14-BIT VOLTAGE-OUTPUT DACs

14-bit DACs use an 18-bit input word consisting of 4 bits to address a particular DAC (of which only 3 are used), and 14-bit data. A reset input to all of the DAC latches brings each analog output to 0 V, regardless of the digital input word. In addition, the serial port is equipped with a disabling SDI-and-clock latch that isolates an unaddressed IC from noise on the clock or data lines.

Alternatively, multiple serial-I/O DACs can be connected in a parallel configuration in which all of the MP7610s share a common SDI bus, but each is controlled by a separate Load command. Because the SDO output is tristated when the Load signal is low, a single SDO line can still return the



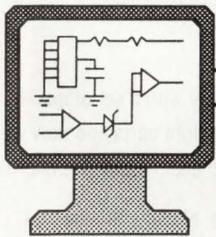
2. EIGHT 14-BIT DACs are crammed onto this 70,000-mil² chip. The secret behind this octal DAC's creation (a little more than one-half the chip is shown) is a 15-tap resistive ladder that's shared by all 8 DACs to create their 4 MSBs.

data signal to the host. The parallel approach can also use an off-chip address decoder to control the Load command.

The MP7611's 14-line parallel interface contains double-buffered latches and a readback line from the first bank of latches for each DAC. Double buffering permits single-cycle, double-cycle, or transparent-mode data writing. A two-bit address input selects the DAC to be loaded. The readback feature allows software to control the system-interconnect so that it can check the data words in the latches. Data is read back from the first latch bank, rather than the second, to isolate the individual DAC outputs from any transient effects caused by readback. Data to each DAC can be up-

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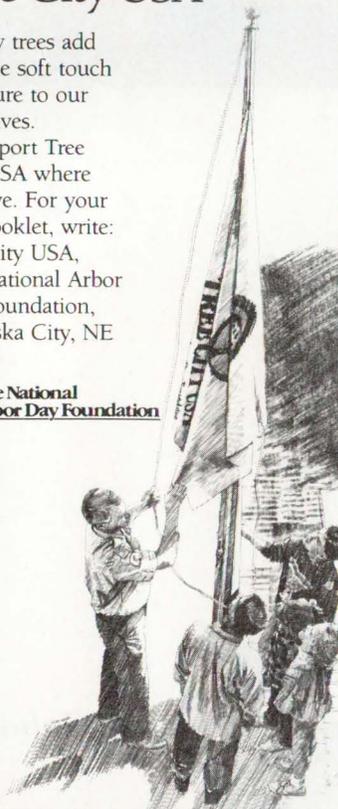
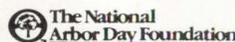
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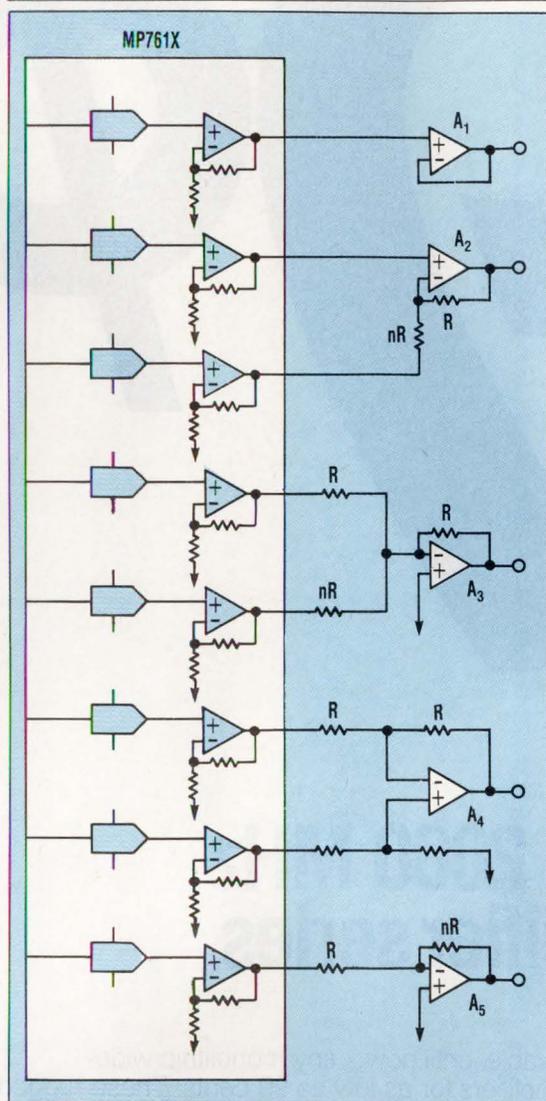
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OCTAL 14-BIT VOLTAGE-OUTPUT DACs



3. WITH THE AID OF external op amps, the current (A_1) or voltage (A_2) output of the MP761X family of 14-bit DACs can be increased. Or their outputs can be summed (A_2 and A_3) to increase resolution.

dated selectively, or all eight DACs can be updated simultaneously. A pair of reset inputs enable the output of selected DACs, or of all eight DACs, to be set to zero.

On the MP7611, the $-V_{\text{reference}}$ is brought out to a pin that can be used as a checkpoint for the on-chip reference circuitry. A capacitor can also be hung on the pin to reduce noise.

Although the op amps are built with bipolar transistors, their changing bias currents in the divider (via the multiplexer) don't cause errors because the divider's total resistance is only 700Ω . The result is a maxi-

mum equivalent Thévenin's source resistance of 350Ω at the midpoint of the divider.

In the chips' layout, the digital I/O runs the length of the right-hand edge, and the four MSBs are developed in the precision center section (Fig. 2). Having all of the precision circuitry in one small section of the die significantly increases yield. Four of the 10-bit DACs lie above the precision section and four below. Their thin-film R-2R networks lie in the center, digital circuitry is on the right, and output op amps are on the far left. Two pins provided for plus and minus supplies minimize the length of the chips' power buses.

By using a few external op amps and/or discrete transistors, the outputs of the eight DACs can create a variety of interesting circuits (Fig. 3). If more current is needed, power buffer A_1 can be added. And the good channel-to-channel MSB matching enables higher-order DACs to be created by combining the outputs of two of the ICs' DACs (A_2 and A_3). The channel containing the resistor nR produces the LSBs, and its mate creates the MSBs. To operate in a noisy environment, A_2 and A_3 can be combined in differential circuit A_4 . For a higher output, gain A_5 can be added. □

PRICE AND AVAILABILITY

The MP7610, 11, 12, and 13 sell for \$65.45, \$66.94, \$59.50, and \$60.82 each, respectively, in 1000-unit quantities. All units are rated for operation from -40 to $+85^\circ\text{C}$.

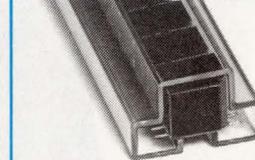
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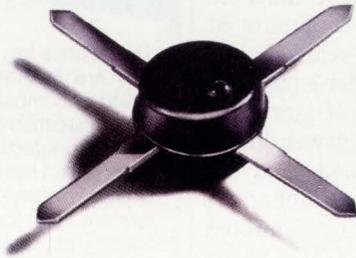
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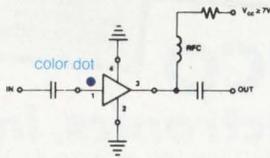
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MAR-2	DC-2000	13	12.5	11	8.5	+3	6.5	1.35	(25)
MAR-3	DC-2000	13	12.5	10.5	8.0	+8□	6.0	1.45	(25)
MAR-4	DC-1000	8.2	8.0	—	7.0	+11	7.0	1.55	(25)
MAR-6	DC-2000	20	16	11	9	0	2.8	1.29	(25)
MAR-7	DC-2000	13.5	12.5	10.5	8.5	+3	5.0	1.75	(25)
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Efficiency is important in power-supply design, whether it's in the interest of extending battery life, or because there simply isn't room in the system for heat sinks. For switching regulators, the key to efficiency is to minimize switching losses.

A 5-V regulator that requires no heat sinking can be built using the LT1158, which is a half-bridge, n-channel, power-MOSFET driver (see the figure).

The regulator delivers efficiency better than 91% with a 12-V input and 2-A output current. Typically, the LT1158 is most often used in pulse-width-modulated systems, such as motor controllers.

But in this case, it's the central element in a constant-off-time, current-mode switcher. The main switching device is MOSFET Q1, while synchronous switch Q2 replaces the Schottky diode typical of step-down regulators. Each MOSFET dissipates less than 400 mW at a 3-A output, which eliminates the need for heat sinking.

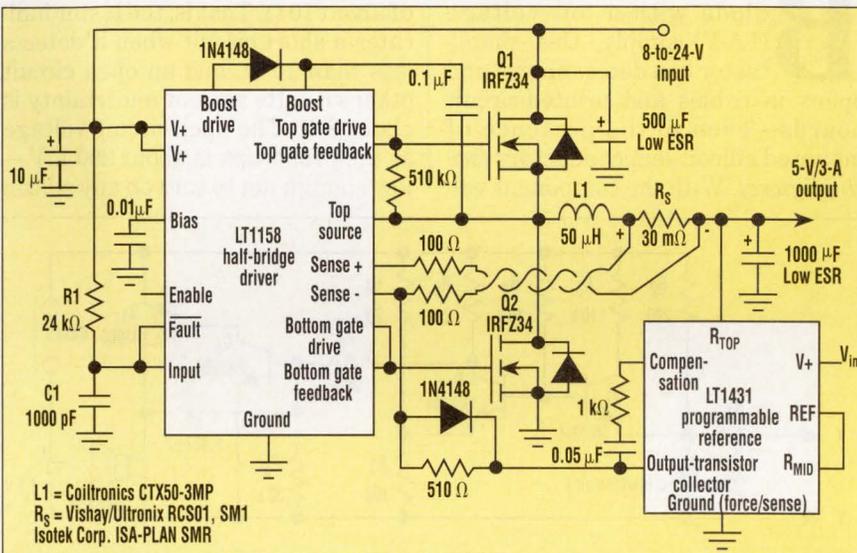
The LT1158 monitors the current in inductor L1 by means of the voltage drop across current-shunt resistor R_S .

Normally, the LT1158 Fault pin would not conduct until the internal 110-mV threshold was reached. But the LT1431 programmable voltage reference adds a loop that senses the output voltage and reduces the fault-conduction threshold to conform to the required load current.

During each switch On cycle (Q1 on and Q2 off), the current in L1 ramps through the threshold set by the LT1431 reference, causing the LT1158 driver's Fault pin to conduct and fully discharge C1. This action pulls the input pin low, thereby initiating the switch Off cycle (Q1 off and Q2 on).

The constant-off-time topology produces a constant inductor ripple current of 800 mA pk-pk and an operating frequency that varies from about 45 kHz to 100 kHz over the 8-to-24-V input range.

If the regulator output is shorted to ground, the LT1431 collector pin



L1 = Coiltronics CTX50-3MP
 R_S = Vishay/Ultronic RCS01, SM1
Isotek Corp. ISA-PLAN SMR

HIGH EFFICIENCY is obtained by synchronously switching two power MOSFETs in a step-down switching regulator. The LT1431 voltage reference combines with the LT1158 half-bridge driver to form a constant-off-time, current-mode loop.

The off time consists of two components. The first component is the time for the current in L1 to ramp down below the sense threshold, thereby releasing C1.

That's followed by the time for C1 to charge back up to the LT1158 input threshold (1.4 V), where the next switch On cycle starts. Variations in these two components with V_{in} tend to cancel each other, resulting in a stable off time of about 8 µs for the circuit shown.

turns off, enabling the LT1158 current sense to revert to normal operation. This yields a current-limit value of four amperes.

From a construction standpoint, the layout's most critical aspect is the routing of the sense leads to avoid coupling from L1. The printed-circuit traces must be run together at minimum spacing or a twisted pair should be used. Another important consideration is that a Kelvin connection is required at R_S .

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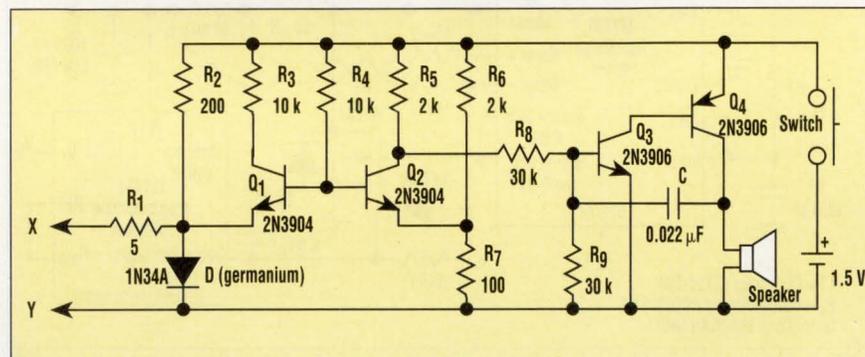
CIRCLE 522 TESTER FINDS SHORTS ON LOADED BOARDS

ALEXANDER L. BELOUSOV

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By combining a germanium diode with a low-voltage (1.5-V) supply, this simple tester can detect shorts and opens in cables and printed-circuit boards—even in the presence of mounted silicon semiconductors (see the figure). With the component val-

ues shown, the tester has a threshold of about 10 Ω . That is, the tester indicates a short circuit when it detects less than 10 Ω , and an open circuit otherwise. Its zone of uncertainty is about 2 Ω . The open-circuit voltage at the probe tips is about 200 mV—low enough not to turn on any silicon



TO FIND SHORTS and opens on boards loaded with silicon components, this test circuit keeps its probe voltage below about 200 mV, low enough to ensure that silicon devices aren't turned on. The diode (D) is a germanium device.

devices. If the probe tips are shorted together, the current that flows will be less than 8 mA.

Transistors Q_1 and Q_2 , together with resistors R_1 through R_7 , make up the input balancing stage, which senses the resistance between points X and Y.

The input stage is essentially a bridge, consisting of R_1 , R_2 , R_6 , R_7 , and the resistance between X and Y.

Transistors Q_3 and Q_4 and their associated passive components form a buzzer, which sounds when the tester detects a short. The buzzer is controlled by the output from Q_2 . When the input resistance is high (more than about 10 Ω), Q_2 turns on, so its collector potential is close to ground, and the buzzer remains off.

When the input resistance is sufficiently low, Q_2 turns off, and the buzzer sounds. The frequency of the sound, which is about 1000 Hz, can be adjusted by varying the value of capacitor (C).

Although the tester calls for a 1.5-V supply, it will continue to function even when that voltage drops below 1.0 V. If desired, the input resistance threshold can be varied by changing resistor R_1 or R_2 . □

CIRCLE 523 BOOTSTRAP CIRCUIT CUTS DISTORTION

WALT JUNG

Analog Devices Inc., 1 Technology Way, Norwood, MA 02062-9106; (617) 329-4700.

Standard-process junction-isolated FETs are popular items for IC op amps because they generally incur few dc errors and offer good ac performance. For example, total harmonic distortion (THD) can be as low as 0.001% (10 ppm) over the audio range.

But the fidelity of high-source-impedance, JFET op-amp circuits drops quickly as distortion rises with an increasing rate of change in the input signal. Fortunately, this distortion can be significantly reduced by using the op amp in a bootstrap circuit configuration.

The distortion problem arises from the nonlinearity of the capacitance at the JFET's two inputs. Typically, JFETs consist of a pair of differential p-channel FETs at the input and npn/pnp bipolar transistors for the remaining stages. The junction isolation is provided by isolation "wells" for the differential FET pair. These wells create a parasitic substrate capacitance of about 3 to 5 pF at the inputs.

The parasitic capacitance is nonlinear with the applied common-mode voltage, so it varies instantaneously with an ac input. When such an op

amp acts as a follower with high source impedance, it can generate excessive THD, which is seen as a 6-dB/octave rise in second-harmonic distortion with a fixed-level frequency sweep.

Bootstrapping reduces the effects of the capacitance. The bootstrap circuit is a second feedback divider referred to the negative supply that feeds back a signal to the V- pin, pin 4 (Fig. 1). When done properly, bootstrapping can cut capacitance-related distortion to below the residual noise level.

In the example circuit, U_1 , an AD744, is loaded only by the high-impedance input (the positive input) of U_2 , so U_1 provides virtually zero drive current.

This arrangement enhances the overall load-dependent linearity as well as the bootstrapping.

Unity-gain follower stage U_2 , an



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It is a relationship which has grown through broad-scale sharing of information and close cooperation in the development of production, testing and quality control procedures.

Today, many of the resistors supplied to Fluke are on a ship-to-stock basis. They are guided by mutually-agreed-upon quality

procedures, including statistical process control.

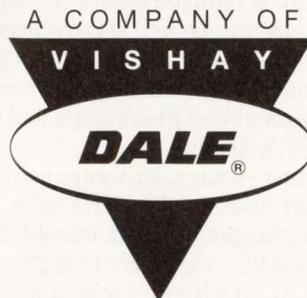
In addition, Fluke's "Aim For Excellence" program is used to provide guidelines for continual improvement through quarterly review and rating of plant-by-plant performance in quality, engineering support, on-time delivery and overall service.

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In addition, Dale's Norfolk, Nebraska, Metal Film Division has worked closely with Fluke in development of special resistors for protection of meter input circuitry. These designs demand precise response—requiring fusing under certain voltage parameters, and ability to withstand heavy pulses under others.

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For more information on how commitment to effective partnering can benefit your operation, please contact Joe Matejka, Vice President, Quality Assurance, Dale Electronics, Inc., 1122 23rd Street, Columbus, Nebraska 68601-3647. Phone 402-563-6511. Fax 402-563-6418.



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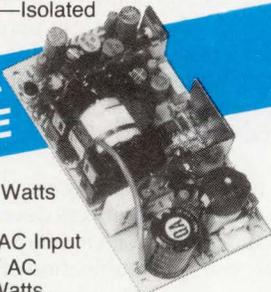
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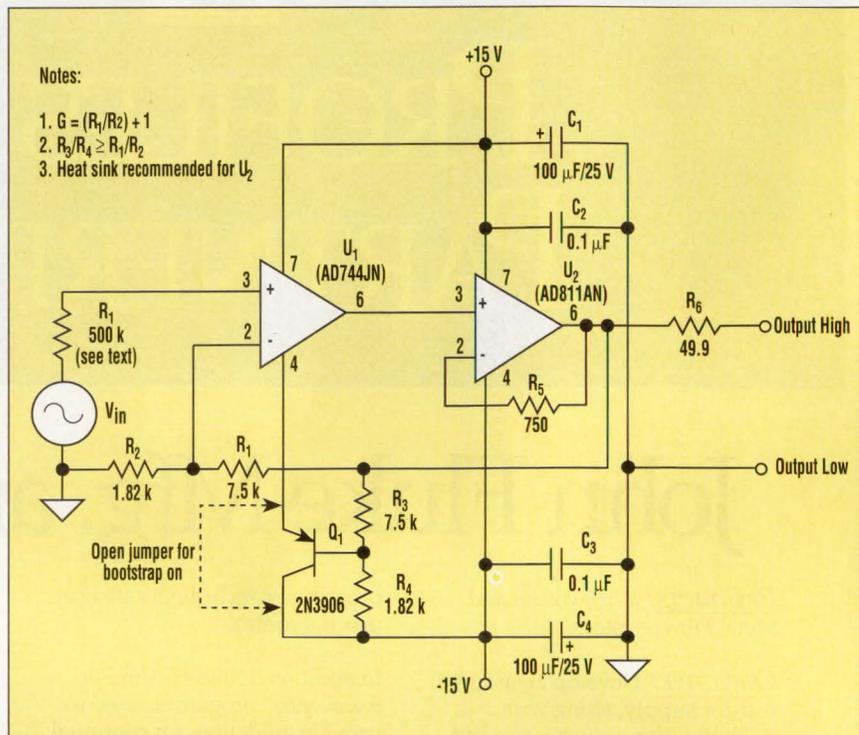
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IDEAS FOR DESIGN



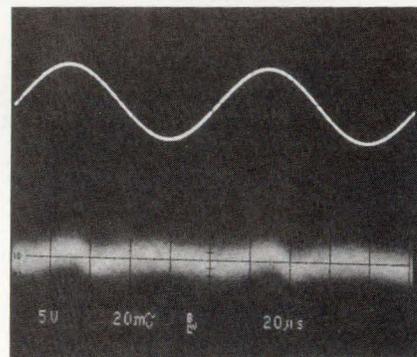
1. A SECOND FEEDBACK DIVIDER in a JFET op-amp circuit (R_3 and R_4) bootstraps U_1 's substrate. As a result, the distortion caused by nonlinear capacitance is reduced.

AD811AN, primarily supplies a 100-mA output drive and good linearity into 600- Ω (or lower) loads.

The circuit's overall voltage gain, G , is set by R_1 and R_2 , just as in a conventional noninverting amplifier. For the bootstrap divider, the ratio of R_3/R_4 must be the same or higher than R_1/R_2 . The values in the example deliver a gain of 5.12 (very low gains aren't recommended because they reduce dynamic range).

The bootstrap drives U_1 's substrate with a signal equal to that at the positive input. As a result, ac voltage is reduced across the nonlinear capacitance and there's less distortion. The bootstrapping will work without U_2 , but the distortion reduction won't be as great and it will vary with U_1 's loading.

In tests with ± 15 -V supplies and a 500-k Ω source, the THD of a non-bootstrapped circuit varied from about 0.01% at 1 kHz to 0.2% at 20 kHz. At 10 kHz and with a 3-V rms output from U_2 , THD was 0.1%. But with the bootstrap, the distortion at 10 kHz dropped by an order of magnitude, essentially disappearing into the residual noise (Fig. 2).

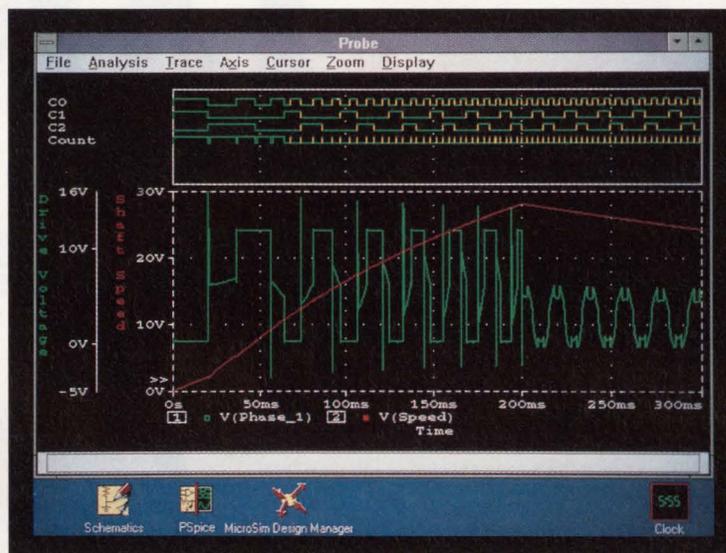


2. THE DISTORTION in a bootstrapped JFET op-amp circuit was cut by an order of magnitude, essentially fading into the residual noise (lower trace). The distortion analyzer was set to a full-scale range of 0.03%

The principles behind this distortion mechanism apply to virtually all JFET input op amps, regardless of source. Junction-isolated bipolar op amps can also exhibit the phenomenon and thus may benefit from bootstrapping.

But unlike JFET amps, bipolar types aren't as likely to be used with high source impedances, where this distortion is a problem. □

Think Universal Analog and Digital Circuit Simulator!



Analog and digital waveforms with multiple Y axes

Think PSpice!!

If you're not using PSpice, then you're working with half a simulator! Why? Most circuit simulators support either analog-only or digital-only circuits. Those simulators claiming mixed-mode support are typically comprised of separate analog and digital programs that are glued together. With PSpice, the analog and digital simulation algorithms are fully integrated within the same program. Think of the benefits!

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Circuit definition is as simple as creating one schematic or netlist of analog and digital device declarations and connections. Choose from over 4,000 analog and 1,700 digital off-the-shelf parts available in our standard libraries, or create your own. Interfaces between analog and digital parts are handled automatically by PSpice.

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PSpice uses an event-driven logic processing technique supporting 5 logic levels, 64 output strengths, and timing modeling, including worst-case timing simulation. Logic states and propagation delays are computed quickly and accurately. By using efficient digital primitives rather than cumbersome macromodels composed of analog parts, PSpice simulates at speeds that are orders of magnitude faster than simulators using macromodel definitions of digital devices.

Paving the Way to Universal Circuit Design

PSpice is now an integrated part of our **Design Center** circuit design environment. Whether your circuit is analog-only, digital-only, or mixed analog and digital, the **Design Center** will provide you with a unified environment for schematic capture (selected platforms), simulation with PSpice, and graphical analysis of the waveform results. To find out more about PSpice and the **Design Center**, call us toll free at (800) 245-3022 or FAX at (714) 455-0554.



MicroSim Corporation

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CIRCLE 116 FOR U.S. RESPONSE

CIRCLE 117 FOR RESPONSE OUTSIDE THE U.S.

QUICKLOOK

EDITED BY SHERRIE VAN TYLE

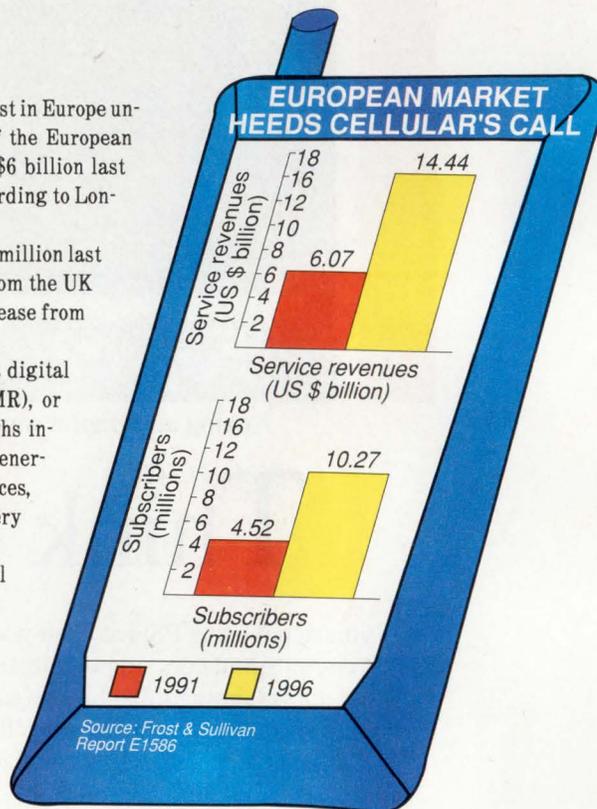
MARKET FACTS

Sales of cellular phones and equipment are expected to stay robust in Europe until the year 2000—the only damper would be a worsening of the European recession. Revenues from cellular services, which topped US\$6 billion last year, should more than double, to US\$14.4 billion by 1996, according to London market researchers Frost & Sullivan International.

Fueling this growth are an increasing number of subscribers, from 4.52 million last year, to more than 10 million by 1996, with much of that growth coming from the UK and Nordic countries. Shipments of cellular terminals are expected to increase from 1.35 million last year to 2.04 million in 1996.

Cellular is expected to compete with other mobile technologies such as digital European cordless telephony (DECT), public access mobile radio (PAMR), or personal communications networks (PCN). Recent technical breakthroughs include widespread introduction of pocket-size voice terminals, the start of Generali Mobile (GSM) digital services, launch of value-added services, and development of small-cell technology that makes possible the use of very low-power hand portables.

Market growth could be slowed by such issues as prices for terminal products and tariffs, which mean that average calls cost 8 to 12 times the equivalent cost of the public switched telephone network (PSTN). The UK, the largest market last year, will be overtaken by Germany by 1996, because of its higher tariffs, larger population base, and brisker economic activity. Still, the market researcher points to the UK as an innovator in services and competitive activity. Italy, where a new analog network was recently installed, is now the fourth largest market in Europe, behind the UK, Germany, and Sweden.



QUICK REVIEWS

The *PHIGS Programming Manual* gives an introduction to three-dimensional Phigs and Phigs Plus programming. By Tom Gaskins, the manual documents Phigs and Phigs Plus graphics standards, including output primitives, attributes, color, and structures. With the book, users can begin to write Phigs programs and use Phigs within the X Window environment, including Xlib, Motif, OLIT, and XView. The book takes as its starting point the PEX Sample Implementation for commercial products. The manual, which has 200 figures, has a programmer's guide, describes all Phigs and Phigs Plus functions, and explains viewing, lighting, and shading, with code examples. It includes the DIS ISO C binding, which is closest to the coming ISO standard. Designing and writing graphics software since 1981, Gaskins was responsible for the design and implementation of the PEX-SI Phigs library. A companion reference manual is in the works. The 968-page book is published by O'Reilly & Associates Inc., 103 Morris St., Suite A, Sebastopol, CA 95472; (800) 338-6887 or (707) 829-0515; fax 829-0104. Softcover price is \$42.95, hardcover, \$52.95 (ISBN 0-937175-85-4). CIRCLE 451

QUICK NEWS: EDUCATION

Battery selection in product design will be covered in a course from the University of Wisconsin-Madison, Department of Engineering Professional Development on May 4-6, 1992. The course will present detailed information on the technology, characteristics, selection criteria, and environmental considerations for primary and rechargeable batteries. Contact Harold Green, Department of Engineering Professional Development, University of Wisconsin-Madison, 432 N. Lake St., Madison, WI 53706; (800) 462-0876 or (608) 262-2061; fax 263-3160. CIRCLE 452

A four-hour course on accelerated fault simulation costs \$50 for preregistered attendees. The course, given in various U.S. cities through May 1992 by Zycad, covers physical and circuit defects and how to test for them, fault models, fault-simulation algorithms, along with a description of various hardware and software tools. Contact Zycad, 1380 Willow Rd., Menlo Park, CA 94025-1516; (800) 243-7286; fax (415) 688-7575. CIRCLE 453

OFFERS YOU CAN'T REFUSE

Design Tool PLL2 Version 1.0 is patterned after the popular PLL3 tool. In PLL2 a designer has an interactive tool in developing 2nd order phase locked loop circuits. Dynamic Bode and transient plots show performance during design. Other parameters calculated include loop filter components, damping, noise, lock range, and lock time. PLL2 requires DOS 3.2, EGA display, and 256k of RAM. Price is \$35 plus \$3 shipping. Contact Software Innovations for Technology Enterprises (Swift), 955 Concord Ln., Hoffman Estates, IL 60195; (708) 776-2119. CIRCLE 454

Computer Modules' catalog describes the company's line of modules and boards. CMI works with design engineers who are creating first-of-a-kind systems by building boards or tailoring software to specific applications. Contact Computer Modules, 2350A Walsh Ave., Santa Clara, CA 95051; (408) 496-1881. CIRCLE 455

The latest issue of *Linear Technology* magazine is free from the company. The lead article gives advice on designing with the new LT1158 low-voltage, half-bridge N-channel Mosfet driver IC. Covered are Mosfet gate-voltage overstress, cross-conduction, or shoot-through currents, and output transients that go below ground or above the supply rail. A subscription to the semiannual magazine is free to analog designers. Contact the Marketing Department, Linear Technology Corp., 1630 McCarthy Blvd., Milpitas, CA 95035-7487; (800) 637-5545. CIRCLE 456

A free catalog describes a line of telemetering products, which includes voltage-controlled oscillators, frequency-to-dc converters, amplifiers, analog signal isolators, pressure transducers, power supplies, wireless data links. Products are ruggedized and miniaturized, suitable for military and industrial applications. Contact Edward Y. Politi, Solid State Electronics Corp., 18646 Parthenia St., Northridge, CA 91324; (818) 993-8257; fax (818) 993-8259. CIRCLE 457

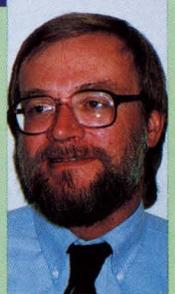
A free 52-page book describes the IXYS line of power IGBTs, Mosfets, diodes, thyristor modules, and power interface ICs. Each product family has a list of key performance characteristics, and package outlines. Contact IXYS Corp., 2355 Zanker Rd., San Jose, CA 95131-1109; (408) 435-1900. CIRCLE 458

DID YOU KNOW?

... that IBM, Boeing, and AT&T rank first, second, and third in leading a list of employers that engineering students would most like to work for. From a previous survey, General Electric falls one place into fourth position and Motorola jumps to fifth from 12th place. General Motors, NASA, Hewlett-Packard, Rockwell, and Hughes rank sixth through tenth. Also moving up in students' rankings when compared with previous surveys: Intel, Westinghouse, Exxon, Procter & Gamble, Bechtel, and Chevron.

Graduating Engineer magazine survey of 1671 students from 275 colleges

K M E T S K O R N E R



BY RON KMETOVICZ

President, Time to Market Associates Inc.
Cupertino, Calif.; (408) 446-4458; fax (408) 253-6085

Most of new product development occurs in the me-too-with-a-twist cell of the product-classification matrix. To work here you should enjoy working with statistical information on markets; feel good about making the next product you're working on a bit better than the one it replaces; strive to minimize technological risk; fully appreciate that it's not so much what you do but how to project the image of what you do; thrive on being product and market competitive; and know that being late and possibly being out of business are about the same. This is the cell for the warrior.

Product development organizations that work in this cell face competent and severe competition. The primary reason for this is that just about everybody knows about the market and the products needed to capture market share—they know how much money is out there and they can see ways to grab a chunk of the money pie for themselves. Once financial information about markets becomes known, raw capitalism swings into action.

There are two ways to get into the me-too game—the very hard way and the hard way. The very hard way requires that you get there by developing products in one of the other three cells first and then drift to becoming a me-too contender—then the challenge becomes one of survival in the me-too environment. You could pioneer a market with a derivative or first of a kind offering and then begin turning out improved versions of these products as more knowledge is obtained from the market. Or your organization may have developed a leap-frog product concept that takes over an existing market, which then begins to age. Organizations that take this path often carry the burden of being too product and technology focused—a curse if your competition is predominantly market focused.

The hard way is to see the opportunity, which usually doesn't take too much intellect, and figure out how to buy into the action. Where barriers to entry can be removed by throwing money and talent at them, expect an attempt to capture market share to occur. The international new product development game gets played this way and many of our more mature industries are subject to attacks of this nature. Think through where the Japanese hit first and how they hit. Look at what the Koreans are doing today. What has AMD done to Intel?

To see one way to perform and win in this cell let's look at Hewlett-Packard's printer operations. The company set an excellent example of how to retain, or grow, market share in highly competitive market segments. First, consider HP's dominance in laser printers. HP had the first-of-a-kind offering in this area years ago. From that first LaserJet, there have been a whole host of me-too spinoffs. In fact, HP has been its own worst competitor—it kills off products before the competition gets the chance. The company knows that it costs far less to maintain and grow market share using this tactic than it would to reclaim lost market share! Second, HP used knowledge acquired from marketing laser printers to open a new market for InkJet printers. The first of a kind ThinkJet lead to the DeskJet, DeskWriter, and now to a next generation of color ink-based printers. To hold on to its lead, HP has rolled out a steady flow of new products. Most have been me-too's, showing the company can hit singles as well as anyone. But triples and home runs can happen at just about any moment. Smart money leaves these markets to HP!

WHAT'S NEW

NO MATTER HOW YOU LOOK AT IT, SHARP'S NEW PASSIVE COLOR DISPLAY REALLY SHINES.

Today's exploding growth in notebook computer sales is matched only by the almost dizzying array of improvements in compatible flat panel displays as manufacturers slim down, lighten up and improve the aesthetics of notebook compatible displays, while expanding screen size.

One of the latest breakthroughs from Sharp is a super-

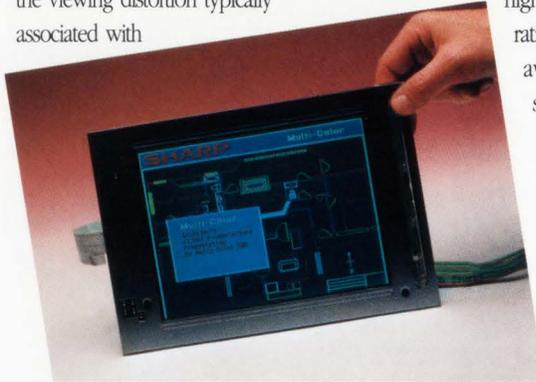
efficient passive matrix color display whose viewing quality leapfrogs anything previously available in its class.

The new LM64C031 passive color LCD provides the compact size, light weight and low power consumption of traditional passive displays — for about half the price of equivalent TFT color models. At the same time, thanks to

Sharp's exclusive three-dimensional film compensation process, the display achieves high brightness, superior color saturation and excellent contrast without the viewing distortion typically associated with

passive color displays. The product offers VGA-quality resolution, a response speed of 450 ms and contrast ratio of 13:1, with mouse-compatible speeds and even

higher contrast ratios to be available soon.



IMAGINATION AT WORK

MAKING IT BIG WITH TFT'S TAKES VISION AND ENORMOUS INVESTMENT.

Thanks to its early and continual investment in the manufacturing process, Sharp supplies some 70% of the world's thin film transistor (TFT) displays. TFT's compact, light, energy-efficient package provides color, clarity and full-motion video equal to or better than CRTs.

Sharp's new flagship TFT manufacturing plant in Tenri, Japan, incorporates the cutting edge in the "giant scale integration" tools required to produce virtually flawless matrices

of hundreds of thousands of transistors. New advancements in

photolithography, chemical vapor deposition and fusion-drawn glass continue to keep Sharp the quality leader in a market expected to grow to \$3.1 billion by 1995.



SHARP IN THE U.S.A.

SHARP: NOW A MAJOR U.S. MANUFACTURER.

Sharp has demonstrated an unprecedented

commitment to its U.S. customers by augmenting IC research and development activities at the company's new facility in Camas, Washington, with an

additional \$30 million investment in LCD production.

The first Japanese company with an LCD manufacturing operation in the U.S., Sharp

is now able to assure the fastest response and repair time possible, backed by the largest support team in the country.



COMING NEXT ISSUE: COLOR FLAT PANEL DISPLAYS. THEY'RE GETTING MORE COMPACT, MORE ENERGY EFFICIENT, WITH LARGER, CLEARER SCREENS. GET THE BIG PICTURE

ABOUT WHAT'S NEW IN TFT AND OTHER COLOR DISPLAYS IN THE NEXT ISSUE OF SHARP INSIGHTS.

SHARP
FROM SHARP MINDS COME SHARP PRODUCTS™

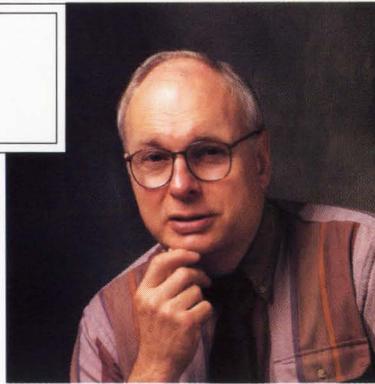
CIRCLE 144 FOR U.S. RESPONSE

CIRCLE 145 FOR RESPONSE OUTSIDE THE U.S.

FIRST PERSON

**THE CHIPS WHOSE
TIME HAS COME.**

**BY CHUCK HASTINGS
MARKETING/APPLICATIONS MANAGER
FIFO AND SPECIALTY MEMORIES
SHARP MICROELECTRONICS
TECHNOLOGIES, INC.**



If some of the gold-rush glamour has worn off the electronics field today, as compared to the entrepreneurial '80s, the same can't be said for the First-In, First-Out (FIFO) memories which serve as data buffers between systems operating at different speeds.

Why? Because these never were glamour parts in the first place — never the parts that show up in the block diagram on system designers' blackboards. As often as not, the lines in between these blocks tum into FIFOs.

Nevertheless, the "unglamorous" FIFOs have proven to be the right parts at the right time. In some ways, their evolution is the gating factor in the convergence of higher system performance with greater design efficiency.

The greater availability of "open system" components gives system designers the freedom to draw parts from off the shelf, instead of designing them from scratch. But it's the FIFOs which compensate for mismatches in data rates, word widths and synchronization between those high-profile intelligent engines.

Similarly, FIFOs serve the trend to greater partitioning

of design tasks among people and teams, expediting the eventual interfacing of subsystems and components simply and economically.

Ultimately, the measure of a FIFO like Sharp's new 36-bit bidirectional LH5420 — the first and only true system-level FIFO to date — is how little time, money, board space and special attention it gobbles up during the hardware development process.

As a low-profile supporting player, the feature-packed LH5420 is a huge success — proof that FIFOs are alive and well, and — given the decidedly less glamorous alternatives — just the stuff which the no-nonsense design environment of the '90s is meant to build on.

THE SHAPE OF THINGS TO COME

PRICELESS PREVIEWS.

The latest issue of Sharp's Memory Data Book includes several "sneak previews" of Sharp memory components now under development: a 32M Mask ROM, for example — the world's largest; a 1024 x 36 unidirectional FIFO with the most fully synchronous

feature set available; and a 20 ns Static RAM in a 64K x 18 configuration. For your free copy of the '91/'92 Memory

Data Book, or for other information about Sharp IC, Opto and LCD components, call your regional Sharp office listed at right.



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Camas, WA
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INSIGHTS

FROM SHARP



NEW 36-BIT FIFO MERGES MOST-ASKED-FOR FEATURES.

Variouly described as “data accordions” or “logical rubber bands,” FIFO (First-In, First-Out) memories serve as data buffers between different CPUs running at different speeds, or between controllers and their peripheral equipment. This data-rate-

matching capability provides an ideal thoroughfare between independent, intelligent processors of differing word widths and/or clock speeds.

Now, Sharp's new 36-bit synchronous, bidirectional LH5420

represents the evolution of FIFOs from byte-sized to system-wide solutions. No longer a mere piece part, the LH5420 handles system-level problems, allowing even the most high-performance

systems to be interconnected by efficient data “superhighways.”

Designed to meet the wish lists of top system designers, the LH5420 offers bidirectional, two-way “funneling/defunneling” from a 32-bit bus to a 16-bit or an 8-bit bus, with two-way parity checking built in.

Fully synchronous, the 36-bit LH5420 also is able to provide full-word-width, two-way communications between most 32-bit processors.

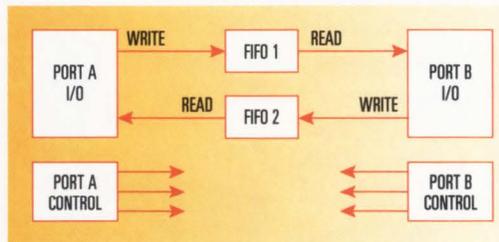
By replacing eight or more standard byte-wide FIFOs, the LH5420 saves real estate, simplifies the design process and accelerates system performance.

Its full-word width helps eliminate the problems of race conditions, metastabilities and speed differentials of side-by-side partial-word FIFOs.

The newest addition to Sharp's broad line of FIFOs — including both small-capacity (“shallow”) and large-capacity (“deep”) buffer memories —

ANSWERING THE WISH LIST.

THE LH5420 COMES PACKED WITH FEATURES WHICH DESIGNERS TOLD SHARP THEY WANTED IN A FULL-WORD-WIDTH FIFO, INCLUDING ON-THE-FLY PARITY CHECKING, TWO-WAY MAILBOX COMMUNICATIONS, SYNCHRONOUS REQUEST/ACKNOWLEDGE SIGNALS AND PROGRAMMABLE ALMOST-FULL AND ALMOST-EMPTY FLAGS. IT IS AVAILABLE WITH CYCLE TIMES OF 25, 30 AND 35 NS, AND IN BOTH PQFP AND PGA PACKAGES.



the LH5420 represents the industry's first system-level FIFO, requiring no external glue to integrate. It is available from Sharp for immediate delivery.

TIPS ON INVESTING

With widespread layoffs and corporate downsizing, engineers more than ever need to invest their savings for retirement, or, unfortunately, to cushion themselves against the loss of a job. Yet investors are facing lower interest rates on their money. The Federal Reserve Board's reduction of key short-term interest rates in 1991 likely will produce economic recovery in 1992. This sharp decline in short-term interest rates is propelling assets in money market funds and CDs into stock and bonds. This flow of funds should increase over time.

Yet only one in five Americans has taken any investment action to combat the effects of lower interest rates, says a recent Gallup survey. As more and more people invest funds in the equity markets for higher returns, stock prices should increase. An unprecedented demand for the returns that stock historically provided will fuel a bull market for the '90s.

In the fixed-income markets, interest rates are expected to remain relatively low, even as the economy recovers. And traditional business cycles will stay with us. No interest rate or financial index travels in a straight line; there are always cyclical fluctuations within their long-term trends.

Interest rates may increase slightly as the economy recovers in 1992. However, short-term interest rates will not approach their 1980s levels of 8% to 9%. If a 4% to 5% rate of interest is unacceptable for income needs, engineers must find other investments. Remember that higher yielding investments involve higher risk. With that said, we believe that the additional risk is worth the greater rewards if your investments are properly diversified and prudently managed. But before you invest even a single dollar and after you have carefully evaluated your resources, circumstances, financial goals and attitudes toward risk, you must ask yourself some very important questions. Chief among them is, "What am I trying to beat?"

Engineering investors would fall into one of two camps: Conservative investors who are averse to risk generally seek returns that are competitive with money market rates; most long-term investors, however, are looking to beat the Standard & Poor's 500.

A conservative investor trying to beat money market returns can choose between two different courses of action. First, consider extending the maturities of your fixed-income investments. In today's economic environment, the difference between short- and long-term yields are unusually large. Consequently, investors who extend maturities are well-compensated for the additional risk they assume—to a point. Generally, 10-year bonds provide most of the yield produced by their 30-year counterparts, but with substantially less risk. If you currently own Treasury bills or notes, consider reinvesting in

government securities with intermediate-term maturities.

Ironically, perhaps the best investments for conservative investors trying to beat money market rates can be found in the stock market. Specifically, large, blue chip, high-dividend stocks are among the safest in the market. And for the first time in more than 25 years, large-capitalization stocks are paying dividends that exceed money market rates.

In addition, stock dividends are likely to grow over time. For example, a good quality, diversified portfolio of dividend-paying stocks may yield 5% today, but that dividend (on a cost basis) could grow to 7.5% or 8% over a five-year period. Blue-chip stocks also offer the potential for capital appreciation, helping investors combat the long-term effects of inflation.

To beat the S&P 500 in 1992, think about investing in the stock market. Particularly attractive for equity investors in 1992 are cyclical, growth, and small-capitalization stocks.

Cyclical stocks are companies in which earnings are sensitive to economic cycles and traditionally benefit from most economic rebounds. As noted, the recovery in 1992 could be much stronger than many now anticipate.

Growth stocks are companies with above-average prospects for earnings growth. They can be either small or large companies and can be found in a wide range of industries. Small capitalization stocks are generally relatively new companies that offer the potential for superior growth over time. The most attractive small capitalization stocks are often those that have captured a market niche or have introduced an innovative new service or product. As a group, small capitalization stocks tend to be risky, but they also have the potential for the greatest rewards.

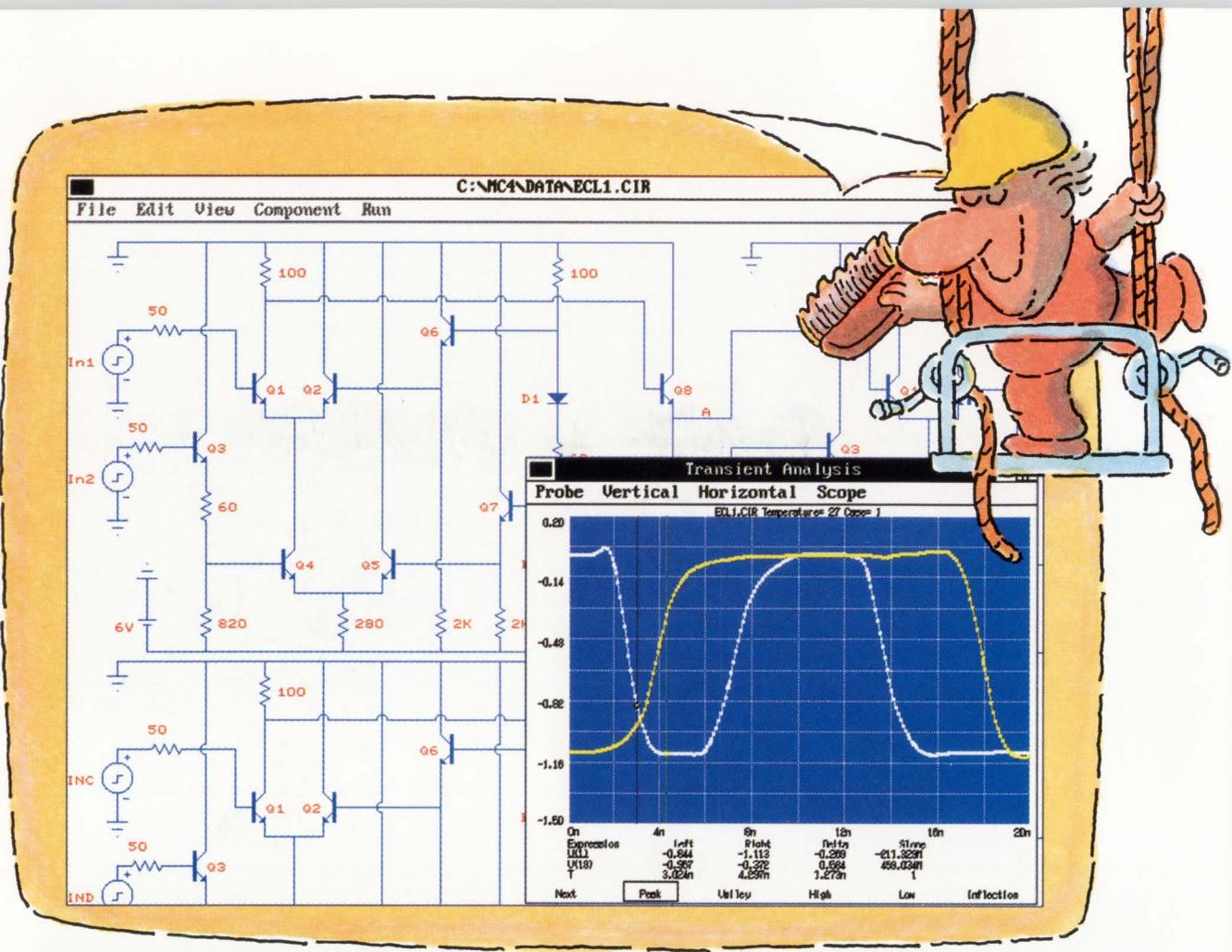
If your portfolio is properly positioned, you should be able to take advantage of the opportunities the financial markets will present in 1992. To prepare for the rest of 1992, it is important to decide on what you are trying to beat—money market rates, the S&P 500 or another benchmark—and then determine which investments are the most suitable for your needs. To obtain a free copy of *TRACK Personalized Investment Advisory Service*, a Shearson Lehman publication, and a prospectus with more complete information, including charges and expenses, call or write to me at the address below.

Henry Wiesel is a financial consultant with Shearson Lehman Brothers, 1040 Broad St., Shrewsbury, NJ 07702; (800) 631-2221. Wiesel also is a qualified pension coordinator with The Private Client Group. He invites questions and comments from readers.

HOT PC PRODUCTS

Sound enhances all types of applications, including those aimed at business and technical environments. Now a PC add-on product eases adding sound to software. The size of a deck of cards, the Audioport from Media Vision attaches to the outside of a PC, plugging into the parallel port and allowing voice recording and playback with a built-in speaker. The Audioport, which works from batteries or an ac adapter, complies with Sound Blaster and AdLib standards. The unit comes with voice-annotation software from Lotus Development Corp. to empower Windows object linking and embedded applications with sound. The Audioport lists for \$199. Contact Media Vision, 47221 Fremont Blvd., Fremont, CA 94538; (510) 770-8600; (800) 348-7116; fax (510) 770-8648. CIRCLE 459

The SnapPro image utility combines image capture, editing, and conversion into one desktop tool. Graphics can be captured or read in, then previewed, edited, converted, printed, combined with other images, or shared with other Windows, DOS, OS/2, and Apple Macintosh applications. Users can save images in formats used by most popular word-processing, page-layout, and paint programs. For DOS programs, SnapPro enables users to capture and edit DOS graphic screens by hitting a hot key. The software enables users to convert graphics files from one format to another. Formats supported include Windows 3.0 BMP and RLE, OS/2 BMP, Mac PICT2, TIFF 5.0, WPG, TGA, EPS, and GIF. SnapPro has a list price of \$69.95. For further information, contact Window Painters Ltd., 7275 Bush Lake Rd., Minneapolis, MN 55439; (612) 897-1305; fax (612) 897-3648. CIRCLE 460

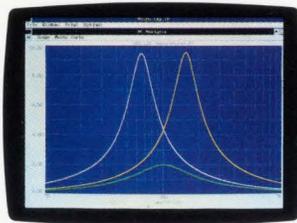


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AC Analysis

from SPICE 2G.6 models plus extensions. Comprehensive analog behavioral modeling capabilities. A massive model library. Instant feedback plotting from real-time waveform displays. Direct schematic waveform probing. Support for both Super and Extended VGA.

And the best is still less. At \$2495, MICRO-CAP outperforms comparable PC-based analog simulators — even those \$5000+ packages — with power to spare. Further, it's available for Macintosh as well as for IBM PCs. Write or call for a brochure and demo disk. And experience firsthand added SPICE and higher speed — on larger circuits.

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WHAT'S ALL THIS VICE-VERSA STUFF, ANYHOW?

Well, I always did want to write a column about vice-versa stuff. As my old friend Dave Ludwig likes to say, "In this world, it's dog eat dog — or vice versa." As I already mentioned in my column about negative feedback, it's nearly impossible to ride a bicycle with your arms crossed, because the arms get their tasks all figured out *one way*, and then you can't tell them to do the job *vice versa*.

So I wanted to write a good column about other vice-versa stories, and along came Jack Fogarty, Darryl Phillips, Doug Grant, and Gunnar Englund, who beat me to the punch. At this point, there's nothing I can do better than to shut up and let you read their letters:



BOB PEASE
OBTAINED A BSEE FROM MIT IN 1961 AND IS STAFF SCIENTIST AT NATIONAL SEMICONDUCTOR CORP., SANTA CLARA, CALIF.

Dear Mr. Pease:

Enjoyed your Jan. 9 column on negative feedback. Let me add one thing about crossed-arm bicycling.

If you try to balance a bicycle while rolling backwards, you'll crash. *But*, if you can cross your arms,

hold them rigid and steer with your *shoulders*, you'll find you can balance — at least for a little while.

If you *think* about what you're doing, you'll crash, but if you let your automatic balance prevail, well, sur-

prise! It works.

JACK FOGARTY
Professional Engineer
Columbia, MD

And I say, that's marvelous. I believe it. I haven't tried it yet, but I will.
Next:

Hi Bob:

You sure hit a nerve with your mention of riding a bike with crossed hands. Of course you're right, and there are implications that go beyond a showoff stunt.

Probably more ingrained in our genetic servo wiring is control of our feet. From the first creatures, the left foot has pushed off to go right. This may actually be the reason the brain lobes are crossed.

We take walking so much for granted it's difficult to even discuss the mechanics, so consider roller skating. You push with the foot opposite to the desired turn. It's equally true on other machines. Sit any kid on a sled, give him a start down the slope, and he will steer it fine with his feet. Push with the left foot to turn right. Can you think of an exception?

There is one. The airplane. The rudder pedals are hooked up "backwards" (you push left to turn left), and it cause the same cross-control problems you alluded to. One of my joys is giving first rides to kids, often in the 8- to 13-year-old group.

Most of them really take to flying, they do better than the typical adult. But taxiing for the first time is a nightmare. Invariably they go the wrong way, and make some comment that it's hard to steer with your feet. They're too overloaded by the unfamiliar surroundings to realize the obvious: the pedals are backwards.

Over the years, I've mentioned the problem to many pilots, and I've yet to find one that agrees. Usually they give me a look that says, "Well, buddy, I don't know about your rudder, but mine is hooked up just fine!"

The human is a very adaptable creature. We learn to fly and do okay most of the time. But within the brain, training is pulling one way and instinct the other. And when things suddenly come unglued — and millisecond response is needed — instinct sometimes wins and the wrong foot is used. It would be better to have the two forces aiding rather than opposing, but it's hard to make the changeover. Anyway, I wanted to share this with someone who understands.

DARRYL PHILLIPS
The Airport Corp.
Sallisaw, Okla.

Now that's a scary thought. Yes, a sled is easy to figure out how to steer. And yes, an airplane is feasible to control, and many people figure out how to fly it quite easily, after you think about it a little. But I never thought of its controls as being backwards or vice versa....

Now let's go on to a story about British Flying Officer H. M. Schofield, who was a pilot for racing seaplanes in 1927: "He took the Short-Bristol 'Crusader' out for a trial flight on Sunday the 11th. No sooner had he lifted off the water when he did a jerky half-roll and slammed back into the sea again. The impact tore the aircraft to bits and ripped off most of Schofield's clothing, smashing his goggles against his forehead. Bewildered, half-drowned, and infuriated, he was carried off to the nearby Italian Naval Hospital. When his aircraft had been reclaimed, it was found that the aileron control cables had been reversed! The best-laid plans...." *

So, just as George Philbrick pointed out that it was impossible for the automatic or "computerized" controllers of his day to accommodate a reversal of polarity — you can be completely gefoozled, even as a skilled human, if somebody springs a surprise change on you. As the seaplane's airspeed began to rise, the pilot saw the right wing

PEASE PORRIDGE

dropping. When he moved the stick to the left to try to bring the wing up, things got worse so fast he never had time to realize that the controls were reversed. Now *there's* positive feedback for you!

It's the same situation as the technician who was trying to mount a gyroscope on the bulkhead of a missile. It was kind of inconvenient to get it bolted down, so he decided to mount it on the other side of the bulkhead — it fit much better using the same mounting holes.

But when the missile was launched, the controls went "haywire," and of course, it also crashed, with controls full-over against the stops. Both of these cases are just like the next story, which you can appreciate without being an airplane pilot:

Dear Bob:

Your column on "Negative Feedback" reminded me of a real-life example of positive feedback described by one of my profs at Northeastern.

The example deals with a dual-control electric blanket, where the controls have ended up on the wrong side of the bed. From any initial condition (for example both set at "5"), the system soon goes unstable. The husband is too cold so he turns "his" control up. The wife, of course, gets too hot and turns "her" control down. This makes the husband colder, so he turns his side up more, causing her to turn hers down. Eventually, both controls end up at the stops and the humans end up at each other's throats.

DOUG GRANT

Wilmington, Mass.

Exactly! Now I'll finish up with a letter about a ship that was moving MUCH slower than 100 mph, when it crashed, and crashed... and crashed repeatedly:

Dear Bob:

It's kind of a privilege to have an opportunity to write to you. I look forward to someday passing the casual remark to my grandchildren, "...and then I told Bob Pease..."

This brings me a little bit closer to the subject. When I was a child myself, me and my friends did just that — bicycling on a lawn with our arms

crossed. You are right, it is very difficult and it hurts, too. Some of us got rather good at it, and I recall that the girls adapted faster than the boys. Is there a lesson to be learned?

The experiment has been repeated here in Sweden recently. Or rather between Sweden and Denmark, on the water separating Swedish Helsingborg from Danish Elsinore. Remember Hamlet?

A clever person decided to make the new ferry more efficient by allowing it to go both ways, without having to turn around each time. The idea isn't very new, but this time the clever person decided to save some money by using the same steering wheel for both Denmark-bound and Sweden-bound traffic. A steering wheel and an old-fashioned machine telegraph seemed to be a bad idea, so the two were combined into one joystick.

Now there was some real confusion: The difference between starboard and backboard is tricky enough, but now you also had to separate Swedish and Danish starboard and backboard. If that's not enough, it seems there were different forwards and backwards as well. One set for Sweden and one set for Denmark.

All good experiments have results. In this experiment, we use the word "consequence" instead. The consequences were: heavy damage to both harbors, heavy damage to the ferry (both ends), damage to cars, and people injured. The experiment went on for some time. Obviously, the experimenters were anxious to rule out random and systematic errors. After some time, with consistent results, the experiment was evaluated. We're still waiting for the report. Moral: Know your polarities, and stick to one set of definitions.

For someone who knows anything about northern Europe, astronomy, and folklore, it comes as no surprise that the name of the ferry is Tycho Brahe.

GUNNAR ENGLUND

Granbergdsdal, Sweden

Well, Mr. Englund, some skiers and some drivers are just "an accident looking for a place to happen," and that ferry boat was, too. Note, Mr. Englund observed that it was appropriate

for the ferry to be named after the great 16th-century Danish astronomer Tycho Brahe. Brahe published a list of "bad-luck" days — the "Tycho Brahe days" — when a great project or journey should not be initiated, because it will come to a bad end. Mr. Englund did confirm that no correlation had been found between the Brahe days and the ferry accidents or the boat's launching date. Perhaps the people who designed the control system for the ferry will propose a 4-lane vehicular tunnel between England and France — with no center divider. So, where do the drivers change over from driving on the left to driving on the right? Any time they want to! — whenever the mood strikes them! Now, there's a vice-versa situation!

All for now. / Comments invited!

RAP / Robert A. Pease / Engineer

Address:

Mail Stop C2500A

National Semiconductor

P.O. Box 58090

Santa Clara, CA 95052-8090

*Excerpted from *The Great Air Races* by Don Vorderman, Bantam Books.

BOB'S MAILBOX

Dear Bob:

Thank you for writing all of those very informative and enlightening articles. They are both educational and bring back memories of my forty years in electronics. I have clipped every one to date for further reference. I believe I have a very good source for high-isolation power transformers, both linear and switching types, for Mr. Neal Iverson of the Boeing Co. His letter was in the February 20 issue. The company is: Glen Magnetics Inc., Third Avenue, Alpha, NJ 08865; tel: (201) 454-3717; fax: (201) 454-2702.

Mr. Iverson should contact Mr. Emil Badway, who is the vice president of engineering. They have made many extremely critical transformers for companies I have been employed by.

GLENN A. THOMPSON

Penn Yan, N.Y.

Thanks for the info.—RAP

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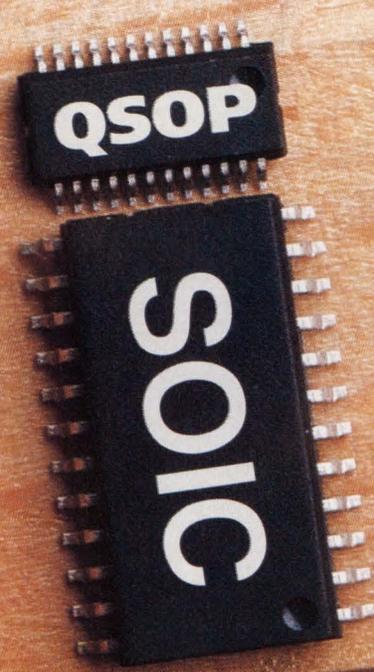
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2163 2373 2646 2843	163 373 646 843		
2191 2374 2648 2845	191 374 648 845		
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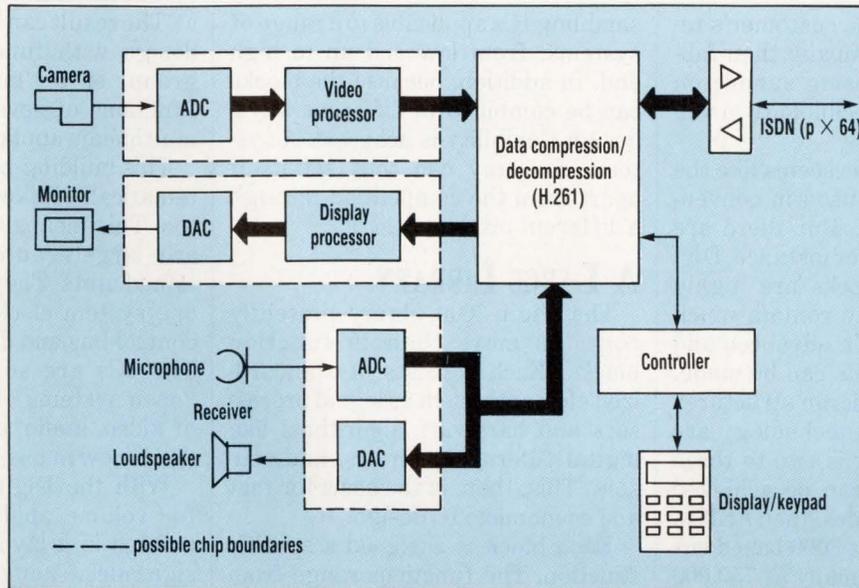
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1. ONLY 13 FUNCTION BLOCKS are needed to implement three ICs (shaded boxes), using ITT Semiconductors' library of high-performance ASIC blocks. The video-telephone circuit links I/O devices, such as a camera, TV monitor, microphone, and loudspeaker, to a 64-kbit/s ISDN primary-rate channel.

DESIGNERS CAN SELECT PARTS FROM A LIBRARY OF BLOCKS TO ASSEMBLE HIGH-PERFORMANCE ICs FOR MANY VOLUME APPLICATIONS.

FUNCTION BLOCKS SPEED UP CHIP DEVELOPMENT

W

JOHN GOSCH

ith a new system of function blocks to implement ASICs, equipment designers and producers can now procure ICs faster than ever before. The Digit 3000 system developed by ITT Semiconductors in Freiburg, Germany, cuts IC development time by as much as 75%, depending on circuit complexity. This means faster delivery of ICs to ITT's customers. For customers, in turn, easy device availability translates into fast time-to-market for their products. The new concept also reduces a product's IC components count—from three to four times compared to previous methods—which drives down product cost.

To benefit from the concept, equipment designers spell out to ITT the tasks they want a desired circuit to perform. From its library of function blocks, ITT chip designers select suitable blocks and assemble them into a

HIGH-PERFORMANCE ASIC FUNCTION BLOCKS

circuit that meets the customer's requirements. The company then fabricates the circuit using submicron CMOS processing technology in volume production.

At first glance, this seems like the classical procedure used in conventional ASIC design. But there are major differences. For instance, Digit 3000 function blocks are highly complex and already contain much software. As a result, advanced and high-performance ICs can be made. Also, because submicron structures in a uniform CMOS technology are used, circuit density is two to three times higher than can be achieved with conventionally designed ASICs. For example, a Digit 3000-based circuit may contain as many as 750,000 transistors.

The diverse function blocks cover video and audio fields, as well as word-processing, graphics and control. With such diversity, they can be assembled into ICs usable in virtually all kinds of electronic systems, such as TV sets, car radios, communication terminals, robots, controllers, automotive equipment or others. One interesting application is multimedia systems. Here, audio, video, and computer technologies merge, and suitable Digit 3000 ICs can handle them all.

Furthermore, because the library contains not only complex but also simple blocks, it lends itself to as-

sembling ICs applicable to a range of systems, from low end up to high end. In addition, because the blocks can be combined in different ways, design flexibility is achieved. A systems company can thus set itself apart from the competition through a different product design.

A LARGE LIBRARY

The Digit 3000 library presently contains more than 40 function blocks. Each consists of standardized elements, such as signal processors and hardware algorithms like digital filters, converters, and sensors. This, then, is the basis for fast and economical IC design.

Each block is assigned a specific function. The functions range from analog-to-digital and digital-to-analog conversion, encoding, decoding, and digital-signal processing to interfacing, frequency synthesis, clock generation, data reduction, and text/graphics processing. By its design, a block is already optimized for its particular tasks.

The function blocks, as well as relevant software components, are arranged in five groups: video, audio, text/graphics, control, and special functions (see the table). By using these blocks, IC designs can be flexibly varied and quickly adapted to suit specific applications.

The functions can be concentrated on one chip or distributed over sever-

al. The result can be a "pure-bred" IC design with functions of only one group, or a "mixed" design with functions of several groups, say, a multimedia application.

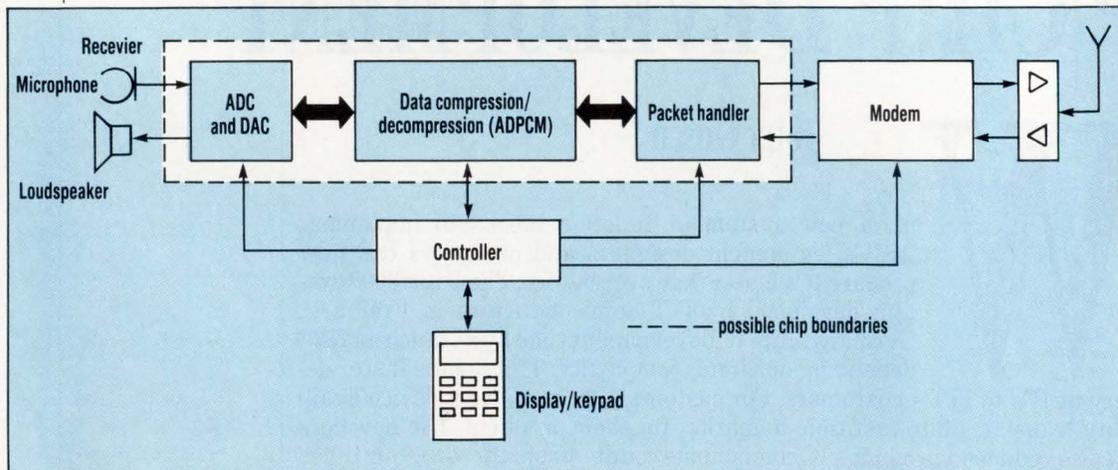
This building-block concept is systematically followed at the IC level, too. This means that Digit 3000 ICs are largely autonomous, self-contained units. They operate with only one system clock and with flexible control-bus and data-bus structures. The ICs are software-supported "open systems" for a large number of video, audio, and computer standards now in use.

With the Digit 3000 system, ICs for volume applications are implemented in a layout with 0.8- μ m design rules. Thanks to uniform submicron CMOS technology, any combination of analog or digital circuits can be realized on one chip for a mixed-mode design.

Integrating analog and digital circuit parts brings important simplifications and benefits for the application: only one power supply is needed. And because no interconnects exist between digital ICs, systems reliability is enhanced. Reliable operation is also achieved by having, for example, signal-processor, converter, and sensor circuits all on the same piece of silicon.

With a suitable DAC, a Digit 3000 IC seen from the outside behaves like an analog circuit, which minimizes interface problems. Still, as many functions as possible—about 90%—are implemented digitally in the ICs to exploit the benefits of digital technology. For example, mostly digital sigma-delta or pulse-density modulation (PDM) converters are used for audio-signal conversions.

When designing a digital system, it's logical to choose a system clock related to one of the system's natural fre-



2. TO IMPLEMENT THE FUNCTIONS shown in the shaded box, eight functions blocks from ITT's library of high-performance ASIC blocks are used. The function blocks form an IC that's used in cordless-telephone applications.

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				-40° - +85°C
CXK581100TM	100/120	TSOP	12/50	
CXK581100YM	100/120	TSOP (rev.)	12/50	
CXK581001P	70/85	DIP 600 mil	12/50	
CXK581001M	70/85	SOP 525 mil	12/50	
CXK581020SP	35/45/55	DIP 400 mil		
CXK581020J	35/45/55	SOJ 400 mil		
CXK581021J	47	SOJ 400 mil		
CXK581120J	15/17/20	SOJ 400 mil		
CXK77910J	20	SOJ 400 mil		Sync., 128K x 9

Note: All packages 5V, 32 pin, 128K x 8, unless otherwise noted.

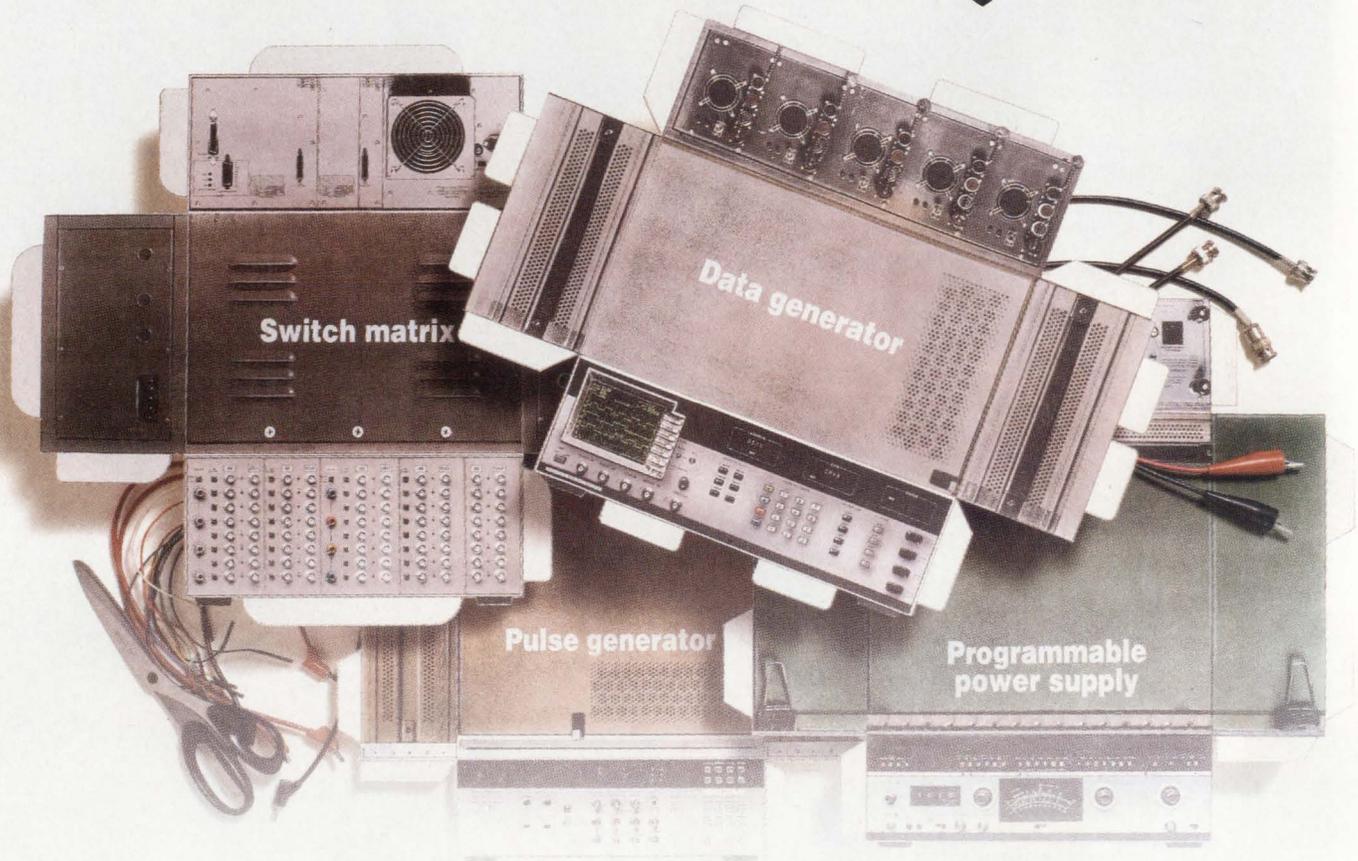
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CIRCLE 163 FOR RESPONSE OUTSIDE THE U.S.

HIGH-PERFORMANCE ASIC FUNCTION BLOCKS

quencies. Difficulties arise, however, when there are several such frequencies that aren't interrelated in any rational pattern. In the past, to avoid expensive computing operations, the timing pattern was adapted to the signal processing.

Now, the computing required to interpolate different data rates is no longer an economic burden because of the submicron circuit structures. A Digit 3000 application can therefore use a common system clock for all processing operations. This gets rid of the many clock

generators previously needed and cuts down interference-induced malfunctions.

The only existing criterion for choosing a system clock is the necessary analog bandwidth of the signals being processed (which, according to the sampling theorem, is twice the Nyquist frequency). It may be a good idea to match the system clock to the data rate of time-discrete or digital signals processed in the same system. Otherwise, these signals must be interpolated for the system clock.

THREE BUSES

ICs constructed from Digit 3000 blocks can exchange data over one of three buses. One is the PICTUREbus, which is a digital, orthogonal (16 + 3)-bit bus for picture signals. Up to eight different signals may be present simultaneously on the bus. In this case, the three extra bits are for priority control.

Another is the SOUNDbus, a digital, serial three-wire bus for sound signals. It can transmit a maximum of four channels of information between audio processors.

The third bus is the DIGITbus, a digital, serial single-wire bus with a flexible protocol structure for systems control. The controller communicates with all processors in the system through the DIGITbus.

ITT Semiconductors has targeted its Digit 3000-based ICs at a multitude of applications, but its sights are set on multimedia systems, a market with enormous growth potentials worldwide. "We want to make our ICs useful for those who want to marry multimedia's audio, video, and computer technologies in one system," says Klaus Heberle, who heads the Human Interfaces and Microcontroller group in the company's Concept Engineering department. The Freiburg company has already launched deals with American computer makers to develop circuits that can be used in multimedia systems.

In a multimedia application, audio and video signals in some form are primarily processed on a PC or workstation. Or conversely, a TV set is equipped with an interface, which permits it to take over computer data. The system configurations will

differ considerably depending on two factors: the media to be combined in a particular application and the demands the signal processing must fulfill.

As an example, a simple two-IC configuration for picture-rate conversion can be designed from seven Digit 3000 function blocks. With such a configuration, video data of different formats, like NTSC and VGA, can be superimposed on a computer's display unit. In this application, storage and further processing in the computer isn't possible.

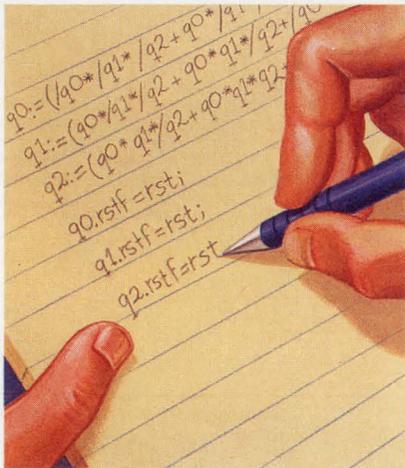
In another multimedia application with optical mass storage and circuits for data compression and/or decompression, still and moving pictures can be handled on the computer. Also, connection to data networks is possible through the data-reduction interface so that the system can also be used as, say, a video-conference terminal. For this particular application, 14 function blocks are assembled into one IC for multistandard audio processing.

With much activity going on in new communication services, applications for Digit 3000-based ICs open

MAJOR APPLICATIONS CATEGORIES FOR ITT SEMICONDUCTORS' DIGIT 3000 ASIC FUNCTION BLOCKS

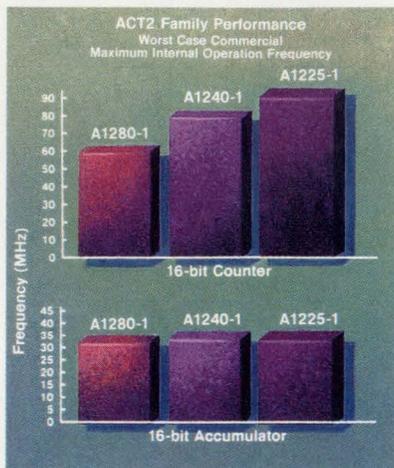
Video	Audio	Text-graphics	Control	Special functions
8-bit ADCs 10-DACs	16-bit ADCs 16-bit DACs	Multistandard Teletext	10-bit ADCs 16-bit DACs (PWM)	Programmable parallel processing
Multistandard processing	Programmable DSP	On-screen display	RISC architecture	Asynchronous operation
Display processing	IF selection/ demodulation	Closed captioning	CISC architecture	Digital HDTV
Satellite TV	Adaptive de-emphasis	Video programming	Integrated sensors and actuators	High-resolution display, projection, LCD
Interfaces with digital systems (PCs)	Multistandard baseband processing	Teletext level 2	Frequency synthesis	Flicker-free progressive scan
Multistandard encoding	Interfaces with digital systems (CDs)	Pixel graphics	I/O interface	Data reduction
Picture memory	Features (spatial sound, radio data system)	Communications services (fax, videotex)	Magic-Wand interface	Industrial applications (robot control)
Features (picture-in- picture, zoom)	Data reduction	Global positioning system	DIGITbus interface	Interfaces
PICTUREbus interface	SOUNDbus interface		Clock generation	

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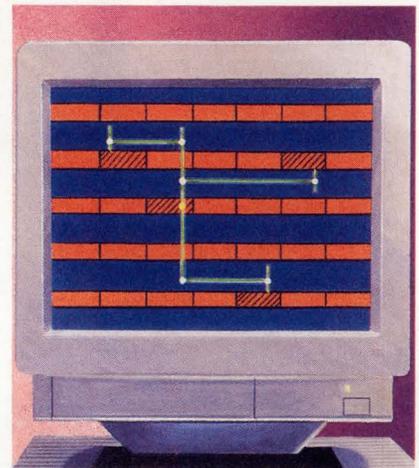
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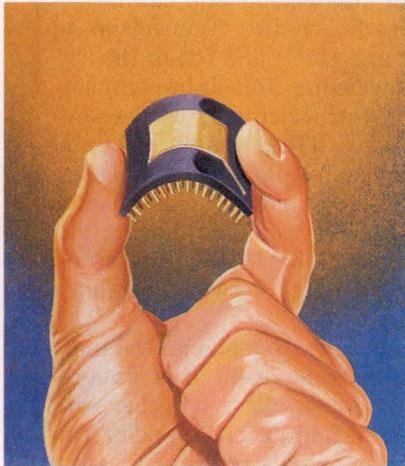
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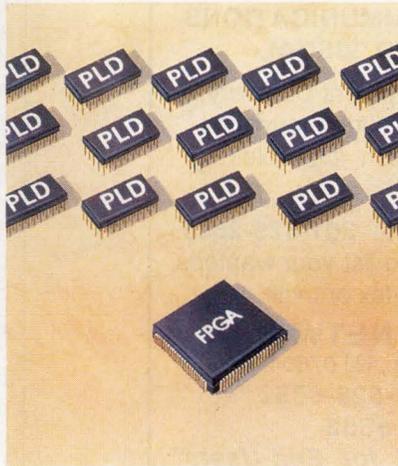
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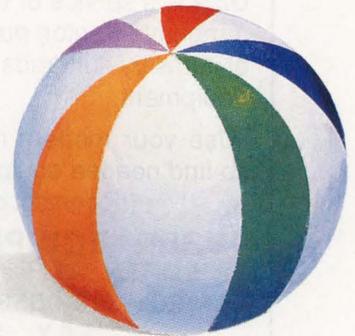
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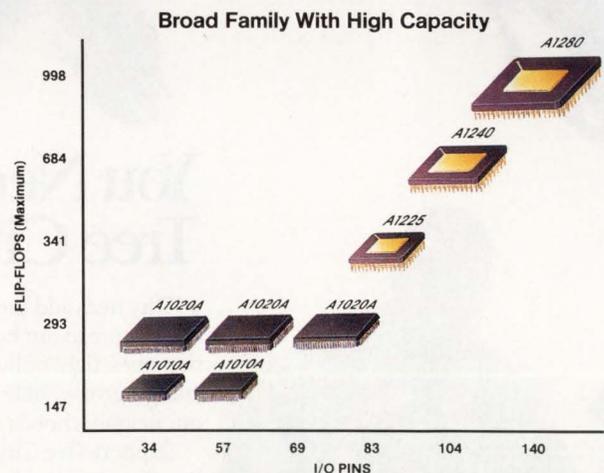
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The FPGA Design Guide

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**HIGH-PERFORMANCE
 ASIC FUNCTION BLOCKS**

up in telecommunications terminals. Two examples of such communications services are the videophone and the cordless telephone. The videophone comprises input/output devices, such as a camera, monitor, microphone and loudspeaker (*Fig. 1*).

With 13 function blocks, three key ICs for this videophone can be designed. The data is converted in ADCs and DACs and fed to the signal-processing and data-compression circuit, which operates according to the CCITT (Consultative Committee on Telephony and Telegraphy) H.261 standard. This enables data to be reduced for moving pictures up to the ISDN (Integrated Services Digital Network) 64-kbit/s primary rate.

In a cordless telephone, the most important component is a data-reduction circuit which, together with converters and a packet handler, can be implemented with one IC using eight function blocks (*Fig. 2*). The IC operates according to the ADPCM (adaptive differential pulse-code-modulation) principle, and is supplemented by circuits for frequency-synthesis and data-packet-handling functions.

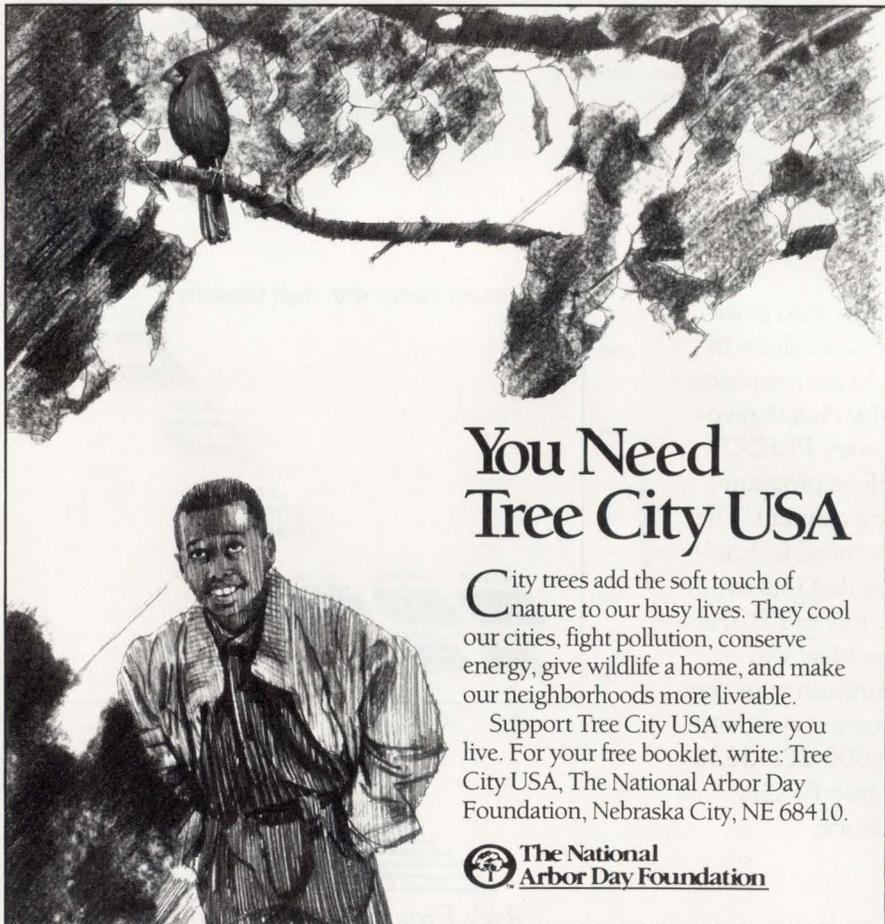
Interfaces with the outside world are formed by the high-frequency link with a modem and a duplex separation filter at the transmitting/receiving end, as well as an audio codec at the user end. All function blocks for audio-frequency processing and for the system controller can be accommodated in one IC. □

PRICE AND AVAILABILITY

The Digit 3000-based ICs sell for less than \$10 each in volume quantities, with the exact price depending on circuit complexity and the number of ICs ordered. Prototypes are available in 6 to 12 months (depending on circuit complexity) after customers have specified for ITT Semiconductors circuit requirements.

ITT Semiconductors, P.O. Box 840, D-7800 Freiburg, Germany; Reinhard Preuss, phone: (0049)-761-517337; fax: (0049)-761-517799.

CIRCLE 518



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MODERATELY
SLIGHTLY

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561
562
563



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- Technical literature, including a handy introductory guide to understanding and using small microcontrollers.

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The low \$50 sticker price on the 68HC05 K-Series In-Circuit Simulator Kit is good only through participating Motorola distributors! But you better act now. This special offer ends June 30, 1992. And at \$50, the 68HC705KICS kit is priced to move.



* Official information on rules, regulations and contest deadlines is included with each 68HC705KICS kit. Government employees and Motorola employees and their families are not eligible for the 68HC705KICS contest. If the winner is not permitted to accept this prize by his or her employer's policies or practices, Motorola will donate an equivalent cash amount to an appropriate charity designated by the winner. Void where prohibited or restricted by law. M and Motorola are registered trademarks of Motorola, Inc. © 1992 Motorola, Inc.

INTELLIGENT SOFTWARE HELPS ENGINEERS BUILD HIGH-SPEED BOARDS AND MCMs THAT ARE CORRECT THE FIRST TIME THROUGH.

PC-BOARD TOOLS SIDESTEP HIGH-SPEED DESIGN SNAGS

LISA MALINIAK

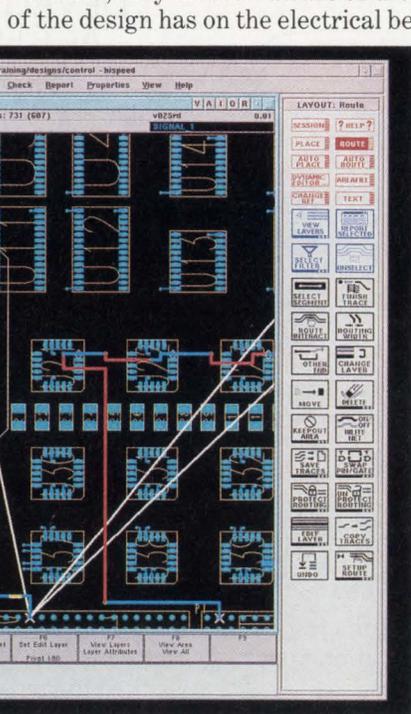
Today's high-speed board designers face tough challenges. Problems and limitations arise from such features as operating frequencies above 50 MHz, 1-ns rise and fall times, and propagation-delay limitations. On top of that, systems are getting smaller while IC packages grow larger. If not approached properly, high-speed board design can be an engineer's worst nightmare.

Engineers must attack these designs with a different technique than the schematic-driven layout provided by a traditional serial design cycle. From the start, they must be aware of the impact that the physical representation of the design has on the electrical behavior of the circuit. For example, parasitic elements and interconnect dimensions of a pc board are each active circuits that can potentially affect the functionality and performance of a design.

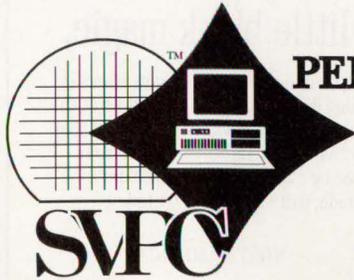
Engineers need software tools that let them make design decisions during iterations between the physical representation and their simulation environment.

Many of the new pc-board tools are trying to fill these needs of complex pc-board design. The latest is the Board Station 500 software from Mentor Graphics Corp. Board Station 500, which addresses the unique requirements of high-speed pc boards and multichip modules (MCMs), is a superset of the company's previous Board Station software version. The Board Station software is a pc-board design and layout system that shares a common database, and encompasses schematic capture, simulation, electronic packaging, physical layout, testing, and documentation.

Board Station 500 combines the existing Board Station software with



AN INTELLIGENT MECHANISM inside Board Station 500 helps users meet high-speed design rules. In this screen shot, the inside diamond shows the distance allowed to meet the minimum-length requirements; the outside diamond shows the distance allowed before violating maximum-length requirements.



SILICON VALLEY PERSONAL COMPUTER DESIGN CONFERENCE

AUGUST 10 - 12, 1992

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**The Santa Clara Convention Center, Santa Clara, California
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The Silicon Valley Personal Computer Design Conference focuses on providing solutions to key PC, Workstation, and Peripheral design and integration issues. SVPC is aimed at designers and strategic planners who are trying to differentiate their systems, or design or evaluate the next-generation desktop, portable and pen-based computer technologies and systems.

The conference will provide many half- and full-day tutorials on the opening day (August 10), and over 100 technical paper presentations in four parallel paper tracks (August 11 and 12). The papers will cover key design and implementation issues for desktop and portable systems. Topics will include:

Motherboard Design Issues...Portable System Design...Memory-Card Interfacing... Mass-Storage Subsystem Design...Pen-based System Design...Multimedia Hardware Design...Data Communications (Data/Fax Modems, Serial cards, Etc.)...BIOS Implementation and Graphical User Interface Issues...Power Management Schemes...Video and Graphics Subsystems...Local-bus Interface Approaches...Peripheral Subsystem Design...System Buses (ISA, EISA, MCA, SBus, NuBus, Etc.)...Network Interfaces (RF, Token Ring, Ethernet, Etc.).....and many other topics.

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Note: Registration fees include coffee break refreshments, lunch, exhibits entry, and one set of tutorial notes, and/or conference proceedings

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HIGH-SPEED BOARD TOOLS

timing-constraint-driven place-and-route algorithms and high-speed analysis to control and analyze physical effects and maintain signal integrity. In addition, Board Station 500 not only identifies electrical-rule violations in real time, but also it provides intelligent mechanisms that guide users in meeting design requirements (*see the figure*). For instance, when an engineer doesn't meet a length requirement, the tool both flags the error and also indicates the distance allowed to meet the minimum-length requirements, along with the distance allowed that won't violate the maximum-length requirements.

DESIGN UNIFICATION

To ensure total coverage of high-speed effects, Board Station 500 unifies all steps ranging from design capture through manufacturing interface. Users begin by specifying a set of electrical rules using Mentor's Design Architect design-creation software. The electrical rules can include such items as method of interconnect, topology constraints, allowable interconnect delays, and impedance characteristics. However, electrical rules don't take into account layer-to-layer, via, or other physical constraints of board design. So Board Station 500 automatically maps the electrical rules into a set of physical rules for subsequent use by automatic and interactive place-and-route algorithms. This design methodology is key as it enables the physical representation to meet the electrical performance requirements of the design.

The principal physical rules that Board Station 500 adheres to include net topology, minimum/maximum length control, stub-length control, matched-length control for clock-skew elimination, via limits, automatic termination assignment, layer restrictions, balanced-pair routing, parallelism control, and shielding generation. Users can also enter and amend the physical rules directly.

There are a variety of examples where the insertion of physical rules into the design layout becomes important. These include using a bal-

anced-pair approach for noise reduction in ECL design, and providing shielding support for the reduction of EMI susceptibility and crosstalk. In addition, timing control must support meander generation to accurately control signal arrival while minimizing interconnect length.

During and after layout, users can check their results with an integrated set of high-speed analysis tools from Quad Design Technology, Camarillo, Calif. The first of these tools, Pre-route Delay Quantifier (PDQ), provides placement-based interconnect-delay calculation and placement evaluation. Another Quad Design tool is the Crosstalk Toolkit (XTK), which offers multi-conductor crosstalk noise analysis. XTK includes electromagnetic field solver and parameter extraction (XFX), and multi-conductor Crosstalk Network Simulator (XNS). PDQ and XTK are encapsulated in Mentor's Falcon Framework for Concurrent Design, and provide full support for the OSF Motif user interface.

With the Falcon Framework, users have access to related Mentor tools: Design Architect for design creation and electrical rules definition, QuickSim II for logic and system-level simulation, QuickPath for critical path and timing analysis, and AutoTherm for thermal analysis. Board Station 500's tight integration with the company's simulation environment allows for back-annotation of interconnect delays for post-layout simulation and timing verification. Once a design is done, the Board Station software generates the necessary manufacturing information and documentation. □

PRICE AND AVAILABILITY

Board Station 500 runs on HP Apollo, HP Series 700, and Sun workstations. It's available now for \$125,000. Upgrades to Board Station 500 from other Board Station versions start at \$30,000.

Mentor Graphics Corp., 8005 S.W. Boeckman Rd., Wilsonville, OR 97070-7777; (503) 685-7000. **CIRCLE 516**

HOW VALUABLE?

HIGHLY	557
MODERATELY	558
SLIGHTLY	559

CIRCLE

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Pleasanton, CA	May 8
Milwaukee, WI	May 11
San Diego, CA	May 11
Chicago, IL	May 12
Irvine, CA	May 12
Houston, TX	May 13
Woodland Hills, CA	May 13
Dallas, TX	May 14
Phoenix, AZ	May 14
Dayton, OH	May 15
Denver, CO	May 15
Minneapolis, MN	May 18
Huntsville, AL	May 18
Waterbury, CT	May 19
Atlanta, GA	May 19
Whippany, NJ	May 20
Tampa, FL	May 20
Smithtown, NY	May 21
Orlando, FL	May 21
Santa Clara, CA	May 27
Rochester, NY	May 27
Beaverton, OR	May 28
Toronto, Can	May 28
Bellevue, WA	May 29
Montreal, Can	May 29
Waltham, MA	June 1
Raleigh, NC	June 2
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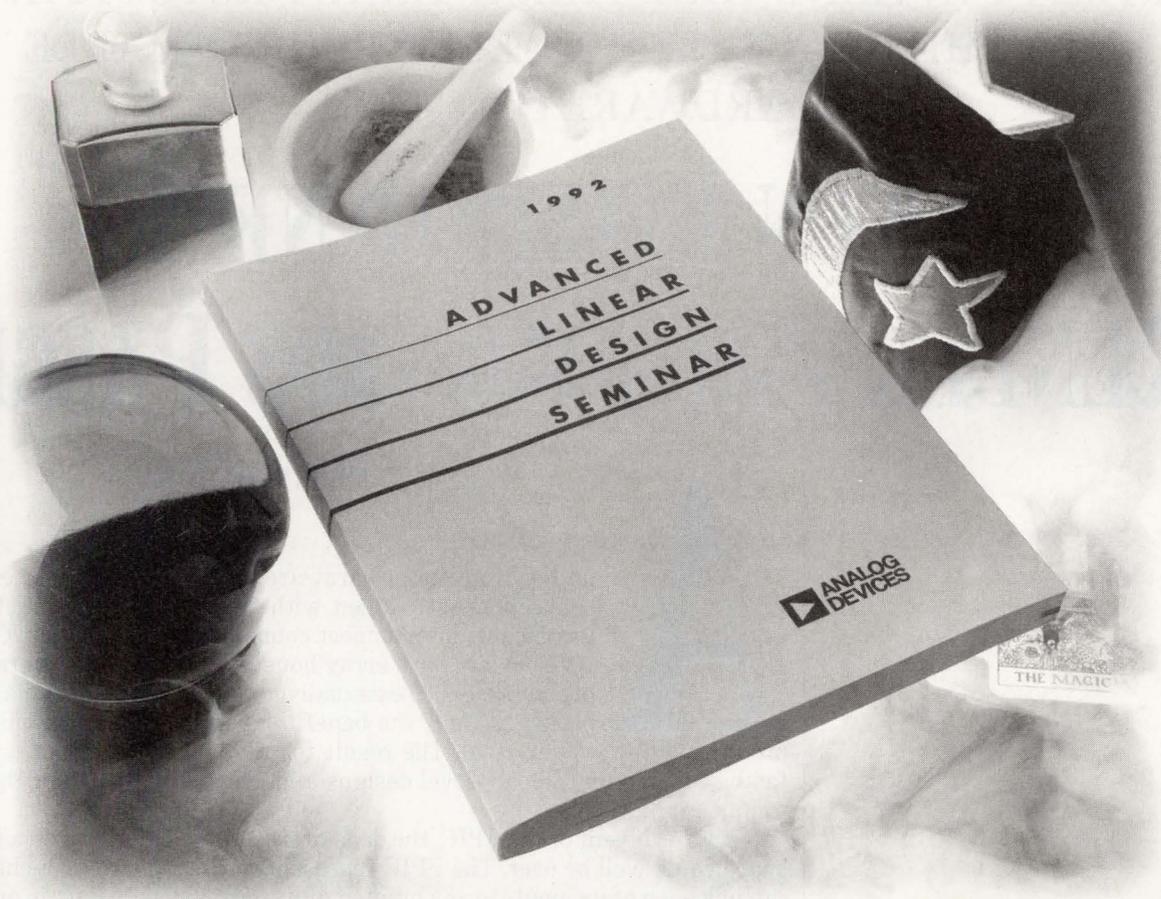
EUROPE

City	Date
Copenhagen, Denmark	May 4
Berlin, Germany	May 5
Wiesbaden, Germany	May 6
Hamburg, Germany	May 7
München, Germany	May 8
Vienna, Austria	May 11
Zürich, Switzerland	May 12
Lyon, France	May 13
Paris, France	May 14
London, England	May 15
Edinburgh, Scotland	May 18
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Stockholm, Sweden	May 20
Rome, Italy	May 21
Milan, Italy	May 22

Far East and Japan seminars to be held in June. Please call 1-617-937-1430 for schedule.



If you've always thought linear design involved a little black magic, here's where you can learn a few of the tricks.



If you're one of the few engineers who realizes the world of analog design isn't all that mysterious, you'll appreciate our Advanced Linear Design Seminar. Because it's the perfect opportunity to pick up a few new tricks.

Hosted by Analog Devices, one of the leading suppliers of analog and mixed-signal ICs, and its distributors, the seminar series will include talks by prominent design wizards such as Derek Bowers, Paul Brokaw, Lou Counts, Barrie Gilbert, Walt Jung, and others.

The full-day tutorials also include solutions-oriented discussions that are geared towards showing you how to increase system performance while actually lowering overall cost. Plus you'll get free product samples, our 700-page *Amplifier Applications Guide*, other technical reference materials, and more.

Admission to the seminar is just \$20, and it includes everything above, lunch, and refreshments.

So if you're a design wizard who wants to add to your repertoire of linear design tricks, it's no secret what you should do — call 1-800-ANALOGD (in Canada, call 617-937-1430) and reserve a seat today. Before they all disappear.



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CIRCLE 86 FOR U.S. RESPONSE

CIRCLE 87 FOR RESPONSE OUTSIDE THE U.S.

A 1024-PIN LAND-GRID ARRAY LIFTS PROTOTYPING INTO THE REALM OF TOTALLY PROGRAMMABLE HARDWARE SYSTEMS.

SILICON INTERCONNECTS RENDER BREADBOARDS PASSÉ

DAVID MALINIAK

Another frontier for hardware programmability—the interconnection—has fallen with the arrival of the field-programmable interconnect component (FPIC). Aptix Corp.'s 1024-pin land-grid array houses a universally programmable matrix of 940 externally accessible interconnects in one package. Thus, the benefits of user programmability are brought to the system level. The result for the system designer is much faster completion of board-level designs and greater control over the end-product's final shape.

With the advent of the FPIC, the days of point-to-point wiring on a breadboard could well be over. The FPIC represents a breadboard-on-a-chip that can link each of its inputs to any number of its outputs, including, in one version of the device, to dedicated pins that act as a "window" to any signal (*ELECTRONIC DESIGN, Jan. 23, p. 31*). Designers gain the high observability and quick turnaround of simulation combined with the form and function of the final product throughout the design-verification process.

The implications for hardware-system prototyping and debugging are considerable. Frequently, designs are held up because software for programmable systems languishes while waiting for its integration with hardware, which must be prototyped and debugged before the two can be meshed. Up until that point, neither software nor hardware can be verified in full. The FPIC, combined with its easy-to-use development system, can shorten the lag from software's development to its integration with hardware by anywhere from 6 to 12 weeks, the company claims. Applications include general connection for board-level circuitry, connecting FPGAs in ASIC-emulation systems, and customer-specific circuit customization.

Initially, two flavors of the FPIC will be offered. The FPIC/R is a reprogrammable, SRAM-based device with bidirectional paths and pin-to-pin path delays as low as 5 ns for critical paths. The FPIC/R is meant for applications where prototype replication and dynamic in-system programming is required. The device, which integrates over 1 million transistors and is processed in 0.8- μ m CMOS technology, comes in a 1024-pin PGA. Of those 1024 pins, 940 are interconnection pins and 20 are for power and initialization.

The FPIC/D device is also reprogrammable, but incorporates a 64-channel diagnostic port with logic-analyzer interfaces that enable rapid debugging of FPIC-based systems. Once attached to a logic analyzer, the diagnostic port makes available any signals passing through the FPIC for observation under software control. The 64 diagnostic signals from the FPIC/D device connect

FIELD-PROGRAMMABLE INTERCONNECT COMPONENT



FAST PROTOTYPING for pc-board and ASIC applications is promised by Aptix's development system for the field-programmable interconnect component. The FPIC/D device, with its on-chip 64-channel diagnostic port, is easily linked to logic analyzers for rapid debugging.

directly from its package to a flex cable, which in turn attaches to a logic-analyzer interface pod. The company is offering its DP-HP1 interface pod, which sends signals from the FPIC/D to Hewlett-Packard's HP 16500 family of logic analyzers.

FPIC applications involving conventional board formats are further aided by the availability of two field-programmable circuit-board (FPCB) formats. The FPCB-AT is a full-sized PC-AT-compatible board that accommodates up to three FPIC devices and more than 2000 connectable component pins. Through-hole row spacing is on 0.1-by-0.3-by-0.1-in. centers. The FPCB-GP2 is a general-purpose 7-by-10-in. board that holds up to two FPIC devices.

An FPCB is divided into FPIC regions, and all potential component-pin locations within a given region connect to that region's FPIC. Each FPIC has from 140 to 200 pins dedicated to global interconnections. Signals can travel through a maximum of two FPIC devices. The FPIC/R devices on top of the board are mirrored on the back side by an FPIC/D device mounted to common through

holes. The FPIC/D device's diagnostic pins serve as windows for analysis of all signals on the board. Used together, the FPIC/D devices implement diagnostics, while the FPIC/R devices implement prototype replication. As a result, prototype replication is made easier and faster.

To support the development of other FPCB form factors, Aptix offers its FPCB Compiler, a software system capable of generating the FPCB routing architecture. With it, pc-board-layout designers can create FPCBs with a multitude of form factors. The software produces standard Gerber-format output files, which are easily assimilated by popular board-layout systems.

Both FPIC/R and FPIC/D devices are supported by the company's easy-to-use development system, which includes programming and diagnostic software and hardware (see the figure). All are accessible through a highly intuitive user interface that, at least initially, runs on a Sun Sparcstation platform.

The development system enables fast prototyping of pc-board and ASIC applications. The system ac-

cepts net-list formats from popular schematic-capture packages and performs both manual and automatic partitioning and placement, as well as fully automatic routing within FPIC devices. Routing time for a fully utilized FPIC device is under 5 minutes. Incremental routes typically take a few seconds. In creating the configuration data for programming the FPIC devices automatically, the software allows the management of critical paths and supports incremental changes of design data.

Both the FPIC/R and FPIC/D devices represented a substantial challenge from the packaging perspective. First, a custom multilayer ceramic package was developed which converted the extremely fine pad pitch on the die to a 50-mil pad pitch suited for mounting on a pc board. Then, the C4 (controlled-collapse chip connection) die-to-package bonding technique was used, primarily because of its reliability and repeatability. In the C4 process, the die is bonded in flip-chip fashion.

In the case of the FPIC/D, a removable land-grid socket is used that interfaces to the board using the Cinch Cinapse fuzzy-button contacts. The FPIC/R is housed in a more standard pin-grid array. □

PRICE AND AVAILABILITY

The FPIC/R and FPIC/D field-programmable interconnect components are available at single-piece pricing of \$1105 and \$2938, respectively. The /D is available in 60 days from receipt of order; the /R will ship in the third quarter. The development system costs \$15,000. Diagnostic-support software adds \$5000. The diagnostic package that supports the HP 16500 logic analyzers costs \$7500 on the Sun platform and includes the features of the standard diagnostic package. The FPCB-AT circuit board costs \$1538, while the general-purpose FPCB-GP2 goes for \$1154. Both are delivered in 60 days. For custom FPCB development, the FPCB Compiler, with Gerber interface, sells for \$15,000. It will be available in the third quarter.

Aptix Corp., 225 Charcot Ave., San Jose, CA 95131; Buck Feltman, (408) 428-6200. CIRCLE 512

HOW VALUABLE?	CIRCLE
HIGHLY	589
MODERATELY	590
SLIGHTLY	591

ASIC FAMILIES PACK UP TO 600,000 GATES THANKS TO 0.6 μM FEATURES

DAVE BURSKY

By shrinking the minimum feature size to 0.6 μm (0.45 μm effective) LSI Logic has developed three families of customer-definable circuits that can pack up to 600,000 usable gates. The largest chip has nearly 1 million raw gates on chip. The CMOS semicustom families include the LCA300K series of gate arrays, the LCB300K standard-cell library, and the LEA300K series of customer-definable masterslices.

Designs done in any of the three approaches can be migrated into either of the other two implementation schemes. As a result, designers can trade off turnaround time, density, and other factors. More than doubling single-chip integration over current ASIC offerings by most other companies, the 300K families are well suited for high-performance, high-complexity data processing, telecommunication, consumer, and military applications.

The LCA300K series includes 14 masterslice arrays that range in density from 10,000 to 500,000 usable gates. Either two or three levels of metal can be used to interconnect the gates. I/O pad counts on the arrays or standard-cell-based chips can exceed 800 pads, thus permitting the chips to readily handle multiple wide buses. On-chip phase-locked loops (PLLs) eliminate chip-to-chip clock skew for clocks up to 160 MHz and "balanced tree" clock distribution networks reduce cross-chip skew by up to 90% over arbitrary clock schemes.

NTL (NMOS transceiver logic) input/output buffers can be used in digital system designs to achieve backplane operating frequencies that are in excess of 75 MHz. Telecommunication designs can also use the NTL capability to implement applications such as Sonet with chip-to-chip frequencies of 156 MHz and greater. LSI Logic's proven PLL technology readily handles clock-recovery requirements for high-speed

data streams in FDDI interfaces.

Consumer applications, a major target for 300K families, can benefit from the low-power capability offered by the 3-V libraries. Circuits fabricated with the 3-V option can trim operating power consumption by as much as 65% as compared to the standard 5-V family. Delay-line memories and specialized audio and video interface cells allow optimized performance and reduced design cycle time for high-end systems.

Besides offering high performance, the LCA300K sports an advanced suite of development tools covering key aspects ranging from the I/O buffer options to final chip layout. The use of hierarchical block compilers allows efficient routing of complex designs with up to 500,000 gates. Systems that require special interfaces and terminations will benefit from a pseudo-ECL I/O option and embedded termination resistors. Such a combination has not been previously been available in other CMOS arrays.

FLEXIBLE DESIGN METHODS

Circuits designed with the LCB300K standard-cell family can pack up to 600,000 usable gates—approximately twice as many as most other cell-based offerings. On a single chip, designers can combine 200,000 gates, 512 kbits of SRAM, and 1 Mbit of ROM. With a power consumption of just 1 μW /gate/MHz (with a 5-V supply), the LCB300K eases power management in low-frequency systems. However, with so many gates on a chip, the total power could typically hit 10 to 20 W when running at 50 MHz.

To support such complex cell-based designs, the company has created enhanced tools to handle the iterative redefinition of chip floor plans based on completed hierarchical circuit block layouts. Those tools let the designer move between top-down and bottom-up methodology as the design evolves, thus achieving

better and more predictable performance.

Included in the tool set is a hierarchical block compiler that manages chip and interblock clock tree, power bus, and signal routing. The compiler also makes automatic adjustments as individual blocks are completed—that results in an optimum layout with minimal clock skew, efficient power busing, and inter-block signal bus routing. Additional tools, including advanced data-path and place-and-route packages keep chip area to a minimum while optimizing circuit performance.

LEA300X embedded-array option allows the designer to combine the performance and density of cell-based devices with the fast turnaround of gate arrays. The option lets designers embed large LCB300K cells—memory and complex logic functions—on a custom-size chip along with a significant number of uncommitted gates.

Unlike most embedded array offerings from other ASIC suppliers that step up in size using the fixed pad rings employed by the gate arrays, the LEA300K option allows designers to create custom-size chips, thanks to a pad-ring compiler that creates the desired I/O support. After a trial layout defines the minimum core size, the I/O compiler finishes the master-slice design and allows base wafer manufacturing and stocking to be done before the customer has completed signoff on post-layout ac performance.

Nonrecurring engineering (NRE) charges start at \$30,000 for the 300K family. Production charges depend heavily on package type selected and the quantity. Cell libraries are now available, with production slated for the first quarter of 1993.

LSI Logic Corp., 1551 McCarthy Blvd., MS: D102, Milpitas, CA 95035; for LCA products, call Peter Santos: (408) 433-7871; for LCB and embedded arrays, contact Todd Scott, (408) 433-7146. **CIRCLE 460**

486 WORKALIKE RETAINS 386SX BUS, PINOUT FOR NOTEBOOK PCs

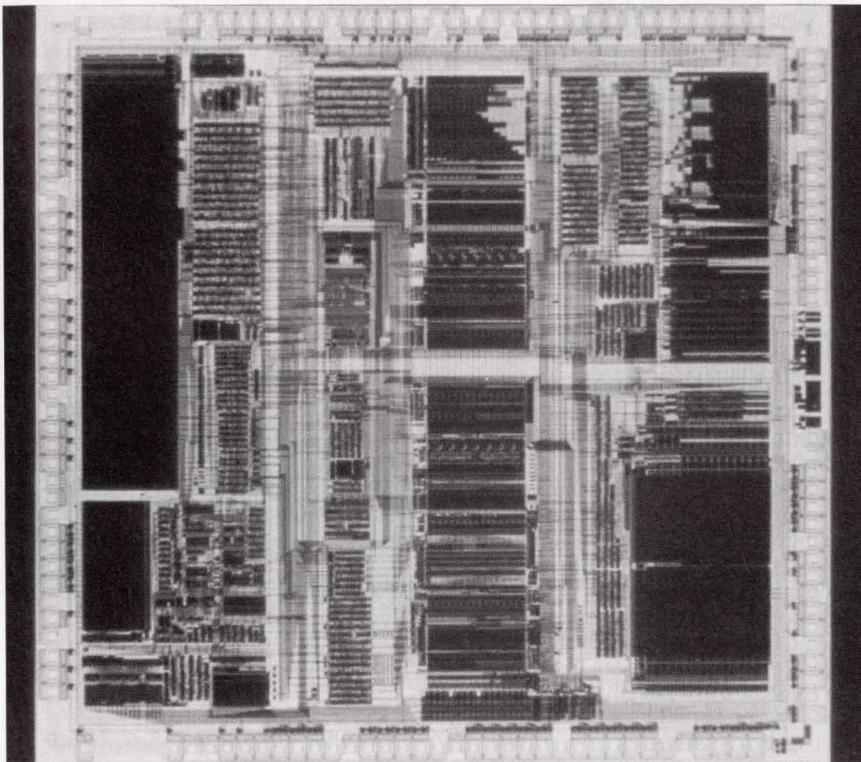
JON CAMPBELL

A 486SX-compatible microprocessor, with 32-bit internal and 16-bit external data paths, the Cx486SLC can drop into existing 386SX systems with only minor changes. The CPU chip, developed by Cyrix Corp., squeezes 486-instruction-set compatibility into a low-cost 100-lead plastic quad-sided flat package that is a superset of the 100-lead 80386SX pinout. In the new processor nine new signals are positioned on pins the 386SX leaves as "no-connect" pins. Built in an 0.8- μ m CMOS process, the CPU is first in a series of processor products with 486 performance and advanced features.

Judging from benchmarks run by Cyrix, the Cx486SLC is the fastest 16-bit-bus microprocessor available for use in high-volume notebook, pen-based, and entry-level desktop systems. It can be used for quick and easy upgrades of 386SX designs to 486-performance at price points competitive with 386SX or SL CPUs. Initial versions of the processor will run at 20 or 25 MHz, thus giving system designers more performance without the higher price tags.

Cyrix emphasizes that the CPU is a new design with an original architecture, not a clone of an existing CPU (see related story, page 30). But the company says that the new chip executes the complete 486SX instruction set and all operating systems designed for this instruction set, including DOS, Windows, and Unix. An alternate source for the 486 chip will likely be Texas Instruments, also expected to manufacture the 486SLC for Cyrix.

The Cx486SLC uses a single-cycle pipelined execution unit, 16-bit hardware multiplier, and tightly coupled 1-kbyte cache. Five pipeline stages allow successive instruction overlap for minimal instruction cycle times. Three versions of the CPU are being announced now. Designed for notebook PCs, the Cx486SLC-V25 and -V20 for 25 MHz and 20 MHz, respec-



tively, operate from a 3- or 5-V supply. Operating with 3 V, the processor consumes typically only 30% of that while operating at 5 V.

Suspend/resume allows power consumption to drop to the microwatt range. Current consumption is typically less than 2% of the operating current. Suspend mode can be entered either by a hardware or software-initiated action.

In notebook PCs, the Cx486SLC-25 has a Landmark version 2.0 CPU performance rating of 78 MHz, operating up to 2.5 times faster than the 386SX-25 CPU and up to 2.3 times faster than the 386SL-25 CPU. The new CPU's Norton SI V6.0 Index of 39.4 is 3.2 times faster than the performance of the 386SX-25 and 2.1 times that of the 386SL-25.

A 5-V 25-MHz version—the Cx486SLC-25—is aimed at desktop systems. According to the company, PC manufacturers can build an entry-level 486 system for the same price as a 386 system. Such systems

have a Landmark V2.0 test rating of 79 MHz—up to 2.5 times faster than traditional 386SX systems and 1.7 times faster than ones built with the IBM 386SLC. Other benchmarks for the 486SLC in a desktop PC are comparable to those obtained using the CPU in a portable PC.

Because of its 386 external form factor, the Cx486SLC can be interfaced to lower-cost 16-bit peripherals such as PC chip sets and coprocessors. The Cx486SLC CPU and 87SLC math coprocessor occupy 1/6th the space of the 486SX and its performance enhancement socket and consume 1/100th the power.

The Cx486SLC-25MP and Cx486SLC-V20MP go for \$119 in thousands. The Cx486SLC-V25MP is \$137 in the same quantities. These chips are being sampled now with general availability scheduled for later in the second quarter.

Cyrix Corp., P. O. Box 850118, Richardson, TX 75085-0118; (214) 238-8387.

CIRCLE 461

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PROGRAM KEYBOARD'S 23 FUNCTION KEYS

The Cherry 2100, an IBM-compatible computer keyboard, has 23 programmable function keys. It is designed for PC, XT, AT, and PS/2 computer systems for applications such as text processing, data input, programming, and software production. The operating mode is selected by a slide switch at the bottom of the keyboard.

Each function key can be assigned 10 memory locations so that 10 by 23 storage locations are possible. Memory capacity is about 2 kbytes. Output speed of program symbols is adjustable. All parameters are typically retained for 10 years.

The keyboard is built from 123 linear key modules using the company's "Gold Crosspoint" contact principle. Operating life of each key is more than 50 million operations, and mean-time-between-failure is better than 80,000 hours. The keyboard works in a synchronous data-transmission mode and a bidirectional serial synchronous interface that communicates with the system via a clock and data line.

The Cherry 2100 operates at only +5 V and has a current consumption of typically 200 mA. The keyboard is now available. Price will be given on request.

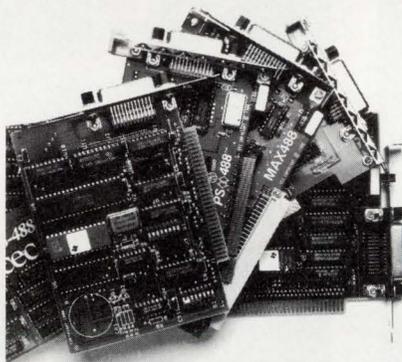
Cherry Mikroschalter GmbH, Cherrystr., D-8572 Auerbach, Germany; 00 49 9643-180; fax 00 49 9643-18262. CIRCLE 462

HIGH-END SYSTEM OFFERS LOE-END PRICE

The MicroFrame computer boasts mainframe power at the price of a high-end PC. The tower-configuration system is based on a 32-bit bus. Up to four 486 processors can be employed. Standard features of the computer include

32 Mbytes of zero wait-state memory, 256 kbytes of cache memory, and a 32-bit SCSI-II host I/O adapter with 4 Mbytes of cache. Peripherals supplied include a 1.2-Gbyte SCSI hard drive, an internal CD-ROM drive, an internal 240-Mbyte tape drive, two high-density floppy drives, a 9600-baud fax-modem, and a 17-in. Super VGA color monitor. MS-DOS and Windows comes bundled with the system. The MicroFrame sells for \$13,995.

Fox Computers, P. O. Box 1846, Big Bear Lake, CA 92315; (714) 866-5700. CIRCLE 463



You get fast hardware and software support for all the popular languages. A software library and time saving utilities are included that make instrument control easier than ever before. Ask about our no risk guarantee.

EISA-BASED PC ADDS CLOCK-DOUBLING 486

One of the first systems to take advantage of Intel's clock-doubling processor technology is the EISA-based Systempro/LT 486DX2/50. Its processor runs at 50 MHz internally, yet is supported by 25-MHz external components. Therefore, users can benefit from the processing power and computing speed of 50-MHz technology at a lower price than a PC using 50-MHz components for both internal and external communications. In addition to the processor's 8 kbytes of internal cache memory, Compaq adds 256 kbytes of secondary two-way set-associative write-back cache. Many different memory and video configurations are available, with prices starting at \$8199.

Compaq Computer Corp., P.O. Box 692000, Houston, TX 77269; (713) 370-0670. CIRCLE 464

486 NOTEBOOK HAS DUAL-DISPLAY CAPABILITY

The Slimnote notebook PC, packaged with an 80-Mbyte hard disk and 4 Mbytes of main memory, is based on a 33-MHz i486 microprocessor. It measures 8.5 by 11 by 1.7 in. and weighs just 5.8 lbs. One feature of the system is its simultaneous dual-display capability. What's displayed on the 10-in., 64-shade liquid-crystal display can simultaneously be displayed on an external Super VGA monitor. Thus, the computer can be used for presentations. Users can add up to 20 Mbytes of memory and a modem. The Slimnote sells for \$3499.

Twinhead Corp., 1537 Centre Pointe Dr., Milpitas, CA 95035; (408) 945-0808. CIRCLE 465

SBUS BOARD ACCELERATES GRAPHICS

The single-slot GXTRA/W SBUS graphics accelerator boasts a resolution of 1600 by 1280 pixels and can draw 100 Mpixels/s for all 2D applications. It supports draw, fill, text, and bit-block transfer operations at the full speed of interleaved page-mode VRAMs. The board runs most Sun software, including SunView and OpenWindows. The board is designed around the Weitek W8720 graphics controller. Prices for single units start at \$3750.

Tech-Source Inc., 442 S. North Lake Blvd., Suite 1008, Altamonte Springs, FL 32701; (407) 830-8301. CIRCLE 466



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Burlington, MA. 01803

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NEW PRODUCTS

SOFTWARE

SOFTWARE TOOLS AID FUZZY-LOGIC DESIGN

Through a relationship with Apronix Inc., San Jose, CA, Motorola has released a software development tool for fuzzy-logic design. The Fuzzy Inference Development Environment (FIDE) tools enable designers to give standard microcontrollers fuzzy logic capabilities. Initially, the 68HC05 and 68HC11 families will be supported. Future plans call for support of the 68HC16 and 68300 microcontroller families and the 56000 DSP family.

The FIDE application tools are easy to use and offer greater flexibility in product design compared to conventional software tools. Users can design and simulate an entire dynamic system, including microcontroller-specific hardware, making it easier to evaluate design scenarios. The general-purpose tools go through the stages of system design, development, testing, debugging, and code generation.

One of the unique features of the tools is its fuzzy inference language which is functional and supports many fuzzy operators, inference methods, and defuzzification techniques. The real-time code generator, which efficiently creates object code, generates assembler source code for Motorola chips. The analyzer features a 3D surface view to supply a clear view of the response function. The tool can also trace from a point on the surface to the originating source code.

Motorola Inc., 6501 William Cannon Drive West, Austin, TX 78735; (512) 891-3938. CIRCLE 467

■ RICHARD NASS

CREATE PROTECTED-MODE WINDOWS APPLICATIONS

The upgraded DPMI-16 DOS Extender now comes with its own DOS-protected-mode interface (DPMI). The product allows applications developers to create protected-mode applications that run automatically in DOS, Windows 3.0, Desqview, Windows NT, and OS/2 2.0. Developers can also create programs to handle physical devices and interrupts completely with the protected mode. Other features include the ability to address 16 Mbytes of code and data space; to run as a DPMI host, independent of an existing server; easy

communication to real-mode tasks; interrupt handling; and the use of dynamically linked libraries (DLLs) in DOS.

The DPMI-16 is available now for \$695. Current users can upgrade for \$300. The kit comes with protected-mode libraries for the Borland and Mi-

crosoft compilers, an enhanced debugger, and a tune program to optimize 286 systems. Support is included for Borland C++ and Microsoft C and Fortran.

Ergo Computing Inc., One Intercontinental Way, Peabody, MA 01960; (508) 535-7510. CIRCLE 468

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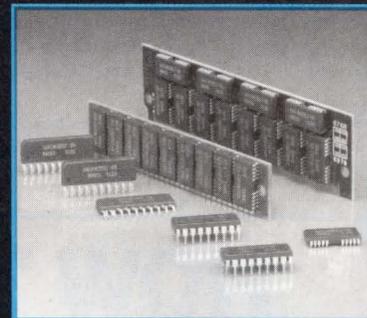
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NEW PRODUCTS

INSTRUMENTS

SYSTEM DOES OVER 40 SEMICONDUCTOR TESTS

The Model 8800 discrete semiconductor tester is a simple-to-use, inexpensive standalone unit. The system performs more than 40 parametric measurements or go/no-go tests for transistors, diodes, MOSFETs, regulators, triacs, zeners, SCRs, and J-FETs in a wide range of packages. The devices can be tested to 1200 V and up to 5 A, with resolutions to 1 mV and 0.1 nA. Only four universal test fixtures are needed. An IEEE-488 port connects the tester to an automatic device handler, computer, printer, terminal, or data logger. A Quick Set function offers a fast way to configure a one-time test setup, and a battery-backed memory stores user-written test routines for repeated use. The standalone instrument weighs 16 lbs. and measures 4.5 in. high by 17 in. wide by 16.5 in. deep. The Model 8800 costs \$6900 and comes with a one-year warranty.

Information Scan Technology Inc.,
487 Gianni St., Santa Clara, CA 95054;
(408) 748-3771. **CIRCLE 469**

DEVICE PROGRAMMERS ARE FULLY INTEGRATED

The ProMaster Series consists of five integrated turnkey systems for handling, programming, testing, and marking of programmable ICs. The ProMaster 2000 offers programming, testing, and labeling for DIP devices to 44 pins. The ProMaster 3000 supplies the same functions for surface-mounted or DIP devices. The ProMaster 7000 performs programming, testing, and laser marking for surface-mounted or DIP ICs. The 3000 and 7000 come in either 44- or 88-pin versions. The series uses programming algorithms approved by device manufacturers. Easy user-configurable changeovers reduce downtime between projects, and automated control software cuts training costs. Prices range from \$63,915 for the ProMaster 2000 base unit with 44-pin capability to \$124,645 for the 88-pin version of the ProMaster 7000 base unit. Delivery is in 8 weeks.

Data I/O Corp., 10525 Willows Rd. NE,
Redmond, WA 98073-9746; (800) 332-8246. **CIRCLE 470**

500-MHZ SCOPE DIGITIZES AT 2 GSAMPLES/S ON 4 CHANNELS

A pair of high-speed, wide-bandwidth digital scopes offer advanced triggering capabilities that suit them for design and debugging of fast digital circuits. The 2-channel TDS 620 and 4-channel TDS 640 fea-



ture 2-Gsample/s digitizing simultaneously across all channels and a 500-MHz bandwidth.

The high sample rate makes it possible to analyze single-shot signals accurately and measure critical timing margins between multiple signals. And the wide bandwidth allows the scopes to capture even fast logic transitions accurately.

With the scopes' advanced logic and fault-triggering capabilities, users can easily capture glitches, noise, or timing violations on nonrepetitive signals. The instruments can trigger on faults or glitches as short as 2 ns, capture race conditions using the unique runt-pulse mode, and find design problems with the time-qualified pattern or state triggering features.

The scopes come with P6205 active probes, which feature a 750-MHz bandwidth. The probes have an impedance of less than 2 pF and 1 M Ω , compared with a capacitance of 10 pF for a typical passive probe. They draw their power from the scope. A graphical interface simplifies operation, and on-board processors perform fast signal averaging, waveform math, interpolation, and automatic measurements.

The TDS 620 costs \$13,540 with two P6205 active probes and the TDS 640 costs \$20,980 with four P6205 probes. Without the probes prices are \$12,500 and \$19,000, respectively. Delivery is 6 weeks after ordering.

Tektronix Inc. Test & Measurement Group, P. O. Box 1520, Pittsfield, MA 01202; (800) 426-2200. **CIRCLE 471**
■ JOHN NOVELLINO

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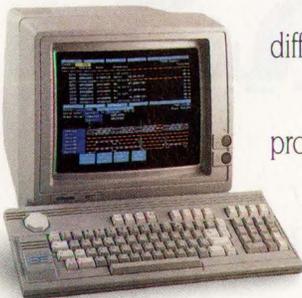
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SURFACE-MOUNTED FUSE QUICKLY GUARDS BOARDS

A line of thin-film, mini surface-mounted fuses provides more precise fusing control in a much smaller package than conventional wire fuses. The Accu-Guard fuses offer tightly controlled electrical characteristics, including a precise fusing point, fast reaction time, extremely accurate current ratings, and a high open resistance of more than 20 M Ω . Ten ratings are available from 200 mA to 2 A at 32 V. The devices come in EIA-standard 1206 packages and are on tape and reel. Typical pricing is \$.25 for 10,000 pieces. Delivery is from stock to six weeks.

AVX Corp., 801 17th Ave. South, Myrtle Beach, SC 29577; (803) 946-0562. CIRCLE 472

MINI TUBULAR SOLENOIDS PACK HEALTHY PUNCH

Boasting a diameter of only 1 in., the L-10 series tubular solenoids kick with up to 208 ozs of force. Two standard lengths of 1-1/8 and 2 in. are available. The units are also offered in push and pull operation types. Both types come with 6-, 12-, 24-, or 110-V dc coils. Other voltages and custom features are available. Standard wattage ratings are from 5 W continuous duty to 100 W pulse duty. Typical pricing is \$8 in OEM lots. Delivery is from six to eight weeks, depending on quantity.

Liberty Controls Inc., 500 Brookforest Ave., Shorewood, IL 60435; (815) 725-241. CIRCLE 473

ULTRABRIGHT AMBER LEDs STAND OUT IN SUNLIGHT

A series of ultrabright amber and reddish-orange LEDs is ten times brighter than existing amber types—bright enough to be visible outdoors in sunlight. The HLMA Series LEDs owe their brightness to aluminum indium gallium phosphide technology, which represents a breakthrough in material technology for LED manufacturing.

With the recently developed AlIn-GaP technology, Hewlett-Packard can fabricate semiconductor devices that emit extremely bright light in a wide range of wavelengths. Current products emit 590 nm (amber) and 620 nm (reddish-orange). Future devices will include ultrabright green LEDs and a variety of lamp and display modules in a range of ultrabright colors.

The amber HLMA-BL00 LED offers a highly focused viewing angle of 3° and an average intensity of 8.4 candela

at 20 mA. The amber HLMA-CL00 has a slightly wider viewing angle at 10° and an intensity of 1.3 candelas at 20 mA. Both of these devices are suited for outdoor signs intended to be seen from a distance, such as highway signs, and for indoor uses such as low-power laser replacements and front panels for medical instruments.

The HLMA-DG00 and -DL00 LEDs come in reddish-orange or amber, respectively, with a viewing angle of 34° and a typical on-axis intensity of 650 millicandela at 20 mA. Their wide viewing angle suits them for moving message signs and automotive lighting.

Volume shipments of the HLMA Series LEDs are expected to start in 1993. Designer kits (HLMA-SMPX) are available at \$50 each.

Hewlett-Packard Co., 19310 Pruneridge Ave., Cupertino, CA 95014; (800) 752-0900. CIRCLE 474

■ DAVID MALINIAK

TTL-RUN ATTENUATOR IS ACCURATE TO 1000 MHZ

A TTL-controlled attenuator is available with steps from 4 to 28 dB and accuracy from 10 to 1000 MHz. The unit is available in a hermetically sealed TO-8 case (model TOAT-4816) or in an SMA-connector version (model ZFAT-4816). The 50- Ω device operates with a 6- μ s switching time and handles power lev-

els up to +15 dBm. Each unit includes three discrete attenuators (4, 8, and 16 dB) that are switchable to supply seven attenuation levels of 4, 8, 12, 16, 20, 24, and 28 dB. Step accuracy is 0.2 dB. Pricing is \$59.95 for the plug-in unit and \$89.95 for the connectorized type. Delivery is from stock.

Mini-Circuits, P. O. Box 350166, Brooklyn, NY 11235; (718) 934-4500. CIRCLE 475

40 YEARS

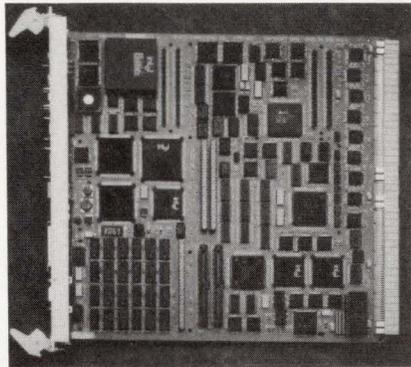
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RUN PC SOFTWARE ON A FUTUREBUS+ CPU BOARD

The 80486 microprocessor is typically implemented on an ISA or EISA bus. By building a Futurebus+ board with the 486 processor, users can take advantage of Futurebus+ features while running PC-based software. The FCPU-486, from Force Computers Inc., is designed around the Futurebus+ architecture and features a 33-MHz processor and 16 Mbytes of dynamic RAM.

The CPU board targets such applications as network and storage servers, databases, telecom and I/O controllers, neural networks, and CAD and CAE systems. Futurebus+ offers a bus bandwidth of more than 1 Gbyte/s, compared with the 33 Mbytes/s of the EISA bus. A Futurebus+ backplane can support up to 14 modules in a cache-coherent environment, supplying the potential for multiprocessing systems using several 486 processors.

The FCPU-486 board comes with an



EISA bus interface, with two or four expansion slots. An Ethernet interface supplies additional I/O. The board conforms to Profiles A and B of the Futurebus+ specification. Available in the third quarter, it sells for \$9950.

*Force Computers Inc., 3165 Winchester Blvd., Campbell, CA 95008; (408) 370-6300. **CIRCLE 476***

■ RICHARD NASS

MCA BOARD SUPPORTS 1600-BY-1280 RESOLUTION

The latest member of the Piranha family, the UDC-8000-TI graphics controller, fits the Micro Channel Architecture (MCA) form factor for the IBM RS/6000 and PS/2 Models 90 and 95. The board, which can execute 40 MFLOPS, has a TI TMS34020 graphics processor

and TMS34082 floating-point unit. Images up to 1600 by 1280 pixels can be displayed. An optional Motorola 20-MHz VSB bus can be incorporated onto the board to supply transfer rates up to 20 Mbytes/s. The UDC-8000-TI starts at \$4695.

*Univision Technologies Inc., Three Burlington Woods, Burlington, MA 01803; (617) 221-6700. **CIRCLE 477***

USE CONTROLLER EXTENSION AS I/O MODULE

The IDAD controller extension module can be used as an I/O module together with PEP's intelligent universal controllers. The IDAD is available in three different A-to-D versions with either 12-, 14-, or 16-bit resolution and handles 16 single-ended or 8 differential channels. Throughput is up to 100 KHz with the 12-bit and up to 50 KHz with the 14- and 16-bit versions. The charge-balanced converter's self-calibrating facility and programmable gain, together with a voltage reference with 0.6 ppm/°C temperature coefficient, makes for high accuracy.

The IDAD has four optional 12-bit D-to-A channels. With the additional 16 digital I/O lines, complete analog measurement and data-acquisition systems can be realized. Optoisolation between the analog and digital section of the IDAD is standard for the 14- and 16-bit versions and optional for the 12-bit version. The analog circuits can be tuned via the built-in test and calibration facility. An internal reference voltage source can be used to determine the exact gain of the amplifiers. Available now, the IDAD modules start at \$770.

*PEP Modular Computers, P. O. Box 1652, D-8950 Kaufbeuren, Germany; 00 49 8341-43020. **CIRCLE 478***

■ JOHN GOSCH

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NEW PRODUCTS

COMPUTER BOARDS

MILITARY HOPS ON MEZZANINE BUS

Mezzanine buses have been widely used throughout the commercial VMEbus community to add functionality to a host board without taking up a slot in the backplane. Until now, military-specification boards were exempt from the advantage that mezzanine buses offer because the buses couldn't meet the strict requirements of the military specifications. That's now changing with Radstone Technology's Military Expansion bus (MXbus).

The MXbus, which fully complies with military specifications, ensures mechanical stability in all three board axes. Stability is directly related to other considerations, including the number of fixing points for the mother-board-daughterboard combination and selecting the proper pc-board material and thickness. Ensuring an even mass distribution over the module's area requires selecting the correct packaging technologies.

These factors can affect the module's response to mechanical excitation. The overall design goal is to increase the module's quality factor (Q), thus supplying a stiffer module that's less susceptible to the flexing that causes mechanical stress on the soldered connections.

The MXbus' machined gold pin-and-socket arrangement of connectors remains electrically conductive, retaining a low contact resistance when subjected to high levels of mechanical shock and vibration, as well as wide and rapid swings in temperature and humidity. The actual configuration supplies multiple contacts per pin, ensuring that the proper connection is made. In addition, the contacts are protected in a base strip material that's more efficient per unit area than connectors with integrated shell housings.

The MXbus architecture isn't limited to 680X0-based processors, although that's how Radstone will first implement it. The existing MXbus implementation and protocol are independent of the CPU type, whether it's synchronous or asynchronous. By adding a line on the MXbus to define the bus operation type, an MXbus module can reside on any board that supports the interface.

**Radstone Technology Corp., 20
Craig Rd., Montvale, NJ 07645;
(800) 368-2738. **CIRCLE 479****

RICHARD NASS

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INDEX OF ADVERTISERS

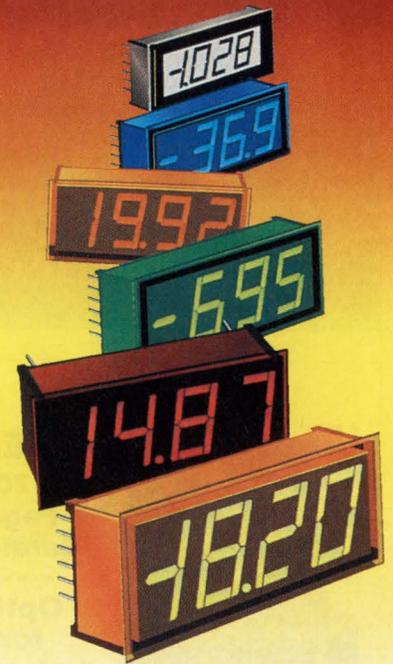
ADVERTISER	READER SERVICE U.S./OUTSIDE U.S.	PAGE NUMBER	ADVERTISER	READER SERVICE U.S./OUTSIDE U.S.	PAGE NUMBER
ACCEL Technologies	401	124	Motorola Semiconductor		
Actel	220, 221	106-107*	Products	◊	109*
Advanced Micro Devices	80, 81	2-3	Murietta Circuits	168, 169	88
	222, 223	10-11	National Instruments	190, 191	19
Altera	172, 173	53*	National		
American NeuraLogix	411	125	Semiconductor	◊	16-17
Analog Devices	84, 85	58-59	Needham's Electronics	408	125
	86, 87	112-113	NMB Technologies	132, 133	119
Apex Microtechnology	88, 89	27	Nohau	403	124
AT&T	90, 91	64-65*	Orbit Semiconductor	228, 229	96B-96D**
Atmel	134, 135	37	P-CAD	◊	48A-48B*
AVX	174, 175	75	Pacific Hybrid	170, 171	69
B&C Microsystems	412	125	Philips Semiconductor	300	33-35**
Capital Equipment	92, 93	118	Philips Test		
Comdisco	94, 95	70	& Measurement	◊	53**
Comlinear	216, 217	84	Pico Electronics	136, 137	89, 94
Compass			Power Convertibles	192, 193	8
Design Automation	96, 97	6-7	Powerex	138, 139	66
Cybernetic Micro			Professional Digital		
Systems	176, 177	14	Components	406	125
Cypress Semiconductor	◊	Cover IV	Quality Semiconductor	140, 141	99
Dale Electronics	98, 99	93	Qualogy	194, 195	18
Datel	◊	72A-72D*	Rolyn Optics	402	124
	178, 179	125	Samsung Electronics	142, 143	12-13**
Digi-Key	102, 103	83*	Samsung		
Digital Equipment	200, 201	54-55	Semiconductor	196, 17	12-13*
Dow Plastics	208, 209	46-47	Sharp		
Echelon	104, 105	50-51	Microelectronics	144, 145	96B-96D*
Emulation Technology	404	125	Siemens AG	146, 147	106-107**
Epson America	180, 181	40*	Siemens Components	148, 149	34-35*
Fenner Industrial			Signal Processing		
Controls	182, 183	120	Technology	198, 199	77
Fortron Source	206, 207	8	Siliconix	212, 213	9
Harris Semiconductor	202, 203	38-39	Silicon Systems	150-151,	
Headland Technology	204, 205	79		158-159	24-25
Hewlett-Packard Co.	224	1	Simtek	152, 153	68
	226, 227	42	Sony Semiconductor	154, 155	103*
	184, 185	62-63	Spectrum Software	230, 231	96F
	106, 107	100*	Stanford Research	214, 215	33*, 40**
Huntsville			Star Semiconductor	156, 157	30
Microsystems	108, 109	128	Systech Research	◊	111
Innovative Software			Tektronix	164, 165	61
Designs	410	124		162, 163	104
International				160, 161	121
Microcircuits	407	125	Telton	405	124
International Rectifier	186, 187	22	UTMC	166, 167	82
Intusoft	409	124	Vicor	168, 169	87
Lambda Electronics	112, 113	80A-80D*	Xilinx	◊	56A-56H
Lattice Semiconductor	188, 189	Cover II	Z-World Engineering	400	125
Mesago, Messe					
& Kongress GmbH	114, 115	122-123**			
MicroSim	116, 117	95			
Mini-Circuits Laboratory,					
a Div. of Scientific					
Components Corp.	120, 121	15			
	122, 123	20-21			
	118, 119	28-29			
	126, 127	90			
	124, 125	Cover III			

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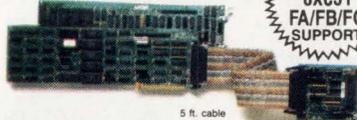
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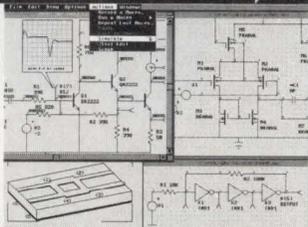
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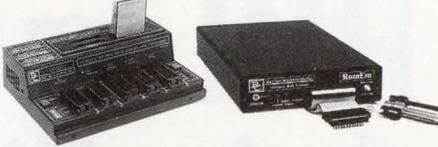
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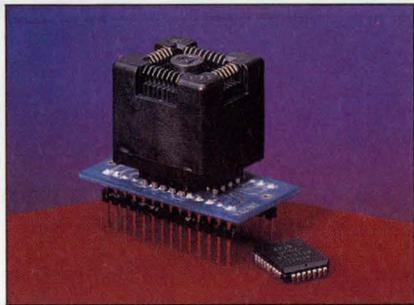
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April 16	3/20/92
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May 14	4/17/92
May 28	5/1/92
June 11	5/15/92
June 25	5/29/92
July 9	6/12/92
July 23	6/26/92
August 6	7/10/92
August 20	7/24/92
September 3	8/7/92
September 17	8/21/92
October 1	9/4/92
October 15	9/18/92
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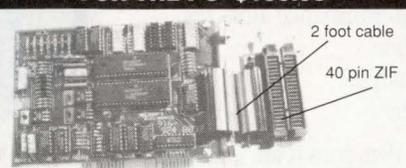
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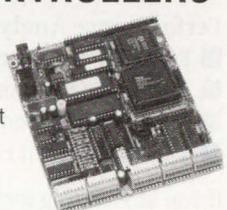
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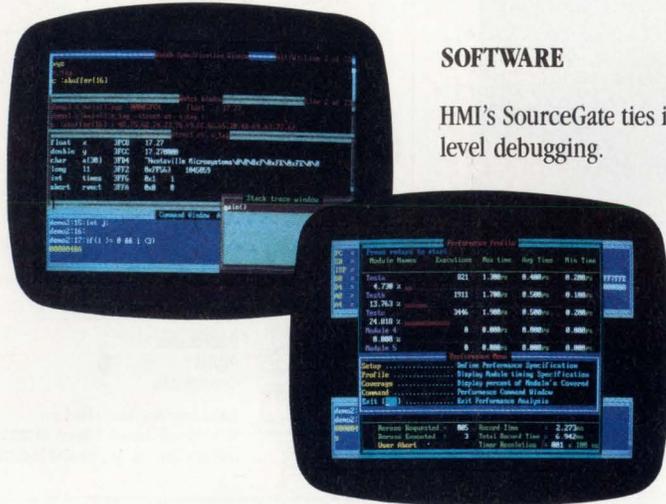
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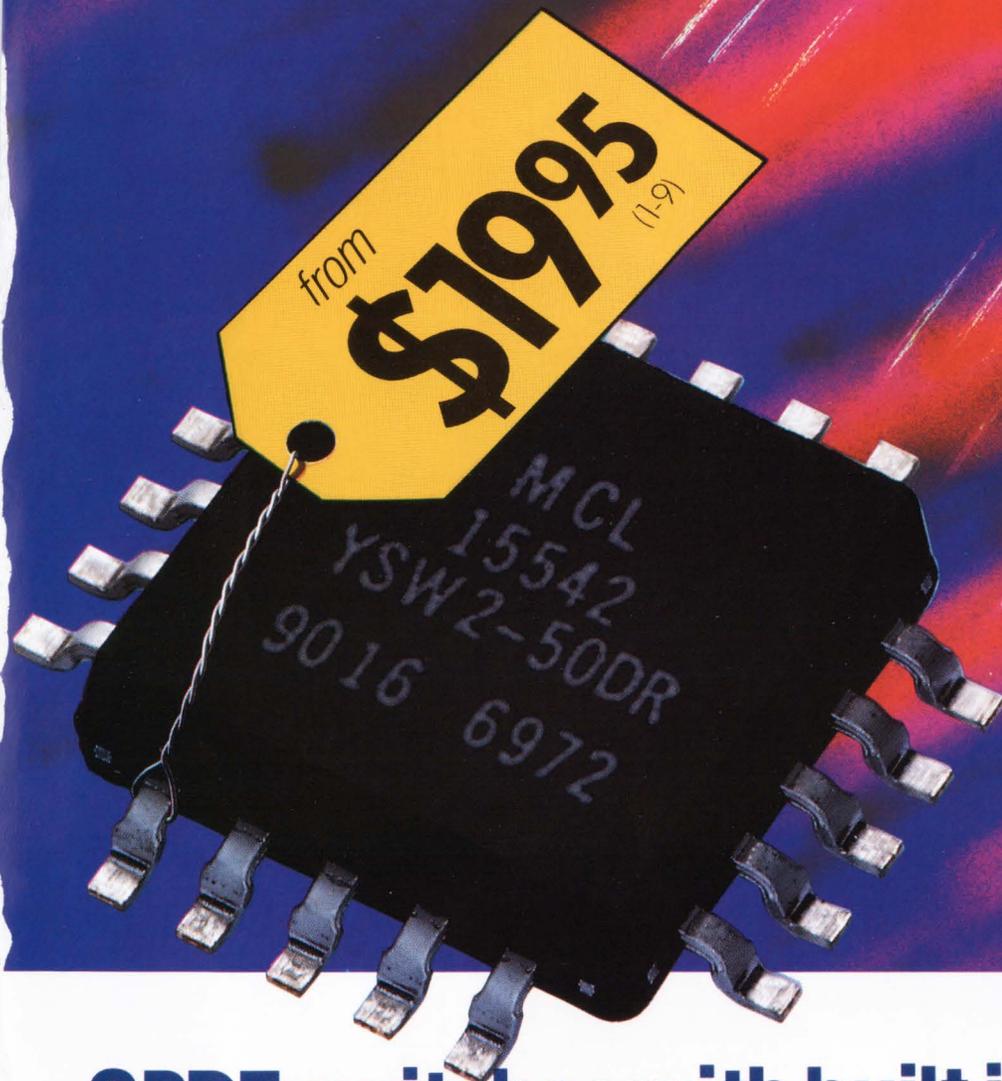
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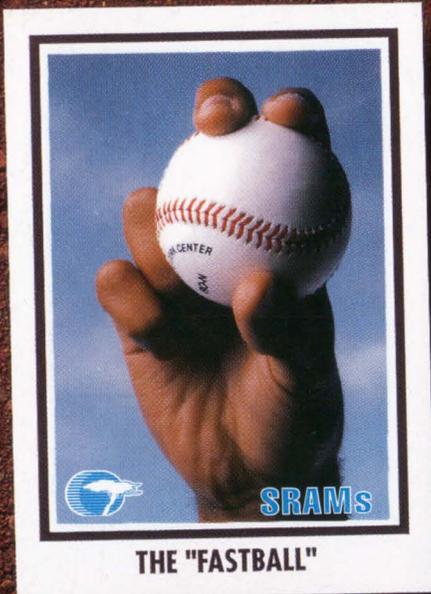
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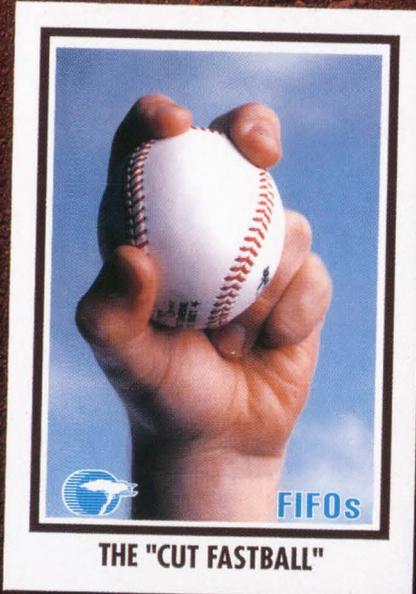
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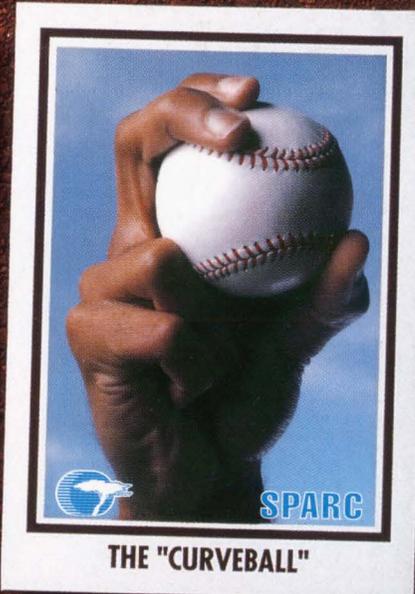
F141 REV. C



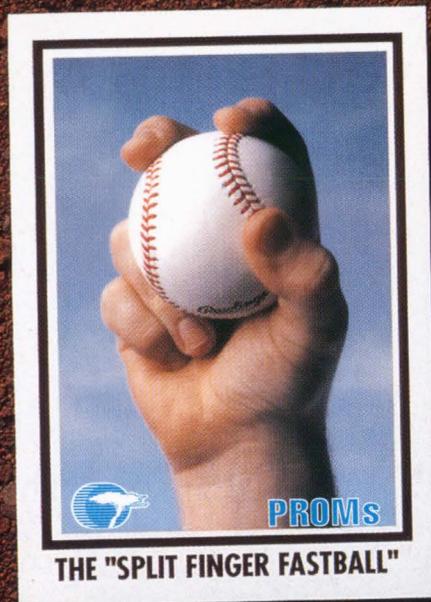
Scorching access times and a wide range of densities make our SRAMs untouchable. 12 ns 256Ks, 8 ns 64Ks, 4 ns 16Ks and more.



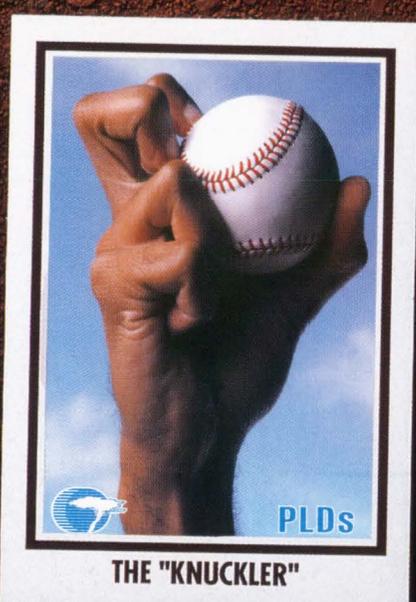
At 70 MHz, with read/write clocks and synchronous flag features, our FIFOs and Bi-FIFOs move data in and out quickly.



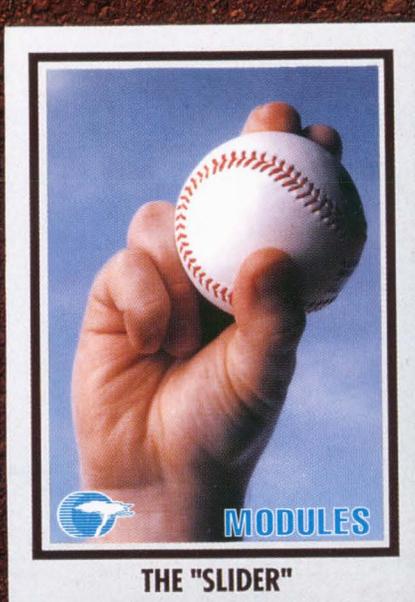
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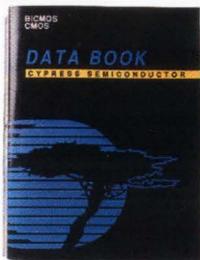


PLDs allow crafty designers to mix Gate Array density with 40 MHz performance; even support 125 MHz state machines.



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