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MARCH 19, 1992

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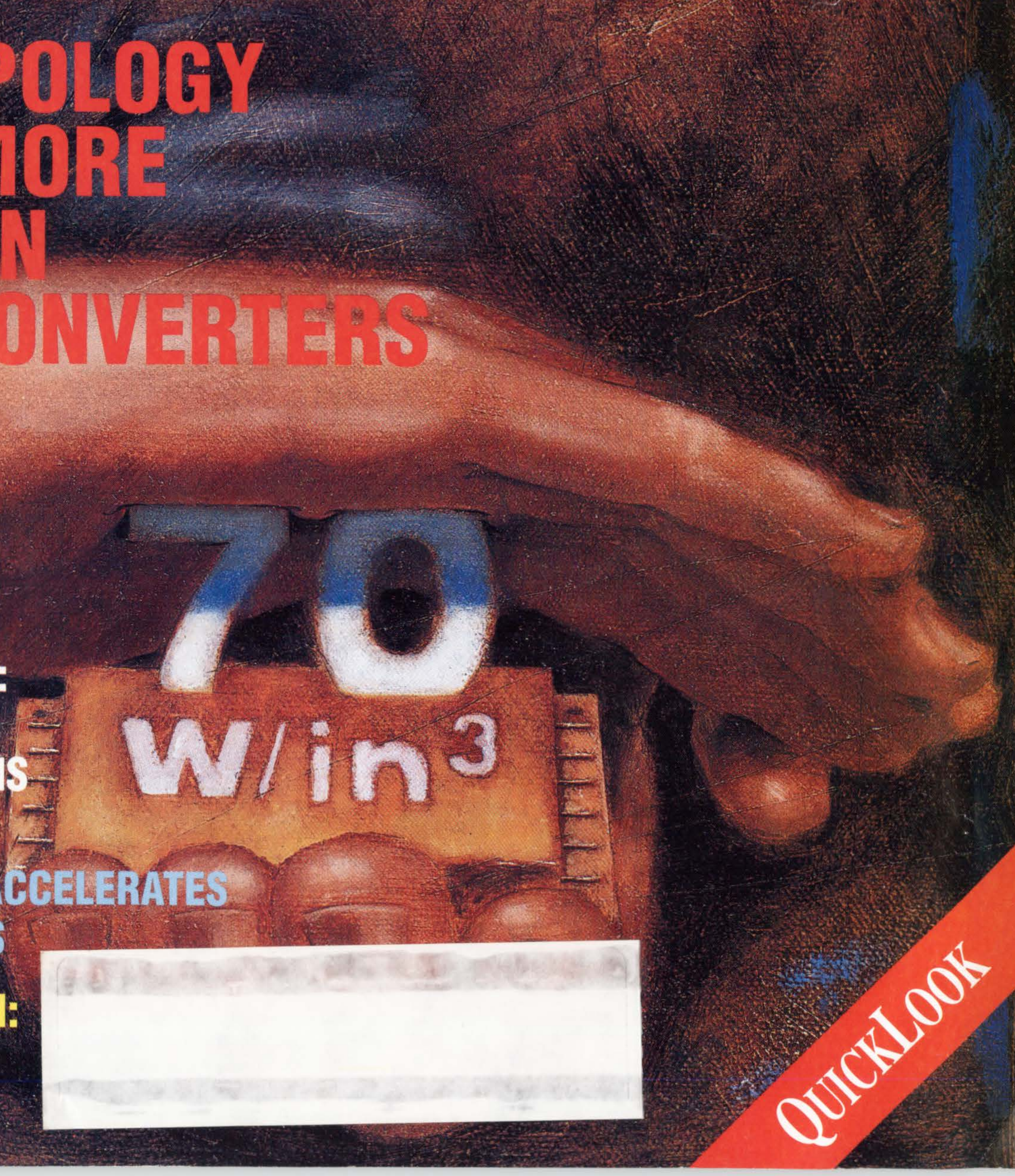

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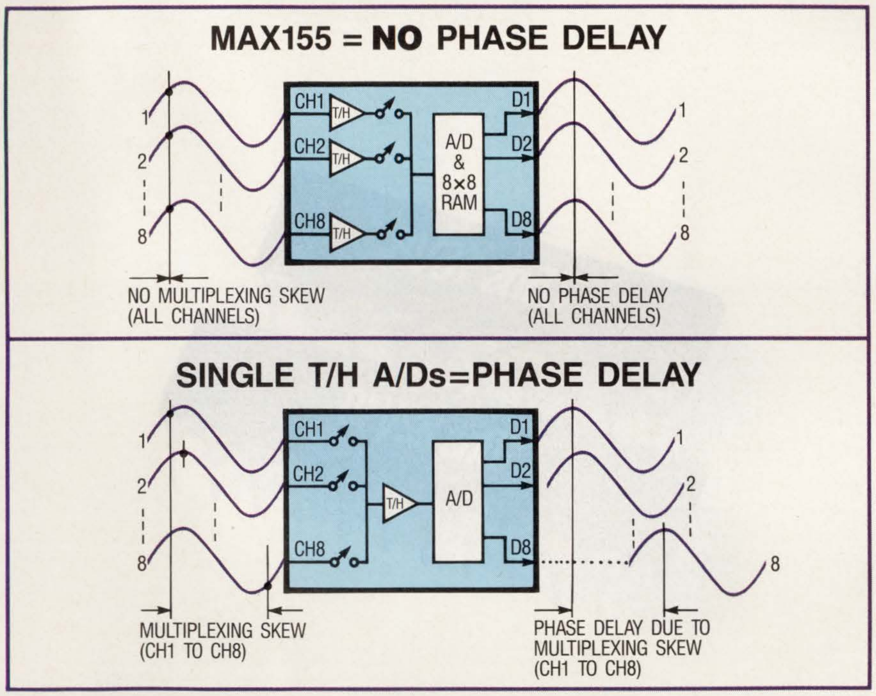

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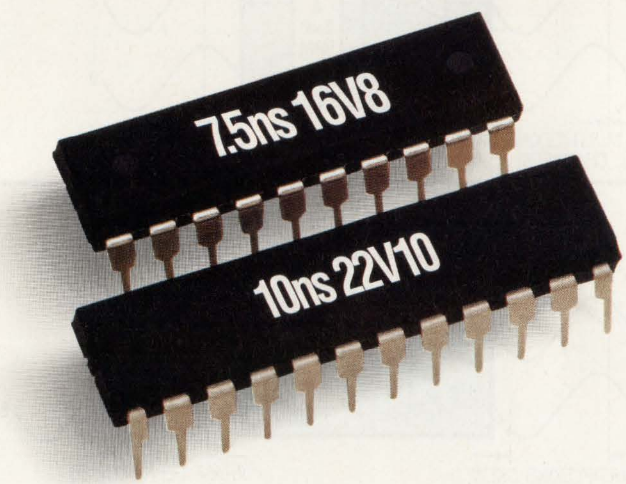

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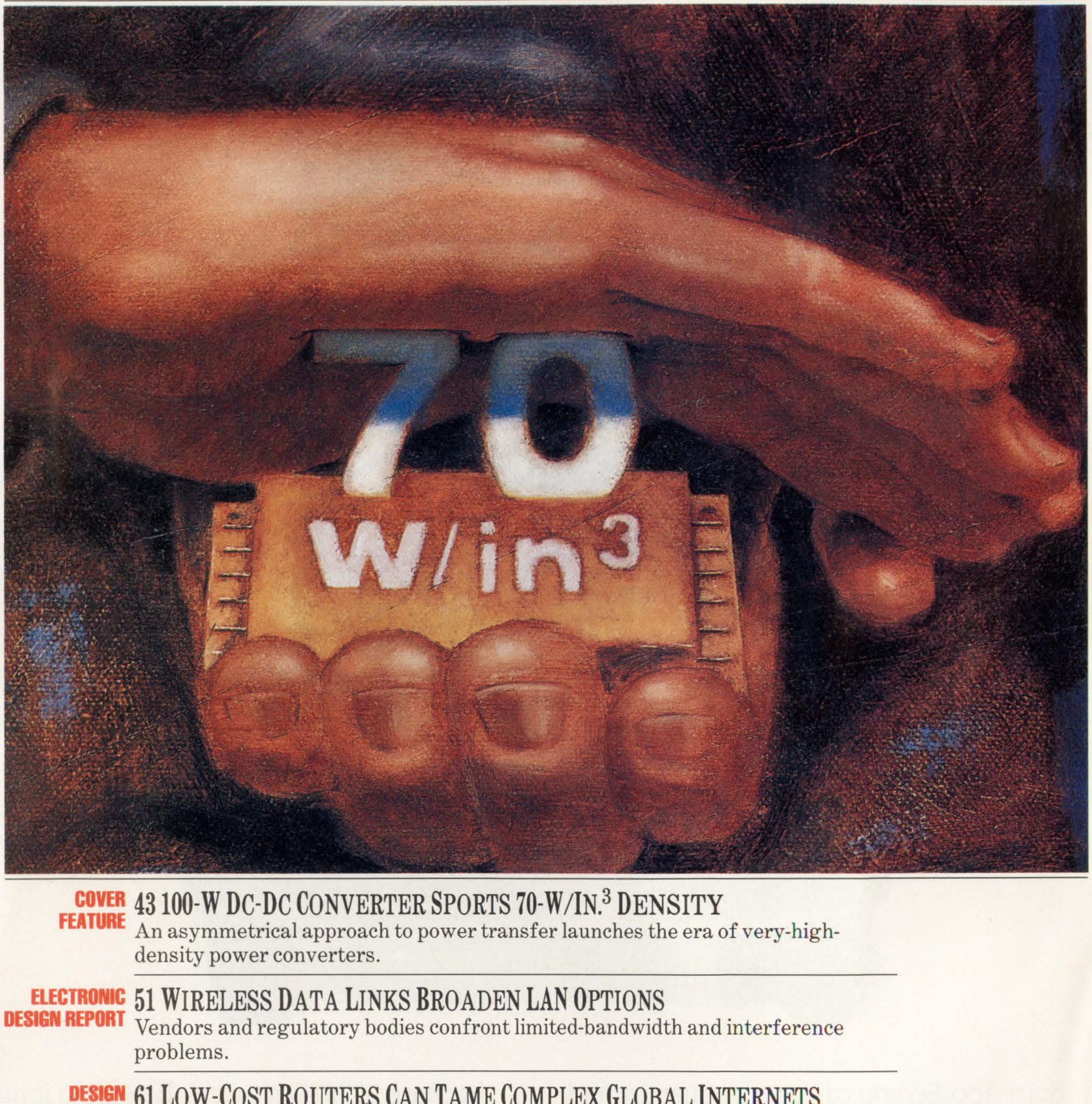

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- Modeling op-amp noise with Spice macromodels
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- Logic-emulation software that promotes parallel hardware-software development
- Plug-in pc boards that aid in mixed-signal processing
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NEW INDUSTRY STANDARD

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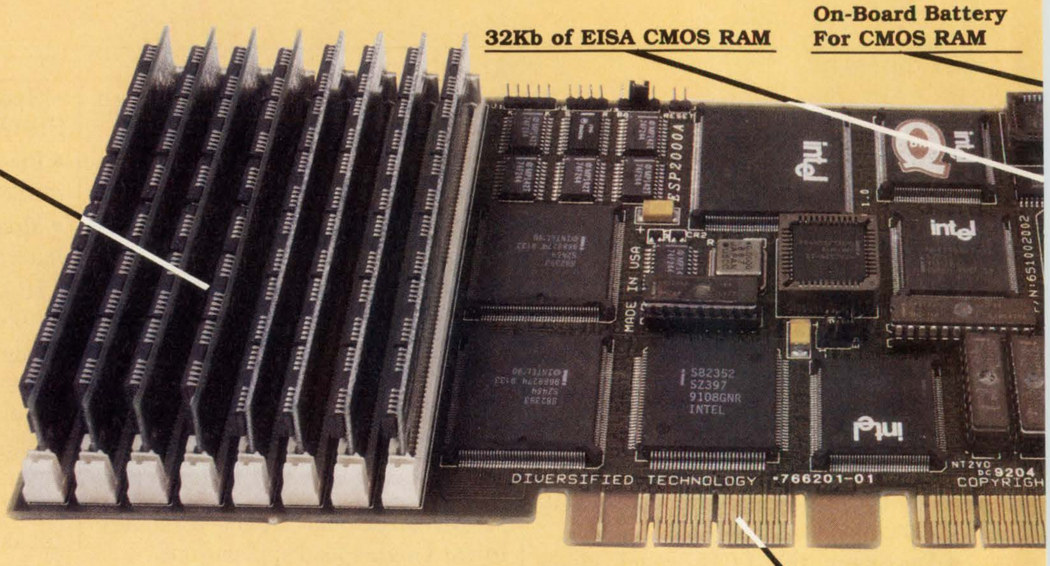

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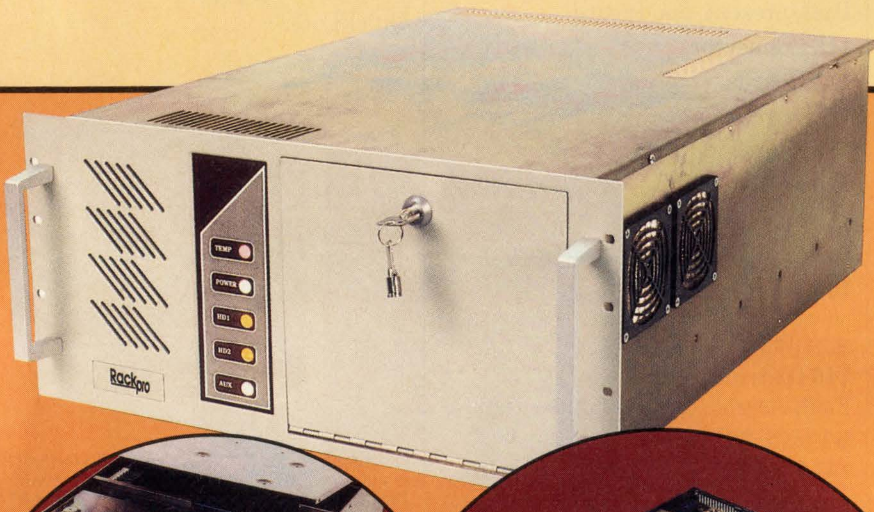

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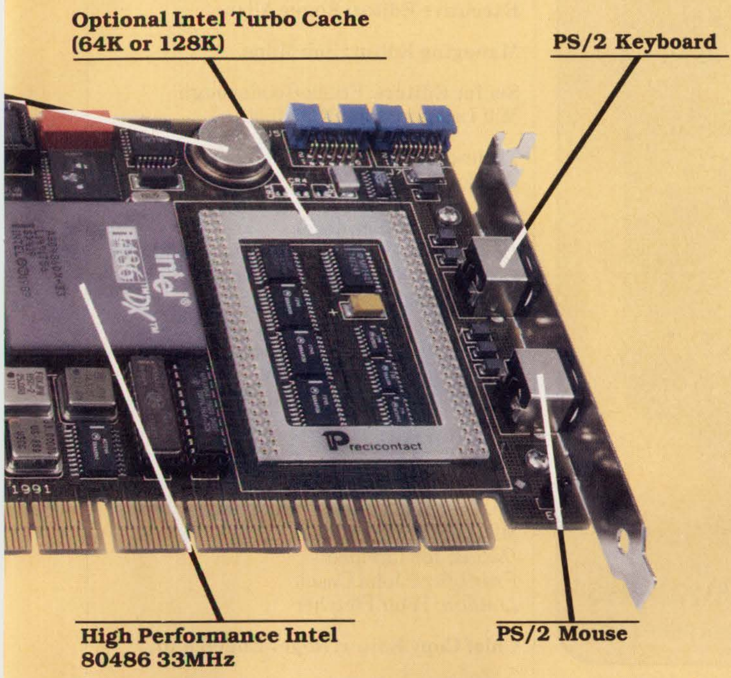

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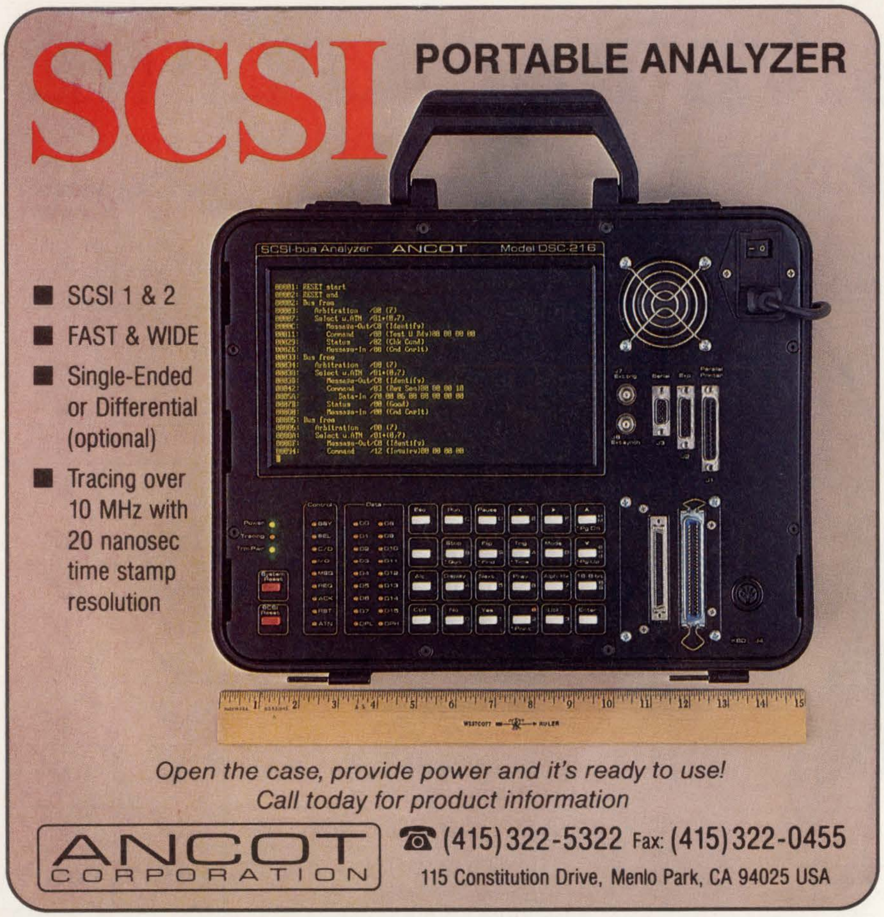

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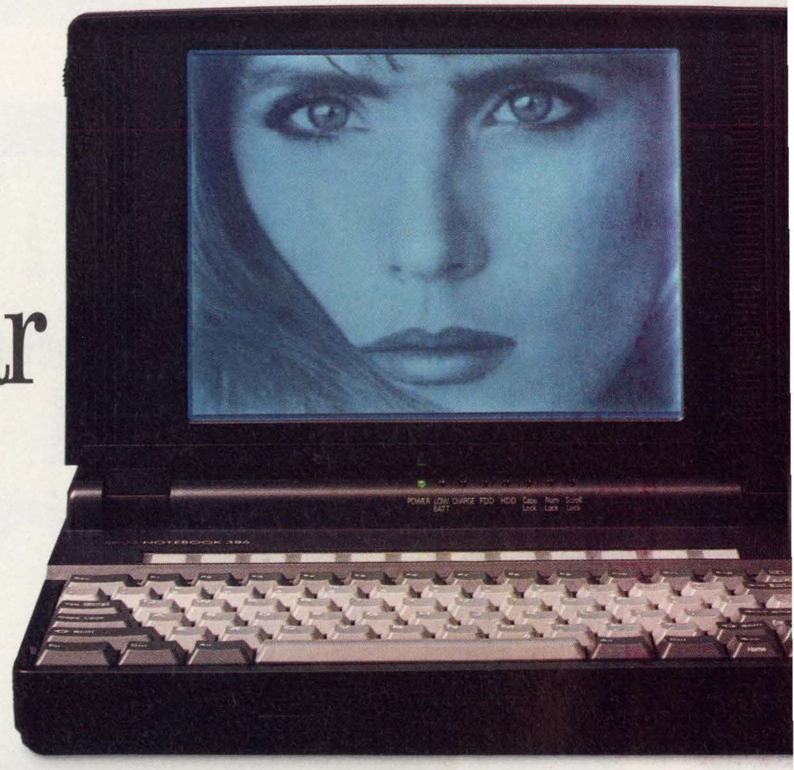

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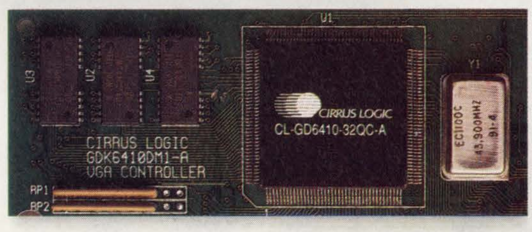

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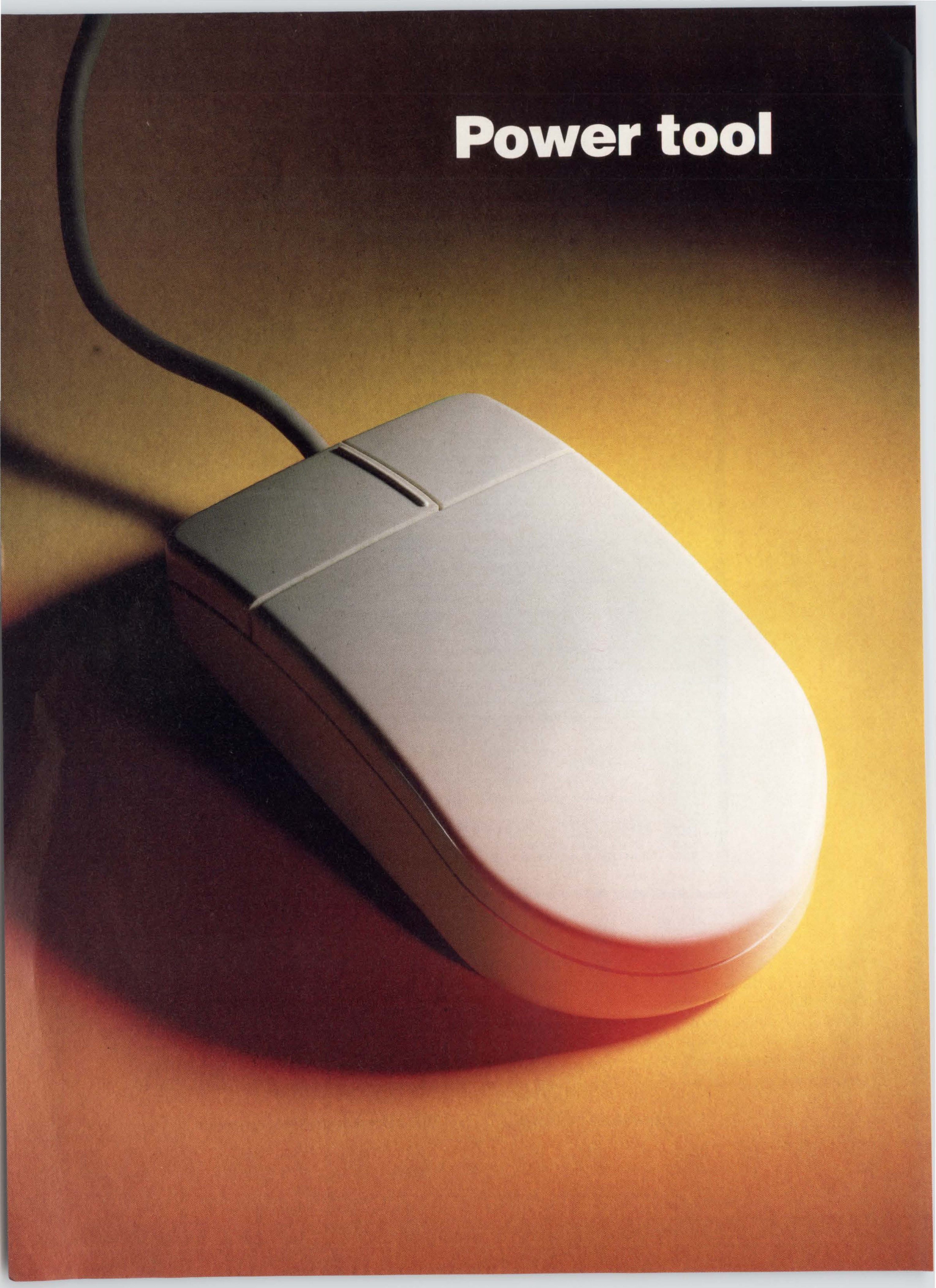


TAKING THE RESPONSIBILITY

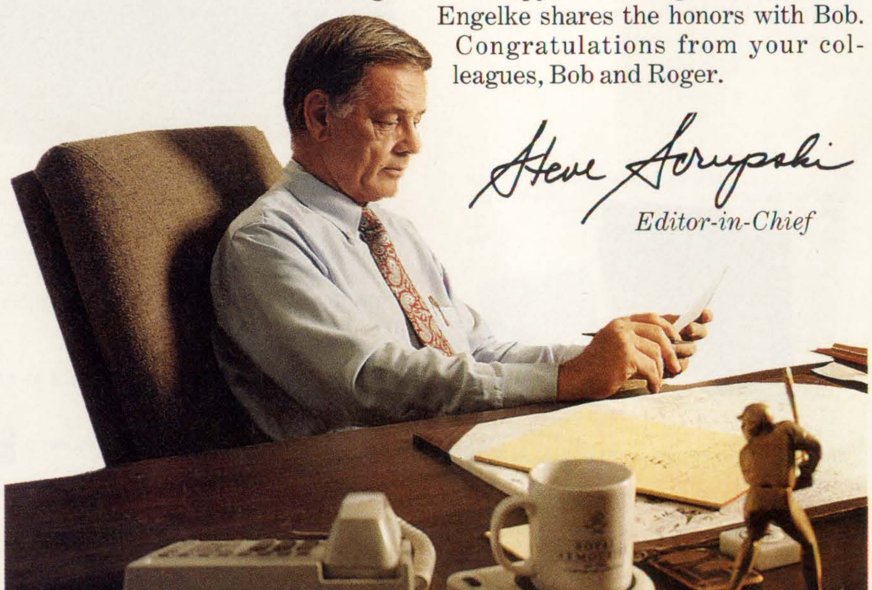
For as long as I can remember, the secret of successfully designing and marketing a product has been "Find a need and fill it." Some slick marketers may have altered this to "Create the perception of a need and then fill it." In either case, the advice carries an implicit recommendation for a pro-active approach. It essentially says "Don't just sit there, go out and do something if you want to succeed." And, conversely, it means that if something goes wrong, you have no one to blame but yourself. Controlling one's own destiny is the American way, at least until recently.

These days, that individualism is being replaced by a "it's not my fault" mode of thinking. There always has to be someone else to blame for our woes. This trend is exemplified in our judicial system, where an overwhelming amount of litigation is burdening the court system. Whenever misfortune befalls someone, it seems the first reaction now is "Whom do I sue, because this obviously could not have been my fault." This litigation craze has even reached the extent that a cab driver in San Francisco gets sued – and loses – because he injures a mugger while restraining him after a crime. We also see this pass-the-blame approach in our schools, where teachers push responsibility onto the parents for a student's poor performance.

"Our principal problems are within and not without...To remain great we must again emphasize politically, economically, and socially those basic methods that made us great in the first place." These two points are made in a recent insightful newspaper ad sponsored by George Romney, former Governor of Michigan and CEO of American Motors. In international trade, Americans can complain about unlevel playing fields, but while we're expending our energy doing that, competitors steadily improve. In today's world, you simply can't afford to wait around for government to redress inequities and expect that to solve competitive marketing problems. It's far better to focus on correcting our own problems, from short-sighted management to a barely coping educational system.

A NEAL CERTIFICATE FOR PEASE PORRIDGE

On a happier note, Electronic Design is proud to announce that the Editorial Committee of the American Business Press has bestowed a Jesse H. Neal Certificate of Merit on Bob Pease's column, "Pease Porridge." The column was honored in the category of Best Regularly Featured Department or Column. Electronic Design's Chief Copy Editor Roger Engelke shares the honors with Bob. Congratulations from your colleagues, Bob and Roger.



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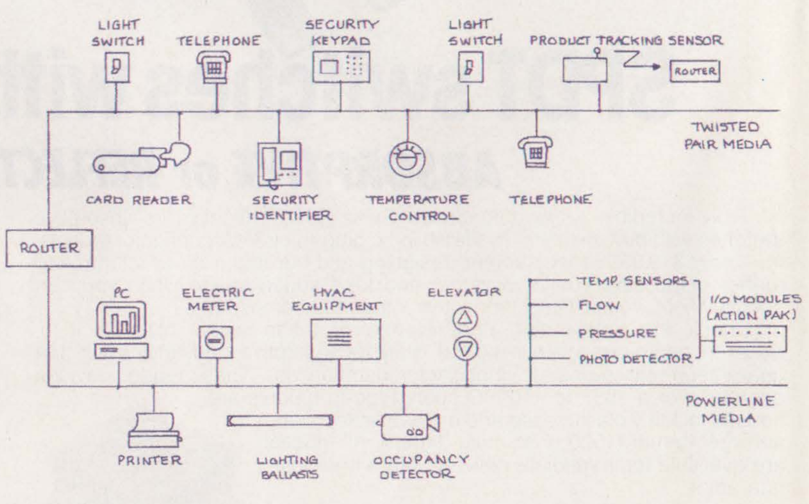
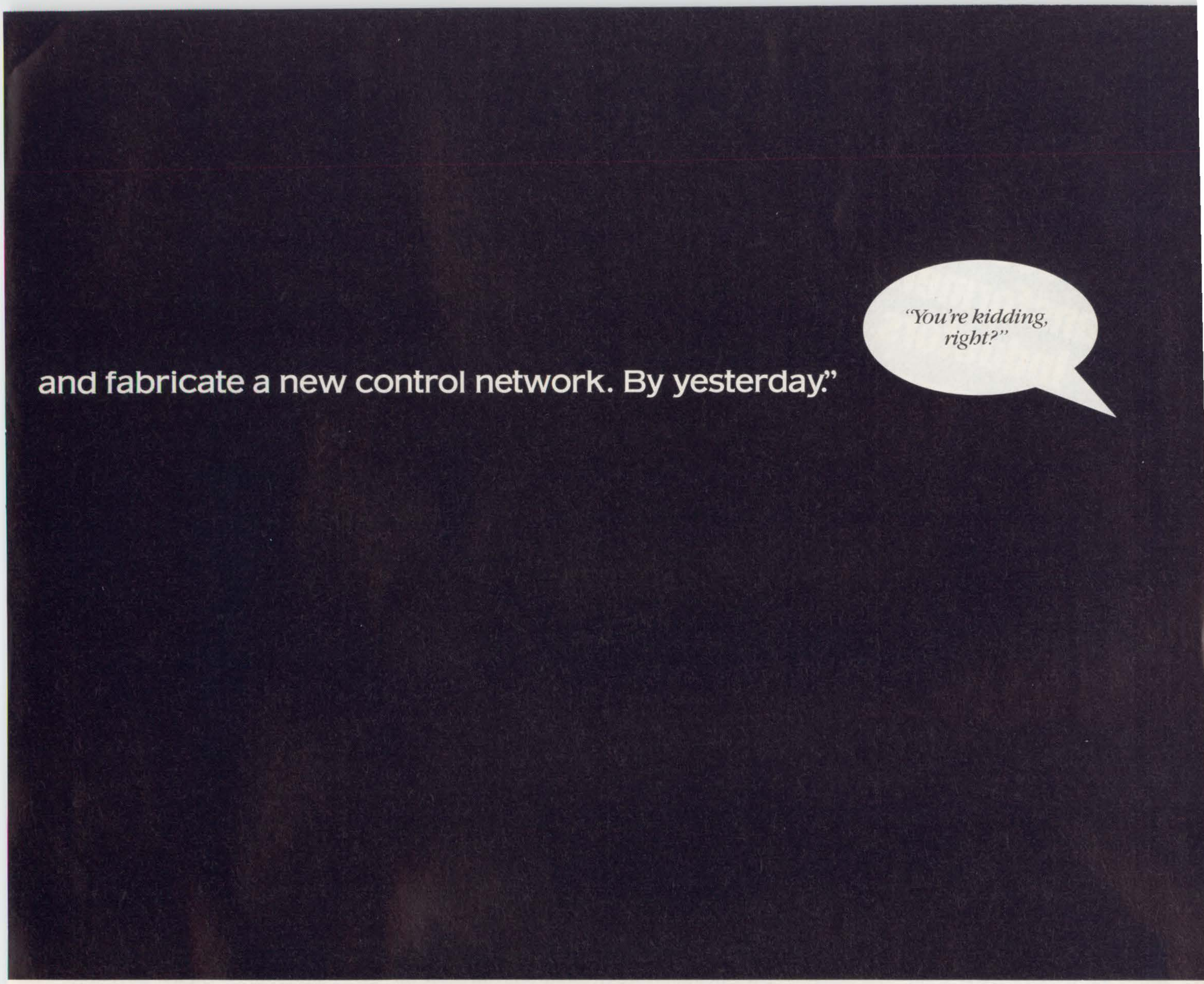




and fabricate a new control network. By yesterday."
"You're kidding, right?"

STANDARDIZE ALL ANALOG MODELING


LISA MALINIAK
COMPUTER-AIDED ENGINEERING

As mixed-signal systems grow in size, they become more difficult and time-consuming to simulate. That's where analog behavioral modeling enters the picture. However, standards for analog behavioral models don't exist. As a result, vendors and users are forced to build their own models, creating a horde of incompatible software. This lack of standards, says Kim Hailey, vice president of engineering at Meta-Software Inc., Campbell, Calif., is due to the complexity involved in describing analog components at a high level, the difficulty in dealing with continuous equations and their derivatives, and the challenge of agreeing on a common set of building blocks.

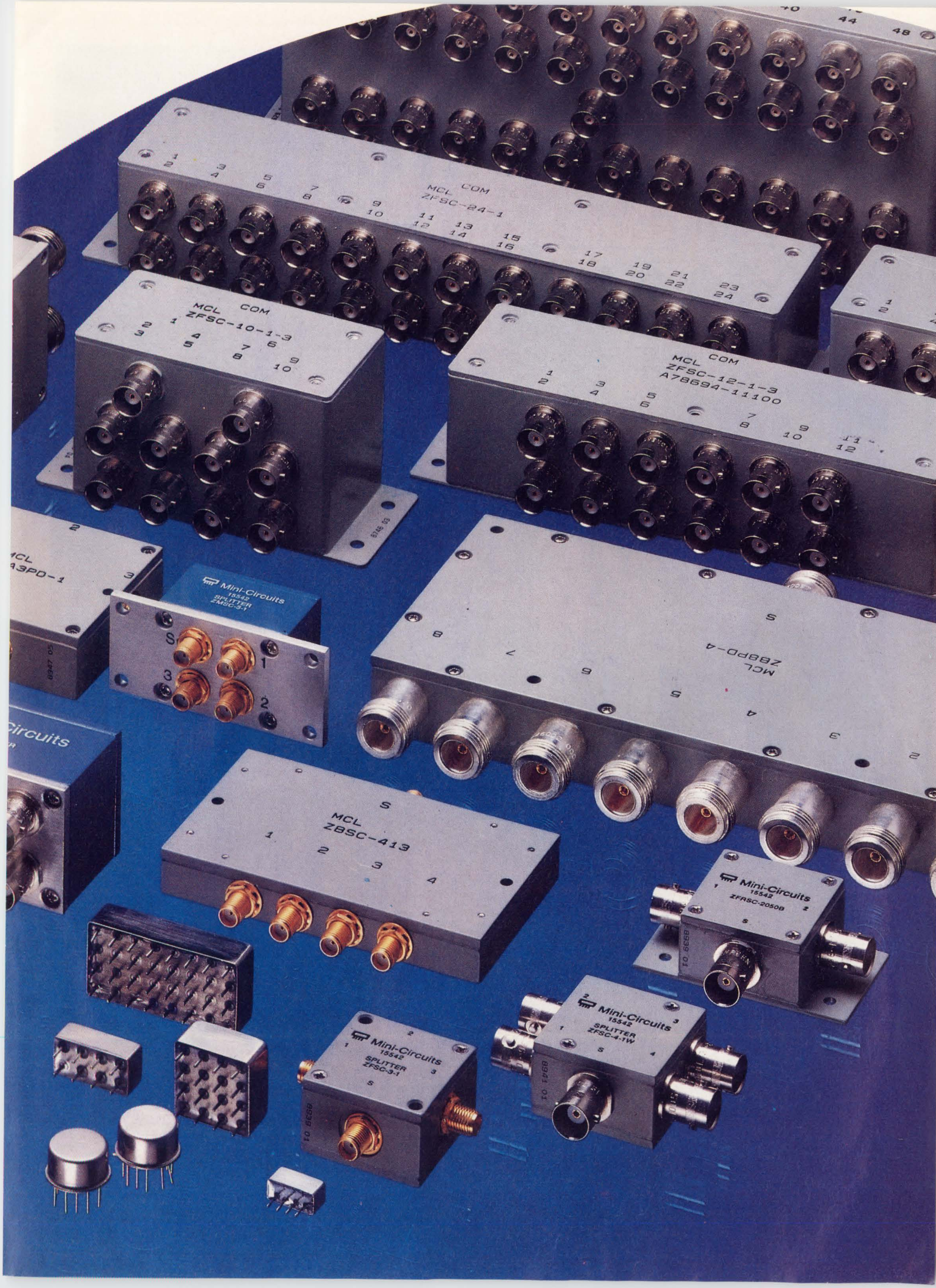
Serious efforts are being made to standardize analog modeling. In spite of that, Jim Solomon, president of Cadence Design Systems' Analog Div., San Jose, Calif., says that it will be several years before there's a complete, standardized solution to help engineers who need analog behavioral modeling. In the meantime, however, intermediate steps can be taken. Engineers can use Spice low-level primitives, such as resistors, capacitors, and diodes, to create rather inefficient behavioral macromodels. In addition, engineers can use the existing Spice behavioral extensions. Ultimately, engineers will need a standard full analog-behavioral-modeling language.

Solomon points out that standardizing extended Spice primitives, an intermediate step between Spice and full language, is easier and faster than standardizing a language. He says he wants to gather a group of interested parties – vendors, universities, and users – discuss the issues, and get to work on setting a standard. The issues should start with the work that's already been done by many vendors. One such example is the PSpice software from MicroSim Corp., Irvine Calif., which includes limited analog behavioral modeling.

The idea of standardizing Spice primitives, however, is not without problems. Ed Cheng, strategic programs director for the Analog Mixed-Signal Div. of Mentor Graphics Corp., Wilsonville, Ore., explains that if the proposed extensions are to deliver on the promise of model portability, then it's critical to have a standard method to verify that each simulator implementation gives the same results for the model extensions. In other words, one major issue will involve developing a calibration suite. In addition, the effort must include semiconductor manufacturers. Mentor has started conversations with semiconductor vendors about standardizing Spice extensions, and is considering making its own extensions available for inclusion with other Spice-based simulators. The Mentor equation-based models don't require the same level of calibration as individual implementations of a standard would.

Mast, a language used with the Saber simulator from Analogy Inc., Beaverton, Ore., is the most proven analog behavioral capability available today. However, although many engineers use Saber, it's not a standard. On the other hand, David Smith, Analogy's vice president of engineering, points out that in practice, Spice isn't a standard either. Each Spice vendor has modified the original Berkeley models so that they're no longer compatible.

Analogy, in fact, is one of many EDA companies actively involved in two significant efforts to develop a standard language for analog and mixed-signal systems. The IEEE has a committee that's been working on analog extensions to VHDL for over a year now. The requirements document has been distributed for review, and work is starting on the language definition. In addition, Darpa has also funded the MIMIC hardware description language (MHDL) program, which is attempting to define a language for designing systems ranging from low to microwave frequencies. MHDL work is ahead of the analog VHDL extension: The MHDL language definition has already started through the initial stages of development and review.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EUROPE TO DEFINE WIRELESS-LAN STANDARDS

European regulators are planning to define standards on a pan-continental basis for high-capacity wireless local-area networks. The networks will use short-range radio links to interconnect workstations and PCs with fixed Ethernet or faster networks. Facing a shortage of commonly available frequencies across Europe, the European Radio Office—the body set up to administer the radio spectrum—has identified spare slots in the 5-GHz and 17-GHz bands. An international working group known as Technical Committee RES 10 (Radio Equipment and Services) has been asked to define a technical specification for networks that can carry data at rates of around 20 Mbits/s. A draft specification ready for public comment is expected by September. The proposed networks are dubbed HiPerLAN for High-Performance Local Area Networks. In the meantime, European regulations have been framed to allow lower-speed "simple" networks to be implemented at frequencies between 2.4 and 2.5 GHz. As in the U.S., that band is designated for industrial, scientific, and medical (ISM) purposes. Wireless LANs operating at those frequencies will have to use spread-spectrum technology to avoid interference with other users of the band. Wireless-LAN systems that are currently available in the U.S. and operate in the North American ISM band around 900-MHz frequencies will not be allowed in Europe. There they are assigned solely for mobile communications. *PF*

DIAMOND-WAFER PROCESS IMPROVES SUBSTRATES

For the first time, freestanding white diamond is being produced by a chemical-vapor-deposition (CVD) process in wafer sizes up to 4 in. in diameter and 1 mm thick. White diamond is the purest form of the material made with CVD. By applying its superior thermal conductivity to substrates and heat sinks, builders of multichip modules and other electronic packages will be able to place faster and higher-power circuitry in a smaller package. The transparency and extreme hardness of the white-diamond film also enhances its applicability for infrared and microwave package windows. The material, developed by the Norton Co.'s Diamond Film Division, Northboro, Mass., was created by fine-tuning an existing CVD process. Earlier diamond-deposition processes have been limited to producing very thin films because of their low deposition rate. Norton's process boasts much higher deposition rates, which yields thicker films. *DM*

ENHANCED FPGA SUPPORTS 50-MHZ-PLUS CLOCKS

By lowering the programmed resistance of antifuses, a forthcoming chip will be able to support microprocessors and memory subsystems running at clock speeds of 33 to 50 MHz and higher. The lower resistance reduces speed-limiting RC delays to improve circuit performance. The QL12x16 developed by QuickLogic Corp., Santa Clara, Calif., enables selective antifuses to be programmed with on-resistances down to 50 Ω. The low resistance combined with small antifuse capacitances accounts for nearly all of the speed improvements. The chip contains a matrix of logic cells organized as 12 rows by 16 columns. Each cell contains a dedicated flip-flop plus sufficient combinatorial logic to create two latches. That yields a total of 576 storage elements and typical gate equivalency of about 2000 usable gates (equalling about 6000 gates, as measured by some of the other large EPLDs or RAM-based arrays). Internal flip-flops in the chip toggle at 180 MHz. Such functions as a 16-bit loadable counter can run at over 100 MHz. The chip will come in an 84-lead plastic leaded chip carrier and packs 68 bidirectional I/O cells and 8 dedicated input cells. In 100-unit lots, the IC sells for $98 each. An updated version of the toolkit sells for $3995 to new users. Existing users can also get software upgrades. Contact Hank O'Hara, (408) 987-2000. *DB*

BRITISH NAVY TO USE FDDI NETWORKS

British Royal Navy submarines are now likely to be fitted with fiber-distributed-data-interface (FDDI) networks. This comes as a result of a study contract awarded by the Ministry of Defence to Ferranti-Thomson Sonar Systems U.K. Ltd. The company has been asked to define a standard data highway for Britain's underwater navy, as well as recommend the most efficient means of implementing and testing it. According to a company spokesman, "a key element of the study will be the implementation of high-performance FDDI communications standards." He says that the proposed data highway has a fiber-optic "ring-of-trees" topology that will interlink a submarine's command and tactical weapon-control systems. The newly formed Anglo-French firm, based in Stockport, Cheshire, U.K., has been involved in significant research using FDDI to provide high-capacity data links for sonar systems. *PF*

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TANGIBLE FUTUREBUS+ PRODUCTS EMERGE

Futurebus+, the open architecture that performs at 3.2 Gbytes/s using 256 bits, was officially announced two years ago. Now, products designed with the architecture are appearing. At a recent product update at Buscon West, 23 companies displayed the fruits of their labor. The products, highlighted by the first commercial Futurebus+ system from Digital Equipment Corp., included connectors, backplanes, semiconductors, test equipment, CPU and peripheral boards, systems, and interfaces. Some exhibitors were AT&T, BICC-VERO, CCT, Force Computers, Hewlett-Packard Co., ITT Canon, Mupac, Nanotek, National Semiconductor, Raytheon, Signetics, Tektronix, and Texas Instruments.

To accelerate the acceptance of the open-systems concept, the Standards and Open Systems group was formed. The group's objectives are to develop and prioritize a common set of standards and specifications, and to expand the scope of the U.S. Open Systems Interconnect Workshop to address the needs of all parties using open systems throughout the world. The areas covered by the group include interoperability and portability, operating systems, user interfaces, systems engineering, data management and interchange, graphics, and networking. *RN*

PASSIVE-MATRIX LCDS REACH VIDEO SPEEDS

By using a new method to address the pixels of passive-matrix LCDs, a developer of color LCDs achieved video speeds without sacrificing display brightness or contrast. Prototype displays driven by the new scheme achieve 50-ms response time with 30:1 contrast. The drive method, developed by In Focus Systems, Tualatin, Ore., is called active addressing. The scheme attains video speeds by using sophisticated, proprietary algorithms that intelligently distribute many small pulses over the frame period, rather than using the single, large row-select pulse characteristic of standard multiplexed LCD-drive methods. The result is a very high-contrast LCD that can be created from high-yield, low-cost passive-matrix technology. According to Paul Gulick, co-founder of In Focus Systems, the breakthrough in speed "debunks the myth that passive-matrix LCDs are inherently slow." Active addressing removes the complexity of the electronics from the glass substrate, which is the approach taken by thin-film-transistor (active-matrix) displays that place a transistor at every pixel location on the screen, and returns it to silicon, Gulick says. The company plans to introduce products using active-addressing technology next year. *DM*

SIGNAL PROCESSING'S BEST AT ICASSP'92

Running the signal-processing gamut from algorithms to the latest hardware is next week's International Conference on Acoustics, Speech and Signal Processing. The IEEE-sponsored conference, to be held at the San Francisco Marriott Hotel, Mar. 22-26, will have over 800 papers and several special sessions. The conference opens on Sunday with tutorials on adaptive filtering, implementation and synthesis of VLSI signal-processing systems, articulatory speech analysis/synthesis, and image sequence processing. This year happens to mark the 25th anniversary of what the conference organizers view as a landmark IEEE transactions publication, "Special Issue on the Fast Fourier Transform and its Application to Digital Filtering and Spectral Analysis" by the Audio and Electroacoustics Group. To mark that event, a special plenary session will provide some perspective on the early development of the FFT. Additional lectures will be given on the "Application of Neural Networks" by Carver Mead, and on "Wavelets" by Martin Vetterli of Columbia University. The general program contains multiple sessions covering such topics as speech synthesis and recognition; filtering; image, communications, and video and TV signal processing; among many others. Registration at the door is $395 for IEEE members and $475 for nonmembers. *DB*

PEN-INPUT CONTROL CHIP SET EASES DESIGN

A cordless touchpen can now be used thanks to a chip set and signal sensor grid that form the heart of a pen-based entry subsystem. Released at last month's Pen-Based Computing Conference sponsored by Technologic Partners Inc., New York, N.Y., the Kurta Lite-Touch Pen supports handwriting, selecting, and gesturing motions, making it useful for almost any type of system. The pen-controller chips, developed by Kurta Corp., Phoenix, Ariz., process the pen signal and serve as the electronic interface to the computer's subsystems. The sensor grid that detects the pen's signals is available as a second assembly. The pen-based hardware is compatible with Go Corp.'s PenPoint, Microsoft's Windows 3.1 for Pen, and Pen Dos from Computer Intelligence. Samples of the chip set are now available. Contact Gary Fitzgerald at (602) 276-5533. *DB*

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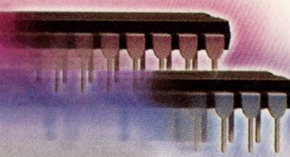

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HP-IBM ALLIANCE PRODUCES STANDARD FIBER MODULE

High-speed optical-fiber connections between computers or peripherals are attractive due to the simplicity of the cabling and the EMI-free nature of the optical communications. However, fiber-channel optical links that can operate at several hundred megabits/s (266 Mbits/s or about 25 Mbytes/s of actual data, to be exact) are quite expensive and require a considerable amount of circuitry to implement.

Designers at Hewlett-Packard Co., San Jose, Calif., and IBM Corp., Rochester, Minn., pooled their efforts and came up with a simple-to-use chip set. Also designed was a standardized module format that will both cost-reduce and, they hope, provide a standard format that multiple manufacturers will eventually support. The companies expect that the modules will trim cost by as much as 80% over current solutions.

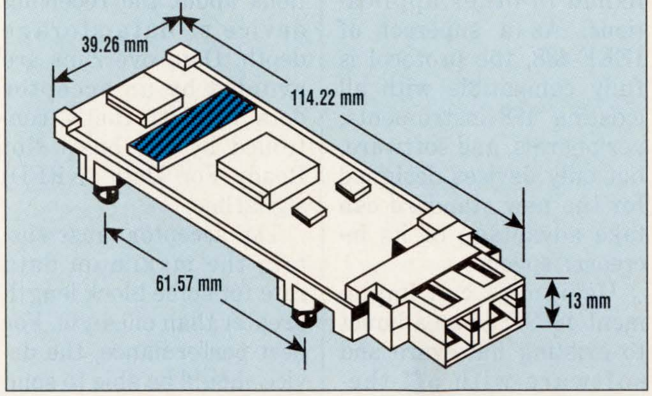
By employing surface-mounting technology and the high-integration levels for the chips, designers at both companies created a 39.26-by-114.22-mm module that's just 13-mm thick *(see the figure)*. The module contains an entire fiber-channel transceiver that can easily be mounted on a circuit board or embedded in a system.

The relatively simple fiber-channel standard for point-to-point communications gives designers a low-overhead, high-speed channel for subsystem-to-subsystem data transfers. Such a connection is sorely needed due to the onslaught of graphics-dependent applications now running on desktop computers—multimedia, medical imaging, client-server systems for scientific visualization, and many other up-and-coming applications.

Although the fiber-channel market is in its infancy (only 40,000 links were installed in 1991, because the standard has only recently been adopted by the American National Standards Institute), it has a bright future projected. HP and IBM estimate 1.5 million links will be installed by 1995, with 1 million links/year expected beyond that.

Of the four standard speeds—133, 266, 531, and 1062 Mbits/s—that are part of the fiber-channel standard, HP and IBM decided to focus on the 266-Mbit/s option. They felt that was the best choice for what could be implemented with current optical technology and silicon control circuits. With this speed option, links employing inexpensive multimode fibers and long-wavelength LED emitters can be as long as 1 km, while a short-wavelength laser diode on the same fiber doubles the length of the link. To achieve the maximum distance of 10 km, a long-wavelength laser diode and more-expensive single-mode optical fibers must be used.

The HP-IBM collaboration resulted in a transmit/receive chip set that performs all of the physical-layer signal handling—10-bit input and output interfacing, laser-safety control, laser driving, and signal retiming and demultiplexing logic. An additional chip for the optical signal detector (a transimpedance amplifier) is required for the receive channel. The chip set can be configured to handle the optical-fiber interfaces, or as an option, a limited-distance ECL coaxial-cable interface. The companies are also working on chip sets to support the higher-speed fiber-channel options.



One unique aspect of the chip set is the special attention paid to optical safety. Special detection logic prevents the link from operating without a fiber inserted into the connector, preventing a user from accidentally looking directly into an active emitter. The modules thus meet every worldwide standard for optical safety.

Both HP and IBM will start selling functionally identical single-channel modules next quarter (chip sets will not be sold at this point). They'll also offer the ability to create custom, multichannel configurations. Furthermore, both companies will make the module's physical design specifications available to other companies who would like to adopt the same size to provide customers with additional alternate sources.

For more information, contact Ed Frymoyer at Hewlett-Packard, (408) 435-4266, or Stephen Sibley at IBM, (507) 253-2943.

DAVE BURSKY

NEW PROTOCOL BOOSTS IEEE-488 DATA TRANSFERS TO 5 MBYTES/S

Although it's been around a long time, the venerable IEEE-488 bus still has plenty of life left. With the tremendous improvements in instrument and device speeds in recent years, however, some users feel that the standard's 1-Mbyte/s data rate is a bit slow. An answer to this outdated speed limit is a new streaming-data technique that boosts the bus' data transfer rate to 5 Mbytes/s.

The new streaming-data protocol for IEEE-488, known as 488SD, was written by Capital Equipment Corp. (CEC) of Burlington, Mass. Although streaming data is new to IEEE-488, the technique is well established in other applications. As a superset of IEEE-488, the protocol is fully compatible with all existing 488 instruments, peripherals, and software, but only devices designed for the new standard can take advantage of its increased speed.

Designers can implement 488SD as an adjunct to existing hardware and software with off-the-shelf components, making it easy for manufacturers to introduce 488SD products. CEC says it will offer 488SD to the IEEE for acceptance as an industry standard.

The 488SD protocol changes the way IEEE-488 handshake lines are interpreted and eliminates unnecessary timing delays. Existing cables and cable topologies easily handle the increased data rate.

CEC uses the analogy that IEEE-488 data transfers are like a bucket brigade, while streaming-data transfers are like a fire hose. That is, the conventional protocol sends data over the bus one byte at a time. As a result, each byte has the overhead of a data-acceptor handshake. The speed of these handshakes is limited by the handshake line's passive RC time constants, which increase as the cable length increases. The handshakes create most of the delays in IEEE-488 data transfers.

The streaming-data protocol, on the other hand, processes data in blocks, eliminating most of the overhead associated with conventional 488 data transfers. In fact, the source data blocks can be any length. The 488SD protocol makes no assumptions about the receiving device's data-storage depth. Data overruns are avoided by an acceptor data hold-off that's controlled by the bus's Not Ready For Data (NRFD) signal line.

The acceptor must sustain the maximum data rate for some block length greater than one byte. For best performance, the device should be able to send and receive an entire data block without interrupting the transfer.

There shouldn't be a problem programming the new protocol. A system can be set up to determine streaming-data capability using a mnemonic similar to those defined by the IEEE-488.2 standard. For example, "STR?" may be used to determine streaming-data capability, and "*STR (1,0)" could enable and disable the streaming mode. IEEE-488.2 devices that don't recognize a command from the controller must return an appropriate message. Therefore, 488.2 devices that don't have streaming-data capability will respond correctly to the query.

Of course, the controller must have the ability to enable or disable the streaming-data mode depending on whether the device can accept or transmit in that mode. And a talker with streaming-data capability must suspend that mode when it's talking to a nonstreaming device.

The first product compatible with the new protocol is CEC's 488EX interface kit. The kit includes a board that plugs into a 16- or 32-bit slot in any ISA or EISA computer bus. The board accommodates all IEEE-488 devices and functions, and can be used either as a system controller or a device.

The board offers direct memory access with user-selectable DMA channels for data-block lengths of up to 64 kbytes. Moreover, user-selectable interrupts can detect 14 maskable interrupt conditions, such as service request, interface clear, and device trigger.

Software included with the 488EX can be used with all popular programming languages, including Windows 3.0 and Visual Basic. Software writers can use any of four methods: callable subroutines, file I/O, a universal language interface, or resident firmware. The programs themselves run under DOS, OS/2, or SCO Unix.

The package includes a software analyzer that detects errors and suggests corrections, and control-line monitor functions. An extensive library of example programs and a programming and applications manual is supplied. The 488EX kit costs $495.

CEC sees initial users as those who need to make very fast computer-to-computer transfers. To do so would require only a 488EX at each end of the system. Using the new protocol's full speed in data-acquisition and test-and-measurement systems will require the development of hardware that supports the streaming-data techniques.

JOHN NOVELLINO

SUBLIMATION PROCESS HERALDS LOW-COST CdTe SOLAR CELLS

By using deposition techniques for cadmium-telluride films, a low-cost process for solar-cell fabrication is now practical. The process, developed at the Battelle Institute in Frankfurt, Germany, permits efficient thin-film CdTe solar cells to be produced rapidly on inexpensive substrates, such as ordinary window glass. Ultimately, the process may cut the cost of such solar cells to a level 80% lower than today's silicon solar cells. Pilot production could start in three years, according to Dieter Bonnet, who heads the CdTe project at the Institute.

With the process, Battelle deposited high-quality CdTe films within one to two minutes, producing solar cells with efficiencies as high as 11%. Much higher efficiencies can be expected, says Bonnet, who adds, "We intend to enter pilot production for this highly promising thin-film solar cell and are inviting interested parties worldwide to participate in this effort."

To compete with energy sources such as coal, oil, and nuclear energy, solar cell costs must come down by four to five times from the present level of $5/W to $10/W (these numbers are based on the solar cell unit delivering 1 W of energy under direct solar irradiation). According to Battelle, only thin-film cells can be expected to be made at such low cost, provided that large-scale production is feasible.

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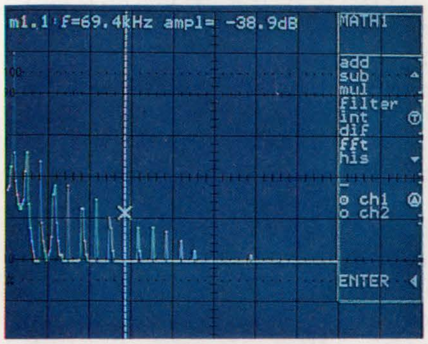

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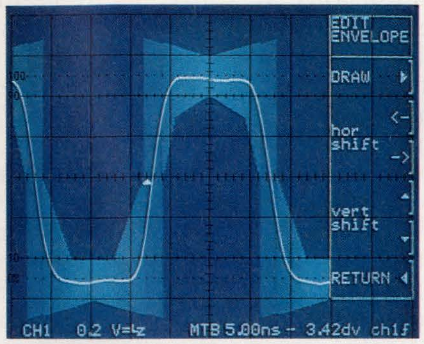

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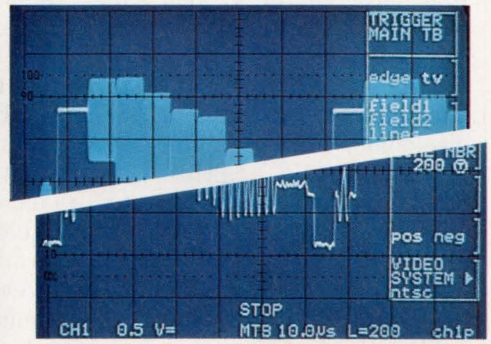

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semiconductor materials are good candidates for thin-film solar cells, Bonnet explains. In fact, only four have so far yielded promising results (efficiencies of more than 10%): amorphous silicon, crystalline silicon, copper indium diselenide, and cadmium telluride. The CdTe cell has turned out to be superior because of its ruggedness and stability.

Battelle's process is based on a closed-spaced sublimation technique that permits top-quality polycrystalline CdTe films to be produced at high deposition rates. In the process, the cadmium telluride is sublimated onto the substrate at a temperature between 600 and 700°C. The substrate, which is located close to the CdTe source, has a lower temperature—around 500°C. Deposition takes place in a moderate vacuum and in an inert-gas atmosphere, which helps to reduce the solar-cell production cost.

The institute is now working on a concept of transferring its fabrication scheme to practical applications. As with photographic films, the price of solar cells is determined not only by the material's performance, but also by the production method employed, Bonnet says. He also adds that with the film, it should be possible to deposit the CdTe films onto moving substrates with the closed-spaced sublimation process. Given the high deposition rate already achieved, this could be done at substrate throughput rates of 6 m^2/hr. and higher.

According to Battelle, a competitive commercial CdTe solar cell module will be available once industrial partners are found for further development. Based on preliminary estimates, the cost of fabricating standardized modules, typically measuring 50 by 50 centimeters, will be less than \$120/m^2 if an annual output of 10,000 m^2 can be realized. This would mean module costs of about \$1200 for an energy output of 1 kW under direct solar irradiation.

Battelle's cost estimate for CdTe cells is roughly 80% lower than the current cost of silicon solar cells. This should open a big market for CdTe solar cells, a market "that justifies heavy industrial commitment," Bonnet points out. He is certain that a strong position can be attained with CdTe cells in the growing market for renewable energy systems. Because fabricating thin-film solar cells can be fully automated, it need not be transferred to low-wage countries.

JOHN GOSCH

STANDARDIZED 3U VME STAKES A CLAIM IN STD 32'S TERRITORY

Spurred on by potential "high-end" competition from the STD 32 bus, the VFEA International Trade Association (VITA), Scottsdale, Ariz., has formed a subcommittee to pursue standards that will push the 3U VME specification to the forefront. The specification governs VMEbus boards with a 3U form factor. STD 32 is a 32-bit bus specification that's intended to propel the STDbus to higher-performance applications than possible with 8 or 16 bits. While 32-bit STD boards have been somewhat successful, they've taken some business only from the "low-end" of the VMEbus market.

Ziatech Corp., San Luis Obispo, Calif., which is the driving force behind STD 32, uses the EISA connector and chip set. STD 32 isn't an IEEE specification, although Ziatech freely distributes the specification to anyone who wants it. However, a gap exists between the older STDbus boards and those boards that are based on the STD 32 specification—they just aren't compatible. "But," says Ray Alderman, technical director of VITA, "though Ziatech has gone forward with STD 32 and has done very well with it, there's a crack in the armor. We feel that a lot of the high-end STDbus users are in transition. Those people will have to make a decision whether or not to go to STD 32 or some other higher-performance bus. We think that we can take some of that business. Anybody that's in transition is a target for the 3U VME specification."

One drawback to STD 32 is its bus data-transfer rate—it tends to run out of steam when pushed to its limit of about 14 Mbytes/s. Consequently, the processor runs faster than the I/O bus for high-speed 386 and 486 processors. Though this offers some advantages, it presents a problem when data is pipelined. This "upper limit" area is where the 3U VME specification is targeted. The specification also provides an easy migration path for boards with form factors up to 6U and into the 64-bit arena.

A few technical issues had to be tackled before standardizing 3U VME. First, to ensure that the bus maintains a high level of performance, Autobahn, the high-speed serial channel, will be proposed as a standard (ELECTRONIC DESIGN, *Oct. 24, 1991, p. 27).* Autobahn's low end comes in at about 200 Mbytes/s, with the high end straddling 400 Mbytes/s in about three years.

According to VMEbus experts, a chip set for such a high-end bus shouldn't cost more than \$50 to \$100 in large quantities. Such a price is more than adequate for data pipeline applications, including graphics and high-speed communications on such networks as the Fiber Distributed Data Interface (FDDI). Autobahn, the data-carrier mechanism for high-performance 3U systems, fits right on its two established pins on the serial bus. The original Autobahn specification was proposed by PEP Modular Computers located in Germany.

The second technical issue involves multiplexing the signals. 3U VME boards have only one connector with 96 pins, including power, ground interrupts, and control circuitry. With grounds between the pins for crosstalk, what remains is 16 bits of data and 24 bits of address. But VME doesn't multiplex data and address. In other words, the address lines aren't used during the data cycle and the data lines aren't used during the ad-

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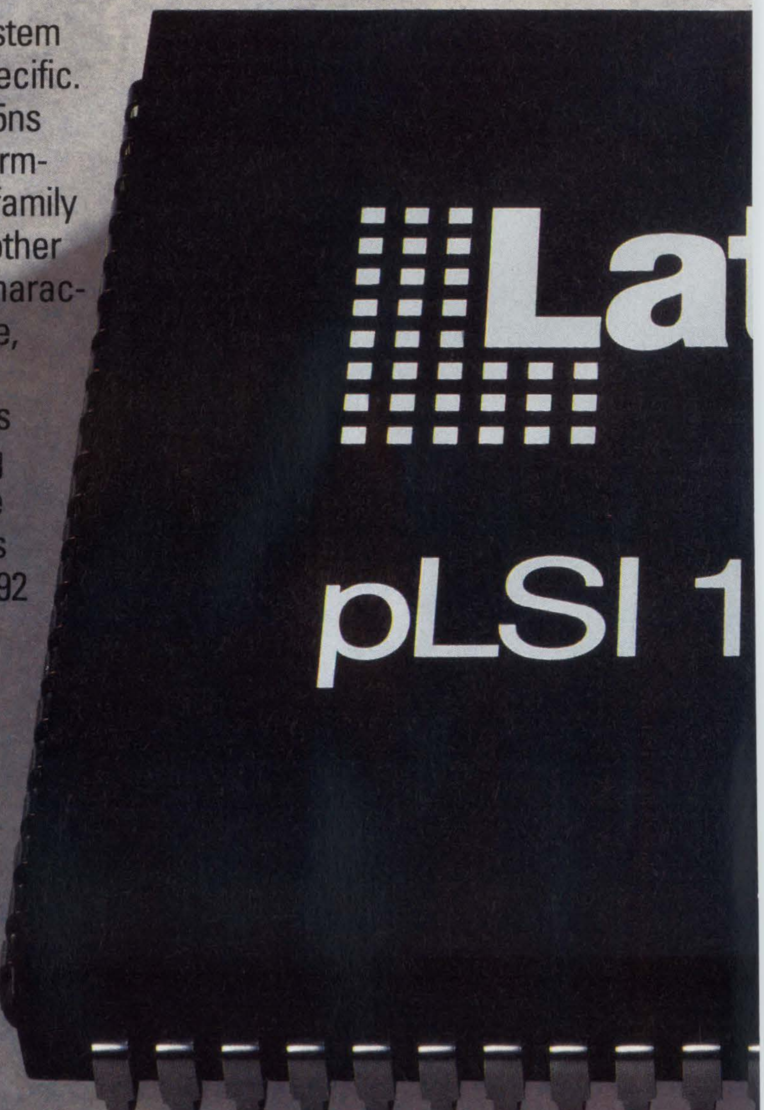

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dress cycle. By multiplexing the address cycle when the data bus is idle, those unused data bits can be added to the address, pushing it to 40 bits. On the data side, the same concept is carried out. In this case, there are 24 address lines, so 16 of them are added to the data bus to get 32 bits. As a result, the first 32 bits of data are latched on the original data lines and the next 16 bits are latched during the data cycle on the first 16 lines of address. This proposal was presented by Mizar Inc., Carrollton, Texas.

The availability of functionality is another important consideration. The STDbus market offers a wide variety of I/O cards—there's an interface for just about anything a user needs. To get more and customized functionality from the 3U VME cards, GreenSpring Computers, Menlo Park, Calif., is standardizing its IndustryPaks daughterboard modules. The modules fit on either processor cards or carrier cards, which are basically bus-interface cards with address decoding and four IndustryPaks slots. With these daughterboard modules, users just snap on the required functionality.

The 3U subcommittee must also fulfill the lack of a standard high-density interconnect coming from the cards' front panels. The connector would probably resemble a 50-mil-spacing pin connector. In a width of about 3 in., this type of connector can supply about 200 I/O pins. When that interconnect issue arises, connector companies, such as Amp, DuPont, and ITT Canon, will likely become more involved.

RICHARD NASS

EUROPEAN STANDARDS BODY UNVEILS RF EMC SPECIFICATIONS

The European Committee for Electrotechnical Standardization (CENELEC) has published the first of a series of European standards designed to prevent interference from the spurious emission of RF signals. EN 50081-1 is a generic emission standard covering all electrical and electronic equipment used in residential, commercial, and light industrial locations. It spells out electromagnetic-compatibility (EMC) test methods and limits of all electrically powered equipment with the exception of radio transmitters, which are to be covered by European Telecommunications Standards (ETS), defined by the European Telecommunications Standards Institute (ETSI).

For equipment containing microprocessors oper-

ating at more than 9 MHz, measured limits set for airborne radiation from an enclosure are 30 dBμV/m at 10 meters for frequencies between 30 and 230 MHz, and 37 dBμV/m at 10 meters for frequencies from 230 to 1000 MHz. Limits for all types of equipment are also set for ac-power-line interference. These limits range between 66 dBμV and 46 dBμV, depending on frequency. A series of recommendations for susceptibility measurements are included in the EN 5008-1 standard for information. They will be detailed in further basic standards that will refer to specific types of equipment.

Measurements are to be made on a port-by-port basis. A port is defined in the standard as "a particular interface of the specified equipment with the external electromagnetic environment." Generally, it refers to the points at which ac or dc power, ground leads, and signal and control leads enter an equipment's enclosure. A further definition specifies that an "enclosure port" is the physical boundary of the apparatus through which the electromagnetic fields may radiate or may impinge.

Both emissions from the apparatus under test and its resistance to spurious emissions are covered by the standard. However, CENELEC president Dr. Enrico Commellini says that the prime concern involving the mandatory aspects of the standard is to prevent any equipment from interfering with other systems.

The European Commission is determined to make the EMC standards mandatory directives that must be applied by national governments. In addition to the twelve European Economic Community member states, CENELEC's membership extends to Sweden, Norway, Finland, Iceland, Austria, and Switzerland.

The new national standards are set to be published on June 1. According to the agreement signed, conflicting national standards of CENELEC members must be withdrawn no later than December 31. The European Commission is determined to make as mandatory the EMC standards directives that must be applied by national governments. Existing, noncompliant equipment may continue to be used for another five years.

The new regulations may also apply in Eastern Europe too, since Czechoslovakia, Hungary, Romania, Poland, and Turkey have become associate members of CENELEC.

For more information on the new regulations, contact CENELEC at Rue de Stassard 35, Brussels-1050, Belgium; telephone: +32 2 519 69 19.

PETER FLETCHER

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IKOS		4.0 up	*Simulation* *Fault grading*
Mentor Graphics	HP/Apollo DNx Series HP9000 Sun/SPARC Solbourne	DNIX 5.03, Sun OS 4.1.1 Digital application 6.1 Digital application 6.3 Digital application 8.0 (in qualification) Parade	*Capture* *Simulation* *Design check* *Layout* *Clock Structures*
Synopsys	Sun/SPARC Interface to Mentor, Valid, Viewlogic	Sun OS 4.1.1	*Design synthesis* *Test synthesis*
Valid	Sun/SPARC Sun-3 DECstation 3100 IBM RS6000	Sun OS 4.1.1 GED, ValidSIM, RapidSIM ULTRIX, ValidSIM, GED GED, ValidSIM, RapidSIM	*Design capture* *Simulation* *Design check*
Viewlogic	Sun/SPARC PC386	Sun OS 4.1.1 Workview 4.0 DOS 3.3, Workview 4.0	*Design capture* *Simulation*

TRANSFORMING TECHNOLOGY INTO CUSTOMER SOLUTIONS

AN ASYMMETRICAL APPROACH TO POWER TRANSFER LAUNCHES THE ERA OF VERY-HIGH-DENSITY POWER CONVERTERS.

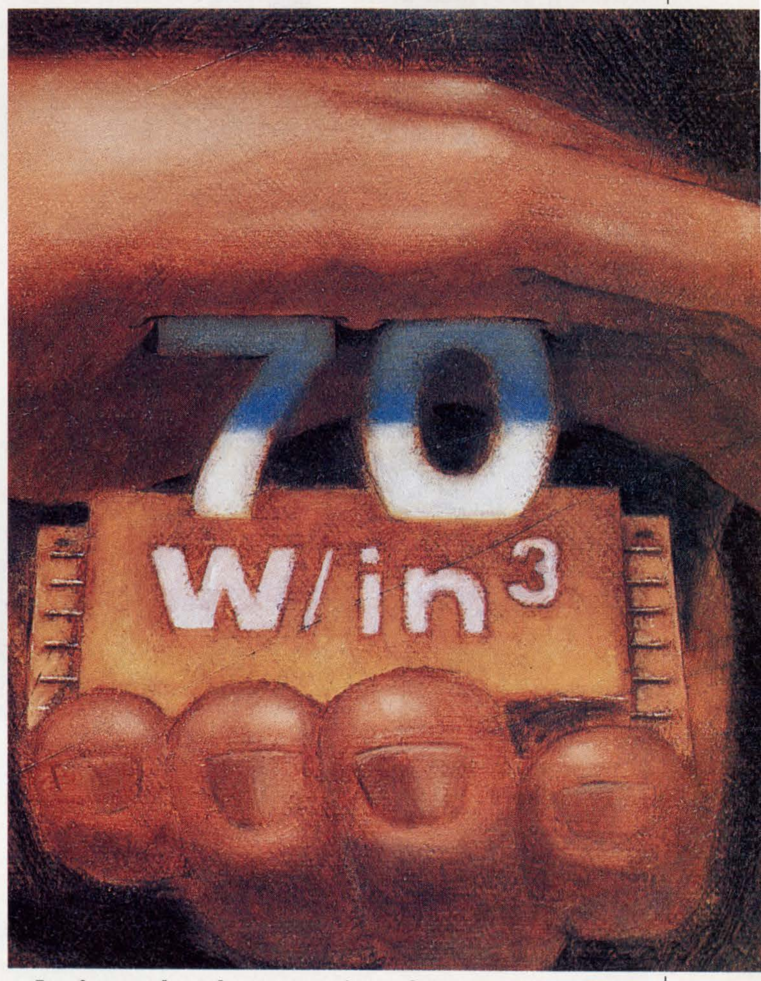
100-W DC-DC CONVERTER SPORTS 70-W/IN.³ DENSITY

DAVID MALINIAK

After creeping upward in tiny increments for several years, power-supply density has taken a significant leap forward with the introduction of Interpoint Corp.'s MFLHP dc-dc converter. The 100-W hybrid supply occupies less than 1.5 in.³ of space—the case measures only 2.5 by 1.5 by 0.380 in.—giving it a power density of just over 70 W/in.³. As the first board-mountable power supply to exceed 50 W/in.³, this converter inaugurates the era of very-high-density (VHD) dc-dc converters *(Fig. 1)*.

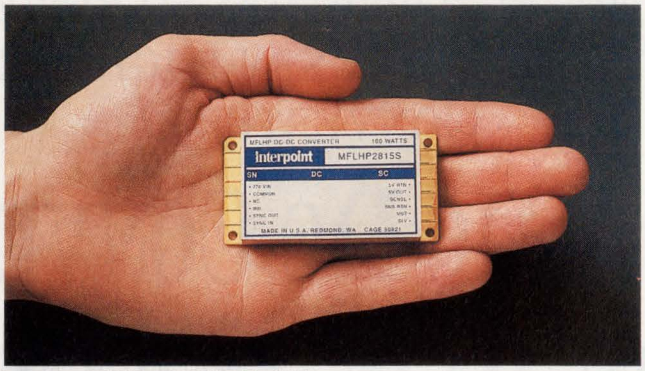
If a switching power supply were a building, the magnetics would be the foundation. They perform the transfer of power from the primary (input) side to the secondary (output) side. To achieve the density breakthrough, Interpoint's product-development engineers attacked the fundamental source of power transfer—magnetics design, construction, and control. Achieving very high power-supply densities depends on increasing the total transfer efficiency. In the case of the MFLHP converter, that meant new technology for controlling magnetics, a new magnetics design, and a new feedback system.

The most important advance in building the converter was the development of a fundamentally new control system designed specifically to minimize losses in the transformer *(Fig. 2)*. This new control system is called asymmetrical power transfer (APT). APT was designed to overcome the fundamental limits on power transfer that typical power-supply design has always encountered—that of balancing core-reset time, forward-conduction time, and peak-voltage stresses on power switches and rectifiers.



In forward-mode conversion, the transformer performs a balanced action to first deliver power to the load and then to reset core flux for the next cycle. Switching power-supply topologies are set up to provide this balance. Push-pull topologies, for example, achieve balance with two primary windings, only one of which is carrying load current at any given time. The magnetic flux induced while one winding conducts current is countered during the conduction time of the other winding. In this topology, only one half of the copper area is available for load current at any one time.

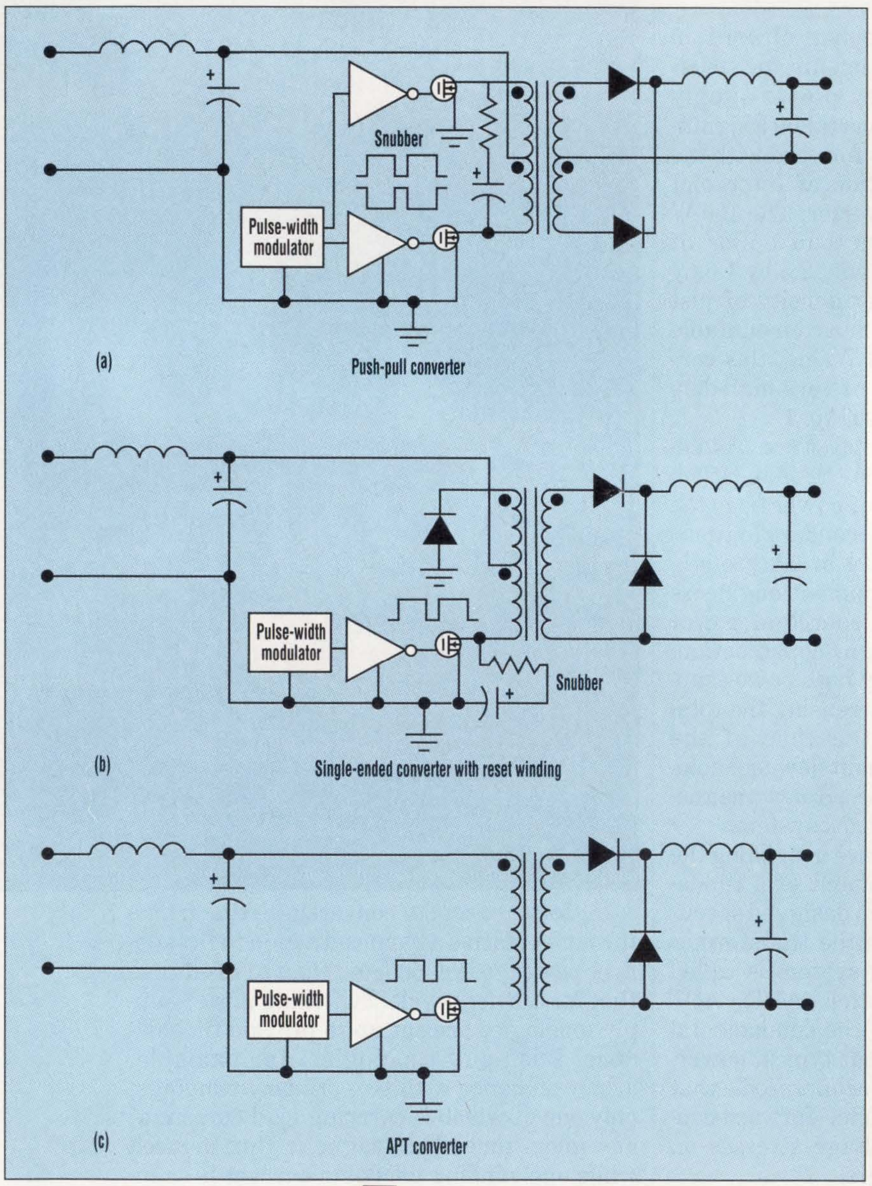
Single-ended topologies address the balance problem a little differently. They dedicate a catch winding in the transformer to the function of resetting magnetics. The main winding is dedicated to power transfer; the catch winding provides a balanced reset of the power winding on each transfer cycle. The V-Sec (voltage-time) product, during which power is delivered to the secondary, induces a flux which must be balanced in non-conduction time by resetting the core flux. The area used by the catch winding is not available for load current, and the conduction time is generally limited to 50% to maintain the symmetry of the power transfer. Extended conduction times can be achieved by fewer turns on the catch winding. However, this increases the voltage stress on the power switch and rectifiers, requiring higher-voltage components with higher conduction losses. Both the push-pull and the single-ended topologies require dissipative snubbers to protect against leakage-induced voltage transients, especially when any unequal turns ratio is used.



1. OCCUPYING LESS than 1.5 in.^{2}, the MFLHP dc-dc converter from Interpoint is the first board-mounted unit with a rating that exceeds 50 W/in.^{2}. The converter owes its density, to among other things, a fundamentally new control system designed to minimize transformer losses.

BETTER POWER TRANSFER

The APT mechanism was developed when research-and-development engineers on the converter-development team investigated how parasitic capacitance and inductance in the converter could be used to provide a reset function for the main winding. The idea was to direct some of this energy to the load in a non-dissipative manner. By balancing the parasitic elements with reset requirements, the designers achieved an automatic and perfectly balanced magnetics-reset scheme for a single-



2. ASYMMETRICAL power transfer (APT) provides an alternate way of balancing core-reset time, forward-conduction time, and peak-voltage stresses in forward-mode converters. Rather than use two primary windings, as in push-pull topologies (a), or a catch winding, as in single-ended topologies (b), the APT converter uses parasitic elements to balance reset requirements (c). The result is an extension of the duty cycle to 67%, a reduction of voltage stresses on semiconductors, and an increase in overall power transfer to very-high-density levels.

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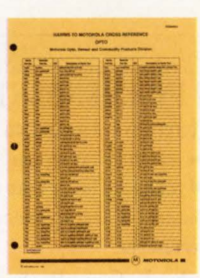

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ended converter that could extend the supply's duty cycle to 67%. At the same time, the voltage stress on the associated semiconductors was reduced.

The result is the elimination of the reset winding, which allows more area for the power winding and the use of lower-on-resistance power MOSFETs and lower-voltage rectifiers. The technology also provides effective snubbing of voltage transients without using dissipative snubber circuitry. This development allows all of the winding area of the magnetics to be used to transfer power—none was wasted on providing symmetrical reset functions. The combined result of the discovery meant dramatically increased transfer efficiency using a constant-frequency, pulse-width-modulated (PWM) topology that provides low-noise, constant-frequency operation, and permits the implementation of a multiple-output converter design.

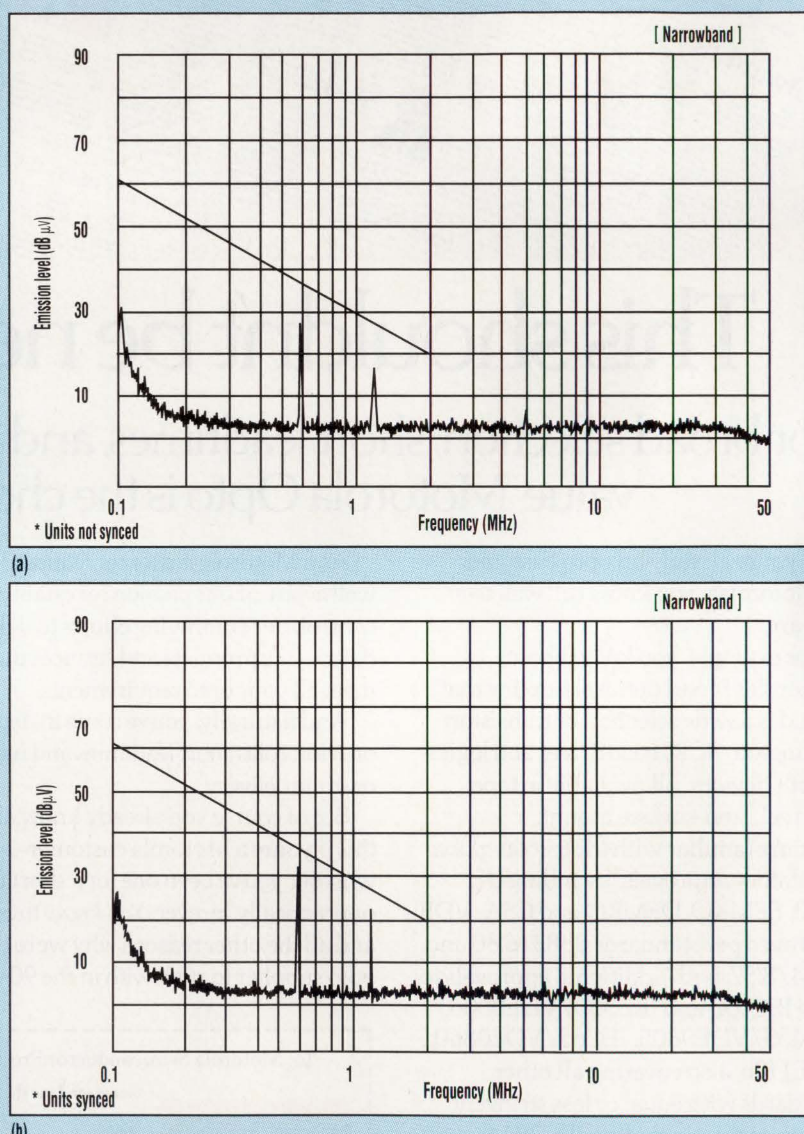
BEEFED-UP MAGNETICS

By itself, however, the APT technology won't result in VHD power supplies. Other advances were needed in the magnetics design. To achieve true very-high-density power levels, the MFLHP converters use new magnetics designed to maximize the copper area available for power transfer. The basic effect is to increase the amount of power the magnetics can handle.

The first magnetics-design change that the MFLHP engineers made was to work with magnetics suppliers to develop new materials that provide an optimal aspect ratio. The goal was a ratio that maximizes current-carrying copper and minimizes ferrite volume and turn length. The design provides a square aspect ratio and is about half the height of conventional magnetics. It was also designed specifically for bobbinless windings using flat copper (planar conductors). By eliminating the interstices inherent in round wire and the area wasted in bobbins, the new magnetics can achieve up to an 80% copper-fill factor (standard round wire wound on a bobbin has a typical copper-fill factor of around 50%). Planar-cross-section conductors also reduce losses by minimizing the high-frequency ac resistance of the conductor. The chief effects involve minimizing skin-effect depth, interwinding capacitance, leakage inductance, and hysteretic loss.

Even the impregnation process for the magnetic elements uses a special low-loss, highly thermally conductive compound designed to help enhance thermal transfer. The compound was selected for its low corona, low losses, high thermal conductivity, and a good thermal match with ferrite materials.

The height of the magnetics is also crucial in boosting converters to VHD levels. Because the magnetics are the tallest components of a power supply, reducing their height is essential to reducing the overall vol-



3. IN BOTH INDEPENDENT and current-sharing modes, the MFLHP converters offer several different synchronization schemes to help reduce interference from switching noise. With three current-sharing units operating in a free-run, unsynchronized mode (a), common spectral peaks are lower than in synchronized units (b). Synchronization, however, eliminates the chances of beat frequencies and allows switching transients to be timed to avoid circuit interference.

ume of the supply. The low-profile magnetics used in the MFLHP reduce its height to only 0.380 in. That dimension is important in two respects. Power supplies are typically the tallest element on a pc board, so reducing their height allows closer board-to-board spacing and reduces overall system area.

The MFLHP converter's lower height also aids thermal transfer. Because the most efficient way for a power supply to dissipate heat is through a conductive path to a heat sink (this sink can be a pc board, a cage wall, or a commercial heat sink), more surface area means better overall conductive thermal transfer. Lower height maximizes surface area for a given volume. An equally dense converter with a height of 0.500 in., rather than 0.380 in., would have 24% less base-plate conductive area for dissipating heat.

In addition to its magnetics and magnetic-control system, the MFLPH converter also enlists a new regulation-feedback mechanism: a cascaded current-error/voltage-error (CE/VE) amplifier feedback circuit. Voltage-error feedback is the most commonly used variety in dc-dc converters. It offers wide bandwidth over a very large load range—from designed discontinuous current to full load—and provides excellent load and line transient response. It's also relatively easy to implement. It does have two drawbacks, however: Transient response drops off at very light loads as the magnetics become discontinuous, and it is difficult to create current-sharing modes for paralleling converters.

Best Of Both Worlds

A current-error amplifier circuit provides very good transients at low loads and makes it easy to parallel converters without complex interconnect circuitry. However, the system-loop dynamics are affected by the load impedance (effective bandwidth, a function of the load, is less than optimal over a wide load range). The MFLHP converter's CE/VE feedback mechanism combines the advantages of both systems. It offers wide bandwidth, insensitivity to load impedance, and excellent transient response at any load.

The MFLHP converter's CE/VE system also simplifies parallel current-sharing operation. Up to three MFLHP units can be paralleled with no external circuitry, and any unit can serve as a master or slave unit in the current-sharing circuit. In addition, the feedback mechanism and independence of the units makes several different synchronization schemes possible. All units may be synchronized using a system clock, or all may be free-running (not synchronized). MFLHP converters may

HIGH-DENSITY DC-DC CONVERTER

also be synchronized unit-to-unit and either tied to the system clock or allowed to operate in the free-run mode *(Fig. 3)*. This gives designers wide latitude in controlling input and output emissions. Synchronized units tend to occur at times when digital signals or sampled analog signals are not affected. In a free-run mode, spectral peaks are not additive, but dissimilar frequencies can generate beat frequencies.

One of the most interesting effects of the CE/VE feedback is that it lets users select either voltage- or current-mode output control. A voltage-control mode, which is the near-universal norm for dc-dc converters, always holds the output voltage constant. For loads that have very low initial resistance, inrush currents can become extremely high. With the MFLHP, users can elect to eliminate inrush spikes by using the part as a constant-current source. In this scheme, the output current can be programmed with an externally applied voltage or current signal. In this mode, the output voltage changes to accommodate the differing resistances. Constant-current sources are ideal for driving loads like I^2L logic and for some applications, such as lamps that have very low initial resistance.

HIGH-REL HYBRID

The MFLHP converter is designed to operate in the high-reliability environments that are typically associated with aerospace and military programs. The part is a full hybrid and is hermetically sealed in a gold-plated, welded case. It's designed to pass full military-screening levels for fine and gross leaks, constant acceleration, temperature cycling, and burn-in, as well as resistance to solvents, salt spray, and high vibration. Internal circuitry allows it to meet the severe transient-protection standards defined in DO160, MIL-STD-704 A through D, and MIL-STD-1275, without the addition of any external components.

Extensive internal filtering, which is performed using low-height, multilayer ceramic capacitors, provides extremely low input and output noise and reliable high-temperature operation. Without external components, the MFLHP has typical output ripple of 20 mV pk-pk to 20 MHz and typical input ripple of 10 mA pk-pk over the same bandwidth. And because the parts have a constant-frequency PWM design, the noise is also predictable and easily filtered. When the units are used with an external companion filter, they meet the stringent MIL-STD-461 CE03 noise standards. The part is also designed using NAVMAT derating guidelines. The typical derating standards applied are 30% or less for current or power ratings, 60% for steady-state voltage ratings, and 80% or less for transient voltages.

The MFLHP converters offer full-power operation over a wide temperature range of –55 to +85°C, and over a wide input-voltage range that meets the operating conditions defined by MIL-STD-704 (19 to 40 V dc for normal operation). The standard also supports input voltages defined for emergency operating conditions. The parts offer efficiency up to 84%, which minimizes heat-sink requirements. Single- or dual-output models are available with 5-, 12-, 15-, ±12-, and ±15-V outputs.

Other features of the MFLHP converter include inhibit functions, low-voltage lockout, and overcurrent protection at the outputs. In the free-run mode, conversion frequency for the part is approximately 600 kHz; when controlled with a system clock, it can be set at any frequency between 500 and 675 kHz.□

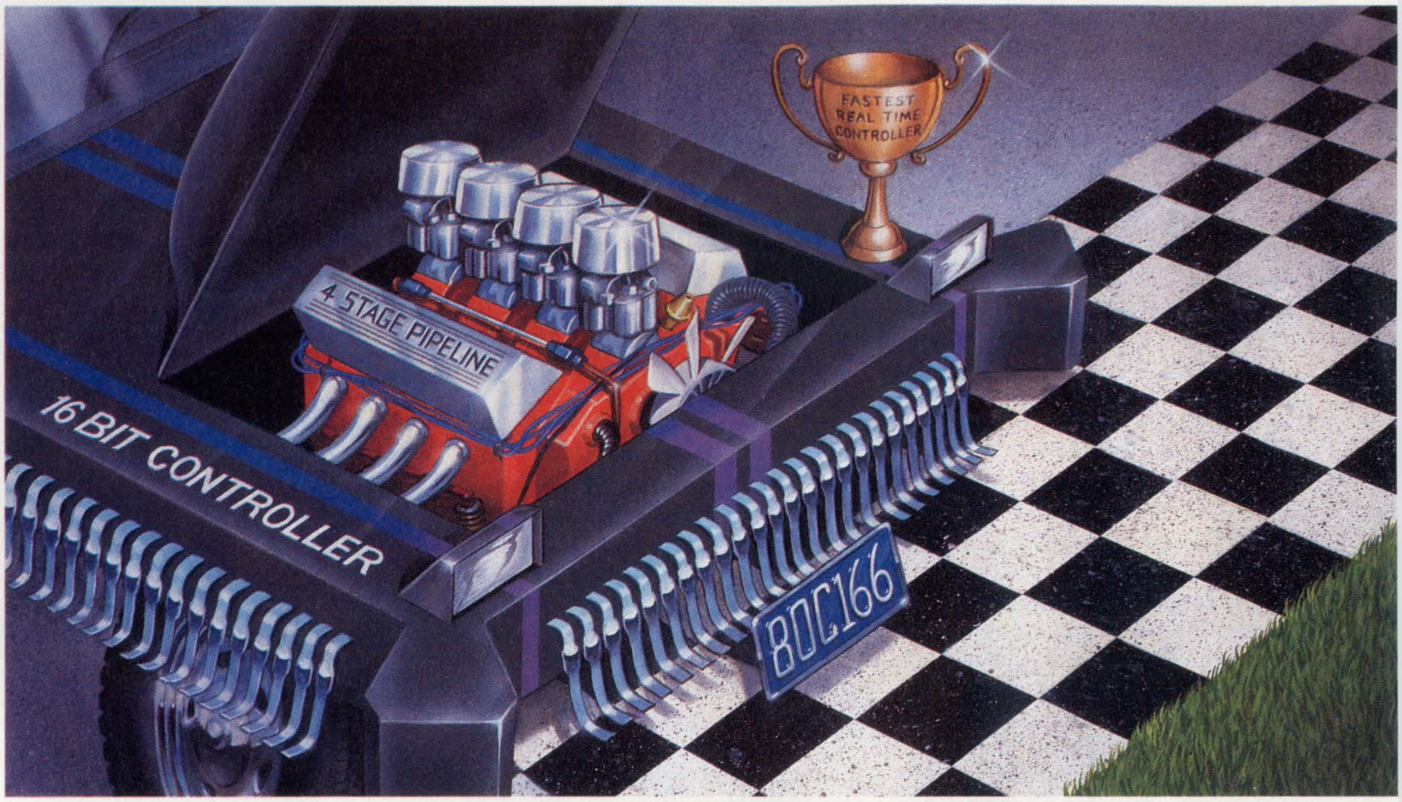
PRICE AND AVAILABILITY

The MFLHP dc-dc converter starts at under $700 each in OEM quantities. Single-output units will be in stock by the end of March, while dual-output units will be available by the end of summer. Interpoint is evaluating how its asymmetrical power-transfer technology will be applied to commercial parts.

Interpoint Corp., 10301 Willows Rd., P. O. Box 97005, Redmond, WA 98073-9705; David Uvelli, (800) 822-8782. **CIRCLE 511**

HOW VALUABLE?	CIRCLE
HIGHLY	541
MODERATELY	542
SLIGHTLY	543

SIEMENS



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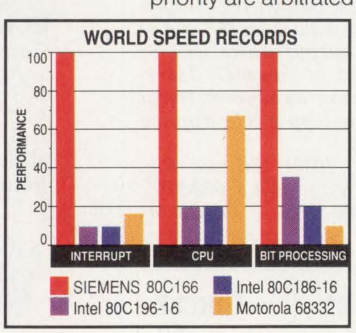

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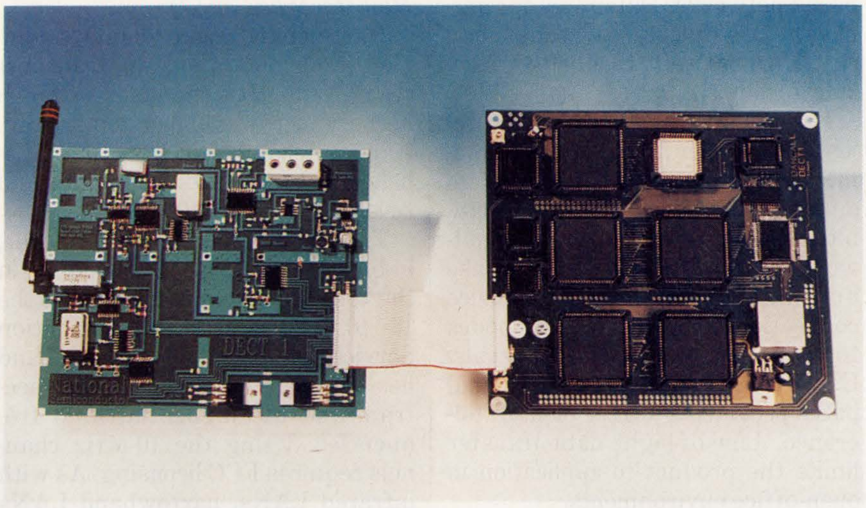


Photo: National Semiconductor/Dancell Radio

WIRELESS DATA LINKS BROADEN LAN OPTIONS

MILT LEONARD

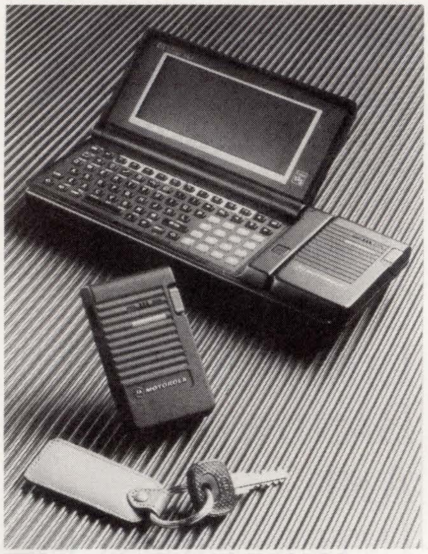
VENDORS AND REGULATORY BODIES CONFRONT LIMITED-BANDWIDTH AND INTERFERENCE PROBLEMS.

Wireless networks for data-communications systems continue to establish themselves as alternative solutions to problems posed by hardwired networks. Twisted-pair, coaxial, and fiber-optic cabling within a building environment are difficult and expensive to install, maintain, and change. Labor and material costs for wiring can reach $1000 per node just for copper wire; coax and optical-fiber costs are considerably higher.

The news gets worse when nodes are added or relocated. Studies by NCR Corp., Dayton, Ohio, show that over one-half of office workers with personal computers move annually. Other studies find that data terminals move as often as 1.5 to 3 times per year with an estimated cost of $200 to $1000 per wiring change. Plus, there's the loss of productivity due to downtime for recabling and resolving problems, such as cross-talk, impedance matching, signal degradation, and data security.

Given the expense and performance limitations of hardwired networking for in-building applications, the concept of using electromagnetic energy to transmit data becomes an attractive alternative. Some observers believe portable computers are an independent driving force with the potential of dominating wireless applications. However, wireless data transfer has its own limitations. Data rates are generally slower than wire-based networks, and the number of connected nodes and their separation distance are limited. Moreover, some wireless techniques are limited to line-of-sight communication. And initial installation costs for desktop computers may be higher than cable due to the electronics needed for communications.

Perhaps the biggest concerns among advocates of radio-based wireless LANs are issues of frequency allocation by the Federal



1. ONE-WAY WIRELESS transmission allows users of Hewlett-Packard's 95LX palmtop computer to receive information through national, regional, or local radio-paging services. Communications is provided by Motorola's NewsStream receiver, which mounts in a cradle tied to the computer.

Communications Commission (FCC) and the lack of standards for wireless technology. Both factors will influence the design of supporting hardware and software, and the degree of interoperability for wireless products. Bob Zavrel, product marketing manager for RF personal communications at GEC Plessey Semiconductors, Scotts Valley, Calif., says the lack of regulatory guidelines has created camps of zealous advocates who are lobbying for standard bandwidths that favor their technology base. "The regulatory environment is beset by a confusion of political, technological, and commercial interests," says Zavrel.

Wireless networks presently link computers through infrared light or radio waves. Implementations for both disciplines vary considerably between vendors. Infrared light signals operate in the electromagnetic spectrum above 1000 GHz. Although restricted to line-of-sight data links, infrared networks don't need FCC licensing and don't have severe bandwidth restrictions. Perhaps their biggest advantage are their high data rates, which are comparable to wire-based networks. Data rates for narrow-beam optical networks can equal or surpass 16-Mbit/s token-ring speeds.

For example, the InfraLAN wireless transceiver from BICC Communications, Westboro, Mass., offers data rates up to 16 Mbits/s. Compatible with token-ring and Ethernet networks, the product consists of a base unit that supports up to six device connections and two optical nodes for incoming and outgoing signals. Using primary and secondary signal paths provides a degree of fault tolerance. Line-of-sight data transfer limits the product to application in open-office environments.

Infrared products that bypass the line-of-sight limitation by diffusing the light beam reduce the need for precise alignment between the transmitter and receiver. However, they're limited to applications that don't require high data rates. One example of this approach involves the Photolink products from Photonics Corp., Campbell, Calif. Unlike BICC's infrared LAN, Photolink data transmissions are directed at a wall or ceiling to be sensed, decoded, and directed to the appropriate device by neighboring sensor modules.

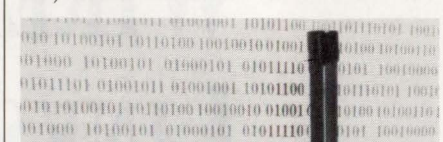
Each Photolink module connects up to four Macintosh computers or terminals, and communicates with other modules throughout an office over a 230-kbit/s infrared link. RS-232 and LocalTalk connections are used (the LocalTalk network is from Apple Computer Corp., Sunnyvale, Calif.). For laptop and portable computers, Photolink's Infrared Transceiver transmits and receives diffused infrared light at up to 1 Mbit/s.

Where infrared data transmission is a matured technology with well-defined advantages, limitations, and application areas, radio-based LAN technology is somewhat fuzzy around the edges. At present, two radio-based approaches are vying for dominance: spread-spectrum and narrowband. Spread-spectrum radio transmission uses complex circuitry to fragment data signals over a wide band of frequencies for increased immunity from interference and eavesdropping *(see "Spread spectrum: How it works," p. 57)*.

Narrowband radio employs simpler implementations to transport data in 10-MHz channels within a higher (microwave) frequency band. A narrowband data link is established by tuning the transmitter and receiver to the same frequency.

The FCC now permits low-power, in-building radio communication in the ten 10-MHz channels within the 18- to 19-GHz Digital Termination Services band. This frequency band lies between the lower spread-spectrum and the higher infrared frequencies. Using the 10-MHz channels requires FCC licensing. As with infrared LANs, narrowband LANs are implemented in various ways for different applications.

One example is the Altair line from Motorola Inc., Arlington Heights, Ill., which is an offshoot from the



2. THE IC-20 radio modem from Monicor uses narrowband transmission for two-way data transfer. Designed for use in large warehouses and process-control facilities, the battery-operated handheld unit has a maximum line-of-sight range of 75 miles. It can act as a base station or a mobile station.

FDDI. From deskwork to network.

Good news for networks!

The X3T9.5 Task Group, under the procedures of ANSI Accredited Standards Committee X3, has reaffirmed approval of the Media Interface Connector (MIC) for the proposed FDDI (Fiber Distributed Data Interface) Physical Layer Medium Dependent (PMD) document.

More good news! AMP has the complete fiber optic interconnection system—the AMP OPTIMATE Fixed Shroud Duplex System—that meets all FDDI PMD requirements. And includes all the physical components you need to make your fiber optic network a reality.

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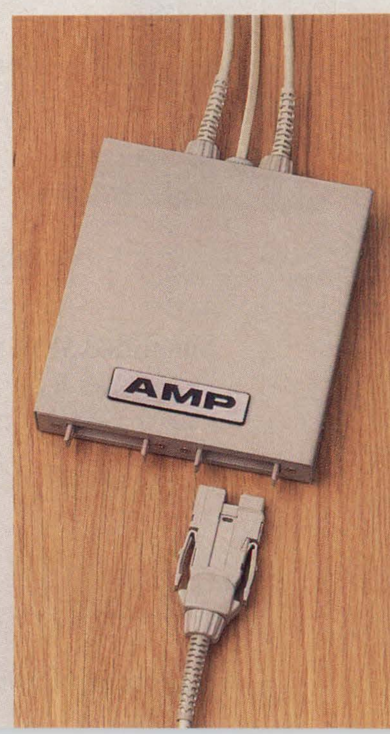
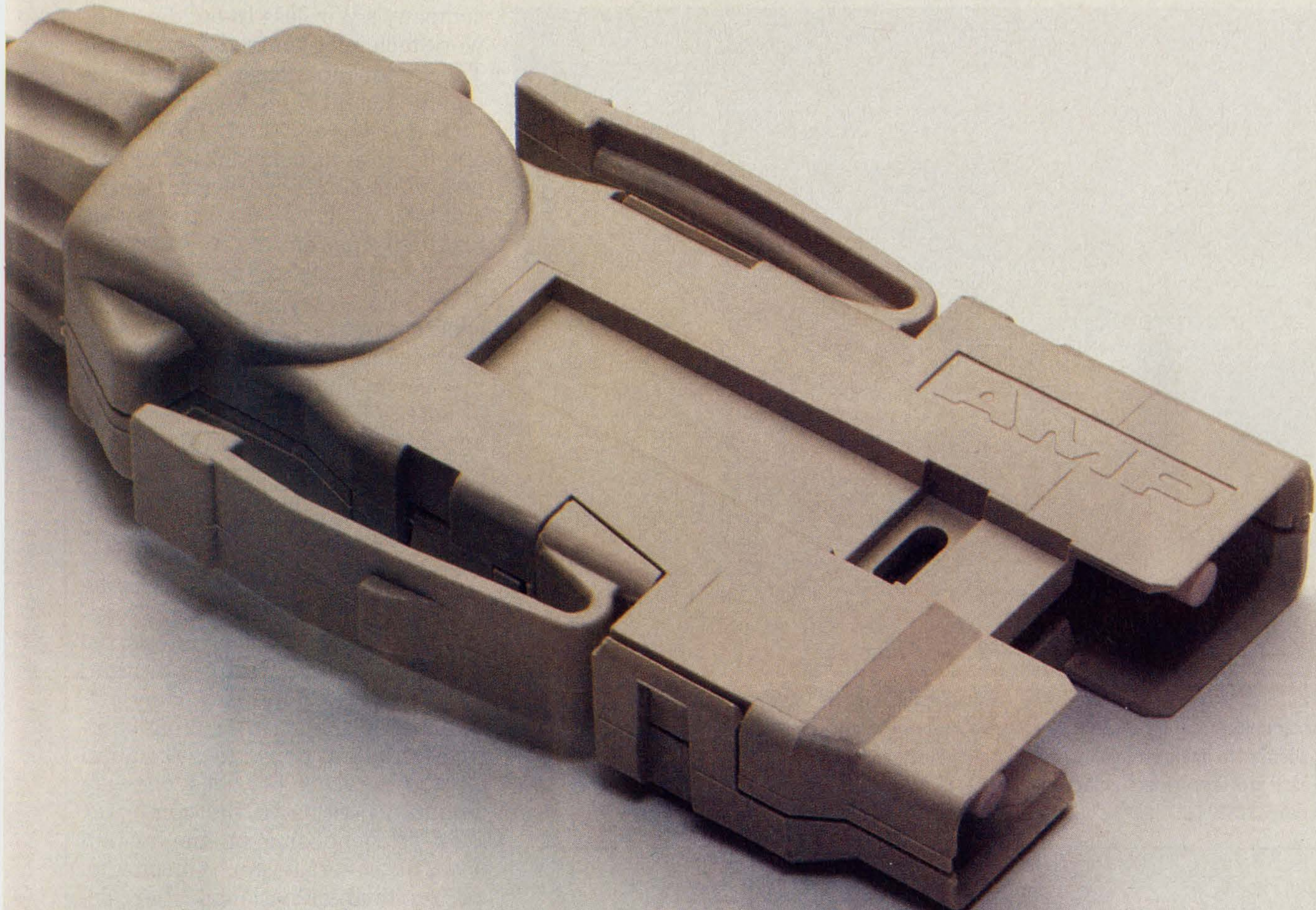
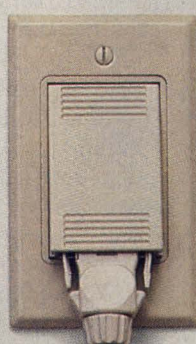
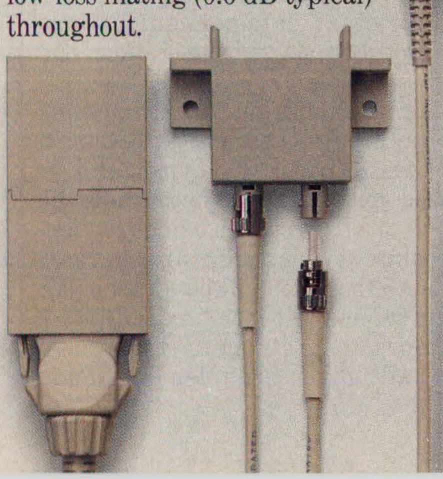




All system components, in fact, are easy to install and reconfigure. Our field termination kit makes short work of attaching duplex connectors to fiber cable. And because all interconnections use a floating interface, you get consistent, low-loss mating (0.6 dB typical) throughout.





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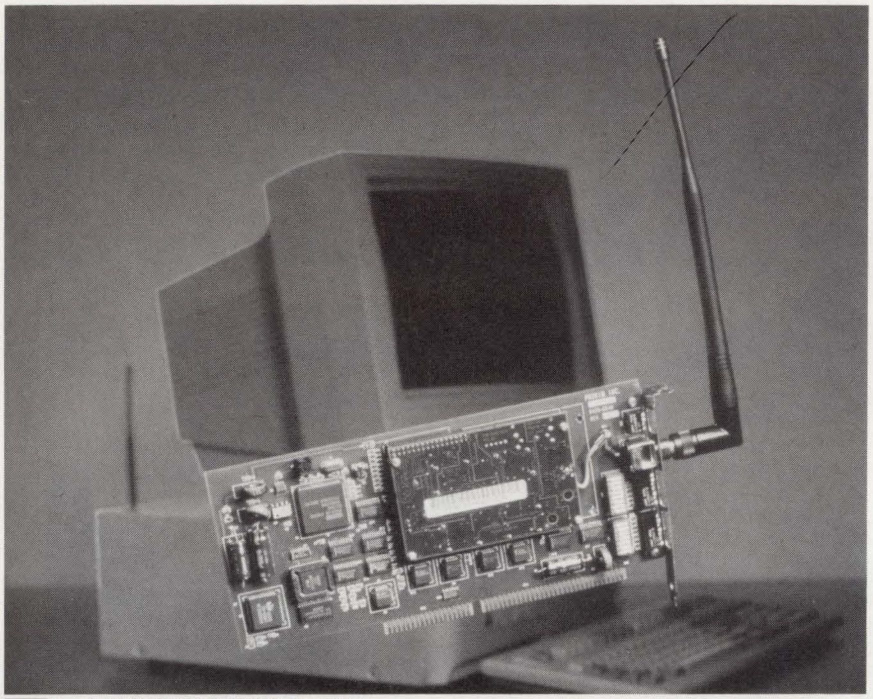
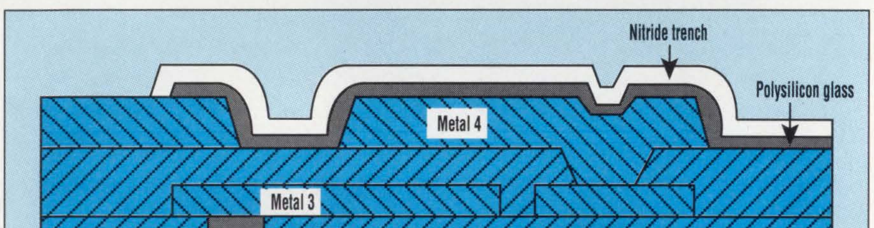


3. A PC ADAPTER CARD from Proxim is based on a patented spread-spectrum technology that provides three communications channels and a data rate of 242 kbits/s. In addition to having a small antenna that extends from the PC backplane, the full-size ISA card provides driver support for a variety of network software. Maximum transmitting range is 800 ft.



4. DEVELOPED FOR WIRELESS SYSTEMS operating in the 900-MHz-to-2.5-GHz frequency range, National Semiconductor's ABiC IV biCMOS process can combine analog-to-digital and digital-to-analog converters, wideband amplifiers operating at gigahertz frequencies, and digital logic on the same die. Among other features, the 0.8-μm, single-polysilicon process uses fully recessed oxide isolation, a 150-Å gate oxide, twin buried layers, and up to four levels of metallization. As a result, the process produces bipolar transistors with 15-GHz speeds, CMOS gates with 100-ps switching speeds, and biCMOS gates with typical speeds under 200 ps.

company's Wireless In-building Network technology introduced in 1990. The product line consists of a ceiling-mounted control module that hooks up to a server or Ethernet backbone, and desktop user modules that connect up to six devices each. Control and user modules automatically adjust to the appropriate frequencies.

Although line of sight isn't required, the signal will be blocked by concrete or steel. User data rate is specified at 3.3 Mbits/s, and the 25-mW power output produces a range of 130 ft. Motorola says the low propagation rate of 18-GHz signals allows portions of the spectrum to be reused without interference. For security, the system encrypts data prior to transmission.

Motorola's narrowband technology is also used in its NewsStream Receiver, which has been integrated with the 95LX palmtop personal computer developed by Hewlett-Packard Co., Palo Alto, Calif. Mounted in a cradle attached to the computer, the receiver provides one-way communications to the computer *(Fig. 1)*. Depending on the system used, the coverage can be on-site, local, regional, or national. When detached from the computer, the RS-232 device can receive and store up to 32 kbytes of data for a later download to the 95LX.

When utilized as a data-entry terminal, a 2-W narrowband radio modem for wireless LANs from Monicor Electronic Corp., Fort Lauderdale, Fla., operates in the 450-to-470-MHz FM band *(Fig. 2)*. Although the IC-20 modem can operate over a 75-mile line-of-sight radius, it's designed for use in large warehouses and process-control sites. The firm's proprietary data-communications protocol supports base stations and up to 48 mobile stations.

In operation, the modem accepts data through a serial RS-232C port; processes bar code, keypad, or digitized voice data; and broadcasts the data to a base station using frequency-shift-keying coding at data rates from 50 baud to 19.2 kbaud. Transmit and receive response time is 2 ms.

Spread-spectrum systems have equally diverse implementations.

NCR's WaveLAN consists of a circuit board cabled to an omnidirectional antenna and mounted in a housing for location near a PC. Capable of up to 2-Mbit/s data-transmission rates, the spread-spectrum system doesn't need an FCC license and supports any number of PCs located within 1000 ft. The use of a directional antenna increases operating range to five miles. Moreover, the system allows individual wireless nodes to be connected to a hardwired backbone. In a typical office environment, one PC used as a file server can be equipped with both a WaveLAN module and a backbone connection. WaveLAN uses the Ethernet carrier-sense, multiple-access with collision avoidance (CSMA/CA) protocol to handle data collisions.

A novel spread-spectrum system innovated by Proxim Inc., Mountain View, Calif., also comprises a circuit board with an attached antenna. When plugged into a full-length PC slot, the antenna extends from the backplane *(Fig. 3)*. RangeLAN has a range of up to 800 ft. and a data rate of 242 kbits/s. Proxim's patented technology divides the available 902-to-928-MHz bandwidth into three subchannels for added noise immunity. This can occur when the user selects the most noise-free channel. "The band partitioning also effectively triples available bandwidth when used concurrently," says Paul Smith, vice president of marketing at Proxim. The product also has a patented post-correlation circuit for signal capture that contributes to low cost, low power, and small size.

The relative merits and weaknesses of narrowband and spread-spectrum technologies provoke considerable debate. Advocates of narrowband technology point out the data-rate limitations of spread-spectrum systems operating within the constricted 900-MHz frequency band. The argument continues that present FCC bandwidth allocation for spread-spectrum communications can't support more than about 20-Mbit/s data rates, which is only one-fifth of the preferred 10-Mbit/s data rate for data communications.

Narrowband supporters concede

SPREAD SPECTRUM: HOW IT WORKS

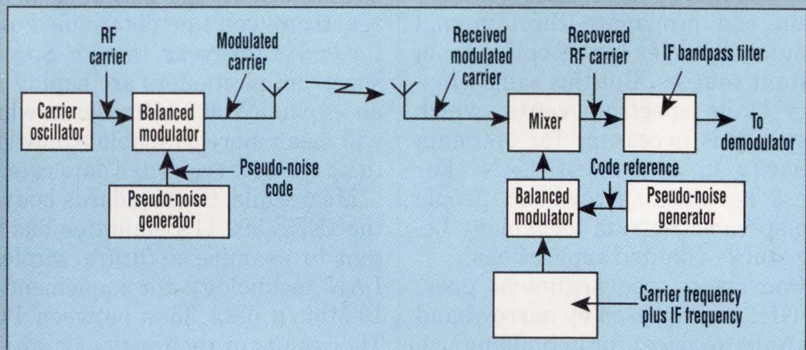
Spread-spectrum data transmission originated in military communications systems that required high immunity to electromagnetic noise, jamming, multi-path signal distortion, and eavesdropping, while preserving high data-transmission integrity. For wireless-LANs, it also offers full compatibility with multiple-access, multiple-user requirements. And it also has the potential for wider bandwidths than what's available.

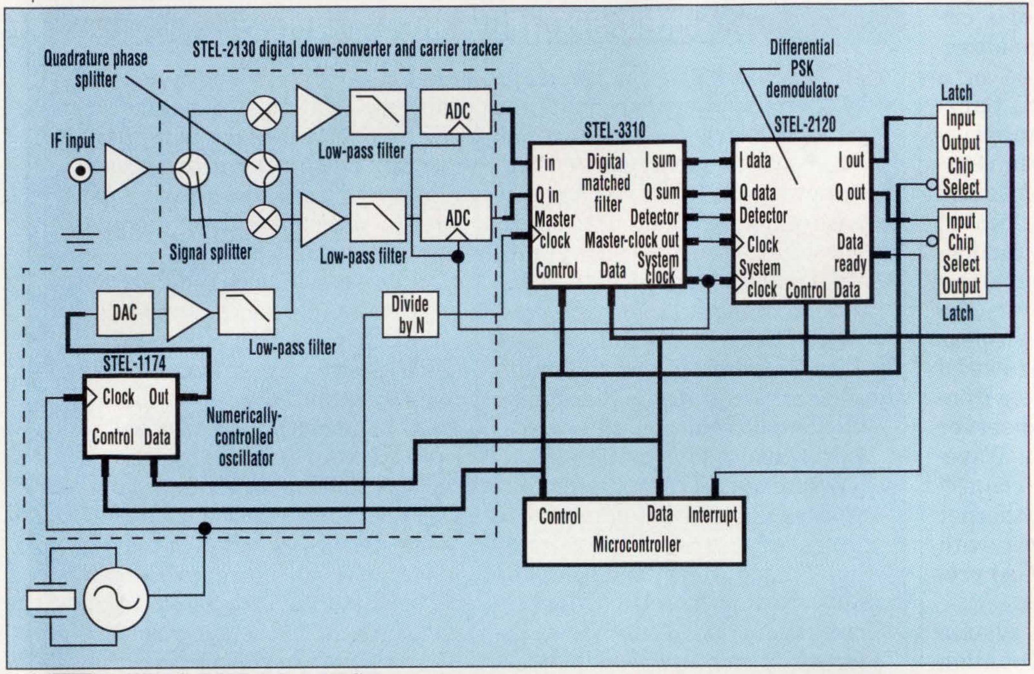
A spread-spectrum system distributes transmitted data over a range of carrier frequencies that's much wider than the minimum transmission bandwidth. A baseband signal of only a few kilohertz is obscured or hidden within a frequency band that's many megahertz wide. At the receiver, the signal is remapped into the original information bandwidth. The result is error-free data transfer in the presence of noise.

The most popular spread-spectrum modulation schemes are direct sequence, frequency-hopping, and pulsed chirp. Direct-sequence modulation uses a code sequence to phase-modulate the carrier across a continuous band of frequencies. Unlike direct-sequence spread-spectrum techniques, carrier-frequency shifting or frequency-hopping shifts the data-modulated carrier frequency across a spectrum of multiple discrete frequencies in a pattern determined by a code sequence. Pulsed-frequency or chirp modulation sweeps the carrier across a wide frequency band during a pulse interval and is used mostly in radar. For wireless LANs, direct-sequence modulation is commonly used.

In direct-sequence modulation, the carrier frequency is modulated by a pseudo-random-noise (PRN) source and the coded data to be transmitted *(see the figure)*. Total bandwidth increases as the rate of these two signals increases, and immunity from interference increases with bandwidth. Secure communications is inherent because the receiver local oscillator and transmitter output signal must be synchronized by some predetermined code that modulates the data stream.

Baseband data is usually digitized and added to the PRN code sequence. The composite signal is then mixed with the carrier-oscillator signal in a balanced modulator, amplified, and mixed at the receiver with a reference that has the same code. The receiver next restores the baseband signal which is sent through a filter that passes only the baseband-modulated carrier. Direct-sequence modulation requires simple circuitry and has good performance. Also, using code-division multiplexing lets multiple users employ different codes to operate simultaneously on the same frequency by applying identical single-carrier transceivers.





5. THIS THREE-PIECE **spread-spectrum demodulator ASIC chip set developed by Stanford Telecom is used in a spread-spectrum receiver. One particular chip, the STEL-2130, integrates many functions that formerly required several chips.**

that RF energy in the UHF environment can propagate through and around obstacles for reception from distant sources. But this same property limits spectrum reuse, which they say is necessary for optimum capacity in a wireless LAN. For these reasons, narrowband people see spread-spectrum technology being stuck in limited applications.

Conversely, the argument goes, 18-GHz signals used by narrowband systems are ideal for in-building use because signal reflection and diffusion can fill a microcellular area using a minimum amount of power. The same frequencies can be reused by other neighboring systems. Moreover, the 18-GHz band is high enough to avoid interference to or by other electrical equipment.

Still, many industry observers expect spread-spectrum technology to thrive in the wireless-LAN arena because of two reasons: its inherently high immunity to interference and the forthcoming new frequency allocations from the FCC.

The FCC recently proposed opening up 220 MHz of the electromagnetic spectrum to accommodate new wireless services. Just where this bandwidth will be allocated in this spectrum won't be determined until the end of this year, though. Spread-spectrum petitioners are hoping for an expanded 900-MHz band, which will mean more available bandwidth to up the now restricted data rate.

Meanwhile, the standards body of the IEEE 802.11 Committee has begun to examine a future wireless-LAN technology for implementing 10-Mbit/s data links between PCs. The results of their actions may significantly influence the product plans of IC chip makers who supply wireless-LAN ICs. These companies include GEC Plessey; Motorola Inc., Austin, Tex.; National Semiconductor Corp., Santa Clara, Calif.; NCR Corp.; Qualcom Corp., San Diego, Calif.; Signetics Co., Sunnyvale, Calif.; and Stanford Telecom Inc., Santa Clara, Calif. By virtue of its involvement in Europe's Digital European Cordless Telecommunications (DECT) program, National Semiconductor is already positioned to supply any wireless technology the standards bodies may favor.

Europe is acknowledged as being a year ahead of the U.S. in establishing digital wireless standards for systems operating beyond 900 MHz. For wireless digital communications, the DECT standard specifies a 1.88-to-1.9-GHz carrier, 250 mW of transmission power, and a 1.152-Mbit/s data rate. National has been working with Denmark's Dancall Radio A/S to develop a transceiver for Pan-European digital communications.

The transceiver board is based on National's bipolar ASPECT IV process, which can implement wideband amplifiers, mixers, phase shifters, oscillators, and frequency synthesizers operating at multigigahertz frequencies. The firm's next-generation ASPECT process, ABiC IV, will mix bipolar and CMOS transistors to integrate unique combinations of switching speed, bandwidth, dense logic, embedded memory, multiple I/Os, and analog and radio functions on one chip for wireless systems *(Fig. 4)*.

GEC Plessey supplies building high-frequency communications blocks, including a 3.5-GHz prescaler for synthesizers, mixers, amplifiers, and digital-signal processors. Processes are on-line to produce npn 14-GHz transistors and 24 GHz later.

Stanford Telecom also has established a base of high-frequency building blocks for telecommunications. Primarily for spread-spectrum systems, these ASICs include modulators and demodulators, pseudonoise coders, and forward-error-correction circuits. A recent design produced a three-piece, spread-spectrum demodulator chip set that reduced the parts count of a prior design by one-half *(Fig. 5)*. The entire design is expected to shrink to a single IC by the middle of this year.□

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Inexpensive Routers Can Overcome Such Bridge-Based Internet Problems As Limited Address Space And Broadcast Storms.

Low-Cost Routers Can Tame Complex Global Internets

Although the personal-computer revolution began with standalone PCs, it was only a matter of time before corporate users discovered that they often needed access to resources beyond those available on their individual machines. The result was the local-area network (LAN), which connected the PCs within a small working group—typically between 10 and 100 computers—to each other. Now those same users are finding that they need access to facilities and data beyond those available on their individual networks. Hence the emergence of the internet—a network of networks that can span an entire enterprise even if it stretches around the globe. As long as the LANs comprising the internet all use compatible ISO LAN protocols, the total number of users is fairly small, and the internet configuration doesn't change too often, few problems will arise if simple bridges are used to interconnect them. But if the internetwork is to serve a large corporation, it will probably contain tens of thousands of diverse devices.

In addition, its computers and their subnets will be of differing types. That size and diversity mean that bridges will often be inadequate to successfully interconnect the individual LANs.

More powerful tools will likely be needed. Tools like routers. The only reason routers haven't seen broader usage is that, until recently, they were quite expensive, often coming in at prices in excess of $15,000. Today however, thanks to recent developments in 32-bit LAN controller chips and RISC processors, a high-performance router can be built from less than $2000 worth of parts.

To understand how a router can help manage a network, it's worthwhile to review how bridges work and to look at the various types of problems that can occur in an internet.

Bridge Basics

Bridges are a practical, cost-effective method for connecting a small number of similar LANs. They can, however, only be used to link LANs with compatible protocols for layers 1 (physical) and 2 (data link) of the OSI network protocol model. Their effectiveness can be reduced as corporate-wide networks increase in size, diversity, and topological rate of change.

One problem that occurs as network size increases is difficulty in handling the large number of data-link addresses representing the stations on all of the connected LANs. Each bridge must maintain a list of every address. The trouble is that most bridges are designed to handle only a few thousand of them. Increasing a

BRIAN EDEM, AVI BAREL, and KAREN PARKER
National Semiconductor Corp., MS D3615, Box 58090, 2900 Semiconductor Dr., Santa Clara, CA 95052; (408) 721-4402.

ROUTERS TAME COMPLEX INTERNETS

bridge's address capability is expensive because it requires costly content-addressable memory.

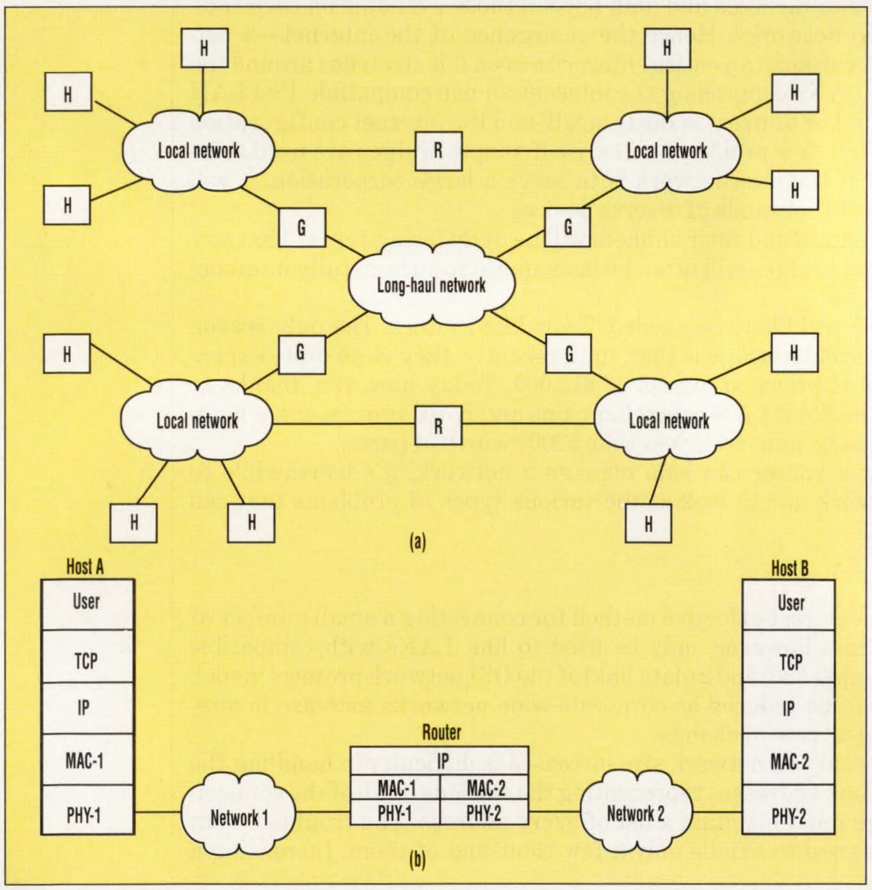
Bridges check the destination addresses of all packets they receive to see if they're local. If they are, the bridge discards them. If not, it simply forwards them to the next LAN. Bridges can't actually route non-local packets—that is, to determine an optimal path and send the packets along that path.

Bridge Problems

Bridges frequently have difficulty responding to changes in network topology, whether caused by adding, dropping, or moving users, or by switched service connections. The problem isn't bad if the changes occur at a slow pace, but bridges have difficulty remaining stable when the rate of change is high.

The most significant problem with bridges, however, is their susceptibility to broadcast storms. If a bridged internet achieves reliability by providing many redundant paths, loops may exist over which broadcast messages can be regenerated, causing them to spread like wildfire through the network. Sometimes receiving a particular broadcast message causes a station to respond with a broadcast message of its own. In such cases, a chain reaction results. That leads to an upsurge in network traffic, which can slow communication to a standstill.

To minimize the likelihood of broadcast storms in bridged internets, the internet topology is often limited to tree structures with only one delivery path. The trouble with that approach is it reduces the network manager's flexibility to respond to clogged internetwork connections.



1. THIS GLOBAL INTERNET includes local-area networks (LANs); hosts (H), which concentrate user connections onto the LANs; routers (R), which connect the LANs to one another; and gateways (G) that provide access to worldwide communication services (a). The routers implement the first three layers of the OSI network protocol standard (b).

Routers overcome many of the aforementioned drawbacks of bridges and provide additional benefits as well. To perform their primary function of reliably directing packets through a group of interconnected networks *(Fig. 1a)*, they implement the first three layers of the OSI network protocol model—physical, data link, and network *(Fig. 1b)*. Unlike bridges, which implement only the first two layers, routers permit translation among different address domains.

The most commonly implemented network layer function used today is the Internet Protocol (IP). The IP header contains both source and destination addresses *(Fig. 2)*. Each address specifies the host ID and Network ID. A router that receives a packet reads the destination network IP address and looks it up in a routing table. The table specifies a path over which the packet can reach its destination, including the address of the next hop and how many hops it will take to reach its destination. That path-determination function is called routing, and is the main function of a router.

After looking up the destination network address, the router forwards the packet to its next destination as defined by the routing table. The table is continually updated with the latest routing information, so, if congestion clogs the usual path, a better one can be specified.

Routers time-stamp the packets they receive *(Fig. 2)*, which gives them a powerful tool to reduce the effects of broadcast storms by blocking the passage of old messages. More importantly, because they recognize all addresses on the internet, they can reduce the need for broadcast messages. With routers, messages can be sent separately to different portions of the internet, accomplishing the same goal without the danger of a chain reaction.

Routers are a powerful management tool, which network managers can use to regulate access to computer resources. They can do so by controlling the flow of data between networks based on the destination and source addresses. That capability ad-

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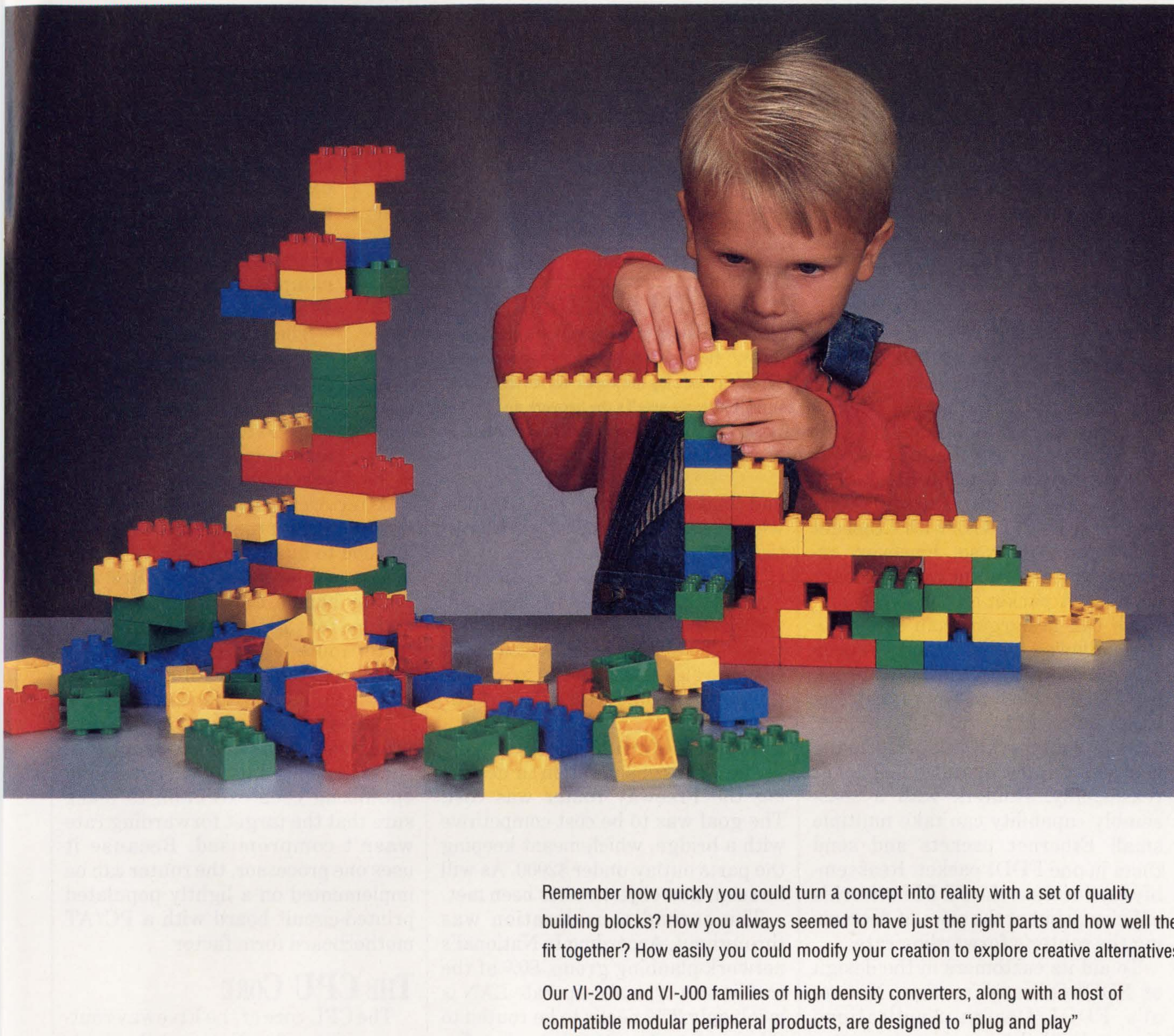

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dresses network security issues as well. In the event of a fault, routers can redirect traffic and reconfigure the network to avoid the failed link. They can also notify a source station of a lost packet, instead of relying on a higher-level protocol to notice the loss. This increases the network's reliability and efficiency.

0	7	15	23	31
Version	IHL	Type of service	Total length	
Identification			Flags	Fragment offset
Time to live		Protocol	Header checksum	
Source address				
Destination address				
Options - padding				
Data				

2. THE INTERNET PROTOCOL (IP) header contains fields to aid in effective network management. The "time to live" field is a time stamp used to remove old frames that may otherwise clog networks worldwide. The destination and source addresses specify the network and host address so that frames can be steered efficiently to their host and source stations can be notified of lost frame events.

PACKET FRAGGING

One strength of routers over bridges is their ability to work with LANs that implement different layer-2 protocols. In particular, routers may be used to interconnect fiber distributed data interface (FDDI) LANs with Ethernet networks. Doing so, however, requires that the router can fragment packets. A packet on the FDDI network can be larger than the maximum allowed by the Ethernet specification, so it's necessary to break the FDDI packet into more than one Ethernet packet.

Some routers can also perform the complementary operation—packet reassembly. Routers with a reassembly capability can take multiple small Ethernet packets and send them in one FDDI packet. Reassembly can increase the FDDI network's efficiency but at the price of decreasing the router's forwarding rate.

To aid its customers in the design of FDDI-Ethernet routers, National's FDDI Design Applications Group decided to engineer a router of its own. To ensure the practicality of the design, the Applications Group worked with the company's Network Planning Group to define an architecture that would function well with National's own worldwide networks. (National Semiconductor, like many other large corporations, has to connect hundreds of LANs around the world to support a wide range of computing activities including order entry, payroll, computer-aided design, electronic mail, finance, accounting, and automated manufacturing. Its network planners are very familiar with routers and make extensive use of them wherever it's economically and practically possible.)

The resultant router, called the Freeway router, has now been built and tested. Its design is provided here as a starting point, which builders of routers may use to reduce their own products' time to market.

DESIGN CONSIDERATIONS

The first consideration in designing the Freeway router was cost. The goal was to be cost competitive with a bridge, which meant keeping the parts outlay under $2000. As will be seen, that objective has been met.

The second consideration was throughput. According to National's network planning group, 80% of the traffic on a typical corporate LAN is local; only 20% needs to be routed to other networks. Based on that figure, if five Ethernet LANs are connected to one FDDI network, the required forwarding rate would be just 12,000 packets/s—the packet rate of one Ethernet LAN. That rate was thus made the design objective for the Freeway router. However, to leave a margin for error, the final design calls for only four Ethernet connections and one FDDI port.

CHOOSING AN ARCHITECTURE

In addition to cost, the choice of a router architecture is driven primarily by flexibility and forwarding-rate objectives. For the Freeway router, flexibility wasn't a requirement because the types of networks to be connected and the internet protocol were well-defined at the outset. The router was to have two main uses: connecting existing FDDI front-end networks to an Ethernet backbone, and connecting existing Ethernet LANs to a campus-wide FDDI backbone.

The moderate forwarding rate requirement of 12,000 packets/s could be achieved with one 10-MIPS processor. Using one processor also helped keep the parts cost to a minimum.

After carefully considering the bus bandwidth requirements, it was decided to build the Freeway router around a dual bus architecture: one bus to handle the network traffic, and one for CPU instructions (actually, the router also has a third bus—a low-speed, 8-bit control path—used mainly for initialization and monitoring). The design team could then deal effectively with two major router issues: avoiding bus bottlenecks and optimizing code execution to make sure that the target forwarding rate wasn't compromised. Because it uses one processor, the router can be implemented on a lightly populated printed-circuit board with a PC/AT motherboard form factor.

THE CPU CORE

The CPU core of the Freeway router consists of a National Semiconductor NS32GX320 microcontroller and its memory system *(Fig. 3)*. The system runs at a clock rate of up to 25 MHz, allowing a peak performance of 12 MIPS. The NS32GX320 has an on-chip interrupt controller, a two-channel DMA controller, separate instruction and data caches, and three timers.

Bus clocks for the entire system are generated by the processor. That greatly simplifies the design by making all bus masters run from the same clock.

To enhance overall system responsiveness, each peripheral within the

ROUTERS TAME COMPLEX INTERNETS

router able to generate an interrupt is assigned a different interrupt level. That makes it unnecessary for the software to poll for the source of an interrupt.

One channel of direct memory access is used by the SCSI controller to transfer data between it and the processor's memory. The SCSI controller was added to allow for peripheral expansion, but isn't necessary for the routing function.

The timers on the NS32GX320 are used by both hardware and software. One timer is employed by the memory systems to set the refresh interval of the DRAMs. A second timer is used by the protocol software to implement software timers, schedule tasks, and keep track of time. The third timer is used by the FDDI station management (SMT) software.

The CPU memory system consists of one bank of 32 DRAMs, which provide either 4 Mbytes or 16 Mbytes of storage, depending on whether the bank is composed of 1-Mbit or 4-Mbyte single in-line memory modules (SIMMs). The CPU memory is used for processor code, stack, and static variables. It operates in page mode, with a page size of 4 kbytes. Page-mode operation tries to amortize the time penalty of the initial access to a page of DRAM memory over several accesses by not completing the DRAM page access until forced to by an access to another page or a memory refresh cycle. Consecutive data accesses that occur within the same page, as is usually the case, are significantly faster using this technique.

THE NETWORK CORE

The network core of the Freeway router handles the actual data traffic. It consists of a memory system (the packet memory), a processor interface (the data buffer), the National Semiconductor FDDI chip set, and four National Semiconductor Ethernet controllers (Sonics). Access to the network bus by these multiple bus masters is controlled by a central arbiter in the network core (not shown in Figure 3). The processor access is of highest priority, followed by the network controllers. The Sonics arbitrate amongst themselves in a round-robin fashion and alternate as a group with the FDDI circuitry.

When no master is requesting the bus, the arbiter parks, granting the processor access. This eliminates arbitration delays for the processor when the bus is idle.

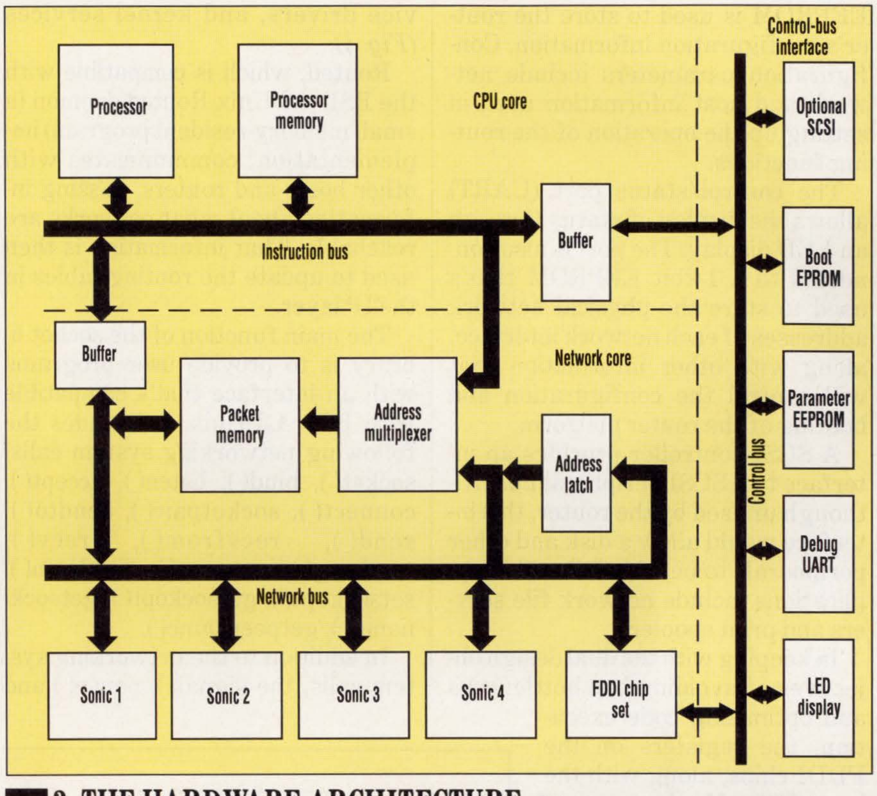
The network-core memory system is similar in size and operation to that used in the processor core except that it uses page-mode operation only for burst transactions. With the network memory, page access ends when the bus masters release the bus.

With the processor interface to the network data bus, the NS32GX320 processor can access both the network memory and the host programmable registers on each of the Sonics. Those Sonics, together with their associated passive components, create four Ethernet interfaces.

On the optical side of the board, the FDDI chip set, along with a pair of optical transceivers, implements a dual-attach connection to an FDDI ring. The chip set consists of a basic media access controller (BMAC), a BMAC system interface (BSI), two physical layer interfaces (PLAYERs), two clock recovery devices (CRDs), and a clock distribution device (CDD).

The router includes a UART to facilitate connecting a terminal that monitors the system's operation. It also provides a serial link for remote debugging of software for the router platform, a task that would otherwise require an Ethernet port.

Up to 1 Mbyte of EPROM is included in the router design for processor code—enough for a small application or for holding the code needed to boot across the network. An 8-kbyte



3. THE HARDWARE ARCHITECTURE of the Freeway router consists of three parts: the CPU core, the network core, and the control-bus interface. The CPU core provides a separate bus interface between the CPU and the instruction memory for higher performance. The network core has a separate bus for network traffic, four Ethernet ports, and one dual-attach FDDI port. The control bus consists of a control interface to the FDDI chip set, a UART for debug, a configuration EEPROM, a boot EPROM, and a SCSI port for the file server expansion option.

ROUTERS TAME COMPLEX INTERNETS

EEPROM is used to store the router's configuration information. Configuration parameters include network and host information used in setting up the operation of the routing functions.

The control/status port (UART) allows the display of status through an LED display. The port is also connected to a 1-kbit EEPROM that's used to store the physical network addresses of each network interface, along with other information that will control the configuration and booting of the router platform.

A SCSI controller provides an interface to a SCSI peripheral bus. Although unused by the router, this interface would allow a disk and other peripherals to be added. Possible applications include network file servers and print spoolers.

In keeping with the dual design objectives of avoiding bus bottlenecks and optimizing code execution, the registers on the FDDI chips, along with the boot EPROM, the parameter EEPROM, the UART, the control/status port, and the optional SCSI port, are connected to the processor via a separate, relatively slow, 8-bit asynchronous bus.

The Freeway router implements the widely used transmission control protocol (TCP) and internet protocol (IP) for its layer-4 (transport) and layer-3 (network) functions, respectively. The TCP/IP software processes incoming frames and forwards them to their destinations. That software gets the information it needs from routing tables maintained by a separate software module, called Routed (pronounced "Rout Dee"). Routed communicates connectivity information using the routing information protocol (RIP). Along with Routed and TCP/IP, the major components of the Freeway software include a Unix socket library, various device drivers, and kernel services *(Fig. 4)*.

Routed, which is compatible with the BSD 4.3 Unix Routed daemon (a small memory-resident program) implementation, communicates with other hosts and routers, passing information about what networks are reachable. That information is then used to update the routing tables in the IP layer.

The main function of the socket library is to provide user programs with an interface that's compatible with BSD 4.3 Unix. It includes the following networking system calls: socket( ), bind( ), listen( ), accept( ), connect( ), socketpair( ), sendto( ), send( ), recvfrom( ), recv( ), sendmsg( ), recvmsg( ), shutdown( ), setsockopt( ), getsockopt( ), getsockname( ), getpeername( ).

In addition to the networking system calls, the signal( ), pause( ) and alarm( ) system calls are also supported. Signal( ) supports only BSD's SIGALRM function. This allows the Routed program to suspend its execution until a specified period of time has expired.

INTERNAL SUPPORT

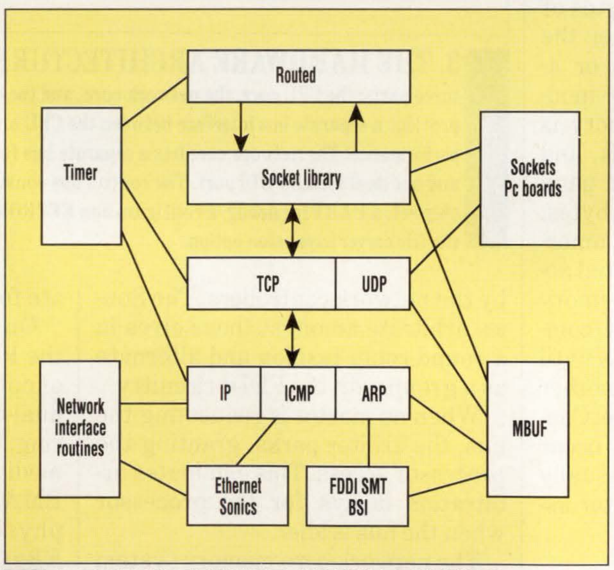
To perform in its main function of routing packets, the IP layer needs information not only from its routing tables, but also from databases associated with each interface. Network device drivers provide the necessary interface between those networking devices and the IP layer software. The drivers implement the required functions so that they easily link with the IP layer, and ensure that the hardware has the buffer resources for proper operation.

The TCP/IP software also requires several services usually provided by the Unix kernel. They include a form of memory management using a memory buffer (MBUF) mechanism, which provides a standard way to allocate memory blocks of different sizes and types.

Not only does the MBUF mechanism provide storage for data, it's also used by TCP/IP and the socket layer to store control information and dynamic lists.

In addition, the MBUF mechanism has an operating mode that references data outside of the MBUF structure in 4-kbyte pages. That capability is used by the device drivers, enabling the network hardware to receive frames directly in a form that the TCP/IP software can manage. Being able to map between the MBUF structures and the data structures generated by the hardware eliminates the time-consuming copying of the data, thereby greatly contributing to the router's forwarding capacity *(Figs. 5 and 6)*.

Timing is another service provided by the kernel. Sev-



4. THE SOFTWARE ARCHITECTURE of the Freeway router consists of four main parts: the buffer-management mechanism, the protocol-software module, the application software, and the hardware-interface software. The buffer-management mechanism uses a paged memory scheme and utilizes Unix MBUF data structures that are shared by the CPU and the network controllers. The protocol software consists of the IP, ICMP, and ARP modules, and may also include the transport protocol modules TCP or UDP (user datagram protocol). The application software consists of Routed and the socket library, which provide a standard BSD Unix interface to the router. The hardware-interface software consists of FDDI station management software and drivers for the Ethernet and FDDI chips.

ROUTERS TAME COMPLEX INTERNETS

eral tables use entry aging to determine when to remove entries. TCP and IP use the timing services to timeout packet reassembly and connections.

Within any communications product, the bandwidth requirement of each subsystem must be studied to ensure that it doesn't take up an inordinate amount of the total system bus bandwidth. Because the Freeway router's network memory is accessed by the FDDI ring, four Ethernets, the protocol processor, and its own refreshing circuitry, each of those devices must be analyzed to make sure that it doesn't become a bottleneck.

In the Freeway router, the transfer of data between the FDDI ring and memory is performed by the BSI. Its bus protocol utilizes burst transfers, which allows multiple words of data to be transferred efficiently between memory and the ring. The access to the first word of a burst requires six clock cycles, with subsequent words requiring two clock cycles apiece. The burst then ends with an idle cycle, giving a total of 21 clock cycles to transfer 32 bytes of data. If the router's bus clock runs at 25 MHz, the BSI will transfer data at a rate of 38 Mbytes/s, or 300 Mbits/s.

In addition to that peak transfer rate, the BSI requires additional bandwidth to fetch descriptors and store status. With an overhead of 25% above that used for data transfer, the BSI could be utilizing approximately 45% of the network memory's bandwidth.

The Sonics don't use burst transfers, but do utilize the memory's page mode of operation. The Sonic's "burst" consists of an initial word access that requires seven clock cycles, and three cycles for each subsequent 32-bit word fetched. This burst will be ended with three idle cycles, giving a total of 20 clock cycles to transfer 16 bytes of data. Again, using a 25-MHz clock, the Sonic transfers data at a rate of 20 Mbytes/s, or 160 Mbits/s.

With four Sonics, network traffic peaks at 40 Mbits/s. If 25% is assumed as overhead for descriptor operations, the Sonics will require 30% of the memory's bandwidth.

To relate the preceding analyses to the real-world operation of the router, three observations are pertinent:

- The Freeway router is indeed a router—that is, most of its traffic will pass from one network interface to another, with almost no overall accumulation or generation of traffic within the router itself.
- A worst-case condition will exist when all of the Ethernet traffic is routed to the FDDI ring.
- An Ethernet network is considered saturated when network traffic approaches 30% of the available bandwidth.

These observations and assumptions suggest modifying the previously calculated bandwidth requirements. It turns out the Ethernet interface will realistically reach 30% of the 30% bandwidth calculated, so only 10% of the memory bandwidth is needed. With all of the Ethernet traffic going through the FDDI ring, that will amount to only 12 Mbits/s, not the 100-Mbit/s capability of the ring. That reduces the BSI's required fraction of the network memory to 7%.

Adding the FDDI requirements to the Ethernet yields 17% of the bandwidth to transfer frames to and from the network, not the 80% calculated by adding the peak values together. The remainder is available for memory refreshing and CPU protocol processing. Memory refreshing, which must be performed every 15.7 ms, requires seven clock cycles, consuming about 2% of the bus bandwidth.

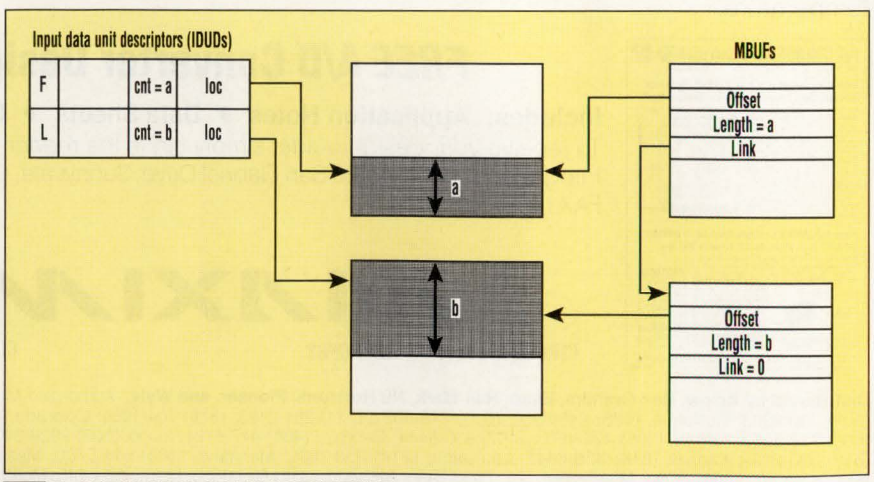
Protocol Processing

Protocol processing requires examining and creating headers for received data packets so they may be forwarded to another network. The headers may have various lengths, but are restricted to a maximum of 60 bytes. The routing process necessitates the creation of a new header, which may not be the same size as the old header.

Therefore, a new header could be created separately from the information portion of the frame. The packet includes a checksum that contains the protocol header, so it would have to be modified.

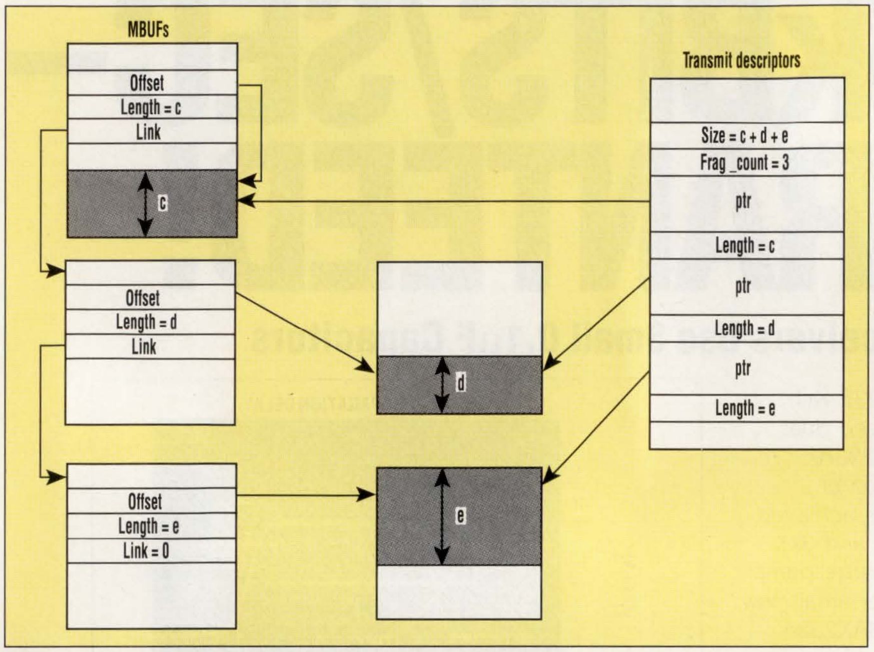
It can be concluded that the processor will need to access the entire header of an incoming frame, and write a header for the outgoing frame. Because the processor contains a rather large data cache, the data will only be fetched once from the network buffer memory, with subsequent accesses made from the cache.

Writing the new header will require more than one access to each



5. MEMORY MANAGEMENT in the Freeway router uses Unix MBUF structures. After a frame is delivered to the memory from the FDDI networks, the CPU links the frame segments together with MBUFs. Doing so eliminates the need to copy the data, and thereby greatly increases the router's forwarding capability.

ROUTERS TAME COMPLEX INTERNETS



6. THE DATA FIELD of the MBUF structure can hold the frame header to more efficiently process frames. Data is easily passed from protocol processing software to the Sonic Ethernet controller by a method based on transferring pointers and length indicators. Because data needn't be copied with this approach, the maximum forwarding rate can be maintained.

word of the header, as fields are created and updated in some header portions. Assuming that each word will be written twice, header handling will require 64 bytes of read and 128 bytes of write.

The read cycles will be performed in bursts of four words. Because a burst read of four words is performed in 12 clocks, all of the reads will require 2 μs per frame. The processor's write cycles aren't performed in bursts.

Each write cycle requires five cycles, or 6.4 μs per frame. For the stated target goal of forwarding 12,000 frames/s, the processor will require 13% of the network buffer-memory bandwidth.

To determine the hard limits of the Freeway router's network buffer memory, several worst-case assumptions are used. Even under those pessimistic conditions, the buffer memory's bandwidth only reaches 80% utilization, allowing protocol processing to continue uninterrupted.

On a hardware level, that level of performance is made possible by the 32-bit architectures of every component, their ability to operate with short bus cycle times, and features in the networking chip sets that eliminate the need to copy data between frame reception and transmission. But a great deal of work is also required on the software level to keep the processing requirements from overwhelming the capabilities of the hardware.

OPTIMIZING THE CODE

To appreciate the efficiencies built into the software, it's helpful to view the packet-handling process in three separate parts: input, protocol processing, and output. In the input part, a packet is received on an interface (Ethernet or FDDI), and a sequence of MBUFs is allocated to describe the incoming packet. Generally only two types of packets are recognized—those that conform to IP or the address resolution protocol (ARP).

The ARP packets are attended to immediately, as part of the interrupt processing. The IP packets are queued into the IP queue, and a special software interrupt is scheduled to begin the IP processing.

During protocol processing, a packet is extracted from the IP queue, some validity checks are done (checksum, header length, etc.), and the packet is forwarded to the next hop. The next destination is selected by looking up the routing tables to find the route to the destination network. The forwarded packet's time-to-live field and the checksum in the IP header are updated, and the packet is passed to the output routine for the outgoing interface (the route information includes the interface to be used).

In the output part, the destination IP address is resolved into the physical address, a new physical layer header is created by the output driver, and the packet is passed to the appropriate device (Ethernet or FDDI controllers).

To meet the goal of routing up to 12,000 packets/s, the average time that can be spent on processing a packet (input, protocol, and output) is about 70 μs. In terms of NS32GX320 CPU performance, that amounts to about 600 instructions. The network software included with BSD Unix code required nearly 2700 instructions to carry out the packet forwarding task. To give the Freeway router its present performance, that code had to be cut by some 80%. The reduction was accomplished by accumulating savings in bits and pieces, as follows:

- Checksum: The checksum routine is called twice during packet processing, once on input to check the incoming packet checksum, and once on output to create the new checksum. The generic checksum routine, supplied with the BSD code, was replaced by a routine tuned for the NS32000 architecture. That saved 400 instructions.
- Extra copies: The original BSD implementation required that the IP header be placed in the MBUF's internal buffer, implying a need for extra data copies. That requirement was eliminated by changing the packet handling.
- Intrinsic functions: Packet pro-

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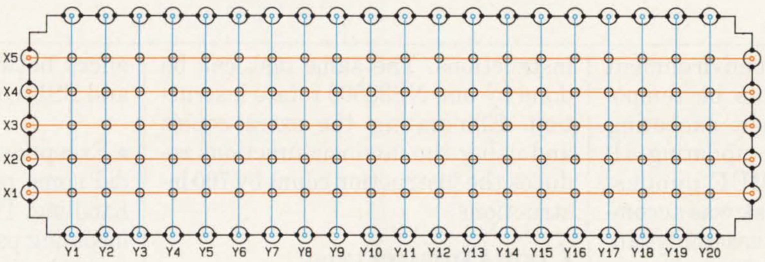

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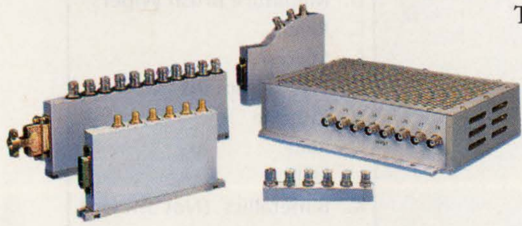

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cessing in the interrupt environment requires that interrupts be temporarily turned off when executing critical code sections (updating IP queues, updating MBUF queues, etc.). Originally that task was accomplished by calling an assembly-language routine. However, using intrinsic functions supported by the GNX compiler (an NS32000 software package), this is done as part of C code, and the subroutine call overhead is eliminated.

Intrinsic functions also eliminate processing overhead when transforming data from big endian (network) to little endian (NS32000 architecture) representation. Using an assembly-language routine, the six steps needed to transform the 16-bit packet length field (push parameter, branch to the subroutine, transform, put result in a register, return, assign the result) took eight machine instructions. The same task can be done by one NS32000 rotate instruction. Eliminating the extra copies and using the intrinsic functions reduces the instruction count by 700 instructions.

CODE OPTIMIZATION

The original BSD code was developed for workstations and computers. In that environment, it's reasonable to assume that most packets arriving at the workstation are indeed directed to the workstation. However, that assumption is clearly not correct for routers, where only a very small percentage of packets are directed to the router. The rest of the packets need to be forwarded. Thus, some checks, which are usually performed by the end (destination) station, can be eliminated or delayed except when the router is the packet's destination.

Consider the following differences between the router software and BSD code:

• Exception handling: The BSD code did some preparations for exception handling. That included copying of an incoming packet header, in case an internet control management protocol (ICMP) message needed to be issued. Router software assumes that things usually work and that the exceptions are rare. The copies for creating ICMP messages are therefore done only for exceptions, reducing the overhead. The improved packet checking policy and exception handling eliminated 300 instructions.

• Route allocation: In order to route a packet, the network and host numbers must be extracted from the destination IP address. The extraction process takes several comparisons (IP address class, subnetting, and so on). In the router software, the process is executed only once for each IP

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address compared with several repeated calculations in the original BSD code.

• Routing tables: The BSD software maintains two routine tables, one for hosts and another for networks. In BSD, the route search is performed first on the host table and then on the network table. The router deals mainly with networks, thus it first checks the network table, and then the host table. The changes in the route allocation and routing-table searches reduces the instruction count by 300 instructions.

• Standard header checksum: The assumption that the majority of packets have the standard IP header (no options) leads to creating a very fast checksum routine for standard IP headers.

• "Our" address recognition: The process of recognizing whether a packet is directed to the router or needs to be forwarded is time consuming, because the router has to compare the incoming packet's destination IP address against all of the IP addresses of every router interface (four Ethernet and one FDDI in the case of the Freeway router). That process can be accelerated by comparing only the upper bytes of the IP addresses in the incoming packet and of the interface IP address. If this comparison fails, which is what usually occurs, then other comparisons can be eliminated.

• Delayed space release: The space occupied by an already transmitted packet is released during the idle loop, instead of during interrupt processing.

• Fast physical address handling: Physical address comparisons and copies can be handled quickly by using long-word and short-word operations instead of subroutine calls, as is the case with BSD code.

Taken all together, the preceding optimizations reduced the instruction count to the design goal of 600 instructions per packet. But they don't exhaust the optimizing possibilities.

For example, further improvement can be achieved by exploiting the profile feedback feature of the NS32000 compiler. With that feature, the source code is first compiled with a special switch, which makes the compiler collect run-time profiling information on the software (to generate that information, it's necessary to supply the compiler with a set of typical inputs). The system is then recompiled, using the run-time profile information as an input to the optimizing compiler. Given both static information (from the source code) and the run-time profile of the software, the compiler can produce improved code.

Another potential area for improvement is in IP route caching. Currently, BSD code caches the last route used for routing a packet. If the same route is used for the next forwarded packet, the route allocation phase is saved. For the router, this approach can be improved by caching routes for each interface. That can save an additional 60 to 70 instructions.□

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Karen Parker, strategic program manager, holds a BS in physics from the University of Massachusetts at Amherst and has studied computer architecture at Stanford University, Calif., and the University of Massachusetts graduate school.

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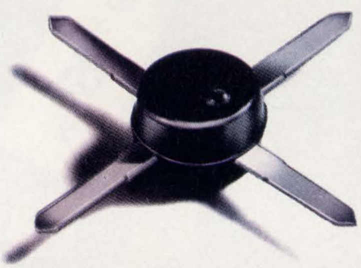

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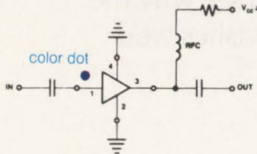

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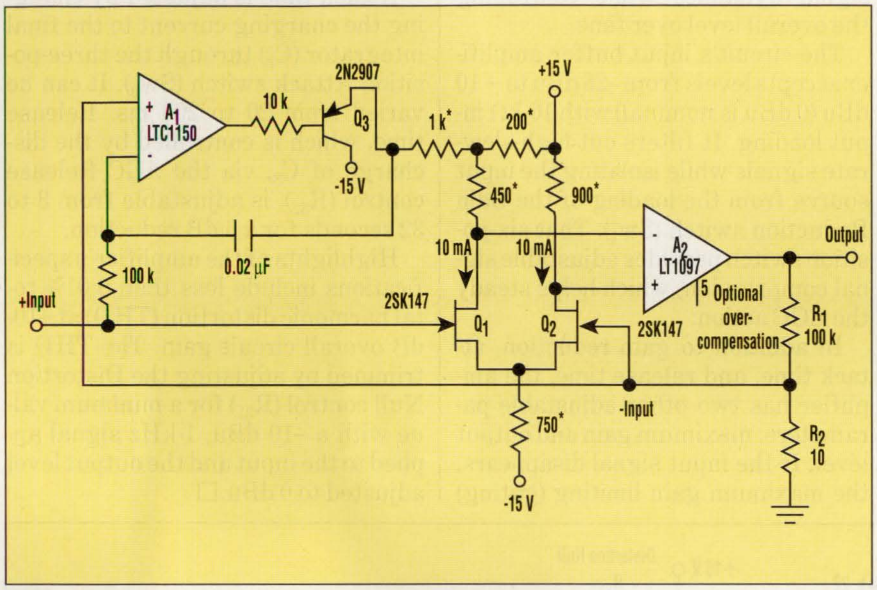


1. LOW-NOISE FETs Q_1 and Q_2 minimize the noise level of this chopper-stabilized amplifier. For best performance, the Toshiba 2SK147 FETs must be V_{gs} matched to within 10% and thermally mated. The resistors marked with an asterisk are 1% thin-film devices.

Usually, amplifier users must decide between the lesser of two evils: the low drift of a chopper-stabilized unit or the low noise of an unstabilized device. No more. By combining a pair of low-noise FETs with a chopper-stabilized amplifier, this circuit has just 0.05 µV/°C of drift and less than 50 nV of noise in the band from 0.1 to 10 Hz *(Fig. 1)*. Moreover, its offset is less than 5 µV, and its bias current is less than 100 pA. Putting that performance in perspective, the noise is almost 35 times less than that of monolithic chopper-stabilized amplifiers. As shown, the amplifier is configured to provide a noninverting gain of 10,000; other gains and inverting operation are possible.

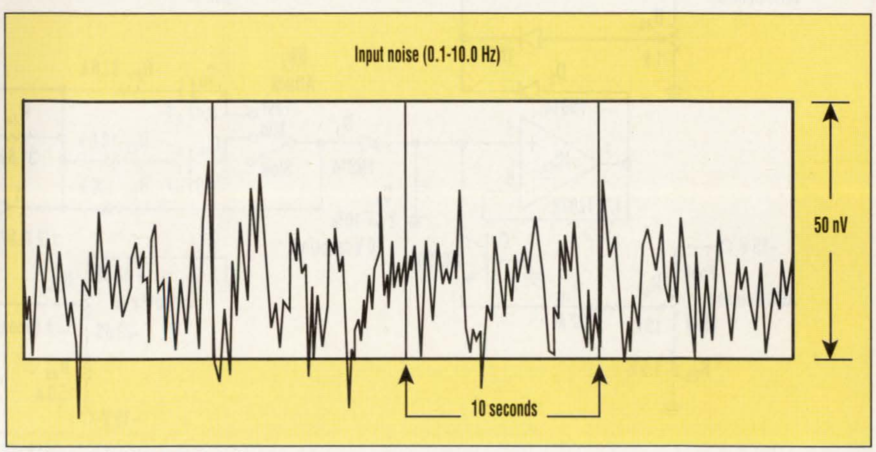
Key to the amplifier's performance are low-noise FETs Q_1 and Q_2, which differentially feed amplifier A_2 to form a simple low-noise op amp. Feedback, via R_1 and R_2, sets the closed-loop gain (to 10,000 in this case) in the usual fashion.

Although Q_1 and Q_2 have very low noise, their offset and drift are uncontrolled. Those deficiencies are corrected by amplifier A_1, a chopper-stabilized device. A_1 does that by measuring the difference between the inputs to Q_1 and Q_2 and adjusting Q_1's channel via Q_3 to minimize that difference. Because there's no way to predict the offset's sign, the FET drain resistor values are purposely skewed enough to force the offset in the right direction—that is, to make its sign so that A_1 can capture it.

In building the amplifier, care must be taken to select the FETs so that their gate-source voltages (V_{gs}), which can vary over a 4:1 range, match within 10%. That will allow A_1 to capture the offset without introducing any significant noise.

Because Q_1 and Q_2 run with 10-mA channel currents, they will experience a significant temperature rise. To obtain the specified noise performance, it's necessary that they be thermally mated and shrouded. Otherwise, small air currents could create temperature differences sufficient to increase noise by an order of magnitude. The thermal shrouding should completely enclose both devices and extend all the way down to the circuit board. Properly built, the amplifier will exhibit input noise characteristics as good as those of the best bipolar amplifiers *(Fig. 2)*.

The transient response of the amplifier is clean, with no overshoots or uncontrolled components. If A_2 is replaced with a faster device, such as an LT1055, the speed can be increased by an order of magnitude with similar damping. A_2's optional overcompensation capability (capacitor to ground) can be used to optimize response for low closed-loop gains.□



2. AS QUIET AS the best bipolar amplifiers, this FET-input circuit generates less than 50 nV of peak-to-peak noise over the band from 0.1 Hz to 10.0 Hz.

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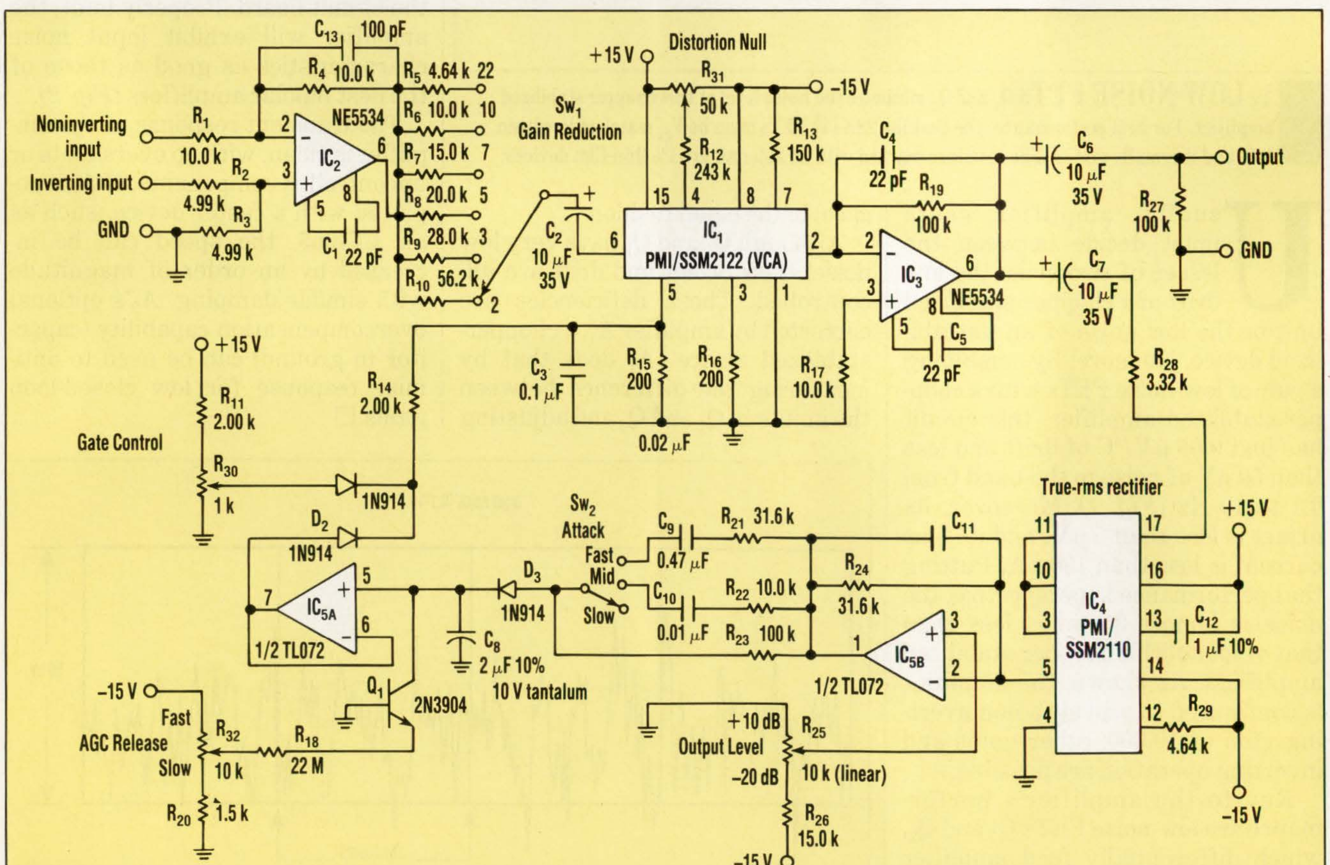
The heart of the circuit is a voltage-controlled amplifier, or VCA (IC_1), regulated by a feedback-type true-rms level detector (IC_4). That combination results in dependable and precise gain-control action, which faithfully retains the input-signal dynamics while controlling the overall level over time.

The circuit's input buffer amplifier accepts levels from –26 dBu to +10 dBu (0 dBu is nominal) with 10-kΩ input loading. It filters out high-slew-rate signals while isolating the input source from the loading of the Gain Reduction switch (Sw_1). That six-position switch provides adjustable signal compression, which helps steady the AGC action.

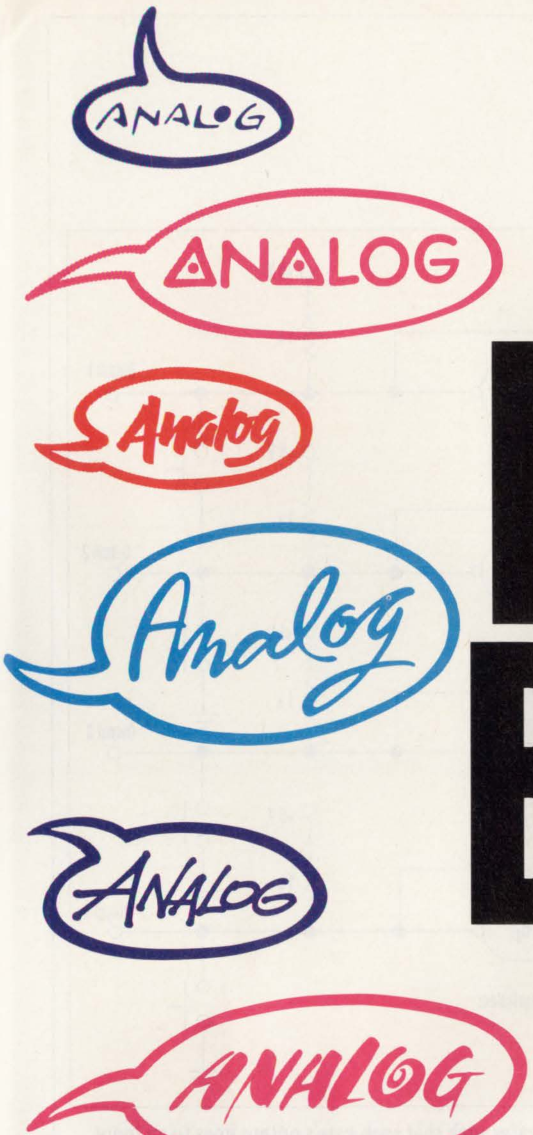
In addition to gain reduction, attack time, and release time, the amplifier has two other adjustable parameters: maximum gain and output level. If the input signal disappears, the maximum gain limiting (gating) circuit limits the input noise floor rise while the AGC circuit hunts for an input signal to regulate. It's adjustable via the Gate Control pot (R_{30}). The output level is set by comparing the voltage on the integrating capacitor, (C_{11}) to a reference set by the Output Level control pot (R_{25}).

Attack time is adjusted by changing the charging current to the final integrator (C_8) through the three-position Attack switch (Sw_2). It can be varied from 20 to 200 ms. Release time, which is controlled by the discharge of C_8, via the AGC Release control (R_{32}), is adjustable from 3 to 32 seconds for a 6-dB reduction.

Highlights of the amplifier's specifications include less than 0.01% total harmonic distortion (THD) at –10-dB overall circuit gain. The THD is trimmed by adjusting the Distortion Null control (R_{31}) for a minimum value with a –10 dBu, 1-kHz signal applied to the input and the output level adjusted to 0 dBu.□



ATTACK AND RELEASE times for this AGC audio amplifier can be adjusted by the three-position Attack switch (Sw_2) and the AGC Release pot (R_{32}), respectively. The output is rated for a 10-kΩ load. To work into 2 kΩ, C_8 must be replaced by a 100-µF, 15-V device.



DON'T BUY IT.

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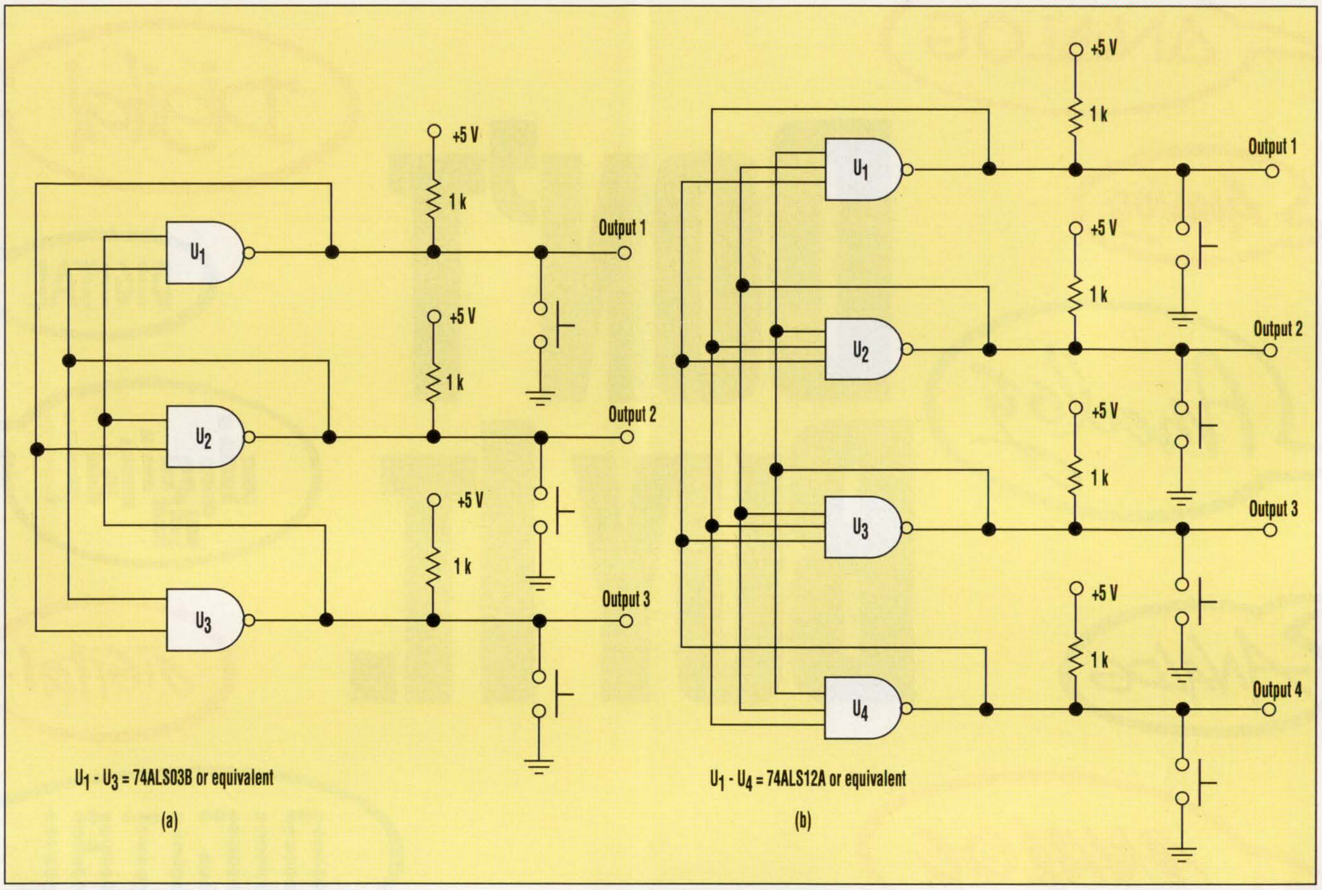


A TRISTABLE MEMORY element is formed by connecting three two-input NAND gates such that each gate's output goes to an input on the other two (a). A quadristable memory element uses four three-input NAND gates (b).

CIRCLE 523

MAKE POLYSTABLE MEMORY ELEMENTS

JOHN DUNN
181 Marion Ave., Merrick, NY 11566; (516) 378-2149.

Bistable memory elements of two stable states can be topologically extended to form memory elements of three or more stable states. The polystable elements are topologically extended in that they have multiple outputs—one for every stable state. For n stable states there exists a quantity of n NAND gates, each having n-1 inputs. The gates are cross-connected by feeding each gate's output to an input on each of the remaining gates. The stable states are defined as one of the n outputs being uniquely at logic 0. All of the others are at logic 1. Needing only n gates to achieve n states (one gate per stable state) can create an economically advantageous situation.

Three two-input NAND gates form a tristable memory element *(see the figure, a)*. Similarly, four three-input NAND gates yield a quadristable memory element *(see the figure, b)*.

Using open-collector gates with passive resistor pull-ups, the desired state can be triggered by a momentary outside closure to ground across the one output, which should be put at logic 0. The element will memorize that state and retain it. Although the outside closures are shown as push buttons, other gates or npn transistors could also be used.□

IFD WINNERS

IFD Winner for October 24, 1991

Henno Normet, Diversified Electronics Inc., P.O. Box 490207, Leesburg, FL 34749-0207; (904) 787-7259. His idea: *"Voltage Divider Needs No Trimming."*

IFD Winner for November 7, 1991

M.J. Salvati, Flushing Communications, 150-46 35th Ave., Flushing, NY 11354; (718) 358-0932. His idea: *"Nanoammeter Is Rugged."*

ELECTRONIC DESIGN

QUICK LOOK

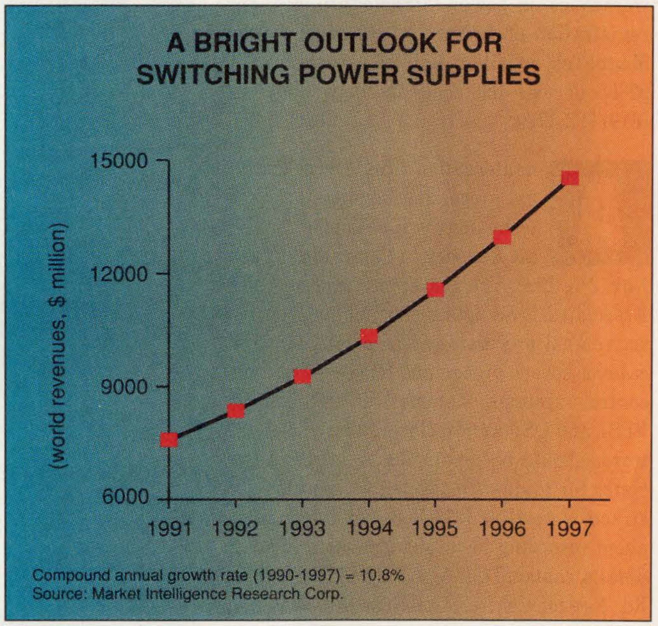
EDITED BY SHERRIE VAN TYLE

MARKET FACTS

Switching power supplies should continue to sell briskly, with revenues nearly doubling from $8 billion last year to nearly $15 billion by 1997, according to a study by Market Intelligence Research Corp. Compound annual revenue growth in that period should amount to 10.8%. The Mountain View, Calif., researcher notes that revenue growth comes even while the market is facing lower prices and increasing global competition. Because there are more than 1000 manufacturers of switching power supplies worldwide, few companies have significant market share.

The medium-power segment—100 to 500 W—is experiencing strong demand and is expected to account for 38% of world market revenues by 1997. Look for developments in modular power supplies, power factor correction, use of hybrid circuits, and surface-mount technology. These technologies will help sustain growth in the nineties.

In terms of world markets, competition is likely to grow even stronger because of the formation of the European Community and trade agreements between the Canada, Mexico, and the U. S. Competition from Pacific Rim countries, including Japan, also will likely remain heated.



OFFERS YOU CAN'T REFUSE

Departing from usual demo disk practice, shareware versions of PADS pc-board layout and PADs-logic schematic tools enable users to save designs. The shareware programs can design boards with up to about 30 ICs, come with a 100-page user manual, and are compatible with the commercial versions of the software. For a $50 registration fee, users receive support from PADS Software Inc., formerly CAD Software. The pc-board shareware includes manual placement and routing, autorouting, auto placement, design rule checking and outputs of photo-plotters. The PADS logic evaluation package supplies the functions of PADS logic, including its multisheet database, on-line rules checking, and context sensitive command handle. Contact PADS Software Inc., 119 Russell St., Littleton, MA 01460, (508) 486-9521. CIRCLE 451

Many engineers don't start to look for a job until they are unemployed. That's a mistake—instead, stay active in the job market while you're still employed. That's the advice of Tony Nayagan, manager of a database that matches resumes from engineers with job orders from companies that have openings. Most jobs fall into the $30,000 to $60,000 salary range in the EMPPLEXII database; the service's number is (412) 824-4343. For more information, contact the United States Information Network Corp., Suite 900, 400 Penn Center Blvd., Pittsburgh, PA 15235; (412) 824-3400; fax (412) 824-8112. CIRCLE 452

QUICK REVIEWS

The second edition of *Spice: A Guide to Circuit Simulation and Analysis Using PSpice*, by Paul W. Tuinenga, is an excellent book for engineers who have never used Spice and for those who have used Spice and want to learn more about it. After a short introduction that explains the origins of Spice and Spice derivatives, Tuinenga builds a simple circuit and walks readers through some dc measurements. The book progresses to ac analysis, feedback and noise analysis, transient response, and device modeling.

Throughout the text, Tuinenga's relaxed writing style provides a friendly alternative to the terse documentation found with most circuit simulation software. Dozens of circuit diagrams, Spice file listings, and screen shots support the author's tutorial approach. In addition, the book comes bundled with program disks for the student version of PSpice, MicroSim Corp.'s version of Spice for the PC. Engineers can use the PSpice disks to follow along with the text for hands-on instruction. The author gives readers exercises to try out features of the program and to demonstrate the use of PSpice for electrical engineering applications.

The book has a thorough table of contents and index that make any subject easy to locate. Four appendices provide an abridged summary of the control statements and device descriptions, a guide to using certain features of PSpice, and a complete Spice analysis of an amplifier circuit. (Prentice-Hall Inc., Englewood Cliffs, N. J., 1992, 254 pp. ISBN 0-13-747270-6. List price is $24.)—*Lisa Maliniak*

QUICK NEWS: CONFERENCES

How to achieve optimal design and engineering for power environments will be the topic for a technical seminar, "Trouble Proofing Your Power Environment," to be held in Washington DC on March 24 and Waltham, Mass. on March 26. Both day-long seminars will feature presentations, open sessions and workshops on power technology issues. For registration or further information, contact MagneTek at 901 E. Ball Rd., Anaheim, CA 92805 or call the seminars department at (619) 792-4730. CIRCLE 453

An international conference on signal-processing applications and technology will be held at the Hyatt Regency in Cambridge, Mass. Nov. 2–5, 1992. The conference sponsor, DSP Associates, is accepting paper submissions in such signal-processing areas as telecommunications, speech processing, image processing, control systems, automotive engineering, VLSI, and DSP architecture. Abstracts of 400 words should be sent or faxed to DSP Associates for review. Deadline for receiving abstracts is April 30, 1992. For more information about reserving booth space, costs, and other details, contact DSP Associates, 18 Peregrine Rd., Newton Centre, MA 02159; (617) 964-3817; fax (617) 969-6689. CIRCLE 454

Design of printed-circuit boards is the focus of a conference to be held March 30–April 1, 1992 at the Fairmont Hotel in San Jose, Calif. At least 60 hours of workshops, lectures, and tutorials are scheduled. Course topics include placement and routing, fine-pitch technology, packaging, design and test, quality and reliability, logic simulation, analog and RF techniques, and data formats. To supplement technical sessions, CAD/CAE vendors will exhibit their products in an adjacent hall. For more information, contact Dan Janzen at Miller Freeman Inc., 600 Harrison St., San Francisco, CA 94017; (415) 905-2354; fax (415) 905-2220. CIRCLE 455

The Pocket Intelligence Research Forum is intended as a central clearinghouse focusing on miniaturized computer and communication technologies. Subscribers to the forum, sponsored by SRI International, will meet twice a year to discuss developments in technology, market trends, and research. For more information contact SRI, 333 Ravenswood Ave., Menlo Park, CA 94025; (415) 859-5815; fax (415) 326-5512. CIRCLE 456

KMET'S KORNER

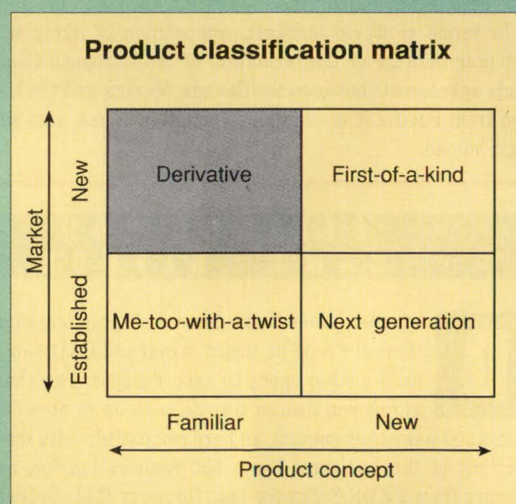
...Perspectives on Time-to-Market

BY RON KMETOVICZ
President, Time to Market Associates Inc.
Cupertino, Calif.; (408) 446-4458; fax (408) 253-6085

In the new product development domain addressed by this column, time to market is very short; development costs are small; there is no major incentive to be the low-cost producer; you have few competitors; and profit potential is high. Is this possible? Certainly! Following a derivative new product development strategy can give you all this and more.

Derivative product developers work with product concepts that are familiar. Doing so keeps development risk and cost to a minimum. It becomes much easier to balance development time, development cost, product performance, and product cost trade-offs when working with a relatively stable product concept that has some history of success and whose limitations are known. Design methods and tools will be familiar. Manufacturing technology and processes will be of the proven variety.

While they have safety on the development side of the equation, derivative developers assume significant market risk. They work into a market that is marginally defined, inadequately measured, and whose statistical properties are unknown. In short, they proceed largely on the intuition of key players that a market will materialize in support of the concept. This kind of thinking is difficult for many people to accept, yet alone support with money from their wallets. Successful derivative efforts must contain key individuals who produce the right alternative at the right time with limited information—the organization works on calculated leaps of faith! Small companies with intuitive risk-tolerant leadership do well in the derivative arena. Most big companies just talk about doing it.



As an example of where the derivative strategy is paying off today, look at the market for portable fax/modems and the number of suppliers that produce them. Somebody called the shots on this market right. A good one costs about $300, about three times more than a fax/modem card, and is about the size of a pack of cigarettes. It weighs next to nothing and runs for about 8 hours on its own internal battery. The technology to produce the product is readily available. Clever design was a must, but high-risk system and component development wasn't required.

The products' packaging and performance are impressive. Yes, they serve their intended purpose, but more important, someone saw the need and they now exist in abundant supply. While a hundred players slug it out to produce notebook PCs, only a handful of companies produce these little wonders of communication technology. Ironically, some of the big players in the conventional modem market missed the opportunity and are trying to get back into this new game, with new rules and new players. I estimate that the initial investment to create and enter this market was less than $2 million the pioneer company. I also conservatively estimate that some suppliers are retailing at least 100,000 units annually while generating at least $5 million in operating profit for their companies each year. The market, which is big, exists now. And a few bright, intuitive, opportunistic companies are running with it! Your company should do some derivative new product development. If not, figure out how to make it happen. Remember the line in *The Field of Dreams*—"If you build it, they will come!"

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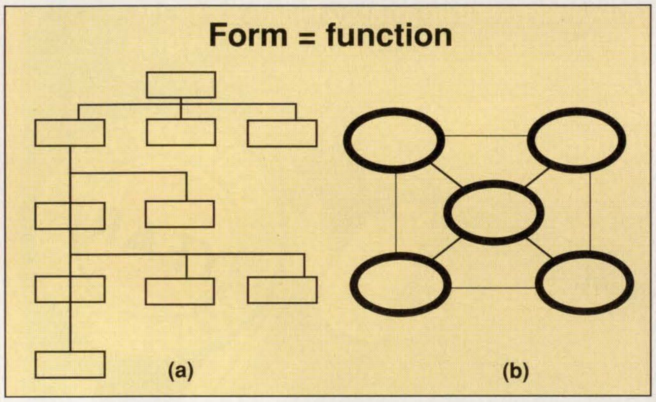
TALES FROM THE SKUNK WORKS

In my columns the words *trust* and *experience* appear often. Why do I stress these qualities in a skunk works? Because a skunk works requires more rigorous dimensions of trust and experience than we are accustomed to.

Note that a traditional, hierarchical, industrial-age organization avoids trusting and risking political mistakes. This top-down organization features control, process, proof, justification, and review *(see the figure, a)*. Decisions occur at the top; action takes place at the bottom. Information is quantitative and specific.

In contrast, the organization for a skunk works or a closed-loop team seeks opportunity and its focus is external *(see the figure, b)*. It distributes decisions and actions. Information is often tacit and intuitive. In this fluid structure proof is elusive and trust is all you have.

Using the wrong organizational paradigm makes success unlikely. Think of what it would be like to play tennis with a golf club or drive screws with a hammer.



IBM was the best of the best, with decades of cumulative experience in "left side" protocols. If the industrial age companies were dinosaurs, they would be Tyrannosaurus Rex. The difference is that they have good brains instead of long claws.

Now, IBM realizes that its way of working is outmoded and must change. Moving to "right side" teams renders much of its experience invalid. Don Estridge succeeded at IBM's PC skunk works because he was given sufficient autonomy to move quickly—but just barely. Estridge once said that he had to attend some 60 corporate meetings the first year of the PC project.

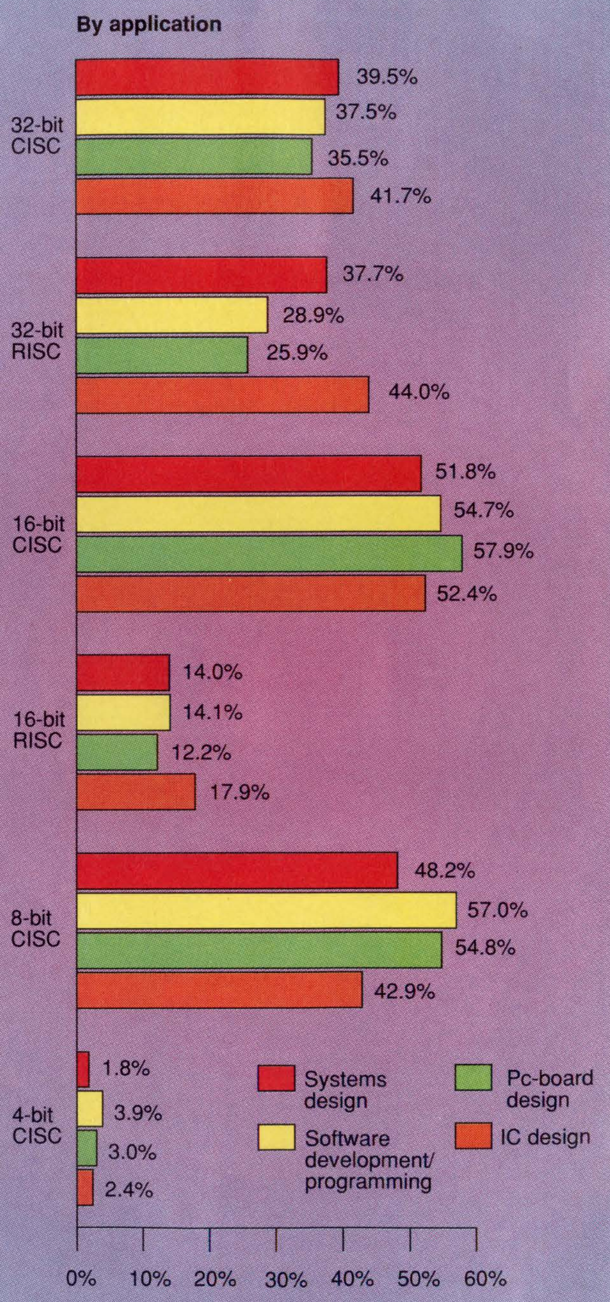
It is more exciting to create new markets than to batter competitors back one painful point of market share at a time. In that respect skunk works are like the passing game in football. But it is the ground game—continuous, grueling, and painstaking improvement—that produces the money you need to fund your skunk works. That is the mission for fast cycle, closed-loop teams, which are organized like a skunk works but are dedicated to fast-cycle, continuous improvement of existing products.

Few U. S. companies have depth of experience in either skunk works or closed-loop teams. This type of learning is mostly experiential, so make it a priority to retain experienced talent to train your employees by working with them.

John D. Trudel lectures and provides business development consulting: The Trudel Group, 52001 Columbia River Hwy., Scappoose, OR 97056; (503) 690-3300; fax (503) 543-6361. To order High Tech with Low Risk: *(503) 962-3755.*

CAD/CAE SURVEY

WHAT MICROPROCESSORS, IF ANY, ARE USED IN SYSTEMS YOU DESIGN WITH EDA TOOLS?



CISC = complex instruction set computer

RISC = reduced instruction-set computer

Source: a survey of Electronic Design readers by The Adams Co., Palo Alto, Calif.; (415) 325-9822.

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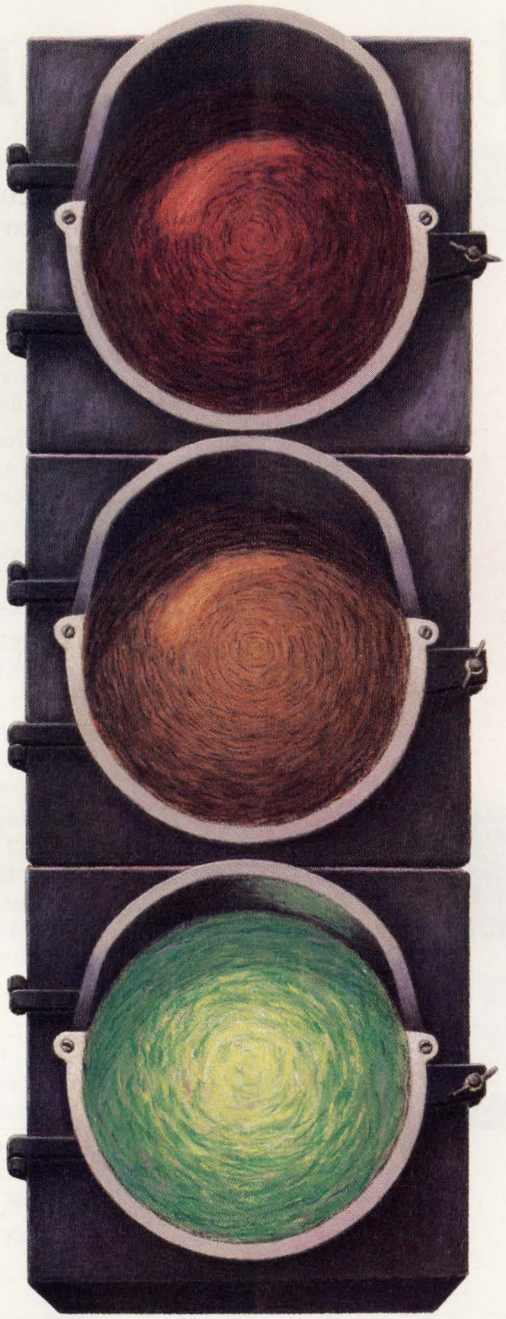

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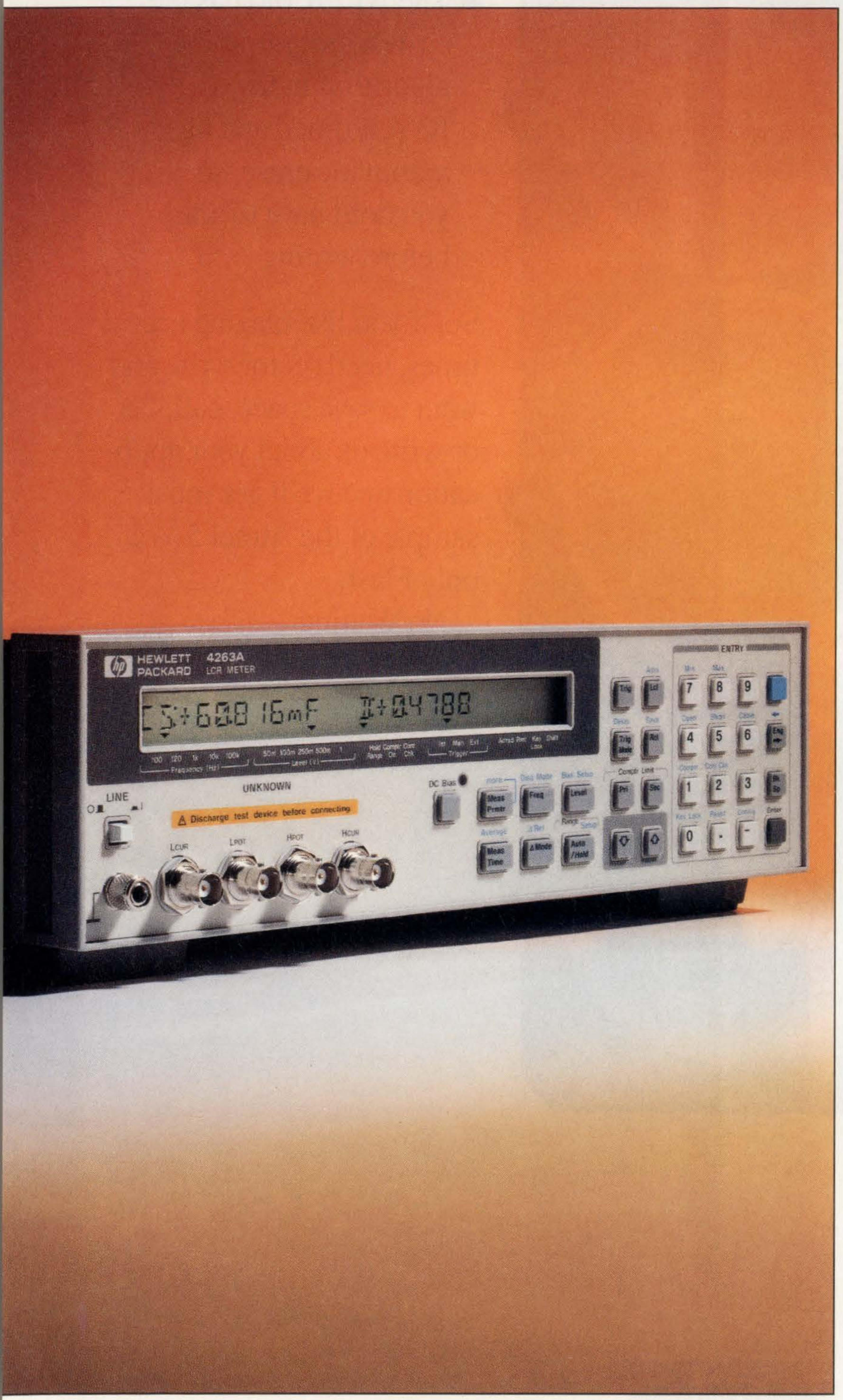

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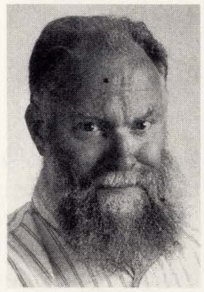


BOB'S MAILBOX

Robert:

...I especially enjoyed the article in the Sept. 26, 1991 issue regarding copper clad. One application which I would like to add to your excellent collection is that of RF stripline design.

Being an old RF Dawg working in the area of 300 to 1000 MHz, I used to buy single-sided copper-clad boards of various thickness to do stripline design. This was accomplished with a roll of 3M copper tape and an Xacto knife with plenty of spare blades for trimming the tape once it was on the board. When my careful calculations were done, I would lay out a board using the copper tape and experimentally determine the effects of inter-trace spacing and trace shape. Using this technique has saved my company lots of square feet of copper clad over the years, and lots of prototype pc-board layout.

LAWRENCE O. RICHARDSON, P.E.
Senior development engineer
Halliburton Logging Services
Houston, Texas

Sounds neat! And versatile for breadboarding.—RAP

●

Dear Bob:

That was a great article on copper-clad board. I use it to make microwave horn antennas. You just need a big soldering iron, a pair of shears, and a waveguide flange.

TOM WEBB
Texas Instruments
Dallas, Texas

Honk if you're a horn expert! I'm not much of an RF man myself.—RAP

●

Hi Bob:

...Having just finished your column on the many uses of pc boards, let me add another trick. Find the local store that deals in materials for STAINED GLASS. One method for joining glass panels is sticky-back copper tape, available in several widths and very solderable. Wrap that around the corners of a pc-board box, run a bead of solder along the seams, and I bet not much will get past that boundary.

There is a certain art to soldering copper foil using a big iron (>200 W). With practice, a pool of solder is formed and the iron is lifted slightly off the foil. Then, as the solder is drawn along the foil and solder is fed in simultaneously, a very beautiful bead forms that's as smooth as silk. Copper-sulfide crystals dissolved in water and rubbed over the solder will return it to its copper color. This might be useful for a "presentation" box. Oxalic acid is the standard stained glass copper flux.

PETER DOHERTY
Address unavailable.

Neat ideas. Pretty, too!—RAP

●

Dear Bob:

...On the top floor of a department store called Seibu Loft in Shibuys, Tokyo, they sell lots of "artsy" stuff at exorbitant prices to Japanese yuppies and yuppie-wanna-bes... I was in Japan recently on a business trip and lo and behold, they were selling lamps and clocks that used surplus pc boards (without any components on them) for the shades and faces. Even more amusing were the prices – some were as high as 50,000 yen for a lamp. Why didn't I think of that?...

...While I lived in Tokyo, I found myself in desperate need of a major project to keep from going totally bonkers, so I decided to try building some electrostatic speakers. The speakers not only sound good, but due to the voltages used (about 1200 V dc with peak ac voltages that approach 4000), they also make great bug zappers. Needless to say, good insulators are essential. That's where FR-4 circuit-board material comes in. The stuff works great! My most recent project uses FR-4 as the insulating frame, which keeps the diaphragm under tension and supports the perforated metal sheets...

...Unfortunately, I didn't realize how difficult it is to saw FR-4 until after I bought it. What a horrible job that was! I ended up cutting the stuff with a carbide hacksaw blade, which I modified to fit my electric scroll saw. You may want to warn your readers about the unhealthy effects of breathing the dust generated by sawing epoxy-fiberglass board.

MARK REHORST
Fremont, Calif.

Good info. I prefer using heavy tin snips to sawing (or see Duncan Moyer's letter below).—RAP

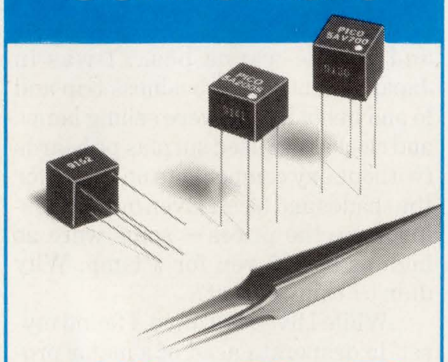
●

Hello Bob:

What's all this penny a square inch stuff, anyhow? Being a long-time practicing frugal engineer, I was very intrigued by your article on copper-clad innovations. I typically have to pay 10 times your mentioned price for the stuff when I can find it. So PLEASE

Pease Porridge—A Neal Certificate Winner

ELECTRONIC DESIGN is pleased to announce that Bob Pease's "Pease Porridge" has been honored by the Editorial Committee of the American Business Press with a Jesse H. Neal Certificate in the category of Best Regularly Featured Department or Column. ELECTRONIC DESIGN's Chief Copy Editor Roger Engelke shares the honors with Bob.



PEASE PORRIDGE

Pease, give me some tips or clues or contacts on your sources.

Thanks for the great column. It's always refreshing to observe a member of our profession in firm contact with the real world.

JOHN K. CARTER
Norman, Okla.

For approximately 36-in.-by-4-in. strips of good G-10 at 1¢ per square inch, call Halted Specialties Co., 3500 Ryder St., Santa Clara, CA 95051; (408) 732-1573, VISA/MC. For virgin 3-ft.-by-4-ft. sheets of FR-4 at 3¢ per square inch, call Advance Electronics, 1661 Industrial Way, Belmont, CA 94002; (415) 592-4550.—RAP

•

Dear Mr. Pease:

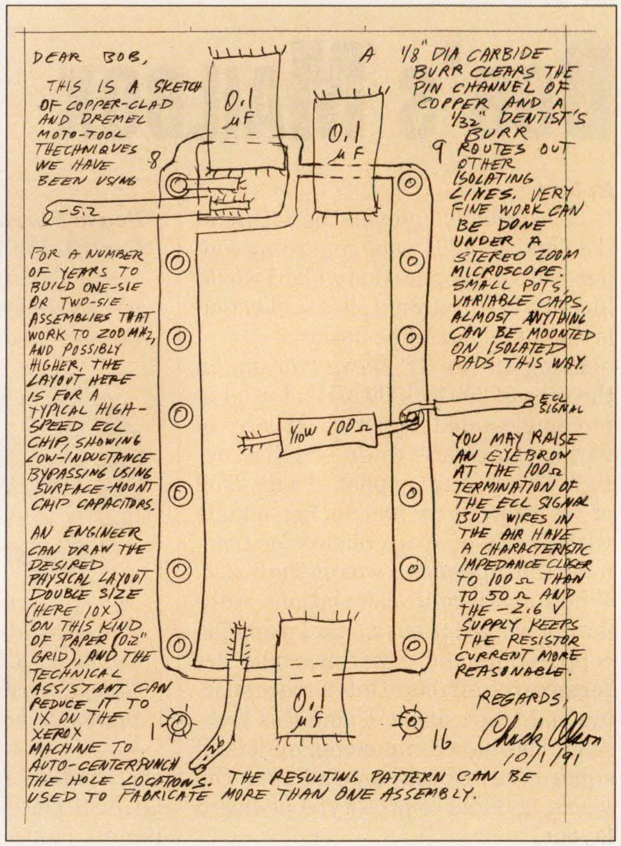
...We use a small paper cutter for cutting circuit board. There is a tendency for the board to be pulled into the blade so square cuts are difficult, but not impossible.

We also use the paper cutter to cut thin aluminum. Cutting both these materials does not destroy the edge on the cutter and we are still able to cut paper quite well.

We obtain, for free, scrap circuit board material from our local board fabricator. He has a good supply of material that is, for the most part, too small for his use. He does see a return, though, because he does our board manufacture.

Larger pieces of braid (outer braid on coaxial cable) make good hinges. Solder-wick also works well for hinges, although it's difficult to keep solder from wicking into the hinge.

DUNCAN MOYER
Technical services manager
Radio Systems Technology Inc.



Grass Valley, Calif.

Good techniques—thanks for sharing.—RAP

•

Dear Mr. Pease:

...Yes, copper-clad board is very useful to me as well. I thought I'd add one more use to the bag of tricks. When I need to epoxy two things together, I use a 2-in. square piece of copper-clad board as an epoxy palette. The epoxy I use has resin and hardener in separate tubes, so I squirt the stuff onto the board and mix it with a hunk of 14 AWG bus wire. Copper-clad palette is great because it's so plentiful (around here) and the surface is clean as opposed to paper products.

I suppose it would work just as well for artistic painting.

DONALD J. DELZER
Electronic design engineer
Tektronix Inc.
Beaverton, Ore.

That stuff sure has many uses!—RAP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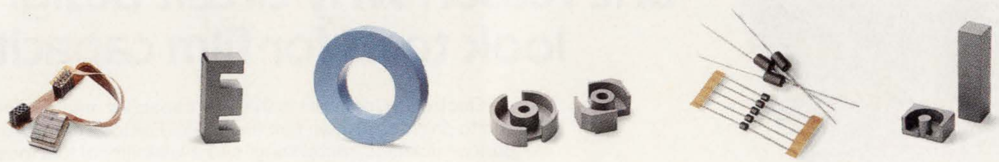

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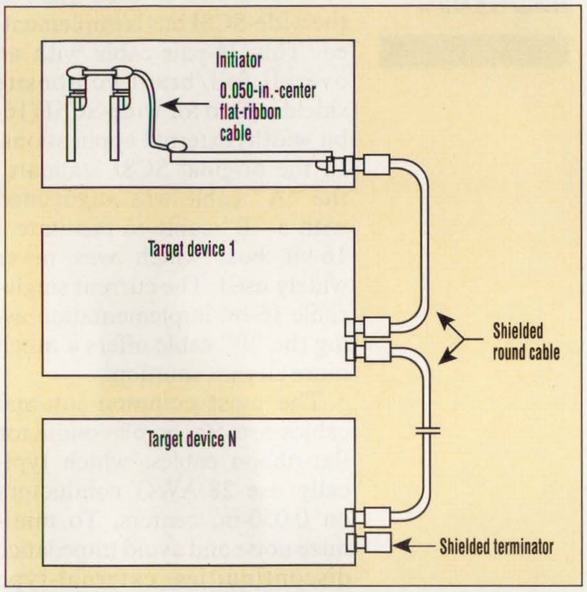
System Cabling For The SCSI Bus: Past, Present, And Future

As the SCSI specification expands, interconnect-cable performance must be re-examined.

BY PETER M. BLACKFORD
Cooper Industries, Belden Division, P. O. Box 1980, Richmond, IN 47375; (800) BELDEN-1.



1. The SCSI bus is controlled by a device known as the "initiator." This device, for example, might initially be a network-node terminal or other CPU. Peripheral devices on the bus are known as "targets." These roles may be reversed as control of the bus is negotiated and data is transferred.

In computer systems of many sizes, today's Small Computer System Interface is becoming the popular choice. While the name Small Computer System Interface, or SCSI, implies use in small systems only, this versatile bus finds applications even in the largest systems.

SCSI's origins date to 1979, when Shugart Associates, a major disk-drive manufacturer, began defining a new type of interface that would provide parallel-I/O capability and more flexibility than existing buses. The interface was called Shugart Associates System Interface, or SASI, and was one of the first to operate on a logical level.

In the SASI scheme, every device on the bus had a logical address instead of a physical address, and each peripheral device contained a degree of its own intelligence. The ability to place intelligence within each peripheral became possible with the advent of large-scale integrated circuits (LSIs). Using intelligence within a disk drive to determine which track, head, and cylinder to use freed the system's CPU and the bus for other I/O requests. Because the SASI bus was bidirectional and the peripherals had their own intelligence, many commands could be in process simultaneously. By exploiting this, the SASI bus could push I/O rates higher.

As the need arose to provide an industry-wide solution for systems with more than one peripheral, SASI was considered as an ANSI standard. The new standard was formally issued as SCSI in 1986.

The first systems to incorporate the interface made only limited use of its capabilities. But with the advent of higher-performance peripherals and processors, the limits of SCSI have been extended. Where system performance is concerned, the characteristics of SCSI interconnect cables themselves are now being further defined.

Today, SCSI permits the interconnection of a mix of communications devices, disk drives, tape drives, and optical-storage products that include WORM drives, rewritable types, and CD-ROM drives. A selection of SCSI devices may be found attached to many different nodes of a network, although communications between the nodes is handled by the network.

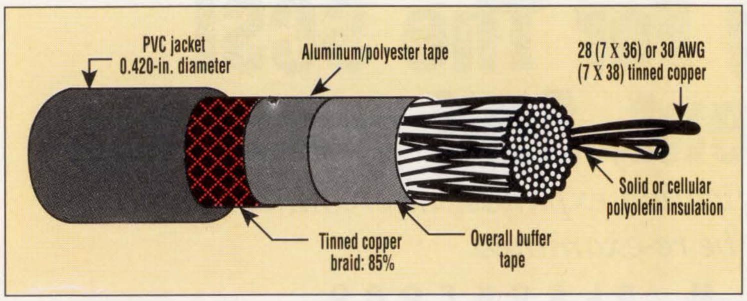
The device that controls the SCSI bus, such as the network-node terminal in the preceding example, is known as the "initiator." The peripheral devices that populate the bus are typically referred to as "targets." These roles may be reversed as control of the bus is negotiated and data is transferred *(Fig. 1)*.

Upon formalizing the standard, SCSI's limits remained largely untested. Since then, the desire for higher data-transfer rates, more features, and greater compatibility between a wider variety of devices has led to an expanded SCSI specification.

Clearly, today's computing environment is radically different from that of Shugart's a decade ago. That's why the development of a relatively inexpensive, flexible, device-independent, high-performance bus fits nicely with the current trend toward system-independent peripherals. The SCSI-2 specification emerged to take advantage of higher-performance peripherals and CPUs. It's compatible with all SCSI systems that support bus parity and meet Conformance Level 2 of the original SCSI standard.

SCSI-2 enhancements include:

- A variety of software enhancements.
- Unique termination techniques to speed error correction and boost effective data rates.
- Mandatory commands for many functions.



2. A common SCSI-2 cable design consists of 28 AWG conductors insulated with solid polyolefin to a maximum diameter of 0.035 in. Impedance variation of outer pairs is typically minimized by a buffer tape applied over the cable core. An aluminum/polyester laminate and an 85%-coverage braid shield handle shielding. The nominal finished cable diameter is 0.420 in.

• A maximum data-transfer rate of 10 Mbytes/s with "fast SCSI" (available only with differential termination).
• A data-path (bus) width of 16 or 32 bits with "wide SCSI" (the 32-bit bus, proposed but rarely implemented under SCSI-2, is being further developed under SCSI-3; the maximum data-transfer rate is 40 Mbytes/s when both wide and fast SCSI are used).
• Standard commands and support for optical devices.

At this point, it's helpful to start with a basic understanding of the significant properties of SCSI. A maximum cumulative bus (i.e. cable) length of six meters is possible when using single-ended (unbalanced) termination. Originally, the single-ended implementation was intended for single-cabinet, complete-system installations. Because it uses low-cost TTL drivers and requires less board space and less power than the differential implementation, the single-ended style is often used by SCSI designers.

When using differential termination, the maximum cumulative cable length is 25 meters. The differential configuration is meant for higher-noise environments, such as installations where peripherals aren't located close to the system.

Other important SCSI characteristics include the fact that single-ended and differential devices can't be mixed on the same bus. The data path is 8 bits wide and has a 4-Mbit maximum data-transfer rate. A typical bus topology has devices daisy-chained on the bus with a unique logical address for each device. The bus also features a device-independent, standardized command set.

Interconnect cables can limit system performance as data rates and the number of devices on the bus increase. Because the original cable specifications for the SCSI standard did not take enough factors into account, both SCSI and SCSI-2 require a new look at cable performance.

The basic cable requirements include cable types and configuration, electrical and electronic performance, and mechanical specifications *(Table 1)*. Cables inside and outside the cabinet are used with SCSI systems. Internal cables are typically flat-ribbon cables, while external cables should be shielded. Where they offer easier routing, size advantages, and better air flow, unshielded or shielded round cables are used inside.

Among SCSI cable types, the "A" cable is the most common configuration. This basic 8-bit external cable is a 25-pair (50-conductor) cable with an overall foil/braid composite shield. The "P" cable will be used more as the wide-SCSI bus is implemented. This 34-pair cable with an overall foil/braid composite shield is used for wide-SCSI (16-bit width) external applications. In the original SCSI standard, the "A" cable was augmented with a "B" cable to facilitate a 16-bit bus, which was never widely used. The current single-cable 16-bit implementation using the "P" cable offers a much more elegant solution.

The most common internal cables are 50- or 68-conductor flat-ribbon cables, which typically use 28-AWG conductors on 0.050-in. centers. To minimize noise and avoid impedance discontinuities, external-type cables may be used internally.

In high-density internal applications, 50- and 68-conductor

TABLE 1: SCSI-2 SPECIFIED CABLE REQUIREMENTS

Basic cable types	SCSI	SCSI-2	Wide SCSI-2	Fast SCSI-2	Proposed SCSI-3
Round, 50-conductor, shielded	X	X		X	X
Round, 68-conductor, shielded			X	X	X
Round, 50-conductor, unshielded	X	X		X	X
Round, 68-conductor, unshielded			X	X	X
Flat, 50-conductor, 0.050 in.	X	X		X	X
Flat, 50-conductor, 0.025 in.		X		X	X
Flat, 68-conductor, 0.050 in.			X	X	X
Flat, 68-conductor, 0.025 in.			X	X	X
Electrical					
Characteristic impedance (ohms) (single-ended)	100	90	90	90	77 Min. 95 Max.
Differential	NS	140	140	132	NS
Attenuation dB/m at 5 MHz (max.)	------	------	------	0.095	0.095
Worst-case change in pair-to-pair propagation delay (ns/m)**	------	0.2	0.2	0.2	0.15
Dc resistance (ohms/meter) (Fast SCSI-2 and SCSI-3 figures for terminal power only)	0.23	0.23	0.23	0.23	0.23
Mechanical (round cable only)*					
Maximum primary diameter	0.035	0.035	0.035	0.035	0.035
Maximum overall diameter	0.400	0.400	0.450	0.450	0.450

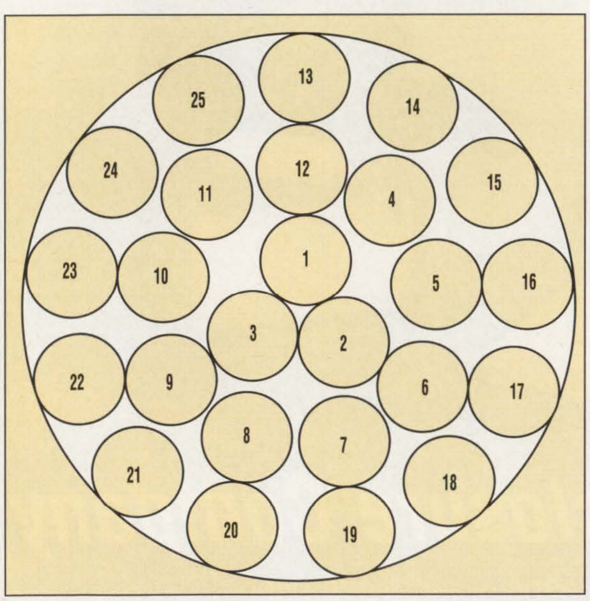
*Due to connector-backshell limitations
**Also referred to as SKEW
NS = not specified

30-AWG flat cables with 0.025-in. centers are being used. Also useful are 28-AWG cables with 1-mm centers.

Some applications that are internal to SCSI systems use specialty cables, such as Belden's Vari-Twist and MASS-TER cables. Vari-Twist cables are flat-ribbon cables consisting of long twisted-pair sections and short, flat, laminated sections that may be terminated the same way as conventional flat cable. Similarly, MASS-TER cable incorporates twisted-pair and flat sections, but is contained inside a round jacket. MASS-TER cables also come shielded.

Impedance and dc resistance are the only electrical requirements cited in SCSI and SCSI-2 specs. According to the standard, "recommended" cable impedance for single-ended systems must be 90 Ω or more. This impedance requirement is subject to question, however, because impedances lower than 90 Ω have been used successfully in SCSI and SCSI-2 for quite some time. Obviously, other cable-performance qualities must be considered. Cable impedance should be 90 to 140 Ω for differential systems.

For fast SCSI, two other requirements have been identified.



3. The correct cable layup for a SCSI-2 cable ensures that its performance is more than adequate when coupled with proper system-termination techniques.

TABLE 2: ELECTRICAL PERFORMANCE OF ROUND SHIELDED SCSI CABLE

Conductor gauge	Insulation type	Single-ended impedance	Differential impedance
28	Solid polyethylene (PE)	79 Ω	117 Ω
28	Foam PE	87 Ω	136 Ω
28/30	Polyvinyl chloride (PVC)/solid PE	87 Ω	136 Ω
28/30	PVC/foam PE	95 Ω	146 Ω

Cable attenuation must not exceed 0.095 dB/meter at a 5-Mbyte data rate, and pair-to-pair propagation delay (skew) must not exceed 0.02 ns/meter.

Single-ended interface problems caused by adding cabling to the system have recently surfaced. Many users now extend total system-cable lengths beyond the previously defined six-meter limit (for systems utilizing single-ended drivers), despite the fact that this configuration was originally meant for internal cabinet use only. What has resulted are more elegant SCSI-2 round-cable designs using advanced materials and manufacturing technologies.

Consideration has been given to such parameters as propagation delay, skew, and crosstalk. Appropriate techniques have been developed to evaluate cable parameters that most accurately represent system-application conditions. For example, single-ended impedance is measured between the signal conductors and the shield, with all grounds tied together. Typically, single-ended impedance is about 65% of the differential impedance value for a given cable.

For most applications, one of four basic SCSI-2 cable designs apply. A common design consists of 28-AWG conductors insulated with solid polyolefin to a maximum diameter of 0.035 in. Cable-pair lay length is chosen for the best crosstalk performance. Impedance variation of outer pairs, caused by their proximity to the shield, is typically minimized by a buffer tape applied over the cable core. An aluminum/polyester laminate and an 85%-coverage braid shield comprise the shielding system. The nominal finished cable diameter is 0.420 in. *(Fig. 2)*. With a single-ended impedance of about 77 Ω, this cable is below the specified 90-Ω minimum. But it works well with the proper system-termination techniques and pinout configuration *(Fig. 3)*.

With recent SCSI-2 committee findings indicating a higher cable impedance to be desirable, several techniques may be used to increase nominal cable impedance to about 90 Ω. For instance, a foam polyolefin extruded over standard 28-AWG conductors may be used to replace the solid polyolefin. Foam insulation offers a dielectric constant of 1.7 (versus 2.3 for solid insulation), lowering the cable's propagation delay from 1.54 ns/ft. to 1.3 ns/ft. Polyvinylchloride may be used to insulate the 28-AWG conductors used for the TERMPWR lead(s).

Foam-insulated cables do, however, carry some disadvantages that should not be ignored. Cable-assembly life is limited by the insulation-displacement system's less secure insulation retention, and attaching connectors to cables is more difficult.

Cable impedance may also be increased by using a hybrid design. In a single cable, the hybrid incorporates 28-AWG conductors used for TERMPWR lead(s), and 30-AWG conductors that are employed on all signal pairs. The 90-Ω impedance goal is achieved by insulating the smaller 30-AWG conductors with a solid polyolefin to a diameter of 0.035 in. Although connectorization of 30 AWG is more difficult than 28 AWG,

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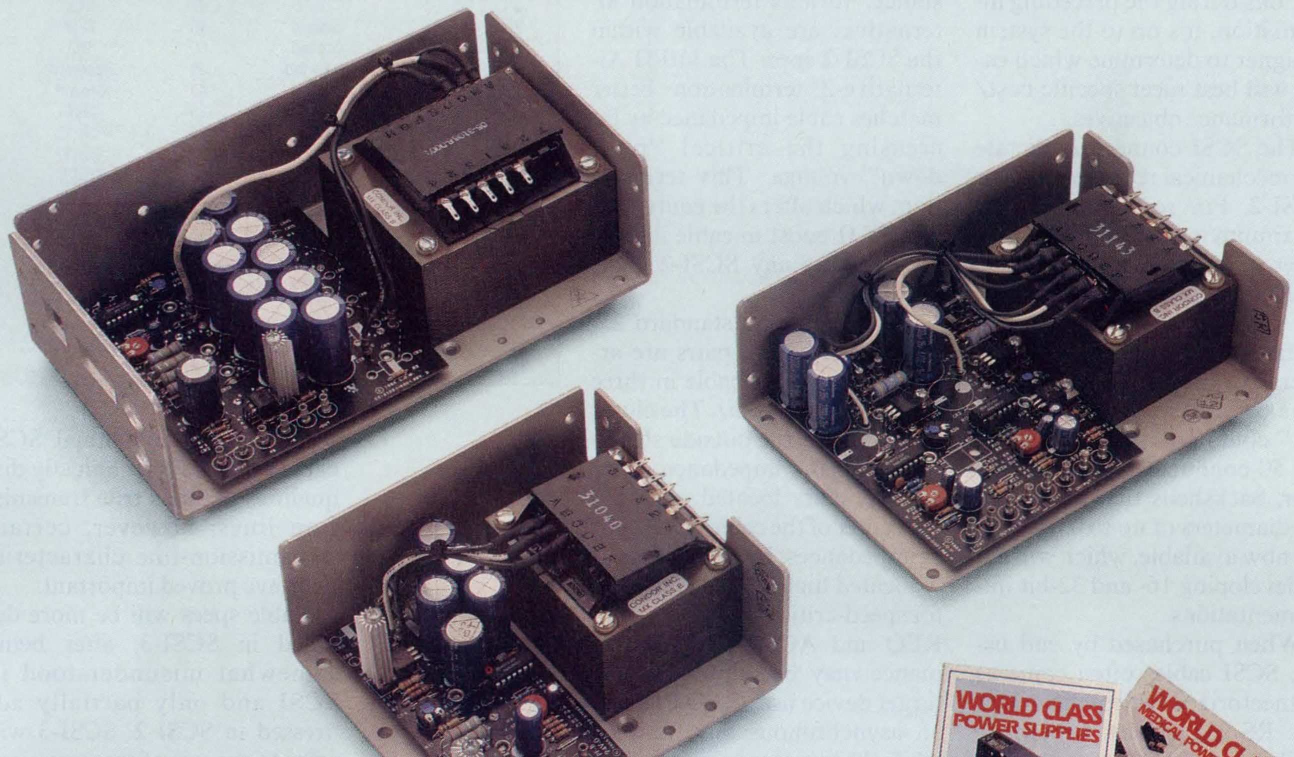

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the solid insulation is securely retained in the connector.

Yet another hybrid design yields even higher impedances by using both 28 and 30-AWG conductors and a cellular polyolefin insulation material. This hybrid's single-ended impedance is about 100 Ω *(Table 2)*.

Considering the preceding information, it's up to the system designer to determine which cable will best meet specific cost/performance objectives.

The SCSI connectors dictate the mechanical requirements for SCSI-2. For round cables, the maximum insulated primary diameter of each conductor is 0.035 in.; for flat cables, connector center-to-center distance dictates dimensions. In the past, overall round-cable diameter, or "maximum backshell diameter," could not exceed 0.400 in. for 50-conductor cables. However, backshells that accept cable diameters of up to 0.0450 in. are now available, which will aid in developing 16- and 32-bit implementations.

When purchased by end users, SCSI cables often come as connectorized assemblies. Unlike RS-232 cables, which are easily assembled by end users, the SCSI connectorization process is specialized. Assembly by most end users is impractical.

Typical cable assemblies are much shorter than the 6 meters allowed by the SCSI standard for single-ended systems, or the 25-meter maximum bus length permitted for differential systems. When used between peripherals outside the main-system cabinet, cable assemblies are typically 1 meter or less in length. Inside the cabinet, short jumper-cable assemblies connect one board to another.

There are two primary methods used in making SCSI and SCSI-2 cable assemblies. For mechanical assemblies, connectors are purchased with an assembled backshell from companies like AMP, Fujitsu, or Honda Connector. Often favored by designers for their cosmetic and mechanical benefits, molded cable assemblies feature an injection-molded backshell/strain relief and are often customized with logos and colors.

Several steps can improve any system's performance. For instance, various termination alternatives are available within the SCSI-2 spec. The 110-Ω Alternative-2 termination better matches cable impedance by increasing the critical "pull-down" voltage. This termination, which offers the equivalent of a 15-Ω boost in cable impedance, makes any SCSI-2 cable work better.

In the case of a standard 25-pair construction, pairs are arranged inside the cable in three layers *(Fig. 3, again)*. The closer the pair is to the outside shield, the lower the impedance. Conversely, pairs located closer to the center of the cable have higher impedances. By using centrally located high-impedance pairs for speed-critical signals, such as REQ and ACK, cable performance may be improved. The target device uses REQ to begin an asynchronous bus transfer, while the initiator acknowledges receipt or transfer of data in response to the REQ signal using ACK. By locating data pairs in the outermost layer of the cable, crosstalk between REQ, ACK, and data lines is minimized *(Table 3)*. Wise placement of key lines within the cable can lead to even higher performance levels. Proper signal location is considered vital for the best SCSI-2 performance.

To handle the soaring data-transfer rates and consistently high performance levels, the ANSI X3T9.2 committee is diligently working on a new version: SCSI-3. The committee is becoming more aware of the interconnect system and views SCSI cabling as a transmission line that's a key to overall SCSI-system performance. The shortness of many individual SCSI cable assemblies technically disqualifies them as true transmission lines; however, certain transmission-line characteristics have proved important.

TABLE 3: RECOMMENDED SINGLE-ENDED SIGNAL PIN ASSIGNMENTS

Pair#	Pin#	Signal name 1	Pin#	Signal name 2
1	24	Ground	48	REQ
2	19	Ground	44	ACK
3	16	Ground	45	ATN
4	17	Ground	42	Ground
5	18	Ground	43	BSY
6	20	Ground	48	RST
7	21	Ground	46	MSG
8	22	Ground	47	SEL
9	23	Ground	48	C/D
10	25	Ground	50	1/O
11	14	Reserved	39	Reserved
12	15	Ground	40	Ground
13	1	Ground	25	-DB(0)
14	2	Ground	27	-DB(1)
15	3	Ground	28	-DB(2)
16	4	Ground	29	-DB(3)
17	5	Ground	30	-DB(4)
18	6	Ground	31	-DB(5)
19	7	Ground	32	-DB(6)
20	8	Ground	33	-DB(7)
21	9	Ground	34	-DB(P)
22	10	Ground	35	Ground
23	11	Ground	36	Ground
24	12	Reserved	37	Reserved
25	13	Opened	38	TERMPWR

Cable specs will be more detailed in SCSI-3, after being somewhat misunderstood in SCSI and only partially addressed in SCSI-2. SCSI-3 will refer to the use of transmission-grade materials, the minimum acceptable impedance, and other parameters that qualify cables for SCSI uses. They're also likely to make a cable-pinout scheme mandatory. Taken together, these changes should aid in choosing the right SCSI cable.

Peter M. Blackford, product development manager at Cooper Industries/Belden Division, earned a BS from Worcester Polytechnic Institute, Worcester, Mass., in 1970.

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Level-3 Pc-Board Connectors Edge Toward High-Speed Applications

Decreasing semiconductor switching speeds need connectors as transmission lines.

BY MATT SUCHESKI

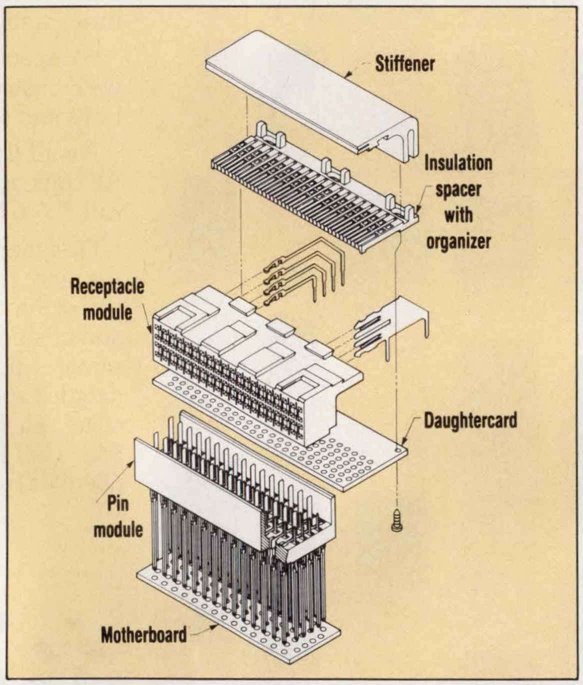
AMP Inc., P.O. Box 3608, Harrisburg, PA 17105-3608; (717) 780-6074.

With growing line counts and surging signal-switching speeds in electronic equipment, electrical connectors can no longer be taken for granted. Word width has grown from 8 to 64 bits, and edge rates have fallen from 8 to 0.5 ns. To meet these requirements, connectors have to support stripline technology and more elaborate bus architectures. Consequently, the interconnections at the backplane/daughtercard level (Level 3) must be analyzed as a transmission-line section.

From that perspective, a fundamental design goal is to homogenize a circuit path. This is accomplished by controlling impedance levels through all circuit sections to minimize reflections. Another goal is to maintain signal integrity, which requires isolating a signal path by proper referencing to ground.

However, today's signal-management practices, which need strategically located electrical lines to be assigned as reference lines, can consume up to half of the available lines when signal-edge speeds are below 3 ns. The reference increase I/O needs and use more signal lines at the backplane interface.

Of course, more lines at the edge of a daughtercard mean larger, more densely populated connectors. This represents a dichotomy of design goals. Larger connectors (pin-field arrays) imply a greater statistically significant variation in such parameters as normal force, durability, and mating force. Higher density dictates higher-performance material that must be manufactured to smaller nominal features using traditional processes, such as stamping, plating, and molding.



1. With 40 effective high-speed signal lines per inch and a pin count of up to 680 lines, this connector exemplifies the stripline approach used to satisfy high-speed interconnect requirements.

In general, the rudimentary design goals of an enhanced-performance backplane (Level 3) connector are:

- Controlled impedance and minimized crosstalk at signal-edge speeds below 1 ns.
- An interconnect card-edge density of 40 effective (isolated) lines per inch.
- Minimal changes imposed upon substrate manufacturers and board-assembly houses.
- Cost- and line-compatibility with the information-processing marketplace.
- Modular construction for design flexibility, just-in-time delivery, and repairability.

At speeds of 3 ns or more, backplane (Level 3) connectors were effectively transparent to the signal wave fronts. As speeds dropped from 3 to 1 ns, the connectors become increasingly exposed as transmission lines. With today's speeds in the subnanosecond range, the conductor's propagation delay becomes a significant fraction of the wave front. In effect, the connector is now a meaningful transmission-line element in the signal's path.

With the edge-rate signals over 3 ns, a low number of lines are required for signal returns. Signal-to-reference (S/R) ratios of 8:1 or higher are workable, and are bound more by common-mode noise than by any other factor. As edge rates move into the 3-to-1-ns range, the need to control crosstalk is apparent, particularly in cases with multiple sources. Here, the connectors use a moderate fraction of the available lines for references, and S/R ratios are 4:1 or less.

When signal-edge rates fall under 1 ns, typical applications need about half of the lines for returns, which means an S/R ratio of 1:1. With wider words, more paths requiring additional effective lines, and higher speeds where up to half of the lines are returns, the connector interface

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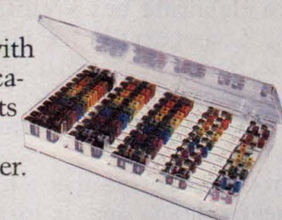

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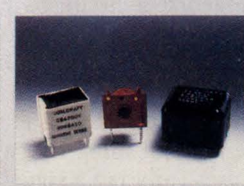

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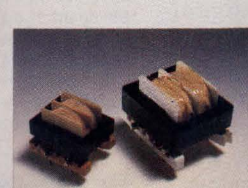

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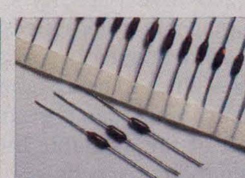

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faces daunting demand.

The effects are particularly acute at the Level-3 (daughtercard-to-motherboard) interconnect. The Eurocard (DIN) 96-position connector, with its characteristic three rows and 30 signal lines per inch (15 effective lines per inch), has been a long-time standard. A significant segment of the market has moved to four-row and even six-row configurations with their 20 to 30 effective lines per inch.

This continuing need for more effective pins (I/O's) dictates a new design approach that achieves several objectives. These include an effective impedance of 50 Ω at 0.5-ns rise time, crosstalk of less than 3%, and 40 effective signal lines per inch. Also realized are pin counts of up to 680 effective lines, improved contact reliability, and maximum power-distribution capability.

In a connector developed using the new approach, contacts are provided on 0.10-in. centerlines with ground shields located between each column of contacts *(Fig. 1)*. The connector profile is 0.74 in. wide and 1.35 in. high in the fully engaged position. An aluminum board stiffener holds the modules together on the daughtercard (receptacle) side. The pin header is press-fit into the motherboard.

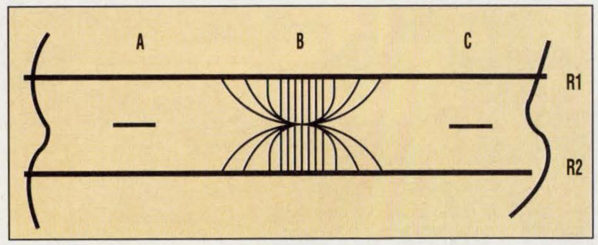
At this point, it's helpful to take a closer look at the stripline concept. Essentially, a driven line B is significantly coupled to two parallel reference planes, R1 and R2, and remotely coupled (isolated) to two adjacent driven lines identified as A and C *(Fig. 2)*.

The fundamental concept identifies columns of pins and receptacles as signal lines, introduces a plate-like element between signal columns, and dedicates its electrical function to a reference plane. The basic arrangement is repeated with 0.100-in. spacing between columns of signal contacts *(Fig. 3)*. This construction provides a stripline configuration for the signal lines and a minimum connection length between the proper substrate planes. The actual connector pattern shows that the holes dedicated for a shielding-power function are located in a staggered, or offset, position from the signal fields *(Fig. 4)*.

Today, connector design is an interactive process where electrical, mechanical, and environmental objectives are identified and optimized to achieve the required performance. Finite-element models analyze the mechanical and electrical properties of proposed design variations. In addition, computer models of the resulting transmission-line systems are constructed. Simulations then reveal the interaction of variables in the expected end-application environment.

There are four primary parameters in the analyses. For one, propagation delay is the time required for a signal to transit a system. The second is the characteristic impedance, which is the voltage-current ratio of the signal in the system. This is defined classically for lossless transmission lines by the inductance/capacitance ratio or $(L/C)^{1/2}$. The third parameter is crosstalk, which is unwanted energy coupled onto a victim signal line electrostatically and magnetically from an active line or lines. The fourth parameter is common-impedance noise, which is unwanted voltage transients created in the power and ground systems. Such noise is caused by current transients in conduction paths shared by multiple signals.

The connection is defined as the length of circuit between a perpendicularly intersecting plane segment (source) on the daughtercard, located at the edge of the stiffener (0.200 in. from the D row), and the top surface of the motherboard.

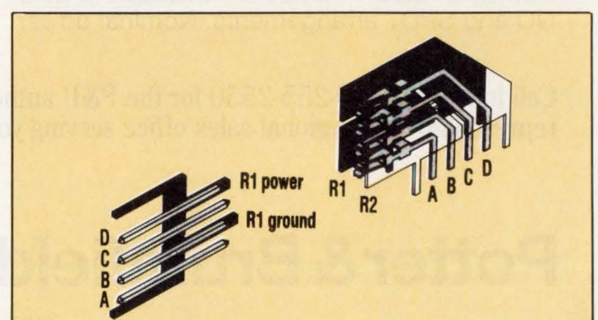


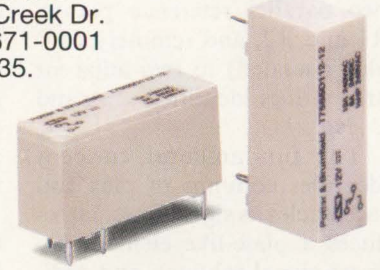
2. In the stripline concept typically used in high-density printed wiring boards and modified for use in connectors, a driven line (B) is significantly coupled to two parallel reference planes (R1 and R2), and remotely coupled or isolated to two adjacent driven lines (A and C).

3. When using the stripline approach, columns of pins and receptacles are signal lines and a plate-like element is placed between the columns to serve as the reference plane. Here, driven lines (B and D) are significantly coupled to two parallel reference planes (R1 and R2) and remotely coupled to two adjacent driven lines (A and C).

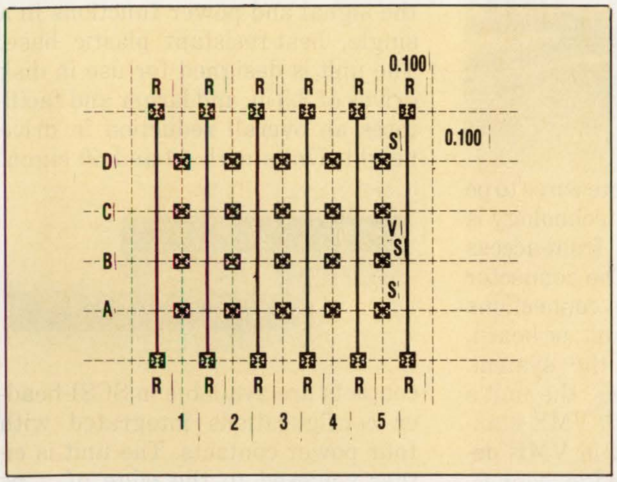
Propagation delay (T_{pd}) of the connection is a part of the total signal-path delay, which has a direct influence on the system's maximum operating speed. Differentials in T_{pd} cause undesirable timing skew in parallel transmissions. Moreover, a variation in propagation delay between rows of a connection (measurement nodes) is directly proportional to variations in impedance and crosstalk. To minimize this variation in the connector, the signal-path lengths are kept as short as possible. The paths' effective dielectric constant is held as low as is practical to keep the velocity of propagation as high as possible in rows C and D. Consequently, there's an average propagation through the defined connection of 185 (±9) ps. Another result is differential propagation times for the four different paths from a source on the daughtercard through the connector to the motherboard *(Fig. 5)*.

In conclusion, stripline connectors embody a concept that approaches homogeneity across the connection of two pc boards. Stripline characteristics of the board are maintained through the connector, which makes the connector virtually transparent



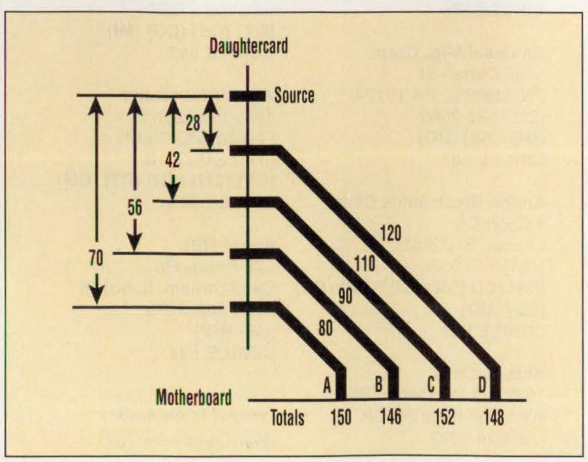


■ LEVEL-3 PC-BOARD CONNECTORS ■



4. The actual connector pattern of the stripline design in Figure 3 shows that holes dedicated for shielding and power functions are located in a staggered position from the signal fields.

5. In this stripline-connector configuration, signal paths are managed to minimize variations in propagation times (shown here in picoseconds). Velocity of propagation is kept as high as possible in rows C and D to balance delay with that of the shorter signal paths in rows A and B.



to the circuit.

The electrical commoning of alternate columns of contacts provides economical application in environments where shielding is of paramount importance. The end result is connectors that offer a cost-effective means of achieving stripline performance at sub-nanosecond edge speeds.

Matt Sucheski, engineering manager for the AMP Capital Goods Business Sector's New Business Development group, earned a BSME from Penn State University, University Park, Pa.

HOW VALUABLE?

HIGHLY	CIRCLE 531
MODERATELY	CIRCLE 532
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▼ PCB CONNECTORS HAVE LOW INSERTION FORCE

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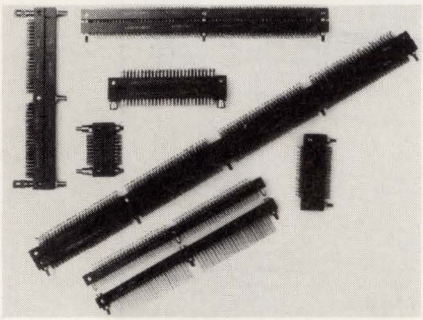
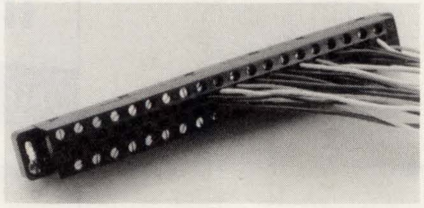


tions, have average insertion forces of 1 oz/contact. Connector heights are from 0.40 to 0.74 in. Sockets are incorporated on one side with tails that serve as mating pins on the other. Call for pricing and delivery.

Hypertronics Corp.
16 Brent Dr.
Hudson, MA 01749
(800) 225-9228
▶ **CIRCLE 751**

▼ CARD-EDGE CONNECTOR FEATURES FRONT ACCESS

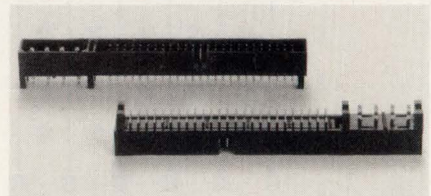


A transition from discrete wires to pc board using card-edge technology is made possible by the front-access card-edge connector. The connector lets the end user make connections without removing the unit, pc board, or front panel from the system. Available in 40 positions, the unit's dimensions comply with VME standards and can be used in VME designs requiring card-edge connections to discrete wires. The connector is on 0.150-in. centers. Call for pricing and delivery.

Augat/RDI
525 Randy Rd.
Carol Stream, IL 60188
(708) 682-4100
▶ **CIRCLE 752**

▼ CONNECTOR COMBINES SIGNAL, POWER FUNCTIONS

A dual-purpose connector combines the signal and power functions in a single, heat-resistant plastic base. The unit is designed for use in disk drives of 3.5 in. and larger and facilitates an overall reduction in drive height. Units with 40 and 50 signal



contacts are available in SCSI-header configurations integrated with four power contacts. The unit is either soldered to the edge of a pc board or fastened to the board by means of right-angle through holes. Call for pricing and delivery.

CW Industries
130 James Way
Southampton, PA 18966
(215) 355-7080
▶ **CIRCLE 753**

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6801 River Place Blvd.
Austin, TX 78726
(800) 326-1368
(ES) (MG) (ER) (TB)
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3M
Electronic Products Div.
Bldg. 130-3N-27
P.O. Box 2963
Austin, TX 78769
(800) 225-5373
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Interconnection Technologies
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Advanced Circuit Technology
118 Northeastern Blvd.
Nashua, NH 03062
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(FC) (ZI) (SM) (CD) (FX) (ES) (ER)
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Advanced Interconnections
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W. Warwick, RI 02893
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Buchanan Div.
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Livingston, NJ 07039
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(DI) (CE) (ID) (ZI) (CD)
CIRCLE 579

American Insulated Wire
36 Freeman St.
Pawtucket, RI 02862
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(TW) (SH) (PW) (HK)
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Scarborough, Ontario, M1B 2X6 Canada
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Interconnect Products
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Endicott, NY 13760
(607) 754-4444
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Bendix Connector Operations
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Sidney, NY 13838-1395
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West Los Angeles, CA 90024-5603
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Miami, FL 33166
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(see p. 114 for key)
(continued on p. 105)

The European Community (EC) Directive for electrical transient immunity is a reality. Sound engineering practices and careful design are no longer enough. Transient suppression will be required in the electronic products you sell to the EC to meet IEC 801–2, IEC 801–4, and IEC 801–5 standards. Don't let your competition pass you by.

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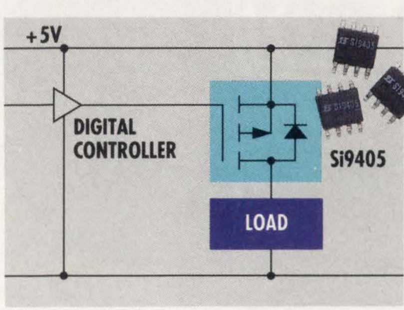

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These SOIC-8 devices can be driven directly by 5-V logic.

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Engineered Connecting Devices
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DuPont Electronics
DuPont Connector Systems
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(302) 992-5212
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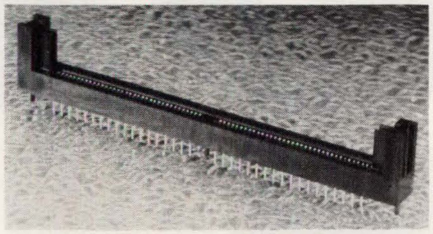
CIRCLE 624

(see p. 114 for key)
(continued on p. 110)

▼ SIMM CONNECTOR BOOSTS MODULE MEMORY

A 0.050-in.-center, dual-readout SIMM connector is designed to increase module memory with the benefit of reduced board real estate. The



connector uses a push-pull concept with contact wipe and high-temperature materials that withstand soldering. It's designed for standard card-edge board thickness, resulting in reduced board cost. Other features include dual inverse-bellows contacts. Call for pricing and delivery.

Methode Electronics Inc.
Connector Div.
7447 W. Wilson Ave.
Chicago, IL 60656
(708) 867-9600
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Printed-circuit boards can be connected to flat-panel displays or to other pc boards using the monosotropic heat-seal connectors from Elform Inc. The connectors can be made with up to 106 terminations per inch while maintaining optimum flex and/or fold characteristics. Connectors are screen-printed on 0.001-in. polyester film using thick-filk conductive inks, dielectric inks, and hot-melt adhesives. Call for pricing and delivery.

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A four-contact circular connector measures less than 1 in. long and 1/4 in. in diameter. The unit is available in a quick connect/disconnect version as well as in a screw-threaded

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POW

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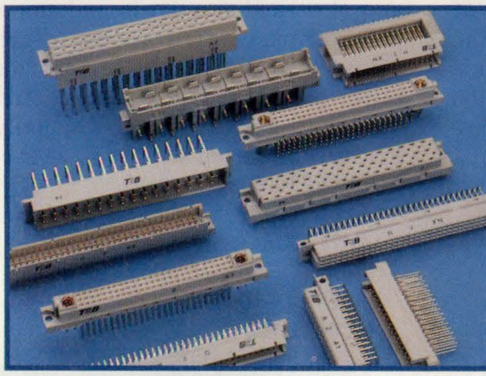
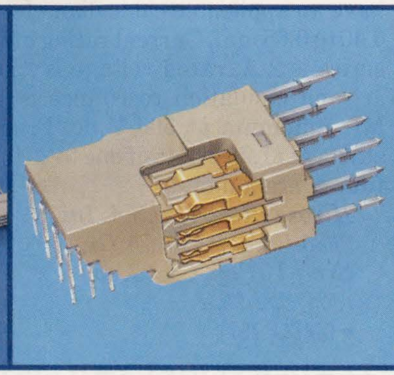
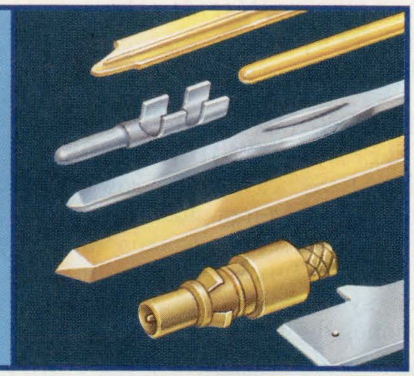
VER







A full range of DIN 41612 connector types – Standard and Inverse, Low Profile and Heavy Duty Power connectors and Modular Coax/Signal/Power combinations.

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A complete selection of termination styles – solder tails and posts, wire wrap, compliant pin, crimp/snap, and coax. Post lengths and plating options for every requirement.

With the high performance features designed as standard into every Thomas & Betts DIN connector, we can solve even your most difficult packaging problems.

Off-the-shelf availability through our authorized distributors means you get what you need when you need it.

Now there's a reliable source with the breadth and depth you need to harness the full power of DIN 41612 versatility. For more information call or fax: Thomas & Betts Corporation, Electronics Division, 200 Executive Center Drive, Greenville, SC 29616. Phone: 803-676-2900. Fax: 803-676-2991.

For the new DIN Catalog call 1-800-344-4744.

Thomas&Betts

•***EUROPE*** **- Belgium:** Brussels, 32-2-645-7711; **England:** Marlow, 44-6284-6055; **France:** Rungis Cedex, 33-1-4687- 2385; **Germany:** Egelsbach, 49-6103-4040; **Italy:** Milano, 39-2-6120451; **Luxembourg:** Foetz, 35-255-0002; **Spain:** Barcelona, 34-3-3002252; **Sweden:** Upplands Vasby, 46-760-88110.

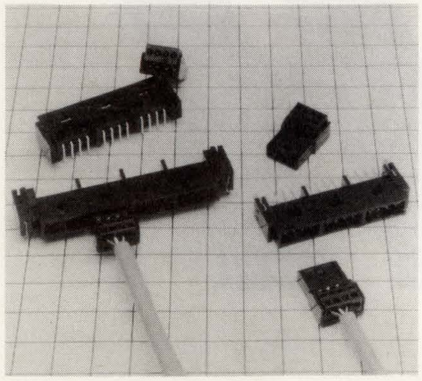
CONNECTORS

▼ MICRO SHUNTS MATE WITH SQUARE HEADERS

The SNM Series of micro shunts mate with 0.018-in. square headers on 0.050-by-0.100-in. centerlines. The terminals pass through the shunt so that they will accept any post with a minimum height of 0.120 in. The shunts are available with gold or tin plating on their phosphor-bronze contacts. Pricing begins at $0.088 depending on plating and quantity. Delivery for up to 1000 pieces is from stock.

Samtec Inc.
P.O. Box 1147
New Albany, IN 47151-1147
(800) SAMTEC9
▶ CIRCLE 756

▼ IDC CONNECTOR MEETS TELEPHONE-SWITCH NEEDS

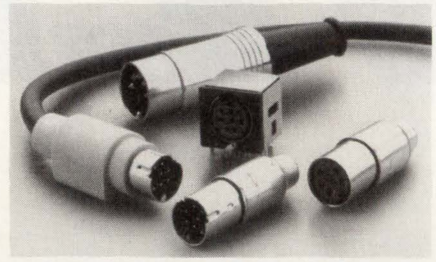


The MQ115 Series of single-row connectors with 2.54-mm pitch meet the need for connectors in main units and branch boxes of telephone switch systems. Useful in digital telephone, digital PBX, and other telephone equipment, the connectors are available with IDC crimping and have an applicable cable diameter of 0.40 to 0.65 mm. Current rating of the series is 2 A, rated voltage is 250 V ac, and insulation resistance is 100 MΩ minimum at 500 V dc. Pricing starts at $1.25 in lots of one to 25 for a four-contact unit.

Hirose Electric U.S.A. Inc.
2685-C Park Center Dr.
Simi Valley, CA 93065
(805) 522-7958
▶ CIRCLE 757

▼ MINI-DIN CONNECTORS COME IN FOUR FLAVORS

Moldable male and female plugs, assembly-type male cord plugs, and pcb-mount receptacles are all included in a line of mini-DIN connectors. Each is made to exacting mechanical



and electrical standards and comes in 3- to 8-pin configurations. All will accept #22 to #28 AWG wire sizes. Silver-plated brass contacts are standard with gold available optionally. Prices range from $0.51 to $0.74 each in lots of 1000.

Preh Electronic Industries Inc.
470 E. Main St.
Lake Zurich, IL 60047-2578
(708) 438-4000
▶ CIRCLE 758

CONNECTOR AND PACKAGING MANUFACTURERS

E-Mark Inc.
4 Daniels Farm Rd., Suite 328
Trumbull, CT 06611
(203) 452-1003
(SM) (DP) (BI)
CIRCLE 625

ECS Composites
3560 Rogue River Hwy.
Grants Pass, OR 97526
(503) 476-8871
(GP) (IN) (VR) (WT) (PT) (EM) (MI) (CM) (ES) (ER) (GK)
CIRCLE 626

ERNI Components
520 Southlake Blvd.
Richmond, VA 23236
(804) 794-6367
(CX) (DS) (DI) (FC) (CE) (ID) (ZI) (SM) (CD) (MD) (BP) (VB) (IB) (BU) (GB) (FL) (CA) (GP)
CIRCLE 627

Eby Co.
4300 North "H" St.
Philadelphia, PA 19124
(215) 537-4700
(CE) (DP) (CD) (MD) (HV) (WR) (FX) (BP) (VB) (SB) (MB) (IB) (BU) (GB)
CIRCLE 628

Elco Corp.
Connector Div.
Huntingdon Industrial Park
Huntingdon, PA 16652
(814) 643-0700
(AU) (DS) (DI) (CE) (ID) (SM) (CC) (DP) (PG) (CD) (MD) (HV)
CIRCLE 765

Elcon Products Int'l Co.
P.O. Box 1885
Fremont, CA 94538
(415) 490-4200
(ZI) (CD) (MD) (BI) (RP) (HC)
CIRCLE 629

Eldre Corp.
1500 Jefferson Rd.
Rochester, NY 14623
(716) 427-7280
(BB)
CIRCLE 630

Electrical Connectors
Trimex Bldg., Rt. 11
Mooers, NY 12958
(518) 298-4810
(SM)
CIRCLE 631

Electrical Insulation Supplier
Electronics Div.
300 N. Mannheim Rd.
Hillside, IL 60162
(708) 547-5400
(CO) (FL) (TW) (SH) (WV) (PW) (MN) (HK) (HN) (CA) (ES) (MG) (ER) (GK) (FR) (SE) (TB) (RC) (VE) (WN)
CIRCLE 632

Electronic Solutions
6790 Flanders Dr.
San Diego, CA 92121
(619) 452-9350
(ML) (WR) (BP) (VB) (SB) (MB) (BU) (GP) (BM) (VR) (PT) (EM) (MI) (CM)
CIRCLE 633

Elform Inc.
P.O. Box 7362
Reno, NV 89510
(702) 829-1905
(EL)
CIRCLE 634

Elma Electronics Inc.
44350 Grimmer Blvd.
Fremont, CA 94538
(510) 656-3400
(DI) (CE) (VB) (IB) (BU) (HN) (GP) (BM) (CN) (IN) (VR) (PT) (EM) (MI) (CM) (ER)
CIRCLE 635

Emcor Products/Crenlo, Inc.
1600 N.W. Fourth Ave.
Rochester, MN 55901
(507) 287-3418
(GP) (CN) (VR) (WT) (EM) (MI) (CM) (ER)
CIRCLE 636

Emulation Technology
2344 Walsh Ave., Bldg. F
Santa Clara, CA 95051
(408) 982-0660
(ID) (ZI) (SM) (CC) (DP) (PG) (CD) (MD) (BI) (WR) (FL)
CIRCLE 637

Enclosure Technologies Inc.
256 Airport Industrial Dr.
Ypsilanti, MI 48198
(313) 481-2200
(IB) (GB) (HN) (GP) (CN) (IN) (VR) (EM) (CM) (ES) (ER)
CIRCLE 638

Equipto Electronics Corp.
351 Woodlawn Ave.
Aurora, IL 60506-9988
(708) 897-4691
(GP) (CN) (IN) (VR) (EM) (MI) (CM) (ES) (MG) (ER)
CIRCLE 639

Everest Electronic Equipment
Standard Products Div.
2100 E. Orangewood Ave.
Anaheim, CA 92806
(714) 634-2866
(GP) (VR) (EM) (MI) (CM)
CIRCLE 640

Fischer Connectors Inc.
28245 Crocker, Suite 210
Valencia, CA 91355
(800) 344-0445
(AU) (RF) (CX) (CD) (MD)
CIRCLE 641

Fujitsu Microelectronics Inc.
Electronic Component Div.
3545 N. First St.
San Jose, CA 95134-1804
(800) 642-7616
(DS) (FC) (CE) (ID) (ZI) (SM) (CD) (FL) (SH)
CIRCLE 642

GEM Inc.
109 State Place
Escondido, CA 92025
(619) 747-9177
(ML) (BP) (VB) (GP) (BM) (CN) (PT) (EM) (MI) (CM)
CIRCLE 643

Garry Electronics
Division of LPL
9 Queen Anne Ct.
Langhorne, PA 19047
(215) 949-2300
(ZI) (SM) (CC) (DP) (PG) (CD)
CIRCLE 644

Gemini Inc.
103 Mensing Way
Cannon Falls, MN 55009
(507) 263-3957
(GP) (IN) (VR) (PT) (EM) (MI) (CM)
CIRCLE 645

General Devices Co. Inc.
1410 S. Post Rd.
Indianapolis, IN 46239
(317) 897-7000
(GP) (VR) (EM) (MI) (CM)
CIRCLE 646

Graphic Research Inc.
9334 Mason Ave.
Chatsworth, CA 91311
(818) 886-7340
(SS) (DD) (ML) (FX) (BP) (PC)
CIRCLE 647

Haewa Corp.
4357-B Park Dr.
Norcross, GA 30093
(404) 921-3272
(GP) (BM) (CN) (IN) (VR) (PT) (CM)
CIRCLE 648

Harting Elektronik
2155 Stonington Ave.
Hoffman Estates, IL 60195
(708) 519-7700
(RF) (CX) (DS) (DI) (FC) (CE) (ID) (ZI) (DP) (HV)
CIRCLE 767

(see p. 114 for key)
(continued on p. 112)

COMING ATTRACTIONS:

April 16

Analog Technology: D/A Converters

This Special report takes an in-depth look at high-resolution (14-bit and higher) converters. One of the report's main goals is to separate the digital-audio DACs from all other high-res DACs, and to examine the use of digital-audio DACs in more traditional applications.

PC Design Special Section

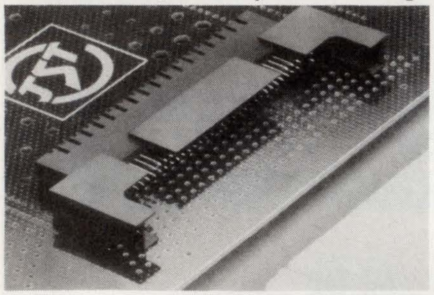
Electronic Design's PC Design Series was created specifically to serve the needs of our many readers developing PCs and peripherals. Everything from chip sets and single-chip solutions to CISC and RISC microprocessors, high-density memories, graphics, peripherals, add-on/add-in boards, buses, interfaces, input devices, and software are thoughtfully discussed from the systems designers' point of view.

In Every Issue...

Our Ideas For Design along with our Technology Newsletter, New Products, and Quick Look sections bring Electronic Design readers the latest in test and measurement, computer-aided engineering, and components.

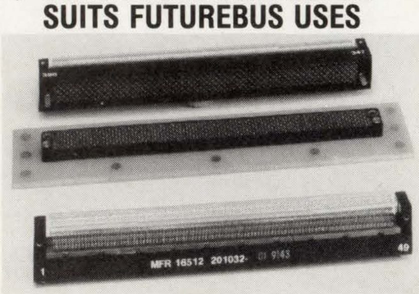
▼ MEMORY-CARD CONNECTOR OFFERS RUGGED BUILD

Rugged two-piece construction is featured in the Series ICM-C memory-card connectors. The devices are designed for 0.050-in. pitch, 68-circuit (two-row) memory cards. Receptacles which become the card interconnect, and headers which are installed in equipment to mate with the cards are included. Contacts have independent twin-beam construction for a minimum of 5000 mating cycles. Pricing is about $0.05 per mated position. Delivery is in eight to 10 weeks.



J.S.T. Corp.
1200 Business Center Dr.
Suite 400
Mt. Prospect, IL 60056
(800) 292-4243
▶ CIRCLE 759

▼ BLADE-FORK CONNECTOR SUITS FUTUREBUS USES



A blade-fork connector system that is in the SEM-E naval avionics format is useful in Futurebus+ systems. The unit is a 396-pin connector on a 0.100-by-0.050-in. grid. Available products include the developmental open-entry, low-profile backpanel interface as well as a closed-entry type. Also offered are molded and stamped-contact headers and metal headers with flex circuitry. Lead times are 14 to 16 weeks. Call for pricing.

CTS Corp.
Connector Div.
9210 Science Center Dr.
New Hope, MN 55428
(612) 533-3533
▶ CIRCLE 760

CONNECTOR AND PACKAGING MANUFACTURERS

Harwin Inc.
4173 Main St., Suite 191
Bridgeport, CT 06606
(203) 261-2679
(ID) (ZI) (SM) (CC) (DP) (PG) (CD) (MD)
CIRCLE 649

Hirose Electric USA Inc.
2685-C Park Center Dr.
Simi Valley, CA 93065
(805) 522-7958
(RF) (CX) (DS) (DI) (FC) (CE) (ID) (ZI) (SM) (CC) (PG) (CD)
CIRCLE 650

Hoffman Engineering Co.
900 Ehlen Dr.
Anoka, MN 55303
(612) 422-2700
(GP) (BM) (CN) (IN) (VR) (WT) (PT) (EM) (MI) (CM)
CIRCLE 651

Honda Connectors
960 Corporate Woods Pkwy.
Vernon Hills, IL 60061
(708) 913-9566
(CX) (DS) (FC) (ID) (SM) (CC) (PG)
CIRCLE 652

Hughes Aircraft Co.
Interconnect Systems
17150 Von Karman Ave.
Irvine, CA 92714
(714) 660-5772
(FC) (CE) (ZI) (SM) (CC) (PG) (CD) (MD) (SS) (DD) (ML) (FX) (PC) (FL) (HN)
CIRCLE 653

Hybricon Corp.
12 Willow Rd.
Ayer, MA 01432
(508) 772-5422
(ML) (WR) (BP) (VB) (MB) (BU) (GB) (GP) (VR) (EM) (CM)
CIRCLE 654

Hypertronics Corp.
16 Brent Dr.
Hudson, MA 01749
(508) 568-0451
(CX) (ZI) (CD) (MD) (BI) (HV)
CIRCLE 655

ITT Cannon
Components Div.
1851 Deere Ave.
Santa Ana, CA 92705
(714) 261-5300
(AU) (RF) (CX) (DS) (DI) (FC) (CE) (ID) (ZI) (SM) (CC) (DP) (PG) (CD) (MD) (BI) (CO) (FL) (TW) (SH) (WV) (PW) (MN) (HK) (HN)
CIRCLE 656

ITT Pomona
1500 E. Ninth St.
Pomona, CA 91766
(714) 623-3463
(AU) (RF) (CX) (SM) (DP) (PG) (CD) (CO) (FL) (TW) (SH)
CIRCLE 657

Instrument Specialties Co. Inc.
P.O. Box A, I-80 Exit
Delaware Water Gap, PA 18327
(717) 424-8510
(ES) (MG) (ER) (GK) (SE) (VE)
CIRCLE 658

Interconnect Devices Inc.
5101 Richland Ave.
Kansas City, KS 66106
(913) 342-5544
(CX) (SM) (HV)
CIRCLE 659

Interlogic Industries
85 Marcus Dr.
Melville, NY 11747-4294
(516) 420-8111
(DI) (CE) (DD) (ML) (WR) (BP) (PC) (VB) (SB) (MB) (IB) (BU) (GB) (IN) (VR) (PT) (CM)
CIRCLE 660

Ironwood Electronics Inc.
P.O. Box 21-151
St. Paul, MN 55121
(612) 431-7025
(SM) (CC) (DP) (PG) (BI)
CIRCLE 661

J.S.T. Corp.
1200 Business Center Dr.
Suite 400
Mt. Prospect, IL 60056
(708) 803-3300
(DS) (DI) (FC) (CE) (ID) (ZI) (SM)
CIRCLE 662

JAE Electronics Inc.
142 Technology Dr.
Irvine, CA 92718
(714) 523-2600
(DS) (DI) (FC) (CE) (ID) (ZI) (SM) (CC) (DP) (PG) (CD)
CIRCLE 663

Keystone Electronics Corp.
31-07 20th Rd.
Astoria, NY 11105-2017
(718) 956-8900
(DS) (IN)
CIRCLE 664

Kycon Cable & Connector Inc.
1772 Little Orchard St.
San Jose, CA 95125
(800) 544-6941
(DS) (DI) (CE) (ID) (SM) (CC) (PG)
CIRCLE 665

L-COM Inc.
1755 Osgood St.
North Andover, MA 01845
(508) 682-6936
(CX) (GB) (CO) (TW)
CIRCLE 666

LEMO USA Inc.
335 Tesconi Cir.
Santa Rosa, CA 95401
(800) 444-5366
(AU) (RF) (CX) (SM) (CD) (HV)
CIRCLE 667

LZR Electronics Inc.
8051 Cessna Ave.
Gaithersburg, MD 20879
(301) 921-9440
(CX) (DS) (DI) (FC) (CD) (CO) (FL) (PW) (HN)
CIRCLE 668

Lansing Instrument Corp.
P.O. Box 730
Ithaca, NY 14851-0730
(800) 847-3535
(GP) (BM) (IN) (PT)
CIRCLE 669

Lumberg Inc.
420 Southlake Blvd.
Richmond, VA 23236
(804) 379-2010
(AU) (DI) (FC) (CE) (ID) (SM)
CIRCLE 670

MWS Wire Industries
31200 Cedar Valley Dr.
Westlake Village, CA 91362
(818) 991-8553
(CO) (FL) (TW) (SH) (WV) (PW) (MN) (HK)
CIRCLE 671

Manhattan Electric Cable Corp.
Station Plaza
Rye, NY 10580
(914) 967-8000
(RF) (CX) (DS) (CO) (TW) (SH) (PW) (HK)
CIRCLE 672

Mark Eyelet Inc.
AMP Inc.
63 Wakelee Rd.
Wolcott, CT 06716
(203) 756-8847
(ZI) (SM) (DP) (PG) (CD) (MD)
CIRCLE 673

Markel Corp.
P.O. Box 752, School Ln.
Norristown, PA 19404
(215) 272-8960
(CO) (TW) (SH) (HK) (CA)
CIRCLE 674

Master Circuits Inc.
424 Apperson Way North
Kokomo, IN 46901
(317) 457-6605
(SS) (DD) (ML) (FX) (PC)
CIRCLE 675

McKenzie Technology
44370 Old Warm Springs Blvd.
Fremont, CA 94538
(510) 651-2700
(DS) (ZI) (SM) (CC) (DP) (PG) (CD)
CIRCLE 676

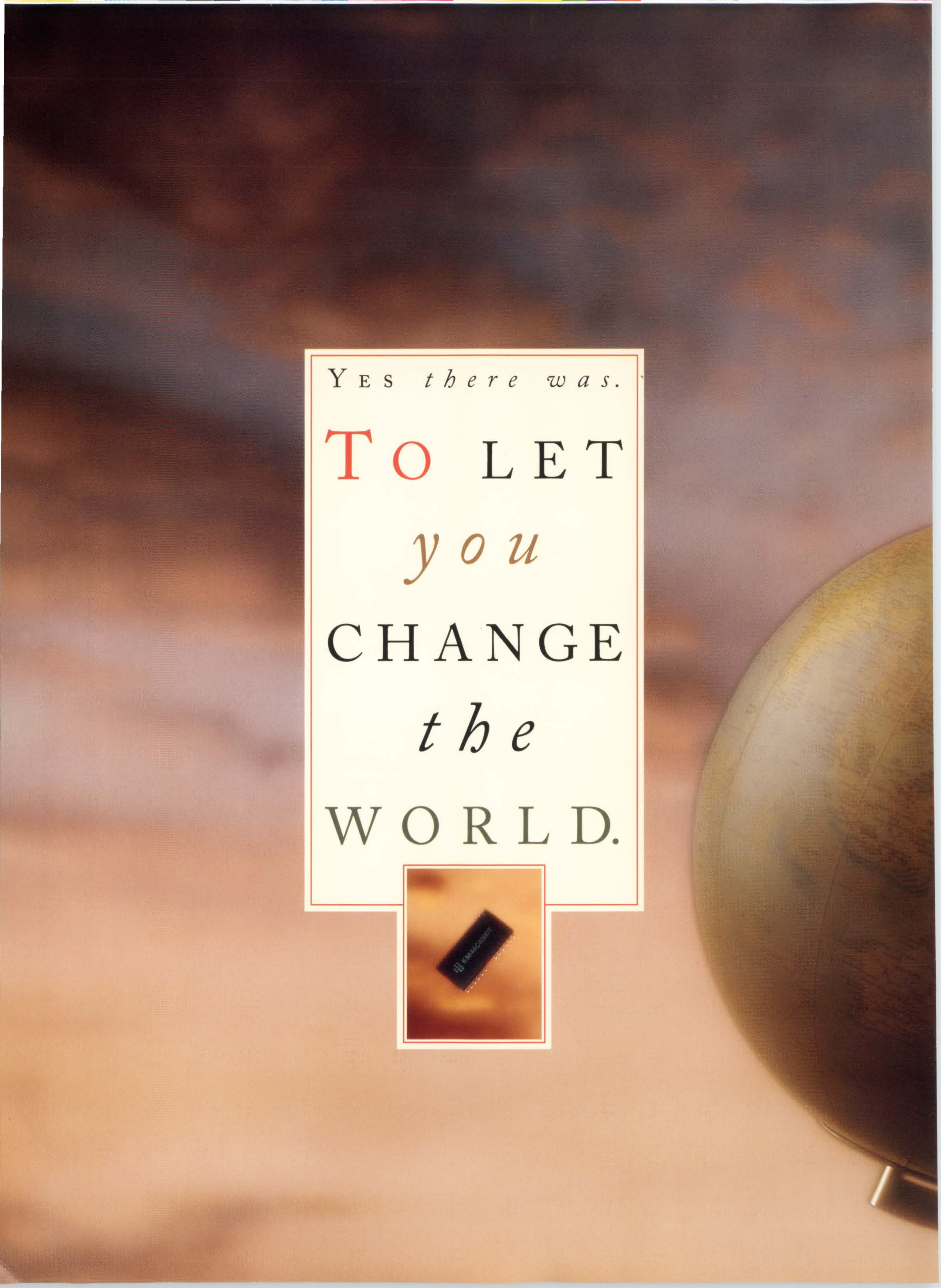
Meritec
Div. of Associated Enterprises
P.O. Box 8003
Painesville, OH 44077
(216) 354-3148
(CX) (DI) (CE) (SM) (CD)
CIRCLE 677

Methode Electronics Inc.
9334 Mason Ave.
Chatsworth, CA 91311
(818) 886-7340
(SS) (DD) (ML) (FX) (BP) (PC)
CIRCLE 678

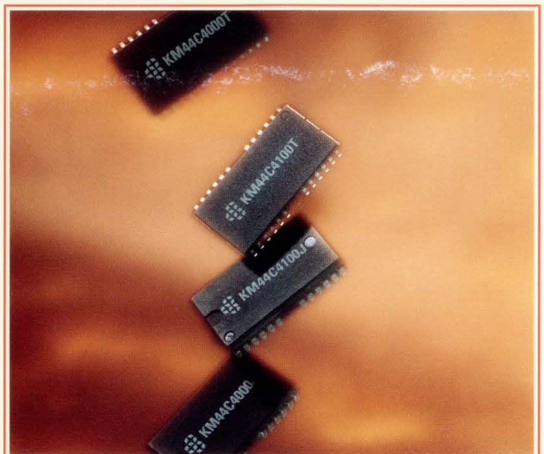
(see p. 114 for key)
(continued on p. 113)

WAS THERE *some special reason we produced*

The WORLD'S FIRST 16 *meg* DRAM?


YES there was.
TO LET
you
CHANGE
the
WORLD.

Samsung began shipping DRAM chips in the new 16M density—in production volumes—during 1991. Our customers for the product include many of the world's premiere computer and workstation makers.



The world's first 16-*meg* DRAM.

Organization	*Mode*	*Speed*	*Samples*	*Production*
16M x 1	FAST PAGE	60/70/80	NOW	NOW
16M x 1	NIBBLE	60/70/80	NOW	6-92
16M x 1	STATIC COL.	60/70/80	NOW	6-92
4M x 4	FAST PAGE	60/70/80	NOW	NOW
4M x 4	STATIC COL.	60/70/80	5-92	8-92
4M x 4 (WPB)	FAST PAGE	60/70/80	5-92	8-92
4M x 4 (WPB)	STATIC COL.	60/70/80	5-92	8-92

2K and 4K refresh available.

They tell us we are the first supplier to complete this next generation of memory.

We, in turn, see it as a significant milestone in the global effort toward elegance and power in computing.

Of equal significance, Samsung's completion of the generation marks something of a transformation in the worldwide map of supply. And we believe consumers of electronic components will benefit from this.

Yet perhaps most important, is the fact that the 16-meg will indeed help the electronics community—in the U.S. and elsewhere—to do nothing less than change the world.

The new-generation DRAMs are a significant boon to the hugely beneficial technology of today's workstations. Machines that allow us to better comprehend the world, and to advance in areas as different as medicine and transportation, finance and filmmaking.

The new generation will also, in short order, facilitate ever-more-capable notebook and palmtop computers. Computers that will make us more productive—and will also define the workplace in a whole new way.

In the near future, more will be heard from Samsung.

We are among the major makers of DRAMs in all organizations and densities, and we are an increasingly major supplier of SRAMs. We make a wide line of fast, ultra-fast, and high-density SRAMs, up to 4M in density and 8 ns in speed. Our specialty memories include ROMs, VRAMs, pseudo and cache SRAMs, EEPROMs, and FIFOs. And we also build superior ASICs, microcontrollers, MOSFETs, and RAM DACs.

And, of course, in DRAMs, there is always the 64-meg.

About which, we hope to be writing soon.

If we may provide further information of any kind, please contact us via the coupon at left, or by telephone at 1-800-446-2760.

YES. *I want to learn about the next generation of memory. Please send more information.*

Name *Title*

Company

Address

City *State* *Zip*

Return coupon to Marketing Communications, Samsung Semiconductor, 3725 No. First St., San Jose, CA 95134. Or call:

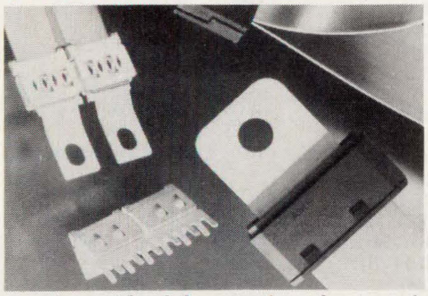
1-800-446-2760

SAMSUNG

A *Generation* AHEAD.

▼ CRIMP CONNECTORS EASE FLAT-CABLE USE

Flat copper power cable can be an alternative to bus bars and standard round wiring in computers and related equipment with the Ampower wave-crimp connector system. The units offer an insulation-displacement, residual-force crimp for termination of flat copper cable, eliminating the need to strip insulation. They're also pluggable and permit running taps off the flat cable. Connectors are rated at from 70 to 110 A, depending on configuration, with a 30°C or less temperature rise. A typical 1-ft. cable assembly with connectors on both ends runs from $5.23 to $6.38 in lots of 1000. Delivery is from four to six weeks.



AMP Inc.
P.O. Box 3608
Harrisburg, PA 17105-3608
(800) 522-6752
▶ **CIRCLE 761**

▼ MINI RIBBON CONNECTORS ARE LIGHTER THAN MOST

One of the smallest and lightest weight ribbon interconnects available is the Access II ribbon interconnects, which are 42% lighter than similar polyimide-insulated cables. The units are made by wrapping Gore-Tex expanded PTFE around single conductors, twisted pairs, or coaxes, and then sintering the jacketed construction together to form a flat ribbon cable. Features include easy branching and routability, chemical inertness, temperature resistance, a low dielectric constant, and a velocity of propagation of more than 90% the speed of light. Pricing is from $0.15 to $2 per conductor foot, depending on style.

W.L. Gore & Associates
7811 Burleson-Manor Rd.
P.O. Drawer Q
Manor, TX 78653
(512) 276-7600
▶ **CIRCLE 762**

CONNECTOR AND PACKAGING MANUFACTURERS

Methode Electronics Inc.
7444 W. Wilson Ave.
Chicago, IL 60656
(708) 867-9600
(DI) (FC) (CE) (ID) (ZI) (SM) (CC) (DP) (PG) (CD) (SS) (DD) (ML) (FX) (PC) (HN)
CIRCLE 679

Micro Plastics Inc.
Connector Div.
9180 Gazette Ave.
Chatsworth, CA 91311
(818) 882-0244
(CE)
CIRCLE 680

Mill-Max Mfg. Corp.
190 Pine Hollow Rd.
Oyster Bay, NY 11771
(516) 922-6000
(ZI) (SM) (CC) (DP) (PG) (CD)
CIRCLE 681

Minco Products Inc.
7300 Commerce Ln.
Minneapolis, MN 55432
(612) 571-3121
(FX)
CIRCLE 682

Mizar Inc.
1419 Dunn Dr.
Carrollton, TX 75007
(214) 446-2664
(VB) (SB)
CIRCLE 683

Molex Inc.
2222 Wellington Ct.
Lisle, IL 60532
(708) 969-4550
(RF) (CX) (DS) (DI) (FC) (CE) (ID) (ZI) (SM) (CC) (DP) (PG) (CD) (HV) (FL)
CIRCLE 684

Molex Industrial Interfaces
1325 Paramount Pky.
Batavia, IL 60510
(708) 879-6262
(CD) (MD)
CIRCLE 685

Mupac Corp.
10 Mupac Dr.
Brockton, MA 02401
(508) 588-6110
(ML) (WR) (BP) (VB) (MB) (IB) (BU) (GB) (GP) (CM) (ER)
CIRCLE 686

NAS Electronics
381 Park St.
Hackensack, NJ 07602
(201) 343-3156
(SM) (CC) (DP) (CD) (MD) (VB) (MB)
CIRCLE 687

Nemal Electronics Inc.
12240 N.E. 14th Ave.
N. Miami, FL 33161
(305) 899-0900
(AU) (RF) (CX) (CO) (TW) (SH)
CIRCLE 688

Nepenthe
2479 E. Bayshore Rd.
Suite 800
Palo Alto, CA 94303
(415) 496-6666
(ZI) (SM) (CC) (PG) (CD) (BI)
CIRCLE 689

Newman, M.M. Corp.
Heli-Tube Div.
P.O. Box 615, 24 Tioga Way
Marblehead, MA 01945
(617) 631-7100
(CA) (TB)
CIRCLE 690

Noble U.S.A.
5450 Meadowbrook Ind'l. Ct.
Rolling Meadows, IL 60008
(708) 364-6038
(FX)
CIRCLE 691

ODU, U.S.A.
Sub. of Otto Dunkel GmbH
4620 Calle Quetzal
Camarillo, CA 93012-8558
(805) 484-0981
(AU) (CX) (DS) (DI) (FC) (CE) (ID) (ZI) (SM) (CD) (MD) (BI) (HV)
CIRCLE 692

Omega Shielding
Products Inc.
1394 Pompton Ave.
Cedar Grove, NJ 07009
(201) 890-7455
(ER) (GK) (SE)
CIRCLE 693

Optima Enclosures
2166 Mtn. Indl. Blvd.
Tucker, GA 30084-5088
(404) 496-4000
(BP) (VB) (SB) (MB) (BU) (GB) (GP) (CN) (IN) (VR) (WT) (PT) (EM) (MI) (CM) (ER)
CIRCLE 694

PCD Inc.
2 Technology Dr.
Peabody, MA 01960
(508) 532-8800
(FC) (CE) (ID) (ZI) (CD) (MD) (BI)
CIRCLE 695

PacTec
Div. of LaFrance Corp.
Enterprise & Executive Aves.
Philadelphia, PA 19153
(215) 365-8400
(GP) (IN) (PT) (EM) (CM) (ER)
CIRCLE 696

Panduit Corp.
Connector Div.
17301 Ridgeland Ave.
Tinley Park, IL 60477-0981
(800) 777-3300
(CX) (DS) (DI) (FC) (CE) (ID) (SM) (DP) (FL)
CIRCLE 697

Penstock Inc.
520 Mercury Dr.
Sunnyvale, CA 94086-4018
(408) 730-0300
(RF) (CX) (MD) (CO)
CIRCLE 698

Poly-Flex Circuits
28 Kenney Dr.
Cranston, RI 02920
(401) 463-3180
(SS) (DD) (FX) (PC)
CIRCLE 699

Power Dynamics Inc.
59 Lakeside Ave.
West Orange, NJ 07052
(201) 736-5722
(ID) (PW) (HN) (ER)
CIRCLE 700

Powerbox Inc.
1503 Spruce St.
Boulder, CO 80302
(303) 444-1461
(IN)
CIRCLE 701

Praegitzer Industries Inc.
9255 S.W. Pioneer Ct.
Wilsonville, OR 97070
(503) 682-5500
(SS) (DD) (ML) (BP) (PC) (VB) (SB) (MB) (IB) (BU) (GB)
CIRCLE 702

Precision Interconnect
16640 S.W. 72nd Ave.
Portland, OR 97224
(503) 620-9400
(CD) (CO) (TW) (SH)
CIRCLE 703

Preh Electronic Inds. Inc.
470 E. Main St. (Rt. 22)
Lake Zurich, IL 60047-2578
(708) 438-4000
(DI)
CIRCLE 704

Premier Metal Products Co.
381 Canal Pl.
Bronx, NY 10451
(212) 993-9200
(GP) (BM) (CN) (IN) (VR) (PT) (EM) (CM)
CIRCLE 705

Pyle-National
1334 N. Kostner Ave.
Chicago, IL 60651
(312) 342-6300
(CX) (EL) (SM) (CD) (MD) (HV)
CIRCLE 706

RF Industries Ltd.
7620 Miramar Rd.
Bldg. #4100
San Diego, CA 92126
(800) 233-1728
(CX) (CO)
CIRCLE 707

Radstone Technology Corp.
20 Craig Rd.
Montvale, NJ 07645
(201) 393-2700
(VB) (MB) (BM) (EM) (MI)
CIRCLE 708

Revere Aerospace Inc.
845 North Colony Rd.
Wallingford, CT 06492-2409
(203) 269-7701
(SH) (WV) (HN)
CIRCLE 709

Ribbon Cable Co.
8753 Lion St.
Rancho Cucamonga, CA 91730
(714) 987-0007
(FL) (TW) (SH) (WV) (HN) (ER)
CIRCLE 710

(see p. 114 for key)
(continued on p. 114)

CONNECTOR AND PACKAGING MANUFACTURERS

Richard Hirschmann of America
Industrial Row, P.O. Box 229
Riverdale, NJ 07457
(201) 835-5002
(AU) (DI)
CIRCLE 711

Rittal Corp.
Electronic Products
3100 Upper Valley Pike
Springfield, OH 45505
(800) 477-4000
(GP) (BM) (CN) (IN) (VR) (WT) (PT) (EM) (CM) (MG) (ER) (VE)
CIRCLE 712

Robinson Nugent Inc.
800 E. 8th St.
New Albany, IN 47150
(800) 338-8152
(DS) (DI) (FC) (CE) (ID) (ZI) (SM) (CC) (DP) (PG) (CD) (MD) (BI) (HV)
CIRCLE 713

Rogers Corp.
Composite Materials Div.
One Technology Dr.
Rogers, CT 06263
(203) 774-9605
(EL) (SS) (DD) (ML) (FX) (PC) (CO)
CIRCLE 714

Rogers Corp.
Flexible Interconnections
2001 W. Chandler Blvd.
Chandler, AZ 85244
(602) 963-4584
(CE) (SM) (CD) (FX)
CIRCLE 715

Rogers Corp.
Power Distribution
5750 E. McKellips Rd.
Mesa, AZ 85205
(602) 830-3370
(FX) (BP) (SB) (BU) (GB) (PW) (HN)
CIRCLE 716

Rogers Corp.
Microwave/Circuit Materials
100 S. Roosevelt St.
Chandler, AZ 85226
(602) 961-1382
(CO)
CIRCLE 717

Rogers Corp.
Circuit Components Div.
2400 South Roosevelt St.
Tempe, AZ 85282
(602) 967-0624
(PG)
CIRCLE 718

Rosenberger/Micro-Coax
Div. of UTI
Box E, 245 W. 5th Ave.
Collegeville, PA 19426-0992
(215) 489-3700
(RF) (CX) (CD) (MD) (CO) (HN)
CIRCLE 719

SMK Electronics Corp. USA
1901 Nanacita Circle
Placentia, CA 92670
(714) 996-0960
CIRCLE 766

Samtec Inc.
810 Progress Blvd.
P.O. Box 1147
New Albany, IN 47151-1147
(812) 944-6733
(FC) (ID) (ZI) (SM) (CC) (DP) (PG)
CIRCLE 720

Schroff Inc.
170 Commerce Dr.
Warwick, RI 02886
(800) 451-8755
(ML) (WR) (BP) (VB) (MB) (BU) (GB) (GP) (BM) (CN) (IN) (VR) (PT) (EM) (CM)
CIRCLE 721

Shin-Etsu Polymer America Inc.
34135 7th St.
Union City, CA 94587
(510) 475-9000
(EL)
CIRCLE 722

Shogyo International Corp.
287 Northern Blvd.
Great Neck, NY 11021-4799
(516) 466-0911
(AU) (CX) (DS) (DI) (SS) (WR) (PC) (CO) (FL) (TW) (SH) (PW) (HN) (PT) (DD)
CIRCLE 723

Shokai Far East Ltd.
9 Elena Ct.
Peekskill, NY 10566
(914) 736-3500
(AU) (RF) (CX) (DS) (DI) (FC)
CIRCLE 724

Siemens Fiber Optic Components
60B Commerce Way
Totowa, NJ 07512
(201) 890-1606
(FO)
CIRCLE 725

Stantron
Unit of Zero Corp.
6900 Beck Ave.
N. Hollywood, CA 91605
(818) 841-1825
(BM) (CN) (IN) (VR) (EM) (MI) (CM)
CIRCLE 726

Strongbox
P.O. Box 2726
Culver City, CA 90231-2726
(213) 305-8288
(GP) (MI) (CM)
CIRCLE 727

Switchcraft Inc.
Components Div.
5555 N. Elston Ave.
Chicago, IL 60630
(312) 792-2700
(AU) (DS) (DI) (SM)
CIRCLE 728

Techmar Corp.
5420 McConnell Ave.
Los Angeles, CA 90066
(800) 832-4627
(GP)
CIRCLE 729

Technit Inc.
129 Dermody St.
Cranford, NJ 07016
(201) 272-5500
(ER) (GK) (VE)
CIRCLE 730

Technology 80 Inc.
658 Mendelssohn Ave. N.
Minneapolis, MN 55427
(612) 542-9545
(VB) (SB) (MB) (IB) (GB)
CIRCLE 731

Tecorp International
Interconnect Div.
19301 S. Santa Fe Ave.
Rancho Dominquez, CA 90220
(213) 764-0040
(CE)
CIRCLE 732

Teledyne Kinetics
8650 Balboa Ave.
San Diego, CA 92123
(619) 576-1005
(CE) (ZI) (SM) (CD) (MD)
CIRCLE 733

Teradyne Inc.
Connection Systems Div.
44 Simon St.
Nashua, NH 03060
(603) 889-5156
(CX) (DI) (ZI) (SM) (MD) (ML) (BP) (PC) (MB) (BU)
CIRCLE 734

Texas Instruments
Connector Systems
34 Forest St.
Attleboro, MA 02703
(508) 699-5213
(PG) (CD) (MD) (BI)
CIRCLE 735

Thomas & Betts Corp.
Electronics Div.
200 Executive Center Dr.
Greenville, SC 29616-2401
(803) 676-2900
(CX) (DS) (DI) (FC) (CE) (ID) (ZI) (SM) (CC) (DP) (PG) (CD) (MD) (FL) (TW) (SH) (HN)
CIRCLE 736

Tracewell Enclosures Inc.
567 Enterprise Dr.
Westerville, OH 43081
(614) 846-6175
(BP) (GP) (BM) (IN) (VR) (PT) (EM) (MI) (CM) (ER)
CIRCLE 737

Tricon Industries Inc.
Electromechanical Div.
2325 Wisconsin Ave.
Downers Grove, IL 60515-4076
(708) 964-2330
(CD)
CIRCLE 738

Trompeter Electronics
31186 La Baya Dr.
Westlake Village, CA 91362
(818) 707-2020
(AU) (RF) (CX) (DI) (CE) (ZI) (CC) (MD) (CO) (TW) (SH) (WV) (ES) (ER)
CIRCLE 739

Underwater Kinetics
1020 Linda Vista Dr.
San Marcos, CA 92069
(619) 744-7560
(GP) (IN) (WT) (PT) (EM) (MI) (CM) (ER) (GK)
CIRCLE 740

Veam
100 New Wood Rd.
Watertown, CT 06795
(203) 274-9681
(AU) (RF) (CX) (ID) (CD) (MD) (HV) (HN)
CIRCLE 741

Vector Electronic Co.
12460 Gladstone Ave.
Sylmar, CA 91342
(818) 365-9661
(DI) (CE) (SS) (DD) (ML) (WR) (BP) (PC) (VB) (SB) (MB) (IB) (BU) (GB) (HN) (GP) (BM) (IN) (VR) (PT) (EM) (MI) (CM)
CIRCLE 742

Vernitron Corp.
Beau Products Div.
P.O. Box 10
Laconia, NH 03247
(603) 524-5101
(CD) (HV)
CIRCLE 743

Viking Electronics Inc.
21001 Nordhoff St.
Chatsworth, CA 91311
(818) 341-4330
(DS) (CE) (ZI) (SM) (PG) (CD) (MD)
CIRCLE 744

W. L. Gore & Associates Inc.
Electronic Products Div.
4755 E. Beautiful Ln.
Phoenix, AZ 85044
(602) 438-2017
(CO) (FL) (TW) (SH) (PW) (HK) (ER) (GK) (VE)
CIRCLE 745

Wieland Inc.
466 Main St.
New Rochelle, NY 10801
(914) 633-0222
(DS) (DI) (FC) (CE)
CIRCLE 746

Wilson Case Inc.
P.O. Box 1106
Hastings, NB 68901
(402) 463-5040
(IN)
CIRCLE 747

Zero Corp.
Zero Enclosures
777 Front St.
Burbank, CA 91502
(818) 841-1825
(GP) (BM) (CN) (IN) (VR) (WT) (PT) (EM) (MI) (CM) (ES) (MG) (ER) (GK) (VE)
CIRCLE 748

Zierick Manufacturing
Radio Circle
Mt. Kisco, NY 10549
(914) 666-2911
(ID) (SM) (PG) (CD)
CIRCLE 749

Zoltech Corp.
16658 Arminta St.
Van Nuys, CA 91406
(818) 780-1800
(BM) (EM) (CM)
CIRCLE 750

KEY

Connectors and Sockets

(AU)	Audio
(RF)	Radio-frequency
(CX)	Coaxial
(DS)	D-subminiature
(DI)	DIN design
(EL)	Elastomeric
(FC)	Flat cable
(CE)	Card edge
(ID)	Insulation displacement
(ZI)	Zero/low insertion force
(SM)	Surface mountable
(CC)	Chip carriers
(DP)	DIP/SIP
(PG)	Pin-grid array
(CD)	Custom design
(MD)	Military design
(BI)	Test and burn-in
(HV)	High-voltage
(RP)	Rack and panel

Boards and Panels

(SS)	One-sided
(DD)	Double-sided
(ML)	Multilayer
(WR)	Wire-wrap
(FX)	Flexible
(BP)	Backplane
(PC)	Printed circuit
(VB)	VME bus
(SB)	Standard bus
(MB)	Multibus
(IB)	IBM PC bus
(BU)	Futurebus
(GB)	Other bus

Wire and Cable

(CO)	Coaxial
(FL)	Flat
(TW)	Twisted-pair
(SH)	Shielded
(WV)	Woven
(PW)	Power cords/cables
(MN)	Magnet wire
(HK)	Hookup wire
(HN)	Harnesses
(CA)	Cabling materials
(BB)	Bus bars

Enclosures

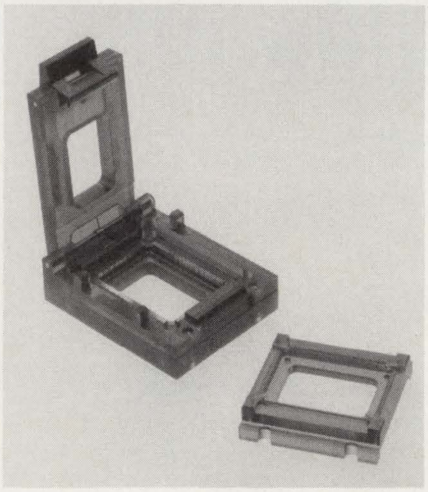
(GP)	General purpose
(BM)	Bench-mounted
(CN)	Consoles
(IN)	Instrument cases
(VR)	Vertical racks
(WT)	Water-tight
(PT)	Portable
(EM)	EMI/RFI design
(MI)	Military design
(CD)	Custom design

Shielding

(ES)	Electrostatic
(MG)	Magnetic
(ER)	EMI/RFI
(GK)	Gasket
(FR)	Ferrites
(SE)	Sheets/strips
(TB)	Tubing
(RC)	Rooms and chambers
(VE)	Vents
(WN)	Windows

CONNECTORS

▼ MCM SOCKET HANDLES TEST AND BURN-IN

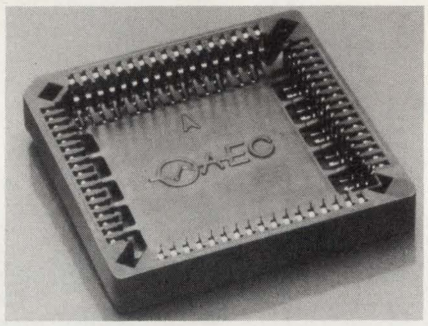


A test and burn-in socket for multichip modules handles a 256-pin unit with a 0.65-mm, 45-by-45-mm body. The socket accommodates one of the outlines included in a proposal made for package-outline standards at the recent JEDEC JC-11 meeting. Suited for high-density test and burn-in, the sockets feature a lid which simultaneously distributes a uniform mating force along all four sides of the package. Custom-machined designs are available down to 0.5-mm pitch.

Nepenthe
2479 E. Bayshore Rd.
Palo Alto, CA 94303
(415) 496-6666
▶ CIRCLE 770

▼ SMT PLCC SOCKETS BOAST LOW PROFILE

A low profile of 0.173 in. off the pc board is featured in the 654-SMO Series of plastic leaded chip-carrier sockets. The sockets accept JEDEC



MO-47 and MO-52 plastic leaded carriers on 0.050-in. centers and permit surface-mount termination to existing pc-board footprints. A high-temperature insulator is compatible with vapor-phase and infrared soldering. Sockets come in 20, 28, 32, 44, 52, 68, and 84 positions. Typical unit price for small lots is \$2.53. Delivery is from stock to four weeks.

Andon Electronics Corp.
4 Court Dr.
Lincoln, RI 02865
(401) 333-0388
▶ CIRCLE 771

▼ DC-POWER JACKS BOOST FLEXIBILITY

A line of dc-power jacks offers a wide variety of sizes, shapes, angles, configurations, platings, and mountings. A full line of mating plugs is also available. The jacks accept female plugs with center-hole diameters ranging from 2.1 to 2.5 mm and depths of up to 4.5 mm. They can be mounted at right angles or vertical on pc boards, panels, and chassis. A right-angle type for pc-board mount with a 2.1-mm center pin and nickel-plated internal components goes for \$0.18 in lots of 10,000. Delivery is within 30 days.

Shogyo International Corp.
287 Northern Blvd.
Great Neck, NY 11021-4799
(516) 466-0911
▶ CIRCLE 772

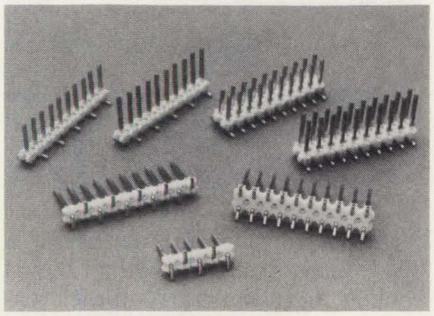
▼ 96-POSITION ASSEMBLIES ARE PROGRAMMABLE

A 96-position DIN impedance-matched cable assembly features an internal pc board which allows programming of grounds and signals to customer specifications. The high-speed, low-noise assemblies are designed for TTL, CMOS, and ECL logic signals. Units are compatible with DIN specification #41612 and mate with standard 96-position DIN connectors. Current rating is 1 A per contact. A 12-in., double-ended female assembly using 95-Ω FEP cable costs \$69.63 in lots of 1000.

Meritec
A Division of Associated Enterprises
P.O. Box 8003
Painesville, OH 44077
(216) 354-3148
▶ CIRCLE 773

▼ SMT GULL-WING HEADER WON'T WARP IN SOLDER

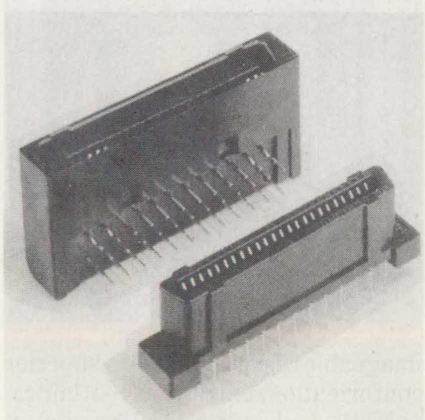
Thanks to high-temperature insulators, a line of true surface-mounted gull-wing lead headers stay dimensionally stable during vapor-phase and infrared soldering. The units include 0.040-in. holes in the insulator, between contact pins on 0.100-in. centers. The holes, along with the basic



configuration of the insulator, allow for interior handling of the connectors for automated placement on boards. Single-row sizes range from two to 40 contacts per strip, while dual-row sizes range from four to 80 contacts. A 10-position, dual-row straight header with 15-μm selective-gold plating on 0.230-in. posts costs $0.56 in lots of 1000. Delivery is in four weeks.

Crane Electronics
4700 Smith Rd., Suite R
Cincinnati, OH 45212
(800) 676-7644
▶ CIRCLE 774

▼ RIBBON CONNECTOR COMES IN HALF-PITCH



A half-pitch (0.050 in.) board-to-board ribbon connector gives designers a choice between pin-and-socket and bellows-type connectors for their microconnection needs. The FCN240 Series consists of a board-mount header and board-mount socket in straight and right-angle types. Typical applications include computer and telecommunication equipment and instrumentation. The series includes 48-, 68-, 80-, and 96-pin units. A 68-pin connector costs $6.66 in lots of 1000. Delivery is from stock.

Fujitsu Microelectronics Inc.
3545 N. First St.
San Jose, CA 95134
(800) 642-7616
▶ CIRCLE 775

▼ FLAT-CABLE JUMPERS LINK BOARDS TO BOARDS

A line of pre-bonded flat-cable jumpers and custom assemblies is designed to provide a low-cost method of direct solder board-to-board connections. The Pan-Flex jumpers are offered with 0.100- and 0.156-in. centerlines and with two to 28 and two to 24 circuits, respectively. They can be furnished with stripped and retained wire at one or both ends, with a connector at one end, or as daisy chains with two or more connectors. Call for pricing and delivery.

Panduit Corp.
17301 Ridgeland Ave.
Tinley Park, IL 60477-0981
(800) 777-3300
▶ CIRCLE 776

▼ MINI CONNECTOR LINE MEETS FUTURE NEEDS

A comprehensive range of miniature connectors meets future needs for connections both internal and external to systems. The range contains seven series, one of which is the Series 60.01/02/03/04 pin-and-socket I/O connector. Features include a contact pitch of 1.27 mm and metal shells and hoods for optimal EMI/RFI screening. Male and female types are offered in many sizes, as are IDC versions for discrete wire from 28 to 30 AWG. Call for pricing and delivery.

Harting Elektronik Inc.
2155 Stonington Ave.
Hoffman Estates, IL 60195-0710
(708) 519-7700
▶ CIRCLE 777

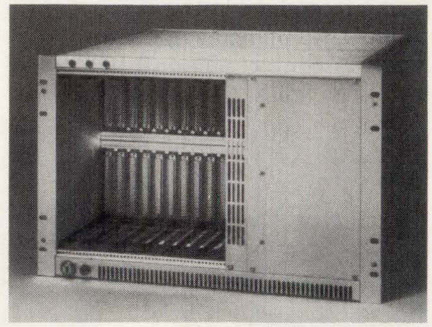
▼ FUTUREBUS+ PRODUCTS INCLUDE CARD CAGES

A family of hard-metric Futurebus+ products includes system enclosures, backplanes, card cages, and wire-wrap boards. The family is designed in accordance with IEEE 896.2. The Series 222 enclosure houses 128-bit applications and includes a 14-slot backplane for 128-bit busing with central arbitration. Card guides accept boards from 1.4 to 2.57 mm thick. A 1000-W power supply is included. Pricing is $9500 in small quantities.

Hybricon Corp.
12 Willow Rd.
Ayer, MA 01432
(508) 772-5422
▶ CIRCLE 778

▼ PRE-WIRED CARD CAGE INCLUDES POWER SUPPLY

An easy-access system offers the protection of a more enclosed, smaller package. The Power Cage III is a rack-mountable, pre-wired unit that

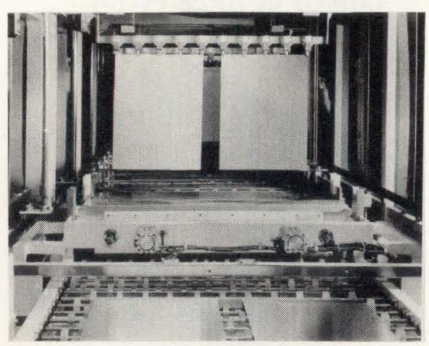


includes a 12-slot VME card cage, a 400-W power supply with integral cooling, and a Eurocard subrack featuring a 10-layer J1/J2 VME backplane. The cage fits into 12-1/4 in. of rack space. List price is $2495 with delivery in four to six weeks.

Electronic Solutions
6790 Flanders Rd.
San Diego, CA 92121
(800) 854-7086
▶ CIRCLE 779

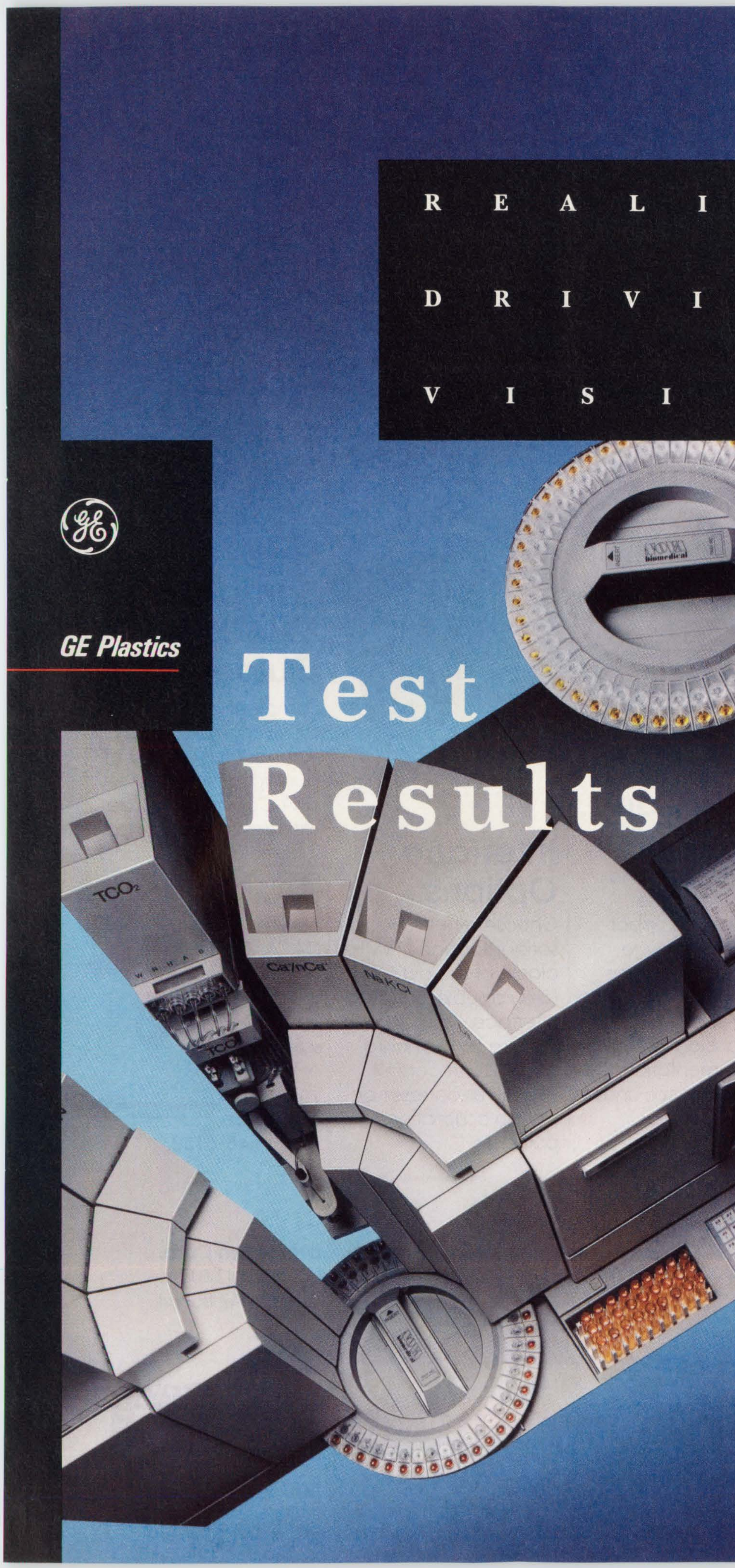
▼ ADVANCED PCB PROCESS TURNS OUT 5-MIL BOARDS

A fine-line process has been developed for volume production of boards with 5-mil lines. That same process will also be able to produce 3-mil boards shortly. The process uses electrodeposition to apply a photo



imageable resist that offers superior conformation, extra-thin coating capability, and coating uniformity on the board. Call for pricing and delivery information.

Praegitzer Industries Inc.
1270 Monmouth Cutoff
Dallas, OR 97338-9532
(503) 623-9273
▶ CIRCLE 780



To ensure your company's positive performance in today's keenly competitive marketplace, start with advanced materials and resources available from the engineering plastics leader.

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Enhance productivity and cost-efficiency with the significant process advances in progress at our massive Polymer Processing Development Center. Profit by GE Plastics' worldwide presence and market expertise.

NOVA Biomedical did, for their advanced Nucleus™ blood analyzer. **Materials:** Lexan® resin, foamable Prevex® resin, Cycolac® ABS resin. **Resources:** Design reviews; material, tooling and process selection. **Results:** Creative design with increased functionality and parts consolidation; reduced assembly and finishing for significant savings in cost.

Partnership product development—only from GE. For more information, call: **(800) 845-0600.**

CIRCLE 172 FOR U.S. RESPONSE

CIRCLE 173 FOR RESPONSE OUTSIDE THE U.S.

GE Plastics

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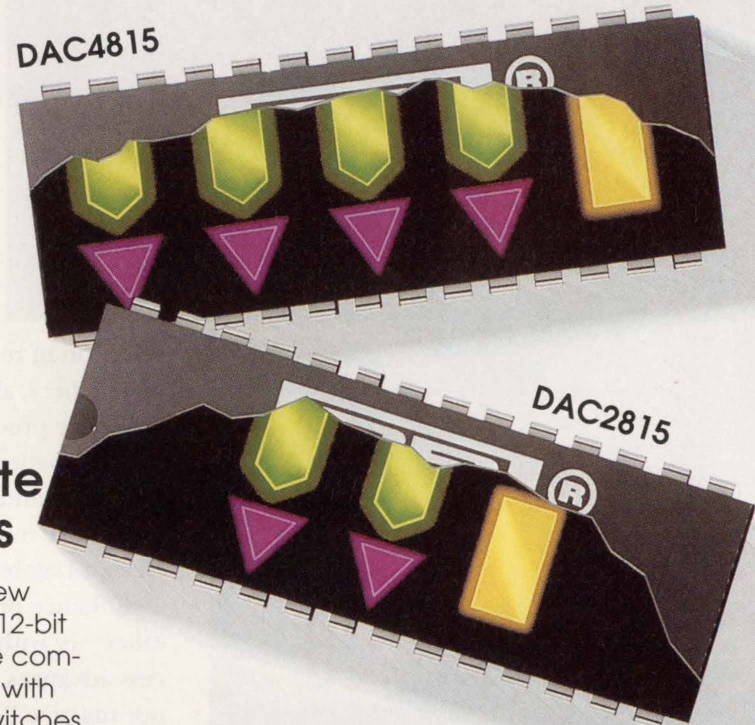
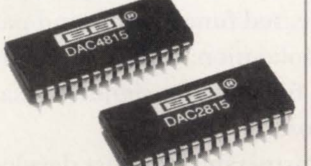
New Family of 12-Bit Dual and Quad DACs



Complete Solutions

Burr-Brown's new generation of 12-bit multi-DACs are complete solutions with CMOS logic switches, high performance buried-zener reference, and low-noise bipolar output amplifiers in cost-saving plastic packages. All are fully specified and monotonic over the extended industrial temp range of –40/+85°C.



Save Space, Cut Costs

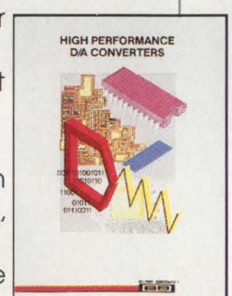
You save space and money with these complete, compact multi-DACs. They're ideal for applications requiring more than one DAC...ATE pin drivers, medical diagnostic and lab instrumentation, industrial control, and general purpose circuits.

Interface Options

Choose a high speed serial interface (10MHz clock) or a 2-byte (8+4) double-buffered interface. All models feature an asynchronous CLEAR control for power-on-reset or system calibration purposes.

Free Samples, Selection Guide

Sample the best DAC for your application. And, ask for a copy of our *High Performance D/A Converters* guide with key specs, performance diagrams, and applications information on our newest DACs. Just contact your local Burr-Brown sales office, or call for immediate assistance, **1-800-548-6132.**



Model	Function	Digital Interface	Output Range
DAC2814	Dual	Serial Port	–10V to +10V, 0 to +10V, 0 to –10V
DAC2815	Dual	8-bit Port	–10V to +10V, 0 to +10V, 0 to –10V
DAC4814	Quad	Serial Port	–10V to +10V, 0 to +10V, 0 to –10V
DAC4815	Quad	8-bit Port	–10V to +10V

Duals from $16.95. Quads from $24.95. *U.S. OEM prices, in 100s.*

Burr-Brown Corp.
P.O. Box 11400
Tucson, AZ 85734

BURR - BROWN®

CIRCLE 166 FOR U.S. RESPONSE

CIRCLE 167 FOR RESPONSE OUTSIDE THE U.S.

▼ BACKPLANE SYSTEM IS NOW SMT-COMPATIBLE

A surface-mount-compatible version is now available of the High-Density-Plus interconnection system. The system comprises individual end-stackable, modular sections that can be combined in any fashion to achieve the desired combination of signal density and power busing. Each modular section features eight rows of contacts—six rows of signal contacts plus two rows of shield contacts—for an equivalent density of 80 signal contacts per linear inch. Current pricing is $0.15 per mated contact pair. Delivery is in eight to 12 weeks.

Teradyne Inc.
Connection Systems Div.
44 Simon St.
Nashua, NH 03060
(603) 889-5156
▶ CIRCLE 781

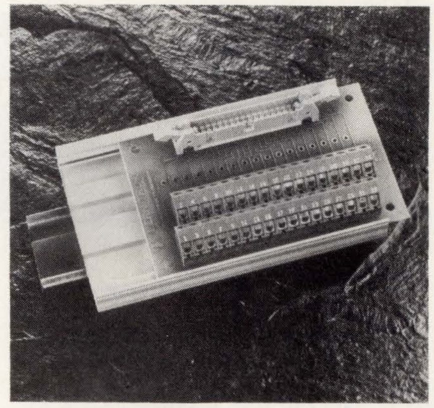
▼ VMEBUS BACKPLANE OFFERS COST GAINS

A six-layer VMEbus monolithic backplane greatly improves cost efficiency without sacrificing performance in a wide range of computing applications. The VMEplus backplane offers a stripline construction that's targeted at medium-to-high-performance applications. Two ground and two power layers separate the tracking layers, providing a secure stripline environment with controlled characteristic impedance relative to the signal traces. The result is low crosstalk, good ground-bounce protection, and a 125-A capability on the 5-V planes. Power can be applied by three different means. Call for pricing and delivery.

BICC-VERO Electronics Inc.
1000 Sherman Ave.
Hamden, CT 06514
(800) BICC-VME
▶ CIRCLE 782

▼ INTERFACE BOARDS LINK RIBBONS TO WIRES

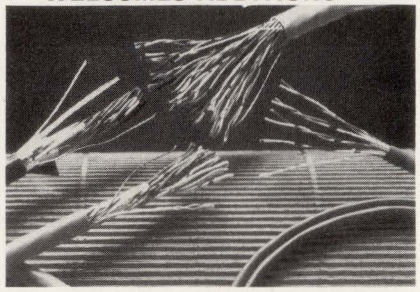
A series of passive interface boards connects ribbon cable to discrete wiring. The boards simplify circuit connections in industrial-control systems. Discrete wires are connected on one side through Eurostyle terminal strips, and emerge by way of a male ribbon-cable connector on the other side. Ten models are available with from 10 to 64 circuits and board lengths from 2 to 5 in. The 34-pin model costs about $30 in small lots. Delivery is from two to four weeks.



Vernitron Corp.
Beau Interconnect Systems Div.
P.O. Box 10
Laconia, NH 03247
(603) 524-5101
▶ CIRCLE 783

WIRE & CABLE

▼ TWISTED-PAIR LINE WELCOMES ADDITIONS

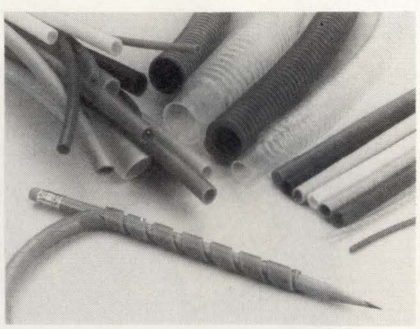


Eight-, 12-, and 25-pair configurations have been added to the DataTwist line of twisted-pair cables for data communication. Because the cables carry both voice and data signals, they save time and costs by simplifying cable runs. Termination can be made easier, especially in the wiring closet, where, for instance, a single 25-pair run of DataTwist cable can serve as a backbone to wire between floors. Call for pricing and delivery.

Cooper Industries
Belden Div.
P.O. Box 1980
Richmond, IN 47375
(800) BELDEN-4
▶ **CIRCLE 784**

▼ SPIRAL CABLE WRAP ADDS VARIETY

Eight different materials, new colors, and a wide range of sizes have been added to the Heli-Tube line of spirally cut cable wrap. The material



is an expandable plastic cable harness that applies like tape without tools. The wrap bundles wire, cable, hoses, and tubing firmly but allows flexibility. Pricing is according to materials, size, and quantity.

M.M. Newman Corp.
P.O. Box 615
Marblehead, MA 01945
(617) 631-7100
▶ **CIRCLE 785**

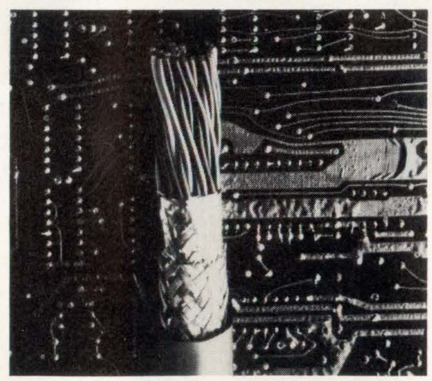
▼ SHRINK CABLE MARKERS ARE COMPUTER-READY

A heat-shrinkable cable marker is pre-mounted on pin-feed carriers to facilitate computer printing of legends. The type FM321 irradiated polyolefin material comes in yellow

only and shrinks at a ratio of 3:1. Extra flexibility permits covering of wires from 22 AWG to 400 MCM. Markers can be printed on any standard tractor-feed mechanism, typewriter, computer printer, or ink-jet system. Pricing in small quantities is $0.26 to $0.95 per marker.

Cole-Flex
91 Cabot St.
West Babylon, NY 11704
(516) 249-6150
▶ **CIRCLE 786**

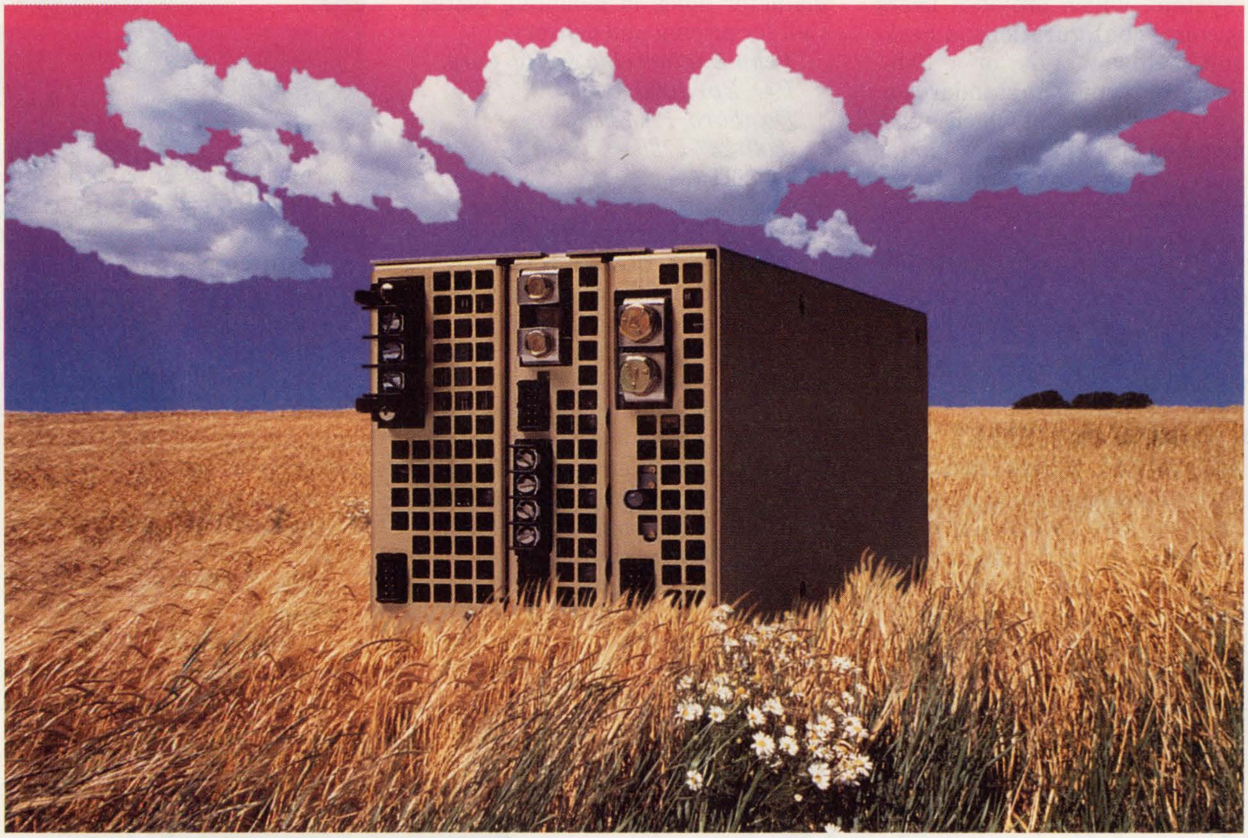
▼ ELECTRONIC CABLES WITHSTAND ABUSE



Protection against temperature extremes, oils, fuels, solvents, chemicals, water, and mechanical abuse is offered by the Xtra-Guard line of electronic cables. The family includes five distinct cable types that survive most environmental hazards while increasing productivity and adding safety. All five grades come in put-ups as short as 100 ft.

Alpha Wire Corp.
P.O. Box 711
Elizabeth, NJ 07207-0711
(800) 52-ALPHA
▶ **CIRCLE 787**

THIS YEAR'S HARVEST HAS YIELDED SOME COLORFUL RESULTS



LIKE THE NEW SPECTRUM SERIES, THE MODULAR DESIGN THAT OFFERS AN ARRAY OF STANDARD FEATURES INCLUDING PFC.

Astec introduces a new high power product of unmatched versatility and value. Its compact footprint and standard PFC front-end make the Spectrum Series compliant with IEC 555-2 while bringing significant space savings to countless designs. With up to 12 outputs plus a full range of output currents and voltages, Spectrum will accommodate any configuration of power between 500 and 2000 watts.

Many features, considered options in the industry, are standard in the Spectrum Series, including current share, remote sense, voltage adjustment, margining, power fail and level A EMI filtering - all at no additional cost.

Standard modules are stocked for fast delivery. To reap the many benefits from Astec's new Spectrum Series, call the toll free number below.

ASTEC

ASTEC STANDARD POWER
Division of Astec America, Inc.
401 Jones Rd.
Oceanside, CA 92054-1216
Telephone: 619-757-1880
Facsimile: 619-439-4243

1-800-233-9973

For Literature or Information

CIRCLE 124 FOR U.S. RESPONSE

CIRCLE 127 FOR RESPONSE OUTSIDE THE U.S.

▼ ENCLOSURE SYSTEM OFFERS HIGH FLEXIBILITY

The concept of flexibility is incorporated into the Vario Module enclosure system, which provides users with several configurations: a desktop unit, a tower style, or a 19-in. rack-mounted type. The standard enclosure is a desktop unit which is easily converted into a 19-in. rack-mount enclosure. Adding feet transforms the unit again into a tower. Call for pricing and delivery.

Rittal Corp.
3100 Upper Valley Pike
Springfield, OH 45504
(800) 477-4000
▶ **CIRCLE 788**

▼ ALUMINUM FASTENERS EASE PANEL MOUNTING

A maker of computer-systems equipment reports a 90% reduction in the time it takes to affix membrane-switch panels to chassis mounting plates and attributes the savings to PEM Snap-Top standoffs. The Type SSA fasteners snap into panels and replace numerous screws, washers, and nylon standoffs. Lengths offered are 0.437 and 0.562 in., and the fasteners are pressed into 0.156-in. diameter holes in mounting plates. Call for pricing and delivery.

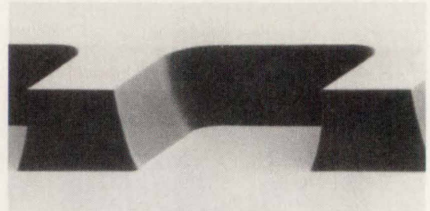
Penn Engineering & Mfg. Corp.
P.O. Box 1000
Danboro, PA 18916
(800) 237-4736
▶ **CIRCLE 789**

▼ HINGED SIDE PANELS SIMPLIFY BOX ACCESS

Hinged side panels that permit quick access to equipment fixed within an enclosure are offered on a heavy-duty line of vertical racks. Other access options include latch-removable side and top panels, hinged doors, and screw-fastened panels. 132 standard color combinations are available. Call for pricing and delivery.

Equipto Electronics Corp.
351 Woodlawn Ave.
Aurora, IL 60506-9988
(708) 897-4691
▶ **CIRCLE 790**

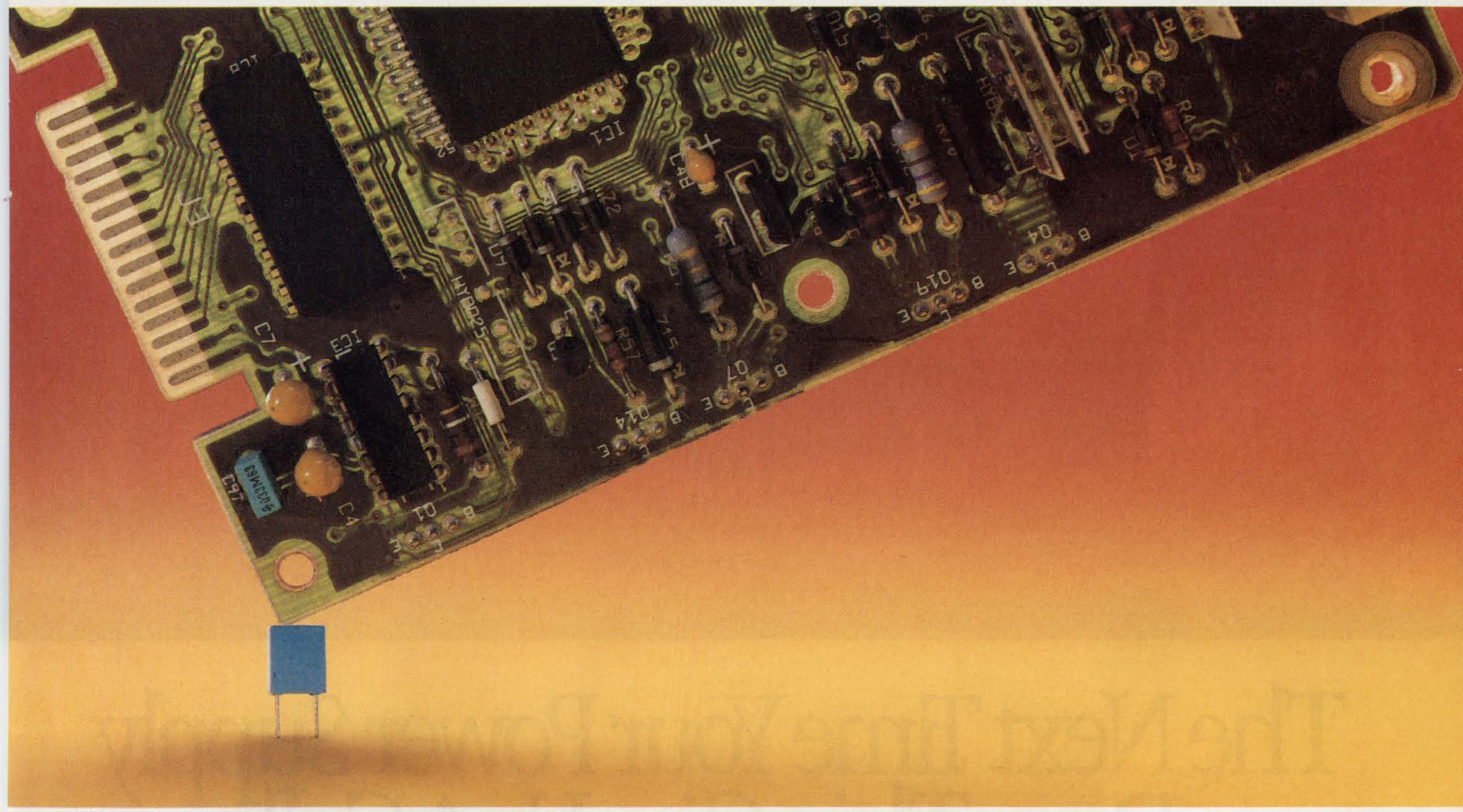
▼ POLYMERIC MCM COATS TAKE WET PATTERNING



A proprietary wet-patterning method has been developed for the Ultradel line of microelectronic coatings for multichip-module fabrication. The wet-patterning process is a low-cost alternative to conventional dry etching, which requires costly equipment and considerable process time. The coatings are also used for interlayer dielectrics, wafer passivation, and drop-on encapsulation. Call for pricing and delivery.

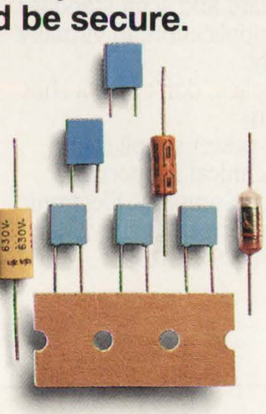
Amoco Chemical Co.
Mail Code 4207
200 E. Randolph Dr.
Chicago, IL 60601-7125
(312) 856-3200
▶ **CIRCLE 791**

SIEMENS



A capacitor can tip the balance.

Specify Siemens and be secure.



That's right. A so-called "commodity component" can tip the balance between a finished product that works and one that doesn't. Siemens capacitors offer quality and reliability you can depend on.

Your design hangs in the balance. For the highest quality at highly competitive prices, specify Siemens capacitors:

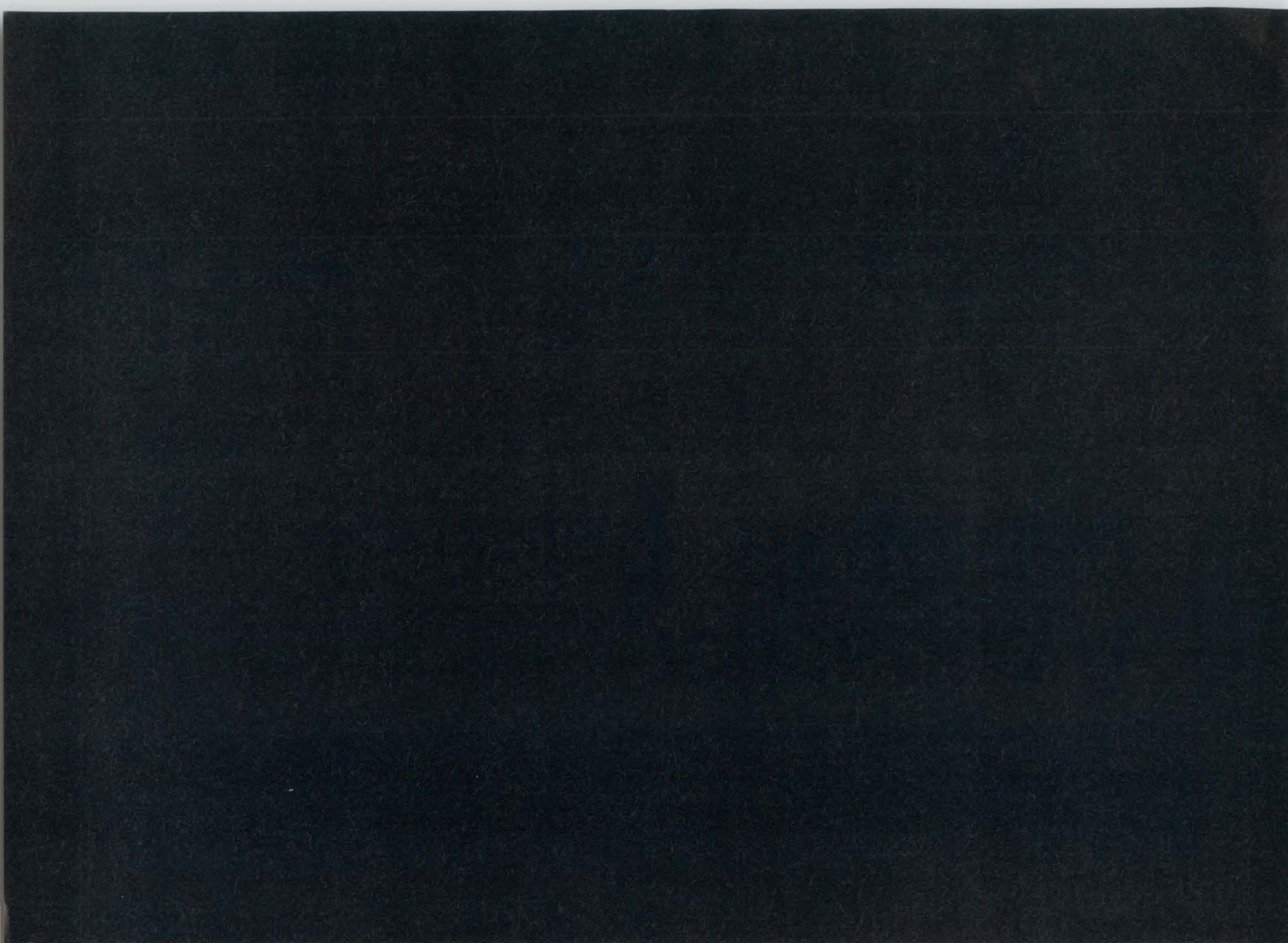
- MKT (Metalized Polyester)
- Film (Polyester, Polypropylene)
- Ceramic (Chip)
- Aluminum Electrolytic
- Power Capacitors

Call 1-800-888-7729 for a quote!
(Or fax us at 1-908-632-2830.)

SCI-1008

CIRCLE 138 FOR U.S. RESPONSE

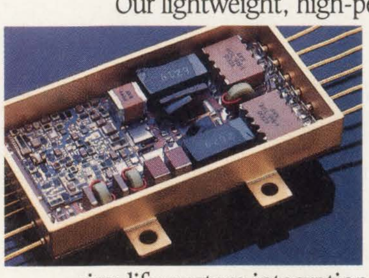
CIRCLE 139 FOR RESPONSE OUTSIDE THE U.S.



The Next Time Your Power Supply Does This, Give Us A Call.

If your power supplies have been leaving your systems in the dark, switch to Raytheon power supplies. Because we design ours specifically for reliability.

Our lightweight, high-performance power supplies boast an overall density of up to 45W/in³ and a power-to-weight ratio of 23W/oz. Modular in design, they have integral EMI filters to simplify system integration. Multilayer copper thick-film substrates for improved thermal dissipation and efficiency. And they're made with ceramic capacitors, exclusively, for increased reliability and higher maximum operating temperatures.



Raytheon's new power supplies are small but their density measures up to a big 45W/in³ and a power-to-weight ratio of 23W/oz.

Designed primarily for military and space-based electronics, Raytheon high-density power supplies are NAVMAT derated. They're manufactured in our fully automated MIL-STD-1772 certified facility. They are ideally suited for SEM-E card format, expandable to a wide variety of input and output voltages, and competitively priced.

Today, Raytheon is the largest high-reliability hybrid manufacturer in the world. We have the capacity and personnel to produce both standard and semi-standard power supplies for virtually any application, in virtually any quantity. Quickly and reliably.

When it comes to power supplies, don't take a shot in the dark. Depend on Raytheon.

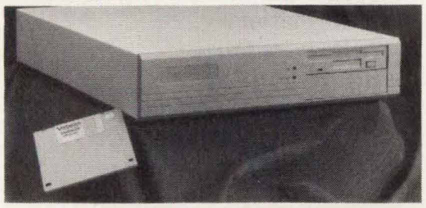
To learn how to integrate our power supplies into your systems, call or write for technical support and applications assistance. Raytheon Company, Electronic Components Division, 465 Centre Street, Quincy, MA 02169. (617) 984-8508. FAX: (617) 984-4199.

Raytheon

Where Quality Starts With Fundamentals.

CIRCLE 184 FOR U.S. RESPONSE CIRCLE 185 FOR RESPONSE OUTSIDE THE U.S.

▼ LOW-PROFILE ENCLOSURE PACKS BIG-SYSTEM POWER



Accommodating slot-CPU boards, including those with 80286, 80386, and 80486 processors, the Model 1250 enclosure incorporates the processing power of much larger and costlier systems. The unit measures just 2.75 in. high by 12 in. wide by 14.75 in. deep, and features a multilayer, three-slot passive backplane for slot-CPU boards. The 16-bit backplane uses ISA card-edge connectors and provides room for terminating resistor networks. Call for pricing.

Enclosure Technologies Inc.
256 Airport Industrial Dr.
Ypsilanti, MI 48198
(313) 481-2200
▶ **CIRCLE 792**

▼ RF/MICROWAVE PACKAGES JOIN STANDARD LINE

Standard detector and diode packages, as well as custom packages for amplifiers, mixers, switches, and SAW devices have been added to a standard line of wingpack, plug-in, and platform packages. The company offers full in-house capabilities including design, metal forming, assembly, plating, and MIL-SPEC-level quality assurance.

Hermetic Devices Inc.
3150 Pullman St.
Costa Mesa, CA 92626
(714) 557-9933
▶ **CIRCLE 794**

▼ TIP-UP CASE HANDLE MOVES IN 30° INCREMENTS

A fully adjustable tip-up carrying handle enables the angle of the Cardpac system case to be adjusted in 30° increments. Handle adjustment is as simple as depressing a central button. The handle is offered with or without a molded finger grip. Side legs are designed of sturdy die-cast zinc and are finished in satin chrome.

Schroff Inc.
170 Commerce Dr.
Warwick, RI 02886
(800) 451-8755
▶ **CIRCLE 795**

▼ ADHESIVES OFFER QUICK SMD PLACEMENT

A series of adhesives is specifically formulated for SMD applications. SMD 881 adhesive is for general SMD usage, while SMD 882 adhesive is for high-speed use and/or compatibility with Fuji placement equipment using vision systems. Both are also offered in ultra-fast curing formulations. The adhesives are suitable for all deposition methods, including pneumatic syringe, screen printing and stencilling, and pin transfer. Call for pricing and delivery.

Multicore Solders
1751 Jay Ell Dr.
Richardson, TX 75081
(214) 238-1224
▶ **CIRCLE 793**

▼ 1000-W SWITCHERS EASE INTO SYSTEMS

Built-in features that simplify system integration are key to the LZ Series of 1000-W switching power supplies. The units feature EMI compliance to FCC Class B and VDE 0871B standards as well as an auto-selectable ac input of 85 to 132 V ac or 187 to 265 V ac. Operation is from –30 to +71°C. Other features include single-wire current sharing, all status indications, wide-range dc outputs, and overtemperature protection. Pricing starts at $1025 in lots of 25, and delivery is from stock.

Lambda Electronics Inc.
515 Broad Hollow Rd.
Melville, NY 11747
(516) 694-4200
▶ CIRCLE 796

▼ DC-DC CONVERTERS OFFER HIGH ISOLATION

A series of 25-to-30-W dc-dc converters offers 1500-V input-to-output isolation, which is becoming a telecommunication standard. The PKE Series is designed for 48- and 60-V systems and offers five different models in single, dual, and triple outputs. Their low-profile (0.42-in. high) 3-by-3-in. footprint package permits board spacing as tight as 0.7 in. Pricing starts at $100 in lots of 100. Delivery is from stock.

Ericsson Components Inc.
Power Products Div.
403 International Pkwy., #500
Richardson, TX 75081
(214) 997-6561
▶ CIRCLE 797

▼ DENSE CUSTOM SUPPLIES JOIN OEM OFFERINGS

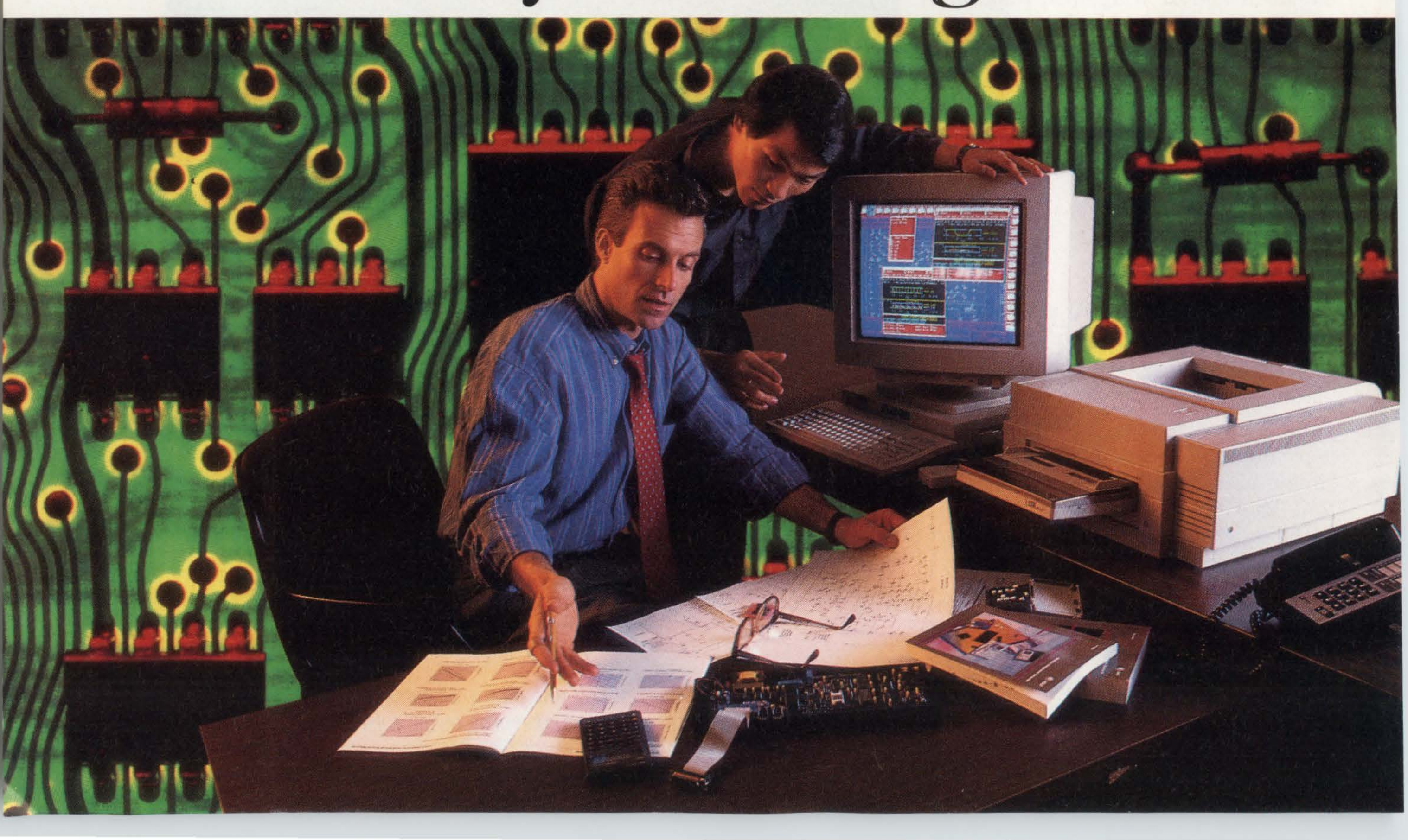
Power supplies built to meet specific performance requirements are offered in densities as high as 3 W/in.^{3} to power ratings of 350 W. The supplies meet VDE and FCC Class B standards for EMI and conform to many VME and Eurocard standards for rack-mounted power equipment. User-selectable input voltages, overvoltage protection, input-surge protection, and primary and secondary current limiting on all outputs are standard. Call for pricing and delivery information.

Taltronics Corp.
404 Armour St.
Davidson, NC 28036
(800) 666-9353
▶ CIRCLE 798

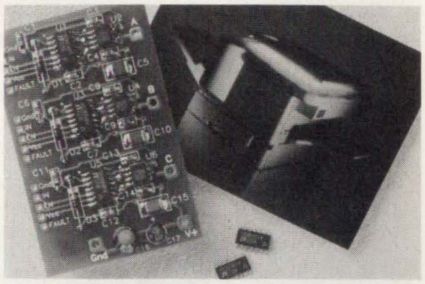
▼ 24/28-V CONVERTERS SUIT MOBILE SYSTEMS

Available in single and multiple outputs, the DB, DBT, and DBX dc-dc converters are designed for critical applications requiring operation from 24 or 28 V dc. The converters are particularly suited for mobile or transportable systems. The DB single-output series provides 250 W from 24- or 28-V dc inputs. The output delivers up to 50 A of tightly regulated 5-V power. Call for pricing and delivery.

Todd Products Corp.
50 Emjay Blvd.
Brentwood, NY 11717-3386
(800) 223-TODD
▶ CIRCLE 799



▼ SMT MOTOR DRIVER DELIVERS UP TO 5 A



The industry's first surface-mount motor driver with capability up to 5 A is the Si9976DY half-bridge driver. With one of the company's 50-V Little Foot dual n-channel MOSFETS, the driver provides a direct interface between a microprocessor and 20-to-40-V motors. The driver comes in a 14-pin, small-outline IC package. In large OEM quantities, pricing starts at $0.90. Samples are from stock.

Siliconix Inc.
2201 Laurelwood Rd.
Santa Clara, CA 95054
(800) 554-5565, ext. 1400
▶ **CIRCLE 800**

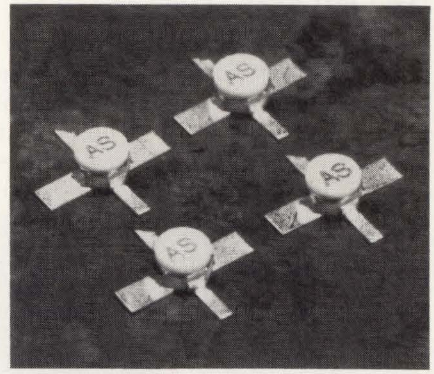
▼ 600-V GATE DRIVER INTEGRATES SIX UNITS

By integrating six output drivers—three floating 600-V types and three ground-referenced low-voltage types—the IR2130 MOS gate driver offers every element needed to drive the switches of an off-line, three-phase motor drive. The unit is the first 600-V, three-phase driver in one power IC to include such features as control logic, protection, and feedback circuitry. Packaging is a 28-pin DIP; SMT type are planned. Pricing is $8.51 in lots of 1000. Delivery is in six weeks from receipt of order.

International Rectifier Corp.
233 Kansas St.
El Segundo, CA 90245
(213) 772-2000
▶ **CIRCLE 801**

▼ LOW-NOISE AMPLIFIER SUITS MICROWAVE TASKS

Two InGaAs, heterojunction FETs are available for low-noise amplification in microwave systems. The RHF1204C/CM typically exhibits a

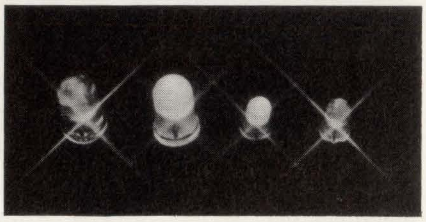


0.8-dB noise figure, while the higher-performance RHF1205C/CM exhibits a 0.7-dB noise figure, both measured at 12 GHz. The transistors have a wide range of application in signal reception from 1 GHz to over 20 GHz. Pricing in sample quantities is $5 for the 1204 and $5.50 for the 1205. Delivery is in 12 weeks from receipt of order.

ROHM Corp.
3034 Owen Dr.
Antioch, TN 37013
(615) 641-2020, ext. 117
▶ **CIRCLE 802**

▼ LOW-COST BLUE LED OPENS APPLICATIONS

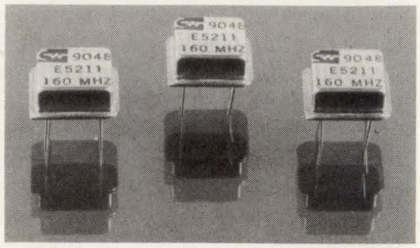
Low-cost blue LEDs are offered in four standard packages, which include T-1 and T-1-3/4 in both clear and diffused lens types. LEDs have been limited to red, green, and yel-



low for high-volume applications, but with the addition of blue, users can produce any color light in the visible spectrum, including white. Typical radiant flux for the blue LEDs is 11 μW. The devices are available for $0.97 each in lots of 1000 with delivery from stock.

Cree Research Inc.
2810 Meridian Pkwy., Suite 176
Durham, NC 27713
(800) LED-BLUE
▶ **CIRCLE 803**

▼ ECL CLOCK OSCILLATORS NOW IN HALF-SIZE CASES

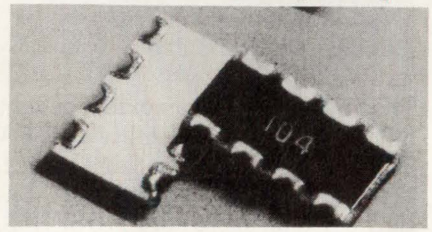


A series of ECL clock oscillators in half-size packages come in both through-hole and SMT styles. The E500 Series comes in frequencies from 24 to 180 MHz. Both standard and industrial temperature ranges are offered. Frequency stabilities are available to 25 ppm. Supply voltages are –5.2 V dc, –4.5 V dc, or 5 V dc. Model E531 (120-MHz unit) costs $43.90 in prototype quantities. Delivery is from stock to seven weeks.

Connor-Winfield Corp.
1865 Selmarten Rd.
Aurora, IL 60505
(708) 851-4722
▶ **CIRCLE 804**

▼ SMT RESISTOR NETWORKS SHRUG OFF TEMPERATURE

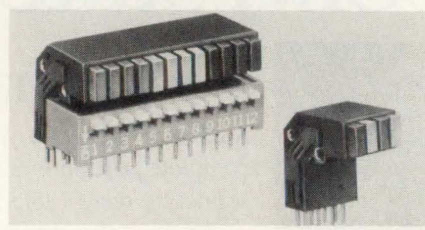
With 200 ppm/°C temperature stability, two families of surface-mounted arrays and networks suit termination and decoupling of high-speed ECL circuits. The CRM Series thick-film resistor arrays compare to 1/8-W resistors in size, but pack up to



eight resistors and two capacitors each. The MRGF Series SMT resistor networks come in 16-pin SOIC packages and carry values from 33 Ω to 2.2 MΩ. Five circuit configurations are available. The CRM Series starts at $0.80, while the MRGF Series starts at $0.30, both in lots of 10,000. Delivery is in eight weeks.

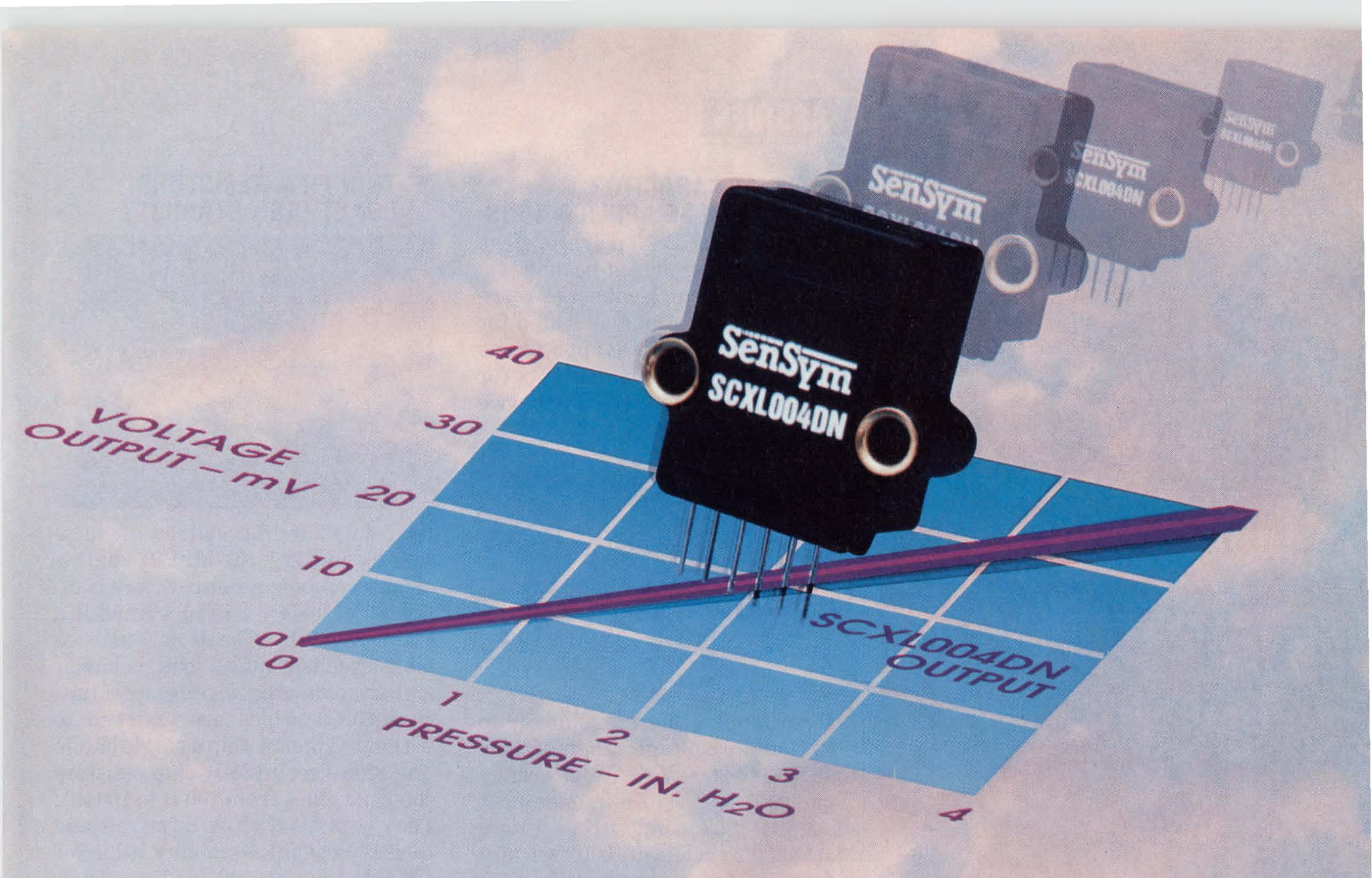
Raltron Electronics Corp.
2315 N.W. 107th Ave.
Miami, FL 33182
(305) 593-6033
▶ **CIRCLE 805**

▼ LED ARRAYS LIGHT DIP-SWITCH GROUPS



A group of right-angle, rectangular-shaped, 2-by-5-mm LEDs on 0.100-in. centers is designed to align perfectly with piano-style, right-angle DIP switches of up to 16 positions. The Series 5632D LED arrays indicate switch status at a glance and is supplied in the exact number of positions needed. Offered in red, green, and yellow, the two-leaded LEDs feature 100° viewing angles. Prices range from $0.30 per position depending on LEDs used. Production lead times are four weeks or less with samples available from stock.

Industrial Devices Inc.
260 Railroad Ave.
Hackensack, NJ 07601
(201) 489-8989
▶ **CIRCLE 806**



NEW LOW PRESSURE SENSOR

(0 to 4 inches of H_2O Full Scale)

ANNOUNCING THE NEW SCXL004DN PRESSURE SENSOR!

This new SCXL004DN sensor offers up to 10x the sensitivity of previously available solid-state sensors.

Features Include:

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- Laser Trimmed for Cal. and Temperature Compensation
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All this available now for **under $50** in 100 piece quantities.

Typical applications include:

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- HVAC Air Flow
- Gas Flows

Complete application assistance and evaluation boards are available. Call or FAX us today.

For Immediate Assistance Call: 1–800–45SENSYM

CIRCLE 234 FOR U.S. RESPONSE CIRCLE 235 FOR RESPONSE OUTSIDE THE U.S.

❒ Please call me, I'd like SCXL004DN samples for evaluation.

❒ Please rush me the *FREE* 1991 SenSym Handbook. *(This Handbook contains over 250 pages of application information and product specifications.)*

Name ____________

Title ____________

Phone # ____________

Company Name ____________

Address ____________

City ____________

State ______ Zip ____________

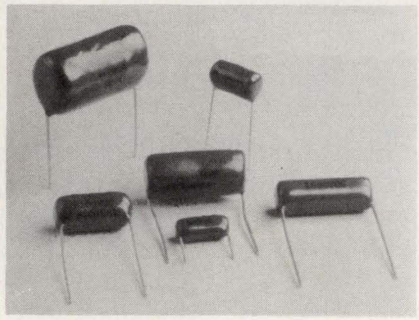
Return to:

SenSym, Inc. • 1244 Reamwood Avenue • Sunnyvale, CA 94089 • FAX (408) 734–0407

PASSIVES

▼ RADIAL CAPACITOR SUITS PULSE APPLICATIONS

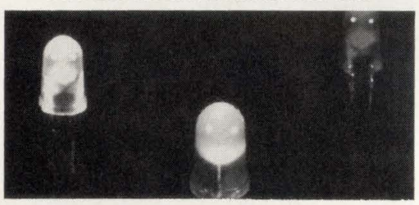
The radial Type 2013 polypropylene capacitor offers a self-healing nature and low equivalent series resistance, which make it well suited for high-current and pulse applications in horizontal deflection circuits for televisions and monitors. The device



offers an operating range of –40 to +85°C and a voltage range of 1000 and 1500 to 2000 V dc. Values range from 0.001 to 0.047 μF in tolerances of ±3%, ±5%, and ±10%. Prices start at $0.20 in lots of 1000. Delivery is from stock to eight weeks.

Tecate Industries Inc.
P.O. Box 711509
Santee, CA 92072
(619) 448-4811
▶ **CIRCLE 807**

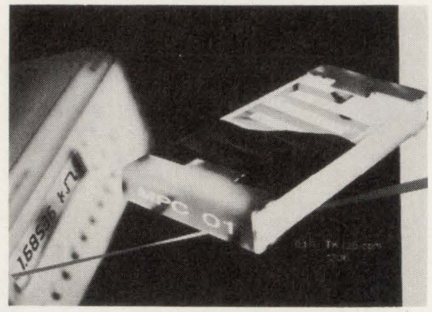
▼ LOW-CURRENT LEDs OFFER HIGH BRIGHTNESS



A line of low-current LEDs, which typically operate at 2 mA of forward current compared with 20 mA for other LEDs, offer a guaranteed luminous intensity at 2 mA. Their high brightness at a low current drive, combined with a wide viewing angle and compatibility with CMOS/MOS and TTL circuits, make these devices suited for use in low-power and battery-operated equipment. Three package sizes are offered (5, 3, and 1.6 mm) as are three colors (red, green, and yellow). Call for pricing and delivery.

II Stanley Co. Inc.
2661 Gates Ave.
Irvine, CA 92714
(800) LED-LCD1
▶ **CIRCLE 808**

▼ THIN-FILM RESISTORS BOAST HIGH STABILITY



By using thin-film instead of thick-film technology, the MPC01 chip resistors combine a temperature coefficient of below 25×10^{-6}/K with a stability of 0.1%. The devices also exhibit excellent pulse-load behavior and are available with temperature coefficients which are matched to within ±5 ppm within a single batch. The 1206-size, 0.125-W chip resistors come in values from 100 Ω to 100 kΩ. They withstand 100 V dc or rms and their typical pulse-stability value for a single pulse is 200 W, 1 μs. Their stability is 0.1% at an ambient 70°C. Call for pricing and delivery.

Philips Components
Discrete Products Div.
2001 W. Blue Heron Blvd.
Riviera Beach, FL 33404-5099
(407) 881-3308
▶ **CIRCLE 809**

▼ RESISTOR NETWORKS BEAT SOLDERING WOES

A ceramic package for chip-resistor networks seems to have solved most solderability problems commonly associated with molded SO14 and SO16 designs. The MNR Series of chip-resistor networks incorporate large solder pads and concave electrodes. The large pads promote a strong bond between component and land pattern, while the concave electrodes take advantage of a strong tendency toward self-alignment during reflow soldering. Resistance range is from 10 Ω to 1 MΩ with a ±5% tolerance. Rated wattage is 0.063 W at 70°C. Pricing starts at $15 for the 2-pin MNR02 in lots of 100,000. Delivery is from stock to 12 weeks from receipt of order.

ROHM Corp.
3034 Owen Dr.
Antioch, TN 37013
(615) 641-2020, ext. 116
▶ **CIRCLE 810**

SWITCHES & RELAYS

▼ RUGGED SPDT SWITCH OPERATES TO 4.6 GHZ

A gallium arsenide single-pole, double-throw switch operates over a wide dc-to-4.6-GHz range at a 3-ns switching speed. The ZFSWA-2-46 switch comes in a metal case measuring 1.25 by 1.25 by 0.75 in. with SMA connectors. It provides 50-dB isolation and has only 1.3 dB of loss at 1000 MHz with a typical VSWR of 1.5 in its off state. Pricing is $79.95 in lots of 10 to 24. Delivery is from stock.

Mini-Circuits
P.O. Box 350166
Brooklyn, NY 11235
(718) 934-4500
▶ **CIRCLE 811**

▼ LIGHTED PUSHBUTTONS OFFER WIDE SELECTION

The Sunmulon line of professional-grade LED-illuminated pushbutton switches and indicators features precious-metal contacts on either connector or wire-wrap terminals, high-intensity LEDs, and precision mechanical construction. A complete selection of panel- and PCB-mounted devices is available, as are matrices of up to 50 switches. Uses include medical electronics, industrial automation, and process control.

A C Interface Inc.
22391 Gilberto
Rancho Santa Margarita, CA 92688
(714) 858-1866
▶ **CIRCLE 812**

▼ SOLID-STATE SWITCH COMES IN 8-PIN DIP

A combination hookswitch and ring detector comes housed in a mini 8-pin DIP package. The P/N TS117 uses an optically isolated, MOSFET-based relay for hookswitch, dial-pulse, or loop-start switching with a bidirectional optocoupler for ringing-current or loop-current detection. The relay portion switches voltages up to 350 V peak ac or dc and passes loop currents up to 120 mA. Call for pricing and free samples.

CP Clare Corp.
Solid State Products Div.
8 Corporate Place
107 Audubon Rd.
Wakefield, MA 01880
(617) 246-4000
▶ **CIRCLE 813**

▼ SOLID-STATE RELAY SWITCHES UP TO 530 V

Line voltages of up to 530 V rms can be switched directly to high-power loads by the 53TP Series three-phase solid-state relays. Models are available to handle 25- or 50-A loads under an ac or dc control signal. The relays replace electromechanical contactors, particularly where high inrush currents and frequent operation can burn contacts. An input-status LED indicator shows the presence of control signal. Call for pricing and delivery information.

Crydom Co.
6015 Obispo Ave.
Long Beach, CA 90805
(800) 8-CRYDOM
▶ **CIRCLE 814**

▼ RUGGED KEYPADS WITHSTAND CONTAMINANTS

Wet, dirty, or otherwise harsh conditions won't affect the Storm 700 and 900 Series of keyboard modules. The silicone-rubber modules totally resist liquids, dust, many solvents and chemicals, and other contaminants. They meet NEMA 4 seal standards when correctly mounted. The 700 Series is non-illuminated, while the 900 Series modules are lighted. Four sizes are available up to a QWERTY 36-key model. Call for pricing and delivery information.

MGR Industries Inc.
450 B Industrial Dr.
Ft. Collins, CO 80524
(303) 221-2201
▶ **CIRCLE 815**

▼ SEALED SWITCHES SAVE BOARD SPACE

Pc-board space is conserved by the KT Series of sealed, miniature pushbutton keyswitches. The units measure 0.112 in. tall by 0.250 in.^{2} and incorporate a seal that withstands soldering and washing. Switch function is SPST, normally open, and momentary. Actuator buttons may be flush or up to 0.100 in. tall. Ratings are from low level to 1 VA maximum at 50 V ac or dc maximum. Prices start at $0.52 in lots of 1000. Delivery is in four to six weeks.

C&K Components Inc.
15 Riverdale Ave.
Newton, MA 02158-1082
(617) 964-6400
▶ **CIRCLE 816**

▼ RF, DATA INTERCONNECTS INCLUDE TWINAXIALS

A full line of twinaxial and BNC connectors, D-subminiatures in standard and pc-mount versions, and IBM banking systems, terminators, and accessories are covered in the 20-page Handbook CL-012. The catalog supplements the company's full-line catalog #120 and is geared toward OEMs, data installers, and the commercial market.

Manhattan Electric Cable Corp.
1 Station Plaza
Rye, NY 10580
(800) 228-MECC
▶ **CIRCLE 817**

▼ CABLE PRODUCTS COVERED IN BROCHURE

Information on high-performance specialty cable families and the integrated, controlled processes that produce them is offered in brochure #82885. AMP Inc.'s Precision Cable Division supplies transmission cable with Teflon insulation; shielded cable with wrapped foil, folded foil, or copper braid; micro and mini coaxial cable; and more. In-house manufacturing ensures high cable quality.

AMP Inc.
P.O. Box 3608
Harrisburg, PA 17105-3608
(800) 522-6752
▶ **CIRCLE 818**

▼ RACKMOUNT CHASSIS FILL 24-PAGE CATALOG

Ready-to-ship rackmount chassis drawers in 28 combinations of seven EIA heights and four standard depths come in dozens of configurations that make it easy to customize your packaging requirements. The products are detailed in a 24-page, full-color catalog replete with drawings, dimension tables, complete specs, application information, and design guides.

Techmar Corp.
5420 McConnell Ave.
Los Angeles, CA 90066
(800) 832-4627
▶ **CIRCLE 819**

▼ ENCLOSURE-SYSTEMS BOOK SPECIFIES USER BENEFITS

A broad line of flange-mounted disconnect enclosure systems is covered in the FMDC enclosure-systems catalog. The eight-page brochure describes three FMDC lines in terms of customer benefits, compatible operating mechanisms, and compliance to automotive and industrial requirements. The color catalog features a 16-page technical data insert detailing specs, accessories, compatibility, and ordering information.

Rittal Corp.
3100 Upper Valley Pike
Springfield, OH 45504
(800) 477-4000
▶ **CIRCLE 820**

▼ FIBER-OPTIC CATALOG SERVES DATACOM NEEDS

A 72-page color catalog aids engineers, network designers, distributors, and end users in selection and placement of fiber-optic cables serving the data-communication, broadcast and CATV, and control and instrumentation markets. The catalog covers the company's full line of fiber-optic products including assemblies for FDDI, cables, and the SuperLite line of hybrid cables.

Belden Wire and Cable
P.O. Box 1980
Richmond, IN 47375
(317) 983-5200
▶ **CIRCLE 821**

▼ 160-PAGE SOCKET BOOK MEETS PLUG-IN NEEDS

A full line of sockets and adapters, including those for DIPs, SIPS, and PGAs, as well as zig-zag and decoupling-capacitor sockets, is detailed in the 160-page Catalog No. 10. The catalog neatly divides products into application areas such as DIP and SIP sockets, board-to-board types, PGA sockets, adapters, and terminals. Dimensional diagrams are included for all products. The company's custom capabilities are covered in a "Design Your Own Terminal" section.

Advanced Interconnections
5 Energy Way
P.O. Box 1342
West Warwick, RI 02893
(401) 823-5200
▶ **CIRCLE 822**

▼ CIRCULAR CONNECTORS DISCONNECT QUICKLY

A 100+-page catalog of quick-disconnect circular connectors includes the mechanical-keying B series and hermaphroditic-keying S series. The catalog covers single-contact, multi-contact, and mixed-contact types. Part numbering and specifying guidelines are included, as are full specifications, illustrations, and technical drawings.

LEMO USA Inc.
P.O. Box 11488
Santa Rosa, CA 95406
(800) 444-LEMO
▶ **CIRCLE 823**

▼ PRESSURE CONNECTORS FOR FLEXIBLE CIRCUITS

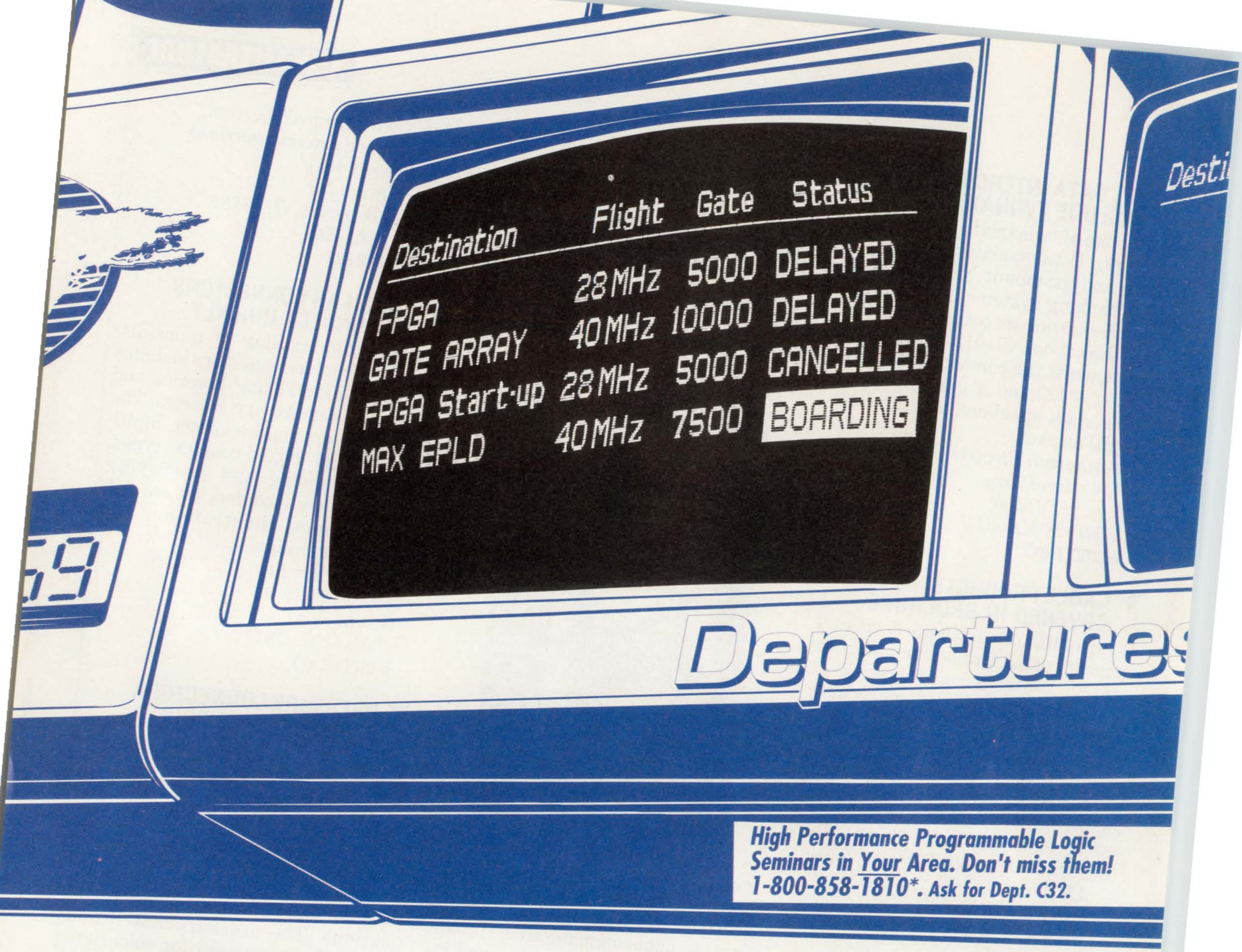
Literature is available describing the Invisicon pressure connection system, which creates demateable connections for flexible circuits. The system provides the high contact density and controlled characteristic impedance required for use in high-density and high-speed digital applications. The pressure-mated pad connections are used for solderless mating and demating of flex-to-board, flex-to-flex, and multichip-module-to-board connections.

Rogers Corp.
Flexible Interconnections Div.
2001 W. Chandler Blvd.
Chandler, AZ 85224
(602) 963-4584
▶ **CIRCLE 824**

▼ FULL-LINE CATALOG COVERS MORE CONNECTORS

The #920 full-line catalog from Molex is 20% larger than the previous edition with more coverage of fiber-optic, telecom, and SIMM-socket products. With over 35,000 devices covered, the catalog is bursting with descriptions, specs, and photos.

Molex Inc.
2222 Wellington Ct.
Lisle, IL 60532
(708) 969-4550
▶ **CIRCLE 825**



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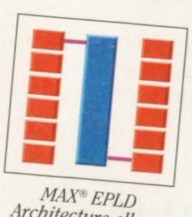

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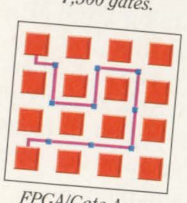

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Data Transfers Of 500 Mbytes/s Are Possible As A Novel DRAM Architecture And Bus Run At 250 MHz With 600-mV Logic Levels.

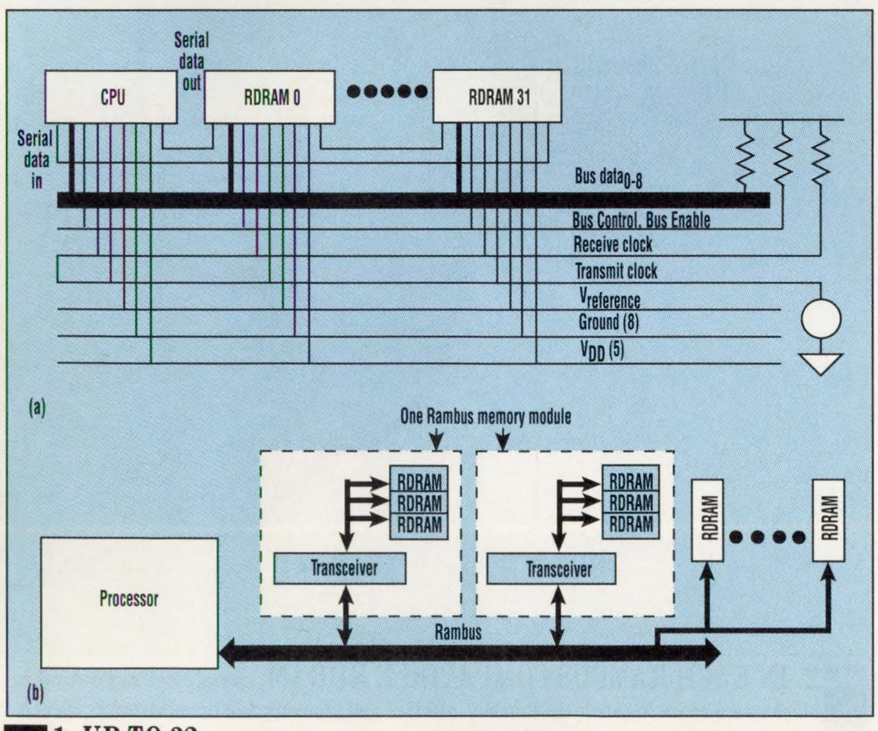
Memory-CPU Interface Speeds Up Data Transfers

Dave Bursky

Improving the throughput of today's high-end microprocessors now depends as much on the external memory subsystem as on the processor itself. This is due, in part, to the implementation of superscalar and superpipelined architectures that rely on primary on-chip caches to keep the processor busy. But keeping the internal cache filled is the task of off-chip secondary caches or other high-speed memory subsystems. Most of those subsystems employ TTL/CMOS-compatible buses over which they move the data at rates of up to about 50 MHz.

However, signals on standard TTL-level (or CMOS) buses—even on buses that tightly control their impedance when operating at high speeds—produce lots of ground-bounce noise and ringing. This tends to limit bus transfers to about 50 MHz. The smaller swing and controlled-impedance level of buses employing ECL lets buses transfer data at speeds of several hundred megahertz. However, power consumption levels soar on ECL buses due to the non-saturating nature of ECL circuits. System costs also increase along with the need for more-expensive ceramic packages, cooling subsystems, and larger power supplies.

By taking advantage of a small logic swing (just ±300 mV centered around a 2-V reference level), designers at Rambus Inc. created a unique DRAM architecture that interfaces to a very-narrow controlled-impedance chip-to-chip memory interface bus. The bus, known as the Rambus Channel, is implemented with CMOS circuits mounted on standard pc boards, yet can operate at clock speeds of 250 MHz and deliver 500 Mbytes/s. Byte-sequential data transfers are performed over the bus using both the leading and falling clock edges of timing signals. The timing, protocol-handling, and other logic signals can either be gen-



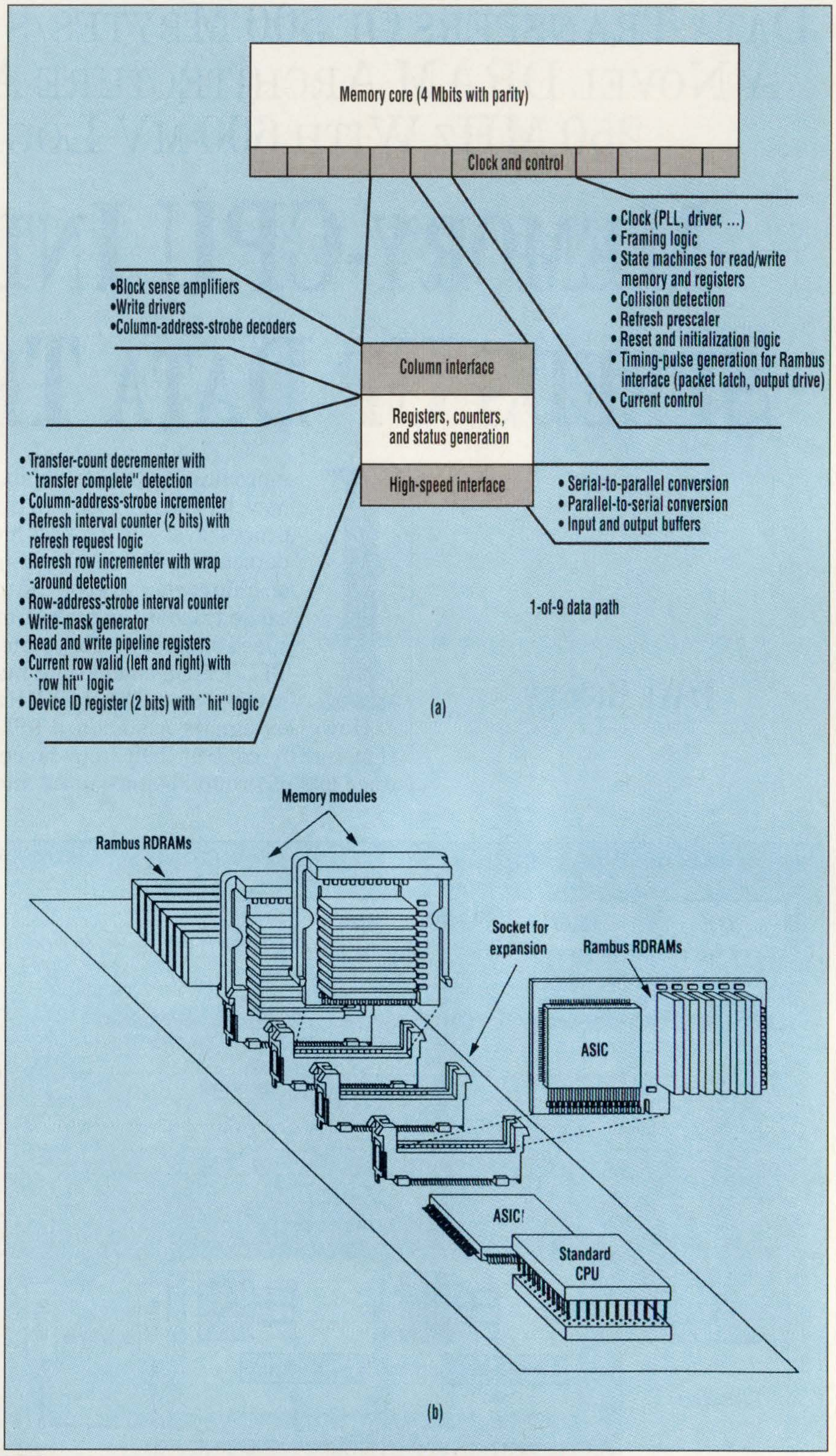
1. UP TO 32 dedicated Rambus-compatible RDRAMs can be connected directly to the CPU in a combination parallel bus and daisy-chain scheme (a). Alternatively, up to 32 RDRAMs can be grouped into a module, and up to 10 modules can be plugged into one Rambus (b).

erated by bus-master logic embedded in a host CPU, or integrated into a custom bus-master control chip. Such high-speed system buses can greatly accelerate CPU performance, or find a home in graphics subsystems.

In addition to the timing-generation, protocol-handling, and bus-interface circuits that must be included in the host logic, dedicated circuitry must be included in the memory chips. To make those memory chips widely available, Rambus tied in with several of the world's largest semiconductor manufacturers, who will supply the Rambus-compatible DRAMs (RDRAMs), as well as ASIC and off-the-shelf bus-interface support circuits. The company will also license the bus concept (patents and circuitry) and protocol to companies wishing to incorporate the bus into their commercial or proprietary products.

The length of the Rambus signals (board traces) is limited by the interrelationship of the speed of electron movement through the traces, the electrical distance, and the 2-ns clock period. As a result, designers can use up 32 discrete RDRAMs, or up to 10 special Rambus-compatible modules in the expandable format *(Figs. 1a and 1b, respectively)*. Each RDRAM is a complete memory subsystem with decoding and refresh logic, as well as Row Address Strobe (RAS) and Column Address Strobe (CAS) control on the chip. Multiple Rambus interfaces can be incorporated into a system to provide multiple data-transfer channels.

The controlled-impedance Rambus interface on the RDRAMs contains 32 pins: 16 are active, eight for grounds, five for power, and three are not yet defined. Of the active lines, there are nine data lines (eight for actual data and one that can be used for parity), two clock lines (one for transmit, one for receive), a logic reference voltage, two bus-control lines (Bus Control and Bus Enable), and Serial Input and Serial Output lines. The serial I/O lines are interconnected in daisy-chain fashion to form a ring with the CPU or other host logic. All RDRAMs, regardless



2. IN EACH RAMBUS-COMPATIBLE RDRAM, special clock and control blocks were added to handle the Rambus interface and protocol. Additional circuitry in each bit-line interface performs the serial-to-parallel and parallel-to-serial conversion needed for high-speed data transfers (a). A typical RDRAM module that contains up to 32 RDRAMs and a transceiver chip can plug into a Rambus "motherboard," which hosts up to 10 modules, for a total capacity of 160 Mbytes, using 4.5-Mbit RDRAMs (b).

of density or manufacturer, are completely compatible, thanks to the pin and bus definitions.

A 250-MHz clock signal is transmitted around a loop formed by the bus master (typically a host processor or logic circuit) and the memory chips or modules that act as slaves. Data can be transferred over the Rambus data lines at 9 bits every 2 ns by employing both the leading and trailing clock edges. Slaves transmit data along with the clock-to-master signal, and receive data in conjunction with the clock-from-master signal. The clock signal can either be generated by the master or by an external source.

Data and clock signals travel in the same direction, with propagation speeds carefully matched. Clock transitions take place at the midpoint of data. An on-chip phase-locked-loop (PLL) phase detector has extremely tight phase jitter and offset, permitting the circuits to handle the precision timing requirements.

The first Rambus DRAM that will be offered contains 4.5 Mbits of storage split into two 256-kword by 9-bit banks, with each bank containing 1 kbyte of sense amplifiers, which also serve as a secondary cache. Each DRAM thus contains two cache entries and performs very efficient cache-line replacement, due to the wide bandwidth between the sense amplifiers and the memory array. A second RDRAM, with a capacity of 18 Mbits (organized as 2M by 9) is being developed. The chip will have the same pinout, a four- or eight-bank organization, and will operate from a 3.3-V supply.

After the master broadcasts an address, the addresses enter the RDRAMs and go to an address comparator that selects the upper or lower address bank (0 to 255 kbytes, or 256 to 511 kbytes) of the RDRAM. The ability to map the DRAM addresses allows the system architect to maximize locality of the cache lines and optimize performance. Clock and control logic on the chip contains the PLL circuitry, framing logic, the state machines for reads and writes, collision detection for the transfer handshake, reset and initialization logic, timing pulse generation for the Rambus interface, and other functions *(Fig. 2a)*.

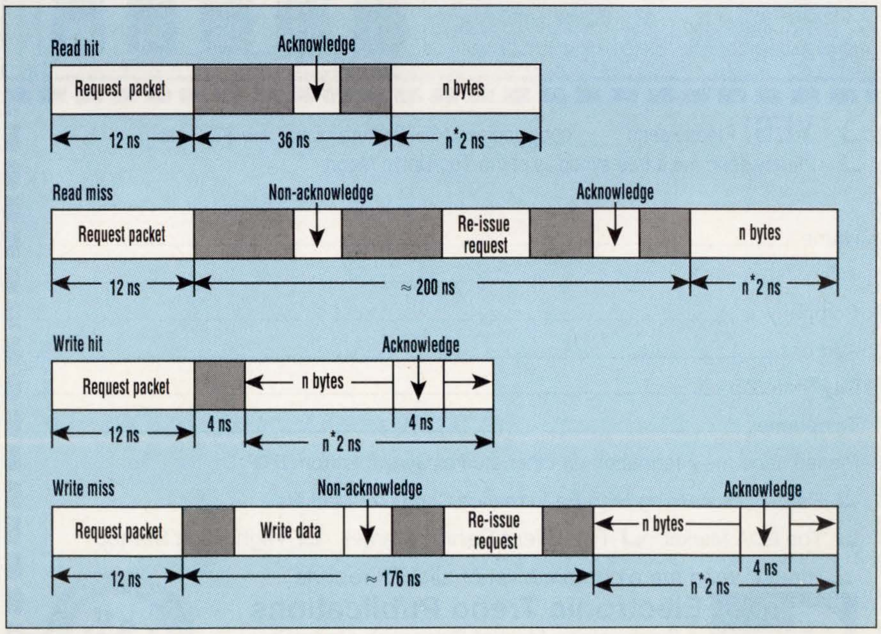
The RDRAM is "bit sliced" such that each bit-line I/O channel is subdivided into three subsections: column interface circuits; various registers, counters and status-generation logic; and a high-speed interface. The column interface section includes the standard DRAM elements, such as sense amplifiers, write drivers, and column decoders. Included in the register section are such functions as a transfer counter, a refresh interval counter, read and write pipeline registers, and more. The high-speed interface section includes serial-to-parallel and parallel-to-serial conversion logic, as well as I/O buffers.

One to 32 RDRAMs can be used directly on a single RAMbus interface, or as many as 32 can be assembled into a memory module and tied into the Rambus via a dedicated transceiver chip that resides on each module *(Fig. 2b)*. In each transceiver chip there are several PLLs to ensure proper signal timing, as well as retiming logic to restore the proper signal relationships. Such logic can also be embedded in a custom system-specific chip.

A single 4.5-Mbit RDRAM has two memory pages and two cache entries. As multiple memories are combined into a module and multiple modules combined in a system, the number of cache entries and pages increases linearly with the number of RDRAMs. A memory subsystem implemented with page-mode DRAMs might typically yield a hit rate of 30% to 40%, while a similar-size system implemented with Rambus memories would yield hit rates of over 90%. The average bandwidth on a system depends on the number of reads and writes and the number of bytes transferred. For 100 read operations of 256 bytes each, the bus has a bandwidth of 443 Mbytes/s.

Although the RDRAMs are configured as 512 kwords (or 2 Mwords) by 9 bits, with the ninth bit typically used for parity, the actual use of the ninth bit is up to the system controller. Address-mapping registers on each RDRAM allow failing chips or subsections of a chip to be mapped out of the memory space, permitting partial RDRAMs to be used while still maintaining a contiguous address space.

Modules are designed as con-



3. ALL BUS TRANSFERS for the 4.5-Mbit RDRAM start with a packet request that requires 12 ns. Once the memory chip and bus-overhead operations are completed, data transfers can take place every 2 ns. One to 256 bytes can be transferred during a Read Hit or Miss, or a Write Hit or Miss operation.

A Report describing the new market opportunity in EDA

IMPACT OF TOP-DOWN SYSTEM-LEVEL DESIGN AND LOGIC SYNTHESIS ON ELECTRONIC DESIGN AUTOMATION

REPORT SUMMARY

Has the EDA hardware user reached the saturation point? Some users are saying that they have purchased all the tools they need but hasten to add, "give me a tool that shortens my time to market and provides real productivity improvements and I'll buy!"

ETP's new 210 page report, **The Impact of Top-Down System-Level Design and Logic Synthesis on EDA**, addresses the shift from bottom up to top down systems design. The report reveals that the designers using system-level or top-down design methodology, residing at the more successful companies such as Apple Computer, Hewlett-Packard, and Sun Microsystems, are employing high-level description language tools in their workstation designs.

It describes the market niche being created for top-down design tools, with this segment growing at a much faster rate than the CAE/CAD market as a whole. Top-down design tools are growing at nearly 50% per year over the five year forecast period – compared to a 13% growth projected for the CAE/CAD tool market in 1992! The report forecasts the top-down design tool market to grow from $175 million in 1991 to $720 by 1995.

The report describes to design and product managers the current state of development of top-down system-level design tools and logic synthesizers. It also provides better insight into which tools are real and which are "hype" and what are the limitations of these tools in actually carrying out a complete design.

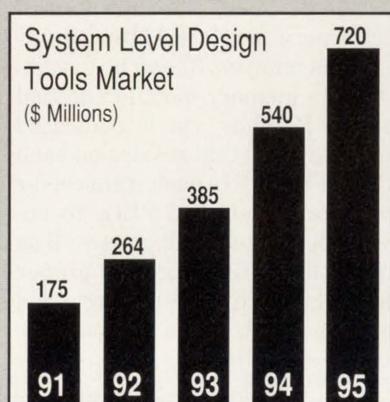
Secondly, for the reader interested in logic synthesis, this report will bring him up to date with the latest developments in logic synthesis since its 1988 market debut. Tools that synthesize logic from VHDL and Verilog (high-level language descriptions) are covered in this report.

The report examines how successful synthesis suppliers have done in their effort to take market share from Synopsys and their HDL product.

Chapter 5 deals with synthesizing programmable logic. It focuses on how and where CAE/CAD tool vendors are hoping to provide top-down tools. These tools will create netlists that can be implemented in the programmable devices in a further attempt to speed products to market!

Chapter 6 profiles twenty-one major vendors and how they are managing in the competitive market environment.

Order the report now and get the latest on this new growth EDA market — 1-800-726-6858.



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About the Author

Jonah McLeod, the editor of Electronics, has been with the magazine five years, previously covering computers and peripherals, semiconductors, and design automation. Before that, he was on the staffs of Electronic Design, Computer Design, and Systems and Software. Jonah, who has a BS in Economics from the University of Texas, has written books on hard disk drives, optical drives, logic synthesis, and silicon compilation. He is the winner of the 1990 Neal Award Certificate of Merit for editorial writing and co-winner of the 1988 Neal for editorial excellence.

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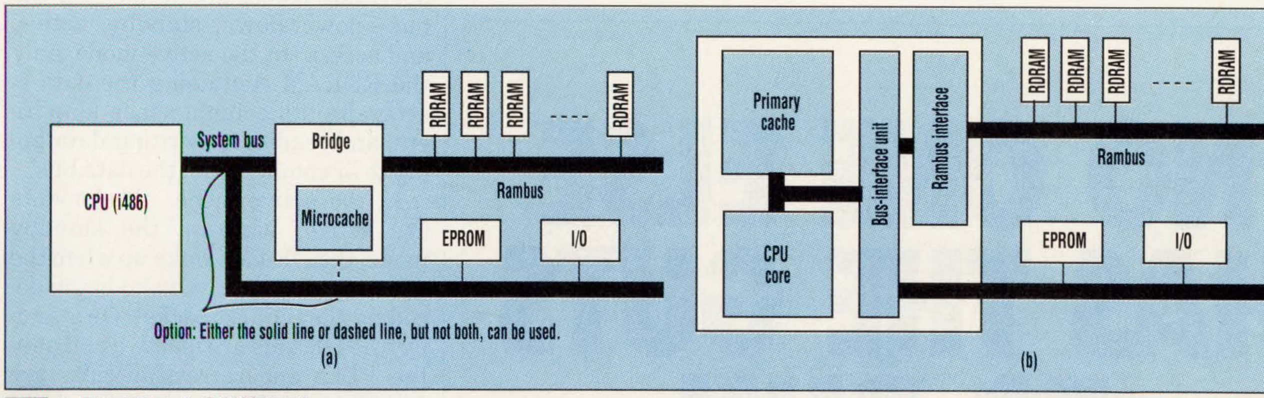


4. TO TIE A SYSTEM into the Rambus, designers can either create a "bridge" chip that ties into a standard host chip, such as an 80486 CPU (a), or create a custom host chip that has one or more Rambus interfaces as well as a standard interface bus (b).

trolled-impedance environments and are physically about 1.2-in. wide, 0.5-in. thick, and from 1- to 4-in. long, depending on the number of RDRAMs. A single Rambus Channel can extend about 10 cm (less than one clock period) and requires a minimum of four layers on the pc board to achieve a bus impedance of 50 Ω ±10%. Complete descriptions of the board layout and material were developed by Rambus to ensure system operation at the high clock rates while using standard pc-board material (FR-4) and 8-mil ±1-mil trace widths.

Up to 10 modules can reside on one Rambus Channel for a total capacity of 160 Mbytes (using the 4.5-Mbit RDRAMs), and 640 Mbytes when future 18-Mbit RDRAMs become available. The RDRAM chips are housed in special 32-lead edge-mount packages that are 950-mils wide by 460-mils high and just 47-mils thick. The package was also submitted to the Electronics Industry Association of Japan (EIAJ) for standardization approval, as well as to the JEDEC standards committee.

When the host requests data or wants to write data, it sends a Request Packet command to the RDRAMs. It then reads or writes up to 256 bytes. The protocols for the various conditions, such as Read Hits and Misses, or Write Hits and Misses, are similar *(Fig. 3)*. A packet request requires 12 ns, and depending on the action necessary, anywhere from 4 to 208 ns of delay before data starts moving across the bus. Data then moves across the bus at 2 ns/byte. Request Packet sequences consist of six consecutive bus transfers that supply the RDRAMs with the operation to be done, the address (up to 36 bits), the byte count, and some additional control information. The RDRAMs reply first with an Acknowledge Packet signal on the two control lines when a data hit occurs (data is in the cache). If a cache miss occurred, the Acknowledge Packet response is delayed until the cache is refilled with the requested data.

The high response speed of the Rambus subsystem allows the RDRAMs to actually replace secondary caches, since hit rates can exceed 95%. For the 4.5-Mbit chips, when a cache hit occurs during a Read Request, just 36 ns are needed to start reading the data (from the end of the request signal). A Read Miss requires about 200 ns for data to start flowing, a Write Hit needs just 4 ns, and a Write Miss requires about 170 ns for data to start moving. The forthcoming 18-Mbit RDRAM will permit even faster response times.

When implementing a system with the Rambus features, many architectural options are available, depending on whether or not the host chips include the Rambus interface. If they don't, then a "bridge" chip can be implemented. The bridge chip can tie a CPU like an 80486 to the Rambus memory subsystem by integrating a micro-cache on-chip along with a local CPU interface and the Rambus protocol and physical-layer interface *(Fig. 4a)*. An alternative would be to have the bridge generate the local bus interface. That offloads the CPU's local bus, improving CPU timing margins.

Additional chip area can be allocated for application-specific needs, such as a high-performance graphics controller. A combination of gate array and standard-cell techniques can be used to quickly create multiple application-specific versions. In a 1-μm process, the physical-layer interface requires less than 7 mm^2 of silicon. A 62.5-MHz crystal provides the timing signals for all bridge logic, except for the specialized Rambus interface, which picks up the 250-MHz Rambus clock generated by an onboard or external synthesizer. The Rambus interface can also accept other frequencies thanks to a unique internal synchronizer.

The same functionality that a bridge chip could incorporate can also be embedded in a custom processor *(Fig. 4b)*. The host chip could incorporate both Rambus and standard CPU bus interfaces, allowing the host chip to tie into standard components, as well as the Rambus-specific devices. By incorporating a small prefetch buffer (as little as 64 bytes) in the primary cache, the system can deliver performance equivalent to a system with a large secondary cache.

Although the Rambus interface employs a reduced-voltage swing, the high clock rates still cause the bus to dissipate a significant amount of power when it's active. To minimize the power drain, four different operating modes are defined for the bus—power-down, standby, active, and access. In the active mode, only the RDRAM containing the data is accessing its column sense amplifiers, and reading or writing data going to or coming from the data bus.

In the active mode, all elements are active, while in the standby mode, the DRAMs wake up when the starting bit is received and begin decoding the request packet. On standby, the DRAMs are inactive and only the PLLs and refresh circuits are functioning. Dissipating the least amount of power of all modes is the power-down mode, in which all circuits are turned off. In a typical Windows frame-buffer application employing 4.5-Mbit RDRAMs, peak RDRAM power runs 590 mW to 1.12 W. Power levels will be further cut when the 3.3-V version of the 18-Mbit chip is used.□

PRICE AND AVAILABILITY

The Rambus interface can be licensed by semiconductor or system manufacturers wishing to incorporate the bus into chips they design. No fees or royalties are paid by system designers using RDRAMs or Rambus-compatible ASICs, or off-the-shelf Rambus products. In production quantities, the 4.5-Mbit RDRAM will probably cost slightly more than its 20%-per-bit die overhead over standard similar-density DRAMs. A host-specific bridge circuit, customized host chip, or graphics controller can be created using ASIC tools and programmable logic or gate-array approaches. Contact Fujitsu, NEC, and Toshiba for their respective product plans regarding 4.5- and 18-Mbit memory introductions, as well as for ASIC cells or off-the-shelf chips.

Rambus Inc., 2465 Latham St., Mountain View, CA 94040; Dave Mooring, (415) 903-3800. **CIRCLE 515**

Fujitsu Microelectronics Inc., IC Div., 3545 N. First St., Bldg. 1, San Jose, CA 95134-1804; Charlie Shafton, (408) 922-9825. **CIRCLE 516**

NEC Electronics Inc., 401 Ellis St., M/S MV4572, P.O. Box 7241, Mountain View, CA 94039-7241; Hank Bardsley, (415) 965-6356. **CIRCLE 517**

Toshiba America Electronic Components Inc., 9775 Toledo Way, Irvine, CA 92718; Linda Malstrom, (714) 455-2000. **CIRCLE 518**

HOW VALUABLE?	CIRCLE
HIGHLY	567
MODERATELY	568
SLIGHTLY	569

ROLL YOUR OWN HIGH-END ANALOG ICs

ANALOG ARRAYS OFFER HIGH-PERFORMANCE ATTRIBUTES, SUCH AS SPEED, BANDWIDTH, AND PRECISION FUNCTIONS.

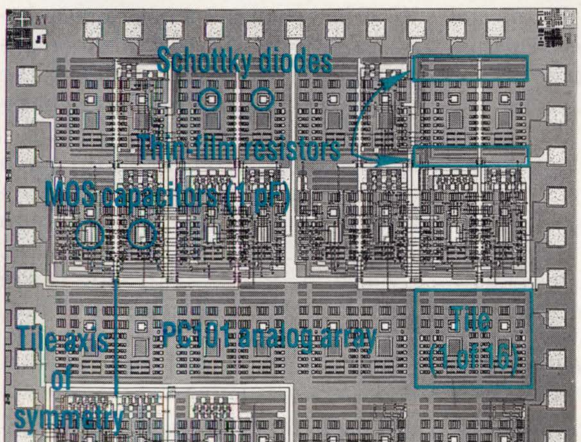
FRANK GOODENOUGH

Driven by a myriad of applications, complementary-bipolar semiconductor processes now dominate in the fabrication of fast/high-frequency analog ICs. Though developers of such processes know who will use the first ICs made on those processes and for what purpose, the path to final-chip definition and the time required to get the ICs on the market varies with each customer.

One approach is to let the customer drive product development. The customer designs a semicustom analog array specifically to fabricate on the new process. The array thus becomes a tool for in-house designers to reduce prototyping time for new standard-product ICs. In the hands of customers, it can quickly create a broad customer base, and indicates what products are needed by specific markets.

Now, AT&T and Raytheon have each chosen an array to showcase new complementary-bipolar (CB) processes. Both offer the IC designer npn and pnp transistors with multigigahertz f_ts. AT&T's 6-V CBIC-V process provides npn transistors with a double-digit f_t of 10.2 GHz, and pnp transistors with an f_t of 4.8 GHz. Raytheon's 10-V CB process offers npn and pnp transistors with f_ts of 4 and 2.5 GHz, respectively. AT&T's process provides designers with the ALA110 analog array, while the Raytheon CB process offers the PC101 analog array.

Although designers at AT&T have long had access to fast CB processes, this is Raytheon's first. In many respects, Raytheon's process, available on a family of arrays, is similar to AT&T's four-year-old, 12-V CBIC-U process whose npn and pnp transistors furnish f_ts of 3.5 and 2.7 GHz, respectively.



1. A COMPLETE ANALOG "system on a chip" can be built with Raytheon's PC101 analog array. It consists of 16 symmetrical and identical tiles, each with 24 npn and 16 pnp transistors. Each tile has general-purpose, precision, and high-speed/wideband macros.

DEFINING DIFFERENCES

Structurally, AT&T's and Raytheon's arrays differ significantly. However, their applications (the markets they aim for) and many of the basic circuit functions they will host are similar. In addition, both come with powerful macros reflecting those functions *(see the table)*. All of the macros have been integrated, tested, and characterized. They range from high-speed/wideband op amps and comparators to special-purpose video, communications, and ATE building blocks, the latter three indicative of their targeted markets. Over the next few months, AT&T will announce a family of high-performance standard products built on the array with these macros.

Raytheon's 12,600-mils² PC101 array employs a tile architecture *(Fig. 1)*. Each of its 16 identical tiles contains 24 npn and 18 pnp transistors of various sizes, for a total of 384 npn and 288 pnp transistors. All but six of the smallest transistors of each type are Schottky-clamped. AT&T's 6400-mils² ALA110 array, on the other hand, distributes the transistors symmetrically about the chip's center line over the die *(Fig. 2)*. The ALA110 contains 51 npn and 48 pnp transistors of various sizes, with the smaller devices on the left for low-level input stages, medium-sized devices in the center, and large driver and output transistors on the far right. Five groups of cross-coupled npn/pnp transistor pairs with common centroids are provided for gain stages. Chip symmetry minimizes thermal gradients and other parasitics.

The AT&T array is designed to build high-speed and wide-bandwidth small-scale-integration analog ICs, like chips containing one op amp or video amplifier, or a high-speed comparator. Alternatively, a chip using the array might contain several matched complementary transistors, several high-speed current sources with active loads, and a fast-settling, precision reference.

In contrast, Raytheon's array puts a complete pc-board system or subsystem on one chip. Most typical systems need slower general-purpose and precision circuits, as well as those offering speed and/or bandwidth. Such an IC will take advantage of the speed offered by the process, as well as its speed-power product and its small transistors, both also functions of the process' fine geometry. Many circuits designed on the process will be general-purpose, or precision, analog building blocks with significant performance at low power. A typical IC might contain a dozen general-purpose op amps, two precision op amps with an offset voltage under 1 mV, and several 160-MHz current-feedback op amps, all of which are available in macros. While most macros occupy only one tile, Raytheon crammed two general-purpose op amps onto a single tile, and expects to raise that to four.

The 16 tiles on Raytheon's array are arranged symmetrically on the chip. Each tile has its own axis of symmetry to minimize parasitics and thermal gradients. The smaller transistors are located at the bottom of each tile and the larger ones at the top. Two large Schottky diodes and two programmable 1-pF-maximum MOS capacitors are located in the center of each tile. The "bright" capacitors are metallized (programmed); the darker ones are not. The long, thin stripes at the top and bottom of each tile are precision thin-film resistors *(Fig. 1, again)*.

FUNCTIONS AND PERFORMANCES FOR AT&T AND RAYTHEON ANALOG ARRAYS

AT&T ALA100

Macro function	Specification
High-frequency active load	Source/sink 1 mA at 1 GHz/30 mA at 750 MHz
Wideband buffer	Output settles to within 0.01% in 200 ns
ECL-compatible ±5-V and single-supply comparators with and without latches	1-ns propagation delay, 8-bit accuracy, 70-ps dispersion, 50-ps overdrive variation (available as a standard product)
Dual/single-supply 100-200-MHz low-power op amp	100-mW power dissipation at 200-MHz bandwidth (available as a standard product by mid-1992)
Dual/single-supply 500-MHz op amp	250-mW power dissipation at 500-MHz bandwidth Settles to within 0.01% in 15 ns (available as a standard product by mid-1992)
Dual/single-supply wideband buffer	1-ns rise and fall time, 750-MHz bandwidth (available as a standard product in the fall of 1992)
Dual/single-supply transimpedance amplifier	500/750-MHz 3-dB bandwidth (available as a standard product in the fall of 1992)
High-speed analog multiplexer	750-MHz bandwidth, 60-dB off-state isolation (available as a standard product in the fall of 1992)

RAYTHEON PC101

Macro function	Specification
Single/dual-supply general-purpose op amp	0.5-mV offset, 70-dB open-loop gain, 4-to-25-MHz user-set bandwidth, settles to within 0.1% in 100 ns
Dual-supply, precision op amp	300-μV offset, 100-dB open-loop gain, 5-MHz bandwidth, settles to within 0.1% in 1 μs
Single/dual-supply 50-Ω-drive op amp	Puts ±3 V across 50 Ω, 5-mV offset, 60-dB open-loop gain, 35-MHz bandwidth
Dual-supply 160-MHz current-feedback op amp	5-mV offset, 1400-V/μs slew rate, settles to within 0.1% in 200 ns
Ultra-fast buffer	Puts ±4 V across 4 Ω, slews at 3000 V/μs, ±0.5-dB full-power bandwidth of 200 MHz
Dual-supply general-purpose comparator	2-mV offset, 25-ns-response-time comparator
Single/dual-supply precision comparator	300-μV offset, 40-ns response time
Dual-supply, ECL-output comparator with latch	5-mV offset, 2-ns response time
Single supply 1.23-V bandgap reference	20-ppm/°C temperature coefficient
Other fast/wideband macros	Synchronous demodulator, AGC circuit, sampling amplifiers

Current gains, or betas, for the ALA110's npn and pnp transistors typically run over 100 and just under 50, respectively. Both types of transistors come in four sizes, with operating currents ranging from less than 1 mA to over 30 mA, depending on current output, current gain, and frequency response required.

The ALA110's over 250 implanted resistors range in value from 25 Ω to 10 kΩ, with absolute accuracy from ±20 to ±40%. Adjacent devices match within ±1%, and while matching, feature a temperature coefficient of resistance (TCR) of about 1200 ppm/°C. For greater precision, approximately 14% of the die is available for the deposition of laser-trimmable, tantalum-nitride resistors. Untrimmed devices match within ±1.4% and have TCRs of –200 ppm/°C. A large selection of programmable capacitors with metallization are available, including those along the die's edges for power-supply bypassing. The array has 16 bonding pads.

Current gains for the PC101's npn and pnp transistors on each tile usually run 80 and 30, respectively. Both transistor types come in three sizes. Typical operating currents range from less than 1 mA to over 15 mA, again depending on current output, current gain, and frequency response required. The array's six complementary pairs of large transistors can be used as low-noise input or high-current output devices. Additional devices on each tile include 2 Schottky diodes, 2 user-definable MOS capacitors, 12 diffused resistors, and 13 user-definable, thin-film, silicon-chromium resistors. The array has 48 bonding pads.

To the user, the macros may well

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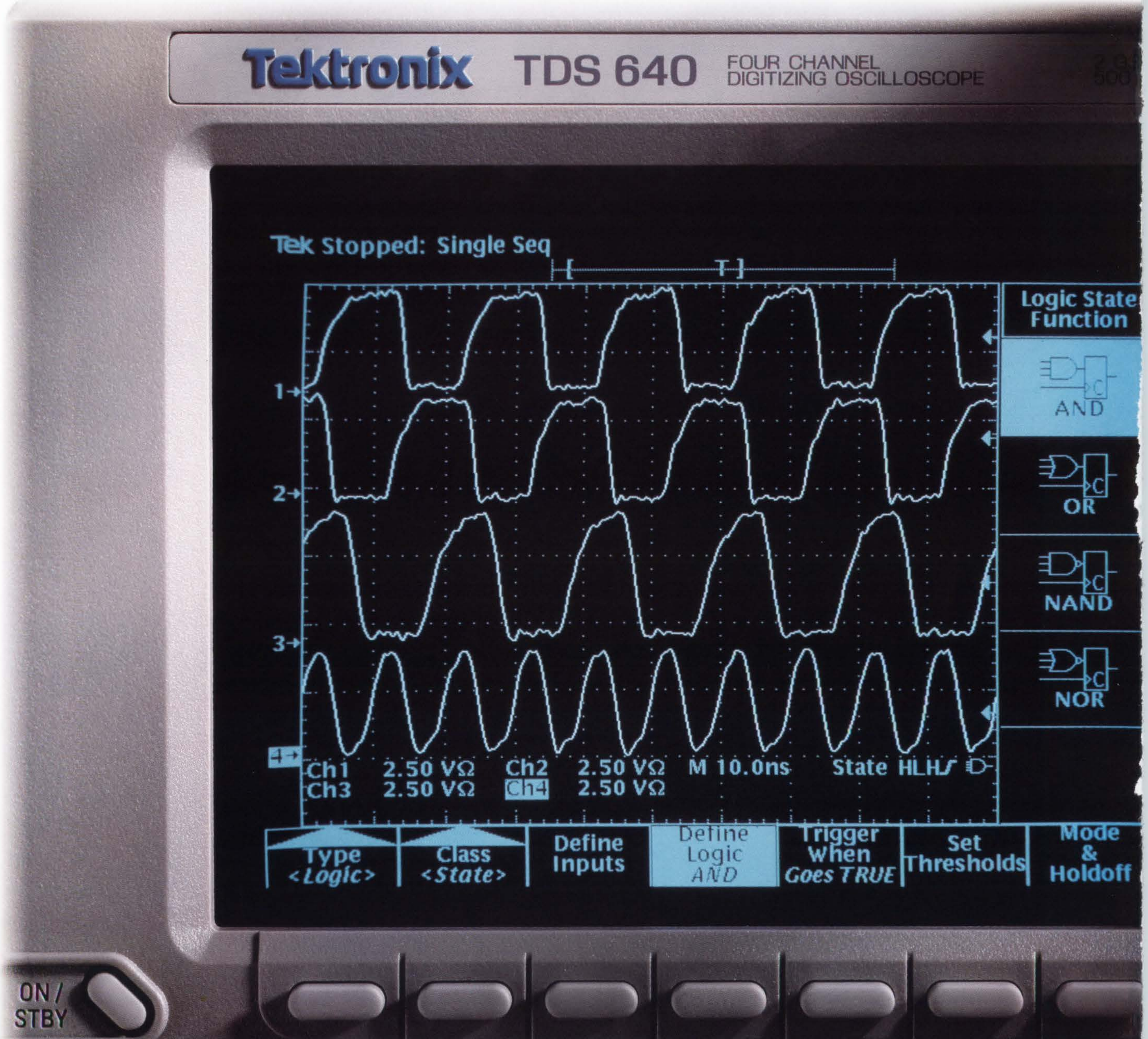

Tektronix TDS 640
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Logic State Function
AND
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Ch1 2.50 VΩ Ch2 2.50 VΩ M 10.0ns State HLH
Ch3 2.50 VΩ Ch4 2.50 VΩ
Type <Logic>
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Define Inputs
Define Logic AND
Trigger When Goes TRUE
Set Thresholds
Mode & Holdoff
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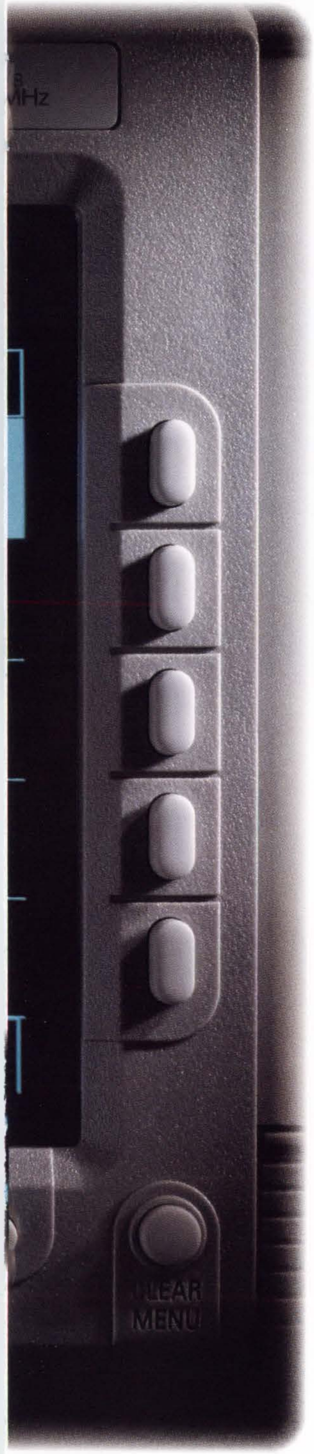

A great face can open a lot of doors. Ours will take you into a world of digital oscilloscope technology that until now has existed only in the maddening pages of some instruction manual. You'll find this face on every TDS scope we make. Intuitive, affordable scopes so easy to use, you'll feel like a digital expert whatever your background. Tektronix. When it comes to digital scopes, we've put on a whole new face. Now all you have to do is get in it.

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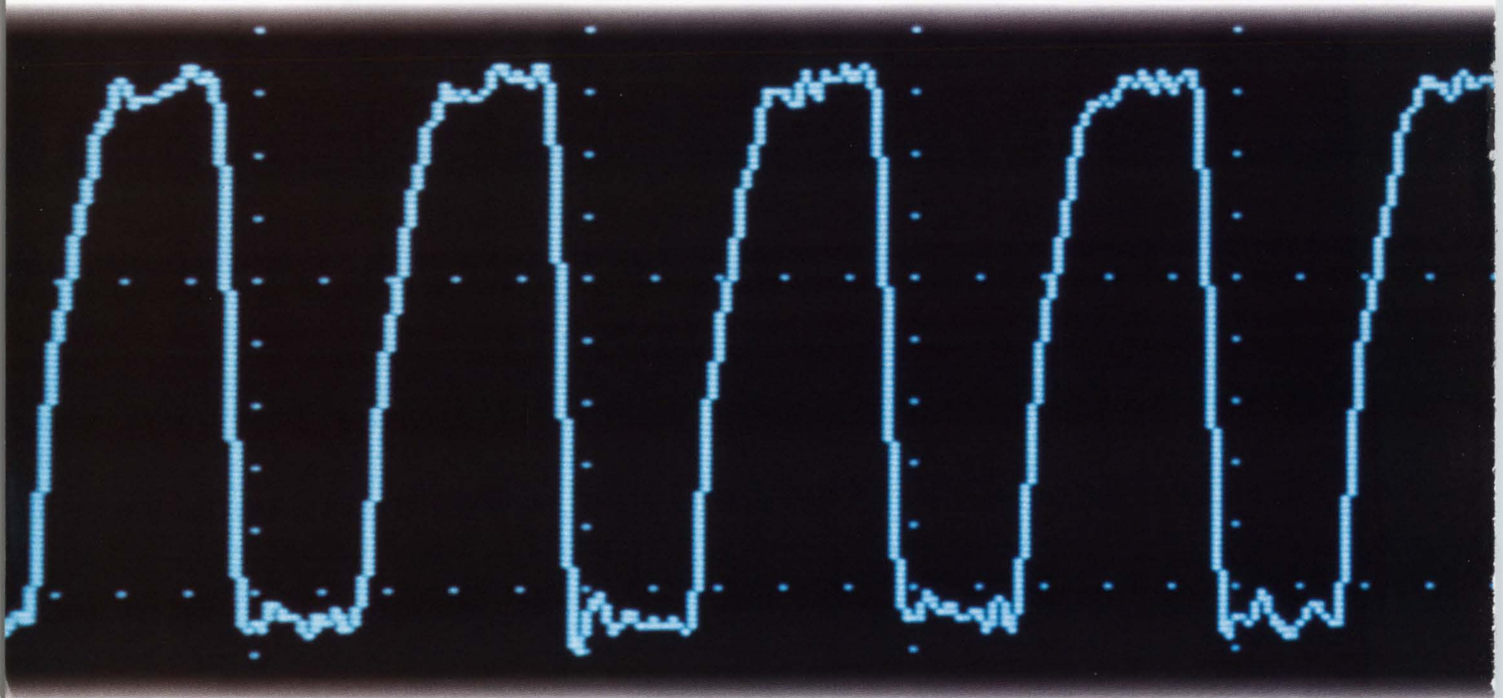
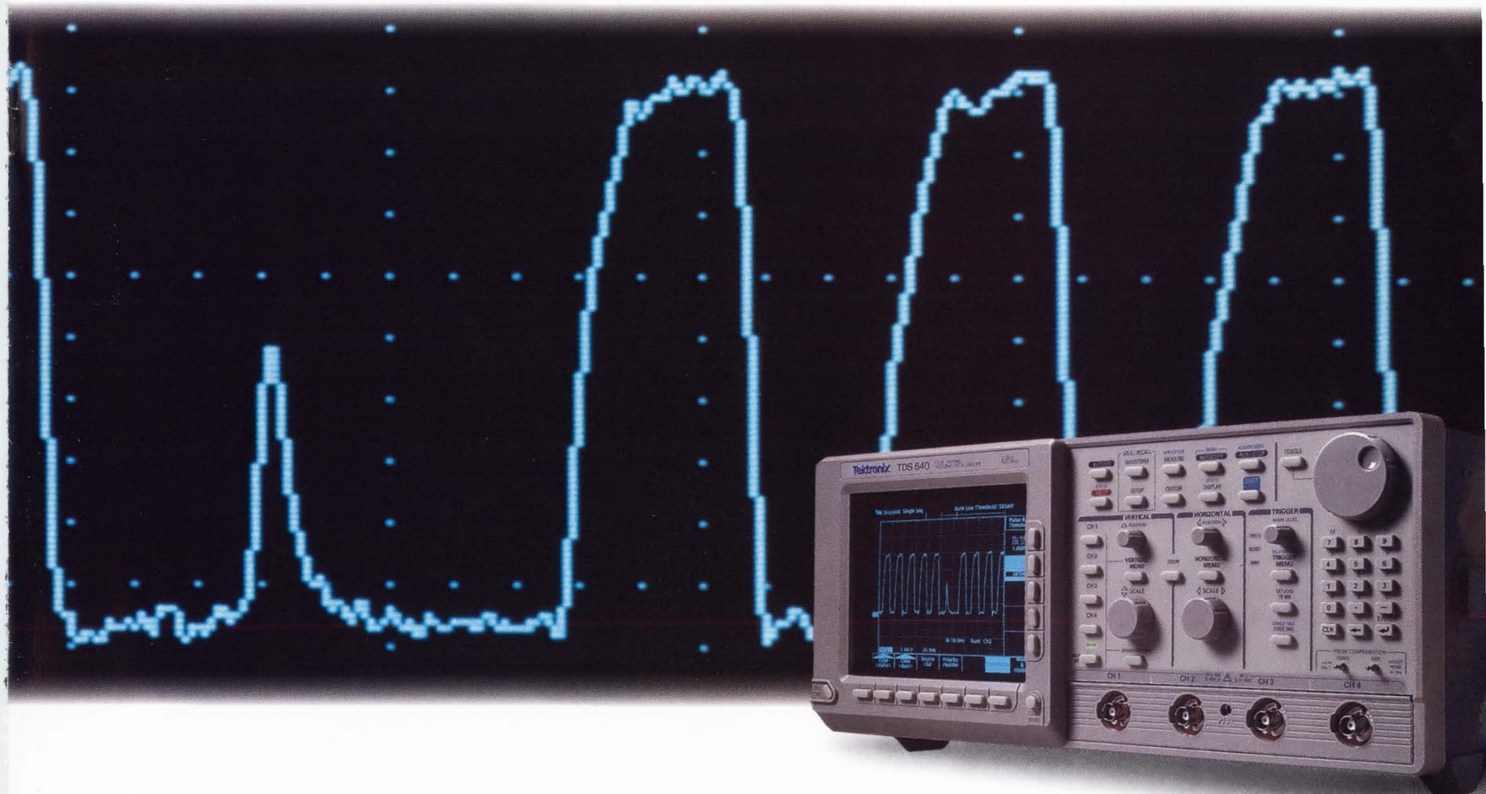
GO AHEAD. PULL THE TRIGGER ON



THE LITTLE RUNT.



Our new TDS 620 and TDS 640 digital oscilloscopes make triggering so easy, it's just like target practice. See, with an extraordinary sampling rate of 2 GS per second on all 4 channels at once, you can get a precisely detailed look at what you're aiming at. And with the ingenious TDS user interface and application-specific icons, you can now quickly access nearly a dozen extended trigger functions, including runt, logic and glitch. Better still, either model is available for a price noticeably lower than any competitive scope. The undeniably accurate, remarkably affordable, intuitively trigger-happy TDS 600 Series digital scopes from Tektronix. Without a doubt, they'll make your day. **TALK TO TEK/1-800-426-2200 EXT. TDS7**

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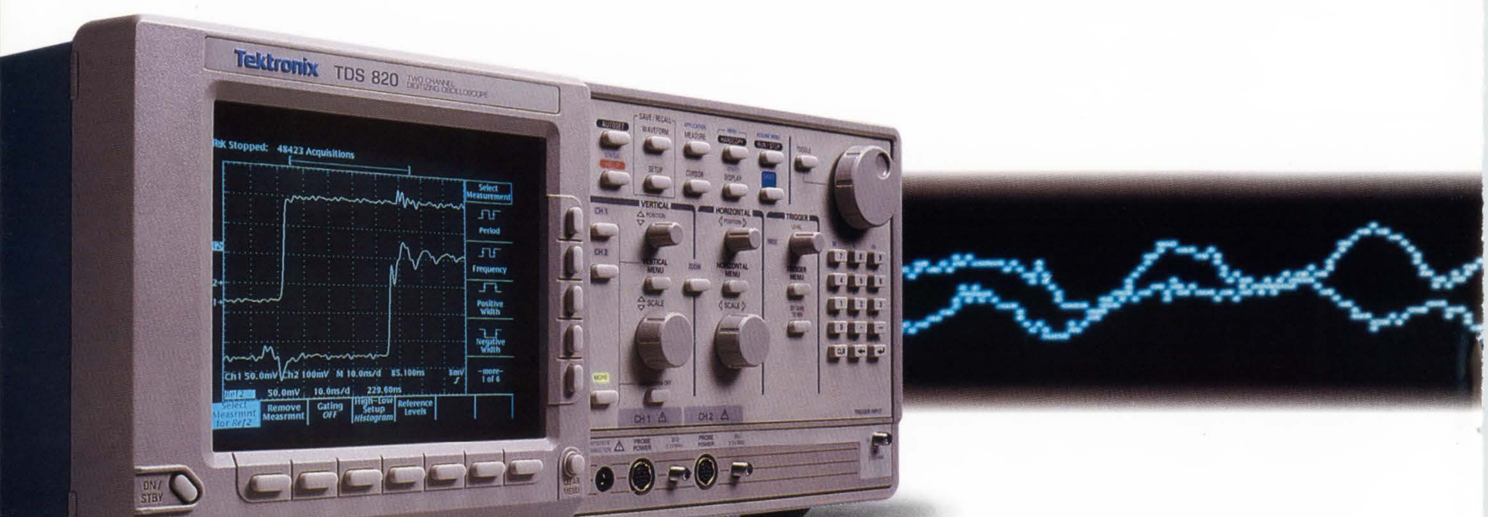

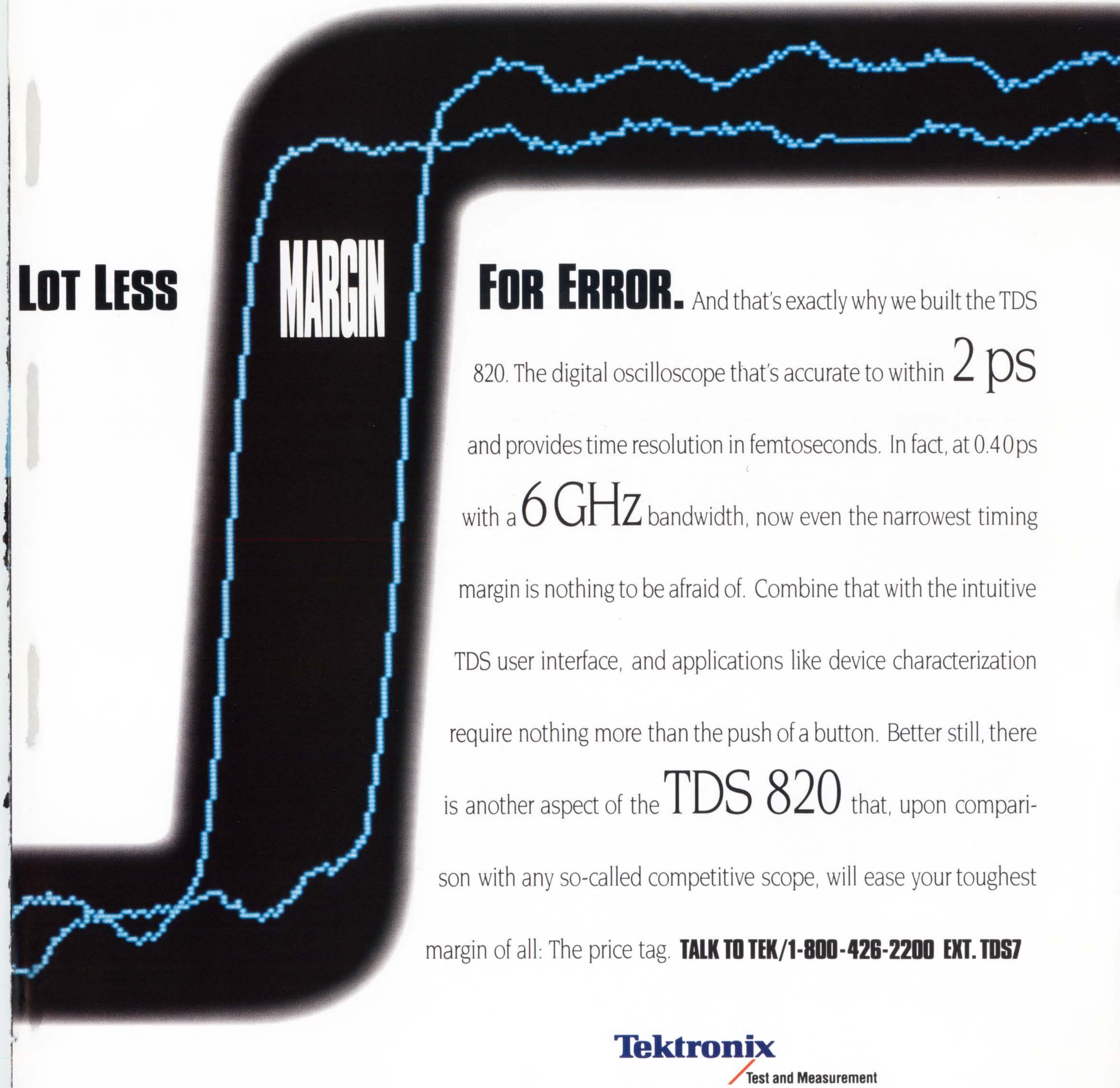
LOT LESS MARGIN FOR ERROR.
And that's exactly why we built the TDS 820. The digital oscilloscope that's accurate to within 2 ps and provides time resolution in femtoseconds. In fact, at 0.40ps with a 6 GHz bandwidth, now even the narrowest timing margin is nothing to be afraid of. Combine that with the intuitive TDS user interface, and applications like device characterization require nothing more than the push of a button. Better still, there is another aspect of the TDS 820 that, upon comparison with any so-called competitive scope, will ease your toughest margin of all: The price tag.
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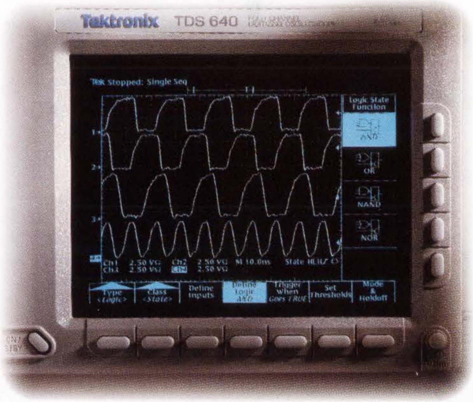
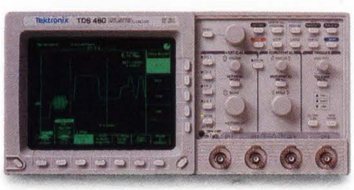


BESIDES EASE OF USE, WE ALSO CONSIDERED SUITABLE FRAMING.

At Tektronix, we designed our TDS Series user interface to be the picture of simplicity. Then, because everybody's needs are different, we framed it seven different ways. For instance, besides the TDS 620, 640 and 820, we also build the TDS 420, 460, 520 and 540.

On the 2 channel TDS 520 and 4 channel 540, you get 500 MHz bandwidth and up to 50k record lengths. A single-channel sampling rate of 1 GS/sec on the TDS 540 and 500 MS/sec on the 520—combined with edge, pattern, state, glitch, runt & pulse width triggering—greatly simplifies debugging and fault isolation. What's more, both feature built-in



FFT analysis. Or, for a more economical solution, take a look at the TDS 420 and TDS 460. First off, they provide up to 350 MHz across 4 channels, at a cost usually found on 2 channel scopes. They provide video triggering, a 30,000 record length, and a sampling rate of 100 MS/sec. And both feature 5 different acquisition modes: sample, peak detect, high-resolution, envelope, and average. All of which you'll find amazingly accessible thanks to the ingenious TDS user interface. The TDS Series of digital oscilloscopes from Tektronix. For more information, don't hesitate. Get in our face. **TALK TO TEK/1-800-426-2200 EXT. TDS7**

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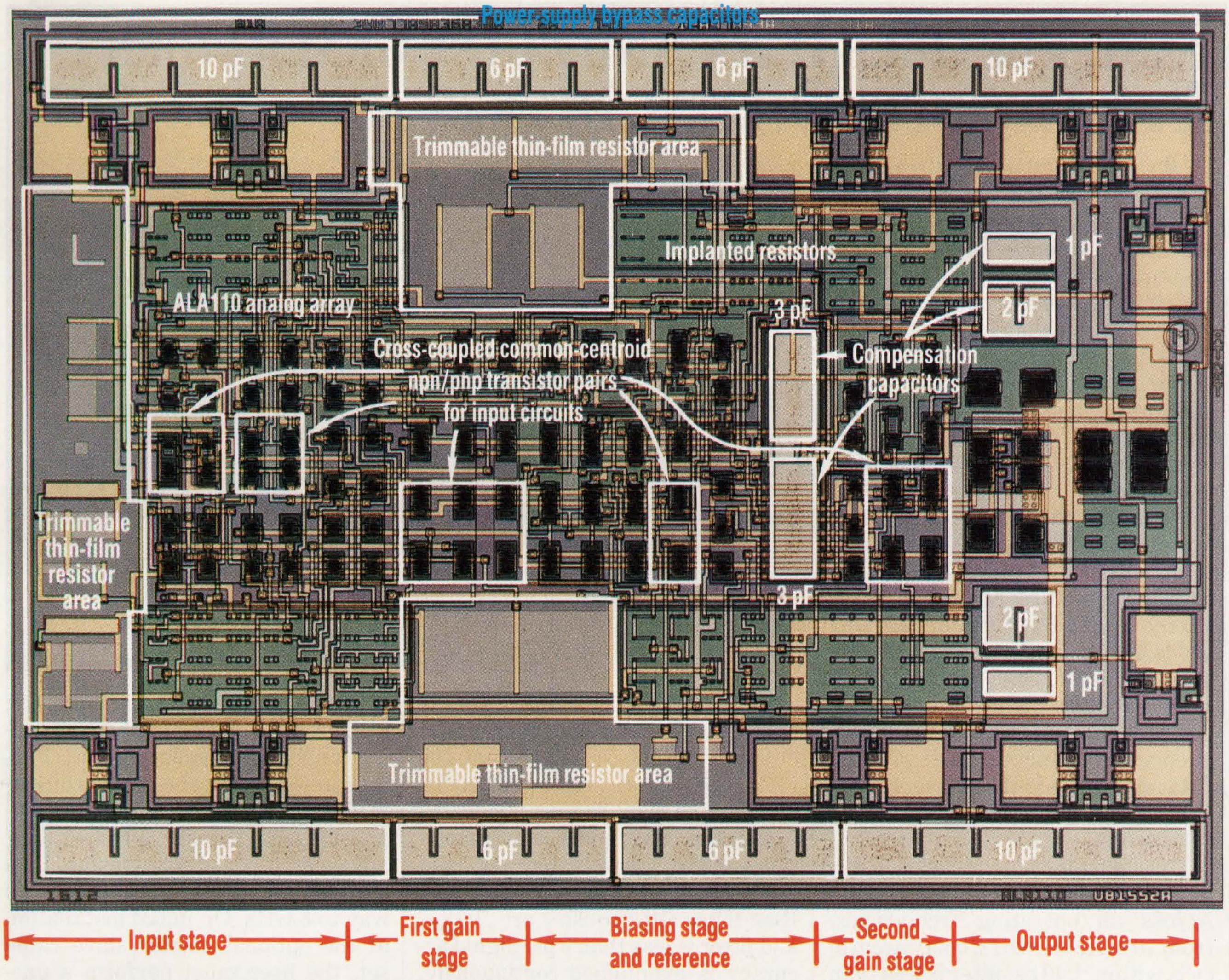
CIRCLE 300

UHF COMPLEMENTARY BIPOLAR ANALOG ARRAYS



2. A SINGLE WIDEBAND/HIGH-SPEED analog circuit, such as a 200-MHz op amp or a 1-ns ECL comparator, can be contained within AT&T's ALA110 analog array. The smaller input-stage transistors are located on the left, increasing in size from left to right.

represent the major features of both the AT&T and Raytheon arrays *(see the table, again)*. One of the most interesting macros is what Raytheon calls an 8-channel multiplexed amplifier with video bandwidth. Functionally an 8-input-to-1-output multiplexer, it consists of eight op amps, each connected to its own input but with a common output. A three-line address input activates one op amp but leaves the outputs of the seven others in a high-impedance state. Unlike conventional CMOS multiplexers, no voltage drop occurs across an input switch (switching between inputs takes 55 ns). The 3-dB full-power bandwidth for a ±3.5-V output is 50 MHz. In the off state, minimum isolation at 1 MHz is 65 dB.

Both AT&T and Raytheon envision the macros as the basis of a standard-cell library to be used for full-custom ICs. To this end, Raytheon is developing a library of ECL cells, as well as a family of video-speed data-acquisition cells. The latter cells include a 10-bit, 40-MHz ADC; a 100-MHz, 8-bit flash ADC; a 12-bit, 25-MHz DAC; and a 12-bit-accurate, 50-ns sampling amplifier.□

PRICE AND AVAILABILITY

Nonrecurring engineering (NRE) cost for ICs built on the AT&T ALA110 array typically runs from $30,000 to $50,000, while NRE charges for a full-custom chip can run to $100,000. Cost of the final ICs can run from as low as $4.00 each to over $40 each, depending on the testing required, volume, specifications, and package.

NRE cost for chips built on Raytheon's PC101 array start at $40,000. Unit price depends on ac and dc test needs, package type, temperature range, and volume. In quantities of 5000, typical ICs from the array (each capable of replacing a pc board) run $25 each.

AT&T Microelectronics, 555 Union Blvd., Dept. 520404200, Allentown, PA 18103; (800) 372-2447; in Canada, (800) 553-2448. **CIRCLE 519**

Raytheon Co., Semiconductor Div., 350 Ellis St., Mountain View, CA 94039-7016; Harry Gill (415) 966-7655. **CIRCLE 520**

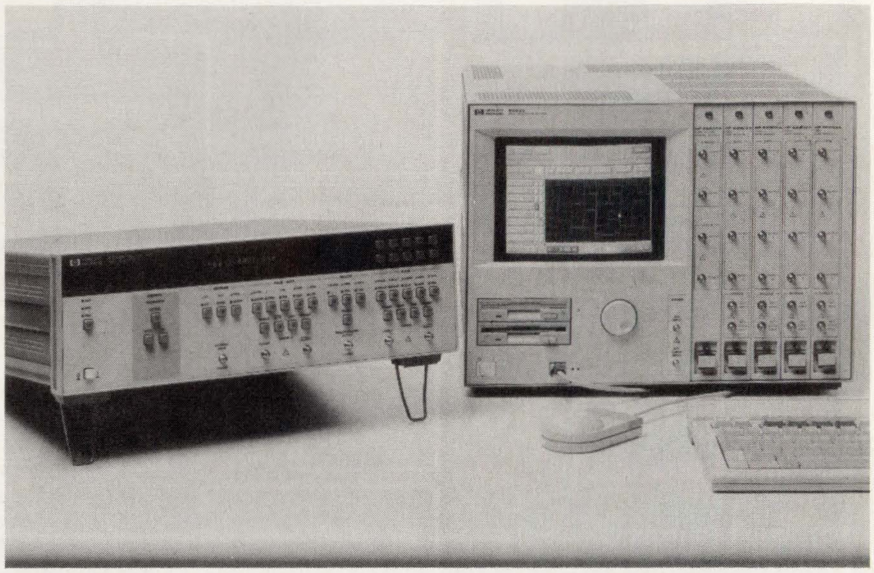
HOW VALUABLE?	CIRCLE
HIGHLY	560
MODERATELY	561
SLIGHTLY	562

FAST, FLEXIBLE DATA AND PULSE GENERATORS TEST ADVANCED DIGITAL DEVICES

JOHN NOVELLINO

As digital circuits grow in speed and complexity, designers must look for faster and more versatile stimulus systems to test those circuits. A pair of stimulus sources from Hewlett-Packard's Boeblingen Instruments Div.—the HP 80000 1-GHz data generator and HP 8133A 3-GHz pulse generator—aim to fill this need for engineers who test high-performance digital ICs, boards, modules, and systems.

The data generator is a modular system that can supply from 4 to 20 channels *(see the figure)*. And an open architecture allows users to easily upgrade the generator as needs change and more modules become available. Data capabilities include a 16-kbit/channel programmable sequence. If required, this sequence can be recycled with random data and a pseudo-random binary sequence (PRBS) for eye-pattern measurements.



The instrument's precision helps minimize measurement uncertainty. Across all operating frequencies, from 10 MHz to 1 GHz, delay accuracy is within ±40 ps, jitter is less than 20 ps, and skew at the device is less than 20 ps. In fact, the HP 80000's output quality is comparable to that of a pulse generator. Transition times (10% to 90%) are less than 200 ps; levels are accurate to 3% and variable to 2.5 V pk-pk into 50 Ω (5 V into an open); and edge placement resolution is 2 ps. Specifications such as those should ensure accurate, repeatable measurements.

The HP 80000 has an intuitive user interface with color pop-up windows that that keep the system setup transparent. Users can choose from a touch screen, a mouse, or a keyboard for making timing adjustments of several nanoseconds or as little as 1 ps. Precise adjustments can also be made quickly using a demand-sensitive knob on the instrument's front panel.

Designers who must make precise parametric measurements on digital devices with clock rates from 100 MHz to 3 GHz will find the HP 8133A ideal for the task. The instrument delivers 1-ps edge-placement resolution, 100-ps timing accuracy, and pulse widths of 150 ps to 10.000 ns. Rise times (10% to 90%) are 100 ps, and jitter is less than 5 ps. Signal accuracy is maintained continuously, even during frequency changes, eliminating the possibility of glitches that would corrupt measurement results.

With a delay range of 10 ns at all operating frequencies, the HP 8133A permits unrestricted timing for tests of high-speed technologies such as CMOS, ECL, and GaAs. In addition, users can choose an optional second pulse channel or an optional second channel that generates either pulse or data. In the data mode, the optional channel offers a return-to-zero or non-return-to-zero format with a 32-bit programmable sequence or a 2^{23} PRBS. This feature lets users perform functional tests, delta-time measurements, laser critical-pattern tests, and eye-diagram tests.

For multiphase clock simulation, users can connect two or three HP 8133As together to create up to six synchronous clock signals. Full timing capability is available on all channels, and phase can be entered directly if required. Users can set up multiphase clock signals incorporating any desired phase relationship. Resolutions of 0.1° are possible all the way to 3 GHz. On initial installation of the optional master/slave cable set, the user must perform a one-time calibration of the multiple instruments using the HP 8133A's deskew capability.

Front panel pushbuttons provide direct access to all of the pulse generator's parameters. The parameters themselves are shown on an alphanumeric display. When needed, the display supplies error messages to tell the user the fastest way to correct any improper settings.

Prices for the HP 80000 data-generator system range from $30,100 for 4 channels to $77,400 for 20 channels. The HP 8133A pulse generator costs from $27,100 to $45,900, depending on configuration. Estimated delivery for both is within 6 weeks after receipt of an order.

Hewlett-Packard Co., 19310 Pruneridge Ave., Cupertino, CA 95014; (800) 752-0900. **CIRCLE 457**

Tool Options Increase For Analog Design On PC And Mac

Intusoft has several new products for analog designers, including a graphical Spice schematic-entry tool for the Macintosh, passive-filter design software, and more than 1000 new Spice models. In addition, the company's newly published reference book, *A Spice Cookbook*, details more than 100 analog simulation examples.

SpiceNet provides graphical schematic entry and editing for engineers working in a Macintosh environment. The resulting net lists are compatible with any Spice program. The SpiceNet program has many features not found in any other schematic-entry packages, such as display of post-processor waveforms and node voltages directly on the schematic and automatic pin placement on subcircuit symbols. SpiceNet is included with the company's ICAPS circuit simulation system.

Another new product, FilterMaster, helps engineers use a DOS-based PC to synthesize low-pass, high-pass, bandpass, and bandstop LC passive filter circuits. Selectable approximations include Butterworth, Chebychev, inverse Chebychev, elliptic, and Bessel. After the final circuit is generated, FilterMaster can analyze and graph the filter's transmission characteristics.

Also, a completely updated version of PreSpice, Intusoft's Spice preprocessing program for the PC and Macintosh computers, now offers more than 1000 Spice models for domestic, European, and hard-to-model components. Many of the models, such as vacuum tubes and fuses, are not commonly available from other Spice vendors. PreSpice is also included with the ICAPS system.

All of Intusoft's new products, including the reference book, are shipping now. Call Charles Hymowitz for information and pricing.

***Intusoft**, P. O. Box 710, San Pedro, CA 90733-0710; (213) 833-0710.*

CIRCLE 459

■ *LISA MALINIAK*

Math Software Quickly Visualizes Scientific Data

Version 4.0 of Matlab combines numeric-computation software with a family of application-specific toolboxes and new graphics capabilities. With one software package, users can analyze and visualize data; prototype, analyze, and optimize engineering system designs and algorithms; create mathematical models and solve systems of equations; and perform general engineering and scientific computations.

Features new to version 4.0 include sparse matrix support to accelerate solving large problems, flexible file I/O for easy data import and export, and debugging tools to ease use of the Matlab fourth-generation programming environment. In addition, sound output provides another method of analyzing data sets, particularly for signal-processing applications.

The time required by math software to compute a solution usually depends on the number of elements in the matrix defining a system. With the sparse-matrix capability in version 4.0, however, computation time is defined by the number of non-zero elements in the matrix, greatly speeding Matlab's performance. Also, Matlab's new graphics capabilities let users more clearly visualize computational results than did previous versions of the product. With the help of rectangular, spherical, and general parametric coordinate systems, users can create color 3D surfaces, mesh plots, contour plots, scatter plots, data trajectories, and images.

Toolboxes extend the Matlab software by adding specialized functions for particular applications, such as filter and control-system design. The toolboxes are created by experts in their respective fields.

Matlab version 4.0 will ship by the end of this quarter. It will initially run under X Windows on DEC, HP, IBM, Silicon Graphics, and Sun workstations. In addition, Matlab can be networked in heterogeneous environments. Pricing is set at $2995 for a single-user version. Network licensing and quantity and educational discounts are available.

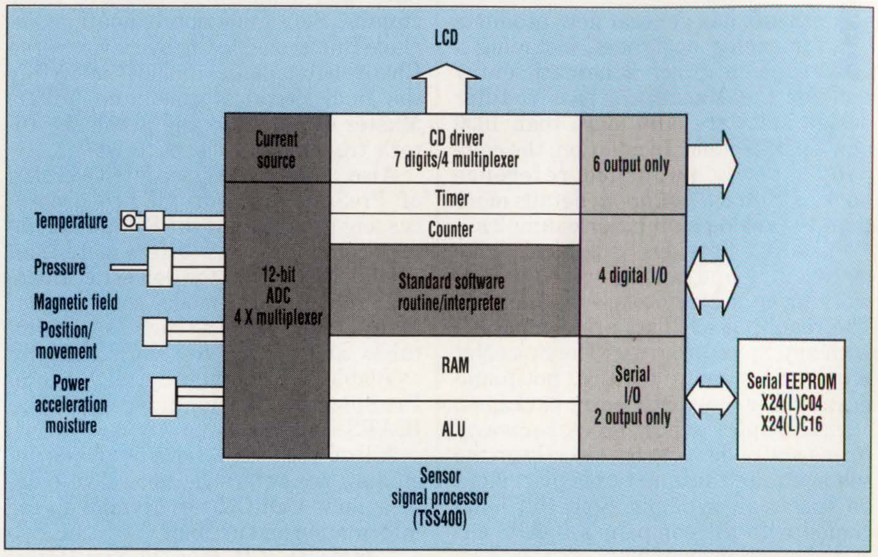
***The MathWorks Inc.**, Cochituate Pl., 24 Prime Park Way, Natick, MA 01760; (508) 653-1415.* **CIRCLE 460**

■ *LISA MALINIAK*

IC Selects Sensor, Digitizes Output, Processes Results, Feeds Display

Frank Goodenough

Now a designer can have one IC designed to select, condition, digitize, and process/calibrate signals from up to four sensors and feed the results directly to an LCD display. The results can also be sent to a host processor via a serial I/O port. From Texas Instruments and called the TSS400, this CMOS IC not only contains a multiplexer, 12-bit ADC, and 7-digit display driver, but an ALU and memory too.



Aimed at processor-controlled sensor-based systems, from portable instruments to autos, the chip consumes little power while it monitors and processes signals from sensors such as those for temperature, pressure, position, motion, and acceleration. Other applications include monitoring currents in battery-powered PCs, climate control systems, security systems and energy management. The 44-pin PLCC can easily replace a handful of parts in a portable-PC system.

The TSS400's front end consists of a four-channel multiplexer, a 12-bit successive approximation ADC, and a current source for exciting resistance sensors such as RTDs (resistance-temperature detectors) and strain gages for operation in a ratiometric mode. Althogh conversion time runs a slow 375 μs, the chip is designed to sense phenomona that are also slow to change—temperature, for example. A 4-bit microcomputer on the chip controls the ADC and performs computations on the digitized inputs. The microcomputer also implements DSP, control, and communication functions.

The chip stores sensor-specific data such as calculated values, or sensor calibration factors, in the on-chip 576-bit RAM. A 32.768 kHz, real-time crystal clock keeps time while an 8-bit parallel output and 4-bit parallel I/O simplify interfacing with switches and relays.

Designed for battery power, the TSS400 works off 3-V lithium cells, and even on voltages down to 2.6 V. Since only a few applications require the chip to be active all the time, it operates in one of four modes to conserve power: done (standby), off, active, and conversion. When put in the done mode, the chip switches off all processor components except the LCD driver, the timer, and RAM. Current drain typically runs just 6 μA. In the off mode the chip's CPU is completely disconnected but the RAM's contents and the digital latch remain unchanged. Current drain is now a mere 100 nA. When in the active mode the chip is functioning but without the ADC, and current drain typically rises to 140 μA.

In the conversion mode the device is fully functional, including the a-d converter. Now current drain climbs to 800 μA. Because in most applications the chip waits in the off mode more than 99% of the time, battery life amounts nearly to its shelflife. The TSS400 comes in three versions: the standard version—the TSS400-S230; and two mask-programmable versions—the TSS400 and the TSS400/4. The two mask- programmable versions are available with 2k and 4k of ROM, respectively.

Without a set of development tools, the TSS400 would be virtually worthless to a system designer. Anticipating this problem, TI has made available the SDT400 Development Kit for the standard version. It consists of a software simulator and a development board. The simulator can run on an IBM-AT compatible PC and permits debugging at the macro instruction level, together with screen simulation of the LCD. The SDT Development Kit goes for $1,295 each.

For the mask-programmable versions of the TSS400 the company designed the PC-based ADT400 Development System. It emulates all functions of the device under real-time conditions.

The TSS400 with a 576-bit RAM (9 pages of 16 by 4 bits) and 2048 instructions in internal ROM comes in 28-pin and 40-pin DIPs depending on digital I/O as well as the 44-pin PLCC. The TSS400/4 with a 960-bit RAM (15 pages of 16 by 4 bits) comes in a similar choice of packages. The standard TSS400-S230 comes only in the 44-pin PLCC. In quantities of 100 the standard TSS400-S230 goes for $14.95 each.

Texas Instruments Inc., Semiconductor Group (SC-91080), P. O. Box 809066, Dallas, TX 75380-9066; (800) 336-5236, ext. 700. **CIRCLE 458**

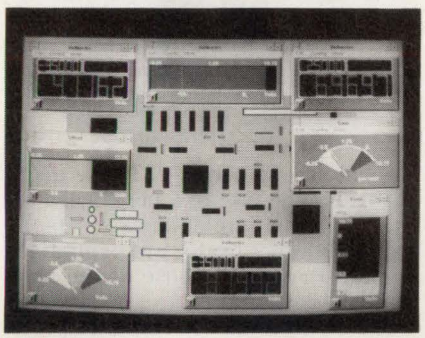
SOFTWARE UPGRADE HAS OFF-LINE MAIL READER

Qmodem version 5, available at retail for the first time, improves on previous versions with the addition of an off-line mail reader. With the off-line feature, users can download packets of mail from a bulletin-board system and read the contents off-line. As a result, users can review and reply to mail without incurring expensive long-distance call charges. Users also can create reply packets to upload. The program is preconfigured for at least 90 modems. List price is $99, with a $35 price to current Qmodem users and system operators using Wildcat BBS software.

Mustang Software Inc., P. O. Box 2264, Bakersfield, CA 93303; (805) 395-0223; fax (805) 395-0713.

CIRCLE 461

METER SOFTWARE RUNS UNDER WINDOWS

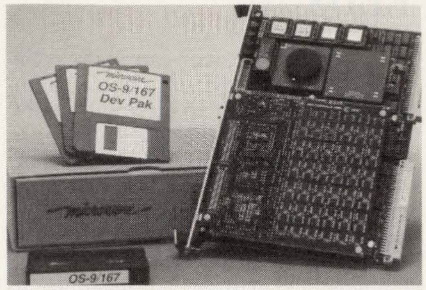


PCImeter, a graphic meter software package for Windows 3.0, displays analog input data as digital and analog meters and bar graphs. Process values can be modified to engineering units using scaling factors, and linearization for thermocouples is also supported. Meters can be saved to PCI meter application files and can be reconfigured at any time. Up to 16 meters can run simultaneously. By means of dynamic data exchange (DDE), PCImeter can also export data to Excel spreadsheets for analysis and report generation. The software runs on IBM PC/AT compatible and EISA personal computers with a hard disk and a 5.25-in. or 3.5-in. floppy drive. List price is $95. A free demo disk comes in 5.25- and 3.5-in. formats. The software also is included free with a purchase of a PCI-20098C Series Multifunction Board from Intelligent Instrumentation/Burr-Brown for U. S. orders placed until March 31, 1992.

Intelligent Instrumentation, 1141 W. Grant Rd., MS 131, Tucson, AZ 85705; (602) 623-9801 or fax 623-8965.

CIRCLE 462

OS-9 REAL-TIME OS COMES TO MOTOROLA SBCS



An optimized version of the OS-9 real-time operating system is being offered for the Motorola MVME167 single-board computer. This latest version of OS-9 for Motorola microprocessor-based products enables designers to take advantage of the 32-bit 68040 processor while providing support for on-board serial, SCSI, and Ethernet hardware. The OS-9 Development Pack includes new OS-9 device drivers for next-generation I/O peripherals included on the MVME167 board family. Tools include a C compiler, macro assembler and linker, user state debugger, shell-command interpreter, and utilities. The development pack, including RTOS modules, device drivers, and development tools, sells for $3,000. The run-time pack provides only the OS modules and costs $1,500. Both the development and the run-time packages are available now. Contact the company for information on licensing multiple copies.

Microware Systems Corp., 1900 N.W. 114th St., Des Moines, Iowa (515) 224-1929; fax (515) 224-1352. **CIRCLE 463**

GUI TOOL WORKS WITH C++ APPLICATIONS

The latest version of Telesoft's development tool for graphical user interfaces offers the ability to develop GUIs for C++ applications. TeleUSE version 2.0.5 runs on Silicon Graphics IRIS-4D workstations and NCR System 3000 under Unix SVR4. The updated version generates ANSI-compatible C source code, provides a new color Pixmap Editor, and supports X Windows on Sparc platforms. Version 2.0.5 also supports OSF/Motif version 1.1.4. TeleUSE version 2.0.5 is available now for most platforms. A single license is $7,500, with multiple discounts available. TeleUSE includes a license for OSF/Motif version 1.1.4 and X11 client libraries.

Telesoft, 5959 Cornerstone Court West, San Diego, CA 92121; (619) 457-2700. **CIRCLE 464**

Transceiver Chip Covers T1 and ISDN PRI Speeds

A transceiver for ISDN and T1 applications from Level One Communications needs only external line-coupling transformers and a few passive components to operate over 6000 ft of twisted-pair cable. The transceiver complies with industry specifications, including AT&T Pub 62411, ANSI T1.403 and T1.408, and FCC part 68. Using on-chip adaptive-equalizer elements, the LXT310 can operate over 36 dB of pole-mounted or buried twisted-pair cable at the T1 primary rate by sampling the input pulses and automatically adjusting the equalizer transfer function.

To compensate for shorter lines, the device supplies 7.5, 15, and 22.5 dB of frequency-dependent transmit-line build-outs. Jitter attenuation is selectable in the transmitter or receiver data path. Receiver sensitivity is also selectable. The transceiver can restore the received signal after transmission through cable with an attenuation of 0 to 26 dB or 0 to 36 dB at 772 kHz.

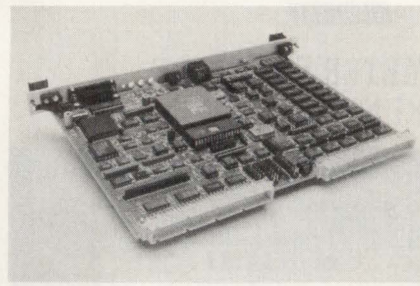
Diagnostic features include a loss-of-signal indicator and local/remote loopbacks enabled by direct control or in-band loopback-code detection. Supplying timing recovery and control, the chip works in channel service-unit network interfaces, DS1 metallic interfaces, T1/LAN bridges, T1 multiplexers, and digital loop carriers. The LXT310 operates from –40 to +85°C and runs on a single 5-V supply. The 28-pin PLCC, ceramic DIP, and plastic DIP packages are $31, $33, and $30 each, respectively, in thousands.

***Level One Communications Inc.**, 105 Lake Forest Way, Folsom, CA 95630; Lon Cantor, (916) 985-3670.* **CIRCLE 465**

■ *MILT LEONARD*

Ethernet Multiplexer Offloads TCP/IP Control

By placing a lot of intelligence on a 6U VME card, the Etherplex multiplexer unburdens the host computer system from handling interrrupts and contact switching in TCP/IP and Telenet processing. The RISC-based card from Systech makes possible systems that support, for example, 80 users. The multiplexer card maintains output of nearly 4000 charac-



ters per second per user. That's about quadruple the rate of a host-based Telenet handler implementation (software only). Input rates are maintained at more than twice those of the host-based implementation.

The board combines standard protocol handling by a 32-bit Ethernet controller and a 960CA RISC processor with a multiplexer-like host interface. That merger was made possible, in part, by the company's terminal control software (TCS), which was originally developed for the firm's Unplug terminal I/O subsystems.

The TCS software implements statistical multiplexing and a very flexible interface that allows the host to transfer most of the terminal processing to the dedicated hardware subsystem. As a result, the Etherplex board appears to the host as a single, multi-line asynchronous multiplexer, while the networked terminal servers see the Etherplex card as a host serving standard Telenet terminal devices.

The board can employ either standard, thin, or twisted-pair Ethernet interfaces by selecting the desired transceiver interface. Single unit price of the card is $3995. Delivery is from stock.

***Systech Corp.**, 6465 Nancy Ridge Dr., San Diego, CA 92121; Charles Citron, (619) 453-7400* **CIRCLE 466**

■ *DAVE BURSKY*

Digital-Audio System Works With Sun VMEbus Workstations

The fundamental problem associated with digital audio—the analog-to-digital and digital-to-analog conversions—are solved by the Multi-rate Digital Audio System. The system lets DAT decks and CD players operate with any Sun workstation that supports the VMEbus and SunOS. Sample frequencies are software selectable. All filtering and sample frequency conversions are performed on DSP hardware, not the Sun workstation.

The system can take on digital audio applications such as speech research, audio data acquisition, vibration and noise analysis, and acoustic-research analysis.

The system consists of software and a Banshee/VMEbus system board, a digital-audio interface board, and a digital-audio device. The system board supplies the data buffering, sample-rate conversions, digital antialiasing filters, and control of the interface board. It takes up one slot in the VMEbus backplane. The interface board connects to the digital-audio device and supports fast block transfers of data.

Digital-audio devices typically operate at sampling rates of 32, 44.1, and 48 kHz. The Multi-rate Digital Audio System lets the Sun application software use two channels of bidirectional I/O to and from the digital audio device at sampling rates of 8, 10, 16, 20, 32, 44.1, and 48 kHz. A second set of filters allows transition-band aliasing, but prohibits passband aliasing. The digital-audio system sells for $11,950.

Atlanta Signal Processors Inc., 770 Spring St., Atlanta, GA 30308; (404) 892-7265. **CIRCLE 467**

■ RICHARD NASS

AutoCAD Accelerator Card Takes Speed Crown

With a drawing speed of 132 Mpixels/s the XHR Gemini20 graphics card claims it delivers the fastest response for AutoCAD applications to date. Based on a 32-MHz version of the Texas Instruments TMS34020 graphics processor and a companion 34082 math coprocessor, the AT-bus compatible card can tackle complex graphics applications such as shading or 3D image manipulation. The card includes 2 Mbytes of high-speed video RAM and can display images with pixel counts from 1024-by-768 to 1600-by-1200 with either 16 or 256 colors. The controller card also includes a digital-loop-through mode for VGA-compatible images. The company includes an AutoCAD driver that offers productivity-enhancing features such as user-definable menu buttons, a fixed magnifying glass, customized panning and zooming, and pop-up menus. Price for the card starts at $2450 (single-unit purchases).

ELSA America Inc., 40 Oyster Point Blvd., South San Francisco, CA 94080; Walter Haefeker, (415) 588-6285. **CIRCLE 468**

Host Adapters Offer Independent Channels

Two VMEbus SCSI-II host bus adapters include independent channels and are software compatible with existing members of the Rimfire 3500 family. The 9U RF3590 and 6U RF3870 feature form factors that plug into workstations without adapters. Designed with a low transaction overhead, the two adapters support 10-Mbyte/s synchronous SCSI-II transfer rates with such peripherals as magnetic and optical disks, CD-ROM, tape drives, and DAT. The two boards support Fast SCSI-II mandatory commands, command sets, and command queuing. Single-ended and differential SCSI are also supported. The boards sell for $3050.

Ciprico Inc., 2955 Xenium Lane, Plymouth, MN 55441; (612) 559-2034. **CIRCLE 469**

VME-Slot Load Board Eases System Modeling

Complete, accurate test simulations of power, bused signal-interface loading, and thermal loads of active VME boards in a system are made possible by passive and active versions of a VME-slot load board. The boards are plugged into systems to enable easy and reliable validation, burn-in, or system-level design without exposing costly VME boards to possible damage during testing. The boards feature a front panel with a dedicated LED and voltage test point for each backplane power pin. Call for pricing and delivery.

Dawn VME Products, 47073 Warm Springs Blvd., Fremont, CA 94539; (800) 258-3296. **CIRCLE 470**

LASER PRINTERS GET IPDS COMPATIBILITY

By incorporating the AT05 and AT06 IPDS laser-printer controllers, users can get intelligent printer data stream (IPDS) compatibility on their non-impact printers. IPDS is the host-to-printer page description protocol for Advanced Printing Function, the printing management component of IBM's System Application Architecture. The AT05 equips printers with several IBM laser-printer emulations, including the Model 3825 with channel interface and the models 3812, 3816, and 4028 that contain coaxial or twinaxial interfaces. The AT06 offers emulation for the models 3825, 3827, 3835, and 3900. The AT05 comes in two versions—the AT05N is for printers rated at 15 to 25 pages/min. (ppm) and the AT05B is for 20- to 40-ppm printers. The AT06 is based on a multiboard architecture. It can be configured with three to eight boards connected through a SCSI bus. This lets the AT06 handle printers up to 300 ppm.

MPI Technologies Inc., 4952 Warner Ave., Suite 301, Huntington Beach, CA 92649; (714) 840-8077. **CIRCLE 471**

LASER PRINTER SENDS POSTSCRIPT FAXES

Laser printers are currently being implemented as facsimile machines but with limited resolutions. An option for the NEC Silentwriter Model 95 laser printer lets users send resolution-independent faxes and receive them in PostScript through the printer. The Silentwriter 95 can be used with a Macintosh, PC, or standalone fax machine. The fax option operates at speeds of 2400, 4800, 7200, and 9600 bits/s. The option sells for $599.

NEC Technologies Inc., 1414 Massachusetts Ave., Boxborough, MA 01719; (508) 264-8000. **CIRCLE 472**

HANG MAC-COMPATIBLE DISPLAY ON THE WALL

The RDI Profile MC is a "convertible" computer that's compatible with all Apple Macintosh applications. It's convertible because the display can remain connected to the system, as in a desktop, or it can be removed and hung on a wall for easier viewing. The display housing contains all the processing circuitry. As a result, when the display is hung, all that remains on the desktop is the keyboard. The 15-lb. unit is built with a Macintosh LC motherboard and operates at 15.67 MHz. It comes with a 120-Mbyte hard drive, a 3.5-in floppy drive, and 4 Mbytes of RAM, expandable to 10 Mbytes. Available in April, the system sells for $7995. A Sun-compatible system was released near the end of last year and a PC-compatible product should be released later this year.

RDI Computer Corp., 6815 Flanders Dr., Suite 160, San Diego, CA 92121; (619) 558-6985. **CIRCLE 473**

HARD DRIVE OFFERS 1-MS SEEK TIME

The DSP3105 3-1/2-in. hard drive has a formatted capacity of 1.05 Gbytes, a 512-kbyte cache buffer, and an average seek time of 9.5 ms. The drive's 1-ms track-to-track seek time is the fastest yet, the company says. These features suit the drive for such applications as networked file servers, multimedia computing, and three-dimensional color graphics.

Advanced data-integrity features are built into the drive, including a 264-bit Reed-Solomon error-correction code, end-to-end check-sum error-detection code, parity on the RAM cache, and multiple copies of each header field. The drive comes with a SCSI-II interface. Its MTBF is rated at 250,000 hours. Available now, the drive sells for $1925.

Digital Equipment Corp., 334 South St., Shrewsbury, MA 01545; (508) 841-6544. **CIRCLE 474**

COLOR PORTABLE WEIGHS JUST 12 LBS.

The T6400 portable computer combines all the features of a full-function desktop system with the benefits of portability. The 12-lb. unit incorporates an active-matrix thin-film transistor Super VGA color display that measures 10.4 in. diagonally. Users have a choice of either a 25-MHz 486SX or a 33-MHz 486DX processor and a 120- or 200-Mbyte hard drive. The system comes standard with 4 Mbytes of RAM, a 3.5-in. floppy drive, two PCMCIA-compatible memory-card slots, a full-size 16-bit expansion slot, an internal dedicated modem slot, and a detachable keyboard. A gray-scale gas-plasma VGA display is also available.

Toshiba America Information Systems Inc., 9740 Irvine Blvd., Irvine, CA 92718; (800) 334-3445. **CIRCLE 475**

FLASH MEMORY PACKS 4 MBITS IN 32 SECTORS

By allowing the selective erasure and rewriting of one or more 16-kbyte blocks, the Hitachi HN28F4000 becomes the first 4-Mbit flash-memory chip to afford small-block updating. The memory, organized as 512 kwords by 8 bits, can also simultaneously erase multiple blocks or the entire chip. Furthermore, users can select whether the chip performs the erase and write operations under host processor control or by built-in automatic sequences.

In the manual mode the host first checks the flash chip to see if it has been erased; if it hasn't, the host must pre-write and erase the memory, and verify the erasure by rereading each byte. The automatic commands free the host from all that overhead. Those commands also eliminate about 100 lines of code plus at least 1 million reads and 512,000 potential writes.

In the automatic mode, the host sends a command and waits for a bit to come back to confirm the memory's status. When the memory chip receives a command from the host, it pre-writes, erases, and verifies itself through status polling and/or data polling.

In portable computers and memory-card storage, the memory has an endurance of 10,000 erase/write cycles. Chip erase time is about 1 second while programming takes place at about 60 μs/byte. Users can get versions with 120-, 150- or 200-ns read-access times with an active current as low as 30 mA and just 20 μA on standby. The chip comes in an 8-by-20-mm, thin, small-outline type 1 package (TSOP) as well as standard 32-lead DIP and SO packages. The 150-ns version sells for $49 in thousands. Samples are available now.

***Hitachi America Ltd.**, Semiconductor and IC Div., 2000 Sierra Point Parkway, Brisbane, CA 94005-1819; Ken Pope, (415) 589-8300.* **CIRCLE 476**

■ *DAVE BURSKY*

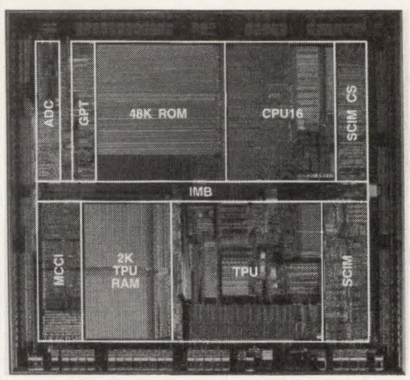
MEGABIT VIDEO DRAM PACKS MILITARY SPECS

Organized as 256-kwords by 4-bits, the MVM4259 video DRAM comes in versions for military, industrial, and commercial applications. Access times for the 28-pin military versions of the chips range from 100 to 120 ns on the DRAM port and 25 to 30 ns for the video port. The chips can be had in any of three package options—a 0.4-in. ceramic LCC (WX suffix), a 0.4-in-wide ceramic DIP (K suffix), and the company's proprietary vertical-in-line ceramic package (V suffix) that requires just a 0.1-in.-wide slice of board space. The military-grade hermetically sealed versions of the VRAMs, processed to Mil-Std-883 Level B Rev. C, sell for $195, $180, and $185 apiece, respectively, in lots of 100. Production quantities will be ready 12 to 14 weeks after ordering.

Mosaic Semiconductor Inc., 7440 Carroll Rd., San Diego, CA 92121; John Guerrero: (619) 271-4564. **CIRCLE 477**

16-BIT MICROCONTROLLER PACKS 48 KBYTES OF ROM

Combining a complex timing control block and 48 kbytes of on-chip ROM, the 68HC16Y1 16-bit microcontroller handles complex timing applications. Motorola has also reduced the price of



its previously released 68HC16Z1. Similar in design to the Z1, the Y1 16-bit CPU core is an extension of the CPU in the popular 68HC11 series controller. The timer block provides up to 16 timing channels that can autonomously handle complex time-critical tasks without assistance from the CPU. Operating from a 16.78-MHz clock, the chip packs 2 kbytes of standby RAM, 48 kbytes of ROM, an eight-channel 10-bit a-d converter, two asynchronous serial ports, and a synchronous serial peripheral. Samples of the Y1 will sell for $38.69 in small quantities, while the older Z1 in its 132-lead PQFP sells for $20.67 in sample quantities.

Motorola Inc., Microprocessor and Memory Technologies Group, 6501 William Cannon Dr. W, Austin, TX 78735-8598; (512) 891-2140. **CIRCLE 478**

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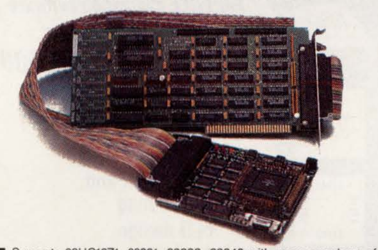

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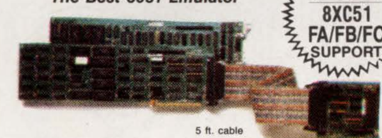

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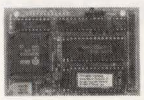

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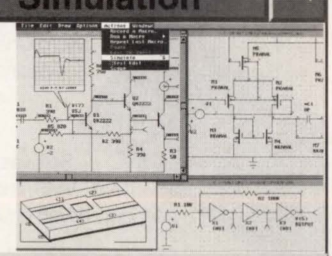

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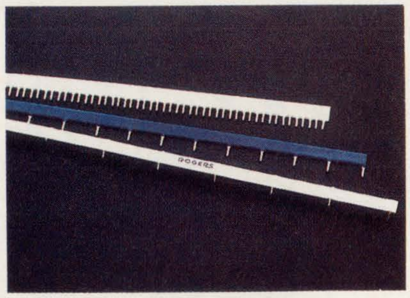

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May 28	5/1/92
June 11	5/15/92
June 25	5/29/92
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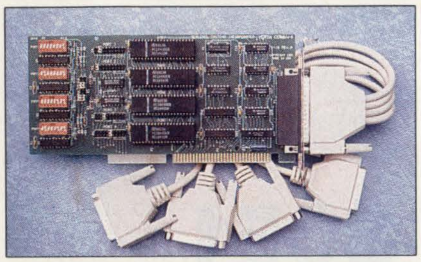

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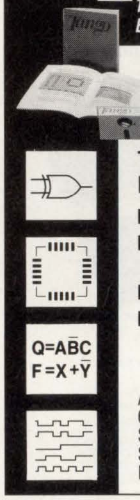

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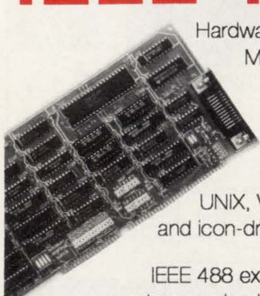

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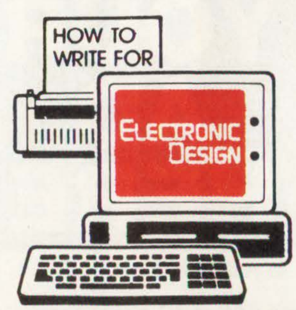

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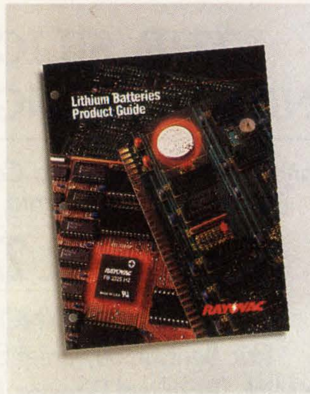

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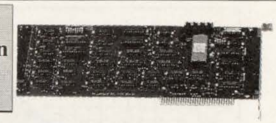

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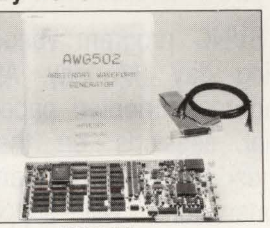

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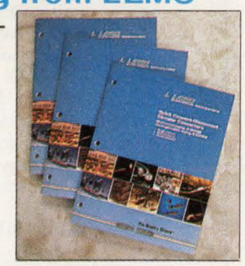

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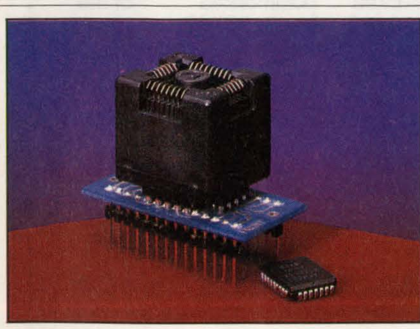

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The SVNC program venue consists of three full-day tutorials on the opening day (Monday, April 27) and more than 70 technical and management-oriented paper and panel presentations arranged in three parallel sessions on the second and third days (Tuesday and Wednesday, April 28 and 29). Table-top product exhibits and demonstrations will supplement the technical paper program on Tuesday and Wednesday. Limited exhibit space is still available; contact Ken Majithia at SysTech Research - (408) 924-3930 - for exhibition details.

The Silicon Valley Networking Conference is a creation of SysTech Research. SVNC is co-sponsored by 3Com Corp., National Semiconductor Corp., and Electronic Design and Electronics Magazines (Penton Publications).

SVNC'92 TECHNICAL PROGRAM OVERVIEW*

Monday, April 27

Tutorial Subjects
(full day seminars)

(T1) FDDI

(T2) INTERNETWORKING

(T3) NETWORK MANAGEMENT

Tuesday, April 28

Keynote Presentation
(morning subjects)
FDDI
Distributed Systems
LAN Foundations
Future Technology Issues
Panel: Technology's Impact on Networking

PRODUCT EXHIBITS** & Lunch

(afternoon subjects)
Internetworking
ISDN and SONET Design
Distributed Systems
LAN Applications and Protocols
LAN Technology Issues
Network Implementation Approaches
Panel: Implementation Issues

PRODUCT EXHIBITS**

Wednesday, April 29

Keynote Presentation
(morning subjects)
Physical Layer Design
Network Management
Internetworking
Wide-Area Networking
Panel: Internetworking Issues

PRODUCT EXHIBITS** & Lunch

(afternoon subjects)
Physical Layer Design
New Architectures and Functions
High-Speed Networking
Network Implementation Approaches
Panel: Wrap-up of All Issues

* tentative; subject to change

*** Product exhibits are open from Noon to 2 pm and from 5:30 to 7:30 pm on Tuesday, April 28, and from Noon to 2 pm on Wednesday, April 29.*

Note: Registration fees for the conference include coffee-break refreshments, lunch, one set of tutorial notes and/or conference proceedings, and one exhibits admission. A $100 handling fee will be charged for registrations cancelled before March 30, 1992; no refunds after March 30.

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(A) Tutorial only (one tutorial on 4/27) Select one: T1 --- T2 --- T3	$250	$295	$350
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(C) Full conference (includes 1 tutorial, all papers and exhibits); mark tutorial in (A). . .	$450	$495	$550
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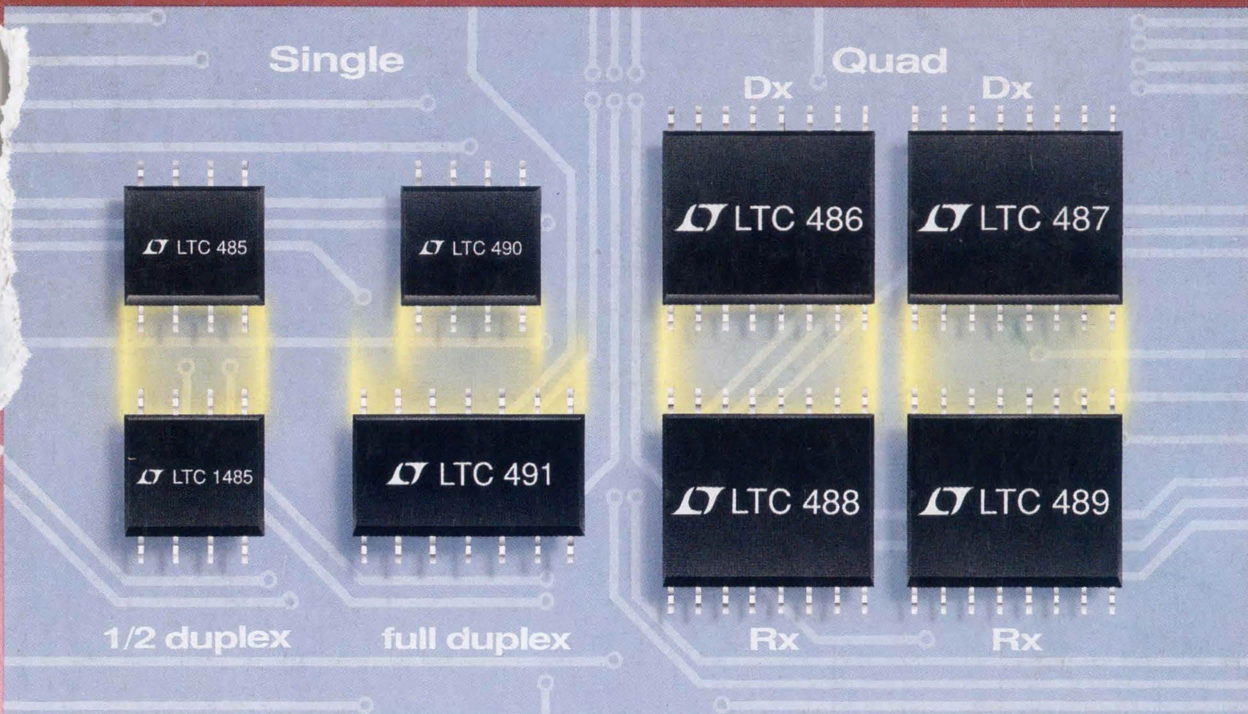

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LTC486	10Mbs Quad Driver	400X Lower	150μA	75172
LTC487	10Mbs Quad Driver	400X Lower	150μA	75174
LTC488	10Mbs Quad Receiver	7X Lower	10mA	75173
LTC489	10Mbs Quad Receiver	7X Lower	10mA	75175
LTC490	Full Duplex Transceiver	140X Lower	500μA	75179B
LTC491	Full Duplex Transceiver	60X Lower	500μA	75ALS180
LTC1485	10 Mbs Half Duplex Transceiver	8X Lower	3.5mA	75ALS176B

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