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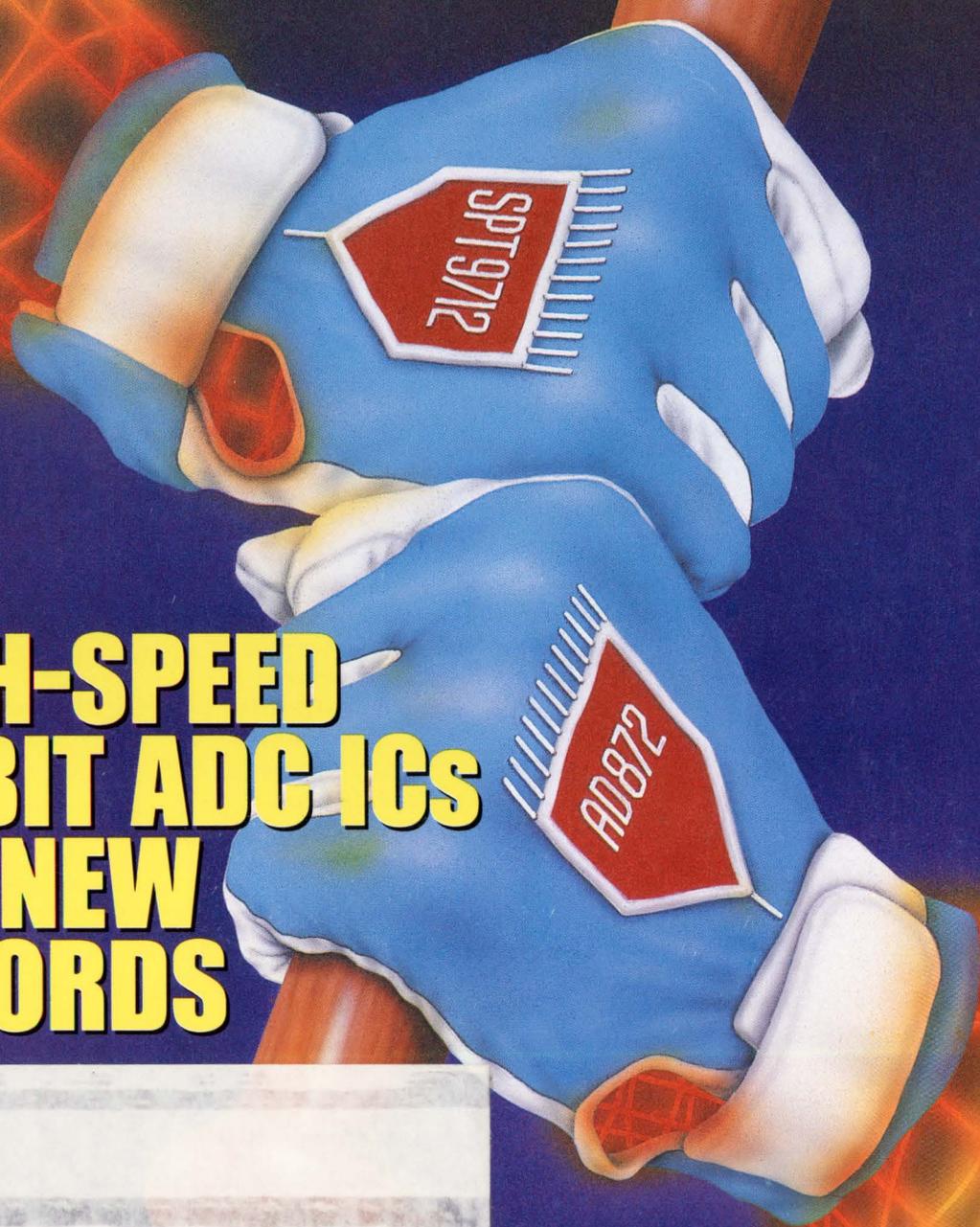
FOR ENGINEERS AND ENGINEERING MANAGERS — WORLDWIDE

# **ELECTRONIC DESIGN**

A PENTON PUBLICATION

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OCTOBER 24, 1991



**HIGH-SPEED  
12-BIT ADC ICs  
SET NEW  
RECORDS**



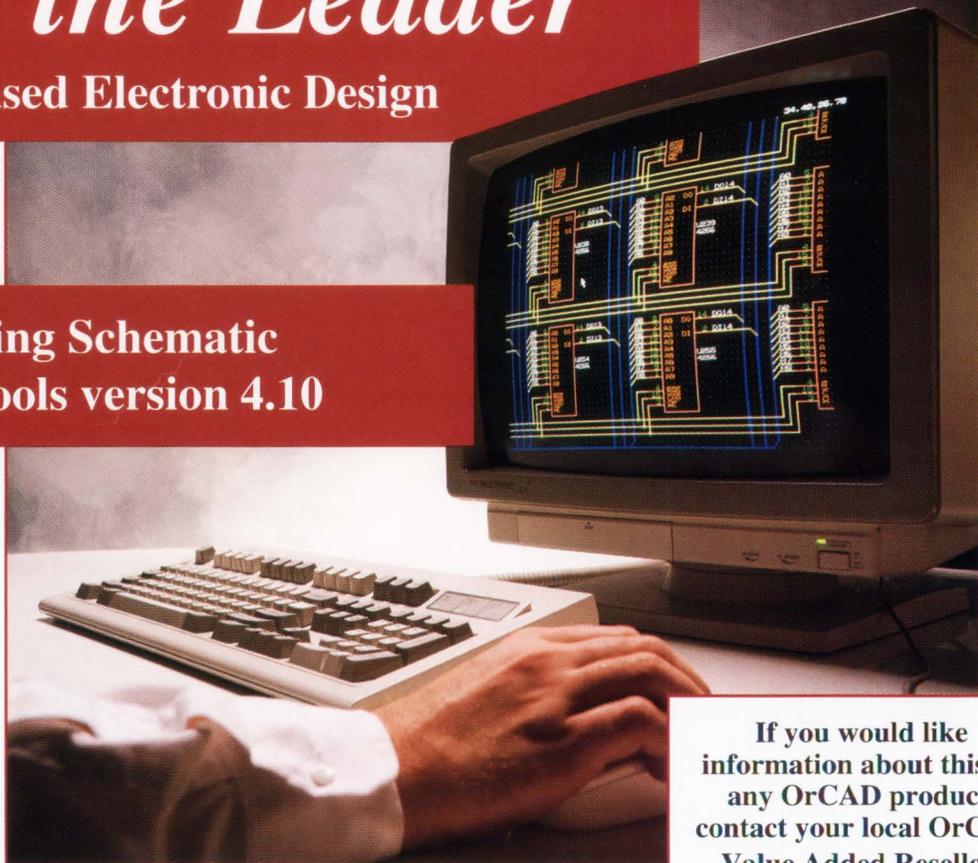
- PREVIEWS OF THE COMDEX/FALL '91 AND ITC '91 SHOWS
- SPECIAL SECTION: PC DESIGN—PC CHIP SETS DESIGNERS' GUIDE

**QUICKLOOK**

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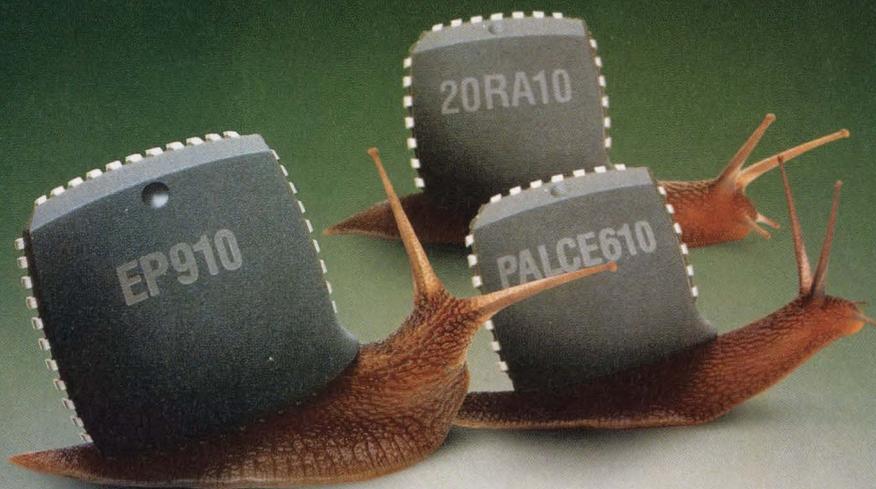
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# ELECTRONIC DESIGN



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1972 Certificate of Merit  
1975 Two Certificates of Merit  
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Cover: Bob Novak

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- Using a new Gilbert-cell analog multiplier
- Simulating VMEbus operations with new software
- Designing with a new combined microprocessor-DSP processor for voice processing
- PLUS:  
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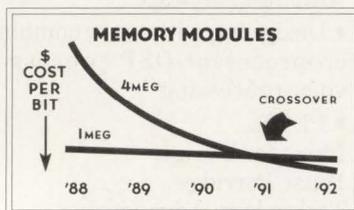
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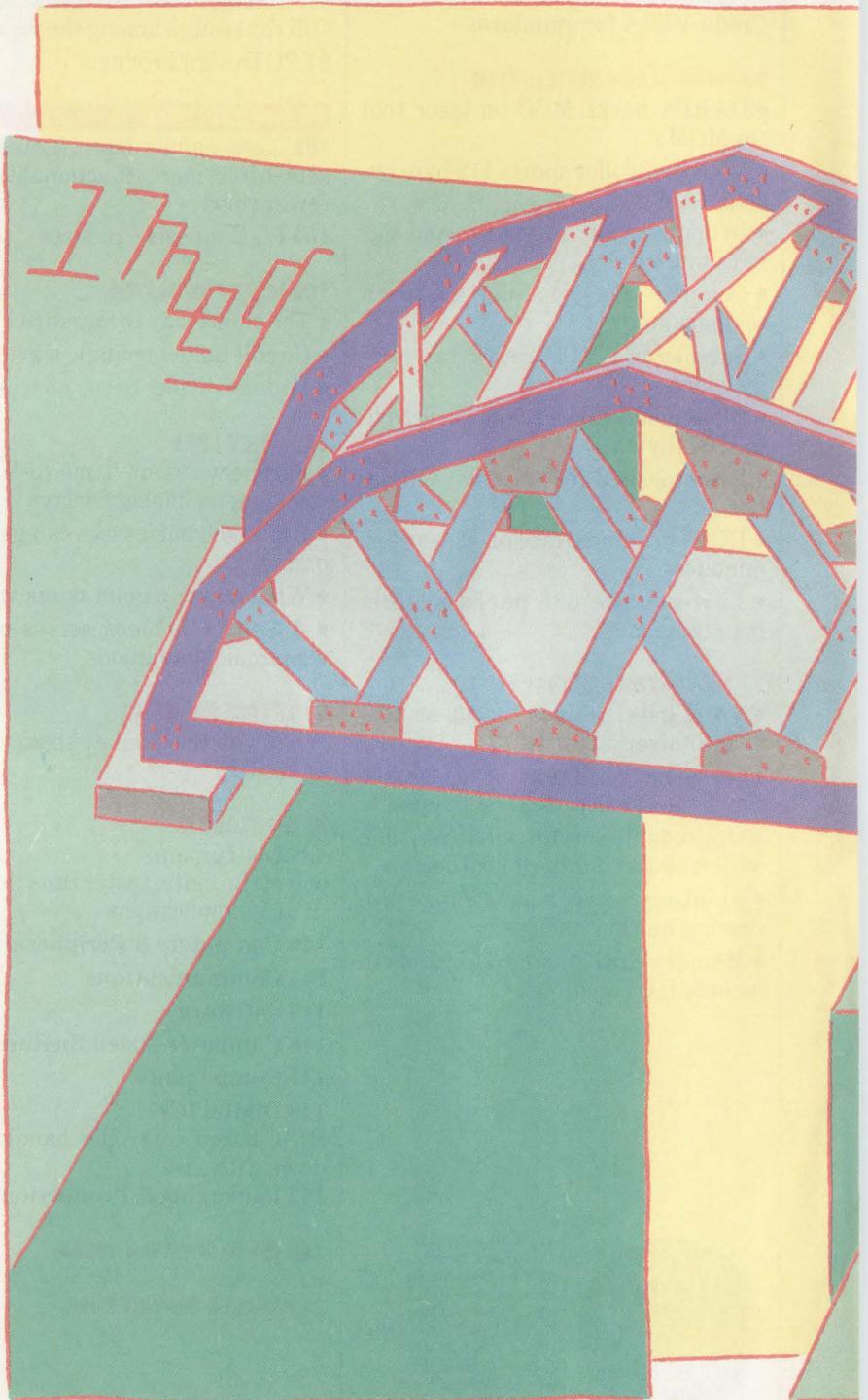
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4	KMM594000A	4M x 9
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4	KMM5331000A	1M x 33
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MACH 210	1800	64	12ns	66.7 MHz	44	MASC 210
MACH 120*	1200	48	15ns	50 MHz	68	MASC 120
MACH 220*	2400	96	15ns	50 MHz	68	MASC 220
MACH 130	1800	64	15ns	50 MHz	84	MASC 130
MACH 230*	3600	128	15ns	50 MHz	84	MASC 230

\* Available Q4 1991.

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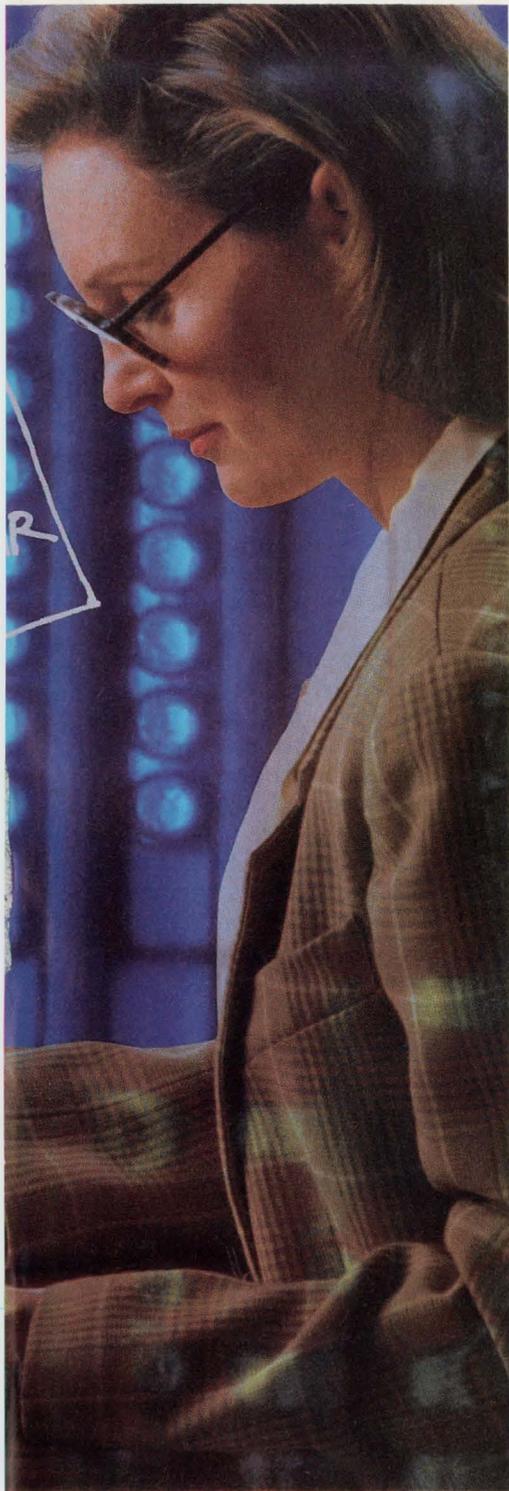
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## EDITORIAL

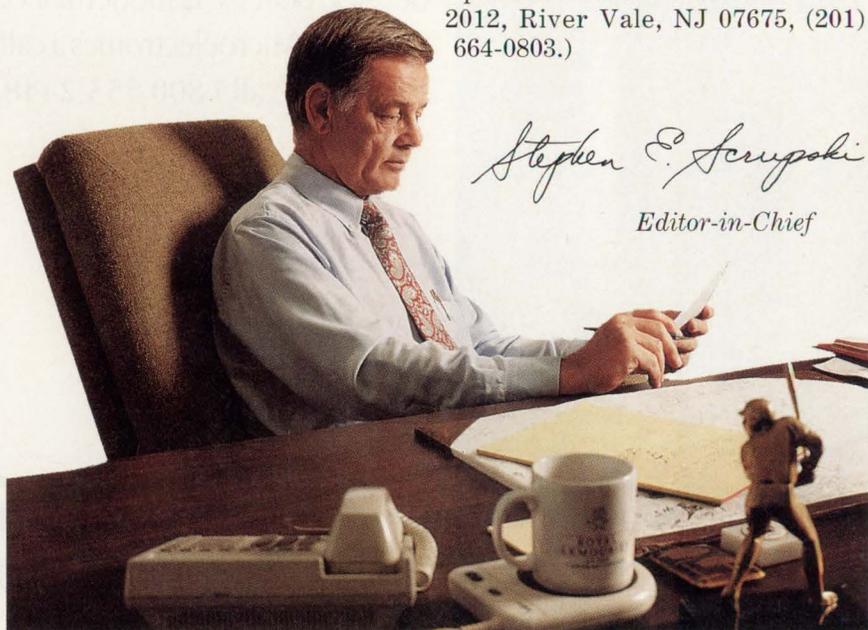
### THRIVING ON RESOLVING CHAOS

In the latest issue of the American Engineering Association's newsletter, *American Engineer*, AEA member Dean S. Carpenter offers a cogent definition of an engineer in a lead article titled "Engineers: Today's Problem Solvers." Carpenter notes that the June, 1989, *Delta Airlines Sky* magazine carried an article that postulated a new personality type; in addition to the well-known type A and B personalities, there are also type C personalities—persons who thrive on resolving chaos. Carpenter then comments: "I know lots of these people—they're called engineers," and proceeds to describe engineers as problem solvers who improve with experience. He closes his commentary with "We are a valuable personality type that should be respected and not a technological 'drill bit' which gets dull and useless in ten years or less."

Although it hardly seems necessary here, within the bounds of the *ELECTRONIC DESIGN* readership, one fact still bears repeating: engineers, more than any other group within a company, are the key people in adopting, applying, and deploying new technology. The product development group is growing in size with the inclusion of marketing, test, and manufacturing specialists. In particular, it seems that much is being said these days about the influence of a company's marketing group in shaping the configuration of new products. Most electronics marketers are engineers—they must be, to be able to deal with the highly technical material involved. And those marketers often are best able to translate customer needs into performance specifications for new products, because they are the closest to customers; we often have made that point here in the pages of *ELECTRONIC DESIGN*.

However, let's keep things in perspective: that viewpoint just underscores the fact that design engineers are the primary force behind converting performance specifications into new products—the people who, from day one in a project, make the critical design decisions that ultimately determine a product's success. In today's world of fast-paced technology advances with ever shrinking product life cycles, experienced engineers, with their seemingly innate ability to thrive on bringing order to chaos, are needed more than ever.

(By the way, if you would like information about joining the AEA, an organization that does appreciate the importance of experienced engineers and is dedicated to improving the lot of American engineers, contact AEA vice president Richard Tax at P.O. Box 2012, River Vale, NJ 07675, (201) 664-0803.)

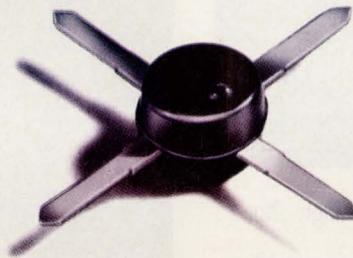


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Editor-in-Chief

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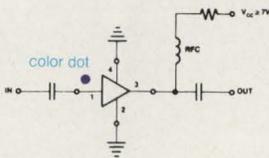
MODEL	FREQ. MHz	GAIN, dB			Min. MHz (note)	• MAX. PWR. dBm	NF dB	PRICE \$ Ea.	Qty.
		100 MHz	1000 MHz	2000 MHz					
MAR-1	DC-1000	18.5	15.5	—	13.0	0	5.0	0.99	(100)
MAR-2	DC-2000	13	12.5	11	8.5	+3	6.5	1.50	(25)
MAR-3	DC-2000	13	12.5	10.5	8.0	+8□	6.0	1.70	(25)
MAR-4	DC-1000	8.2	8.0	—	7.0	+11	7.0	1.90	(25)
MAR-6	DC-2000	20	16	11	9	0	2.8	1.29	(25)
MAR-7	DC-2000	13.5	12.5	10.5	8.5	+3	5.0	1.90	(25)
MAR-8	DC-1000	33	23	—	19	+10	3.5	2.20	(25)

NOTE: Minimum gain at highest frequency point and over full temperature range.

- 1dB Gain Compression
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### designers amplifier kit, DAK-2

5 of each model, total 35 amplifiers  
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\*MAR-8, Input/Output Impedance is not 50ohms, see data sheet. Stable for source/load impedance VSWR less than 3:1

Also, for your design convenience, Mini-Circuits offers chip coupling capacitors at 12 cents each.†

Size (mils)	Tolerance	Temperature Characteristic	Value
80 x 50	5%	NPO	10, 22, 47, 68, 100, 220, 470, 680, 1000 pf
80 x 50	10%	X7R	2200, 4700, 6800, 10,000 pf
120 x 60	10%	X7R	.022, .047, .068, .1µf

† Minimum Order 50 per Value

- Designers kit, KCAP-1, 50 pieces of each capacitor value, only \$99.95

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C113-Rev. D

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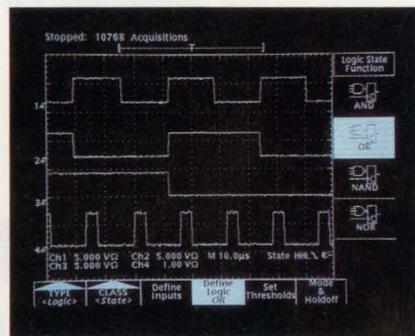
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Only by the addition of Tek's TriStar™ Digital Signal Processor (DSP).

Only by Tek's capacity for taking the hard work out of high performance.

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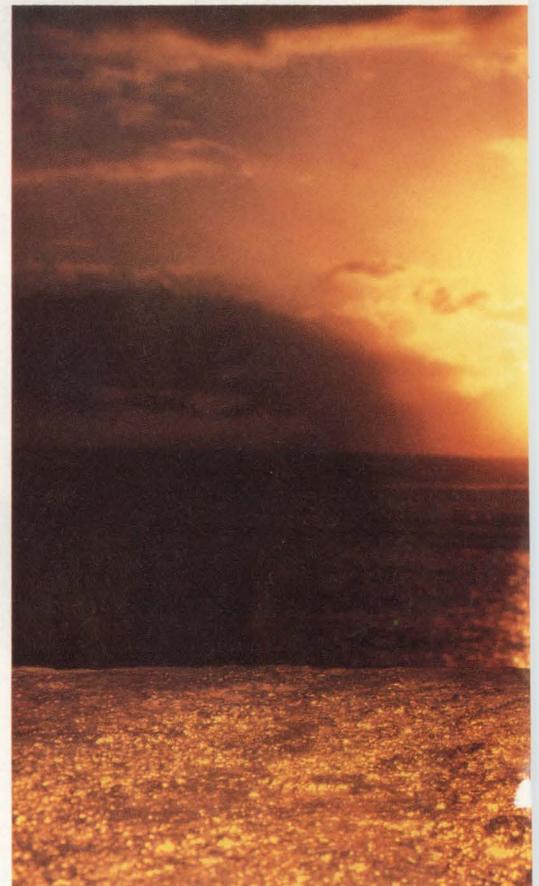
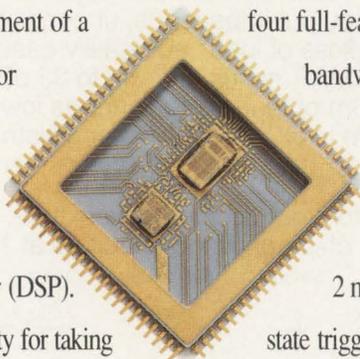


time DSP lets you perform single-shot averaging and extend resolution to 12 bits. The TDS Series arms you with up to

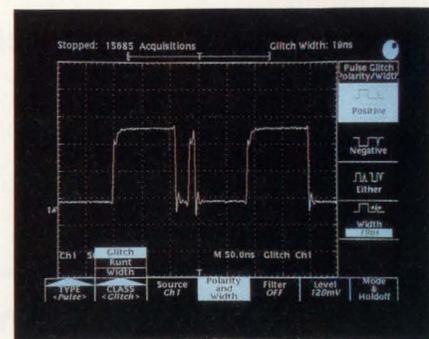
four full-featured channels. 500 MHz bandwidth. Up to 1 GS/s sampling and 4 ns peak detect.

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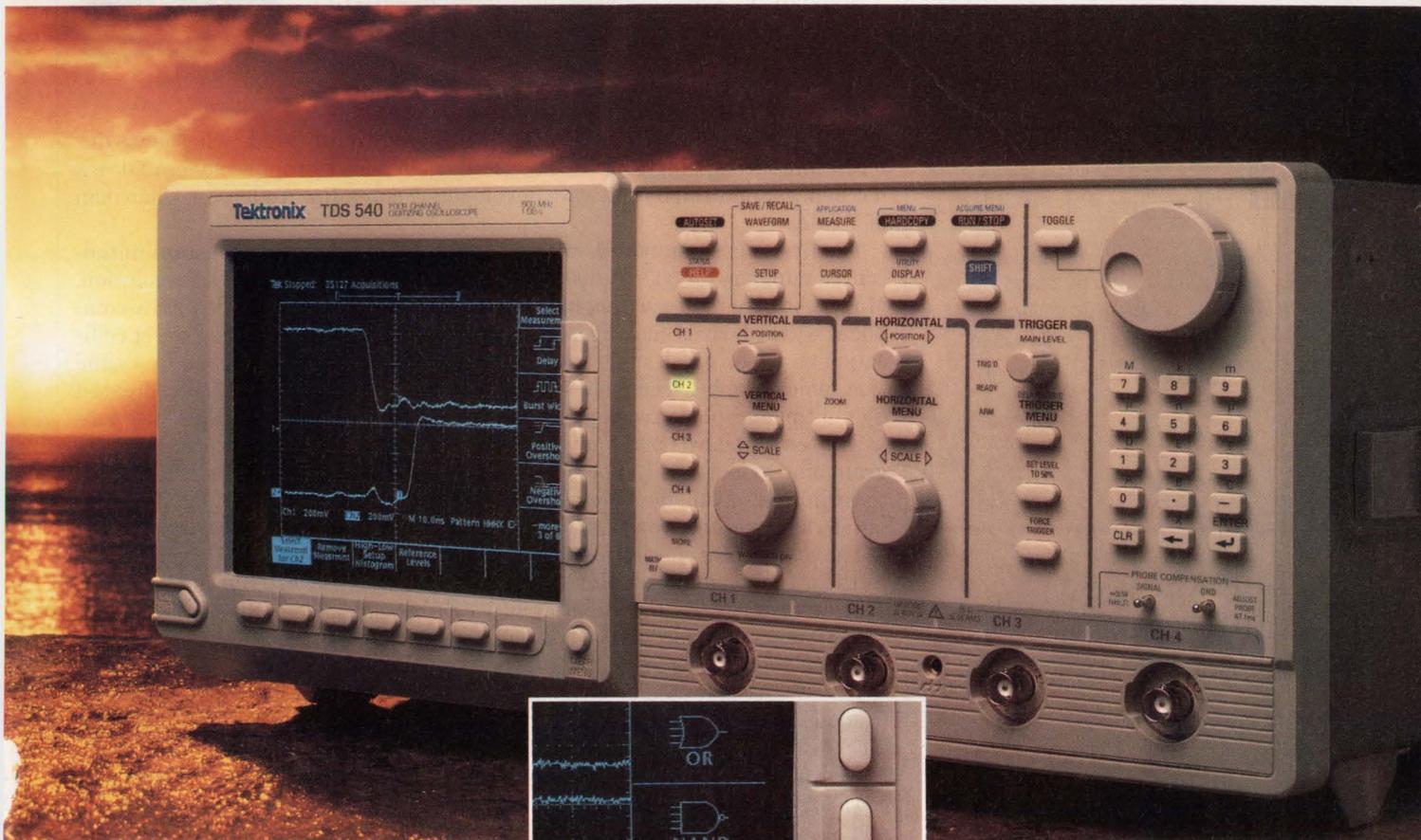
2 ns glitch, runt, pattern and state triggers. With acquisition sensitivity and fast overdrive recovery bringing greater waveform detail within your grasp.



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# million oscilloscopes one like this.



could be, you owe yourself a demo of the TDS. Its simplified front panel, VGA-quality display resolution, on-line help text, innovative icons that instantly differentiate menu functions — all add up to a scope that makes the user's manual more a formality than a necessity.

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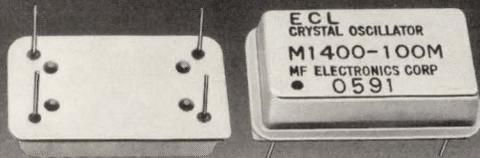
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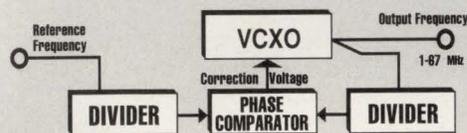
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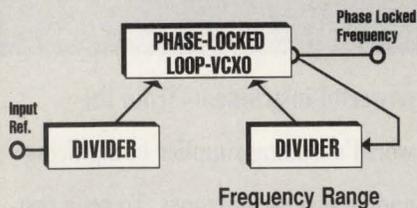
With MF VCXO's, since the specification is computer-tested over the full operating temperatures, you can be assured that the specified frequency-deviation is what you get for capture range.

	Control Voltage	Deviation
M2001	0.3 to 10V	±175 ppm
M2002	0.2 to 4V	± 75 ppm
M2003	0.3 to 10V	±300 ppm
M2004	0.3 to 10V	±125 ppm
M2005	1.0 to 4V	± 75-300 ppm
M2006	0 to 5V	±150 ppm
M2007	0.5 to 4.5V	±250 ppm

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## TECHNOLOGY BRIEFING

### CREDIT VESA FOR STANDARDS

In today's video graphics market, compliance to standards is required to achieve 100% system compatibility. Standards guide product development and help shorten design cycles, tighten budgets, and differentiate products. For these reasons, the Video Electronic Standards Association (VESA) was formed in an effort to standardize extended video-graphics modes. Its membership is open to anyone involved with graphics.



RICHARD NASS  
COMPUTER SYSTEMS

Standard PCs and graphical-user interfaces (GUIs) further the need for high-performance graphics. While PC graphics implementation has traditionally been one of the best ways to differentiate system performance, it's also been one of the most exasperating compatibility problems facing designers. "As a result, designers must decide whether to differentiate through higher performance and 'enhanced' graphic modes and risk not being supported by software developers," notes Jim Anderson, Chairman of VESA.

The first VESA standard, known as "Mode 6Ah" defines consistent initialization numbers for 800- by 600-pixel, 16-color Super VGA (SVGA) resolution. Mode 6Ah gives software engineers concrete specifications for all VESA-compliant SVGA boards, making it easier to build applications. Putting the specification on paper was a small step technologically, but it marked the first time that major graphics companies worked together to end the confusion created by multiple graphics architectures. Since issuing Mode 6Ah, VESA has published ten standards and four technical guidelines, and has developed a programming toolkit. VESA now contains four technical committees with charters to explore all available video-graphics technologies, develop standards proposals, and present proposed standards to VESA's entire voting membership.

The committees consist of design engineers working on specific graphics projects for their companies. Hence, the companies have a vested interest in proposed standards. By participating in VESA technical committees, engineers can influence standards development in their early stages. At the same time, they can get a head start on their own development projects.

The SVGA committee has defined more than a dozen VESA BIOS extension calls to support extended-mode VGA operation. Software developers can use SVGA's VESA driver to support almost all of the SVGA products available today.

VESA's XGA committee addresses the transferring of IBM's XGA for Micro Channel to EISA- and AT-bus platforms. IBM Corp., White Plains, N.Y., and SGS-Thomson Microelectronics, Carrollton, Texas, to whom IBM recently licensed its XGA chip set, are two active participants on the XGA committee, along with many other companies interested in this emerging standard. An XGA-standard proposal presented at the October 20 VESA meeting is expected to be voted on in early 1992. In addition, a standard for a protected-mode driver that supports Unix and OS/2 environments was voted on.

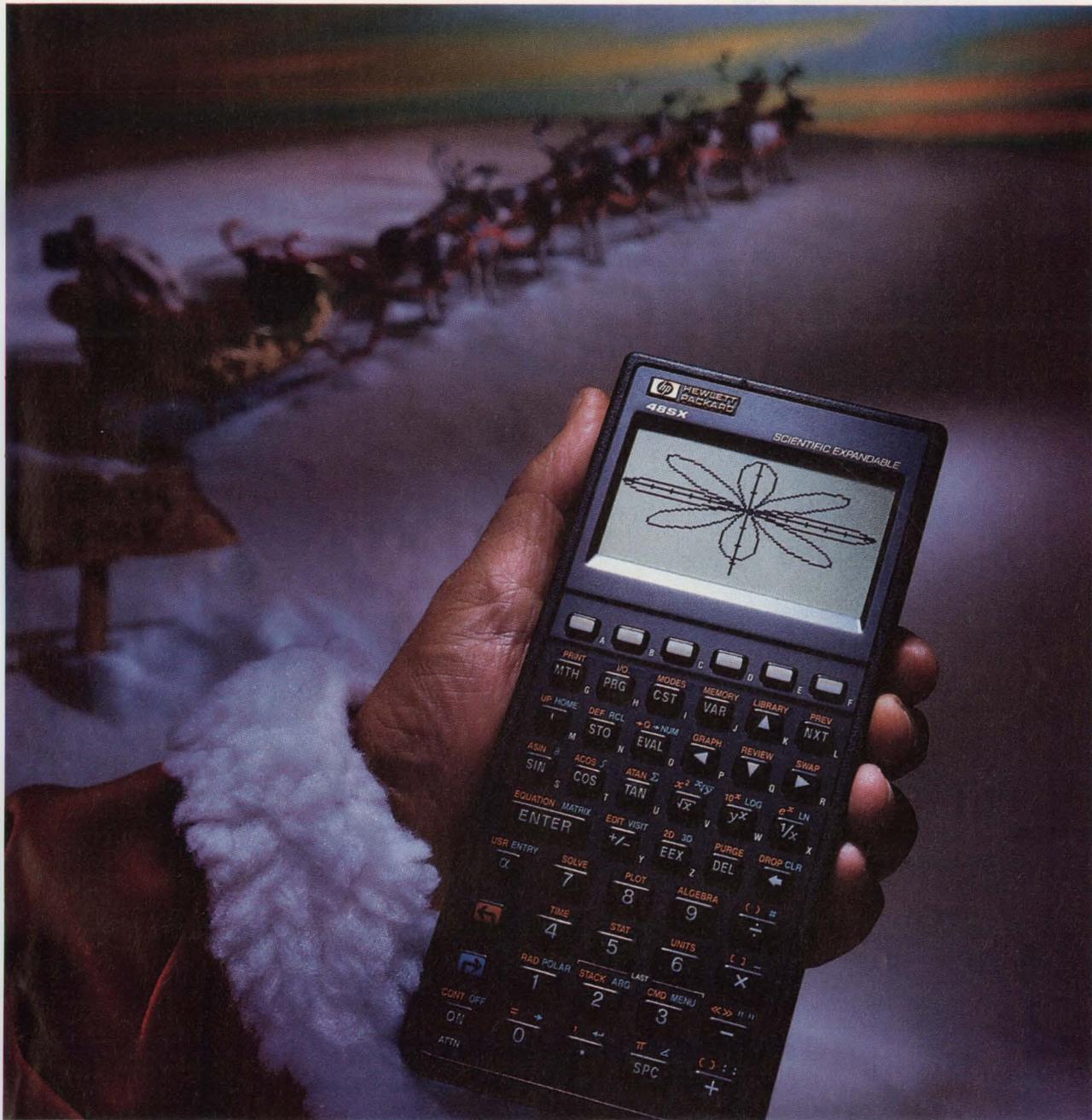
The multimedia committee's objective is to define and standardize emerging multimedia technologies. The first proposals will define standards for connectors and signal levels. For instance, one proposal will discuss which audio and video input and output jacks should be used to ensure that all parts of a multimedia environment work together.

VESA also has a GUI-X forum to address issues involving hardware accelerators for GUIs, such as X-Windows systems, Windows 3.0, Presentation Manager, and CAD environments. With the forum, GUI developers can interact with designers of chip sets, drivers, and systems.

Future VESA-related columns will appear in ELECTRONIC DESIGN'S PC Design section throughout 1992. Those columns will explore various emerging video-graphics technologies and VESA standards in detail. For information on VESA, call (408) 971-7525.

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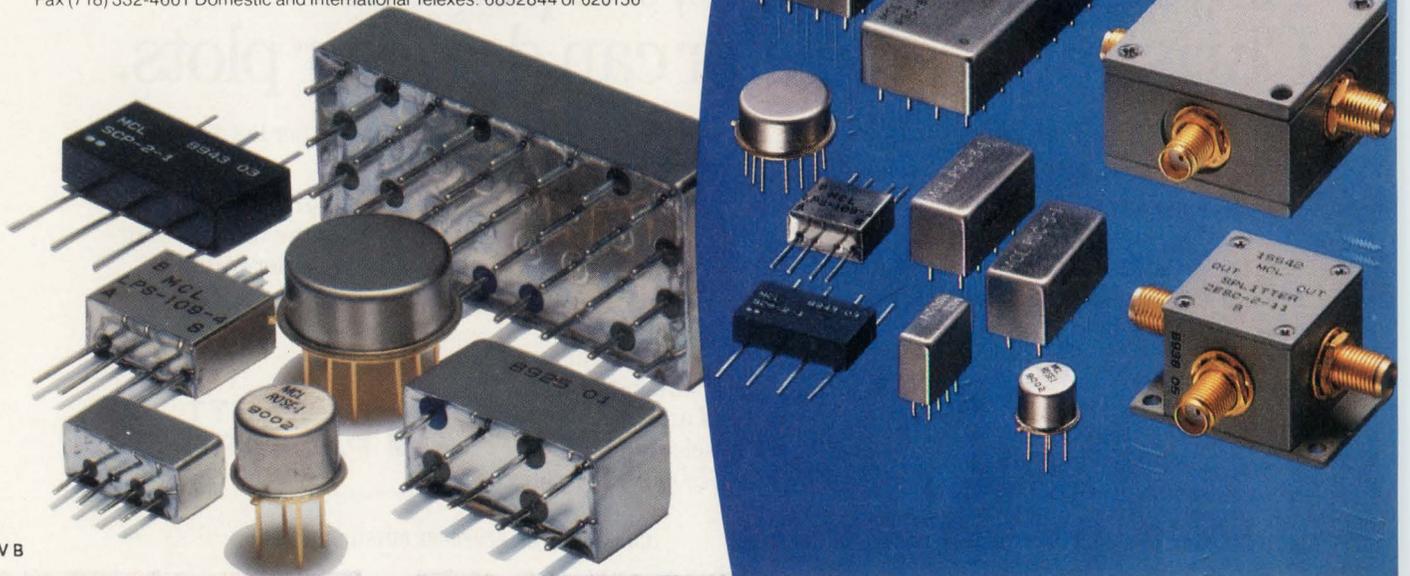
For detailed specs and performance data, refer to the MicroWaves Product Directory, EEM or Mini-Circuits RF/IF Signal Processing Handbook, Vol. II. Or contact us for our free 68-page RF/IF Signal Processing Guide.

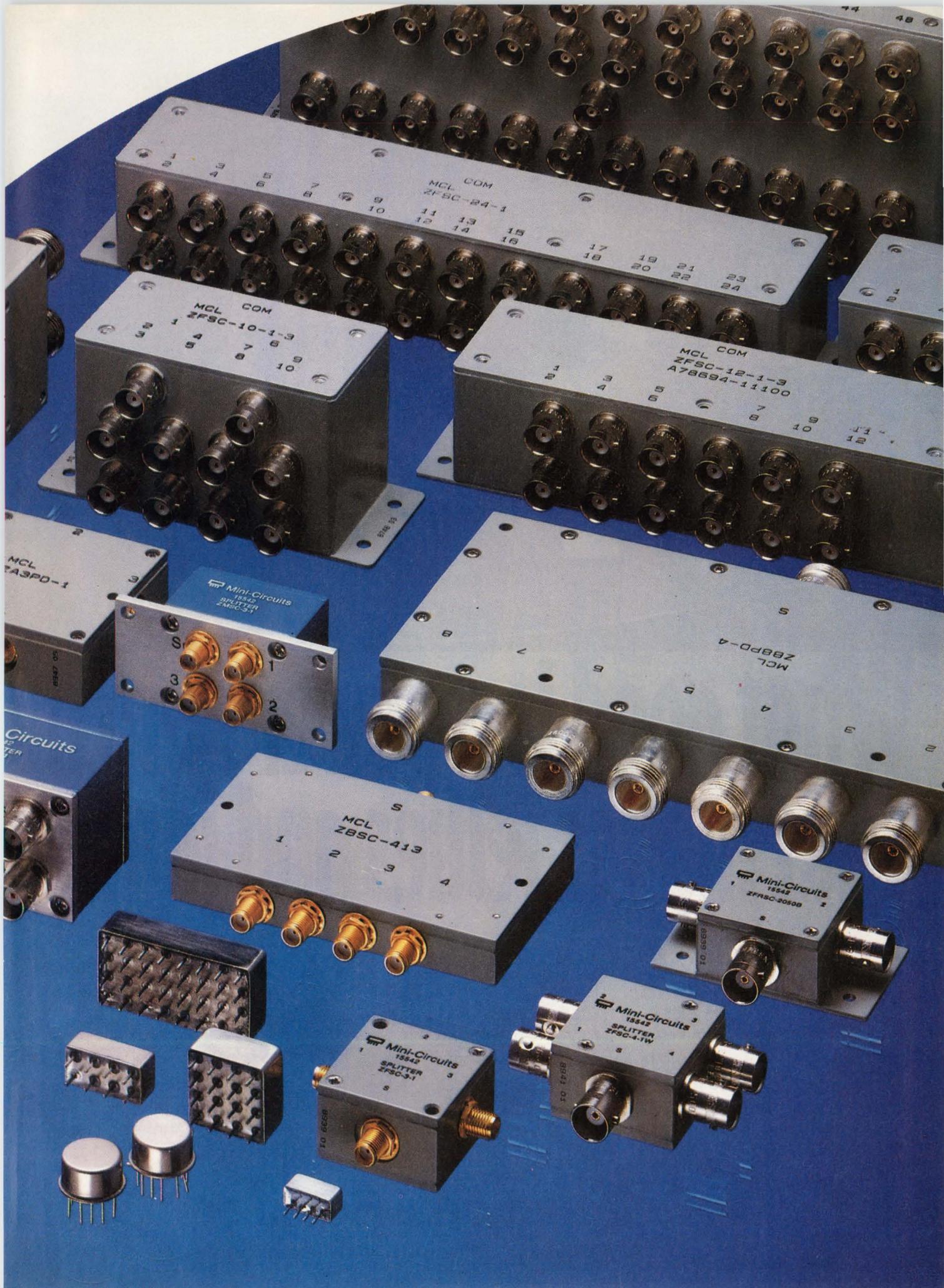
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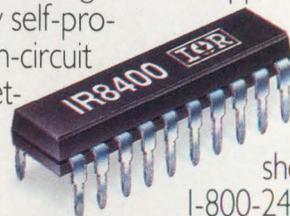
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## DARPA BACKS MCC ON LASER TOOL FOR MCMS

A programmable-laser customization tool for multichip-module (MCM) interconnection substrates is the object of a continuing project at the Microelectronics and Computer Technology Corp., Austin, being funded by the Defense Applied Research Projects Agency. With the tool, users can reduce the time to produce alternative MCM designs from weeks to hours. By coupling the laser tool with a special version of MCC's Quick Turn Around Interconnect technology, "blank" interconnection substrates can be made in advance. The final (customized) layer of circuitry will be "drawn" using the laser tool. A built-in router selects the laser operations required to transform the generic substrate into custom circuitry for the given module. DARPA authorized \$1.2 million for Phase II of the development, providing for integration of the first phase's components into one or more functional demonstrations of the technology. In doing so, MCC will expand its scope from using its own substrates to using those produced by outside vendors. *DM*

## MICROCONTROLLER SPORTS 512-BYTE ON-CHIP RAM

The first 80C51-compatible controller to feature 512 bytes of on-chip RAM has arrived claims Philips Semiconductors, Eindhoven, the Netherlands. The 83C528 also has 32 kbytes of on-chip ROM, which together with the high RAM capacity allows the device to run compiled application software programs written in high-level languages like PL/M and C. According to the company, the limited RAM and ROM capacity of existing 80C51-compatible microcontrollers often requires programs to be hand-crafted in assembly language. This results in higher software-development costs and programs that are more difficult to debug. The 512-byte RAM of the 83C528 also supplies enough space for context switching, especially for stacking enhancements in internal memory. Another feature, a watchdog timer with its own on-chip oscillator, allows the timer to run during power-down mode and wake up the microcontroller from that mode when a watchdog-timer overflow occurs. The 83C528 can also be awoken by an external interrupt signal, which allows it to continue program execution from the status of the last program instruction executed before it entered the power-down mode. *JG*

## IN-DEPTH REPORT REVIEWS MIXED-SIGNAL SIMULATORS

A 200-page report entitled "Mixed Analog-Digital Simulation in the 1990s" is available from Technology Information Publishing, Aptos, Calif. The report is intended for engineers using, supporting, or developing analog and digital simulators. It provides a comprehensive, comparative analysis and selection guide for commercial simulators, and describes how their impact on modern design methodology serves as a gateway to new and advanced circuit designs. Hans Klein, Ph.D., authored the report, which sells for \$995 in the U.S. and \$1350 abroad. Contact Technology Information Publishing at (408) 685-9217. In Europe, call the Denmark office at 4543712044. *LM*

## COMPAQ TAKES MODULAR APPROACH TO UPGRADING

With an eye to PC users as well as to CAD engineers, Compaq Computer Corp. has unleashed a line of modular PCs that can be upgraded by lifting boards out of the chassis and sliding new ones in. The Houston, Texas, company parcels out system components onto five subsystem boards—processor, video graphics controller, EISA bus, I/O, and memory expansion. To enable an upgraded system to keep pace with a new processor's higher speed, Compaq developed several ASICs for the subsystems, including a custom memory controller. Separate subsystems also mean that users can upgrade more than processors and memory, typical of other modular systems. At the low end is the Deskpro 386/25M, built around a 25-MHz 386 processor with a 25-MHz cache memory controller. At the high end is the Deskpro 486/33M, with a 33-MHz 486 processor (other models sport 16- or 25-MHz versions of the 486), an integrated cache controller with 8 kbytes of cache memory, and an integrated 387-compatible numeric coprocessor. System prices range from \$3099 to \$7199. Upgrade prices go from \$169 for a 1-Mbyte memory expansion SIMM to \$1999 for a kit to upgrade to the fastest 486 processor. *SVT*

## SUBMICRON CMOS GATE-ARRAY FAMILY WIDENED

A submicron 0.7- $\mu$ m triple-metal CMOS gate-array family offers 250-ps speeds and high densities, and has the industry's widest range of sizes, according to its developer SGS-Thomson Microelectronics, Milan, Italy. With such features as JTAG support and direct drive of standard buses, the ISB24000 Complete family solves many system-level problems facing designers. With usable gate counts ranging from 3000 to more than 200,000, the family addresses high-performance computer, telecommunications, and data-communications requirements, from medium-density bus-interface applications to fully integrated systems on-a-chip. With 18 different array sizes available, silicon

efficiency isn't compromised. The ISB24000 Complete series reduces costs and improves system speed by driving standard backplanes directly. The I/O features include variable slew-rate control, independent I/O and core-power distribution, and compatibility with EISA, ISA, MCA, and SCSI standards. Other features include compatibility with the emerging 3.3-V standard, excellent clock distribution for minimum skew, and testability support at the device and system level, with full support for the IEEE 1149.1 JTAG specification. *JG*

## GLASS MEDIA TAKES 2.5-IN. HARD DRIVE TO 180 MBYTES

Using glass media in 2-1/2-in. hard-disk drives isn't new, but taking the technology to 180 Mbytes is. Areal Technology Inc., San Jose, Calif., achieves this plateau in its A180 drive. Glass disks, claims Areal, are harder, flatter, and smoother than advanced thin-film aluminum disks used in competitive drives. These factors permit the A180 drive to store more data per square inch, increasing the drive's areal density (the amount of data that can be stored per square inch of disk surface). Because more data can be stored with fewer platters, and ultimately fewer heads, manufacturing costs, size, weight, and power consumption are reduced, while reliability is increased. Areal rates the A180 drive at 80,000 start-stop cycles before failure. Because of the media's hard surface, it's more resistant to failure from inadvertent head-disk contact while in transit. Stiction is also less of an issue with glass media than other types of media because it's less prone to chipping. Stiction occurs when humidity within a drive combines with tiny particles chipped from the disk surface by the heads. The A180 drive should be available by the end of the year. *RN*

## PATENT ISSUED FOR SELECTIVE SIMULATION

The U.S. Patent Office has issued a patent to Aldec, Newbury Park, Calif., for the selective simulation technology used in Aldec's Susie logic simulator. Unlike other simulators that need to operate on an entire design, Aldec's product lets designers choose a specific area of interest for viewing and simulation. This speeds the overall verification time by as much as 100 to 1000 times over traditional methods. The new technology changes the way that designers can work. For instance, using the selective simulation, they can first verify the core of the design and then selectively allow other areas of interest to interact with the core. For more information on the selective simulation technology, call Aldec at (805) 499-6867. *LM*

## IEEE TO STANDARDIZE ON SENSOR TERMINOLOGY

The TC-9 Technical Committee on Sensors of the Institute of Electrical and Electronic Engineers has formed a task group to develop standards for terminology and units covering pressure and acceleration sensors. A draft revision, the Sensor Terminology Standard, is being circulated to interested parties for comments. The draft revision covers three major areas: general definitions, technology-related terminology, and performance-related definitions. The Instrument Society of America already has such standards, which have been adopted by some industries. Now with the development of silicon micromachined sensors, the need for standards acceptable by all industries (i.e. process control, automotive, medical, industrial controls, etc.) has become even more important. The draft revision was developed by Dr. Janusz Bryzek of Lucas Novasensor, Fremont, Calif., and Dr. Kenneth G. Kreider of the National Institute of Standards and Technology, Gaithersburg, Md. Interested parties may contact Dr. Bryzek at (510) 490-9100 (fax is 510-770-0645) or Dr. Kreider (fax is 301-975-3845). *RA*

## LOW-VOLTAGE 386 PACKS SYSTEM MANAGEMENT

When it comes to saving system power, chip designers typically have two options—either slow down the system or reduce the power-supply voltage. In portable computers, however, performance compromises to save power are usually unacceptable. So designers at Advanced Micro Devices, Austin, altered the transistor characteristics of their CMOS process to create versions of their 80386-family replacements that can operate at supply voltages of 3.3 V. As a result, the Am386SXLV and DXLV can save about 40% of power consumed by a 5-V implementation. AMD also orchestrated the development of several related low-voltage circuits from suppliers of motherboard logic chip sets, video controllers, and other chips so that the rest of a portable computer can also be implemented with chips operating at 3.3 V. To ease system control of power consumption, a system-management interrupt capability was given to the CPU chips, a feature that matches the capability Intel gave its high-integration 80386SL processor, which was designed for portable computer systems. (*Note: The AMD low-voltage processors will be featured in our next issue.*) *DB*

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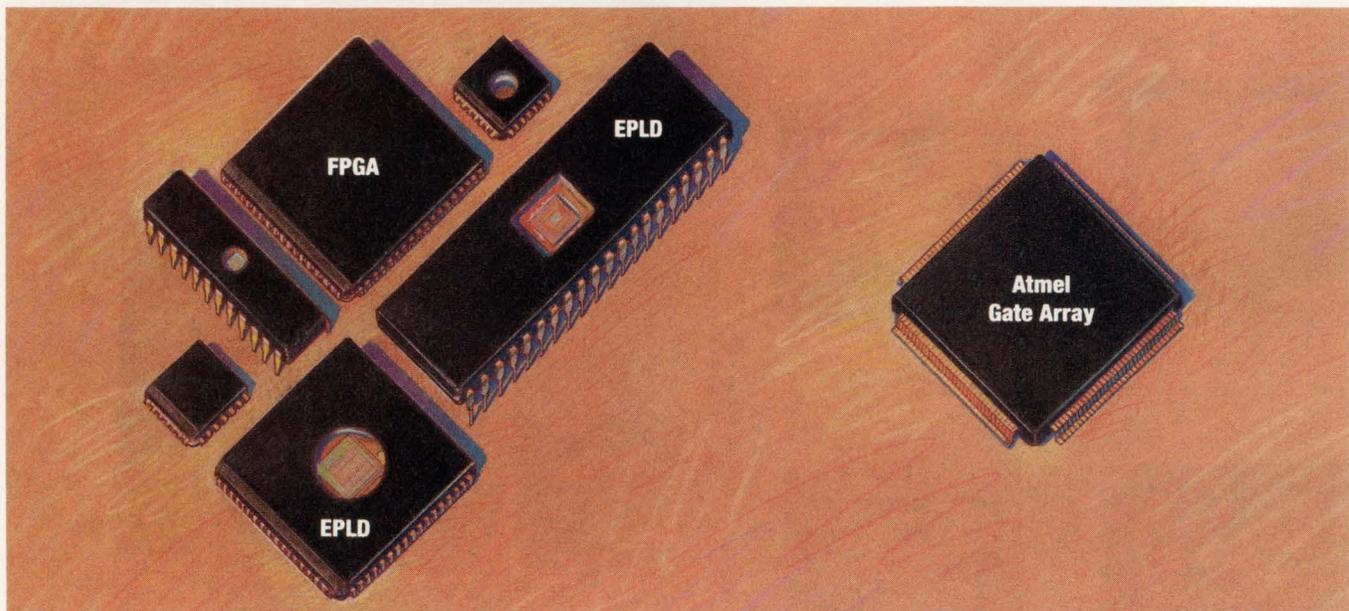
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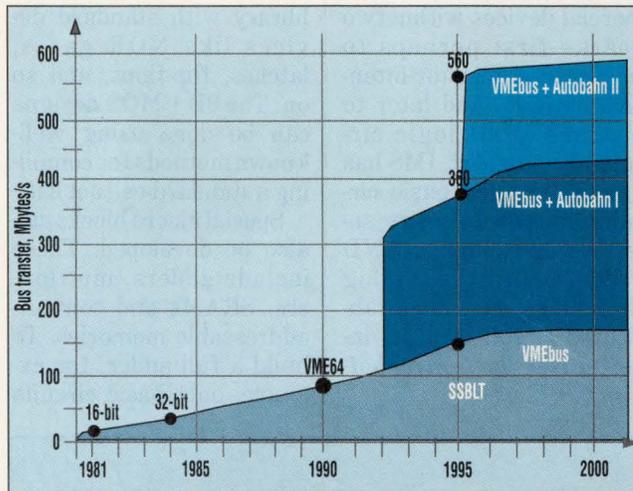
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## VME GETS 10-TIMES BOOST AS TEN-YEAR ANNIVERSARY GIFT

The VMEbus will mark its tenth anniversary with a performance level that has soared to an all-time high of 3.2 Gbits/s—a 10-fold increase. This performance boost is due to Autobahn, a technology developed at PEP Modular Computers, Carnegie, Pa., which can transfer digital data to the serial bus at a rate of 400 Mbytes/s. Josef Kreidl, PEP's president, and one of the key architects behind Autobahn, says that he's been working out the details of Autobahn over the last few years, but the IC technology wasn't available until recently. Autobahn I, slated for arrival in early 1992, will transfer data across the bus at 200 Mbytes/s. By the end of next year, Autobahn II should arrive, completing the push to 400 Mbytes/s (see the figure).

The data transfer takes place as a differential serial exchange on two existing, though rarely used, pins of the VMEbus, SERCLK and SERDAT. The bus' existing data-transfer features can be used simultaneously because everything else is the same. Although Autobahn was designed for the VMEbus, it's actually bus-independent. It can be used with any bus structure containing two spare pins, such as Futurebus+. In addition, Autobahn is compatible with the IEEE 1014 VMEbus specification and its proposed extensions, including VME64 and SSBLT. The new technology will probably use eight address-modifier codes that aren't presently being utilized.



Autobahn reduces data-transfer latency on the bus to nearly zero. This feature will be a big boost to such applications as graphics, image processing, and mass storage. The same technology can also be applied to transparent cache transfers in multiprocessing schemes and fast data updates for redundant systems. Because the basic transfer mechanism is serial, any bus width can be defined. Hence, it lends itself to nearly instantaneous bus-width conversions. Autobahn can also serve as a high-speed bridge between two generations of buses, such as VME and Futurebus+.

Autobahn's design includes a very sophisticated high-frequency signal line that can be mounted to the VME backplane in the form of a small piggyback. Because the signal is transferred differentially, there's very little attenuation, noise, or crosstalk in the two signal lines. A differential transfer means that while one line voltage has a positive signal and the other has a negative signal, a positive change on

one line produces the exact same signal on the negative line in the negative direction.

The high transfer rates are made possible due to advancing IC technology. Although the original plans included gallium-arsenide parts, PEP turned to ECL gate arrays developed by Motorola Semiconductor, Austin, Texas, when multipoint backplane noise problems couldn't be rectified. ECL's line-driver characteristics allow longer distances and multipoint con-

nections. In addition, because of the low 0.15-to-0.5-V level of the ECL signal, crosstalk and RFI are inherently small when compared to VME's 0-to-5-V TTL signal.

The chip set for Autobahn I should be available in the first quarter of next year. The set includes an ECL multiplexer-demultiplexer, a phase-locked loop, a prescaler, a voltage-controlled oscillator, and a dc-dc converter. The set should consume a total of about 1 W. The chips will initially operate in the  $-40^{\circ}$  to  $+85^{\circ}\text{C}$  temperature range, later expanding to the full military range. By the end of 1992, the five Autobahn parts should be integrated into one chip. The Autobahn II chips should appear by the end of 1992. National Semiconductor Corp., Santa Clara, Calif., will also be a supplier of the ECL Autobahn chips. Kreidl notes that the cost of implementation shouldn't exceed \$100 when volume shipments commence.

RICHARD NASS

## 3D SILICON VLSI PROCESS OFFERS FIVE TIMES THE DENSITY OF 2D TECHNIQUES

Typically, to satisfy the growing demand for a larger number of logic functions on a chip, die size is increased and feature sizes decreased. But further scaling of present two-dimensional circuit technologies down to the submicron region is becoming more and more difficult. Three-dimensional stacking of transistors

would thus seem a logical method for raising on-chip circuit complexity.

This is the approach taken by a group of researchers at Germany's Institute for Microelectronics Stuttgart (IMS). Using a 3D CMOS technology called Epilog, they've pushed VLSI circuit density two to five times beyond the levels attainable with compa-

rable 2D CMOS techniques now in use (see the figure, top).

IMS feels that the Epilog technology is a milestone in VLSI circuit development, and after a 7-year R&D phase, has now reached maturity. "It has advanced to a point where the industry could use it to build commercial 3D VLSI parts," says Bernd Höfflinger, director of IMS and the man behind the new technology.

He believes the industry could apply Epilog to commercial devices within two years—first perhaps to fabricate transistor-intensive SRAMs, and later to produce VLSI logic circuits. For its part, IMS has already created basic circuits, such as inverters, selectors, and 2-input NAND gates, using the Epilog technology. One such fabricated circuit is a 3D inverter (see the figure, bottom).

These basic circuits could be used to build a cell library with standard devices like NOR gates, latches, flip-flops, and so on. The 3D CMOS designs can be done using well-known methods for compiling a standard-cell net list.

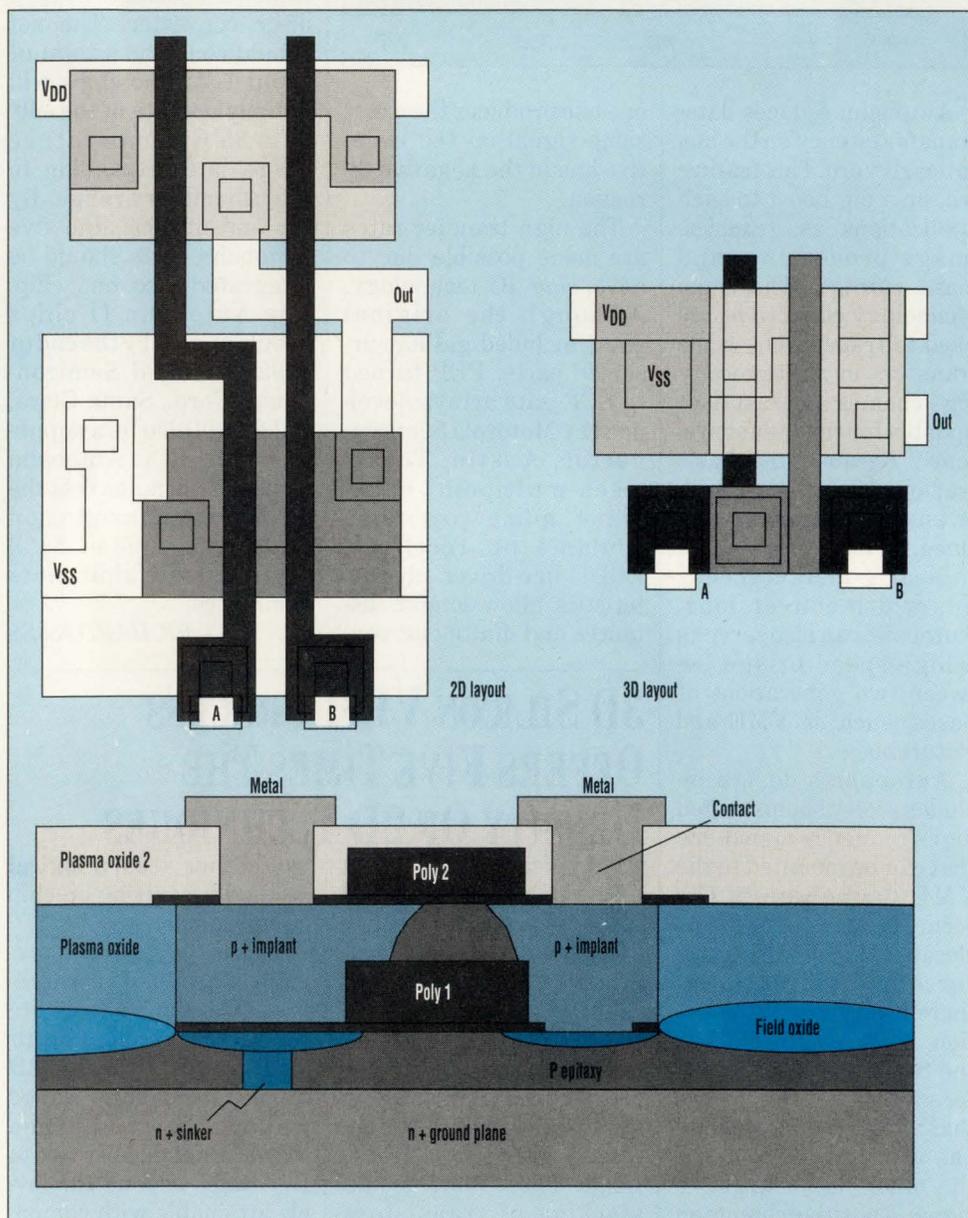
Special macro blocks can also be developed. These include adders, multipliers, SRAMs and content-addressable memories. To build a full adder, for example, only basic circuits

are used. A parallel multiplier can easily be made by abutting a half-adder line, a full-adder array, and a ripple-adder line.

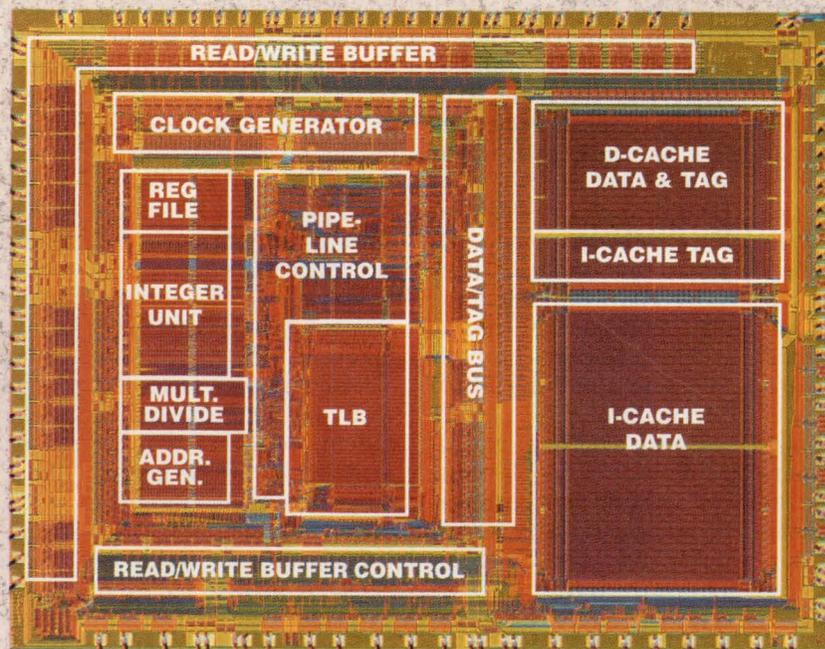
Conventional 2D CMOS VLSI devices, for all of their high-speed, high-functionality and low-cost advantages per function, have a number of shortcomings. The interaction between the closely spaced transistors can lead to disastrous latch-up. Also, the large area occupied by the interconnections can result in high load capacitance, increased power dissipation, and slower speed. Worst of all is the chance of electromigration, whereby the ions in the metal interconnections can produce catastrophic short-circuits.

Investigated for more than a decade, 3D or stacked CMOS technologies have been based mainly on polycrystalline silicon films on oxide. But efforts to recrystallize the films haven't led to any products—except to some marginal-performance, high-resistance polysilicon thin-film load transistors used in six-transistor-cell CMOS SRAMs.

"The real issues of 3D CMOS integration are silicon-film quality, surface planarity, the vias between the different layers, process complexity, device and interconnect density, and thermal budget—that is, the sum of all high-temperature cycles encountered in the fabrication process," states Höfflinger. "It may be hard to believe, but it's true that the Epilog technology is a high-quality yet simple method that satisfies all the criteria that 3D CMOS integration dictates."



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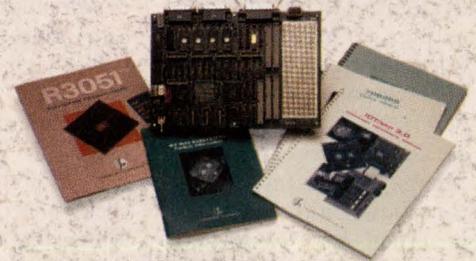
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The new technology starts from a standard bulk NMOS process and uses selective silicon epitaxy to grow a single-crystal vertical connection—the silicon via. Following this is a lateral crystalline overgrowth over the underlying oxide and polysilicon structures. This overgrowth extends across a characteristic device length. The silicon islands formed in this process are bounded by a plasma oxide that serves as lateral isolation and as a spacer for perfect planarization of the resulting stacked transistor structures. Planarization is achieved by chemo-mechanical polishing.

The Epilog technology (it's name derives from epitaxial lateral overgrowth) uses some steps, such as selective epitaxy, that

have been worked out in the early 1980s at the MIT Lincoln Laboratories in Cambridge, Mass., and at what was then the RCA Laboratories in Princeton, N.J. In 1984, Höfflinger, who headed the School of Electrical Engineering at Purdue University, Lafayette, Ind., refined these steps and worked out the 3D CMOS concept that he and his associates brought to maturity at the Stuttgart institute.

Epilog's features and capabilities can best be illustrated by using a high-performance, true six-transistor cell for a CMOS SRAM. The minimum cell size could be held to less than  $150 L^2$ , where  $L$  is the minimum feature size and the assumed metal pitch is  $5L$ . So when  $L$  equals, say,  $0.8 \mu\text{m}$ , the cell area would be

less than  $100 \mu\text{m}^2$ . That would be about half as small as an SRAM cell using conventional 2D CMOS technology.

The cycle time depends on the memory organization and would be typically from 10 to 15 ns. The minimum quiescent currents are low because of the high quality of the silicon films and the pn junctions. The inherently latch-up- and electromigration-free cell with only two aluminum-silicon contacts can be made with a single-metal, minimum-complexity process of only nine masks.

Because of the absolutely planar surface achieved by chemo-mechanical polishing, a standard metal process can be used. The perfect planarity also allows a narrow pitch to be employed. A dual-gate

PMOS load ensures that the cell has excellent transfer characteristics for maximum pull-up and pull-down speed. The PMOS off-on current ratio can be as high as 1:100,000,000.

With a two-layer metal interconnect on a perfectly plane surface, seven interconnect levels—three global and four local—are available. Using a maximum of ten masks, the two-metal 3D fabrication process, given the inherent planarity, is simpler than the comparable 2D two-metal process that requires 11 to 12 masks. The buried silicon ground plane and the silicon sinkers and vias not only provide superb density, but also eliminate ground bounce and metal contact as well as electromigration.

JOHN GOSCH

## UPGRADABLE SERVERS MADE POSSIBLE WITH MODULAR MOTHERBOARD DESIGN

A redesign of the main system board employed in a family of multiprocessor compute servers plus other upgrades allows users to get systems with performance ratings ranging from 50 to over 90 Specmarks. To achieve such performance levels, the just released 600 series servers from Sun Microsystems Inc., Mountain View, Calif., sport a redesigned 9U VME CPU card that was employed in the 400-series servers. By using an existing card format, users are given a choice—they can either upgrade existing systems with a board swap or purchase new complete systems.

The revamped CPU

board represents a design approach change for Sun Microsystems, explains Thomas Minot, the company's manager of electronic design automation market development. It's the first Sun Microsystems server CPU card that includes from 64 to 640 Mbytes of main memory (*see the figure*).

In addition, the revamped CPU board contains two Mbus slots that hold two of the dual-processor Sparc CPU modules released last month by the Ross Technology Div. of Cypress Semiconductor Corp., Austin, Texas (ELECTRONIC DESIGN, Sept. 26, 1991, p. 170). Each postcard-sized module contains two 40-MHz Sparc CPU and floating-point-unit

chips along with two CY7C605 multiprocessor memory management units and 64 kbytes of cache memory for each CPU.

The daughtercard modules connect to the motherboard using the 64-bit Mbus interface, allowing data transfers of as much as 320 Mbytes/s. By placing the CPUs on the Mbus daughtercards, Sun Microsystems allows simple system-CPU upgrades from their own efforts or from other card suppliers. Supplementing the motherboard are four SBus slots into which users can add various I/O support and graphics functions.

One possible upgrade path for the CPUs might have Texas Instruments

create an Mbus card version of its soon-to-be-released biCMOS SuperSparc chip subsystem (the CPU is known in the industry as the Viking, its code name during the development phase).

Estimates indicate that the 3-million-plus-transistor Viking chip will deliver two to three times the performance of existing Sparc CPUs. As a result, system performance is boosted between two and three times, delivering from 100 to over 200 Specmarks for dual- and quad-CPU systems.

In addition to the spruced-up motherboard with the high-speed CPU modules, Sun Microsystems defined a new disk-drive performance level with a 1.3-Gbyte drive that accesses in just 11.5 ms.

To control the drives and handle the multiple proces-



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## TECHNOLOGY ADVANCES

sors, designers at Sun Microsystems also ported the Solaris 1.0 Sun operating system to the board. That software also includes storage-control routines that allow disk striping to improve access time for sequential files that are divided (striped) across several disk drives (a software Raid level-3 implementation). Additional software features permit disk concatenation to handle files that are too large for any single drive, and mirroring to provide on-line backup with a spare drive.

For two of the three servers in the family—the 630 and 670MP—the system can address up to 26 Gbytes of storage, while the largest box, the 690MP,

can handle up to 52 Gbytes of storage. That large system employs IPI disk drives so that dual-ported systems can be implemented, improving overall system availability and permitting one of the two sys-

tem interfaces to fail without totally shutting down the system.

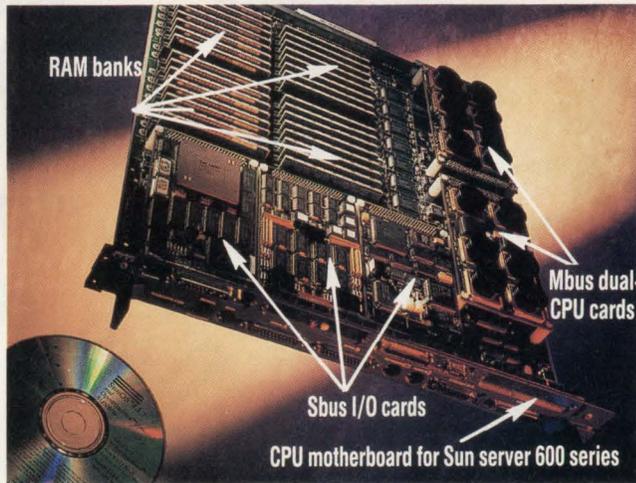
Thanks to the higher-performance CPUs, the faster drives, the better multiprocessor operating system, and more intelli-

gent I/O control, the Specmarks specifications showed more than a doubling in performance level from the previous high-end model—the SS490—and the number I/O transactions/s increased by over 60% over the older system.

Prices for a base-model dual-CPU 600-series server, which includes a CD-ROM drive for software distribution, 64 Mbytes of main memory, one 1.3-Gbyte hard-disk drive, and 5 VME card slots, start as low as \$45,000.

For more information on Sun Microsystem's revamped CPU board, contact Michael Schafir at (415) 969-9131.

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## ROTATING MATRIX MAKES IMAGE PROCESSING QUICKER AND EASIER

By using a 2D frequency-domain processor that works in tandem with a fast-Fourier-transform (FFT) processor, Array Microsystems, Colorado Springs, Colo., developed a two-board solution that processes images much faster than is possible with competitive techniques. The company's a66545 Cornerturn frequency-domain array processor board, when used with the firm's a66540 board, can process an entire 256-by-256-pixel image in 15.2 ms and 30 frames/s. The 6U VME-based Cornerturn board is designed

for medical imaging, radar, sonar, and other 2D image-processing applications. The two-board set features performance of 400 MOPS at a clock rate of up to 40 MHz.

Key to the board's operation is the rotation of the image's X-Y matrix in real time by 90°. By rotating the matrix, memory on the Cornerturn board sees the video-data columns as rows, making it easy to sequentially address the data to the FFT processor (see the figure).

Data representing an image is typically stored in a matrix of X rows by Y col-

umns. To process that data, each point is passed though the system's processor, and an FFT is performed on that data.

Fundamentally, two-dimensional FFTs are processed by first going through the one-dimensional FFTs on each row of data. Next, an FFT is performed on each column. Doing the FFTs on the columns may cause problems because the data is stored in one big block of sequential memory. Hence, when doing the FFT on the first row of a 512-by-512-pixel matrix, the 512 points are beside each other sequentially in memory. Therefore, it's easy to pick up those points and perform the FFTs. But when the

columns are addressed, the task becomes much more difficult. In the computer's memory, the first point is at location zero. The computer's memory sees the next point as being 512 points away. As a result, those points can't be processed sequentially.

The FFTs are performed in order to put the image into the frequency domain. Here, it's easier to operate on and filter the image. After doing the forward FFT, the data could be filtered by a simple multiplication or just observed to see what the frequency content of that image is. Then, an inverse FFT could be performed to get back to the spatial domain with the filtered data. Because of

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### Product family highlights

Part #	Orgn	Speeds(ns)	Features
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ATT7C116	2Kx8	10,12,15, 20,25ns	Common I/O Output Enable
ATT7C166	16Kx4	10,12,15, 20,25ns	Common I/O Output Enable
ATT7C185	8Kx8	10,12,15, 20,25ns	Common I/O Output Enable Two Chip Enables
ATT7C174	8Kx8	12,15,20,25ns	Tag RAM, Flash Clear & Comparator
ATT7C183	2x4Kx16 or 8Kx16	25,35,45ns	Cache RAM for 386 Systems
ATT7C194	64Kx4	15,20,25ns	Common I/O
ATT7C199	32Kx8	12,15,20,25ns	Common I/O
ATT7C157	16Kx16	15,20,24,33ns	Synchronous



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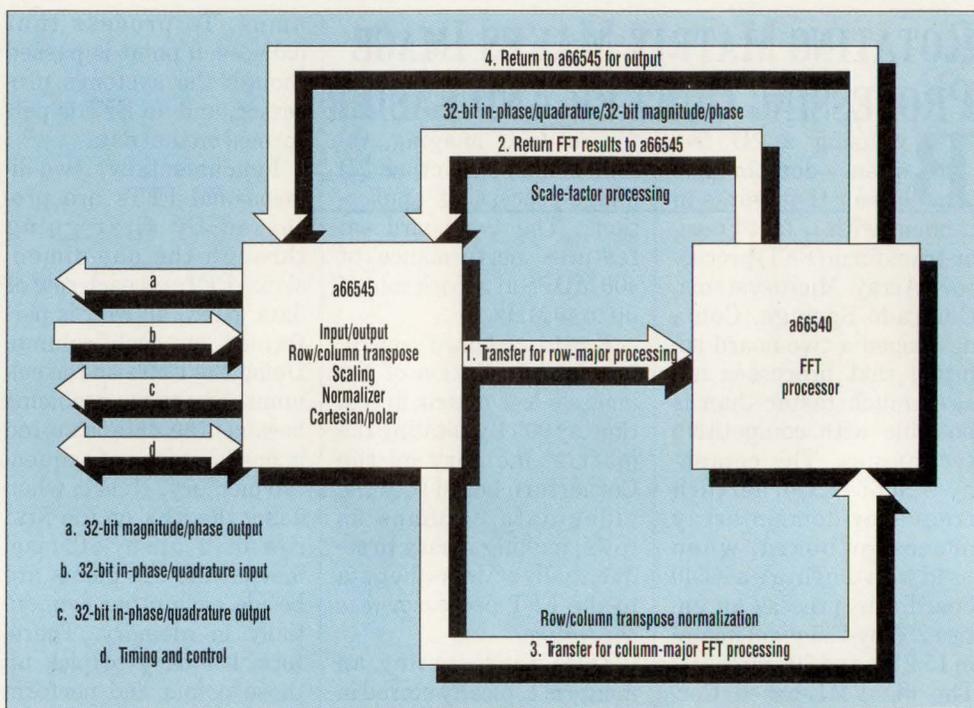
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the manner in which the image is set up, the inverse FFT could be executed using the same rotational procedure as the original FFT.

It's widely recognized that these operations should be performed in the frequency domain. Until now, though, it couldn't be done in real time. "Even with a TI 320-based DSP chip, it typically takes anywhere from tens of seconds to many minutes to do the transform," says Tony DiRenzo, vice president of board products at Array Microsystems.

To help speed up the image processing, methods were developed to perform some of the processing in the spatial domain. One technique is to do spatial convolutions. This involves taking a small 2D kernel, a 3-by-3 matrix, for example, and convolving it with the entire 512-by-512-pixel matrix. Because it's difficult to determine the coefficients in the spatial domain, this method isn't as effective or as precise as working in the frequency domain. Particular frequencies can't be extracted



as easily, so a lot of trial and error is probably required.

A good example of image processing is in today's frame grabbers and cameras. Most frame grabbers are monochrome (digitized gray scale), while most cameras are color. In the camera, color information is typically carried in a sub-carrier at around 3.5 MHz.

If a color image is digitized with a monochrome frame grabber, a herring-bone pattern will appear through the image representing that frequency. In the frequency domain, the 3.5-MHz subcarrier frequency could be notched out and brought back to the spatial domain, looking "clean as a whistle."

"With an i860-based so-

lution, people can get down to something on the order of 1 frame/s," says DiRenzo. That's a much slower rate than the 30-frame/s rate possible with the two-board Array Microsystem solution.

For more information on the Cornerturn array, contact Array Microsystems at (719) 540-7900.

RICHARD NASS

## MEMORY-CARD STANDARD EXPANDS TO INCLUDE I/O FUNCTIONS

Promising to change the designer's approach to portable-computer design as well as other applications, the just-released PC memory-card standard version 2.0, and the accompanying BIOS-level socket services software specification (release 1.0), provide a common definition to promote card interchangeability. Moreover, an extension that sits on top of the standard offers guidelines for add-

ing I/O functions, such as modems and network-interface cards, in the same 68-pin card slot that the memory cards plug into.

The latest release of the standard supersedes the previous version and has the full support of both the Personal Computer Memory Card International Association, Sunnyvale, Calif., and the Japan Electronic Industry Development Association, Tokyo, Japan. Both have over 150

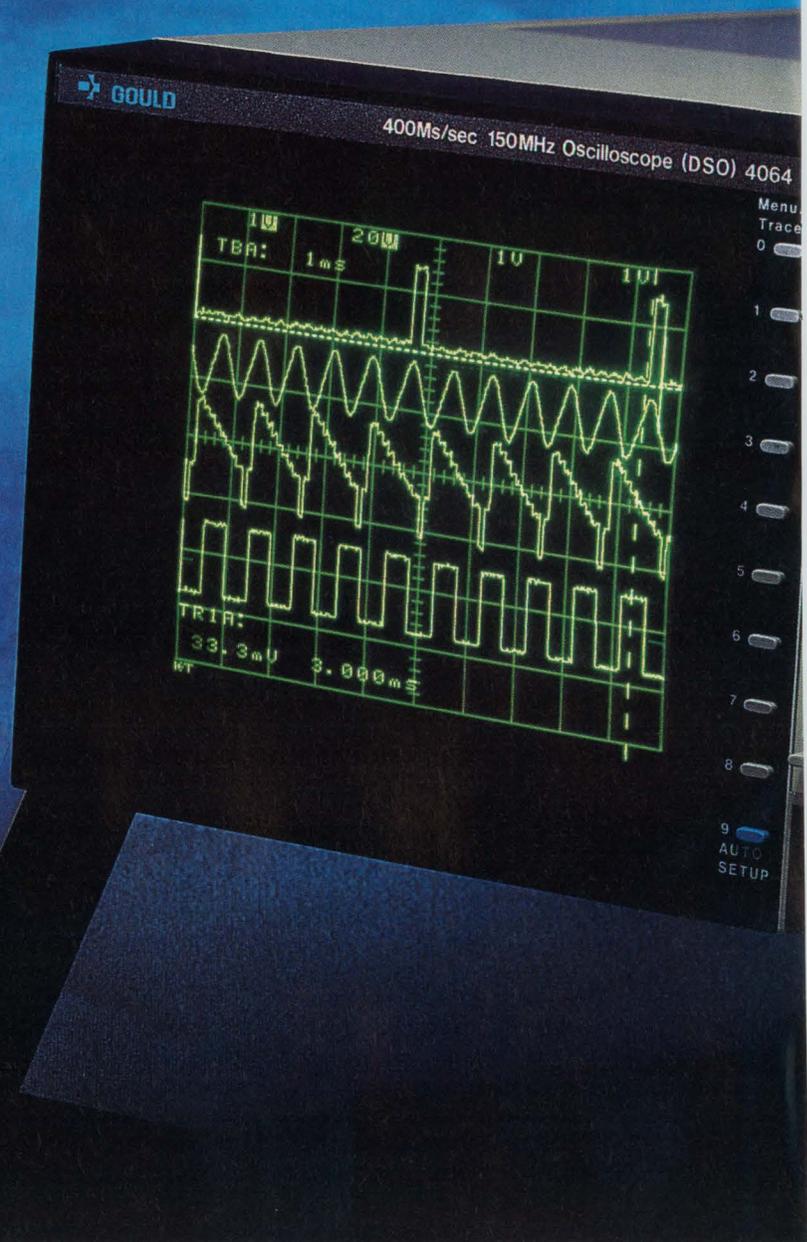
member firms and organizations. A chapter in Taipei, Taiwan has also been formed at the Institute for Information Industry.

Memory cards are practical replacements for floppy disks or other storage devices in applications that demand rugged, yet removable storage and I/O functions. Although the memory-card standard doesn't define the memory type inside the cards, it does define the physical

size and connector arrangement for the card, plus the pressure and torque for the connectors, pin functions, and power supplies. The latest version has extensions for dual-voltage operation (5 or 3.3 V), definitions for execute-in-place (XIP) software, improved memory performance, clearer definitions and explanations of memory-card functions, IEEE nomenclature for timing charts, and require-



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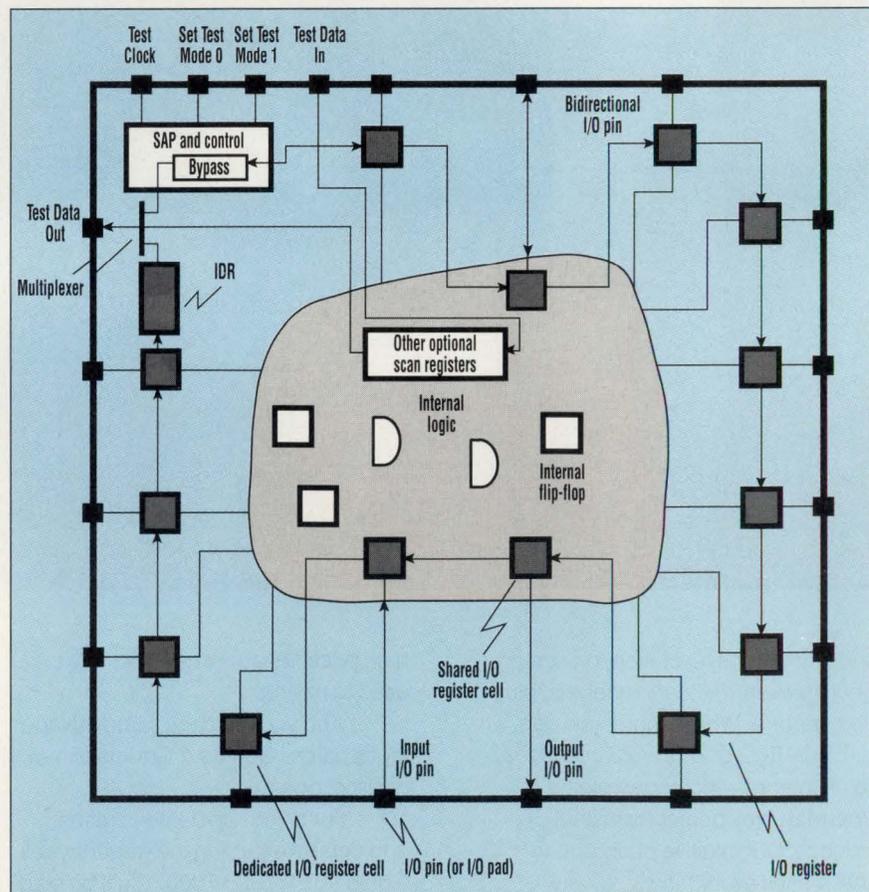
# ITC '91 FOCUSES ON TESTABILITY ISSUES

A JOINT MEETING OF TWO IEEE WORKING GROUPS HIGHLIGHTS DISCUSSIONS ON DESIGN-FOR-TEST AND CONCURRENT ENGINEERING.

JOHN NOVELLINO

**T**est: Faster, Better, Sooner—that's the theme of the 1991 International Test Conference, which offers attendees 128 papers, 17 tutorials, 6 panel sessions, and a poster session, all aimed at easing the burden of testing today's complex circuits. Papers will cover the latest techniques for reducing the cost and time devoted to testing designs. One strong point at this year's meeting is discussions of current and future design-for-test (DFT) techniques.

The three days of technical sessions at the Opryland Hotel and Convention Center kick off with a keynote address by Phil Robinson, president of Mentor Graphics' Concurrent Engineering Group. The opening plenary session also includes an invited paper by Frank Wright, manufacturing manager of Raytheon's Advanced Device Center. A highlight of this year's conference is a luncheon meeting on Monday co-hosted by the IEEE



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standard C code and allow fast test-program generation. In a typical configuration, the GR9000 costs \$225,000. Delivery is in 90 days.

**GenRad Inc., Concord, MA; (508) 369-4400. CIRCLE 506**



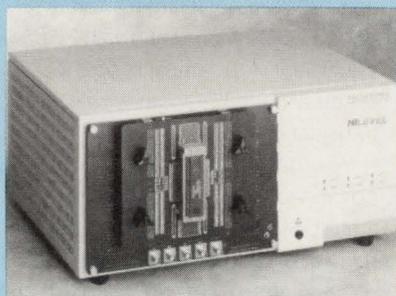
P1149.2 and P1149.3 Standards Working Groups. The groups are defining a test architecture and test interface, respectively, and will seek comments from attendees on the

groups' work to date.

In a repeat of a popular event at last year's ITC, the IEEE 1149.1 Working Group will hold an open meeting on Monday evening (Panel

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less than \$32,000. Field-programmable options include a dc parametric measurement unit, additional power sources, and added software utilities.

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■ Booth 1403

1). Last year's meeting highlighted the need for a language to facilitate the interchange of test patterns and diagnostic data during boundary-scan testing. Thus this year's discussion will revolve around the group's work on a language for describing standardized test logic for ICs.

The conference theme reflects the primary challenge to a maturing electronics industry, according to program chairman Kenneth Mandl. That is, how can engineers satisfy growing customer expectations of quality in an increasingly cost-competitive market? The technical program covers three broad areas: traditional electronic test topics, concurrent-engineering strategies and techniques, and the application of design and test techniques. The tutorials and professional group meetings will be held on the weekend of October 26-27. The technical sessions and exhibits are October 28-30.

Robinson's address will support the conference theme by describing how concurrent engineering can create designs that are easier and faster to test. He will talk about the paradigm shift needed to move test development to the earliest possible point in the product design cycle. The address will also cover how vendors and users of design automation have accepted the need for concurrent engineering and what steps they're taking to ensure its success.

On the other hand, Wright will explain to attendees how test and its database can support the analysis and synthesis of improvements to both the manufacture and design of semiconductors. Such improvements will ensure that semiconductor manufacturers, and their customers, will realize their goals of reduced device failures.

The meeting hosted by the P1149.2 and P1149.3 groups is meant to be an educational session rather than a working-group meeting. The IEEE 1149.1 boundary-scan standard published last year has received much publicity, and both working groups felt it was time to give the test-engineering community a status report on the progress of other standards work. But group leaders hope for an

## ITC '91 PREVIEW

interactive meeting, with attendees supplying feedback and adding new ideas to the mix.

The P1149.2 group's job is to develop a standard for scan-based testing of individual chips that can also be extended to the board and system levels. One important difference between IEEE 1149.1 and P1149.2 is that the former concentrated on boundary scan and merely provided the hooks needed for other techniques, such as internal scan. But according to Bulent Dervisoglu, who chairs the P1149.2 working group, the new standard will consider internal scan as essential. Dervisoglu is a consulting engineer at the Chelmsford Systems Laboratory in Hewlett-Packard's Workstation Systems Div., Chelmsford, Mass.

The P1149.2 standard will coexist with 1149.1, and will not replace it, says Dervisoglu. In fact, it will permit parallel as well as serial scan

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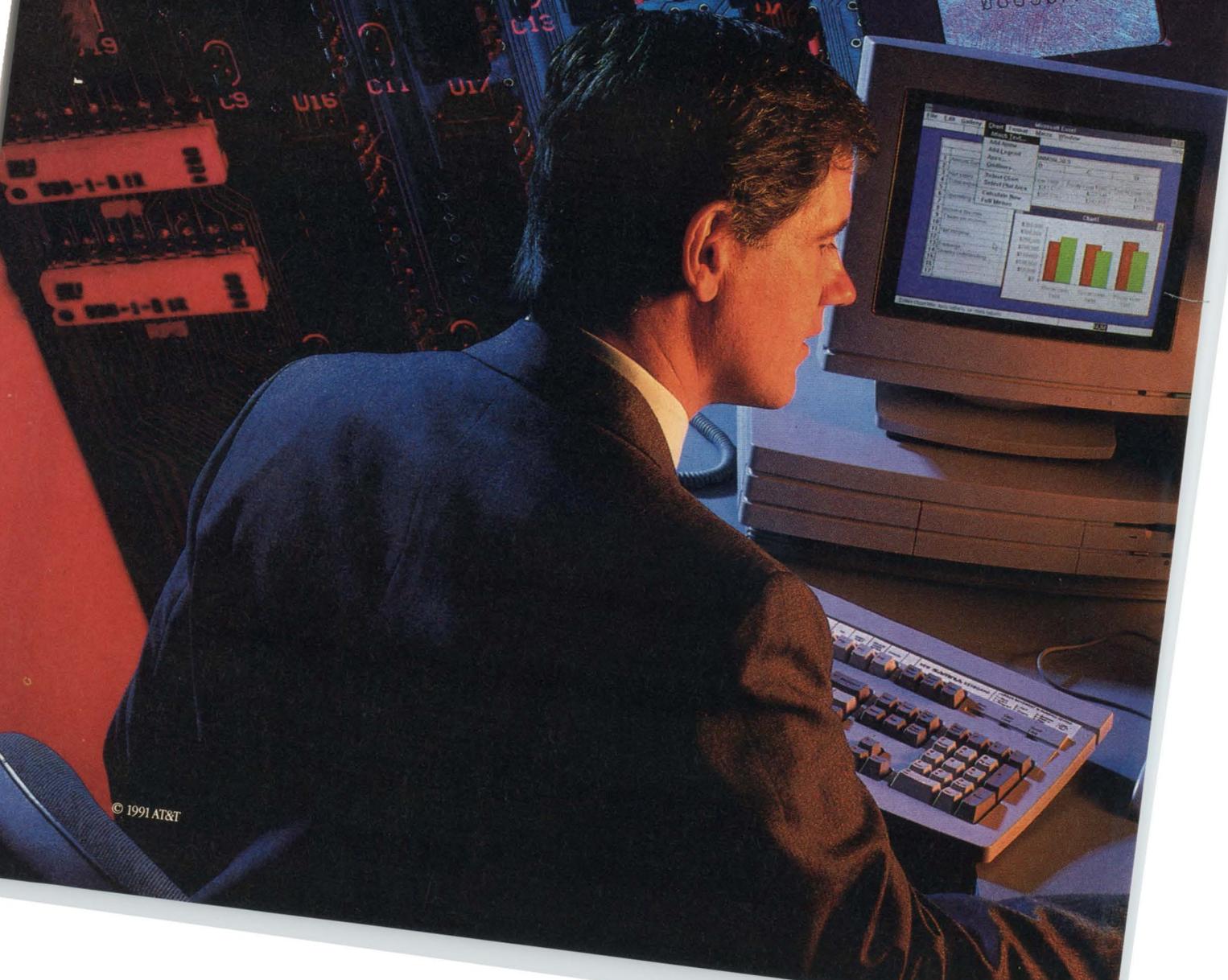
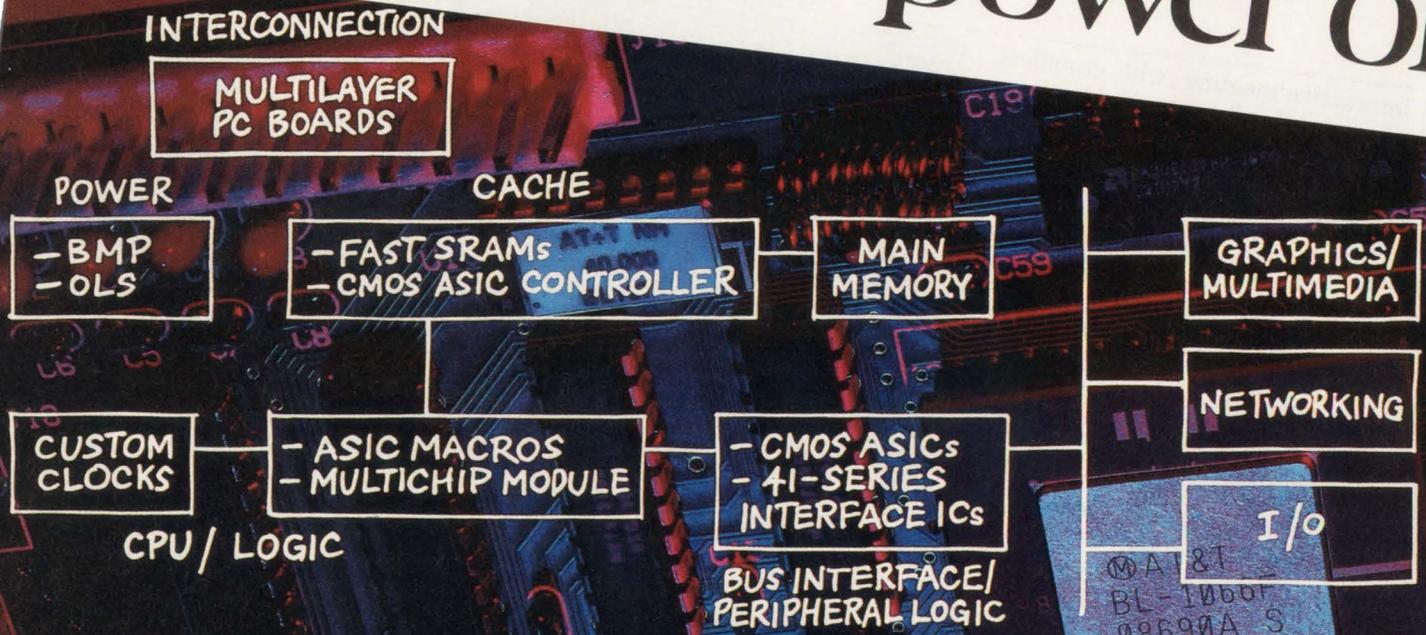
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## ITC '91 PREVIEW

chains for both internal and boundary scan, which is basically a chip-based technique that facilitates testing of board-level interconnections. But P1149.2 will require the minimal on-chip circuitry for boundary scan, leaving some aspects of 1149.1, such

as the parallel update stage, as options. "If, as a designer, you intend to solve your board-level problem in a slightly different way, then we should not force you to implement some of these features that 1149.1 includes," says Dervisoglu.

The boundary-scan standard uses a test-access port (TAP) controller that Dervisoglu says is too complex for some of the basic operations envisioned by P1149.2. As a result, the P1149.2 standard will implement a combinatorial scan-access port (SAP) controller. The basic SAP will need only two pins on the chip, but it can be extended to include additional test functions if the designer wishes. Other on-chip circuitry specified by the proposal includes an I/O register cell associated with each I/O pin, an Implementation Detail Register (IDR) for accessing implementation-specific features of the component or additional information about its testability features, and a bypass register for shifting scan data in or out of a multicomponent scan path (*see the figure*).

Meanwhile, the P1149.3 working group is defining a third type of testability bus. It's intended to be a family of buses under the umbrella of the overall 1149 effort. The P1149.3 standard was originally aimed at providing direct access between test resources and unit-under-test internal nodes in real-time or at-speed applications. That goal has been expanded, according to Fred Harrison, the working group's secretary and former chair.

"It's taking on several functions," says Harrison. "One is to give that direct access into a circuit, so that you can either generate a signal into a node or read a signal at a node in real time. The second area or responsibility that it's taking on is to act as an interface with buses like 1149.1 and P1149.2." For instance, a board might have two 1149.1 boundary-scan chains and a P1149.2 internal-scan chain. A P1149.3 bus would then supply the interface or channel through which the test resources could access those chains.

The 1149 subdivisions grew out of a realization that boundary scan has limitations, according to Harrison, who is president of C&H Engineering in Austin, Texas. "What many of us—and this is not a unanimous opinion—wanted to see was a multiplicity of ways to help people address the test problem," he says. The P1149.3

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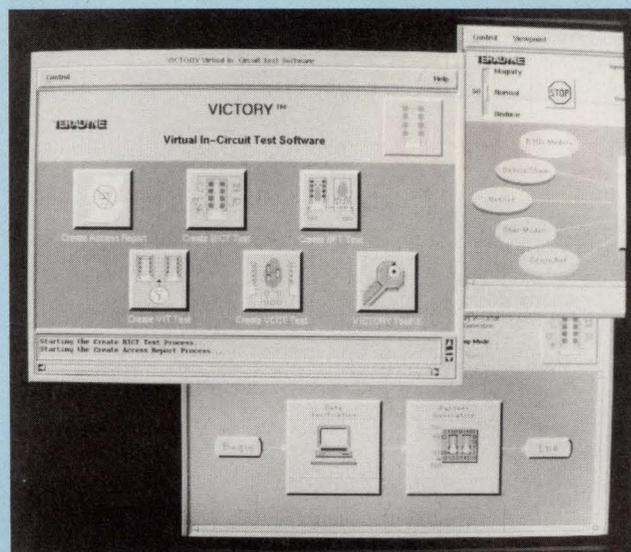
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## MODULES ENHANCE BOUNDARY-SCAN SOFTWARE

**T**wo new software modules and a process-oriented graphical user interface based on Windows 3.0 have been added to a software package for testing printed-circuit boards with boundary-scan devices. The Victory 2.0 release includes the Virtual Component/Cluster Test (VCCT) module, which allows the boundary register to be used as virtual channels to test non-boundary-scan devices that can't be accessed by a bed-of-nails fixture. In addition, the Boundary Functional Test (BFT) module lets users test the internal circuitry of individual boundary-scan devices. Using Boundary-Scan Description Language device data and circuit board netlists, Victory 2.0 generates tests for Teradyne's L-series testers. Victory 2.0, which runs on VAX and PC platforms, can be ordered now. Prices start at \$5000.

**Teradyne Inc., Boston, MA; (617) 482-2700. CIRCLE 509**

■ Booth 703



document will create testability features that designers can place on their boards or in their systems. It will not require on-chip circuitry, as boundary scan does, although that will be an option.

The open meeting of the IEEE 1149.1 group is only one of six panels. Another panel that should draw interest is Software Testing: State of the Practice. Panel members will describe current practices used for software testing, focusing on their successful experiences. A third panel will look at the acceptance barriers confronting DFT and built-in self-test (BIST). Members will discuss

possible reasons for a continuing reluctance on the part of some designers to incorporate DFT and BIST into their circuits. The three remaining panels will address the question of whether IC burn-in testing is still required and will discuss trends in automotive electronics testing and the need for education in test engineering.

DFT and BIST also get extensive treatment in the tutorials, with eight of the sessions emphasizing one or both of those techniques. A two-session tutorial, Advanced Techniques in Testing (tutorials 4 and 12), concentrates on fault simulation and

DFT on the first day and on automatic test generation (ATG) and BIST on day two. In the first-day session, the discussion starts with fault-simulation procedures that offer differing trade-offs between generality and efficiency. The DFT portion involves advanced scan techniques dealing with partial scan, the design and optimization of multiple scan chains, and boundary scan (IEEE 1149.1).

The second session reviews ATG concepts, then discusses techniques used in advanced ATG systems for such tasks as accelerating ATG algorithms, selecting and targeting faults, fault-independent test generation, integrating different test-generation methods, and others. The BIST portion begins with a brief overview of compression techniques.

Built-in Self-Test I and II (tutorials 1 and 9) will describe the state of the art in the technology. The first session addresses the technical issues of BIST using pseudorandom inputs. Subjects in the second session include diagnostic aids for signature test, an improved cutting algorithm, partitioning for test, and ac test. □

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streaming tape backup. The test cycle is an integer multiple of the system reference clock, with a clock period between 20 and 40 ns. The tester features multiple edges per pin, on-the-fly switching, and multiple parametric measurement units. The 212 will be available in production quantities at the end of the first quarter of 1992. Prices range from \$2500 to \$3500 per pin, depending on configuration.

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# 12-BIT IC ADCS SAMPLE SIGNALS AT UP TO 20 MHz

FRANK GOODENOUGH

**T**he integration of discrete and hybrid devices into monolithic form continues at a breakneck pace, especially in analog-to-digital and digital-to-analog converters. Just over a year ago, for example, the cover of *ELECTRONIC DESIGN* announced the first 12-bit ADCs, 1-by-2-in. chip-and-wire hybrids that sample at 20 MHz. Even 10-MHz-sampling-rate ADCs were hybrids then (*ELECTRONIC DESIGN*, Sept. 13, 1990, p. 47). Such hybrids were less than three years old, replacing board-level ADCs of 5 by 7 in. Now Signal Processing Technologies (SPT), formerly a division of Honeywell, and Analog Devices (ADI), have each come up with monolithic 12-bit ADCs that sample at 10 and 20 MHz (Fig. 1).

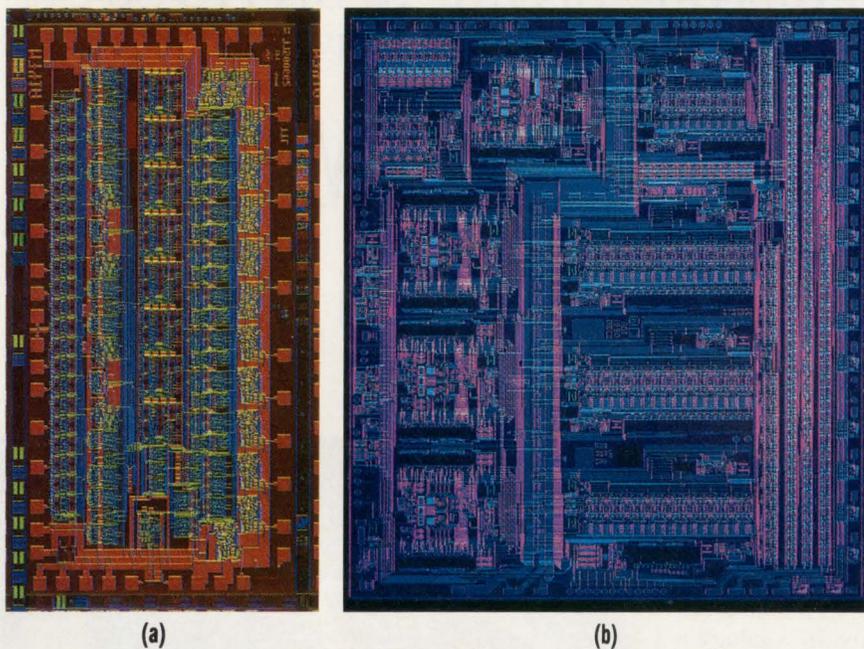
The SPT7912 from SPT produces 12-bit digital words of sampled analog voltages at 20 MHz, while the ADI AD872 does the same at 10 MHz. In addition, each sports one or more 10-bit kid brothers that employ similar architectures. SPT's 10-bit, SPT7814 samples and converts at 40 MHz, and its 7810 samples at 20 MHz. ADI's 10-bit AD773 runs at 18 MHz. The SPT 10-bit converters arrived a bit ahead of the 12-bit version (*ELECTRONIC DESIGN*, June 27, p. 153). In addition to smaller size and lower cost, the 12-bit IC converters typically use an order-of-magnitude less power.

Both the ADI and the SPT converters employ pipelined, multistep architectures (see "Stepping through the pipe," p. 58). But there's little to compare them with architecturally. That's because both families represent the first standard-product IC (or hybrid) ADCs that use more than two conversion steps in their operation (the exception is ADI's AD671, a non-sampling 12-bit, 2-MHz design that uses four steps). The proprietary



(patented) architecture of the SPT converters employs a set of algorithms called "trigonometric interpolation," creating a whole new ball game in high-speed, greater-than-8-bit ADC design (Fig. 2). On the other hand, the 3-step/4-step (10-bit/12-bit) ADI architecture might be considered conventional because it's an extension of most present two-step designs, although it incorporates numerous patented circuit-design innovations (Fig. 3).

# 12-BIT 10/20-MHz-SAMPLING-RATE ADCs



**1. ADVANCED FINE-LINE PROCESSES** have made possible two 12-bit analog-to-digital converters that sample at high frequencies in monolithic form. The SPT7912 from Signal Processing Technologies is a 16,600-mil<sup>2</sup> bipolar chip with 2000 transistors that samples at 20 MHz (a). The AD872 from Analog Devices is an even denser 75,000-mil<sup>2</sup> bipolar-CMOS chip with 11,000 transistors that samples at 10 MHz (b).

All five ADC specifications are spelled out (*see the table*).

Sampling 12 bits at 10 or 20 MHz produces signals with a tremendous amount of resolution. Therefore, the question arises: Where can such ADCs find applications? Recording and TV studios, doctor offices, electronics labs, and even some homes use high-sampling-rate ADCs. Communications links and police cars also use them. But these applications generally have 8 and 10 bits of resolution. Still, they presently use large and bulky devices that dissipate much power and have prohibitive price tags. Now that integration (and its attendant lower costs) has put the price of ADCs within reach of more users, the new ADCs may find homes in these applications as well as challenge the imagination of system designers, since their price-performance lends them to over and under-sampling applications.

While there's a dichotomy between 10- and 12-bit ADC applications, significant overlapping will occur, depending on cost-performance trade-offs. Today, 10-bit devices are

a natural for professional video; tomorrow they'll be needed for high-definition TV (HDTV), machine vision, and potentially even camcorders. They'll also find their way into oscilloscopes, spectrum analyzers, industrial and medical imaging, various military systems.

The 12-bit converters will find homes in sophisticated spread-spectrum radio and radar receivers, where they'll join direct-digital-synthesis (DDS) DACs in the reception, reconstruction, and generation of analog waveforms (*ELECTRONIC DESIGN, Sept. 12, p. 63*). They'll also be used in infrared (IR) imaging systems that use focal-plane-array ICs with one sensor/pixel. The output of the array is multiplexed, pixel-by-pixel, into the ADC. While the bandwidth of each sampled input is relatively low, the desired data rate is high for motion-detection applications using a large 360,000-pixel (600-by-600) array.

Each SPT converter requires just 20 full-time comparators and 21 additional circuits that perform part-time comparisons. The output is also com-

pletely free of sparkle codes. Following a low-capacitance-input (5-pF) buffer, a four-bit flash converter produces the four most-significant bits (MSBs). It also eliminates the input signal's need to remain constant while waiting for the remaining portions of the circuit to settle.

In parallel with the flash converter, an analog circuit called the "analog gain-compression processor" (a prescaler) transforms the input signal into a waveform for further processing by trigonometric algorithms. The ADC also does the job of the DAC and summing amplifier found in conventional subranging ADCs, and does it without latching the digital word or reconstructing the analog signal with a DAC.

After the initial analog-processing step, the signal enters a bank of sample-and-hold amplifiers (SHAs) that sequentially feed an array of interpolators to produce the eight least-significant bits (LSBs). This technique is somewhat analogous to a successive-approximation-register (SAR) converter. Within the converter, time delays between the analog signals and the interpolator outputs, and the propagation time of digital words to the latches at the output of the 4-bit flash, become significant as the input signal's slew rate rises with its frequency. The problem stems from disagreements between comparators in successive stages of the conversion process in detecting the same input-signal level. Patented error-correction/decoding circuits fix this problem by letting early stages enable logic transitions. Later stages, where the LSBs are decoded, act on those transitions.

The bank of SHAs between the analog processor and the interpolators reduces the need for a fast 12-bit-accurate SHA on the front-end of the ADC. That's because the internal SHAs pipeline out the delays through the relatively slow interpolators. The converter's speed is limited only by the 4-bit input-flash ADC and the bandwidth of the analog processor, both of which multiply the frequency before it reaches the SHAs. Frequency (gain-bandwidth) multiplication represents a generic

# 12-BIT 10/20-MHz-SAMPLING-RATE ADCs

problem. It limits the performance of all multistep-architecture ADCs, including the SAR. Each additional stage in any multistep ADC doubles the small-signal bandwidth requirement, albeit reducing the accuracy of that stage by a similar factor.

Frequency multiplication (and complexity not easily handled by hybrids) has restricted earlier subranging converters to two steps, preventing optimization of device size and power. Most two-step hybrids add a SHA on the front-end, reducing ADC bandwidth so that it settles to a given accuracy within a given time (including the SHA's settling). The SHA must settle rapidly and accurately while driving the high and usually code-dependent input capacitance of a 6-to-8-bit flash ADC, making it difficult to produce at reasonable cost and power.

Adding SHAs after the compression stage eases the accuracy and signal-swing requirements of the SHAs while they pipeline out the slow interpolators. Like most high-speed SHAs, those on the SPT chips treat errors due to charge injection, droop, settling time into hold, and clock jitter, as common-mode effects and eliminate them at the input to the interpolators, at the expense of bandwidth-limiting, frequency-multiplication effects in the input compression stage. But the low input capacitance reduces drive requirements and lowers the demands on an external SHA if a user decides to add one to improve dynamic performance. The interpolators further reduce the total number of active devices (relative to earlier designs) and thus reduce power dissipation.

Like the SPT converters, the ADI converters also add SHAs. The AD872 and AD773 represent four- and three-step versions, respectively, of the conventional two-step ADC. In the 12-bit AD872, a pair of stages (steps) precede the basic two-step elements described in "Stepping through the pipe" (Fig. 3, again). Each ADC consists of a SHA, a flash ADC (quantizer), a DAC, and a gain-producing residue-current-summing network. The first stage of the 12-bit AD872 uses a 3-bit flash ADC, which has to supply only

## 10- AND 12-BIT MONOLITHIC ADCs SAMPLING AT 10 TO 40 MHz

Model	Units	SPT9712	SPT7814	SPT7810	AD872	AD773
<b>Conditions for specifications</b>						
Over temperature	Y/N	N	N	N	Y	Y
Sampling rate	MHz	20	40	20	10	18
Input signal	V	2	2	2	1	0.5
Supply rails	V	--(+5 and -5.2)--			( +5, +5, -5)	
<b>Specification</b>						
<b>Resolution</b>	bits	12	10	10	12	10
<b>Dc accuracy</b>						
Differential nonlinearity (25°C)	±LSB	0.5(t)	0.5(t)	0.5(t)	0.5(t)	0.5(t)
Differential nonlinearity (OT)	±LSB	NS	NS	NS	1	1
No missing codes	Y/N	Y	Y	Y	Y	Y
<b>Input</b>						
Resistance (t)	kΩ	300	300	300	50	50
Capacitance (t)	pF	5	5	5	10	10
<b>Power dissipation</b>	W	1.8	1.8	1.8	1.2(t)	1.4
<b>Ac specifications</b>						
<b>Effective number of bits (ENOB)</b>						
$f_{in} = 1$ MHz	NA	10.7(t)	9(t)	8.7(t)	11.3(t)	9.2(t)
$f_{in} = 3.58$ MHz	NA	9.5(t)	8.8(t)	8.7(t)	NS	NS
$f_{in} = 8.1$ MHz	NA	NS	NS	NS	NS	8.7(t)
$f_{in} = 9$ MHz	NA	NS	NS	NS	NS	8.5(t)
$f_{in} = 10.3$ MHz	NA	TBD	7.5(t)	7.3(t)	NS	NS
<b>Signal-to-noise ratio without harmonics</b>						
$f_{in} = 1$ MHz	dB	68 (t)	57	55	NS	NS
$f_{in} = 3.58$ MHz	dB	67 (t)	56	55	NS	NS
$f_{in} = 10.3$ MHz	dB	TBD	50	48	NS	NS
<b>Total dynamic error (TDE)</b>						
$f_{in} = 1$ MHz	dB	66 (t)	52	55	NS	NS
$f_{in} = 3.58$ MHz	dB	59 (t)	52	54	NS	NS
$f_{in} = 10.3$ MHz	dB	TBD	44	44	NS	NS
<b>Signal-to-(noise + distortion), (S/(N + D))</b>						
$f_{in} = 1$ MHz	dB	NS	NS	NS	67	52
$f_{in} = 4.99/8.1$ MHz	dB	NS	NS	NS	65	NS
$f_{in} = 8.1$ MHz	dB	NS	NS	NS	NS	50
$f_{in} = 9$ MHz	dB	NS	NS	NS	NS	46
<b>Total harmonic distortion (THD)</b>						
$f_{in} = 1$ MHz	-dB	66 (t)	57	54	68,72(t)	58,64(t)
$f_{in} = 3.58$ MHz	-dB	62 (t)	56	52	NS	NS
$f_{in} = 4.99$ MHz	-dB	NS	NS	NS	64	NS
$f_{in} = 9$ MHz	-dB	NS	NS	NS	NS	47,56(t)
$f_{in} = 10.3$ MHz	-dB	TBD	46,48(t)	46,48(t)	NS	NS
<b>Spurious-free dynamic range (SFDR)</b>						
$f_{in} = 1$ MHz	-dB	70(t)	70(t)	70(t)	65	67(t)
$f_{in} = 3.58$ MHz	-dB	TBD	NS	NS	NS	NS
$f_{in} = 4.99$ MHz	-dB	NS	NS	NS	70	NS
$f_{in} = 10.3$ MHz	-dB	TBD	NS	NS	NS	NS
<b>Intermodulation distortion (IMD)</b> ( $f_{in} = 1.0$ MHz and 1.05 MHz)						
Second-order products	dB	NS	NS	NS	NS	69(t)
Third-order products	dB	NS	NS	NS	NS	63(t)
<b>Input bandwidth (-3 dB)</b>						
Small-signal (t)	MHz	120	120	120	75	NS
Full-power (t)	MHz	NS	NS	NS	50	100
<b>Aperture jitter (t)</b>	ps rms	5	5	5	10	10
<b>Differential phase</b>	Degrees	NS	NS	NS	NS	0.2
<b>Differential gain</b>	%	NS	NS	NS	NS	0.8
<b>Pipeline delay (latency) clock cycles</b>		1	1	1	3	4
<b>Price (100s)</b>		\$385	\$109	\$99	\$185	\$55

All specifications are maximums or minimums unless noted typical (t). OT = over temperature. TBD = to be determined. NS = not specified. NA = not applicable.

# 12-BIT 10/20-MHz-SAMPLING-RATE ADCs

4-bit accuracy. However, the SHA and DAC must be 12-bit accurate. The remaining stages use 4-bit flash ADCs and DACs. The 12-bit device uses a total of 56 comparators.

The secret behind the AD872's performance, besides pipelining, is several innovative analog circuit techniques in and between blocks. Most are described in detail in the IEEE Journal of Solid-State Circuits (Vol. 26, No. 8, Aug. 1991, p. 1103). In pipelining, steps one and three can acquire new samples from the input and the previous step respectively, while steps two and four quantize signals acquired from previous steps. At the next clock cycle, steps one and three quantize the signals they've just acquired, while steps two and four obtain new samples.

The handling of signals as currents and voltages represents the major circuit innovation used to process pipe signals (Fig. 3, again). While the SHAs must drive the quantizers with voltages, the SHAs' unique circuits also take current signals from the summing networks and provide current-output signals to those networks. This enables low-impedance, current-summing techniques to generate the residue signals. Speed climbs with no capacitance to charge.

Implementing interstage gain in an open-loop manner with scaled current sources also avoids gain-bandwidth (frequency multiplication) effects that usually limit sampling rates in subranging ADCs. Interstage gain is determined by laser-trimming resistors to set the values of the current sources. This gain maintains reasonable input-signal levels for the second and third quan-

tizers and substantially reduces the noise from the second, third, and fourth stages. Errors are minimized by using differential circuits from the input SHA through the fourth quantizer's outputs.

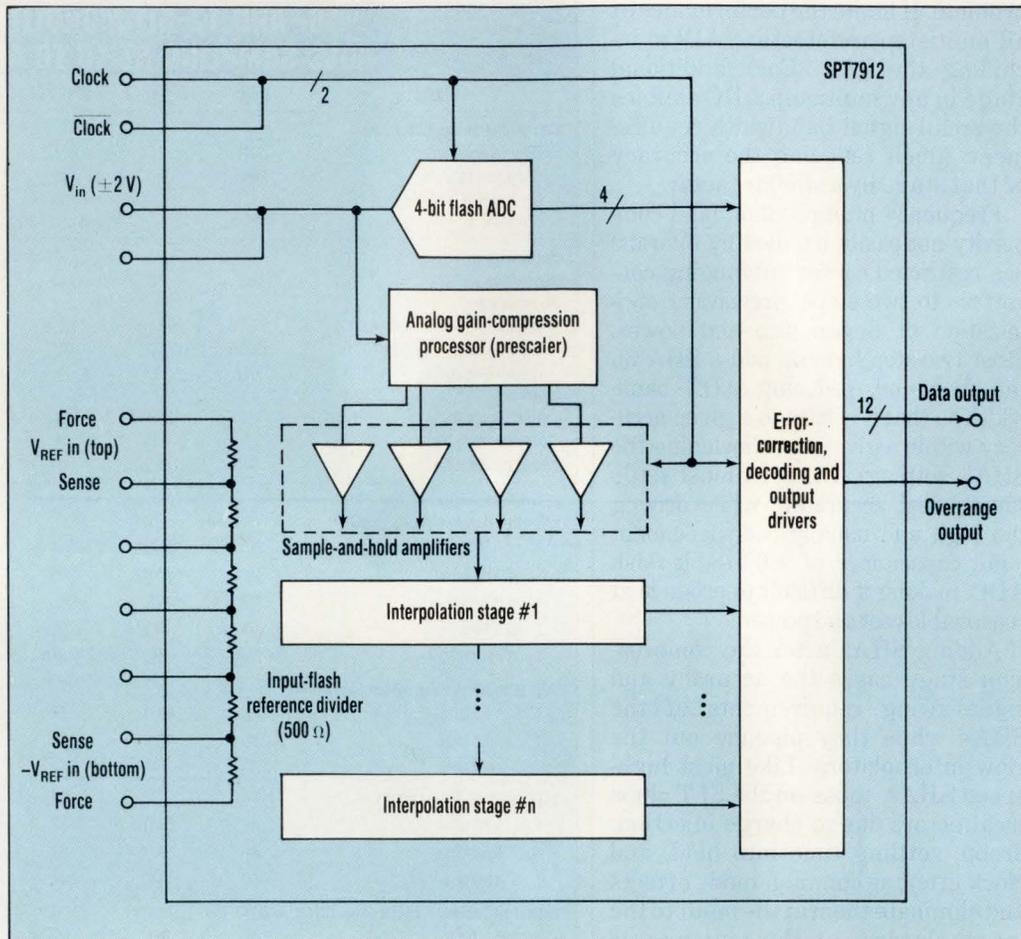
Adding the overlapping digital (binary) words from the four quantizers results in digital error correction being performed in the following manner:

```

Digital words
step 1 = AAA
step 2 = BBBB
step 3 = CCCC
step 4 = DDDD
    
```

```

Binary sum =
XXXXXXXXXXXXXXXX
The final result is the converter's
12-bit output word plus the over-
    
```



**2. SAMPLING SIGNALS AT 20 MHz**, this 12-bit ADC's flash circuit provides the 4 most-significant bits. A series of interpolators offer the 8 least-significant bits.

range bit. Because the converter takes a bipolar analog input voltage, looking at the overrange bit and the MSB determines if the overrange is positive or negative.

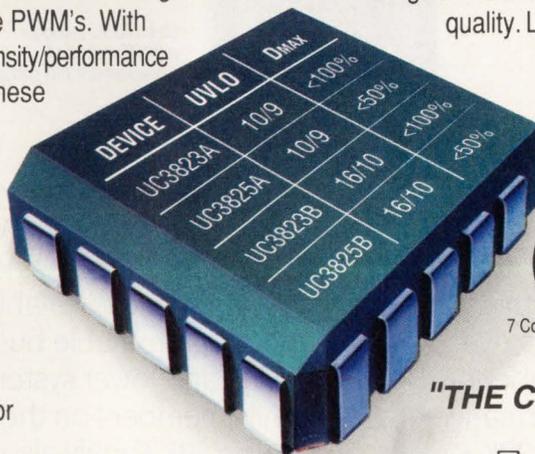
Aside from being easy to drive (5 to 10 pF of input capacitance and an input resistance over 50 kΩ), needing both plus and minus 5-V supplies, and providing an overrange output, the two families of converters share little in pins-out characteristics, including many specifications (see the table and Figs. 2 and 3, again). Even devices within the families differ in more than just resolution and/or sampling rate. For example, the ADI units are TTL/CMOS-compatible while the initial SPT ADCs use ECL. However, SPT converters using TTL will soon be available; they will use 300 mW less power or about 1.5 W. For specified performance,

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## 12-BIT 10/20-MHz-SAMPLING-RATE ADCs

the SPT units need a  $\pm 2$ -V full-scale input while the AD872 only needs  $\pm 1$  V, and the AD773, only  $\pm 500$  mV.

The SPT converters have two signal-input pins. They connect on-chip to drive a single-ended 300-k $\Omega$ /5-pF impedance circuit. They can also be used together with an op amp to implement a force-sense-type input. The two inputs to both ADI converters, on the other hand, are true differential inputs specified as 50-k $\Omega$  resistances. Converters from either family should be easy to drive with many op amps or doubly terminated transmission lines.

The AD872 alone carries its own voltage reference, and can be used for a system reference. An external reference can also be used. Conversely, the 500- $\Omega$  internal reference ladder inside the SPT converters must be driven, with plus and minus 2.5 V at the top and bottom, respectively, from a low-impedance source, such as an op amp. To ensure 12-bit accuracy, the SPT7912 provides both

force and sense input nodes at the top and bottom of the ladder. Moreover, because these pins can be driven with a variable voltage permitting changes in full-scale signal on the fly, the SPT7912 can be considered a multiplying ADC (changing the reference varies the full-scale signal). In fact, the bandwidth of the reference ladder typically runs 50 MHz.

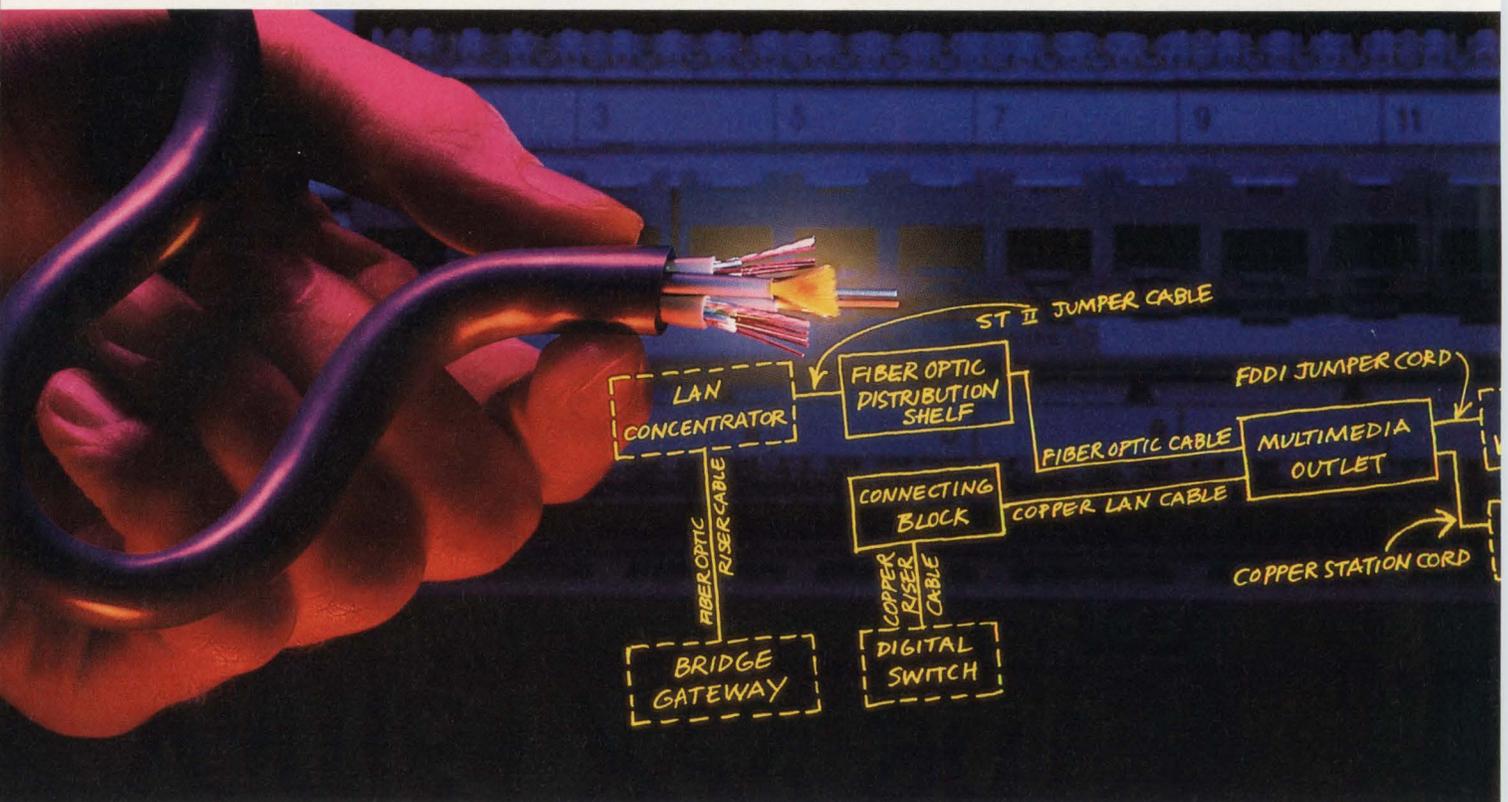
Comparing the specifications of these converters isn't a trivial task for several reasons. To start, Analog Devices has joined the growing (and very popular with the user) trend of adding minimum ( $t_{\min}$ ) to maximum ( $t_{\max}$ ) temperatures to the basic conditions for all specifications called out at the top of the data sheet. SPT data sheets, though, list 25°C as the temperature for the specifications (the final data sheet will also call out  $t_{\min}$  to  $t_{\max}$  as a condition for the specifications). In addition, because sampling rates run between 10 and 40 MHz, a different set of input-signal frequencies are used to define the ac

(dynamic) specifications of each converter. And ADI specifies signal-to-(noise + distortion), or S/(N+D), while SPT specifies total dynamic error (TDE) and signal-to-noise ratio (without harmonics). According to SPT, TDE is similar to S/(N+D).

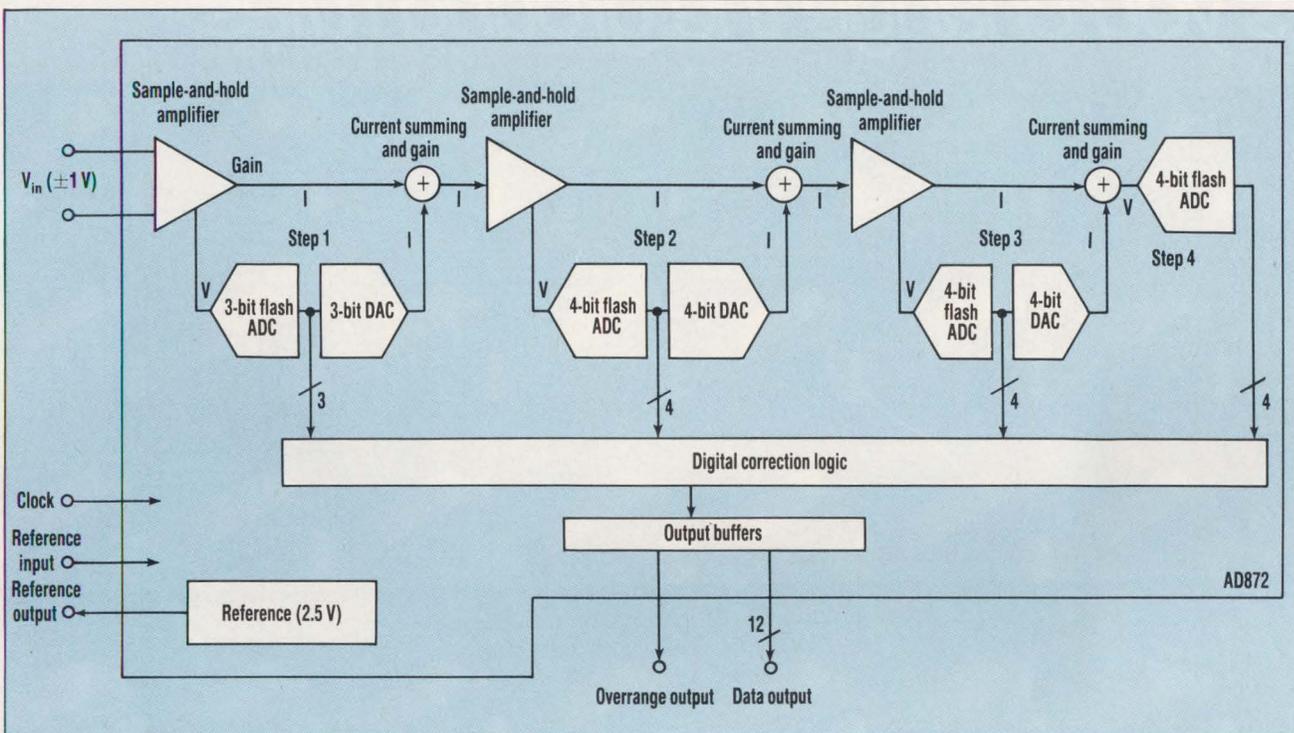
In addition, although both companies are sampling their converters, these new ICs aren't fully characterized, particularly for the dynamic specifications that require a rigorous and time-consuming task to obtain. For example, only the AD773 offers values for differential phase and gain, or for a spurious-free dynamic range. The first two specifications are vital for 10-bit video applications; the last specification is important for 12-bit receivers.

While innovative designers fought the limitations of physics to successfully overcome effects that made these ADCs "theoretically" impossible to design, they would've still been impossible to produce without access to high-speed analog semicon-

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## 12-BIT 10/20-MHz-SAMPLING-RATE ADCs



**3. THE SAMPLE-AND-HOLD AMPLIFIER** on the input of this 12-bit/10-MHz, 4-step ADC, and the first DAC stage, must be 12-bit accurate. But the 3-bit flash circuit need only be 4-bit accurate.

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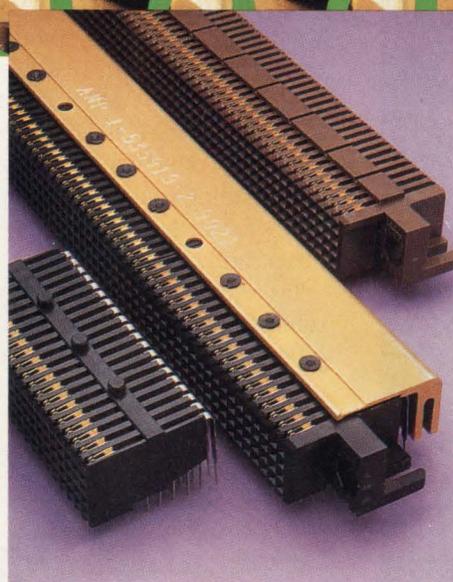
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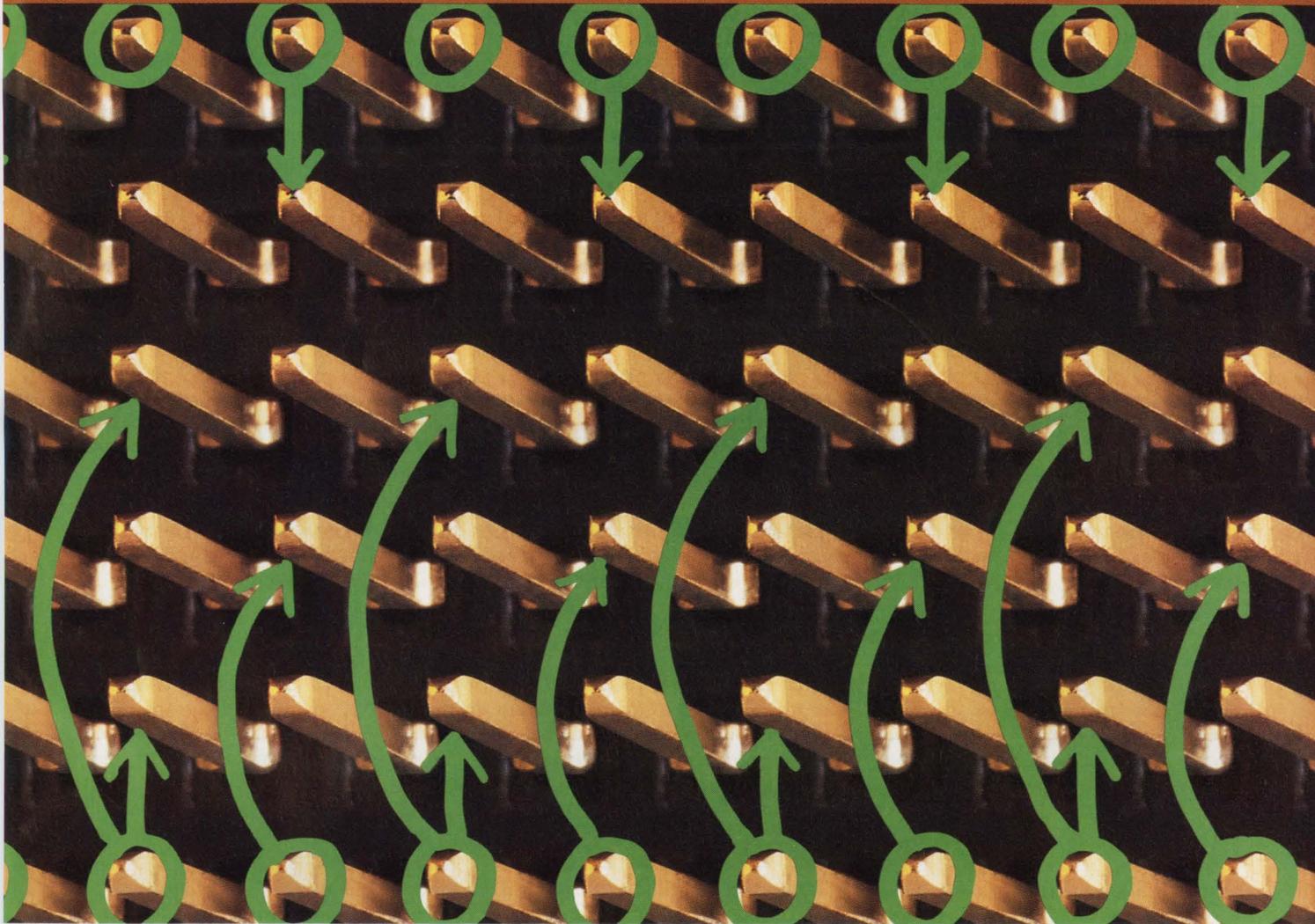
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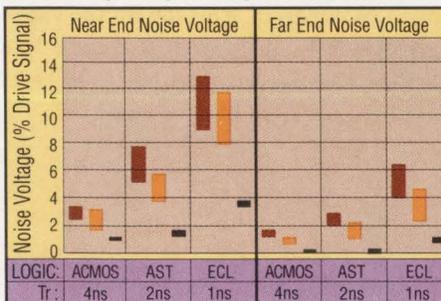
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*Note: performance of AMP TBC Plus connectors with evenly dispersed 'checkerboard' grounding; some competitive styles don't allow this.*



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## 12-BIT 10/20-MHz-SAMPLING-RATE ADCs

ductor processes on which to build them. The ADI chips are built on a fine-line (2- $\mu$ m), advanced bipolar-CMOS process called ABCMOS. The  $f_T$  of its npn transistors runs 2 to 3 GHz. Moreover, although the process needs 19 mask steps, including laser-trimmable thin-film resistors, it's not a laboratory or pilot-line process. Instead, it's a robust commercial technology that ADI builds on for its audio DACs in CD players.

The density of the process lets the 12-bit AD872's designers squeeze its 11,000 transistors (about six times that of a 574) on a 75,000-mil<sup>2</sup> die (just over 0.25 in. on a side). Both of the

ADI converters were developed under a contract for the U.S. Army Strategic Defense Command. Minimum modifications of the commercial process flow, and the addition of several mask steps, create a radiation-tolerant version of the process called RBCMOS. Moreover, a common set of layout rules allows the same layout database to generate masks for devices, such as the AD872, to be built on either process.

The SPT converters are fabricated on a very high speed, fine-geometry non-complementary, bipolar process that, like ABCMOS, has access to laser-trimmable thin-film resistors.

The 12-bit ADC employs just 2000 transistors on a tiny 16,600-mil<sup>2</sup> (89 by 187 mils) chip.

Like most complex, high-speed, mixed-signal devices, the "simple" job of hooking up and testing the ADCs turns out to be fairly complicated. To make the job of evaluation easier for the user, both ADI and SPT created evaluation boards containing, at a minimum, a reconstruction DAC, a reference, and interface circuitry. SPT's board is somewhat more complex and comes with a 15-page application note. Analog Devices makes their boards, along with a converter, available to potential us-

### STEPPING THROUGH THE PIPE

**A**DC architectures break down into several classes for resolution and speed. Each class represents a compromise between the number of comparators, clock cycles, and sample-and-hold amplifiers (SHAs), if any. The more comparators, the faster the device, but also the larger and more costly it becomes. Adding clock cycles sacrifices speed but cuts the number of comparators and usually simplifies the device. SHAs add sampling to the ADC (theoretically an ADC without sampling is merely a quantizer), which permits the quantizing of fast-changing signals and makes pipelined converters possible. The "right" SHA can up the performance of virtually any ADC.

Flash ADCs, the fastest quantizers, employ  $2^n - 1$  comparators, where  $n$  is the resolution in bits, but they take only *one* clock cycle. A 12-bit flash ADC would take  $4096 - 1$  comparators. So far, practicality has limited them to 10-bit resolution. Integrating, tracking, and successive-approximation-register (SAR) converters take just *one* comparator. However, their clock cycles range from  $n$  for the SAR to over  $2^n$  for the integrating converter. Other architectures use a comparator and a clock cycle per bit of resolution.

Basically, a multistep (often

called multipass or subranging) converter combines the speed of the flash, with the multiple clock cycles of the other designs. Though most multistep converters have applied their input signal sequentially to two or more flash ADCs (or to a single flash two or more times), one or more flash circuits could be used with any of the other architectures or with a new one (the SPT converters).

In a multistep converter, the sum of the resolution of each step is equal to or greater than the specified resolution of the complete converter. For example, a 12-bit two-step ADC might use two, 6-bit flash ADCs and thus require just 126 comparators (until now, most multistep ADCs have been two-step devices, often called half-flash ADCs). However, most multistep converters (and all those with 12-bit or greater resolution) employ digital error correction. The sum of the resolutions of their two or more flash circuits exceeds the specified resolution of the complete converter, usually by one or more bits.

A typical 12-bit two-step ADC consists of a 6- and an 8-bit flash ADC, a 12-bit-accurate 6-bit DAC, a summing circuit with (or followed by) gain, and digital-correction logic stages (see the figure, a). The input voltage  $V_{in}$  is applied to the input of the 6-bit flash. At

the Convert command, the clock strobes its 127 comparators. The six output lines are fed to the DAC and the digital-correction logic.

The combination of a 12-bit-accurate DAC and digital error correction relieves the flash's fast comparators from having to provide 12-bit accuracy—it's easier to build fast, 12-bit-accurate DACs than fast, 12-bit-accurate comparators. The output of the DAC is summed with the input signal. The difference (often called the residue) is gained up by amplifier A whose maximum output voltage equals the full-scale input voltage of the 8-bit flash. The 8-bit circuit's 255 comparators are strobed by a second clock pulse, and its 8-bit output is applied to the correction logic. The 14 input bits correct the MSBs to produce a 12-bit-accurate output word.

A conversion time of 200 ns and a throughput of 5 MHz is achievable if the propagation delay of the comparators is about 80 ns, the DAC and summing amplifier settle in about 10 ns each, and the error correction and other logic takes 20 ns. However, the input must not change during the 200-ns period, thereby limiting the maximum signal frequency (for a 2-V pk-pk sine wave) for 12-bit accuracy to under 1 kHz. Such a design suits many relatively slow inputs that are multiplexed and con-

# 12-BIT 10/20-MHz-SAMPLING-RATE ADCs

ers for the asking. SPT, on the other hand, is charging \$495 per board.

These converters all represent the start of a new generation of high-speed monolithic ADCs. The lower-power TTL versions are expected from SPT by year's end, and slower versions (for example, units with sampling rates of 5 MHz or even lower) sometime next year. Because the architecture of the SPT converters may lend itself to higher-resolution designs, higher-resolution ADCs may yet become available from SPT. One of ADI's test chips (for ADI's military contract) had an automatic gain-ranging front-end that provid-

ed four bits of additional dynamic range, resulting in a 16-bit converter with 12-bit accuracy. The gain is changed on a sample-by-sample basis. A commercial version of this ADC may emerge by the end of 1992.

All three SPT converters are available in die form. The 10-bit units come in 28-pin and the 12-bit SPT7912 in 32-pin double-width ceramic DIPs. Additionally, the SPT7814 comes in a 28-pin LCC. All handle the industrial-temperature range. The AD773 is also available in a 28-pin double-width ceramic DIP and a 28-pin plastic skinny DIP. The AD872 comes in a 44-pin LCC. Both operate over the

commercial-temperature range. Both SPT and ADI will have military devices by sometime next year. □

### PRICE AND AVAILABILITY

All SPT and ADI converters are sampling at the present time. See the table for prices. Signal Processing Technologies Inc., 1510 Quail Lake Loop, Colorado Springs, CO 80906; Richard Mintle, (719) 540-3900.

CIRCLE 511

Analog Devices Inc., 181 Ballardvale St., Wilmington, MA 01887; Paul Errico, (617) 937-1297.

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HIGHLY	518
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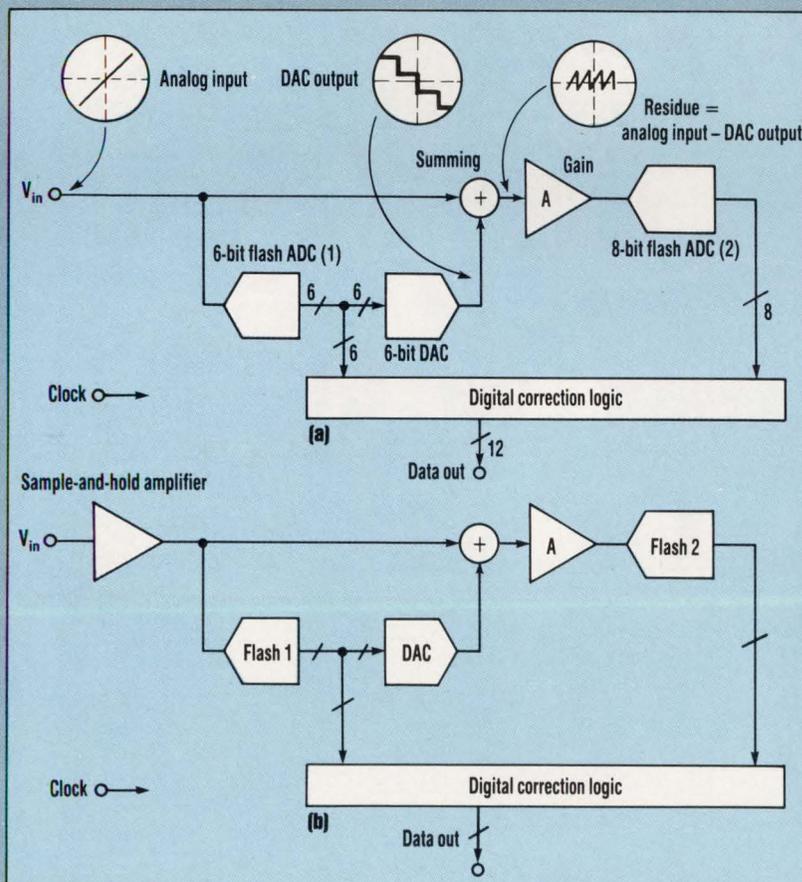
Adding a fast SHA with 100-ns acquisition time and 20-ps aperture uncertainty (jitter) raises total conversion time to about 300 ns, and the throughput rate (now sampling rate) drops to about 3.30 MHz (see the figure, b). But now

the converter easily handles Nyquist-rate sine waves, and an extra clock period must be added for the SHA to acquire the signal. The conversion thus requires three clock cycles of about 100 ns each.

Alternatively, adding the SHA can turn the circuit into a pipe-

lined converter with at least twice the sampling rate. At clock-cycle zero, the SHA is put into hold, storing the sample it has just acquired; flash<sub>1</sub> is strobed (latched), holding a digital word representing the the SHA's sample; and flash<sub>2</sub> is unlatched. While the DAC and summing/gain circuits settle, comparators in flash<sub>2</sub> "acquire" the latter's output. At clock-cycle one, flash<sub>2</sub> is strobed, its output is fed to the correction logic and output, and both the SHA and flash<sub>1</sub> are put into the acquire mode to get a new sample. At clock-cycle two, the SHA is again put into hold and the events of clock-cycle zero repeated. At clock-cycle three, the events of clock-cycle one are repeated and the data word for the sample taken at clock-cycle two is fed to the correction logic.

While such a pipelined conversion (two data samples are always in the pipeline) still takes two clock cycles, the sampling rate is doubled because both conversion steps are performed each cycle. The hypothetical converter described in the previous paragraph could sample at about 10 MHz. The delay between taking the first sample and the availability of its value as a digital output word, called latency, is usually specified in clock cycles. In most applications, the delay isn't critical.



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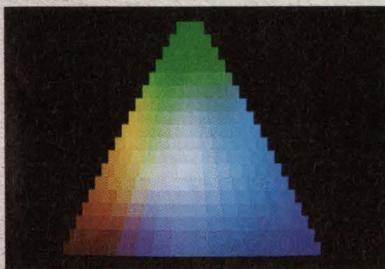
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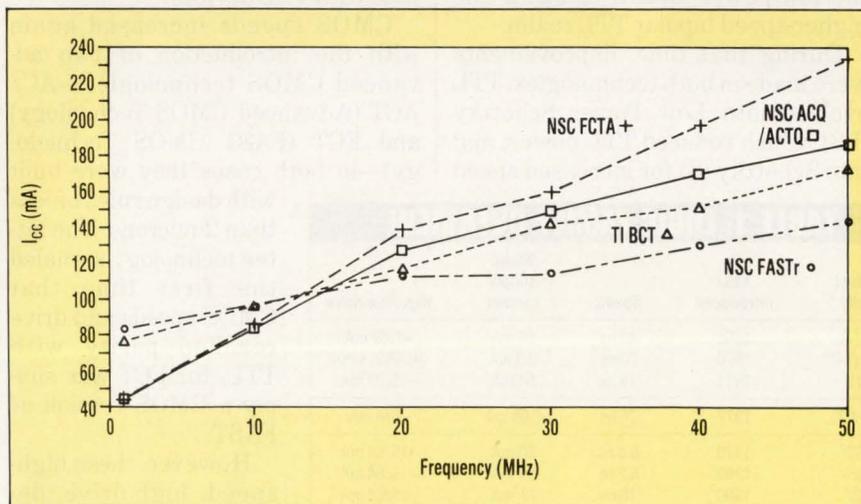
**A**s recently as 1985, designers of logic-based systems had only ten logic families to choose parts from for their designs. Those families differed enough in speed and power consumption to make the selection process relatively simple. Since then, over twenty new logic families have been introduced, some with very subtle differences.

The reason for the proliferation of logic types is the trend toward ASICs. As designers use more ASIC devices, they demand a more nearly perfect match between their custom designs and the standard logic used to "glue" those custom chips into systems. Because most circuit functions are performed by the ASICs, the designers are less impressed by logic families that boast a broad array of functions than by devices with cutting-edge performance. Basically, all they want are interface devices—but with outstanding specifications.

The response of the semiconductor manufacturers has been to keep their logic interface devices at the cutting edge of the performance envelope—one step ahead of the ASIC solutions—by emphasizing four key areas: speed, power, drive, and noise. No single family can be best in all categories, so new families have been introduced, each representing an optimization of two (or

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# ADVANCED LOGIC SELECTION

sometimes even three) of the performance parameters. Such efforts have greatly increased the number of logic families on the market.

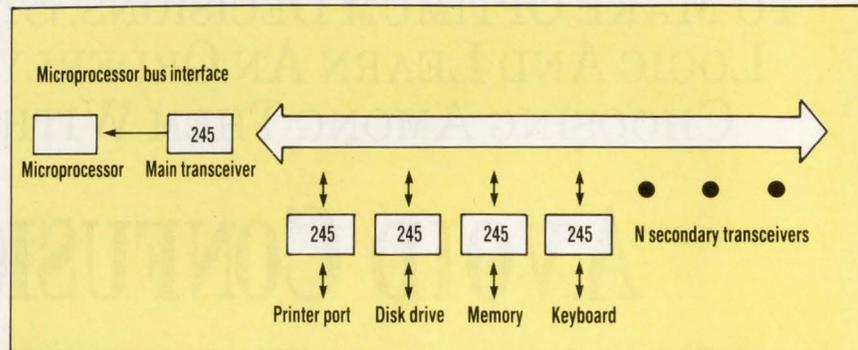
Further complicating the designer's selection process among these families is that each performance area can no longer be described with one parameter, but is instead described by several subparameters. For example, power today isn't specified as a single number, but as two or three: there's static power, dynamic power, and (in the case of CMOS) TTL power.

How is one to make an intelligent choice from among the plethora of logic types currently available? Get a good working knowledge of the basic logic types, see where the new types fit into the overall picture, and then use a flow-chart approach to make the selection. Here's how.

## FIRST THERE WAS TTL

The first major logic family—Standard TTL—hit the scene in the late 1960s. It was quickly followed by the CD4000 series CMOS family. Although the CD4000's propagation delays approached 100 ns, it captured a significant share of the market because of its negligible static power consumption. For the next twenty years, designers and their subsequent systems fell into either the low-power CMOS camp or the higher-speed bipolar TTL realm.

During that time, improvements were made in both technologies. TTL evolved into Low Power Schottky (LS), which reduced TTL power, and into Schottky (S) for increased speed



**2. THE OPTIMUM CHOICE** of technology for a bus transceiver depends on precisely what the transceiver will be doing. In this example, the constantly toggling main transceiver is best implemented in advanced bipolar, whereas the secondaries will do better with CMOS.

and drive. TTL recombined in the late 1970s to form FAST (Fairchild Advanced Schottky TTL). Through advances in process geometries, FAST logic successfully integrated the low power of LS and the speed and drive of S into one comprehensive logic family.

At the same time, CMOS underwent a similar technology transformation. The development of 5-V polysilicon-gate high-speed CMOS (HCMOS) gave system designers a CMOS solution that was four times faster than its 15-V metal-gate CD4000 predecessor. HCMOS split into two extensions: HC to interface with CMOS devices and HCT to interface with TTL devices.

CMOS speeds increased again with the introduction of two advanced CMOS technologies—AC/ACT (Advanced CMOS Technology) and FCT (FAST CMOS Technology)—in both cases they were built with design rules of less than 2 microns. The latter technology signaled the first time that CMOS speeds and drive reached parity with TTL, for FCT was simply a CMOS version of FAST.

However, these high-speed, high-drive, devices with CMOS output swings were rather noisy. Although noise had always been recognized as an important

system parameter, it became a major differentiating factor among technologies with the introduction of advanced CMOS technologies.

## CHOOSING AN OLD STANDBY

Even though there are vast performance differences among logic families, a number of major commonalities also exist (Table 1). Established families tend to be low in cost, be available from multiple vendors, have proven track records, and offer many functions. However, system designers must beware of technologies where suppliers are dropping out and component prices are on the rise. This is currently true of Standard TTL, CD4000 series CMOS, Low Power Schottky, and Schottky.

The most popular older families for new designs make up the lower two-thirds of Table 1, and can be grouped as shown into three broad categories based on speed, noise, and power consumption.

Within each category, significant differences show up. For example, ALS uses one-third the power of FAST but is only slightly more than half its speed; AC/ACT maximizes transmission drive with symmetrical  $\pm 75$ -mA output current; and FCT maximizes static termination drive with an  $I_{OL}$  specification of 64 mA.

Choosing among these older technologies is fairly straightforward. The process begins with the macro categories. The designer of a commercial, low-cost portable computer might go through the following se-

**TABLE 1: LOGIC FAMILY OVERVIEW**

Product family	Year introduced	Speed	Static supply current	High/low drive
Std TTL	1968	40 ns	30 mA	-2/32 mA
CD4K/74C	1970	70 ns	0.3 mA	-0.48/6.4 mA
LS/S	1971	18 ns	54 mA	-15/24 mA
HC/HCT <sup>1</sup>	1977	25 ns	0.08 mA	-6/6 mA
FAST <sup>2</sup>	1978	6.5 ns	90 mA	-15/64 mA
AS <sup>2</sup>	1980	6.2 ns	90 mA	-15/64 mA
ALS <sup>2</sup>	1980	10 ns	27 mA	-15/64 mA
AC/ACT <sup>3</sup>	1985	10 ns	0.08 mA	-24/24 mA
FCT <sup>3</sup>	1986	6.5 ns	1.5 mA	-15/64 mA

<sup>1</sup>Low speed, low noise, low power.

<sup>2</sup>High speed, low noise, high power.

<sup>3</sup>High speed, high noise, low power.

# ADVANCED LOGIC SELECTION

lection steps:

Because the end product should carry a low price tag, a mature technology is most appropriate because of its low component cost. Because low power consumption is essential in a portable PC, a CMOS-based technology is almost mandatory. If the system will operate at 12 MHz or below, then HC/HCT is ideal. If it's to operate above 16 MHz, AC/ACT will be needed. Between 12 MHz and 16 MHz, a detailed timing analysis can determine which technology to use.

## WHAT'S NEW?

That simple selection process can get quite complex when newer logic families are considered. To see how, the four major categories of new logic families must be discussed (Table 2). They are:

- Second-generation advanced CMOS (ACMOS) that emphasizes low noise (ACQ, ACTQ).
- Second-generation CMOS that emphasizes speed (FCTx, FCTxT).
- Second-generation advanced bipolar TTL [FASTr].
- First-generation biCMOS (BCT).

Unlike mature families, these technologies are typically sourced by fewer than three suppliers, and feature mostly bus-interface devices. They typically offer various word widths (9, 10, 16, 18, and 32 bits), special provisions to make them easily testable, and built-in series resistors.

In addition, they tend to be packaged in surface-mountable packages with 25-mil pin spacing to cut their footprints in half. The functionality and packaging, coupled with a new generation of specifications, gives today's designers unprecedented flexibility. To exploit that flexibility, though, the new families' performance trade-offs must be fully understood by designers.

ACQ/ACTQ is a pure CMOS technology. Its advanced circuitry minimizes all types of noise while maintaining extremely low CMOS power at respectable speeds. In addition, ACQ/ACTQ features symmetrical  $\pm 24$ -mA dc and  $\pm 75$ -mA ac outputs to drive low-impedance transmission lines. Many designers who

like first-generation ACMOS specifications but became disillusioned with its noise aspects have migrated to this technology.

Similar to its predecessor, ACQ/ACTQ is available in a version with CMOS input levels (ACQ) and in a TTL-interface version (ACTQ). The ACQ version sports higher (low-level) noise margins with the switching threshold at 50% of  $V_{CC}$ , propagation delays that are 1 to 2 ns faster, and a full set of ac/dc specifications at a supply voltage of 3.3 V.

FCTx and FCTxT are spin-offs from the original FCT family. Although both are pure CMOS technologies with TTL-compatible input levels, FCTx has CMOS output swings while FCTxT utilizes reduced-swing TTL-like outputs for lower noise. In some cases, those reduced swings have cut FCT noise in half. However, ground bounce still tends to be above 1.5 V in a test fixture. Both the CMOS- and TTL-output versions come in three speed grades (A, B, and C), with propagation delays ranging from 4.1 to 4.8 ns on popular buffer-type devices. In addition, FCTx and FCTxT feature an  $I_{OL}$  rating of 64 mA for driving bipolar-type terminations.

FASTr is currently the fastest 5-V logic family on the market (other than ECL, of course). Its propagation delays are down to a mere 3.9 ns. With up to 40% power reduction over its predecessor, FASTr became the natural choice for designers who were comfortable with FAST/AS but needed even more speed, high drive, and low noise.

BCT is a biCMOS technology. It's largely TTL for high speed but strategically utilizes CMOS transistors in its TRI-STATE circuitry. Al-

though BCT uses more static power than ACMOS technologies and isn't as fast as FASTr, it doesn't have any weaknesses. It combines excellent dynamic power, extremely low noise, and a 64-mA  $I_{OL}$  to provide a solid balance of the four key selection criteria designers are concerned with.

## ANALYZE THE APPLICATION

Because of the compression of performance characteristics of the four newest technologies, system designers must select their technology on the basis of subparameters, as mentioned earlier. To do so requires that the subparameters be related to specific aspects of the system under design. The selection process usually begins with a power analysis.

Power is the most complex and sometimes most misunderstood selection criterion. Systems that are portable, battery operated, lightweight, or require above average reliability must clearly make minimizing power consumption a top priority. But determining which advanced logic family will use the least power in a given system isn't always a clear-cut choice.

Several incorrect assumptions are commonly made in that connection. Designers who misunderstand the dynamic power component of CMOS may erroneously choose ACMOS as the lowest power option for all applications. Conversely, those who understand dynamic power may be misled by test fixture comparisons or databook calculations that fail to accurately represent a real system. It's also important to understand that biCMOS families (such as BCT) have a static power consumption more in line with bipolar than ACMOS.

On the device level, the power con-

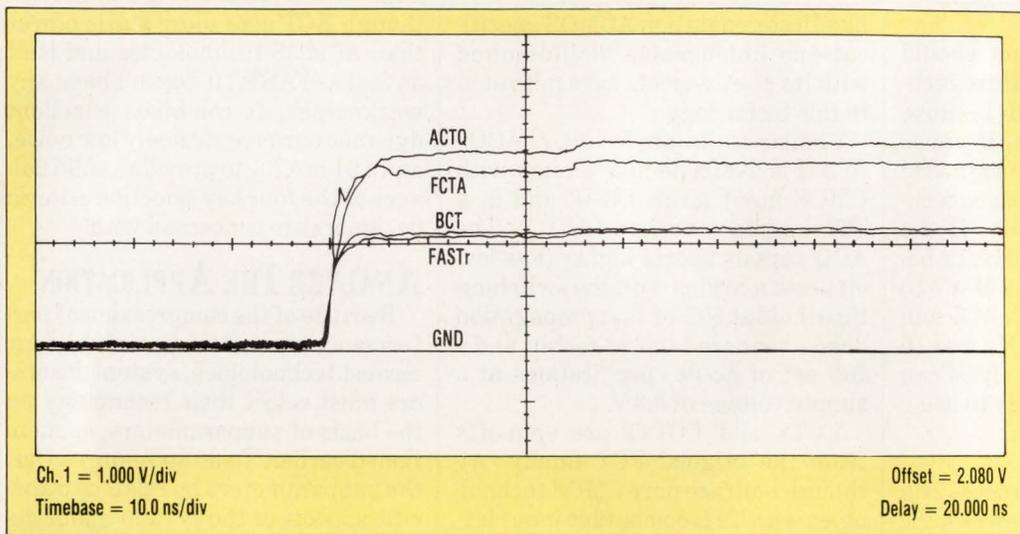
**TABLE 2: ADVANCED LOGIC GENERAL CHARACTERISTICS**  
(Comparison of '244 buffer function)

Family	Year introduced	Number suppliers	Technology base	I/O levels	Speed	Maximum static supply current	High/low drive
ACQ	1989	2	CMOS	CMOS/CMOS	6.0 ns	80 $\mu$ A	-24/24 mA
ACTQ	1989	2	CMOS	TTL/CMOS	7.5 ns	80 $\mu$ A	-24/24 mA
FCTx	1987	3	CMOS	TTL/CMOS	4.1-4.8 ns	1.5 mA	-15/64 mA
FCTxT	1990	2	CMOS	TTL/TTL	4.1-4.8 ns	1.5 mA	-15/64 mA
FASTr	1990	1	Bipolar	TTL/TTL	3.9 ns	50 mA	-15/64 mA
BCT	1987	2	BiCMOS	TTL/TTL	5.5 ns	10 mA	-15/64 mA

x = A, B, C (3 speed grades)

DESIGN APPLICATIONS

## ADVANCED LOGIC SELECTION



**3. DRIVING TRANSMISSION LINES** is clearly the province of the CMOS technologies. The bipolar-based families barely meet  $V_{IH}$  levels because of their weak  $I_{OH}$  capability. Note that these traces were taken without pull-up resistors. The outputs of the bipolar-based families would increase dramatically if such terminations were used, but so would their power consumption.

sumed by advanced bipolar and biCMOS is relatively easy to calculate. It consists of a dominant static component and a negligible dynamic component. BCT's advantage over FASTr is greatly reduced power in TRI-STATE (its  $I_{CCZ}$  is just 9 mA, compared with 50 mA for FASTr).

Power for the ACQ/ACTQ and FCT families consists of a negligible static component, a dynamic component, and an  $I_{CCT}$  component. The  $I_{CCT}$  component is the additional power a CMOS device consumes when operating at TTL-input levels. The

dynamic component, of course, is the power dissipated when charging and discharging the CMOS device capacitance.

Comparing the dynamic power dissipation for different technologies is a tricky business (Fig. 1). The figure plots power-supply current versus frequency for the four technologies under consideration. It assumes a standard test fixture that applies a 50-pF/500- $\Omega$  load to the outputs. Note that the CMOS technologies cross over with FASTr and BCT in the range of 12 to 15 MHz. Despite

that crossover, it's not true that FASTr and BCT are always more power efficient than CMOS at frequencies above that range. To see why, several points must be considered.

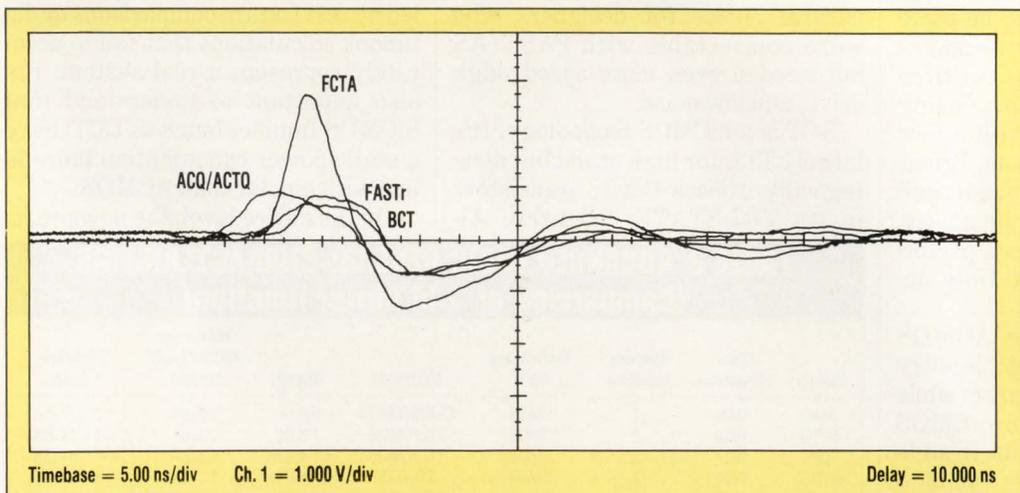
First, the standard test fixture load of 500  $\Omega$  shunted by 50 pF imposes a large penalty on the AC MOS devices with their 5-V swing. Compared with the 3-V TTL swing, the penalty is calculated to be 19.2 mA at 10 MHz. In an actual system with high-impedance loads and recommended low-power CMOS termination schemes, the load would be much lighter and the

penalty to CMOS would not exist.

TTL/ACMOS crossover frequencies in real-life, constantly switching systems are typically above 20 MHz. Above that point, advanced bipolar and biCMOS technologies exhibit lower dynamic power and may be preferred over ACMOS—if the applications indeed involve constant switching. However, most applications share switching duty cycles with two or more devices. In those applications, the real advantage of ACMOS lies in its negligible static power dissipation.

Designers must scrutinize their own systems to determine which technology will really consume the least power. Where power-down and TRI-STATE conditions exist, ACMOS is ideal. However, if active signals are present on a powered-down device, BCT or FASTr offer better I/O protection. Where higher speed pipelining exists, FASTr or BCT are best.

To see how the choice of logic family is intimately related to the



**4. GROUND BOUNCE** is a problem only for the FCTx family. Every other technology exhibits similar characteristics and is suitable for all applications that require low ground bounce.

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## ADVANCED LOGIC SELECTION

precise nature of the application, consider the case of a microprocessor bus interface (Fig. 2). Only two of the secondary transceivers are active at any given time (in non-broadcast modes) while the remaining  $N-1$  transceivers remain in TRI-STATE.

Therefore, the way to minimize overall power consumption is to use AC MOS for those transceivers even though the data frequencies are well above 20 MHz. As the number of secondary transceivers attached to the bus gets larger, the power advantage of AC MOS over FASTr or BCT becomes more pronounced. AC MOS's low static power consumption minimizes the loading caused by the many inactive devices.

On the other hand, because the main bus transceiver is always toggling, the best choice for that part with the same operating frequency is FASTr or BCT. That transceiver's higher static dissipation is vastly outweighed by its lower dynamic consumption at high frequency.

In contrast to power dissipation, comparing logic family speeds is a snap. All that's needed is to analyze the requirements, then match them with the propagation delay times published in the various logic family

databooks. In approaching a timing analysis, the designer begins by determining the clock period and subtracting all of the delay elements and setup times in a specific path. Typically, ASIC, memory, and VLSI devices are considered first, with the remaining time allocated for logic.

### THE TIMING BUDGET

Historically, logic has typically accounted for approximately 25% of the timing budget for a given path (Table 3). To maintain that percentage for systems based on high-speed RISC and 486-type processors, such logic devices as FASTr, BCT, and FCTA are required. For 286- and 386-based systems, AC MOS such as ACQ and ACTQ, are ideal.

Designers should pay close attention to propagation delays when several outputs change state at the same time. In databooks, most  $T_{PD}$ s are specified under single-output switching conditions. Consequently,

### TABLE 3: IMPORTANCE OF SPEED

System clock speed	Clock period	Predominant logic	Propagation Delay	% of Fastest clock period
2 - 10 MHz	100 - 500 ns	HC, LS	18 - 25 ns	22%
10 - 30 MHz	33 - 100 ns	ALS, AS, FAST, FACT, FACT QS	6.5 - 10 ns	25%
30 - 66 MHz	15 - 33 ns	FASTr, BCT, FCTA	3.5 - 5 ns	28%

The 25% Rule: Throughout system evolution, logic delays have represented approximately 25% of the total system clock cycle. FASTr, BCT, and FCTA easily meet the speed requirements of systems with clock rates in excess of 30 MHz.

these numbers may not always represent the worst case in a real-world environment.

When several outputs switch together, the ground currents increase, extending the propagation delays. Most advanced families supply derating numbers in the applications section of the databook for evaluating multiple-output-switching (M-O-S) conditions (a typical derating figure is 250 ps for each additional switching output).

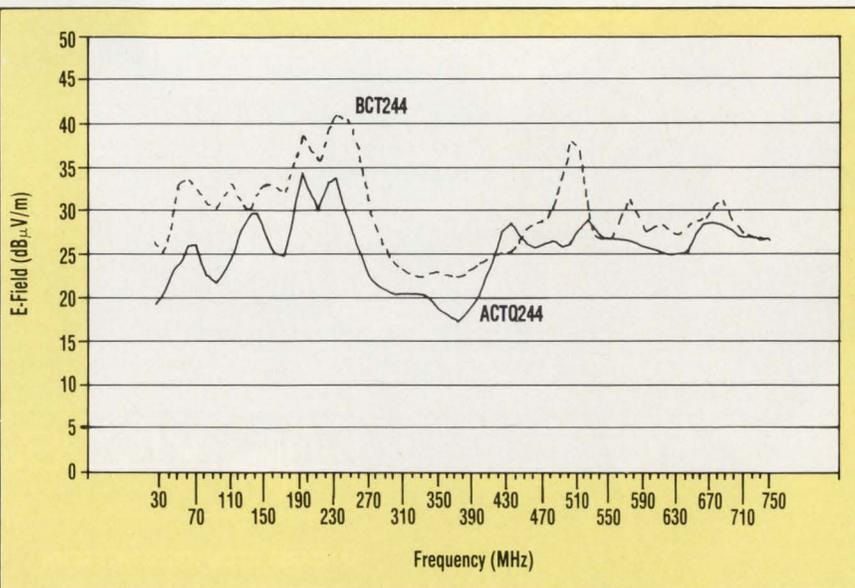
BCT and FASTr are unique in that their databooks include  $T_{PD}$  figures that are valid under M-O-S conditions (all outputs switching). For example, the  $T_{PLH/HL}$  for the 74FR244 is specified at 3.9 ns over the commercial temperature range under single-output-switching (S-O-S) conditions and at 5.0 ns under M-O-S conditions.

### LOADING CONSIDERATIONS

Other specification advancements deal with changing load conditions. Early logic was specified into a 15-pF load. As bus applications became more popular, and ATE stray capacitance prevented accurate 15-pF measurements, a 50-pF load became standard.

However, 50 pF falls short of emulating the load imposed by a highly capacitive memory array. The  $T_{PD}$  of BCT and FASTr are specified for a 250-pF and a 50-pF load; other families stick to 50 pF as a standard capacitive load and provide derating curves. For example, the previously cited 3.9-ns FASTr specification is valid for 50 pF. It grows to 7.3 ns when the part must work into 250 pF.

Current-drive applications can be divided into two types: static loading and transmission-line driving. The



**5. ELECTROMAGNETIC RADIATION** is fast emerging as the most important noise specification for many applications. Despite its low ground bounce and output swing, BCT comes in second behind ACQ/ACTQ because of the latter's output waveshaping, as this plot shows.



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static-drive capabilities of the various logic families are easily compared using databook  $I_{OL}$  and  $I_{OH}$  specifications. By examining the databooks for the four technologies, it shows that ACQ/ACTQ has a  $\pm 24$ -mA symmetrical drive whereas FCTx/xT, BCT, and FASTr have ratings of 64 mA for  $I_{OL}$  and  $-15$  mA for  $I_{OH}$ . The advantage in static drive definitely goes to the technologies with the 64-mA  $I_{OL}$ .

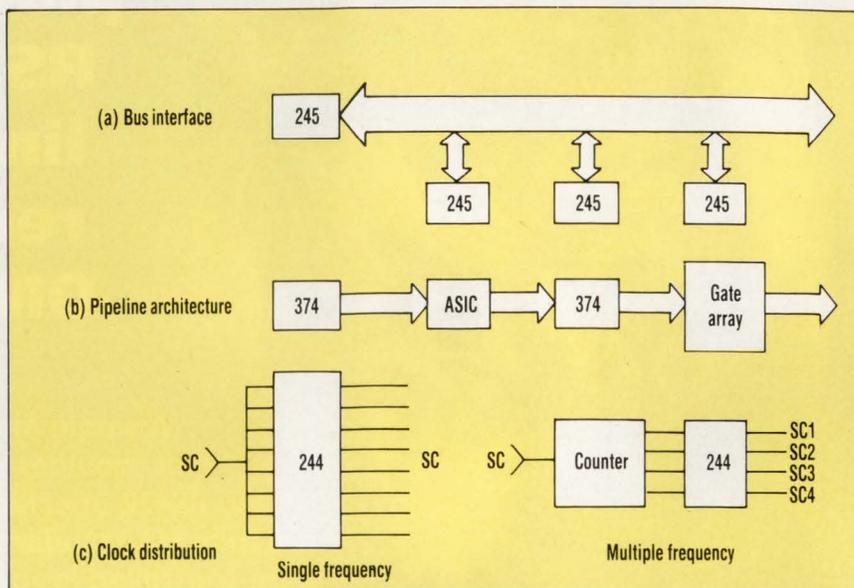
That's important for many of today's standard buses, such as the VMEbus, which requires a Thevenin termination at both ends. Because of the dual termination, any device that drives the VMEbus may have to sink up to 48 mA of current—unless, of course, a blocking capacitor is placed in series with the termination resistors, which is occasionally done.

One consequence of the continuing move toward tighter circuit-board trace geometries is that line impedances are dropping, creating a need for increased transmission-line drive capability. In addition, as more devices are attached to the lines, their distributed capacitances further decrease the impedance into which logic drivers must work. When line driving is an important consideration, ACQ/ACTQ and FCTA have a significant edge over other logic types (Fig. 3). As the figure shows, they easily drive a 50- $\Omega$  line to better than 3.4 V with the incident wave.

By comparison, BCT and FASTr must strain to provide a  $V_{OH}$  level of 2.0 V on a 50- $\Omega$  line without the aid of power-consuming pull-up resistors. Without such terminating resistors, they can't reliably drive lines with impedances of less than 50  $\Omega$ .

A heavily loaded pc-board trace with a characteristic impedance of 100  $\Omega$  can easily have an effective impedance below 50  $\Omega$ . Therefore, great care should be taken by designers to select a logic family with sufficient transmission-line drive. Unfortunately, high speed and drive capability tend to be accompanied by increased noise.

Noise can be divided into two main categories: that which originates in the device, and that which is generat-



**6. THE THREE MAIN AREAS** in which logic is applied are bus interfacing (a), pipeline architecture (b), and clock distribution (c). Each has its own unique requirements, and may therefore be best served by a logic family different from the others.

ed by the system.

Device-generated phenomena are typically lumped into the category of ground bounce. They're caused by switching transients flowing through device power and ground inductances. Ground bounce manifests itself in several ways, of which the most important is positive ground bounce ( $V_{OLP}$ ).

$V_{OLP}$  pulses generally aren't a problem on synchronous data lines because they occur during the part of the clock cycle when data is regarded as invalid. However, if the amplitude is great enough, problems can occur when the  $V_{OLP}$  pulse appears on an asynchronous signal, such as a clock line, reset, preset, memory write enable, load signal, or other control line (Fig. 4).

The figure shows a worst-case comparison of the ground bounce in a test fixture for the four technologies under consideration. Clearly, ACQ/ACTQ, BCT, and FASTr exhibit excellent ground-bounce characteristics (between 0.8 V and 1.0 V) in a test

fixture and would easily remain below  $V_{IL} = 0.8$  V in an actual system. FCTA  $V_{OLP}$  could cross a TTL  $V_{IL}$  in an actual system. Therefore, FCTA isn't recommended for driving asynchronous signals where quiet output switching conditions can occur.

## TEST FIXTURE EFFECTS

As with power consumption, caution must be exercised when analyzing test-fixture data. The test fixture is a good comparative tool, but it doesn't correlate well to ground bounce in an actual system. As in the power case, the culprit is unrealistic loading.

Because of the distributed nature of system capacitive loading, typical system ground bounce is only 50 to 65% of test-fixture ground bounce for the same total capacitance.

**TABLE 4: TRANSITION TIME COMPARISON**

Family	$T_{rise}$	$T_{fall}$	Voltage Swing*	Line length (in.)
ACQ/ACTQ	4.5 ns	5.0 ns	4.9 V	16
FCTx	4.0 ns	1.5 ns	4.8 V	6
FASTr	4.5 ns	2.0 ns	3.4 V	10
BCT	4.5 ns	2.5 ns	3.4 V	12

\*  $V_{CC} = 5$  V

Rise and fall times are the key parameters in determining whether a given pc-board trace will exhibit transmission-line effects and necessitate termination. The slow rise and fall times of ACQ/ACTQ necessitate terminations to eliminate ringing only for lines longer than 16 inches.

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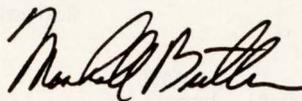
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Undershoot ( $V_{OLV}$ ) can be a problem when driving other devices that lack adequate input protection. Some DRAMs, PALs, and DACs are sensitive to  $V_{OLV}$  greater than  $-1.5$  V.

As Figure 4 makes clear, the undershoot characteristics of the four technologies under consideration pose no threat to sensitive devices: Their  $V_{OLV}$  is no greater than  $-1.2$  V. However, that's not necessarily the case with all new advanced logic technologies. So any new family's  $V_{OLV}$  characteristics should be studied before any of its members are used to drive a sensitive input.

## TRANSMISSION-LINE RINGING

Unlike device-generated noise, system-generated noise can be controlled by proper design techniques regardless of technology. The differences among the various technology families is one of degree—more care must be taken with the faster families than the slower ones.

Consider transmission-line ringing. All technologies can cause the same level of ringing on a transmission line. Conversely, all technologies can be terminated with equal effectiveness. What separates them is the length of pc-board trace or wire that requires termination. The faster the technology, the shorter the trace that must be terminated.

A metallic connection will behave as a transmission line and exhibit ringing if its one-way propagation delay is greater than one-third of the signal's minimum rise or fall time, which ever is shorter. On a given circuit board, the faster technologies are likely to require terminations on a larger number of system traces than the slower ones, resulting in added cost and increased use of valuable board real estate (Table 4).

Table 4 compares pulse edge rates for the various technologies, and shows the line lengths above which termination is required. The

slow edge rates of ACQ/ACTQ require terminations on pc-board trace lengths greater than 16 in., whereas FCTx/xT families require terminations on all lines greater than 6 in. The others fall between those two extremes.

When terminating transmission lines driven by the AC MOS technologies, it's best to use series or ac terminations to maintain low system power, while parallel or Thevenin terminations can be used for FASTr and BCT.

Crosstalk is another category of system-generated noise that can be controlled by proper design. It comes about when currents are coupled from one signal line to another.

The amount of capacitive crosstalk current is proportional to the signal's edge rate and to the coupling capacitance between the signal lines. Other than choosing a logic family with a low edge rate, if other considerations permit, the best way to control crosstalk is to minimize the coupling capacitance. Such minimizing techniques include:

- Increasing the spacing between

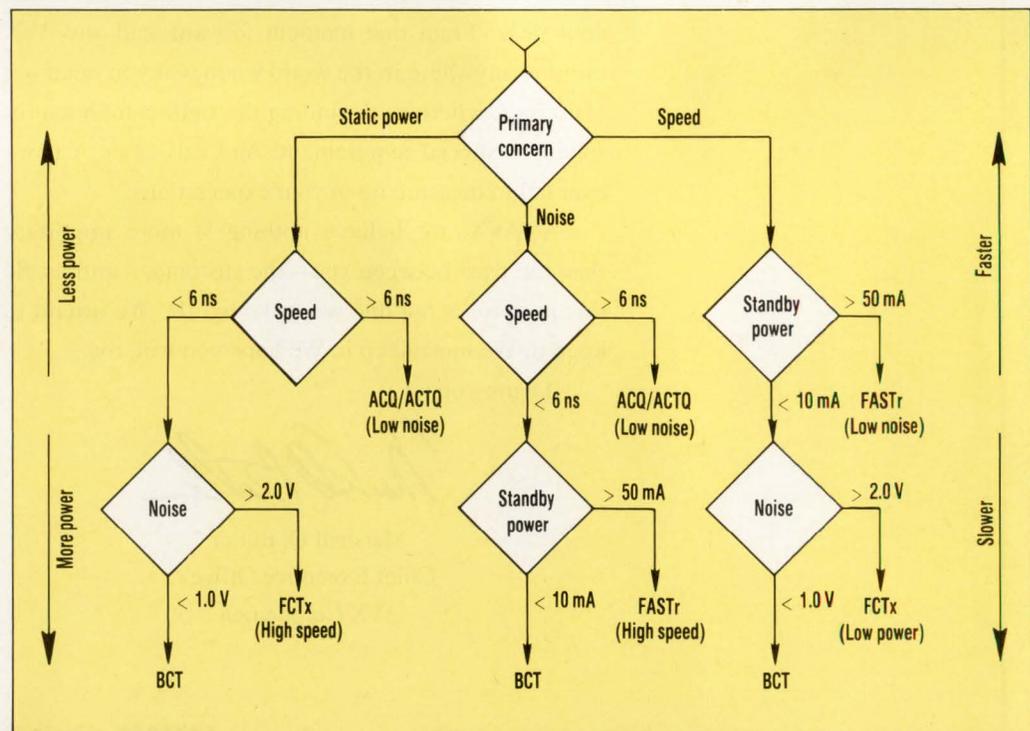
signal lines.

- Using multilayer pc boards.
- Keeping the trace directions on adjacent layers of multilayer pc boards orthogonal to each other.
- Shielding the layers of a multilayer pc board with ground and power planes.
- Shielding susceptible lines with ground and power traces.
- Using coaxial, differential, or twisted-pair wiring.

EMI—that is, radiated noise—is the most complex of all noise types. It requires thought at all levels of design, from IC selection through board layout to system shielding.

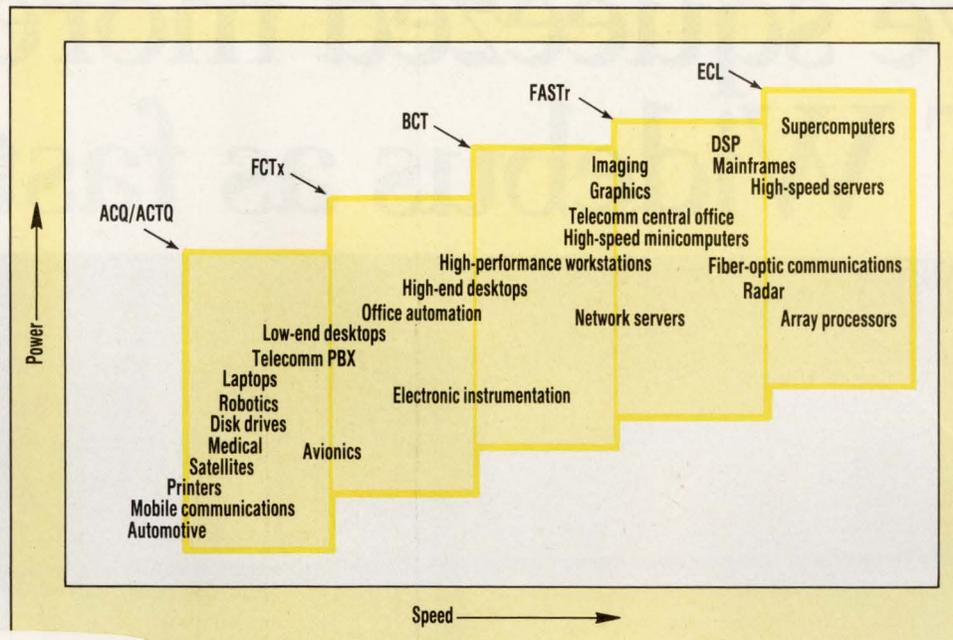
In considering ICs as sources of radiated noise, the designer is best advised to take a frequency-domain point of view. In general, the more high-frequency energy in a chip's output waveform, the greater the amount of system-level EMI that chip will generate. As a general rule, the spectral composition of a waveform tilts toward the higher frequencies as rise and fall times decrease, and as the transitions get sharper.

Logic is a major contributor to sys-



**7. A SYSTEMATIC methodology for choosing logic families is provided by this flow chart. The left side is for applications in which minimizing power consumption is most important. The right is for speed. As one proceeds down the chart to optimize secondary parameters, the primary parameters are somewhat compromised.**

# ADVANCED LOGIC SELECTION



**8. MIX AND MATCH:** This chart, which matches logic families and applications, is useful mainly as a starting point for logic selection. Mid-range applications may well require a mix of technologies for optimum performance.

tem-level EMI because logic interface devices tend to be used to drive high-current and/or long board traces, such as those used to distribute the system clock.

Because they have the slowest edge rates, ACTQ and BCT present the fewest problems concerning EMI. Even though BCT has excellent ground-bounce levels and a reduced-swing output, designers should be aware that ACQ/ACTQ's output waveshaping produces slower rise and fall times and more rounded transition corners. It therefore radiates less spectral energy across the entire frequency range (*Fig. 5*).

Even the noisiest technology can be dealt with by the proper application of board-design and system-shielding techniques. As might be expected, however, there's usually a cost penalty associated with protecting against EMI. Thus, whenever possible, a low-EMI technology like ACQ/ACTQ should be used.

There are three main categories of logic applications in most systems: bus interfacing, pipeline architecture, and clock distribution (*Fig. 6*). As stated earlier, the secondary TRI-STATEable elements in the bus (*Fig.*

*6a*) should typically be implemented in AC MOS to reduce power, whereas the primary bus drivers should be implemented in FASTr or BCT for high-frequency operation. Because most bus operation is synchronous, noise other than EMI should not be a factor in logic selection.

If VME-type termination requirements exist, then FCTx, FASTr, or BCT must be used. On the other hand, if transmission impedances dip below 50  $\Omega$ , then ACQ/ACTQ and FCTA become the families of choice. Clearly, if both requirements prevail, the selection is limited to FCTA.

The logic used in the pipeline architecture (*Fig. 6b*) will be almost entirely dictated by speed. In such applications, the logic is usually required to refresh the system clock, and can therefore consume no more than 10 to 20% of the system clock period. Speed, clearly, is an essential ingredient.

At the higher frequencies, FASTr and BCT may use less total power than AC MOS; however, AC MOS may nevertheless be required to maintain voltage-level compatibility with ASIC inputs. Noise and drive are not usually a differentiating fac-

tor with this type of configuration because of the short trace lengths, low loading, and synchronicity involved.

Clock distribution circuits (*Fig. 6c*) are excellent examples of the differentiating characteristics of logic. Such circuits generally run at high speed, involve very long controlled-impedance paths, and are extremely sensitive to both system- and device-generated noise.

Like the pipeline architecture, clock-distribution circuitry saves little or no power by using AC MOS at high clock frequencies. Nevertheless it may require AC MOS for voltage-level compatibility with other devices or for its transmission-line driving capability.

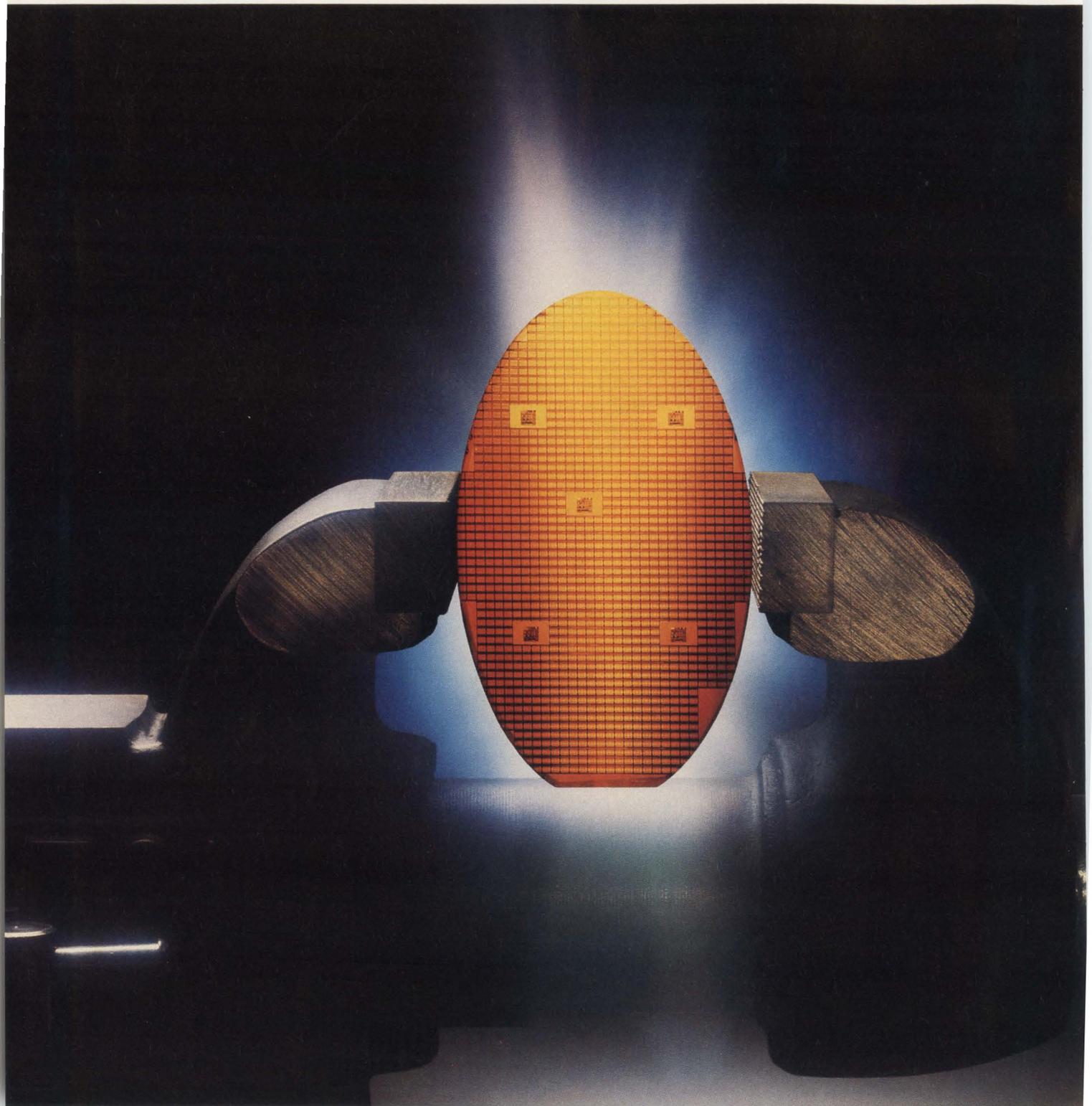
The traces that distribute the system clock are usually heavily loaded, low-impedance transmission lines, which almost always require terminations. Designers are free to choose an ac termination so that 64-mA static-drive capability isn't needed unless the designer wants to minimize the component count by using a parallel termination.

If the clock distributor has to deal with only one frequency (*Fig. 6c, left*), there won't be quiet output, so ground bounce should not be a problem, even with FCTA. However, because of the great length of most clock lines, EMI and crosstalk will be issues. If FCC guidelines must be met, then a low-radiation technology like ACQ/ACTQ or FASTr should be used.

If, on the other hand, the clock distributor must handle multiple frequencies (*Fig. 6c, right*), then things will be quite different on several counts. First, because the average frequency throughout the system is much lower than the system clock rate, pure CMOS technologies, such as ACQ/ACTQ or FCTA, will usually yield the lowest power. However, ground bounce will be a consider-

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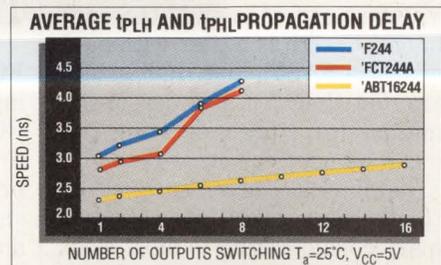
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## ADVANCED LOGIC SELECTION

ation. The higher frequency clock lines could couple ground bounce pulses onto the lower-frequency lines causing system malfunction. For that reason, FCTA isn't recommended for multifrequency clock buffering.

When selecting logic for clock circuits, several other characteristics specific to clock driving must also be considered. For example, skew between switching outputs must be kept to a minimum to maintain tight system timing. The four logic families under discussion have a guaranteed pin-to-pin output skew of less than 1.0 ns, but that won't necessarily be true for all advanced technology families.

Secondly, because clock distribution always occurs in an M-O-S environment, design is easier with such families as FASTr and BCT, which guarantee their  $T_{PDS}$  under M-O-S conditions (of course, derating factors can be used for other technologies, but it's less convenient).

Finally, duty cycle integrity is a primary consideration to most clock designers. The faster technologies like FCTA, FASTr, and BCT typically keep duty-cycle degradation below 5%.

### A SELECTION METHODOLOGY

To crystallize the trade-offs that must be made when choosing a logic family for a particular application, one can make good use of a flow chart (Fig. 7). It also offers a uniform methodology for making selections and helps prevent accidental oversights.

The charting process begins by asking the user to decide whether speed, power, or noise is of primary importance for his or her application. It then proceeds down to issues of secondary, and then tertiary importance. At each decision point, the chart asks whether a given parameter should be chosen more or less stringently.

If the less stringent branch is taken, the remaining parameter is optimized automatically. If the more stringent option is selected, the user gets to choose again. Unfortunately, because all parameters can't be opti-

mized at the same time, the further the overall optimization proceeds, the more likely the primary parameter is to be compromised.

To see how the process works, consider the design of a notebook PC bus circuit. Clearly, static power will be chosen as the primary concern. The chart then dictates that the second decision be made on speed. If the system is to operate below approximately 25 MHz, then transition times on the order of 6.0 to 7.5 ns are acceptable, and the chart suggests ACQ/ACTQ, which has the lowest noise of all the remaining options. If higher speed is needed, then the user is asked to make a decision based on noise performance.

### TRADEOFFS

The less stringent choice yields FCTx, the faster of the two remaining possibilities; the other calls for BCT. Because the notebook will need to meet FCC regulations, BCT will probably be the right choice. But it should be noted that the further down the flow chart one goes, the more power the technology uses—and low power was the primary condition to be optimized.

Similarly, a designer of a high-speed minicomputer will pick speed as the primary concern. As the designer works down the right side of the chart, it may be desirable to optimize power and noise. However, the technologies become slower as the designer goes further down the chart.

The considerations discussed in this article clearly apply to the broad middle range of applications in which technologies overlap. With certain applications, however, the best choices are immediately obvious (Fig. 8).

For example, some lower speed, low-power applications, such as disk drive controllers, are best implemented in ACQ/ACTQ, whereas high-end pipeline DSP functions are clearly best suited for FASTr. For the ultimate in high-speed applications, including super computers and array processors, ECL technologies are employed.

ECL is so obviously suited for

high-speed applications, and only high-speed applications, that it was unnecessary to include it in the preceding discussions.

Mid-range applications like workstations may use a combination of the technologies to optimize specific paths within the system. For those systems, following the guidelines presented in this paper for matching device characteristics on the subparameter level to system architecture and system performance requirements is essential to optimize system design. □

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*William M. Hall, National Semiconductor's Strategic Marketing Manager for its Advanced Logic Group, directs all new product development activities. He graduated from Drexel University in Philadelphia.*

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HIGHLY	524
MODERATELY	525
SLIGHTLY	526

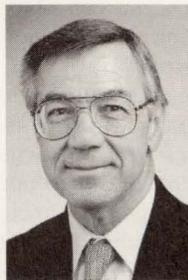
## THE CONTROVERSY

*It's not often that the basic precepts under which designers work get challenged. But now some industry experts are questioning MIL-HDBK-217's validity. For many years, it's guided engineers concerned with reliability. Will it continue to do so? Here are three views on the subject that highlight the growing controversy. We'd like to know how you feel about the issue.*

# MIL-HDBK-217: IT GETS MY VOTE OF CONFIDENCE

**I**n the January issue of this magazine, I wrote an article discussing the techniques of design for reliability. One technique I advocated at that time was the use of stress analysis and derating in electronic-circuit design. Among the points covered in the article was the need for some method to measure the reliability of your designs on a "real time" basis as you do the design work. Therefore, you can make the necessary design adjustments to achieve the desired reliability. I recommended several methods of doing this, including using the methods of MIL-HDBK-217 in a computer-aided, reliability-prediction program to simplify the process.

This method of reliability prediction was one of several reliability design methods used during the time from October 1980 through October 1990. It was employed to improve the reliability of our products by a factor of ten and meet the challenge given to us by John Young, the President of Hewlett-Packard Co. This improvement was measured by using actual field reliability data from the beginning 6-month period compared to the ending 6-month period. It's important that you understand that reliability engineering isn't just predicting reliability and changing the



**ROY WHEELER**  
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design in some way to respond to the results of the prediction. It involves stress testing; reviewing field failure data; analyzing circuit variability; looking for all possible failure modes, including user abuse; and much more. For now, I will be mainly addressing the issues of reliability prediction.

After completing the work on my January article, I read two other articles relating to the subject of design for reliability that I would like to comment on. The first article was published in the October 1990 issue of *PCIM, Power Conversion and Intelligent Motion*. This recent article is the latest of several by Charles T. Leonard of the Boeing Commercial Airplane Group that criticized the use of MIL-HDBK-217 techniques to analyze the reliability of electronic circuits. In the October article,

it was suggested that the MIL-HDBK-217 offers only one solution to the problem of failure rate reduction. The solution is the reduction of operating temperature. The point is that reducing temperature is accomplished at great expense in weight and total operating power by fans and other costly cooling methods. While this may be true in the data quoted in the article, it's not generally the case, and certainly not in the use of MIL-HDBK-217 predictions at the division of Hewlett-Packard where I worked.

I'm unaware of a single instance where our response to issues raised by the reliability prediction process was to reduce the ambient temperature. As I stated in my article, the appropriate response to this kind of issue is design changes to reduce the stress on the component where the stress level was found to be too high. This almost always involves reduced current, voltage, power, or increased stress rating by changing the choice of component used.

Mr. Leonard's article criticizes the modeling techniques of MIL-HDBK-217 as not realistically predicting the actual field failures of our equipment. My response is that the modeling techniques of MIL-HDBK-217 are based on millions of hours of field failure data and well known and understood principles of the physics of the failure of electronic devices. While the actual model used is a much simplified view of the actual failure mechanisms and cannot be proven theoretically, I have found by experience that this model is a reasonable and "good enough" predictor of failures to be a very effective tool. The use of the tool is to find design weaknesses without the time and expense of life testing each design.

In our modern electronic circuits, the failure rate of individual parts are generally measured in a few failures per billion hours of operation. To use life tests or field failure data to find these failure rates would take thousands of circuits tested over years of time—a completely impractical approach in the fast paced business we work in.

Let me give you a simple logical ar-

# THE



# CONTROVERSY

gument to support the use of MIL-HDBK-217 for predicting reliability. These methods just make the assumption that reliability is related in some fashion to the stress applied. I will support that argument by asking you to accept that in the limit, at Zero stress, even a faulty part will not fail. For a particular failure mode, the Zero stress environment might be dry cold storage with no voltage or current.

This is the limit condition of no stress. The other limit is at very high stress. Here, even a perfect part would fail with temperature, voltage, current, or power set so high as to melt, breakdown, cause migration of metal or doping, etc., of some critical element of the part and cause immediate failure.

All that you have to accept to give the MIL-HDBK-217 value is that these two conditions are connected by some continuous probability curve of some shape. The relationship assumed for the MIL-HDBK prediction is exponential, but this is certainly not correct for some failures. It's a reasonably good approximation of field failure experience when considered as a whole, over a lot of experience with a lot of different failure mechanisms and a lot of different parts.

Another criticism leveled at MIL-HDBK-217 is that it won't predict the failures in a well designed piece of electronic equipment. I agree. The whole point of the prediction is to design out the kind of failures the process predicts. I consider it as a success that these kinds of failures rarely show up any more in actual field experience.

I can tell you from my experience of many years of designing electronics that it's only since we started paying careful attention to the stress analysis of our designs that we stopped having these kind of failures. The prediction methods of MIL-HDBK-217 are just a tool to make sure we haven't overlooked a stress problem that will lead to field failures later.

The other problems, shown by the data in the October article as the ma-

ior cause of electronic-equipment failures, are what's left after proper design has eliminated the stress-induced failures. We as designers of electronic equipment should also be working to eliminate these failures. Things like user abuse, assembly errors, no trouble found, etc., are things that can and should be addressed at the design level to eliminate the root causes of these problems. Our designs should be nearly impossible to damage by any reasonable level of abuse, so easy to assemble correctly that to assemble them incorrectly is a rare event, so well designed that to misdiagnose a problem is nearly impossible.

One more comment about this October article. While the suggestions concerning cost-effective design are valid from a thermal design point of view, it's safe to say that it's a rare circuit indeed where you can place components on the board in the manner that was suggested.

The first thing the circuit has to do is deliver the electronic performance it was designed for. This requires placing the components in the proper relationship for circuit performance, which usually severely limits placing the components to achieve the desired ideal passive cooling that was advocated.

This isn't meant to minimize the need for good thermal design as part of the design process. I just wanted to say that there are other design considerations that necessarily take priority over the placement of components for optimum passive cooling.

The March 14 issue of *Electronic Design* contains the second article I want to talk about. It's a very entertaining if somewhat inaccurate article by one of my favorite authors, Bob Pease. If you haven't yet read it, please do so. I think you will enjoy it. In his article, Bob took some pretty heavy hits at statistics and people that use them and also people that use MIL-HDBK-217 methods to predict reliability.

Bob and Mark Twain both agreed that statistics were the work of the devil. I have to disagree. In fact, I would go so far to say that both Bob

and Mark make or made use of statistics every day in the conduct of their daily activities. Everybody does.

Bob and I are contemporaries. When he was working toward his BSEE at MIT, I was doing the same at the University of Illinois. At Illinois, and perhaps at MIT also, a course in statistics was required for graduation in the school of electrical engineering.

I wonder if Bob might just be pulling your leg a little with his comments on the subject of statistical analysis. In fact, I would go so far to say that I believe with a "99.99% confidence" (statistical talk meaning "damn sure") that his company uses statistical techniques in almost every aspect of the design and manufacture of semiconductor devices.

There's another point where I really have to differ with Bob. That's when he totally discounts the use of MIL-HDBK-217 for predicting reliability performance of electronics. Bob made the point that both statistics in general and MIL-HDBK-217 in particular were faulty because he had seen people use them and get incorrect answers.

You will pardon me if I observe that this is somewhat like refusing to use a hammer because you once saw someone hit his thumb with one. Statistics and MIL-HDBK-217 are tools. Sure they can and have been misused by people that don't take the time to understand the tool and how it works. I hope that you will look beyond the humor of Bob's article and my response to see the value in both these tools. I don't see how you can survive in a modern high-tech industry without them.

If you're interested in this topic I can recommend a good companion article that addresses the issue of reliability prediction. It appeared in the November/December 1990 issue of the *Journal of the Institute for Environmental Science* and is titled "Use and Application of MIL-HDBK-217."

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# MIL-HDBK-217: It's Time To RETHINK IT

**I**n the January 10th issue of *Electronic Design*, the article "Design for Reliability Reshapes Designing," authored by Roy Wheeler, states that its purpose is to "convince you to take another look at the way you do your job." There's no questioning the high quality of the products of Mr. Wheeler's organization, Hewlett-Packard, or of their dedication to high quality. However, his products possibly could be made better and at lower cost if some fondly held ideas are modernized. Some of his reliability improvement recommendations are similar to some that are common to the aerospace industry, where reliability is the item of first importance and virtually any cost that yields improved reliability will be accepted. However, some activities should be questioned, for they may result in unnecessary costs and actually degrade reliability because of additional complexity.



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ENGINEERING  
ASPECTS OF RELI-  
ABILITY-ENHANC-  
ING ACTIVITIES  
EMPLOYED FOR  
ELECTRONIC  
EQUIPMENT.

My employer is concerned regarding the costs from following the recommendation taken from 217. We have joined with some 16 others who are equally concerned to sponsor research at the Electronic Packaging Research Center at the University of Maryland to improve the

technical base. We feel that a new paradigm for cost-effective reliability is badly needed, directed mainly to packaging issues.

The sources of concern are the beliefs:

- That parts are the dominant source of unreliability. Our research indicates that properly selected and installed parts are quite reliable and cause a trivial fraction of failures.

- That parts fail in a mathematically predictable way. We find that parts fail for a reason, and when the cause of the failure is identified and corrected, the cause is almost universally one of design, application, processes, etc., and not at all something that's predictable.

- That failures are accelerated exponentially by temperature. Our research indicates this concept to be fallacious. It appears that temperature is largely a scapegoat blamed for electronic failures, a fig leaf that covers technical nakedness. The temperature effects can be accommodated by design so that in moderate ranges, temperature can be removed as a consideration for reliability. Or stated another way, reliability would not be improved by lowering the temperature. Therefore, the challenge is to remove the cause of the problem, not to lower the temperature. Elevating the temperature for design can sometimes lead to major reductions in cost, weight, complexity, and other penalties.

- That screened or MIL-spec parts will operate more reliably. Our research indicates this isn't necessarily true. Part supplier controls and track record of successes are far more important.

- That derating to large amounts provides improved reliability. Our research indicates this isn't the case. Derating can allow use of poorly made parts, but a better tactic seems to at-

tack the source of the problem—manufacturing controls.

One example of the costs that can accompany the temperature ingredients of "Reliability" efforts illustrates the point. A major ground-based missile system is to be provided with a complex cooling system for electronics to improve the probability of the rocket's proper operation on demand. The rationale used by the reliability-and-manufacturability engineers was to take the specified MTBF of the boxes to be used and their coolant interface temperature, then select a new, lower, interface temperature that gives a calculated improvement to desired levels using 217's Arrhenius relationship. By so doing, a new temperature was established, and thus the operational requirement for a complex cooling system was established. All in the name of "Reliability." Never mind that there are no data concerning actual box performance, what the actual failure mechanisms are, or what stimulates them, or what role temperature plays, if any. Never mind that the cooling system itself is so complex that it's a plumber's nightmare, and weighs a ton-and-a-half!

Roy discusses examples of sources of unreliability that he has experienced. In each case, his corrective action required a design or process change. Doing the things encouraged by 217 to a greater extent wouldn't have made one bit of difference. Operating cooler, buying parts to tighter screening levels, or using fewer of them would not change anything except raise costs. These are the same conclusions as ours. Therefore, if it doesn't make any difference, why do it? And, how much of the activities that we do actually affect the end results, and how do we know? Could we do less of the expensive and complex things and not reduce reliability? These are important questions and it's time we have good answers for them. We don't have good answers now.

Roy's discussion concerning the futility of accelerated testing as a means to demonstrate reliability is puzzling. We have a good bit of information to demonstrate exactly the opposite. In fact, we're in the process of expanding our activities in this area, using the

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Packaging Research Center. Maybe I'll have a full story for the readers in the future.

For another vision of the same question, Bob Pease's Pease Porridge in the March 14, 1991 issue referred to a Guest Editorial of mine ("Is Reliability Prediction Methodology for the Birds?," *PCIM, Power Conversion and Intelligent Motion*, November, 1988). The message I relayed was that Failure Prediction Methodology, FPM, (MIL-HDBK-217, etc.) is erroneously based, causing damage to those who take guidance from its concepts. Some of the actions guided by FPM may not produce desired or intended results, all the while causing increased costs, complexity, and other penalties like increased weight and volume. To use Mr. Pease's expression, "worse than useless" definitely applies to certain current uses of FPM. Notwithstanding the gross deficiencies and misleading aspects of FPM, it has become widely accepted as engineering guidance for reliability, such that it's now the single most influential document in existence today affecting high-quality electronic equipment.

Mr. Pease picked up upon a portion of my argument, which stated that one should not look to lowered temperature as a means of improving the reliability or performance of electronic equipment. The source of unhappiness with equipment that's performing below expectations may have nothing at all to do with its temperature. He refers to the "silliness of 217," a sentiment I thoroughly support, though he recognizes that those in "some businesses" must use it regardless. He then goes on to state, "...but in the industrial and instrument business, we don't really have to follow its every silly quirk and whim." From this, one could assume that Mr. Pease has, and others in his field have, escaped the damage from FPM, and that they operate at greater heights of intellectual integrity by not being befuddled by FPM.

The concepts of 217, however, have pervaded even Mr. Pease's organization. The device manufacturing industry has years of complicity in perpetuating the foundation cornerstone of 217, the notion of the exponential ef-

fects of temperature (the "Arrhenius relationship") on reliability. Devices manufactured by his company, and those of virtually all others in the industry, are sold with representations of Arrhenius-based predictions of failures versus temperature. "Base failure rate" data are gathered by device manufacturers by their operating a number of devices at a high temperature/electrical stress, measuring operating time and counting failures. Then, using the Arrhenius relationship and other manipulations, they generate and publish the well-known curves of exponential failures versus temperature.

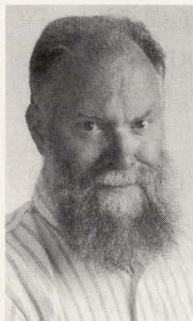
Never mind that the failures occurring at the high stress condition are due to failure mechanisms that don't usually follow Arrhenius. And never mind that the failures that do occur are usually due to built-in defects in the devices under test, which could be eliminated by closer process controls. The high stress failures are usually attributable to failure mechanisms that don't occur in properly designed systems. Extrapolating those failures at high stress conditions to more usual conditions of use employing Arrhenius models gives a falsely pessimistic picture of the failures that should be anticipated at lower-stress usual operational condition. Arrhenius models attach undeserved value to temperature reduction by emphasizing a quick fix rather

than exposing the problem.

When device manufacturers are queried concerning the technical base for their temperature/failure rate representations, the " $\pi T$  factor" of 217, their usual response is to the effect that "there's no basis for the representation, but that's what everyone else uses, so we do the same!!" They make the plea that to validate failure rates at lowered temperatures would take too long ( $10^6$  hours is 114 years!) to be of value. In fact, the time to failure at lowered stress conditions may actually be several service lifetimes for devices that are carefully controlled in the manufacturing process, applied properly, and installed with care.

It's time we look critically into the things we do to produce our products, and to open issues that have laid dormant for years. The statement has been made that 217 is a valuable tool and 25 years of good application is behind it. I can't think of a better reason to open it up for scrutiny. We did just that, and we're quite unhappy at what we've found.

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**BOB PEASE**

OBTAINED A BSEE FROM MIT IN 1961 AND IS STAFF SCIENTIST AT NATIONAL SEMICONDUCTOR CORP., SANTA CLARA, CALIF.

## WHAT'S ALL THIS MIL-HDBK-217 STUFF, ANYHOW?

**W**ith all due respect to Roy Wheeler's views, I must say that I tend to agree with Charles Leonard about MIL-HDBK-217. Just because a tool once did some good doesn't mean that it's not now systematically doing harm. Designing circuits and systems to meet 217 wastes a lot of time and energy and money that would be well invested in other methods of improving reliability.

As for derating factors that are foolishly maintained in

# THE CONTROVERSY

systems like 217, I must say that I once heard of a request from Hewlett-Packard for op amps and other ICs to have an absolute max rating of 2 x the operating voltage. Because it's unreasonable to ask a  $\pm 15$ -V LM741 to have an absolute max rating of  $\pm 30$  V, this leads to a system where LM741s can only be operated on  $\pm 9$ -V supplies. They can then have a 2:1 safety factor versus the normal  $\pm 18$ -V absolute max rating.

It really doesn't seem reasonable to me that LM741s operating on  $\pm 9$  V will be appreciably more reliable than on  $\pm 12$  or  $\pm 15$  V. It also seems unreasonable to specify high-voltage amplifiers such as LM344, just to be able to run on  $\pm 15$  V with a big safety margin. And, I don't see much point in operating TTL ICs on a +3-V supply to give them that 2:1 safety factor.

I've also seen many customers asking, "How many transistors are in your IC?" Of course, when we ask why they need to know, they explain that 217 requires them to. Now I see that Analog Devices has even started listing the "number of transistors" in the characteristics column of some of their data sheets, so that users can get this valuable (?) piece of information without bugging the customer-service people at ADI.

Of course, if the computed reliability isn't good enough with a 42-transistor IC, the reliability would be even better with a 22-transistor IC (just choose an amplifier with the input-protection transistors omitted and the output protect/current limit transistors deleted).

And it would be even higher yet with a UA702 that has only 9 transistors, RIGHT? But, Mr. Leonard is much more knowledgeable than I am in these areas, and I will let him address these topics.

At this point, I will address some of Mr. Wheeler's questions about what I said about statistics. First of all, when I attended MIT in 1961, NO, there was *not* any specific requirement to study a course in statistics.

In similar fashion, there was no specific requirement to study a course on digital computers or operational amplifiers. We did study lots of obscure

topics that were much more generally valuable, like large motors and microwave VSWRs.

Do I use statistics every day? I use many kinds of math, but almost always when I want to look at a distribution, I look at a one-dimensional distribution. Some people call them histograms, but around here we often call them "ADARTs", which is apparently an old name devised by Teradyne (I think it's an acronym for Automatic Distribution Analysis in Real Time).

I have an absolute preference for looking at ADARTs, and a well-rooted aversion to any analysis that simply says, "Average value = 1.20168 mV, sigma = 0.17357 mV." Too many evils are hidden when the data aren't Gaussian. Yes, it's *possible* to get your statistical tools to check the data to see if the distribution *is* Gaussian, but almost nobody checks that.

I mentioned in an earlier column that when the yield to a 1% accuracy spec is worse *after* trimming than *before*, somebody is being badly fooled. And letting the statisticians wield a bigger whip isn't likely to solve the problems. No, I eschew statistics. Yes, I use graphical methods of analysis, which I use to solve problems that other people get into when they let themselves be fooled by statistics and computers (not to mention spreadsheets that deceive and lie....). Some of our product engineers get some very good software that lets them provide two-dimensional plots (scatter-plots) that are quite educational. This I encourage...

Do other people at NSC use statistics? Well, I'm sure some people do. As long as they don't do any harm, so long as they don't do it in the streets and scare the horses, I shan't complain. But, when they screw up, well, I'm the guy they call in to fix the problem.

You ask me why I condemn statistics in my column. Well, already I'm getting letters from people who say "You think things are screwed up at *your* company, you should see how bad they are at *my* company."

Then some truly horrifying stories are spilled out. (So far, I've gotten about 150 letters about my column. A few dozen simply like my column. A few dozen agreed that Golden-Eared

experts were fools when it came to splices. But many people have volunteered examples of outrageous things in the industry).

Like the guy who wrote that his boss started to chew him out for having bad averages and bad distributions on some of his older designs. When he searched into the situation, he found that the test engineers were taking statistics on the data without throwing out the dead units.

So, if there were more *shorts* one week, and more *opens* the next week, the average value would go all over the place, even though the distribution of the *good* parts wasn't moving anywhere at all.

In another case, an engineer designed some operational amplifiers that had extremely high gain, well above 150 dB. The QC people condemned the performance because they wanted to see a correlation between the gain at room temp, and the gain at hot and cold. Well, the gain was so high that you could not see any correlation at all, so they made him do 100% testing at hot and cold, even though there was no rational reason to do so. They never did find any failures or problems, but they made him perform useless, unnecessary tests that were never required on low-gain or medium-high-gain amplifiers. He was willing to list a relaxed spec at hot and cold temperatures, to give a good safety margin, and ensure that a bad part would never be shipped that failed the spec. But the QC people refused to accept that on this very-high-gain part, even though that was permitted in the past.

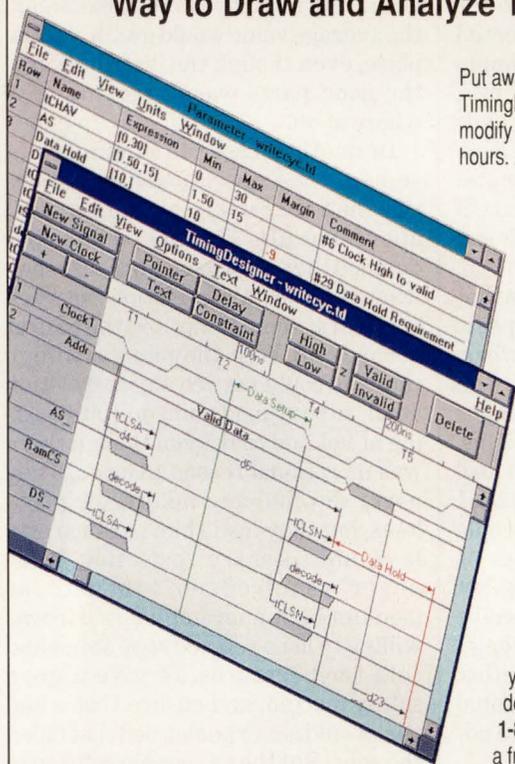
So, I will continue to point out that the absent-minded use of any computerized procedures, such as Spice, or Statistics, or Spreadsheets, or Analog Synthesis, or *any other mindless use of computers*, can lead to serious problems. Of course, there are absurd problems at many other places in the industry, and I'm pleased to see that many of Electronic Design's readers count me as a helpful resource when I point out these problems.

In Mr. Wheeler's column in this issue, he points out that "...it's a rare circuit indeed where you can place com-



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ponents on the board in the manner that was suggested... there are other design considerations that necessarily take priority over the placement of components for optimum passive cooling." Maybe in high-powered instruments, passive cooling isn't an important consideration—you just give up on the passive cooling and throw in a fan. But, if you don't let every other engineer pull an absolute priority over the need for wise location of hot components and good thermal management, it's indeed possible to negotiate a good thermal layout without degrading other electrical specifications. Certainly on *my chips*, I have to arrange the high-power components very carefully, as thermal gradients are a critical aspect of the performance. And I don't have any option to put a tiny little blower on the hot end of my chip to prevent it from heating the precision front end. Even 5 or 10 mW can be disastrous if not properly managed.

Just last week, I had to troubleshoot a "newly improved circuit," which the engineer had carefully analyzed with Spice and other tools. The performance was awful. Finally, I spotted a strategic error in the layout. It turned out there was absolutely nothing wrong with the schematic, but the circuit's performance was destroyed by a bad layout.

Therefore, when you use statistics, as with any kind of mathematical or computerized scheme, you do so at your peril. If you use the tools wisely, that's fine.

But, if you get in the habit of letting the computer do all of the easy stuff, you may forget the basics. Then you will gradually lose the perception of when a situation is normal and when it's going very wrong. I don't think you can train your computer to watch out for every kind of "wrong." And that's my point.

All for now. / Comments invited!  
RAP / Robert A. Pease / Engineer

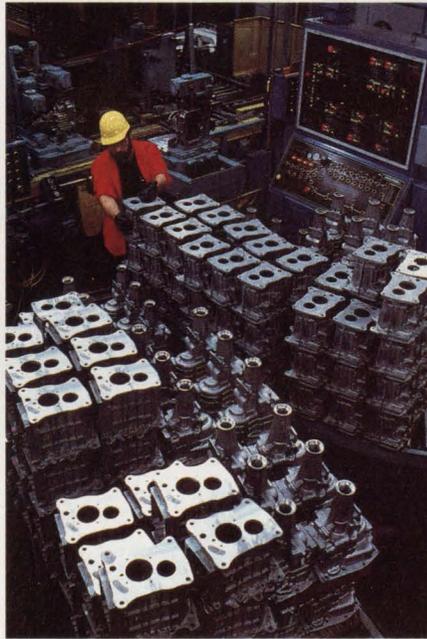
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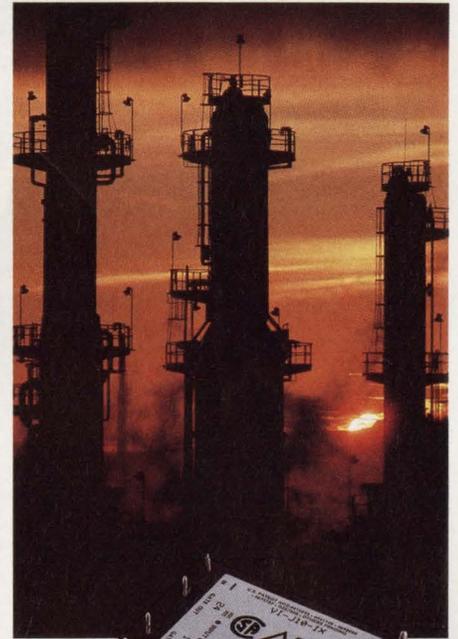
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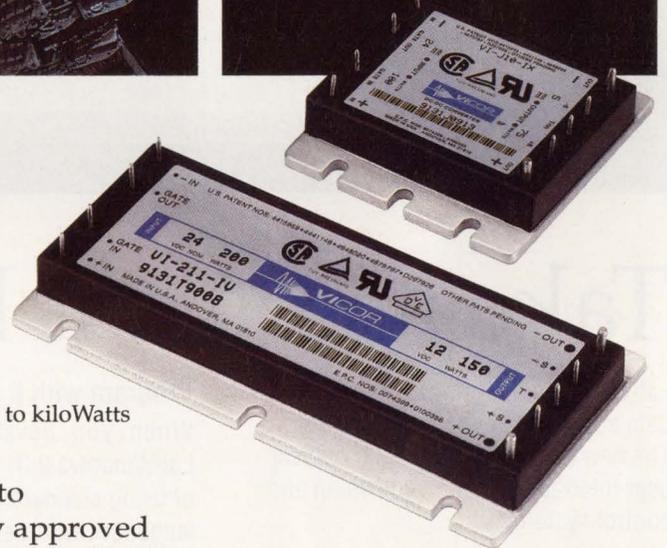
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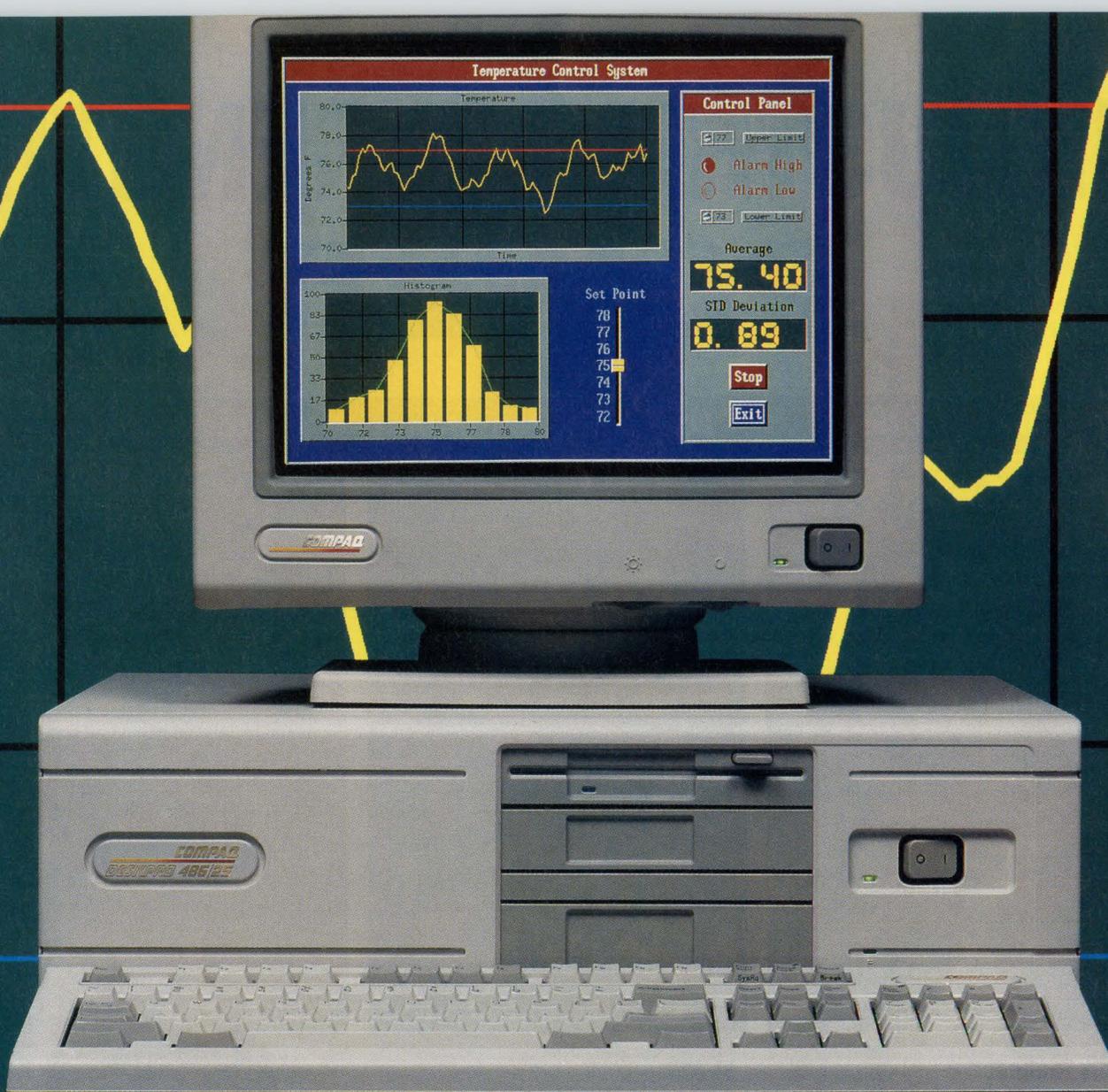


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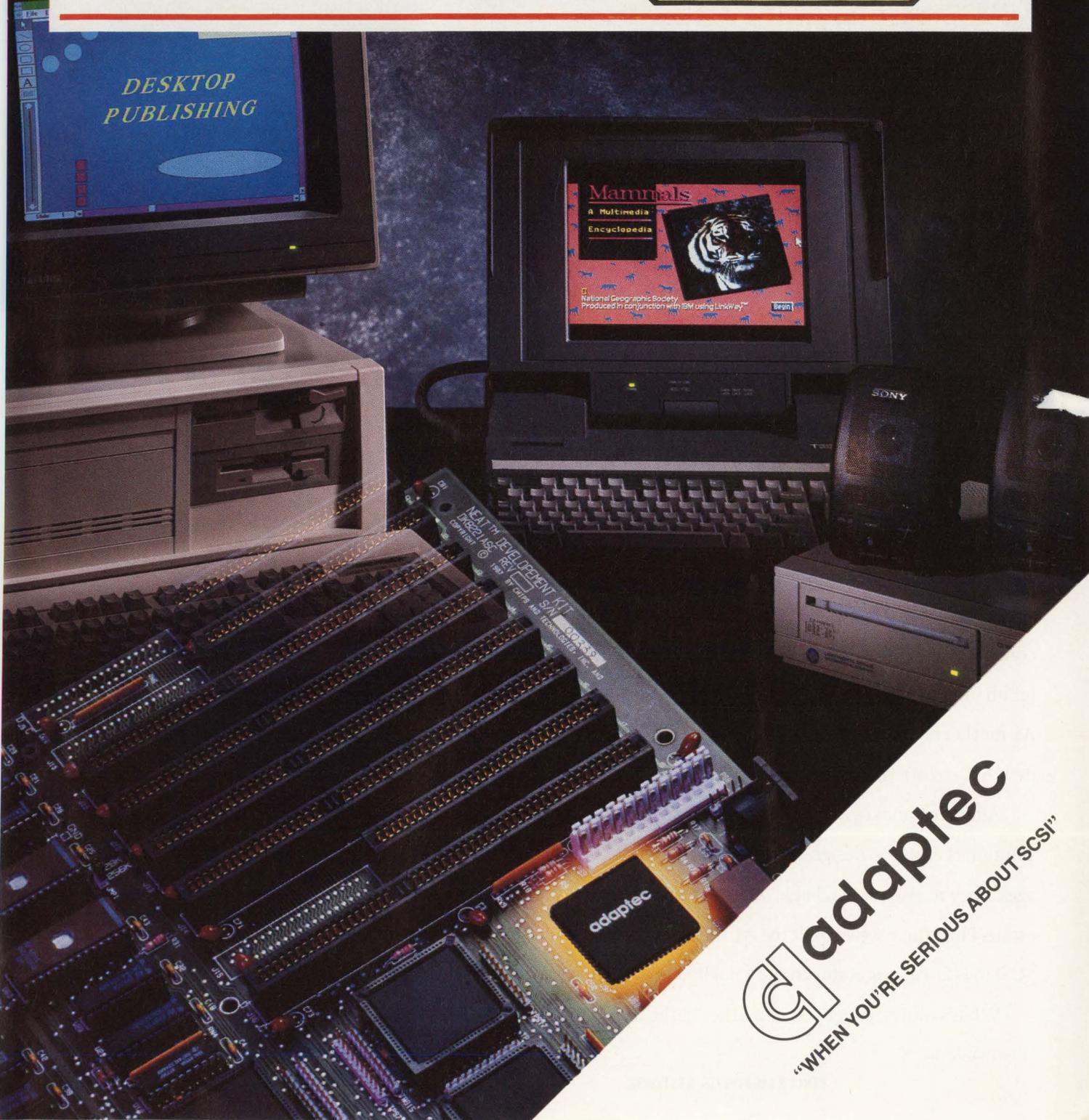
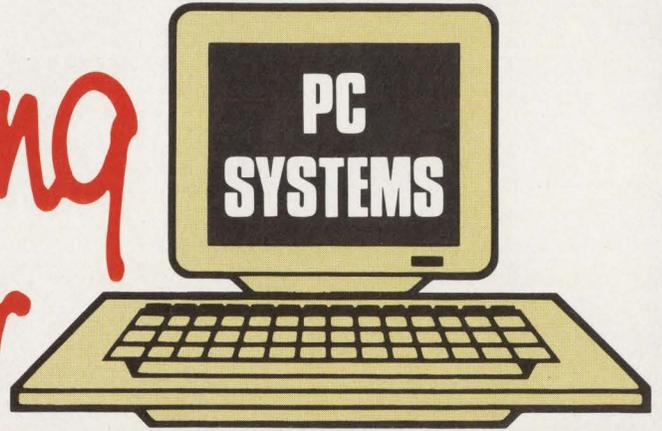
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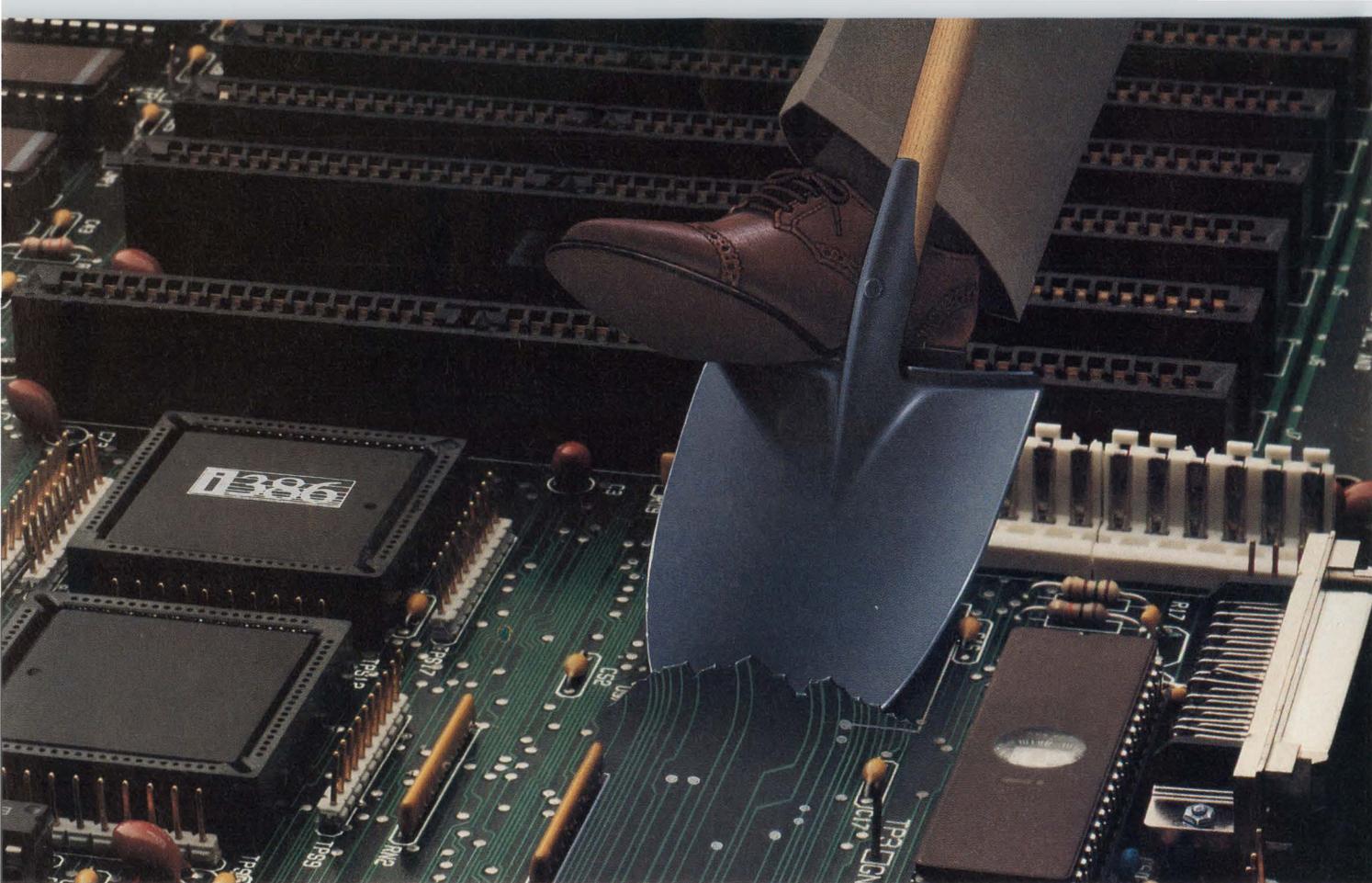
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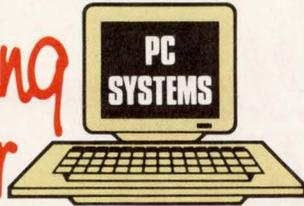
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## MACINTOSH PORTABLES GET TOTAL REDESIGN

A COMPLETE REDESIGN of the Macintosh portable by Apple Computer Inc., Cupertino, Calif., has cut system weight, improved usability, and packed more features into a smaller package. Apple's designers improved the base design and created three base models from which to select: the low-end 16-MHz 68000-based PowerBook 100, the mid-range 16-MHz 68030-based PowerBook 140, and the high-end PowerBook 170 made for the power user. The 170 employs a 25-MHz 68030 running with a 68882 math coprocessor. All three are notebook-style portables that deliver about three hours of battery life and weigh 5.1 to 7.5 lbs., depending on model and options. The PB 100 and 140 come with 2 Mbytes of RAM and a 20-Mbyte 2.5-in hard-disk drive. The PB 170 starts with 4 Mbytes of RAM, a 40-Mbyte hard-disk drive, and a built-in 2400-baud MNP5 modem. Unlike the original portable, the PB 100 and 140 use a passive-matrix 640-by-400-pixel flat-panel display, with backlighting standard. An active-matrix display, however, is used in the PB 170. All keyboards include a built-in trackball mouse. But unlike the first Mac portable that has a left- or right-side mounting option, the new portables have the trackball mounted in the center of what would be the keyboard region. And unlike conventional laptops that place the keys at the lowermost edge of the computer, the keys are pushed up near the top of the machine, near the hinges that hold the display panel. That design gives users a clear palm-rest area on the computer, hopefully reducing wrist strain and preventing the lower keys from being mis-struck from unintended pressure from the edge of the hand. Base prices for the portables range from \$2300 to \$4600. Call Apple at (408) 996-1010. DB CIRCLE 455

## PC CHIP SETS SUPPORT 3.3 V FOR 386, 486

A PAIR OF CHIP SETS and a single-chip motherboard logic subsystem—the Bluejay, Falcon, and Eagle—have been optimized from the ground up to support the 80386DX, 80486, and 386SXL processors. The trio of chip sets are available from Elite Microelectronics Inc., San Jose, Calif. The Bluejay single-chip subsystem works from a 3.3-V supply and operates with a 20- or 25-MHz CPU. The Falcon chip set for the 486 (the e88C411 and C412) includes “power-burst” data transfer for a second-level cache and the DRAM main memory. All cache-control logic, except for the tag RAMs, is on the C411 memory/cache control chip. A five-word-deep posted-write buffer in the Falcon chip set improves CPU performance by allowing the CPU to write several words sequentially into the buffer without waiting for the memory subsystem. Writes are done in the background while

the CPU begins its next task. The power-burst sequence moves data in 2-1-1-1 bursts for cache transfers and 3-1-1-1 for DRAM transfers, improving overall data-transfer efficiency. The chip set also implements a local-bus interface, which when used for time-dependent I/O functions such as video output, can enhance system performance by almost 20% over the AT-bus I/O interface. The Eagle chip set for the 386DX, unveiled late in 1990, will be upgraded to 33- and 40-MHz versions. Each chip has power-management logic to help minimize system power consumption. Samples of all chips are available. Call Jeff Winters at (408) 943-0500. DB CIRCLE 456

## NEW BATTERY SCHEME TRIMS WEIGHT AND SIZE

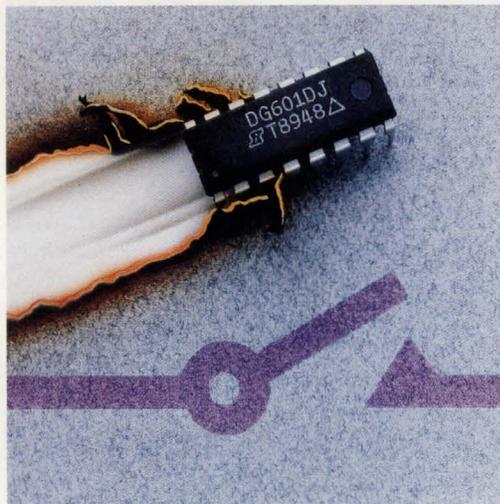
A VALVE-REGULATED sealed lead-acid rechargeable battery, designed as a flat, thin package—just 3.12 by 5.32 by 0.332 in.—has the right shape to fit neatly into portable computers. The rectangular cell uses space much more efficiently than cylindrical or cube-shaped batteries. The planar energy cell from Portable Energy Products Inc., Scotts Valley, Calif., provides improved lead-acid efficiency—between 40 and 60%—over earlier lead-acid cells. It has an accurate “gas gauge” voltage-decline characteristic that can determine the exact amount of charge remaining, enabling users to gauge the amount of system use time available. The lead-acid cells also have a slow self-discharge rate. They can be left fully charged on a shelf for about a year before recharging. The initial cell to be released, the PLA350250, is specified at 2 V, and 5 ampere-hours. In lots of 200,000, it will go for \$6.50 apiece. Contact Gerry Monneypenny, (408) 439-5100. DB CIRCLE 457

## LAN ADAPTERS, TOOLS, ENHANCE NETWORKS

A HIGHLY INTEGRATED seven-chip card design for a 16-bit (AT-bus) Ethernet (thick or thin cable) or 10baseT unshielded twisted-pair cable has been developed by Intel Corp., Hillsboro, Ore., for high-performance networking. And for even higher performance, there's a 32-bit EtherExpress bus-master adapter for EISA-based systems. Token-ring cards are available for 8- or 16-bit ISA, 16-bit Micro-Channel-Architecture, and 16-bit EISA bus-based systems. The TokenExpress cards operate at 4 or 16 Mbits/s with shielded or unshielded twisted-pair cabling. List prices for the network adapter cards range from under \$200 to almost \$900 in single-unit lots. To support the large networks, Intel also created NetSight, a family of network-management tools. These include NetSentry, a full-featured network monitor; Analyst, a low-cost portable protocol analyzer; and NetSight Professional, a combination monitor and analyzer that includes real-time data collection and diagnosis. The tools are supported by a software utility, LanSight Support, a windows-compatible upgrade of Intel's previously released version of LanSight. For groups sending facsimiles from network nodes, Intel has also developed fax server software that runs on the previously released SatisFAXtion board. The software consists of the server software and LanSpool FAX, a routine that brings out-bound fax capabilities to the just-released LanSpool 3.0 print server. Contact Intel at (503) 629-7354. DB CIRCLE 458

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# Comdex/Fall '91: Data Storage Still Ranks High Among The Issues

*Floppy-drive and tape-backup technologies don't sit back and rest on their laurels.*

BY RICHARD NASS

Like last year's event, disk drives are the talk of the town at this year's Comdex/Fall '91. But whereas hard-disk drives took center stage at last year's show, floppy-disk drives are stealing some of the scenes at this year's meeting. Also receiving more attention are magnetic-tape drives for backup applications.

Both floppy- and hard-disk drive capacities are increasing as their size shrinks. Last year, the show emphasized hard-disk drives, which took the path lined with higher capacities and smaller form factors. One such case was the unveiling of a 2-1/2-in. hard-disk drive with substantial capacities. Now the floppy-disk drive is taking that small form-factor, high-capacity trail.

The Flextra drive from Brier Technology Inc., Norcross, Ga., is an example of this trend. The company has been shipping its 25-Mbyte Flextra floppy-disk drive for about a year, and has recently increased the drive's throughput performance by 70%. The throughput increase comes from adding internal caching to the drive.

Brier's drive differs from typical floppy-disk drives in how it reads the patterns on the disk. The conventional drive uses a stepper motor that has no way of knowing its position because it lacks feedback from the media. On Brier's proprietary media, an embedded servo pattern is written to both sides of the disk. The pattern saturates down through the coating to the Mylar, but not through to the other side.

The pattern consists of curves going in one direction on one side of the disk and in the opposite direction on the other side. The servo head on each side of the disk reads the pattern. When writing, the head moves across the disk and drops a string of data by sending a current pulse through the head. Then, the process continues—the head moves across to the next set of curves, drops another string of data, and so on, with short time intervals between the two heads. The heads keep track of their position by noting the time interval between them. Hard disks, unlike conventional floppies, use a servo scheme.

The servo track separates Brier's drive from competitor's drives because of its precision. In addition, Brier feels that it can take the drive to even higher capacities. The company says that there wasn't any standard for this type of "media tracking" when the Flextra was first announced. Now, some high-density floppies use a scheme called sector servo, where the drive gets information from the disk, but not in a continuous fashion like the Brier disk. The head moves along the disk searching for the information. Also,

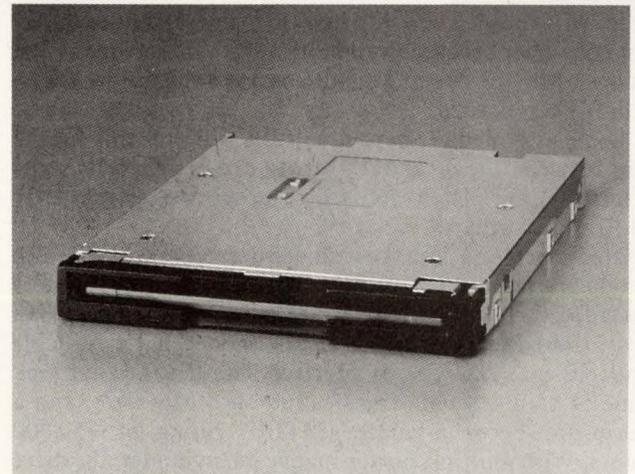
the Brier head-carriage mechanism is a voice-coil actuator that operates at a very high speed—14 ms from track to track. The stepper motor used in traditional floppy-disk drives is inherently slower.

The barium-ferrite material used in the Brier media differs from that used in standard 1.44-Mbyte disks. However, it's the same material that's employed in the 4-Mbyte disks released recently. Users get the 25-Mbyte disks directly from Brier for about \$25. The drives start at \$850 each.

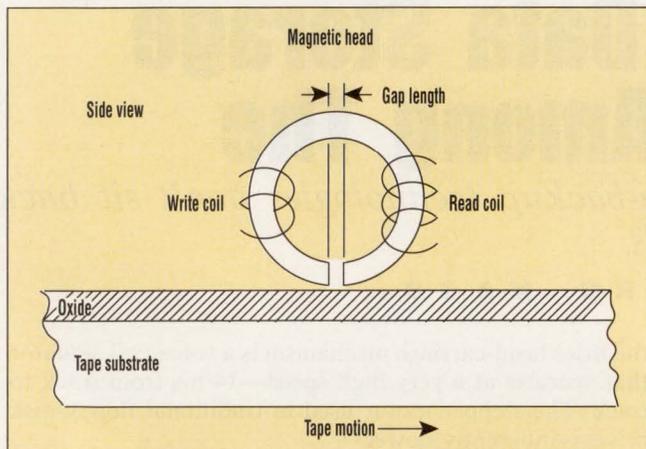
A second floppy-disk drive just released doesn't focus on high capacity, yet it's the smallest 3-1/2-in. floppy-disk drive currently available. Teac America Inc., Data Storage Products Div., Montebello, Calif., offers the FD05 with a height of just 1/2 in. (Fig. 1). The company feels that it has reached the theoretical size limit with the FD05.

Teac's designers met many challenges in trying to squeeze a fully compatible drive into a 1/2-in.-high form factor. One obstacle was that there couldn't be much extra space when inserting the disk. In a 1/2-in.-high unit, the path the media follows when entering the drive must be very specific—there's no room for play. Because the drive is built with dual heads to read the information on either side of the disk, the head-carriage assembly had to be made much thinner. Also, the drive's sheet-metal cover is thinner than its base by 0.1 mm to provide some extra clearance.

Other floppy-disk drive makers have released near-1/2-in. models. For example, in June of this year, Mitsubishi



1. Low-profile 3-1/2-in. floppy-disk drives were previously 1-in. high. Teac's FD05 cuts that form factor in half—the drive measures 12.7 mm (1/2 in.).



2. The gap length in a read/write head is the opening between the read and write head coils. Newer head materials, such as thin films, allow a smaller gap length, which leads to higher storage capacities.

Electronics America Inc., Torrance, Calif., released a 14.8-mm-high drive. The MF355E drive features downward read-write operation and power-saving options when in the standby mode. At the time, Mitsubishi said it was the smallest drive available.

To push a 2-Mbyte floppy-disk drive to a 4-Mbyte capacity, its head must be modified. The magnetic head gap in the 4-Mbyte drive is much narrower than in the 2-Mbyte unit, meaning that the magnetic pattern laid down on the disk is smaller. As a result, more patterns fit on the disk. Because different media types are used, a 2-Mbyte disk will work in a 4-Mbyte drive, but only in the 2-Mbyte mode. A 4-Mbyte drive, on the other hand, works in three modes: 4 Mbytes (2.88 Mbytes formatted), 2 Mbytes (1.44 Mbytes formatted), and 1 Mbyte (720 kbytes formatted).

As volumes go up and cost comes down, 4-Mbyte floppy-disk drives should replace 2-Mbyte drives, even though a 4-Mbyte drive is harder to build due to its more complex read/write head. The 4-Mbyte system does require a different controller because the data-transfer rate is twice as fast as the 2-Mbyte system. This also means a change in the system BIOS is needed.

Some intermediate-capacity drives will probably fill the gap between the 4- and 25-Mbyte drives. There is some effort, for example, to standardize these drives, particularly at 10 and 20 Mbytes.

Not to get left out in the cold, hard-drive makers are also producing large-capacity and small form-factor drives. For instance, there's the Apache 2585 from Maxtor Corp., San Jose, Calif., an 85-Mbyte 2-1/2-in. model that's available with either an AT or SCSI interface. The drive boasts a seek time of 15 ms, a data-transfer rate of 8 Mbytes/s, and a mean-time-between-failure (MTBF) rating of 250,000 hours. With multiple power-management modes, the drive draws 1.1 W when idling, 0.2 W in the sleep mode, and 2.7 W during read/write operations. By using a high level of VLSI technology, all of the 2585's components fit on one side of a board. The dual-platter 2585 weighs 6 oz. OEM-

quantity pricing is \$395 each.

A second 2-1/2-in. hard drive shatters the 100-Mbyte barrier. The ST9144 from Seagate Technology, Scotts Valley, Calif., holds 128 Mbytes on its three platters. The drive boasts an average seek time of 16 ms and a latency of 8.7 ms. The four-phase power management cuts the power consumption in seek and read-write modes to 2 W, 1 W in idle mode, and 0.3 W in standby and sleep modes. The drive can withstand an operational shock of 10 Gs (150 Gs non-operational) and has an MTBF of 150,000 hours. Its operating environment is from 5° to 55°C. Priced at \$595, evaluation units of the ST9144 will be available in December, with production scheduled to commence in the first quarter of 1992. Two versions will be available, one with a PC/AT interface and one with a SCSI interface.

Floppy-disk drives are only part of the removable-media story gaining momentum. Tape backup is also receiving much attention. Because designers now work with extremely large files, these files can't be backed up easily on floppy disks. This is where magnetic-tape storage comes in. Thanks to some recent developments in the Quarter-Inch Cartridge (QIC) Committee, a magnetic-tape standards group, tape backup is becoming quick and easy. And the number of magnetic-tape drives sold indicates users' increased confidence in this method. According to QIC, the installed base of 1/4-in. tape drives exceeds 7 million.

There are two main classes of 1/4-in. cartridge drives, the mini cartridges (DC2000) and the large full-size data cartridges (DC6000). QIC 40 and 80, two drive standards, both employ floppy-drive interfaces using a modified-frequency-modulation (MFM) code. Cost can be reduced by sharing an interface with a floppy-disk drive. The difference between QIC 40 and 80 is the linear recording density and track pitch. The former's recording density, specified in flux reversals/in. (FRI), is 10,000 FRI on 20 tracks; the latter's recording density is 14,700 FRI on 28 tracks.

Quarter-inch cartridge technology uses longitudinal recording, meaning that each recording stripe goes the full length of the tape. Within each stripe, one bit is recorded in 1/14,700 of an inch. Therefore, there are 14,700 possible polarity changes/in. on each stripe.

On the smaller tape drives incorporating a floppy interface, data is stored similarly to how its stored on a floppy disk. Both devices store in sectors, but the tape puts several tracks on one physical tape track. Hence, the data for a particular file is all in the same place, making recovery quicker. On a disk, data is scattered about, wherever there's unoccupied space.

Tapes can be interchanged between different manufacturers' drives as long as both drives comply with the QIC physical and logical interchange standards. The physical standards correspond to the FRI and the track width, while the logical standards correspond to the directory structure (how a file and filename are saved).

By using a different material to construct the heads, higher track densities could be used. The tapes can go up to 42,000 FRI and 34 tracks. Typically implemented in metal, the new heads will be fabricated from thin films, like the

magneto-resistive (MR) types under investigation. That lends them to smaller gap-length geometries, and, in turn, higher precision (Fig. 2). A smaller gap length also helps push the drives to higher capacities.

Today's read/write heads employ inductive pick-ups in the gap to sense magnetic-field changes. Conversely, thin-film heads use a resistive element in the gap. Changes in the resistance value corresponding to magnetic-field changes are sensed. Magneto-resistive heads are desirable because the tape can pass by at any speed. Therefore, the tape drive could theoretically run as fast as the computer, even in a multiuser system.

MR heads are also turning up in hard-disk drives, specifically in a drive released by IBM Corp., Rochester, Minn. Its 1-Gbyte drive fits in a 3-1/2-in. form factor.

As tracks become narrower in magnetic-tape storage, the need grows for a servoing technique like that used in floppy- and hard-disk drives. That's because moving tape doesn't always follow a perfectly straight path, making it even more difficult to read narrower-width tracks. The use of servoing could lead to an increase in the number of tracks, from 30 to 144. In fact, the QIC committee recently decided to adopt servoing technology. Using the new technology, storage levels in large cartridges can be pushed from 2 to 10 Gbytes, and in mini cartridges from 400 Mbytes to 3 Gbytes.

Using the servoing technique, prewritten servo tracks are incorporated onto the tape. Then, a servo mechanism is built into the drive to follow these tracks with high precision, increasing the tape's track density. "Servoing will probably appear on the next generation of magnetic-tape drives, in about two years," says Alan Richards, vice president of engineering at Colorado Memory Systems, Loveland, Colo., one of the leaders in 1/4-in. tape drives.

The QIC committee is also looking at run-length limited (RLL) coding. This approach pushes the recording density to 50,800 FRI, translating to 67,733 bits/in. RLL coding supplies more bits per inch than the number of flux repetitions. The information on the tape can be coded so that it transmits with fewer flux reversals. One flux reversal isn't needed for each bit change. For example, if there are five consecutive ones, each bit wouldn't require a flux reversal. Therefore, fewer changes are made in the magnetic field to

transmit the same data.

In addition to rising capacities, transfer rates in 1/4-in. tape drives have also increased. With the servoing drive, two channels can be active at one time, doubling the transfer rate. Using QIC 80, the transfer rate ranges from 63 to 125 kbytes/s.

On the system side, Sparc-based computing has elbowed its way into the Comdex foray. The Sparcbook 1, from Tadpole Technology Inc., San Jose, Calif., is a notebook-sized computer based on the Cypress Semiconductor CY7C-601A-25UC integer unit running at 25 MHz. Coupled with the 604A Sparc reference MMU and 64 kbytes of zero-wait-state cache memory, the Sparcbook 1 offers 18 MIPS of performance.

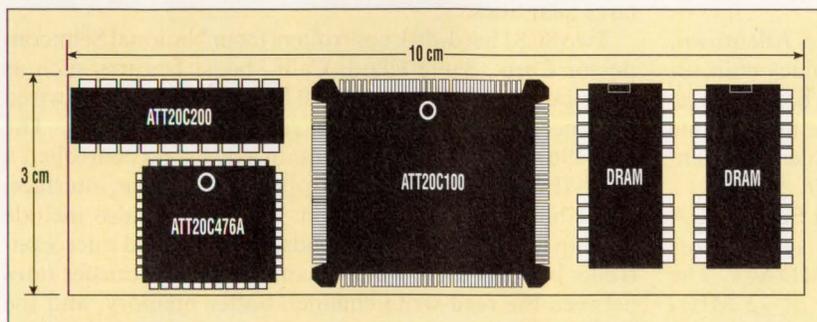
The core system is built with two conventional pc boards with parts surface-mounted to both sides of the boards. The core consists of the processor, 8 or 32 Mbytes of DRAM, and an Ethernet interface. The system offers DOS emulation, running as a task under Unix. Prices for the Sparcbook 1 start at \$5950 for an 85-Mbyte hard-disk version.

AST Research Inc., Irvine, Calif., recently announced what the company calls the fastest notebook PC available—a 25-MHz model. The Premium Exec 386SX/25 is based on AMD's AM386SXL-25 processor. The 7-lb. computer features 4 Mbytes of RAM and an 80-Mbyte hard-disk drive. The AMD processor gives users the advantage of high speed without sacrificing any battery life. The system sells for \$4795.

A third portable PC, the SuperTablet from Tusk Inc., Lake Park, Fla., is one of the first that's based on Intel's 386SL microprocessor. The system can handle either a pen or keyboard input. The 6-lb. computer comes with an 11-1/2-in. VGA display, a 124-Mbyte shock-proof hard-disk drive, 64 kbytes of cache memory, and 8 Mbytes of RAM, expandable to 32 Mbytes. A 9600-baud modem is standard. The system will eventually run such operating systems as DOS, UNIX, OS/2, Windows 3.0, PenApps, and Pen-Point. Prices for the system will probably range from \$5500 to \$6500 each.

The SuperTablet should be in volume production in the first quarter of next year. Though Tusk wants to make the system available earlier than next year, the operating systems from Go Corp., Foster City, Calif., and Microsoft Corp., Redmond, Wash., aren't ready yet. "The real market for pen-based systems will take off when Windows for pen systems becomes available," says Chuck Krallman, Tusk's chief executive officer.

The system has three modes of operation. It can be used as a notebook PC, a desktop computer, or as a pen tablet. The detachable display, called the roving unit, contains all of the computing power. Consequently, the roving unit is all that's needed to take the system on the go as a pen portable. As a desktop, the entire computer hooks up to a docking station.



3. A VGA graphics subsystem can be constructed with just five chips. The design occupies just 30 cm<sup>2</sup> (shown here in actual size). This implementation is suitable for portable-system design.

The SuperTablet is encapsulated in a ballistic housing that's made to withstand all of the bouncing around experienced by a portable system. "We've even shot one of our machines with a shotgun and it survived," said Krallman. The unit is completely sealed and can even be dropped in water.

A small circuit board inside the pen alleviates some of the intelligence typically needed by the digitizer. The digitizer has a resolution of two-thousandths of an inch. The pen's point is equipped with a button that clicks when it's touched to the screen, activating the pen. There's also a second button on the pen that operates like a mouse button.

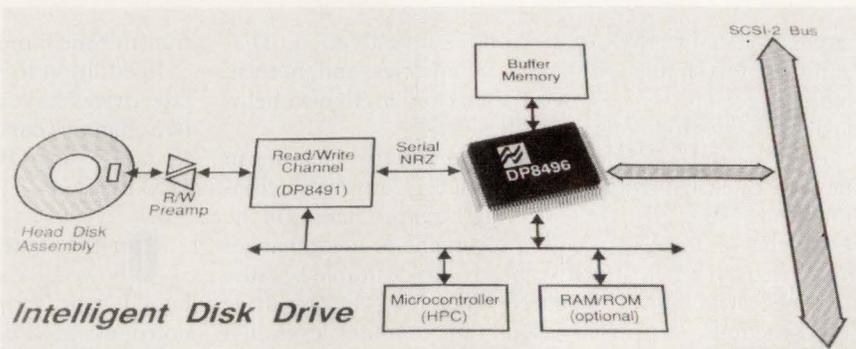
Tusk tried to implement as many features of the 386SL processor as possible. Virus protection plus suspend-resume and clock slow-down features that turn off certain components are three that were instituted. Because other features will be implemented later, Tusk employed a telephone-upgradable BIOS. This way, users can upgrade at a later time.

A second pen-based system that employs a 20-MHz Intel 386SL is the PenMaster, from Samsung Information Systems America Inc., San Jose, Calif. Built for the power user, the system can hold 20 Mbytes of RAM and a 120-Mbyte hard-disk drive. The system's software permits the stylus to write or edit documents by printing on the back-lit VGA screen. In addition, users can delete a word by drawing a line through it, or add a word or phrase by inserting a caret at the desired location. The 5-lb. computer measures 9.25 by 11.5 by 1.48 in. Samsung plans to sample the PenMaster in April of 1992, with production starting in September.

Pen-based computing is on the minds of many leading-edge designers, exemplified by a forum at Comdex devoted to that topic. The forum, Comdex Jumps (Japan-U.S. Marketing Partnership Summit), invites the U.S. and Japanese companies to jointly participate in a series of product presentations and demonstrations, discussions of technology, and informal one-on-one sessions. Some of the participants include Grid Systems, IBM, Microsoft, NCR, PenMagic Software, and Phoenix Technologies.

**A**t the chip level, AT&T Microelectronics, Allentown, Pa., is offering a high-resolution graphics chip set that shortens the design cycle and reduces board space. These two features make the chip set suitable for portable PCs as well as desktops. In a motherboard implementation, the board space required is just 30 cm<sup>2</sup> (Fig. 3).

The 0.9- $\mu$ m CMOS chip set consists of a Super VGA controller (ATT20C100), a clock synthesizer (ATT20C200), and a selection of four RAMDACs. The controller manipulates data to the monitor at 72 MHz, while supporting a 70-Hz video-display refresh at a resolution of 1024 by 768 pixels. The single-chip controller is housed in a 132-pin quad flat pack.



4. The DP8496 SCSI hard-disk controller from National Semiconductor supplies on-chip single-ended transceivers to drive the SCSI II bus. The part maximizes data transfer by offloading tasks from the drive's embedded microcontroller.

The clock synthesizer has 32 selectable frequencies, up to 80 MHz. Because the device has an on-chip loop filter, no external loop-filter components are needed. A power-down input, packaged in a 20-pin DIP, is offered for portable applications.

The set of RAMDACs (ATT20C475A/476A/477A/478A) is plug- and function-compatible with industry-standard parts. The 6- or 8-bit devices are each available in versions running at 66, 80, 100, or 110 MHz. Typical power consumption for the RAMDACs is 500 mW. Available with an on-chip voltage reference accurate to better than  $\pm 3\%$ , these parts can also be powered down.

Samples of the AT&T chip set are available now. The controller will go into production in the first quarter of next year; the clock synthesizer is slated for the second quarter. The RAMDACs are in production now. Evaluation kits for each chip, which are available now, consist of an evaluation board, an application manual, and all of the necessary software.

Also designed for portable computers is the Si9405DY, a p-channel logic-level load switch that overcomes the difficulties of high-side load switching. The part, from Siliconix Inc., Santa Clara, Calif., doesn't require the extra drive circuitry typically needed by n-channel high-side switches. It also has a very low on-resistance (0.12  $\Omega$ ), even when operating from logic signals. Housed in a compact SO-8 package, the Si9405DY is available now for 95 cents each in large quantities.

Two SCSI hard-disk controllers from National Semiconductor Corp., Santa Clara, Calif., boast features such as SCSI-bus transfer rates up to 10 Mbytes/s and a hardwired sequencer that permits data rates of 50 Mbits/s. The DP8496 and DP8497 each contain a disk data controller, a SCSI-II-compatible bus controller, a processor interface, and a buffer-memory manager. The devices also include on-chip intelligence that offloads the embedded microcontroller in a disk drive while maximizing data-transfer rates between the read-write channel, buffer memory, and the SCSI bus.

The DP8496 supplies on-chip single-ended transceivers for driving the SCSI bus, while the DP8497 offers all of the

## COMDEX PREVIEW

control signals necessary to control external differential transceivers (Fig. 4). Both chips are available now in 100-pin plastic quad flat packs. Large-quantity prices start at \$23 each for a 33-MHz version.

An IC that's designed to read the photoelectric current in optomagnetic disk drives comes from Fujitsu Microelectronics Inc., San Jose, Calif. The MB4150 read amplifier is a wide-bandwidth (40-MHz typical) part dedicated to reproducing the data stored on high-speed, read-write optomagnetic disks. It extracts the magnetic-optical (MO) and address-identification signals from the current levels of two photodiodes. The read amplifier contains two balanced I-V amplifiers that convert the photodiode currents into equivalent voltage levels. From these voltages, a summing amplifier and a differential amplifier obtain the ID signal, while a second differential amplifier extracts the written data. Available now in a 16-pin shrink small-outline package, the MB4150 read amplifier is priced at \$5 each in 1000-piece quantities.

S-MOS Systems Inc., San Jose, Calif., a pioneer in low-power and low-voltage components, has released a 3-V floppy-disk controller that's earmarked for next-generation drives. Called the SPC2055, the IC combines high speed and density with the low power consumption needed to effectively build 4-Mbyte floppy-disk drives. Data rates up to 1 Mbits/s are supported.

The 3-V part's high speed is facilitated by an on-chip analog phase-locked-loop data separator. The separator connects directly to the PC's bus through high-current line drivers of 12 mA from the host and 38 mA from the drive itself.

The SPC2055 is housed in an 80-pin quad flat pack and a very-thin quad flat pack (VQFP). The VQFP's height is a mere 1.4 mm. The part will be sampling in December and should be in volume production in the first quarter of next year. In quantities of 1000, it will sell for \$5.50 each.

As always, Comdex hosts a diversity of products that are usually launched at this trade show. For example, MiniBoard, a multifunctional miniature keyboard, is being released by Marquardt Switches Inc., Cazenovia, N.Y. The 82-key keyboard features all of the functionality of a full-size keyboard, even though it measures just 12.2 by 5.91 in. MiniBoard is fully compatible with the IBM PC/XT/AT and PS/2 formats.

This year's Comdex conference features two new showcases, each with its own dedicated site: multimedia and network computing. There will be a host of conference sessions addressing multimedia, supported by IBM, one of the leaders in this technology. There are also a number of sessions devoted to networking technologies, products, and applications.

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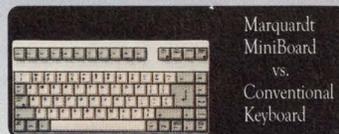
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# COMING ATTRACTIONS...

## NOVEMBER 7 CASE

Object-oriented technology is receiving more and more attention—many claim that it will make development problems easier. In fact, object paradigms touch numerous aspects of code development, often in surprising and not so obvious ways. Our Design Application Feature this issue offers a fresh look at CASE and how this leading-edge technology is making designer's lives easier.

## PROGRAMMABLE LOGIC DEVELOPMENT TOOLS: A DESIGNERS' GUIDE

One of the fastest growing market segments, programmable logic development tools enable designers to

greatly shorten time to market and get their products to market fast. This *Electronic Design* special, edited by CAE Editor Lisa Maliniak, consists of two Design Application Features as well as a manufacturers guide to design tools for programmable logic. There's also a bevy of new product modules, which bring designers the very latest in this hot marketplace.

## IDEAS FOR DESIGN

*Electronic Design* was the first and is still the leader with innovative circuit designs. We show our readers how to hook up the total system—from passive to active components. That's why *Electronic Design's* Ideas for Design continue to be "readers' favorites" month after month.

## November 21 ANALOG AND MIXED-SIGNAL ASICs

If designers can put their analog or mixed-signal circuit or system on a printed circuit board, they can also put it on one or several ASICs. Doing so will cut size, cost, and power; increase reliability and the proprietary nature of their product; and raise product performance. In this Technology Analysis Feature, our resident analog expert Frank Goodenough offers a series of brief case histories based on a survey of 30 engineers designing with mixed-signals. He examines the problems they encountered as well as their solutions. It's a *must-read* for any designer interested in this cutting-edge technology.

## SPECIAL SECTION: PIPS

(Power sources, Interconnections, Passive components, and Switches and relays)

*Electronic Design's* popular PIPS sections are a unique look at basic products. Our PIPS coverage this issue focuses on packaging, EMI and RFI shielding, and materials, including a who's who of these manufacturers and their products, giving this issue great shelf-life. In addition to a technical article on packaging, power, interconnections, passives, switches and relays are all capsulized.

## WESCON PREVIEW

This year's WESCON (Nov. 19-21, San Francisco) promises to be one of the year's major showcases for manufacturers of components, interconnections, test instruments, hardware, and CAE software. Communications Editor Milt Leonard previews major new product introductions as well as technical papers to be presented at the show. This horizontal industry-wide show/feature is geared toward all senior designers and test engineers.

## IN EVERY ISSUE...

Our Ideas For Design along with our Technology Newsletter, New Products, and Quick Look sections bring *Electronic Design* readers the latest in test and measurement, computer-aided engineering, and components.

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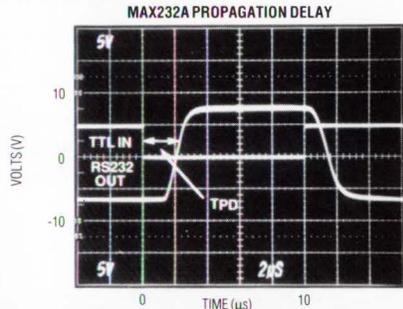
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## Analog Solutions For Tough Design Problems

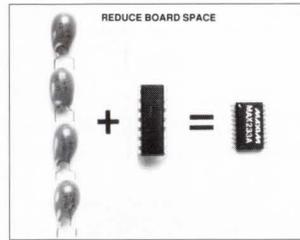
### New +5V RS-232 Transceiver Doubles Speed of Existing +5V RS-232 Devices!



The **MAX232A** +5V dual RS-232 transceiver is guaranteed to operate at data rates up to 116kb/s, while driving real loads – 250pF and 3kΩ. And, the MAX232A uses space-saving 0.1μF caps.

(CIRCLE 238)

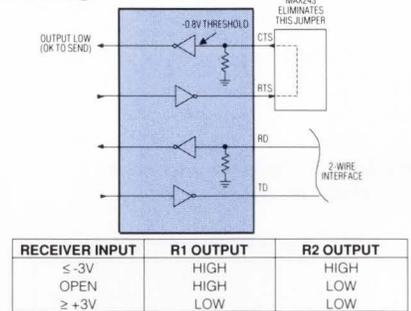
### +5V-Powered, Dual RS-232 Transceiver Needs No External Components



The **MAX233A** dual RS-232 transceiver saves board space by integrating all charge-pump capacitors needed for +5V operation within a 20-pin DIP or SO package. Guaranteed data rates up to 116kb/s.

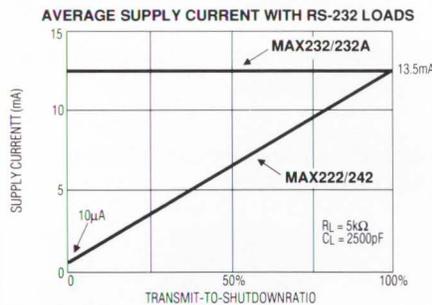
(CIRCLE 239)

### RS-232 Transceiver Simplifies Cabling



The **MAX243** switches between 2-wire and 4-wire interfaces without interrupting communications, and requires no cable change or extra jumpers. This device operates with 0.1μF capacitors, and is guaranteed for data rates up to 116kb/s. (CIRCLE 240)

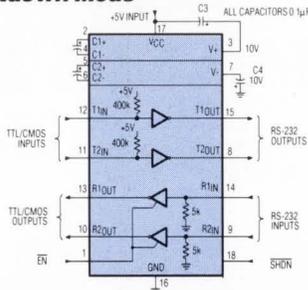
### RS-232 Dual Transceiver Saves 67mW of Power in Shutdown Mode



The **MAX222** dual transceiver is guaranteed for data rates up to 116kb/s and operates with space-saving 0.1μF capacitors. It saves up to 67mW of power by reducing supply current from 13.5mA during normal operation to only 10μA in shutdown mode.

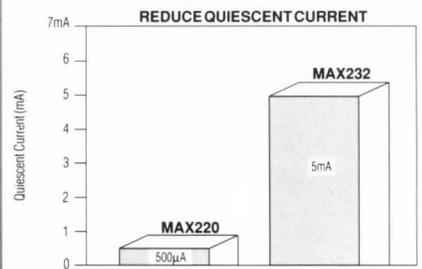
(CIRCLE 241)

### Power-Saving RS-232 Dual Transceiver Stays Active in Shutdown Mode



The **MAX242** dual transceiver is guaranteed for data rates up to 116kb/s and saves space with 0.1μF external capacitors. It features a shutdown mode that saves up to 67mW of power. And, the MAX242 receivers remain active in the shutdown mode. Separate three-state output controls allow bused configurations. (CIRCLE 242)

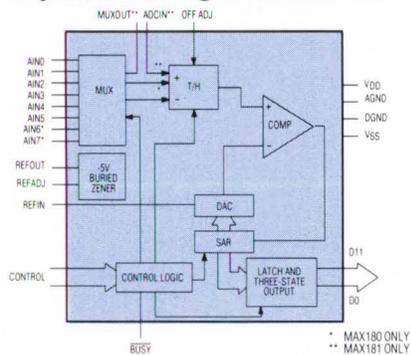
### RS-232 Transceivers at 1/10th the Power!



The **MAX220** dual +5V transceiver is designed specifically for low-power operation. Quiescent operating supply current is a mere 500μA unloaded. And, the MAX220 is guaranteed to operate at data rates up to 20kb/s.

(CIRCLE 243)

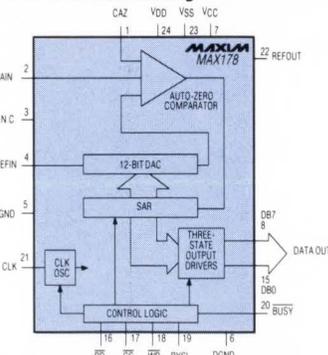
### Self-Contained 8-Ch 12-Bit System Simplifies "Analog In-to-Data Out"



The **MAX180/181** have a programmable mux 7.5μs conversion times, 6MHz full-power bandwidth track/holds, and a 25ppm/C low voltage reference.

(CIRCLE 244)

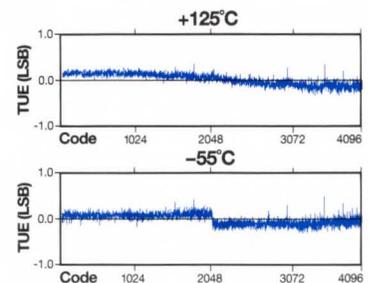
### Calibrated 12-Bit ADC with T/H Has ±1LSB Accuracy



The **MAX178** 60μs ADC is calibrated for ±1LSB total unadjusted error, providing true 12-bit performance over the full military temperature range.

(CIRCLE 245)

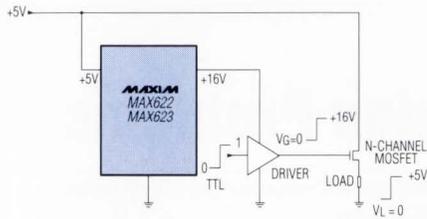
### 4-Channel ADC with T/H Maintains ±1LSB Accuracy



With no gain, offset, or linearity adjustments, the total error for a **MAX182** stays below ±1LSB from -55°C to +125°C for all codes. Pin-compatible upgrade for AD7582.

(CIRCLE 246)

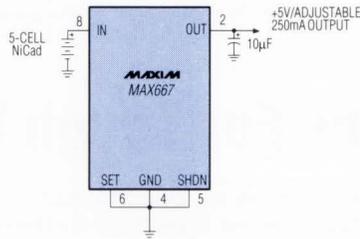
**Regulated Charge Pumps Generate High-Side Voltages and Eliminate Expensive FETs**



The MAX622/623 high-side, charge-pump converters provide the supply voltage required to drive low-cost, N-Channel MOSFET switches in high-current applications.

(CIRCLE 247)

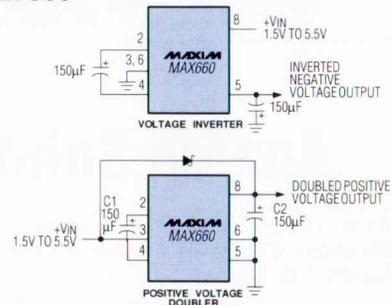
**5V Linear Voltage Regulator Has 150mV Dropout at 200mA**



The MAX667 is the only CMOS linear voltage regulator that has both low dropout and ultra-low, 20µA, no-load quiescent current. Ideal for battery-powered applications.

(CIRCLE 248)

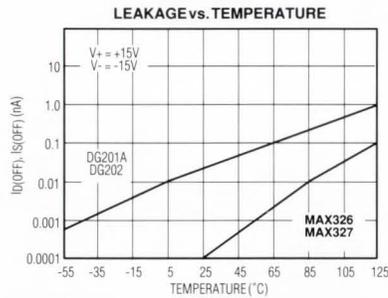
**100mA-Output, Monolithic Voltage Converter Upgrades ICL7660**



The MAX660 charge-pump voltage inverter converts a +1.5V to +5.5V input to a -1.5V to -5.5V output. It is a pin-compatible, high-current ICL7660 upgrade. 100mA is supplied with only a 0.65V voltage drop. Efficiency exceeds 90% for most applications.

(CIRCLE 249)

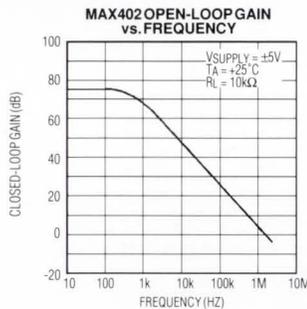
**Switches Reduce Leakage Currents to 10pA max**



The MAX326/327 quad, SPST, CMOS analog switches have low 10pA max leakage and operate from single or dual supplies. Upgrade to DG201A/202 and DG211/212.

(CIRCLE 250)

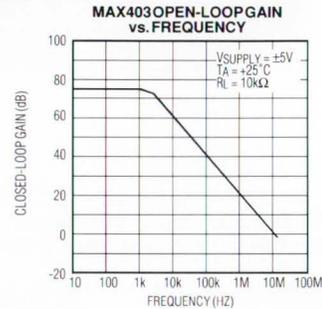
**2MHz Micropower Op Amp — 7V/µs Slew Rate from <75µA**



No other op amp matches the new MAX402's combination of high speed and micropower operation. It has a 2MHz unity-gain bandwidth and draws only 75µA max supply current.

(CIRCLE 251)

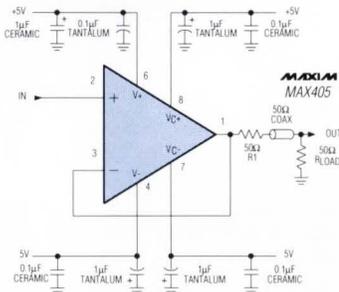
**10MHz Micropower Op Amp Slews at 40V/µs — From Less Than 375µA Supply Current**



The MAX403 is unity gain stable and uses 1/10th the supply current of an OP37. Ideal for low-power signal processing and remote sensors.

(CIRCLE 252)

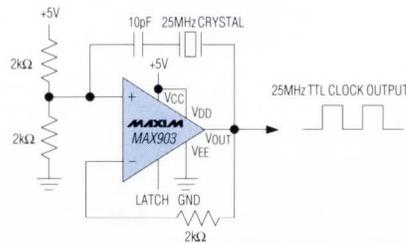
**Precision Video Buffer Amplifier Guarantees 0.99V/V Gain Over Temp**



The MAX405 combines 180MHz bandwidth, 650V/µs slew rate, and 0.01° diff phase and 0.03% diff gain from ±5V supplies. Available in small 8-pin DIP or SO packages.

(CIRCLE 253)

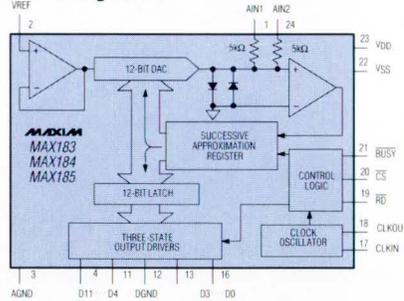
**8ns, 18mW Comparators Operate from Single +5V Supply**



The MAX900 series of single/dual/quad comparators offer 8ns response time and draw only 3.6mA per comparator from a +5V supply. Unlike other high-speed comparators, the common mode voltage range extends below ground for single +5V applications.

(CIRCLE 254)

**World's Lowest Cost 12-Bit, 3µs ADC — Only \$15\***



The MAX183/184/185 BiCMOS, high-speed, 12-bit ADCs have low code-edge noise and low 90mW power consumption. These devices, with wide input range (+15V, +10V or ±5V) and versatile power-supply operation (+5V and -12V to -15V), are ideal for PC data-acquisition cards.

\*FOB USA 1000pc (CIRCLE 255)

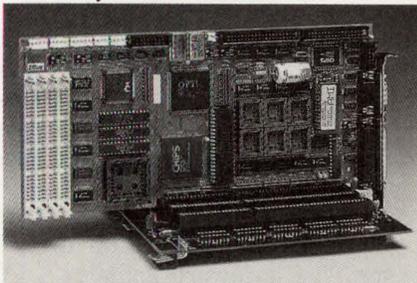
★ DATA SHEETS ★

MAX232A (CIRCLE 238)	MAX178 (CIRCLE 245)	MAX403 (CIRCLE 252)
MAX233A (CIRCLE 239)	MAX182 (CIRCLE 246)	MAX405 (CIRCLE 253)
MAX243 (CIRCLE 240)	MAX622/623 (CIRCLE 247)	MAX900/1/2/3 (CIRCLE 254)
MAX222 (CIRCLE 241)	MAX667 (CIRCLE 248)	MAX183/ (CIRCLE 255)
MAX242 (CIRCLE 242)	MAX660 (CIRCLE 249)	MAX184/185
MAX220 (CIRCLE 243)	MAX326/327 (CIRCLE 250)	
MAX180/181 (CIRCLE 244)	MAX402 (CIRCLE 251)	

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▼ **SBC OFFERS SMALL SIZE, LOW POWER**

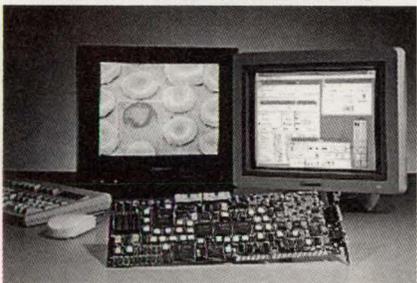


The I386SX single-board computer (SBC) features a watchdog timer, advanced power-fail detect circuitry, and support for 1.5 Mbytes of flash memory. The compact board (10 by 4.75 in.) operates with less than 6.5 W of power while running at 20 or 25 MHz. Because of its small size and low power draw, the I386SX is suitable for battery-operated equipment, factory-floor automation, and embedded controllers. The board comes standard with an IDE-floppy disk controller, two serial ports, one parallel port, and a socket for an 80387SX math coprocessor. It supports up to 16 Mbytes of page-mode interleaved SIMM DRAM.

**I-Bus Inc.**  
9596 Chesapeake Dr.  
San Diego, CA 92123;  
(619) 569-0646

► **CIRCLE 541**

▼ **FRAME GRABBER WORKS UNDER POOR CONDITIONS**



Better effective resolution can be applied to signal data that's taken in under low light or low contrast conditions with the DT2867-LC precision frame grabber. These conditions are more prevalent in microscopy and astronomy work. The device contains a continuously adjustable analog-to-digital offset and reference, and a separate programmable gain amplifier. These functions fine-tune the board's input range to allow over 16,000 selectable ranges. Consequently, the board makes it possible

to select gains from less than 0.5 to greater than 16, enabling input ranges of 0 to 0.060 V, to 0 to 1.920 V.

Images from video cameras, VCRs, or still-video devices are captured in real time (1/30 second) with full 640-by-480-pixel spatial resolution and 256 gray scales. For jitter-free image capture, a phase-locked-loop circuit compensates for sync aberrations common to VCRs. To synchronize image capture with an external event, the DT2867-LC frame grabs can be initialized with an external trigger. The frame grabber is available now for \$2495.

**Data Translation Inc.**  
100 Locke Dr.  
Marlboro, MA 01752;  
(508) 481-3700

► **CIRCLE 542**

▼ **GRAPHICS ACCELERATOR PUSHES SUPER VGA**

Operating at an average speed that's ten times faster than standard super VGA cards in the Windows environment, the Fahrenheit 1280° accelerator offers flicker-free graphics. The board supports most popular resolutions and is fully backward compatible with previous graphics standards. It comes with drivers for Windows 3.X and AutoCAD. Two configurations are available: 512 kbytes and 1 Mbyte. The board sells for \$449 (512 kbytes) and \$549 (1 Mbyte).

**Orchid Technology**  
45365 Northport Loop West  
Fremont, CA 94538;  
(415) 683-0300

► **CIRCLE 543**

▼ **CONTROLLER EASES EISA BOARD DESIGNS**

When designing add-in boards for EISA bus systems, consider the HD64981F ESIC (EISA slave interface controller) as a flexible, cost-effective building block. The controller can transfer data at 33 Mbytes/s. Built-in control registers permit programming of the on-board peripheral functions. Using these registers, the chip decodes the addresses of two memory and four I/O areas. Each memory and I/O area includes a wait-state generator. Applications for the ESIC range from simple EISA add-in boards, such as serial or parallel ports, data-acquisition, and IEEE-488 instrumentation control-

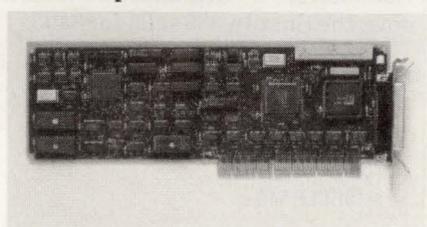
lers, to complex board like graphics controllers, network interfaces, and disk controllers. The HD64981F is housed in a 100-pin quad flat pack. Available now, it sells for \$16 in 1000-unit quantities. An evaluation board is also available.

**Hitachi America Ltd.**  
2000 Sierra Point Pkwy.  
Brisbane, CA 94005;  
(415) 589-8300

► **CIRCLE 544**

▼ **EISA SYSTEMS BENEFIT FROM SCSI ADAPTER**

Fast SCSI II support comes to 32-bit EISA systems using the RF5600 SCSI adapter from Ciprico Inc. When connected to fast SCSI II drives, the adapter can transfer data at rates up to 10 Mbits/s. The board's



architecture features separate data paths for simultaneous transfer of SCSI data and commands into an on-board queue. The command queue and the adapter's microprocessor work together to reduce SCSI command overhead. By sorting and combining commands, the RF5600 further minimizes overhead by reducing disk seek times for multisector transfers.

The adapter comes with Soft-Cache, a powerful caching utility that uses system memory to cache disk data. Files that are frequently read get stored in cache, eliminating disk accesses on subsequent requests for the same file.

Up to eight RF5600s can be installed in each EISA system, and each adapter can control up to seven SCSI devices, for a total of 56 SCSI devices per system. Most operating systems are supported, including NetWare 3.11 and SCO Unix and Xenix. DOS is supported by the on-board BIOS EPROM. The RF5600 is available now for \$795.

**Ciprico Inc.**  
2955 Xenium Lane  
Plymouth, MN 55441;  
(612) 559-2034

► **CIRCLE 545**

## PC DESIGN PRODUCTS

### ▼ PROCESSOR UPGRADE CONVERTS 286 TO 386

The capabilities of an 80286-based PS/2 can be upgraded using the SnapIn 386 upgrade module. The compact module boosts system performance up to that of an 80386SX-based system. The device plugs directly into the socket of an IBM PS/2 Model 50 or 60. The upgrade PC has the ability to run 32-bit applications that take advantage of the 80386SX. Upgrading with the SnapIn 386 permits users to run Windows 3.0 in 386 enhanced mode. The module will connect with an Intel 287XL math coprocessor, which is equivalent to the 80387SX coprocessor. It comes with 16 kbytes of cache memory, as well as a DOS device driver. An OS/2 device driver is available. Available now, the SnapIn 386 sells for \$495.

**Intel Corp.**

5200 N.E. Elam Young Pkwy.

Hillsboro, OR 97124;

(800) 538-3373 or

(503) 629-7354

► CIRCLE 546

### ▼ CONNECT OPTICAL DRIVE TO PC

Connectivity problems between operating systems and rewritable optical drives are solved by the OCU-125S intelligent hardware interface. Common integration obstacles include variations in block size or the lack of removable media support. By using the OCU-125S, all 5-1/4-in. rewritable optical drives can attach easily to most PCs that have SCSI support. Operating system support includes DOS, Netware, OS/2, Ultrix, Unix, and VMS. Specific software drivers aren't needed if the hardware interface is used. Optical subsystems run with standard operating-system commands. Features of the OCU-125S include 256-kbyte cache RAM and a battery-backed cache. The interface sells for \$895.

**Ten X Technology Inc.**

4807 Spicewood Springs Rd.

Bldg. 3, Suite 3200

Austin, TX 78759;

(512) 346-8360

► CIRCLE 547

### ▼ KIT BRIDGES GAP FROM PCs TO SPARCSTATIONS

A workstation's power and functionality can be carried over to a PC using the Sparcard Kit, which contains all of the components needed to upgrade a standard PC to full SparcStation functionality. The kit comes with the hardware, software, cables, and step-by-step documentation to ensure easy migration for any PC user. The hardware includes a PC add-in card with a 25-MHz RISC processor, 8 Mbytes of DRAM, a color frame buffer, two SCSI connectors, one SBus slot, and on-board Ethernet support. The software includes a DOS interface and Opus' port of SunOS 4.1.1, which enables PC users to run both MS-DOS and SunOS. The diskless configuration sells for \$4495. A 213-Mbyte hard drive can be added for \$1135.

**Opus Systems Inc.**

329 North Bernardo

Mountain View, CA 94043;

(415) 960-4040

► CIRCLE 548

# How well does Texas Instruments support



▼ **EL DISPLAY ACTS AS TOUCH SCREEN**



Functioning as either a standard EGA terminal or as a touch screen, the ViewBox electroluminescent (EL) display is enclosed in a rugged, splash-proof cast-aluminum housing. The EL display has a resolution of 640 by 350 pixels with a highly visible bright-orange screen. The optional touch screen, which contains 1024 by 1024 points, uses a capacitive method to detect operator touches. The touch screen comes with calibration and mouse-driver software. The ViewBox sells for \$1995; the touch-

screen option costs \$700.

**Pro-Log Corp.**  
2555 Garden Rd.  
Monterey, CA 93940;  
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▼ **17-IN. COLOR MONITOR FEATURES DMS**

The 5017/FST 17-in. color monitor features autoscanning, a full square tube, and digital memory sizing (DMS). It adapts automatically to any horizontal frequency between 30 and 64 kHz. DMS ensures a consistently high-quality output of constantly used signals. Using the touch-sensitive controls, users can optimize the image for any incoming signal and store the setting in the monitor's memory. DMS then recognizes the signal and adjusts the image automatically, according to the users' preset instructions. The full square tube reduces glare from reflections and minimizes distortion.

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1943 Providence Ct.

College Park, GA 30337;  
(404) 991-2246  
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▼ **FREE SCANNER TOOLKITS AVAILABLE**

To support a family of SCSI scanners, Ricoh Corp. is offering IBM PC and Apple Macintosh toolkits with complete driver support. The toolkit supports MS-DOS, Windows 3.0, and all Macintosh systems, including System 7. With the kit, designers can connect multiple scanners to the same SCSI bus. Users previously had to re-cable the scanner each time they wanted to access more than one scanner for a specific application. The free kit comes with scanner drivers, a sample application with source code, a programmer's guide and reference, and specifications for all Ricoh scanners.

**Ricoh Corp.**  
5 Dedrick Pl.  
West Caldwell, NJ 07006;  
(201) 882-2000  
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CIRCLE 152 FOR U.S. RESPONSE

CIRCLE 153 FOR RESPONSE OUTSIDE THE U.S.

# Less Equals More: Latest Chip Sets Offer More Functionality With Fewer Chips

BY DAVE BURSKY

In an effort to cost-reduce the personal computer and RISC-based workstations, several suppliers have developed multiple generations of off-the-shelf chip sets. The PC's open architecture has been both a blessing and a curse for system designers and chip-set manufacturers. The standard functions that should be included in the base motherboard make it easy to define the chip set needed to minimize board area and system cost. However, that same "fixed" architecture (and the millions of lines of software based on it) places some restrictions on the innovative freedom designers have when maximizing performance or adding new features.

Though bound by those architectural restrictions, designers have found ways to innovate in the areas of caching, local bus interfaces, power management, and user-programmable features. Today, a seemingly unlimited variety of chip sets for the XT, AT, EISA, and even Micro Channel Architecture (MCA) buses are available (*see the table*). But what constitutes a chip set? Today's base computer, which most users consider acceptable, is yesterday's dream machine. No longer is a hard-disk drive an option. Color VGA displays have become the de facto standard for viewing. And most programs require a trackball or mouse (thus requiring a serial port or bus interface). A number of early chip sets, however, didn't include such functions as the keyboard interface, floppy-disk controller, video controller, serial or parallel I/O ports, and hard-disk controller. That's because those were functions IBM Corp. relegated to the add-in card for the XT or AT bus.

Thus, even though manufacturers talk about one-, two-, or three-chip sets to implement a motherboard, system designers must still add at least two more logic chips to supply the disk control, video, and serial and parallel I/O. These supporting chips aren't counted by most companies as part of the base chip set. But perhaps they should be, so that designers get a better picture of what's needed. Chip manufacturers have, of course, plied their integration skills on those chips as well. "Combo" chips, now available from several suppliers, contain serial and parallel ports, a floppy-disk controller, real-time clock, and an integrated-drive-electronics (IDE) interface.

The IDE drive interface is much simpler than the original ST-506 type used on the earlier add-in drive-controller cards. In IDE systems, the controller is integrated into the disk drive, requiring just a simple bus-interface card with some decoders and buffers. Because the controller is embedded in the drive, the motherboard-resident logic needed

to control the drive becomes trivial.

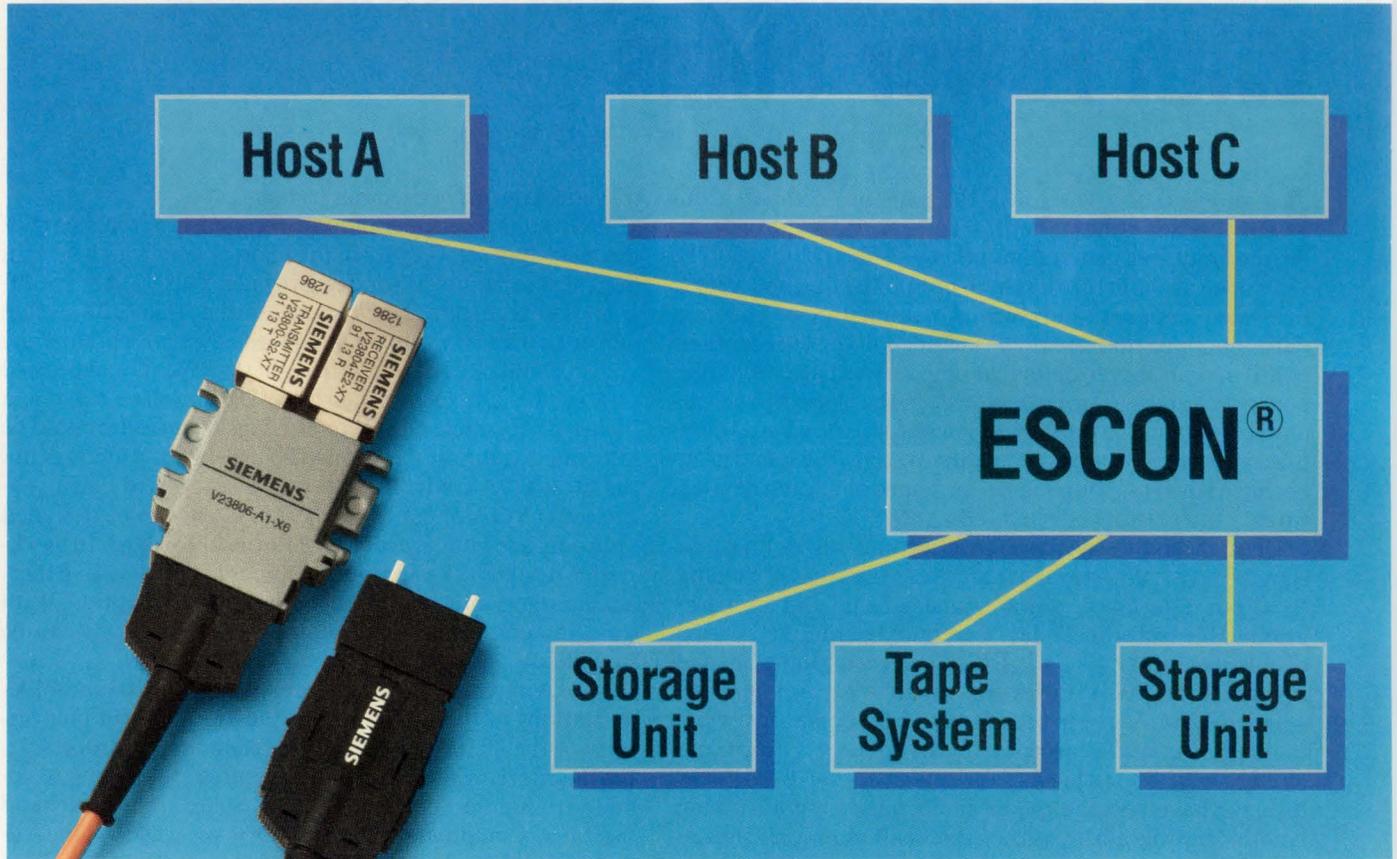
Because the peripheral control functions aren't part of the main chip set, they form the main area in which system designers can innovate or design systems targeted at specific market segments. For instance, rather than just adding one or two serial ports on a high-end system, perhaps the system could be designed with eight serial ports and be used as a server. Or, rather than the IDE interface, maybe a higher-performance ESDI or SCSI disk controller could be integrated right on the motherboard. In the video realm, the latest VGA controllers are so well integrated that an entire color-VGA or super-VGA subsystem can be designed onto only a few square inches of the motherboard. In workstation designs, a basic video-graphics capability, an Ethernet interface, and a SCSI port are standard features. With some integration, the inclusion of those functions can be simplified.

Most companies at least offer chip sets for AT-bus implementations of the 16-bit 80286, the 16- or 32-bit bus versions of the 80386, and the 32-bit 80486 microprocessors. Furthermore, workstation architectures are starting to solidify around the Sun Microsystems Sparc architecture and the Mips Computer Systems R3000 processor. The Advanced Products Division of Fujitsu Microelectronics Inc., San Jose, Calif., and Tera Microsystems are among several companies that have created chip sets for Sparc-architecture processors, while LSI Logic and Bull-Mical, Minneapolis, Minn., have developed chip sets for use with the Mips architecture.

Concerning the 80286 and the 80386SX, a number of companies have compressed the logic down to one VLSI chip and between 6 and 10 simple MSI-level parts. With the 80386DX and the 80486, most systems use two to four VLSI chips for the basic motherboard, though single-chip solutions are emerging. EISA and MCA chip-set implementations are a little more complicated—the latest chip sets can put the logic onto three to eight large chips. The EISA-bus chip sets aren't that widely available. The four best known suppliers of these sets include Intel, OPTi, Symphony Labs, and Texas Instruments. Chip sets for the IBM MCA are even scarcer—just Chips and Technologies, Intel, and Toshiba have offerings.

One distinction drawn between chip sets is type of cache control, if any, that they implement. Some chip sets rely on yet another support chip, such as Intel's cache controller or a competing equivalent from other sources. Different sets, like those from Elite, Mosel, Symphony, and others, inte-

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CIRCLE 204 FOR U.S. RESPONSE

CIRCLE 205 FOR RESPONSE OUTSIDE THE U.S.

## ■ PC CHIP SETS ■

grate the cache controller as part of one of the chips in the chip set. Cache implementations can be write-through or write-back, and proponents for each approach claim that its architecture is better in cost or performance. But the application actually makes that determination.

Another direction some chip-set vendors have taken is to create a secondary bus that isolates the CPU, cache, and floating-point unit from the rest of the system. By separating the CPU subsystem from the main system memory and all of the system logic, the CPU core block can be upgraded without disturbing the rest of the system. Consequently, cost is reduced while performance is upgraded. Toshiba adopted that approach when designing its MCA chip set. Similarly, Tera Microsystems created a processor bus for the Sparc-based CPU block.

Many companies used a similar approach in PCs as far back as the S-100 bus computers. At that time, the level of integration dictated the need for modularity, with the CPU on one card, I/O on another card, RAM on a third, and so on. Most recently, Compaq Corp., Houston, Texas, unveiled a modular PC family that allows any of five main system sections to be upgraded by simply replacing one of the modules with a newer version.

In addition to using a processor bus to "disconnect" the CPU clock from the system clock, some new recent new

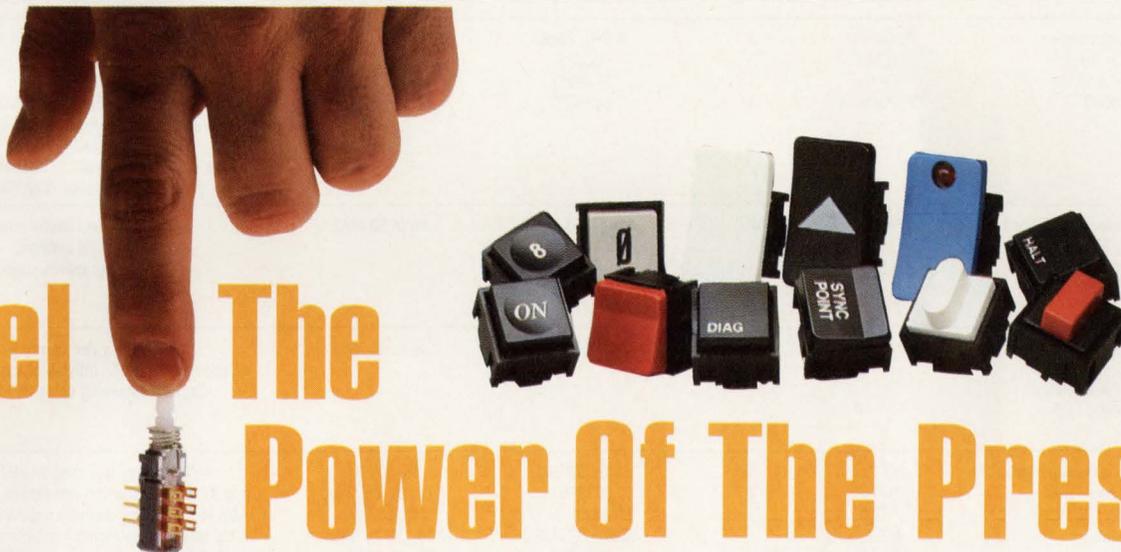
chip-set offerings allow the video subsystem to tie directly into the 20-to-40-MHz processor bus rather than the slow, 8-MHz AT-bus. With this local-bus interface, the video subsystem can accelerate many data-transfer operations. As a result, new data can be put on the screen more rapidly. Furthermore, because the video data no longer goes over the AT bus, the bus is freed up for other activities.

Notable trends in the area of portable systems include chip sets that have power-management capacity and the ability to operate at low voltages. Almost every chip set for battery-powered systems includes some control logic that will work with the BIOS. This permits unused sections of the system to power down after various preset periods, thus saving battery power. Multiple clock-speed settings are also a means to conserve power—several chip sets automatically scale down the clock by ratios of 4 to 10. Because the systems are CMOS, any reduction in clock frequency linearly translates into a reduction in power consumption.

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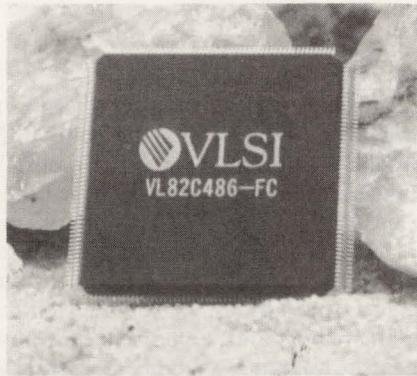
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## PC CHIP SETS PRODUCTS

### ▼ SINGLE-CHIP CONTROLLER REPLACES NINE PARTS

Designed for 486SX- and 486DX-based systems, the VL82C486 is a 1- $\mu$ m CMOS single-chip chip set that can operate at speeds ranging up to 33 MHz. The 208-lead device replaces nine components on a typical PC motherboard. The parts include two DMA controllers, a programmable interval timer, a clock generator and ready interface, two interrupt controllers, a memory mapper, and a bus controller. The VL82C486 also incorporates a memory-refresh controller and bus steering, as well as parity checking, burst-mode control, and



parity-checking logic.

By including the memory-control logic on the device, the VL82C486 supplies direct support for up to 64

Mbytes of system DRAM. This lets the controller drive up to four banks of 256-kbyte, or 1- or 4-Mbyte DRAMs without any external buffering.

Samples of the VL82C486 controller will be available in the fourth quarter, with volume production expected to commence in the first quarter of 1992. Single units will sell for about \$75; volume quantities will go for about \$46.

**VLSI Technology Inc.**  
8375 South River Pkwy.  
Tempe, AZ 85284;  
(602) 752-8574

► **CIRCLE 470**

### A SAMPLING OF CHIP SETS

Manufacturer	Model	Number of chips in set	Processors supported	Speeds supported	Additional features
ACC Microelectronics Corp. 3295 Scott Blvd. Santa Clara, CA 95054 (408) 980-0622 <b>Circle 481</b>	2046 82021 2036 82300	1 4 1 3	80386DX, 80486SX/DX 80286, 80386SX 80286, 80386SX 80386SX	up to 50 MHz 16, 20, 25 MHz 12, 16, 20, 25 MHz 20, 25 MHz	Supports double-phase clock 386 systems to 40 MHz (2046). Supports 512 kbytes of cache memory (2046). Supports up to 64 Mbytes of memory (2046).
Appian Technology Inc. 477 N. Mathilda Ave. Sunnyvale, CA 94086 (408) 730-5400 <b>Circle 482</b>	A90	1	80386SX	16, 20 MHz	Aimed at notebook PCs. Power-management controller. Expansion--bus buffer. Intelligent look-ahead memory coprocessor.
Chips & Technologies 3050 Zanker Rd. San Jose, CA 95134 (408) 434-0600 <b>Circle 483</b>	PEAK/DM M/PAX SCATsx CHIPSliteSX	3 5 1 4	80386, 80486 80486 80386SX 80386SX	20, 25, 33, 40 MHz 25, 33, 50 MHz 16, 20, 25 MHz 16, 20, 25 MHz	Integrated cache support (PEAK/DM). Supports up to six 80486 50-MHz processors (M/PAX). 128-bit wide bus (M/PAX). Aimed at notebook and desktop PCs (SCATsx, CHIPS-liteSX). Includes power-control unit, LCD controller, and universal I/O controller (CHIPSliteSX).
Elite Microelectronics Inc. 4003 North First St. San Jose, CA 95131 (408) 943-0500 <b>Circle 484</b>	Falcon	2	80486SX/DX	up to 50 MHz	Secondary-level cache support. 486 burst support. Local-bus graphics support.
Fujitsu Microelectronics Inc. 50 Rio Robles, Bldg. 3 San Jose, CA 95134 (408) 922-9722 <b>Circle 485</b>	Sparc chipset	5	Sparc	up to 40 MHz	Built-in video controller. Supports up to 512 Mbytes of main memory. Cache addressing up to 256 kbytes.
Headland Technology Inc. 46221 Landing Pkwy. Fremont, CA 94538 (510) 623-7857 <b>Circle 486</b>	HT15 HT18 HT21 HT22 HTK320	1 1 1 1 2	80386SX/SXL 80386SX 80286, 80386SX 80286, 80386SX 80386DX	16, 20 MHz 16, 20, 25 MHz 16, 20 MHz 16, 20, 25 MHz 25, 33, 40 MHz	CPU local bus support (HT15). Up to 16 Mbytes memory supported (HT15, HT22). Up to 20 Mbytes memory supported (HT18). Up to 8 Mbytes memory supported (HT21). Internal cache controller (HTK320).
Intel Corp. 1900 Prairie City Rd. Folsom, CA 95630 (916) 351-2747 <b>Circle 487</b>	82350DT 82311	7 7	80386DX, 80486SX/DX 80386SX/DX	20, 25, 33 MHz 16, 20, 25, 33 MHz	EISA compatible (82350DT). Tuned to maximize Intel's cache controller (82350DT). Micro Channel compatible (82311). Supports up to 16 Mbytes of page-interleaved DRAM (82311).
LSI Logic Corp. 1551 McCarthy Blvd. Milpitas, CA 95035 (408) 433-8000 <b>Circle 488</b>	MipSET	8	R3000	25 MHz	Complies with ARC specifications. Runs both ACE-specified operating systems.
Mosel Corp. 914 W. Maude Ave. Sunnyvale, CA 94086 (408) 733-4556 <b>Circle 489</b>	MS400	1	80386DX, 80486SX/DX	20, 25, 33, 40, 50 MHz	Supports 64 Mbytes of main memory. Supports 64-bit data path to DRAM.

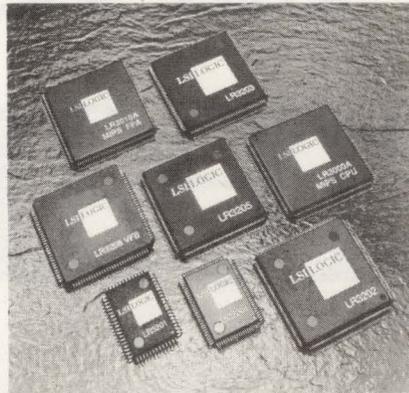
**▼ MIPS CHIP SET SUPPORTS ARC SPECS**

System designers can now build high-performance, low-cost computers that are fully compliant with the Advanced Computing Environment's (ACE) Advanced RISC Computing (ARC) specification Rev. 1.0. The MipSET, a chip set from LSI Logic Corp. that was upgraded to become fully compliant, runs at 25 MHz and is based on the LR3000A CPU and the LR3010A floating-point accelerator (FPA). This upgrade reduced the number of chips in the set from eight to six.

Systems built with the MipSET use two buses for internal communication. The C-bus is for communications between the CPU and the cache

memory, while the L-bus is for communications between the CPU, main memory, and I/O devices.

A new member was added to the previous version of the chip set: The



LR3208 video-frame controller drives a 1024 by 768 by 8 terminal consistent with the ARC specification.

The chip set can be used with either ARC-compatible designs or more traditional Unix systems, such as those supporting AT&T's Unix System V, Rev. 4.0. The chip set's other components include a reset-interrupt controller, a bus controller, a DRAM controller, a DRAM data buffer, and a block-transfer buffer. The MipSET is priced at \$495 in 10,000-piece quantities.

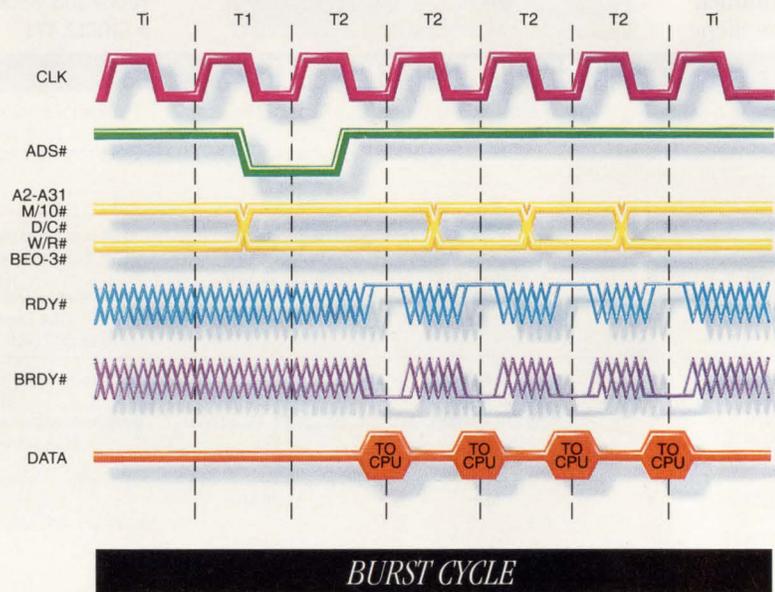
**LSI Logic Corp.**  
1551 McCarthy Blvd.  
Milpitas, CA 95035;  
(408) 433-8000

► **CIRCLE 471**

**A SAMPLING OF CHIP SETS**

Oak Technology Inc. 139 Kifer Ct. Sunnyvale, CA 94086 (408) 737-0888 <b>Circle 490</b>	OakNote	3	80286, 80386SX	up to 25 MHz	Power management is OS independent. Local-bus video support. Requires only one external TTL for complete motherboard.
OPTi Inc. 2525 Walsh Ave. Santa Clara, CA 95051 (408) 980-8178 <b>Circle 491</b>	SXPI	2	80386SX	16, 20, 25 MHz	Built-in power-management features (DXNB). On-chip comparator for hit-miss detection (486SXWB). Built-in local bus support (DXPI). EISA compatible (EISAWB). Integrated cache comparator (EISAWB).
	DXNB	2	80386DXL, 80486SX	20, 25, 33 MHz	
	486SXWB	3	80486SX/DX	20, 25, 33 MHz	
	DXPI	2	80386DX, 80486SX/DX	20, 25, 33, 40 MHz	
Symphony Laboratories 2620 Augustine Dr., Suite 250 Santa Clara, CA 95054 (408) 986-1701 <b>Circle 492</b>	EISAWB	4	80386DX, 80486SX/DX	20, 25, 33, 40, 50 MHz	
	SL82C360	2 or 3	80386SX/DX	16, 20, 25, 33, 40, 50 MHz	Supports up to 1 Mbyte of cache memory (SL82C360, SL82C470). Built-in cache-posted write buffers (SL82C460). EISA compatible (SL82C470).
	SL82C460	2 or 3	80486DX	25, 33, 40, 50 MHz	
SL82C470	3	80386DX, 80486SX/DX	16, 20, 25, 33, 40, 50 MHz		
Tera Microsystems 5200 Great American Pkwy., #250 Santa Clara, CA 95054 (408) 987-5600 <b>Circle 493</b>	microCORE	4	Sparc	25, 33, 40 MHz	1.0- $\mu$ m CMOS technology. Interfaces with AMD's Lance Ethernet controller.
Texas Instruments 8330 LBJ Freeway 75243 Dallas, TX 75265 (214) 997-5470 <b>Circle 494</b>	TACT82S411	1	80286, 80386SX	12, 16, 20 MHz	EMS 4.0. NEAT compatible (82S411). Highly software programmable (83000). Supports 16-Mbit DRAMs (845000). EISA compatible (84500).
	TACT83000	3 (SX) or 4 (DX)	80386SX/DX, 80486SX/DX	20, 25, 33, 50 MHz	
	TACT84500	4	80386SX/DX, 80486SX/DX	20, 25, 33, 50 MHz	
Toshiba America Inc. 9775 Toledo Way Irvine, CA 92718 (714) 455-2000 <b>Circle 495</b>	MCA chipset	4	80486DX	25, 33 MHz	Micro Channel compatible. Eight DMA channels. Supports secondary-level cache. Supports up to 16 Mbytes of memory.
Via Technologies Inc. 860 East Arques Ave. Sunnyvale, CA 94086 (408) 746-2200 <b>Circle 496</b>	Flex II	2	80386SX/DX	16, 20, 25, 33 MHz	Configurable through programmable registers.
VLSI Technology Inc. 8375 S. River Pkwy. Tempe, AZ 85284 (602) 752-8574 <b>Circle 497</b>	VL82C286	2	80286, 80386SX	up to 25 MHz	Shadow RAM support. Built-in sleep features (VL82C286, VL82C386). Support for up to 64 Mbytes of DRAM (VL82C486).
	VL82C386	3	80386DX	up to 33 MHz	
	VL82C310/311	1	80286, 80386SX	up to 25 MHz	
	VL82C486	1	80486SX/DX	up to 33 MHz	
Western Digital 8105 Irvine Center Dr. Irvine, CA 92718 (714) 932-6250 <b>Circle 498</b>	WD7700	3	80386SX	up to 25 MHz	Real-time clock with CMOS RAM. Internal cache control (WD7700, WD7700LP, WD7900, WD7900LV). Advanced power management (WD8600LP).
	WD7700LP	3	80386SX	up to 25 MHz	
	WD7900	3	80386SX	up to 25 MHz	
	WD7900LV	3	80386SX	up to 25 MHz	
	WD8600	3	80386DX, 80486SX/DX	25, 50 MHz	
	WD8600LP	3	80386DX, 80486SX/DX	25, 50 MHz	

# Go ahead. Scream.



It's time to take the brakes off your 486 machine and let it fly to its full potential.

How? With a BurstRAM™ from Motorola.

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with the microprocessor and the cache controller without extra logic.

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## PC CHIP SETS PRODUCTS

### ▼ CONTROLLER SUPPORTS MULTIPLE 386s

Supporting both the Intel 386SX and the AMD 386SX/SXL processors, the HT15 offers a complete set of ISA core logic components packaged in one 184-pin chip. The part's high performance comes from its zero-wait-state memory-control technique and page-mode memory controller. The combination of these memory-controller options offers designers optimal flexibility. The controller can handle CPU speeds up to 25 MHz. Up to 16 Mbytes of on-board memory are supported.

**Headland Technology Inc.**

46221 Landing Pkwy.

Fremont, CA 94538;

(415) 623-7857

► CIRCLE 472

### ▼ CONTROLLER SUPPORTS PORTABLE 386, 486

Designers of laptop or notebook PCs can pack their systems with workstation-like power using the ACC-2146 single-chip AT controller. The controller supports 486DX, 486SX, and 386DX microprocessors. The 2046 integrates most of the logic and performance of a 20- to 50-MHz single-phase-clock-based 486 AT system into one 208-pin plastic quad flat pack. The chip also supports a double-phase-clock-based 386 AT system up to 40 MHz. In addition, it contains support for up to 512 kbytes of direct-mapped cache-control memory, shadow RAM for video and system BIOS, and dynamic-memory remapping. The controller can handle one to four memory banks of 32-bit DRAM, using 256-kbyte, or 1- or 4-Mbyte DRAMs on a system board that allows up to 64 Mbytes of on-board memory. The timings for DRAM parameters are programmable. In quantities of 1000, the 25-MHz part costs \$100, the 33-MHz part is \$125, and the 40-MHz part costs \$140.

**ACC Microelectronics Corp.**

3295 Scott Blvd.

Santa Clara, CA 95054;

(408) 980-0622

► CIRCLE 473

### ▼ NOTEBOOK CHIP SET CONTAINS INTEGRATED PMU

Built with an integrated power-management unit (PMU) this 32-bit notebook PC chip set enables designers

to build 386DXL and 486SX systems running at 20, 25, or 33 MHz. Each chip in the two-chip set is housed in a 208-pin quad flat pack. The integrated write-back cache controller can support up to 256 kbytes of static RAM. It maximizes performance while complementing the page-interleaved memory controller, which is capable of supporting up to 64 Mbytes of DRAM.

The PMU reduces system power consumption by supplying sleep and suspend-resume functionality. It also takes full advantage of the power-saving features found in the DXL CPU. The chip set costs \$60 in OEM quantities. Volume shipments should start in the fourth quarter.

**OPTi Inc.**

2525 Walsh Ave.

Santa Clara, CA 95051;

(408) 980-8178

► CIRCLE 474

### ▼ BUILD EISA BUS SYSTEM TO 50 MHZ

The SL82C470 chip set offers a high-performance, highly integrated, cost-effective implementation for PCs based on the 32-bit EISA bus. The chip set supports 386DX, 486SX, and 486DX processors operating at speeds from 20 to 50 MHz.

The chip set can operate in either standard or buffered configurations. In the standard configuration, the cache subsystem is dedicated to bus snooping, while a DMA or master device becomes active. In the buffered configuration, the CPU-cache operation continues as bus snooping is performed for the DMA or master device. This helps achieve maximum concurrency between the CPU and the EISA bus.

In addition to the chip set and memory devices, only ten TTL parts are required to complete a motherboard design. If a buffered configuration is being implemented, five extra parts are required. The set consists of three components: an integrated cache-DRAM controller, an EISA bus controller, and a DMA controller. Each chip is packaged in a 160-pin plastic quad flat pack.

**Symphony Laboratories**

2620 Augustine Dr., #250

Santa Clara, CA 95054;

(408) 986-1701

► CIRCLE 475

# Read between the lines.



What's new in Motorola's Fast Static lineup? This chart gives you but a glimpse. Mail in the coupon below for our complete quarterly update of new Memory products. We think you'll like our line of thinking.

#### MOTOROLA FAST STATIC RAMS

256K x 4	MCM6229	25ns
128K x 8	MCM6226	25ns
256K x 1	MCM6207	15/20/25ns
64K x 4	MCM6708**	10/12ns
	MCM6709** (OE)	10/12ns
	MCM6208	15/20/25ns
	MCM6209 (OE)	15/20/25ns
32K x 8	MCM6706**	10/12ns
	MCM6206	15/17/20/25ns*
32K x 9	MCM6205	15/17/20/25ns*
16K x 4	MCM6288	10**/12/15/20/25ns*
	MCM6290 (OE)	10**/12/15/20/25ns*
64K x 1	MCM6287	12/15/20/25ns*
8K x 8	MCM6264	12**/15/20/25ns*
8K x 9	MCM6265	12**/15/20/25ns*
4K x 4	MCM6268	20/25/35ns*
	MCM6269 (CS)	20/25/35ns
	MCM6270 (OE)	20/25/35ns

#### Synchronous Fast Static RAMs

64K x 4	MCM62982*	12/15ns
4 x 64K x 1	MCM62983*	12/15ns
64K x 4	MCM62980	15/20ns
4 x 64K x 1	MCM62981	15/20ns
32K x 9	MCM62950	20/25ns
	MCM62960	17/20ns
	MCM62110	15/20ns
16K x 16	MCM62990	12**/15**/20ns
16K x 4	MCM6294	20/25ns
	MCM6295	25/30ns
4K x 10	MCM62963	18/25ns
4K x 12	MCM62973/4	18/25ns
	MCM62975	25/30ns

#### BurstRAMs™

32K x 9	MCM62940	19/24ns
32K x 9	MCM62486	14/19ns

#### DSPRAM™

8K x 24	MCM56824	20**/25/35ns
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#### Latched Fast Static RAMs

16K x 16	MCM62995	12**/17/20ns
8K x 20	MCM62820	17**/23ns

#### Cache Tag RAM Comparators

4K x 4	MCM4180	18/20ns
4K x 4	MCM62351	20/25ns

#### Fast Static RAM Modules

256K x 32	MCM32257Z	20/25ns
256K x 8	MCM8256Z	15/20ns
64K x 32	MCM3264Z	15/20ns
2 x 32K x 36	MCM3632Z	15/20ns

\* Fabricated in BiCMOS technology

\*\* Production scheduled July 1991

◆ Registered outputs for two-stage pipeline

♣ Also available in slower speed

▲ Production scheduled 3Q91

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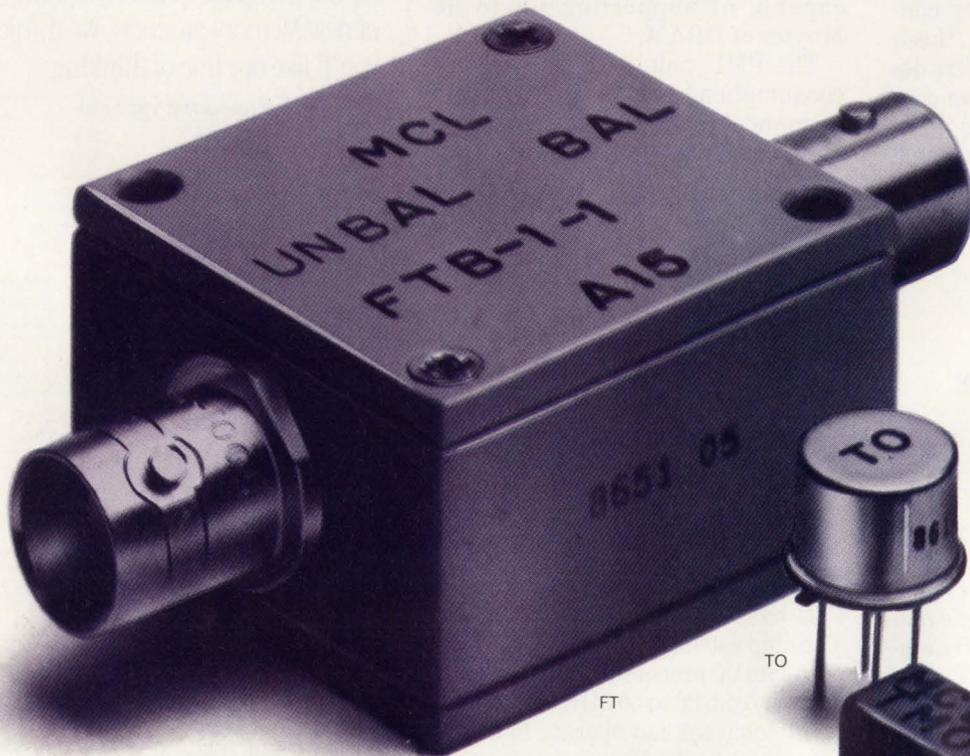
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\*units are not QPL listed

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### case styles

T, TH, case W 38, X 65 bent lead version, KK81 bent lead version  
TMO, case A 11, † case B 13 FT, FTB, case H 16  
NEW TC SURFACE MOUNT MODELS from 1MHz to 1500 MHz

### NSN GUIDE

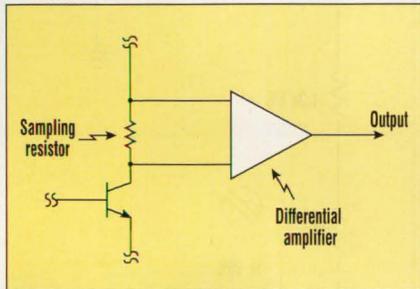
MCL NO.	NSN	MCL NO.	NSN
FTB1-1-75	5950-01-132-8034	TMO2-1	5950-01-183-6414
FTB1-6	5950-01-225-8773	TMO2.5-6	5950-01-215-4038
T1-1	5950-10-128-3745	TMO2.5-6T	5950-01-215-8697
T1-1T	5950-01-153-0668	TMO3-1T	5950-01-168-7512
T2-1	5950-01-106-1218	TMO4-1	5950-01-067-1012
T3-1T	5950-01-153-0298	TMO4-2	5950-01-091-3553
T4-1	5950-01-024-7626	TMO4-6	5950-01-132-8102
T9-1	5950-01-105-8153	TMO5-1T	5950-01-183-0779
T16-1	5950-01-094-7439	TMO9-1	5950-01-141-0174
TMO1-1	5950-01-178-2612	TMO16-1	5950-01-138-4593

**CIRCLE**  
**521 THE SMART WAY**  
**To MEASURE  $I_C$**

JOHN DUNN

181 Marion Ave., Merrick, NY 11566; (516) 378-2149.

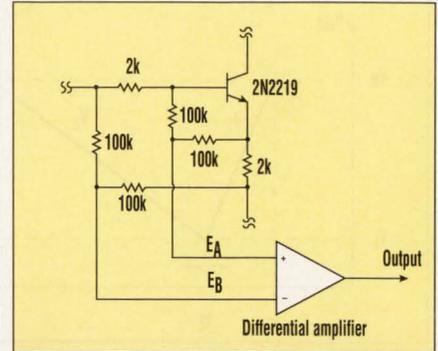
**T**he obvious way to measure a transistor's collector current,  $I_C$ , is to insert a small sampling resistor in series with the collector, and then to measure the voltage drop across that re-



**1. THE DIRECT** way to measure collector current—at the collector—can lead to common-mode problems and collector loading.

sistor (Fig. 1). Because the resistor floats above ground, the measuring instrument must have a differential input or be preceded by a differential amplifier. If the collector voltage is high, finding a differential amplifier with a suitable common-mode range may be difficult. Finding one at a feasible price may not be possible. Moreover, even if a suitable amplifier is found, its input capacitance may seriously affect the transistor's performance—limiting its bandwidth, among other things.

A better solution is to determine  $I_C$  indirectly, as the difference between the emitter and base currents. A network of resistors combines with a differential amplifier to sample those currents, and subtract one from the other (Fig. 2). Because the



**2. THE INDIRECT** way, which finds the collector current by subtraction, leaves the collector circuit completely untouched.

voltages in this configuration are much closer to ground, the common-mode requirements for the differential amplifier are easily met. Also, with no connection to the collector circuit, the amplifier's input capacitance is of much less concern.

For the component values of Fig. 2 and a unity-gain differential amplifier, the output voltage is approximately one volt per milliampere of collector current. □

**CIRCLE**  
**522 CIRCUIT TAILORS**  
**TRIANGLE WAVEFORMS**

V.V. SHKARUPIN

P.O. Box 690/4, Kiev-65, USSR, 252065.

**W**ith this triangle wave generator, the user can adjust its four key parameters independently of each other (Fig. 1). The parameters, which are maximum amplitude, minimum amplitude, frequency, and shape, completely determine the triangular waveform.

The high and low amplitudes are determined by the externally supplied voltages  $V_H$  and  $V_L$ , respectively. The frequency is determined by capacitor  $C$  and potentiometer  $R_3$ , regardless of the position of the wiper on  $R_3$ . The waveform's shape—that is, the relative durations of its positive and negative slopes—is adjusted by varying  $R_3$ .

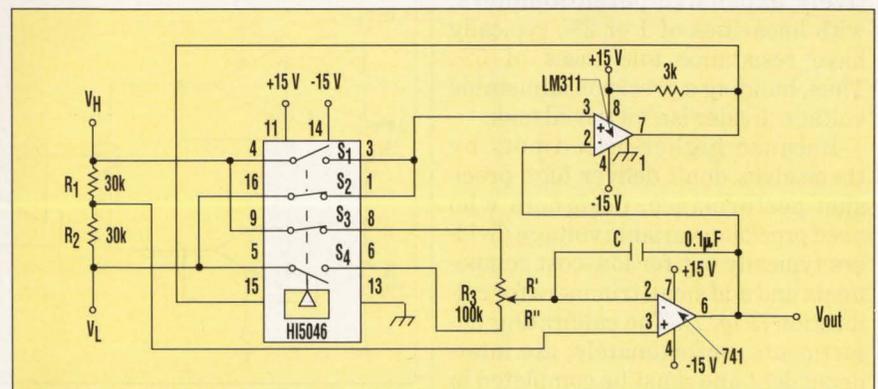
Potentiometer  $R_3$  provides two different resistance paths for the inte-

grator formed by itself, capacitor  $C$ , and the 741 op amp. The negative-going portion of the triangle wave,  $V_1$ ,

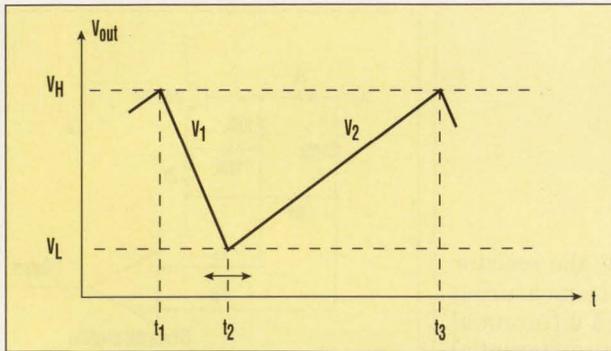
is produced when switches  $S_2$  and  $S_3$  of the HI5046 are closed (Fig. 2). It's given by:

$$V_1 = V_H - (1/\tau_1) \{ [(V_L + V_H)/2] - V_L \} t$$

where  $\tau_1$  is the time constant  $R''C$  and  $t$  is measured from  $t_1$ . When the decreasing voltage  $V_1$  reaches  $V_L$ , the LM311 comparator changes state, causing switches  $S_2$  and  $S_3$  to open, and  $S_1$  and  $S_4$  to close. That



**1. ALL IMPORTANT PARAMETERS** of a triangle wave can be adjusted independently with this simple generator circuit. The value of potentiometer  $R_3$ , with that of capacitor  $C$ , determines the generator's frequency. As  $R_3$  is adjusted,  $R'$  and  $R''$  change, varying the shape of the waveform.



marks the beginning of the positive-going portion of the waveform,  $V_2$ , which is described by:

$V_2 = V_L + (1/\tau_2)\{V_L - [(V_L + V_H)/2]\}t$   
 where  $\tau_2$  is the time constant  $R'C$  and  $t$  is measured from  $t_2$ .

The duration of waveform segment  $V_1$  is easily seen to be  $2\tau_1$ , while the duration of segment  $V_2$  is  $2\tau_2$ . Hence, the total period of the trian-

gle waveform is:

$$T = 2(\tau_1 + \tau_2) = 2(R' + R'')C = 2R_3C.$$

Thus, the frequency of the triangle wave, given by:

$$F = 1/T = 1/2R_3C,$$

depends only on  $R_3$  and  $C$ , independent of all other values. It's most conveniently changed by adjusting the value of the capacitor. □

**2. VARYING** potentiometer  $R_3$  in Figure 1 changes the shape of the triangle wave, moving the location of point  $t_2$  between points  $t_1$  and  $t_3$ , which remain stationary.

## CIRCLE 523 VOLTAGE DIVIDER NEEDS NO TRIMMING

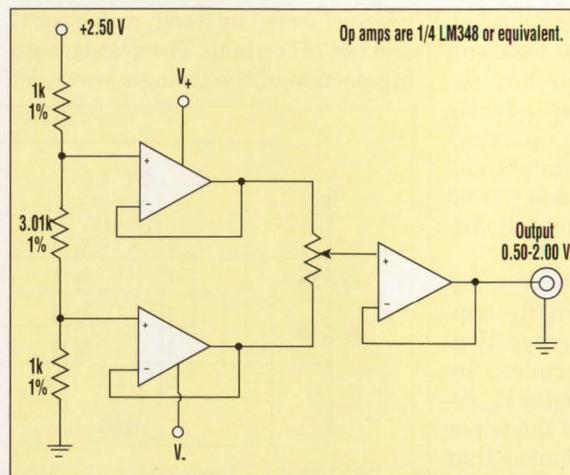
HENNO NORMET

Diversified Electronics Inc., P.O. Box 490207,  
 Leesburg, FL 34749-0207; 904-787-7259.

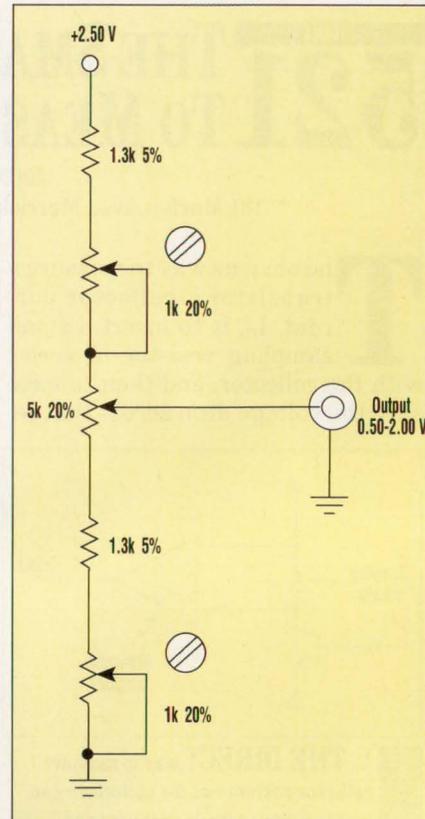
**A**lthough fixed-precision components like 1% metal-film resistors and highly accurate IC voltage references are readily available today at modest cost, the same cannot be said for variable components. Even relatively expensive potentiometers, with linearities of 1 or 2%, typically have resistance tolerances of 5%. Thus, building a precision adjustable voltage divider isn't a trivial task.

Because higher-priced pots by themselves don't deliver high-precision performance, designers who need precision variable voltage dividers typically opt for low-cost components and add small trimmers for calibration (Fig. 1). The calibrating adjustments, unfortunately, are interdependent and must be completed in a specific, time-consuming sequence. Replacing the pot, of course, requires that the complete calibration procedure be repeated.

Fortunately, there's a faster, easier way. An active divider circuit can, in fact, eliminate the need for calibration adjustments altogether (Fig.



**2. CALIBRATION IS ELIMINATED** with this active circuit, which uses op amps to fix the potentials at the pot terminals. The third op amp gets rid of errors caused by loading of the potentiometer.



**1. INTERDEPENDENT** calibrating adjustments make trimming this voltage divider a tedious business. The calibration procedure must be repeated whenever the 5k pot is replaced.

2). With the component values shown in the diagram, the circuit provides a 0.5-2.0-V output from a 2.5-V reference, regardless of the pot's tolerance. The circuit uses two unity-gain voltage followers to set the pot terminals at voltages determined by the voltage reference and the precision fixed resistors—2.001 V and 0.499 V, in this case. The third op amp supplies a low-impedance output, and eliminates loading errors.

Though this circuit removes overall pot tolerance as a source of error, it doesn't affect linearity. The linearity of the output can still be no better than that of the pot itself. □

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R4000

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CIRCLE 180 FOR U.S. RESPONSE

CIRCLE 181 FOR RESPONSE OUTSIDE THE U.S.

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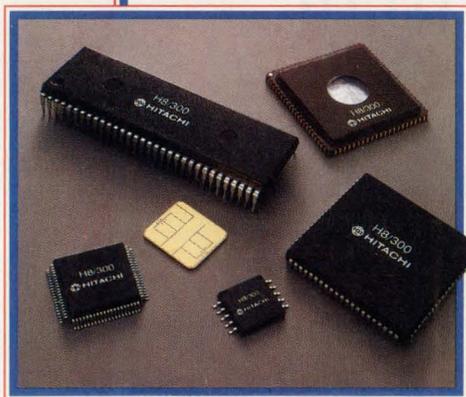
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**Circle 166 for Literature Only (U.S. Response)**

**Circle 167 Have Hitachi Representative Call (U.S. Response)**

**Circle 168 for Literature Only (Response Outside U.S.)**

**Circle 169 Have Hitachi Representative Call (Response Outside U.S.)**

Description	H8/310 Smart-Card IC	H8/322 General-Purpose Real-Time Controller	H8/323 General-Purpose Real-Time Controller	H8/324 General-Purpose Real-Time Controller	H8/325 General-Purpose Real-Time Controller	H8/330 High-End Real-Time Controller	H8/350 Servo-Positioning Controller
ROM/RAM/EEPROM	10K/256/8K	8K/256/0	16K/512/0	24K/1K/0	32K/1K/0	16K/512/0	32K/512/0
Timers			3			5	10
Serial Channel			2			1	2
A/D Converter						8-Bit, 8 Channel	8-Bit, 16 Channel
Interrupts			4 External 16 Internal			9 External 19 Internal	9 External 47 Internal
I/O Ports	1-Bit I/O Common		47 I/O 4 Input Only			58 I/O 8 Input Only	50 I/O 16 Input Only
Other Features	Security Function		Parallel Handshake Port Programmable Pull-up for All I/O			15-Byte DPRAM, Prog. Pull-up for I/O	One 19-Bit Timer, Timer Network
Package	Die Form COB* SOP-10		DP-64S QFP-64 DC-64S w/Window			PLCC-84 QFP-80 LCC-84 w/Window	PLCC-84 QFP-80 LCC-84 w/Window

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CIRCLE 178 FOR U.S. RESPONSE

CIRCLE 179 FOR RESPONSE OUTSIDE THE U.S.

# QUICK LOOK

EDITED BY SHERRIE VAN TYLE

## MARKET FACTS

**M**ore and more digital audio tape drives are being pressed into use to back up networks and desktop systems. And shipments of DAT drives should overtake 8-mm drives this year, according to Freeman Associates. The Santa Barbara, Calif., market researchers predict that this year, 169,000 DAT drives will ship. That figure is 157% more than 1990 shipments of 65,800 drives. That compares with 127,200 8-mm units, which represents an increase of 27% over 1990's shipments of 100,200 drives.

The revenue picture shapes up differently because DAT drives cost less than 8-mm ones. Revenues for DAT drives will reach only 84% of 8-mm drives this year, but are expected to top 8-mm revenues in 1992 and stay on top.

All in all, tape drives using helical scan technique—DAT, 8-mm, and VHS—should have an OEM value of \$957 million in 1996. This represents annual growth of 27% from the 1990 market, worth \$231 million. The lion's share of this market goes to the DAT and 8-mm drives for data recording, with VHS being applied to specialized, high-performance tasks.

DAT drives in 3.5-in. enclosures, which today store 2 Gbytes, will eventually pack 10 Gbytes, thanks to data compression and metal film tape. Also look for strong competition among drive manufacturers, which should keep prices low. At least 19 companies make DAT drives. And 8-mm drives should stay strong to serve workstations that use high-capacity hard drives and networked desktop systems. Data compression should increase capacity in these drives too.

### TAPE DRIVES REEL IN STEADY GROWTH

	1991	1993	1996
DAT	169	445	875
8-mm	127	170	228
VHS	0.3	0.6	1.1

in thousands of drives shipped

Source: Freeman Associates

## TALES FROM THE SKUNK WORKS

**T**he key attributes of an effective skunk works are instability, self-organization, overlapping development phases, multi-learning, subtle control, and organizational transfer of knowledge. It starts with instability, when the team is given a goal, not a plan, by upper management. The team's goal should be aggressive, for example, "Build a replacement for our best product with half the manufacturing cost and the same quality."

Once given a goal, the team is self-organizing. Separate and autonomous, the team develops its own plan. Once the team's plan is approved—and approving the plan means committing the agreed-to resource and budget—the team leader takes it from there. Management opens its purse and shuts its mouth, except at milestone reviews. A skunk works without autonomy is just a facade.

The effective skunk works is self-transcendental. It must break through, not extend, known limits to achieve the goal. The best teams are cross-fertilizing. The members have diverse backgrounds, and they draw from and share their knowledge.

The correct project approach is overlap, so all phases evolve in parallel. In my book I called this the Fat Arrow: the team members interact closely, subtly, rapidly, and without organizational friction. In the concept phase the technologist and guru (guru: the marketing equivalent of a chief engineer) iterate market need and com-

petitive opportunity against cost, risk, and schedule to make effective choices. Later this iteration is expanded to include production test, quality, and other issues. These early tradeoffs are critical. The time of creation, when over 90% of the investment is still ahead of you, entrenches most of the project's cost, risk, and success factors.

The team is multi-learning, which means its members draw their knowledge from everywhere. They use their experience, study competitive products, and examine seemingly unrelated things. Perhaps a feature from a consumer product might benefit a new type of computer. Anything is fair game for the team's innovation.

The control of the team should be subtle. This is not what one learns in most MBA classes, but it is true. Leadership, especially by example, is crucial. Management by directive or objective is usually inappropriate. You manage a skunk works by selection and developing a common vision. You want competent, fast-track, results-oriented people. If you

do this right, the energy released is amazing. (The saying, "Which way did they go? I am their leader and need to be in front!" usually prompts wry smiles from those who have been there.) Constructive peer pressure is encouraged but withholding information is cause for removal.

John D. Trudel is director of The Trudel Group, 52001 Columbia River Hwy., Scappoose, OR 97056; (503) 690-3300.



**A**t least 100 practical examples of analog circuit simulations are given in *A Spice Cookbook* by Karl Heniz Mueller. The reference, which comes with a disk, enables experienced engineers as well as novice Spice users, to model circuits and to develop future analog circuit simulations.

Circuit applications include RF, power, filter, digital, and microwave. For each example, the book gives a technical overview, including related equations, background data, schematic, IsSpice netlist, and resulting output graphs. Many circuit examples have a section that gives IsSpice tips and covers situations encountered during circuit simulation such as circuit initialization, convergence, Spice syntax pitfalls, device modeling, and circuit partitioning.

*A Spice Cookbook* is available from Charles Hymowitz, Intusoft, P. O. Box 710, San Pedro, CA 90733-0710; (213) 833-0710; fax (213) 833-9658. List price is \$49.95, including a disk. Educational discounts are available.

CIRCLE 451

**W**ritten by a technical placement specialist, *Job Search for the Technical Professional* guides engineers through a job search from mental outlook to resume writing all the way to interview techniques. Author David J. Moore points out that engineering jobs are more complex than other professional positions. As a result, job requirements are more stringent; competition for the best jobs is keen. That's all the more reason for technical job seekers to refresh their communication skills—written and oral.

Asserting that most hiring managers devote just 30 seconds or so to reading a resume, Moore suggests writing an FAB instead. This document tells an employer what a candidate has done (features); what the candidate has done with these features (accomplishments); and how a prospective employer might benefit from what has been accomplished (benefits). The FAB not only sets a candidate apart from the usual onslaught of resumes, Moore says, but also becomes a marketing tool to sell the job seeker to the employer. It's also good preparation for an effective interview.

Moore goes on to offer practical suggestions on creating a job search network, improving interpersonal skills, and negotiating salary. The book sells for \$29.95 in cloth and \$14.95 in paperback.

Contact John Wiley & Sons Inc., Professional, Reference, and Trade Group, 605 Third Ave., New York, NY 10158-0012 (ISBN 0-471-53137-5).

CIRCLE 452

**C**ontrol theory, implementation, and applications using TI's family of digital signal processors are covered in one-day seminars to be held around the U. S. this fall. The seminars describe how to implement control applications, like hard-disk drives, robotics, and motor control, with TI TMS320 DSP chips. Motor control theory is covered as well. The seminars are aimed at engineers and engineering managers involved in designing control systems and those who evaluate DSPs for control applications. A seminar will be held in Milwaukee on Nov. 4; in Chicago on Nov. 6; in Detroit on Nov. 8; in Cleveland on Nov. 11; in Toronto on Nov. 13; in Rochester, N. Y. on Nov. 15.

Registration fee for the seminar is \$50, which includes lunch, seminar workbook, and TI's application book, *Digital Control Applications with the TMS320 family*. Contact Texas Instruments Inc., Semiconductor Group, SC-91058, P. O. Box 809066, Dallas, TX 75380-9066; (800) 336-5236, ext. 700 or (214) 995-6611, ext. 700.

CIRCLE 453

### K M E T S K O R N E R

## ...Perspectives on Time-to-Market

**BY RON KMETOVICZ**

President, Time to Market Associates Inc.  
Cupertino, Calif.; (408) 446-4458; fax (408) 253-6085

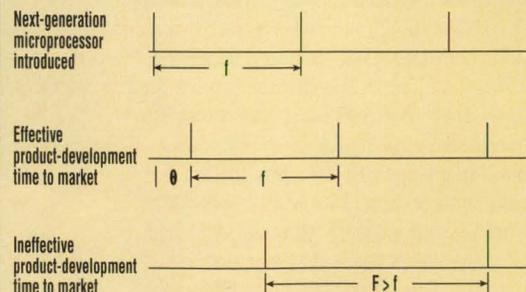


**I**mproving time-to-market performance helps eliminate technological change as a delay factor. The reason is obvious: Get the project/program done before a change can take place! In engineering terms, if the frequency,  $f$ , of product development and technological change are held equal and an effective phase relationship is established, then negative effect from this delay element is avoided (see the figure).

For most industries, you can gain an insight on the rate of technology turnover as a function of time. In the illustration, the predicted arrival from suppliers of new microprocessors—the technology that paces product development—is determined ( $f$ ). With this timing information in hand, the organization adjusts its product-development process ( $\theta$ ) to mirror arrival of the new technology—the company's new product follows right on the heels of the processor's introduction ( $\theta + f$ ). Taking this action helps the organization survive in the marketplace.

An organization that does little to understand the rate at which new technology can be expected to appear, however, will find itself in the situation set by the third timing diagram. Here the product based on the first generation of microprocessor arrives late ( $F > f$ ). Nonetheless, it's still ahead of the next generation of technology. Sales are lost, profits reduced, but marginal success will probably be achieved. Still, this extended TTM hammers the next product into market defeat. As shown, a product based on second-generation technology enters the market much later than the competitor's model and also at the same time the competitor introduces the third-generation model.

Set the timing of developing a new product to mirror the timing of new technology. Don't think that this is impossible until you've looked at some trends. Often, it's easy to predict how frequently technology will change. From that data, apply some engineering judgment to set your process timing requirements. Then design and install a product-development process that works within this window of opportunity. Strive to err by being too quick!



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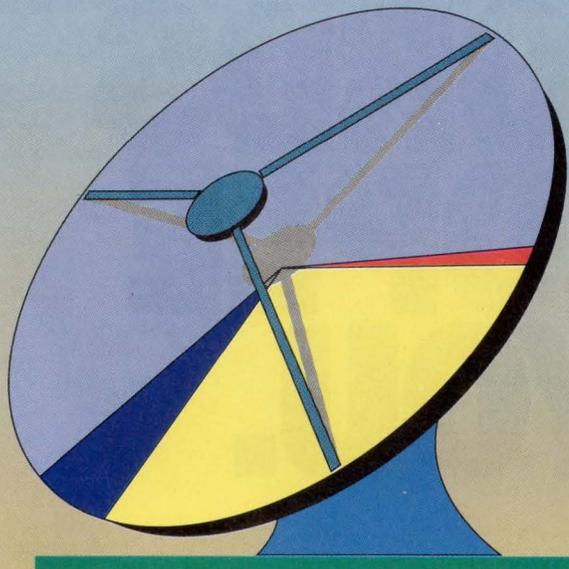
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CIRCLE 220 FOR U.S. RESPONSE

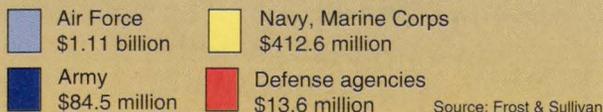
CIRCLE 221 FOR RESPONSE OUTSIDE THE U.S.

COME SEE US AT COMDEX  
BALLY'S HOTEL, BOOTH #B320

## DISHING UP DOLLARS FOR MILITARY SATELLITE COMMUNICATIONS



Total 1991 market \$1.62 billion



U.S. military communications depend on satellites, so much so that the U.S. will spend \$2 billion on them in 1992. The communications area is one of the few defense sectors to expand rather than to shrink, say New York market researchers Frost & Sullivan Inc. Growth lies in tactical terminals—extremely high frequency, super high frequency, and ultra high frequency—and in network-control equipment. Opportunities abound in ground communications. That sector should expand from its one-third share in 1991 to more than half of the market by 1996.

## QUICK NEWS

**S**mall, high-tech businesses are getting some help to tap into online public and private technology, services, and expertise under a program from the U. S. Commerce Department's National Institute of Standards and Technology (NIST) and the Small Business Administration (SBA). The Technology Access Program helps pay for small businesses' access to commercial, on-line data services. In Oregon, the program subsidizes access to Dialog, Vutech, CompuServe, and NASA databases and supplies access to consultants through a newly developed Oregon Network of Experts. In Pennsylvania, databases include Batorlink, Cartermill, CompuServe, Dialog Information Services, Dun & Bradstreet, Edin, and Knowledge Express Data Systems. Contact NIST, Administration A903, Gaithersburg, MD 20899.

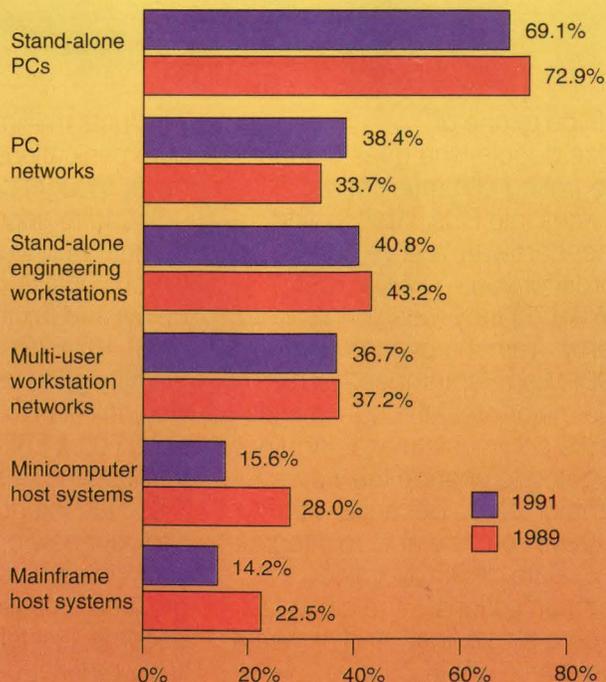
## OFFERS YOU CAN'T REFUSE

**A**s more and more designers work with digital signal processors so grows the need for information on DSP design. New software and hardware has improved Dr. BuB, Motorola's 24-hour DSP bulletin board. The system now has downloadable routines for the DSP96002, 56116, and 56000/1. Registered users can download files, send e-mail to the sysop or another user, and join discussions about digital signal processing and other topics. Expert applications engineers log on every day to monitor and join discussions. To login, dial (512) 891-DSP1 (891-3771) for 2400, 1200, or 300 baud modems. For the 1200-baud V.22 European standard, dial (512) 891-3772. Set the character format to 8 data, no parity. After making the connection, first-time users can log in as a guest or open a new account by selecting new, then following the prompts. Help is available at most levels. For answers to questions, leave mail for the sysop. For further information, contact Motorola's Digital Signal Processor Operation, Mail Drop OE314, 6501 William Cannon Dr. West, Austin, TX 78735-8598. **CIRCLE 454**

**F**ield-programmable gate arrays—the fastest growing category of programmable logic—are the subject of a free series of technical seminars to be given by Texas Instruments. TI developed the technical series to assist users in understanding the FPGA antifuse architecture and the role of FPGAs in design applications. The series will be held in 24 cities in the U. S. and Canada through late November. For more information on dates and times or to register, call TI at (800) 336-5236, ext. 3713.

## CAD/CAE SURVEY

### WHICH SYSTEMS DO YOU FOR CAD/CAE?

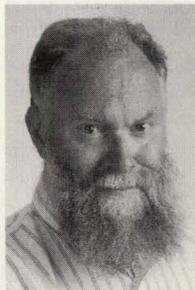


Source: a survey of Electronic Design readers conducted by the Adams Co., Palo Alto, Calif. (415) 325-9822

Readers gave multiple answers to the question.

# WHAT'S ALL THIS QUAKEY SHAKEY STUFF, ANYHOW?

**Y**ou only have to read the newspaper occasionally—*any* newspaper—to be aware of the earthquakes that occasionally rock and rattle various areas of California. People who live in the hills above Santa Cruz are VERY aware. For several years, I've proposed that we Californians need a good earthquake detector. Then suddenly I came up with 3 good ideas—three ideas with different levels of sophistication and usefulness. When a major scientific panel came up with an idea quite similar to my best idea, I asked the editors at Electronic Design to expedite this column.



**BOB PEASE**  
OBTAINED A BSEE FROM MIT IN 1961 AND IS STAFF SCIENTIST AT NATIONAL SEMICONDUCTOR CORP., SANTA CLARA, CALIF.

between. But, you need to do this in at least 2 dimensions, in 4 directions, and most people would find this bulky, expensive, and dangerous.

So my first invention, costing as little as \$1, is to set up a stack of 30 pen-

nies, a stack of 25 pennies, and stacks of 20, 10, and 5 pennies, on a standard sheet of paper. After a quake, you can see which of the piles fell, and in which direction. I set up one of these at home and one at work. During the big 7.1 quake, at home, the stack of 30 pennies fell, and the 20, but not the 25. At work, everything fell except the 5. So, for a small investment, you can compare notes with your friends. It's not absolutely calibrated, but you can get a ballpark indication of the amount of shock in your area.

I was still not completely satisfied, so I designed another detector-recorder. It's not exactly as technically correct or elegant as a seismograph built with levers and 10,000 turns of wire, as shown in *The Scientific American*. But you can use the little circuit shown below, to be triggered by a "swaying pendulum," and make a stretched-out pulse of perhaps 60 or 120 seconds.

This pulse can turn on your tape recorder or your camcorder for a minute or two to detect the creaking or rattling of things in your house. If you hear sirens, then the neighborhood may be on fire. If it also turns on a little radio, you can hear the radio announcer say, "Oh, my Gosh, that's a big one." If all the books fall out of your book-case, that will all be recorded, too. I just got it built up this weekend. I haven't yet seen how touchy it is about false alarms, but I can live with that....

On a more serious level, I realized that every time I climb under my car to work on something, or jack up the car even to change a tire, or climb up a ladder, I wish I could get an early warning of a far-off quake. When the workers at the Cypress Structure in

Oakland were using their heavy equipment to demolish the ruined concrete, they had the benefit of a little radio transmitter that would detect any quake down by Loma Prieta, the epicenter. A little radio receiver at the work site would give them 10 or 20 seconds of warning to jump off their crane, to get away from the dangerous piles of rubble, and increase their safety considerably. I don't know who engineered this, but as far as it went, it was a darned good idea. It must have made those brave workers feel a little less nervous about a quake sneaking up on them.

Well, I want to take that idea and expand it. I want to add in a bunch of features and make it available to everybody:

- I want to have a whole bunch of quake detectors, scattered all around the San Francisco Bay Area, located at interesting sites near and along each major fault. (Los Angeles can have their own network, and so can Tokyo).

- I want all of the sensors to transmit the warning of any significant quakes to a suitable central station, which can process the information and send it out immediately on two or more radio stations or TV channels.

The first radio station can monitor ALL quakes, large, medium, or small, and broadcast the information, and you can tune it in if you're going up on a ladder or under your car, or if you are just interested or curious. This will be a clear channel that will broadcast nothing but earthquake information and other related emergency info (tsunami reports, etc.), with an occasional tone to let you know you really are tuned in.

The second radio station would monitor all BIG quakes. Then you might just leave *this* station on all the time, even when you're asleep, so if it wakes you up with a computerized voice saying "Big one, Loma Prieta, Big one, BIG ONE...." you would have some warning to get under a table or a doorway, to grab a flashlight or a video camera, or to head for your kids' bedroom, or whatever you have decided in advance to do.

This second channel would be avail-

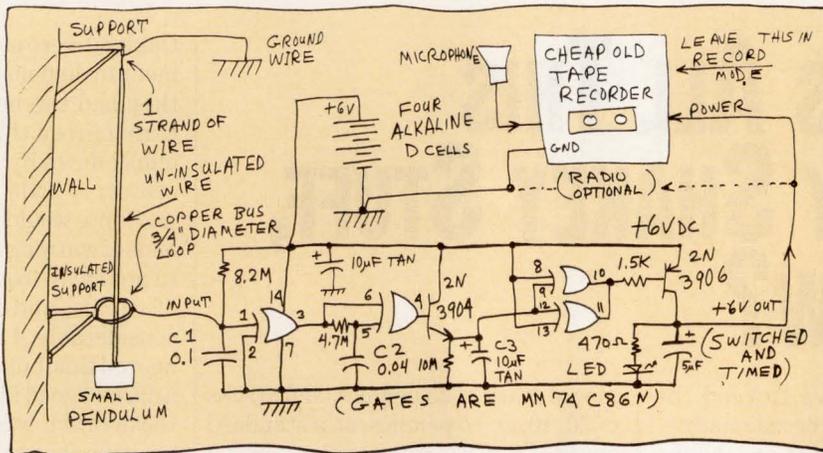
# PEASE PORRIDGE

able to any other radio station, for a small charge, so it could break in and give you advance warning, even if you're listening to a ball game, or the opera, or whatever. It could add onto a TV station, and break into the regular program material. The number of useful, life-saving possibilities is large but finite. You can use your own imagination.

Let's say you're listening and you hear about a quake starting in Sonoma. If you live in San Francisco, you know that's a few dozen miles away, so you have a number of seconds (at the rate of about 1.8 second per mile) to get in a safe mode. If you live in adjacent Napa county, you might have only a few seconds. So, the broadcast would have to tell you the location of the strongest shock, from a standard list of places, and you would have to be prepared to act suitably and instantly, depending on where YOU are located. You have to plan in advance, and you have to recognize all of the places on the standard list.

The sensors have to give you a very quick indication of what is the significance of the magnitude of the quake. I read in one popular scientific tabloid that some scientists were planning to set up a network of sensors and (digital) computers to analyze the data, and then give a warning in just "15 or 20 seconds." Don't look now, guys, but most of the people closest to the quake will be hit with the shock in only 5 or 10 seconds.

A perfectly computed analysis in 15 seconds would be no help at all. The key to the sensor is to have some wide-range logarithmic amplifiers and sensors that can put out appropriate signals for every size of tremor. Back in October of 1989, a friend of mine was standing in his garage, about 3 miles from the epicenter. He said, "In the first second, it knocked me on my butt". If a quake



THE FIRST GATE ACTS AS A HI-Z PREAMP WITH INPUT NORMALLY HIGH. THE NEXT GATE ACTS AS AN "ACTIVITY DETECTOR": ANY EDGE, RISING OR FALLING, CAUSES IT TO PUT OUT A HIGH PULSE FOR 0.1 SECOND. THE NPN HELPS STRETCH THAT PULSE FOR 50 SECONDS. THE OTHER 2 GATES ARE ALSO HI-Z PREAMPS WHICH DRIVE THE PNP AS A SWITCH & TURN ON THE TAPE RECORDER FOR A FEW DOZEN SECONDS AFTER ANY "ACTIVITY".  
NOTE, ONLY ONE FALSE EVENT/YEAR... RAP 1990-91

of that magnitude comes along, you can have pretty simple sensors, linear and logarithmic amplifiers, and discriminators or comparators that will get out the message "in the first second," which is the right kind of warning to save lives.

What if the quake's center is so deep underground (as it was in the Loma Prieta quake of 1989) that the shock waves hit areas several miles away from ground-zero, at just about the same time as it arrives at the sensors at ground-zero? Easy—drill a deep hole and put a few sensors down deep, to give advanced warning. Every mile of depth can help another few vital seconds.

Obviously, there are lots of practical and legal considerations. What if some driver gets the message and jams on his brakes, causing a pile-up worse than the quake damage? What if people get nervous and panicky and the first thing they do is call their lawyers? Obviously, the practical considerations aren't trivial. Still, if we plan a little, this system can be much better than no warning at all.

When I had this radio-warning idea back in December of 1989, I took it immediately to our Patent Committee at

National. They considered the scheme and decided it wasn't related to any of National's business, so they told me I could do anything I wanted to with it. I sent a technical note to a couple of the major radio and TV stations and newspapers in the Bay Area. The silence was almost overwhelming.

But in late August of 1991, a National Research Panel of experts from the National Academy of Sciences proposed a similar plan to assemble a system of seismometers, computers, and radios to give people an early warning\*. I immediately wrote off to the chairman, Mr. I. Selwyn Sacks of the Carnegie Institution in Washington. Soon I hope to hear more about their proposals. But you have already heard about my plans and proposals.

So, if this system gets going and it saves your life someday, you can buy me a beer. Fully-paid licenses, of course, are available at a very reasonable fee.

You may not have many earthquakes in your area, but you have to agree, it's certainly a fascinating and challenging set of problems to think about. Maybe you have ideas that are better than mine, or that would improve mine when added to it. You don't have to sit on top of a big fault to have good ideas.

All for now. / Comments invited! /  
RAP / Robert A. Pease / Engineer

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\* "Experts Push High-Tech Quake Detection System," Warning of even a few seconds could save lives; San Francisco *Chronicle*, August 28, 1991, page 1.

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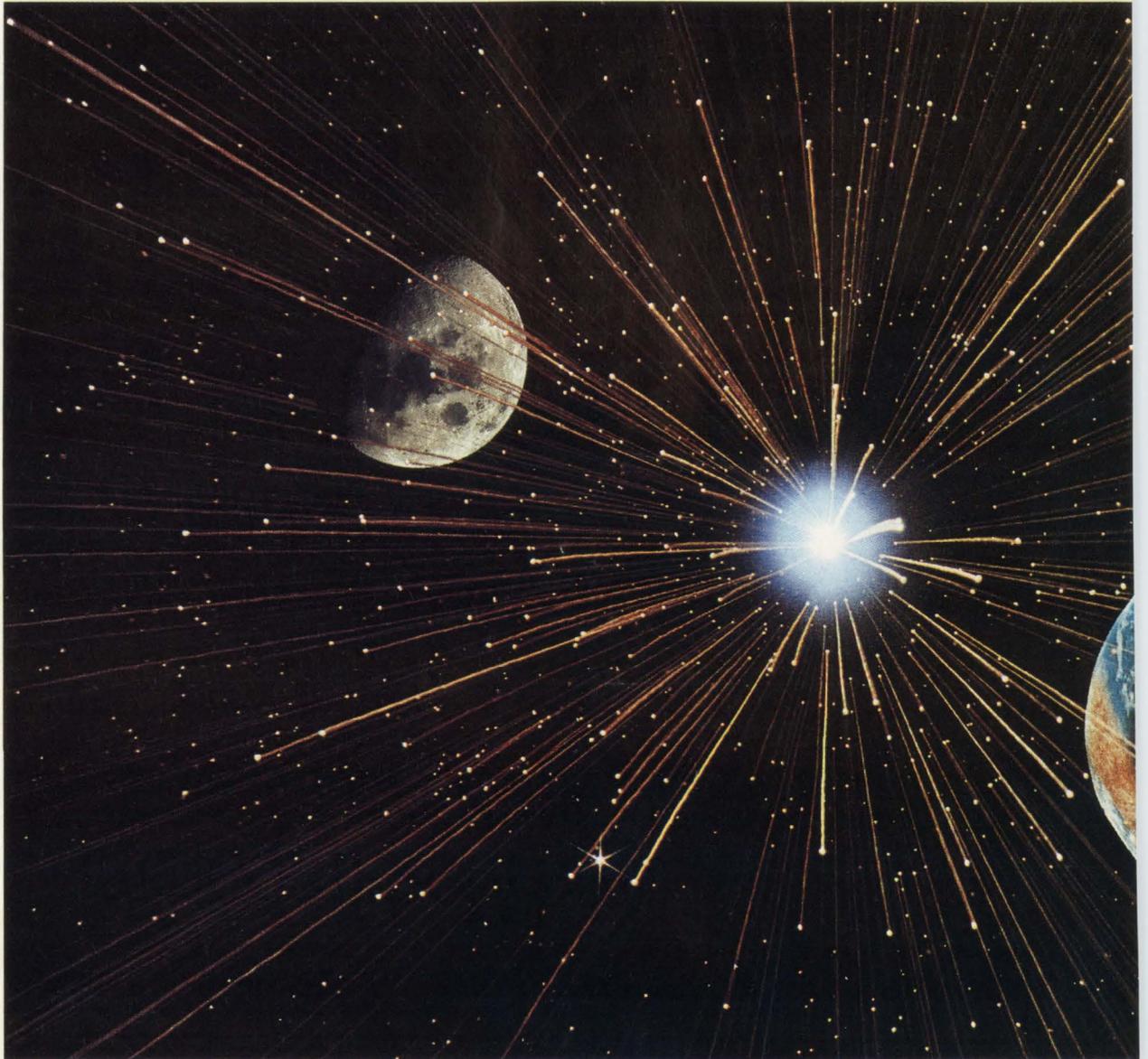
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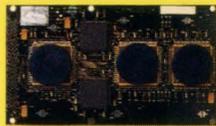
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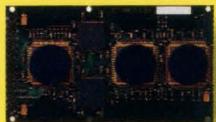
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# 8-BIT VOLTAGE- OUTPUT DACS SPORT 11-BIT RESOLUTION

FRANK GOODENOUGH

An 8-bit DAC is an 8-bit DAC is an 8-bit DAC. Well... not always. Micro Linear's latest 8-bit digital-to-analog converters give you 11 bits of resolution and dynamic range. The four members of this new family of "anything but conventional" 8-bit voltage-output DACs—the ML2340/41 and ML50/51—offer a number of innovative features for the first time (*Fig. 1*). However, one feature in particular stands out. A 2-bit input word on the gain-control inputs sets the output op amp gain at 1/4, 1/2, 1, and 2. That is, changing the gain-control bits from 00 through 01 and 10 to 11 doubles the full-scale output voltage three times. Each doubling essentially adds a bit of resolution and dynamic range to give you a final effective resolution and dynamic range of 11 bits (*Fig. 2*).

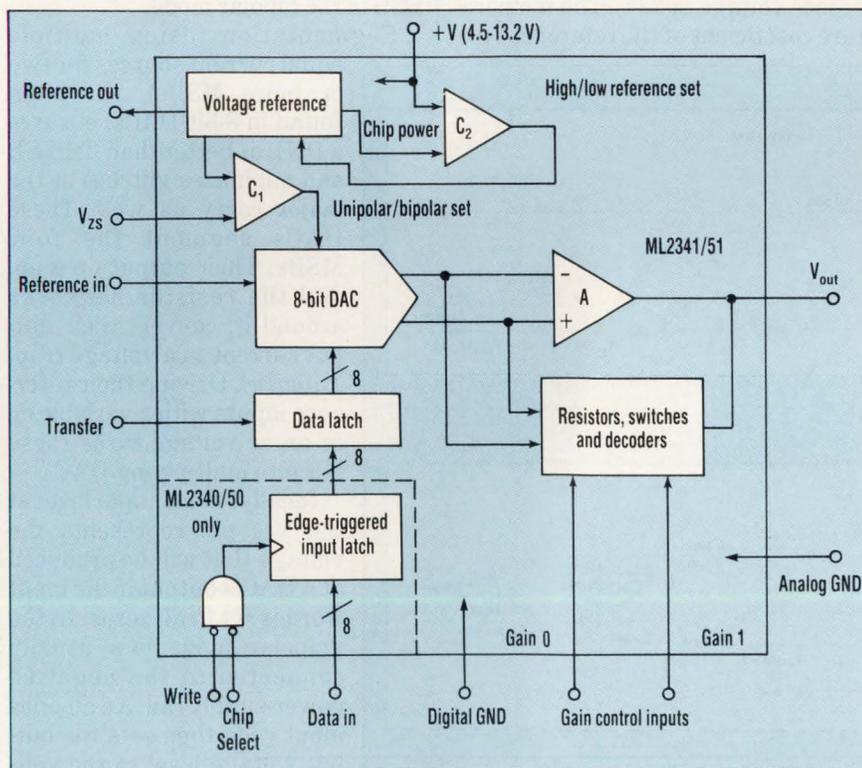
Moreover, the DACs' ability to operate from a single power supply enables them to provide unipolar or bipolar output voltages. Comparator  $C_1$  monitors the  $V_{ZS}$  pin. By connecting the comparator to less than 1 V, you can get a unipolar output that swings from the voltage on that pin to within 100 mV of the plus power-supply rail (at maximum gain). If the  $V_{ZS}$  pin is connected to greater than 1.5 V, you can get a bipolar output swinging around  $V_{ZS}$

(*Fig. 2, again*).

And if those analog circuit tricks aren't cunning enough, how about a second comparator,  $C_2$ , that monitors the power-supply voltage? If it's less than approximately 7.5 V, the internal reference is set at 2.25 V (ML2340/41) or 2.5 V (ML2350/51). If the power-supply rail is above 7.5 V, the reference voltage automatically doubles.

Though aimed at single-supply applications, particularly disk-drive and automotive uses, these DACs can fill a variety of size-8 DAC shoes. The ability to change the amplifier's gain is especially useful in servos. These include the speed-control loop for the voice-coil head-positioning motor in a disk drive, and the speed or position control loop for automotive actuators.

In a position-servo application, the set-point input drives the  $V_{ZS}$  pin, while the digital input word to the DAC represents the error signal. When a new set point is applied, the error signal is large. Thus, maximum gain is required. If operating in the bipolar mode from a 12-V power-supply rail, each code change represents



**1. A TWO-BIT WORD** on the gain-control inputs of the single-buffered ML2340/2350 8-bit DAC changes the output voltage by a factor of up to eight. As a result, 11-bit resolution and dynamic range is provided. The double-buffered version, the ML2341/2351, is identical except for the additional circuitry shown within the dotted lines.

# 8-BIT DACs WITH 11-BIT DYNAMIC RANGE

35 mV. As the servo begins to home in on the set point, the gain is reduced until reaching corrections as fine as 5 mV per code change.

In a speed-control loop,  $V_{ZS}$  is tied to ground for unipolar (unidirectional) operation, and to the reference for bipolar (bidirectional) operation. The digital word to the DAC represents the speed command, which will have a maximum value when motion is requested. As the set point is approached, the DAC's analog output will be reduced in amplitude by decreasing the value of the digital word and also by decreasing the gain of the op amp.

## KEEPING UP

With a 30-ns maximum write time and no hold time, the DACs can keep up with the latest microprocessors. Each DAC output sources and sinks a minimum of 10 mA and swings to within 10 mV of ground and 40 mV of the plus power-supply rail as it drives a load of 100 k $\Omega$ . While driving a load of 1000  $\Omega$ , it swings within 1 V of both power-supply rails and settles to within 1/2 LSB of those levels

## SINGLE- VS. DOUBLE-BUFFERED 8-BIT DACs

	ML2340 buffered	ML2350 buffered	ML2341 buffered	ML2351 buffered
Characteristic Digital interface	Single	Single	Double	Double
Voltage reference (V)	2.25 or 4.5	2.5 or 5	2.25 or 4.5	2.5 or 5
Packages	18-pin DIP 18-pin SOIC	18-pin DIP 18-pin SOIC	20-pin DIP 20-pin PCC	20-pin DIP 20-pin PCC

in under 3  $\mu$ s maximum. Settling time to within 1/2-LSB accuracy and to within 100 mV of the power-supply rails takes 6  $\mu$ s maximum. Any gain change requires 3  $\mu$ s maximum. Such specifications are more than fast enough for virtually any electro-mechanical servo-loop application.

The four DAC models differ chiefly in their reference voltage, digital interface (double or single buffered) and packages (*see the table*). Micro Linear states that operating-temperature (T) conditions for all specifications (including those mentioned previously) run from  $T_{min}$  to  $T_{max}$  and from both 5- and 12-V power-supply rails. In addition, it specifies the reference voltage at 25°C. The temperature coefficient of the reference typi-

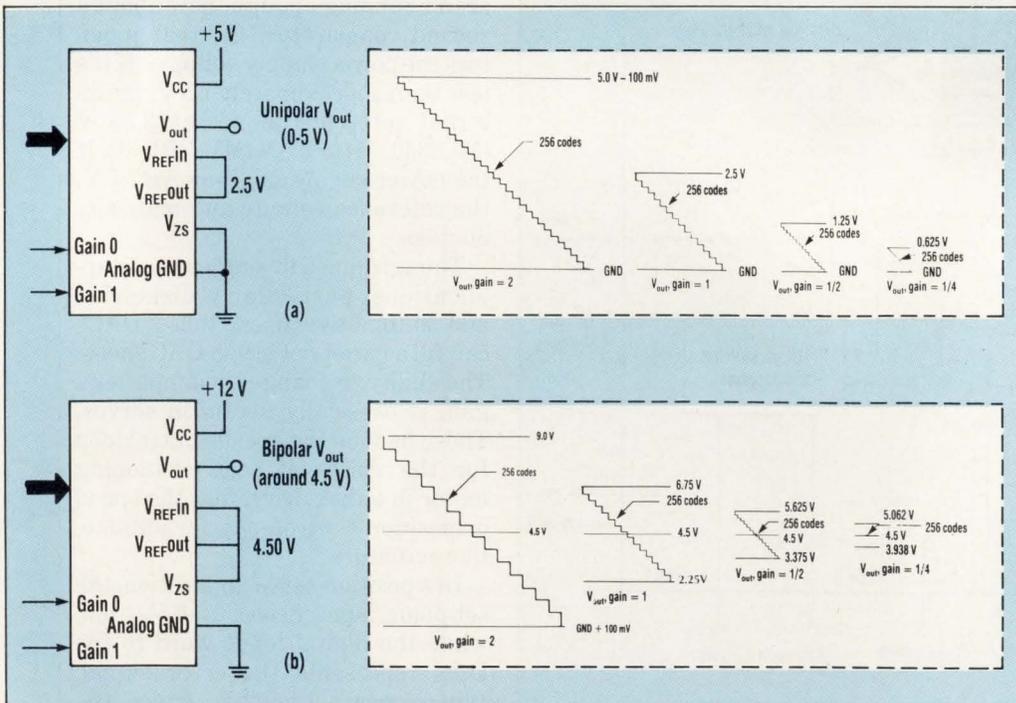
cally runs 50 ppm/°C.

Three performance grades are available. They permit devices to be selected with maximum differential and integral linearity (DNL and INL) errors of  $\pm 1/2$  or  $\pm 1/4$  LSB while independently selecting between maximum gain errors of  $\pm 2\%$  and  $\pm 2.5\%$ . These specifications hold regardless of gain setting, and whether operating in a bipolar or unipolar mode. Because DNL over temperature is better than  $\pm 1$  LSB, monotonicity, which is mandatory for servo-loop applications, is assured. Offset error in the unipolar mode runs a maximum of  $\pm 24$  mV, and no more than  $\pm 10$  mV,  $\pm 2.5$  LSB in the bipolar mode.

Segmentation (using multiple equal current sources for two or more MSBs), not often found in 8-bit DACs, ensures a DNL of better than  $\pm 1$  LSB and minimizes glitches at the major carry as well. These DACs segment the four MSBs. Their output op amp, and the resistor networks around it, convert their output current to a voltage (*Fig. 1, again*). Driving their reference inputs with a variable dc or an ac voltage turns these ICs into multiplying DACs.

Ideally, the voltage level at the  $V_{ZS}$  pin represents the voltage that will be produced at a DAC's output if the input word is set to all zeros. In the unipolar mode, it's usually connected to the negative power-supply rail. An all-ones input code then sets the output voltage level to the voltage level at the reference input, multiplied by the gain (*Fig. 2, again*).

Typically, when operating



**2. THE ML2340 FAMILY** of 8-bit DACs from Micro Linear can supply a unipolar output voltage from zero to the reference voltage multiplied by the gain by setting  $V_{ZS}$  below 1 V (a). Setting  $V_{ZS}$  above 1 V provides a bipolar output, around  $V_{ZS}$ , which is also a function of the reference voltage and the gain (b).

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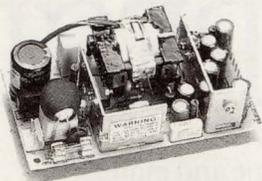
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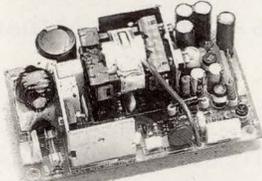
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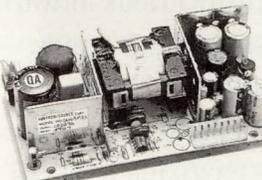
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## 8-BIT DACs WITH 11-BIT DYNAMIC RANGE

in the bipolar-mode, the  $V_{ZS}$  pin connects to the reference and the output swings above and below it. However, other voltages can drive the pin, such as the output of a second DAC.

The input word applied to the basic DAC is in a two's-complement-binary format, resulting in an output voltage equal to  $V_{ZS}$  for an all-zeros input. An input code of one followed by all zeros (10000000) produces an output of  $V_{ZS}$ , minus the full-scale voltage. An input code of zero followed by all ones (01111111) produces an output of  $V_{ZS}$ , plus the full-scale voltage. As in the unipolar mode, the full-scale voltage is the voltage at the reference input multiplied by the gain.

The unique dual-voltage reference (it sources 5 mA and sinks 1 mA) lies at either 2.25 V (or 2.5 V), or 4.5 V (or 5 V), depending on whether the voltage on the plus power-supply rail is above or below 7.5 V (see the table, again). As a result, to prevent the reference and thus the output from oscillating between two values, the device should not be operated from a 7-to-8-V plus power-supply rail.

On the other hand, operating from this power-supply rail could provide some interesting performance: For example, it offers another bit of dynamic range and could make a very interesting variable-amplitude square-wave generator. It should also be noted that while 7-8 V isn't a standard power-supply rail, some mix of batteries might reach those levels while discharging or charging. And with a current drain of between 5 or 10 mA from 5- and 12-V power-supply rails, respectively, these DACs are a natural for battery-powered applications.

### FLOW-THROUGH WORDS

When choosing between the single-buffered ML2340/50 DAC and double-buffered ML2341/51 DAC, both of which offer two (digital) operating modes, you can select a wide range of digital I/O flexibility (Fig. 1, again). The I/O of the single-buffered ML2340/50 DAC consists of just the 8 data inputs and the Transfer input. In the single-buffered mode, the input words pass through

an 8-bit transparent latch on the rising edge of the Transfer command. Because the latch's outputs connect directly to the inputs of the current DAC, changes in the digital word—while Transfer is active—causes an immediate change in the DAC's output voltage. To hold the digital word on the latch, the Transfer input must be brought low while the data is stable. In the flow-through mode, the input latch is bypassed. The Transfer input is held high and any changes in the data appear at the DAC's analog output.

The I/O of the double-buffered ML2341/2351 DAC adds a Chip Select and a Write input to the data and Transfer inputs. Operating in a single-buffered mode, the DAC's Transfer input is held high to put the DAC latch in a transparent mode. The rising edge of a command on the Write input, when the Chip Select input is low, latches the input word into the input latch and updates the analog output.

In the double-buffered mode, the rising edge of a command on the DAC's Write input while the Chip Select input is low latches the data into the input latch. Bringing the DAC's Transfer input high then moves the data into the DAC latch, updating the analog output.

A power-on Reset internal to all four DACs initializes them when power is first applied. The reset interval, typically 8  $\mu$ s, starts when the supply rail reaches about 2 V. During this period, every latch is set to all zeros. □

### PRICE AND AVAILABILITY

Commercial-, extended-industrial-, and military-temperature grade DACs are available. In quantities of 100, pricing for the single-buffered ML2340/ML2350 starts at \$3.75 each in 18-pin plastic DIPs. Their double-buffered cohorts in the same quantity each go for just 10 cents more. Surface-mount-packaged DACs will be available by year's end.

Micro Linear Corp., 2092 Concourse Dr., San Jose, CA 95131; Al Tremain, (408) 433-5200.

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# CHIP SET, STANDARD TAKE

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### TO 10 GBYTES

BUILT FOR SERVO TECHNOLOGY AND MAGNETO-RESISTIVE HEADS, A FOUR-CHIP SET INCREASES TAPE CAPACITY.

**RICHARD NASS**

**I**n a recent announcement, the Quarter-Inch Cartridge (QIC) Committee disclosed a new standard that raises the capacity of quarter-inch magnetic-tape drives from 2 to 10 Gbytes. To reach such capacities, changes had to be made in the recording head, and servoing technology had to be added to the tape drive. These alterations require modifications to the drive's electronics. To meet that demand, International Microelectronic Products (IMP) Inc., San Jose, Calif., is offering a chip set that completely integrates the read-write and servo channels for magneto-resistive (MR) heads. MR heads offer greater bit and track densities and produce a much larger signal output than current technologies.

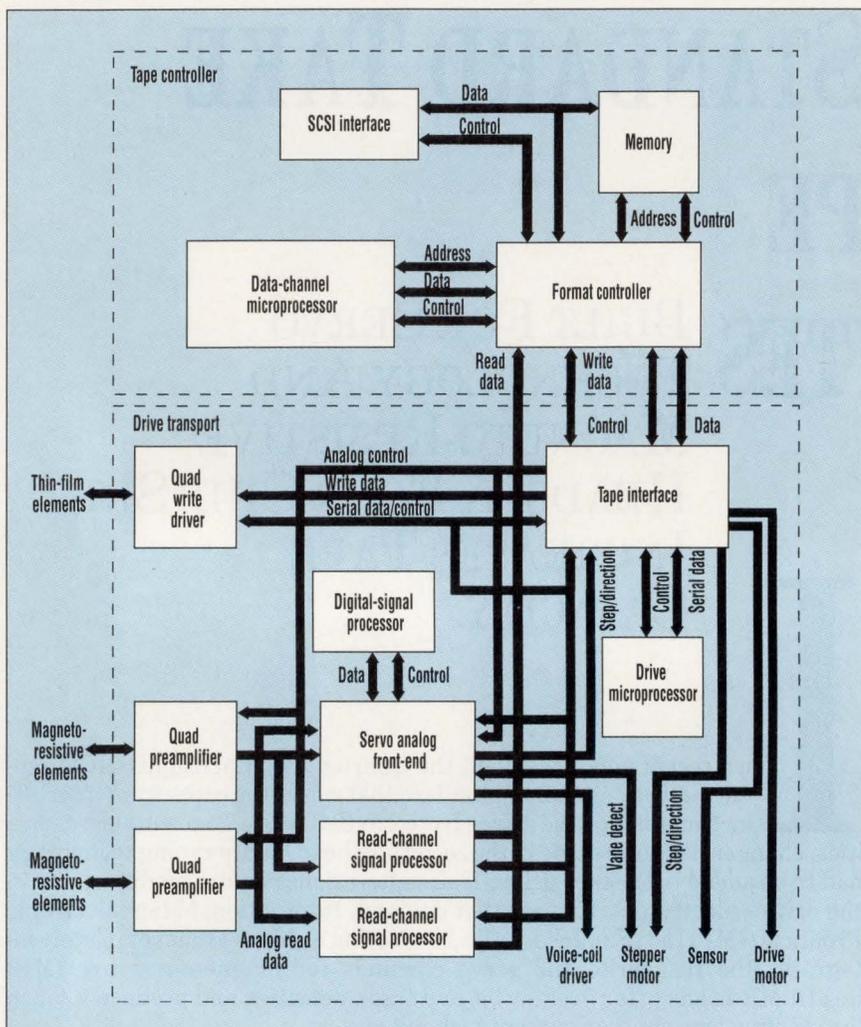
The chip set is the product of a joint development project involving IMP and 3M Co., St. Paul, Minn. The parts will be manufactured and sold by IMP, and will also be used in 3M data cartridges that employ magnetic tape. 3M is a main supplier of data cartridges.

The set consists of four chips: the IMP52C414 quad magneto-resistive preamplifier, the IMP52C434 quad write driver, the IMP52C464 read-channel signal processor, and the IMP52C484 servo analog front end. The set was built with a 1.2- $\mu$ m CMOS process. IMP claims that this is the first time CMOS has been used as a low-noise preamplifier for an MR-head-based system. Previously, the functions were implemented in bipolar technology. The chip set operates from a single-ended, +5-V supply. Many previous chip sets required an additional 12-V supply.

The chip set is currently specific to QIC tape drives. In the future, IMP will try to migrate the technology to hard-disk applications using MR heads. The company feels it has a jump on the competition because it has already invested a few years working with MR technology. Its goal is to be the first to supply a single-chip read channel with an electronic filter to the hard-disk-drive makers. IMP feels that this is the first true integration of dedicated read, write, and servo channels done in CMOS that are targeted for MR heads. It's also the first chip set designed for QIC drives with storage capacities greater than 2 Gbytes.

The set is compatible with all QIC drives dating back to the 40-Mbyte standard. It was originally designed to meet the QIC 6-Gbyte standard, but it can also fulfill the recently announced 10-Gbyte standard. In addition, the

# 10-GBYTE 1/4-IN.-TAPE CHIP SET



**TO BUILD A QIC-COMPATIBLE TAPE DRIVE** using the IMP chip set, two quad preamplifier chips, two read-channel signal processors, one quad write driver, and one servo front-end chip are required. This configuration can store 10 Gbytes of data. The 10-Gbyte standard was recently passed by the QIC committee.

chip set pushes the range for the data-transfer rate to 30 to 72 Mbytes/min.

IMP contends that the 414 is the first commercial preamplifier for MR heads. The MR heads offer a higher signal level and permit higher tape densities. They differ from earlier heads because a bias current is required. As the MR head passes over a flux transition, the resistance changes. When the bias current is applied to the resistance change, the resulting voltage change is sensed. The 414 supplies the needed biasing.

Very little noise should be present in the bias current, a factor that influenced the switching from bipolar to CMOS. The preamplifier doesn't

require any external circuitry, except for some resistors that set the sense current and one that serves as a current reference.

The chip contains four independent amplifiers. In the QIC 6000 standard, the tape holds 96 tracks of data and 16 tracks of servo information. The 10-Gbyte standard increases the number of data tracks to 144, plus 24 tracks of servo information. At any one time, the head could be reading one servo track and two data tracks. IMP realized the potential for incoming standards to read four tracks simultaneously. Consequently, the chip set is partitioned in four separate chips to allow for future upgrades by the QIC commit-

tee. The chip's fourth amplifier helps support older standards where the track width is wider and a servo isn't used.

The 434 write driver, which can be configured through the serial interface, contains four input channels that can be gated to any of the four driver outputs. The chip's inputs can all write data simultaneously. Configuring consists of mapping the inputs to the outputs. The chip's write current is programmable, which lets the drive program the optimum write current. Too much or too little current could have an adverse effect on the bit-error rate (the probability of one error occurring in a particular number of data bits). According to IMP, this feature doesn't exist on any other write driver.

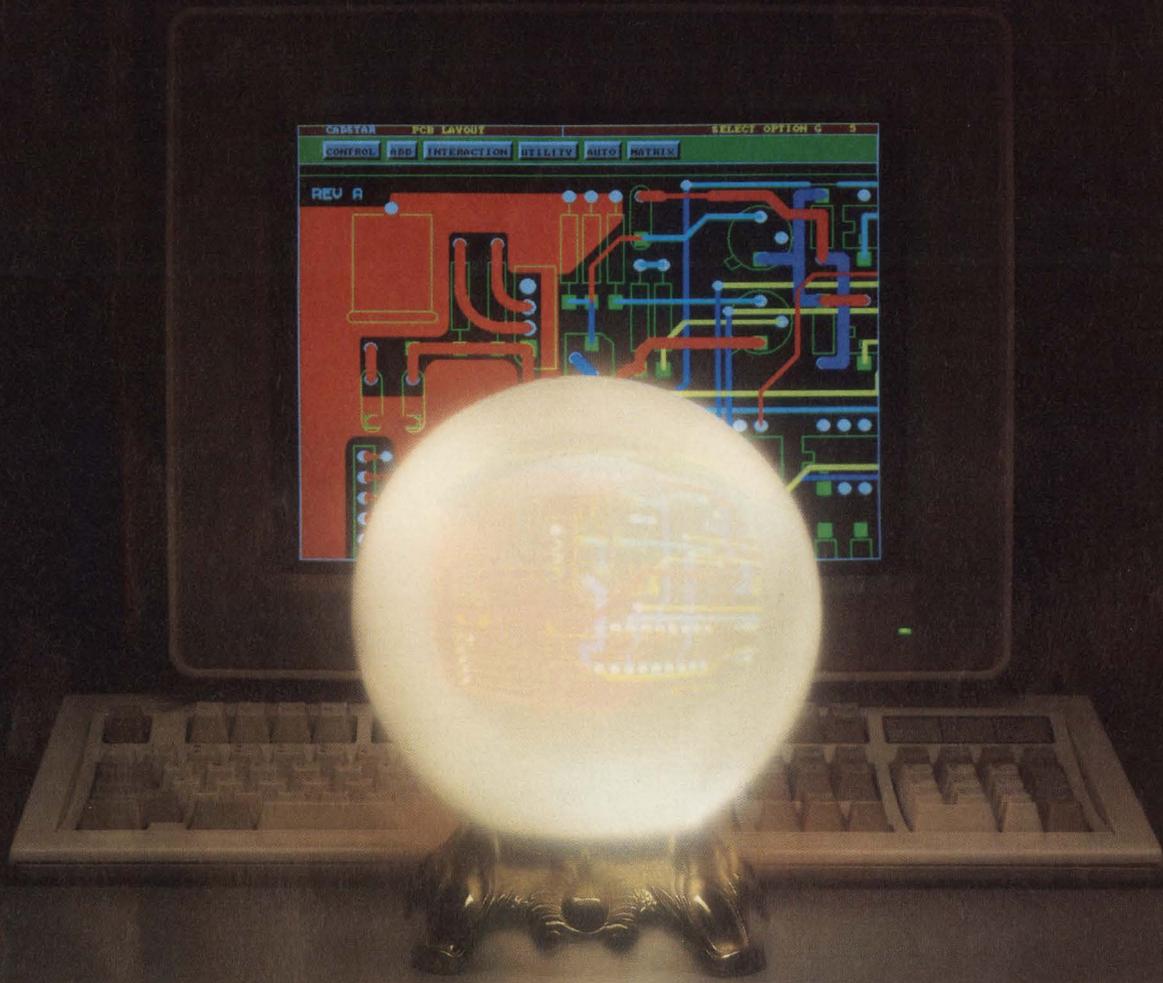
Automatic demagnetization is another feature that IMP maintains doesn't exist in competitive products. After each write cycle, the write current is ramped down and the output is toggled, erasing any residual magnetization that might be on the head. Although the part runs at 5 V, clamping doesn't occur until the output reaches 8 V. If it's clamped earlier, the settling time would increase. This is because the time constant of an RLC network is  $L/R$ , where a small  $R$  corresponds to a large settling time. With this method, fast transitions are achieved, as well as a high data rate.

## COMBO CHIP

The read-channel signal processor, which includes a gain block, filtering, a pulse detector, and a data separator, is commonly referred to as a combo chip. It contains a multiplexer on the input to select any one of eight preamplifiers. A drive typically contains two quad-amplifier chips to form a row of forward and backward read elements, so that everything written to the tape can also be read. The gain block can be digitally programmed through the serial interface.

An analog automatic gain-control loop controls the gain once it's been set in the right range. And the filter supplies equalization for amplitude and phase distortion for the input

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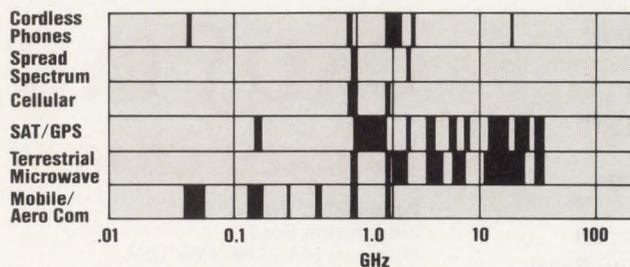
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## 10-GBYTE 1/4-IN.-TAPE CHIP SET

read signal. It bandlimits the signal's noise and performs a pulse-limiting function that narrows the pulses to minimize interaction between adjacent pulses. IMP claims that no other vendor's parts supply both magnitude and phase equalization.

For phase adjustment, the 464 contains two stages of lead-lag. It also attenuates low-frequency noise, a characteristic of the MR head. Users can program the amount of pulse slimming, the location of poles and zeros that affect phase equalization, and where the filter's cutoff should be. The chip's pulse detector senses the filter's output and determines where the pulse reaches its peak, then supplies an output pulse corresponding to that peak. The hysteresis for qualification is also programmable.

The 464's on-chip data separator extracts a clock from the data and synchronizes the data to that clock. It allows a phase-locked loop (PLL) to operate over a wide range of data rates and supplies the backward-read compatibility for different QIC standards, including varying tape speeds, encoding schemes, and corresponding data rates. The PLL can be programmed to support each standard.

### FRONT-END CONTROL

The QIC standard is the first to support a servo. The servo functions are handled by the 484 analog front end. This part combines with a DSP chip, such as a TMS32010, to implement the servo loop filter. All of the analog outputs are supplied by the front-end chip so that the loop filter can be implemented in the analog domain. The implementation of the loop filter depends on the mechanics of the specific drive. The servo positions the head on the tape after determining which tracks are being read. It contains coarse and fine positioning.

Fine positioning is achieved by placing a modulated carrier on the tape. The servo front end demodulates the servo signal and provides a signal that corresponds to the head's position on that servo track. The demodulated signal is then taken off-

chip to either the DSP IC or the analog servo filter. In the DSP implementation, the signal is taken back on-chip to a digital-to-analog converter that drives a voice coil, ultimately supplying the fine head positioning. The coarse positioning is done by a stepper motor.

The chip contains two demodulators, one for each row of read elements. The demodulators read the two elements, then take an average to get the most-accurate head positioning and compensate for any rotation that might exist in the head assembly. The part also improves noise sensitivity while compensating for small dropouts. The chip's programmable circuitry detects different error conditions, such as out-of-range signals, dropout detection, and whether a servo or data track is being read.

The drive talks to the front-end chip, then the front-end chip converses with the DSP chip. Hence, all of the control goes through the front-end part. A typical system would contain two quad preamplifier chips, two read-channel signal processors, one quad write driver, and one servo front-end chip (*see the figure*).

In a one-data-track system, all that's needed is one preamplifier, one servo, one read-channel signal processor, and one write driver. It's also possible to increase the number of tracks by adding more preamplifiers, read-channel signal processors, and write drivers. That's one reason why the servo front end was kept separate from the read-channel processor.

### PRICE AND AVAILABILITY

*The chip set goes for \$300 in single-unit quantities. Production should begin in the first quarter of next year. Depending on the configuration, the chip set should sell for \$35 to \$65 by the end of 1992 in OEM quantities.*

*International Microelectronic Products Inc., 2830 N. First St., San Jose, CA 95134; (408) 432-9100. CIRCLE 514*

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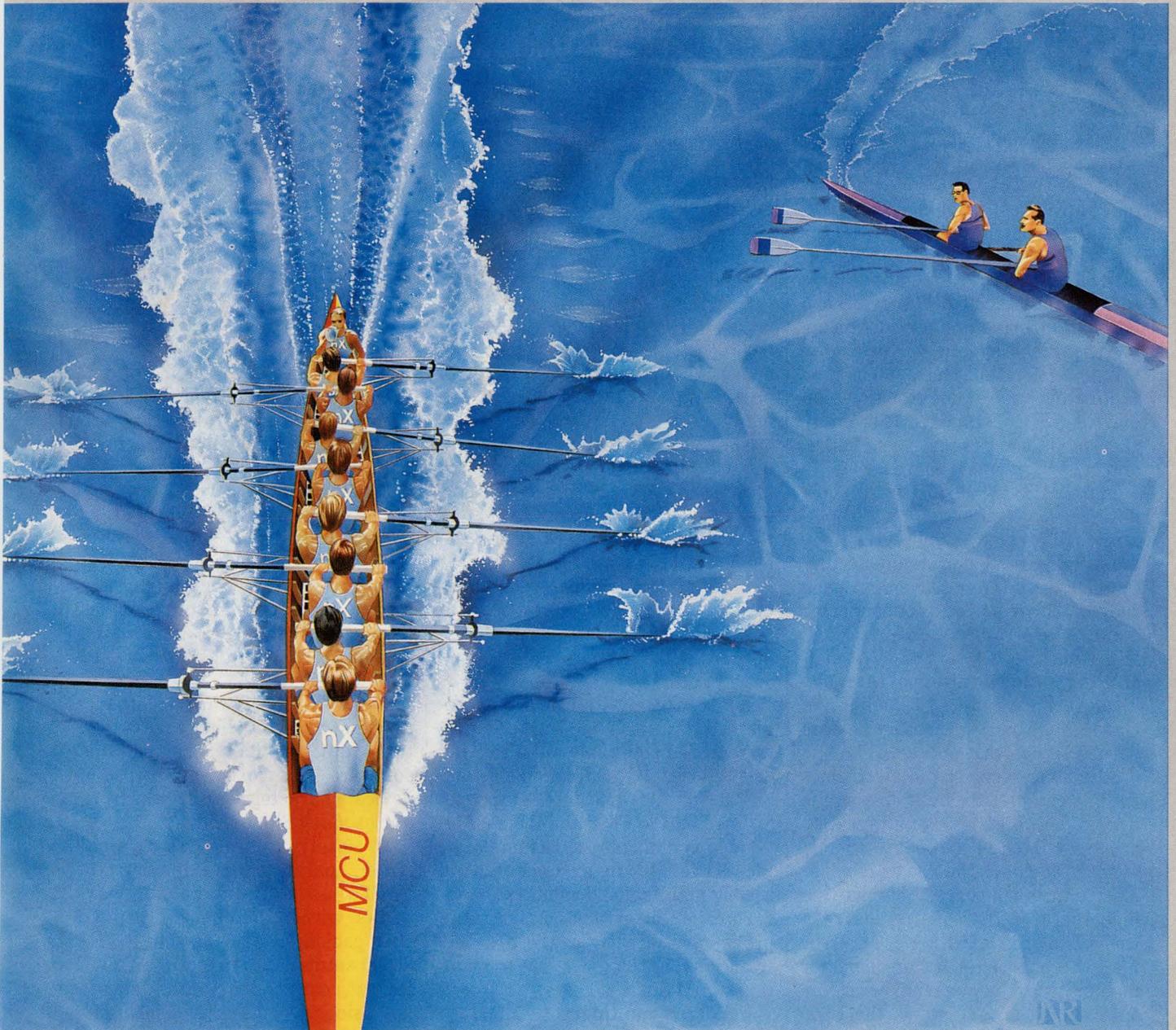
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# 660-MHz DIGITAL TESTER RUNS THE GAMUT OF IC APPLICATIONS

JOHN NOVELLINO

As digital devices become faster and more complex—and more costly to test—users have been looking for solutions that can economically solve the entire test problem. Hewlett-Packard's answer to this quest is the HP 83000 Model F660, a high-performance, digital test system that tests the most advanced digital devices in both engineering and production applications. The system performs prototype verification, characterization, failure analysis, and production testing for ASICs, standard ICs, multi-chip modules, gate arrays, PLDs, and even high-speed boards.

The HP 83000 F660 boasts some impressive specifications: a top operating frequency of 660 MHz (non-multiplexed), measurement accuracy of 50 ps, and edge-placement accuracy of 80 ps at the I/O connector plane. A level range of  $-2.5$  to  $+5.5$  V, with a maximum swing of 5 V, is suitable for testing a variety of technologies, including ECL, CMOS, and GaAs. A 1-Mvector memory is standard; 4 Mvectors is optional.

All driver-receiver pin electronics for one channel are built on a single hybrid. This high level of integration accommodates 16 channels on one I/O board. Besides the driver-receiver electronics each board holds two timing generators, a formatter and real-time-compare (RTC) logic, an error map, three level generators, a vector memory, and sequencing electronics. Using the RTC logic, the F660 checks the sampled data in real-time against the expected results stored in the vector memory. The compare result is stored in the error map.

The compact test head mainframe holds up to 32 boards for a maximum channel capacity is 512 pins (see the figure). But HP plans to introduce the capability to add a second mainframe, which would double the channel count.

The F660 includes one dc parametric-measurement unit (PMU) per I/O



board. All installed PMUs can run in parallel, for faster dc measurements.

The system's tester-per-pin architecture allows users to select timing, levels, and sequence control on a per-pin basis, with the ability to change those set-up parameters during the test procedure. Data formats include nonreturn to zero, delayed nonreturn to zero, return to zero, return to one, and return to complement. Users can switch to tristate at any time on any format.

HP is offering four device-under-test (DUT) interfaces. The 512-pin interface is compatible with the HP 82000-series IC evaluation system. (HP 82000 files and test setups can be used on the F660 and the user interface is similar.) A 1024-pin interface is available for systems with the second mainframe. In addition, a wafer-prober interface connects the probe card directly to the pin electronics using coaxial cables to maintain signal fidelity.

Finally, a multipurpose interface creates a mechanical connection to the mainframe as well as an electrical connection to the I/O boards. This type of arrangement gives users the ability to design their own customized interface to the DUT. The interfaces can be quickly changed without tools.

A high-speed fiber-optic link connects the system controller, an HP 9000 Series 400 workstation, to the tester hardware. This link speeds both the commands from the work-

station and the downloading of data to the tester. In addition, data is sent in a compressed format, which speeds up downloading by a factor of five, compared with uncompressed transmission.

The industry-standard, open-architecture controller supports the X-Terminal networking standard. As a result, one person can be on-line running a test program on the F660 hardware while three others are developing test programs off-line at remote terminals.

The F660's software includes a new fast-Shmoo facility that is five times quicker than normal Shmoo software. This can be very helpful in device characterization, which requires many Shmoo plots.

To closely integrate design, simulation, and test development, the F660's user interface software works with a number of popular CAE packages. Also, most of the HP 83000 setup data is stored in ASCII format, so users can edit the data off-line using any editing tool, including word processing software. IEEE-1149.1 boundary-scan testing can be performed using HP boundary-scan software, which includes the boundary-scan description language (BSDL)

The HP 83000 Model F660 price depends on configuration, with a typical 256-channel system selling for about \$1.6 million.

Hewlett-Packard Co., 19310 Pruneridge Ave., Cupertino, CA 95014; (800) 752-0900. CIRCLE 571

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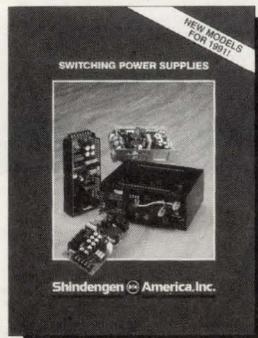
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Front-panel operation is through either the keypad or a multifunction rotary knob with detents. The unit stores 15 user-defined waveform setups in a non-volatile memory. Users can select a 50- or 600- $\Omega$  output. Arbitrary waveform data can be downloaded through the 2030's IEEE-488 or RS-232 ports into a 256-kpoint waveform memory. The instrument can then output the waveform at up to 50 Mpoints/s.

The 2030 generates waveforms by calculating the selected waveshape, along with digital corrections for the



analog output stages. This technique yields nearly ideal sine, haversine, square, triangle, ramp, and pulse waveforms. Linear and log sweeps are phase continuous. White noise can be added to any waveform. Because the chosen modulation signals are merely a part of the waveshape calculation, they have virtually no distortion or frequency limits.

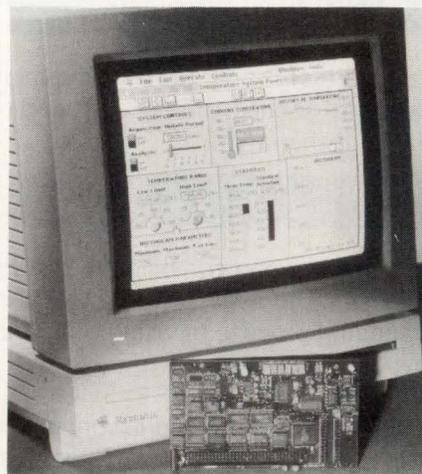
The Model 2030 costs \$3995, including isolated output, full waveform generation capability, RS-232 and IEEE-488 interfaces, and PC software.

**Analogic Corp.** 8 Centennial Dr.  
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■ JOHN NOVELLINO

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Three plug-in boards expand data-acquisition options for users of the Macintosh LC and Macintosh II. The Lab-LC is a multifunction analog, digital, and timing I/O board for the Mac LC. The board has eight 12-bit single-ended analog input channels, two 12-bit analog output channels, 24 TTL digital I/O lines, and three user-available 16-bit counter-timer channels for timing I/O functions. The NB-TIO-10 and NB-DIO-96 are for the Mac II. The NB-TIO-10 is a timing and digital I/O interface with ten 16-bit, 7-MHz, user-configurable counter-timers, and 16 TTL digital I/O lines organized into two 8-bit, bit-configurable ports. The NB-DIO-96 has 96 TTL digital I/O lines organized into 12 8-bit ports. The board can operate in either unidirectional or bidirectional mode, generate interrupt requests, and handshake with peripheral equipment.



The Lab-LC costs \$695; the NB-TIO-10, \$495, and the NB-DIO-96, \$355. All are available immediately.

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## NEW PRODUCTS

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### UV PEN MAKES POSSIBLE LOW-COST PHOTO-PLOTTER

By swapping the standard pen of a standard X-Y plotter with an ultraviolet (UV) light source, Mega Electronics Ltd. reckons that it can sidestep some of the time-consuming photographic processes involved in translating output from CAD software for pc boards and the like into photoresist masks. The standard route to etching masks is to plot pc-board layouts oversize on paper as camera-ready artwork, then photographically reduce them to final size on UV-sensitive film.

Mega's Photoplot consists of a high-intensity UV-light generator that transmits a fine beam of light through a 1.3-m length of optical fiber to a light pen mounted on the plotter. Light to the pen is controlled automatically by a shutter as it's raised and lowered over the plotter bed. In that way, pc-board track patterns can be written at final size directly onto UV-sensitive film.

The company stresses that the system can be operated in normal ambient light and requires no modification to existing computer or plotter hardware or software. Two light-pen styles are available to produce minimum track widths of 0.2 or 0.35 mm. Mega also offers a film-processing kit with 50 sheets of A3-sized UV-sensitive film, developer and fixer, processing trays, dryer, and other accessories.

Factory price of the Photoplot is £1,698.00 for the 0.2-mm-resolution system, and £1,495.00 for the 0.35-mm system.

*Mega Electronic Ltd., Mega House, Grip Industrial Estate, Linton, Cambridge, CB1 6NR, United Kingdom. Telephone +44 (0)223 893900.* **CIRCLE 576**

■ PETER FLETCHER

### TAKE 50-MHZ SYSTEM ON THE ROAD

Now 50-MHz computing has become portable. The PAC 486-50E combines a 50-MHz 486 processor with 32-bit EISA architecture to maximize performance. The system has 128 kbytes of external RAM cache and 1 Mbyte of dedicated memory attached to



disk I/O. These features permit the machine to achieve 21.5 MIPS. Although the 486-50E is a portable system, it maintains some of the expandability found in desktop computers. There are three full-size EISA expansion slots with bus-mastering capability. In addition, an optional expansion chassis, the Back-PAC, offers three more full-size ISA slots, as well as a 200-W power supply and a cooling fan. Hard-disk drives afford storage of 40 to 420 Mbytes. Up to 32 Mbytes of system RAM is available. Users can choose between two VGA-compatible display options. The base price for the 486-50E is \$16,995.

*Dolch Computer Systems, 372 Turquoise St., Milpitas, CA 95035; (408) 957-6575.* **CIRCLE 577**

# Local Bus Graphics Solutions

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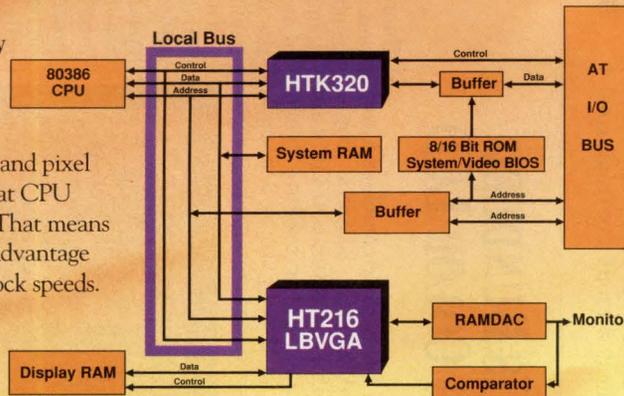
## Local Bus CPU Implementation— The Bus of the Future

The standard VGA controller is limited by the 8MHz ISA Bus bottleneck. The HT216's CPU local bus allows commands and pixel data to be transferred at CPU speeds up to 33MHz. That means the HT216 takes full advantage of fast 386 and 486 clock speeds. The result—greatly improved performance without the high cost of a graphics co-processor.

## Optimizes Windows™ Performance

The HT216 features a 32-bit system address bus interface, and an independent dot and memory clock, which permit the processing of

asynchronous events. By placing the VGA graphics controller on the CPU local bus and incorporating Windows raster operations functions, the HT216 displays Windows applications two to four times faster than standard VGA controllers—at very little added cost.



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## Core Logic that Supports Local Bus

Headland also offers a family of 386SX/DX core logic products that supports the local bus HT216.

The HTK320 supports the 386DX at system frequencies of up to 40MHz and supports local bus peripherals, including the HT216. The HT15 runs at zero wait states with the 386SX to

## Catch the Bus of the Future

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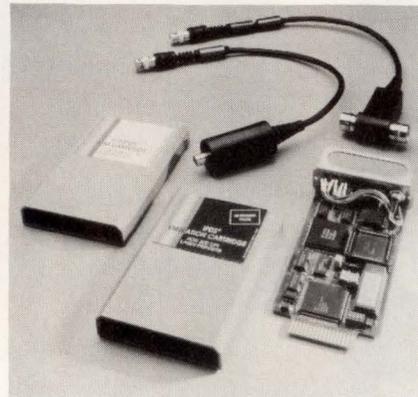
## NEW PRODUCTS

COMPUTERS & PERIPHERALS

### KIT CONNECTS HP LASERJET To IBM MAINFRAME

**A** Hewlett-Packard LaserJet printer can be connected to an IBM mainframe or midrange computer using the Blue Kit, from MPI Technologies. The kit is a coax-twinax IPDS (intelligent printer data stream) emulation package that supplies the compatibility. IPDS is the host-to-printer page-description protocol for advanced printing systems operating under IBM's Systems Application Architecture (SAA) interconnection standards. The Blue Kit is compatible with the HP LaserJet Series IID, IIP, III, and IIID printers.

The kit consists of a coax-twinax interface board and an IPDS emulation cartridge. The board is inserted into the printer's I/O slot and the cartridge is plugged into the printer's left cartridge slot. Then the cable is connected to the mainframe computer. After connection, the printer can be used in three modes: PCL mode by a PC, IPDS mode by the IBM mainframe or midrange computer, or by an IBM mainframe in non-IPDS mode. The printer can automatically switch between the PC and the IBM host without any front-panel



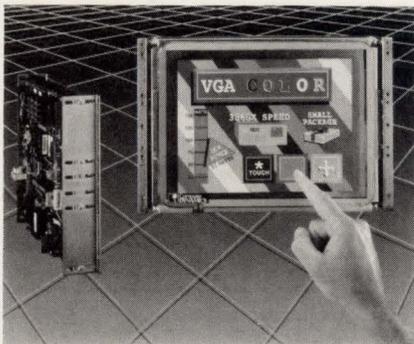
intervention. This is accomplished by recognizing the incoming data traffic and time-out values. By installing a RAM upgrade into the printer, the Blue Kit can quickly complete time-consuming jobs such as vector graphics and raster images. The kit sells for \$2600. It comes with a one-year warranty.

**MPI Technologies Inc., 4952  
Warner Ave., Suite 301, Hunting-  
ton Beach, CA 92649; (714) 840-  
8077. CIRCLE 578**

■ RICHARD NASS

### SBC IS BUNDLED WITH COLOR LCD

**T**he DisplayPac combines a rugged 20-MHz 80386SX single-board computer, a 10.4-in. color LCD display, and a resistive touchscreen in an 11.5- by 8.5 by 2-in. package. The system is suitable for embed-



ded applications because of its small size, ruggedness, and low power consumption (31 W).

The thin-film transistor (TFT) display features a built-in, high-intensity

fluorescent backlight for cool operation, even in harsh environments. The display's high speed permits the use of animation and moving displays. A host of applications become available due to the display's high-resolution color capabilities.

The DisplayPac comes with up to 4 Mbytes of DRAM, up to 1.5 Mbytes of EPROM/RAM disk, two serial ports, speaker, printer, and keyboard ports, a real-time clock, hard- and floppy-disk interfaces, and support for a math coprocessor. MS-DOS can be run from the on-board RAM/ROM disk, making a totally diskless system. Expansion modules can be added using the PC bus expansion slots or through the industry-standard iSBX connectors. The base color configuration is priced at \$6174. Monochrome models are available for \$2083.

**Computer Dynamics, 107 S. Main  
St., Greer, SC 29650; (803) 877-  
8700. CIRCLE 579**

■ RICHARD NASS

## LAN TOOLS IMPROVE SPEED AND RELIABILITY

In a spate of networking introductions, 3Com has come up with high-performance desktop wiring hub—LinkBuilder 3GH—that gives users access to individual 10-Mbit/s Ethernet links as well as to 100-Mbit/s FDDI channels. For bridge and router solutions, the company also released Netbuilder II, a compact bridge/router that adds FDDI to the bridging options.

LinkBuilder 3GH employs a multi-processing architecture based on RISC processors as well as fault-tolerant design to ensure maximum network up time. The main components of LinkBuilder include Ethernet, token ring, and FDDI on the system backplane, and slots for 12 different modules. Up to 10 buses can be supported inside the chassis—3 Ethernet, 3 FDDI, 3 token ring, and 1 VME. Each of the modules for the private Ethernet LANs supports up to eight ports. In the modules, a RISC processor from AMD's 29000 family exercises control. (The NetBuilder also uses the 29000 on its base unit.) For overall system control, the system board uses a Motorola-family 68030 CPU. Features such as hot swapping allow users to change modules without turning off the power to the network, and a hot-standby feature permits redundant system managers to take over if the primary controller should fail. For maximum up time, a redundant 1000-W power supply is an option.

The resulting performance of the system amounts to filtering rates of over 500,000 packets/s for Ethernet-to-FDDI bridging, and an aggregate throughput of more than 400,000 packets/s. The FDDI backbone connectivity module links directly with a dual ring or to a concentrator—the module self-configures for single or dual attachment. A concentrator module that ties four ports to primary, secondary, or tertiary rings is also available.

An 800-Mbit/s backplane in the NetBuilder II system allows maximum throughput when the system has to support high-speed interfaces such as FDDI and T3. The system comes in either a four or eight-slot chassis, and supports multiprotocol routing with the use of modules for FDDI, Ethernet, and T1/E1 wide-area networks. Future modules will include token ring, T3, and others. Protocol support for bridging includes spanning tree and translation bridging and SRT. For multiprotocol routing the system handles all major protocols, including TCP/IP, (OSPF,

RIP, EGP), OSI (EIS-IS and IS-IS), XNS, IPX, DECNet, AppleTalk, and wide-area network protocols too.

Prices for LinkBuilder 3GH range from \$27,500 to about \$150,000. NetBuilder II prices range from \$10,495 up

to about \$32,695. Both systems will be available late in the fourth quarter.

**3Com Corp., 5400 Bayfront Plaza,  
P. O. Box 58145, Santa Clara, CA  
95052; (408) 764-5000. **CIRCLE 594****

■ DAVE BURSKY

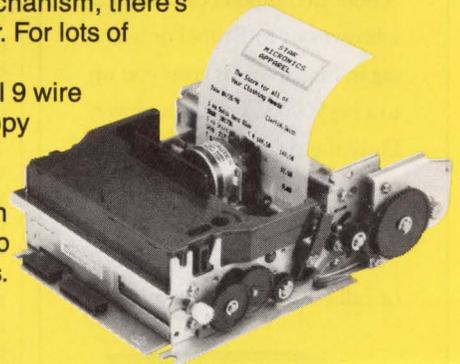
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## NEW PRODUCTS

COMMUNICATIONS

### THREE-CHIP SET SUPPORTS ALL MODEM AND FAX STANDARDS

The Universal Modem Engine from Phylon Inc. is a three-chip solution for supporting all voice-band and fax modem standards, including V.32bis (14,400 bits/s). The chip set consists of the PHY-02 digital-analog interface, the PHY-10 transmit digital signal processor, and the PHY-11 receive DSP. Key to the architecture is the mixed-signal PHY-02 front-end chip. Containing an equal mix of analog and digital circuitry, the PHY-02 includes filters, analog-to-digital converters, and echo-cancellation circuits to maintain good dynamic range and low distortion. An automatic network-balancing feature gives a signal-to-noise ratio of 10 to 15 dB.

Maximum dynamic range is ensured by fully differential circuits and auto-calibrating converters. Additional functions include a speaker drive, a pair of 8-bit DACs for observing the

eye-pattern, a common-mode reference generator, and a resistance-to-digital converter for measuring the value of the programming resistor in the phone jack of programmable-mode installations.

The PHY-10 digital-signal processor (DSP) handles transmission while the PHY-11 DSP controls data reception. These chips accept 40 simple commands from the modem host microprocessor for controlling functions ranging from modulation selection to data I/O. The DSPs also control protocol negotiation with other modems and provide diagnostics such as analog and digital loopback testing. The chip set is available now for \$65 per set in quantities of 10,000. A module configuration costs \$90 in the same quantities.

*Phylon, Inc., 4027 Clipper Ct., Fremont, CA 94538; (415) 656-2606.*

**CIRCLE 596**  
MILT LEONARD

### NETWORK CHIPS IMPLEMENT ETHERNET AND TOKEN RING

For use in PCs and LAN adapter cards, the ChipsLAN two-chip set from Chips and Technologies Inc. handles both Ethernet (IEEE 802.3) and token-ring (IEEE 802.5) network protocols. Connecting directly to an 80386SX or -DX local bus, the 82C581 LAN controller operates as a bus master while transferring data between host memory and the network. The 82C581 supplies statistics for network management and supports software-programmable changes in protocol type and speeds, or I/O and memory base-address locations.

The controller interfaces with the network media through the 82C585 serial interface chip, which has an attachment unit interface for 10Base5 and 10Base2, and a transceiver for 10BaseT Ethernet. It also supports token ring on shielded or unshielded twisted-pair cables. Manchester encoding/decoding functions and constant-gain phase-locked loop (PLL) circuits supply the decoding and recovery of clock and data for receiving and encoding for transmitting.

A third chip, the 82C576, interfaces the ChipsLAN to a Micro Channel bus. The 82C581 comes in a 208-pin plastic

quad flatpack (PQFP), the 82C585 is in a 64-pin PQFP or a 68-pin plastic leaded chip carrier. Priced at \$90 in 1000-piece quantities, the ChipsLAN chipset will be sampled in the fourth quarter this year.

*Chips and Technologies, Inc., 3050 Zanker Rd., San Jose, CA 95134; Gavin Bourne, (408) 434-0600.*

**CIRCLE 597**  
MILT LEONARD

### INTEGRATED DEVICE TARGETS GHz JOBS

Intended for spread-spectrum receivers, cordless and cellular telephones, and pagers working at radio frequencies of up to 1 GHz, the SL6442 integrated radio front-end chip contains a low-noise amplifier with automatic gain control. The chip operates from a single 5-V supply, requires 4 mA of current during operation, and powers down to less than 7  $\mu$ A in the standby mode. It's housed in a 20-lead SO package and sells for \$16 each in quantities of 100.

*GEC Plessey Semiconductors Ltd., Cheney Manor Swindon Wiltshire, SN2 2QW, United Kingdom; Phone: +44 (0)793 51800*

**CIRCLE 598**

## NEW PRODUCTS

SOFTWARE

### BUILD DATA-ACQUISITION AND ANALYSIS TOOL IN WINDOWS 3.0

Using Snap-Master for Windows 3.0, designers of data-acquisition systems can define custom test instruments that duplicate the proficiency of conventional instruments. The icon-based software takes advantage of the Windows graphical user interface as well as the expanded-memory capabilities.

Snap-Master operates at the maximum speed of the analog-to-digital hardware, up to 400 ksamples/s. It can control sensors, transducers, actuators, and signal conditioners. The tool can also simultaneously handle several data-acquisition cards operating on different types of data, including analog-to-digital plug-in cards, digital bits, counters, or proprietary devices. This can be done at different sample rates with few limitations on how the data is acquired, displayed, analyzed, or stored. Snap-Master can display different data sources on the same screen with zoom or pan capabilities. Plots can be put into a strip-chart

form.

To create a custom test instrument, the user defines the flow of data through the test system with a flow chart. Graphical icons represent each element of the instrument. The icons are connected together with data pipes to route the data flow through the system. Dialogue boxes define the details for each icon, including channel settings. Setup time can be reduced by performing group operations on similar channels, thereby bypassing the need to define settings for each channel. In addition, defaults are supplied if they aren't set by the user.

Hardware requirements include an IBM-compatible PC, 2 Mbytes of system memory (4 Mbytes recommended), EGA, VGA, AT&T, or Hercules graphics, MS-DOS 3.0 or higher, and the applicable analog I/O hardware. A math coprocessor is recommended. Snap-Master is priced at \$995 and is available now.

**HEM Data Corp., 17336 12 Mile Rd., Suite 200, Southfield, MI 48076; (313) 559-5607. CIRCLE 583**  
■ RICHARD NASS

### REAL-TIME DEBUGGER RUNS IN X-WINDOWS

Offering users an X-windows Motif interface, the LDB debugger for real-time Unix and Posix software supplies both source- and kernel-level debugging. Those levels support debugging of multiple threads and/or multiple processes.

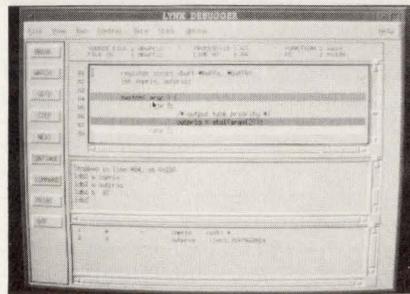
The source-level debugger can pass blocked signals or stop signals to the process being debugged and can generate (or not generate) a message when the signal occurs. The debugger also gives users an unlimited number of breakpoints, all of which are assigned ID numbers. The points can be set to be absolute, always stop, conditional, or stop only if a certain condition is met.

Furthermore, breakpoints can be disabled or deleted according to their ID number. Additional features include watch points and trace points, single stepping, and stack examination.

The software also permits users to search and examine source files, print search directories, examine data or symbol tables, alter code execution,

and construct command subroutines. LDB can also debug a program remotely, using an Ethernet link as the interface to the system.

The initial release of the LDB de-



bugger will support LynxOS, a ROMable real-time Unix. Then, versions of LDB will be released in 1992 to handle standard Unix variants. The current release will be an 80386 AT source-level applications debugger and sells for \$895.

**Lynx Real-Time Systems Inc., 16780 Lark Ave., Los Gatos, CA 95030; Dr. Moses Joseph, (408) 354-7770.**

■ CIRCLE 584

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## GRAPHICAL INTERFACE SPEEDS VERIFICATION

Engineers can speed the process of verifying chip designs with simulation test patterns by using Quickturn's emulation products. These were bundled with the QuickWave graphical interface from TSSI Inc. Initially, QuickWave will be bundled with Quickturn's Rapid Vector Evaluator. QuickWave offers an interactive, graphical environment for managing stimulus and response patterns for ASIC and custom chip design verification. Users create, display, and modify patterns quickly with QuickWave, which accepts patterns in many CAE formats. Rapid Vector Evaluator bundled with QuickWave is available now for \$35,000.

*Quickturn Systems Inc., 325 E. Middlefield Rd., Mountain View, CA 94043; (415) 967-3300. CIRCLE 601*

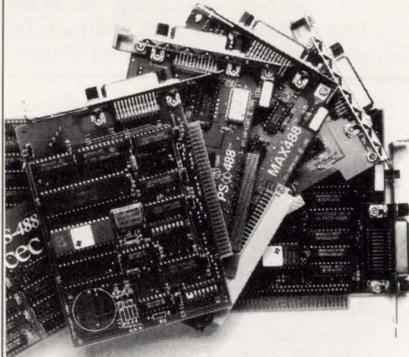
## SOFTWARE HELPS USERS DESIGN FOR QUALITY

Engineers can design products for manufacturing and quality using the Simultaneous Engineering Design System (SEDS) from Pacific Numerix that combines the company's pc-board analysis tools into one system. SEDS provides software for thermal, vibration, fatigue, soldering, and transmission-line analysis. In addition, this analysis can take place before the board is routed. The company claims that when products are run through the system, they can pass through manufacturing easier and be of higher quality. SEDS runs on all Unix workstations that use the X-Windows and Motif standards. Pricing starts at \$20,000 for a stand-alone system and \$30,000 for a network version.

*Pacific Numerix, 1200 Prospect St., Suite 300, La Jolla, CA 92037; (619) 587-0500. CIRCLE 602*

## AUTOPLACER TOOL USES INTELLIGENT ALGORITHMS

The MaxPlace interactive autoplacement program runs on DOS, Unix, and Apple operating systems. Many of the tool's features are built with intelligent algorithms created to satisfy requests from CAD designers. For instance, MaxPlace calculates the available board space automatically and places components in order of their importance and priority as desired by the designer. In addition, the parts are placed in the most optimum routing position.



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Component Cluster technology is also included. It's the same rule-based procedure designers use when they look at a schematic and mentally take note of which components should be grouped together or next to a particular component. MaxPlace is shipping now. The DOS version costs about \$4500. Contact the company for Unix and Macintosh pricing.

*Massteck Ltd., P.O. Box 1130, 95 Russell St., Littleton, MA 01460; (508) 486-0197. CIRCLE 603*

## PROTOTYPING PROGRAM AIDS CFI COMPLIANCE

Object Design now has a CAD Framework Initiative (CFI) Prototyping Program for its object-oriented database-management system called ObjectStore. The company provides program participants with a complete package of services, ObjectStore Design Representation Programming Interface

(DRPI) source code, and a trial license for an ObjectStore Software Developers Tool Kit used for Unix workstations. DRPI is a procedural interface guideline proposed by the CFI to give users a means of exchanging design information among point tools with a CAD framework. The Prototyping Program, including initial consulting and training, costs \$4995.

*Object Design Inc., One New England Executive Park, Burlington, MA 01803; (617) 270-9797. CIRCLE 604*

## CREATE COMPLEX CAD FOOTPRINTS IN SECONDS

The CAD Manager is a CAD compiler from Expert Views Inc. that extracts package-dimension information from the company's centralized database and generates CAD footprints that meet layout, documentation, and manufacturing standards. Even a complicated footprint, requiring hours to create by hand, can be generated in seconds using CAD Manager and exported into a pc-board design system. CAD Manager compiles the footprint graphics into IGES, the standard for transferring information between CAD systems. CAD Manager, which runs on Unix workstations, is shipping now. It operates as part of the company's Component Information System.

*Expert Views Inc., 100 Fifth Ave., Waltham, MA 02154; (617) 890-0333.*

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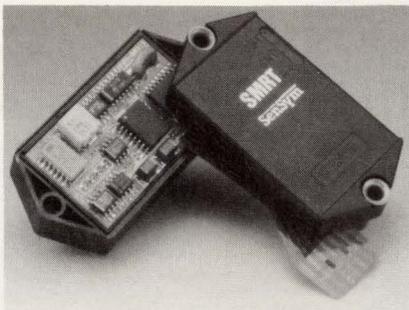
## NEW PRODUCTS

COMPONENTS

### PRESSURE SENSORS DELIVER DIGITALLY CALIBRATED OUTPUTS

**F**ive pressure sensors from SenSym Inc. deliver digitally calibrated digital outputs for absolute, differential, and gage-pressure measurements. These range from 0-1 psi to 0-100 psi with a resolution of 1:10,000. Based on a semiconductor sensing element, the SMRT series sensors use a RISC microprocessor with on-board EPROM to perform linear interpolation for error correction over pressure and temperature ranges. Maximum error is 0.5% of full scale over temperatures from -20°C to +85°C. Long-term stability is better than 0.1% full-scale, and response time is under 80 ms maximum.

For use with noncorrosive fluids and gases, the SMRT series sensors deliver a synchronous, serial digital output for direct interface to microprocessor-based systems. Output signals are in a 16-bit, signed-binary, two's comple-



ment format. Operating from a 5-V power supply, the sensors are packaged in a thermoplastic housing with a standard single in-line package connector and barbed ports for plastic hose hook-up. SMRT sensors are available now at prices starting from \$115 each in 100-piece quantities.

An evaluation kit for the sensors, which supplies RS-232 and LCD outputs, plus all the necessary signal-con-

ditioning circuitry, costs \$385 apiece in single quantities.

*SenSym, Inc., 1244 Reamwood Ave., Sunnyvale, CA 94089; (408) 744-1500. CIRCLE 589*

■ MILT LEONARD

### ACTUATORS PRECISELY CONTROL FLOWS

Extremely precise, high-speed flow control of gases and liquids is the forte of the ASB series of ceramic actuators. The multilayer piezoelectric actuators are hermetically sealed in a metal case for use underwater or in oil. Thanks to the actuators' conversion of electrical energy into mechanical movement, users can control movement into the micron range. Six products are offered in surface- and pad-mounting types. Prices range from \$450 to \$790 each, depending on package, displacement variation, and quantity. Delivery is in from 8 to 10 weeks.

*NEC Electronics Inc., 401 Ellis St., P.O. Box 7241, Mountain View, CA 94039; (415) 960-6000. CIRCLE 590*

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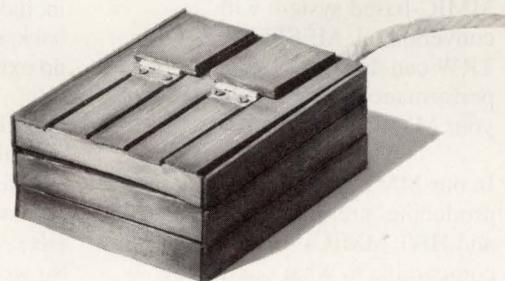
For almost as many years, the Penton Press Division has been recycling scrap paper, obsolete inventory, and printing press waste materials. In 1991, Penton Press will recycle some 5500 tons of paper, 9 tons of aluminum plates, and 3 tons of scrap film negatives. Furthermore, the Press Division has invested \$500,000 in air pollution control equipment.

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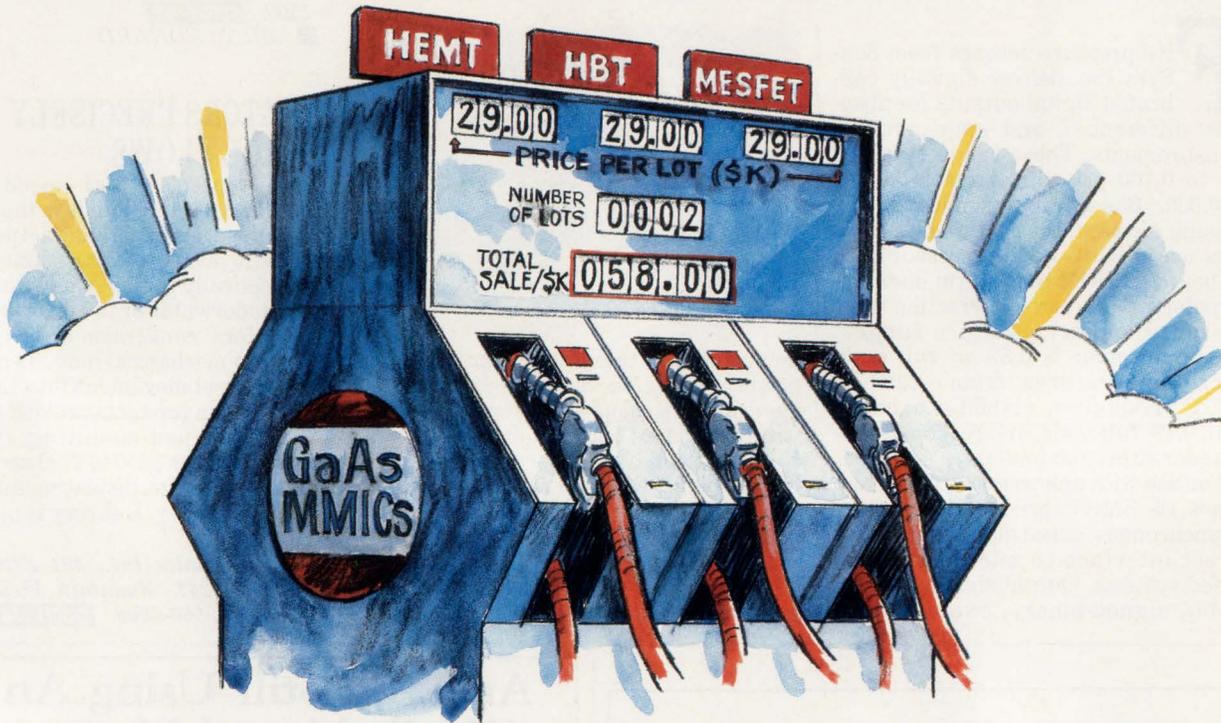
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# RISC-BASED CONTROLLER HANDLES WINDOWS WITH EASE

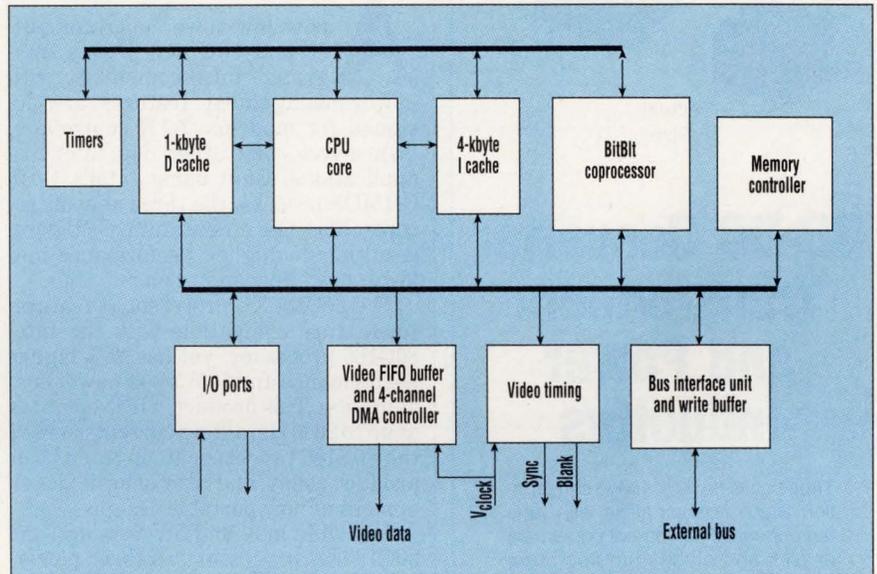
DAVE BURSKY

**T**aking aim at X-window terminals and other graphics-based applications, the LR33020 "self-embedding" controller from LSI Logic simplifies the design of high-performance video systems. Employing a modified version of the MIPS R3000 RISC processor CPU at its core, the 33020 adds to that processor 4 kbytes of direct-mapped instruction cache and 1 kbyte of data cache (also direct-mapped), support of interleaved DRAM and video RAM, automatic wait-state generators, a 1-word-deep write buffer, two PS/2-style serial interface (for a keyboard and mouse), and two 24-bit general-purpose timer/counters and one 12-bit DRAM refresh timer.

To support the video and graphics applications, designers also added a dedicated bit block transfer (BitBLT) coprocessor, flexible video timing generation, a video data FIFO register for speed matching with a DRAM-based frame buffer, and four DMA channels for pixel-move operations and display refresh.

With its on-board caches and graphics hardware, the chip can drastically reduce the system chip count for X-window terminals, laser-printer controllers, and other imaging hardware. That overall reduction in chip count reduces system power consumption and size. Since the processor is also software compatible with the MIPS family, software written for R3000 or R2000 CPUs can easily be migrated to the 33020.

The BitBLT unit on the chip is implemented as coprocessor 2 on the MIPS coprocessor interface that is part of the R3000 core. Existing R3000 instructions—MTC2, MFC2, SWC2, and LWC2—are used for loading and reading the coprocessor registers. Source-to-destination data moves with bit alignment can be done with the coprocessor, and within the block is a 16-function logical unit that performs Boolean operations on the image data. Pixel depths



can be as small as 1 bit and increase in powers of 2 up to 32 bits. For efficient control of font bit maps, the coprocessor also includes a color expansion capability and hardware support for bit-map transparency. Two of the chip's DMA channels control the pixel movements during BitBLTs.

The video timing block on the chip generates the Hsync, Vsync, and Blank signals and generates the timing from a video-clock input that can be asynchronous to the CPU's system clock input. So that page printers can also be implemented by the LR 33020, the Vsync signal can be programmed to deliver a bidirectional output to rapidly draw the scan line. Interrupts can be generated either after each scan line or on a single scan line.

An on-chip 32-word-by-32-bit FIFO register and video shifter allows the chip to employ lower cost DRAMs rather than the higher performance and more expensive VRAMs. Thanks to the buffer, high-resolution monochrome and medium-resolution color displays or laser printers can employ the controller with DRAMs to trim system costs. One of the two remaining DMA controllers on the chip is used to minimize CPU

and bus overheads by performing the block transfer of refresh data from the DRAM; however, the controller can also support VRAMs to implement the highest resolution or more bits per pixel. The serial video output can contain 1, 2, 4, or 8 bits for each video clock period. Furthermore, when VRAM is used, the FIFO buffer can store hardware cursor data and, as a result, enhance cursor performance.

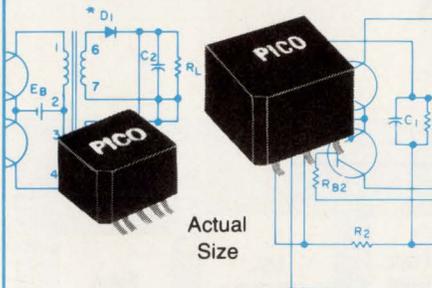
Since the controller chip is trying to lower system cost, it can boot up from either 8- or 32-bit memories. On-chip logic does the byte gathering with a single 8-bit-wide memory employed for system booting.

The 25- and 33-MHz versions of the LR33020 come in either a 208-lead metal quad-sided flat package or a 224-lead ceramic pin-gird array. A 40-MHz version will also be available in the PGA option. In lots of 1000, the 25-MHz MQFP-housed LR33020 graphics controller sells for \$129 apiece. Samples will be available late this quarter, with product quantities at the end of the first quarter of 1992. Military-qualified parts will be available in late 1992.

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The 80C186XL processor is feature-for-feature compatible with the Intel 80C186 processor, yet has 25% higher performance and 50% lower power consumption. This product, which operates at up to 20 MHz, allows current users of the 80C186 processor to upgrade their product easily and also affords development of new portable designs.

Available in 3- and 5-V versions, the 80C186EA processor has three power-management modes—idle, which freezes the CPU clock while keeping peripherals active; powerdown, which freezes all internal clocks; and power-save, which uses a programmable in-

ternal clock divided to allow processes to occur at a slower rate. Applications using the 3-V processor (designated 80L186EA) can run on two AA batteries with an 80% reduction in power vs. a standard 80C186 processor.

Also available with idle, powerdown, and powersave, the 80C186EA microprocessor has four direct memory access (DMA) channels, two interrupt controllers, 22 input/output pins, and four timers, besides standard 186 processor peripherals.

Two serial channels afford inter-processor communications, diagnostics, and interfacing with modems; two I/O ports make it possible to connect to scanners, LEDs, keypads, and displays. All devices are available now. The 80C186XL, the 80C186EA, and 80L186EA are priced at \$11.80 each; and the 80C186EC is \$17.70 each, all in lots of 1000.

Intel Corp., Literature Packet LP-89, P. O. Box 7641, Mt. Prospect, IL 60056-7641; (800) 468-8118.

CIRCLE 581

■ JON CAMPBELL

## DATA COMPRESSION IC RUNS FAST, HANDLES MULTITASKING

**B**y upping the clock frequency to 50 MHz and enhancing the on-chip logic to expand the addressing range and handle multitasking operations, Stac Electronics has created the first data-compression chip that can handle network traffic. It can compress and decompress files that have been packetized and transmitted over networks by multitasking—quickly switching between more than 1500 concurrent full-duplex communication sessions. Such a capability suits the chip for use in LAN cards and in bridges and routers.

The state of the compression chip for each session is stored in an external memory—either 16 Mbytes of DRAM or 256 kbytes of SRAM (maximum)—and the chip quickly switches between states to keep track of each session. An on-chip DRAM and memory controller handles refresh, addressing, and read and write-strobe generation.

When running at 50 MHz, the 9705 delivers compressed data at rate of 2.5 Mbytes/s. That is about 35% faster

than the previous, non-multitasking versions of the chip. The worst-case average lossless data compression ratio is 2:1 and for best case situations—CAD and image files—the chip can achieve 18:1 results. Such compression rates can drastically improve network transfer speeds without any data loss. In contrast, image files compressed with lossy schemes can't recover content lost by compression. Decompression rates are faster than compression speed: Received files can be delivered at up to 6 Mbytes/s.

The CMOS chip was also intended for use in portable systems, either for networking or for storage applications, and has a low-power standby mode that consumes just 1.5 mW from a 5-V supply. The chip is pin-and-software compatible with the company's 9704 chip and in lots of 50,000 sells for \$24 apiece. Samples are available now.

Stac Electronics, 5993 Avenida Encinas, Carlsbad, CA 92008; Steve Koschmann, (619) 431-7474.

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# 3M Announces Double-Coated Foil Shielding Tape

Copper foil base with electrically-conductive adhesive on both sides for reliable point-to-point grounding.

AUSTIN, Tex. — This new UL Recognized tape has a multitude of uses in electronic design, test, and QC laboratories where good grounding paths are required. Other applications include shielding of PC boards, microwave antennas and display boards; grounding and static charge draining.

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Scotch Brand Foil Shielding Tape #1182 is one in a family of metal foil tapes.

For more information contact a 3M Electrical Specialties Division representative or authorized distributor or call 1-800-233-3636.

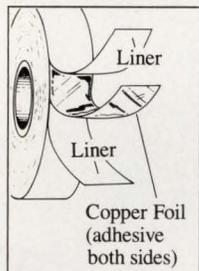
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CIRCLE 80 FOR U.S. RESPONSE

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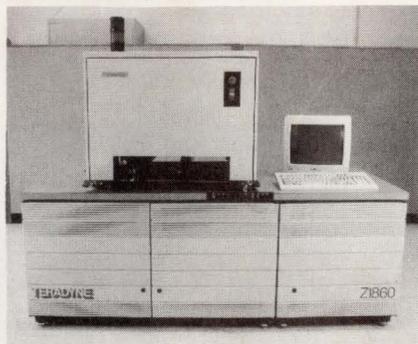


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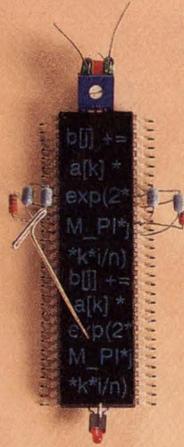
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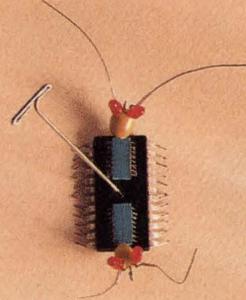
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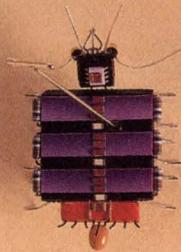
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INCORRECT  
REGISTER  
VALUE



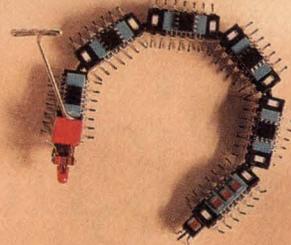
RANDOM  
OUTPUT



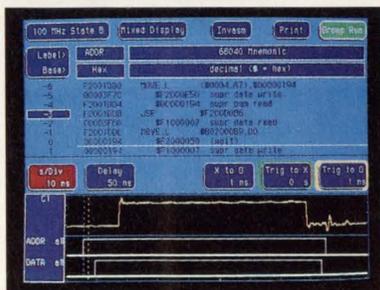
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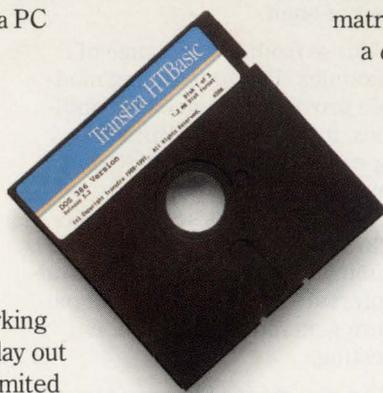
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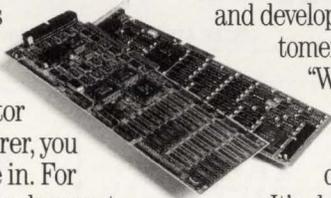
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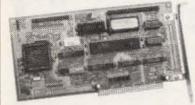
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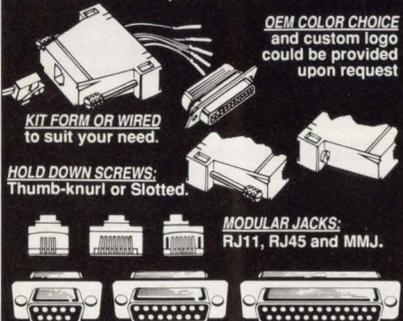
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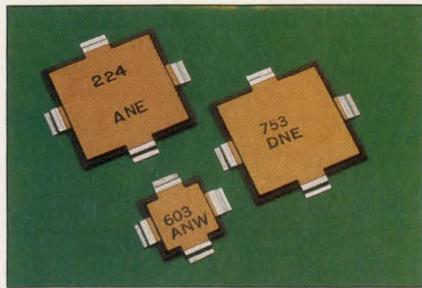
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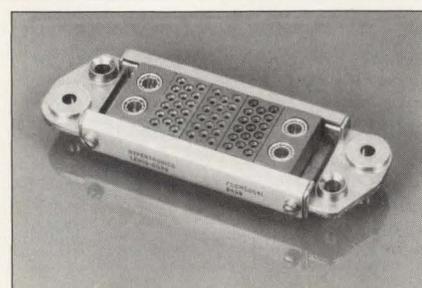
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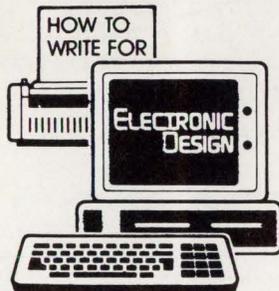
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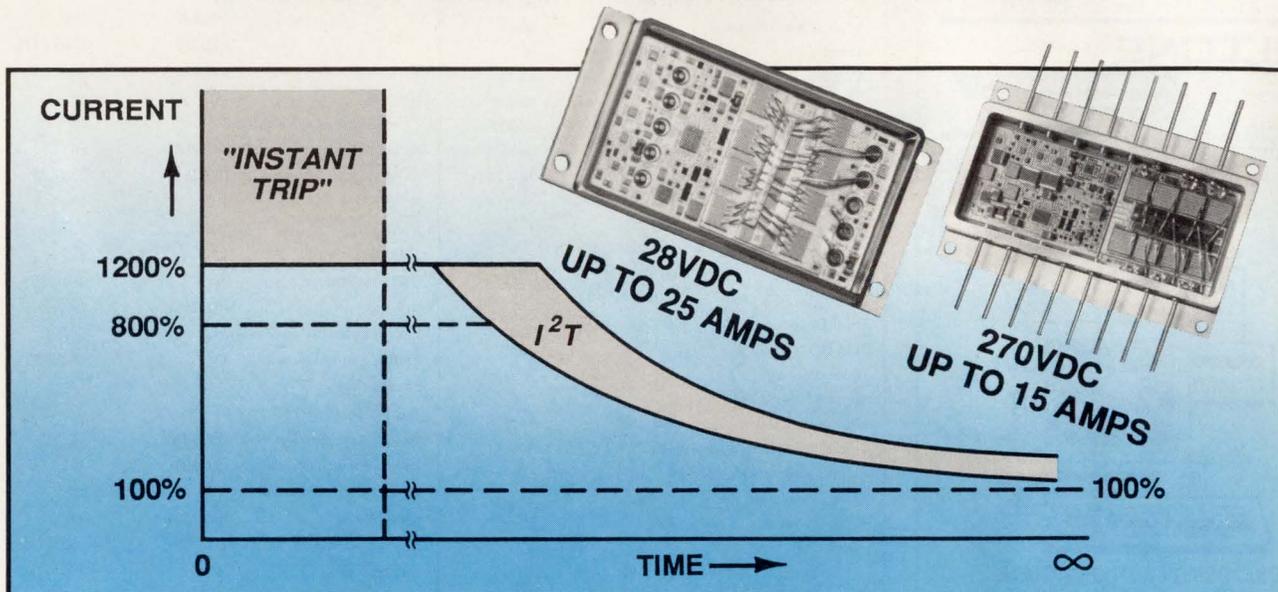
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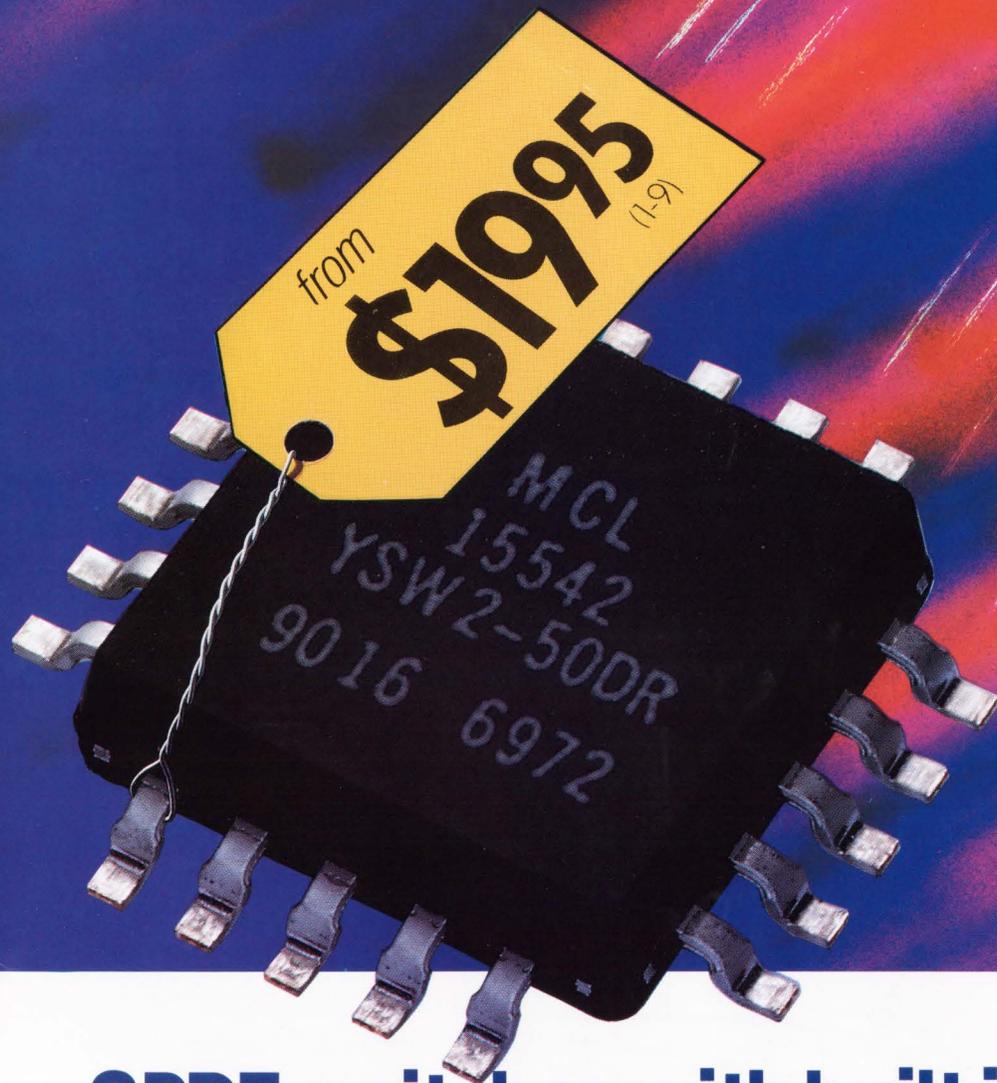
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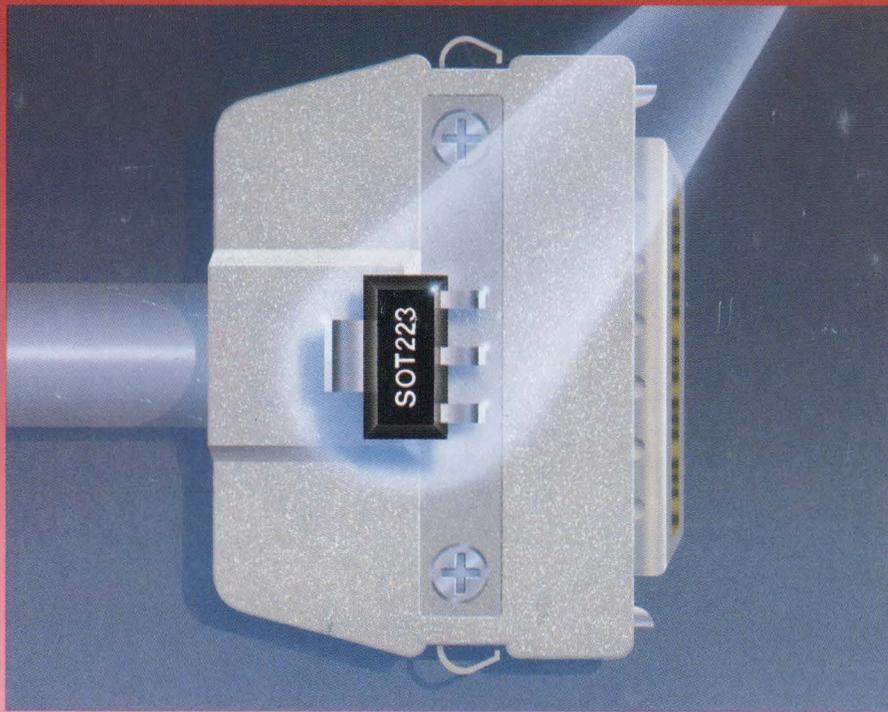
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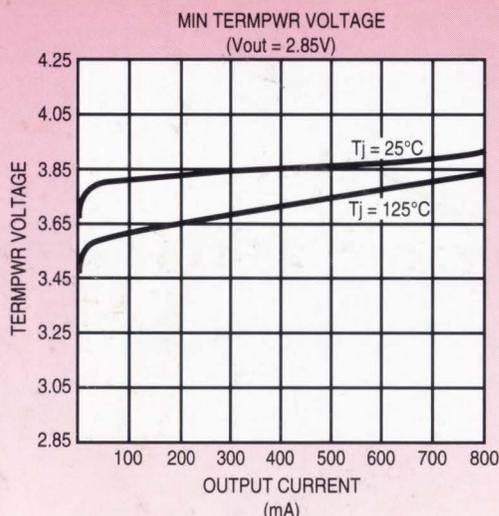
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