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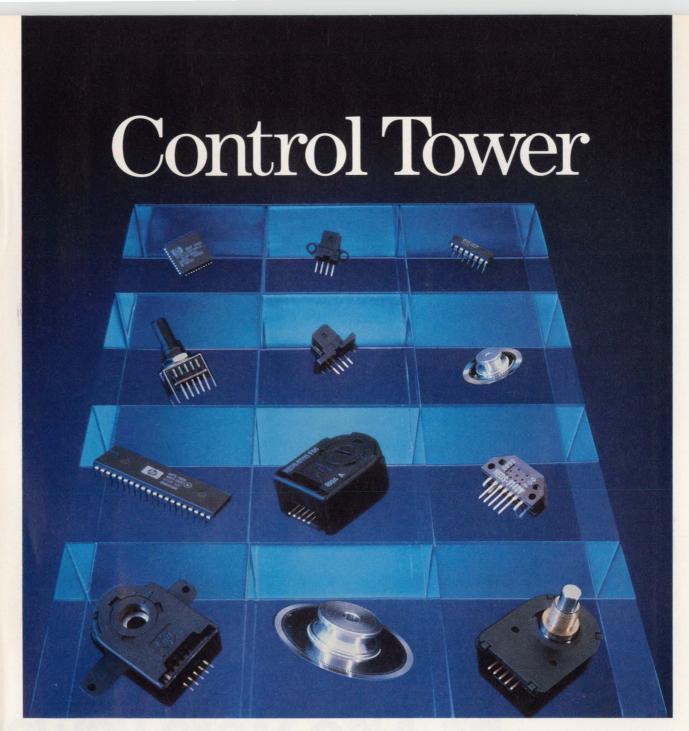
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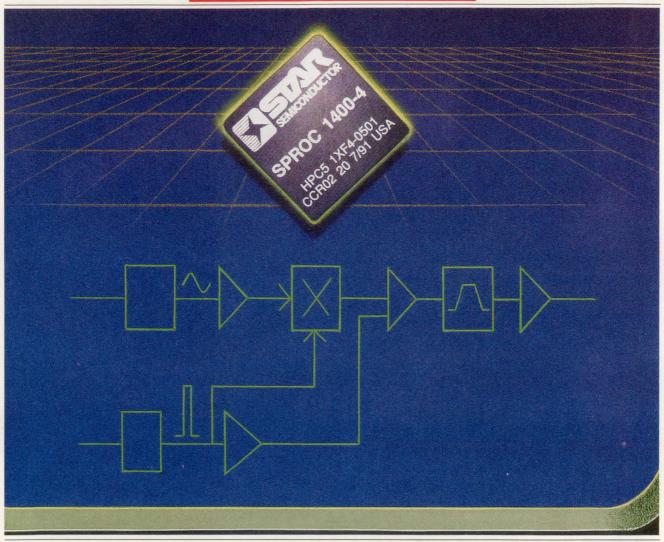


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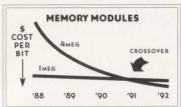
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IN MEMORY MOD CROSSOVER HAS J

You've heard the old saying, "we'll cross that bridge when we come to it." Well, we have.

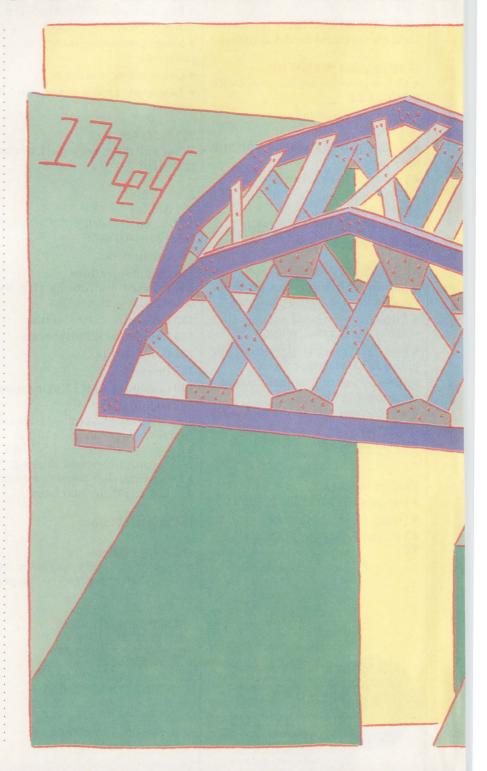
Cost crossover today makes 4-meg DRAMs more economical per bit than 1-meg DRAMs. And given all the benefits in reliability and board real estate, that's good news.



People are lining up to take advantage of it.

One specific advantage is in memory modules. Samsung 4-meg-based modules are actually more cost-effective today than their 1-meg-based counterparts.

All the modules listed here have reliability specs based on 600 temperature cycles (0-125°C) and 500 hours (85°C, 85% RH). Available features include 70, 80, and 100 ns access



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1	KMM591000AN	1M x 9
4	KMM584000A	4M x 8
4	KMM594000A	4M x 9
4	KMM5321000A	1M x 32
4	KMM5331000A	1M x 33
4	KMM5361000A	1M x 36
8	KMM5322000A	2M x 32
8	KMM5332000A	2M x 33
8	KMM5362000A	2M x 36

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Now there's a 100 MHz digital scope that handles just like analog.

Digital oscilloscopes have certain advantages that are hard to overlook. But for troubleshooting, many engineers still prefer analog scopes. Simply because they like the way they handle.

The HP 54600 changes that. It *looks* like a 100 MHz analog scope. All primary functions are controlled directly with dedicated knobs. And it *feels* like one.

The display responds instantly to the slightest control change.

But when it comes to trouble-shooting, the HP 54600's digital performance leaves analog and hybrid scopes in the dust. At millisecond sweep speeds, the display doesn't even flicker. Low-rep-rate signals are easy to see without a hood. It has all the advantages that only a true digital scope can provide. Like storage, high-accuracy, pretrigger viewing, hard copy output, and programming. And since it's one of HP's basic instruments, the HP 54600 gives you

all this performance at a very affordable price. Only \$2,395* for a 2-channel scope; \$2,895* for the 4-channel version.

So, if you need the power of a digital scope, but like the feel of analog, call **1-800-752-0900**. Ask for Ext. 2282,† and find out how well the HP 54600 handles your troubleshooting needs.

There is a better way.



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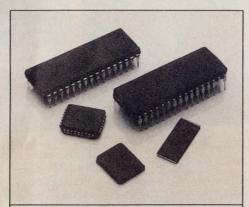
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PAGE 2B



How Fast Is A Flash? A Direct Comparison

Density	AMD	Fastest Competitor				
256K	90ns	120ns				
512K	90ns	120ns				
1 Mbit	90ns	120ns				
2 Mbit	90ns	150ns				

AMD Ships 2 PLCC Flash

SUNNYVALE — The computer industry takes a giant leap forward in performance with the help of the new Flash memory family from Advanced Micro Devices, Inc. Flash memory is a high-density, reprogrammable,non-volatile

technology that has a bright future in computation, laser printers, network and telecommunications hardware. Many military systems use Flash technology in radar and navigational applications.

Flash memory also has the potential to eliminate mechanical hard disks and the need for cumbersome batteries. These are two of the biggest and heaviest obstacles in laptop and notebook

computer applications.

Today, Flash memory is the most cost effective replacement technology for UV EPROMs and EEPROMs in applications that require in-system programming. Flash memories can literally be reprogrammed in a flash—

Standard, But With A Little More Flash

AMD's Flash memory family effectively etches in silicon the de-facto standard for this burgeoning technology that is compatible with Intel's initial

Because AMD Flash memories are pin-for-pin compatible with the now standard architecture, AMD is positioned as an alternate source for design engineers and purchasing agents

alike.

"Alternate source may be an inadequate term," said Jerry Sanders, chairman and CEO of Advanced Micro Devices. "Given our speed and feature set, our customers think of us as a superior

Indeed, AMD's Flash memory family offers designers significant performance advantages (see chart), with speeds almost twice as fast as the nearest competitor.

Engineer Spontaneously Combusts At Mosting

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Chips And Salsa

A Business Person's Guide To Silicon Valley Restaurants

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MORNING EDITION

ASHES! Megabit, 90ns, Memories

The AMD Flash family offers designers and purchasers many packaging options. Particularly popular is AMD's advanced 2 Megabit, PLCC part. Other packaging options include PDIP, CDIP and LCC in 256K, 512K, 1

PDIP, CDIP and LCC in 256K, 512K, 1
Mbit and 2 Mbit capacities. TSOP
packages will be available in the second
half of this year. (LCC not currently
available in 2 Mbit.)
AMD's 2 Mbit Flash memories
come complete with embedded program
and erase algorithms on board. These
automatic algorithms speed upthe design
process and considerably shorten time
to market. Previously, engineers were
required to develop tedious and timeconsuming algorithms to implement inconsuming algorithms to implement in-system reprogrammability. AMD's automatic algorithms also allow several Flash memories to be written or erased at once, without tying-up the CPU. The system is now free to perform other tasks while these operations are in

progress. AMD plans to include embedded algorithms in a future release of its 1 Mbit part.

The Ultra-Violet Blues

Flash technology is particularly suited to applications requiring surted to applications requiring reprogramming in place, because these devices can be reprogrammed in seconds, and within the system.

To update the code on a UV EPROM, the part must first be removed from the system.

from the system. Once removed, erasure can take up to a full 20 minutes. After reprogramming, the part is then plugged back into the system. The process can result in damage to other components, costly service calls, and headaches. Flash memories, on the other hand,

can be bulk erased in about one to two seconds, without system disassembly. Reprogramming can then be accomplished via floppy disk, overphone lines, or even ISDN

sident To Speak

Stop the presses!

Advanced Micro Devices makes big news again—this time with an enhanced family of Flash memory devices.

That's good news for veteran and new Flash users alike.

Because our Flash devices are pin-for-pin compatible with Intel's existing Flash memory architecture, they establish the de facto industry standard.

Our standards, however, are a bit higher. And so are yours.

That's why our Flash Memory family offers densities, speeds and packaging options that improve performance and save board space. For instance, our advanced 2 Mbit PLCC part with a scant 90 nanosecond delay.

You can also choose from Flash devices in 256K, 512K and 1 Mbit densities. As well as packaging options that fit your design best, including CDIP, PDIP, LCC, TSOP, and PLCC.

And you'll find implementation faster and easier than ever because we've included automatic programming algorithms on all our 2 Mbit devices, and soon on our 1 Mbit parts, too. So you'll spend less time writing code, and take less time getting products to market.

To keep up to date with all the latest and greatest in Flash memory, call AMD today at **1-800-222-9323.** And start making some headlines of your own.



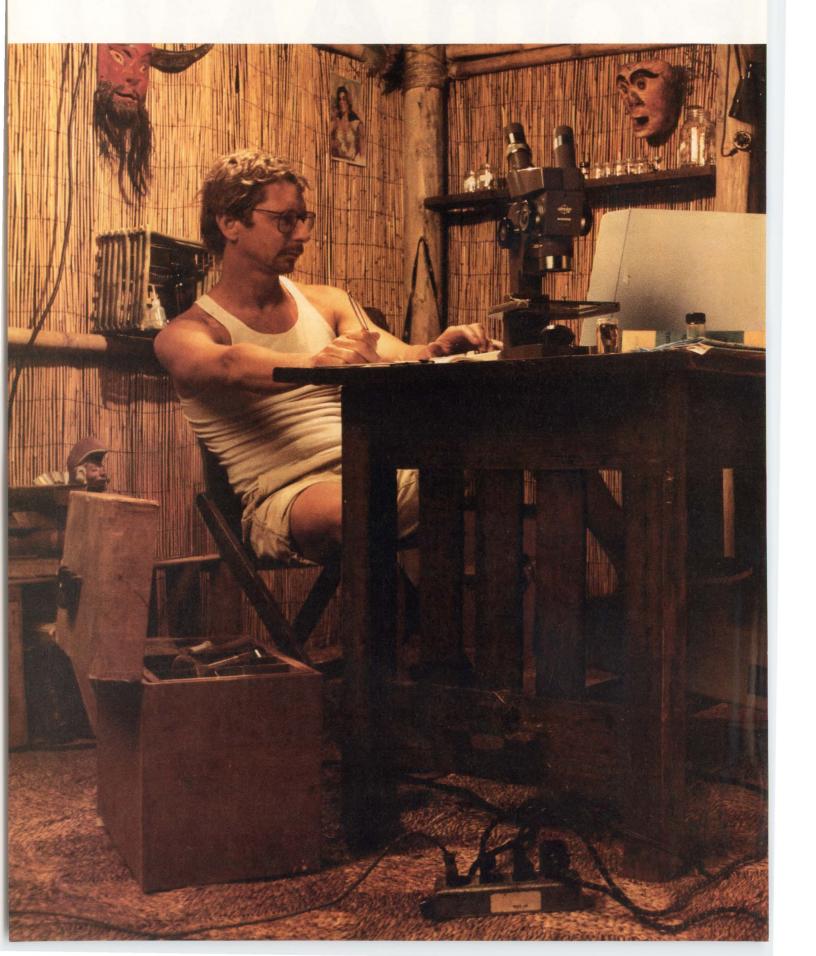
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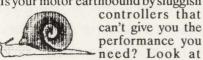
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EDITORIAL

WELCOME TO THE REAL WORLD

f something were in short supply, you would think that people would conserve that resource. Under such circumstances, everyone's efforts should focus on refreshing or recycling the shrinking supply and extending its useful life. These thoughts were brought on by the continuing clamor about an engineering shortage, and the real-world comments that we received from our readers during our annual salary survey (see "Salary Survey," p. 155).

In fact, every time we survey Electronic Design's readers concerning the engineering profession, we come away more convinced that there's something wrong with the ways that electronics industry management and the government deal with one of our most precious resources: engineers—the people who convert scientific phenomena into real-world products.

In particular, the government and electronics industry management must do more to satisfy the educational needs of working engineers. Consider the following readers' quotes gleaned from the article:

"Engineers should be rewarded with salary increases as they improve themselves educationally. Some companies don't."

How can anyone claim there is an engineering shortage if they won't reward those engineers who work to improve their skills?

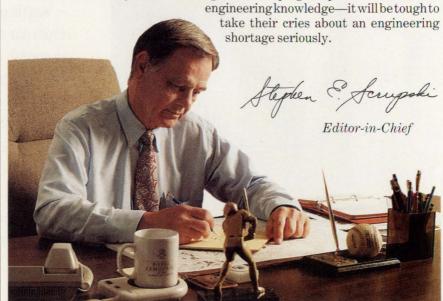
"We have taken a hit in unreimbursed costs compared with managers who don't have the expense of technical skills maintenance."

This quote refers to the recent change in the U.S. tax code, which partly eliminated the deduction for educational expenses. Managers, because of their elevated status within the company, most likely will have the company pay for their management-skills courses. But every day, engineers are on the firing line, facing technology advances they must master if their product designs are to be competitive.

"I want to learn more about shielding noise, but I do not have a current project that will pay for this external course."

This quote refers to the fact that more and more companies want the courses to be project-specific before they reimburse the engineer. Of course, when this engineer does hit a situation where he needs to add some shielding to a circuit, he will be under such time pressure that he won't have the time to take the course to help him solve the problem.

Until the government and electronics industry management wake up and put some effort and money into conserving and developing this precious resource—







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TECHNOLOGY BRIEFING

DATA MANAGEMENT FOR DESIGN GROUPS

he push is on to give project leaders new management tools that will provide them with better control of design groups practicing concurrent engineering. The tools required for today's design-project managers continue to change rapidly as projects get ever more complex, time-to-market windows shrink, and engineers use different EDA tools with different versions of the same data. There's still lots of opportunity, though, to develop new approaches to solve these problems, which show no sign of diminishing in the future.



LISA MALINIAK COMPUTER-AIDED ENGINEERING

Basically, what concurrent-engineering managers need are tools that will let them leverage their existing investment in hardware, tools, and data. Frameworks, for example, aren't

only being developed to combine individual tools, but also to deliver comprehensive analyses of the overall project that will help managers cope with their growing problems. The workgroups need to create, share, update, and distribute information in large volumes over a variety of hardware and operating systems. They must have facilities to track changes to files, and control and manage different configurations of data to support various design alternatives.

Frameworks, however, still have some limitations: tool integration and encapsulation can take anywhere from three to six months or longer. Furthermore, no standard currently exists for tool integration. Consequently, each time there's a new data type, new hardware, or new EDA tool, the entire integration and encapsulation process must be repeated. On top of that, many companies continue to be uneasy about adoption and the long learning curve involved.

Concurrent engineering isn't always easy to implement because it requires the companies that are using it to change the way they operate. Data management is basically the first step toward implementing a concurrent-engineering environment. Moreover, the implementation must cultivate concurrent efforts with as little disruption to the current work flow as possible. Today's concurrent-engineering solution must coexist with prevailing solutions, because companies don't want to lose their investment in processes and internal tools.

For example, one recently developed solution is the TeamNet data-management system from TeamOne Systems Inc., Sunnyvale, Calif. David Hoffman, TeamOne's president, points out that today's design project may be distributed across the country in networked workgroups that must operate concurrently. Communication flows internally between networked groups with different disciplines, such as EDA, publishing, CASE, and MCAD. Managing that data is quite a task, and Hoffman asserts that "frameworks are tomorrow's approach, while TeamNet is the solution today." According to Hoffman, TeamNet works transparently, without modifying or encapsulating existing tools. It accomplishes this by using the common denominator in the tools, platforms, and data: NFS. NFS is Sun Microsystem's Network File System, a de facto standard that's supported on machines ranging from PCs to mainframes. It's the key to TeamOne's approach because with it there's no need for numerous versions of the TeamNet product for many different platforms. TeamNet supports all existing tools and data on a network that support NFS. Another plus is that engineers can take advantage of specialized computers as long as they support NFS. There's no pressure to port to different platforms.

TeamNet is an example of the types of tools that will enable groups to thoroughly exploit concurrent-engineering disciplines. Without such tools, that concept will remain the impossible dream.



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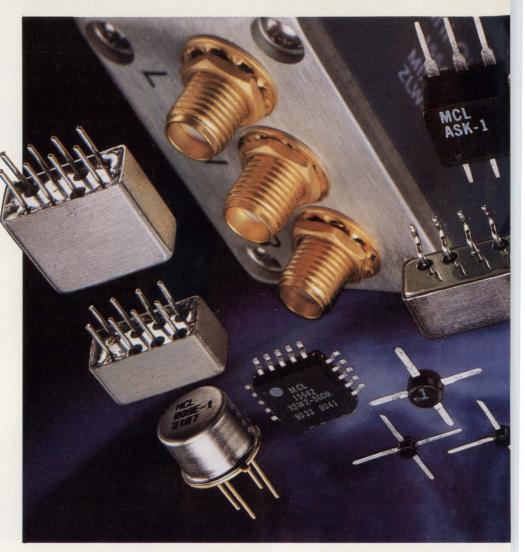
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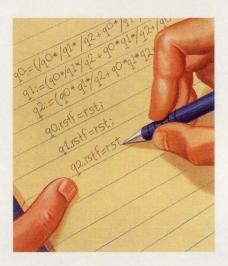


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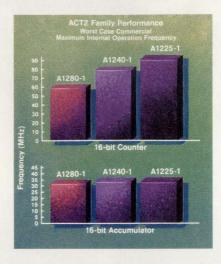
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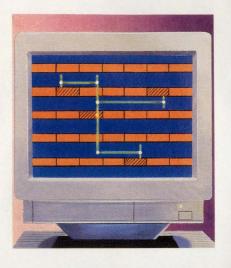
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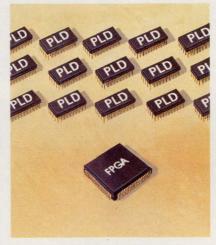
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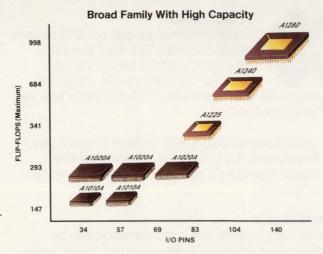
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TECHNOLOGY NEWSLETTER

MEMORY-CARD SELECTION Last month's release of the major upgrade to the Personal Computer Memory Card International Association standard, rev. 2.0, also unleashed a spate GROWS WITH PCMCIA 2.0 of new memory and I/O cards that fit the 68-pin connector slot. One intrigu-

ing newcomer was a family of flash-memory-based memory cards that will be available in capacities of 2.5, 5, 10, and eventually 16 Mbytes during 1992. The cards will function just like disk drives even though they're based on a flash-EEPROM technology developed by SunDisk Corp., Santa Clara, Calif. The company has filed for over a dozen patents covering the optimized flash-EEPROM technology and intelligent controller. Also showing off flash storage, Intel Corp., Santa Clara, Calif., released a 2-Mbyte card that fills the gap between its 1- and 4-Mbyte cards (see related story, p. 149).

BIOS-level software support for both the memory cards as well as the exchangeable card architecture (ExCA) was also unveiled by both Phoenix Technology Ltd., Norwood, Mass., and SystemSoft Corp., Natick, Mass. The Phoenix offering includes PC Card Manager, a BIOSlevel supplement that supports all memory cards, as well as the new I/O cards and the socketservices supplement to the PCMCIA standard. SystemSoft released details of its plans to support the ExCA interface through the memory-card controller chip—the 82365SL—released by Intel along with the flash memory card. That chip reduces board area for the memory-card

support logic to just 2 in.2.

Both Databook Inc., Ithaca, N.Y., and Fujitsu Microelectronics Inc., San Jose, Calif., released design/evaluation kits that designers can quickly set up to run the memory cards through their paces. The Databook kit includes a card "drive" that can read and write data to the memory card, plus a host-interface card and abundant documentation. Fujitsu's "kits" give designers two choices. The first is a low-density kit that packs a 256-kbyte SRAM card, a 512-kbyte EPROM card, and a 1-Mbyte flash-based card. The other choice is a high-density kit incorporating four cards—one that contains 512 kbytes of SRAM, another with 1 Mbyte of EPROM, another with 1 Mbyte of flash storage, and the last with 1 Mbyte of one-time programmable storage. For product details, contact John Reimer at SunDisk (408) 562-0570; Intel at (800) 548-4725; Steve Cox at Phoenix, (408) 452-6540; Jonathan Joseph at SystemSoft, (508) 651-0088; Daniel Sternglass at Databook, (607) 277-4817; and Larry Gagliani at Fujitsu, (408) 922-9000. DB

VIDEO PROCESSOR SUITS East-European market needs have driven Siemens AG, Munich, Germany, to develop a video-processor chip that handles characters and symbols used in SIX LANGUAGES six languages: Czech, Polish, Rumanian, Serbo-Croatian, German, and Swedish. The SDA 5248C2, which its developer calls the "East Europe" chip, recognizes and stores up to 128 pages of video text and can process four pages simultaneously. For use in TV sets to display information broadcasted by the transmitter in the TV signal's blanking intervals, the processor offers 192 alphanumeric characters and 128 graphic symbols. The processor works with the inter integrated-circuit (I2C) bus, which allows direct access to the page memory. There, DRAMs that are either 64k by 4 bits or 256k by 4 bits in size can store 32 or 128 videotext pages. Characters and graphic symbols are displayed in a 12-by-10-dot matrix. Siemens says the SDA 5248C2, available now, helps satisfy East Europe's growing demand for technical features of many TV sets made in West Europe. JG

SOLDER PROCESS A method of regulating the shape, size, and uniformity of solder pads on pc boards promises to significantly reduce board rework after assembly. The MAKES UNIFORM SMT PADS Optipad process, developed by Velie Circuits Inc., Costa Mesa, Calif., is intended to solve a basic problem in pc-board technology: uneven and irregular solder pads. Typically, these pads vary in size and shape. The Optipad process creates pads that are flat and uniform in size, with no runoff into the spaces between conductors. To achieve this, panels are run through the process in a vertical orientation with a solder wave on each side. Temperatureconditioning chambers force the solder to stay in place. The objective, according to the company, is to provide uniform pads at an 8-mil pitch for surface-mounting applications. A secondgeneration process, which would be aimed at chip-on-board technology at very fine pitches, might facilitate reflow attachment of TAB chips and flip chips. Contact Larry Velie at (714) 751-4994. DM

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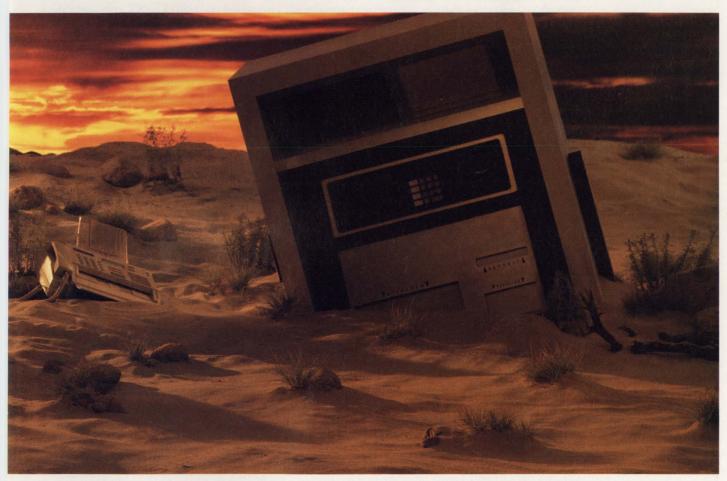
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TECHNOLOGY NEWSLETTER

TINY QUAD FLAT PACKS

To further shrink future generations of computers, system designers must have smaller IC packages. To that end, S-MOS Systems, San Jose, Calif., is introducing a series of quad flat packages (QFPs) and thin small-outline packages (TSOPs) that are half the thickness of current packages. Intended for low-power ASICs and standard ICs, the packages feature extremely small body sizes of, for example, 7 by 7 by 1.4 mm for 48-pin ICs and 14 by 14 by 1.4 mm for 100-pin ICs. The 1.4-mm thickness is roughly half that of standard QFPs at 2.7 mm. Lead pitches for the packages, which are sampling in November, are 0.4 mm. A 1.0-mm-thick version with 32 and 100 pins will be sampled in February and July of 1992, respectively. DM

FASTER X86 FAMILY OF Tightened manufacturing tolerances and minor process adjustments have allowed Intel Corp., Santa Clara, Calif., to optimize speed and power-dissipation characteristics of its popular 386SL, 486DX and 486SX microprocessors

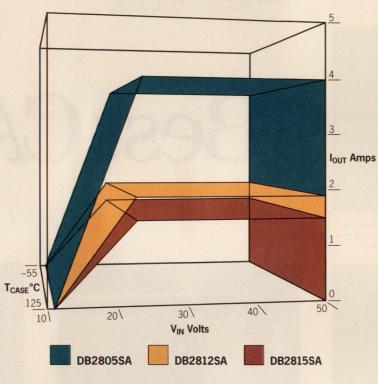
CPUS UP PERFORMANCE allowed Intel Corp., Santa Clara, Calif., to optimize speed and power-dissipation characteristics of its popular 386SL, 486DX and 486SX microprocessors for battery-powered PCs. The 386SL's top clock speed has been increased by 25% to 25 MHz. This latest upgrade gives designers the ability to create no-compromise 386-grade battery-powered systems that match the throughput of most desktop systems. Furthermore, although several adventurous companies have already embedded the 486DX or SX into portable systems, lower-power versions of those CPUs will extend system battery life. The just-released lower-power versions consume just 25 to 50% of the power required by the currently available 486DX and 486SX. The low-power 486DX will come in a 25-MHz speed grade, while the 486SX has three grades—16, 20, and 25 MHz. Samples of all new chips are immediately available. In 1000-unit lots, the 25-MHz 386SL goes for \$189 apiece, while the 25-MHz 486DX and SX sell for \$471 and \$366 each, respectively, in similar quantities. Contact Intel at (800) 548-4725. DB

SUPERSCALAR CPUS MORE Two superscalar RISC processors, one defined by Mips Computer Systems Inc., and the other by Sun Microsystems Inc., both of Mountain View, Calif., promise new peak levels of throughput for workstations, servers, and other

THAN DOUBLE THROUGHPUT promise new peak levels of throughput for workstations, servers, and other performance-critical systems. Although details of the R4000 architecture from Mips were released earlier, the chip is now out of the ovens and ready for sampling from three of its sources—NEC Electronics Inc., Mountain View, and Performance Semiconductor Corp., Sunnyvale, Calif., and LSI Logic Inc., Milpitas, Calif. The Sparc-compatible processor, codenamed Viking by co-developer Texas Instruments Inc., Dallas, has not yet been released. However, sources indicate that TI is already shipping samples of the biCMOS chip to Sun. Both the R4000 and Viking chips will clock at 50 MHz. The R4000 will be able to launch two instructions per clock cycle, while the Viking chip will launch three. Such launch capability coupled with the high clock speeds would theoretically give the chips peak throughputs of 100 to 150 MIPS.

Both chips are highly integrated processors—the Viking chip includes two integer units, the floating-point unit, memory manager, dual 16-kbyte caches, and an Mbus interface, all on a single chip. The all-CMOS R4000, which packs a similar functional integration as the Viking, contains a 64-bit integer unit, a 64-bit floating-point unit, dual 8-kbyte caches, primary and secondary cache-control logic, and a memory-management unit. TI's Viking packs about 3.1 million transistors onto a chip implemented with 0.8- μ m design rules and triple-level metal. The R4000 is less complex, but NEC also uses 0.8- μ m rules to yield a chip almost 13 by 16 mm. When running with an external clock of 50 MHz (100 MHz internal), either processor will consume close to 10 W.

Samples of NEC's V_R4000 will be available in three interface options. A 179-lead PGA version (the 4000PC) uses only the on-chip primary cache (it's targeted at desktop systems). Two 447-pin versions—the 4000SC and MC—can control secondary caches. The SC is aimed at uniprocessor systems, while the MC includes control signals for use in multiprocessor architectures. Price for NEC's SC version will be \$1800 apiece in lots of 10. Both PC and SC versions from Performance Semiconductor and LSI Logic will be available this quarter. They're fabricated with a 0.6- μ m process, and although prices haven't been set, they should be less expensive than NEC's version. Full details of the Viking are expected to be released at next month's Microprocessor Forum at the Hyatt hotel in Burlingame, Calif. Contact Yuichi Kawakami at NEC, (415) 965-6273; Jim Keim at Performance, (408) 734-8200, ext. 214; John Hughes at TI, (713) 274-2000; or Eric Almgren at (408) 433-7343. DB



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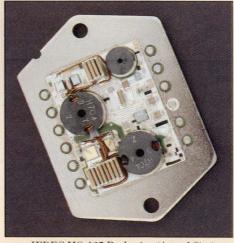
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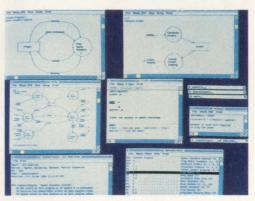
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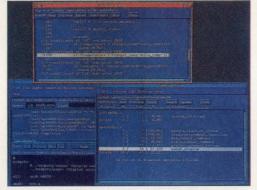
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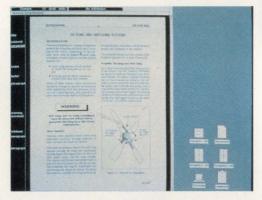
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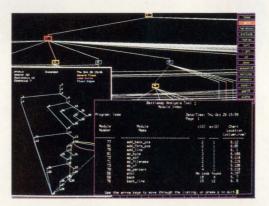
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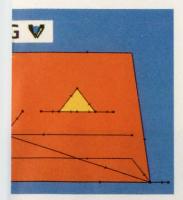


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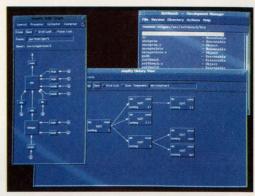


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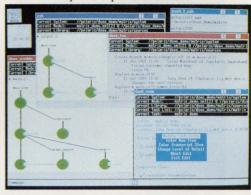


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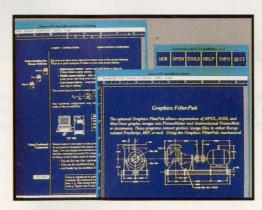
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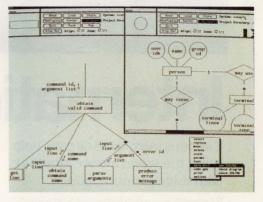
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LIBRARY OF 3D GRAPHICS PROMOTES STANDARDIZATION ACROSS PLATFORMS

multi-company advisory panel is being created by Silicon Graphics Inc., Mountain View, Calif., to guide future enhancements to its Iris graphics library (GL). Iris GL, probably the most popular graphic primitive library in the industry, is employed on Silicon Graphics' 3D graphics workstations. The announcement of an advisory panel comes on the heels of the company's "opening" of the library, which previously had been proprietary, for licensing by any system or software developer that can meet the cost (although Iris GL has been licensed to IBM Corp., and most recently to Microsoft Corp., it wasn't available for general industry use). One objective of the advisory panel is to guide future extensions to the library, thus ensuring that it stays open.

As system users analyze more complex problems on their workstations and high-end PCs, 3D graphics is playing an ever-increasing role in visualizing the resulting data sets or the actual product being conceptualized (see the figure). This role, however, has been somewhat blunted by a lack of 3D-graphics standardization. In the workstation world, for example, there's very little commercial software standardization of underlying graphics primitives used to create the images.

Silicon Graphics' latest move might improve this lack-of-graphics-standards situation by making Iris GL the standard around which most 3D graphics applications can be written.

The library's opening has been endorsed by such

Mips Computer Systems RISC chip set, or on a special graphics card IBM developed for its workstations.

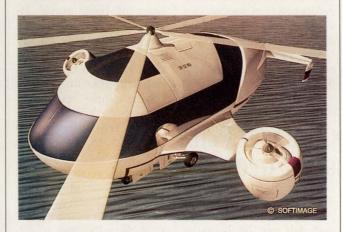
With the opening of the library, DOS-based platforms with graphics coprocessors, possibly based on Intel's i860 superscalar processor, as well as other platforms can take advantage of the library. Micro-

late complex 3D images; perform lighting, shading, and texture mapping of the objects; and implement more-advanced graphics functions, such as motion blur as well as simulated fog or haze.

Based on an immediatemode approach to 3D graphics, Iris GL offers better efficiency than display list approaches because graphic calls are executed directly on the screen. With display lists, an intermediate representation of the object (the display list) is first modified. then the modified version is sent to be rendered and displayed. Iris GL also allows programmers to access low-level control of system features like the Z buffer, so that image rendering can be tuned to its optimum level.

Other standards, including GKS (graphics kernel software) and PHIGS (programmer's hierarchical interface for graphics), have been available in the industry for a decade or more. However, they haven't received universal industry support even though they were made standards by The American National Standards Institute (ANSI). PHIGS, initially developed for the mainframe and terminal environment, employs a display-list approach. Many X-terminal manufacturers and users have adopted PHIGS, and it has even been expanded into PEX (PHIGS extensions to X). But for local high-performance rendering, displaylist approaches are too

Another potentially competing software standard is Renderman, a rendering approach that Pixar



companies as Compag Corp., Houston, Texas, Digital Equipment Corp., Maynard, Mass., Intel Corp., Santa Clara, Calif., and Microsoft Corp., Redmond Wash., all of whom are working on operatingsystem software or hardware that will incorporate hooks into the library. Compag, for instance, will include the library in its advanced computing environment (ACE) Unix platform that's being developed for release in 1992.

Iris GL enables programmers to create software solutions that let users visualize and manipulate color images. The Silicon Graphics library is independent of any specific windowing system or hardware platform.

So far, the library has been implemented either on the hardware-based

soft plans on incorporating key elements in a future version of the NT (new technology) addition of windows.

Over 1400 applications already employ the library, and many potential users would like to see the same applications ported to other platforms they may already have, rather than be "forced" into buying another platform that doesn't run most of their current applications.

The library itself con-

sists of over 440 software calls for creating geometric shapes. Those calls reside in system software and sit between the end-user's application software and the system-specific

graphics hardware in either a PC or a workstation. By employing the calls, programmers can create and interactively manipu-

TECHNOLOGY ADVANCES

Inc. released in 1990. It has garnered some degree of interest for use as a standard, but only a small number of applications are based on it.

There will be three tiers of licensing set up for Iris GL. Level I licenses the GL specification, a suite of tests to evaluate conformance and specification for interfaces that allow Iris GL to interact with various windowing systems. This level also includes the right to create and distribute a product that meets the specifications for Iris GL

Level II includes all of

Level I features plus the source code (referred to as the reference port) for a hardware-independent version of Iris GL. Also included is the source code that allows the software to connect with various windowing systems.

And Level III includes all of the previous levels and the right to distribute source code based on the Iris GL specification and reference port source to a verified Silicon Graphics direct-source licensee.

For more information, contact Bill Glazier at (415) 960-1980.

DAVE BURSKY

main level, but the wings move up and down. Yaw is where the object rotates about its center, such as how a fan blade rotates about its center.

Another 3D input device uses a magnetic field sensor. There are three wirewrapped ferrite cores pointed orthogonally, one in each plane direction, all at 90° angles to each other. Also, a sensor reads the position of these cores. To move the object on the screen, users pick up the device and move it in the desired direction. A second implementation of this "flying mouse" uses radio waves to do the task.

The Ice-Cube never leaves its mouse pad. It uses Mouse Systems' M5 technology, previously used in an earlier product, to get the X, Y, and yaw motions (ELECTRONIC DE-SIGN, May 10, 1990, p. 32). Two optical sensors built into the underside of the mouse track the X, Y, and rotational (yaw) positions. The first sensor tracks its location with respect to the second sensor, thereby determining the three directions.

The Z-direction movement is done by a roller that Mouse Systems calls Zarpa (Z-axis roll-pitch actuator). The roller, which rolls forward or backward to get an up or down (Z) movement, can be tilted to the left or right sides (see the figure, b). This brings about the pitch and roll. If the Zarpa is tilted to the left and rolled, pitch is obtained. If it's tilted to the right and rolled, the roll is obtained. A decision hasn't yet been made as to whether the Zarpa will be an optical or an optomechanical implementation.

The Ice-Cube can also be used in painting and imageprocessing applications. If the device is employed as a traditional mouse, only the X and Y functions are being used. But, keep in mind, the Ice-Cube has four other directional movements that are idle. Therefore, they can be used to control other functions. For example, in a paint program, the roller can be used to intensify or change the shade of a color. The pitch mechanism could change paint brushes or the width of the brush, and so on. Other applications where extra functions could come into play is in computer games. Here, many functions that are now controlled by the keyboard could more easily be controlled by the mouse. In addition, this would make the games more realistic.

The Ice-Cube will be demonstrated at this year's Fall Comdex. Shipments probably won't commence until next April. For more information, call Mouse Systems at (415) 656-1117.

RICHARD NASS

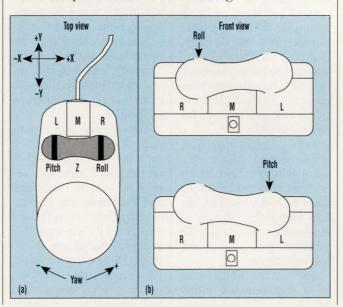
THREE-DIMENSIONAL MOUSE FLIES WITHOUT LEAVING THE GROUND

Devices designed to input data using three dimensions exist, but most are quite costly and are employed only in 3D CAD and modeling applications. Now, a mouse designed by Mouse Systems Corp., Fremont, Calif., can input data in all three planes (X, Y, and Z) and operate as a standard mouse, with a few added wrinkles.

Developed under the internal code name Ice-Cube, it looks like a typical mouse with the exception of a rolling element added to the top (see the figure, a). Mouse Systems claims that their mouse will sell for under \$400, less than half of what competitive 3D input devices cost.

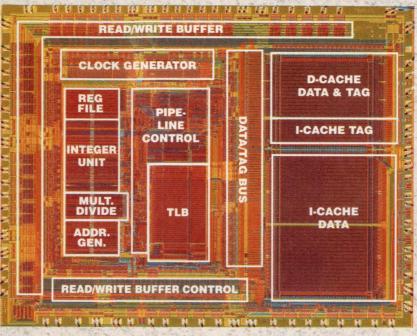
An alternative 3D input device appears as a ball attached to the top of a joystick. Users grab the ball and push, pull, lift, or rotate it as if they were holding on to the object on the screen. Such a device of-

fers six degrees of freedom—X, Y, and Z, plus pitch, yaw, and roll. Pitch and roll can be best described by envisioning an airplane. If the wings are level and the nose of the plane is slightly facing down, the plane has a downward pitch. When there's roll, the nose and tail of the plane would re-



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FAST COMPRESSION ALGORITHM SIMPLIFIES JPEG SILICON

proprietary technology for compressing digital color images reportedly performs up to 500 times faster than other software alternatives and occupies considerably less space in silicon implementations. Developed at the California Research Center of Ricoh Corp., W. Caldwell, N.J., the new patented algorithm is based on the Generalized Chen Transform (GCT), which is a variant of the JPEG standard's discrete-cosine transform (DCT). The DCT requires about 150 multiplications to transform an 8-by-8 block of pixels into a two-dimensional wave. On the other hand, the GCT requires just 64 such opera-

tions, including the transformation and quantization steps specified by the international JPEG standard. This means quantization needs just one multiplication operation per point, which occurs at the back end of the transform. The remaining transform portion of the image-compression process is done with add and shift operations. These operations can be executed simpler and faster by a computer.

The algorithm delivers compression ratios ranging from 2:1 to 100:1. In a demonstration at the Ricoh's Research Center in Menlo Park, Calif., GCT software running on an Apple Computer Macintosh IIfx using a 40-MHz

68030 processor reduced typical 512-by-512-by-24bit full-color images to 30 kbytes in about 1.75 seconds. This performance represents a 25:1 compression ratio and a compression speed of about 200 kbytes/s. For 512-by-512by-24-bit color images, decompression time is also about 1.75 seconds, including color-space conversion, GCT transformation. quantization, and Huffman encoding. Disk access time, compressed-file save time, or painting of a window aren't included. Using a 68040-based machine, estimated compression and decompression times for the same image is 600 ms.

Ricoh says the GCT offers competitive advan-

tages in either software or hardware designs. When implemented in silicon chips, the GCT replaces complex multiplier structures with adder circuits. It also eliminates the control logic, lookup tables. RAMs, and ROMs used in other JPEG chip designs. Ricoh says the GCT technology is equally applicable to MPEG and Px64 standards. Applications are expected to span a broad range of office and consumer products that process full-color images.

Ricoh is currently seeking to license the technology to software and IC hardware developers. Contact Edward W. Onstead at (408) 281-1436 or (415) 496-5719.

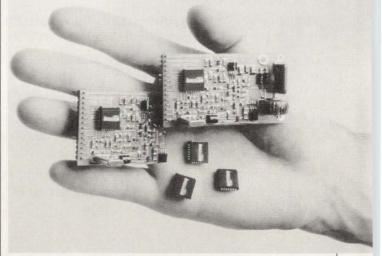
MILTLEONARD

SPREAD-SPECTRUM SIGNALS COMMUNICATE OVER POWER LINES

n a local distributedcontrol network, using ac power lines to transport control and data signals is an attractive concept for implementing "intelligent buildings," because it avoids the cost of installing a separate wiring system. Unfortunately, this advantage has been offset by the need for expensive analog functions, such as adaptive receive and transmit filters. The filters are required to cope with the uncontrolled ac power-line environment plagued with electromagnetic interference, narrow-band frequency impairments, varying impedances, and signal attenuation. Moreover, most existing power-line signaling methods use

simple on-off keying of a narrow-band signal at a typical data rate of 60 bits/s—too slow for installations where many networked sensors and control devices are communicating.

Intellon Corp., Ocala, Fla., overcomes these limitations with a patented technique based on spreadspectrum technology, a proven data-transmission method used for secure military radio-communications operating in hostile environments. Classical spread-spectrum communication involves randomly spreading signals across a broad frequency range, rather than using a fixed carrier frequency. Therefore, if the transmission media distorts portions of



the signal in some frequency bands, this signal redundancy ensures that enough of the signal gets through for reliable communication. The problem is that traditional spread-spectrum technology is incompatible with Ethernet-like carrier-sense, multiple-access (CSMA) networks. The time taken to detect

and generate a carrier signal for effective network arbitration exceeds the time constraints of a CSMA network.

Intellon's patented approach, called Spread Spectrum Carrier technology, has the transmitter generate a unique waveform, called a chirp, over a wide range of frequencies. Each



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networked device uses fuzzy-logic correlation to detect the chirp immediately, without requiring synchronization between transmitter or receiver. The sequence of chirps can be used as the equivalent of a carrier signal in CSMA networks.

Spread Spectrum Carrier technology is scalable over various frequency ranges and data rates. To meet European regulatory requirements on ac power lines, Intellon uses a frequency band of 20 to 80 kHz that supports data rates of 2000 bits/s. In the U.S., the FCC-accepted frequency range for power-line transmission is 100 to 400 kHz. This range meets the Electronics Industries

Association's specification for the ac power-line physical layer in its CEBus home-automation standard (EIA IS-60) for 10-kbit/s data rates. Higher-frequency ranges for higher data rates are available. Intellon says the technology is equally effective with noisy media other than ac power wiring.

The company has implemented this technology in power-line modem ICs that are priced under \$5 each in quantities of 25,000. Development boards are also available (see the figure). Each board costs \$105 apiece in quantities of ten. Both products will be available in the fourth quarter.

Product names are trademarks or registered trademarks of their respective companies. 386 & 486 are trademarks of Intel Corp. SLOTpro is a trademark of Diversified Technology Inc.

MILT LEONARD

ASICS AND ENHANCED SOFTWARE SPRUCE UP LASER PRINTER OUTPUT AND SCANNER INPUT

y combining a pair of ASIC chips and improved imaging algorithms, a new family of laser printers can offer smoother characters and lines as well as higher system throughput. The printers, just released by Apple Computer Corp., Cupertino, Calif., not only produce sharper-looking text thanks to the two ASICs, but also turn out betterlooking half-tone images due to an improved grayscale algorithm. The algorithm, with smaller dots, can create up to seven

times more gray shades than in the previous Laserwriter IINTX. An improved 8-bit gray-scale scanner also lets systems capture more realistic images.

To get the better character appearance on the 300-dot/in. laser-printer engine, Apple Computer designers developed a scheme they call FinePrint technology, which smooths text and lines to simulate higher-resolution printers. One of the two custom chips handles the algorithm. The gray-scale



TECHNOLOGY ADVANCES

upgrade, a scheme called PhotoGrade, was implemented in the other imaging ASIC. That chip adjusts the dot sizing and position selection of the dots to better produce the image. Two additional custom chips were created to simplify the internal circuitry of the printer and handle the three I/O ports.

Unlike most other printers that come with just a serial or parallel port, the Laserwriter IIf and IIg come with three I/O ports, all of which can simultaneously be active. The three ports include a Local-Talk interface, a standard RS-232 serial port, and an Ethernet port on the IIg. All three ports can simultaneously accept data from multiple systems, eliminating network or localized performance bottlenecks that result from printer sharing (waiting because the printer is busy).

To solve the bottleneck problem, the 68030-based controller in the printer arbitrates the ports and allows the incoming jobs to run on a first-in/first-out basis. It accomplishes this by feeding the other incoming jobs into a memory queue formed in part of the 2 to 32 Mbytes of DRAM mounted on the system board. And by employing a 68030, running at 20 or 25 MHz (IIf and IIg, respectively), as the controller. throughput is at least twice that of the NTX.

To send better quality

images to the laser printer, Apple also developed an 8bit gray-scale 300-dot/in. scanner that performs adaptive calibration, and can quickly scale and rotate captured images. The Photoscan operation of the unit checks the entire bed of the scanner to locate the image and then restricts the scanner's range to the size of the image, thus reducing the capture time. Furthermore, prior to capturing the image, the scanner analyzes the image to determine if it's a photograph or line art. Once the image is scanned, the system can automatically straighten the image, crop out excess white space, and be ready for the user to select the area of the image that must saved. Once that region is selected, the system sharpens the image to enhance contrast.

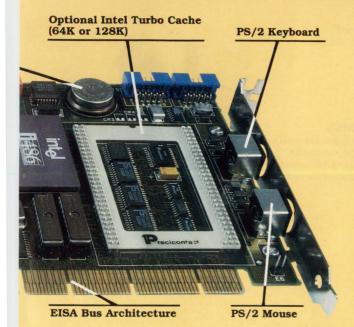
Both the IIf and IIg have the FinePrint capability built in. The PhotoGrade capability is an upgrade feature on the IIf, but comes standard on the IIg. Furthermore, the IIf only has the LocalTalk and RS-232 ports, while the IIg adds the 10-Mbit/s Ethernet port. Both systems also include Adobe Postscript level 2 and PCL 4. Prices for the IIf and IIg systems are \$3999 and \$4999, respectively. The scanner sells for \$1399.

For more information, contact Michael Hopwood at (408) 996-1010.

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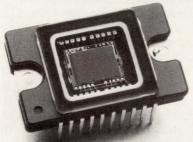
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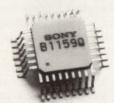
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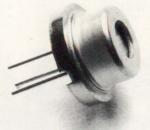
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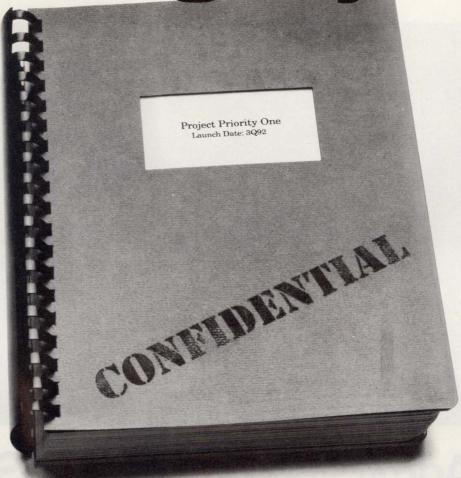
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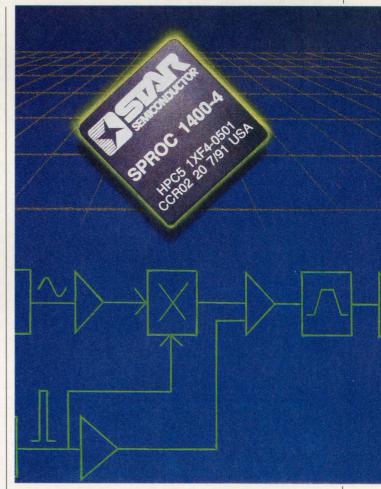
PARALLEL-PROCESSING DSP CHIP DELIVERS TOP SPEED

DAVE BURSKY

s the tasks put before digital-signal processors become more complex, singlechip DSP systems give way to parallel - processing schemes with multiple DSP chips. However, arrays of parallel processors bring their own headaches. In particular, there's the difficulty creating complex software programs needed to control and coordinate the multiple chips, as well as implementing the desired computation algorithm. Difficulty of programming was, for example, the major problem with the systolic digital-signal processor chips introduced in the 1980s. Now, a singlechip DSP with a new multiprocessor architecture, supported by easy-to-use development tools, may smash through that roadblock and open up wide areas of signal-processing-system design to DSP implementations.

By combining single-chip programmability and parallel-processor efficiency with a set of software development tools called Sproclab, designers at Star Semiconductor say they have achieved the right balance of parallelism and ease of software creation. With their Sproc DSP chip, they say that any designer, even an engineer with no expertise in digital-circuit design, can develop signal-processing algorithms on the Sproc with minimal training (see "An analog designer's point of view," p. 44).

The first implementation of the chip, the Sproc 1400, has a multiprocessor architecture optimized for real-time performance and can handle real-time signal bandwidths of 250 kHz, when clocked at 50 MHz. At the heart of Sproc is a shared central memory unit (CMU) that's surrounded by four independent gen-



eral signal processors (GSPs). The shared memory consists of 1024 words (24 bits wide) of RAM for data storage, and a similar-sized RAM for code storage (Fig. 1). Also included on Sproc are four serial ports, a 24-bit (8/16/24-bit selectable) parallel port, and a 16-bit address bus (the lower 12 bits are for internal memory addressing, and all bits are used for external memory access). A small boot ROM (512 words by 24 bits), a special serial-access

PARALLEL PROCESSING DSP CHIP

port, and a novel signal probe are also on the chip.

The Sproc 1400's 24-bit word width gives the chip a dynamic range of 144 dB. That's wide enough to handle over 95% of the signal-processing applications, according to Jeff Robinson, one of the company founders and chief architect of the chip.

Each GSP executes programs out of the shared memory just as any standard processor would execute from its own dedicated memory. The CMU has over a dozen ports, according to Star's Robinson. To get the large number of ports without complicating the memory-cell structure, he employed time-division multiplexing to create a multiport memory, with each GSP and the chip's internal controller block getting a time slice of the memory. When the external clock is set at a frequency of 50 MHz, the internal clock cycle is 100 ns. During that cycle, the chip can execute four instructions (one for each

GSP) and one I/O operation.

The GSP instruction set is similar to that of a microprocessor, with three cycles needed for a multiplication, and most other instructions executing in one cycle. Each GSP contains a hybrid 24-by-24-bit multiplier (a serial-parallel combination) that can deliver a 48-bit result. There are an additional eight guard bits that allow the math block to actually accumulate the results up to 56 bits. The ALU can run in parallel with the mul-

AN ANALOG DESIGNER'S VIEW OF SPROC

he late George Philbrick would have loved a system like Sproc. He's the guy who realized that the operational amplifier was a signal-processing-system element, rather than just a basic analog computer building block. If you design analog systems that must process signals in real-time accurately and reliably, but can never quite get the performance you need, or they take too long to design, Sproc may be the solution. The new chip and suite of tools may be particularly relevant if you're still wary (scared) of a digital approach, or worse vet, you tried one or more of the available DSP chips and decided that writing code was for the birds.

If you have at least moved to a schematic-capture tool on a PC, you can usually capture a goodsized schematic after a few hours of training. Moreover, you needn't wait for the schematic to be laid out and fabricated: it can be modified any time you likeeven on the fly. That flexibility, coupled with the power of some of the sophisticated simulation tools available on high-end PCs and workstations, gives an inkling of what Sproclab, Star Semiconductor's software development system, is all about.

The tools, at times, can give you an eerie feeling of "virtual reality." You can create a circuit, and the stimulation signals for it, with the capture software. The code to configure the chip can then be

generated automatically and downloaded to the chip. After that, instead of simulating, you can instantly look at any circuit node with a *real* oscilloscope attached to the probe output port of the Sproc chip.

To illustrate, you can synthesize a square wave by capturing a series of sine-wave generators and specifying one as a fundamental frequency and the remaining as its 3rd, 5th, 7th and nth harmonic. You can also call out the amplitude of each. The output of each is buffered with an op amp, and every signal is summed by an additional op amp. By loading that compiled signal flow algorithm into Sproc, you can look at the output square wave or any of the individual sine waves on the oscilloscope. Each harmonic can be turned on and off to see the effect on the square wave and determine how many you need to get the desired square wave. It's a convenient way to replace the tens of hours that manual drawing might have taken prior to computer-based tools (and a good way to teach Fourier analysis!).

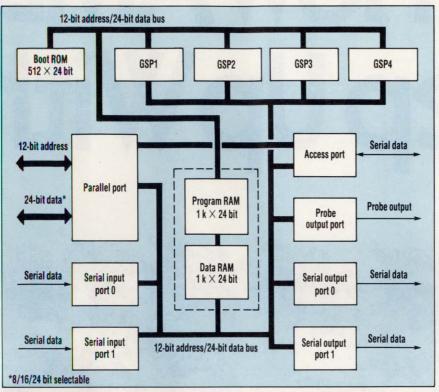
Another example involves an adaptive filter that eliminates a variable-frequency, yet coherent and therefore correlatable, interfering "noise" from a complex analog signal, say, music. Because music is virtually noise, the random-noise-generator cell must first be captured from the library for use as the signal. A *real* interfering signal from a *real* function

generator is connected to the Sprocboard, where it's digitized by a 16-bit delta-sigma ADC and fed to Sproc. This is where you truly have trouble determining reality. Synthetic noise is being used as a signal, and a real signal as noise. The digitized noise from the ADC is brought up on the PC's screen from the I/O port and mixed with the "music." The adaptive filter is then constructed from cells in the library using the filter-design program, Sprocfil, and added to the circuit.

You can now examine any of the waveforms, both inside and outside of the chip, using the oscilloscope. You can look at the clean, random noise (music) generated by the chip, the interfering signal from the function generator, and the music plus the interference. The clean music out of the filter can be compared with the original synthesized noise. As you change the frequency of the interference from the real function generator, the scope will show the filter adapt to the changing, coherent interference. The interference from the signal should then be eliminated. Sproc can run a fast Fourier transform on the cleaned up "music" to look for signs of the interference. Alternatively, knowing the interfering frequency, a very narrow bandpass filter can be implemented with Sproc and connected to the output of the adaptive filter to look for remnants of the interference.

FRANK GOODENOUGH

PARALLEL PROCESSING DSP CHIP



1. A CENTRAL MEMORY consisting of two blocks of RAM—program and data—is used by the four general signal processors (GSPs) and the serial and parallel ports on the Sproc chip developed by Star Semiconductor. Every instruction cycle, the chip performs one instruction in each of the four GSPs and one I/O operation.

tiplier, permitting the pipelined combination to deliver fast multiply-and-accumulate operations. These types of operations are crucial in most filtering and other signal-processing operations.

Part of the design library bundled with the development tools includes prewritten blocks of code. Those code segments offer over 50 basic blocks, such as amplifiers, multipliers, integrators, infinite-impulse-response filters, limiters, finite-impulse-response filters, rectifiers, oscillators, and many other functions. Cell parameters can then be set during system programming.

Within a GSP, an amplifier is the simplest function to implement, while the most complex function could range up to dual adaptive filters for modems, noise cancellers, and speech compression and recognition. Algorithms like fast wavelet transforms (an algorithm developed at the Massachusetts Institute of Technology and by Prof. Mike God-

frey at Stanford University) are stream oriented, and they fit the GSP blocks well. The algorithms fundamentally require one sample in for one sample out and use multiple channels. In comparison, most cur-

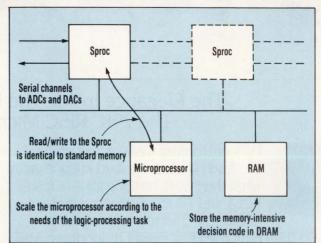
rent algorithms are block-oriented, in which multiple samples are collected and executed on as a single block.

Control and status registers are memory-mapped into the internal address space of the chip, making it a simple matter to address and access the registers. To coordinate the four GSPs, the Sproc chip includes a powerful and flexible mech-

anism that manages the data and instruction flow between the serial ports, the CMU, and each GSP. These data flow managers handle the I/O tasks, offloading the GSPs, which eliminates any I/O operation impact on GSP performance. The data-flow managers communicate with the GSPs and other on-chip elements over the internal 24-bit data bus and to the outside world through programmable serial ports.

The serial interfaces consist of two dedicated input ports and two output ports. Each port can operate with its own internal or external clock. Four signal lines are on each of the input or output ports: data, clock, strobe (this signal line acts like a data-valid line), and synchronization (this line is used to synchronize block transfers). Word length and bit ordering are both programmablewords can be 8-, 12-, 16-, or 24-bits long and data ordering can be set for most-significant or least-significant bit first. The parallel port is a bidirectional, asynchronous interface up to 24-bits wide. During chip configuration, the word width of 8, 16, or 24 bits and the byte ordering of MSB or LSB first can be selected. Through the parallel port, the Sproc can be dynamically reprogrammed by a host processor (when the Sproc is in its slave mode).

Supplementing the standard serial ports is a five-line access port that



2. THE SPROC CHIP can be used as either a standalone chip or with a host microprocessor. In either case, multiple Sproc chips can share the data bus to tackle applications too complex for one Sproc to handle.

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PARALLEL PROCESSING DSP CHIP

offers a direct link between an interface module, called the Sprocbox, and the chip. The five lines consist of a clock, data input, data output, strobe input, and strobe output. The clock line can run at up to about 40% of the master clock frequency. Special software (Sprocdrive) enables the user to dynamically modify system parameter values over the access port, thus permitting system debugging and calibration without the need for expensive logic analyzers or in-circuit emulators.

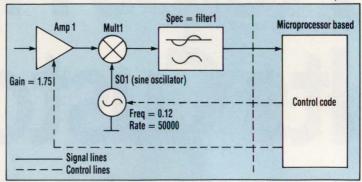
The same Sprocdrive software controls an internal software-directed signal probe that functions just like an oscilloscope probe. Internal circuitry under control of the Sprocdrive software steers selected internal signals to a dedicated output port that includes an 8-bit digital-to-analog converter. There, the signals can be viewed or measured during chip operation. The probe port has three signal lines-clock, strobe, and data output (either digital or analog lines)—and can be used interactively when the chip is executing its DSP algorithms.

The chip can be employed in either

standalone mode as a controller (master) or with a host microprocessor as memorymapped peripheral (slave). In the master mode, the onchip boot ROM, upon power-up, tells the chip to upload its configuration from an external bytewide memory over the parallel port into the onchip RAM. In the

slave mode, the chip relies on an external controller to handle the downloading of configuration files. A simple watchdog timer is included as part of the parallel port to prevent any bus lockups from totally freezing the system. The timer interval is fixed at 160 master clock cycles (about $4 \mu s$).

In a multi-Sproc system, there can be only one bus controller—either a



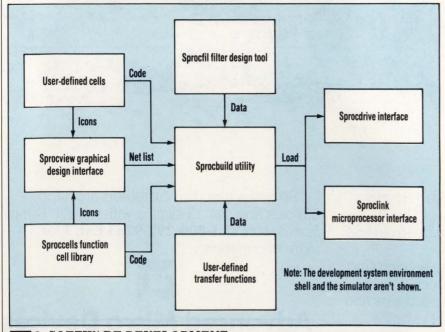
4. A SMALL SEGMENT of a signal flow diagram shows the typical elements that designers would assemble to define an application. Signal-processing blocks, such as amplifiers, multipliers, signal sources, and filters, can be interconnected. Then the code representing those blocks will be scheduled by the Sprocbuild utility.

host processor or one Sproc configured as a master and the others configured as slaves. In a typical system, the Sproc chips handle all signal-processing functions, while a host microprocessor would manage the logic processing and system control (Fig. 2). The bus controller must individually enable the chip-select input of each Sproc as its configuration data is downloaded. Four special external-memory address pins allow up to 16 Sproc chips to communicate over a common data bus. The address field must be decoded externally to create the multiple chip-select signals needed for the Sprocs.

RAPID DEVELOPMENT

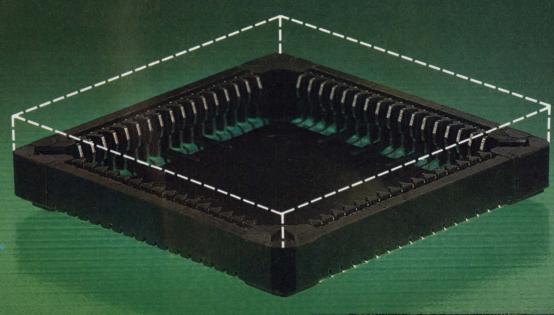
Development tools created by Star-the Sproclab development system—make it easy to apply the chip. The tools are based on a signalflow design approach and can automatically generate the code that controls and configures the Sproc chips. The environment, a real-time application development setup, makes it possible for users to create production applications in just minutes. Those applications can range in complexity from solid-state inertial navigation systems to multimedia addons for workstations to secure military communications modems to instrumentation (the chip has already been committed for these places by some of the beta sites).

A graphical design-entry front-



3. SOFTWARE DEVELOPMENT tools for Sproc include an integrated set of packages that consist of a library, a cell builder, a filter design tool, an interface to the hardware development tools, and a graphical design package. Once net lists are created, the Sprocbuild utility will convert the net list, link all of the code blocks, and prepare a file for downloading to the target chip.

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end, loaded onto an IBM PC or clone that runs the ViewLogic or OrCAD design capture software, is the best starting point when developing an application with the toolkit. The PC should have at least an 80386 processor, a DOS 3.1 or higher operating system, 5 Mbytes of extended memory (including the base 640 kbytes), two serial ports, one parallel port, a 101-key keyboard and three-button mouse, an EGA or VGA monitor, and a hard-disk drive with at least 5 Mbytes of free space.

By employing the Sproclab development tools in combination with the Sprocbox development/interface adapter and Sprocdrive, the serial port on a PC can tie into the five-line access port. Combining the PC-based software and the access port allows users to perform interactive debugging right on the target system.

The entire procedure for a typical project might follow this scenario:

1. Define the signal-processing applications and determine the design requirements.

2. Capture the design as a signal flow diagram.

3. Define any necessary filters and transfer functions.

4. Convert the diagram and definitions into code and create the load file

5. Load, run, and debug the design on the chip.

6. Incorporate changes from debug into the design diagram.

7. Convert the revised flow diagram and generate an updated load.

8. Port the design into the actual application.

COMPATIBLE SOFTWARE

The Sproclab icon library installs under the OrCad or ViewLogic software, making it possible to create signal flow diagrams on the screen. All of the tools are coordinated by the Sprocbuild utility, which converts the net list, user-defined cells, library cells, and the other tools into a unified code list that can be downloaded to the chip (Fig. 3).

A typical signal flow diagram consists of blocks, such as amplifiers; signal sources; and functions, such

as multipliers. All of these blocks are interconnected like a schematic drawing (Fig. 4). Once the diagram is developed and the parameters attached to the various blocks, the design can be compiled and downloaded to the target system.

In addition to the library and various interface tools, the toolkit comes with a routine specifically for digital filter design, Sprocfil. That tool simplifies the task of programming the chip to implement IIR and FIR filters. When called up, Sprocfil allows users to just enter in the filter they desire and the various filter characteristics. Then the software will compute all of the configuration parameters, coefficients, and prepare the code for loading into the chip. The entire process, from signal flow diagram to executable code, typically takes less than five minutes, which is orders of magnitude less time than traditional DSP programming approaches.

To go along with the software tools, Star developed a free-standing evaluation board that contains the Sproc chip as well as 16-bit dual ADCs and DACs for the I/O ports. Also included on the evaluation board are various communications interfaces and additional components necessary to evaluate signal-processing performance during development. A small line-operated power supply delivers the 5- and 12-V levels needed by the Sprocbox and evaluation board. □

PRICE AND AVAILABILTY

The 20-MHz version of the Sproc chip, the Sproc 1400-2, comes housed in a 132-lead ceramic pin-grid array and sells for \$450 apiece in 100-unit lots. Less expensive dual and single GSP versions of the chip will be released in 1992. Furthermore, 40- and 50-MHz speed grades will be released in the first quarter of 1992. The starting price in single-unit quantities for the development system is \$8950. Delivery of the chip or the system is from stock.

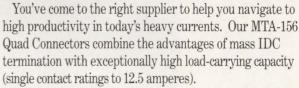
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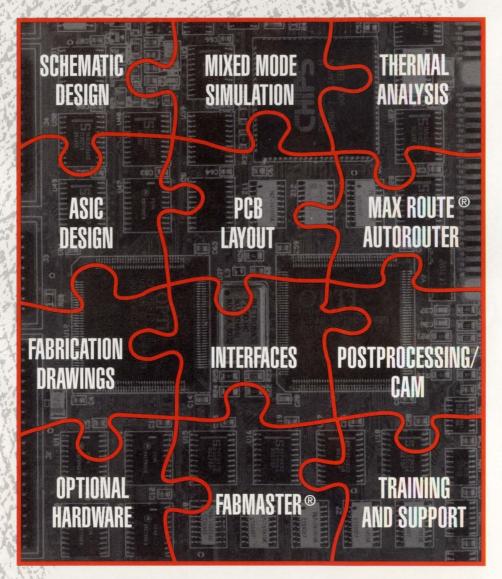
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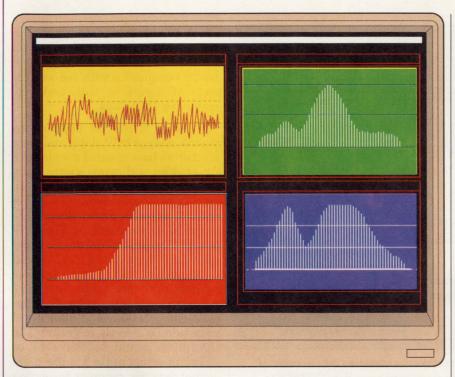
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DSPS EXPAND ROLE AS COST DROPS AND SPEED INCREASES

ver the past two decades, digital-signal processing has evolved into a pervasive "How did we ever get along without it?" capability. That's a far cry from its roots as a hard-touse, expensive technology that could rarely perform its magic in real time. Today's single-chip DSPs have replaced yesterday's minicomputers and mainframes with microprocessor-like ease of use and low commodity-component prices. The ability to integrate the key functions required DAVE BURSKY

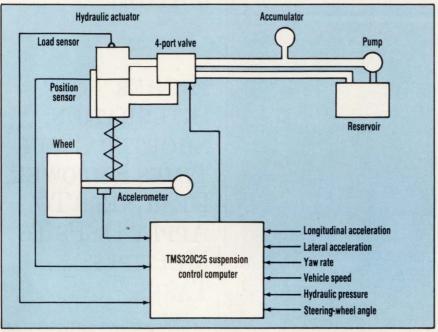
HIGHER
INTEGRATION,
SHORTER CYCLE
TIMES EMPOWER
DESIGNERS TO
APPLY DSPS TO
MULTIPLE
TASKS.

for DSP operations—fast multiplication and accumulation—along with a programmable processor, started designers down a path that, in addition to its many traditional uses, has led to hundreds of innovative applications previously considered impractical.

DSP chips can now be found in cars, wireless telephones, stereo equipment, video cameras, modems, computers, disk drives, robots, test equipment, satellites, rockets, and many other places. New medical diagnostic procedures, based on computation-intensive DSP-centered ultrasound and other imaging technologies, have revolutionized health care. In computers, DSP-based servo control and compression techniques allow hundreds of megabytes to be stored in ever-smaller disks. Digitally based television sets include DSP functions to eliminate "ghost" images, while digital audio systems apply DSP to deliver unprecedented fidelity without the background hiss common to analog recording.

Future developments will see advanced car stereo systems that apply DSP-based noise-cancellation circuits to remove road noise and car rattles while the music is playing. Other automotive DSP uses will include adaptive suspensions that adjust wheel height in response to road conditions (Fig. 1). And, future gen-

DSP TECHNOLOGY TRENDS



1. BY APPLYING A DSP CHIP to suspension control in a car, researchers at Oakland University were able to use the fast computational power of the TMS320C25 to continually adjust the hydraulics. As a result, the car's passenger compartment could remain stable as it rides over rough surfaces.

erations of DSP chips will open up even more applications—multimedia, video conferencing, voice command, handwriting recognition, etc.—as multiprocessing architectures allow designers to add almost unlimited compute power.

For DSP chips to gain such momentum, many factors had to come together and continue progressing over the last few years:

• VLSI circuit manufacturing had to hit the submicron regime and continue shrinking for chip makers to fabricate complex and fast integer or floating-point chips that can be sold to the mass market for a few dollars to a few hundred dollars each.

- Innovative architectures had to be developed to achieve supercomputer-like giga-operation-per-second (GOPS) performance levels and thus sidestep VLSI manufacturing limitations (density, power, speed, etc.).
- High-level-language programming support, such as with C compilers and other languages, had to be developed to allow algorithms to transfer rapidly from the R&D bench to manufacturing.

• And, finally, lots of designer education had to take place (and it still continues) to familiarize the general design community with the key aspects of designing with and programming DSP chips.

Although a host of applications can use integer DSP chips, and manufacturers have created a wide variety of chips with word widths from 12 to 24 bits, many designers are migrating to 32-bit floating-point processors, explains Shaul Berger, director of applications at The DSP Group. "Designers eye the floatingpoint DSP chips as the ideal target, since much of the software development done on workstations and large computers employs 32-bit floatingpoint computations and algorithms and could be directly migrated. The algorithms would not have to be scaled to compensate for the more limited dynamic range or resolution of an integer processor."

Hardware is important, continues Berger, but to speed application development, more powerful software tools are needed for algorithm development. High-level languages are good for outlining an application and performing simulation, but hand-coding at the assembly-language level will still be key for the critical subroutines within algorithms. Code density affects performance, memory size, and system power.

Real-time operating systems are also starting to impact DSP applications in such areas as industrial control and instrumentation. In those areas, the DSP chips are often called on to perform some degree of control

Generation Era	First c. 1978-1983	Second c. 1983-1986	Third c. 1986-1990	Fourth c. 1990-1994	Fifth c. 1994-1997
Analog macrocells	No	No	No	Yes, A/D & D/A	Extensive
Architecture	von Neumann & Harvard	Harvard	Harvard	Harvard	7
Cycles/MAC	2	1	1	1	<1
DMA	No	Yes	Yes	Yes	Yes
I/O Ports	Parallel only	Serial/Parallel/Timer	Multiple	Multiple	Multiple
Instructions	RISC	RISC + event control	RISC+event+Boolean	RISC+event+Boolean	CISC
Interrupts	No	Yes	Yes	Yes	Yes
MAC Time	> 200 ns	< 160 ns	< 80 ns	< 35 ns	< 20 ns
Memory division	Prog + Data + Coeff	Prog + Shared Data/Coeff	Reconfigurable	Reconfigurable	Reconfigurable
Memory options	ROM/External	ROM/EPROM/External	RAM/ROM/EPROM/external	RAM/ROM/EPROM/external	RAM/ROM/EEPROM/externa
Memory space	4k words	64k words	64k-16M words	64k-16M words	64k-16M words
On-chip emulation	No	No	No	Yes	Yes
Operations/clock	1/60	1/2	3	3	5
Process	3-µm NMOS	2-µm CMOS	1.2-µm CMOS	0.8-µm CMOS	0.5-µm CMOS



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DSP TECHNOLOGY TRENDS

Vendor	PN	Function				
ADI	ADV7141	Continuous edge graphics				
AMD	Am7911	1200/150 bps modem				
C-Cube	CL-550	DCT image compression IC				
Dallas	DS2160	DES encryption chip				
DSP group	DSPG6000	Answering machine processor				
Exar	XR-2401	2400 bps MNP5 modem processo				
Intel	89C026	2400 bps modem				
III	Digit 2000	TV chip set				
NEC	μPD77501	Speech synthesizer				
NPC	SM5804	CD audio filter				
Oki	MSM6994	V.32 modem chip				
Pioneer	PD0029	Filter chip (fixed)				
Plessey	PDSP16401	Edge detector chip				
Rockwell	RD96NFX	9600 bps fax modem (hybrid)				
Sanyo	LC7860	CD player filter/servo IC				
Seimens	PEB2091	ISDN U transceiver				
Sierra	SC11046	2400 bps modem				
Sony	CXD1144AP	CD player filter				
ST/Inmos	IMSA121	DCT image compression IC				
Yamaha	YM-3805	CD player filter/servo IC				
Zoran	ZR36020	DCT image compression IC				

as well as signal processing, and may often have to change functions based on an input control signal or changing system conditions. Both Spectron Microsystems Inc., Santa Barbara, Calif., and AT&T have such real-time operating systems. Currently, each company has single-tasking versions, but Spectron is now working on a multiprocessor version of SPOX, its real-time OS for the Texas Instruments TMS320C30.

Existing tools provide only part of the solution, but toolsets like the Signal Processing Workstation from Comdisco Inc., Foster City, Calif., are a good starting point. With the Comdisco tools, algorithms can be developed and implemented with software building blocks and tied into compiler tools for several specific DSP chips; once the algorithm is firm, the system can automatically translate the algorithm into a program listing for the particular DSP chip. Future tools will also allow the user to compile custom chips directly from the algorithm.

The industry has already seen three generations of DSP chips, with the fourth generation just starting to appear and the fifth now in definition (Table 1). Many of the current-generation high-end DSP chips are fabricated with processes that can create 0.8-to-1- μ m minimum device features, packing half-a-million or more transistors onto one chip. The

When considering DSP, take

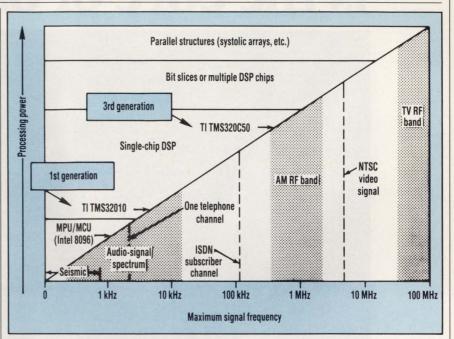


DSP TECHNOLOGY TRENDS

next-generation DSP chips promise to more than double that number to add more memory and compute resources. New technologies like biC-MOS (the merger of bipolar and CMOS logic on the same chip) promise significant improvements in performance as well.

Many companies have already applied biCMOS to produce high-speed static RAMs. And those RAMs are key elements that must be integrated into top-performing DSP chips. Another area ripe for biCMOS, internal to the chip, is to drive large buses that start to crisscross the chip. In some VLSI chips, as much as 75 meters of fine-line metallization can be squeezed onto the surface of silicon.

The large buses are employed so that chip designers can cram as much parallelism into the architecture as possible. To do that, lots of data must be moved between various sections of the chip all at the same time. Multiple data moves, in turn,



2. AS THE SIGNAL FREQUENCY increases, Forward Concepts projects that more processing power is needed to handle signals above 1 MHz. Below 1 MHz, one chip can suffice. But above that, multiple chips or even systolic arrays are needed.

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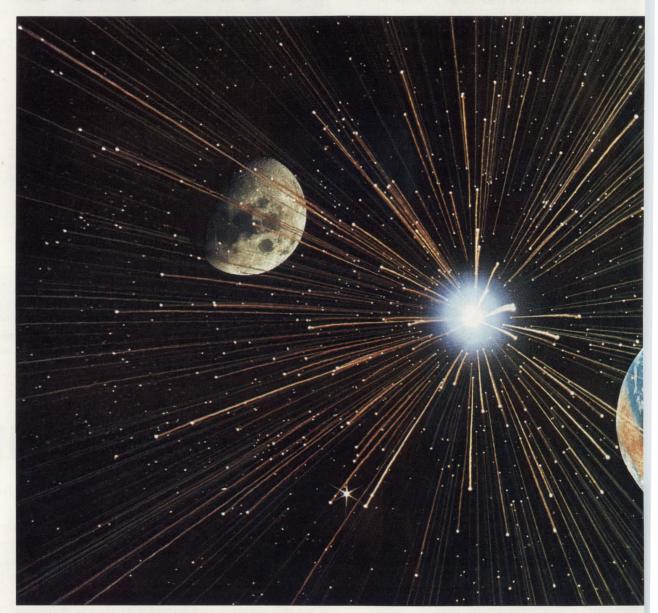
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DSP TECHNOLOGY TRENDS

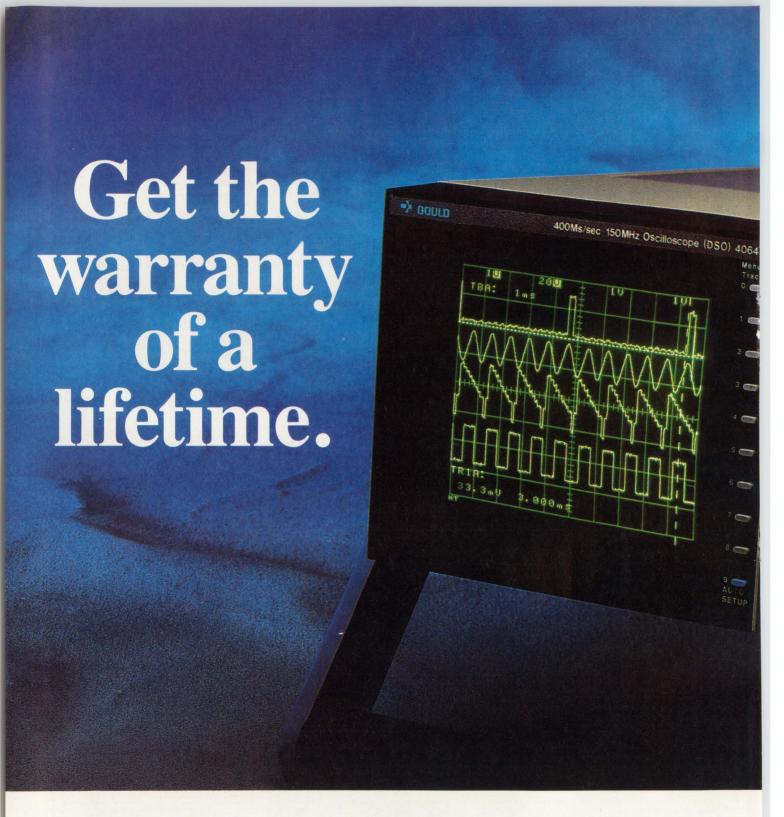
Company	Part number	Cycle time (ns)	Parallel I/O ports	Serial I/O ports	DMA inter- face	Multiply and accu- mulation	Program memory	External memory	Data RAM (words × bits)-	External data RAM	Data ROM	Comments
MI/Gould	S7720	250	1	2	N	16 × 16 =	512 × 23 ROM	None	128 × 16	None	510 × 13	NEC 7720 2nd source
	S77C20	150	1	2	N		$512\times23\text{ROM}$	None	128 × 16	None	510 × 13	NEC 77C20 2nd source
analog Devices	ADSP2100A	80	0	2	N	16 × 16 =	None	32k × 24	None	16k × 16	None	
	ADSP2101/02	80	0	2	N	16 × 16 = 40	2k × 24 (/02 ROM)	8 (2k × 24) EPROM	1k × 16	14k × 16	2k × 24	-
	ADSP2105	100	0	1	N	16 × 16 =	$1k\times 24$	-	512 × 16	11-11	1	Price \$9.90 any qty
	ADSP2111	77	1	2	N	16 × 16 =	$2k\times 24$	-	1k × 16	14k × 16	$2k\times 24$	Host interface port
	ADSP21MSP50	75	1 × 16	2	N	16 × 16 = 40	$2k \times 24$	-	1k × 16	476	<u>-</u>	w/Lin. CODEC/pwr dwr
T&T	DSP-16-55	55	1 × 16	1	N	16 × 16 = 32	2k × 16 ROM	64k × 16 (Alt)	512 × 16	64k × 16	= 1	75 ns ver. available
	DSP-16A-25	25	1 × 16	1	N	16 × 16 = 32	$4k \times 16 ROM$	$64k \times 16$	2k × 16	64k × 16	$4k \times 16$	55, 75 ns and MIL versions
	DSP-16C	38.5	= 1	Ŧ	-	16 × 16 = 32	12k × 16	5-ju	2k × 16	4-1	-	For cellular
ujitsu	MB87064	100	-	0	-	16 × 16 = 32	4-1	1-1	128 × 16 × 2	1k × 16	None	Mask-ROM-only version
	MB8764	100	0	0	Y	16 × 16 = 26	$1k \times 24 \text{ ROM}$	$1k \times 24$	$128\times16\times2$	1k × 16	None	Device for modems
Matsushita Panasonic)	MN1901	250	1 × 16	2	Υ	20 × 20 = 32	$2k \times 32 \text{ ROM}$		66 × 16	4k × 16		Volume chip
	MN19011	200	1 × 16	2	Υ	20 × 20 = 32	$2k \times 32 \text{ ROM}$		256 + 512 × 16	4k × 16	-	
	MN1902A	100	1 × 16	2	Υ	20 × 20 = 32	$3k \times 32 \text{ ROM}$	1-:	66 × 16	4k × 16	-	-
	MN19041A	100	1 × 16	2	Y	20 × 26 = 32	$4k \times 32 \text{ ROM}$		256 + 512 × 16	4k × 16	F.	7
	MN1909	250	1 × 16	2	Υ	20 × 20 = 32	External only	$8k \times 32$	66 × 16	4k × 16	8k × 16	DMA, development chip
	MN19091A	200	1 × 16	2	Υ	20 × 20 = 32	External only	$8k \times 32$	256 + 512 × 16	4k × 16	-	
	MN1911	100	1 × 16	2	Υ	20 × 20 = 32	$2k \times 16 ROM$		256 + 288 × 16	4k × 16	-	- 1
	MN1920	80	2 × 16	2	Y	24 × 24 = 40	$4k \times 40 \text{ ROM}$	-	514 + 1k × 24	<u> </u>	(-	Under development
licrochip	DSP320C10	200	0	0	N	16 × 16 =	1536 × 16 ROM	4k × 16	144 × 16	None	None	
	DSP320C10-32	122	0	0	N	16 × 16 =	1536 × 16 ROM	$4k \times 16$	144 × 16	None	None	Fastest 1st generation
	DS0320EE12	200	0	0	N	16 × 16 =	$\begin{array}{c} \text{2.5k} \times \text{16 EE-} \\ \text{PROM} \end{array}$	$4k \times 16$	144 × 16	None	None	1 11 -/ 1
lotorola	DSP56000	74	1 × 8	1	N	24 × 24 = 56	2k × 24 ROM	64k × 24	256 × 24 × 2	64k × 24 × 2	256 × 24 × 2	ROM-based
	DSP56001	74	1 × 8	1	N	24 × 24 = 56	$512\times24\text{RAM}$	$64k \times 24$	$256\times24\times2$	$^{64k}\!\times\! ^{24}\!\times\! ^{00000000000000000000000000000000000$	256 × 24 × 2	RAM-based
	DSP56116	50	1×8	2	N	16 × 16 = 40	$2k \times 16 RAM$	64k × 16	2k × 16	64k × 16	-	
	DSP56156	50	1 × 8	2	N	16 × 16 =	$2k\times 16RAM$	$64k \times 16$	$2k\times 16$	64k × 16	-	w/Linear CODEC/40 MH

ELECTRONIC DESIGN REPORT

DSP TECHNOLOGY TRENDS

Company	Part number	Cycle time (ns)	Parallel I/O ports	Serial I/O ports	DMA interface	Multiply and accu- mulation	Program memory	External memory	Data RAM (words $ imes$ bits) $-$	External data RAM	Data ROM	Comments
NEC	μPD7720	122	1	2	N	16 × 16 = 31	512 × 23 ROM/EPROM	None	128 × 16	None	510 × 13	Sampled in Japan Q2/8
	μPD77220	122	1	1	N	24 × 24 = 47	$2k \times 32 \text{ ROM}$	$4k \times 32$	$256\times24\times2$	8k × 24	$1k \times 24$	Integer ver. µPD77230
	μPD77C20	122	0	1	Υ	16 × 16 =	512 × 23	None	128 × 16	None	510 × 13	Oki sells as MSM77C20
	μPD77C25	122	1	1	N	16 × 16 = 32	$2k \times 24 \text{ ROM}$	None	256 × 16	None	1k × 16	EPROM version
Oki Semicon- ductor	MSM77C21	122	0	1	Y	16 × 16 =	512 × 23	None	128 × 16	Non	510 × 13	NEC μPD77C20
Philips	PCB5010	122	1 × 16	2	N	16 × 16 =	987 × 40 ROM	None	$128 \times 16 \times 2$	None	512 × 16	
	PCB5011	122	1 × 16	2	N	16 × 16 = 40	None	$64k \times 40$	256 × 16	512 × 16	None	-
SGS-Thomson	ST18930	80	-	2	N	16 × 16 =	$2k \times 32 \text{ ROM}$	None	128 × 16 × 2	4k × 16	512 × 16	32-bit/CMOS Ver of 68930
	ST18931	80	-	2	N	16 × 16 = 32	None	$64k\times32$	$128\times16\times2$	4k × 16	512 × 16	CMOS ver of 68931
	ST18940	100	1	1	Y	16 × 16 = 32	$2k \times 32 \text{ ROM}$	None	$127\times16\times2$	4k × 16	-	w/CODEC serial I.F.
	ST18941	100	1	1	Y	16 × 16 =	None	$64k\times32$	128 × 16	64k × 16	512 × 16	w/CODEC serial I.F.
	TS68930	160	-	0	-	16 × 16 = 32	$\begin{array}{c} \text{1.2k} \times \text{32} \\ \text{ROM} \end{array}$	None	$128\times16\times2$	-	-	-
	TS68931	160	-	0	-	16 × 16 = 32	None	$64k \times 32$	$128\times16\times2$	4k × 16	512 × 16	-
ТІ	TMS320C10	160	1	0	N	16 × 16 =	1536 × 16	4k × 16	144 × 16	None	None	Pin compat w/TMS320
	TMS320C14	160	1 × 16	1	N	16 × 16 = 32	$4k \times 16 \text{ ROM}$	$4k \times 16$	256 × 16	None	-	CODEC/compare/PWI
	TMS320C15	160	1	0	N	16 × 16 = 32	$4k \times 16 ROM$	$4k \times 16$	256 × 16	None	None	
	TMS320C16	114	1	0	N	16 × 16 = 32	$8k \times 16 \text{ ROM}$	$64k \times 16$	256 × 16	None	None	Low-end chip (10-k qty
	TMS320C17	160	1	2	N	16 × 16 = 32	$4k \times 16 \text{ ROM}$	None	256 × 16	None	None	Compander/timer/I.F
	TMS320C25	80	0	1	N	16 × 16 = 32	$4k \times 16 \text{ ROM}$	$64k\times16$	288 + 256 × 16	64k × 16	4k × 16	100, 200 ns ver. avail
	TMS320C26	80	0	1	N	16 × 16 =	1.5k × 16	$64k \times 16$	288 + 256 × 16	64k × 16	4k × 16	
	TMS320C50	35	1 × 16	2	N	16 × 16 = 32	$8.7k/2k \times 16$ RAM/ROM	$64k \times 16$	1056 × 16 shared	64k × 16	-	Emulat/JTAG/pwr dwi
	TMS320C51	35	2 × 16	2	N	16 × 16 = 32	$1k/8k \times 16$ RAM/ROM	$64k\times16$	$1056 \times \text{shared}$	64k × 16	-	On-chip emulation/JTA
Toshiba	T6386/7	250	-	0	-	16 × 16 = 31	512 × 16 ROM/External	-	128 × 16	_	512 × 16	T6386: ROM, 28 pins
Zoran	ZR34161	100	1	0	Υ	17 × 17#	None	64k × 16	128 × 19 × 2#	64k × 16	Look up	# Handles complex ma

Note: Data for the table supplied by Forward Concepts Inc.



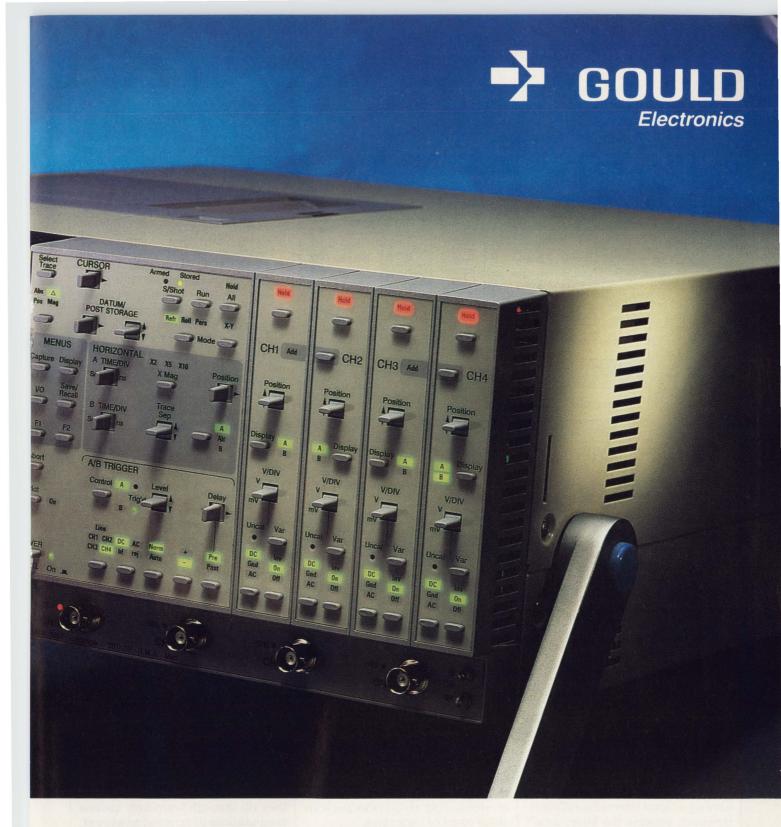
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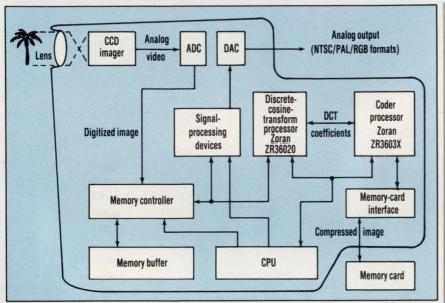
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DSP TECHNOLOGY TRENDS



3. TO SQUEEZE VIDEO IMAGES onto storage-limited memory cards, a new still-image camera developed by Fuji Film and Zoran contains image digitization and compression circuits. Thus, the memory card need only store the compressed image, which may just contain 1/10 to 1/30 the original amount of data.

require that multiple buses be used to tie the chip's subsections together. Those buses are heavy capacitive loads and are better driven by bipolar devices than by MOS transistors.

Multiple operations are common in 32-bit DSP chips, for example. The logic could, in a single cycle, perform an integer and a floating-point calculation in parallel, and at the same time compute new data and instruction addresses and store a previous result in a register file. Typical of such an architecture are the TMS 320C30 and 40 from Texas Instruments and the 96002 from Motorola. Integer processors like the DSP-16 from AT&T and the TS68930 series from SGS-Thomson and others also have significant internal parallelism. However, because the buses aren't as wide and the chip is smaller, the loading factor is lower and biCMOS probably won't be used heavily in the 16-bit world.

Today's chips are typically uniprocessors—one CPU per IC that can rip through computations at rates measured in tens of nanoseconds per operation. The biggest of these chips typically measure almost 0.6 in. on a side—the largest area practical with today's 10X reduction

step-and-repeat lithography systems. Future chips, though, will take advantage of lithography improvements. These enhancements will widen the imaging field to almost an inch on a side, doubling or even tripling the available circuit area.

While area increases, feature sizes are expected to decrease. Therefore, by the second half of this decade, chips containing transistors with minimum features of 0.4 µm will be in mass production. As a result, when the increased chip area and decreased features are combined, logic "superchips" about an inch square with 20 to 40 million transistors will be practical. Memory chips will, of course, be even denser—containing about twice the transistor count of logic chips.

Some activity in these large chips can be seen in research on systolicarray processors (sometimes referred to as wavefront processors) implemented with wafer-scale integration. Arrays containing a few to several hundred processors on one silicon substrate have been demonstrated at IEEE-supported symposiums, such as the International Conference on Wafer-Scale Integration and the International Conference on

Acoustics, Speech and Signal Processing. None, though, are ready for commercial release because many issues, such as redundancy, interconnection, programming, packaging, cost, and even power consumption, must be addressed.

Nearly every DSP manufacturer employs CMOS for its chips to minimize power consumption. But as the clock frequencies extend past 30 and 40 MHz, power dissipation jumps considerably. The chips' high clock rates—20-to-40-MHz for today's production chips—push the power drain into the 3- to 6-W range for some of the larger chips (thus a wafer with 15 to 30 such chip sites interconnected could end up dissipating well over 100 W). And, as complexity increases and operating speeds exceed 50 MHz, power levels—even for CMOS chips—may end up surpassing 10 to 15 W per chip unless other means are employed to reduce power.

By the middle of the decade, we'll probably see the use of a reduced external power supply. Today's standard 5-V supply will give way to the 3.3-V standard supply level that's already starting to garner significant support in the notebook-style personal computers. That will also allow the DSP chips to meld into portable computers, where they will perhaps be used for various time-shared tasks-image compression/decompression, speech recognition and synthesis, signal processing for modem and facsimile transmission and reception, handwriting recognition, and other tasks for the mobile com-

puter user.

DSP chips have taken on many of the tough algorithmic problems, and they rip through seemingly endless computations to arrive at an answer. But the DSP chips aren't the only solution—some analog-signal processing will always be required. Analog front- and back-ends—the analog-todigital and digital-to-analog converters-are still needed when dealing with speech, music, and many other analog signals of the "real" world.

Furthermore, various situations exist that aren't defined sufficiently for an exact algorithm to execute, explains Bill Strauss, president of



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ELECTRONIC DESIGN REPORT

DSP TECHNOLOGY TRENDS

Forward Concepts Co., Tempe, Ariz., a market research company. As such, those applications could be solved by neural networks or fuzzy logic systems that build in some tolerance for adjustment by "learning" how things change over time and then compensating for it. Similar precepts are used in adaptive digital filtering, in which the DSP chip and algorithm monitor the channel and change the filtering characteristics, depending on the line condition.

According to Strauss, neural networks and DSP chips seem to be entangled in a love-hate relationship. High-speed DSP chips are ideal as a means to emulate neural characteristics and may even end up being coresident in neural computer systems. Strauss says one such example of pairing is in acoustic signature analysis. The sensory data is first converted from the time domain to the frequency domain with the algorithmic-intensive DSP chip, producing a sequence of feature vectors. The neural network is then trained on the vectors from a set of representative data (the signature) to recognize specific vector object signatures.

The other side of the relationship is the opportunity for neural networks to replace DSP chips in some applications—character recognition, for example. However, he estimates that it will probably take another three or four years for neural networks to reach any significant level of commercialization.

Over the last two decades, DSP design approaches have bounced in several directions, starting with building blocks, moving into dedicated functions, and then into programmable processors and multiprocessor schemes in efforts to improve throughput (Fig. 2). In the early seventies, with only MSI and LSI levels available, such building blocks as multipliers and multiplier-accumulators working with lots of TTL MSI chips were the only way to imple-

Company*	Part number	Cycle time (ns)	Parallel I/O ports	Serial I/O ports	DMA interface	Multiply and accu- mulation	Program memory	External memory	Data RAM (words × bits)-	External data RAM	Data ROM	Comments
Analog Devices	ADSP21000	50	-		Y	24E8 (IEEE)	32 × 48 Cache	16M × 48	$16\times40 \\ \text{(register file)}$	4G × 40	None	IEEE-P1149 JTAG port
AT&T	DSP-32	160	1 × 8	1	Υ	24E8 (IEEE)	$512\times32\times2\\ \text{Shared}$	14k × 32	Shared	Shared	512 × 32	2-cy first mpy:8 MFLOPS
	DSP-3210	-	1 × 32	1	Y	24E8 (IEEE)	$\begin{array}{c} 512 \times 32 \times 2 \\ \text{Shared} \end{array}$	$14k \times 32$	Shared	Shared	512 × 32	Multimedia with VCOS
	DSP-32C	80	1 × 16	1	Y	24E8 (IEEE)	$\begin{array}{c} 512 \times 32 \times 3 \\ \text{Shared} \end{array}$	$4M \times 32$	Shared	Shared	$2k \times 32$	ROM ver: RAM = $4k \times 32$
	DSP-32C5E	80	1 × 16	1	Y	24E8 (IEEE)	$\begin{array}{c} 512\times32\times3\\ \text{Shared} \end{array}$	None	Shared	None	$2k \times 32$	No external memory access
Fujitsu	MB86220	75	1 × 8	1	Y	18E6	$2k\times30ROM$	$4k \times 30$	$256\times24\times2$	64k × 24	Shared	PGA ver expands; PQFF does not
	MB86224	75	0	1	_	18E6	$2k\times30ROM$	_	$256\times24\times2$	128k × 24	Shared	IIC serial bus for audio
	MB86232	75	1 × 32	2	Υ	24E8	512 RAM + 1k × 32 ROM		512 × 32	$1M \times 32$	Shared	IEEE 754 format
Motorola	DSP96002	50	2 × 32	2	Υ	24E8 (IEEE)	1088 × 32 ROM	4G × 32	512 × 32 × 2	$4G\times32\times2$	None	Dual 32-bit ports
NEC	μPD72230	150	1	1	N	24E8 = 47E8	$2k \times 32 \text{ ROM}$	8k × 32	256 × 32 × 2	8k × 32	1k × 32	Double precision; EPROI version
	μPD77240	90	0	0	N	24E8 = 47E8	$2k \times 32 \text{ ROM}$	$64k \times 32$	$512\times32\times2$	$16M \times 32$	$1k \times 32$	IEEE format conversion
Oki Semicon- ductor	MSM6992	100	Shared	0	N	16E6	$1k \times 32 \text{ ROM}$	64k × 32	128 × 22 × 2	64k × 22	Shared	
	MSM699210/15	100	Shared	1	N	16E6	$2k\times32ROM$	$64k \times 32$	$256\times22\times2$	64k × 22	Shared	-15 only has serial I/O
TI	TMS320C30	60	Shared	2	Υ	24E8	$2k/4k \times 32$ RAM/ROM	16M × 32	1024 × 32 × 2	16M × 32	Shared	2 timers and 2 bus inter faces
	TMS320C31	75	0	1	Υ	24E8	$\begin{array}{c} 2k/4k\times32\\ RAM/ROM \end{array}$	$16M \times 32$	Shared	16M × 32	Shared	2 timers and 1 bus inter face
	TMS320C40	40	2 × 32	6	Y	24E8 (IEEE)	$\begin{array}{c} 2k/4k\times32\\ RAM/ROM \end{array}$	4G × 32	Shared	Shared	4k × 32	6 data communication ports
Toshiba	T9506	100				24E8		32k × 16	17	512 × 512 × 32	-	Aimed at image process ing
Zoran	ZR34525	80	1	0	Υ	24E8 (IEEE)	None	16M × 32	128 × 32	16M × 32	256 × 32	# Handles complex mat

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DSP TECHNOLOGY TRENDS

ment systems that required painstaking programming, equivalent to writing microcode.

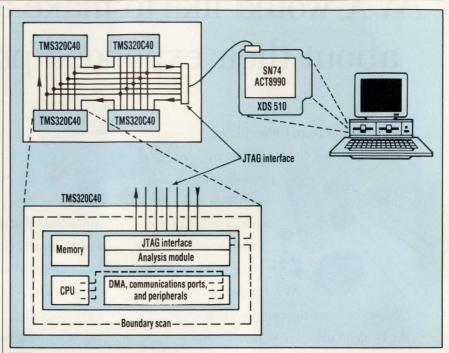
Building-block-based designs have continued to be used where designers must optimize the processing architecture down to the smallest computation function. Their functionality over the past two decades has improved as higher integration levels have allowed more functionality and larger word sizes to give designers more flexibility.

Today, many of those building blocks still exist as standalone chips, albeit with advanced features and larger word sizes (24-, 32-bits, and so on). More than half a dozen chip makers supply and still develop additional building blocks. GEC/Plessey, Harris Semiconductor, Stanford Telecommunications, and TRW LSI Products are prominent suppliers of building-block multipliers, multiplier-accumulators, correlators, numerically-controlled oscillators, and other functions.

Though the blocks can be purchased as standalone chips, they're now also commonly found as macrocells in many companies' gate-array or standard-cell design libraries, or compiler and synthesizer toolkits—such as offered by Harris, LSI Logic, GEC/Plessey, or VLSI Technology. With such libraries or tools, designers can create their own function-oralgorithm-specific IC, optimized to solve their DSP problem.

Dedicated DSP functions (hardwired algorithms) date from the late 1970s and very early 1980's, when the building blocks started to combine on one chip. Such chips as complex multipliers, correlators, fast-Fourier and discrete-cosine transform processors, finite-impulse response filters, and others started to show the practical implications of affordable DSP functions. They ran through the computations faster than minicomputers and general-purpose microprocessor-based systems, and cost many times less.

Such algorithm-specific ICs are still emerging as popular off-theshelf functions, and are also available as part of ASIC design libraries. As off-the-shelf products, digital fil-



4. DESIGNED FOR USE in multiprocessor systems from the start, the TI TMS 320C40 includes a JTAG test port that can be employed by a PC-hosted JTAG controller card to debug arrays of the DSP chips. The card, in turn, enables the PC to display multiple activity windows, one for each DSP chip, and control the operation of the DSP chips.

ters are readily available from Harris, Inmos, LSI Logic, and Zoran. One typical filter of this ilk is the HSP43881 that Harris manufactures as a licensee of the Zoran architecture. The chip contains eight filter cells, each containing various registers, multiplexers, and an 8-by-8-bit multiplier with 26-bit internal accumulation. Able to operate at sample rates of 30 MHz, the chip can perform real-time processing of 8-bit digital-video signals.

By employing two chips—a discrete cosine transform processor (the ZR36020) and a compression/decompression processor ZR3603X)—Zoran, with Fuji Film Co. of Tokyo, Japan, created a videocompression subsystem. The twochip set allows Fuji to build a handheld still-image filmless video camera that can store compressed images on nonvolatile memory cards (Fig. 3). The camera captures images through a solid-state image sensor, then digitizes the image and stores the digital image in a buffer. The DCT chip next processes the image data, and the compressor squeezes the file by a factor of 20 or more. When used as a playback unit, the coder chip decompresses the data and the DCT restores the digital data for playback through a DAC.

Dedicated chips for image compression are a hot subject today due to the interest in the consumer and computer markets in multimedia and digital-video-interactive (DVI) systems. Image compression/decompression chips are now all rallying around the Joint Photographic Experts Group (JPEG) standard for still images and the Motion Picture Experts Group (MPEG) standard for motion video. Although the first-generation Zoran coder chip isn't JPEG-compatible, the company plans to offer a JPEG version.

About a half dozen companies have developed dedicated chips or chip sets to perform lossy image compression. The chips enable users to compress digitized video images with ratios from 1 to 100, reducing multi-megabit image files to just a few hundred kilobits. Above compression ratios of about 30:1, however, the lossy process starts to pro-

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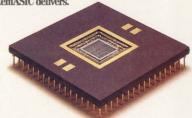
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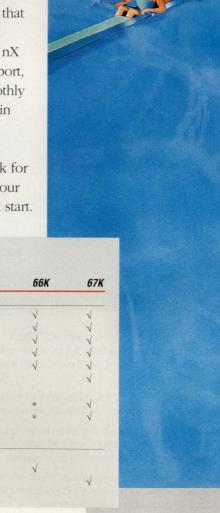
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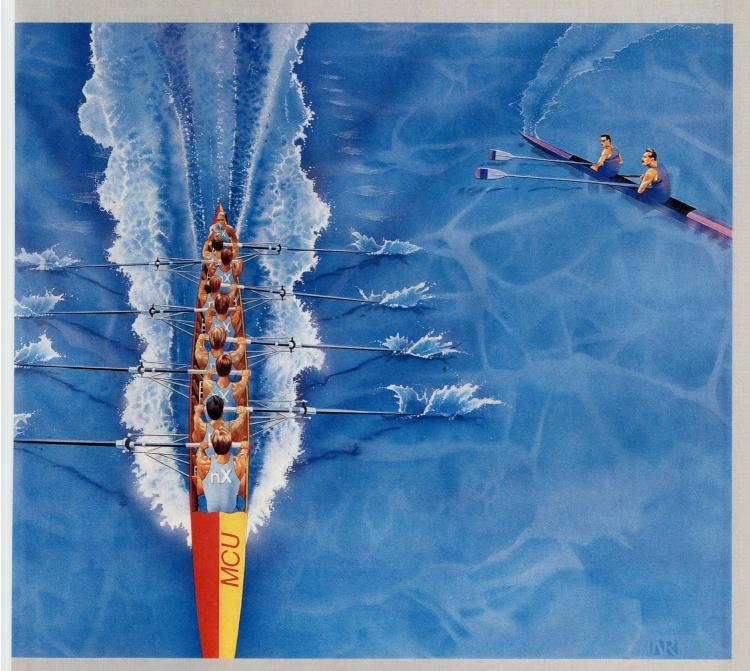
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DSP TECHNOLOGY TRENDS

duce noticeable image deterioration. Large amounts of computational power—at least several hundred million operations per second—are needed to perform such compression and expansion operations so that video can be handled in real time.

One of the first companies to offer such a dedicated chip was C-Cube Microsystems, with its CL-550. Several other companies have also developed chips that can perform similar functions to meet the standard (Table 2). Some of the JPEG chip suppliers include Integrated Information Technology, LSI Logic, SGS-Thomson, and UVC. Application-targeted DSP chips from these companies will see continued growth as design tools improve and more companies add the key cells to their design libraries. Of course, some of the high-end general-purpose DSP chips can also perform JPEG/MPEG compression or decompression. However, they may not have the throughput to necessary for real-time operation.

Other products also incorporate dedicated DSP functions. They include end products, such as data and facsimile modem chips (offered by Rockwell International, Sierra Semiconductor Corp., and Yamaha's Systems Technology Center); speech recognizers and synthesizers (available from NEC, Oki, TI, and several others); speech processing like that done by the DSP Group; image recognition processors (robotic vision systems), such as developed by LSI Logic and SGS-Thomson; echo can-

celers; and many others.

General-purpose, standalone DSP chips have been around about as long as dedicated-function DSP chips: In 1978, Gould-AMI (then known as American Microsystems Inc.) introduced what most designers agree was the first commercial single-chip programmable DSP IC, the S2811. However, the chip, intended to operate as a peripheral to a host processor, turned out to be unmanufacturable due to the hard-to-control, proprietary, V-groove MOS process AMI had used. It wasn't readily available until it was redesigned for standard NMOS processing in 1983.

Both NEC and Texas Instruments already gained footholds with DSP chips that could operate as standalone components by the time the NMOS 2811 appeared. The $\mu PD7720$ series from NEC and the TMS32010 from TI were 16-bit integer processors that performed 16-bit multiplications in less than 300 ns-an unheralded speed for a microprocessorlike chip (in 1982, a 16-by-16-bit multiplication on a 16-bit microprocessor required upwards of 60 clock cycles, which translated into a time of tens of microseconds).



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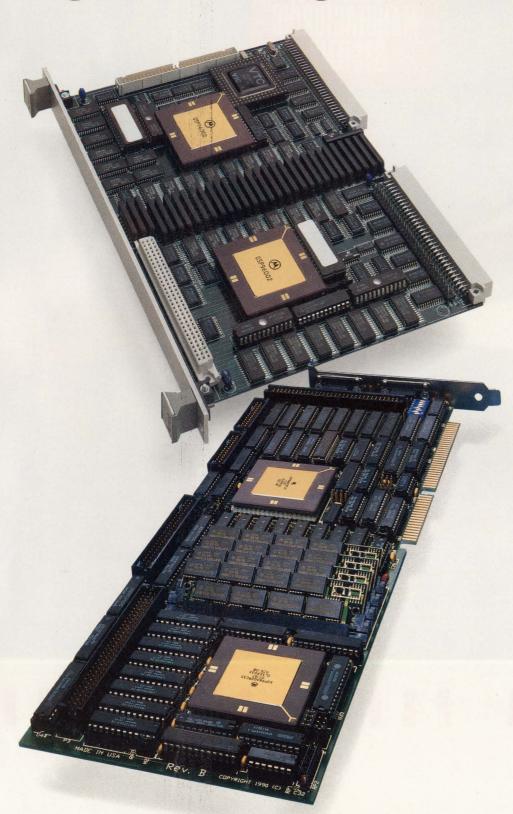
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DSP TECHNOLOGY TRENDS

The past ten years have seen dozens of chip architectures released for DSP chips with 12-, 16-, 20-, and 24-bit word sizes (Table 3), and floatingpoint DSPs with mantissa and exponent formats of 16E6, 18E6, and 24E8 (Table 4). Most designers, though, have settled on using the standard 24E8 (32-bit) IEEE floating-point format.

Close to a dozen companies claim to offer "dedicated" but generalpurpose DSP chips, a la the TMS320 series and others. In addition to the basic chips in the respective families, a number of suppliers—notably Analog Devices, AT&T, and Motorolahave already released applicationoptimized versions of their 16-bit integer DSPs. Those chips include ADC and DAC blocks, plus other features to optimize their functionality for cellular-radio applications.

Suppliers have also placed the core processor used in many of the DSP chips into their standard-cell design libraries so that application-specific versions of DSP chips can quickly be generated. Texas Instruments, for example, has its integer DSP core available and offers two levels of customization. The simplest level just custom configures the amount of RAM or ROM on the chip. The more complex option enables the entire resource mix to be altered with such functions as serial ports, timers, ADCs, DACs, and so on, which are incorporated or removed as needed by the application.

Adding to the proliferation of options, both National Semiconductor and Zilog have now released microcontrollers that also include a special DSP-oriented sub-block that packs fast multiplication, single-cycle instruction execution, and other functions. A few years back, MicroChip (then General Instrument) and Texas Instruments took the opposite tack and added microcontroller fea-

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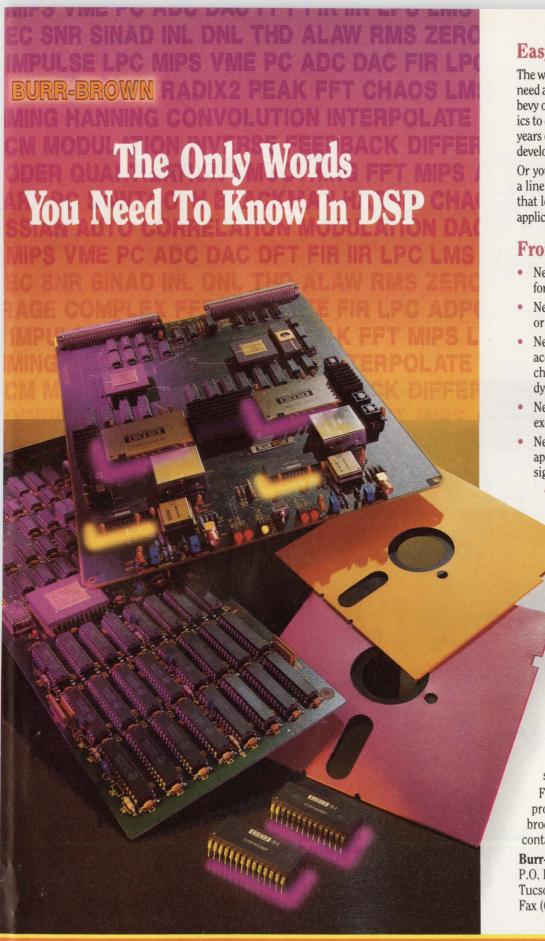
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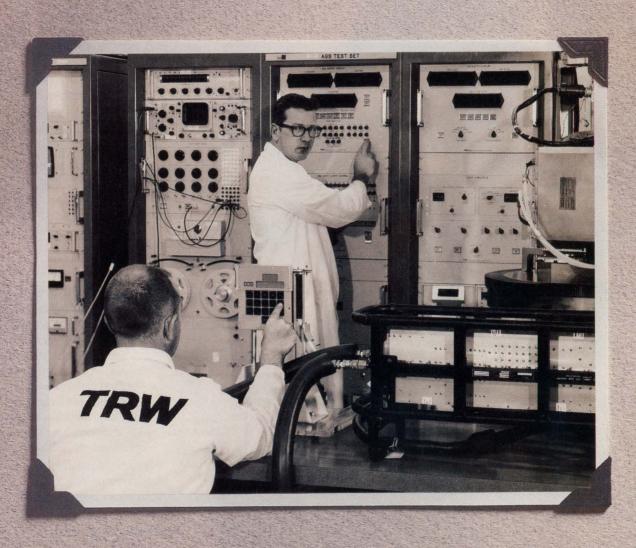
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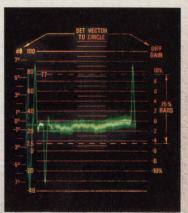
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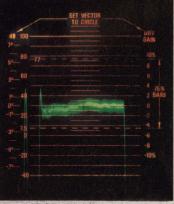
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tures to the 16-bit TMS32010 DSP chip to solve some of the same issues that National and Zilog are focusing on in 16- and 8-bit controllers.

Even RISC CPU vendors have found their chips in many signal-processing and graphics applications. The Am29000 family from Advanced Micro Devices, for instance, which has targeted many embedded-control applications, offers a significant number of applications in image pro-

cessing—especially chips like the Am29050 RISC processor with onchip 32-bit floating-point capability. These applications and chips have begun to blur the line between what is or isn't a DSP chip.

In the world of high-performance DSP applications, designers are moving en masse toward parallel processing as a means to accelerate algorithms and improve application performance. Multiple general-pur-

DSP TECHNOLOGY TRENDS

pose DSP chips are already being applied by several companies in graphics accelerators and multimedia hardware. For example, Silicon Graphics, IBM, and Hewlett-Packard all employ arrays of TMS320C30 floating-point DSP chips as computation accelerators for 3D graphics. AT&T has built a pixel-processing machine out of dozens of its DSP32C floating-point DSP chips. Furthermore, Intel's i860 superscalar processors have also found their way into graphics applications, thanks in part to their high-performance, onchip floating-point units.

However, most of the current DSP chips were not meant for multiprocessor environments because they typically require some external coordination and control logic. One of the first chips to focus specifically on the multiprocessor environment, the TI TMS320C40, contains many on-chip features, including four serial I/O links and large on-chip memories that suit it to parallel-processing environments.

When designing multiprocessor systems, one of the biggest issues is the software development problem-debugging multiple processors and not having to set up a large rat's nest of in-circuit emulators, cables, logic analyzers, and other test hardware. When developing the 320C40, TI engineers found that by adding a JTAG (Joint Test Advisory Group) standard test port and controller, they could not only control and observe the operation of every chip in a multiprocessor system, but also test each chip and use the port to download control software.

To control the array of DSP chips, the JTAG ports are all interconnected to a parallel debugger card, the XDS 510, which also contains a JTAG controller on one side and a PC-bus interface on the other (Fig. 4). That card then plugs into a PC, and software that runs on the PC controls the card and enables multiple windows to be displayed. Each window provides a view into one of the processors in the array. That promises to drastically reduce the complexity of developing parallel processor systems. Another special block that de-

ELECTRONIC DESIGN REPORT

DSP TECHNOLOGY TRENDS

signers included on the 320C40s works with the JTAG port on the DSP chip. That block consists of an analysis module that supplies separate on-chip breakpoint comparators for program, data, and DMA accesses; a program discontinuity trace stack; and an event counter for benchmarking and profiling.

Just hardware alone isn't sufficient enough for algorithm development in parallel-processing applications. To solve some of the development problems, Comdisco is developing extensions to its signalprocessing workstation to help engineers parallelize DSP algorithms. The Multiprox software will let users "cut apart" code and distribute the functions over multiple processors, and automatically generate each processor's code and insert interprocessor communication links. Further out, Comdisco expects to add more intelligence to the software so that it can automatically partition the code, eliminating manual designer intervention.

Parallel processing at the chip level has also been designed into a number of chips. Several years ago, designers at United Technologies Microelectronics Center created a computation-oriented chip containing three floating-point multipliers and a pair of accumulators so that multiple computations could be done simultaneously. Array Microsystems also produced a high-throughput twochip set—the a66110 and 210—aimed at fast Fourier transforms and other key signal-processing computations. Systolic chips from ITT Semiconductors (the DataWave processor), NCR, (the GAPP), Oki, and Oxford Computer were released in the late 1980s through 1990, but all suffered from the lack of good software development tools to create or map the algorithms across the array of processing elements. That, in turn, limited their popularity and kept them out of widespread use.

New classes of processor chips geared for high-throughput parallel processing, such as the iWarp processor from Intel, can communicate over eight serial ports for an aggregate transfer speed of 320 Mbytes/s, somewhat akin to the serial channels on the recently released Inmos T9000 transputer. One iWarp processor performs 20 MFLOPS of single-precision and 10 MFLOPS of double-precision floating-point computations, and has an architecture optimized for fine-grain computing as typically found in real-time signal- and imageprocessing applications. Combining floating-point and RISC architectures on one chip, designers at Micron Technology created a chip, dubbed the FRISC, that delivers 80 MFLOPS of double-precision computations and can be used in multiprocessor arrays. The first details of the chip were recently unveiled at the IEEE "Hot Chips" Symposium at Stanford University, Stanford, Calif.

One company that hopes to break through the programming barrier to parallel processing is Star Semiconductor, a newcomer to the DSP field. Its entry into the market combines a powerful multiprocessor chip, the SPROC-1000, and a suite of easy to use software development tools (see "Parallel-Processing DSP Chip Delivers Top Speed," p. 43). The tools were designed to let designers take for granted the details of code generation and scheduling that typically consume valuable design time and energy. The chip contains multiple, programmable, general-signal processors that surround a multiported, shared data space and shared program memory. Data-flow managers direct data exchanges among the multiple serial I/O ports, memory, and signal-processing blocks.

In addition to an array of software-development tools, SPROC's designers included a dedicated serial port for the tools on the chip, as well as a software-addressable built-in probe that consists of an 8-bit DAC and a serial output port. Under the control of the SPROC drive software, any internal signal in the implemented system can be accessed for display or measurement. □

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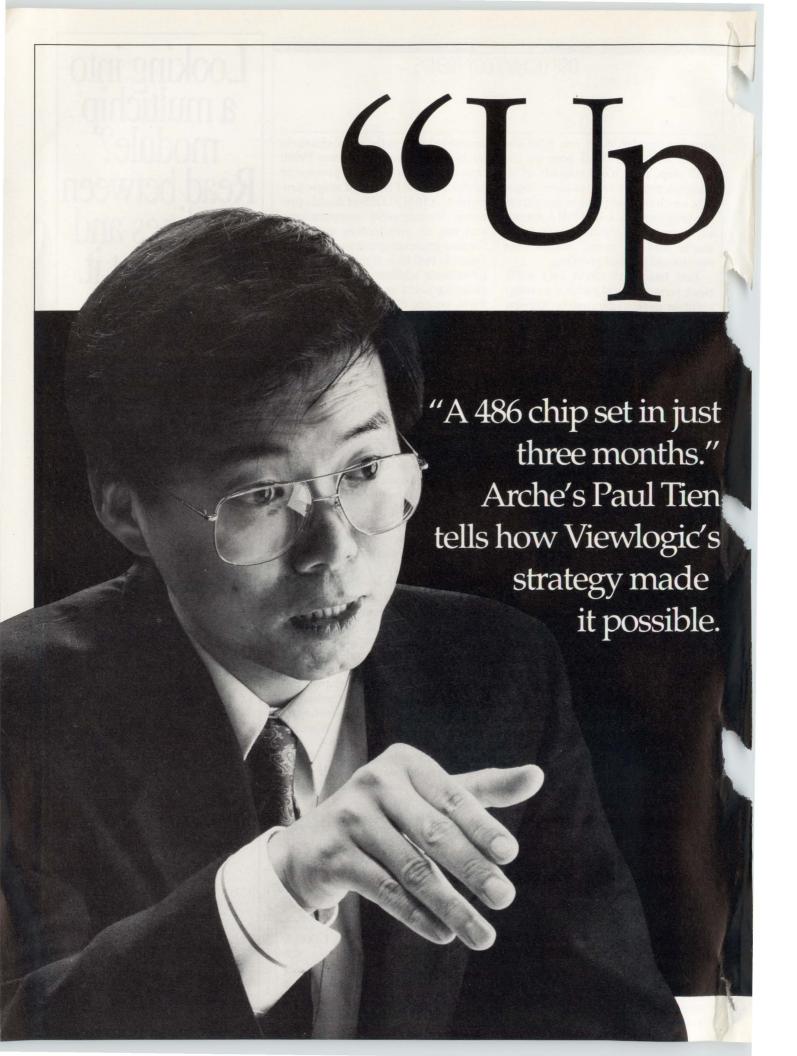
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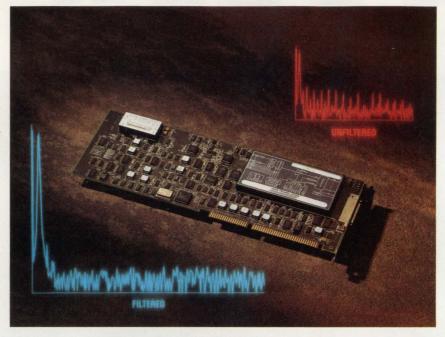
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s many designers have learned the hard way, electromagnetic interference (EMI) problems often crop up when a design's near completion. Often, the major contributors to EMI problems are radiated emissions from cables carrying digital data. The cables may be internal, or they may connect separate components of a computer system. To make matters worse, it's very difficult for designers to predict whether these emissions will cause the product to fail its final radiated emissions test. At this point, a solution may be costly and could delay a product's introduction.

A relatively simple benchtop measurement, however, enables designers to estimate worst-case radiated emissions. Although the actual farfield emissions will likely differ significant to the control of t

nificantly from this estimate, the technique can predict possible EMI problems early in the development process. And it's always better to have a solution in reserve, rather than trying to remedy the problem late in a tight development schedule.

The procedure uses a current clamp and a spectrum analyzer to measure the commonmode RF cur-

rents on the suspect cable. Then the cable is modeled as an ideal dipole antenna, for which the designer can easily calculate the electric field that might result in an open-area test site. Although this estimate may have significant errors, it's fast and easy and can alert designers to possible problems.

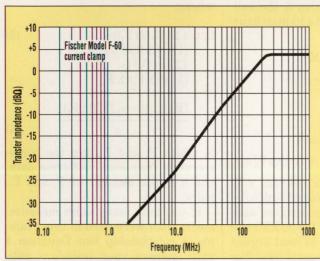
The first step is to measure the RF current on the cable, which you can easily accomplish with an appropriate current clamp. A current clamp is a device with a transfer function that relates a measured voltage to the net current flowing through the conductors in the center of the clamp. A receiver or spectrum analyzer connected to the clamp's output measures the voltage. Because the receiver or analyzer usually has a $50-\Omega$ input impedance, the clamp's transfer impedance is:

$$Z_t = V_o / I_c \tag{1}$$

where $V_{\rm o}=$ the measured output voltage for a 50- Ω termination, and $I_{\rm c}=$ the current passing through the center of the clamp. Current-clamp manufacturers may specify the transfer function in graphical form, with the transfer impedance expressed in decibels relative to one ohm (Fig. 1).

Next, you can model the cable as an ideal dipole carrying the measured current. Equations for the electric field at some distance from a dipole in free space are presented in a number of books. Les Because the designer wants to know the field's magnitude when the dipole is oriented for maximum radiation in the direction of the receiving antenna (that is, the worst case), an appropriate equation is:

$$E_{\text{max}} = (2\pi \times 10^{-7}) \frac{f I_o L_e}{r}$$
 (2)



1. A CURRENT CLAMP'S transfer function relates a measured voltage to the current flowing in the conductors surrounded by the clamp. The transfer function is often specified graphically in decibels relative to one ohm.

ESTIMATE AND CORRECT EMI

where E_{max} = the maximum electric field in volts/meter, f = the frequency in hertz, I_o = the RF current in amps, L_e = the effective length in meters, and r = the distance to the measuring antenna in meters.

The effective length is the length of an equivalent dipole with a constant current distribution. When estimating the worst case EMI, the safeest approach is to assume that the data cable's effective length equals its physical length. In some cases, however, a shorter length might render a better estimate.

For example, an ideal dipole will have a triangular current distribution if the dipole is electrically short. Short means the antenna's overall length is small compared to the wavelength of interest. The physical length must be one-tenth of a wavelength, or less, usually. In this case, the effective length is exactly half the physical length. That means the dipole radiates like a dipole half its length but with uniform current. Data cables may also behave in this manner.

CREATING A SHORT DIPOLE

Short dipoles with nearly uniform current distributions can be built by adding capacitive loading to each end. The load usually takes the form of a circular end-plate or wire array perpendicular to the dipole. In a data cable, the assemblies connected to each end can act as capacitive loads for the dipole-like cable. Therefore, the current in a short data cable may be equally distributed along the cable's length, so that the effective length is roughly equal to the cable's physical length.

To conform to regulations for commercial EMI tests, Equation 2 must be multiplied by two. The reason is that such tests are done over large ground planes, with the receiving antenna height adjusted to maximize each received signal. As a result, the EMI that travels directly to the receiving antenna is added constructively to the reflection from the ground plane.

Also, for convenience, the frequency can be expressed in megahertz and the current in microamperes (or the clamp output voltage, V_c , in microvolts). Because these changes complement each other, no conversion factor is needed. However, it's also more convenient to calculate the field in microvolts/meter, so Equation 2 should be multiplied by 10^6 . Combining these changes with Equation 1, the equation for the worst-case electric field in microvolts/meter becomes:

$$E_{\text{max}} = \frac{1.26 \text{f V}_{c} L_{e}}{Z_{t} r}$$
 (3)

This technique was demonstrated on a 0.9-m-long digital cable connecting a PC to a peripheral device. The computer was operated in a typical, but repetitive, manner to minimize emission variations. The current clamp was placed around the cable (Fig. 2). For increased sensitivity, the clamp's output went through a small broadband amplifier (an HP 10855A) before entering the spectrum analyzer (an HP 8591A). The measurement used video averaging to approximate the averaging that occurs in final EMI open-site tests.

One of the measured signals had an amplitude of $30.4~\mathrm{dB}\mu\mathrm{V}$ at $203.7~\mathrm{MHz}$. Subtracting the amplifier's 22-dB gain from that level gives the current clamp output, $8.4~\mathrm{dB}\mu\mathrm{V}$ or $2.63~\mu\mathrm{V}$. The clamp's transfer impedance at this frequency is about $3~\mathrm{dB}\Omega$, or $1.41~\Omega$. Using Equation 3, the estimated electric field at a $10~\mathrm{m}$ measuring distance is:

$$\begin{split} E_{max} = & \left[(1.26) \ (203.7 \ \text{Mhz}) \ (2.63 \\ & \mu V) \ (0.9 \ \text{m}) \right] \div \left[(1.41 \ \Omega) \\ & (10 \ \text{m}) \right] \\ & = & 43.1 \ \mu V/m \end{split}$$

Expressed in $dB\mu$, this is

 $20 \text{Log}(43.1 \,\mu\text{V/m}) = 32.7 \,\text{dB} \,\mu\text{V/m}.$

By comparing this estimate with the CISPR Class B limit of $30~\mathrm{dB}\mu\mathrm{V}/\mathrm{m}$ at 203.7 MHz, the designer sees that the product may fail its EMI site tests. The estimate at least argues for contingency preparations. For example, a shielded cable or ferrite devices that reduce RF currents could be acquired in case the more precise EMI site tests later show a

problem. These precautions could save lots of time.

To expand on this example, 15 strong currents on various cables were measured using the same system. The estimated electric fields were then calculated using a general-purpose spreadsheet. For the most part, the estimates, plotted along with the CISPR Class B limit, were higher than actual open-area test-site (OATS) measurements (Fig. 3). So, although the estimates are significantly off in some cases, the errors are generally on the conservative side.

LOOKING FOR PATTERNS

A plot of the errors (the estimated emissions minus the measured emissions) shows that a pattern seems to exist (*Fig. 4*). Therefore, some curve fitting was tried in an attempt to develop simple equations that could define the relationship.

A logarithmic equation seemed to work best, but the data scattering makes this a very rough fit. The curve fitting started with the equation for a simple least-squares fit to a straight-line equation.⁴ The natural log of the frequency, F, was substituted for x in this equation, which then became:

$$E_r = b_o - b_1 (\ln F) \tag{4}$$

where:

$$b_{1} = \{ \sum [E_{ri}(\ln F_{i})] - (1/n)[\sum (\ln F_{i})](\sum E_{ri}) \} \div \{ \sum [\ln F_{i})^{2}] - (1/n)(\sum F_{i})(\sum F_{i}) \}$$
(5)

$$b_{o} = \frac{[R (E_{ri})] - b_{1} [R (\ln F_{i})]}{n}$$
(6)

in which F_i and E_{ri} are the corresponding frequency and error data, and n is the number of F_i and E_{ri} pairs.

If you take many more measurements than were used in this example, a relationship like Equation 4 may improve your emissions estimates. By fitting the errors to a suitable equation, you can calculate a correction factor that can be applied to estimates. This should narrow the

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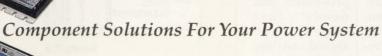


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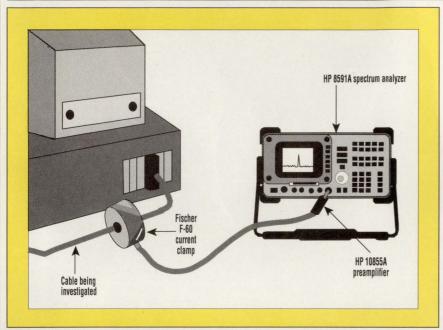
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2. IN THIS EXAMPLE TEST SETUP, the current in a cable linking a personal computer to a peripheral device is measured by a current clamp. The computer was operated in a typical, but repetitive, manner to minimize variations in emissions.

gap between the estimates and the open-site results. The basis for this assertion is certainly circumstantial, but the purpose here is simply to make an educated guess.

If you determine that a cable in your system or device may fail an EMI site test, there are several things you can do, or prepare to do, to solve the problem. Equations 2 and 3 show that the only parameters you can really control are the cable length and RF current on the cable. If you can shorten the cable, by all means do it. But a big change is required to make much difference. For example, cutting the cable length in half will reduce the field by only half, or 6 dB.

You're far more likely to make a significant improvement by reducing the RF current. The most cost-effective tack is to reduce the current at the source as much as possible. The first questions to ask are: Where does this current come from, and why is it there now? Then you can look at the cable for ways to reduce its current.

The current's source will very likely be on a pc board filled with ICs and other components. If the EMI is a

harmonic of a clock frequency, look for ways to slow the offending clock's rise and fall times to only what the system needs to function. A resistor in series with the clock output will combine with the clock line's distributed capacitance to form an RC low-pass filter to the ground plane. If the capacitance is too small, you may have to add a capacitor from

the resistor to ground. Another device that works well is a ferrite bead on a wire, instead of the resistor. A little experimentation is needed to find the right ferrite device.

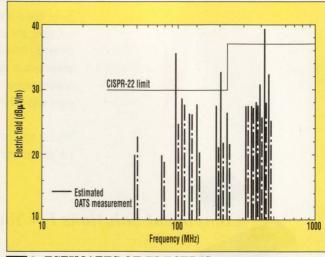
Even if the offending clock drives a microprocessor that needs fast edges, you should consider whether the rest of the circuit needs the same fast edges. If not, you can put the clock (or the clock crystal, if the clock circuit is in the microprocessor) and the microprocessor close together on the pc board, then send a slower version of the clock to other parts of the circuit. This solution also minimizes EMI generated by the current loop that connects the clock and microprocessor, because the loop area will be as small as possible.

CHOOSE SLOWER GATES

The distributed clock could be slowed by choosing gates in a slower technology. By selectively changing to devices that have the same functions and pin assignments, but are in a slower digital IC family, you can slow down the clock without increasing parts count.

You may want to save money by designing the pc board to have only two layers. But it can be very difficult to create an effective grounding system on a two-layer board. If the board can't have a separate, dedicated ground plane, a good alternative is a gridded ground. This technique uses whatever space is available to form a mesh-like ground plane on a two-layer board. Grounded nodes are multiply-interconnected by traces of whatever size will fit, intertwined on both layers between signal and power traces.

For that matter, why not have a



3. ESTIMATES OF ELECTRIC fields emitted by various tested cables generally were higher than the actual fields measured in open-area test-site measurements.



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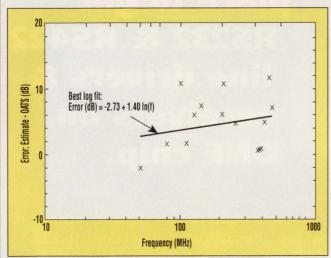
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CIRCLE 187 FOR U.S. RESPONSE

ESTIMATE AND CORRECT EMI



4. THE ERRORS IN the 15 example measurements in Figure 4 were subjected to curve-fitting techniques. This was done to try to develop a simple equation that would define the relationship between the estimates and the actual emissions.

multilayer version of the pc board ready in case it's needed? It's better to prepare a multilayer board early in the development process and then not use it, rather than find out late in the program that the design won't pass EMI tests without one.

After you've done everything possible to reduce the source of the EMI current, you can try to minimize it on the offending cable. If the cable isn't shielded, that might be a good first step. If it's already shielded, the problem may be a poor shield termination or a noisy ground driving the cable shield.

Cable shields are most effective when they completely enclose the cable. Braided shields work well, but holes in the weave limit their coverage to something less than 100%. Foil shields offer much better coverage, except that the joint where the foil edges overlap can form one long slot if the overlap isn't properly designed. Compound shields of braid over foil exploit the best properties of each. If such shields are properly designed, the foil provides nearly 100% coverage, and the braid shorts the foil seam.

However, you must be very careful how you terminate the cable shield at each end. Shielded connector housings that securely attach to the shield completely around the ca-

ble should be employed. These types of housings effectively flare a continuous shield to the connector shell, where the housings again must be securely attached to the shell. Avoid pigtails (short-wire shield-to-ground connections) if possible, because they can compromise most of the cable's shielding effectiveness and increase crosstalk.

Another key factor is to choose galvanically compatible metals. Dissimilar metals will corrode at their junction if their galvanic potentials are too far apart. A good first choice is tin plating. Tin is in the middle of the galvanic table, and its naturally occurring surface oxide breaks easily under pressure.

If you've properly shielded the cable and the EMI common-mode current is still too high, the cable may be attached to a connector with a noisy shell. That is, the connector's shell may not be at ground or at zero potential at the EMI frequency. An example might be a connector shell grounded to the pc board that the shell is attached to. The board ground may be at some RF potential other than zero. A better procedure is to securely ground the connector shell independently to the cleanest ground point available. If the pc board resides in a metal box, the box is probably the cleanest ground.

Another solution might be to attach a ferrite device around the cable to choke the EMI currents. Ferrites come in many shapes and sizes, including toroids or two-piece half cylinders in plastic holders that snap together over cables. These latter devices are frequently used on video cables for computer displays.

Ferrites, however, aren't an ideal

permanent solution because they deal with the symptoms rather than the causes of EMI. Ferrites also break easily and must be protected in some way. Consequently, you should probably use a cable-mounted ferrite only as a last resort.

But adding a ferrite can be a useful experiment. If placing the device around the cable changes the total emission amplitude seen at a distance, you know that currents on the cable were significant. If the emission drops, the cable is probably the dominant radiator. If the emission rises, chances are another radiator exists. The second radiator just happens to cancel some of the emission from the cable with the added ferrite. In this case, leave the ferrite in place, at least temporarily, and go hunting for the other radiator.

References:

¹John D. Kraus and Keith R. Carver, *Electromagnetics*, Second Edition, (New York: McGraw-Hill, 1973), 613. ²Ramo, Whinnery, and Van Duzer, *Fields and waves in communication electronics*, (New York: John Wiley & Sons, 1965), 644.

³Limits and methods of measurement of radio interference characteristics of information technology equipment, Publication 22 of the Comite International Special des Perturbations Radioelectriques, 1985.

⁴William Volk, Engineering statistics with a programmable calculator, (New York: McGraw-Hill, 1982), 141-142 and 147-149.

⁵Henry W. Ott, *Noise-reduction* techniques in electronic systems, Second Edition, (New York: John Wiley & Sons, 1988), 283-285.

Scott Roleson, an electromagnetic compatibility engineer with the Hewlett-Packard Co., San Diego, Calif., received a BSEE from Arizona State University, Tempe, and an MSEE from the University of Arizona, Tucson.

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SBL-1-1	0.1-400	5.5	35	40	+7	7.25
SBL-3	0.025-200	5.5	45	40	+7	7.25
• SBL-11	5-2000	7.0	35	30	+7	18.75
SBL-1LH	2-500	5.8	68	45	+10	5.50
SBL-1-1LH	0.2-400	5.2	64	52	+10	8.25
 SBL-1XLH 	10-1000	6.0	40	55	+10	7.25
SBL-2LH	5-1000	5.9	61	54	+10	8.25
SBL-3LH	0.07-250	4.9	60	53	+10	8.25
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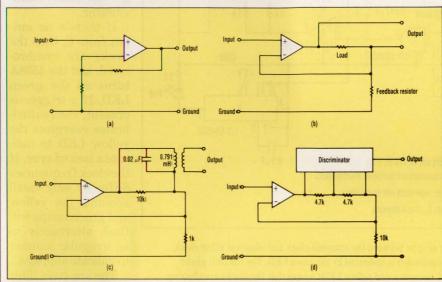
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521 USE OP AMPS WITH TUNED CIRCUITS

JOE CHAMBERLAIN

AJC Design, 72, The Lawns, Field End, Hemel Hempstead, Hertfordshire HP1 2TD England; 0442 241 470.



THE CONVENTIONAL VOLTAGE-FEEDBACK op-amp circuit isn't suitable for driving parallel-tuned circuits because of its low output impedance (a). A higher output impedance is possible with a current-feedback amplifier configuration (b). The tuned amplifier can be coupled to any desired load using transformer coupling (c). The last configuration is used to drive a frequency discriminator (d).

n certain applications, inductorcapacitor tuned circuits offer more flexibility than active-filter or digital techniques. The conventional voltage-feedback op amp, however, isn't suitable for driving parallel-tuned circuits due to its

low output impedance (see the figure, a). By reconfiguring the circuit, it's possible to produce an amplifier with a high output impedance (see the figure, b). The op amp's output then more closely approximates a current source and can drive a parallel-tuned circuit in much the same fashion as a grounded-emitter transistor amplifier stage. The advantages of the configuration are maintained, with the only problem being that the output isn't referred to ground. However, by making the inductor of the tuned circuit a transformer, the output can be coupled to any desired load—floating or grounded (see the figure, c).

For the values shown in the figure, part c, the stage's gain at resonance is 19.95 dB, the resonance frequency is 40 kHz, and the Q factor is 50. The exact type of amplifier chosen isn't crucial, but it must maintain its gain out to frequencies about an order of magnitude greater than those to which the parallel L-C circuit is tuned. To ensure compliance with that condition, an LF351 was used in the development circuit.

The stage's approximate gain at resonance is determined by the ratio of the load impedance to the current-feedback resistor. With an op amp having a high open-loop gain and a coil possessing a high Q factor, a voltage gain of nearly 20 dB (10:1) is possible for the component values shown in the figure, part c. The amplifier has proven to be stable and easy to link with other circuits, and has performed as predicted by the preliminary calculations.

With a slight modification, the circuit can be used to drive a frequency discriminator built with transformer-coupled tuned circuits (see the figure, d). \square

522 HANDY TESTER CHECKS CLOCK SYNC

CHARLES HARTLEY

P.O. Box 614, San Carlos, CA 94070; (415) 364-3367.

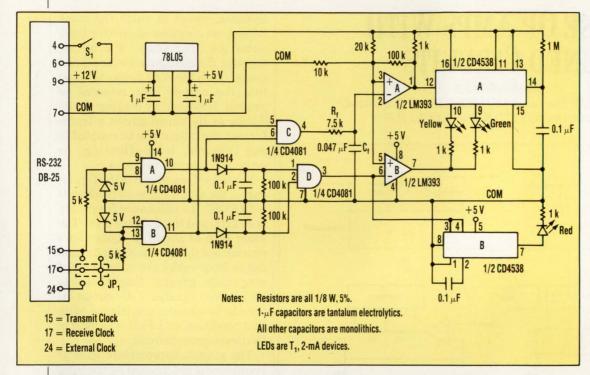
roblems in high-speed synchronous data-communications systems often result from poor synchronization between send and receive clocks. In a multiplexed full-duplex system, each channel has its assigned time slot, so that even a small amount of slippage

between the clocks can garble communication. In troubleshooting such systems, it's helpful from the outset to determine whether the trouble does involve clock synchronization.

To help with that determination, this compact tester, which is built on an RS-232 breakout adapter, instantly indicates whether the clocks are in sync, out of sync, or slipping. It also reveals whether either of them is missing. The unit is small, simple, and inexpensive, making it particularly useful for field service applications, for which an oscilloscope might be too large, heavy, or costly. It's been used at up to 128 kHz with no problems.

The tester is powered by the +12-V accessory pin (pin 9) on the DB25 RS-232 connector, through a 78L05 low-power regulator, dropping the voltage to 5 V.

Pin 15 of the connector supplies



THE YELLOW LED indicates the lack of sync between the transmit clock and whatever other clock signal is selected by jumper JP₁. Proper synchronization is indicated by the green LED. The red LED glows when either clock isn't present. A flickering of the green and yellow LEDs means that the clocks are slipping with respect to each other—that their frequencies differ by a tenth of a hertz or so.

the transmit clock, which is used as a reference (see the figure). A shorting jumper gives the user a choice for the second clock signal: pin 17 (the receive clock), pin 24 (an external clock), or pin 15 (the transmit clock to test the tester).

The clock signals are buffered by

gates A and B, and then detected by gates C and D—all of which make up a 4081 quad IC. Gate D detects the presence of the clocks, turning on the red LED if either of them is missing, and making it possible to operate the green and yellow LEDs otherwise.

Gate C detects the frequency difference between the clocks and provides a low-frequency signal, filtered by R_f and C_f, to comparator LM393A to trigger the 4538A multivibrator.

If there's no output from C, then the clocks are synchronized, and the 4538A turns on the green LED. If a trigger is present, the multivibrator energizes the yellow LED to indicate a lack of sync. If the clock frequencies differ by only small amount, the yellow and green lamps will flash alternately in an irregular manner to indicate slippage.

The low-pass filter formed by resistor R_f and capacitor C_f has

a cut-off frequency below 400 Hz, and multivibrator 4538A has a frequency of just 10 Hz, so the circuit will not respond to large frequency differences. That's no great limitation, however; its purpose is to detect frequency errors of a few hertz and slippage of a few tenths of a hertz. □

523 VOLTAGE REFERENCE HAS ADJUSTABLE TC

JOHN DUNN

181 Marion Ave., Merrick, NY 11566; (516) 378-2149.

major contributor to gray hair among electrical engineers must be components with pronounced temperature sensitivity. In many cases, those temperature sensitivities can be canceled out by the circuit presented here—a voltage reference whose temperature coefficient (TC) can be adjusted as the situation requires (see the figure). Changing the loca-

tions of R_2 and IC_3 in the figure switches the TC from positive (a) to negative (b).

Key to the voltage reference's operation is IC_3 , a temperature-dependent current source with a nominal TC of 1 μA per degree Kelvin. If its current is I_S , the voltage output of the reference is:

$$V_{REF} = 5 V \times [R_2/(R_1 + R_2)] + I_S \times$$

 $[{\rm R_1R_2/(R_1+R_2)}]$

for positive TCs, and

$$\begin{split} \mathbf{V}_{\rm REF} &= 5 \ \mathbf{V} \times [\mathbf{R}_2/(\mathbf{R}_1 + \mathbf{R}_2)] + 10 \ \mathbf{V} \times \\ [\mathbf{R}_1/(\mathbf{R}_1 + \mathbf{R}_2)] - \mathbf{I}_{\rm S} \times [\mathbf{R}_1 \mathbf{R}_2/(\mathbf{R}_1 + \mathbf{R}_2)] \end{split}$$

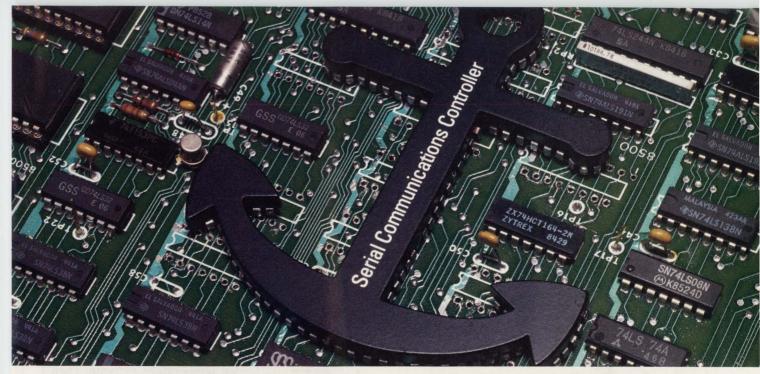
when the TC is negative.

Taking the partial derivative of voltage with respect to temperature, it can readily be seen that the TC of the circuit is:

 $\pm[R_{\vartheta}R_{2}/(R_{1}+R_{2})]\times1\,\mu\text{A}/^{\circ}\text{K}$

which is a simple function of R_1 and R_2 .

Tailoring the reference to a specific application is a simple four-step process:



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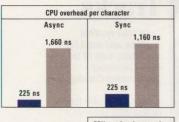
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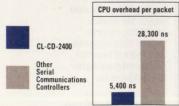
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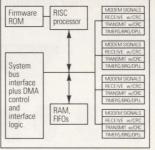
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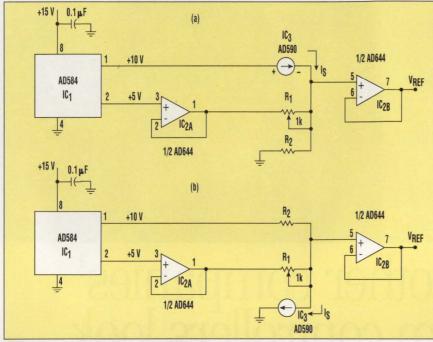
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IDEAS FOR DESIGN



THIS VOLTAGE REFERENCE can be configured to have either a positive (a) or negative (b) temperature coefficient. All of its ICs, including the temperature-dependent current source, are manufactured by Analog Devices.

1. Choose either the positive (a) or negative (b) circuit configuration.

2. Set R, to some finite value.

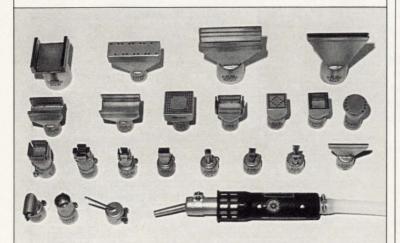
3. With the voltage reference and the target circuit at room temperature, adjust R, for zero voltage drop across R₁ or for exactly 5 V at the output (V_{REF}). For a room temperature of 25°C, R2 turns out to be about 16.78k (5 V divided by 298 μA—the nominal value of Is at 25°C). Note: standard resistor values will lead to different values for "room temperature," 30° C for $R_2 = 16.5$ k, and 23° C for $R_2 = 16.9k$.

4. Take the voltage reference and the circuit to be compensated to the intended temperature extreme. Then adjust R, so that the circuit parameter to be compensated is brought back to its room temperature value.

That's it. Following this procedure not only compensates for the temperature sensitivity of the target circuit, it does so without ever explicitly determining the circuit's precise temperature coefficient.□

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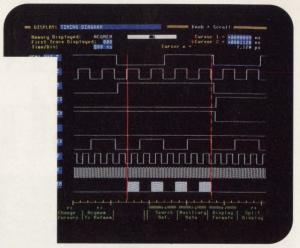
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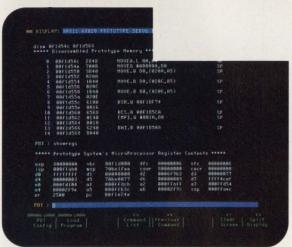
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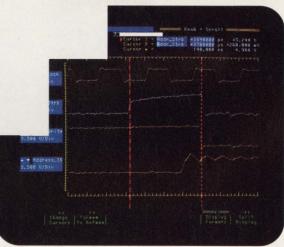
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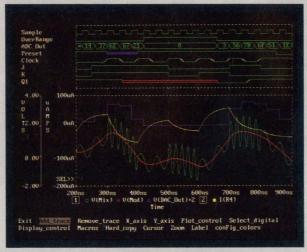
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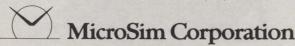
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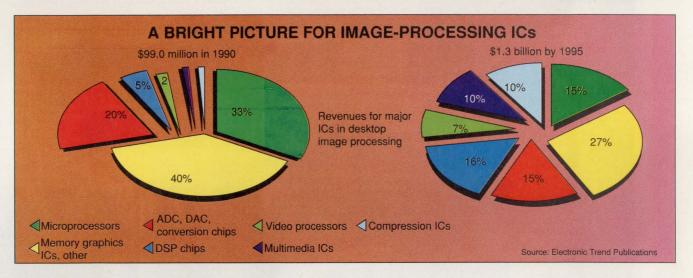
y mid-decade, image processing will likely outpace number crunching and word processing as the most popular computing application. As a result, revenues of the worldwide image-processing industry are expected to grow at a compound annual rate of 45%. Revenues worldwide, which stood at \$1.8 billion in 1990, are expected to top \$12 billion by 1995. These predictions come from Elec-

tronic Trend Publications' recently published report, Impact of Digital Signal Processing on the Semiconductor Industry.

Who can ride the crest of this wave? IC makers, for one. They supply digital and video signal processors, multimedia processors, and compression/decompression ICs. Image-processing related chips, which had revenues of \$99 million last year, should account for revenues of \$1.3 billion in 1995, says the Saratoga, Calif., market researcher.

The most sophisticated video and multimedia processors may act as microprocessors in imaging systems. Most of these systems, once housed only in mainframes, will fit on a desk. Accordingly, revenues for desktop systems are expected to grow 67% a year.

Image-processing systems are going to work in insurance, financial, commercial, and advertising sectors, which together account for 28% of systems sold; government and military systems account for another 25% of the market. Manufacturing and engineering firms use 22% of systems, with professional services companies accounting for 10% and transportation and utility industries, 8%.



TIPS ON INVESTING

he recent IBM-Apple announcement suggests a new balance of power in the PC world, as many engineering investors are aware. In the early 1980s, Microsoft, Intel, and IBM led a redefining of PCs. This time the winners may be IBM, Apple, Motorola, and buyers and end users.

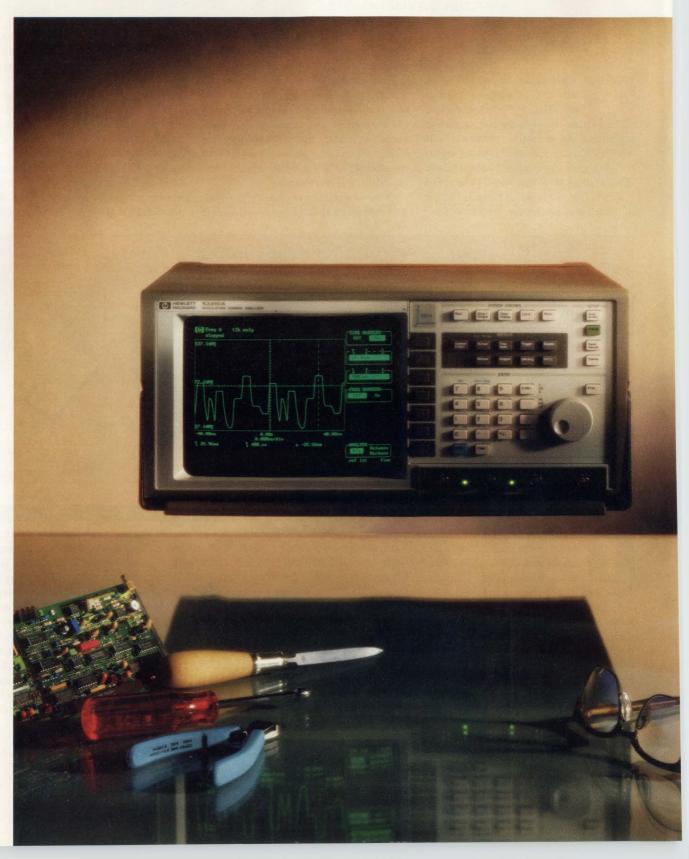
The announcement was far-reaching, affecting PC and workstation suppliers, software suppliers, and semiconductor companies. The iron triangle of Microsoft, IBM, and Intel is being challenged, as is the ACE consortium. The immediate positives are for Apple, a shift to software valuation; for IBM, a regaining of control in profitability and the PC business; for Motorola, the benefit of making a key microprocessor.

The negatives for Intel are that IBM's RISC chip is an alternative; for Microsoft, a new operating system as an alternative, and mild negatives for Sun Microsystems, Compaq, Digital Equipment, Hewlett-Packard. Compatibility is the watchword. The distinction is blurring between workstations based on the Unix operating system and RISC microprocessors and traditional PCs using Microsoft operating systems and Intel microprocessors.

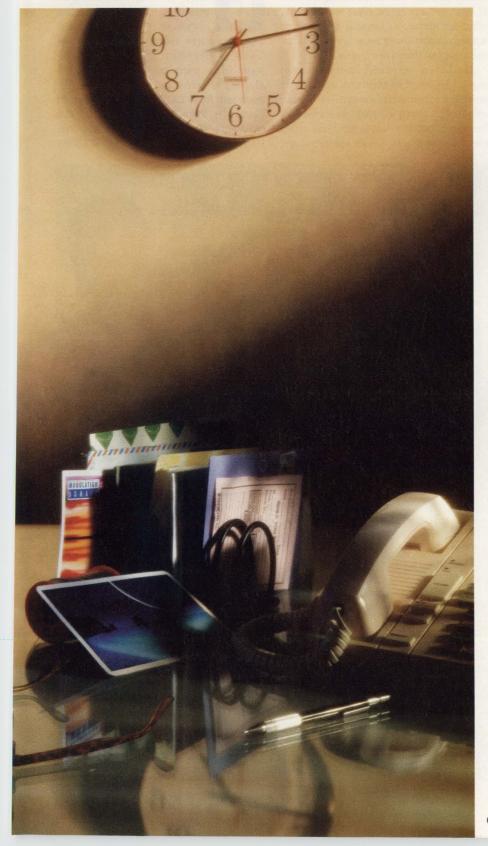
What does this all mean to engineers? Consolidation, retraining and elimination of positions all lead to lump sum distributions. The funds within your retirement plan have been growing on a tax-deferred basis. Taxes will be postponed until you withdraw the funds from your account. So, once you receive this large sum of money, you can pay taxes now—you may be eligible to take advantage of certain favorable tax rates and then, use or reinvest the balance as you wish. Or if you don't need the money, you can deposit it into an IRA rollover account within 60 days of receipt of your distribution, which allows the full value of your retirement funds to continue to grow tax-deferred. Or you may elect to roll over only part of the distribution into an IRA, but you must pay income taxes on the amount you keep, at ordinary rates. For a free copy of "Making the Most of Your Lump Sum Distribution," a Shearson Lehman publication, call or write to me.

Henry Wiesel is a financial consultant for Shearson Lehman Brothers, 1040 Broad St., Shrewsbury, NJ 07702; (800) 631-2221 or (908) 389-8653.

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QUICKLOOK

QUICK REVIEWS

ome keys to success in Japan are revering the customer as God; controlling your own destiny; researching and manufacturing the right product for Japan; and building a world-class organization and management. These conclusions are drawn from a new book, Cracking the Japanese Market, by James C. Morgan and J. Jeffrey Morgan.

Rather than yet another book on how U. S. industry has lost its competitive edge to Japan, Cracking the Japanese Market asserts that the Japanese have redefined the global marketplace. To succeed in this new marketplace, U. S. firms must learn to compete and win against the Japanese in Japan.

The authors back their assertions with examples from their own experience: James C. Morgan is chairman of Applied Materials Inc., a maker of semiconductor processing equipment, which does nearly 50% of its business in Japan. J. Jeffrey Morgan, James's son, worked in Tokyo at Mitsui & Co., which is Japan's oldest conglomerate.

Authors Morgan are frank about the mistakes they made and acknowledge the real difficulties Americans face doing business in Japan. Still, success in Japan is not only possible, they write, but also leads to overall excellence within a company and success in world markets.

The book is published by the Free Press, New York, 1991. (ISBN 00-02-921691-5) \$24.95.

Everything You Ever Wanted To Know About Business Otsukiai: A Guide to Japanese Business Protocol

Business Otsukiai is a guide to the practice of getting along in Japanese business society. Compiled from the advice of Japanese managers, the book sets forth guidelines for appropriate behavior in myriad business situations—from setting up appointments to sending gifts all the way to building a consensus for a business proposal.

Practical and specific—"don't keep business cards in a back pocket—" the book gives an unguarded look at behavior in corporate Japan (Japanese executives were identified by last initial only).

Business Otsukiai is essential reading for those doing business in Japan. For other readers, it's a fascinating look at the behavioral underpinnings of another culture.

James V. Reilly translated and edited the book, which was compiled by NTT Mediascope and published in the U. S. by HCI Publications, 50 East 42nd St., Suite 1501, New York, NY 10017-5495; (800) 472-1666; fax (212) 557-5975. (ISBN 0-9628775-0-6)

OFFERS YOU CAN'T REFUSE

macromodel library is being offered free for Advanced Linear Devices' family of CMOS op amps—CMOS, rail-to-rail low voltage, low power, and micropower. Intended for any Spice simulation environment, the op amp macromodels feature the basic effects of input voltage range, input bias currents, input impedance; differential and common mode gain; open loop gain, output impedance; rise time, fall time, and overshoot.

The library can model input and output characteristics of op amps such as extended input and output voltage ranges (rail-to-rail operation), change in ouput impedance as a function of output voltages, input and output clamp diodes, output voltage, and output cur-

rent limiting effects, and input/output ac characteristics.

For the disk, contact ALD at 1180F Miraloma Way, Sunnyvale, CA 94086-4606; (408) 720-8737; fax (408) 720-8297. CIRCLE 451

raphical user interfaces, or GUIs,

are cropping up everywhere, especially for the Unix operating system, much to the confusion of some computer users. The UniForum Guide to Graphical User Interfaces explains GUIs (pronounced gooeys) and has a glossary of terms and acronyms. The GUI guide sells for \$19.95. Contact UniForum, 2901 Tasman Dr., Suite 201, Santa Clara, CA 95054; (408) 986-8840; fax (408) 986-1645. uunetluni4um1ed.

...Perspectives on Time-to-Market

BY RON KMETOVICZ

President, Time to Market Associates Inc. Cupertino, Calif.; (408) 446-4458; fax (408) 253-6085

n the last column, a change of managerial roles was discussed. In this column, we'll take a brief look at actions that can be taken when the team's composition changes during the execution phase. You do not know who will leave or when an exit will take place. But it's reasonably certain that it will happen at some point in time to almost every new product development effort. Usually the departure of a team member is preceded by an early warning signal—sometimes the departure is abrupt. In general, the departure of a team member is a problem that cannot be backed up with a contingency plan because most organizations don't have a surplus of human resources. It is, however, a problem that can be quickly resolved (frequently without milestone impact) with the aid of simple tools and techniques.

Two primary solutions to the problem exist. The first is to assign the departing individual's work to a replacement; second, the work can be distributed to others on the team without adding additional resources. Also, a combination of the two might be appropriate. If the model of the project's execution phase was constructed correctly, determination of how to adjust to the change is easy to accomplish. To determine the best approach, use departing individual's "to-do" list and the project's database.

The to-do list of the exiting team member records all his/her remaining activities ordered by scheduled completion date. Each task on the list is assigned to another resource and the impact on time to market is calculated. Doing this work is very easy now that the project's network model is in minimally serial form. Once assignments are made, the tools leveling algorithms are utilized to ensure that the redistribution of work is realistic. More often then not distribution of work between existing project members increases time to market. If the added delay is unacceptable, a replacement from within the organization must be identified. The project manager, with help from advisers, then takes into account the skills of all team participants and effectively redistributes work between existing members of the team and those who were recently added.

With the to-do list and a properly structured project database, it's clear to see an effective way to work with the problem, yet many organizations decide to deal with this situation by relying on intuition and luck. A to-do list and database make it possible to achieve time-to-market objectives under changing resource conditions. Relying on luck and intuition will surely lead you down the long road.



QUICKLOOK

	1991	1990	
Unix System V	52.2%	52.3%	
SCO Unix	37.7	in "other" categor	
SunOS	35.2	31.9	
Xenix	25.8	26.9	
AIX	23.0	11.7	
HP UX	21.4	14.3	
Ultrix (DEC)	19.2	17.0	
Interactive Unix	15.4	in "other" categor	
A/UX (Apple)	9.1	7.6	
Other	10.7	15.5	

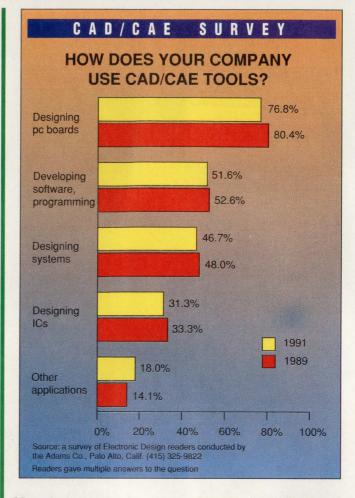
The Unix operating system is winning converts among technical and managerial types. A survey of 600 members of UniForum shows that 93.1% use Unix. But 81.1% of them still run DOS. SCO Unix is gaining ground. Whereas in 1990 SCO's version of Unix fell into the "other" category, along with 25 other brands, in 1991, 37.7% of those surveyed reported using SCO Unix. Also, 45.9% plan to upgrade to Unix System V.4 and 16.3% to OSF/1. And 17.4% plan upgrades to both operating systems; 20.4% don't plan upgrades to either.

HOT PRODUCTS

frequency detector/counter from Optoelectronics Inc. has a dynamic range of 1 MHz to 2.4 GHz and sells for less than \$100. The Handi-Counter Model 2300 has sensitivity of 10 mV that holds through 900 MHz for use with cellular phones. The unit also has an eight-place readout that holds up all the way to 2.4 GHz and a display-hold switch to keep the detected frequency in view.

The frequency detector's low price derives from its low parts count and design for manufacturability, the company says, including use of the same PC board and aluminum housing from another one of its products. The frequency counter, one of just two ICs in the unit, is built in CMOS. The other IC, an ECL frequency scaler, affords gigahertz operation. Dual MMIC amplifiers support the input circuits. Trimmer capacitors with expensive NPO dielectrics are used in the oscillator circuits.

The Model 2300 sells for \$99 apiece in quantity. Delivery is from stock. An optional NiCad battery pack is \$29, also from stock. Contact Optoelectronics, 5821 NE 14th Ave., Fort Lauderdale, FL 33334; (800) 327-5912 or (305) 771-2050; fax (305) 771-2052. CIRCLE 453



More than ever, engineers are relying on CAD/CAE products to design systems and equipment. To find out how engineers are working with CAD/CAE, the Adams Co. surveyed 1020 *Electronic Design* readers earlier this year. The poll collected data on types of hardware and software that engineers are using. Also of interest were the applications for CAD/CAE. Engineers were asked about total company spending for CAE/CAD and any expected changes in expenditures over the coming year. Readers also were asked which products they preferred in hardware, software, and system configurations. The Palo Alto, Calif., market researcher received survey results directly and then tabulated them.

BEST SELLER

Which technical books are the most popular in Silicon Valley?

ELECTRONICS:

- 1. C Language Algorithms for Digital Signal Processing by Paul Embree and Bruce Kimble. Prentice-Hall, 1991. \$55.
- 2. Art of Electronics, 2nd ed., by Paul Horowitz and Winfield Hill. Cambridge University Press, 1990. \$54.50
- 3. Computer-aided Circuit Analysis Using Spice by Walter Banzhaf. Prentice-Hall, 1989. \$28.
- 4. Modular Series on Solid State

Devices: Advanced MOS Devices by Dieter Schroder. Addison-Wesley, 1986. \$30.50

5. Digital Communications by Bernard Sklar. Prentice-Hall, 1988. **\$64**.

COMPUTER SCIENCE:

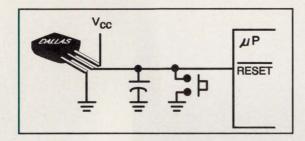
- 1. C++ Primer by Stanley Lippman. Addison-Wesley, 1991. \$30.50.
- 2. C Programming Language by Brian Kernigan and Dennie Ritchie. Prentice-Hall,

1988. \$33.

- 3. C++ Programming Language by Bjarne Stroustrup. Addison-Wesley, 1991. \$28.75.
- 4. Unix System Administration
 Handbook by Evi Nemeth, Garth Snyder,
 and Scott Seebass. Prentice-Hall, 1989. \$38.
- 5. Cyberpunk by John Markoff. Simon & Schuster, 1991, \$22.95

This list is compiled for *Electronic Design* by Stacey's Bookstore, 219 University Ave., Palo Alto, CA 94301; (415) 326-0681; fax (415) 326-0693.

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KickStarter	18	4	FA 2 877			~
Power Fail Interrupt NMI	~			~		~

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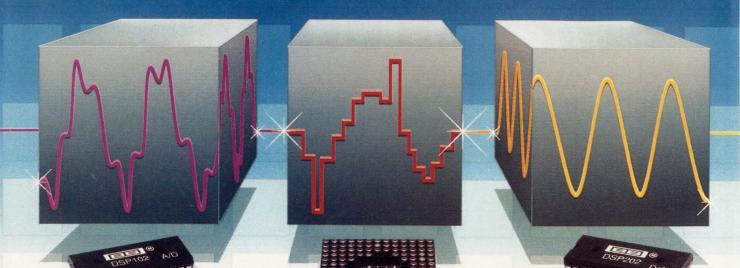
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PEASE PORRIDGE

WHAT'S ALL THIS SPICEY STUFF, ANYHOW? (PART III)

irst, let's have an esaeP's Fable: A person (when I tell the story, I always say it was a Harvard graduate, but you can insult anybody you think is appropriate...) had died and was wandering through Limbo and Purgatory. He came to two paths with two signs. One sign pointed "To Heaven." The other sign said "To a Lecture On Heaven." So of course he decided to go to the Lecture On Heaven. End of Fable.

I was at an Evening Panel Session of the International Solid-State Circuits Conference (ISSCC) in February. Some engineers were talking about CAD—Computer-Aided De-



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CALIF.

sign-and its importance in their work. They said that they got so wrapped up in their CAD that they almost forgot what their mission was. Was their mission to use CAD tools to build perfect circuits on the first silicon-no matter how long it takes to get all of the perfect answers from the CAD? NO! Their mission was to build good circuits quickly and with low cost.

If they used their CAD tools until they were convinced the layout and design were *perfect*, that might take months. But if they thought their layout and design were *pretty good*, they could go to fab and get silicon in three weeks. Then they would really find out if their design was good. It's easy to get tricked into following the path leading to the Lecture On Heaven. But, where is it that you're *really* trying to go?

One of the things I do in my spare time here at National is to serve on the Patent Committee. About one morning a month, several of us engineers get together and review the patent proposals and Invention Disclosures. We try to encourage the good ones, and we grouse about the people who bring them in late. A couple of years ago, one of the inventors gave us a neat explanation of his new circuit that featured greatly improved frequency response. I looked at it. I waited patiently while he explained how well it worked, under all worst-case conditions. Then, I must admit, I pounced. "There's just one problem, my friend. That circuit will not work at all." He showed consternation on his face. "But I evaluated it thoroughly...." I broke in, "Yeah, in Spice." He blanched. "How did you know? Yes, I evaluated it in Spice, and it worked perfectly."

I told him that was just the problem. When you get a circuit perfectly balanced in Spice, it will stay perfectly balanced. Just like inverting the Great Pyramid and perching it on its tip. In Spice, that will stay balanced forever. But in the real world, it will fall over, without even waiting for a windy day. That was the first weakness of his circuit. I asked him, "If you take an operational amplifier with a dc gain of a million, and an offset voltage of 2 mV, and you put a 1-V ac signal right into its input and ask Spice to tell you the dc gain, what will it give you for an answer?" He thought and said, "It will tell you the

gain is 1 million." I agreed, that's what Spice will say, but in the real world you can't evaluate an op amp by feeding a volt right into the negative input. And in his circuit, which called for two perfectly matched and balanced stages, you could ask Spice to give you an answer. Spice might give you an answer, but that answer is NOT the real one. Spice is sometimes incapable of telling you what will really happen at a circuit's output.

Later, I gave the would-be inventor some tips, and suggested he bring the circuit back to the Patent Committee if he could get it working on a breadboard—not just on Spice alone. Unfortunately, I haven't seen the fellow since then. I'm not even sure where he is these days. But at least I saved him the embarrassment of getting a big circuit made up and discovering the silicon doesn't work, and couldn't ever be made to work. If you just trust Spice, and don't verify with a breadboard (or a good sharp-pencil analysis), that can get you into real trouble when Spice gives you answers that don't have any foundation in the real world. "Proverai no Doverai"—Trust, but Verify.

But you don't have to just take the word of an analog freak like Pease. If your area of expertise is digital circuits, you know about metastability. A latch's or flip-flop's output may not be able to make up its mind for a surprisingly long time if the input data is moving at just the wrong time—when you're CLOCKING it. Metastability is a real problem, but everything that I've heard says that Spice can't model metastability, nor can any other form of CAD simulate that. Is that not still true? Breadboarding is NOT obsolete.

This problem in the digital realm is quite analogous to another analog problem in Spice. If you have an op amp and put feedback around it with the inputs inadvertently crossed, and ask the circuit's gain, Spice can tell you the op amp's gain—even though the inputs are reversed and the feedback is *positive* feedback. So you really can't count on Spice to even give you a sanity check! Spice can look right at your crossed-up circuit and

PEASE PORRIDGE

say that nothing is wrong!

Recently I was talking with a teacher who had a student come up to him, saying very enthusiastically, "Mr. Johnson, I just designed an operational amplifier with a gain of 10 million!" The teacher asked how he had designed it. The student said he had designed one good stage with a gain of 10—and then cascaded 7 stages. Of course, it didn't have a differential input, and it might have terrible offset, drift, and PSRR. But, it did have a gain of 10 million.

And if you tried to apply feedback from the output back to the input, would it work like an op amp? Could you control the gain and the response? The student stopped and thought for a while. He realized he didn't have a clue. And he didn't know how to wire it up and do a real evaluation to see how the real circuit would work. He had not developed an understanding of what makes an operational amplifier different from just any old amplifier.

Spice can insulate you, shield you away from an understanding, an appreciation, of what makes a real circuit work. You can now take a circuit in Spice, tweak the parameters—try out all sorts of values of resistors—and get a circuit that is "optimized." In fact, if you are a really smart programmer, you can program the computer to do it all for you. But Spice doesn't really UNDERSTAND your circuit—and neither do YOU if you only optimize things that way.

At that ISSCC Evening Panel Session, a member of the audience asked one of the panelists, a university professor, "In your department, what is the ratio of students studying CAD to the number studying circuit design?" The ratio, he estimated, was 25 to 1. I thought that was a shocker. But some panelists thought, hey, no problem, you can learn to drive the Spice and UNIX and CAD tools first, and then learn to design circuits later. They said that, but I don't think it's that simple. It bothers me that designing circuits is considered just a minor, trivial task, an exercise that can be learned later by any good computer jockey. In my experience, there are very few engineers who can design amplifiers (or circuits) worth a darn without lots of experience in amplifier design (or circuit design).

I bet a lot fewer than 1/25 of the students are learning anything about measuring these days—measuring voltages, measuring currents, measuring signals, measuring noise. I've gotten letters from readers who explain that at some schools, you can earn your BSEE, and even a Master's degree, by studying just computer-simulated circuits. That's because they don't have any lab courses any moreno op amps, no flip-flops, probably not even any gates. There are no DVMs, no VOMs, no Scopes—just computers! Everything is simulated. That sure sounds scarv to me.

At the ISSCC, there was also an evening session on the topic of Designing Integrated Circuits with Mixed Signals (Analog and Digital), and what the impediments are to making good designs. Some of the panelists said that CAD is making great strides, "and even though we cannot always believe Spice when it says a circuit will work, at least we can believe it when it says a circuit will not work." I stood up and took the microphone. I asked for a straw vote-how many engineers in the audience had a lot of trouble with the case of a circuit that does work, but Spice said it does not work? About 15 or 20% of the audience held up a hand. They could not easily trust Spice because 20% of the time they had caught it lying about circuits that really do work. I shut up and sat down. But that just confirmed my suspicion that more CAD (even more powerful CAD) isn't going to be the solution.

For example, every year, I can tell when spring is here: In April, I start getting phone calls from students who can't get the LM117 to run on Spice. I tell them that, no, there's not an error in the schematic. The schematic in the data sheet really is the schematic for an LM117 (just be sure that Q19 and Q3 and Q7 and Q24 each have 10 emitters). I tell them, hey, don't feel bad, a lot of other people can't get the LM117 to run in Spice either. Now, someday, if I get all my other projects cleaned up (that's supposed to be a joke....), I'll try to run the LM117 in Spice and see what trouble I get into.

Come to think of it, every time I do a Spice run on a high-powered regulator I'm amused, because the output transistor can run at 1 A and $V_{ce} = 20$ V, but the V_{be} never decreases as time goes on because the circuit never gets hot. If you have a circuit like that, which runs well on Spice. you're headed for deep trouble when you try to lay it out. That's because in the actual silicon, the transistors really do get hot. And they heat up the adjacent transistors, with various gradients and isothermal lines. A smart engineer will lay out his critical matched transistors along the isothermal lines. But most CAD systems won't help you at all with that. Just as a digital designer won't get any help on metastability problems, designers of high-power linear circuits won't get help from Spice or from most any CAD system on thermal gradients, isotherms, thermal run-away, or secondary breakdown.

The final proof of the pudding for any circuit is how well does it work in the system. When people design an ASIC, they know there's only one customer, and the customer's specifications are very specific. So the engineers and designers use CAD very heavily to confirm that the IC will do *exactly* what the customer says he wants.

These days, CAD works well enough that about 50% of the ASICs meet their specs on the first try (OK, that's not a wonderful success rate, but I don't want to worry about that here). However, of the ASICs that do meet every spec, 20% of them don't work in the customer's system. All of the CAD tools in the world—all of the models and computers and numbercrunchers and timing diagrams—are worth little if the chip designer made an error in understanding what his system really needs. Or, to be more honest, if the customer fails to specify what he really needs. Compared to computers (or even some people) that can only follow instructions, people who can think and comprehend the entire system are still worth quite a bit.

Now, some people have asked me, "Bob, why do you keep saying all these terrible things about Spice? When we come out with our Spice models, peo-

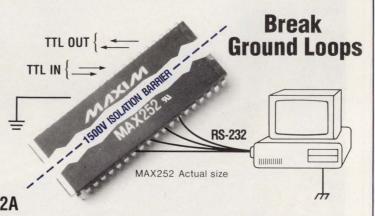
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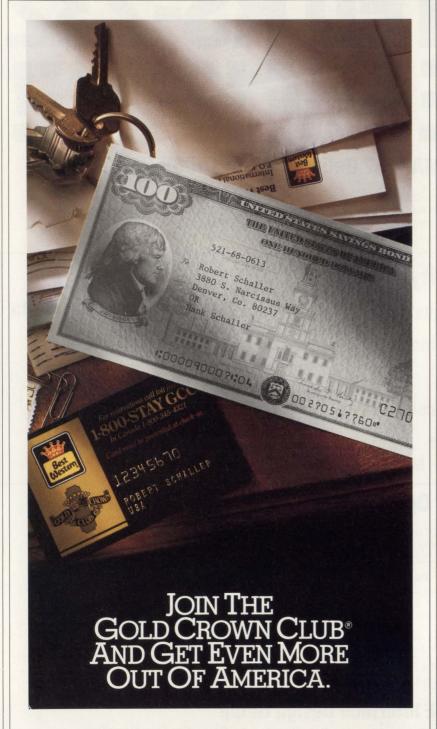
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PEASE PORRIDGE

ple will say you have wrecked our credibility. Can't you say anything nice about Spice?"

I respond: "Ah—that is exactly the point. If I only said good things about Spice, smart engineers would refuse to believe us! We would *lose* our credibility. This industry already has too many people who can do nothing but say good things about CAD and Spice. What I am doing is drawing attention to specific problem areas of Spice and other CAD tools, so that our friends will be educated about problem areas to beware of."

Now, it's true that there are, despite the things I grouse about, some good things I can say about Spice and similar circuit-simulation programs. Primarily, Spice is good for a first estimate of a circuit's feasibility—as an aid to help you compute how the circuit is likely to work, ideally.

Spice can help you decide what's a good circuit to breadboard. Then when you have the breadboard running, you want to confirm that the Spice results really are consistent with the breadboard data, so you can cross-check that your models are good. If you have good models, you can use Spice to exercise the system through a first round of worst-case tests, more quickly than with a breadboard. For example, it might be really hard to find any real worst-case op amps, but it might be easier to use Spice models than to do many hand calculations. So, Spice can be a useful tool in the hands of a good engineer, to help him analyze variations on the central theme. It's only when people start making euphoric statements that breadboarding is passé and superfluous that we get worried. So, why do I keep saying these "terrible" things about Spice? Well, it's not my fault that it only takes five sentences to say what Spice is generally good for and five pages to list some of the pitfalls.

All for now. / Comments invited! RAP / Robert A. Pease / Engineer

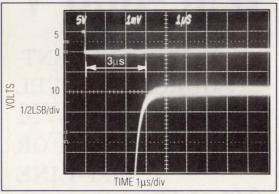
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ICS LEVEL-SHIFT 3-PHASE MOTOR-DRIVE PWM -500 V

500-V PNP CURRENT-SOURCE IC LEVEL SHIFTERS SIMPLIFY PWM DRIVE CIRCUITS FOR OFF-LINE 1/3-To-1-HORSEPOWER BRUSHLESS DC MOTORS.

FRANK GOODENOUGH

n today's world of million-transistor chips, why build an IC containing just 12 devices? And why put it in a package with five pins missing? The answers to these questions lie in a newly introduced high-voltage motor-drive chip that contains just seven pnp transistors, two Zener diodes, and three resistors in an innovative circuit topology. Those components are all that's required to accomplish fairly sophisticated tasks simply. Furthermore, the 20-pin skinny DIP housing the high-voltage motor-drive chip contains only 15 pins, because that scheme allows the high-voltage input pins to be spaced wider apart, which in turn lets the pins handle 115- or 230-V ac line voltages.

When used with two other ICs and power MOSFETs or insulated-gate bipolar transistors (IGBTs), the new motor-drive chip simplifies the drive and speed-control requirements of 1/3-to-1-horsepower brushless dc motors. Such motors typically operate from the rectified 115- or 230-V ac line (applications for these smooth-running, variable-speed motors range from washing machines to ventilating-blower systems, pumps, and compressors; however, because the new IC can't provide holding or braking torque, it's not aimed at servo-positioning-type applications).

The new circuit topology replaces the complex, usually expensive, high-side switching circuitry typically used in off-line pulse-width modulated (PWM) motor-drive applications. In virtually all of today's drive circuits, the PWM signals—at either TTL levels or at the 10-to-15 V from controllers or drivers—must be level-shifted to the positive high-voltage rail. And if MOSFETs or IGBTs are being driven, which is the trend for new designs, the drive must be moved 10 to 15 V above that rail.

The available alternatives are far more complex. They include complicated discrete approaches using transformers or optoisolators, driver ICs and chip sets built on expensive (multimask set) low-voltage/high-voltage processes and chip sets requiring the use of transformers (ELECTRONIC DESIGN, May 9, p. 34).

Most techniques require a bootstrap circuit that's "refreshed" by the pulse-width modulator. However, when power is called for by the system, it takes time to recharge the bootstrap circuit's output capacitor. Thus, after relatively short periods at a low speed, or after the motor has been stopped and must be restarted, the drive voltage can decay to zero. The charging time, which can be in the millisecond range, could significantly delay the motor in reaching its required speed. An undervoltage-lockout circuit might protect the FET from damage due to low gate-drive voltages, but it won't provide the gate drive required to turn on the motor. Consequently, a common, yet expensive, solution employs a separate floating supply for each high-side switch.

The new IC comes in two versions—the MDC2125 and the MDC2150. They're identical except for voltage rat-

HI-SIDE POWER SWITCHING EXTENDS BATTERY LIFE

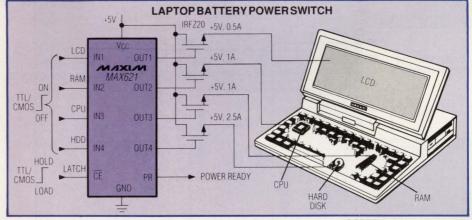
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Logic-level signals independently control four high-current MOSFET switches.

MAX620 FAMI	LY OF HIGH-SIDE	SWITCHES, D	PRIVERS, AND F	OWER SUPPL	IES
	MAX620	MAX621	MAX622	MAX623	MAX625
Function	4 Drivers	4 Drivers	Power Supply	Power Supply	4 Switches
Internal Power Supply	YES	YES	YES	YES	YES
Internal FET Drivers	4	4	External	External	4
Internal FET Switches	External	External	External	External	4x1.0A/0.2Ω
External Capacitors	3	0	3	0	0
# Pins/Package	18/DIP, SO	18/DIP	8/DIP, SO	16/DIP	24/DIP
Price (1000-up)†	\$3.91	\$5.82	\$1.99	\$3.95	Available 9/91

*Comparison based on difference between using IRFZ40 (35A/0.028 Ω) NMOSFETs and MAX620 versus using IRF9Z30 (18A/0.14 Ω) PMOSFETs, 1000-up.



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500-V LEVEL-SHIFTING IC FOR MOTOR CONTROL

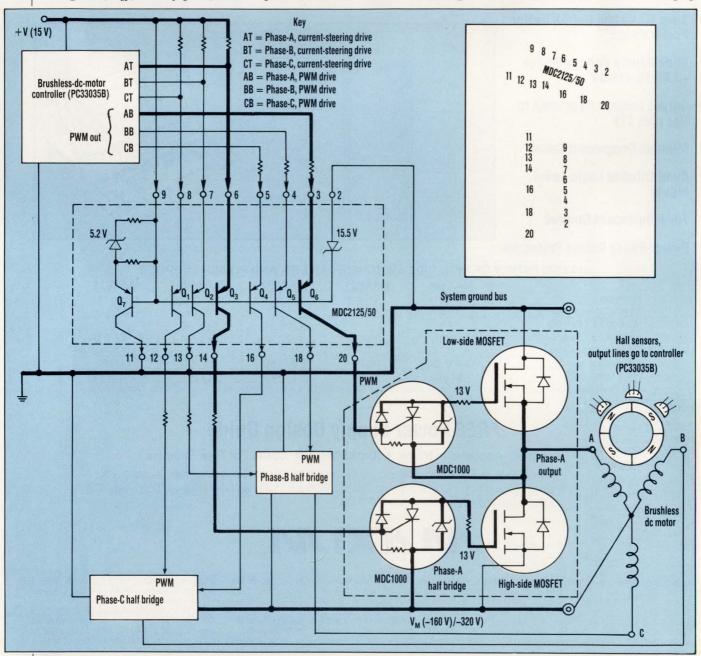
ing, which are 250 V and 500 V, respectively (the former handles the 115-V jobs, the latter 230 V). Together, the MDC2125/50 and the previously available MDC1000 controller IC eliminate high-side switching problems by incorporating several innovations. To start, in the new topology, the motor's power source is moved from the commonly used positive high-voltage rail to a minus high-voltage rail, $V_{\rm M}$ (see the figure). That

is, the junction of the motor's three windings are connected to a minus power-supply rail. The other end of each winding is connected to the output of one of the three power-MOS-FET half bridges. The half bridges operate between $V_{\rm M}$ and ground.

By moving the motor's connections, the motor can be driven with current pulses, rather than the usual voltage pulses. These current pulses, taken from the low-voltage

positive rail, drive both the low- and the high-side MOSFET switches in the half bridges. It's worth noting that virtually all of today's high-speed analog circuits, from op amps to analog-to-digital converters, are also switching from voltage-mode to current-mode operation, albeit to gain speed, not voltage isolation (analog designers across the board are trying new tricks).

The MDC2125/50's seven pnp



A 500-V LEVEL-SHIFTING IC, the MDC2125/50 from Motorola, implements a new, simpler topology for off-line motor-speed control. Its 20-pin DIP has had five pins removed to handle the high voltages (to 500 V) present.

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Step 1: Choose corner frequency and C. Step 2: Calculate folook and R. DONE! And DC offset is only a few microvolts! R IN OUT OUT OUT Foliate A Step 2: Calculate folook and R. DONE! And DC offset is only a few microvolts!

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500-V LEVEL-SHIFTING IC FOR MOTOR CONTROL

transistors are connected as common-base current sources. The outputs of the PC33035B controller (a modified version of Motorola's MC33035 brushless-dc-motor controller) drive the emitters of transistors Q_1 through Q_6 , turning their currents on and off. The seventh pnp transistor and the 5.2-V Zener diode form a reference, setting the currents of the other six transistors. In many respects, operation is similar to that of a bipolar-transistor, current-steering-output digital-to-analog converter with 500-V compliance, but just one bit of resolution. The controller decodes the outputs of the Hall-effect sensors in the motor to provide commutation timing, generate the PWM, and limit current.

The lower "low-side" MOSFETs are connected to the negative motor-supply rail. Their drive comes from the "steering" outputs of the controller. The outputs are labeled AT, BT, and CT, because in the more common applications they would drive the top transistors in the half bridge. The low-side transistors are switched by the currents from transistors Q_1 , Q_2 , and Q_3 . To commutate the motor, these currents switch the MOSFETs on slowly and off quickly at a relatively slow rate determined by the Hall-sensor outputs.

When using the 500-V MDC2150 (mandatory if the negative powersupply rail exceeds 250 V), an IGBT replaces the lower MOSFET (not shown in the figure). This enables a fast-recovery external rectifier to be used as a snubber, replacing the slower internal diode available if a 500-V FET had been employed. The upper "high-side" MOSFETs in the half bridges (their drains connected to ground) control motor speed with PWM. They're driven with PWM current pulses from transistors Q4, Q_5 , and Q_6 , which receive their drive from the controller's PWM outputs (AF, BB, CB). The internal diode of the high-side, PWM-driven, MOS-FETs don't typically see any current, so a 500-V FET can be used for 230-V ac applications.

The little MDC1000A/B/C (which come in TO-92, SOT-23, and SOT-223 packages, respectively) represents

the system's third innovation (ELEC-TRONIC DESIGN, January 10, p. 190). The MDC1000 was designed as a versatile MOSFET/IGBT driver offering active turn-off and self-protection. However, Motorola had the current-source-drive-motor-control topology (made possible by the MDC2125/50), in mind during its development. Regardless of the compliance voltage of the current source driving the MDC1000's input, its Zener diode clamps the IC's output, driving the FET gate to a safe 13 V. When the current pulse is removed, the silicon-controlled rectifier turns on and quickly discharges the FET's gate capacitance, and thus turns the FET off fast.

CRISS CROSS

Because it can dissipate 1.25 W, the MDC2125/50 might be considered a cross between a power IC and a discrete power device. The three large pnp transistors (Q_4 , Q_5 , and Q_6) can handle 50 mA continuously, while the three small tansistors can handle 2 mA. With devices rated at 250 and 500 V, it obviously falls in the high-voltage IC category.

Motorola puts the MDC2125/50 (and the MDC1000) in a new family of products called Smallblocks. These products come from the company's discrete-semiconductor group that also produces bipolar and MOSFET power devices and "smart-discrete" products. While appearing simple, additional process, layout, and packaging innovations were required to create the final MDC2125/50 high-voltage motor-drive IC.

The MDC2125/50's 120-mil-by-85-mil die is fabricated on a new high-voltage process that prevents its high-voltage lateral pnp transistors from saturating at low collector-to-base voltages. This feature not only permits effective operation at collector-to-base voltages as low as 5 V, but also prevents potential disasters that can occur if just one pnp transsitor saturates

If that occurs, minority carriers flood the epitaxial layer, permitting base-to-collector current to flow in the other pnps. Both switches in each H-bridge turn on at the same time, shorting the power rail directly to ground and causing meltdown. The process also minimizes collector-to-base capacitance, making it possible to operate at high dv/dts.

Pins 1, 10, 15, 17, and 19 were removed from the standard, 20-pin-DIP leadframe in order to handle the 500 V that can develop between the collectors of the pnp transistors (see the figure). Because the collectors of Q_1 , Q_2 , Q_3 , and Q_7 all operate at close to the same potential, their spacing is the standard 0.1 in. The collectors of the other three pnps, however, see the full-rail voltage between them (one may be at ground, the others at up to 500 V), so they must have appropriate spacing. From a safety point of view, the spacing between the pc-board pads represents the most critical criterion for high-voltage semiconductor packaging. A minimum creepage distance of 0.040 in. (1 mm) between pads is required for 115-V ac operation, twice that needed for 230-V ac operation.

Completely removing the pins provides an additional margin of safety and reliability. The lack of even a dead pin, or any exposed leadframe metal, increases the creepage distance along the surface of the package to over 2 mm. In addition, the increased leadframe spacing inside the package offers greater dielectric strength as well as resistance to the long-term effects of corona discharge.□

PRICE AND AVAILABILTY

Although in plastic packages, both the MDC2125/50 and the MDC1000 are designed to operate from -65°C to 150°C. However, the dissipation of the former derates linearly from 1.25 W at 25°C to zero at 125°C. Similarly, the current rating of the MDC1000 drops to zero at 150°C. In quantities of 1000, the MDC2125 in its "20-pin" DIP goes for \$2.50 each; the MDC2150 runs an additional 10 cents each. In similar quantities, the MDC1000A goes for just 25 cents each in a TO-92 package.

Motorola Inc., Discrete and Materials

Motorola Inc., Discrete and Materials Technology Group, MD Z201, 5005 East Mc-Dowell Rd., Phoenix, AZ 85008; Leonard Rennick, (602) 244-3810. CIRCLE 512

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JOHN NOVELLINO

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The solution that Integrated Measurement Systems (IMS) came up with is a "performance-optimized architecture." That is, carefully choose the right technology for each area, ranging from the hottest technology in performance-critical circuits to inexpensive mainstream devices where appropriate. The result is the Logic Master ATS, a test station with the accuracy and performance of traditional mainframe automated test equipment (ATE) at a fraction of the cost (Fig. 1).

The ATS's performance makes the

system ideal for a wide range of applications. Clock speeds go to 200 MHz and data rates to 400 Mbits/s. Edge placement is within 50 ps, and accuracy of up to ± 100 ps is possible. Other features that add to the tester's flexibility include programmable slew rates and current loads. The system handles all standard digital test requirements for standard ICs, ASICs, and multi-

chip modules. And within a month or so, IMS plans to introduce mixed-signal capability. As a result, the ATS is suitable for analytical applications, such as verification, characterization, failure analysis, and quality assurance.

Test stations are a relatively new but fast-growing segment of the test and measurement industry. The term is not formally defined, but basically test stations are to traditional ATE as mainframe computers are to workstations. The object is to get most of the benefits of ATE for as little as a tenth of the price. "Traditional ATE" means the room-size, multibay device testers that generally require special facilities and airconditioning arrangements.

The most significant departure from ATE systems is the ATS's lower throughput. But the system is useful for low-volume production test, especially when equipped with the optional per pin de parametric measurement unit, which significantly increases throughput. Standard features that enhance production testing include the system's excellent accuracy, which permits smaller guardbands and, in turn, increased yields. Also, software tools for the tester's Sun SparcStation host simplify test program creation and execution. And an internal 502-Mbyte hard disk stores extremely long test programs.

The ATS's accuracy also translates to increased confidence in device characterization. Using a feature typical of ATE systems, users can select a simple push-button automatic calibration that offers a skew of ± 500 ps. But for specific tests or devices that demand higher accuracy, users can perform a manual calibration that drops skew to ± 100 ps. Device characterization is facilitated



1. WITH SPECIFICATIONS LIKE a 400-Mbit/s data rate and 50-ps edge placement resolution, the Logic Master ATS offers ATE-like performance in an extremely compact package requiring no special environmental considerations.

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by a host of other features. For maximum flexibility, each channel can be programmed with its own format and timing, and set to its own drive and threshold levels. Programmable current loads make three-state measurements easy.

PROGRAMMABLE SLEW RATES

Furthermore, the ATS provides window strobes, dual-level comparators, programmable slew rates, and automatic measurement of standard parameters such as setup and hold times, propagation delay, and dc measurements. Test libraries, shmoo plot routines, and test sequencing tools for the Sun host augment these features.

Many of these same features enhance the ATS's ability to perform failure analysis and quality assurance testing. For example, the tester's programmable loads allow engineers to recreate real-world conditions under which the device under test might break down.

IMS leaned heavily on industry standards to ensure that ATS operators can link the tester to their design environment and existing ATE. The ATS has an Ethernet port so it can be integrated into the user's local-area network. Additionally, the system's interface and control software runs under Unix so any workstation on the LAN can access the ATS.

To provide the design-to-test link needed for fast test program creation. IMS will make available the WaveBridge software from Test Systems Strategies Inc. (TSSI). With this package, users can automatically create a test program from the device's design database. It also includes waveform editing and analysis tools. Other TSSI modules available from IMS automatically convert test programs written for ATE systems to the ATS format. Thus, programs written for high-volume production test on expensive ATE systems can be used for failure analysis on the much less expensive ATS. Users need not take their production test equipment off line to perform the analysis.

The performance-optimized archi-

tecture in the ATS runs the gamut from a full-custom GaAs driver-receiver to inexpensive field-programmable gate arrays. A tester's most critical circuitry is the pin electronics—consequently, that's where IMS invested the time and effort to come up with the state-of-the art driver-receiver. To take maximum advantage of the technology used, the assembly is placed in a very-high-density hybrid package.

Backing off one step from the pin electronics, the timing, calibration, and formatting circuitry does not need such exotic technology. Consequently, those circuits use standard cells based on an ECL substrate. Dropping down another level, the interface circuitry to the high-speed memory required only semicustom CMOS gate arrays. Finally, the glue logic consists of field-programmable arrays.

The result of this multi-technology architecture is the high performance at minimal cost, and a minimum size. One ATS board holds 16 complete I/O channels, everything from the driver-receiver hybrids to 128-kbytes of memory.

The ATS is compatible with the IMS Logic Master XL ASIC verification system, accepting both test fixtures and software designed for the XL. The new tester includes all the features of the XL including interactive screens for easy "what-if" analysis and the ability to display expected and actual test results simultaneously.□

PRICE AND AVAILABILTY

Prices for the Logic Master ATS are approximately \$2600 to \$3200 per channel, depending on options. A typical system with 128 I/O channels and a 128-kvector pattern memory costs \$360,000. Two mainframes are available. The ATS1 supports from 16 to 224 channels and the ATS2 permits up to 448 channels. Systems are available for order immediately, with delivery estimated within three months.

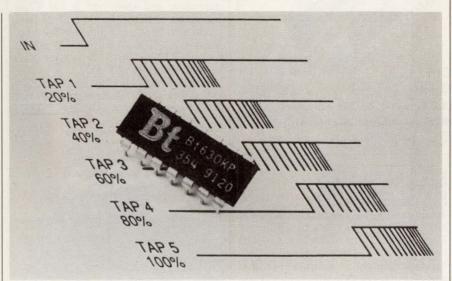
Integrated Measurement Systems Inc., 9525 S.W. Gemini Dr., Beaverton, OR 97005; (503) 626-7117. CIRCLE 513

How VALUABLE?	CIRCLE
HIGHLY	534
MODERATELY	535
SLIGHTLY	536

TTL SIGNALS SET DELAY OF IC DELAY LINE FROM 25 TO 400 NS FRANK GOODENOUGH

hen thinking of a wideband tapped delay line, you visualize a number of inductors and capacitors connected together in the familiar series-parallel circuit. The passive devices are potted in a SIP several inches long with an approximately square cross section between 1/4 and 1/2 in. on a side. Fat, high, plastic DIPs are also available with active buffers at the taps. However, on both package types, the delay between the input and each tap is cast in epoxy. That description, however, doesn't fit Brooktree's Bt630, which is a CMOS IC in a 14-pin plastic DIP that has a programmable delay. A 2bit, TTL word (on two control pins) sets the full-scale delay at the end of the line (the 100% tap) to cover one of four ranges: 25-50 ns, 50-100 ns, 100-200 ns, and 200-400 ns. The other four taps provide delays representing 20%, 40%, 60%, and 80% of the four, programmed, full-scale ranges. This gives the designer a wide range of delays that would be impossible without a large and varied inventory of fixed-span, tapped lines, an expensive and inconvenient solution.

While a two-bit digital word sets the coarse, 100%-delay range, an external resistor and capacitor set an exact value delay within each range. That is, one external resistor and capacitor set a specific value for the delay provided within each of the four ranges. For example, using the recommended 100-pF capacitor with a $7.68-k\Omega$ resistor (the minimum value) offers full-scale delays of 24, 48, 96, and 192 ns, respectively. Using the same capacitor and raising the programming resistor to 16.9 k Ω (the maximum value) provides delays of 52.8, 105.6, 211.3, and 422 ns, respectively, for the four ranges. As a result, a 10-kΩ potentiometer (connected as a variable resistor) in series with a 7.68-k Ω resistor, when used with the two digital inputs, varies the full-scale delay from 24 to 422 ns. The delay at the 20% tap now varies from



4.8 ns to 84.4 ns. The chip isn't programmable "on the fly," because the circuit takes about 50 ms to settle to a new delay range after changing the 2-bit control word.

Minimum input-pulse width for all ranges at minimum delays runs 10 ns. It rises just 5 ns at maximum delays. Minimum period between pulses for all ranges runs 20 ns at minimum delays, rising 10 ns for maximum delays, rising 10 ns for maximum delays. Delay accuracy runs within $\pm 5\%$ or ± 2 ns, whichever is greater. Bandwidth is typically 50 MHz. Typical power usage from a 5-V rail runs 50 mW. Each output tap can drive at least 10 TTL loads. Maximum drive for all five taps is 20 TTL loads. More loads can be driven, but timing accuracy degrades.

While the Bt630 is basically designed for digital applications, it suits analog uses in control or data systems based on pulse-width modulation. Digital-system applications range from pulse generators to CPU-clock, memory, and bus-interface timing. The Bt630 should find its way into computers and disk drives, plus instrumentation and telecommunication systems, and printers and copiers.

To ease the job of trying out the Bt630 programmable delay line, Brooktree unveils a demonstration

board called the Bt630DEM. In addition to a Bt630, the board contains a pair of 74LS123 one-shot multivibrators, DIP switches, the 100-pF capacitor, and three potentiometers. The one-shots generate TTL pulses that can be varied in width from 35 to 400 ns with two potentiometers. The DIP switches let you select one of the four ranges, while the third potentiometer adjusts the Bt630's delay. A single 5-V supply powers the board. Test points enable you to compare input and output waveforms with a two-channel oscilloscope, using high-impedance probes. However, Brooktree makes it clear that the board's basic role is to let you "play with" the Bt630. The layout isn't optimized and the board shouldn't be employed for precision evaluation of the delay line.

Designed for operation over the commercial-temperature range, the Bt630 goes for \$11.10 each in quantities of 100. Small lots are available from stock. Production quantities will be available early in 1992. Demonstration boards, completely equipped with a Bt630, are available for \$39 each.

Brooktree Corp., 9950 Barnes Canyon Rd., San Diego, CA 92121; Deborah Hancko, (619) 535-3395. CIRCLE 454



5-PA FET OP AMP SETTLES IN 85 NS

Traditionally, FET-input op amps are either fast or offer low bias current. Burr-Brown's OPA671 offers a mix of both, albeit it at a typical specification. While maximum bias current at 25°C runs 50 pA, it's typically under 5 pA. For a 10-V step, the output settles to within 1%, 0.1%, and 0.01% of final value in 85, 150, and 240 ns, respectively. Such performance lends the op amp to applications in fast current-to-voltage converters (for example, handling currents from photo diodes or DACs), sampling amplifiers, integrators, and buffering CMOS multiplexers. The amplifier slews at over 100 V/µs, which translates into a full-power bandwidth of over 1 MHz. Unity-gain bandwidth runs 35 MHz. A true op amp, its openloop gain runs a minimum of 74 dB while driving 200 Ω with ± 10 V. In its plastic 8-pin DIP, the OPA671 is rated for operation over the industrial-temperature range. In quantities of 100, it goes for \$5.95 each

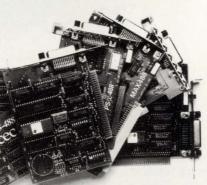
Burr-Brown Corp., P.O. Box 11400, Tucson, AZ 85734; John Conlon, (800) 548-6132. CIRCLE 455

VIDEO-BAND BUFFER HAS 0.9900 MINIMUM GAIN

Built on Maxim's complementary bipolar process, the MAX405 precision video buffer offers an order-of-magnitude better gain accuracy than similar devices and a minimum gain of 0.9900 over temperature. What's more, differential gain and phase, typically 0.03% and 0.01°, respectively, also are superior to those of similar devices.

Unlike virtually all available buffers, this IC's closed-loop circuit provides an inverting input that can be used with an external potentiometer to trim the gain to exactly zero, or even to 1.1. Over temperature and while operating from ± 5 -V rails and driving 50 Ω , the buffer's 3dB bandwidth for a 1-V rms signal runs 110 MHz minimum, full-power bandwidth for a 6-V pk-pk input runs 18 MHz minimum, and slew rate is 350 V/µs minimum. Settling time to 0.1% of final value runs 70 ns minimum for a 3-V step. Maximum quiescent current is 43 mA. In its 8-pin DIP, the MAX405 goes for \$4.25 each in quantities of 1000.

Maxim Integrated Products Inc., 120 San Gabriel Dr., Sunnyvale, CA 94086; Steve Pratt, (408) 737-7600. CIRCLE 456



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± 10 -V VIDEO OP AMPS CAN BE DISABLED

A pair of current-feedback op amps, the CLC411 and CLC430, offer a mix of price, performance, and features not previously available. The CLC411's output can be disabled (switched to a high impedance) in just 15 ns, and back on in 20 ns, while the CLC430 needs about 10 times longer. This feature permits high-speed multiplexing of the outputs to a video-distribution bus. The CLC411 is the fastest op amp capable of running off ±10-V rails. A 6-V output step typically settles to within 0.1% of final value in 2.7 ns. Typical 3-dB bandwidth for a 2-V pk-pk output runs 280 MHz. The output is flat within -0.1 dB from dc to 30 MHz and slews at 3000 V/ μ s while driving 100 Ω . The CLC430 offers a 3-dB bandwidth of 30 MHz for a 4-V pk-pk output, and 20 MHz for a 10-V pk-pk output, and slews at 1500 V/µs. In quantities of 1000, pricing for the

CLC411 and CLC430 start at \$5.76 and \$2.54 each, respectively.

Comlinear Corp., 4800 Wheaton Dr., Fort Collins, CO 80525-9483; Thomas Baldwin (303) 226-0500. GIRGLE 457

FREQUENCY GENERATOR REPLACES 16 CLOCKS

The AV9116 replaces up to 16 crystal oscillators on PC-compatible graphics boards. This CMOS IC, which generates clocks for graphics standards such as VGA, provides two outputs-one each for the video clock and memory clock. There are two standard versions, the AV9116-06 and AV9116-08. A 6-bit input word on each version selects one of 16 video clocks and one of 4 memory clocks. The former is used for Cirrus Logic's 6410 graphic controller IC and the latter for Tseng Laboratories' graphic controller IC. The AV9116-06's 16 video clocks range from 14.318 MHz to 79.64 MHz and its four memory clocks from 33.11 MHz to 49.22 MHz. The AV9116-08's video clocks range from 25.28 MHz to 108.28 MHz and its memory clocks from 39.0 MHz to 55.5 MHz. An "ASIC" version, the AV9116, lets users select exact frequencies for implementation with a metal mask. Two phase-locked loops, locked to a 14.318-Hz crystal or a TTL-input clock, develop outputs. In 20-pin DIPs, standard models are \$8.35 each in quantities of 1000.

Avasem Corp., 1271 Parkmoor Ave., San Jose, CA 95126; Barry Olsen, (408) 297-1201. CIRCLE 458



Burlington, MA. 01803

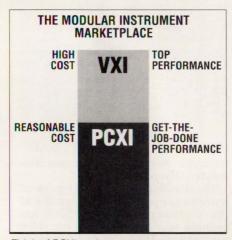
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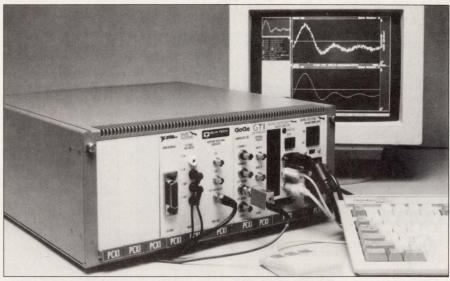
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For many of your testing requirements, PCXI is comparable to VXI, at a much lower cost. We even look alike, and offer similar ATE/MDA systems.

function modules (except PCXI has thousands of module choices from hundreds of manufacturers – all interchangeable). Both offer software (except PCXI offers software with every module). Both are multi-vendor systems. We both have our own industry Consortiums and published standards. We even look alike.

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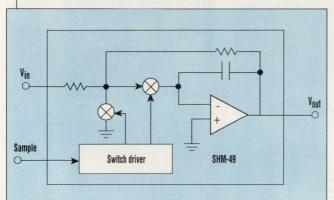
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etting new industry records in size and performance, Datel has squeezed a 200-ns, 12-bit-accurate, sample-and-hold amplifier (SHA) into an 8-pin DIP, and a 35-ns SHA with similar accuracy into a 14-pin DIP. Though they're chip-and-wire hybrids, the SHAs are in single-width DIPs. The first SHA, the SHM-49, acquires a 10-V input step in 200 ns maximum. Its aperture uncertainty or jitter runs a maximum of just 25 ps, easily permitting it to grab 3-MHz, 20-V pk-pk sine waves. The SHM-49 needs 415 mW. Though a hybrid, it's priced like a one-chip SHA, going for just \$39 each in 100s. It should be noted that the SHM-49's 1500-Ω input resistor must be driven by the output of a high-speed op amp. However, its architecture, in which that resistor is the input resistor of an integrator circuit, minimizes pedestal (sample-to-

hold) error to 25 mV maximum (see the figure). This is because currents, not voltages, are being switched into a virtual ground.

Its cohort, the SHM-43, acquires a 2-V step in a maximum of just 35 ns to within 0.01%. If only accuracy within 0.1% is required, acquisition time drops to 25 ns. Aperture uncertainty is an unmeasur-

able 3 ps maximum, permitting the sampling of 5-MHz, 4-V pk-pk sine waves. This is easily possible because the full-power bandwidth of the SHA, while tracking, runs a minimum of 20 MHz. Small-signal bandwidth runs 100 MHz minimum. Maximum harmonic distortion, a mandatory specification for signal processing, is a minimum of -70 dB from dc to 5 MHz (11.3 bits) for a ± 1 -V sine wave. Between 5 and 10 MHz, it runs -60 dB (9.7 bits). Feedthrough for a 2-V step is -76 dB, and input impedance is 50 k Ω . The SHA can put $\pm 1.5 \text{ V}$ across 50 Ω . Power dissipation runs just 625 mW maximum.

In quantities of 100 units, the SHM-43 SHA goes for \$103 each.

Datel Inc., 11 Cabot Blvd., Mansfield, MA 02048; Bob Leonard, (508) 339-6356. CIRCLE 459

■ FRANK GOODENOUGH

NEW DI PROCESS BUILDS FAST, LOW-POWER, LOW-COST OP AMPS

n advanced dielectrically isolated (DI) complementary-bipolar process developed by Harris dramatically lowers the power required by IC op amps to achieve a given speed/bandwidth-power product. Furthermore, cost is reduced. Six op amps from this process are price-per-

Performance Features of 6 New Lower-Power Harris Op Amps

PRODUCT TYPE	SLEW RATE (V/LS)	GAIN- BANDWIDTH (MHz)	MINIMUM STABLE GAIN (V/V)	MAXIMUM SUPPLY CURRENT (mA
HA-2839	600	600	10	13
HA-2840	600	600	10	13
HA-2850	340	470	10	8
HA-2841	250	54	1	11
HA-2842	375	80	2	15
HA-5020	800	100	1	10

formance competitive with junctionisolated (JI) op amps.

The HA-2541 and HA-2842 represent lower-power performance upgrades of the company's HA-2541/2542 announced over six years ago for video applications. They also find their way into various applications, from medical and industrial instrumentation to radar. A trio of devices (HA2839/40/50), only stable at gains of 10 or more, are optimized for high-speed signal processing. They can track and amplify fast waveforms, yet introduce little noise. Input noise runs below 6 nV/ $\sqrt{\rm Hz}$. The sixth op amp, the HA-5020, represents Harris' first current-feedback amplifier. Like most others of its genre, it's aimed at video applications. Also like others, bandwidth does not drop 6 dB for every 6-dB increase in closed-loop gain. Bandwidth runs 100 MHz at unity gain and is still 65 MHz at a gain of ten. Pricing in quantities of 100 for the six devices ranges between \$3 and \$4 each.

The process' npn transistors need just 3 mA to achieve fts of 800 MHz. Previous process transistors needed over three times that current. Harris calls this feature Reduced Feature Back-Diffused Collector (RFBC).

Harris Corp., Semiconductor Sector, P.O. Box 883, Melbourne, FL 32902-0883; (800) 4-HARRIS, ext. 1133. CIRCLE 461

■ FRANK GOODENOUGH

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scope can compare a source trace on channel 1 against a specified template, while simultaneously testing a source trace on channel 2 against four sets of measurement tolerances specified by the operator. If a failure occurs, the scope can take any of six actions: stop the acquisition; make a screen dump; store the trace to internal memory; store the selected trace to the memory card; emit an audible alarm; or output a pulse. The memory card can be read from or written to by any DOS-compatible computer through the computer's card drive or through the scope if the computer is connected to the instrument by an IEEE-488 bus. An autostore function automatically stores each waveform after acquisition. Transfer to the memory card is up to 100 times faster than to a floppy disk. The Model 9450A base price is \$13,990, with delivery in 8 weeks.

LeCroy Corp., 700 Chestnut Ridge Rd., Chestnut Ridge, NY 10977-6499; (914) 4525-2000. GIRGLE 462

LOW-COST DSO FEATURES 200-MSAMPLE/S RATE



With a 100-MHz bandwidth and 200-Msample/s digitizing rate, the model 465 digital storage oscilloscope offers an exceptional priceperformance ratio. The full digitizing rate is available on both channels, and comprehensive trigger capabilities allow the scope to cap-

ture glitches as short as 5 ns with a 0.4% (8-bit) vertical resolution on all vertical sensitivity settings. Advanced features include a 4-color plotter, automatic on-screen measurements, automatic setup, and a variable-persistence mode. The unit permits trace manipulation and testing of limits. Nonvolatile memories store the current setup parameters and up to three traces. In the persistence mode the scope displays all acquisitions captured over a specified time or number of sweeps. Users can select infinite persistence to permanently display all traces. The scope reads the new IEEE-488.2 Standard Commands for Programmable Instruments. Base price of the 465 is \$3490; delivery is in 30 days.

Gould Inc., Test and Measurement Group, 8333 Rockside Rd., Valley View, OH 44125; (216) 328-7263. GIRGLE 463

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INSTRUMENT CONTROLLERS BOAST HIGH PERFORMANCE

our additions to the HP 9000 Series 300 instrument-controller line offer the highest performance of the Motorola-based line at about half the price of the older units. The new models offer features typically needed in test systems, including expandable device-I/O capability, standard color graphics, integrated mass storage, and instrument-size packaging.

ing.
The Model 362 is a modular desktop controller based on the 25-MHz MC68030; the Model 382 is a similar unit built around the 25-MHz MC68040. The corresponding integrated versions, the Models R/362 and R/382, are rackmountable in 7-1/2 in. of vertical space—the standard instrument-rack size.

The Model 362 comes with a 14-in. standard VGA monitor. The Model 382 can be ordered with a VGA monitor or a 16-in. 1024-by-768 high-resolution monitor. Both monitors fit in a standard 19-in. instrument rack.

The system-processing-unit boards for the desktop models are housed in 3-1/2-in.-high instrument packages that hold the power supply, floppy-disk drive, and optional mass-storage devices. Both models have built-in device I/O capability and optional I/O expanded units. The rack-mountable versions include mass-storage devices, four device I/O slots, a 9-in. gray-scale display,



and a full-function keyboard.

Models 362 and R/362 can operate as standalone HP Basic and HP Pascal workstations or with other third-party operating systems. The 382 versions support the same operating systems as the 362 models, as well as the HP-UX operating system and software applications, such as HP Basic/UX and HP VEE-Engine and HP VEE-Test.

The Model 362 offers 6 MIPS performance, which is ideal for cost-sensitive test and measurement applications. The Model 382's 20 MIPS performance is suitable for higher-performance applications.

Instrument-controller bundles vary in price depending on the software, memory, and displays chosen. Typical prices range from \$6990 for a Model 362 to \$11,900 for a Model R/382. Delivery is in 4 weeks.

Hewlett-Packard Co. Measurement Systems Operation, 19310 Pruneridge Ave., Cupertino, CA 95014; (800) 752-0900. GIBCLE 464

JOHN NOVELLINO

SOFTWARE, ON-CHIP MATRIX DIAGNOSE ASIC FAILURES

workstation-based diagnostic software package, CX-Probe, cuts the ASIC debug cycle by automatically isolating and identifying functional failures in the devices. CX-Probe works with CrossCheck's patented on-chip test structures, which create a test-point matrix that acts as an on-chip grid of sense probes.

In effect, CX-probe, a workstation, and an ATE system form an automatic logic analyzer. Because of the large number of embedded sense probes provided by the on-chip structures, the resulting chip-level analysis tool offers massive, cell-level observability. CX-Probe uses the ATE system's output to diagnose functional failures caused by manufacturing defects, CAD errors, and macrocell library errors. The software identifies these errors during prototype debugging, analysis of production test yields, quality and reliability assurance analysis, and debugging of macrocell libraries.

Without CX-Probe, engineers typically must isolate defects by backtracking from test results. This trial-and-error procedure involves multiple test sessions. If backtracking fails to isolate the defect, time-consuming electron-beam probing must often be used. CX-Probe eliminates this manual, time-consuming interpretation of test results and makes electron-beam searching unnecessary.

CX-Probe works independently or with CX-Test, CrossCheck's fault-simulation and automatic test-pattern generation software. The software requires a Sun 4, SparcStation 1, or SparcStation 2 workstation. The package supports the Advantest 3320, Ando 8034 and 9035, Schlumberger Sentry 50, and Credence ASIX-2 ATE systems.

CrossCheck's on-chip test technology has been licensed to Fujitsu Ltd., Harris Semiconductor, LSI Logic Corp., Oki Electric Industry Co. Ltd., Raytheon Corp., and Sony Corp. LSI Logic and Oki recently introduced products using the test structures.

CX-Probe is available now for a license fee of \$125,000 per copy, which includes one year of software support.

CrossCheck Technology Inc. 2833
Junction Ave., Suite 100, San Jose,
CA 95134: (408) 432-9200.

JOHN NOVELLINO

ANALYZER MEASURES BIT ERRORS TO 72 KBITS/S

erforming error analysis on modems, multiplexers, and data circuits, the PF-25 bit-error analyzer works at bit rates up to 72 kbit/s. It facilitates troubleshooting by not just counting the bit errors, but also by showing when the errors occurred. This feature is useful in correlating the time an error occurred with external events.

Besides being used to troubleshoot data circuits, the PF-25 can be employed in developing and testing modems, multiplexers, and baseband and wideband modem circuits. All events for the last 60 hours as well as the distribution of bit errors are displayed as histograms on a large liquid-crystal

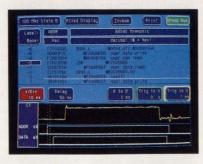
display. Minimum resolution is one minute. After a standard bit-error test, the bit-error ratio is computed for the overall test interval. The instrument can also evaluate results in accordance with CCITT Recommendation G.821. This evaluation gives a better idea of a communication link's performance, because a distinction is made between error bursts and randomly distributed errors.

The PF-25 is available now. Additional information and prices are available on request.

Wandel & Goltermann GmbH, P.O. Box 1262, D-7412 Eningen, Germany. Phone: (0049) 7121-861851; Fax: (0049) 7121-88404. CIRCLE 465

■ JOHN GOSCH

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STANDARD WAVEFORMS

bank of 16 standard waveforms and two line-segment drawing modes make the Model 2202A arbitrary waveform generator (AWG) easy to use. The instrument also features 12-bit resolution, 32kwords of battery-backed memory, and a waveform-sampling rate of 0.1 Hz to 20 MHz.

Users can create custom waveforms either from scratch, a segment at a time, or by interspersing arbitrary and standard waveforms. Also, any two standard or arbitrary waveforms stored in memory can be added, sub-



tracted, or multiplied. Waveform parameters for the standard waveforms are called up using soft keys and a 20character backlit LCD display. For a sine wave, typical total harmonic distortion plus noise is less than -65 dB over an 80-kHz bandwidth.

In the vertex drawing mode, users create waveforms by establishing end points at the desired addresses and then positioning a vertex between them. The Model 2202A automatically creates the connecting line segment. In the line mode, the user works from one left-hand anchor and creates one segment at a time by positioning a vertex to the right of the anchor, locking that point down, and establishing a new left anchor. Both modes can be accessed by using the eight front-panel keys or a mouse. An optional waveform sequence generator repeats a defined waveform to 1000 times.

An RS-232C interface is standard. Horizontal resolution is 32 kpoints, and vertical resolution is 4095 points (+2047 and -2048).

The Model 2202A costs \$2495. The sequence generator option is \$895 and the IEEE-488 interface is \$495.

> Pragmatic Instruments Inc. 7313 Carroll Rd., San Diego, CA 92121-2319; (619) 271-6770. CIRCLE 467

■ JOHN NOVELLINO

GENERATOR HAS 16 | AMPLIFIER MODULE GIVES **SCOPES 3-GHZ BANDWIDTH**

he 11A81 3-GHz amplifier plugin for the Tektronix 11403A and CSA 404 digitizing oscilloscopes features a rise time of less than 130 ps. The amplifier has an external trigger bandwidth of 2 GHz and a ±50division offset range.

The 3-GHz bandwidth provided by the amplifier makes the scopes suitable for characterizing high-speed GaAs, ECL, and biCMOS devices. With lower bandwidths, the observed rise times of such devices may be slower than the actual rise time. Used with the CSA 404, which is designed specifically for communications applications, the 11A81 enables designers to analyze communications systems at up to 625 Mbits/s. This figure is approximately one-fifth the scope's bandwidth, the ratio needed to assure accurate measurements and representations of the signals.

The plug-in uses a BNC connector with a Tekprobe interface, This arrangement is compatible with a variety of Tektronix's passive and active probes, including the P6700 series optical probes. The amplifier is fully pro-



grammable via GPIB and RS-232 interfaces. Together with the 11A81 frontend amplifier, the 11403A and CSA 404 offer wide dynamic range and flexible pretrigger capability, without the need for delay lines. Sensitivity of the 11A81 is 10 mV/div. to 1 V/div. in a 1-2-5 sequence.

The 11A81 plug-in amplifier costs \$5495, with delivery within 4 to 6 weeks. The 11403A digitizing-oscilloscope mainframe costs \$18,950; the CSA 404

mainframe goes for \$22,000.

Tektronix Inc. P.O. Box 19638, Portland, OR 97219-0638; (800) 426-2200 or (503) 627-7111. CIRCLE 468

JOHN NOVELLINO

HIGH-DENSITY SWITCH SYSTEM SIMPLFIES SETUP

two-slot switch system can handle up to 80 channels of two-pole switching in a half-rack mainframe. Together with three new switch cards and more than 30 other cards from Keithley, the Model 7001 supplies switching capabilities from 30 nV to 1300 V, 1 fA to 5 A, and dc to 500

The open-closed status of all channels is displayed simultaneously on the 7001 mainframe. Inserting any of the three new high-density cards in a slot automatically configures the mainframe and display for the correct number of channels, switch type, and switch settling time. The display also provides error messages, help, and setup and configuration prompts. The three cards include the Model 7011 40channel multiplexer card, Model 7012 4by-10 matrix card, and Model 7013 20channel independent switch card.

Users can program a scan (channel spacing, scan spacing, and number of scans) either over the IEEE-488 bus or through the Model 7001 without tying up the host computer. A nonvolatile memory in the mainframe stores up to 100 complete switch patterns. An additional 10 memory locations store complete instrument setups. The need for card-to-card wiring is virtually eliminated by the 7001's analog backplane, which automatically makes the intercard connections inside the mainframe.

No additional cards are needed for hardware triggering. A built-in Trigger-Link feature delivers more precise, repeatable triggering of multiple instruments with higher throughput than is possible over the IEEE-488 bus. The system offers six trigger lines through a rear-panel DIN connector.

The Model 7001 switch system costs \$1795. The Model 7011, 7012, and 7013 plug-in cards cost \$995 each. Delivery is in 2 weeks.

Keithley Instruments Inc. 28775 Aurora Rd., Cleveland, OH 44139; (800) 552-1115 or (216) 248-0400. CIRCLE 469



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Mismatched, nonintegrated

development tools can throw off a design team's efforts in no time.

RISC-BASED MULTIMEDIA CHIP EXECUTES MULTIPLE ALGORITHMS MILT LEONARD

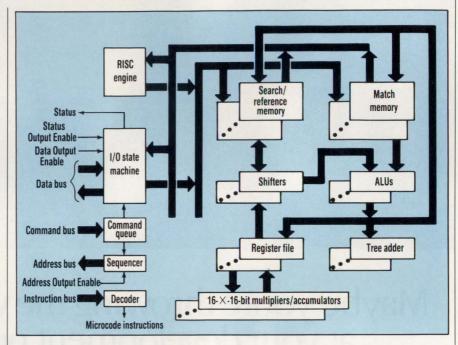
microcoded, programmable video-signal processing chip from Integrated Information Technology Inc. can execute all of the JPEG, MPEG, and CCITT H.261 (Px64) video-compression and decompression algorithms for multimedia applications. Structured around a 64-bit parallel architecture, the Vision Processor's (VP's) on-chip functions include a 16bit, 32-instruction RISC engine, four parallel 16-by-16-bit multiplier-accumulators, and reconfigurable parallel 64-bit ALUs (sixteen 8-bit or eight 16-bit ones).

Also included on the microcoded, programmable video-signal processing chip are a shifter and tree adder circuits for motion estimation, a six-deep command queue and sequencer for host-processor commands, and three triple-ported register banks (see the diagram).

There's still more circuitry on the chip. This includes custom address generators and a 32-bit DMA port that links to external page-mode dynamic RAM. On-chip ROM stores the IIT-supplied microcode, and memory space is also provided for search, reference, and match functions. Algorithm parameters, such as quantization values, are user-programmable. This architecture enables the chip to perform 1.9 billion operations per second at a 40-MHz clock rate.

The VP runs all stages of the compression/decompression algorithms from pixels to run/amplitude tokens for data compression, and from run/amplitude tokens to pixels for decompression. Functional capability includes forward and inverse discrete-cosine transforms, quantization and inverse quantization and inverse quantization and decoding, motion estimation and compensation, and filtering.

The VP video-signal processing chip can execute instructions from the microcoded ROM or from microcode stored in external static RAM. The 14-bit microcode address bus al-



lows up to 16,000 32-bit static-RAM locations to be addressed.

Fabricated in a 1-µm CMOS process, the VP runs on a single 5-V power supply. The chip dissipates just 1.5 W while operating at a clock frequency of 40 MHz. The chip is also available for operation at 25- and 33-MHz clock frequencies. Packaged in a 144-pin plastic quad flat pack, the 40-MHz VP is available now for \$150 each in quantities of 10,000. A JPEG-only version goes for \$60 each in the same quantity.

A full evaluation unit with JPEG, MPEG, and Px64 encoding/decoding capability will be available from Integrated Information Technology early next year. The Integrated Vision Module (IVM) is a plug-in, 4.5-by-4.5-in. circuit card that includes the VP video-signal processing chip, a companion Vision Controller (VC) chip, program and data storage, and frame-buffer memory.

The VC vision controller chip is a resource manager that shares memory with the VP, provides an interface to the video data stream, and performs pre- and post-processing of

video data. Included on the chip are a 32-bit MIPX-S microcontroller, host-and pixel-bus interfaces, direct memory access, reference memory, a temporal filter, decimation and interpolation filters for pixel-data I/O, and a Huffman-coding engine for final pixel-to-bit translation. The VC permits multiple VPs to be connected in parallel to support higher resolutions and greater bandwidths.

The IVM card has pixel buses that can interface to video cameras, VCRs, and scanners for inputs, and to monitors, VCRs, and printers for outputs. Frame buffering is handled internally by the IVM.

The host-computer bus links to standard PC buses and to microprocessor buses for embedded applications. In addition to transferring data, this bus is used by the host computer to program such parameters as Huffman and quantization tables.

Single units of the IVM vision module will cost \$1200 each.

Integrated Information Technology, Inc., 2445 Mission College Blvd., Santa Clara, CA 95054; (408) 727-1885. CIRCLE 470



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X-RAY SYSTEM QUICKLY INSPECTS SMT SOLDER JOINTS

he world's first in-line X-ray system for solder-joint inspection promises to solve a host of problems for high-volume, hands-off circuitboard assemblers. The CXI-3300 Series of automated, real-time systems features advanced microfocus imaging for

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and Precision Wound

high-resolution applications.

In this system, users who were limited to vision-based inspection for in-line process control now have high-speed, high-resolution X-ray inspection at their disposal. Using a pass-through design, the CXI-3300 systems easily support surface-mounted assembly

Pulse



processes and handles lead pitches as fine as 20 mils. The system inspects gull-wing, J-lead, and leadless devices as well as plated-through-hole solder connections. It also accommodates dense single- and double-sided boards.

The system was developed with an eye toward volume production of fine-pitch SMT devices. Parallel image processing enables the CXI-3300 system to perform production-speed inspection. Its computer-controlled variable imaging field gives greater magnification on fine-pitch SMT devices and less magnification (with higher throughput) on all other devices. Peak throughput rates exceed 75 solder joints per second.

Application development is fast and efficient. The system accepts common SMT pick-and-place machine formats. Each system is delivered to users with the customer's production application ready to run immediately upon installation. Further, CAD-driven programming makes it possible to develop new inspection software in less than one day. A powerful workstation for offline application development is available. The system also draws from the company's comprehensive application library of measurement and fault-classification software.

With its high-speed parallel image processing capability and a complete application-software library, the CXI-3300 system's base price is \$365,000. Delivery is in 12 to 14 weeks.

IRT Corp., 3030 Callan Rd., San Diego, CA 92121; (619) 450-4343. CIRCLE 472

■ DAVID MALINIAK

CORRECTION

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On page 25 of our Sept. 12 issue, the story titled "No-clean flux method beats low-yield barrier" contained an incorrect phone number. The number for Pensar Corp. is (414) 739-4355.

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Si9953DY	Dual P-Ch	20 V	0.25Ω	2.3 A
Si9955DY	Dual N-Ch	50 V	0.13Ω	3.0 A
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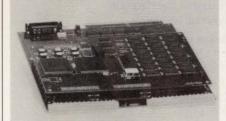
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2K-BY-2K DISPLAY CONTROLLER COMES IN BELOW \$10,000

esigned for display subsystems with resolutions from 1280 by 1024 to 2048 by 2048 pixels, the Ω5700 X-Window-based controller from Metheus Corp. fits in one VME slot. The main component of the board, which goes for \$9950, is the video frame buffer (VFB) that comes with both on- and off-screen memory connected through a 256-Mbyte/s bit-block transfer (BitBLT) ASIC. Double-buff-



ered operation is inherent in the design. Either the entire screen or individual windows can be updated at high speeds through the BitBLT ASIC without visible flickering.

The VFB is also populated with color lookup tables, a hardware cursor, and a video generator. The generator can be configured for almost any high-resolution monitor. Memory expansion modules for the VFB include added offscreen and overlay memory. The VFB can operate in a stand-alone configuration with the company's host-based X-Window server software.

The $\Omega5700$ consists of three 6U VME boards that can be assembled in different configurations to supply single- or multiple-display systems at different performance and cost levels. The VFB is the first board. Metheus offers the individual boards for insertion into a chassis complete with a power supply and bus-extension boards to interface non-VME host systems.

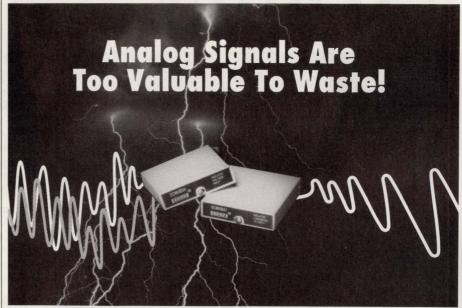
The second board is an i860-based graphics accelerator (GXA). The GXA supplies fast floating-point capabilities as well as 2D and 3D graphics functions. With the GXA in the system, all graphics functions of the X-Windows server are executed by the i860. The third board in the set, the video windowing controller (VWC), adds one full-motion video window to the graphics

screen. The VWC accepts video input from one source and supplies one 640-by-480-pixel full-motion, scalable window with up to 64,000 colors. Acceptable video sources include standard inputs from television cameras or recorders, including NTSC, PAL, and SECAM formats. Other nonstandard sources,

such as radar video, are also supported. The first two boards are available now and the VWC will be ready in November.

Metheus Corp., OGC Science Park, 1600 NW Compton Dr., Beaverton, OR 97006; (503) 690-1550. GIRGLE 473

■ RICHARD NASS



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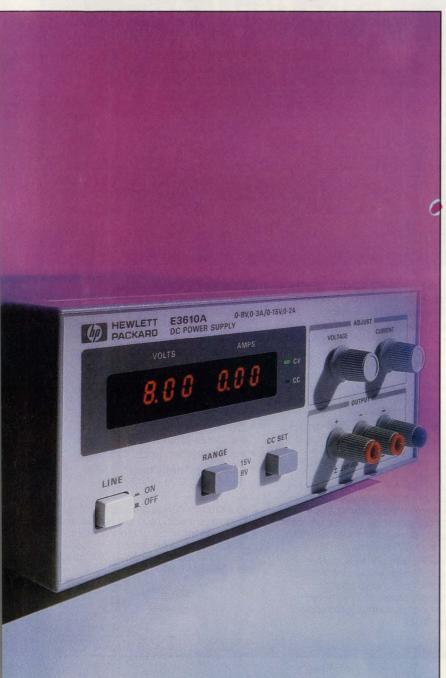
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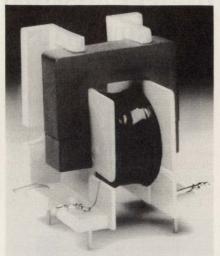
	30-watt ver supplies	E3610A	E3611A
put	Range 1	8V, 3A	20V, 1.50A
Output	Range 2	15V, 2A	35V, 0.85A
Load or line regulation		0.01% + 2 mV	
	le and noise Hz-10 MHz)		

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50-A LOAD DETECTOR INSTALLS IN A SNAP



A snap-on design is featured in the LD-50 load-detecting device. The device accurately monitors continuous load currents of up to 50 A rms and 150 A for short periods. The snap-on design reduces cost and simplifies installation in pre-wired systems without disturbing the wiring. Frequency response is 30 Hz to 15 kHz and accuracy is $\pm 3\%$ from 5 to 50 A. Pricing is \$1.98 in lots of 5000. Delivery is from stock.

Amecon Inc., 1900 Chris Ln., Anaheim, CA 92805; (714) 634-2220.

VARICAP DIODES SUIT VHF, UHF, TV TUNERS

A range of four varicap diodes is designed for VHF, UHF, and TV applications. The BB515, BB619, BB620, and BB811 come in two-lead hermetically sealed SOD-123 plastic surface-mountdevice envelopes. They suit TV and AM/FM radio tuners, CATV converters, communications equipment, and electronic disk-drive control. The diodes withstand a continuous reverse voltage of 30 V and pass reverse currents of 10 nA (20 nA for the BB811). Depending on type, the minimum capacitance is between 0.85 and 2.9 pF; capacitance ratios at 1 MHz vary between 9 and 25. The series resistance is typically between 0.5 and 1.45 Ω . Each sequence of seven diodes is matched to within 2.5%. In quantities of 10,000, price ranges from \$0.07 to \$0.13 each, depending on type.

Philips Components, Discrete Product Div., 2001 W. Blue Heron Blvd., Riviera Beach, FL 33404-5099; Miriam Coleman, (407) 881-3257. GIRGLE 475

MOTION SENSOR WORKS IN OR OUTDOORS

A micropowered passive infrared sensor combines interchangeable optics and electronics in a tiny, weather-tight aluminum housing. The IR2000 sensor permits communication with other sensors.

sors in a network to verify detection and eliminate most false alarms. A 24-V ac or 6-to-24-V dc supply is required; sources can be batteries or solar panels. Single-quantity price is \$97.50.

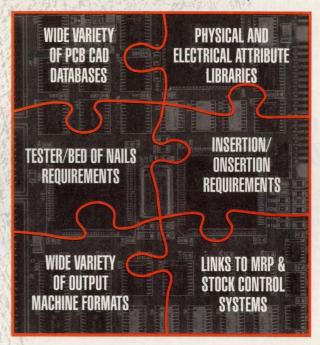
Infrared of NJ Inc., P.O. Box 59, River St. Station, Paterson, NJ 07544; (201) 523-1618. GIRGLE 476

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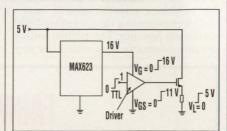
CIRCLE 269 FOR U.S. RESPONSE CIRCLE 270 FOR RESPONSE OUTSIDE THE U.S.

ICS YIELD HIGH-SIDE FET-DRIVE SUPPLY 11 V ABOVE POWER RAIL

f you're driving n-channel power-MOSFETs in low-voltage high-side switch applications, a pair of charge-pump ICs from Maxim—the MAX622 and MAX623—may be your ticket.

To turn on an n-channel MOSFET used as a high-side switch, the ICs' gates must be pulled at least 10 V positive with respect to the drain, which is usually connected to a plus rail. These CMOS chips, when connected to a supply between +3.5 and +16.5 V, provide an additional regulated supply rail 11 V more positive to act as the power source for the MOSFET's driver. The MAX622, in its 8-pin DIP or 8-pin SOIC, requires three external capacitors; its sibling in a 16-pin DIP contains these capacitors. Output current ranges from 500 µA to 5 mA, depending on input-voltage and capacitor values.

The charge-pump ICs eliminate the need to use logic-level or p-channel FETs in low-voltage applications, which usually cost more and are limited



in selection. A power-ready output from the chips goes to logic-level high when the output voltage rises more than 10 V above the input rail. The charge pump protects the MOSFETs by preventing turn on before the MOSFETs have sufficient drive voltage. In their 8- and 16-pin plastic DIPs, the MAX622 and MAX623 go for \$1.99 and \$3.95 each, respectively, in quantities of 1000.

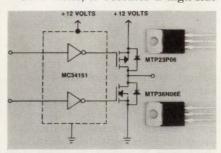
Maxim Integrated Products Inc., 120 San Gabriel Dr., Sunnyvale, CA 94086; Chris Neil, (408) 737-7600. GEGIE 417

■ FRANK GOODENOUGH

COMPLEMENTARY DMOSFETS SWITCH HIGH-SIDE LOADS EFFICIENTLY

hough a number of techniques and ICs make driving n-channel MOSFETs in high-side applications relatively easy, they take up time and space and are often costly. A new p-channel power MOSFET from Motorola, the MTP23P06, can serve as an alternative.

Used alone, it becomes a high-side



switch you can turn on by bringing its gate to ground, and turn off by bringing the gate to the plus rail. It handles 60 V from drain to source. Because its on-resistance is a maximum of just 120 m Ω , it can carry 23 A continuously, and three times that for a single 10- μ s pulse. The power MOSFET can switch fast, turning on and back off in under one-half μ s, lending it to switching regulators

When half- or full-bridge applications are needed, such as motor control, it can be used with its complementary cohort, the n-channel MTP36N06E. The n-channel device is also rated at 60 V. Its maximum on-resistance is a mere 40 m Ω , permitting it to carry 36 A continuously, and over four times that during a single pulse. It turns on, and off, in under 225 ns.

In many applications, the low on-resistance of these MOSFETs permits them to operate at lower than rated currents, without the need for heat sinks, from their TO-220 packages, again saving time, space, and cost.

In quantities of 100 units, the MTP35N06E and MTP23P06 DMOS-FET IC switches go for \$2.59 and \$2.87 each, respectively.

Motorola Inc., MD Z310, 5005 E. Mc-Dowell Rd., Phoenix, AZ 85008; Kirby Dorwachter, (602) 244-3370.

■ FRANK GOODENOUGH

RESONANT CONTROLLER SWITCHES AT ZERO VOLTAGE OR ZERO CURRENT

he ML4816 resonant-mode switching-regulator controller from Micro Linear not only runs in practical supplies at switching frequencies as high as 2.5 MHz, it also operates in multiple, user-selected topologies. These include zero-current-switched quasi-resonant converters requiring constant on time and modulated off time, as well as frequency-modulated designs running above resonance, in series mode, and using zero-voltage switching.

The user programs both minimum and maximum frequency limits of the resonant-mode switching-regulator controller. The output frequency can be directly, or inversely, proportional to the error voltage from the supply's output.

This controller is fully loaded with the features needed to protect the supply from potential disasters. These include pulse-by-pulse and dc-current limiting; so-called "integrating softstart," in which overload protection (shutdown) is triggered after a pro-



grammable delay time and restart after shutdown is also delayed by a user-programmable time; and low start-up-current and undervoltage lockout (with 6-V of hysteresis) to support off-line supplies. The pair of totem-pole out-puts provide the peak currents (to 2 A), needed to rapidly charge power-MOS-FET gate capacitance to over 10 V. In its 20-pin DIP or plastic chip carrier, the ML4816 goes for \$5.75 each in quantities of 1000.

Micro Linear Corp., 2092 Concourse Dr., San Jose, CA 95131; Charles Gopen, (408) 433-5200. ☐☐☐ 478 FRANK GOODENOUGH



It's an 8-channel MUX, a track-and-hold amp, and a 10-bit A/D converter in one.

Presenting the world's most complete sampling system on a single chip. The Harris HI-7153.

Channels: 8
Data Output: 10 bits
Conversion Time: 5 µsec
Resolution: 0.1%
Accuracy: 0.2%
Power Requirements: 150 mW

The 7153 combines speed, precision and low cost in one easy-to-use package. It can sample eight different signals up to 200,000 times per second. And its built-in sample and hold amplifier allows you to digitize 20 KHz signals to better than nine effective bits.

We even buffered the on-chip

MUX, so you don't need to add an external op amp. And it's microprocessor compatible.

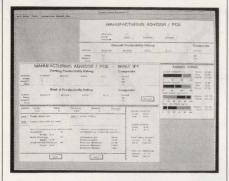
So for a complete sampling system on a single chip, there's one single number to call. 1-800-4-HARRIS, ext. 1153.



CIRCLE 113 FOR U.S. RESPONSE
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SOFTWARE ALERTS ENGINEERS TO MANUFACTURING PROBLEMS UP FRONT

ngineers can have better control over product cost, quality, and delivery with Manufacturing Advisor/PCB, a tool that alerts users to downstream effects of early design decisions regarding manufactur-



ing. The product was developed by Texas Instruments' Information Technology Group using Mentor's Decision Support System (DSS). DSS is a visual control panel with a programming language for prototyping and developing concurrent-engineering applications.

Manufacturing Advisor/PCB identifies parts-related manufacturing problems in pc boards early in the design

cycle. It offers a manufacturability "score" in an environment that allows for what-if analysis to test the effect of recommended design alternatives.

Prior to beginning schematic capture, engineers can enter a parts list to perform a preliminary analysis. As components are added to the design, Manufacturing Advisor monitors the consumption of available placement area. If exceeded, it will identify those components that could be mounted in an alternate configuration with a smaller footprint. As the design is refined through schematic capture and pc-board layout, Manufacturing Advisor continues to identify parts associated with unusual labor requirements, special manufacturing processes, high risk of manufacturing rework, and failure to comply with standards.

Manufacturing Advisor/PCB costs \$16,900. It will ship this month on HP/Apollo workstations, and next year on Sun machines. A component library containing manufacturability information on more than 800 package styles costs \$1500.

Mentor Graphics Corp., 8005 S.W. Boeckman Rd., Wilsonville, OR 97070-7777; (800) 547-3000.

CIRCLE 480

■ LISA MALINIAK

PCB DESIGN SYSTEM HAS CURVED TRACKS



Version 3.0 of the Pads-2000 pc-board design software offers many new features, including curved tracks. Users can automatically insert an arched or beveled miter at each route corner. The software allows for the definition of up to seven different mitering radii to meet varying design requirements. An interactive routine gives users the option to miter or unmiter a specific corner. In addition, users can manually route with arc segments. Curved segments will be recognized by the copperpour routines, and will be space checked accordingly. Other features include pad-stack modification on individual components and drill-hole checking. Pads-2000 Version 3.0 runs on PCs. It's shipping now for \$6995.

CAD Software Inc., 119 Russell St., Suite No. 6, Littleton, MA 01460; (508) 486-9521. GIRGLE 483

SIMULATION FAMILY ADDS TWO NEW MEMBERS

Silos III and P/C-Silos Version 5.0 are the two newest additions to the Silos simulation product family. Silos III, which runs on both PCs and workstations, makes it possible for users to perform behavioral modeling with the Verilog hardware description language. In addition, the memory-management system improves loading, compiling, and overall simulation time, and the amount of system memory that's needed. Silos III will ship early next year for use on most workstations and 80386and 80486-based PCs. The PC-based Version 5.0 is a logic simulator that runs as a Windows 3.0 application. Included in this version is the Silos Data Analyzer, a productivity tool that gives an interactive graphical view of the simulation results. P/C-Silos 5.0, which runs on PCs with 2 Mbytes of memory, is shipping now.

Simucad Inc., 32970 Alvarado-Niles Rd., Union City, CA 94587; (415) 487-9700. GIRGIE 481

AGREEMENT YIELDS IC SIMULATION MODELS

An agreement between Intel Corp. and Logic Automation Inc. will produce software simulation models for a broad range of Intel's future VLSI devices. The Logic Automation software models, called SmartModels, are behavioral simulation models. Under the terms of the agreement, Intel will give Logic Automation early access to new product information for timely model development. The two companies will work closely to ensure accuracy. Also, customers will have access to selected models at their announcement. Models of the microprocessor and key peripheral components will generally be available at the same time. Models that result from the agreement will be distributed and supported through the Logic Automation SmartModel Library subscription service. The first of these models will be available by year's end.

Logic Automation Inc., P.O. Box 310, Beaverton, OR 97075; (503) 690-6920. GIRGIE 482

TOOLS DELIVER TURNKEY MIXED-SIGNAL DESIGN

The Mixed-Signal Fastrack design system from Harris delivers front-to-back design for the company's analog-intensive mixed-signal ASIC libraries. The mixed-signal system, an extension of Harris' Analog Fastrack design system introduced in 1990, features multiple simulation engines on one simulator, macro/behavioral synthesis tools, and a dynamic switched-capacitor simulator. Switched-capacitor analysis runs with non-deterministic input signals and clocks. Mixed-Signal Fastrack consists of Cadence's cdsSpice and Verilog simulators, and Harris' Monte Carlo, ASIM, and SCAN products. Also included are physical-design, designrules-check, layout-versus-schematic, and layout-parasitic-extraction tools from Cadence. The system runs on HP/ Apollo and Sun workstations. Pricing depends on system configuration.

Harris Semiconductor, P.O. Box 883, Melbourne, FL 32901; (407) 724-3000. GIRGIE 484



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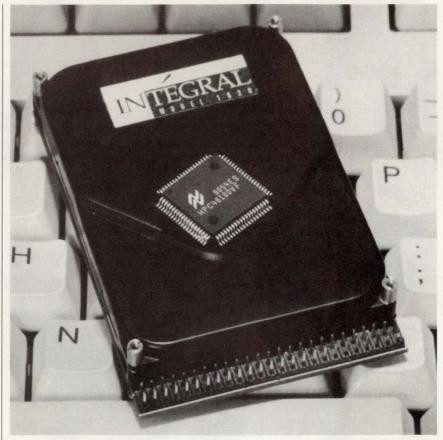
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CIRCLE 282 FOR RESPONSE OUTSIDE THE U.S.

40-MHZ MICROCONTROLLER ADDS DSP FUNCTIONALITY, EXPANDS TO 16 BITS RICHARD NASS

ith a cycle time of 50 ns, National Semiconductor Corp. claims HPC+ is the fastest 16-bit CMOS microcontroller. The 40-MHz chip combines high-performance digitalsignal-processing (DSP) capabilities with those typically akin to a highperformance microcontroller. This combination makes the part suitable for embedded servo applications, including hard-disk drives, automobiles, robotics, and industrial control. The part is fully upward sourcecompatible with the existing HPC family, while incorporating mixedsignal capabilities. The high speed is a result of the move from the 1.5- μm process of earlier family members to the 1.0-µm process of the current family. The part also offers an easy migration path from the traditional analog servo mechanisms to digital servos that offer better control and higher performance. As a disk-drive controller, the chip can handle both data-flow and motor-control func-

While not really a digital-signal processor, the part actually has comparable specifications to state-ofthe-art DSP chips. However, if the HPC+ were replaced with a traditional digital-signal processor, a second part would be needed to handle the microcontroller functions. Therefore, the board-space reduction becomes two-fold; one chip is eliminated and the single-chip microcontroller that's retained is housed in a tiny 14-by-14-mm package.

In addition to the HPC+'s 16-bit core CPU, the part includes a tightly coupled multiply-and-accumulate (MAC) unit, an 8-bit, high-speed analog-to-digital converter, 1 kbyte of zero-wait-state RAM, three timers, and a programmable UART. Analogto-digital conversion is performed in 5 µs, and DSP algorithms are executed three to five times faster than microcontrollers. competitive Throughput is increased as the microcontroller operates at frequen-



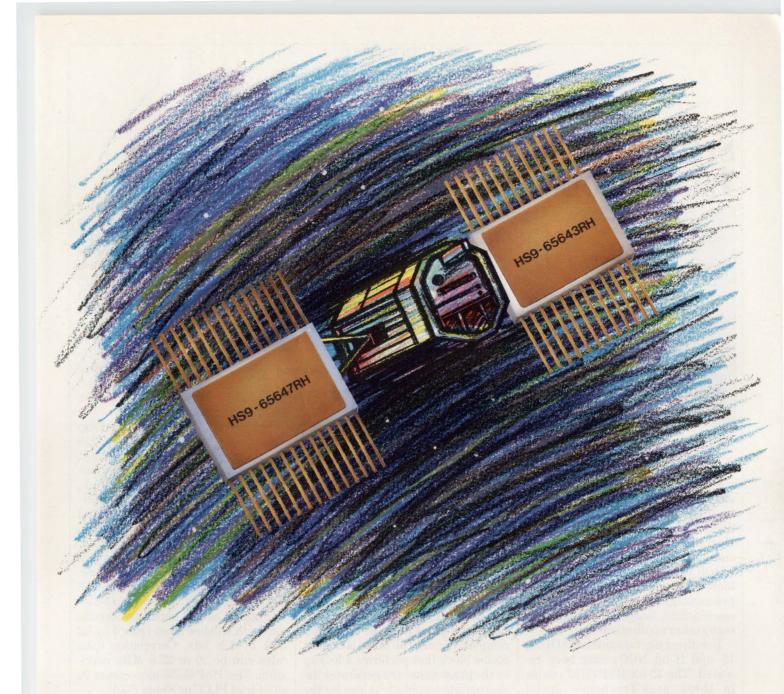
cies up to 40 MHz. At this speed, the MAC unit performs the 16-bit signed-integer MAC operation that forms the basis of a digital-filter implementation in 400 ns, outputting a 32-bit result. The chip is optimized for implementation of a finite-or infinite-impulse-response digital filter by supplying MAC and circular-buffer management.

The microcontroller's softwareconfigurable ADC can convert up to eight single-ended channels or four differential-channel pairs. It can be triggered for single readings or scans, or can perform these operations continuously.

The three high-speed timers supply processor-independent pulsewidth-modulation (PWM) signal generation. The timers and their support logic add independent control of PWM frequency and duty cycle with a minimum resolution of 50 ns while running at 40 MHz. The built-in UART features multiple character widths and stop bits, complete status reporting, error detection, an address-monitoring mode, and diagnostic-testing capabilities.

The HPC+ will make its first appearance in a pair of 1.8-in. hard-disk drives from Intégral Peripherals Inc., Boulder, Colo. (ELECTRONIC DE-SIGN, Sept. 12. p. 28). The Mustang Model 1820 is a single-platter, 20-Mbyte drive, while the Stingray Model 1842 is a dual-platter version that holds 40 Mbytes of data. The HPC+ is packaged in an 80-pin quad flat pack. In quantities of 1000, the part is priced at \$23. It should be in production by the first quarter of next year.

National Semiconductor Corp., 2900 Semiconductor Dr., P.O. Box 58090, Santa Clara, CA 95052; (408) 721-5000. CIRCLE 486



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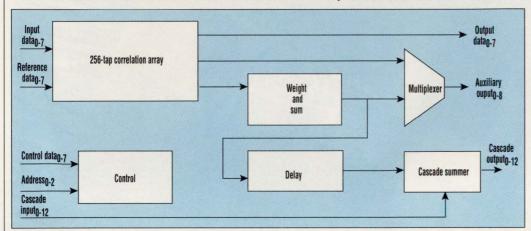
How does 50 ns access speed, an SEU error rate of less than 1×10^{-12} Errors/Bit Day, and full functionality beyond 1M rad sound? (Pretty out of this world, wouldn't you say?) And remember, Harris is the largest Class S Rad Hard supplier in the

universe. So if it sounds like we're handing you the best of all possible worlds, it's because we are.

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SPECIALIZED-FUNCTION DSP BLOCKS TACKLE COMMUNICATIONS, IMAGING DAVE BURSKY



family of building-block chips—numerically controlled oscillators (NCOs), binary correlators, finite-impulse-response filters, and address sequencers—are all part of Harris Semiconductor's solution to signal and image processing. The CMOS chips are the key functional blocks for radar and sonar signal-processing, spread-spectrum communications, image-processing, and many other applications.

For direct digital synthesis (DDS), 12- and 16-bit NCOs have been released. The 12-bit HSP45102 comes in three peak-frequency speed grades of 33, 40, and 50 MHz. The 16-bit HSP45106 offers maximum frequencies of 25.6, 33, and 40 MHz.

Aimed at cost-sensitive DDS applications, the 12-bit NCO contains a frequency control section, a 32-bit phase accumulator, a phase-offset adder, and a sine ROM. Frequency settings can be loaded serially but tuning resolution is to within 0.012 Hz at 50 MHz. The serial-load capability minimizes the pin count so that the chip requires only a 28-pin package (DIP

or SOIC).

Aimed at performance-critical applications, the 16-bit unit has direct tuning over a 16-bit microprocessor host interface and delivers 16-bit sine and cosine outputs. It also keeps spurious frequency components to less than -90 dBc. At 40 MHz, the

chip has tuning resolution of less than 0.01 Hz. The output frequency can be changed, cycle-by-cycle, to produce FM, PSK, FSK, or MSK modulated waveforms. To simplify PSK generation, a 3-pin interface is included on the chip to permit modulation of up to eight levels. The chip has two main sections. The first is a phase and frequency control block that stores the phase and frequency control inputs and uses them to calculate the phase angle of a rotating complex vector. The other is a sine/ cosine block that performs a lookup on the phase value and generates the appropriate amplitude values for the sine and cosine outputs. The multiple 16-bit buses on the chip bring the pin count up to 84 leads on the PLCC version and 85 on the PGA option.

Tackling signal filtering in adaptive or polyphase systems as well as for image processing or correlation, the HSP43168 dual FIR filter provides two independent 8-tap filters that operate at clock rates of 25.6, 30, or 40 MHz. The filters employ 10-bit data words and 10-bit coefficients, and store up to 32 coefficient sets on chip. Coefficients can be changed, cycle-by-cycle, which enables the filter to easily handle polyphase or adaptive filtering.

The two filters can be cascaded to form one 16-tap filter. The filter can implement 16-by-16 2D kernel operations or perform decimation with or-

ders of up to 16, turning the filter into a unit with 256 effective taps. The FIR cells can be configured to perform quadrature filtering, complex filtering, 2D convolution, 1D or 2D correlations, and interpolation or decimation filtering. Like the 16-bit NCO, the FIR filter comes in an 84-lead PLCC or 85-pin PGA package.

Matching digital signals, the HSP45256

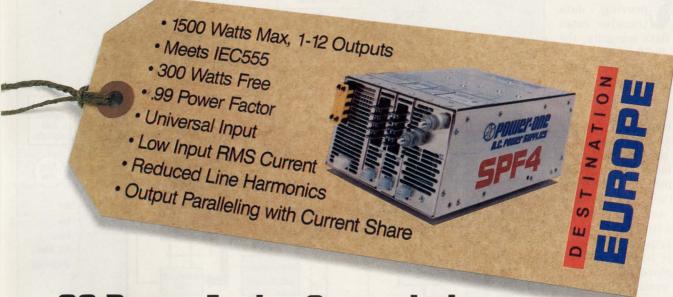
256-stage correlator provides eight 32-tap stages. The stages can be cascaded internally to process 1-, 2-, 4-, or 8-bit input data with a 1-bit reference. The array can be configured for 1D or 2D operation. Unused taps can be masked out to reduce the correlation length. Depending on the number of input-data bits, the correlation length can range from 256 down to 32 taps. The chip can also be configured as two separate correlators with window sizes from 4 by 32 to 1 by 128 bits. Correlation data rates can be 20 or 25.6 MHz maximum. The HSP45256 also comes in an 84-lead PLCC or 85-pin PGA.

Finally, the HSP 45240 address sequencer supplies most of the system logic needed to generate the data addresses to quickly feed data structures to the filter and correlator chip. It will also come in 33-, 40- or 50-MHz versions.

Samples of all units are available from stock. In 1000-unit lots, the least-expensive versions of each chip—the 33-MHz HSP45102 NCO, the 16-bit 45106 NCO, the 30-MHz 43168 FIR filter, the 20-MHz 45256 correlator, and the 33-MHz 45240 address sequencer—sell for \$13.08, \$34.62, \$67.70, \$42, and \$20.67 each, respectively.

Harris Corp., Semiconductor Div., 1301 Woody Burke Rd., Melbourne, FL 32902; (407) 724-3739. CIRCLE 487

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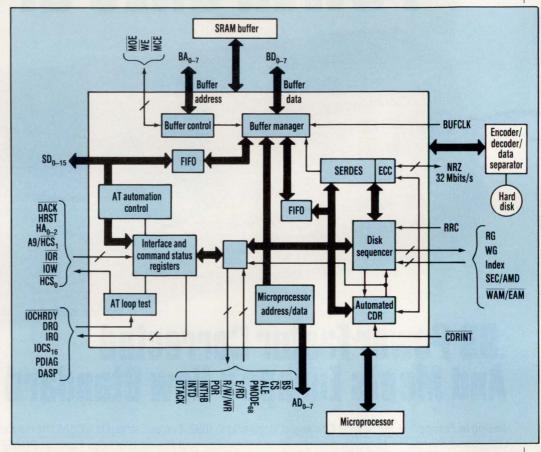
DRIVE CONTROLLER SIMPLIFIES EMBEDDED ISA AND EISA INTERFACES DAVE BURSKY

educing overheads, improving data transfer rates and data integrity, the AIC-8060 intelligent disk controller integrates more features that previous-generation devices. This suits the controllers for use in 2.5- and 3.5-in. harddisk drives. The chip is the latest extension of Adaptec's AIC-6000 and 7000 series disk controllers and includes features such as automatic AT sequencing, automatic buffer control, extensive internal test and system diagnostic capabilities, and support for an external 16bit local microcontroller.

The AIC-8060 works with a local microcontroller to perform the ISA/EISA interface, buffer control, disk se-

quencing, and error correction. The microcontroller communicates with the 8060 by reading from and writing to the 8060's registers. The registers appear to the microcontroller as unique memory or I/O locations that are randomly accessed and operated upon. Automatic read and write data tranfers can be done without processor intervention. Transfers can be single- or multiple-sector in length.

Host data rates of up to 10 Mbytes/s are supported with 16-bit transfers for data and 8-bit transfers for error checking and correction bytes on the host bus. The chip can support any AT-bus interface speed thanks to programmable and automatic wait-state insertion. The onchip ECC circuits detect and correct errors in the disk data stream as the data is read from the disk. The chip can generate a 32- or 56-bit fixed | take place at up to 15 MHz, with a 30-



polynomial ECC or an 88-bit Reed-Solomon ECC code for the data field and a 16-bit CRC-CCITT for the header field. The on-chip hardware performs autocorrection of a sector within a 1/2 sector time. The chip supports an 8 or 16-bit parallel interface mode and a direct-memory access mode with an on-chip slave DMA controller. An on-chip 16-byte speed-matching FIFO register between the host port and the data buffer maximizes data throughput. Master-slave logic for daisy-chaining two embedded disk controller drives on a PC AT is also included on the chip. Programmable powerdown modes let the chip reduce system power while nonactive.

Up to 256 kbytes of external static RAM can be addressed by the chip's buffer controller. Data transfers can MHz buffer clock. Thanks to a programmable interface, different speed SRAMs can be supported. The host, disk, and ECC circuits all have dedicated pointers into the data buffer. All ports into the buffer RAM may be active simultaneously in either direction. Circuitry in the 8060 resolves priority conflicts between the disk, correction, host, and microcontroller ports.

Controlling the internal workings of the chip is a programmable 31word x 32-bit RAM-based sequencer that handles primary format, read, write, and verification operations. Data rates as high as 32 Mbits/s of non-return-to-zero-coded data can be handled by the sequencer. Automatic zero-latency reads can be performed by the sequencer with virtually no microcontroller intervention. Also on the chip is a programmable

Go ahead ... add 5 psec



Picoseconds are no problem for the DG535 Precision Pulse & Delay Generator.

The DG535 provides 4 edge (delay) and 2 pulse (delay and width) outputs, all with 5 ps resolution, 1000 sec range, 50 ps rms jitter, and adjustable output levels. The outputs drive 50 Ohms or high impedances to 4 Volts with a slew rate of 1 V/ns - just right for driving TTL or ECL or even high speed analog circuits. Throw in the 35 Volt output option and you can trigger almost anything. For even greater accuracy and stability, add the 1 ppm optional timebase.

Top it off with the intelligent menu-based front panel and standard GPIB interface, and the DG535 is probably the most versatile timing generator you can find.

On the bench or in a test environment, the DG535 has the accuracy, stability, precision, and reliability you need to solve your tough timing problems - all at a price you can afford. Call SRS for more information on the DG535, even if you don't need picosecond resolution.



DG535

\$3500

- 4 delay, 2 pulse channels
- 5 ps delay resolution
- 50 ps rms jitter from trigger
- Adjustable output levels to 4 Volts
- 0 to 1000 sec delay range
- Internal/external trigger to 1 MHz
- Internal/external timebase
- 9 location set-up memory
- · GPIB interface standard
- ±35 Volt output option
- 1 ppm timebase option
- 100 ps rise/fall time option



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CIRCLE 175 FOR U.S. RESPONSE
CIRCLE 176 FOR RESPONSE OUTSIDE THE U.S.

servo event counter to support embedded servo or defect skipping with zone-bit recording.

The local microcontroller interface ties into Intel or Motorola-type multiplexed address/data buses and uses a 13-bit address and an 8-bit data bus. Two interrupt lines are available. All interrupt sources are individually maskable, allowing interrupt or polling operations. On the host-bus side, the 8060 emulates the ISA/EISA task file, which contains the 11 I/O registers that enable the host PC to set drive configurations. execute commands, and check their status. The AIC8060 notifies the host when it finishes executing a command by posting the appropriate status and/or generating an interrupt.

The AIC-8060 comes in a 128-lead quad-sided flat package and in lots of 10,000 sells for \$17.50 apiece. Delivery of samples is from stock.

Adaptec Inc., 691 S. Milpitas Blvd., Milpitas, CA 95035; Steve VonderHaar; (408) 945-8600.

CIRCLE 485

EISA SLAVE CHIP TRANSFERS 33 MBYTES/S

The HD64981F EISA interface chip simplifies slave-interface-card implementation. Fully EISA compatible, it transfers 33 Mbytes/s over the EISA bus. Built-in control registers allow programming of the chip's peripheral functions and address decoding of two memory and four I/O areas. Memory and I/O decoding, plus interrupt and DMA control, can be configured. Each of two user DMA interrupt channels can be assigned to one of the four EISA DMA and interrupt channels. If those channels aren't used, the signal pins turn into a 6-bit input port and a 6-bit output port. EISA board ID is supported through the use of an external PLD or PROM. The chip has a user-programmable 4-bit output port for external control tasks. Samples of the chip come in 100-lead PQFPs for \$16 each in 1000-unit lots. An evaluation board (US64981EVB1) costs \$625 in single-

Hitachi America Ltd., Semiconductor and IC Div., 2000 Sierra Point Pkwy., MS-080, Brisbane, CA 94005-1819; John Palladino, (415) 589-8300.

CIRCLE 488

E²PLDs SUIT STATE-MACHINE DESIGNS

GS-Thomson Microelectronics' CMOS GAL-6001S electrically erasable PLD is said to have an architecture well-suited to the design of state machines whose functions depend on their past history, as well as on current input signals. According to SGS-Thomson, the chip differs from rival PALs in that it contains a programmable AND array, a programmable OR array, and 38 logic macrocells configured in a 78-by-64-by-36 FPLA architecture. Other PALS are simpler, says SGS, generally with a programmable AND array feeding a fixed OR array.

Eight of the macrocells are buried in the logic structure for storing past state information; ten more are associated with inputs to the array, and a further ten are dedicated to output. Both input and output macrocells can be configured as asynchronous, latched or registered I/O, allowing data synchronization, merging, and widowing operations to be handled without external devices. Chip configuration is specified by a 68-bit-architecture control word, while a 72-bit user electronic signature can be employed to store pattern revision numbers, manufacturing dates, and other user-defined data. A security cell prevents unauthorized copying of array patterns by disallowing read access to the AND and OR arrays, unless the entire pattern is first erased by a bulk-erase operation.

Other features include a registered preload capability that allows all of the registers and buried macrocells to be preloaded to any desired state. That enables the user to test recovery from illegal states that might arise from power

surges or brownouts.

Maximum clock-to-output delay is 12 ns, and typical current consumption is 90 mA. Packaging is in 24-pin, 300-mil DIPs or 28-pin PLCCs, which are compatible with standard hardware and software programming tools. SGS guarantees 100% field programmability and claims minimum data retention of 20 years. In quantities of 3000, prices range from \$4.60 to \$5.30, depending on package. Availability is now.

SGS Thomson Microelectronics
Ltd., Planar House, Globe Park,
Marlow, Buckinghamshire, SL7
1YL, United Kingdom.

PETER FLETCHER

MEMORY-CARD HOLDS FLASH OR LAN FUNCTION

ow that the 68-pin memory card standard (PCMCIA 2.0) has been locked in by the memory-card manufacturers, companies are investigating ways to exploit the interface for storage and I/O functions. Consequently, Intel has developed a 2400-baud MNP5 modem that fits in the same 68-pin card format, in addition to offering a 2-Mbyte flash-based memory card. To support both memory-card and function-card interfaces, Intel has also developed the 82365SL. To standardize the interface for the function cards, the company also created an interoperability guideline called ExCA, short for exchangeable card architecture. A number of other card manufacturers have agreed to follow the ExCA open-systems architecture so that common drivers can be written, thus permitting widespread use of the cards.

The 82365\$L embodies the ExCA definition and provides interchangeable support for I/O and memory cards in the same socket. The chip holds power-management functions and inter-

faces to the ISA (AT) bus and to two PCMCIA-compatible card sockets. It reduces the interface to less than 2-in.² and eliminates system configuration jumpers because it can dynamically configure the cards in the system.

The flash memory card is just 3.3-mm thick, matching the dimensions of the PCMCIA standard. The modem card, however, employs the 5-mm-thick alternative option that's also part of the standard. In that credit-card-sized package is a full 2400-baud MNP5 modem, the first two versions of which will be offered with U.S. or Japanese telephone-system compatibility.

In 1000-unit lots, the U.S. modem card sells for \$200 apiece, while the Japanese version is \$230 each. In similar quantities, the 2-Mbyte flash card goes for \$375 apiece, while the 82365SL sells for \$35 each. Samples of all are available from stock.

Intel Corp., 3065 Bowers Ave., P.O. Box 58065, Snata Clara, CA 95052-8065; (800) 548-4725.

CIRCLE 489

DAVE BURSKY

WE'VE GOT TWO WORDS FOR PEOPLE LIKE YOU.

FAX VODEM \faks'vo-dem\n
[origin: Yamaha LSI] 1: world's first single-chip
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multimedia communications device 3: transfers data,
ADPCM voice and caller I.D. 3: transfers data,
fax and voice via a single line

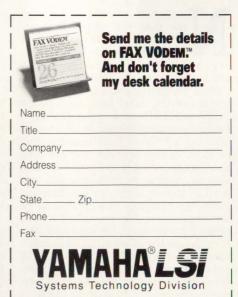
If you're one of those people who goes around integrating communications devices into PCs, laptops and other hardware, we've got two words for you — FAX VODEM™.

What do they mean? In a word, plenty. Yamaha defined FAX VODEM on September 26, 1991, as a major breakthrough in multimedia communications. And now it's going to change the way you communicate. Because with FAX VODEM, you'll be able to integrate Fax. Data. ADPCM voice communications. And caller I.D. All on a single line. And all with a single-chip LSI that'll give your

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So start integrating FAX VODEM into your new products. And when your colleagues notice what a great communicator you've become, just tell them you've got two words for people like them.



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ENHANCED CONTROLLERS PACK MORE RAM, EPROM

dditional RAM and nonvolatile storage on several 8-bit microcontrollers eases the programmer's task when trying to squeeze programs created with high-level C-language tools. The Philips-Signetics 83C524 and 528 controllers, which are 8051-compatible derivatives, now have 512 bytes of static RAM. The 80C528 is the ROMless version of the 83C528, which contains 32 kbytes of ROM. The 87C528 holds 32 kbytes of EPROM.

Versions of the 8XC524 offer the same options, but with 16 kbytes of nonvolatile memory. The controllers are 40-pin devices and include four 8-bit I/O ports, two serial ports (one a full UART and the other an IIC-compatible port), three 16-bit counter-timers, and watchdog timer. Two speed grades of the controller are available—one that has a 16-MHz upper limit and can operate from 3.5 to 16 MHz, and another with a 20-MHz upper limit.

In another move, the company added other controllers that have IIC serial

ports and on-chip EPROM storage with a one-time-programmable plastic package option. The 83C652 and 654 controllers are also compatible extensions to the 80C51 family and include 8 kbytes or 16 kbytes, respectively, of EPROM and 256 bytes of static RAM. Additional resources include four 8-bit I/O ports, two 16-bit counter-timers, and a full UART serial port. Both devices also come in either 16- or 20-MHz versions and are housed in either 40-pin DIPs or 44-lead PLCCs or PQFPs.

Prices for the 16-MHz controllers start at \$7.50 each for the ROM-based 83C528 in lots of 10,000, and go up to \$38.50 each in lots of 1000 for the EPROM-based 87C528. Prices for the 87C652 start at \$22.50 each in lots of 1000 for the DIP version, and \$28.50 each for the 87C654, also in lots of 1000.

Philips Components/Signetics Co., 811 E. Arques Ave., P.O. Box 3409, Sunnyvale, CA 94088-3409; Thomas Brenner, (408) 991-3552

CIRCLE 491

■ DAVE BURSKY

CLOCKED FIFO REGISTERS CLAIM SPEED LEAD

quartet of clocked first-in/first-out registers with fixed or programmable status flags can be used in systems clocking up to 70 MHz. Claimed by Cypress Semiconductor to be the fastest commercial FIFO registers, the chips come in versions with fixed flags—the CY7C441 and 443—and with programmable flags—the CY7C451 and 453. The 441 and 451 have 512 words by 9 bits of storage; the other two have 2 kwords by 9 bits.

The 441 and 443 include Empty, Almost Empty, and Almost Full status flags. In the almost-empty and almostfull states, the flag signals the host when the memory is within 16 words of being empty or full. The status flags are actually signals from two flag pins that are decoded to provide four states. The fourth state not previously mentioned is the intermediate state, which indicates that more than 16 words are left in the memory and more than 16 words of storage are available.

Offering user-programmability of the status flags, the 451 and 453 provide the user with three status pins when the registers are used in their standalone mode. When cascaded, either the width or depth can be increased. However, the 70-MHz top speed possible in the standalone mode drops to about 50 MHz in the cascaded mode. The three status pins can be decoded into six status conditions: Empty, Almost Empty, Less Than Half Full, Greater Than Half Full, Almost Full, and Full. The Almost Empty/Full flag is lost when the registers are cascaded to increase depth. When programmed, the user can set values for all flag states except for the Empty and Full conditions. For instance, the Almost Empty flag can be set for any value from 1 to 240. The 441 and 443 come in 28-lead DIPs or 32-lead PLCCs or LCCs, while the 451 and 453 come in 32pin DIPs or 32-contact PLCC or leadless packages. In lots of 100, the CY7C441, 443, 451, and 453 sell for \$25.85, \$41.30, \$33.75, and \$56.80 each, respectively, for PLCC packages. Delivery of samples is from stock.

Cypress Semiconductor Corp., 3901 N. First St., San Jose, CA 95134; Bill Eichen, (408) 943-2600.

CIRCLE 493

■ DAVE BURSKY

SPEED WINDOWS WITH ACCELERATED VGA CHIP

y adding hardware cursor support and bit-block-transfer (bitBlt) logic onto a VGA controller chip, Western Digital created a video chip that accelerates most of the operations encountered when using the Microsoft Windows graphical user interface on PCs. The chip, the WD90C31, is a pin-compatible upgrade to the company's best-performing VGA chip, the 90C30. However, it can execute video operations in windows an average of four or five times faster than any other dedicated VGA (or Super VGA) controller chip.

Located on the chip is logic for a 64-by-64-by-2-pixel hardware-supported cursor, and for displaying images of up to 1024-by-768 pixels with up to 256 colors at a noninterlaced refresh rate of 72 Hz. In the lower-resolution modes, the chip can display up to 65,000 colors, giving VGA displays the display capability of IBM Corp.'s new XGA standard. Character fonts with 6 to 16 dots (character width) per character and up to 132 columns of text are also supported by

the controller.

The 90C31 can operate with a 50-MHz MCLK signal, which permits the system to use 60-ns Fast-Page-mode DRAMs rather than the more-expensive video RAMs. The chip's videomemory interface can be configured to operate with 16- or 32-bit-wide memory arrays. Any of three memory types-256k by 16, 256k by 4, or 64k by 16—can be used to form the storage area. The chip also provides a linear address space for up to 1 Mbyte of image data. An on-chip FIFO buffer provides some elasticity on the memory transfers, permitting the chip to operate at maximum performance levels.

In production quantities, the controller will sell for about \$30 when housed in a 132-lead plastic quad-sided flat package. It's also available in a 144-lead metal QFP. Samples are available immediately.

Western Digital Imaging, 8105 Irvine Center Dr., Irvine, CA 92718; Vipul Menta, (714) 932-4900.

CIRCLE 492

DAVE BURSKY

CPU COMBINES CACHES, FPU, AND R/W **BUFFFERS**

icking the best features to integrate on one chip, designers at Performance Semiconductor have created Piper-properly integrated performance easy rider—a highly integrated R3000A family member. On one chip, the company combined the R3000A CPU, the R3010A floatingpoint coprocessor, 4-word-deep read and write buffers, and cache-8 or 4 kbytes of instruction cache and 2 or 4 kbytes of data cache. Furthermore, all critical clock signals are generated and kept on the chip, simplifying system design and eliminating the need to route high-speed clock signals on circuit boards. Additional on-chip resources include two 32-bit counter-timers. Optimized for advanced embedded-control applications, the single chip replaces as many as 50 chips and cuts power requirements by 75% or more.

The cache arrangement on the chip gives designers a choice of two organizations that can be configured upon power-up. The base option upon powerup gives the Piper chip 8 kbytes of Icache and 2 kbytes of D-cache. By loading some parameters, the cache can be balanced to 4-kbytes each of I and D

The on-chip read and write buffers reduce the number of times the CPU must wait to store results or read data. The read buffer also supports block refills to further improve system performance. Both static column and pagemode DRAMs are supported.

The two on-chip counters can be used as watchdog timer circuits profiling or scheduling clocks. Or they can be used

as event counters.

cache.

Housed in a 160-lead quad-sided flat package, the Piper is available in versions that run at 35, 40, and 45 MHz. At 35 MHz, the processor dissipates about 5 W, while the 45-MHz version consumes 6 W, typical and 7.5 W, worst case. In quantities of 10,000 units, the 40-MHz version sells for \$143 apiece. Samples of the processor chip will be available in November.

> Performance Semiconductor Corp., 610 E. Weddell Dr., Sunnyvale, CA 94089; Jim Keim, (408) 734-8200 CIRCLE 494

DAVE BURSKY

CONTROLLER SUPPORT CHIPS ADD RAM, EPROM

pplications that employ microcontrollers most often require off-chip memory and I/O pins as extensions. Typically, RAM and EPROM are needed to suit the application, or as in the case of ROMless controllers, multiple memory chips must be attached. With the addition of five members to its programmable system device family, WaferScale Integration offers a variety of EPROM, RAM, and I/O expansion options on single chips to satisfy many systems.

Included in the PSD3xx family are five chips that can add up to 1 Mbit of UV EPROM, 16 kbits of static RAM, and 19 individually configurable I/O lines. Built-in page logic expands the address space of controllers that have limited address spaces of their own. The chips also contain two programmable arrays (Pads A and B) that provide 40 product terms and up to 16 inputs and 24 outputs, plus a "no-glue" interface for most 8- and 16-bit microcontrollers and DSP chips. The programmable logic in Pad A can be used to map the I/O ports, eight segments of

EPROM and SRAM, anywhere in the address space of the controller. Pad B logic can implement up to four sum-ofproduct expressions based on address

inputs and control signals.

Previously, the company had one device, the PSD301, which included 256 kbits of EPROM and 16 kbits of SRAM. and could be configured as a byte-wide or 16-bit-wide device. The family now includes the PSD302 and 303, which double or quadruple (512 kbits or 1 Mbit) the on-chip EPROM storage. Three other chips, the PSD311, 312, and 313, are identical to the 301, 302, and 303, except that they have a dedicated 8-bit host interface.

PSDs come with access times of 120, 150, or 200 ns and are housed in various 44- and 52-lead packages. As a price example for production quantities, the PSD312 sells for less than \$9 each, while the more flexible 302 goes for less then \$11 each.

WaferScale Integration Inc., 47280 Kato Rd., Fremont, CA 94538-7333; Dale Prull, (510) 656-5400.

CIRCLE 495 DAVE BURSKY

SINGLE-CHIP CONTROLLER PACKS EEPROM, RAM

NEC has added two controllers with EE-PROM-based storage to its K2 series of 8-bit single-chip controllers. The two models include the $\mu PD78244$, which packs 512 bytes of EEPROM plus 512 bytes of RAM and 16 kbytes of ROM, and the 78243, which has no ROM. Both versions can address up to 64 kbytes of program memory and up to 1 Mbyte of external data memory. The 78244 can execute instructions in 333 ns while the 78243 requires 500 ns per instruction. Additional features include an 8-bit ADC, two serial ports (one UART and one clocked serial interface), and one 16-bit and three 8-bit counter-timers. All features are supported by a high-performance interrupt controller-NEC's proprietary peripheral management unit. The controllers come in 64-pin shrink DIPs or PQFPs. Prices for the ROM version start at \$17 each in lots of 10,000: the ROMless version is \$14 in similar quanti-

NEC Electronics Inc., 401 Ellis St., P.O. Box 7241, Mountain View, CA 94039; Ron Mitchell, (415) 965-6094. CIRCLE 496

VOLUME SHIPMENTS **CUT VIDEO CONTROLLER** PRICES BY 60%

The price of Inmos Ltd. G300 series range of color-video-controller (CVC) chips have been cut by 60%. In quantities of 1000, individual chip prices now range from \$55 each for an 85-MHz version up to \$128 each for a full-specification 110-MHz controller chip that supports a 64-bit pixel bus that's compatible with microprocessors like Intel's i860. Dave Partinton, graphics marketing engineer at Inmos cites increases in shipment volumes as a factor in reducing production costs. These productioncost reductions in turn have led to the lower device prices. The company says it has shipped over 25 million CVC chips to personal-computer and workstation makers.

All CVC chips support graphics resolutions up to 1280 by 1024 pixels. Two chips in the series also provide hardware cursors.

Inmos Ltd., 1000 Aztec West, Almondsbury, Bristol, BS12 4SQ United Kingdom, Phone: +44 (0)454 616616. GIRGLE 497

NFW LITERATURE

BURN-IN SYSTEMS

Conventional heat soak rooms for burning in power supplies are very limited in the nature and efficiency of the tests they perform. A brochure from Intepro discusses those limitations and goes on to describe what it has done about them, which is develop a new computer-controlled burn-in system that makes use of dynamic stress-cy-cling techniques. The brochure dis-cusses the technical concepts behind the system's advanced source-, load-, and temperature-cycling capability. It also gives details on the various components that can be used to build a custom

Intepro Systems Inc., Six Fortune Drive, Billerica, MA 01821; (508) 663-7555, Mike O'Connor. CIRCLE 498

CATALOG DETAILSDC-DC CONVERTERS

Eleven new families have been added to a line of dc-dc converters and are detailed in a short-form catalog. The catalog contains over 330 standard models and over 20 added features such as N+1 redundancy, alternative pinouts, and others. Standard models are rated from 1/2 W to 200 W, and custom units are rated up to 500 W.

International Power Devices Inc., 155 N. Beacon St., Brighton, MA 02135; (617) 782-3331 CIRCLE 499

FREQUENCY DISCRIMINATORS

A line of frequency discriminators that covers the frequency range from 100 MHz to 18 GHz is described in a sixpage color brochure. The brochure describes the architecture and operation of the modular fast filter discriminators, gives performance curves, and includes a limited amount of tabular data on three models.

The filter frequency discriminators are built around a pair of filters, which provide a phase shift that is proportional to input frequency. The devices can process pulses as narrow as 30 ns, operating under signal-to-noise ratios as low as 3 dB.

K&L Microwave Inc., 408 Coles Cir., Salisbury, MD 21801; (301) 749-2424. GIRGLE 500

WAFER ETCHING

Lam Research's Rainbow family of single wafer-etching systems is reviewed in a new 16-page color brochure. The brochure includes technical descriptions, photos, scanning electron microscope images, and extensive baseline performance data on each product in the Rainbow line.

The Rainbow 4500 dielectric etch system uses a patented split power-reverse RF plasma source for uniform results from one wafer to another and within a wafer. As the brochure describes, the system works well on 200mm wafers with geometries below half a micron.

Lam Research Corp., 4650 Cushing Pkwy., Fremont, CA 94538; (415) 659-6692 (Karen McLennan). GIRGLE 501

INDUSTRIAL CONTROL

A 24-page industrial source catalog from Acculex gives data on the company's lines of digital panel meters, signal conditioners, timers, totalizers, communication products, and printers. It includes complete specifications, applications information, wiring diagrams, details on accessory products, and

Among the new products featured in the catalog are the DP-680 series of low-cost rate meters, totalizers, and

timers, as well as various communication interface boards for plug-in use in the IBM PC/XT/AT computer and compatibles.

Acculex, 440 Myles Standish Blvd., Taunton, MA 02780; (508) 880-3660. CIRCLE 502

CATALOG-ON-DISK SPEEDS SUPPLY CHOICE

A computer disk is available that contains complete and up-to-date information on over 400 standard ac-dc and dcdc power converters. The PowerPath digital catalog dramatically simplifies the task of matching power supplies with applications.

The disk runs on any IBM PC or compatible (256 kbytes of RAM are required) and is available for both 5-1/4in. and 3-1/2-in. drives. Subscribers to the catalog will automatically receive the latest updated disks as they are issued.

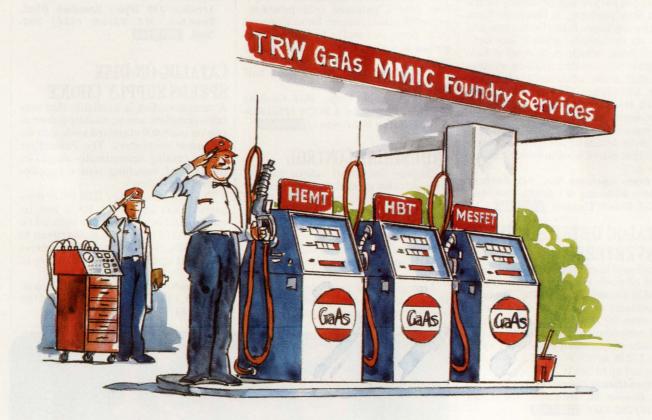
Computer Products/PCA, 3797 Spinnaker Ct., Fremont, CA 94537-5102; (415) 657-6700 CIRCLE 503



CIRCLE 265 FOR U.S. RESPONSE

CIRCLE 266 FOR RESPONSE OUTSIDE THE U.S.

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FOR ENGINEERS, PAY INCREASES OUTPACE INFLATION, BUT SALARY COMPRESSION CONTINUES

BY SHERRIE VAN TYLE

ith the U. S. economy struggling out of a recession, what kind of pay increase can engineers expect this year? And what about that perennial thorn for engineers, salary compression? Is management the only growth path open to an engineer who has 15 years in the profession? To gather readers'

opinions on these and other pressing salary issues, ELECTRONIC DESIGN surveyed 1500 readers in July.

On the face of things, the survey shows that ELECTRONIC DESIGN readers seem to have fared pretty well. Four out of five readers received a raise in the past 12 months (see the figure). And the average increase was 6.10% for the past 12 months, compared to 5.95% for the previous 12-month period. One blot in this picture is that salary compression still holds sway for some readers (see "Engineers sound off on salary ceilings," p. 156).

The reader, on average, is male and 41 years old. With 15 years of experience, he has a BSEE and earns \$54,985. The most common title is that of design engineer, for 21% of readers; senior engineer follows, for 16%; and project

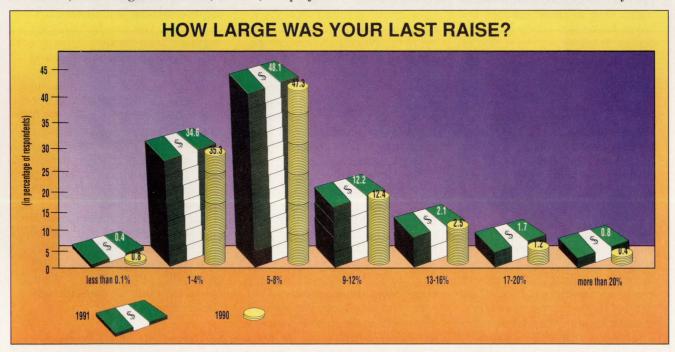
engineer, 12%. And he works for a company with \$474 million in annual sales. These figures are weighted averages based on median values of readers' responses.

The 6.1% average raise for ELECTRONIC DESIGN readers stacks up pretty well against what the average U. S. white collar worker can expect this year. A nationwide survey of 3000 companies by William M. Mercer Inc. shows that salaries rose an average of 5.3% in 1991, on the heels of a 5.5% increase in 1990. Next year should see an average raise of 5.2%.

What's more, readers' 6.1% average increase looks good in light of relatively stable consumer prices in the U. S. The consumer price index (inflation rate) is expected to level off at 4.7% for 1991 compared with a 6.1% advance for 1990, the largest price surge in eight years, according to the U. S. Bureau of Labor Statistics. And 1992's CPI is expected to hover between 3.8 and 4%.

But increase averages don't tell the whole story. For one thing, one of five readers did not receive a pay raise in the past 12 months. "I've had no raise for three years," says one reader. Another says, "It seems the only way to increase your salary is to change companies."

These readers are not alone. The Mercer survey shows



that in 1991, one in 25 companies froze pay or deferred pay increases for hourly or salaried employees; one in 15 companies had such freezes for their executives. In contrast, last year, just one in 100 companies had plans to freeze salaries or defer raises, according to the Mercer poll.

It's also worth noting that 35% of ELECTRONIC DESIGN readers who received raises got the smallest percentage of 1 to 4%, while 48% received raises in the range of 5 to 8%. A 9 to 12% raise was reported by 12% of the readers. Also of interest is that the total number of readers reporting raises for the past 12 months dropped 2.2 percentage points com-

pared with the previous 12-month period (see the table, p. 159).

Are there any bright spots for readers? One encouraging note is that next year, 2% of companies expect to freeze salaries versus the 11% that held off raises this year, according to a survey of 1100 companies by accountants Coopers & Lybrand.

Still, some readers aren't worried about pay increases—because they're more concerned about keeping their jobs. "The major problems in engineering are unemployment and unpaid overtime," a reader says. Echoes another, "Job security is of prime importance now."

Some segments of the electronics

business are faring better than others. Shrinking profit margins have hit computer makers hard, which has reverberated throughout the industry. Notes a reader, "The computer industry is in a state of turmoil for long-established companies. Ours has put on salary freezes to try to pull out of [its] problems."

Another engineer says, "My company has financial problems and cannot pay more. I have taken a salary

cut instead of job loss."

Mergers and acquisitions have eliminated entire engineering departments. Corporate downsizing and more time-to-market pressure often result in a longer work week

ENGINEERS SOUND OFF ON SALARY CEILINGS

'EE salaries do cap in the \$60,000-range unless the EE is some type of manager, excluding a project or team leader.'

s in past surveys, readers have plenty to say about salary compression—that is, a leveling off of engineers' salaries after 15 or so years in the profession. In other professions, such as medicine and law, income typically rises in steady jumps until retirement. One in three readers believes his or her salary has hit a ceiling. Readers peg the ceiling at an average of \$63,500.

Zeroing in on readers without management responsibilities and the question of salary ceilings, 29% think their salaries have topped out while 71% think that future raises are likely. These engineers are probably young, expecting plenty of growth ahead. Up one rung, among readers supervising one to five engineers, 41% think their salaries have hit a ceiling. Climbing another step, among engineers supervising 6 to 10 people, 46% think their salaries have hit a ceiling. A turnaround comes at the highest level—just 22% of higher level managers, those who supervise 10 or more engineers, think their salaries

have leveled off. This could well mean that these readers are managers with a growth path open to them. Still, their smaller number adds a caveat to a hard and fast conclusion.

When age is cross-referenced to the salary ceiling question, of the engineers who say their salary has hit a ceiling, more than half are 40 to 54 years old. And more than half of the engineers who say their salary hasn't yet hit a ceiling are 40 or younger.

To break through salary ceilings, some engineers enter management. Nonetheless, some engineers chose engineering because the technical aspects of engineering rather than the idea of managing people appealed to them. One reader says, "The only way to get a higher salary is to go further into management, which doesn't interest me."

Forcing a technically oriented person into becoming a manager can be disastrous. As one engineer points out, "The current salary structure lures the best engineer to move to management and often [to become] a substandard manager." Another problem derives from demographics that come into play here. The number of persons in the 30- to 49-year-old age bracket competing for management spots far exceeds the number of positions. As corporate downsizing continues, a flatter management flowchart further shrinks the number of open spots.

As one ELECTRONIC DESIGN reader points out, "The only way to make a significant increase in salary is to enter the saturated field of management.'

Other engineers circumvent ceilings by becoming indispensable to their companies. "In an engineering category, you have to offer something that others can't. Otherwise, you are just another engineer," one says.

Ceilings could also be considered a catalyst for change. "Engineers need to be flexible and continue to acquire new capabilities." says one respondent. Remarks another, "If I can't break through the ceiling, I'll probably either go out on my own or start in another profession." One reader agrees, "I plan to find another profession after I hit 15 years as an engineer."

Not all readers concur that ceilings exist: "They exist only in the minds of those unwilling to work hard and take bigger risks," says one reader. Others think individual talent punches through ceilings. For instance:

• "I feel there is no ceiling for

for engineers. One reader sums it up: "So much work, so little time." Another says, "My typical work day is 10 hours.

On another front, the U.S. government/military sector is facing a shrinking defense budget. Indeed, the Mercer survey shows that government workers are likely to receive the lowest pay raises of all economic sectors-about 4.6% next year. Government salaries on average are already lower than those in private companies, readers say. One estimates that "government employees are underpaid by 27 to 35% compared to industry." Another says, "Federal government salaries are

those who continue to increase their productivity, knowledge, and value to their employer. This cannot be measured by degree level alone."

- "Too many engineers expect to be paid at a certain level for a certain degree (or number of years of experience) rather than examining their value to the company they work for."
- "Ceilings imposed by industry aren't reflective of individual contribution.'
- "All engineers are not the same. Some have more knowledge than others and should be paid for their talents and contribution to the company as a whole."
- "In my years, I've seen too many lazy engineers! Companies should adopt a Scanlon plan type compensation package with a floating ceiling based on quality productivity."
- "Self-starters who are entrepreneurial often make millions."

Joseph Scanlon of the Massachusetts Institute of Technology came up with an employee cashincentive program in the 1930s and 1940s based on sharing the savings from a reduction in labor costs from a described standard.

far too low, especially with reference to high cost of living areas."

Keep in mind that engineers' salaries haven't risen uniformly over the years. A reader takes a historical per-

spective as he compares salaries with inflation rates: "I think engineering salaries have just kept up with inflation. The median salary income 20 years ago is almost equal to the median income today. So basically we aren't getting ahead." In a related vein, a reader says the wages in Silicon Valley "do not cover the cost of living, i.e., housing in the area."

Along the same lines, a reader describes his situation: From a gross salary of \$56,000, his take home net after mandatory deductions is \$36,000; deductions eat up \$20,000 or 35.7% of the gross. "The total annual increase in all deductions alonetax, retirement, medical insurance, Medicare, and so on-more than cancels out the approximately 4% annual cost-of-living adjustment. My effective salary is thus declining each year."

Despite some gripes and some ex-

ceptions, 73% of the respondents feel their current salary is comparable to others' pay for similar work within their companies. Comparing their pay with what other companies offer is another matter, however. About 46% of readers think their pay is comparable while 41% believe that they earn less than their counterparts at other companies.

Two-thirds of the readers say they're paid adequately for their work as an engineer. Not surpris-

O MUCH WORK, SO LITTLE TIME

ingly, engineers making higher salaries tend to believe they're paid adequately, or 81% of those making \$60,000 to \$65,000, vs. 59% of those making \$40,000 to \$45,000.

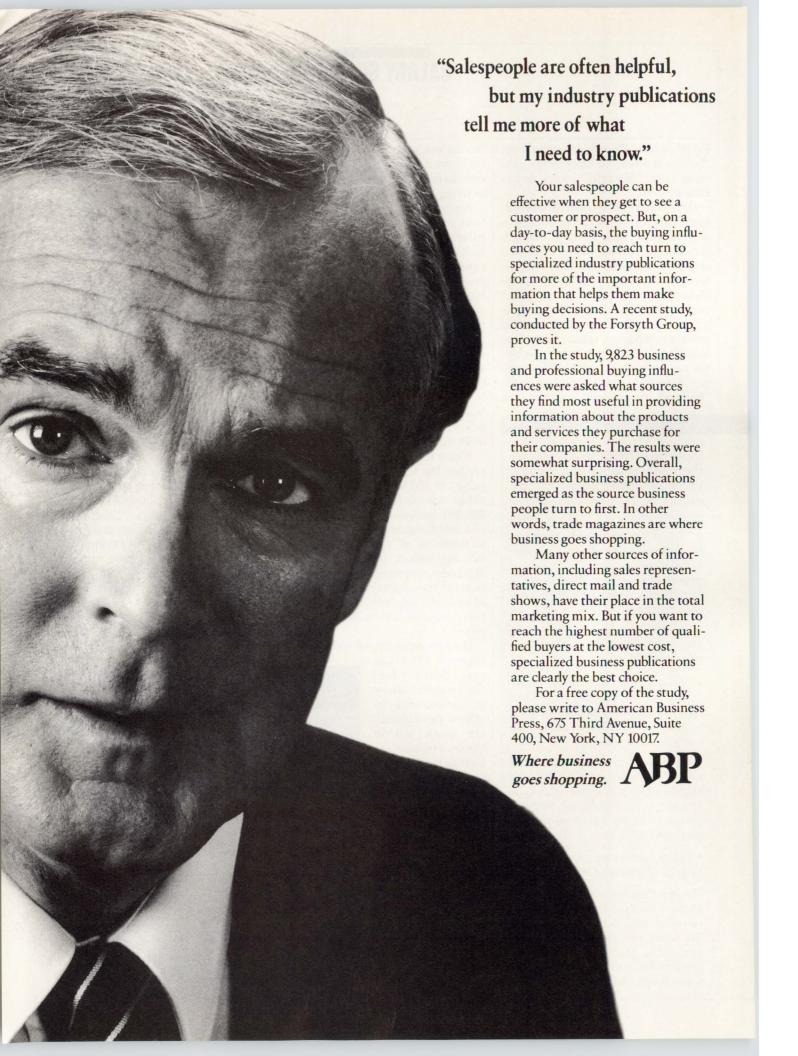
Several readers comment that age discrimination drags down engineering salaries and diminishes the profession's reputation. "Engineering salaries in general are low because managers place a low value on experience, presumably because the cost/benefit ratio is better for a young engineer versus an older engineer," he says. "The fact that this kind of incomplete analysis is so prevalent in the engineering community seems to confirm the suspicion that the quality of engineering is declining." Another says, "This profession gets better with age, and for its reward gets laid off-it's criminal."

One way to circumvent minimal cost-of-living raises and wage freezes is to reward engineers for outstanding work. A reader suggests assigning a percentage of gross revenue from a product or service to each group involved in gener-

VARIABLE PAY PROGRAMS ARE CATCHING ON

Type of program Percentage of comp	anies
Special award (cash award based on special contribution)	43
Current profit sharing	34
Incentive award based on individual performance targets	34
Recognition program	31
Lump-sum merit award (never made a part of base salary)	26
Company-wide bonus	20
Exception grants of restricted stock or stock options	18
Small group or team incentive	16
Gainsharing (gains shared by unit in cost reduction)	13
Pay for knowledge (skill-based pay)	10
Two-tier pay	3
Source: a survey of 2,700 companies by The Conference Board	d,

New York, N.Y., to which 537 companies responded.

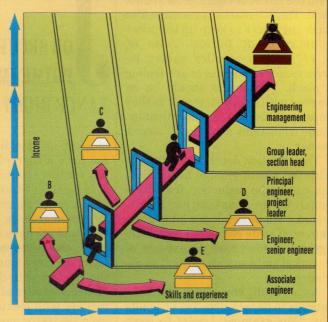


CLIMBING THE CAREER LADDER

ritical to career advancement for engineers is knowing when it's time to move on or to step up to the next level in their careers. To advance, engineers need to master a set of skills and then move promptly through a transition window to a higher level of skill, responsibility, and salary—as person A has done. The straight arrow represents the ideal relationship between experience and compensation. Deviating from this line inhibits success.

Persons B and C have wandered off course. Both became experts and their companies have compensated them accordingly. Both people are worth more to their current employers than in the marketplace, making them vulnerable in a recession when many others have their skills and are available at a lower salary.

Also vulnerable to layoffs, persons D and E have allowed themselves to stagnate. Perhaps thinking that job security depends on longevity, D and E have held the same jobs too long. Person E can't obtain a senior-level position because he or she is still performing junior-level functions. Although D has moved through the first level, he hasn't developed project control and supervisory skills to qualify for first-line management.



ating it—engineering, accounting, manufacturing, marketing, sales, and so forth. "In short, give tangible incentives to perform, aside from guaranteed base salary," he adds.

Such incentives could replace part of engineer's salaries. That's what several readers suggest: "Engineering salaries should be smaller with total compensation related to product revenues." Another says "Salaries should be more correlated to the impact the engineer has on the P&L of the product."

Another reader notes that, "engineers should receive yearly royalties on their designs, similar to copyrights for songwriters or authors."

The disparity in salaries between hands-on design engineers and managers is an ongoing source of friction. One engineer says, "The gap

between corporate managers and line managers grows wider as the gap between incoming and experienced engineers narrows," (see "Climbing the career ladder," above). Another, tapping into belief that engineers are the ones who really do the

work, says, "Higher-level management is overpaid for what they contribute or produce to the overall product." Another engineer plays a similar tune: "Compared with what managers or marketing/salespeople make for controlling or selling the products engineers create, I think our salaries are pitiful."

To remedy this, one reader suggests a dual career track "so that engineers and other technical people can be compensated on the basis of contribution."

Some companies are doing just that, though focused more on general performance. To motivate employees and reward good work by individuals, an increasing number of companies are adopting variable pay programs. A survey of 2700 companies by The Conference Board, New

York-based management consultants, showed that 76% of surveyed companies have in place at least one variable pay program. Most popular are special awards for outstanding individual effort, used by 43% of the companies (see the table, p. 157). Following that are current profit sharing and incentive awards based on individual performance targets.

One reader agrees with the board survey: "All engineers must be participants in a profit-sharing plan of the company and all companies must have a profit-sharing plan."

Some readers find it irritating that engineering salaries don't adequately reflect the amount of education required. As one engineer puts it, "Engineering salaries are generally low, especially when considering those of less skilled, blue-collar workers."

Another agrees, "Engineering salaries are low in comparison to other professions in the metropolitan area."

"For the amount of schooling to stay abreast of technology, engineers are poorly compensated relative to legal and medi-

DID YOU RECEIVE A RAISE?		
	1991	1990
Yes	80.1	82.3
No	19.9	17.7

cal fields." Most engineers have to spend money and time to keep up with the latest developments in their field. Time-to-market pressures also push engineers to keep up technically (ELECTRONIC DESIGN, June 13, p. 117). With smaller salary increases, some engineers are feeling a pinch. "Engineers should be rewarded with salary increases as they improve themselves educationally. Some companies don't do it," says a reader.

The situation deteriorates further with the recent change in the U.S. tax code—the deduction for educational expenses has been partly eliminated. "We have taken a hit in unreimbursed costs compared with managers who don't have the expense of technical skills maintenance," an engineer says.

As a result, companies want the courses to be task-specific, he points out. "For example, I want to learn

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more about shielding noise, but I do not have a current project that will pay for this external course."

In terms of education, 52% of readers have a college degree; another 29% have gone on to achieve a masters; and 5% have a doctorate. Typically, the more education readers have, the more money they make. Of the readers with doctorates, for instance, 80% earn at least \$55,000. For readers with master's degrees, 70% earn \$55,000 or more.

And bigger companies tend to pay engineers higher salaries: 45% of readers making \$75,000 or more work for companies with \$1 billion in sales. But working for a big company may have a down side in terms of salary. Several readers note examples of large companies sharing salary information with one another, "to keep salaries low."

Because just 2% of the respondents are female, no conclusions based on gender can be drawn.

ELECTRONIC DESIGN'S salary survey is based on a mail survey. On July 9, 1991, questionnaires were mailed to 1500 names selected randomly from ELECTRONIC DESIGN'S U.S. circulation.□

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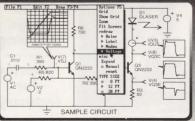
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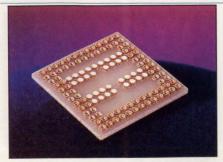
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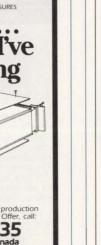
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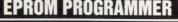
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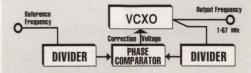
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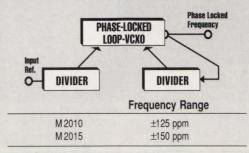
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