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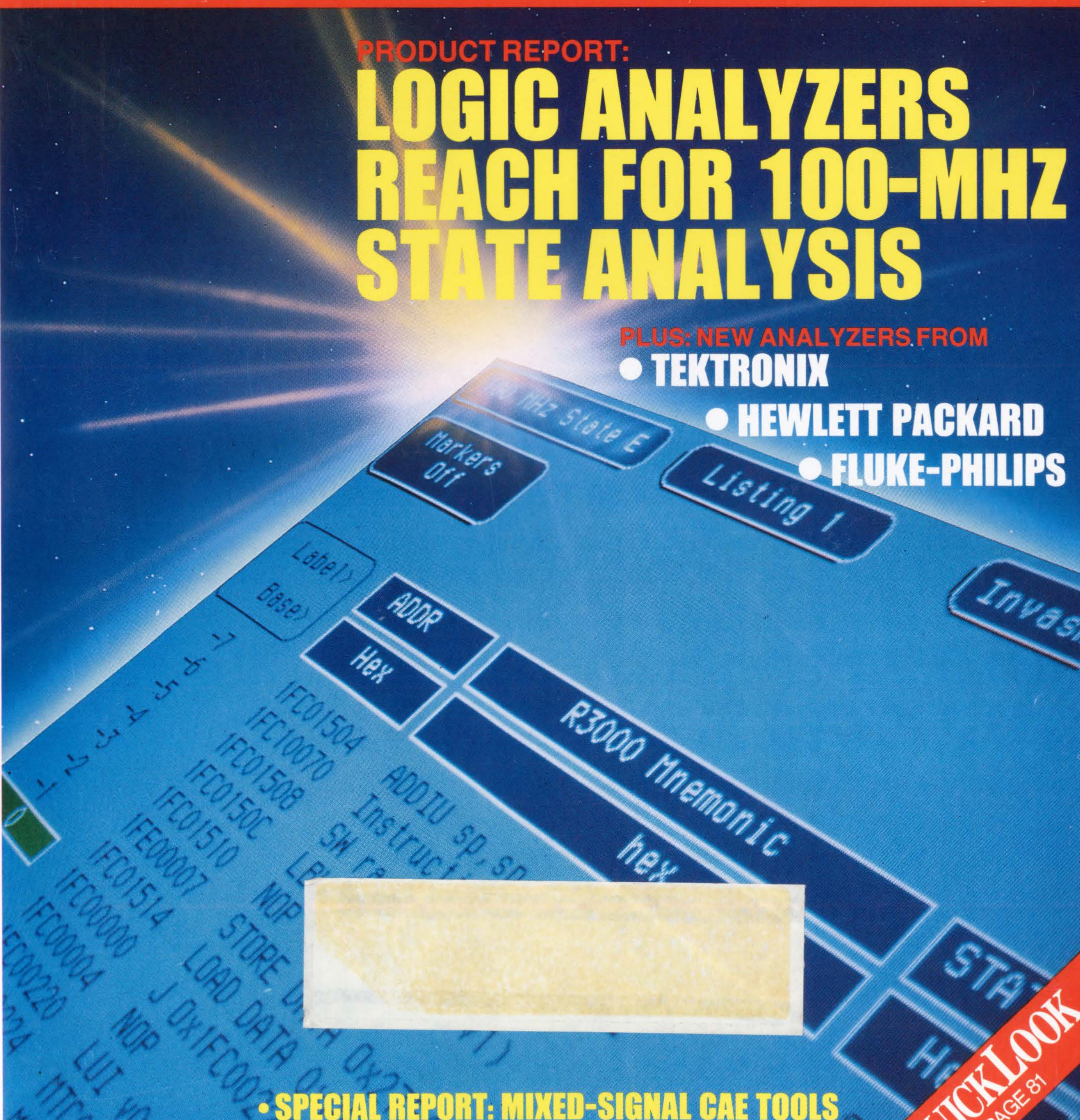

PRODUCT REPORT:

LOGIC ANALYZERS REACH FOR 100-MHZ STATE ANALYSIS

PLUS: NEW ANALYZERS FROM

- TEKTRONIX
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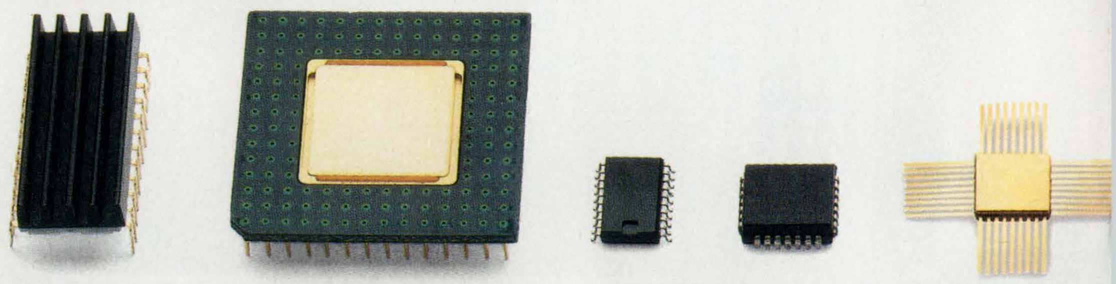
Our new pulse generators will test what you have.



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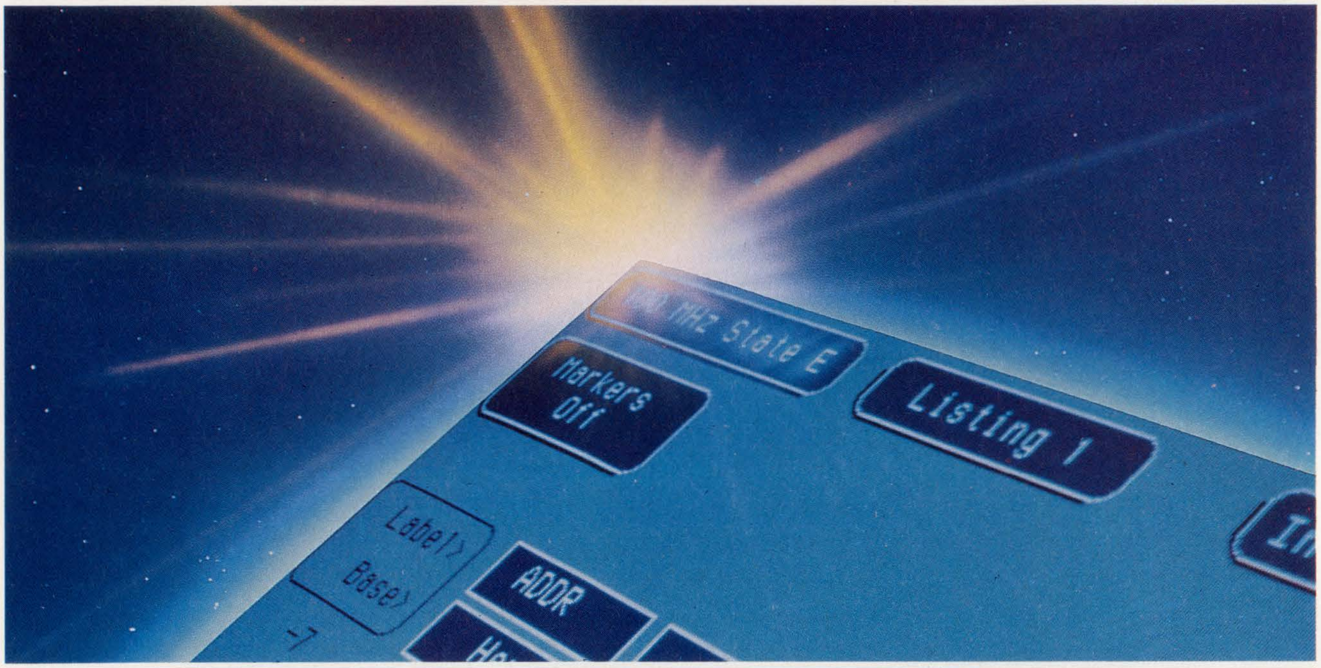

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Cover photo of HP 16500A screen courtesy of Hewlett-Packard Co.

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- First details on a new RISC embedded controller IC
- Wescon 90: What's new in CAE, test and measurement, and components
- Delving into the fine points of data-converter dynamic specs
- Achieving precision in linear ASIC devices
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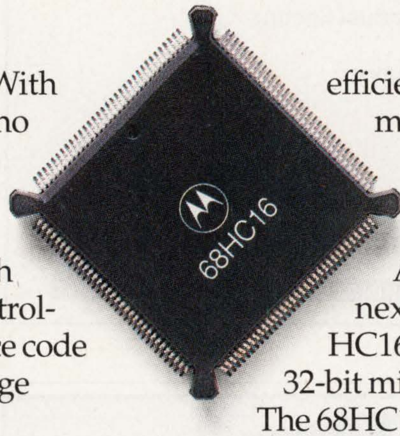

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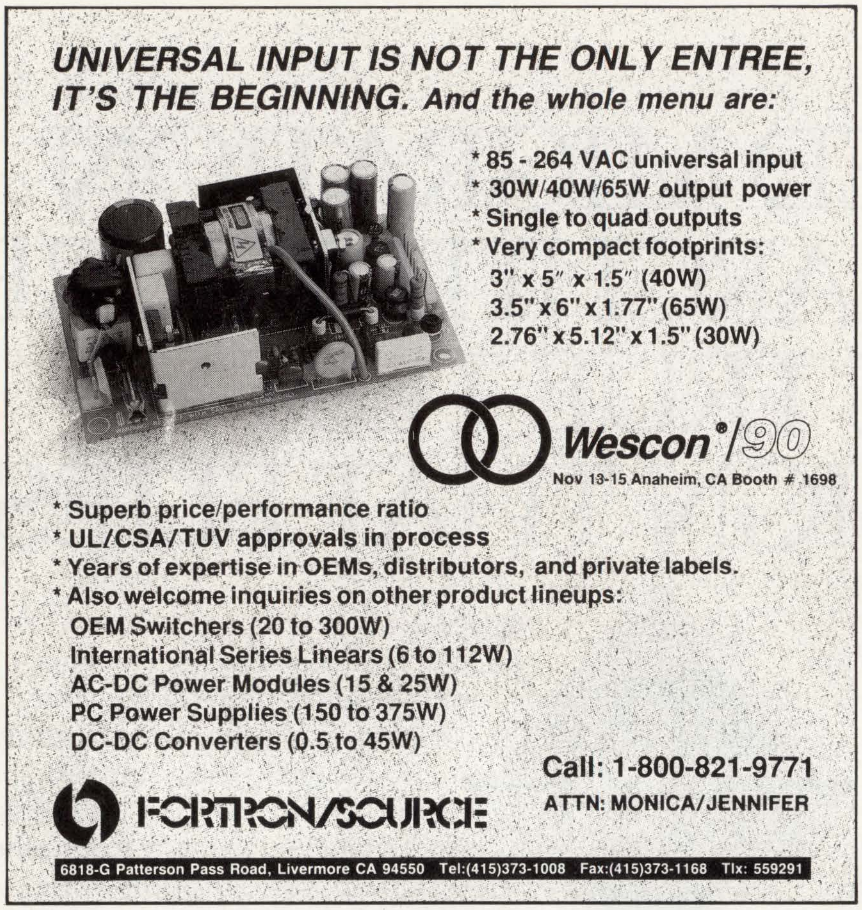

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Editorial Offices: (201) 393-6272

Advertising Production: (201) 393-6093 or FAX (201) 393-0410

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Subscription Inquiries: Mary Lou Allerton (216) 696-7000

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40 MHz

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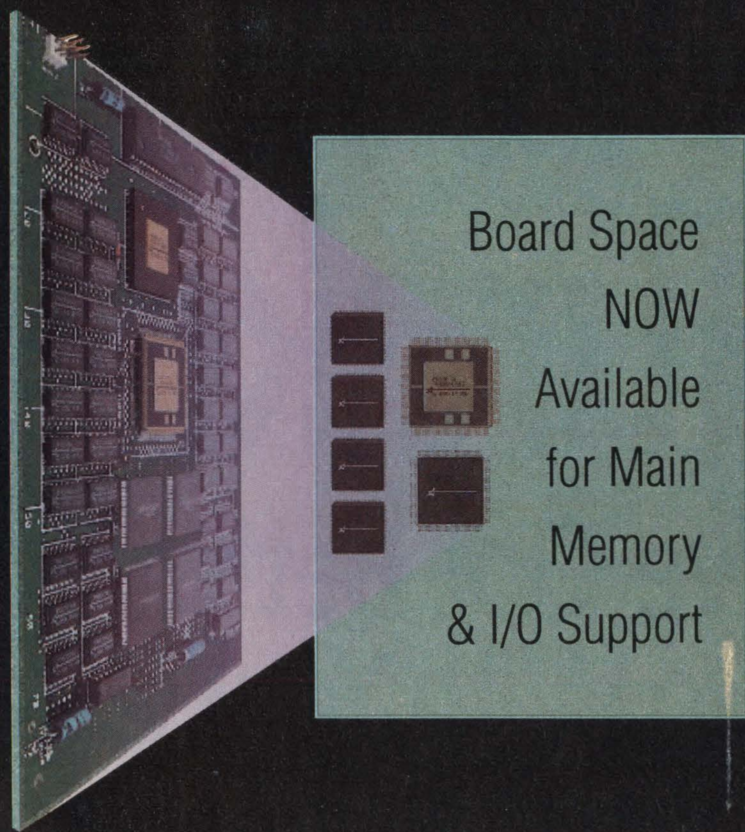

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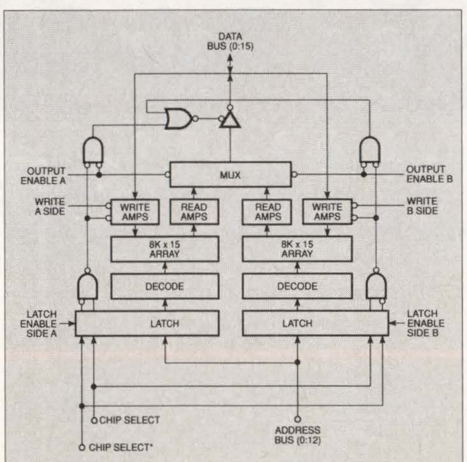

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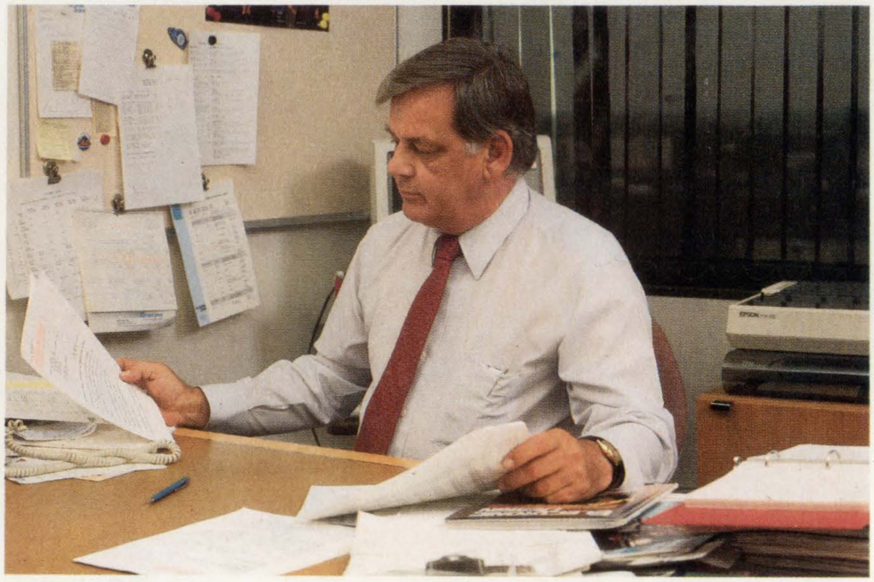


SHOWTIME

Summer once again has come and gone, and we find ourselves in the midst of autumn. But just as autumn once meant back to serious schoolwork and studies, for us it means we've come to the serious time of year for the electronics business: the industry trade show season. Buscon East was held a couple of weeks ago in Marlborough, Mass. (see the preview in our previous issue). In this issue, we preview Electronica, the giant international show held biennially in Munich (this year, from Nov. 6 to 10), and in the next issue, we'll look at both Comdex (Las Vegas, Nov. 13-17) and Wescon (Anaheim, Calif., November 13-15).

Of these, Wescon deserves some special comment this year (as well as a small commercial at the end of this piece). It's certainly the oldest of the group, and, like Electronica, it spreads its wings over the entire electronics industry (although Electronica is much larger), while the other fall shows are more specialized. As a show, Wescon certainly has seen better years in attendance and in numbers of exhibitors. In years past, it was the premier show on the West Coast. What still brings us back to Wescon year after year is the wide mix of technologies and new products that can be found each year on the exhibits floor. Plus there's the steadfast belief that the show still is important to the electronics industry as a whole. In recent years, for example, it has attracted a growing number of exhibitors offering PC-based CAE tools, as well as exhibitors from the Far East, Europe, and Canada.

Ah yes, the commercial. If you plan to attend Wescon next month, be sure to set aside some time to attend "CAE Day," an all-day track of technical sessions on CAE. The three sessions, which will be jointly sponsored by Electronic Design Automation Companies (EDAC) and Electronic Design, will kick off with a panel of experts from EDAC member companies discussing EDA directions in the 1990s. That will be followed by a session on VHDL chaired by Electronic Design CAE Editor Lisa Maliniak. The day concludes with a panel session, moderated by myself, discussing the shifting price-performance crossover point between PC-based CAE and workstations.

Stephen E. Scrupski
Editor-in-Chief

MIXED-SIGNAL SIMULATION IS PROVEN

FRANK GOODENOUGH
ANALOG & POWER

Practicality is obviously a key factor when examining all of the elements in a particular emerging technology. And, when writing a report, such as the one in this issue on mixed-signal CAE *(see "Mixed-Signal Simulators Abound," p. 43)*, it's my aim to bring you up to date on a technology that's either practical now or soon will be. However, it's easy to succumb to the spell of a technology that has promise, yet isn't totally practical. After many false starts, mixed-signal simulation might appear to be dangerously close to this category. But, stemming from the events at the recent Bipolar Circuits and Technology Meeting (BCTM) in Minneapolis, it seems that mixed-signal simulation has arrived as a bona fide, practical design tool.

At the BCTM evening panel session, six teams, employing tools from eight CAE companies, proved hands-down that a 12-bit successive-approximation IC analog-to-digital converter (ADC) could be simulated successfully beyond the transistor level. Moreover, the simulation techniques that were demonstrated included finding and fixing serious bugs.

The six teams (and their tools) were Analogy with Saber, Cadence with Analog Artist-Verilog, EES/Mentor with Precise-LSIM, Intergraph with ISIM-se, Meta-Software/Mentor with HSpice-LSIM, and Viewlogic/Microsim with PSpice-Viewsim. Four of the six employed Sparc workstations; Intergraph engineers used their Clipper-based Interpro and Meta-Software employed the Apollo DN4500. Meta-Software also made a few runs with the DN4500 for LSIM, while a more powerful Apollo DN10000 handled HSpice.

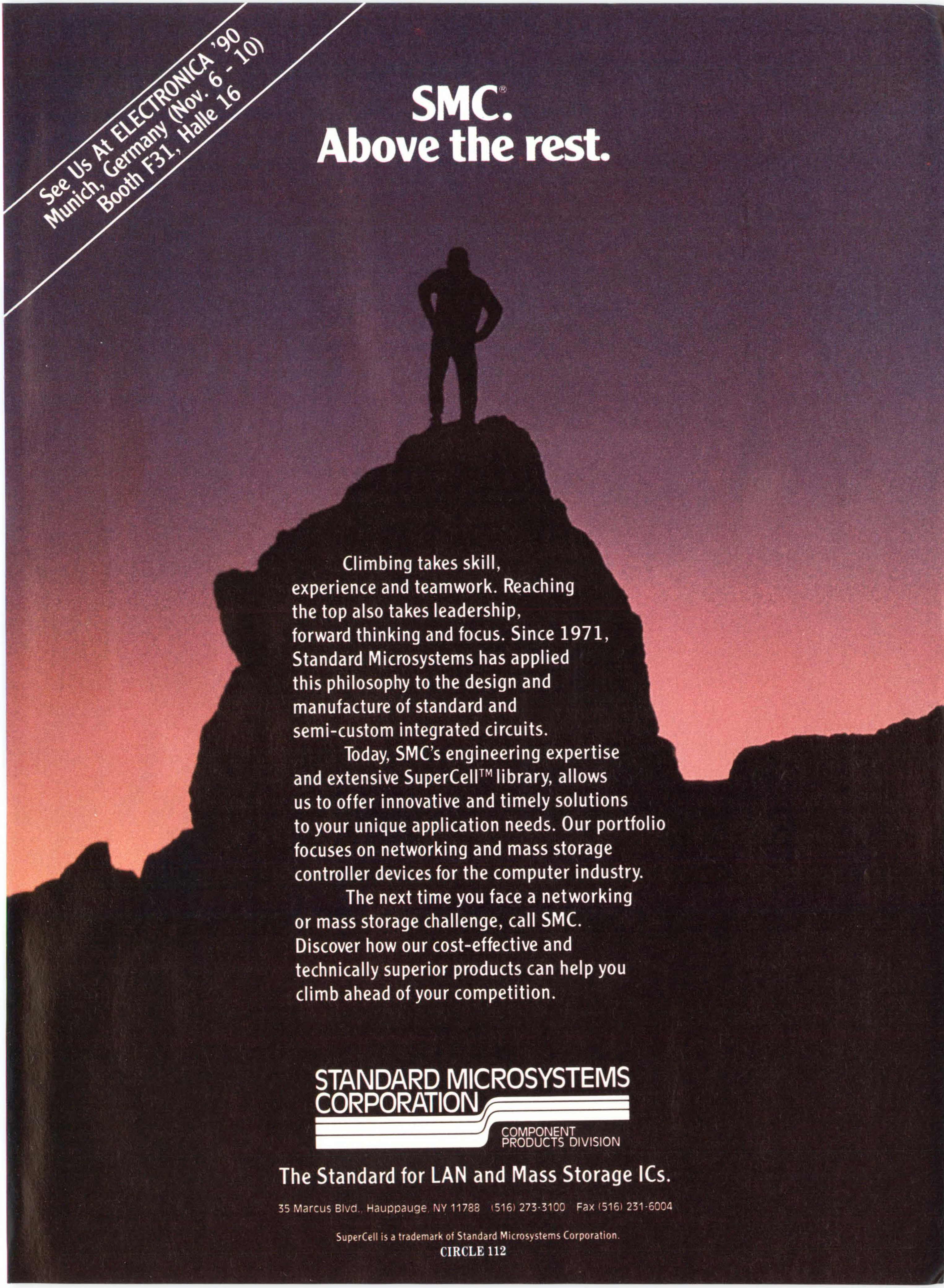
Before the meeting, session moderator John Shier of VTC, Bloomington, Minn., gave the teams transistor-level schematics of the ADC and Spice models of its transistors *(for an earlier article on these tests, see* ELECTRONIC DESIGN, *July 26, p. 16; for more information, call VTC's Jan Jopke at (612) 934-5082)*. Results from all of the teams were consistent. According to Shier, ADC conversion times were expected to run between 100 and 250 ns, and the results ran from 90 to 260 ns. Simulation times, depending on the platform and the level of modeling, ranged from less than a minute to about two hours.

What came through loud and clear is that all of these mixed-signal tools are hierarchical, making possible top-down and bottom-up design. A mix of both approaches was used by each team. However, all of the teams made it mandatory that individual behavioral circuit-blocks, whether analog or digital, must be simulated at the primitive (transistor-resistor-capacitor) level at some time prior to, or during, the design process.

The bottom-up approach, for example, was used by Intergraph. They captured the primitive schematic and simulated the individual blocks. Then behavioral models were developed—particularly for the successive approximation register (SAR)—simulated, and the results of the simulations compared.

Analogy started at the top, capturing the block diagram of the ADC in their behavioral language, and simulating to prove functionality. Then each block was broken down in more and more detail until the primitive level was reached. Simulation time ran 20 seconds pure-behavioral, 75 minutes pure-primitive (510 transistors), and 2 minutes in a hybrid mode with 50 transistors. In the hybrid simulation, the DAC's switches were a mix of primitive and a digital-switch model, and the SAR, D-latch, and clocks were pure digital behavioral-models. Indicative of compute power, the pure-primitive HSpice-LSim that ran on the two Apollos took less than two minutes.

For some designs, these tools may never replace breadboards or transistor-level simulations. However, the tools' ability to quickly simulate complex mixed-signal circuits, hundreds or even thousands of times, enables you to optimize such circuits and play "what if" games early on.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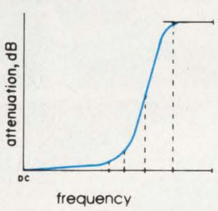

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PLP-50	DC-48	55	70	90	200	1.7	18	11.45
PLP-70	DC-60	67	90	117	300	1.7	18	11.45
PLP-100	DC-98	108	146	189	400	1.7	18	11.45
PLP-150	DC-140	155	210	300	600	1.7	18	11.45
PLP-200	DC-190	210	290	390	800	1.7	18	11.45
PLP-250	DC-225	250	320	400	1200	1.7	18	11.45
PLP-300	DC-270	297	410	550	1200	1.7	18	11.45
PLP-450	DC-400	440	580	750	1800	1.7	18	11.45
PLP-550	DC-520	570	750	920	2000	1.7	18	11.45
PLP-600	DC-580	640	840	1120	2000	1.7	18	11.45
PLP-750	DC-700	770	1000	1300	2000	1.7	18	11.45
PLP-800	DC-720	800	1080	1400	2000	1.7	18	11.45
PLP-850	DC-780	850	1100	1400	2000	1.7	18	11.45
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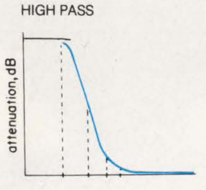

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PHP-300	290	1200	245	190	145	1.7	17	14.95
PHP-400	395	1600	360	290	210	1.7	17	14.95
PHP-500	500	1600	454	365	280	1.9	17	14.95
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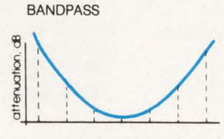

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PIF-30	30	25	35	7	120	1.9	210	DC-330	14.95
PIF-40	42	35	49	10	168	2.6	300	DC-400	14.95
PIF-50	50	41	58	11.5	200	3.1	350	DC-440	14.95
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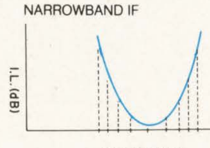

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PBP-21.4	21.4	19.2-23.6	15.5	29	3.0	80-1000	1.7	18.95
PBP-30	30.0	27.0-33.0	22	40	3.2	99-1000	1.7	18.95
PBP-60	60.0	55.0-67.0	44	79	4.6	190-1000	1.7	18.95
PBP-70	70.0	63.0-77.0	51	94	6	193-1000	1.7	18.95

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CIRCLE 123

F132-2 REV. ORIG.

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The UNIX based DECstation™ 5000 Workstation digital™

leads by example.

Example #1: Performance

No matter how you measure it, Digital's DECstation 5000 workstation leads all others in performance. Whether it's raw CPU performance, 2D or 3D graphics speed, or price/performance, the DECstation 5000 workstation comes out ahead. In fact, for overall performance, nothing else is close. And we've got the numbers to prove it.

PERFORMANCE COMPARISON CHART (1)	SUN SPARCstation 1+	IBM 320/520	DECstation 5000 cx
Graphics & Windowing (2)	0.24	0.71	1.59
Integer	1.04 (3)	1.34	1.61
Floating Point	1.10 (3)	2.6	1.7
Overall Performance	0.65	1.35	1.63

(1) All data normalized to DECstation 3100. Comparable configurations tested. Geometric mean used to combine results. Performance will vary depending on applications and environment. (2) Graphics and windowing data measured using X11perf benchmark. CPU Integer and Floating Point performance measured from running SPEC V1.0 workload. (3) SPEC performance estimate based on SUN 4/330 results published by Sun Microsystems, Inc.

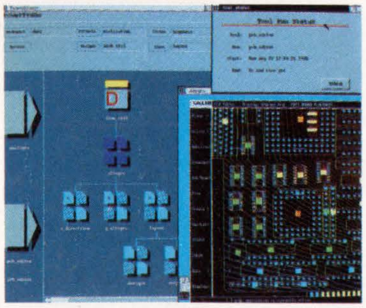
Example #2: UNIX based Applications

When you run with the leader, you know you're in good company. The DECstation 5000 workstation runs more than 1,500 UNIX based applications, including the industry's most popular MCAD and EDA applications.

Example #3: PowerFrame™ for Design Integration.

With Digital's PowerFrame design framework, you can easily integrate the DECstation 5000 workstation with your existing UNIX based EDA and MCAD systems. PowerFrame is the most widely used framework for heterogeneous design management.

And, of course, as the leader in integrated multi-vendor networked computing, you can count on Digital for full service and support. We can help you design, implement and maintain an engineering computing strategy that capitalizes on today's technology, while keeping your options open for the future.



For your copy of benchmark test results and a list of available applications, call 1-800-343-4040, ext. 970. These are filled with examples of what you expect from a leader.

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- 10,000 V/µs Slew Rate
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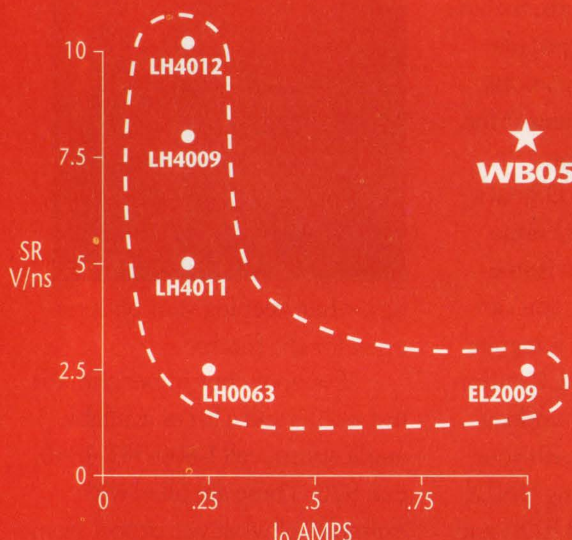
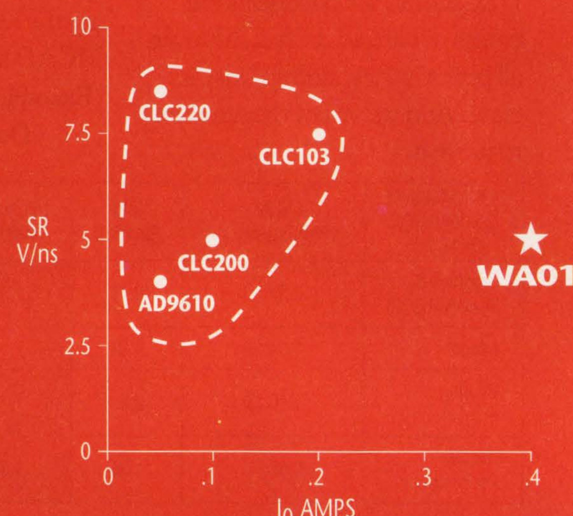
- Up To 10 Watts Dissipation





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CIRCLE 142

TI CASE Tools Aim At Multiple Platforms

As the software backlog grows, so does the demand for computer-aided software engineering (CASE) tools. To tap this rich vein—estimated to hit $8 billion by 1995—Texas Instruments Inc., Dallas, is making its CASE software run under Digital Equipment Corp.'s VMS operating system, TI1500 Unix, and Fujitsu Unix, starting early next year. Later in 1991, developers will be able to write for the Tandem Computers Inc. NonStop environment. With TI's case tools, which the company calls the Information Engineering Facility (IEF), applications can be written for many platforms from the same specification. A developer chooses from a menu of languages, operating systems, and database management systems. Then the IEF's construction tools generate the appropriate source code, data structures, and screens. *SVT*

Emulate LaserJet In Hardware And Software

The first complete hardware and software emulation of HP's LaserJet III/ PCL 5 is now available. Printer-control language (PCL) 5, an extension of PCL 4, is the newest page-description language (PDL) that controls the functions of the LaserJet III. Previously, OEMs could get either the hardware or software emulations from a supplier. Now they can get LaserAct 5 from Destiny Technology Corp., Milpitas, Calif. It's a complete solution that incorporates all of the LaserJet III functionality and adds such features as PostScript capability and on-the-fly scaling of resident or downloadable fonts from 0.25- to 999.75-point size. Its powerful image modeling can accomplish overlay-image combinations in transparent or opaque modes to create special effects, such as shadows and reverse-image printing. Destiny has also come up with a software architecture for the language. The architecture breaks the language down into four modules, each supplying a relationship to a different area: orientation, image modeling, coordinate translation, and network interfacing. Destiny will supply the software as well as the ASICs to OEMs. *RN*

Small Disk Drives Pack Intelligent Cache

By simultaneously developing a disk-drive controller chip set and the drive itself, a pair of 2.5-in.-diameter drives offer designers formatted capacities of 31.5 or 62.9 Mbytes. From Western Digital Corp., Irvine, Calif., the AT-compatible drives include an intelligent caching scheme called CacheFlow. The scheme improves system performance by using a multisegmented adaptive cache algorithm that evaluates the way data is requested by the system, and then adapts automatically to the optimum caching mode (such as sequential or repetitive). The drives offer six modes for power management—read-write, seek, idle, standby, sleep, and shut-down. They work with the company's WD7600LP motherboard logic chip set, which is optimized for low-power laptop, notebook computers. The drives are also the lowest-weight units yet released. The WDAB130, with its 31.5 Mbytes of storage and 19-ms access time, weighs in at just 144 grams and is just 0.6-in. high. The WDAH260 packs double the storage, has the same access time, and weighs in at 160 grams due to its second platter. The extra platter also increases the drive's height to 0.75 in. Evaluation units sell for $325 and $495, respectively. Contact Bob Blair at (714) 932-7834. *DB*

Technology Centers Ease Design Access

Following the path of several other companies in an effort to offer customers easier access to ASIC, SCSI, and PC design expertise, NCR Corp., Dayton, Ohio, is assembling a worldwide network of Regional Technology Centers. The RTCs will be set up at strategic locations around the U.S., as well as in other parts of the world. The centers will provide extensive technical support, and will offer design resources for NCR customers developing application-specific ICs as well as other products, such as SCSI-based host adapters. The first center is based in San Jose, Calif., and includes private work areas with Apollo, Sun, and 486-based workstations. The workstations run software from Mentor, Cadence, and Viewlogic for customers that don't have their own in-house design capability. Also available will be various logic analyzers, scopes, and PC platforms for easier software and hardware debugging. Five additional centers are slated to open before the end of 1990. They'll be located in Orange County, Calif; Boston, Mass.; Dallas, Texas; Munich, Germany; and Taipei, Taiwan. Each RTC will be linked to all of NCR's other facilities through a wide-area computer network. *DB*

DUAL 18-BIT 96-KHZ ADC RUNS OFF 5-V RAIL

Hailing from a newcomer to the ADC field, a novel dual IC meant for digital-audio applications may fill the need for 12-to-18-bit sampling ADCs. The AT76C120, from Atmel, San Jose, Calif., is the first of the genre to run off a single 5-V supply, and it costs just $25 each in 1000s. If two converters are required, the cost drops to $12.50 each for an ADC that offers a typical signal-to-noise ratio of 90 dB (approximately 15 bits) while sampling at 96 kHz. Moreover, a reference isn't required (it's on-chip), and both ADCs on the chip sample simultaneously. Differential linearity is ±1 LSB at 18 bits (no-missing-code performance). Atmel brings their expertise in EEPROMs to the AT76C120. The chip contains two successive-approximation ADCs. Each combines binary-weighted polysilicon-oxide-polysilicon capacitor arrays for the MSBs, with polysilicon resistor strings forming the LSBs. The switched-capacitor arrays provide the inherent sampling needed to capture signals to 44 kHz. At the completion of each conversion, a digital correction for tap-weight errors (in the capacitor arrays) modifies the two serial output words. The correction factor is determined during factory testing and stored in the on-chip EEPROM. Call Jeff Katz, (408) 441-0311. *FG* **CIRCLE 349**

NEWWAVE GROWS WITH INTEGRATOR, E-MAIL, FAX

With the arrival of three new software products, Hewlett-Packard Corp.'s (Palo Alto, Calif.) suite of NewWave tools now numbers twenty. One product, called AdvanceLink, enables PC users to integrate minicomputer-based applications with a workstation. The tool automates repetitive tasks, such as logging onto the host or transferring data, by creating a command file that's invoked with a simple sequence of keystrokes or by using a mouse. AdvanceLink also supports Microsoft's DDE (dynamic data exchange) protocol, making it possible for further integration with other PC applications. And it supplies emulation of HP 2392 and 700/94 terminals, allowing users to access applications running on HP 3000 or 9000 systems in line or block mode. AdvanceLink should be available by year's end for $299. The second product is NewWave Mail, an electronic-mail tool that lets users send messages, video objects, and other data types to other users. It's available now for $195. Finally, with OfficeFax, NewWave Mail users can send other users facsimile messages directly from their computers. It costs $6000 and is also available now. For more information, contact HP's customer information center at (800) 752-0900. *RN* **CIRCLE 350**

DIGITAL I/O CARD CUTS COST, RAISES RELIABILITY

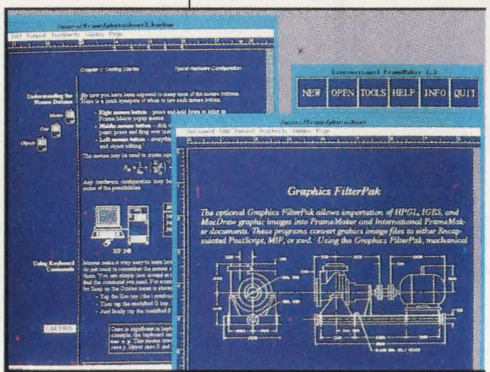
Using a PC/AT interface card designed around a proprietary ASIC, users can get reduced cost per I/O and improved reliability. The ZT 14CT72 from Ziatech Corp., San Luis Obispo, Calif., consolidates 192 points of bidirectional digital I/O on one card and connects AT-type systems to high-current peripheral devices. The card can drive high-current peripherals, such as industrial I/O modules, with the help of the 16C48 48-point ASIC. In addition, it supplies a current sink of 12 mA. Each of the 14CT72's digital I/O lines can be programmed individually as an input or an output, adding configuration flexibility for industrial applications. The digital I/O card also features open-collector outputs that don't glitch at power-up and power-down. Therefore, external devices aren't inadvertently triggered. The board, which takes up only one slot in the backplane, costs $5450 and comes with the device-driver software. Large-volume discounts are available. For more information, call Phil Nash at (805) 541-0488. *RN* **CIRCLE 351**

UNDERVOLTAGE SENSORS RESET MICROPROCESSORS

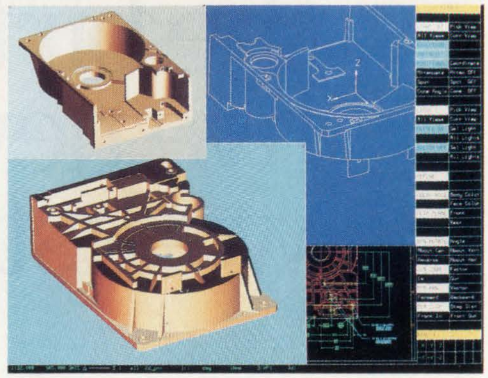
The MC34164-3 and MC33164-5 from Motorola, Phoenix, Ariz., can monitor the supply rails of 3- and 5-V microprocessors, respectively, and apply a reset pulse at power-on. Such a pulse is mandatory in MC68HC11-family microcontrollers and beneficial in many others. When the 3-V rail rises between 2.55 and 2.8 V, the MC34164-3's output goes high; when the rail drops to that window, the output goes low. A minimum of 30 mV of hysteresis is supplied to prevent erratic operation. The 5-V rail monitor's window is between 4.15 and 4.45 V, and the hysteresis is a minimum of 20 mV. Quiescent current of these chips is just 15 μA from a 3-V rail, and 20 μA from a 5-V rail. As a result, they lend themselves to battery-powered applications from automotive to medical to PCs. The MC34164-3 and MC33164-5 are for commercial-temperature-range operation; two siblings will handle industrial temperatures. All four come in plastic 3-pin TO-226AA (modified TO-92) and SO-8 packages. Pricing in quantities of 10,000 ranges from $0.43 to $0.55 each. (602) 897-3615. *FG* **CIRCLE 352**

HP and Apollo proudly announce the birth of five new workstations.

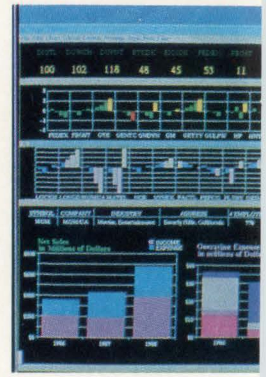
As you'd expect, compatibility runs in



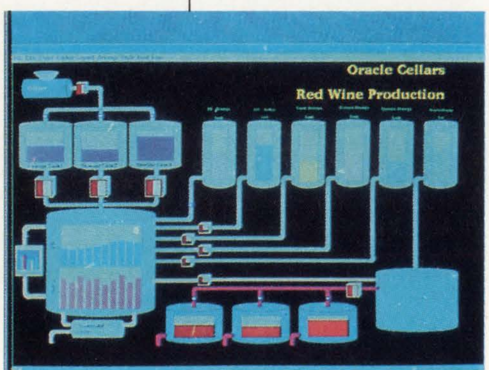
Documentation



Solid modeling for mechanical engineering



Graphic informa



Graphic information system

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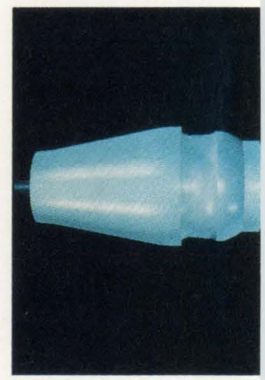
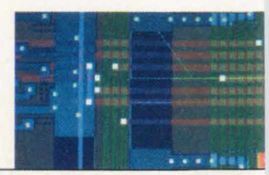


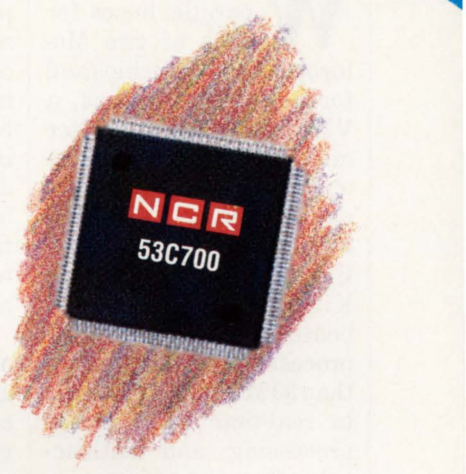
Mechanical computer-



The HP Apollo 9000 Series 400.

New Product Announcement!

Here's another.



The NCR 53C700 SCSI I/O Processor… So good, *Electronic Design* named it the product of the year.

"You can't tell a good SCSI chip just by looking at it…" and according to Electronic Design, NCR's 53C700 is the best there is.

The only third generation SCSI device on the market today, it concentrates all the functions of an intelligent SCSI adapter board on a single, smart and extremely fast, chip… for about 15% of the cost.

As the first SCSI I/O processor on a chip, the 53C700 allows your CPU to work at maximum speed while initiating I/O operations up to thousands of times faster than any non-intelligent host adapter. DMA controllers can burst data at speeds of up to 50 Mbytes/s. This new chip cuts down system time hookup to a fraction of what it has been.

Those are just a few of the reasons Electronic Design's "Best of the Digital IC's" award went to NCR's 53C700 last year.

And now the NCR 53C710!

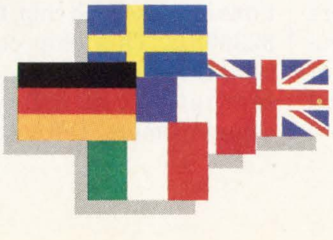
For the complete story on the NCR SCSI product line featuring the new 53C710, as well as the upcoming SCSI seminars with the NCR SCSI Development Team, please call:

1-800-334-5454

NCR

Creating value

CIRCLE 157



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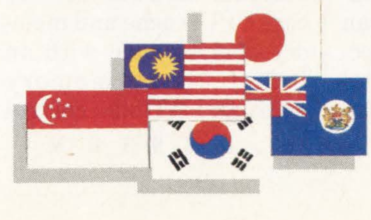

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32-Bit VMEbus Board With Two DSP ICs Delivers 30 MFLOPS

With a pair of 32-bit parallel buses for each of two Motorola DSP-96002 chips and for a shared VMEbus, a VMEbus board can offer multiprocessor systems more flexibility and processing power. Developed by Data β Ltd., Theale, Berkshire, the United Kingdom, the DBV96 board delivers sustained processing power of more than 30 MFLOPS, suiting it to real-time DSP, array-processing, and math-acceleration applications in standard workstations and other systems. Up to eight boards can be connected in various topologies, including rings and cubes, with each board accessing up to 20 Mbytes/s.

Each DSP96002 has access to two expansion ports on nonshared parallel data buses, to common memory, and to the VMEbus for optimum configuration *(see the figure)*. Robert Shaddock, Data β's director, explains "In a radar or sonar application, a parallel connection might be the most efficient, while for graphics image processing, the boards would be connected in series as a pipeline." Because they operate independently, the two DSP96002s can be interconnected in series to form a single-board linear multiprocessor suitable for complex-number arithmetic.

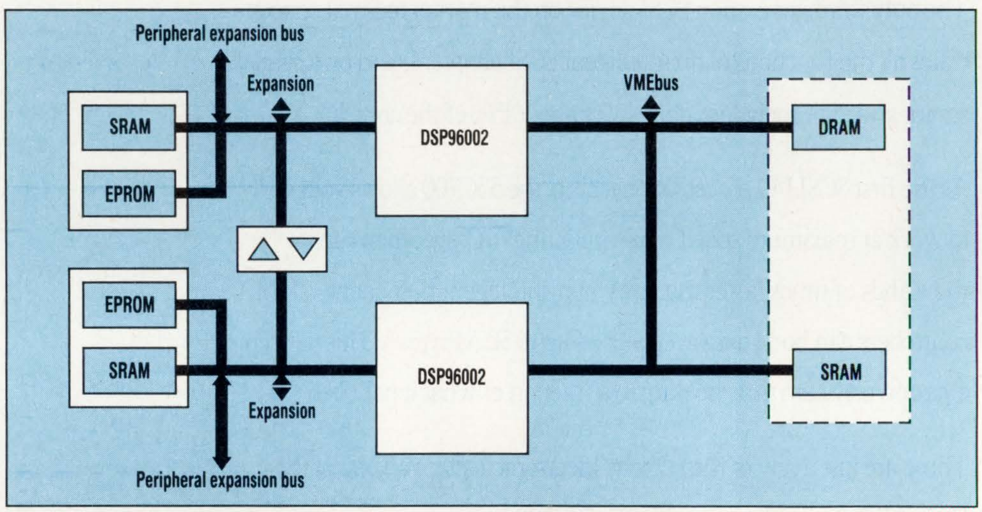
One expansion port, a 24-bit peripheral bus, provides an interface to data-acquisition systems. It can be used for direct connection with analog-to-digital converter systems or video boards. The other port supplies a high-speed 32-bit multimaster data and address facility to interconnect with other DBV96 boards. It's also used as an interface with a series of daughter modules that can be coupled to the user-defined pins on the DSP96002 to create interfaces with non-VMEbus bus systems.

Each processor has its own 256-kword fast SRAM array, accessed by a dedicated 32-bit bus, for programming or scratchpad use. Each also contains its own bootstrap EPROM for firmware and data libraries. Both processors have access to a 4-Mword shared-memory array that combines static and dynamic RAM. Up to 16 Mbytes of common memory on the board are multiported between the two processors and the VMEbus. With access to the VMEbus, memory can be shared with processors on other boards in a system. As a result, each processor can address a full 4-Gbyte memory and the whole 32-bit memory space of the VMEbus as a master.

An assortment of software and development tools are available from Data β. Cost of the board depends on configuration, ranging in price from £5,000 to £12,000. The DBV-96 will be marketed in Europe by Data Cell Ltd. In the U.S., it will be marketed by Areal Inc., Highland Park, N.J. Prices in the U.S. have yet to be set.

For more information, contact Data β Ltd., Unit 7, Chiltern Enterprise Centre, Theale, Berks RG7 4AA, United Kingdom, Telephone +44 (0)734 303631; or Data Cell Ltd., 10 West End Rd., Mortimer Common, Reading, Berks RG7 3SY, United Kingdom.

PETER FLETCHER

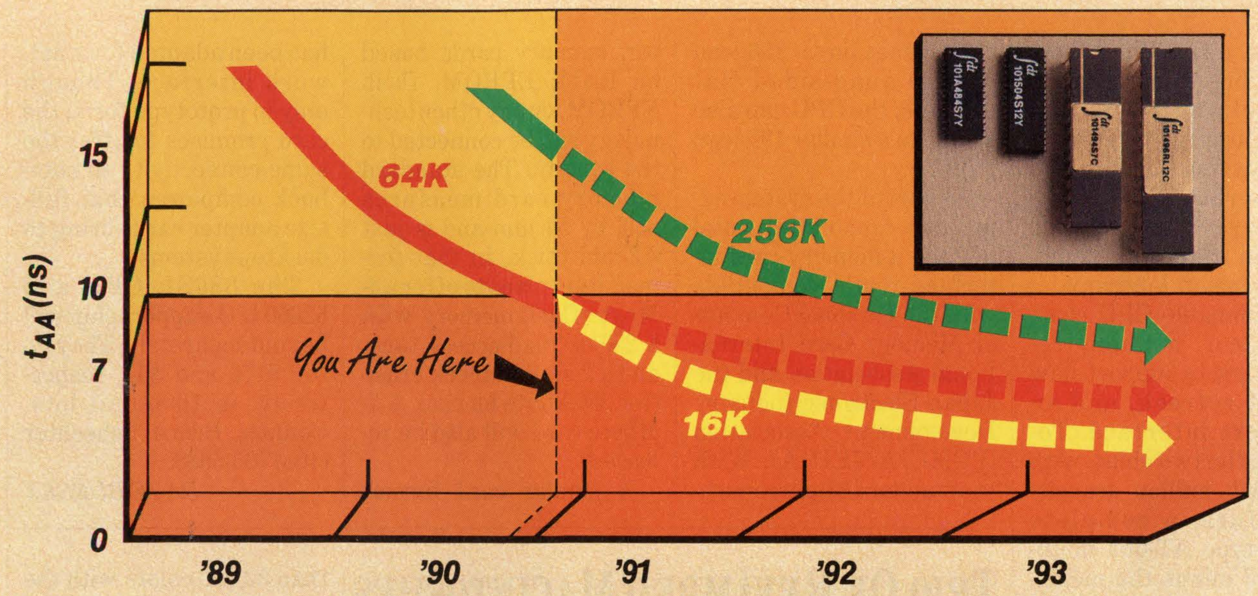


Integrated 80386SL Simplifies Laptop Systems, Trims Power Demands

Fulfilling their promise to merge the CPU chip with the basic support circuitry on a PC's motherboard, Intel Corp., Santa Clara, Calif., created a high-integration version of the 80386SX. The 80386SL includes the 386 core CPU, cache and memory control logic with an LIM EMS 4.0 memory manager, AT-bus control circuits, a high-speed peripheral interface bus (with twice the standard AT speed), and flexible power-management capabilities. With special programmable features for cache and other memory on the chip, system designers can create various configurations. Thus a range of system performance and price points is possible.

Unlike the recently unveiled 286ZX from Advanced Micro Devices Inc., Austin, Texas, which includes many of the PC/AT motherboard functions, Intel decided to put all of the I/O and control functions into a second chip, the 82360SL. This chip contains the programmable interrupt controllers, counter-timers, DMA con-

Break Through 7ns



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Design tomorrow's fastest systems today. Our IDT10484 (4K × 4) will be the fastest high-density BiCMOS memory to run primary caches in ECL systems. At 7ns, the IDT10494 (16K × 4) is the fastest BiCEMOS 64K ECL SRAM available in volume production today.

In addition, we offer the densest BiCEMOS ECL RAM, the IDT10504 (64K × 4), at 12ns. And our new 12ns IDT10496RL (16K × 4) synchronous self-timed SRAM (STRAM) offers registered inputs, latched outputs, and self-timed write for easier system design.

Each of our ECL SRAMs is available today in 10K, 100K, and 101K configurations in 300mil SOJ and 400mil Sidebraze DIP packages.

Technology for the '90s

We engineered BiCEMOS technology to offer the best of both worlds: the low power consumption of CMOS with the high speed of bipolar technology.

Count on our BiCEMOS ECL to take you through the 7ns speed barrier for 64K densities. We believe our BiCEMOS ECL will achieve speed increases of 20% a year every year for the next five years, making BiCEMOS the technology for the '90s.

Samples Available

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Integrated Device Technology

BiCEMOS ECL SRAM Family

Part No.	Description	Max. Speed (ns)	Typ. Power (mW)
IDT10484	16K (4K × 4) 10K ECL	7	700
IDT100484	16K (4K × 4) 100K ECL	7	500
IDT101484	16K (4K × 4) 101K ECL	7	700
IDT10490	64K (64K × 1) 10K ECL	8	420
IDT100490	64K (64K × 1) 100K ECL	8	320
IDT101490	64K (64K × 1) 101K ECL	8	420
IDT10494	64K (16K × 4) 10K ECL	7	700
IDT100494	64K (16K × 4) 100K ECL	7	500
IDT101494	64K (16K × 4) 101K ECL	7	700
IDT10496RL	64K (16K × 4) 10K STRAM	12	1000
IDT100496RL	64K (16K × 4) 100K STRAM	12	800
IDT101496RL	64K (16K × 4) 101K STRAM	12	1000
IDT10504	256K (64K × 4) 10K ECL	12	800
IDT100504	256K (64K × 4) 100K ECL	12	600
IDT101504	256K (64K × 4) 101K ECL	12	800

CIRCLE 134

trollers, a real-time clock, 24-mA bus drivers, and a parallel and serial I/O port. Various power-management functions are also incorporated. These include event recognizers that can trigger a system-management interrupt, a programmable CPU clock generator, memory refresh logic to support slow DRAM refresh, and an IdeaPort interface. Together, the two chips, with their 1.1 million transistors, form a complete 386SX-type AT-bus motherboard minus the memory, math coprocessor, and such major peripheral controllers as keyboard, video, and mass-storage control.

The first version of the chip set is optimized for portable applications, such as notebook computers. It consumes much less power than other integrated solutions: Intel estimates that systems based on the SL chip set may double their battery life. To keep power low, a new interrupt scheme was created. The scheme is based on what Intel designers defined as a system management interrupt (SMI), which allows the system to perform many power-management tasks. Those tasks include suspend or resume operation, put peripherals into standby, control the CPU speed, and allow uninterruptible power-supply changeovers. There's also various other extensions users can define.

To minimize the CPU chip space in portable environments, the IC will be housed in a 227-pad land-grid-array package. The package can be surface mounted and has no leads that can be damaged. The companion system support chip comes in a 196-lead plastic quad-sided flat package; the CPU can also be had in a similar 196-lead PQFP.

As part of the system expansion capabilities, Intel defined a memory-card interface that's compatible with the Personal Computer Memory Card International Association and the Japan Electronic Industry Development Association (PCMCIA/JEIDA). With the standard 68-pin connector, memory cards based on RAM, EPROM, flash EPROM, or any other technology can be connected to the system. The standard memory card measures 85.6 by 54 mm and is just 3.3-mm thick. In that format, Intel plans to offer a 4-Mbyte flash memory with a 250-ns read-access time, and a 2-second block erase (for 256-kbyte blocks). A 1-Mbyte card will also be released.

A similar card format has been adapted for a network interface. Though only in prototype form, the card promises to offer the same connectivity to notebook computers that full-size adapter cards bring to desktop systems.

The 386SL CPU and 82360 I/O support chip will be sold separately. They go for $176 and $45, respectively, in 1000-unit lots. Contact Bruce Schechter (408) 765-5688.

DAVE BURSKY

TRIO OF REVAMPED MACINTOSHES TRIM COSTS, OFFER NEW OPTIONS

With the arrival of three recently unveiled Macintosh computers, sporting more feature-laden motherboards and sleeker cabinets, the minimum cost of the all-in-one original Macintosh as well as the modular Macintosh II family has been reduced. And designers at Apple Computer Inc., Cupertino, Calif., brought the prices down while improving performance.

The lowest-cost system is the sub-$1000 Macintosh Classic, the only one that still retains the 9-in.-diagonal monochrome display and all-in-one cabinet (though slightly restylized). Based on an 8-MHz 68000, it delivers about 25% more performance than the Macintosh Plus. It includes 1 Mbyte of RAM (expandable to 4 Mbytes on the motherboard) and 512 kbytes of ROM to hold the basic operating system and device drivers. The system also has one SuperDrive, which can read and write to any 3.5-in. Macintosh, ProDos, or IBM-compatible DOS diskette. Moreover, the cabinet can hold a second drive internally—a 40-Mbyte hard-disk drive—which ups the price to $1499, including a second megabyte of RAM. Built-in features include AppleTalk network interfaces, an Apple Desktop Bus interface, a SCSI port for peripheral expansion, a floppy-disk expansion port, and a four-voice sound generator that drives a sound-output port.

The Macintosh LC, Apple's lowest-cost color system at $2499, has a limited-expansion modular format. Based on a 16-MHz 68020, it delivers about double the throughput of the Macintosh SE for about the same price. Support is also included for three monitor types—a new 12-in. RGB unit with 256-color, 512-by-384-pixel capability; a 12-in. monochrome monitor with 16 gray scales and 640-by-480-pixel resolution; and the already available 13-in. AppleColor 16-color monitor. An optional 512-kbyte video-RAM module enables the system to display more than 32,000 colors with the 12-in. RGB monitor.

The LC's low-profile cabinet is just 3-in. high and about 12-by-15-in. on its sides. The box has all basic features of the Classic plus a sound-input port. The port digitizes microphone input signals for voice annotation of documents and electronic mail. A 40-Mbyte hard-disk drive is standard.

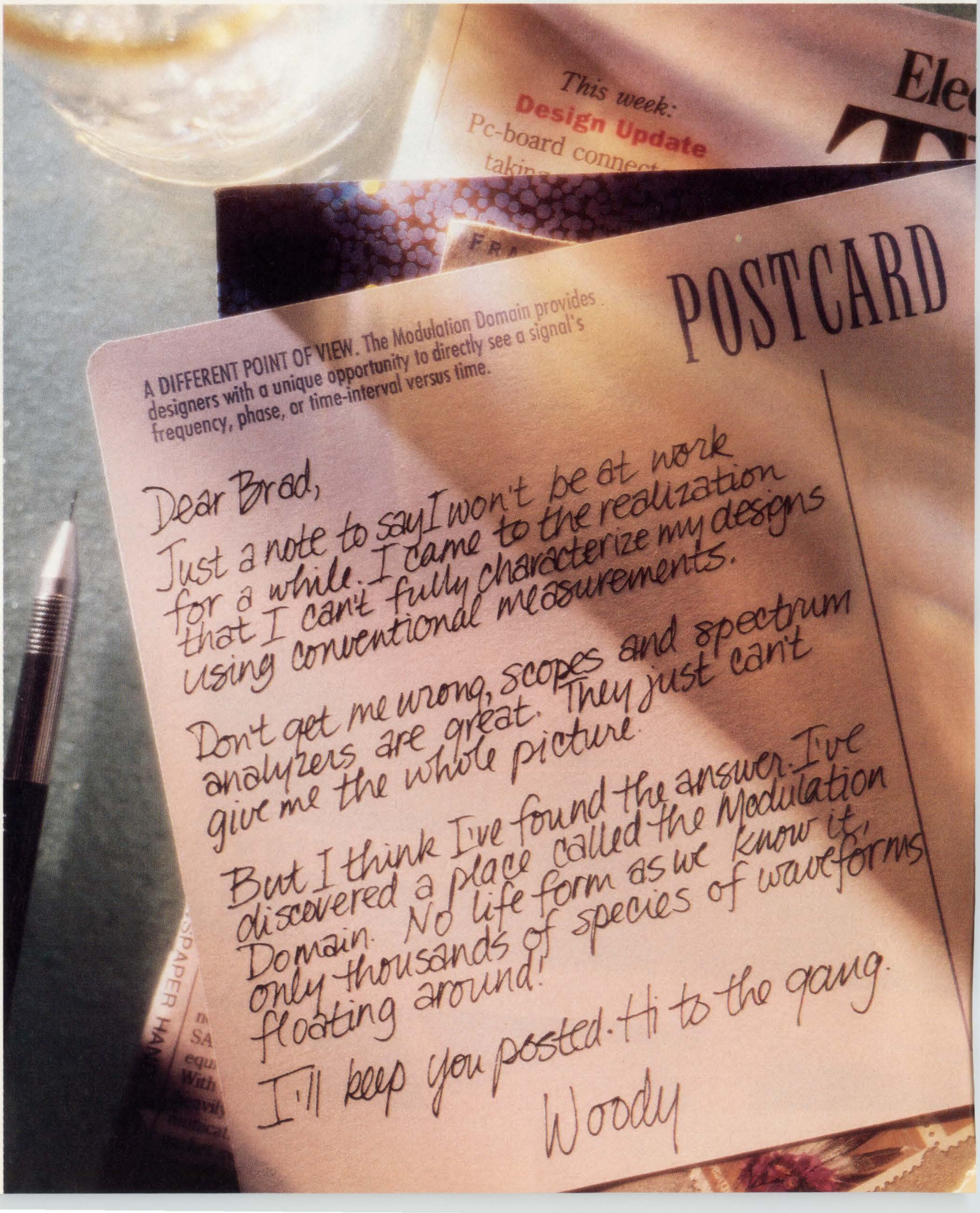
A unique LC option is an Apple IIe add-in card that allows most, if not all, of the thousands of IIe software packages to run on the Macintosh screen.

The IIsi swings in on the low end of the modular Mac II family, with its 4-in. high by 12.4-by-14.9-in. cabinet. It sets a new low-cost option—$3769. Its single expansion slot can be configured as a NuBus-compatible slot or as a processor-direct slot via an adapter card. Based on a 20-MHz 68030, it's about five times faster than the Macintosh SE. The IIsi comes standard with 2 Mbytes of RAM, a 40-Mbyte hard-disk drive, one SuperDrive, and all the I/O ports of the LC. A new release of Apple's A/UX Unix will be ready for the IIsi later this year.

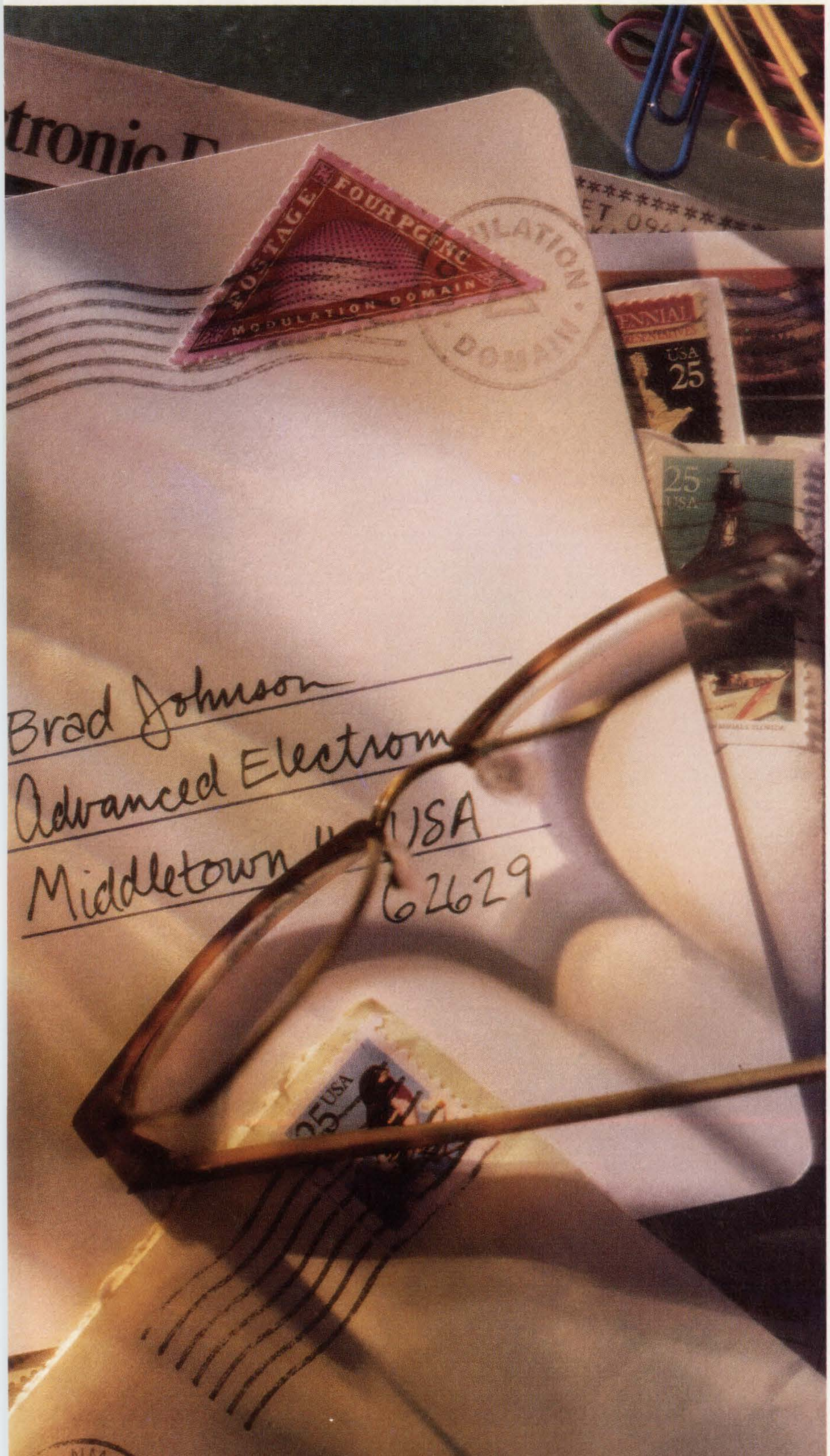
DAVE BURSKY

Like you, Woody Newman will go to any length to become a better designer. This time he went into another dimension.

Woody Newman has vanished into to get a better look at his designs.



the Modulation Domain



Recently, a design engineer named Woody Newman was working against a deadline when he found himself in a familiar predicament: To get the performance he wanted from his design, he needed a better understanding of his prototype.

Like many modern designers, Woody knew the information he needed would be revealed if he could just see the dynamic behavior of frequency agile signals, study the transient response of phase-locked loops, or understand potential sources of jitter. But conventional measurement techniques simply couldn't give him the right perspective.

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CIRCLE 119

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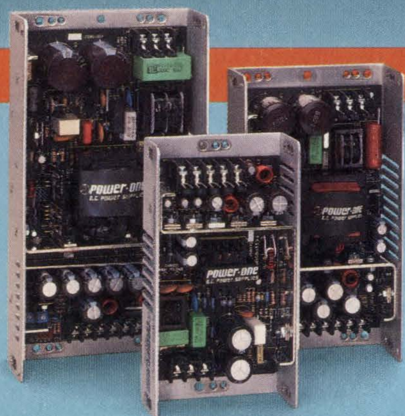

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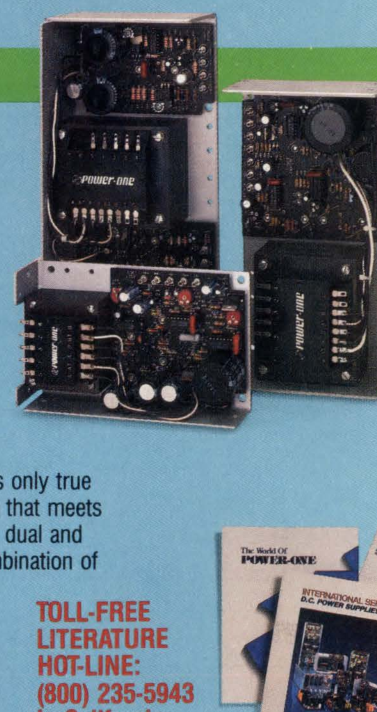

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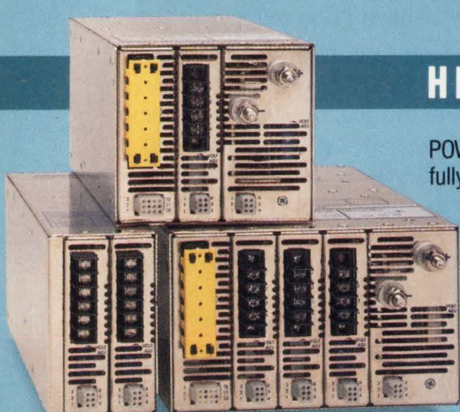

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CIRCLE 176

WITH MORE EXHIBITORS FROM ASIA, EASTERN EUROPE, AND THE U.S., THE HUGE SHOW IS TRULY INTERNATIONAL.

ELECTRONICA HIGHLIGHTS COMPONENTS, ASSEMBLIES

JOHN GOSCH AND PETER FLETCHER

If there were a hall of fame for the world's most significant electronics shows, Electronica, a biennial event in Munich, Germany, would certainly be an entrant. And if exhibitions were narrowed down to shows devoted to components and assemblies only, Electronica may well find itself at the top. That, the show's organizers say, is the view of industry and trade officials in the U.S. and Japan.

The significance of Electronica 90, to be held Nov. 6-10, lies not only in its size in terms of floor space and numbers of visitors and exhibitors, but also in its international quality and the type of exhibitors *(Fig. 1)*. The latest count shows nearly 2000 exhibitors, about 10% more than at Electronica 88. Besides their own wares, they'll display those of an additional 530 companies.

Of the 2000-plus "direct" exhibitors, around 870 will come from outside Europe, 44% of the total. They'll come from 39 different countries, both East and West. Carrying the U.S. flag will be 223 firms, representing the largest foreign contingent at the show. Second and third in line will be the United Kingdom with 125 firms and France with 85.

1. ELECTRONICA 90, an international trade fair for electronic components and assemblies, opens its doors Nov. 6 through 14. The annual event will be held at the Fairgrounds in Munich, Germany.

Some 120,000 visitors are expected—about 12% more than in 1988—to flock to the Bavarian capital to see Electronica 90 displays in 16 exhibition halls with a total floor space of 110,000 m^2, or about 1 million ft^2. Electronica will draw 30% more visitors from East European countries than in the 1988 edition, which is "a result of the political thaw between East and West," says Gerd vom Hövel, managing director of the Munich Trade Fair Corp., Electronica's host.

A key element of the show is it's specialization. Electronica officials keep a close watch on what firms plan to exhibit. Anything that's not components-oriented or related to electronic subassemblies is barred from the show. This ensures that only the specialists attend the fair, that is, those who are potential buyers of the products displayed, vom Hövel says.

The Microelectronics Congress, which ran concurrently with the exhibition, will no longer be held. Show organizers felt that what was presented at the congress was often too remote from the practitioner and diverted attention from the displays. Compensating for the absence of the congress will be a number of seminars and conferences relating to components and their markets.

Of note will be a half-day conference on Nov. 6, at which Raimondo Paletto, chairman of the management board of the Joint European Submicron Silicon Initiative (Jessi) will discuss Jessi's status, direction, and goals for the next five years. Jessi aims to develop equipment, materials, and technologies needed to produce, for instance, engineering samples of 0.5-μm ICs by mid-1991, first silicon of 0.3-μm parts by mid-1993, and engineering samples of such parts by mid-1994. The 0.3-μm samples will be in pilot production by the end of 1995.

A number of seminars will be conducted at the show. They range from microsystem technology, test-cost optimization, and power electronics to producers' liability, quality assurance, microelectronic sensors, and connector miniaturization.

Much attention will focus on memories, demonstrating how Europe ranks in the field. Germany's Siemens AG will present samples of 16-Mbit DRAMs. The 0.6-μm CMOS IC integrates more than 33 million elements on a 142-mm^2 chip.

The Siemens memory, the result of a two-year development effort that drew heavily on the Siemens/Philips high-density-memory Mega project, is now being transferred into pilot production. Full production will start in 1992, when Siemens believes it will have pulled even with Japanese memory producers.

SGS-Thomson Microelectronics (STM), the Italian-French semiconductor maker, will present the latest additions to the company's EEPROM family. A minimum of one million write/erase cycles are possible. Such performance is an order-of-magnitude improvement over previous-generation EEPROMs.

The ST93C46A and ST93CS56 are 1- and 2-kbit EEPROMs built with a special process STM calls CMOS F3. This is a single-metal/single-poly process derived from the firm's established 1.5-μm CMOS technology, with additional process steps adapted for implementing high-performance nonvolatile memory cells.

The 5-V ST93C46A and ST93CS56 guarantee 10-year data retention after one million erase/write cycles per word. They include built-in electrostatic-discharge protection; all inputs withstand 2 kV.

The increase from 100,000 to 1 million write/erase cycles means virtually unlimited write/erase capability in most applications. Coupled with the low CMOS power consumption and the small footprint of the 8-pin package, this makes the devices ideal for use in TV and radio tuners, telephone dialer memories, and cordless phones.

LCDs Advance

Eying the vast potential for liquid-crystal displays to move color pictures, Philips Components developed a high-resolution 6-in.-diagonal LCD that will be unveiled as preliminary samples. The active-matrix LCD works with less than 50 leads to drive more than 400,000 pixels in 756 lines and 565 columns.

The Philips LCD achieves a contrast ratio of at least 1:100 over a temperature range of –10 to +60°C. Viewing angle in the horizontal plane is 60 to 90° before the contrast falls to below a 1:10 ratio. In the vertical plane, the viewing angle is 40°. Color displays on the screen compare in quality with those attained by CRTs. The LCD has a gray scale of 256 different shades. Development work on the LCD will be finished by the end of this year. Working samples will be ready during the second half of next year and pilot production will begin in early 1992.

Also moving to center stage at this year's Electronica will be ICs for telecommunications applications. In this field, Siemens will show a single-channel high-level communications controller for local-area network, Integrated Services Digital Network (ISDN), and point-to-point high-level data-link control (HDLC) applications. The SAB82526 has won over 70 design-ins in Europe so far, and many more are expected to come.

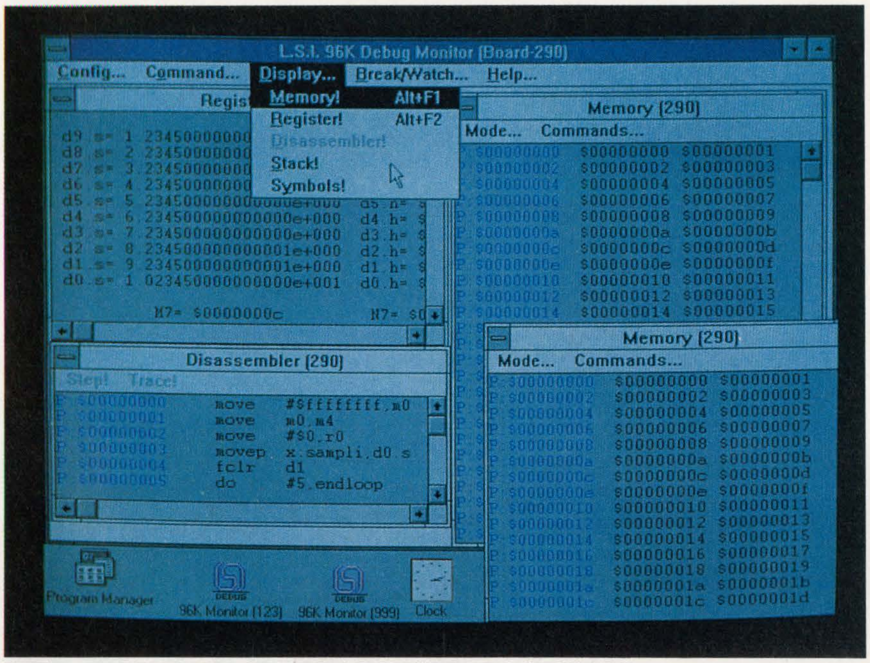
The controller features a transfer speed of up to 6 Mbits/s, a 1.2-Mbit/s digital phase-locked loop, and a 64-byte internal first-in, first-out (FIFO) memory for the transmitter and receiver. Also included are a DMA interface and collision detection. The controller is suitable for printers, diagnostic systems, robotics and communication networks. It's in a 44-pin plastic leaded chip carrier and costs $8 in 10,000-unit lots.

To speed up design-in time, Siemens offers an evaluation board for IBM PCs. The board has two SAB82526 ICs, an 80188 processor, and a dual-port RAM. Menu-driven software, a board description, and a manual complete the design kit.

Rugged miniature pushbutton switches that comply with MIL-STD-22885C and the new pan-European CECC96000 quality-assessment approval will be exhibited for the first time at Electronica by ITW Switches Ltd., Portsmouth, England. The momentary-action with tactile-feedback silent Series 59 switches, using improved-contact plating techniques, have a life of 50,000 cycles.

To debug a multiprocessor computer, Microsoft Corp.'s Windows 3 graphics user interface would be a good choice. This is particularly true when the processors to be debugged are on cards added into a IBM AT or compatible. That way, each processor can have its own set of windows, visible on-screen simultaneously with each of the others. That environment was chosen by Loughborough Sound Images Ltd., Loughborough (pronounced LUFF-bruh), United Kingdom, to ease software development for its new DSP96002 DSP board *(Fig. 2)*.

Up to four of the cards, based on the Motorola DSP-96002 digital-signal-processor chip, can be added to a PC and interlinked to give a combined processing power of up to 200 MFLOPS. Each board can contain up to 4 Mbytes of fast static RAM. The



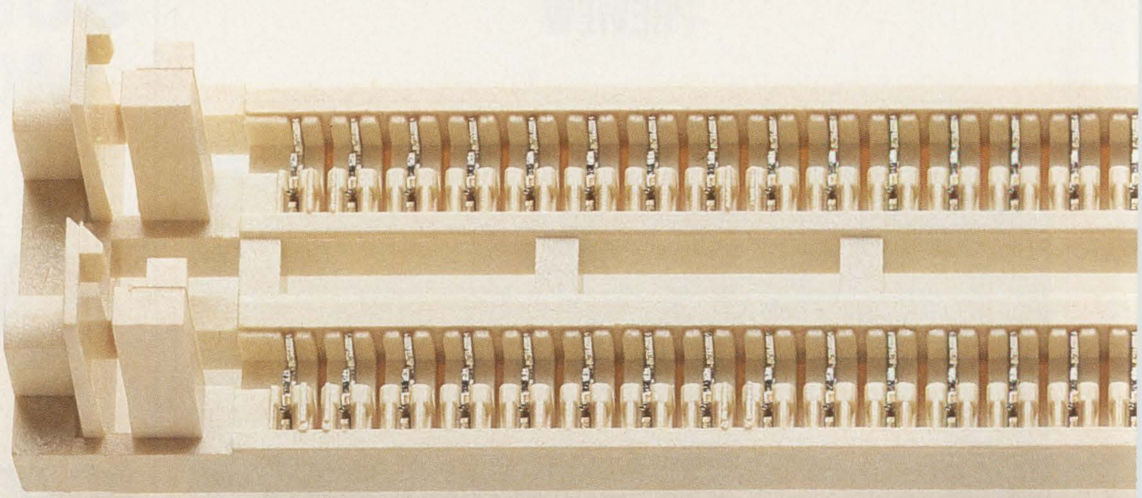
2. DEBUGGING SEVERAL MICROPROCESSORS **simultaneously in a multiprocessor system (each with its own window) is possible with the DSP96002 DSP board from Loughborough Sound Images. Register, disassembler, and memory activity can all be displayed at the same time to ease software development.**

SRAM can be configured in one of two ways: to provide three distinct data regions for each of the 96002's two ports as well as for program memory, or for partitioned memory to software, enabling X and Y memories to be defined dynamically during operation. Proprietary logic controls 2 kwords of dual-port RAM, which appears as an 8-kbyte block in the host-PC's memory map. The map is accessed through the ISA bus for fast data transfer to hard disks and video displays.

The DSP-96002 board is rich in interfaces. In addition to the ISA PC bus connection to the host PC, Loughborough has made full use of the Motorola chip's many ports. Interprocesser links are set up through a proprietary 96-way parallel backplane that the company calls Motoway. This is an extension of the memory bus with added control lines for arbitration logic. With these lines, each of up to four interconnected boards can be defined dynamically as bus-master, thus making it possible to address the SRAM on all other boards in the system. Loughborough describes the set-up as a "four-layer round-Robin arbiter." Using the Motoway bus allows the DSP boards to transfer 32-bit words at 44 Mbytes/s. For external interconnection, an "open-standard" 50-way interface uses the Motorola DSPLINK ports to provide access to "off-board resources." Loughborough is building a range of peripheral interface boards for such applications as digital audio processing, multichannel analog-to-digital converters (ADCs) and digital-to-analog converters (DACs), and a board to capture high-speed transients.

United Kingdom price for the DSP96002 board is between £3295 and £3795, depending on memory configuration. Adding support software, including Windows 3, may tack on an extra £1,200. Loughborough says delivery depends on the availability of the Motorola DSP 96002 chip. The board will be ready to ship during December.□

HOW VALUABLE?	CIRCLE
HIGHLY	562
MODERATELY	563
SLIGHTLY	564



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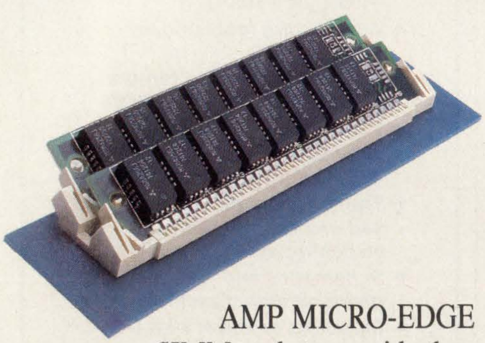

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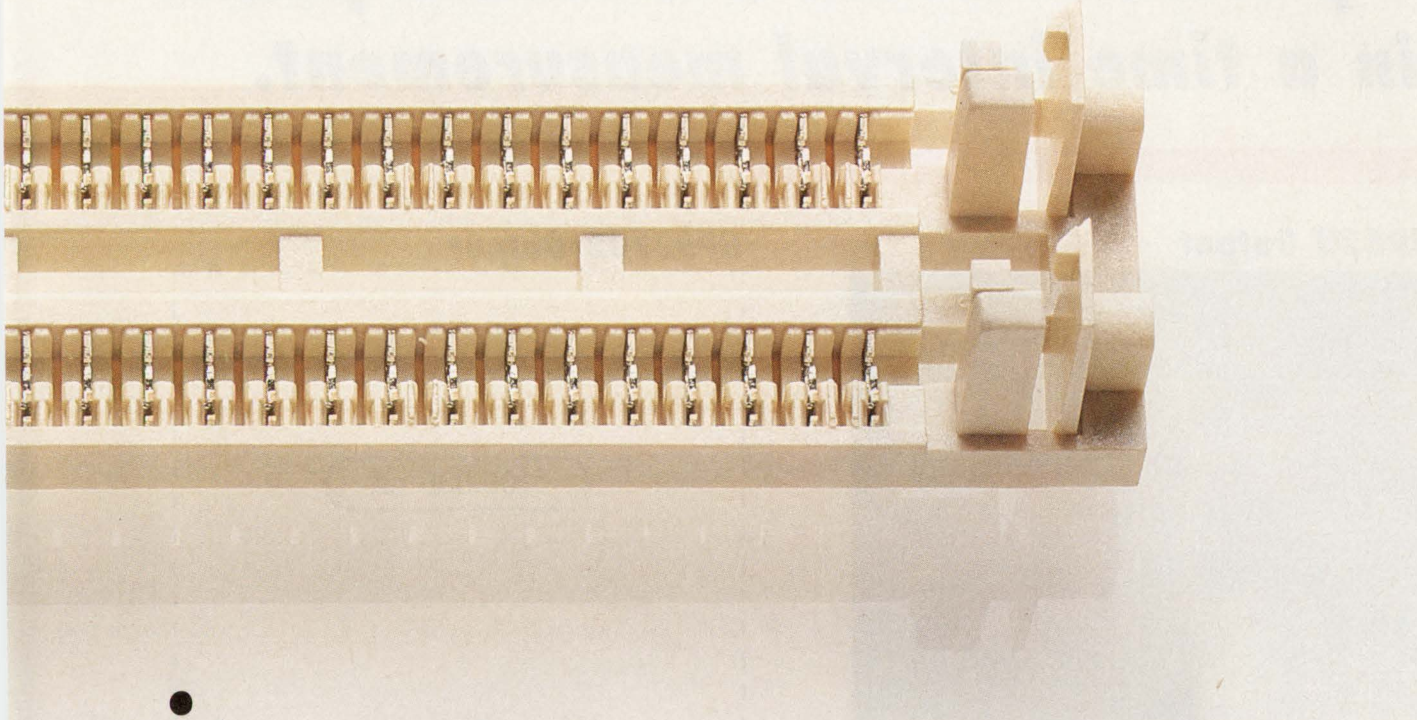
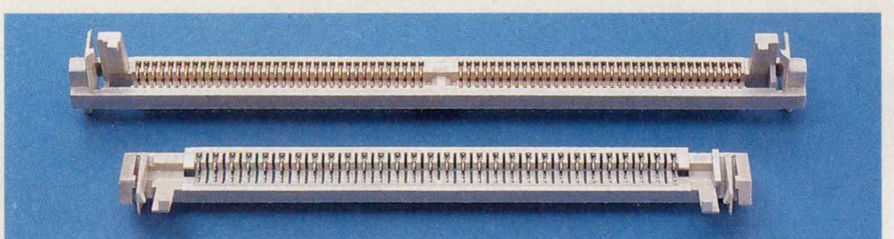
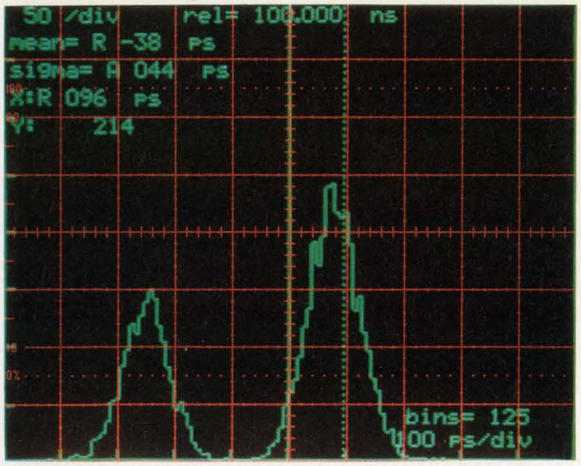




A picture is worth a thousand points in a time interval measurement.

SR620 Output



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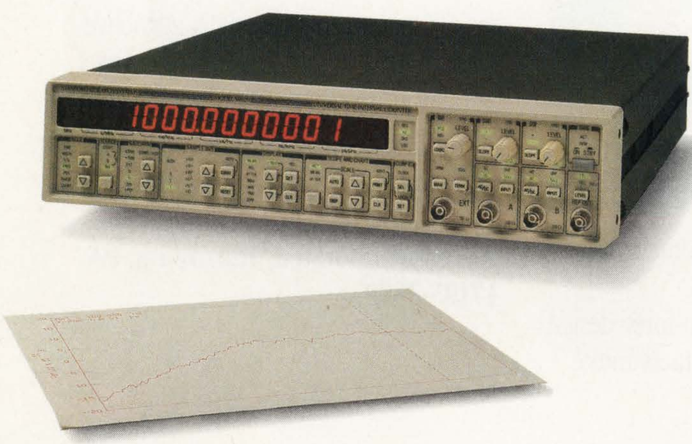

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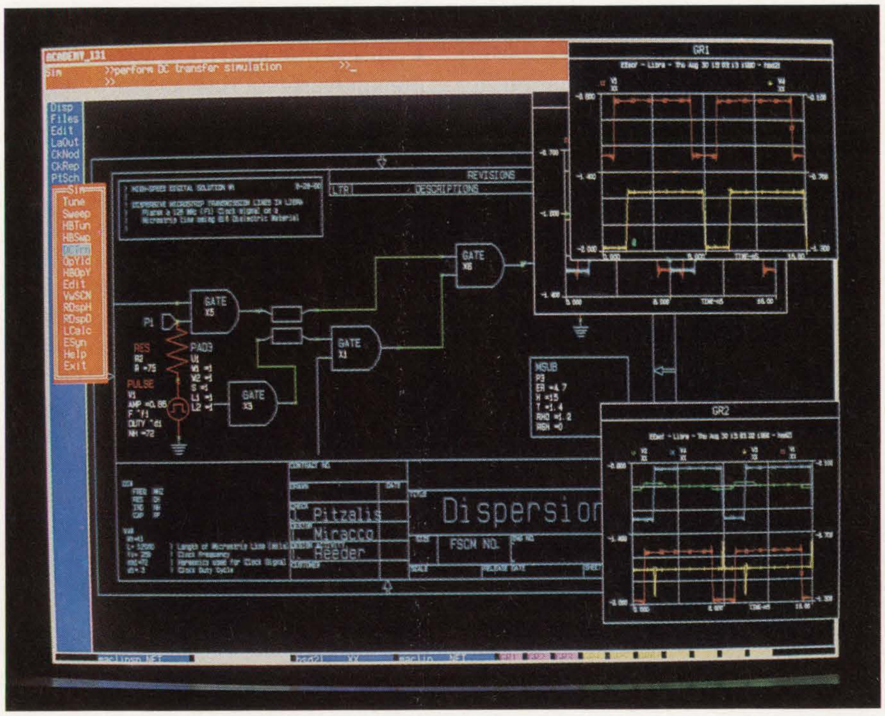


MIXED-SIGNAL SIMULATORS ABOUND

FRANK GOODENOUGH

TODAY'S MIXED ANALOG-DIGITAL SIMULATORS HANDLE JOBS FROM DC AND FAST LOGIC TO MICROWAVES.

The upsurge in systems well-populated with mixed-signal ASICs has spearheaded the arrival of a broad range of mixed-signal simulators. Although these tools aim at aiding the design of both mixed-signal systems and ASICs, a major need for these tools has sprung up from another quarter. Rapidly rising clock speeds of purely digital systems have forced board and ASIC designers to consider second- and third-order analog effects that cause clock skew and ground bounce. As a result, mixed-signal tools and a diverse group of circuit simulators—from special versions of Spice to special versions of microwave simulators—are being brought to the digital design arena.

Most mixed-signal simulators consist of one or more analog and/or digital point tools, under the aegis of the large open frameworks being developed by major electronic-design-automation (EDA) tool suppliers. In most cases, the point tools are hierarchical, operating at levels ranging from circuit primitives (discrete active and passive devices) to such programming languages as VHDL (its analog equivalent, AHDL, may be no more than three years away).

Many of those point tools, particularly analog-circuit simulators, come from third-party tool suppliers and are available within frameworks from multiple companies. Each tool and framework offers its own features and benefits. Analog tools continue to increase in speed and performance. Such features as optimization, synthesis, and design centering are being added to their presently available statistical tools, including Monte Carlo and sensitivity analysis.

While some mixed-signal tools focus on IC design, and others on system design, the capabilities of each are being forced to merge. Today's designers must capture and simulate a complete system at a high level, then gradually partition the system into standard parts and ASICs. Next, designers must determine the mix of analog, mixed analog-digital, and digital ASICs; in each case deciding between array and cell approaches. Finally, the individual ASICs must be partitioned and designed. Throughout the process, the simulation of the complete system and its parts must be repeated, with different blocks modeled and simulated at different levels.

If the design process occurs within a framework, it's possible to sequentially simulate different parts of the circuit or system at different levels of hierarchy. This permits concurrent top-down and bottom-up designs, with designers often changing simulators as the design process continues. Moreover, the ultimate goal of framework designers is to let the tool user switch between levels and simulators on-the-fly, and employ several simulators of the same type at the same time. While more than one digital simulator can now be used simultaneously on different parts of a system, no one has figured out how to do it with circuit simulators.

So-called mixed technology, or mixed-media tools, has added another dimension. These tools aren't limited to modeling and simulating just electrical/electronic elements; they can also handle mechanical, optical, thermal, chemical, and other phenomena. Simulators with this capability are now available from Analogy, Intergraph, Meta-Software, and Valid Logic. Real-world analog signals can be used to stimulate simulation and hardware modelers. Hardware accelerators are available for the digital portion of the systems. In addition, most of the frameworks offer the use of multiple platforms, at the same time, to speed simulation.

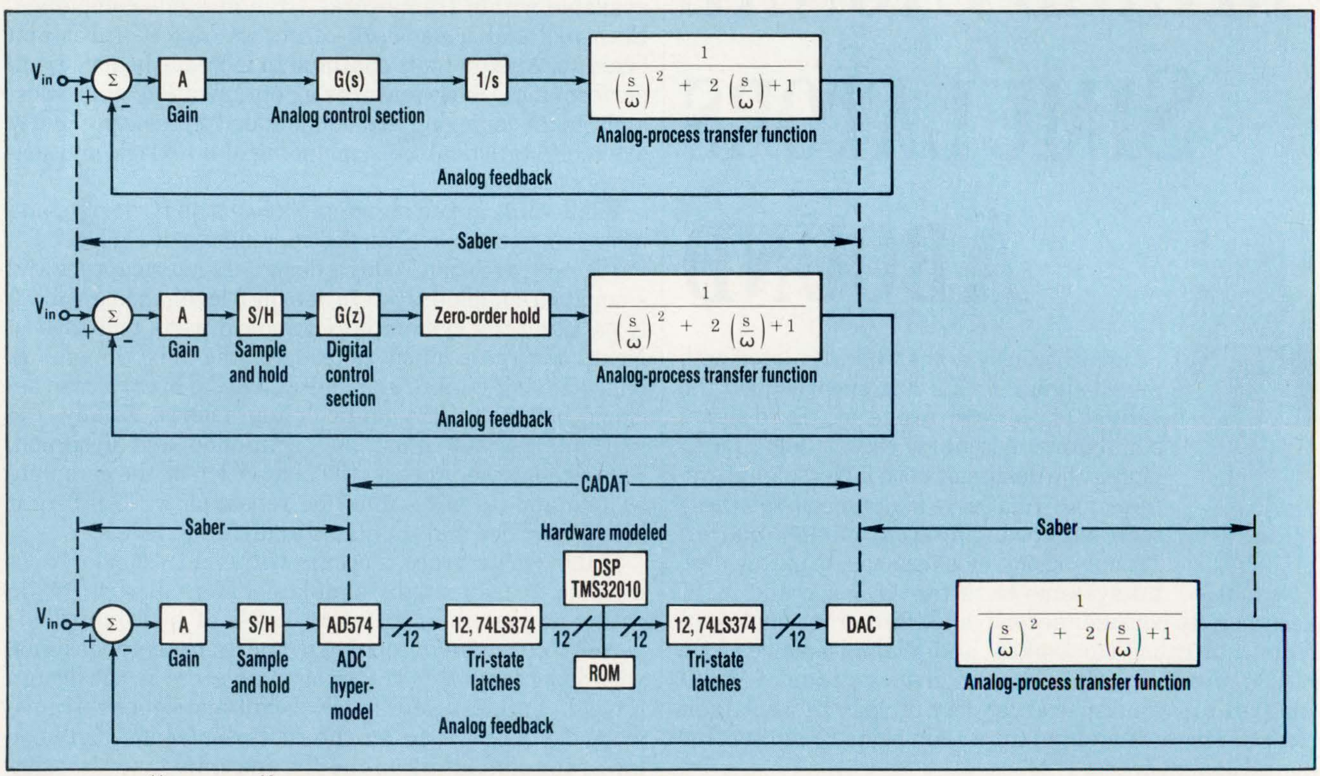
The most accurate simulators are circuit tools, such as the ubiquitous Spice. *(see "SpiceY tips," p. 45)*. In its most accurate form, circuit simulation of complex analog circuits with transistor-level models can take hours on a Cray computer, while a million-transistor microprocessor simulated in Spice could tax the computing power of a code-cracking organization. Basically, multilevel and mixed-signal simulators trade off simulation accuracy for computing time.

If all versions of Spice as well as the different look-and-feel of each point tool are included on each framework porting it, the varieties of mixed-signal simulators can be overwhelming. But even though mixed-signal simulators breakdown into the six general species, at times it's unclear as to which group a particular tool belongs. In order of decreasing accuracy and increasing computational speed, mixed-signal simulators can be classified as:

- A Spice simulator.
- One that uses high-level analog models of functional digital blocks, such as gates, flip-flops, and registers (and analog blocks that include op amps).
- One with a built-in, event-cue-driven digital simulator.
- A so-called "glued" simulator, in which digital and circuit simulators are tightly linked by communications software.
- An event-cue-driven, logic or timing-analysis tool with analog ability.
- A high-level language that can handle both analog and digital entries.

In general, the glued simulator works best for loosely coupled systems containing large blocks of analog and digital circuits with relatively few events passing between the two simulators. Easy multiprocessing is possible with the simulator. For example, the digital logic can be handled by the user's workstation, and by the compute-intensive analog simulation on a server or second networked workstation (Valid Logic and Analogy recently announced the ability to offload a portion of a pure analog simulation on additional machines).

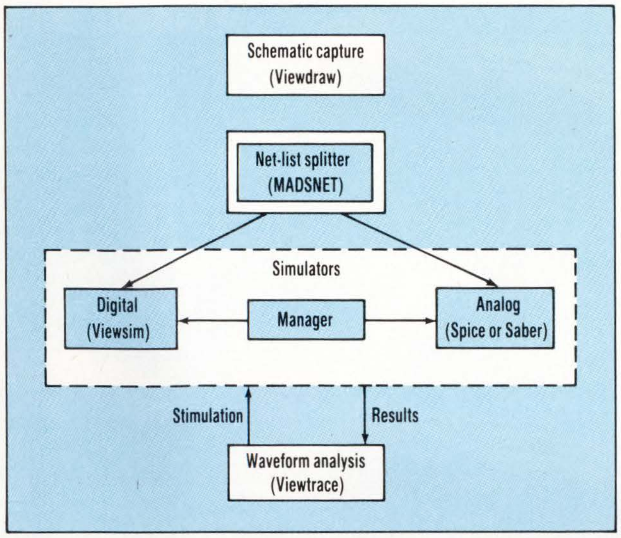
The top-down design of a mixed analog-digital feedback control system is one example of the glued simulator's proficiency. At the heart of the system lies a digital signal processor, although both the input signal (the process itself) and the feed-



1. THE "GLUED" MIXED ANALOG-DIGITAL SIMULATOR, Saber-CADAT from Analogy/Recal-Redac, allows for top-down design, simulating a process plant feedback control system at three levels: frequency domain, G(s), top; time domain, G(z), including the acquisition and processing of sampled data, center; and circuit level (bottom). At the circuit level, the TMS32010 digital signal processor is operated within a hardware modeler.

back signal are analog. A 12-bit analog-to-digital converter (ADC) and digital-to-analog converter (DAC) connect the processor with the real world *(Fig. 1)*. The circuit was simulated with Saber-CADAT from Analogy/Recal-Redac at three different levels. At the third level (bottom), a CATS 12000 hardware modeler simulated the TMS32010 digital signal processor as a real device.

With the exception of the last item on the listing of simulators, the remaining tools are often lumped under the general term "core" or "unified" simulators. They're particularly useful when there's tight coupling between analog and digital circuits (for example, within an ADC or phase-locked loop). However, nearly all the major glued and core simulators successfully simulated tightly coupled circuits.



2. "NETWORK-SPLITTER" software is used in glued mixed-signal simulators, such as Viewsim/AD from VIEWlogic. The splitter sends digital models to a digital simulator and analog models to a circuit simulator. Models tagged for a simulator are available in the frameworks library. Designers can tag them at the schematic-capture stage.

Either or both tools (digital and circuit simulators) that form a typical glued simulator may already have some mixed-signal capability. For example, the analog tool might have so-called analog macro, or behavioral, models of digital blocks, like the Spice models in Valid Logic's "Analog Workbench II," Cadence's "Analog Artist," Meta-Software's "HSpice," and "Precise" from Electrical Engineering Software (EES) (Non-Spice-based Saber also has analog macros). Alternatively, they might have built-in event cues, such as Analogy's "Saber," MicroSim's "PSpice," and the just-announced "ISIM-se" from Intergraph.

With the exception of the pure-circuit simulators, all of the mixed-signal tools contain code that determines whether a portion of a circuit (a model) should be handled as an analog or as a digital entity. In such glued tools as VIEWlogic's "Viewsim/SD," this code is called a "net-list splitter." It divides the initial net list created during capture of the system schematic into two separate net lists—one for the analog simulator and one for the digital simulator *(Fig. 2)*. In both the core and glued tools, circuit/system elements are tagged as either analog or digital models so that the simulator knows how to treat them. These tags are attributes of the model and are handled similarly to the resistance of a resistor, the beta (current-gain) of a bipolar transistor, or the propagation delay of a logic gate.

If the blocks are standard parts in the library of a framework, the tags are already there at capture. If designers create a model at any level from discrete transistors to a high-level language, they apply the tag. In most mixed-signal tools, the type of model (either analog or digital) can be switched at any time.

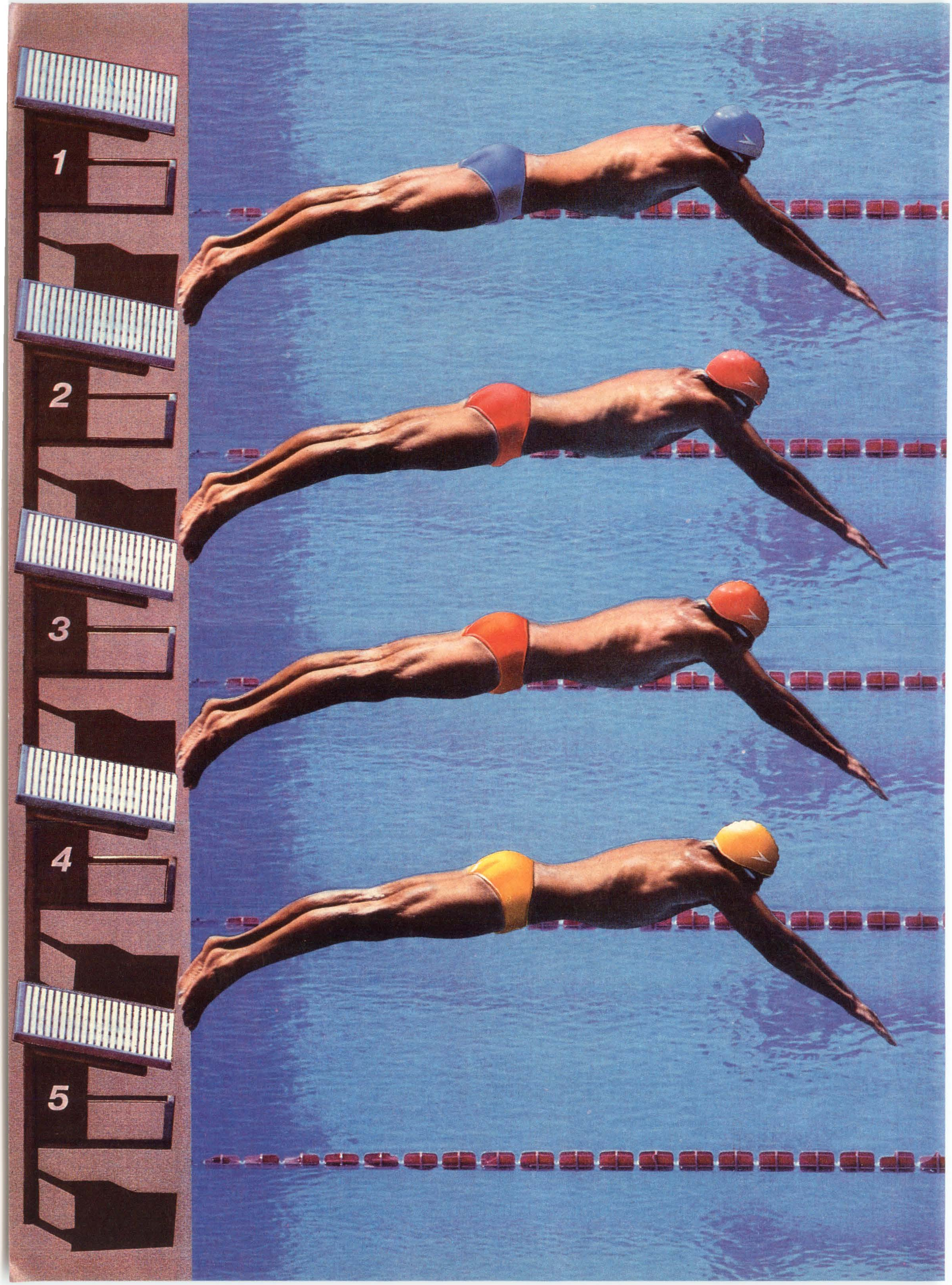
As the net-list splits in the glued simulator, a one-bit ADC model is inserted automatically between analog and digital circuits if the analog circuit drives the digital circuit. Should the digital model drive the analog one, a one-bit DAC model is inserted. The accuracy of these converters, often called "hooks", determines the performance of the simulator. Similar hooks do the same job in the unified tools. Analogy calls these hooks "hyper-models."

Regardless of tool type, the level of simulation selected in the hierarchy for each portion of the circuit/

"SPICEY TIPS"

Whether you're a day-to-day user of Spice or a newcomer to circuit simulation, you may want to take advantage of the newsletter "Inside Spice," published six times a year by RCG Research of Indianapolis, Ind. Each issue of this 8-page letter packs up-to-date information about circuit simulation and includes tips on curing convergence and other problems that can occur when using Spice. Many tips are given in its "User's Corner," where questions from readers are answered. Additional topics have included modeling, and the relative speed of various PC platforms. The latest issue is devoted to a hands-on evaluation/comparison (including pricing) of five popular versions of Spice available for the PC: IS—Spice from Intusoft, HSpice from Meta-Software, Spice2 and Spice3 from Northern Valley Software, MicroSim's PSpice, and Microcap III from Spectrum Software. Visionics' Spice-based tool will be reviewed in an upcoming issue.

A subscription to Inside Spice runs $60 for the first copy; each copy is $24. RCG Research also offers one-day hands-on training classes (in major U.S. cities) for beginners, present users, and expert users of Spice. Each one-day class costs $240. For additional information on Inside Spice and/or the classes, call Ron Kielkowski at 1-(800) 442-8272.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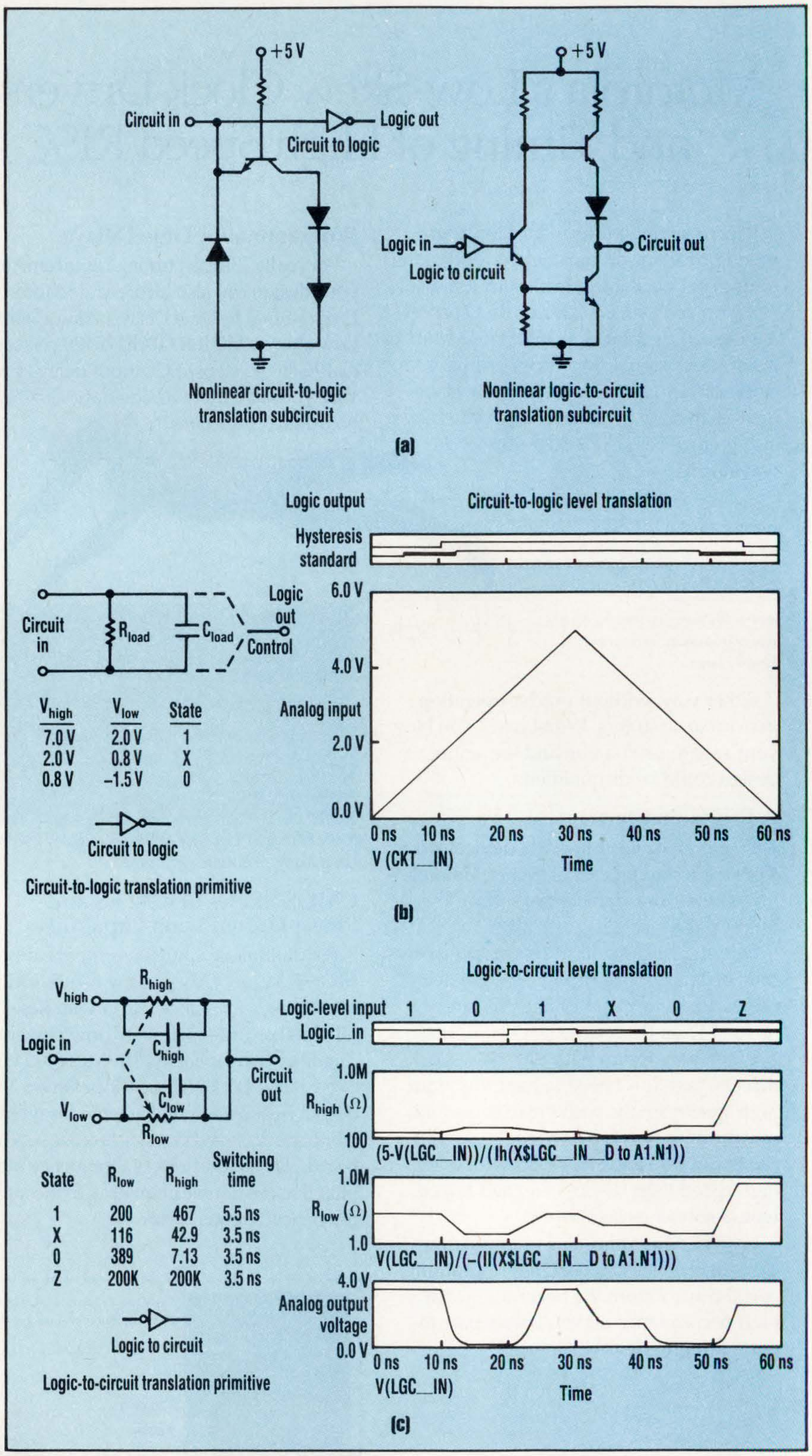
system determines the complexity of the hooks. The hooks can be nonlinear subcircuits or simple primitives *(Figs. 3a, 3b, and 3c)*. These software models are used by MicroSim (called circuit-to-logic and logic-to-circuit translators by the company) in their "Digital Simulation" option, a single unified simulator using a 28-state event cue within PSpice.

A digital event is a change in a signal's state at a specific time. When a time-step of the on-going, current simulation reaches that of any pending events, the signal's new state is propagated to every device it's driving. The new devices, in turn, are evaluated to see if a transition should occur. This causes another event at the current time plus the propagation delay of the device. Similar translators are used in the glued simulator Viewsim/SD, which employs PSpice as its circuit simulator.

The TTL circuit-to-logic (C-to-L) primitive looks like an R-C circuit *(Fig. 3b)*. When fed up and down ramp voltages, it delivers a logic-zero output when the input is between –1.5 and 0.8 V, an X (unknown) state between 0.8 and 2 V, and a logic 1 when the input is between 2 and 7 V. The analog output of the TTL logic-to-circuit primitive models the upper and lower npn transistors in a totem pole as different resistor values for the 1, X, 0, and Z (high-impedance) states *(Fig. 3c)*. The capacitance is handled by the switching time (TSW). The result is an output waveform of rise and fall times, and dc values. There's a double line in the digital waveforms for the X state and solid lines for the Z state (three state). The C-to-L and logic-to-circuit (L-to-C) symbols can be shown on the schematic, or deleted.

At the heart of all simulators lie their numerous algorithms. One of the most important in mixed-signal tools is the algorithm that synchronizes the timing between the circuit simulation and the internal event cue of a unified simulator or the digital tool of a glued simulator. In virtually all cases, the two run separately and are synchronized only when information must be passed between them. With these algorithms, the cir-



3. SIMPLE 1-BIT ADCs AND DACs in mixed-signal simulators prepare signals for alternative forms of processing. Called "circuit-to-logic" and "logic-to-circuit" translators by MicroSim, they may contain active, nonlinear elements (a). They may also be simple primitives (b and c). However, even in the latter two cases, the effects of resistance and capacitance are considered when handling, or creating, real-world waveforms.

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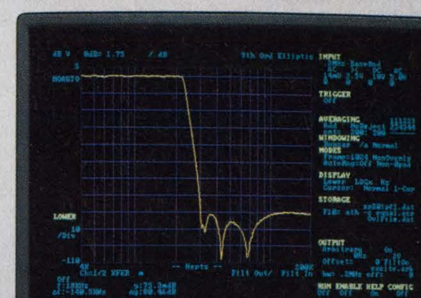

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cuit simulator can run at a maximum rate when nothing is happening in the analog circuitry. As a result, the variable time-step capability of typical circuit tools, such as Spice and Saber, is used to its maximum. Inherent in today's circuit simulators is a record of everything that has previously run. Thus, it can jump ahead of the digital simulator in time.

FROGGY TOOLS

For example, if the circuit tool is at some arbitrary time t_5, and the digital tool has a new event input for it at an earlier time t_3, the circuit tool jumps back to t_3. It also receives the new information and takes up a new simulation path, integrating the new data into the differential equations it's solving. Similarly, if an analog event causes a change of state in the digital world, it will be given to the event cue for scheduling, with a delay if the circuit tool is ahead of the digital tool. Alternatively, the digital operations can be processed with zero delay, feeding the results back to the circuit tool to see the effects. It's mandatory that these mixed-signal tools accurately handle feedback of all types at every level.

Analogy calls their software that implements these techniques within Saber the "Calaveras algorithm," from Mark Twain's famous story about a frog that jumped forward and backward. Saber and its frog is now used as the circuit tool in the following glued simulators: Saber-CADAT, Cadence's new system simulator "Saber-Verilog," and in Europe, GenRad's "Saber-HiLo." Saber-CADAT is also available from ComputerVision, and from NCR and Gould AMI for use with their mixed-signal standard-cell libraries. Other similar glued tools include Analog Artist-Verilog and Viewsim/SD.

Virtually all successful mixed-signal simulators are also multilevel tools. For example, Saber has device-level primitives and analog macros, and can also represent large parts of a system when capturing a system at high-level equations. And Analogy's MAST programming language can be employed at an even higher level.

Moreover, alternatives to Saber for high-level circuit modeling and simulation are now accessible. Meta-Software supplies behavioral models for HSpice, and can employ equations as functional blocks. They're now available as the analog tool in Viewsim/AD, complementing PSpice as an alternative to Cadence-Spice in Analog Artist, and along with Saber and Precise as the analog simulators in Mentor's Explorer Lsim. Also, Valid's recently announced Analog Workbench II can do multilevel analog simulation.

DIFFERENT STROKES

Explorer Lsim from Mentor Graphics was designed originally as a unified, multilevel digital tool so that designers of digital CMOS ICs could operate with different parts of their systems, modeled and simulated at different levels, from device to VHDL. However, it evolved into a framework incorporating a collection of simulators, including both unified and glued multilevel, mixed-signal tools. It's equally at home with ASICs, boards, and even systems. And by the end of next year, it will operate under Mentor's Falcon Framework.

The tool's digital capability is built from a multilevel digital simulator plus a special high-speed circuit simulator for CMOS digital circuits. IN addition, HSpice, Precise and Saber are also now available for circuit-level simulation. These three tools also take care of analog-simulation tasks. Mixed-signal simulation is performed either by moving vertically or horizontally through the mixed-signal boundary *(Fig. 4)*. Vertical movement occurs when digital-circuit simulation is performed; horizontal movement occurs when handling mixed analog-digital blocks. However, even Lsim's programming language M can provide analog behavioral modeling of digital circuits with text entry, creating the analog-to-digital and digital-to-analog primitives. It produces an analog waveform by calculating a V_{out} applied to a gate output that's modeled as a

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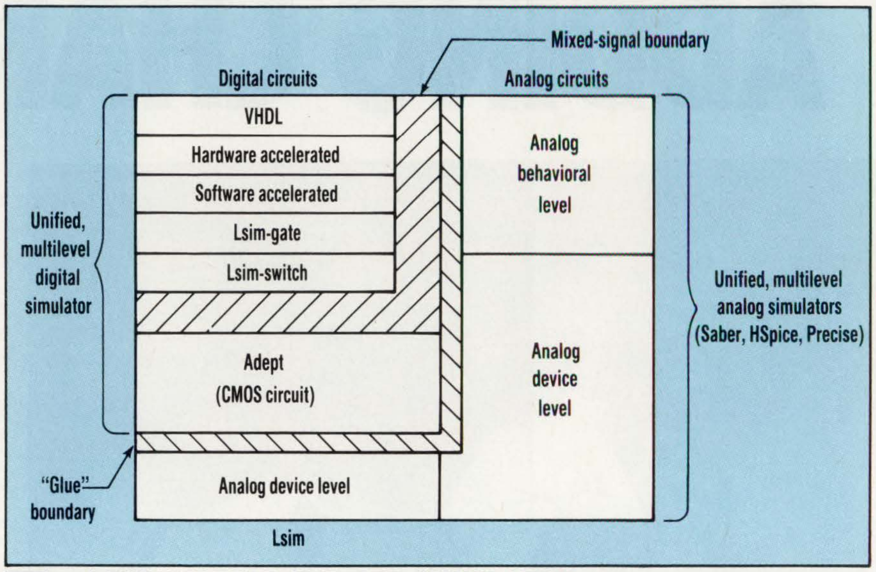
Thevenin-equivalent driver—similar to those described for PSpice.

The multilevel digital portion of Lsim enables users to assign, and reassign, portions of the circuit to any level during the simulation, depending on the accuracy desired. Consequently, one part of the circuit can employ VHDL, another major block may use the hardware accelerator MACH (built by Zycad), a third may work at the gate level, and a fourth could take advantage of the accurate timing offered by the switch-level tool. The tool includes not only R-C circuit parasitics, but it can also simulate bidirectional circuits, such as a CMOS pass-transistor EXOR gate.

In addition, designers can move a part of a CMOS circuit at any time into Adept, a unique transistor-level analog-simulator for digital circuits. Unlike Spice or its variants, which take discrete time steps and solve equations for voltage, Adept takes discrete voltage steps and solves for time. In addition, similar to event-driven logic simulators, it only evaluates active nodes. As a result, simulation time grows linearly with the number of transistors rather than exponentially, as with Spice. Mentor says Adept always converges.

Semicustom chip makers Sierra Semiconductor and International Microelectronic Products (IMP) have adopted Lsim for their mixed-signal standard-cell libraries. In fact, Sierra added proprietary analog algorithms to Lsim to create a mixed-signal tool called Montage.



4. A MULTILEVEL UNIFIED SIMULATOR is incorporated in the Lsim mixed-signal tool within a glued simulator. The mixed-signal boundary may be crossed vertically while simulating digital circuits, or horizontally to handle analog circuits.

SALTY SIMULATION

A real sleeper in the mixed-signal simulator arena could be SALT from the CAD Group Inc. A true multilevel, mixed-signal, unified simulator, SALT was designed, like Lsim, to deliver high-speed and accurate simulation of large digital ICs and even multi-IC systems. Also like Lsim, it's event-driven and handles digital models at all levels, from switch to HDL, concurrently within the same simulator. SALT also handles analog circuits and incorporates analog-to-digital and digital-to-analog hooks. Its speed on analog circuitry is 50 to 100 times that of Spice, and its performance correlates well with Spice. SALT also was ported to, and successfully run on, platforms from PCs to Crays (virtually all other mixed-signal tools require too much memory for PCs).

Various forms of statistical analysis represent major features secondary to most circuit simulators. These features include Monte Carlo, sensitivity, and stress analysis, all based on performing repeated and directed simulations. For example, Analog Workbench II using Monte Carlo determines the combined effect of variations in component tolerance on the dc, ac, and transient performance of the circuit. Sensitivity analysis run with the tool determines the sensitivity of a circuit's dc, ac, or transient performance to individual design variables—component values, temperature, and process variables. When performing stress analysis, Analog Workbench II simulates actual operating conditions of all circuit elements, including passive parts, semiconductors, and power supplies. It flags any of these elements which exceed their voltage, current, or power ratings.

New features in this genre include optimization, synthesis, and design centering. Optimization programs, available as an option to Precise and to Analog Artist, help designers choose exactly the right components to maximize circuit performance. For example, optimization goals for an amplifier can include maximizing voltage gain, or gain-bandwidth, while minimizing power drain. Optimization programs are particularly useful in tailoring the frequency response of a circuit with multiple peaks and dips. And it's been used successfully to reduce ground-bounce in digital IC design.

Just as designers might do multiple "what ifs" on a breadboard (or simulator), an optimization tool takes an initial circuit and performs multiple simulations. For each simulation, it changes from one to all component values. But these aren't random selections. Rather, after each simulation, the tool examines and analyzes the results and tries a new value based on the results. If a larger resistor was expected to raise gain at a given frequency on a particular pass, but the gain dropped, the tool would try a smaller resistor on the next pass.☐

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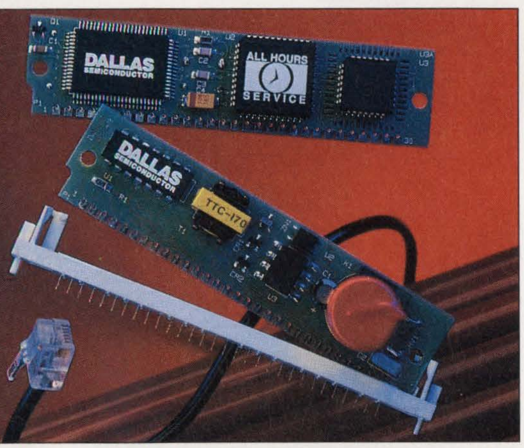

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LOGIC ANALYZERS

DESIGNERS WHO ONCE SHUNNED THE LOGIC ANALYZER NOW FIND INSTRUMENTS THAT ARE MORE CAPABLE AND EASIER TO USE.

JOHN NOVELLINO

The logic analyzer was often considered a tool of last resort, the instrument designers pulled out only when they couldn't find a problem by other means. Today, however, a logic analyzer is often the designer's tool of choice, from board turn-on through hardware-software integration. In addition to their traditional role in research and development, logic analyzers are finding applications that stretch into manufacturing and service.

Several reasons account for this new popularity. Better interfaces, including menu-driven screens, and microprocessor pods and adapters for fast connections, make logic analyzers easier to use. In addition, higher levels of integration have reduced analyzer prices while improving performance. And in some cases, the logic analyzer is simply the only instrument fast enough to debug current designs.

The speed issue is particularly important to designers working with advanced microprocessors. With 33-MHz speeds becoming common, it's hard to find suitable emulators, especially if price is a concern. But logic analyzers and disassemblers available today can help designers debug microprocessor code over 50 MHz.

Consequently, a trend toward using logic analyzers as the primary debugging tool has emerged. It started with the introduction of RISC processors, because no emulators existed for these devices. The trend spread to digital-signal-processing applications, because no emulators exist for DSP chips, and to the high-power CISC processors competing with RISC speeds.

Emulators have two important pluses compared with logic analyzers: They can single-step through code and are able to look inside a chip's registers. But an emu-

lator is at a disadvantage because it must get signals out to the system under test and back, and it must simulate the system's entire memory, notes David Blakemore, vice president of Arium Corp. Sending signals out and back is a technical challenge, and both problems are very expensive. "An analyzer with a really good disassembler, an embedded debugger, and a ROM-emulation system (either separate or in the logic analyzer) costs much less than a microprocessor emulator for the same speed," says Blakemore.

Although logic analyzer prices have ebbed in recent years, designers shouldn't expect that trend to continue, especially if they want to work with the latest microprocessors. These devices need analyzers with more channels and deeper memories, as well as 50- to 100-MHz speeds. Adding channels and memory aren't major technical hurdles, although they obviously increase prices. Keeping up with processor speeds is the tough job.

As a result, analyzer prices are probably going to flatten out, according to Greg Peters, a product marketing manager at Hewlett-Packard Co.'s Colorado Springs Div. "We're forced to use more expensive technology to get the functionality that the customer needs," says Peters. "For 100 MHz, we have to go to ECL, and that gets a lot more expensive. ECL obviously has less density and needs more power, and those factors generally mean a higher cost of processing."

As important as cost is in these competitive times, no instrument is a good value if it doesn't do its required job. For complex instruments, the right specifications are highly dependent on the application. This is even more true of logic analyzers. Speed, number of channels, and memory depth, are obvious considerations and relatively easy to evaluate.

Designers working on microprocessor-based systems, however, must make microprocessor support their first priority. They should look at the disassembler available for the specific processor or processors being used, as well as the probing scheme for connecting the analyzer to the device in the system.

TAKE A TEST DRIVE

Peters advises prospective users to actually connect hardware to competing systems: "Just try out what they have. I say that because whenever people talk about microprocessor support, so many variables are always involved."

HP offers a broad range of microprocessor support, which the company calls preprocessing, for its two logic-analyzer lines. The low-cost, portable HP 1650 series and the high-performance, modular HP 16500 series accommodate processors from Hitachi, Intel, Motorola, National Semiconductor, Zilog, and other manufacturers. Five models in the 1650 series range from 32 to 80 channels, with 100-MHz timing analysis and 25- or 35-MHz state speeds. The 80-channel 1652B and 32-channel 1653B include two 400-Msample/s digitizing oscilloscope channels. HP limits the scope bandwidth to one-fourth the sample rate—100 MHz—to avoid aliasing.

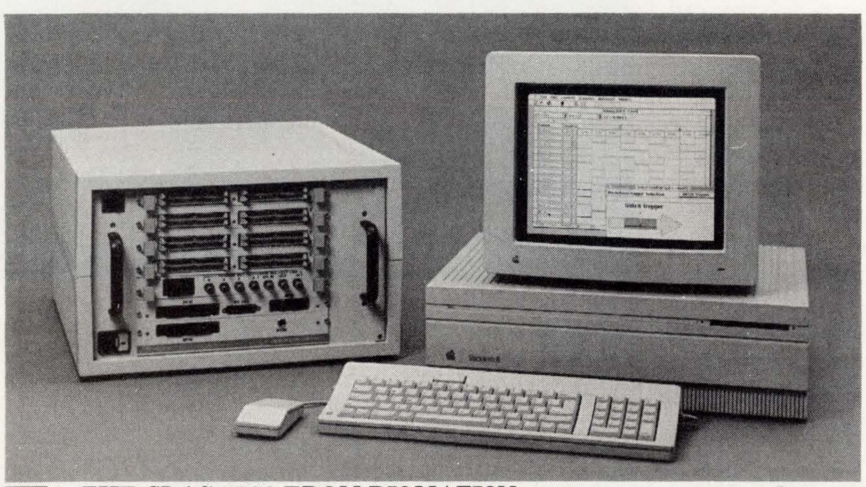
The 16500 series is based on a five-slot mainframe with a 9-in. color display. The HP 16510B module supplies 80 channels of 100-MHz timing analysis and 35-MHz state analysis. It also allows simultaneous timing and state analysis. Other modules offer 1-GHz timing capability, 5-Mbit/s pattern generation, and digital-oscilloscope functions. The newest module, the HP 16540A, boasts 100-MHz state and timing capability *(see "100-MHz Card, Improved Interface Enhance Analyzer," p. 68).*

Another critical consideration is the analyzer's trigger capabilities and trigger speed. To debug complex systems, triggering on event A, or event A followed by event B, may not be sufficient. Designers may want to trigger on a certain event, but only after executing a specific subroutine and after a specific pattern of interrupts. That requires a state machine with multiple states.

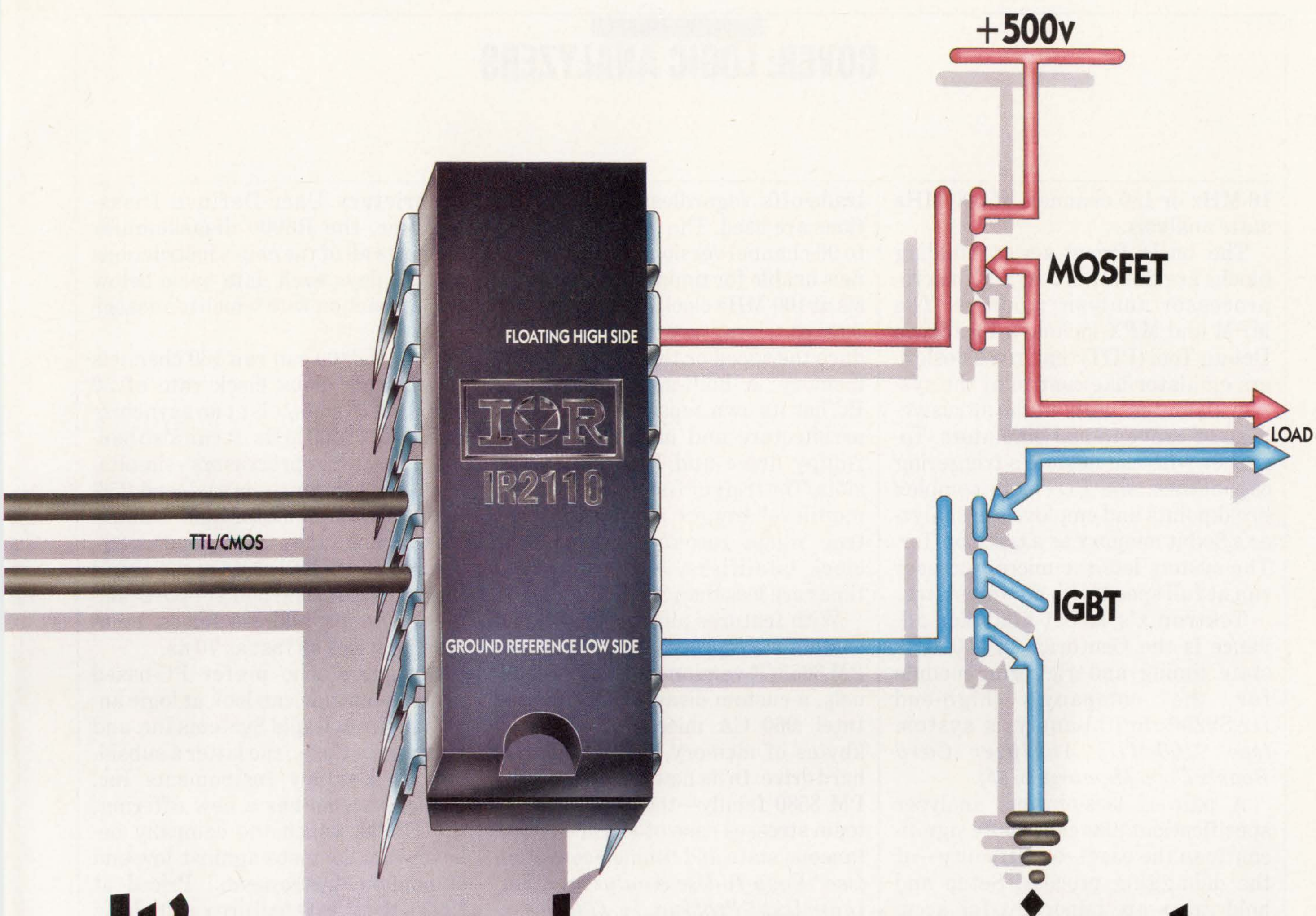
It's hard to generalize how many states are needed, but four is probably a good minimum, according to Chuck Wiley, strategic planning manager in Tektronix Inc.'s Digital Instruments Div. He notes that state triggers are more advanced than level triggers, so it's tough to equate the two types in terms of numbers.

For state analysis, it's important to trigger at the same speed at which the designer wants to acquire data. Because very high-speed triggers are hard to implement, Wiley cautions users to read the fine print. The analyzer may run at the desired speed, but if it won't trigger at that speed, the data rate for state analysis will be limited.

Tektronix expanded its logic-analyzer product line last year with the Prism 3000 series, a modular system available in three different package configurations. The Prism architecture integrates emulation and real-time performance analysis into the same platform with the more conventional logic-analyzer functions of state and timing analysis and microprocessor disassembly. Maximum capabilities include 90 channels of 200-MHz or 40 channels of 2-GHz timing analysis, and 960 channels of



1. THE CLAS 4000 FROM BIOMATION (left) is hosted by a Macintosh II computer. The analyzer mainframe can hold up to four 96-channel cards, which can be used as one 394-channel instrument or four separate units.



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CIRCLE 166

16-MHz or 180 channels of 300-MHz state analysis.

The basic Prism series building blocks are the MPM and MPX microprocessor analysis modules. The MPM and MPX include a Prototype Debug Tool (PDT) that gives designers emulator-like control of the system under test without the intrusiveness of conventional emulators. Together with the module's triggering capabilities, the PDT sets complex breakpoints and employs the analyzer's 8-kbit memory as a trace buffer. The system lets the microprocessor run at full speed with no wait states.

Tektronix's latest analyzer advance is the Centurion, a 100-MHz state, timing, and triggering module for the company's high-end DAS9200 digital-analysis system *(see "100-MHz Analyzer Card Boasts Deep Memory, p. 65).*

A pair of less-obvious analyzer specifications also contribute significantly to the ease—or difficulty—of the debugging process. Setup and hold times are important for accurate capture of the system-under-test's performance. Also, probe loading and its effect on signal capture can be critical. If the probe capacitance is too high, some microprocessors must be slowed down for proper operation. Moreover, probe resistance can mask glitches in the acquired signal.

Even with a thorough knowledge of an analyzer's specifications, designers must read data sheets carefully to find out if using various functions will affect the instrument's performance. For instance, a unit may be rated for 25-MHz state speed and 100-MHz timing. But if complex clocks are needed, the speed may drop to 17 MHz, warns Bob Roth, product marketing manager for logic analyzers in John Fluke Manufacturing Co.'s Philips T&M Group. Furthermore, the use of the glitch-capture mode or time tagging may cut speed and channel count or even state memory, says Roth. Designers can usually work around these limitations, but doing so can increase total test time significantly.

The Fluke/Philips PM 3655 logic analyzer requires no performance trade-offs, regardless of which functions are used. The unit comes in 24-to 96-channel versions, with all channels usable for timing or state analysis at 100-MHz clock rates. Using the 5-ns glitch-capture mode won't reduce the speed or the 2-kbit/channel memory. A built-in MS-DOS-based PC has its own separate system bus architecture and includes a 5.25-in floppy drive and four expansion slots. The trigger function features a multilevel trigger word sequencer, true range recognition, and four clock qualifiers. Setup and hold times are less than 2.5 ns.

With features aimed at RISC and custom microprocessor designs, the PM 3655/R version includes 96 channels, a custom disassembler for the Intel i960 CA microprocessor, 640 kbytes of memory, and a 40-Mbyte hard drive. In its new analyzers—the PM 3580 family—the Fluke/Philips team stresses ease of use and simultaneous state and timing acquisition *(see "Easy-To-Use Analyzers Eliminate Dual-Probing," p. 66).*

Arium also added RISC capability to its line with the MIP-R30 microprocessor support package for the ML4400 logic analyzer. The hardware-software package consists of a target interface adapter and disassembler for the MIPS R3000 RISC device. The adapter creates an easy connection to the board under test by plugging into the R3000's PGA socket. The processor plugs into the adapter. Implemented with Arium's proprietary User-Defined Disassembler, the R3000 disassembler supports all of the chip's instructions and displays each data cycle below the instruction with which it's associated.

The ML4400 can run 160 channels at a synchronous clock rate of 50 MHz and 16 channels at an asynchronous rate of 400 MHz. It can also handle four microprocessors simultaneously. A recently introduced 256-kbyte ROM emulator pod can replace and emulate most popular 28-, 32-, and 40-pin EPROMs in the user's target circuit. The pod supports single- or double-address buses, emulating devices as fast as 70 ns.

Designers who prefer PC-based instrumentation can look at logic analyzers from Rapid Systems Inc. and MetraByte Corp., the latter a subsidiary of Keithley Instruments Inc. Rapid Systems has a new offering, the R3800, which the company believes can compete against low-end standalone instruments. Priced at $2995, the R3800 features a 100-MHz sample rate on 32 channels. It performs timing analysis at up to 100 MHz and state analysis to 50 MHz. Memory depth is 16 kbits/channel for timing and 8 kbits/channel for state analysis.

For timing analysis, trigger capabilities include a sequence of four 32-bit data patterns. Multilevel, multiword triggers with data qualifiers are possible for state analysis. The analyzer comes with EGA color

LOGIC-ANALYZER VENDORS

Arium Corp. Anaheim, Calif. (714) 978-9531 **CIRCLE 301**	**Keithley MetraByte Corp.** Taunton, Mass. (508) 880-3000 **CIRCLE 305**	**Panasonic Factory Automation Co.** Secaucus, N.J. (201) 392-4050 **CIRCLE 309**
Biomation Corp. Cupertino, Calif. (408) 988-6800 **CIRCLE 302**	**Kontron Elektronik** Sunnyvale, Calif. (408) 733-0272 **CIRCLE 306**	**Rapid Systems Inc.** Seattle, Wash. (206) 547-8311 **CIRCLE 310**
John Fluke Mfg. Co. Inc./Philips Everett, Wash. (800) 443-5853 (206) 347-6100 **CIRCLE 303**	**Orion Instruments Inc.** Redwood City, Calif. (415) 327-8800 **CIRCLE 307**	**Tektronix Inc.** Beaverton, Ore. (800) 835-9433 **CIRCLE 311**
Hewlett-Packard Co. Palo Alto, Calif. (800) 752-0900 (719) 590-2429 **CIRCLE 304**	**Outlook Technology Inc.** Campbell, Calif. (408) 374-2990 **CIRCLE 308**	**Trace-Tek Instruments Inc.** Carrollton, Texas (214) 446-9906 **CIRCLE 312**

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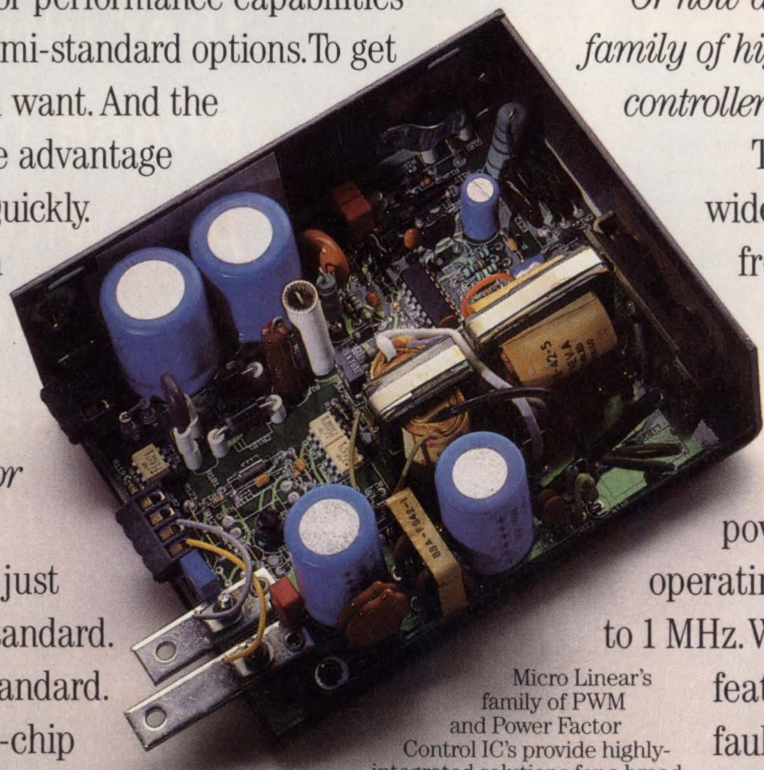

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Resonant Control	ZVS and ZCS to 3 MHz
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of the power curve.

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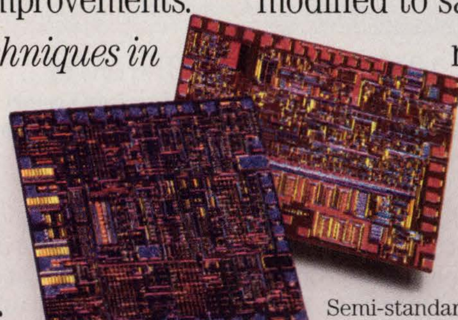

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CIRCLE 162

software with file, setup, trigger, display, and options menus. Optional disassemblers are available for most processors.

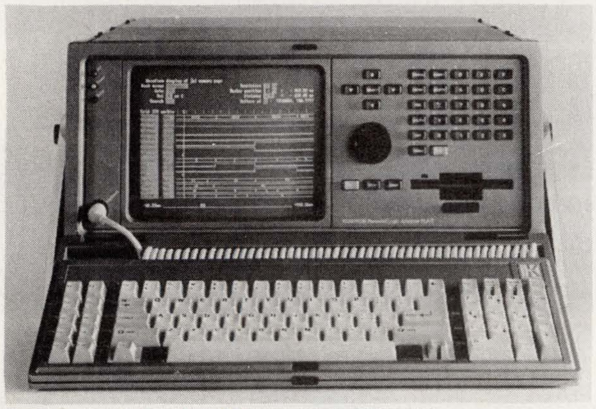
At only $1295, MetraByte's PCIP-DLA delivers a user-programmable sampling rate up to 20 MHz in either synchronous or asynchronous modes. A setup time of 2 ns ensures the validity of the acquired data, which can be displayed in a timing diagram or state format. The system consists of a full-size PC card containing clock, timing, memory, and interface functions, and two 8-channel pods. The pods, which connect to the board through a 3-ft. ribbon cable, hold all sampling comparators and buffer circuits.

To conserve data memory, users can set the programmable trigger function to pre-, post-, or midpoint positions. Alternatively, triggering can be initiated randomly through the keyboard. Trace memory is 256 words by 16 bits. The analyzer comes with menu-driven software for programming display type, board-address setup, trace type, clock select, sample period, display magnification, and data/disk functions.

Macintosh Control

A unique feature of the Biomation CLAS 4000 is that users control the system through an Apple Macintosh IIcx with a graphical interface *(Fig. 1)*. Pictorial representations establish probe location and reassignment, triggering, and external clocking. The Mac's large color monitor can accommodate 16 windows that contain such information as instrument configuration, status, and time-correlated data in multiple formats. A mainframe holds up to four measurement modules, a separate trace-control triggering module, and a Motorola 68000-based computer for mainframe control.

The basic measurement module supplies 96 channels at sampling rates to 50 MHz, with either internal or multiple external clocks. The module is software-configurable to 48 channels at 100 MHz or 24 channels at 200 MHz. The four modules can operate as completely independent analyzers or can be connected for 384-channel operation. A crosspoint switch in the module makes it possible for users to reorder the channels or reassign them as high-resolution inputs without moving the connections.



2. IN ADDITION TO OFFERING up to 192 channels, the PLA/2 portable logic analyzer from Kontron holds a complete PC/AT-compatible host computer. The 3.5-in. floppy drive and a 25-Mbyte hard disk are standard.

Another modular logic analyzer, the Kontron PLA/2, is hosted internally by a complete 80286-based, 10-MHz PC/AT-compatible computer. The system has a 3.5-in floppy drive, a 25-Mbyte hard disk, and an EGA/Hercules-compatible graphics card *(Fig. 2)*. Three open AT slots allow RAM expansion, modem use, or additional measurement capability. The basic analysis card is the Kontron 48-channel General Purpose Data Acquisition (GPDA) board. A PLA/2 can hold four GPDAs, which users can configure as one 192-channel analyzer or four independent units. Synchronous analysis of 50 MHz and asynchronous analysis of 100 MHz are possible with 4- or 16-kbit/channel memory. Triggering capability includes 12 levels, with 15 pattern and two range recognizers. And users can avoid programming complex statements across an array of levels by writing a Boolean trigger statement in one level.

To uncover a particularly tricky timing problem, designers may require more than the 1-bit resolution of a logic analyzer. But reprobing can be time-consuming if only a typical two-channel oscilloscope is available. Consequently, Outlook Technology Inc. introduced its model 1600 Logic/Oscilloscope. The system's mainframe offers a 200-MHz synchronous or asynchronous sample rate for logic analysis on each of 16 channels. Every channel can also be used in the scope mode, with a 100-Msample/s sampling rate and 4-bit resolution in the one-shot mode, or 6-bit resolution in the repetitive mode (ELECTRONIC DESIGN, *April 26, p. 57)*. With a full complement of nine expansion modules, the system supplies 160 channels of logic analysis and scope capability. Users can store setups or data on the standard 3.5-in floppy drive. An optional hard drive is also available.

A unique instrument is the OmniLab II from Orion Instruments Inc. In addition to a 48-channel logic analyzer, the OmniLab holds a 2-channel digital oscilloscope, an arbitrary-analog-waveform function generator, a 24-channel digital stimulus generator, and a 500-MHz frequency counter. The basic system comes with 4 kbits of trace memory and 4 kbits of stimulus memory.

The logic analyzer handles state analysis to 34 MHz and timing analysis to 204 MHz. Orion's Mixed A/D Triggering system examines all analog and digital inputs simultaneously to help capture rarely occurring events or mixed-mode problems. And designers can use the logic-analyzer criteria, such as time qualification and pass counters, to describe analog waveforms for capture by the scope. Test setups are programmed with a mouse to adjust settings shown on the screen. With the OmniMacros programming function, users can arrange the setups into an automated test sequence.□

How Valuable?	Circle
Highly	541
Moderately	542
Slightly	543

TEXAS INSTRUMENTS

A PERSPECTIVE ON DESIGN ISSUES:

Creating systems with an analog edge

IN THE ERA OF

MegaChip

TECHNOLOGIES

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Challenge: Design a compact, cost-efficient direct broadcast satellite TV descrambler for consumer use.
Solution: TI's TLC5602 8-bit Video DAC. Our LinEPIC™ process combines one-micron CMOS with precision analog to satisfy the demands of the application for video speeds and low-power operation.

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Challenge: Build a modem for high-speed data transmission between computers; allow flexible operation and minimize data errors.
Solution: Our TLC32040 Analog Interface Circuit (AIC). A product of our Advanced LinCMOS process, the AIC combines programmable filtering, equalization, and 14-bit A/D and D/A converters with such digital functions as control circuitry, program registers, and a DSP interface.

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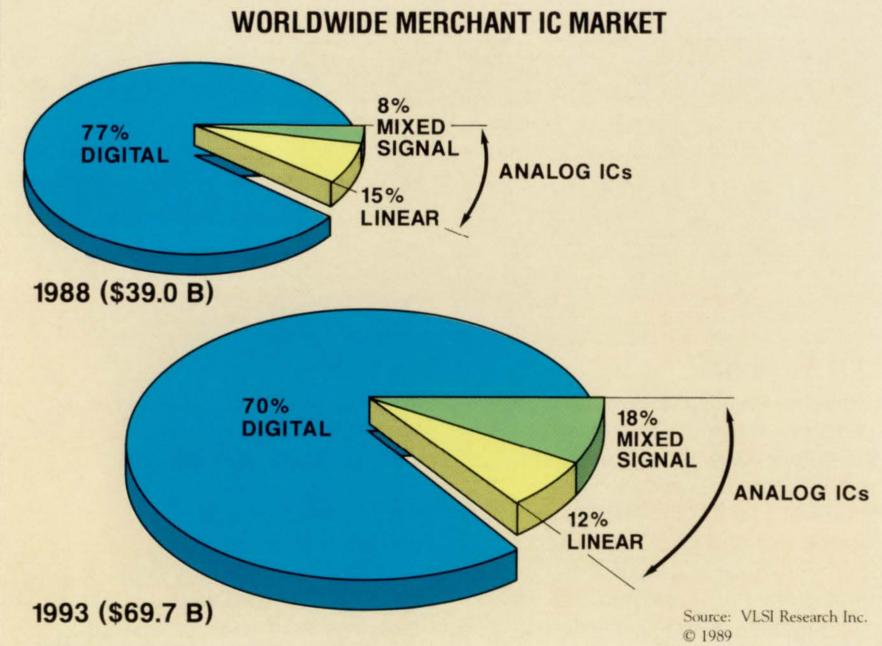
All of these examples point to one conclusion: TI's Advanced Linear functions are adding an analog edge to many system designs. They are contributing significantly to the enhanced system performance that marks a market winner.



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An increasing share of the total analog market is being captured by mixed-signal devices. As they gain more widespread acceptance, they are driving the expansion of the overall analog market (*see above*).

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TEXAS INSTRUMENTS

100-MHz Analyzer Card Boasts Deep Memory

John Novellino

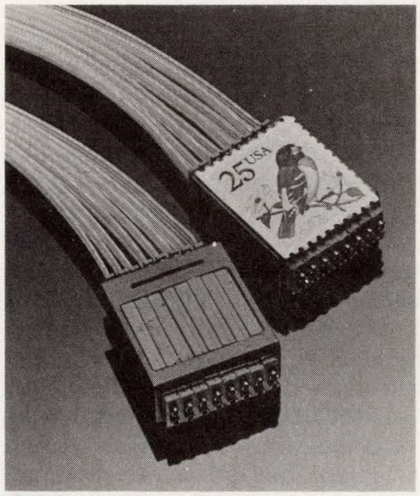
The rare baseball player who hits 40 home runs and steals 40 bases is known as a 40-40 man. An equivalent magic number in today's logic-analyzer field is 100. So it's natural that Tektronix named its newest analyzer, which hits that goal in five categories, the Centurion.

The Centurion, offered as a card for the DAS9200 digital-analysis system, features 100-MHz sampling, clocking, triggering, and time stamping on 100 channels (96 data and 4 clock). Channels can be multiplexed for asynchronous acquisition up to 400 MHz on 24 channels. Users can connect three cards in one DAS mainframe and as many as 16 cards with expansion units.

Introduced this month, the Centurion supports 10 32-bit RISC and CISC devices with microprocessor analysis packages: the AMD 29000; the Intel 80386, 80486, 80860, and 80960; the MIPS R3000; and the Motorola 68020, 68030, 68040, and 88100. The modules include preprogrammed setups for clocking, channel names and groups, and symbol tables. A sample reference memory allows quick familiarization with processor-specific capabilities.

Tektronix says it can quickly add support for other devices as demand warrants. This ability is based on the Centurion's 16-state, 100-MHz state machine, which can accommodate new microprocessors without additional hardware or emulator pods. The state machine, which permits real-time tracking of bus activity, can be programmed to emulate the machine-state operation of complex buses and to properly place samples for processor monitoring.

To ensure real-time operation at the analyzer's full speed, the trigger must run at the same speed. Therefore, the Centurion has a 100-MHz trigger that can identify an event and make a trigger decision before the next event occurs. The trigger can operate at full speed across all channels. In addition, users can program the state-machine trigger from libraries or by defining their own events. Full symbolic triggering simplifies the definition of complex events. Trigger resources include 16 programmable states, 8 decisions per state, 8 events and actions per decision, and 17 action types.



THE CENTURION logic-analyzer probes can be used individually for isolated lines, or bundled together in groups of eight with a special clip for fast connection to wide buses.

The 8-kbit memory in the Centurion 92A96 should facilitate debugging (a 92A96D version stores 32 kbits). Because the root of a problem may occur long before its first visible symptom, users must trigger on the symptom, then look back on the acquired data. To supply sufficient memory economically, Tektronix developed an efficient way to interface the analyzer circuitry to commercial bulk memory. In traditional designs, performance demands require that the RAM be integrated onto the custom analyzer chips, an expensive proposition.

To squeeze 96 channels of 100-MHz analysis capability onto one card, Tektronix designed custom ICs. The company packed many functions onto each chip, so that most signal traffic is on-chip and chip-to-chip connections are minimal. This eliminated most of the timing and skew problems encountered when functions were split across several smaller devices.

With speeds as high as they are today, probe technology is critical to any measurement instrument. Vendors must counter lead capacitance to ensure signal fidelity. In the Centurion, Tektronix uses the same passive compensation technique found in the company's high-performance oscilloscopes. The probes incorporate a nichrome wire that creates a complex characteristic impedance. The result is a transmission-line quality connection from the probe tip to the analyzer's front end, which itself has a 200-MHz bandwidth.

Mechanical connections are also important in dense circuitry. Consequently, the company designed the probes to be used separately or in groups. Each probe can be connected individually to isolated lines, such as clocks and strobes.

Alternatively, a special clip enables designers to band eight probes together into a small package for easy connection to wide buses *(see the figure)*. The same probes can connect to a microprocessor bus for state analysis with disassembly, or to a fast asynchronous clock to look at bus timing.□

Price And Availabilty

Prices for the Centurion 92A96 start at $17,950, which includes one year of on-site support. Delivery is estimated at 6 weeks after receipt of an order. DAS 9200 mainframes start at $9970.

Tektronix Inc., Logic Analyzer Div., P.O. Box 12132, Portland, OR; (800) 245-2036. **CIRCLE 544**

How Valuable?	Circle
Highly	545
Moderately	546
Slightly	547

EASY-TO-USE ANALYZERS ELIMINATE DUAL-PROBING

JOHN NOVELLINO

Performance specifications don't always tell the whole story in test and measurement. Sometimes ease of use is as important in determining how fast and how well a task gets done. The Philips PM 3580 family of logic analyzers is one example. Because of their improved architecture and probe technology, even inexperienced users can have them up and running in less than 30 min., according to the John Fluke Manufacturing Co., which is introducing the analyzers in North America.

The family's performance is good enough to stand on its own. In the maximum configuration, they offer 96 channels of 50-MHz state analysis and 200-MHz timing analysis, with 2 kbits of memory per channel *(see the figure)*. But the key contribution made by the 3580 series is a dual-analyzer per pin architecture. Using only one set of probes, every channel can collect both state and timing information simultaneously.

This capability eliminates the need to either dual-probe a circuit under test or acquire two sets of data successively. It also cuts down on the total number of channels needed.

The other alternative, dual probing, is potentially unreliable and can load down the target system. The new low-capacitance passive and semi-passive probing adapters, however, hold loading to only 7 pF, even while recording both state and timing data. In most cases, the quick-connect adapters are matched to device-specific software disassemblers. In cases where clock timing requires an active adaptor (such as the 80386), Fluke can supply a separate adapter for timing information.

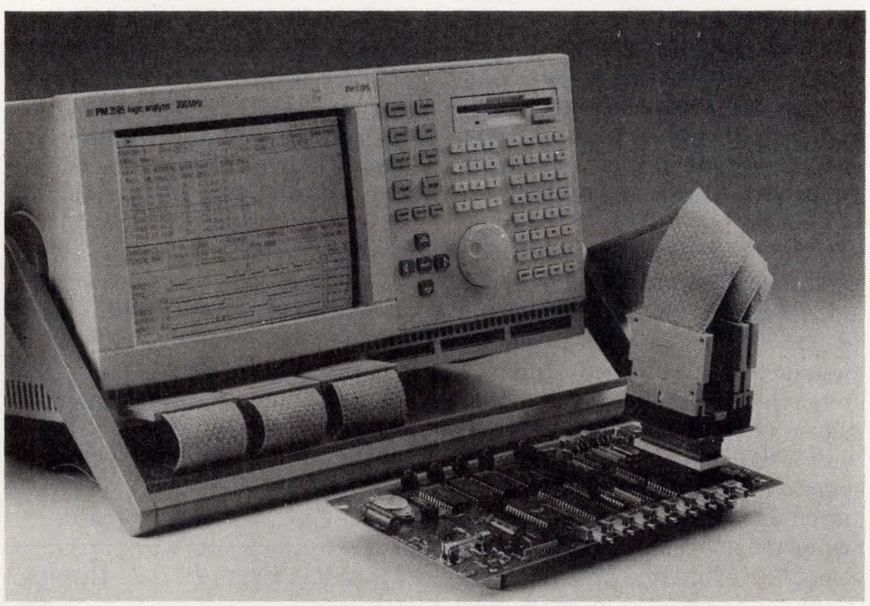
Pop-up menus and VGA graphics also make the analyzers easy to use even for inexperienced or occasional operators. But expert users can speed the process by taking one-letter short cuts. For instance, hitting "T" on the front-panel keyboard moves the cursor to the trigger point. The full alphanumeric keypad makes it easy to enter labels and values, and the large rotary dial speeds data scrolling or the positioning of the cursor.

The analyzers feature a fully integrated state and timing trigger sequencer that users can program with any combination of state and timing parameters, such as data patterns, bus ranges, edges, or glitches. As a result, designers can use a state sequence to define a trigger for a timing acquisition. Or a glitch can trigger the instrument, even if only state data is being collected.

When an external clock is defined, the memory splits between state and timing data automatically so that both can be stored. But users can configure the memory for either state or timing information. Therefore, the sequencer can use one type of data as a trigger to collect the other version.

A transitional timing scheme optimizes memory use during timing acquisitions. Rather than continuously collect data, the analyzers record the changes and time stamps indicating when they occurred.

Also, memory depth automatically adjusts for the speed of the recorded signals. For fast signals, transitional timing ensures at least the same recorded length as a conventional timing analyzer with the same memory size. For slower signals, the technique permits longer data acquisitions.□



ONE SET OF PROBES, attached with quick-connect adapters, acquires both state and timing data on the PM 3580-series logic analyzers. Users can display both sets of data on the widowed interface.

PRICE AND AVAILABILTY

Prices for the PM 3580 family range from $4250 for the PM 3580/30, with 32 channels of 50-MHz state and 100-MHz timing recording and a 1-kbit deep memory, to $10,950 for the PM 3585/90, which features 96 channels, 50-MHz state and 200-MHz timing analysis, and 2-kbits of memory.

John Fluke Mfg. Co. Inc., P.O. Box 9090, Everett, WA 98206-9090; (206) 347-6100.

CIRCLE 548

HOW VALUABLE?	CIRCLE
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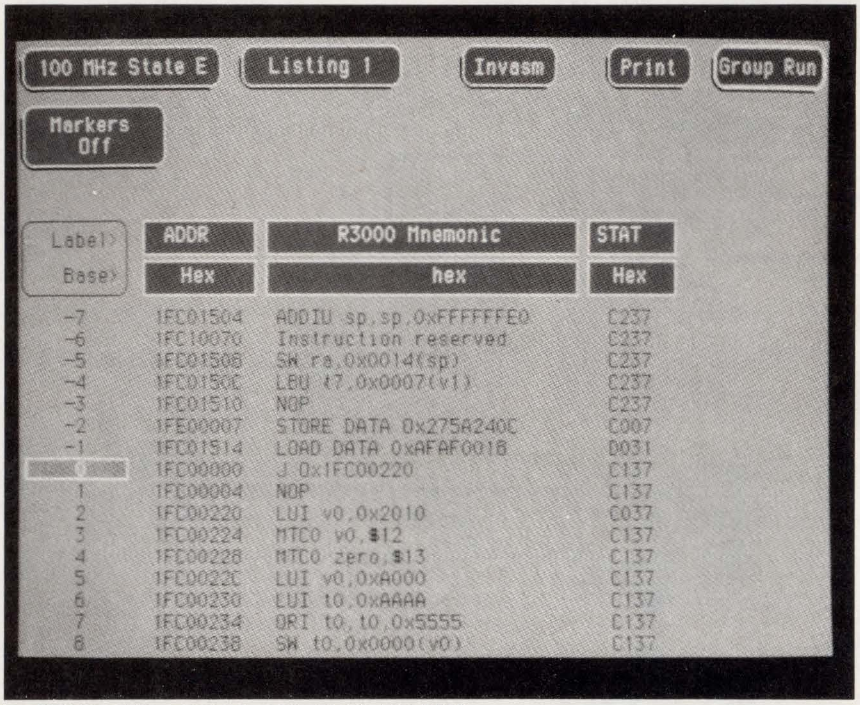
SLIGHTLY	551



THE HP 16540A OFFERS 100-MHz state analysis with microprocessor support for several RISC and high-performance CISC devices. Shown here is the disassembled code for the MIPS R3000.

100-MHz Card, Improved Interface Enhance Analyzer

John Novellino

Building on its successful HP 16500A-series logic-analysis products, Hewlett-Packard has introduced a 100-MHz state and timing module with full-speed triggering and adjustable setup and hold times. The company also improved the system's user interface.

The HP 16540A is the basic master card that supplies 16 channels of 100-MHz state and timing analysis. Up to four 48-channel HP 16541A expansion modules can also reside in the 16500A mainframe, offering a total of 208 channels. The 100-MHz speed is available across all channels, as is the full-speed (10-ns) triggering. The analyzer features a 4-kbit/channel memory with full-speed time or event tagging.

The ability to adjust setup and hold times (T_S and T_H, respectively) enables users to capture narrow windows of valid data. Three pairs of settings are possible: $T_S = 4$ ns and $T_H = 0$ ns; 2 ns and 2 ns, or 0 ns and 4 ns.

Interface enhancements include the ability to control the logic analyzer using the built-in color touchscreen, or through an optional mouse, trackball, or ASCII keyboard. The keyboard, for instance, speeds entry of labels and pattern-generator data. In addition, users can now scroll through data acquired by the optional 1-GHz timing module and 400-Msample/s digital-oscilloscope module.

The basic interface and software features are similar to those in the system's first-generation module, the HP 16510A. That unit offers 100-MHz timing analysis and 35-MHz state analysis.

Along with the two modules, HP is adding processor support interfaces for the latest RISC and high-performance CISC devices. The devices supported include the Intel 80386, 80486, 80860, 80960CA and KA; Motorola 68030, 68040, and 88100/88200; AMD 29000; and MIPS R3000 *(see the figure)*. The interfaces bring the number of microprocessors supported by the analyzer series to nearly 100.

The HP 16540A eases the debugging process with four trigger sequence levels. Before triggering, each level can be qualified with an occurrence counter (up to 65,535 times), store qualifier, and a branch to a previous level. A store qualifier follows the trigger level.

Trigger capabilities include four pattern recognizers, each an AND combination of bit patterns in each label. A range recognizer identifies data that's numerically on or between two specified patterns. The maximum size is 32 bits. The state trigger can also cross arm the 1-GHz timing module and digital scope module to look for glitches that may be causing a problem.

Two master clocks on the 16540A can clock in data lines on the module and on the 16541A. In addition, two slave clocks are available on each 16541A when operating in the multiphased mixed mode. Users can OR together clock edges to run simultaneously in the single-phase or multiphase mixed mode.□

Price And Availabilty

The 16-channel HP 16540A master card costs $7000, and the 48-channel HP 16541A expansion card goes for $8500. Delivery is within 16 weeks. The HP 16500A mainframe costs $7500. The new microprocessor interfaces range from $1200 to $2500, with estimated deliveries of 2 to 16 weeks.

Hewlett-Packard, Colorado Springs Div., P.O. Box 2197, Colorado Springs, CO 80907-2197; (800) 752-0900. **CIRCLE 552**

How Valuable?	Circle
Highly	553
Moderately	554
Slightly	555

ML4400 LOGIC ANALYZER

New! RISC, CISC and DSP Support

Arium announces three new features on their high-speed, modular ML4400

1 High-Speed RISC Support

- Fastest R3000 support available
- Supports the 88000
- Priced 60% below the competition
- User-modifiable disassemblers for R3000 and 88000 micros with full instruction mnemonic and data display
- Low-impedance, locally buffered connection to the R3000 and 88000 micros

2 High-Speed CISC Support

- Full hardware and software support available for the 68030, 80386, 80486 micros
- The only fully synchronizing disassemblers for these micros

3 Full DSP Support Software

- Disassembler support available
- Supports Motorola's 56000, Analog Devices' ADSP2100, and more
- Source code for disassembler provided; user can customize displays

The ML4400 Features:

- Synchronous channels: 160 @ 50 MHz, 64 @ 100 MHz
- Timestamped trace, data qualification
- Real-time performance analysis (histograms)
- 400 MHz on 16 ch., with 32K bits/ch. trace depth
- 100 MHz on 80 ch., with 8K bits/ch. trace depth
- Transitional timing, up to one billion virtual samples
- Trigger functions include AND, OR, NOT, RANGE, COUNT, TIME and GOTO
- User-defined disassembler

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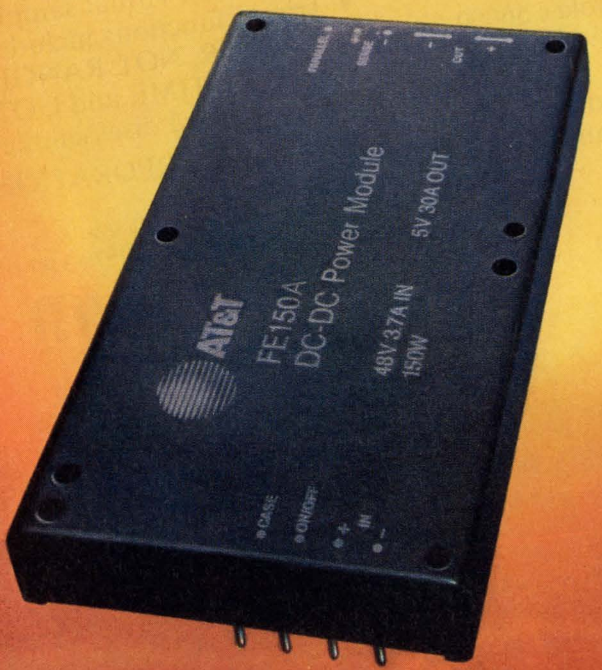

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CIRCLE 81

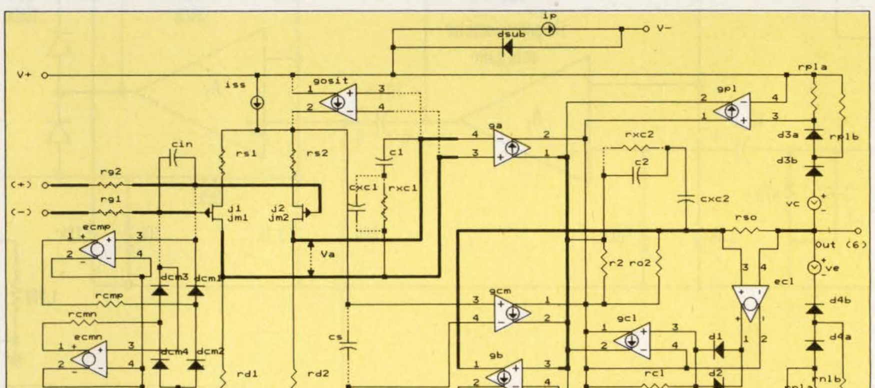
By Taking Into Account Effects Like Output Limiting And Asymmetrical Slew Rates, Spice Macromodels Perform As Actual Op Amps.

Models Can Mimic Behavior Of Real Op Amps

WALT JUNG
Linear Technology Corp.,
1630 McCarthy Blvd.,
Milpitas, CA 95035;
(408) 432-1900.

Op amp macromodels are, in a sense, much like actual parts. For example, a given op amp is good or bad for an application, depending on its usage. Logically, it can be expected that op-amp models successfully mimicking modern parts will contain a diversity of features, as do their real counterparts. But many don't. Rather, they're extremely generic and don't accurately depict such phenomena as current and voltage limiting, common-mode problems, phase-reversal, and asymmetrical slew rates. Yet the purpose of Spice simulations, which is to minimize, supplement, or corroborate breadboarding with accuracy, is pointless if the models aren't accurate.

When transistor-level op-amp models are used, the memory usage and simulation time required quickly become impractical for anything but small



Notes:
Basic Boyle model equations:
SR = iss/c2 (or iee/c2) (See box on asymmetric SR)
Avd = (ga*r2)(gb*ro2)
GBP = 1/(2*pi*rd1*c2) or, 1/(2*pi*rcl*c2)
Notes for these adaptations (junction & PMOS FETs, bipolars).
JFET input clamping optional.
Output voltage/current limiting varies with device type.
JFET SR symmetry control optional (see box).
Phase/frequency extensions usable with any amplifier type.

1. THIS MODIFIED BOYLE **op-amp macromodel can represent IC op amps with virtually any differential transconductance stage on the input. As a result, it can be adapted for op amps with npn, pnp, JFET or MOSFET input stages.**

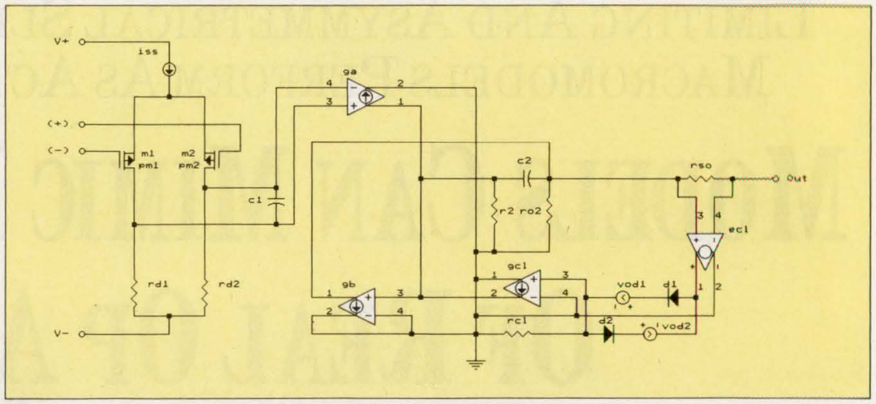
circuits. In contrast, using op-amp macromodels has the advantage of allowing memory use and simulation speed to become much more attractive, making larger circuits possible. In truth, the macromodel approach to Spice may be the only practical way for designers to simulate today's complex circuits in reasonable times. Otherwise, circuit size is limited by the inescapable bounds of memory and computer speed.

Though op-amp macromodels are hardly new, the most important thing to remember is their fundamental objective—to beat the simulation memory/speed limits. If they don't meet this, they're virtually useless. And, while IC op-amp designers have access to a full transistor-level model, most board and system users of op amps will likely never encounter it. Therefore, good op-amp macromodels are critical when using Spice in real-world designs.

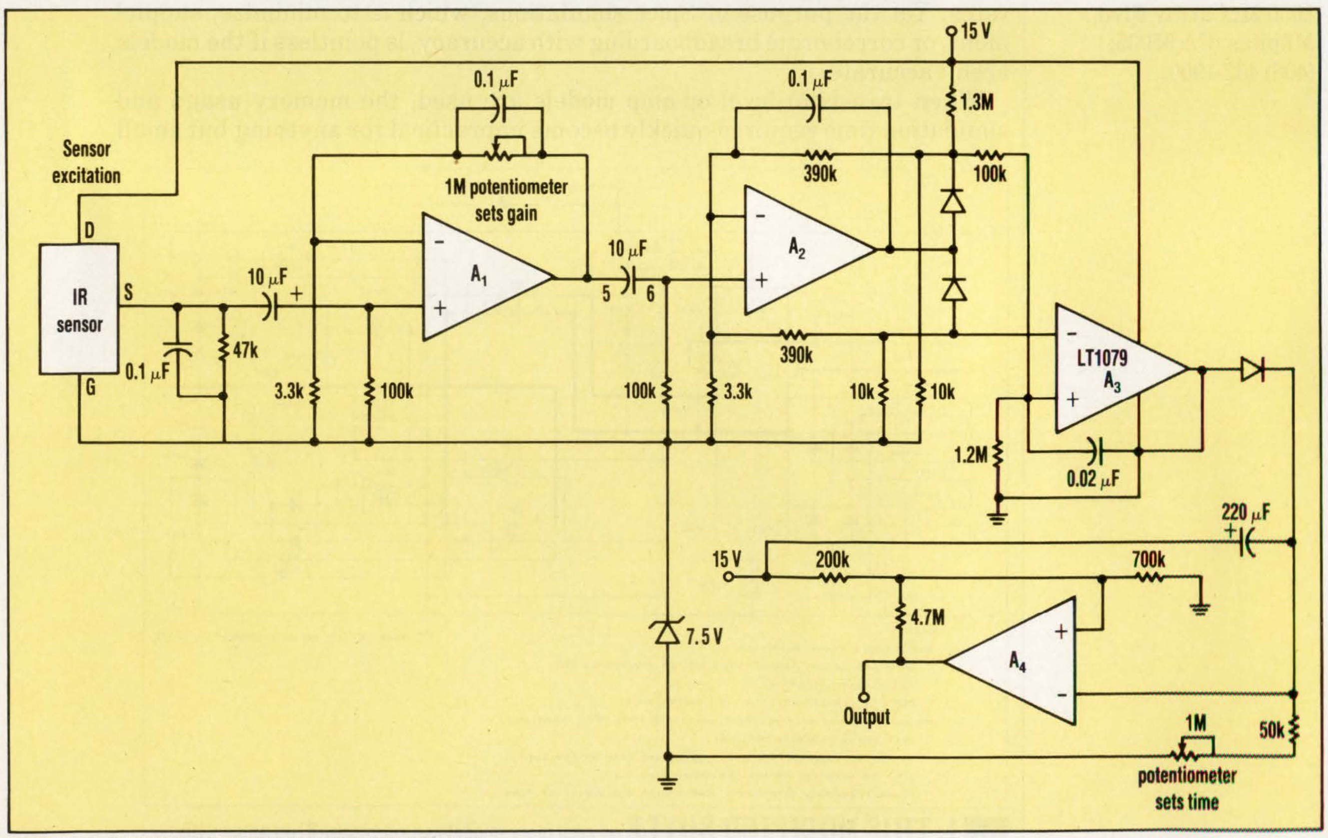
Internally, a macromodel achieves efficiency by using elements inherent to Spice. For active gain, this means using "ideal controlled source" stages instead of transistors, a few passive resistors and capacitors, and generally minimum use of p-n junctions. Four basic "controlled sources" dominate most op-amp macromodels: the voltage-controlled voltage-source (VCVS), the voltage-controlled current-source (VCCS), the current-controlled current-source (CCCS), and the current-controlled voltage-source (CCVS).

Typically, a macromodel will have two transistors at the input to realistically simulate most input parameters. Depending on model complexity, macromodeling can show useful reductions in simulation time and memory usage.

Macromodeling got its start about



2. THIS SIMPLIFIED PMOS-INPUT-STAGE op-amp macromodel provides accurate simulation of op amps with dissimiliar output current sink-to-source ratios.



3. A MOTION DETECTOR CIRCUIT using an IR sensor and a quad micropower single-supply op amp (an LTC1079) can be simulated with a macromodel that accurately represents the op amp. The amp can put out 15 mA, yet it draws just 45 μA from a single supply.

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REAL OP-AMP MACROMODELS CAN SLEW ASYMMETRICALLY

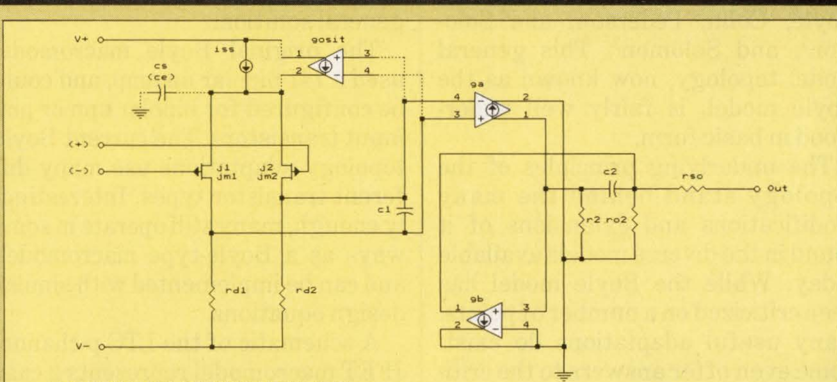
Many popular p-channel, JFET-input op amps like the 1974-vintage 355/356 types intrinsically slew twice as fast for negative-going outputs swings. Similar comments apply to the OP-15 and OP-16 clones. The slew rate (SR) specified on the data sheet typically was the lower of the two rates, the positive.

Most JFET macromodels available simply don't address the asymmetric slew rate at all. Others have seldom modeled it accurately. Slew-rate control was built into the original Boyle model, and it addresses asymmetry for common-mode signals by means of capacitor ce (or cs for JFET amps). However, this approach leaves something to be desired, because the slopes produced are inconsistent. LTC has implemented a new means of modeling slew rate asymmetry *(upper figure)*.

This circuit represents a much simplified Boyle-type model with p-channel JFET input devices j1 and j2. In typical usage, the slew rate is simply iss/c2, which is symmetrical when cs is zero. When the common source capacitor cs is added, the slew rate for common-mode signals can be adapted (ce, as is noted in the Boyle paper). Unfortunately, this strategy works best when dealing with common-mode inputs, and not as well with inverting inputs.

LTC models asymmetrical slew rates by adding a VCCS, designated "gosit" (shown dotted), which dynamically modifies the total tail current available to j1/j2. This source is driven by the differential output of j1/j2 and produces a current which adds to, or subtracts from, the fixed current iss. Consequently, the resulting current available to charge or discharge compensation capacitor c2 is higher for one slewing slope than for its opposite. This holds regardless of whether the amplifier operates in the inverting or noninverting mode. As an option, cs (also shown dotted) can still be used for further slew control of common-mode inputs.

When generating a macromodel with asymmetrical slew rates, the lower of the two slew rates is taken from the data sheet, in addition to the ratio of the high-to-low slew rates. Algorithms in the program then calculate an appropriate static value for iss and the gain of the VCCS "gosit." This is so that a proper slewing characteristic is produced by the model. Noninverting-mode Spice waveforms of an LT1056 op amp and those produced by an actual device clearly depict asymmetrical slewing *(lower figure a and b, respectively)*.

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Key equations for asymmetric slewing model
  Parameters input:
   a) LSR = data sheet SR (lower of two)
   b) DSR = ratio of high/low SR (typ. 2/1)

   for a 1056 type amplifier (356 topology),
   LSR = 14v/us, DSR = 2,
   HSR = higher of two SR = DSR * LSR
       = 2 * 14v/us = 28v/us
   ISR = intermediate SR
       = 4/3 * LSR
       = 18.67v/us
   iss = ISR * c2
       = 560uA with c2 = 30pF
   gosit = iss/2
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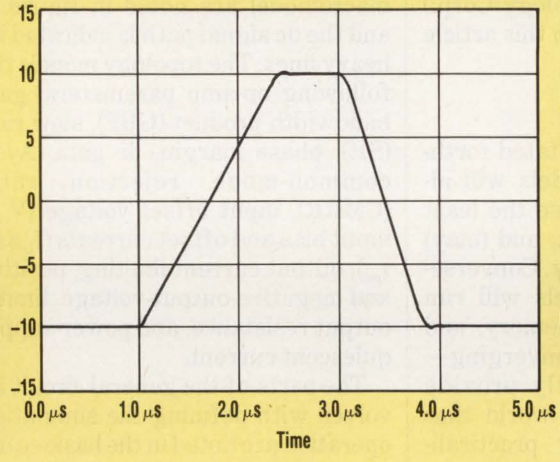
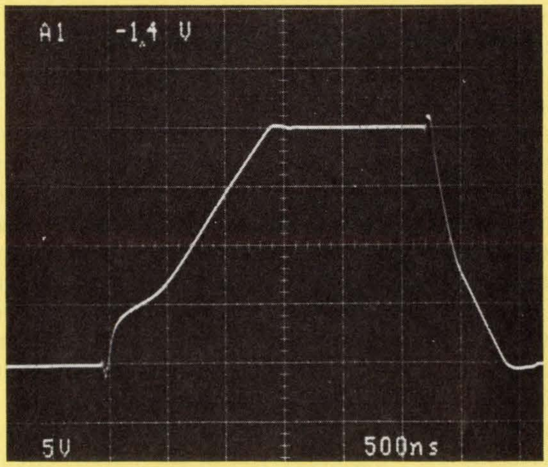


(a)



(b)

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15 years ago with seminal papers by Boyle, Cohn, Pederson, and Solomon[1], and Solomon[2]. This general model topology, now known as the Boyle model, is fairly well understood in basic form.

The underlying principles of the topology stand behind the many modifications and extensions of it found in the diverse models available today. While the Boyle model has been criticized on a number of points, many useful adaptations do exist. Some even offer answers to the criticisms.

Spice modeling in general and macromodels in particular have certain "facts of life" which sooner or later become evident. For example, it's a non-negotiable truth that more complex models (whether based on the Boyle topology or not) must obey certain simulation trade-off rules. The LTC (Linear Technology Corp.) models to be discussed in this article are no exception.

MODEL TRADE-OFFS

Several rules can be stated forthright: Simple macromodels will always run the fastest, use the least overhead, converge fast, and (may) produce modest accuracy. Conversely, more complex models will run slower, use the most memory, and may have difficulty converging—but they can ultimately provide greater accuracy. In a world that deals with engineering practicalities, we designers must always be aware of these factors.

If the modeling process is carried to an extreme, it's possible to produce a very complex macromodel that offers little or no speed and/or overhead advantages over a transistor-level model for the same circuit. Worse yet, it may never find a bias point in large- or medium-sized circuits (even when the Spice defaults are "tweaked"). At this stage, the obvious question becomes "What's the point of such a macromodel?" If we ignore these factors, it can lead to complex models which simply don't perform as needed. Because of such simulation issues, overly-complex models (which can actually supply very fine emulation in certain areas) may never turn out to be a totally general solution.

The original Boyle macromodel used a 741 bipolar op amp, and could be configured for bipolar npn or pnp input transistors. The current Boyle topology adaptations use many different transistor types. Interestingly enough, many still operate in some ways as a Boyle-type macromodel, and can be implemented with similar design equations.

A schematic of the LTC p-channel JFET macromodel represents a case in point *(Fig. 1)*. This model behaves fundamentally as a Boyle type, but has a host of added enhancements (many are optional to the user). It's used as an example in the following discussions for the general Boyle topology, and as a departure point for other variations.

Key equations for a basic Boyle macromodel are noted in figure 1, and the dc signal path is indicated by heavy lines. The topology models the following op-amp parameters: gain bandwidth product (GBP), slew rate (SR), phase margin, dc gain (Avd), common-mode rejection ratio (CMRR), input offset voltage (V_{os}), input bias and offset currents (I_b and I_{os}), output current limiting, positive and negative-output-voltage limits, output resistance, and power-supply quiescent current.

The parts of the general circuit involved with defining the simulation operation are noted in the basic equations (lower left of figure 1). Some minor variations occur when input transistors change from junction to PMOS FET types, or to npn or pnp bipolar transistors. More op-amp-specific options involve details of voltage/current limiting and slew rate control, so these equations aren't shown *(see "Real op-amp models can slew asymmetrically," p. 73)*. This topology adapts well to different op amps. Devices using all of the transistor types mentioned can be used in the front end. Moreover, various options can be added for input clamping, differential or common-mode characteristics, limiting employed in the output circuit, and the complexity of phase-frequency compensation used.

To appreciate the Boyle model topology's flexibility in adapting and/or extending to other input transistor types, look no further than the j1/j2 input differential JFET pair (q1/q2 if bipolar, m1/m2 if MOS), which is set by the design parameters to operate at a differential gain of unity. This normalization step has the benefit of increasing the utility of the model when simplifying design expressions for slew rate and gain-bandwidth product. It can substitute other input devices within this architecture relatively easy.

MODEL FLEXIBILITY

Specifically, the input-stage gain-normalization step enables other structure variants to be implemented without major topology changes. As noted, the original paper allowed for bipolar pairs in the basic design equations. However, if this model is viewed more generally, a fundamental characteristic stands out—virtually any differentially operated transconductance pair can be used in the front end. From the point in the circuit Va (the differential outputs of j1/j2), the signal path through the model remains essentially the same and the basic design equations hold.

While JFETs j1/j2 are shown at the input here, other variations have provisions for transconductance adjustments so that other transistor types also operate at unity gain with suitable biasing. As a result, this concept allows many variations of the original Boyle model to exist. The design equations in the figure dictate the overall model performance. It can be extended to include all of the transistor types mentioned. To create a model for an op amp with different input-transistor types, Spice transistor model-parameters q1/q2 or m1/m2 replace j1/j2. The transistor-model parameters of these devices then determine the amplifier's V_{os}, I_b, and I_{os}.

Though this input-stage gain normalization step makes the input flexible, it does insert a trade-off. This occurs because the input transistors operate at currents and gain levels unlike that used in an actual op-amp circuit. As a result, input noise per-

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formance of a Boyle model won't usually track a real part accurately. This factor isn't unique just to the Boyle model, but is true of other models with input-stage gain normalization.

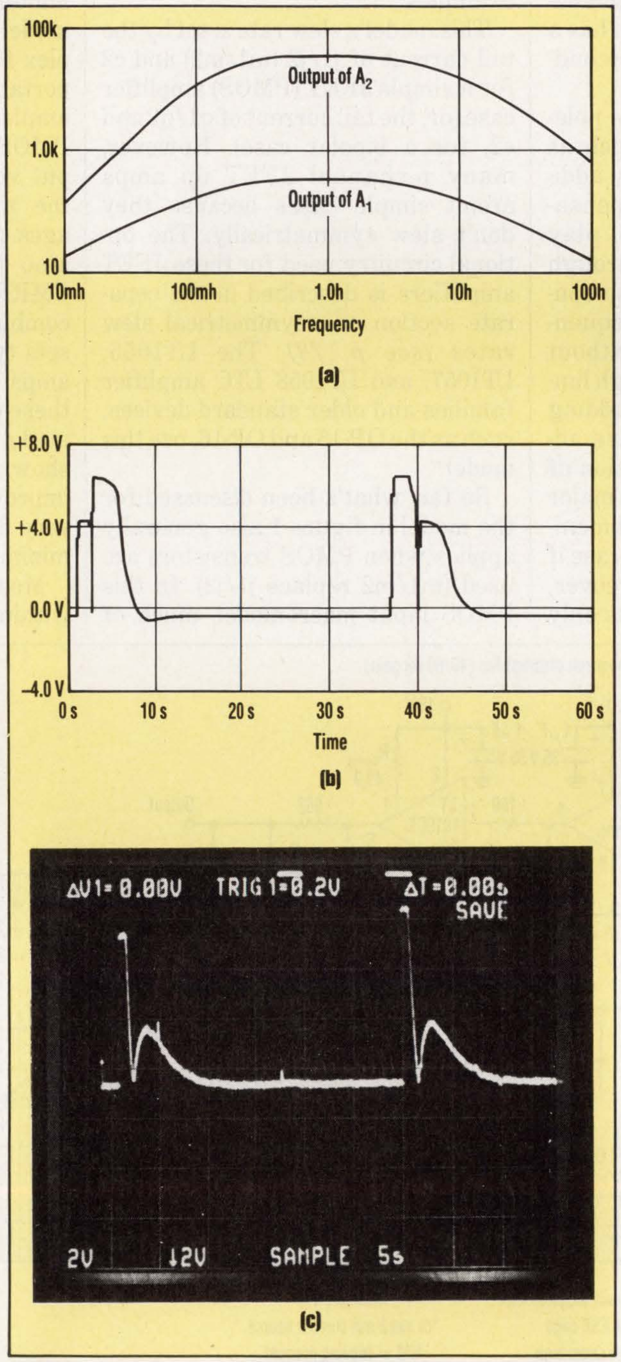
In the original Boyle model's output stage, voltage limiting is set by a diode and voltage source (brute force) hard-clamp to the rail for the positive limit (not shown). A similar diode and voltage source supplies a negative rail limit, and typically these limits are within a volt or two of their respective supply rails. This relatively simple limit scheme produces high internal currents approaching 100 A when limiting.

Current limiting of the original Boyle model is supplied by back-to-back diodes. They work in concert with controlled sources producing a buffered voltage drop proportional to load current (not shown). At high output currents, the diodes conduct and limit the output current. As with the voltage limiter, this is also a brute-force limit design, producing high currents in operation.

These limiting schemes have been improved in several regards within model upgrades, allowing more freedom for the limits and less interaction with the model's small signal performance. In the model shown, more complex voltage limiters are deployed, which may or may not be used for a given op-amp type. The diodes d3a, d3b, and controlled source (gpl) form a positive voltage limiter, while d4a, d4b, and gnl form a negative voltage limiter. The improved current limiter is described later.

The LTC approach to macromodel design aims toward practical macromodels that emulate the amplifiers in both specification and functionality while maintaining reasonable speed and accuracy. The Boyle macromodel was chosen to be built upon, enhancing it where appropriate, extending and redesigning it where necessary.

To generate new models, LTC uses a family of programs that implement four types of custom macromodels. Each op-amp input type, JFET, PMOS FET, npn, and pnp has an associated program. These produce new, unique, ready-to-run op-amp-specific macromodels from data-sheet specifications. With this approach, the company can quickly respond with new models, or to requests for custom values.



4. AN ULTRA-LOW-FREQUENCY analysis from the motion detector's input to amplifier outputs is easy on the simulator (a). A transient analysis under "alarm" conditions on a simulator (b) and on the bench (c) show similar results.

The use of junction and MOSFET transistor types in a macromodel input stage was described by Krajewska in an early Boyle model enhancement.[3] LTC's p-channel JFET model is fundamentally similar to Krajewska's, but with further adaptations added. With all its features active, this model is one of the more complex within the LTC library. It may appear overly busy, but seldom will all options be present at once. The following discussions highlight the various enhancements that go beyond the basic Boyle model.

The j1/j2 front end offers a number of possible options within the stage. Input capacitance is simulated by capacitor cin, and the buffered clamping network around dcm1-4 simulates the anti-phase-reversal, common-mode clamping of LTC JFET amplifiers (because this circuit isn't needed for all simulations, it comes "commented out" in the model file).

Transistors j1/j2 have model characteristics calculated to yield unity gain with gate currents consistent with the I_b and I_{os} of the amplifier modeled. The j1/j2 model parameters for V_{to} supplies V_{os}, and voltage source vcm2 simulates the negative common-mode characteristic of some JFET amplifiers. In general, these macromodels should act as a real op amp. For example, they contain a power consumption current source ip, as well as a reverse diode dsub that also models maximum

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supply voltage.

In the model's inner stages, gain and frequency response characteristics are set by ga, gb, r2, ro2, and c2. For a simple case, this essentially follows the Boyle equations. Capacitor c2 is used alone as the main compensation capacitor, while c1 is used alone across the input to ga to control phase margin. The system has a primary pole set by c2, and a secondary one set by c1.

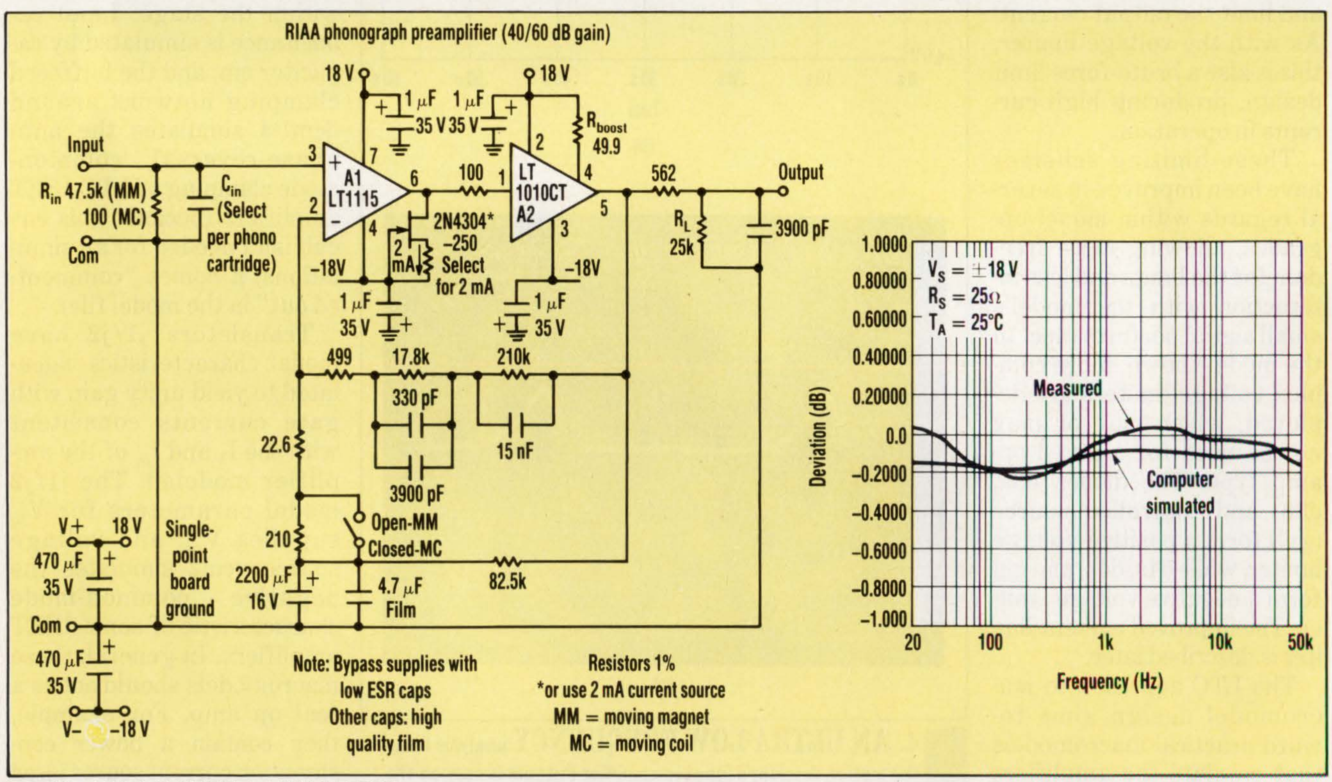
For amplifiers with multiple pole-zero compensation stages, such as the LT1007 and OP-27 families, additional phase-frequency compensation can be brought into play through rxc1 and cxc1, or through rxc2 and cxc2. Together, these controls enable more complex frequency responses to be simulated without additional active stages. Though limited in versatility relative to adding many gain stages, it does have advantages. It's a simple extension of the Boyle model and it adds no major penalty in simulation time and memory needs, which would be the case if active stages were added. Moreover, because this extension consists only of passive parts, optionally added to the internal main frequency control points of a Boyle-type model, it can be incorporated with any op amp in the families under discussion. The extension is used in the LT1007 and OP-27 models mentioned, as well as the LT1115 model illustrated in later examples.

This model's slew rate is set by the tail current of j1/j2 (m1/m2) and c2 for a simple JFET (PMOS) amplifier case (or, the tail current of q1/q2 and c2, for a bipolar case). However, many p-channel JFET op amps aren't simple cases because they don't slew symmetrically. The optional circuitry used for these JFET amplifiers is described in the separate section on asymmetrical slew rates *(see p. 73)*. The LT1056, LT1057, and LT1058 LTC amplifier families and older standard devices, such as the OP-15 and OP-16, use this model.

So far, what's been discussed for the model in figure 1 also generally applies when PMOS transistors are used (m1/m2 replace j1/j2). In this PMOS input macromodel, much of the rest of the overall model is similar, and there are few changes in the FET equations. The PMOS-input-stage model easily handles such useful device categories as the low I_b, low V_{os} chopper-stabilized units as well as single-supply CMOS devices.

The output current and voltage limiters used with the LTC PMOS model are usually of the more complex form shown, due to several important performance issues. For example, amplifiers emulated by these PMOS models have rail-to-rail output voltage swings combined with the millivolt-level saturation voltages typical of CMOS outputs. They also have gains of 160 dB and CMRRs of 140 dB. Moreover, that's combined with the sub-microvolt offsets typical of chopper-stabilized op amps. The ability to handle many of these performance characteristics is made possible by model features shown in the figure. These include improved voltage limiters supplying very low saturation voltages with minimal gain error.

Most current-limit schemes used within op-amp macromodels sink and



5. AN AC SPICE ANALYSIS of an RIAA preamplifier, using a macromodel of the LT1115 op amp, agrees to within 0.1 dB when compared with a frequency-response plot run in the lab.

source output current symmetrically. This typically isn't a problem, because most real op amps also have symmetrical limits. However, some types don't limit symmetrically at all. Their sinking and sourcing current levels may differ by a factor of 3 to 5. For example, some CMOS amplifiers have common drain outputs, and the lower n-type device can sink more current than the upper p-device can source. For example, the LTC1050—a chopper-stabilized op amp with a CMOS output stage—can only source 5 mA of current, yet it sinks 20 mA.

LTC implemented an improved technique to model current limiting, one that can also incorporate different degrees of asymmetry. A much simplified PMOS input stage macromodel shows how it's done *(Fig. 2)*. In this circuit, output current is sampled by a low-value series resistor, rso, which is typically 1 Ω. The current, proportional to the voltage drop across rso, is scaled up by the VCVS ecl. This eliminates any possible effects of the limiting loading the output and thus reducing gain. The technique was developed to remove the loading effects of brute-force limiting. The brute-force approach can cause gain errors in a very-high-gain amplifier, such as the chopper-stabilized LTC1050. In general, any op amp modeled with a gain of more than 120 dB can be subject to limiter-related loading errors. In chopper-type amplifiers, where gains are typically 160 dB or more, the effects of brute-force limiting can cause significant errors.

Selecting the value of rso, the gain of ecl, the diodes d1-d2 and voltage sources vod1-vod2 provide plus and minus current-limit thresholds. The gain of ecl is common for both plus and minus current limits, and the voltage of the two voltage sources is adjusted to reflect the desired sinking and sourcing thresholds (for equal current limits, the diodes are the same and the voltage sources are dropped). When an output current limit occurs, a predetermined voltage appears across rcl. The overall-current-limiting feedback loop is then balanced in defining the output current limit, with VCCS (gcl) absorbing the current from the main signal path through the VCCS (ga).

A somewhat more subtle advantage of this limiter is its freedom from large internal currents in limit, unlike brute-force limiters. Although it's shown in the context of the LTC1050 PMOS chopper-stabilized op amp, the limiter is also quite adaptable. Variations of it appear in a number of other LTC macromodels, including those mentioned along with the JFET families and many of the npn bipolar types.

Not all IC vendors have taken these steps in modeling PMOS input, CMOS output op amps. Inspecting some models released reveal such obvious deficiencies as input transistors that are totally different from the part actually modeled, and lack of close attention to output limiting levels. Obviously, such a model can't simulate input or output common-mode ranges with a high degree of fidelity. Nevertheless, these parameters can be critical in single-supply operation. For example, what engineer would trust a model simulation that depicts amplifier output swing going negative at limit when only a positive power supply is used? Some models do just that.

PNP MACROMODELS

The pnp-input-transistor macromodel behaves very similar to the Boyle-derived, enhanced-FET models (just described), with pnp transistors replacing j1/j2. However, other practical differences exist due to the functional characteristics of the amplifiers that it models. These differences are the thrust of the enhancements for the pnp-input models.

To start, pnp-input op amps are often designed for single-supply and/or micropower applications. For these applications, common-mode input and output ranges are crucial. Obviously, a good model should reflect what the real parts do for meaningful simulations. More than just the basic dc gain and frequency response should be considered. For example, models should take into account common-mode input voltages to ground (or slightly below it), like the actual parts will see when they're in the circuit. Similarly, common-mode transients should be clamped as in the real parts. The pnp model addresses these additional points brought on by micropower and single-supply applications.

LTC single-supply op amps have a unique, common feature—input-phase-reversal protection using a common-mode clamp network. In the macromodel, common-mode diodes referenced to a voltage (vcmc) clamp voltages applied to the input pair. Though not shown, this is similar to the buffered clamp network of the first model discussed *(Fig. 1, again)*. Using this clamping in the models is optional, but when present, it allows linear common-mode response to a few hundred mV below ground with no phase reversal, just like the actual parts behave.[4]

Though not depicted in figure 1, an extra output network enhances small-signal saturation behavior while still allowing full short-circuit currents. This represents another important feature of the pnp model that's also specific to micropower devices. It comes into play in the LT1078 and LT1178 series devices. For this type of amplifier, one of the more difficult aspects of model performance lies in simulating the supply-rail saturation voltage while still retaining the effects of micropower current drain coupled with high maximum output current. For example, in the case of the LT1078, the typical supply current is only 45 μA and output resistance is a few kilohms, but it can deliver ±15 mA to a load. The output network makes it possible to model concurrent micropower small-signal characteristics and high maximum current. The LTC LT1013/LT1014/LT1006 and related micropower pnp-input op-amp families use this model.

NPN MACROMODELS

The npn macromodel schematic is also similar, with of course, npn transistors replacing the JFETs *(Fig. 1, again)*. As with other amplifier models, there are many part-specific details the npn model can handle, depending upon the specific op amp be-

ACCURATE, DEVICE-SPECIFIC, IC OP-AMP MACROMODELS

ing modeled.

Precision npn input op amps often use differential-input clamp diodes. For example, the LT1001 and OP-07 family models have back-to-back clamp diodes, series resistors, and the input capacitance cin. Others have various clamping-resistance combinations. Most op amps today are compensated internally, yet the LTC models also handle externally compensated units. For instance, with the LM108 family of amplifiers, compensation capacitor c2 is outside the model.

The extended phase-frequency combinations discussed previously come to play within a number of npn-input, op-amp types, such as the LT1007/LT1037, the OP27/37, the LT1028 and LT1115, and the LT118 series. Most of these also use the improved voltage-current limiters shown in the first model discussed. Others, like the LT1012, LT1097, and OP-97, use a classic Boyle method of current limiting.[5]

It may or may not be obvious, but the enhancements added to the various models are generally "removable." In other words, these moderately complex models aren't cast in concrete. Examples include the anti-phase-reversal clamp and the differential clamps. For situations where these enhancements are not essential, the items can be commented out in the model file to enhance speed, lower memory requirements, and aid convergence.

Virtually all of the enhancements can be selectively disabled this way, either as a potential aid to troubleshooting, or simply to enable a "turbo" mode. However, while this is possible, it's not recommended unless the different ramifications are understood, and in no case should model tweaking be attempted by the inexperienced.[6]

Readers should note that a given macromodel available from a vendor may or may not model all of the device parameters listed. For example, V_{os} and I_{os} can often be skipped, simplifying a model's front end to just one transistor model for both j1/j2 (or q1/q2 for bipolar, m1/m2 for MOS). With V_{os} and I_{os} modeled, appropriately different transistor models are used, as opposed to one common transistor. The latter approach is an example of trading off simplicity (and a slightly faster speed) against the loss of several rather key performance parameters.

MODELS AT WORK

The "proof of the macromodel pudding" lies in how well they achieve the tasks intended. In this section, two circuits are both simulated and lab tested. The examples are chosen to bring out some of the modeling issues discussed.

The first example circuit is a motion detector. It uses a single-supply op amp, the LT1079 quad micropower device *(Fig. 3)*. The detector has the general design objectives of low power consumption from a single battery. Consequently, the LT1079 with a standby drain of 45 μA/amplifier is a good choice.

The circuit operates with an IR detector placed in a field illuminated by an IR source. When motion within the field occurs, the sensor produces an ac output. This signal is amplified, detected, and stretched to trigger an alarm. The circuit consists of a two-stage bandpass amplifier (A_1 and A_2) with variable gain and an absolute value detector (also A_2). These are followed by a threshold comparator (A_3) and a resettable timer (A_4).

The circuit was simulated for both ac and transient analysis, using the LT1079 model. Spice ac analysis makes it easy to check gain vs. frequency, even down to 0.01 Hz. This is a difficult and time-consuming task in the lab. The ac Spice analysis of the circuit was run between the signal input and the outputs of both A_1 and A_2. In this case, the amplifier gain peaks between 0.1 and 10 Hz, as shown in the Spice plot *(Fig. 4a)*. Transient results from both Spice and the lab test show the composite operation of the system exercised with a 1-mV pulse input, which is detected as an "alarm" condition *(Figs. 4b and 4c)*.

This system was designed and tested on the simulator, and later verified in the lab. Only minor adjustments to address parasitic coupling issues were necessary in the lab. There were no convergence problems found in the simulation. Typical runs took 2-3 minutes on a MAC using PSpice.

An ac preamplifier with frequency-dependent gain was chosen for the second simulation example *(Fig. 5)*. In the past, when this was a popular method to accomplish Record Industry Association of America (RIAA) phono equalization, predictive analysis was very useful toward designs of this circuit type. Regardless of the dwindling popularity of LP records, this type of amplifier is still sufficient to illustrate the utility of Spice analysis.

The circuit employs frequency-dependent feedback around a very high quality amplifier gain block. With the appropriate choice of the network values and sufficient amplifier gain bandwidth, very close conformance to a standard RIAA curve can be attained. To correctly deemphasize the preequalized signal, three well-known time constants are required: 3180, 318, and 75 μs.[7]

In this circuit, four passive R-C components comprise the main RIAA equalization network as detailed on the LTC demo-diskette[8] and the LT1115 data sheet[9]. For the chosen gain of 40 dB, the network supplies accurate RIAA equalization with standard values. The active circuit consists of an LT1115 op amp with its output followed by an LT1010 unity gain IC buffer *(Fig. 5)*. The LT1115 model is from the LTC library, while a unity gain VCVS stands in for the LT1010.

In audio circuits of this type, relative errors on the order of $\pm$0.25 dB or less for frequency response are considered negligible. In figure 5, both the Spice and lab results show deviations less than this. The agreement between the lab and Spice results is mostly within $\pm$0.1dB.

This circuit was designed entirely on the simulator, and later verified in the lab. No problems exist with convergence. The simulation took 9.4 seconds on a 16-MHz 386 PC clone. Interested readers may try it for themselves with the LTC demo Spice macromodel diskette (available free

ACCURATE, IC OP-AMP MACROMODELS

from LTC literature request 1 (800) 637-5545). Any of the LTC application notes listed in the references can be obtained by calling that number.□

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Walter Jung, staff scientist at Linear Technology Corporation, specializes in application circuits and technology. A recognized authority on op amp applications, he's the author of the "IC Op Amp Cookbook," which is now in its third edition. Jung attended Drexel University, Philadelphia, Pa.

HOW VALUABLE?	CIRCLE
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MODERATELY	560
SLIGHTLY	561

CIRCLE 100

ELECTRONIC DESIGN QUICK LOOK

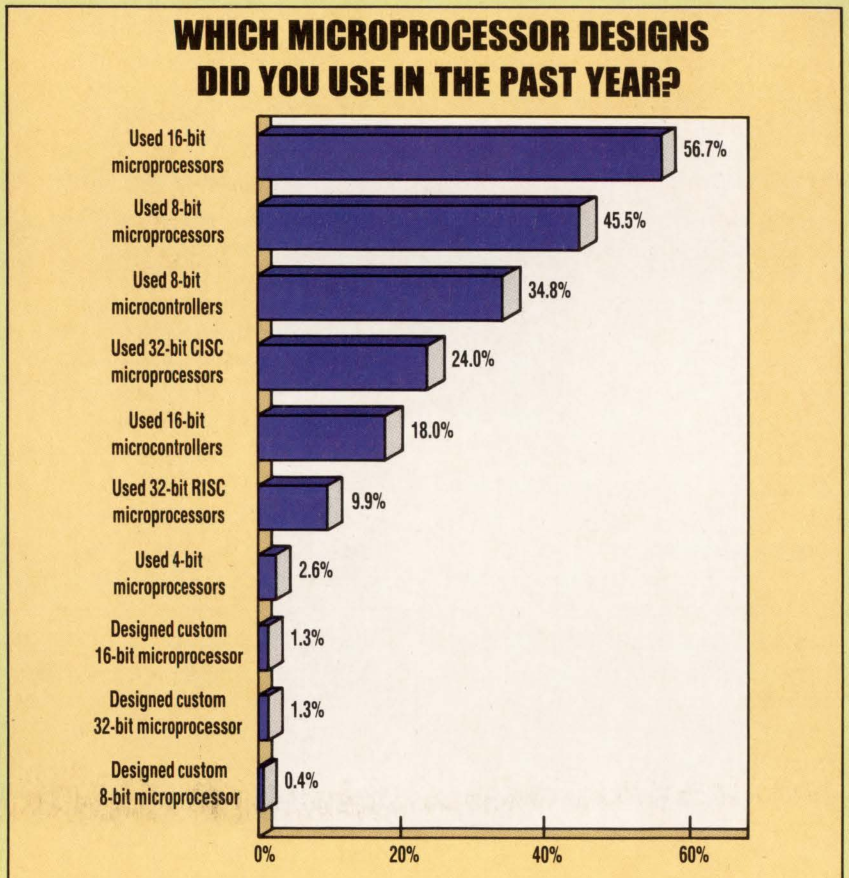
EDITED BY SHERRIE VAN TYLE

TIPS FOR ENTREPRENEURS

- Venture capitalists look at early stage companies, not early stage products. Don't focus on the merits of the product. Rather, show precisely what is needed to build a company to produce and market it.
- Set your marketing priorities early and research well, squeezing out risk at each stage.
- Clearly identify your customer base and profile it in detail in your business plan. To show existing support and shrink investment risk, share your product idea with potential customers and garner early endorsements.
- Seek the best support: a reputable industry consultant, respected accounting firm, and, if the product core is patentable, a top legal firm. Get them excited about your company so they can help you network with contacts in the financial community.
- Don't underestimate your competition for venture capital funds. Early stage funding is available but harder to get than in the past. Those who do the best homework may have the edge. Study the major players, their track records, and distribution channels.
- Watch your industry to be sure your product will be competitive in two years.
- A special product should be able to pull together an experienced team of senior marketing and salespeople. They are essential to engineers and designers. A business plan without them probably will lack credibility.
- Like packaging on a new product, how a business plan is written plays an important role in its acceptance. Consult expert sources who can help you do a professional job. Be sure the plan answers key risk parameters.
- Be creative in pursuing funding. Besides venture capital, consider aligning with strategic corporate partners, perhaps in a royalty relationship; check out Small Business Administration loans and boutique investment banking firms; or put together an investor group of friends and relatives.
- Don't lose hope. It's a long and difficult process where persistence pays.

by Alex Cilento, vice president of 321 Ventures, Newport Beach, Calif., which funds technology startups.

MICROPROCESSOR SURVEY



Source: survey of Electronic Design readers conducted by the Adams Co., Palo Alto, Calif.

Most design work still focuses on 16- and 8-bit applications. The next 12 months should bring big changes, though. More designers are working with 32-bit microprocessors as fewer focus on 8-bit-based projects. About one-third use 8-bit microcontrollers. These conclusions come from a recent survey of *Electronic Design* readers on microprocessor design and use.

Use of reduced-instruction-set computer (RISC) chips is growing sharply. About 10% of the designers polled currently use 32-bit RISC microprocessors. In the next 12 months, 20% plan to use 32-bit RISC processors. In comparison, 24% of the readers now use 32-bit complex-instruction-set computer (CISC) chips. And 32% expect to use CISC processors of 32 bits in the next year. In the next 12 months, about half the readers expect to use 16-bit CISC processors. And 19% expect to use 16-bit RISC processors.

Earlier this year, the Adams Co. mailed surveys to 1000 *Electronic Design* subscribers in the U. S., chosen at random. The Palo Alto, Calif.-based company received and tabulated the 406 responses.

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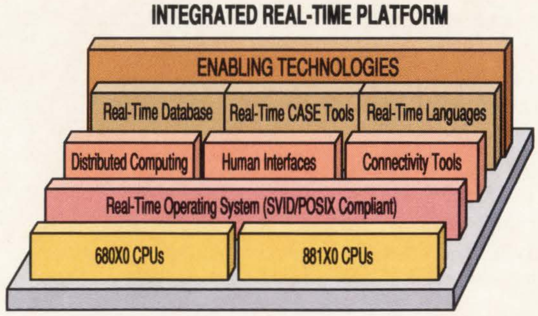

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IRAs: WHEN YOU CHANGE JOBS

Engineers are changing jobs more often these days. Career growth, company mergers, and defense cutbacks all play a part. On leaving a company with a 401(k) retirement plan, an employe receives a lump sum distribution of the vested amount.

Funds in retirement plans have been growing on a tax-deferrred basis. Taxes are postponed until funds are withdrawn. Once an engineer receives the lump sum, he can:

- **Pay taxes now.** He may be eligible to take advantage of certain favorable tax rates. Then he can use or reinvest the balance.
- **IRA rollover.** If he doesn't need the money immediately, he can deposit it into an IRA rollover account within 60 days of receiving the distribution. His retirement funds thus keep growing tax-deferred.
- **Partial IRA rollover.** He may elect to roll over part of the distribution into an IRA. He must pay income taxes on the amount kept, at ordinary rates.

If he decides to keep the entire distribution, his age and number of years he participated in his company's plan determines how the distribution is taxed.

- If he is more than 59 1/2 years old and participated in the plan for at least 5 years, he may elect favorable tax treatments known as 5- or 10- year income averaging. Income averaging calculates his tax liability as though his distribution were received in equal, yearly installments. As a result, the distribution may be taxed at a lower overall rate than if it was considered ordinary income.
- Those who receive less than $500,000 benefit most from 10-year averaging (1986 rates).
- If an engineer turned 50 before Jan. 1, 1986, participated in the plan for at least 5 years, but is still under 59 1/2, he can take advantage of 5- or 10- year averaging. But he is subject to an additional 10% penalty tax (unless he's taking early retirement at 55).
- If he wasn't 50 before Jan. 1, 1986, he must pay income tax *and* a 10% penalty tax.

An engineer can avoid all taxation and the penalty tax by rolling over the lump sum distribution into an IRA. He should weigh all his choices against his near- and long-term financial needs and goals and consult his tax and financial advisors.

by Henry Wiesel, a licensed financial consultant with Shearson Lehman Brothers, Shrewsbury, N. J. He is also a qualified pension coordinator. Comments and questions are invited c/o the editor.

OFFERS YOU CAN'T REFUSE

The X terminal market is a turbulent one. Vendors and product models enter and leave the market almost daily. Sorting out X products and players should get a bit easier, though. A free *Comparison Guide to X Terminals* is available from the X Business Group. The fall edition covers 90 products, monochrome and color, from 30 vendors.

The X Business Group, a market research and consulting company, focuses on X windowing systems, graphical user interfaces, and X terminals. For a copy of the guide, contact the X Business Group, 39791 Paseo Padre Parkway, Fremont, CA 94538; the telephone number is (415) 226-1075; the fax number is (415) 226-1094.

KMET'S KORNER

...Perspectives on Time-to-Market

BY RON KMETOVICZ
President, Time to Market Associates Inc.
Cupertino, Calif.; (408) 446-4458

I devote this column to a definition problem often called "creeping features." First off, it's unlikely that such features will ever be stopped—too many forces are at work to ensure their existence. But they can be brought under control.

At the intersection of the market information row and the product column of the Definition Matrix (Kmet's Korner, Sept. 13), the product development team is asked to agree upon *necessary* performance, *features*, cost, price, and timing.

A change in the product feature set is likely to influence the product's performance, cost, price, and timing. Change to the original definition should be produced only with close coupling and interaction between functional members of the team. R&D, marketing, and manufacturing must calibrate each other on what change is desired, why it is necessary, and what is possible within a given time reference. All participants need to compromise. Good business judgment must dominate. At times, certain team members have to really flex to make necessary changes a reality. At other times, the program progresses without altering the product's feature set. The team has to make difficult choices followed by rigorous work.

Using the external reference specification (ERS) as a control document exposes feature creep throughout new product development. Any change, regardless of size, should be presented to the entire matrix team so they can assess the affect it will have on their work. The program manager then collects team feedback to determine the possible impact in the marketplace. Based on the cost/benefit analysis, a decision is made. If change is viewed as desirable, the ERS is revised.

A cost/benefit analysis is easiest to produce on me-too-with-a-twist and next-generation product-development efforts. For these classifications, a fair amount of market knowledge is available. This makes it easier to assess the sales gains produced by the added feature. Market research techniques (sales research, structured surveys, focus groups, interviews, and so on) can be put to good use so that hte customer's desires are included in the decision-making process.

Cost/benefit analysis is difficult to do on first-of-a-kind and derivative development efforts that are targeted at new markets. These efforts are also the ones most subject to the creative instincts of those involved in coming up with new product and market concepts. Completing a Definition Matrix for these types of efforts is an important step forward to keep creeping changes visible and under control. Visionary people now have a product and process model that exists outside of the mind that they must physically modify. This action forces them to think through the cause-and-effect relationships of their actions. If the visionaries are prudent, they will do the mind work before they suggest changes in the product's feature set.

I don't advocate making feature change difficult for first-of-a-kind efforts. Sometimes it's very necessary. But those who advocate changes should be made fully aware of the implications of their actions.

1-MINUTE OPINIONS

What do you think about the education that young engineers are receiving these days?

As a 1987 BSEE, I feel that I have a good perspective on the current status of the engineering curriculum.

Post-secondary schools are getting an unfair portion of the blame for low-quality engineers. Much of current public elementary and secondary education consists of learning by rote. Students are not taught how to think, only to regurgitate the facts. Universities are the last stage of the educational process, and the most visible to employers, so most of the blame gets directed at them. If employers are worried about the continued supply of good engineers, I feel that, for now, they should be concentrating more on elementary and secondary schools than on universities.

Improvements can be still be made at the university level. The curriculum should be lengthened to five years, but not necessarily to cram in more technology. The courses that should be added are ones that address production and manufacturing concerns, concurrent engineering philosophies, and real-world scenarios for engineering business, instead of focusing strictly on design. Requiring internships for the engineering profession would also give young designers an introduction to the demands of an engineering career.

Finally, leave room for humanities courses. Bringing in real-world issues from outside the laboratory can help broaden students' perspectives, help them appreciate diversity, and encourage new and creative ways of thinking. **Brad R. Kelley**, *Albuquerque, N. M.*

Humanities courses must continue to play a role in engineering education. Granted, today's electronics engineer faces ever-challenging technologies; they are equaled by the world's ever-challenging social conditions. In short, things are tough all over.

All students must be aware of environmental issues, the alarming incidents of racial and cultural intolerance on North American campuses, the erosion of individual liberties in the U. S., and the importance of maintaining physical health to enhance mental performance. To these, add the importance of written and verbal communication skills in the workplace.

It's essential for graduating engineers to participate in the contemporary global climate that engineers previously helped to establish. **Craig Cullum**, *McFarland, Wis.*

The current level of learning upon graduation can be considered adequate. It would always be nice to learn more, but you must draw the line somewhere. When a young engineer graduates, he may have four years of student loans to reimburse. Adding an extra one or two years will strongly "demotivate" pursuing engineering when you can make as much money from business, commerce, or other fields.

The first use of an engineer is in low-level design and this is what the curriculum should provide for. Humanities and other ancillary courses may rather be more appropriate when going up into management (for example, group leader, and so forth) and should be provided by employers. Does the inverse stand? I don't believe that graduates of humanities are required to take engineering courses. That is also why too many managers do not have technical knowledge. Only the bottom line counts, and the Japanese corporations surpass the American ones.

In addition, too many employers treat engineers as disposable resources (i. e. do not allow technical upgrading during business hours). Engineers must often reinvent the wheel because of this and can make serious errors of omission while doing so, thereby exposing their employer to serious liabilities. By formal upgrading, learning from the mistakes of others also prevents the unnecessary stress associated with reinventing the wheel within an optimistic and management-imposed deadline.

Let me add another question: Should an engineer learn a second language to provide access to untranslated engineering knowledge (for example, Russian, Japanese, German, or French)? This could also ease access to foreign markets. **Alain Beaulieu**, *Ottawa, Ontario, Canada.*

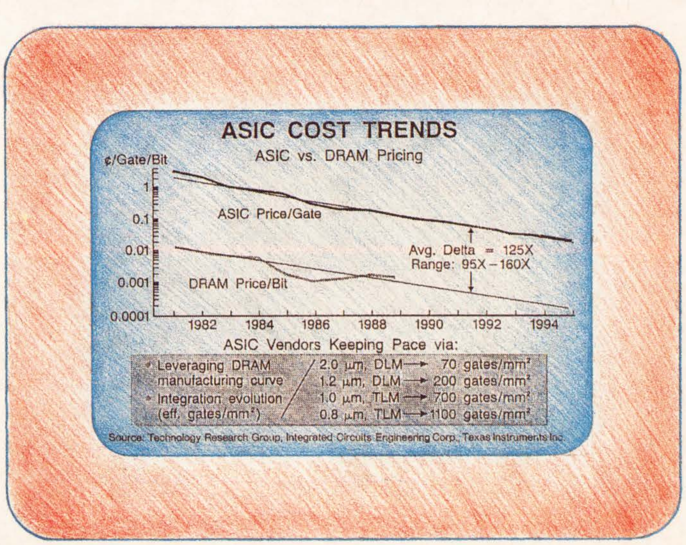
What's your opinion on the education of today's young engineers? Which areas are being under- or over-emphasized? What role should humanities courses play in engineering education? Are four years enough to give young engineers a good foundation? Send your opinions to our fax (201) 393-0637 or to Compuserve address 75410,3624. Or mail your responses to *Electronic Design*, Reader Opinions, 611 Route 46 W., Hasbrouck Heights, NJ 07604.

HOT PC PRODUCTS

Moving various shapes around on flowcharts can be a headache, whether the charts are drawn by hand or in software. To ease making these changes, Patton & Patton's Flow Charting 3 displays the object or area as it is moved to ensure precise placement.

Flowcharts can be imported and exported to other documents. Flow Charting 3 makes multipage charts and prints at 300 dots/in. on HP LaserJet laser printers and compatibles in normal, compressed, and ultracompressed modes. Version 3, an upgrade to II+, also has drivers for dot-matrix printers.

Besides a pop-up menu that has 35 predefined shapes, the program permits use of 200 shape sizes. Text can be displayed and printed in 10 styles, inside and outside of shapes. The program has a list price of $250; an upgrade from II+ costs $60. For more information, contact the company at 485 Cochrane Circle, Morgan Hill, CA 95037; (800) 525-0082, ext. 3366; fax (408) 778-9972.



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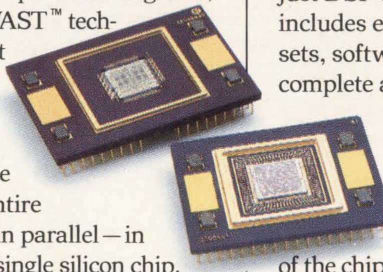

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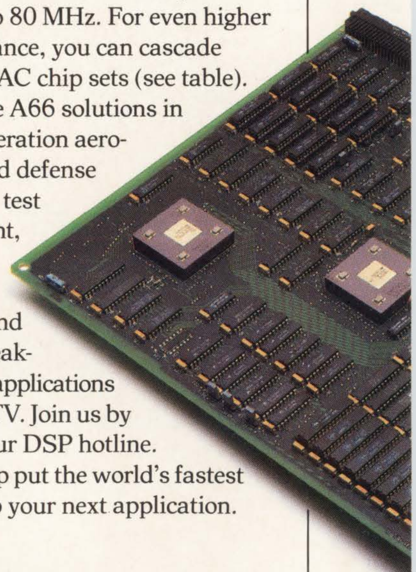

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CIRCLE 131

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PEASE PORRIDGE

What's All This Neatness Stuff, Anyhow?

Once upon a time, there was a rapidly converging conflict: My boss thought my office was getting messier and messier, and he wanted me to make it neater. Now, this was just a year or so after my desk had won a $500 prize for being the "Ugliest Desk in Northern California." So I guess he thought he was justified in pressuring me to clean up my act. He solved that problem by making it one of my goals to get my office to an acceptable (whatever that meant) level of neatness. Well, we never found out what that meant. Every time he would ask me how I was coming on the neatness campaign, I would tell him all of the other things I was doing to help our customers.

What if I came in on a Saturday with good intentions of neatening up some of my office, and the phone rang. Should I tell the customer, "No, I won't help you, I have more important things to do"?

BOB PEASE
OBTAINED A BSEE FROM MIT IN 1961 AND IS STAFF SCIENTIST AT NATIONAL SEMICONDUCTOR CORP., SANTA CLARA, CALIF.

So every year he would mark me down points in my review for not fulfilling my goals. He finally got so discouraged that he left the company. The poor guy. He just wasn't devious enough! He could have waited until the next earthquake and told one of the guys to knock over a couple of my piles of papers. Then he could then explain that I had to get it at least to a reasonable level of *safety*. But he never figured that out, and I didn't tell him until after he left.

Some people keep their desk neat because that's what feels good to them. I find that neatness is not a priority compared to a number of other things, such as answering the phone when a guy needs help, or volunteering advice when a customer has a problem. Some people find it easy to keep a neat desk because they throw out things that make it look messy. I just don't operate that way.

One time I was working on a Saturday after being at National just a few months. My desk was already stacked up pretty high. Another guy was at his desk, which had just a few dozen things on it. He was picking them up, one by one, studying them, and then throwing most of them in the wastebasket. I commented, "You sure do keep your desk neat." He said, "Yeah, if I find something I don't need, I throw it out." I said, "Doesn't your wife ever get nervous?" He replied, "It's my third wife...." No, I don't operate that way.

One day, an engineer stepped gingerly into the entry way of my office and asked, "Bob, do you have a Siliconix catalog?" I replied, "Sean. . . . you're standing on it." He looked down and, indeed, he was. He was impressed. But I knew right where it was, because I had recently tossed it over by the doorway so I could then put it in the bookcase by the door. Sean just happened to walk in before I put it in the bookcase.

More recently, I inherited a couple of filing cabinets and a huge 7 ft. × 3 ft. × 7 ft. cabinet from a Fairchild laboratory. Our secretary explained that I would have to junk it unless I could find a use for it. I said, "Well, I could always put it in my office." She looked at this huge ark and said, aghast, "No, you couldn't do *that*."

I thought about it. I got a yardstick, and I figured out that, with an

PEASE PORRIDGE

inch to spare, I *could* do that. My technician and I spent nearly all morning reassembling that cabinet and easing it into the corner of my office. I put about 1/3 of a million cubic inches of my paperwork into that, and into the other file cabinets, and improved the appearance of my office so much that our senior secretary admitted that I qualified for an "Enviros Award." In the past, the various departments would vie to achieve cleaner clean rooms and higher-yield fab lines by having better cleanliness. A whole department of 20 or 30 people would work real hard to cut down the number of particles in their area and win an Enviros Award. But I got my Enviros Award single-handedly. I hate to guess how many *particles* I straightened up.

Right now, my office seems to be in the getting-messier-again phase. When I have to review a mask set, with precision down to the last tenth of a micron, I get my head in the right mood to do that. And when I'm done, in sheer rebellion I guess, I abandon the neatness for a while. I save what seems to me to be of value. Often that includes documents and papers and notes that other people would think aren't very valuable—until they come to see me years later, hoping I might have the information they need. Often I do. Go ahead, call me *retentive*. See if I care.

Now that the NBS has changed its name to the "NIST" or "National Institute of Standards and Technology," I have figured out the next way to enhance the neatness of my office. I'm going to buy a big dresser with 6 big drawers and a mirror and everything. I'm going to put it right at the entrance of my office, and put our ultra-precision resistors and capacitors in those dresser drawers. And I'm going to call it "The National Bureau of Standards."

All for now. / Comments invited! / RAP / Robert A. Pease / Engineer

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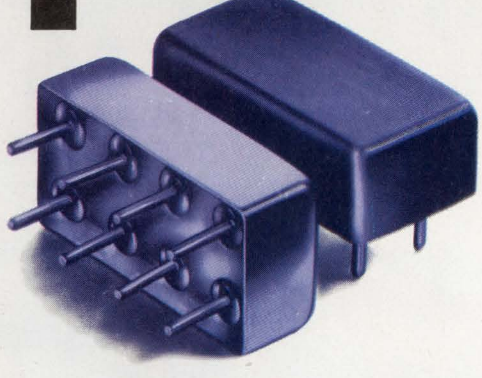

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MAN-1LN	0.5-500	28	1.0	8	2.8	60	15.95
◇MAN-1HLN	10-500	10	0.8	15	3.7	70	15.95
*MAN-1AD	5.500	16	0.5	6	7.2	85	24.95

††Midband $10f_L$ to $f_{u/2}$, ±0.5dB †1dB Gain Compression ◇Case Height 0.3 In.

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CIRCLE 126

C118 REV. E

CIRCLE 521

AMP STABILIZES WEIN BRIDGE OSCILLATOR

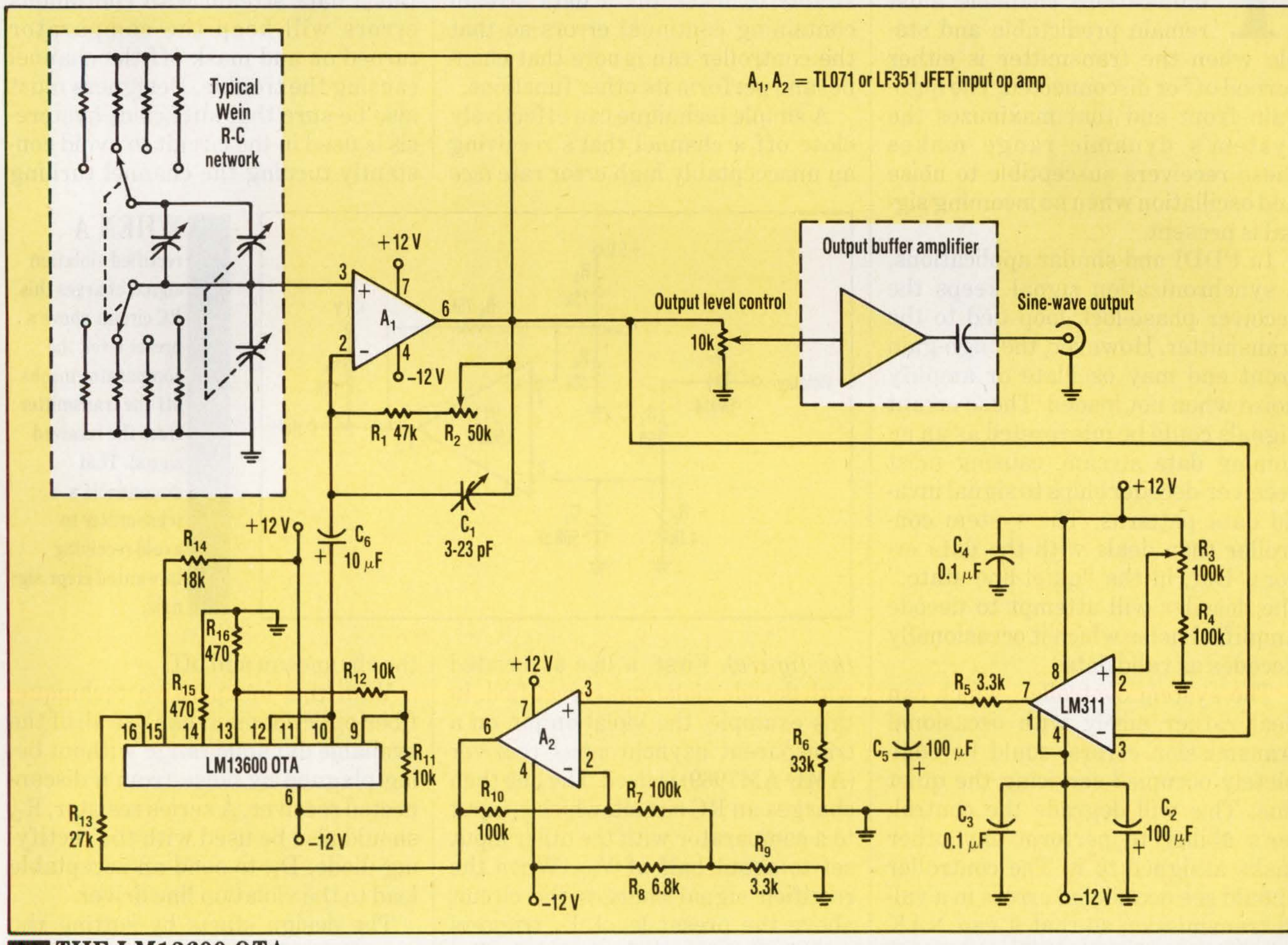
KARL TIPPLE
P.O. Box 181208, Dallas, TX 75218.

When making frequency-response measurements with a Wein Bridge oscillator-type audio-signal generator, it can be frustrating and time consuming to check and reset the generator output level after each frequency change. Unfortunately, many such signal generators using light bulbs or FETs as gain-control devices in the oscillator circuit suffer from fairly severe amplitude variations as the frequency is changed.

A circuit using an LM13600 operational transconductance amplifier (OTA) can stabilize the output level. The OTA is connected as a variable resistance in the oscillator circuit's negative feedback loop *(see the figure)*. The circuit operates with a maximum amplitude variation of about 0.1 dB over each decade in the 20-Hz to 20-kHz frequency range. This comes from combining the large dynamic resistance range represented by the OTA with the oscillator level-sensing scheme used. An additional 0.1 to 0.2 dB variation is evident up to a maximum operating frequency slightly above 100 kHz. The maximum operating frequency of the circuit shown is determined by the characteristics of the OTA.

The variable resistance represented by the OTA circuit is connected effectively between pin 3 of oscillator amp A_1 and ground, through C_6 and the OTA. This resistance, with R_1 and R_2, form a voltage divider that determines the gain of A_1.

The OTA circuit gets its control voltage from A_2. A_2 is biased so that the OTA represents a low resistance for oscillator startup. As the oscillator output rises to about 6 V pk-pk, the positive peaks of the sine wave begin to exceed the LM311 comparator threshold set by the voltage divider R_3 and R_4. As a result, the comparator output is switched low for a short time on each positive peak. This action prompts a negative dc voltage to develop across C_5, which alters the control voltage for the OTA, causing it to represent a higher resistance. The higher resistance re-



THE LM13600 OTA, connected as a variable resistance in the negative feedback loop of a Wein Bridge oscillator, stabilizes the output. This serves to eliminate amplitude variations as the frequency is changed.

duces the oscillator circuit's gain. At this point, any slight variation in the oscillator output's amplitude causes a significant change in the comparator's conduction low period. The resulting correction of the OTA control voltage supplies regulation to the oscillation amplitudes.

The R_6-C_5 time constant must be long enough to supply stable operation at the lowest desired oscillator frequency. The various values shown in the figure work down to 20 Hz. If a lower frequency limit is desired, say 10 Hz, it may be necessary to increase either R_6 or C_5. A longer-than-necessary time constant is undesirable because of the adverse effect on the circuit's recovery time after a frequency change.

Circuit adjustment should start in the 100-Hz to 2-kHz frequency range. Vary the circuit by first increasing R_2 until oscillation starts and then stabilizes over the tuning capacitor's full range. A_1's output should be about 6 V pk-pk. Next, adjust the dial pointer and tuning-capacitor trimmer for best dial calibration and tracking. Tweak R_2 for maximum flatness as the tuning is varied over the full range. At higher frequencies, the OTA starts to introduce phase shift, which degrades dial-calibration accuracy if left uncorrected. As a result, the final circuit adjustment is to set C_1 for correct dial calibration at some high frequency, such as 20 kHz or above.□

CIRCLE 522

Disconnect Unstable Comm Channel

H. STEPHEN BERGER
ROLM Systems, 2420 Ridgepoint Dr., Austin, TX 78754; (512) 469-5000.

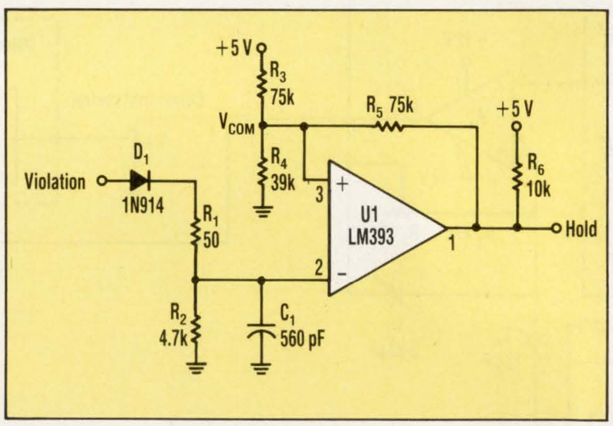
The receivers used in today's high-speed fiber-optic communications channels must remain predictable and stable when the transmitter is either turned off or disconnected. The high-gain front end that maximizes the system's dynamic range makes these receivers susceptible to noise and oscillation when no incoming signal is present.

In FDDI and similar applications, a synchronization signal keeps the receiver phase-lock loop tied to the transmitter. However, the high-gain front end may oscillate or amplify noise when not loaded. These errant signals could be interpreted as an incoming data stream, causing most receiver-decoder chips to signal invalid data patterns. The system controller then deals with the data errors. But, in the "quiet-line state," the decoder will attempt to decode amplified noise which it occasionally decodes as valid data.

The system controller, which can deal rather nicely with occasional transmission errors, could be completely occupied servicing the quiet line. This will degrade the controller's ability to perform any other tasks assigned to it. The controller should see occasional errors in a valid transmission so that it can NAK (negative acknowledge) the transmission, call for retransmission, or deal with the error according to the system's protocol. However, it's desirable to mask off a data stream containing continual errors so that the controller can ignore that channel and perform its other functions.

A simple technique can effectively close off a channel that's receiving an unacceptably high error rate *(see the figure)*. First, a line associated with decode violations is rectified. In this example, the violation pin on a transparent asynchronous receiver (AMD AM7969) is used. The line then charges an RC circuit, which is input to a comparator with the other input set to about half of V_{CC}. When the rectified signal charges the circuit above the preset level, U_1 triggers and generates a low signal that masks off the received signal.

The values of the RC circuit are chosen so that an occasional error won't trip the comparator and the circuit will discharge before the next error occurs. Designers must define the frequency of errors that that would trigger the circuit. Occasional errors will be fed through because they won't charge the RC combination enough to trip the comparator. But a data stream with continuous errors will keep the comparator turned on and mask off the channel causing the trouble. Designers must also be sure that sufficient hysteresis is used in the circuit to avoid constantly turning the channel turning the channel on and off.



WHEN A rectified violation signal charges this RC circuit above a preset level, the comparator masks off the transmitter from the received signal. That disconnects a transmitter to avoid receiving unwanted error signals.

With this inexpensive technique, fiber-optic channels can use all of the available dynamic range without being plagued by noise from a disconnected receiver. A series resistor, R_1, should also be used with the rectifying diode, D_1, to send an acceptable load to the violation line driver.

The design starts by setting the comparator's trigger and reset level. This circuit generates an active-low

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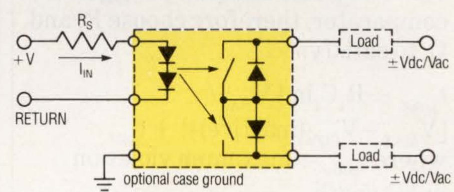
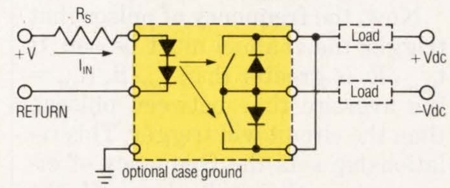
INPUT ELECTRICAL CHARACTERISTICS (−55° to +105° unless otherwise noted)			
	Min	Max	Units
Continuous Input Current (I_{IN})	10	50	mA_{DC}
Input Current (Guaranteed On)	10		mA_{DC}
Input Current (Guaranteed Off)		100	μA_{DC}
Input Voltage Drop at (I_{IN}) = 25mA		3.25	V_{DC}

OUTPUT ELECTRICAL CHARACTERISTICS (−55° to +105° unless otherwise noted)				
Part Number	FB00CD	FB00FC	FB00KB	Units
Bidirectional Load Current (I_{LOAD})	±1.0	±0.50	±0.25	A_{DC}/A_{PK}
DC Load Current (I_{LOAD})	2.0	1.0	0.5	A_{DC}
Bidirectional Load Voltage (V_{LOAD})	±80	±180	±350	V_{DC}/V_{PK}
DC Load Voltage (V_{LOAD})	80	180	350	V_{DC}
ON-Resistance (R_{ON}) at (I_{LOAD}) max.	0.72	1.8	12.9	Ohms
Turn-On Time (T_{ON})	800	800	500	μs
Turn-Off Time (T_{OFF})	300	600	500	μs

Notes: 1. A series resistor is required to limit continuous input current to 50mA (peak current can be higher).
2. Rated input current is 25mA for all tests.
3. Loads may be connected to any output terminal.
4. ON resistance shown is for the bidirectional configuration. The DC ON resistance is ¼ of these values.



B-directional and ac configuration



DC configuration

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CIRCLE 114

output. The first comparison voltage (V_{COM}) triggers the comparator.

$V_{COM}(inactive) = +5R_4/\{R_4 + [R_3R_5/(R_3 + R_5)]\}$.

The violation pulses must charge C_1 above this level to drop the output. Once the comparator is triggered, its output goes low. This lowers the comparison voltage, which is the circuit hysteresis. The reset level—the point where the circuit output goes high—is calculated as:

$V_{COM}(active) = +5[R_4R_5/(R_4 + R_5)]/\{R_3 + [R_4R_5/(R_4 + R_5)]\}$.

The circuit will reset when the error pulses are infrequent enough so that the voltage on C_1 falls below $V_{COM}(active)$.

The next step is to determine a hold time—the time the circuit stays low after triggering. This can be calculated as:

$t_{hold} = R_2C_1\ln[V_{MAX}/V_{COM}(active)] + t_{393}$, where $V_{MAX} = V_{signal}(high) - V_{diode}$ and t_{393} = LM393 response time.

Finally, the density of the violations that trigger the circuit must be set. One pulse shouldn't trigger the comparator, therefore choose R_1 and C_1 to satisfy:

$t_{pulse} > R_1C_1\ln\{V_{MAX}/[V_{MAX} - V_{COM}(inactive)]\} + t_{393}$, where t_{pulse} = maximum violation pulse width.

Now, the frequency of pulses that trigger the channel must be set. If t_{pulse}/R_1 is greater than t_{off}/R_2 (t_{off} = the average time between pulses), then the circuit will trigger. This relationship sets the frequency of error pulses that will close off the channel.□

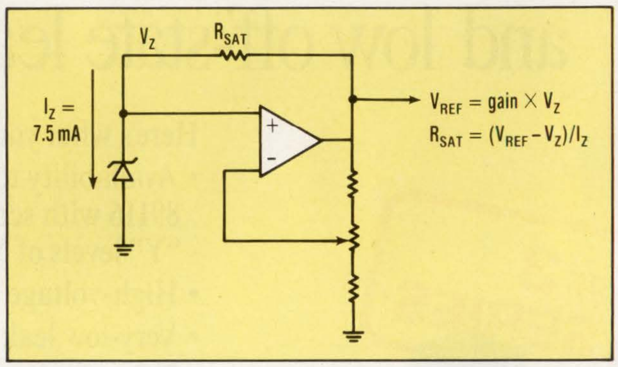
VOTE!

Read the Ideas for Design in this issue, select your favorite, and circle the appropriate number on the Reader Service Card. The winner receives a $150 Best-of-Issue award and becomes eligible for a $1,500 Idea-of-the-Year award.

CIRCLE 523

Obtain Optimum Zener Current

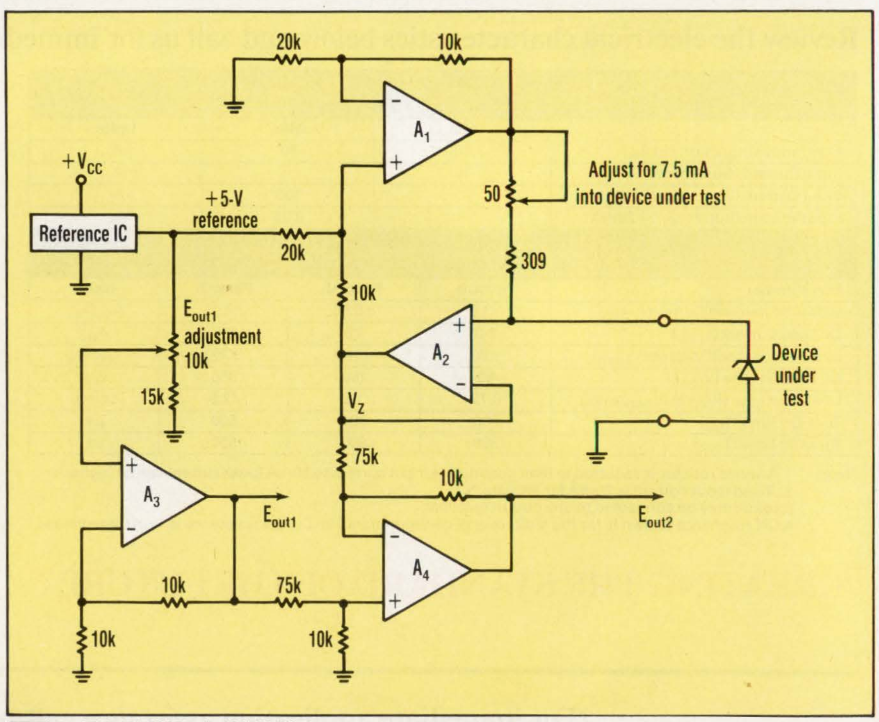
JOHN DUNN and CHUCK MEYER
Bertan Associates Inc., 121 New South Rd., Hicksville, NY 11801; (516) 433-3110.



1. THIS circuit derives reference voltages not readily acquired by common reference ICs. But, because the Zener voltage is toleranced at ±5%, a gain adjustment is needed to get the exact reference voltage.

Typically, an op amp and zener diode are used to derive reference voltages that aren't readily obtained from common reference ICs *(Fig. 1)*. The circuit's Zener diode can be a temperature-compensated device from the 1N823 family. However, that type of diode requires a 7.5-mA current to guarantee the best possible temperature coefficient. Because the actual Zener voltage a device can exhibit at 7.5 mA is toleranced at ±5%, a gain adjustment is needed to obtain the exact reference voltage required. Thus, a select-at-test resistor, R_{SAT}, must be calculated on a case-by-case basis to establish the required current.

This procedure can be cumber-



2. TO FIND A VALUE for the select-at-test resistor easily, adjust the potentiometer so that E_{out1} equals the V_{REF} from the first circuit. Then measure E_{out2}. This number, in millivolts, is equal to R_{SAT} in ohms.

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IMAGE PRESENTATION

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Bt261: HSYNC Line Lock Controller, 30 MHz Pixel Clock Generation, MPU Programmable Video Timing, Programmable Noise Gating, Generate HSYNC, Recovers VSYNC and FIELD, External VCO or High Speed Crystal Oscillator Clock Generation, 28-Pin PLCC Package.

MANIPULATION

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Bt294: YCrCb to CCIR 601/SMPTE RP125 Decoder, Handles Video Timing Recovery, Ancillary Output Port, Error Checking, 16-Bit YCrCb I/O Bus, YCrCb to RGB Output Look-up Tables, 100-Pin PLCC Package.

PRESENTATION

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some because the Zener voltage, V_Z, of the device at currents other than 7.5 mA won't be exactly the same as the 7.5-mA V_Z value. Trying to find R_{SAT} by adjusting for 7.5 mA in the circuit can be difficult because any metering needed to measure that current can, upon removal, cause a marginal current shift.

A convenient solution to the problem is a test circuit *(Fig. 2)*. The device-under-test is the specific Zener diode to be used in the voltage reference circuit. With the Zener diode connected, first adjust the 10-kΩ potentiometer so that E_{out1} in the test circuit equals the intended V_{REF} output from the first circuit. Then, E_{out2} is measured. This measurement will be in millivolts, equal to the required R_{SAT} resistance in ohms.

For example, let the intended V_{REF} equal 8.0 V. Then connect a Zener to the circuit and turn it on. Op amps A_1 and A_2 will pump exactly 7.5 mA into the Zener, regardless of the exact value of V_Z. Afterwards, set E_{out1} for the intended value of 8.0 V. Assume that the Zener exhibits 6.32 V at 7.5 mA. Then:

$E_{out2} = (E_{out1} - V_Z)/7.5 = (8.0 - 6.32)/7.5 = 224$ mV, meaning that R_{SAT} of the first circuit should equal 224 Ω to go with the Zener being tested.

This result's accuracy depends on the accuracy of the components chosen for the second circuit. Using quality op amps, resistors, and a good +5-V reference IC is highly recommended.□

IFD WINNERS

IFD Winner for June 14

Robert A. Pease, National Semiconductor Corp., 2900 Semiconductor Dr., Santa Clara, CA 95051; (408) 721-5613. His idea: *"Protection circuit cuts voltage loss."*

IFD Winners for June 28

Jeff Kirsten and Len Sherman, Maxim Integrated Products, Inc., 120 San Gabriel Dr., Sunnyvale, CA 94037; (408) 737-7600. Their idea: *"Isolate data-converter signals."*

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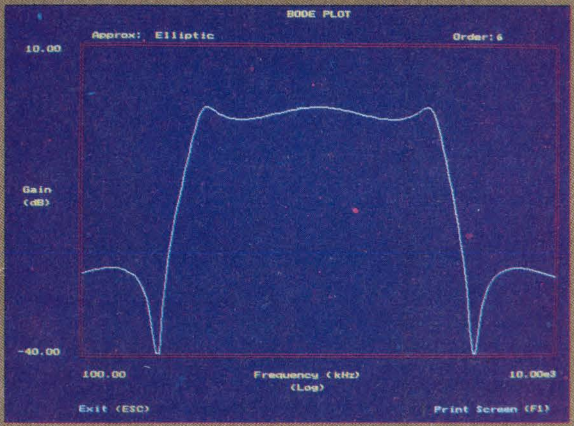

Advanced Filter Designer Bode Plot

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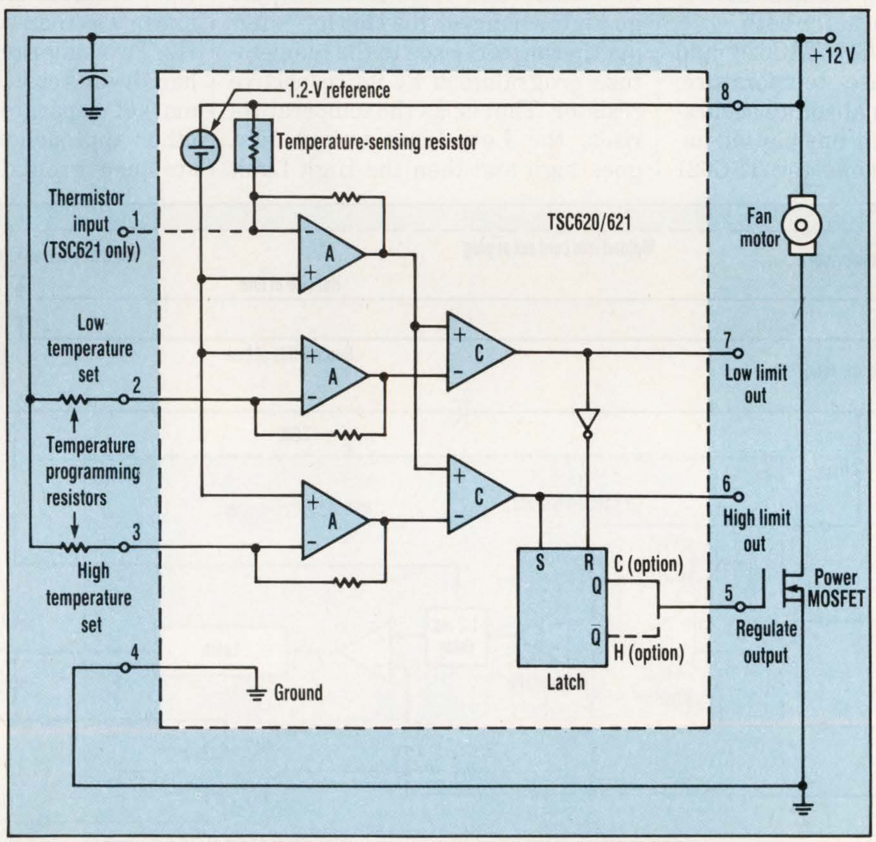
CIRCLE 103

SOLID-STATE SENSOR SWITCHES SAVE LIVES AND EQUIPMENT

TEMPERATURE AND CURRENT-SENSING ICs WILL GO IN PRODUCTS FOR HOME, OFFICE, AND FACTORY.

Two new low-cost chips, from Raytheon and Teledyne Components, can help overcome two natural hazards to every piece of electrical or electronic gear—water and high temperature. The Teledyne ICs represent the first members of a new family of solid-state thermal switches, designed to replace expensive, vibration-sensitive, bimetallic temperature sensors commonly used in applications ranging from coffee makers to home-heating thermostats. Raytheon's device is a low-power two-wire ground-fault interrupter (GFI) controller. Though designed



1. THE TSC620 TEMPERATURE-SENSING SWITCH from Teledyne Components has been programmed to sense when the chip's temperature rises to specific high and low set-point. When it reaches the High set-point, it turns the MOSFET and then the fan on. When its temperature drops to the Low set-point, it turns them off.

FRANK GOODENOUGH

for use in home hair dryers, it could be used as a safety element in anything that plugs into the ac line which gets wet at the same time a human touches it. It's a result of Underwriters Laboratory (UL) edict UL943: To be UL certified, all hair dryers sold in the U.S. after 1990 must include a leakage current detector in the dryer, or in the cord.

Because both the Teledyne and the Raytheon ICs aim at products for the consumer, they are low-priced: In low volume, they go for under $1 each. Therefore, not only will they find their way into various appliance, toy, entertainment, garden, automotive, and tool products for the consumer, but they also should represent a low-cost way for sharp designer-marketers to distinguish their products from the competition. Computers and office machines of all types (for example, medical instruments) seem a natural for both.

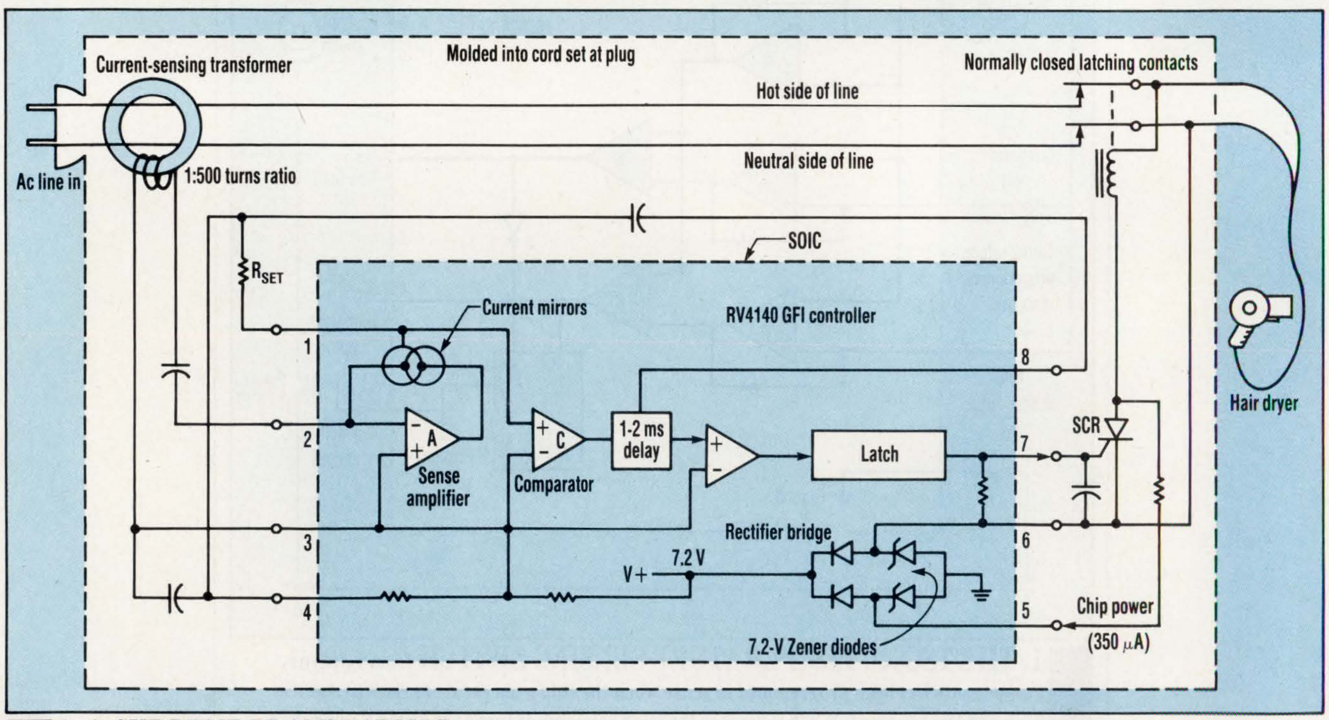
The Teledyne ICs, TSC620 and TSC621, both sense temperature: The TSC620 has an absolute accuracy of ±3°C with an on-chip ion-implanted resistor, while the TSC621 uses an external thermistor. The TSC620 can replace the snap-action thermal switches found in many appliances or motors, providing simple on-off protection and/or control. However, unlike such switches, these ICs sport high and low-temperature, user-programmable (with two resistors) set-point inputs and a trio of logic outputs for control. As a result, they lend themselves to simple, but versatile, multi-temperature alarm or control systems. One TSC620 and less than two dozen low-cost parts can build a complete heating-cooling thermostat for the home.

One 90-kΩ to 200-kΩ resistor connected between each programming input and the supply determine high and low temperature set-points, respectively *(Fig. 1)*. The two logic outputs, Low Limit and High Limit, obey the following truth-table: The Low Limit and High Limit outputs go high whenever the chip (or external thermistor) rises to the temperature programmed by its respective resistor. That is, as the temperature rises, the Low Limit output first goes high and then the High Limit output will go high. Each limit-output goes low when the chip (or thermistor) temperature drops about two degrees below its programmed value. In a typical application, when the Low Limit goes high, it could turn on a fan and alert a host (human or silicon). If the temperature rises enough to trip the High Limit, the system can shut down and set off an alarm.

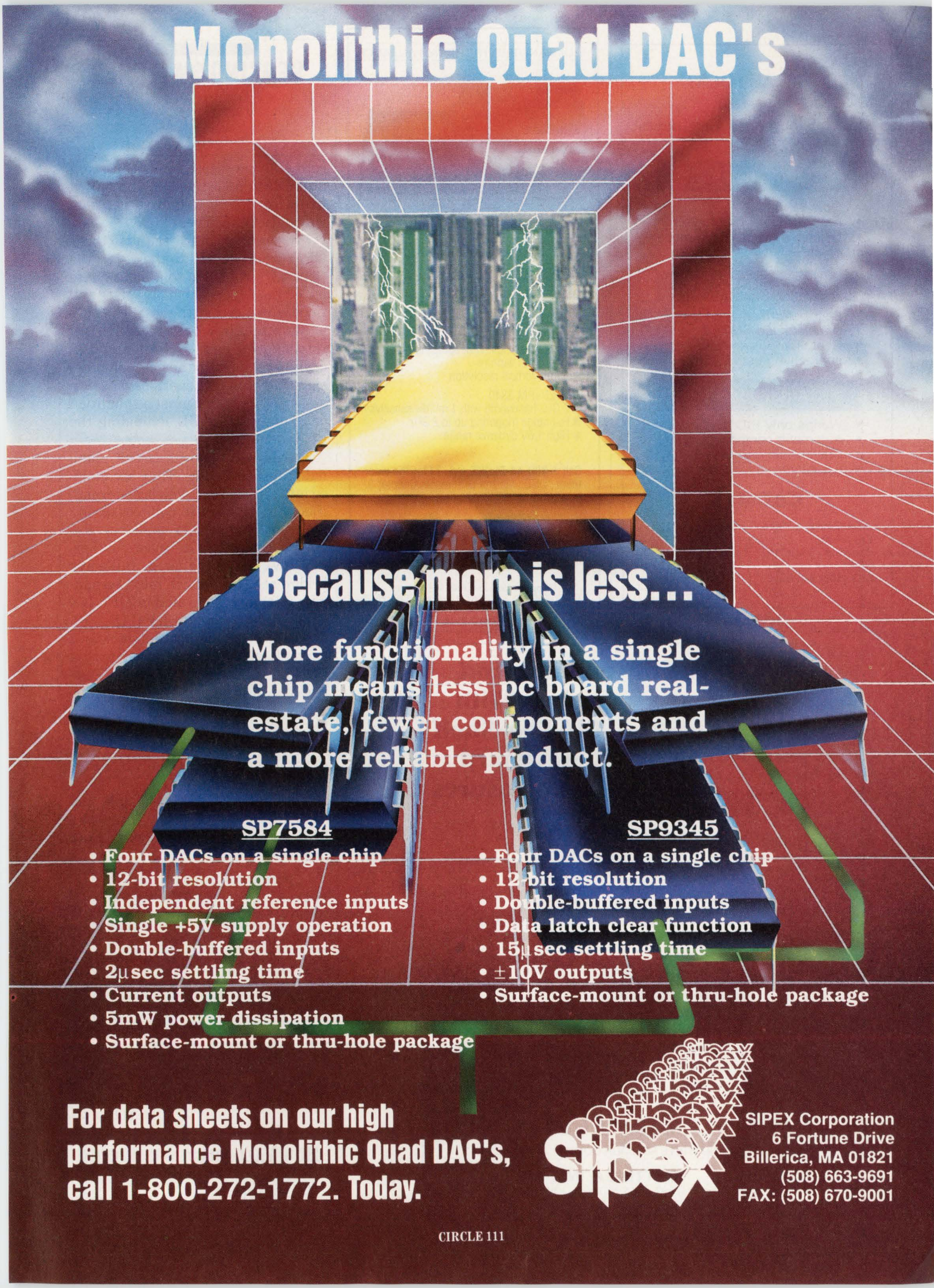
The Regulate logic output goes high when the temperature that's sensed rises to the High set-point and goes low when it drops below the Low set-point.

No More Shockers

The Raytheon device's job is to open both sides of the ac line in less than 24 ms if a dangerous condition arises. That is, it must detect 5 or 10 mA of leakage current (5 mA in the U.S., 10 mA in Europe) and open the line in less than two cycles of 50 or 60 Hz. Two major features that affect a hair dryer's cost, design, and time-to-market separate the RV4140 from other approaches for detecting and stopping ground-fault leakage cur-



2. A CURRENT TRANSFORMER, plus the RV4140 two-wire ground-fault interrupter (GFI) from Raytheon, senses the difference in current between the hot and neutral side of the ac line if the leakage current between the two through the load exceeds 5 mA. The same situation would occur if a load, such as a hair dryer, falls into a tub of water. When detecting the fault, the chip fires the SCR, which in turn opens the latched relay and then the line.



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CIRCLE 111

rent—no modification to existing dryer designs is needed, and only a two-wire line is required between wall outlet and dryer *(Fig. 2)*.

Present solutions require three wires from the GFI to the dryer; the third wire connects to a metal plate inside the dryer. The metal plate and third wire increase the cost. The metal plate requires both redesign and retooling for each existing and new design, adding further cost and design time. Finally, every new design and every redesign must be qualified or requalified by UL, extending the time-to-market.

The RV4140 and its circuit eliminate these problems. They are molded into the cord set, which, once qualified, can be used to connect to any dryer, or to any other appliance. Reducing cost and size even further, the RV4140 contains a full-wave bridge rectifier, which must be added externally to available GFI ICs (including Raytheon's RV4145).

At the heart of the detector is a current-sensing transformer with a toroidal laminated-steel or solid-ferrite core. A ground fault causes a difference between the currents in the hot and neutral wires.

Amplified, rectified current generates an error at pin 1. If the error is greater than the reference voltage at pin 3, the comparator C trips and fires the SCR, thus opening the relay and the line to the dryer.□

Price And Availabilty

In quantities of 100, Teledyne's commercial-grade TSC620 goes for $1.18 each, dropping to $0.70 in volume quantities. The Raytheon RV4140 typically runs on 350 µA from the ac line through pin 8 and the bridge rectifier. It comes in 8-pin DIPs and SOICs. In quantities of 100, the controller goes for just $0.68, and is significantly less in greater volume.

Teledyne Components, 1300 Terra Bella Ave., P.O. Box 7267, Mountain View, CA 94039-7267; Rich Clarke, (415) 968-9241.

Raytheon Company, Semiconductor Div., 350 Ellis St., Mountain View, CA 94039-7016; Harry Gil, (415) 968-9211.

CIRCLE 533

How Valuable?	Circle
Highly	534
Moderately	535
Slightly	536

The power-user's guide to the new HP 48SX.

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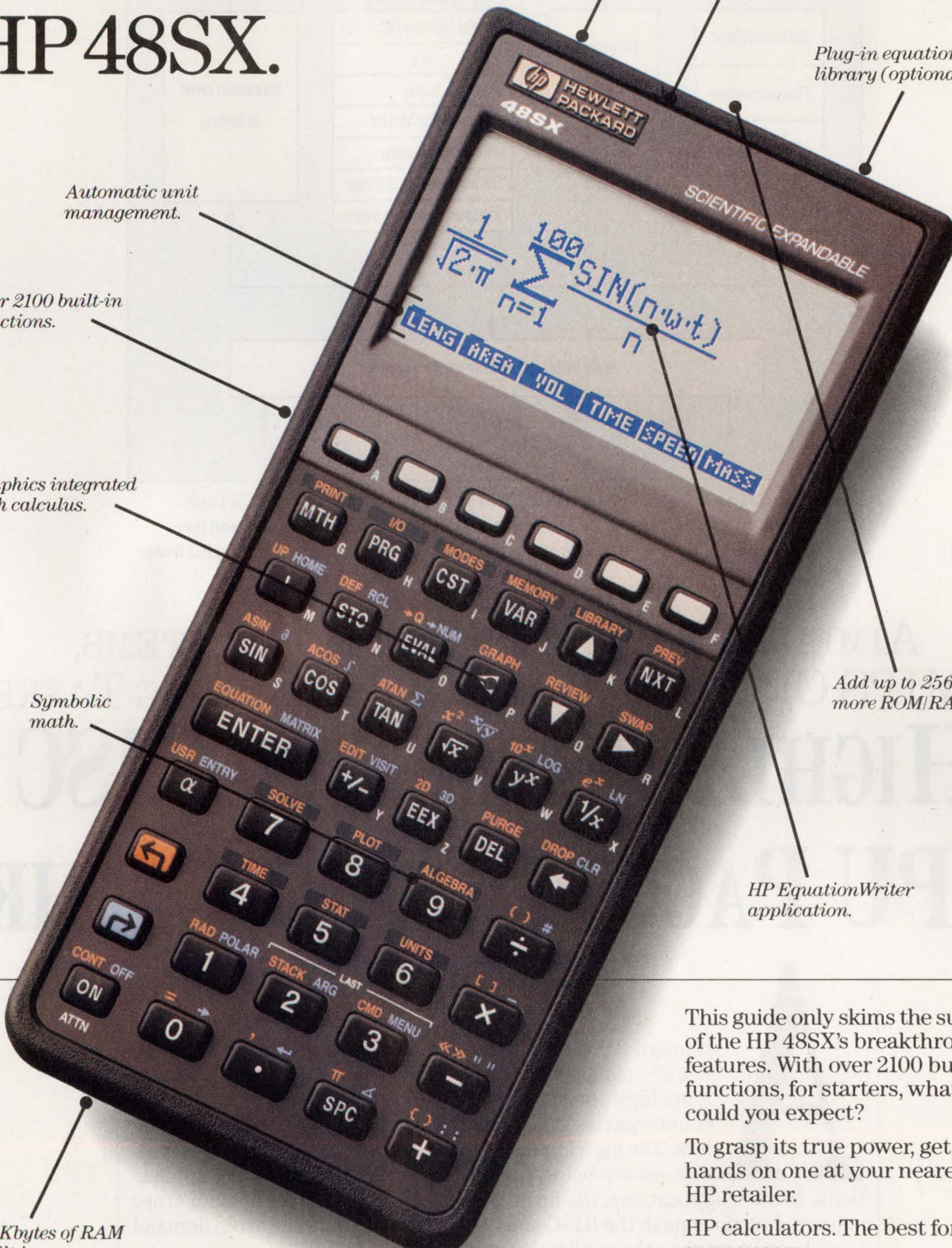

This guide only skims the surface of the HP 48SX's breakthrough features. With over 2100 built-in functions, for starters, what could you expect?

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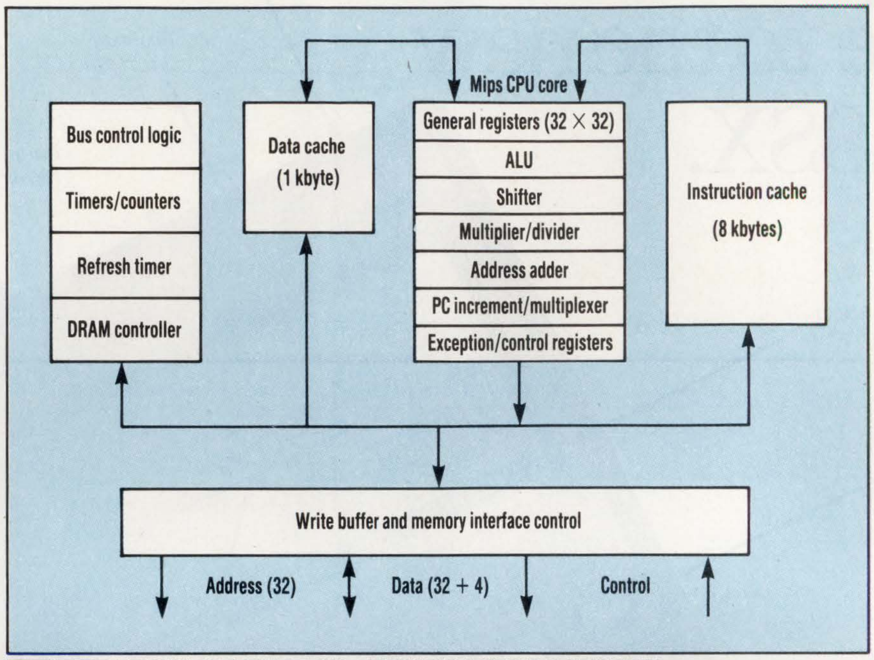
CIRCLE 96



THE HIGHEST-INTEGRATION MIPS PROCESSOR **from LSI Logic packs 8 kbytes of instruction cache, 1 kbyte of data cache, a DRAM controller, and three counter-timers. The chip's features let the processor tackle demanding control applications.**

AIMED AT EMBEDDED CONTROL SYSTEMS, A MIPS CPU CHIP TAKES ON DEMANDING TASKS.

HIGHLY INTEGRATED RISC CPU PACKS I/O AND CACHE

DAVE BURSKY

Although RISC-based systems offer top performance, they're usually expensive to implement because they require many more high-speed support components than their CISC-based counterparts. This is particularly true for embedded controllers. The high implementation cost is critical when RISC processors are being considered for embedded control applications. In such applications, the large number of fast static RAMs and other support functions push the RISC subsystem cost up, and very often demand more board area than the application can spare.

By redesigning its licensed version of the R3000 processor, LSI Logic has taken into account many of the system-level requirements for an embedded controller. As a result, they've combined the equivalent of about 20 chips into one device—the LR33000. The CMOS chip is built with static logic to minimize power consumption during standby or power-down situations.

Along with the R3000-compatible integer processor, the LR33000 proces-

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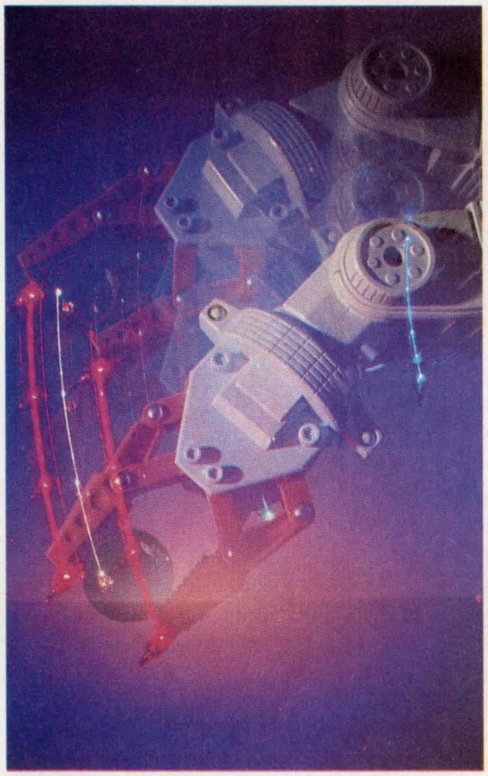

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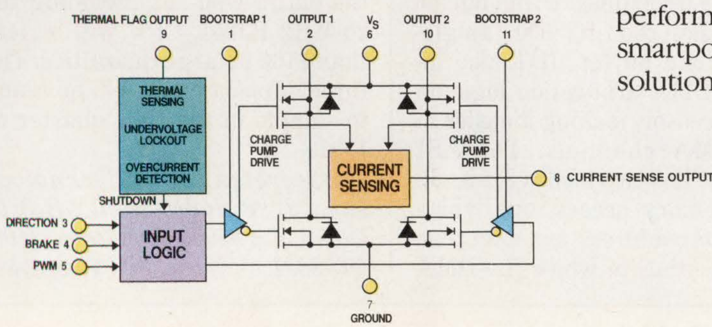

FAIL-SAFE PROTECTION.

Not only does the LMD18200 know when to start, it knows when to quit. Specially equipped with a two-stage thermal warning system, it transmits a distress flag to the host system at 145° C, allowing you enough time to take any corrective action.

And if the temperature reaches 170° C, the device automatically shuts down. A fail-safe feature that eliminates damage to your equipment.

What's more, the LMD18200's on-chip defense system provides overcurrent protection, which prevents damage both to the device and the motor in case a shorted load causes the motor to draw excessive current.

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HIGH-INTEGRATION MIPS CPU

sor includes 8 kbytes of instruction cache, 1 kbyte of data cache, a dynamic-RAM refresh controller, three counter-timers, a one-word-deep write buffer, and other features *(see the figure)*. All of that memory and logic has been compressed into one 160-lead quad-sided plastic flat package or a 155-lead pin-grid array. One reason for the high pin count is separate address and data buses, and optional parity lines on the data bus. The processor will come in maximum operating frequencies of 25, 33, and 40 MHz, with maximum power consumption of 2 W at 25 MHz.

On-chip caches and an integrated write buffer give the chip almost the same performance as the R3000 CPU with a large external cache for embedded systems applications. The benefit of integrating on one IC cache and other logic with the CPU was also adopted by Integrated Device Technology. The firm has also embellished the R3000 CPU with features targeted at embedded control *(see "Approaching the problem differently," this page)*.

Both the on-chip caches on the LR33000 are direct-mapped. To ensure data-cache coherency, a write-through approach is used to keep data current. Single-word memory references or blocks of data can be loaded into the cache. The block size for refill operations of 2, 4, 8, or 16 words can be programmed independently for both the data and the instruction caches.

To offload the write operations, a one-word write buffer lets the processor think it wrote a word into memory. Therefore, the CPU can start its next operation while the buffer actually writes the word into main memory. If the buffer is full and the CPU tries to write to external memory, the processor will stall until the buffer is free. In addition, if an entry is located in the cache, the processor will update the cache as well as the main memory.

To pack all of the system features on the chip, designers at LSI did make some sacrifices. Unlike the R3000, the LR33000 doesn't include a memory-management unit because most embedded control applications

APPROACHING THE PROBLEM DIFFERENTLY

As if they gazed into a crystal ball concerning LSI Logic's introduction, designers at Integrated Device Technology Inc., Santa Clara, Calif., jumped the gun on LSI and unveiled a pair of Mips-based CMOS embedded-controller chips targeted for similar applications. However, the chips have a different mix of features than those selected by LSI. As a result, they're optimized, perhaps, for yet a different set of embedded-control applications. The IDT R305X family consists of two basic high-integration CPUs, both based on the R3000A processor.

Four different speed options—20, 25, 33, and 40 MHz—will be available for each processor, giving users a performance span from 16 to 35 MIPS. Designers at IDT, though, decided not to redesign the CPU core to use static CMOS logic. Consequently, the R305X processors, like the R3000A, require that a clock signal always be present to keep the internal dynamic logic active.

The lowest-cost version, the 20-MHz R3051, contains instruction and data caches of 4 kbytes and 2 kbytes, respectively. A higher-integration version, the R3052, packs 8 kbytes of instruction cache and also 2 kbytes of data cache. But unlike the LR33000, which has separate address and data buses, the IDT processors employ a multiplexed address/data bus to reduce chip pin count, squeezing into 84-lead plastic leaded chip carriers. Furthermore, the IDT processors include both a 4-word-deep read buffer and a 4-word-deep write buffer rather than the LR33000's single-word write buffer. IDT also includes DMA arbitration logic on the processor, making it easier to add DMA channels. The LSI LR33000 has two modes for its direct memory access, one which grants the address and data bus, and the other in which the DMA logic uses the on-chip DRAM controller to access the memory.

Although the 3051 or 3052 don't have the DRAM controller or the counter-timers that LSI felt necessary to include on the chip, the IDT processors kept the memory-management unit (MMU) and translation-look-aside buffer (TLB). Actually, IDT designers thought that each processor should be available with a choice. As a result, two versions of the R3051 and two versions of the 3052 actually exist: one version of each without the TLB for lowest cost, and another version of each with the TLB for slightly more.

The more-spartan CPU chips from IDT will sell for less—in 1000-unit lots the lowest-cost version of the R3051 (20 MHz, no TLB) will sell for about $45, while the larger-cache version, the 3052, will go for about $65. Limited sampling will start this quarter.

To add many of the system-level features, such as multiple DMA channels, serial I/O ports, DRAM control, parallel ports, counter-timers, interrupt controllers, and more, IDT has planned a trio of support chips. The circuits include the IDT79R3720 bus exchanger, the 79R3721 DRAM controller, and the 79R3722 I/O interface controller. The three support chips will come in low-cost 68- and 84-lead plastic leaded chip carriers and a 132-lead plastic quad-sided flat package, respectively. When used as a set with the high-integration CPU, they form a compact and relatively complete RISC system—somewhat akin to a PC motherboard. The cost for the entire chip set, including the 20-MHz R3051, CPU will be less than $100 in large quantities. The three support chips will be ready to sample in the first quarter of 1991.

Integrated Device Technology Inc., 3236 Scott Blvd., Santa Clara, CA 95052; Bob Rowe, (408) 492-8631. **CIRCLE 524**

HIGH-INTEGRATION MIPS CPU

don't rely on virtual memory addressing. Moreover, because floating-point math is more the exception than the rule in embedded control, the math coprocessor interface was also eliminated.

One area that LSI didn't skimp on, though, was aids for troubleshooting and diagnostics. Because debugging embedded systems can be more difficult than debugging general-purpose computers, a strong set of diagnostic features were included on the chip. Separate instruction and data breakpoint registers are available. And the processor can perform instruction traces to track down erroneous operations.

Furthermore, since the chip is still software-compatible with the R3000, existing R3000 software development tools will serve the development teams. However, because nine instructions using the coprocessor and four that reference the translation-look-aside buffer can't execute, the processor traps when it encounters one of those commands and can either raise a flag or vector to a subroutine to aid in program debugging.

To take on the embedded applications, the three on-chip timers serve both the on- and off-chip timing needs. Of the three timers, two are 24-bit down counters and are available for any application. Each counter operates at the system clock rate. Each will reload the initial count value after it reaches a 0 count. Timer 2 also has a Terminal Count Output pin, as well as a Count Enable Input pin, suiting it for timing external events.

The third timer is just 12-bits long and supports the DRAM refresh controller. That refresh controller includes a programmable wait-state generator that allows almost any-speed DRAM to be used with the chip. Commonly available 70- and 80-ns memories can be used with the processor. When running with the page-mode DRAMs, four CPU cycles are needed for the first access, and then two for each subsequent access on the same memory page.

The chip provides the row-address-strobe, column-address strobe (RAS, CAS) and output-enable signals needed to control standard and page-mode DRAMs. The on-chip memory controller allows for an address space of 256 Mbytes. However, to drive more than one bank of memory chips, address multiplexers and buffers should be used. The memory controller can also tie into off-chip DMA controllers that use a synchronous bus protocol. Single-cycle block refills can thus be done when interleaved memories are employed.

The processor can handle 32-, 16-, and 8-bit data-words. Byte ordering can be set for either "big-endian" or "little-endian" formats. To deal with different system-cost strategies efficiently, the processor can boot itself from either a low-cost 8-bit EPROM, or from a full 32-bit storage subsystem. A Bytewide control pin tells the processor which type of memory subsystem to look for. With a programmable wait-state generator, users can also specify the time between reads, from 0 to 15 wait states. In addition, the internal wait-state generator can be overridden by setting a control bit in the processor's configuration register. That lets the memory access be controlled by the External Data Ready signal.

Furthermore, a generic synchronous 32-bit interface makes it easy to tie the LR33000 into support chips or moderate-speed static RAMs. A memory-mapped 16-Mbyte I/O space gives users plenty of room for peripheral extensions to the chip.□

PRICE AND AVAILABILTY

In 1000-unit quantities, the 25-MHz, ceramic pin-grid-array version of the LR33000 sells for $192; samples will be ready in December. A plastic quad flat-packaged version of the 25-MHz chip will sell for $99.95, available in the second quarter of 1991. Ceramic PGA versions of the 33- and 40-MHz chips will be ready to sample in the first and second quarters of 1991 and will sell for $230 and $385, respectively.

LSI Logic Corp., MIPS Div., 1525 McCarthy Blvd., Milpitas, CA 95035; Rob Tobias, (408) 954-4789. **CIRCLE 525**

HOW VALUABLE?	CIRCLE
HIGHLY	526
MODERATELY	527
SLIGHTLY	528

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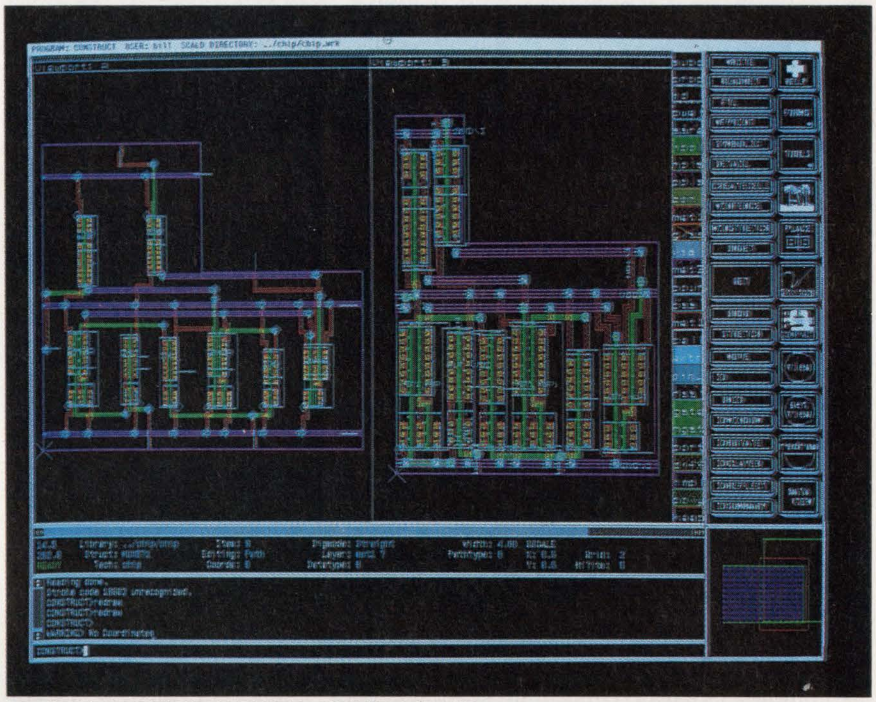
CIRCLE 82

PROCESS-INDEPENDENT IC TOOLS AID TOP-DOWN DESIGN

A DEVICE-LEVEL COMPACTOR IS THE KEY TO FAST AND EASY MIGRATION OF DIGITAL ICs TO ALTERNATE PROCESS TECHNOLOGIES.

LISA MALINIAK



THE DEVICE-LEVEL COMPACTOR in Construct P.I. is the essential element in process-independent IC design. The compactor references the technology database to shrink or expand all layers of the layout while keeping design-rule correctness. In this screen, the compacted layout is in the right window.

Two major concerns for engineers are the ability to reuse IC designs and the ability to catch critical mistakes before the end of the design cycle. These concerns can now be driven away with two IC design tools from Valid Logic Systems: Construct Process-Independent (P.I.), an advanced cell-layout tool, and Compose Architect, a floorplanning tool. These devices implement process-independent and top-down IC design methods. Process independence means that users can create IC designs without concern for specific process design rules.

With the tools, which are enhanced versions of Valid's previous Construct and Compose software, users can architect and analyze an entire chip at a high level. Both tools enable design teams to migrate chips quickly when a process change occurs. In addition, they save time because design teams can reuse portions of their design in future chips.

Construct P.I. includes device-level compaction, graphical device generation, and net-list-driven layout. Essentially, it brings process-independence into the realm of the layout designer. The device-level compactor is the key to process-independent physical layout. This new feature complements the existing process-independent methodology for chip assembly made possible by the mixed block-cell compactor in Compose. In addition, these compactors work from one process technology database.

Device-level compaction spaces (shrinks or expands) the layout automatically according to the design rules in the technology database *(see the figure)*. The software can compact both orthogonal and encapsulated non-orthogonal geometries. It also maintains connectivity between wires and devices during compaction.

The single technology database centralizes control over both physical-layout and chip-assembly tasks, eradicating schedule impacts due to design-rule changes. Design rules stored in the technology database can be easily modified when a change in process is necessary due to technology advancements or foundry changes. For instance, designs can be easily migrated from a 2-μm to a 1-μm CMOS process with a minimal amount of manual layout work.

In addition to the device-level compactor, Construct P.I. implements process independence through the Graph-A-Cell graphical device generator. Graph-A-Cell minimizes the effort needed to lay out and maintain device libraries. Designers automatically generate parameterized cell (PCELL) programs that produce design-rule-correct layout. In addition, because the primary input source is graphical, layout designers of all skill levels can easily generate PCELL programs rather than rely on a CAD programmer to accomplish this task.

Graph-A-Cell

Using Graph-A-Cell, designers can quickly sketch a device without regard for design rules or efficient use of area. Graph-A-Cell then uses scanning technology to assign layer-to-layer constraints automatically. The C-code program output from Graph-A-Cell can be stored in a device library and called by the designer during layout editing to generate PCELLS instantly. These programs can also be manually modified to create complex PCELLS containing spirals and odd angles. Entire device libraries, as well as the designs containing the devices, can be rolled over to a new process simply by changing the rules in the technology database and recompacting for design-rule correctness.

Construct P.I. achieves correct-by-construction layout design with net-list-driven editing that maintains actual connectivity in the design database. The net-list-driven editing feature reads the net list and associated schematic properties—such as gate sizes, wire widths, and device groupings—to drive the physical-layout design. Net-list-driven editing and correct-by-construction layout design reduce the need to perform design-rule checking and layout-vs.-schematic comparison.

Construct P.I. also includes symbolic editing. This editing technique gives engineers the flexibility to view and edit physical design data at the symbolic level for simplified data representation and faster display speeds. It also lets them view and edit at the mask level for detailed representation.

In addition to a process-independent IC design environment, Valid offers Compose Architect, a multilevel, top-down floorplanner for mixed block-cell chips. The top-down design implemented by Compose Architect improves designer productivity and shortens the design cycle.

Compose Architect is a net-list-driven chip floorplanning and analysis tool that lets IC design engineers explore architectural trade-offs early in the design cycle. They can work with mixed block and cell designs from the top level of hierarchy down, assembling a chip floorplan to optimal size and performance specifications. This top-down method facilitates the use of different design methodologies on one chip. For example, engineers can create chips using a combination of handcrafted devices, compiled modules, standard cells, synthesized layouts, and scaled existing layouts.

At any level of design hierarchy, Compose Architect coordinates the assembly of IC design elements in varying stages of abstraction or completion. Each design level and design element can be individually floorplanned and partitioned so that design teams can work simultaneously. Top-down floorplanning is linked with bottom-up chip assembly and layout to minimize design iterations. Detailed placement, routing, and compaction can be performed throughout the floorplanning process before all of the underlying physical layout data is fully created. Compose Architect tracks the status of all levels and elements in the floorplan to the end of the design cycle. At this point, the floorplan represents the finished chip design, incorporating all physical layout data.

To speed floorplanning and facilitate concurrent design, Compose Architect includes a suite of in-process tools for power, delay, and path analysis. With these tools, engineers can identify and correct chip size and performance problems up front, before the problems seriously affect the design or work schedule.

Compose Architect's power analyzer improves the accuracy of power-supply tapering by calculating voltage drops and adjusting net widths accordingly. With the delay analyzer, engineers can dynamically examine chip timing at any design stage. Compose Architect calculates pin-to-pin delays automatically for direct input into Valid's RapidSim digital simulator or other commercial simulators. Engineers can further improve chip speed with the static critical path analyzer. Compose Architect calculates resistance and capacitance values and passes them to Pathmill. Pathmill then highlights critical paths and delay bottlenecks in the floorplan.

Valid's Design Process Framework is the key to providing a complete family of IC products. The framework features rules-driven and multilevel design techniques that improve communication between engineering and layout personnel using the products. Front-to-back integration through the framework ties Valid's front-end tools with Construct, Construct P.I., Compose, Compose Architect, and the Confirm verification tools. The Confirm suite includes tools for on-line design rule checking and layout-vs.-schematic comparison.☐

Price And Availabilty

Construct P.I. and Compose Architect will begin shipping in the fourth quarter for Sun workstations. Both will be available for the DEC and IBM workstations in early 1991. Construct P.I., including the device-level compactor, starts at $50,000. Current Construct users can upgrade to process independence by purchasing the device-level compactor separately. The device-level compactor option begins at $15,000. Compose Architect can be purchased standalone starting at $30,000. It also comes bundled with the detailed routers of the Compose chip assembly tool, starting at $65,000. All prices include Access network licensing.

Valid Logic Systems Inc., 2820 Orchard Pkwy., San Jose, CA 95134; (408) 432-9400. **CIRCLE 529**

How Valuable?	Circle
Highly	530
Moderately	531
Slightly	532

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CIRCLE 122

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NEW PRODUCTS

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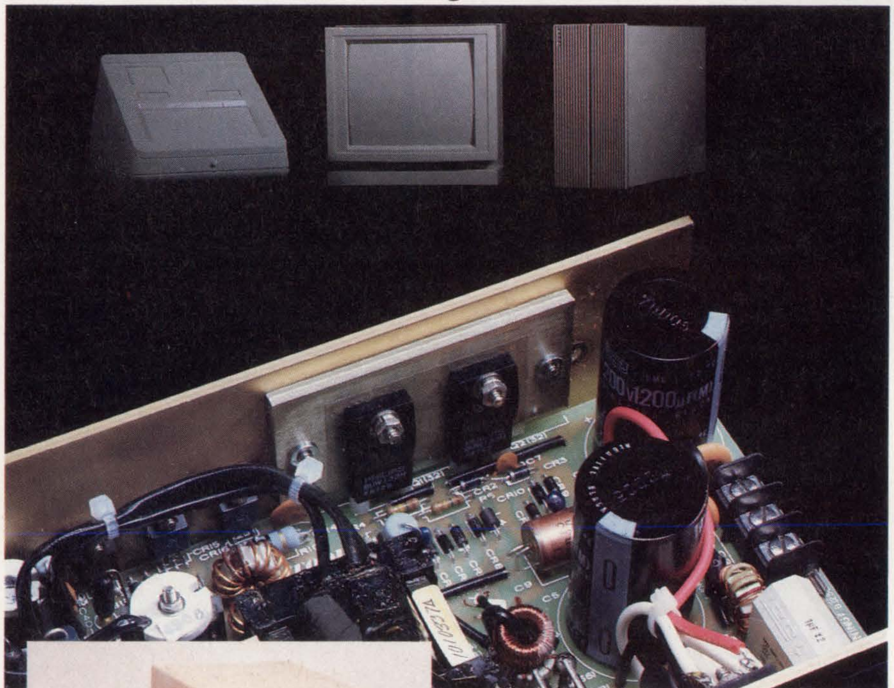
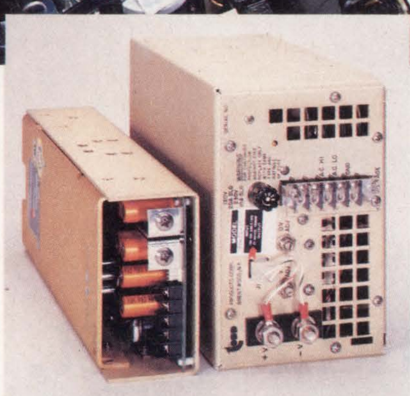
Single Board Construction Shrinks 750W Size and Cost: 58% Smaller, 30% Cost Savings





Designed for high-end computer products, TODD's MAX-750 combines a compact size, 13.5" x 5" x 2.6" compared to the typical 5" x 8" x 11" shoebox switcher (see photo insert), and very competitive pricing. OEM product designers can reduce product size with a MAX-750 or build in power supply redundancy, replacing one "shoebox" switcher with two MAX-750's in the same space.

The small package size, high power density of 4 watts/in., high peak current for motor starting, and cooling options, make the MAX-750 the power supply of choice for VMEbus systems, workstations, file servers and mini-computer systems. The switcher provides 120 amps of +5 volts for logic and memory, and features up to three auxiliary outputs providing high efficiency, tightly regulated 12 volts or −5.2 volts at up to 20 amps. Designed for world wide use, the series offers AC power fail, AC autoline select, and meets International Safety standards and Class A RFI requirements of FCC and VDE 0871.

Call 1-800-223-TODD, or CIRCLE 169

High Efficiency DC Converters Fit AC To DC Footprint

TODD's DC to DC converters provide up to 350 watts from 48 volts DC input. Designed as companion units to TODD's standard line of AC input power supplies, they are fit, form, and function compatible with the MAX-350, MTC-250, MTC-350, and certain single output SC series products.

Available in a 250 watt "DC" single output series and a 350 watt multi output "DCX" series these power supplies have up to 50 amp main output of tightly regulated 5V power, two fully regulated, high-efficiency, post-regulated mag-amp outputs and one low-power three-terminal regulated output.

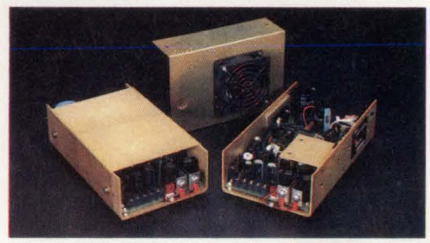
Call 1-800-223-TODD or CIRCLE 170

New Technology Shrinks 500 Watt Power Supply

TODD's MAX-500 switchers pack 25% more power into TODD's 400 watt package size (11.5" x 5" x 2.5"). The series incorporates a new SMT circuit, newly-available components, improvements to TODD's VERI-DRIVE current-fed inverter topology, monocoque construction, and a high efficiency FLUX-GATE switching mag-amp auxiliary post regulation. Result: higher performance, higher reliability (approaching 100,000 hours MTBF) and lower cost.

Call 1-800-223-TODD or CIRCLE 171

Super Micro Supply Has a Cool 350 Watts



Targeting the computer-based OEM, TODD engineers developed the 9" x 5" x 2.5" MAX-350 series of competitively priced switching power supplies. Low component count, extensive use of SMT and raising efficiencies to 80% with attendant reduction of heat sink requirements results in MTBF approaching 100,000 hours.

The series features up to 50 amps of +5 volts for logic and memory and fully regulated high efficiency mag-amp outputs to power up to four disc drives. Auxiliary outputs power common peripherals like ECL monitors, RS232 outputs, communications drivers, etc.

Call 1-800-223-TODD, or CIRCLE 172

More information on these and the full line of TODD Switching Power Supplies can be obtained in EEM File 4000, by circling the response card numbers, or by contacting:

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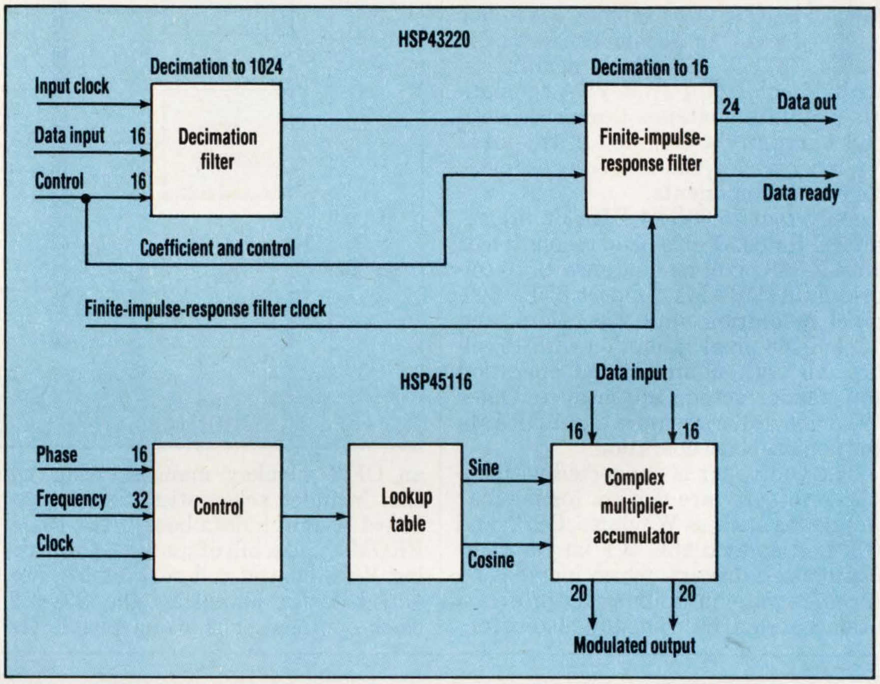
FAX (516) 231-3473

SEE US AT ELECTRONICA

Communications-Targeted DSP Chips Deliver Top Throughput

Dave Bursky

As the communication spectrum gets more crowded, more precise filtering and frequency control is needed to ensure high-quality and stable reception of transmissions. To aid in the filtering and tuning, a digital decimation filter and a combination numerically controlled oscillator and modulator have been developed by Harris Semiconductor. With those two CMOS chips, designers can now build the heart of a digital receiver with an out-of-band attenuation of 96 dB and a tuning accuracy of 0.006 Hz (with a 30-MHz sampling rate). The chip set can considerably simplify applications such as i-f channels for satellite data links, radar and sonar data gathering, narrowband spectrum analysis, and others.



The first of the two chips, the HSP43220 decimating digital filter, operates at clock rates of up to 35 MHz and can be programmed for decimation levels of up to 16,384—loosely equivalent to about 512,000 standard filter taps. On the chip is actually a two-stage filter structure, with the first stage performing the high-order decimation. The decimation is performed with a sample-rate-reduction scheme that delivers decimations of up to 1024 through a coarse low-pass filtering process. The high-order section provides up to 96 dB of alaising rejection in the signal passband.

Employing a finite-impulse-response decimation filter in the second stage, the circuit can appear as a transversal FIR filter with up to 512 symmetric taps, or an arbitrary-phase filter with up to 256 taps. The FIR section can perform decimation by up to 16 while preserving the 96-dB rejection.

Data words fed into the filter chip are 16 bits wide, and data outputs are 24 bits. The wider data output bus allows more accurate results to be delivered. Internal routing paths permit the designer to bypass either the high-order filter or the FIR filter section if only one level of filtering is needed. The chip has three-state outputs, which permit multiple circuits to tie into a common bus.

With a complex multiplier and complex accumulator as well as a quadrature numerically-controlled oscillator (NCO), the HSP45116 allows complex vectors to be rotated for quadrature modulation and demodulation subsystems. The NCO portion of the chip includes a phase and frequency control section, as well as the sine/cosine ROM. The resultant sine and cosine outputs of the NCO section are fed into the complex multiplier-accumulator that computes the product of those terms with the magnitude and phase values of the incoming vector.

A 32-bit input controls the input frequency, with a frequency resolution of better than 0.01 Hz at 30 MHz. Furthermore, the error in the sinusoidal vector is less than -90 dB. Although input vectors are represented with 16-bit real and imaginary values, the chip delivers two 20-bit output values that represent the rotated complex vector.

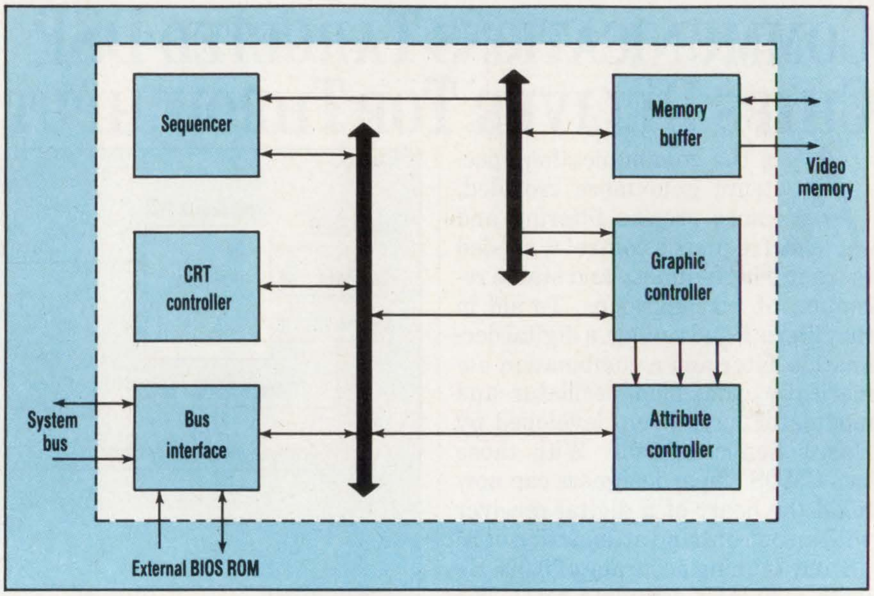
When the HSP45116 is used in conjunction with a pair of 43220 decimating digital filters, the trio forms the main section of a quadrature downconverter. The system can tune in on signals whose bandwidths are several orders of magnitude less than that of the input-signal sampling frequency. The entire system could offer sampling rates of over 30 MHz, 16-bit accuracy, out-of-band attenuation of up to 96 dB, and 0.006-Hz tuning accuracy. The chips permit the tuning frequency and phase to be altered in a single clock period, with no loss of data due to settling time. That permits schemes such as frequency-hopping for secure communications.

Samples of both chips are immediately available. The 84-lead pin-grid array version of the HSP43220 decimating filter sells for $140 in 1000-unit lots, while the 144-pin PGA version of the HSP45116 goes for $175 in similar quantities.

Harris Semiconductor Corp., 1301 Woody Burke Rd., Melbourne, FL 32902; Clay Olmstead, (407) 724-3868. In the U.S., call (800) 442-7747, ext. 1083. **CIRCLE 336**

VGA IC UPS RESOLUTION

The OTI-067 graphics controller from Oak Technology provides 1028-X-768-pixel resolution with 16 colors for IBM VGA-compatible graphics systems. Compared with the company's OTI-037 entry-level VGA controller, the 067 requires fewer external components.



Only two 256k-by-4 DRAMs are required for 800-X-600-pixel resolution or 1024-X-768-pixel resolution with 16 colors. Four DRAMs support 800-X-600-pixel resolution with 256 colors, and 1024-X-768-pixel resolution with 16 colors, all with noninterlaced operation for cleaner screen appearance. Older VGA controllers require eight DRAMs for noninterlace operation.

The controller is supported with application software drivers for popular programs such as Windows, OS/2, and GEM. Also available is a kit for user-customized drivers, which includes internal register definitions and an evaluation board. The company also offers an OEM turnkey manufacturing kit that includes schematics, film for pc-board layout, a data book, VGA BIOS PROMs, and a bill of material for making VGA boards and subsystems. For added design simplicity, the OTI-069 clock synthesizer is also available for replacing four discrete crystals. Now in full production, the OTI-067 is priced at $29.00 each in lots of 1000.

Oak Technology, Inc., *139 Kifer Ct., Sunnyvale, CA 94086; Scott Alberts, (408) 737-0888.* CIRCLE 337

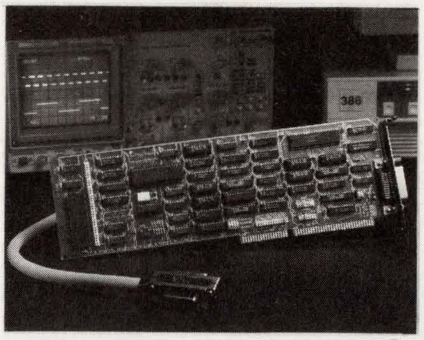
■ *MILT LEONARD*

IEEE-488 INTERFACE INCLUDES I/O LINES AND COUNTER/TIMERS

The Power488CT board carries not only an IEEE-488.2 interface, but also 40 digital I/O lines and five programmable 16-bit counter/timers. All that is packed onto a full-slot card that plugs into a 16-bit PC/AT-style bus. The board is programmable using the new Standard Commands for Programmable Instruments (SCPI). It's fully compatible with IEEE-488.2, including the ability to monitor bus handshake lines and detect changes on the SRQ line.

The board reads data from IEEE-488 devices at the standard's full speed of 1 Mbyte/s. It also supports interrupt-driven I/O capability, with 11 user-selectable interrupt lines. The counter/timers can be configured for counting pulses or for measuring frequency or time. The unit counts pulses and frequency to 7 MHz and measures time to a resolution of 140 ns.

The board comes with Driver488, an enhanced version of IOtech's device driver software. Among other improvements, the company added serial port control, which lets users integrate control of serial devices with the board's other functions.



The Power488CT costs $595. Without the counter/timers, the Power488 goes for $495. Delivery is from stock.

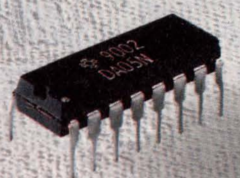
IOtech Inc., 25971 Cannon Rd., Cleveland, OH 44146; (216) 439-4091. **CIRCLE 338**

■ *JOHN NOVELLINO*

MIXED-SIGNAL SYSTEM TESTS 50-MHZ DEVICES

The M3600 mixed-signal test system offers versatile component test capabilities at digital clock speeds to 50 MHz and on up to 256 mixed-signal pins. The system, built by SZ Testsysteme and offered in North America by SemiTech International, is well-suited to production and characterization testing and can easily be adapted to incoming-inspection test. A modular architecture allows the M3600 to expand as needs change. In the standard configuration with 64 pin drivers, analog, and digital instrumentation, 20 slots remain available for special instrument requirements. Timing resolution is 500 ps. The M3600 runs more than 1000 applications developed for the earlier M3000 Universal Test System. Prices for the M3600 start at under $175,000 in North America, and include a 32-bit Hewlett-Packard color graphics workstation. Orders are being accepted, with delivery in 10 to 12 weeks.

Marketing Dept., SemiTech International, 56 Roland St., Boston, MA 02129; (617) 628-8880. **CIRCLE 339**



100-MHZ TESTER BOASTS 350-PS ACCURACY

The HP 82000 IC evaluation system family has been extended to include a 100-MHz version, the Model D100. The system delivers edge-placement accuracy of 350 ps and a maximum pin count of 512 pins, with full tester capability on each channel. The D100 is fully compatible with the 50-, 200-, and 400-MHz versions of the HP 82000, running the same software and operating system. Thus users can upgrade their system as needs change. Automatic-test functions and fast setup time offer users high-volume design throughput. And HP's recently introduced production-

test firmware enhancements allow the same test system to be used for testing small- and medium-size production runs. The system's software and true tester-per-pin architecture allow all channels to operate at the maximum frequency, so users can perform thorough tests on even the most complex devices. Per-channel cost is about \$2000. In a typical 128-channel configuration, the HP 82000 Model D100 costs \$260,000. Delivery is estimated at 14 weeks after receipt of an order.

Hewlett-Packard Co., 3000 Hanover St., Palo Alto, CA 94304; (800) 752-0900. **CIRCLE 340**

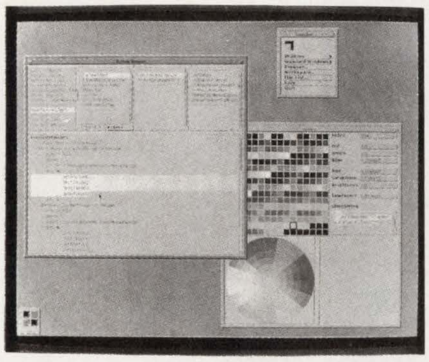
VXI-BUS ANALYZER AIDS TESTING

Suitable for testing systems as varied as radar and computer disk drives is the latest VXI bus product from Racal Instruments Ltd. of Slough, Berkshire UK. The 2351 is a time-interval analyzer built in a two-slot-wide, C-size VXI module which carries out high-resolution time and frequency measurements on consecutive signals. It's capable of continuous data collection while making time measurements, Racal claims. Performance includes 8-ps single-shot resolution on time interval or 11 digits/s frequency resolution, with external arming and logic-analysis trigger positioning. The 2351 stores up to 8,000 samples on each of two 250-MHz-bandwidth input channels, to ensure the capture of all signals with separations down to 200 ns. In addition to intervals and frequency, measured parameters include pulse width, duty cycle, rise and fall times, and phase. The 2351 also has ROM programs for statistical analysis and Allan-variance plots. Applications include radar pulse measurement, frequency-variation plotting, magnetic digital-recording device testing, and agile-radio testing.

Racal Instruments Ltd, 480 Bath Rd., Slough, SL1 6BE United Kingdom. **CIRCLE 341**

ENHANCED SMALLTALK GETS MORE POWERFUL, PORTABLE

A bevy of enhancements to ParcPlace Systems' year-old release of Smalltalk 2.5 has resulted in a more portable, more feature-laden and more-efficient version, Objectworks/Smalltalk Release 4. For starters, the latest release includes the hooks necessary so that it can work with all standard windowing systems, thus making it easier to program and



use by anyone already familiar with the window controls. Furthermore, the company developed a Smalltalk portable imaging model that allows Smalltalk to maintain consistent graphic images for application programs on different computers. Thus, an application running on a Sun workstation would look the same (within machine limitations) when it runs on an Apple Macintosh, for example.

Additional improvements include the ability to implement 24-bit non-indexed true-color imaging descriptions so that photographic-quality color imaging can be done consistently on any platform that runs Release 4. A more efficient "garbage collection" scheme that incrementally reclaims storage space was added to transparently eliminate intermediate results that are no longer needed. To attract international users, ParcPlace added the ability to Release 4 so that it can simultaneously handle multiple character sets and double-byte character definitions.

The company also added considerably to the portable object library that comes with the software, upping the count to about 300 reusable objects that come with source code and documentation. An optional advanced programming ObjectKit includes analysis tools, programming tools, browser programs, communication drivers, and more. Initial versions of Release 4 will be released first on the Sun 3 and 4 workstations, Apple Macintosh computers, IBM PS/2 and RISC System 6000, Digital Equipment DECstations, and Hewlett-Packard and HP-Apollo workstations. On the Sun workstations, the single-user price will be $3500, with availability slated for November. In the first quarter of 1991, users can add ObjectKit for $500.

***ParcPlace Systems Inc.**, 1550 Plymouth St., Mountain View, CA 94043; Catherine Tucker, (415) 691-6700.* CIRCLE 342

■ *DAVE BURSKY*

NEED BROAD-BAND COAXIAL RELAYS? FROM 2 TO 24 THROW, MATRIX HAS THE ANSWER

Our versatile 7000 series of coaxial relays have band-widths from DC up to 800 MHz. They're available from 2 to 24 throw. And by using our 9000 series cross-straps, switching matrices of any size can be configured.

Why have Matrix broad-band relays become the industry standard? Because we construct them of precision machined anodized aluminum alloy, all signal shield paths are silver plated, and basic switch elements are hermetically sealed in nitrogen filled gas envelopes with rhodium plated contacts to insure non-stick operation.

The end result is extremely low crosstalk, EMI and VSWR. Another plus, all switchpoints are individually field replaceable.

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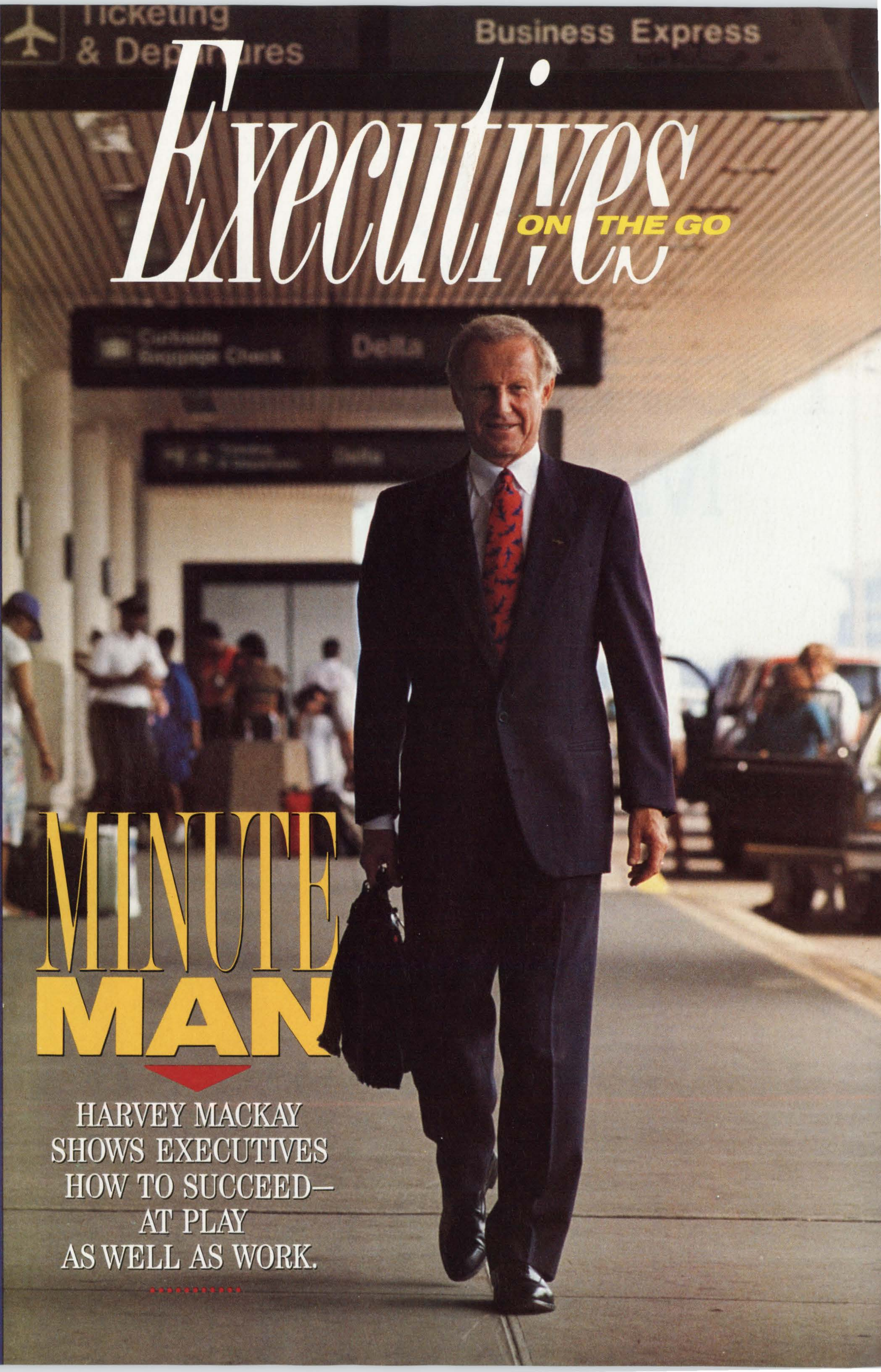

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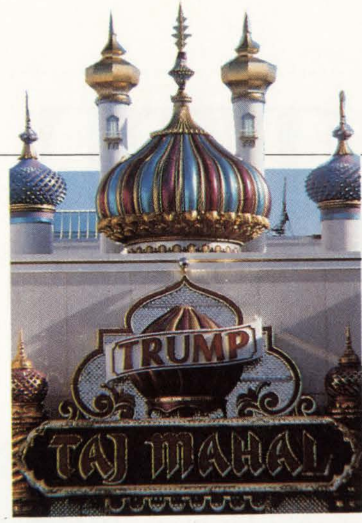
TAJ WOOS EXECS...

High-roller executives are being tugged east and west by the newest and most extravagant upscale casino resorts in Atlantic City and Las Vegas. Donald Trump labels his $1 billion Taj Mahal, the 17-acre casino and hotel complex that opened on Atlantic City's Boardwalk in April, "the eighth wonder of the world." Among its credentials: a 120,000-sq-ft casino that's the biggest in the world; 1,250 rooms and suites; $14 million worth of Austrian crystal chandeliers, including two dozen in the casino valued at $250,000 apiece; a dozen restaurants; and 175,000 sq ft of convention and exhibit space. On the top 12 floors of the 51-story tower are 237 luxury suites and the exclusive Maharajah Club. The 51st floor features seven luxury two-bedroom penthouse suites, topped by the 4,500-sq-ft Alexander the Great, which has its own butler as well as steam room, sauna, and weight room. Cost is $10,000 a night but no one ever pays; the lavish suites are given to big spendors and special guests. Regular room rates now are $140 and $150. FOR INFORMATION, CIRCLE NO. 15



...SO DOES MIRAGE

In Las Vegas, the $630 million Mirage is "a special place," says owner Steve Wynn. "It's a resort hotel which includes a casino—not a casino which includes a hotel." The Mirage, which opened last November on a 100-acre site north of Caesars Palace, has 3,049 rooms in three 30-story towers. There's no "cheap neon," which Wynn says typified "yesterday's Las Vegas." Rather, the Mirage appears as a tropical paradise in the desert. Its entrance is marked by a lagoon with a five-story waterfall and a volcano which erupts every few minutes. The casino measures 60,000 sq ft but the gaming areas are grouped under separate Polynesian-style roofs to give the feeling of intimacy. Attractions include a 53-ft, shark-filled aquarium; the royal white tigers of illusionists Siegfried and Roy; five restaurants; and over 60,000 sq ft of convention space. Rooms are $89-$159, suites $325-$750, and six lanai bungalows $750-$1,250. In June Circus Circus Enterprises opened the largest hotel in the world—the $290 million Excalibur, containing 4,032 rooms. With rooms $45-$110, it aims at a more middle-class market. The Mirage competes directly with the spectacular Caesars Palace and Wynn's Golden Nugget, both completely renovated.

Atlantis submarines have sufficient life support systems to stay submerged up to 72 hrs.

Checking in at the Mirage includes checking out a 20,000-gallon aquarium.

DIVING IN STYLE

Even if you're not a scuba diver or snorkeler, you can discover the brilliantly colored fish, exotic marine life, coral formations, and other natural wonders of life beneath the sea—while enjoying the air conditioned comfort and safety of a tourist submarine. Atlantis Submarines International operates the largest fleet—six submarines in Grand Cayman Islands, Barbados, St. Thomas/U.S. Virgin Islands, Guam, and Hawaii (Kona Coast of Hawaii and Waikiki Beach in Honolulu). It will launch its seventh sub in Aruba in November. The 65-ft-long, $3 million subs, which dive to a maximum 150 ft, seat as many as 46 passengers and three crew members. They have 26 2-ft portholes and a 52-ft front viewport. The hour-long voyages cost $58-$85 a person (604/875-1367).

A TOUCH OF CLASS

To appeal to executives required to travel at coach rates, MGM Grand Air—the luxury airline flying between New York and Los Angeles— has added a "Grand Class Coach" to its premium "Grand Class First" service. The line now flies three DC-8 Super 62 planes, reconfigured for 79 seats, 40 of them coach. For $623 one way (same as full-price coach on other airlines), the "Grand Class Coach" traveler receives the equivalent of typical first-class service, or better: oversized seats with a phone and TV for every pair, free movie screenings, gourmet entrees served on china, and complimentary cocktails. "Grand Class First" passengers pay $1,067 one way (same as full first class on other airlines) and receive even more: individual reclining and swiveling "sleeper" seats, dining table seating for 20 passengers, a stand-up bar near several large TV's, a fax machine, and the privacy of two staterooms that can convert to twin or queen-sized beds. MGM Grand Air (800-933-2MGM) flies twice daily to and from New York's Kennedy Airport and Los Angeles.

MINUTE MAN

By Jim Braham

JUDY OLAUSEN

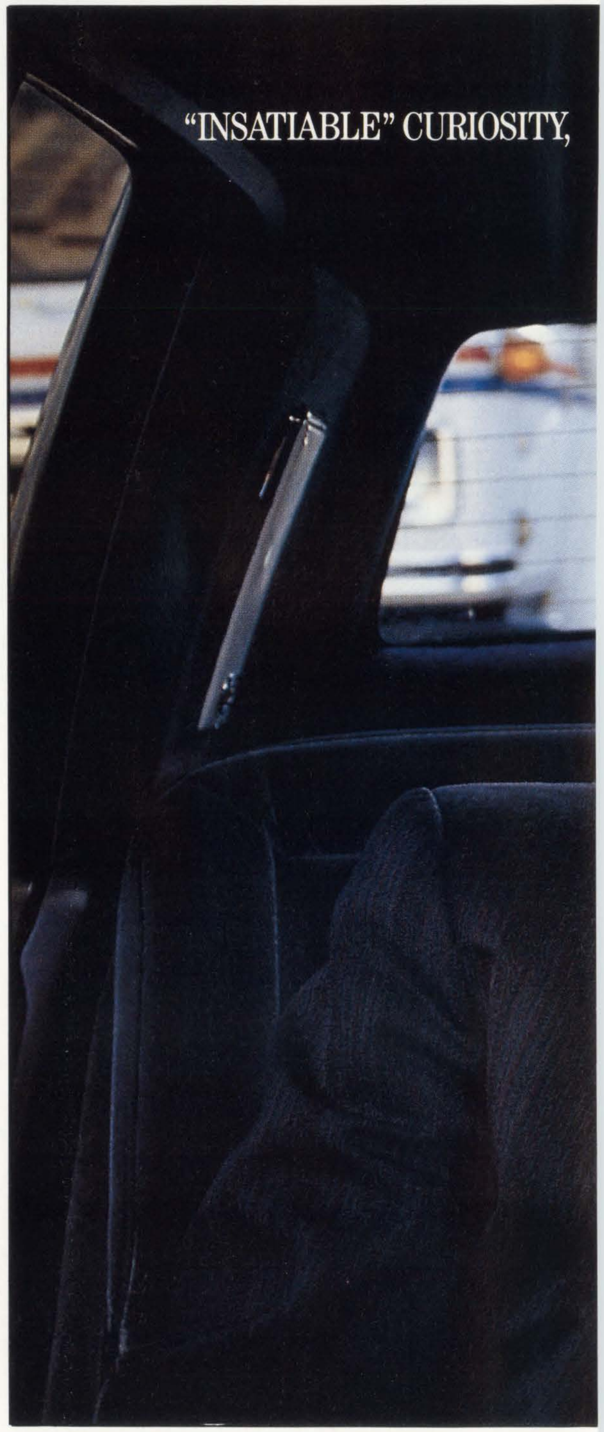
▶At 6 o'clock nearly every morning, Harvey Mackay hits the floor running. In a few minutes he's off on his seven-miler. "With all the traveling I do, if I didn't run I'd be a basket case," says the man whose dizzy day of activities usually doesn't wind up until one the next morning. Even then he's reluctant to go to bed. Why? "I might miss something."

A "time freak" who opens his company sales meetings by holding up a watch and calling time "our *only* competition," who deliberately keeps his watch 11 minutes fast, who schedules appointments and meetings at times such as 3:10 rather than three o'clock ("that way people remember"), who over a two-year period scientifically reduced his nightly sleep from eight to seven to six and finally to five hours, Harvey Mackay is an executive on the run.

He's also an executive on a mission: to show that success—at play as well as work—can be assured, even come easily, if you simply "do your homework" and are "prepared to win." This means leaving little to chance. "If you"re really organized, you don't have to hurry. You can beat 80% of the competition just be showing up. Show up on time with a plan, a commitment to carry it out, and then execute it—and you'll beat the competition 100% of the time," says this super-salesman, whose energy and fitness hide his age ("57 and holding"). To him, "superior information" is the ultimate "weapon."

With this approach, he has built Mackay Envelope Corp. of Minneapolis into a $35 million business, and himself into a smash hit in bookstores and lecture halls across America. His new book—*Beware the Naked Man Who Offers You His Shirt,* subtitled *Do What You Love, Love What You Do, and*

EXECUTIVES ON THE GO periodically will profile dynamic executives who can make an impact and a difference in our lives. Harvey Mackay, who leads off this series, is such a leader.



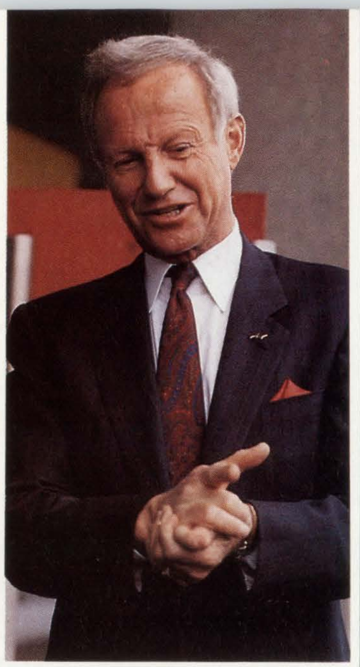
PAUL TEPLEY

Whether he's in a hotel or car, Harvey Mackay carries along his cellular phone. It's one of about 35 "time savers" that go into his briefcase for every trip.

WITH "FANATICAL" ATTENTION TO DETAIL AND AN BUSINESSMAN/AUTHOR HARVEY MACKAY SHOWS EXECUTIVES HOW TO SUCCEED —AT PLAY AS WELL AS WORK.

PAUL TEPLEY

COVER PHOTOGRAPHY: ANDREW HOLBROOK/BLACK STAR



PAUL TEPLEY

Deliver More Than You Promise—is another easy-to-read primer of short, simple business "lessons" topped by clever, snappy titles. Like *Swim with the Sharks without Being Eaten Alive*, it's a best seller.

His publishing success has propelled his lecture popularity to the point where he commands $20,000 for a typical one-hour presentation, and he gives 40 to 50 a year. He's also a sports-oriented Minneapolis civic leader, donating a quarter of his time to volunteer work. As an avocation, he has counselled more than 500 college students.

The man, obviously, is organized. He seems to prepare for *everything:* "I have a fanatical attention to detail, but it's not that difficult. All success is, really, is having a predetermined plan and carrying it out successfully over a long period of time—reaching your potential." The result becomes, to quote one of his pet phrases, "a piece of cake."

Thus, want to be creative? Start reading books on creativity. Hang around with creative people. "All of a sudden, it's a funny thing, you start to become creative."

Want to become a better tennis player—advance from class B to A? With the Mackay way there's usually a list of things to do. In this case, one, find a really good "mentor" or teacher. Two, take "copious" notes, and refer to them often (Mackay still has his golf notes from playing for the University of Minnesota in the 1952 NCAA championships). Three, tape the lessons so you can hear them while driving. Four, videotape yourself playing tennis for "visualization." Five, attend tennis tournaments. Six, watch tennis on TV. Seven, ask your instructor for "the five best books on tennis—not just the technical but the mental aspect, too." Eight, hang around with tennis players, and play with better players. Nine, compete in tournaments. Result: Harvey Mackay, who took up tennis in his mid-30s, is now No. 1 ranked in his age group in Minnesota.

Want to run a 26-mile marathon—even though you're 55 years old and the most you've ever run is three miles? Again, simple. Follow practically the same steps as for tennis, plus "change your eating and sleeping patterns," and in time the event itself becomes "incidental." Even before the 1988 New York Marathon began, he already had "won." How? "By trying my guts out for 100 days. Perfect practice makes perfect," says Mackay, preparing now to run his second New York Marathon Nov. 4.

PEOPLE DON'T CARE HOW MUCH YOU KNOW ABOUT THEM ONCE THEY REALIZE HOW MUCH YOU *CARE* ABOUT THEM.

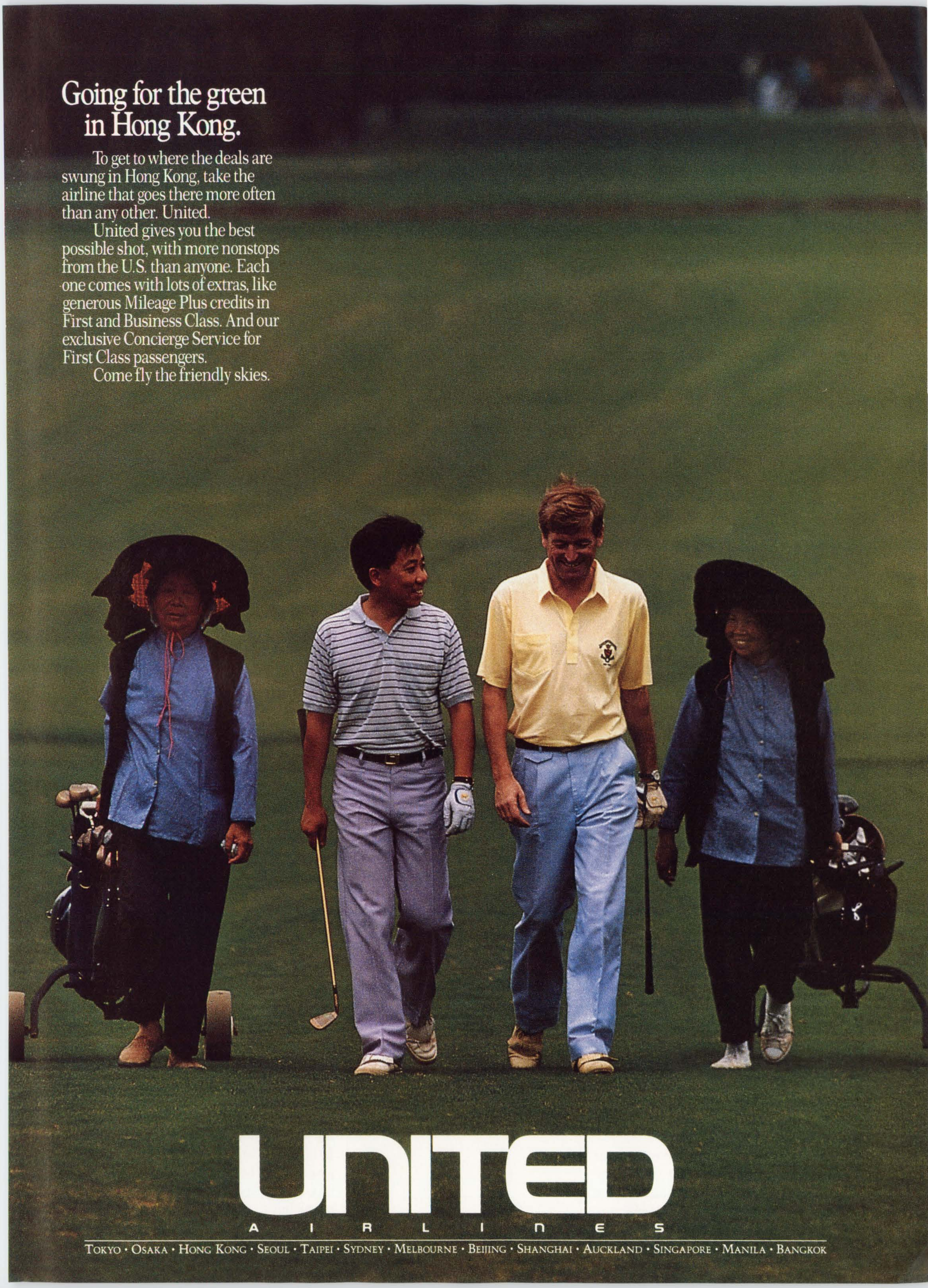
In promoting his books, Harvey Mackay followed his own advice. Before selecting a publisher he researched the industry, visiting bookstores across the country. He even hired his own publicist and attended the Frankfort, Germany, book fair to personally solicit foreign buyers.

"It's all research, doing your homework, preparing to win," he stresses, citing his early September trip to the Soviet Union as an example. Finvest, the Soviet chamber of commerce, invited him to speak on national Soviet TV about free enterprise and the American way of doing business. His audience: "the whole damn Soviet Union!" he exclaims. "I will have an opening seven-minute talk—so what do you think I'm going to do? I'm going to deliver the speech in *Russian!*" Last month he hired his own "Russian instructor. It is one of a half-dozen languages he has studied.

In his appreciation of time, travel ("the best education you can give a child"), contacts, research, and curiosity ("I have an insatiable curiosity to know about human beings"), Harvey Mackay has adopted habits he learned from his "mentor"—his father Jack, who was a veteran Associated Press reporter and bureau chief in the Twin Cities. "My whole life is one-on-one networking," Harvey says. "When I was about 18, my dad taught me that every person you meet for the rest of your life, assuming you want to keep in touch with him or her, goes into a card file. You do that for about 40 years and you've got a pretty good network."

Rolodex is the "key," says the man who in 40 years has accumulated some 6,500 cards or names, in several files. "It's simple," he says. "Every time you go to a conference or a party or you sit on an airplane, you meet somebody and ask him for a card, and you jot down maybe one or two salient points." His cards include such personal data that, when a man phoned recently from Bombay, for example, Mackay was able to quickly flip through his Rolodex and ask: "How's your daughter Carol?" Says Mackay, "This shows I care about them. People don't care how much you know about them once they realize how much you *care* about them."

Approximately 20% of his 6,500 cards, alphabetically arranged, represent people with whom he maintains regular contact.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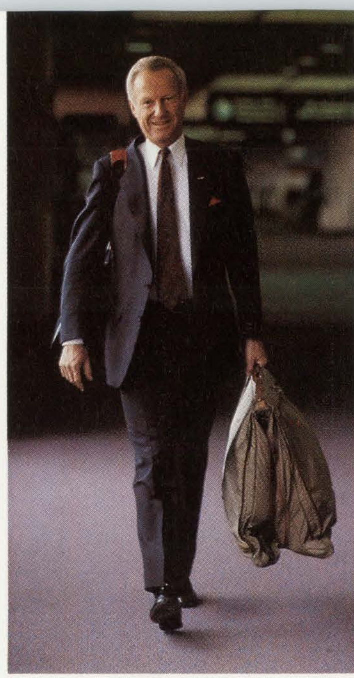


PAUL TEPLEY

The others are sorted by cities, states, and countries. When he travels, Mackay simply looks up his cards for that area and jots down the names and phone numbers of people he intends to call. So lavish has been his praise for Rolodex—"the most important word in the English language"—that he has written a book on how to best use it. *The Harvey Mackay Rolodex Network Builder* will be available in late September.

Of course, much of Mackay's information comes from reading 35-40 hours a week—mostly business and current events—in all the major business journals, news magazines, and local and national newspapers. He also gleans much from the Cable News (TV) Network.

Instructional or inspirational cassette tapes provide further information. Mackay has more than 300 tapes to listen to while traveling. "Most people drive 12,000 miles a year. If you live to be 72, that's 3½ years in a car," he reasons. "Why not turn your car into a university?"

Much of this year Mackay has been criss-crossing America on a combined book and lecture tour, and even the interviews to him present opportunity: "You *learn* from a Larry King or an Oprah Winfrey. You get a chance to study at their feet. Any new experience is another opportunity." The tour also permits him to visit his son in Los Angeles or daughters in New York and Detroit.

Despite all its problems, Mackay seems to thrive on travel. In fact, he and Carol Ann, his wife of 29 years, have a goal to see every country in the world; they have visited about 60 of the approximately 170. "Flying is like jogging. At 30,000 feet it's all in the attitude," says the upbeat Mackay. "It can be so fabulous with the nice views, the peace and quiet, and the fascinating people you meet. Of course, 40 below zero can be exciting—if you *want* it to be exciting."

The detail-minded Mackay offers some tips to make traveling more pleasant. For example, he always sits "on the side of the plane where I can see the sunset and sunrise. It's a little thing but it really makes traveling nice."

When the airline doesn't have the seat he'd prefer, he asks whether any "non-revs" (non-revenue passengers, usually airline personnel) are aboard, and requests one of those seats if desirable. "The airline will ask the 'non-revs' to move—but you have to know to ask this."

YOU CAN BEAT 80% OF THE COMPETITION JUST BY SHOWING UP.

At hotels, Mackay also makes sure he enjoys the finest view. "It costs virtually the same, you just have to ask," says Mackay, who insists on being on an upper floor, with a view of water, skyline, mountains, or the like. He even knows what room numbers to request. He also prefers hotels near a park, track, or golf course on which he can run.

No matter where he goes, he carries his "prioritized" reading material, for business and pleasure. In larger cities, he arranges to be picked up by a town car at the airport. Why? "To take advantage of night reading. Cabs don't have a reading light in the back."

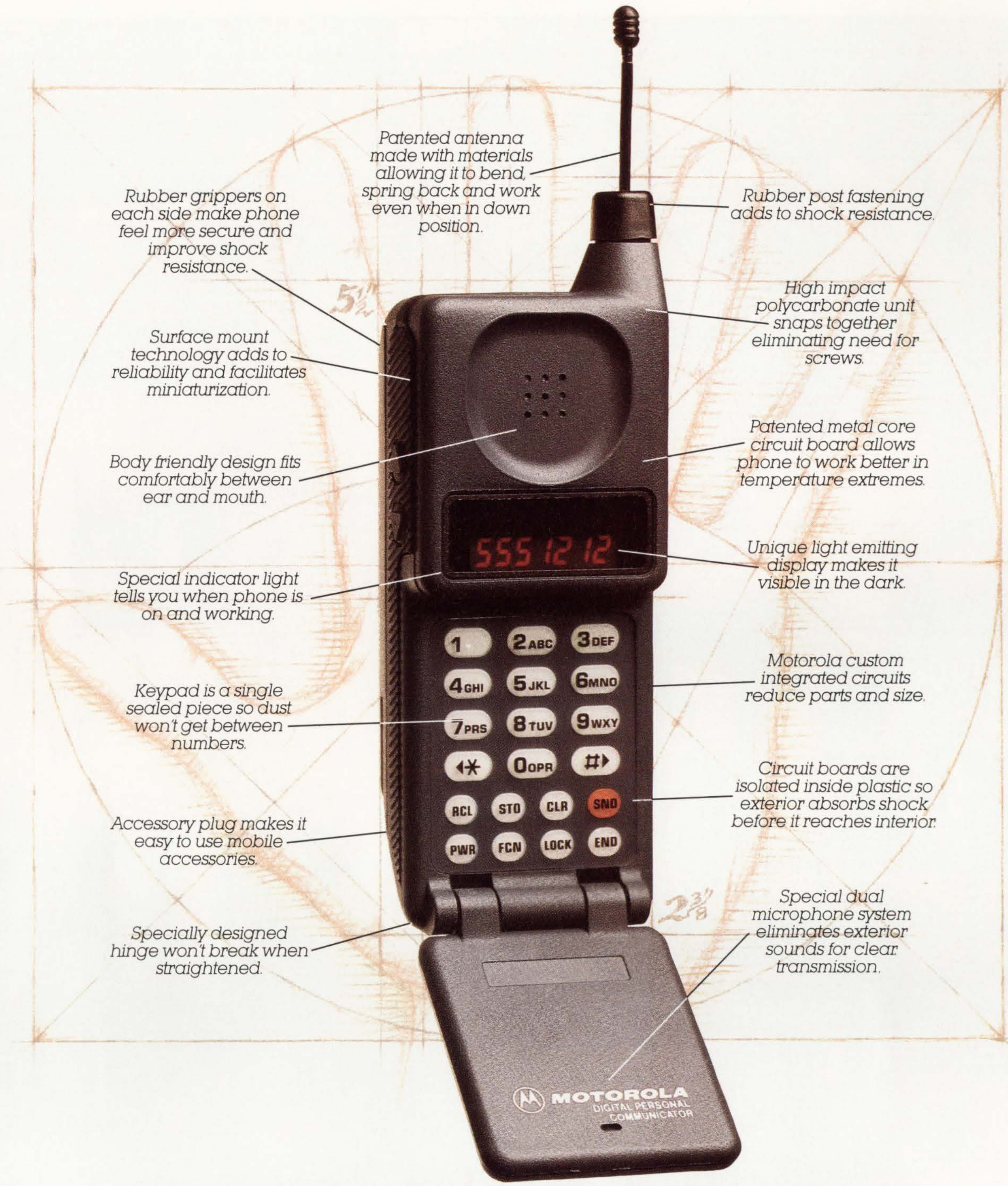
His briefcase always contains his 35 or so "time savers," including a cellular phone with extra batteries, a tiny dictating machine, a list of 250 phone numbers of people he calls regularly, postage stamps, Swiss Army knife, Post-it notes, 25 new dollar bills, and change. He carries his list of favorite restaurants for that city.

Just as meticulous about his health, Mackay neither smokes nor drinks coffee, and rarely drinks alcohol. What he does drink is an astounding amount of water—as many as 20 glasses a day. He didn't need to be convinced by his marathon "running coach" to consume 16-20 glasses daily to prevent dehydration. He already knew the wonders of water, that it cools the body, improves circulation and digestion, and fuels the muscles. "Whether you're a runner or not, water is fabulous. It gives you unbelievable energy!" Mackay exclaims.

"Totally addicted" to running for its relaxing benefits, Mackay also uses his seven miles daily as an opportunity to work on speeches—and even Minnesota's winters don't deter him.

As for work, Mackay says that he's not a "workaholic," that his family comes first. He takes his wife on about a third of his business trips. For two weeks every holiday season the family vacations together; every four years he takes them all to the Olympics.

He "cannot fathom" ever retiring. To him his job is not work, just as it wasn't to his father, who "was successful and happy and loved what he was doing. Find what you love to do," says Harvey Mackay, "and you'll never have to work a day in your life." ✎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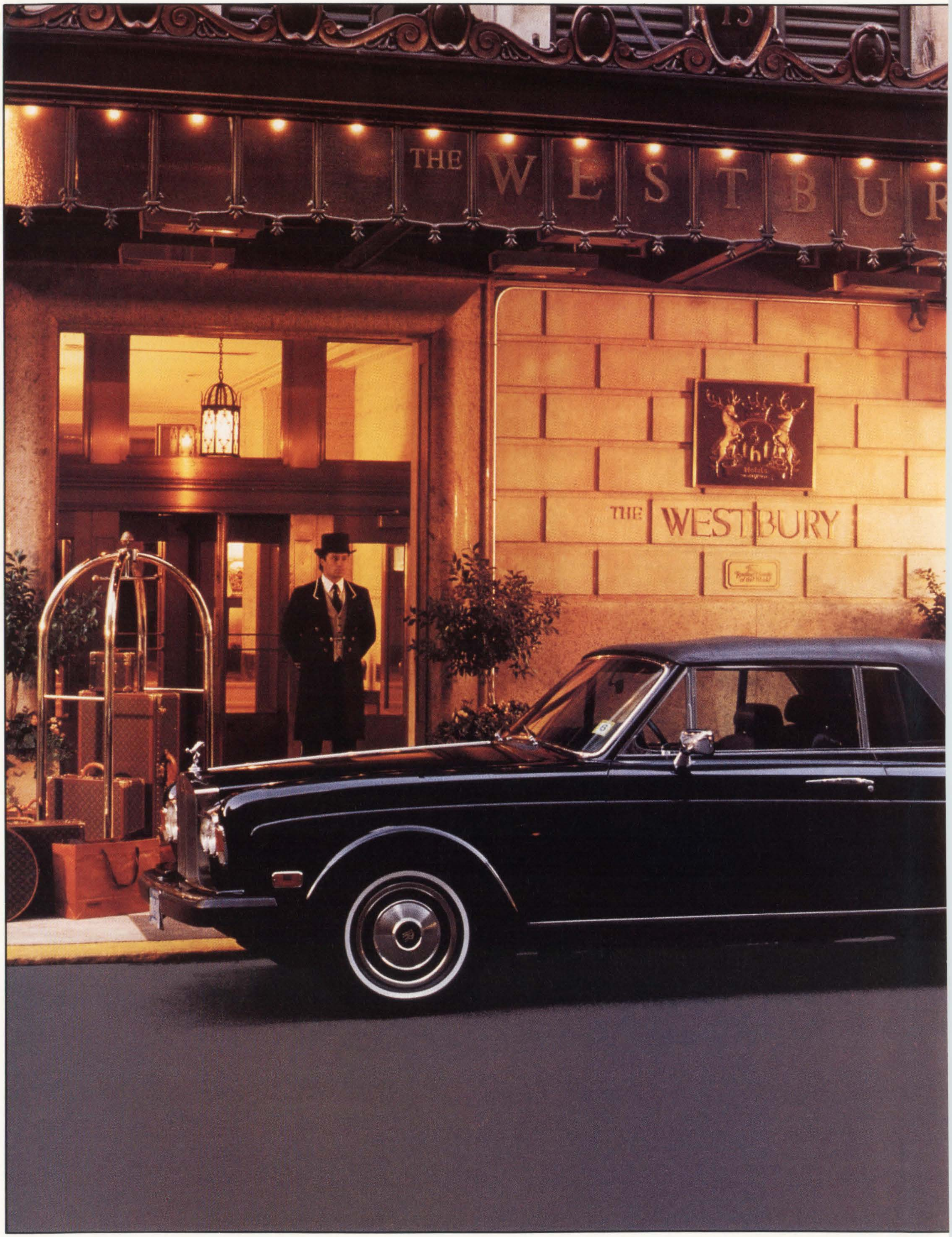

THE WESTBUR
THE WESTBURY

HOTELS WITH A SOUL

At Manhattan's small luxury hotels—offering warmth, intimacy, elegance, and impeccable service—every guest is a VIP.

▶Bearded, cultured, and charming—a man surely ordained by central casting to play host and general manager of a small, elegant European-style hotel—Dario Mariotti sips his coffee and ponders the question: what makes his hotel, and others like it, so very, very special?

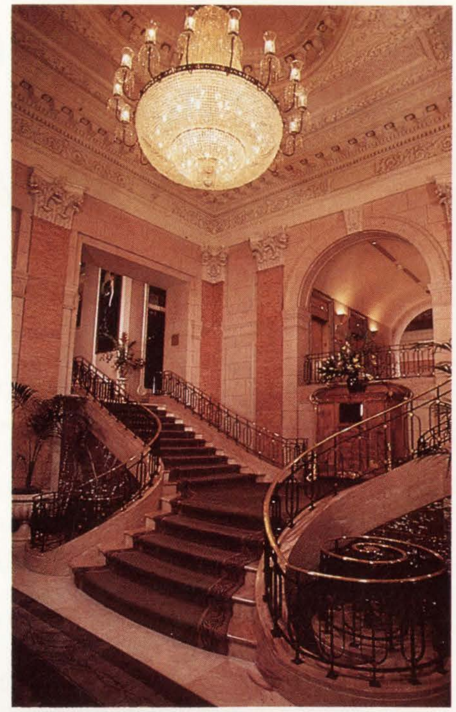
"It's the size. It's like the difference between a deluxe bus and a limousine," says the cheery Italian, settling back into a plush chair in the sunken lobby lounge of Manhattan's Mayfair Regent Hotel. "Big hotels are very good for their size, but a general manager of a big hotel is like the mayor of a city more than the general manager of a hotel. I see 75% of our guests. I know most of their names. Big hotels are valid for conventions; Americans do that very well. We Europeans do better at smaller hotels."

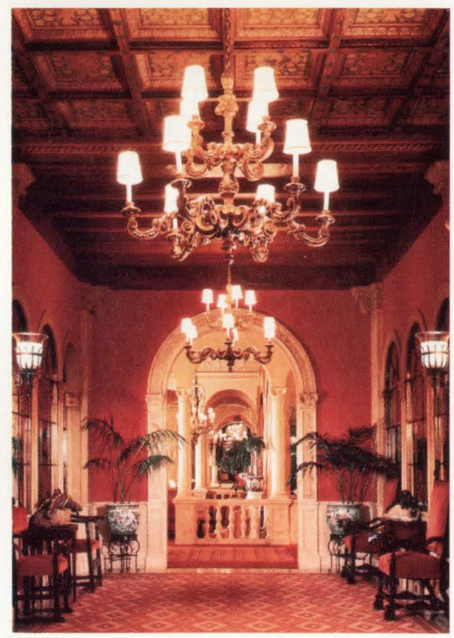
"A hotel with a soul," the Mayfair Regent has been aptly described. Similar sentiment might be accorded the Carlyle, Lowell, Plaza Athenee, Pierre, and Stanhope—all generally considered the *creme de la creme* of New York's finest small luxury hotels—as well the jewel-like Peninsula, Ritz-Carlton, Parc Fifty One, Mark, and Westbury. With no more than 250 rooms apiece, each specializes in personalized, VIP service, each in its own distinctive manner. Room rates typically begin at about $250 a night.

Most of these hotels are on New York's fashionable Upper East Side, in the center of high style, society, and wealth, within walking distance of the museums, galleries and concert halls, high-fashion shops and boutiques, apartments of the rich and famous, as well as Central Park.

With each, less is more. Often the hotel appears more like a private club or residential building. The entrance is small and discreet, but friendly. A few highly capable staffers await behind the desk

BY JIM BRAHAM





New York's finest small hotels present a welcome sight, from the Westbury (left) where a Rolls-Royce is not in the least uncommon, to the Peninsula (above) where a sweeping marble staircase leads up to the lobby, to the Mayfair Regent whose lobby is among the loveliest of public rooms.

and you'll see no lines or signs, certainly no conventions.

Return guests represent the majority of business, and client preference and whims are recorded and extended at each visit. No request seems excessive. Two tickets to *Phantom of the Opera,* toughest tickets on Broadway, you say? No problem, says Frank Bowling, vice president/manager of the Carlyle. "By the way," he adds, "did you know that Andrew Lloyd Webber wrote some of *Phantom* while staying here?"

At many of these hotels, afternoon tea is a favorite activity, usually in a small lounge area off the lobby. The dining rooms are elegant but relaxing, the food and drink superb. Operators often man the elevators and room service is around the clock.

The luxuriously comfortable rooms are frequently adorned by fresh flowers, and perhaps a fruit bowl. The baths are marble, the mini-bars well-stocked. Multiple phones and lines are common, as are stereos, VCRs, 6-ft bath towels, terrycloth robes, exotic soaps and toiletries, bathroom scales, hair dryers, evening turndown service, complimentary shoeshines overnight, and complimentary newspapers at your door in the morning.

At these hotels, privacy of the many celebrities is protected, but hosts aren't above dropping a few names. As Mariotti says, "We get our share of Hollywood and business people, bankers, and glamorous ladies. We don't court the large official groups because it disrupts the hotel. But Mrs. Reagan likes to stay here, so what are you going to do?"

♦♦♦

THE CARLYLE

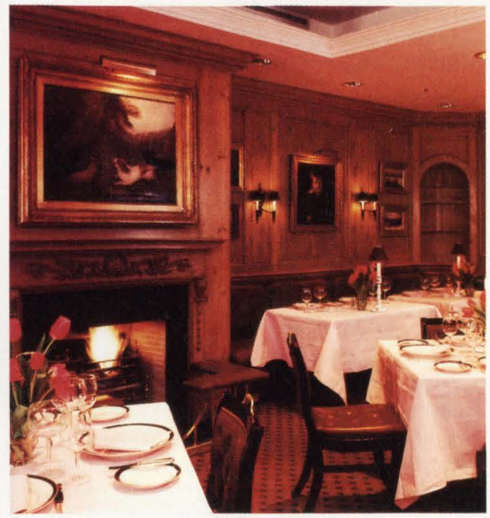
Unlike most of its competitors, the classically elegant Carlyle doesn't advertise. New York's only Mobil Five Star hotel doesn't have to. The 60-year-old *grande dame* has everything: location, service, and facilities. Towering above its residential neighbors, the 35-story Carlyle permits outstanding views of Central Park and the skyline. Every one of its 196 rooms is unique in decor and has a stereo entertainment center including a CD player and VCR. Practically every room has a Jacuzzi and fax machine, and fresh fruit and flowers are standard. Service is impeccable from a veteran staff that outnumbers guests. A new fitness center sports the latest equipment. The Carlyle Restaurant features the finest French cuisine, Bobby Short is still singing strong in the Cafe Carlyle, and Bemelmans Bar remains a favorite watering hole. (Room rates \$250-\$1,300; Madison Ave. at E. 76th St.; 800-227-5737).

♦♦♦

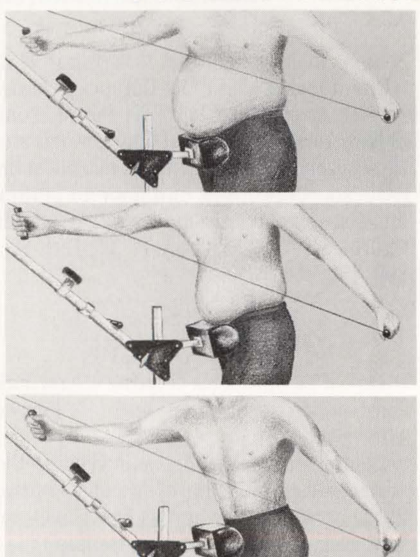
THE MAYFAIR REGENT

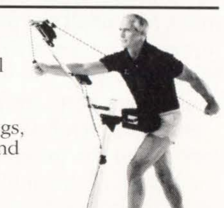
Displaying papers from around the world, the newspaper rack in the lobby lounge of the Mayfair Regent receives considerable

Dining is also feast for the eyes at Le Regence restaurant in the Plaza Athenee (left), the Jockey Club in the Ritz-Carlton (below), and the Caryle Restaurant (bottom left).



NORMAN McGRATH





attention. Little wonder: in this "European island in New York," as managing director Dario Mariotti calls his 16-floor hotel, about 40% of the guests in the 80 rooms and 1119 suites are European. When we visited, Queen Sofia of Spain was staying, but you'd never find that out from the white-gloved elevator operators for whom mum's the word. One of America's best (and priciest) restaurants is off the lobby: owner Sirio Maccioni's Le Cirque, where both people-watching and cuisine (pasta primavera is his specialty) are spectacular. Among new services: a fitness room and pocket-sized cellular phones ($15 daily rental). A soap lady daily brings to the room a basket of unusual European selections. (Rates $265-$1,700; 610 Park Ave. at 65th St.; 800-545-4000).

♦♦♦

THE LOWELL

With only 60 rooms, the Lowell "is able to care for and pamper our clients to the hilt," says general manager Martin Hale. Outnumbering guests by a more than 2-to-1 ratio, the concierges (dressed in morning coats and striped trousers) and other staffers do everything from stoking a log fire (most rooms are suites, with wood-burning fireplaces) to stocking your refrigerator (every apartment has a kitchen) to tailoring an individual menu for your room. The only New York member of the exclusive Relaix & Chateaux Chain, this intimate haven of understated opulence is an historical-landmark building, completely renovated. The independent Post House steak palace is off the boutique-sized lobby. (Rates $240-1,200; 28 E. 63rd St.; 212/838-1400).

♦♦♦

THE PLAZA ATHENEE

At this sister hotel of the famed Hotel Plaza Athenee in Paris, incoming guests realize immediately that they are in no ordinary hostelry. For one thing, they sit down at the front desk to register. That's just a hint of all the personalized attention forthcoming in this exquisite,17-story European gem, for the last six years a Trusthouse Forte property. The 160 rooms —most of which have pantries and refrigerators—echo the luxurious, but understated, good taste of the public areas. Le Regence restaurant is a feast for eyes as well as palate. When guest leave, they receive another indication of all the extra-special service and surroundings: the average room rate of $350 is highest in the U.S. (Rates $245-$1,950; 37 E.64th St.;800-CALL THF).

♦♦♦

THE PIERRE

The toast of Upper Manhattan since it opened in 1930, the Pierre remains a grand tradition, ideally situated on Fifth Avenue along Central Park. The 205-room hotel has been given a fresh, new look by the Four Seasons management that took over in 1981, without losing a bit of its European charm, service, or elegance.The Cafe Pierre is one of New York's finest hotel dining rooms and the classic Rotunda—with its marble staircase, soaring ceiling, and floor-to-ceiling murals—is a favorite meeting spot. (Rates $265—$1,750; Fifth Ave. at 61st St.; 800-332-3442).

The Stanhope (above) has been restored in the tradition of the grand hotels

♦♦♦

THE STANHOPE

One of the first signs of spring in New York comes when the Stanhope opens its Terrace sidewalk cafe. It's a perfect spot for people-watching and resting between visits to the Metropolitan Museum of Art and Central Park, both directly across Fifth Avenue. The elegant and intimate Stanhope (141 rooms, including 88 suites)—since 1926 a home away from home for business and art leaders—recently underwent a $28 million restoration by the Grand Bay Hotels. The new owners aren't tampering with formality: the hotel remains the only one in Manhattan where ties and jackets still are required (except for breakfast) in the dining areas. (Rates $245-$2,000; 995 Fifth Ave.; 800-828-1123).

of Europe, while art deco features some suites in the Parc Fifty One Hotel.

♦♦♦

THE RITZ-CARLTON

At the Ritz-Carlton on Central Park South, be sure to request a room on the north side. From these 77 rooms (amoung the hotel's 228), the view is spectacular: Central Park with all its greenery, framed by the skyscrapers along Fifth Ave. and Central Park West. Off the intimate, pine-paneled lobby is the popular Jockey Club restaurant and bar, where Norman the bartender seems to know everyone and crab cakes are everyone's favorite. The Ritz-Carlton chain, which took over the onetime Navarro residential hotel last year, will begin a $30 million renovation in late September; additions will include a health club. (Rates $190-$1,200; 112 Central Park South; 800-241-3333.

♦♦♦

PARC FIFTY ONE HOTEL

Not all of the cabbies have heard of the Parc Fifty One, but they will. The former Grand Bay at Equitable Center (before that the old Taft Hotel) has been completely renovated and since January part of Park Lane Hotels International. The first European-style luxury hotel on the West Side, near midtown business as well as the theater district, is a surprising jewel, exquisitely decorated and furnished. Its relatively large lobby and public areas are deceptive, for it has only 178 rooms on seven floors. From the marble-floored lobby with its piano bar and lounge, a staircase leads to the Mezzanine Cafe for breakfast. The popular Bellini by Cipriani restaurant (privately owned) is on the ground floor. Amenities include clean reading: the complimentary Sunday New York Times comes with white gloves. (Rates $220-$925; 152 W. 51st St.; 800-338-1338).

♦♦♦

THE PENINSULA

With sweeping marble staircases leading up to the lobby and dining rooms, the 23-story Peninsula—at the corner of 51st and Fifth Avenue—appears at first to be a large hotel. Not so, the former Hotel Maxim's de Paris (orginally the Gotham) has but 250 rooms Completely remodeled and now owned by Hong Kong's Peninsula Group, the hotel offers grand, elegant public areas and large, well-appointed guest rooms, with over-sized marble baths. The 21st and 22nd floors house a new, 35,000-sq-ft. health spa, with a 42-ft, glass-enclosed pool. On the rooftop, the Pen-Top Bar & Terrance (also glass-enclosed) serves lunch with a view. For more formal dining, there's the Adrienne and Le Bistro restaurants, as well as the Gotham Lounge. (Rates $220-$2,500; 700 Fifth Ave.; 800-262-9467).

♦♦♦

HOTEL WESTBURY

From its small but stately marble lobby to its 235 elegant guest rooms (all furnished with writing desks), the Hotel Westbury reflects the warmth and grace of an English country manor. Like the Plaza Athenee, it was acquired (in 1983) by Trusthouse Forte Hotels, which has spent $12 milllion in restoring the 64-year-old Upper East Side landmark. The Polo Restaurant, one of the city's finest, specializes in French-inspired American cuisine; there's piano music in the Polo Lounge. (Rates $240-$2,000; 15 E. 69th St. at Madison Ave.; 800-CALL-THF).

♦♦♦

THE MARK

A block north of the Carlyle, the new, 16-story Mark offers a quiet alternative to its long-established neighbor. Opened in 1926 as the Hyde Park and renamed the Madison Avenue Hotel seven years ago, the 180-room, neo-Italian Renaissance property with the striking art-deco facade was taken over last year by the Rafael Group. The new owners have spent $30 million in renovation, and it shows. Additions include Mark's Restaurant, just beyond the elegant lobby. (Rates $250-$1,500; Madison Ave. at E. 77th St.; 800-THE-MARK). ✎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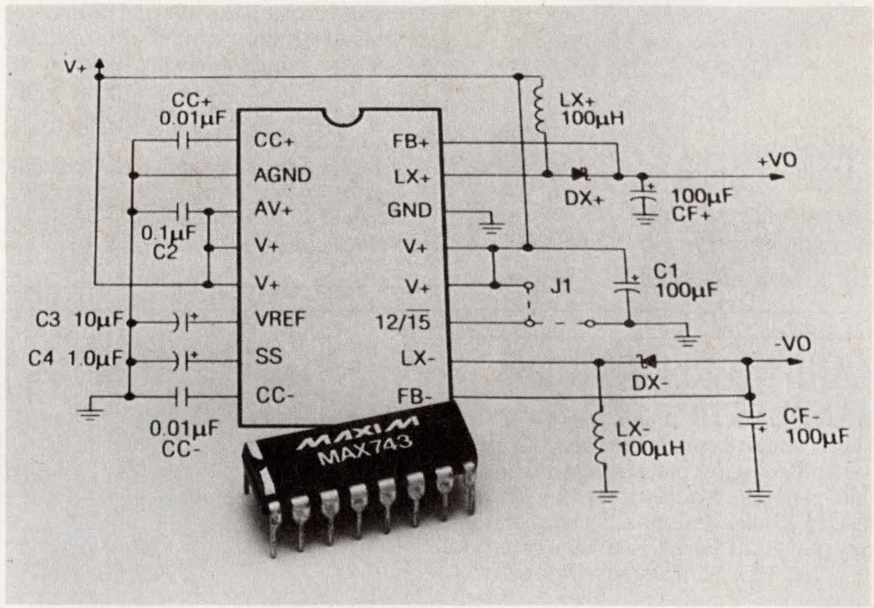
BUILD 5-V-IN, 100-MA, ±15-V-OUT CONVERTERS ON YOUR PC BOARDS

FRANK GOODENOUGH

How would you like tell your boss that you can save ten dollars out of 16 on every dc-to-dc converter module that converts +5 V to ±12 or ±15 V? If you use several thousand converters a year, that's quite a savings. If you're ready to try building your own converters on your own pc boards, Maxim now eases the task with the MAX743. You can get 1000 pieces of the MAX743, a dual (two switches), current-mode boost-converter IC, for just $5820, and for another $2360 you can get all the other parts needed to build 1000 supplies—including the two inductors in each supply. The converters come kitted up, ready for board stuffing. No circuit design, component selection, or multi-supplier purchase is required.



Every MAX743 is burned-in and then final-tested, in the circuit. Thus every converter built from the production kits is guaranteed to meet its basic specification. The output voltage will hold within ±4% of its nominal values of ±12 or ±15 V over worst-case conditions of input voltage, load current, and temperature. Input-voltage range is 4.5 to 5.5 V, and load-current range is 0 to ±100 mA for ±15 V out and 0 to ±125 mA for ±12 V out. Commercial-, extended-industrial and military-temperature-range models are available.

In addition to cost savings, these constant-frequency (200-kHz) pulse-width modulated switching regulators offer another advantage, efficiency over a wide range of loads. With ±100 mA out, efficiency typically runs from 78% to 84% over the 4.5-to-5.5-V input-voltage range. Efficiency still runs better than 70% with ±10 mA out. Typical 3-W modules are about 60% efficient at ±100 mA, and less than 20% efficient at ±10 mA. In addition, if some of your designs need ±12 V while others need ±15 V, there's no need to order (and stock) additional parts. Connecting pin 11 of the 16-pin DIP or SOIC to ground with a jumper gets you ±15 V out; connecting pin 11 to the +5-V input gets you ±12 V out.

The converters offer other interesting features. For example, there's undervoltage lock-out, a feature that takes over between 3.8 and 4.5 V. The chip also typically shuts down if its temperature exceeds 190°C. Its soft-start circuitry limits peak switch currents at power-up, and resets for all fault conditions—including a short between the reference pin and ground or the supply—or if the supply goes out of regulation. Soft-start action can be delayed by an external capacitor to further limit surge currents at start-up.

A 200-kHz oscillator is laser-trimmed to its frequency, on-chip, and requires no external timing components. It turns on both switches at the same time. But each switch is turned off when its current reaches a threshold set by the error signal—the difference between the output voltage and the reference voltage. The result is a duty-cycle modulated pulse train where the duty cycle is a function of the output-voltge error signal and the peak inductor current, resulting in cycle-by-cycle current limiting. Duty cycles can reach 90%—one of the reasons for high efficiency—along with a switch-resistance of just 3-ohm.

Other specifications include a maximum quiescent current from the 5-V input of 40 mA, and a maximum standby current during shutdown of 4 mA. Maximum line and load regulation are 0.05% and 1%, respectively, over the input and load currents called out earlier.

Each production kit contains one MAX743, two 100-µH inductors, 3 100-µF low-ESR capacitors, and 2 1N5817 Schottky rectifiers. In addition to these kits, Maxim also has evaluation kits containing a pc board ready for stuffing, as well as additional components including compensation capacitors, and optional pi-filter output inductors. (Without the inductors, 200-kHz output ripple typically runs 75 mV pk-pk at full load on the negative output, and 20 mV less on the plus output). The filters drop the noise about 30 dB. The evaluation kits (comercial-grade only) go for $20 each in small quantities. The production kits are also available in extended-temperature ranges.

Maxim Integrated Products Inc., 120 San Gabriel Dr., Sunnyvale, CA 94086; Douglas Vargha. (408) 737-7600. **CIRCLE 343**

P AND NDMOS H-BRIDGE HANDLES 10 A AT 60 V

Aimed at driving small dc, servo, voice-coil and stepping motors, as well as solenoids and other actuators, the Motorola MPM3004 contains a complementary power MOSFET H-Bridge rated at 60 V and 10 A (continuous for any two transistors). The four die are contained in Motorola's isolated, multi-chip power SIP (single inline package) called the ICePAK. Maximum permissible pulsed drain current runs 25 A. With 10 V of gate-to source voltage, and 5 A of drain current, static on resistance of the p-channel FETs in the upper legs of the bridge runs a maximum of 280 mΩ, while that of the n-channel FETs in the lower legs is about 150 mΩ. Since 2000 V rms of isolation is provided between any pin and the metal mounting tab, no insulating hardware is required for mounting. Operating temperature range is -40 to 125°C. In quantities of 1000, the MPM3004 go for $7.90 each.

Motorola Inc., msZ310, 5005 E. McDowell Rd., Phoenix, AZ 85008; Kirby Dorwachter. (602) 244-3370. **CIRCLE 344**

5-V LDO REGULATOR OFFERS ACTIVE RESET

Designed to post-regulate the output of a switching power supply, Cherry Semiconductor's CS-403 low-dropout (LDO) linear regulator controls up to 500 mA at 5 V. The typical voltage drop across it is 1 V while putting out 350 mA, and 1.1 V while putting out 500 mA. The regulator offers a unique feature called active-reset, useful if powering critical logic or a processor: when the output voltage drops below 4.75 V, an open-collector output goes low acting as a flag to digital circuits. As the voltage rises back to within regulation, internal circutitry creates a reset pulse at the open-collector output. Load regulation from 5 to 500 mA, with 8.5 V in, is a maximum of 50 mV. The CS-403 optimizes power-supply rejection by switching the internal reference from the regulator's input to its output, when the nominal output voltage is reached. The CS-403 comes in a 5-pin TO-220 package and goes for $.95 each in quantities of 10,000.

Cherry Semiconductor Corp. 2000 South County Trail, East Greenwich, RI 02818; Robert LeFort. (401) 823-3959 **CIRCLE 345**

FAST DUAL, MOSFET DRIVER OFFERS UVLO

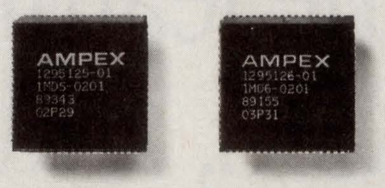
Designed to turn 5-V logic inputs into the 10-to-12-V pulses needed to turn a pair of medium to large-power MOSFETs on and off fast, Motorola's MC34151/33151 dual inverting-drivers offer guaranteed maximum rise and fall times of 30 ns. And that's while driving 1-nF loads (typically 60 ns for driving 10-nF loads). Operating from a 12-V rail, these bipolar ICs provide totem-pole outputs capable of sinking or sourcing up to 1.5 A. The output swings from 1.2 to 10.5 V, handling 10 mA. The input stage offers 170 mV of hysteresis—independent of the supply rail—insuring fast switching regardless of input-signal transition time. No oscillations occur as the input thresholds are crossed. The chip's undervoltage lockout (UVLO) circuit, operating with its on-chip reference, keeps the outputs low as the supply rail rises from 1.4 to 5.8 V. Once above 5.8 V, the outputs go low when the voltage drops to 5.3 V. The drivers come in 8-pin DIPs and SOICs—commercial (MC34151) and industrial versions (MC33151). Unit pricing in quantities of 10,000 runs from $0.65 to $0.87 each.

Bipolar Analog IC Div., Motorola Inc., EL-340, 2100 E. Eliot Rd., Tempe, AZ 85284; (602) 897-3615. **CIRCLE 346**

QUAD DMOSFET DRIVERS HANDLE OTHER JOBS

Four families of quad "Power Logic" drivers from Teledyne Semiconductors were designed to turn on and off four power MOSFETs fast. However they're just as much at home providing direct or PWM drive to motors, relays, small solenoids and LEDs, or hitting pulse transformers with fast pulses. Typical peak output is 1.2 A. The four families are designated by their output circuits: the TSC4435/6/7/8/9 has pull-up outputs; the TSC4455-59 has pull-down outputs and a clamp to the plus supply; the CMOS TSC4465 has pull-up/pull-down outputs; and the TSC4485-89 has pull-up outputs. Each driver is available with any of the following input logic: OR, NOR, NAND, AND, and AND with inverted output. Rise and fall times driving 470 pF run 25 ns maximum. Delay time is 75 ns. The chips take 4 mA from a 4.5-to-18-V supply.

Teledyne Components, 1300 Terra Bella Ave., P.O. Box 7267, Mountain View, CA 94039-7267; Rich Clarke. (415) 968-9241. **CIRCLE 347**



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CIRCLE 147

SEE HIGH-RES AND VGA GRAPHICS ON ONE MONITOR

Featuring digital VGA loop-through technology, two graphic-controller boards from Elsa America Inc. enable users to combine high speed and high resolution with DOS compatibility of existing VGA cards on a multisync monitor. Now, users can switch between VGA and high-resolution graphics on the same monitor without waiting for time-consuming redraws of text and graphics since both images are resident on separate frame buffers.

The digital VGA loop-through architecture of the XHR Alpha and XHR Spectra boards take the signal from the feature connector of the existing VGA card and run it through the ELSA controller where it automatically switches between VGA and high-resolution modes, depending on which software is updating the data on the screen. With the loop-through feature, any application can be operated that would normally run with a standard VGA video controller.

The Elsa graphics controller contains its own coprocessor. The drivers are designed to balance the workload between the system CPU and the graphics processor to achieve the fastest and most efficient computing speeds. The Alpha and Spectra, with resolutions of 1024 by 768 and 1280 by 1024, respectively, are available now for $1765 and $2450, respectively. All necessary cables and drivers are included.

Elsa America Inc., 400 Oyster Point Blvd., Suite 109, South San Francisco, CA 94080; (800) 272-ELSA or (415) 588-6285.
CIRCLE 348

■ *RICHARD NASS*

DEVELOP AND DEBUG APPLICATION CODE ON A

The CPU-186 CMOS single-board computer for industrial OEMs lets users develop their own application code directly on a PC under MS-DOS. It offers up to 16 MHz of true 16-bit processing, an increased instruction set, and twice the throughput of an 8086-based system.

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The board, with software, sells for $1395 in single quantities, with discounts for large quantities. Availability is stock to 30 days. A free demo disk is also available.

Computer Dynaimics Sales, 107 S. Main St., Greer, SC 29650, (803) 877-8700. CIRCLE 349

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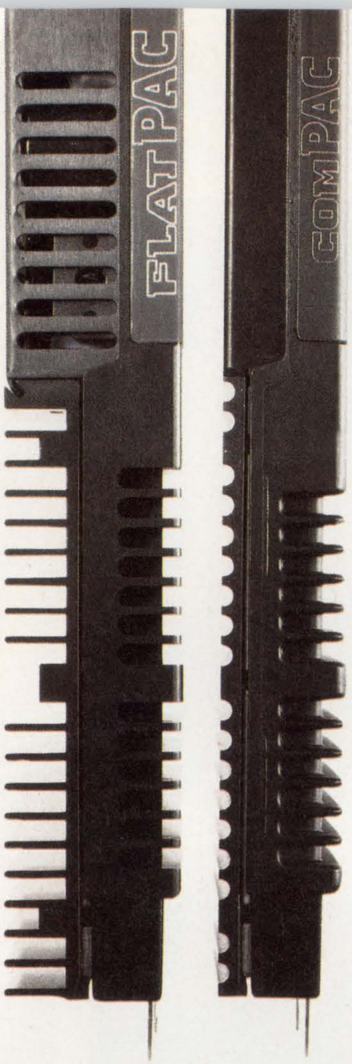
CIRCLE 138



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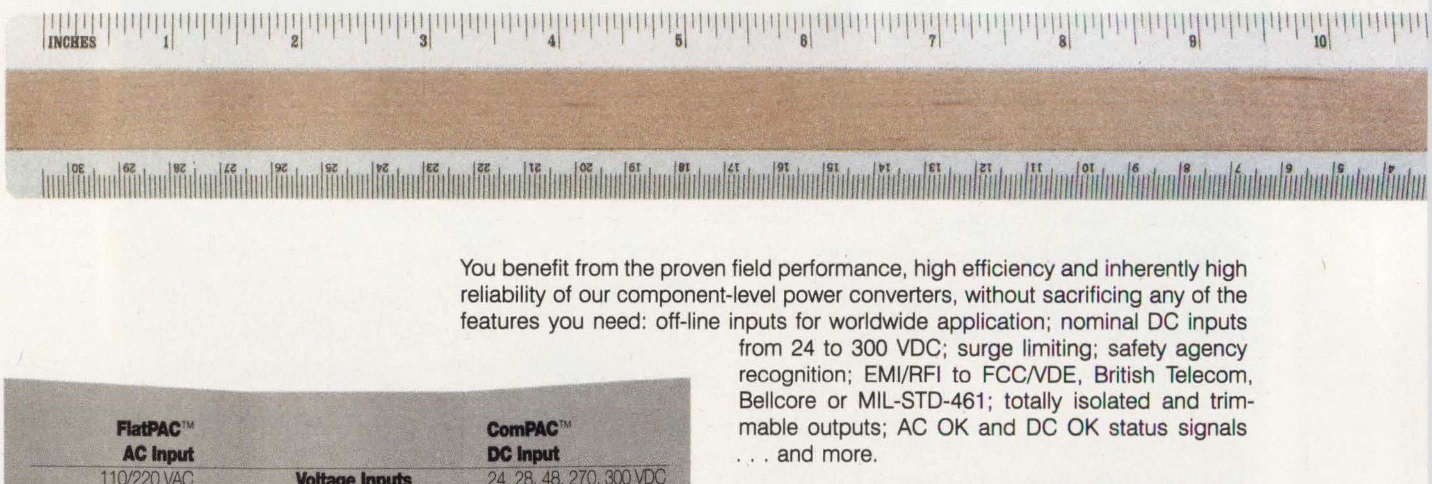

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FCC Part 15, Class A VDE 0871, Class A IEEE Std 587-1980	**Applicable Specifications**	Bellcore (24/48 V) British Telecom (24/48 V) FCC/VDE, Class A (300 V) MIL-STD-461 C (28/270 V) MIL-STD-704A

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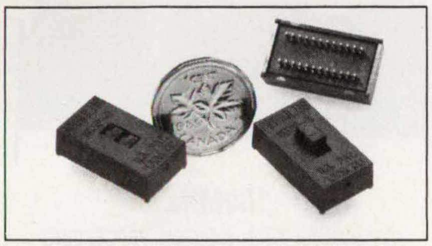

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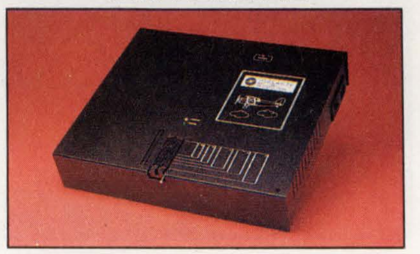

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Compilation time	17 sec	18	12
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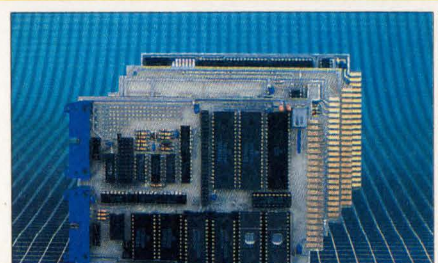

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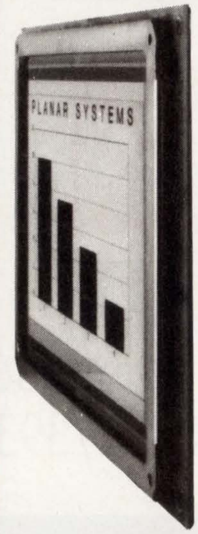

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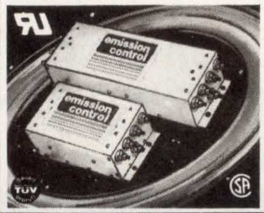

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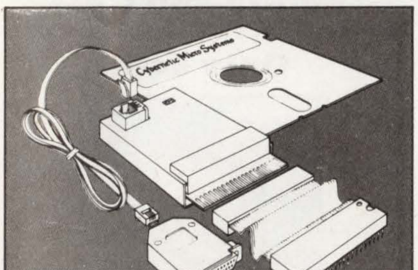

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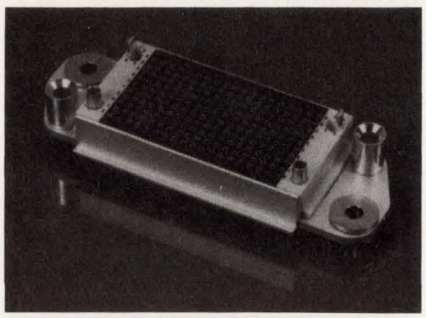

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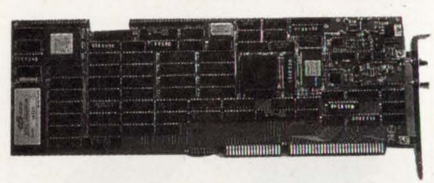

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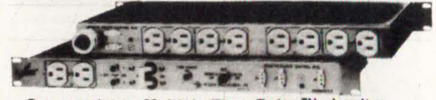

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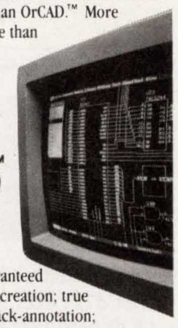

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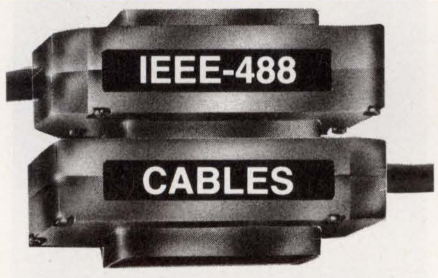

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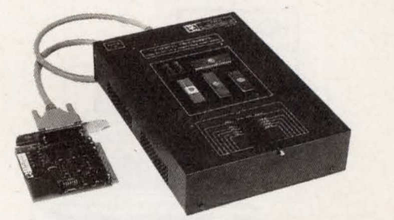

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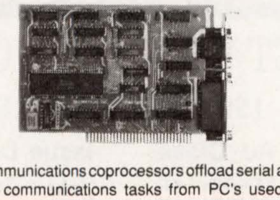

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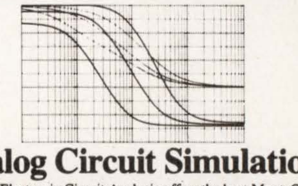

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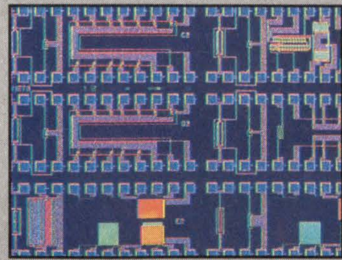

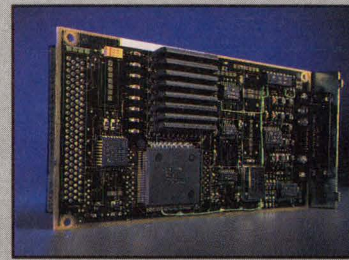

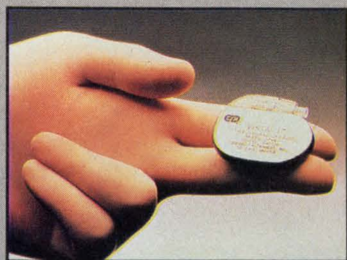

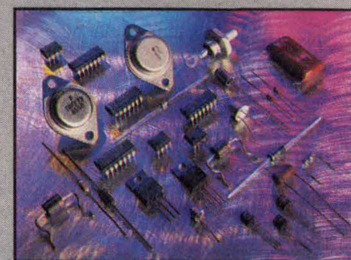

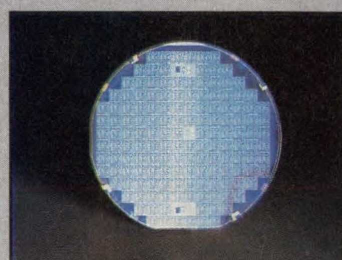

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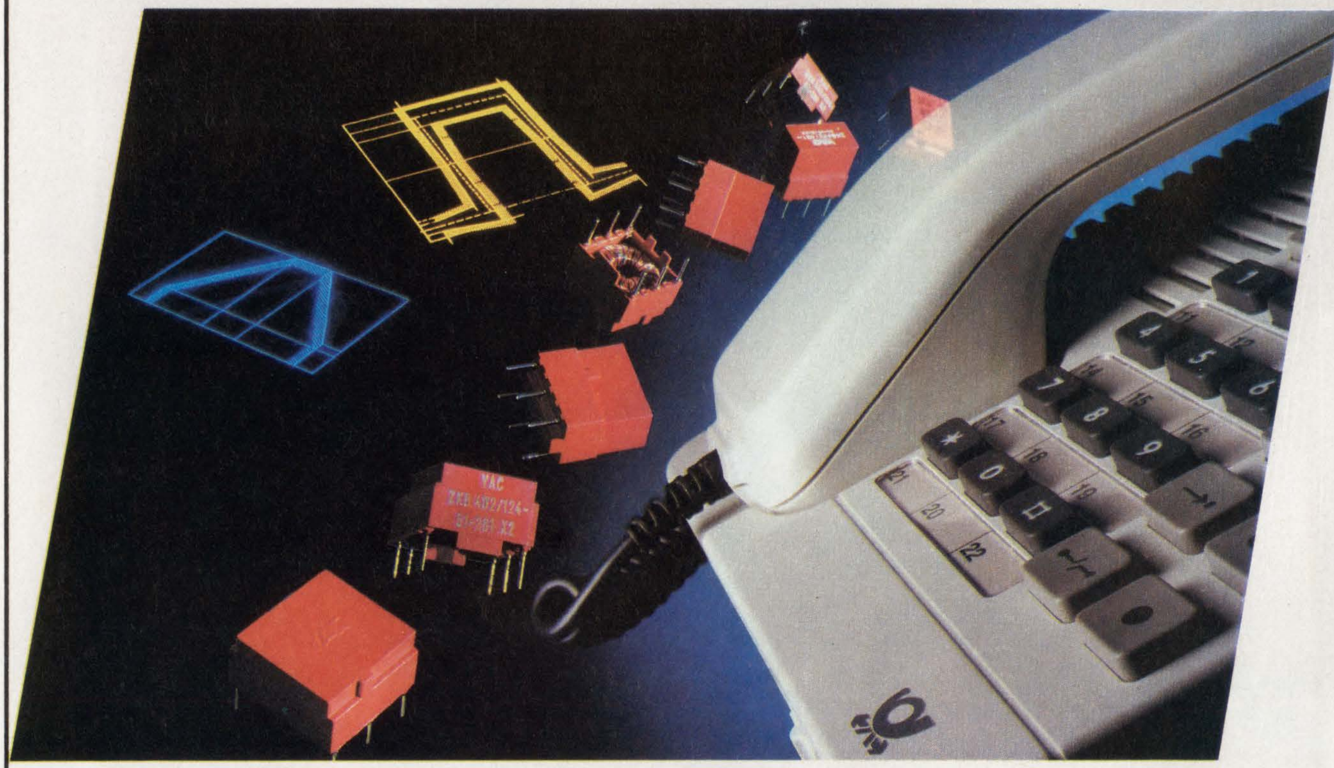

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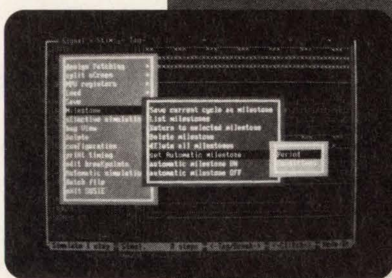

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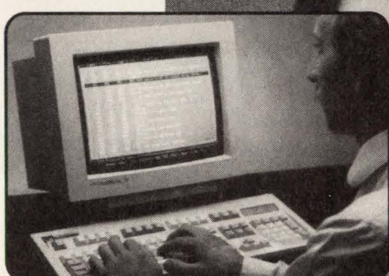

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Z-World Engineering 141

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1MEG SRAMS

25ns x1, x4, x8

AVAILABLE NOW!

Part #	Organization	Speed*	Packages	Availability
MT5C1001	1 MEG x 1	25ns	PDIP, CDIP, SOJ, LCC, Flatpack	NOW
MT5C1005	256K x 4	25ns	PDIP, CDIP, SOJ, LCC, Flatpack	NOW
MT5C1008	128K x 8	25ns	PDIP, CDIP, SOJ, LCC, Flatpack	NOW
MT5C2561	256K x 1	20ns	PDIP, CDIP, SOJ, LCC	NOW
MT5C2564	64K x 4	20ns	PDIP, CDIP, SOJ, LCC	NOW
MT5C2565	64K x 4 $\overline{OE}$	20ns	PDIP, CDIP, SOJ, LCC	NOW
MT5C2568	32K x 8	20ns	PDIP, CDIP, SOJ, LCC, ZIP, Flatpack	NOW

Part #	Organization	Speed*	Packages	Availability
MT5C6401	64K x 1	12ns	PDIP, CDIP, SOJ	NOW
MT5C6404	16K x 4	12ns	PDIP, CDIP, SOJ	NOW
MT5C6405	16K x 4 $\overline{OE}$	12ns	PDIP, CDIP, SOJ	NOW
MT5C6406/7	16K x 4 S. I/O	12ns	PDIP, CDIP, SOJ	NOW
MT5C6408	8K x 8	12ns	PDIP, CDIP, SOJ, LCC, Flatpack	NOW
MT5C1601	16K x 1	12ns	PDIP, CDIP, SOJ	NOW
MT5C1604	4K x 4	12ns	PDIP, CDIP, SOJ	NOW
MT5C1605	4K x 4 $\overline{OE}$	12ns	PDIP, CDIP, SOJ	NOW
MT5C1606/7	4K x 4 S. I/O	12ns	PDIP, CDIP, SOJ	NOW
MT5C1608	2K x 8	12ns	PDIP, CDIP, SOJ	NOW

* Slower speeds also available.

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CIRCLE 101

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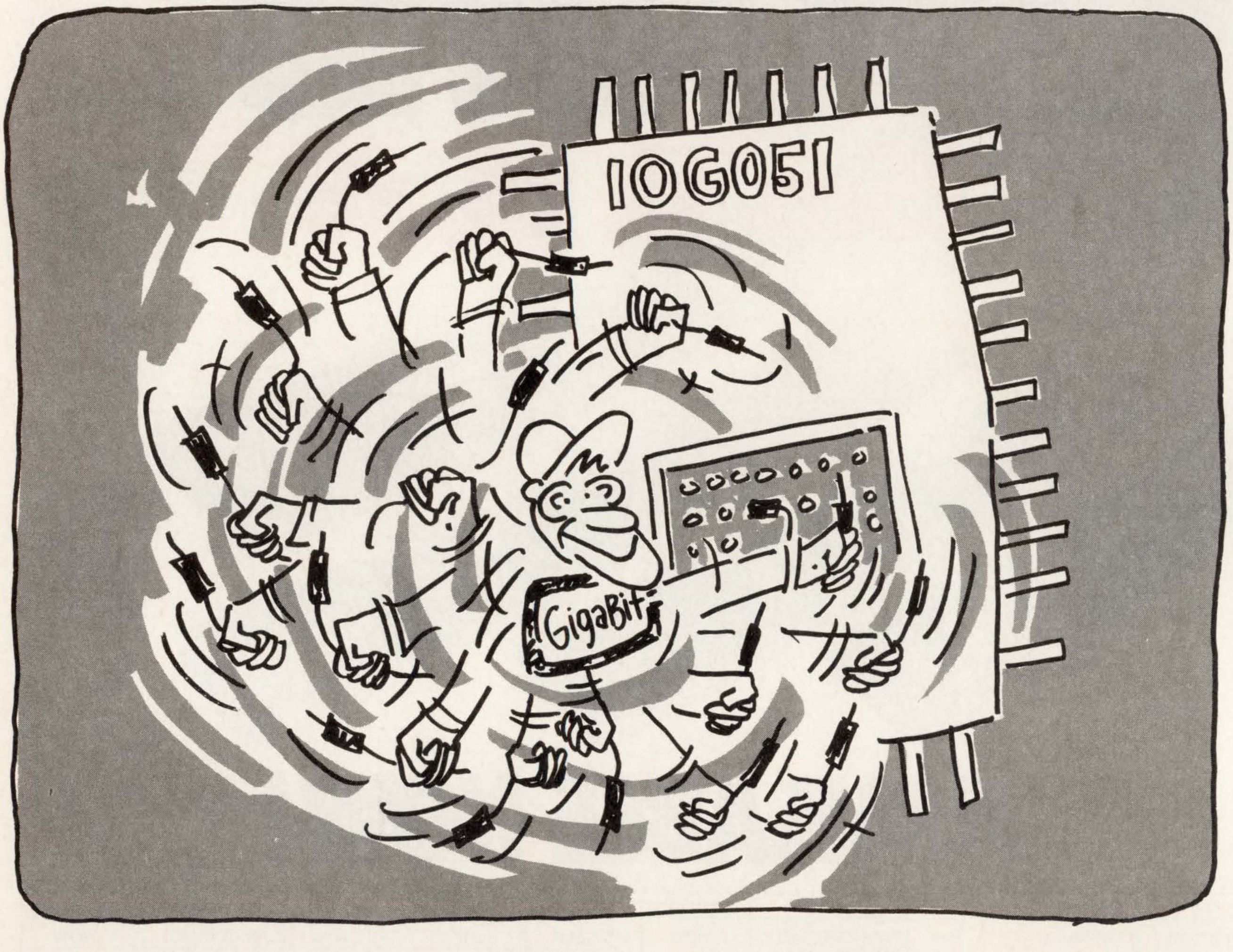

Not even a 16-hand operator can switch this fast! GigaBit's new 10G051 16x16 Crosspoint Switch IC can switch signals at 2.6 Gbit/s rate in less than 2 ns. With its wide bandwidth, the 10G051 handles SONET OC3 to OC48 as well as HIPPI/Fiber Channel signals at full speed.

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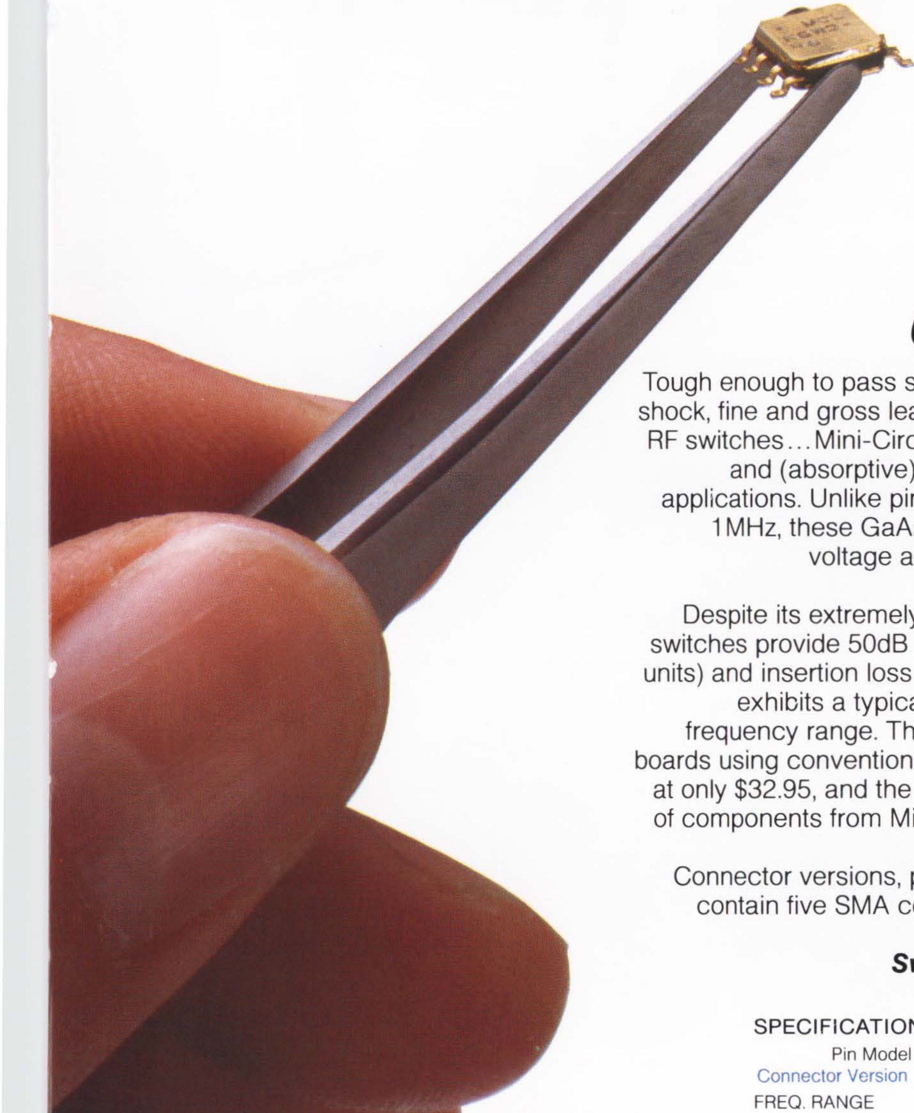
Switch to the fastest optical fiber communications IC family available. Contact us for more information on the 10G051 as well as our high-speed clock and data recovery circuits, transimpedance amplifiers, laser diode driver, LED driver, mux/demuxes, limiting amplifier, and the rest of the PicoLogic™ line of high-performance ICs. For more information, call:United States and Canada: (805) 499-0610; Europe: GIGA, +45 4343 1588; and Japan: Tokyo Electron Ltd., 423 33 8009.

GBL GigaBit Logic

CIRCLE 140 FOR MORE INFORMATION

CIRCLE 141 HAVE A REPRESENTATIVE CONTACT ME

TINY SPDT SWITCHES
ABSORPTIVE... REFLECTIVE



dc to 4.6 GHz from $32.95 (10-24)

Tough enough to pass stringent MIL-STD-883 vibration, shock, thermal shock, fine and gross leak tests... useable to 6GHz... smaller than most RF switches... Mini-Circuits' hermetically-sealed (reflective) KSW-2-46 and (absorptive) KSWA-2-46 offer a new, unexplored horizon of applications. Unlike pin diode switches that become ineffective below 1MHz, these GaAs switches can operate down to dc with control voltage as low as -5V, at a blinding 2ns switching speed.

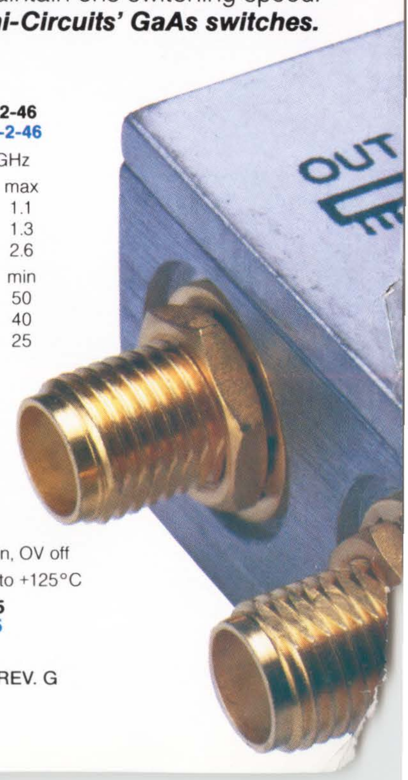
Despite its extremely tiny size, only 0.185 by 0.185 by 0.06 in., these switches provide 50dB isolation (considerably higher than many larger units) and insertion loss of only 1dB. The absorptive model KSWA-2-46 exhibits a typical VSWR of 1.5 in its "OFF" state over the entire frequency range. These surface-mount units can be soldered to pc boards using conventional assembly techniques. The KSW-2-46, priced at only $32.95, and the KSWA-2-46, at $48.95, are the latest examples of components from Mini-Circuits with unbeatable price/performance.

Connector versions, packaged in a 1.25 x 1.25 x 0.75 in. metal case, contain five SMA connectors, including one at each control port to maintain 3ns switching speed.

Switch fast... to Mini-Circuits' GaAs switches.

SPECIFICATIONS

Pin Model	KSW-2-46		KSWA-2-46	
Connector Version	ZFSW-2-46		ZFSWA-2-46	
FREQ. RANGE	dc-4.6 GHz		dc-4.6 GHz	
INSERT. LOSS (db)	typ	max	typ	max
dc-200MHz	0.9	1.1	0.8	1.1
200-1000MHz	1.0	1.3	0.9	1.3
1-4.6GHz	1.3	1.7	1.5	2.6
ISOLATION (dB)	typ	min	typ	min
dc-200MHz	60	50	60	50
200-1000MHz	45	40	50	40
1-4.6GHz	30	23	30	25
VSWR (typ) ON	1.3:1		1.3	
OFF	—		1.4	
SW. SPEED (nsec) rise or fall time	2(typ)		3(typ)	
MAX RF INPUT (bBm)				
up to 500MHz	+17		+17	
above 500MHz	+27		+27	
CONTROL VOLT.	-8V on, OV off		-8V on, OV off	
OPER/STOR TEMP.	-55° to +125°C		-55° to +125°C	
PRICE (10-24)	**$32.95**		**$48.95**	
	$69.95		**$79.95**	



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