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## COVER FEATURE

## 39 GaAs Clock Chips Remove Skew

Two clock-generation circuits simplify high-speed TTLcompatible system design by delivering clock signals with skews under 500 ps . The chips also offer programmable control of timing-signal edges.

## ELECTRONIC DESIGN REPORT

## 45 Microcontrollers: Features Galore

For embedded control, microcontroller ICs solve most application needs, particularly with recently added onchip support functions.

## AUTOMOTIVE ELECTRONICS

## 57 Engine Controulers Go Modular

Today's automotive systems need microcontrollers with modular architecture to handle changing engine requirements.

## 71 New ICs Drive Auto Electronics

Specially designed ICs are opening up a wide range of new automotive applications.

## DESIGN APPLICATIONS

## 89 How To Use Low-Skew Clock Drivers

Careful design is needed for stringent timing and clean clock signals in MPU systems.

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4}\begin{array}{lllllllllllllllll}{\mathbf{E}}&{\mathbf{L}}&{\mathbf{E}}&{\mathbf{C}}&{\mathbf{T}}&{\mathbf{R}}&{\mathbf{O}}&{\mathbf{N}}&{I}&{C}&{C}&{D}&{\mathbf{E}}&{\mathbf{S}}&{I}&{G}&{\mathbf{N}}
    AUGUST 9,1990
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## 14 EDITORIAL

## 16 TECHNOLOGY BRIEFING

Graphics mature, but at what price?

## 23 quick look

## 29 TECHNOLOGY NEWSLETTER

- Molding compounds hasten IC demise
- ASIC makers promote standard test port
- Server brings back mini memories
- SmartModels run simulations with

Max

- HDTV's first impact to hit computer industry
- Spice model creates better GaAs ICs
- Megabit flash EPROM performs sector erase
- Process merges tungsten deposition and etchback
- Submicron biCMOS packs 300 kgates/chip


## 35 TECHNOLOGY ADVANCES

- X-Windows gets true colors simultaneously
- Instant gate arrays have wiring configured by laser
- GaAs comes of age in low-cost satellite downconverter


## 105 IDEAS FOR DESIGN

- Test ganged pot tracking
- Build a precise, low-current source
- Find temp with RTD, varied current


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Jesse H. Neal Editorial
Achievement Awards

## NEW PRODUCTS

## 111 Analog

Workstations and HDTV get triple 10 -bit $80-\mathrm{MHz}$ DAC ICs

## 114 Instruments

115 Computer \& Peripherals
116 Computer Boards
118 Software
120 Digital ICs
123 Communications
126 Computer-Aided Engineering

## 128 Power

135 Components
136 Packaging \& Production

## 141 INDEX OF ADVERTISERS

## 143 READER SERVICE CARD

## WHET'S YOUR OPINIOL?

- How important are analog design skills for engineers in the future?
- How do the design skills of today's EE graduates stack up against those of young engineers of the past?

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- A preview of the International Test Conference-boundary-scan testing takes the spotlight
- The ins and outs of designing with DSP chips
- Using new delta-sigma d-a converters
- First details on new mixed-signal simulators
- Plus regular features:

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## Noyce On Education

It's already been a couple of months since Robert Noyce died in Austin, Texas, where he moved to direct operations at Sematech, the consortium for semiconductor manufacturing technology. Noyce's last interview may have been one of his most profound, published in the July/ August, 1990 issue of Intel Corp.'s house organ "Microcomputer Solutions." Here he noted, among other things, "We need to decide now whether we are going to make an investment in education. The outcome of that decision will be with us for the next 40 to 50 years."

Few will deny that Robert Noyce earned the right to predict for the next 40 to 50 years. His achievements-as the co-inventor with TI's Jack Kilby of the integrated circuit and as a co-founder of both Fairchild Semiconductor and Intel Corp.-will be with us for at least that long. And his comments on education, albeit posthumously recorded, are again right on target.

With all due respect to the leaders of the American education system, we believe that few experts exist in the process of education-at least not as expert in the same sense that Noyce was an expert in semiconductor technology. Education is not a rigorous science, as is physics-cause and effect in people are not as predictable as, say, the movement of electrons in a conductor or semiconductor. Just about the only common link between the two disciplines is that, in today's world, there won't be much progress without large upfront investments. But successful education programs involve more than money. The home and community environment must actively support the education process, and there must be a promise of employment opportunity when the education is completed.

The tributes to Noyce have been offered, the eulogies have been delivered. What could possibly remain to be said? Perhaps nothing need be said. Perhaps what's needed is action.


Stephen E. Scrupski Editor-in-Chief


## dc to 2000 MHz amplifier series

SPECIFICATIONS

| MODEL | FREQ. <br> MHz | GAIN, dB |  |  |  | - MAX PWR. dBm | $\begin{aligned} & \mathrm{NF} \\ & \mathrm{~dB} \end{aligned}$ | PRICE <br> Ea. | \$ ${ }^{\text {aty }}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | $\begin{aligned} & 100 \\ & \mathrm{MHz} \end{aligned}$ | $\begin{aligned} & 1000 \\ & \mathrm{MHz} \end{aligned}$ | $\begin{aligned} & 2000 \\ & \mathrm{MHz} \end{aligned}$ | Min. (note) |  |  |  |  |
| MAR-1 | DC-1000 | 18.5 | 15.5 | - | 13.0 | 0 | 5.0 | 0.99 | (100) |
| MAR-2 | DC-2000 | 13 | 12.5 | 11 | 8.5 | +3 | 6.5 | 1.50 | (25) |
| MAR-3 | DC-2000 | 13 | 12.5 | 10.5 | 8.0 | +80 | 6.0 | 1.70 | (25) |
| MAR-4 | DC-1000 | 8.2 | 8.0 | - | 7.0 | +11 | 7.0 | 1.90 | (25) |
| MAR-6 | DC-2000 | 20 | 16 | 11 | 9 | 0 | 2.8 | 1.29 | (25) |
| MAR-7 | DC-2000 | 13.5 | 12.5 | 10.5 | 8.5 | +3 | 5.0 | 1.90 | (25) |
| MAR-8 | DC-1000 | 33 | 23 | - | 19 | +10 | 3.5 | 2.20 | (25) |

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CIRCLE 91

Graphics Mature, But at What Price?

Displays on graphics workstations are nearing the point where the improvements in resolution are can't be seen by the human eye. On the other hand, monitor manufacturers are struggling to keep up with rapidly rising pixel refresh rates now possible with higher-speed ICs. However, such performance improvements-higher resolution and faster refresh rates-are expensive. The question is: How much will users pay for this high performance? Makers of high-end graphics systems will be looking for conclusive evidence, one way or the other, as they display their wares at the Siggraph '90 Computer Graphics Conference, August 6 th to the 10th, in Dallas, Texas.


RICHARD NASS COMPUTER SYSTEMS

In today's market, a 1280-by-1024 monitor's cost (about $\$ 3000$ ) is about the most users seem willing to spend on a display. Units with a resolution as high as 2048 -by-2048 pixels are available, but they still cost much more: up to $\$ 50,000$ with today's technology, primarily because of expensive CRT technology. As manufacturers begin to supply users with alternative, potentially lower-cost monitor technologies, such as color LCD, high-res display prices should start to drop. This may even put added pressure on CRT developers to innovate lower-cost CRT technology.

Consequently, the next few years will see only those users who need high resolution move to 2048 -by- 2048 displays. Rather than higher resolution, the most significant improvements probably will be refinements in CRT design to improve overall display quality and convenience (such as flatter screens, shorter depths, etc.), or in high-resolution flat-panel screens, making them larger (greater than 15-in.-diagonal) at an affordable price.

For example, Dolch Computer Systems, San Jose, Calif., developed a mere 10 -in. display with a resolution of 640 by 480 , which represents a solid starting point for the active-matrix LCD technology. Using a thin-film transistor (TFT) method, the Dolch VGA-compatible display is a step above standard electroluminescent or gas-plasma displays. It boasts a contrast ratio of 100 to 1, five times that of conventional LCDs and a typical response time of just 40 ms , compared with the LCD's usual spec of 300 ms .

One key issue facing graphic-workstation designers is integrating different data-handling functions, such as image processing, volume rendering, and interactive graphics. Users typically would prefer to perform all of their graphic analyses on one system, rather than jump from one specialized system to another to get the optimum data-displaying method. Because the need for visualization and the amount of data that requires the integrated technologies has grown so rapidly, workstation makers had to turn integration from wishful thinking into reality.

Another issue to be discussed at Siggraph involves tuning up the graphics processing system. Producing graphics involves more than just displaying an image. Many imaging requirements reside in a "graphics" environment in order to offload the CPU from graphic-specific tasks. As a result, it's free to handle memory and move data around quickly. The graphics processor then performs the graphics-oriented operations, such as zooming, panning, rotations, and clipping. Users are now finding that the bottleneck once located in the processor has shifted. Statistics indicate that up to $80 \%$ of computing time is spent processing I/O information to disks, peripherals, or to the graphics subsystem. The standard solution of increasing the processing power won't help ease the bottleneck. Therefore, it's likely that vendors will now focus their resources on increasing I/O performance. I/O specifications will be highlighted instead of the MIPS that are always tossed about. And because the high number of MIPS can't be utilized effectively, those numbers may be leveling off.

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|  |  |  | Max. | Max. | Min. | typ. | typ. |  |
| PLP-10.7 | DC-11 | 14 | 19 | 24 | 200 | 1.7 | 18 | 11.45 |
| PLP-21.4 | DC-22 | 24.5 | 32 | 41 | 200 | 1.7 | 18 | 11.45 |
| PLP-30 | DC-32 | 35 | 47 | 61 | 200 | 1.7 | 18 | 11.45 |
| PLP-50 | DC-48 | 55 | 70 | 90 | 200 | 1.7 | 18 | 11.45 |
| PLP-70 | DC-60 | 67 | 90 | 117 | 300 | 1.7 | 18 | 11.45 |
| PLP-100 | DC-98 | 108 | 146 | 189 | 400 | 1.7 | 18 | 11.45 |
| PLP-150 | DC-140 | 155 | 210 | 300 | 600 | 1.7 | 18 | 11.45 |
| PLP-200 | DC-190 | 210 | 290 | 390 | 800 | 1.7 | 18 | 11.45 |
| PLP-250 | DC-225 | 250 | 320 | 400 | 1200 | 1.7 | 18 | 11.45 |
| PLP-300 | DC-270 | 297 | 410 | 550 | 1200 | 1.7 | 18 | 11.45 |
| PLP-450 | DC-400 | 440 | 580 | 750 | 1800 | 1.7 | 18 | 11.45 |
| PLP-550 | DC-520 | 570 | 750 | 920 | 2000 | 1.7 | 18 | 11.45 |
| PLP-600 | DC-580 | 640 | 840 | 1120 | 2000 | 1.7 | 18 | 11.45 |
| PLP-750 | DC-700 | 770 | 1000 | 1300 | 2000 | 1.7 | 18 | 11.45 |
| PLP-800 | DC-720 | 800 | 1080 | 1400 | 2000 | 1.7 | 18 | 11.45 |
| PLP-850 | DC-780 | 850 | 1100 | 1400 | 2000 | 1.7 | 18 | 11.45 |
| PLP-1000 | DC-900 | 990 | 1340 | 1750 | 2000 | 1.7 | 18 | 11.45 |
| PLP-1200 | DC-1000 | 1200 | 1620 | 2100 | 2500 | 1.7 | 18 | 11.45 |

high pass dc to 2500 MHz

| $\begin{gathered} \text { MODEL } \\ \text { NO. } \end{gathered}$ | PASSBAND, MHz(loss <1dB) |  | fco, MHz (loss 3db) Nom. | STOP BAND, MHz (loss $>20 \mathrm{~dB}$ ) (loss $>40 \mathrm{~dB}$ ) |  | vSWR |  | $\begin{gathered} \text { PRICE } \\ \text { Qty. } \\ (1-9) \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | Min. | Min. |  | Min. | Min. | band | band typ. |  |
| PHP-50 | 41 | 200 | 37 | 26 | 20 | 1.5 | 17 | 14.95 |
| PHP-100 | 90 | 400 | 82 | 55 | 40 | 1.5 | 17 | 14.95 |
| PHP-150 | 133 | 600 | 120 | 95 | 70 | 1.8 | 17 | 14.95 |
| PHP-175 | 160 | 800 | 140 | 105 | 70 | 1.5 | 17 | 14.95 |
| PHP-200 | 185 | 800 | 164 | 116 | 90 | 1.6 | 17 | 14.95 |
| PHP-250 | 225 | 1200 | 205 | 150 | 100 | 1.3 | 17 | 14.95 |
| PHP-300 | 290 | 1200 | 245 | 190 | 145 | 1.7 | 17 | 14.95 |
| PHP-400 | 395 | 1600 | 360 | 290 | 210 | 1.7 | 17 | 14.95 |
| PHP-500 | 500 | 1600 | 454 | 365 | 280 | 1.9 | 17 | 14.95 |
| PHP-600 | 600 | 1600 | 545 | 440 | 350 | 2.0 | 17 | 14.95 |
| PHP-700 | 700 | 1800 | 640 | 520 | 400 | 1.6 | 17 | 14.95 |
| PHP-800 | 780 | 2000 | 710 | 570 | 445 | 2.1 | 17 | 14.95 |
| PHP-900 | 910 | 2100 | 820 | 660 | 520 | 1.8 | 17 | 14.95 |
| PHP-1000 | 1000 | 2200 | 900 | 720 | 550 | 1.9 | 17 | 14.95 |

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## 1-M I N U T E O P | N | 0 N S

## Is the IEEE truly serving its membership?

I've been an IEEE member for 12-plus years now, with no regrets at all. There is a lot of voluntary work involved, so you can't complain too much. Some of the publications are great; I have a large pile that I haven't read through. There are a lot of academic papers-I would like to see more practical examples that I can immediately come to grips with and apply in my work. James D. Traill, Tokyo, Japan

For a not-for-profit organization with so many volunteers in different societies, I believe IEEE is serving its membership. I do not mean that there is no room for improvement. However, in the local chapter that I belonged to, there are so many workshops and seminars-from how to grow in your own profession to how to start your own business. A lot of time and energy has been put in by those volunteer organizers. It is a self-service organization. I don't think it is fair to lay back and say that it didn't serve me well enough. Janpu Hou, Bridgewater, N. J.

What is the goal of the IEEE? Is it to help distribute information and push forward technology? I think that these are the goals of the IEEE and the IEEE is doing fine on these goals. I do not feel that the IEEE needs to be a union for engineers; nor should there be a union for engineers. Richard Lokken, Milwaukee, Wis.

Instead of surveys and public opinion polls, which seem to have the intent of IEEE bashing, you would serve your engineering readers better by sending your writers out to report the actions taken by IEEE PACE groups.

How can your readers know that despite any hearsay resulting from the previous reputation of the IEEE, that there are volunteers working within the IEEE structure to help the "working" engineers, including the unemployed? The tone set by your magazine in both " 1 -Minute Opinion?" and the career survey is such that it debases the efforts of the IEEE volunteers.

In addition to the EA, the IEEE has on-line services for jobs. It has a national network, plus local BBS services, which on Long Island include a message area: "jobs for LI. engineers." A number of IEEE volunteers have been fighting what they call ESP-engineering shortage propaganda. We have other groups-the Consultants Network, the Retired Engineers, and the group that I chair: the Small Business Development Group for engineering entrepreneurs and engineerowned businesses.

Remember, the IEEE is a volunteer organization. Anyone with a complaint about what the IEEE does (or does not do) needs only to become an active mem er to be able to participate with us in improving the member services. Marlene S. Farber, East Meadow, L. I.

What's your opinion on the IEEE? . . . or how about the importance of analog design skills . . . or the quality of today's EE graduates. See the table of contents ( $p$. 5) for a complete list of questions and fax your opinions to (201) 393-0637. Or mail your opinions to Quick Look, Electronic Design, 611 Route 46 W, Hasbrouck Heights, NJ07604.

## G A E S U R V E Y

Which systems do you use for automated design (including CAE or CAD), 1990 vs. 1989?


Source: Survey of Electronic Design readers conducted by the Adams Co., Palo Alto, Calif.

\section*{|  | H | 0 | T |  | P | O |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| P | R | 0 | D | У | C | T | $S$ |}

with line powering, a compact, 2400 baud modem works without an ac adapter or internal batteries. The Stowaway 2400 modem from Vocal Techologies Ltd. instead derives power from its serial port connection to a computer and from the phone line, which is how conventional telephones operate. Compatible with the AT command set, the modem, which has dimensions of 2.2 in . by 3 in , slides easily into a shirt pocket or the pouch for a laptop or notebook computer.

Because it can be tucked behind other equipment and doesn't need to be monitored, the modem also may find use in embedded applications. The Stowaway 2400 , which sells for $\$ 295$, is available from Vocal Technologies, 3032 Scott Blvd., Santa Clara, CA 95054 ; phone (408) $980-5181$; fax (408) 980-8709

## TRAVEL

- MAKE productive use of downtime in the airport or during in-room time at your hotel. More and more hotels, like the Radisson in Irvine, Calif, offer computers and peripheral equipment for rent; special phones in the rooms ease modem connection. When booking a room, check with the particular hotel about computer facili-ties-reservationists at toll-free numbers rarely
 have this information.
- LUGGING a portable computer through airports could well be a thing of the past. LapStop Corp. offers laptop computers from Apple and Zenith for rent at Avis car rental counters in Boston, Chicago, Newark, and Washington D.C. airports. Next on LapStop's list-airports in Atlanta, Dallas, Houston, Los Angeles, and San Francisco.


Analog Dialogue is a free quarterly technical journal that covers circuits, systems, and software for real-world signal processing. Journal No. 23-4 discusses highspeed pin electronics, the electrical interface between an ATE system and each pin of the device under test. The 24 -page issue describes two new high-speed pin driver chips (the AD1321 and AD1322) and a complete active load (the current-switching AD1315). $\mathrm{Re}^{-}$ quest a copy from Analog Devices Literature Center, Shawmut Rd., Canton, MA 02021.

Another free journal, for those interested in or working with OSI, is The SPAG Standard. The spring edition has articles on testing open systems and the role of the Standards Promotion \& Application Group in open systems. The 12-page issue also has a glossary, which spells out 27 of the myriad abbreviations in the world of standards and OSI. For a copy, contact Karen Garside, SPAG sa, Avenue Louise 149, Box 7, 1050 Brussels, Belgium; phone (32) 25350811 ; fax (32) 25372440.

A new version of Motorola Inc.'s Data Disk has information on more than 13,000 of the company's ICs and components. The database, contained on a floppy disk, also has crossreferences to 25,000 competitive devices. The free disk is available in IBM PC and Macintosh formats. Contact Motorola Data Disk Literature Distribution Center, P. O. Box 20924, Phoenix, AZ 85063; (800) 521-6274.

## Which technical books are the most popular in Silicon Valley?

## ELETRIDNICS:

1. SPICE: A Guide to Circuit Simulation and Analysis Using PSPICE. Paul Tuinenga. Prentice-Hall, 1988. \$21.

Noise Reduction Techniques in Electronic Systems, 2nd ed. Henry W. Oh. Wiley, 1988. \$42.95.
3. Microelectronics Packaging

Handbook. Rao R. Tummala, Eugene Rymaszewski. Van Nostrand-Reinhold. $\$ 94.95$
4. Logic Design Principles. Edward McClusky. Prentice-Hall, 1986. \$58.60. 5. Art of Electronics. Paul Horowitz, Winifred Hill. Cambridge University Press. $\$ 49.50$.
From Stacey's Bookstore, 219 University, Palo Alto, CA 94301; (415) 326-0681.

# ...Perspectives on Time-to-Market 

## BY RON KMETOVICZ

President, Time to Market Associates Inc. Cupertino, Calif:; (408) 446-4458

Iaving discussed first-of-a-kind, me-too-with-a-twist, and derivative classifications for new products, now I turn to
 next-generation products. These replace an aging product family that has little room left for market growth and that is being picked apart by the competition. For these products, time to market (TTM) is a prime concern. TTM shouldn't be so short that new products appear before they are needed, nor too long so that products reach the market too late.

Care must be taken to offer new capabilities, not just a smaller, faster, and less expensive version of the original. Next-generation products need to be in tune with the overall market, not merely redesigned versions of their predecessors! In all cases that I've studied, TTM was longer and engineering effort (number of person months) was higher on the nextgeneration product than on the first-of-a-kind effort. This suggests that a starting point for an estimate of TTM for a next-generation product is that it should least equal that of the TTM of the product about to be replaced.

Often, improved competitiveness results because next-generation efforts move the entire organization in a new direction. With a next-generation program, Xerox reduced its dependence on a large number of material suppliers and established new manufacturing capability. Hewlett-Packard draws on technology from all over the world to maximize its efforts in laser printers. Apple, IBM, NCR, and TI have used next-generation efforts to integrate, fuse, and develop design-for-manufacturing and computer-integrated-manufacturing processes and systems. Cooperative alliances and development of next- generation products seem to be this year's hot strategic business issue.

Describing next-generation products is relatively easy since prior product descriptions already exist and data has been collected from the marketplace over the years. Likewise, knowledge about customer desires and the competition is highest for this type of product, in fact, next-generation products are often pulled into the market. Information culled from the market feeds the product-development process, creating a product that meets requirements set by the market. It is usually very clear to the development team what has to be done, but usually not too clear how to achieve project objectives. For this reason, next-generation efforts tend to produce major gains in an organization's tactical and logistical performance.

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| PART | APPLICATIONS | $\begin{aligned} & \text { SWITCH } \\ & \text { CURRENT } \end{aligned}$ | PACKAGES |
| :---: | :---: | :---: | :---: |
| LM2575-5.0 | STEP-DOWN | 1A | K, T |
| LM2575-12 | STEP-DOWN | 1A | K, T |
| LM2575-15 | STEP-DOWN | 1 A | K, T |
| LM2575-ADJ | STEP-DOWN | 1A | K, T |
| LM2577-12 | STEP-UP. FLYBACK FORWARO CONVERTER | 3 A | K, T |
| LM2577-15 | STEP-UP. FLYBACK FORWARD CONVERTER | 3 A | K, T |
| LM2577-ADJ | STEP-UP FIYBACK FORWARD CONVERTER | 3A | K, T |

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CIRCLE 121

## OULOX

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## TECHNOLOGY NEWSLETTER

An important cause in the degradation of the intermetallic region of the gold-wire-to-aluminum-bonding-pad interface has been identified in several types of IC devices. In a paper presented at the International Reliability Physics Symposium in New Orleans in March, it was reported that antimony trioxide - a common component of semiconductor molding compounds-is the overriding factor in causing "ball lift," leading to a near-complete loss of bond strength. The test results, reported by scientists from Dexter Electronic Materials, Olean, N.Y., contrast sharply with earlier reports that antimony trioxide improves wire-bond reliability in dry environments. Dexter disclosed that the commonly used substance actually weakens many molding compounds. Using ion-scavenging additives with specific types of flame retardants solves the problem. Dexter's scientists believe that their test procedures will help screen molding compounds and benefit many applications. DM

Several leading ASIC suppliers have formed a specification group to enhance and promote a standard test-access port for on-chip test structures developed by CrossCheck Technology Inc., San Jose, Calif. The group's first meeting discussed how to improve and extend the test circuitry while ensuring compatibility with independently developed application software tools, such as fault-simulation and automatic-test-pattern-generation (ATPG) programs. With a standard port, ASIC designers could use the same application software to design ASICs with different suppliers. Members include Fujitsu Ltd., Harris Semiconductor Corp., LSI Logic Corp., and Raytheon Co. The group, all of which are licensees of CrossCheck technology, decided that the test port should be usable as a standalone port or with the IEEE-1149.1 test-access port for board testing. The patented test structure is a grid with many test points embedded in the ASIC's base array. Using the grid and specially developed ATPG software, designers can get faster high fault coverage than with conventional techniques. JN

The recently announced VAX 4000 model 300 "server" from Maynard, Mass.based Digital Equipment Corp., closely resembles the minicomputer of yesteryear. The VAX is the first that DEC designed and optimized specifically for client-server operation, coming on the heels of the company's proclamation that clientserver computing will rule in the 1990s. Fully compatible with other members of the VAX family, the server can utilize the extensive library of existing application software. The pedes-tal-enclosure machine occupies less than 20 ft . ${ }^{2}$ and doesn't require any special air conditioning or a separate computer room. Systems start at $\$ 127,000$. The server, as well other products, were announced at DECWorld ' 90 . RN chips from Altera Corp., San Jose, Calif., has just become possible thanks to called SmartModels, from Logic Automation Inc., Beaverton, Ore., enable designers to simulate the EPLDs as standalone devices and simulate the entire system, into which the EPLDs are inserted. One option available for the models is a "window" feature that allows designers to view some of the inner workings of the EPLDs. With the window viewports, designers can set breakpoints, single-step through instructions, change register values, and group various registers or bits together to form a cluster that can be observed as one entity. SmartModels will be available next quarter for the four current Max family members, and for two soon-to-be-released additions to the Max EPLD family. Contact Rick Denker at Logic Automation, (503) $690-6900$. DB fluence the evolution of desktop workstations significantly. According to the study, HDTV and workstation designers must replace bulky CRT screens with flat-panel displays, and adapt to higher-capacity communications channels. The study examines the current state of HDTV hardware and the probable future direction of the technology and its marketplace. The study, which was recorded on videotape, serves as a buying and planning guide for users with

## TECHNOLOGY NEWSLETTER

production and closed-circuit applications. It offers manufacturers, programmers, and educators a thought-provoking analysis and forecast of the HDTV movement. Also, the debate on standards, program delivery, and interactivity is addressed. The report was released at the Siggraph ' 90 conference. For information on obtaining the tape, call (800) $523-5503$. RN

Spice Model Creates Better gais ICs

By correcting several deficiencies in existing models, a new Spice model allows designers to more accurately represent GaAs metal-semiconductor field-effect transistors (MESFETs). For instance, in most existing Spice models (like Raytheon-Statz Spice models), the correct drain conductance can be predicted only for a small range of drain current values. The new model, developed by TriQuint Semiconductor Inc., Beaverton, Ore., rectifies this problem by making pinch-off voltage a function of drain voltage, and by correcting self-heating more efficiently. It also incorporates several features unique to GaAs technology, and more accurately predicts small-signal parameters over many bias conditions. As a result, the improved model delivers more realistic results for gain compression and other nonlinear parameters. The model is available now to TriQuint customers, and may soon be included with commercial Spice programs. For more information, call (503) 644-3535. LG

Megabit Flash EpROM
Performs Sector Erase
Unlike the simple flash memory chips that just erase the entire chip, a 1-Mbit flash memory's space divided into 128 sectors of 1 kbyte each. Each sector of the 128 -kword-by- 8 -bit memory from Philips Components-Signetics Corp., Sunnyvale, Calif., can be erased and rewritten independently. The entire chip can also be erased, as is the case with the simpler chips. The 48 F010 is the first flash memory chip from Philips-Signetics to come as a result of a technology-sharing agreement inked between Seeq Technology Inc., San Jose, Calif., and Philips in the fall of 1989. Philips is an alternate source for the previously released Seeq megabit flash memory. Data in the 48F010 can be read in 200, 250 , or 300 ns (depending on the speed grade), and can be stored in just $0.5 \mathrm{~ms} / \mathrm{byte}$. The 48 F 010 requires a 12 -V supply for the erase/program cycle and can endure 100 such cycles; screening can yield units with 1000 -cycle ratings. Future chip versions will be able to endure up to 10,000 erase-program cycles. DB tween metal layers in multimetal layer ICs has been developed to reduce wa-fer-processing cycle time and particle-induced defects. The system, developed by Applied Materials Inc., Santa Clara, Calif., combines chemical vapor deposition (CVD) of tungsten with tungsten etchback and maintains the wafer under vacuum throughout the processing sequence to avoid airborne contaminants. After receiving the CVD tungsten deposition, the wafer is then transferred to the etchback chamber where a magnetically enhanced reactive ion etching removes the tungsten blanket at a rate greater than $7000 \mathrm{~A} / \mathrm{min}$., but leaves tungsten in the contacts or via holes. At this point, the etch system removes any residual tungsten and the adhesion layer on the oxide surface using a highly selective overetch step. To prevent plug recess, the system-called the Precision 5000 WCVD-uses an end-point-detection scheme based on multiline optical emission. This detects the interface between the blanket tungsten film and the underlying adhesion layer. ML

Subuicron BiCMOS Packs 300 Kgates/Chip

A next-generation biCMOS process with drawn features as small as $0.8 \mu \mathrm{~m}$ makes it possible to pack 300,000 gates on a chip. Up to 120,000 ECL gates (including embedded RAMs), or 200,000 to 300,000 biCMOS gates, as well as mixed ECL, TTL, or CMOS I/Os can be integrated. Dubbed ABIC IV (advanced biCMOS IV) by its creator, National Semiconductor Corp., Santa Clara, Calif., the process can implement loaded ECL gates with delays as short as 50 ps, biCMOS gates with delays of less than 200 ps , and CMOS gates with loaded delays of about 400 ps . The process employs twin buried layers and double-diffused npn transistors to get $15-\mathrm{GHz}$ cutoff frequencies for the bipolar devices. In addition, contactless self-aligned structures with polysilicon sidewall silicidation are used. Silicide also coats the source, drain, gate, base, and emitter regions to reduce contact resistances. Short polysilicon local interconnections are also silicided. Tungsten plugs are used in the dielectric contact holes between metal layers so that subsequent metal layers are deposited on planar surfaces, thus eliminating step-coverage problems. With the planar layers, four levels of metal can be used for device interconnections, resulting in high wiring densities. DB

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- VMERAM: The VMERAM is the low-cost alternative for EDC memory, with pricing comparable to parity memory. The VMERAM is available in 2 to 16 MB densities.
- VSBRAM-EC1: Features include "extra-bit" EDC and dual 64-bit caches for simultaneous transfer capabilities. Dual-ported for the VMEbus and VSB subsystem bus, the VSBRAM-EC1 is available in 2 to 64 MB densities.


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CIRCLE 127

Thanks to a RAMDAC with a unique architecture and a virtualresource scheme, X-window terminals can now have true colors simultaneously for all windows. The RAMDAC, dubbed the Bt463, was developed jointly by Brooktree Corp., San Diego, Calif., and Digital Equipment Corp., Maynard, Mass. The chip's vir-tual-resource scheme enables each X-terminal window to have its own color map and the associated pixel data that's structured uniquely by the graphics chip without any color degradation.

The Bt463 operates at 110 to 170 MHz and is the first commercially available monolithic IC that offers a high-resolution truecolor palette (see the figure). According to Brooktree, the device's mapping functions are completely different from any other RAMDAC's, and is the key to its performance.

The chip's lookup tables have enough storage space to switch between a full eight-plane pseudo-color and a full 24 -plane true-color display. By adding the pixel-mapping function, called window-type tables, the lookup table can be subdivided into 16 smaller tables, depending on the window types being supported.The window-type tables offer the ability to switch on a pixel-by-pixel basis for different visual types (gray-scale, true-color, or pseudo-color). In addition, they make it possible for a window to be set at any depth. For example, one window can have a 24 plane true-color format, another a 12 -plane true-col-

## X-Windows Gets True Colors Simultaneously

or format, and still another an 8-plane pseudo-color or gray-scale format.

The Bt 463 is constructed so that each residing application can have control over its own lookup table.

that time.
At 170 MHz , the chip can achieve $1 / 2$-pixel resolu-tion-at 110 MHz , that equates to $1 / 4$-pixel resolution. The chip, which contains a standard microprocessor interface, isn't designed exclusively for DEC hardware. It isn't Xwindow specific either, just window specific.

The chip's pixel ports are reconfigurable on a pixel-by-pixel basis, offering the flexibility for multiple display modes. The reconfigurability feature also makes the frame buffer more efficient because the same buffer can be used for pseudo- and true color.

The RAMDAC lets DEC-one of the key instigators behind the X -windows software standardpromote the graphical user interface as a standard more easily.

RICHARD NASS

## Instant Gate arrays Have Wiring Configured By Laser

Aproprietary laserpatterning process has been developed that eliminates many drawbacks of other fastturnaround patterning schemes. It also lets premetallized gate arrays be configured in minutes. By predefining a two-levelmetal X-Y matrix of wiring above the gate array, Chip Express Corp., Santa Clara, Calif., can pattern both layers at the same time, thus eliminating processing steps of other fastturnaround gate arrays. That promises to reduce the turnaround time for gate arrays to 1 to 5 days.
Although the scheme can theoretically work with almost any gate ar-
ray, its key is the custom XY wiring grid for each array family. However, to ensure no hitches on the first product release, the company, along with International Microelectronic Products Inc., San Jose, Calif., developed its own family of gate arrays with predeposited metalization grids. The CMOS arrays have 3000,6000 , and 10,000 gates, and typical loaded gate delays of 500 ps .
Because the grid sits atop a standard chip, the company expects utilization to be near that of fully mask-configured arrays. To "instant" program a gate array, the base array is coated with metal. The metal is then patterned to
form the first-level grid, an oxide insulating layer is deposited, and the second metal level is deposited and patterned. Tiny window regions are next etched away in the oxide regions formed between the grid of sec-ond-layer metallines, to expose the programming points on the first metal layer (see the figure, $p .36$, left part).
For accurate laser positioning and minimal vaporized aluminum-wiring redepositing, a thin, proprietary antireflection material is deposited over the chip surface. Wafers can then be stockpiled for configuration at any time. An array is configured under the proprietary Quick la-ser-micromachining system. About an hour later (for up to 12,000 -gate arrays), a configured chip
emerges (see the figure, right part).

Post-processing removes the antireflection coating and any redeposited aluminum. A sealant cap layer is used to protect the chip. Chips can then be tested with customer test vectors and then delivered.

All of this works well for a few chip samples with a turnaround of 1 to 5 days. However, when a few dozen to a few hundred chips, there are two alternatives through IMP. The first is the OneMask production option, which allows all metal lines to be patterned in a single etch step.

Most double-level-metal arrays require four mask steps to custom-create the two wiring layers, result-

ing in a much longer processing cycle. For major production volumes, the second option lets IMP create custom metal masks for the Chip Express arrays to further optimize performance. For either option, customers can deal directly with IMP.

Chip Express doesn't plan to sell its laser system initially, but hopes to be-
come a "service house," making possible designs in either of two modes. Customers can provide a circuitnet list and testvectors created with the library of macrocells supplied by Chip Express and standard tools from popular workstation vendors. Chip Express will then do the layout (a fuse cut list) and supply post-layout parame-
ters for final simulation before signing off.

Alternatively, customers can purchase the layout software tools from the company and do all placement and routing. Then they just supply a final approved fuse pattern and test vectors.

Contact Adi Gamon, (408) 988-2445.

DAVE BURSKY

## GaAs Comes 0f Age <br> In Low-Cost Downconverter里 <br> tion run of any GaAs IC.

Gmay finally be over. For years, proponents of GaAs technology have predicted that the material's time was just around the corner. It took longer than originally thought to turn that corner, but Anadigics Inc., has done so. The Warren, N.J., company is producing more than 70,000 GaAs downconverter ICs a month to fulfill a 1-millionpiece order from British Satellite Broadcasting. This is the largest produc-

The Anadigics low-noise block downconverter is mounted in the Ku-band antenna's feedhorn. The circuit drops the incoming $11.7-$ to $-12.5-\mathrm{GHz}$ signal to 950 -to- 1750 MHz , a frequency range than can be sent through coaxial cable to the indoor direct-broadcast satellite (DBS) receiver. The downconverter and a preceding two-stage lownoise amplifier also boost the signal by 50 dB (see the figure). The Anadigics IC replaces more than 50 dis-
crete components used in older-generation downconverters.

To win the British Satellite order, Anadigics had to come up with a way to produce large numbers of GaAs ICs with a higher yield and lower price than is typical for the GaAs industry. To do that, the company bought moderately priced, commercially available equipment and modified it to fit the project's needs. Production technology was also improved to increase yields.

Furthermore, the company developed a quickturn design cycle that went from mask tape to device to

evaluation in just 2 weeks. The whole cycle requires only 4 weeks, compared with a typical 16 weeks.

The chip was packaged in a modified TO-5 can that costs less than $\$ 1$, rather than the $\$ 10$ or more for a specialized microwave package. In fact, the whole chip sells for under $\$ 8$. The discrete components being replaced cost from $\$ 5.50$ to $\$ 7$, depending on quantity. However, the IC also permits a smaller and simpler antenna, reduces manufacturing and test costs, and improves reliability and consistency.

The $12-\mathrm{GHz} \mathrm{Ku}$-band transponders, which have transmitters in the $100-\mathrm{W}$ range, make it possible for home receivers to use antennas of less than 1 m and costing about $\$ 500$. This compares with C-band systems in the U.S. with $3-\mathrm{m}$ antennas and price tags of $\$ 1500$ and up.

JOHN NOVELLINO

## Embedded RISC



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When evaluating RISC processors for embedded applications, you need real benchmark data from independent sources. The R3001 Performance Comparison Report is a collection of the original third-party data used in the graph below.

## Benchmark Your Code

Of course, we know that published data can't give you all the information. You'd prefer to perform benchmarks for your specific application, and our six technology centers are equipped to do just that bring us your code and we'll run your benchmarks!


Sources: Electronic Engineering Magazine, High-Performance Systems Magazine, Microprocessor Forum Conference Fall 1989, Independent Assessment Benchmark Report Atlantic Research Corporation
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[^0]If your product demands innovative power supplies, yet PKC. With a footprint smaller than a credit card, these sub-miniature converters offer the unique option of In-Card low profile mounting. The mechanical design allows the center of the module to rest in a slot in the $P C B$, giving a maximum height of just 8.5 mm .

The PKA and PKC can be easily paralleled for higher power applications and they make ideal components for $\mathrm{n}+1$ parallel redundancy applications.

# Two Clock-Generation Circuits Simplify High-Speed TTL System Design By Delivering Clock Signals With Skews Under 500 PS. Eliminate Signal Skews WIth Gais Clock Chips 

## Dave Bursky

0ne of the most difficult aspects of high-speed system design is distributing minimal-skew high-speed clock signals across one or several circuit boards. Often, board designs have to be "tuned" by adding inverter strings or delay lines to reduce clock skews. Such tuning lowers the maximum performance because the board must operate with worstcase trims. Yet another problem is distributing high-speed clock signals across multiple circuit boards so that the clocks can all be synchronized.

Although ECL systems have dealt with both issues for years, the latest crop of high-speed TTL-compatible systems now face this same problem as clock speeds go to 33 or 50 MHz and beyond. A 5-ns clock skew across a large board or system caused by improper buffering or system design could detract as much as $20 \%$ from the throughput in systems that run at 40 MHz .

By trimming the clock skew between clock output lines to less than 500 ps , most skew-related performance degradations can be eliminated. A pair of gal-lium-arsenide-based timing support chips, the GA1110 and 1210 from Gazelle Microcircuits, accomplish just that. They offer flexible and programmable control of timing-signal edges for systems with clock frequencies of $25,33,40$, or 50 MHz , or with doublefrequency clocks of up to 100 MHz .

The GA1110 can generate as many as five TTL clock signals that are phase-

and frequency-synchronized to a master clock, adjust the clock edges in 2 -ns steps, and buffer the clock signals for distribution. The GA1210 generates multiple output-clock signals at double the input frequency. Those clocks are also phase-aligned to the input clock.
In its basic configuration, the GA1110 serves as a multiple-output, zero-skew clock buffer. Inputs and outputs are all TTL compatible, with each

## CLOCK GENERATOR CIRCUITS



1. CONTAINING A $500-\mathrm{MHz}$ PHASE-LOCKED LOOP, the multioutput Gazelle GA1110 clock generator delivers five buffered outputs that are phase and frequency synchronized to the input clock. By using S1 and S0 control inputs and a feedback path, the clock output edges can be adjusted in 2-ns steps to provide early or late clocks, or an inverted clock.
output able to deliver symmetric waveforms with an output drive of $\pm 24 \mathrm{~mA}$. Output lines can be paralleled if higher drive currents are needed. The chip generates five identical phase-aligned output clock signals, as well as one $180^{\circ}$ phasealigned output clock, from a periodic reference clock (Fig. 1). Both the phase and frequency relationships of the output clocks to the input clock are controlled by the circuit through an on-chip phase-locked loop (PLL) that operates at about 500 MHz .

Proprietary PLL circuitry, similar to that employed in the company's previously released Hot Rod serial communication circuits, eliminates
the need for any external components to support internal phase locking at up to 500 MHz . That makes the GA1110 very simple to use. A sixth clock output serves as the feedback signal to the PLL and synchronizes the outputs to the input clock. Multichip clock chains and clock trees can now be easily configured thanks to the tight skew control.

There's no requirement, however, that the external feedback connection be directly hardwired from an output pin to the feedback input (FBIN) pin. Additional logic can be inserted in the feedback path as long as the signal arriving at the FBIN pin is derived directly from one of the

|  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Configuration number | Select pins |  | Outputs fed to feedback input pin | Output phase shift |  |  |  |  |  |
|  | S1 | S0 |  | Q0 | Q1 | Q2 | Q3 | Q4 | Q5 |
| 1 | 0 | 0 | Q0, Q1, Q2, Q3, or Q4 | 0 | 0 | 0 | 0 | 0 | 1 |
| 2 | 0 | 0 | Q5 | 1 | 1 | 1 | 1 | , | 0 |
| 3 | 0 | 1 | Q0, Q1, or Q4 | 0 | 0 | t | - 1 | 0 | 1 |
| 4 | 0 | 1 | Q2 | -t | -1 | 0 | -2t | -t | I-t |
| 5 | 0 | 1 | Q3 | $t$ | t | $2 t$ | 0 | t | I +t |
| 6 | 0 | 1 | Q5 | 1 | 1 | $1+t$ | H-t | 1 | 0 |
| 7 | 1 | 0 | Q0, Q2, or Q3 | 0 | $t$ | 0 | 0 | -t | -2t |
| 8 | 1 | 0 | Q1 | -t | 0 | - | -t | -2t | -3t |
| 9 | 1 | 0 | Q4 | t | 2 t | t | t | 0 | -t |
| 10 | 1 | 0 | Q5 | 2 t | 3 t | 2 t | 2 t | $t$ | 0 |
| 11 | 1 | 1 | Q0 | 0 | $t$ | t | -t | -t | -2t |
| 12 | 1 | 1 | Q1 or Q2 | -t | 0 | 0 | -2t | -2t | -3t |
| 13 | 1 | 1 | Q3 or Q4 | $t$ | 2 t | 2 t | 0 | 0 | -t |
| 14 | 1 | 1 | Q5 | 2 t | 3 t | 3 t | t | $t$ | 0 |
| Notes: 1. t represents the incremental phase-shift adjustment (2 ns ) <br> 2. A 0 phase shift indicates the output is aligned to the clock input <br> 3. A negative phase indicates the output precedes the input clock <br> 4. A positive phase indicates the output follows the input clock <br> 5. I indicates an inverted version of the input clock |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |

output pins, and it maintains the output pin's frequency. The internal PLL will adjust the output clocks to ensure zero phase delay between the FBIN and CLKIN signals. This feature is very handy when custom chips must be synchronized to the system clock. There's one caveat, though: The signal at the FBIN pin must stay continuous (it can't be a gated or conditional signal) to ensure synchronization.

A pair of active-high control signals, S1 and S0, combined with the feedback of an output clock signal to the FBIN, enables users to select any of 14 timing relationships between the five output clocks (Table 1). Consequently, the clock edges can be placed in precise, digitallycontrolled 2-ns increments ( + or - ) relative to the input and feedback clock phase. In systems where clocks must be sequential, or where wiringtrace and loading mismatches develop, the chip can supply the early or late clocks. When the chip is powered up, or the system clock is reset, the PLL requires a short time period ( $\mathrm{T}_{\text {sync }}$ ) to lock onto the signal.

In a typical system, designers may require several low-skew outputs, one early clock, one late clock, and one inverted clock. Such a system can be satisfied by setting S1 low, S0 high, and connecting Q0, Q1, or Q4 to the FBIN input (row 3 of table 1). The result is that Q0, Q1, and Q4 will be phase-aligned to the input clock, Q3 provides the early clock (by one 2-ns increment), Q2 delivers the late clock (also by one 2-ns step), and Q5 supplies the inverted clock.

Output clock signals are generated with $50 / 50$ duty cycles, even if the input clock isn't completely symmetrical. Ratios of up to $75 / 25$ for the input clock can be handled. Housed in a standard 16-pin DIP, the chip has three pins assigned for power and another three serve as ground lines. As a result, it permits more than adequate power-supply bypassing to eliminate noise. The chip operates from a $5-\mathrm{V}$ supply and typically draws about 120 mA .

Working either in conjunction with the GA1110 or as a standalone circuit, the GA1210 delivers multiple

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## CLOCK GENERATOR CIRCUITS

| TABE 2: OUPT GIOMESFOR TIE AH1210 |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Control pins |  | Clock output lines |  |  |  |  |  |
| Enable 2-phase clocking | Invert Q1 output | Q0 | Q1 | Q2 | Q3 | Q4 | Q5 |
| $\begin{aligned} & 0 \\ & 0 \\ & 1 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \\ & 0 \\ & 1 \end{aligned}$ | $1 X$ $1 X$ $1 X$ $1 X$ | $\begin{gathered} 1 \times(1) \\ 1 X \\ 1 \times(1) \\ 1 X \end{gathered}$ | $2 X$ $2 X$ $2 X$ $2 X$ | $2 X$ $2 X$ $2 X$ $2 X$ | 2 X 2 X PH1 PH1 | $\begin{aligned} & \hline 2 \mathrm{X} \\ & 2 \mathrm{X} \\ & \mathrm{PH} 2 \\ & \mathrm{PH} 2 \end{aligned}$ |
| Notes: 1. 1X is an output clock, a phase-aligned copy of the input clock signal. <br> 2. (I) indicates inverted version of 1 X clock ( $180^{\circ}$ out of phase) <br> 3. 2 X is an output clock, a phase-aligned double-frequency copy of the input clock signal. <br> 4. PH1 and PH2 are the first and second of two clock phases, synchronous to the input clock. |  |  |  |  |  |  |  |

low-skew clock signals that are twice the frequency of the input clock, which can be as high as 50 MHz (Fig. 2). The chip also generates several 1X clocks, one of which is fed back to the FBIN input so that the PLL can maintain synchronization.
All of the generated clocks (up to 100 MHz ) are phase-aligned to the periodic clock input. Such a circuit solves the problem of distributing high-frequency clock signals in large systems. A low-frequency clock of 50 MHz or less can be distributed to each board and then doubled on the board by a GA1210, so that 50 -to- 100 MHz clocks can time the logic on that particular card.
Several different configurations can be set up on the chip to accommodate various system requirements through the Enable 2-phase Clocking (EN2) and Invert Q1 (INV1) control pins (Table 2). In addition to supplying the 2 X clock, the chip can be configured to generate non-overlap-
ping two-phase clocks.
As with the GA1110, the clock multiplier accepts a master-clock input frequency from 25 to 50 MHz , has a maximum skew of 500 ps between outputs, recreates a $50 / 50$ duty cycle on each output, and can drive up to 24 mA on each output line. The GA1210 also comes in a 16 -pin DIP, and includes triple power and ground lines to minimize noise.

## Price And Availability

The GA1110 and 1210, which come in 16pin DIPs, are immediately available. The commercial-temperature-range versions of the 25- and 33-MHz speed grades sell for $\$ 28.50$ in 1000-unit quantities. The higherspeed grades will be sampled next quarter.

Gazelle Microcircuits Inc., 2300 Owen St., Santa Clara, CA 95054; Bob Gunn, (408) 982-0900. CIRCLE 511

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| SLIGHTLY | 549 |


2. GENERATING CLOCK INPUTS that are 2 X or 1 X multiples of the input clock, the GA1210 clock circuit can use its high-frequency PLL to synchronize the output clock signals to the input clock.


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 0n-Chip FeaturesSingle-chip microcontrollers are evolving with more features and higher throughputs, and are packed with CPU, RAM, and nonvolatile memory (ROM, EPROM, or EEPROM), and other system resources. The ubiquitous chips can be found embedded in multiple quantities in almost every product that has some electronic circuitry. From their beginnings as 4 -bit systems on a chip, they've progressed to 8 -, 16 -, and 32 -bit subsystems.
Although a few Japanese manufacturers are still creating new 4-bit microcontrollers, most low-end em-
bedded controllers are moving to the 8-bit plateau as the chips' tasks get more complex. A wider choice of third-party development tools is also available for 8 -bit and larger microcontrollers, and so are some alternate sources-features lacking in the 4-bit arena.
The latest crop of 8-bit controllers offer a kaleidoscope of features that tackle nearly every application niche. Aside from the expected RAM, ROM, and EPROM options, more controller manufacturers are adding electrically-erasable memories as an on-chip feature, with some makers now eying the use of flash memories. Commonly available

## Dave Bursky

## For Embedded CONTROL, MicroCONTROLLERS Solve Most NEEDS.

functions include timers, counters, serial ports, and parallel I/O ports.

Additional support functions becoming popular include interrupt controllers, large register files, and DMA controllers. Furthermore, manufacturers have created specialized I/O functions that include complex timer modules, pulse-width modulators, analog-to-digital and digital-to-analog converters (ADCs and DACs), and others for automotive system, telecommunication, con-sumer-equipment, and computer-peripheral applications.

On the whole, the older NMOS controllers have given way to CMOS. However, for applications that aren't power-critical, NMOS 8 -bit controllers are still viable and cost slightly less than the newer CMOS chips. NMOS-device choices are somewhat limited to older- or firstgeneration architectures-the MCS48 and 51 families originated by Intel Corp., Chandler, Ariz.; the 6805 series from Motorola Inc., Austin, Texas; and the Z8 from Zilog Inc., Campbell, Calif.; among others.

One way manufacturers can cut chip cost is to design a simple processor that performs its operations with minimum hardware by time-sharing the silicon resources. In previous designs, that approach worked because processor throughputs could handle the expected applications.

Today's demanding applications, however, require much higher performance. As a result, controller makers are taking two approaches to meet the customer's needs. The simplest approach is to up the clock fre-
quency that the controller runs at. Over the past few years, clock frequencies have crept from 8 MHz up to 16 MHz , and later this year some suppliers expect to ship controllers that run at 20 MHz and beyond. Unfortunately, elevated clock frequency creates several problems-testing the chips at the higher speeds, potentially reduced yields of higherspeed devices (and thus a higher device price), and more generated ra-dio-frequency interference caused by higher clock frequencies.

Alternatively, more silicon can be used to address the throughput issue. The processor's time-shared internal architecture can be restructured to a more parallel structure that enables multiple operations to be done in one clock cycle.

Many original low-cost 8-bit processors, such as the 80 C 51 family from Intel Corp.; the 68 HC 05 series from Motorola Inc.; the TMS7000 series from Texas Instruments Inc., Dallas; and the Z8 family from Zilog Inc.; require 8 to 12 clock cycles ( 1 to $2 \mu \mathrm{~s}$ ) for one instruction to execute. In contrast, some of the latest 8 -bit controllers-such as the H8 processors from Hitachi Semiconductor Inc., Brisbane, Calif.; the updated PIC family from Microchip Corp., Chandler, Ariz.; the K series chips from NEC Electronics Inc., Mountain View, Calif.; and the TMS370 family from TI-require just a few cycles (less than 500 ns ) to complete an instruction. Consequently, for a much lower clock rate, the processor can perform the same work. The drawback is that more silicon area is needed for the more efficient processor core, increasing chip cost.

Today's workhorse processors, the 8-bit microcontrollers, come in a dazzling array of configurations. A well-established family, such as Intel's 80 C 51 , which has several licensed alternate sources, contains more than two dozen commercial versions from Intel; Advanced Micro Devices Inc., Austin, Texas; Oki Semiconductor Inc., Sunnyvale, Calif.; Philips-Signetics Corp., Sunnyvale; Siemens Corp., Santa Clara, Calif.; and others.
The original CMOS versions in the

MCS-51 family include the 80C51 with 4 kbytes of ROM and 128 bytes of RAM, and the 80 C 52 , which includes 8 kbytes of ROM and 256 bytes of RAM. UV EPROM and ROM-less versions of both chips are also available. Other 80 C 51 resources include a pair of 16 -bit timercounters, a full-duplex serial port, 32 bidirectional I/O lines (four 8-bit ports), and a five-source interrupt structure with two priority levels. The C52 adds one more timercounter and its interrupt source.

Intel's latest offering is the 87 C 51 FC , which offers the largest on-chip program storage in the MCS51 family: 32 kbytes of EPROM, doubling the memory of the company's previous version-the 87 C 51 FB . Along with the expanded program memory, the chip packs an array of programmable counters with five I/ O channels to handle complex timing applications with minimum CPU overhead. Either a windowed ceramic package or a one-time-programmable (OTP) plastic package can house the chip.

Additional 87C51FC resources include 256 bytes of RAM, a serial I/ 0 port, three 16 -bit timer-counters, and a two-level program lock to guard against software piracy. A simpler version of the chip, the 87C54, eliminates the complex counter array to trim the price. The chips are designed to handle some of the complex operations in automotive control systems, and can operate over a -40 to $+125^{\circ} \mathrm{C}$ temperature range at either 12 or 16 MHz .

The 80C515, packing 48 I/O lines, a 16 -bit watchdog timer, three additional 16 -bit counter-timers, a fullduplex serial port, an 8-bit ADC, as well as 8 kbytes of ROM and 256 bytes of RAM, is an extended-I/O version of the 80 C 51 offered by AMD and Siemens. Housed in a 68 -lead PLCC, the controller's ADC has eight multiplexed inputs and performs a conversion in $13 \mu \mathrm{~s}$. When operating at 12 MHz , the controller executes most commands in about 1 $\mu \mathrm{s}$. Higher-speed $16-\mathrm{MHz}$ units are also available.

AMD and Siemens went in different directions for additional control-
lers based on the C51 CPU core. AMD created the 80C541,521, and 321, as well as a forthcoming chip, the 80 C 324 . The first three share a common architecture that includes 16 kbytes, 8 kbytes, or no ROM, respectively, and 256 bytes of RAM. The controllers have a dedicated watchdog timer and dual data pointers to reduce the CPU's access time to external memory. The C324 has all of the ROM-less 321 's features plus a port-expansion mode that enables the chip to control up to fifteen 8-bit ports by multiplexing signals over its 8-bit Port 1.
Pushing towards the high-end of the 8 -bit range, the SAB80C517 and 537 (ROM-less) from Siemens start with the 80 C 51 core, 8 kbytes of ROM, and 256 bytes of RAM. To that base the company added a complex compare-capture unit (CCU), a watchdog timer, a priority interrupt subsystem with four levels, a multi-plication-division block, a second serial port, an 8 -bit 12 -channel ADC, eight data pointers for indirect addressing, and nine parallel I/O ports.
The CCU block includes one 16 -bit

timer-counter, one 16 -bit compare timer, one 16-bit reload-capture-compare register, four 16 -bit capturecompare registers, eight 16 -bit compare registers, the ability to perform concurrent compare operations, and up to 21 channels of compare outputs. The multiplication-division block tackles the math-intensive applications and delivers results on 32 bit numbers in just 4 to $6 \mu \mathrm{~s}$.

In addition to the MCS-51-compatible chips, Siemens just signed a deal with SGS-Thomson Inc., Phoenix, Ariz., to alternate source and jointly develop future versions of SGS's Sseries microcontrollers. The ST8 series from SGS is based on a core CPU that can address up to 32 kbytes of program memory and a 6 -bit stack pointer (future versions will increase the pointer to 8 bits to address up to 256 bytes). The first two processors in the family, the ST8108 and 81E08, pack 8 kbytes of ROM and EPROM, respectively, 176 bytes of RAM, timers and serial I/O ports, as well as bidirectional I/O ports. Future members will include EEPROMS, ADCs, DACs, and other functions. SGS also
has two other families, the ST6 to tackle the low-end applications, and the ST9 to handle the most complex 8-bit applications.
Tackling I/O-intensive applications, Philips-Signetics created an extended I/O processor-the 83C451-which offers seven 8 -bit I/ 0 ports in a 68 -lead PLCC version. One unique port includes a "mailbox" feature that makes it possible for the port to serve as an I/O port or as a control and status register. The chip packs the same amount of RAM and ROM as the original 80 C 51 .

A more complex version of the same chip-the 83C552-starts with the 80 C52 memory and adds six bytewide parallel ports, a 10 -bit 8-channel ADC, two pulse-width-modulated (PWM) outputs, and an inter-IC bus serial port for chip-to-chip communications (see the figure). Also available are an EPROM version, and a version without the ADC and PWM outputs and with only four ports.
Very large memories on a version similar to what Intel included on the 877 C 51 FC are also on the horizon. Philips-Signetics plans to offer the

83C528 with 32 kbytes of EPROM and 512 bytes of RAM. In addition, the company will have two ver-sions-the 83 C 053 and 054 -both of which pack 192 bytes of RAM, and 8 or 16 kbytes of EPROM, respectively. These two chips are aimed at TV remote-control subsystems and pack a separate 128 -byte display RAM and three digital video outputs.

Going in the low-cost and minimalI/O direction, Philips-Signetics slimmed down the 80C51, creating the 83C751. It comes in a 24 -pin skinny DIP (300-mils wide) and packs 19 I/O lines, one counter-timer, a sin-gle-level interrupt structure, 2 kbytes of ROM, and 64 bytes of RAM. A slightly larger version-the 83C752-comes in a 28 -lead DIP or PLCC, and packs the same memory and counter-timer, but has three parallel ports (two 8-bit and one 5-bit parallel ports), an inter-IC serial interface, one PWM output with timer, and a five-channel 8-bit ADC. Both chips can't use off-chip memory.

Philips-Signetics is also upgrading its 80 C 51 direct-equivalent controllers so that they can operate at 20


ONE OF the most complex microcontrollers based on the 80 C51 processor core is the PCB83C552 from Philips-Signetics. It packs an eightchannel ADC, a pair of PWM outputs, a pair of serial ports, multiple timer-counters, and a large number of $I / 0$ lines.
and 24 MHz . The $24-\mathrm{MHz}$ unit becomes the fastest C51 controller available from any source and can execute typical commands in just 500 ns . The company hopes to be the first supplier to include EEPROM on an 80C51-based controller. Plans are underway to create the 83 C 851 , an 80 C 51 with 256 bytes of EEPROM. One alternative to EEPROM for the 80 C 51 is a battery-backed version offered by Dallas Semiconductor Corp., Dallas, Texas. By embedding a long-lifetime battery-backed RAM in the same package as an 80C51equivalent controller, Dallas devised a controller that can retain data for about 10 years, if used in accordance with its data sheet.

Although many C51-based CMOS controllers can operate at voltages down to about 2.5 V , even lower oper-ating-voltage requirements led designers at Philips-Signetics to create another version of the C51-the 83CL410. The CL410 was designed with static CMOS logic and can operate with supply levels of just 1.5 V , or draw less than 1 mA when operated at 3 V and 3 MHz .
As prolific as the MCS-51 family is thanks to its multiple suppliers, Motorola has limited alternate sources to its low-to-mid-range 68 HC 05 architecture microcontrollers, establishing itself as a sole-source for its mid-to-high-end 8 -bit family-the 68 HC 11 series. However, that hasn't limited the proliferation of the 68 HC 05 controllers. Nearly two dozen versions of the 68 HC 05 already exist, with a few of these alternatesourced by Harris Semiconductor Corp., Melbourne, Fla. (an outgrowth of Harris's acquisition of RCA Corp., the original licensee of the Motorola processors). The chips' typical instruction execution time is about $1 \mu$ s and contain a similar software structure to the original 6800 microprocessor.
Needless to say, a wide variety of memory, I/O, and control functions are available in the processor family, and more "standard" versions are planned by both Harris and Motorola. To create so many versions, Motorola implemented a customer-specific adaption program that tries to
match similar customer requests with similar features and then to turn all of the requests into a common piece of silicon that can be offered commercially. The company also expects to add such capabilities as handling high voltages for display driving or high-current outputs to directly drive small motors.
For more demanding applications, Motorola offers the $68 \mathrm{HC11}$ family, the first microcontrollers to offer RAM, ROM, and EEPROM on one chip. The original HC11 processor packed 256 bytes of RAM, 512 bytes of EEPROM, and 8 kbytes of ROM, as well as a timer, both simple and complex serial ports, multiple parallel I/O ports, an 8-channel ADC, and a watchdog timer. One forthcoming HC11 processor will include no ROM, but will offer demultiplexed address and data lines, 1 kbyte of RAM, and 512 bytes of EEPROMthe 68 HC 11 F 1 . Additional processors with larger on-chip memories are also in development.
The HC11 processors execute a superset of the original 6800 and 6801 instruction sets and include the ability to tie the dual 8 -bit accumulators together and perform 16-bit arithmetic operations without looping. The simplest version in the family is the 68 HC 11 D 3 , which contains just a 4 kbyte ROM, 192 bytes of RAM, and comes in a 40 -pin DIP. Memory capacities for large programs are also available-the HC11E9 packs 12 kbytes of ROM, 512 bytes of EEPROM, and 512 bytes of RAM.
Also offering two families of 8-bit microcontrollers, TI developed the TMS7000 series to tackle what it considers low- to mid-range applications, and the TMS370 series to handle the mid-range to high-end applications. About a dozen versions of the TMS7000 processor exist, all offering performance levels competitive with the MCS-51 and 68 HC 05 families. The TMS7000 chips pack up to 4 kbytes of ROM or EPROM, 128 or 256 bytes of RAM, timers, serial ports, and up to 32 I/O lines. One CMOS processor, the 70 C 42 , operates from as low as 2.5 V and as high as 6 V . At the low value, the chip must run at a much-reduced clock
frequency- 800 kHz , maximumrather than the 5 to 6 MHz when powered by a 5 - or $6-\mathrm{V}$ supply.

Employing a more complex CPU core, the TMS370 series chips compete more with the $68 \mathrm{HC11}$ and the K-series from NEC Electronics. TI actually divided its 370 family into several sub-families, which total close to two dozen choices. The subfamilies consist of the 370 Cx 10 , Cx3x, and Cx5x series. The Cx10 aims at the lower end of the higherperformance range, the Cx3x for slightly more complex applications, and the Cx5x solves the high-I/O and large memory needs of the most challenging applications.

Various members of the Cx10 series offer up to 4 kbytes of program ROM or EEPROM, 128 bytes of RAM, another 256 bytes of data EEPROM, a counter-timer and a watchdog timer, a serial port, and up to 22 I/O lines. More formidable applications might use the Cx5x processors, which pack up to 16 kbytes of ROM or EPROM, or 4 kbytes of EEPROM, as well as 256 or 512 bytes of RAM, 256 or 512 bytes of data EEPROM, an 8 -channel ADC, two counter-timers plus a watchdog timer, two serial ports, and up to 55 I/ 0 lines.

Some of the most recent family members include versions that operate at clock frequencies as high as 20 MHz . They add on-chip functions such as a multichannel ADC, or a multi-output complex timer array that can offload the Cx32 core processor, much like the timing array Intel and Siemens included in their 80C51-based controllers. The programmable acquisition and control timer module provides six capture inputs, eight timer-controlled outputs with PWM capability, up to 20 configurable comparison lines, a watchdog timer, and a full serial port.

With ROM capacities of 2 or 4 kbytes, Zilog's NMOS Z8 family gives customers about a dozen variations with pin counts ranging from 28 to 64 leads. All of the chips in the Z8600 family pack 124 bytes of RAM, either 1 or 4 external interrupt inputs, two timers, and in most versions, both an asynchronous serial port and another simpler, synchro-

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## EMBEDDED CONTROLLERS

nous serial port. The CMOS Z8 family includes over 15 processors that have as few as 18 and as many as 40 pins. On-chip memory ranges from 2 to 8 kbytes of ROM or EPROM, while RAM is either 124 or 236 bytes.

Several Z8 versions are designed to retain data when the power supply dips as low as 2 V , and they can operate from 3 to 5.5 V with clock speeds of 2,8 , or 12 MHz . When running at 12 MHz , the average instruction executes in about $1 \mu \mathrm{~s}$. Some also include analog comparators to perform level-sensing operations and programmable timers with programmable prescalers (the Z86C08, 09, 30, 40 and the ROM-less C90).

The company's older NMOS Super 8 processor will soon be converted to CMOS, thus reducing power, possibly increasing the on-chip ROM to 16 kbytes, the RAM to 512 bytes, and improving performance. The NMOS version packs many resources-a DMA controller, high-performance math instructions and commands to support threaded-code languages such as Forth, a large 128 -kbyte address space, a complex interrupt-service unit that responds to an interrupt in just 600 ns , a pair of countertimers, a full-duplex serial port, and 40 parallel I/O lines.

One version of the Z8, the Z86C27, is optimized for television control, and contains an 8 -kbyte ROM, 256 bytes of RAM, a separate 180-byte character RAM, 4-kbyte character ROM, and 13 PWM outputs with 6 or 8-bit resolution (except for one that offers 14 -bit resolution). The chip also includes some analog comparators, a pair of counter-timers, 36 parallel I/O lines, and fast-responding interrupt control logic.

Future members of the Z8 family will tackle such applications as hard-disk control, thanks to a separate ALU that accelerates multiplication and division operations, thus improving response times in servo control loops.

In addition to offering an alternate source to the old Intel MSC-48 family, Mitsubishi America Inc., Sunnyvale, has a family of over thirty 8-bit controllers in its proprietary M50xxx and M37xxx families that are soft-
ware-compatible with the 6500 family instruction-set processors. Onchip ROM ranges from 3 to 16 kbytes on the smallest to largest units, with RAM growing from a minimum of 96 bytes to 512 bytes at its maximum.

Minimum instruction execution times range from about $2.5 \mu$ s when a 3.2 MHz clock is employed, to just 670 ns when the chips run from a 12MHz clock. The 6502 processor core is also used by NCR Corp., Colorado Springs, Colo., to create custom custom microcontrollers, while Rockwell International, Newport Beach, Calif. has developed a single-chip controller with 2 kbytes of RAM and 64 bytes of RAM.

Depending on the chip in Mitsubishi's family, there can be from 14 to 48 I/O lines, asynchronous or synchronous serial ports, ADCs, DACs, PWM outputs, counter-timers, and special features including vacuumfluorescent or liquid-crystal display drivers, telephone-tone generators, or variable-threshold comparators. A complex chip, the M37409M2, combines the controller, 192 bytes of dual-ported RAM, 320 bytes of normal RAM, 4 kbytes of ROM, three full-duplex serial ports, an 8-bit timer, and two byte-wide I/O ports.

Targeting the high-throughput applications, the K-series processors from NEC offer designers highly efficient CPUs. The company currently has close to 20 devices defined and in production, with more to be released before year's end. In the K2 family, versions are available with RAMs as large as 1 kbyte and ROMs or EPROMs of up to 32 kbytes. As with the Motorola $68 \mathrm{HC11}, \mathrm{NEC}$ offers one type that packs 16 kbytes of ROM, 512 bytes of RAM and 512 bytes of EEPROM-the uPD78244.

The K-series is crafted for speedat 12 MHz the K 2 chips execute instructions in 333 ns -about half the time required by the 68 HC 11 or TMS370 controllers. Due later this year are $16-\mathrm{MHz}$ versions that cut the instruction cycle time to 250 ns . Serial I/O ports, counter timers, and multichannel ADCs and DACs are common on most devices in the K series. One carryover from the previous uPD7800 family of 8-bit control-
lers is an improved on-chip peripheral management unit that offloads the CPU core from handling interrupts and greatly reduces the processor's response time to interrupts.

Hitachi's H8 series also offers high speed, executing instructions in as little as 200 ns . It comes with a wide variety of memory and I/O options, including EPROM, OTP, ROM, and ROM-less versions. First off the production line is the $\mathrm{H} 8 / 532$, an 8-bit unit with an ADC, 1 kbyte of RAM, 32 kbytes of EPROM, eight timers, a high-performance serial port, and $65 \mathrm{I} / \mathrm{O}$ lines.

Yet another controller family is available from Fujitsu Microelectronics Inc., San Jose, Calif.-the MB89700 series. The controllers pack up to 16 kbytes of ROM or EEPROM, 512 bytes of RAM, an 8-bit 8channel ADC, multiple counter-timers, a serial port, and up to 53 parallel I/O lines. They also have a relatively high-performance instruction set, executing the shortest commands in just 500 ns when running at 12 MHz .

Tackling the high-speed but lowend, minimal-feature set needs in the market, Microchip offers two simple controllers that rip through their instructions at just 200 to 400 ns each. The PIC16C54 and C55 have small ROMs and RAMs-just 512 bytes of EPROM and 32 bytes of RAM-and low-pin counts- 18 and 28 pins, re-spectively-to keep the chip prices to less than $\$ 1$ in large quantities, for the smallest unit.

Another high-speed offering comes from joint effort by National Semiconductor Corp., Santa Clara, Calif., and Sierra Semiconductor Corp., San Jose, Calif. The COP800, which also goes after the low end of the market, comes in versions with ROM or EEPROM on-chip and contains a simple mix of the basic I/O functions-parallel ports, countertimers, and simple serial ports that tie into National's family of serial peripheral support chips.

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## Transportation emerges as the next catalyst for electronic component technology.

IHE ELECTRONICS industry is undergoing a fundamental change, spurred on by new applications in vehicles. Automakers in the 1990s will increasingly depend on electronics to meet ever more strict safety and emissions standards. Moreover, manufacturers now see auto electronics technology as a means of getting a competitive edge. The result: Innovative applications in ride control, entertainment, and driving aids have already been developed, and indications are that the best is yet to come. The next phase of automobile development will treat the auto as a total integrated system which will rely on substantially higher levels of computer speed and memory.

Experts feel that automotive ap plications may stimulate the demand for electronics in the 1990 s as the PC did in the early 1980 s. Electronics companies that supply European and Japanese auto makers may benefit in particular. The reason is that these car builders tend to buy electronic components from outside suppliers. The Big Three automakers in Detroit, on the other hand, tend to obtain most of their electronics from internal divisions.

## TRENDS AND PROJECTIONS

According to Roger Grace Associates, a San Francisco-based consulting firm, automakers' increasing dependence on electronic solutions (along with a growing automotive market) will boost the worldwide automotive


ELECTRONIC CONTROLS for the power train of American cars are expected to account for the lion's share of the auto electronics market, according to Dataquest. Electronics for vehicular controls will experience the largest growth, while other market segments undergo little change.
electronics market from an estimated $\$ 12.5$ billion in 1987 to $\$ 35$ billion by 1995. Growth for North American auto electronics is equally dramatic. Where a 1970 model car from Ford Motor Co. contained about $\$ 25$ worth of electronics, the electronic content per vehicle of 1984 models averaged $\$ 585$. Projections for 1995 indicate a jump to $\$ 1,500$ per vehicle, and to $\$ 2,000$ by the end of the decade. Similarly, Chrysler Corp. estimates a jump from an average $\$ 350$ for a 1988 model to about $\$ 1,400$ for a 1992 model. The increased emphasis on automotive electronics is also reflected in a study conducted by The University of Michigan at Ann Arbor. The Delphi V study reports that electronics will represent $20 \%$ of a car's total value by the

## year 2000

Another study by Dataquest Inc., a San Jose-based market research and consulting firm, divides an estimated $\$ 2.6$ billion electronics market for the North American passenger-car industry into application areas. Most expenditures (40\%) will go toward power-train controls such as ignition systems, emission control, and engine and transmission control. Vehicle controls will comprise another $19 \%$, followed closely by the safety, comfort, and convenience (SCC) aspects of automotive design, which will consume $17 \%$ of the market. Currently the fastest growing segment of the automotive market, SCC includes keyless entry, automatic climate control, memory seats, and antiskid

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Sensors give the EFI controller information about the volume of air inducted so it can calculate the precise amount of fuel to be injected. Direct-measuring mass airflow sensors were not readily available for use in early EFI systems. Rather, a so-called speed density system was employed that measured engine speed, manifold vacuum, and inducted air temperature. Mass air intake
could only be interpolated from these secondary measurements. Inaccuracies resulted and had to be corrected.

However, Bosch of Germany recently developed an advanced mass airflow sensor that overcomes such drawbacks. The air meters use either a hot wire or hot film as the sensing element. Inducted air tends to cool the heated resistance element as it passes. The idea is to adjust current through the element to keep it at a constant temperature. The amount of current flow is proportional to airflow and, thus, serves as a measure of inducted air mass.

Exhaust emission and fuel economy requirements have forced engine designers to constantly improve fuel-management techniques. For example, systems are being designed to learn and
adapt to changing driving conditions and engine parameters. New solutions to internal-combustion engine-management problems include injection valves with split spray jets for engines containing four valves per cylinder, hot wire mass airflow meters, and highly integrated electronic ignition systems.

Two basic types of EFI systems are widely used. The first is called multiport injection where each cylinder has a separate fuel injector. The other is single-point injection where one main injector sits in the throttle body.

The Mono-Jetronic system by Bosch uses a simple single-point, throttlebody injection system (TBI). Gasoline is injected through a single solenoid-operated valve located above the throttle valve. This thoroughly atomizes fuel at the point of maximum air velocity.


gas. The intelligent system takes into consideration warm-up characteristics, differences in temperature, air pressure, and the engine condi tion.

The exhaust gas Lambda sensor developed by Bosch has been in production since 1976. It is used in the U.S., Japan, and Europe on more than 10 million vehicles.

The Lambda sensor sit in the exhaust gas stream, typically in the exhaust pipe

The TBI system consists of a throttle valve, injection valve, pressure regulator, throttle valve potentiometer, temperature sensor, and throttle valve servomotor. Because of the compact and lowprofile design, the throttle body can mount directly on the intake manifold.

Fuel-injection control and exhaust gas optimization is handled by an intelligent system, called Alpha-n control. This is a selfadapive controller that monitors the exhaust gas (Lambda) sensor, throttle valve angle, and engine speed. These inputs determine the fuel-control schedule, also known as the engine map.

The computer monitors exhaust gas composition and stores the data in memory. Next, it calculates an optimum operating point, outputs a new fuel-injection signal, then rechecks the exhaust
ahead of the catalytic converter. The external surface of a $\mathrm{Z}_{\mathrm{r}} \mathrm{O}_{2}$ ceramic sensing element protrudes into the exhaust gas flow and the inner surface is exposed to outside air. The $\mathrm{Z}_{\mathrm{r}} \mathrm{O}_{2}$ electrodes generate a small voltage that is proportional to the ratio of residual oxygen in the exhaust gas to oxygen in ambient air. When the ratio changes, the output voltage also changes.

The electronic control unit uses the Lambda output voltage as a factor in adjusting the air-fuel ratio. The exhaust gas composition is kept at a level that is optimum for treatment by the catalyst.

The Lambda sensor can only operate when the exhaust gas and manifold exceed $900^{\circ} \mathrm{C}$. On some engines, the time for Lambda sensor warm-up is prohibitive so a selfheating sensor was developed. This permits closed-loop control within 30 s of starting and during idle.
braking. Driver information systems, such as digital gages, service reminders, trip and navigation computers, and CRT and head-up displays, will account for another $14 \%$, and entertainment and body systems, such as multiplexing and lighting will comprise the rest.

## NEAR-TERM BENEFITS

New car models showcase ad vanced electronic control systems from the power train throughout the chassis. For example, General Motors Corp. plans to equip all luxury and full-size 1991 cars with ABS (antilock braking systems), which will become standard on all models by 1994. A typical ABS combines wheel-speed sensors, microcontrollers, and brake-pressure modulators to apply pulsed brake pressure at each wheel with out brake lockup.

Using many of the same components as ABS, traction control minimizes wheel slippage during vehicle acceleration. The frontwheel drive of the 1990 Cadillac Allante has a 2 -stage antislip sys tem made by Robert Bosch GmbH of Stuttgart, West Germany. The system combines front-axle traction control with Bosch's fourwheel ABS. Cadillac's 1992 El dorado and Seville are expected to be similarly equipped. Other U.S. cars expected to have traction control next year are the Lincoln Town Car from Ford Motor Co. and the New Yorker Fifth Avenue and Imperial from Chrysler Corp.

Active suspension improves vehicular handling and safety by changing the damping force of shock absorbers according to driving conditions. European and Japanese auto suppliers are leading the technology with systems that respond to such variables as road surface, axle load, wheel turning angle, and even side loads caused by wind.

The list goes on with antitheft and security systems. GM's PASSKey (personalized automotive security system) has an ignition key with an embedded resistor code which is read by electronic sensors in the ignition lock cylinder. If an
improper key is inserted, the system disables the starting and fuel systems. In a more aggressive system by Ford, opening the door turns on the horn, blinks the lights, and disables the starter coil when the dome light is lit by opening the door.
With the number of in-vehicle control modules doubling to over 60 during the past ten years, the size and weight of wire harnesses that interconnect these functions has increased dramatically. To reduce the complexity of such links, U.S. carmakers are turning to multiplexed designs. These use a microprocessor to send pulse-widthmodulated commands over a single wire to distributed output devices.

For example, an integrated system on the Buick Electra controls exterior mirrors, window motors, and door locks, and provides keyless entry, antitheft, and illuminated entry functions. Multiplexing reduced the number of wires passing through the door on the driver's side from 56 to 20 . Multiplexing is also being used in the Cadillac Allante to power inte rior lighting modules and in Chrysler's collision-detection system to allow an engine-control module, body computer, and tripfuel consumption computer to share data from various sensors.
The deployment of multi plexing technology in automotive applications has been delayed by a lack of international standards. In pursuit of a common approach to system protocol, standards com mittees in the U.S., Japan, and Europe have devised three classes of multiplexed systems as a starting point: Class A for low-speed body wiring and control functions, Class B for medium-speed data communications, and Class $C$ for high speed, real-time control. Further more, the Society of Automotive Engineering (SAE) is expected to complete its recommended practice (J1850) for Class B applications late this year.
Networking schemes will also show up in automotive applications. Bosch has developed a tech
nique called the automotive serial controller area network (CAN). Its protocol is supported in silicon from both Microcontroller Div. of Motorola Inc. (Austin, TX) and Intel Corp. (Santa Clara, CA) The network topology is a multimaster bus configuration that operates over either two shielded copper wires or fiber cable with a maximum bus length of 40 m and a data rate of $1 \mathrm{M} \mathrm{bit} / \mathrm{s}$. Other standards vying for universal acceptance are the CarLink protocol from Detroit's Big Three, and Automobile Bus and VAN (vehicle area network) in Europe.

## ON THE HORIZON

Even more intriguing features are in the planning stage. Digital signal-processing (DSP) techniques for speech synthesis and speech recognition will enable cellular telephones to be controlled by voice and talk to the driver. Cellular users can already use a system from L.A. Cellular in Los Angeles to receive traffic updates, vehicle location, and recommendations for hotels, restaurants, and trip designations.

For truck drivers, an emerging satellite technology called radio determination satellite service (RDSS) beams messages to areas not serviced by traditional communications systems. A terminal mounted in the cab displays the message on a screen, prints out a hardcopy, or delivers the message with a speech-synthesis system developed by Berkeley Speech Technologies of Berkeley, CA.

DSP technology is also behind an active noise-cancellation system being developed by Lotus Engineering in the United Kingdom. Aimed at reducing interior car noise, the system effectively "fingerprints" the sound picked up by several microphones distributed throughout the car, generates out-of-phase noise signals, and broadcasts this sound through the car's stereo speakers to cancel the noise. The system is expected to be offered to auto manufacturers within two years.

Although market growth beyond
the mid-1990s is difficult to predict, driver information systems that work with "smart highway" equipment are expected to help fuel continued growth. Japan and Europe are far and away the leaders in this and related technologies such as sophisticated vehicular navigation systems. However, an experimental program in the U.S. may spur interest among domestic carmakers.

In part because of its legendary traffic jams, California is experimenting with a smart highway program which could lead to a commercial system by the mid-nineties. Jointly conducted by the California Department of Transportation (Caltrans), the Federal Highway Administration, and General Motors Corp., the Pathfinder program was initiated in 1988 to relieve traffic tie-ups by integrating traffic information with a vehicle navigation system.

The $\$ 1.6$ million experiment uses 25 Oldsmobile Delta 88 sedans equipped with electronic navigation systems from Etak of Menlo Park, CA. The navigation system consists of a trunkmounted communications console and a display screen fitted on the dashboard. The two-way communications system is linked to other test vehicles and to the Caltrans traffic operations Center in Los Angeles. Drivers receive traffic information visually on the display screen or by computer-synthesized voice. The screen shows area street maps, tracks the vehicle's position, and gives alternate routes for avoiding traffic.

The ultimate solution for smart highways will need to include sensors along the highway for gaging traffic density and speed. A traffic control center will retransmit this information to properly equipped vehicles. The scheme might even be used to regulate vehicle speed automatically. Though the prospects for smart highway technology are dramatic, several major hurdles remain, such as high installation cost, software development, and the need for communications protocols.

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[^2]
## PASSENGER RESTRAINT SYSTEMS

Seat belts have been widely used on American vehicles since the early 1960s. But recently, lawmakers have dictated that cars be equipped with passive restraints.

Beginning with model year 1990, all U.S. cars must provide a passive restraint system for the driver, and in 1994 it must be available for the front seat passenger as well. Safety legislation places unusual de mands on designers to provide air bag systems that are reliable, do not deploy during minor fender-bend ers, can remain unused without de gradation for long periods, and can survive a crash but still deploy. Key to such a system is a trigger unit that senses the magnitude of the crash.


In a collision, a weight bends beammounted strain gages. The gages are a bridge circuit driven by a reference voltage. Strain changes gage resistance that is related to deceleration, unbalances the bridge, and signals the ECU. The ECU determines when the airbag should deploy.

The trigger unit must contain an acceleration sensor that accurately determines when to blow the air bag or tighten a seat belt. When an evaluation circuit detects de celeration indicative of serious ac cidents, a firing cartridge triggers an air bag and activates the seatbelt tensioner. In a frontal collision at $30 \mathrm{mph}(18 \mathrm{~km} / \mathrm{h})$ - the velocity needed to trigger the air bag - the
calculation is so fast that the cartridge fires within only 10 ms .

At the same time, the system must be sensitive enough to discern minor bumps that must not deploy the air bag. To prevent such problems, the device checks itself against data from test crashes to implement filtering action. For further reliability, a diagnostic program continuously checks the integrity of the entire electrical system, including the controller, cable and plug, and trigger unit

At specified deceleration, the trigger sends an electrical pulse to a detonator located in a gas genera-


Drivers are protected by an airbag in the steering wheel. Passengers are restrained by a special belt tensioner. Upon impact, a capsule is detonated by an electrical signal, and the resulting high pressure expels a fluid against turbine blades. The turbine turns the shaft, reverses the roll-up mechanism, and tightens the seat belt.
tor. The propellent detonates and fills the air bag. After 100 ms , the gas escapes through slots around the edge of the bag and collapses to absorb the kinetic energy of the driver's body.

The seat-belt tensioner for the front seat passenger operates from the same trigger unit as the air bag. Propellent forces fluid against impeller blades of a turbine. Turbine wheel rotation forces a roll-up shaft to tighten the belt

If the vehicle battery is disabled during an accident, a large capacitor gives enough backup power to operate the restraint system. A voltage converter assures that the full operating voltage is available for the trigger unit even if the battery drops as low as 4 Vdc .

A check lamp monitors the electrical system. The lamp illuminates when the ignition switch is on and remains lighted for about 10 s during a test cycle. If the system is operable, the lamp goes out. The lamp stays lighted if system service is needed.

Older restraint systems were primarily mechanical, employing several sensors that can monitor only two or three parameters. Acceleration in these devices contained mechanical switches that tended to cause inadvertent bag deployment. In contrast, newer electronic units contain more sophisticated acceleration sensors, with microprocessor and digital signal-processing ICs for control and monitoring functions.

The accelerometer in a Bosch AB6 system, for example, uses a spring-weight system and electronic circuitry. The dual element sensor detects vehicle de. celeration during frontal collision. The movable weight bends a spring that is bonded to four sensing resistors in a bridge circuit. The device generates a voltage that is proportional to the deceleration. The voltage is fed to an amplifier through a highpass filter.

A limiter stage follows that filters out high-frequency vibrations and subtracts signals less than 4 g accelerations encountered during normal driving conditions. The threshold deceleration value for the seat belt is relatively low. Belts tighten at a frontal collision speed of only $25 \mathrm{mph}(15 \mathrm{~km} / \mathrm{h})$. But the threshold level for the air bag is approximately $42 \mathrm{mph}(25 \mathrm{~km} / \mathrm{h})$.

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## CIRCLE 97

# Newly Developed ICs Driving Auto Electronics 

## Early automotive electronics had to make do with older semiconductors, but specially designed ICs are opening up a wide range of new applications.

## RANDY FRANK AUTOMOTIVE SEGMENT

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cARBURETORS and points have gone the way of horse shoes and saddles in the area of personal transportation Just as the automobile replaced the horse, increasingly sophisticated electronic control systems have made formerly essential components of the auto obsolete. The new systems improve performance, safety, convenience, communi cations, and manufacturability, and reduce emissions. In addition, they offer superior system diagnostics for improved serviceability, and system integration for increased reliability.

Although the microcontroller unit (MCU) is the critical control element in many current systems (12 applications depend on MCU technology), other semiconductor technologies will also play a key role in achieving high-volume production. Applications will include transient suppression, load controls that need more rugged and smarter power devices, and sensing of numerous vehicle inputs. In addition to supplying more precise control, the automotive semi conductors used in these applications must cope with one of the harsher environments for electronic components.

A good example of an automotive electronic control system is an antilock braking system (ABS). Virtu ally every auto manufacturer offers some sort of ABS on selected mod els. The typical ABS uses an MCU,
several sensors, semiconductor power devices, and hydraulic components to automatically pump the brakes rapidly and repeatedly. As a result, the driver can maintain steering ability and vehicle stability under difficult road surfaces, such as ice or wet asphalt and under hard braking conditions.

Functions performed by a typical ABS controller include actuation of solenoids, motors, and indicator lamps. A simplified model of a ge-
neric ABS system starts with inputs from either vehicle sensors (or switches) or driver-actuated switches (Fig. 1). These inputs are converted to a form that can be employed by the MCU. For simple switched inputs, the interface requirements are minimal or nonexistent, but many sensing inputs require amplification, buffering, temperature compensation, or analog-to-digital conversion.

If designers develop custom ICs


1. DESIGNERS CAN REDUCE the complexity and component count in an antilock braking system controller by developing custom ICs to link the sensors to the microcontroller unit. That interface circuitry is represented by the input-signal conditioning block in this simplified model.
to link the sensors to the MCU, the ABS controller's complexity and component count can be considerably reduced. For instance, combining signal conditioning with the sensing elements to allow bidirectional communication with the MCU creates a "smart sensor." Smart sensors are typically monolithic semiconductor devices that offer fewer components, improved reliability, and reduced system cost.

The MCU's low-current, digital output must be amplified before it can control the power semi conductor or relay that will ultimately actuate the desired solenoid, motor, lamp, or display. As in the smart sensor, output signal conditioning and power semi conductor devices can be combined into smart-power ICs.

Besides easing the interface task, smart I/O devices also protect the system and supply fault-detection or diagnostic capabilities. With increased vehicle-system complexity, circuit protection and diagnostics are viewed as mandatory for improving manufacturability, safety, and first-time success for repairs.

The sensors measure the speed of the wheels and send the MCU an ac signal whose frequency is proportional to the wheel's speed. When the MCU detects a wheel lock-up, the controller drives relays that activate solenoid valves. The valves control the hydraulic pressure applied to each wheel to keep it in an optimum slip range. Present systems use electrome chanical relays and bipolar power transistors or power FETs to activate the solenoids.

One of the many problems that confronts automotive-electronics designers is that the nominal $12-\mathrm{V}$ system in passenger cars is just about anything but 12 V . In typical operations, charging systems regulate the alternator's output to supply sufficient voltage to keep the battery charged under various temperature and load conditions. This voltage can range from over 15 V at $0^{\circ} \mathrm{F}$ to about 12 V at maximum un-der-hood temperatures.

2. AN ALTERNATOR PROTECTED with new avalanche rectifiers generates a much smaller voltage transient when it's disconnected from the charging circuit (dashed line). The vehicle's electronics can then use less expensive power FETs with lower breakdown voltages.

Moreover, electronic assemblies on cars must withstand reverse bat tery conditions to -13 V , jump starts from tow trucks ( 24 V ), short duration voltage transients that can easily exceed $\pm 100 \mathrm{~V}$, and long. duration ( 400 ms ) "load-dump" transients that can exceed +80 V . To prevent damage due to exces sive voltage, the systems must either use electronic components

3. A CURRENT-LIMITED FET is actually a small IC that holds the power FET plus a small-signal npn and related components.
As the npn unit turns on, gate drive is taken away from the FET, limiting its maximum current.
with a breakdown voltage that can withstand the various automotive voltages, or they must include protective circuits.

The load-dump effect is a good example of the varying-voltage problem and how it can be remedied. To the voltage-regulated alternator, a properly connected battery appears as a large capacitor, maintaining a low and constant bus voltage. However, when it's disconnected, the alternator suddenly generates a high (by automotive standards) voltage transient lasting several hundred milliseconds (Fig. 2). This transient can cause catastrophic damage to voltage-sensitive electronics.

A common and relatively inexpensive way to suppress these transients is to place a short voltage clipper-such as a Zener diode or surge supressor-across the input of the electronics. The suppressors, which for automotive applications are in the $24-\mathrm{V}$ to $32-\mathrm{V}$ range, must withstand the energy of the transient. This energy level is defined by many automotive specifications, the most common being $60-\mathrm{V}$ or $100-\mathrm{V}$ peak transients decaying exponentially to a $14-\mathrm{V}$ battery level
: in a time constant of 0.115 seconds.

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Therefore, for five time constants : ( 0.575 seconds), the suppressor must sustain this source or compliance voltage through a specified limiting resistance. The general range of resistor values produces surge currents in the $0.5-\mathrm{A}$ to $10-\mathrm{A}$ range. In addition, the specifications usually require that the device withstand 10 transient pulses, one every 30 seconds.

The duration of the load-dump transient will cause excessive junction temperatures even in many ruggedized power MOSFETs. However, using avalanche rectifiers : (such as Motorola's MR2535L) in the alternator can limit the max-: imum voltage to 40 V , even with 90 : A of reverse current for $80 \mu \mathrm{~s}$ at a junction temperature of $175^{\circ} \mathrm{C}$ : (Fig. 2, again).

This solution is very cost-effective because the on-resistance of : power FETs increases as their : breakdown voltage is increased to the 2.2 power. If a lower breakdown voltage can be used, the resulting reduction in on-resistance will re- : duce the cost of the power FETs, assuming that die size remains constant. Even if only a few power FETs are used, the savings can easily offset the cost of the avalanche ? rectifiers.

The spectrum of new automotive systems is pushing the development of power electronic components (including smart power ICs), which will ease system design and lower costs. The devices must control lighting, solenoid (inductive), and motor loads; illuminate displays; and perform dc-dc power conversion for 12 -to- $15-\mathrm{V}$, 12 -to- $24-\mathrm{V}$, and 12 -to- $48-\mathrm{V}$ systems (see the table). Many of these loads require relatively high in-rush and/or high steady-state currents, so to minimize power dissipation or heatsinking requirements large : output devices are used. Power : FETs are the most frequently used semiconductor device in these cost-sensitive applications.
A critical factor in under-hood automotive applications is a high : ambient temperature. As a result, the auto industry has pushed for : higher maximum junction temperatures for power devices. By using plastic packaging materials with a glass transition temperature approaching $200^{\circ} \mathrm{C}$ makes it possible for $175^{\circ} \mathrm{C}$ ratings for the newest, energy-rated power FETs, such as Motorola's E-FET power MOSFETs.

Another class of devices, ruggedized FETs like the Motorola TMOS series, are designer-friendly

4. A FULLY INTEGRATED pressure sensor contains the piezoresistive silicon sensor element and all of the necessary signal conditioning circuitry in the same die.
components that offer opportunities to reduce the number of circuit components because they're easier to interface and they perform special functions. For example, using tighter processing controls and techniques developed for fabricating MCU and memory chips has substantially improved the typical gate-rupture capability of the MTP50N06E (a $60-\mathrm{V}$, $50-\mathrm{A}, 0.028-\Omega$ power FET) from approximately 40 V to over 90 V . In many applications, this improvement can eliminate the need for an external Zener diode on the gate.

The procedures used to qualify new power devices are also being beefed up. Standard practice is to use $80 \%$ of the breakdown rating during reliability tests. For all power FETs, this has been increased to $100 \%$ of the maximum data-sheet rating to ensure that devices are stressed to the combined maximum temperature and voltage. For example, high-temperature gate bias tests are conducted at $100 \% \mathrm{~V}_{\mathrm{GS}}$ and $150^{\circ} \mathrm{C}$, and hightemperature reverse bias testing is done at $100 \% \mathrm{~V}_{\mathrm{Ds}}$ and $150^{\circ} \mathrm{C}$. Devices that can operate at $175^{\circ} \mathrm{C}$ are being qualified at the higher temperature as well.
Another important feature of power ICs is the ability to withstand a shorted load. A current-limited FET, such as the MLP1N08L, offers an integrated solution to protect semiconductor power devices from high in rush current as well as from short circuits. With a current rating of 1.1 A, minimum breakdown voltage of 80 V , and an on-resistance of $0.75 \Omega$ at $25^{\circ} \mathrm{C}$, the MLP1N08L limits the current that can flow in a logic-level power FET.

The current-limited FET incorporates a small-signal npn transistor and a diode from the gate to the source of an n-channel, logic-level FET (Fig. 3). Because it's designed for medium-speed switching applications that require rfi and emi to be minimized, the device has an integral resistor, $R_{1}$, that limits the gate charge and discharge rate. $\mathrm{R}_{2}$ is the sensing resistor that determines the maximum current level for forward biasing of the npn tran-

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## Siemens...pioneer and leader in SOT technology.

sistor. As the npn transistor turns on, gate drive is taken away from the power FET, limiting the current. The current limit is temperature dependent and decreases with increasing temperature, from 2.3 A at $25^{\circ} \mathrm{C}$ to 1.1 A at $150^{\circ} \mathrm{C}$. The MLP1N08L withstands over 8 kV in electrostatic discharge tests conducted with the human-bodymodel test circuit.

Because the MLP1N08L conducts current and dissipates power :
even during a short circuit, a heat sink is needed to keep the junction temperature below the maximum of $150^{\circ} \mathrm{C}$. To simplify the user's assembly process, therefore, the cur-rent-limited FET will also be offered in a fully isolated package whose thermal performance is similar to schemes that use additional hardware, such as mica washers or commercially available isolation pads. Both versions of the FET are suitable for low-cost applications. Two ideal automotive uses are in incandes. cent-lamp operation and in injector drivers.

A standard, logic-level power FET process produces the current-limited FET. The process, which can create small-signal devices as well as power ICs, enables designers to boost integration levels with only a small increase in area beyond that needed by the basic power FET and with the addition of only one masking layer. Consequently, the cost of the added circuitry is minimal compared with the total cost of the power switching device. An intermediate level between smart-power ICs and standard power MOSFETS, dubbed Smart discretes, differs from an IC process by the
lack of isolation between circuit elements (except for the oxide-isolated diodes). Eliminating the isolation keeps the cost down but also limits the circuits that can be obtained. Moreover, parasitic elements that can occur must be accounted for in each design.

Devices made possible by the Smartdiscrete process also help fill another need in automotive electronics: diagnostic signals. The process permits a simple opendrain diagnostic scheme that can indicate the presence of an open or short fault by sending a flag to an MCU. The diagnostic uses information supplied by either the currentlimit or thermal-sensing circuits.

Electronic engine control systems have used semiconductors for sensing manifold absolute pressure (MAP) for over seven years. Most frequently, a MAP sensor uses two silicon wafers to produce a piezoresistive silicon pressure sensor. The top wafer is etched until a thin, square diaphragm (approximately 1 mil thick) is created. The square area is extremely reproducible, as is the $54.7^{\circ}$ angle of the cavity wall. In addition to absolute pressure measurements, atmospheric pressure or a reference pressure can be applied to one side of the sensor through a hole that's micromachined in the second, constraint wafer.

The latest development in semiconductor pressure sensors is the integration of all conditioning circuitry on the same chip as the micromachined diaphragm. This circuitry adjusts the offset and span, compensates for temperature effects on both offset and span, and supplies an amplified signal (Fig. 4). The device is based upon one piezoresistive sensing element positioned at a $45^{\circ}$ angle in the center of the edge of the square diaphragm. The variation of the offset voltage and the full-scale span of this sensing element with temperature is highly predictable.

The added circuitry comprises an interactively laser-trimmed 4 stage network produced in one monolithic structure. The circuit uses silicon area that's needed to

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## AUTOMOTIVE



## 5. PROCESSING REVISIONS and improvements in process control have yielded LEDs whose current transfer ratio (a measure of the diode's light output) remained at $\mathbf{9 8 \%}$ of its initial level even after 7,500 hours.

mechanically support the diaphragm, so the die size for the fully signal-conditioned unit is 145 by 130 mils, compared to 120 by 120 mils for the uncompensated element.

The laser trim procedure yields a device (the MPX5100D) with a zero-pressure offset voltage of $0.5-\mathrm{V}$ nominal and a full-scale output voltage of 4.5 V when connected to a $5.0-\mathrm{V}$ supply. Therefore, the output dynamic range caused by an input pressure swing of $0-15 \mathrm{psi}$ is 4.0 V . The output depends on the supply voltage, which can be a maximum of 10 V .

To measure pressures or levels of vehicle fluids, semiconductor sensors must be exposed to one or more liquids (oil, fuel, coolant) detrimental to the semiconductor circuit's operation. Each application must be addressed separately, but cost limits generally prohibit the use of stainless steel isolation. Instead, more cost-effective protective polymers and chemically tolerant plastic and rubber materials are needed. Recently developed materials have made possible a 100 -psi sensor, the MPX700, that can measure oil pressure. A custom version of this unit has with-
stood over 1 million pressure cycles at high temperature.
Several manufacturers have adapted the techniques used for making piezoresistive pressure sensors to develop piezoresistive accelerometers. The piezoresistive accelerometer, however, with its beams and suspended mass, is considerably more complex than the simple diaphragm used in most pressure sensors. A three-layer structure is needed to supply overrange stops, a bending beam, and air damping.

Optical sensing techniques us ing infrared emitters and detectors have been used successfully for several years in rather benign environments to accurately sense rotational and linear motion. But their extension into automotive elec tronics has been delayed due to temperature sensitivity and sta bility problems with the emitters. With recent improvements, however, optical sensors can work at temperatures to $150^{\circ} \mathrm{C}$.

Detailed studies of LEDs from U.S. and non-U.S. sources showed that under accelerated conditions it's common for the diode to degrade $15 \%$ to $20 \%$ after 1000 hours of testing. Processing revisions and
improvements in process control implemented by Motorola have : greatly increased long-term reliability. The tests used the current transfer ratio (CTR)-the ratio of transistor collector current to forward current-as a measure the LED's light output. After 7500 hours, the average CTR of the improved LEDs was still almost $98 \%$ of their initial value (Fig. 5). This testing was performed at room temperature but tests are in progress to evaluate their operation at $85^{\circ} \mathrm{C}$, $105^{\circ} \mathrm{C}$, and $125^{\circ} \mathrm{C}$.
Several custom optical sensors have already been developed for automotive use. Two pairs of optical emitters and detectors were mounted at the end of the steering column to measure steering wheel turn angle direction and speed as part of a ride-control system. Multiple slots in a shutter interrupt the light path of the two pairs of emitters and detectors to provide the quadrature signal.

The MCU in the ride-control system uses an algorithm that determines the straight-ahead wheel position and then calculates the lateral acceleration that will result from the turn angle. If this lateral acceleration is above a programmed level, the shock absorber damping is switched to firm. The optical steering sensor also sends the MCU information that enables it to determine the rate at which the steering wheel is turning. If this rate is too high, the damping is switched to firm to supply more maneuverability
Perhaps the most significant as pect of semiconductors is the fabrication process, which offers the ability to integrate functions while aggressively reducing cost, especially in the volumes repre sented by automotive applications. In the 10 years since the first use of microprocessors in vehicles, prices have dropped by more than an order of magnitude, while features and computing capability in creased significantly. Continuing development ensures that new devices will be available for cost-effective performance in future automotive systems

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Wed like to name names, but the story is still unfolding.

One of the Big Three automobile manufacturers had been buying custom controllers for instrumentation lighting from an off-shore vendor-we're talking about a million pieces annually-when the dollar suddenly took a downturn.

Faced with continuing price increases, they went looking for a reliable domestic supplier. "All we need is a simple form, fit and function replacement," they said.

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up to 24 in ., speeds to $2 \mathrm{in} . / \mathrm{s}$ and with : loads up to $1,500 \mathrm{lb}$.

The weatherproof actuators, which consist of a motor, gearbox, and lead screw, are simple to install because complex wiring is not needed. Warner Electric/Dana Corp., 449 Gardner St., S. Beloit, IL 61080; (815).389-3771.

## COMPARATOR IC <br> TESTS CIRCUITS

THE AD22001 IS A five-channel comparator IC which tests the series circuit leading to a lamp to determine if a circuit is intact and a functional lamp is in the socket. This IC continually monitors the status of up to five bulbs. It features a wide temperature range ( -40 to $125^{\circ} \mathrm{C}$ ) and low voltage drop (nominal 1.75 mV at $22^{\circ} \mathrm{C}$ ).

The comparators, which can be connected to a car battery, are designed to check the amount of voltage applied to automotive lamps. The AD22001 generates a digital display to show
whether the amount of voltage is correct. In addition, the AD22001 is designed to provide an output to supply $15-\mathrm{V}$ CMOS interface circuits. Analog Devices Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062: (617)329-4700.

CIRCLE344

## HALL SENSOR <br> ACTIVATES LAMPS

THE UGQ5140K IS AN IC Hall sensor that can activate incandescent lamps, relays, and solenoids. The IC is equipped with an internal protection system. A voltage regulator on the chip allows use of the device to be used with supply voltages of 4.5 V to 28 V .
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Built according to military standards, the 86 meter includes probes and alligator clips. The 88 includes heat probes, needle point probes, and alligator clips. Both meters have safety features which warn users when leads are connected to the current jack

while the meter is selected for voltage or resistance. An added feature for the 88 meter is smoothing, which displays the average of eight measurements and provides a stable display for fluctuating signals. U.S. list prices are $\$ 459$ for the 88 and $\$ 399$ for the 86 . John Fluke Mfg. Co. Inc., P.O. Box 9090, Everett, WA 98026; (206)881-6966.

CIRCLE 346

## SURGE SUPPRESSORS CHALLENGE ZENER DIODES

THE V 24 ML FAMILY of surge suppressors are designed as alternatives to Zener diodes for automotive applications. The devices are rated for peak currents of up to $2,000 \mathrm{~A}(8 / 20-\mu \mathrm{s}$ current wave), have a jump-start overvoltage capability of 24.5 V for five minutes and can operate at a wide temperature range $\left(-55\right.$ to $\left.125^{\circ} \mathrm{C}\right)$ to handle the harsh environment of the auto-

## motive industry.

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Production quantities of the V24ML1210 are now available at $\$ .46$ each. The V24ML1206, 2820 and 2220 will be available at the end of this year. Harris Semiconductor, P.O. Box 883, Melbourne, FL 32901: 1-800-4-Harris, ext. 1066.

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THE CS-403 IS A LINEAR postregulator IC for switching power supplies. It features low drift and noise immunity and is the first regulator IC to provide an active reset. The reset functions at voltages as low as 3 V . The CS-403 also offers low quiescent current (for example, 3 mA for $0-\mathrm{mA}$ load; 5 mA for
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[^3]
# Careful Designing Is Needed To Meet Today's Stringent Timing Requirements And To Supply Clean Clock Signals. 

 L0w-Skew Cl0CK DRIVERS MAXIMIZE MPU SYSTEMSCHRIS HANKE AND GARY THARALSON
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oday's CISC and RISC microprocessor systems have frequencies that approach 40 to 50 MHz . As a result, maintaining a synchronous system demands precise, well-controlled clock signals. Many microprocessors also require input clock duty cycles very close to $50 \%$. These stringent timing requirements mandate the use of special, low-skew clock distribution circuits, or clock drivers. Just plugging one of these parts into a board doesn't ensure a trouble-free system, however. Meeting system timing requirements and providing clean clock signals call for careful design techniques for systems and pe boards.

Designers of microprocessor systems want to use as much of a clock cycle as possible without adding unnecessary timing guardbands. Unfortunately, propagation delays of peripheral logic don't scale with frequency. Therefore, as the


1. IN DEFINING CLOCK-DRIVER skew, $\mathrm{T}_{\text {os }}$ measures the difference between the fastest and slowest propagation delays between the outputs of one part. $\mathrm{T}_{\mathrm{PS}}$ measures the difference between the high-to-low and low-to-high transition for one output (pin). $\mathrm{T}_{\mathrm{PV}}$ measures the maximum propagation-delay delta between any pin on any part. clock period decreases, system designers have less time but the same logic delays to accomplish the function. How do designers gain more time? One option is to use a special clock source that minimizes clock "uncertainty."

A simple example illustrates this concept. At $33 \mathrm{MHz}, \mathrm{T}_{\text {cycle }}=30 \mathrm{~ns}$. An FCT240A octal inverter buffer, for example, has a high-low uncertainty of the $\min / \max$ spread of $t_{\text {PLH }}$ to $t_{\text {PHL }}$ of about 3.3 ns . If 1.7 ns of pin-to-pin skew due to the actual part and pcboard trace delays is also considered, then only 25 ns of the clock period is still available. The worst-case $t_{p}$ of clock-to-data valid on the 88200 M bus is 12 ns , which leaves only 13 ns to accomplish other functions. In this case, $17 \%$ of a cycle is required for clock distribution or clock "uncertainty." From a system designer's point of view, this percentage is an unacceptable penalty. At 50 MHz ,

## DESIGN APPLCATIONS <br> LOW-SKEW CLOCK DRIVERS


2. A SCALE REPLICATION of a RISC 88000 system board-layout section includes
an MC88100 CPU, MC88200 cache MMU devices, and MC88914 CMOS clock driver. The only
pc-board traces shown are the clock-output traces from the MC88914 to the various loads.
For this clock driver, the output-to-output skew ( $\mathrm{t}_{\text {oS }}$ ) is guaranteed to be less than 1 ns at
any given temperature, supply voltage, and fixed load up to 50 pF .
the penalty balloons to $25 \%$.
A maximum of $10 \%$ of the period allotted for clock distribution is an acceptable standard. If multiple levels of clock distribution (one clock driver's output feeding the inputs of several other clock drivers) are necessary owing to large clock fan-outs, the additional part-to-part skew variations add even more to the clock uncertainty. Standard logic has always been specified with a large (and conservative) delta between the minimum and maximum propagation delays. This delta creates excessive clock uncertainty, which system designers have been forced to design into their systems, even though it's unrealistic.

When system frequencies were below 16 MHz , this large clock penalty could be tolerated. As the preceding example points out, that's not the case today. A clock driver's specifications guarantee this min/max del-
ta to be a specific, small value. To reduce the clock overhead to manageable levels, a clock driver with minimal variation (less than $5 \%$ ) from a $50 \%$ duty cycle and guaranteed low output-to-output and part-to-part skew must be used.

## Clock-Skew Definitions

A typical clock driver has one input, which is usually driven by a crystal oscillator. The clock driver can have any number of outputs, which have a certain frequency relationship to the clock input. And clock-driver skew is typically defined by three different specifications (Fig. 1).

The first specification, $t_{0 S}$, measures the difference between the fastest and slowest propagation delays (any transition) between the outputs of one part. Note that this number must be 1 ns or less for highend systems.

The second specification, $\mathrm{t}_{\mathrm{PS}}$, measures the difference between the high-to-low and low-to-high transition for one output (pin). It defines how close to a $50 \%$ duty cycle the clock driver's outputs will be. For example, if this specification is 1 ns ( $\pm 0.5 \mathrm{~ns}$ ), the output duty cycle at 33 MHz is $50 \%( \pm 3.5 \%)$. A clock driver, which buffers only the crystal input, creates a 1:1 input to output frequency relationship. This can be a problem if a very tight tolerance to a $50 \%$ duty cycle is required.

## Output Duty Cycle

In this case, the output duty cycle depends on the input duty cycle, which isn't well-controlled in most crystal oscillators. The clock driver's outputs switching at half the input frequency $(\div 2)$ is a common relationship. This means that the outputs switch on only one edge of the oscillator. As a result, the output doesn't depend on the duty cycle of the input (crystal oscillator frequency is very stable).

The third specification, $t_{p V}$, measures the maximum propagation-delay delta between any given pin on any part. This specification defines the part-to-part variation between any clock driver (of the same device type) ever shipped. This number reflects the process variation inherent in any technology.

For CMOS, $\mathrm{t}_{\mathrm{PV}}$ is usually 3 ns or less (see "What's available now?"). High-performance ECL technologies can bring this number down into the 1 -to- 2 -ns range. Another way to minimize the part-to-part variation is to use a phase-locked-loop clock driver, which is just now becoming available.

When designing a clock driver into a system, it's important to give consideration to the skew specs that are usually specified at a fixed, lumped capacitive load. In a real system environment, the clock lines usually have various loads distributed over several inches of pc-board trace, which can contribute additional delay. Because the clock lines sometimes act as transmission lines, the system designer must use careful board-layout techniques to minimize the total


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- The TMS320C25 is limited to one access of external data every two cycles.
-The only zero-overhead loop the TMS320C25 can execute is one instruction repeated no more than 256 times.
- Circular buffers? The TMS320C25 doesn't support them.
-The TMS320C25 is programmed with 133 mnemonics like SPAC, BGEZ, MACD, XORX, and SBRK. A multiplication/accumulation is coded as MACD $>$ FF03,* - . While this might not scare the XORX out of you, it's not the easiest thing to debug or maintain.

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[^4]
# DESIGN APPLICATIONS <br> LOW-SKEW CLOCK DRIVERS 

system skew. In other words, just plugging a low-skew clock driver into a board won't solve all timing problems.

Consider a scale replication of a section of an RISC 88000 system board layout (Fig. 2). The board section includes the MC88100 CPU, the MC88200 cache MMU devices, and the MC88914 CMOS clock driver. The only pc-board traces shown are the clock-output traces from the MC88914 to the various loads. For this clock driver, the output-to-output skew ( $\mathrm{t}_{0 \mathrm{~S}}$ ) is guaranteed to be less than 1 ns at any given temperature, supply voltage, and fixed load up to 50 pF .

## Minimize Clock Skew

To calculate the total system skew, the difference in clock pcboard trace length and loading must be taken into account. For an unloaded pc-board trace, the signal delay per unit length, $\mathrm{t}_{\mathrm{pd}}$, depends only on the dielectric constant, $\mathrm{e}_{\mathrm{r}}$, of the board material. The characteristic impedance, $\mathrm{Z}_{\mathrm{o}}$, of the line depends upon $e_{r}$ and the trace's geometry. These relationships are depicted for a microstrip line (Fig. 3). The formulas for $\mathrm{t}_{\mathrm{pd}}$ and $\mathrm{Z}_{\mathrm{o}}$ are slightly different for other types of strip lines. For simplicity, all calculations in this article assume a microstrip line.

The equations are valid only for an unloaded trace. Loading down a line increases its delay and lowers its impedance. The signal-propagation delay ( $\mathrm{t}_{\mathrm{pd}}$ ) and characteristic impedance ( $\mathrm{Z}_{0}{ }^{\prime}$ ) due to a loaded trace are calculated by the formulas:
$\mathrm{t}_{\mathrm{pd}}{ }^{\prime}=\mathrm{t}_{\mathrm{pd}} \sqrt{1+\mathrm{C}_{\mathrm{d}} / \mathrm{C}_{\mathrm{o}}}$
$\mathrm{Z}_{\mathrm{o}}{ }^{\prime}=\mathrm{Z}_{\mathrm{o}} / \sqrt{1+\mathrm{C}_{\mathrm{d}} / \mathrm{C}_{\mathrm{o}}}$
$\mathrm{C}_{\mathrm{d}}$ is the distributed load capaci-tance-per-unit length, which is the total input capacitance of the receiving devices, divided by the length of the trace. $\mathrm{C}_{0}$ is the intrinsic capacitance of the trace, which is defined as:

$$
\mathrm{C}_{\mathrm{o}}=\mathrm{t}_{\mathrm{pd}} / \mathrm{Z}_{\mathrm{G}}
$$

Assuming typical microstrip dimensions and characteristics as $\mathrm{w}=$ $0.01 \mathrm{in} ., \mathrm{t}=0.002 \mathrm{in} ., \mathrm{h}=0.012 \mathrm{in}$., and $e_{r}=4.7$, the equations yield $Z_{o}=69.4$ $\Omega$ and $\mathrm{t}_{\mathrm{pd}}=0.144 \mathrm{~ns} /$ in. (Fig. 3,
again). $\mathrm{C}_{0}$ is then calculated as 2.075 $\mathrm{pF} / \mathrm{in}$. If it's assumed that an MC88100 or 88200 clock input load is 15 pF and that two of these loads, along with a $7-\mathrm{pF}$ FAST TTL load, are distributed along a $9.6-\mathrm{in}$. clock trace, $\mathrm{C}_{\mathrm{d}}=37 \mathrm{pF} / 9.6 \mathrm{in} .=3.85 \mathrm{pF} / \mathrm{in}$. The loaded trace propagation delay and characteristic impedance are then calculated as $\mathrm{t}_{\mathrm{pd}}{ }^{\prime}=0.243 \mathrm{~ns} / \mathrm{in}$. and $Z_{o}{ }^{\prime}=41 \Omega$.

In terms of trace c , the two

MC88200s are about 3 in. apart (Fig. 2, again). Using the calculated value of $t_{\text {pd }}$, the clock-signal skew due to the trace is about 0.7 ns . Because these two devices are on the same trace, this is the total clock skew between these devices. Careful inspection of all the clock traces shows that clock-signal skew was accounted for and minimized on the board layout. The longest distance between any 88000 devices on one clock trace is

## WHAT'S ADIILBLE NOWP

Low-skew clock drivers come in several technologies (see "How is a lowskew clock-driver chip achieved?", $p .96$ ). There are big differences among clock drivers in operating frequencies, voltage levels, power consumption, and packaging (see the table). Some drivers have features like poweron reset and external reset, which enables multiple clock-driver devices to be synchronized.

One clock driver design that can be helpful in large applications is the MC88915 phase-locked loop. Using an internal $\mathrm{V}_{\mathrm{Co}}$ and phase/ frequency detector, the PLL forces the driver output always to be in phase with the input signal. Thus, a system clock, which feeds several boards and may be of lower frequency, can be regenerated after crossing a backplane to ensure that each board is synchronous with the others.

| IMP1 | Binan | RGIBS |  |  |
| :---: | :---: | :---: | :---: | :---: |
| Parameter | CMOS ${ }^{4}$ | TTL ${ }^{5}$ | ECL ${ }^{6}$ | ECL/TTL ${ }^{7}$ |
| Max. input clock frequency (min.)(MHz) | 110 | 70 | 1000 | 135 |
| Output characteristics Number | $4 \mathrm{Q}+2 \mathrm{Q}^{\prime}$ | 4Q' | $9 Q+9 Q^{\prime}$ | 80Q-1:1 |
| Levels: (V) |  |  |  |  |
| $V_{\text {oh }}$ | $\mathrm{V}_{\mathrm{cc}}$ | 2.5 | -1.0 | 2.5 |
| $\mathrm{V}_{\mathrm{ol}}$ | GND | 0.5 | -1.6 | 0.5 |
| Timing (50-pF load; maximum values): tos-propagation delay skew ${ }^{1}(\mathrm{~ns})$ | 1 | 1 | 0.15 | 1 |
| $t_{\text {tPs }}$-output-to-output skew ${ }^{2}$ (ns) | , | 1.5 | 0.05 | 0.5 |
| tpv-part-to-part skew $^{3}(\mathrm{~ns})$ | 3 | 3 | 0.15 | 1 |
| Rise/fall times (ns) | $3 / 3^{\prime}$ | 3/3 | 0.5/0.5 | 1.7/1.6 |
| Drive sink/source current (mA) | 24/24 | 20/24 | $50 \Omega$ | 24/15 |
| Input requirements: |  |  |  |  |
| $V_{\text {ih }}(\mathrm{V})$ | 2.0 | 2.0 | -0.7 | PECL/TTL |
| $\mathrm{V}_{\text {il }}(\mathrm{V})$ | 0.8 | 0.8 | -1.4 | PECL/TTL |
| Pulse width (minimum) ( ns ) | 3 | 6 | 0.1 | 3.5 |
| Power: |  |  |  |  |
| Supply voltage (V) ICC (quiescent) (mA) | $\begin{gathered} +4.5 \text { to }+5.5 \\ 1.5 \end{gathered}$ | $\begin{gathered} +4.5 \text { to }+5.5 \\ 70 \end{gathered}$ | $\begin{gathered} -5.0 \text { to }-5.4 \\ 60 \end{gathered}$ | $\begin{gathered} +4.75 \text { to } 5.25 \\ 70 \end{gathered}$ |
| Packaging: | $\begin{aligned} & \text { 14-pin DIP } \\ & \text { 14-pin SOIC } \end{aligned}$ | $\begin{aligned} & \text { 14-pin DIP } \\ & \text { 14-pin SOIC } \end{aligned}$ | 28-pin PLCC | 28-pin PLCC |
| NOTES: |  |  |  |  |
| 1 It PHL actual-t ${ }_{\text {PLH }}$ actuall |  |  |  |  |
| 2 Any two outputs from a given input clock |  |  |  |  |
| 3 For a given set of conditions (that is, capacitive load, temperature, and $\mathrm{V}_{\mathrm{CC}}$ ) at each dev |  |  |  |  |
| 4 Reference data sheet MC74F803 |  |  |  |  |
| 5 Reference data sheets MC88913, 88914,88915 |  |  |  |  |
| 6 Reference data sheets MC10E111, 100E111 |  |  |  |  |
| 7 Reference data sheets MC10H, 100H640, 641, 642, 643 |  |  |  |  |



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## DESIGN APPLICATIONS <br> LOW-SKEW CLIOCK DRIVERS

about 4.5 in., which translates to about 1.1 ns of skew.

The two 88000 devices farthest from the clock driver (traces a and c) are at about the same distance along their respective traces. This makes the clock skew between them the 1 ns guaranteed from output to output of the clock driver. As a result, the worst-case clock skew between any two devices on this board is about 2.1 ns , which at 33 MHz is $7 \%$ of the period. Unless a designer pays careful attention to matching the clock traces on the board, this number could easily exceed 3 ns and the $10 \%$ cutoff point, even if a low-skew clock driver is used.

Transmission-line effects occur when a large mismatch is present between the characteristic impedance of the line and the input or output impedances of the receiving or driving device. The basic guideline to determine if a pc-board trace needs to be examined for transmission-line effects is as follows: If the smaller of the driving device's rise or fall time is less than three times the propagation delay of a switching wave through a trace, transmission-line effects will be present. This relation-

3. IN CALCULATING SYSTEM skew, the difference in clock pc-board trace length and loading must be taken into account. For an unloaded pc-board trace, the signal delay per unit length, $\mathrm{t}_{\mathrm{pd}}$, depends only on the dielectric constant, $\mathrm{e}_{\mathrm{r}}$, of the board material. These relationships are depicted for a microstrip line.
ship can be stated as an equation:
$3 \times \mathrm{t}_{\text {pd }}{ }^{\prime} \times$ trace length $\leq \mathrm{t}_{\text {rise }}$ or $\mathrm{t}_{\text {fall }}$
For the MC88914 CMOS clock driver described previously, rise and fall times are typically 1.5 ns or less (from $20 \%$ to $80 \%$ of $\mathrm{V}_{\mathrm{CC}}$ ). Analyzing the clock-trace characteristics presented earlier for transmission line effects means that $3 \times 0.243 \mathrm{~ns} / \mathrm{in}$. $\times$ trace length $\leq 1.0 \mathrm{~ns}$ ( 1 ns is used as "fastest" rise or fall time). Therefore, the trace length must be less than 1.5 in. for the transmission-line effects to be masked by the rise and fall times.

Consider then a clocksignal waveform seen at the receiver end of an unterminated 0.5 -in. trace and an unterminated $9-\mathrm{in}$. trace (Fig. 4). These results, which were obtained using Spice simulations, may not be exact but are adequate to predict trends and for comparison purposes. The 9 -in. trace, well beyond the $1.5-\mathrm{in}$. limit where transmission-line effects come into play, exhibits unacceptable switching characteristics caused by reflections shuttling along the trace. Even the $0.5-\mathrm{in}$. line exhibits substantial overshoot and undershoot. At these edge rates, any unterminated line shows some overshoot and undershoot.

Clock lines shorter than 1.0 to 1.5 in. are unrealistic on a practical board layout. As a result, CMOS clock lines should be terminated if the driver has 1 - to 2 -ns edge rates. Termination, which closely matches the line to the load or source impedances, has been a reality in the ECL world for many years. But, CMOS and TTL devices have only recently reached the speeds and edge rates that require termination. CMOS outputs further complicate the issue by driving from rail to rail ( 5 V ), with slew rates exceeding those of high-

4. SPICE SIMULATIONS, run with parameters of $25^{\circ}$ and $\mathbf{V}_{\mathrm{cc}}$ of 5 V , were done for an unterminated, 0.5 -in., $41-\Omega$ transmission line (a) and an unterminated, 9 in., $41-\Omega$ transmission line (b). The 9 in. trace shows unacceptable switching characteristics caused by reflections moving back and forth along the trace. Even the $0.5-\mathrm{in}$. line shows a great deal of overshoot and undershoot.

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performance ECL devices.
Because clock lines are driven only from one location, they lend themselves to termination more easily than bus lines, which are commonly driven from multiple locations. Digital systems use various types of termination techniques (Fig. 5). Because no single termination scheme is optimal in all cases, the trade-offs in the use of each needs to be discussed and recommendations made specific to clock drivers.

The driving device in the Spice simulations of various termination schemes was the MC88914 output buffer. In all simulations, it drove a $9-\mathrm{in}$., $41-\Omega$ transmission line. The simulations were run using model parameters at $25^{\circ} \mathrm{C}$ and $\mathrm{V}_{\mathrm{CC}}$ of 5.0 V .

## Series Termination

Series termination is recommended if the load is lumped at the end of the trace and the output impedance of the driving device is less than the loaded characteristic impedance of the trace. It's also recommended when a minimum number of components is required. The problem with series termination arises when the driving device has different output impedance values in the low and high states, which occurs in TTL and some CMOS devices. A well-designed CMOS clock driver should have nearly equal output impedances in the high and low states, avoiding this problem. An additional advantage is that series termination doesn't create a dc current path.

As a result, the $V_{\mathrm{OL}}$ and $\mathrm{V}_{\mathrm{OH}}$ levels aren't degraded. The Spice-generated waveforms of series termination show that this termination effectively masks transmission-line effects.

If each clock output is driving only one device, series termination is recommended. Because this isn't realistic in most systems, series termination isn't generally advised for clockline termination.

Parallel termination uses one resistor tied to ground or $\mathrm{V}_{\mathrm{CC}}$, whose value is equal to the line's characteristic impedance. Its major disadvantage is the dc current path it creates when the driver is in the high state (if the resistor is tied to ground). This

## HOW IS A LOW-SKEW CIOCK DRIVER CHIP AGHIEVEI?

Designing and manufacturing a low-skew clockdriver chip calls for many of the same factors in system design, but obviously on a much smaller scale. Careful circuit design, symmetrical layout techniques, and good control of the fabrication process are needed for low output-to-output and part-to-part skew characteristics. First, using circuit design methods, the high-to-low and low-tohigh transitions from the clock input to the distributed outputs must be as close as possible to each other. Then the rise and fall times of a signal out of the output buffers (drivers) must be evenly matched. This is done by matching the output impedances of the pull-up and pull-down transistors. Satisfying these two requirements results in a $50 \%$ duty cycle.

The design-related methods depend on computer simulations and the accuracy of the simulator models. But when the circuit is implemented in silicon, layout parasitics can adversely affect circuit performance. Chip-level parasitics are similar to the pe-board trace parasitics that must be accounted for when calculating signal delays on the board level. However, one advantage at the chip level, due to the short length of signal lines, is that transmis-sion-line effects are negligible. A clock-distribution part has several outputs, usually at least four, whose propagation delay skews must be matched within a given tight specification (for example, less than 1 ns ). If the path to one output has more layout-induced parasitic resistance and/or capacitance than the other outputs, then its propagation delay might be slower than the others by more than the specified limit.

Layout parasitics are always present, therefore the trick is to match the parasitics of each output as closely as possible. This means that the layout must be
symmetrical, with the path from clock input to each output looking almost identical. As such, the length and parasitic resistance and capacitance of each signal path must be equal. ECL's extremely high switching speeds also demand that the characteristic impedance of the paths be tailored to avoid reflections at the branching points.

Packaging effects must also be considered to minimize skew. The leads of a standard DIP package have large and variable inductive parasitics. As a result, the outputs must be connected to package leads that have matched in-ductances-that is, symmetrical pins on opposite sides of the package. Again, for ECL, the high speeds demand a package such as a plastic leaded chip carrier, which minimizes the inductive and capacitive effects of the pins. External impedance matching of clock lines is also important.

Within a part, the circuit design, layout, and packaging techniques that are described guarantee that one part will have low output skew. However, in a synchronous system using more than one clock driver device, the part-topart output skew must be within a reasonable tolerance (two to three times the output-to-output skew). Achieving this goal requires tight control over the fabrication process. CMOS particularly doesn't have ECL's temperature and voltage compensation features. How well critical process parameters, such as channel length and threshold voltage, are held within a small tolerance determines how small the part-to-part variation will be.

## References

1. "A Clock Distribution Circuit with a $100-\mathrm{ps}$ Skew Window" by Rajnish Maini, James McDonald, and Lou Spangler, IEEE 1987 BTCM.
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causes excessive power dissipation and $V_{O H}$ level degradation. Because a clock driver output is always switching, the de-current-draw argument loses some credibility at higher frequencies. For one thing, the ac switching current becomes a major component of the overall current. Therefore, the key consideration in parallel termination is how much $\mathrm{V}_{\mathrm{OH}}$ degradation can be tolerated by the receiving devices. This termination technique is effective in minimizing switching noise. Nonetheless, Thevenin termination has some advantages compared with parallel termination.

Thevenin termination uses one resistor tied to ground and a second tied to $\mathrm{V}_{\mathrm{CC}}$. When designers use this type of termination, it's important that they consider the choice of resistor values to avoid settling of the voltage between the high and low logic levels of the receiving device. TTL designers commonly use a 220 / 330 resistor value ratio, but CMOS is somewhat tricky because the switch point is at $\mathrm{V}_{\mathrm{CC}} / 2$. With a $1: 1$ resistor ratio, a failure at the driver output would cause the line to settle at 2.5 V . Besides causing system-debugging problems, this could lead to potential damage to the receiving devices.

## $\eta$ HEVENIN AND AC TERMINATION ARE THE RECOMMENDED SCHEMES FOR CLOCK LINES, BUT IT DEPENDS ON THE CLOCK'S FREQUENCY.

In Thevenin termination, the parallel equivalent value of the two resistors should equal the line's characteristic impedance. A dc path does exist in both the high and low states. However, it's better than parallel termination because the resistance in the Thevenin dc path is at least two times greater.

The Thevenin termination waveforms exhibit characteristics similar to those for parallel termination but with less $\mathrm{V}_{\mathrm{OH}}$ degradation (Fig. 6). The only real advantage of parallel

5. COMMON TERMINATION TECHNIQUES, represented shematically, are a transmission line with no termination (a); a transmission line with series termination (b); a transmission line with parallel termination (c); a transmission line with Thevenin termination (d); and a transmission line with ac termination (e).
over Thevenin is fewer resistors (half as many), resulting in more available board space. If space isn't a factor, Thevenin termination is recommended over parallel.

Ac termination typically uses a resistor and capacitor in series to ground. The capacitor blocks de current flow but allows the ac signal to flow to ground during switching. The time constant of the resistor and capacitor must be greater than twice the loaded line delay. Ac termination is recommended because of its low power dissipation and the availability of the resistor and capacitor in single-in-line packages (SIP). A pullup resistor to $\mathrm{V}_{\mathrm{CC}}$ is sometimes added to set the dc level at a certain point because of the failure condition described in regard to Thevenin termination. As noted earlier, the argument of lower dc current is less convincing at high frequencies. The acterminated waveform walks out slightly toward the end of a high-tolow or low-to-high transition, making it somewhat less desirable than Thevenin termination at higher frequencies.

Thevenin and ac termination are the two recommended termination schemes for clock lines, but it depends on the clock's frequency. It's safe to assume that ac is the best choice at frequencies of 25 MHz and below. If the system frequency could reach 40 MHz and beyond, Thevenin becomes the better choice.
The results presented might imply that terminating the clock lines completely solves noise problems, but termination can cause secondary problems with some logic devices. Termination acts to reduce the noise seen at the receiver, but that noise actually appears as additional current and noise at the driving device's output. If the internal and input logic on the source device isn't sufficiently decoupled on chip from the high-current outputs, internal threshold problems can occur. This phenomenon is commonly known as "dynamic threshold." It's usually evidenced by glitches appearing on the outputs of a fast, high-current drive logic device as it switches high or low. This is most severe on "ACT" devices,

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## DESIGN APPICHITIONS <br> LOW-SKEW CLOCK DRIVERS


6. SPICE SIMULATIONS, run with parameters of $25^{\circ}$ and $V_{\text {CC }}$ of 5 V , were done for various terminations of a 9 in., $41-\Omega$ transmission line. Simulation results are for series termination (a); parallel termination (b); Thevenin termination (c); and ac termination (d). The waveforms for Thevenin termination show similar characteristics to those of the waveforms for parallel termination, but there is less $\mathrm{V}_{\mathrm{OH}}$ degradation.
which have high current and high slew-rate CMOS outputs, along with TTL inputs, which have low noise immunity. This problem can be minimized by decoupling the internal ground and $V_{\text {CC }}$ supplies on-chip and in the package.
This decoupling is accomplished by having separate "quiet" ground and $V_{C C}$ pads on-chip, which supply the input circuitry's ground and $\mathrm{V}_{\mathrm{CC}}$ references. These pads are then tied to extra "quiet" ground and "quiet" $\mathrm{V}_{\mathrm{CC}}$ pins on the package or to special "split leads." These resemble a tuning fork and use the leadframe inductance to accomplish the decoupling. When choosing a clock source, designers should note that the part must have one of these decoupling schemes.

A reliable, high-frequency microprocessor system requires a lowskew clock driver, along with special attention to the board layout of clock traces. The line lengths and loading must be matched to avoid excessive signal skew between CPUs, cache MMUs, and other critical peripheral devices.
To ensure a clean clock signal throughout the system, clock traces must also be terminated in some fashion. Carefully addressing these issues early in the design cycle helps designers to guarantee optimal system performance.

References

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2. Application Note AN1051, Trans-
mission Line Effects in PCB Applications, Motorola Inc., 1990.
3. Motorola FACT Data, Motorola Inc., 1990.

Chris Hanke, a CMOS design engineer in Motorola's Logic IC Division, received BSChemEng and MSEE degrees from Rensselaer Polytechnic Institute, Troy, N. Y.

Gary C. Tharalson, a new product planner in Motorola's Logic IC Division, Mesa, Ariz., received a BSEE from the University of Minnesota and an MBA from Arizona State University.

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| Moderately | 542 |
| Slightly | 543 |

 pc board area as a TO-8 and can take tougher punishment with leads that won't break off. Models are unconditionally stable and available covering frequency ranges 0.5 to

1000 MHz , NF as low as 2.8 dB , and power output as high as +15 dBm . Prices start at only $\$ 13.95$, including screening, thermal shock $-55^{\circ} \mathrm{C}$ to +100 C , fine and gross leak, and burn-in for 96 hours at $100^{\circ} \mathrm{C}$ under normal operating voltage and current.
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|  | FREQ. <br> RANGE <br> (MHz) | GAIN dB |  | MAX. OUT/PWR $\dagger$ | $\begin{aligned} & \mathrm{NF} \\ & \mathrm{~dB} \end{aligned}$ | $\begin{aligned} & \text { DC PWR } \\ & 12 \mathrm{~V} \text {, } \end{aligned}$ | PRICE <br> \$ ea. |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| MODEL | $\mathrm{f}_{\mathrm{L}}$ to fu | min | flatnesst† | dBm | (typ) | mA | (10-24) |
| MAN-1 | 0.5-500 | 28 | 1.0 | 8 | 4.5 | 60 | 13.95 |
| MAN-2 | 0.5-1000 | 19 | 1.5 | 7 | 6.0 | 85 | 15.95 |
| MAN-1LN | 0.5-500 | 28 | 1.0 | 8 | 2.8 | 60 | 15.95 |
| $\triangle$ MAN-1HLN | 10-500 | 10 | 0.8 | 15 | 3.7 | 70 | 15.95 |
| * MAN-1AD | 5.500 | 16 | 0.5 | 6 | 7.2 | 85 | 24.95 |

[^6]Max input power (no damage) +15 dBm ; VSWR in/out 1.8:1 max.
*Active Directivity (difference between reverse and forward gain) 30 dB typ.
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# 21 TeST GANGED <br> 521 P0T TRACKING 

M. S. NAGARAJ

Isro Satellite Centre, Digital Systems Div., Airport Rd., Vimanapura P.O., Bangalore 560 017, India.

The values shown in the circuit are for $10-\mathrm{k} \Omega$ ganged potentiometers. For other values, let resistors $\mathrm{R}_{3-6}$ equal a potentiometer value of 0.1 to restrict the maximum output voltages of $U_{1}$ and $U_{3}$ to within $80 \%$ of the supply voltages.

Ganged potentiometers are widely used in audio stereo systems and in many instrumentation circuits. Often, the performance deficiencies in this type of equipment can be traced back to the ganged potentiometers, which have two resistance tracks that are out of step. Here, a circuit is developed to rapidly test the ganged-potentiometer tracking. The tracking error can be measured with an accuracy of better than $1 \%$ at all shaftslider positions in the entire electrical travel of the potentiometer.

The circuit uses ultra low-offsetvoltage op amps, eliminating the need for offset nulling (see the figure). The inverting amp built around op amps $\mathrm{U}_{1}$ and $\mathrm{U}_{3}$ uses the potentiometers under test as feedback resistors.

At any given shaft-slider position, let $R_{1} / R_{2}=n$ volts at point $A$. As a result, $\mathrm{V}_{\mathrm{A}}=1 \mathrm{~V} \times\left(\mathrm{R}_{1} \mathrm{k} \Omega / 1 \mathrm{k} \Omega\right)=\mathrm{R}_{1}=$ $\mathrm{nR}_{2}$.

The voltage at point $\mathrm{D}, \mathrm{V}_{\mathrm{D}}=\mathrm{V}_{\mathrm{C}} /$ gain of $\mathrm{U}_{3}=n \mathrm{R}_{2} /\left(\mathrm{R}_{2} / 1\right)=\mathrm{n}$, and at point $\mathrm{E}, \mathrm{V}_{\mathrm{E}}=10 \times(\mathrm{n}-1)$.

These relationships show that $\mathrm{V}_{\mathrm{E}}$ is positive when $R_{1}>R_{2}$, zero when $R_{1}=R_{2}$, and negative when $R_{1}<R_{2}$. One volt at the circuit's output corresponds to a tracking error of $10 \%$.

## IFD Winners

IFD Winner for April 26, 1990
Kerry Lacanette, National Semiconductor, 2900 Semiconductor Dr., P.O. Box 58090, Santa Clara, CA 95052; His idea: "Create an Accurate Noise Generator."

IFD Winner for May 10, 1990 Gary Multer, Sen Majumdar, and Raj Pisupati, Digital Equipment Corp., 20 Hampden St., Boston, MA 02119; His idea: "Drive Stepper Motor, Cut Cost."


THIS CIRCUIT MEASURES THE TRACKING ERROR of ganged
potentiometers. Less than $1 \%$ accuracy can be achieved at all shaft-slider positions of the potentiometer.

## ₹2) BuILD A PRECISE, Low-Current Source

JOHN GUY

Precision Monolithics Inc., 1500 Space Park Dr., P.O. Box 58020, Santa Clara, CA 95052; (408) 727-9222.

Acurrent source that attains a resolution as low as 10 pA is useful in applications where a precise, low-value current is needed. When the circuit forces current into ground, the output remains within $2 \%$ of the ideal current over the $\pm 100-\mathrm{nA}$ range. Over the -4 to $+3.5-\mathrm{V}$ compliance range, the error that appears is less than $5 \%$. This accuracy results from using an OP80 op amp from Precision Monolithics in the feedback loop
(see the figure, $p .106$, top). The OP80 has an $\mathrm{I}_{\mathrm{B}}$ of 200 fA typical.
For a given voltage $\left(\mathrm{V}_{\mathrm{in}}\right)$, amp $\mathrm{U}_{1 \mathrm{~A}}$ generates an output voltage so that the current through $\mathrm{R}_{5}$ equals $\mathrm{V}_{\text {in }}$ divided by $R_{5}(10 \mathrm{M} \Omega)$. This current causes a voltage drop across $R_{5}$, which is sensed by the unity-gain-differential amp consisting of $\mathrm{U}_{1 \mathrm{~B}}$ and $\mathrm{U}_{2}$. Thatamp's output is connected to the inverting input of $\mathrm{U}_{1 \mathrm{~A}}$, completing the feedback loop.

The noise in the circuit is of partic-

## IDEAS FOR DESIGN

ular concern, especially that produced by resistor $\mathrm{R}_{5}$. The circuit is limited to low-frequency and dc applications due to its $400-\mathrm{nV} / \sqrt{\mathrm{Hz}}$ noise. For applications that don't require the circuit's $10-\mathrm{pA}$ output, lower values of $R_{5}$ can be substituted. This will cause an increase in bandwidth.

Because a high impedance exists at the input, a 10:1 resistive attenuator can be added to enhance the resolution of the input source. The output of the circuit is trimmed to 0 pA , while the input is grounded. As the circuit is assembled, care should be taken to prevent leakage-current errors. When the prototype was built, $\mathrm{R}_{5}$ was mounted on teflon standoffs and pin 3 of $\mathrm{U}_{2}$ was soldered directly to $\mathrm{R}_{5}$. .


A HIGH-ACCURACY, LOW-VALUE CIRCUIT can be achieved by using an 0P80 op amp in the feedback loop of a current-source circuit.

# 2? Find Temp With RTD, Varied Current 

ROBERT MAYER

Peerless Instrument Co., 90-15 Corona Ave., Elmhurst, NY 11373; (718) 592-3300.

$T$o measure temperature with a resistance-temperature detector (RTD), a known current is passed through the RTD as the voltage across it is measured. By applying Ohm's law, the RTD's resistance is calculated as V/ I. This resistance then corresponds to a one-to-one function of the RTD's temperature.

The RTD's resistance can also be found by determining the current and voltage separately (see the figure). When the 7407 open-collector output transistor is on, current I flows through $R_{1}, R_{2}$, and the RTD.

## UOTE!

Read all the Ideas for Design in this issue, select your favorite, and circle the appropriate number on the Reader Service Card. The winner receives a $\$ 150$ Best-of-Issue award and becomes eligible for a $\$ 1,500$ Idea-of-the-Year award.

106
$\mathrm{R}_{1}$ limits this current to a maximum of 33 mA .

A data-acquisition system mea-


TEMPERATURE CAN BE measured with an RTD by taking two voltage measurements-one across $\mathrm{R}_{2}$ and the other across the RTD. The current and then the RTD resistance are then calculated. The temperature is then a function of the resistance.
sures the voltage across $R_{2}$ and across the RTD. The circuit's microprocessor (not shown in the figure) divides $V_{R 2}$ by $R_{2}$ to find I, then divides $V_{R T D}$ by $I$ to find the RTD resistance. When these steps are followed, I drops out of the equation leaving:
RTD resistance $=\mathrm{R}_{2} \times \mathrm{V}_{\mathrm{RTD}} / \mathrm{V}_{\mathrm{R} 2}$.
This approach offers four advantages over conventional methods that employ a constant-current source to supply the known current. First, the signal-to-noise ratio (SNR) is excellent because a large RTD voltage is induced by a large current. Second, only one precision component $\left(R_{2}\right)$ is required to supply a highaccuracy result. A constant-current source with the same accuracy and SNR would need additional high-precision components.
The third advantage of this method is that the current can be switched on and off by a TTL signal. Errors caused by selfheating of the RTD can be can be reduced by turning the current off between measurements. Finally, the RTD resistance can vary over a large range. The constant-cur-rent-source method has a much smaller range because it can't supply the required current when the RTD resistance exceeds the quotient of $\mathrm{V}_{\text {supply }} / \mathrm{I}_{\text {constant }} . \square$


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CIRCLE 125

## 68040 SYSTEMS EQUIPPED YOU'LL NOTICE A

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Samsung System Accelerators, ${ }^{\mathrm{TIM}}$, the part is highly integrated and inherently fast. And as the cutting edge in memory control, it can help you simply and economically enhance even 68040 performance.

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to the microprocessor. Which saves you dollars, board real estate, and

| C8030 PERFORMANCE SUMMARY |  |  |  |  |
| :--- | :---: | :--- | :---: | :---: |
| Accesd Clocks | DRAM Speed | Frequency $($ Mhz $)$ |  |  |
| $4-2-2-2$ | 70 ns | 20 |  |  |
| $5-2-2-2$ | 120 ns | 20 |  |  |
| $5-2-2-2$ | 80 ns | 25 |  |  |
| $6-2-2-2$ | 120 ns | 25 |  |  |
| $6-2-2-2$ | 80 ns | 33 |  |  |
| $7-2-2-2$ | 100 ns | 33 |  |  |
| $\quad \mathbf{6 8 0 4 0}$ |  |  |  | PERFORMANCE SUMMARY |
| Acceso Clocks | DRAM Speed | Frequency $($ Mhz $)$ |  |  |
| $3-2-2-2$ | 80 ns | 25 |  |  |
| $5-2-2-2$ | 100 ns | 25 |  |  |
| $6-2-2-2$ | 120 ns | 25 |  |  |
| $5-2-2-2$ | 80 ns | 33 |  |  |
| $6-2-2-2$ | 100 ns | 33 |  |  |

design time, since it means you don't need additional glue logic.

Ease of design is another advantage. As a glance at our System Design Guides will show, it's an unusually simple chip to design in.

All in all, we believe the 84 C 31 is the best memory controller solution available today.

For details on using it to make your designs take off, contact DRAM Controller Marketing, Samsung Semiconductor, 3725 No. First St., San Jose, CA 95134. Or call 1-800-6695400, or 408-954-7229.

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# Workstations And HDTV Get Triple 10-Bit $80-\mathrm{MHz}$ DAC ICS Frank goonesocaf 

For the first time, designers of high-resolution computer graphics systems can get 10 bit video digital-to-analog converter (DAC) ICs. Moreover, they can get three of these $80-\mathrm{MHz}$ DACs on a single chip for under $\$ 20$. The ADV7121/22 triple DACs from Analog Devices can resolve over one billion colors at any given time, a capability that's well beyond that of the human eye. Such capability is needed by sophisticated color graphics systems such as HDTV and workstations, to linearize the transferfunction curve of drive current to light output (also known as a Gamma curve) of the display system (see the figure).

The DACS are aimed at any highresolution color graphics application employing a true-color system or a special lookup table. These include workstations, medical imaging, and even high-end PCs.

With the higher 10 -bit resolution (instead of the more common 6 or 8 bits), calculations for the required color shadings become simpler. For the graphic designer in need of a color with half the intensity, it's much easier to call out a digital half-code than to calculate which code associated with the given display system will produce the desired color.

This feature is in such high demand that NHK (the Japanese equivalent of the FCC) designed the 7121 into the prototype system they use for receiving their MUSE HDTV standard. Other HDTV development teams in both the U.S. and Europe are already using these DACs for their prototype systems. The DACs also comply with the Society for Motion Pictures and Television Engineering (SMPTE) 240, a proposed U.S. production HDTV standard.

At the heart of each ADV7121 and ADV7122 lie three RGB, 10-bit 30 -, $50-$ or $80-\mathrm{MHz}$ DACs, each with its own TTL-compatible latched pixel input port. An additional input is provided for the pixel clock which
strobes the latches to refresh the DAC outputs. A reference amplifier converts an external 1.235-V reference to a 17.7 -to- $18.5-\mathrm{mA}$ fullscale current source for each DAC. A variable resistor connected to the amplifier sets the exact fullscale cur-rent-the white level for all three DACs. The current sources are complient from -1.4 to +1 V . Thus, each DAC can develop 0.5 V at the end of a doubly terminated $75-\Omega$ line.

## Identical Devices

The two devices are identical (the same chip) except that the 7121 lacks the SYNC and BLANK inputs due to its 40-pin double-width DIP package (the 7122 is in a 44-pin PLCC). In addition to the three speed-versions and two packages types, there are two performance grades. Integral and differential nonlinearity (INL and DNL) of the J-grade device run $\pm 3$ and -1 LSB maximum, respectively, over the temperature range of 0 to
$70^{\circ} \mathrm{C}$. Under similar conditions, INL and DNL of the K-grade units run $\pm 2$ and $\pm 1$ LSB, respectively. All are guaranteed to be monotonic over temperature.

The availability of three speed versions permit system designers to choose the most economical device as a function of CRT resolution. For example, at a refresh rate of 60 Hz , the $80-\mathrm{MHz}$ converters are required for the latest 1024-by-1024-pixel CRT displays. Maximum current consumption from a 5 -V power-supply rail for these CMOS chips is just 125 mA for the $80-\mathrm{MHz}$ units and 100 mA for the others.

In quantities of 1000 , pricing ranges from $\$ 18.35$ each for the 30 MHz , J-grade ADV7121 to $\$ 35.30$ each for the $80-\mathrm{MHz}$, K-grade ADV7122. Small quantities are in stock.

Analog Devices Inc., 804 Woburn St., Wilmington, MA 01887; Chris Hyde, (617) 937-1422 CIRCLE 301

# Multiplexed Sampling Amplifier DELETES COSTLY DACS 

While the cost of 12 -bit IC d-a converters (DACs) has dropped, if you need a lot of them, total system cost can climb-and they not only take space, but the input digital lines to them do as well. Another approach, somewhat analogous to dynamic vs static RAMs, uses a single DAC and multiple sample-and-hold amplifiers which are continuously refreshed. To fill that need, Precision Monolithics has announced the SMP08 . It has eight, voltage-output, sam-ple-and-hold amplifiers any one of which can have its held voltage uniquely updated, at any time, from a single DAC. A 3-bit input word selects the channel. An update to 8-bit accuracy for 0 and 10 V typically takes $1 \mu \mathrm{~s}$. Droop rate is $0.25 \mathrm{mV} / \mathrm{ms}$. And that's with on-chip capacitors. Absolute accuracy is 8 -bits, linearity 12 -bits. Unit price in lots of 100 runs $\$ 6.25$.

Precision Monolithics Inc. P.O. Box

58020, Santa Clara, CA 95052-8020; Walt Heinzer (408) 562-7254. GTIGTF 302
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## SAMPLE T0 16-BIT ACCURACY IN 250 NS

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Sipex Corp. 6 Fortune Dr., Billerica,
MA 01821; Jack Worthen (508) 663-
9691. CTRGIF 303

## Shunt Reference In T0-92 SINKS 100 MA

An adjustable shunt-type linear reference/regulator, the LT1431, comes in a 3 -pin TO-92 as well as 8 -pin DIPs and SOICs. It contains a 2.5 -V band-gap reference, its output transistor sinks 100 mA , and, with just a single external resistor, can be connected to deliver 2.5 or 5 V out with $1 \%$ accuracy. Two resistors

set the output voltage between 2.5 and 36 V . It can also provide the reference and isolated negative feedback in a $5-\mathrm{V}$ switching regulator by connecting a resistor to the regulator's output and driving the LED in an opto-isolator with the IC's open-collector npn. The LT1431 (TO-92) goes for just $\$ 0.92$ each in hundreds.

Linear Technology Corp., 1630 McCar-
thy Blvd., Milpitas, CA 95035-7487;
Bob Scott, (408) 432-1900. GITGIF 304

## Want to see a precision narrowband sweep that usually takes about a minute?



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This analyzer offers unprecedented speed in two measurement modes. In the swept mode, you get a 10 Hz to 150 MHz range, RBW as narrow as 1.1 Hz and measurements up to 16 times
faster than previously available. The narrowband-zoom mode gives you a span of 40 kHz or less anywhere in the 150 MHz range, RBW to 0.0045 Hz and measurements up to 400 times faster than traditional swept analyzers.

So, call 1-800-752-0900 today. Ask for Ext. 1212, and we'll send a videotape demo so you can see these fast measurements for yourself. But don't blink.


There is a better way.

## IC Evaluation System Features 400-MHz VECTOR RATE, 512 PINS



The latest member of the HP 82000 family of IC evaluation systems, the Model D400, boasts a $400-\mathrm{MHz}$ maximum vector rate that lets engineers verify their designs and characterize prototype ICs and ASICs at the devices' full performance limits. In the past, designers had to use formulas to make assumptions about device behavior at full speed.
The system accuracy is an excellent $\pm 200 \mathrm{ps}$. Maximum pin capacity is 512 pins. Memory capacity of up to 1 Mvec-
tor is available behind each I/O pin. A tester-per-pin architecture permits independent per-pin timing and voltage levels.

The HP 82000 series features a modular design, so users can start with a basic configuration and increase pin count and vector rate as the need arises. HP can supply a variety of links to all commonly used electronic design automation systems. New highthroughput software is available to make the tester suitable for smallbatch production testing.
The HP 82000 Model D400 costs about $\$ 3400$ per I/O channel, depending on the number of channels and the system configuration. Delivery is estimated at 12 weeks.

Hewlett-Packard Co. Inquiries,
19310 Pruneridge Ave., Cupertino, CA 95014; (800) 752-0900.

## CIIGIF 305

- JOHN NOVELLINO


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of SMD, DIP and pin grid components and connectors in a matter of seconds with the Leister-Labor " S " hot-air tool. Electronic control of temperature and air supply. Over 400 special nozzles available.


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phone: (201) 938-2700

## E-BEAM PROBER B0ASTS 80-NM PROBE SIZE

A newly designed lanthanum hexaboride high-performance electron source produces an $80-\mathrm{nm}$ probe size for the IDS 5000 Plus integrated diagnostic system. The new source offers a long, reliable cathode life approaching 2000 hours on the electron-beam probing system to ensure full brightness during design debug and verification, failure analysis, and device characterization. The unit features an electron column positioning system that delivers $0.2-\mu \mathrm{m}$ resolution over a die area four times that of other systems, so engineers can probe chips up to 32 mm square. The IDS 5000 Plus costs $\$ 625,000$. Current IDS users can retrofit the IDS 5000 Plus submicron capabilities and other features to their older systems.

Schlumberger Technologies, ATE Div., 1601 Technology Dr., San Jose, CA 95110-1397; (408) 453-0123. GIBCIF 306

## PC/AT ACQUISITION CARD B0ASTS 16-BIT PRECISION



A 16-bit multifunction data acquisition board for the PC/AT and compatibles features 16 single-ended and eight differential analog inputs. The LSDAS-16 includes an autocalibrating analog-todigital converter, a $50-\mathrm{kHz}$ sample rate, two deglitched digital-to-analog converters with optional buffer memory, a digital I/O port, and timers. An optional 32 -ksample buffer memory generates waveforms independently of the host. The board comes with a full-function setup program and data acquisition utilities. Other software support available includes libraries to help in program development and a high-level language interface for C, Pascal, QuickBasic, and Fortran. Available from stock, the LSDAS-16 lists for $\$ 1395$. Volume discounts are available. The optional memory costs $\$ 200$.

[^7]
# i486-BASED COMPUTERS INCORPORATE Micro Channel Architecture 

Afamily of workstations and servers, from NCR Corp., combine the Micro Channel bus with an i486 microprocessor to achieve 27 MIPS. The first product, a $33-\mathrm{MHz}$ system, is intended for compute-intensive applications including CAD, graphics, simulation, and networking. The PC486/MC ${ }_{33}$ boasts Super VGA graphics using a chipset integrated onto the main processor board.

NCR's Micro Channel chipset includes a processor-interface controller, a dual-port memory controller, memo-ry-error detection and correction, and direct memory access. The chipset also lets users upgrade BIOS through software without changing any hardware. The computer also achieves zero-waitstate performance for memory read and write operations using intelligent bus masters.
The base system, which comes with 4

Mbytes of RAM and a 1.44-Mbyte, 3.5in. floppy disk drive is priced at $\$ 14,195$. It will be available in July.

A second system, the $\mathrm{S} 486 / \mathrm{MC}_{33}$, is a deskside computer that functions as a high-performance network or database server for multiple users. This system contains the same graphics abilities as the PC486/MC ${ }_{33}$. An addition to the S486/MC ${ }_{33}$ is a 53 C 700 SCSI controller that increases peripheral support by decreasing system access time, resulting in faster throughput.
The system can hold a 1.26 -Gbyte SCSI hard-disk drive and contains nine drive bays-six half height and three full height. It also has seven Micro Channel expansion slots, four memory slots, and a SCSI I/O slot. Available in Jüly, base models start at \$16,195.

NCR Corp., Workstation Products Div., 1601 South Main St., Dayton,

OH 45479; (513) 445-7443. Gliblis 308

- RICHARD NASS


## MACINTOSH MOUSE, SCANNER EMPLOY OPTICAL POSITIONING SYSTEM

Two products from Mouse Systems Corp., designed for use on the Macintosh computer, incorporate optical technology for improved accuracy. The Little Mouse offers a $50 \%$ higher resolution over Apple mouse alternatives. In addition, it's $22 \%$ smaller and $38 \%$ lighter than the standard Apple mouse. Its optical positioning system contains no moving parts so it requires no cleaning or adjustment. Available now, the Little Mouse costs $\$ 129.95$.
The second product, the PageBrush full-page scanner, can also double as an optical mouse and digitizer. The scanner, which looks like a typical mouse, lets the user "paint in" full-page hardcopy text and images to a host computer. The size of the scanned image is limited only by the host computer's memory. PageBrush sells for \$795.95.

Mouse Systems Corp., 47505 Seabridge Dr., Fremont, CA 94538; (415) 6561117. CHIETF 309

# Small Company's New Golf Ball Flies Too Far; Could Obsolete Many Golf Courses 

Pro Hits 400-Yard Tee Shots During Test Round<br>Want To Shoot An Eagle or Two?

By Mike Henson
MERIDEN, CT - A small golf company in Connecticut has created a new, super ball that flies like a U-2, putts with the steady roll of a cue ball and bites the green on approach shots like a dropped cat. But don't look for it on weekend TV. Long-hitting pros could make a joke out of some of golf's finest courses with it. One pro who tested the ball drove it 400 yards, reaching the green on all but the longest par-fours. Scientific tests by an independent lab using a hitting machine prove the ball out-distances major brands dramatically.

The ball's extraordinary distance comes partly from a revolutionary new dimple design that keeps the ball aloft longer. But there's also a secret change in the core that makes it rise faster off the clubhead. Another change reduces air drag. The result is a ball that gains altitude quickly, then sails like a glider. None of the changes is noticeable in the ball itself.

Despite this extraordinary performance the company has a problem. A spokesman put it this way: "In golf you need endorsements and TV publicity. This is what gets you in the pro shops and stores where $95 \%$ of all golf products are sold. Unless the pros use your ball on TV, you're virtually locked out of these outlets.

TV advertising is too expensive to buy on your own, at least for us.
"Now, you've seen how far this ball can fly. Can you imagine a pro using it on TV and eagle-ing par-fours? It would turn the course into a par-three, and real men don't play par-three's. This new fly-power forces us to sell it without relying on pros or pro-shops. One way is to sell it direct from our plant. That way we can keep the name printed on the ball a secret that only a buyer would know. There's more to golf than tournaments, you know."

The company guarantees a golfer a prompt refund if the new ball doesn't cut five to ten strokes off his or her average score. Simply return the balls - new or used to the address below. "No one else would dare do that," boasted the company's director.

If you would like an eagle or two, here's your best chance yet. Write your name and address and "Code Name S" (the ball's R\&D name) on a piece of paper and send it along with a check (or your credit card number and expiration date) to National Golf Center (Dept. H-1448), 500 S. Broad St., Meriden, CT 06450 . Or phone 203-2382712, 8-8 Eastern time. No P.O. boxes, all shipments are UPS. One dozen " S " balls cost $\$ 24.95$ (plus $\$ 2.50$ shipping \& handling), two to five dozen are only $\$ 22.00$ each, six dozen are only $\$ 109.00$. You save $\$ 55.70$ ordering six. Shipping is free on two or more dozen. Specify white or Hi-Vision yellow.

## ARRAY-PROCESSOR B0ARD COMBINES i860, 1960 RISC CHIPS

Aboard-level array processor, the Warrior III, from Sky Computers Inc., combines the Intel i860 and i960 RISC processors to achieve a processing speed of 80 MFLOPS. A prevectorized software li-
brary optimizes the 64 -bit i860, which performs all arithmetic operations. The i 960 chip, acting as a DMA engine, handles system I/O, memory transfers, diagnostics, and other housekeeping functions. It can fetch data from anywhere in the VME host and is responsi-


Australia (02) 654 1873, Austria (0222) 3876 38, Benelux +31 1858-16133, Canada (514) 689-5889, Denmark (02) 658111 , Finland 90-452 1255, France (01)-69 412 801, Great Britain 0962-73 31 40, Israel (03) 4848 32, Italy (011) 7710010 , Korea (02) 784784 1, New Zealand (09) 392-464, Portugal (01) 8356 70, Sweden, Norway (040) 922425, Singapore (065) 284-6077, Spain (93) 217 2340, Switzerland (01) 74041 05, Taiwan (02) 7640215, Thailand (02) 281-9596, West Germany 08131-1687, USA FAX (408) 378-7869
ble for prefetching and caching the data. Thus feature minimizes the need for dedicated memory for the array processor.

Because of the extensive software library that exists for the Warrior III, users can easily develop custom applications in C or Fortran. There's no need to resort to complex assembly code or microcode. Users can access and manipulate data in rows, columns, or any pattern in a multidimensional array stored in memory.

Multiple Warrior III boards, operating in parallel, can be tied together without any I/O degradation. And the board uses just 37 W of power with a full complement of memory-nearly $50 \%$ less than typical array-processing boards.

Operating systems supported include Unix, SunOS, VxWorks, OS-9, and Concurrent RTU. It's available in either 6 or 9 U sizes and conforms to all Sun and VME mechanical requirements. External interface options include SCSI, 32 -bit parallel, and custom daughtercard. The Warrior III is priced at $\$ 8225$ in OEM quantities and is available in 60 days.

Sky Computers Inc., 27 Industrial Ave., Chelmsford, MA 01824; (508) 250-1920. GIBGIF 310

RICHARD NASS

## 4096 PROCESSORS FILL ONE B0ARD

Using just one 32-bit adapter slot, the Coherent Processor board gives an IBM Micro Channel workstation the power of 4096 parallel processors. The board possesses 16 processing elements, each of which contains 256 parallel processors. Content-addressable memory is used to search and operate on an entire table of data in parallel. The board is aided by a Development System that offers hardware and software support for writing, debugging, and running parallel application programs in C language. A compiler lets users create custom design routines. Typical applications are for speeding up databases, neural networks, or expert systems, or to work in a real-time environment such as local-area networks, radar, or process control. The Coherent Processor is available now for $\$ 19,500$. In addition, a Sun-compatible board will be released later this year.

Coherent Research Inc., 1 Adler Dr.,
East Syracuse, NY 13057; (315) 433-
1010. GIRGIF 311

## TELECOM DC/DC CONVERTERS

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## S0FTWARE ENvIRONMENT MAXIMIZES WIND0WS 3.0

In conjunction with the recent Microsoft Windows 3.0 release, Hew-lett-Packard Co. announced version 3.0 of their NewWave software applications environment. NewWave, which runs on any 80286- or 80386-
based PC running MS-DOS, integrates applications from many different software vendors. The list of independent software vendors porting their software to NewWave is an ever-growing one and now stands at more than 100.

NewWave offers a single, consistent


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CIRCLE 114
user environment with icons to simplify use. Users aren't forced to learn the workings of DOS or how to manage different files and programs. Version 3.0 of NewWave also includes an objectstorage feature, which lets users share information on a network server by simply moving icons on the screen.
The user environment takes full advantage of all the new features added to Windows 3.0. These features include improvements to the memory management which lets NewWave run with 2 Mbytes of memory rather than 3 Mbytes. Windows also maximizes of the protected mode of 80286 and 80386 microprocessors to supply added memory for both the environment and the applications running on it. The MSDOS Executive in the existing Windows programs are replaced with a Program Manager, a File Manager, and a Task List to supply a visual shell for completing directory, application, and file-management tasks. Color and design enhancements add to the polished user interface.

HP's NewWave will be available in August for $\$ 195$. Present users of NewWave can upgrade for $\$ 50$. Windows 3.0 is available now for $\$ 150$.

Hewlett-Packard Co., 19310 Pruner-
idge Ave., Cupertino, CA 95014; (800) 752-0900. GIBEIF 312

Microsoft Corp., One Microsoft Way, Redmond, WA 98052; (800) 323-3577. GITEIF313
RICHARD NASS

## ANALYZE SOFTWARE <br> FOR 8-T0 32-BIT CPUS

Three software-analysis products aim to meet price and speed requirements of developers working on 8 -, 16 -, and 32 bit microprocessor systems. The tools are based on the architecture of the company's Software Analysis Workstation (SAW), and consist of the SFA1000 for performance analysis, the SAW2000 for software debug and performance analysis on 8 - and 16 -bit microprocessors, and the SAW3000 for 32 -bit processors. All tools are language independent. Also new is TaskView, an Ada debug and analysis tool that supplies a run-time view of an entire multitasking embedded system. The SFA1000, SAW2000, SAW 3000 , and TaskView cost $\$ 10,500, \$ 15,850$, $\$ 19,500$ and $\$ 4500$, respectively. All the tools are available now.
Cadre Technologies Inc., Portland Div., P.O. Box 1309, Beaverton, OR 97075; (800) 547-4445. GIRGIF 338

# National's family of CMOS op amps rises to a new all-time low: 40 femtoamps. 

## TAKING IT TO THE LIMITS WITH ULTRA-LOW INPUT BIAS CURRENT.

National's new quad/dual CMOS op amps, the LMC660/662 and the LPC660/662, feature an extremely low input bias current of 40 fa typical. You can't go much lower.

Featuring rail-TO-RAIL OUTPUT SWING.

With a newly patented double feed-forward circuit architecture, National's op amps provide an output swing that extends from one supply rail to the other. You can't swing any more than that.

Use the LMC660/662 and LPC660/662 to drive rail-to-rail input A/Ds, or take advantage of the LMC's fully specified $600 \Omega$ load capability to process audio in telecom and cellular radio applications. Other typical applications include:

- Handheld meters
- Medical instrumentation
- Remote sensors
- Electrometers
- Spaceborne/Avionic subsystems


Photooliode current-To-voltage converter


INPUT BIAS CURRENT VS. TEMPERATURE: 40 tA AT $25^{\circ} \mathrm{C}$

## NATIONAL <br> REDEFINES SINGLE-SUPPLY OPERATION.

In the past, a single-supply op amp was an amplifier whose input common-mode range included ground. But in today's +5 V systems, you need op amps that take advantage of every last volt that the supply provides, and whose outputs swing fully from rail-to-rail. National was the first to deliver rail-to-rail performance with the LMC660 and now has a complete family- all in CMOS.

## POWER UP WITH LOW POWER AND MICROPOWER.

If you're looking for low power, there's the LMC660/ 662 , which operate at $375 \mu \mathrm{~A} /$ amplifier. Or if your application calls for $40 \mu \mathrm{~A} / \mathrm{amplifier}$, we offer the LPC660/662, micropower versions of the popular LMC series. In either case, you get lower power dissipation and a longer lasting battery.

LMC660/PC660 VS. THE COMPETTIION

|  | LMC660AI | LPC660AI | TLC274AI |
| :--- | :---: | :---: | :---: |
| Output Swing <br> $\left.\mathbf{N}^{+}=+\mathbf{5 V}\right)$ | $\mathbf{0 . 1 5 V}$ to 4.82V | $\mathbf{0 . 0 3 V}$ to 4.97 V | $\mathbf{0 . 0 5 V}$ to 3.2 V |
| $\mathrm{~V}_{\text {OS }}$ (max) | 3 mV | 3 mV | 5 mV |
| $\mathrm{I}_{\mathrm{b}}$ (typ) | 40 fA | 40 fA | 600 fA |
| Supply Current <br> (typ) | $375 \mu \mathrm{~A} / \mathrm{amp}$ | $40 \mu \mathrm{~A} / \mathrm{amp}$ | $675 \mu \mathrm{~A} / \mathrm{amp}$ |

## GET THE LOWDOWN.

For more information on our new CMOS op amps and growing family of high-performance amplifiers, including VIP, ${ }^{m i}$ Bi-FET, ${ }^{\text {m }}$ SuperBlocks,' ${ }^{\text {m }}$ and precision, call or write us today: 1-800-624-9613, Ext. 66. In Canada: 1-800-548-4529, Ext. 66. National Semiconductor Corporation, P.O. Box 7643, Mt. Prospect, IL 60056-7643. And find out how we can help take your designs to new heights.

## Pass Data at 25 MHz With Bidirectional FIF0

Rather than use two memory blocks on the same chip to form a 2-kword-by-9-bit bidirectional first-in/first-out memory, the CY7C439 employs a lone 2-k-by-9 memory block and some on-chip control logic to move
data. Furthermore, Cypress Semiconductor's designers add two other data paths into the chip-a registered bypass mode and a transparent bypass mode.
The registered mode acts like a 1 -word-deep FIFO register in the reverse

## 4-MEGABIT SRAMs



If you thought we were crowding a lot of memory into a small space before, look again. Now we've packed 4-Megabit ( 512 Kx 8 ) of CMOS SRAM memory into a single 32-pin Dip. They offer read access and write cycle times from $45 n \mathrm{nec}$ to 120 nSec , and three temperature ranges. Screening per MIL-STD-883C is an available option.
These new high-density memories will cut your design time, save you board space, and conserve power, too. They're housed in a rugged $1.6^{\prime \prime} \times 0.6^{\prime \prime}$ ceramic package with JEDEC standard pinouts. A welded metal cover and co-fired construction assures maximum integrity and hermetic seal, and lends itself to the most demanding low power battery-backed commercial, industrial, and military applications.

Other Key Specifications Include:

- 37 mA Typical Operating Current
- Data Retention With Voltages As Low As 2.0 Volts
- 10uA Typical Data Retention Current at $25^{\circ} \mathrm{C}$.
- Temperature Ranges:
$0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$
$-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$
$-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$
But, if 4-Megabit isn't enough, we have a new 8-Megabit Flash PROM in a 34 -pin package available now, and a 2 " $\times 2$ " 64 Megabit flat-pack in test. And there's more. We're designing memory systems in the gigabit and even terabit regions. If you're looking for a complex single-package system, a supercomputer array, or a totally defined multi-package management information system, give us a call. Your design or ours, we'll make it happen.

CIRCLE 80
direction to the main FIFO buffer. It permits the sending system to transfer a 9-bit status word to the FIFO buffer's write port. The transparent bypass feature allows a single 9-bit word to be immediately transferred in either direction, temporarily turning the chip into a 9 -bit bidirectional buffer. With these modes, the chip can serve in applications such as a disk-drive buffer in which the transparent mode allows the host to configure a 'dumb' peripheral while the registered bypass mode holds the status response from a data transfer.

Able to access in just 30 ns and operate with a $25-\mathrm{MHz}$ cycle frequency, the bidrectional FIFO register's transfer direction can be selected on a cycle-bycycle basis. Indicator flag signals are available for conditions such as Empty/Full, and Half-Full.

Since only one memory block is required, the chip is small enough to squeeze into a 300 -mil-wide DIP or small-outline J-leaded package. In 100unit quantities the chip sells for $\$ 33.15$. Samples are available from stock.

Cypress Semiconductor Corp., 3901
N. First Street, San Jose, CA 95134; Bill Eichen (408) 9432600 GIBGIF 314

DAVE BURSKY

## WIDE-INPUT PLDS DECODE ADDRESSES FAST

Designed specifically for address decoding, a very-wide-input decoder packs 36 input lines, 10 dedicated output lines and 12 additional programmable I/O lines. Fabricated in an advanced bipolar process the PHD48N227 can decode up to a 48 -bit bus pattern (by using the $12 \mathrm{I} / \mathrm{O}$ lines as additional inputs) in just 7.5 ns from input to output (through the AND logic), making the chip the fastest wide decoder available from any company. Four of the 12 bidirectional I/O lines also serve as OR logic outputs, and three of those four provide 7 product terms; the fourth line has 12 product terms. These OR lines are especially helpful in dealing with microprocessor Wait and Interrupt signal lines and they have a slightly longer propagation delay-8 ns. The wide decoder is available in production quantities, and the plastic-housed leaded-chipcarrier version sells for $\$ 22$ in 1000 -unit lots.

Philips-Signetics Corp., 811 E. Arques Ave., P.O. Box 3409, Sunnyvale, CA 94088; Paul Sasaki, (408) 9912000. GTIGIF 315

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CIRCLE 112
FOR IMMEDIATE APPLICATION

## 9600-BIT/S M0DULE EASES MODEM DESIGN



Offering full-duplex operation at 9600 bits/s, the CH1790 modem module provides full V. 32 compatiblity. It has fallback and compatibility with 4800 -, 2400 , 1200-, 300- and 110-bit/s rates and meets CCITT V.32, V. 22 bis, V.22, V.21, and Bell 212A and 103 standards. Able to respond to the full Hayes "AT" command set, the modem can be controlled by a wide variety of available data-communication packages. Features include automatic answer, automatic speed and partiy adjustment, and call-pro-
gress tone detection. Trellis forward error correction is used at $9600 \mathrm{bits} / \mathrm{s}$ along with MNP Level 4 error control. A built-in RS-232 $(5-\mathrm{V})$ serial interface allows the host to communicate with the module. An evaluation test system that contains the modem, DAA and other hardware to run the module through its paces is also available-the CSP9696A. In small quantities, a fullfeatured V. 32 modem, sells for less than $\$ 500$.

Cermetek Microelectronics Inc., 1308
Borregas Ave., Sunnyvale, CA 940883565; Thomas Newton, (408) 752 5000. CHIGEF31G

## Fax M0DEM CHIP TARGETS PORTABLE APPLICATIONS <br> Features added to the YM7109 fax mo-

 dem IC qualifies the device for portable and remote applications. The new chip, the YM7109E, combines the capabilities of the earlier version with error correction for Group 3 fax, HDLC framing including bit stuffing, bit stripping, and CRC calculations, aUART for Bell 103 transmission, and an external clock synchronous mode for cellular phone and remote fax applications using radio transmission or satellite communications. Also on the chip are serial and parallel ports, a scrambler and descrambler, a programmable touch-tone generator and detector, and a programmable tone-detector for nonDTMF tones.

On-chip data converters have a 9.6 K samples/s sampling rate with a 12 bit resolution for voice recording and playback. The chip complies with standard half-duplex synchronous CCITT V. 29 at $9600 / 7200 \mathrm{bps}$ and V. 27 ter at $4800 / 2400 \mathrm{bps}$; synchronous CCITT V. 21 half- and full-duplex at 300 bps ; and full-duplex asynchronous Bell 103. The CMOS chip comes in a 40 -pin DIP, a 64 -pin quad flatpack, or a 68 -pin PLCC. Pricing is $\$ 35$ each in quantities of 10,000 . Samples are available now, and production quantities are coming in November.

Yamaha Corp. of America, 981 Ridder Park Dr., San Jose, CA 95131; Robert Starr, (408) 437-3133. साiG1F317

# CUT FREQUENCY HIGHS DOWN TO SIZE Micro/Q $\mathbf{3 0 0 0}$ Controls High Frequency Noise From ASICs 

Design PGA packaged ASICS or MPUs into your board design and the noise level starts climbing. Surround these PGAs with standard 2 pin decoupling capacitors, and you'll use valuable board space and provide inferior decoupling.
Micro/Q 3000 decoupling capacitors from Rogers provide excellent noise suppression over a wide frequency range. For space savings, they're specifically designed to fit under PGA devices such as fully custom


Micro/Q 3000 capacitors fit under PGA packaged ASICs and MPUs.
decoupling capacitors is through-hole mounted under pin grid arrays, PGA sockets, and PLCCs/LCCs mounted in sockets. They are available for all PGAs in a variety of sizes and dielectrics, including X7R and P3J dielectrics for greater temperature stability.
Micro/Q 3000 capacitors. Excellent noise suppression for high performance.
Write or call for free literature and product samples.

ASICs, MPUs and gate arrays - where low noise and high density are essential.
Featuring the high performance reliability you've come to expect from Rogers, this family of very low inductance

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## NEW PRODUCTS

## CONTROLLERS B00ST SERIAL

 COMmunications PerformanceTwo CMOS serial communications controllers from Zilog Corp. simplify system design by integrating functions previously performed by discrete devices.
The Z85130 enhanced serial communications controller (ESCC) is a dualchannel, full-duplex multiprotocol controller with each channel containing a crystal oscillator, baud-rate generator, and digital phase-locked loop. The ESCC also includes an 8-byte-deep receive FIFO buffer and a 4 -byte-deep transmit FIFO buffer for reducing data overruns, interrupts, and host CPU overhead by accumulating byte strings. The programmable FIFO and DMA request levels allow the user to select packet-handling response. SDLC protocol enhancements offload the CPU with automatic handling of frame conditions.
The Z 85 C 80 serial communications and small computer interface (SCSCI) combines Zilog's Z85C30 10-MHz serial
communications controller (SCC) and the 3-Mbyte/s Z53C80 small computer system interface (SCSI). Both functions share an 8-bit address and data bus for use in any system having a SCSI interface defined by the X3.1311986 standard. The SCSCI has all features required to build a network using a typical disk-based file server, including an interface to multiplexed or nonmultiplexed CPUs, programmable channels for asynchronous or synchronous datacom protocol, and a 10-by-19bit FIFO buffer and 14-bit byte counter that support high-speed SDLC transfers using DMA controllers.
Packaged in a 40 -pin DIP and 44 -pin PLCC, the Z85130 $16-\mathrm{MHz}$ version costs $\$ 13.65$ in 1000 -piece quantities. The $10-\mathrm{MHz}$ part costs $\$ 8.85$. Packaged in a 68 -pin PLCC, the Z 85 C 80 costs $\$ 12.43$ each in 1000 -piece quantities.

Zilog Corp., 210 Hacienda Ave., Campbell, CA 95008; Mike Hulme, (408) $370-8000$. CIITEIF 339

- MILT LEONARD


## 9600-BPS V. 22 BIS-C0MPATIBLE Modem Trims Price, Not Features

Able to operate at $9600 \mathrm{bits} / \mathrm{s}$ in a full-duplex mode, the 9624 modem series employs a custom chip set developed by Sharp to achieve CCITT V. 22 bis compatibility. The custom chips allow the company to incorporate MNP5 error correction as well as the company's own extended-

baud-rate technology, which, together, permit a 2400 -bit/s chip set to provide 9600 -bit/s full-duplex asynchronous operation, as well as standard 2400 -, $1200-$, and $300-\mathrm{bit} / \mathrm{s}$ data modes. (To achieve the $9600-\mathrm{bits} / \mathrm{s}$ rate, a pair of
units, one on each end, must be used.)
The modems achieve a throughput equivalent to or better than that specificed by the V. 42 bis standard. Two versions of the modem are available: the 9624 , a $3 / 4$-size card that plugs into the PC bus, and the 9624 e , an external unit that connects to any system's serial port.
Both models include a speaker and comply with the standard Hayes (AT) command set. Single-unit prices for the modems are $\$ 299$ for the card version and $\$ 399$ for the external unit.

Sharp Digital Information Products
Inc., 16841 Armstrong Ave., Irvine, CA 92714; Greg Peel, (714) 2616224. GIIGIF 340

DAVE BURSKY

## BOARDS PUT MACINTOSH ON ARCNET LANS

A line of board-level products enables Macintosh SE and Macintosh II computers to join an ARCNET local area network, the environment typically used for networking IBM PCs and compatibles. The Macintosh-on-ARCNET
family allows the use of PC-type file servers and printers, eliminates the need for a dedicated Macintosh server, and enables Macs to share data among themselves without additional networking accommodations or cable. Furthermore, networks can employ coaxial cabling, twisted-pair wiring, or a mix of the two in star, bus, or daisychain topologies. Hardware consists of a controller board and a transceiver board for the MAC SE, while the MAC II requires only one board. To accommodate the various topologies and cabling systems, four versions are available. For the MAC SE, the SE100 supports the coax star topology and the SE250 handles twisted-pair star and daisy-chain topologies. For the Macintosh II, the NB210 supports coax star and bus topologies, while the NB250 is for twisted-pair star and daisy-chain topologies. The SE100 and SE250 sell for $\$ 495$ each; the NB210 and NB250 cost $\$ 545$ each.

Standard Microsystems Corp., 35 Marcus Blvd., Hauppauge, NY 11788; (516) 273-3100. GITHF 341

## daA MODULE Tackles HIGH-SPEED M0DEMS



Designed specifically to improve the performance of high-speed modems, the CH1832 data access arrangement mates directly to V. 32 , V. 33 and V. 29 type modems. The DAA passes voice and data at speeds starting at 300 bps and up to 38.4 kbps . High-voltage isolation and surge protection up to 1000 V are built into the DAA. System features include ringing detection, hookswitch control, billing delay, and provisions for 2-wire or 4 -wire leased-line operation. A 2 -wire-to-4-wire converter is included in the 2.2 -by- 3.25 -by- 0.65 -in. module. The DAA module is also preregistered for FCC part 68, thus reducing the waiting time needed by a system that must obtain part 68 approval.

Cermetek Microelectronics Inc., 1308 Borregas Ave., Sunnyvale, CA 940883565; Thomas Newton, (108) 752 5000. GIIGIF 342

## IEED-488


device with our cards, cables, and software for the PC/AT/386, EISA, MicroChannel, and NuBus.

## REVAMPED SUSIE Simulator Runs 30 Times Faster

The newest version of the popular Susie logic simulator from Aldec Co. is not only up to 30 times faster than the previous version, but also supports VHDL IC models and easy-to-use windowing. Susie 6.0 achieves the speed gain with a new event-driven algorithm and by taking advantage of 32 -bit direct addressing on 80386 - and 80486 -based computers. In addition, the simulator runs from mouse-driven pop-up menus.
Version 6.0 gives users the same real-time operation they are used to, but adds high-speed simulation of VHDL IC models. Users can toggle switches, move jumpers, change propagation delays of any IC, modify Jedec and hex files, and then instantly simulate the new design without visible compilation. Users can also perform instant simulation of selected design areas, which can speed the simulation process by 10 to 100 times.
Also, Aldec's VHDL IC timing model builder, Mobic/T, is a high-level modeling language designed specifically for Susie. It generates IC timing models with 11 input states and 15 output states, and includes predefined functions for modeling memories and PLDs. Susie 6.0 comes with TTL VHDL libraries. There are over 6000 parts available in Aldec's optional libraries.
Susie 6.0 is available now for $\$ 5995$. The Mobic/T IC-model builder is $\$ 1995$, and the optional libraries start at $\$ 795$.

Aldec Inc., 3525 Old Conejo Rd.,
Suite 111, Newbury Park, CA 91320
(805) 499-6867. CHIVGIF31B

- LISA GUNN


## MICR0WAVE EDA T00LS Span Design Cycle

The Cadence Microwave Musician design tools carry engineers from schematic capture through physical layout in one integrated package. The system offers front-to-back design capability for both monolithic microwave ICs and hybrid devices. Users can produce hierarchical schematics using a library of ideal components and a library of foundry components. In addition, the package supports multiple simulation runs at the same time. The Musician front end, which consists of schematic


You get fast hardware and software support for all the popular languages. A software library and time saving utilities are included that make instrument control easier than ever before. Ask about our no risk guarantee.
capture and a microwave component library and interfaces to most of the popular microwave simulators, costs $\$ 15,000$. The complete system, which includes the front end as well as synthesis, layout, and design verification, costs $\$ 30,000$.

Cadence Design Systems Inc., 555 River Oaks Pkwy., San Jose, CA 95134; (408) 943-1234. GITGIF31P

## SCHEMATIC-CAPTURE COSTS LESS THAN $\$ 100$

Engineers can have a schematic-capture system for less than $\$ 100$ with Omation Inc.'s Schema-Quik software, a low-cost version of the company's Schema III software. The package is aimed at PLD manufacturers as an alternative to data entry with logic equations, truth tables, or state machines. Drawings created in Schema-Quik are
transferred through a system manager to the manufacturer's design and compilation software. Each system is tailored to the needs of the manufacturer by controlling libraries, hierarchies, drawing sizes, and output forms. The Schema-Quik package includes software, reference manual, and tutorial, and is upgradable to the Schema III package. The product is shipping now for $\$ 99$.

Omation Inc., 801 Presidential Dr., Richardson, TX 75081; (800) 5539119. GIGGIF 320

## FRONT-END AUTOMATES FILTER DESIGN

Filter Designer is an interactive frontend tool that lets engineers design and analyze active filters, using such features as a menu-driven interface, hardcopy report summaries and plots, concatenation of multiple designs, and interfaces to PSpice. Available filter types include low-pass, high-pass, band-pass, and band-reject, all of which may be synthesized by Butterworth, Chebyshev, inverse Chebyshev, and elliptic functions. With the tool's editor, engineers can insert, delete, and reorder stages, and can modify coefficient values. Pricing for the Filter Designer, which is shipping now, ranges from $\$ 600$ to $\$ 900$ depending on configuration. A Filter Designer evaluation package is available for $\$ 35$.

MicroSim Corp., 20 Fairbanks, Irvine, CA 92718; (800) 245-3022 or (714) 7703022. GIRGIF 321


CIRCLE 90


# Is Your PC Really Up to Speed? 

You may think your PC is already up to speed, but what if it could run even faster? The fact is, with the Intel Math CoProcessor, your software can run up to $500 \%$ faster.

And speaking of fast, installation is fast - and easy - because compatible PCs already have a socket for an Intel Math CoProcessor. And with Intel Math CoProcessors for PCs, ATs and $386^{\text {™ }}$ microprocessor-based systems in stock, Hamilton/Avnet can deliver in virtually no time.

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So don't waste another nanosecond. Get your system up to speed by calling Hamilton/Avnet, toll free, 1 (800) 442-6458.
*386 is a trademark of Intel Corp.


## RUGGED ON-LINE UPS SYSTEM Can Handle Broad Input

Aimed at military and hostile industrial applications is an online ruggedized UPS from Transistor Devices Inc. The MIL-UPS combines the company's BCE battery charger/power supply with its ACE sine-wave inverter.
The BCE module's wide input range of 90 to 250 V from 40 to 440 Hz , as well as its high power factor, provide immunity to ac-input-voltage fluctuations. The system can handle a broad range of line disturbances such as extendedbrownout conditions as low as 83 V , and frequency disturbances from 40 to 440 Hz , without battery power. It's suited for remote site locations where generator fluctuations and low-power-factor loads can be too much of a burden for other UPSs. Thanks to its universal-input feature, the system can function as a frequency changer and voltage conditioner between American, European, and special military power applications.
The charger/supply module also features a battery-equalizer function,
which optimizes battery-cell potentials and extends battery life. To prevent too many repetitive equalizing cycles, the function is automatically locked out at the end of each equalizing cycle. In addition, the BCE module has a reducedvoltage mode that prevents the batteries from heating excessively during a rapid recharge cycle.

From the sine-wave-inverter module, a true sine wave is generated with less than $1 \%$ total harmonic distortion. The module's fixed-frequency output is crystal-controlled to better than $0.1 \%$ stability. The zero-lead-to-zero-lag load power factor of the system's inverter easily drives unfriendly, non-linear power demands such as motors and rectifier loads

A $2-\mathrm{kVA}$ system occupies only 12 in . of height in a $19-\mathrm{in}$. rack. Without batteries, the system weighs under 65 lbs . Such a system goes for about $\$ 10,000$ without batteries.

Transistor Devices Inc., 85 Horsehill Rd., Cedar Knolls, NJ 07927; (201) 267-1900. GIREIF 322

DAVID MALINIAK

## Converter and Filter Tandem NeAr MILSTD-883C ApPR0VAL

With final process certification near, a combination of a de-dc converter and EMI filter will soon pass the last hurdles to full compliance with MIL-STD-883C, method 5008. Interpoint's MHF converter and matching FMC-461 EMI filters give military designers the reliability of components that have passed test conditions applied to mission-critical components.
The 883C versions of the converters and filters have dramatically increased tolerance to temperature extremes and acceleration. That's achieved by using higher switching frequencies to reduce the magnetics' mass and by redesigning the platforms the magnetics are attached to.
Input range for the 883 C -qualified converter is 16 to 40 V dc. It produces closely regulated outputs of $5, \pm 12$, or $\pm 15 \mathrm{~V}$ de in single or dual configurations up to a maximum output of 12 W . The operating temperature is from -55 to $+125^{\circ} \mathrm{C}$. The package is a low-profile ( 0.325 in .) hermetically sealed, gold-

plated steel case that takes up just 1.6 square inches of board area. Power density for the device, which switches constantly at 600 kHz , is 30 W per cubic inch. The matching FMC-461 EMI filter reduces the converter's reflected inputripple current to meet MIL-STD-461B CEO3 standards.

Pricing for the MHF converter is $\$ 780$ in quantities of 100 . In similar quantities, the FMC-461 EMI filter goes for $\$ 365$. Pending qualification testing for the company's process, the MIL-STD-883C-compliant devices will be available this fall.

Interpoint Corp., Box 97005, Redmond, WA 98073-9705; (206) 8823100. GTIGIF 323 DAVID MALINIAK

## CONTROL 400 V AT 1 A WITH 5-V LOGIC

The PWR-NCH201 IC can control solenoids, lamps, relays, and small motors with $5-\mathrm{V}$ logic while powered directly from the rectified $115-\mathrm{V}$ ac line. Packaged in a 16-pin "batwing" DIP, it contains a monolithic pair of MOSFETs rated at 400 V and 675 mA each. Onresistance of each is just $5 \Omega$. Another version, the PWR-NCH401, holds four smaller FETs with a similar voltage rating, but with a current rating and on-resistance of 335 mA and $10 \Omega$, respectively. It is in a 24 -pin skinny DIP. With both FETs in parallel, the 201 handles up to 1 A ; with all four FETs in parallel, the 401 handles up to 675 mA . Unlike other high-voltage MOSFETs, these turn on hard with just 5 V between gate and source, permitting log-ic-level control. The devices are current sensing, or mirror FETs. Each has a separate source output-pin that provides a scaled current equal to approximately $1 / 1500$ of the FET's current. Versions rated at 200 and 400 V are also available. Pricing in hundreds ranges from $\$ 2.60$ to $\$ 5.84$.

Power Integrations Inc., 411 Clyde Ave., Mountain View, CA 94043; Doyle
Slack, (415) 960-3572. CTIGIF 324

## Regulator IC SENSES VOLTAGE AT LOAD

A low-dropout linear regulator, the LT1087, offers both adjustable output voltage and 4 -wire Kelvin sensing of the voltage across the load. The chip is rated at 5 A and regulates down to an input-to-output voltage of just 1.5 V maximum at 5 A . The 4 -wire remote sensing feature eliminates load-regulation errors caused by voltage drops in the hot side of the line to the load and in the ground return. The feature is particularly important where sensitive circuitry, such as wide-band op amps operating at high gain, must be isolated from heat or noise generated by power supplies; in most regulators today the output voltage is sensed inside the package. The chip's reference voltage is trimmed to $1 \%$ and the current limit is trimmed as well. This precision current limit minimizes stress on both the regulator and the power-source circuitry when the circuit is overloaded. The LT1087 comes in 4 -pin TO-3 metal cans and 5 -pin TO-220 packages. In quantities of 100 pricing for the latter runs $\$ 4.45$.

Linear Technology Corp., 1630 McCarthy Blvd., Milpitas, CA 95035-7487; Bob Scott (408) 432-1900. EIIVIFI2

## High-Resolution LCD M0dule Makes Grade For Laptop PCS

Athin plastic film is used in the EG9007 LCD graphics-display panel to achieve a high-contrast black-and-white display that's well suited for notebook- and laptop-PC applications. With its depth of just 0.33 in., the display offers the LCD market's thinnest profile, according to Epson OEM.

Epson's use of its newest formulated twisted-nematic technology in the EG9007 display results in a lighter, thinner module as well as lower manufacturing costs. The single-layer LCD also enabled the company to use edge lighting for the display, which further contributes to its thin profile.

Also featured in the 10 -by- $6.25-\mathrm{in}$., $1.5-\mathrm{lb}$. display is a chip-enable transmission system that significantly reduces power consumption. Thanks to Epson's chip-on-flex technology, the display's
drivers are mounted on a flexible print-ed-circuit board that is lighter and more compact than traditional rigid printedcircuit boards. The display, which weighs a scant 1.5 lbs , produces white characters on a black background with a resolution of 640 by 480 dots and a 1/ 242 multiplex ratio.

The EG9007 display also offers a faster fluid response time ( $120-\mathrm{ms}$ turnon at $25^{\circ} \mathrm{C}$ ) than competitive displays. This translates into faster animation of text and graphic images. A cold-cathode fluorescent backlight provides illumination of the display.

In quantities of 100, the EG9007 display costs $\$ 285$. It is available now in OEM quantities.

Epson OEM Division, Epson America Inc., 3415 Kashiwa St., Torrance, CA 90505; (213) $534-$ 4500. GIIGIF 326

DAVID MALINIAK

## TINY SURGE KILLERS SUIT AUT0 TASKS

A cost-effective and reliable alternative to Zener diodes for transient-voltage suppression in automotive applications has arrived. The V24ML series of semiconducting ceramics come in leadless chip form and are fabricated to absorb internally or externally generated surges that might otherwise damage or destroy a car's electronic components. The surface-mounted devices have no lead inductance and therefore act faster. The series is rated for peak currents up to 2000 A and comes in $1206,1210,2220$, and 2820 sizes. Samples of the V24ML1210 are available now and production lots will be available in August. In lots of 1000, the device costs $\$ 0.46$.

Harris Semiconductor, Box 883, Melbourne, FL 32901; (800) 442-7747.
GIBCIF 327

## 10-IN. COLOR LCD HITS PRODUCTION

Higher resolution, contrast, and brightness than the company's earlier color-TFT LCDs is offered in Hitachi's TM26D01VC $10-\mathrm{in}$. display, which is now in production. The direct-view display offers 640 -by-480-pixel resolution and eight colors. When used with thirdparty gray-scale controllers, the number of colors can increase to 256 . Contrast ratio is $100: 1$ and the display's
brightness level is 80 NT , which meets or exceeds the brightness of CRTs. Response is quick enough for real-time monitoring applications. The display's wide viewing angles suit it to use in medical instruments. Production units are available now with samples priced at $\$ 3500$ each. Initial production pricing is less than $\$ 2000$ per unit.

Hitachi America Ltd., Electron Tube Div., 300 N. Martingale Rd., Suite 600, Schaumburg, IL 60173; Tim Patton, (708) 517-1144. GIRGIF 328

## T0-254 HEATER <br> REGULATES TEMPERATURE

Hermetically sealed in a TO-254 package, the DN-501 is the first in a series of proportionally controlled heaters whose temperature can be programmed between $50^{\circ}$ and $100^{\circ} \mathrm{C}$ by one external resistor. What's more, it can deliver up to 28 W of power from an unregulated supply. The subminiature device, which operates from $-55^{\circ}$ to $+100^{\circ} \mathrm{C}$, can be used for regulating the temperature of sensitive electronic components, such as crystal oscillators and microwave filters. It features $28-\mathrm{V}$ operation and is electrically isolated from the case. The part can also be customized to meet specific application requirements.

Dawn Electronics Inc., 2049 California St., Suite 2, Carson City, NV 89701; (702) 882-7721. GIGGIF 323]

## SLIDE-BASED LED REPLACES BULBS



Slide-based incandescent lamps can be directly replaced with a high-intensity packaged-LED device. The 5 SBF multiLED device uses six discrete chips and boasts a lifetime of 100,000 hours. The incandescent pilot light it replaces, the 120 PSB , lasts only 7500 hours. That suits the LED to tasks with high vibration. The LED device draws 7 mA at 120 V and comes in seven colors with peak wavelengths ranging from 555 to 660 nm . Pricing starts at $\$ 3.56$ for lots of 1000 with availability in six weeks after receipt of order.
Data Display Products, 445 S. Douglas St., El Segundo, CA 90245-4630; (213) 640-0442. GIBGF 330

## 5-IN. C00LING FAN B00STS AIR FLOW

Air flow that's improved by up to $50 \%$ while reducing noise by $50 \%$ compared with $4.7-\mathrm{in}$. fans is featured in the Galaxy 5 -in. fan. The 1.5 -in.-deep unit delivers air-flow levels of 150,125 , and 110 cfm at 12, 24 , and 48 V. Comair Rotron's


ThermaPro-V circuitry provides programmability, voltage regulation, and thermal speed control. Other features include electronic locked-rotor protection with automatic restart. The fan costs from $\$ 18$ to $\$ 20$ in OEM quantities. Samples are available now and production lots will ship in late August.

Comair Rotron, North St., Saugerties,
NY 12477; (914) 246-3615. GIIGFF 331

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## PhYSICAL-VAPOR-DEPOSITION SYSTEM Boasts High Vacuum For Purer Films

An ultra-high vacuum level ( $10^{-9}$ torr base pressure) in the process chamber of Applied Materials' Endura 5500 physical-vapor-deposition (PVD) system is the key to purer aluminum-alloy and barrier-metal films for advanced IC metallizations. Besides higher purity, films produced with the system also exhibit a nine-fold improvement in resistance to aluminum electromigration.
By building on the company's experience in chemical-vapor deposition, the PVD system is designed to give exceptional step coverage and step-coverage symmetry-even in high-aspect-ratio, sub-micron features over wafers up to 200 mm . A down-sputtering source design uses rotating permanent magnets to give complete surface target erosion, with no adjustment needed in process parameters over the life of the target. The result is better uniformity and step-coverage symmetry.
A low-voltage precleaning chamber, which is part of the mainframe unit, conditions each wafer before metal deposition. This yields maximum wafersurface cleanliness with no damage

Then, within the process chambers, careful attention is paid to achieving a very low particulate level. Special antiflake shields greatly reduce particle generation, while a redesigned robotic handling system with external magnetic couplings keeps particulates out of the vacuum chamber.


Base pricing for the Endura 5500 PVD system starts at under $\$ 2$ million. The first system was shipped in April.

Applied Materials, 3050 Bowers Ave., P.O. Box 58039, Santa Clara, CA 95052; (408) 727-5555.

DAVID MALINIAK

## Fiberglass Webs Provide insulation

Craneglas fiberglass webs offer thermal and electrical insulation for a wide range of industrial, commercial, and consumer applications. When laminated with dielectric films and papers, as well as woven fabrics, they offer unique advantages as electrical tapes, wire and cable coatings, gaskets, flame retardants, and thermal-insulation materials. Combining Craneglas with foil results in an excellent heat-shield material. Non-wicking and abrasion-resistant treatments are also available. As a carrier for thermosetting electrical insulating resin systems, Craneglas webs are a low-cost means of insulating motors, generators, transformers, and reactors. They are also a cost-effective alternative as a core material for composite laminates in printed circuit boards. Craneglas is offered in a range of thicknesses from 5 to 120 mils $(0.005$ to 0.120 in .). Call for pricing and availability.

Electrolock Inc., P.O. Box 368, 16838 Park Circle Dr., Chagrin Falls, OH 44022; (216) 543-6626.

## POWER CONNECTOR HAS SECONDARY LOCKS

The Mini-Fit TPA power connector incorporates secondary locks in the form of red-colored keys that are inserted into the housings, ensuring that the terminals within are correctly and permanently sealed. The connector is particularly useful in wire-harness applications, where wires and connectors are often abused during manufacture. The red secondary locking keys cannot be inserted unless the terminals are properly inserted, fully seated, and locked in the housings. An optional lock - a redundant, independent secondary housing lock - is applied after the connectors are mated. The Mini-Fit TPA can handle up to 9 A per circuit, at 250 V depending on circuit size. The centerline between contacts is 0.165 in . and from row to row is 0.217 in . The envelope size of a mated pair of wire-to-wire connectors is 1.36 in . Typical pricing for a 10 -circuit housing is $\$ 0.06$ per mated line (production quantities). Lead time is four to six weeks.

Molex Inc., 2222 Wellington Ct., Lisle, IL 60532; (312) 969-4550.
GITGIF 334

#  

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CIRCLE 291

## A D S



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| A |
| :---: |
| ACCEL Technologies .......................... 140 |
| Advin Systems Inc.............................. 138 |
| Aerospace Optics.................................. 43 |
| AMP...................................... 54-55, 80-81 |
| Ampro Computers, Inc.......................... 22 |
| Analog Devices...........................91, 93, 95 |
| Applied Microsystems....................... 32-33 |
| AT\&T. |

B\&C Microsystems ..... 137
Bivar ..... 139
BP Microsystems ..... 139
Buscon/90 East ..... 124
Capital Equipment Corp. ..... 126
Clearpoint Research ..... 31
Cybernetic Micro System ..... 14, 140
Cypress Semiconductor ..... Cover IV
Data Instruments .....  85
Data I/0 ..... 56, 138
ECM for Midcom ..... 110
Emulation Technology ..... 138
Enertec ..... 139
Ericsson Components AB ..... 38John Fluke70
GE Plastics ..... 58-59
GCOM ..... 140
Hamilton Avnet ..... 34, 127
Harris Semiconductor ..... 64-65
Hewlett-Packard Co....1, 9, 49, 67-69, 97, 113
IEE. ..... 122
Integrated Device Technology ..... 37
IOtech ..... 139Lambda Electronics129-134
LeCroy Corp. ..... 63
Karl Leister ..... 114
Melfess Five ..... 138
Mentor Graphics. ..... 6-7
Mesago, Messe \& Kongre $\beta \mathrm{GmbH}$ ..... $\ldots$
MetaLink
MetaLink
99-102
99-102
Micro Linear ............ ..... 112
Mini-Circuits Laboratory,
a Div. of Scientific Components
Corp. ..... 15, 18-19, 104, Cover III
Motorola Semiconductor. ..... 51
Murata Erie


## 0

Object Design ..... 107
Omation ..... 139
Orion Instruments ..... 138
Outlook Technologies, Inc. ..... 26-27
Paradigm Technology, Inc. ..... 17
Philips Discrete Products ..... 20-21
Pico Electronics, Inc. ..... 16, 42
Plastics Engineering ..... 84
Potter \& Brumfield. ..... 83
PseudoCorp. ..... 140
Pulizzi Engineering ..... 139
Raytheon ..... 12-13
Rogers Corp. ..... 123, 139
Rolyn Optics ..... 138
-Saelig137
Samsung ..... 108-109
Sanyo Energy ..... 77
Sealevel Systems ..... 140
Siemens Components ..... 44
Siemens Corp. ..... 73, 75
Signum Systems ..... 139
Silicon Composers ..... 137
Silicon General. ..... 82
Single Board Solutions. ..... 138
Sony Microsystems Co. .....  28
Standard Microsystems, Inc. ..... Cover IITatum Labs, Inc140
T-Cubed Systems. ..... 137
Teltone ..... 140
Toshiba America. ..... 52-53



Vicor Corp117
White Technology ..... 120
Xeltek ..... 140
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[^4]:    Analog Devices, Inc, One Technology Way, P. . Box 9106, Norwood, MA 02062-9106; Headquarters: (617) 329-4700; California: (714) 641-9391, (619) 268-4621,(408) 559-2037; Colorado: (719) 590-9952; Maryland: (301) 992-1994; Ohio: (614) 764-8795; Pennsylvania: (215) 643-7790; Texas: (214) 231-5094; Washington: (206) 575-6344; Austria: (222) $885504-0$; Belgium: (3) 237 1672; Denmark: (2) 845800 ; France (1) 4666-25-25; Holland: (1620) 81500 ; Israel: (052) 911415 ; Italy: (2) 6883831 , (2) 6883832 , (2) 6883833 ; Japan: (3) 263 -6826;Sweden: (8) 282740 ; Switzerland: (22) 315760 ; United Kingdom: ( 932 ) 232222; West Germany: (89) 570050 . EDN, "EDNs DSP Benchnarks," September 29, 1988.

[^5]:    Micro Linear 10BASE-T products are available in both

[^6]:    $\dagger+$ Midband $10 \mathrm{f}_{\mathrm{L}}$ to $\mathrm{f}_{\mathrm{U} / 2}, \pm 0.5 \mathrm{~dB}$
    $\dagger \mathrm{IdB}$ Gain Compression $\diamond$ Case Height 0.3 In .

[^7]:    Analogic Corp., Data Conversion
    Products Group, 360 Audubon Rd., Wakefield, MA 01880; (800) 446 -
    8936. GTIGIF 307

[^8]:    Also available through Mektron Europe, Ghent, Belgium and Rogers Inoue Corp., Nagoya, Japan.
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