FOR ENGINEERS AND ENGINEERING MANAGERS — WORLDWIDE

JUNE 12, 1986

ELECTRONIC® DESIGN

A HAYDEN PUBLICATION

ECL faces competition in sub-ns gate arrays

X.25 comm boards take to the VMEbus

Las Vegas sizzles as Design Automation Conference moves in

CAE software lets designers use actual device layouts


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Once upon a time, we only supplied IDC flat cable and connectors...

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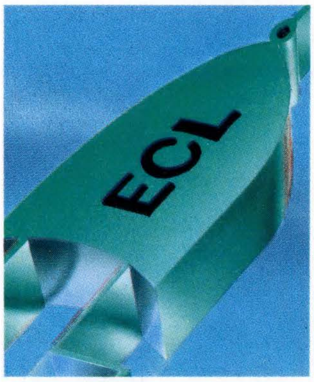
INSIDE LOOK

Designing in the fast lane



Raw speed has always fascinated humans—cars hitting 200 mph at Indianapolis, the Concorde landing in New York before its take-off time in Paris, bullet trains in France and Japan barreling down the track at 300 mph—and, for electronic design engineers, logic systems running at 100 MHz and up.

For a growing number of designers, anything under 100 MHz seems like poking along in a horse-drawn carriage. Subnanosecond speed is the name of their game in such things as automatic test equipment, complex graphics, fiber-optic communications, robotics, real-time process controllers, and the like.

Now, new types of subnanosecond gate-array chips are arriving to help designers cope with the problems. These chips differ from early gate-array chips in more than just speed; they represent a whole new approach to using gate arrays.

The early TTL-based gate arrays were aimed at simply reducing costs by squeezing many discrete IC logic blocks into one large chip, thus eliminating bulky pc boards. The arrays may also have improved performance by cutting path delays, but that was a bonus.

By contrast, the fast ECL arrays are opening fresh applications. In fact, with the new breed of gate arrays, designers are likely to leapfrog the discrete logic phase and go directly to the gate-array implementation. Often the designs are not feasible with discrete SSI- or MSI-level ECL, as those multiple-chip implementations are just too expensive and require ungainly cooling measures.

What's more, with the arrival of the fast arrays, designers now have choices beyond silicon-based ECL. As discussed in the ELECTRONIC DESIGN Report on p. 74, ECL still has a clear lead in subnanosecond gate arrays, but it's facing a challenge from CMOS. Gallium arsenide arrays are coming on strong, too, although their cost remains a major drawback.

No matter how the race among technologies shapes up, one thing is clear: With systems continually setting speed records, the sure winner today may be ripe for the overtaking tomorrow.

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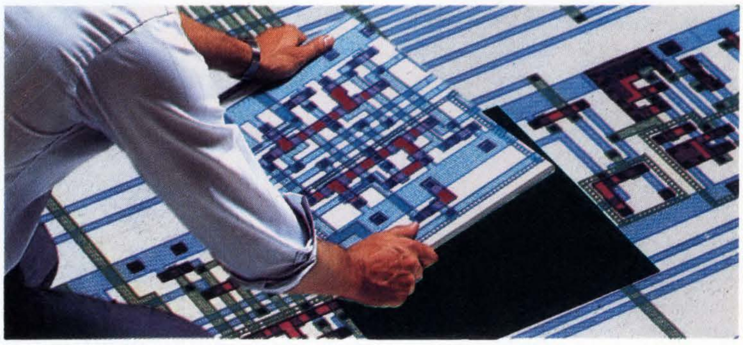
ELECTRONIC DESIGN

Departments



News

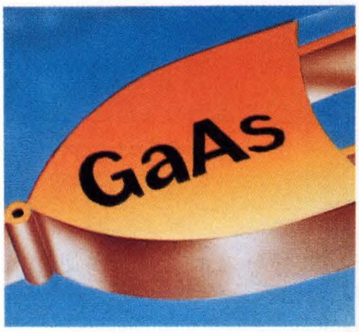
Newstrend

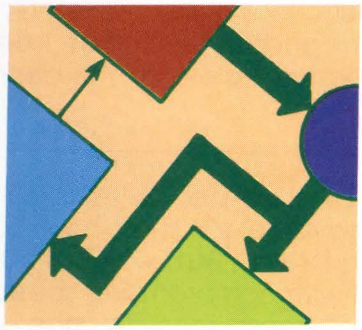
Industry Newsmaker

Electronic Design Report

Design Entries

1986 winner, Jesse H. Neal
Editorial Achievement Award.
Best in-depth analysis article series:
1985 Technology Forecast





In The Next Issue

Designer's Special Edition

- Special reports on hybrid circuits and DIN keyboards
- Directory of microprocessor development systems
- Product Probings: 16-bit microprocessors, logic analyzers, and fiber-optic connectors

Design Applications

Cover photography by Herbert/Wagner Computer Images

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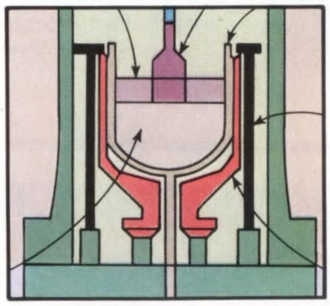
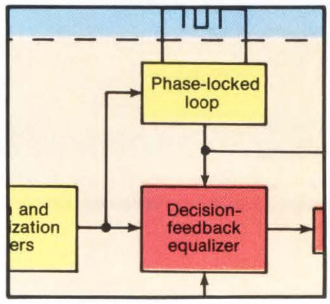
New Products

DON'T MISS THESE...

23 A newly developed ingot-growing process may cut the price of gallium arsenide devices by producing five times as many usable wafers from one ingot. Surrounding the molten GaAs is a magnetic field that keeps temperatures close to the desired value.

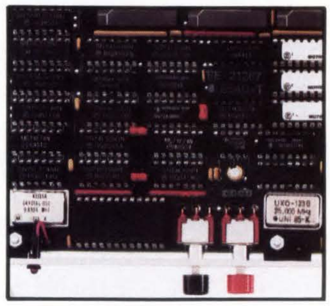


51 Twisted-pair wire is still a favorite for short-haul data transmission. But when you're faced with compromising speed in favor of transmission distance, you might consider this transceiver chip. By adapting to line losses, it passes up to 4 Mbits/s over 3000 ft of unshielded twisted pair.



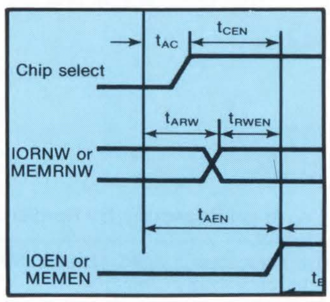
57 With an international packet-switching network finally in place, the action in X.25 products is heating up.

VMEbus board manufacturers have hopped on the bandwagon, introducing X.25 links that transfer data at speeds of up to 10 Mbits/s and that also run OSI software.



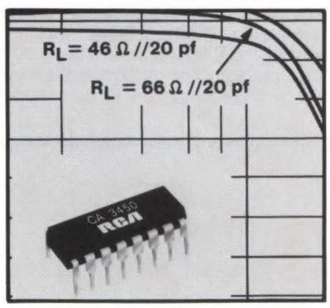
115 Microprocessor systems usually need a separate chip for each peripheral function.

An ASIC cell library now lets you combine all the functions you need on one chip. We're talking about CRT, DMA, bus, and programmable interrupt controllers, as well as counter-timers, RAMs, and ROMs.



133 If it's bandwidth you need in a monolithic op amp, will 170 MHz at unity gain do? That's the greatest bandwidth of any op amp chip around.

The IC achieves that bandwidth when operating without compensation at a noise gain of 10 and driving a 50-Ω load.



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Searching for a high-quality, low-cost amplifier? Our ZFL-500 flat from 50KHz to 500MHz, delivers 10 dBm output for the unbelievably low price of only $69.

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SPECIFICATIONS

Model No.	**ZFL-500**	**ZFL-1000G**	**ZFL-2000**	**ZFL-1000H**
Freq (MHz)	0.05-500	10-1000	10-2000	10-1000
Gain (dB), Min.	20	17	20	28
Gain Flatness (dB) Max.	±1.0	±1.5	±1.5	±1.0
Max. Power (dBm) (1dB compression)	+10	+3	+17*	+20
NF (dB) typ.	5.3	12.0	7.0	5.0
3rd order Intercept pt (dBm)	+18	+13	+25	+33
Current at 15V dc	80mA	90mA	100mA	150mA
Price $	69.95	199	179	219
qty.	1-24	1-9	1-9	1-9

For complete specs on these and our 1- and 2-W models refer to 1985-86 Gold Book or Microwaves directory.

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Such a demanding objective required demanding specifications: true 32-bit architecture; a complete computing cluster, including memory management and floating point coprocessors; full software compatibility, both upward and downward; high level language support; and comprehensive development tools.
The Siemens design team investigated a range of 32-bit solutions, and found only one that met all their needs: National's Series 32000 family.
Unlike other 8- and 16-bit processors being extended upward, the Series 32000 has no programmer-visible changes in architecture—throughout the entire family. So Siemens could develop any application the market demanded, now or in the future, without depreciating its existing software investment.
Which means the Series 32000 was not only the right engineering decision for today, but was also the right business decision for tomorrow.
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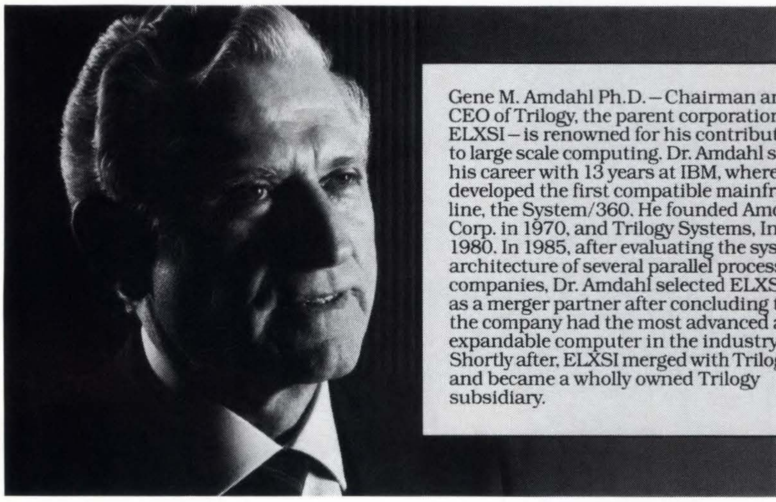
THE SUPERMINI ON A CHIP
SERIES 32000

Gene Amdahl tells how ELXSI's parallel multiprocessing computer fills the void between supermini and supercomputer.

"...we do a superb job of parallel processing and multiprocessing at the same time. Our 320 megabyte/second GIGABUS architecture eliminates bottlenecks and guarantees future expansion!"



Gene M. Amdahl Ph.D. – Chairman and CEO of Trilogy, the parent corporation of ELXSI – is renowned for his contributions to large scale computing. Dr. Amdahl started his career with 13 years at IBM, where he developed the first compatible mainframe line, the System/360. He founded Amdahl Corp. in 1970, and Trilogy Systems, Inc. in 1980. In 1985, after evaluating the system architecture of several parallel processing companies, Dr. Amdahl selected ELXSI as a merger partner after concluding that the company had the most advanced and expandable computer in the industry. Shortly after, ELXSI merged with Trilogy Ltd. and became a wholly owned Trilogy subsidiary.

"The difference between a parallel processing computer and a single-processor computer is significant. For instance, the single-processor supermini is very efficient – but it quickly reaches its limit. If you add more processors, you can increase total potential computing power, but there's no communication between CPUs; they find it difficult to share the load. The work doesn't get completed much faster, and one or more processors may frequently be idle.

Making multiple processors work

"We were the first company to take another approach to solve this problem. We place from two to twelve CPUs on a high speed bus – which we call the 'GIGABUS™' – with an advanced communications protocol to keep the processors working together. The system has two modes of operation:

"When multiple CPUs run different jobs concurrently they're in the Multiprocessing mode. But sometimes you have a large, long-running job, and want several processors to cooperate on processing it. Such operation is called Parallel Processing.

ELXSI, GIGABUS and System 6400 are trademarks of ELXSI

Multiple and Parallel Processing can coexist

"ELXSI™ is unique in that our System 6400™ can do an efficient job of Multiprocessing and Parallel Processing at the same time. It keeps the processing power of the system fully exploited, and system response optimized to the priorities of the user. This capability contributes greatly to the 6400's outstanding price/performance ratio.

Importance of the GIGABUS

"With the 6400, each CPU is tied through its cache memory to the 320 megabyte/second GIGABUS. If the CPU were tied directly to the bus, traffic density would be 10 to 20 times what it actually is. The interconnection point of the processors occurs at the lowest traffic-density point in the system. Low system traffic on the bus assures that communication interference can't generate a bottleneck in the system.

Gridlock and bottlenecks

"A bottleneck is a lot like 'gridlock' in a street with lots of traffic lights and heavy traffic. You can have a high powered Ferrari, but the traffic and traffic system restrictions won't let you go any faster than if you were in a golf cart.

"We provide much broader streets, with intersections farther apart, and we haven't found a Ferrari fast enough to create gridlock yet. Now, for the first time, a large system is able to use the total computing power available to it, and still have room to spare for growth."

ELXSI makes large-scale computing practical

ELXSI introduced the first commercial parallel processing computer in 1983, and today has more than 60 major installations around the world. System 6400 computers are used by up to several hundred engineers at a time, performing a wide variety of sophisticated engineering and scientific applications.

Many major aerospace companies use at least one ELXSI System 6400, including Rockwell, Boeing, Martin-Marietta, Singer Link, Hughes, Northrop and NASA.

At NASA/Ames Dryden Flight Research Facility at Edwards, California, the ELXSI system functions as a general-purpose computer supporting the entire engineering department, with applications ranging from analysis of space shuttle data to monitoring the flight test performance of experimental aircraft.

Other applications include circuit simulations, graphics image processing, structural analysis and computer-aided design, engineering and manufacturing (CAD/CAE/CAM).

Northwest Bell uses a 6400 for loop engineering, and Tektronix/CAE Systems uses theirs for designing gate arrays and developing software for complex PC board layout.

In addition, the system sees extensive use in companies such as Eastman Kodak, Honeywell and General Data Communications for complex integrated circuit layout.

Ask for product and application information on ELXSI's powerful System 6400 family. From ELXSI, 2334 Lundy Place, San Jose, CA 95131. Phone (408) 942-0900.

TRILOGY ELXSI

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CIRCLE 7

NEWSPULSE

Price of 68020 to plunge 46%

As of July 1 system designers can end their anxious wait for less expensive 32-bit microprocessors and peripheral chips. On that date **Motorola Inc.'s** Microprocessor Products Group (Austin, Texas) will **slash the price of two 68020 versions** by as much as 46%. In 100-piece lots, the 12-MHz 68020 will be tagged at $174—down nearly half from the current $325. Similarly, the 16-MHz chip will drop from $481 to $311. Dramatic cuts are also in store for the 68881 floating-point coprocessor, which is cropping up in more and more design specifications. In quantities of 100, the coprocessor will go for $131, down almost 50%. Designers looking for even higher speeds can opt for the 20-MHz version of the 68020 at $580, and a 24-MHz device that will likely be introduced late this year.

GaAs logic family unveiled

A broad-based **family of GaAs logic** chips will be introduced during the next 10 months by **Gigabit Logic Inc.** (Newbury Park, Calif.). Until now a handful of "silver bullet" GaAs ICs filled a few high speed functions like signal processing. Now, designers can build most of a board or a subsystem with the fast MSI chips—typical gate speeds are about 300 ps. The Pico Logic line will include adders, decoders, demultiplexers, gates, multiplexers, octal registers, and register files. The components are at least four times faster than ECL at more than five times the cost. Based on depletion-mode MESFETs, the surface-mounted devices interface easily with ECL.

System inspects unsoldered circuit boards

A vision system for manufacturing circuit boards packs a one-two punch, evaluating both sides of an unsoldered board at once. Most **vision systems** look at only soldered boards and only one side at a time. The DR 2000, designed by **Intelledex Inc.** (Corvallis, Ore.), makes repair a much simpler matter and also doubles throughput over other machines. Introduced at Vision '86 last week in Detroit, the system compares live camera images with correct specifications stored in memory. It then passes or fails the boards based on criteria like lead lengths, clinch and wipe angles of the leads, and proximity to neighboring contacts. Moreover, it detects the presence or absence of the required components, be they surface-mounted, leaded, or hybrid.

Will SCSI and ESDI coexist?

Don't bet on predictions that the Enhanced Small Device Interface (ESDI) will supplant the slower Small Computer Systems Interface (SCSI). The race is not over. Winchester drive buyers looking for high-capacity 5¼-in. units seem to favor SCSI-based interfaces for office networks, whereas the faster ESDI-based devices get the nod for high-performance graphics workstations.

Drive designers are responding to the dichotomy by **offering a choice of interfaces.** For example, at next week's National Computer Conference, **Micropolis Corp.** (Chatsworth, Calif.) will announce a 382-Mbyte subsystem with both SCSI and ESDI ports. Furthermore, Fujitsu America Inc. (San Jose, Calif.) predicts that the performance distinctions between ESDI and SCSI may disappear within two or three years. A synchronous SCSI controller promoted by Fujitsu could boost data rates to 2 Mbytes/s, if not more.

Analog IC eases T1 link to ISDN

Connecting T1 lines to an integrated services digital network (ISDN) is getting simpler, thanks to a smart analog chip from **Crystal Semiconductor Corp.** (Austin, Texas). To be introduced later this month, the CMOS device operates at ISDN's 1.544 Mbits/s and contains a **programmable pulse-shaping line driver** that compensates for differences in line lengths and types. It transparently frames data in the T1 format, includes phase-locked-loop circuitry, and replaces about six discrete components. The chip's 16 bits of elastic storage remove up to 14 unit intervals of jitter. In addition, a monitor circuit detects and isolates malfunctioning T1 lines. The 5-V chip is housed in a 28-pin plastic DIP.

Japanese seek memory, logic on light emitters

Speculation had it that the new **optoelectronic consortium** of Japanese electronics companies would focus on the optical computer. But the Opt Technology Research and Development Co. will initially zero in on high-speed data communications over fiber-optic cable, says analyst Sheridan Tatsuno of Dataquest Inc. (San Jose, Calif.). He contends that the group, made up of NEC, Hitachi, Toshiba, Fujitsu, and nine other Japanese companies, wants to develop a second-generation of semiconductor lasers—**light emitters with memory and logic integrated on the same chip.** Tatsunò predicts that a lattice structure of indium phosphide, gallium aluminum arsenide, and gallium arsenide layered on a silicon substrate will be used to produce a light emitter capable of 1.6-Gbit/s transmission rates.

Robots to sense temperature and pressure

Researchers aim to endow industrial **robots with fingers** for sensing pressure, temperature, and proximity of objects. Under NASA funding, a team at **Stanford University's Center for Integrated Systems** (Palo Alto, Calif.) is developing a tactile-sensing grid made of rows of silicon circuits on a skinlike flexible polyimide substrate. A 5-by-5 grid of sensors can detect normal and shear forces, a 16x16 grid is on the way that will sense temperature and proximity with signal-processing circuitry. The Stanford researchers are also trying to boost yields in the wafer backside-etching process. In addition, they are considering a sensor-addressing scheme with triple redundancy for optimal fault tolerance, response time, and silicon use.

Custom chip costs capped

The expense of fabricating standard-cell–based semicustom chips need no longer be couched in "ifs, ands, and buts." **Zymos Inc.** (Sunnyvale, Calif.) has developed a procedure, dubbed Sure Fire, that enables it to **quote a fixed price** for standard-cell designs submitted in either schematic or net-list form.

Using that information, Zymos estimates the gate count and even does rough layout and routing to determine a quote. The preliminary layout helps circumvent cost penalties exacted by belatedly discovered design errors. There is no fee for the Sure Fire service, but once a customer commits to Zymos, there is a modest charge for the CPU time required for the circuit simulator, router, and other design tools.

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The IMS2800 from INMOS. Experience the speed for yourself.

Part Number	Function	Address Access Time (Max.)	$\overline{RAS}$ Access Time (Max.)	$\overline{RAS}$ Read/Write Cycle Time (Min.)
IMS2800-60*	Static Column Decode	32ns	60ns	121ns
IMS2800-80		43ns	80ns	146ns
IMS2800-10		53ns	100ns	176ns
Part Number	**Function**	**Column Access Time (Max.)**	**$\overline{CAS}$ Access Time (Max.)**	**Page Mode Cycle Time (Min.)**
IMS2801-60*	Enhanced Page Mode	32ns	11ns	35ns
IMS2801-80		43ns	13ns	46ns
IMS2801-10		53ns	16ns	56ns

Data on Nibble Mode and Extended Serial Mode versions available upon request.

*Contact factory for delivery.

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EDITORIAL

Keeping you on the leading edge with exclusives

Magazine publishing has never had the same glamour as television or Hollywood. But believe me, on occasion it provokes the same sort of name-calling and fierce competition that prevails in those industries. In fact, there's one helluva brouhaha going on right now. I'm talking about the controversy over ELECTRONIC DESIGN's exclusives.

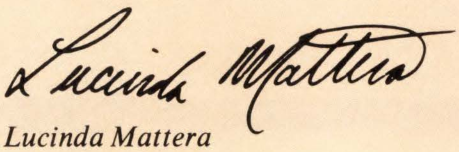
For the past six years, ELECTRONIC DESIGN has held the enviable position of exclusively breaking virtually every major electronics announcement to you, our reader. We've introduced literally thousands of new products, new design concepts, and new technologies—weeks, if not months, ahead of all other publications in the world. Needless to say, exclusives give ELECTRONIC DESIGN a singular advantage, one that has irritated other publications for years.

Why do we do it? Simple. We know that being first is an important part of your competitive edge and of ours. We understand how critical timeliness is to your job, especially with product lifetimes shrinking and product development times expanding.

Recently, other publications have accused ELECTRONIC DESIGN of extra editorial enticements just to get an exclusive. Nonsense! The technical expertise of our staff is why ELECTRONIC DESIGN garners exclusives so successfully. It all boils down to solid coverage by the most knowledgeable editors in the business.

To counter that success, some publications—the weeklies, primarily—have set a new editorial policy, one that I consider very questionable. If a story or announcement is given exclusive treatment by anyone else, those weeklies refuse to cover it at all. Talk about cutting off your nose to spite your face.

At ELECTRONIC DESIGN, we believe in bringing you the best coverage on the most important events, be they our exclusives or not. Indeed, ELECTRONIC DESIGN is the publication you can count on—exclusively.



Lucinda Mattera
Editor-in-Chief

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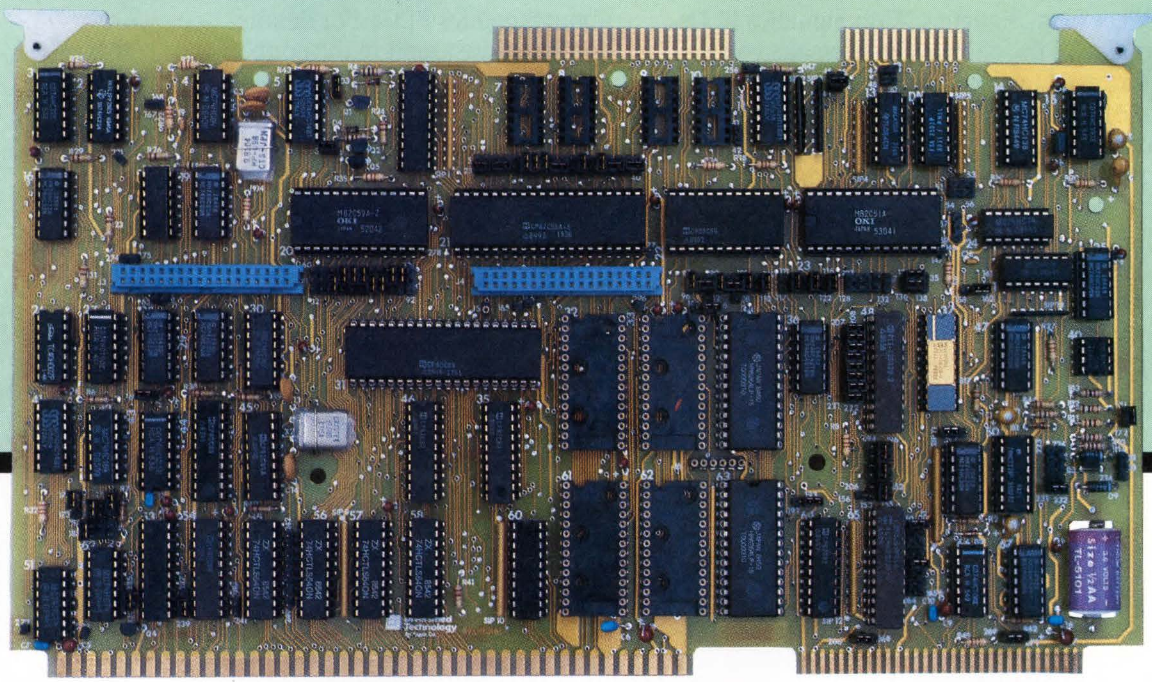

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CIRCLE 11

OCCASIONALLY, EVERYONE WISHES HE HAD ANOTHER SHOT AT HIS DESIGN.

There are some things man was not meant to tamper with.

Semicustom circuits, for example. If you happen to have second thoughts about your design, you're powerless to do anything about them. Unless you have the luxury of lots and lots of time and money. But when you're trying to get your products to market before the competition, extra time is something you rarely have, and extra money is something you *never* have.

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TEK 7934
STORAGE OSCILLOSCOPE

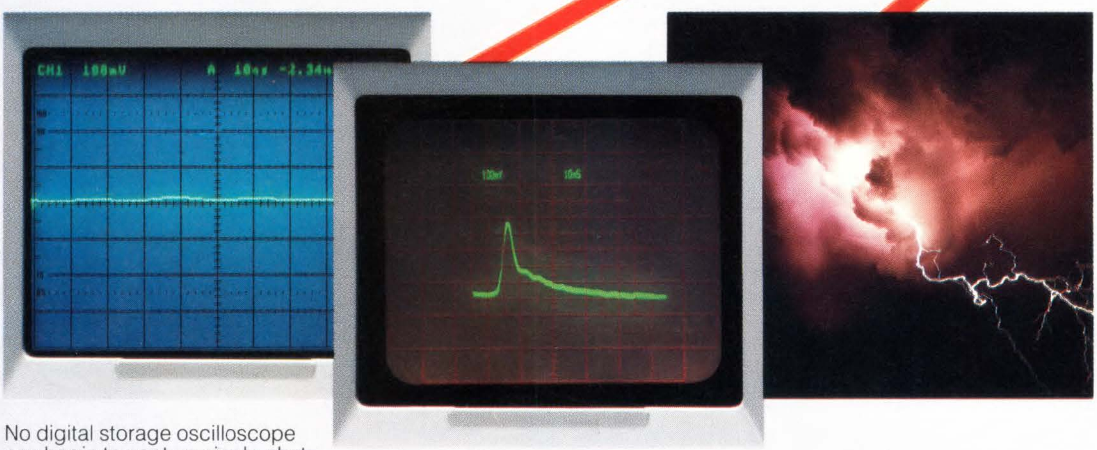
Tek's new 7934: at 4 cm/ns it catches what no digital scope can!

With its 500 MHz bandwidth, 700 ps risetime and 4 cm/ns writing rate, the new Tek 7934 is the fastest storage oscilloscope in the world. When you're working with any combination of outer-edge measurements, one-shot opportunities and now-or-never timelines—the 7934 will show you what you're looking for when all else fails.

Glitches that slip between digital sampling intervals, details distorted by lesser bandwidth scopes—show up the first time, every time, on the 7934. The 7934 gives your measurement capabilities a welcome boost if you are pushing the edge of high-speed digital design; NMR, EMP and laser research; advanced power supplies, and other applications where fast transients and high-frequency bursts defy digital detection and capture.

The 7934 also serves as a general-purpose, non-store 500 MHz oscilloscope—further adding to the flexibility of a system that begins with some 30 interchangeable plug-ins and lets you design your own scope.

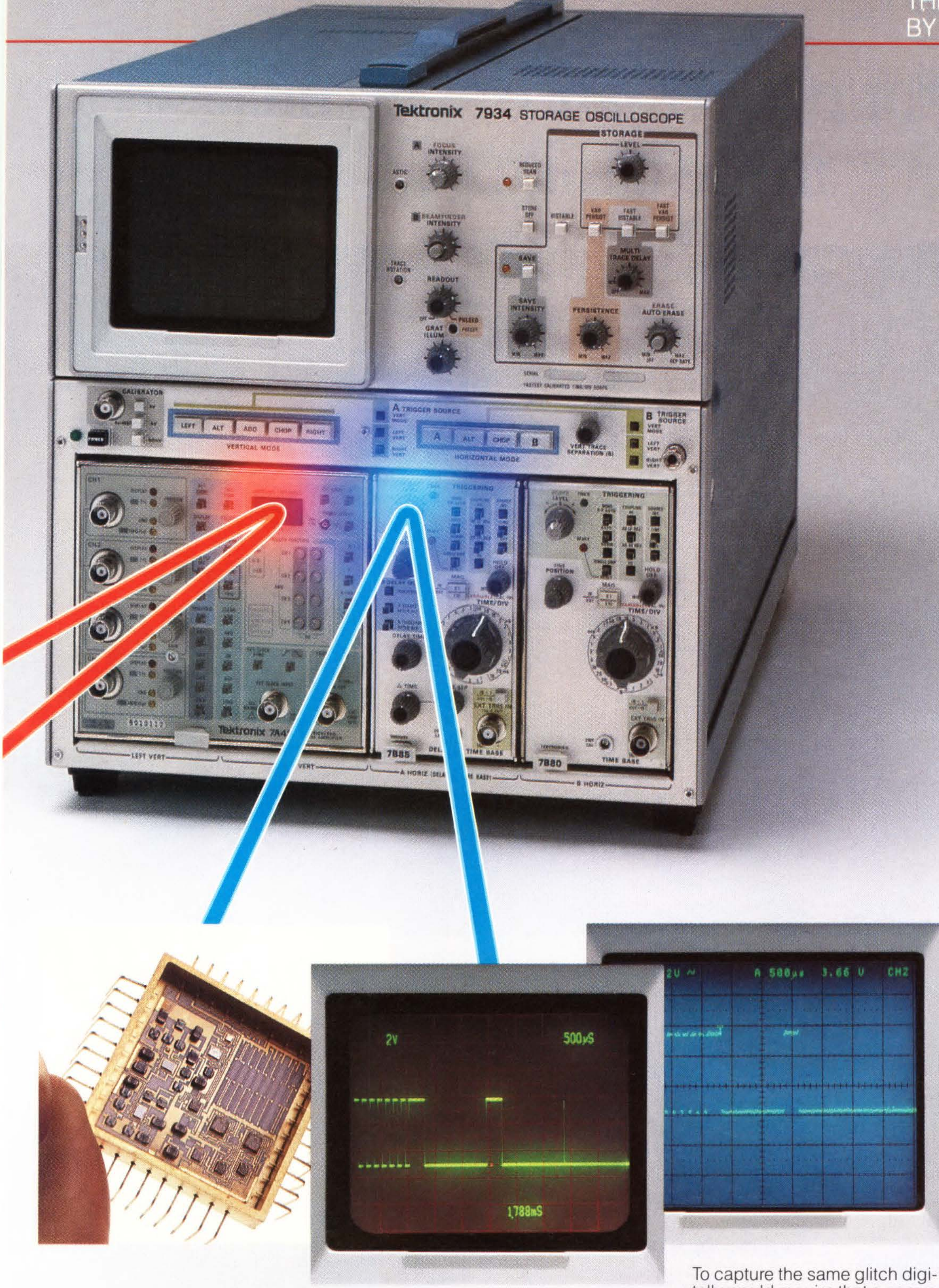
For a sure shot at the fastest waveforms you ever saw, see the new 7934 soon. Contact your local Tek sales engineer, or call (800) 547-1512 for more information. In Oregon: (800) 452-1877.



No digital storage oscilloscope can begin to capture single-shot events and fast transients.

Transient Capture. Single-shot electrostatic discharge captured using the 7934's Fast Variable Persistence storage mode in reduced scan and 7A29 Dual Trace Amplifier plug-in.

THE ANSWER
BY ANY MEASURE



Glitch Capture. The 7934 captures a glitch (near 8th division) in VLSI circuit design using a 7A29 Dual Trace Amplifier plug-in and variable persistence storage mode.

To capture the same glitch digitally would require that a scope have a sample interval narrower than the glitch. Even then there is no assurance you would know the glitch's true amplitude.

CIRCLE 14

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Magnetic field boosts GaAs wafer yield fivefold

BY DAVE BURSKY

Kawasaki, Japan—The cost of the IC-quality gallium arsenide wafers used for picosecond logic may soon tumble by a factor of five. An ingot-growing technique adopted by Toshiba Corp. surrounds the molten GaAs with a 3400-Gauss magnetic field keeps temperature fluctuations within the melt to less than 1°C, thereby avoiding the 15°C variation typically encountered without a magnetic field. Tight control over temperature lets the gallium and arsenide mix more consistently as the single-crystal, liquid-encapsulated Czochralski ingot is pulled from the molten material.

The greater consistency should allow Toshiba to cut five times as many usable wafers from each ingot. With more wafers coming from the same amount of material, the process will likely translate directly into less expensive wafers.

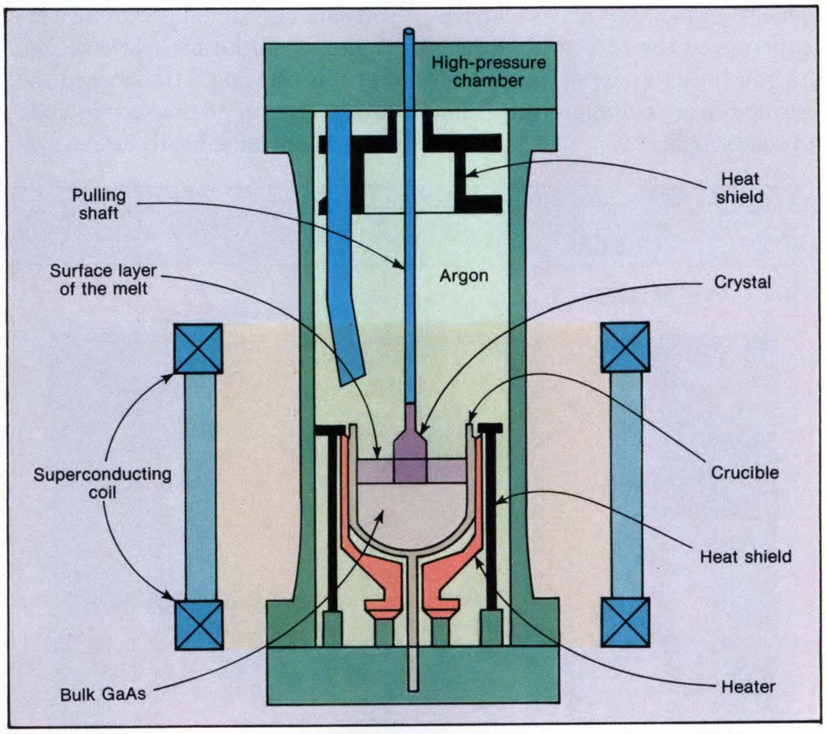
PRECEDENCE SET

The Toshiba project is not the first to use a magnetic field for ingot growth. Just last year the Optoelectronics Joint Research Laboratory—an industry-wide group sponsored by Japan's Ministry of International Trade and Industry—used a magnetic field for GaAs wafers with 2-in. diameters. Now Toshiba applies the technique to wafers with 3-in. diameters.

Besides distributing gallium and arsenide evenly through the melt, the magnetic field also disperses carbon. In addition, Toshiba's improved heater design allows only one-third as much carbon to reach the ingot as other techniques allow (see the figure). The less carbon in the material, the fewer defect sites and, therefore, the higher the circuit yield of good devices.

Another benefit of the improved material means a big bonus for the circuit designer. To build complex LSI circuits with GaAs, the transistor threshold voltage should deviate as little as possible from the nominal value.

Earlier GaAs chips exhibited deviations of 35 to 50 mV, too wide a range to ensure high yields for complex circuits. The Toshiba approach keeps variations below 20 mV. At that level, the process stands a much better chance of turning out such complex circuits as 4- and 16-kbit static RAMs and multithousand-gate arrays. □



Surrounding the GaAs ingot growth chamber is a superconducting coil that generates a magnetic field of 3400 Gauss. The field better controls the molten material's temperature.

HP spreads its CAE wings with third-party software

BY BOB MILNE

Fort Collins, Colo.—After a somewhat tardy and low-key entry into the CAE arena, Hewlett-Packard Co.'s Design Systems Group is rolling up its sleeves and getting serious. In May the company took the wraps off a raft of hardware upgrades for its workstations. As a follow-up, this month HP is integrating a long list of design functions, many drawn from outside sources, into its workstation-based system dubbed the

DesignCenter.

On the list are board layout, analog schematic entry and simulation, computer-aided software engineering, and HP's 64000-UX microprocessor development environment. Moreover, enhancements are being added to the logic design system introduced last year.

With these additions, the DesignCenter can support electrical and mechanical engineering along with microprocessor software development. In fact, HP may well have leapfrogged the rest of the workstation industry by offering the broadest array of design tools from any one supplier.

To get to this point from what was a standing start, HP augmented its own hardware and software products with third-party electrical and mechanical design tools. Just as HP buys resistors, capacitors, and ICs from others to build instruments, it now relies on externally developed software for its CAE lineup.

AUTOMATIC BOARD DESIGN

The new pc board design package automatically lays out digital, analog, and mixed digital-analog boards with through-hole and surface-mounting technologies. The software also contains extensive facilities for thick-film hybrid design. For this offering, HP licensed the latest version of the source code for a mainframe board design system from Northern Telecom (Nashville, Tenn.) and its subsidiary, Bell Northern Research (Ontario).

To handle analog designs, HP fully integrated the Analog Workbench software from Analog Design Tools Inc. (Menlo Park, Calif.). Thus, designers will be able to capture schematics with HP software, then pass the analog portion to the Analog Workbench software for simulation and verification. Digital and analog data can then be reintegrated into a common-user data base on the HP hardware. In this way, schematic output, layout, and other tools all can be used.

The DesignCenter gains the power to do computer-aided software engineering from the HP Teamwork/Structured Analysis software package. A companion for the HP 64000 logic design system, the package is the first in a series intended to help engineers develop and manage software specifications. It lets a project team capture design requirements quickly and easily and organize them into models for evaluation and maintenance.

BETTER DESIGN SYSTEMS

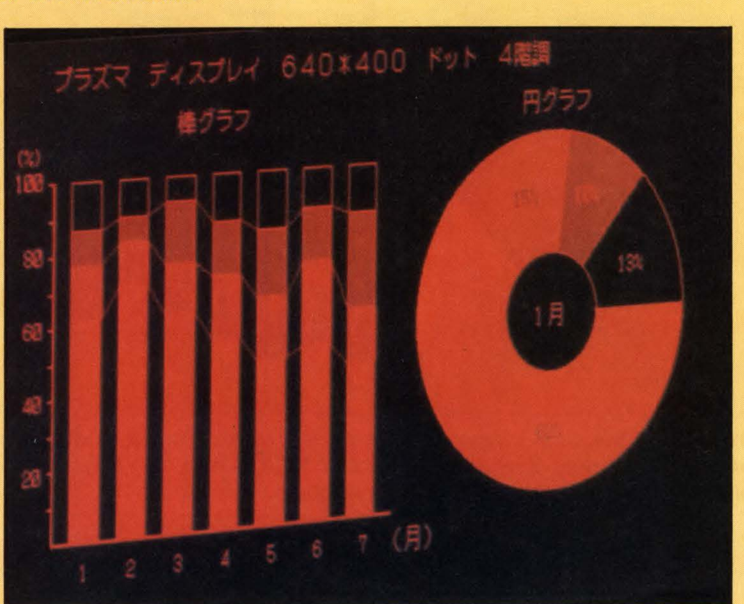
To enhance its logic design system, HP is adding color display software and improving the design capture and verification setups. For example, gate-array libraries from NEC Corp. (Mountain View, Calif.) consist of more than 150 cells all told and support NEC's full line of CMOS gate arrays in 2-μm geometries. The engineer has over 20 types of popular CMOS logic devices to choose from, ranging in complexity to 20,000 gates.

Design verification gets a boost from the Hichip universal hardware modeling system from GenRad Inc. (Santa Clara, Calif.). With Hichip, simulations can be conducted with an actual VLSI device rather than a software model. The system complements the Hilo-3 simulation tools already available on the logic design system.

Importantly, the logic design system is tightly coupled to HP's new

Efficient gray-scale plasma display debuts

BY DAVE BURSKY



Custom display drivers combine pulse-width modulation and 64 channels to yield the first commercial plasma display with up to 16 gray-scale levels. Panasonic Industrial Co. (Secaucus, N.J.) introduced the display a few weeks ago as a screen for computers or instruments used for graphics-intensive applications such as bar and pie charts (see the photograph).

Other plasma displays use software to get limited gray-scale shading, but the processing overhead slows the application programs. With silicon controlling the intensity, the driver chips can vary the dot-pulse width over four levels—full intensity, two-thirds, one-third, and background. Initial estimates place the cost at about the same as non–gray-scale subsystems: less than $500 each in large volumes ($1200 for samples).

board design system, forming a complete front-to-back solution. The two systems automatically transfer net lists and parts information while keeping track of engineering changes and back-annotated data. Added interfaces help move logic design information to other board layout systems, including the HP Engineering Graphics System and systems from Racal-Redac (Westford, Mass.) and Computervision (Bedford, Mass.).□

MAP development system spurs on factory networks

BY ROGER ALLAN

Laguna Niguel, Calif.—The first development system for the Manufacturing Automation Protocol (MAP) promises to ease the design of factory networks. Called MAPStart, the system can simulate and evalute MAP compatibility among up to 32 factory automation elements, such as robots, programmable controllers, data-collection devices, sensors, and work cells.

MAPStart was developed by Honeywell Inc.'s subsidiary, Digital Datacomm Inc., and will be licensed beginning this summer. The system helps determine the types of data that can be collected, as well as how much traffic the MAP network can handle. It also identifies data storage loads and hardware requirements for local processing.

TRY BEFORE YOU BUY

"Users can begin with MAPStart in the laboratory, develop their own applications, and then transport the whole thing down to the factory floor," says Wayne Kerr, Digital Datacomm's director of R&D and MAPStart's principle developer.

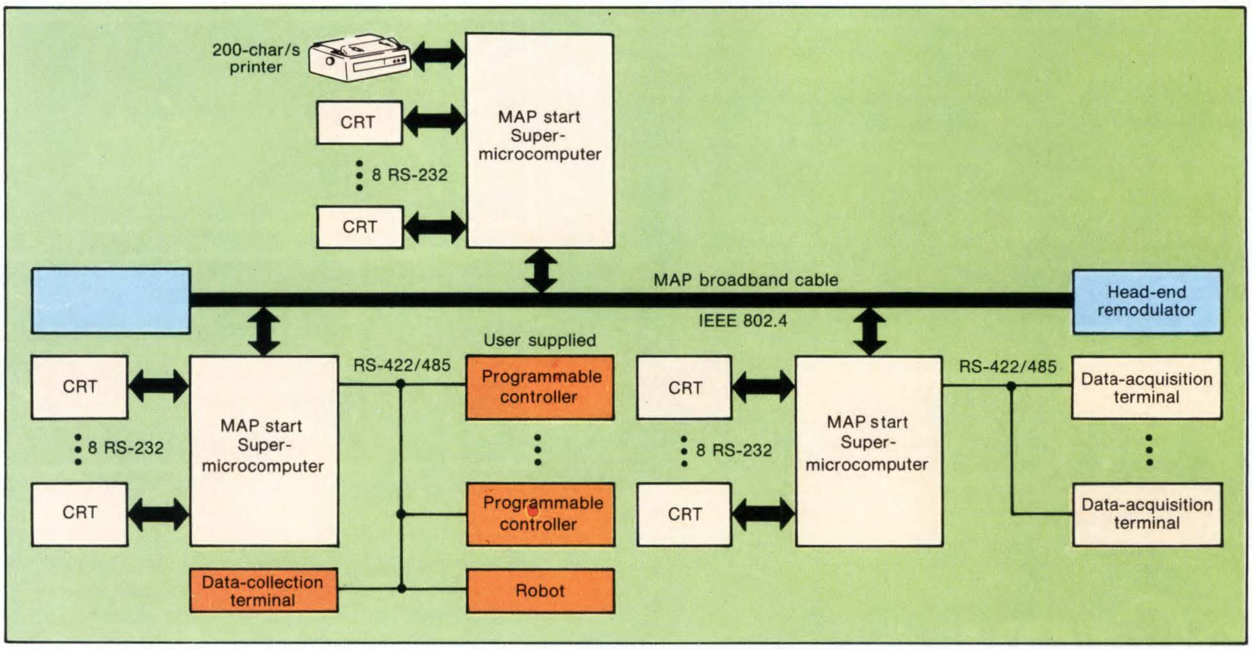
MAPStart's test configurations can be horizontal or vertical. The system can simulate data transmission across several work cells or concentrate on communication within one particular work cell and its supervisor. The system now operates at 5 Mbits/s over the IEEE-802.4 broadband backbone, but a 10-Mbit/s version is under development.

Supported by Honeywell's Manufacturing Systems Division (Phoenix), MAPStart is expected to cost about $176,000. Though the price may seem steep, it will allow a user to work with MAP before making a significant capital investment.

The system handles any brand of MAP-compatible automation equipment. It comes complete with processors and operating systems, CRT terminals, broadband cable, head-end remodulator, splitters, terminators, and a 200-char/s printer (see the figure). The user need only develop application software.

At MAPStart's core are three supermicrocomputers, each based on a Motorola MC68000 microprocessor. Future versions will include the full 32-bit MC68020 microprocessor.

Each supermicrocomputer con-



The MAPStart development system, from Honeywell, will give designers a real-world analysis of MAP system requirements. It will simulate and test up to 32 robots, programmable controllers, and other factory floor devices. (The orange area represents user-supplied hardware.)

tains 2 Mbytes of dynamic RAM in main memory, 4 kbytes of high-speed cache static RAM with 20-ns access times, a floppy-disk drive, and a magnetic tape for backup. Each processor is Multibus-compatible and has eight RS-232 serial ports and one parallel port. Two of the supermicrocomputers have 55-Mbyte Winchester disk drives, the third has an 85-Mbyte unit.

The computers run under a Unix-derived real-time operating system that handles the current MAP version 2.1 upper-layer protocols (ELECTRONIC DESIGN, May 15, p. 102). As other protocols become standardized, they will be incorporated into future MAPStart versions.

A key achievement in MAP-Start's design is the 68000's memory-management unit (MMU). A proprietary implementation, it lets the processor operate at its maximum clock rate of 12.5 MHz with no wait states. Typically, a system incurs one or two wait states because its memory functions more slowly than the microprocessor.

Says Kerr: "Our MMU allows us to do more things faster at the cell level—responding to interrupts faster, getting data to the network faster, and so on. Speed is a critical issue on the shop floor."□

Corporate CAD network ties disparate CPUs, software

BY MARTIN GOLD

Princeton, N.J.—To manage CAD resources more effectively at its various operations, RCA Corp. is putting together the final links in a massive corporate-wide design network. Workstations, minicomputers, and mainframes around the country will tie into an integrated communication system to speed hardware and software development. Moreover, the system will bring together design tools from various suppliers.

Going by the name Victor, the network is scheduled to be phased in this month and to be up and running some time later this year. RCA component plants here, in Somerville, N.J., and in Lancaster, Pa., will be hooked up to the company's television factory in Indianapolis, as well as to its military equipment works in Moorestown, N.J.

"Victor can be considered a generic mousetrap," says James Miller, director of engineering computing for RCA and head of the project. "While the system's main focus is on VLSI, it can also be used for mechanical, equipment, and software design."

The heart of the communication system is Victornet, which links Digital Equipment's VAX superminicomputers to Apollo workstations and IBM mainframes. VAX computers communicate using the Ethernet protocol, while the Apollos are joined to VAX machines via TCP/IP. Different operating systems will also be cohabiting: The workstations will run under Unix, the VAX machines under VMS, and the IBM mainframes under VM/CMS.

GROWING UP WITH SOFTWARE

Victor is a home-grown network. RCA is writing a large chunk of the software, such as the hard-to-come-by networking programs needed to transparently handle communication between software design tools.

Interestingly, RCA chose not to develop project management software. Instead, it incorporated a VAX-based program developed by Sherpa Corp. (San Jose, Calif.). RCA worked closely with the company, founded as Cadtec Corp. in 1980, for over a year to define and specify details of this package.

The two companies essentially created a file management system for a CAD network, primarily to monitor use of standard-cell libraries. The system automatically tracks and controls data access, including drawings, documents, and revisions related to any project.

Cell libraries can be easily updated, alerting designers to the latest revision. Sherpa's system will also indicate whether a simulation and design-rule check were performed on each cell library, and by whom.□

Simulation accelerators tackle logic and faults

BY TERRY COSTLOW

Hopkins, Minn.—A turnkey accelerator system for CAE workstations underscores its high speed with features that can save considerable design time and eliminate replication of tasks. The MX-100 from XCAT Inc., set to be introduced at the Design Automation Conference in Las Vegas later this month, lets users simulate both logic and faults on a personal computer or a workstation. And it does so at up to 2 million events per second.

The $49,000 to $200,000 system can work with IBM PC ATs and PC XTs, communicating at 1 Mbyte/s, as well as with Apollo workstations and Digital Equipment's VAX and

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CIRCLE 20

MicroVAX—CPUs. Furthermore, it taps into most popular communication networks and into XCAT's proprietary XNET.

Combining fault and logic simulation on an accelerator is still relatively new. Silicon Solutions Corp. (Menlo Park, Calif.), a three-year-old accelerator manufacturer, is introducing its logic and fault simulation accelerator, the Mach 1000F, at Design Automation. The system includes some timing features not found on the XCAT machine and processes simulations at 500,000 events per second.

Such accelerators give users a good deal of design flexibility. Breakpointing, for instance, lets them interrupt a task while it is running; the system then automatically stores all data on the task being interrupted. In contrast, many multitasking accelerators cannot be interrupted while running simulations or other tasks. Since simulation can take hours if not days, interruptions can cause a major bottleneck in making design changes.

Assume, for instance, that a gate needs to be altered during a simulation. Traditionally, the designer would either wait until the task was completed, or he would halt the operation, make the change, and then start the program from the beginning. The MX-100's save-and-restart feature lets the designer stop the simulation, then return to the same point later.

The system also saves many hours of design time by not repeating work that has already been done. A rework command lets users make minor changes, such as move a gate or wire, without recompiling the data base—a task that can take up to 40 minutes. The program builds an audit file so that all changes can be tracked at all times.

All features can be used in both logic and fault simulation, unlike in many other systems that address only one of these tasks. Running both tasks on the same system lets users access the same data base. It also makes it easier for a designer to put together a system that can be more readily tested.

Despite giving users a variety of options, the system does not scrimp on speed or capacity. It uses as many as 256 four-input, one-output primitives, including basic gates, flip-flops, bidirectional transistors, user-definable logic, and switch-level truth tables. Designers can also simulate up to 2 Mbytes of high-speed RAM or ROM.□

Common Lisp goes parallel in a big way

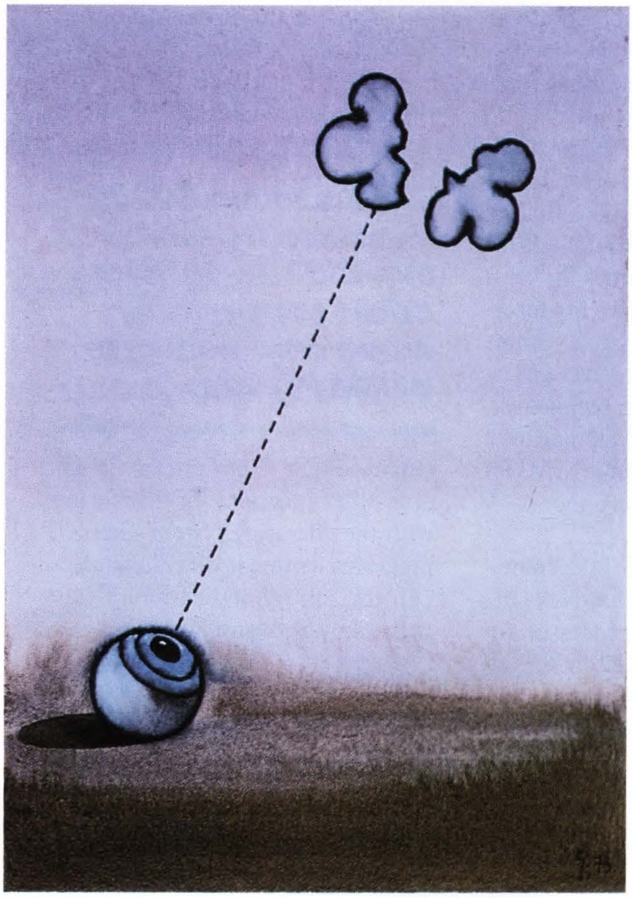
BY RAY WEISS

Cambridge, Mass.—Take a new parallel processor designed with off-the-shelf parts, and then add a well-established language for artificial intelligence. The resulting computer may give American systems a much-needed leg up over the Japanese. Equally important, it represents the commercial debut of an AI language for large-scale parallel processing.

Just last month Gold Hill Computers Inc. gave word that it had integrated its Golden Common Lisp language with the iPSC-VX, a multiprocessor system designed by Intel Corp.'s Scientific Computers Division (Beaverton, Ore.). The new iPSC-MX system, geared for the scientific community, is being billed as an ideal mechanism for studying concurrent processing for AI applications.

Yet the machine is more than just

If it happens in a blink, we'll catch it.



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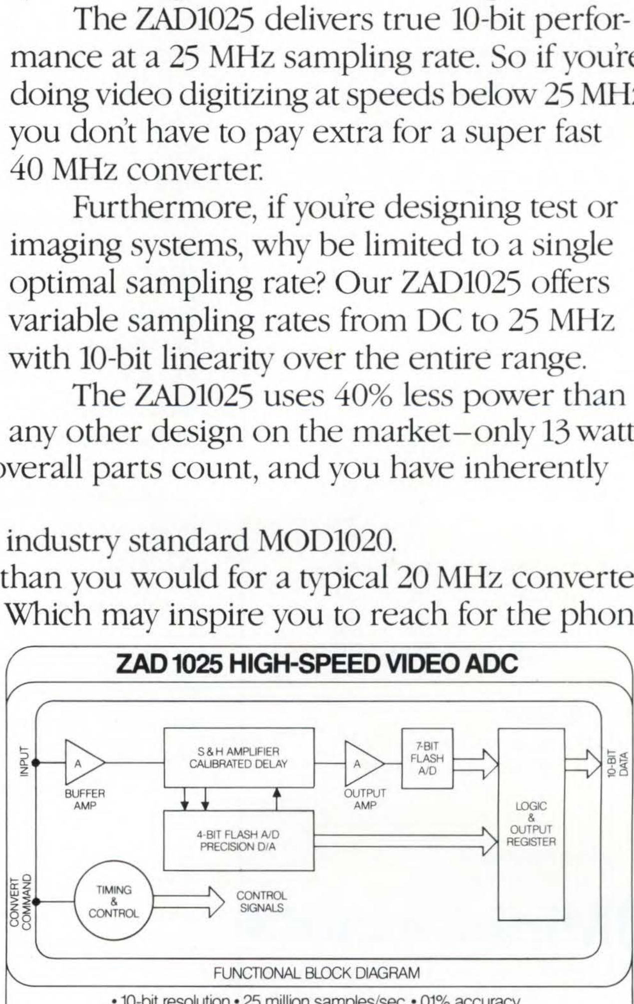
CIRCLE 22

ZAD 1025 HIGH-SPEED VIDEO ADC



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an esoteric research tool. The up to 64 processor nodes can simultaneously execute Lisp programs in a loosely tied configuration. Using 288 Mbytes, the iPSC-MX executes up to 50 MIPS. That level of power satisfies the tremendous demands of fifth-generation computer projects—say, systems that can perform high-speed symbolic processing—many reaching far beyond the realm of any workstations now running Lisp.

As American researchers buckle down in their contest against the Japanese, AI implementations will become critical. "The iPSC-MX opens up all kinds of possibilities for computing and specifically for intelligent parallel processing," notes Carl Hewitt, a professor at the Massachusetts Institute of Technology. One of the first iPSC-MX machines is scheduled to be delivered to MIT's Artificial Intelligence Laboratory later this month.

Another advantage of the combination stems from the hardware design. Intel's parallel processor design uses the 80286 microprocessor at each node in the hypercube interconnection concept developed by the California Institute of Technology. Since the iPSC-MX revolves around the same chip that drives the IBM PC AT, in the not-too-distant future, concurrent processing and Lisp software could conceivably move onto networks of PC ATs. Thus, progress at the hypercube level may invite software advances at the PC AT level.

THE EASY PORT

Designers at Gold Hill Computers were surprised at how easily they could port Golden Common Lisp to the iPSC's parallel structure. They simply added communication primitives for passing messages from node to node and from node to host. These primitives can dispatch Lisp object code from one node to another for remote execution. As a result, Lisp application software running on one node can transmit messages to any other node.

The code was fairly easy to implement, Gold Hill officials say, since the iPSC's underlying message-based operating system handles most of the message passing. Because the operating system is multitasking, several Lisp tasks can run on each node. Moreover, Golden Common Lisp supports multitasking through the use of different stack groups for tasks.

The Lisp package already accepted foreign subroutine calls to

Thanks to the 80286, concurrent processing and Lisp software could conceivably move onto networks of IBM PC ATs.

languages like C or Fortran. By adding other functions for interfacing with the operating system's kernel, programs written in other languages can run jointly and communicate with a Lisp task on a node.

GOLDEN RULE

Developed originally for the IBM PC, Golden Common Lisp is a subset of the emerging Common Lisp standard. It comes with a full set of development tools, including an Emacs-like editor. An existing version, the 286 Developer, is designed to run on the PC AT and within 15 Mbytes of memory.

By beefing up node memory to 4.5 Mbytes, Intel gave each iPSC-MX node enough storage to process Lisp. The iPSC-MX is available in configurations with 16, 32 or 64 nodes (ELECTRONIC DESIGN, April 17, p. 12). A system-wide Ethernet bus links the nodes to the host, while an Intel 810 development system running under Xenix acts as the host processor. Additionally, a dedicated AI processor like the Symbolics 3600 affords a sophisticated development environment.□

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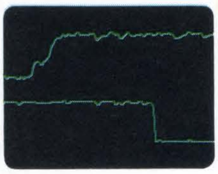

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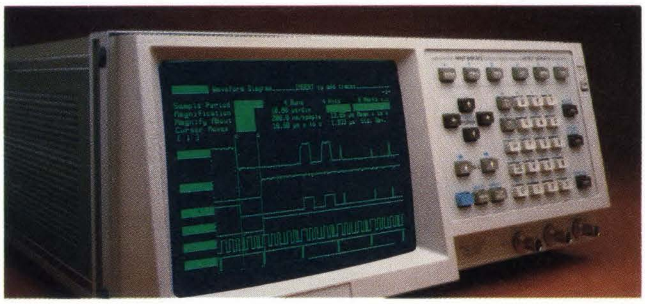

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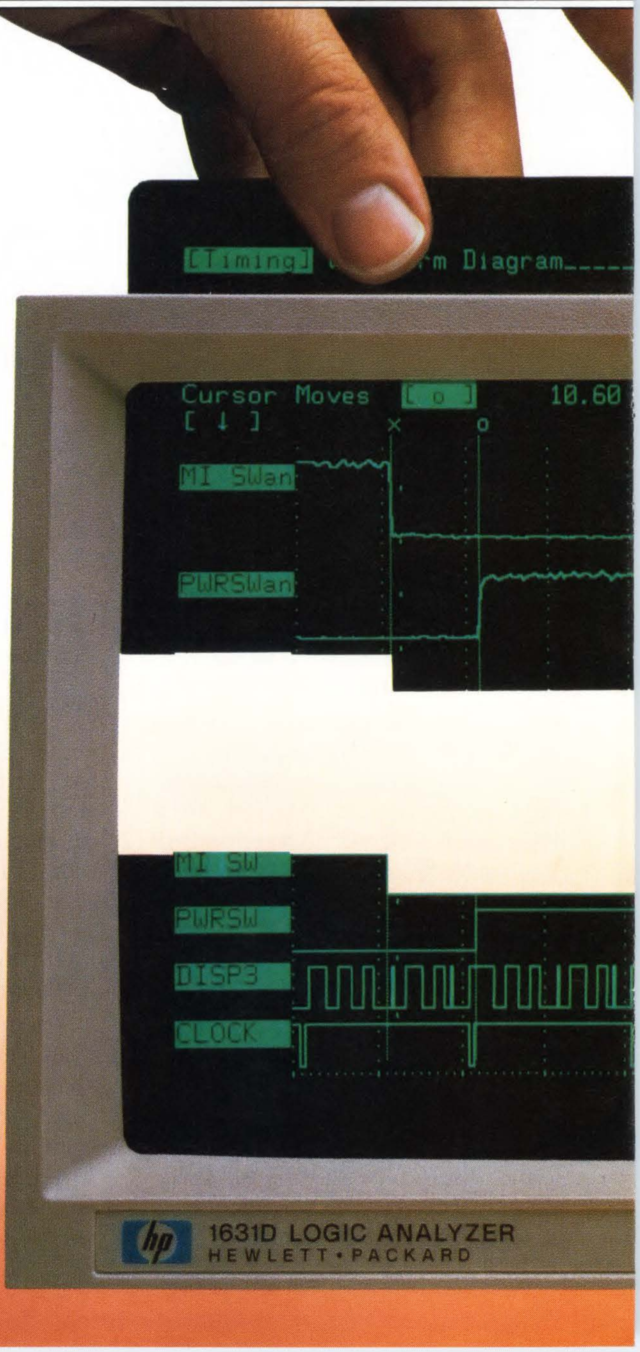

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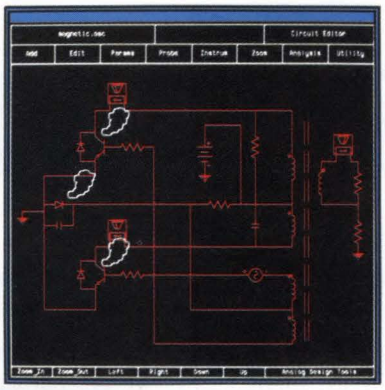

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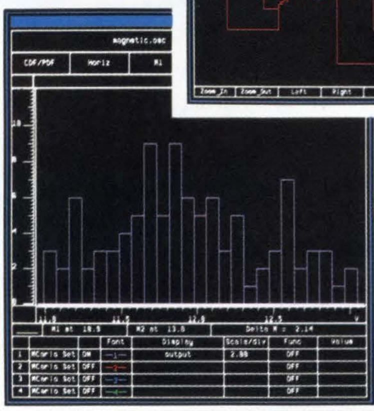

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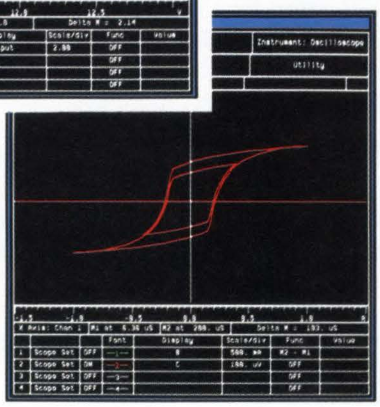

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ANALOG DESIGN TOOLS

CIRCLE 24

CONFERENCE PREVIEW

DESIGN AUTOMATION CONFERENCE

Advanced software improves silicon layout and sharply raises simulation efficiency

BY BOB MILNE

Silicon chip conservation and fast simulation for circuit design will be among the scores of topics to be discussed at the upcoming Design Automation Conference. Several universities, along with research teams from IBM and other companies, will describe recent work on software used to design and test integrated circuits.

Experiments on numerous industrial circuits show that a standard-cell placement and global routing package from the University of California can reduce a chip's silicon area by anything from 15% to 75%. Called TimberWolf 3.2, the software was devised by the university's Department of Electrical Engineering and Computer Science (Berkeley).

THREE-STAGE PROCESS

The package moves through cell placement and routing in three stages, the first two making use of a general combinatorial optimization technique called simulated annealing. In the first stage, the cells are placed in a way that conserves the amount of silicon algorithmically estimated for the interconnections.

In the second stage, the same simulated annealing procedure takes place after the insertion of feedthrough cells. The final part of the second stage, a global routing step, closely estimates the number of wiring tracks needed on the chip. In the third stage, local changes are made in the cells' placement to reduce the number of wiring tracks.

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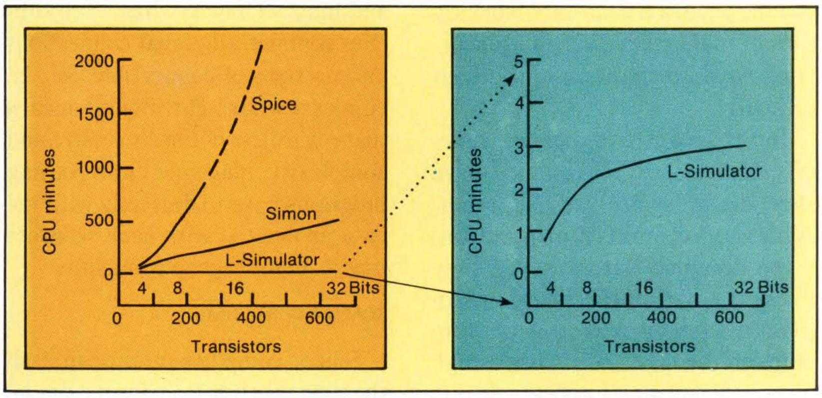
For evaluation, TimberWolf was put to work on some American Microsystems circuits. On CktF, a 2700-cell circuit, the cell placement saved 69.4% in area, with an additional 8% derived from the router for a total reduction of 75%.

According to the Berkeley report, TimberWolf fared well when compared with a commercially developed placement program. The comparison was made on two double-metal microcircuits, one containing 2500 cells along with two macro blocks, the other, 469 cells. On the larger circuit, total channel density was reduced by 36%. Moreover, TimberWolf needed 35% fewer feedthrough paths and 75% fewer feedthrough cells than did the other program.

For the smaller circuit, total channel density was reduced by 23%, and the number of feedthrough paths was reduced by 18%. In addition, feedthrough cells were not required.

In silicon compilers too, cell placement is of great importance. Control Data Corp.'s Advanced ECAD Laboratory (Minneapolis) joined the University of Minnesota's Electrical Engineering and Computer Science departments (Minneapolis) in devising an automated



Plots of CPU time against circuit size show that the Adept timing algorithm from Silicon Design Labs is orders of magnitude faster than the Spice and Simon circuit simulators for a wide range of CMOS counters. The dashed line shows where Spice could no longer simulate the circuit because of limitations of convergence and circuit size. An expanded-scale graph (on the right) is needed to plot the Adept algorithm. (The numbers 4 to 32 above the transistor axis indicate the size of the counter in bits.)

layout-synthesis procedure for a silicon compiler.

The new process serves as the layout and synthesis portion of the Yasc compiler developed by Control Data and the University of Iowa (Iowa City). Introduced at last year's Design Automation Conference, Yasc uses the initial behavioral description to synthesize a chip's physical layout.

PERMUTABLE STRUCTURE

Working similarly with the initial behavioral description, the new technique also generates functional cells with a permutable inner structure. The cells can be arranged in columns, with the chip's global properties determining their final inner structure. The result is a smaller chip with improved performance.

Physical design techniques must often balance a number of conflicting goals. Ideally, a design system should be fast, produce chips with high circuit density, and remain unaffected by any changes in the design's ground rules. A system should partition data into working files of manageable size and incorporate updates in the design without difficulty.

But the real world dictates tradeoffs. Gate arrays, for instance, have short design cycles and lend themselves to automated production; when designed flat, however, they present formidable problems in placement and wiring.A custom chip, on the other hand, has a high circuit density and accepts design updates in its individual macros, yet it is more vulnerable to changes in design rules.

TOP-DOWN DESIGNS

To combine the best features of gate arrays and custom chips, researchers at IBM Corp.'s Thomas J. Watson Research Center (Yorktown Heights, N.Y.) have come up with a top-down physical design system. Called Vanguard, it routes the interconnections through porous macro designs. By combining the advantages of gate-array and custom design techniques, Vanguard produces high-density chips as well as standard chip images.

With each level of physical hierarchy imposing constraints on the levels beneath it, the chip's I/O locations influence its floorplan, which guides the intermacro nets. The nets are in turn routed through rather than around the intervening porous macros, using areas created specially for the wires. The procedure works best when there are considerably fewer connections between macros than there are connections within each macro.

L-Sim is 1000 times faster than Spice and 136 times faster than Simon in simulating a 24-bit counter.

Vanguard partitions the chip physically along the boundaries of its macros. Besides macro circuitry and internal macro wires, each subchip contains all global connections and portions of connections for the chip as a whole. Partitioning means that regardless of the chip's size and complexity, placement and routing programs have to deal only with the data associated with each separate macro, in manageable amounts.

SLASHING THE TIME

Silicon compilers promise to slash the time taken to transform a design concept into an actual piece of silicon. Doing so would intensify the need to evaluate a circuit's performance accurately, and simulation, already a highly CPU-intensive process, would become even more of a bottleneck.

A mixed-mode simulator, which Silicon Design Labs (Liberty Corner, N.J.) calls L-Simulator, or Lsim, combines behavioral timing, switch-level, and circuit-level simulators. The last of the three simulators is based on the Adept timing algorithm (for "automatic dynamic electrical partitioning of transistors"). The three simulation algorithms together form a consistent, interactive MOS simulator, with Stafan fault simulation at the transistor level to grade the test vectors.

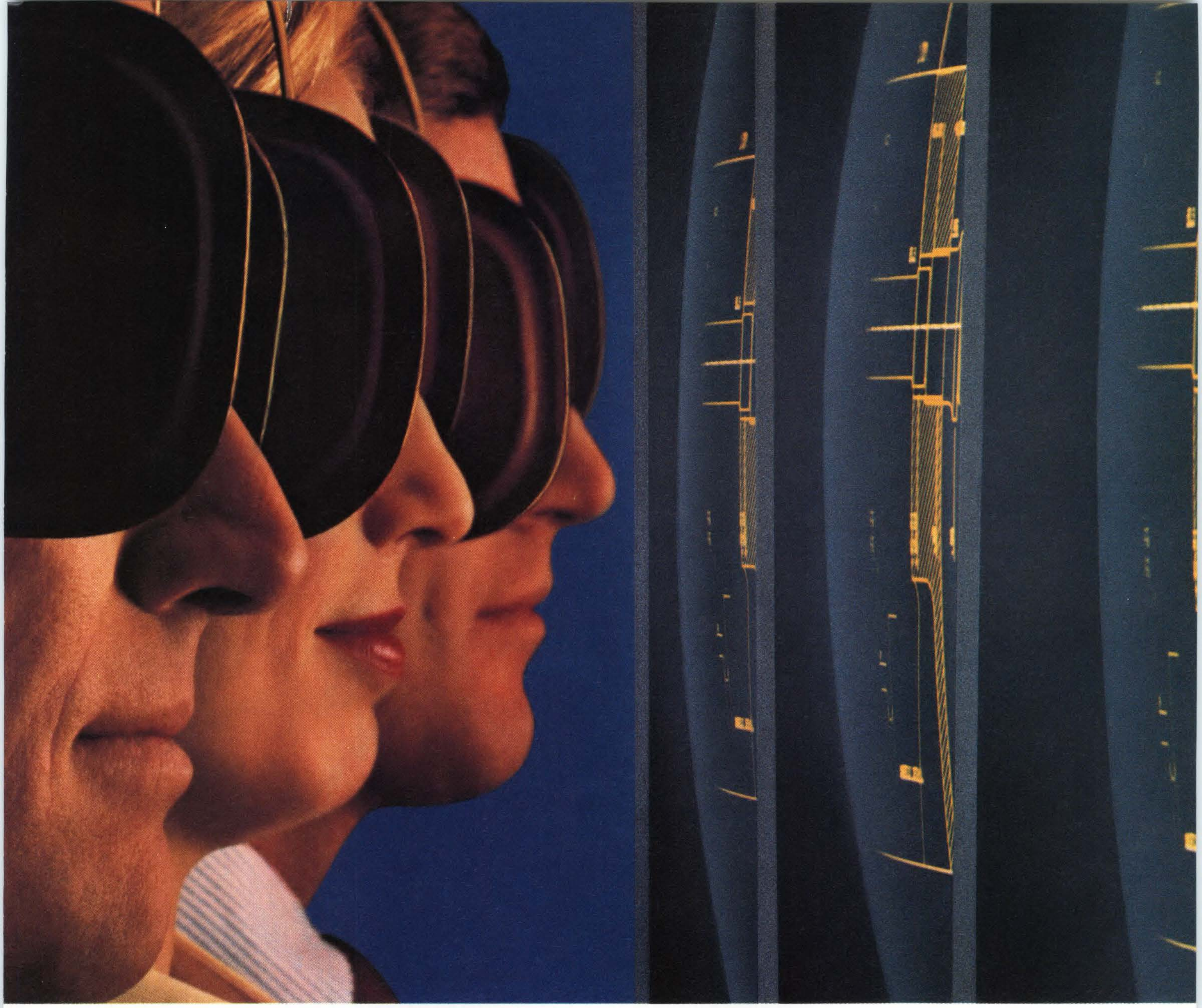
The Adept algorithm yields circuit-simulation results comparable to those of Spice. Based on selective trace simulation, it interfaces naturally with the switch and behavioral simulation levels without special synchronization blocks.

Because of its selectivity, the algorithm simulates large circuits easily, without Spice's large CPU and memory requirements. Silicon Design built and simulated several versions of a CMOS counter, using Spice, Simon, and Adept (see the figure p. 37). For a 24-bit counter the Adept algorithm proved 1000 times faster than Spice and 136 times faster than Simon.

The resulting simulation waveforms were identical, but the Adept algorithm is so much faster than the other two that it can be viewed only with an expanded time scale. The algorithm CPU time grows linearly with respect to nodal activity—in other words, less than linearly with respect to circuit sizes.□

Be sure to see Electronic Design's Professional Opportunities Section.

It starts on page 180.



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CIRCLE 25

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TC15G014	1400	92	3	2.5	5.0
TC15G022	2200	114	3	2.5	5.0
TC15G032	3200	138	3	2.5	5.0
TC15G042	4200	156	3	2.5	5.0
TC15G060	6000	180	3	2.5	5.0
TC17G005	540	44 48	2	1.5	3.0
TC17G008	880	52 68	2	1.5	3.0
TC17G014	1400	68 86	2	1.5	3.0
TC17G022	2200	82 106	2	1.5	3.0
TC17G032	3200	98 128	2	1.5	3.0
TC17G042	4200	118 150	2	1.5	3.0
TC17G060	6000	146 188	2	1.5	3.0
TC17G080	8000	174 222	2	1.5	3.0
TC17G100	10000	180 232	2	1.5	3.0

NOTES:
[1] For a 2 input NAND gate having a fan out of 2 and 2mm of metal interconnect.
[2] At 70°C and Vdd = 5v ± 5%

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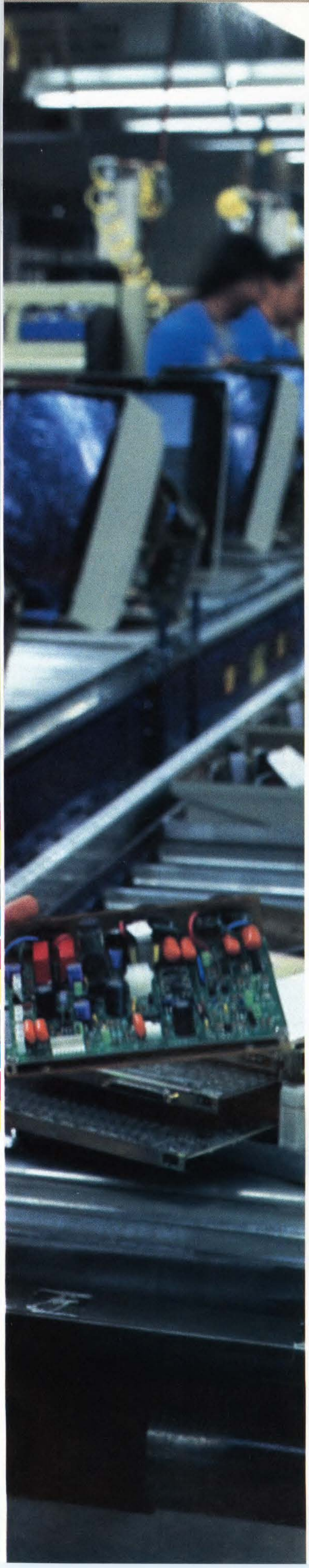
CIRCLE 26



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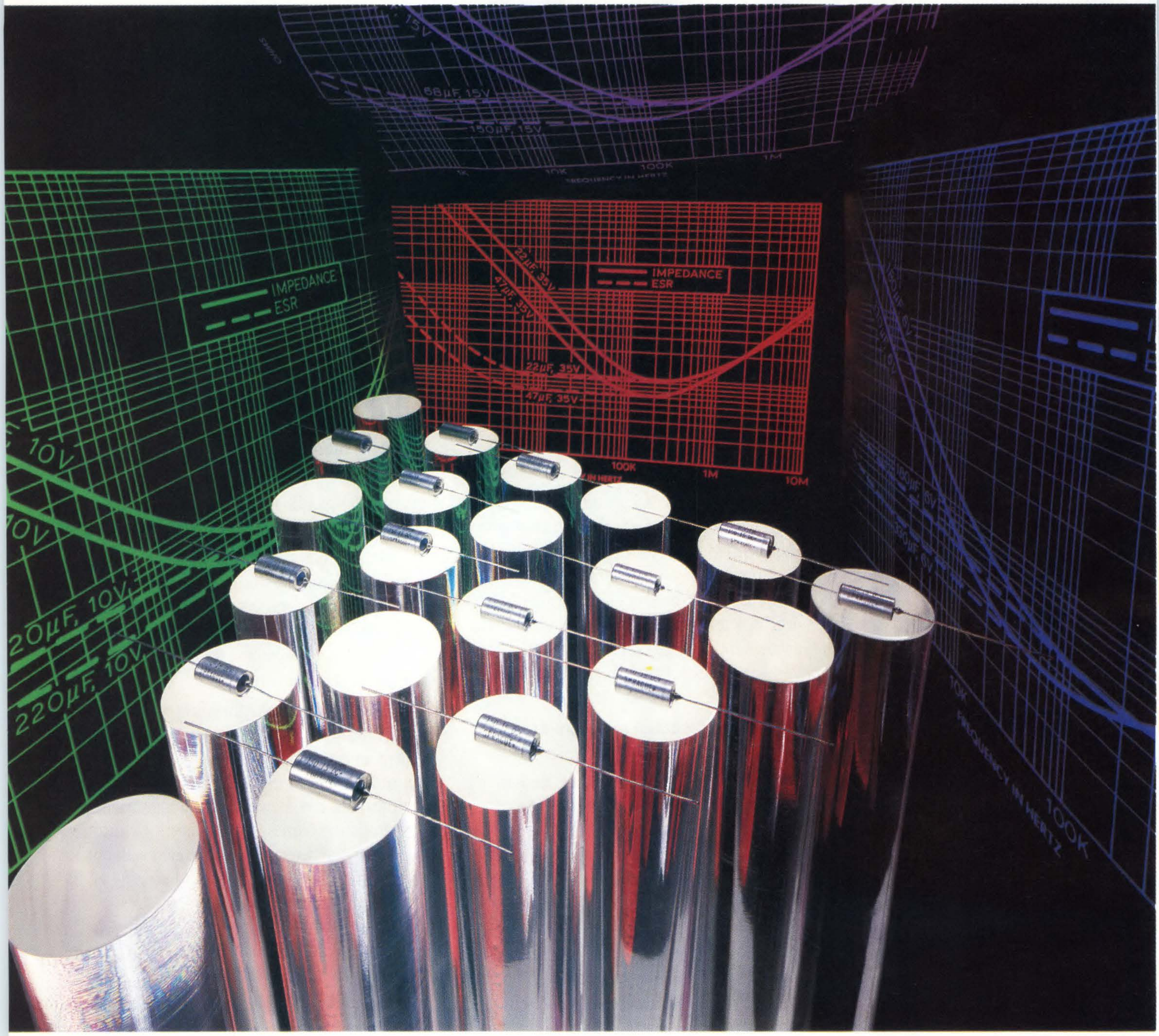

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CIRCLE 28

EXCLUSIVE INTERVIEW

EEs need CAE flexibility, not more horsepower

Jan W. Takke

Jan W. Takke is manager of the computer-aided systems and services support group at NV Philips in Eindhoven, The Netherlands. He has more than 20 years of experience at Philips. He received a degree in electrical engineering from The College of Advanced Technology at Arnhem, The Netherlands.

The sophistication of a CAE system for electronics design should be measured not by the number of standard-cell libraries available nor by whether the processor produces three-dimensional graphics in real time. Instead, suggests Jan W. Takke, manager of the computer-aided systems and services support group at N.V. Philips, a CAE system should provide continuity—from the initial design to the final product. The system that an engineer uses to describe a circuit in a schematic drawing, he explains, must be flexible enough to place parts on a pc board *and* to deliver the solder masks and drilling tapes for the board.

To integrate all of that information, Philips as well as other European manufacturers are putting many of their CAE projects on mainframe or minicomputer systems. Opting for CAE systems based on IBM, Digital Equipment or Computervision hardware, Takke insists, means choosing "flexibility over performance." Rather than buying a new high-performance workstation or CAE package that may be incompatible with what a company already owns, Takke and others are resisting the CAE horsepower race in favor of getting finished products out the door with more limited systems.

Consider the CAE data-base system Philips uses to design its popular compact audio disks. The system attempts to vertically integrate an entire consumer product line—from conception to final production runs. Besides containing electrical information like the schematic or circuit layout, the data base must hold mechanical assembly drawings and sketches of how the finished product will look. For example, pc boards in Philips products often are oddly shaped to ensure a compact fit with rotating parts, like motors, and also to avoid rfi or other signal crosstalk.

Furthermore, since dozens of designers around the world can work on one project, they must be able to access the same data base for schematic drawings, product specifications, simulation data, physical layout, and a variety of manufacturing process constraints.

Many CAE systems, Takke points out, deliver high performance for one or two applications, such as schematic entry and layout. But he contends they do not solve the real CAE challenge: mixing mechanical and electrical engineering tasks with mainframe database management and project tracking (see the figure).

Even with a migration to a mainframe-based system, Philips is a long way from CAE nirvana. The software is tailored to analog board design and to Philips' manufacturing design rules for trace widths and solder masks restraint. Even so, a lot of data remains outside of the system.

"No CAE system," Takke stresses, "is a turnkey system."

Now, Philips' designers must manually identify ground planes, shields, and high-frequency transmission lines for the analog boards. "And since Philips also manufactures its boards in-house," Takke adds, "CAE system users must

Stephan Ohr

constantly check manuals and guidebooks to be sure that the software is consistent with the company's board manufacturing processes."

In fact, Philips suspects that the time spent hunting through books may mean CAE systems offer little time savings over hand-drawn pc board layouts. It will be years before the board rules are on-line with the layout editor.

To maintain the drive toward continuity, Philips wants to control the proliferation of incompatible hardware and software. There is a limit to the variety of systems that a company will buy, Takke emphasizes. "Every new equipment purchase has the potential of creating a wall rather than enhancing communication."

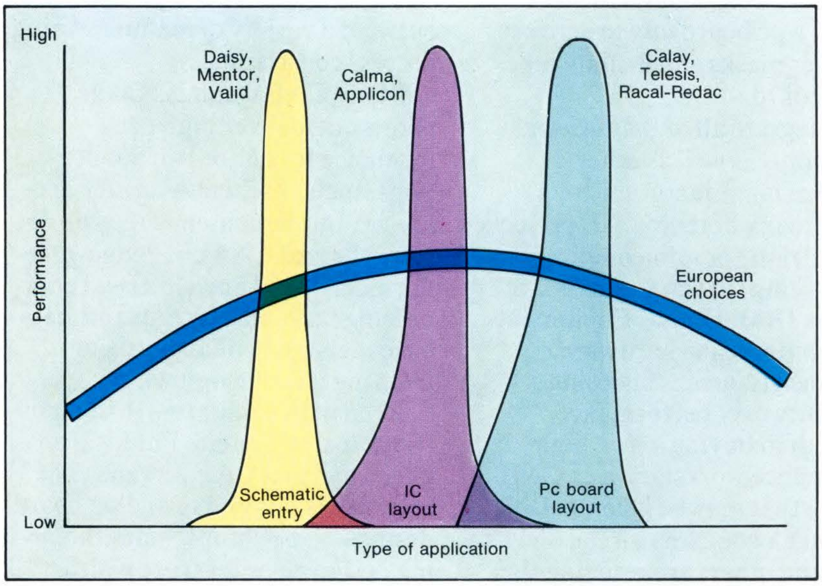
Does the Philips policy sound familiar? For one, General Motors Corp. will only buy hardware that meets the Manufacturing Automation Protocol (MAP). Philips is issuing a similar edict when it comes to computational resources for CAE applications. But Takke believes that the approach is not a catchall solution. "MAP and its companion Technical Office Protocol will aid communication between systems," he states. However, they're a long way from delivering the common data-base language and commands that are critical for a real CAE system.

Every purchase has the potential of creating a wall rather than enhancing communication.

Takke is well aware that managerial edicts are often criticized as stifling to the creative process. "Any CAE, CAD, or CAM system," he concedes, "may limit a designer's creativity if it is standardized for more rapid product turnaround." However, he envisions a compromise system that he calls "innomation." The system would furnish a workable balance between a designer's innovative spirit and an organization's automation needs and goals.

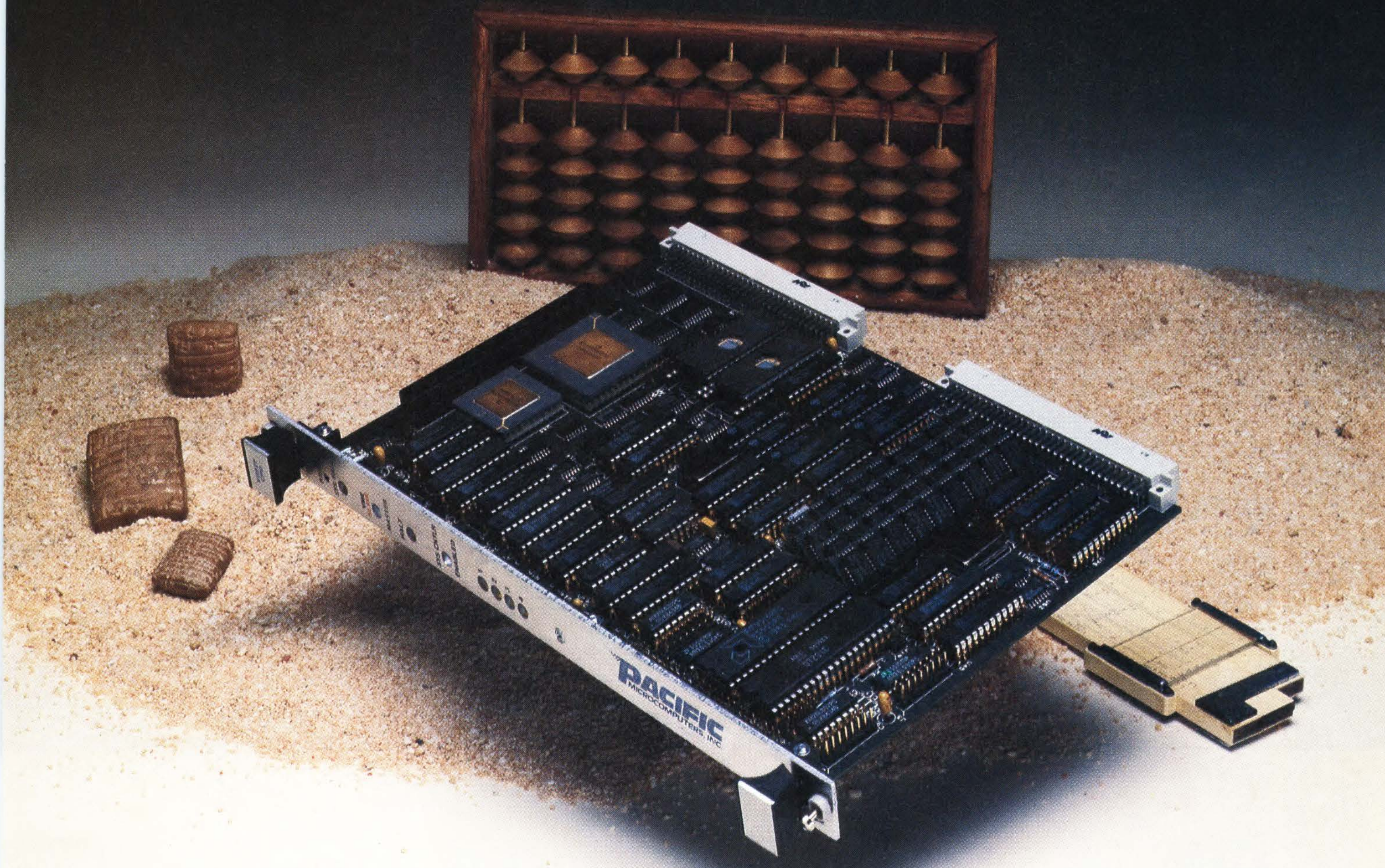
To illustrate, the needs of the designer and the organization can be met by a CAE system incorporating the ubiquitous IBM PC personal computer along with a mainframe or minicomputer. Philips, in fact, is exploring the use of personal computers for assorted drafting applications.

Of course, linking IBM PCs to a mainframe economically in a real-time network is easier said than done. Philips' efforts revolve around IBM PC ATs using microcomputer versions of Computervision's minicomputer software. The approach follows Takke's principle of limiting variety and maintaining continuity throughout the design process. □



When it comes to CAE hardware and software, Philips, as well as a number of other European companies, is choosing compatibility and flexibility over performance. Rather than selecting a more powerful product for any one application from a relatively focused supplier, they frequently compromise by buying a broad-based but lower-performance system.

Ingenuity: taking a good idea and making it better.



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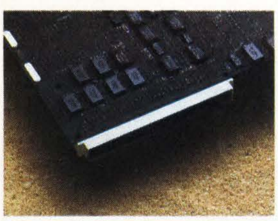
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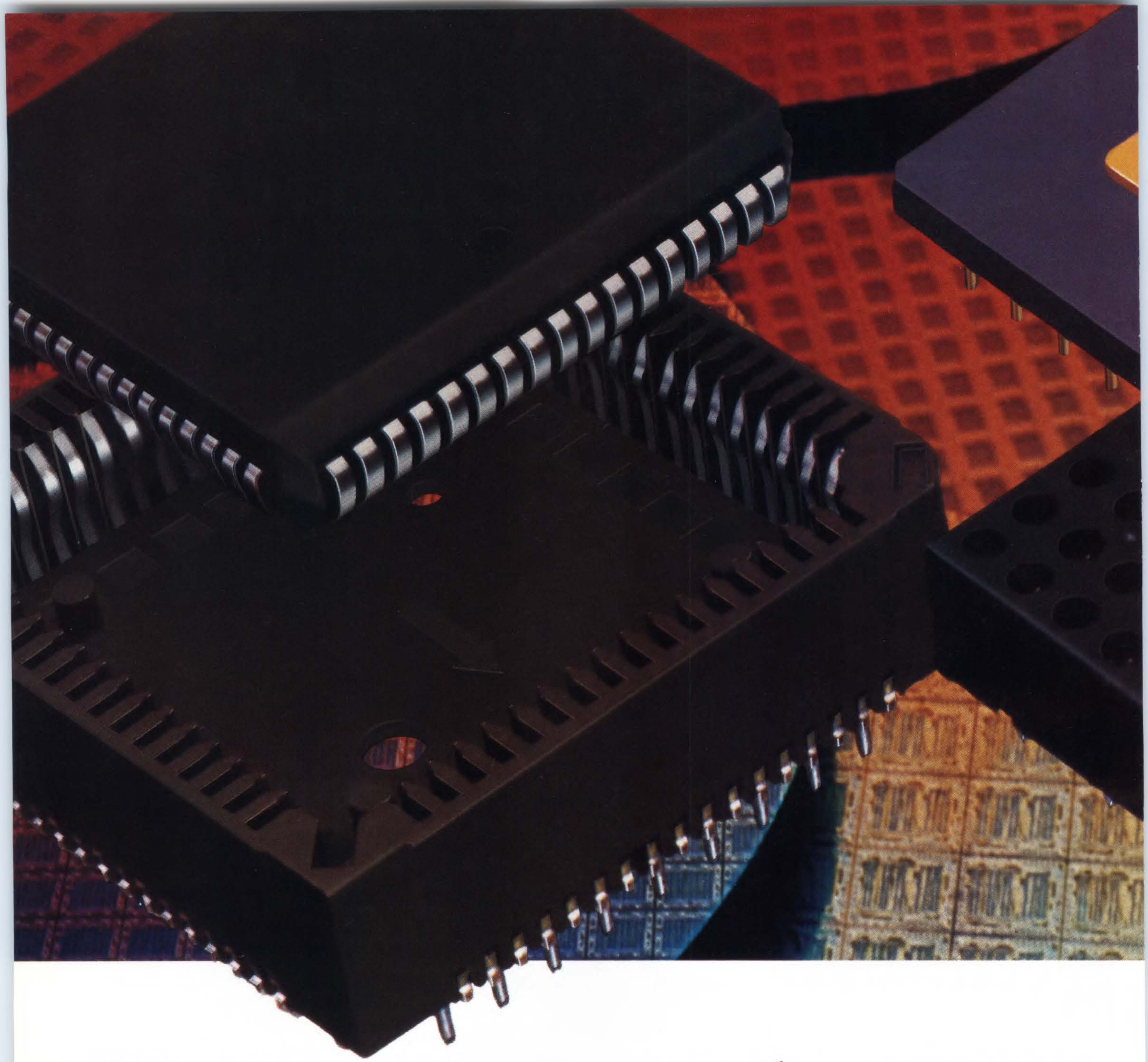
CIRCLE 29



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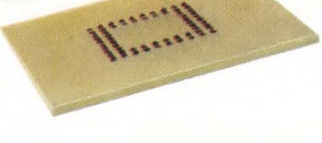

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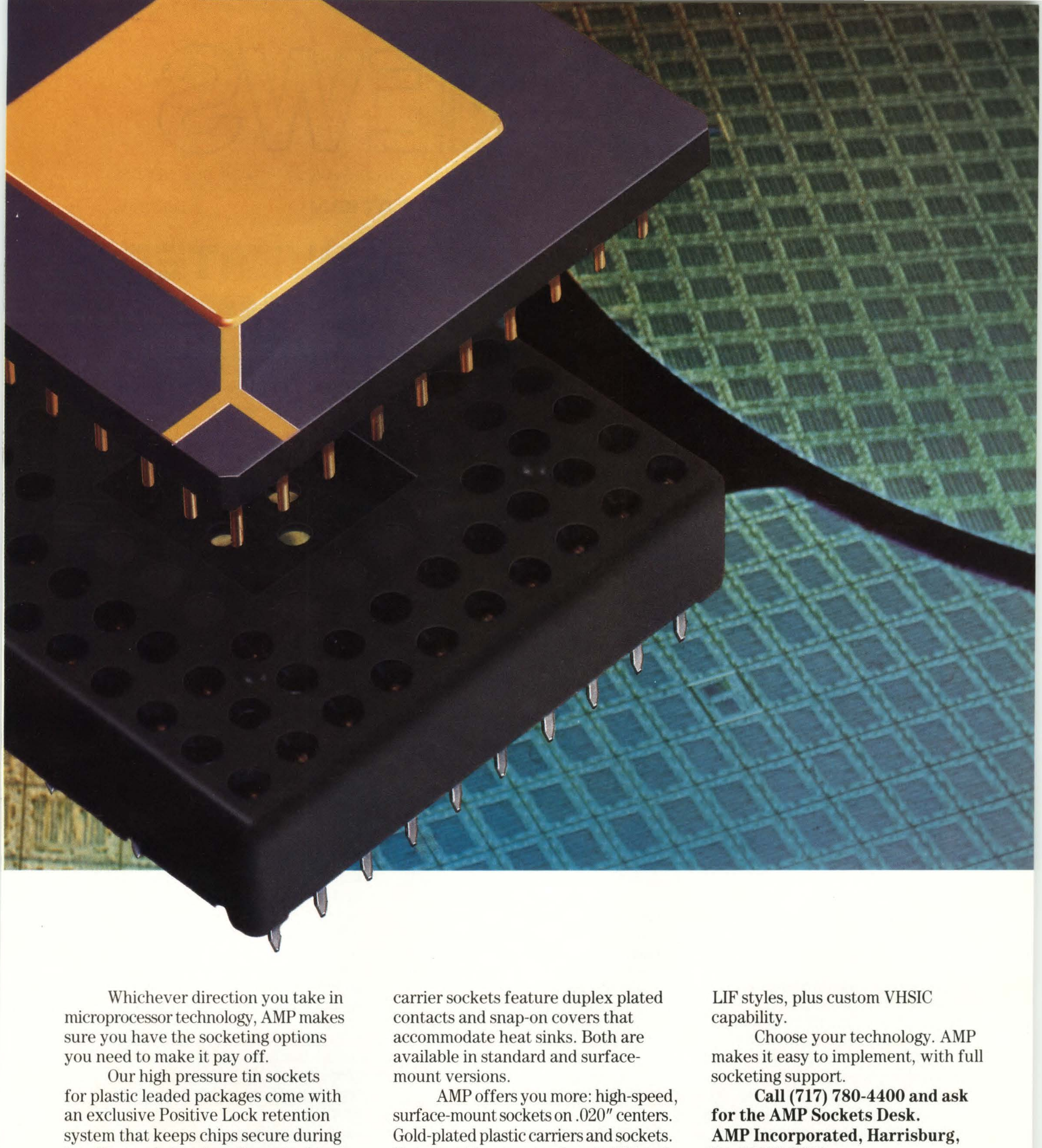

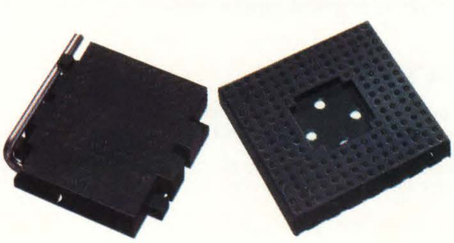

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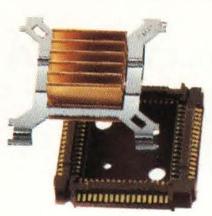
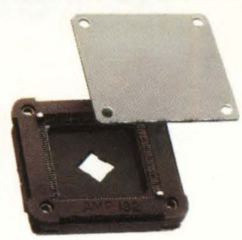


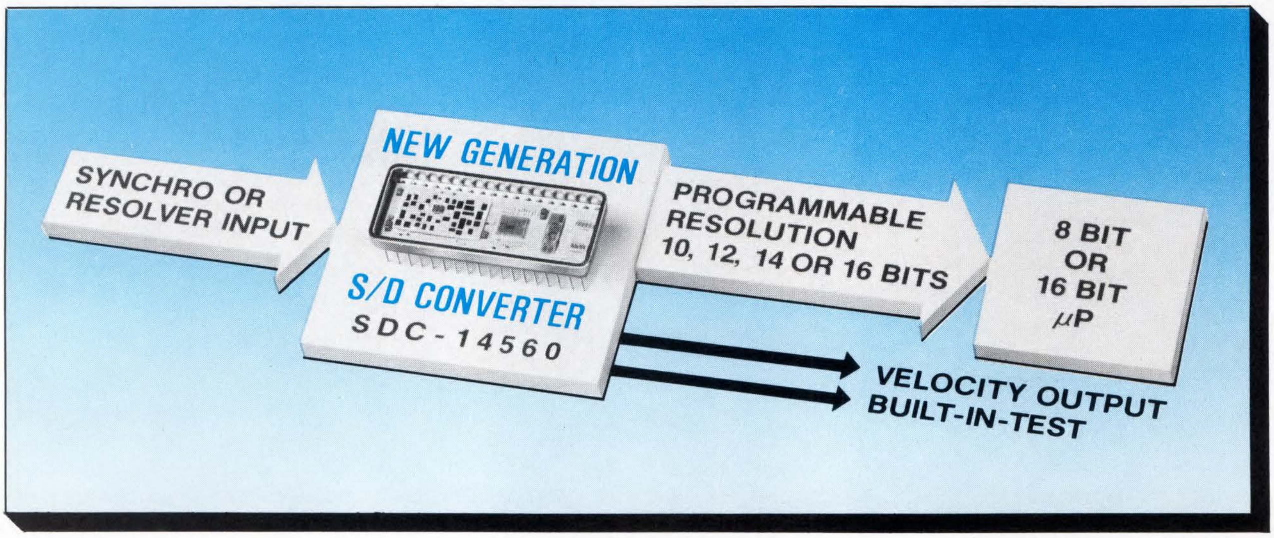


DDC NEWS

ABOUT SYNCHRO-CONVERSION • HIGH-SPEED, HIGH ACCURACY D/A & A/D CONVERSION • DATA BUS DEVICES

PUBLISHED BY **ILC DATA DEVICE CORPORATION** JUNE 1986

MILITARY SYNCHRO CONVERTER OFFERS DYNAMIC PROGRAMMING



The SDC-14560 series S/D converters offer programmable resolution of 10, 12, 14, or 16 bits, tachometer-like high quality velocity output and accuracy to 1.3 arc minutes. In addition, a Built-In-Test (BIT), CT mode operation, transparent latch, and three-state output in two bytes are standard features.

The SDC-14560 was configured to provide new capabilities to system designers. Programmable resolution allows both high speed position tracking and precise positioning with one converter. Where speed is essential, 10 bit resolution allows the highest tracking rate of 160rps. Conversely, when exact positioning is required, 16 bit resolution can be dynamically selected.

Velocity output (VEL) from the SDC-14560 is a ground based voltage of 0 to ±10VDC at the highest tracking rate for each resolution. VEL is positive for an increasing angle. Through the use of this highly characterized signal, the electro-mechanical tachometer may be eliminated from the system. The benefit is savings in system size, weight and cost.

All SDC-14560 converters provide Built-In-Test (BIT), a transparent latch and three-state output in two bytes. The BIT circuit detects over-velocity, out-of-null circuit conditions, and most converter or input failures. The three-state, two byte output and transparent latch provide for easy computer interface and continuous angle tracking while an inhibit is applied during data transfers.

Two input options are included in the SDC-14560 series: synchro or resolver. Models are offered with broadband frequency ranges of 360 to 1kHz, or 47 to 1kHz.

The SDC-14560 is a Monobrid® design which incorporates a custom LSI chip in its circuitry. Use of the LSI chip results in fewer parts, thereby increasing the reliability. The converters are packaged in a compact 36-pin DDIP measuring 1.9 x 0.78 x 0.21 inches and weigh 0.7 oz. Power requirements are ±15VDC and +5VDC supplies. Two operating temperature ranges are available: 0°C to +70°C and −55°C to +125°C.

The SDC-14560 series is designed for use in modern high performance high reliability commercial and military motion control systems. All models are available with MIL-STD-883 processing as a standard option. Some typical applications include radar, navigation and fire control systems, flight instrumentation and flight trainers or simulators.

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ELECTRONIC DESIGN EXCLUSIVE

4-Mbit/s transceiver works over 3500 ft

Aimed at point-to-point twisted-pair links, an analog IC's digital adaptive-equalization circuits give it a 40-dB dynamic range.

BY ROGER ALLAN

Transmitting data over twisted-pair wiring usually means trading off data rate against distance. An increase in either one seriously degrades a data signal's quality, as intersymbol interference rises and signal-to-noise ratio drops. Even the best IC transceivers operate at no more than 1 Mbit/s over some 5000 to 6000 ft. At four times the speed, the maximum distance shrinks to a few hundred feet.

One way out is to add circuitry that compensates for line abnormalities and data rate problems. But the extra components take up extra power and extra space and are likely to decrease reliability. A single-chip, full-duplex transceiver about to appear promises a far better solution.

The CSC82200 from Crystal Semiconductor operates at a data rate of 2.35 to 4 Mbits/s across up to 3500 ft of 22-gauge shielded twisted-pair wiring. Over unshielded 24-gauge twisted-pair wires the maximum distance falls to 3000 ft. The chip's bit error rate is less than 10^{-9}, against the 10^{-6} for T1 links and voice-grade modem lines. Moreover, for short packet bursts of under 16 kbits, it stands better than a 95% chance of error-free transmission for a given second. What's more, its external needs amount only to a pair of isolation transformers, an ac coupling capacitor, and a crystal.

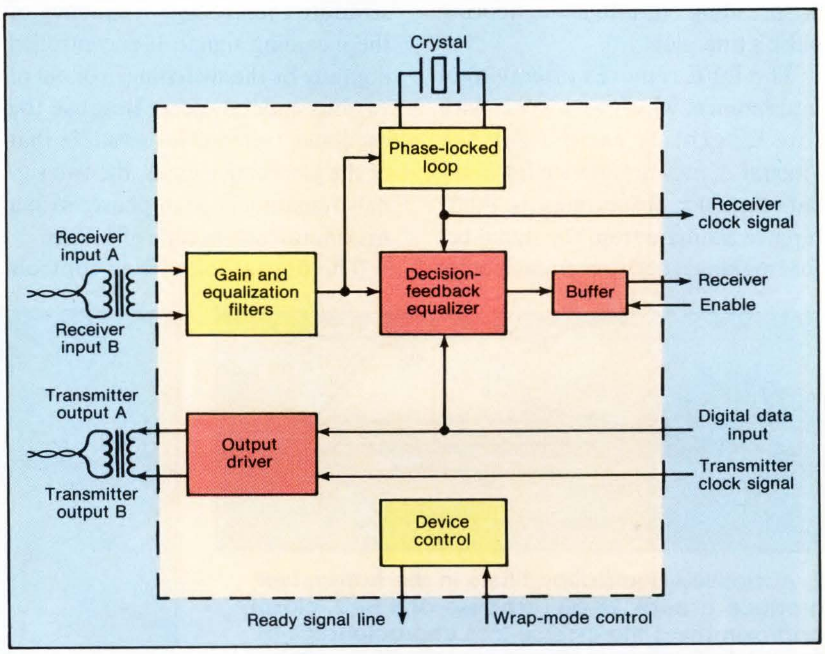
The 24-pin-DIP device is designed with a 3-μm CMOS process and operates from a single 5-V supply. Its digital inputs and outputs are both CMOS- and TTL-compatible, and it supports differential Manchester encoding.

The chip gains its speed and long-distance performance by adapting to line losses over a wide dynamic range. To do so, it relies on intelligent digital circuitry that supplements the analog parts.

The CSC82200 can be used in the middle of a full-duplex link as a full repeater or on one end of a full-duplex point-to-point link. Among such links are local-area networks; serial buses for computers and controllers, lines between high speed modems, and desktop computers, or among CAD/CAM and CAE workstations and their peripherals.

In either configuration—mid-link or link-end—the chip performs the functions of receiver-signal equalization, data and clock recovery, asynchronous data transmission, and fault diagnosis. It has a gain-and-equalization filter, a fully digital decision-feedback equalizer (DFE), a phase-locked loop, and an output driver (Fig. 1).

The CSC82200 provides adaptive equalization, data recovery, and low-jitter clock recovery. A transformer couples the distorted and attenuated signal into front-end equalization filters—made up of transconductance amplifiers and capacitors—that compensate for line losses during the transmis-



1. A pair of isolation transformers, an ac coupling capacitor, and a crystal are all the external components needed by a monolithic 4-Mbit/s transceiver that works over 3500 ft of twisted-pair lines. The analog device includes intelligent digital circuitry that compensates for transmission-line losses, suppresses interference signals, and ensures clock signal recovery.

sion. Varying the transconductance of the amplifiers through biasing trains the active filters to a critical operating frequency controlled by a 4-MHz, ±200-ppm crystal oscillator. An automatic gain control loop further checks the incoming signal's gain and shape.

The adaptive equalization process is controlled digitally, with eight different gain and shape settings that span a 0- to 40-dB dynamic range. The filter's response is at its best with a gain of about 28 dB at 4 MHz and at the maximum distance of 3500 ft (Fig. 2a). It rolls off rapidly on either side of the peak frequency, closely following the inverse-loss characteristics of a wire line.

Even with adaptive equalization, the fact that losses take place all along the line, coupled with the different characteristics of cable, means that some distortion will get past the filters. But the CSC82200 uses its DFE section to deal neatly with the intersymbol interference. Such interference is caused by energy from one data pulse smearing or spreading out into a neighboring pulse's time slot.

The DFE removes intersymbol interference, which gets worse with line length, by estimating the amount of an interference for every data time slot. It subtracts the interference estimate from the signal before making a decision on each pulse (Fig. 2b). The signals it receives from the adaptive equalizer have already been digitized by a 5-bit analog-to-digital converter. The DFE has separate elements for digital interference subtraction, updating, and storage.

MORE INTELLIGENCE

But the CSC82200's intelligence does not stop there. The DFE also deals with near-end cross talk caused by the proximity of the on-chip receiver and transmitter each other, or by coupling in wire bundles and PC-board conductors.

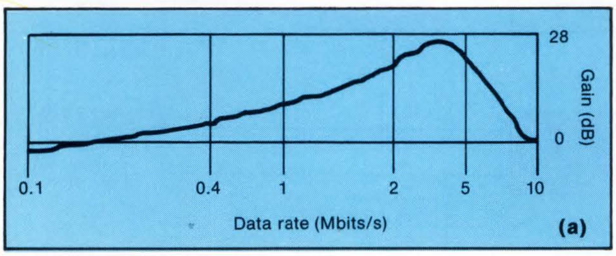
The DFE's near-end cross talk canceler, akin to an echo canceler, estimates the interference's amplitude and, as is done with the intersymbol interference, subtracts it from the signal. A very low bandwidth phase-locked loop with a Q of 2000 performs clock recovery, using a switched-load voltage-controlled crystal oscillator and a digital loop filter.

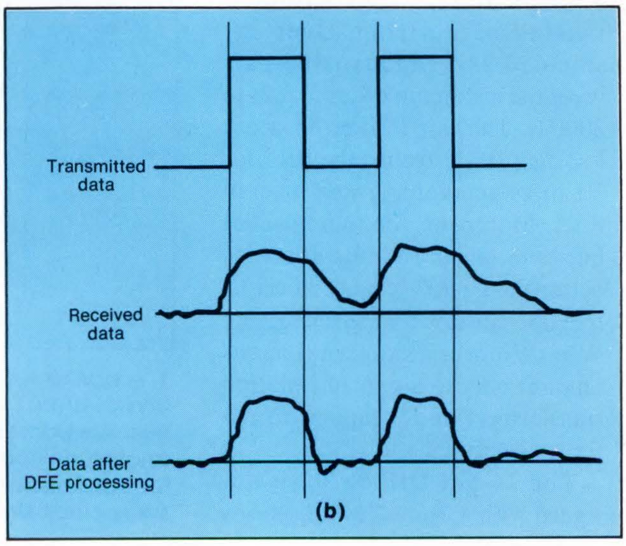
The oscillator operates at any one of four discrete frequencies that straddle the average frequency of the incoming signal. It is controlled digitally by the switching in or out of various capacitances. Because the oscillator frequencies straddle that of the incoming signals, the two signals remain locked in phase, with a maximum lock-in time of 1.5 ms.

The digital loop filter controls load switching by sampling a series of phases, calculating their average, and updating the oscillator frequency accordingly. The CSC82200's phase-locked loop's architecture also provides low-jitter clock recovery, holds accumulation of jitter to a negligible fraction of a symbol period, and keeps alignment errors to the minimum.

On the transmitter side, the chip drives a 150-Ω medium with a 3- to 4.5-V symmetrical signal that meets FCC standards for radiation from shielded twisted-pair wiring. An on-chip servo loop governs the transmitted signal's harmonic content by controlling the output waveform's rise and fall times. This slew-control circuitry keeps third, fifth, and seventh harmonics, for example, down to −10, −15, and −20 dB, respectively. The chip is designed to operate over the commercial temperature range of 0° to 70°C.□

> **Price and availability**
>
> **The CSC82200 transceiver IC will be available for sampling in the third quarter, priced at about $30 apiece in lots of 1000.**
>
> ***Crystal Semiconductor Corp., 2024 East Saint Elmo Rd., Austin, TX 78744; Bob Bridge, (512) 445-7222.***
>
> **CIRCLE 511**





2. Adaptive-equalization filters in the transceiver produce a peak 28-dB response at 4 MHz, closely approximating the inverse-loss characteristics of the twisted-pair wire. The sharp roll-off on either side of the 4-MHz peak keeps out-of-band unwanted signals to a minimum (a). A decision-feedback equalizer circuit removes intersymbol-interference and distortion (b).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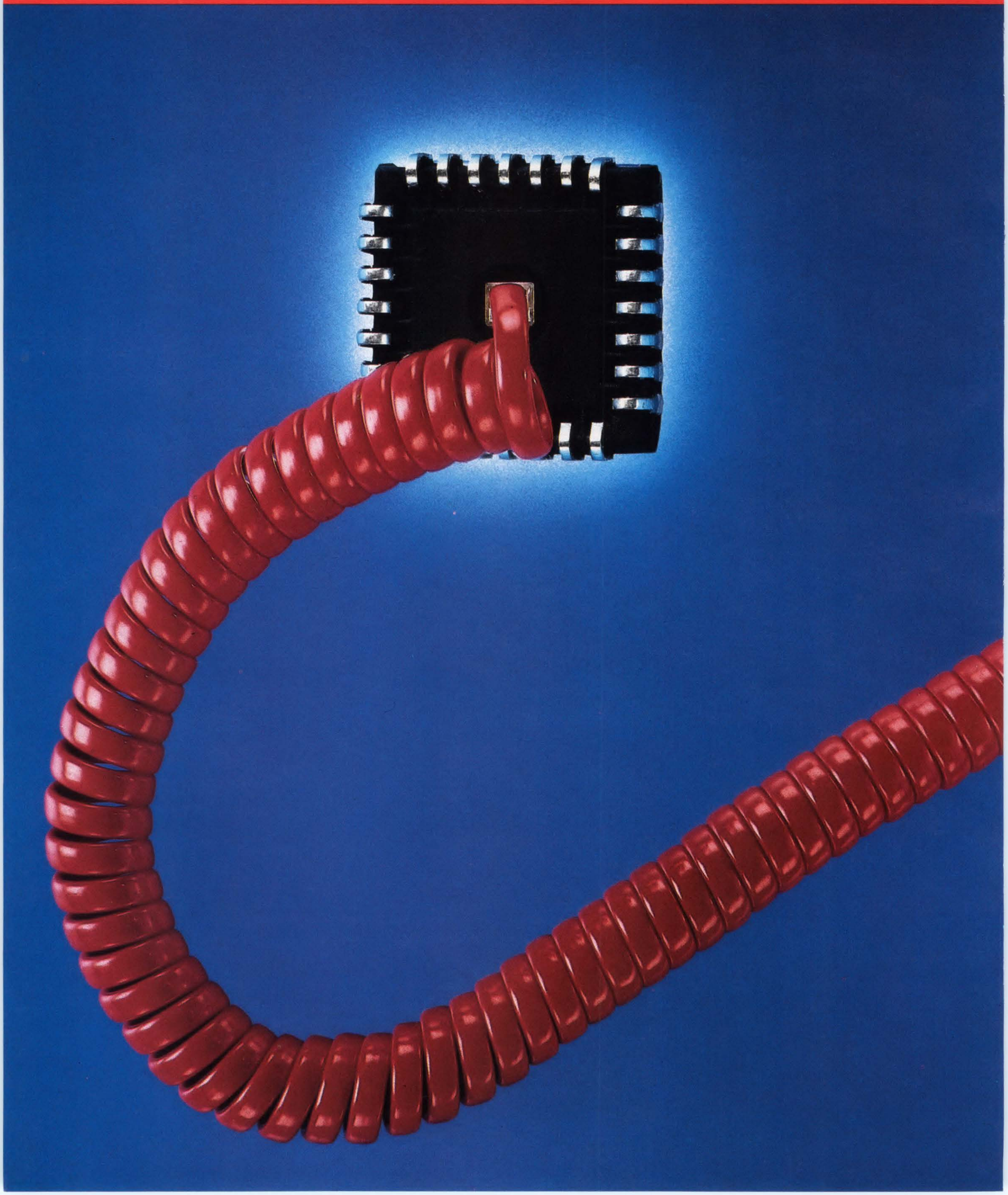

the single-chip CMOS modem.

Introducing the K212, a complete Bell 212A compatible, full duplex modem on a single chip. It provides all the functions on one chip that used to require up to five separate chips.

Developed by Silicon Systems Inc., this 1200/300 bps modem is alternate sourced by RCA.

Peripheral-on-a-chip.

To the system designer, the K212 looks like a peripheral. It includes full Bell 103 and 212A operating modes, a call progress monitor and a DTMF dialer.

Interface with popular micros.

The K212 interfaces directly with the 8048/8051 family of low-cost micros. Modem operation is controlled through the on-chip, 8-bit multiplexed address and data bus, or through an optional serial-command bus. The address-latch-enable control line simplifies address demultiplexing. Data communications go only through a separate serial port.

The on-chip DTMF enables the K212 to dial its own calls. And a call-progress detection feature allows it to change calling action in response to dial tones, busy signals or ring back. The dial-up phone line is connected through an external direct access arrangement interface (FCC approved).

And because it's CMOS, the K212 consumes very little power (less than 10mW in the idle mode and only 120mW in operation).

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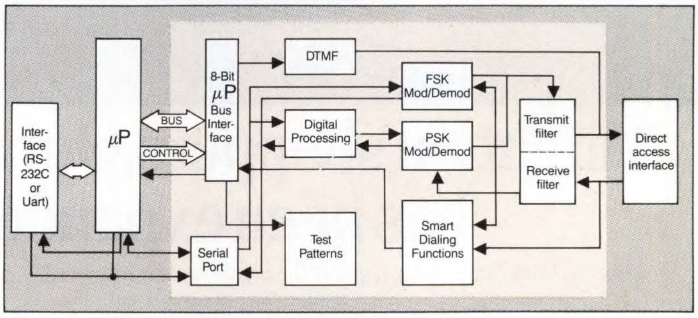

voice/data terminals, portables or battery operated systems. Ideal for free-standing products or systems; synchronous or asynchronous communications.

By eliminating multi-chip sets, you save board space, testing and time in bringing your product to market.

Futurespeak: the V.22 modem.

The K221 modem is coming soon, to support CCITT V.22 and V.21 communications protocol standards for Europe.

Availability: lines are open now.

You can get the K212 in 22-pin and 28-pin DIPs, or in quad packages. Samples are available for evaluation right now.

To order samples, write: RCA Solid State, Box 2900, Somerville, NJ 08876, or Silicon Systems, 14351 Myford Road, Tustin, CA 92680.

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CIRCLE 34

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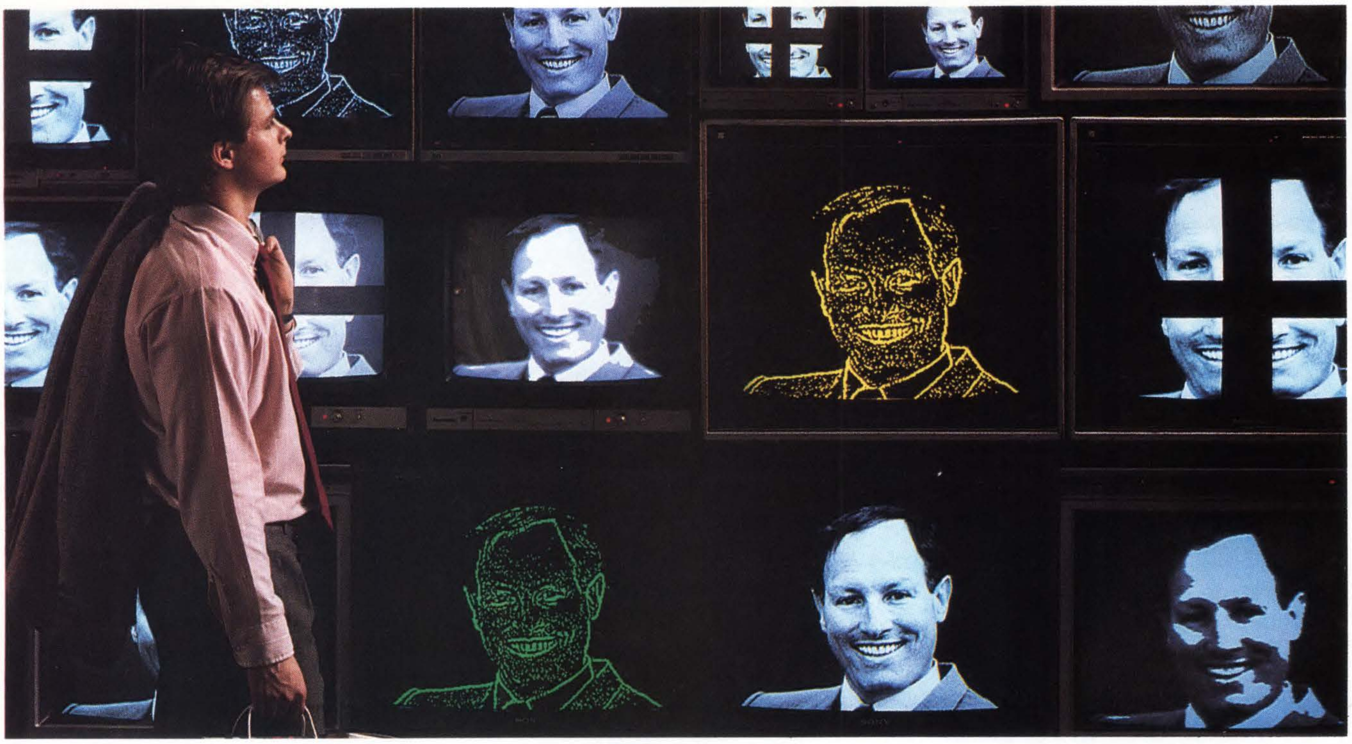

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DT2803 Low Cost Frame Grabber	IBM PC, PC XT, PC AT	256x256	64	Yes	Yes		8*	Yes	Yes	1 buffer 256x256x8 (64 Kbytes)					VIDEOLAB PC SEMPER	$1495
DT2851 + DT2858 High Resolution Frame Grabber and Auxiliary Frame Processor	IBM PC AT	512x512	256	↓	↓	Yes	8*	↓	↓	2 buffers, 512x512x8 each (512 Kbytes), and 1 buffer, 512x512x16 (512 Kbytes)	Yes	Yes	Yes	Yes	DT-IRIS	DT2851 $2995 DT2858 $1495
DT2603 Low Cost Frame Grabber	MicroVAX II	256x256	64	↓	↓		4	↓	↓	1 buffer 256x256x8 (64 Kbytes)					Coming Soon	$1895

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CIRCLE 35

VMEbus boards handle X.25-based packet-switched communications

As packet switching over the public data networks catches on, a growing number of boards is emerging to help make it happen.

BY MITCH BEEDIE

Paying only for the data you transmit, rather than for the length of time you connect to the line, is the attraction of packet-switching across the Public Data Networks (PDNs). Advocates of the scheme are counting on that attraction to make packet-switched PDNs the dominant wide-area network for data transfer of the 90s, surpassing even ISDN (the Integrated Services Digital Network), which attacks the problem from the voice side of information transfer (see "The Letters Game," p. 59).

Although packet switching is potentially much cheaper than circuit switching over leased analog lines, it has been slow to press its advantage. This is mainly because the major customers have been large companies, which are understandably reluctant to invest in unproven technology. But with an X.25-based Packet-Switching Network (PSN) now in place, transferring data internationally, things are starting to speed up.

Equipment from all of the major mainframe and minicomputer manufacturers already connects to packet-switching networks using their own (or third-party) X.25 links, and it is now being joined by VMEbus systems—in the main across dial-up telephone lines.

X.25 boards will therefore increasingly head up VMEbus systems, transferring data cheaply across public and private packet-switching networks. Some half-dozen companies have announced these boards, with each embodying a different idea of what the market wants and needs. Product offerings range from sophisticated, high-speed boards capable of transferring data at 10 Mbits/s over several kilometers, to slower, cheaper units that connect to public packet-switching networks.

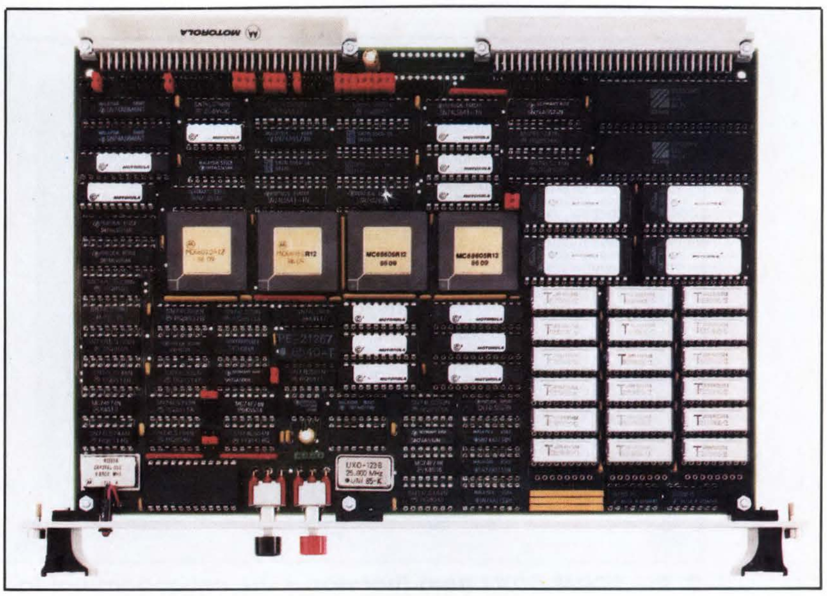
THE SPEED KING

When it comes to speed, the top VMEbus performer is undoubtedly the MVME 334 from Motorola Inc., which has two independent X.25 channels that each work at 10 Mbits/s—ten times faster than anything else on the market (Fig. 1).

To reach that speed, the 334 uses two MC68605 chips and a 68010 processor. Also, it is configured with 32 address lines, rather than the usual 24, so that it can access 4 Gbytes without being slowed down by address translation. The board's sheer speed makes it attractive for private exchanges.

Despite the blazing speed of the Motorola board, X.25 cannot compete with the efficient, high-performance protocols needed for closely-coupled computer systems. But it does ensure reliable data transfer, and therefore comes into its own when widely separated systems must be interconnected.

Geographically separated industrial or office sites that need data interchange—especially when there are common data bases to be updated—are natural applications for



1. Motorola's MVME334 zips through 10 Mbits/s; it owes much of its performance to two MC68605 XPC (X.25 protocol controller) chips that implement layer 2 of X.25.

X.25. For them, a cluster of serial channels does not come amiss, and the six or seven 1-Mbit/s multiprotocol links on the VME 7300 from Mizar Inc. will do nicely. Even this many serial channels leaves one or two 1-Mbit/s links free for X.25; normally a single X.25 link is enough, unless the board is to form part of some kind of switching station, in which case two are needed.

Like most other X.25 boards, the VME 7300 connects on level 1 of the X.25 protocol using either X.21 or X.21bis, with messages being buffered by dual-port RAM (in this case 128 kbytes), and VMEbus-to-X.25-board message transfer using a 68450 DMA controller. (The levels of X.25 correspond to those of the ISO's Open System Interface Model. Level 1 is the physical layer, which concerns voltage values, transmission rates, connector configurations, and so forth.)

When forwarding messages across the X.25 link, level 3 imposes flow control to prevent the links from becoming overloaded. (For X.25, level 3, the network layer, is the packet level, which sets up network connections.) A sender may only transmit a predefined number of packets (through a 'window') before it has to request the window to be opened for more packets. This number varies from board to board (see manufacturer's data at the end of the article), and is determined by the EPROM-based firmware. This firmware is held in EPROM (or may be downloaded at system startup) along with the other OSI layer-3 routines.

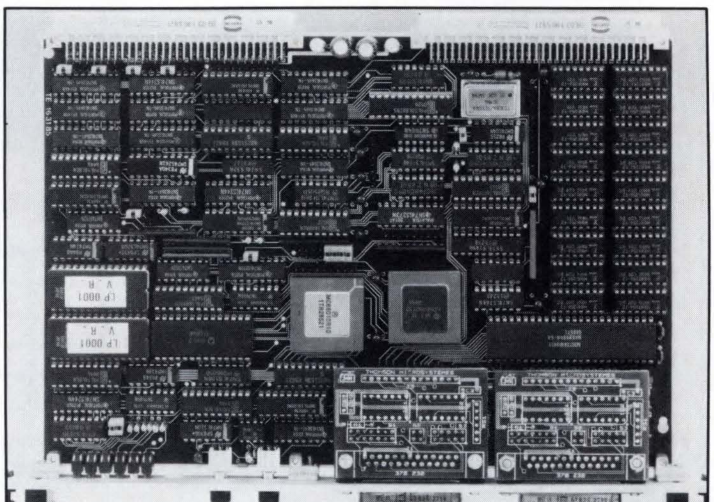
The OSI model aims to make the type of network in use invisible to the higher-layer software, thus allowing, for example, VMEbus systems to talk quite happily to mainframes and minicomputers. DEC computers will be brought into the fold across Reltek Data Inc.'s line of X.25 boards. This line includes boards for the VMEbus, as well as DEC's Q-bus and Unibus; later in the year it will link up to IBM PCs, again using X.25. The VMEbus board even adds a VAX/VMS driver to the Unix type that is universally available.

Reltek's X.CAL-VME board has a 68000 processor backed up by two WD2511 protocol controllers. This illustrates a current industry-wide trend: not only are peripheral boards increasing in intelligence to offload host processor boards, the processors on the peripheral boards are themselves being offloaded by increasingly intelligent, specialized peripheral chips. In this case, the 2511 controllers handle layer 2 of X.25; they detect any errors in data received, and request retransmissions where needed, interrupting the processor once the whole process is complete and error free data is safely in RAM. (Layer 2 makes the physical transmission medium invisible to the higher layers.)

TheWD2511 protocol controllers give Reltek's board two 1-Mbit/s channels. Although these rates (and above) are needed for LANs, they are somewhat of an overkill for actually transmitting data across a PDN, which is limited to some 48 or 64 kbits/s.

WHAT'S THE THROUGHPUT

Besides the data transfer rate, however, an important figure is the throughput. This is perhaps best measured in packets/s and depends largely, of course, on the packet length, although the maximum rate with a zero-byte packet is determined by software overheads. The Thomson Semiconducteurs' TSVME 540 and 541 boards (Fig. 2) for example—which have a maximum data transfer rate of 100 kbits/s—translate a data rate of 64 kbits/s into a maximum 300 packets/s for a zero-byte packet, but this falls to 170 packets/s for a 128-byte packet, and to 28 packets/s for a packet size of 1024 bytes.



2. The TSVME 540/1 from Thomson is the only board not to have a full X.21 link; instead two V.21bis links can connect the board to dial-up telephone lines.

These boards have as a main target controlling remote industrial VMEbus systems or transferring data between two medium-speed networks. For these applications a full X.25 link is not needed, and so the board has two V.21bis—that is, RS-232 or RS-422—links for connecting to dial-up telephone lines—currently the most common way of connecting to PDNs.

Thomson was in fact the first company to announce an X.25 board (ELECTRONIC DESIGN, July 11, 1985)—the current board is their second-generation product—and will also be the first with higher-layer software: layer 4 (the transport layer) should be available in the next month or so, and will be joined over the next few months from similar packages from other manufacturers.

A bunch of forward-looking software packages will soon be available for a board that was designed jointly by Heurikon Inc. and Morning Star Technologies Inc. One of these packages implements Teletex (high-speed telex), while another enables a terminal to emulate a Group-3 facsimile machine (both of these packages are planned for release by September). In addition, an X.400 message-handling system is scheduled for release soon after the final specification has been defined.

Like a couple of other companies, Heurikon/Morning Star uses software release X.25-80; although this does not have the streamlined international addressing (and other improvements) of the more recent X.25-84, many of their client companies are still working with it. And those who change over from one to the other can expect some inconsistencies between the two versions of the CCITT's standard. The X.25-84 version is expected to be ready in the next few months.

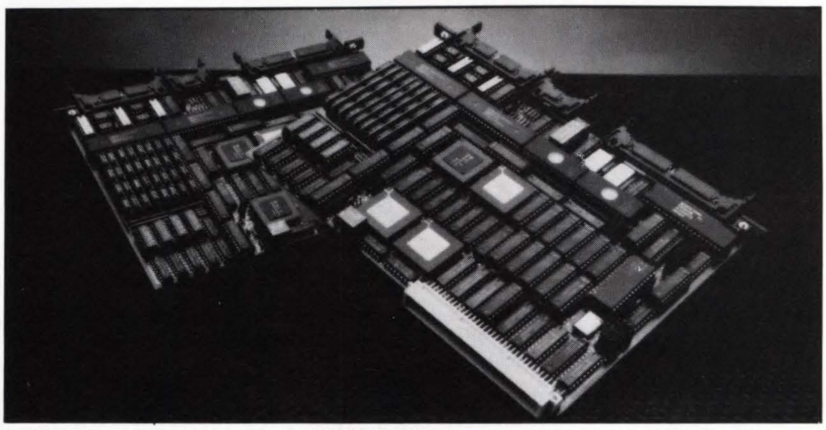
A concept central to both versions of X.25 is the concept of virtual circuits between terminals on the network. Although the standard allows for 4095 different virtual circuits, few of these need be implemented on a VMEbus board, since each virtual circuit will normally be dedicated to one user or task. A common figure is 32 or 64 channels; Heurikon/ Morning Star has 120.

The board itself (Fig. 3) has up to 1 Mbyte of dynamic RAM and up to two serial X.25 links running at 64 kbits/s. In a few months the company will increase that to 4 Mbytes of dynamic RAM, and four X.25 links—all running at 64 kbits/s.

But even lines that transfer data at 48 or 64 kbits/s are expensive. A cheaper alternative is to connect to a packet-switching network across dial-up telephone lines using X.21bis. Here, speed is not an issue, since dial-up lines are generally limited to 1200 or 2400 baud unless quadrature amplitude modulation is used to boost them to 9.6 kbits/s or more (ELECTRONIC DESIGN, April 17, 1986, p. 89).

The 19.2-kbit/s speed of Stollman's SICC board (Fig. 4) is therefore plenty for transmitting across X.21bis and through a PDN. The board has a 4-MHz Z80A, although a 68000-based version of the board that will work at up to 64 kbits/s is planned for later this year. Also in the pipeline at Stollman (and Heurikon/Morning Star) is SNA software that will allow the Unix-based VMEbus system to communicate with an IBM mainframe using the 3270 protocol.

Extending the reach of X.25 are PADs—Packet Assemblers and Disassemblers. Although X.25 was designed for packet-switching terminals, simple asynchronous terminals are not ignored, and can be at-



3. Heurikon/Morning Star's HK68/V10 board works at 64 kbits/s; it has a 68000 processor and a megabyte of dynamic RAM.

The letters game

Bad as the acronym situation is in the electronics industry as a whole, it is worse yet in the telecommunications segment, although not as bad as in the military. Public Data Networks (PDNs) are being set up alongside the familiar analog Public Switched Telephone Networks (PSTNs). Transmitting data over the PDNs is the subject of the CCITT's X.-series of recommendations, while transmitting data over the PSTNs is the subject of the V.-series. The ISDN (Integrated Services Digital Network) is the subject of the I.-series.

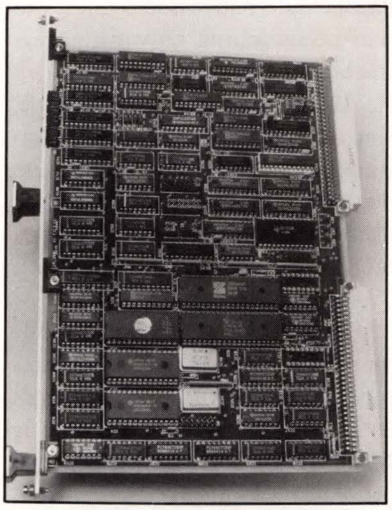
A Packet-Switching PDN (PSPDN) stands alongside Circuit-Switching PDNs (CSPDNs), of which there are only a few: the companies and authorities responsible for operating telecommunications systems have favored packet-switching networks.

In the UK, the PSPDN services are termed PSSs (for Packet Switch Stream). The International Pocket Switch Stream is the IPSS. In West Germany, the PSPDN is called Datex-p; in France, it is Transpac; in the USA, Telenet, Tymnet, and others: and in Canada, Datapac.

To add to the confusion, Teletex, the high-speed telex service, sounds a lot like Teletext, a scheme for displaying computer information on television sets. Systems similar to Teletext are also known as Videotex, Viewdata, Bildschirmtext, Viditel, Teletel, Telidon, Captains, Prestel, and others. Some are one-way broadcast systems; others are interactive and make use of telephone lines for transmission. All are intended to link homes and small businesses with central data bases.

tached using a PAD. This software, as its name suggests, assembles transmitted messages into packets for a terminal, and strips off the packet from received messages. It is currently being planned by a couple of manufacturers, but is only available right now on Stollman's board, and the one from Heurikon/Morning Star.

Although the number of X.25 boards on the market currently is rather small, many such boards are in the planning stage. Data Sud (Montpellier, France), for example, is working on a double-height Eurocard, half of which will hold the processor and VMEbus interface logic, while the other half holds the application-specific circuits (here, the X.25 circuits). The company will have a whole range of such circuits, including hard-disk controllers, serial-to-parallel interfaces, and a-d and d-a converters. This type of arrangement is in fact being taken up by a couple of VMEbus manufacturers; it aims to free a user from tangling with VMEbus specifications, while at the same time allowing him to use the same core of hardware and software for a wide range of applications.



4. The SICC board from Stollman has a 4-MHz Z80A, and uses 8-bit data transfers across the VMEbus. (All other boards use 16-bit data transfers.)

Plessey (Towcester, England) too has a board waiting for the X.25 software that is now in preparation, and Electronic Modular Systems GmbH (Neu-Isenburg, W. Germany) may base one on their CPU-2PB board, which has 512 kbytes of RAM and the ever-present 68450 DMAC.

Although a long way off yet, X.25's eventual promise is for user applications running on machines spread out all across the world to be able to communicate with each other as if they were all on the same machine—even though they may be running on different types of computers, in different languages, using different operating systems.

And there are more possibilities, with packet-switching networks in the future providing cable TV, videotex, teletex (high-speed telexes), facsimile, and message-handling systems. In fact, the eventual aim is to link packet-switching networks with the voice-based ISDN.□

Directory of X.25 board manufacturers

						X.25 Ports					Serial ports (multiprotocol)				
Company	Model	Processor	Maximum EEPROM (kbytes)	RAM (bytes)	DMA controller	Number	Data transfer rate (bits/s)	Throughput[2] (packets/s)	Maximum packet size (octets)	Number of virtual circuits	Number	Transmission rate (bits/s)	Cost[5] ($)	Availability (samples/production)	Circle
Heurikon Inc. 3201 Latham Dr. Madison, WI 53713 608-271-8700 telex: 469532 **Morning Star Tech. Inc.** 1760 Zollinger Rd., Columbus, OH 43221 614-451-1883 TWX: 5106003273	Horizon 240V	10-MHz 68000	128	512k or 1 M	68450	1 or 2	64k	180	1024	120	0 or 1	256k	4990	Now/now	**479**
Mizar Inc. 20 Yorkton Court St. Paul, MN 55117 612-224-8941 telex: 469542 **Mizar Inc. Ltd.** 100 White Hall Estate Glenrothes, Fife KY6 2RP, Scotland (+44) 592 771615	VME7300	8-MHz 68000	64	144k	68450	1 or 2	1 M	N.a.	N.a.	N.a.	6 or 7	1 M	4500[7]	August/ N.a.	**480**
Motorola Inc. Microsystems Marketing 2900 South Diablo Way Tempe, AZ 85282 602-438-3501 **Motorola GmbH** Abteilung Microsystem Taunusstrasse 51 8000 Munich 40 (+49) 89 356094 TWX: 522 199	MVME334	12.5-MHz 68010	256	2 M	63450	2	10 M	1000	1024	32	4[4]	1.5 M	2900[6]	Sept./ Nov.	**481**

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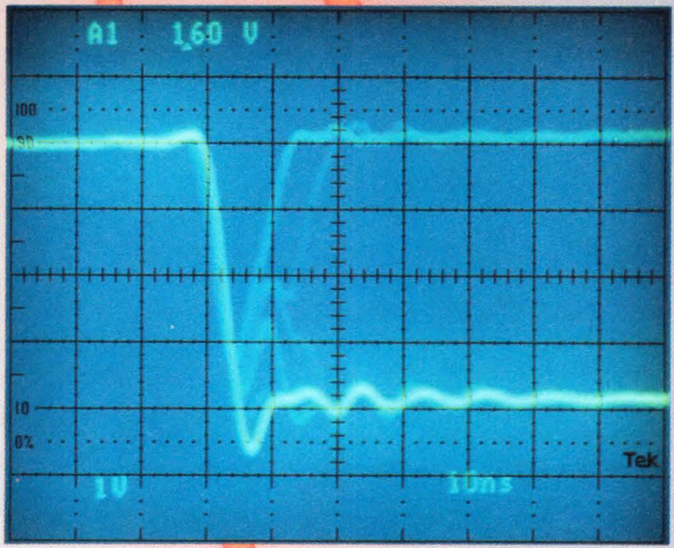

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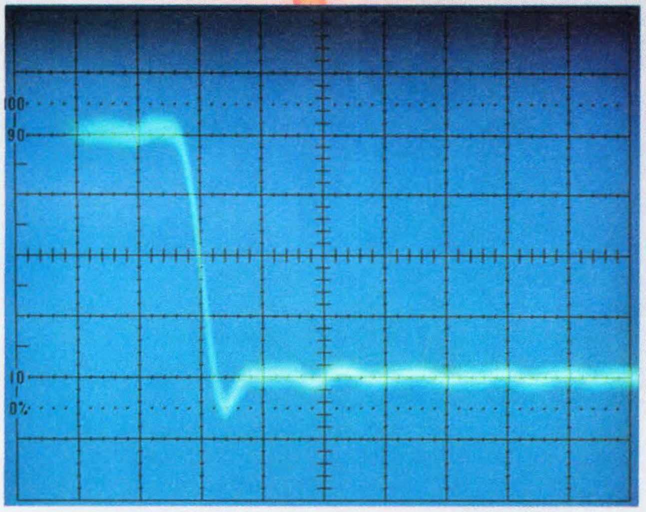

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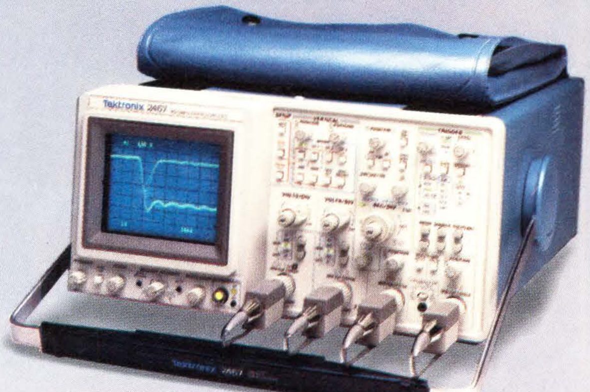

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CIRCLE 36

Directory of X.25 board manufacturers (cont'd.)

Company	Model	Processor	Maximum EEPROM (kbytes)	RAM (bytes)	DMA controller	X.25 Ports: Number	X.25 Ports: Data transfer rate (bits/s)	X.25 Ports: Throughput[2] (packets/s)	X.25 Ports: Maximum packet size (octets)	X.25 Ports: Number of virtual circuits	Serial ports (multiprotocol): Number	Serial ports (multiprotocol): Transmission rate (bits/s)	Cost[5] ($)	Availability (samples/production)	Circle
Reltek Data Inc. 44 Steacie Dr. Kanata, Ontario Canada K2K 2A9 613-592-2411	X.CAL-VME	10-MHz 68000	64	1 M	None[1]	1	1 M	750	4096	64	2	19.2k	4845	Now/ July	**482**
Stollmann GmbH Max-Brauer-Allee 81, D-2000 Hamburg 50, West Germany; (+49) 40 3890030	SICC	4-MHz Z80A	32	16k	None	1	19.2k	100	512	63[3]	0	—	3650	Sept./ Nov.	**483**
Thomson Semiconductors VSI 761 E. University Mesa, AZ 85203 602-962-9579 **Thomson Semiconducteurs** 173 bd Haussmann 75379 Paris Cedex 08 France (+33) 1 561 96 00 Telex: TCSF 204780F	TSVME540/1	10-MHz 68010	128	128k or 512k	68450	1 or 2	100k	170	1024	64	0 or 1	1 M	2700/ 2900	Now/now	**484**

Notes: [1] Uses instead two 512-byte bidirectional FIFOs.
[2] With a 128-byte packet.
[3] 12 can be active simultaneously.
[4] Software not yet implemented.
(N.a.)—Not available
[5] Single-quantity; includes board, driver, and X.25 software.
[6] Projected price.
[7] Board only, not including Unix driver.

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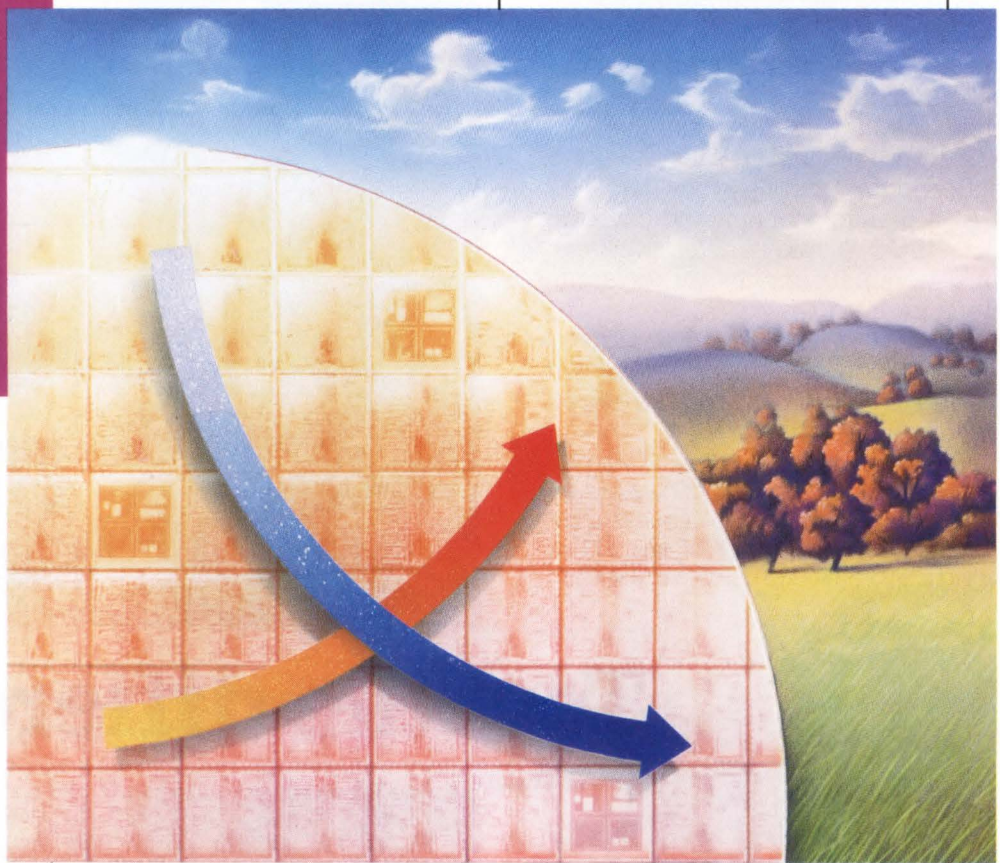

Ride down the experience/cost curve with our VLSI devices while we push them up the function integration curve.

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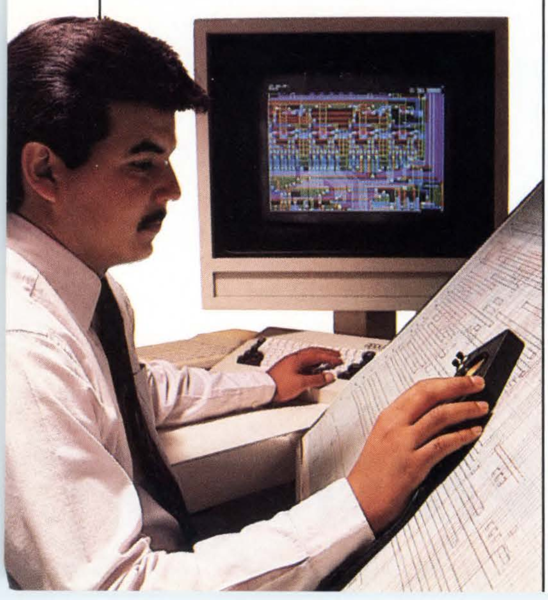

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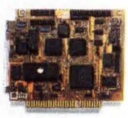
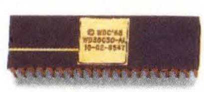


WD1002A-WX1 4.95" x 3.85" half-slot IBM XT compatible controller for up to two ST506 drives.



WD30C30/31 CMOS ST506/RLL Hard disk controllers with on-chip ECC and analog data separator.

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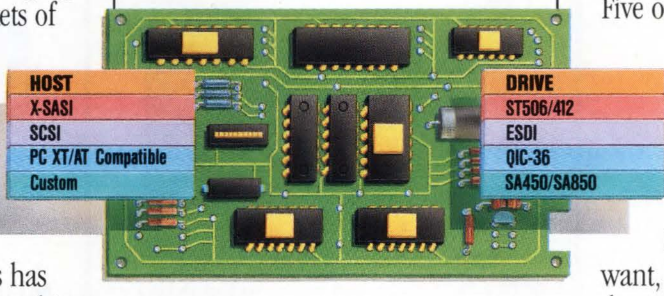

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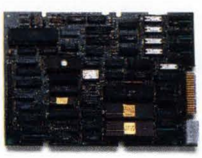

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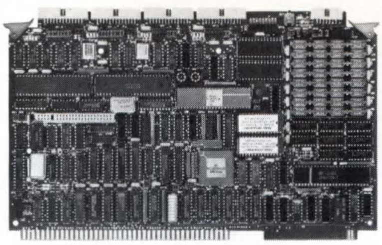

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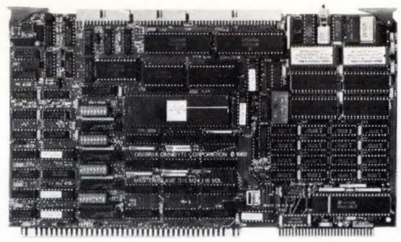

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- (7) prioritized-vectored interrupts
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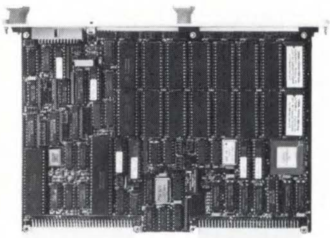

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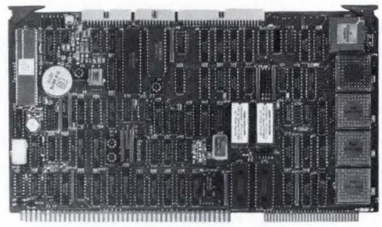

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- (2) 28-pin ROM sockets
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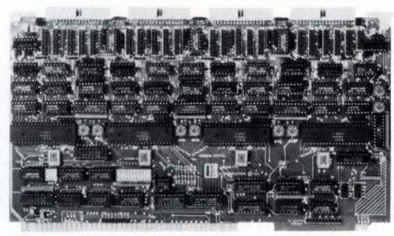

OB68K/OCTAL™ MULTIBUS SERIAL I/O BOARD

- (8) RS-232C or RS-422 serial I/O ports
- Individually programmable baud rates between 50 and 38.4K baud
- (4) 68681 DUART chips
- (4) Multi-function programmable 16-bit counter/timers
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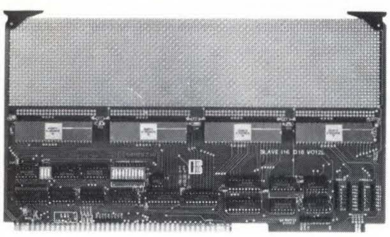

OB68K230™ MULTIBUS 96-BIT PARALLEL I/O TIMER BOARD

- 96 bits of software definable parallel I/O
- (4) 68230 PI/T chips
- (4) 24 bit timers
- 35 sq. in. of prototyping area
- Omnibyte two year limited warranty

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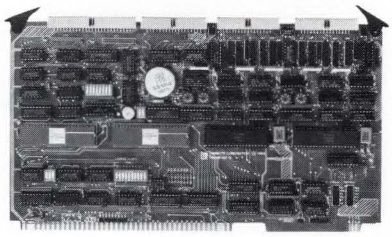

OB68K/INT(S)™ MULTIBUS HOST ADAPTER/ SERIAL I/O BOARD

- (2) 68230 PI/T chips
- (2) 68681 DUART chips
- (4) RS-232C or RS-422 serial I/O ports
- SASI interface to disk controller
- Parallel printer port
- Real time calendar clock with battery back-up
- Omnibyte two year limited warranty

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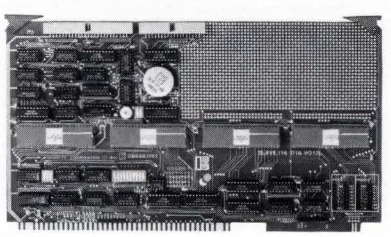

OB68K/INT(P)™ MULTIBUS HOST ADAPTER/ PARALLEL I/O BOARD

- 48 bits of software definable parallel I/O
- Real time calendar clock w/battery back-up
- (4) 68230 PI/T chips
- 15 sq. in. of prototyping area
- Parallel printer port
- SASI* interface to disk controller
- Omnibyte two year limited warranty

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CIRCLE 220

READER FEEDBACK

More on models

Your April 3 Viewpoint article featuring Nick Van Brunt for the first time addressed a very important and misunderstood issue in board- and system-level design analysis: how simulation is best accomplished with physical modelers and software models.

We were very interested in your article because Logic Automation's business is to supply software models of complex ICs to CAE users. Software models offer many advantages to the designer performing logic simulation at the board or systems level. If the models are written at the behavioral level, they are considerably faster than physical modelers. Models are also much less expensive and don't suffer from the same physical limitations, that is, restrictions in total pin count and vector storage depth.

At Logic Automation we largely agree that physical modeling for board-level simulation is not the panacea that it first appeared to be. Indeed, the problems are even larger than outlined in the Viewpoint article. Still, physical modelers do play an important role in solving board-level simulation problems, probably somewhat more than Van Brunt believes. They are an excellent way to include ASICs in board simulation or to simulate components for which no models are available. And it's very unlikely that software models will ever be available for every IC.

The IC manufacturers realize the importance of this problem and are so far being quite supportive of our efforts. Some are even going to the lengths of providing us with their test vectors to verify the models, as well as advance information on new products so that models are available even before some parts are in silicon. Building models for the myriad of ICs available is a huge job, and one that the IC companies don't want to undertake. It really is most cost-effective for an independent company to do it, as development costs can be amortized across similar "pin compatible" products from multiple vendors.

Michael Turner
Director of Marketing
Logic Automation
Beaverton, Ore.

Correction

A number of errors crept into our news story in the March 6 issue, p. 28. The piece described SGS' improved version of Spice for bipolar power transistors (not just for the biFET, which is a trademark of National Semiconductor). Standard Spice underestimates the gain for high collector current densities and decreasing values of collector-emitter voltage (and not just between 0.5 to 2 V). SGS' model improves on this by adding a nonlinear resistance to simulate the transistor's collector-emitter resistance, which can be 10 times higher than the 30 to 50 Ω that Spice assumes.

The correct equations for the collector resistance are: $R = R_o/(1 + exp[(4x/W_c) - 2])$, *and* $x/W_c = (K/I_c)(h\, exp(V_{bc}/V_t) - 1)$, *where h is a constant that depends on the epitaxial doping level.*

Be sure to see Electronic Design's Professional Opportunities Section.

It starts on page 180.

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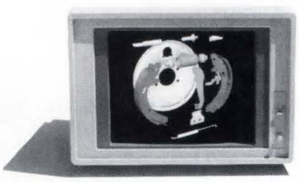

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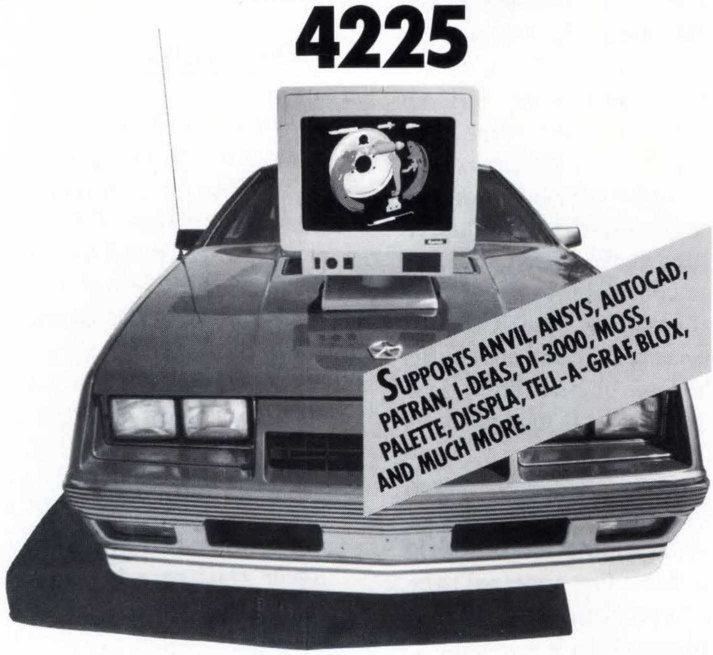

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Ramtek

CIRCLE 66

The end user price comparisons are based on Tektronix 4125 at $19,950 vs. the 2020-4225 at $10,995 and Chrysler Laser base price of $8,854. Ramtek is a registered trademark of Ramtek Corporation.

UPCOMING MEETINGS

Conference on Lasers and Electro-Optics (CLEO '86), June 9–13. Moscone Convention Center, San Francisco, CA. CLEO '86, Optical Society of America, 1816 Jefferson Pl. N.W., Washington, D.C. 20036; (202) 223-0920.

14th International Conference on Quantum Electronics (IQEC '86), June 9–13. Moscone Convention Center, San Francisco, CA. IQEC '86, Optical Society of America, 1816 Jefferson Pl. N.W., Washington, D.C. 20036; (202) 223-0920.

4th European Comdex International Conference & Exposition, June 10–12. The Acropolis, Nice, France. Comdex International, The Interface Group, 300 First Ave., Needham, MA 02194; (617) 449-6600.

IFAC Workshop, Digital Image Processing in Industrial Applications, June 10–12. Helsinki, Finland. Martin Ollus, Technical Research Center of Finland, Otakaari 5 1, SF02150 Espoo, Finland.

IMEKO/IFAC Symposium, Intelligent Measurement, June 10–14. Jena, East Germany. Professor D. Hofmann, Friedrich-Schiller University, Section Technology, GDR-6900, Jena, E. Germany.

International Conference on Power Electronics and Variable Speed Drives, June 10–12. London, England. Conference Services, Institution of Electrical Engineers, Savoy Place, London WC2R 0BL, England; (+44) 1 240 1871.

NEPCON East '86 Electronics Packaging, Production and Testing Conference & Exposition, June 10–12. Bayside Exposition Center, Boston, MA. NEPCON East '86, Cahners Exposition Group, 1350 E. Touhy Ave., P.O. Box 5060, Des Plaines, IL 60017; (312) 299-9311.

1986 Scottish Electronics Show, June 10–12. Anderston Center, Glasgow, Scotland. Network Events Ltd., Printers Mews, Market Hill, Buckingham, MK18 1JX, England; (+44) 280 815226.

1986 International Computer Exhibition, June 12–15. Cologne, West Germany. Messe- und Ausstellungs-Ges.m.b.h. Koln, Messeplatz, Postfach 21 07 60, D-5000 Cologne 21, West Germany; (+49) 221 821-1.

1986 National Computer Conference & Exhibition (NCC '86), June 16-19. Las Vegas Convention Center, Las Vegas, NV. NCC '86, American Federation of Information Processing Societies (AFIPS), 1899 Preston White Dr., Reston, VA 22091; (800) NCC-1986.

1986 Topical Meeting on Ultrafast Phenomena, June 16–19. Snowmass Conference Center, Aspen, CO. Optical Society of America, Ultrafast Phenomena, 1816 Jefferson Pl. N.W., Washington, D.C. 20036; (202) 223-0920.

ISC EXPO '86 Central, International Security Conference & Exposition, June 19–21. O'Hare Exposition Center, Rosemont, IL. ISC EXPO'86 Central, Cahners Exposition Group, Cahners Plaza, 1350 East Touhy Ave., P.O. Box 5060, Des Plaines, IL 60017; (312) 299-9311.

1986 IEEE Computer Vision and Pattern Recognition Conference & Exhibition, June 22–26. Fontainbleau Hilton Hotel, Miami Beach, FL. Dr. Linda Shapiro, Conference Chairman, Machine Vision International, 325 E. Eisenhower Pkwy., Ann Arbor, MI 48104; or IEEE Computer Society, 1730 Massachusetts Ave. N.W., Washington, D.C. 20036; (202) 371-0101.

Image Processing and Applications Conference, June 23–25. London, England. Conference Services, The Institution of Electrical Engineers, Savoy Place, London WC2R 0BL, England; (+44) 1 240 1871.

7th Power Modulator Symposium, June 23–25. Hyatt Seattle, Seattle, WA. Leslie Gallo, Program Secretary, Palisades Institute for Research Services Inc., 2011 Crystal Dr., 1 Crystal Pk., Ste. 307, Arlington, VA 22202; (703) 769-5580.

Automatic Test Equipment (ATE) East '86 Conference & Exhibition, June 23–26. World Trade Center, Boston, MA. Morgan-Grampian Expositions Group, 1050 Commonwealth Ave., Boston, MA 02215; (617) 232-3976.

(continued on p. 70)

UPCOMING MEETINGS

(continued from p. 69)

CPEM '86, Conference on Precision Electro-Magnetic Measurements, June 23–27. National Bureau of Standards, Gaithersburg, MD. CPEM '86 Technical Program Chairman, Norman B. Belecki, National Bureau of Standards, B146, Metrology, Gaithersburg, MD 20899; (301) 921-2715.

4th European Fiber Optics Communications & Local Area Networks Exhibition (EFOC/LAN '86), June 23–27. International Congrescentrum Rai, Amsterdam, The Netherlands. Joan Barry, Information Gatekeepers Inc., 214 Harvard Ave., Boston, MA 02125; (617) 232-3111.

Power Electronics Specialists Conference (PESC '86), June 23–27. University of British Columbia campus, Vancouver, B.C., Canada. Peter Wood, Westinghouse R&D Center, 1310 Beulah Rd., Pittsburgh, PA 15235; (412) 256-2306.

1986 Advanced Manufacturing Systems Conference & Exposition (AMS '86), June 24–26. McCormick Place, Chicago, IL. AMS '86, Richard John & Co., 1350 E. Touhy Ave., P.O. Box 5060, Des Plaines, IL 60017; (312) 299-9311, Jane Allred.

23rd Design Automation Conference & Exhibition (DAC '86), June 29–July 2. Las Vegas Hilton, Las Vegas, NV. DAC '86. Donald E. Thomas, Program Chairman, IBM Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, NY 10598.

International Workshop on Systolic Arrays, July 2–4. University of Oxford, Oxford, England. Dr. Will Moore, Secretary, Systolic Array Workshop, Dept. of Engineering Science, University of Oxford, Parks Rd., OXFORD, OXI 3PJ, England; 0865 59988.

4th Annual Personal Computer (PC '86) Exposition & Conference, July 9–11. Jacob K. Javits Convention Center, New York, NY. PC Expo, 333 Sylvan Ave., Englewood Cliffs, NJ 07632; (201) 569-8542.

British Information Technology (Britec '86) Conference & Exhibition on Engineering Software, July 14–16. Hilton Hotel at Colonial, Wakefield, MA. Dr. C. A. Brebbia, Computational Mechanics Inc., Ste. 6200, 400 W. Cummings Pk., Woburn, MA 01801; (617) 933-7374.

1986 American Society of Mechanical Engineers, (ASME) International Computers in Engineering Conference & Exhibition, July 20–24. Hyatt Regency, Chicago, IL. Dr. David Dietrich, Conference Chairman, Swanson Analysis Systems Inc., P.O. Box 65, Houston, PA 15342; (412) 746-3304.

2nd International Committee on Acoustic Emission from Reinforced Plastics (CARP) Conference & Exhibition, July 21–25. Montreal, Canada. James R. Mitchell, Organizing Committee CARP/SPI, Physical Acoustics Corp., P.O. Box 3135, 819 Alexander Rd., Princeton, NJ 08540; (609) 452-2510.

1986 Summer Computer Simulation (SCSC '86) Conference & Exhibition, July 28–30. MGM Grand Hotel, Reno, NV. SCSC '86, Society for Computer Simulation, P.O. Box 17900, San Diego, CA 92117; (619) 277-3888.

SIMS '86, Symposium for Innovation in Measurement Science, August 3–6. Hobart and William Smith College campuses, Geneva, NY. Instrument Society of America, P.O. Box 12277, Research Triangle Pk., NC 27709; (919) 549-8411, Marie Long.

5th International Conference on Artificial Intelligence, August 11–15. Philadelphia Convention Center, Philadelphia, PA. Lorraine Cooper, AAAI, 445 Burgess, Menlo Park, CA 94025; (415) 328-3123.

13th Annual Computer Graphics and Interactive Techniques (Siggraph '86) Conference & Exhibition, August 18–22. Dallas Convention Center, Dallas, TX. IEEE Computer Society, 10662 Los Vaqueros Circle, Los Alamitos, CA 90720; (714) 821-8380, Lorraine Weeks.

15th Annual International Parallel Processing Conference, Aug. 19–22. Pheasant Run Resort, St. Charles, IL. 1986 International Conference on Parallel Processing C/O IEEE Computer Society, 1730 Massachusetts Ave. N.W., Washington, D.C. 20036.

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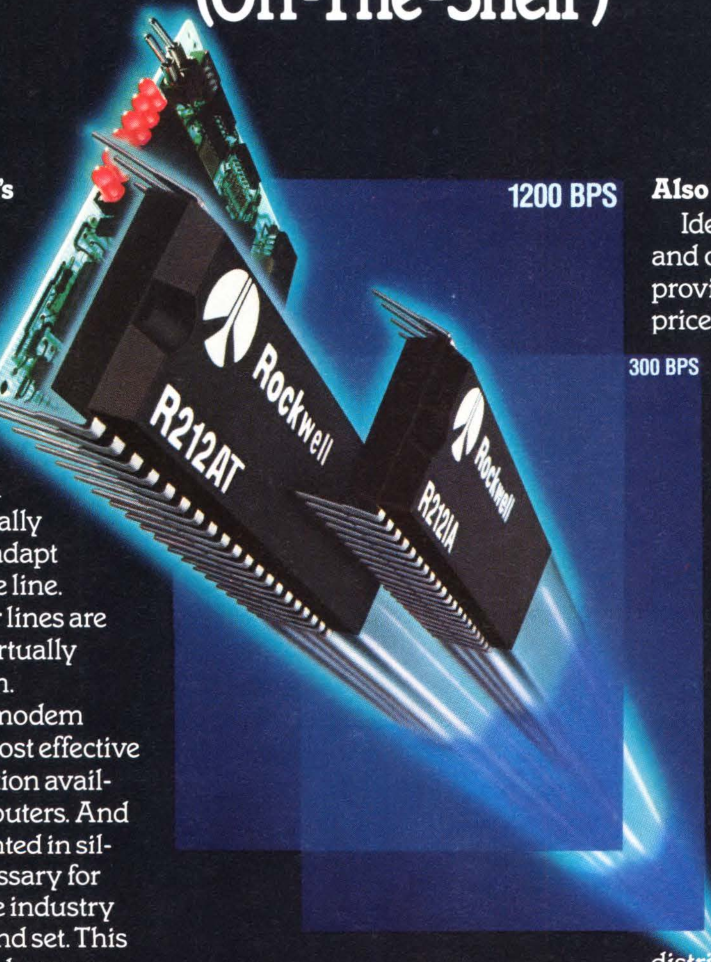

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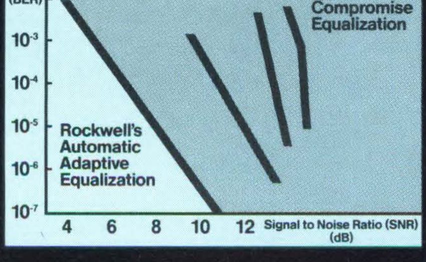

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CIRCLE 46

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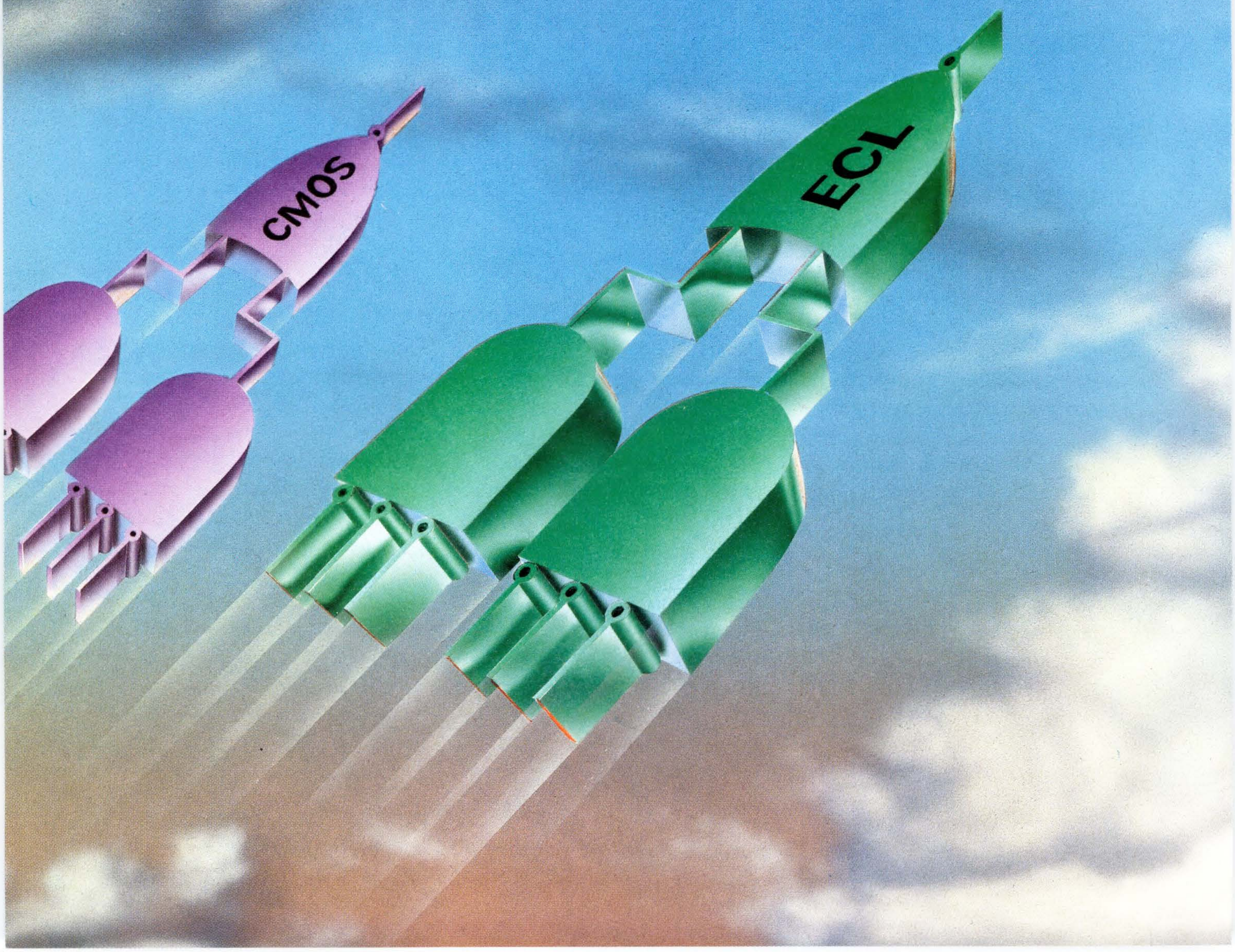
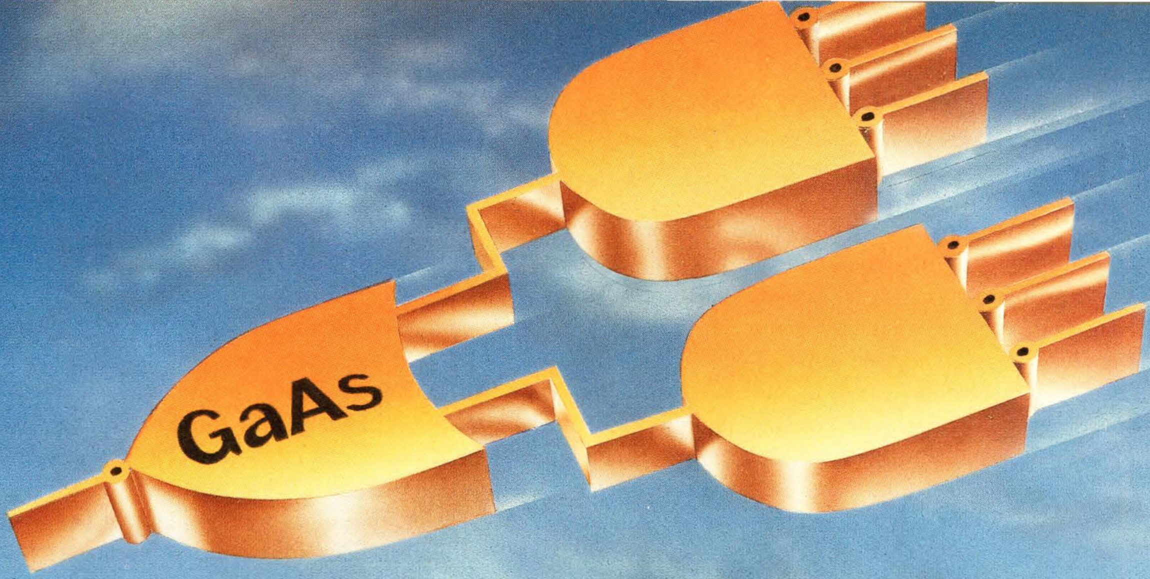
ELECTRONIC DESIGN REPORTS

Subnanosecond silicon ECL gate arrays face challenge from GaAs and CMOS

Dave Bursky





The mainstay of the fastest digital systems, silicon ECL gate arrays face an onslaught of competition as new processes and materials run tight on their heels. Fortunately, the same technological advances that give MOS its advantages will guarantee that bipolar arrays remain several steps ahead of MOS and mixed bipolar-MOS and in stride with the subnanosecond speeds of gallium arsenide. In fact, before the year ends, ECL gate arrays will pack as many as 10,000 gates and deliver gate delays of only 200 to 300 ps.

Nonetheless, ECL does stand to lose its edge in certain fields. For instance, boards built with previous-generation SSI and MSI ECL chips can now be replaced by high-density CMOS gate arrays and mixed bipolar-CMOS chips, with delays of 0.7 to 1 ns and integration levels of 5000 to 50,000 gates. At the same time, gallium arsenide may outrun ECL in some designs calling for extremely high speed (Fig. 1). GaAs logic arrays and standard cells now come in with delays of 200 ps or less and complexities of a few hundred gates to a few thousand.

For the most part, the industry's manufacturing experience with ECL, coupled with costs that are lower than those for GaAs, ensures that ECL will remain the high-speed workhorse throughout the decade and beyond. Yet right now, the field of competitors is small. Only about a dozen companies compete in subnanosecond gate arrays, a far cry from the 50 or so that churn out CMOS gate arrays. Even fewer companies expect to deal in commercial gallium arsenide arrays — perhaps half a dozen in 1987 and several more by 1988.

In standard cells, the game is similar. Loads of companies offer CMOS cells, but only one or two plan to get involved with bipolar digital standard cells. The expense of developing and maintaining a standard-cell library seemingly would not be justified by production volumes of only a few thousand chips, quantities that would be perfect for gate arrays. (For more on standard cells, see the box.)

Bipolar gate arrays fabricated with ECL or even current-mode or nonthreshold logic now sport complexities ranging from a low of 100 equivalent gates to about 8000. The higher number will double again by the end of next year, thanks to smaller low-power transistors, adjustable speed-power products, and chips reaching 400 mils on a side. A few chips squeeze some static RAM alongside the logic elements, a strategy that improves silicon efficiency by a factor of two or three when register files are needed. More logic-plus-memory chips are on the way.

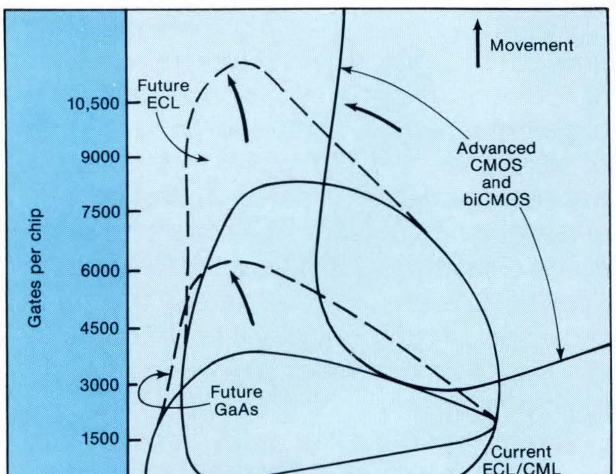
The term "equivalent gates" is peculiar to bipolar gate arrays. Unlike other types, the majority of bipolar arrays do not have gates prediffused into the chip. Instead they have groups of transistors and resistors (here, called macrocells) that are used to build multilevel cascode logic circuits (ELECTRONIC DESIGN, Feb. 6, 1986, p. 127). Cascode ECL structures implement various circuit functions (such as an exclusive-OR, exclusive-NOR circuit) far more efficiently than predefined gates can (Fig. 2).

Unfortunately, multilevel cascode structures make the term "gate propagation delay" almost meaningless, since the chip contains no true gates. Therefore, instead of specifying gate delay, most manufacturers specify the speed and power for some typical functions (multiple-input NOR gates, flip-flops, multiplexers). Further complicating matters, the number of gates in arrays offered by different manufacturers defies comparison, as each manufacturer defines a gate differently.

Many of the arrays expected in the near future will replace boards of smaller arrays or MSI logic and thus must provide plenty of I/O lines that can handle either ECL or TTL-CMOS signal swings. With that requirement, input- and output-only buffers are giving way to I/O buffers that can be programmed for either direction. Just as I/O lines and buffers will change, pin counts will more than double from today's range of 120 to about 160: Packages with 300-plus pins already are nearing production. They will withstand the 15 W or more that the next generation of ECL arrays will demand at top speed.

When operating at full throttle, high-speed gates typically draw between 3 and 5 mW each; fortunately, in a large array, not every gate has to run at top speed. Thus all array manufacturers are exploring ways, usually through ion implantation or metal masks, to provide a lower-power, lower-speed operating point for each circuit macrocell. Doing so could decrease gate power by a factor of two to four but lengthen the delay of that particular gate proportionally.

Macrocells usually include resistors of more than one value and transistors of more than one type. By properly selecting those components during circuit design, an engineer can alter each cell's current draw for the task at hand, thereby maximizing the overall speed/power ratio (Fig. 3). An adjustable speed-power product, common to just about all arrays, is critical as gate counts rise above 3000. Without the low-power option, a 5000-gate chip might consume anywhere from 15 to 25 W; with optimized current, it might demand 5 to 10 W.



1. The traditional realm of ECL gate arrays is now under attack: fine-line CMOS and mixed bipolar-CMOS processes from the low-speed front, practical GaAs chips from the high-speed front.

By giving designers a choice of two silicon starting points—wafers identical in all respects except the ion-implantation dose used to set the current-source resistance—Thomson-Mostek's Vatic Systems Inc. (Carrollton, Texas) doubles the number of speed-power choices that mask-programming alone provides. Vatic's three arrays carry 750 to 3632 gates and have delays that can be programmed for 800 ps to 1.3 ns (see the table). The chip's total power, though, is determined by the I/O interface, which can be programmed for either ECL 10K or TTL levels. A faster 3500-gate chip is now in design.

Motorola Inc.'s Semicustom Group (Phoenix, Ariz.) has taken a similar approach. A 10,000-gate chip, the first in the MCA 3 family, will be offered with two speed ranges and two mask-programmable current levels. The faster version will sport gate delays of 150 to 250 ps with switch currents of 0.8 to 0.4 mA; the slower chip, gate delays of 300 to 500 ps at about half the current. In addition, through metal options the designer can select one of several levels within the current range. Like preceding chips, the array, due late this year, operates with a −4.5-V supply instead of the usual −5.2 V needed for ECL 10KH chips. The lower supply voltage further reduces the chip's power consumption by about 16% without sacrificing ECL 10KH logic swing compatibility.

To keep the MCA 3 chip's gate power to about 2.5 mW, Motorola turned from 2-μm geometry to 1.5 μm, enlisted a high-performance transistor structure (one using self-aligned polysilicon bases, emitters, and collectors), and reduced the gates' internal logic swing. However, the smaller logic swing dictates the ECL 10KH input signals and outputs from the array core pass through interface buffers. The buffers add some delay to the signal, but the delay is considered insignificant when evaluated as part of the overall chip delay.

Although Motorola has yet to release samples of the 10,000-gate chip, another half-dozen ECL arrays are now in volume production within the MCA 2 and MCA 1 families. Those arrays will soon be joined by one with about 800 gates, the MCA800. Although it aims at telecommunications, it has no special on-chip resources. Motorola does guarantee its operation, as well as its software library macros, for 770 MHz—a frequency crucial for some of the latest digital communication systems.

Two versions of the MCA 2 arrays carry some static RAM to satisfy designs that require small amounts of memory. For instance, a predefined metal mask optionally gives the MCA2800 a 16-by-8-bit multiport memory that accesses in 6 ns. However, for larger amounts of RAM, dedicated silicon yields denser and faster memories more efficiently. Motorola counted on exactly that to squeeze about 1 kbit of 2-ns single-port RAM on its MCA1500M.

On-chip RAM attracts other companies too, now that a thousand bits or more can fit on the same chip as the logic. Within the recently released turbo upgrade for the Philips-Signetics ACE family, one chip incorporates 1280 bits of 4-ns RAM and 1450 gates with 250-ps delays. The 30T00 chip quadruples the RAM included on the earlier ACE 1320 RAM-equipped array, halves the access time, and slashes gate delays by more than 30%. The 128 I/O lines can be programmed for ECL 10KH, ECL 100K, or TTL signal levels. Older and slightly slower, the QM1600S from Applied Micro Circuits also contains 1280 bits of RAM. However, a 20% faster version is slated for sample release in about two months.

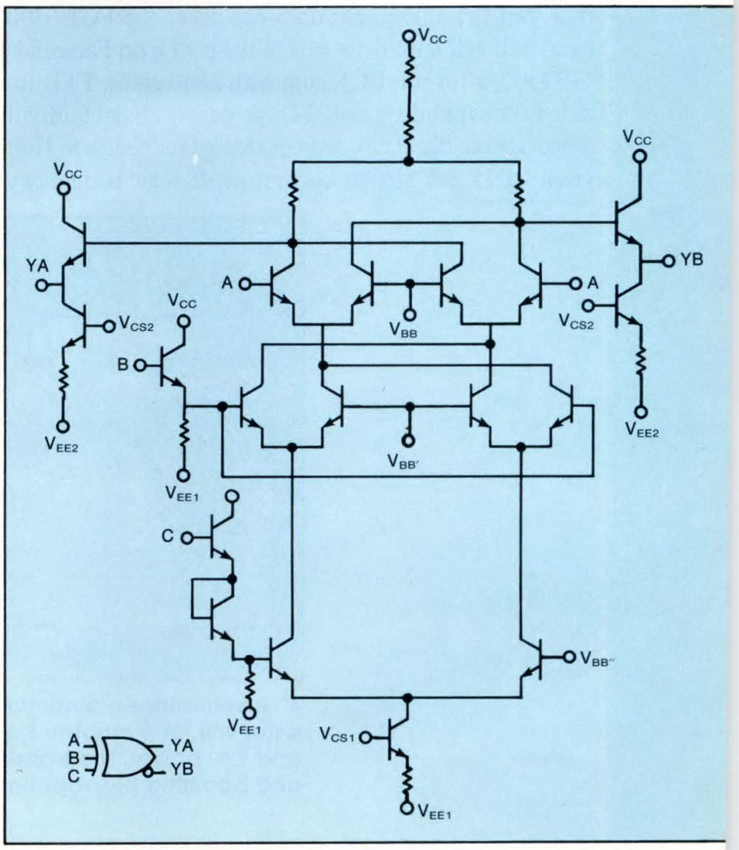
Rounding out the list of currently available memory-plus-logic arrays is one that packs 1152 bits of RAM next to 3700 additional gates. Developed by Advanced Micro Devices, the Am3525 manages to keep the memory access time to 5.5 ns and worst-case gate delays to 650 to 950 ps.

Naturally, more combination arrays will eventually see the light of day, some by the end of the year: Fairchild Semiconductor's Semicustom Division plans to release a RAM-equipped version of its new FGE6300. The FGE6320R contains eight RAM blocks of 32 by 9 bits but gives up about 2300 gates to do so. The basic FGE6300 sports about 6300 equivalent gates and has 216 I/O pads (ECL 100K, ECL 10KH, or TTL) and 80 or more for power and ground. A 301-lead pin-grid array holds the chip when all signal and power pads are used.

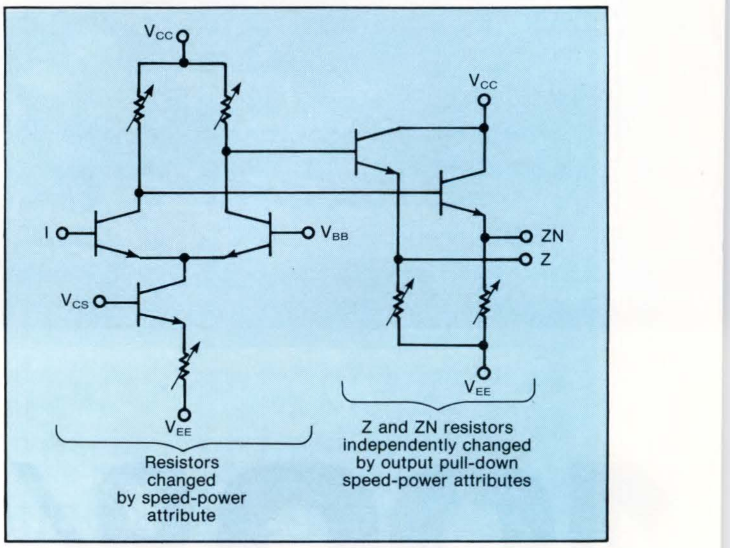
A new entry in the ECL array field, Fujitsu Ltd. (Tokyo) has in the works a RAM-plus-logic chip, with a target release date of late 1987. Though Fujitsu's in-house designers can already take advantage of a 2000-gate array with a 16-kbit RAM (ELECTRONIC DESIGN, March 6, 1986, p. 28), in all likelihood, a version with less RAM and more logic will be what makes it into the commercial realm. Another logic-plus-memory array, this one from NEC Corp. (Tokyo), is scheduled for release in mid-1987. Preliminary word indicates about 3000 logic gates and 2 kbits of 5-ns RAM.

Though arrays with embedded memory have their attraction, many systems demand arrays with just random logic, lots of it. Two of the largest chips around, the FGE6300 and the HE8000, can adequately fill most designers' needs. The first, made by Fairchild, furnishes 6300 gates and 225-ps delays; the latter, fabricated by Honeywell's Digital Products Center, carries 8000 gates with 210-ps delays. Both have plenty of I/O resources.

Each company now acts as an alternative source for the



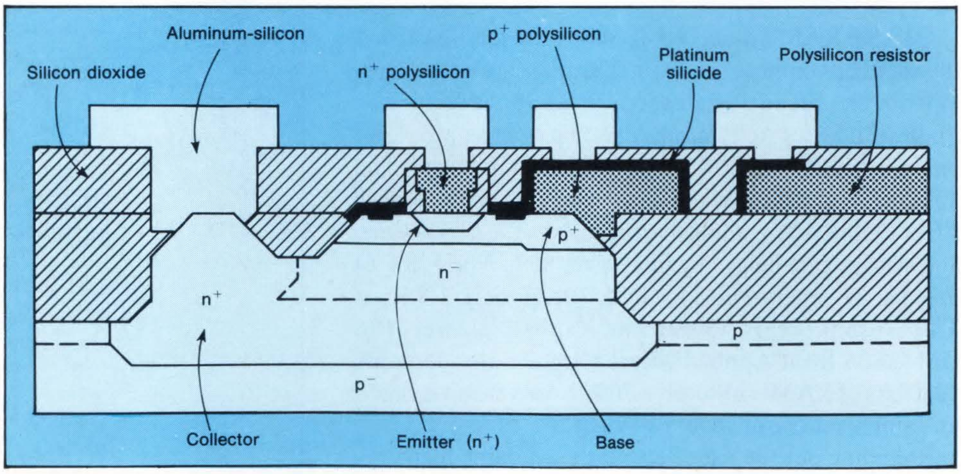
2. Trilevel cascode logic, as used in Motorola's three-input exclusive-OR, exclusive-NOR circuit, implements logic functions very efficiently. Significantly more transistors would be needed if the same circuit were built with elemental gates.



3. Designers can choose among two or more resistor values in many circuit macrocells, enabling them to tailor a gate array's speed-power level to the job. For instance, Fairchild's internal cell contains five adjustable resistors—grouped as one set of three (left) and one set of two (right)—which the user sets on a CAD system.

other, but the agreement does not cover the FGE6300. Honeywell will initiate its part of the pact with Fairchild's FGE2500, a 1.5-μm ECL chip with 2840 gates, TTL and ECL I/O capability, and 225-ps delays. Fairchild will second-source the HE8000 in exchange for access to Honeywell's 1.25-μm bipolar current-mode logic technology.

To maintain the 6300's short delays with its 1.5-μm process, Fairchild ties the array's internal termination resistors to a −2-V supply. Additionally, when gates must handle a large fan-out, on-chip drivers can reduce the delay deterioration caused by the heavy loading. Few other companies include the built-in termination resistors or the



4. A self-aligned platinum silicide coating on the base of this scaled bipolar transistor will let Mitsubishi Electric reconcile trade-offs between high performance and low power. The transistor will be used in arrays carrying close to 15,000 gates and boasting propagation delays of only 100 ps or so.

on-chip drivers.

From England, Plessey Ltd. (Caswell, Northants.) plans to offer a family of ECL arrays with 125-ps delays and 500 to 2000-plus gates. The gates' power consumption can be mask-programmed from 5 mW/gate for the fastest version to 1 mW for the slowest option. Like the arrays offered by most companies, Plessey's chips contain three layers of metal interconnections, but unlike those others, a polyimide-based dielectric material will serve as the intermetal insulator. The polyimide forms a much flatter surface than the more common deposit of silicon dioxide. The smoother surface not only reduces the risk of poor step coverage, it also allows metal lines to be kept very thin and the wiring to be routed over contact regions, clearly leading to greater silicon efficiency.

Another European company expected to enter the fray is Siemens AG (Munich, West Germany). It has quietly started developing some arrays, probably with 3000 to 6000 gates, based on the self-aligned bipolar transistors it uses for a 9000-gate CML array. That chip contains 256 I/O buffers, which convert external ECL 100K or 10K signal levels to CML levels or vice versa, and 64 power and ground pads.

From Japan, both Fujitsu Ltd. and NEC Corp. have recently unveiled ECL arrays. Fujitsu's ET3000 and ET4500, with respective counts of 3000 and 4500 gates, offer mask-programmable combinations of 220 ps at 5 mW or 260 ps at 2.4 mW. I/O buffers in the arrays can be configured for ECL 10KH or LSTTL compatibility. Late next year, a 1-μm trench isolation process will reduce transistor spacing enough to pack somewhere between 6000 and 8000 gates on extremely compact arrays.

Using its own counting method, NEC pegs its eight-array family at 300 to 5000 gates, though it admits that the count would actually be about 8000 gates maximum, if it applies Motorola's counting approach to the μPB63xx family. Most of the arrays have loaded delays of about 700 ps, but the smallest chip keeps the figure down to just 500 ps. A 4000- and a 5000-gate unit, the two largest chips, can tie their I/O buffers into TTL, ECL 10KH, or ECL 100K levels. Now in development is a series of arrays with loaded delays as short as 220 ps at about 4 mW. A 1200-gate device is first on the schedule.

Designers with big ideas will meet their match with a 15,000-gate ECL array now being defined by Mitsubishi Electric Corp. (Itami, Japan). The chip, which may be ready for release toward the end of 1987, will use a new 1.2-μm technology that relies on self-aligned silicide ("salicide") contacts and bases; first details were revealed at ISSCC 1986 (Fig. 4). Gate delays of 150 ps with milliwatt-level power consumption will keep chip power to reasonable levels.

Giving older-generation ECL a run for its money are two mixed bipolar-CMOS schemes, described by Motorola and NEC just last month at the Custom IC Conference. Both approaches merge CMOS logic gates and bipolar buffer drivers for each array cell, with current results being gate delays of 900 ps tops. A bipolar drive stage greatly reduces the loading effect that long metal wires and large fan-outs have on CMOS gates—a critical problem as arrays grow.

The gate delays of the bipolar-CMOS chips are sure to plunge even further. At Motorola, shrinking 2-μm design rules by 30% should slash propagation delay to less than 650 ps. Motorola's basic cell consists of five n-channel and two p-channel MOS devices and two npn transistors set up as a push-pull driver (Fig. 5). NEC's process already employs fine features to deliver gate delays of 800 ps. The element arrangement is similar to Motorola's, but it adds three n-channel and two p-channel devices, as well as a resistor, to the basic cell. Motorola's chip will carry 6000 gates and 202 I/O buffers, NEC's only 3100 gates and 140 I/O buffers, despite its larger cell.

Even arrays that are made solely with CMOS structures can reach the subnanosecond internal delays of ECL or bipolar-CMOS. But to do so, they must use exacting lithography (typically with minimum feature sizes of 1.5 μm or smaller). Moreover, internal loading takes its toll far more quickly on CMOS than on bipolar circuits. In many instances, though, the higher densities possible with CMOS more than compensate for the slightly slower internal gates.

Not surprisingly, the greatest threat to ECL's speed title comes from gallium arsenide. With an intrinsic electron mobility about five times greater than that of silicon, GaAs transistors can switch that much faster. Moreover, they operate at lower power levels, since the substrate's semi-insulating property keeps down both device parasitics and hence switching losses. In addition, GaAs operates over a wider temperature range ($-100°$ to $+200°C$ is considered possible) and withstands higher levels of radiation than do most silicon circuits, facts that make the technology attractive to military system designers. Few ECL gate arrays, for example, are guaranteed for operation over the full $-55°$ to $+125°C$ range. (For a review of the status of GaAs, see ELECTRONIC DESIGN, Dec. 12, 1985, p. 79.)

Most GaAs activity centers on enhancement-mode and depletion-mode MESFETs (metal semiconductor FETs) formed via ion implantation. But two relative newcomers, high-electron-mobility transistors (HEMTs) and heterojunction bipolar transistors (HBTs), offer even faster switching characteristics than MESFETs.

Today, GaAs arrays carry anywhere from a few hundred to a couple thousand gates. Samples are starting to appear, and several companies plan to release arrays with about 4000 counts for sale in 1987. Gate delays will fall between 100 and 200 ps, and power levels will be similar to those of today's ECL. However, adjustable speed/power ratios will keep a chip's overall power demands to half or below that of silicon ECL.

For instance, an experimental 4032-gate array built with HBTs by Texas Instruments (Dallas) relies on integrated injection logic to obtain good packing density and drive capability. The array consumes just 1 mW/gate at delays of 400 ps, but slowing gates to 1250 ps lowers the power to 0.2 mW. Further process refinements will allow delays as short as 100 ps with a gate power of 4 mW. The

Standard cells find their niche

Although silicon bipolar standard-cell designs promise better performance than gate arrays, their high cost has discouraged their use. IC manufacturers are reluctant to invest the large sums required to maintain standard-cell libraries because of the traditionally low volumes of high-speed circuits. Users, for their part, don't want to incur the additional NRE charges necessitated by the six to nine extra masks (over and above those required by gate arrays). Only two companies, VTC Corp. (Minneapolis) and Plessey Ltd. (Northants, U.K.), currently intend to deal in bipolar standard cells.

With typical loaded gate delays of 350 ps, VTC's standard-cell family, the Series 2000, includes both digital and analog functions. Plessey's capability will likely be released next year as a supplement to its Classic design automation system. The ECL megacells, appearing as fixed macros in the library, will match the performance levels of an ECL array family scheduled for introduction late this year.

More companies plan to enter the gallium arsenide standard cell market, partially because fewer masks lower the NRE charges but mostly because MESFET technology does not lend itself to gate arrays. Transistor speeds deteriorate rapidly as distances and loads increase, much more rapidly than with bipolar transistors; thus large MESFET-based GaAs gate arrays might actually operate more slowly than ECL chips. GaAs standard cells, in contrast, permit designers to minimize circuit loading and distances between cells. Though GaAs material costs about 20 times more than silicon and is more prone to material defects, standard cells use the real estate so efficiently that a GaAs chip's cost-performance could actually compete with silicon.

Triquint Semiconductor Inc. (Beaverton, Ore.) is pioneering the GaAs standard cells, and other companies are embarking on contractual custom development programs before releasing their libraries.

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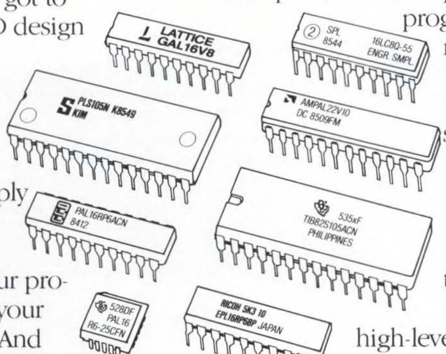

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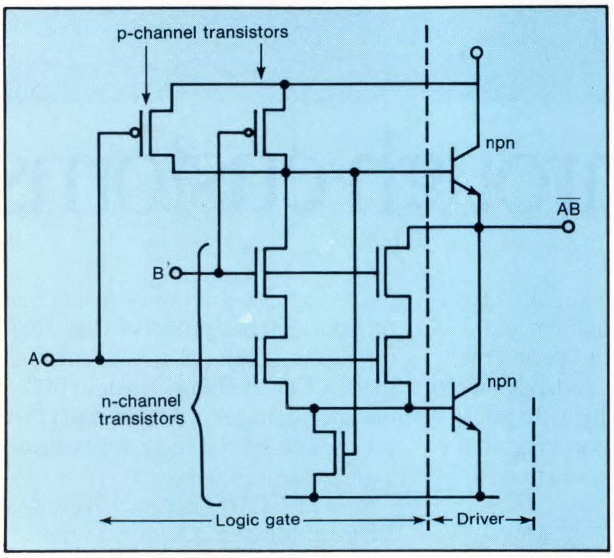
160 I/O buffers interface with ECL signal levels; the chip will operate from −100° to +200°C.

Although the 4032-gate chip is still experimental, TI plans to offer a commercial version, as well as a 2-k and a 6-k version by next year. Similar commercial plans are in the works at Ford Microelectronics and Honeywell's GaAs IC Product Center (both in Colorado Springs).

By the end of the year, Ford expects to have a 1000-gate array ready for designers' use. At the Custom IC Conference last month, it gave some indication of what it expects from proprietary depletion-mode MESFET configurations. Based on a 504-gate chip, gate delays hit 250 ps with a 0.7-V noise margin and a power drain of about 2 mW. The circuit structure, called FET-diode-FET logic, can implement four-input NORs with optional output buffers; the configuration handles highly capacitive loads and thus large fan-outs.



5. The basic mixed bipolar-CMOS cell in Motorola's MCA6000ETL array contains n- and p-channel MOS devices, which form the logic, and two npn bipolar transistors, which strengthen drive and reduce loading effects on the gate.

As for Honeywell, it has already started offering a commercial 1950-gate chip with 56 I/O pads. The HGG-2020 has gate delays of about 230 ps with a power of 3 mW; the I/O buffers add a mere 500 ps—about half that of ECL and an eighth that of bipolar-CMOS. The I/O buffers can be arranged to tie into TTL, CMOS, or ECL signals and into other GaAs systems. Honeywell is in the midst of evaluating an array with three times the density; gate delays will be close to those of the smaller chip, but per-gate power will plummet to one-tenth.

Smaller arrays are already hitting the streets. Triquint Semiconductor (Beaverton, Ore.) and Harris Microwave Semiconductor (Milpitas, Calif.) offer chips with clock rates of 2 GHz. Triquint's Q-chip array consumes about 3 W and holds about 150 gates in its 28 cells, which can be customized through their 20 transistors and 8 diodes.

The HMD-11100-3 array from Harris can deal with signals as fast as 3 GHz. Predicated logic functions enable Harris to about double the gate count of the Q-chip. Instead of an array of gates, the chip contains 8 master-slave flip-flops, 88 inverters, 48 AND gates, 8 NOR gates, 6 dual-phase clock drivers and differential amplifiers, 16 input buffers, and 8 output buffers. To get the speed and flexibility, designers pay the piper in power consumption: 35 mW/gate on average with a 130-ps delay.

Fujitsu also plans to release several small arrays by the end of this year, and several other companies are also actively researching GaAs array concepts. NEC, Toshiba (Tokyo), Gigabit Logic (Newbury Park, Calif.), and Oki Electric (Machioji, Japan), all are talking about arrays with a few hundred to about 3000 gates.

Toshiba reported incredible 42-ps delays on a 2000-gate chip unveiled in 1985, NEC showed off 48-ps delays in a 3000-gate chip, and last month's Custom IC Conference had Gigabit describing 76-ps delays in an array-based ring oscillator (using proprietary capacitor-diode FET logic). Oki developed a slower structure called super-buffered FET logic that yields 390-ps delays but can handle big fan-outs without much of a slowdown. □

ECL gate arrays

Company	Part number	Equivalent gates (RAM)	Gate speed (ps); gate power (mW)	I/O pads; logic-level interface	Features and comments	Circle
Advanced Micro Devices Inc. 901 Thompson Pl. Sunnyvale, CA 94088 (408) 732-2400	AmMPA1850[1] AmMPA3500[2] AmMPA3525 AmMPA3550[2]	1800 4988 3718 (1152 bits, 5.5 ns) 5228	800–1200; 4–0.7 600–900; 3–1.5[3] 600–900; 3–1.5 600–900; 3–1.5[3]	75; ECL, TTL 134; ECL 135; ECL 124; ECL, TTL	[1]Compatible with Motorola MCA 1 library [2]Superset of Motorola MCA 2 library [3]Three programmable speed-power levels	465
Applied Micro Circuits Corp. 5502 Oberlin Dr. San Diego, CA 92121 (619) 450-9333	Q700 Q1500 Q3500 QM1600S	250, 500, 1000 1500, 1700 1300, 2400, 3500 1600 (1280 bits)	500–900; 8–5[1] 500-900; 12–5 275–700; 15–4 275–700; 15–4	36–76; ECL, TTL 84–120; ECL, TTL 76–120; ECL, TTL 106; ECL, TTL	All arrays available for military temperature range; [1]Two programmable speed power levels; all others, three	466

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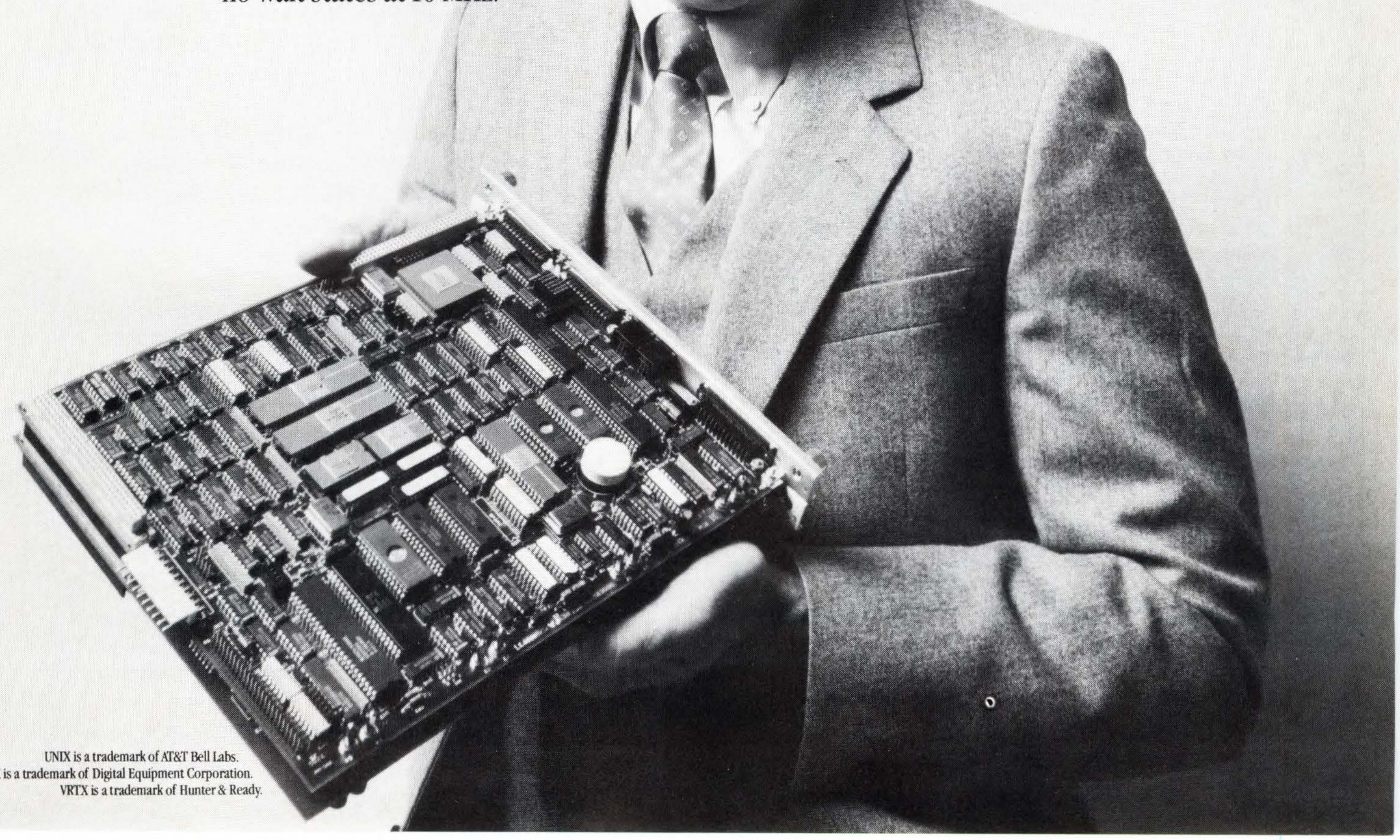

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ECL gate arrays (cont'd.)

Company	Part number	Equivalent gates (RAM)	Gate speed (ps); gate power (mW)	I/O pads; logic-level interface	Features and comments	Circle
Fairchild Semiconductor Inc. 1801 McCarthy Blvd. Milpitas, CA 95035 (408) 942-2672	FGE0050, 0550, 2000 FGE2500 FGE6300[1] FGE6300R[1]	100, 680, 2500 2840 6300 4000 (2304 bits)	225–570; 9–2.5 225–570; 9–2.5 225–570; 9–2.5 225–570; 9–2.5	21–120; ECL 120; ECL, TTL 216; ECL N.s.	All models have three programmable speed-power levels; [1]Internal −2-V termination	467
Fujitsu Microelectronics Inc. 2985 Kifer Rd. Santa Clara, CA 95051 (408) 727-1700	ET3000 ET4500	3072 ~4500	220–570; 4,7–2–4 220–570; 4.7–2.4	72 ECL I/O 192 TTL I/O E/T N.s.	In both models, ECL inputs can go directly to logic cells	468
Hitachi America Inc. 2210 O'Toole Ave. San Jose, CA 95131 (800) 842-9000	HG28	630–2550	800	48–114	Bipolar-CMOS logic cells and I/O buffers	469
Honeywell Inc., Digital Products Center 1150 E. Cheyenne Mountain Blvd. Colorado Springs, CO 80906 (800) 328-5111, ext. 3422	HM1000, 3500[1] HE2000 HT5000[2] HE8000[3]	1000, 3500 2000 5000 8000	800; 2 300; 2 550–740; 0.6–0.4 210; 0.6–0.4	60–110; ECL, TTL 140; ECL 10K/KH 120; TTL, CML 196	[1]Radiation-hardened versions available [2]Military temperature range available [3]Two programmable speed-power levels; mixed TTL-ECL and TTL-only in development	470
Mitsubishi Electronics America Inc. 1050 E. Arques Ave. Sunnyvale, CA 94086 (408) 730-5900	VSC	3000–15,000	150; 1	N.s.; ECL 10KH		471
Motorola Inc. P.O. Box 20912, M/S ADV 72 Phoenix, AZ 85036 (602) 244-6900	MCA 1 MCA 2	652, 1192 902–2958[1]	900–1200; 3.3 300–1100; 2.6	46,60; ECL 10KH/K 54–120; ECL, TTL[3]	[1]Two models have on-chip memory [2]Some versions are ECL-only; one, TTL-only	472
NEC Electronics Corp. 401 Ellis St. Mountain View, CA 94039 (415) 960-6000	MCA 3 MCA6000 ETL (biCMOS) ECL-2 ECL-3 ECL-4 Bipolar-CMOS[1]	10,000 8192 300–2000 1200–3000 4000–5000 3100	150–250; 4–1[3] 900–1100;22μW/MHz 500–700; 5.4–1.9 1000; 1.1 700; 1.9 800; 30μW/MHz	256; ECL 202; ECL 10KH, TTL 56–108; ECL 100K 88–180; ECL 10KH 156–172; ECL, TTL 140; TTL, CMOS	[1]In final development	473
Philips International BV and Signetics Corp. 811 E. Arques Ave. Sunnyvale, CA 94086 (408) 991-2000	ACE (standard) ACE (turbo) ACE (turbo RAM) ACE (low power)	1650 (310 bits, 5 ns) 660–2700 1450 (1280 bits, 4 ns) 660–2700	350; 0.9 250; 3 250; 3 450; 1.5	112; ECL, TTL 28–128; ECL, TTL 128; ECL, TTL 28–128; ECL, TTL		474
Plessey Semiconductors Inc. 3 Whatney Irvine, CA 92714 (714) 951-5212	SCD 1000 Future[1]	75–600 500–2000+	500–2000; 5–2 125–250; 5–1	24–54; ECL 10K N.s.	[1]Late 1986 [2]Early 1987	475
Siemens Components Inc. 186 Wood Ave S. Iselin, NJ 08830 (201) 321-3400	SH100B/1, B/2 SH100B/3 SH100C Future[1]	700, 960 700 (bits, ns) 960, 2500 4000–9000	500; 2 500; 2 350; 2 150; 7.5–5	58; ECL 100K 58; ECL 100K 58–120; ECL <256; ECL	[1]Currently for internal use only	476
Thomson-Mostek Vatic Systems Inc. 1215 W. Crosby Rd. Carrollton, TX 75006 (214) 466-6000	B600–B3500	750–3632	800; 2–1	72–128; ECL 10K, TTL	Adjustable speed-power levels	477
VTC Inc. 2401 E. 86 St. Bloomington, MN 55420 (612) 851-5000	Standard cell	Variable	350; 2	User-defined; ECL 10KH, TTL	Military and radiation-hardened (10-Mrad) versions available	478

N.s. = not specified yet

Probe is shown approx. 50× actual size

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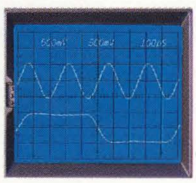

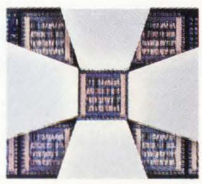

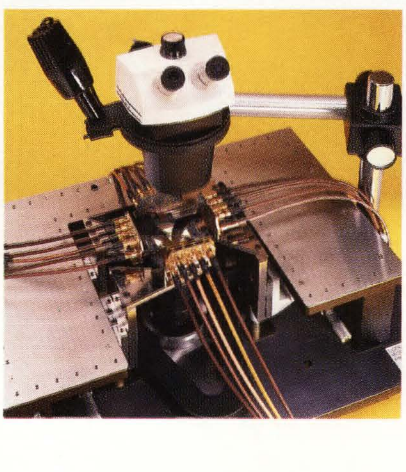

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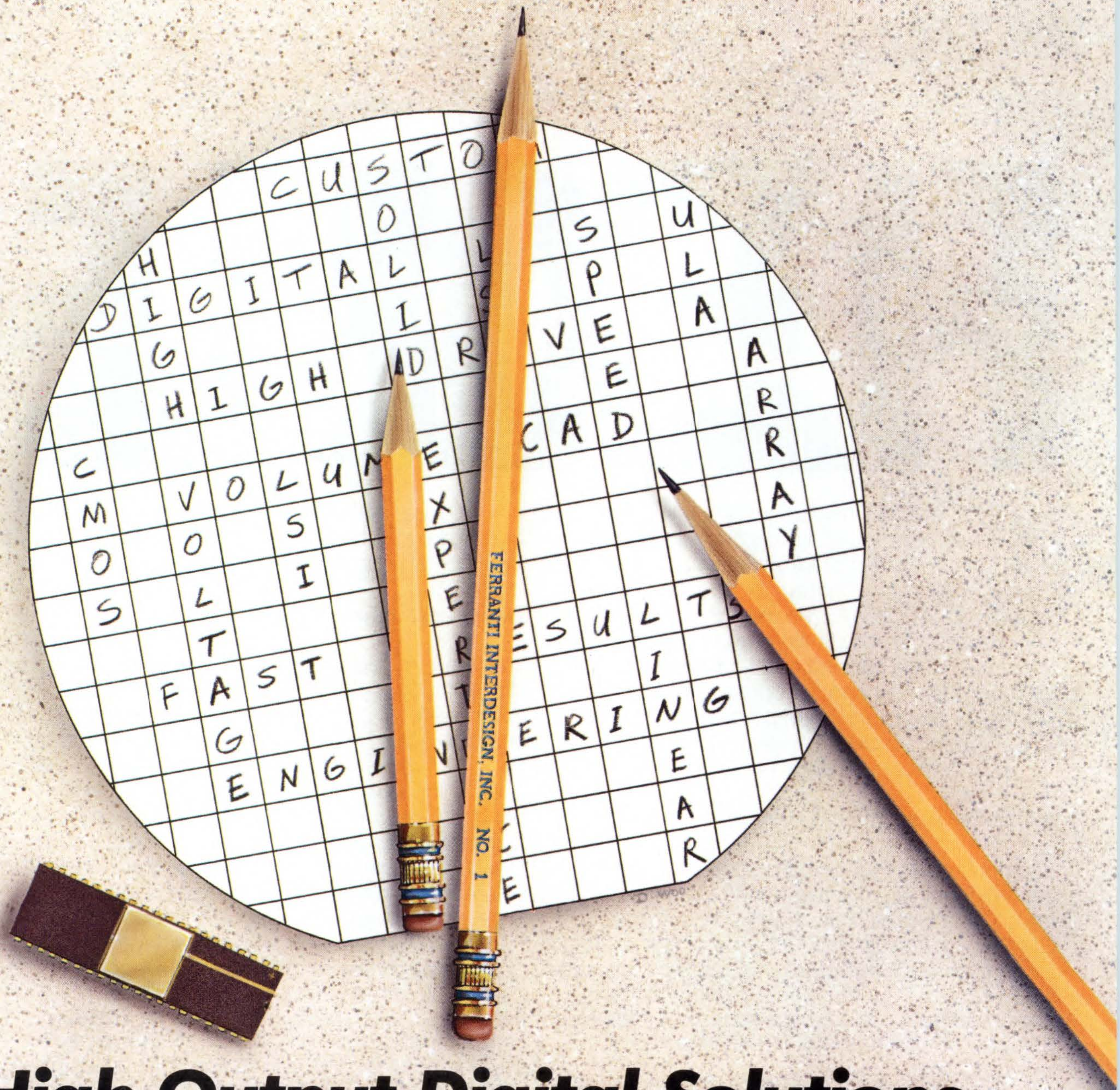
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Symbolic layout software accelerates IC design

Yuh-Zen Liao, Nang-Ping Chen, and Troy Gau
Ecad Inc., 2455 Augustine Dr., Santa Clara, CA 95054; (408) 727-0264.

For IC designers, little compares with the exhilaration of wrapping up a project. But few designers truly relish the idea of dealing with a conventional polygon editor at the final stages. Either they have to refer continually to an elaborate set of design and process rules or worse, they have to memorize the rules. To further aggravate the problem, they must manually draw the diffusion, polysilicon, and metal contact areas, always paying close attention to the detailed set of rules.

IC designers can see productivity rise with layout software that lets them work at the symbolic device level, not the polygon level. ICs arrive compact.

Standing in sharp contrast to polygon editing is symbolic layout, which allows IC designers to place and wire transistors in the same way circuit designers place and wire components on a schematic diagram. Sitting at a workstation, they can concentrate on the device level, without the tedium of hand-drawing the pertinent areas. The change pays off in productivity. Output rises anywhere from two to ten times. In fact, experienced IC designers can turn out more than 50 transistors a day with symbolic editing—a far cry from the 10 or 15 produced with conventional polygon editing.

When a symbolic layout editor is coupled with another automatic tool, one dedicated to creating the most compact layout consistent with process design rules, the result comes very close to that of hand-drawn, hand-packed designs. The Symbad system distinguishes itself as the first IC layout system that fully exploits the symbolic approach to IC design. Engineers can pick predrawn transistors—or even entire functional cell blocks—from a design library and simply interconnect them. The compactor automatically applies the appropriate spacing to the transistors and contacts.

Since process design rules are built into each transistor that Symbad compacts, the results are automatically correct by construction. More important, for those who question the silicon efficiency of symbolic editing, experience indicates that Symbad, teamed with a compactor, comes within 10% or 15% of a highly polished manual design (Fig. 1).

Nevertheless, symbolic editing has little chance of replacing polygon editing: Even in the age of precharacterized cell blocks and chips with hundreds of thousands of transistors, seasoned IC designers still must visually inspect and sometimes handtweak each transistor. So, to set itself up as an allround solution, Symbad also includes a polygon (geometric) editor. After compaction, symbolic data can be easily converted to polygon format for modification by the geometric editor.

Underlying the system's efficiency is an unusually structured, intelligent data base that all Symbad tools share. The common data base eliminates the net-list extraction and reformatting operations typically encountered when moving from activity to

activity, say, from layout editing to block placement and routing. Activities proceed almost independently, yet remain linked through the data base.

From still another angle, a built-in data-base manager takes on duties similar to an operating system. It relieves application software of file-management tasks; enables several users to access files concurrently, even through a network; and keeps track of files in use through time stamps and version numbers.

A BASIC OVERVIEW

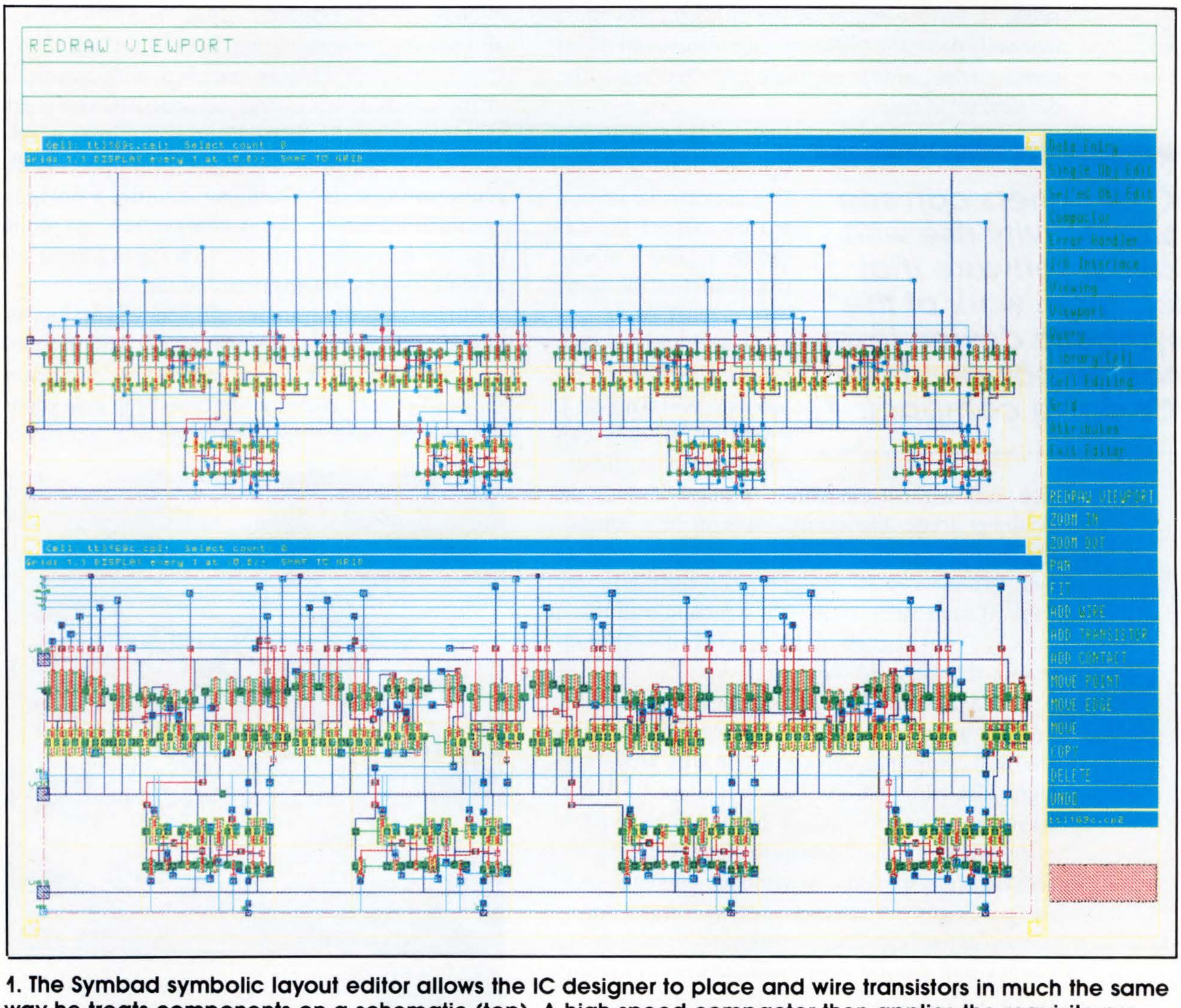
The Symbad system encompasses all aspects of IC design work, from the initial entry of data to the generation of mask tapes. An interactive interface gives designers complete control over layout, no matter what the level or step in the mask design process.

Designers interact with the system through a Tektronix 4115 or 4125 terminal (or a compatible Seiko 1104 or 1105 terminal) that is equipped with a mouse or graphics tablet.

In the future, Symbad will run with VAX GPX and Apollo workstations. For now runs on VAX minicomputers, including the MicroVAX II, under the VMS operating system. For top efficiency, it needs 5 Mbytes of main memory; the symbolic editor and associated libraries may require up to 400 Mbytes of disk space.

Symbad accepts Calma GDS II or CIF file inputs, as well as Tegas or Silogs net lists. Its outputs include GDS II stream or CIF tapes for mask generation or Versatec plotter outputs. (The Symbad tools are 100% compatible with Ecad's Dracula, a well-recognized design verification package.)

Symbad's hierarchical, full-function graphics editor works on three different levels: block, symbolic, and geometric. Block placement and routing software occupies the highest level; symbolic layout and editing software,



1. The Symbad symbolic layout editor allows the IC designer to place and wire transistors in much the same way he treats components on a schematic (top). A high-speed compactor then applies the requisite process design rules to find the smallest area of silicon (bottom).

the main level; and polygon editing, the lowest level.

Though the system is hierarchically organized, it controls the IC design process in a bottom-up fashion—that is, designers use transistors to build cells, then cells to build blocks, and finally blocks to build ICs. For extra convenience, they can create their own library models of transistors and other semiconductor devices using both templates supplied with Symbad and their own process design rules. Process-related information—such as layer definition, device construction and spacing rules—and system-wide parameters—such as scaling factors and measurement units—are contained in the technology file.

They can be entered in a textual format with a relatively simple syntax (Fig. 2). For example, the statement EXT POLY DIFFUSSION GE 2.0 means that the external spacing between the polysilicon and the diffusion area must be at least 2 μm.

After the technology file is coded, the Symbad technology file compiler translates the ASCII design rules for specific processes—NMOS, n-well and p-well CMOS, bipolar, even GaAs—into an internal binary format to which all Symbad application tools can refer.

VISUAL FEEDBACK

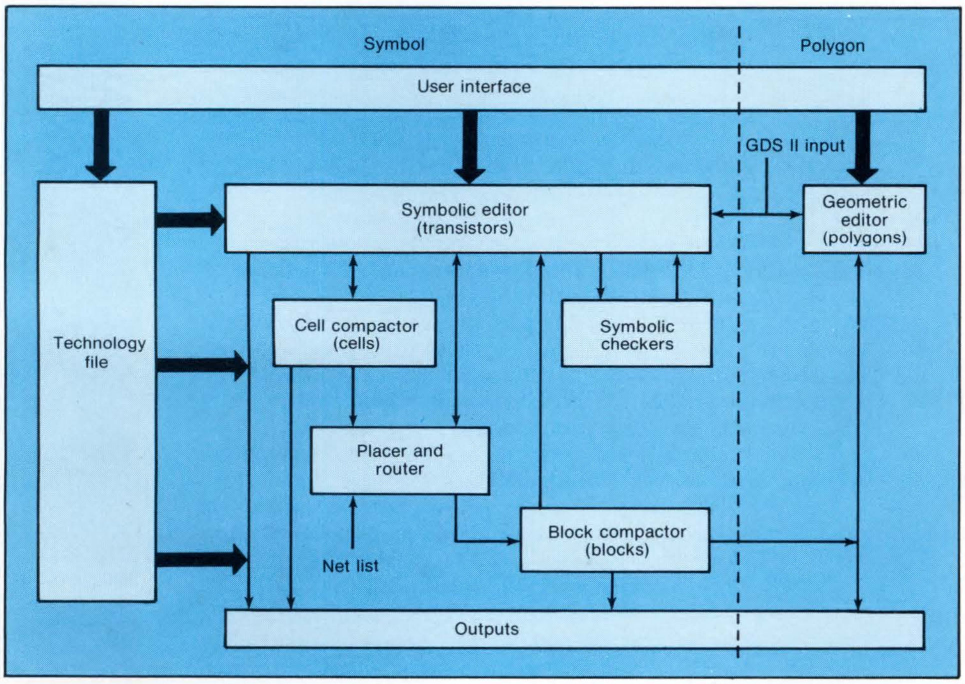
On the workstation or terminal screen, Symbad depicts transistors, contacts, and other fixed-size circuit elements in true geometric form, so that users get visual feedback of the physical relationships. After selecting and placing transistors, users then interconnect them with stretchable wires, which can be shown either in their true width or in short-hand form with only their center lines (Fig. 3).

Once the elements are chosen, placed, and routed, Symbad's cell compactor finds the smallest area consistent with the design rules supplied. Based on a constraint-graph algorithm, it negotiates the best compromise between speed and silicon area. As a gauge of its haste, it compacts a 2000-transistor design in only 5 minutes on a VAX-11/750. In fact, speed and design complexity enjoy an almost linear relationship: Doubling the number of objects means only slightly more than double the compaction time.

Designers can alter the compaction process by specifying contingencies—say, "jog" or "fence"—that in effect give the compactor more freedom. For instance, though a wire stretches lengthwise in only one direction, a user can identify a jog point at which the wire can stretch in another direction. The wire appears to take two 90° turns, yet within the software it is actually composed of three wire segments at right angles to each other.

Fences enclose a number of elements, so that they can be treated as a subunit in the context of the whole cell. By fencing in a group of functionally related objects, designers can limit the movements of group members and thus guarantee that they remain close to one another.

User and internal design rule constraints make up all the contingencies of the layout. Dimensional constraints, for example, can be specified if a designer wants to build a family of cells of the same height or width—standard



2. The Symbad software modules are linked through a common intelligent database. The user can move from symbolic layout editing to block placement-and-routing (and back again) without re-compiling his data. In addition, the database can accept GDS II or CIF formatted files, as well as Tegas or Silos netlists.

cells, in other words. With restrictions, the pin pads of one cell can be matched with those of other cells to ensure smooth abutment or easy connection to an external bus.

The block compactor, a subset of the Symbad compactor, is noteworthy for its ability to fix overcongestion. To do so, it automatically inserts jogs on any wires that limit the movement of blocks and interconnections. The compactor guarantees that the compacted result is 100% design rule correct. Once Symbad constructs and compacts cells, programs for block placement and routing, editing, and block compaction all can use them as functional blocks.

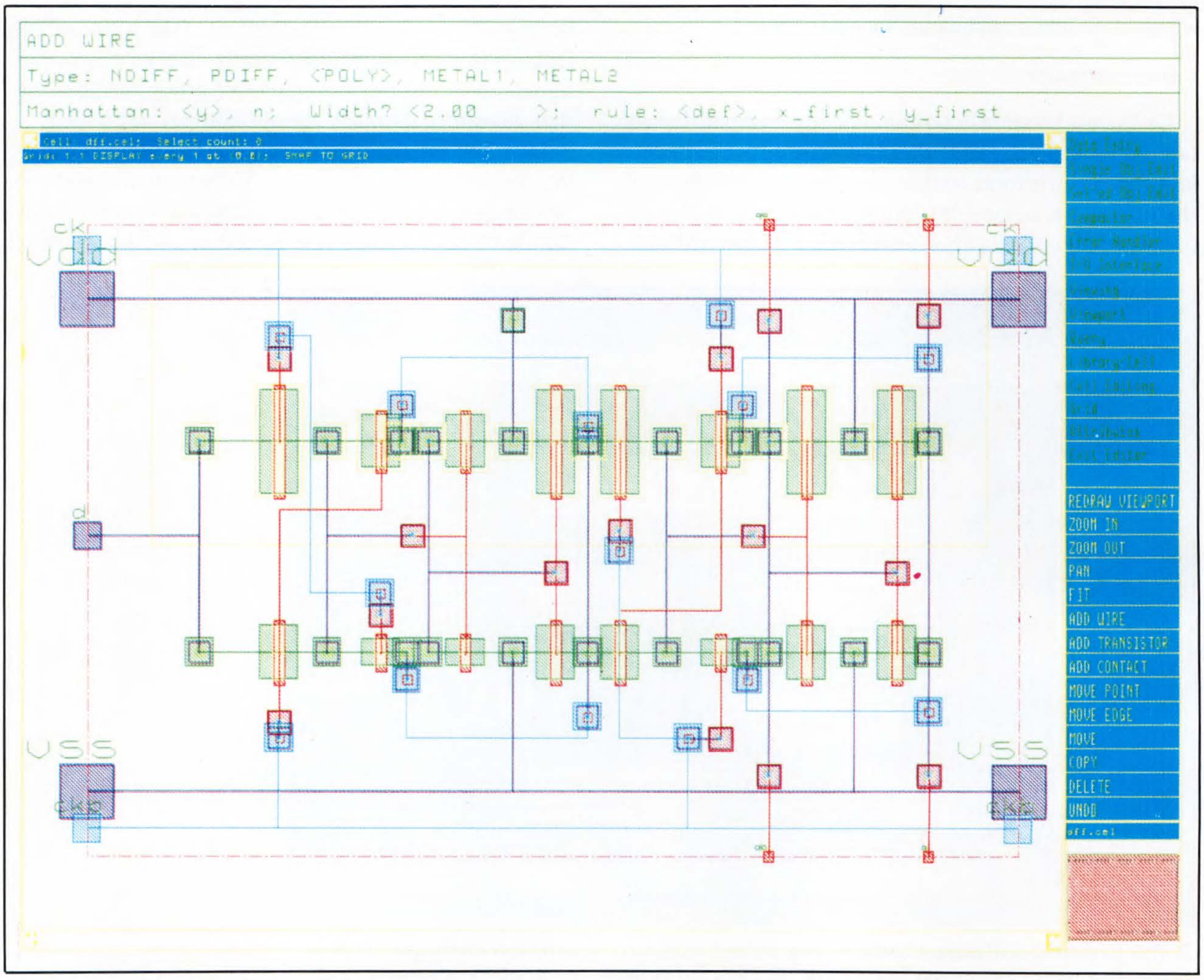
CHIP OFF THE OLD BLOCK

Symbad's block placer-router assembles functional blocks generated either by the system's design tools (say, the symbolic layout editor) or by other layout tools. Symbad's import mechanism compiles a Tegas or Silogs net list or a completely laid out block in either a GDS II stream or CIF format.

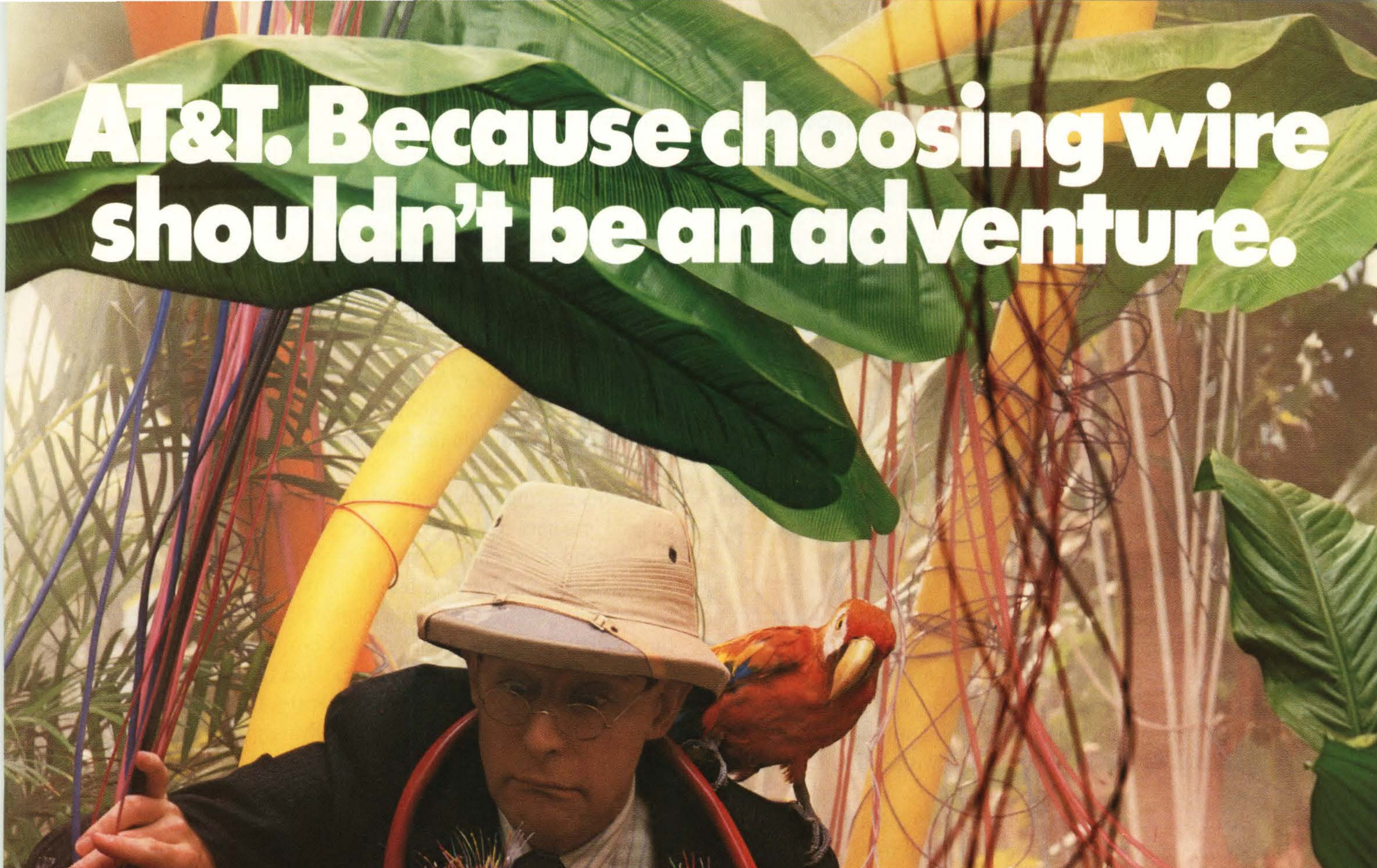
Designers can position predefined blocks by hand, or they can leave the job to Symbad's placer, which arranges and orients blocks of any height or width according to block size and shape, pinouts, and interconnections. Governing its execution is one goal: to make the layout as efficient as possible in the least amount of silicon. Of course, designers also must identify those wire nets whose length is critical to the performance of a part. The placer then attempts to keep the identified paths as short as possible.

Initially the software places and routes the blocks—automatically or interactively—without referring to design rules, using only the connectivity information housed in the data base. Then the block compactor steps in to apply a specific set of design rules. Though that process runs automatically, the user can intervene at any time to modify or fine-tune the machine's decisions.

In operation, the placer first makes a floor plan, using only the connections identified by the net list, the physical outlines of the block, and the location and layers of the bonding pads. The most densely connected blocks are



3. Symbad generally depicts transistors and contacts by their true geometric dimensions on the user screen. Wires, however, can be represented simply by their center lines.


AT&T. Because choosing wire shouldn't be an adventure.

clustered and arranged in a pseudo row structure, in which the channel widths vary by the density of the interconnection paths (Fig. 4). A global path-assignment algorithm estimates the routing area between blocks.

With the help of "fly lines," straight lines drawn between pin pads on the same net, designers can visualize the signal flow and assess the quality of the placement. By issuing the Move, Rotate, and Mirror commands for individual blocks and by making selections from the command menu, they can work toward better placement before automatic routing begins. The system guarantees 100% routing—regardless of the initial block placement.

BLOCK ADJUSTMENT

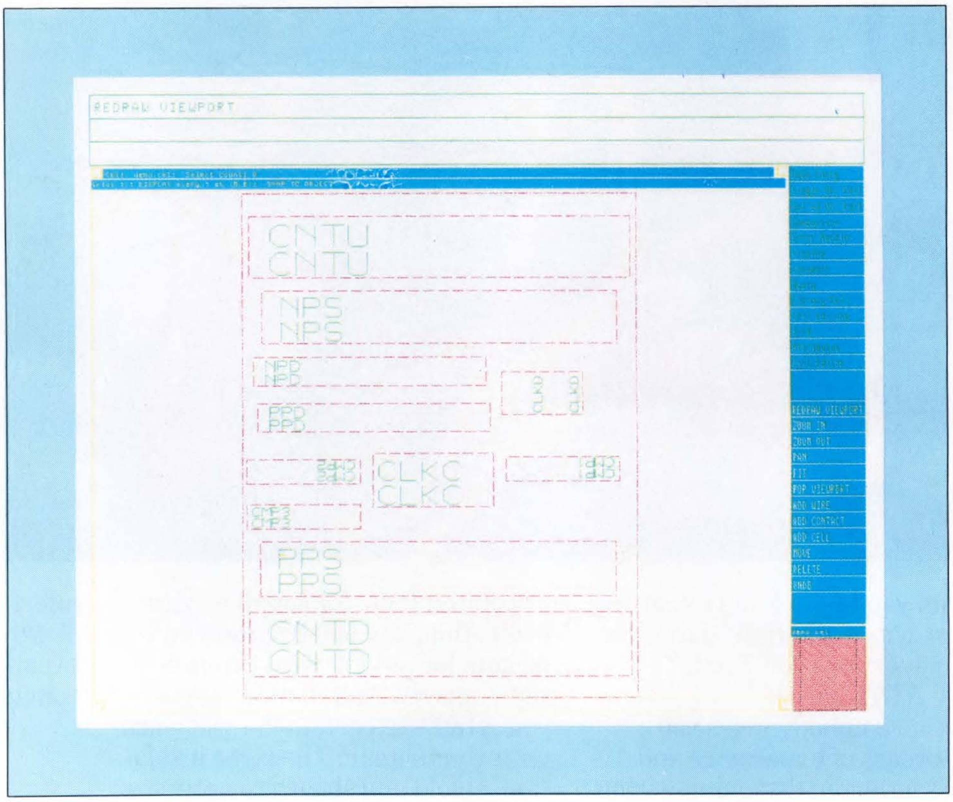
The routing areas of a manually modified placement may not accurately reflect the space required for physical routing, since it is difficult for human designers to predict the space easily. However, designers can request the system to perform a global routing and automatically adjust the blocks to show the placement with estimated routing areas.

The Symbad router relies on two algorithms, one for channel routing and the other for switch-box routing. The channel router focuses on the region between fixed-pinout boundaries of two neighboring blocks. The open ends of the channel allow signals to flow in and out. The switch-box router works in areas where channels intersect. These junctions typically have signals on all sides. The router connects the signals from side-to-side like a switch box; hence the name "switchbox routing".

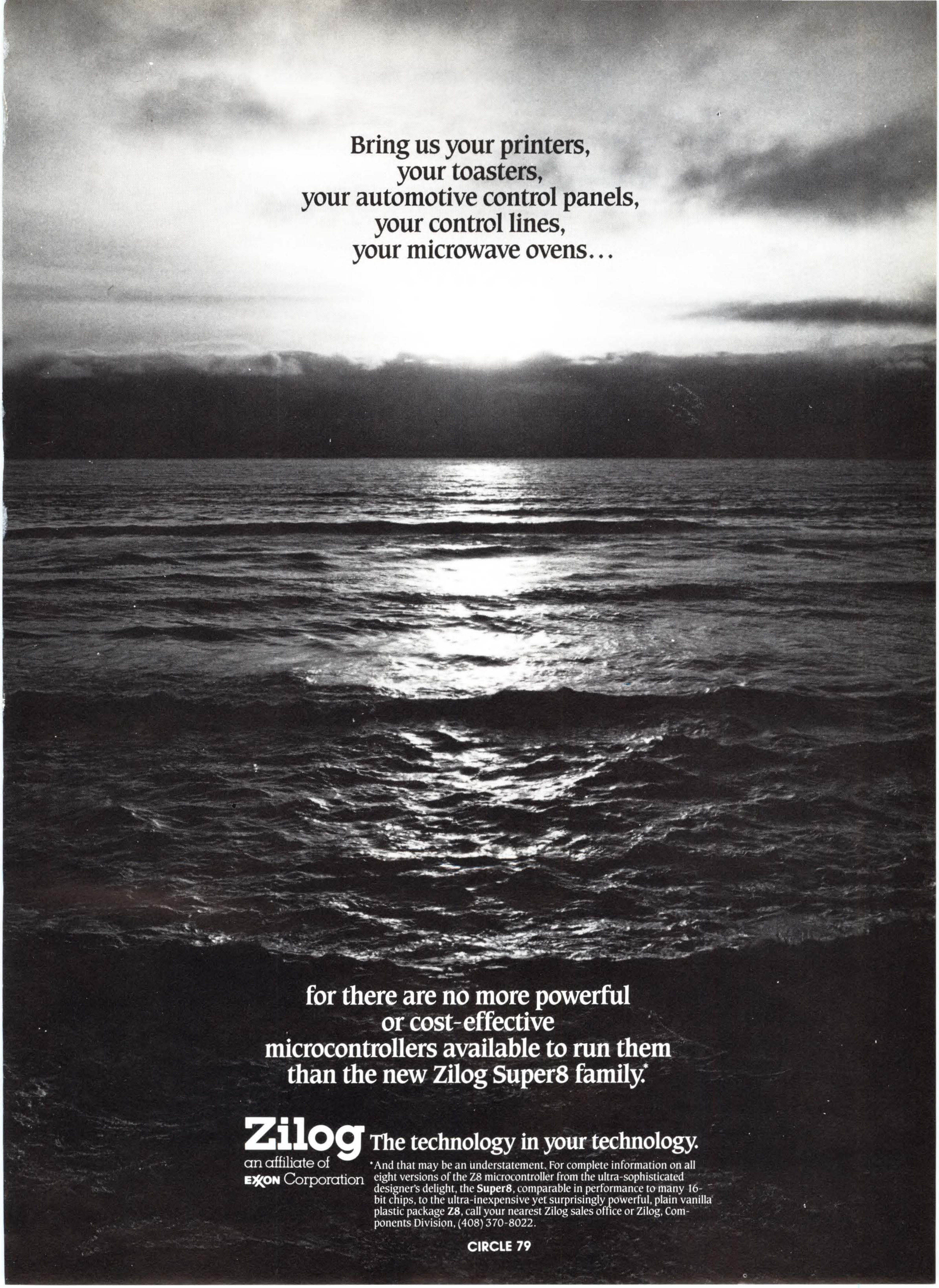
Overall the Symbad router implements the physical interconnections with the shortest wire length and the smallest routing area. Moreover, it works with rectangular blocks of arbitrary shape and size, and it imposes no artificial restrictions on the locations and layers of the terminals.

Besides routing individual nets, the program also routes buses. Here nets are bundled together to minimize capacitive loading differences between the wires. The router is sensitive not only to wire length, but also to local congestion. In operation, it avoids locally congested channels for noncritical nets, preventing block positions from being significantly different after compaction than they were during initial placement. Consequently, the user must weigh trade-offs between minimum wire length and channel congestion before putting the router in gear.

At any time during automatic routing, designers can get in on the action. Instead of letting the software route all nets automatically, they can hand-wire a single net or single bus—say, to control a critical timing path—and let the system take care of the remaining nets. Moreover, with any routing operation designers can direct the soft-



4. The automatic placement program arranges cell blocks in row clusters according to the density of their interconnections. Blocks packing the most interconnections are situated closest together. The dimensions of the routing channel are estimated by a global path-assignment algorithm.



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CIRCLE 79

Price and availability

The block placement and routing software will be available this month, with prices starting at $75,000. Transistor-level design software will follow soon after. **CIRCLE 504**

ware to use a preferred layer for traces in the major channel direction and a secondary layer for the jogs or pin pads; set the wire widths for the two layers individually; or tell the router to follow a prescribed path or to avoid certain areas. Every time the router receives a command, it extracts the positions of the existing blocks and interconnections before it actually embarks on the task. It treats existing wires like obstacles.

SPACE-ADEPT

The router relies on the underlying symbolic data base to bypass the traditional speed limitations of conventional routing programs. In the Symbad environment, spacing between objects is finalized only after compaction, so the machine spends significantly less time attempting to resolve design rules than would a router without the benefit of compaction. The latter, for example, would have to calculate the physical coordinates of each interconnection line before it could generate a layout that adheres to design rules.

Besides that, if the routing space estimated during placement differed from the actual routing required, the conventional router either would have to shift the blocks to accommodate the physical width of the wire or would have to shrink the routing area to reduce the slack. Those time-consuming computations preclude interactivity and force the routers to operate only in the batch mode. □

Yuh-Zen Liao, a principal member of Ecad's technical staff, is an expert on compaction software, an area he also explored at Singer Link and IBM. He earned his doctoral degree from the University of California at Berkeley.

Ecad's expert on autorouting, Nang-Ping Chen gained experience in Hewlett-Packard's computer-aided design group and at the University of California at Berkeley, where he earned his PhD and wrote papers on block routing.

Troy Gau, an IC designer at Ecad, previously worked at Integrated Device Technology and Hewlett-Packard. He holds a BSEE from San Jose State University.

How valuable?	Circle
Highly	541
Moderately	542
Slightly	543

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LW SERIES
VOLTAGE AND CURRENT RATINGS—CONT'D
DC INPUT. SINGLE OUTPUT.

DC INPUT 20.0-40.0 VDC

MODEL	REGULATION (line, load)	RIPPLE (mV pk-pk)	MAX CURRENT IN AMPS (MAX WATTAGE IN WATTS) 40°C	50°C	60°C	PKG. SIZE	DIMENSIONS (inches)	PRICE QTY. 1	QTY. 100	QTY. 1000
4.75-16 VOLTS ADJ.										
LWS-295-5	0.1%, 0.4%	100	5.0(25)	4.3(21.5)	3.6(18)	95	2.5 x 4.5 x 1.5	$150	$127	$95
15-30 VOLTS ADJ.										
LWS-295-24	0.1%, 0.4%	200	1.65(25)	1.4(21.5)	1.2(18)	95	2.5 x 4.5 x 1.5	150	127	95
20-40 VOLTS ADJ.										
LWS-296-28	0.1%, 0.4%	200	2.5(50)	2.1(42)	1.8(36)	95	2.5 x 4.5 x 1.5	200	170	127
30-60 VOLTS ADJ.										
LWS-296-48	0.1%, 0.4%	200	1.67(50)	1.4(42)	1.2(36)	95	2.5 x 4.5 x 1.5	200	170	127

DC INPUT 20.0-60.0 VDC

4.75-16 VOLTS ADJ.										
LWS-394-5	0.1%, 0.4%	100	3.0(15)	2.6(12)	2.3(11.5)	94	1.25 x 3.5 x 2.5	$119	$101	$75
15-30 VOLTS ADJ.										
LWS-394-24	0.1%, 0.4%	200	1.0(15)	0.9(13)	0.75(11.5)	94	1.25 x 3.5 x 2.5	119	101	75

DC INPUT 30.0-60.0 VDC

4.75-16 VOLTS ADJ.										
LWS-395-5	0.1%, 0.4%	100	5.0(25)	4.3(21.5)	3.6(18)	95	2.5 x 4.5 x 1.5	$150	$127	$95
15-30 VOLTS ADJ.										
LWS-395-24	0.1%, 0.4%	200	1.65(25)	1.4(21.5)	1.2(18)	95	2.5 x 4.5 x 1.5	150	127	95
20-40 VOLTS ADJ.										
LWS-397-28	0.1%, 0.4%	200	3.0(60)	2.5(50)	2.1(42)	95	2.5 x 4.5 x 1.5	200	170	127
30-60 VOLTS ADJ.										
LWS-397-48	0.1%, 0.4%	200	2.0(60)	1.67(50)	1.4(42)	95	2.5 x 4.5 x 1.5	200	170	127

DC INPUT. DUAL OUTPUT.
DC INPUT 5V ±10%

MODEL	Vo	REGULATION (line, load)	RIPPLE (mV pk-pk)	MAX CURRENT IN AMPS 40°C	50°C	60°C	PKG. SIZE	DIMENSIONS (inches)	PRICE QTY. 1	QTY. 100	QTY. 1000
±12 VOLTS ±3% FIXED											
LWD-191-12	±12	0.2%, 0.2%	120	.060	.060	.060	D-91	1.77 x 1.19 x .40	$62	$49	$25.50
LWD-192-12	±12	0.2%, 0.2%	120	.120	.120	.084	D-92	1.85 x 1.85 x .47	76	60	31.00
±15 VOLTS ±3% FIXED											
LWD-191-15	±15	0.2%, 0.2%	150	.050	.050	.050	D-91	1.77 x 1.19 x .40	62	49	25.50
LWD-192-15	±15	0.2%, 0.2%	150	.100	.100	.070	D-92	1.85 x 1.85 x .47	76	60	31.00

DC INPUT 12V ±10%

±12 VOLTS ±3% FIXED											
LWD-291-12	±12	0.2%, 0.2%	120	.060	.060	.060	D-91	1.77 x 1.19 x .40	$62	$49	$25.50
LWD-292-12	±12	0.2%, 0.2%	120	.120	.120	.084	D-92	1.85 x 1.85 x .47	76	60	31.00
±15 VOLTS ±3% FIXED											
LWD-291-15	±15	0.2%, 0.2%	150	.050	.050	.050	D-91	1.77 x 1.19 x .40	62	49	25.50
LWD-292-15	±15	0.2%, 0.2%	150	.100	.100	.070	D-92	1.85 x 1.85 x .47	76	60	31.00

DC INPUT 24V ±10%

±12 VOLTS ±3% FIXED											
LWD-391-12	±12	0.2%, 0.2%	120	.060	.060	.060	D-91	1.77 x 1.19 x .40	$62	$49	$25.50
LWD-392-12	±12	0.2%, 0.2%	120	.120	.120	.084	D-92	1.85 x 1.85 x .47	76	60	31.00
±15 VOLTS ±3% FIXED											
LWD-391-15	±15	0.2%, 0.2%	150	.050	.050	.050	D-91	1.77 x 1.19 x .40	62	49	25.50
LWD-392-15	±15	0.2%, 0.2%	150	.100	.100	.070	D-92	1.85 x 1.85 x .47	76	60	31.00

LW SERIES: Specifications

DC OUTPUT
Voltage range shown in tables.

REGULATED VOLTAGE

regulation, line .... 0.1% from minimum to maximum and from maximum to minimum. 0.5% on LWS-190, 191, 290, 291, 390, 391. 0.2% on both outputs of dual output models for input variations from 21.6 to 26.4 VDC or 26.4 to 21.6 VDC on LWD-391, 392; from 10.8 to 13.2 VDC or 13.2 to 10.8 VDC on LWD-291, 292; from 4.5 to 5.5 VDC or 5.5 to 4.5 VDC on LWD-191, 192.

regulation, load .... 0.4% for load variations from no load to full load and full load to no load. 1.0% on LWS-190, 191, 290, 291, 390, 391. 0.2% on dual output models.

ripple and noise .... 20mV RMS, 100mV pk-pk for -5 models of LWS-193, 194, 195, 294, 295, 394, 395.
120mV pk-pk for 5V models of LWS-190, 191, 290, 291, 390, 391 and 12V models of LWD-191, 192, 291, 292, 391, 392.
150mV pk-pk for 12V models of LWD-191, 192, 291, 292, 391, 392 and 12V and 15V models of LWS-190, 191, 290, 291, 390, 391.
25mV RMS, 200mV pk-pk for all other models.

efficiency .... LWS-194, LWS-294, LWS-394, and LWS-193: 50% minimum
LWS-195: 57% minimum
LWS-190: 58% minimum
LWS-191: 60% minimum
LWS-391: 64% minimum
LWS-390: 67% minimum
LWS-291: 68% minimum
LWS-290: 70% minimum
LWS-296, 397: 75% minimum

temp. coeff. .... 0.03% / °C. 0.02% on LWS-190, 191, 290, 291, 390, 391 and on all dual output models.

AMBIENT OPERATING TEMPERATURE
Continuous duty 0 to +60°C with suitable derating above 40°C for LWS-193, 194, 195, 294, 295, 296, 394, 395, 397, and dual output models. Continuous duty −5°C to +60°C with suitable derating above 45°C for LWS-191, 291, 391. Continuous duty −5°C to +65°C with suitable derating above 50°C for LWS-190, 290, 390.

OVERLOAD PROTECTION
External overload protection. Automatic electronic current limiting circuit limits the output current to a preset value, thereby providing protection for the load as well as the power supply.

STORAGE TEMPERATURE RANGE
−55°C to +85°C. −20°C to +85°C for LWS-190, 191, 290, 291, 390, 391. −30°C to +85°C on all dual output models.

OVERSHOOT
No overshoot at turn-on, turn-off, or power failure.

COOLING
All units are convection cooled. No fans or blowers needed.

MOUNTING
PC board mountable. Refer to outline drawings in catalog.

OUTPUT VOLTAGE ADJUST
LWS-193, 194, 195, 294, 295, 296, 394, 395, 397
Output voltage can be set to desired value within the entire range by inserting a resistor between +V and RP terminals. Resistor can be selected as per equations supplied in instruction manual.

INPUT / OUTPUT CONNECTIONS
DC input and outputs are via pin type connections. Refer to outline drawings in catalog.

ISOLATION RATING
1500 VDC on LWS-394, 395, 397.
500 VDC on all other models.

PHYSICAL DATA

Package Model	Weight Lbs. Net	Weight Lbs. Ship	Size Inches
LWS-190, 290, 390	.10	.12	1.85 x 1.85 x 0.47
LWS-191, 291, 391	.16	.19	1.85 x 1.85 x 0.75
LWS-193	.65	.90	2.50 x 3.50 x 1.25
LWS-194, 294, 394	.65	.90	2.50 x 3.50 x 1.25
LWS-195, 295, 395	.75	1.00	2.50 x 4.50 x 1.50
LWS-296	.75	1.00	2.50 x 4.50 x 1.50
LWS-397	.75	1.00	2.50 x 4.50 x 1.50
LWD-191, 291, 391	.06	.10	1.77 x 1.19 x .40
LWD-192, 292, 392	.09	.12	1.85 x 1.85 x .47

UL / CSA
Under evaluation

GUARANTEE
90 day guarantee includes labor as well as parts.

LW SERIES
VOLTAGE AND CURRENT RATINGS
DC INPUT. SINGLE OUTPUT.

DC INPUT 4.5-6.0 VDC

MODEL	REGULATION (line, load)	RIPPLE (mV pk-pk)	MAX CURRENT IN AMPS 45°C	50°C	60°C	65°C	PKG. SIZE	DIMENSIONS (inches)	PRICE QTY. 1	QTY. 100	QTY. 1000
5V ±5% NON-ADJ.											
LWS-190-5	0.5%, 1.0%	120	0.5	0.5	—	0.200	90	1.85 x 1.85 x 0.47	$49	$39	$21
LWS-191-5	0.5%, 1.0%	120	1.0	—	0.400	—	91	1.85 x 1.85 x 0.75	59	47	25
12V ±5% NON-ADJ.											
LWS-190-12	0.5%, 1.0%	150	0.21	0.21	—	0.084	90	1.85 x 1.85 x 0.47	49	39	21
LWS-191-12	0.5%, 1.0%	150	0.42	—	0.168	—	91	1.85 x 1.85 x 0.75	59	47	25
15V ±5% NON-ADJ.											
LWS-190-15	0.5%, 1.0%	150	0.17	0.17	—	0.060	90	1.85 x 1.85 x 0.47	49	39	21
LWS-191-15	0.5%, 1.0%	150	0.34	—	0.136	—	91	1.85 x 1.85 x 0.75	59	47	25

DC INPUT 4.5-10.0 VDC

MODEL	REGULATION (line, load)	RIPPLE (mV pk-pk)	MAX CURRENT IN AMPS (MAX WATTAGE IN WATTS) 40°C	50°C	60°C	PKG. SIZE	DIMENSIONS (inches)	PRICE QTY. 1	QTY. 100	QTY. 1000
4.75-16 VOLTS ADJ.										
LWS-193-5	0.1%, 0.4%	100	2.0(10)	1.7(8.5)	1.5(7.5)	94	1.25 x 3.5 x 2.5	$89	$76	$62
LWS-194-5	0.1%, 0.4%	100	3.0(15)	2.6(12)	2.3(11.5)	94	1.25 x 3.5 x 2.5	119	101	75
15-30 VOLTS ADJ.										
LWS-193-24	0.1%, 0.4%	200	0.65(10)	0.57(8.5)	0.50(7.5)	94	1.25 x 3.5 x 2.5	89	76	62
LWS-194-24	0.1%, 0.4%	200	1.00(15)	0.90(13)	0.75(11.5)	94	1.25 x 3.5 x 2.5	119	101	75

DC INPUT 10.0-15.0 VDC

MODEL	REGULATION (line, load)	RIPPLE (mV pk-pk)	MAX CURRENT IN AMPS 45°C	50°C	60°C	65°C	PKG. SIZE	DIMENSIONS (inches)	PRICE QTY. 1	QTY. 100	QTY. 1000
5V ±5% NON-ADJ.											
LWS-290-5	0.5%, 1.0%	120	0.60	0.60	—	0.24	90	1.85 x 1.85 x 0.47	$49	$39	$21
LWS-291-5	0.5%, 1.0%	120	1.20	—	0.48	—	91	1.85 x 1.85 x 0.75	59	47	25
12V ±5% NON-ADJ.											
LWS-290-12	0.5%, 1.0%	150	0.25	0.25	—	0.10	90	1.85 x 1.85 x 0.47	49	39	21
LWS-291-12	0.5%, 1.0%	150	0.50	—	0.20	—	91	1.85 x 1.85 x 0.75	59	47	25
15V ±5% NON-ADJ.											
LWS-290-15	0.5%, 1.0%	150	0.20	0.20	—	0.08	90	1.85 x 1.85 x 0.47	49	39	21
LWS-291-15	0.5%, 1.0%	150	0.40	—	0.16	—	91	1.85 x 1.85 x 0.75	59	47	25

DC INPUT 10.0-20.0 VDC

MODEL	REGULATION (line, load)	RIPPLE (mV pk-pk)	MAX CURRENT IN AMPS (MAX WATTAGE IN WATTS) 40°C	50°C	60°C	PKG. SIZE	DIMENSIONS (inches)	PRICE QTY. 1	QTY. 100	QTY. 1000
4.75-16 VOLTS ADJ.										
LWS-195-5	0.1%, 0.4%	100	5.0(25)	4.3(21.5)	3.6(18)	95	2.5 x 4.5 x 1.5	$150	$127	$95
15-30 VOLTS ADJ.										
LWS-195-24	0.1%, 0.4%	200	1.65(25)	1.4(21.5)	1.2(18)	95	2.5 x 4.5 x 1.5	150	127	95

DC INPUT 10.0-30.0 VDC

4.75-16 VOLTS ADJ.										
LWS-294-5	0.1%, 0.4%	100	3.0(15)	2.6(13)	2.3(11.5)	94	1.25 x 3.5 x 2.5	$119	$101	$75
15-30 VOLTS ADJ.										
LWS-294-24	0.1%, 0.4%	200	1.0(15)	0.9(13)	0.75(11.5)	94	1.25 x 3.5 x 2.5	119	101	75

DC INPUT 20.0-30.0 VDC

MODEL	REGULATION (line, load)	RIPPLE (mV pk-pk)	MAX CURRENT IN AMPS 45°C	50°C	60°C	65°C	PKG. SIZE	DIMENSIONS (inches)	PRICE QTY. 1	QTY. 100	QTY. 1000
5V ±5% NON-ADJ.											
LWS-390-5	0.5%, 1.0%	120	0.60	0.60	—	0.24	90	1.85 x 1.85 x 0.47	$49	$39	$21
LWS-391-5	0.5%, 1.0%	120	1.20	—	0.48	—	91	1.85 x 1.85 x 0.75	59	47	25
12V ±5% NON-ADJ.											
LWS-390-12	0.5%, 1.0%	150	0.25	0.25	—	0.10	90	1.85 x 1.85 x 0.47	49	39	21
LWS-391-12	0.5%, 1.0%	150	0.50	—	0.20	—	91	1.85 x 1.85 x 0.75	59	47	25
15V ±5% NON-ADJ.											
LWS-390-15	0.5%, 1.0%	150	0.20	0.20	—	0.08	90	1.85 x 1.85 x 0.47	49	39	21
LWS-391-15	0.5%, 1.0%	150	0.40	—	0.16	—	91	1.85 x 1.85 x 0.75	59	47	25

ELECTRONIC DESIGN EXCLUSIVE

6-GHz analog transistors, ECL team up in versatile array

Robert Sparkes and Winthrop Gross
Tektronix, Inc., P.O. Box 500, Beaverton, OR 97077; (503) 627-2515.

In monolithic structures, analog and digital circuits make uneasy bedfellows. Digital circuitry takes large numbers of small-geometry transistors, some specific resistor values, and not much else. Designing a digital circuit with an analog array, while not quite so unproductive as trying to fit a square peg into a round hole, often results in poor use of the device and a waste of precious space on the chip.

Gate arrays, on the other hand, without pnp transistors, high-value or thin-film resistors, capacitors, and other components, are even less suitable for analog applications. Even a chipful of npn transistors—a bipolar gate array's strong suit—is of little help, since these are all small, low-current devices. In chip design, analog and digital functions might stay forever apart were it not for the growing number of applications demanding both technologies in close proximity.

Putting superfast analog and digital elements on a single bipolar chip gives designers a precise, high-density ASIC, with reduced power.

Combining analog and digital functions on one monolithic IC, the QuickChip 4, profits designers by shortening the distance required for interfacing between the two sections. The combination cuts out interconnection parasitic effects and delays, and because the interface between the two sections is at a higher impedance level, the chip uses less power—all of which improves reliability. Further, more functions exist in a smaller space, which makes for easier packaging.

The QuickChip 4 IC brings together the QuickChip 2 6 GHz analog array and an ECL gate array, both of which are fabricated with the same IC process and use the same design rules (Fig. 1). Although the process was developed for analog applications, it produces high-speed and high-density ECL elements. The result is an analog array with more than 290 very fast npn transistors (f_T typically 6.5 GHz), along with a high-speed ECL gate array (up to 500-MHz clock rate) with over 300 equivalent gates.

The complexities of the combined array make good simulation essential in aiming for first-time success. To help the designer anticipate the system's performance, two simulators accompany QuickChip 4: Tlogs for logic and timing and Tspice for circuits. Tlogs analyzes the chip's testability, and Tspice, an enhanced version of Spice 2G, has powerful plotting and analysis routines and good numerical convergence.

The design package includes three model libraries: one for Tspice that covers all analog components, one for the Tlogs logic that covers standard digital functions in the gate-array portion, and the third a Tspice circuit library for the standard digital cells. This last can simulate the interface dynamics between the IC's digital and analog portions.

For layout design, the QuickChip 4 IC design package includes QuicKic, an interactive graphics editor that routes metal interconnections. A grid layout system, in which the grid equals the minimum metal pitch (7 μm), simplifies layout rules.

The IC's analog portion consists of an array of uncommitted bipolar transistors, capacitors, and resistors. The npn transistors have a 6.5-GHz f_T with high current-drive capability (up to 30 mA per large device) and moderate collector-base and collector-substrate breakdown voltages (BV_{CBO} = 15 V, BV_{CS} = 32 V). The IC process used also provides excellent V_{BE} matching, well-characterized pnp transistors, zener diodes, and implanted resistors. For precision applications, or when absolute impedance levels are important, there are optional thin-film nichrome resistors which can be laser-trimmed to 0.01%.

An array of 15 tiles gives the analog section ample space for supply busing and nichrome resistors. Each tile contains 18 npn and 10 pnp transistors and a versatile assortment of implanted resistors.

The ECL gate array portion of the QuickChip 4

IC, however, packs four times more npn transistors into its half of the IC, compared with the analog half. It bases its digital design on the placement of predesigned and characterized cells in appropriate core or I/O sites. The gate-array tiles connect through two layers of gold as do the analog tiles, with via holes in the intervening dielectric layer. Library cells include OR, NOR, NAND, and AND gates, D flip-flops, latches, and multiplexers, besides the ECL and TTL I/O cells. Typical propagation delays are in the range of 300 to 400 ns; the D flip-flops toggle at 500 MHz.

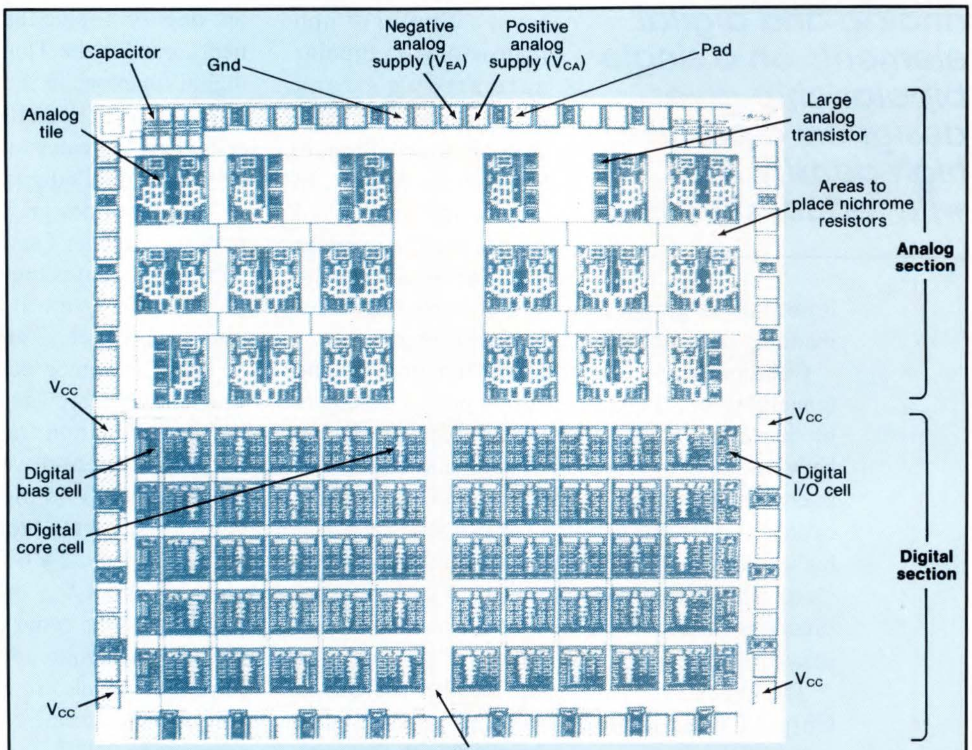
TRIGGERING AN EXAMPLE

A high-speed trigger circuit for a portable oscilloscope demonstrates the combined analog-digital array's capabilities. The circuit generates a stable ECL transition when the input signal passes a voltage threshold that the user sets with an external potentiometer. The circuit accepts five analog input channels (Fig. 2) selected by a TTL input. The trigger design exhibits less than 50-ps jitter in the sweep trigger mode, with a 300-MHz input signal. A trigger must occur only on one slope—also specified by the user over a serial data bus—of the input signal.

In an oscilloscope, the trigger circuit determines when the electron beam will be deflected horizontally across the face of the CRT. In most, the deflection occurs at a constant speed determined by the sweep circuit. A viewer usually wants to see the waveform in a particular time window or sweep duration, and the trigger circuit sets the window accordingly. When the trigger signal crosses the voltage threshold, the trigger fires and starts the sweep. The crossing may be fast or slow; it may occur once only, or it may repeat at widely varying frequencies. But the trigger circuit must fire as consistently as possible, particularly on repetitive signals, so that the waveform remains stationary on the screen.

The triggering signal can come from one of several sources. It can also be filtered and set for a maximum trigger-repeat rate. Each time the user changes one of the front-panel controls, a serial data word is loaded into a shift register on the IC to set the switch combination.

In the normal sweep-trigger mode, a hold-off command allows the sweep to reset and settle before sweeping again. The IC has an ECL trigger driven by arm and trigger comparators. Further, a hysteresis generator improves the stability of the gate output (TG) by guaranteeing that it always makes the same transition with respect to the analog input signal. The circuit detects two threshold crossings in a row, firing on the second. The first threshold crossing sets the arm latch; the second, the trig-



1. A high-speed bipolar array integrates analog and digital functions on one chip. Providing tighter packing density and greater reliability than separate ICs, the chip's analog npn transistors have an f_T of 6.5 GHz, while the digital section operates at up to a 500-MHz clock rate.

ger latch.

The trigger circuit also has a comparator mode that functions more simply than the normal sweep-trigger mode. It detects a single threshold crossing in the appropriate direction and resets when the threshold is crossed the opposite way.

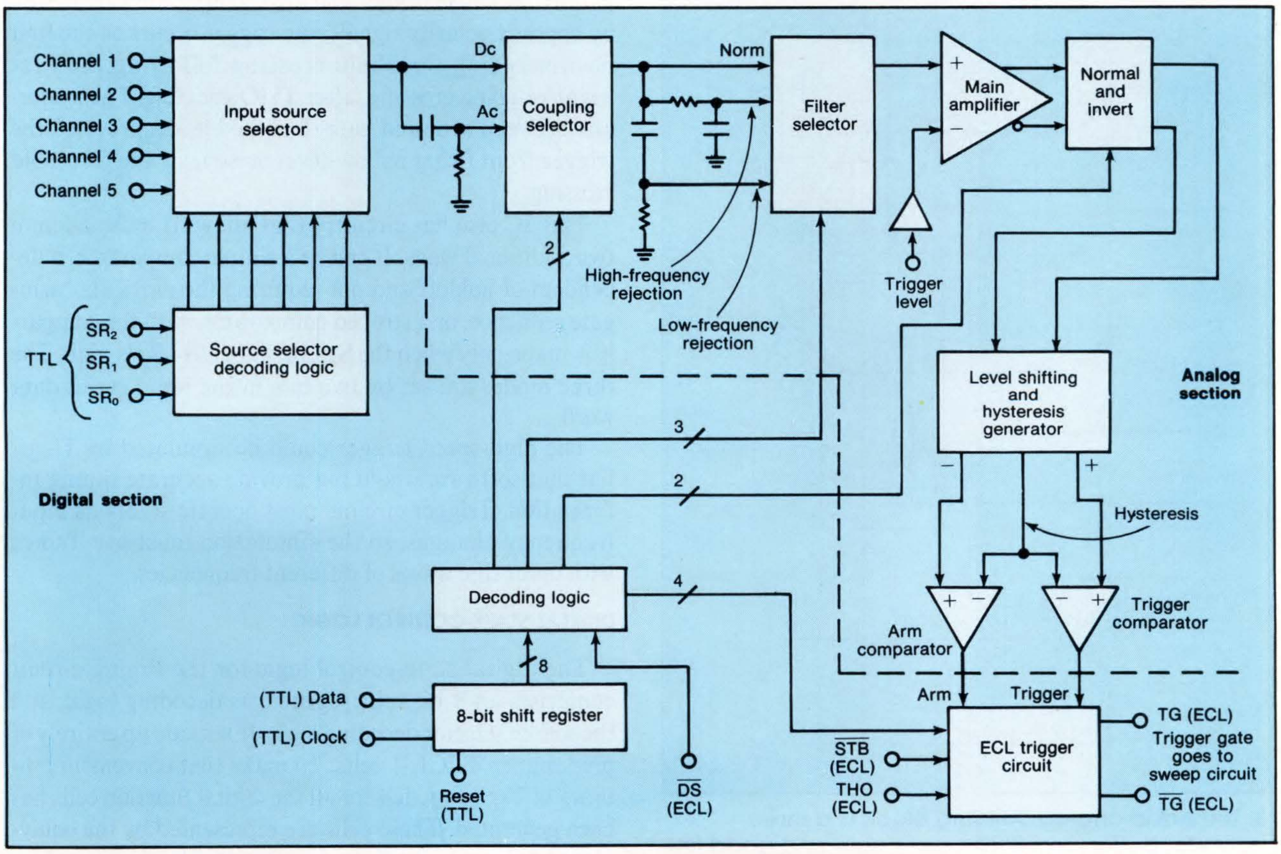
THREE MAIN AREAS

The trigger IC design has three main areas: the analog signal-conditioning circuitry, the digital state-control logic, and the high-speed ECL trigger circuitry. The signal-conditioning circuitry is designed with the array's analog tiles, using Tspice for simulation and drawing on the analog device library for its models.

The state-control logic, designed for the most part from low-speed ECL, uses the TECL-1 gate-array cell library and is simulated on Tlogs. The simulation draws on the logic models in the QuickChip 4 library of standard digital functions. The high-speed ECL trigger is designed from the TECL-1 functional cells but is simulated on Tspice to determine actual performance. That final simulation depends on Tspice models for the TECL-1 cells.

Several variations of a three-transistor buffer serve as building blocks in designing the trigger circuit's analog portion. The buffer's properties include unity gain, good linearity, and parameters constant with temperature and processing. It has high input impedance and low output impedance. Moreover, it exhibits no change in dc level from input to output—an important characteristic, since the design is implemented with an IC process that yields relatively poor pnp transistors. Its bandwidth is about 1 GHz.

A five-channel multiplexer provides the IC's input (Fig. 3). By steering the current to the separate differential pairs, the inputs can be selected in turn, a configuration that offers excellent signal rejection of deselected inputs and that interfaces well with ECL. In the Tspice simulation for this stage, transistor and resistor models are drawn from the analog device library, while the NOR gates that drive the current-steering transistors are mod-

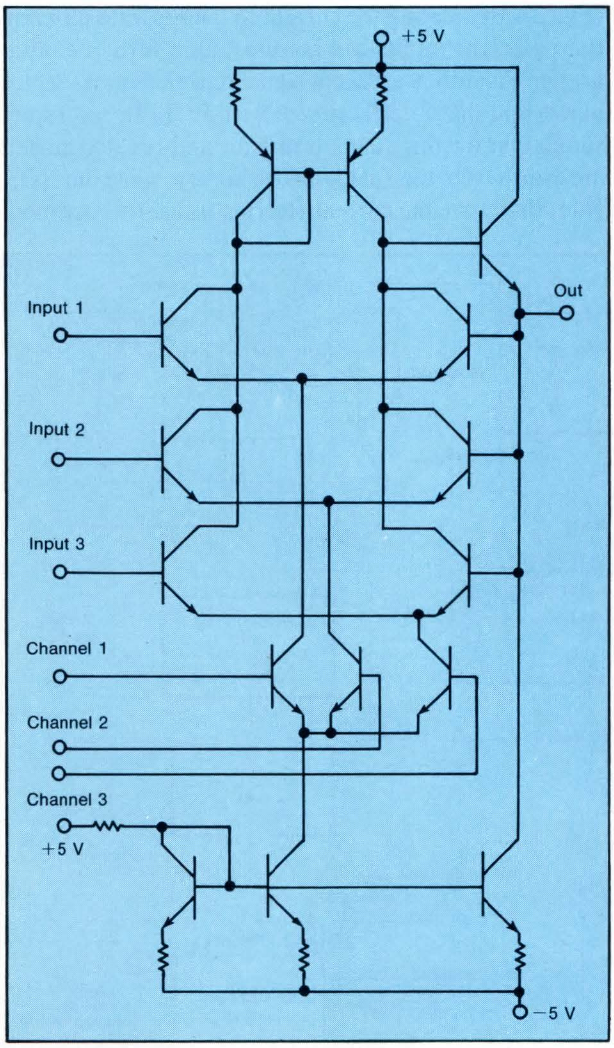


2. When used in a high-speed trigger circuit for an oscilloscope, the mixed analog-digital chip chooses five input signals under digital control. An 8-bit shift register stores the digital word that controls the circuit's operation. The trigger is a high-speed ECL signal.

eled through the digital cell library. These models accurately simulate digital cell behavior, such as settling time between source selections.

The input source selector is followed by two cascaded multi-input selectors (Fig. 2 again). The ac-dc coupling selector is followed by a three-input filter selector buffer. The signal comes either directly, or through a high-pass or low-pass filter. (Because the filters require large capacitors and accurate time constants, they are not themselves on the IC.)

Gain, threshold injection, and signal inversion circuitry follow (Fig. 4). The threshold level, set by the user with the trigger-level control, feeds one side of the cascode differential amplifier through another three-transistor buffer. The signal is applied to the other side of the amplifier, which has a gain of about 25. The high f_T and low C_{CB} (capacitance from collector to base) of the IC process that is used permit a bandwidth wider than 600 MHz.



3. The basic analog building block is a three-transistor buffer circuit with unity gain and good linearity. Exhibiting a high input and a low output impedance, it provides a bandwidth of 1 GHz. More transistors increases the number of inputs.

An alternate common-base path (Q_1 and Q_2) inverts the signal. Zener diodes shift the output level to drive the ECL comparators operating between −5 V and ground.

The differential outputs of the emitter-followers (Q_3 and Q_4) drive a pair of comparators, whose reference voltage is about 50 mV less than the common-mode level of the emitter-follower outputs. That 50-mV shift provides trigger hysteresis and prevents input signal noise from creating trigger jitter. The comparators are simple differential pairs with emitter-follower outputs and with their output levels interfacing with the devices in the ECL cell library.

HIGH-SPEED TRIGGER SECTION

The actual trigger circuit, constructed from predesigned high-speed ECL cells that come with the array, has a pair of latches, arm and trigger, to realize the trigger operation. A signal from the decoding logic (Fig. 2 again) activates the normal-sweep trigger mode, and the Holdoff signal (THO) enables an arm latch, which resets on the first negative transition of the arm comparator after THO goes low.

With a low from the arm latch, the trigger gate latch sets on the next negative transition from the trigger comparator. Because trigger and arm comparators are driven by opposite polarity signals, the trigger occurs on the first positive-going threshold crossing following the first negative-going crossing, after THO goes low. The hysteresis between arm and gate threshold levels prevents the trigger from firing on low-level noise near the threshold crossing.

This IC also has circuitry that allows it to function in two additional ways. It can be a simple comparator, independent of holdoff and not requiring the particular arm-gate sequence, or a strobed comparator, with the comparison made only when the Strobe signal (STB) is high. The three modes are set by two bits in the input serial data word.

The high-speed trigger could be simulated by Tlogs, but that software would not provide accurate timing information. Trigger circuits must operate stably as input frequency changes, so the simulation must use Tspice with input sine waves of different frequencies.

DIGITAL STATE-CONTROL LOGIC

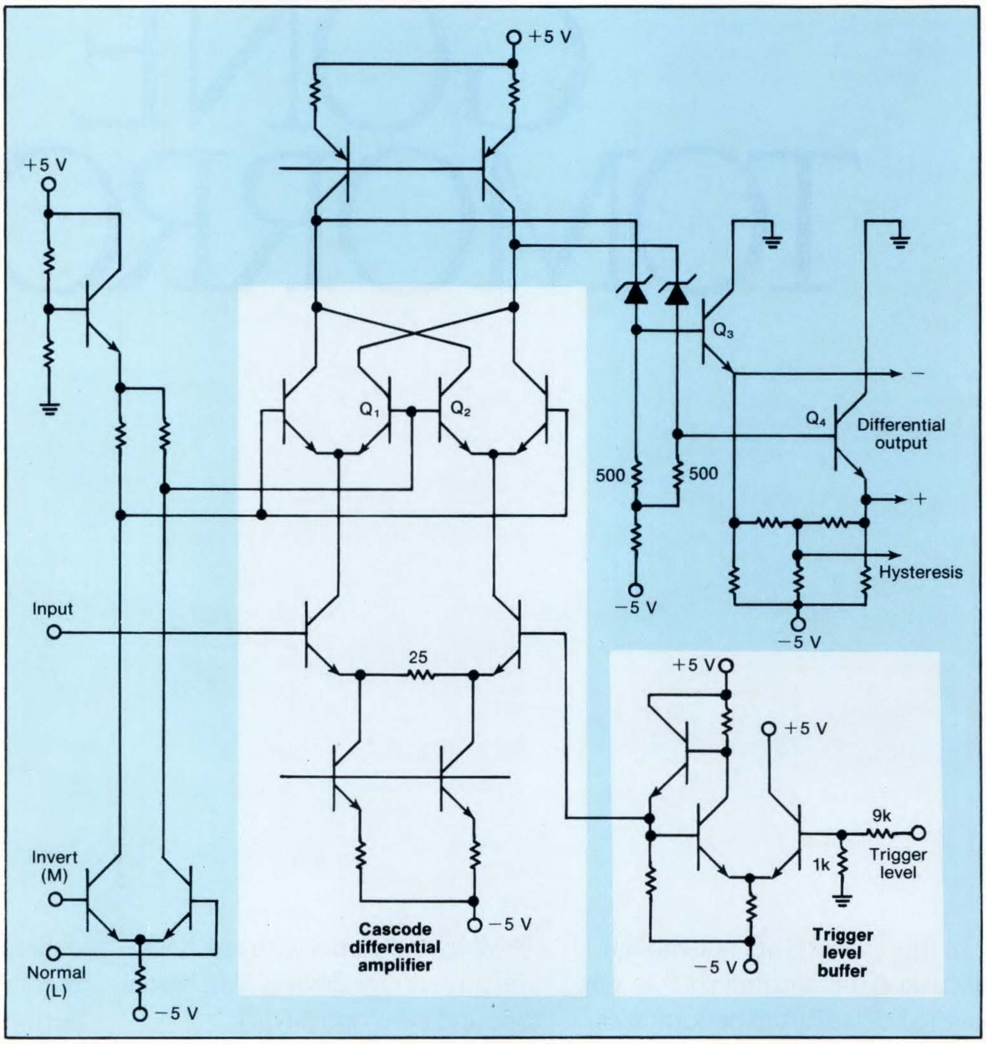
The digital state-control logic for the timing circuit comprises an 8-bit shift register, its decoding logic, and the source selector decoding logic. It is made up entirely of predesigned TECL-1 cells. To make that convenient a library of Tspice models for all the digital function cells has been generated. Those cells are represented by the equivalent of Spice cells. The circuitry can be simulated on Tlogs using cells from the standard library. Since Tspice and Tlogs have a common input language, a single net-list

description of the source selector logic, for example, can be simulated either at the logic level with Tlogs or at the circuit level with Tspice by attaching the appropriate library file. By using a single input language for the net list, the entire circuit layout is verified at once.□

Robert Sparkes, a senior design engineer in Tektronix's Integrated Circuit Operation, has worked for the company for six years. He is program manager for the QuickChip bipolar arrays and has designed many digital and analog circuits. Born in Canada, Sparkes received his BA, master's, and doctoral degrees in electrical engineering from the University of Toronto.

Winthrop (Wink) Gross is IC design manager for the IC operation. With Tektronix since 1969, he was responsible for developing the vertical-output amplifiers for the Model 7104 oscilloscope and the 2465 portable oscilloscope. Gross earned a BA at Harvard University and an Electrical Engineer degree at Massachusetts Institute of Technology. He holds two patents in high-speed analog IC design.

How valuable?	Circle
Highly	544
Moderately	545
Slightly	546



4. The threshold level of the trigger circuit is set by adjusting a trigger-level control on the front panel. That level is fed through a three-transistor buffer to a cascode differential amplifier, with the differential output and hysteresis signal applied to the arm and trigger comparators (see Fig. 1).

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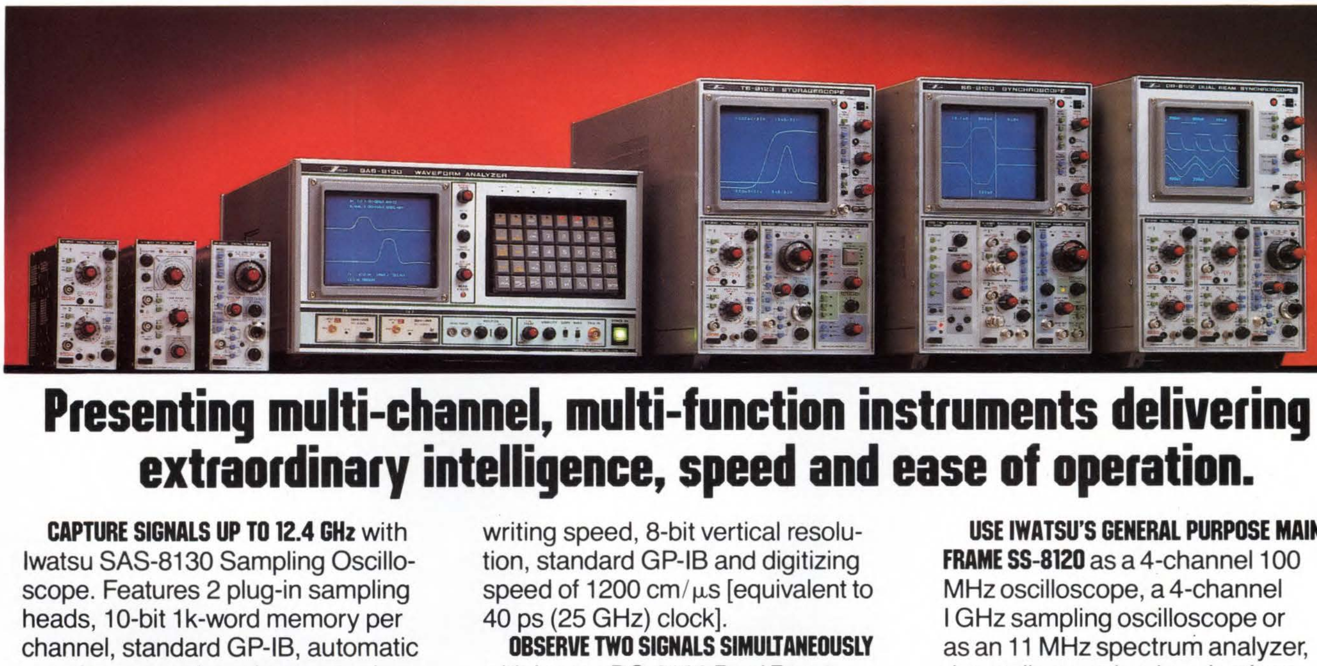

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CIRCLE 57

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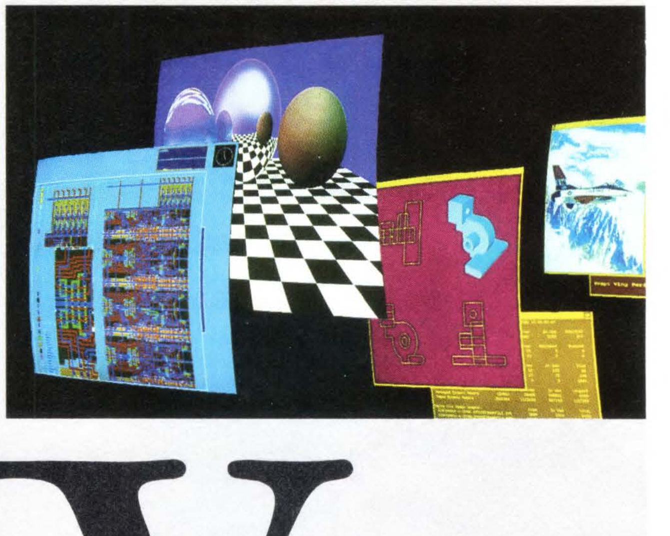

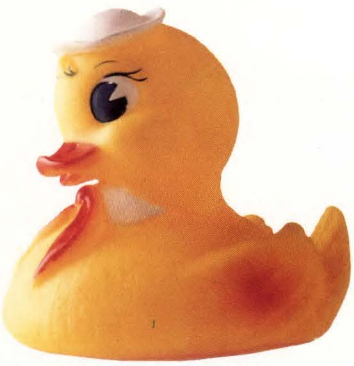

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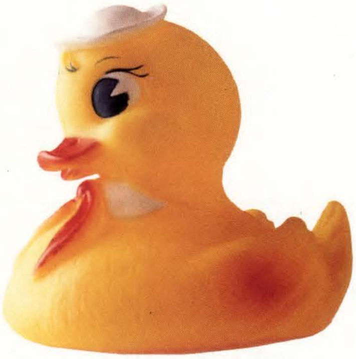

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CIRCLE 59

ELECTRONIC DESIGN EXCLUSIVE

Large-scale ASIC library merges microprocessor peripherals

Andrew Haines
VLSI Technology Inc., 1101 McKay Dr., San Jose, CA 95131; (408) 434-3000.

One-chip microprocessors that include on-board peripheral circuits offer many advantages over those that do not. Such devices typically combine 8-bit microprocessors, serial I/O ports, direct-memory-access controllers, and timer/counters. As a result, they cut chip count and printed circuit board space, shrink design time, and simplify interface problems. Perhaps most important, these parts improve reliability. For these reasons, they are increasingly important to system designers.

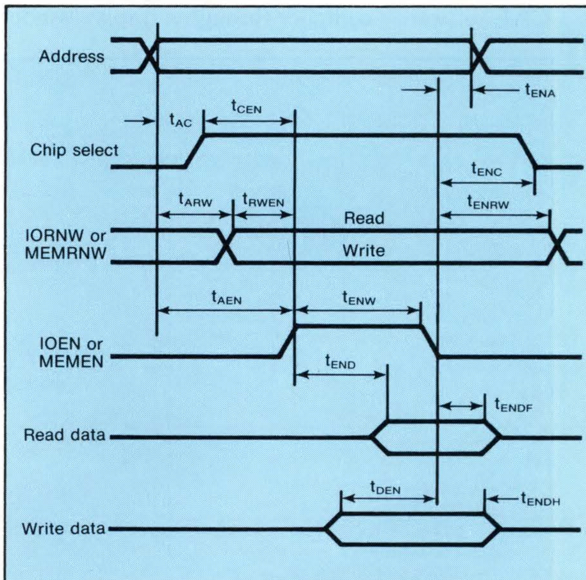
Fitting peripheral ICs together can be a stumbling block. To the designer's rescue come an ASIC device technology that weds glue and peripherals.

However, as standard products addressing a multitude of needs, they risk meeting none of them best. For example, a device may have too few timers or serial lines, or its DMA controller may be the wrong type, forcing a designer to compensate by adding other chips.

For the first time, the technology for building application-specific ICs (ASICs) can help solve the problem by giving designers the raw material and tools to tailor a chip that includes only the parts they need. A library of popular 8086 and 8088 microprocessor peripheral devices, called megacells, includes CRT, DMA, bus, and programmable interrupt controllers, as well as an asynchronous communications element. The library also contains such general-purpose circuits as a timer/counter, clock generator and programmable peripheral interface and four byte-wide CMOS memories. The memories consist of two RAMs, 1k-by-8 and 256-by-8 bits, and two ROMs, 1k-by-8 and 4k-by-8 bits.

But a megacell library alone is not enough to make a complete peripheral circuit. The system is one of the first to include a microprocessor bus structure, as well as a standard-cell library, with which users can create their own functions. In addition, the development system's CAE software tools enable engineers to analyze a design quickly and accurately. Furthermore, packaged versions of each megacell are available for checking out a system before designing the ASIC. Engineers can plug these versions directly into an existing system to ensure that they will perform correctly in the surrounding software and hardware.

The combination of peripheral and standard cell



Key to abbreviations			
Symbol	Parameters	Minimum (ns)	Maximum (ns)
t_{AC}	Address to chip-select delay	0	
t_{AEN}	Address to enable delay	40	
t_{ARW}	Address to read-write delay	0	
t_{CEN}	Chip select to enable setup time	10	
t_{DEN}	Write data to enable setup time	50	
t_{ENA}	Enable to address hold time	10	
t_{ENC}	Enable to chip-select hold time	10	
t_{END}	Enable to read-data delay		50
t_{ENDF}	Enable to data-bus float	5	30
t_{ENDH}	Enable to write-data hold time	10	
t_{ENRW}	Enable to read-write hold time	10	
t_{ENW}	Enable pulse width	50	
t_{RWEN}	Read-write to enable setup time	10	

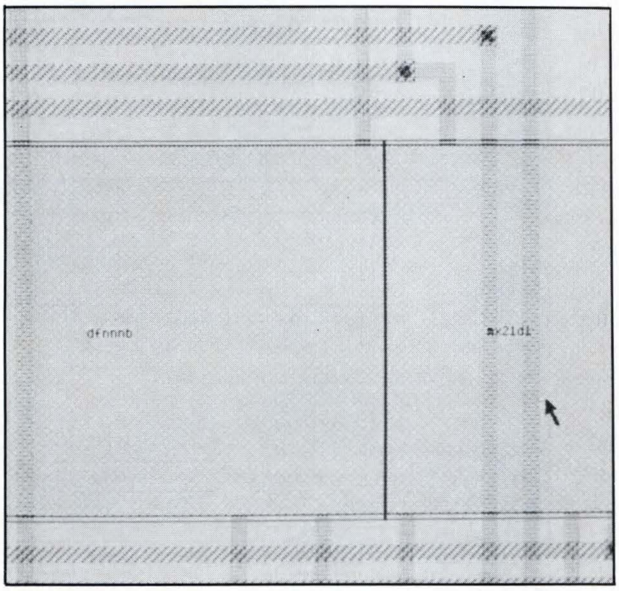
1. In the megacell ASIC architecture, the microprocessor bus acts like a standard system bus, making simple work of connecting large-scale cells and other logic throughout the chip. Reading and writing starts when the system processor addresses and selects a megacell and then chooses an operation.

libraries goes beyond the core microprocessor concept. Each megacell meshes optimally with the other library elements; all cells are a standard height. In addition, because the locations of buses, control signals, and power lines are standardized, all library elements connect in the same way and in a straight line. As a result, layouts make the most efficient use of silicon. Such efficiency is especially important in bus-oriented microprocessor designs, where meandering buses can consume valuable chip area.

SUPERIOR IMITATIONS

The microprocessor peripherals, built with 2-μm, double-metal CMOS, duplicate the functions of standard products. But they use less power and perform about 75% faster than their NMOS counterparts. Equally important to a one-chip system are the SSI and MSI functions. The standard-cell components, dense and compact, fit an average of two transistors into 1 mil^2, and the cell height is only 72 μm.

Designers can incorporate memory elements into the integrated system in three ways. They can access the CAE software's compiler through a display window and specify the memory's length, word width, and performance. Then the compiler automatically generates a physical layout, simulation model, and schematic symbol. Another approach is simply to have the megacell vendor compile the memory and supply the simulation model and schematic. The third choice is one of the bytewide memories in the megacell library.



2. Unlike most other software that places functional blocks and routes their connections, the megacell system can automatically route the second metal layer over a cell (arrow). The metal requires no feedthroughs or paths between cells. That ability is critical because it caps the die size for single-chip systems that might otherwise grow too large.

The VTIbus, the megacell system's standard bus, makes a simple link between the various integrated components. The bus architecture and operation mimic a standard microprocessor bus (Fig. 1). Reading and writing operations begin when a system processor addresses and selects a particular megacell and chooses the operation.

For I/O operations, the processor controls line IORNW; for memory operations, it switches MEMRNW. Data transfers when the processor holds the corresponding enable line, either IOEN or MEMEN, high for at least 50 ns. When data is being read, it appears on the megacell output within 50 ns of the enable line going into its high state. For writing, the processor must put data on the bus at least 50 ns before the enable line returns to a low.

The simple interface is similarly defined for all megacells, regardless of their bus requirements. Moreover, standard microprocessor interfaces can be created for off-chip connections.

TOOLS OF THE TRADE

No library would be adequate without suitable software to place and route cells. For this, the megacell software takes full advantage of CMOS' two metal layers. Unlike commercial systems, which require a feedthrough or routing path between cells, the megacell approach automatically routes second-layer wires over cells wherever possible (Fig. 2). As a result, die size decreases.

Though microprocessor peripherals make particularly heavy demands on automatic design tools, the megacell system solves the difficult problem of placing blocks of arbitrary height among blocks of standard height. In addition, a proprietary editor takes a hierarchical approach to placing symbolic elements. Final placement occurs after routing, during a "compaction" phase, which closes the space between cells.

In addition to placing, routing, and schematic entry software, the CAE package includes such verification tools as a functional simulator and test description language. The functional simulator is dramatically faster than the gate-level ones that most device manufacturers require. What's more, it suits microprocessor systems, which can have up to 15,000 gates, and, consequently, are slow to simulate at the gate level. Thus, it avoids the delays that invite designers to take shortcuts and therefore compromise a design's integrity.

The simulator's display window accepts a large number of commands and provides both waveform and text outputs. Using a hierarchical approach, designers first work on subblocks and then individual blocks of a design. The final task is on the interaction between the blocks.

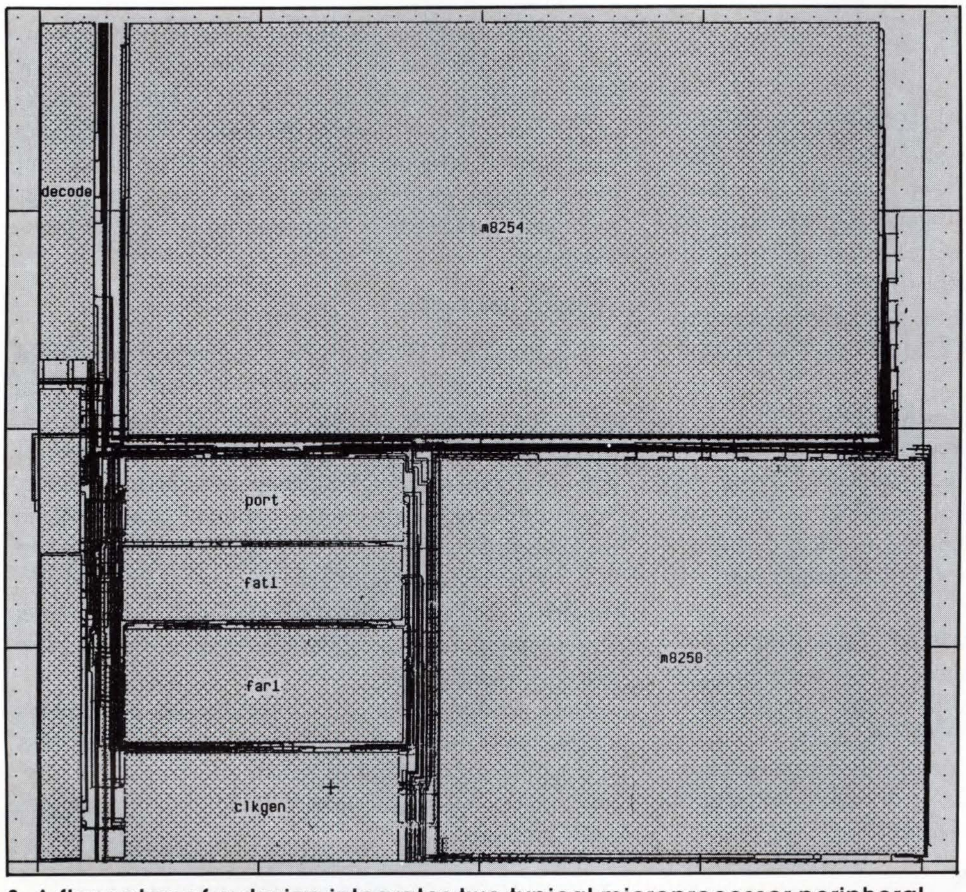
A TASTE FOR TESTING

Because the functional model written for each megacell comes thoroughly tested, no effort goes into simulating their complex functions; only the interaction between megacells must be checked.

Each megacell has its own test program, which is identical to that of the part's standard product. Therefore, the two versions respond in the same way to the same test. In addition, test modes are built into chips that contain multiple megacells. The modes access the internal bus and allow off-the-shelf tests to exercise individual megacells. As a result, the devices are easier to test thoroughly and the megacell operates just as its standard product version does.

Designers apply VTItest, the test (and simulation) description language, in a hierarchical manner from the bottom up. First, they define a sequence of vectors (1s and 0s) that perform a particular operation. Once described, the vectors can be shared by as many operations that need them, thus simplifying the job of specifying those operations. For example, read and write cycles would naturally share a vector pattern.

Moreover, once it is described and named, an operation can be combined with others to form higher-level functions that can be called by a single command. The com-



3. A floor plan of a design integrates two typical microprocessor peripheral circuits, an 8254 timer-counter and an 8250 serial I/O port. Also on board are small functional elements, namely a clock generator, address decoder, and keyboard interface, as well as glue logic. The ASIC compresses 30 in.^{2} of circuit consuming 6.5 W into a 1-in.^{2} device using only 0.5 W.

mand, in effect, invokes hundreds of test vectors. The functions can also take parameters. For example, writing a sequence of bytes is performed with repeated references to the same operation, changing only one parameter, which is passed to the write function each time it is called. Working at the functional level, it also easier to predict a circuit's output and verify that the prediction matches the output of the simulated circuit.

The floor plan (Fig. 3) of a chip shows how peripherals are integrated to solve a problem faced by many microprocessor system designers. Taken individually, the chip's functions correspond to those of an 8254 timer/counter, 8250 serial I/O port, clock generator, address decoder, glue logic, and keyboard interface. The combination of those functions applies to a wide range of electronic systems, including personal computers, telecommunication systems, and industrial controls.

TIMING AND I/O

The timer/counter and serial I/O port are popular LSI peripherals common in 8086 and 8088 microprocessor systems. In this case, the processor is an 8088. The timer/counter supplies the system's general-purpose timing pulses; the I/O line carries serial communications. In addition, the clock generator divides the incoming 4.77-MHz reference signal into appropriate timing pulses for the timer/counter, UART, and keyboard interface circuits.

The address-decoding logic selects system devices. It turns A_0 through A_9 of the processor's address lines into enabling signals that travel on chip and off. The on-chip signals select the I/O ports, keyboard logic, and the LSI peripheral logic. Off-chip, the signals select peripheral devices, such as a floppy disk, DMA controller, and real time clock and calendar.

The keyboard logic converts serial data from a keyboard into bytes, and double buffers it to ensure integrity. On receiving data, the logic also interrupts the processor. The glue logic performs the remaining tasks—to control an external audio output port, generate a nonmaskable interrupt when a memory parity-error occurs, and control bidirectional three-state data buffers.

A CONVINCING COMPARISON

The ASIC circuit occupies a single 68-pin package and 1 in.^{2} of board space and dissipates less than 0.5 W. If built conventionally, the same design would require two 24-pin LSI circuits and 22 TTL devices of MSI scale. It would consume 30 in.^{2} of space and 6.5 W of power. In addition, the many solder joints throughout the board would make it less reliable.

What does it take to design the circuit as an ASIC? Since the megacell library includes the serial I/O port and the timer/counter, those are included as ready-made functional blocks. Moreover, because the megacells correspond exactly to their standard component counterparts, existing software can be used. Furthermore, connecting the megacells is no problem for designers familiar with popular 8-bit busing concepts, and the glue logic is readily available, as it comes straight from the standard-cell library.

All library components appear as standard logic symbols and are handled by the schematic editor. The editor offers simple pop-up menus and a mouse interface, making it especially easy to enter the design. The schematic, once entered, supplies the database for the simulation phase to follow. In addition, it also documents the project and creates a net list to be compared with that of the physical layout.

SIMULATE FOR SUCCESS

The simulation phase invokes the functional models of the standard cells and megacells. The full simulation takes about 65% less time than a gate-level model would. Then, using the test description language, the resultant circuit outputs can be checked against those predicted. For example, obviously a serial stream of 1s and 0s from the keyboard should produce bytes of alternating 1s and 0s from the keyboard interface every eighth bit time. It is simpler to predict the output working with the high-level representation of the keyboard function, rather than its gate-level descriptions.

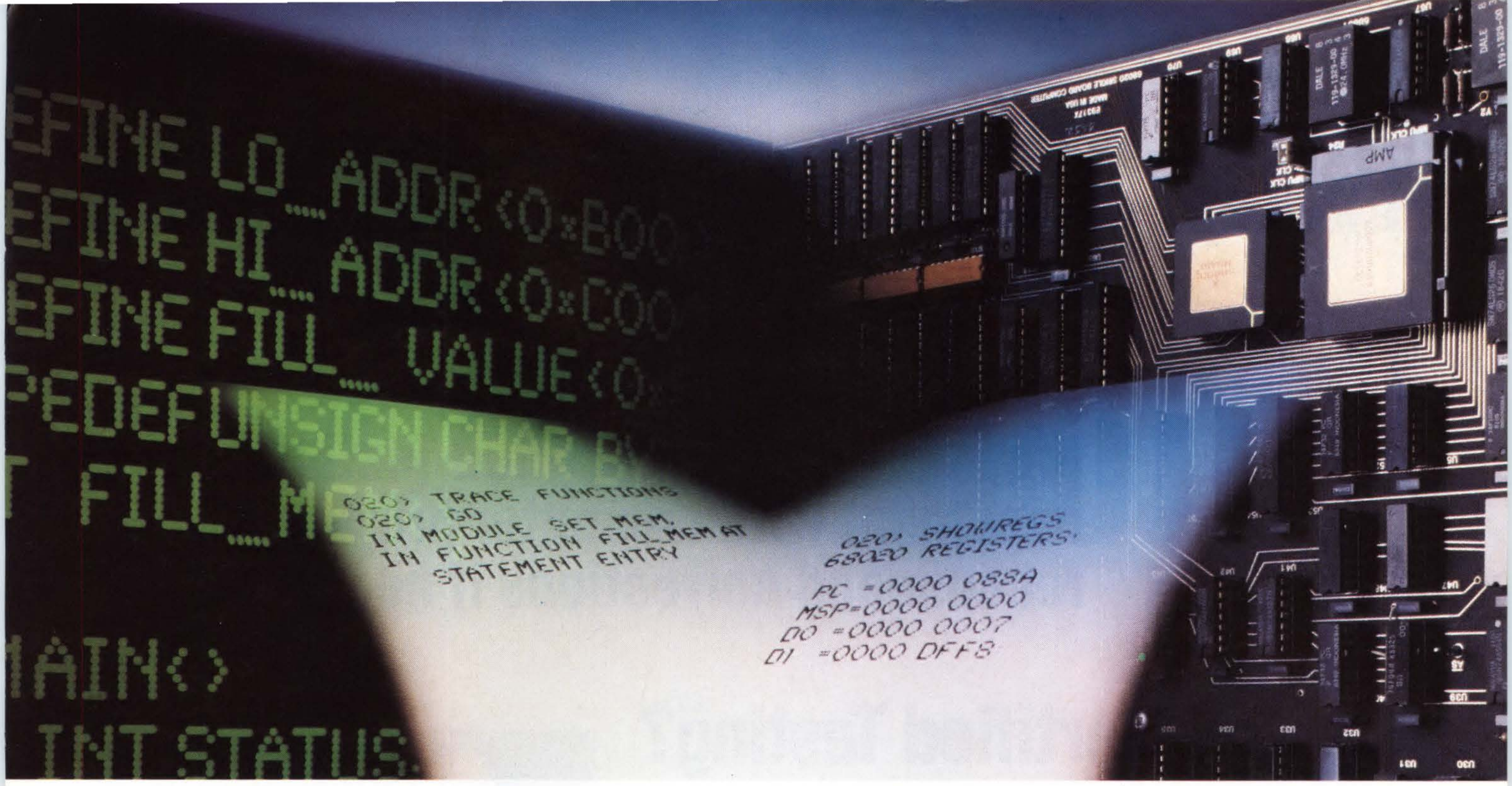
Once verified, the design database enters the vendor's prototype and manufacturing process through a network of design centers linked to the manufacturing facility. From that point, typical turnaround for prototype chips is 8 to 12 weeks.□

Andrew Haines is a manager for strategic marketing for VLSI Technology's ASIC division. During his five years with the company, he has also served as a marketing manager for ASIC design tools and gate-array products. He has a BS in physics from the University of Wisconsin.

Price and availability

Individual megacells cost from $3000 to $6000, depending on their complexity. The price includes a packaged version of the cell, simulation model, test program, and icons for the physical and logical design schematic. Megacells are available as software for customers' engineering workstations or through facilities at design centers. CIRCLE 502

How valuable?	Circle
Highly	547
Moderately	548
Slightly	549



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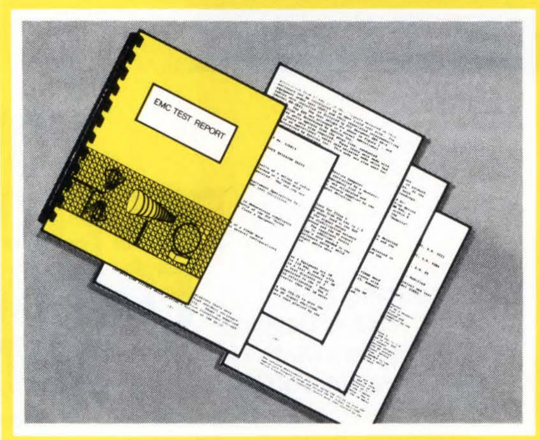

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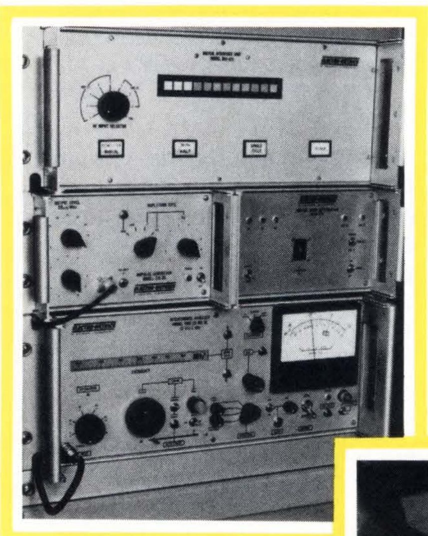

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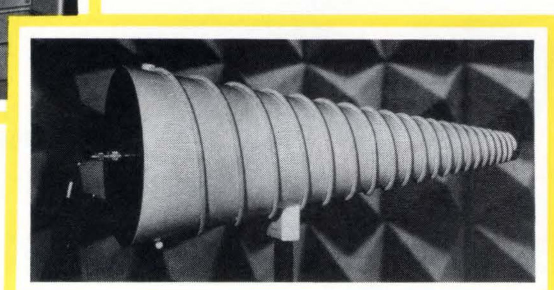

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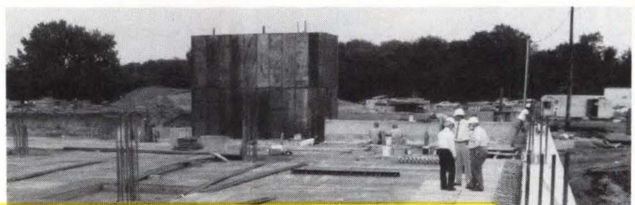
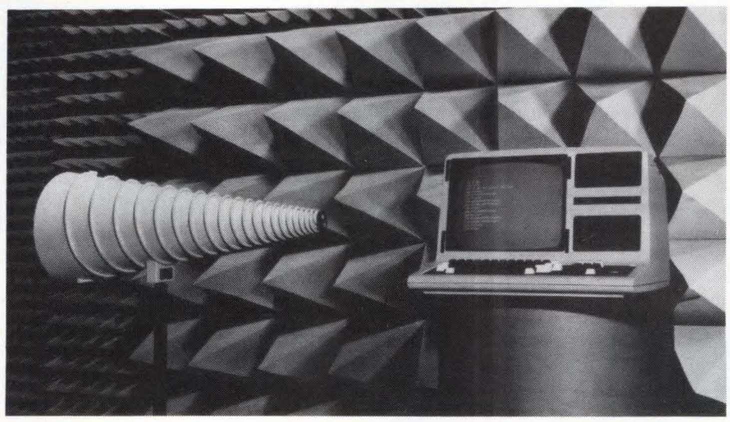
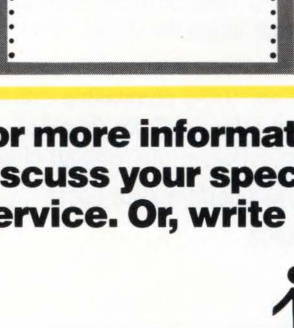




What do you get?



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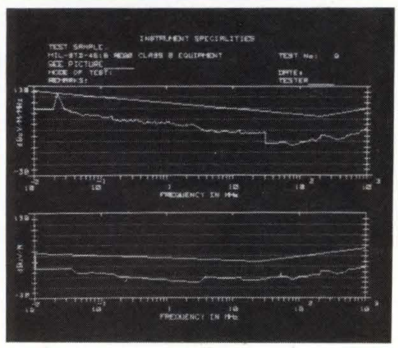

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ELECTRONIC DESIGN EXCLUSIVE

Fast modem designs benefit from DSP chip's versatility

John Roesgen
Analog Devices Inc., Two Technology Way, Norwood, MA 02062-0280; (617) 329-4700.

This is the last in a series of four articles detailing a new digital signal processor with many applications. Previous articles introduced the ADSP-2100 (Feb. 20, p. 131), covered its versatility in imaging and machine vision systems (March 20, p. 135), and showed how it succeeds in linear predictive coding analysis for speech (April 17, p. 153).

To send data at more than 4800 bits/s over the limited bandwidth of telephone lines, modems use quadrature amplitude modulation and thus mandate digital signal processing. As the data rate climbs above 9600 bits/s (as high as 19,200 bits/s in some recent modems), the computational demands become particularly severe. For instance, error-correcting codes must be applied to the data stream to maintain acceptable performance. Furthermore, bidirectional fast transmission over a single phone line requires either echo cancellation or rapid signal reversal to quickly change direction.

Quadrature amplitude modulation is one modem task this DSP chip handles. Its high density simplifies design; a dual bus speeds operation.

Because that level of complexity cannot be met by current single-chip signal processors, designers have turned to multiple processor configurations, bit-slice architecture, and custom VLSI. Those avenues, however, not only require longer and more difficult design cycles than a single-chip processor but also extort a higher cost.

Now, the ADSP-2100 DSP microprocessor packs enough horsepower to single-handedly tackle high-speed modem tasks. Its dual-bus architecture, on-chip cache memory, parallel arithmetic units, and powerful program sequencer combine to accommodate the many required algorithms. In addition, extensive development tools reduce both hardware and software design time.

In operation, external program memory supplies instructions to the processor and stores coefficients for the various filters, while the external data memory holds internal processing variables, sample buffers, and filter delay lines (Fig. 1). The large address range of the chip gives plenty of storage space in both memories.

The digital interface section ties the modem to the terminal or computer equipment. A serial transmitter/receiver maps into the processor's data-memory address space as a peripheral device, as does a receiver tracker, which keeps the receiver bit clock synchronized to the transmitter at the far-end modem. The transmitter tracker establishes timing for the local transmitter, and both tracker circuits generate processor interrupts to synchronize the software. Those interrupts are serviced by the chip with almost no overhead.

The telephone line connects to the modem through an analog interface, with three devices in that section memory-mapped to the processor. A digitally programmed automatic gain control (agc) circuit normalizes the incoming signal to a predetermined level. After filtering, an analog-to-digital converter generates samples of the received signal and passes them to the processor. On the transmitting side, a d-a converter takes samples from the processor and generates an analog output signal, which is then filtered and coupled to the transmitting line.

Depending on the complexity of the nonDSP tasks (front panel displays and network-control features, for example), a host microprocessor may be desirable, connected most simply through the program memory interface. With the bus request and grant signals on the chip, the host gains direct access to the program memory. Consequently, it can download processor programs and control their execution. The interface can also accommodate data exchanges between the two processors.

While the heart of a modem lies in its signal-processing software, modem performance depends on the processor's ability to execute a variety of software tasks in real time. Generally, those tasks fall into two major groups: tasks that perform the transmitter function and tasks that perform the receiver function.

SCRAMBLED DATA

The transmitter section (Fig. 2) converts the incoming digital bit stream to an analog form compatible with the telephone channel. First it scrambles the data in a pseudorandom fashion, making the spectrum of the transmitter output resemble white noise to use the channel bandwidth more efficiently. The operation eases the recovery of the carrier and timing signal at the receiving end.

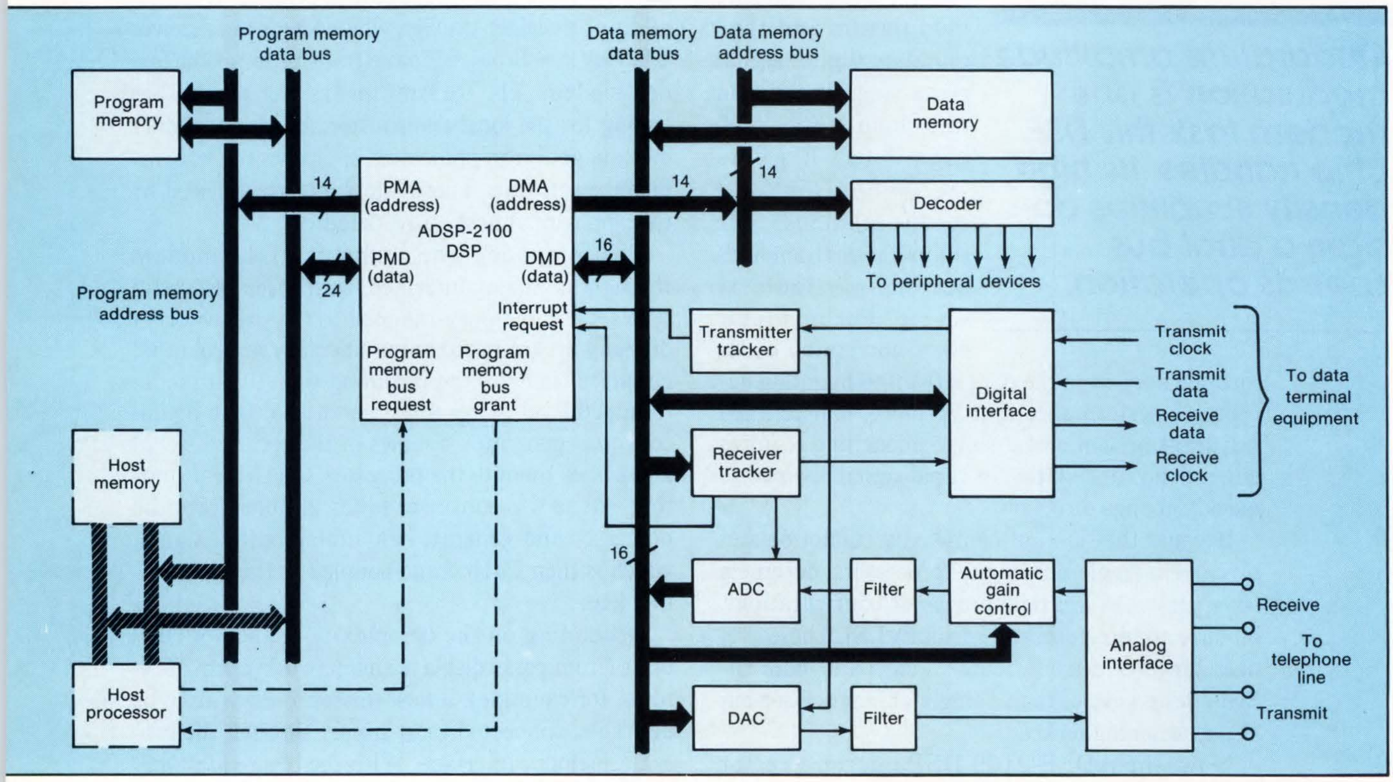
After "whitening" the output spectrum, the transmitter converts the scrambled serial bit stream into parallel multibit words called symbols. The number of symbols depends on the modulation structure. At 9600 bits/s, four bits define a symbol, and 16 symbols are used. The symbol rate is therefore one-fourth of the data rate, or 2400 symbols/s. Higher data rates require more symbols to keep the symbol rate lower than the channel bandwidth.

The encoder maps each symbol into a particular combination of carrier amplitude and phase. If an error-correcting code is used, the redundant bits are computed and added to the output at this point. Since the phase information is usually encoded differentially, each symbol generates a change from the previous phase rather than generating an absolute phase. The result is a complex number representing the desired amplitude and phase of the carrier for each symbol interval.

The multiplier unit modulates the encoder output by a complex carrier to convert the frequency spectrum into the channel's pass band. An interpolating digital filter receives the modulated carrier, increases the sample rate, and removes some of the repetitions within the spectrum. A d-a converter changes the real output of that filter to analog form, which becomes the modem's audio output.

The receiver section (Fig. 3), which recovers the transmitted data, is not as straightforward as the transmitter. Since the channel loss is unpredictable, it first normalizes the incoming signal through an agc circuit. After converting the normalized signal to digital form, a phase-splitting filter recovers the imaginary part and reduces the sample frequency to the symbol rate.

If the channel were perfect, the output of the phase-splitting filter would be identical to the input of the trans-



1. The ASDP-2100's dual bus structure speeds operation by allowing the DSP microprocessor to fetch instructions and data simultaneously. The digital interface connects the modem with the data terminal equipment or to the computer. With d-a and a-d converters, the analog interface ties the modem to the phone line.

mitter's interpolating digital filter, and the receiver could simply demodulate the signal to recover the data. However, the channel amplitude and phase characteristics are not uniform. They vary widely from channel to channel and may also change over time on a single channel. Since the carrier amplitude and phase contain the information, equalization must compensate for any distortion. Furthermore, because the equalizer is adaptive, it can adjust to any channel and track any changes.

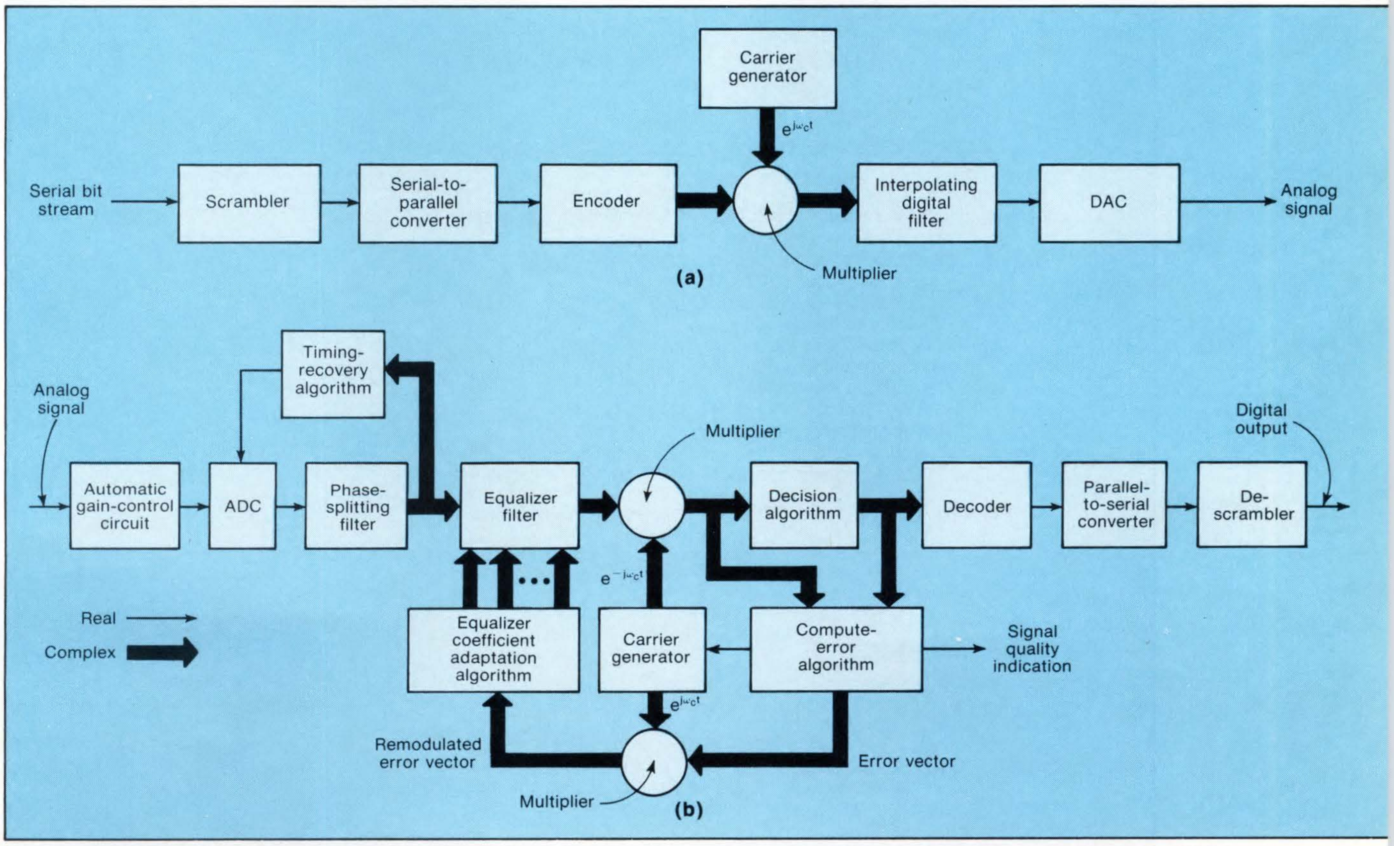
Multiplication by a local carrier demodulates the equalizer output. At this point, since the signal may still be corrupted by noise or short-term channel disturbances that the equalizer cannot track, its amplitude and phase may not exactly match that of the original transmitted signal. Fortunately, as the receiver has been programmed for the allowable amplitude and phase combinations, it decides which of these is closest to the received signal, usually by choosing the reference combination with the smallest Euclidean distance (in real-imaginary space) to the received signal. However, if convolutional error-correcting codes are used, a far more complex search algorithm must make the decision.

In either case, an error computation compares the decision output to the received signal and calculates an error vector. As long as the decision is correct, the error vector indicates how far the received signal deviates from its ideal amplitude and phase. A second multiplier remodulates the error vector into the pass band and drives the equalizer coefficient update algorithm. The error algorithm feeds back the phase component of the error to the local carrier generator, keeping the received carrier synchronized to the transmitted carrier.

DESCRAMBLED DATA

The receiver's last three blocks invert the operations performed by the first three blocks of the transmitter. The decoder maps the received amplitude and phase into a multibit symbol and converts it to a serial bit stream. Descrambling the stream recovers the original data.

Though all the functions generate a substantial quantity of software, a few critical tasks produce most of the processing burden and limit modem performance. The modem receiver's adaptive equalizer accounts for the largest part of the total processing demand. It consists of a



2. By converting the received digital signal into analog form, the transmitter section enables digital equipment to send its information over analog telephone lines. To do this, first it "whitens" the spectrum of the signal in the scrambler, thus easing recovery of the carrier and timing signal at the receiving end. To control precision and repeatability, the transmitter performs all its functions digitally (a). Because the receiver section (b) contains most of the processing functions, it accounts for most of the signal-processing demand. That results from signal degradation on a telephone line. Since the channel is imperfect, equalization compensates for distortion, and a decision algorithm corrects for added noise.

filter routine and a coefficient adaptation algorithm. The equalizer filter uses a finite-impulse-response structure, while the coefficient adaptation employs a least-mean-squared algorithm. They are coded into subroutines and called from an executive program.

A subroutine for the filtering portion of the equalizer demonstrates the microprocessor's efficiency in dealing with complex numbers (Fig. 4, left). Both the samples and the coefficients have real and imaginary parts, which are kept in separate buffers to simplify access. Coefficients are stored in the program memory and samples in data memory, enabling them to be fetched simultaneously.

Input and output variables pass through internal registers. Each time the subroutine is called, it processes an input sample and produces an output sample. Index registers are set up with pointers to the filter sample buffer (delay line) and coefficient storage area. Preloading the length registers with the filter order triggers the modulo-addressing capability, ensuring that the pointers will be confined to their respective buffers.

The filter code contains two Do . . . Until loops, both without overhead cycles. The first computes the real part of the output using only two instructions. One instruction accumulates the products of the real coefficients and the real samples; the other subtracts the products of the imaginary coefficients and the imaginary samples. The second Do . . . Until loop computes the imaginary output by accumulating the cross terms (real × imaginary and imaginary × real), again using two instructions.

The Do . . . Until structure imposes no penalty for loop sequencing. Fetching of samples and coefficients parallels the computation. Even though the coefficients are fetched from program memory, the program flows without interference because the internal cache memory supplies the loop instructions after the first pass.

The modem accomplishes other major filtering operations with similar routines. For instance, as in the equalizer the transmit filter also uses complex inputs and complex coefficients to compute the real output. Similarly, the phase-splitting filter produces a complex output from real

```
            Equalizer Filter Subroutine

                                 L - 1
            Algorithm:  Yr (N) = SUM [ Hr (K) • Xr (N-K) - Hi (K) • Xi (N - K) ]
                                 K = 0

                                 L - 1
                        Yi (N) = SUM [ Hr (K) • Xi (N-K) + Hi (K) • Xr (N - K) ]
                                 K = 0

            Input:  AX0 contains real input Xr, AX1 contains imaginary input Xi,
                    I0 points to starting place in real delay line
                    I1 points to starting place in imaginary delay line
                    I4 points to real coefficients
                    I5 points to imaginary coefficients
                    L0 contains filter order
                    L1 contains filter order
                    L4 contains filter order
                    L5 contains filter order
                    M0 contains 1
                    M4 contains 1

            Output:  SR1 contains real output Yr, MR1 contains imaginary output Yi

            Execution Cycles:  (4 • L) + 24        where L is the filter order

CMPXFIR:    DM (I0, M0) = AX0;                                          { Store Xr in delay line }
            DM (I1, M0) = AX1;                                          { Store Xi in delay line }
            AY0 = L0;                                                   { Subtract 1 from filter order }
            AR = AY0-1;
            CNTR = AR;                                                  { Load loop counter }
            MR = 0, MX0 = DM (I1, M0), MY0 = PM (I5, M4);               { Clear MR, Get Xi, Get Hi }
            DO REALLOOP UNTIL CE;
               MR = MR - MX0 • MY0, MX0 = DM (I0, M0), MY0 =PM (I4, M4);   { Xi • Hi, Get Xr, Get Hr }
REALLOOP:      MR = MR + MX0 • MY0, MX0 = DM (I1, M0), MY0 = PM (I5, M4);  { Xr • Hr, Get Xi, Get Hi }
            MR = MR - MX0 • MY0, MX0 = DM (I0, M0), MY0 = PM (I4, M4);  { Xi • Hi, Get Xr, Get Hr }
            MR = MR + MX0 • MY0 (RND);                                  { Xr • Hr }
            SR1 = MR1;                                                  { Save Yr }
            CNTR = AR;                                                  { Load loop counter }
            MR = 0, MX0 = DM (I0, M0), MY0 = PM (I5, M4);               { Clear MR, Get Xr, Get Hi }
            DO IMAGLOOP UNTIL CE;
               MR = MR + MX0 • MY0, MX0 = DM (I1, M0), MY0 = PM (I4, M4);  { Xr • Hi, Get Xi, Get Hr }
IMAGLOOP:      MR = MR + MX0 • MY0, MX0 = DM (I0, M0), MY0 = PM (I5, M4);  { Xi • Hr, Get Xr, Get Hi }
            MR = MR + MX0 • MY0, MX0 = DM (I1, M0), MY0 = PM (I4, M4);  { Xr • Hi, Get Xi, Get Hr }
            MR = MR + MX0 • MY0 (RND);                                  { Xi • Hr }
            RTS;
```

inputs and complex coefficients, requiring only minor alterations to the equalizer filter code.

Sample rate changes through filters are also easily done by adjusting the two M register values. Those values modify the coefficient and data pointers after each memory access. The ratio of the M register values determines the input-to-output sample ratio. To effect a sample rate increase of four, the data pointer would be moved by one, but the coefficient pointer would be moved by four. Or moving the data pointer by four and the coefficient pointer by one yields a sample rate decrease of four.

The program adapts the equalizer filter coefficients in small steps. Each time a new error vector becomes available, the coefficients get closer to their ideal values. A subroutine for the adaptation algorithm updates each complex coefficient in only six cycles (Fig. 4, right). Inputs to the routine include pointers to the sample and coefficient buffers, pointer modification values, and the error vector. The output is a set of updated coefficients. Combining arithmetic operations with a memory access, the six instructions in a single Do . . . Until loop perform all the work. That loop updates the real and imaginary parts of each coefficient, based on the corresponding sample in the filter delay line and the error vector. Sharing the computational load, the multiplier-accumulator computes the update terms and the ALU adds them to the coefficient. The processor then writes the new coefficient back into program memory and can proceed to the next filtering operation.

Another time-consuming task is the received signal decision. In the simplest method, the processor compares each received sample to all the possible transmitted values, and chooses the nearest one. One comparison measure is Euclidean distance in the real-imaginary plane, with the best choice being the point at the least distance from the received sample.

Assembly code for the received signal decision executes this task in just nine cycles per comparison. Inputs to the routine are the received sample, the total number of reference points, and a pointer to the memory buffer containing the reference coordinates. The reference points represent the allowable transmitted signal values, one of which

```
        Equalizer Filter Coefficient Adaptation Subroutine

        Algorithm:  Hr (K) = Hr (K) - Er • Xr (N-K) + Ei • Xi (N-K)
                    Hi (K) = Hi (K) - Er • Xi (N-K) - Ei • Xr (N-K)

        Input:  I0 points to Xr buffer, I1 points to Xi buffer
                I4 points to Hr buffer
                I5 points to Hi buffer
                L0 contains filter order
                L1 contains filter order
                M0 contains 1
                M4 contains 0
                M5 contains 1
                MX0 contains Er
                MX1 contains Ei
                CNTR contains number of complex coefficients

        Output:  Coefficients updated in coefficient buffers

        Execution Cycles:  (6 • N) + 8
                  where N is the number of complex coefficients

UPDATE:     MY0 = DM (I0, M0);                                  { Get Xr }
            MR = MX0 • MY0, MY1 = DM(I1, M0);                   { Er • Xr, Get Xi }
            DO COEFLOOP UNITL CE;
               MR = MR - MX1 • MY1 (RND), AY0 = PM (I4, M4);    { Ei • Xi, Get Hr }
               AR = AY0 - MR1, AY1 = PM (I5, M4);               { Hr - Er • Xr + Ei • Xi, Get Hi }
               PM (I4, M5) = AR, MR = MX0 • MY1;                { Store Hr, Er • Xi }
               MR = MR + MX1 • MY0 (RND), MY0 = DM (I0, M0);    { Ei • Xr, Get Xr }
               AR = AY1 - MR1, MY1 = DM (I1, M0);               { Hi - Er • Xi - Ei • Xr, Get Xi }
COEFLOOP:      PM (I5, M5) = AR, MR = MX0 • MY0;                { Store Hi, Er • Xr }
            RTS;
  ENDMOD;
```

4. In the equalizer filter subroutine (left), the microprocessor deals with complex numbers. Separate buffers contain the real and imaginary parts of both the samples and the coefficients. The equalizer filter coefficient adaptation subroutine (right) updates each complex coefficient in six cycles, producing a set of updated coefficients.

will be returned to the calling program as the receive decision.

The parallel arrangement of arithmetic units permits flexible operation sequencing in loop instructions, for example. Computation of Euclidean distance requires a sum of squares of differences; that is, two subtractions followed by two multiplications followed by an addition. This nonstandard succession generates much data-shuffling overhead in a serially organized machine.

The remainder of the loop compares each new distance with the previously found minimum distance. If the new one is smaller, it becomes the minimum, and the loop counter value is saved as an index. After all the distances are computed and compared, the subroutine returns the minimum distance and the corresponding reference index to the calling program. The program interprets the reference index as the received signal decision, and the minimum distance is the squared length of the error vector.

The software routines that have been described account for a large portion of the total processing load in a high-speed modem. The chip's performance for these tasks can be calculated using the execution cycle formulas given in the subroutine headers. A standard 9600 bit/s modem will be assumed. A 40-tap equalizer needs 184 cycles for the filtering operation and 248 cycles to update the coefficients. Because the transmit filter has no imaginary output, and the phase splitting has no imaginary input, they execute twice as fast as the equalizer. If both of these filters have 30 taps, they require 72 cycles each. A receive signal decision with 16 reference points uses 148 cycles, yielding a total of 724 cycles.

Since each routine runs 2400 times/s, 1,737,600 processor cycles are used every second. Since the chip executes 8 million cycles/s, the loading on the processor is 22%. This relatively small number for such a major portion of the modem indicates an ability to handle even more sophisticated algorithms and higher data rates than indicated here.□

John Roesgen, a staff engineer at Analog Devices and the principal architect of the 2100, joined the Digital Signal Processing Division in 1982. Roesgen has a BSEE from the University of Connecticut.

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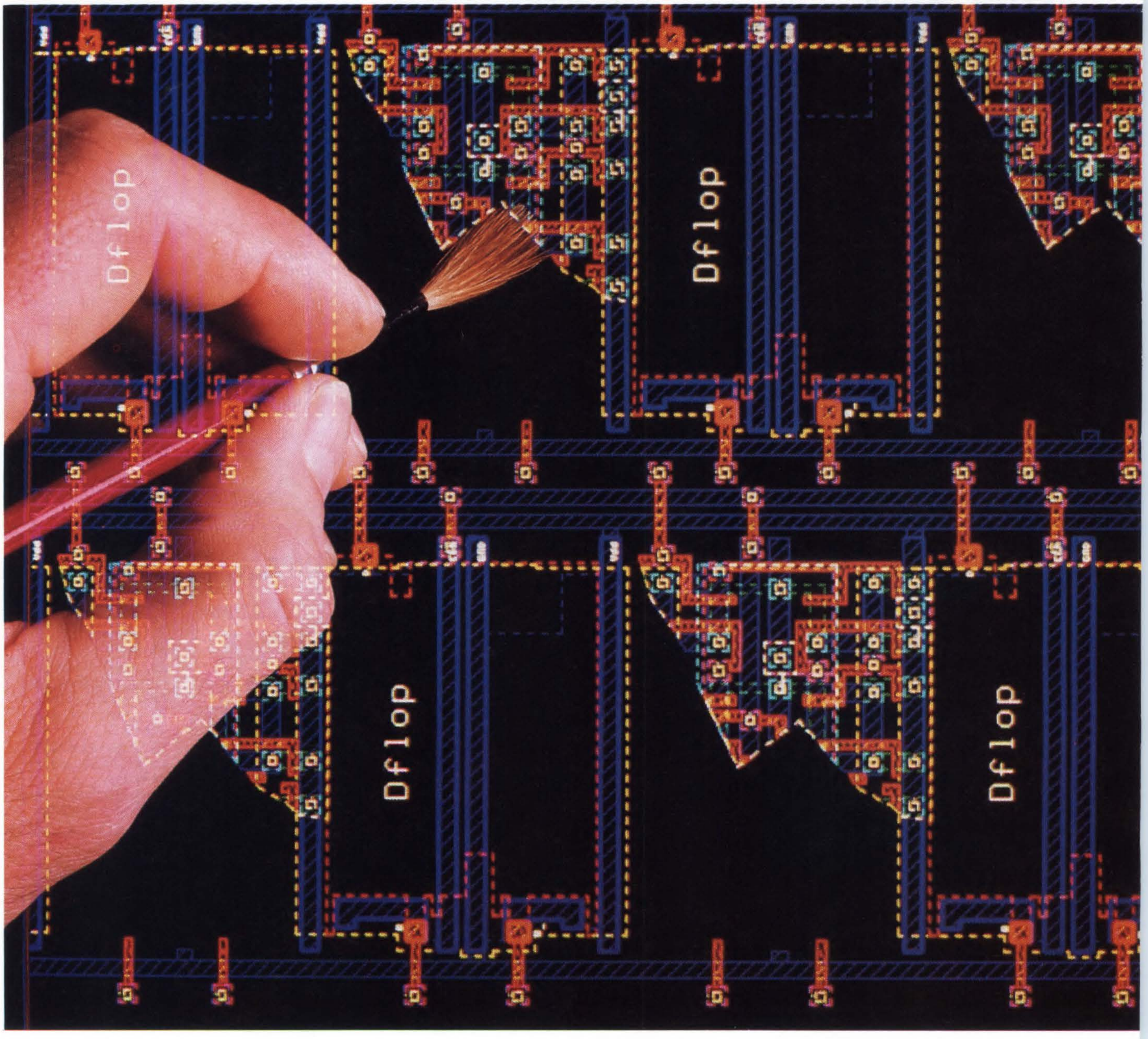

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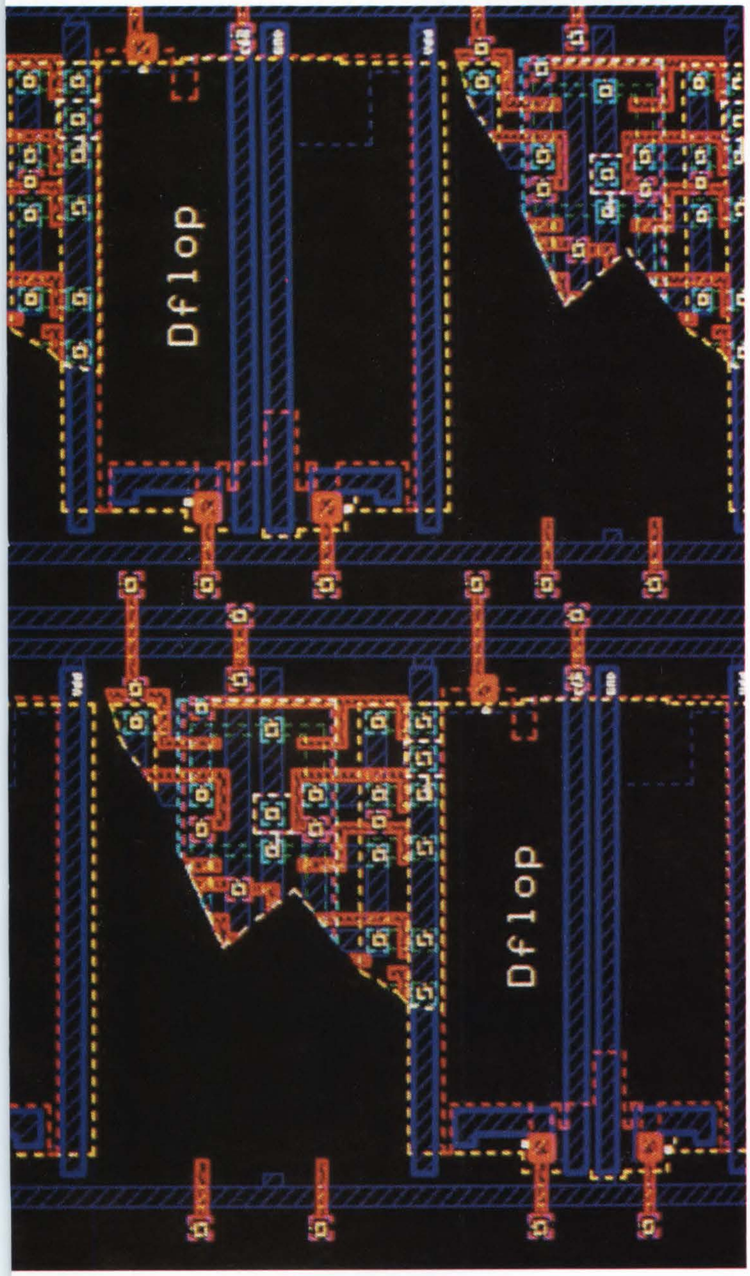

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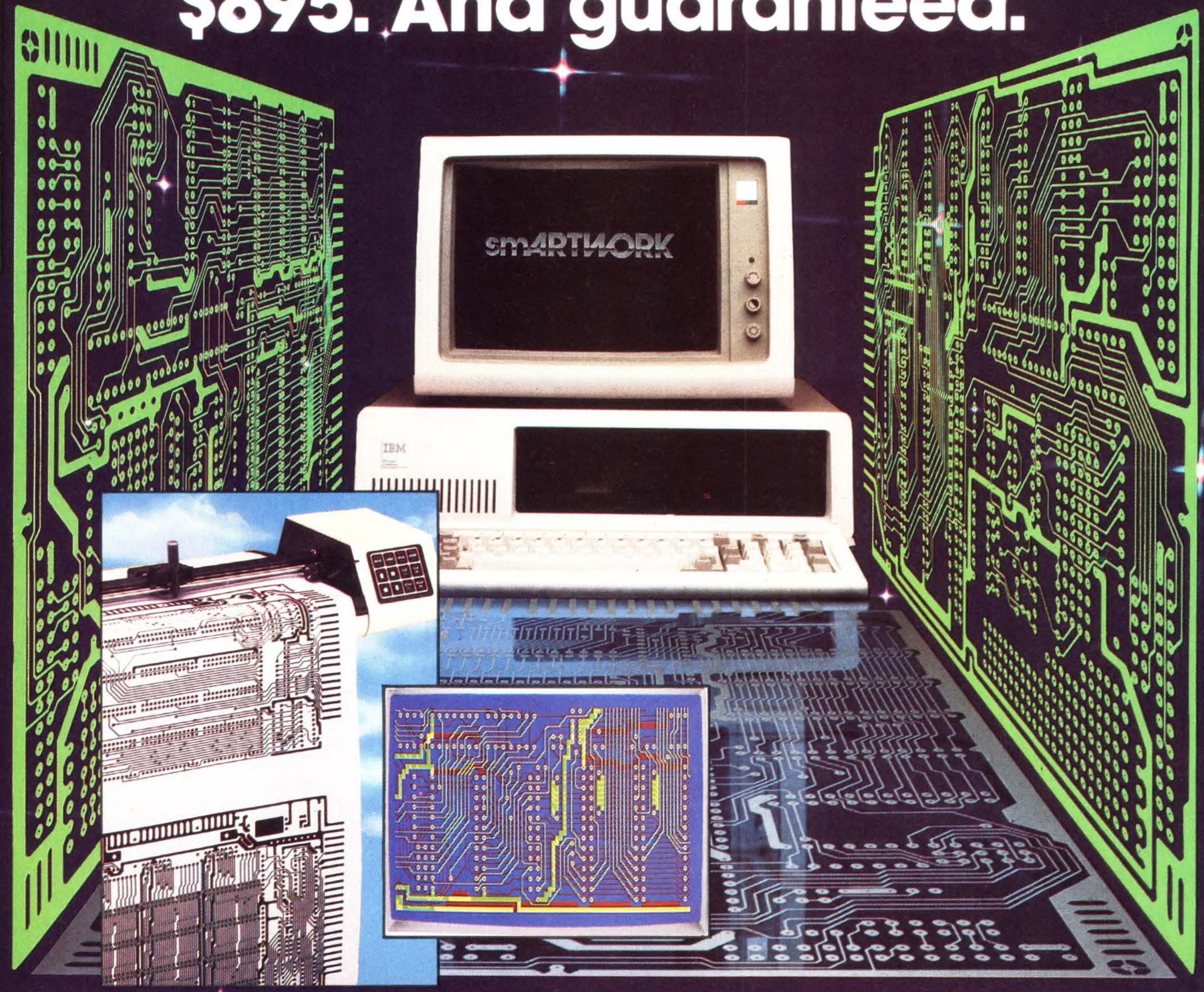

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CIRCLE 71

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In Europe contact: RIVA Terminals Limited, Woking, Surrey GU21 5JY ENGLAND, Telephone: 04862-71001, Telex: 859502

NEW PRODUCTS

ANALOG

ELECTRONIC DESIGN EXCLUSIVE

Single-chip op amp mixes top speed and power dissipation

Designers of wide bandwidth video systems can benefit from a monolithic op amp with a minimum unity-gain bandwidth of over 170 MHz—the widest of any such device. Moreover, that figure is reached by RCA's CA3450 while operating uncompensated at a noise gain of 10 or more and driving a 50-Ω load.

When the op amp operates with a closed-loop gain between 1 and 10, and a single 5-pF capacitor compensates it, the bandwidth narrows slightly to a few percent below 170 MHz. Hooked up to a ±6-V supply, and working at a gain of 5, the chip puts 5 V across its 50-Ω load, and that is while slewing at 160 V/μs, minimum. With essentially no load, except for the 20 pF and 1 mΩ found across an oscilloscope probe, the slew rate virtually doubles, and the output swing rises to 7 V. In either case, the slew rate at least reflects a 10-MHz full-power bandwidth.

Since the chip's maximum open-loop gain is only 60 dB, engineers may hold its accuracy in doubt. However, look again: It settles to 0.1%, in a mere 35 ns—at a gain of 10, again with 50 Ω at the output terminals. Moreover, it can source and sink up to 75 mA and drive 220 pF.

While not up to the 741 in dc characteristics, the 3450 is quicker than many op amps that are faster than the 741. Its 350-nA maximum bias current is 1% that of some op amps. And its offset voltage, a maximum of 15 mV at 25°C (and no more than 30 mV at 100°C) is 20% that of another super-fast part, a recently announced GaAs op amp chip (ELECTRONIC DESIGN, March 20, p. 21). Also, offset voltage can be externally reduced to zero with a potentiometer.

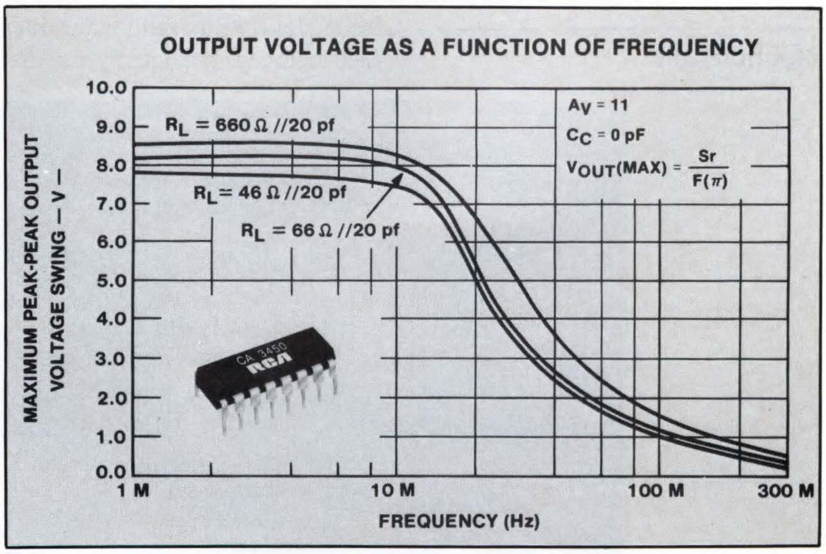
The CA3450 does require a hefty quiescent current of 35 mA. However, it can dissipate 1.5 W up to 55°C. Above that temperature, it must be derated at a rate of 16.6 mW/°C. Between 90° and 100°C (its maximum temperature), a heat sink is necessary and the chip must be derated more steeply—at 25 mW/°C. A heavy copper leadframe lets the op amp handle this kind of power even though it is housed in a 16-pin plastic DIP.

Working with the CA3450 requires careful attention to common-mode voltages; its common-mode rejection ratio is only 50 dB, minimum. When operating with ±6-V power rails, the 3450's maximum common-mode voltage is ±3.5 V. However, the video signals it is designed to handle rarely exceed 2 to 3 V so this should not be a problem. Maximum voltage between the power rails is 14.5 V, and the power-supply rejection ratio is a minimum of 60 dB.

The output of the amplifier can be protected from the effects of short circuits by inserting 10-Ω decoupling resistors between the power pins and the supply lines. Decoupling capacitors (0.001 μF) then connect the power pins to ground.

In quantities of 1000, unit price of the CA3450 is $9.00. Small quantities are available from stock.

RCA Solid State, Route 202 Somerville, NJ 08876; Len Metzger, (201) 685-7369. **CIRCLE 314**



Frank Goodenough

COMPUTER-AIDED ENGINEERING

ELECTRONIC DESIGN EXCLUSIVE

Logic synthesis program injects level-sensitive scan into ICs

Level-sensitive scan design is a technique that guarantees that all of the internal nodes of a complex logic array will be accessible to an IC tester. The approach provides 100% testability, which ensures the high reliability of production ICs, but it typically exacts a toll in chip real estate and the gate-array designer's time. The designer must make an extra effort to equip a circuit with scanning registers and ring counters.

Although little can be done about the 10% or 15% extra chip space required, at least adding the required scanning circuits can now be accomplished automatically. A synthesis program developed by Aida Corp., part of the company's Automatic Test Pattern Generation (ATPG) package, does just that.

Level-sensitive scan design exposes the inner logic of a complex design through built-in logic blocks that can be pulsed serially to supply a characteristic signature. The signature can then be read and interpreted by a specialized IC tester.

The logic blocks include scanning registers and serial rings that, under test, record the status of gates within combinatorial logic circuits that cannot be accessed by any other means. Although much simple combinatorial logic—AND, OR and NAND gates—may be tested with a carefully thought-out stimulus pattern, more complex logic will need some other means of revealing its functionality. A D flip-flop, for example, may not give a readable output until many clock cycles have passed. Some other mechanism is required to read the cell within one clock pulse (that is, before a valid output appears).

The synthesis program and library devised by Aida examines each logic cell, and determines what logic should be added to convert it into a scannable logic cell. In many cases, the synthesis program adds additional clock lines to provide the needed inputs and outputs.

Although the package must run with Aida software on an Apollo workstation or IBM mainframe, translators are available for converting Daisy and Mentor Graphics files into Aida-compatible schematics.

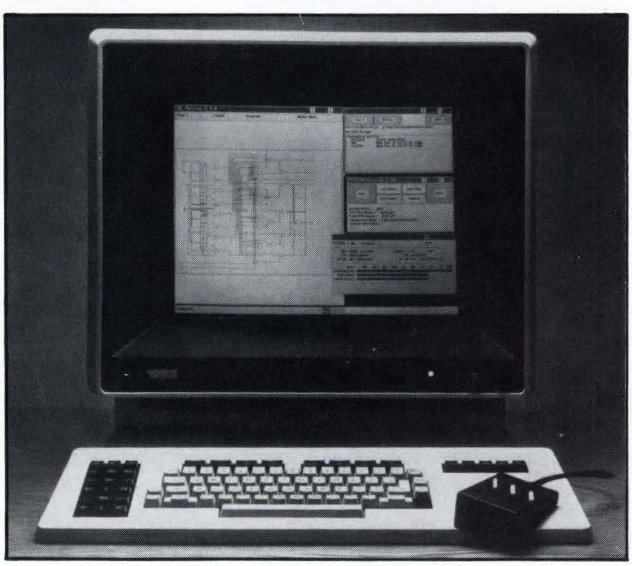
The synthesis package currently works with Fujitsu Microelectronics' 20K gate arrays, mapping out additional logic blocks and providing the additional pin-outs required for the chips to implement a level-sensitive scan. Synthesis software for other manufacturer's gate arrays will be announced soon. Outputs of the program are a net list compatible with Fujitsu's gate array simulation and layout programs.

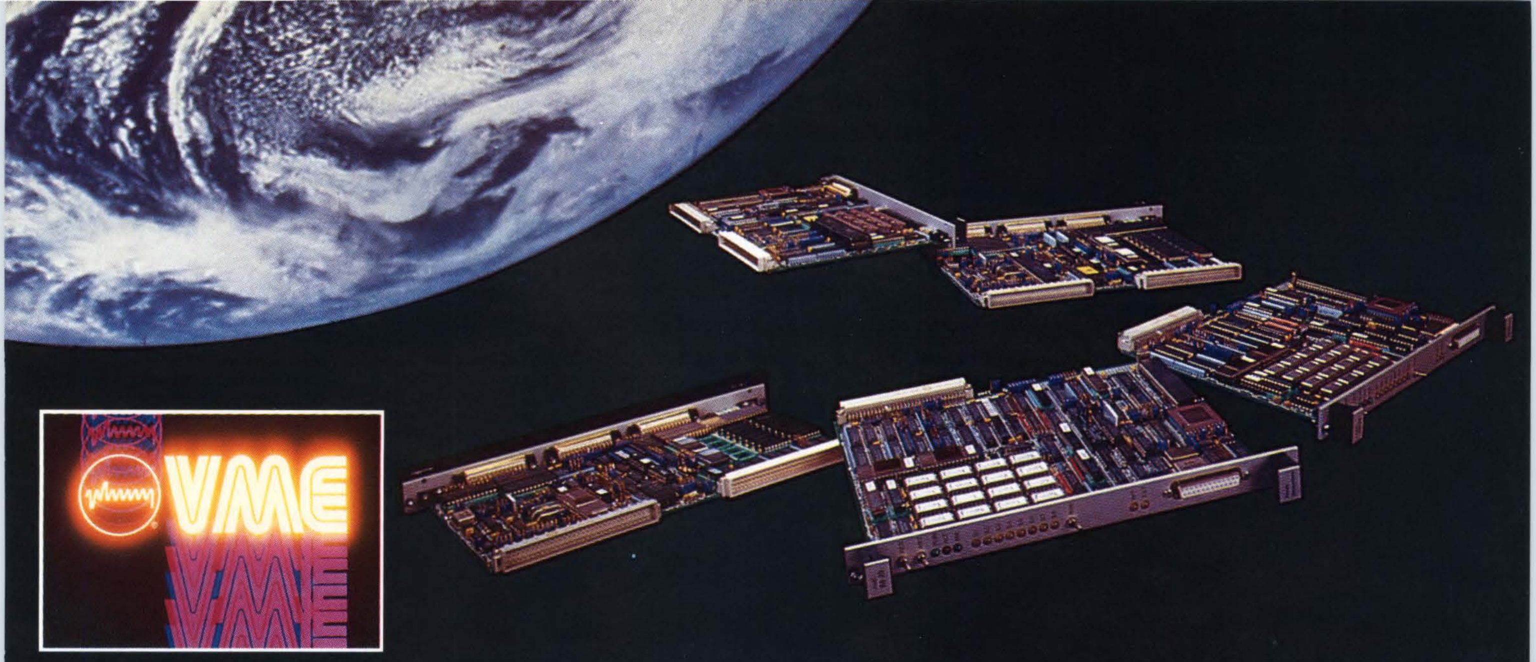
Generating test vectors is completely automatic. It is done by the synthesis program, but the vectors can be executed only on those IC testers equipped for level-sensitive scanning. The Fairchild Sentry 20 is the primary tester for that task, and test vectors are provided in its format. In the future, the system also will supply test vectors compatible with the Takada Riken line of testers.

The synthesis program is available for immediate delivery. For the Apollo computer, its price is $45,000.

Aida Corp., 3375 Scott Blvd., Suite 340, Santa Clara, CA 95054; Michael Chiang, (408) 748-8571. **CIRCLE 313**

Stephan Ohr





What in the world can you do with Plessey Microsystems VMEbus processor boards?

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Data acquisition, coprocessing and other multiprocessor environments.

Our PME 68-2D gives you up to 512 Kbytes of dual-ported RAM, and full system controller functions. Selecting or eliminating options on this processor allows you to develop the most cost-effective multiprocessor system.

The perfect UNIX engine, designed to optimize the performance of system hardware and software.

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NEW PRODUCTS

COMPUTER-AIDED ENGINEERING

Software eases programmable logic development

The third-party software crowd for programmable logic has just gained a powerful ally. Running on the IBM PC and its clones, the LOG/IC package developed by Elan Digital Systems optimizes devices, converts design files into any appropriate device (including gate arrays), and creates and prints computer-generated circuit block diagrams from input data. The package is also up and running on Apollo, Prime, and Digital Engineering's VAX computers.

The software's ability to create a circuit block diagram from the input data makes it possible for the user to verify his logic design and to supply final design documentation.

The design package allows an engineer to enter a design in the form of truth tables, state diagrams or logic equations (schematic capture is not yet available), select the target programmable device, and then optimize the design. Up to 32 inputs and 32 outputs can be handled simultaneously by the IBM PC implementation of the software. The version of the LOG/IC package intended for the VAX computer doubles that figure.

If the selected device cannot hold the entire circuit, those terms that cannot be realized are printed out, thus guiding the user to perhaps choose a different chip. Test vectors can be generated by the LOG/IC package to deliver 100% fault coverage.

The software will be available in four "capability" levels—the lowest handles design and user-generated simulation vectors for Monolithic Memories' PAL devices; the next adds all other programmable devices plus automatic test vector generation; the third adds the ability to design with microprogrammable logic; the fourth handles microprogrammable systems.

Prices range from $1190 for the lowest level on the IBM PC to $19,700 for the full VAX package.

Elan Digital Systems Inc., P.O. Box 1610, San Anselmo, CA 94960; (408) 734-2226. CIRCLE 311

Introducing the LH Research LM Series: a line of fully regulated, 250 to 600 watt, convection cooled switchers.

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UL recognized/CSA certified for easier system certification.

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MODEL NUMBER	WATTS OUT	OUTPUTS*				CASE SIZE	QUANTITY PRICING			
		MAIN VDC/AMPS	2 VDC/AMPS	3 VDC/AMPS	4 VDC/AMPS		1-9	10-49	50-99	100
LM11-1	250	5 @ 50				1	**$420**	**$390**	**$370**	**$345**
LM11-2	250	12 @ 21				1	**420**	**390**	**370**	**345**
LM11-3	250	15 @ 17				1	**420**	**390**	**370**	**345**
LM11-5	250	24 @ 11				1	**420**	**390**	**370**	**345**
LM11-6	250	28 @ 9				1	**420**	**390**	**370**	**345**
LMX22-12	300	5 @ 50	12 @ 9			2	**520**	**480**	**455**	**430**
LM23-122	300	5 @ 50	12 @ 5	12 @ 5		2	**550**	**510**	**480**	**455**
LM24-1221	300	5 @ 50	12 @ 5	12 @ 5	5 @ 1.5	2	**580**	**535**	**510**	**480**
LM24-1122	300	5 @ 50	5 @ 5	12 @ 5	12 @ 1.5	2	**580**	**535**	**510**	**480**
LM24-1331	300	5 @ 50	15 @ 4	15 @ 4	5 @ 1.5	2	**580**	**535**	**510**	**480**
LMX33-122	350	5 @ 50	12 @ 10	12 @ 9		3	**620**	**575**	**540**	**510**
LM34-1221	350	5 @ 50	12 @ 10	12 @ 5	5 @ 5	3	**650**	**600**	**570**	**535**
LM34-1522	350	5 @ 50	24 @ 5	12 @ 5	12 @ 5	3	**650**	**600**	**570**	**535**
LM34-1331	350	5 @ 50	15 @ 8	15 @ 4	5 @ 5	3	**650**	**600**	**570**	**535**
LM41-1	500	5 @ 100				3	**625**	**580**	**550**	**515**
LM41-2	500	12 @ 42				3	**625**	**580**	**550**	**515**
LM41-3	500	15 @ 34				3	**625**	**580**	**550**	**515**
LM41-5	500	24 @ 22				3	**625**	**580**	**550**	**515**
LM41-6	500	28 @ 18				3	**625**	**580**	**550**	**515**
LM54-1221	600	5 @ 100	12 @ 10	12 @ 5	5 @ 10	4	**815**	**755**	**715**	**670**
LM54-1212	600	5 @ 100	12 @ 10	5 @ 5	12 @ 10	4	**815**	**755**	**715**	**670**

CAUTION: Total loading of all outputs not to exceed rated output power.

Prices subject to change without notice.

*Many additional standard voltage/current output combinations are available; refer to 1985 General Catalog or contact factory.

Ordering Information (Typical part number encoded)

LM 2 3 – 1 2Y2 / 1 1 5

- **Series** — LM
- **Model*** — 2 3
- **Output V1** (table 1)
- **Output V2** (table 1)
- **Output V3** (table 1)
- **Output V4** (table 1)
- **Input Voltage** (115 or 230VAC)

OPTIONS Dual input voltage: use 115-230.
OVP for auxiliary output: add letter Y after auxiliary output voltage code.

*Last Digit = number of outputs.

Table 1	
0 = 2VDC	4 = 18VDC
1 = 5VDC	5 = 24VDC
2 = 12VDC	6 = 28VDC
3 = 15VDC	8 = 48VDC

Options for LM Series

DELIVERY
Most LM Series switching power supplies with selected options are shipped within 48 hours after placement of your order. Units with optional dual 115/230VAC input require 3-4 weeks.

OPTIONS	QUANTITY 1*
Dual 115/230V Input	$16.00
OVP (not available for outputs rated at 1.5A)	
1 auxiliary output	22.00
2 auxiliary outputs	44.00
3 auxiliary outputs	66.00

*For multiple unit pricing, contact factory.

Product Specifications

OUTPUT POWER
250 to 600 Watts maximum.

OUTPUT VOLTAGES
2, 5, 12, 15, 18, 24, 28VDC. 48VDC available on some models; contact factory.

OUTPUT CURRENT
See specific model.

NUMBER OF OUTPUTS
1 to 4.

COOLING
Convection.

INPUT VOLTAGE
92-130VAC or 184-260VAC, 47-440Hz.

HOLD-UP TIME
20msec in regulation minimum, after removal of nominal AC input.

LINE REGULATION
0.4% over entire input range for all outputs.

LOAD REGULATION
0.4% from no load to full load for all outputs, except 1.5A outputs are 1.5% or 70mV, whichever is greater.

INTERACTION (CROSS REGULATION)
0.1% maximum.

PARD (RIPPLE & NOISE)
1%p-p or 50mV, whichever is higher.

EFFICIENCY
Up to 80%; 70% typical.

POWER FAIL DETECTION
Upon removal of AC, the power fail signal drops to logic zero at least 2msec before loss of DC output. Upon AC turn-on, signal remains low until outputs are in regulation.

OVERVOLTAGE PROTECTION
Standard on V1. Factory set for 125% ± 5%. Optional on all auxiliary outputs except 1.5A.

CURRENT LIMIT
All outputs have current limiting.

REVERSE VOLTAGE PROTECTION
To 100% of rated current for main output.

OVERTEMPERATURE PROTECTION
Internal thermal switch turns off power supply if overheating occurs.

OVERSHOOT & UNDERSHOOT
2% maximum deviation with a load change of 25% at 5A/μsec. No overshoot or undershoot during AC turn-on or turn-off.

RESPONSE TIME
200μsec to within 1% after a 25% load change at 5A/μsec.

TEMPERATURE COEFFICIENT
±0.02%/°C from 0°C to 50°C after half hour warm-up.

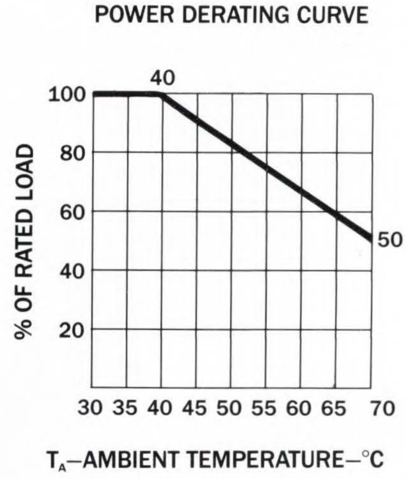
OPERATING TEMPERATURE
0°C to 70°C, full power to 40°C. Derates linearly to 50% power at 70°C.

STORAGE TEMPERATURE
−55°C to 85°C.

VOLTAGE ADJUST RANGE
±5% minimum, all outputs.

MINIMUM LOAD
Zero for single ouput models. 10% required on V1 of multiple output models to insure regulation of auxiliary outputs. Contact factory for minimum load if main output is other than 5V. Lack of minimum load will not damage supply.

OUTPUT POLARITY
All outputs are floating and may be referenced to each other or chassis ground as required. Outputs may be isolated up to 100 volts from chassis ground.



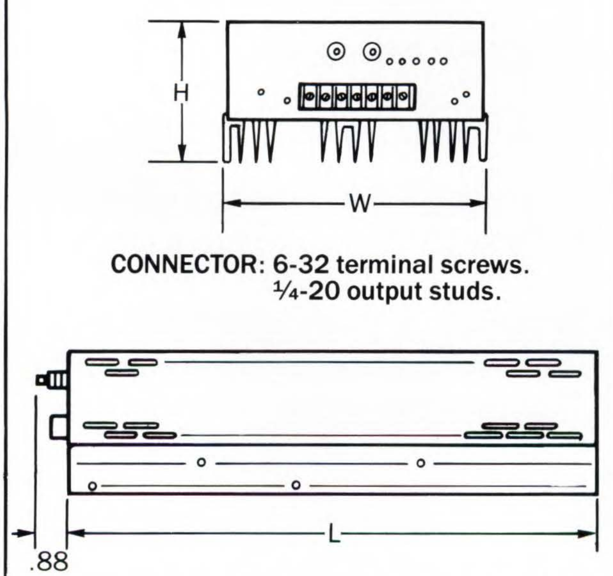
LIMITED INRUSH CURRENT
The AC input inrush current is limited to 42A rms when averaged over one cycle.

REMOTE SENSE
Standard on main outputs and auxiliary outputs having 5V current rating of 10A or greater. Compensates for up to 250mV of total lead cable loss. All outputs are internally sensed if the sense leads are opened.

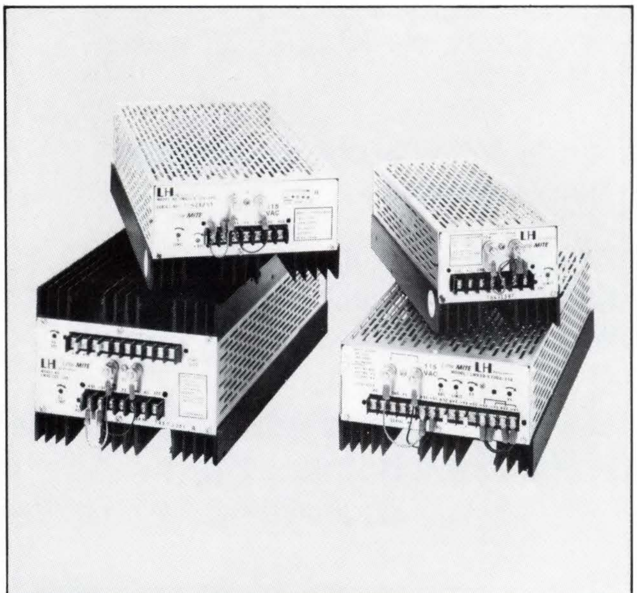
REMOTE ON/OFF
The power supply is turned on with open circuit or TTL logic '1' and turned off by switch closure or TTL logic '0'.

SAFETY
UL recognized. CSA certified.

OPTIONS
OVP on most auxiliary outputs.
Dual 115-230VAC inputs.



Note: Overall exterior dimensions may be increased by up to 0.194″ maximum on some models due to possible protrusion of hardware.



DIMENSIONS (in./cm.)

Case Size	L	W	H
1	11.25/28.58	5.00/12.70	4.00/10.16
2	11.25/28.58	5.00/12.70	6.45/16.38
3	15.03/38.18	7.50/19.05	4.12/10.46
4	15.00/38.10	7.50/19.05	6.00/15.24

Pcb prototyper links to CAD

A printed circuit board prototyping system is directly compatible with all major pcb CAD systems that provide output in the Gerber photoplotter format. The CM-3000 integrates the basic processes of artwork generation, automated drilling, and etching into a self-contained package which produces double-sided prototype circuit boards up to 10.0 by 16.5 in. System resolution is 0.001 in. with ±0.002-in. absolute accuracy.

ProtoCAD Inc., 1050 Elkton Dr., Colorado Springs, CO 80907; (303) 548-0222. $39,500; 45 days.

CIRCLE 316

Design software runs on Macintosh

With DesignScope, a software package for Apple's Macintosh computer, engineers can construct electronic circuits on the computer's screen and run simulations to verify the design. The software allows the user to develop block diagrams, assign parameters to the various blocks, and run a simulation while viewing the resultant waveforms. If a problem is encountered, component parameters can be easily changed and the simulation rerun. Amplifiers, comparators, filters, phase-locked loops, voltage-controlled oscillators, analog switches, voltage sources, integrators, differentiators, rectifiers, multipliers, peak detectors, sample and holds, delay lines, and noise generators are just a few of the component blocks available in DesignScope.

Brainpower Inc., 24009 Ventura Blvd., Suite 250, Calabasas, CA 91302; (818) 884-6911. $249.95.

CIRCLE 317

Software designs active filters

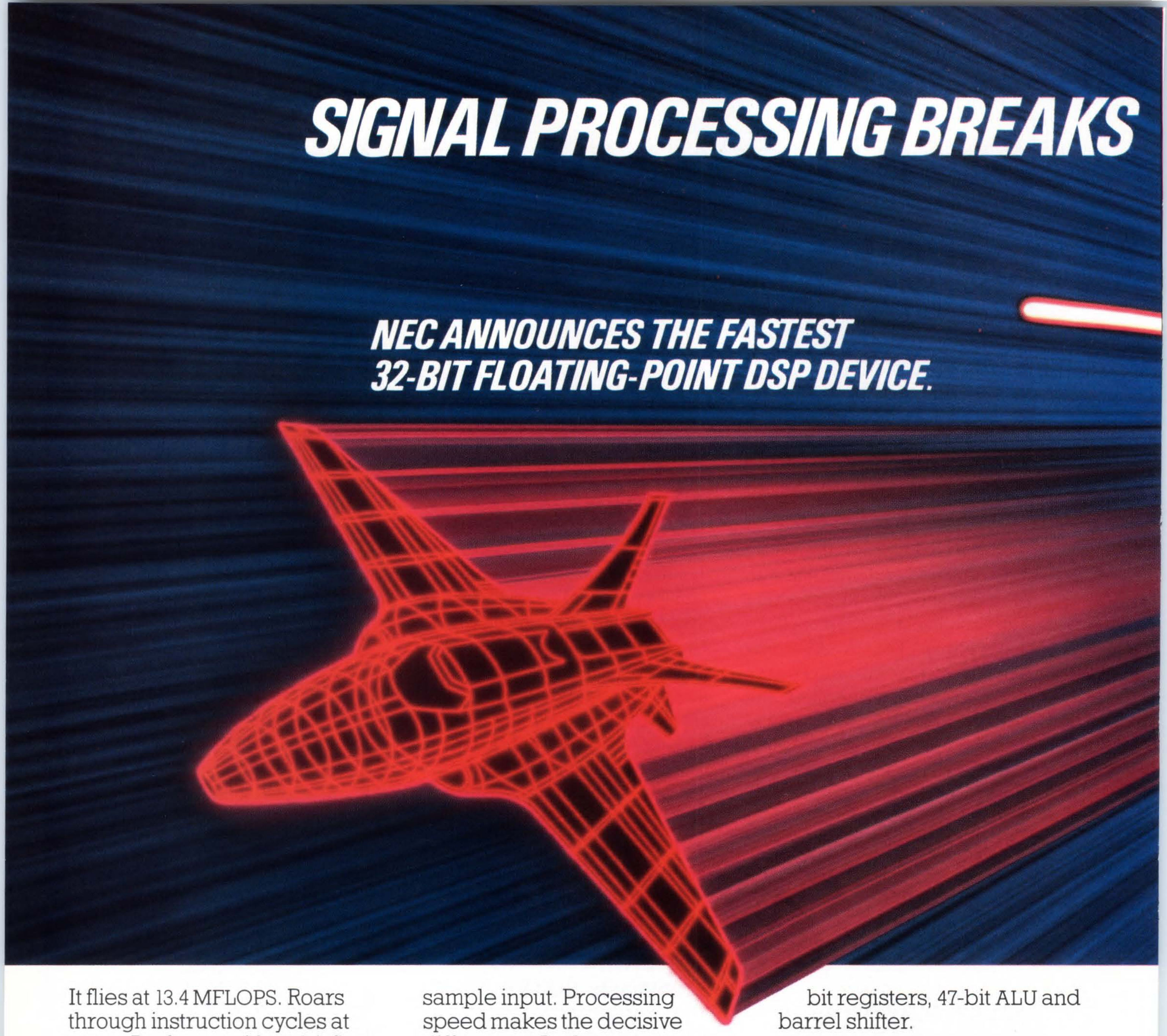
A software package for the IBM family of personal computers can be used to design Butterworth, elliptic, Chebyshev, and Bessel low-pass, high-pass, band-pass, and band-stop active filters. It also allows the direct entry of pole and zero locations or transfer functions. Facilities are included for cascading filters and storing filter data for future analysis or modification.

RLM Research, 1020 Albion Way, Boulder, CO 80303; (303) 499-7566. $450. **CIRCLE 318**

Simulation model supports 80386 μP

Logic Automation now offers SmartModel support for the Intel 80386 microprocessor. SmartModels are behavioral-level logic simulation models that run on popular CAE workstations and are accessed during simulation by the workstation's simulator. Available exclusively on SmartModels is Symbolic Hardware Debugging, a series of checks for timing and other error conditions. When an error occurs in the design, the model generates a message that pinpoints the exact cause, location, and time of the problem.

Logic Automation Inc., 19545 N.W. Von Neumann Dr., Beaverton, OR 97005; (503) 690-6900. $1830. **CIRCLE 319**



It flies at 13.4 MFLOPS. Roars through instruction cycles at 150ns. Performs with 32-bit floating-point precision. And packs all that processing power onto a single CMOS chip. NEC's μPD77230 Advanced Signal Processor gives you the edge in image processing, graphics workstations, telecom and instrumentation. Because it delivers overpowering advantages in speed, accuracy and expandability.

SPEED IS EVERYTHING.

Today's DSP devices work with sum-of-products algorithms that require hundreds of multiplication operations for each sample input. Processing speed makes the decisive difference. And no processor keeps pace with the 77230. It gives you 32-bit full floating-point arithmetic at 13.4 MFLOPS. And executes up to six concurrent operations, including multiply and accumulate, in a 150ns cycle.

IDEAL PRECISION.

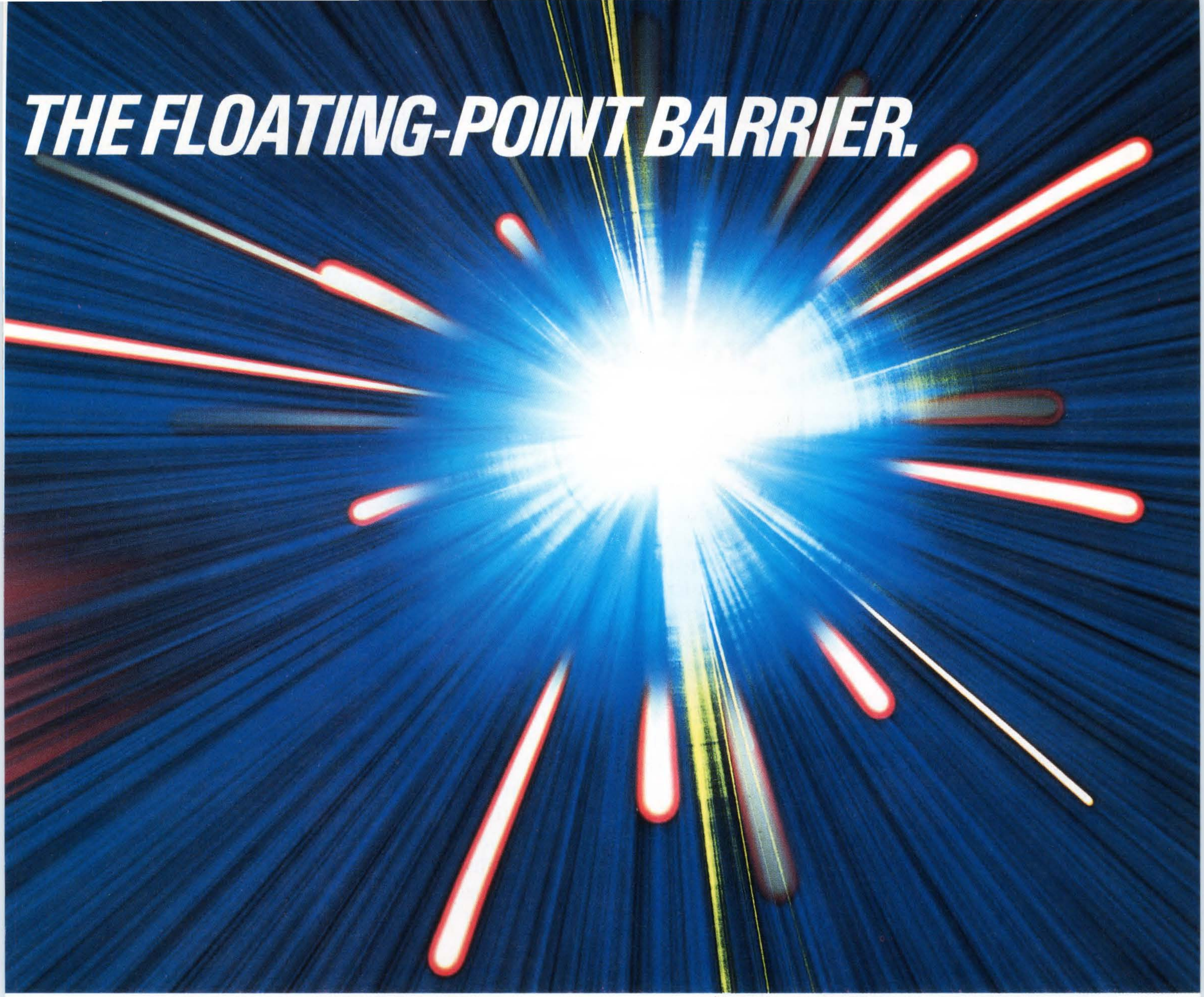
With 32-bit floating-point capability, our advanced signal processor eliminates problems with round-off error, quantization noise, scaling, limit cycles and over/underflow. And the 77230 is unique in offering a 55-bit multiplier result (8-bit exponent, 47-bit mantissa). With eight 55-bit registers, 47-bit ALU and barrel shifter.

EXPANDABILITY.

The 77230 not only provides large internal memory blocks (512 × 32 × 2 data RAM, 2K × 32 program ROM and 1K × 32 data ROM). It offers external expansion up to 4K of program RAM and 8K of data RAM. Serial and parallel I/O give you added flexibility. The serial interface links with codecs, DACs and AD converters. And opens the option of cascading. The parallel interface supports master- and slave-mode operations.

Find out how NEC's high-speed floating-point processor

C&C
Computers and Communications



can help your product break performance barriers and open new market opportunities.

Benchmarks (Floating-point or fixed)
- □1,024-point complex FFT 12.3ms
- □512-point complex FFT 4.7ms
- □2nd order biquad filter 0.9μs
- □32-tap FIR filter 5.25μs
- □Square root 9.0μs

	μPD77230	77220	7720	7720A	77P20	77C20
DESCRIPTION	Fixed-point			Die shrink	EPROM version	CMOS version
CYCLE TIME	150ns	150ns	244ns	240ns	244ns	244ns
PACKAGE	68 PGA	68 PLCC	28 DIP	28 DIP	28 DIP	28 DIP
POWER CONSUMPTION	0.8W typ.	TBD	1.4W max. 0.9W typ.	850mW max. 0.6W typ.	1.75W max. 1.35W typ.	200mW max. 120mW typ.
TECHNOLOGY	1.5μm CMOS	1.5μm CMOS	3.1μm NMOS	2.4μm NMOS	3.1μm NMOS	3.0μm CMOS
ON-CHIP MEMORY						
DATA RAM	1K×32	512×24	128×16	128×16	128×16	128×16
PROGRAM ROM	2K×32	2K×32	512×23	512×23	512×23	512×23
DATA ROM	1K×32	1K×24	510×13	510×13	512×13	510×13
OFF-CHIP MEMORY						
PROGRAM RAM	4K×32	4K×32	—	—	—	—
DATA RAM	8K×32	8K×24	—	—	—	—
INTERNAL BUS	32-Bit	24-Bit	16-Bit	16-Bit	16-Bit	16-Bit
MULTIPLIER	32×32	24×24	16×16	16×16	16×16	16×16
SERIAL I/O	5MHz	5MHz	2MHz	2MHz	2MHz	2MHz
SYSTEM CONFIGURATION	MASTER & SLAVE	MASTER & SLAVE	SLAVE	SLAVE	SLAVE	SLAVE

For further information, please contact:

■ **USA**	**NEC Electronics Inc.** **Tel:415-960-6000. TWX:910-379-6985**
■ **Europe**	**NEC Electronics (Germany) GmbH** **Tel:0211-650302. Telex:8589960 NE D.**
	NEC Electronics (Benelux) Netherlands **Tel:040-445-845. Telex:51923 NEC B NL.**
	NEC Electronics (Scandinavia) Sweden **Tel:08-732-8200. Telex:13839 NECSCAN.**
	NEC Electronics (France) S.A. **Tel:1-3946-9617. Telex:699499 NEC EF.**
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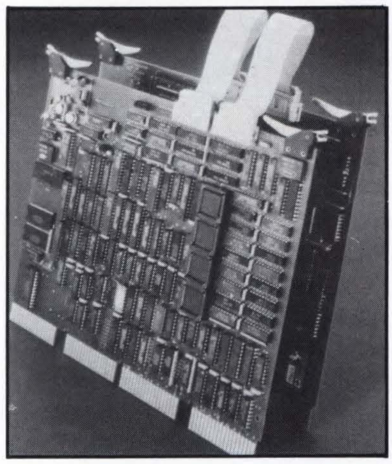
NEC

ELECTRONIC DESIGN EXCLUSIVE

Two-board Q-bus set processes real-time images



A pair of Q-bus boards provides MicroVAX II, Micro/PDP-11, and LSI-11 computers with unparalleled real-time performance. The Data Translation duo, for instance, performs convolutions 25 times faster than the MicroVAX II at a fraction of the cost: $4590 vs about $15,000. What's more, the duo replaces about a half-dozen existing boards.

The DT2651 frame-grabber is the first to perform real-time mathematical and logical operations on the Q-bus. It accepts nonstandard or standard video inputs, digitizes them, then applies the mathematical and logical operations. The results are then converted back to analog form for display on a monitor. The board contains an ALU that processes 8-bit images (512 by 512 pixels) at a 100-ns rate.

In turn, the ALU is part of a lookup table processor that feeds back data to the ALU from two 256-kbyte output buffers (organized as 512 by 512 by 8 bits). The board also includes four 512- by 8-bit input lookup tables and eight 256- by 24-bit output lookup tables; an 8-bit video analog-to-digital converter; a 4-channel input multiplexer; and a phase-locked loop. Completing the picture are three 8-bit video digital-to-analog converters for the red, green, and blue primary colors.

The companion board, the DT2658 auxiliary frame processor, has a 16-bit pipelined processor that connects directly to the frame grabber over special I/O ports. It includes a 512-kbyte frame-store memory, organized as 512 by 512 by 16 bits; a 256- by 32- bit histogram table; a histogram generator; six 256- by 16-bit conversion tables; division logic; and zoom, pan, and scroll circuitry.

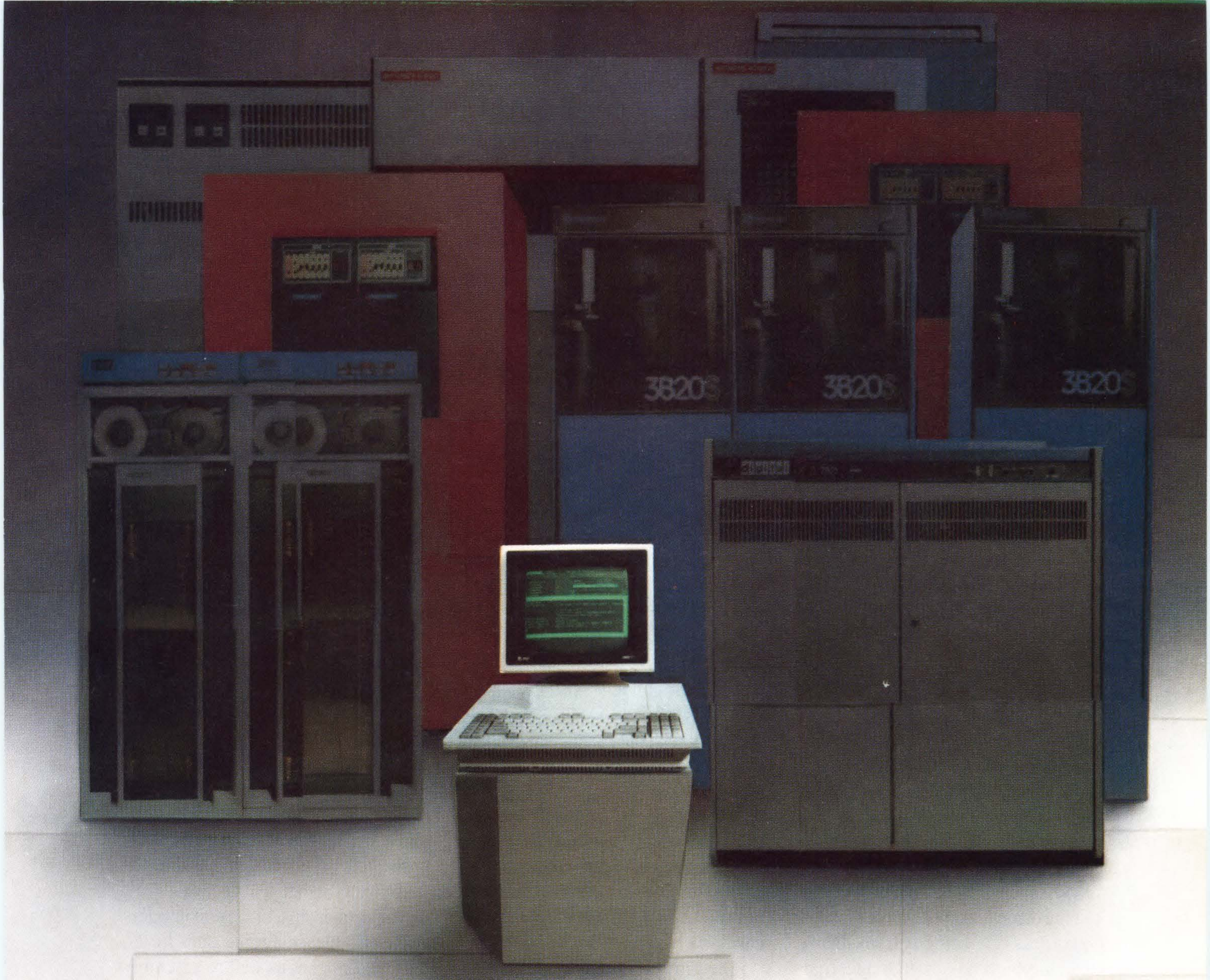
The processor board executes user-defined N-by-M convolutions at near real-time speed. For example, it outdoes the MicroVAX II by zipping through a 3-by-3 convolution on a full frame of 512- by 512- by 8-bit pixels in a mere 0.85 seconds.

The board also makes possible 16-bin histograms and performs all pixel calculations at 16-bit accuracy. Other functions include X2, X4, and X8 zooming, frame averaging, logic operations, multiplication and division, frame addition and subtraction, and logarithmic or arbitrary normalization.

The frame grabber is priced at $2995 and the processor at $1595. Both are available from stock.

Data Translation Inc., 100 Locke Dr., Marlboro, MA 01752; (617) 481-3700. **CIRCLE 303**

Roger Allan



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COMPUTER BOARDS

ELECTRONIC DESIGN EXCLUSIVE

Board pair transforms PCs into 32-bit high-resolution machines

Engineers working with personal computers can now upgrade them into 32-bit processors that deliver high-resolution graphics. In fact, Definicon Systems two-card set shoehorns the power of a full 32-bit 68020, running at 16.7 MHz, into an IBM personal computer or compatible. Furthermore, the card set can deliver a screen resolution of 1280 by 960 pixels.

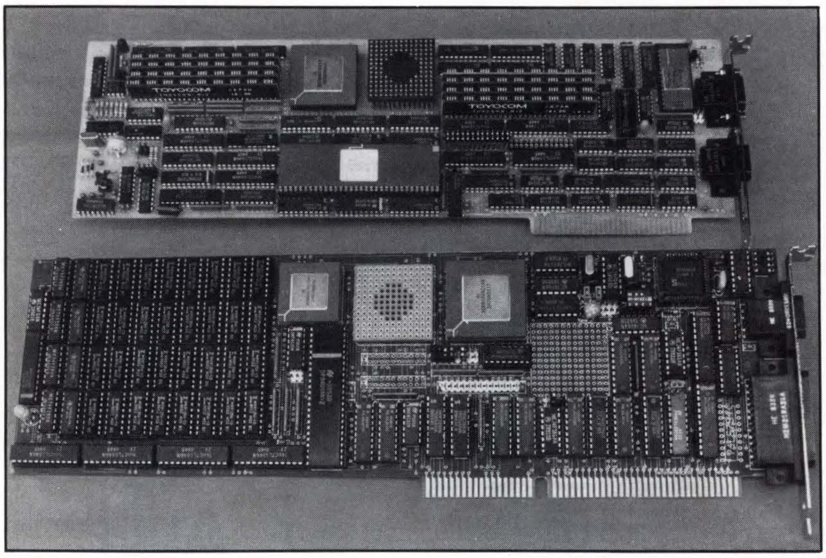
The board combination handles resolutions ranging from 1280 by 960 pixels down to 320 by 200 pixels (for CGA compatibility). Up to 256 colors can be displayed from a palette of 1.6 million.

Moreover, the dual-card set does not require the high overhead of a Unix-class operating system. Definicon has built a Unix-like shell that looks like Unix to an application program. Unix System V applications can run on this shell, but most of the I/O functions are passed to the PC's own DOS for processing.

Ray Weiss

The 780 processor card contains a 68020, a 68881 floating-point coprocessor, and four Mbytes of dynamic RAM. A National 8419 RAM controller directs the memory, which is built up of 256-kbyte, low-profile SIPS. The RAM is designed to be upgraded to 16 Mbytes: All of the chips are socketed for easy replacement, and the memory SIPS used are pin-compatible with forthcoming, higher-density 1-Mbyte parts. Also, the 8419 can be replaced with the 8429 controller designed for 1-Mbyte chips. Finally, the board can be used without the graphics card.

The graphics engine is linked to the 780 by moving the latter's 68881 onto the graphics card and replacing it with a connector that bridges the two boards. The graphics card is built around the new Hitachi 63484 chip, which furnishes a set of graphics primitives.



By closely coupling the two cards, the power of the 68020 can be used to directly build the display bit map. For graphics operations that require floating-point math, the 68020 can be used; for primitive operations, the graphics chip is employed. Relying on a unique bus design, the 68020 can directly access the frame memory, bypassing the 63484. The graphics card holds 2 Mbytes of frame memory, which allows the user to keep multiple windows of data while maintaining the full-screen bit map for high-speed hardware windowing.

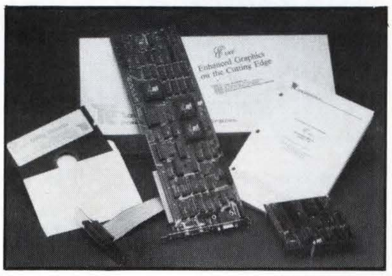
A number of language compilers are available, including ones for C, Pascal, Fortran, as well as assembly language. The card is supplied with a real-time multi-tasking kernel, a load driver for the PC CPU, a linker, and a debugging monitor. System V Unix will be available in the fall of this year, as well as Motorola's virtual memory chip.

Actually, the card set can be teamed with a second 780 processor card. Also, one of the card sets can be paired with a Unix-based 32032 card that Definicon makes, allowing one 68020 to be fully dedicated to graphics processing.

The fully loaded 68020 card cost $3295 apiece. Lower-cost versions are available with 12.5-MHz parts and restricted to 16 colors out of a 256-color palette.

Definicon Systems Inc., 31324 Via Collinas, Suite 108, Westlake Village, CA 91362; (818) 889-1646. **CIRCLE 315**

Graphics card has zoom function



EVA (Enhanced Video Adapter) is a color graphics board that improves on the IBM EGA standard by providing a compatible superset of extended features. Based on Tseng's ET2000 graphics chip set, the board's zoom capability makes possible up to 8× linear magnification on the X axis and as much as 16× on the Y axis.

The EVA board doubles the maximum font size from IBM's 8 by 32 pixels to 12 or even 16 by 32 pixels. It also offers a third hardware window, a microsequencer for fast raster operation, and a 132-column text display.

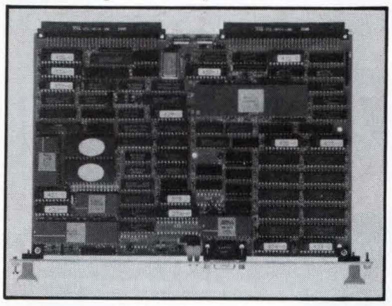
Tseng Laboratories Inc., 205 Pheasant Run, Newtown, PA 18940; (215) 968-0502. $525. **CIRCLE 367**

ESDI controller works on VMEbus

The Model 712 is a high-performance controller for ESDI (Enhanced Small Disk Interface) disk drives on the 32-bit VMEbus. It can support four of the industry-standard drives, up to and including the recently announced 1.2-Mbyte/s devices. Full VMEbus address and data support allows 8-, 16-, or 32-bit operating modes to be selected in software. A programmable throttle that determines the length of time the controller remains on the VMEbus is another software-selectable option. To ensure maximum throughput, the board comes with a 2-kbyte command buffer, and it is also filled out with an 8-kbyte FIFO buffer.

Xylogics Inc., 144 Middlesex Tpke., Burlington, MA 01803; (617) 272-8140. $1295 (1000 units); 60 to 90 days. **CIRCLE 368**

VME card displays 640 by 480 pixels



The VG-640 color graphic controller brings 640-by-480-pixel resolution to the VMEbus. It is capable of drawing up to 35,000 vectors/s (30-pixel vectors). Character drawing speeds reach 5000 char/s, while raster operations are handled at 1,200,000 pixels/s. A complete screen can be drawn in under a second. The single dual-height card can display 256 colors from a palette of 262,144. Over 90 high-level graphic commands are available, including two- and three-dimensional drawing, modeling transformations, windowing, projection and viewing, and image transmission.

Matrox Electronic Systems Ltd., 1055 St. Regis Blvd., Dorval, Que., Canada H9P 2T4; (800) 361-4903 or (514) 685-2630. $2995. **CIRCLE 369**

Board transfers 360,000 bytes/s

Two carrier boards that plug into the IBM PC and compatibles each provide mounting space, power, and intermodule communications for up to three instrument modules of Burr-Brown's PCI-20000 data acquisition, test, measurement, and control system. One board also has DMA capability to allow high-speed transfers of analog, digital, and counter data to or from the PC memory at rates of up to 360,000 bytes/s. Both the PCI-20041C-2 and PCI-20041C-3 offer interrupt-driven or polled modes of operation and an 8-MHz pacer clock for timing data acquisition and transfers.

Burr-Brown Corp., P.O. Box 11400, Tucson, AZ 85734; (602) 746-1111. $595 and $695 (DMA version). **CIRCLE 370**

Kit builds 32-bit computer board

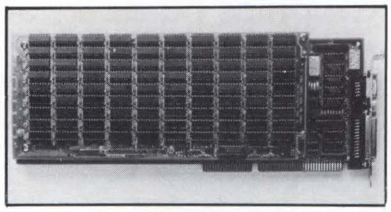
Two versions of an economical designer kit provide the key components needed to build a personal 32-bit single-board computer. Each kit—one based on the NS32016 and the other on the NS32032—provides the complete computing cluster chip set, including CPU, memory-management unit, floating-point unit, timing and control unit, and interrupt control unit. Development aids such as firmware, manuals, application notes, and a data book are also included in the kit.

National Semiconductor Corp., 2900 Semiconductor Dr., P.O. Box 58090, Santa Clara, CA 95052; (408) 721-6874. $59 (NS32016) and $75 (NS32032). **CIRCLE 371**

COMPUTER BOARDS

AT board expands memory to 4 Mbytes

A multifunction board for the IBM PC AT, the IDEA Supermax/EMS, expands the computer's memory to 4 Mbytes. The card also contains two serial ports and one parallel port. It is compatible with software applications written to the Lotus/Intel/Microsoft expanded memory specification (EMS). Included with the card is print spooling software that uses expanded

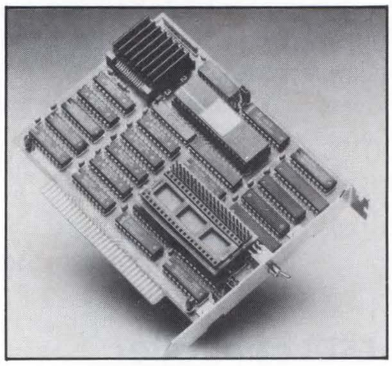


memory to print large files. The RAM can also be used to create a large virtual disk up to the total system memory. The base model can be fitted with from no memory to 1.5 Mbytes of RAM. With a daughter card the capacity increases to 4 Mbytes.

IDEAssociates Inc., 35 Dunham Rd., Billerica, MA 01821; (617) 663-6878. From $495 to $2595.

CIRCLE 320

PC accelerator fits half slot



The TinyTurbo 286 accelerator board triples the processing speed of an IBM PC or XT, yet requires only a half-size slot in the expansion chassis. Its 80286 processor plugs directly into the host computer's 8088 CPU socket, while the 8088 is plugged into a socket on the TinyTurbo. A toggle switch is used to alternate between the two processors. The board operates independent of, but in tandem with, the PC and is able to access all system memory.

Orchid Technology, 47790 Westinghouse Dr., Fremont, CA 94539; (415) 490-8586. $695.

CIRCLE 321

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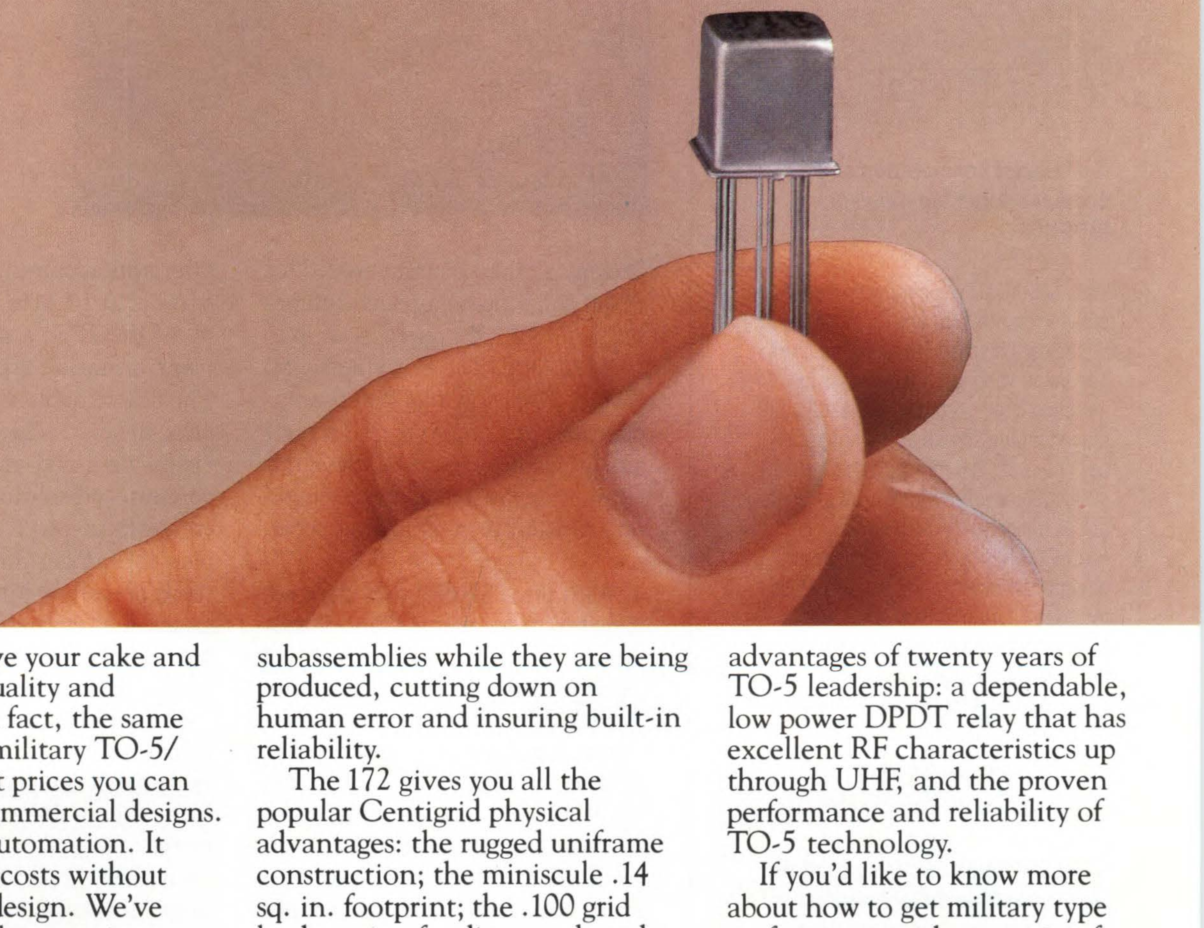
We put Centigrid® in civvies to save you money



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The 172 gives you all the popular Centigrid physical advantages: the rugged uniframe construction; the miniscule .14 sq. in. footprint; the .100 grid lead spacing for direct pc board plug-in without spreader pad, which retains the low .375 in. total profile.

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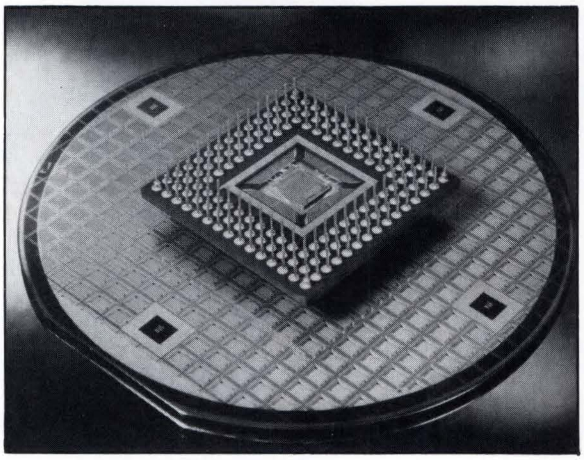
CIRCLE 54

NEW PRODUCTS

DIGITAL ICs

ELECTRONIC DESIGN EXCLUSIVE

32-bit CMOS MACs perform floating-point calculations



Packing all the resources needed for 32-bit IEEE floating-point arithmetic, the WTL3332 operates at up to 20 MFLOPS. The first single-chip CMOS 32-bit floating-point multiplier and accumulator, the circuit also carries a four-port, 32-by-32-bit register file, as well as three temporary registers to minimize bus accesses.

With three 32-bit buses on hand, transfers flow easily. Those buses plus a 33-bit instruction bus and various control signals let the WTL3332 make the most out of a 168-lead pin-grid array package. To reduce the number of pins to 144, the WTL3132 multiplexes all three 32-bit buses over a single 32-bit bidirectional interface bus. Moreover, it drops one of the instruction input pins.

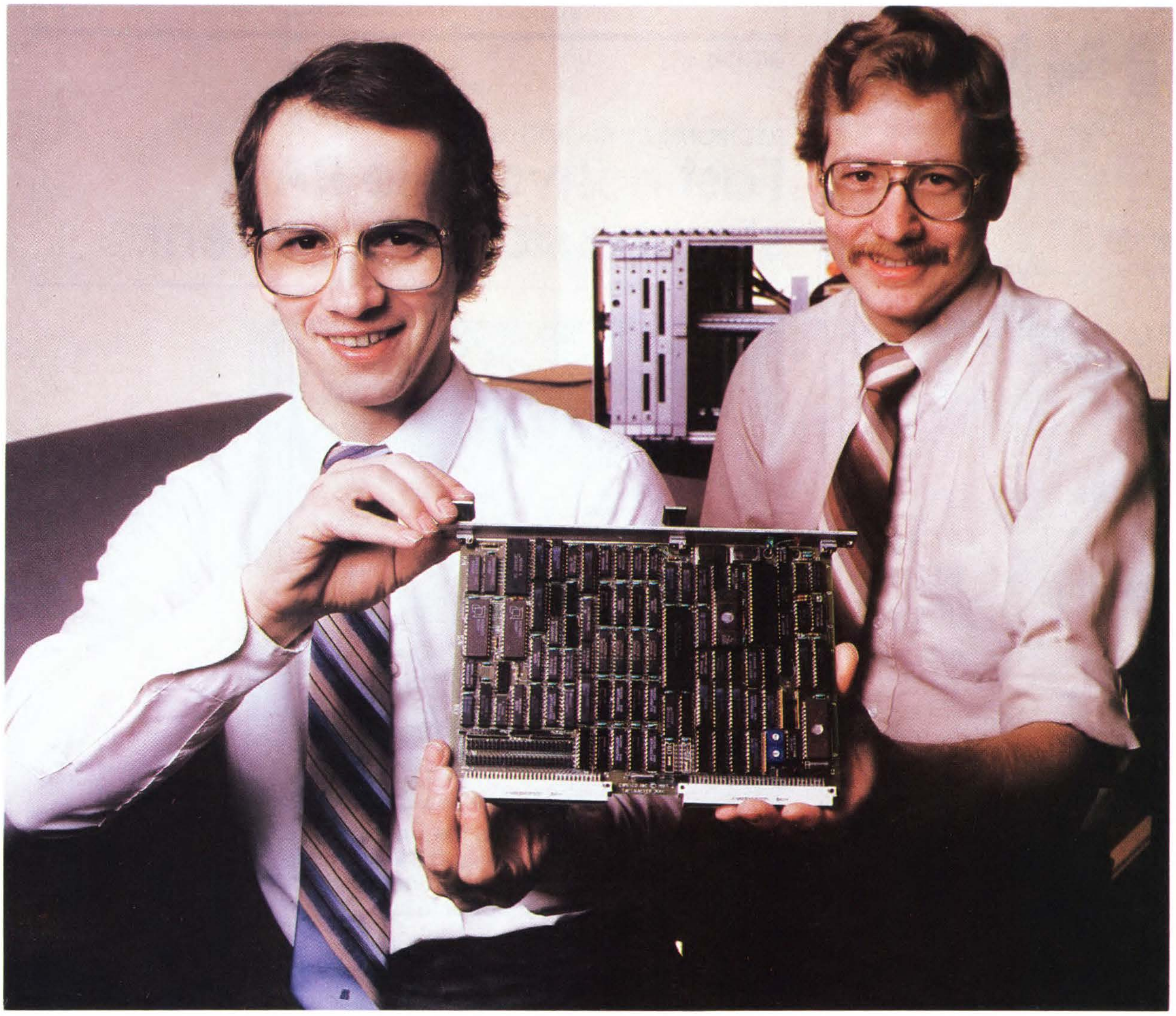
Either version of the multiplier-accumulator can operate with a 100- or 160-ns clock signal, which results in a throughput of 20 MFLOPS or 12.5 MFLOPS (both the multiplier and accumulator operate in parallel at 10 MFLOPS each). At 20 MFLOPS, a 4-by-4-matrix transformation takes only 1.6 μs. The device adds, subtracts, multiplies, divides (Newton-Raphson division via an on-chip ROM), and computes absolute values. It also converts to and from two's complement integer format. However, for multiplications, ALU operations, and multiplication-accumulation, there is a register-to-register latency of three cycles.

In addition to the two speeds and pinout options, the chips will also be available in two operating temperature ranges—0° to 70°C for commercial use and −55° to +125°C for military applications. Just a 5-V supply is needed, and the maximum power demanded by any of the chips stays under 1 W. Samples of the chip will be available in August. Prices in 100-unit lots start at $350 (one port) and $425 (three port).

Weitek Corp., 1060 E. Arques Ave., Sunnyvale, CA 94086; (408) 738-8400. **CIRCLE 302**

Dave Bursky

YOU ASKED FOR A FAST VMEbus ½" TAPE CONTROLLER THAT WOULD ALSO OPTIMIZE YOUR SYSTEM'S PERFORMANCE



Tapemaster 3000 design engineers Bob Simning and Larry Hull

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With this architecture we've given you the ability to operate the slowest start/stop to the fastest GCR caching tape drives at maximum efficiency on the VMEbus. You've asked us for the highest performance products possible. At Ciprico we listen . . . and respond.

CIRCLE 81

Other Tapemaster 3000 features include:

- 32 bit addressing, 8, 16, or 32 bit data transfers
- Programmable interrupt level and interrupt vector
- Hardware byte-order swapping
- Supports pass-through commands with optional parameters to support vendor-unique features
- Three cable exit options: through P2, from on-board connector, or through additional face-plate
- Scatter Read/Gather Write
- Reads or writes tape records of unknown and unlimited record length
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- Companion board to the Ciprico Rimfire 3200 VMEbus SMD-E disk controller

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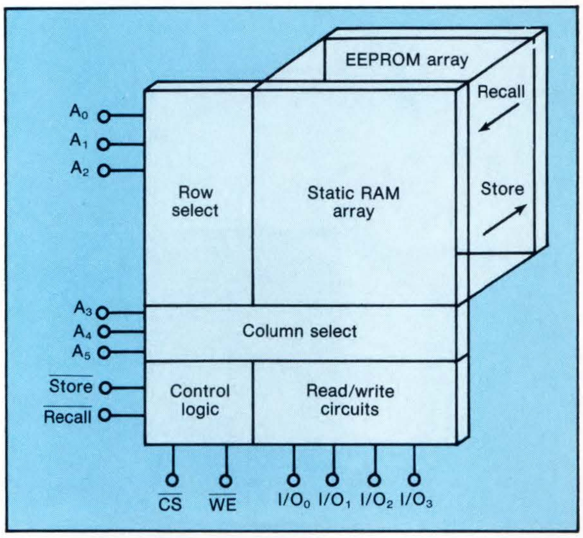
ELECTRONIC DESIGH EXCLUSIVE

Fast nonvolatile RAM slashes standby current



Nonvolatile RAMs overcome the slowness of stand-alone EEPROMs by using a RAM array for quick reads and writes, moving data to the built-in EEPROM only during a power failure.

Playing the game of electronic leap-frog, Catalyst Inc. has slashed nonvolatile RAM standby current from 60 mA to 30 μA, at the same time shaving access times from 300 to 200 ns. With such low standby current, the 1-kbit CAT22C12 is suited to applications like car phones or pocket dialers.

CMOS is behind the lower power and higher speed, no simple feat because the higher voltages of EEPROM cells tend to throw CMOS logic into a latch-up tailspin. CMOS construction also extends the operating temperature range on the low end down to $-40°C$.

The CAT22C12 contains 1 kbit of RAM and 1 kbit of EEPROM, both organized as 4 by 256 bits. A microprocessor can read and write to the RAM in 200 ns and can command the part to copy the RAM data into the EEPROM for preservation during power failure (see the figure). The copying operation takes 10 ms. Another first for Catalyst is circuitry that automatically copies data from RAM to EEPROM without processor intervention.

The RAM requires a single 5-V supply, which draws 30 mA during read or write operations, then reverts to 30 μA on standby. Versions of the device are available with access times of 200, 250, or 300 ns. The 18-pin JEDEC part is available immediately. In quantities of 100, the 1-kbit CAT22C12 (200-ns version) is priced at $14.87; a smaller version, the CAT22C10, offers 256 bits of storage (arranged as 4 by 64 bits) for $5.65.

Curtis Panasuk

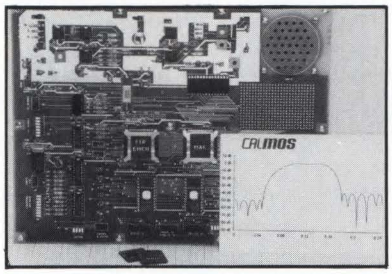
Catalyst Inc., 1800 Wyatt Dr., Suite 17, Santa Clara, CA 95054; (408) 980-9144. **CIRCLE 304**


Ford

NEW PRODUCTS

DIGITAL ICs

Evaluation kit builds FIR filter



A programmable 16-bit, 128-tap FIR filter can be built with an evaluation kit from Calmos Systems. Based on the company's CA128X16 data-memory and control-unit IC, the kit comes complete with a pc board and parts kit including the CA128X16, a-d and d-a converters, EPROM set, audio amplifier with speaker, and full technical documentation. Wire-wrap prototyping space is also available on the board for filter customization.

Calmos Systems Inc., 20 Edgewater St., Kanata, Ont., Canada K2L 1V8; (800) 267-7231 or (613) 836-1014. $500. **CIRCLE 322**

Logic arrays offer up to 10,013 gates

High-performance CMOS logic arrays, the RL7000 series, provide from 880 to 10,013 equivalent gates. The product family is identical to the LL7000 series of HCMOS arrays developed by LSI Logic. The RL7000 series uses 2-μm technology and has eight master-slice options. The devices operate at 1.4 ns/gate and consume just 18 μW/gate/MHz. They are suitable for replacement of high-speed SSI and MSI logic devices. Extensive macrocell and macrofunction libraries are available.

Raytheon Co., Semiconductor Division, 350 Ellis St., Mountain View, CA 94039; (415) 966-7716. **CIRCLE 323**

DIGITAL ICs

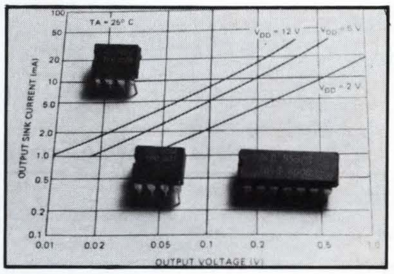
Floating-point ICs rival NMOS chips

Able to drop into sockets established by the popular NMOS 1064/1065 and 2064/2065 floating-point multiplier and ALU chips created by Weitek, the IDT72064/72065 and IDT72264/72265 CMOS equivalents consume less than a third the active power. The IDT chip sets provide the first direct replacement for the Weitek chips and operate from a single +5-V supply, eliminating the need for the second supply used by the Weitek devices. The CEMOS II process used to fabricate the chips allows operating speeds about 20% faster than the Weitek chips when performing the same IEEE 64-bit floating-point calculations—10 MFLOPS for pipelined ALU operations or single-precision multiplications.

Integrated Device Technology Inc., 3236 Scott Blvd., Santa Clara, CA 95054; (408) 727-6116.

CIRCLE 324

CMOS timer sinks up to 80 mA



A CMOS timer chip, the ALD555, can drop into existing sockets for the popular NE555, but opens up new opportunities and system upgrades thanks to its ability to sink up to 80 mA (at 5 V). Additionally, the chip offers expanded timing ranges due to a guaranteed input leakage current of no more than 200 pA. Thus, on the high-frequency side, the timer can operate in a monostable mode and deliver pulses as short as 500 ns, while on the low-end of the range, timing periods can extend to several days when a low-leakage capacitor is used with the chip. The timer can operate over a 2- to 12-V range and consumes just 100 μA in its quiescent state.

Advanced Linear Devices Inc., 1030 W. Maude Ave., Suite 501, Sunnyvale, CA 94086; (408) 720-8737. From $0.71 for dice or 8-pin plastic DIP to $1.18 for 14-pin DIP (100 units); stock. **CIRCLE 325**

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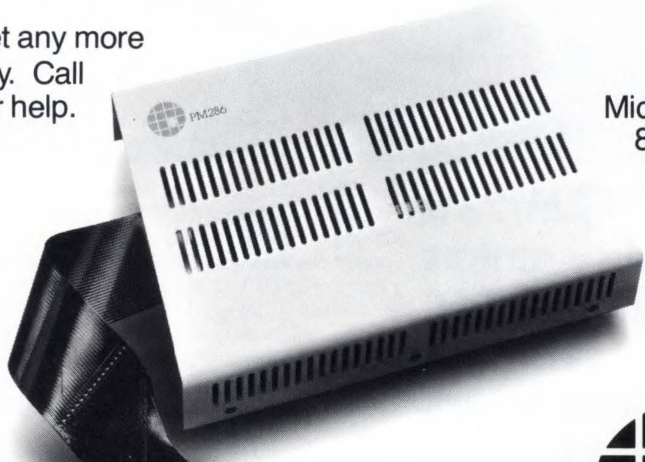

Microcosm Supports 8088, 8086 80188, 80186, 80286, V20, and V30 Microprocessors.

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CIRCLE 87

Dc-dc converter powers LAN chips

A line of 24-pin DIP dc-dc converters is capable of delivering −9 V to power Cheapernet local-area transceiver chips (National Semiconductor's DP8392 and Advanced Micro Devices' AM7995). The units take power from a +5- or +12-V dc power bus and convert those voltages into −9 V dc at either 100 mA regulated or 145 mA unregulated. I/O isolation is specified at 500 V ac. Eight models are available in the CM600 series with 5- or 12-V dc inputs, with or without a PI input filter.

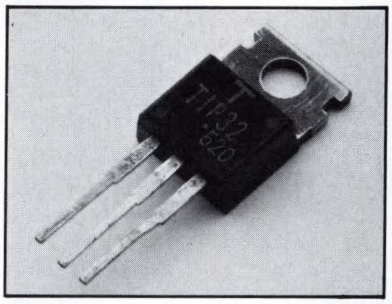
Computer Products Inc., Power Products Division, 2900 Gateway Dr., Pompano Beach, FL 33069; (305) 974-5500. From $36.75; stock to six weeks. **CIRCLE 326**

Kits simplify HIVIC design

Two prototyping parts kits shorten the time between prototyping and developing a production-version high-voltage integrated circuit (HIVIC). Each kit contains components capable of operating at up to 500 V. The TMH5155 is housed in an 18-pin plastic DIP and contains n- and p-channel enhancement-mode DMOS FETs. It also has both a high-voltage thyristor and an insulated-gate thyristor, plus a high-voltage diode. The TMH5156, in a 16-pin DIP, packs an npn bipolar transistor, n-channel depletion-mode DMOS FET, and a pair of p- and n-channel enhancement-mode DMOS FETs.

Telmos Inc., 740 Kifer Rd., Sunnyvale, CA 94086; (408) 732-4882. $10.75 each (25 units). **CIRCLE 327**

Transistors handle 1 to 6 A



A series of transistors is designed for high-power switching applications such as hammer drivers, pulse motor drivers, and inductive load switching. The TIP series consists of 24 devices which offer sustained collector power dissipation from 30 to 65 W and collector current from 1 to 6 A. The triple-diffused silicon transistors are housed in TO-220AB packages and are available in complementary npn and pnp types.

Toshiba America Inc., Semiconductor Division, 2692 Dow Ave., Tustin, CA 92680; (714) 832-6300. $0.20 to $0.44 (1000 units). **CIRCLE 328**

MOSFETs boast fast switching

High-speed switching coupled with very low input and output capacitances make the ZVN14 family of n-channel MOSFETs an ideal choice for high-speed test equipment and telephone switching circuitry. Turn-on and turn-off times fall into the subnanosecond range, while input and output capacitances are 6.5 and 3.0 pF. The devices also feature drain-source breakdowns to 90 V for low drain current requirements of up to 10 mA.

Ferranti Semiconductors, 87 Modular Ave., Commack, NY 11725; (516) 543-0200. $0.20 (10,000 units); stock to six weeks. **CIRCLE 329**

Darlingtons handle 1-A collector current

A series of medium-power Darlington amplifier transistors, ZTX600, handles collector currents of up to 1 A, making it ideal for automotive and industrial applications. Pulsed currents of up to 4 A and gains of up to 100,000 are possible. The V_{CEO} ratings are 140 and 160 V. The parts come in E-Line packages produced by injection molding of a silicone plastic. The resulting encapsulant, coupled with the transistor chip, permits junction temperature operation to 200°C. That is equal to temperatures of metal-can devices with power dissipations up to 1.5 W.

Ferranti Semiconductor, 87 Modular Ave., Commack, NY 11725; (516) 543-0200. Less than $0.18 (50,000 units); stock. **CIRCLE 330**

Power transistors handle 200 W

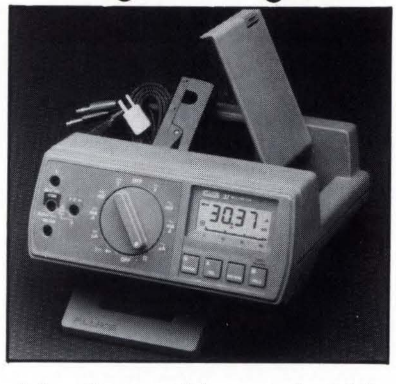
A series of complementary npn and pnp silicon power transistors handle voltages of up to 150 V and currents up to 25 A. The devices are designed for motor controls, high-current amplifiers, and switching circuits. The collector current is 25 A at an h_{FE} of 12. Typical switching time at a collector current of 10 A is 0.3 μs.

Solitron Devices Inc., 1177 Blue Heron Blvd., Riviera Beach, FL 33404; (305) 848-4311. From $4.50 (100 units); six to eight weeks. **CIRCLE 331**

NEW PRODUCTS

INSTRUMENTS

Meter displays analog and digital



A benchtop multimeter, the Fluke 37, features a combined analog and digital display in a case designed to improve ease of use and functionality. With 0.1% basic dc accuracy and wide bandwidth ac response, the unit meets or exceeds the specifications of any $3^1/_2$-digit bench multimeter. A carrying handle is molded into the case for portability, and the front panel has a 15° slope for optimum visibility.

John Fluke Manufacturing Co. Inc., P.O. Box C9090, Everett, WA 98206; (800) 426-0361 (206) 347-6100. $229. **CIRCLE 332**

Digital tester suits military use

A MATE-compatible digital word generator/analyzer, the System 45, supports all ATLAS digital test types for military environments. It has 128 to 1024 bidirectional channels. A modular design allows a user to build a system to match testing requirements. A complete system includes the Test Module Adapter, a control chassis, and an expansion chassis. The TMA is linked to a host via an IEEE-488 bus.

Interface Technology, 2100 E. Alosta Ave., Glendora, CA 91740; (818) 914-2741. Typical configurations start at $44,000; 12 to 16 weeks. **CIRCLE 333**

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NEW PRODUCTS

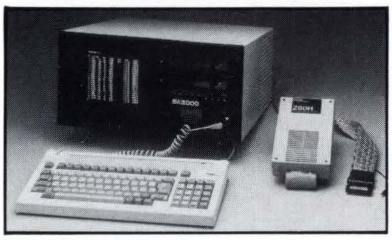
INSTRUMENTS

Menu-driven system logs data and more

The PCI ControLOGraph is a fully integrated, IBM PC-compatible hardware and software system for data logging, graphics display, alarm annunciation, and digital control. Hardware consists of modules from Burr-Brown's PCI-20000 family of data acquisition, test, measurement, and control products. Data inputs include 21 analog signals, 24 digital bits, and 3 frequency/event counting channels. To ensure ease of use, menu-driven software guides the inexperienced user through the configuration process.

Burr-Brown Corp., P.O. Box 11400, Tucson, AZ 85734; (602) 746-1111. $2750. **CIRCLE 334**

System handles any 8-bit CPU



The SA2000, a portable development system, can handle almost any 8-bit CPU and provides real-time emulation capability. The system's standard equipment includes a 9-in. CRT, twin 5¼-in. 360-kbyte disk drives, a keyboard, an EPROM programmer, 2 kbytes of trace memory, and an RS-232-C serial port.

Software bundled with the system consists of a screen editor, in-line assembler, and a debug command language that allows full symbolic debugging and the concatenation of operations.

Microprocessor pods for the portable unit are or will be available by the end of the third quarter for just about every 8-bit processor, including chips from Hitachi, Intel, Motorola, NEC, Rockwell, and Zilog.

Sophia Computer Systems Inc., 3337 Kifer Rd., Santa Clara, CA 95051; (408) 733-1571. $7995 (base unit including software and one pod); additional pods are available; they cost $3245 each. **CIRCLE 335**

Software supports test, measurement

Burr-Brown now offers three software support packages for its PCI-20000 system of data acquisition, test, measurement, and control products. The Basic, C, and Turbo-Pascal packages are for use with the IBM family of personal computers and look-alikes. Each effectively buffers the programmer from the details of the hardware by offering a set of calls to invoke all major hardware manipulations.

Burr-Brown Corp., P.O. Box 11400, Tucson, AZ 85734; (602) 746-1111. $225 each. **CIRCLE 336**

Simulator tests PCM systems

Designed for communication systems that use pulse-code modulation (PCM) techniques, the Model 515A PCM simulator generates a T-1 bit stream compatible with all the common D-bank formats, plus the extended superframe. For parametric characterization of DS1-compatible equipment, the unit can supply a wide range of digitized tones and signaling combinations on a selected channel.

T-COM Corp., 160 E. El Camino Real, Mountain View, CA 94040; (415) 964-3415. $3200. **CIRCLE 337**

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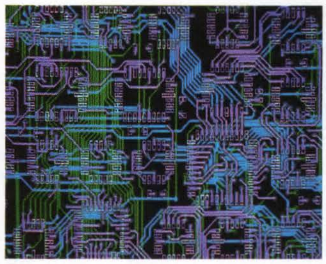
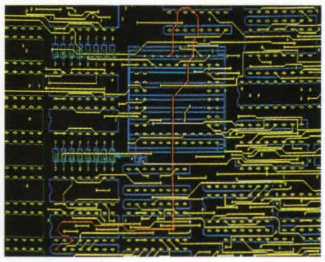
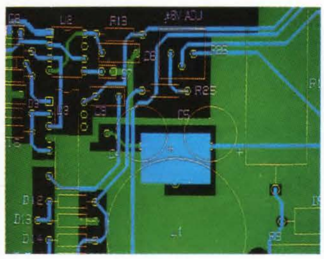


SMD TOOLBOX
For surface-mounted and thick-film hybrid designs.



ECL TOOLBOX
Automates design of transmission lines.



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CIRCLE 84

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Rely on our circuitry. EECOflex two-layer fully laminated switch circuits are screen printed on heat stabilized polyester. Conductors are always fully cured. Built-in shielding is available to block out EMI and ESD interference. State-of-the-art CAD equipment generates a prototype design with precision and speed —typically within 4 weeks after we receive your drawing. From prototype to final assembly, your EECOflex membrane's circuitry is built to work for you. Every time. And continue working. All switch elements are rated for an average lifetime of 5 million actuations.

Look into our graphics. You'll see bold, sharp, accurately registered overlays. Brilliant colors matched to individual lighting conditions. Take a closer look. At some of the most sophisticated graphics features in the membrane industry. Features like selective texturing for smooth integration of readout windows. Embossed key surround for definitive tactile location. A snap-dome contact system for tactile feedback to your operator. These and many more custom features add up to the visual appeal that sells your system. Up front.

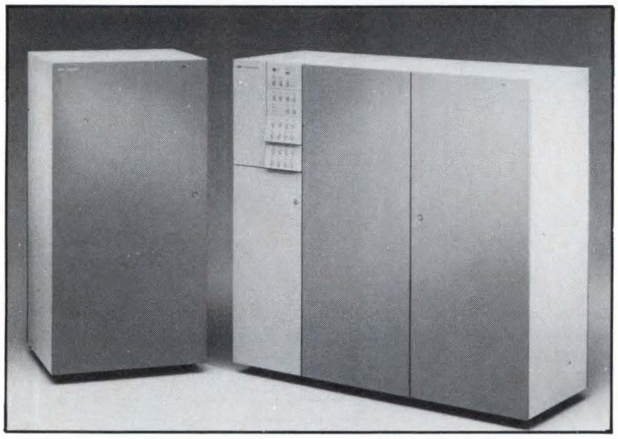
Give us your membrane design. We'll implement it your way. EECO applications engineers work with you from Day One to make sure our membrane meets your toughest design criteria. A dependable, professional service organization assures on-time delivery and follow-up assistance. Design questions? No problem. We're only a phone call away with designer's guides, test results and specifications. Call us at (602) 272-5645, TWX 910-950-0196. Or write EECO Incorporated, 1601 East Chestnut Avenue, Santa Ana, California 92702-0659 for a product catalog.

CIRCLE 92

COMMUNICATIONS

ELECTRONIC DESIGN EXCLUSIVE

Communications processor peaks out at 3.5 MIPS



Operating at an average of 3.5 MIPS, a large-scale communications processor triples the processing speed of its fastest competitors. Further, NCR Comten's 5660 lets it communicate with up to eight mainframes and handle 1024 communications lines.

The processor, which uses ECL macrocells and VLSI chips to achieve its speed, operates with high-speed T1 telephone lines and takes care of polling, application routing, and other tasks. The combination of quick processing and high-speed lines greatly improves throughput over processors that cannot perform other tasks while tied to a T1 line.

Overall speed is further improved by a 64-kbyte cache memory, one of the first implementations of a cache in a communications processor. Even when the necessary commands are not in the cache, though, throughput remains high. The main memory, which ranges from 4 to 6 Mbytes, is built around a four-port design that permits accessing of data from one port while the others are being filled with data, thereby eliminating loading and transfer delays.

The 5660 also furnishes extensive error checking and correction: fixing single-bit errors and detecting double-bit discrepancies. When irreparable errors are detected, the processor will log the error and then continue operating until interrupted for repair.

The system itself simplifies such repairs, incorporating an extensive subsystem that delivers self-testing and diagnostics. When problems arise, a built-in modem can be used to contact service personnel, denoting the nature of the problem and pinpointing a specific problematic board.

Pricing for a basic unit with 4 Mbytes of main memory, which handles 128 communications lines, is $540,000. Initial deliveries will begin this winter.

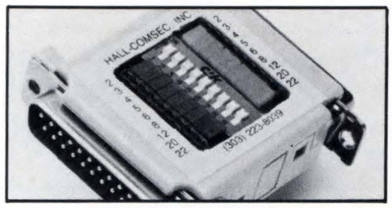
NCR Comten Inc., 2700 Snelling Ave. North, St. Paul, MN 55113; (612) 638-7777. **CIRCLE 305**

Terry Costlow

COMMUNICATIONS

Breakout box aids RS-232 diagnostics

WireTap, a miniature breakout box, assists diagnostics and configuration of RS-232 serial data lines. The pocket-sized unit permits observation of nine of the most commonly used signals by using 18 LEDs, two each per line. The LEDs provide visual evidence of positive and negative voltages while a 9-position DIP switch, dual 9-position female headers, and multiple jumper wires provide a simple way to reroute signals to create null-modem adapters or special configurations.



Hall-ComSecm Inc., 1024 Wakerobin Ln., Fort Collins, CO 80526; (303) 223-8039. $37.50

CIRCLE 338

Products mate PCs with PBXs

A family of hardware and software products, called the PC/PBX Connection, converts a personal computer into an integrated voice-data workstation. The user has on-screen access to more than 200 voice and data features of the AT&T System 75 and System 85 digital PBX systems, in addition to high-speed simultaneous voice-data communications at 64 kbits/s. The products work with a variety of computers operating under MS-DOS or Unix, including AT&T's PC 6300 and Unix PC 7300, as well as the IBM PC and most compatibles. A full-function arrangement consisting of PC expansion cards and software packages for MS-DOS or Unix costs $700 and will be available in mid-1986.

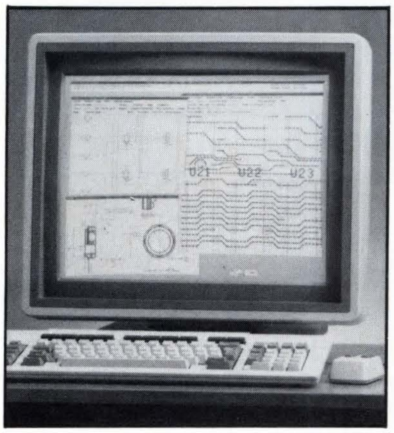
AT&T Information Systems Group, 100 Southgate Pkwy., Morristown, NJ 07960; (201) 898-8337. **CIRCLE 339**

NEW PRODUCTS

COMPUTERS & PERIPHERALS

ELECTRONIC DESIGN EXCLUSIVE

Pc board workstation runs DOS programs in window



A printed circuit board workstation based on a bit-slice architecture not only routes and simulates logic in a blaze, with an optional 80186 co-processor installed it can run popular PC-DOS software as a concurrent task. Just how fast does the 6085 Expert Designer work? The autorouter has been benchmarked at a little over 3 hours with a board containing 150 ICs (with 98% completion). A product of the Engineering Information Systems (EIS) Division of Xerox Corp., the workstation is to be shown for the first time at the Design Automation Conference in Las Vegas later this month.

The workstation displays PC-DOS applications in a window on its 15-in., 697- by 880-pixel screen (or on an optional 19-in. 925- by 1184-pixel screen).

The 2901-based 6085 is fully compatible with previous Xerox Star workstations, yet is about half the size—small enough to fit under a desk. It stands 21.5 in. high, 9.5 in. wide, and 12.5 in. deep. And it is also faster. Because it executes a 48-bit–wide instruction, it is between 15% and 20% quicker than previous Star systems, and it is smart to boot. Its computational power is on the same level as a 1-MIPS 68020-based workstation—about as good as it gets in this size machine.

The 6085's hardware includes a proprietary CPU running from an 8-MHz clock, up to 3.7 Mbytes of main memory (with a 23-bit virtual memory), an I/O subsystem controlled by another 80186, up to 80 Mbytes of 5¹/₄-in. hard disk storage, and an IBM compatible 5¹/₄-in. floppy disk. An additional insert card containing an 80186 with up to 640 kbytes of contiguous memory allows the 6085 to run the PC-DOS programs concurrently with Xerox design programs.

One program, the Expert Placement and Routing system, furnishes any combination of interactive and automatic placement and routing for boards with up to 16 layers. The available parts libraries include TTL, ECL, and CMOS logic, as well as popular microprocessors and peripheral chips. Outputs of the system include automatic drilling tapes, as well as traditional photoplots.

The entry-level workstation, with a 1.1-Mbyte main memory and a 20-Mbyte hard disk, costs approximately $7000. Delivery is from stock.

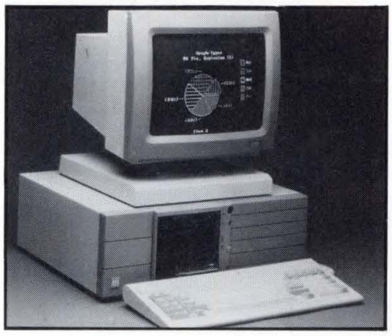
Xerox Corp., Engineering Information Systems, 2945 Oakmead Village Ct., Santa Clara, CA 95051; Janet Gilmore, (408) 982-8187. **CIRCLE 301**

Stephan Ohr

NEW PRODUCTS

COMPUTERS & PERIPHERALS

Supermicro runs DOS and Xenix



The newest member of the ITT XTRA family of computers, the XTRA XL runs under both DOS and Xenix operating systems. Based on an 8-MHz 80286 processor, the standard configuration includes 640 kbytes of RAM, a 1.2-Mbyte floppy-disk drive, a 40-Mbyte hard-disk drive, one serial and one parallel port, and a monochrome monitor and adapter.

ITT Information Systems, 2350 Qume Dr., San Jose, CA 95131; (408) 945-8950. From $5299.

CIRCLE 342

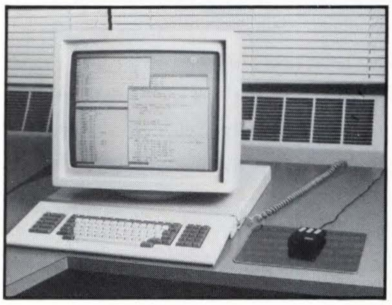
PICK-based VDT is AT-compatible

An IBM PC AT-compatible video display terminal is targeted to multiuser environments running under the PICK and Xenix operating systems. With a list price of $479, the ATerm is the first terminal priced under $500 that specifically addresses PC AT multiuser systems. It comes with a keyboard that is identical to that of the IBM machine, plus a 14-in. green or amber display. The ATerm emulates such popular terminals as the ADDS Viewpoint and Regent 25, as well as the Lear Siegler ADM3A.

Esprit Systems Inc., 100 Marcus Dr., Melville, NY 11747; (800) 645-4508 or (516) 293-5600.

CIRCLE 343

CADAT simulator transfers to ATE



A postprocessor converts circuits simulated with CADAT-5 into a form needed for the company's automatic board testers. The postprocessor runs on a VAX computer or Sun workstation and converts the simulator's circuit description, along with the input stimuli and nodal activity files, to an ATE format. Unusually, little extra editing is needed to debug and optimize the test program.

Factron Ltd., Ferndown Industrial Estate, Wimborne, Dorset BH21 7PP, England; (+44) 202 893535; Telex: 41436. **CIRCLE 344**

Small DPM has mV and resistance i/p

A linearizing digital panel meter measuring just 96 by 48 by 88 mm has millivolt and PT100 resistance inputs that connect to thermocouples or resistance thermometers. The DMM 500 offers ±12-bit resolution and operates from a 240- or 110-V supply. Resolution is a maximum of 1°C for temperatures of −50° to 1800°C. A separate unit allows five thermocouples to be switched into the meter; any number of these switch units can be connected.

CIL Electronics Ltd., Decoy Rd., Worthing, Sussex BN14 8ND, England; (+44) 903 204646; Telex: 87515 wisco g att cil. **CIRCLE 345**

ELECTRONIC DESIGN EXCLUSIVE

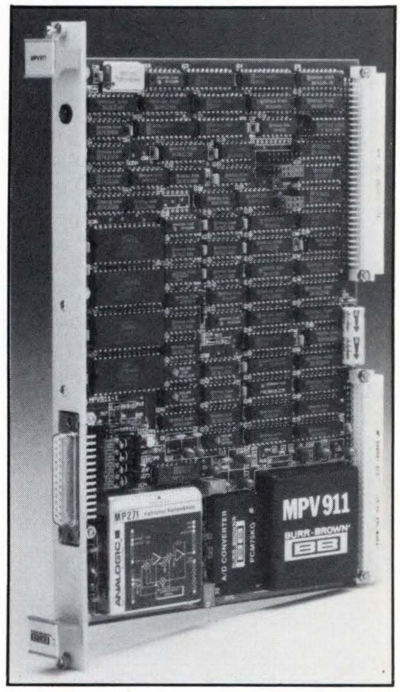
16-bit resolution spotlights VMEbus board

Sixteen kwords of on-board memory allow a 16-bit analog input board to transfer data across the VMEbus under DMA control of a host processor—the first 16-bit analog board to do so. Burr Brown's eight-channel MPV911 has a software programmable timer that samples an input signal at periods stretching from 1.43 ms down to 22.4 μs, the latter corresponding to a maximum sampling frequency of 44.6 kHz. The board suits instrumentation, high-resolution digital signal processing, process control, and robotics applications.

The weakest link in 16-bit systems is the sample-and-hold amplifier. The company achieves its high sampling rate using Analogic's MP271 hybrid sample-and-hold circuit. This device's 50-kHz bandwidth ensures the 44-kHz sampling rate called for in PCM telephony and digital audio equipment.

The board is fitted with eight multiplexed input channels. The crosstalk from the seven off-channels to the single on-channel is below −84 dB, which corresponds to an accuracy of 14 bits. A programmable-gain amplifier can boost the dynamic range to 96 dB, resulting in an accuracy of 16 bits. Each of the eight analog input channels is accurate to ±0.006% of full scale and is linear to within ±0.004%.

The sampled signals are fed into "swinging" buffers. One-half of the buffer, stores incoming data while the other half is being accessed across the VMEbus. There is no data loss while data is being transferred.



The double-height Eurocard has 16 data and 24 address lines, and the base address may be placed anywhere within a 16-Mbyte memory. Working between 0° and 60°C, the board draws 3.5 A from the 5-V line. It decodes seven vectored interrupt levels and uses the VMEbus' full range of address-modifier codes. A status register indicates when the input signal is oversampled.

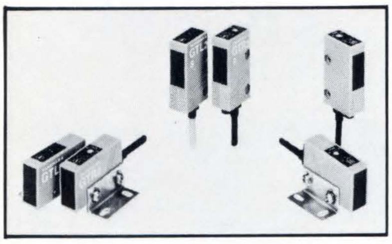
A driver for pSOS-68 is available now, and VERSAdos 4.4 and PDOS drivers are in development. Samples cost $2495.

Burr-Brown Corp., International Airport, Industrial Park, P.O. Box 11400, Tucson, AZ 85734; (602) 746-1111. **CIRCLE 306**

Burr-Brown Ltd., Simpson Pkwy., Kirkton Campus, Livingston EH54 7BG, Scotland; (+44) 506-414445. **CIRCLE 307**

Mitch Beedie

Ac or dc models for IR photoelectrics



The E series of photoelectric switches offers six infrared models, all in compact 16-by-60-by-75-mm polycarbonate cases. Three versions, the ET5D, ER03 and ER3MD operate from a 24-to-240-V ac or dc power supply. For their part, the ENT3, ENR03 and ENR3M require a 12-to-24-V dc supply.

Both the ET5D and ENT3 use separate transmitter and detector modules, while the ER03 and ENR03 are direct-reflection systems. The remaining two use a retroreflective detection scheme.

All units have a wide-angle detector lens that permits sensing of the IR signal from angles as high as 70° (from perpendicular), even in the presence of ambient light as high as 20,000 lux. The three ac/dc models provide a relay output capable of handling a 250 V ac, 2 A (max) noninductive load and have a response time of 25 ms (max). The dc-only units can sink up to 100 mA at 30 V. The dc only equipment responds in just 2 ns.

Takenaka Electronic Industrial Co. Ltd., 20-1 Narano-cho, Shinomiya, Yamashina-ku, Kyoto, Japan 607, (075) 581-7111, Fax (075) 501-6944.

CIRCLE 346

Single unit checks digital links

Evaluating the quality of digital links to CCITT G821, a digital transmission analyzer incorporates transmitter and receiver in a single case. The 7702 stores 10 standard measurements in ROM and another 10 sets of front-panel settings in nonvolatile memory. It can monitor lines for any period between 1 s and 365 days. The instrument extends jitter measurements right down to dc transmission rates and can detect errors and jitters on 2-, 8- and 34-Mbit/s links.

Solartron Instrumentation Group, Victoria Road, Farnborough, Hants, GU14 7PW, England; (+44) 252 544433; Telex: 858245 solfar g.

CIRCLE 347

SOFTWARE

Expert systems gain "delivery vehicle"

For the development of expert systems, Symbolics' 36xx series has long been the preferred hardware. But because of its price, some artificial intelligence companies passed it by for less expensive "delivery vehicles," thereby sacrificing performance. Realizing that, Symbolics has gone all out to cut costs. Using application-specific ICs and surface-mounted memory chips in the 3610AE cuts the chip count by half, the board count from 8 to 5 and—not content with these gains—shrinks the unit so that it fits under a desk.

Simultaneously, the company offers a new version of its Lisp software system, dubbed Release 7. It addresses the fact that the last 20% of an AI package—usually the user interface—often consumes 80% of the development time. More intelligent interactive interface drivers not only speed development, but give the user simpler man-machine communication. For example, the system not only validates all user entries but also suggests correct responses if the input appears incorrect or inappropriate.

At the output side, Release 7 automatically formats displays for any workstation's console and reformats its outputs automatically for all compatible printers and storage devices. Further, windows "remember" their contents, so that users can return to a screen without having to go through the cumbersome tasks necessary to retrace command sequences.

Furthermore, Release 7 implements continuous, hardware-assisted garbage collection without disrupting processing. Safeguards against accidental file access protect an expert system's integrity.

With a 19-inch console, 5.5 Mbytes of RAM (1 Mword), a 190-Mbyte disk, and Release 7, the 3610AE costs $39,600 in quantities of 10, and $31,500 in volume (76 or more). Delivery starts in October.

Symbolics Inc., 11 Cambridge Center, Cambridge, MA 02142; (617) 577-7500. **CIRCLE 312**

NEW PRODUCTS

COMPONENTS

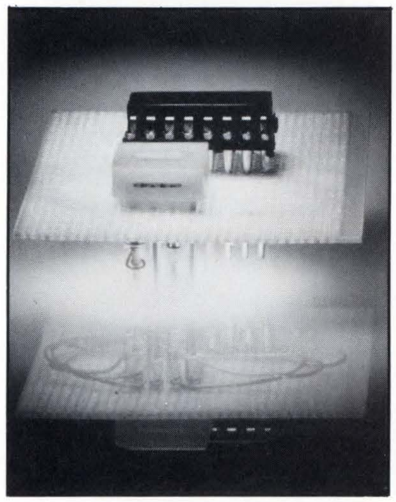
Small sockets seat small-outline ICs

Because they have the same effective dimensions as their corresponding small-outline ICs, Surface Mount Devices' SMIP line of sockets will save precious board space. The sockets come in 8-, 14-, 16-, 20-, 24-, and 28-pin prototype (staggered-pin), surface-mountable, and wire-wrap versions.

Each socket comes with a molded snap-on cover that prevents improper orientation and aligns the IC with the socket. The cover also ensures suitable ventilation for the chip and allows for in-circuit checks with test probes via pin holes. An optional high-impedance, 30% glass-filled thermoplastic cover that withstands up to 209°C is available. It is fire retardant and meets UL 94V-O standards.

All of the pins in the SMIP line are molded into the socket's base. The pins are made from beryllium copper and plated with both a 10- to 20-μin. layer of nickel and a 20- to 30-μin. layer of gold.

The sockets require a minimum contact force of 65 g, and all conform with all JEDEC standards for both the top and the bottom pin-contact surfaces.



The price for the prototype version, which has a staggered-pin arrangement on 50-mil centers and pin spacings of 100 mils, is $4 (in quantities of 1000). The surface-mountable version (standard 50-mil spacing) is $3, as are the wire-wrap models. Unit price breaks of 25¢ for all versions occur at 1–10 thousand, and again at 10–100 thousand units. Price breaks beyond 100,000 units are available on request. Delivery is from stock.

Surface Mount Devices Inc., P.O. Box 16818, Stamford, CT 06903. (203) 322-8290. **CIRCLE 310**

EL displays pack parallel interfaces

Two 4-by-8-in. ac thin-film electroluminescent displays include on-board parallel interfaces and related support electronics. The interfacing scheme includes 8 parallel data lines, 14 address lines, and 11 control lines, which are used for handshaking, dimming, fault monitoring, and display feature selection.

An on-board microprocessor provides a large variety of alphanumeric and graphics modes. Because the screen's pixel information resides in an on-board refresh buffer, text and graphics can be mixed. Standard 5-by-7 character blocks are used in 25 lines of 80 characters each. An optional 12-by-16 pixel block provides true descenders, superscripts, subscripts, and underscoring.

Industrial Electronic Engineers, Inc., 7740 Lemona Ave., Van Nuys, CA 91405; (818) 787-0311. **CIRCLE 348**

BEST IN-DEPTH ANALYSIS

The Jesse Neal Award is the "Pulitzer Prize" for journalism. This year, only 15 publications were recognized out of 730 entries. Among the world's largest magazines, Electronic Design was singled out for its 1985 Technology Forecast Report which predicted major change in the role of the design engineer.

This year's Neal Award acknowledges what loyal Electronic Design readers have known for years. Information of vital interest to electronics engineers is covered *first and best* in Electronic Design.

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Want to contact us? Address your correspondence to:

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PRODUCT NEWS

CMOS DMA controller works with 68000 μP

The **Semiconductor and IC Division** of **Hitachi America Ltd.** (**San Jose, CA**) has released a CMOS version of the company's HD68450, a 68000-microprocessor family DMA controller. Designated the HD63450, the device offers high-speed operation up to 12.5 MHz, complete compatibility with the NMOS HD68450, low power dissipation of 500 mW, and new multiple-block transfer commands. Plug-compatible with its 64-pin DIP predecessor, the HD63450 is also available in a 68-pin plastic leaded chip carrier. Sample quantities are available now with volume deliveries scheduled for the second quarter. Sample price is \$45 for the 12.5-MHz chip carrier version. **CIRCLE 349**

68000 microprocessor is MIL-qualified

Signetics Corp. (**Sunnyvale, CA**) announced the release of a military-qualified 68000 16-bit microprocessor. The company is listed as an approved source of supply on the Defense Electronics Supply Center (DESC) drawing for the 68000 microprocessor (No. 82021). The company is also pursuing a JAN qualification for the 68000. Devices are available in both 6- and 8-MHz versions, priced at \$346 and \$385, respectively, in lots of 100. Both versions are housed in 64-pin DIPs. A 68-pin leadless chip carrier will be forthcoming. **CIRCLE 350**

Op amp comes in surface-mount package

The industry-standard OP-07 precision operational amplifier may now be specified in an 8-lead surface-mount package, as well as the more common TO-99 and 8-lead plastic DIP and Cerdip. **Maxim Integrated Products** (**Sunnyvale, CA**) offers the OP-07 in five grades, specified for operation over two temperature ranges (0° to 70°C and −55° to +125°C). As with all Maxim standard products, the OP-07 is 100% burned-in at 150°C. **CIRCLE 351**

PLD meets MIL requirements

A military version of the GAL16V8 Generic Array Logic device is now available from **Lattice Semiconductor Corp.** (**Portland, OR**). This version of the erasable programmable logic device guarantees performance over the full military temperature range of −55° to +125°C and from 4.5 to 5.5 V. Of special interest to the military, GAL devices eliminate expensive field failures. Lattice guarantees 100% field programmability and 100% ac/dc functionality of its devices. The company will have 883C certification for the GAL16V8 by December. The cost of the array, housed in a ceramic package, is \$17.60 in lots of 1000 units. **CIRCLE 352**

PRODUCT NEWS

SOT-89 package locks out moisture

Rohm Corp. (Irvine, CA) is making available a series of transistors in a special SOT-89 package which incorporates a lock-in mechanism for the power tab to prevent separation from the plastic base. This internal design and construction of the surface-mounted package prevents the incursion of moisture between the two surfaces, the most common source of unreliability with SOT-89 packages. Sixteen parts are initially available for the U.S. market, ranging from 30 to 80 V, 500 mA to 2 A, and include RXT, 2SD, and 2SB part numbers. Pricing in 10,000-unit lots is $0.14 to $0.16. Delivery takes four to six weeks. **CIRCLE 353**

Redesigned ADCs cost less

Just about everything but the model numbers have been changed on a trio of 16-bit hybrid analog-to-digital converters from **Burr-Brown Corp. (Tucson, AZ)**. The ADC71, ADC76, and PCM75 have all been redesigned with appoximately 50% fewer active and passive chips for greater reliability. JG and KG versions of the ADC71 also have new bottom-brazed ceramic packages. Since the new designs cost less to manufacture, users realize price reductions of 30% to 40%, depending on model and quantity ordered. All converters remain pin-compatible with their earlier industry-standard versions. Prices start at $63 (ADC71), $99 (ADC76) and $87 (PCM75). Small quantities are available from stock. **CIRCLE 354**

4-bit MPU slice cuts power by 75%

A high-speed 4-bit microprocessor slice from **Advanced Micro Devices Inc. (Sunnyvale, CA),** the Am29C01, offers the low-power advantages of CMOS and is a plug-in replacement for AMD's industry-standard Am2901 bit-slice microprocessor. The Am29C01 reduces the full-speed power consumption to 0.4 W, a 75% reduction over the equivalent bipolar device. The part is now in production in a 40-pin ceramic DIP, with plastic DIPs to follow. **CIRCLE 355**

681 DIP functions meet MIL-STD-883C

More than 600 integrated circuit functions offered by the military products department of **Texas Instruments Inc.'s Semiconductor Group (Dallas, TX)** comply fully with the requirements of MIL-STD-883, Revision C, paragraph 1.2.1. The 681 functions represent virtually all of the company's military IC family and include dual-in-line versions of bipolar and CMOS logic, bipolar memory, linear, interface, digital signal processing, and programmable array logic devices. The availablility of fully compliant products packaged in flat packs and leadless chip carriers is scheduled later in the first quarter. **CIRCLE 356**

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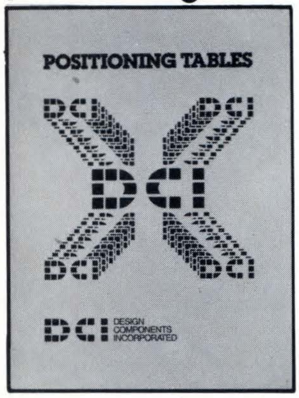
Selecting positioning tables



A 20-page catalog provides engineering selection and application data on single, dual, and rotary type positioning tables available in both precision and commercial grades. Topics include accuracy, ball vs cross-roller bearings, load capacity, length of travel, multiple axes, and life expectancy. The catalog includes mechanical drawings and dimensional details that will assist the designer when selecting and specifying tables for a particular application.

Design Components Inc., 1 Kenwood Cir., Franklin, MA 02038; (617) 528-7300. **CIRCLE 357**

Connector selection guide

A comprehensive 596-page design guide and product catalog (No. C-100) gives detailed specification and ordering information for TRW's entire line of connectors. The application-oriented guide provides basic data on all standard connector types, including grid densities, tail configurations, and application advantages and disadvantages. The product presentation is designed around a 16-page connector selection guide. Application categories include board to board, board to flexible circuit, board to discrete cable, board to component, and cable to cable.

TRW Electronic Components Group, Connector Division, 1501 Morse Ave., Elk Grove Village, IL 60007; (312) 981-6000. **CIRCLE 358**

Digital storage oscilloscopes

The applications and purchase considerations of digital storage oscilloscopes are reviewed in a 12-page pamphlet. The document also compares the the digital scope to tube storage oscilloscopes and describes the former's advantages, such as computer interfacing, signal processing, plotter outputs, and pretrigger viewing.

Gould Inc., Recording Systems Division, 3631 Perkins Ave., Cleveland, OH 44114; (216) 361-3315. **CIRCLE 359**

CAD/CAM analysis

The Society of Manufacturing Engineers is offering its most recent book, *New Directions Through CAD/CAM*. It provides information on numerous aspects of CAD/CAM, including the latest technological developments, discussions of CAD/CAM management and justification, system applications. A portion of the inclusive text even offers suggestions for the future. The 230-page hard-cover volume is written for all levels of manufacturing personnel—from technologist to engineer to corporate executive.

Society of Manufacturing Engineers, Marketing Division, 1 SME Dr., P.O. Box 930, Dearborn, MI 48121; (313) 271-1500, ext. 418 or 419. $37 ($32 for SME members). **CIRCLE 360**

Digital/rf article reprints

A volume of nine technical articles is of interest to all who work with digitally controlled rf components. The first seven articles serve as a cohesive primer on the art of digitally controlling rf components, a discipline that spans the disparate worlds of rf and digital. The two remaining articles are tutorial in nature and provide useful insight into two technical areas (switch-matrix designs and phase shift) that are not fully understood by all.

Lorch Electronics Corp., 105 Cedar La., Englewood, NJ 07631; (201) 569-8282. **CIRCLE 361**

Test instruments

A 350-page catalog provides detailed specifications and illustrations of Marconi's complete line of test instrumentation. A tutorial section procedes each major instrument category and includes application information, selection charts, measuring techniques, etc. Technical publications and application notes available from Marconi are also described in a separate section.

Marconi Instruments, 3 Pearl Ct., Allendale, NJ 07401; (201) 934-9050. **CIRCLE 362**

NEW LITERATURE

Europackaging systems

A four-color brochure includes technical specifications and product features, outline drawings, dimensions, and photographs of Vector's extensive line of Europackaging systems. Five bulletins cover VMEbus backplanes and extenders; Euro subracks and dividers; Eurocard prototyping boards (VMEbus and Multibus II); and custom subracks, backplanes, and piece parts.

Vector Electronic Co., 12460 Gladstone Ave., P.O. Box 4336, Sylmar, CA 91342; (818) 365-9661. **CIRCLE 362**

Enclosures and cases

Hudson Tool & Die announces the availability of its catalog of enclosures, stampings, and assemblies. The 66-page document showcases a complete line of deep-drawn metal enclosures and covers, offered in a variety of shapes and materials. Also featured are military cases and a series of crystal and miniature relay housings. A metric conversion table and a chart of standard modifications are included.

Hudson Tool & Die Co., 18 Malvern St., Newark, NJ 07105; (201) 589-1800. **CIRCLE 363**

Fiber-optic transmission

The Fiberlink product group of Math Associates offers an 84-page catalog describing a comprehensive line of fiber-optic transmission systems. Analog, digital, audio, video, and RS-232 systems are covered, as well as special-purpose systems, fiber-optic test equipment, fiber-optic cable, terminating sets, and the company's installation capabilities. Also presented are all of the accessories necessary to install, service, and maintain a complete fiber-optic system.

Math Associates Inc., 2200 Shames Dr., Westbury, NY 11590; (516) 334-6800. **CIRCLE 364**

Push-button switches

Push-button switch configurations are detailed in a 19-page brochure. Specifications are given on the popular lines distributed by ECG, including reliable, miniature, modular, watertight, and economical types. Pricing information and samples are free on request.

Electronic Components Groupe, 26 N. 5th St., Minneapolis, MN 55441; (612) 559-0720. **CIRCLE 365**

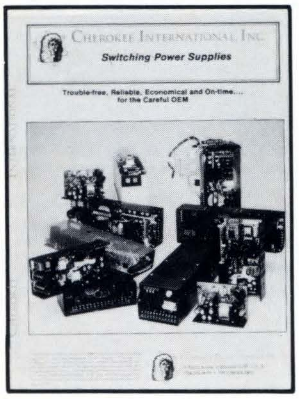
Watertight instrument cases

A 32-page catalog describes a line of portable instrument cases constructed with a special seal to ensure a watertight closure. Information is provided to ease the selection process, along with a chart of standard modifications.

TA Instrument Case Co., 4625 Alger St., Los Angeles, CA 90039; (818) 242-8855. **CIRCLE 366**

NEW LITERATURE

Switching power supplies



Switching regulated power supplies are the subject of a six-page short-form catalog. A product selection guide provides electrical and mechanical specifications, voltage ranges, output combinations, and ratings for all of Cherokee's products. Supplies range from single-output 50/60-W models to five-output 500-W switchers.

Cherokee International Inc., 8 Autry, Irvine, CA 92714; (714) 951-9679.

CIRCLE 421

CAM hardware directory

The *International Computer-Aided Manufacturing Directory* provides a detailed, specification-oriented description of all types of hardware for CAM applications. Selected contents include CAM and CAT systems; flexible manufacturing systems; material management systems; mainframe, mini, and microcomputers; memory devices; interfacing devices and data converters; workstations and terminals; factory networks; CNC equipment; and printers.

Technical DataBase Corp., P.O. Box 720, Conroe, TX 77305; (713) 439-1687. $40; update service is an additional $25.

CIRCLE 422

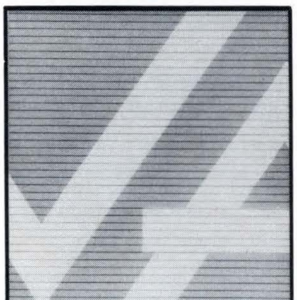
Light-emitting diodes

Entitled *An LED Universe*, this 48-page catalog gives product specifications for both panel- and board-mounted LEDs, as well as a large variety of devices that mount in standard sockets as incandescent replacements. LED types covered within include discrete wide viewing angle, snap-in, multichip illuminators, industrial lamps, LED arrays, and tricolor and bicolor lamps. Also detailed are sockets and other mounting hardware.

Data Display Products, 301 Coral Cir., El Segundo, CA 90245; (800) 421-6815 or (213) 640-0442.

CIRCLE 423

Test and measurement



Wavetek is offering its 1986 test and measurement instrumentation catalog containing descriptions, specifications, prices, and ordering information. Indexes and charts are included in the 176-page publication to aid in readily finding specific instruments and features. Product categories include low-frequency and rf test equipment, broadband cable communication test equipment, rf and microwave components, microwave test equipment, instrumentation computers, and more.

Wavetek Corp., 9191 Towne Centre Dr., Suite 450, San Diego, CA 92122; (619) 450-9971.

CIRCLE 424

Fiber-optic RS-232-C kit

A four-page color brochure describes a ready-to-install RS-232-C fiber-optic communication kit. It provides simple, clear, illustrated installation procedures, as well as specifications and a parts list. The kit itself contains two asynchronous modems and power sources, plus 100 ft of twin fiber-optic cable with assembled connectors.

Augat Fiberoptics, 710 Narragansett Park Dr., Pawtucket, RI 02861; (401) 724-4400.

CIRCLE 425

Adhesives and encapsulants

A selector guide details a line of high-purity die-attach adhesives, surface-mount adhesives, electronic coatings and encapsulants, and wafer sorting inks. New products and information updates on standard products are provided in grid format showing extensive physical and chemical data, as well as suggested applications.

Furane Products Co., 5121 San Fernando Rd. W., Los Angeles, CA 90039; (818) 247-6210.

CIRCLE 426

BY CAROLE PATTON

Engineer vs boss: Still a slugfest over priorities, ethics

An historic clash is under way between engineering and corporate mindsets. At issue are two Morton Thiokol engineers who told a White House panel that they had urged a delay of the Jan. 28 Challenger launch because of cold weather. They were overruled by their own management. At a later hearing, both said they had since been reassigned—as punishment for letting the cat out of the bag.

Thiokol's chief executive officer, Charles S. Locke, denies that the engineers were punished. True, both were reassigned, yet neither engineer has taken a pay cut or been demoted, he says.

But the veneer of fair play is paper thin. Already Locke has shown his displeasure with the whole controversy. According to the *Wall Street Journal* (May 15, p. 5), Locke maintains that the two engineers have traveled "all over the country at our expense to appear before commissions." Locke adds that Thiokol, which made Challenger's solid-fuel booster rockets, has been "very open and above board" about the problem, but once the commission report appears, the engineers' situation would change. "People are paid to do productive work for our company," Locke says, "not to wander around the country gossiping."

Though he is sorry that the two engineers are unhappy, "our concern is for the best interests of our nation's space effort," he points out. Voicing concern for Thiokol's best interests, Locke made it plain that he didn't think NASA should bring in a second supplier for the rockets.

Underlying his comments is the corporate ethic. It perpetuates itself by selling a product and turning a dollar—a worthy pursuit in a nation whose economic keystone is capitalism and whose folk hero is Horatio Alger. Most employees readily adapt to this scenario, contribute to corporate growth, and ultimately retire with the corporation's thanks and a gold watch. But engineers often see things differently.

QUALITY OVER LOYALTY

In fact, engineers take pride in optimal—not just adequate—design. When life-threatening risks are taken merely to save a few dollars or to ship something on time, the resulting anger and frustration can tear even the most tightly woven corporate fabric. The Morton Thiokol case is only one example. A few years ago, the rabble-rousers were Westinghouse engineers working on a San Francisco transit system. Like the Thiokol engineers, they made their safety concerns public and embarrassed their employer.

The rules that engineers follow are best illustrated in a recent *Wall Street Journal* article (May 13, p. 1) on "ditch day" at the California Institute of Technology. A Cal Tech tradition, ditch day pits the technological prowess of engineering seniors against underclassmen, the "wimps." The idea is to keep the wimps from invading the senior's dormitory rooms. But keeping wimps out involves exotic technical challenges, such as locks that can be opened only by heat, lasers, sound, or sometimes by outsmarting a computer programmed for speech (like Hal in *2001*). The seniors even leave clues on how to break in.

Other locks are purely cerebral: One senior left his room unlocked, but with a physics problem taped to the door. No one could open the door because no wimp could solve the equation. (In fact, even a Nobel-laureate faculty member was unable to solve it.) Some seniors say they spend years creating unbreachable fortifications.

Beneath this tomfoolery lies an insight into the type of systems that engineers are comfortable with. Its rules specify a knowable universe—as unchanging as the correct answer to a physics equation. Here, scientific laws don't bend for love or money, and the challenge is found in outwitting others by applying the same rules but more deftly.

SHRINKING THE UNIVERSE

Rules and theorems or the latest corporate philosophies aim at reducing many possibilities to a thimbleful of manageable choices. Though systems create narrow worlds that the human mind can deal with, they also can turn engineers pursuing an elegant design or managers protecting corporate welfare into well-mannered carriage horses, their judgment impaired by self-imposed blinders. The real challenge lies in knowing when to scrap the system's rules and take in the landscape's broader brush. As Douglas Hofstadter points out in his book *Godel, Escher, Bach,* systems exist everywhere. The more civilized we become, the more systems we erect. Some of the worst snarls arise, Hofstadter says, when systems turn back on themselves—for example, when government investigates its own wrongdoing.

For my part, I distrust systems. They are small-minded, self-perpetuating, and constantly watchful of their own safety. But systems and their supporting structures must ultimately bow to universal truths. The truth here is simple—no system is worth more than human life.

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A BSEE or Physics degree and 2-4 years of experience is required. You'll be responsible for characterization, specification, and qualification of devices in high reliability applications including Class (B) and Space Grade Class (S) parts.

Design Engineers
We ask that you have a BSEE and 1-3 years experience in the design of advanced high-speed logic. Specific tasks will pertain to the design and simulation of circuits, design/layout verification, and generation of test specification. Knowledge of ECAD software and MENTOR GRAPHICS/APOLLO workstations is desirable.

Test Engineers
You'll design and develop software and hardware for the testing of integrated circuits and develop test specifications utilizing Sentry 7, 20 or 21 systems. A BSEE and 3 or more years experience is required.

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Electronic Design

Openings in these areas range from two to 15 year's experience in analog or digital design. Some experience with monochrome and/or color CRT systems, including display processor or a closely-related field, is also preferred. Customer interface and proposal experience is also desired. Other openings include: High-speed Digital Processing, Analog-to-Digital Converters, and Raster/Stroke CRT Circuitry Design.

Helicopter Avionics

Avionics System Engineer

In this position you should have a BSEE with three or more year's experience on military avionics programs. You should also have experience with designs using Mil-Std-1553 interface and the associated software/hardware background design requirements. Experience in working with the man-machine interface and familiarity with structured analysis/design methodologies is desired.

Software Engineer

To qualify you should have a BSEE or BSCS and two or more years of real time software experience using Assembly and/or High Order Languages, for embedded processor applications, or computer graphics. Experience/exposure to Ada programming and/or environment is highly desirable. Familiarity with Structured Analysis and Structured Design methodologies is also desired.

Flight Control Systems

Flight Controls Engineer

These positions require a BSEE degree and two or more year's experience associated with the design of microprocessor-based systems including I/O, data transmission, bus architecture, signal conversion and analog/digital circuit design. Applications include: Flight management development, wide band analog and high speed digital circuit design, flight control system development, software development and simulation/algorithm development.

Tactical and Reference Systems

Product Engineer

To qualify for this position you will need a BSEE degree with a minimum of two year's experience. In this position you will be working in support of momentum programs associated with digital and/or analog military avionics. You will be responsible for solving engineering design problems on the production line and for coordinating customer required changes into production hardware. Some direct customer interface also included.

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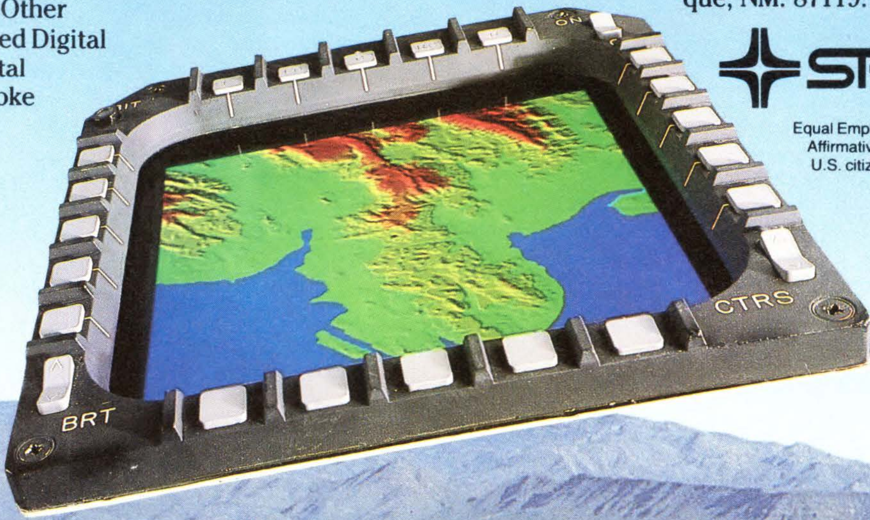

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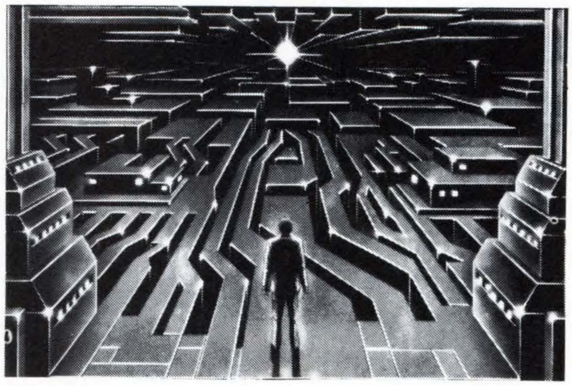

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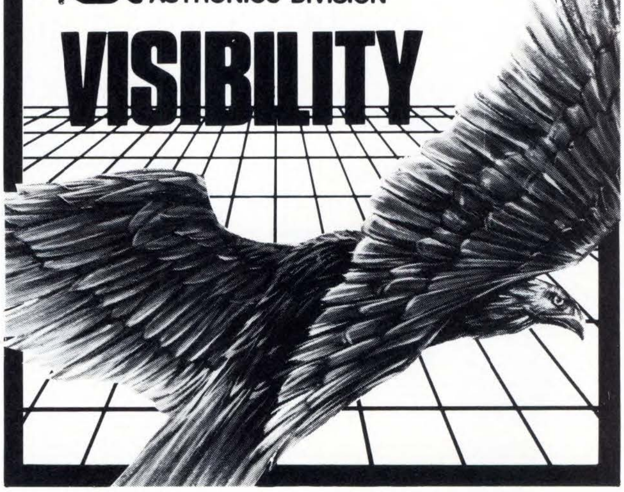

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HARDWARE ENGINEER BSEE or CE combined with 2+ years of microprocessor applications design experience.

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COMPONENT/RELIABILITY ENGINEER BSEE or equivalent plus 2-3 years experience as a component or reliability engineer. Thorough knowledge of microprocessors also required.

CONTINUING ENGINEER BSEE or CE with 5+ years of microprocessor applications design experience.

SYSTEMS ENGINEER BSEE or CS plus 2+ years experience in design, systems, product evaluation or test engineering.

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Circulation by Industry

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Computers	12,295
Computer peripheral equipment	9,548
Systems integration	6,427
Office and business machines	3,007
Communications Systems and equipment	22,480
Total:	**53,757**
Military and Test	
Navigation and guidance systems and equipment	6,249
Aircraft, missiles, space, and ground support	15,037
Oceanography and support equipment	708
Test, measurement, and instrumentation	11,846
Government and military	10,104
Total:	**43,944**
Industrial Controls, Research, and Medical	
Industrial control systems, equipment, and robotics	15,354
Independent research and testing	2,616
Medical electronics	4,404
Total:	**23,374**
Components, Consumer, and Other	
Components and subassemblies	5,542
Consumer electronics	3,713
Other OEMs	4,597
Users of electronic equipment	1,255
Total:	**15,107**
Total qualified circulation:	**136,182**

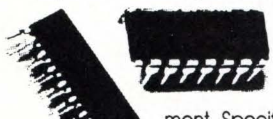
Leadership through Innovation

In the field of advanced microprocessor-based avionic systems for our nation's premier defense aircraft, Lear Siegler technology has earned industry-wide respect for innovation and mission-proven performance. With Weapons Control Systems setting new standards of reliability on-board the Harrier AV-8B and F/A-18 Hornet, we are now embarking upon our next decade of technological challenges.

With major, long-term Full Scale Engineering Development Programs to retrofit Weapons Control Systems for the F-14D Tomcat and A-6E Intruder Upgrade now underway, we are currently seeking seasoned professionals in the following categories at our campus-like facility in the rolling hills of Northern New Jersey.

COMPONENT ENGINEERS
Intermediate & Senior Levels
Failure Analysis

You'll perform detailed failure analysis on electronic components (diodes, resistors, capacitors, relays, filters, analog and digital microelectronics) for microprocessor-based Weapon Control Systems, and report the results to project management. Specific duties will include designing special test fixtures to accomplish trouble shooting of components, developing reliability test plans to demonstrate reliability requirements and providing specific design recommendations to improve component quality and reliability.



We require a BSEE and 3+ years reliability engineering experience with emphasis on component failure analysis. Previous exposure to a military electronics environment and hands-on experience operating a Scanning Electron Microscope is highly desirable.

SR. ELECTRONIC COMPONENT ENGINEERS

You'll assume responsibility for reviewing designs on assigned projects to ensure compliance with military and company standards. Since your specific duties will include the preparation of Specification Control Drawings (SCD), parts screening and the preparation of data items, a thorough knowledge of a wide range of available components, as well as non-standard parts application procedures is mandatory.

Your qualifications should include a BSEE or the equivalent and 5+ years' experience working with MIL-Standards (i.e., 38510, 19500, 883C). Similar experience in commercial design companies will also be considered.

SYSTEMS ENGINEERS

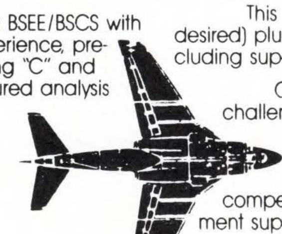
You'll assume responsibility for overall systems architecture and details for systems changes, weapon interface and hardware/software integration. This will require reviewing the preparation of systems design and test specifications, preparing systems specifications for Built-In Test, and testing systems and major software functions. You will also be involved in customer interface, technical reviews of software designs, and coordinating and reviewing solutions for systems integration and flight test problems.

We require a BSEE (MBEE preferred) and at least 5 years' experience in airborne military electronic systems (i.e., stores management or digital/analog systems).

SOFTWARE ENGINEERS
Real Time Design

You'll assume responsibility for the design, implementation and integration of software for avionic Weapon Control Systems in conformance with DOD-STD 1679A.

These positions require a BSEE/BSCS with 4-7+ years' software design experience, preferably 80986/80286 systems using "C" and Assembly. Experience with structured analysis and design a plus. "Hands-on" knowledge of operating systems, VAX and previous experience in an avionics environment would constitute a positive asset.



Software Test:

Your primary responsibilities will include the design and implementation of Test software for avionic Weapon Control Systems in conformance with DOD-STD 1679A.

These positions require a BSEE/BSCS and 4-7 years' experience in either testing of real-time software, or the development of Test-Set operational and simulation software. Previous experience with MIL-STD's, and knowledge of hardware a plus. "Hands-on" experience with 80986/80286, RMX operating systems, "C", PLM-86 and Assembly language would be highly desirable.

ANALOG SECTION HEAD

You'll manage the engineering activities of the Analog Design Section. Your responsibilities will include interfacing with senior management and providing technical direction for conformance to sound engineering techniques in analog design and analysis. Specific duties require managing supervisory, design and analytical personnel combined with varying levels of administrative personnel.

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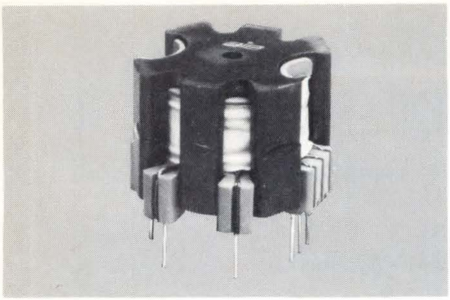

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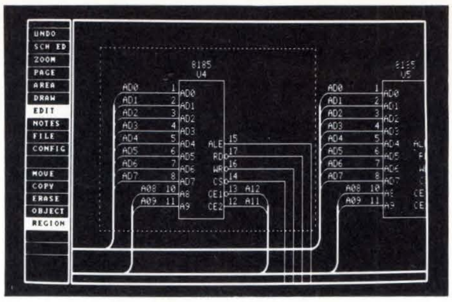

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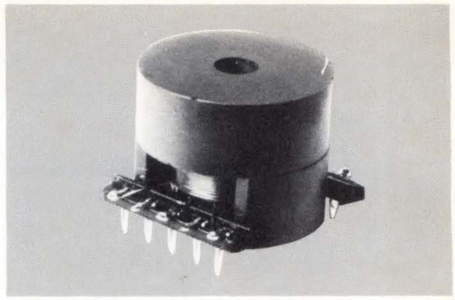

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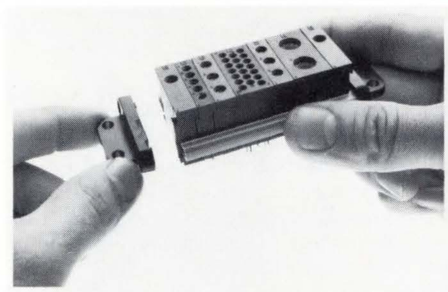

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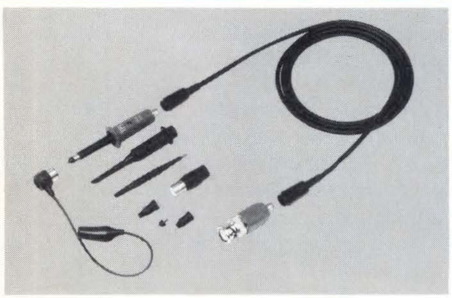

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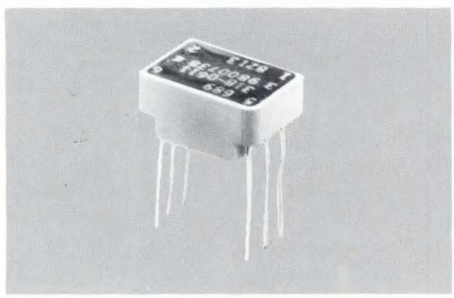

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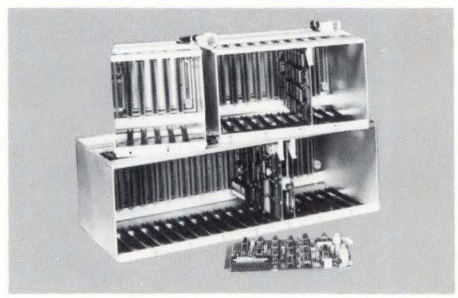

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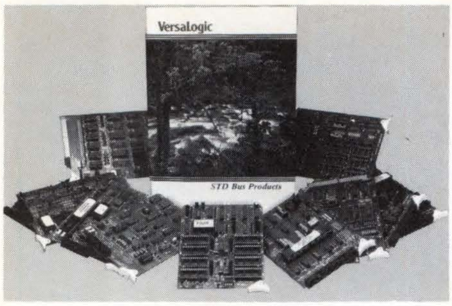

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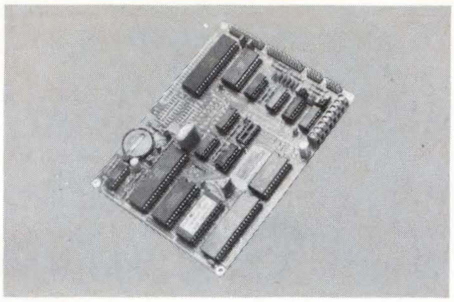

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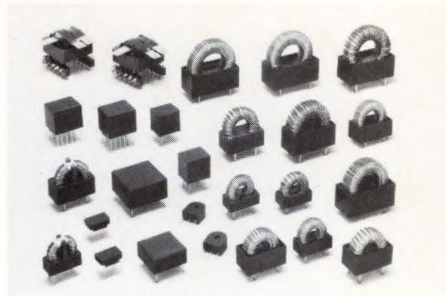

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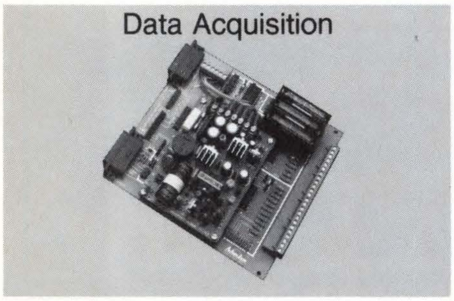

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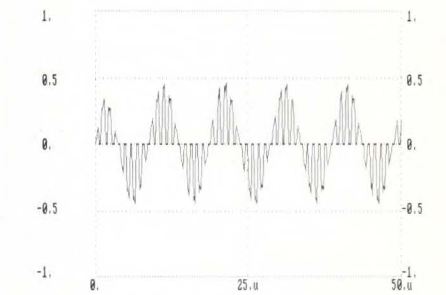

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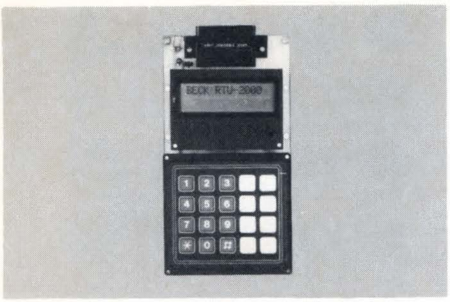

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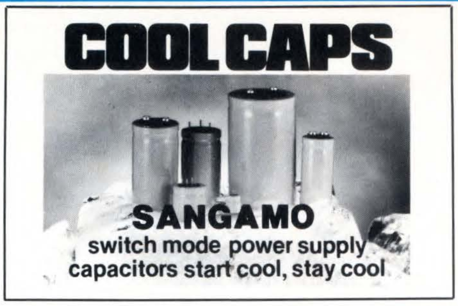

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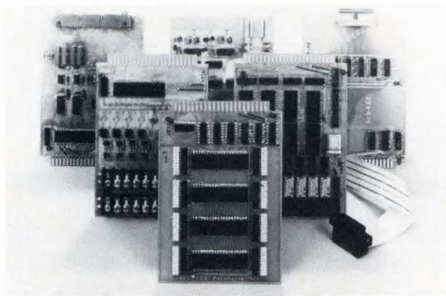

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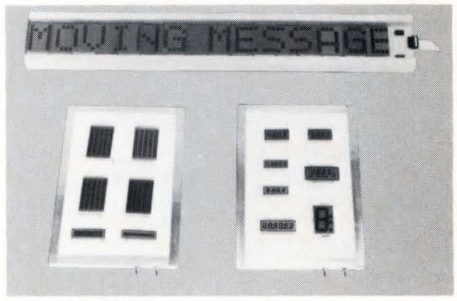

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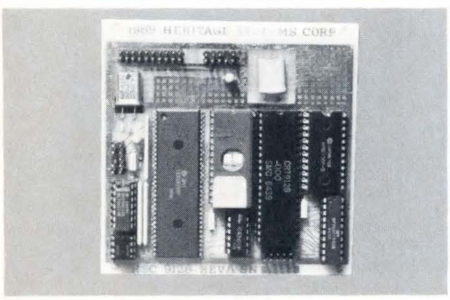

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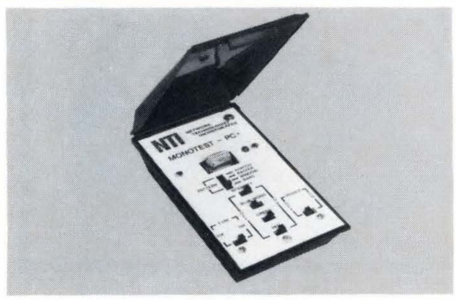

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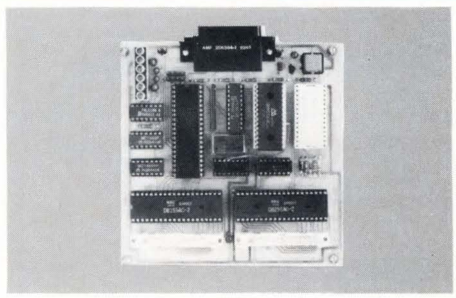

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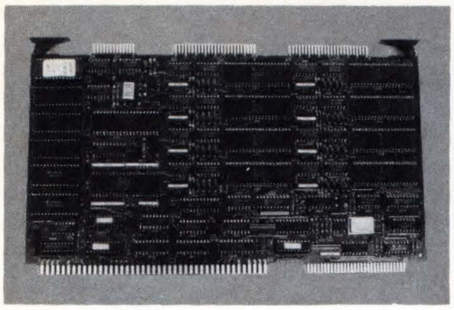

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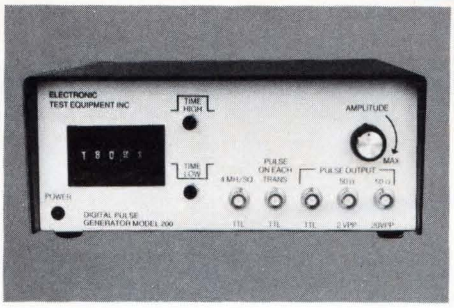

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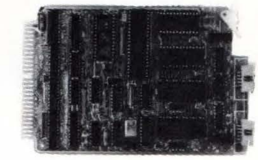

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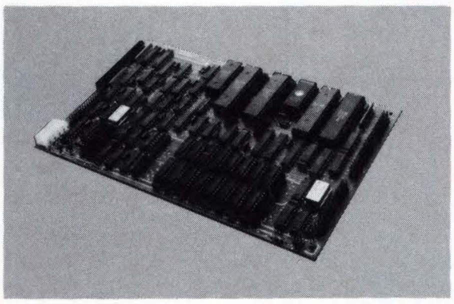

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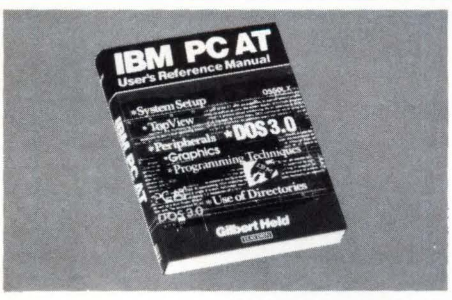

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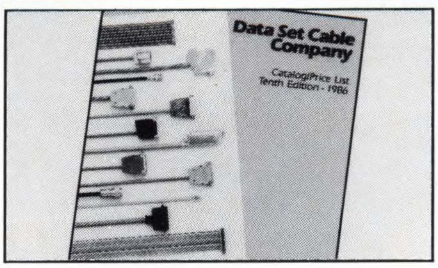

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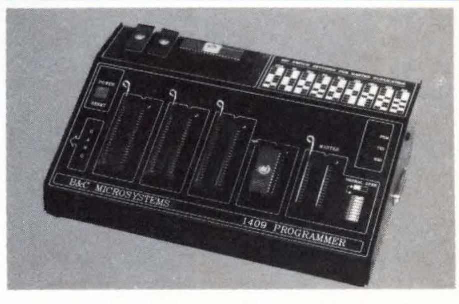

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