

Mini and microcomputers have become lookalikes that make the distinction often meaningless. Whether you need a computer on a chip, on a board, or in a box, the many choices can be confusing. But if you ask the right questions, you can find the best values ever for your money. For help, GOTO 24.



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International Marketing Offices: European Headquarters — Switzerland 042/23 22 42 • Belgium 02/218 2005 • France 01/2039633 • Germany 0711/24 29 36 • Italy 02/32 56 88 • Netherlands 70/87 44 00 • United Kingdom 01/572 6531 • Norway 2/71 18 72 • Sweden 764/20 110 • Japan 075/921 9111 • Australia 02/55-0411 03/95-9566 • Israel 77 71 15/6/7 For Immediate Application — Circle 130 or for Future Application — Circle 230 When we surveyed the pulse generator market, we discovered that what many of you wanted was unavailable: a Wavetek pulse generator.

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We could go on about the fixed ECL, TTL, and ECL outputs, and the variable outputs up to plus and minus 20 volts. Or the adjustable rise/fall from less than 5 nanoseconds. But this is an ad, not a data sheet. So why not circle our reader service number and get all the specs on Wavetek's first pulse generator. WAVETEK, 9045 Balboa Avenue, P.O. Box 651, San Diego, CA 92112. Telephone: (714) 279-2200, TWX 910-335-2007.



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160 160

Advanced Micro Devices' new Am2903. It's a four-bit CPU slice with sixteen internal working registers, two address architecture, multi-function arithmetic logic unit and shifting logic.

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YOUT

THE AM 2903 ARCHITECTURE

Am 2901

AND NOW,

THE

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LEFT RIGHT PARALLE

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ELECTRONIC DESIGN 2, January 18, 1978

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Across the desk

Can't save money without losing money

Your article on calculators for the blind (ED No. 20, Sept. 27, 1977, p. 32) was the most thorough we've seen. But we do take exception to the implication that technological wizardry can significantly reduce costs. For example, you stated, "Incorporating microprocessors into these systems promises to substantially reduce costs—but in future designs."

Our SPEECH+ calculator contains two one-chip microprocessors, a TI TSM-1000 and a custom microcontroller. Keeping costs low was a major design goal. The speech synthesizer itself consists of but two integrated circuits: the microcontroller and a 16-k ROM, so it is no more complicated than the \$100 architecture proposed in your article.

The cost problem is economic, not technical. The one-to-two-order-ofmagnitude price difference between calculators for the blind and the sighted is small compared to the ratio of market sizes. The \$10 pocket calculator is only possible with mass production for a market of tens of millions. With a market in the low thousands as we have, such economy of scale is not possible. Development and tooling costs must be recovered over a relatively small number of units, distribution costs are proportionally higher, parts buys are small, and manufacturing costs are relatively high. We know of no way to circumvent these iron laws of economics short of losing money.

Also, the dedicated microcontroller in our speech synthesizer is manufactured by Silicon Systems, Inc., Santa Ana, CA, not Texas Instruments. We would also like to point out that the SPEECH+ speech-synthesis technology was licensed from Prof. Forrest Mozer of Berkeley, CA. J.S. Brugler, Ph.D. Vice President Engineering Robert E. Savoie, Ph.D. Research Scientist Telesensory Systems, Inc. 3408 Hillview Ave. P.O. Box 10099 Palo Alto, CA 94304

Misplaced credit

Jim McDermott's article on talking and Braille calculators (ED No. 20, Sept. 27, 1977, p. 80) contains a minor error that is "major" to me. In describing the Speech Plus calculator he explains that "the synthesizer uses two custom LSI circuits, one of which is a 16-k MOS ROM. The other is a dedicated Texas Instruments' microcontroller. .."

The dedicated microcontroller used for speech synthesis was developed and is produced by Silicon Systems Incorporated of Irvine, California, not by TI.

> Jim Meyer Director of Marketing

Silicon Systems Inc. 16692 Hale Ave. Irvine, CA 92714

A few stages less

Your News Scope article, "BBD Time Delay Sets Record at 4096 Stages" (ED No. 18, Sept. 1, 1977, p. 20), has two inaccuracies. According to the "IEEE Standards for Charge Transfer Devices," P-582, a stage of a BBD encompasses the whole portion covering a bit or element of charge. So over-all delay is the product of the number of stages (continued on page 152)

Electronic Design welcomes the opinions of its readers on the issues raised in the magazine's editorial columns. Address letters to Managing Editor, Electronic Design, 50 Essex St., Rochelle Park, NJ 07662. Try to keep letters under 200 words. Letters must be signed. Names will be withheld upon request.





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n <u>8273 SDLC/HDLC Protocol Controller</u>. For SDLC and HDLC communications. <u>8275 Programmable CRT Controller</u>. Provides fully buffered interface and control of almost any raster scan CRT display.

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computer peripheral are talking about.

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MOTOR

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OP-09/OP-11 Features

	TYP.	MIN./MAX.
• Low Vos	0.30 mV	0.5 mV MAX.
Low offset current	8.0 nA	20 nA MAX.
• Low supply current (Total for all 4)	3.5 mA	6 mA MAX.
Voltage gain	250K	100K MIN.
Slew rate	1.0 V/µS	0.7 V/µS MIN.

· Matched positive and negative slew rate for low distortion.

2.0 MHz MIN.

We make them match.

Bandwidth

Another important advantage: we guarantee that all four op amps will match in terms of V_{OS} and CMRR. Here's how we specify them:

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			P-09A			P-09B		
Parameter	Symbol	Min	Тур	Max	Min	Тур	Max	Units
Input Offset Voltage Match	ΔV_{0S}	-	0.5	0.75	-	0.8	2.0	mV
Common Mode Rejection	ACMRR	-	1.0	20	-	1.0	20	$\mu V/V$
Ratio Match	J. C. C. C.	94	120	-	94	120	-	dB

(Match exists between all four amplifiers)



These matching dc characteristics should interest you. They reduce distortion, improve system performance, and simplify your design. But that's not all.

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And, you can enter your tolerances

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excellence. Priced at \$6,995*, you save dollars but don't sacrifice accuracy or overall performance.

For perfection in automated calibration, you'll want the 5101A with its *mini-tape cassette reader*, a unique new feature that allows you to store up to 58 calibration settings, including limits and tolerances. Only \$8,995*.

Both models have a friendly calculator-type keyboard. And, both have the RS232 or IEEE 488 system options you want for remote operation or hard-copy printouts of results.

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CIRCLE NUMBER 270

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The regulator consists of a monolithic chip driving a discrete series pass element and shortcircuit detection transistors. And that's not all. Our µA79HG needs no electrical insulator because its case is isolated.

CHARACTERISTIC	CONDITION	MIN	TYP	MAX	UNITS
Input Voltage Range		-40		-7.0	V
Nominal Output Voltage Range	$V_{IN} = V_{OUT} - 5V$	-24		-2.23	V
Line Regulation	$V_{IN} = -7 V \text{ to } -40 V$		0.4	1.0	% (VOUT)
Load Regulation	$V_{IN} = V_{OUT} - 10 V, I_{OUT} = -10 mA \text{ to } -5 A$		0.7	1.0	% (Vout)
Control Pin Current		19.6		3.0	μA
Quiescent Current	$V_{IN} = -10V$	23	3.513	5.0	mA
Ripple Rejection	$V_{IN} = -8.5 V \text{ to} -18 V$ $V_{OUT} = -5 V, f = 120 \text{ Hz}$	50			dB
Output Noise Voltage	10 Hz ≤ f ≤ 100 kHz, VOUT =-5V		200		μV
Dropout Voltage	$I_{OUT} = -5 A$		2.0	Vines	V
Peak Output Current	$V_{IN} = -10V$		8	No.	A
Control Pin Voltage (Reference)	$V_{IN} = -10 V$	-2.35		-2.11	V

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The SGS-ATES range of silicon PNP devices for VHF/UHF offers the following specific advantages over well-established equivalent germanium types:

very low noise figure

higher linearity with low cross modulation distortion

higher power dissipation and maximum junction temperature

higher stability and reliability even under extreme environmental conditions

replaces germanium types directly pin-to-pin

Devices	Applications	LVCEO (V)	Ic max (mA)	fr (GHz)	lc (mA)	Vce (V)	PG (dB)	NF (dB)	f (GHz)	Equivalent germanium types	Package
BF479S BF479 BF679 BF679M BF679S BF680A	Amplifier for PIN-Diode tuner High current VHF-UHF amplifier UHF AGC amplifier UHF mixer-oscillator Low noise UHF AGC amplifier UHF mixer-oscillator	25 25 35 35 35 35	50 50 30 30 30 30	1.3 1.4 1 1 0.65	8 10 3 3 3 3	10 10 10 10 10 10	15 18 15 15 16 12	3.5 3.5 3.5 4 3 5	0.8 0.8 0.8	AF379 AF279-AF367 AF369 AF279S AF280-AF369	T plastic
BFT95 BFT96	Wide-band amplifier up to 1.5 GHz Medium-power amp. up to 1.5 GHz	15 15	50 100	55	15 50	10 10	12 10	24	1		T plastic
BFT95H	Wide-band amplifier for hybrids	15	50	5	15	10	12	2	1		Lead formed T plastic
BF324 BF414 BF506 BF509	VHF-FM tuner VHF-FM Low noise VHF mixer-oscillator VHF AGC amplifier	35 30 35 35	30 25 30 30	0.4 0.4 0.4 0.7	1 1 1 3	10 10 10 10	- 17 18	3 2 2.5 2	0.1 0.1 0.2 0.2	AF106-AF306 AF109	TO 92
BF272A BF316A BF516 BFR38 BFR99	UHF AGC amplifier UHF mixer-oscillator RF general purpose VHF-UHF amplifier Low cross-mod. VHF-UHF amplifier	35 35 35 35 25	20 20 20 20 50	0.85 0.6 0.8 1 2.3	3 3 3 3 10	10 10 10 10 15	15 12 12 14 10	3.5 5 4 3.5 3.5		AF239 AF139-AF240 AF239	TO 72



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- Wide measurement values allow you to test a greater number of component types. Test L from 00.001 to 99999 μ H; C from 00.001 to 99999 pF, Q from 00.01 to 999.9, D from .0001 to 9.999, R from 00.01 Ω to 999.9 K Ω , and G from 00.01 μ S to 999.9 mS.
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SGS-ATES NPN RF PRODUCT RANGE

SGS-ATES production includes a variety of RF NPN silicon transistors, as shown in the following table. Some of these products, which are intended for well-established solutions, are second sourced by SGS-ATES. In addition, constant research and development provide a steady flow of new products for new and more sophisticated applications. The latest of these new products is the BFW 94 for ultralinear wide band applications up to 1.5 GHz.

Devices	Applications	VCBO (V)	LVCEO (V)	lc max (mA)	fr (GHz)	lc (mA)	Vce (V)	Pa (dB)	NF (dB)	f (GHz)	Package
BFW92 BFR90 BFR90A BFR91* BFR96*	Wide band amplifier Wide band amplifier up to 1.5 GHz Wide band amplifier up to 1.5 GHz Wide band amplifier up to 1.5 GHz Medium power amplifier up to 1.5 GHz	25 20 20 15 20	15 15 15 12 15	50 25 25 50 100	1.6 5 5 5 5	25 14 14 30 50	5 10 10 5 10	16 19.5 13.5 16.5 16	4 2.4 2.2 3.3	0.5 0.5 1 0.5 0.5	T plastic
BFW94	Ultralinear wide band amplifier	25	20	200	3	80	7.5	14	5	0.5	4 leads, plastic
BFR36 BFW16A BFW17A 2N3866 2N4427 2N5109	Ultralinear CATV-MATV output Ultralinear CATV-MATV output Ultralinear CATV-MATV output VHF-UHF power amplifier and oscillator VHF-UHF power amplifier and oscillator Ultralinear CATV-MATV output	40 40 55 40 40	30 25 25 30 20 20	200 200 500 500 200	1.4 1.4 1.3 1 1.3	70 70 70 50 50 50	15 15 15 15 15 15	16 16 10 16	4 5 6 - 3	0.2 0.2 0.2 0.4 - 0.2	TO 39
BFX89 BFY90 2N918 2N2857 2N3600 2N3839 2N5179	Wide band amplifier Wide band amplifier Amplifier and oscillator VHF-UHF amplifier VHF amplifier Low noise UHF-VHF VHF-UHF amplifier	30 30 30 30 30 30 20	15 15 15 15 15 15 15 12	50 50 50 50 50 50 50	1.2 1.4 0.8 1.2 1 1.4 1.4	25 25 4 5 5 5 5	5 5 10 6 6 6 6	12 13 21 16 22 17 21	6.5 5 3.8 4 3 3	0.5 0.5 0.2 0.45 0.2 0.45 0.2	TO 72



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I/O Power

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News scope

JANUARY 18, 1978

E-beam + X-ray litho = high-density circuits

By combining both E-beam and Xray lithography processes, engineers at Rockwell International's Electron Devices Group expect to solve production problems encountered with the highdensity fabrication methods—resolution, processing speed, and resist composition, for starters.

Although either technique can be used to obtain very fine line widths, Ebeam techniques by themselves would just take too long to mass-produce wafers, says George Pulliam, Director of Physical Sciences at the Anaheimbased facility. However, E-beam techniques do offer the flexibility of being able to alter the pattern being drawn on the fly—different adjustments can be made on the same wafer under computer control of the electron beam.

Soon, the E-beam process will be used to make a master pattern and then X-ray processing along with a step-and-repeat sequence will generate a complete wafer mask from the master. At this point, however, this combined technology isn't ready to be applied to a production line.

Right now the resists used on the

wafers are too slow or don't have the necessary resolution. Development speed of the resist must go up so that exposure time for the wafer can go down. The shortened exposure time will result in less harm to the semiconductor material, which can be irreparably damaged by E-beam and Xray bombardment.

As the devices on chips get smaller, speed increases and power decreases. But that isn't all. Certain "edge effects" and threshold voltages are becoming more of a factor in device design. In some of the large devices of, say, a year or two ago the effects could be ignored. To handle new factors such as these, new device models will have to be developed so that performance predictions can be made more accurately before sample devices are made.

Still, work on the E-beam/X-ray process has reached the point where a 4-megabit magnetic-bubble memory on a single chip is considered feasible for late 1978 or early 1979 production. The chip is expected to be about 0.4 in.² and have a serial data transfer rate of about 0.5 MHz.

IC flowmeter measures blood in two directions

A totally implantable pulsed-Doppler blood-flowmeter is the first to measure blood-vessel diameter and bidirectional flow. But it wouldn't have been possible without IC chips to hold the Doppler electronics.

Like pulsed-Doppler radar, the ultrasonic system, designed at Stanford University's Integrated Circuits Laboratory, in Palo Alto, CA, telemeters both velocity and range information. It uses range data to measure diameter and volume flow as well as bloodvelocity profiles. Bidirectional velocities are shown at 16 points along the vessel's inner diameter.

Bidirectionality is needed because blood flow may reverse during part of

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each heart cycle and turbulence may cause local reversals at other times. Ultimately, the tiny unit may be implanted in an unborn lamb to provide new information on fetal heart functions—up to and even during birth.

Designed to transmit data on command for six months or more, the implantable system consists of four packages connected by Teflon-covered wires: Doppler electronics, a transducer, a battery and an output-data coil (antenna).

The Doppler electronics, with over 200 linear circuit components on two 3-mm-square custom IC chips, has only eight discrete parts. Mounted on a hybrid substrate in a hermetic can and encapsulated, they occupy only 2.9 \times 3.8 \times 0.8 cm.

"This pulsed Doppler design is so complex, it would have been impossibly bulky without custom ICs and hybrid interconnect," says Dr. James Knutti, co-designer of the system. One Doppler IC generates the pulsed 6-MHz ultrasonic signal and quadrature reference signals; the other receives the Doppler-shifted signal, compares it to the references, and outputs pulse-delay and difference-frequency data to external electronics via the data coil.

Sutured against the side of a vessel, the transducer, a 3-mm-square leadtitanate-zirconate crystal, sends and receives the 25-kHz pulses of 6-MHz ultrasound.

To extend the operation of the 50hour battery, an external rf burst turns power on. After a preselected 1-to-5 minute interval of 20-mW operation, two oscillator/counter chips encapsulated with the battery turn the power off again.

CRT brightness boosted by tweaking gun design

A 20 to 40% increase in the brightness of an electrostatic CRT display—with no loss of resolution—has been achieved by optimizing element lengths and aperture positions and diameters in the CRT's electron gun. This higher brightness not only improves visibility in high-ambient lighting, but also increases the separation between displayed shades of gray, a feature needed in diagnostic medical ultrasound and nondestructive-testing displays.

The improvements, developed at Hewlett-Packard Co.'s Colorado Springs Division, are achieved "through a rigorous application of generally accepted ray-tracing theory and equations that don't involve any modifications in classical electron lens theory," says product manager Art Porter. Computer-aided design techniques yielded a CRT electron gun with very few stray electrons. The electron lens increases brightness by focusing more electrons on the correct spot on the screen.

Two versions of the new CRT will be available next month in HP's Model 1332A display unit. A standard version, which will cost the same as the 1332A and previous CRT, \$1400, maintains the present spot size of 0.3 mm, but with a 20 to 40% increase in brightness. An even brighter version, the Option 530, adds \$75 to the price tag, and is two and a half times brighter than the CRT currently in the 1332A, but with only a 10 to 15% increase in spot diameter. With a spot size of 0.38 mm, this Option 530 has a specified brightness of 500 cd/m² (about 150 foot-Lamberts) at 2.5mm/ μ s writing speed and a 60-Hz refresh rate.

In the other version, the CRT's beam current is to three times greater than for existing designs, with no increase in accelerating voltage, power consumption, or circuit complexity.

CIRCLE NO. 319

Alarm clock wakes you up —and puts the coffee on

The most flexible "alarm clock" yet not only gets you up but turns home appliances on or off at preset times. Up to 100 line-powered appliances such as coffee makers, lights, engine-oil heaters and hi-fi systems can be handled by a central-control console via coded pulses riding on the ac line.

The Coby 1 home control center from Energy Technology Inc., Las Cruces, NM, is built around an Intel 8085 microprocessor. It can be programmed to turn equipment on or off at times that can be set up to 11 months in advance.

The control center sends coded pulses over house wiring to remote switches that go between plug-in appliances and wall sockets. In a few months, Energy Technology expects to have remotes to replace wall switches and other remotes to handle built-in equipment such as water heaters and air conditioners. Each remote will have a unique address.

Programs are entered, stored, and modified through 12 function and control keys, a 10-key numeric pad, and AM and PM keys. As commands are entered, a display lights up to confirm. The display can also review commands already stored in memory.

The display reads out year, month, day, hour, minute and second with an accuracy to five seconds per month. The calendar is preprogrammed to show the correct date until 2021.

Along with control, power supply, coding and signal-generating circuitry, the control console contains 2048 words of RAM and 2048 bytes of ROM. A rechargeable battery will keep the clock and other memory circuits working during a blackout. The battery, which recharges whenever the control console is plugged in, also allows the console to be unplugged and moved without losing memory contents.

The suggested retail price for the Coby 1 control console is \$450, and each remote is \$45. But until the end of February, one console and one remote will go for \$399.

Packet-switched data transmitted by radio

Packet switching, a data-communications technique usually involving copper wires or optical fibers, has taken to the airwaves. A system of packet-switched radio data links using microprocessors to route tactical messages from one mode to another has been developed to enhance tactical radio communications for military field operations. Both fixed base and mobile units can participate in the network developed by the Collins Telecommunications Div. of Rockwell International in Dallas, TX.

Packets of data with identifying headers and error-correcting trailers are broadcast from a main station and routed independently and asynchronously throughout the system. Actual transmission is spread over a wide band of frequencies to provide special safeguards against jamming and eavesdropping.

Rockwell is developing the packetswitched radio-communications system for the Advanced Research Projects Agency. So far, 28 packet radios have been built for ARPA and are being evaluated by Stanford Research Institute.

PCBs get broken up by electron 'bullets'

How do you get rid of the toxic effects of polychlorinated biphenyls? Until recently, with great difficulty. Now, researchers at the Massachusetts Institute of Technology have discovered that high-speed electron bombardment—about 10 kilorads—significantly alters the composition of PCBs or other toxic organic compounds in water, and prevents the toxic material from building up in the food chain.

"The high-speed electrons are like bullets," according to Dr. Edward W. Merrill, professor of chemical engineering at MIT. "When they hit the water molecule, it splits into very active fragments, one of which is called the hydroxyl radical. This radical attaches itself to the trace organic compound—such as the PCB—and transforms it into a molecule, like alcohol, which has a hydroxyl group that makes it water soluble."

PCBs are widely used as cleaning fluids for PC boards and other hardware, in electrolytic capacitors and in transformers for insulation and cooling. They are persistent toxic agents in other words, they degrade extremely slowly in the environment and exist in water or animal tissue for a long time.

The MIT researchers also found that electron bombardment doses of about 400 kilorads may obliterate PCBs in sludge. But more experiments are needed, they point out, because the makeup of sludge varies from day to day—even from hour to hour—at any given location.

Problem studies aimed at microwave solar energy

Two studies are being conducted to determine the negative or harmful effects of transmitting solar energy in the form of microwaves to earth stations, which would convert them into electricity. Both studies are being handled by Battelle Memorial Institute's Pacific Northwest Laboratories, Richland, WA, at the request of the Dept. of Energy and NASA.

The microwave transmissions would come from a proposed series of satellites in stationary orbits around the earth. Solar energy, caught above the earth's atmosphere would be converted into microwave energy on the satellites. Researchers have calculated that 20 to 25 satellites could have provided all of the United States' power needs in 1975.

But what problems would crop up with these microwave transmissions? One Battelle study group will try to find out if any electromagnetic or radio interference trouble would stem from such transmissions. The other group will try to uncover any potential harmful effects on the earth's environment. All work is expected to be completed by September, 1978.

R & D spending up in '78

National spending on research and development will reach \$44.1-billion this year, according to Battelle Columbus Laboratories, Columbus, OH. That's an increase of \$3.3-billion, or 8%, over National Science Foundation estimates for 1977, but the Ohio research group says the increase will be entirely swallowed up by inflation and represents no real growth.

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DP Dialogue

Notes and observations from IBM that may prove of interest to the engineering community



Terminal Stands the Heat at Ford Steel

Computer equipment has now moved right up to the mouth of the fiery furnace. At River Rouge, Ford Motor Company's sprawling complex of industrial plants in Dearborn, Michigan, IBM 5937 Industrial Terminals adjacent to two huge steelmaking units — a basic oxygen furnace and an electric furnace — guide operators in the crucial step of measuring alloying ingredients into the molten metal. Because the 5937 is tolerant of extreme heat, vibration and Steel from the basic oxygen furnace at Ford is poured into ingot molds. An IBM 5937 Industrial Terminal helps the furnace operators control the amount of costly alloying materials they add during the heat.

corrosive atmosphere, it can be installed where no ordinary computer terminal would work for long.

Ford Steel Division makes and processes over 10,000 tons of steel a day. In its completely integrated River Rouge facility, the division smelts ore and performs a wide variety of steel-making and finishing operations. An online computer tracks every slab of steel from the furnace right up to shipment to the customer, using data acquired through sensors in the processing machinery.

Closing the Loop

The two IBM 5937 Industrial Terminals close the loop from the metallurgical laboratory back to the furnace operators. The loop begins at the furnace, where a small sample of the molten steel is drawn and sent to the laboratory — in another building—through a pneumatic-tube delivery system. The lab promptly analyzes the sample, and the results pass automatically from the analytical instruments to the IBM System/370 Model 148.

"When the operator is ready to add alloying ingredients," explains Earl O'Shaughnessy, general superintendent of basic oxygen furnace melting operations, "the computer flashes a chemical analysis to him that shows just how much of each additive to use."

It is this analysis that tells the furnace operator how much manganese, aluminum, carbon, silicon or other alloying material must be added to make the type of steel required of each melt.

"Before we had the 5937 terminals, the operators had to walk to a typewriter terminal in a protected environment some distance away to see the analysis," O'Shaughnessy says. "Or, if time was short, they simply added excessive amounts of these costly materials, to make sure the specifications were met.

"Putting a rugged terminal like the 5937 right out on the floor with the operators has meant significant direct dollar savings in steelmaking costs."

CADAM: Interactive Graphics for Design Engineers

Producing a modern aircraft can require more mechanical drawings than rivets.

Traditionally, engineers sketch, then draftsmen draft. Then engineers discover needed changes or improvements, and draftsmen draft some more. A lot more. Move a stiffener or bracket, say, two inches to the left, and a chain reaction of changes riffles through the entire set of drawings.

But now the computer has opened up a new way to meet design engineering needs with speed and reliability for a broad range of products, from highperformance aircraft to complex integrated circuits. Computer-Graphics Augmented Design and Manufacturing (CADAM), a set of interactive programs available from IBM, allows the designer to sketch directly on the screen of a graphic terminal. He defines lines and contours by pressing keys and positioning a light pen, and the computer displays what he has expressed.

Curve fitting, or reducing the design to a set of control equations, is completed iteratively at the terminal, eliminating coding, card punching, and repeated computer batch runs. Then CADAM converts the preliminary design to a dimensioned drawing with auxiliary views.

If something needs fixing — if, for example, the dimensioned drawing reveals a problem of component or subassembly compatibility — the pieces can be moved around with the light pen and CADAM will revise all of the affected drawings. And do it automatically.

® CADAM is a trademark of Lockheed-California Corp.

CADAM encourages doodling, an important source of design inspiration. The user can translate or rotate any graphic element. Or change its scale. Or stack parts, separate them, or watch moving parts move.

CADAM stores the design as it is developed, displays any element on demand, then generates the final detailed drawings. It supports complete design of the part, including structural members and such elements as ribs, stiffeners, lightening holes and fasteners. Once a design is stored in the system, CADAM analysis programs can calculate its weight or determine its structural properties. Any frequently used design element or drawing symbol can be stored and reproduced automatically wherever it is needed.

As its name implies, CADAM includes a direct link to manufacturing. It can generate a "part program" (path of travel) for the cutter of an automatic machine tool.

CADAM has cut drafting manhours drastically for engineering departments —by as much as 90 percent or more on a few special tasks. It helps prevent and correct errors and improves the quality of the engineering product. One user's experience is described below.

Productivity Up

Northrop Corporation is one of the world's largest manufacturers of high performance jet aircraft. Today, Northrop engineers design complex aircraft parts with CADAM in a fraction of the time once spent at drafting boards.



Engineers at Northrop Corp. use computer graphics to speed the structural design of high-performance jet aircraft.



CADAM converts freehand sketches, made directly on the CRT screen with a light pen, into fully defined and dimensioned graphics.

Says Northrop's Aaron Feder: "In addition to the time savings, we can identify improvements in design quality. Because changes are so easy to make at a CADAM terminal, we can keep up with changes traditionally required during the design development of an aircraft part and still release the drawing on time." Feder is manager of technical computer graphics at Northrop's Aircraft Division in Hawthorne, California.

"Before installing CADAM," Feder points out, "we ran a number of carefully controlled tests. When we saw productivity gains ranging from four to one to as high as 17 to one, for changes to a drawing, we saw the potential for CADAM and decided to adopt it.

"We compared the manhours required to prepare several types of drawings using CADAM with the time requirements using our established manual systems.

"This involved a broad sampling of different types of drawings, including layouts, structural and electrical drawings. We saw productivity gains of four to one or better on every one of 14 test problems. Even though productivity is lower in the hectic, day-to-day development design world, CADAM has still proven cost-effective.

"Once a tentative design is in the computer," Feder adds, "we can run CADAM engineering analyses: calculating weights and determining the capabilities of the design aircraft and the dynamic behavior of its structure.

"The data required for this kind of analysis is already in our System/370 as a byproduct of the graphic design effort. That means another major savings in manhours, the elimination of a significant source of error, and the assurance that all departments are working from the same data."
Fast Answers to Tough Energy Questions

"Suppose the government made major changes in national energy policy," speculates Prof. John J. Donovan of MIT. "What would be the economic impact on each region of the U.S.? How would the economy change if the fuel supply were to be altered? If prices were to change? What effective actions can be taken by homeowners, industry and public policymakers?"

To help provide prompt answers to such questions, the Generalized Management Information System (GMIS) was jointly developed by IBM, MIT Sloan School of Management and the MIT Energy Laboratory. IBM provided staff support and the use of a System/370 Model 158 at its Cambridge Scientific Center. GMIS has been used to analyze conservation strategy in, for example, the consumption of energy for residential heating across the United States. And it has been used to produce programs and a data base for energy policy analysis in New England. Called the New England Energy Management Information System (NEEMIS), this application was developed through a collaborative effort among MIT, the New England Regional Commission (a Federal-New England states partnership) and IBM.

What can the homeowner do? According to Donovan, an associate professor at the Sloan School: "An econometric model shows that, for a homeowner in the Northeast or upper Midwest, a thermostat setting of 65 degrees (daytime) and 55 at night — or 63 around the clock — will save 15 percent of his energy costs.

"Other computer models produced using GMIS suggest measures for commercial buildings. For some institutions in the Boston area, these models identified ways to reduce energy costs by 40 percent (of which 20 percent required no capital improvements).

"To answer questions like these," he continues, "the Energy Laboratory has



Most homeowners today want to keep warm without wasting energy. At MIT, computer simulation has shown that a 24-hour thermostat setting of 63 degrees saves as much fuel as a night setting of 55 degrees.

collected data and computer programs from government research, professional and technical groups, and university research efforts. A user can scan the data base interactively to locate and define the needed data and select a suitable modeling system.

"GMIS is a universal bridge to this diverse collection of data: Whatever type of analysis is to be used — a simulation or a regression analysis, for instance — GMIS provides the interface between the required language and the data."

Users with terminals in their offices are now working out solutions interactively. Using programs created under GMIS, engineers in the government of the state of Maine are conducting studies to determine the best use of the money available for energy conservation.

GMIS data has helped the New England region avert a proposed oil tariff by demonstrating its negative economic effects there.

"Sound public and private policymaking and resource management require prompt, accurate information on many such issues," Donovan says. "GMIS is designed expressly as a tool to provide that information."

FORTRAN and Logic Programming Aids

Three program products available from IBM simplify the programming of engineering and scientific applications:

1. FORTRAN Interactive Conversion Aid facilitates the conversion of non-System/370 FORTRAN dialects into System/370 FORTRAN IV executable source code.

2. APL Decision Table Processor (DTABL) converts a decision table (a powerful method of notation for complex logic) into an executable program. 3. FORTRAN Interactive Subroutine Library (FISLIB) makes FORTRAN a truly interactive tool for any application that requires human judgment during the course of the program.

For more information on these and other IBM program products, contact your local IBM branch office or write to the Editor of DP Dialogue at the address on the right. DP Dialogue is designed to provide you with useful information about data processing applications, concepts and techniques. For more information about IBM products or services, contact your local IBM branch office, or write Editor: DP Dialogue, IBM Data Processing Division, White Plains, N.Y. 10604.





Time was when a mini was a mini, a micro was a micro, and the picking was easy. Not any more.

Should the computer in your next equipment be a minicomputer or a microcomputer? A year or two ago, you would have answered the question much faster. You would have known that:

- Minis come in boxes, micros don't
- Minis are "turnkey," micros aren't
- Minis cost more than micros
- Minis are larger than micros
- Minis are faster than micros

Minis use longer words than micros

Minis offer more software support

 Minis can address more memory But now these "truths" have become "maybes." There are enough exceptions to make you stop and examine each fact before you decide which road to take.

"The real difference between the two groups is the marketing approach," says Adolf Monosson, President of American Used Computer Corp. (Boston, MA). He would keep microcomputers in the hands of designers: "If a businessman's μ C fails, he can't afford to take the hardware and his data to a technician." But Ed Zander, Manager of Data General's Micro Prod-

Max J. Schindler Associate Editor ucts Marketing Group, disagrees. "We provide the same maintenance for the microNova as for the Nova."

Both are right, but full support is still more the exception than the rule for μ Cs. Although μ Cs have by now infiltrated practically all mini applications, the bulk of the micro business does not come from end users, but from OEMs like you. But while you often choose your own computer configuration (Fig. 1) and write much of your own software, you may not always have the time.

If you opted for a small "turnkey" system a year or two ago, you would probably have wound up with a minicomputer. But today half the microcomputer models on the market come ready to plug-in and run. On the other hand, many minicomputer makers have retaliated by shedding their minis' power supplies and housings.

A matter of dollars and sense

While you can no longer tell a mini from a micro by its looks, perhaps you can tell them apart by their price tag?

"A micro is a mini at half the price," quips Hugh O'Neill of New Engineering Systems (Peacehaven, England). In fact, the cost difference between minis and micros can be much larger. According to Ronald Todd, President of ECD (Cambridge, MA), his company's \$2500 MicroMind II outperforms minis in the \$40,000 class.

But the price difference can also be quite small. Data General's smallest Nova costs \$2600, while the minimum microNova configuration goes for \$1995. DEC's LSI-11 microcomputers (Fig. 2) go for \$634 to \$1594, while the Naked Mini of Computer Automation sells for \$548, and Interdata's 516, single-board mini costs \$898 (all in quantities of 100).

Computers in various degrees of undress are obviously not aimed at the end-user, unless he happens to be a hobbyist (i.e. often an engineer after hours). Yet, it seems that mini makers don't compete very hard for that big OEM market. Fig. 3 shows clearly why most minicomputer makers are more interested in expanding the top of their line, than in fending off microcomputer inroads at the low end.

The low-end mini with its established software support is, however, still a viable alternative in some OEM applications. "Only for high-volume designs does it pay the OEM to duplicate existing mini capability," comments Bill Rosser, Vice President for



Corporate Development at Perkin-Elmer Data Systems, Interdata's parent. With increasing volume, the economics shift to the special-purpose micro, and eventually (in the high thousands) to the custom-LSI chip, a descendent of hard-wired logic.

Smaller is better

Often size is more important than price, and there the microcomputer has a clear lead. After all, the smallest computers are one-chip micros. And Texas Instruments Chairman, Mark Shepherd Jr. predicts that by 1982 or 1983 TI will have a single-chip 32-bit μP with 1 Mbit of on-board memory.

Size is also the major distinction between minis and micros for Data General's Ed Zander. "But when the size is comparable, it's just a marketing decision whether to call the machine a micro or a mini," he adds (see Fig. 4).

So, it has become very hard to distinguish minis clearly from micros by such external characteristics as housings, price or size. But will the important operating charcteristics-speed, addressable memory, throughputclear up the picture?

"While microcomputers are LSI devices, minis are largely based on MSI

chips, and that's inherently a faster technology," states Ned Chang, Senior Marketing Vice President of Wang Laboratories. Gary Cole, PDP8 Product Planning Manager at DEC, concurs. "Bipolar technology and separate buses give minis a speed advantage over the mostly NMOS-based micros."

Victor Maxted, Minicomputer Marketing Manager of Raytheon's Data Systems Co. estimates that minis execute instructions about twice as fast as micros; in data transfer rate, the difference is even bigger: Mbytes/s for the minis, compared with 10 to 100 kbyte/s for the micros.

Paul Wintz, President of Wintek (Lafayette, IN) offers the following comparison:

6800-based

micro	computer					
Cycle time	1000 ns					
Throughput	1.6×10^4 bit/s					
16-bit multiply	2 ms					

PDP11/45

minicomputer Cycle time 200 ns Throughput 6.4×10^6 bit/s 16-bit multiply 5 µs And that does not include the effect of many minis' powerful microinstructions, which can require whole subroutines in a μ C.

But some additional chips can boost the speed of a micro to give minis a good run for their money. Advanced Micro Devices' 9511 math chip reportedly increases the performance/ price ratio of a μ C by a factor of ten. And Hewlett-Packard's silicon-on-sapphire technology-although at present limited to HP instruments-is going to improve speed in general, while reducing power consumption.

Intel's new peripheral chips are eliminating some of the µCs' I/O restrictions, and throughput is catching up generally. Take the well-stacked, suitcase-size μ C Micral C (Fig. 4) from R2E (Orsay, France), which claims a transfer rate of 920 kbyte/s-higher than the PDP11/45's.

Meanwhile, another "absolute truth" is beginning to wreak havoc with definitions of minicomputers and microcomputers.

Putting in their 8 bits' worth

"I suggest we call computers with 16 bits or more minis, and anything less micros," says Dwight D. Carlson, President of PCS (Saline, MI). If he could persuade his industry to accept that definition, life would be easier for the



1. **OEMs often build their own microcomputers** and integrate them into their systems. In Foxboro Co.'s VIDEOSCOPE, the logic cards are at top left, the CRT is at top right, and the power supply is at the bottom.

digital designer. But then, how do you label a 16-bit machine that's put together from 4-bit slices like AMD's 2901? Or TI's promised 32-bit computer on a single chip? Or a μ C with address, instruction, and data word lengths both above and below 16 bits?

And then there are μ Cs like the Intel SBC80/20. By using a bus-master chip on the board, Intel can parallel up to 16 of these boards, communicating over a 16-bit bus. "They can even use a mini as a slave," says Jim Medlin, Intel Application Engineer. So, he offers a different definition: "Minis can develop their own software, while micros can't." But some micros can. "Learning to design good software takes 5 to 10 years," says DEC's Gary Cole. And it seems that chip makers like Intel have now accumulated that knowledge, and are duplicating the evolution 10 years ago of minicomputers into full-fledged systems.

Because programming time is so expensive, more and more higher-level languages are being implemented in microcomputer systems. Although Basic and Pascal are current favorites, compilers for PL/I and Fortran derivatives have found their way into μ C operating systems. But software houses like FORTH Inc. are developing



2. **The LSI-11/2 microcomputer from DEC** can operate many programs developed for the PDP-11, at a fraction of the mini's cost. The operating system contains Fortran, Basic, APL and FOCAL.

new languages, better tuned to μP architecture. "We find the compact code of μ FORTH ideal for our microcomputer products," says Robert Winder, Director, MOS Systems at RCA (Somerville, NJ).

Software no paper tiger

While μ C-system software is getting better, what about application software? For large customers, a μ C vendor may provide software assistance, but most OEMs have to design their own, often using the chip makers' development system.

Microcomputer-based software development, however, may not be the best approach. Compilation is slow, and diagnostics limited. According to Mike Rooney, President of Boston Systems Office (Boston, MA), "99.9% of all programmers make mistakes. A development system on a large computer can make it a lot easier to find and correct them—and maybe as much as 10 to 50 times cheaper."

Cross-assemblers run mostly on minicomputers, and are also available on several time-sharing systems. But before you commit yourself to any one, get a benchmark—development costs can vary by more than an order of magnitude between systems.

Another problem with μ C-software development is the profusion of instruction sets, and the frequent chip improvements. "If only they kept the instructions and pin-out constant!" laments Foxboro's Corporate Research Manager Richard Caro.

So a large OEM like Foxboro Co. (Foxboro, MA) is designing its own μ Cs for industrial controls from bit slices and other LSI chips. "That way we retain control over our software," explains Caro.

All sorts of memories

The amount of addressable memory is another bone of contention between minis and micros. "A microprocessor's 40-pin DIP certainly imposes limitations on the microcomputer," comments DEC's Gary Cole. But multiplechip CPU sets and multiplexed address/data buses help to overcome this limitation. And Texas Instruments now puts its SPB 9900 microprocessor in 64-pin DIPs to gain more bus lines.

So, here too, the distinction between micros and minis is fading. Directly addressable memory of 64 kbytes is no longer a rarity for a μ C. ECD's Micro-

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3. In total dollars, microcomputers are still "small fry"—compared with minis and mainframes—as this chart from Perkin-Elmer's Data Systems shows. It was compiled for the 1977 market.

Mind 2 is even said to access 64 Mbytes. And it's almost common practice to treat all peripherals as memory. "We use the I/O ports on our micros now only for special functions," says Doug Cassell, Marketing Vice President of Control Logic (Framingham, MA).

Just as the minicomputer's development depended on dropping core prices, the continuing reduction of semiconductor memory prices will largely determine the microcomputer's future development—not so much because lower memory prices open up new applications, but because they affect software development. While memory was scarce, machine and assembly languages prevailed. But by now the cost of software already outweighs that of hardware more often than not, and the ratio is steadily getting worse. What's the answer?

Some μ C designers are venturing into territory not previously cultivated by minis. J. T. Boren, Marketing Manager at Sperry Univac predicts a new breed of much more cost-effective, solution-oriented machines, with software-dominated architecture. Other industry experts echo this forecast. But nobody is ready to say just how that software/hardware merger will be im-



5. This well-stacked μ C in a suitcase contains a plasma display, floppy drive and printer. It comes from R2E (France), and obviously speaks Le Basic.



4. Fully dressed, minis and micros are often hard to tell apart. Perkin-Elmer's Interdata 516 (top) is a minicomputer, while Data General's microNova is a micro. Why? Because their makers say so.

plemented in practical systems.

In any case, the next breakthrough in data processing will probably come in CPU architecture. Except for scientific applications (which constitute a tiny share of the data processing market), typically 90% of processing time is taken up with data sorting or storing. And today's address-oriented CPU architecture is ill-suited for that task.

So, what will the data-processing system of the future look like? It makes little sense to build a \$50,000 system around a \$10 processor. Terminals, disc drives, and peripherals of all kinds could perform 60% of a computer's processing load, according to Larry MacPherson of Interdata, a Perkin-Elmer subsidiary (Oceanport, NJ). So, it's much more sensible to distribute processing activities throughout the system as in Intel's $80/20 \ \mu$ C.

One 80/20-based micro system, Realistic Controls' Z//300 supports up to 480 terminals, with 1.2 billion bytes of memory. A Z//300 can take care of inventory, payroll, scheduling, shipping, and general ledger. Even at maximum configuration, terminal reaction time will not exceed 4 seconds, says Dr. Leroy Anderson, Realistic's General Manager. Many a mini would be proud of such performance.

(continued on page 30)

Whether you use an MDS or a computer for microprocessor-based system development,

you need this Logic State Analyzer to speed debugging.

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CIRCLE NUMBER 19

(continued from page 28)

	Circle		Micro	compute	Minicomputer		Other	
Companies	Circle number	Chip	Board	1	Devel. sys.	Boards		products
Advanced Micro Devices	451	•	•		•	C. Sugar		
American Microsystems	452		•	A. B. S.	•			•
Apple Computer	453			•				
Applied Data Communications	454			•				
Applied Systems Corp.	455		•					•
Automated Computer Systems	456		a seren a	•				
Bedford Computer Systems	457		•					
Boston Systems Office	458						•	•
Burroughs Corp.	459							
Byte Inc.	460							
Central Data	461		•				The second	
Computer Automation	462			•		•	1	
Control Data	463						•	•
Control Logic	464		•	•	•			
Cramer Electronics	465							
Cromemco	466		•	•	PARTICIPAL OF			No.
Data General	467							
Datanumerics	468		•					
Digimetric	469							
Digital Equipment	470							
Digital Group	470						NOT THE	
E & L Instruments	472							
ECD Corp.	473							
Electronic Control Technology	474							
Electronic Memories & Magn.	475							
Fairchild Instr. & Controls	476					COLONE DE LA		Sector Sector
Ferranti	477						and the second	
Futuredata (Microkit)	478							Service Service
General Automation	479							
General Instruments	480					The Martin		
Gnat Computers	481							
GRI Computer Corp.	482							5. 32
Harris Computers	483			1.1.1	100			
Harris Semiconductors	484		1.1.1.1.1.1					6.67
Heurikon Corp.	485							
Hewlett-Packard	486							
Honeywell	487							
Hughes Solid State Div.	488							
lasis Inc.	489							
IBM Corp.	490			N. Carlos				
IMS Inc.	491							
Imsai	492		•			1. 199		
Infinite Inc.	493							
Information Control	494							
Intel	494						-	
Intersil	495							-
IT&T	497							
Microcomputer Associates	498							
Microcomputer Associates	450					Service and the service of the servi		

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GENERAL 🍪 ELECTRIC

CIRCLE NUMBER 20

(continued from page 30)

Companies	Circle		Micro	compute	Minicomputer		Other	
	number	Chip	Board	System	Devel. sys.	Boards	Systems	product
Microdata	499		1				•	•
MITS, Inc.	500	1. 1. 1.		•	10.11		Philip and	
Modcomp	501	10.19	1.15				•	
Monolithic Memories	502		-		1 1 1 1 2 1		1000	
Monolithic Systems	503	- Artic			•			
MOS Technology	504							
Mostek	505							
Motorola	506				•		N. W. S. M.	
Multisonics	507							11.5
muPro, Inc.	508				•		1	
National Semiconductor	509						and the set	•
NEC Microcomputers Inc.	510							
North Star Computers	511							
Ohio Scientific	512	12 and						1
Omnibyte	513							
Omron	513							
Panasonic	515							
PC/M Inc.	516						And the Ste	
	517							
Perkin-Elmer (Interdata)		-10.5						
Plessey	518		-					
Prime Computer	519	A see					•	See - See
Process Computer Systems	520	10	•		•		No. State	No.
Processor Technology	521			•				
Pro-Log Corp.	522	146						
Quay	523		•					11111
Raytheon Data Systems	524						•	
RCA Solid State Div.	525	•						
RCI/Data	526	E.A.	•	•				
Relational Memory Systems	527		•	•				
Rockwell International Inc.	528	•	•	•	•			A. A. Const
R2E America	529			•			1.4	
Scientific Microsystems	530	•	•	•			Non co	
Signetics	531	•	•	•	•		Start &	3
Southwest Technical Products	532		•	•			EN LON ET	1
Space Byte Corp.	533	14.14	•	•	•			
Sperry-Univac (Varian)	534			Server 5	State State		•	
Technical Design Labs	535			•			and the second	
Tektronix	536			•	•			•
Texas Instruments	537	.•	•	1919	•	•	•	•
Toshiba	538	•					Sec. 20	
Three Phoenix	539			•				•
Wang Laboratories	540						•	•
Warner & Swasey	541		•	•	•			
Western Digital	542	•	•					
Wintek	543		•	•	•		The Party	
Wyle Laboratories	544	-	•	•	•			•
Zilog	545	•	•	•	•			

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CIRCLE NUMBER 21

CRT terminals will be more complex, but simpler to build

The CRT terminals of the future will be simpler—and more complex. New LSI devices are reducing the number of circuits necessary to build simple terminal systems, even as user demand for more features is adding more and more circuitry to the terminal. So claimed Lee Felsenstein, President of LGC Engineering (Berkeley, CA), in his paper at the Mini/Micro 77 conference in Anaheim, CA.

Low-cost terminals will work with one-chip and general-purpose microprocessors, and even ordinary television receivers. Moreover, the microcomputer and specialized controller circuits will permit a minimal system to be built with less than two dozen IC packages. This is one reason terminals for low-end systems will drop from over \$600 all the way to about \$200 in another year or two.

Personal computing cuts cost, too

Another reason is the personal computing explosion—users are looking for virtually minimal performance at minimum cost. And, since many of the personal-computing applications do not demand high resolution, a television receiver can be used to display the data. Typical displays are 16 lines \times either 32 or 64 characters per line for alphanumeric data and up to 256 \times 256 points for graphic displays.

A television receiver, fed either by a modulated rf or a composite video signal, eliminates a major part of a CRT terminal's cost—the video monitor.

Meanwhile, however, applications that demand high resolution or special graphics capabilities are increasing. Thanks to microprocessors, the ability to perform editing, graphics and special functions without a remote computer is getting easier to design into terminals.

But with all this added capability, terminal complexity will also rise—but not just in hardware. Software inside the terminal has become an important design factor since the μP has taken over many of the control functions originally handled by hard-wired logic.

For terminals that require graphics capability, for example, new software techniques help minimize the memory needed by the display. Minimizing is necessary, since one bit of memory must be used for each dot on the screen.





Displays with resolutions of, say, 1024×1024 or 4096×4096 dots would require over 131,000 or 2,000,000 bytes of storage just for the display data.

One new technique, virtual bit mapping, dynamically allocates memory according to how much graphic information is to be displayed, reported Stan Davis, a project engineer at Tektronix (Beaverton, OR). Thus, on a standard alphanumeric terminal graphics capability can be integrated with functions such as forms fill-out, scrolling and text editing. Since data are stored in dynamically allocated RAM, positional changes are simple.

However, to take advantage of virtual bit mapping, powerful software must be developed to manipulate bits and allocate memory. The additional software will raise design overhead and the terminal complexity.

A typical design scenario, as suggested by Bub Bleininger, Vice President Peripherals of Microdata (Irvine, CA) will go as follows: A semiconductor manufacturer comes to a plant with an application note and samples showing how his μ P and support chips will allow the designer to build a bus-structured CRT terminal. By themselves, the chips, power supply, keyboard and display almost make a terminal.

The μ P system created will have expansion capabilities well beyond that of a teletypewriter replacement. So as soon as the basic terminal is finished, a proposal will be made to increase the terminal's capabilities so that it is "smart." And when that system is completed, yet another proposal will come forward for an "intelligent" terminal.

Within a few years Bleininger goes on, the simple terminal will have grown to almost a complete computer system. But in the rush to develop the various features, the inflexibility of the software will often be overlooked. Then additional hardware capability will mean little, Bleininger warns, if a terminal's operating system can't take advantage of it....

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As test and measuring instruments spread out, safety concerns grow

Test and measuring instruments have caused relatively few accidents and injuries, but with concern growing over liability for work-place hazards, instrument safety is getting more and more attention, engineers were told at Midcon in Chicago. Not only that, but U.S. companies interested in selling their instruments abroad, especially in Europe, had better be ready to meet safety standards.

"The instrumentation and testequipment industry has enjoyed a commendable safety record," says Donald Mader, associate managing engineer in the electrical department at Underwriters' Laboratories Inc., Melville, NY. But this record may not hold under changing conditions in the electronics industry.

Measuring instruments and testing equipment are cropping up more and more in common work places, Mader notes, which means that highly sophisticated and complex devices are being used by an ever-increasing number of employees with little or no technical training.

Richard Nute, corporate product safety engineer at Tektronix Inc., Beaverton, OR, believes that designers have a duty to design protections into equipment. "In today's world, the product must be deliberately—not incidentally—designed for safety." But there's more to it than that, according to Nute. Instrument makers are stepping up efforts not only to provide safer gear, but to protect themselves from lawsuits and government involvement in instrument design.

So far there has been no pattern to the few instrument-related accidents. That's fortunate, says Nute, because a pattern of accidents is usually the basis for legislation, such as the type leading to radiation control for microwave ov-

Andy Santoni Associate Editor



You can't change the fuse on gear equipped with this Corcom power module without first unplugging the line cord. For safety's sake, you have to pop the fuse before you change the voltage setting, too.

ens and television sets. But as more and more people have access to sophisticated electronic equipment, says Nute, the probability of a pattern of safety problems increases.

Heading off the law

Partly to forestall restrictive laws that could hamper an instrument firm's design efforts, many firms have joined with Underwriters' Labs to write a safety standard for testing and certifying instruments. Actually, manufacturers approached UL as early as five years ago, Mader recalls, and expressed interest in submitting electrical metering and measuring equipment for investigation. At that time, UL was reluctant to become involved because some of the probes, terminals and connectors used with measuring and testing equipment could not comply with UL's historically-accepted requirements for inaccessibility of parts operating at potentials capable of delivering an electric shock. In addition, instrumentation and test-equipment operators were apparently adept at modifying and repairing their equipment without any concern for risks.

Even examining instruments for safety presents problems, says Mader, who points to two special features of instrument evaluation: Power is delivered into the equipment not only from the branch circuit supplying operating electrical energy, but also from the external circuitry supplying energy through the measuring terminals.

Also, electrical test equipment is intended either to perform a nonsafety function or is relied on ultimately to indicate or control the safe performance of other equipment.

Nevertheless, UL has been accepting submittals of test equipment since 1972, relying for guidance on two existing safety standards, the International Electrotechnical Commission (IEC) Publication 348 and the American National Standards Institute (ANSI) Publication C39.5, as well as UL standards and newly developed requirements, wherever they could be applied. Meanwhile, UL began writing its own instrument-safety standard, UL 1244.

"UL and industry are reviewing the final draft of the proposed UL 1244 standard so that it can be published soon," says Mader. Once it has been published and adopted, the standard CASCADE[®] LEGAL RULED PAD

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should become effective within 18 months. UL then plans to submit it for recognition as an American National Standard, and expects the document to be submitted to the IEC as the U.S. proposal for a revised international instrument-safety standard.

Safety concerns are worldwide

Instrument safety is more than just a domestic concern, as U.S. instrument makers doing business abroad are finding out. In Europe, says Robert Wersen, president of Panel Components Corp., Berkeley, CA, "most industrial products are not yet subject to presale testing, but I find that more and more European institutions are requesting bids and quotations stating that certain components must be tested."

In the past few years, many instrument companies have seen most of their sales shift away from the U.S. and mainly toward Europe. To keep sales growing in Europe, U.S. firms will have to pay more attention to the increasing demand there for safetytesting products, Wersen insists.

"Most domestic companies are not actively pursuing what's taking place abroad," say Wersen. "They seem to prefer to ignore these sorts of things, or hope that they will go away." Worse yet, companies heeding European safety standards find the going tough.

One big reason for the rough road, Wersen points out, is that 16 European countries have their own national testing laboratories-each reserving the right to test any product before it can be sold in that country. A Certification Body based in Denmark is supposed to coordinate national testing efforts and help manufacturers gain international approvals by getting the testing results from one lab transferred to other labs. While this sometimes helps avoid the time and expense of separate submissions, the national testing lab of one country in many cases will still not accept the results obtained at another lab, Wersen says.

The IEC has published safety standards as well, but there are also national specifications to worry about—and the final authority in each country is the national document, not the IEC document, says Wersen. In addition, European safety standards may differ from U.S. and Canadian standards. Designers working on products aimed at international markets have to take all of the standards into account before they start designing, or risk expensive redesigning to comply with all applicable documents.

Wersen suggests that firms interested in complying with safety standards first make sure that someone examines a prospective design's features before real designing begins. A safety engineer, involved with the design from the start, should then develop a working knowledge of the safety requirements of each country in which the company expects to sell the product. It even helps to bring working prototypes of new products to various testing agencies to determine as early as possible what might have to be changed to bring the product into compliance, says Wersen.

Recognized parts help

Another way to simplify gaining acceptance from UL and international



Shock protection is provided on the Simpson 461 DMM's test leads by reversed connectors; the male end is recessed in the case and the leads house the insulated female end.

testing agencies is to use testing-labrecognized components in new products. When the product is undergoing safety testing, such components needn't be examined separately to ensure compliance. Many UL-recognized components and lines were on display at Midcon.

For example, a line of recognized fuseholds and switches was presented by Panel Components. The firm specializes in components that have been accepted by international safety-testing agencies.

An Alpha Wire Corp. line of more than 400 multiconductor and multipaired cables for communication and control has gained both a UL listing and a Canadian Standards Association (CSA) certification. According to the Elizabeth, NJ, company, wire and cable installed properly according to the National Electrical Code and using ULlisted cable results in an installation acceptable to the Occupational Safety and Health Administration. "Every time a user does a new installation, performs maintenance or repairs, or moves a piece of electronic equipment, he must use cable that is installed properly and that is UL-listed in order to avoid OSHA violations."

A voltage-selecting and fused connector shown by Corcom Inc., a maker of RFI power-line filters based in Chicago, is recognized under UL's components program. The connector incorporates an international-standard power-line connector, a fuseholder, an optional interference filter, and a voltage selector—a PC card that can be inserted four ways to change the wiring to the final product's power transformer primary.

The power module was developed by Hewlett-Packard Co., Palo Alto, CA. It is manufactured under license by Corcom and other firms, including The Potter Co. division of Pemcor Inc. (Wesson, MS), another Midcon exhibitor. The Corcom VS&F connector has already been incorporated into some products displayed at Midcon, including logic analyzers and transient recorders from Biomation Corp., Cupertino, CA.

The unit is designed so that the line cord blocks the sliding fuse-access door and so must be unplugged before the fuse can be removed. This prevents hazardous voltages from appearing on the fuse terminals when they are accessible.

In addition, the fuse must be removed before the transformer tapswitching card can be removed. Though this doesn't prevent mistakes, it does remind an operator that the fuse may have to be changed when the line voltage is changed.

Other products at Midcon have features aimed at protecting users from hazards. For example, a fully insulated measuring terminal and a mating connector are incorporated into the Model 461 digital multimeter from Simpson Electric Co., Elgin, IL. In this terminal design, similar to that used in the Model 60 volt-ohmmeter from Triplett Corp., Bluffton, OH, the instrument's front panel has a recessed banana plug and the test lead has a fully insulated banana jack, instead of the usual reverse assembly.

Should the test-lead pull out of the instrument, no live terminal will be exposed. According to Irv Linker, director of marketing at Simpson, the design was originally used in VOMs built for Western Electric.

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Progress is slow but steady in optical communications

It still looks like years before telephone systems will really shift from copper wires to fiber optics. But as papers at the National Telecommunications Conference in Los Angeles reveal, optical-communications technology is advancing substantially on several fronts:

• Optical sources and detectors are pacing the development of optical fibers and appear ready to be transferred from the lab to the field.

• Optical cables can now be installed by the same crews who install regular cables, and with similar equipment. They can be cut and spliced in a manhole.

• Optical-telecommunications systems now operating in such cities as Los Angeles, Chicago and London are functioning well.

Lasers and light-emitting diodes, the front end of any optical communications system, have gained ground in the recent past, according to Dr. H. Takanashi of Fujitsu Labs, Kawasaki, Japan. The latest generation of Burrustype semiconductor lasers (those with a double-heterojunction of aluminum, gallium and arsenide) have longer lifetimes (well above 10³ hours), better linearity (the wiggle in the input-output transfer curve has been straightened), and higher frequency response (flat to 2 GHz) than they used to. Lasers can now be used in the field. he says.

LEDs don't degrade as much

LEDs are improving as light-fiber optical sources, too. Specially designed for telecommunications, the devices used to degrade to their half-life within 20 hours. But by burning them in, then weeding out the ones with dark-line defects, LED half-life has zoomed to a

Dick Hackmeister Western Editor



LEDs used as optical transmitters now have a half-life of a million hours at 20 C. To achieve the long life, the devices are first burned in then checked for dark-line defects. (Graph courtesy of Fujitsu Labs, Kawasaki, Japan).

million hours at 20 C (see Fig.).

On the receiving end, noise in avalanche photodiodes (APDs) has been reduced by increasing the thickness of their avalanche region. Response time has been improved without increasing the operating voltage, and APD gain-bandwidth products are up to 300 GHz and a multiplication factor of 400.

But can optical technology cope with the real telecommunications world? It can, according to Dr. J.H. Mullins of Bell Labs.

Encouraged by the success of their experimental Atlanta fiber-optic telephone link, Bell Labs engineers installed a fiber-optics system in what must be one of the severest environments available—conduits in Chicago that not only date back to 1890, but are 30 ft underground and sloshing with water from the Chicago River a block away (see ED 11, May 24, 1977, p. 21). The Chicago experiment interconnects two Bell Company telephone-switching centers and a large commercial office building in the downtown Loop area.

"To date, the results have been excellent—they've exceeded our own hopes," Mullins reports. Twenty-four individual fibers carry all the trunk lines between the two switching centers, all the subscriber phone service for the Brunswick Building, and Bell's Picturephone video-conference facilities to boot. All communications are digital, and occur at 44.7 Mbits/s, an already-established, CCITT-approved standard data rate. A mix of LEDs and lasers is used at the front end, and avalanche photodiodes at the rear end.

The cable, designed by Bell, is modular, constructed at the factory, and fitted with optical connectors that can be connected easily in the field. Fiber ends are cut and polished at the factory, so the per-splice attenuation can be held to 0.4 dB. Over-all attenuation in the cable amounts to 5.0 dB/km,

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which is 1 dB better than Bell's Atlanta installation.

Field splicing is successful

One problem that Bell did not address in Chicago is splicing a fiber-optic cable in the field. But a fiber-optic installation between Artesia and Long Beach in southern California did.

The connection, installed by General Telephone Labs of Waltham, MA, is 5% miles long (9 km). The cable, developed by General Cable of Union, NJ, is a steel-and-aluminum protected, plastic I-beam-shaped core. On one side of the I is a laminated plastic ribbon of six optical fibers (monofilament strands, not bundles) from Corning Glass. On the other is three pairs of insulated copper wires, which help power two repeater stations along the route.

In GTE's splicing approach, a grooved, heated anvil is positioned below the two prepared fiber ends. The fibers are anchored. As the anvil is raised, the fibers enter the grooves, and the two butt ends slide gently toward each other. Once they are in contact and under a slight bias toward each other, the junction is flooded with an index-matching glue and sealed in heat-shrinkable tubing (see photo).

The cable, after being drawn through 50 manholes and spliced at 20 places, wound up with an optical loss of 6.2 dB/km—a small premium to pay for the convenience of field splicing, considering that Bell did little better (5.0 dB/km) with its elaborate factory-prepared connections.



A grooved anvil rises from below to guide the ends of optical fibers into position for splicing. Index-matching glue is applied and the junction is sheathed in heat-shrinkable tubing. This GTE splice scheme was used in a fiber-optic link between Artesia and Long Beach, in southern California.

Back in the labs, other splicing developments are "very encouraging"; according to Mark Dakss of GTE Labs. Splice losses in the quarter-dB range are common in the lab and can be achieved with a number of different techniques. But more life-test data need to be generated to know which techniques will prove significant.

Splice options that have made it out of the lab include grinding and polishing instead of scribing and cracking to prepare the fiber ends, using micromanipulators instead of preform tubes to align the ends, and indexmatching adhesion in place of electricarc fusion to bind the ends together.

Traffic control at your fingertips



Traffic-light control programs can be modified in the field with a calculator-like handheld terminal that can be programmed in easily readable alphanumerics instead of binary. The main program in the system, the Series M developed by Siemens AG of West Germany, is loaded via paper-tape or mag tape cassettes. And since the Series M equipment can communicate with central computers via a single conductor pair, it won't cost as much as older systems. Applications include fixed-time or traffic-dependent control at individual or centrally controlled crossings.

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ELECTRONIC DESIGN 2, January 18, 1978

Washington report

McDonnell Douglas tops defense-contract list

McDonnell Douglas, on the strength of its production of the F-15 fighter aircraft for the Air Force, again led all defense contractors during the past fiscal year. The firm received nearly \$2.3-billion worth of prime contracts during fiscal year 1977, which ended last Sept. 30, and \$1.3-billion of that sum came from the Air Force's Aeronautical Systems Division, which is responsible for procuring the F-15.

The figures come from a market research study prepared by Washington Communications Service, Vienna, VA. All prime contracts of \$1-million or more awarded during fiscal 1977 by the Pentagon to the top 100 defense contractors, were included in the report. Nearly \$32-million worth of contracts was recorded for the year.

McDonnell Douglas, which reached first place on the defense contractors' list for the first time in fiscal 1976, accounted for more than 7% of all prime-contract dollars awarded last year. Second place went to Boeing with \$1.4-billion, up from sixth place the year before. Rounding out the top 10, which received \$11.5-billion or nearly 36% of the total, were United Technologies Corp., Lockheed, General Electric, Grumman, Hughes, General Dynamics, Raytheon and Chrysler.

Among the predominantly electronics companies, GE received \$1.1-billion, Hughes had \$1-billion and Raytheon received \$689-million. Other electronics firms placing high were Westinghouse in 11th place with \$625-million, IBM in 15th with \$445-million, Sperry Rand in 16th with \$400-million and Honeywell in 19th with \$340-million.

Energy Dept. spends \$7-million on solar cells

Not only has the Department of Energy ordered another 190 kilowatts of solar cells from five firms at an estimated cost of nearly \$3-million, it is also spending \$4-million more to automate solar cell production in an attempt to reduce costs.

The awards are part of the department's goal to reduce costs from the present \$11 per peak watt to \$2 per peak watt by 1982 and 50 cents by 1986, in each case as measured in 1975 dollars. (When inflation is taken into account, the current \$11 figure is almost \$13.) Previous government purchases of solar cells averaged \$21 per peak watt in early 1976 and \$15 later in the year, again in 1975 dollars.

The five solar cell suppliers are Motorola Inc., Phoenix, AZ; Sensor Technology Inc., Chatsworth, CA; Solarex Corp., Rockville, MD; Solar Power Corp., Wakefield, MA; and Arco Solar, Chatsworth, CA. Estimated cost per peak watt ranges from Motorola's \$9.49 to Solarex's \$13.16 (in 1975 dollars).

Nine firms got fabrication-study contracts: Lockheed, Sunnyvale, CA; MB Associates, San Ramon, CA; Motorola, RCA, Princeton, NJ; Sensor Technology, Chatsworth, CA; Solarex; Spectrolab, Sylmar, CA; Texas Instruments, Dallas, TX; and Westinghouse, Pittsburgh. Both programs are managed jointly by the Department of Energy and NASA's Jet Propulsion Laboratory in Pasadena. Solar cell arrays already purchased in the program are being used to power an irrigation system in Nebraska, a residential-scale test system at MIT's Lincoln Laboratory, an electrically operated dust-warning sign on Interstate 10 in Arizona, and automatic weather-reporting stations in Alaska, Florida, Hawaii, Maine, New Mexico and New York. Construction has begun on a 240-kW array to provide heat and electric power to Mississippi County Community College in Blytheville, AR, and a 60-kW array for military applications at Mount Laguna, CA. For more on solar cells, see "Solar Cell Technology Advances—But Slowly" in ED No. 26, Dec. 20, 1977, p. 24.

Aerospace sales will keep going up

The aerospace industry experienced real growth in sales last year for the first time since 1974 and should do it again this year, according to the annual forecast of the Aerospace Industries Association.

Industry sales last year reaped \$32.4-billion—up \$2.4-billion from the previous year, reports AIA president Karl Harr. And he looks for \$34.9-billion worth of sales in 1978.

When these figures are translated into constant 1968 dollars, however, the growth is more modest: from \$15.2-billion in 1976 to \$15.7-billion in 1977 to \$16.2-billion in 1978. Industry sales in 1968 were \$26.4-billion.

Still, all four industry segments should grow during the coming year, Harr foresees. As measured in current dollars, defense receipts should grow from \$16.3billion to \$16.9-billion, NASA funding from \$2.8-billion to \$2.9-billion, commercial sales from \$7.6-billion to \$8.9-billion, and sales of nonaerospace products from \$5.7-billion to \$6.2-billion. And for the fourth consecutive year, exports are expected to be above \$7-billion.

Capital Capsules: Cubic Corp. of San Diego has received \$15 million from Iran to build an air-combat range that permits electronic scoring of simulated dog fights, which are used in fighter-pilot training. This air-combat-maneuvering-range instrumentation (ACMRI) will help train pilots on F-4, F-5 and F-14 aircraft. Cubic has built four ranges in the United States and is building a fifth in impact statement for its controversial Seafarer ELF communications facility to test one-way data links with submerged submarines. As expected, the Navy chose a site near Marquette, MI, which it plans to link via leased line with the present test site at Clam Lake, WI. The Navy is expected to seek development funds in the 1979 defense budget for installing a transmitter and 130 miles of buried antenna at the Michigan location. Alternate sites in Nevada and New Mexico were rejected because construction costs would have been higher....The Department of Energy's Argonne National Laboratory has discovered a new particle it is calling the diproton because it appears to have two protons and an electric charge of +2. The particle was observed during experiments with a beam of polarized protons in Argonne's Zero Gradient Synchrotron.... The Army is going ahead with its plan to transfer the headquarters staff of its Electronic Research and Development Command from Fort Monmouth, NJ, to Adelphi, **MD**, after soliciting public opinion on the subject since last summer, as required by law. However, many of the research and procurement functions will remain in New Jersey.



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CIRCLE NUMBER 37

Editorial

Protecting the members

Well, they finally got Irwin Landes. Since he graduated with honors from Harvard Law School in 1951, Landes, a fourth-termer in the New York State Legislature, has been practicing law with great success—but without benefit of license.

They got James D'Adamo, too. For more than 20 years, D'Adamo has been using naturopathy to cure or help thousands of people with a wide range of ailments. Unfortunately, naturopathy is a school of healing that's not approved by the American Medical Association. Since D'Adamo lacked the blessings of AMA-endorsed education, he never learned that many of the patients he cured were



incurable and many he helped were beyond help. So they hauled D'Adamo through the courts and made him spend thousands of dollars for legal help.

Now please don't confuse these two episodes (or hundreds of other cases of harassment of nonconformist practitioners of healing arts) with featherbedding. That malodorous practice is the effect of labor unions trying to save jobs for their members—laborers. The cases of Landes and D'Adamo stem from the American Bar Association, the lawyers' union, and the American Medical Association, the doctors' union, trying to save jobs for their members, lawyers and doctors—not laborers.

Since lawyers and doctors are higher-class folks than laborers, it stands to reason that they should have more powerful influence on law enforcement. So in most states it's unlawful for you to get legal advice or a cure for an ailment from somebody who's not a member of the club.

Now let's talk of licensing electronics engineers. That might not be a bad idea. Engineers have certainly had enough bad breaks, so it might be appealing for us to form some sort of protective club with licensing powers and great influence on the law.

Then, if anybody who's not in our club develops a significant product especially one that threatens us competitively—we'll haul him into court. Our problems will be over.

Spore Rotting

GEORGE ROSTKY Editor-in-Chief



TTTTTTT

In a world of claims and counterclaims, one thing is clear. EMM SEMI is still in the lead. Of course, we not only had a healthy head start, but we field a whole family of 4K static RAMs.

We delivered the industry's first 4K static RAM in 1975, a full year and a half before anyone else. We are now delivering 7 basic static RAM types with many versions

of each, and producing them at a greater monthly rate than our nearest competitors combined. By now we have more 4K static RAMs operating in a wider range of customer equipment than anyone else in the semiconductor memory business - from 10 Megabyte IBM add-on memory systems to hobbyist microprocessor kits.

Whatever your application, from mass storage to telecommunications, from medical electronics to toys and games, chances are there's an EMM SEMI static RAM just right for you. Please call or write today for full details - and ask about our byte oriented RAMs, too.





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LET'S PUT OUR HEADS TOGETHER.



The Facit 4540 Serial Matrix Printer has already made a name for itself with its standard 250 characters a second – all crisp, fullbodied and perfect throughout the 500 million character service life of the printhead. Versatility comes from the rare 9×9 dot matrix, and the Facit 4540 offers a genuine 100% duty cycle and entire elimination of adjustment and lubrication.

The whole secret is in the unique printhead and its microprocessor controlled impact printing mechanism.

Integration of mechanics and electronics has made Facit peripheral data products world famous. Facit 4540 extends this tradition. So let's put our heads together. To make your systems more efficient, more competitive and more in demand.



Facit 4540 Serial Matrix Printer with the unique printhead.



CIRCLE NUMBER 40

Now...LOOK at GPIB Activity:

ASCII decoded device dependent message transmitted over data bus

Attention message on the bus Attention mes-

sage mnemonic

Data byte in hexadecimal

Listen, talk or secondary address in decimal (no \$) End or identify when asserted



Service request when asserted

4 user definable lines

Remote enable when asserted

Announcing visible GPIB communications at the touch of a button: the new TEKTRONIX DF2 Display Formatter. The DF2 monitors and displays activity on the GPIB bus as disassembled instructions in familiar IEEE 488 mnemonics.

Touch another button, and information is displayed in ASCII format, with further character decode in hex, binary, or octal—all on the same display.

The DF2 Display Formatter works with our 7D01 Logic Analyzer: for the first time, you have a complete logic analysis tool that can deal specifically with GPIB activity. And that means GPIB design and integration is now faster. Simpler. And more convenient.

Designing A Controller? Use The DF2!

It's plug-to-plug compatible with GPIB controllers so you monitor commands at a glance.

Designing Talkers/Listeners? Use The DF2!

Now it's simple to make sure talkers are responding properly to the controller and listeners are receiving correct data.

Integrating GPIB Systems? Use The DF2!

You know monitoring and displaying bus events and their sequence are essential for effective integration of multi-vendor GPIB products. Now you have the essential tool: use the DF2 to analyze any specific data transaction you wish.

You'll also find the DF2 a powerful service tool. Observe GPIB bus activity to simplify troubleshooting and keep your system up and running properly.

The DF2 Display Formatter also provides displays in timing and mapping modes as well as state tables in binary, hexadecimal, or octal notation. Combined with the DF2, our 7D01 Logic Analyzer is the most comprehensive and versatile logic analysis tool available today. And because the 7D01 Logic Analyzer System is compatible with *any* TEKTRONIX 7000 Series oscilloscope, you may already own part of a Logic Analyzer package.

TEKTRONIX Logic Analyzers: we call them The Versatile Ones.

Now, with the unique and exclusive DF2 Display Formatter, they're more versatile than ever.

And GPIB is a lot more visible.

Call your local Tektronix Field Engineer for more information about the DF2. Or write Tektronix, Inc., P.O. Box 500, Delivery Station 76-260, Beaverton, Oregon 97077. In Europe, write Tektronix Limited, P.O. Box 36, St. Peter Port, Guernsey, Channel Islands.



Tektronix COMMITTED TO EXCELLENCE

TEKTRONIX Logic Analyzers: The Versatile Ones

Let 4-bit microcomputers do the simple jobs. They cost less than 8-bit units and offer almost as much processing power. The catch? They may not be as fast.

A 4-bit dedicated microcomputer offers a less expensive alternative to an 8-bit processor—and often without any performance penalty. For example, on a single chip, the MN1400 4-bit family of microcomputers includes an ALU, a ROM, a RAM, I/O ports, a counter/timer and a clock generator—for less than half the cost of an 8-bit system. However, the 4-bit units may not operate as fast as 8-bit processors, due to word-size limitations among other things.

The MN1400 family, except for the PMOS model, operates from a 5-V supply, has a $10-\mu$ s instruction cycle and uses 8-bit instruction words and 4-bit data words. Eight versions of the microcomputer are available, the MN1400, 1402, 1403, 1404, 1405, 1430, 1498 and 1499 (Fig. 1). The MN1400 and 1402 have internal ROM capacities of 1024 and 768 bytes, and on-chip RAM sizes of 64 and 32 nibbles, respectively. (A nibble is four bits, or half a byte.) The 1498 and 1499 have no internal ROM but can address 1024 or 2048 bytes, respectively. Both units have an internal RAM of 64 nibbles. The other four versions, including the lone PMOS circuit, offer various combinations of ROM and RAM.

The MN1499, designed to evaluate MN1400 system prototypes, comes in a 64-pin ceramic package so that all memory address and data lines are accessible without tying up any of the I/O ports. (The various combinations of I/O ports available on all the MN1400 devices are listed in Table 1, which also summarizes many of the other μ C features.)

Both the memory and I/O lines of any MN1400 part operate asynchronously at any speed, up to the maximum data-transfer rate of the memory circuits. The counter/timer available on the MN1400 and 1499 counts up to 256 and is software-programmable. Depending on the model, as many as 75 instructions are available to the programmer, including 18 datatransfer commands, 18 arithmetic and logic instructions, nine I/O commands, and 30 program and machine-control commands.

Since an MN1400-based microcomputer forms a complete system, to understand its operation you should examine its individual sections and know what's in each one (Fig. 2):

1. Arithmetic and logic unit: an ALU, a 4-bit accumulator, a temporary register and various flag registers.

2. Data-memory section: a RAM, and X and Y registers.

3. Program-counter section: a program counter, a mask-programmable ROM and a subroutine stack.

4. Instruction-decoder block: an instruction register and an instruction-decoding programmable-logic array.

5. Counter/timer section: an 8-bit programmable counter/timer and two input lines, SNS1 and $\overline{\text{CSLCT}}$.

6. I/O block: input ports A and B, output ports C, D and E, and three lines, SNS0, SNS1 and RST.

7. Clock generator block: an internal clock generator and an input line, OSC, that permits an external clock signal to be input.

The microcomputer works like this. . .

All mathematical and logic operations are performed by the ALU, including addition, Boolean logic, straight transfers, and incrementing. They are performed on two 4-bit binary-data words and the results are stored in the accumulator, the Y register or the temporary register, depending on the instruction.

The accumulator in the ALU block is the MN1400's primary working register. The 4-bit temporary register, TEMP, is for storing intermediate data during program execution. It is not program-addressable and is not really "seen" by the programmer.

Three flag flip-flops are used to indicate various conditions due to arithmetic or logic operations. A carry flag is set when a carry is generated and reset when a carry is not generated during an operation. The CF can be controlled either by an ALU operation or by direct software command.

A zero flag (ZF) is set whenever the result of an operation is zero, and is reset if the result is not. A program-status flag (PS) is a one-bit flag that is controlled by software, set by the SP instruction and reset by the RP command. (For a list of the instructions, see the box on software, p. 62.)

Some multifunction instructions such as LIC, LDC, STIC and STDC increment or decrement the contents of the Y register after data transfer. And the results

Bill Bottari, Product Manager, and **Terry Kobayashi,** Product Specialist, Panasonic, 1 Panasonic Way, Secaucus, NJ 07094.

Features Device			MN1400	MN1402	MN1403	MN1404	MN1405	MN1430	MN1498	MN1499
Package s	ize (DIP)		40-pin	28-pin	18-pin	16-pin	40-pin	40-pin	40-pin	64-pin
Process te	chnology	1	NMOS	NMOS	NMOS	NMOS	NMOS	PMOS	NMOS	NMOS
Number of	instruct	ions	75	57	50	48	75	75	66	75
Subroutine	e stack	Section Section	2 level	2 level	2 level	2 level	2 level	2 level	2 level	2 level
Instruction	1	On chip	1024 x 8 bits	768 x 8 bits	512 x 8 bits	512 x 8 bits	2048 x 8 bits	1024 x 8 bits	28-	-
memory si	ze	External	-	-	-	- 00	-		1024 x 8 bits	2048 x 8 bits
Data mem	ory size		64 x 4 bits	32 x 4 bits	16 x 4 bits	16 x 4 bits	128 x 4 bits	64 x 4 bits	64 x 4 bits	64 x 4 bits
On-chip co	unter/tir	unter/timer 8 bits 8 bits 8 bits		-	8 bits					
Power-on	reset circ	cuit	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Input	Para	Ilel lines	4 bit x 1	4 bit x 2	4 bit x 1	4 bit x 1	4 bit x 2	4 bit x 2	4 bit x 1	4 bit x 2
ports	Sens	se lines	2	2	1	1	2	2	1	2
Output	Para	Ilel lines	4 bit x 1	4 bit x 2	4 bit x 1	-	4 bit x 1	4 bit x 1	4 bit x 1	4 bit x 1 5 bit x 1
ports PLA lines		lines	8 bit x 1	-	100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100 - 100	-	8 bit x 1	8 bit x 1	-	(- P
D		rete lines	12 bit x 1	5 bit x 1	4 bit x 1	6 bit x 1	12 bit x 1	12 bit x 1	9 bit x 1	12 bit x 1
Supply vol	Itage		5 V	5 V	5 V	5 V	5 V	-15 V	5 V	5 V
Instruction	cycle ti	me	10 µs	10 µs	10 µs	10 µs	10 µs	15 µs	10 µs	10 µs

Table 1. Comparison of microcomputer features

of incrementing or decrementing leave a zero in the Y register, which sets the ZF flip-flop.

In the data-memory block the RAM space is divided into four files, with 16 words in each file for the 64word RAMs (Fig. 3). Two bits of the 3-bit X register select one of the four files. The value in the 4-bit Y register selects which of the 16 words will be accessed. Thus, all 64 RAM locations are addressed by the X and Y registers.

However, four locations (X = 0, Y = 0 to 3) can also be addressed directly by the LD and STD instructions. The former transfers the memory contents to the accumulator and the latter does the reverse. When the X register isn't used to specify a file, it is used to hold the three least significant bits of the instruction, when commanded to by the LX instruction. The output of the 4-bit Y register can also be output to a decoder that controls output port C, thus permitting I/O control.

The program-counter (PC) section includes an 11bit counter and two 11-bit program-stack registers. The value held in the PC addresses the mask-programmable memory, which has up to 2048 locations. Unless the instruction is JMP, CAL, RET, or a conditional branch, which alter the contents of the program counter, the contents of the PC are incremented by one every instruction cycle. The CAL command saves the PC value in the stack so that when the routine being called is finished, the computer can return via the RET command to the point in the program just after the CAL command. Up to two addresses can be stored in the subroutine stack.

A conditional branch command sets the least significant eight bits of the program counter to one of 256 memory locations on the specified page of ROM. If the instruction following the branch command is not





1. **These four pinout versions** of the MN1400 microcomputers have varying degrees of I/O capability as well as different amounts of on-chip RAM and ROM.

Software for the microcomputers

The instruction set for the MN1400 series of microcomputers consists of 75 commands, all of which are available on the MN1400 and 1499. The MN1402 can use only 57 of the instructions and the MN1498 can use 68 commands. All 75 are listed in the accompanying table, and each represents an 8-bit word, except for the branch commands, which require a second byte for the branch address.

Three addressing modes are available to the microcomputer programmer:

• Direct—the two least significant bits of the STD or LD instruction contain the exact memory address holding the data.

• Register indirect—the X and Y registers contain the address of the data.

• Immediate—the instruction contains the data in the four least significant bits.

A programming model of the processor consists of the RAM, ROM and associated status and X and Y registers. Learning how to take advantage of the directly accessible RAM addresses can aid your programming efforts since these locations can be used as high-speed buffers or temporary memory for storing intermediate results.

The first four locations of the RAM's lowest bank are directly addressable via instructions and are used for high-speed storage. The other locations are used for storing data, holding the flag bits, and storing the address vectors for ROM routines.

There are only slight differences in the software for each of the four microcomputers. The MN1402 and 1498 instruction sets are subsets, of course, of the 75 commands. The 1402s lack the counter/timer instructions and several data-movement commands since it is the most I/O limited of the four μ Cs. The 1498 lacks the instructions used to manipulate the internal ROM and several I/O commands.

For programs that use subroutines, the unconditional jump (JMP) and call (CAL) instructions can summon a subroutine by setting the contents of the program counter equal to the starting address of the desired routine. The CAL instruction, though, marks a return spot by storing the current contents of the program counter in the two-level stack. After the subroutine is executed, a return (RET) instruction will remove the return address from the stack and replace it in the program counter so that the processor will return to the normal program flow at the instruction following the CAL command.

The internal ROM is divided into 256-word pages, and branch instructions use the last eight bits in the program counter to divert program flow within the current page. If the flow must be diverted from the current ROM page, a JMP instruction must be used to set all 11 bits of the program counter.

The second second							
Mnemonic	Hex op code	Description					
MART PRO		sfer instructions					
L	0D	Load accumulator with contents					
Sec. Sec.		of memory location addressed					
LD	2a	by X and Y registers. Load accumulator with contents					
		of memory location addressed					
LI	5d	by 2-bit immediate field. Load accumulator with contents					
	ALC: NO.	of immediate field.					
LIC	0E	Load accumulator with contents					
	M. L. S.	of memory location addressed by X and Y registers and incre-					
100	0.5	by X and Y registers and incre- ment contents of Y register.					
LDC	OF	Load accumulator with contents of memory location addressed					
1111 1111	S. Salar	by X and Y registers and decre-					
ST	OA	ment contents of Y register. Store contents of accumulator					
51	00	in memory location addressed by X and Y registers.					
STD	2(1)2)	by X and Y registers.					
310	2(4+a)	Store contents of accumulator in memory location addressed					
OTIO		by 2-bit immediate field.					
STIC	OB	Store contents of accumulator in memory location addressed					
State Street	Cast of	by X and Y registers and incre-					
STDC	oc	ment contents of Y register. Store contents of accumulator					
0100	00	in memory location addressed					
Sec. Sec. 12	Sec. 1	by X and Y registers and decre- ment contents of Y register.					
LX	3d	Load X register with contents of					
LY	64	immediate field.					
LY	6d	Load Y register with contents of immediate field.					
TAX	01	Transfer contents of accumula-					
TAY	03	tor to X register. Transfer contents of accumula-					
TYA	02	tor Y register. Transfer contents of Y register					
	1993	to accumulator.					
TACU	19	Transfer contents of accumula- tor to most significant 4 bits of					
Same and		counter time.					
TACL	18	Transfer contents of accumula- tor to least significant 4 bits of					
S. Martin	- Arishi	counter/timer.					
TCAU	1B	Transfer contents of the most significant 4 bits of the counter/					
1000		timer to accumulator.					
TCAL	1A	Transfer contents of the least significant 4 bits of the counter/					
	有行的的 是	timer to accumulator					
		d logic instructions					
AND	04	The contents of the accumulator are ANDed with the contents					
	and she is	of the memory location					
ANDI	7d	addressed by X and Y registers. The contents of the accumulator					
AND	10	are logically ANDed with the					
OR	OF	contents of immediate field. The contents of the accumulator					
UR	05	are Inclusive ORed with the					
A Martin State		contents of the memory location					
XOR	06	addressed by X and Y registers. The contents of the accumulator					
		are Exclusive ORed with the					
		contents of the memory location addressed by X and Y registers.					
A	07	Add with carry the contents of					
		memory location addressed by X and Y registers to the accumu-					
Sec. With	Constant in	lator.					
AI	8d	Add without carry the contents of the immediate field to the					
Sec. 2		accumulator.					
S Shares							

Mnemonicop codeDescriptionArithmetic and logic instructions (cont d)CPL08The contents of the accumulato are complement.C09Compare contents of accumula- tor with contents of memory location addressed by X and Y registers (two's complement arithmetic). The accumulator remains unchanged.CI9dCompare contents of accumula- tor with contents of immediate field (two's complement arith metic). The accumulator re- mains unchanged.CYAdCompare contents of Y register (Exclusive-OR). The Y register memics unchanged.SL1ESL1ESL1EDCY2DDCY2DDCM2FDecrement contents of Y register ter by one.DCM2FDecrement contents of memory location addressed by X and Y registers by one.DCM2FDecrement contents of memory location addressed by X and Y registers Sy cone.DCM2FDecrement contents of memory location addressed by X and Y registers. Specific bit(s) desig- nated by 4-bit immediate field memory location addressed by X and Y registers. Specific bit(s) desig- nated by 4-bit immediate field memory location addressed by X and Y registers. Specific bit(s) desig- nated by 4-bit immediate field memory location addressed by X and Y registers. Specific bit(s) desig- nated by 4-bit immediate field memory location addressed by X and Y registers. Specific bit(s) desig- nated by 4-bit immediate field memory location, addressed by X and Y registers. Specific bit(s) desig- nated by 4-bi		Hex	
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CO12). Control instructions RC 28 Reset CF flip flop. RP 29 Reset PS flip flop. SC 2A Set CF flip flop. SP 2B Set PS flip flop. BS0 3B On SNS0 high branch to current	000	Steel St.	Y register.
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RP29Reset PS flip flop.SC2ASet CF flip flop.SP2BSet PS flip flop.BS03BOn SNS0 high branch to current			
SP2BSet PS flip flop.BS03BOn SNS0 high branch to current	RP	29	Reset PS flip flop.
BS0 3B On SNS0 high branch to current			
		the second s	On SNS0 high branch to current
		mm	page address specified by the
second byte.	Real State	The start	second byte.
		1 2 - 1 - 1 - 2	

Inemonic	Hex op code	Description	Mnemonic	Hex op code	Description			
Arith	metic and	logic instructions (cont'd)	(nstructions (cont'd)			
CPL	08	The contents of the accumulator	BS1	3D	On SF set branch to current page			
	No. of Street	are complemented. Binary 1's	Carl States	mm	address specified by the second			
С	09	complement. Compare contents of accumula-	Doot	05	byte.			
U	09	tor with contents of memory	BS01	3F mm	On SNS0 high and/or SF s branch to current page addre			
Section 19		location addressed by X and Y			specified by the second by			
		registers (two's complement	BSNO	3A	On SNS0 low branch to curre			
		arithmetic). The accumulator remains unchanged.		mm	page address specified by the			
CI	9d	Compare contents of accumula-	BSN1	3C	second byte. On SF reset branch to curre			
		tor with contents of immediate		mm	page address specified by the			
		field (two's complement arith-	FONIO		second byte.			
	Section 1	metic). The accumulator re- mains unchanged.	BSN01	3E mm	On SNS0 low and SF res			
CY	Ad	Compare contents of Y register	A REAL PROPERTY.	mm	specified by the second by			
		with contents of immediate field	BP	E9	On PS set branch to curre			
and the second		(Exclusive-OR). The Y register remains unchanged.		mm	page address specified by the			
SL	1E	Shift the contents of the accu-	BC	E5	second byte. On CF set branch to curre			
	A STAN	mulator left. The least significant	50	mm	page address specified by th			
IOV		bit becomes 0.		State State	second byte.			
ICY	2C	Increment contents of Y register by one.	BZ	E3	On ZF set branch to curre			
DCY	2D	Decrement contents of Y regis-		mm	page address specified by the second byte.			
		ter by one.	BPC	ED	On PS and/or CF set branch			
ICM	2E	Increment contents of memory		mm	current page address specific			
	Mark and	location addressed by X and Y registers by one.	BPZ	EB	by the second byte. On PS and/or ZF set branch			
DCM	2F	Decrement contents of memory	DFZ	mm	current page address specifi			
	C AN A	location addressed by X and Y			by the second byte.			
- Carlos Train	C. C. C. C. C.	registers by one. (Two's comple- ment subtraction.)	BCZ	E7	On CF and/or ZF set branch			
SM	Bd	Set bit(s) in contents of memory	and the second second	mm	current page address specifi by the second byte.			
		location addressed by X and Y	BPCZ	EF	On PS, CF and/or ZF set bran			
		registers. Specific bit(s) desig-		mm	current page address specifi			
RM	Cd	nated by 4-bit immediate field. Reset bit(s) in contents of		C. San	by the second byte.			
THIN	UU	memory location addressed by X	BNP	E8 mm	On PS reset branch to curre page address specified by the			
	No. Company	and Y register. Specific bit(s) de-	The second second		second byte.			
тв	Dd	signated by 4-bit immediate field.	BNC	E4	On CF reset branch to curre			
1 D	Du	Test bit(s) in contents of accu- mulator. Specific bit(s) desig-		mm	page address specified by the second byte.			
	Parts Alfan	nated by 4-bit immediate field.	BNZ	E2	On ZF reset branch to curre			
Se al antipe	1/0 i	nstructions		mm	page address specified by t			
INA	14	Read information present on A	DNIDO	FO	second byte.			
		input port and transfer to accu-	BNPC	EC mm	On PS and CF reset branch page address specified by the			
1110	15	mulator.	and the second	State of the	second byte.			
INB	15	Read information present on B input port and transfer to accu-	BNPZ	EA	On PS and ZF reset branch			
		mulator.		mm	current page address specifie			
OTD	12	Write and latch contents of accu-	BNCZ	E6	by the second byte. On CF and ZF reset branch			
OTHE		mulator and PS to D output port.	DIVOL	mm	current page address specifi			
OTMD	11	Write and latch contents of memory location, addressed by		Legel Rouge	by the second byte.			
		X and Y registers, and PS to D	BNPCZ	EE	On PS, CF and ZF reset brand			
and the second	A States	output port.	and the second second	mm	to current page address spec fied by the second byte.			
OTE	10	Write and latch contents of accu-	JMP	4p	Unconditional 2 k program mer			
OTIE	Fd	mulator to E output port. Write and latch contents of im-	A Real Andrews	mm	ory jump. The contents of the			
		mediate field to E output port.	Sector Sector		program counter is substitute			
RC0	16	Reset C output line addressed			with 11-bit direct address data bits 1st byte, 8 bits 2nd byte).			
SC0	17	by register.	CAL	4(8+p)	Unconditional 2 k program mer			
000	No. 14	Set C output line addressed by Y register.		mm	ory jump. The contents of the			
CCO	13	Reset C output (CO0 through			program counter is substitute			
	1.44 1.517	CO12).			with 11-bit direct address data bits 1st byte, 8 bits 2nd byte			
	Contro	l instructions		Standard Real	Return address is stored in t			
RC	28	Reset CF flip flop.	DET	10 H C 1	stack.			
RP	29	Reset PS flip flop.	RET	1F	Return from subroutine. The			
SC SP	2A 2B	Set CF flip flop. Set PS flip flop.		ANTER AND	contents of the stack is subs tuted into the program counter			
BSO	2B 3B	On SNS0 high branch to current	EC	1D	Enable counter/timer by setting			
	mm	page address specified by the			E/D flip-flop.			
al all and all	Constant and	second byte.	DC	1C	Disable counter/timer by rese			
States of the States		the second second second second second	NOP-	00	ting E/D flip-flop. No operation.			
AND THE REAL PROPERTY AND ADDRESS OF			NOP.		No operation			

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Symbols

Abbreviations

MPX	Multiplexer
L	Latches
С	Comparing circuit
S	Synchronizing circuit
G	Logical gates
ROM	Instruction Read Only Memory
PC	Program counter
STACK	Subroutine stack register
SP	Stack pointer
IR	Instruction register
INSTRUCTION PLA	Programmable instruction decode circuit
RAM	data RAM
X	X register
Y	Y register
4-12 DEC	Decoder. 4-bit data select one of 12 latches
ALU	Arithmetic logic unit
T/C	"Truth or Complement" circuit which complements or straight transfers data under program control
A	Accumulator
ТЕМР	Temporaty register. This register is not program addressable and is only used for the internal execution of program.
PS	"Program status" flag
CF	"Carry" flag
ZF	"Zero" flag
PLA	Output PLA which performs 5-bit to 8-bit data conversion
COUNTER	Programmable 8 bit counter/timer UP: Upper, most significant 4 bits of it
	LW: Lower, least significant 4 bits of it
E/D	Enable/disable counter/timer flip-flop
SF	Sense flip-flop
CLOCK GEN	Clock generator

2. **The internal architecture** of the four microcomputers looks like a complete computer system. Not only does the unit come with its RAM and ROM, but also all but one version has an 8-bit counter/timer.



3. **On-board RAM space** is divided into four banks of 16 locations. Three bits from the X register determine the bank and the four Y-register bits determine the specific word from the 16 words in the memory bank.



4. Four different types of I/O ports are available on MN1400-family microcomputers. The A and B ports are dedicated 4-bit input ports (a), the C port offers 12 individually controllable output lines (b), the D port uses a PLA to decode a 5-bit input into an 8-bit output (c), and the E port is a simple 4-bit latched output (d).

on the current page of memory, the JMP instruction is used to change pages after a branch instruction.

During normal operation, the instruction-decoder block performs most of the processor-control functions. A fetched instruction is stored in the instruction register and is then decoded by a programmable-logic array to generate the appropriate control signals.

Counter and ports give flexible control

The programmable counter/timer included on four of the eight microcomputer chips consists of two cascaded 4-bit sections. The four least significant bits, LW, and the four most significant bits, UP, can be set in sequence by data-transfer commands to shift data from the accumulator to the counter/timer. To enable the counter/timer, the E/D flip-flop of the counter/timer section must be set by using an EC instruction. To disable the unit, just reset the E/D flip-flop with a DC instruction.

When the count value in the counter/timer overflows, it sets its SF flip-flop. The state of the SF flipflop can be tested by several of the conditional branch instructions. When they detect the flag is set, they



5. By sensing switch closures on the A input port, the MN1400 microcomputer can easily control a solenoid connected to one of the port-C output lines via software.

P

rogram (Hex)					
ROM Address	Industruction Code	Label	Mnemonic	Operar	nd
000	60		LY	0	
001	14	ST	INA		
002	E301		BZ	ST	
004	92		CI	2	٦
005	E501		BC	ST	J
007	14	L1 .	INA		
008	D2		ТВ	2	
009	E307		BZ	L1	
00B	17		SCO		
000	14	L2	INA		
00D	91		CI	1	1
OOE	E20C		BNZ	L2	ì
010	14	L3	INA		-
011	D1		ТВ	1	
012	E210		BNZ	L3	
014	16		RCO		
015	4001		JMP	ST	

A←A-port

A←A-port A A 1

C-port(0)←0

Branch to L2 when A<1

Branch to L3 when ZF=0

Jump nonconditionally to ST

6. Flow-charting the solenoid control is straightforward (a). The control program (b) makes minimal use of the



processor's computational power and logic decision capability to turn the solenoid on or off.

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7. Controlling the operation of a major appliance such as a washing machine is well within the capabilities of the MN1400. It probably will even have power to spare for extras such as a clock and display controller.

Table 2. Washing machine sequence

Fully automatic operation

Water supply starts when the start switch is pushed. Processor monitors the water level. Water supply shuts off at predetermined level. Washing starts, continues for t minutes. Wash cycle ends. Water is drained from the washer. Fresh water fills the washer. Processor monitors the water level. Water supply shuts off at predetermined level. Rinse cycle for t minutes. Water is drained from the washer. Water is added to washer. Washing recommences for t minutes. Water is drained from the washer. Washer goes into spin cycle to remove major moisture. Washer shuts off.

Wash only

Water supply starts when start switch is pushed. Processor monitors the water level. Water supply shuts off at predetermined level. Washing starts, continues for t minutes. Water is drained from the washer.

Rinse only

Water is added to the washer. Water is drained as new water is added. Water is drained from the washer. Washer stops.

A step-by-step process

Developing a program for a one-chip microcomputer requires a great deal of caution: Once the chips are made, you're stuck with the algorithm built in. Constructing the program step-by-step can help minimize the chance of error. A typical sequence for program development is shown in the accompanying figure, and can be summarized by the following eight steps:

1. Organize the inputs, outputs and RAM assignments.

2. Develop the flow chart for the desired program.

3. Generate the first sequence of assembly mnemonics for the ROM.

4. Prepare a paper tape or card-deck listing of the mnemonics.

5. Assemble the source code into an object-code listing and try to eliminate any errors that appear.

6. Simulate the final system by using the paper tape or card deck to program an emulator version of the system.

7. Debug the program and prepare the final code tape or deck to be supplied to Panasonic for final ROM patterns.

8. Give production go-ahead after final evaluation of the chips. Prototypes are produced and supplied by Panasonic for final evaluation.

can divert the program flow. External events can trigger the counter by causing low-to-high transitions on the SNS1 input pin. Each transition that occurs when the CSLCT pin is held low increments the counter by one.

The I/O block of the MN1400 family devices is one of the most flexible and extensive to be found in a 4-bit device (Fig. 4). Depending upon the model, you get the following:

• Two 4-bit parallel inputs, ports A and B.

- Two sense inputs, SNS0 and SNS1.
- Two control inputs, CSLCT and RST.

• One 4-bit parallel output, port E.

• One 8-bit PLA decoded output, port D.

• Twelve individually programmable output lines, port C.

Ports A and B, noted in Fig. 4a as A10-3 and B10-3, respectively, handle dedicated input. The data from port A are transferred to the accumulator by an INA instruction and data from port B by an INB. The sense lines can be used to control program flow—conditional branches can be executed depending on the input level to the SNS0 pin. The input logic level on this line can be tested directly, without any signal preconditioning.

The SNS1 input can be used in two ways, depending on the condition of the CSLCT pin. When high, the Control Select (CSLCT) pin permits a high signal on the SNS1 pin to set the SF flip-flop. When CSLCT is low, the counter/timer is enabled and transitions on the SNS1 input toggle the counter/timer.

Port E, the dedicated 4-bit output port, lines E00



8. To develop the program that controls the washing machine, the first step is, of course, to flow-chart the basic

operation. From these flow-charts, the details of each operating mode can be worked out.

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to E03, latches the output of the accumulator when an Output to port E (OTE) instruction is executed. Data contained in an instruction can also be latched into the port by executing an Output immediate to port E (OTIE) command. The PLA decoded D output port, lines D00 to D07, accepts a 5-bit input word, latches the data, then decodes the data by using a mask-programmed PLA. The 5-bit input consists of the four bits of data from either the RAM or the accumulator and the PS flag bit. An OTD instruction transfers the accumulator contents and the PS flag into the D port latches, while an OTMD command transfers the RAM location's contents and the flag bit to the port.

Port C consists of 12 discrete-output lines, each of which can be set or reset under program control. An SCO instruction forces the output selected by the Y register to go high while an RCO instruction brings the selected line low. All 12 lines are reset if a CCO command is used.

To time the MN1400 microcomputer systems, you can use the on-chip clock or connect an external signal source to the OCS pin. Either a simple resistor/capacitor combination or a crystal can be used for the on-chip oscillator. If you use an external clock, it should operate at about 300 kHz, maximum.

A single-phase clock signal is fed into the clock circuit on the chip and broken down into three nonoverlapping phases, CP_1 , CP_2 and CP_3 . A machine cycle consists of all three signals going through their phases. An instruction cycle consists of a machine cycle plus the CP_1 phase of the clock—the instructionfetch and execute times are included. If the instruction-fetch time is omitted, the instruction will take only 10 μ s to be executed.

Get the processor on-line

Now that you know what makes your MN1400-based system tick, you can get it working. Many hardware and software tools are available to simplify program development and hardware debugging. For hardware development, the main tool is the MN1499, a microcomputer without any on-board ROM. For software development, Panasonic offers a cross-assembler (C support 1400), which runs on a Panasonic microcomputer system and an HS1400 hardware simulator.

The cross-assembler can generate object-code listings, possible-error statements, and a tape for hardware simulation. Able to run on several generalpurpose large computer systems, the Fortran-based cross-assembler is available on card, paper tape or magnetic tape.

A complete development system based on the Panafacom PFL-16A microcomputer can be used with the cross-assembler to develop your system program and directly load the hardware simulator, which contains an MN1499. This evaluation unit is functionally identical to the MN1400 except that it requires external ROM.

However, the MN1499 evaluation circuit can also



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help with program development:

• To interface to a static ROM with access times of 2 μ s or less, the address lines and the data lines of the MN1499 can be connected directly to the ROM lines.

• To simplify debugging, the MN1499 can be singlestepped through its instructions—just use the input RDY line in conjunction with the output SYNC line.

• The MN1499's PLA can be set up outside the chip because the D output port sends out the contents of the latches rather than an eight-line encoded signal.

To set up a working prototype system, you must combine the MN1499 or 1498 with a power supply, external ROM or PROM and the necessary control signals. A simple control application might require the microcomputer to control a solenoid. The circuit shown in Fig. 5 will be used and the program set so that the solenoid will be turned on only if SW_1 is closed first, then SW_2 . The solenoid will be turned off only if SW_2 is opened first and then SW_1 is opened.

The flow chart and the program for solenoid control are shown in Fig. 6. For the sequence control to function properly, the program first checks the input port to see if any of the switches are closed. If no switches are closed, the program loops back and checks the switches again. If any closed switches are detected, the program then checks to see if SW_2 is closed.

When the program checks the switch, it must make a decision—if SW_2 is closed, the program must loop back to the reading of the port and start over again; if SW_2 is open, it goes on to the next step and reads the input-port data to determine whether SW_2 's line has changed state. The program then loops around the second read step until SW_2 is closed. Once the switch is closed, the program breaks out of the loop and drives the solenoid.

Once the solenoid is powered, the program starts another read-port sequence to check the switch status and to shut off the solenoid if the switches are opened in the proper sequence. If the switches aren't opened correctly, the solenoid stays on. When the proper sequence is detected, the program goes back to step 1 and waits for the switches to be closed in the proper sequence again.

But this solenoid application is very simple, and can easily be duplicated with several TTL packages. A more complex control application is a washing machine (Fig. 7). With a microcomputer to control all the functions and the over-all operation of the machine, reliability can be improved and eventually the cost can be reduced.

The typical operating sequence of a washing machine is outlined in Table 2. Operation can be split into three modes—fully automatic, wash only, and rinse only. The flow charts for all three are shown in Fig. 8. In each case, most of the operating sequence involves direct execution of a command and requires no decision, so the economics of using a microcomputer may be highly questionable unless the microcomputer is also used to perform auxiliary jobs such as controlling a display and a clock.

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BENCH

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Technology

When one μ **P** controls another, the interface becomes the focal point. Base the boundary on an IEEE-488 general-purpose bus, and speed the bilateral flow of data.

When joining several microprocessor-based devices, you can solve the age-old problem of interfacing by using a general-purpose, interface-bus (GPIB) module. While the following design is aimed at an automated chemical-analysis experiment (Fig. 1), the underlying principles lend themselves to many other applications.

The system involves two microprocessor controllers. At the heart is a Tektronix GS 4051 graphic-display terminal—the master controller of the two microprocessors and the source of instructions for the second controller, an MCS 80 series microcomputer (μ C). The MCS 80 has two major responsibilities: Handle the "handshaking" protocol requirements of the GPIB and maintain operational control of the experiment. The microcomputer system contains all power supplies, memory boards, memory-bus backplane, and several connector slots that are free for interfacing.

Design the GPIB module to plug into and operate from any memory-bus slot of the 8080-based μ C. The interface then becomes a standard stock device available for general use.

Proms hold addresses

In the GPIB interface, address recognition is accomplished through two 256-word fusible-link PROMs, IC₁ and IC₂ in Fig 2. The inputs to the PROMs are wired to the card-edge fingers corresponding to the memory-bus address lines, A_2 through A_{15} . When previously selected address lines are asserted, the chips become qualified and their output lines go LOW.

The outputs are OR-wired together to develop the "chip-select-low" (CS) signal. Chip IC₂ is programmed with zero data in address 370 (all addressing is represented as octal numbers). All other memory locations are loaded to ONEs, causing OR-wired outputs 9 through 12 to go LOW only when address 370 appears on address lines A_8 through A_{15} .

Outputs 9 through 12 of IC₂ are wired to the chipselect inputs of IC₁, which is programmed and wired to produce a LOW output when addresses 374 to 377 are selected on address lines A_0 to A_7 . This combined configuration causes the GPIB interface to appear as





a memory device addressed at memory-page 370, locations 374 through 377.

Out of the 8080, data flow from the memory-data lines 1 through 8 via IC_3 , then onto the GPIB data bus via ICs 4 through 7. Into the 8080, data flow from the GPIB data bus via ICs 4 through 7, and onto memory-bus input lines A through J via ICs 8 and 9.

Chip IC₃ is a versatile 8255 programmable peripheral interface, designed to be used primarily with the MCS 80. Here, the 8255 supplies eight latched outputs for data (PA₀ through PA₇) and eight latched outputs for handshaking-control lines (PB₀ through PB₇). To operate in this mode, you must program the 8255 to the output mode by loading its control word with the proper information. Loading the controlword address, 377 370, with a 244 will do.

Selecting memory locations

Once peripheral-chip IC_3 is set in the output mode, you can load data or handshake information into the data registers by writing into the desired address

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2. The general-purpose interface bus (GPIB) is designed around fusible-link PROMs (ICs 1 and 2), which recognize device addresses. Data from the μ C to the bus flow through a programmable peripheral-interface chip (IC₃). Data

from the bus into the μ C flow through quad three-state receivers (ICs 4 through 7) and quad three-state multiplexers (ICs 8 and 9), which also handle the bus hand-shaking information.

location. For output data, load the memory-bus information into memory address 374 370. This places the data on outputs PA_0 through PA_7 . If the memorybus information contains handshaking data, load it into location 375 370. This places data on outputs PB_0 through PB_7 .

ICs 4 through 7 are 3441 quad three-state transceivers, permanently enabled to allow the GPIB bus to follow the outputs of the 8255 (IC₃). The receiver outputs of the 3441 chips always reflect the data states of the GPIB—a capability that becomes important when the display terminal places data on the GPIB bus. At such time, the receivers deliver the data directly to quad three-state-input multiplexers IC₈ and IC₉.

Both the data and handshaking information are placed on the inputs of ICs 8 and 9. Which byte of data gets placed onto the memory-input lines depends on the condition of address bit A_0 . If A_0 is HIGH, established by address 375 370, the handshaking information is placed on the memory-bus lines. If A_0 is LOW, the data at address 374 370 are placed on the memory-bus lines.

The 8080 instruction (input or output) determines whether data are sent to or received from the GPIB. When an output instruction appears, the 8255 chip places data on the GPIB bus. If an input instruction appears, data are read from the GPIB through ICs 8 and 9. The data and handshaking information are accessed via a flat-ribbon connector on the rear of the GPIB module. From here, the GPIB bus is cabled to the back of the computer chassis and wired to a standard GPIB 34-pin connector. Remember that the outputs of the 8255 chip are latched. They will remain on the bus lines until the MCS 80 coding clears the device. Therefore, the bus must be released after each transfer operation by loading zeroes into the 8255 data buffers.

Working out the protocol

The most important function of the 8080 code is to maintain the handshaking protocol for communication between the 8080 and the GS 4051. The coding also maintains the data-acquisition and peripheral control of the experiment. The code associated with the GPIB interface can be divided into address recognition, data input, and data output.

When idle, the MCS 80 runs in a monitor loop, looking for an Attention (ATN) signal asserted on the GPIB control lines. The signal is activated whenever the GS 4051 places an address command on the bus.



3. How the 8080 recognizes addresses: Routine $REST_1$ looks for ATN, which the 4051 terminal asserts when it supplies addresses for devices and operations.

The terminal must send out an address with every instruction to tell which device hanging on the bus is being instructed.

Once the program takes care of the initialization routines, it runs in the monitor loop, checking the GPIB for the ATN line at the routine labeled REST₁ (Fig. 3). First, the program executes a CALL ADRIN, and the eight control bits are read into the A register. If the attention line is not asserted, the program enters an EXIT routine that clears the A register, and returns to the REST₁ routine. The program remains in the idle loop until an ATN is recognized. Then it passes through the ATN check and continues on to the ADRIN coding.

Two types of addresses needed

When the GS 4051 asserts the attention line, it supplies a primary and secondary address. The former address determines which device is receiving information, the latter which operation is being requested. The IEEE-488 standard defines specific protocol operations necessary to transfer this information across the bus (Fig. 4).

Once ATN is recognized, the program enters the DATAIN routine. The 8080 sets control signal NRFD HIGH, and NDAC LOW. The GS 4051 should send DAV to the bus. The 8080 will look for DAV only for an allotted length of time. If DAV doesn't appear within this period, an error condition is assumed and the search is aborted.

When DAV is recognized, the 8080 acknowledges by setting both NRFD and NDAC LOW. The μ C then retrieves the data (primary address) from the eight data lines. As soon as the data are read, NDAC is set HIGH. The 8080 once again looks for DAV. If DAV is recognized in time, the program returns to the regular program sequence. Here, the 8080 checks the primary address to see if the 4051 is talking to the 8080 or to some other device on the bus.

If the primary address is the 8080's primary address, program flow continues to the REST_2 routine. CALL ADRIN is once again executed, this time in a search for the secondary address. If all the proper handshaking requirements are fulfilled in ADRIN, the program returns with the secondary address.

This secondary address can now be compared to all other valid available addresses. Each must be coded to perform a specific operation when called upon. When a secondary address is recognized, program flow enters the coding to execute that specific operation. If none of the secondary addresses match, an error condition is presented to signal an invalid secondary address.

Some GS 4051 commands may require parameter data to be sent after the secondary address. If so, the 4051 releases the attention line and places the data on the bus. When the 8080 is ready to accept the additional data, it calls the subroutine DATAIN. Notice that, without the ATN recognition section,





5. When the 8080 and 4051 exchange roles as the listener and talker, the handshaking control is assumed by the DATAOT routine.

DATAIN is identical to ADRIN. The handshaking requirements are exactly the same as those in the address-recovery program.

The 8080 reverses its role

Up to now, the 8080 has acted as a listening device, receiving information from the GS 4051. However, there are times when the 4051 becomes the listener and the 8080 the talker. When the 4051 commands the 8080 to return data through the GPIB, the microcomputer sends the data back via the bus with DATAOT, a routine that handles all the handshaking responsibilities (Fig. 5).

In Fig. 5, the 4051 is expected to send a READ data request to the 8080. When the coding enters the DATAOT routine, the data to be sent are contained in the A register. Since the A register participates in the handshaking routines, the data are saved in memory locations until needed.

The 8080 then monitors the control lines for a legal condition. (NRFD and NDAC cannot both be HIGH.) Once the bus is legal, the data are recovered and placed on the eight data lines. The bus is then checked for NRFD HIGH, and DAV is sent LOW. The bus is once again checked, this time for an NDAC HIGH. Recognition of a HIGH completes the transfer operation, and clears the control and data lines. The program returns to its normal coding to see if more data must be sent.

Be careful when designing the interface. The 8255 peripheral chip can produce problems in the interface operation. For example, because of the latched outputs of the buffer registers, you must make sure the registers are cleared before leaving the subroutine.

With a 3446 bus transceiver, instead of the 3441, the data and control lines assert to the LOW state whenever the control word is loaded. This occurs because the 8255 ZEROs its output registers whenever the control word is loaded. Replacing the 3446 with the 3441 variety corrects the problem.)

The GS 4051 sometimes requires special treatment by the 8080 software package—for example when the 4051 sends out a PRINT statement. Since the terminal converts the primary and secondary addresses into listen addresses, special coding is required for the 8080 to recognize them.

The PRINT statement calls for timing characteristics different from some other instructions'. When the address information is on the bus, the attention lines stay asserted for more than 800 μ s. A time-out error will occur during data recovery unless you code to wait for the ATN to go away before the program proceeds to the DATAIN routine....

Acknowledgments

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Multiplying with a microcomputer can be a drag. A simple multiplier/shifter can speed up signed 12-bit multiplications by a factor of 10 or more.

With two Am25LS14 serial/parallel multiplier chips, you can design a multiplier/shifter that will multiply much faster than 12 or 16-bit microprocessors. Multiplications that result in 24 or 32-bit numbers can take several milliseconds with a μ P, and are often followed by time-consuming double-register shifts to obtain fixed-point scaling. But a high-speed multiplier/shifter peripheral can quicken the process by more than an order of magnitude.

Although designed to work with the PACE microprocessor, the peripheral can easily be adapted to other 12 to 16-bit computers. Using fewer than 20 ICs, the circuit of Fig. 1 performs a 12-bit signed two's

Anthony Kolodzinski, Staff Electronics Engineer, Fairchild Space & Defense Systems, Syosset, NY, and David Wainland, Electronics Engineer, FAA/NAFEC, Atlantic City, NJ. Both were employed at the Naval Surface Weapons Center, Silver Spring, MD, when the article was written.





complement multiplication, and is capable of shifting the 24-bit product. The whole operation is executed under software control and takes around 100 μ s.

The multiplier/shifter uses serial multiplication, that is, the Y value is multiplied with the X value by serially shifting the Y value, one bit at a time, into the multiplier chips that hold the X value. While the Y value is being shifted into the multiplier IC, the 24-bit result gets shifted from the multiplier to the Y register, replacing the Y value. The multiplier chip calculates the product with a technique called Booth's Algorithm (see box).

The PACE timing signals (Fig. 2) control the operation over a common data/address and I/O bus, which transmits address and channel information to the decoders (Fig. 3). The data are latched when the signal BNADS occurs. A channel-decoder output CHN; and device decoder output, DEV 10 are NANDed to BIDS to provide an enable pulse that reads data into the PACE from a peripheral. A similar circuit, using the signal BODS, provides an enable pulse to output data to a peripheral. All control signals are generated by software commands.

The multiplier/shifter works in the following sequence (Fig. 4):

1. The X value is loaded into the multiplier/shifter from the computer (under software control).

2. The Y value is loaded from the computer (under software control).

3. The number of shifts, N, required to do the multiplication and then the scaling is loaded from the computer (under software control).

4. The multiplication is carried out, the result is placed into the register and the result is scaled or shifted (under internal control).

5. The result is loaded into the computer from the Y register/shifter (software controlled).

The Y register/shifter has several functions:

It temporarily stores the Y value.

• It shifts the Y value to the X register/multiplier, least significant bit first, ready for the multiplication.

• It loads the result while shifting the Y value into the X register.

It scales the result.

The main parts of the Y register/shifter are the shift registers (Am25LS22 chips) and flip-flop 1 (Fig. 5a).

Whose algorithm?

Booth's algorithm is a technique that can reduce the number of operations required for multiplications. A computer multiplies by adding the multiplicand x as often to itself as the multiplier y indicates. But strings of ZEROs in the multiplier don't require any additions—only shifting. And strings of ONEs can be expressed as $2^{s+1} - 2^{r}$.

For example, if y = 001110, then r=1 and s=3; so, $y = 2^4-2^1$. Instead of three additions, Booth's algorithm requires only one shift and one subtraction on the partial products.

Both the multiplier and the multiplicand are expressed by the algorithm in two's complement. This is possible for the multiplicand x because addition and subtraction logic are identical for unsigned, and two's-complement numbers. And for the multiplier y, the last operation is a subtraction if y ends in a string of ONEs. So two's complement is the most logical format.

Normal binary "add and shift" multiplication is

performed by summing partial products of the form

$$\pi = \sum_{i=0}^{i=n-1} y_i \times 2^i$$

where n is the number of bits in y.

If y_i is the i-th most significant bit of an n-bit multiplier, y_{n-1} is the sign bit, and X the multiplicand, then Booth's algorithm works as follows:

1. Compare y_i with y_{i-1} . If they are equal, add 0 x. 2. If $y_{i=1}$ and $y_{i-1}=0$, subtract 1 x from the partial product (i.e. add the two's complement).

3. If $y_i=0$ and $y_{i-1}=1$, add 1 x to the partial product. While you now have a rough idea how Booth's algorithm functions, you may want to dig deeper, and work a few examples. You'll find them in Advanced Micro Devices' *Digital Signal Processing Handbook* on p. 23, in "Understanding Booth's Algorithm in 2's Complement Digital Multiplication" by John R. Mick.

Flip-flop 1 produces the pulses that clock the registers for parallel loading and serial shifting. The computer uses a decoder (Fig. 3) to select the proper points for loading and unloading the multiplier/shifter. When the lines DEV 10, CHN 1 and BODS go from low to high, the output of NAND gate 1 goes from high to low, and the parallel inputs of the registers are enabled. With the positive going-edge of the next PACE CLK pulse, the output, Q, of flip-flop 1 goes high, and causes the parallel inputs (DATA/AD-DRESS bus, Fig. 5) to be loaded with the Y value.

As BODS goes low, the NAND gate-1 output becomes high, which returns the registers to serial operation, and forces the Q-output of flip-flop 1 to go low. After the X value and the shift number, N, are loaded into their proper locations, the shift pulse generator drives the preset and clear pins (P and C) of flip-flop 1.

The answer comes in chunks

The shift registers are activated by the positivegoing edge of the output pulse of flip-flop 1. When



2. The timing diagram of the PACE μ P governs the operation of the multiplier/shifter.



3. **The decoder's primary job** is to distribute the 16 data bits between the low and high-bit ICs.

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4. The various multiplier/shifter operations can be easily distinguished on a scale labeled in μ s. The shaded operations are under internal timing, and a 60- μ s delay in the software assures that they are completed.

the whole operation is completed and the 24-bit product is ready, the computer requests the answer, low-order bits first. Lines DEV 10, CHN 3, and BIDS go high, the output of NAND-gate 2 switches from high to low, three-state output is enabled, and the low order bits of the result are presented to the computer. Then DEV 10, CHN 4 and BIDS go high, and present the high-order bits to the computer.

The X register/multiplier not only stores the Xvalue, but also performs the multiplication. The major components of the X register/multiplier are the two Am25LS14 multiplier ICs (Fig. 5b). The computer decodes the parallel-input controls of the multiplier chips, namely lines DEV 10, CHN 0, and BODS. When they switch high, NAND-gate 1's output goes low and X is loaded. When the shift pulses begin, the Y value is shifted in and the answer is shifted out.

To complete the multiplication and scaling, the shift-pulse generator (Fig. 5c) produces the proper number of shift pulses. There are six major components in this part of the device. They are the programmable counters (74LS193), NAND-gates 1 and 2, and NOR-gates 1 and 2. The programmable counters store the number of shift pulses needed to complete the operation, and counts the shift pulses as they are gated. The gates enable and disable the shift pulses.

When the power is first applied, the counters are

at zero, the borrow lines are low, NOR-gate 1 output is high, and NAND gate 1 is disabled. The computer decodes the parallel input controls of the programmable counters when DEV 10, CHN 2, and BODS go high, and the 8-bit equivalent of the shift number N is loaded. When the parallel input control pin is activated, the eight bits are loaded, the borrow lines of the counters switch to high, and NOR-gate 1 output goes low, enabling NAND gate 1. At the same time BODS disables NOR gate 2.

Note the inverters marked "delay." When the parallel-input line is activated, the counter cannot operate. So, the pulses must be disabled until the input line is deactivated by removing BODS. After the parallel-input line is deactivated, the programmable counters must settle before the shift pulses appear. The propagation time of the inverters provides this delay. The shift-pulse generator then produces the pulses and when their number equals the number N, the counters reach zero, the borrow lines switch low, and NOR-gate 1's output goes high, which disables NAND gate 1.

Watch that sign

In two's complement arithmetic the multiplier's sign must be preserved during shifting operations. The Y value is a 16-bit number whose first 11 bits define the magnitude, while the last five repeat the sign. But to complete the operation, the Y value has to be shifted 25 times, so the multiplier must be extended another 8 bits to ensure a correct answer. The answer is also sign-extended during scaling.

The sign-extend control device consists of two programmable counters (74LS193), flip-flop 1 and the decoding gates (Fig. 5d). Flip-flop 1 controls the sign extended of the Y value. After eight shift pulses, output Q of flip-flop 1 goes high and removes the signextend from the Y value, which is now sign-extended to 24 bits. The sign-extend circuit for the answer consists of NAND gate 1, NOR gate 1, and NOR gate 2. When the counter reaches 25, the output of NANDgate 1 switches to low, which enables NOR gate 1. When the shift pulse goes low, the NOR gate 1 output goes high, and the sign-extend for scaling is turned on. At the same time, the counters stop counting because NOR gate 2 is disabled.

The complete 12-bit multiplier/shifter is shown in Fig. 6. This circuit can also be used for 8 and 16-bit multiplications. No modifications are necessary for 8bit numbers, but if you want to perform only 8-bit multiplications, you can eliminate some of the chips. For a 16-bit multiplier you must make some timing changes—most notably in sign-extending—and add another Am25LS22 shift register to handle the 32-bit result.

The 12-bit multiplier/shifter can also be used with other computers besides the PACE; however, vari-



5. **The major building blocks of Fig. 1** are shown in more detail. Sign-extend (a) duplicates the sign bit so it is not lost during shifting, the multiplier (b) also serves as x-

register, the shifter (c) doubles as the y-register, and the shift-pulse generator (d) produces the multiplier/shifter's internal timing pulses.



LI

2.5

out multiplication.

JSR XMLT

ations in timing signals and buses from one computer to another may require modifications. Naturally, the software will be different.

Avoid hardware problems

In constructing the multiplier circuit, take care to keep noise levels low. Each chip should be bypassed between the supply lead and ground with a 0.1- μ F ceramic capacitor. The board-supply input should have a 10- μ F tantalum bypass capacitor. Crosstalk problems can arise if the BIDS signal is coupled into other parts of the circuit. Care in layout of parts and shielding the BIDS line carefully should eliminate crosstalk.

The multiplier/shifter is interfaced to the computer through the multiply subroutine shown in Fig. 7. Before calling this subroutine, the values to be multiplied are stored in registers 0 and 1. The number of places to be shifted after the multiplication is stored in register 2. This sequence would look as follows:

LD 0,X ; load multiplier LD 1,Y ; load multiplicand mal) is added to the number of shifts already stored in register 2. The extra 25 shifts are required to carry

The second line in Fig. 7 places the address of the multiplier/shifter (80D0) in register 3. The values to be multiplied, and the shift value are then gated into their respective locations in the multiplier/shifter. After the shift value is loaded, multiplication starts.

In the multiply subroutine, the value 19₁₆ (25 deci-

load number of shifts (N = 5)

jump to multiply subroutine

While the multiplier peripheral is doing its trick, the computer executes the shift instruction SHR 2,4,0. This instruction merely serves as a time delay, to make sure that the hardware multiplier/shifter is finished before the computer continues.

After the shift instruction is completed, data from the multiplier/shifter are read into the computer by two load instructions. The 16 low-order bits are read into register 1, then the eight higher order bits are loaded into register 0, with the sign of the eighth bit extended. After the multiplication and shifting, the

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ØØØØ E9Ø	9 A	XMLT	ADD	2,T5
ØØØ1 CD9	07 A		LD	3,MULTAD
ØØØ2 D30	A Ø		ST	Ø,(3)
				(Store X)
ØØØ3 D70			ST	1,1(3)
4442 014	1 1		51	
4444 004			OT	(Store Y)
ØØØ4 DBØ	02 A		ST	2,2(3)
				(Store Shift)
ØØØ5 2EØ	8 A		SHR	2,4,Ø
				(Time Delay)
ØØØ6 C7Ø	3 A		LD	1,3(3)
				(Load Low Bits)
ØØØ7 BFØ	4 A		LSEX	0.4(3)
+++			LOLA	(Load High Bits)
4440 044	d .		DTC	(Luau High bits)
ØØØ8 8ØØ			RTS	
ØØØ9 8ØD		MULTAD:	.WORD	Ø8ØDØ
ØØØA ØØ1	9 A	T5:	.WORD	Ø19
ØØØ	Ø		.END	XMLT
Charles and the second second	(1997) 57/11			

7. A simple program, written in assembly language, has only to load the values X and Y, and retrieve the answer. During the actual multiplication, it idles.

ELECTRONIC DESIGN 2, January 18, 1978

6. **The over-all schematic of the multiplier** is arranged the same as the block diagram of Fig. 1. The bus-pin connections are given by the colored numbers.

subroutine returns control to the main program.

You can reduce the software execution time for multiply/shift combinations that require only a few shifts. Connect the borrow line from the multiply/shift counter to condition bit 15 on the PACE, and replace the "SHR 2,4,0" by "WAIT: BOC OF, WAIT," to create a variable time delay. While execution with fixed time delay takes approximately 110 μ s, the variable delay can save you five to 15 μ s—a significant amount of time if you need numerous multiplications.

The alternate operation works as follows: While the multiply/shift counter is down-counting, the borrow signal remains high. The branch-on-condition instruction (BOC) tests condition-bit 15 (Borrow line). If bit 15 remains high, the computer again executes the branch-on-condition instruction. When the counter has completed down-counting, the borrow line goes low. This time bit 15 is low, so the computer executes the next instruction in the sequence, instead of repeating branch-on-condition.

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It's time to convert to complex-BCD. However,

CPUs can work more efficiently if a hardware converter replaces software for time-data conversion.

Changing a computer's binary-time information into so-called "complex-BCD" code with a hardware converter helps eliminate repetitive software conversions by a CPU. Complex-BCD format—displaying time in days, hours, minutes and seconds—makes computer time-information readouts easy for a human operator to understand.

A binary-to-complex-BCD hardware converter not only relieves the CPU of time-conversion tasks; hardware can work several times as fast as software. And with complex-BCD format to indicate time on numeric displays, analog strip charts and computer terminals such as printers and CRTs, an operator is freed from deciphering binary-seconds time data.

Converting to complex BCD requires special binaryto-BCD logic, since complex BCD differs from conventional (8421) BCD code. The term "complex" means that data represented by the code is a combination of units which are not all direct multiples of a given numeric base. Two numeric bases—base 10 and base 6—must be used to represent complex-BCD information. Hardware must be programmed for conversion. For time signals, two types of algorithms, base-10 and base-6, are used in a converter to change binary time to complex BCD.

Conversions get you on the right base

To begin the binary-to-complex-BCD conversion process, you first must change binary seconds to BCD units of seconds using a binary-to-BCD conversion algorithm. Since the least significant complex-BCD digit, units of seconds, can have any value from 0 to 9, a binary-BCD algorithm handles the conversion. The algorithm applies to units of minutes, which also has a 0 to 9 range of values. And with the algorithm, called a base-10 or modulo-10 conversion, you get a step-by-step routine for converting binary to BCD. The procedure is as follows:

When going from binary to BCD, first examine the three most significant binary bits. If they, as a separate 3-bit number, have a sum greater than or

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1. A modulo-10 conversion algorithm changes binary numbers to BCD code. Four-bit BCD decades are formed by shifting the binary number to the left, one bit at a time. Binary three (0011) is added to each 4-bit BCD number with a value of 5 (0101) or greater.



2. Combining modulo-10 and modulo-6 conversion algorithms lets you convert binary seconds to complex-BCD minutes and seconds. Decades (mod-10) are treated as in Fig. 1, but hexades (mod-6) must be examined separately, as each 3-bit group is formed.

equal to five (101), add three (011) and shift one bit to the left. If the sum is less than five, shift left without adding three. After each shift, examine the BCD number being formed—only now, one 4-bit decade at a time—and add three to each decade with a value of five (0101) or greater. Then shift again. Continue this iterative process until the last, or least significant, binary bit is shifted into the least significant BCD position. At this point the BCD decades contain the correct BCD number. An example using the procedure is given in Fig. 1 for a 9-bit binary number.^{1,2}

While units of seconds are converted with a base-10 algorithm, tens of seconds require a base-6 conversion because the number five for tens of seconds cannot be exceeded. Sixty seconds must be entered as one minute to the next higher decade. And here, it's convenient to use base-10 and base-6 algorithms simultaneously to change binary seconds to complex-BCD tens and units of seconds.

To create a complex-BCD number, you must examine not only each 4-bit decade being formed, but each 3-bit hexade (base-6) number being formed at the same time. The 4-bit decade is handled as a base-10 conversion like the example in Fig. 1.

For a hexade, each 3-bit number having a value of three (011) or greater must have one (001) added to it before shifting. If the value is less than three, shift without adding one. Shifting and adding (where necessary) continues until the last or least significant binary bit is shifted into the least significant complex-BCD position. At this point, the BCD decades and hexades contain the correct complex-BCD number. An example of this combined procedure is given in Fig. 2 for a 9-bit binary number.

To build a complex-BCD time converter, first program hardware to perform the conversion algorithms. And with a single type of IC, you can construct a converter for days, hours, minutes and seconds.

One ROM goes a long way

A 16-word by 4-bit read-only memory (ROM) is the only IC type needed in the design, but 90 of them are required for an entire converter. Both a modulo-10 and

		Truth Table I IC Module — MC 4001P											Table II Module					
			INPU	IT	OU	TPUT						NPU	T	00	TPUT		184.5	State of the second second
	D	C	В	Α	Q7	Q6	Q5	Q4		D	C	В	Α	Q7	Q6	Q5	Q4	
No Conversion	0 0 0 0	0 0 0 0	0 0 1 1	0 1 0 1	0 0 0 0	0 0 0 0	0 0 1 1	0 1 0 1	* *	0 0	0		0 1	0 0	0 0		01	No Conversion
	0	_ 1	_ 0	0	0	1	0	0	*	0	1		0	0	1		0	
Modulo-10 Conversion	0 0 0 1 1	1 1 1 0 0	0 1 1 0 0	1 0 1 0 1	1 1 1 1	0 0 0 0 1	0 0 1 1 0	0 1 0 1 0	* *	0 1 1	1 0 0		1 0 1	1 1 1	0 0 1		0 1 0	Modulo-6 Conversion
Don't care states (impossible inputs)	1 1 1 1 1 1	0 0 1 1 1 1	1 1 0 0 1 1	0 1 0 1 0 1	1 1 1 1 1 0	0 0 1 1 0 1	0 0 1 1 1 0	0 1 0 1 1 0		Ρ	erma Grou "O'	nd	t		n	term ot		

Truth tables for modulo-10 and modulo-6 conversions are programmed into one 16-word ROM. Every ROM in a binary to complex-BCD converter can be programmed with these tables.



4. A complete binary to complex-BCD converter changes binary seconds into a days, hours, minutes and seconds

time code. Only one IC type, a 16-word \times 4-bit ROM, is used in the circuit.

a modulo-6 conversion algorithm can be programmed into a single ROM (see the truth table of Fig. 3 for an MC4001P ROM). Note that the six words not required for modulo-10 conversion are used to hold the modulo-6 conversion program. For modulo-6 conversion, a permanent low (0 V) is applied to the B input, and the Q_5 output is not used since modulo-6 numbers are only 3 bits long.

In an all-ROM complex-BCD converter (Fig. 4), conversion speed depends only on propagation delays through the ICs. Since each ROM has a delay time of 50 ns, and the longest delay path is through 22 ROMs, a conversion can be completed in 1100 ns. And 1100 ns is faster than one machine-instruction cycle of most computers. Conversion is not only fast, but easy to test also, because the circuit is entirely static (no clock). If you put a known binary-time count on the input lines, the complex-BCD outputs can be easily checked for the correct high levels (+5 V) with either indicator lights or a voltmeter.

Converting hours to days is not as easy as converting to seconds and minutes. Ordinarily, two digits for hours must be checked, 10¹ and 10⁰, which would require a modulo-24 algorithm. However, a modulo-6 conversion can replace modulo-24 if you consider every six hours one-quarter of a day. A quarter of a day, when doubled, becomes a half-day, etc. So the circuit uses modulo-6 until the last two levels of conversion, then switches to modulo-10 to present the remaining number of hours—not as fractions of a day, but as a two-digit (00 to 23) representation of hours. The most significant digit is a two-line terminal stage that needs no conversion module. The least significant digit is generated by a modulo-10 algorithm in the last two levels of conversion.

Days are converted by a standard modulo-10 algorithm, but there is no provision for converting days to years.

If time data are to be communicated between a computer and its I/O terminals, complex-BCD signals from a terminal must be converted to binary for input to the CPU. And to change complex BCD to binary, you'll need another type of hardware converter, but it's also a static circuit that requires only a single IC type to build a complete converter.

Anyway you look, it all adds up

A complex-BCD-to-binary converter generates serial binary bits by adding selected complex-BCD bits. The entire conversion requires only add operations, so you can use a single type of IC, an SN 7483 4-bit full adder, to build a complete converter. You'll need 31 adders to do the job, but there's no programming

Table. Binary/complex-BCD equivalents

20.00		Decimal			Decimal	Octal	
Signal	Days	Hours	Minutes	Seconds	Seconds	Seconds	
S1 S2 S4	00	00	00	00 1 2 4	000 000 000 1 2 4	000 000 000 1 2 4	23 0 000 000 000 000 000 000 000 000 1 10 100
S8 S10 S20 S40				8 10 20 40	8 10 20 40	10 12 24 50	1 000 1 010 10 100 101 000
M1 M2 M4 M8 M10			1 2 4 8 10	0 0 0 0	60 120 240 480 600	74 170 360 740 1 130	111 100 1 111 000 11 110 000 111 100 000 1 001 011 000
M10 M20 M40 H1 H2 H4		1 2 4	20 40 0 0 0	0 0 0 0 0	1 200 2 400 3 600 7 200 14 400	2 260 4 540 7 020 16 040 34 100	10 010 110 000 100 101 100 000 111 000 010 000 1 110 000 100 000 111 000 010 000 111 100 001 000 000
H8 H10 H20 D1 D2 D4	1 2 4	8 10 20 0 0 0	0 0 0 0 0	0 0 0 0 0	28 800 36 000 72 000 86 400 172 800 345 600	70 200 106 240 214 500 250 600 521 400 1 243 000	$\begin{array}{cccccccccccccccccccccccccccccccccccc$
D8 D10 D20 D40 D80 D100	8 10 20 40 80 100	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0	$\begin{array}{c} 691 \ 200 \\ 864 \ 000 \\ 1 \ 728 \ 000 \\ 3 \ 456 \ 000 \\ 6 \ 912 \ 000 \\ 8 \ 640 \ 000 \end{array}$	$\begin{array}{cccccccccccccccccccccccccccccccccccc$	10 101 000 110 000 000 000 11 010 010 111 100 000 0
D200	200	0	0	Ő	17 280 000	101 726 000	1 000 001 111 010 110 000 000 000



6. A full adder is the only IC type needed to build a complex-BCD-to-binary converter. Since the design isn't clocked, testing is easy.

90

Binary weight	Signals to be added with this binary weight							
20	S1							
21	S10	+	S2					
22	M1	+	S20	+	S 4			
2 ³	M10 S10	+++	M2 S8	+	M1	+	S40	+
24	H1 M2	+++	M20 M1	+++	M10 S20	+	M4	+
25	H10 M4	+++	H2 M2	+++	M20 M1	++++	M8 S40	+
26	H20 M8	+++	H4 M4	+++	M40 M2	+	M10	+
27	D1 M8	++++	H10 M4	+	H8	+	M20	+
28	D10 M40	+++	D2 M8	+	D1	+	H20	+
2 ⁹	D100 D2	+++	D20 H1	+++	D10 M10	+	D4	+
2 ¹⁰	D200 D10 H2	+++++	D100 D8 H1	+ + +	D40 D4 M20	+++	D20 H10	+++
211	D200 D10 H4	++++++	D80 D8 H2	++++++	D40 H20 H1	+ + +	D20 H10 M40	+++
212	D100 D1 H2	+++	D80 H20	+++	D40 H8	+++	D20 H4	++++
2 ¹³	D200 D2	++	D80 H8	++++	D40 H4	+	D10	+
214	D100 D1	+++	D80 H8	+	D20	+	D4	
215	D200 D2	+++	D100 H10	+	D40	+	D8	+
216	D200 D4	+++	D100 D1	+++	D80 H20	+	D10	+.
217	D200 D2	+	D100	+	D20	+	D8	+
218	D200	+	D40	+	D10	+	D4	
219	D80	+	D20	+	D10	+	D8	
220	D40	+	D20					
221	D80	+	D40					
222	D80							
223	D100							
224	D200							

5. **Complex-BCD components of binary numbers** are found by reading down the binary seconds columns in Table 1. Summing the correct complex-BCD signals with full adders generates all 24 binary-seconds bits.

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involved in the conversion.

The complex-BCD components of each binary number are found by constructing a chart (see Table) of binary and complex-BCD equivalents. Reading a binary-seconds column vertically tells you which complex-BCD components, when added together, form a particular binary number. Say you want to find the components of the 2³ binary bit. Locate all ones in the table, by reading the 2³ column from top to bottom. Project the ones across to the left side of the table and read out the complex-BCD components: S₈, S₁₀, S_{40} , M_1 , M_2 and M_{10} . These signals must be summed by the hardware to produce a binary 2³. Since all 24 binary digits in the table have an equivalent sum, a listing is easily made by reading down each column, and picking out the signals to represent the binary numbers. Fig. 5 shows the result of that process, a list of all complex-BCD components that must be added to generate the binary time bits.

Adders, adders everywhere

To build a complete complex-BCD-to-binary converter (Fig. 6), interconnect 31 adders according to the add operations dictated by Fig. 5. For addition, the order of operations doesn't matter, so signals to be added can be intermixed as long as they're added with the proper binary weighting. For clarity, in Fig. 6 signal abbreviations of complex-BCD inputs are used, to eliminate crossing of lines on the schematic.

When you interconnect adders, be sure that carry bits are always a carry-in to the next more significant bit. And to avoid false values from being generated, ground unused carry-in and adder input pins. Note that the least significant binary bit, 2°, doesn't need an adder because no sums are involved, and no carries will be produced.

Buffering at the adder inputs is not required since complex-BCD output drivers can fan out to eight adder inputs. And testing a converter is similar to testing a binary to complex-BCD type, since they're both static and require only a known input to check for the correct outputs. Again, indicator lights or a voltmeter are all that are needed for test equipment.

As with a binary-to-complex-BCD converter, conversion speed is limited only by propagation delays through the ICs. The longest path is through 14 ICs, each with a 50-ns delay. So maximum delay is 700 ns. This is 400 ns faster than a binary to complex-BCD converter, and well within one instruction time of most computers. Conversion time can be made shorter, either by using faster ICs or full adders having lookahead-carry logic.

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CIRCLE NUMBER 49

Synchronizing giant generators

by hand can create expensive fireworks. But a mini closes the large circuit breakers with precision.

Before a power generator can be connected to a grid bus—usually in response to peak demand—it must be synchronized carefully. Otherwise, the surge of power will unleash potentially destructive forces in the generator.¹ And the larger the generator, the more precise the match must be.

For example, the new 600-MW generators at the Grand Coulee Dam can tolerate a phase error of only 2 degrees. Because a skilled operator typically achieves no better than a 5-degree match, large generators must be controlled automatically.

The Grand Coulee generators will be monitored and controlled by a distributed processing system whose smart remote terminal units limit-check data and control generator load and voltage. With only a small increase in the host minicomputer's memory, and some additional hardware, the control system can also sequence start-up and shut-down of individual generators. With conventional synchronizers, the cost of individual control would be prohibitive.

Field tests on a 125-MW generator² provide the design base for such a control system: When the circuit breaker connecting the incoming bus to the running bus is closed, say, with a 15-degree phase-angle mismatch, a peak power surge of 225 MW (1.8 times the generator's rated output) creates a loud bang that rocks the whole power plant. A frequency mismatch of 0.25 Hz causes a 20-MW surge, and a voltage mismatch of 1% sucks in 9 MVA of reactive power. As a result of these tests, the Bureau of Reclamation has established the following synchronization criteria, at the point of breaker closure:

- Maximum phase error—2°.
- Max frequency mismatch-0.1 Hz.
- Max voltage deviation—0.1 %.

David controls Goliath

The synchronization control loop of the Grand Coulee control system (Fig. 1) uses step-down transformers to couple the running-bus and incoming-bus wave to the sync-module input. When commanded by

William R. Berger, Member of the Technical Staff, Communications Switching Systems Division, Rockwell International, 3330 Miraloma Avenue, Anaheim, CA 92803



1. **The synchronizer compares voltages** from two buses, and creates three outputs. One controls the generator's speed, one its voltage, and a third activates the circuit breaker, when phase and voltage are matched.

the CPU, the sync module digitizes the two waveforms and, using direct-memory access, fills a pair of image buffers. The CPU is now available to handle tasks of the remote-terminal unit.

When interrupted by the sync module, the CPU software analyzes the fresh data in the buffers and generates error signals proportional to waveform differences. Control algorithms in the software use these error signals to modify generator speed and voltage through digital-to-analog converters that drive the generator control ports. When the error signals have been reduced to prescribed limits and maintained for defined periods, the software sends a command to close the circuit breaker, which allows for the closing delay of the breaker.

Software makes the match

The control algorithms are known as proportionalintegral-derivative. Each control output is formed by summing weighted values consisting of a term proportional to the variable, a term corresponding to the integral of the variable, and one representing the derivative of the variable. The weighting coefficients, K_{xy} , are adjusted to match the response of the gener-

statistics and statistics

These responses and the second second second at a response response and the second se

ator that's being synchronized (some of the coefficients are zero).

The voltage-adjust equation requires only the proportional and integral terms as follows:

 $V_{ADJ} = K_{PV} V_{R} + \Sigma K_{IV} V_{R} + V_{NL}$ (1) where

 V_{R} = relative voltage, or the difference between incoming and running-bus amplitudes.

 V_{NL} = voltage no-load set point.

The terms $\Sigma K_{IV}V_R$ and V_{NL} represent the computer equivalent of the voltage integral, with the voltage no-load set point as the initial condition.

Similarly, speed-adjust output is formed as follows: $S_{ADJ} = K_{P\dot{\theta}} \dot{\Theta}_{R} + K_{I\dot{\theta}} \dot{\Theta}_{R} + S_{NL} + K_{d\dot{\theta}} \ddot{\Theta}_{R}$ (2) where

 $\dot{\Theta}_{\rm R}$ = relative angular velocity

 $\ddot{\Theta}_{R}$ = relative angular acceleration

 S_{NL} = speed no-load set point

Phase control is achieved by varying the speedcontrol output. First the speeds are matched, then the generator speed is allowed to slip slightly to bring the waveforms into phase correspondence. The final value of the described speed-adjust output forms the initial condition for the phase-control integral. As a result, the phase-control output is another speed control: $S_{ADJ} = K_{P\theta} \Theta_R + \Sigma K_{I\theta} \Theta_R + S_{ADJ}(s,f) + K_{d\theta} \dot{\Theta}_R$ where (3)

 $\Theta_{\rm R}$ = relative phase angle

 $S_{ADJ}(s,f) =$ initial condition-final condition from speed-control Eq. 2.

Caution-waveform crossing

The four derived quantities in the control equations, V_{R} , Θ_{R} , $\dot{\Theta}_{R}$, and $\ddot{\Theta}_{R}$ are obtained by analyzing the waveforms stored in the data buffers for axis crossings (Fig. 2). The time between zero crossings is inversely proportional to angular velocity $\dot{\Theta}$. The difference between $\dot{\Theta}$ values, observed on the same channel in subsequent passes, is directly proportional to angular acceleration $\ddot{\Theta}$ over the repetition period. The peak amplitude is halfway between X_1 and X_2 (Fig. 3). By locating both the positive and negative peaks, the software can compensate for any dc offset and correct the resulting error in Θ .

The relative quantities required by the three control equations are simply the differences in corresponding



2. Axis crossings are the key to determining the phase difference between the generator and the grid.

values of the incoming bus and running bus—e.g. the relative phase angle Θ_R is proportional to the time between positive (or negative) zero crossings in the two image buffers.

Each of the derived quantities (Eqs. 1 to 3) contains a finite uncertainty whose magnitude can be expressed as a function of the uncertainty in the axis-crossing time. Analysis reveals that Θ_R shows the highest sensitivity to axis crossing errors. The uncertainty in the relative phase angle is equal to $\pm 2 \omega n$, where ω is the angular velocity in rad/s of both waveforms at synchronization, and n is the uncertainty in the axis-crossing time, in seconds.

At an angular velocity of 377 rad/s (60 Hz), and a maximum phase uncertainty of 0.1°, the maximum axis-crossing uncertainty is $\pm 2.5 \ \mu s$.

Actual axis-crossing time is determined by a software routine that interpolates between two points on opposite sides of the axis. But these two points aren't simply two measured values—each is the result of averaging three samples immediately before and immediately after the sign change (Fig. 3).

With this technique, noise effects are minimized in the vicinity of the axis crossing. Because the uncertainty in the axis-crossing point is proportional to the uncertainty in the sampled voltage, and inversely proportional to the velocity of the wave at the axis crossing, a limit of $\pm 2.5 \,\mu$ s requires a voltage uncertainty of less than ± 134 mV—one part in 2180 when referred to the input waveform. For this resolution, a 12-bit analog-to-digital converter is needed because an 11-bit converter's error of one part in 2048 (=2¹¹) is not quite good enough.

Timing is everything

The averaging technique used for locating an axis crossing requires that seven samples be taken near the axis, over an interval in which the sine wave appears linear—i.e., the sine function must not deviate from its maximum slope by more than half the least significant bit (LSB). This requirement can be expressed as

 $A\omega t - A \sin \omega t \le 1/2$ LSB.

By representing $\sin \omega t$ as a power series, this equation can be solved for t, with the following result:

$$T = \sqrt[3]{\frac{3LSB}{A\omega^3}}$$

Since the waveform is symmetric about the axis, the total period of linearity is twice the calculated value. For seven samples to be taken in this linear interval, the sample period must be 2T/7, or 90 μ s.

The correction signals (Eqs. 1 to 3) all stem from differences between the two bus inputs, and errors common to both channels are self-canceling. By using one a/d converter to digitize both channels, conversion errors tend to disappear. However, two conversions must then be made during each 90 μ s sample period, and the available conversion time is below 45 μ s.

The most suitable a/d converters use a successive approximation technique, which requires that the input not change by more than $\pm 1/2$ LSB during conversion. At the maximum velocity of the given inputs, this means a 600-ns conversion period.

Because conversion times under 1 ms are expensive, a sample/hold network can be installed ahead of the converter. Again, a single network would minimize errors associated with the sample/hold network, but acquisition time would be doubled, and the software would have to correct the derived quantities for time skew. The best solution is to use one sample/hold network for each input, and then multiplex the network's outputs before conversion, even though the differential errors are higher. Allowing time for sample/hold action, multiplexer settling, and two memory access cycles leaves the a/d converter with about 25 μ s per conversion.

Missed opportunities count

When designing the software for the synchronizer (Fig. 4), two additional problems must be considered. Since each new "image" is sampled at program request, the software might miss a sampling opportunity. To maintain an accurate time base even when this happens, the hardware keeps track of the number of missed opportunities, and stores it in a buffer location at the end of the next image sample.



3. The accuracy of axis crossings is greatly improved by averaging and interpolating test points.

As part of the final closing sequence, the software calculates the time remaining until the close command. When this period is less than the time required to process one more image pair, the program stops sampling and places the sync module in the timing mode. A number representing the time until close command is stored in the sync module. This number forms the initial condition for a precision interval timer. Once the specified time has elapsed, the sync module generates an interrupt that causes the program to transmit the close command.

Another problem stems from the circuit breaker's closing delays. A short but significant time elapses between the command to close and the actual circuit breaker closure. Since the delay is repeatable for each breaker, the software can compensate for it. Depending on the closing delay time, either of two methods of circuit-breaker closing can be used. If the relative angular velocity is small enough, the circuit breaker is commanded to close when Θ_R conforms to the synchronizing criteria. In this case the value of $\theta_{\rm R}$ is so low that the angle can't change significantly during the closing delay. For larger values of $\dot{\theta}_{R}$, the software must calculate the time remaining until the waveforms coincide. All closing delays are subtracted from this time to determine when the closing command must be given.

For synchronizing generators at Grand Coulee Dam, Rockwell International's Communications Switching Division has chosen Interdata's 7/16 minicomputers with 48 kbytes of core. Features of this model include 1 μ s cycle time, automatic restart circuitry in case of power failure, signed multiply/divide hardware, linesynchronized clock, and binary front-panel display. Loader storage is provided for down-loading the system from the master station, and a programmable asynchronous/synchronous line adapter (PASLA) is available for interfacing to a portable programming unit like the HP2640.



4. As the flow chart shows, the synchronizer not only controls the generator's speed and voltage, but also watches for abnormal waveforms and sounds an alarm.

Synchronizer hardware is mounted on a single PC card that plugs into the minicomputer's backplane. Control logic is on the main card while the analog circuits, which consist of conditioning amplifiers, multiplexer, sample/hold networks, and the a/d converter, are mounted on a small "piggyback" board that plugs into the main card. Power for the analog circuitry is generated locally by a dc/dc converter.

The minicomputer-controlled synchronizer has been tested by the Bureau of Reclamation. Using an analog simulator to model generator response during a wide range of conditions, the system has repeatedly synchronized the generator within the limits set by the Bureau. The synchronizers should be working with the big generators by the end of 1978.

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* 8 *

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Compute delay times of ALU adders. Knowing

they're fast is not good enough—it takes a trip through an adder's delay path to calculate its actual speed.

To design a fast arithmetic logic unit (ALU) you've got to make certain that delay through the adder components does not exceed that allowed by your system's speed requirements. Since adders come in two basic types—ripple-carry and lookahead-carry it's important to be able to assign a speed or delay time number to each one. Although a lookahead-carry design is naturally faster than ripple-carry, you won't know how much faster until you've calculated delays through the circuit components.

Fast ALU adders can be built with arithmetic functional blocks,¹ allowing you to design a 16-bit adder which then serves as a system block. And arithmetic operations can be easily extended to 32 and 64-bit words by interconnecting the 16-bit system blocks. But you must first trace the delay paths of 16-bit ripple-carry and lookahead-carry schemes to see how their speed performance fits your ALU specs.

Short delay path means high speed

High-speed arithmetic results when a 16-bit adder senses anticipated carries from each of its individual

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4-bit adders. This scheme, a lookahead-carry adder (Fig. 1), is faster than ripple-carry, but an additional component, a carry-lookahead generator, such as the Am2902, is needed to achieve the higher speed. To find the actual delay time of a lookahead-carry adder, trace the path delay through its components.

The data path, from input to output, determines the time delay of a bit progressing through an adder. In Fig. 1, this path begins at the least significant 4-bit adder, goes through the carry-lookahead generator, and ends at the most significant 4-bit adder.

Because Am25LS381 adders can generate anticipated carries, carry bits are sent out to the carry-lookahead generator without having to ripple through all 16 adders in the block. Since delay through an Am2902 carry-lookahead generator is only 10 ns (Fig. 2), over-all delay of a lookahead-carry scheme is small. The longest delay occurs in a 4-bit adder (Am25LS381 or Am25LS2517) from operand inputs, A_i or B_i , to sum outputs, F_i . This delay is listed in Fig. 2 as 27 ns, and if a carry-in, C_n , from a less significant adder takes place, an additional 23-ns delay is introduced before final sum bits are available. However, as can be seen in Fig. 2, the total 16-bit delay of a lookahead adder scheme is only 60 ns.

In this lookahead scheme, delay to the most significant adder or to the next less significant 4-bit adder



1. A lookahead-carry adder's high-speed performance comes from using an Am2902 carry-lookahead generator.

Delay is reduced because a 2902 can sense anticipated carries across the entire 16-bit block.

Path		Output		
	Fi	C _{n+4}	OVR	
Ai or Bi to G or P	27	27	27	ns
G_i or P_i to C_{i+i} (Am2902)	10	10	10	ns
C _n to F _i	23		-	ns
C_n to C_{n+4} or OVR		22	22	ns

2. Since path delay in a lookahead scheme is short, add operations take only 60 ns for a 16-bit word. But 12 and 16-bit adders both have 60-ns delay times since their combinatorial delay paths are the same.

is the same, so a 12-bit and 16-bit adder have the same delay time. This is because the same types of combinatorial delays are involved in each case.

The longest delay for a lookahead adder comes when a 16-bit block is commanded to a particular operating mode via its function-select inputs (S_i). Am25LS381 and Am25LS2517 functional blocks perform eight different arithmetic/logic operations and a 21-ns delay occurs (Fig. 3) if there is a change in operating mode. Adding this delay to the 27 ns previously found for the block results in a total of 48 ns delay for an

Select-input delay for 16-bit adder (+5 V and 25 C maximum delays)

Path	Output			Units	
	Fi	C _{n+4}	OVR		
S; to G or P	47	47	47	ns	
G'_i or P_i to C_{i+i} (Am2902)	10	10	10	ns	
C _n to F _i	24		_	ns	
C_n to C_{n+4} or OVR	-	22	22	ns	
Total	01	70	70		
16-bit delay	81	79	79	ns	

3. Additional time is needed to output data if an adder's operating mode is changed. The additional time occurs only in a 4-bit adder, because of propagation delays in the function select circuits of an adder.

adder. The additional 21 ns must be reflected at the sum outputs, so worst-case add time becomes 60 + 21 = 81 ns. Note, however, that all delay times in Fig. 2 are at 5 V dc and 25 C, which obviously aren't worst-case voltage and temperature conditions.

Serial delay path means low speed

To calculate delay time for a ripple-carry scheme, trace its delay path almost as you would the path of a lookahead adder. By computing delay for a 16-bit



4. Serial operation makes a ripple-carry scheme slower than lookahead types. Carries from the least significant to the most significant adder must travel a long path, building up delay time in each block.

ELECTRONIC DESIGN 2, January 18, 1978

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Data-path delay of 16-bit ripple-carry adder (+5 V and +25 C maximum delays)

Path	0	Output			
	Fi	C _{n+4}	OVR		
A _i or B _i to C _{n+4}	36	36	36	ns	
C_n to C_{n+4}	22	22	22	ns	
C_n to C_{n+4} C_n to C_{n+4}	22	22	22	ns	
C _n to F _i	23		-	ns	
C_n to C_{n+4} or OVR		22	22	ns	
Total		0		13.3	
16-bit delay	103	102	102	ns	

5. Although a ripple-carry adder is slower than a lookahead, its 103-ns delay time for 16 bits is still fast by most standards.

ripple-carry adder, you can compare it directly with a 16-bit lookahead scheme for speed.

A 16-bit ripple-carry adder is built with 4-bit functional blocks having carry-output pins available. In Fig. 4, each 4-bit adder is an Am25LS2517, which replaces Am25LS381s when a carry output, C_{n+4} , is required. Notice that no lookahead-carry generator is used, and all carry bits progress serially through 16 adders. Each C_{n+4} carry output is connected to the succeeding adder's C_n , carry input.

To compute delay time of a 16-bit ripple-carry scheme:

1. Select the longest combinatorial delay in the least significant bit adder; this path usually runs from operand inputs A_i or B_i to carry output C_{n+4} .

2. Add the carry input to carry output delay as many times as necessary (twice for this 16-bit adder) to represent each intermediate 4-bit adder.

3. Add the delay from the final or most significant bit adder's carry input to sum output.

This computation is not the worst-case delay since mode changes are not included.

A delay chart (Fig. 5) shows the contribution of each adder. Here, as in a lookahead adder, the longest delay, 36 ns, is in a 4-bit adder, from operand inputs to sum outputs. Carry bits leaving the least significant adder pass serially through the next two adders, accumulating an additional 44 ns of delay. Delay through the most significant adder is 23 ns, and summing all delays gives a total of 103 ns for a 16-bit ripple-carry adder. Comparing ripple-carry and lookahead-carry delay, you find that ripple-carry is about 68% slower.

Worst-case ripple-carry delay (neglecting variations due to temperature and supply voltage) occurs when commands are changed via function select inputs. An extra 19 ns is needed to output a sum bit when the operating mode is changed and this must be added to the total delay. So the worst-case delay for a 16bit ripple-carry scheme becomes 122 ns.

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CIRCLE NUMBER 53

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CIRCLE NUMBER 54

Ideas for design

Twin-tee filter rejects more than 70 dB with capacitance-multiplier circuit

A capacitance-multiplier circuit, whose effective capacitance you can vary with a potentiometer, allows you to trim twin-tee notch filters to obtain more than 70-dB rejection. The gain of the circuit's op amp is varied with a 120-k Ω variable resistor. Signals across the filter's 0.068- μ F shunting capacitor are sensed by the amplifier and inverted. The inverted voltage is in series-aiding with the capacitor's signal swing. Consequently, increased current flows through the capacitor as if its capacitance were larger than the 0.068- μ F value (remember the old Miller effect?).

Twin-tee notch filters are excellent for removing single-frequency interference produced by 60 and 400-Hz power lines, but tuning the filters is usually difficult. Normal variable capacitors have values that are too low for use below 5 kHz and fixed capacitors limit adjustment flexibility.

The multiplier circuit's effective capacitance is

$$C_{eff} = 0.7 C (A_{CL}),$$
 (1)

where the op-amp's gain is

$$A_{\rm CL} = 0.2 + 0.67/x$$
 (2)

In Eq. 2, x is a fractional number that represents the unshorted portion of the gain-setting potentiometer. Because of the high impedance of the feedback tee-resistor network, a high-value summing resistor of 3.9 M Ω can be used, which limits loading of the filter network.

The circuit's tuning range centers about the gain setting, x = 0.55, so $C_{eff} = C$ and the null, therefore, occurs at a frequency

$$f_o = \frac{1}{\sqrt{2} \pi RC}$$

The component values in the figure tune to about 60 Hz. Of course, other values of f_o can be rejected by changing R and C, but keeping the proportionate relationships shown in the diagram.

A FET-input op amp limits the otherwise high output offset voltage that would result from any substantial input bias current in the feedback network. Although the op amp is capacitively coupled to the filter, a high offset voltage would decrease the op-amp's signal-swing capability. For a 30% adjustment of C_{eff} the op-amp's closed-loop gain must be as high as two; therefore, only signals up to one-half the rated output voltage of the op amp can be handled by the filter without distortion.

The 3.9-M Ω summing resistor produces 1% attenuation of the low-frequency signals that pass the resistance-topped branch of the twin tee. At high frequencies, however, the signal path is through the two 0.1- μ F-capacitor branch, which isn't affected by the capacitor-multiplier circuit. To make the passfrequency attenuation more uniform, connect a capacitor with a value of about C/100 from the junction of the 0.1- μ F capacitors to ground.

Bibliography

Wong, E. and Ott, W., Function Circuits; Design and Applications, McGraw-Hill, 1976.

Jerald Graeme, Manager, Monolithic Engineering, Burr-Brown Research Corp., International Airport Industrial Park, Tucson, AZ 85734.

CIRCLE NO. 311



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Switching supply converts -60 V to +5 and ± 6.3 V with 83% efficiency

The switching-regulated dc-to-dc converter in the figure combines series-switching regulation and voltage conversion-and does it with just three signal and two power transistors and one voltage-regulator IC. With an efficiency of about 83% and regulation to within $\pm 0.1\%$, power output is 5 W at +6.3 V and 4 W at +5 V over an input range of -50 to -80 V (nominally -60 V).

The converter is a driven type, modified to be regulated by pulse-width modulation. Signal transistors Q_1 and Q_2 switch on and off alternately, driven by a 50% duty-cycle square wave. When Q_1 is on, diode D_1 is forward-biased and current flows through half the driver-transformer primary of T_1 . The same thing happens for Q_2 and D_2 . The voltage developed across half the primary equals approximately $(N_1/N_2)V_{BE}$, where V_{BE} is the voltage across a converter power transistor, Q_3 or Q_4 , and N_1 and N_2 are the number of turns in half the primary and secondary, respectively. Capacitor C3 charges to twice the (N₁/N₂)V_{BE} voltage.

Because the voltage across C3 can't change instantaneously, the voltage across T_1 gradually shifts from the conducting power transistor to the other transistor. This action produces a "dead time" that not only prevents damaging cross-conduction of the power transistors, but also reduces RFI noise. Dead time, which occurs when both power transistors don't have enough base-emitter voltage for conduction, is proportional to C₃ and inversely proportional to the current from the controlled current source, Q₅.

Because inductor-input filters are used after the rectifier section, D₅ through D₈, the output voltages are proportional to converter "live" time. And since dead time is inversely proportional to the controlled

source current, controlling source current controls the converter output voltage. A 723 regulator IC, loop filter and reference voltage before the current source complete the regulator loop.

The converter operates from -60 V, and the regulator operates from +19 V in the circuit shown. But, both can be made to operate from the same supply voltage. Resistor R₃ helps damp out ringing in T₁. A current-limiting feature in the 723 regulator limits the maximum current from current-source Q₅; resistor R₇ determines this current. Resistors R11 and R12 average the two final output voltages for comparison with a 5.6-V reference voltage, which is determined by a selected resistor, R₁₀. Diode D₄ helps minimize any overshoot occurring at turn on.

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Philip M. Cowett, Jr., Electronic Engineer, U.S. Army, Harry Diamond Labs, 2800 Powder Mill Rd., Adelphi, MD 20783.

CIRCLE NO. 312



A driven switching power supply includes capacitor C3 to produce a gradual cross-over of power when switching from Q1 to Q2. The resulting dead time for Q₃ and Q₄ prevents cross-conduction and damage to the transistors, minimizes RFI and enables pulse-width modulation regulation.

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Ideas for design

Current inverters make current sources out of monolithic-IC d/a sink outputs

Convert the outputs of IC d/a converters from sinks to sources with an op-amp, floating, current inverter (see figure). Not only does the circuit provide a current-source drive from a current-sink input, it can also scale currents, to make the output much greater (or less) than the typical 2-mA full-scale d/a sink current. Virtually all IC d/a converters currently available have npn-based outputs. As a result, these converters are characteristically current sinks.

The op amp, acting as a precision, floating, current inverter, monitors an input current, I_{0A} , at its inverting input, which is the d/a's sink current.¹ With equal feedback resistors, R_1 and R_2 , the op amp then sources an equal current, I_{0B} , at its noninverting terminal. A load, R_L , can be referred to any potential within the d/a's voltage-compliance limits, as well as ground.

Currently, popular IC d/a converters include Precision Monolithics' DAC-08 (8-bit) and DAC-20 (2-digit BCD) and Analog Devices' AD561 (10-bit) units. These devices have nominal 2-mA current-sinking outputs, voltage-compliance ranges that extend to over 10 V, and output impedances of 20 M Ω or more.

An untrimmed 741 works reasonably well for 8-bit accuracy as a simple 1:1 current inverter. However, low-offset versions such as Analog Devices' AD741L or PMI's OP-02E guarantee 8-bit accuracy, and do well even to 10 bits. For micro-amp-level output (or input) currents, FET input devices such as National Semiconductor's LF355 or PMI's OP-15 should be used. Of course, if I_{0B} is to be more than a few milliamperes, a power op amp such as the Fairchild μ A759—with an I_0 to 350 mA—can be used for the floating current source and provide power output. But no matter which op amp you select, R_1 should provide a voltage drop of 1 V or more, at the maximum d/a current, to minimize the effect of op-amp offset. If output-voltage compliance is not a major factor, R_1 can drop as much as 10 V, which will minimize offsetvoltage errors.

Because both positive and negative feedback are used in the circuit, C_1 provides more negative feedback and thus ensures stability. High d/a output impedance also helps stabilize the circuits.

Reference

1. Gilbert, B., "Current Inverter with Wide Dynamic Range," Analog Dialogue 9-1, 1975.

Walter G. Jung, Consultant, Pleasantville Laboratories, Forest Hill, MD 21050. CIRCLE NO. 313



IFD Winner of September 13, 1977

George W. Masters, Teledyne Microelectronics, 12964 Panama St., Los Angeles, CA 90066. His idea "Demand Power Supply Draws Low Standby Current" has been voted the most valuable of Issue Award.

Vote for the Best Idea in this issue by circling the number of your selection on the Reader Service Card at the back of this issue. SEND US YOUR IDEAS FOR DESIGN. You may win a grand total of \$1050 (cash)! Here's how. Submit your IFD describing a new and important circuit or design technique, the clever use of a new component or test equipment, packaging tips, cost-saving ideas to our Ideas for Design editor. Ideas can only be considered for publication if they are submitted exclusively to ELECTRONIC DESIGN. You will receive \$20 for each published idea, \$30 more if it is voted best of issue by our readers. The best-of-issue winners become eligible for the Idea of the Year award of \$1000.

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ELECTRONIC DESIGN 2, January 18, 1978

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Transformer Catalog — A 20-pager for the do-it-yourself power supply designer with instructions on how to specify for your custom units. Also covers 833 of our standard military, industrial and miniature pcb power transformers. Included are 60 and 400Hz, single phase input units, with prices starting as low as \$5.10 for up to 9 pieces.

Circle Card Number 92

See Power Supply Section 4000, and Transformer Section 5600, Vol. 2, of your EEM catalog; or Power Supply Section 4500, and Transformer Section 0400, Vol. 2, of your GOLD BOOK for complete information on Abbott products.

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INCORPORATED

International technology

Video-disc system uses record-like platters

A video-disc system from Matsushita Electric Industrial Co. Ltd. uses plastic platters similar to standard audio records. As a result, the polyvinyl chloride discs can be manufactured on audio-record production equipment, so they won't cost as much as discs designed for laser, capacitive, or compression playback, like the ones proposed by Philips, RCA and Telefunken/Decca.

The Matsushita disc has a 30-cm diameter and is 2 mm thick. It spins at 450 rpm and provides 30 minutes of audio and video signals on each side with a track pitch of 4.6 microns, or 60 minutes per side with a 2.3-micron track pitch. The retail price for a onehour disc is expected to be about 20 to 50% greater than that of conventional audio records.

The disc, which handles video and two channels of audio on a bandwidth of 10 MHz, is cut in real time with a micro-cutting stylus that is ultrasonically driven by a piezoceramic material device. With conventional mechanical cutting methods, the master disc rotates at a fraction of playing speed, so the signal must be divided propor-



tionately to permit high frequencies to be engraved.

Matsushita's video-disc system, the VISC, includes a player that is projected to sell in Japan for \$480 to \$600. The player has an NTSC color signal with a signal-to-noise ratio of 45 dB and more than 270 lines of resolution. Audio bandwidth is 20 kHz, and audio s/n is about 60 dB.

Matsushita will hold off on marketing the VISC until it gets support from software suppliers, since the company feels "strong consumer acceptance of the video-disc player will depend to a significant degree upon the easy availability and wide range of quality software."

Grounding simplified with conductive cement

A conductive building material that mixes with cement makes it much easier to ground installations for rf transmitters, computers and similar equipment.

Normally, such installations are grounded by making connections to a network of wires buried in the ground outside and around a building. The location of these earth-electrode systems can help avoid mutual interference between equipments in the building.

With Marconite, developed by Marconi Communication Systems Ltd.

ELECTRONIC DESIGN 2, January 18, 1978

of Chelmsford, England, flooring, walls and sub-basement concrete structures can be produced with a predetermined volume resistivity. This concrete can also be used to form earth planes outside the building. Marconite can also be used in cathodic protection systems and as a high-loss tangent dielectric.

The volume resistivity varies from 0.5 Ω -cm or less for preformed, pressure-cured concrete sections to 15 Ω -cm for floors laid by hand. Where higher resistivities are required, such as for antistatic floors and high-loss dielectrics, the proportions of Marconite in the concrete mixture can be reduced by adding sand.

Chlorinated compound for capacitors is safer

A safe nonchlorinated ester-based compound with excellent electrical properties has been developed to replace unsafe chlorinated hydrocarbons in high-voltage capacitors.

The highly toxic nature and long term stability of chlorinated hydrocarbons, commonly used as power capacitor dielectrics not only make them unsafe but also ecologically unsound. However, the new liquid, benzyl neocaprate, has been demonstrated to be both nontoxic and easily biodegradable by common bacteria.

The compound took five years of joint research by Rhone-Poulenc, France, and ASEA, Sweden, to be developed. Rhone-Poulenc is now planning large-scale production and will make the fluid available to all capacitor manufacturers. ASEA is already producing capacitors using the fluid.

Fiber-optic connector places/aligns fibers

A new type of optical fiber connector eliminates a major problem hampering present connectors—the high cost of precision machine assemblies required for aligning the fibers precisely. Available connectors must first accurately mount the fiber in a ferrule, then align the ferrules in an external sleeve. The new connector developed by the British Post Office at its Research Center in Martlesham Heath Ipswich aligns and locates fibers simultaneously.

In the connector, a set of three small spheres of the same size accurately self-aligns with a similar set rotated through 60° . When the two sets are pressed together the balls rotate and lock into alignment, which leaves a small hole in the center.

Connectors for a fiber of $125-\mu m$ diameter require tungsten balls of 810- μm diameter, mounted in the sleeve one set behind the other. These balls are readily available.

MANAGERS-WORLDWIDE

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2. *High Speed:* Arrow-M R Relays can be operated at 500 cycles/sec.

The tiny power memory reed

3. Greater reliability and lower cost, due to simultaneous automatic fabrication of coil bobbin, contact and terminal.

4. In addition to the standard there are 1 coil and 2 coil latching types, which are useful for logic circuit design as a memory component.

5. Not only can they be automatically wave soldered on PC boards with a high density of electronic parts, but they are simple to clean with most degreasers and detergents without affecting maximum contact reliability.

6. *High Sensitivity:* Minimum operating power: Single Side Stable 80 mw/Bistable 40 mw

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21

CIRCLE NUMBER 62

New products

Mass-produced precise and stable resistors surpass wire-wound units



Caddock Electronics, Inc., 3127 Chicago Ave., Riverside, CA 92507. (714) 683-5361. 1 MΩ, 0.01%: \$4.43; 1 MΩ, 0.1%: \$2.04 (1000 qty); stock.

Caddock's TF series of oxide-film resistors overcome limitations of other precision-resistor types with these five advantages of the new Tetrinox thickfilm, complex-oxide technology used to make them:

1. Resistance values as high as 10 $M\Omega$. A 10-M Ω wire-wound resistor needs over half a mile of expensive fine wire. For example, a Dale wire-wound unit (WW412, $\pm 0.01\%$, 0.75 W) costs about \$40 compared to \$10.32 for a $\pm 0.01\%$ tolerance TF050N in quantities of 1000. And Vishay's ultraprecision resistors reach only to 100 k Ω in single resistors, so they're out of this race.

2. Temperature coefficients as low as 5 ppm/°C from -55 to 105 C. The TF050N's 15 ppm/°C tempco rivals Dale's WW412's 20 ppm/°C.

3. Long-term stabilities as low as 0.005% per 1000 hours, which is comparable to the best wire-wounds.

4. Tolerances as close as $\pm 0.005\%$, also comparable to the best wirewounds (and Vishay foil units).

5. *High-volume production*, which costs less than the special production methods and often painstaking hand labor required when producing ultra-

fine-wire, high-resistance, wire-wound units.

The stability inherent in Tetrinox technology allows design engineers to use relaxed tolerances. Values of as high as $\pm 0.01\%$ can be used without compromising long-term stability. To attain the same stability with other resistor types, you must often use $\pm 0.005\%$ tolerance, according to Caddock.

Caddock's $\pm 0.01\%$ -tolerance units can achieve a total-error-band stability of 0.02% for 1000-h operation under full load conditions—according to Caddock. Extensive tests have shown that the average drift under full load and maximum ambient temperature (70 C) for large test samples is less than 0.008%, or 80 ppm, after the first 1000 h.

The Tetrinox resistance film is a thick-film complex-oxide system in a glass matrix, fired onto an aluminumoxide ceramic substrate. Caddock believes the film to be the first and only nonmetallic resistance material that can consistently produce a tempco within 5 ppm/°C along with ultra longtime stability. Further, the material can be laser-trimmed in complex patterns without disturbing stability, whereas most thick and metal-alloy films tend to lose stability, and are thus limited to simple cutting patterns.

Moreover, the Tetrinox film provides high sheet resistivity ranging from 500 to 50,000 Ω /square. Fine nickel-chrome alloy wire (0.0005-in. dia) provides 3200 Ω /ft, and evaporated nickel-chrome only 200 Ω /square.

Vishay's nickel-chrome foil furnishes a low 2 Ω /square in practical thicknesses. For those reasons, it takes 100 Vishay-foil, 100-k Ω , S102 resistors or half a mile of the fine wire to make a 10-M Ω resistor.

Caddock	CIRCLE	NO.	306
Dale	CIRCLE	NO.	307
Vishay	CIRCLE	NO.	308

Mini dry-reed switch handles 115 VA



Hamlin, Lake & Grove Sts., Lake Mills, WI 53551. W. Bruenger (414) 648-2361. \$0.58 (5000 qty).

The MRT-2 miniature dry-reed switch has a 115-VA, resistive, rating and a 0.13-in. diameter by 0.8-in. length glass case. The maximum switching voltage is 200 V and contact resistance is 0.1 Ω max. Insulation resistance is 10⁸ Ω .

COMPONENTS

Low-cost, flashing red LED has built-in IC timing circuit

Litronix Inc., 19000 Homestead Rd., Cupertino, CA 95014. Terry Snowden (408) 257-7910. P&A: See text.

Lumen for lumen, flashing indicator lights attract attention far more effectively than steady-on lights. So Litronix has put a red LED lamp, the 650-nm FRL-4403, into a T-1-3/4 envelope with an IC timer. The unit flashes on and off approximately 2.5 times a second with an almost 50% duty cycle, whenever a steady 5 V is applied to its two leads.

The built-in IC flasher eliminates external switching circuitry. Of course, the LED can be driven directly from TTL circuits; it needs only 20 mA of drive current.

The FRL-4403 can operate over a range of 2 to 10 V, but then the flashing rate varies from once per second to nine times per second.

The lamp's viewing half-angle is 45° (at the 50% intensity points), and it delivers 1.2-mcd peak intensity.

Best of all, the price is hard to beat —a low \$0.59 in quantities of 1000. The FRL-4403 is available from stock.

CIRCLE NO. 305



Flasher IC

Reed relay offers low thermal EMF



Coto-Coil, 65 Pavilion Ave., Providence, RI 02905. Bill Poisson (401) 467-4777.

Low thermal-EMF reed relays, CR-3300, are used in input switching. They are epoxy-encapsulated in a flame-retardant polyester case (SE-O rated), and coated with a silicone rubber to provide stress-free encapsulation. Tinned electrolytic-copper pins minimize thermal-EMF junctions at the PC-board connections. The coil and coil terminations are well isolated from the switches and shield. They provide 1500-V-rms isolation between control and signal circuits. All relays are magnetically shielded.

CIRCLE NO. 322

Mini film/foil caps come taped or reeled



Seacor, 598 Broadway, Norwood, NJ 07648. (201) 768-6070. See text; stock to 4 wks.

Available taped or reeled for automatic-assembly operations, Type 102 capacitors use a polyester wrap with extended foil to give a noninductive characteristic. The capacitors come in values from 0.001 to 0.47 μ F at 100 to 600 V dc. Dissipation factor is 0.75% max at 1 kHz and 25 C. Operating temperature range is -40 to 125 C with voltage derated 1.5%/°C above 85 C. Size ranges from 0.197 to 0.625-in. diameter and length from 0.433 to 1.437 in. Price is \$0.063 (5000 qty) for a 0.01 μ F, 20%, 200-V unit. CIRCLE NO. 323

Ceramic capacitors fit with DIPs



EMCON, P.O. Box 81542, San Diego, CA 92138. Tom Sale (714) 459-4355.

Empac type 501 ceramic capacitors have a DIP configuration with maximum case height of 0.135 in., width of 0.28 in. and thickness of 0.1 in. Lead spacing meets IC-package circuitry specs. Type Z5U, X7R and COG (NPO) dielectrics with capacitances from 10 pF to 0.47 μ F are available in voltages of 25, 50 and 100 WV dc.

CIRCLE NO. 320

Thermal reed switch senses temperature



George Ulanet, 413 Market St., Newark, NJ 07105. (201) 589-4876. \$1 (1000 qty); 6 to 8 wks.

The OHD series of thermal reed switches uses a temperature-responding ferrite as a sensing element and a reed switch as an actuating trigger. The switches are rated at 120 V ac, 0.5 A. The maximum mean differential is 10 C and operating range is from 60 to 130 C. Both open-on-rise and close-onrise switches are available.

CIRCLE NO. 321

How fast can you accurately measure period or frequency of this wave form?



GATE TIME

10



MICROPROCESSING TIMER/COUNTER

The old way.

(About 5 minutes)

- 1. Find a scope and voltmeter.
- 2. Connect signal to scope.
- 3. Determine proper trigger points.
- 4. Connect signal to counter
- 5. Select period or frequency function.
- 6. Select time base.
- 7. Set input voltage range.
- 8. Set input coupling to DC.
- 9. Connect voltmeter to trigger level output-if counter has output. (If not, good luck.)
- 10. Set desired trigger level.

The easy way.

(About 5 seconds)

- 1. Connect signal to Racal-Dana 9000 counter.
- 2. Push P or FA button.
- 3. Push TL button.
- 4. Push AU button.
- The rest is automatic.

Now it's up to you.

You can continue to struggle along the old way. Or you can find out about the Racal-Dana 9000 Microprocessing Timer/Counter. The patented Auto-Trigger capability makes it the fastest and most accurate instrument in the world for the precision measurement of wave forms. Give us a call and we'll tell you how Racal-Dana systems technology can solve all your measurement problems the easy way.



Racal-Dana Instruments, Inc., 18912 Von Karman Avenue, Irvine, CA 92715, Phone: 714/833-1234.

COMPONENTS

Ceramics can replace crystals and LCs



Murata Corp. of America, 1148 Franklin Rd., S.E., Marietta, GA 30067. (404) 952-9777. \$0.30 to \$0.35 (5000 qty).

A line of piezoelectric ceramic resonators can replace quartz crystals and LC networks for audio and rf generation. These resonators are offered in two frequency ranges—195 to 600 kHz and 3 to 12 MHz. The units have a frequency tolerance of ± 2 kHz in the lower frequency ranges and $\pm 0.05\%$ in the higher ranges. Temperature stability is 35 ppm/°C from 195 to 600 kHz and ± 20 ppm/°C from 3 to 12 MHz. Dimensions for the largest unit in the line (lowest frequency) are about $13 \times 14 \times 4$ mm.

CIRCLE NO. 324

Pushbutton code switch comes in four formats



IVO Industries, 1109 Green Grove Rd., Neptune, NJ 07753, John Becker (201) 922-3600. \$3.50; stock.

A modular bidirectional pushbutton code switch, designated C3, comes in four formats: decimal, BCD, plus/minus and BCD complement. The switch carries loads up to 0.5 A at 60 V. Switch elements snap-lock together in any combination to form a dense switching assembly that spring locks into a simple rectangular cutout. A single switch element is 0.945-in. high, 0.3-in. wide and weighs 0.158 oz.

CIRCLE NO. 325

Inverter transformers operate at 15 to 25 kHz

Pulse Engineering, P.O. Box 12235, San Diego, CA 92112. John Kerr (714) 279-5900. \$7.60; stock.

A line of encapsulated ferrite-core inverter transformers are usable both in saturated or in driven nonsaturated states within a frequency range of 15 to 25 kHz. Output voltages of $\pm 6, \pm 9.5$ or ± 19 V dc can be obtained, after rectifying and filtering. Models designed for input voltages of 5, 12.6 or 29 V dc are available. Nine models provide power ratings from eight to 25 W. The transformers are packaged for PC mounting. Board space is 0.94 × 0.775 in. for the 8-W unit and 1.2 × 1 in. for the 25-W part. Max heights are 0.8 and 1 in., respectively.

CIRCLE NO. 326

Thick-film circuit is audio power driver



Centralab Electronics, 5757 N. Green Bay Ave., Milwaukee, WI 53201. A.J. Koschnick (414) 228-2751. \$2.95 (1000 qty).

The audio power driver is a thickfilm hybrid circuit in a Class AB quasicomplementary audio configuration that can drive a pair of external npn power transistors. By proper selection of power output transistors, audio amplifiers in the range of 3 to 35 W can be designed. The driver provides up to 150-mA drive current at low distortion (1%) over a typical bandwidth of 22 kHz.

CIRCLE NO. 327

Chip thermistors are directly solderable

Keystone Carbon, St. Marys, PA 15857. John Brock (814) 781-1591.

Chip thermistors have silver-contact pads that can be soldered with silverbearing soft solders by IR-reflow, hottip or immersion techniques. Size of chips is $0.1 \times 0.5 \times 0.01$ to 0.06 in. thick. The small size results in low thermal mass, fast response time, and a low dissipation constant of 2.5 mW/°C. Resistance values range from 3 to 20 k Ω .

CIRCLE NO. 328

Call your nearest ISC sales representative.

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COMPONENTS

LCD meter is housed in analog-type case



International Microtronics, 4016 E. Tennessee St., Tucson AZ 85714. Otto Fest (602) 748-7900. \$45 (100 qty).

The Model 800 LCD digital panel meter is housed in a standard 3-1/2in. analog-meter case. The display is a 0.75-in. high transflective type. For low ambient light, or in darkness, an optional backlight is available. The meter features autozeroing, bipolar-input capability and over 1000-M Ω input impedance. Accuracy is $\pm 0.05\%$ FS ± 1 digit.

CIRCLE NO. 329

Mini resistance trimmers use carbon on ceramic



International Importers, 2444 S. Western Ave., Chicago, IL 60608. Jeff Swanson (312) 254-4252. \$0.10 (10,000 qty); 8 to 10 wks.

HDK trimmers are made with carbon-film resistance elements on a miniature ceramic base. The trimmers have self-supporting terminals and knobs or shafts. Resistance elements are enclosed to prevent solder and dust penetration. Perpendicular and parallel mountings are available. The power rating is 0.3 W at 70 C, and the resistance range is 200 Ω to 1 M Ω .

CIRCLE NO. 330

Pots and resistors combined in one package

Bourns, Trimpot Products, 1200 Columbia Ave., Riverside, CA 92507. Bill Galvan (714) 781-5204.

Multifunction trimmers (MFT) combine cermet trimming potentiometers and resistor networks into one assembly. Nine configurations of the multiple trimmer and network combinations are offered. Packaged in DIPs, the assemblies are compatible with auto-insertion and automatic-test equipment. Five basic trimmer configurations in nine different models are packaged with various combinations of trimmers and resistor networks in 6, 8, 14 and 16-pin DIPs. Two models are available for op-gain trim applications.

CIRCLE NO. 331

Digital display counter works in hostile areas



Scientific Technology, 1201 San Antonio Rd., Mountain View, CA 94043. T. Scholten (415) 965-0910. \$85; 3 wks.

A six-digit-display event counter is for severe industrial use in hostile environments. The LED display, counter circuitry and power supply are mounted in an aluminum-die NEMA 4 and 12 rated enclosure. Counting rate is up to 1 MHz and input-power sources from 12 V dc to 240 V ac can be accommodated. Standby battery power is also available. The unit accepts either contact closure or logic inputs.

CIRCLE NO. 332

Power resistor is noninductive

Vishay Resistive Systems, 63 Lincoln Hwy., Malvern, PA 19355. (215) 644-1300.

Hermetically sealed power resistors, Model VHP-3, are noninductive and have a 2.5 ppm/°C tempco. Inductance is typically only 0.08 μ H; rise time 1 ns; and noise -32 dB. Power rating, either chassis mounted or with a heat sink, is 10 W; 3 W in free air. Maximum working voltage is 750 V, resistance range is 10 Ω to 39.2 k Ω and they are available to $\pm 0.01\%$ tolerance.

CIRCLE NO. 333

Capacitors are thin metallized polyester



TRW Capacitors, 301 W. "0" St., Ogallala, NE 69153. (308) 284-3611. From \$0.35; stock to 10 wks.

Lightweight metallized-polyester capacitors with a thin oval shape, types X663F and X663FR are as small as 0.93 \times 0.187 \times 0.438 in. The units are axially leaded, have a voltage range of 50 to 600 V dc and a dissipation factor of less than 1% at 1000 Hz. The capacitance values for the two types range from 0.01 to 10 μ F and the operating temperature range is -55 to 100 C.

CIRCLE NO. 334

Indicator lights offer press-to-test feature

Dialight, 203 Harrison Pl., Brooklyn, NY 11237. (212) 497-7600.

Indicator lights have a press-to-test feature that can check the lamp in a normally deenergized indicator circuit. Finger pressure on the lens cap breaks the normal circuit and connects a test circuit. The indicators are available in subminiature, miniature and large sizes for mounting holes from 0.469 to 1 in., with neon or incandescent lamps. The QPL approved lights meet the requirements of MIL-I-7961B and L-3661.

CIRCLE NO. 335

Berg Interconnection System sews up the electronics in the Athena 2000 machine by Singer.

Berg supplied 80% of the low voltage interconnect system for the Athena 2000 sewing machine by Singer—world's first electronic push button home sewing machine.

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INSTRUMENTATION

Logic probe uses pulse accumulator



A VR Electronics, Box 19299, San Diego, CA 92199. (714) 447-1770. \$22.95. The Catch-a-Pulse Experimentor uses a pulse accumulator and LEDs that respond to single pulses up to 20 μ s. The probe will accumulate multiple pulses in pulse trains with frequency response greater than 40 MHz. It is compatible with RTL, DTL, TTL, CMOS, MOS and microprocessors using a 3.5 to 15-V power supply. Thresholds are automatically programmed. LEDs indicate HI, LO, bad level, open-circuit and pulses.

CIRCLE NO. 336

Hand-held unit debugs micros



Computer System Dynamics, 7100 Broadway, Denver, CO 80221. (801) 487-8711. \$250.

A stand-alone microcomputer system analyzer (MSA-8) is a hand-held instrument that performs firmware and hardware debugging of 8080A, 8085 and Z80 microsystems. The device connects directly to the microprocessor. Data, address and a ready signal are displayed. Single step, single-step enable, trace enable and breakpoint thumbwheel switches are provided for control. Single step, hardware breakpoint and oscilloscope trigger capabilities are also included.

CIRCLE NO. 337

Digital multimeter reads true-rms, dBm



Data Precision, Audubon Rd., Wakefield, MA 01880. (617) 246-1600. \$279; stock.

The Model 1750 3-1/2-digit multimeter offers 36 ranges and six functions in a 0.1% basic accuracy instrument. The meter measures dBm and HI/LO excitation resistance in addition to dc and true-rms ac volts and current. The unit measures dc V from 100 μ V to 1000 V; ac V from 100 μ V to 1000 V (true rms), with a frequency response of 10 Hz to 20 kHz; and dc current from 100 nA to 10 A. Also measured are resistance from 100 m Ω to 20 M Ω , and dBm directly from -60 to +20 dBm.

CIRCLE NO. 338



Frequency counter spans 10 Hz to 18 GHz



Hewlett-Packard, 1501 Page Mill Rd., Palo Alto, CA 94304. (415) 493-1501. \$4500.

Keyboard control, coupled with a microprocessor, allows the Model 5342A microwave counter to measure both input-signal level and input frequency simultaneously over the range of 10 MHz to 18 GHz. The operator can define his own frequency offsets with a few keystrokes for fast receiver testing. Offsets may be positive or negative, and can be stored in memory for recall and display to the user. Frequency deviations about a given value are monitored.

CIRCLE NO. 339

minninnin

Function gen operates on ac or batteries



Exact Electronics, 455 S.E. 2nd Ave., Hillsboro, OR 97123. (503) 648-6661. \$250; 2 wks.

An ac or battery operated sweepfunction generator, Model 117, offers sine, square, triangle, ramp and pulse outputs. The main output is variable up to 15 V pk-pk open circuit, 7.5 V pkpk into 600 Ω . The unit has a range of 2 Hz to 200 kHz in three steps. Control of frequency can be internal with the frequency dial, or the unit will automatically sweep over a 1000:1 (3 decade) range, either linearly or logarithmically.

CIRCLE NO. 340

Waveform gen sweeps up or down



Krohn-Hite, Avon Industrial Park, Avon, MA 02322. (617) 580-1660. \$295; 4 wks.

The Model 1200 sweep generator sweeps up or down and delivers 20-V pk-pk sine, square and triangular waveforms from 0.2 Hz to 3 MHz. The sweep duration is adjustable from 1000 s to 1 ms. Also included are a 1500:1 manual tuning dial, 5% fine-tune vernier, variable dc offset, external VC input, control-voltage output proportional to frequency and auxiliary TTL output with less than 15-ns rise and fall.

CIRCLE NO. 341



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INSTRUMENTATION

In-circuit tester prescreens PC boards



Teradyne, 183 Essex St., Boston, MA 02111. Bob Sigsby (617) 482-2700. From \$54,500; 12 to 16 wks.

The L529 in-circuit tester prescreens PC boards for workmanship and component faults prior to a functional board test. The microprocessor-controlled tester includes an operator's test station, board handler and programming console. The test station includes a control panel that directs all system functions, two tape drives and a strip printer for generating diagnostic error messages. The programmer's console contains an interactive keyboard and CRT. Three tests are used for high-fault coverage on boards having up to 700 nodes: node-to-node continuity, guarded-component measurements and impedance.

CIRCLE NO. 342

Test system checks ICs with up to 120 pins

Fairchild Systems Technology, 1725 Technology Dr., San Jose, CA 95110. Ken Daub (408) 998-0123. \$500,000; 12 wks.

An automatic semiconductor test system, Sentry VIII, is capable of handling devices with up to 120 I/O pins. The system will handle microprocessors, peripheral chips, bit slices, phase lock loops, RAMs, ROMs, shift registers, UARTs and digital hybrids in NMOS, CMOS, SOS, ECL, DTL, TTL and I²L. Included are 16 timing generators, expanded waveform generation and 160-ps timing resolutions. Multitask software for simultaneous compiling, editing and testing are provided. Test programming can be created with a high-level language called FACTOR that permits the user to produce the most complex testing routines. Functional dc and ac tests can also be carried out with available stock programs.

CIRCLE NO. 343

Modular test set analyzes data systems

International Data Sciences, 100 Nashua St., Providence, RI 02904. (401) 274-5100. \$4050; 8 wks.

The Model 20910 is a modular, general-purpose test set that analyzes data-communication systems operating asynchronously up to 2400 bits/s and synchronously up to 20 kbits/s. The unit contains six modules in a rackmounted chassis that include a transmitter, receiver, error counter, and interface modules. The device provides a three-digit display of the bit-error rate.

CIRCLE NO. 344

F/v converter spans 10 Hz to 50 kHz



Gould Instruments, 3631 Perkins Ave., Cleveland, OH 44114. R.F. Kerzman (216) 361-3315. \$595; 12 wks.

A wideband frequency-to-voltage converter, Model 13-4618-20, permits direct measurement and recording of the frequency of signals from 10 Hz to 50 kHz. It detects the zero crossing of any waveform and outputs an analog dc voltage which is directly proportional to frequency. Unipolar signals which do not go through zero, such as TTL level pulses, are handled by switching-in an offset voltage of ± 1 V from the front panel. The unit responds to input signals of 10 mV to 500 V rms. Exact frequency is determined by selecting one of 36 calibrated frequency ranges, with full-scale outputs of 5.0 V dc.

CIRCLE NO. 345

MICRO/MINI COMPUTING

UV lamp erases EPROM chips



Ultra-Violet Products, 5100 Walnut Grove Ave., San Gabriel, CA 91778. (213) 285-3123. \$59.50.

The UVS-11E short wave lamp erases up to four EPROM chips at one time in 14 minutes. A safety interlock system protects the user against accidental UV exposure. The system comes with a holding tray for maintaining a constant exposure distance of 1 in.

CIRCLE NO. 346

Central-processor module supplied without memory



Digital Equipment, 1 Iron Way, Marlborough, MA 01752. Don Mallinson (617) 481-7400. \$459.

A central-processor module, KD11-HA, does not contain memories and is intended for uses that require custom RAMs or ROMs. The device is part of the LSI-11/2 family of microcomputer modules. Also included in the family are memory modules with the same half-width size (5×8.5 in.) as the central processor. The memories are available in 4, 8, 16 and 32-kword configurations with optional byte parity.

CIRCLE NO. 347

Memory expansion boards are for TI's CPU



Texas Instruments, P.O. Box 1443, M/S 653 (Attn: TM990), Houston, TX 77001. Alan Lofthus (713) 776-6511. \$595 (990/201), \$585 (990/206) in 1-9; stock.

Two memory expansion modules are for use with TI's TMS 9900-based CPU, the TM-990/100M. The TM990/201 board has 4 k \times 16 words of EPROM and 2 k \times 16 words of static RAM. The unit is expandable to 16 k \times 16 words of RAM by plugging in TMS 2716 EPROMs or TMS 4045 static RAMs. The TM-990/206 board has 4 k \times 16 words of static RAM, expandable to 8 k by plugging in 4045 static RAMs.

CIRCLE NO. 348







MICRO-DIP...10 and 16 position miniature binary coded DIP switch designed to be mounted directly to PC Boards. Ideal for address encoding, presetting, PCB programming...every area of digital electronics.

Packaged in a color coded, glass-filled nylon housing with terminals on .100 x .300 centers. It occupies only one half of a standard 14-pin DIP socket.

Screwdriver slot is rotated in either direction to desired setting. Gold contacts protected by dust-seal design.

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One year warranty.





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One year warranty.



CIRCLE NUMBER 69

MICRO/MINI COMPUTING

They're worth their weight in plastic.

Introducing Johnson's ______ new Micro J-80 capacitors with plastic bases.

Compared to monolithic rotor capacitors with ceramic bases, the Micro J-80 costs 30-35% less. Yet, in many aspects, its performance is equal or superior to the ceramic versions. Its one-piece stator and stator terminal provide uninterrupted current flow for greater reliability. Temperature characteristics exceed comparable units with ceramic bases by 1-2%. And Q is 300 or higher.

The Micro J-80 is available in either horizontal or vertical printed circuit mounting styles. For more information, mail us the coupon. Johnson's revolutionary Micro J-80. It costs like plastic, but it performs like ceramics.



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Card allows plotter use with HP System 45

Hewlett-Packard, 1507 Page Mill Rd., Palo Alto, CA 94304. (415) 493-1501. \$600; 12 wks.

The HP 98040A card adds the capability of controlling incremental drum and flatbed plotters to the HP 9800 System 45 desktop computer system. The plotter interface can be used with plotters that require user-coded data inputs. It enables the System 45 to use computer ROM commands to control nearly all plotting functions. Provided with the card are pulsed $\pm X$ and $\pm Y$ data lines that accept data rates from about 100/s to 5000/s in discrete steps of 100/s. Pen control is possible through pulsed "pen up" and "pen down" lines. The "pen down" delay is 30 ms or 60 ms, "pen up" is 15 ms or 30 ms.

CIRCLE NO. 349

Board set uses 6800 microprocessor

Adaptive Science, 1201 Park Ave., Emeryville, CA 94608. Dick Strang (415) 652-1805. From \$115/board; 6 wks.

A set of boards using the 6800 microprocessor is available in the Type 1000 series on standard 4.5×6.5 -in. cards. Each card has a 44-pin edge connector, and a fully buffered bus interface. Included in the set is a combination MPU/RAM board with 4 kbytes of static memory. An 8-kbyte static memory board allows system expansion if the use requires additional memory. while an 8-k ROM/PROM board provides permanent storage. A serial/ TBG board offers serial I/O with selectable baud rates from 75 baud to 19.2 kbaud and a programmable counter with a crystal-controlled oscillator for time base generation. A 32-bit parallel I/O board provides active or open collector outputs and buffered inputs. Analog input is provided by a 16-channel multiplexed 12-bit ADC board with a 20-us conversion time. A dual 10-bit DAC board provides analog output. A two-board video set features video generation for a 64-char by 16-line display. The 7×9 character set includes upper and lower case with descenders.

CIRCLE NO. 350

CIRCLE NUMBER 70
Personal computer hooks into TV set



Umtech, 150 S. Wolfe Rd., Sunnyvale, CA 94086. Rich Melman (408) 737-2680. \$500 (retail).

The Videobrain computer comes with everything necessary to hook it up to a TV set and start running programs. The brain is an 8-bit microcomputer containing 1 kbyte of RAM and 4 kbytes of ROM. The preprogrammed cartridges can contain up to 13 kbytes of ROM or RAM. The unit has jacks for tape cassettes, printer and telephone. Built-in are the basic text and timekeeping programs. The text program allows the typing and editing of a message of 7 lines with 16 char/line.

CIRCLE NO. 356

Systems aid in μ C product development

Futuredata Computer, 11205 S. La Cienega Blvd., Los Angeles, CA 90045. R. Scharf (213) 641-7700. \$4325 to \$7675; 2 to 4 wks.

Microcomputer product development systems, the Microsystem 12, 15 (tape-based), 20 and 36 (disc-based) are all built around Z-80 µPs. They include CPU with up to 56-k memory, highspeed 960-character CRT, ASCII keyboard, dual floppy disc or cassettetape unit, operating system software and documentation. Optional accessories and software include in-circuit emulator, line printers, extended Basic, Basic compiler, RDOS (disc operating system with relocatable macroassembler and linkage editor), and word processor. Plug-in modules permit the systems to be converted to 8080 or 6800 processors. Systems include two RS-232 serial ports, 8-bit parallel TTL I/O port, real-time clock, bootstrap in PROM, memory write-protect under software control, eight-level vectored interrupts, DMA capability and disc and tape operating systems with monitor, debugger, editor, assembler and copy utility.

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MICRO/MINI COMPUTING

EPROM programmer copies masters

SMR Electronics, 3 Haven Rd., Medfield, MA 02052. S. Rudnick (617) 359-7697. \$825.

Model 7608, a self-contained programmer for type 2704 and 2708 EPROMs, is used to copy master EPROMs and to read preprogrammed memories. Program entry via panel keyboard and true hexadecimal display of addresses and data are provided. An accessory emulator unit permits loading from an external keyboard or computer. Type 2716, $2 \text{ k} \times 8 \text{ EPROMs may}$ be programmed in two passes using an optional adapter board. Editing capabilities allow insertion and deletion of data with resequencing prior to programming.

CIRCLE NO. 358

16-k RAM goes into 8080 and Z80 computers

North Star Computers, 2547 9th St., Berkeley, CA 94710. (415) 549-0858. \$399 (kit), \$459 (assembled).

A 16-k RAM board, for S-100 bus computers, can be used in both 8080 and Z80 systems operating at full speed up to 4 MHz. The board uses 200-ns dynamic RAM chips and the on-board memory refresh is invisible to the processor. Bank-switching capability is provided and the addressing of the board is switch-selectable in two 8-k sections.

CIRCLE NO. 359

Mainframe forms basis for thrifty μ C

Integrand Research, 8474 Avenue 296, Visalia, CA 93277. Bob Frank (209) 733-9288. \$200; stock.

The Model 800 mainframe is a completely assembled and tested cabinet, motherboard, power-supply combination that allows complete freedom in building an economical computer by supplying only the chassis unit. The user can choose complementary CPU, memory, and I/O cards to complete a system. The chassis contains a 15position S-100 motherboard, 15-slot card cage, fan, line cord, EMI filter, fuse, power and reset switches and power supply.

CIRCLE NO. 360

Add-on memory upgrades Z80 development board



Mostek, 1215 W. Crosby Rd., Carrollton, TX 75006. (214) 241-0444. \$945; stock.

RAM-80B add-on memory The board, designated MK78108, upgrades the memory capability of the Z80based software development board, SDB-80. Using the MK 4116 RAM, the add-on board has 16, 32, 48, or 65 kbytes of RAM. Strapping options position the decoded memory space to start on any 16-k address boundary. Also provided are ports from the two on-board MK 3881 Z80 PIO circuits. Each I/O port is fully TTL buffered and has two handshake lines per port. Logic for a "page-mode operation" permits up to 1 Mbyte to be used in a single SDB-80 system.

CIRCLE NO. 361

Floppy-disc controller works with 8010 CPU



GSI Systems, 223 Crescent St., Waltham, MA 02154. Ed Letscher (617) 899-6688. \$495; stock.

The Model 10043 floppy-disc controller is a microprocessor-based disc control card that accepts commands from an 8010 CPU card via the 8010 backplane. The controller has an IBMcompatible format with 3328 bytes of data per track; a non-IBM-compatible high-capacity option formats each track with two sectors containing a total of 4096 bytes. When equipped for stand-alone operation, the 10043 responds to commands and transfer data via a high-speed serial RS232C port or modem. The unit can control up to four disc drives.

CIRCLE NO. 362

μP has double-density dual-drive floppy discs



Digital Systems, 6017 Margarido Dr., Oakland, CA 94618. John Torode (415) 428-0950. \$4995 to \$8135.

A microcomputer system with dualdrive, double-density floppy discs, Micro-2, is housed in a single cabinet with two Shugart floppy-disc drives. The single computer board has a Z80 CPU, 32 or 64-k RAM, four RS232 serial interfaces and a real-time clock. The disc controller uses either IBM 3740 format or a double-density format of 571 kbytes per diskette. With optional double-sided drives, the system can store up to 2.3 Mbytes.

CIRCLE NO. 363

Single-board memory mates with 6800 micros



Chrislin Industries, 31312 Via Colinas, Westlake Village, CA 91361. (213) 991-2254. See text; 2 to 3 wks.

The CI6800 16-k \times 8 semiconductor memory system operates with the Motorola EXORcisor and the MEC-6800 evaluation module. The memory allows expansion to 32, 48, or 64 k by interchanging the 4027, $4 \text{ k} \times 1$ dynamicmemory chip with its 16-k equivalent. The board plugs directly into existing EXORcisor connectors. Maximum processor throughput is obtained with the use of hidden refresh-control logic on board. Data access time is 300 ns, and cycle time is 750 ns. On-board memory select is available in 4-k increments up to 64 kwords. A write-disable switch makes the RAM a ROM to the outside world. OEM pricing is \$390 for 16 k × 8 and \$1230 for 64 k \times 8.

CIRCLE NO. 364

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Low-cost series . . . three inexpensive probes to answer many requirements.







MICRO/MINI COMPUTING

F8 micro is on a single board

Comptronics, 19824 Ventura Blvd., Woodland Hills, CA 91364. (213) 340-8843. \$249 (kit), \$299 (assembled).

The Model 1080 F8 development board is a microcomputer on an $8 \times$ 13-in., PC board. The unit has an F8 CPU, a Fairbug PSU, a 3853 SMI, 2 k × 8 RAM, 2-MHz crystal clock and interfacing circuits. Also included are a buffered address and data bus to an S-100 memory expansion connector and sockets for 4 kbytes of 2708 memory. The unit provides 1 k of 2708 user custom monitor and 32 bits of I/O arranged in four 8-bit ports. The microcomputer has RS232 or 20-mA currentloop support circuitry and two sockets for I/O expansion.

CIRCLE NO. 365

Software links PDP-8s for data exchange

Digital Equipment, Maynard, MA 01754. John Bond (617) 897-5111. \$900; stock.

DECnet-8 permits networking between PDP-8 systems. The package operates under the RTS/8 real-time, multitask operating system and supports as many as eight physical lines and 32 logical links. Asynchronous, synchronous, parallel, full and halfduplex lines are supported. On appropriate hardware configurations the RTS/8 implementation permits OS/8 operations as background.

CIRCLE NO. 366

Flexible-disc drive has dual heads

Memorex, San Tomas at Central Expressway, Santa Clara, CA 95052. (408) 987-2203. \$585 (OEM).

The Model-552 disc drive has two ceramic read/write heads that allow recording or reading of data on both sides of a dual-sided flexible disc. The drive records 492 kbytes in IBM 4964 format or up to 1600 kbytes of unformatted data. Access time is 3 ms/track. The data transfer rate is 250 kbytes/s in single-density mode. With an appropriate controller, the 552 can be operated in the double-density mode with a data transfer rate of 500 kbytes/s.

CIRCLE NO. 367

Add-in memory gives 32 kwords for Novas

Monolithic Systems, 14 Inverness Dr. E., Englewood, CO 80110. (303) 770-7400. 4 wks.

An add-in expansion memory, Model 3401, for Nova 800 and 1200 series, is expandable in 4-k steps to 32 kwords and is totally Nova hardware and software compatible. The memory is designed around the Burroughs-pinout, 4 k \times 1, NMOS static RAM, and is configured in 16-bit words. The nonvolatile memory has an access time of 240 ns, with 800-ns cycle time. Memory addressing is programmable in contiguous 4-k steps.

CIRCLE NO. 368

Convert 300-baud printer to 1200-baud terminal

Datasouth Computer, 122 W. Woodlawn Rd., Charlotte, NC 28210. Jim Busby (704) 523-8500. \$635 (25-99 qty).

A kit, Model DS120, converts a DEC LA36 300-baud teleprinter to a 1200baud interactive terminal by replacing the standard LA36 circuit card. The kit also provides bidirectional printing at 165 char/s, and automatic carriage movement to tab over white space. An EIA interface, horizontal and vertical tabs, X-on, X-off protocol, double-wide characters, parity selection, error detection and self-test mode are also included.

CIRCLE NO. 369

Audio cassette recorder can sub for paper tape

Pacific Cyber/Metrix, 3120 Crow Canyon Rd., San Ramon, CA 94583. Ted Netoff (415) 837-5400. \$117 (kit), \$187 (assembled).

A mag-tape interface module, 12080, allows an ordinary audio cassette recorder to be substituted for a papertape reader and punch in the PCM-12 microcomputer. The module uses bytestandard, self-clocking FM circuitry and allows operation at a rate three times faster than that of the reader/punch on a TTY terminal. In a system, an audio cassette can store 30,000 characters on a single side. A reader/punch module, 12070, is also available to interface the Addmaster Model 601 paper-tape reader and the Epson Model 6110 paper-tape punch to the PCM-12.

CIRCLE NO. 370

MICROWAVES & LASERS

Image-rejection mixers cover 2 to 12.4 GHz



Varian, Salem Rd., Beverly, MA 01915. (617) 922-6000.

The 9753 low-noise image-rejection mixers cover 2.0 to 12.4 GHz in bands up to an octave wide. Each model consists of two mixers; a 90° hybrid and a power divider combined in a single microwave IC. Compact packaging is achieved by combining the i-f quadrature network and mixers in a single housing. Minimum image reflection is 18 dB. Local oscillator level is +6 to +9 dBm. I-f frequency is dc to 300 MHz, and i-f bandwidth is any 20% band.

CIRCLE NO. 371

Harmonic mixer accepts 0.1 to 26-GHz inputs



Millimeter, P.O. Box 5097, Santa Monica, CA 90405. (213) 823-2768.

Series 1050 harmonic mixers cover an input rf range of 0.1 to 26 GHz. Responding to even or odd orders through the 50th harmonic of the LO, the mixers provide new capabilities for systems with limited LO bandwidths or power. I-f output bandwidths are available to 1 GHz. SMA connectors are standard.

CIRCLE NO. 372

Coaxial attenuator is compact, rugged



Telonic/Berkeley, 2825 Laguna Can-

yon Rd., Laguna Beach, CA 92652. Dick Aaron (800) 854-2436. \$30.

The tubular attenuator, Model 8207, weighs 0.5 oz and measures 1.24 long by 0.38-in. dia. and meets MIL-A3933B/III and MIL-A3933B/15. The unit has a \pm 0.3-dB flatness across its full attenuation range and a power rating of 3 W at 85 C. Over the frequency range (dc to 4.5 GHz), the impedance is 50 Ω . Standard attenuation values are 3, 6, 10, 20, 30, 40, 50 or 60.

CIRCLE NO. 373

Need a second source on optically coupled isolators?

HIGH SPEED ISOLATORS Spectronics 6N135-6N139 are pin-for-pin replacements for respective HP6N135-139 devices.

3000 VDC Isolation!

Part No.	Input Current	Data Rate	CTR
6N135 (SCH-4350)	16 ma	1 Mbit/sec	7% (min)
6N136 (SCH-4351)	16 ma	1 Mbit/sec	19% (min)
6N138 (SCH-4370)	1.6 та	300 Kbit/sec	300% (min)
6N139 (SCH-4371)	0.5 ma	300 Kbit/sec	400% (min)

Spectronics SCS11C1-C3 are pin-for-pin replacements for respective GE H11C1-C3 devices. 5000 VDC Isolation!

PHOTO SCR ISOLATORS

PART NUMBER	TURN ON CURRENT (MAX) (IF)	FORWARD BLOCKING VOLTAGE (V _{DM} @ R _{gk} = 10 Kohm)
SCS11C1	11mA	200V (Min)
SCS11C3	14mA	200V (Min)

For more details and delivery information, contact Commercial Component Marketing, 830 E. Arapaho Road, Richardson, Texas 75081, (214) 234-4271.



ELECTRONIC DESIGN 2, January 18, 1978

MODULES & SUBASSEMBLIES

Field-repairable i-f strips cut purchase, inventory costs



Ple

RH

Var

Plessey Semiconductors, 1641 Kaiser Ave., Irvine, CA 97214. Dennis Chant (714) 540-9979. \$575-\$650 (unit qty), \$350-\$475 (1000-up), depending on specific requirements; 8 wks.

A series of hybrid-circuit amplifiers for 120, 160 and 240-MHz i-f frequencies offers low cost, better protection against the environment and quicker repair than amplifiers using packaging that's supposed to be more sophisticated.

Instead of using uncased, monolithic, IC-amplifier chips, transistors and discrete and hybrid passive components on a few ceramic substrates in an aluminum shell, the Plessey PSLT series houses amplifier chips in eight 8-pin TO-5 cans. The chips are mounted on 50×60 -mil ceramic substrates with two chip capacitors and a thin-film resistor.

The cans are mounted with discrete components on a single PC board that's mounted in a $4-1/2 \times 1-3/4 \times 1/2$ inch aluminum shell. That's about the same size that's used for competitive amplifiers from companies like Varian and RHG.

The Plessey approach offers several advantages. The semiconductors are protected from the environment in hermetic cans. In case of failure, the canned amplifiers can be replaced individually. So, instead of stocking complete amplifiers that cost \$650 to \$850 in unit quantities (for competitive units), a user can stock \$24 cataloged TO-5 amplifiers that are easy to replace in the field.

The amplifiers are intended mainly for radar receivers in electronic-warfare and electronic-countermeasures equipment, but they're suitable for a wide range of communications receivers. Bandwidths are available from about 9 to 25 percent of the center frequency. Gain is available to 100 dB and dynamic range to 70 dB.

CIRCLE	NO
CIRCLE	NO
CIRCLE	NO
	CIRCLE

14-bit hybrid d/a has differential input

ILC Data Device, Airport International Plaza, Bohemia, NY 11716. (516) 567-5600. \$245; stock to 4 wks.

A 14-bit hybrid multiplying d/a converter, DAC-U, has differential input, a remote ground and sense capability. The device has a linearity of 0.0125% with a settling time of less than 20 μ s and maintains full resolution for two as well as four-quadrant operation.

CIRCLE NO. 374

302

303

304

Digital process monitor takes nonlinear inputs



Dynamic Sciences, 7660 Gloria Ave., Van Nuys, CA 91406. Sylvia Sass (213) 893-6341. \$568; 4 wks.

The digital process monitors in the 7000 series can be programmed to accept inputs from any linear or nonlinear transducer. The meter handles transducers with multiple-valued transfer functions. The monitor is a 3¹/₂-digit instrument with 0.43-in. LED displays. It accepts current inputs of 0 to 1, 4 to 20 and 10 to 50 mA and voltage inputs of 0 to 1, 1 to 5 and 0 to 10 V. Common-mode rejection is 100 dB at 60 Hz, increasing at 20 dB/decade. Sampling rate is factory set at 3 to 5 s and is field adjustable from 40 readings/s to 1 reading/10 s. The accuracy is 0.1% FS ± 1 LSB. CIRCLE NO. 375

8-bit a/d converts at rate of 20 MHz



Datel Systems, 1020 Turnpike St., Canton, MA 02021. Eugene Murphy (617) 828-8000. \$1995.

ADC-TV is an 8-bit (48 dB) a/d converter with a conversion rate of 20 MHz. Digital and analog connections are made with a 37-pin subminiature "D" connector and a 3-mm terminated coax connector, Either ECL or TTL can be chosen as well as various inputtermination impedances. Conversion pulses adjust throughput for any rate up to 20 MHz and the characteristics can be optimized at popular conversion rates of 14.3 or 17.72 MHz. No time delays are required.

CIRCLE NO. 376

Only one thing beats our Super-Mini Impact Printer...

Why stop with the data/text versatility of our 120 cps, 20-column multiple-copy mini. It works even harder as a complete system. Teamed with its own microprocessor interface and power supply, there's virtually nothing our DMPT-3 can't handle - from telemetry to process control, from unattended system recording to providing hard-copy data terminal output, even in POS and inventory control. Mated with any ASCII system, it takes either parallel or serial input at speeds up to 16 KHz or 1200 bps.

Alone or as a system, of course, the industry's smallest alphanumeric impact printer lets you economize with ordinary adding machine roll paper.



PA



With both full alphanumerics and enhanced characters, our little

workhorse calls attention to emergency conditions. And with its 75,000-line life, ink cartridge that's replaceable in seconds, you know you're set for a good, long time.

For more details, call or write today. System \$452 (Printer, \$192; Controller, \$150; Power Supply, \$110); \$330 complete in 100's.



PRACTICAL AUTOMATION, INC. Trap Falls Road, Shelton, Conn. 06484 Tel.: (203) 929-5381

CIRCLE NUMBER 75

FIX-A-DIP & FORM-A-DIP which do you need to straighten and reform IC leads . . . or both?



FIX-A-DIP — used to reform any IC to a reusable state by means of a dual set of precision racks. Insert IC between teeth and strike handle to complete reform.

Works with all IC sizes of 0.3"

to 0.6" and 6 to 40 pins.

FORM-A-DIP-

used to resplay any IC to its original 8 to 12° splay after burn in or testing. Reforms to prevent falling out of insertion tools, automatic equipment or PC boards.

Micro Electronic Systems Inc. ^{8 Kevin} Drive, Danbury, CT 06810 Tel. (203) 746-2525, Telex 969659

vin Drive, Danbury, CT 06810 Tel. (203) 745-2525, Telex 9696 Distributor stocked throughout the U.S.A.



See Booth #G-201 at NEPCON WEST. CIRCLE NUMBER 76



MODULES & SUBASSEMBLIES

First 16-bit support boards mate with TI microcomputer

Analog Devices, P.O. Box 280, Norwood, MA 02062. (617) 329-4700. P&A: See text.

The first analog I/O PC boards aimed at Texas Instruments' 16-bit microcomputers—and only the second such 16-bit cards on the market—are functionally, electrically and mechanically compatible with the TI TM-990/ 100M μ C. The Analog Devices RTI-1240 family consists of two output subsystems, two input subsystems and two input/output boards:

■ RTI-1242—Four 12-bit analogoutput channels with eight digital-output peripheral drivers.

■ RTI-1243—Same as the 1242 but with eight analog output channels.

■ RTI-1240-R—32 single-ended or 16 differential inputs with a resistor-programmed-gain amplifier.

■ RTI-1240-S—Same as the "R" but with software-programmable gain.



■ RTI-1241-R—I/O card with inputs like 1240-R's plus two 12-bit output d/a converters.

■ RTI-1241-S—I/O card with 1240-S features plus two 12-bit d/a's.

Each card is memory-mapped, so the TI μ C treats them as any other memory location. Prices range from \$395 and \$675 for the 1242 and 1243, respectively, to \$445 and up for the 1240 and 1241. Delivery is from stock.

CIRCLE NO. 301

Active notch filter mounts into DIP socket



A.P. Circuit, 865 West End Ave., New York, NY 10025. Felix Ellern (212) 222-0876. \$35 (100 qty); 2 wks.

A miniaturized active notch filter, Model APN-3, measures $1.3 \times 0.8 \times 0.6$ in. and mounts into a 24-pin DIP socket. The filter comes pretuned to eliminate a specified frequency such as 60 Hz and can be externally tuned to a different frequency with one pot. Any pretuned frequency from 1 Hz to 30 kHz can be provided. Temperature stability of the center notch frequency is $0.025\%/^{\circ}C$.

CIRCLE NO. 377

Multiplying d/a has 12-bit accuracy



Beckman Instruments, 2500 Harbor Blvd., Fullerton, CA 92634. Josephine Rickard (714) 871-4848. \$85 (100 qty); stock.

The 7521M CMOS 12-bit multiplying d/a converter is hermetically sealed in an 18-pin DIP and has 12-bit accuracy and resolution from -55 to 125 C. Compatible with TTL and CMOS logic, the addition of external amplifiers enables unipolar or bipolar operation. The converter consumes 20 mW from +5 to +15-V supplies. Material, construction and workmanship conform to MIL-STD-883 Method 2017 Level B.

CIRCLE NO. 378

Keyboard uses μ C and Hall-effect keys



Micro Switch, 11 W. Spring St., Freeport, IL 61032. (815) 235-6600.

A full-function "intelligent" keyboard, Model 103SD24-1, combines a single-chip microcomputer with 103 Hall-effect key modules. The microcomputer integrates an 8-bit CPU, a ROM program, RAM, I/O lines and a time-event counter on a single chip. Additionally, a 40-pin EPROM is available that is pin-compatible with the standard ROM. Among the features are: 14 relegendable keytops for programming keys; four-mode, 8-bit USASCII code assignment; choice of serial or parallel data outputs; 8-deep FIFO character storage; N-key rollover; timed/auto repeat for selected keys; secretary shift, and a signal for audio-feedback drive.

CIRCLE NO. 379

Processor-panel display can be cut to length

Telesis Lab, 41½ S. Paint St., Chillicothe, OH 45601. Jim Eley (614) 773-1414. \$76; 1 to 6 wks.

The DMO-16 processor-panel display may be cut to any length between 8 to 16 digits. The numeric-display characters are 7-segment 0.3 in. LED types. Display includes drive electronics for mating to an 8-bit TTL processor output. The character address uses four bits; the remaining four bits provide the BCD data to be displayed by the addressed character. Multiplexing is done by software scanning, but for systems with hardware multiplexing, a 16 \times 4 RAM is provided.

CIRCLE NO. 380

The Titchener Difference saved 100% in internal costs and 200% in weight in this microcomputer



Digital Equipment Corp.'s PDP 11/03 microcomputer

... A real plus in your production planning because we can nearly always improve performance characteristics, reduce weight *and* lower the unit cost of the part or component! Big claim? Then you'll be more interested in what one of our customers, Digital Equipment Corp., has to say about the wire and sheet metal chassis we did for their microprocessing equipment.

"We used your wire form construction on both our PDP 11/03 and PDP 11/04 units. As a result, internal structural costs were reduced 100%; weight of the component was reduced 200%. In addition we achieved more efficient cooling, better accessibility and reduced assembly time.

Because of the success of these two designs, we'll be considering your wire forms in future work!"

That's what the Titchener Difference is all about. Want to bet we can do the same kind of thing for you? Just contact.

TITCHENER

E. H. Titchener & Co. 22 Titchener Place Binghamton, N.Y. 13902 (607) 772-1161

Creative design and production in wire, sheet metal and tubing.

ELECTRONIC DESIGN 2, January 18, 1978

Memory Power Eternacell® 10 year lithium primary battery for semiconductor memories

Don't risk memory failure. Eternacell[®] high reliability, lithium primary batteries are the ideal standby power source for all types of volatile memory applications. The reasons:

- Steady voltage (2.9 volts per cell) at low continuous current
- Shelf life of up to 10 years
- Highest energy per unit weight and volume
- No recharging
- Hermetically sealed
- Designed for pc board mounting

For complete information and pricing write: Power Conversion, Inc., 70 MacQuesten Parkway South, Mt. Vernon, N.Y. 10550. Or call (914) 699-7333

Model 440 2.9 volts 1.0 ampere-hours 0.64" diameter 1.31" height DWEER COENCERS

CIRCLE NUMBER 80



6500 Tracor Lane • Austin, Texas 78721 • AC 512/926-2800

POWER SOURCES

Compact dc/dc converters deliver 40 W



Semiconductor Circuits, 306 River St., Haverhill, MA 01830. Ted Brewster (617) 373-9104. \$109.95/\$104.95; stock to 2 wks.

Two encapsulated modular dc/dc converters deliver 40 W and occupy $3.5 \times 2.5 \times 2$ in. The Model CW12-5S8000 operates from an input range of 9 to 18 V dc. The Model CW24-5S8000 accepts an 18 to 32-V-dc input range. Both models deliver a single +5 V dc at 8-A output with foldback protection. The units have respective line and load regulation of 0.5 and 1% and output ripple and noise of 13 mV rms. Both models operate with no derating from -25 to +60 C.

CIRCLE NO. 381

Open-frame switcher gives four outputs

LH Research, 1821 Langley Ave., Irvine, CA 92714. Wally Nusslock (714) 546-5279. \$297 (100 qty); 8 wks.

The Model TM-34 switcher power supply packs 175 W of four-outputpower in 13 by 6 by 2.75 in. The supply gives four output voltages from 5 to 28 V. The main output is 5 V at 20 A. Second and third outputs can be any combination of the following: 5 V at 5 A, 12 V at 5 A, 15 V at 4 A, 18 V at 3 A, 24 V at 2 A, or 28 V at 2 A. The fourth output can be any of 5, 12, or 15 V at 1.5 A. The total power may not exceed 175 W.

Storage batteries handle high-rate discharges



Globe-Union, 900 E. Keefe Ave., Milwaukee, WI 53201. Tom Wagner (414) 228-2581.

A series of Tel/Cell storage batteries is designed for the high-rate, shortduration discharges found in switchgear and uninterruptible power systems. The Tel/Cell UPX Series line of batteries packs more power per pound for discharges of less than one hour than other battery types. Every battery is custom built for each application. The batteries range in size from 1 to 7 kW/cell and from 600 to 2000 Ah. CIRCLE NO. 383

Solar cells have high efficiency



Optical Coating Lab, 15251 E. Don Julian Rd., City of Industry, CA 91746. (213) 968-6581.

A line of silicon solar cells operates at high conversion efficiences under concentrated sunlight. Tests have verified a conversion efficiency of 16.5% at a 20-sun concentration and 15% with a 50-sun concentration at 28-C celloperating temperature. The cells are for use at concentrations of from 10 to 50 suns. Cells range up to 37 cm² in a variety of shapes.

CIRCLE NO. 384

Triple output switcher has fourth-output option



Hewlett-Packard, 1507 Page Mill Rd., Palo Alto, CA 94304. (415) 493-1501. \$636 (100 qty); 4 wks.

A multiple-output, switching-regu-

lated power supply, HP 63312F, provides three adjustable output voltages of 5, -12 to -15, and +12 to +15 V. An optional fourth output, as specified by the customer, is offered. The 550-W modular supply has brownout-protection circuits that allow full output power with input voltage from 87 to 127 V ac. The unit's three main outputs are regulated to 0.1% for full line and load variations, with ripple and noise of 0.05 V pk-pk at the 5-V output and 0.075 V pk-pk at the dual outputs.

CIRCLE NO. 385



tance (L, C) and loss (D, R, G) of passive components are now practical for anyone with ESI's Model 252 Digital Impedance Meter. Check these features: · Measures D as well as L, R, C, G, automatically . Light weight tilt stand handle • 0.25% basic accuracy · Wide ranges (autoranging optional) • 1 kHz test frequency (120 Hz optional) • Four measurements/sec. • External bias • 4-terminal connection • Analog outputs • Low power design · Large 31/2-digit

calibration · Optional front panel dust cover.

Measurements are simple, fast and accurate...Set the range and connect to unknown. Four-terminal KELVIN KLIPS® are included and the 252 can be combined with ESI's Model 1412B Limits Comparator and a special test fixture for go/no go testing.



Electro Scientific Industries, 13900 N.W. Science Park Dr., Port-ELECTRO land, OR 97229. Tele-SCIENTIFIC phone: 503/641-4141. land, OR 97229. Tele-



- * IN-CIRCUIT EMULATOR
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- * SELF POWERED
- * STAND ALONE
- * PORTABLE



GET THE BUG! \$ 1860.



ICs & SEMICONDUCTORS

Sample-and-hold device gives 12-bit accuracy



Burr-Brown, P.O. Box 11400, Tucson, AZ 85734. Steve Harward (602) 294-1431. \$7.95 (1-24 qty); stock.

Contained in a TO-99 package, the SHC298 sample-and-hold amplifier combines 12-bit throughput accuracy, wideband noise less than 20 µV rms, and a droop rate of 5 mV/min with a $1-\mu F$ external capacitor. The unit has fully differential logic inputs for mode control, allowing inputs to be driven with a twisted pair. Input logic levels are DTL, TTL and PMOS compatible. Input impedance is greater than $10^{10} \Omega$, and acquisition time is less than 10 μ s. Other specs include gain error less than $\pm 0.005\%$, gain drift less than 4 ppm/°C, and full power bandwidth of 125 kHz with a 1000-pF holding capacitor. Power supply range is ± 4.75 to ± 18 V.

CIRCLE NO. 386

1-A rectifiers have 50 to 1000-V PRV



Solid State Devices, 14830 Valley View Ave., La Mirada, CA 90638. Dee Peden (213) 921-9660. See text; stock to 2 wks.

A line of fast-recovery rectifiers, the RP1 series, has peak-reverse voltages from 50 to 1000 V at 1 A with max reverse current of 5 μ A. Max reverse-recovery time is 250 ns for PRVs up to 600 V and 500 ns for the 800 and 1000-V devices. The diffused-junction devices are packaged in molded-plastic DO-41 cases. The 50-V devices are priced at \$0.20 each and the 1000-V units are priced at \$1 each in 1000 quantity.

100-A transistor claims largest junction



Germanium Power Devices, Andover, MA 01810. J.Q. Adams (617) 475-5982.

A power transistor with $I_{\rm C}$ up to 100 A is based on what is believed to be the largest discrete germanium junction ever used, a 0.475-in. diameter chip. The GPD 100SC series gives high gain (h_{\rm FE} = 120 at -60-A I_{\rm C}, -1-V V_{\rm CE}). V_{\rm CE} (SAT) is 0.5 V max at 100-A $I_{\rm C}$ and only 0.3 V max at 75-A $I_{\rm C}$. The transistor is housed in a TO-68 case.

CIRCLE NO. 388

Power transistors handle 800-MHz mobile FM

Motorola, P.O. Box 20912, Phoenix, AZ 85036. Alan Wagstaffe (602) 244-6394. \$4.90 to \$20; stock.

Four uhf Class C power transistors, ranging from 1 to 20-W continuous output, operate in the 806 to 947 MHz FM band. All devices can operate from 12.5 V mobile supplies. The MRF838 and MRF838A are 1-W, stripline studless and stud common-emitter devices. MRF840, rated at 7 W and MRF842, at 20 W, are both connected for commonbase operation in a CS-12 package. Input matching is optimized for 100-MHz instantaneous bandwidth. Series equivalent input and output impedances are specified for large signal operating conditions, with power gains ranging from 6 to 8 dB.

CIRCLE NO. 389 ELECTRONIC DESIGN 2, January 18, 1978

Single chip acts as FM i-f subsystem

Motorola, P.O. Box 20912, Phoenix, AZ 85036. Dough Fryman (602) 962-3101. \$1.75 (100 qty); stock.

The MC3357 i-f subsystem contains nearly all components, from second mixer through audio and squelch outputs, needed for narrowband FM reception. Input is a first i-f frequency, typically 10.7 MHz. An internal doubly balanced mixer, driven by a Colpitts local oscillator, produces a second i-f in the 455-kHz range. After routing this signal through an external multipole bandpass filter, the device provides a five-stage, emitter-coupled, limiting i-f amplifier chain, followed by a balanced quadrature detector. Detected audio is amplified and processed by an active filter amplifier, and squelch is detected by a noise-operated switch. Additional outputs are used for audio muting and to provide logic triggering for scanning receivers. Typical 10.7-MHz mixer input sensitivity is 5 μ V. The detector produces 350 mV of audio from a narrow 3-kHz signal deviation.

CIRCLE NO. 390

8-bit d/a has 85-ns settling time



Datel Systems, 1020 Turnpike St., Canton, MA 02021. Eugene Murphy (617) 828-8000. \$8/\$12; stock.

Two fast monolithic 8-bit d/a converters with 85-ns settling time are available. Model DAC-08BC comes in a 16-pin plastic DIP and operates over 0 to 70 C and the DAC-08BM is in a 16-pin ceramic DIP and operates over -55 to +125 C. Nonlinearity is held to less than 0.19% or $\frac{1}{2}$ LSB. An external reference current programs the scale factor and can be varied, resulting in one or two-quadrant multiplying operation. The output current has a compliance of -10 to +18 V, allowing direct current-to-voltage conversion with just an output resistor.

CIRCLE NO. 391

Data collection made easy with reliable low cost optical badge and card reader.



The only reader that interchanges plastic & paper cards. Hollerith-punched paper or plastic cards read instantly. At any insertion speed. No adjustments necessary.

A complete package. No code converters to add. Plugs into standard printed circuit connector. Internal or external clocking capability. All information and controls in one unit.

No moving parts. Won't damage cards, badges. Advanced optical sensing and electronic logic circuitry for high reliability, long life.

Transmit at any speed. Independent data clocking and storage enables reader to transmit at desired rate without adjustments.

Self-checking! Can't make a mistake. Integrated monitor signals any defect in a sensor, light source, card, number of characters or position of card. Transmits only good messages. NUMERIC Model D-57

...

122121121



Ask us how optical reliability can improve your data collection.

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CIRCLE NUMBER 84

ELECTRONIC DESIGN 2, January 18, 1978

DATA PROCESSING

Microcomputer products from Dynabyte



16K FULLY STATIC RAM. S-100 bus, 250 ns. or 450 ns. RAM access time, bank select, 4k block addressing on 4k boundaries, write protect, assembled, tested, burned in, 1 year guarantee, 250 ns.—\$555, 450 ns.—\$525.

32K FULLY STATIC RAM. S-100 bus, 250 ns. or 450 ns. RAM access time, 4k block addressing, 70° max. ambient operating temp., assembled, tested, burned in, 1 year guarantee, 250 ns.—\$995, 450 ns.—\$925.

16K DYNAMIC RAM. S-100 bus, no wait states, transparent refresh, DMA control, 350 ns. access time, assembled, tested, burned in, 1 year guarantee, \$399.

DUMB TERMINAL, an S-100 bus board, add keyboard and video monitor to replace stand-alone terminal and serial I/O board, saves 30-60%, 80x24 display, upper & lower case, addressable cursor, block mode, assembled, tested, burned in, 1 year guarantee, \$350.



4020 Fabian, Palo Alto, CA 94303, (415) 494-7817, Cable "Dynabyte"

CIRCLE NUMBER 85

MAGNETICALLY SHIELDED DATA PRESERVERS

Protect your Flexible Disks from magnetic degradation, erasure, or physical damage. Cases are designed for storage, shipment and hand carrying. A wide choice of models and capacities also available for Minidisks, Diskettes, Standard Reels, Disk Packs, Standard Cassettes.





FLOPPY DISK

SEND FOR NEW TP-5 CATALOG

Smart modem replaces three different ones

Vadic, 505 E. Middlefield Rd., Mountain View, CA 94043. (415) 965-1620. \$850.

A microprocessor-controlled modem, the VA3467, automatically recognizes, and communicates with the Vadic VA3400 (1200 bps full duplex), the Bell 103 (300 bps full duplex), and the Bell 212 (1200 bps full duplex). It contains all the components needed for direct connection to switched telephone lines, eliminating the need to rent DAA's from the phone company. Computers capable of using the VA3400, or the Bell 103 and 212 can use the VA3467 without altering hardware or software. The smart modem satisfies every answer mode application for switched network data transmission in asvnchronous data format, at rates from 0 to 1200 bps, and occupies two card slots in the standard Vadic VA1616 or VA1601 chassis. Another unique feature is the VA3467's ability to continuously test itself by turning on its transmitter, switching its receiver to the same carrier, and sending a scrambled mark into the transmitter. If the receiver doesn't get the proper signal, a flashing status light alerts the operator. The VA3467 complies with FCC registration requirements to connect directly to switched telephone lines through a phone company-supplied data jack.

CIRCLE NO. 392

300-Mbyte mass storage plugs into SyFA units

Computer Automation, 18651 Von Karman, Irvine, CA 92713. (714) 833-8830. \$32,500; 16 wks.

A 300-Mbyte mass storage device, DSK300, meets the large-scale data base requirements of SyFA network processing systems. The device offers 220 Mbytes of user accessible storage, and employs CDC 9883-91 removabledisc packs. Up to eight DSK-300s can be linked to a SyFA system, extending total user-accessible storage to 1760 Mbytes. Storage is totally compatible in format and hardware with existing SyFA systems.

CIRCLE NO. 393

Data-acquisition device uses portable calculator



Hewlett-Packard, 1507 Page Mill Rd., Palo Alto, CA 94304. (415) 493-1501. \$1375: 12 wks.

The Model 97S I/O is based around the HP-97 programmable printing calculator and uses BCD interfacing to gather data from a wide range of instruments. Data are manipulated by user-designed programs to produce a printed report. The calculator has 224 merged-program steps, a "smart" magnetic-card reader, three levels of subroutines, labeling, indirect and relative addressing, RPN logic and a fourregister automatic memory stack. Ten BCD input lines allow entry of data. Four output lines aid in the instrument control. These outputs may be set and cleared under software control.

CIRCLE NO. 394

Smart plotter uses built-in micro



Houston Instrument, 1 Houston Sq., Austin, TX 78753. Rod Schaffner (512) 837-2820. \$3495; 4 wks.

The DP-101 intelligent plotter contains a microprocessor for the generation of vectors, characters, arcs, circles and special symbols. The unit can be used for time-sharing and attaches to any RS-232C interface. Transmission errors are automatically detected. In addition to real time applications the plotter can be driven offline by a floppy disc or tape cassette. Included are rates of 110, 300 and 1200 baud and a 960-char data buffer. Step size is 0.005 in./step at a speed of 400 steps/s. The flatbed instrument, with vacuum holddown, uses 11 × 17-in. paper for an effective plot size of $10 \times$ 15 in.

CIRCLE NO. 395

Translator operates on serial data stream

Sigma Data Systems, 715 Torreya Ct., Palo Alto, CA 94303. Cliff Kirkhart (415) 494-1138.

A device which performs code translations on a serial data stream is completely self-contained, including a power supply. The serial data translator communicates via two RS-232 ports at up to 19.2 kbaud. Standard translations include ASCII. EBDIC. BAUDOT, and terminal control codes (such as cursor control). Other translations are available or may be userprogrammed. The unit contains an Intel 8035 microprocessor and up to 1 kbyte of EPROM. Since the unit communicates via serial ports, it is compatible with any host computer.

CIRCLE NO. 396



ELECTRONIC DESIGN 2, January 18, 1978

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CIRCLE NUMBER 93

DATA PROCESSING

Voice-data entry device is video/TTY compatible

Threshold Technology, 1829 Underwood Blvd., Delran, NJ 08075. Joe Simmons (609) 461-9200. \$13,500.

The Model 600 voice-data input system can be used as a direct replacement for either a video or teleprinter terminal. The Model 600 is compatible with RS232C, CCITT-V24 or 20-mA currentloop teleprinters. It allows full duplex communications via ASCII or other codes. Magnetic-tape mini-cartridge storage is provided to handle output character strings, training prompts, and speaker reference data. All voice recognition functions are controlled by the terminal. Included hardware consists of a speech-recognition processor, a 16-character alphanumeric display, two noise-canceling microphones, an operator console and a cartridge storage unit.

CIRCLE NO. 397

Thrifty computer handles small-business data



Info 2000 Corp., 20630 S. Leapwood Ave., Carson, CA 90746. (213) 532-1702. Under \$10,000; 2 to 4 wks.

The Model 2000 Business System for processing small-business data consists of a Z80-based computer, dual flexible-disc drives, high-speed printer, video terminal and business-applications software. The mainframe uses the S-100 bus and contains a Z80 CPU, up to 56 kbytes of RAM, 8 kbytes of EPROM, a filtered forced-air cooling system, and power supply. The printer is a 160-char/s, 132-column line device that provides all 95 ASCII upper/lower case alphanumeric and graphic characters. The video console displays all ASCII characters with dual-display intensity and protected fields at 19,200 bits/s.

CIRCLE NO. 398

Box checks and controls multipoint data network

Syntech, 11810 Parklawn Dr., Rockville, MD 20852. George Fritkin (301) 770-0550.

The System 5 provides a central computer site with the status of, and control over the performance of multipoint data communications network. The device can be used with both digital and analog networks and is independent of modem type. The device continuously scans all system components and automatically detects and reports faulty equipment. The report includes a hard copy printout of fault time, line number, remote address and failed equipment.

CIRCLE NO. 399

Data handler gives computers mass storage

August Technology, 2040 N. Maplewood St., Orange, CA 92665. (714) 998-1639. From \$3250; 8 to 12 wks.

A data-handling and recording peripheral, the Model 7701 provides multiple I/O channels, data-manipulation capabilities, and can record up to 580 kbytes on a Philips cassette. The unit interfaces with the HP 9800 calculators, the Wang 2200 and the IBM 5100 computer. Having an 8080 microprocessor and up to 64 kwords of memory, the 7701 provides up to 10 TTY current-loop, synchronous or asynchronous RS-232 ports and an 8-bit parallel data bus. Data may be recorded and played back through any port on the bus at different rates. Data may also be transferred among ports without recording.

CIRCLE NO. 403

Baud converter adjusts terminal to modern speed

Triformation Systems, 3132 S.E. Jay St., Stuart, FL 33494. (305) 283-4817. \$995.

The Model CB-1 is a baud rate converter which may be installed between computer terminals and modems conforming to the E.I.A. Standard RS-232-C to make them compatible with input or output speed. The device has a conversion range of 10 to 960 char/s and is capable of storing 2048 char. The unit comes equipped with an overflow alarm and indicator light.

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CIRCLE NUMBER 94





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CIRCLE NUMBER 96



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CIRCLE NUMBER 106

PACKAGING & MATERIALS

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Emerson & Cuming, Canton, MA 02021. Jeanne O'Brien (617) 828-3300. \$11.55/lb; stock.

Eccosorb CF-S is a castable silicone rubber that exhibits high loss in the uhf and microwave range. The product is magnetic with a high loss tangent. Also, it's nonconductive electrically, and can be poured or painted on almost any surface. When applied, the coating suppresses surface currents, reduced reflectivity of objects and lowers the Q of cavities.

CIRCLE NO. 405

Test system improves harnessing efficiency



T & B/Cablescan, 145 E. Emerson Ave., Orange, CA 92665. (714) 998-1961. From \$1850.

The automatic Random Work Director System, Model RWD-1000, helps harness makers maintain zero defects. increase productivity, eliminate fatigue and rework and reduce wireidentification costs. The system consists of a remote-control display, a mainframe for circuit interface and 50wire plug-in modules. The system identifies each conductor numerically, locates termination points with lamp indicators and performs continuity testing after final assembly. A programmed back-wired harness board is interfaced to the assembly to be made. When interfacing is completed, the system is activated on all circuits to instruct, verify and test.

CIRCLE NO. 406 ELECTRONIC DESIGN 2, January 18, 1978

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Types

Wire-wrapping kit's tool strips and wraps

O.K. Machine & Tool, 3455 Conner St., Bronx, NY 10475. Judy Camen (212) 994-6600.

A wire-wrapping kit, for prototype work, includes a wire-wrapping tool, a 50-ft roll of wrapping wire and prestripped wire in four lengths of 1 to 4 in. The kit's combination tool, Model WSU-30, wraps and unwraps #30 wire on 0.025-in. square pins after first stripping the wire with its built-in stripper.

CIRCLE NO. 407

Thermoplastic replaces rubber in bumpers



Ashland Products, 10910 S. Langley, Chicago, IL 60628. Bill Walter (312) 568-6500.

Made of thermoplastic instead of rubber, the soft and resilient bumpers can dampen vibration and cut noise. The bumpers are corrosion and abrasion resistant and they can be used up to 275 F and stay flexible to -60F.

CIRCLE NO. 408

Two conformal coatings meet MIL-I-46058C

Conap, 1405 Buffalo St., Olean, NY 14760. (716) 372-9650.

Two polyurethane conformal coatings for PC boards meet the requirements of MIL-I-46058C for Type UR coatings. Conathane CE-1165 is a twopart system for thin-film use on components and printed circuitry. The coating provides humidity resistance and hydrolytic stability. A tracer dye in the material becomes fluorescent under ultraviolet light as an aid to inspection. Conathane CE-1166 is a single component, moisture-cured polyurethane coating with similar properties.

Multilayer bus bars have square pins



Methode Electronics, 1700 Hicks Rd.,

Rolling Meadows, IL 60008. (312) 392-3500.

Square-staked and soldered pins are used in multilayer bus bars to increase reliability of wrapped wires. Square 0.025-in. pins, press fitted into round holes and soldered for positive connection, to make the bus bars have passed mechanical and environmental tests for shipboard use. Conductor layers are of electrical-grade copper and the pins can be supplied in phosphor bronze or beryllium copper.

CIRCLE NO. 410

Actual Size



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CIRCLE NUMBER 107

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Application notes

Bulletin board

Gauges and sensors

Semiconductor strain gauges, temperature sensors and integrated force/deflection sensors are discussed in a 20-page bulletin. Application notes, a specifications chart, installation instructions and ordering information are included. Kulite Semiconductor Products, Ridgefield, NJ CIRCLE NO. 411

Instrumentation amplifiers

The selection and application of high-performance instrumentation amplifiers are covered in a four-page brochure. Key specifications, error budgets, and circuit approaches are described in detail and typical applications are shown for biomedical and strain-gauge amplification. Micro Networks, Worcester, MA

CIRCLE NO. 412

Voltage regulators

A 198-page softback covers all aspects of power-supply design and helps engineers to select the proper regulator ICs and associated components for higher levels of system performance. Complete data-sheet information on all components and mechanical hardware is a major part of the book. A list of 66 different types of TI regulator circuits, a glossary of voltage-regulator terms and selection guide are also included. Texas Instruments, Dallas, TX

CIRCLE NO. 413

Memory testing

"Memory Testing with a Difference," 20 pages, discusses a number of factors involved in the selection of memorytest equipment, including timing resolution, automatic calibration, software, and analog performance. Teradyne, Boston, MA

CIRCLE NO. 414

Elpac Power Systems' µPS-35 microprocessor power supply now costs less than \$50 (100 qty).

CIRCLE NO. 415

Pro-Log has been granted Underwriters' Laboratory listing on all its PROM programmers, erase lights and personality modules.

CIRCLE NO. 416

Gettys Manufacturing has received Underwriters Laboratories' recognition for its N350 servo controller and panel assembly.

CIRCLE NO. 417

VIZ Test Instruments Group has cut prices on its WD-752A frequency counter from \$255 to \$200 and WD751A digital VOM from \$179 to \$150.

CIRCLE NO. 418

Texas Instruments has received FCCtype acceptance for its Model 2000 vhf-FM marine radiotelephone.

CIRCLE NO. 419

National Semiconductor slashes LM129 and LM199 series voltage reference prices by more than 40%. CIRCLE NO. 420

Bendix has introduced a microprocessor-based interactive drafting and mapping system for under \$40,000. CIRCLE NO. 421

Signetics' digital-to-analog converter IC prices have been reduced as much as 29%.

CIRCLE NO. 422

Cambridge Memories has reduced prices on its 370/STOR 168 add-on memory system for large IBM System/370 Model 168 computers by at least 9%.

CIRCLE NO. 423

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CIRCLE NUMBER 109 ELECTRONIC DESIGN 2, January 18, 1978 AUGAT

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Recorders

"The Recorder Book" illustrates strip chart, multipoint and circular chart instrument lines. Capabilities, prices, options and accessories of each model are listed. Honeywell Process Control Div., Fort Washington, PA CIRCLE NO. 424

FET data book

A 260-page FET data book contains an industry-wide cross-reference and substitution guide, Siliconix preferred parts selector guides, complete product specifications, geometry characteristics and mechanical data. Siliconix, Santa Clara, CA

CIRCLE NO. 425

Switches

Subminiature and microminiature switches are described in a 48-page catalog. The catalog gives complete specifications and includes a 4-page section on mounting information, hardware, and accessories. C&K Components, Watertown, MA

CIRCLE NO. 426

Connectors

A 180-page standard-line-connector catalog with a special selection guide covers how to order, materials and finishes, electrical data, contact arrangements and tooling accessories. Included are cutaway drawings and photographs. ITT Cannon Electric, Santa Ana, CA

CIRCLE NO. 427

Switching power supplies

Two brochures describe switching power supplies. The specifications of 12 models in the SMG series, rated from 8 to 2250 W, are detailed in one brochure. The MG switching-powersupplies brochure describes the specifications of products ranging from 50 to 500 W. Gould, Electronic Components Div., El Monte, CA

CIRCLE NO. 428

Processor storage system

Features of the Multimemory/148 processor storage system are offered in a data sheet. EM&M, Computer Products Div., Hawthorne, CA

CIRCLE NO. 429

Minicomputers

Four brochures describe a family of minicomputers. Each minicomputer's capabilities are written in understandable, nontechnical terms with color photographs showing each version. Cincinnati Milacron, Electronic Systems Div., Lebanon, OH

CIRCLE NO. 430

Digital panel meters

Technical specifications and prices for the Slimline Series II panel meters are given in a 12-page catalog. Nationwide Electronic Systems, Streamwood, IL

CIRCLE NO. 431

Temp sensing devices

Basic temperature-sensing methods using thermocouples, thermistors and resistance-temperature devices (RTDs) are shown in a 40-page catalog. Conax, Buffalo, NY

CIRCLE NO. 432

Computer systems

A 20-page booklet describes the use of computer systems in large business applications. Included is a section describing five major industrial applications, a catalog of peripherals, an overview of distributed processing, a list of available software and a description of HP's training support and maintenance programs. Hewlett-Packard, Palo Alto, CA

CIRCLE NO. 433

PM motors

"Permanent Magnet Motors and Integral Motor Tachometers for Servo Applications," 20 pages, offers all motor parameters and size specifications plus complete performance data with curve charts. Indiana General, Motor Products, El Paso, TX

CIRCLE NO. 434

Oscillators

A 44-page catalog covers frequency controls. Greenray Industries, Mechanicsburg, PA

CIRCLE NO. 435

Solenoids

A complete range of box frame, tubular, laminated and "c" frame solenoids for ac or dc applications is presented in a 60-page catalog. Dormeyer Mfg. Co., Chicago, IL

CIRCLE NO. 436

Rectangular connectors

Over 200 components of the MR Series connector family are described with full physical and electrical specifications in a catalog. AMP, Harrisburg, PA

CIRCLE NO. 437

Silicone products

A 40-page catalog covers hundreds of silicone, organosilicon, and silicon products and their uses in over 25 major industry classifications. Dow Corning, Midland, MI

CIRCLE NO. 438

Resistors

Positive-temperature-coefficient resistors are covered in an eight-page catalog. Murata, Marietta, GA

CIRCLE NO. 439

Memories

Six, two-page data sheets describe DEC PDP-11 compatible memories, including planar (add-in) and modular (add-on) memories in capacities from 12 kwords to 4 Mbytes. The bulletins include design features, specifications, and addressing and operating data for PDP-11 users. Monolithic Systems, Englewood, CO

CIRCLE NO. 440

Breadboards

Microcomputer boards, printed circuit boards and off-the-shelf designer breadboards are covered in a six-page brochure. Artec Electronics, San Carlos, CA

CIRCLE NO. 441

Display calculator

Important features of the 2102 display calculator, including its full 12digit capacity, decimal selection for add mode, 0, 2, 3, 4, 6 or floating decimal, and a complete 4-key memory, are outlined in a data sheet. Facit-Addo, Greenwich, CT

CIRCLE NO. 442

Noise-blanking circuitry

Noise-blanking circuitry available as an option with broadband amplifiers, designed to reduce noise and/or gain on a rapid, repetitive basis, is described in a bulletin. Amplifier Research. Souderton, PA

CIRCLE NO. 443

Ribbon connectors

Ribbon-contact rack and panel connectors are described in a 20-page catalog. TRW Cinch Connectors, Elk Grove Village, IL

CIRCLE NO. 444

Foils

High-purity electroformed copper and nickel foils and thin metals are described in a literature package. Gould, Foil Div., Cleveland, OH CIRCLE NO. 445

Connectors and cables

A 40-page catalog includes sections on patching, connectors and cable assemblies. Trompeter Electronics, Chatsworth, CA

CIRCLE NO. 446

Rotary switches

Nine standard, stock configurations of Rotocode rotary switches in a choice of nine output codes from 10 to 60 positions are featured in an eight-page catalog. Application data and dimensional product drawings are provided. Cherry Electrical Products, Waukegan, IL

CIRCLE NO. 447

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ELECTRONIC DESIGN 2, January 18, 1978

Across the desk

(continued from page 7)

or elements times the cycle time of the clock. Thus, the MN3005 you describe has only 2048 stages or elements of delay, and 4096 transfers.

The clarification becomes important when comparing different technologies. For example, Reticon Corp. markets a 2000-stage delay element, R5101, with comparable time-delay capability; however, this is a four-phase CCD with 8000 transfers.

Also, you imply—erroneously—that charge-transfer devices cannot be connected in series without intermediate amplifiers and low-pass filters. The devices are sampled devices, with input-aperture times substantially less than one microsecond. Reticon's SAD-1024, for example, has an aperture time of approximately 100 ns. Furthermore, the SAD-1024 permits unity gain, so one can couple the output from one to the input of the next.

Inserting a low-pass filter degrades the performance, because a $(\sin \pi f/fc)/(\pi f/fc)$ frequency factor applies any time the stair-step sampled nature of the signal is converted to a smooth analog signal, whether between stages or not. Output filtering is desirable and usually required, but only one such filter should be applied, and that at the output. Interstage filters will compound the frequency roll-off unnecessarily.

> Robert R. Buss Staff Engineer

Reticon Corp. 910 Benicia Ave. Sunnyvale, CA 94086

Brother of laetrile

I have picked through the bones of contention in your laterile controversy and my X-ray shows two most important bones have not been dealt with.

The first is public fraud. You may assert that laetrile can't hurt anyone, and so can the seller of snake-oil. For the medicine man knows that the little amount of whiskey he has spiked his concoction with may get you high enough to make you feel good for a little while and get you to come back for some more. But there is no cure for anything, and he says there is and takes your money under false pretenses. That's FRAUD! We have laws that can be invoked to protect the innocent and the gullible from such lying charlatans, and they apply to laetrile promoters.

The second "bone" has to do with civilian responsibility for keeping government honest. This country has a dread social disease, NIWSST-Nobody Is Watching So Screw Them. No government agency will work properly if not constantly monitored, and likewise no individual will do right unless constantly monitored by friends, family, churches, bosses, the Law, etc. We make government agencies because we know they can be stronger in righting wrongs than individuals. To destroy our bureaucracies is a retrograde step that will make things as bad as they were when we found it necessary to make bureaus. If our "computer design"-in this case, the FDA-has a glitch and won't fulfill a function, don't destroy the computer, deglitch it!

Nathaniel Cunningwell Managing Director

Computronics Engineering 7225 Hollywood Blvd. Los Angeles, CA 90046

Daughter of laetrile

I am absolutely ashamed that a spokesman for my profession would criticize the American medical profession. Everyone knows how editors will write just anything to get people to read the ads in their publications. The facts would seem to indicate your Editorial in the July 19, 1977, issue of ELECTRONIC DESIGN is such an article.

The wife of a colleague of mine had terminal cancer. Three clinics-one in San Diego, one in Los Angeles, and one in San Francisco-independently reached the same conclusion: She would die within six months, but a heroic attempt to save her life could be made. It was important that the treatment start as soon as possible so that if modern medical research discovered a cure, there would be ample time to save her life. Unfortunately, modern medical research didn't come up with a cure, but my friend's wife went to Mexico, one of 26 countries where laetrile is accepted. She is still alivesix years later.

Clearly, my colleague's wife is an exception. There are probably no more

than 100,000 "exceptions" in the U.S. today. But there are a good many more who choose the treatment provided by modern medical research and generate additional funds for research as a result of their choice.

Come on, George. You know that it is the number one responsibility of a professional to raise money for his profession. Let's hope that laetrile backers fail so that the electronics industry will be able to supply additional equipment for cancer research. Steven Riggin

1316 Palmer Ave. Camarillo, CA 93010

Misplaced Caption Dept.



After you again trace all circuit connections and review the manual, you are ready to apply power to the \$3000 klystron tube.

Sorry. That's Hans Memling's "Portrait of Martin van Nieuwenhove," which hangs in the Hospital of Saint John, Bruges, Belgium.

Creative Growth Games—Eugene Raudsepp with George Hough, Jr., Princeton Creative Research, 10 Nassau St., Princeton, NJ 08450. Paper. 224 pg. \$3.95.

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1.1.1

Block diagram of MN1400 with on-chip, 1024x8-bit ROM.



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Power Supply		+ 5V	+ 5V	+5V	+ 5V
Instruction Cycle Time		10µs	10µs	10µ s	10µs
Instruction	Set	75	57	68	75
Instruction Memory	Instruction ROM	Internal 1024 x 8 bits (8192 bits)	Internal 768 x 8 bits (6144 bits)	External 1024 x 8 bits (8192 bits)	External 2048 x 8 bits (16384 bits)
Total on Chip RAM		64 x 4 bits (256 bits)	32 x 4 bits (128 bits)	64 x 4 bits (256 bits)	64 x 4 bits (256 bits)

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