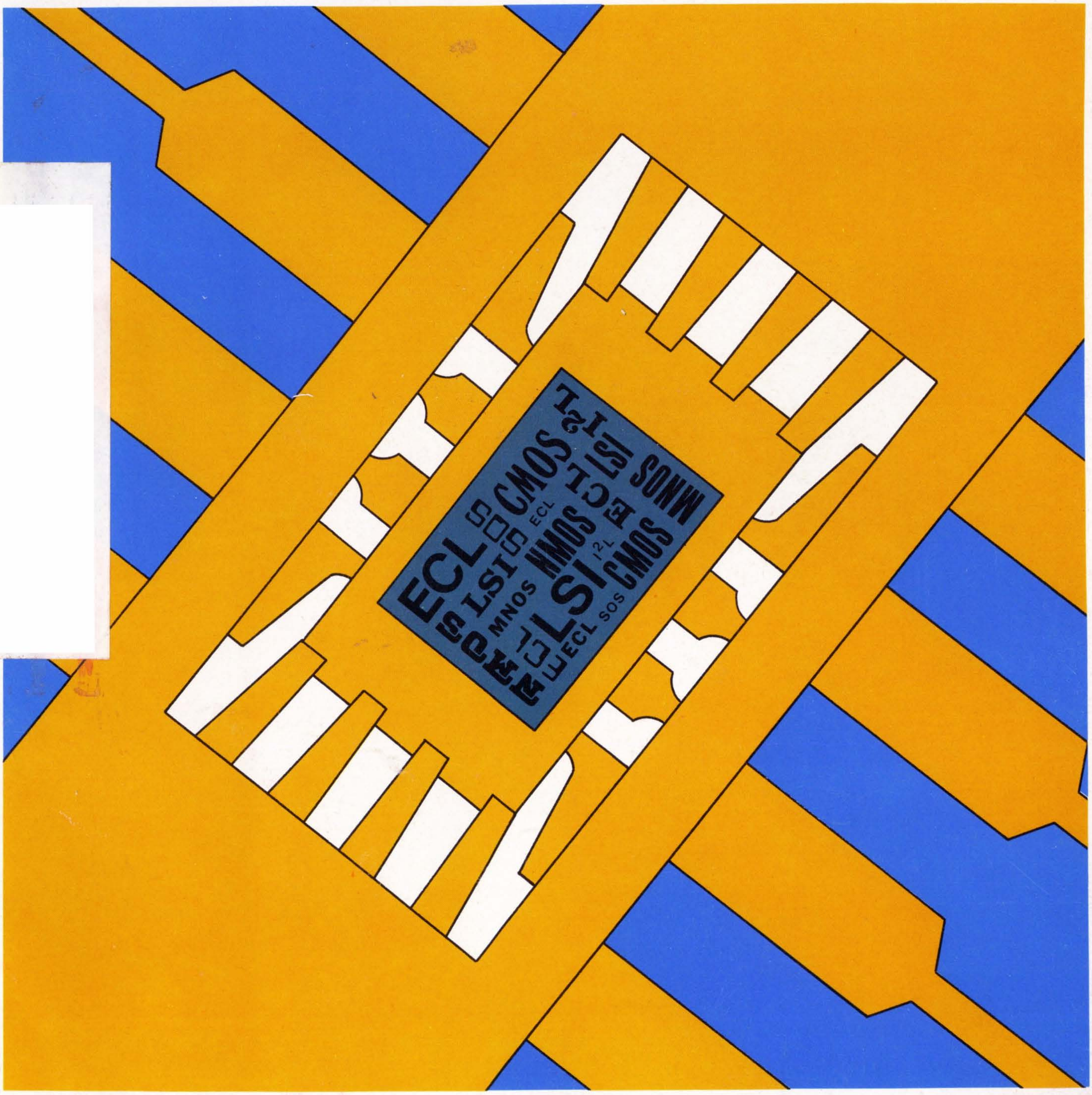
Electronic Design®

FOR ENGINEERS AND ENGINEERING MANAGERS

VOL. 25 NO. 7

MARCH 29, 1977

IC performance is improving with new and better fabrication techniques. Advances in double diffusion, ion implants and the polysilicon process are increasing digital-chip speeds and circuit density. Dielectric isolation cuts cross-talk to a minimum in linear circuitry. For details of the latest IC technology, turn to page 42.



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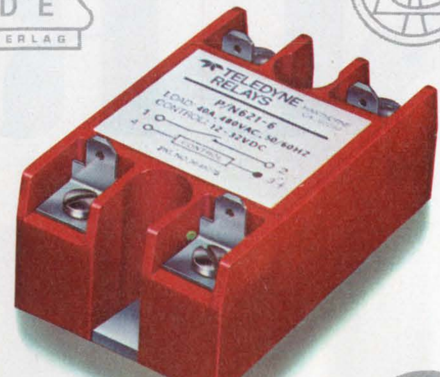
CIRCLE NUMBER 2

SSR UPDATE

Our International Connection



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- 480VRMS output voltage rating for reliable 3-phase switching
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CIRCLE NUMBER 3

VOL. 25 NO. 7

Electronic Design

FOR ENGINEERS AND ENGINEERING MANAGERS

MARCH 29, 1977

NEWS

TECHNOLOGY

PRODUCTS

DEPARTMENTS

Cover: Cover designed by Art Director Bill Kelly.

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CIRCLE NUMBER 9

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Across the Desk

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We have openings at our home office in Rochelle Park, NJ. Call Mike Elphick at (201) 843-0550.

New but misleading

In our new-product article on Figaro Engineering's semiconductor gas sensor (ED No. 1, Jan. 4, 1977, p. 162) we goofed when we said: "The gas sensor is claimed to be the first and only UL-approved detector of natural and propane gas." What we should have said was "The gas sensor is the *heart* of Craft-Alarm, the first and only UL-approved detector of natural or propane gas."

Boosting R&D output is a matter of opinions

Al Cookson's timely comments on boosting R&D output (ED No. 25, Dec. 6, 1976, p. 100) were very refreshing and directly to the point.

Hopefully, Mr. Cookson will not object if I add an additional facet that has always been of special interest to me. Information retrieval is an often neglected, but valuable, tool for boosting R&D output, in addition to reducing unnecessary engineering time and expense. Mr. Cookson perhaps intended this as a specific for accomplishing point no. 2 of his list of "fundamentals." However, I feel that this area is so important that it bears emphasizing.

It has been my personal experience over more than 27 years of patent practice that engineers, when assigned a new project, just can't wait to grab a pencil and draw a line. Rarely do they make an effort to determine whether the same or similar lines have been drawn previously.

However, many company technical libraries, as well as conveniently located public libraries, have excellent collections of textbooks and trade periodicals readily available for examining the general state of the art. Lately, terminals for "on-line" information retrieval have also become readily accessible.

Many companies have internal patent departments with large collections of prior art. Very often, in limited fields, these collections may be more extensive than references available in the U.S. Patent Office Search Room. A visit to the patent department soon after a project is initiated should be a company must.

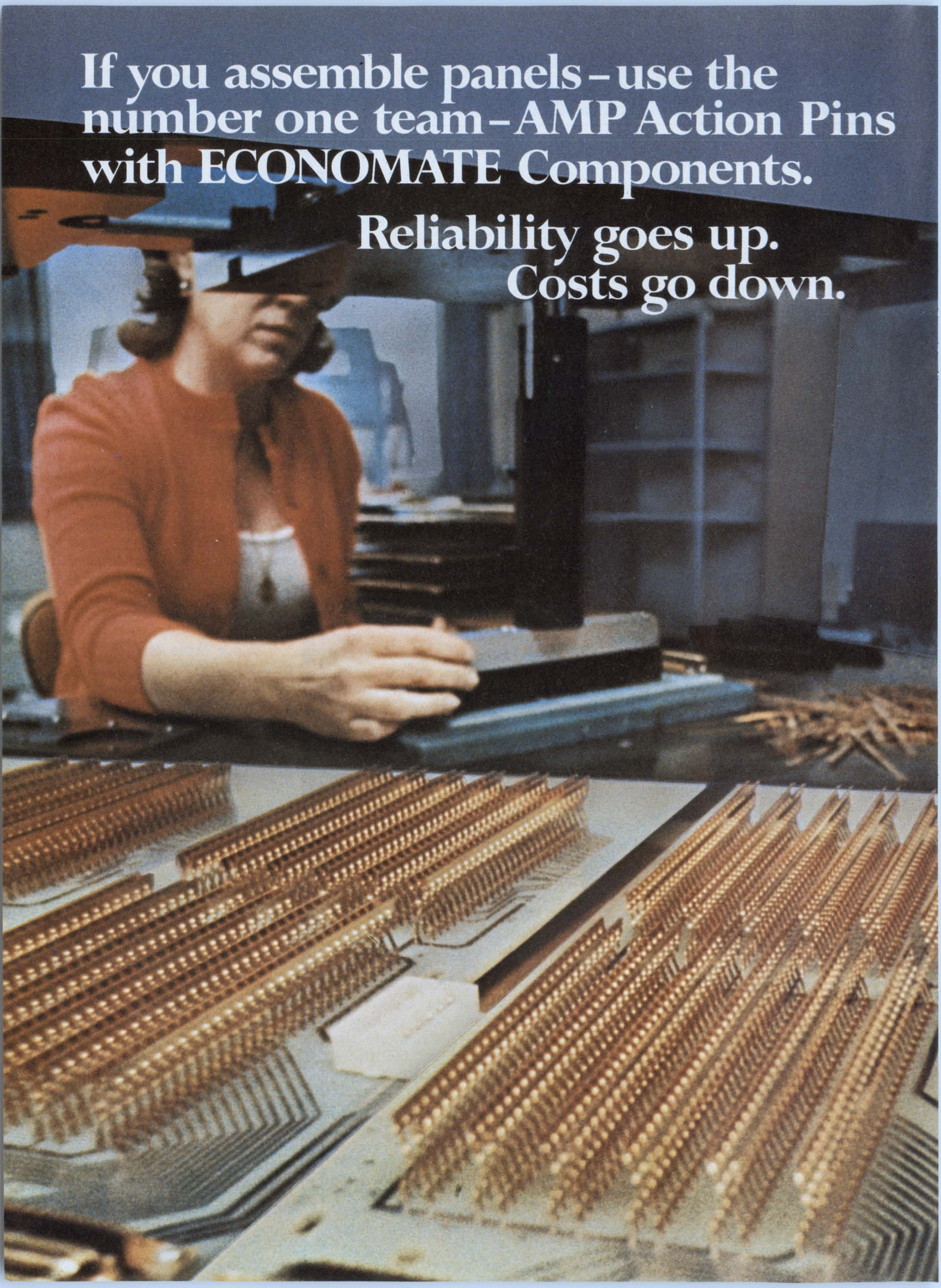
Arnold J. Ericsen
Manager
Patent Law Dept.
Allen-Bradley Co.
1201 S. Second St.
Milwaukee, WI 53204

Al Cookson's ideas on boosting R&D output represent the narrow view of a large corporation clearly dedicated to marginally improving its existing products and perpetuating its older technologies.

His suggestion to beware of transient inventors and promoters of inventions is oblivious to the fact that half of the significant

(continued on page 14)

Electronic Design welcomes the opinions of its readers on the issues raised in the magazine's editorial columns. Address letters to Managing Editor, Electronic Design, 50 Essex St., Rochelle Park, NJ 07662. Try to keep letters under 200 words. Letters must be signed. Names will be withheld on request.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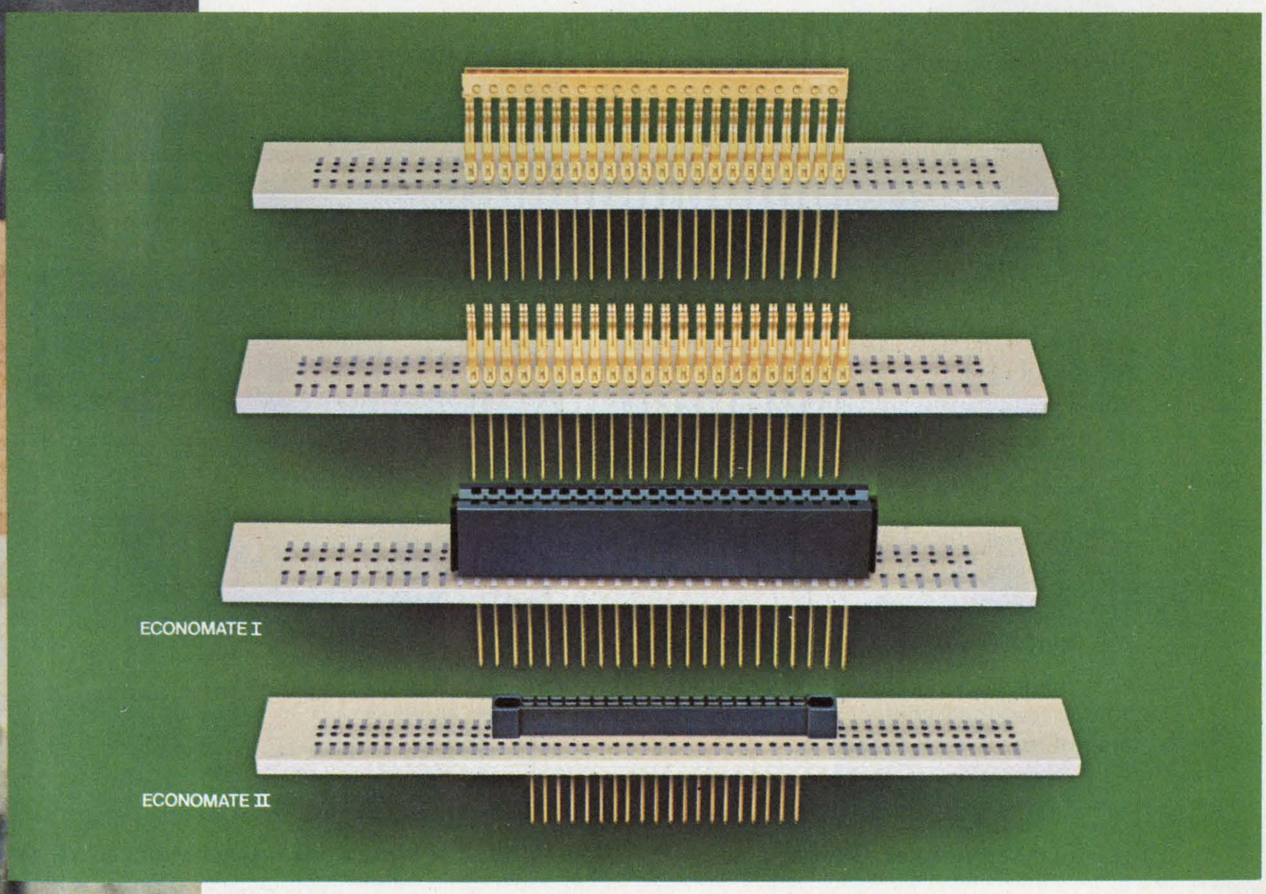

TRANSISTORS

A WEALTH OF WIDGETS RIDES AGAIN.

And now, the continuing story of transistors: those funny little devices that everybody needs but nobody invites to lunch.

When last we left you, Fairchild was busily pumping out a plethora of power, a deluge of Darlingtons and a quantum of quads, to name but a few.

In today's ad, we continue the legacy with a new product line and a few wrinkles on some old favorites.

THE EVER POPULAR TO-3

If you're in the market for TO-3 power transistors, we can show you how to get top quality, fast delivery and good prices with a single phone call. Fairchild produces over 200 of the most popular JEDEC and house numbers. Ranging from 2 to 50 amps for transistors and 2 to 20 amps for Darlingtons. With VCEOs up to 350 volts. And extensive NPN and PNP capability. Tack on the most competitive pricing in the business and you've got a pretty good reason to call Fairchild next time you get lonesome for a good TO-3.

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Do yourself a favor. Take a look at our top-of-the-line 2N6251. Then compare it with anybody else's top-of-the-line switch. Ten times out of ten, Fairchild performance is going to come out on top.

YOU'VE SEEN THE PACKAGE, NOW READ THE BOOK.

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All this is made possible by a revolutionary Fairchild process called TWN. Now we've written a brochure about the wonders of TWN and how it makes our new TO-92 the most reliable package ever developed. Drop us a line and we'll send you a brochure.

CIRCLE NUMBER 10

ACROSS THE DESK

(continued from page 7)
inventions that provide new technology and employment in this country are made by individuals outside big, established corporations.

His other suggestion against the brilliant invention shows the near-sightedness of his commitment to the short-term profit result and lack of motivation for serious innovation. In the last 14 years his company's standing for products honored is at the bottom of the list in a recent survey *(Industrial Research,* October, 1976, p. 24)—only for 2 out of 1400 products by 100 companies and even fewer from the output of companies much smaller in size.

As long as corporations keep putting their money into improvements of marginal products and keep neglecting the most prolific sources and goals of innovation, we will continue the waste accompanied by grand pronouncements of boosting R&D output with the management (whip) approach.

Let's face it: With Al Cookson's point of view we will wind up having large corporations with super-efficient R&D managements but with increasingly marginal and inefficient products. He could save a good portion of his R&D budget by running down to the Patent Office and looking over the most recent inventions and innovations by individual inventors that may fill his bill. Or he can consider hiring individual inventors or small business firms engaged in R&D to obtain the biggest bang for his buck.

James Constant
RCS Associates, Inc.
1603 Danbury Dr.
Claremont, CA 91711

I would not have given much thought to Al Cookson's article had it been titled ". . . Boosting D Output." However, the implication that his thoughts should be followed by R&D managers is erroneous. This is not the way to run a true R&D "railroad."

Al Cookson's management philosophy does not apply to the management of basic research, applied research, or even advanced development. Had he been at Bell Laboratories instead of Jack Morton we would not have had the transistor today, or had he been at the Office of Scientific Research and Development instead of Vannevar Bush, we would have lost World War II.

Unfortunately, the article does not show the efficiency of ITT's R&D. It would be interesting to speculate what that efficiency would be if Mr. Cookson used a more enlightened and holistic management philosophy.

The 2% of gross sales that ITT invests in R&D cannot compare with Hewlett-Packard's 9.4%. *Business Week*'s criterion that high-technology companies spend more than 5% excludes ITT from this league—probably due to, or because of, its management philosophy.

Remember what happened to the railroads, because management did not realize that they were in the transportation-system business, and did not know what "research" meant.

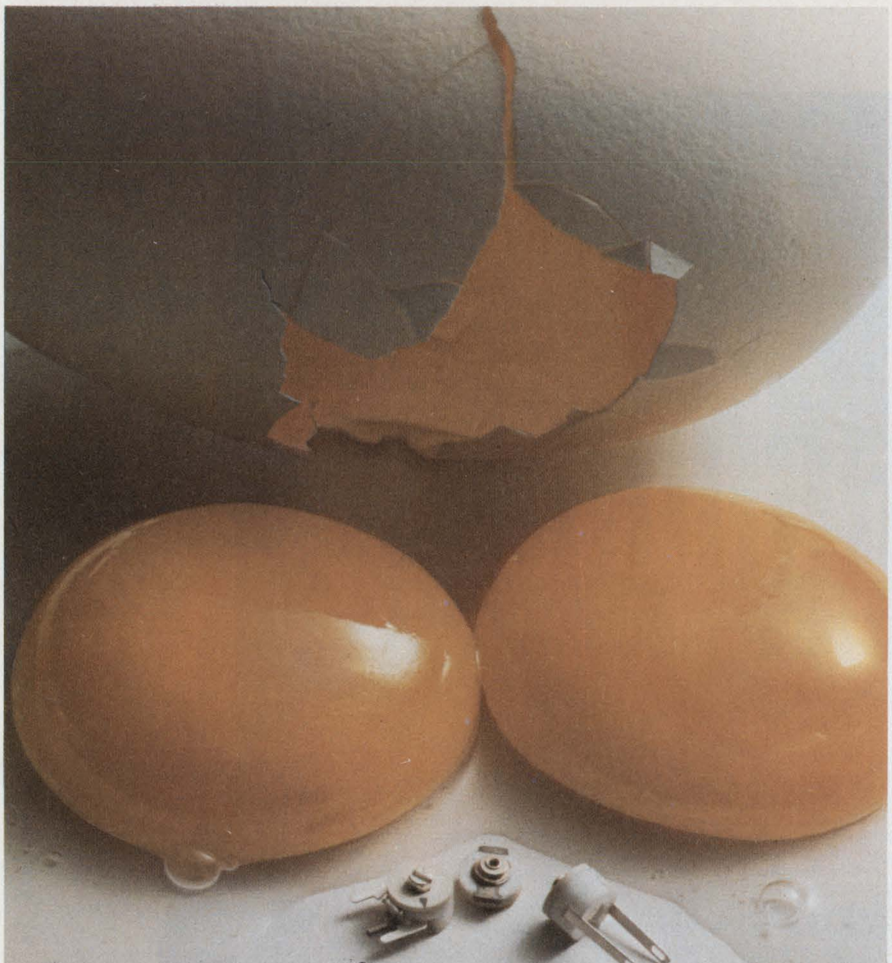
J. S. Zumbado
Electronics Engineer and
Student of R&D Management
15505 Norman Dr.
Darnestown, MD 20760

Mr. Cookson replies

I would only like to quote from a recent article by Jenkin Lloyd Jones, Editor of the *Tulsa Tribune*: "As I have grown older, I have become more and more intrigued with what works, and this is a very unsettling form of inquiry for much of what ought to work doesn't and much of what shouldn't work does." We at ITT have honed our R&D management approach for many years and it works for us. In 15 years (1960 to 1975), our sales have grown by 1400% ($800-million to $11,400 million) and our net income by 1300% ($30-million to $400-million).

Although we have made many acquisitions, a substantial percentage of this growth has been internally generated and dependent on successful R&D. However, in a field as difficult and complex as R&D management, there fortunately exists a great range of competitive philosophies that are constantly being tried by good companies,

(continued on page 16)



ACROSS THE DESK

(continued from page 14)
large and small. In this free, highly competitive society, the optimum approach will succeed in time and its proponents will prosper.

Misplaced Caption Dept.

Let go of me! I'm late for a design review.

Sorry. That's "Samson and Two Philistines," by an unknown sculptor after Michelangelo. It hangs in the Frick Collection in New York City.

Full DACs are here

We were wrong in saying that single-chip conversion circuits, complete with reference, ladder network and output amplifier, were just emerging (ED No. 1, Jan. 4, 1977, p. 36). In fact, though many engineers prefer conversion chips without a built-in reference (so that, for example, several converters can share a common reference or a d/a converter can be used as a multiplying DAC), complete monolithic converters have been available for many years. The Precision Monolithics monoDAC-01, for example, a full 6-bit, single-chip DAC, was introduced in 1970. A 10-bit DAC, the monoDAC-02, was introduced in 1972. Both have internal reference and output op amp on chip.

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At other semiconductor companies, ROMs are only one of dozens of diverse products competing for attention. At EA, ROMs are the very heart of our business. So your order for ROMs receives the highest priority. You can expect very rapid delivery. And very low prices—because we've learned to fine-tune our production process to a peak of efficiency.

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electronic arrays, inc.

CIRCLE NUMBER 15

News Scope

MARCH 29, 1977

Tracing signatures finds faults on μP boards

To track down faults on printed-circuit (PC) boards containing microprocessors, two firms have come up with similar approaches. Both borrow the cyclic-redundancy-check (CRC) technique from digital communications. This method, which guarantees error-free digital communications, has been refined into what John Fluke Mfg. Co. Inc.'s Trendar subsidiary calls "merged sequencing" and Hewlett-Packard Co. dubs "signature analysis."

Cyclic-redundancy checks are applied by feeding a digital data stream through a shift register that has feedback taps. The feedback signals are applied to a modulo-2 summing network at the input to the shift register. Since the transmission is coded, the resulting sum is known; but an error in the transmission causes an error in the sum, and can be detected.

In PC-board testing, a known data stream is fed into the circuit's input and a shift-register measurement made at each node of a known-good board. A signature is yielded for each point on the board in much the same way as feeding an analog signal into an analog PC board, under fixed conditions, yields a repeatable waveform at each node on the board. By tracing faulty signatures back through a board, as in tracing erroneous waveforms through a troubleshooting tree, a technician can locate the faulty node precisely.

Merged sequencing is incorporated in Trendar's new automatic board tester, the Model 3040A, which the firm calls the first low-cost system designed specifically for boards containing microprocessors. The system, which is priced from $60,000 to $95,000 depending on options, drives a board under test with pseudorandom data streams at rates up to 5 MHz. To test the microprocessor itself, which requires data in the proper syntax and cannot employ pseudorandom signals, user-defined test sequences can be processed at rates up to 1.5-million input words per second.

These bit patterns are used in go/no-go board testing. If the board fails, the test-system operator is directed to probe individual nodes. The tester determines the signature at that node. If the signature does not match the stored known-good signature, the tester directs the operator to probe nodes further back on that signal path to determine the point at which the fault first appears.

Earlier Trendar testers used a similar troubleshooting-tree approach to isolate faults, but simply counted transitions at each node. The more sophisticated merged sequencing measurement is more apt to find errors, says Don Allen, vice-president of marketing at Trendar, adding: "Transition counting approaches the error-detecting quality of CRC, but doesn't reach it."

Regardless of the subtlety of the fault, signature analysis yields a 99.998% certainty of spotting a faulty bit stream, according to Hans Nadig, project manager at HP's Santa Clara division. To help engineers apply the technique, HP has introduced the Model 5004A signature analyzer, a $990 instrument designed for field-service as well as laboratory use.

The signature analyzer is applied to manual troubleshooting much like the Trendar automatic system for fault isolation.

One major difference is in HP's readout: a nonstandard hexadecimal character set (0123456789ACFHPU) is compatible with seven-segment displays and avoids the difficulty of differentiating between the 6 and the b of the usual notation (0123456789AbcdEF).

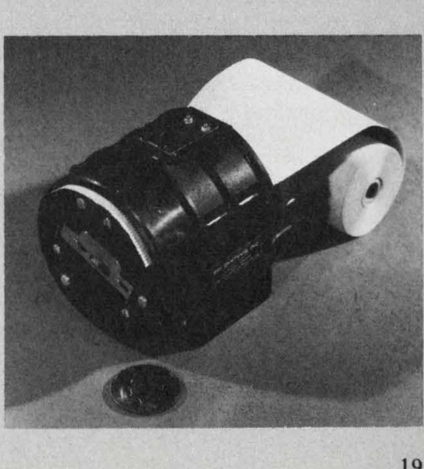
The only difficulty with signature analysis, notes Nadig, is that the product must be designed from the beginning with testability and signature analysis in mind. "From my experience, retrofitting to employ signature analysis into existing equipment doesn't work," says Nadig. When a product is in development, it is simpler to incorporate the necessary data-stream generators into the software and provide a means for breaking feedback loops to prevent a fault from disturbing properly functioning nodes.

Novel rotary printer prints 2200 characters/s

Weighing only 3 lb and with just nine moving parts, a printer is still able to bang out 2200 characters per second because of its unusual rotary printing mechanism.

The unique and simple device, introduced by SCI Systems, Inc., Huntsville, AL, doesn't take up too much space—4 × 5 × 9 in. But even so, it can print 136-column computer data with standard 10-character/in. spacings. A 5 × 7 dot matrix is used to form characters, and print resolution is 70 lines/in.

The rotary-design printer con-consists of three main elements: a drive unit, a 400-ft roll of paper, and a printhead, which is the one replaceable part—but has a life exceeding 25-million characters. One small dc motor drives all elements of the printer: it belt-drives a central shaft, which supports both a code wheel at the rear of the drive unit, and the printhead at the front. A single-paper-feed roller is driven from the shaft through a



worm-gear arrangement.

The housing consists of several molded plastic parts: end plates, top and rear covers, and a writing platen that surrounds the printhead. An electronics board in the housing drives the motor and stylus assemblies.

The printhead contains three multiwire stylus assemblies mounted 120° apart on a plastic rotor and protected by a molded cover. A slip-ring disc forms the rear structure of the printhead and is connected through flexible etched cables to the styli themselves. Slip-ring brushes connect the printhead to the drive electronics.

The printer uses electrosensitive paper, which is reportedly less expensive than conventional Xerox copy and available from a number of companies, including the Nicolet Paper Co., De Pere, WI.

The paper is inserted through the writing platen and formed into a 120° arc by a snap-down top cover. In operation, the drive roller continuously pushes the paper through the unit. Centrifugal force extends the stylus wire through slots in the printhead cover, and into contact with the platen and paper as the head rotates.

Constant-size characters are formed regardless of motor speed because writing pulses are timed directly from the code wheel. Each stylus assembly prints a column of characters as it sweeps over the paper, so the head prints three columns per revolution. A printed line can be any length—132 columns may be printed just as easily as 40 columns.

The unit sells for about $300 to OEMs (in large quantities) and under $1000 for single units, including power supply and cabinet.

Later this year, SCI plans to introduce a printer that will print on standard 8-1/2 in.-wide paper. It will produce 80 characters/line at 10 characters/in., at a rate of 4000 characters/s.

CIRCLE NO. 318

Wang small business computer line expanded

"To double the range of its current small Series 2200 business computer line," Wang Laboratories, Lowell, MA, has introduced the first minidiskette-based desktop computer for small business, the PCS II; two larger computers, the WCS/25 and the WCS/40; and new interactive terminals, printers, IBM-compatible diskettes, multiplexers and communications controllers.

Besides minidiskettes, the expanded line makes extensive use of microprocessors, a new terminal-access method (TAM) and "mini-front-end" capabilities that permit intelligence sharing by multiple terminals in the WCS/25 and WCS/40.

A self-contained unit, the PCS II includes a large 1024-character CRT screen; a typewriter-like keyboard with separate numeric keypad and 32 special-function keys for data entry and control. Its high-speed processor has two memories, and the 8 kbytes of user-available memory is expandable to 32 kbytes.

In its basic configuration, the WCS/25 includes a Series 2200 processor with 24 kbytes of user memory and 42.5 kbytes of read-only operating system memory to store Wang's extended BASIC language interpreter. It also features two diskette storage devices, a 120-characters/s printer, a Model 2236 MXC μP-based "mini-front end" controller, and three Model 2236 interactive terminals.

The WCS/40 is built to meet higher volume and more stringent form-filling and form-processing requirements than the WCS/25.

A fully equipped PCS II, including a high-speed printer, costs about $9100. A typical WCS/25 is priced at under $30,000, and a WCS/40, at $48,950.

CIRCLE NO. 319

Electric power may come from thermal noise

A long-unwanted phenomenon of electronics stands a good chance of becoming a useful energy producer—thermal noise voltages generated in resistors by elevated temperatures. To produce electrical power, a system based on this innovation will take the form of a thin, flat plate that theoretically can produce about 500 W per square meter of surface exposed to a hot sun.

Proposed by inventor Joseph Yater of Energy Unlimited, Lincoln, MA, the new energy-producing concept was the only one designated suitable for funding by the National Bureau of Standards out of more than 4000 ideas examined. With a $40,000 grant from the Energy Research & Development Administration, Yater is proceeding with the initial stages of development.

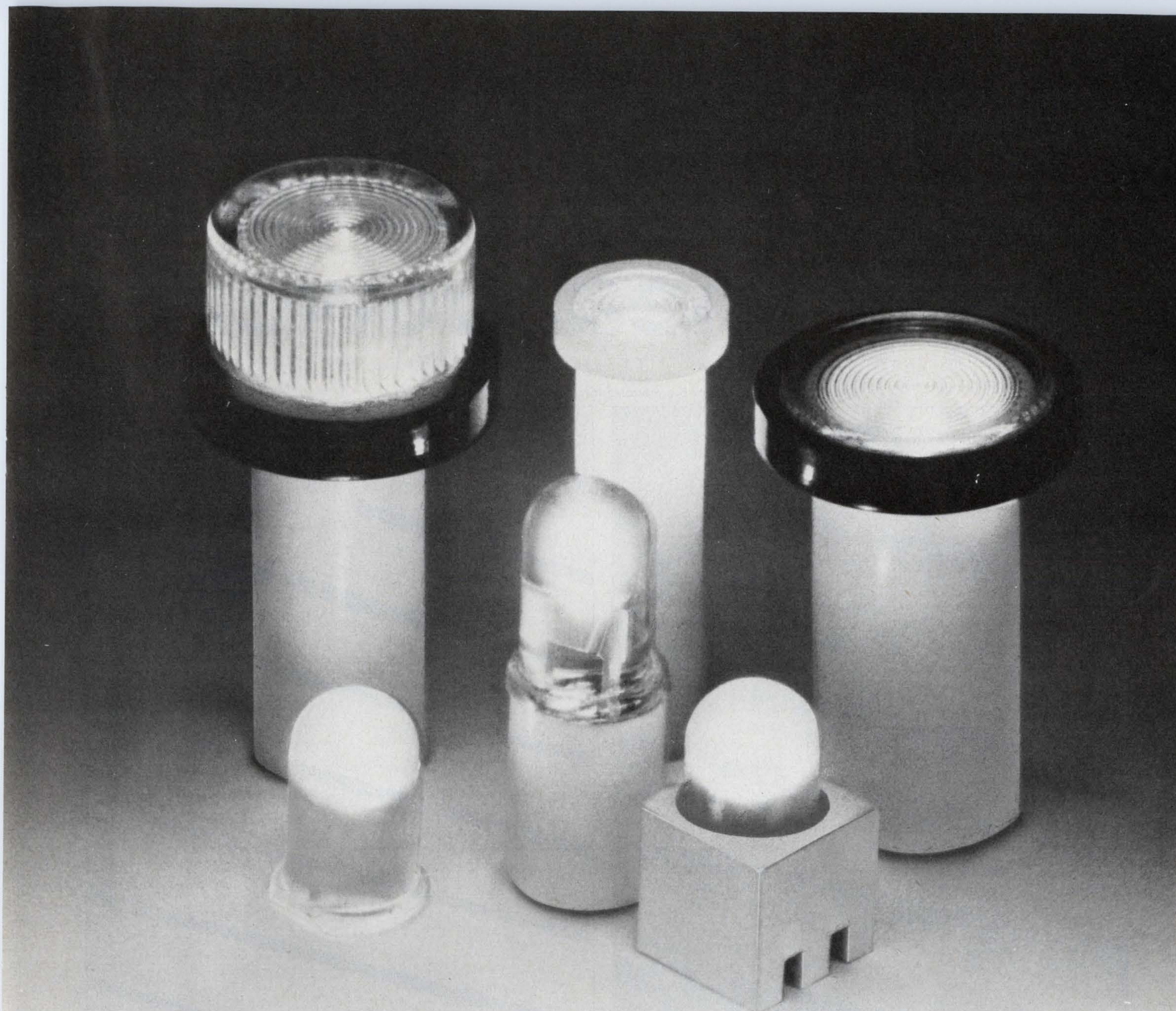
There are three components, Yater explained to ELECTRONIC DESIGN. One is a planar, insulating substrate that holds the other two key elements. On the upper, or hot side, resistors are exposed to either the sun or another heat source. On the bottom side, planar diodes rectify the noise voltages produced by the resistors. The resistors are connected in series, the diodes in series-parallel.

The key to system operation is the fact that the noise voltages due to the thermal agitation of electrons in the resistors cover a band of frequencies up to 1 THz ($=10^{12}$ Hz). These voltage fluctuations are coupled to the diodes through the capacitance formed by the resistor-insulator-diode sandwich structure.

News Briefs

Soon to be added to the growing list of μP-based-computer suppliers is Heath Co. of Benton Harbor, MI. Parts of the extensive product line Heath plans to offer are said to be coming from the Digital Equipment Corp. catalog. And both Heath, by far the leading supplier of electronic kits, and the Maynard, MA, minicomputer maker have clamped tight security on their product plans. Introduction appears to be set for August at the Personal Computing '77 Consumer Trade Fair in Atlantic City, NJ.

The first of its PIC 1650 single-chip microcomputers should be shipped by General Instrument Corp.'s Microelectronics Division in Hicksville, NY, within the next few weeks. The 1650 (see ED 23, November 11, 1976, p. 38) is expected to sell for $6 to 7 in moderate volume and less than $5 in large quantities. Delivery quotes are about 90 days, including ROM mask-making time.



The end of the incandescents.

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CIRCLE NUMBER 16

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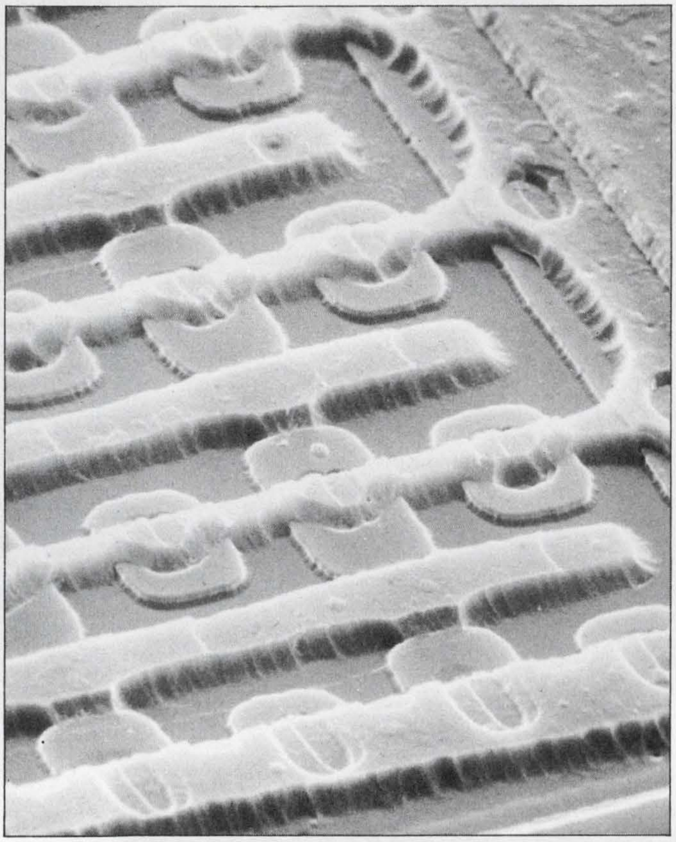
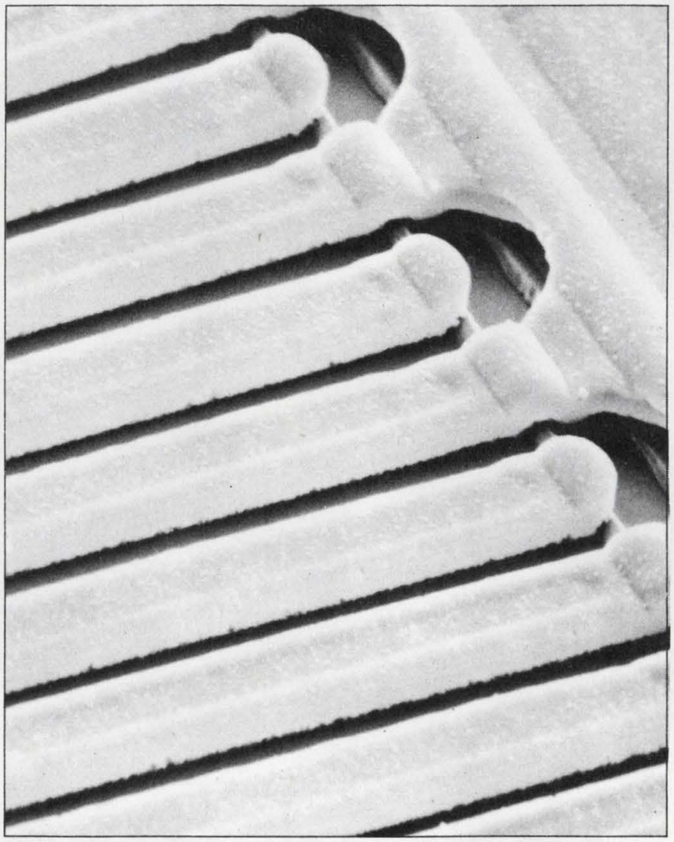


Conventionally-etched die metalization. Etched scalloping in metal fingers produces current crowding and resultant failure through metal migration.



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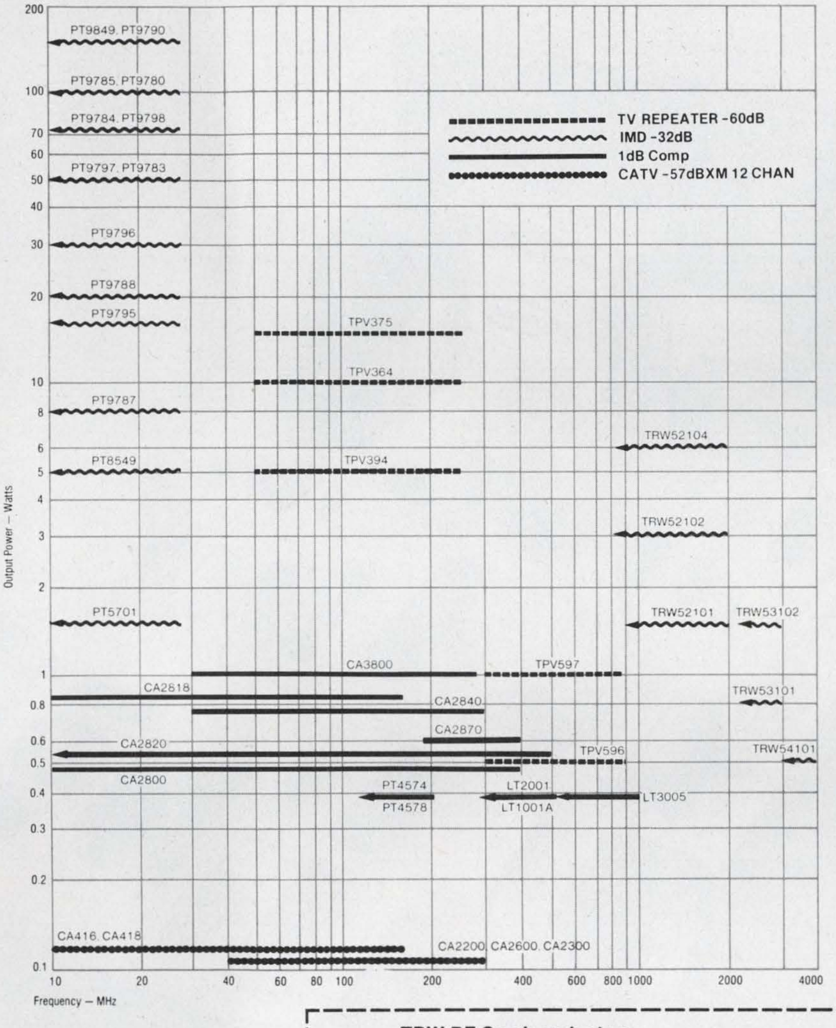

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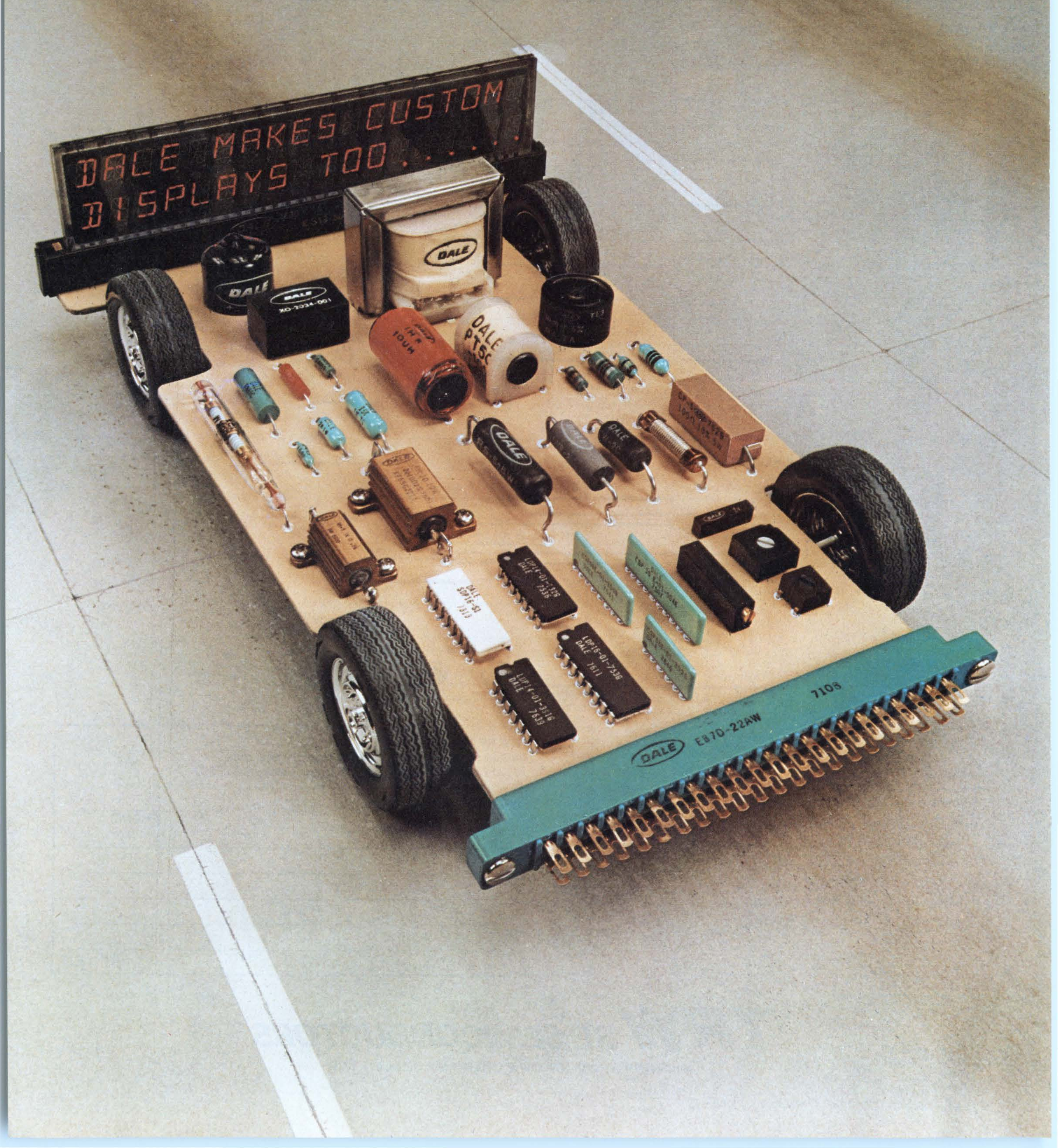
How to get more mileage from discrete components.



News

AT THE INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE

Users and manufacturers don't speak the same μP language

"We're fed up with trying to master a new language every time another manufacturer develops a microprocessor."

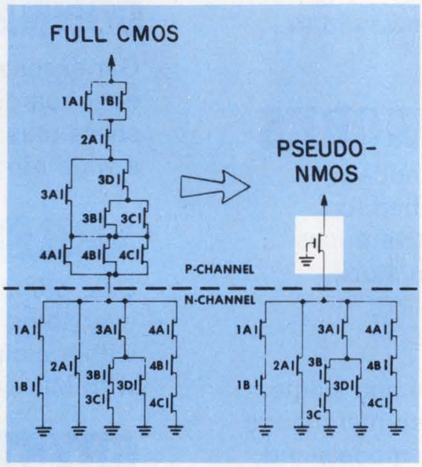
That's what many users were saying at a panel discussion on standardizing low-end microprocessors at the 1977 International Solid-State Circuits Conference in Philadelphia. Attendees let loose their ire at the μP manufacturers, who did little more than describe their available processors.

If anything, the *lack* of standardization from vendor to vendor was thrown into the limelight.

Those who attended another panel discussion on high-performance microprocessors were not as upset with the lack of standarization. But the vendors, who in the past would let the proverbial cat out of the bag, revealed little in the way of upcoming products.

Within low-end product families most vendors offer compatibility from model to model. For example, Joel Cyprus of Texas Instruments (Dallas, TX), Gordon Smith of Rockwell (Anaheim, CA) and George Reyling of National Semiconductor (Santa Clara, CA) discussed their companies TMS-1000, PPS-4 and COPS Series, respectively. But, there is no easy way to switch from one series an another, protested irate users, adding that a "universal" development language is needed, which can be shared by everyone.

The following editors contributed to this report: Dave Bursky, Andy Santoni, Stanley Runyon and Jim McDermott.



By using a pseudo-NMOS structure instead of normal CMOS design, engineers at Bell Laboratories managed to reduce the complexity and size of the gate logic in their 8-bit CMOS microprocessor.

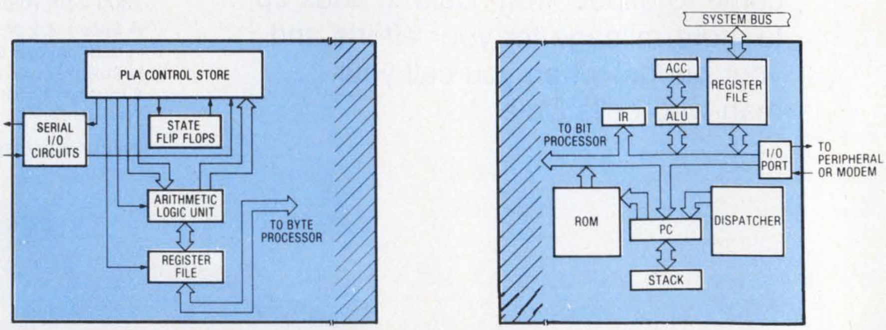
This universal language the users proposed should be supported by all low-cost-μP vendors so that any program developed can be easily converted into the specific op code for the μP selected. But the vendors disagreed and stressed the inefficiency of the final op code.

According to the manufacturers, the user doesn't want compatibility so badly that he's going to sacrifice performance in the μP chip to get it. It's too early to talk about a standardized instruction set, claimed both Smith, Manager of Systems and Logic Design at Rockwell and Claude Alleaume, Director of μP Engineering at Fairchild (Mountain View, CA). "Each one of the machines developed by now has a very unique history and has its own place," continued Alleaume.

In the meantime, manufacturers are still "hard at work" developing new low-cost processors so that users can extract the optimum dollar/performance tradeoffs.

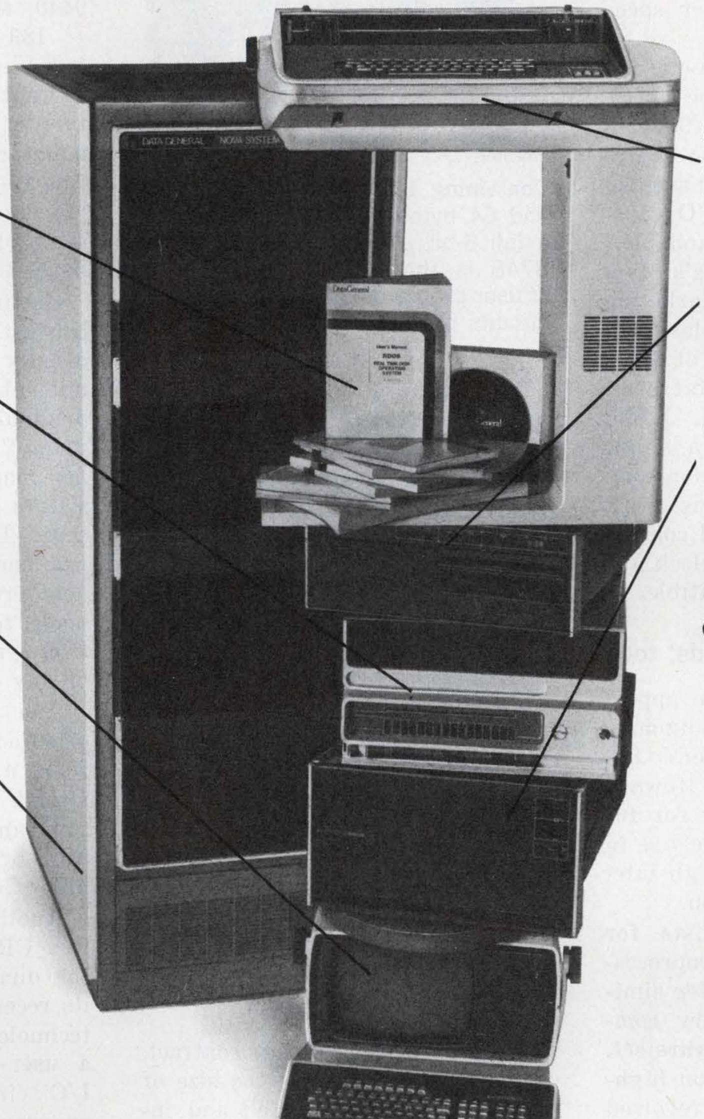
Intel (Santa Clara, CA) has opted for a new language set in its 8035/8048/8748 series of one-chip microcomputers, pointed out Henry Blume, Program Manager for the 8048. The 8748, when announced late last year, was a revolutionary design—not only did it contain a microprocessor with over 90 instructions but 1024 bytes of ultraviolet-erasable programmable read-only memory (UV EPROM)—all on a single chip.

Texas Instruments is going a different route, said Joel Cyprus, who is Manager of Systems and



What's better than one μP on a chip? Why two, of course. Combining both a bit and byte-oriented processor on a single chip, Intel has been able to make programmable controllers from the same basic chip.

Here's how Data General's NOVA 3/D system stacks up against the competition.



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CIRCLE NUMBER 18

Applications. "We currently offer the TMS-1000 series of PMOS microcomputers and will soon introduce an NMOS equivalent of the TMS-1000 called the TMS-2000, which will be instruction-compatible but offer better speed performance."

By year's end, an all-in-one 16-bit microcomputer will be introduced as well. Dubbed the 9940, it will use a subset of the TMS-9900 instruction set and have on-board ROM, RAM and I/O capability, but will not be expandable.

Owen Williams, Motorola's Manager of Systems and Marketing (Austin, TX), unveiled plans for two more μPs by the end of 1977. The 6801, an all-in-one 8-bit processor, will contain ROM, RAM, timer, clock and I/O on a single chip and be 6800-instruction-compatible. Also on the way is a μP called the 6802, which will contain 128 bytes of RAM and a clock and be 6800 instruction compatible.

There are hidden standards, too

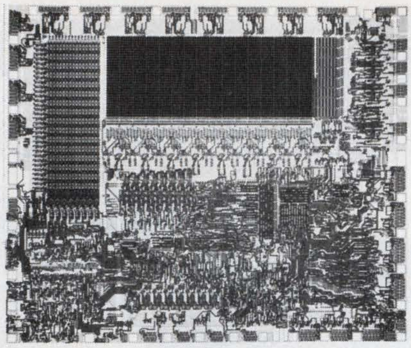
Even though there is no apparent effort to standardize language, most of the manufacturers' approaches are similar, said Howard Raphael, Product Manager for Intel. All of them are interested in the same features—I/O, high integration, low cost, and so on.

The same situation exists for the high-performance microprocessors—many of the μPs offer similar features although every company uses a different software set. But the panel discussions on high-performance processors revolved around several technology developments—such as device scaling, integrated-injection logic design, 5-V EPROM design, CMOS-on-sapphire and closed-loop CMOS—as well as a few new architectural and circuit designs.

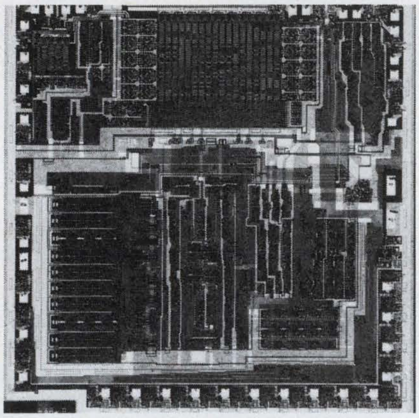
For instance, Hewlett-Packard of Palo Alto, CA, has crammed a 16-bit CMOS microprocessor into a chip only 34 mm^2. By taking full advantage of CMOS-on-sapphire to cut capacitance losses, the processor can operate at a 6.7-MHz clock rate and dissipate only 0.5 W (with a 12-V supply). However, this μP can't be purchased by itself—it's designed for controller applications within HP instruments and computer equipment.

RCA, Somerville, NJ, in research funded by a government contract, found a way to reduce the size of the CMOS transistor cell and increase speed by eliminating the guardband usually needed between n and p-channel devices. The closed CMOS logic is self-guardbanding and the transistor capacitance is low. As a result, dynamic circuits can offer five times the speed of standard CMOS. Used in the company's 1802 μP, the C^2L design packs transistors in a 238 × 172-mil chip.

By going to a pseudo-NMOS design, Bell Laboratories' designers in Murray Hill, NJ, can pack 7000 devices in a 220 × 230-mil CMOS chip. Noncomplementary structures for certain portions of the logic result in a processor with the functional density of NMOS but with the power dissipation and noise margins approaching CMOS.



Containing 1024 bytes of UV PROM and 64 bytes of RAM in addition to a full 8-bit μP on a single chip, the 8748 is the first of a new breed of user-programmable microcomputer circuits pioneered by Intel.



Duplicating the Nova instruction set, the 9440 microprocessor developed by Fairchild uses I^3L processing to attain a chip size of only 182 × 189 mils.

Exploiting its Isoplanar version of integrated injection logic (I^3L), Fairchild has developed a 40-pin 16-bit μP that executes the same instruction set as the Nova 1200 series of minicomputers. Called the 9440, the chip measures only 182 × 189 mils and can operate from a 5-V supply and a 1-V, 180-mA current source. One unusual feature of the 9440 is its 4-bit accumulator—instead of performing a full 16-bit operation like all other processors, it does four consecutive 4-bit operations. This method reduces the general logic functions.

Getting "the mostest into the leastest," Intel has pushed device density to 0.41 devices per square mil—about four times that of its original 8080 μP. On a chip measuring 218 × 244 mils, the company has managed to pack 22,000 transistors in the form of two processors. Designed to be microprogrammed at the mask level, the dual processor circuit can thus be made to perform floppy-disc control, synchronous data-link control, or any other function.

The basic chip has a byte-oriented processor with 46 instructions, a 1.25-μs execution time, and almost 7000 bits of control-store program space. Also on the chip is a bit-oriented processor, with 3300 bits of control-store memory.

Another circuit planned by Intel is a CRT controller, also based on the dual processor chip. Based on its recently developed 5-V EPROM technology, Intel will soon release a user-programmable, universal I/O circuit, the 8741/8041. The programmable circuit is expected to hold 1024 bytes of UV EPROM like the 8748, and take only 2.5 μs to execute instructions. And by the end of this year, further circuit development should increase transistor density to 30,000 devices on a 200 mil^2 chip.

Other μP peripheral circuits, such as a/d and d/a converters, are also getting some new twists. For instance, Precision Monolithics of Santa Clara, CA, described a novel converter trim technique, that quickly zaps diodes in current sources under computer control instead of doing time-consuming laser trimming of deposited resistors. (See "First Monolithic 12-bit DAC," ELECTRONIC DESIGN, No. 4, Feb. 15, 1977, p. 34). ■■

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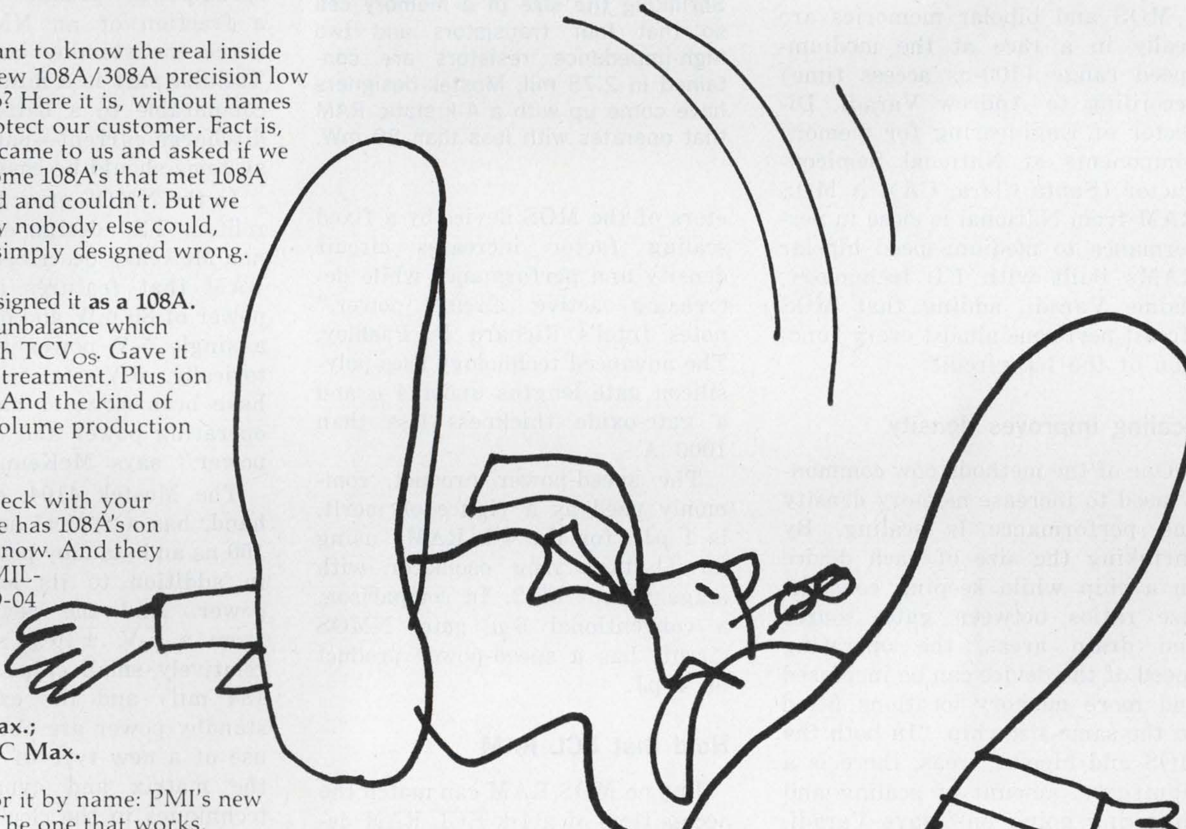

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CIRCLE NUMBER 19

MOS memory performance matches bipolar in medium-speed range

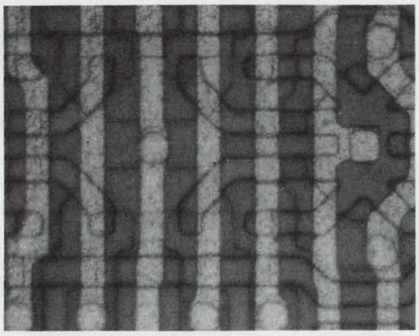
The relentless pursuit of bipolar speed by MOS memories continues. But even though today's MOS memories match last year's bipolar speeds, the bipolar circuits are getting even faster. In fact, one bipolar RAM described in a paper at the International Solid State Circuits Conference accesses in only 7.5 ns. However, MOS devices maintain their leads in high density and low power dissipation.

MOS and bipolar memories are really in a race at the medium-speed range (100-ns access time) according to Andrew Varadi, Director of Engineering for memory components at National Semiconductor (Santa Clara, CA). A MOS RAM from National is close in performance to medium-speed bipolar RAMs built with I^2L technology, claims Varadi, adding that MOS circuit performs almost every function of the I^2L circuit.

Scaling improves density

One of the methods now commonly used to increase memory density and performance is scaling. By shrinking the size of each device on a chip while keeping constant size ratios between gate, source and drain areas, the operating speed of the device can be increased and more memory locations fitted on the same-size chip. "In both the MOS and bipolar areas, there is a significant amount of scaling and shrinking going on," says Varadi, adding that "speed, die size, yield —everything is in favor of scaling."

Taking advantage of device scaling, Intel (Santa Clara, CA) has improved the access time of its 4-k static RAM. An n-channel MOS device, the memory has a typical access time of 45 ns, about 30% better than other available MOS RAMs. (At the 1976 conference, Intel described a 70-ns, 1-k MOS RAM.)



Shrinking the size of a memory cell so that four transistors and two high-impedance resistors are contained in 2.75 mil, Mostek designers have come up with a 4-k static RAM that operates with less than 80 mW.

"Reducing the physical parameters of the MOS device by a fixed scaling factor increases circuit density and performance while decreasing active circuit power," notes Intel's Richard D. Pashley. The advanced technology uses polysilicon gate lengths under 4 μ and a gate-oxide thickness less than 1000 A.

The speed-power product, commonly used as a figure of merit, is 1 pJ (for the 4-k RAM) using an 11-stage ring oscillator with stage fanout of 3. In comparison, a conventional 6-μ gate, NMOS circuit has a speed-power product of 4 pJ.

Hold that ECL RAM

But no MOS RAM can match the access time of a 1-k ECL RAM developed by Nippon Telephone and Telegraph and Fujitsu Ltd. in Japan. With a typical access time of 7.5 ns, it's twice as fast as even the fastest ECL RAM previously reported. The Japanese memory consists of four blocks, each 256 words by 1 bit. Each block can be selected independently by four block-select terminals, so the device can be configured as 256 words by 4 bits or 1024 words by 1 bit.

Typical operating power is 832 mW for the ECL RAM and 500 mW for the Intel 4-k MOS part. But while these numbers may sound comfortably small, they may be too high for large systems that pack many memory chips on a single board.

A 4-k static RAM built with CMOS technology is aimed at such high-density applications. Designed by Tokyo Shibaura Electric Co. Ltd. of Japan, the circuit has a speed-power product of 10 nJ—a fraction of an NMOS RAM's. Since the standby current of the Toshiba part is a minute 0.1 μA—comparable to a battery's natural discharge current—battery backup systems should be easy to set up.

In the NMOS area, Mostek (Carrollton, TX) design engineer Vernon McKenny described a 4-k static RAM that features an operating power of 80 mW and operates from a single 5-V power supply. "Historically, 5-V static MOS RAMs have been slow, or have had high operating power and high standby power," says McKenny.

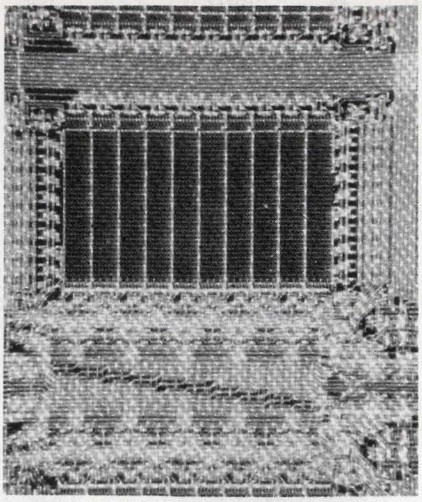
The Mostek 4104, on the other hand, has a typical access time of 150 ns and standby power of 8 mW, in addition to its low operating power. And the device operates from a 5-V ±10% supply. "The relatively small chip size (136 × 184 mil) and the extremely low standby power are obtained by the use of a new type of static cell in the matrix and dynamic circuit techniques in the clock generators, row and column decoders, and output buffers," notes McKenny.

Another Mostek RAM, designed for high-density applications, packs 16 kbits into 27,700 mil. This dynamic RAM is organized as 16 words by 1 bit—the same as all other 16-k RAMs. It can access a word in 150 ns and is housed in a standard 16-pin package. Seven address bits are multiplexed, and all clocks and other inputs are TTL-compatible.

The largest bipolar RAM de-

Comparison of memory technologies

	MOS RAM	CCD	Magnetic bubble
Storage (kilobits)	16	65	100
Access time	100 to 200 μs	200 to 400 μs	1 to 10 ms
Transfer rates (Mb/s)	2 to 3	5	0.05 to 0.2
Chip size (mm^2)	13 to 17	20 to 26	63
Cost per bit (relative)	1	0.25 to 0.4	0.2 to 0.3



A 92,160-bit CCD memory tolerates faults in single-memory cells because any of the 36 blocks like this one can be disconnected from the circuit, leaving only good cells in operation.

scribed at the conference is a 4-k I^2L design from Fairchild Camera and Instrument Corp., Mountain View, CA. Fully static, the memory is organized as 4-k × 1 and uses a walled-emitter Isoplanar process to obtain small memory-cell and chip size, as well as high speed. ECL techniques are used for internal circuitry to produce a typical access time of 35 ns and a current consumption of 185 mA at 5 V.

"Another figure of merit—access time × chip size × power dissipation—is considerably better for bipolar devices than for MOS devices. But the two technologies are converging," according to Thomas A. Longo, vice-president and chief technical officer at Fairchild. "The cross-over point, if the trend continues, is in the 1980s," he says.

Predicting future is risky

But care must be taken when projecting the future of semiconductor memories, comments Ronald J. Whittier, director of engineering at Intel's Components Division. If memory cells follow the historic path, the size of a storage location will shrink to zero by 1979, he quips. So will manufacturing cost and selling price. "Another good point," adds Whittier, "is that by 1979 the volume will be infinite."

Users need projections, however, to decide on purchases, says Michael Gutman, product-engineering manager for systems and devices at Digital Equipment Corp. (Maynard, MA). Concerning 16-k RAMs, for example, Gutman foresees a trickle of parts in the first half of this year, a small to modest flow of parts later in the year, and, he hopes, "some serious availability of parts in 1978." Says Gutman: Buy too early and the price will be high; buy too late and the competition will have an edge.

L. W. Wu, manager of design engineering at Amdahl (Santa Clara, CA), looks at costs through the eyes of a user. "As we see it, there's a doubling of memory density every two years, which allows the system designers to develop a product at lower cost." But even as Mostek's senior staff engineer Paul Schroeder notes that the trend has been toward quadrupling the size of memory every three years, he cautions: "We probably will not see that kind of growth continuing ad infinitum.

"We're now at a point where there is very little density to gain just from reducing cell size," Schroeder adds. "But there are still some things that could conceivably be done to get us to the next level of integration. I'm not necessarily suggesting that any of these are practical or are going to work out, though."

Room for improvements

Schroeder points to three possible avenues for improvement.

- One is to use fault-tolerant techniques in designing memory devices so that wafers that have dies where some bits aren't functioning can be used in systems nevertheless.
- Another possibility is to go to different computer architectures, which would allow high-density CCDs to be used for low-cost virtual storage.
- A third alternative is to restore historical growth patterns through scaling, among other techniques. "If that is the route by which semiconductor memories develop further, it may turn out that there is some justification for a 32-k RAM," says Schroeder. "There might be a sufficiently wide time window in which it's the economical configuration."

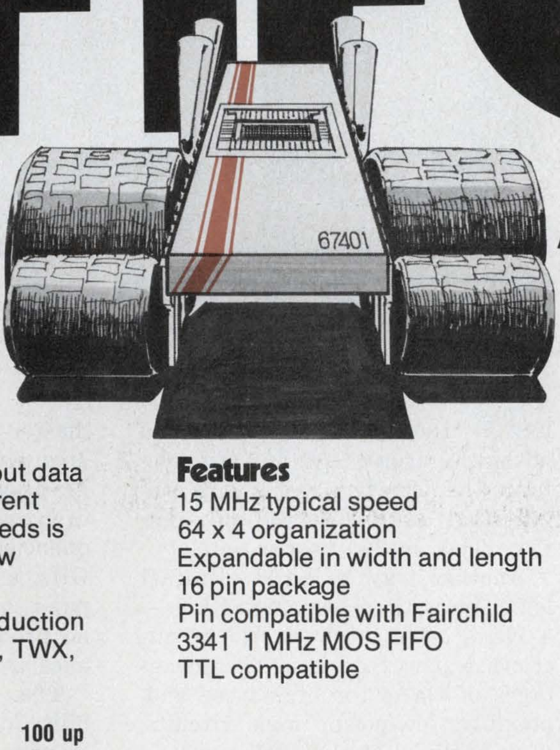
A 92,160-bit CCD serial memory developed by Honeywell Information Systems (Phoenix, AZ) uses the first approach suggested by Schroeder. The memory is divided into 36 blocks, each containing 2560 bits of storage. Each block can be connected into the system via a laser link-burning test system that zaps shorting links at the wafer-probe level. Thus, only a small part of the device is lost due to a single bit failure—not the entire memory.

A 256-k CCD memory will be available by 1980, predicts Fairchild's Longo. And Mark Guldry, manager of MOS-CCD memory design at Fairchild, notes that since the CCD structure is somewhat simpler than that of MOS RAMs, "the CCD memory can be somewhat denser," and its price per bit potentially lower.

Just a few years ago, CCDs were referred to as "gap-filler technology," recalls Al F. Tasch, branch head for advanced memory technology at Texas Instruments Inc. (Dallas, TX). But as CCD performance and chip size come closer to that of MOS RAMs (see table), Tasch predicts that CCDs find greater application in computer systems for virtual memory as well as for operating-system storage.

An while CCDs will never replace RAMs, in the view of Thomas L. Palfi, vice-president for research at Intersil Inc. (Cupertino, CA), they will find use in such applications as buffer storage in time-shared systems. ■■

First Fast FIFO



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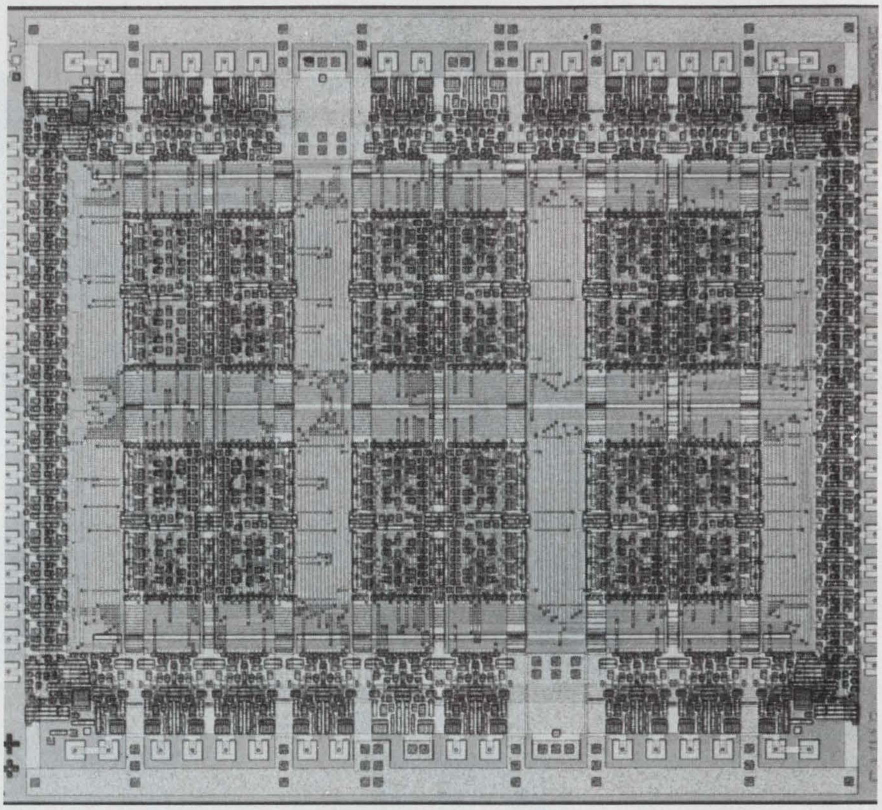
CIRCLE NUMBER 21

Ultra-high-speed logic—more than just a promise in LSI

The 10-year-old promise of subnanosecond ICs may finally be kept—and with lower power consumption and larger scales of integration than ever before. Among the more impressive advances reported at the International Solid State Circuits Conference were bipolar ICs with propagation delays under 100 ps, 4-GHz GaAs MESFET ICs and a "masterslice" LSI circuit targeted at subnanosecond, random-logic applications.

Although high-speed ICs have been around for some time, high cost and a voracious power appetite have kept such chips prohibitive for high-volume applications. A new bipolar process—called Elevated Electrode IC (EEIC)—may change all that.



In the Siemens "masterslice" LSI chip, 24 logic cells are arranged in blocks of four. Instead of basic gates, each cell contains 38 transistors and 16 resistors, which can be wired in a desired arrangement.

Elevated structure raises speed

Described by Tetsushi Sakai of Musashino Electrical Communication Laboratory, Tokyo, Japan, the EEIC process produces elevated electrodes (emitter and collector) from arsenic-doped polycrystalline silicon (P-Si). All interconnections and electrodes are formed without fine lithography or etching.

The elevated structure is processed to form an overhanging edge, which separates the P-Si from the lower level. When the metallization is applied, the various evaporated metals are isolated from each other by the shadowed area under the overhanging edge.

The high performance made possible with EEIC was demonstrated by an experimental, 15-stage ring oscillator and an 8-bit arithmetic and logic unit (ALU). In a low-power configuration, the oscillator shows a blazing propagation delay of only 102 ps and a minuscule power-delay product of 0.075 pJ. An even higher-speed version clocks in at 85 ps and 0.187 pJ, respectively.

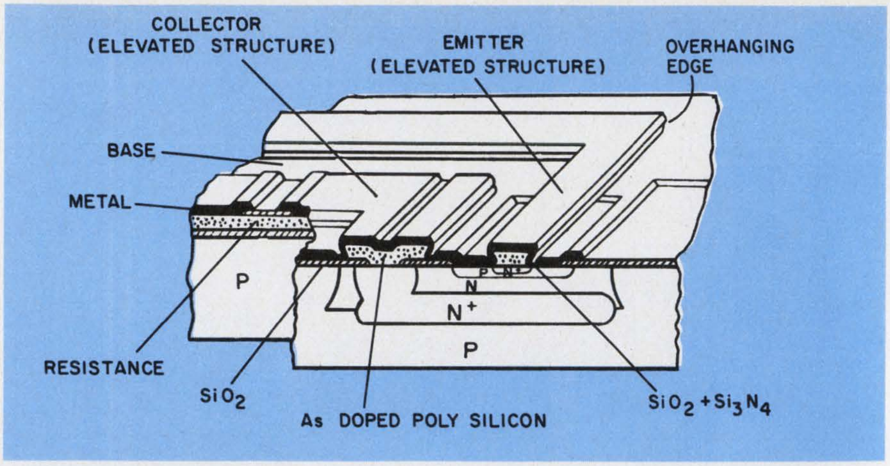
The ALU illustrated the high packing density also possible with EEIC: 180 gates are integrated within an area of 1.6×1.0 mm^2—twice the density possible with conventional ICs. Observed propagation delay is 260 ps per gate.

Another way to build ultrafast logic is with GaAs MESFETs—a rising star in the world of microwave power devices. The advantages of GaAs for high-speed and, possibly, low-power logic circuits, were outlined at the conference.

From microwaves to logic

A 4-GHz frequency-divider IC may offer enormous potential for designers of frequency counters and other instruments. Described by Rory Van Tuyl of Hewlett-Packard Laboratories in Palo Alto, CA, the divider is made up of master-slave flip-flops and operates with sinusoidal inputs down to dc. However, the input sensitivity drops sharply with increasing frequencies above 3 GHz. And at 4 GHz, a rather large 3 V pk-pk input is needed in a 50-Ω system. But no problem exists for high-impedance uses.

The present MSI density capability of GaAs MESFET technology, explained Van Tuyl, is obtained at 25 to 30% yields—at least for a gated prescaler built with three of the frequency dividers. The future, according to Van Tuyl, should bring 6-to-8-GHz counting circuits as well as more complex chips that consume less power. The current divider chip measures 440×400 μm and dissipates 160 mW.



This integrated transistor structure uses the Elevated Electrode IC process developed by Musashino Electrical Communication Laboratory. EEIC achieves ultra-high speeds in part by decreasing junction capacitance.

A twist on the "usual" GaAs MESFET logic was reported by Hajime Ishikawa of Fujitsu Laboratories, Kawasaki, Japan. A 13-stage ring oscillator was built with normally-off FETs, instead of the usual normally-on approach. As a result, power-speed products as low as 0.026 pJ and propagation delays as low as 280 ps were obtained—but not simultaneously.

Keep it off to keep it fast

Compared with normally-on logic, the "off" technique dissipates one-hundredth the power—and even more drastic reductions are expected, clamed Ishikawa, as design and fabrication are refined. In fact, packing density as high as 800 gates/mm² may be achievable.

The key to fabricating normally-off MESFETs is to control the threshold voltage, V_T. Reported V_T is 0.1 V, with a logic swing of 0.6 V, noise margins of 0.27 V and 0.06 V, an active-region dc gain of 2.5 and a V_{DD} of 1.2 V. Some attendees doubted the validity of the noise-margin specifications, and the ensuing discussion failed to resolve the question.

When asked about the possibility of LSI MESFETs, Ishikawa responded that the cost of GaAs would be the limiting parameter, and LSI products wouldn't appear for another five years. But the importance of building circuits in LSI to reach high-volume markets was underscored by Walter Braeckelmann of Siemens AG in Munich, West Germany, who told of a bipolar "masterslice" LSI. Composed of E²CL circuitry arranged in a complex, cell-based logic array, the LSI chip provides up to 700 gate functions at average speed-power products of 2.5 pJ per gate.

Instead of basic logic gates, the masterslice builds up logic with extensive series gating and complex functions. Each cell—the smallest repetitive part of the LSI chip—consists of 38 transistors and 16 resistors, which can be connected by various intracell wirings to arrive at different complex cell types.

Two basic layouts, with either 24 or 36 cells, have been built, with respective chip sizes of 36 and 28 mm². Up to 700 gate functions are possible with the 36-cell array, and 500 with the 24 cell. Typical performance levels for delay and power consumption are 0.5 ns, 9 mW for an OR/NOR gate (with one gate function), and 0.8 ns, 11 mW for a 4-bit multiplexer (with seven gate functions). Typical logic swing is 400 mV. Previous masterslices consisted of basic gates, and had a speed-power product of 17 pJ and 100 or 200 gates per chip.

In the Siemens design, intracell wiring is laid out just once. Internal gates are connected with LSI pins through level shifters to obtain high noise immunity, compatibility with standard ECL and outputs that can drive 50-Ω lines. The shifters can also perform logic functions or even act as latches in some cases.

Approximately 25% of the area of the 24-cell slice is occupied by the logic cells, another 25% by the intercell wiring, and 16% by the pads. The remaining real estate (24%) holds the supply lines and level shifters. Of the chip's 64 pads, 58 are used for logic, 6 for power. A special 64-pin ceramic package holds the LSI chip, and the package's thermal resistance is 20° K/W at 3 m/s of forced air flow.

Better I²L coming soon

Speed and chip size, as well as getting more on the chip, dominated many of the sessions. For example, in the session on LSI technology, Tich T. Dao of Signetics, Sunnyvale, CA, showed how threshold I²L can save area over conventional I²L designs.

Present technology makes multilevel logic possible, and Dao described a deskewing FIFO that sets flags to indicate the one-quarter, one-half and three-quarter-full conditions.

The conditions are derived by enumeration of the ONEs in a 16-bit control register. For example, the one-quarter-full condition is true if four or more consecutive bits in the register are ONE. To indicate such a condition with conventional two-level circuitry requires 13 AND gates—much more than threshold I²L.

Although I²L is used mostly for linear ICs, a new fabrication approach outlined by Stanford University's Roderick Davies pushes I²L switching speed to better than 10 ns at 100 μW per gate—two to three times faster than existing I²L processes.

Digitial I²L foretold

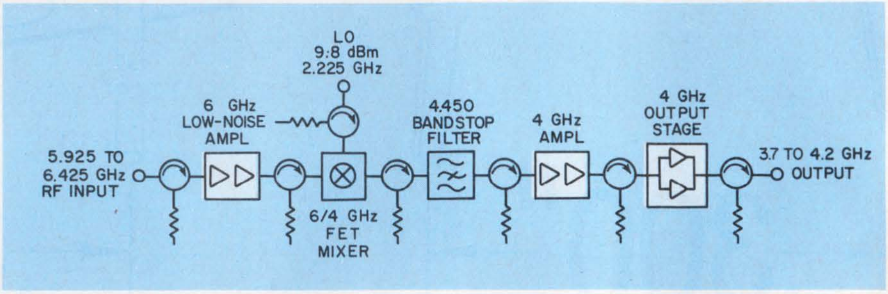
The new technique—termed Poly I²L—gains its advantages from an improved doping profile of the npn transistors and from formed poly-epitaxy diodes acting as clamps or antisaturation devices.

The speed premium of Poly I²L is gained without increasing standard IC-process complexity too much, and without degrading linear-circuit capability or losing compatibility with low-speed, micropower I²L. What's more, such benefits open new doors to the construction of complex analog and digital functions on a single monolithic chip —a topic of considerable interest today. ■■

Fabrication and circuit progress leads to better microwave devices

Both the power output and frequency range of microwave devices have improved significantly this past year. One reason is better device fabrication technology. Another is the development of improved interfacing and matching circuitry. Not surprisingly, these key advances highlighted the microwave sessions at the International Solid State Circuits Conference. Chief among the developments discussed were:

- A 12-W, 4-GHz transistor amplifier with a new type of self-aligned bipolar structure.
- A bipolar transistor that uses state-of-the-art interfacing techniques to give a 7-dB CW power gain at 5 GHz and 5-W output.
- Deep-diffused, low-loss p-i-n diodes with breakdown voltages greater than 1500 V which can handle 5-kW peak power in a microwave phase shifter.
- A fixed-tuned Trapatt amplifier that is insensitive to diode parameter variations such as junction capacitance and breakdown voltage.
- A gallium-arsenide FET satellite communications receiver that provides a 60-dB gain with a maximum noise figure of 3.7 dB.



High gain, excellent linearity and low noise figures are provided by gallium-arsenide FETs in this satellite-communications receiver.

Bipolar amp gives 12 W at 4 GHz

A three-stage amplifier that relies on transistors made with a new kind of self-aligned bipolar structure delivers a high rf-power output using a 20-V-dc supply. The 12 W of rf is due to the improved high-frequency performance of the bipolar transistors and a well-designed power-combining circuitry, according to the amplifier's developers, Nippon Electric of Japan.

Seven transistors, each capable of delivering 3 W at 4.2 GHz are used in the three-stage amplifier. Transistor gain is 5 dB, with a 17% power-added efficiency in a common-base configuration.

The transistors are fabricated with polysilicon-emitter fingers that have an overhang cross section. The emitter structure is formed on the base region by employing a differential etching rate between the undoped polysilicon on top and the arsenic-doped polysilicon of the lower layers.

Output capacitance is decreased as a result of very narrow spacing between the emitter and base metallic contacts. These contacts are formed with a relatively simple alignment procedure, which consists of applying metallization after the polysilicon eaves are formed. Also, the parasitic MOS capacitance associated with the bonding pads is reduced by introducing a porous silicon dioxide layer about 2.5 μm thick beneath the bonding-pad metallization.

Each transistor assembly in the amplifier contains microstrip input and output-matching networks. The latter are connected to the power-combiner/divider of a double-section 3-dB quarter-wave hybrid.

One of the major advantages of the transistor's construction is the low junction operating temperature—below 120 C at a 50-C ambient.

Parallel cells give 5-W output

State-of-the-art input and output matching techniques are employed in a 5-GHz bipolar transistor developed by TRW (Lawndale, CA). In the transistor the outputs of six transistor cells are combined to deliver a total of 5 W. Applications for such devices abound in transmitter amplifiers for troposcatter communications, satellite-communications systems and phased-array radars.

The transistor assembly's gain and stability are improved by two techniques. First, a reactive component in the output current at the common-mode base device is minimized by returning the collector-shunt inductor directly to the base bonding pad. Second, gain and stability are further increased by double-bonding to return the base more directly to ground.

The blocking capacitor for the collector shunt is placed as close as possible to the transistor chips. Not only does this reduce losses in the collector circuit, but it also lowers the VSWR that the remainder of the circuit must tune out.

To further reduce losses at the internal-to-external circuit interface, the collector-matching network resides entirely on the substrate. The input circuit is a minimum-loss, low-pass network that permits maximum transfer of drive power while maintaining an acceptable input match. Over-all thermal resistance is reduced by spacing the six transistor cells widely apart.

Collector efficiency is 24% for

Microwave device performance and applications

	Technoloy	Devices	Present Performance	Performance Goals	Advantages	Limitations
Digital	Bipolar	Logic elements	1 Gb/s SSI 0.5 Gb/s MSI	1 Gb/s MSI/LSI	① Mature technology ② Practical for LSI ③ Well controlled threshold ④ Wide speed/power range	① Low noise immunity ② Limited frequency range
	GaAs MESFET	Frequency dividers	4 Gb/s 3.5 pJ MSI	> 5 Gb/s 1 pJ MSI	⑤ Simple device structure ⑥ Semi-insulating substrate ⑦ Practical for MSI ⑧ High speed	③ Needs large input signal ④ Excessive power consumption
	GaAs TED	Multiplexers	2 Gb/s 5 pJ SSI	5 Gb/s 1 pJ MSI	⑤ ⑥ & ⑧ Above ⑨ Intrinsic pulse regeneration ⑩ Simple circuits	③ and ④ above ⑤ Interface problems
Analog	Bipolar	4-quadrant multipliers	0.75 GHz BW	1 GHz BW	① and ② above	② above ⑥ Difficult impedance matching
	GaAs MESFET	Monolithic amplifiers	6.5-12.5 GHz 20 ± 0.5 dB	8-12 GHz 20 ± 0.5 dB	⑤ to ⑦ above ⑪ Broadband ⑫ Cost, size, repeatability better than hybrids	⑦ Poor component Q-values
	GaAs TED	BPSK modulators A/D converters	—	5 GHz CW 1 Gb/s Data 5-G Samples	⑤ to ⑩ above	⑤ above ⑧ Poor performance repeatability

a 24-V-dc supply. Typical saturated output is 6-W CW, and peak is 12 W with a 10-μs pulse width.

Deep-diffusion keeps losses low

The lowest loss yet of any high-power diode phase shifter has been obtained in a 5-kW, peak-power, microwave IC phase shifter that includes a recently developed RCA (Princeton, NJ) p-i-n diode. This deep-diffused type has an average loss of 1 dB under 50-mA forward-bias and −40-V reverse-bias conditions.

Breakdown voltage is greater than 1500 V, report RCA researchers. The diode has a forward-resistance loss of less than 0.2 Ω at 50 mA and a Q greater than 1000 at 900 MHz and −40-V reverse bias.

Experimental results show that the p-i-n diode's power handling is improved by the deep diffusion process, RCA reports. Forward-bias resistance is minimized by maximizing the lifetime of the minority carrier in the diode fabrication at 12 μs for a forward current of 20 mA.

A 3.13-GHz amplifier that can withstand variations in Trapatt-diode junction capacitance and breakdown voltage has been developed at the Hughes Research Center (Torrance, CA). The insensitivity of the amplifier voltage to diode parameter variations makes it particularly useful in applications requiring many of these devices, such as phased-array radar systems.

The twin-diode stagger-tuned amplifier produces more than 260-W peak power at 25% efficiency, report Hughes researchers. Several lots of mesa Trapatt diodes, with junction capacitances ranging from 5 to 16 pF and breakdown voltages from 65 to 95 V, have been operated in this amplifier without having to be retuned. Most of the diodes tested produce power-added efficiencies of at least 20% and power gains from 4 to 9 dB.

The amplifier's design is based on the bandpass impedance-transforming characteristics of a pair of coupled lines. To achieve high efficiency, fundamental mode extraction is also employed. The amplifier itself consists of a multiple-section bias filter, a pair of open-ended coupled lines about one-quarter wavelength long, and an SMA output connector.

GaAs FETs make satellite receiver

By using all gallium-arsenide FET active elements, the communications-satellite transponder receiver from RCA Ltd. in Montreal, Canada satisfies the stringent requirements of gain linearity and noise figure imposed on these high-performance systems. This FET receiver has a 60-dB gain with a 0.5-dB flatness over a 5.295-to-6.425-GHz input bandwidth and a 3.7-to-4.2-GHz output bandwidth. At the worst point in the band, the gain slope is 0.01 dB/MHz, and the noise figure is 3.7 dB. But the noise decreases to as low as 3.3 dB at the band center.

In the receiver, an input isolator is followed by a 6 GHz, two-stage low-noise GaAs FET amplifier whose output is fed to a 6/4-GHz mixer. The mixer has an over-all gain of 1 dB with a 9.8-dBm, 2.225-GHz local oscillator signal applied to the mixer-FET drain. ■■

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I^2L and CMOS battle for lead as IC-technology race heats up

Monolithic IC technologies are expanding simultaneously on a broad number of semiconductor fronts. Rival chip fabricators are outdoing each other by creating smaller chips with ever increasing numbers of integrated elements. These in turn provide such performance features as lower power, higher operating speeds, improved temperature characteristics and lower noise. Where the fabricators are unable to accomplish these goals with processing—diffusion, ion implantation, dielectric isolation—they rely on the ingenuity of their chip-circuit designers to overcome performance obstacles.

I^2L is coming up fast

Probably the fastest moving technology today is I^2L. The processing difficulties, which made this bipolar technology's potential uncertain just two years ago, have been licked, and I^2L is becoming useful for applications ranging broadly from wristwatches to microprocessors.

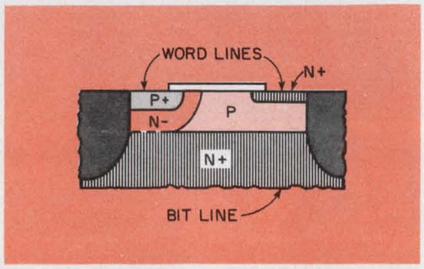
Not only does I^2L give better packing density than MOS, but it provides better performance as well. And it's giving CMOS—its leading competitor—substantial competition in low-power devices.

I^2L watch-circuit density has improved in the past few months. A LED watch chip can now be fabricated on 20,000 mil^2 or less—a trend that will continue, according to Dean Toomes, vice president of engineering for Texas Instruments' Semiconductor Group.

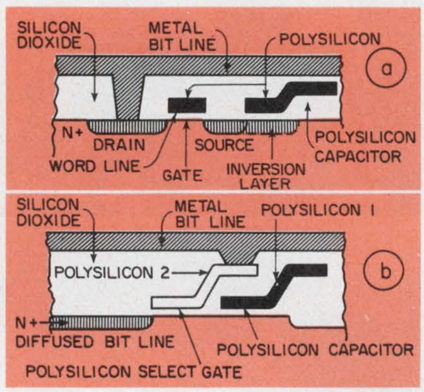
The I^2L watch chips are optimized to consume minimal power. In LED watches the I^2L power drain is the same as that of CMOS, about 5 μA at 3 V.

In some respects, I^2L is even better than CMOS for LED watches,

Jim McDermott
Eastern Editor



1. **The simple cell structure of the I^3L RAM** of Fairchild gives the 4096-bit device two to three times the speed of its MOS RAM competitors.



2. **Construction of a single-level, polysilicon 4-k RAM cell** (a) is compared with that of a double-level polysilicon 16-k RAM (b). The two-level process reduces 16-k cell size to one-half that of the 4 k.

which need a 5-mA display-drive capability. Because I^2L is a bipolar technology, bipolar transistor drivers can be put onto the I^2L chip efficiently to get this capability.

But for an equivalent CMOS chip, the drivers—consequently the chip—are necessarily larger because of higher losses. (However, where the application doesn't require a high current capability, CMOS is a good solution.)

Another advantage of I^2L over CMOS is its ability to operate with a single 1.5-V battery, down to 1-V supply voltage. CMOS is more difficult to fabricate for these low voltages because it requires threshold voltages of less than 1 V.

High-performance I^2L technology is tailored to applications that benefit from the inherent low power but require logic switching speeds close to or exceeding standard TTL. An example is TI's 16-bit I^2L 9900 microprocessor.

For this technology, propagation delay is about 20 ns at 100 μW per gate. A 5000-equivalent-gate device has only 0.5-W dissipation. Indications are that the present 20-ns technology can be reduced to 5-to-10-ns for complex logic functions.

Advances in I^2L circuit density are being made at Motorola and Fairchild Semiconductor. Several Motorola custom I^2L chips have gates in the 500-to-1000-gate complexity.

"Three years ago," says Joe Brendel, manager of linear design operations, "we had only 70-to-100-gate complexity."

Another version is I^3L

Fairchild Semiconductor is using its version of I^2L—isoplanar integrated injection logic (I^3L)—for logic, memories and a new 16-bit "micromini" processor.

"We get greater densities per chip with I^3L than with MOS technology," says Thomas A. Longo, vice president and chief technical officer. "An I^3L chip is about 60% the size of an isoplanar n-channel chip of equivalent density. For example, our 9408 microprogrammed sequencer chip, which is used with the four-bit slice microprocessors, is about 12,000 mil^2 and has a 1000-gate complexity.

"Another example, our recently announced 4-k dynamic memory, has 4096 bits on a 12,000-mil^2 chip. And we can shrink it even further. Also, it has a single 5-V supply, two supplies less than the number needed for MOS RAMs."

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CMOS is now making a strong recovery. JEDEC standards were established in 1976 for the first and new B-series of CMOS parts.

CMOS technology expanding

Significant CMOS advances are being made by RCA in watch chips, automotive control functions, and CB frequency synthesizers. To better compete against established watch chip suppliers like TI, National, AMI and Fairchild, RCA developed the low-voltage aluminum-gate process (LoVAG), a proprietary CMOS technology that is considerably simpler than the self-aligned silicon gate approach. According to RCA, the company is following a defect-density-tolerable approach both in the masks and in the process line—and moving ahead quickly.

"In the first LoVAG generation, the chips had about 5800 transistor equivalents on a 28,900-mil^2 chip," says Jerry Beckman, director of COSMOS at RCA. "The second generation has a device count of over 10,000 per chip. The latest design philosophy uses dynamic logic on one-half of the chip and static on the other to attain more circuit density."

Acquiring bipolar versatility

Originally developed for low-power digital circuitry, CMOS is now being tailored for a variety of strictly linear circuits as well as for chips containing both linear and digital devices. "You can make any analog function using today's CMOS technology," says Dave Bingham, engineering manager of Intersil's industrial timing group. "This includes op amps, other amplifiers, current or voltage sources, and signal conditioners.

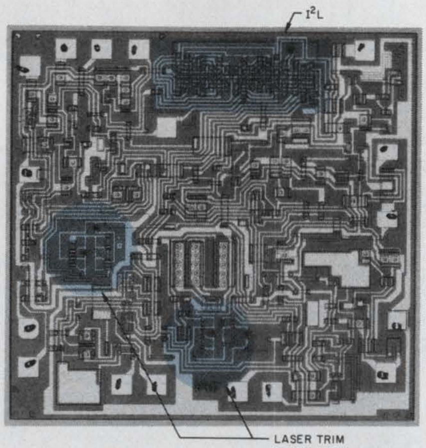
"Intersil and probably the rest of the industry are capitalizing on CMOS silicon and metal gate technologies for combining both analog and digital signal processing on a single chip.

"Using circuit-design tricks," Bingham continues, "we can achieve, in CMOS, almost anything you can do in bipolar. But we can't get quite as high a speed, nor can we get the close match of bipolars.

"For example, we can operate CMOS counters at 20 MHz, where a good low-power Schottky process will go up to 70 or 80 MHz. We can match CMOS transistors better than 10 mV whereas bipolars can be matched within 2 mV."

A 3-1/2-digit multimeter CMOS chip has just been completed by Intersil with "everything on it," according to Bingham. It provides noise performance down in the 10-μV range, draws lower current and has smaller chip size than has been achieved to date in any other technology.

"We can even go into high power applications with CMOS," Bingham adds. "For example, we have products under development that can drive large LED displays requiring several hundred mA per digit, directly from the chip."



Linear and digital technologies are combined in this high-density variable-slope delta modulator by Motorola. A linear-compatible I^{2}L process used in the digital portions of the chip reduces chip size by 5 to 1.

Semiconductor manufacturers are also improving on the ability to combine both bipolar and MOSFET devices on the same chip. For example, while dual op amps using the BiFET technology have been around for some time, TI has just announced the first quad version.

The technology advance was achieved, according to TI, with a thorough understanding of processing—particularly ion implantation—and clever chip circuitry.

Motorola is achieving linear-digital circuit compatibility through a variety of fabrication techniques such as low-power Schottky T^{2}L technology, laser trimming, ion implanting, dielectric isolation and linear-compatible I^{2}L circuitry.

While I^{2}L and CMOS developments are taking the spotlight on the IC-technology stage, there are a number of other competing technologies making important contributions in different device areas.

Double-layer poly process

One of the older technologies that has aided the development of the new 16-k RAMs is the double-layer polycrystalline silicon (polysilicon) process.

"With this technology," says Derrell Coker, Mostek's applications manager for memory products, "we're able to build a 16-k dynamic RAM, like the MK 4116, with a chip size of less than 27,000 mil^2—essentially the same size as its 4-k predecessor, which was fabricated with the single-level polysilicon process.

The double-level polysilicon process isn't new; it's been around as standard technology for CCDs. But it offers advantages for the new 16-k RAM products. Coker explains:

"The latest generation of 4-k RAMs are designed with n-channel silicon-gate processes. They use a single-transistor storage cell made up of a pass transistor and an associated storage capacitor.

In the 4-k RAMs these elements occupy individual areas. But with the double-layer polysilicon process, one is mounted over the other, so that areawise it looks like one component instead of two."

Access times of the MK 4116 range from 350 ns to less than 150, depending upon its mode of operation in a microprocessor system.

Advanced fabrication and IC circuit-design techniques have smashed speed barriers for static NMOS RAMs. A new 4-k $\times$ 1 RAM in pilot production at Intel, the 2147, has a typical access time of 45 ns. Announced by Intel at the International Solid State Circuits Conference, the RAM achieves its speed not through new technology but by scaling down the physical dimensions of on-chip devices and providing on-chip substrate biasing. The RAM operates from a single 5-V supply.

The 2147 approach beats both I^{2}L and CMOS on performance, Intel claims. But static 1-k RAMs with speeds equal to or better than

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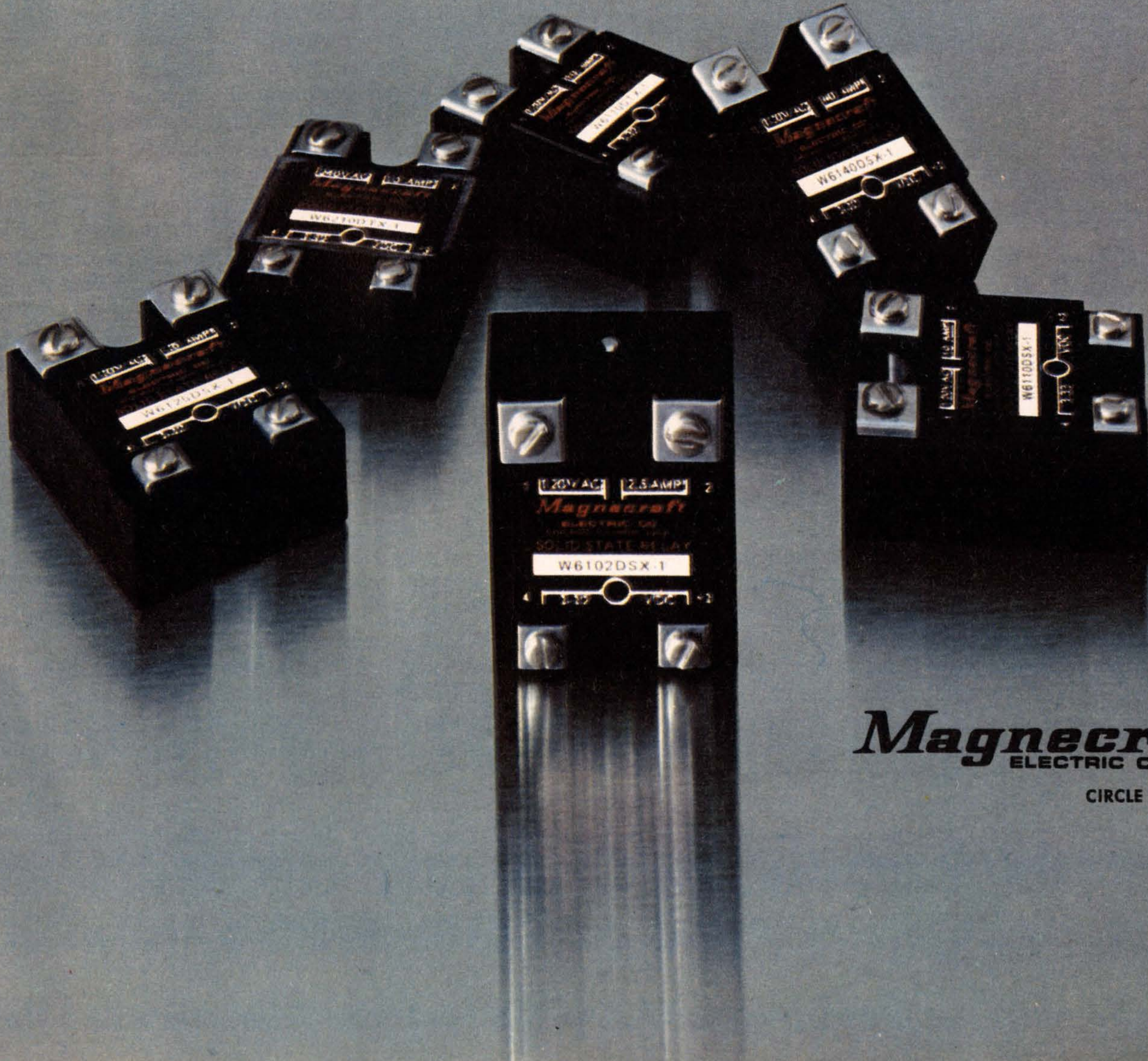

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the 2147 have been reported for VMOS devices.

VMOS makes fast ROMs

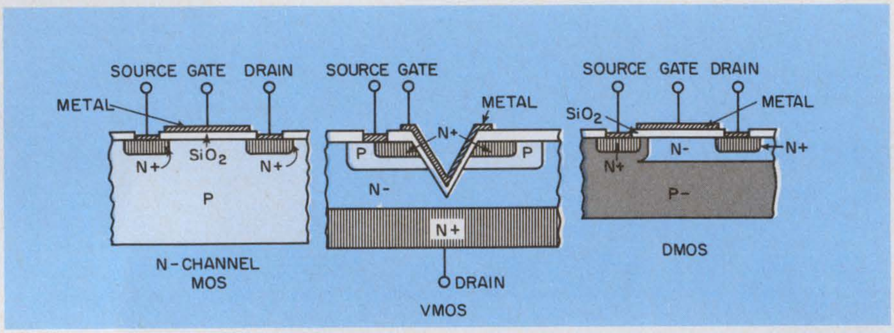
Vertical MOS (VMOS) is one of the newer technologies with great promise for high-speed, high-density logic and memories as well as for linear devices like high-power, high-frequency amplifiers. Unlike conventional planar MOS, with the source, gate and drain on the surface of the chip, the VMOS structure looks like an inverted pyramid etched into the chip.

In the VMOS structure the source is on top and the drain—like the collector of a bipolar transistor—is on the bottom. The gate is formed on the sides of the V-shaped notch between the source and drain. Current flows from the source to the drain along the sides of the notch.

Conference by American Microsystems designers, is suitable for a ROM, an EPROM or a dynamic RAM. All cells have the same topology and surface area (0.36 mil²). Each cell consists of a 6 μ × 6-μ VMOS transistor at the intersection of orthogonal gate and drain conductor stripes. Die size for a prototype 1-k static VMOS RAM is 81 × 125 mil. Access time, at 75 C and 4.75 V, is 45 ns.

The advantages of VMOS technology have also been applied by Siliconix designers to rf power FETs operating in the 200-to-300-MHz region. "We're in production with 2-A devices at 100 V that can dissipate up to 35 W," says Gary Hess. "Applications range from high-speed switches to communications amplifiers."

Fabricated on a chip together with zener protection, these amplifiers have under 10-ns on-off times,



3. **N-channel MOS, VMOS and DMOS structures** are compared above, left to right. In the VMOS device the current travels vertically, giving high source to drain breakdown and low gate-to-drain parasitic capacitance.

A 16-k, 5-V static ROM made with this process has been demonstrated by American Microsystems. The 16-k device occupies a chip somewhat less than 17,000 mil²—a marked contrast to standard n-channel ROMs, which occupy an additional 5000 mil².

Because of the device structure, capacitance between the drain and the source is substantially reduced over conventional MOS cells. The result is an access time of 50 ns or less.

In general, however, this type ROM has a limitation. Because all its memory cells share a common source element, the substrate of the chip, independent control of each memory cell is complicated.

A new VMOS-cell structure, reported at the Solid State Circuits

according to Hess, and can be driven directly from a CMOS logic element because of the high VMOS input impedance. "These devices are free from problems of bipolar transistors, including secondary breakdown or thermal runaway," Hess adds.

Developments are currently under way to extend voltage ratings up through 200 and the frequency capability into the GHz range. Ultimately, Hess notes, Siliconix expects to make a multiple device on a chip.

Small, fast chip elements can also be produced with the double-diffused MOS (DMOS) process. DMOS structures provide an effective 1-μm channel length by double-diffused doping in the gate region.

DMOS logic and memory ICs from Nippon Electric operate with speeds of 1 to 5 ns. Discrete transistors fabricated by Signetics with DMOS have worked into the gigahertz region. Signetics has also recently announced DMOS transverse filters and analog delay lines as well as analog switches.

Like VMOS elements, DMOS devices are more complex to fabricate and consequently more costly, than devices made with conventional silicon gate processes. Just how well DMOS will fare in the cost-competitive environment of the semiconductor world remains to be seen.

Programmable ROMs improving

Several different technological advances are being made in a specialized, but diverse area of memories: programmable ROMs. For example, the first CMOS PROM with fused silicon links has just been announced by Harris Semiconductor. It was developed to provide programmable CMOS memories for microprocessor use.

UV-erasable PROM (EPROM) technology has taken two steps forward at Intel with the announcement of two new devices. One, the 2716, is a 16-kbit EPROM that uses a single 5-V supply. The other is the 8748, a single-chip 8-bit, 5-V microcomputer with an 8-k EPROM built into the chip.

The 8748 is the reprogrammable version of the recently introduced 8048 single-chip device. The 2716 is a new double-layer, polysilicon n-channel MOS device and a third-generation EPROM.

Electrically alterable ROM (EAROM) technology hasn't been standing still, either. New devices have been developed jointly by both NCR Microelectronics and General Instrument. One part is an 8-k bit device, while the second is a 4-k bit unit that is, for the first time, word-alterable.

The latest GI EAROMs have been speeded up. For example, the ER3401's erase time is only 10 ms, well down from 100 ms for earlier versions. "And we've reduced the write time to 1 ms whereas the fastest previous EAROM was 10 ms," says Brian Cayton, General Instrument's memory-product manager. Access time has been reduced to under 1 μs from a previous best of 2 μs. ■■

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2N6121	45V, 4A, 40W, NPN	General P	*	.50
2N6122	60V, 4A, 40W, NPN	Genera	se*	.55
2N6123	80V, 4A, 40W, NPN	Gene	base*	.59
2N6124	45V, 4A, 40W, PNP	Ge	ibase*	.55
2N6125	45V, 4A, 40W, PNP		pibase*	.59
2N6126	45V, 4A, 40W, PNP		Epibase*	.63
2N6288	30V, 7A, 65W, NPN		Epibase*	.51
2N6290	50V, 7A, 65W, NPN		Epibase*	.54
2N6292	70V, 7A, 65W, NPN		Epibase*	.54
MJE13004	350V, 4A, 75W		ouble-diffused Mesa	1.35
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MJE13006	350V, 8A, 80W		ble-diffused Mesa	1.95
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MJE13008	350V, 12A, 100W		ble-diffused Mesa	3.30
MJE13009	400V, 12A, 100W		ble-diffused Mesa	3.95
TIP31	40V, 3A, 40W, NPN		Epibase*	.47
TIP31A	60V, 3A, 40W, NP		Epibase*	.50
TIP31B	80V, 3A, 40W, NP		Epibase*	.54
TIP31C	100V, 3A, 40W, NP		Epibase*	.58
TIP32	40V, 3A, 40W, PNP		Epibase*	.50
TIP32A	80V, 6A, 65W, NPN		Epibase*	.53
TIP32B	100V, 6A, 65W, NP		Epibase*	.58
TIP32C	40V, 6A, 65W, P		Epibase*	.61
TIP41	60V, 6A, 65W, PNP		Epibase*	.60
TIP41A	80V, 6A, 65W, PNP		Epibase*	.65
TIP41B	100V, 6A, 65W, PNP		Epibase*	.68
TIP41C	250V, 1A, 40W, NPN		Epibase*	.79
TIP42	300V, 1A, 40W, NPN		ibase*	.66
TIP42A	350V, 1A, 40W, NPN	G		.73
TIP42B	400V, 1A, 40W, NPN	Ge		.79
TIP42C	60V, 3A, 40W, PNP	Gene		.89
TIP47	80V, 3A, 40W, PNP	Genera	ase	.62
TIP48	100V, 3A, 40W, PNP	General	Base	.66
TIP49	40V, 6A, 65W, NPN	General	Base	.70
TIP50	60V, 6A, 65W, NPN	Gen	Base	.82
TIP110	60V, 4A, 50W, NPN Darlington	Gene	*	.70
TIP111	80V, 4A, 50W, NPN Darlington	General		.75
TIP112	100V, 4A, 50W, NPN Darlington	Gen		.84
TIP115	60V, 4A, 50W, PNP Darlington	Ge		.79
TIP116	80V, 4A, 50W, PNP Darlington	Ge	base*	.84
TIP117	100V, 4A, 50W, PNP Darlington	General Pur	pibase*	.94
TIP120	60V, 8A, 65W, NPN	General Purpos	pibase*	.86
TIP121	80V, 8A, 65W, NPN	General Purpo	Epibase*	.96
TIP122	100V, 8A, 65W, NPN	General Purpo	Epibase*	1.10
TIP125	60V, 8A, 65W, PNP	General Purpose	Epibase*	.92
TIP126	80V, 8A, 65W, PNP	General Purpose	Epibase*	1.03
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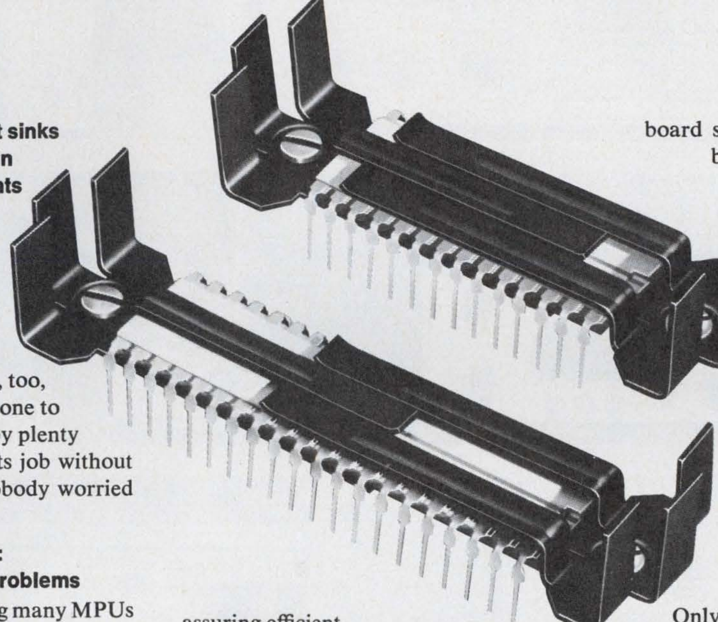


Unique new Micro-Clip heat sinks permit MPU operation in much hotter environments

Time was when microprocessors posed no thermal problems for designers. That's because earlier MPUs required very little power — up to 250 mw or maybe ½ watt at most. Then, too, designers usually spec'd only one to a circuit board. Surrounded by plenty of air, the lonely MPU did its job without generating much heat. So nobody worried much about heat dissipation.

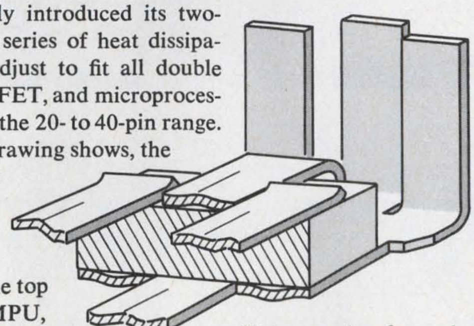
Today's reality: serious MPU thermal problems

Today, designers are specing many MPUs on the same board. And these boards often must operate in military-type environments where ambient temperatures reach 71°C. Also, today's MPUs do more and, therefore, generate much more heat than earlier models. For example, they often function as both the arithmetic logic unit and the control section of a computer. These factors combine to cause serious thermal problems. Coping with these problems has become an increasingly important part of a circuit designer's job.

IERC finds efficient solution

To solve growing MPU thermal problems, IERC recently introduced its two-piece "Micro-Clip" series of heat dissipators. These units adjust to fit all double DIP, CMOS, MOS-FET, and microprocessor packages within the 20- to 40-pin range.

As the adjacent drawing shows, the Micro-Clip's unique spring-finger design lets the dissipator make good, solid contact with both the top and bottom of the MPU, assuring efficient heat transfer from case to dissipator. Tests show these units dissipate up to 100 percent more heat than conventional glued-down devices.



Unique spring-finger design helps assure efficient heat transfer.

Staggered-finger design also assures more efficient heat dissipation

Micro-Clip series dissipators capitalize on IERC's patented staggered finger design. Heat radiates to the ambient, never transfers from one finger to another. In forced air modes, the staggered fingers maximize turbulence, further increasing heat transfer efficiency. Three finger heights are available — ¼ in., ½ in., and ¾ in. — to meet varying space and dissipation requirements. Micro-Clip dissipators weigh only 4 grams and require only .6 in.[2] more board space than the IC device itself. So board densities and spacing between rows of, for example, double DIPs and CMOSs are unaffected.

Stocking problems greatly reduced

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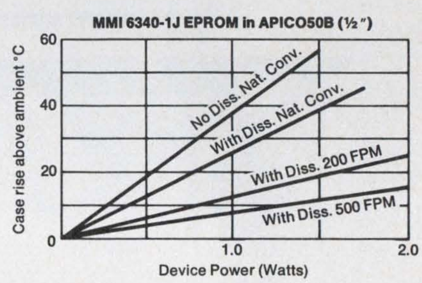
Only two screws or rivets or dots of thermally conductive epoxy are needed to fasten Micro-Clip dissipators securely into position. Mounting Micro-Clip units to MPUs already mounted to boards requires no disassembly.



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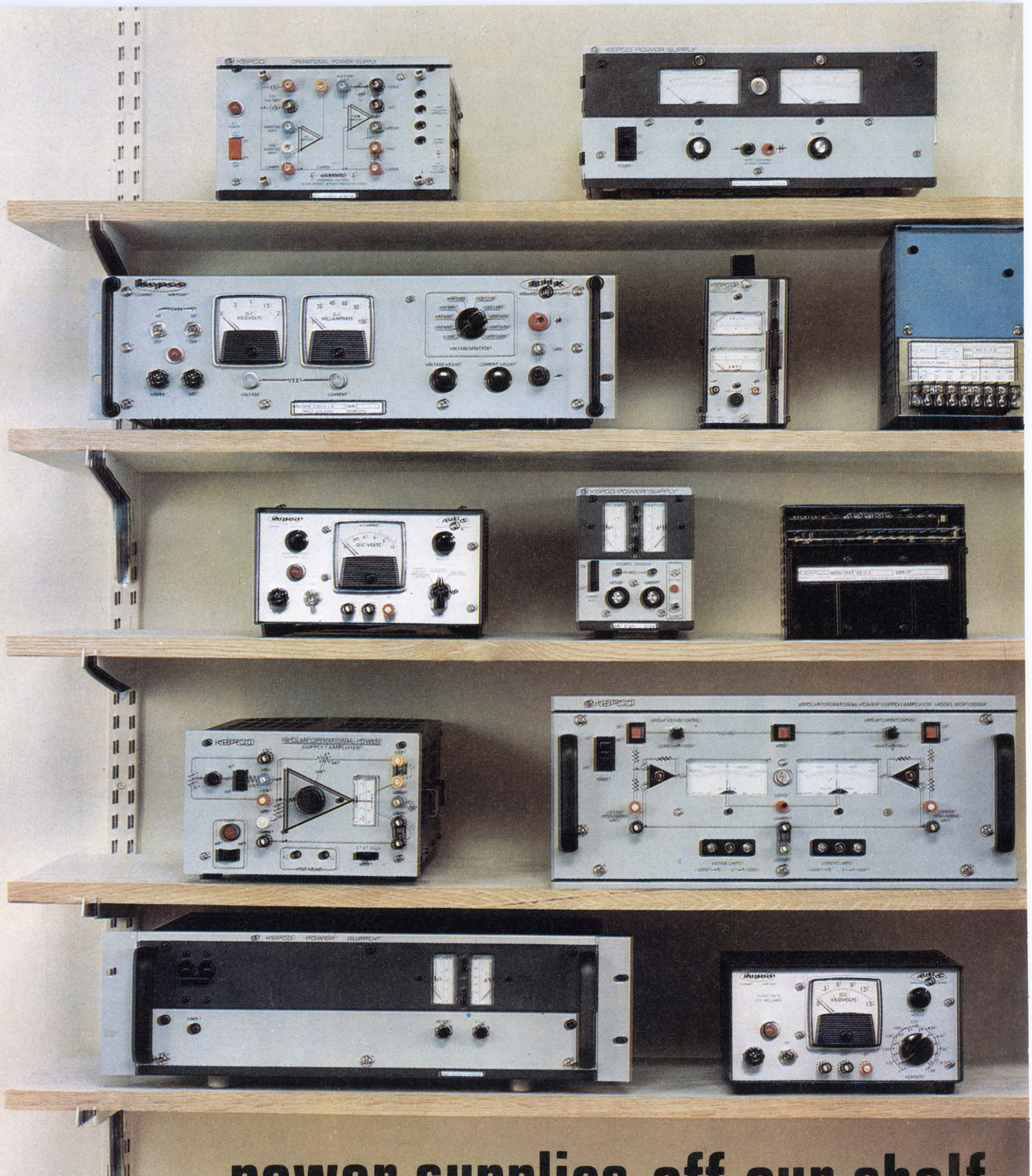

Washington Report

Navy ships to be protected from missile attacks

Next year 284 Navy surface ships will begin to be outfitted by Raytheon Corp. with a new electronic warfare (EW) suite, the AN/SLQ-32 (V). It will protect them against incoming missiles by detecting and jamming enemy radar.

The new EW suite replaces current manually operated systems based on vintage-mid-1950s vacuum-tube technology, and uses computer control for instant response. It will be installed on small amphibious and auxiliary craft, medium-size combatants such as destroyers and frigates, and cruisers and large amphibious and auxiliary vessels. First installation is planned for May, 1978 on a Navy destroyer (DD 973), with all the ships to be outfitted by the end of 1981. Cost before inflation is estimated at $180 million.

In a head-to-head prototype competition known as the Design to Price Electronic Warfare Suite (DPEWS), Raytheon was declared the winner over Hughes Aircraft. A four-year contract is due to be awarded in April after a meeting of the Defense Systems Acquisition Review Council (DSARC).

Exxon will use RCA Satcoms for off-shore platforms

Despite objections from competing communication-satellite-system operators, the Federal Communications Commission has approved Exxon's request to put portable satellite receivers on its off-shore oil rigs to use the RCA Satcom system. The 4.5 m antennas, which use band-edge frequencies of the share-spectrum allocation, will be mounted on platforms in the Gulf of Mexico, the Atlantic and Pacific Oceans, and off the Alaskan coasts to warn of approaching storms as well as provide a two-way data link.

Comsat General and Western Union had objected on the grounds that the Exxon application was essentially maritime, their MARISAT system should provide the service. ITT and AT&T filed similar protests. However, FCC ruled that since the Exxon stations are mobile, they are exempt from any restrictions imposed on temporary-fixed stations in terrestrial-fixed radio services.

Navy prefers Michigan for Seafarer ELF system site

Public hearings on the Navy's proposed Seafarer system for extremely-low-frequency (ELF) communications with submerged submarines are scheduled to run all during April in Michigan, Nevada and New Mexico. But the Navy has made it clear that its favored site is on Michigan's Upper Peninsula.

Although the hearings are required before the final environmental-impact statement can be written and a site chosen, the Navy's preliminary statement concludes that the most cost-effective site would be near K. I. Sawyer Air Force Base, just south of Marquette, MI. Total system costs there (including receivers in the submarines and the first 10 years of operation) are put at $593-million, and at $837-million for an alternate site at Nellis Air Force Base in Nebraska and $718-million at White Sands Missile Range in New Mexico.

Further, nearly global coverage would be provided by the Michigan site because of the nonconductivity of the rock strata there, the Navy believes, while the New Mexico site would cover only the adjacent waters around North America and the Nevada site slightly more.

The system operates in an FM mode at a center frequency of 76 Hz and an estimated data rate of 10 bits/min., which is considered adequate for communicating with submerged nuclear submarines. The Navy proposes to build five transmitters at the Michigan site and install 2400 miles of buried antenna cable in segments over a 4000-square-mile area.

FAA research aimed at air-traffic control in 1990s

The Federal Aviation Administration's $85-million engineering, research and development (ER&D) request for the new fiscal year is a down payment on an air-traffic control system for the 1990s, FAA Administrator Dr. John McLucas told the House Transportation Subcommittee.

Introducing a new technology into the air-traffic system requires 15 to 20 years from concept formulation to field implementation, he said, although some of the results will be felt sooner. Technical programs in ER&D include conflict alert, air-traffic-delay reduction, wind-shear-and-microwave landing systems.

"High-priority" has been given by the FAA to implementing a conflict-alert capability at en route centers, as well as to minimum-safe-altitude warning systems, according to McLucas.

The wind-shear problem is being studied by testing detection devices at Washington, DC's Dulles and Chicago's O'Hare airports, as well as by evaluating an anemometer-based system. Possible solutions to air-traffic delay problems include developing a wake-vortex advisory system, which will allow reduction of the longitudinal separation requirements, and a discrete-address beacon system as well as an airport-surface-traffic control system to allow more aircraft to operate in the same traffic areas.

Capital Capsules: **A next-generation multi-spectral scanner**, the thematic mapper, will be built for NASA's Landsat-D by the same company that built the multi-spectral scanner in the current Landsat program: Hughes Aircraft. An object-plane linear scanner, the instrument will provide one more channel of imaging (six) and better resolution (30 m to 80 m) than the current scanner. It was chosen over a TRW candidate using an image-plane linear scanner from Perkin-Elmer. The Landsat-D is due to be launched in 1981. . . . The Pentagon has **increased the single-pulse power output of rare-gas halide lasers** operating in the ultraviolet and visible spectra from 1 joule to more than 350 joules over the past year as part of its High Energy Laser (HEL) weapons program. Efficiency was only 10%, however. In the coming year, research will be focused on scaling up the output of hydrogen-fluoride chemical lasers operating in the infrared spectra (2.7 m).

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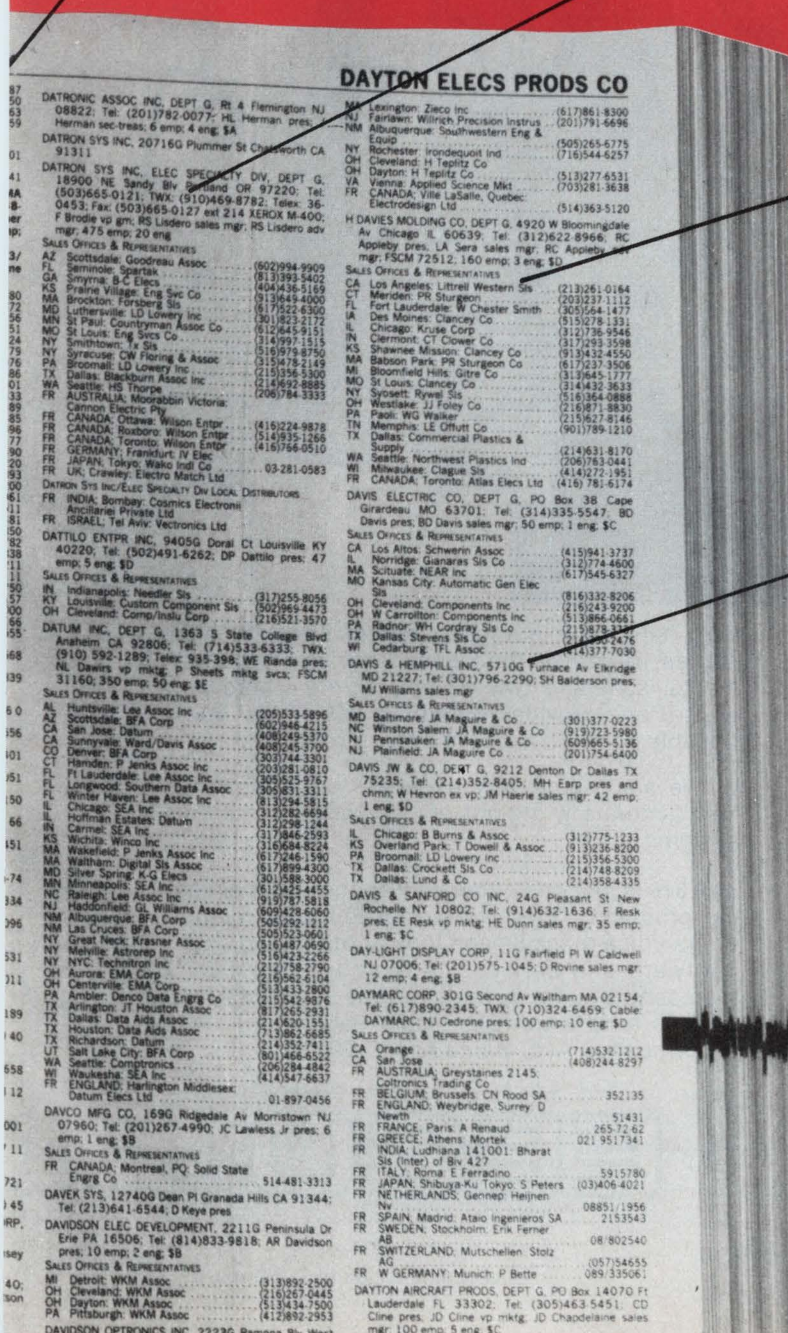

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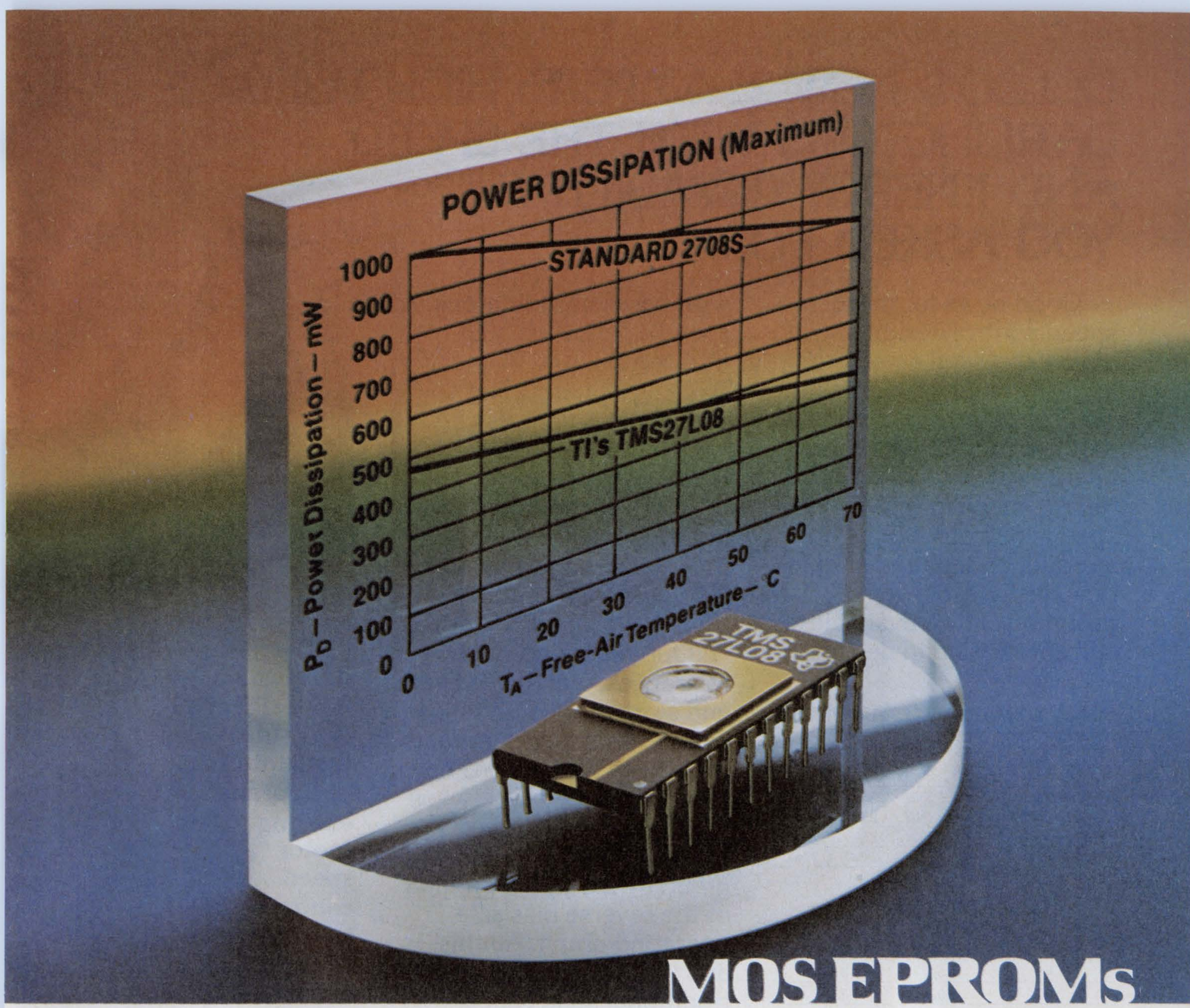

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Pin-for-pin compatible with the standard 2708, it requires less than half the power. Typically 245 mW.

The TMS 27L08 also features ±10% power supply voltage tolerances, and increased output drive capability. When interfaced with standard TTL, the TMS 27L08 has guaranteed dc noise immunity in both high and low states.

Easily erased and reprogrammed, the new TMS 27L08 is ideal where programs must be debugged quickly. It's available now in a 24-pin ceramic DIP at $37.75 each (100 pieces).

For existing designs, plug in TI's TMS 2708. It's identical to the standard version; $32.75 each in 100 pieces.

Once your program is defined, you can use the economical, pin-compatible, mask programmed TMS 4700 ROM for large production runs.

To get your 27L08s fast, or for more data on the 27L08, 2708, and 4700, call your TI distributor. Or write Texas Instruments, P. O. Box 1443, M/S 669-27L08, Houston, Texas 77001.

TEXAS INSTRUMENTS
INCORPORATED

CIRCLE NUMBER 36

63124

DELCO'S NEW 25-AMPERE HIGH VOLTAGE DARLINGTONS WITH THE SPEED AND ENERGY CAPABILITY YOU ASKED FOR.

Good news for motor speed control designers who have expressed a need to upgrade horsepower ratings. The 25-ampere gain of these new Darlingtons permits increased horsepower ratings of existing AC motor speed control systems and a reduction in paralleling in new designs. However, grouping of t_{off} is available for current sharing in designs with parallel Darlingtons. A speed-up diode is built into the DTS-4074 and DTS- 4075 permitting data sheet t_f typicals of 1.0 μs. Drive circuit techniques involving $I_{B2} \geqq 2$ A and a Baker clamp produce t_f typicals in the 0.4-0.6 μs range for the DTS-4066, DTS-4067, DTS-4074, and DTS-4075.

Our experience with tolerances, faults, transients, and start-stall conditions in most systems convinces us that these Darlingtons have the right trade-off between speed and peak power handling capability. Note the greater than 10 kVA region of the reverse bias safe operating graph. All this, and you still get Delco's traditional solid copper TO-3 hermetic package that has a conservative 0.75°C/W thermal resistance.

These Darlingtons are already in high volume production and are available on distributor shelves. Prices, applications literature, and data sheets from your nearest Delco sales office or Delco distributor can complete the story on these new Darlingtons.

MAJOR PARAMETER LIMITS

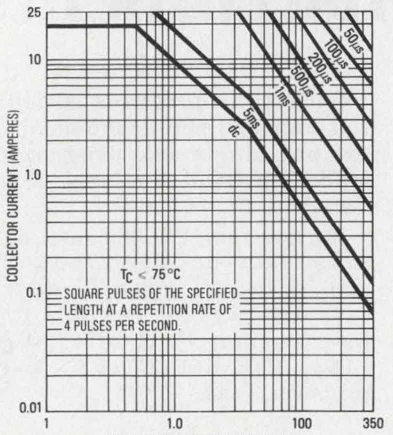
Type	h_{FE} @25A	h_{FE} @10A	V_{CEO} (sus)	V_{CE} (sat) @20A	I_{CEO} @600V
DTS-4066	5	75	350V	3.5V	0.25mA
DTS-4067	10	150	350V	2.0V	0.25mA
DTS-4074	5	75	350V	3.5V	0.25mA
DTS-4075	10	150	350V	2.0V	0.25mA

TYPICAL SWITCHING

	DTS-4066 DTS-4067	DTS-4074 DTS-4075
t_r	0.5μs	0.5μs
t_s	5.0μs	3.2μs
t_f	4.5μs	1.0μs

NPN triple diffused silicon Darlingtons are packaged in solid copper cases conforming to JEDEC TO-3 outline dimensions.

SAFE OPERATING CURVES

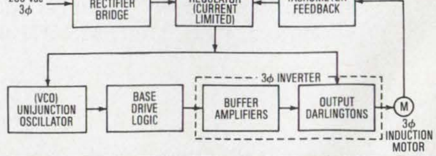


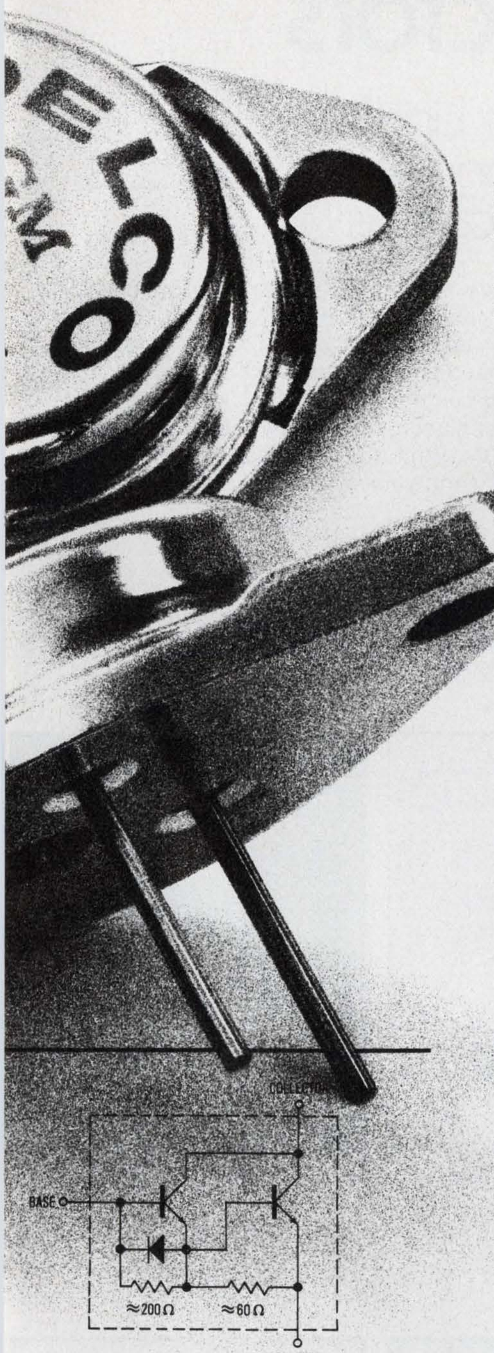
Features of Delco's new DTS-4066, 4067, 4074, 4075 Darlingtons.

- ☐ **Upgrade existing motor speed control horsepower ratings.**
- ☐ **Reduce need for paralleling in new systems.**
- ☐ **Offer switching speed improvements over our earlier types.**
- ☐ **Achieve greater than 10 kVA peak power dissipation.**
- ☐ **Available with t_{off} grouping**
- ☐ **Delco hermetic copper package with 0.75°C/W.**
- ☐ **Currently in high volume production.**

208/220 Vac, 3ϕ MOTOR SPEED CONTROL

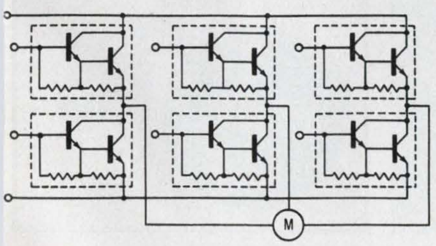
6 STEP WAVEFORM—5 to 60 Hz—1.5% SPEED CONTROL ACCURACY





SPEED-UP DIODE USED ON DTS-4074/4075 ONLY

3ϕ DARLINGTON INVERTER DTS-4066-4067



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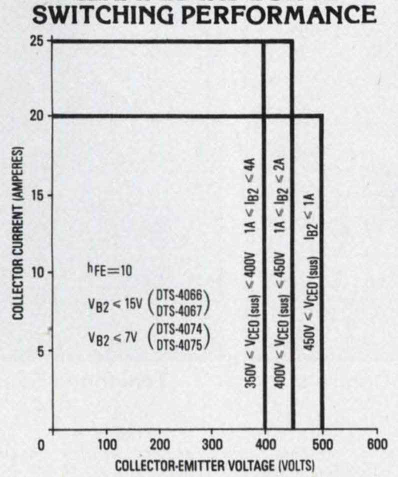

Delco Electronics
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Vactec serves manufacturers of a wide range of modern electronic products. Pictured are a few examples. All these devices are both made and sold by Vactec, including complete lines of LDR's (photoconductive cells, CdS and CdSe); silicon solar cells, as well as silicon high speed and blue enhanced cells; NPN phototransistors and darlingtons; opto-couplers (LED/LDR, lamp/LDR and neon/LDR); selenium photovoltaic cells; silicon photodiodes, blue enhanced and PIN; and custom C-MOS and bi-polar IC's. Write for technical bulletins on the types that suit your requirements. Or send your application, and Vactec will recommend the right cell for the job.

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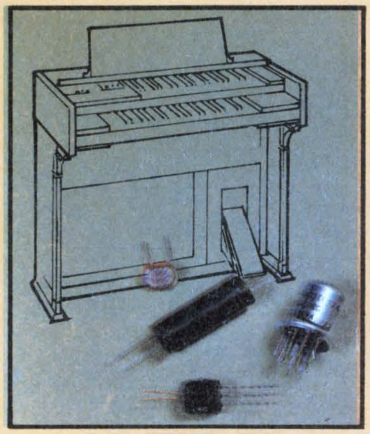
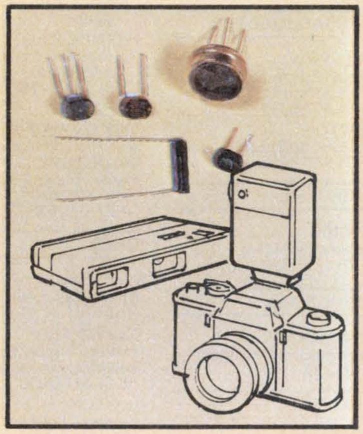


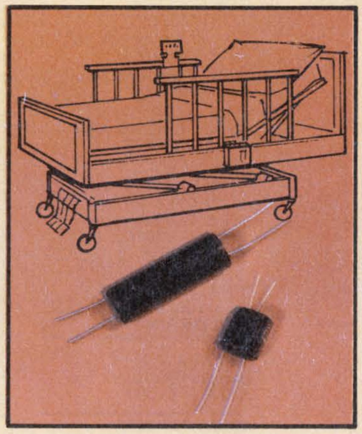
Electronic Organs

LED or lamp/LDR Vactrols for audio, and CdS cells for swell pedal controls.



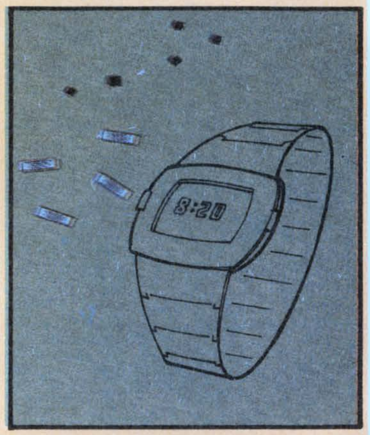
Cameras and Projectors

CdS or blue enhanced silicon photodiodes for automatic shutter timing; aperture servo systems for automatic projector focus; and slave flash controls.



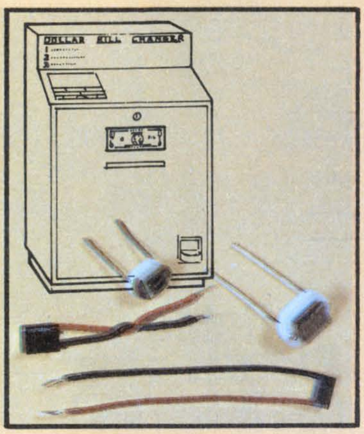
Triac Motor Controls

A special Vactrol gates a triac for forward and reverse motor operation as in hospital beds.



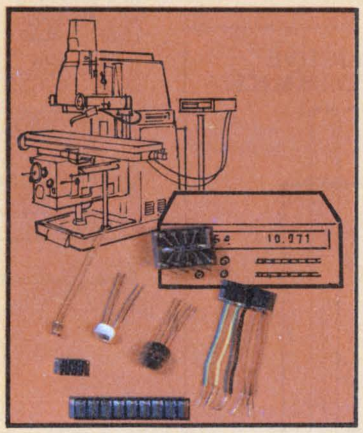
LED Watches

Photoconductive or phototransistor chip controls LED brightness.



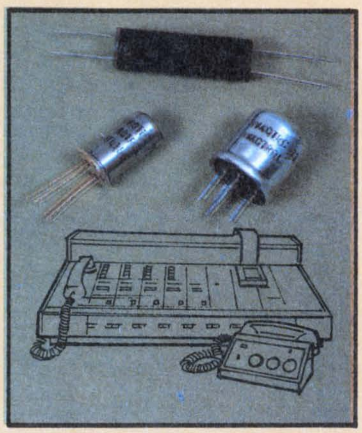
Dollar Bill Changers

Silicon photovoltaic cells analyze optical characteristics.



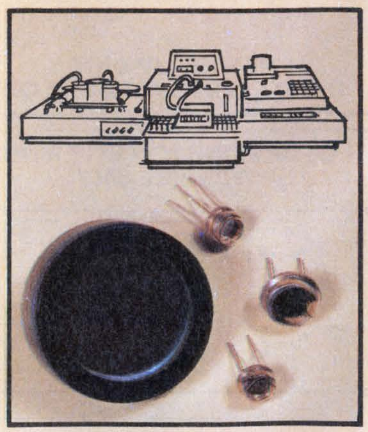
Machine Tool Controls

High-speed photovoltaic cells or transistor arrays help computer control repetitive operations, non-contact sensing, and counting and weighing.



Telephone Equipment

Neon/LDR Vactrols sense ringing. Direct a-c coupling, slow LDR response isolates electronics from noise.

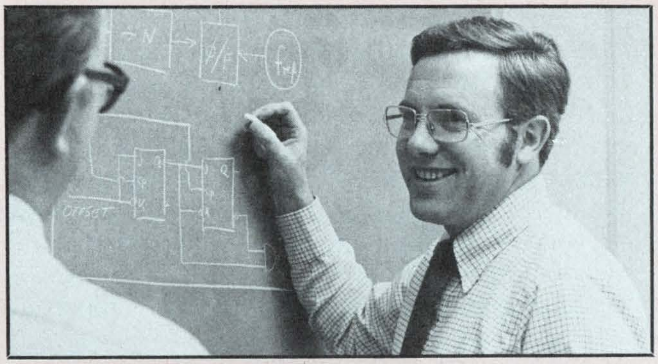


Scientific Instruments

Blue enhanced silicon or selenium photovoltaic cells detect solutions densitometrically for precise blood chemistry and other analyses.

CIRCLE NUMBER 41

MOS μP or bipolar slice? It's more than a matter of speed



Peter Alfke, Fairchild Semiconductor

MOS μP or bipolar bit slice? What are the trade-offs? Which is best, speediest, lowest in build cost, or most flexible for your application?

"Speed is the place to start," says Peter Alfke of Fairchild Semiconductor. "As manager of applications engineering for digital products, I deal with both sides, the MOS F8 and the bipolar Macrologic.

"You usually have a certain amount of execution time available. If you have enough time and memory, the F8 or the 8080 or the 6800 can do any job. But if you have to do a multiply in 6 μs, every μP is too slow by a factor of 100 or so."

But Steve Herrick of Computer Linguistics warns:

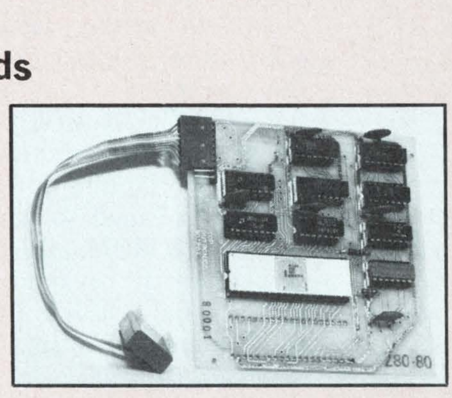
"The computing-speed criterion fools people. You may not have a computing-rate constraint at all, yet have to go bit-slice because of the need for large files on-line. Why? Because floppies can't handle really big jobs. If hard disc is necessary, you simply have to go to a faster machine than MOS."

Herrick, the President of the Colonie, NY, software firm, also likes the emulation capability of the bit-slice approach. "When a hardware manufacturer changes instruction sets or just discontinues a line of hardware, you don't want to throw out a 20-man-year software

(continued on page 64)

David Uimari, Raytheon Semiconductor

Swap the 8080 CPU for a Z80 without changing boards

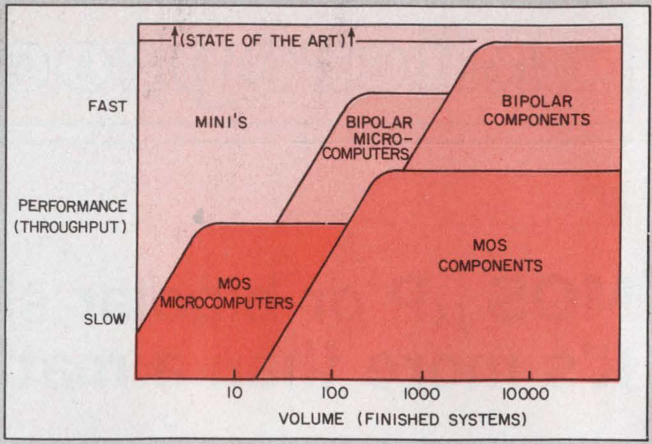


Don't replace the entire CPU card in an Altair, Imsai or any other Altair-bus-compatible microcomputer. To change the CPU from the 8080 to a Z80 simply plug the Z80-80 piggy-back card into the 8080's socket, and a cable into the 8212's vacated socket.

A system monitor on paper tape comes with the board, as well as a Z80 manual. The board costs $159.95, and delivery is from stock.

R.H.S. Marketing, 2233 El Camino Real, Palo Alto, CA 94306. (415) 321-6639.

CIRCLE NO. 500



Processor volume vs performance

(continued from page 63)

library. By building new bit-slice hardware that uses the old instruction set you can keep it and continue to use it."

"But the moment you consider bit-slice, you're talking 30 to 50 chips," says Alfke. "You're leaving the realm of a \$20 solution with a μP. True, your bit-slice approach gives you a new degree of freedom, a more efficient, more dedicated, and more specialized solution.

"If you can possibly do your job with a MOS μP, do it," Alfke advises. "In a bit-slice design, if you can avoid the insanity of inventing your own instruction set, do that," he adds, acknowledging that bit-slice microcoding lets you use existing supported instruction sets, and does not force anyone to create "orphan" command sets. "Bipolar and supported instruction sets come together in our 9440," notes Alfke. "It's a Nova for a lot less money but without the support hand-holding."

The Transitron 1601 slated for 1978 has its own fixed instruction set, too (see ED Microprocessor Design, March 1, 1977, page 41), along with fast bipolar hardware.

"The advantages of both—the fixed instruction set of the μP, plus the speed of bipolar—are merged in bipolar μCs like our 8X300," Joe Conway of Signetics Applications observes. "The 8X300 is very good for fast controllers. In 250 ns, it can take in pieces of data, massage them, and dump them back out. But if you have to really crunch numbers, a bit-slice gives you much more—we don't have the register architecture for top speed arithmetic."

"All these different approaches have their place," notes Dave Uimari, LSI product manager at Raytheon Semiconductor. "But a big factor often forgotten is the number of units you are going to build. If you can write development costs off over a long run of finished systems, you'll be able to take your choice—lots more throughput for the same build cost, or much lower unit cost for a given performance level.

"We plot the whole thing out for the design engineers we work with," Uimari adds, pointing to a volume-versus-performance chart (see figure). "All boundaries on the chart are in motion as new technologies develop; but you need an overview of five solutions to know which ones can apply to your problem. The bipolar μCs showed up just recently in the very middle, where four other approaches all used to compete. Everything is moving upward and to the left, and eating up territory that once belonged to the minis alone. Bit slices like our 2901 are in the "bipolar components" group. They're moving the same way, as hardware speeds go up and as development aids like our RAYASM microcode assembler cut the basic development costs."

Jumbo ROM offers 32-k storage for PPS systems

Able to cut the package count in PPS processing systems, the A66XX, a 32-k ROM, offers 4 k × 8 of program storage. The ROM is believed by Rockwell to be the largest unit on the market.

Two main features of the ROM are dynamic address decoding and device-select circuitry. Up to 16 ROM circuits can be selected directly with the device's 12 address and four chip-select inputs, and memory easily expanded through normal or "virtual" bank switching. The virtual mode permits simple switching-command arrangements.

The 32-k ROM, which consists of a 156 × 242 mil chip housed in Rockwell's standard 42-pin plastic package, is designed as a direct replacement for the smaller capacity A52XX and A05XX ROMs. Price for the ROM depends on pattern and quantity but is approximately \$23 in 1000-unit lots.

Rockwell International, 3310 Miraloma Ave., P.O. Box 3669, Anaheim, CA 92803. (714) 632-8111.

CIRCLE NO. 501

Keyboard and display round out μC evaluation kit

Available in kit form, the MEK6800D2 microcomputer evaluation system even includes a keyboard and a display. When assembled, the system is a fully functional microcomputer based on the 6800 μP.

The MEK6800D2 consists of two boards—the microcomputer module (9.75 × 8.3 in.) and a keyboard/display module (10 × 6.25 in.) that includes an audio cassette interface designed to accept data recorded according to the tape interface known as the "Kansas City Standard."

Six 7-segment LED readouts on the keyboard module display the four-digit hex address and the two-digit data. The keyboard has all hexadecimal keys plus eight additional command keys. The μC module also contains a 6800, a JBug-monitor ROM, three 6810 RAMs, two 6820 PIAs, a 6850 ACIA and a 6871B clock. In addition, the system can be expanded on a breadboard area with up to twelve 16-pin ICs and two 24-pin DIPs.

The price is $235, less power supply and cassette recorder. Delivery is from stock.

Motorola, 3501 Ed Bluestein Blvd., Austin, TX 78721. (512) 928-2600.

CIRCLE NO. 502

Time-sharing software available for 2900 development

Developed to generate microinstructions for use with the Am2900, the AMDASM software system is available worldwide through Computer Science Corporation's Infonet Service. Written by Advanced Micro Devices, the program provides software assistance and documentation for writing and modifying microprograms and generating tapes for PROM programmers.

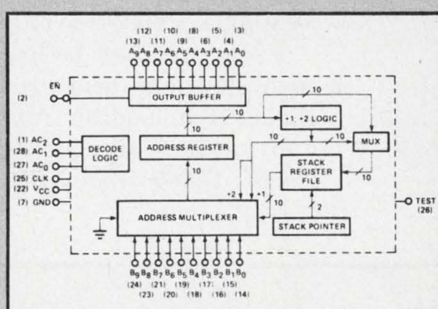
AMDASM includes a framework for a common language, automatic accounting information and billing control. Budget limits, character-rate option and batch rates make AMDASM cost-competitive with in-house software.

Documentation currently available explains how to interact with AMDASM to microprogram all control signals and memory. Variable instruction set microprogramming makes field service and system enhancements easy, since they require only additional data in the microprogram memory.

Advanced Micro Devices, 901 Thompson Pl., Sunnyvale, CA 94086. Elliot Sopkin (408) 732-2400.

CIRCLE NO. 503

Control-store sequencer simplifies microprogramming



All random logic needed to do microprogram sequencing in bipolar μPs can be replaced by the 8X02, a control-store sequencer. This microprogrammed control section for computers, controllers and sequenced logic elements, combines with standard ROMs or PROMs to form a complete controller.

The 8X02 is a low-power Schottky device that can address up to 1 kword of microprogram expandable to any microprogram size by conventional paging techniques. External page registers, when provided, can be controlled either entirely or partially by the microprogram.

Compared with other available units, the 8X02 provides several advantages. The 1-k addressing capability is not available in other units, nor is the 8X02's subroutine-nesting capability. The controller has a four-way stack-register file and offers conditional nesting

(continued on page 66)

(continued from page 65)
for branching to a subroutine or for handling interrupts automatically.

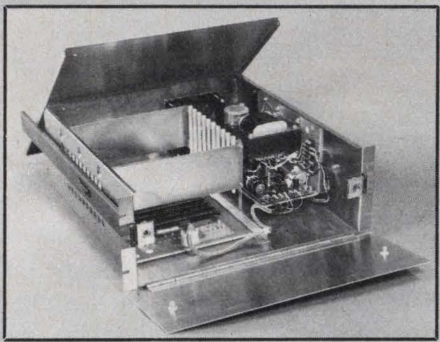
There are three control lines for the three-bit command code; control instructions include increment, test-and-skip, and conditional-branch-to-subroutine. One 8X02 cycle takes only 80 ns. The unit operates from a +5-V supply and consumes 1 W.

The control-store sequencer is housed in a 28-pin plastic DIP and costs $19.45 when purchased in 100-unit lots.

Signetics, 811 E. Arques Ave., Sunnyvale, CA 94086. (408) 739-7700.

CIRCLE NO. 504

Micromodule chassis and racks ease system development



Several Micromodule card cages and a power supply have been added by Motorola to support M6800-based equipment development. Two card cages are available: one with five card slots, the other with 10. Both cages have motherboards that are pin-compatible with all Micromodules and EXORciser modules.

The available power supply delivers 15 A at +5 V dc, 2.5 A at +12 V dc, 1.5 A at −12 V dc and 0.1 A at 8 V ac. Short-circuit, overload and overvoltage protection are provided. A remote-voltage-sensing capability for the 5-V output can compensate for as much as a 0.5-V drop along the connecting leads. The supply requires a single-phase, 47-to-420-Hz input from 95 to 125 V or 205 to 250 V.

A bare chassis with five card slots costs $98 and a 10-slot unit costs $147. Card cages with power supplies and chassis built-in cost $610 and $660, respectively. Both fit 19-in. RETMA racks. By itself, the power supply costs $295. All units are available from stock.

Motorola Semiconductor Products, P.O. Box 20294, Phoenix, AZ 85036. (602) 244-6900.

CIRCLE NO. 505

Upgraded software permits easy program development

A substantially upgraded version of Imsai's self-contained software-operating system for 8080-based machines is now available. The enhancements offer a package for developing medium-size assembly-language programs. Software features include a debugger with multiple dynamic and static breakpoints, number conversions, memory searches, an I/O-port control, a trace and hex arithmetic. There is enough symbol-table space for 8192 bytes. A facility for adding device drivers to support a wide variety of I/O devices is available (teletypewriter driver is included).

Programs may be loaded from industry-standard object paper tapes. The software resides in high-order memory locations so that it may reside with application programs and Basic. A line-editor routine is also included. A paper-tape listing of the program costs $40 and includes all source listings. Delivery is from stock.

Imsai, 14860 Wicks Blvd., San Leandro, CA 94577. (415) 483-2093.

CIRCLE NO. 506

Z80 microcomputer board fits into Intel MDS systems

A $10,000 investment may not be necessary when switching from an MDS-800 development system for 8080 μPs to a system that handles Z80s. The Z80/MDS microcomputer board from Relational Memory Systems can convert MDS-800 development systems into a system for Z80 programs for less than $1500.

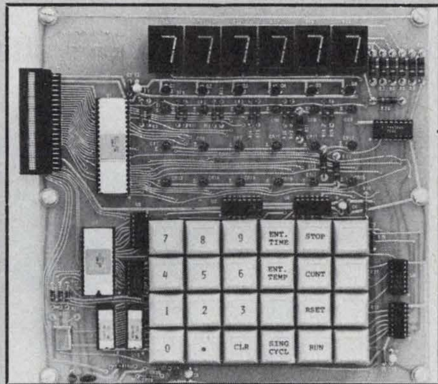
The Z80/MDS board runs with ICE-80, ICE-30, ROM simulators and other Intel 8080 accessories. The board also provides a single-cycle capability via a switch mounted on the board. LEDs on the board indicate whether the Z80/MDS is accessing memory or I/O ports.

Two versions of an assembler program are supplied with the board. One is disc-based for users of the ISIS DOS system, and the other is a stand-alone, one-pass assembler that operates five times faster than Intel's stand-alone assembler. The complete μP board and software package costs $1490, and delivery takes 30 days.

Relational Memory Systems, 150 Saratoga Ave. 332, Santa Clara, CA 95050. James Kelley (408) 248-6356.

CIRCLE NO. 507

Microcomputer controller offers wide choice of options



A completely self-contained microcomputer family, dubbed the HT-1000, is designed specifically for control-systems applications. All units in the HT-1000 series can monitor or control up to 160 points as well as provide the user up to 24 function keys.

Input options for the system include ac signals, logic levels, switch contacts, dc voltages and resistance changes, while output options include solid-state relays up to 220 V at 40 A, SCR control and dc voltages. Data can be displayed on up to six 0.6-in.-high LED displays or as many as 18 LED lamps.

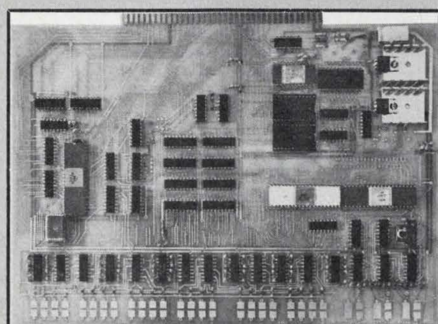
Each HT-1000 uses a 6502 μP and comes with its own power supply, which requires about 25 W. Typical size of the controller board is 8 × 8 in., and the operating temperature range 0 to 50 C. But wider ranges are available.

A typical HT-1000 system, which costs about $745 (in 100-unit lots and depending upon program complexity), may consist of eight logic-level or switch inputs, eight 115-V-ac, 1.5-A optically isolated relay outputs, eight LED indicators, a 16-key control panel, a three-digit numeric display, a power supply and a program.

TechnoVation, 14 Crandall Ave., Pompton Lakes, NJ 07442. (201) 839-0740.

CIRCLE NO. 508

Microcomputer card comes in tutorial & industrial models



Capable of being expanded into a full microcomputer, the Datac 1000 microprocessor card is available in both a tutorial version and an industrial model. The processor card, claimed by Datac Engineering to be the most adaptable card around, is based on the 6502 microprocessor.

The tutorial card carries the μP, 256 bytes of RAM, a one-bit serial output latch, eight data, eight address and nine control touch pads (used for data entry) and eight data and eight LED address indicators. On-board regulators permit operation from raw dc, and a single-cycle operating mode permits simple program debugging.

The expanded industrial version permits 16-bit addressing and has 1 kbyte of RAM sockets for 2 kbytes of UV PROM, a ROM containing I/O routines for a teletypewriter as well as a current loop or RS-232 interface, a cassette interface, two parallel I/O ports, and a bus structure that permits simple expansion.

Unique touch pads used by Datac facilitate data and address entry and permit faster bit-by-bit data entry than entry via conventional toggle or slide switches. Aside from the address and data-bus pads, controls are provided for halt, run, reset, single step, normal,

(continued on page 68)

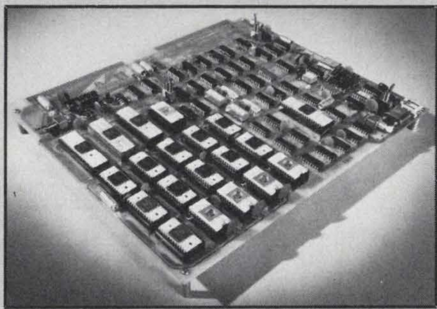
(continued from page 67)
step, examine, load, and deposit. The addresses, data and status are displayed on LEDs.

Prices for the Datac 1000 start at $185 for the tutorial version, including manual, and end up at $345 for the industrial card—each in single-unit quantities. Delivery is stock to 60 days.

Datac Engineering, P.O. Box 406, Southampton, PA 18966. (609) 854-7852.

CIRCLE NO. 509

Microcomputer kits available for all experience levels



A series of inexpensive microcomputer kits has been designed to meet various needs—from the beginner's to the advanced engineer's. The kits in American Microsystems' EVK series are based on the 6800 μP and range in price from $133 to $765.

There are three kits: the EVK-99, 100 and 200—plus an assembled version of the 200 called the EVK-300. All come with 10.5 × 12 in. PC boards with two 86-pin edge connectors, one for the μP bus lines and one for the I/O.

The EVK-99 is for beginners, and features 6800-family parts—one μP, four 128 × 8 RAMs, one PIA, one 2-k × 8 ROM and one ACIA. The mid-range kit, the EVK-100, costs $295 and contains all the EVK-99 parts plus enough TTL circuits to make a terminal-communication port.

For the weathered engineer the EVK-200 includes everything in the EVK-100, but also I/O interfaces, a serial RS-232 port, 1 k of RAM, 2 k of EPROM, an on-board programmer, a crystal clock and switch-selectable baud rates from 0 to 9600—all for $495. Its fully assembled version, the EVK-300, costs $765 and also includes four EPROMs and a paper tape containing a version of Tiny Basic.

American Microsystems, 3800 Homestead Rd., Santa Clara, CA 95051. Tom Eden (408) 246-0330.

CIRCLE NO. 510

Micro Capsules

A full 16-bit microcomputer on a single chip is currently in development by Texas Instruments, Dallas. The chip, dubbed the TMS 9940, will use a subset of TMS 9900 instruction set and have ROM, RAM, I/O and the processor all on a single chip. . . . **Containing ROM, RAM, timer, clock and μP on a single chip**, the 6801 microcomputer will soon be released by Motorola, Austin, TX. Instructions will be compatible with the company's 6800 μP and the chip will hold 1024 bytes of ROM and 64 bytes of RAM. . . . **Another combination processor/UV PROM** will soon be available from Intel, Santa Clara, CA. The 8041/8741 as it will be called is intended for universal interface development and will have an instruction cycle time of 2.5 μs. On the 8741 will be 1024 bytes of UV EPROM and the 8041 is a pin-compatible mask-programmed version. . . . **Look for some new software from National Semiconductor**, Santa Clara, CA, to support the PACE and SC/MP μPs by mid-1977. For the PACE will be a 7-k ROM software package containing Basic and for the SC/MP will be a full resident-assembler package.

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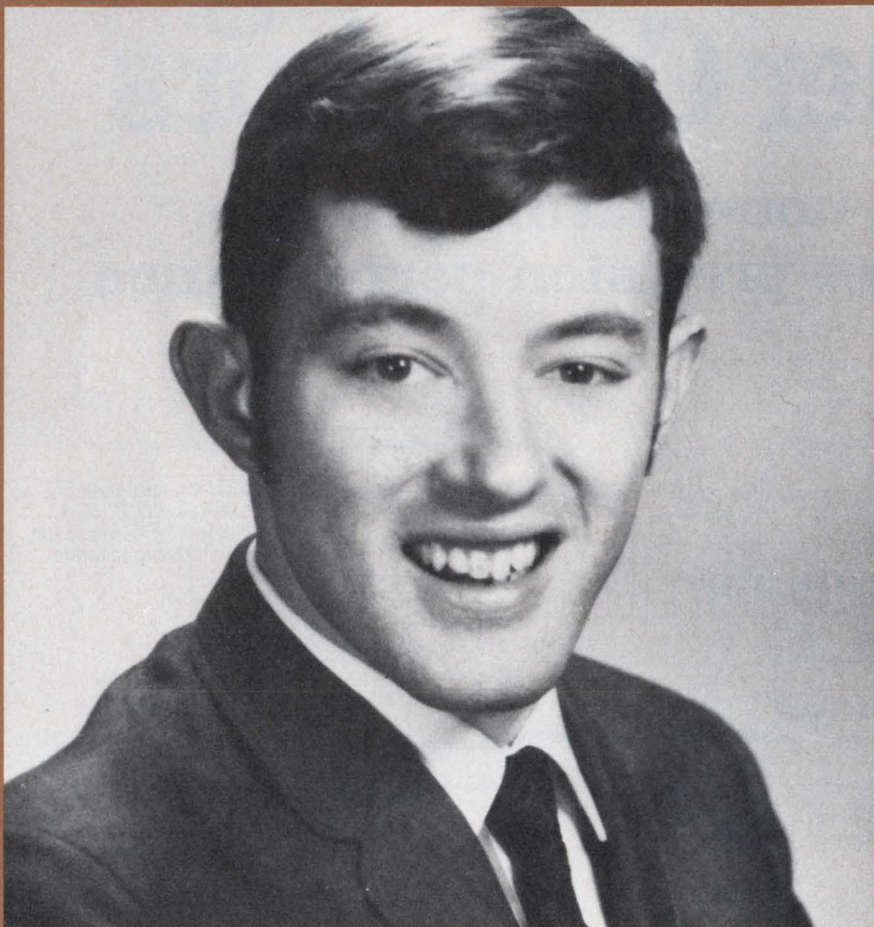

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M.A. Richards is Component Engineer at Litton G/CS, Woodland Hills, California, a leading producer of inertial navigation systems. Richards is responsible for hybrid microcircuit activity including evaluation, selection of and vendor liason. His directory? *Electronic Design's* GOLD BOOK.

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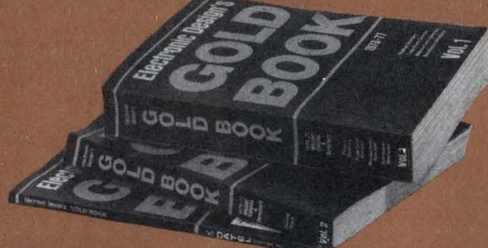

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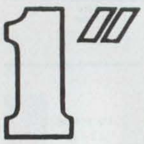

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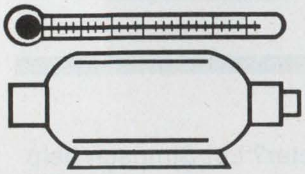

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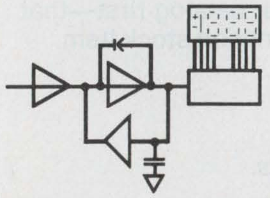
LFE series 4400 DPM's can accept optional second printed circuit board to provide for most signal conditioning conversions. Complete boards available for linearized thermocouple, RTD, AC motor speed, power line, and other special inputs.



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See LFE's complete line of process control instruments at booths 1634-1636, **Electro77**, April 19-21.

CIRCLE NUMBER 45

Editorial

The paper mountain

There's an old tale about an executive who finally realized that his staff was drowning in paper, so he stormed in one day and ordered that all files be discarded. "But first," he cautioned, "copy everything in triplicate."

There's less humor in the fact that Marks and Spencer, a powerful British chain store, saved almost a million pounds a year by slashing the amount of paper it produced. That was some years ago, when the pound was real money, worth $2.40 in American dollars—and dollars were real.

Somewhat sadder, at least for Franklin M. Jarman, was his ouster in January from the position of chief executive of Genesco because of what *Business Week* called "paperwork paralysis." What's worse, the poor fellow had his salary chopped from $285,000 to a mere $180,000.

Apparently, Jarman was a great believer in managing by computer printout—so much so that operations were often stalled by paperwork and red tape. Urgent decisions would frequently be postponed while Jarman demanded more analysis.

Jarman's love for paper, coupled with less than excessive sensitivity to people (to make a point, he once gave each of his top executives a hangman's noose), made it relatively easy for Genesco's directors to strip him of corporate power.

But why should we worry about a billion-dollar clothing and retailing conglomerate? We're in a different business and we don't run our operations by paperwork. Or do we?

Many of us, fearful of making wrong engineering or business decisions, hesitate. We busy ourselves generating paper and analyzing reports. We conceal inaction behind paper screens, the mark of modern management.

Or we shuffle data till we find support for a preconceived conclusion. Or become slaves to our own creation, the digital computer. For who can argue with decisions based on computer analysis?

Perhaps that's where it all will end. Maybe we're destined to freeze as we climb yet another mountain of paper, hoping that the next mountain will provide answers we need before we can make a decision.

George Rostky

GEORGE ROSTKY
Editor-in-Chief

Microdata introduces a matrix printer that thinks.

A built-in microprocessor makes Microdata's new matrix printer the smartest buy in the industry.

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CIRCLE NUMBER 46

The IC Tester that's in a class by itself has graduated to MPU.

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IT-200 will perform DC parametric as well as functional testing via standard factory programs. It can also use an associated MPU instruction set to perform customer specified test routines.

Test the 6800 or the 8080, just to name two of the MPU's which the IT-200 can now handle.

All this plus its original IC test versatility. The 100 kHz functional capability, coupled with a powerful DC parametric capability, allows testing of CMOS, NMOS, PMOS, ECL, and TTL devices of any complexity. The particularly powerful DC parametric test capacity provides current ranges from ±200 na to ±200 ma, and voltage ranges up to ±20V.

Check out the IT-200. You'll find the specs are truly in a class by themselves and the price is surprisingly low.

For more information on what IT-200 can do for you, write or call Cliff Small, Siemens Corporation, Measurement Systems Division, 3 Computer Drive, Cherry Hill, New Jersey 08034. (609) 424-2400.

SIEMENS

IT-200 is manufactured by Imperial Technology and marketed by Siemens.

CIRCLE NUMBER 47

Technology

SOFTWARE for Microprocessors: Part 4

Your microcomputer's I/O software may well determine its over-all performance. And in real-time applications, I/O timing often means everything.

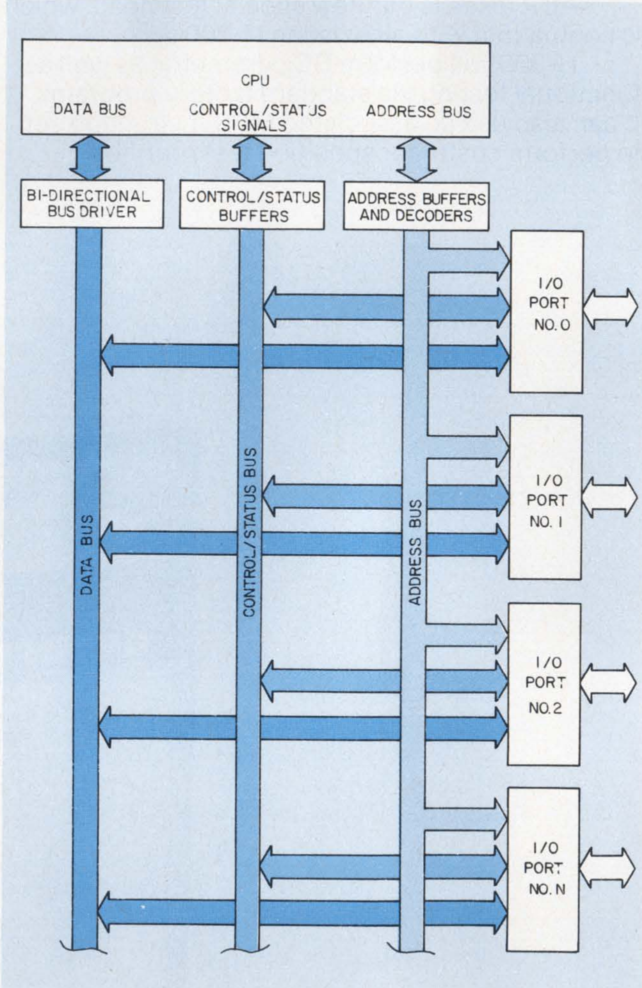
No matter how ingenious or efficient your microcomputer program, it will do you no good if you can't get the data into your machine and the answers out. That goes for a computer of any size, but input/output (I/O) is especially critical for microcomputers. Micros are most often used in real-time dedicated applications, converting inputs from sensors, keyboards, and meters of all kinds, to outputs that control machines, test equipment—even other computers.

While I/O software for general-purpose computers is contained in the operating system, for micros you usually have to write your own I/O routines as part of the applications programs. They are often the most critical part.

Your I/O routines must fit specific hardware interfaces. The hardware's job is to make a physical connection between the computer's data bus and the external data sources and destinations. Equally important, the hardware must translate electrical signal levels, synchronize signals, store data temporarily, and isolate the computer from unwanted data.

Most microcomputer systems have several I/O ports for interfacing devices such as keyboards, CRT terminals, printers, disc memories, tape units, instruments, control switches, indicator lights, and all kinds of data transducers. In a generalized I/O scheme (Fig. 1), the I/O data bus is isolated from the CPU data bus by a bidirectional bus driver. When properly addressed and enabled, any of the I/O ports may be used to route data to or from the CPU.

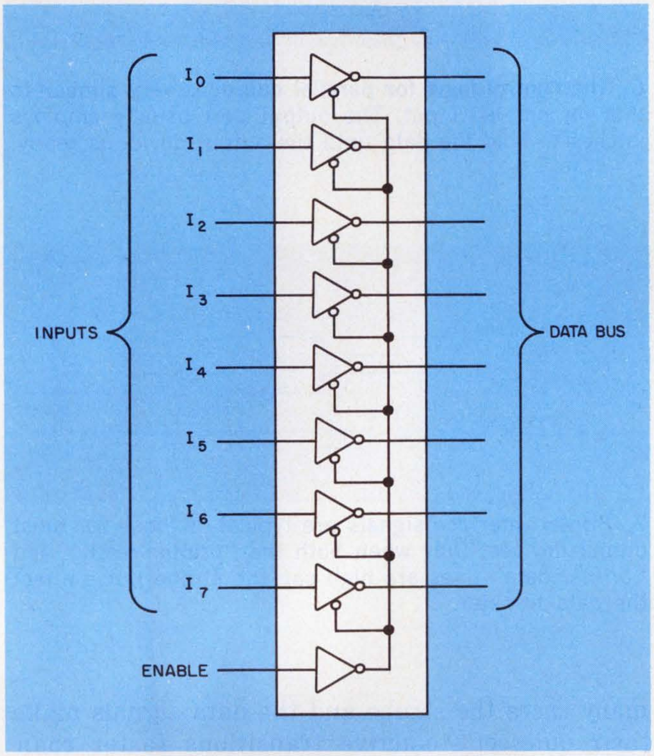
The control/status bus may be as simple as a single read/write line, or it may have several lines for "handshake," interrupt and timing functions. The complexity range of the address decoder/driver can be extreme—from a complicated multilevel decoder to nothing at all. The I/O ports themselves match the devices to be interfaced, but can usually be classed as parallel-input, parallel-output, serial-I/O, or multiple-bit discrete I/O ports.



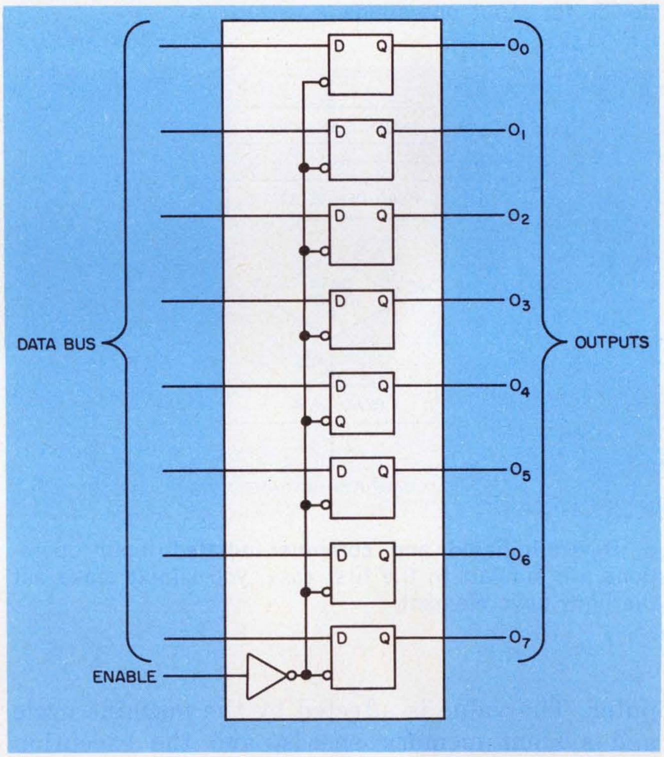
1. The generalized I/O system of a microcomputer shows how input and output ports are linked in the central processing unit. Only one of the three linkage levels (dark) actually carries data.

Fig. 2 shows a simple 8-bit input port with three-state outputs. A simple 8-bit output port (Fig. 3) uses latches to store a byte from the bus until it can be accepted by an external device. More complex parallel I/O ports often use multiplexers and addressable latches to provide multi-

Robert W. Ulrickson, President, Logical Services Inc., 711 Stierlin Rd., Mountain View, CA 94043.



2. **An 8-bit parallel-input port** is essentially a multipole switch that connects the inputs with the data bus when the "enable" pulse occurs.



3. **A simple 8-bit output port** uses latches to store data from the bus. When the output device is ready to receive, the "enable" pulse makes the connection.

ple ports and control individual bits for discrete-bit input or output.

Marching to different drummers

I/O devices seldom operate at the same speed as the computer—so synchronizing the I/O, or timing, is usually required. This can be accomplished with control signals, software timing loops, hardware, or combinations of the three.

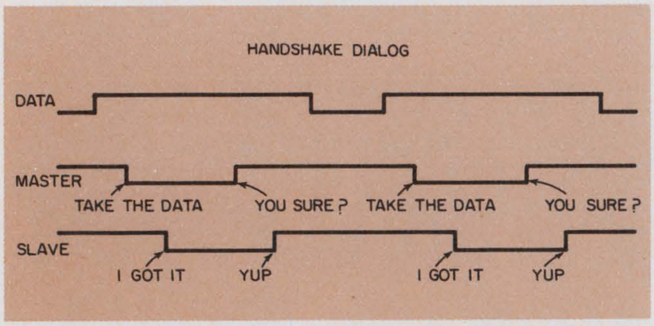
Status and control signals can direct the data transfers between the computer and the I/O device. In such I/O operations the computer waits for one or more status indicators to show that the device is ready before supplying control signals to actuate the transfer. These signals may be present in any order or combination. Some applications may require only one or the other.

Status and control signals provide a very flexible and reliable way to transfer data to and from the computer. When you are designing a computer I/O system, reserve some I/O ports for the timing and control signals that are required by your peripherals.

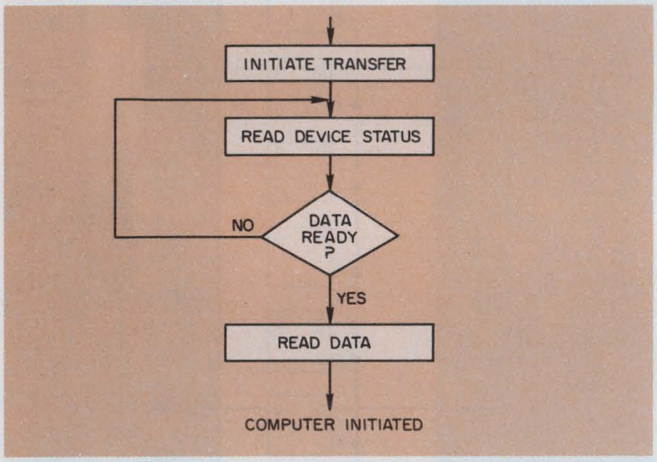
A software timing loop is a program section or subroutine that idles the computer for a fixed period of time. Such loops normally load a constant into a register and increment or decrement it until it reaches zero. The loop constant is chosen so that the loop terminates after a known period of time.

Selection of the loop timing constant depends greatly on the characteristics of your microcom-

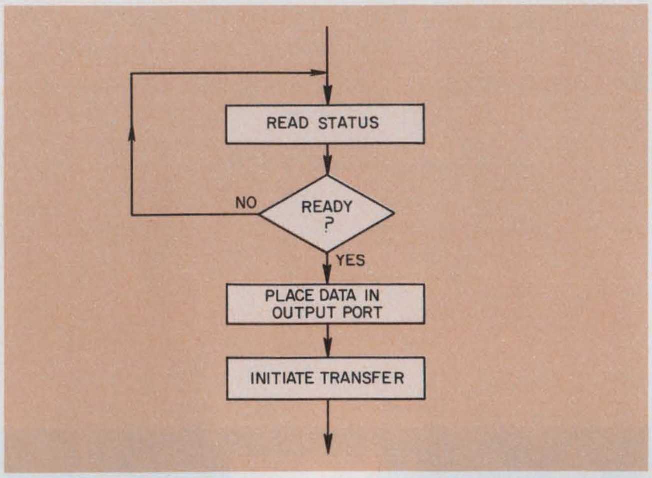
(continued on next page)



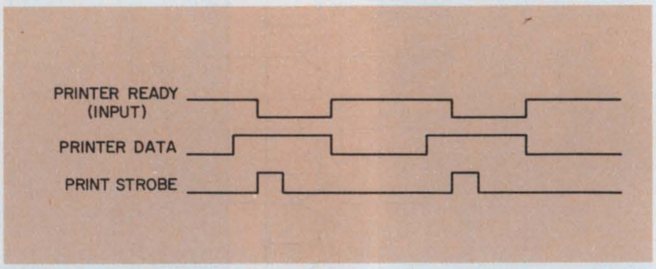
4. **The handshake dialog ensures proper signal flow** between a "master" and a "slave" device. Usually the CPU is the master for output operations, and the I/O device for input operations.



5. **Device-initiated and computer-initiated** input operations are similar. In the first case, you simply leave out the light logic element.



6. **The control logic for parallel output** is very similar to that for parallel input. The output port usually employs latches to hold the data until the output device is ready.



7. **Printer interface signals** are typical of those for most output devices. Only when both the "printer ready" and "printer data" lines are high can the strobe pulse effect the data transfer.

puter. The value is affected by the machine cycle and system memory speeds, and the execution time of the instructions in the loop.

Remember that most timing loops are only approximations, and they are not suitable for applications requiring extremely precise timing. The total delay, t_D, in a delay routine is given by the following equation:

$$t_D = N * t_L + t_p$$

where N states how often the loop executes, t_L is the execution time for the loop, and t_p is the execution time of subroutine instructions not within the loop. With a delay routine you can vary the loop constant to generate pulses or repetitive waveforms of any duty cycle and pulse width.

Is your chip fast enough?

In some applications you will find that software alone is not fast enough to detect certain peripheral status signals. For example, an ASCII-encoded keyboard often shows a strobe pulse to indicate that a parallel character is ready. In many cases the strobe and the data signals make their quiescent-to-active transitions faster than the microprocessor can detect.

If you are using a typical microprocessor (2-MHz clock, no-wait memory), you will be hard pressed to reliably detect pulses shorter than 10 μs. If the CPU is too slow to detect data, you need some additional hardware to widen the pulses. For instance, you use the short strobe pulse to trigger a monostable multivibrator. The multivibrator output can then be adjusted to a width the computer can detect, so you can then test the output of the one-shot just as you test any other pulse input. Or, you can gate the input signal into a latch and then test the latch output. Whenever it shows an active level, you know that the signal has occurred.

Slaves require handshakes

Before data can be transferred in most I/O operations, you need to make sure that the I/O device is ready. In some cases, you also want to test after the transfer, to make sure that the I/O operation has been completed before initiating the next transfer. Such transfers are handshake-controlled.

The device that initiates the I/O transfer is called the master device, the device responding to the transfer is called the slave device. In most computer applications, the central processing unit (CPU) is the master for output operations and the I/O device is the master for input operations. Handshaking requires at least two separate I/O control lines in addition to the data lines (Fig. 4).

The master device makes the data available and initiates the transfer. The slave device then reads the data and sets the signal to indicate it has been received. The master device in turn resets the "transfer" signal, after which the slave device resets the "received" signal. Finally, the master device outputs the new data and re-initiates the cycle.

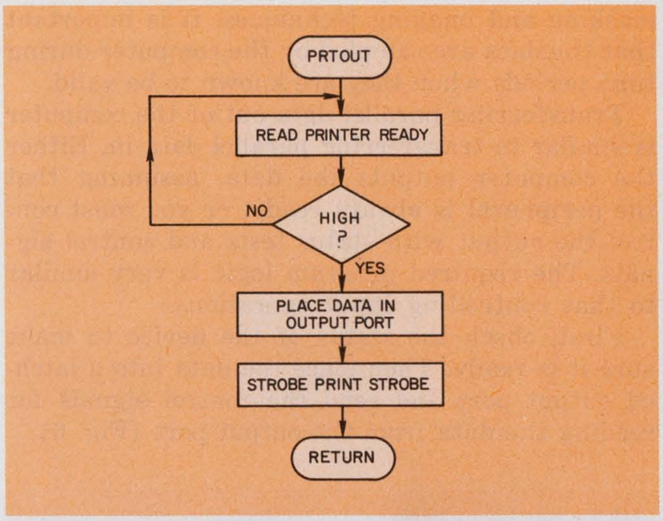
The handshake can be implemented in several ways. If the devices are fairly slow, the entire handshake can be accomplished by software. For faster devices you may need a combination of hardware and software logic.

A common variation of the basic handshake I/O: The master device outputs the control signal to the slave device as a strobe, and then reads the handshake signal as a latched input. This causes the slave to respond with a pulse after the data transfer is complete. Because it's no longer necessary for both the master and the slave to sense signal transitions, the interface becomes somewhat simpler.

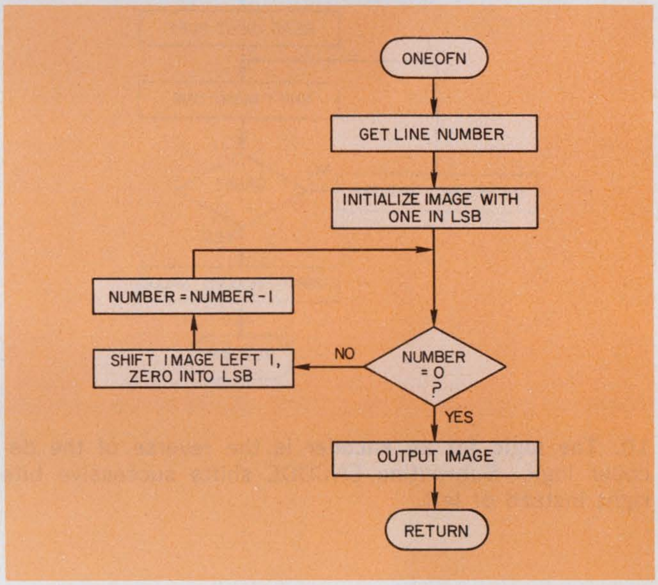
Parallel or serial?

Data transfer through an I/O port must conform to the type of port used. Parallel data move through an I/O port in a single operation. Serial data require several operations to transfer the data, one bit at a time. Parallel-data transmission is usually faster and requires less programming—therefore, less memory—whereas serial transfer requires only one bit of I/O-port hardware. Both of these methods are commonly found in microcomputer systems.

Parallel-input operations can be initiated either by the input device or the computer. In a device-initiated input operation, the computer simply waits until the data are supplied by the input device. In a computer-initiated input operation, the computer sends a strobe signal to the input device, then waits for the device to supply the data. The computer initiated operation is nearly identical to the device-initiated routine except that you need additional logic to tell the input device that a transfer is to be performed (Fig. 5).



8. **PRTOUT is a subroutine** for printer-interface logic. After the data are transferred, control is returned to the main program.



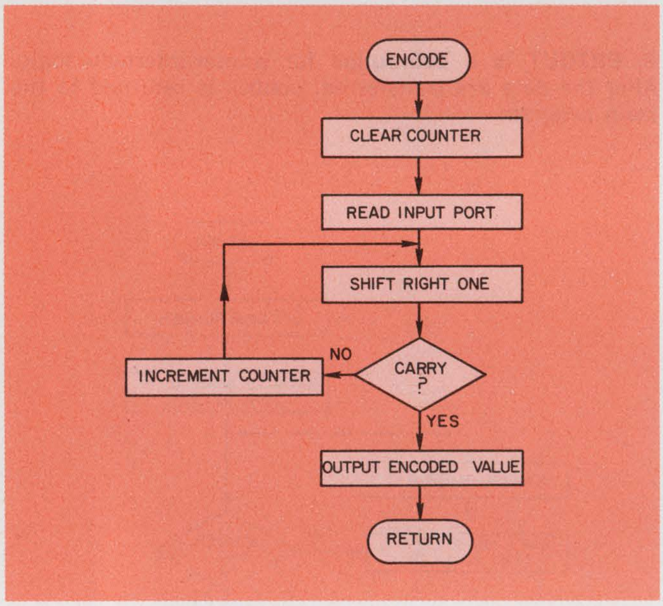
9. **The algorithm ONEOFN** illustrates operation of a "one-of-N" decoder. The number of available lines, N, is usually 8, 10, or 16.

At least two separate input ports are usually required by parallel-input operations. One input port contains the input data and the other, called a status input port, contains the signal(s) that indicate when the data are ready. Computer initiated transfers, on the other hand, require a control-output port that starts the transfer by transmitting transfer-initiation signals(s) that trigger the input device.

A single-status input port and a single-control output port can usually serve several different devices in turn. The correct bits for each device are selected from such a shared port by software masking and imaging techniques. It is important that the data are sampled by the computer during time periods when they are known to be valid.

Transferring parallel data out of the computer is similar to transferring parallel data in. Either the computer outputs the data, assuming that the peripheral is always ready, or you must control the output with status tests and control signals. The required program logic is very similar to that controlling input operations.

First, check the status of the device to make sure it is ready. Then place the data into a latched output port and send the control signals for reading the data from the output port (Fig. 6).



10. **The logic for an encoder** is the reverse of the decoder logic. Subroutine ENCODE shifts successive bits right instead of left.

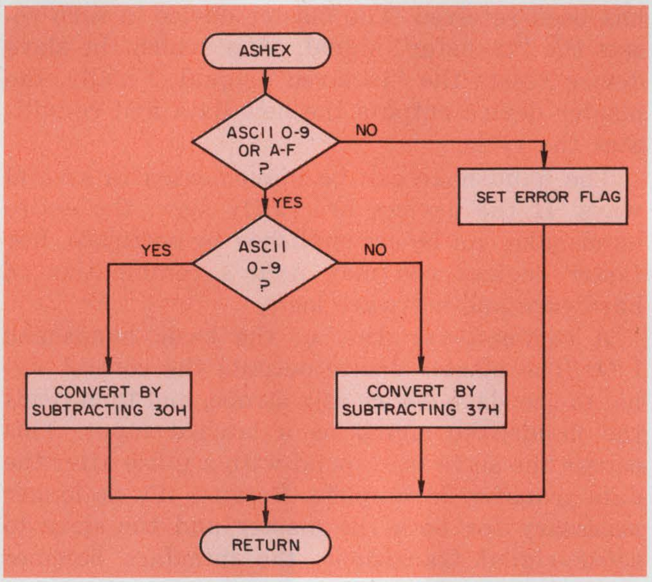
A line printer is a typical parallel-output interface and is controlled by the timing, control, and data waveforms of Fig. 7. The "printer ready" signal is HIGH whenever the printer is ready to accept data from the computer. The data are placed in the output port and the "print strobe" signal is driven HIGH. The "printer ready" line then goes LOW until the character is printed. As long as "printer ready" is LOW the character in the output port must remain stable.

The control logic for this interface (Fig. 8) shows that after the read strobe has been issued, the program exits without testing "printer ready." This happens because the printer hardware sets the "printer ready" signal LOW as soon as the strobe is received. If several characters are to be printed consecutively, you must test for "printer ready" HIGH to make sure that the previous character has been accepted before sending out new data.

What's your line?

Often microcomputers have to select one of a group of data lines. For example, you may want the system to input a number from lines 0 through 9 and activate or de-activate the device attached to the selected line. This scheme is called a one-of-N decoder, because only one of N possible lines is selected for use.

To implement this algorithm, use the input value as a loop-control variable and initialize the output image to zeroes with a "1" in the least-significant-bit position (Fig. 9). Count the loop control variation down, shifting the output image left by one bit position for each count, and put a zero in the least-significant bit. When the loop terminates, the image has a "1" in the selected bit position.

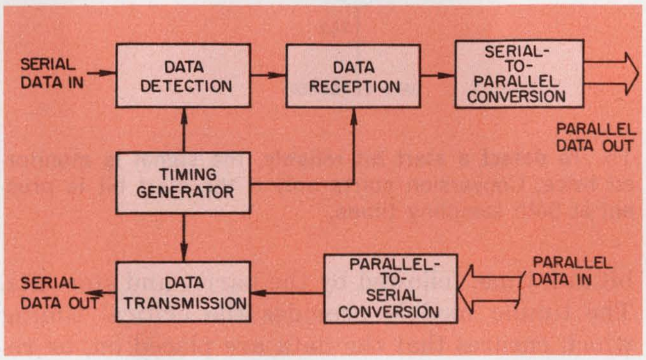


11. **Subroutine ASHEX converts ASCII code** to hexadecimal data format. Because numerals as well as letters are involved, a rather complex algorithm is necessary.

Now that you have the correct image, transfer it to the correct control-output port. The number of lines that can be decoded by the program logic shown in Fig. 9 is virtually unlimited, but the most common decoders are 1-of-8, 1-of-10, and 1-of-16. The computer requires enough output ports to provide one control line for every legitimate input value. Thus, a 1-of-16 decoder implemented on an 8-bit microcomputer requires two 8-bit output ports.

The reverse operation is performed by a parallel encoder, whose input is a single active line; the output is that line's bit position (Fig. 10). First, clear a counter in a register or memory location. Then read the input port, and enter the main loop. The loop rotates the input data one position to the right, moving the data in the least significant bit into the carry flag. Since only one bit of the input port is active, the loop exits when that bit is found.

On every pass through the loop, the counter is incremented; when the loop exits, the counter contains the encoded value. This basic logic can be expanded to a large number of input lines, but the most common encoders have 8, 10 or 16 levels.



12. **In the block diagram of a serial I/O interface,** the "data detection" box detects serial inputs, and the "data transmission" box forms output signals.

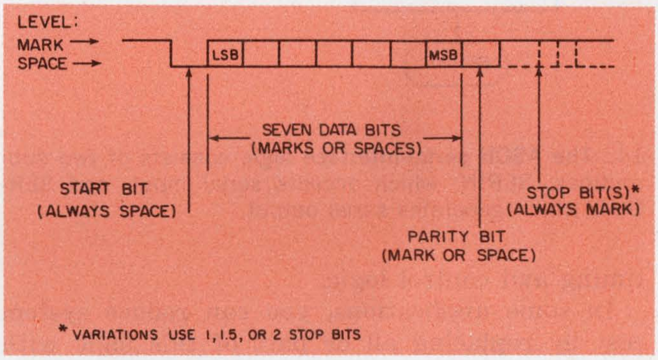
Hex your ASCII

Translating data from one form or number system into another form is a very common software operation for parallel I/O. Conversions from ASCII code to hexadecimal or BCD (and vice versa) are required to properly interface a microcomputer with a terminal or hard-copy printer device.

For an example of parallel-code conversion, consider a routine to translate parallel ASCII characters from a keyboard into hexadecimal numbers for arithmetic operations within the CPU. The input is an ASCII character code representing the hexadecimal numbers 0-9, A-F. These ASCII codes (in hexadecimal notation) are 30-39H, and 41-46H, respectively. The result of the operation will be a 4-bit hexadecimal number, 0-F.

Notice that the ASCII codes for 0-9 can be converted to their hexadecimal equivalents by merely removing the "3" in the most significant digit. This conversion can also be performed by subtracting hex 30 from the number (e.g., ASCII 0 = 30, and 30-30 = 0). The ASCII codes for A-F are each greater by 37H than their corresponding hexadecimal values. Therefore, if you subtract hex 37 from the ASCII code, the remainder should be the hex value represented by that code. For the A with an ASCII value of hex 41, you obtain 41 − 37 = 0A which is the correct value. You now have all the material needed to prepare a flow chart for this algorithm.

The test to ascertain that an ASCII character falls in the range 0-9 and A-F is more complex than the logic flow chart (Fig. 11) indicates. The ASCII character codes for 0-9 and A-F are not contiguous values. So, tests must be performed to eliminate all characters less than 30H, greater than 46H, or in the 39-40H range. Therefore implementing the general logic with assembly language will require several separate tests.



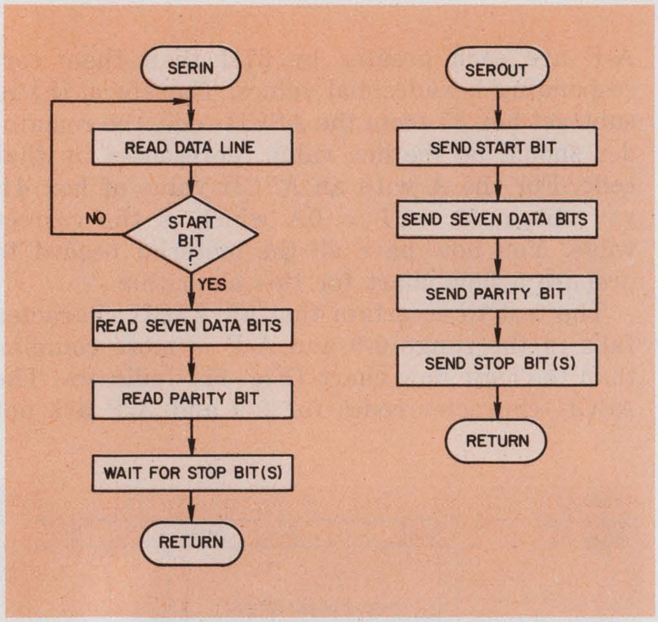
13. **In ASCII serial format,** the two logic levels are called "mark" and "space" instead of HIGH and LOW. Each character requires 10 to 11 bits.

In serial I/O, precise timing is essential

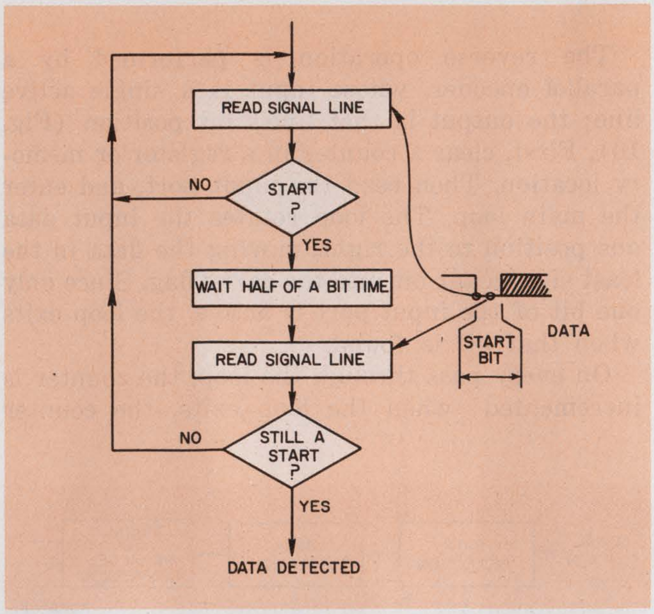
The most common type of serial I/O device is the Universal Asynchronous Receiver/Transmitter (UART), commonly used to connect teletypewriters and other data terminals to a computer. The UART looks like a parallel port to the computer, but to the terminal device it presents a standard bit-serial signal with start bits, stop bits, data bits, and parity.

Serial data are transmitted as a sequence of individual bits. Since most modern computers operate on parallel data, serial I/O operations mainly convert data from serial to parallel on input and from parallel to serial on output. Normally, serial data are input and output using multiple input and output operations on a single bit of a parallel-I/O port.

Serial I/O operations require precise timing between the sending and receiving devices. Therefore, most serial I/O is performed by dedicated hardware that incorporates the necessary



14. **The ASCII serial-interface logic** consists of two subroutines: SERIN, which accepts serial input, and SEROUT, which generates serial output.



15. **To detect a start bit reliably,** the signal is monitored twice. Conversion starts only if the start bit is present at both sampling times.

timing and control logic.

In some applications, you can reduce system cost by replacing all or part of this logic with software. When you replace the critical timing hardware by software timing loops, such "software serial I/O" encounters all the problems that plague timing loops. Not all applications can tolerate that.

Although many serial data formats are used in various systems, all of them have certain common characteristics. Serial data consist of a start bit, the actual data, and a stop bit. Because serial devices usually cannot use strobes to indicate a "data ready" condition, a start bit is sent ahead of the data to indicate to the receiving device that a data transmission is beginning. After the start bit is received, the receiving device can process the input data. Several bits follow the transmitted data with error-detection information to verify the data's validity, as well as stop bits(s) that set up the receiver to listen for the next data transmission.

In a general block diagram for a serial I/O system (Fig. 12), the data-detection block monitors the signal line and determines when a valid start bit has occurred. Then it sends the serial data stream to the serial-to-parallel block which outputs the parallel data. After receiving the stop bit, the data-detection block listens for a new start bit, which indicates the start of the next data transmission.

The output section of Fig. 12 works in reverse. After the parallel-to-serial conversion block receives a character, the data transmission block generates the start bit. The characters are then converted from parallel to serial and sent out one bit at a time, followed by the parity and stop bits. The timing module provides the critical timing which ensures that the data are placed on, or received from, the data line at the correct rate. When data bytes are sent and received at the same rate, the timing module is shared by the send and receive modules. If different data rates are required, both modules have separate timing generators.

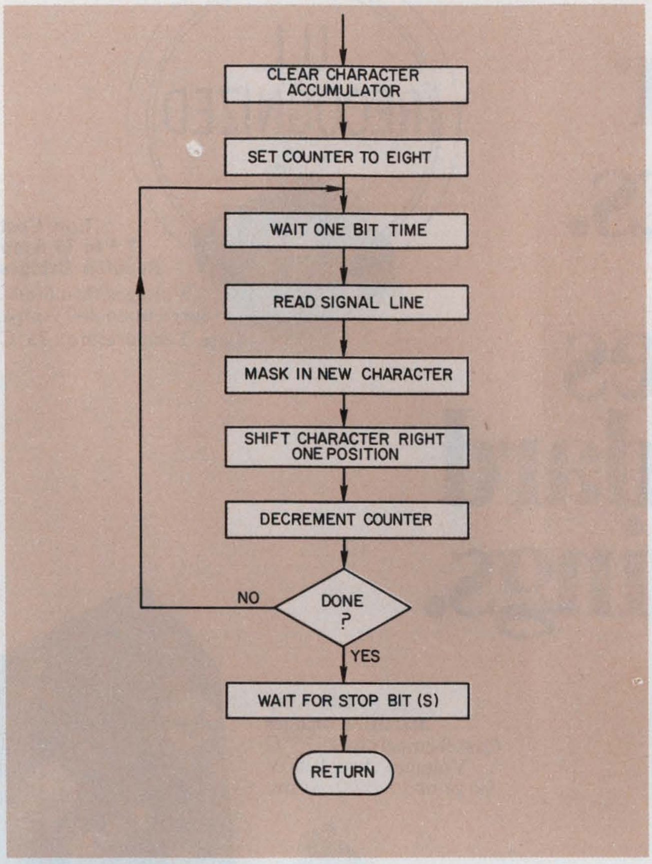
The ASCII format exemplifies a serial-data transmission system because it is the most common of all serial data formats (Fig. 13). Each character consists of 11 data bits. The data line idles in the "mark" state.

The start bit is always in the "space" state, and the stop bit(s) always in the "mark" state. The data proper starts with the least significant bit and takes up seven slots. Parity bit and stop bit(s) complete the transmission of an ASCII character. The flow chart for an ASCII serial interface (Fig. 14) summarizes the receiving and transmitting sequence.

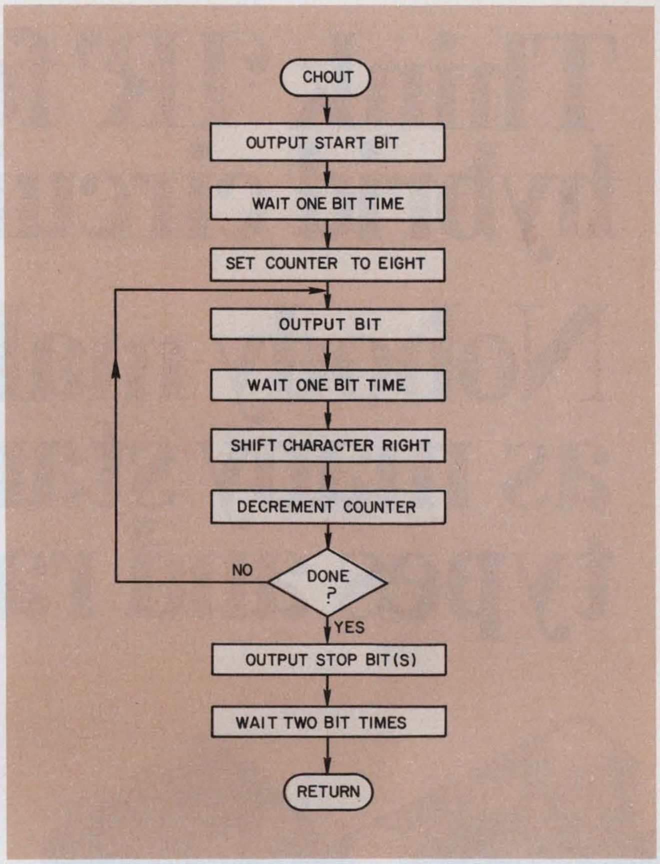
Beware of false starts

A serial ASCII data transmission begins with the start bit. The highest speed normally used with this character format is 960 characters/s. At this speed, the individual data bits are sent at a rate of approximately one bit every 100 μs. If you simply search for the presence of the transition from "mark" to "space," you will detect the leading edge of the transition and you need very exact timing to ensure that the data bits are read at the right moment.

But external factors can produce noise or other-



16. **Converting a serial character to hex** requires that the data bits be assembled in the proper sequence. The least significant bit arrives first.



17. **The serial-character-output algorithm CHOUT** looks much like the serial/hex conversion logic, but is easier to implement.

wise trick your computer into accepting a false start. So, a double-test method is more reliable. After the transition is detected, insert a delay equal to one-half the start-bit time, then test again. If at that time the signal doesn't show a start bit, ignore the false start and resume monitoring. If the start bit is still there, you can be fairly sure of a valid start (Fig. 15). If subsequently you wait one full bit time, you will sample the center of each data bit. The conversion thus becomes much less susceptible to small variations in data frequency.

ASCII data arrive with the least significant bit first. If you input and save the incoming bits the right way, the input operation and serial-to-parallel conversion can be accomplished at the same time. Simply shift the partially accumulated character right circularly, and mask-in the new bit. After eight circular shifts, the character is assembled in the correct order. Having waited for the appropriate stop bit(s) to ensure data synchronization, transfer the converted character to the main program (Fig. 16).

Serial-data output is usually easier to realize than serial-data input because generating the start and stop bits is easier than detecting them. In the case of serial-ASCII characters, simply output the proper levels to the data port for fixed periods of time. After the start bit is transmitted, the character is shifted out one bit at a time, followed by the stop bit (Fig. 17).

The standard rates for data interchange in the serial ASCII data format are 10, 15, 30, 120, 240, 480, and 960 characters per second. These rates are often expressed as the number of bits/s, or baud rates. For the characters with seven data bits per character, standard rates are 110, 150, 300, 1200, 2400, 4800, and 9600 baud. You can adapt the general-purpose serial I/O routines to any of these rates by adjusting the loop timing for the critical timing loops. Solving the delay equation for N, you obtain this equation:

$$N = \frac{t_d - t_p}{t_L}$$

where t_L and t_p are the actual execution times of the machine code in your application. The result, N, is the loop variable for the required delay.

Remember that serial data transfers are highly time sensitive. So you must pay close attention to time delays both in the hardware and the software.

The program-initiated I/O operations described so far merely scratch the surface of I/O software. Others yet to be discussed include I/O software for interrupts, real time I/O, scanned I/O, and block data transfers. ■■

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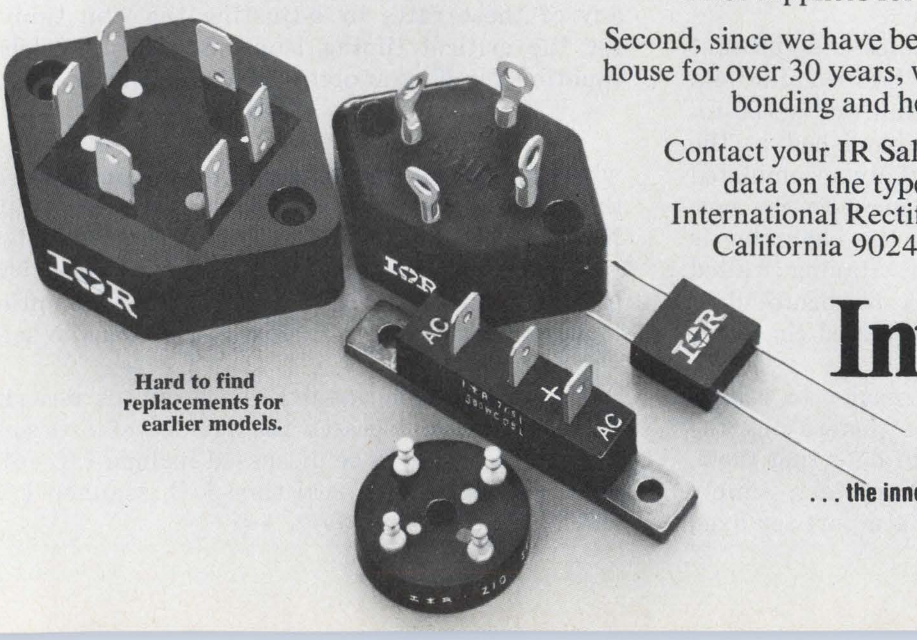

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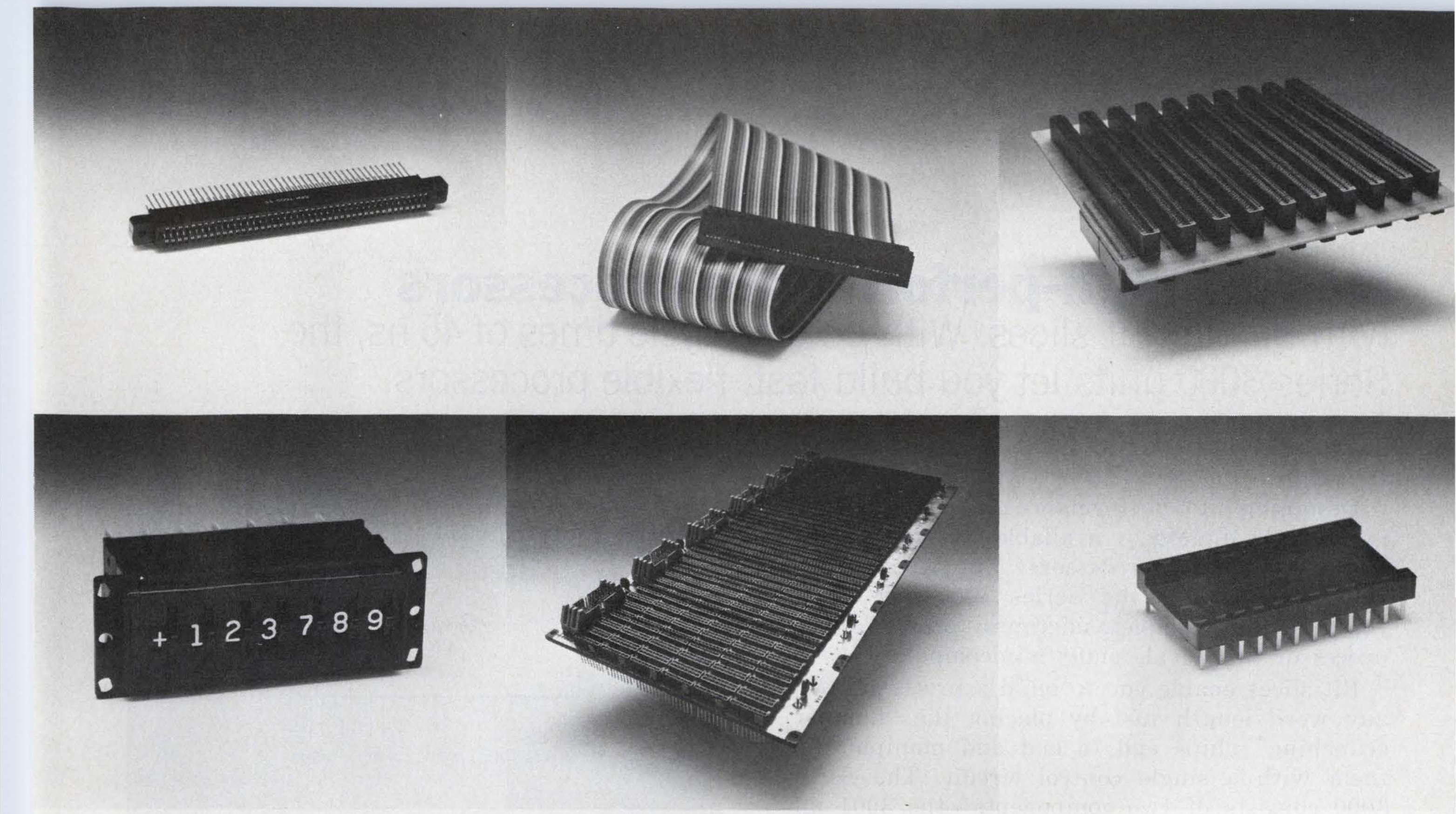

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CIRCLE NUMBER 49

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Designing high-performance processing systems is normally limited by available single-chip MOS and bipolar microprocessors. But with bipolar LSI elements like the Series 3000 bit slices,* you can build a complete microprogrammed digital processor that rivals many minicomputers.

Bit slices enable you to build a processor with any word length just by placing the "number-crunching" chips end to end and manipulating them with a single control circuit. The Series 3000 consists of two components—the 3001 microcontrol sequencer and the 3002 arithmetic and logic unit (ALU) processor (Fig. 1)—and is supported by virtually all TTL circuits (some directly related circuits are shown in Table 1). And since both the 3001 and 3002 have typical microcycle times of only 45 ns, rapid computations are possible.

The current level of integration possible with bipolar-Schottky technology has precluded the development of full submicrosecond microprocessors (8-bits and larger) on a single chip. However, by partitioning the processor system into three major blocks (Fig. 2) high-performance bipolar LSI circuits can be fabricated:

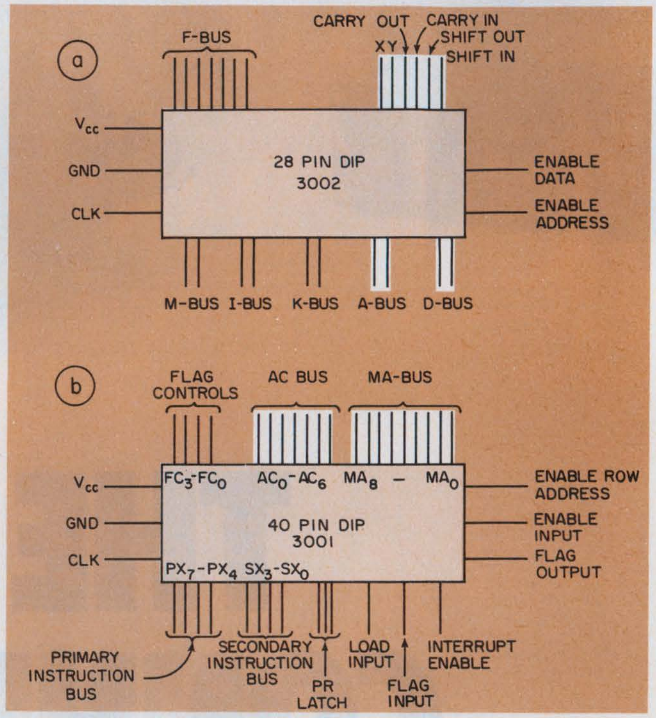
1. The processing section, containing the ALU, some general-purpose registers, an accumulator, special-purpose registers and status flags. This section provides all data-transfer paths, manipulates data in the ALU, generates status flags and provides some storage files.

2. The control section, consisting of a macroinstruction decode circuit, a control store, a test-branch decode circuit and microprogram-sequencing logic. This block initiates memory and I/O operations, decodes macroinstructions, controls the manipulation and transfer of data, tests status conditions and responds to interrupts.

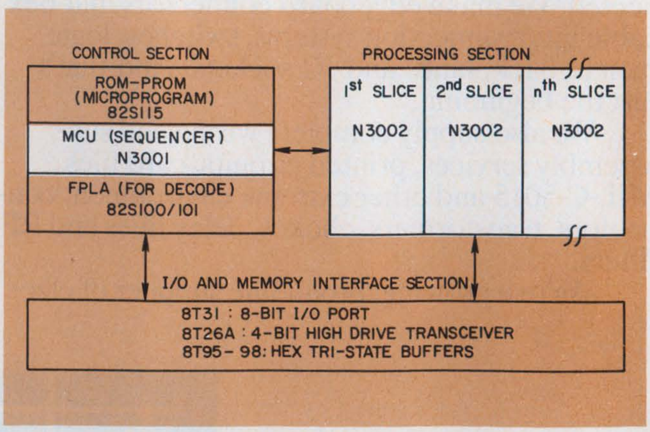
3. The I/O and memory-interface section, containing mainly I/O ports, high-power bus driver/

*For more on bit slices, see "A Primer on Bit-Slice Processors" by Dr. John Nemec, Gordon Sim and Brian Willis, Electronic Design, Feb. 1, 1977, p. 52.

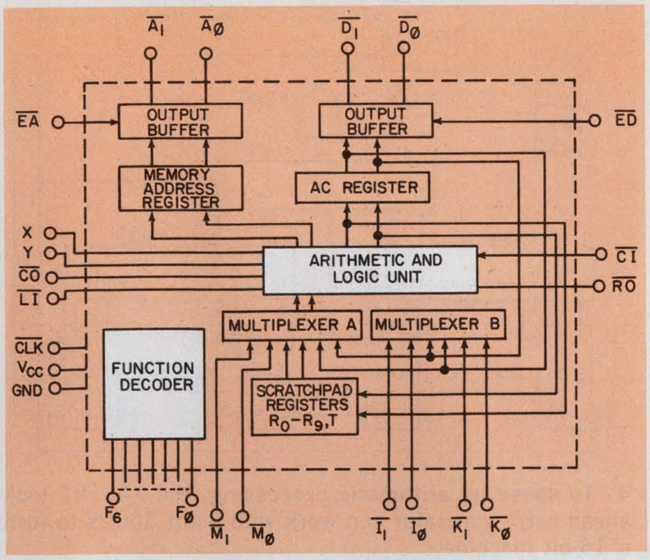
Stephen Y. Lau, Manager, Bipolar MPU Development and Support, Signetics, 811 E. Arques Ave., Sunnyvale, CA 94086.



1. **Capable of being cascaded to any desired word length,** the 3002 two-bit processor (a) comes housed in a 28-pin DIP. Its controller, the 3001 (b), can handle as many 3002s as are needed for a particular application (up to its unbuffered loading capability of 10).



2. **To build a complete central processor,** you only have to interconnect three major blocks—a controller, a processor and an I/O and interface section. All these blocks, though, consist of many subsystems.



3. **Basic to the CPE is the arithmetic and logic unit** that, under control of the F bus, can perform over 40 Boolean and logic operations.

receivers and some temporary storage facilities. This block multiplexes data to the proper destination, provides bus interfacing and usually has temporary data latches for storage.

Build outward from the processor

Since all data manipulations are handled by the processor section, start the over-all processor design by taking a close look at the 3002 Central Processing Element (CPE). The CPE represents a complete 2-bit slice of a computer's data-processing section. The 3002 contains 11 general-purpose registers (R_0 to R_9 and a T register), one accumulator (AC), one memory-address register (MAR), one multifunction ALU and three-state address and data bus buffers (Fig. 3).

Each 3002 has five independent two-line buses and one seven-line microfunction input bus (F bus). Functions for each of the two-line buses are defined as follows:

1. Input M bus—transfers data from external memory.
2. Input I bus—transfers data from the I/O device.
3. Input K bus—functions as a microprogrammed mask.
4. Output A bus—acts as a memory-address bus and is fed by the MAR.
5. Output D bus—functions as a data bus and is fed by the AC.

The F bus accepts microprogram words and controls the internal operation of the CPE by selecting both the operands and the operation they will perform. As you can see from the list of commands given in Table 2, over 40 Boolean and binary operations are possible with the ALU built into the 3002.

Table 1. Series 3000 hardware

Circuit function	Part number	100-up prices
Bit-slice processor	N3002	$11.70 ceramic 7.65 plastic
Microprogram controller	N3001	22.50
PROM 4 k, (512 × 8)	82S115	15.50
PROM 8-k (1 k × 8) bipolar	82S180/181	34.40
PROM 8-k (1 k × 8) UV erasable	82S2708	*
PROM, 16 k, (2 k × 8)	82S190/191	*
Field programmable gate array	82S102/103	7.00
Field-programmable logic array	82S100/101	16.00
Bus buffers and transceivers	Entire 8T family, but specially: 8T26 8T28 8T31 8T32 8T95 8T96	 2.40 2.40 3.00 3.00 1.25 1.25
Parity generator	74180	1.35
Carry look-ahead generator	74182	1.00

*To be announced

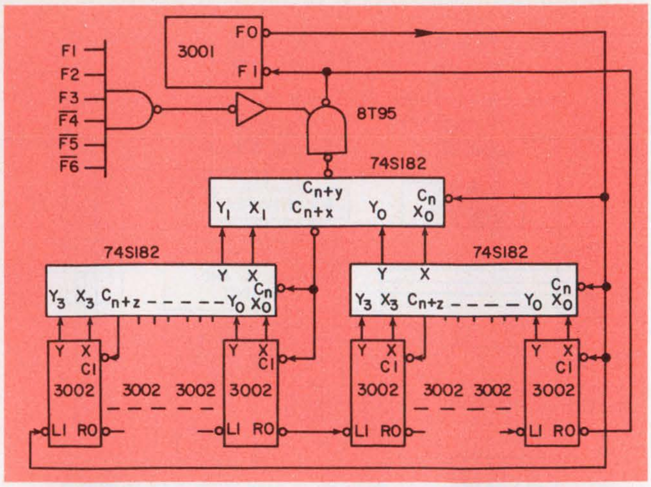
A 28-pin dual in-line package houses the CPE. Besides the seven F bus lines and the 10 lines for the five smaller buses, two lines are used for carry-propagate and carry-generate outputs (X and Y lines), one line is needed for the clock-timing input and two more for power-supply hook up. Of the six remaining lines, four provide additional control of the ALU and the other two enable or disable the three-state A and D buses.

The various I/O buses can be put to good use. For example, output buses A and D are often used to present address and data to the main memory during the same microcycle. This capability is a significant advantage over available 4-bit processors, which require two microcycles plus an extra address register to do the same job.

Another example that "flexes" the CPE's capabilities is a byte-swap operation, which connects the lowest eight bits of the D bus to the highest eight bits of the M bus and the highest eight bits of the D bus to the lowest eight bits of the M bus. The byte-swap operation requires just one microcycle on the 3002, but can require as many as four microcycles for other bit slices.

By employing inputs to the K bus as masks or constants, the CPE offers yet another advantage over other slices: Most of them require that the mask or constant be loaded into an internal register—which requires an additional microcycle. But with its output bus, the CPE's dedicated MAR permits simultaneous operations—such as presenting an address on the address bus and data on the data bus to the main memory—without external hardware or an extra microcycle.

Several of the 3002 CPEs can be cascaded to form a processor of any word length by paralleling all the control signals and cascading the X and Y lines so that carries and borrows will proceed normally. Even readily available circuits such as the 74S182 look-ahead carry generator can speed up the addition process (Fig. 4).



4. **To speed up arithmetic processing,** the 74S182 look-ahead carry generator can work with eight 3002s to form a 16-bit machine.

Manipulate the CPE with the controller

To generate all the control signals necessary to manipulate the processor formed from cascaded CPEs, the 3001 Microprogram Control Unit (MCU) keeps track of the sequence in which microinstructions are accessed. Microinstructions are, of course, the codes stored in ROM, PROM or RAM that determine the operations performed by the CPE and any other support circuits. Inside the MCU (Fig. 5) is an address-control section that provides a 9-bit output to address up to 512 words of control program. For additional addressing capability, you can use external registers, controlled by the MCU.

In addition to the 9-bit address output, the MCU has a 4-bit program latch, 2 flag registers, 11 jump commands, 8 flag-control commands and buffers on all output lines for three-state operation. Simple decoding is possible with a two-dimensional addressing scheme for the microprogram memory which separates the nine address lines into MA_0 to MA_3 for columns and MA_4 to MA_8 for rows. The microprogram memory can be expanded if necessary by adding a page-control flip-flop (Fig. 6).

Control of the MCU is exercised by microinstructions applied to the AC_6 to AC_0 lines and the FC_3 to FC_0 lines. These two control buses define a group of jump/test functions that create the next microinstruction address. Table 3 outlines how and what each of the jump/test functions performs, while Table 4 describes the eight flag-control capabilities of the 3001. The next address logic permits the MCU to unconditionally jump anywhere within a particular row or column but not anywhere within the 16 × 32 matrix. For any location contained in the matrix, the next address can be selected from a fixed subset of microprogram addresses.

Lines FC_0 to FC_3 enable the MCU to save the carry output of the CPE and control the carry input to it. Two flags, called the C flag and the Z flag, and a simple latch called the F latch indicate the current state of the CPE array's carry-output line. Combined with the carry and shift logic of the CPE, the MCU's flag logic can perform shift/rotate and arithmetic functions.

There are two special instruction buses on the MCU: the primary instruction bus, PX_7 to PX_4, and the secondary instruction bus, SX_3 to SX_0. The primary bus holds data that are tested by a JPX instruction to determine the next microprogram address. Secondary bus data are loaded into a four-bit PR latch and when PX-bus data are being tested, simultaneously appear at inputs to the next-address logic section. During a subsequent cycle, the contents of the PR latch may be tested by the JPR, JLL or JRL commands (see Table 3) to determine the next microprogram address. Information held in the PR latch can determine any of 16 possible branch addresses, while the latch outputs, PR_2 to PR_0, help to either modify microinstructions at the outputs of the microprogram memory or provide additional control lines.

Loading information into the MCU is controlled by the load (LD) line. If the line is active-high at the rising edge of the clock, the data on the PX and SX buses are loaded into the microprogram-address register and the M_8 bit is set to 0. Since the interrupt-strobe enable of the MCU permits priority-interrupt control circuits to override the selected next-row address from the MCU, the MCU is forced to a new address.

Control the controller with memory

The microprogram memory addressed by lines MA_0 to MA_8 can be formed from many of the commonly available RAMs, ROMs or PROMs that have cycle times of 50 ns and longer. A circuit like the 82S115, a 512-word × 8-bit bipolar fusible-link PROM, will fit the bill. The 82S115 even has on-chip output latches that can be used as a

Table 2. CPE instruction set

Mnemonic	F bus bits 654	3210	...3210	K-bus	Functions
Logical operations					
ANR	100	0000 1100	→1001 →1101	All 1	AND AC with register and test result for zero.
ANM	100	1010 1011		All 1	AND M bus with AC and test result for zero.
ANI	100	1110 1111		All 1	AND I bus with AC (ORT) and test result for zero.
TZR	101	0000 1100	→1001 →1101	All 1	Test register for zero.
	101	0000 1100	→1001 →1101	K	Mask register with K bus.
LTM	101	1010 1011		All 1	Load M-bus in AT and test for zero.
	101	1010 1011		K	Mask and test result for zero.
TZA	101	1110 1111		All 1	Test register for zero.
	101	1110 1111		K	Mask and test result for zero.
ORR	110	0000 1100	→1001 →1101	All 1	OR AC to register; and test previous AC value for zero.
*ORM	110	1010 1011		All 1	OR M-bus to AC and test previous AC value for zero.
ORI	110	1110 1111		All 1	OR I-bus to AT and test I-bus data for zero.
**XNR	111	0000 1100	→1001 →1101	All 1	Exclusive-NOR AC with R_n; force CO to 1 if ($R_n \wedge$ AC) is non-zero.
XNM	111	1110 1011		All 1	Exclusive-NOR M-bus with AC; force CO to 1 if (M $\wedge$ AC) is non-zero.
XNI	111	1110 1111		All 1	Exclusive-NOR I-bus with AC or T register; force CO to 1 if (AT $\wedge$ I) is non-zero.
Control operations					
DSM	001	0000 1100	→1001 →1101	All 1	Set MAR to all one's. Decrement R_n conditionally.
LDM	001	1010 1011		All 1	Set MAR to all one's. Load conditionally decremented M-bus in AC or T register.
CLR	100	0000 1100	→1001 →1101	All 0	Clear register and force CO to CI.
CLA	100	1010 1011		All 0	Clear AC or T and force CO to CI.
NOP	110	0000 1100	→1001 →1101	All 0	Null operation and force CO to CI.
CSR	010	0000 1100	→1001 →1101	All 0	Conditionally clear or set R_n to all 0's or l's, respectively.
CSA	010	1010 1011		All 0	Conditionally clear or set AC or T register to all 0's or 1's, respectively.
Shift operations					
SRA	000	1110 1111		All 0	Shift or rotate right one bit.
ALR	000	0000 1100	→1001 →1101	All 1	If (R_n) = (AC), the operation is equivalent to shift left by one bit.
Move operations					
LMI	001	0000 1100	→1001 →1101	All 0	Move R_n to MAR, conditionally increment R_n. Can be used to maintain program counter.
LMM	001	1010 1011		All 0	Move M-bus data to MAR; increment M-bus by 1.
SDA	010	1010 1011		All 1	If CI is true, move AC to AC or T register.
LDI	010	1110 1111		All 1	If CI is true, move I-bus data to AC or T register.
ACM	011	1010 1011		All 0	If CI is false, move M-bus data to AC or T register.
LTM	101	1010 1011		All 1	Move M-bus to AC or T register and test for zero.
LMF	110	1010 1011		All 0	Move M-bus to AC or T register; force CO to CI
CMR	111	0000 1100	→1001 →1101	All 0	Complement R_n; force CO to CI.
LCM	111	1010 1011		All 0	Load AC or T register with complemented M-bus; force CO to CI.
CMA	111	1110 1111		All 0	Complement AC or T register; force CO to CI.
Arithmetic operations					
ILR	000	0000 1100	→1001 →1101	All 0	Load AC from R_n or to increment R_n and load result in R_n, AC.
ALR	000	0000 1100	→1001 →1101	All 1	Add AC to R_n or R_n + 1.
ACM	000	1010 1011		All 0	Load or increment M-bus to AC or T register.
AMA	000	1010 1011		All 1	Add M-bus or the incremented M-bus to AC (may be used for indexing).
LMI	001	0000 1100	→1001 →1101	All 0	Load MAR with R_n; or increment R_n. Used to update and maintain program counter.
DSM	001	0000 1100	→1001 →1101	All 1	Force MAR to all 1's. Conditionally decrement R_n.
LMM	001	1010 1011		All 0	Load MAR with M-bus; add 1 to M-bus with result stored in AC or T register used for indirect addressing.
LDM	001	1110 1111		All 1	Force MAR to all 1's. Load M-bus or decremented M-bus to AC or T register.
CIA	001	1110 1111		All 0	Add CI to complemented value of AT. Used to obtain 1's or 2's complement of AC or T register.
DCA	001	1110 1111		All 1	Decrement AT by 1 conditionally.
SDR	010	0000 1100	→1001 →1101	All 1	Conditionally decrement or transfer AC to R_n.
SDA	010	1010 1011		All 1	Conditionally decrement AC by 1, or transfer AC to AC or T register.
LDI	010	1110 1111		All 1	Conditionally decrement I-bus by 1 or transfer I-bus to AC or T register.
INR	011	0000 1100	→1001 →1101	All 0	Conditionally increment R_n by 1 or transfer R_n to R_n.
ADR	011	1010 1011		All 1	Add AC to R_n if CI is false. Sum + 1 if CI is true.
INA	011	1110 1111		All 0	Conditionally increment AC or T register by 1.
AIA	011	1110 1111		All 1	Add I-bus to AC or T register if CI is false; sum + 1 if CI is true.

Symbol	Meaning
I, K, M	Data on the I, K, and M buses, respectively
CI, LI	Data on the carry input and left input, respectively
CO, RO	Data on the carry output and right output, respectively
R_n	Contents of register n including T and AC (R-Group I)
AC	Contents of the accumulator
AT	Contents of AC or T, as specified
MAR	Contents of the memory address register
L, H	As subscripts, designate low and high order bit, respectively
+	2's complement addition
−	2's complement subtraction
$\wedge$	Logic AND

microinstruction register. With this extra register, pipelined operations can be performed with very little extra hardware.

Even programmable logic arrays can be used as MCU microprogram storage or decoder elements. A unit such as the 82S100/101 FPLA can be used to decode macroinstructions by classes. These arrays offer up to 48 product terms (AND terms) and eight product function outputs. Each output can be programmed for either true active-high or true active-low; the true state of the output functions is controlled by an OR matrix.

For buffering data and instructions while they move around with a system, multiple-bit transceiver circuits, such as the 8T31, 32 and 33, provide buffering and on-board storage latches for up to eight bits of data. Many other devices offer two, four or six I/O buffers in single DIPs. Commonly used circuits include the 8T26A and 8T28 4-bit, three-state transceivers and the 8T95 to 8T98 6-bit, three-state buffers.

Developing the microprogram code to be stored in the control memory is usually the most difficult part of the entire bit-slice processor design. First, let's establish two basic definitions: A microinstruction is the smallest instruction the MCU-CPE combination can perform. A macroinstruction represents a sequence of microinstructions that will be performed when the macroinstruction is requested.

Basically, the microinstruction (microword) consists of a number of control fields that handle the following functions:

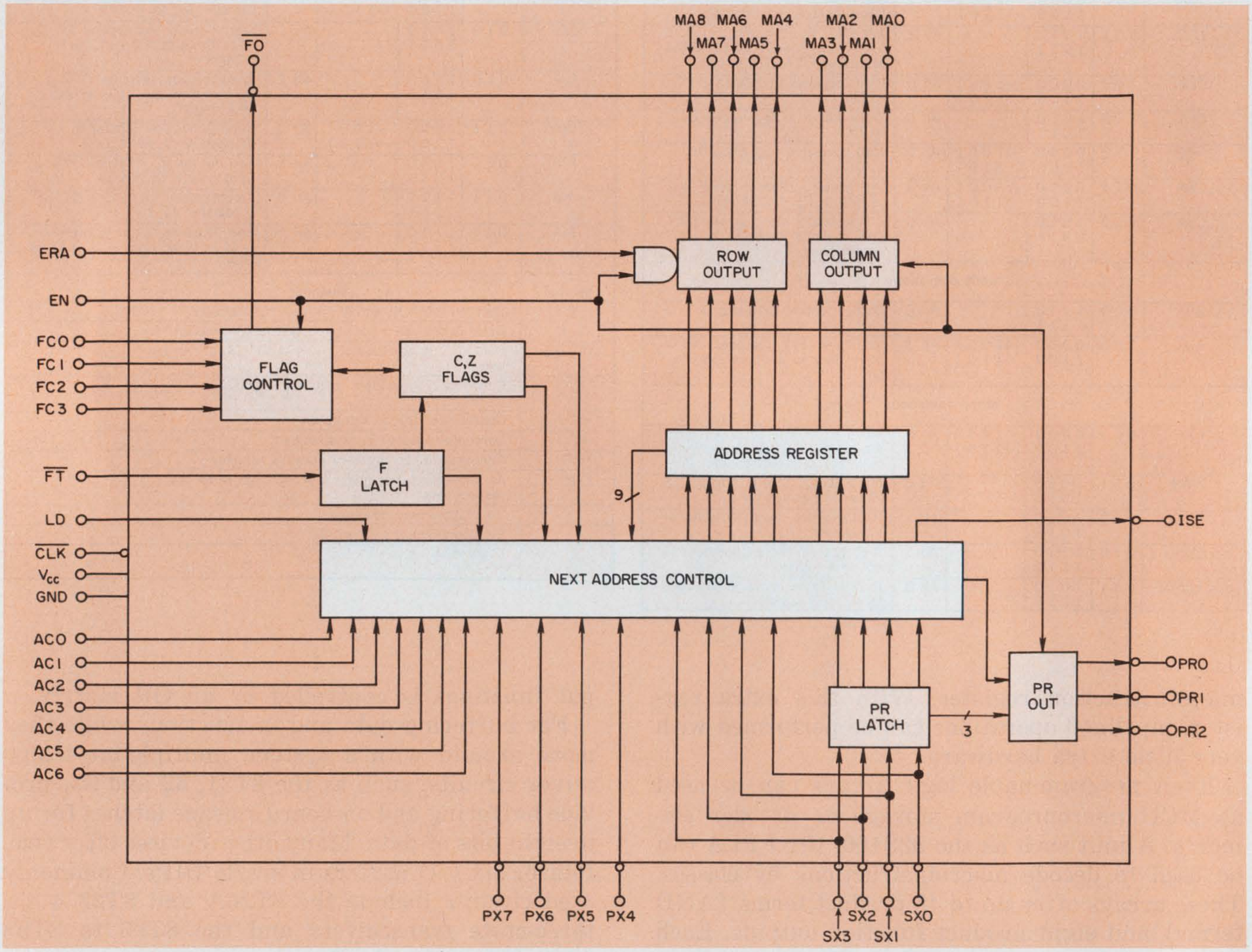
1. Initiate main-memory operations.
2. Initiate I/O operations.
3. Decode instructions.
4. Control data transfers.
5. Test machine status.
6. Respond to processing interrupts.
7. Sequence addresses.

After all possible and necessary control functions are defined, the microword can be structured. For example, look at the structuring of a 32-bit microword in Fig. 7a. Split into many small groups of bits (called fields), the word can do many jobs at the same time.

Often user-defined macroinstructions are employed to call forth a sequence of microwords. Basically however, a macroinstruction is set up in a manner similar to a microinstruction. A typical 16-bit macroinstruction can be broken into five basic fields (Fig. 7b). To start with, the word might consist of two 2-bit, address-mode control bits, two bits for the source operand (AMS) and two for the destination operand (AMD). Two 3-bit fields can define the source register (RS) and the destination register (RD), which are then used in conjunction with the AMS and AMD fields to define where the source operand (data) is and where to put it (address). The other six bits are used for an operation code that defines the desired functions.

Define the controller macroinstructions

For an example of a macroinstruction, consider the command, Move Word. If AMS is set so that the source operand (the word to be moved) is in the location specified by RS, and AMD is set so that the destination address is formed by add-



5. **Able to address up to 512 words of any length,** the 3001 microprogram controller provides its companion 3002 processor with flexible control. The address register splits the 512 words into 32 rows × 16 columns.

Table 3. MCU jump commands

Mnemonic Definition	Description and diagrammatic explanation
JCC Jump in current column	AC_0 to AC_4 are used to select 1 of 32 row address in the current column, specified by MA_0 to MA_3, as the next address.

Function	Next row	Next column
AC_6 5 4 3 2 1 0	MA_8 7 6 5 4	MA_3 2 1 0
0 0 d_4 d_3 d_2 d_1 d_0	d_4 d_3 d_2 d_1 d_0	m_3 m_2 m_1 m_0

Mnemonic Definition	Description and diagrammatic explanation
JZR Jump to zero row	AC_0 to AC_3 are used to select 1 of 16 column address in row 0, as the next address. *See Note.

Function	Next row	Next column
AC_6 5 4 3 2 1 0	MA_8 7 6 5 4	MA_3 2 1 0
0 1 0 d_3 d_2 d_1 d_0	0 0 0 0 0	d_3 d_2 d_1 d_0

Mnemonic Definition	Description and diagrammatic explanation
JCR Jump in current row	AC_0 to AC_3 are used to select 1 of 16 addresses in the current row, specified by MA_4 to MA_8, as the next address.

Function	Next row	Next column
AC_6 5 4 3 2 1 0	MA_8 7 6 5 4	MA_3 2 1 0
0 1 1 d_3 d_2 d_1 d_0	m_8 m_7 m_6 m_5 m_4	d_3 d_2 d_1 d_0

Mnemonic Definition	Description and diagrammatic explanation
JCE Jump in current column/row group and enable PR-latch outputs	AC_0 to AC_2 are used to select 1 of 8 row addresses in the current row group, specified by MA_7 and MA_8 as the next row address. The current column is specified by MA_0 to MA_3. The PR-latch outputs are asynchronously enabled.

Function	Next row	Next column
AC_6 5 4 3 2 1 0	MA_8 7 6 5 4	MA_3 2 1 0
1 1 1 0 d_2 d_1 d_0	m_8 m_7 d_2 d_1 d_0	m_3 m_2 m_1 m_0

Mnemonic Definition	Description and diagrammatic explanation
JPR Jump/test PR-latch	AC_0 to AC_2 are used to select 1 of 8 row addresses in the current row group, specified by MA_7 and MA_8, as the next row address. The four PR-latch bits are used to select 1 of 16 possible column addresses as the next column address.

Function	Next row	Next column
AC_6 5 4 3 2 1 0	MA_8 7 6 5 4	MA_3 2 1 0
1 1 0 0 d_2 d_1 d_0	m_8 m_7 d_2 d_1 d_0	p_3 p_2 | p_1 p_0

Mnemonic Definition	Description and diagrammatic explanation
JLL Jump/test left-most PR-latch bits	AC_0 to AC_2 are used to select 1 of 8 row addresses in the current row group, specified by MA_7 and MA_8, as the next row address. PR_2 and PR_3 are used to select 1 of 4 possible column addresses in col_4 to col_7 as the next column address.

Function	Next row	Next column
AC_6 5 4 3 2 1 0	MA_8 7 6 5 4	MA_3 2 1 0
1 1 0 1 d_2 d_1 d_0	m_8 m_7 d_2 d_1 d_0	0 1 p_3 p_2

Mnemonic Definition	Description and diagrammatic explanation
JRL Jump/test right-most PR-latch bits	AC_0 and AC_1 are used to select 1 of 4 high-order row addresses in the current row group, specified by MA_7 and MA_8, as the next row address. PR_0 and PR_1 are used to select 1 of 4 possible column addresses in col_{12} to col_{15} as the next column address.

Function	Next row	Next column
AC_6 5 4 3 2 1 0	MA_8 7 6 5 4	MA_3 2 1 0
1 1 1 1 1 d_1 d_0	m_8 m_7 1 d_1 d_0	1 1 p_1 p_0

Mnemonic Definition	Description and diagrammatic explanation
JPX Jump/test PX-bus and load PR-latch	AC_0 and AC_1 are used to select 1 of 4 row addresses in the current row group, specified by MA_6 to MA_8, as the next row address. PX_4 to PX_7 are used to select 1 of 16 possible column addresses as the next column address. SX_0 to SX_3 data is locked in the PR-latch at the rising edge of the clock.

Function	Next row	Next column
AC_6 5 4 3 2 1 0	MA_8 7 6 5 4	MA_3 2 1 0
1 1 1 1 0 d_1 d_0	m_8 m_7 m_6 d_1 d_0	x_7 x_6 x_5 x_4

Mnemonic Definition	Description and diagrammatic explanation
JFL Jump/test F-latch	AC_0 to AC_3 are used to select 1 of 16 row addresses in the current row group, specified by MA_8, as the next row address. If the current column group, specified by MA_3, is col_0 to col_7, the F-latch is used to select col_2 or col_3 as the next column address. If MA_3 specifies column group col_8 to col_{15}, the F-latch is used to select col_{10} or col_{11} as the next column address.

Function	Next row	Next column
AC_6 5 4 3 2 1 0	MA_8 7 6 5 4	MA_3 2 1 0
1 0 0 d_3 d_2 d_1 d_0	m_8 d_3 d_2 d_1 d_0	m_3 0 1 f

Mnemonic Definition	Description and diagrammatic explanation
JCF Jump/test C-flag	AC_0 to AC_2 are used to select 1 of 8 row addresses in the current row group, specified by MA_7 and MA_8, as the next row address. If the current column group specified by MA_8 is col_0 to col_7, the C-flag is used to select col_2 or col_3 as the next column address. If MA_3 specifies column group col_8 to col_{15}, C-flag is used to select col_{10} or col_{11} as the next column address.

Function	Next row	Next column
AC_6 5 4 3 2 1 0	MA_8 7 6 5 4	MA_3 2 1 0
1 0 1 0 d_2 d_1 d_0	m_8 m_7 d_2 d_1 d_0	m_3 0 1 c

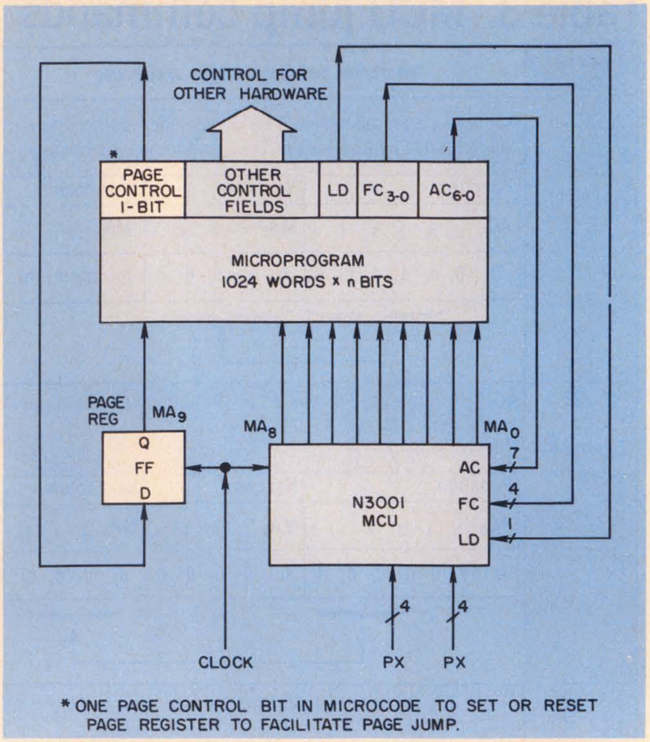
Mnemonic Definition	Description and diagrammatic explanation
JZF Jump/test Z-flag	Identical to the JCF functions, except that the Z-flag, rather than the C-flag, is used to select the next column address.

Function	Next row	Next column
AC_6 5 4 3 2 1 0	MA_8 7 6 5 4	MA_3 2 1 0
1 0 1 1 d_2 d_1 d_0	m_8 m_7 d_2 d_1 d_0	m_3 0 1 z

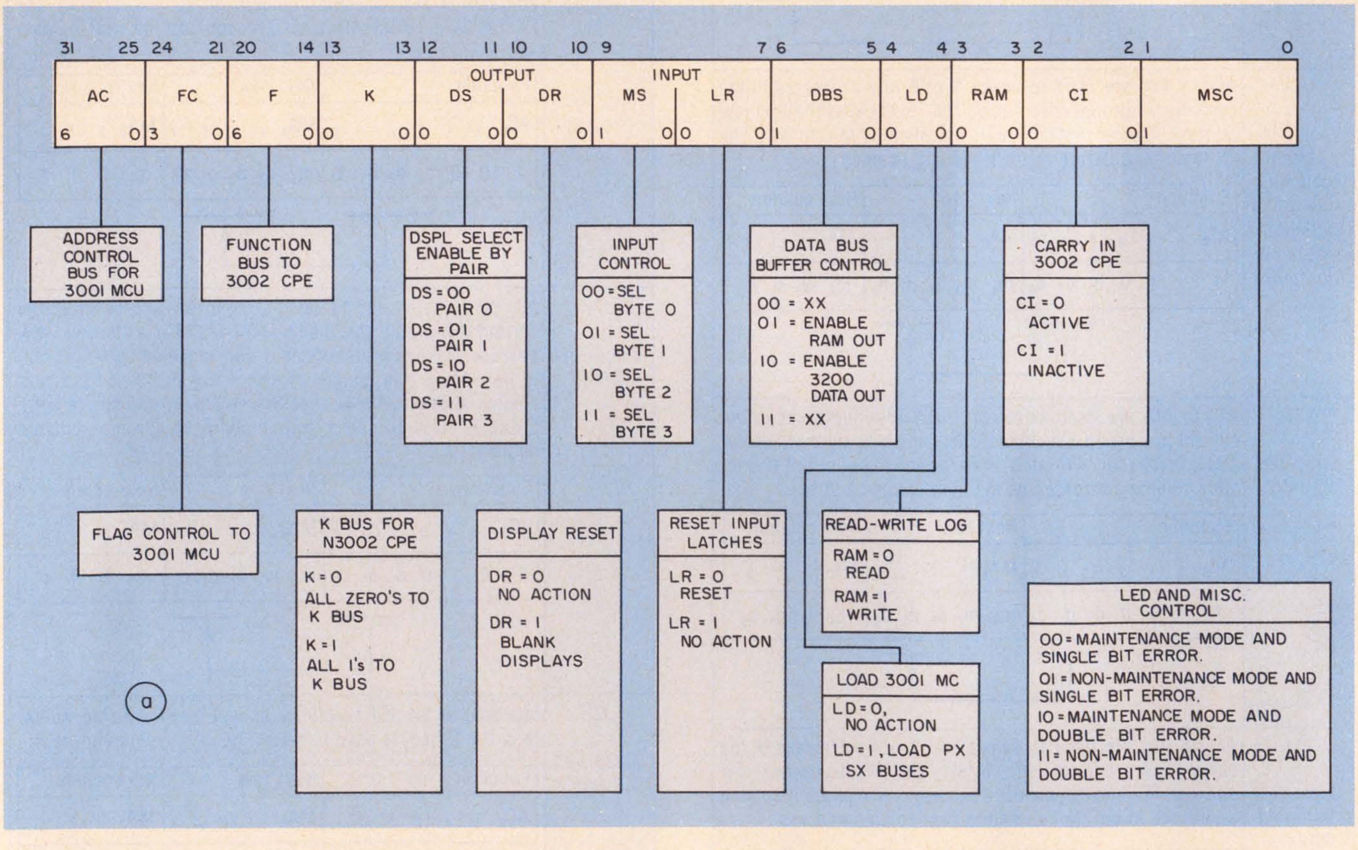
Note: When $d_3\ d_2\ d_1\ d_0 = 1111$, the ISE signal will be active. This signal can be used to communicate with the interrupt priority logic or some other type of logic.

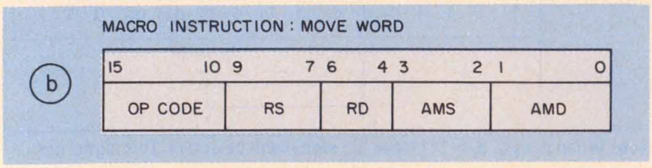
Table 4. Flag controls for MCU

Flag output control functions (C, Z)			
Mnemonic	FC_3	FC_2	Function description
FFO	0	0	Force FO to 0. FO is forced to the value of logic 0.
FFC	0	1	Force FO to C. FO is forced to the value of the C-flag.
FFZ	1	0	Force FO to Z. FO is forced to the value of the Z-flag.
FF1	1	1	Force FO to 1. FO is forced to the value of logic 1.
Flag input control functions (C, Z)			
Mnemonic	FC_1	FC_0	Function Description
SCZ	0	0	Set C-flag and Z-flag to F1. The C-flag and the Z-flag are both set to the value of F1.
STZ	0	1	Set Z-flag to F1. The Z-flag is set to the value of F1. The C-flag is unaffected.
STC	1	0	Set C-flag to F1. The C-flag is set to the value of F1. The Z-flag is unaffected.
HCZ	1	1	Hold C-flag and Z-flag. The value in the C-flag and Z-flag are unaffected.

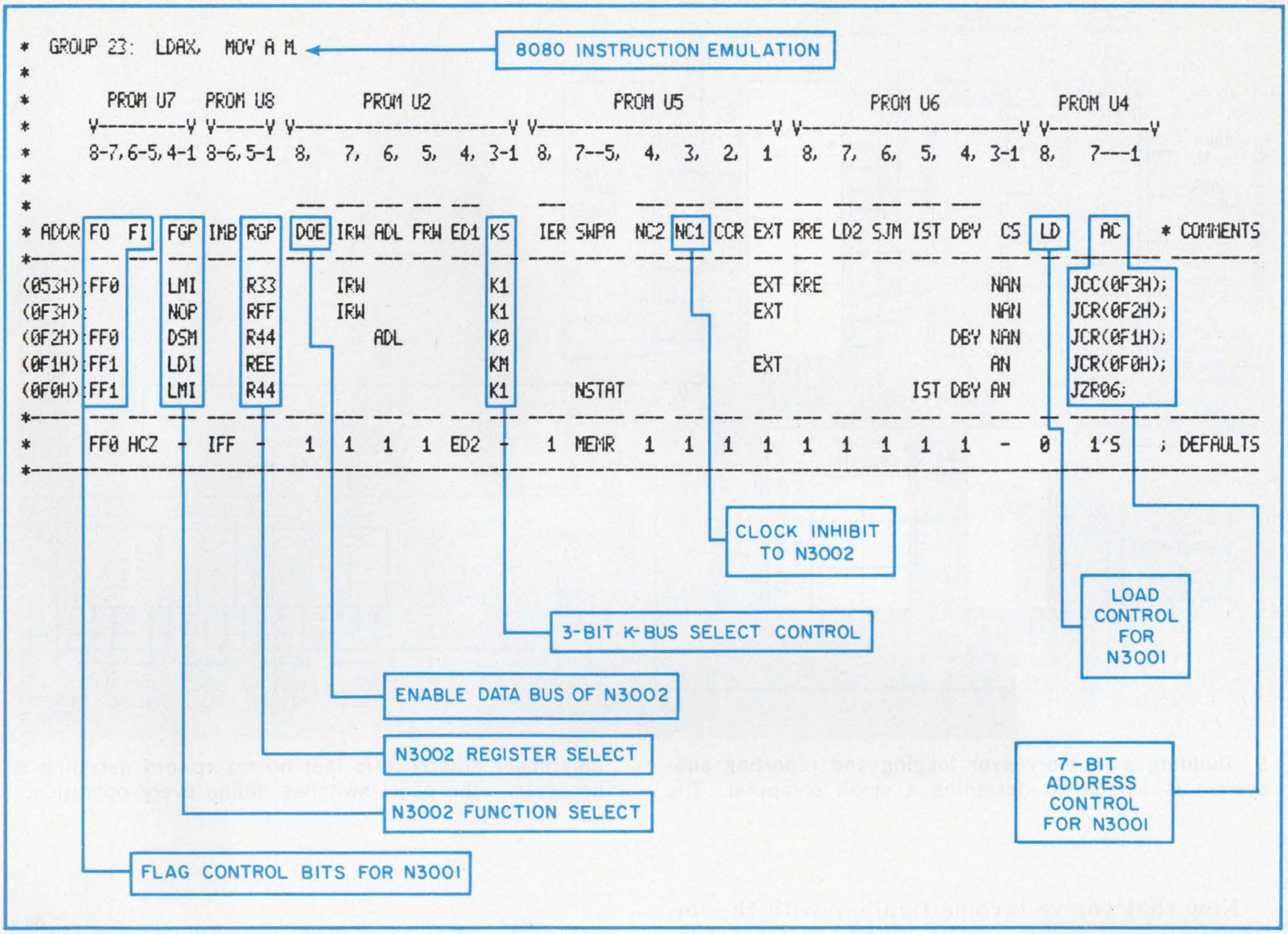


6. **If more than 512 words of microprogram memory are needed,** the address bus of the 3001 can be expanded by adding an extra flip-flop for paging.





7. **By making the microword as long as necessary,** every control function you will ever want can be given its own field (a). A macroinstruction word can also be divided into fields (b), which must be decoded further into microinstructions.



8. **Using a high-level Micro Assembler** to turn mnemonic microword listings into executable code can cut the time required to develop and assemble microcode. Available on time-sharing, the Micro Assembler developed by Signetics handles mnemonics, symbols and delimiters to simplify microcode generation.

ing the register contents specified by RD to the controller's base address, the sequence of operations performed by microinstructions (the microprogram) goes like this:

1. Fetch macroinstruction and update program counter.
2. Decode macroinstruction into classes with PLA or ROM.
3. Form destination address.
4. Form source operand address.
5. Execute transfer.
6. Allow for interrupts at end of execution.

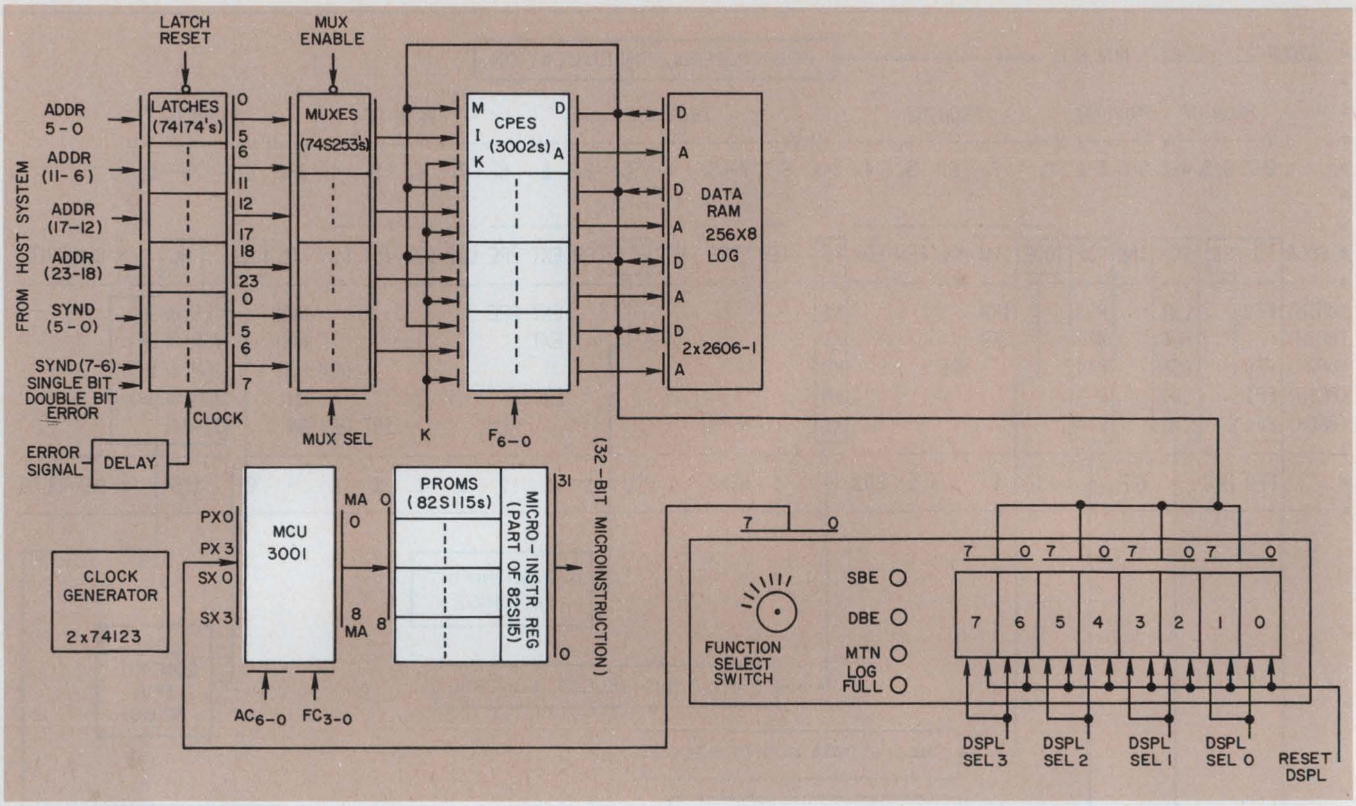
In the mnemonics of the Series 3000 processors, the sequence of operations goes as follows:

1. AC=JCC; FC=HCZ, FFI; F=LMI
2. AC=JPX; FC=HCZ, FF0; F=ACM
3. PC→ACCUM, PC; AC=JRC; FC=HCZ, FF0; F = ILR
4. RD+ACCUM→RD, ACCUM; AC=JPR; FC=HCZ; FF0; F=ALR
5. RS→ACCUM; AC=JCR; FC=HCZ, FF0; F=JLR
6. AC=JZR; FC=HCZ, FF0; F=LMI

Of course, writing such programs requires that you carefully structure exactly what you want the machine to do. But some program development aids will help you prepare microprograms for the Series 3000 processors. A Micro Assembler program from Signetics can translate a microprogram written in symbolic assembly language into executable binary form. Thus, microprogram commands can be expressed with mnemonics, symbols and delimiters (Fig. 8).

The Micro Assembler helps you keep track of all branch points by automatically assigning a physical address for each symbolic label. After the microprogram is assembled, it can be loaded directly into the appropriate PROMs or RAMs for execution. The Micro Assembler is available either on NCSS time-sharing networks or in purchasable form.

When debugging an assembled program, you can often employ a ROM simulator to temporarily hold the program. A ROM simulator is basically a read/write memory configured to appear just like a particular type of ROM or PROM. However, unlike ROMs or PROMs, you can alter specific bits in the ROM simulator's memory.



9. **Building a memory-error logging and reporting subsystem** is similar to designing a small computer. The only major difference is that no macroword decoding is necessary—the panel switches define every operation.

Now that you've become familiar with the important aspects of the Series 3000 bit slices, let's step through a short design example of an 8-bit intelligent controller called a memory-error logging and reporting subsystem (MELRS). Look for the following attributes in the MELRS:

1. The subsystem is totally independent of its host system, a machine such as an IBM 370/168.

2. The MELRS logs single-bit and/or double-bit errors, and has a capacity for logging up to 51 errors that can be associated with 51 specific addresses of the host system. Each error may be monitored for occurrence up to 256 times at the scanning rate of the MELRS. The syndrome bits (or parity bits) associated with each error can also be logged. Logging proceeds until all log space is occupied; an indicator lights when it is full.

3. All error status reports in the log are displayed on hexadecimal displays. The error count can be used to judge the seriousness of a particular memory error.

4. The MELRS has two reporting modes: (a) single-step, in which errors are reported one at a time, and (b) auto-step, in which error data are displayed every 0.5 s with internally programmed delay routines. Once all errors have been shown, the display can be terminated by deactivating the execute switch.

5. A feature is included to stop the MELRS each time an error is detected and displayed. No logging will take place, and a manual reset will restart the MELRS.

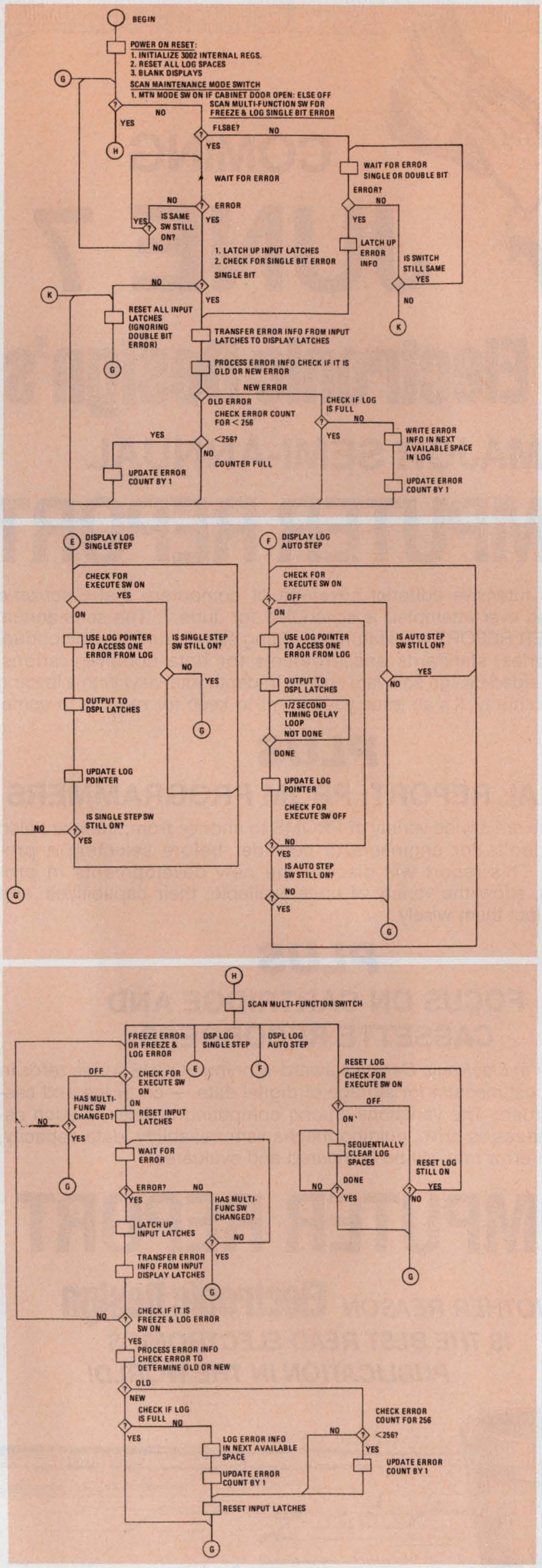
6. Another mode not only permits an error to be detected and displayed, but also logged into the next available space if it is a new error. If an error is already logged, its associated count is updated.

7. A log-reset control clears all log memory, including all 3002 CPE registers.

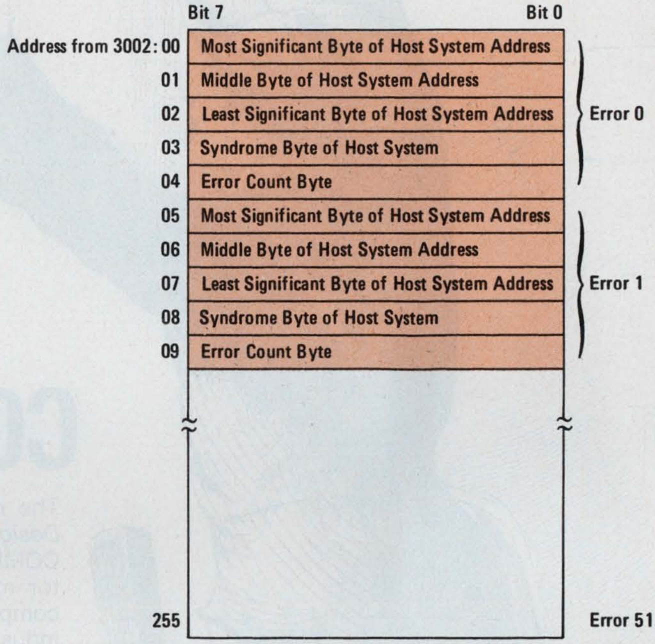
Basically, the MELRS subsystem resembles a simple computer, as shown in Fig. 9. The design,

	Bit 7 ... Bit 0
R_0	Most Significant Byte of Host System Address
R_1	Middle Byte of Host System Address
R_2	Least Significant Byte of Host System Address
R_3	Syndrome Byte of Host System
R_4	Error Count Byte
R_5	For Miscellaneous Storage
R_6	Data RAM Pointer (Log Pointer)
R_7	Data RAM Address Counter (Log Addr Counter)
R_8	Mask of All 0's.
R_9	Mask of All 1's.
T	Working Register

10. **Jobs must be assigned to each of the 3002's 11 internal registers,** because there are many pieces of data to be stored.



11. **Flow-charting the machine's operation** before the program is written is a must. Since there are many decision points, the MELRS flow chart gets to be very complex.



12. **The random-access memory needed to hold the log data** must be grouped into blocks of five bytes for each error file. Three bytes are needed for the system address, one for the parity and one for the error-count.

however, differs from a typical computer structure in that it has no macroinstruction set to execute. Instead, the subsystem responds to commands from the activated front-panel switches that load instructions directly into the 3001.

The processing section consists of four 3002 slices cascaded to form 8-bit data and address paths. Internal registers in the 3002 are assigned different functions, as defined in Fig. 10. A single 3001 stores and decodes the function-select commands. The control program is stored in four PROMs to provide a 512-word × 32-bit memory, whose format is similar to the control word shown in Fig. 7a. A flow chart describing the entire machine's operation is shown in Fig. 11.

All commands come from the front panel and all inputs of loggable data (addresses, parity bits, and so on) come from the host system. An error signal generated by the host system indicates when information on the address and data buses should be latched and subsequently processed.

The log consists of two 2606-1 RAMs, connected to look like 256 words × 8 bits and organized as shown in Fig. 12. Five bytes of storage space are reserved for each error: three bytes for the host system address, one byte for the parity bits and one for the error count. ■■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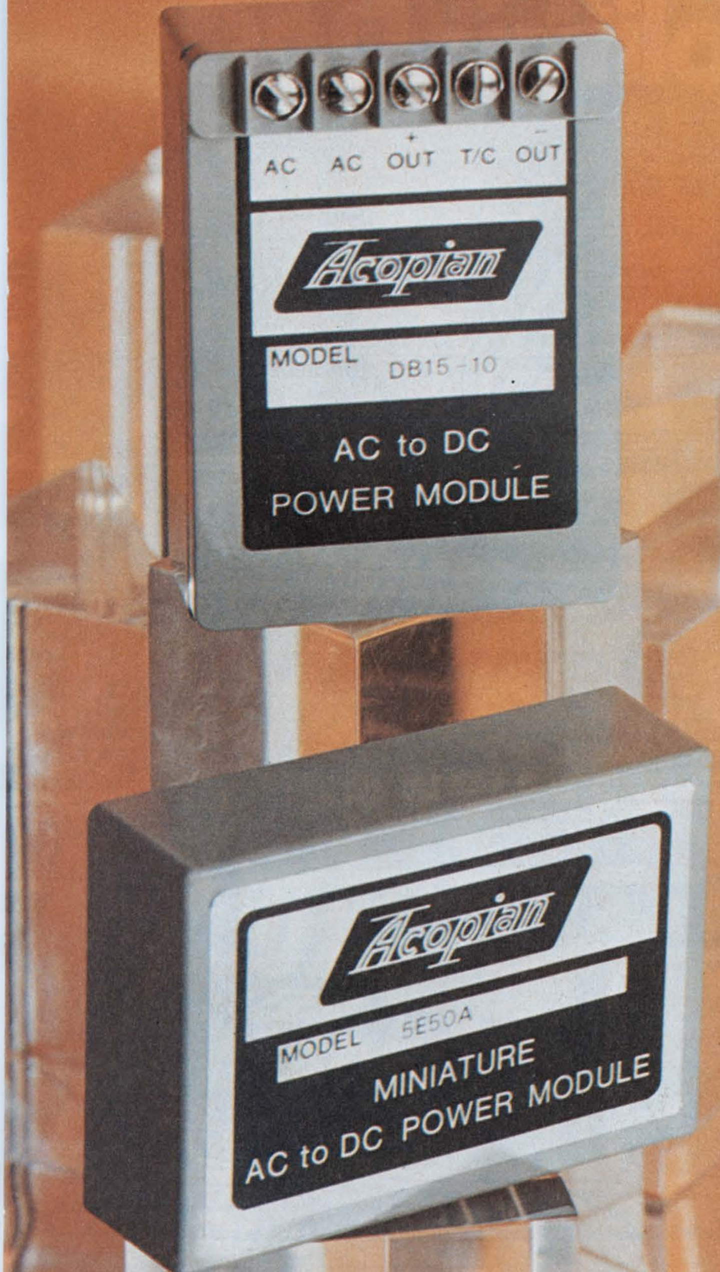

For Logic and Op Amps

With Screw Terminals

Nominal Output Voltage	Output Current Amps.	Regulation Load ±%	Regulation Line ±%	Ripple mv RMS	Price	Model	Case Size
5	.500	.15	.05	1	$ 55	5EB50	EB-10
5	1.0	.25	.05	1	75	5EB100	EB-13
5	1.5	.35	.1	1	105	5EB150	EB-13
5	2.0	.25	.05	1	115	5EB200	EB-20
5	2.5	.25	.05	1	130	5EB250	EB-20
±12	.100	.05	.05	1	55	DB12-10	EB-10
±12	.150	.05	.05	1	65	DB12-15	EB-10
±12	.200	.05	.05	1	75	DB12-20	EB-10
±12	.300	.05	.05	1	105	DB12-30	EB-13
±12	.350	.05	.05	1	110	DB12-35	EB-13
±12	.500	.1	.05	1	135	DB12-50	EB-20
±15	.100	.05	.05	1	55	DB15-10	EB-10
±15	.150	.05	.05	1	65	DB15-15	EB-10
±15	.200	.05	.05	1	75	DB15-20	EB-10
±15	.300	.05	.05	1	105	DB15-30	EB-13
±15	.350	.05	.05	1	110	DB15-35	EB-13
±15	.500	.1	.05	1	135	DB15-50	EB-20

PCB Mounting

Nominal Output Voltage	Output Current Amps.	Regulation Load ±%	Regulation Line ±%	Ripple mv RMS	Price	Model	Case Size
5	.250	.05	.05	0.5	$ 39	5E25	ES-10
5	.500	.1	.05	1	49	5E50A	EL-10
5	1.0	.2	.05	1	69	5E100	EL-13
5	1.5	.3	.1	1	98	5E150	EL-13
5	2.0	.15	.05	1	110	5E200	EL-20
5	2.5	.15	.05	1	125	5E250	EL-20
±12	.025	.1	.05	1	24	D12-03	ES-10
±12	.050	.1	.05	1	39	D12-05	ES-10
±12	.100	.05	.05	1	49	D12-10A	EL-10
±12	.150	.05	.05	1	59	D12-15A	EL-10
±12	.200	.05	.05	1	69	D12-20	EL-10
±12	.300	.05	.05	1	98	D12-30	EL-13
±12	.350	.05	.05	1	105	D12-35	EL-13
±12	.500	.1	.05	1	130	D12-50	EL-20
±15	.025	.1	.05	1	24	D15-03	ES-10
±15	.050	.1	.05	1	39	D15-05	ES-10
±15	.100	.05	.05	1	49	D15-10A	EL-10
±15	.150	.05	.05	1	59	D15-15A	EL-10
±15	.200	.05	.05	1	69	D15-20	EL-10
±15	.300	.05	.05	1	98	D15-30	EL-13
±15	.350	.05	.05	1	105	D15-35	EL-13
±15	.500	.1	.05	1	130	D15-50	EL-20

Input Voltage: 105-125 Vac, 47 to 420 Hz, single phase.

Output Voltage Setting: Single output models are factory preset to within ±2% of nominal output voltage, and may be more precisely trimmed to the nominal voltage rating with an external trim resistor. Dual models are set to within ±1% of their nominal ratings, and are not trimable.

Polarity: Either positive or negative terminal of a single output module may be grounded. Dual output modules have a positive/common/negative output terminal configuration.

Ambient Operating Temperature: −20 to +71°C. (Model 5E150 and 5EB150, 0 to +71°C.) No derating required.

Temperature Coefficient: 5-volt models, .03%/°C; dual output models, .015%/°C.

Impedance: 0.07 ohm at 1 kHz, 0.2 ohm at 10 kHz (approx.).

Optional 230 Volt Input: To order, add suffix "-230" to model number and $10.00 to price.

Case Sizes and Weight:
EB-10: 3.5" x 2.5" x 1.375" (1 lb)
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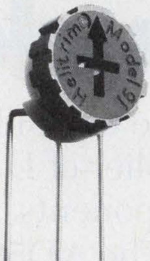

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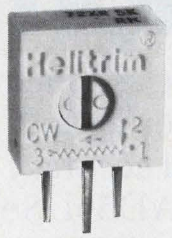

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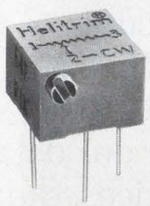

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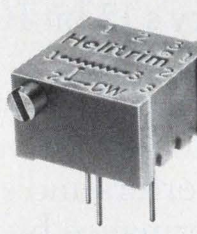

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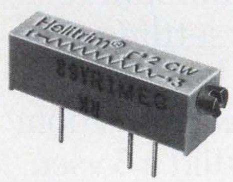

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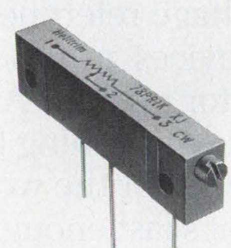

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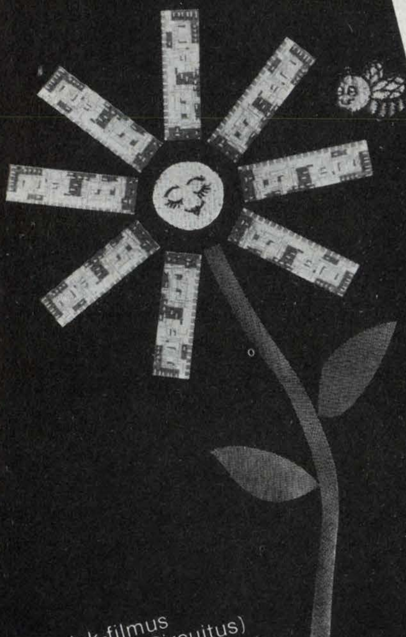

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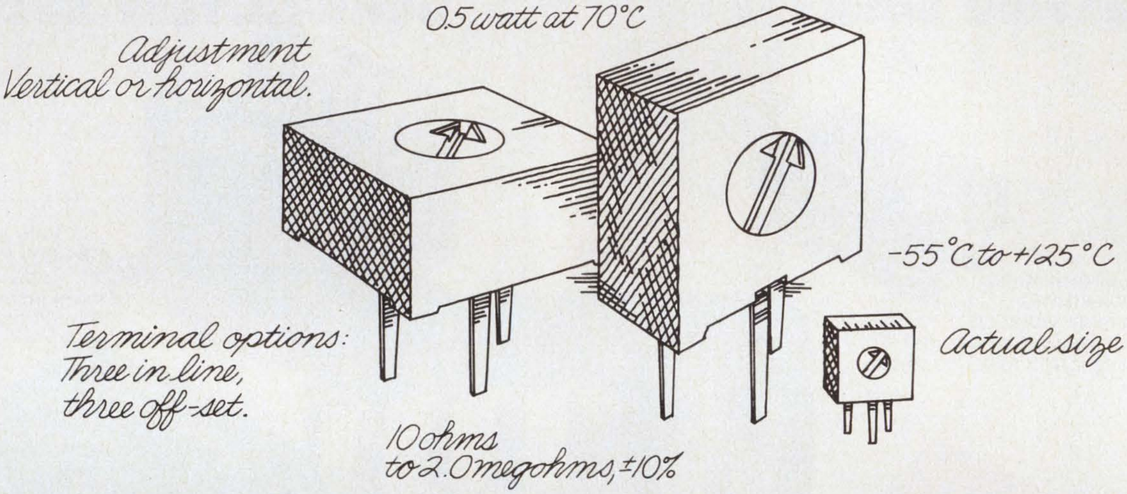

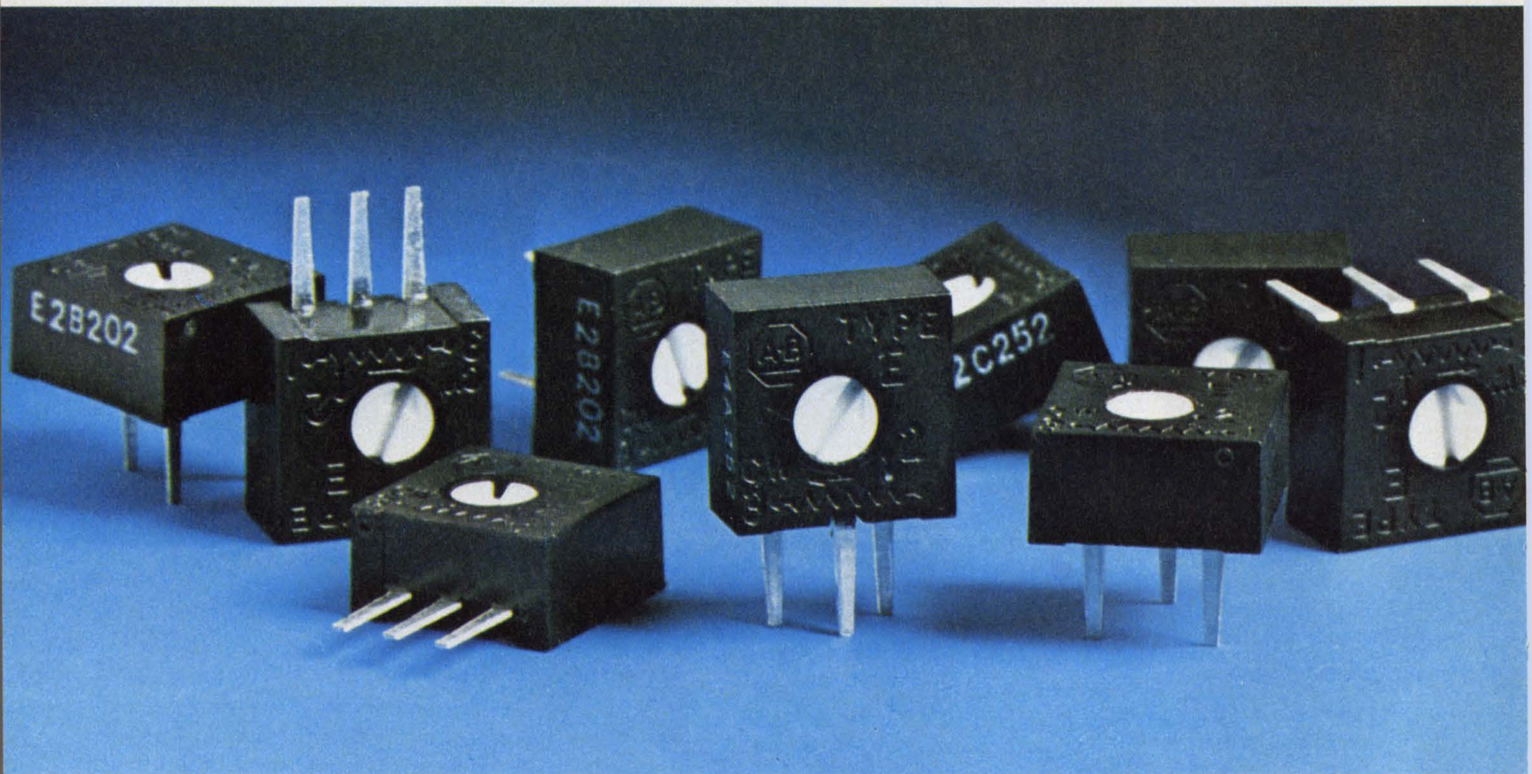

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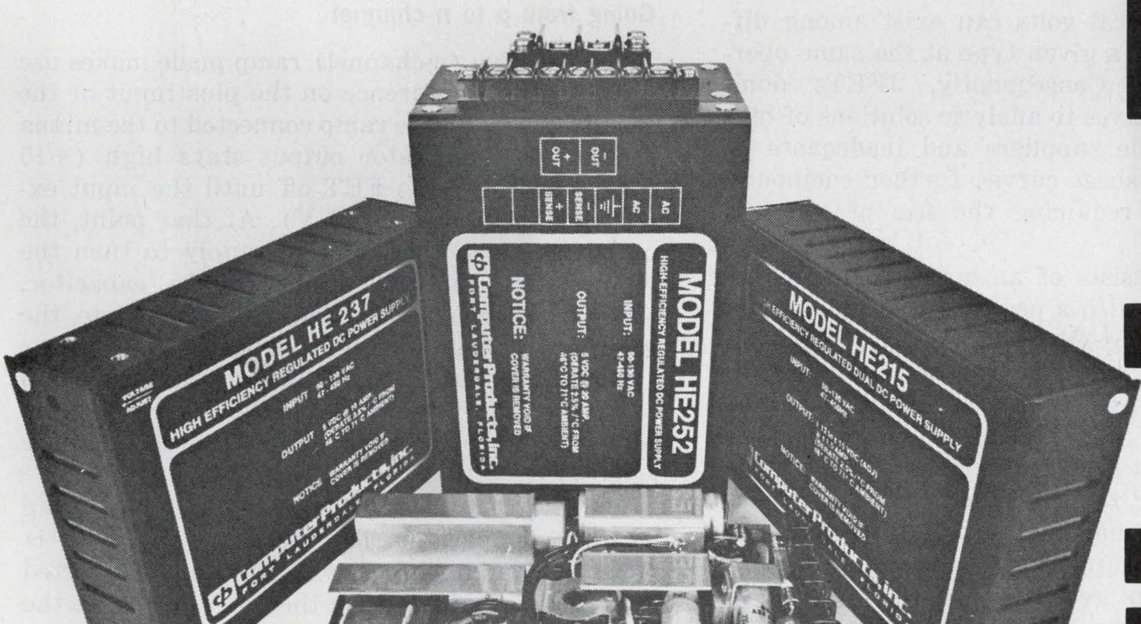

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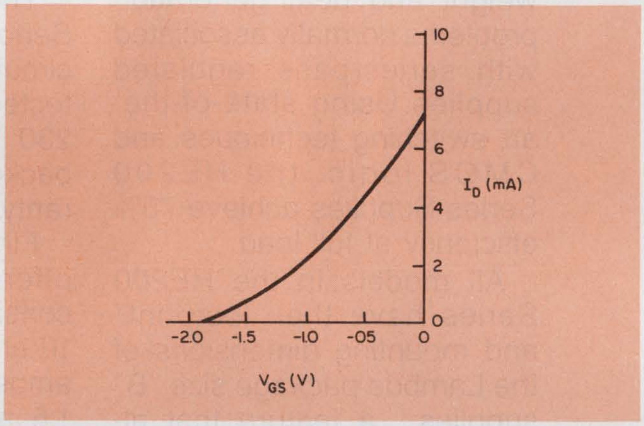
CIRCLE NUMBER 58

Trace FET bias curves on any oscilloscope, and save extensive computation time. A simple curve tracer can be made with relatively few parts.

You can build a simple curve tracer with a quad op amp and a handful of parts. The circuit displays drain current-vs-gate voltage for both p and n-channel JFETs on any oscilloscope at a constant drain voltage (Fig. 1).

The circuit may be limited to merely displaying I_D vs V_{GS}, but this curve is the one most needed by designers—it provides insight into parameter variations of bias circuits, and can be used to observe temperature effects on the FET.

The oscilloscope's vertical input shows the drain current and the horizontal shows gate voltage. If no horizontal input is available, the horizontal sweep can be used. In that case, a sweep rate of 0.5 ms/cm corresponds to 0.5 V/ms, which allows the curve tracer to be used with any scope.



1. **Output of the curve tracer** is a typical FET transfer curve, like this one for an n-channel unit.

The problem with calculations

By their very nature, JFETs are voltage-controlled devices. Unfortunately, gate-to-source variations of several volts can exist among different versions of a given type at the same operating conditions. Consequently, JFETs don't easily lend themselves to analytic solutions of bias networks. Multiple suppliers and inadequate or nonexistent data-sheet curves further compound the problem by requiring the use of a curve tracer.

The circuit consists of an op-amp, current-to-voltage amplifier with a positive or negative-gate sweep voltage (Fig. 2). The amplifier takes up one-fourth of the quad op amp and uses switchable feedback resistors to scale drain current: 1 kΩ for 1 mA/V, 200 Ω for 5 mA/V and 100 Ω for 10 mA/V. An npn-pnp emitter follower buffers the amplifier to handle high FET currents (to 100 mA). A unity-gain inverting amplifier provides proper drain-current polarity.

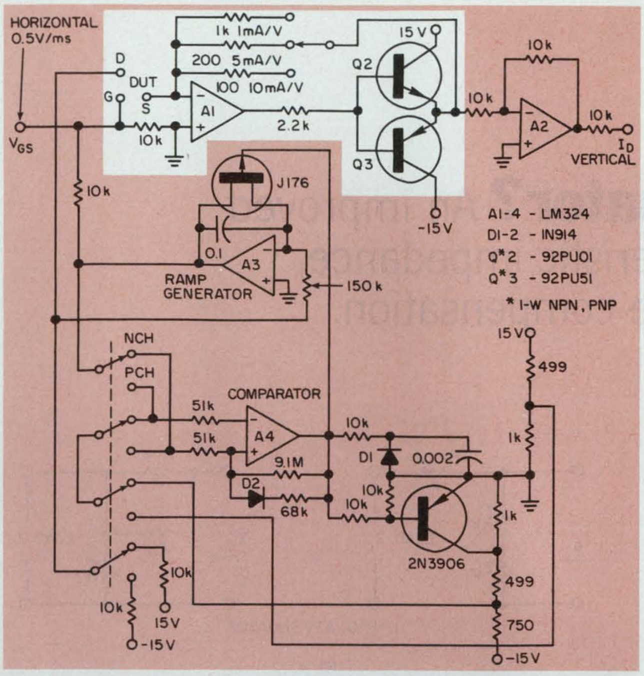
The gate-sweep generator consists of a resettable linear ramp generator and a window comparator. The ramp generator is an op amp with a capacitor in its feedback loop (Fig. 3). Sweep rate is set by a constant current supplied to the capacitor through a resistor tied to either the plus or minus voltage supply.

Going from p to n channel

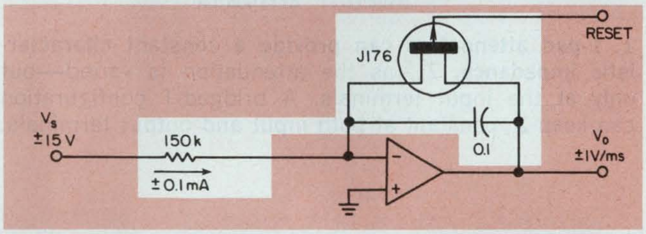
The positive (p-channel) ramp mode makes use of the positive reference on the plus input of the comparator, with the ramp connected to the minus input. The comparator output stays high (+15 V), and pinches the FET off until the input exceeds the reference (+10 V). At that point, the output snaps to the negative supply to turn the FET switch on and discharge the capacitor. When the comparator output is in a low state, the reference voltage at the plus input is set near ground by the 51-kΩ input resistor, diode D_2 and 68-kΩ feedback resistor. When the capacitor is discharged, the comparator resets, and restarts the ramp (Fig. 4a).

A negative sweep is more difficult to generate with the comparator. The reference (−10 V) is now on the minus input, with the ramp connected to the plus input. As with the positive sweep, the comparator output stays high until the negative sweep exceeds the reference. Now, the reference cannot be set to ground for the reset sweep but must be set to a negative voltage so that when the ramp is at zero, the comparator resets (Fig. 4b). The function of Q_2 is to short R_1,

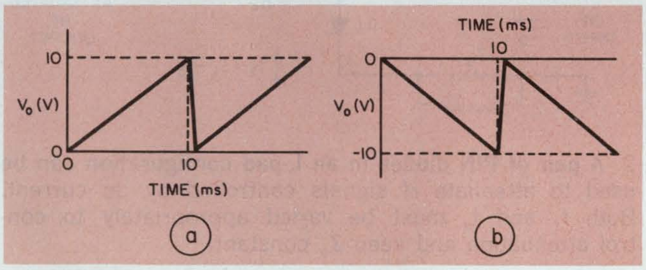
John Maxwell, Senior Engineer, National Semiconductor, 2900 Semiconductor Dr., Santa Clara, CA 95051.



2. **Basis of the tracer** is a current-to-voltage converter designed around an op amp (A_1), one-fourth of a quad. Amplifier A_2 forms a unity-gain inverter, while A_3 and A_4 form the sweep generator. Sweep rate is 0.5 V/ms.



3. **The linear ramp generator:** the J176 resets the ramp, and the RC combination determines the sweep rate.



4. **Switching operation from p-channel to n** charges the sweep from a positive (a) to a negative-going ramp (b). In both instances, the sweep time is 10 ms.

which changes the reference voltage from −10 to −6 V.

In both positive and negative cases, the sweep takes 10 ms. The resistive attenuator on the FET gate terminal divides the voltage in half to yield a sweep rate of 0.5 V/ms with a maximum gate voltage of ±5 V. This rate should be adequate for most FET amplifiers. If additional gate voltage is required, the attenuator can be switched out. ■■

Need a PIN-diode attenuator? An improved circuit provides a constant characteristic impedance, logarithmic control and temperature compensation.

If you configure a PIN-diode attenuator properly, you can achieve a constant characteristic impedance, temperature compensation and a logarithmic control of attenuation. Here's a simple arrangement that provides all these properties and operates to 120 MHz with better than a 1.1-to-1 VSWR. The maximum attenuation is over 30 dB and the minimum attenuation, or insertion loss, is 0.3 dB.

At high frequencies, PIN diodes function as current-controlled resistors whose resistance can be varied over a range of about 2 Ω to 10 kΩ. This behavior allows them to be used as rf switches and electronically variable attenuators.

At low frequencies, PIN diodes act like conventional diodes. The transition frequency between the two modes is governed by the diode's minority-carrier lifetime and may be as low as 1 MHz for the latest diodes. Above the transition-frequency, distortion introduced by the diode rapidly declines.

In fact, PIN-diode attenuators produce much less intermodulation distortion than variable-gain transistor stages. And with proper combinations of shunt and series diodes that are suitably biased, the PIN attenuator can provide a constant-impedance characteristic.

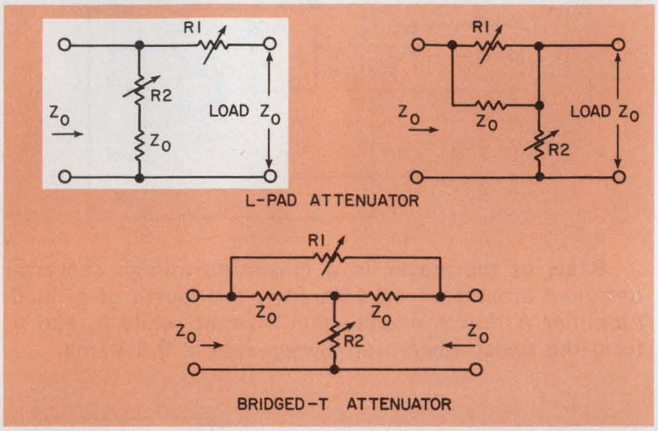
However, it's difficult to maintain a correct relationship among the dc currents that are used for biasing the different diodes at all attenuation settings. Conventional drive circuits employ combinations of current and voltage sources, but they are at best only a compromise solution. The circuits don't keep the impedance constant over the whole attenuation range.

Before attacking the problem of biasing the diodes, let's look at the criteria for constant impedance in L and T pads.

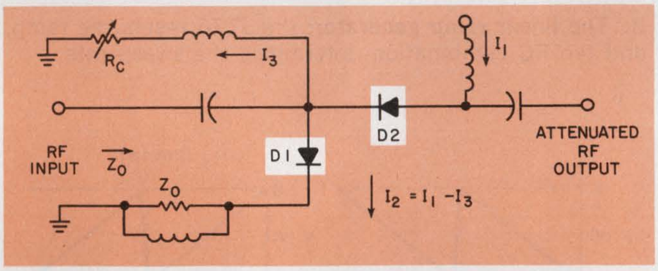
Keeping the attenuator impedance constant

A single-section attenuator pad can have three variable elements, such as in a T or π section, or

Roger S. Viles, Principal Electrical Engineer, Xerox Research (UK) Ltd., 99 Bridge Rd., East, Welwyn Garden City, Hertfordshire, AL7 1LQ, UK.



1. **L-pad attenuators can provide a constant characteristic impedance,** Z_0, as the attenuation is varied—but only at the input terminals. A bridged-T configuration can keep Z_0 constant at both input and output terminals.



2. **A pair of PIN diodes in an L-pad configuration** can be used to attenuate rf signals controlled by dc current. Both I_1 and I_2 must be varied appropriately to control attenuation and keep Z_0 constant.

two variable elements, R_1 and R_2, as in the L or bridged-T sections of Fig. 1. When correctly configured, the L-pad sections present a constant impedance, only when "looked at" from the input side. The bridged-T configuration, however, is matched in both directions.

If the voltage ratio, V_{out}/V_{in}, is r, then for the L pads,

$$R_1 = \frac{Z_0\,(1 - r)}{r},$$

and

$$R_2 = \frac{r\,Z_0}{(1 - r)}$$

to keep the input constantly equal to Z_0 as r is varied. For the bridged-T pad,

$$R_1 = Z_0\,(1 - r)$$

and

$$R_2 = \frac{Z_0}{(1 - r)}.$$

Therefore, the two-variable-element attenuators have a characteristic impedance given by

$$Z_0 = \sqrt{R_1\,R_2}. \qquad (1)$$

And maintenance of a constant impedance independent of the attenuation setting requires that the product, $R_1\,R_2$, be held constant.

Implementing a PIN L-pad

A constant-input impedance, Z_0, can be attained for variable attenuator action if two PIN diodes, D_1 and D_2, are arranged as in Fig. 2, and the dc currents through them, I_1 and I_2 respectively, are properly controlled. The inductors and capacitors in Fig. 2 merely serve to separate the rf signals and dc-current paths; variable resistor R_c provides a path for dc current and allows variations in I_1 and I_2.

The high-frequency resistance of a PIN diode is given by the equation,

$$R = \frac{A}{I^x}, \qquad (2)$$

where

I = forward current,
$x \approx 0.88$ (a constant),
A = diode constant.

To satisfy the constant-impedance criterion of Eq. 1, the product of the resistance, $R_1\,R_2$, of D_1 and D_2 must be kept constant. So if $A_1A_2/I_1^xI_2^x$ is to be constant, then I_1I_2 must be held constant.

Most methods for keeping the product of two currents constant involve expensive circuit elements such as analog multipliers or logarithmic amplifiers. However, a simpler method can be used for a two-PIN-diode attenuator pad. Since the diode's forward current is an exponential function of forward voltage, keeping the sum of the two forward voltages constant will hold the product of the two currents constant.

For each PIN diode, the forward current can be expressed as

$$I = I_0\,e^{qV/kT}, \qquad (3)$$

when forward-biased by a voltage, V. The other terms in this equation are defined as

q = charge on an electron,
k = Boltzmann's constant,
T = temperature in °K
I_0 = reverse saturation current.

As a result,

$$I_1\,I_2 = I_{01}\,I_{02}\,e^{q(V_1+V_2)k/T}.$$

However, this result is true at only one temperature, because

$$I_0 = B\,f(T),$$

where B is a constant for any one diode. Therefore,

$$I_1\,I_2 = B_1\,B_2\,f^2\,(T)\,e^{q(V_1+V_2)/kT}.$$

Compensating for temperature changes

The temperature sensitivity of the PIN diodes can be compensated with two reference diodes, D_3 and D_4, as in Fig. 3. If in each reference diode the current is

$$I' = B'\,f(T)\,e^{qV'/kT},$$

for the two diodes in series, the current product is

$$(I')^2 = B_1B_2\,f^2(T)\,e^{q(V_1'+V_2')k/T}.$$

By maintaining

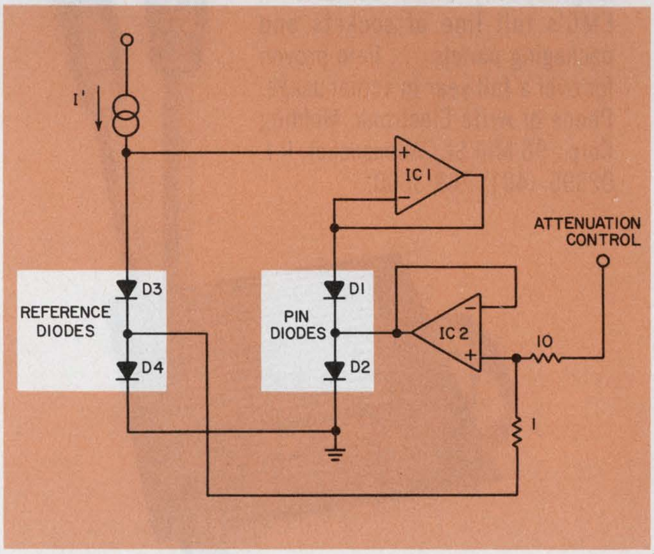
$$V_1 + V_2 = V_1' + V_2', \qquad (4)$$

then

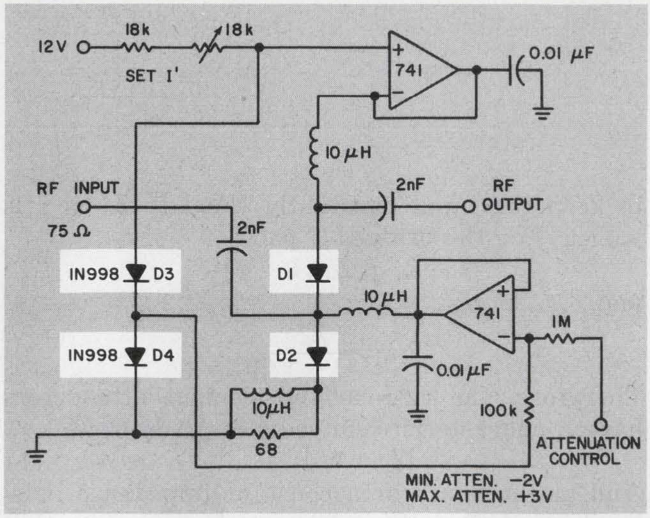
$$\frac{I_1I_2}{(I')^2} = \frac{B_1B_2}{B_1'B_2'}.$$

Consequently, I_1I_2 can be constant as required if I' is held constant, and if all four diodes, when mounted in the circuit, are kept at the same temperature by close thermal coupling.

In Fig. 3, the voltage follower, IC_1, keeps the



3. **Constant attenuator impedance and temperature compensation** are attained when the PIN diodes are matched against reference diodes in this arrangement. Op amp IC_1 keeps the voltage drive to both sets of diodes equal, and IC_2 acts as a current-sink control for the PIN diodes and as a temperature compensator.



4. **A working PIN-diode attenuator** must provide separation of the dc control-current and rf-signal paths.

sum voltage across the PIN diodes equal to the sum voltage across the reference diodes, in accordance with Eq. 4. And voltage follower IC_2 acts as a current-source and sink to change the PIN-diode current and control the attenuation.

As derived previously, temperature compensation of the constant-impedance part of the circuit is inherent in the four-diode design. However, the temperature compensation of the attenuation-control function is achieved by referencing the attenuation-control input to the mid-point of the reference diodes.

Since the attenuation-control voltage varies the PIN-diode currents exponentially (Eq. 3), a fairly linear relationship exists between control voltage and attenuation on a logarithmic, or dB, scale. This relationship is highly advantageous for many applications.

Building a practical attenuator

The functional circuit of Fig. 4 follows the configuration of Fig. 3 and provides the necessary blocking capacitors, inductors and low-pass filters to separate the dc and rf paths. The circuit is designed as a 75-Ω L-pad attenuator with HP5082-3081 low-distortion PIN diodes. For these diodes the I_1I_2 needed to attain 75-Ω impedance is $(540\ \mu A)^2$ and the corresponding sum of forward voltages is 1.2 V. The 68-Ω resistor in the path of D_4 differs from the theoretical value of 75 Ω because of the residual series resistance of the PIN diode.

Of course, good high-frequency design and layout techniques are essential to take advantage of the circuit's ability to achieve a constant impedance over a wide frequency and temperature range. The use of chokes and blocking capacitors with low parasitic reactances is especially important. ■■

Simple CMOS keyboard encoder circuit programs voltage source in 1-V steps

You can now easily get the convenience of keyboard control of a voltage source by using a CMOS IC key encoder. The encoder scans, debounces, encodes and latches the position of any key in an array.

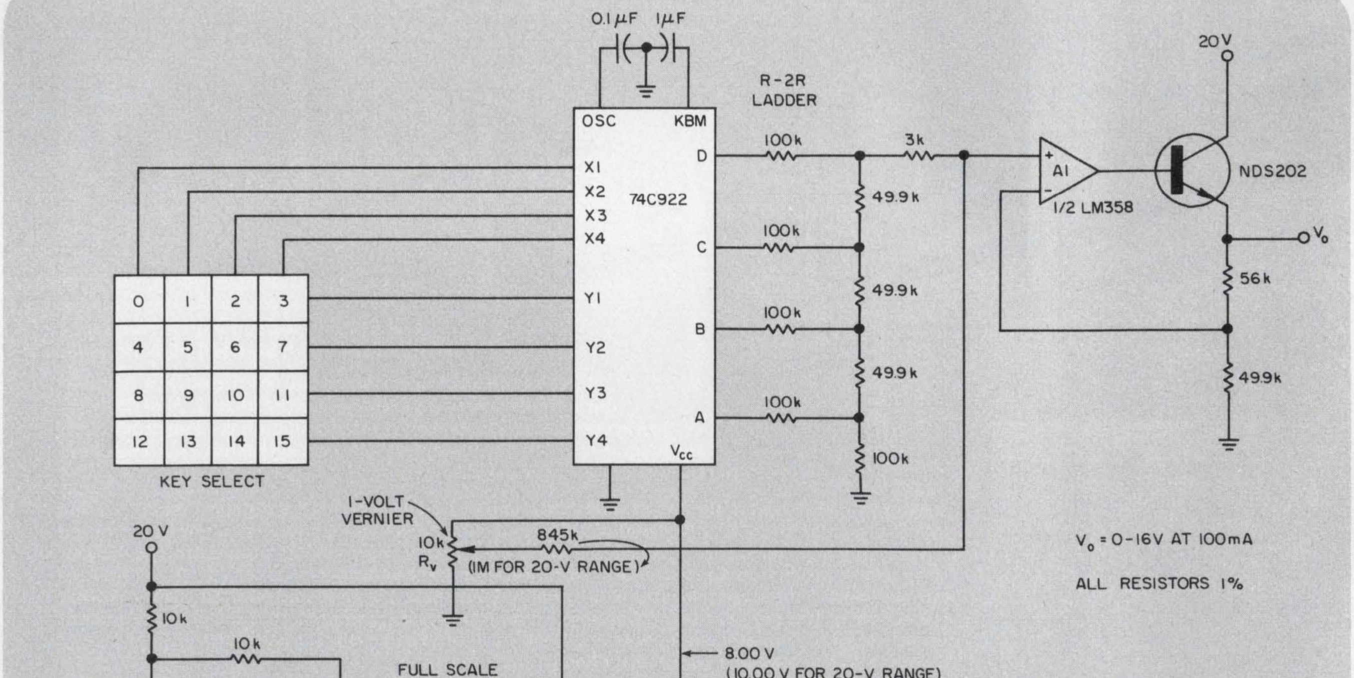
In the circuit shown in the figure, the keys program output voltage in 1-V steps from zero to 15 V, when a 74C922 IC encoder is used. A 1-V vernier, R_v, adjusts voltages between steps, increasing them above the keyed value, so the full range is zero to 16 V. The arrangement can easily expand to 20 V maximum by using a 74C923, a 20-key assembly and another resistor-ladder section. At least 100 mA can be supplied without the aid of an external heat sink.

The encoder binary outputs are summed in an R-2R ladder and then added to a properly weighted vernier voltage to become the reference input voltage for the circuit's output op amp, A_1.

The V_{CC} supply of the encoder, derived from op amp A_2, is adjusted accurately to 8.00 V for a 16-key encoder and 10.00 V for a 20-key unit.

Gerald Buurma, National Semiconductor, 2900 Semiconductor Dr., Santa Clara, CA 95051.

CIRCLE NO. 311



Press a key and the corresponding voltage appears at the output in 1-V steps. A 1-V vernier adjustment varies the voltage between steps and adds the vernier to the keyed value.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At the bench . . . away from the bench . . . This super-compact five function, 22 range DVOM has all the features you'd expect from Triplett. Like 3½ digit hi-intensity LED display, rechargeable snap-in Ni Cad Battery Pac™ with an AC charger. And, you get all the "automatics" that make life a lot simpler: Auto-zeroing, auto-polarity and auto low-battery warning. The red and gray probe includes a switch with momentary "ON" and lock "ON" and "OFF" positions for convenient operation.
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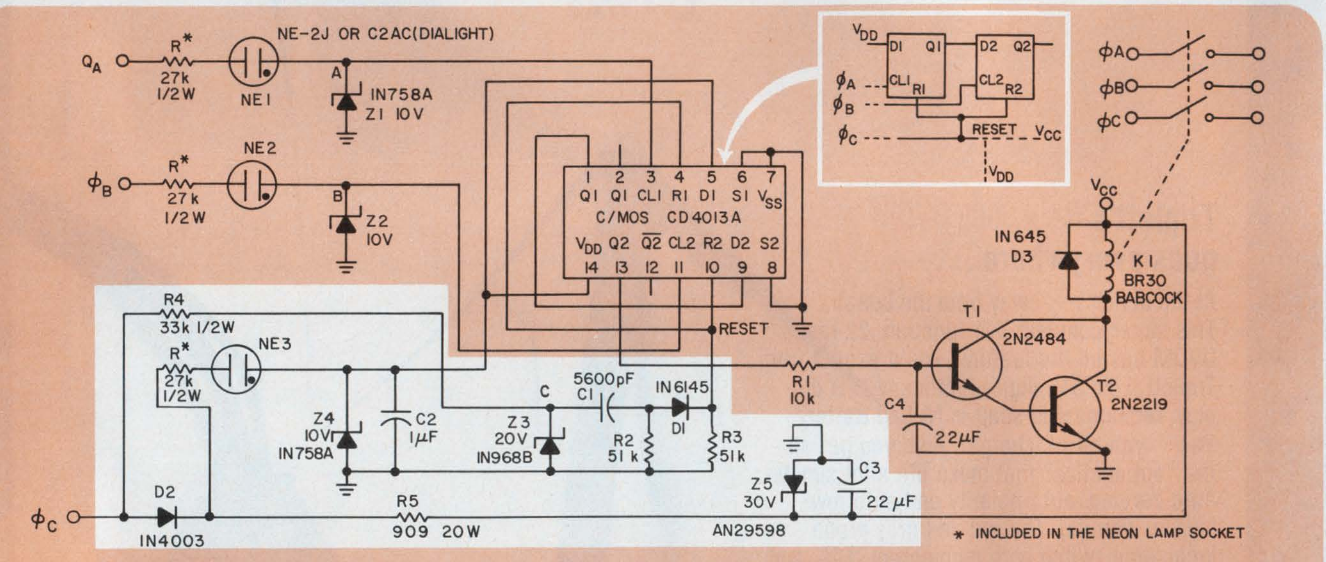
Phase-sequence detector built with a dual D-type flip-flop

One CMOS dual D-type flip-flop and several easily obtainable discrete components are all that is needed to build a circuit to detect the correct phase sequence in a three-phase ac source (Fig. 1). The circuit energizes a relay when the phase rotation is correct. Though the values shown are for a 115-V, 400-Hz three-phase source, the circuit can work on other power frequencies and with little modification on other voltages. The relay de-energizes when the sequence is wrong, or if one of the phases drops below 50% of the nominal voltage value.

The sine wave of each input phase is squared by the zener diodes Z_1, Z_2 and Z_3, and square waves A and B (Figs. 1 and 2) are applied to the flip-flop clock inputs, CL_1 and CL_2, respectively. Square wave C is differentiated by the C_1R_2 combination.

Positive-going pulses that develop across R_2 are fed through diode D_1 to both reset inputs of the two flip-flops. As a result, when the input sequence is correct, a train of rectangular pulses appears at the Q_2 output of the second flip-flop (Fig. 2). Finally, after some low-pass filtering by R_1 and C_4, these Q_2 pulses drive the output Darlington, T_1 and T_2, into conduction and energize a relay.

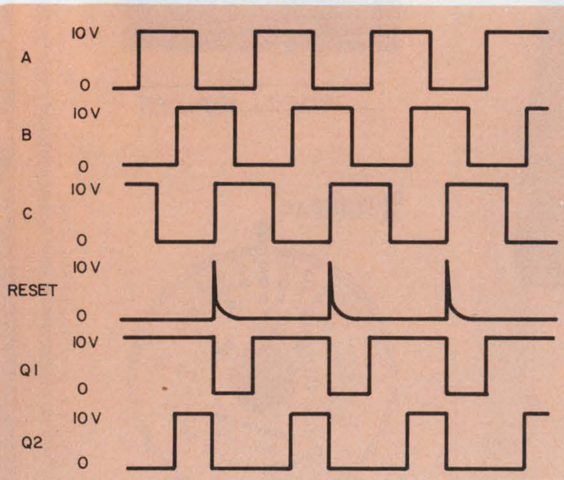


1. The phase-sequence detector circuit derives its supply voltage, V_{cc} and V_{dd}, from ϕ_c. This factor, together with the neon lamps and zener diodes in the phase inputs, establishes a 50% threshold that detects low voltage or absence of one or more phases. Relay K_1 energizes for correct phase volts.

If the phases are in a wrong sequence, or if ϕ_A or ϕ_B is missing or less than 50% of the nominal voltage, the output Q_2 remains LOW. In addition, the relay won't pull in if ϕ_c drops below the 50% threshold since the circuit's power voltages, V_{cc} and V_{dd}, are both obtained from ϕ_c.

The neon lamps, NE_1, NE_2 and NE_3, give a visual indication when the three phases are present, and together with the 10-V zener diodes provide the required 50% threshold.

If a visual indication is not desired, the neon lamps can be replaced by suitable Diacs or four-layer diodes.



2. Any one of the following correct phase sequences—ABC, BCA or CAB—will produce a train of rectangular pulses at the output Q_2, in Fig. 1. For incorrect sequences—BAC, ACB or CBA—the output, Q_2, stays LOW.

Amos Blumin, Technician Engineer, Ministry of Defense, State of Israel, P.O.B. 2250, Haifa, Israel.

CIRCLE NO. 312

Build a warbling alarm generator with two op-amp oscillators

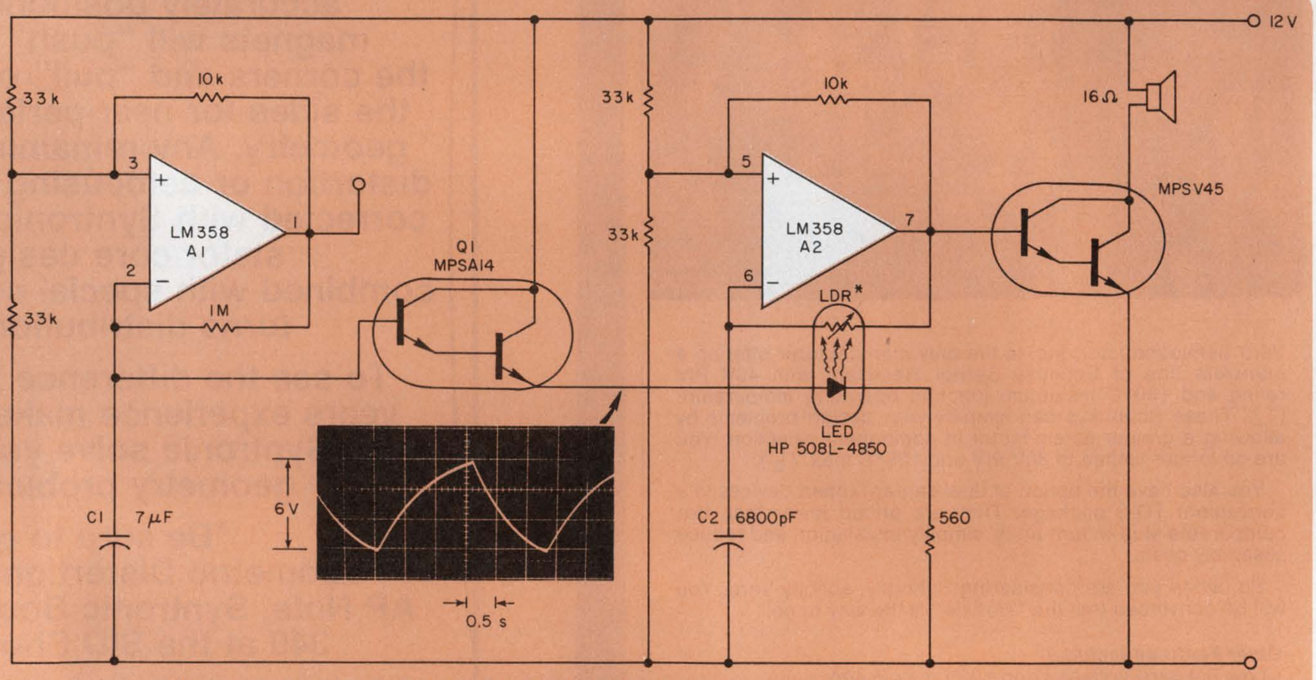
A penetrating alarm that's difficult to ignore and capable of cutting through high background noise is generated by the circuit in the figure. It consists mainly of two op-amp oscillators. One oscillator, A_1, operates around 1/2 Hz and another, A_2, operates at a variable frequency, sweeping from 200 to around 5000 Hz.

Oscillator A_1 generates a triangular signal at its inverting input terminal. The signal is amplified by the Darlington, Q_1, which drives a LED. The LED current changes from 0 to about 30 mA and back. The resistance of the light-sensitive resistor, LDR, which is illuminated by the LED, varies accordingly and changes the frequencies of oscillator A_2.

With the components shown on the diagram, the sound from the speaker rises gradually from about 200 to 5000 Hz in 1.02 s and then decreases in 1.32 s. The frequency range can be shifted by changing C_2 and the time of rise and fall by changing C_1.

Gunnar Gotschalken, Lavrans vei 15, Oslo 6, Norway.

CIRCLE NO. 313



*LDR - LIGHT-SENSITIVE RESISTOR, PHILIPS (232260094001) ENCLOSED, AND ILLUMINATED BY LED.

A distinctive alarm is generated by this two-oscillator circuit. Op amp A_1 generates a triangular signal that sweeps the frequency of op-amp oscillator A_2 from 200 to 5000 Hz.

IFD Winner of November 22, 1976

Wallace E. DeShon, Engineer, Applied Automation, Inc., Pawhuska Rd., Bartlesville, OK 74004. His idea, "Use TTL or CRT Interchangeably on µP System" has been voted the Most Valuable of Issue Award.

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CIRCLE NUMBER 66

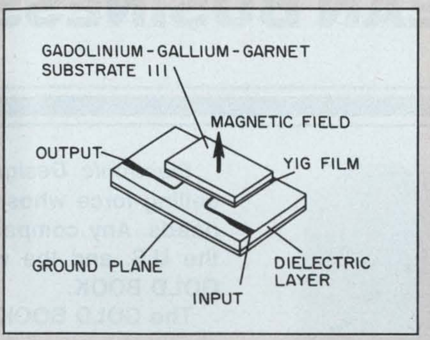
CIRCLE NUMBER 67

Compact YIG film delay line is nondispersive

A compact, low-loss microwave delay line with a 150-MHz bandwidth in the 7-to-11-GHz operating range has been developed by the General Electric Co., Wembley, England. Magnetostatic-wave propagation within an epitaxial yttrium-iron-garnet (YIG) film is used to provide such delays.

Earlier delay lines of this kind suffered from a major drawback—they were inherently dispersive because the group delay was a monotonic function of frequency.

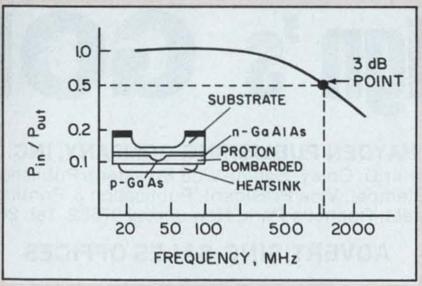
The delay line provides nondispersive delays of 75 to 125 ns over any 150-MHz bandwidth from L to the X-band. An applied magnetic field controls the operating frequency. Delay is achieved with forward-traveling magneto-static volume waves that propagate within a dielectric layered structure. The magnitude of the delay, like the nondispersive bandwidth, remains virtually constant.



An 18.4-μm YIG film is grown by the liquid-phase-epitaxy technique on a < 111 >-oriented gadolinium-gallium-garnet substrate. Preliminary measurements have revealed no saturation effects for forward-traveling magnetostatic volume waves at frequencies down to 0.6 GHz. Below this frequency, excessive insertion loss occurs because the YIG film is no longer magnetically saturated.

Gallium-arsenide LED has high bandwidth

A gallium-arsenide LED produced by researchers at the University of Munich, West Germany, has an unusually high 3-dB modulation bandwidth that is greater than 1 GHz. Usually, the bandwidth of such a device—which is used in optical-transmission systems—is limited by a long electron lifetime as well as the diode's space-charge capacitance.



For high-speed LEDs, a short electron lifetime can be obtained by high active-layer doping. But as the doping level is increased, LED efficiency is reduced and its spectrum broadened. A homostructure with an active-layer width shorter than the electron diffusion length can be used to reduce the electron lifetime further. The time delay due to the diode's space-charge capacitance can be shortened as well by using a small area for the p-n junction and a low doping level for the electron-emitting n layer.

All these techniques have gone into making the German-produced LEDs. The devices consist of a 2-μm wide layer of n-GaAlAs doped with Sn ($n = 5 \times 10^{16}$ cm^{-3}) and an active layer of p-GaAs doped with Ge ($p = 1.5 \times 10^{19}$ cm^{-3}). Active-layer width is 1.2 μm. The p-layer doping level corresponds to a bulk electron lifetime of 1 μs and an electron diffusion length of 2.3 μm. Because the width of the active layer is only 1.2 μm, the effective electron lifetime is reduced to less than 200 ps. Isolation of the p-n junction outside the light-emitting area is achieved by proton bombardment to obtain a small active area 50 μm in diameter.

The figure shows the normalized light output against modulation frequency; the broken lines indicate a 3-dB modulation bandwidth of 1.1 GHz (1100 MHz).

For a dc bias of 100 mA, the LED emission is W/steradian/cm^2 with an emission wavelength of 895 nm and a spectral line width of 36 nm.

Laser used for remote air pollution sensing

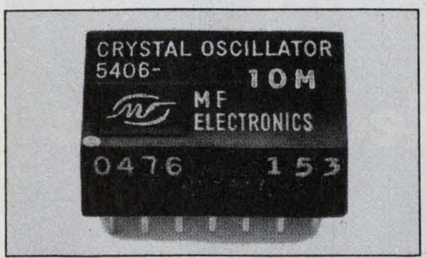
In a two-year research project, sponsored in part by the National Swedish Environment Protection Board in Stockholm, laser beams are being used for the remote sensing of air pollution.

Beams are directed at smoke emitted from chimneys. Reflections from smoke particles are returned to a receiver and converted into computer data.

Tests have been made at Sweden's West Coast Scanraff refinery and AB Ferrolegeringar in Trollhattan.

Remote sensing of pollution has so far been carried out from a distance of between 300 m and 2 km.

One failure in 3,810,000 unit hours proves our success.



At MF Electronics, people were constantly telling us how good our oscillators were, usually over the phone.

In fact, an engineer from Stromberg-Carlson, one of our major customers, told us some pretty impressive facts. Also over the phone.

Could you, we wondered aloud, put that in writing? We're not asking for an endorsement. Just tell us your experience with our product.

He did. And what he wrote back to report to us was this:

Our oscillators were used on a clock card assembly in the common control to provide primary timing signals for switching network and feature operation. Since the system was designed with a non-redundant single common control, *reliability* of the clock card and oscillator was *essential*.

Breathlessly, we read on.

Out of approximately 3,810,000 part-hours of crystal oscillator operations, he wrote, ONLY ONE failure was identified!

Just as we were about to burst with pride, we remembered the one failure. Because we guarantee our oscillators, naturally we replaced it.

But what we won't replace is our determination that none of our oscillators will ever fail.

And from this we will not waver.

Below, we have listed various types of the oscillators we make. Browse through it. If you are interested in a quality oscillator, MF Electronics makes it.

MF DIP CRYSTAL OSCILLATORS • 4-65 MHz

Series	Temperature of Operation	Frequency Accuracy, All Conditions
5406 / 5407	0 to +65°C	±.005% (±50 ppm)
5406-1 / 5407-1	0 to +65°C	±.0025%
5406-2 / 5407-2	–55 to +65°C	±.005%
5406-3 / 5407-3	0 to +85°C	±.005%
5406-4 / 5407-4	0 to +125°C	±.0075%
5406-5 / 5407-5	–55 to +85°C	±.005%
5406-6 / 5407-6	–55 to +125°C	±.0075%

SPECIFICATION OVER ALL TEMPERATURES, FULL LOAD 5406 / 5407 (All units)

	MINIMUM	TYPICAL	MAXIMUM	
Input Voltage	4.75	5.0	5.25	volt
Input Frequency	As Specified from 4 to 65 MHz			
Input Current 4 MHz to 10 MHz		20	40	ma.
Input Current Above 10 MHz to 65 MHz		25	50	ma.
Frequency Accuracy (All Conditions)	See Preceding Table			
Waveform Symmetry, measured at 1.5 v	40/60		60/40	
Rise Time, 4 MHz to 10 MHz, 0.8 to 2.4 volts		7	20	ns.
Fall Time, 4 MHz to 10 MHz, 2.4 to 0.8 volts		4	20	ns.
Rise Time over 10 MHz to 19.9999 MHz, 0.8 to 2.4 v		3.5	15	ns.
Fall Time over 10 MHz to 19.9999 MHz, 2.4 to 0.8 v		3	10	ns.
Rise Time from 20 MHz to 65 MHz, 0.8 to 2.4 volts		2.5	5	ns.
Fall Time from 20 MHz to 65 MHz, 2.4 to 0.8 volts		2	5	ns.

MF ELECTRONICS CORP.
118 E. 25th St., New York, N.Y. 10010 (212) 674-5360 TWX: 710-581-4109

CIRCLE NUMBER 71

A/D and D/A Converters... Call the Can-Do Company

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CIRCLE NUMBER 72

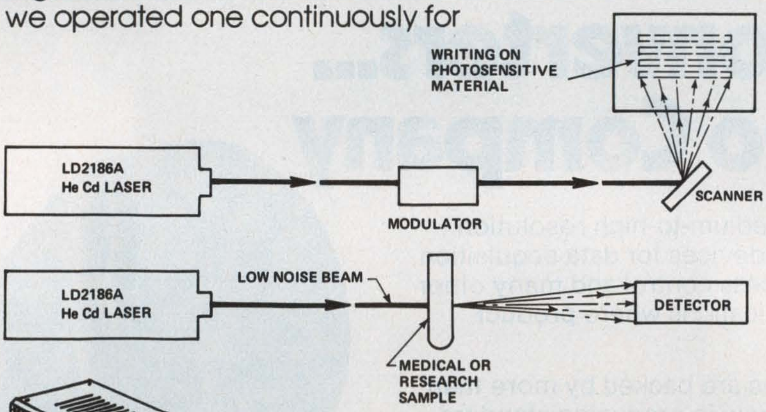
Opening new frontiers with electro optics

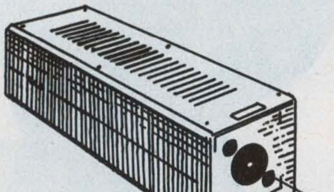
RCA Helium-Cadmium lasers offer long life: we ran one for more than 12,000 hours.

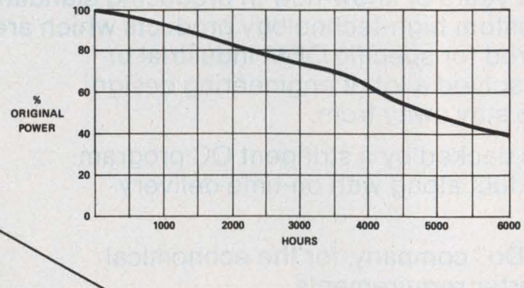
If you need 20 mW typical output in the blue region (441.6 nm), you get that and a lot more in RCA's Helium-Cadmium Laser System LD2186A.

You also get excellent long-term stability: ±1% typ. Low noise: 0.7% rms typ. (10 Hz to 10 MHz). Convection cooling: no fans or water. And—very important—long life.

As the graph shows, typical life is greater than 6,000 hours—but we operated one continuously for more than 12,000 hours. A helium reservoir plus an innovative recirculating cadmium system are what make the LD2186A a reliable, long-life system for facsimile, COM, phototypesetting, pollution monitoring, video recording and non-impact printing. LD2186A is available from stock. For UV applications, we also offer a version with 325 nm output.



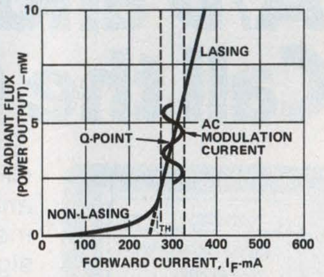




Circle 141

Solid state laser breakthrough: CW output at room temperature!

You get at least 5 mW of continuous lasing in a solid state package. RCA's new AlGaAs CW injection lasers have a rise time of less than 1 ns—allowing modulation rates beyond 100 MHz. This plus small source size (13 x 2 μm typical) and 820 nm wavelength make the C30130 and C30127 well suited to optical communications, facsimile, fiber-optic transmission, document reading, flying spot scanning.



Circle 142

If electro optics can solve your problem, remember: EO and RCA are practically synonymous. No one offers a broader product spectrum. Or more success in meeting special needs. Call on us for design help or product information. RCA Electro Optics, Lancaster, PA 17604. Phone 717-397-7661. Sunbury-on-Thames, Middlesex TW16 7HW, England; Ste.-Anne-de-Bellevue, Quebec, Canada; Belo Horizonte, Brazil; Hong Kong.

RCA

New Products

Fast fall-time power transistors handle large secondary breakdown energy

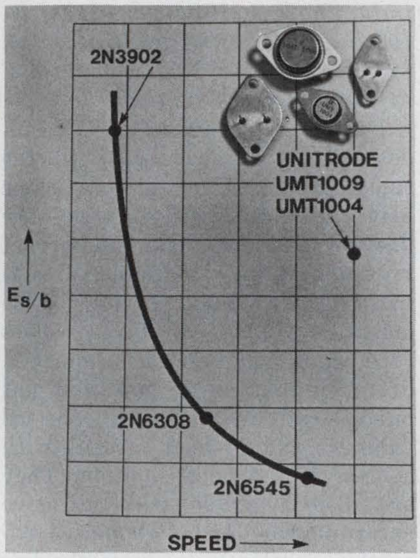
Unitrode Corp., 580 Pleasant St., Watertown, MA 02172. (617) 926-0404. $5.62: UMT 1009 (100 up); spring, 1977.

A significant advance in the state of the art of switching power transistors has just been announced by Unitrode. Under uniform test conditions, its UMT1008/9 (8 A, 400/500 V_{CEV}) npn transistors, which are built into an innovative, triple-diffused mesa configuration, can provide about half the fall time (t_f) and more than three times the reverse-biased, secondary-breakdown energy capability ($E_{s/b}$) of such competing units as the popular 2N6514, 2N6544 and 2N6579.

Since fall time, in particular, greatly depends not only on circuit configuration but also voltage, current and load levels, uniform test conditions are mandatory for valid comparisons. Representative units were checked in the circuit and under voltage/current conditions specified by both Unitrode and the competition. Most often, according to Unitrode engineers, UMT1008/9 units had a superior t_f.

Preliminary specifications for the UMT1008/9 guarantee a maximum t_f of 0.4 μs and $E_{s/b}$ of 1.5 mJ at 25 C. In the comparison tests, however, units typically checked out with a t_f as fast as 0.17 μs and an $E_{s/b}$ as high as 5 mJ. And at 100 C, the Unitrode transistors came out even better than the other units tested.

Unitrode claims that its new proprietary transistor design eliminates the performance compromises imposed by conventional designs: Low t_f designs usually result in poor $E_{s/b}$. In addition, when a conventional power transistor is turned off, the transistor's conduction region shifts from the periphery of the emitter structure toward the center. This shift has two adverse effects:



1. As conduction shifts away from the emitter edge, the base resistance between the shifting conduction site and the base terminal increases. Consequently, when the base is driven from a practical impedance source with a finite resistance, the increasing base resistance reduces the turn-off base drive by 1/2 to 1/4 the initial value and greatly increases fall time.

2. As the conduction area shrinks and moves toward the center of the emitter, the power density increases and severely limits the conventional device's $E_{s/b}$.

Unitrode's design innovation holds the conduction region at the emitter periphery during the entire turn-off period. As a result, the turn-off base drive remains substantially constant during device turn-off, t_f improves considerably and the $E_{s/b}$ limitation caused by current crowding vanishes.

As a result, the cost of the base-drive circuitry can be reduced by trading the improved t_f off against reduced turn-off base drive. For example, fall times adequate for efficient operation of a 20-kHz, off-line switching regulator can be achieved without using a high negative-voltage turn-off signal. Simply putting a resistor and a ferrite bead between base and emitter can provide a suitable turn-off time.

An efficient switching transistor must possess a low t_f, because a major portion of the transistor's power dissipation occurs during this time: The collector current, although falling, is still substantial, while the collector voltage is at least 90% of the circuit's V_{cc}. Therefore, manufacturers invest considerable effort in designing power transistors with low fall times. In addition, the circuit designer is advised to strongly reverse-bias the transistor when turning it off, which also reduces fall time.

Since many loads are inductive, the $E_{s/b}$ rating is important: It defines the amount of energy that the transistor can safely absorb, unclamped, in a reverse-biased avalanche mode. Although circuit designers should avoid working the transistor in the avalanche mode, by using clamping or snubbing devices, a high permissible $E_{s/b}$ indicates a high safety factor.

Unitrode CIRCLE NO. 301
Motorola CIRCLE NO. 302
RCA CIRCLE NO. 303
TRW CIRCLE NO. 304

Five-digit LED display offers many options

National Semiconductor, 2900 Semiconductor Dr., Santa Clara, CA 95051. (408) 737-5000. $8.40 (100 up); stock.

The 5900 series of GaAsP LED reflective displays, 0.5-in. high, offers both common-anode (NSB-5922) and common-cathode (NSB-5921) multiplexed versions for five digits, and an option of direct-drive overflow/polarity indication with four digits in a common-anode multiplexed format (NSB-5917). Electrical connection is by PC-board terminals on the edges of the displays. CIRCLE NO. 308

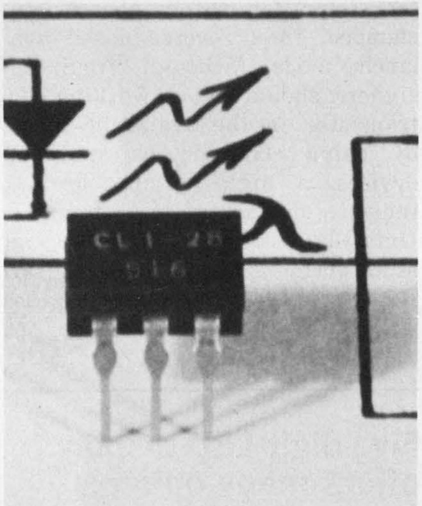
Power transistor rated 100 W at 500 V

International Rectifier, 233 Kansas St., El Segundo, CA 90245. (213) 322-3331. $7.93 (100-999); stock.

A new power transistor, the npn 2N5157, rated for maximum power dissipation of 100 W and designed for operation at 500 V (collector-to-emitter) and 3.5 A is available with collector-to-base voltage ratings as high as 700 V. The units are especially well suited for applications in inverters and chopper regulators, automotive ignition circuits and high-voltage power supplies. Packaging is in industry standard JEDEC TO-3 metal cases. Maximum junction operating temperature is 150 C, and the maximum thermal resistance (junction-to-case) is 0.75 C/W.

CIRCLE NO. 309

Opto-isolators operate directly on ac inputs

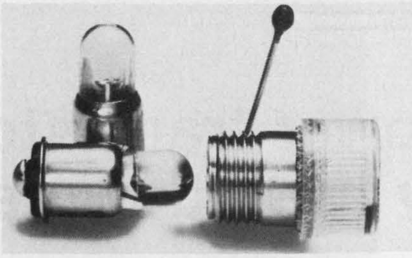


Clairex Electronics, 560 S. Third Ave., Mount Vernon, NY 10550. (914) 664-6602. $1.40 (1000 up); stock.

Four new opto-isolators permit operation directly with an ac input. The units use two infrared emitting diodes connected in inverse parallel in the input circuit. Two of the units (CLI-25/26) use phototransistors in the output circuit, and the other two units (CLI-27/28) use photo-Darlington outputs. All of the units provide a minimum isolation of 2500 V peak.

CIRCLE NO. 310

LEDs directly replace incandescent lamps



Data Display Products, 5428 W. 104th St., Los Angeles, CA 90045. (213) 641-1232. $1.21: 5 & 6 V (1000 up); stock to 5 wks.

Direct replacement of incandescent bulbs with LEDs in the same package and at the same brightness, but with 10 times the lifetime and only half the current required is now possible. Designated the MF200 series, these lamps available in three colors (red, amber and green) require a drive current of 20 mA and put out typically 50 mcd (red), 35 mcd (amber) and 24 mcd (green) with a clear tinted encapsulation. They are also available with diffusive encapsulation. Although pulsed operation drastically reduces the life of incandescents, LEDs can operate either pulsed or continuously for at least 10 yr at 20 mA. LEDs can also display short pulses for which an incandescent can't respond quickly enough. All of the LED lamps are available with built-in resistors for various voltages ranging from 3.6 to 28 V dc. Units are also available for ac operation.

CIRCLE NO. 320

Darlingtons offered in complementary series

Solitron Devices Inc., 1177 Blue Heron Blvd., Riviera Beach, FL 33404. (305) 848-4311. $12: 2N5286/3, $15: 2N6284/7 (1-99); 2 to 4 wks.

All planar, the 20-A complementary Darlington power-transistor series is packaged in standard TO-3 cases. The npn units are identified as 2N6283-84 and pnp as 2N6286-87. Typical specifications for these devices include V_{CE} (sat) at 10 A of 2 V, an h_{FE} of 750 to 18,000 at $I_C = 10$ A and a maximum power dissipation of 160 W. The 2N6283 and 2N6286 units feature a BV_{CEO} of 80 V; the 2N6284 and 2N6287, a BV_{CEO} of 100 V.

CIRCLE NO. 321

New counters from Mostek.

Our 28 pin up/down series feature price and performance.

Mostek's new MK 50398N and MK 50399N P-Channel MOS counters offer important cost/performance advantages to a broad range of up/down counting applications: six decades, single power supply, plus the economy of a plastic package.

More Features that Count.

Versatile, up/down counting with the ability to pre-set the individual decade stages to any BCD number, increases your systems operating capability.

➤**Scan Oscillator.** Multiplexed scanning of the digit strobes is controlled by the scan oscillator input, which is self-oscillating when terminated with a capacitor; or the scan input can be driven by an external signal, a feature useful for synchronization in microprocessor applications.

➤**High Frequency Counting.** DC to one MHz, selectable to two MHz.

➤**CMOS Compatibility.** Interfaces with CMOS logic operating in the 10 to 15 volt range.

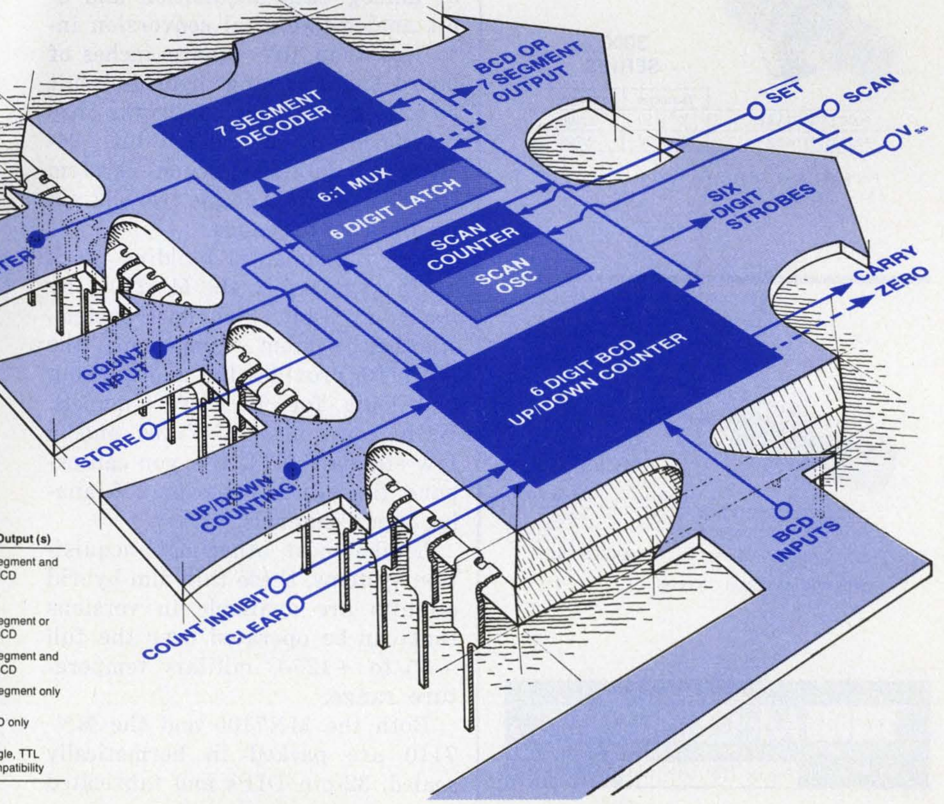
➤**BCD or 7-Segment Outputs.** The MK 50398N presents 7-segment output data from the counter contents, while BCD outputs are provided by the MK 50399N.

More Mostek counters to choose from:

The MK 50398 counter series joins Mostek's complete family of counter circuits ranging from four decade to multifeatured six decade devices. Contact your Mostek representative or franchised distributor for full specifications.

MOSTEK

1215 West Crosby Road • Carrollton, Texas 75006 • (214) 242-0444 • **MOSTEK GmbH** • West Germany • Telephone: (0711) 701096 • **MOSTEK ASIA** • Hong Kong • Telex: 85148MKA HX

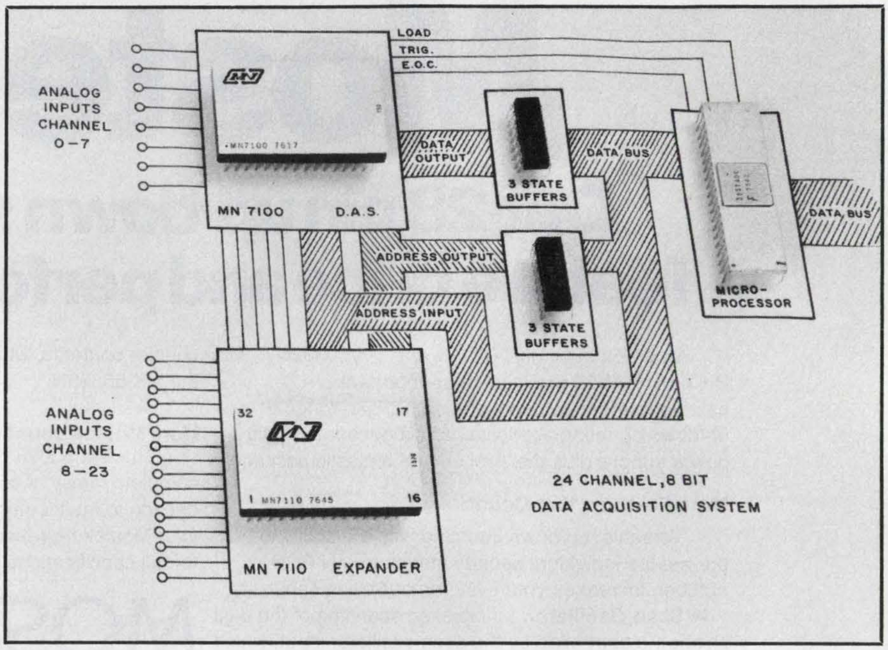


Mostek's complete counter family.

Counter Series	Description	Maximum or Frequency Access Time	Dip Leads	Output (s)
MK 50395/6/7N	6-decade Up/ Down Counter w/compare Register	1MHz	40	7 Segment and BCD
MK 50398/9N	6-decade Up/ Down Counter	1MHz	28	7 Segment or BCD
MK 5002N	4-digit Counter/ Latch Decoder	250KHz	28	7 Segment and BCD
MK 5005N	4-digit Counter/ Latch Decoder	250KHz	24	7 Segment only
MK 5007N	4-digit Counter/ Latch Decoder	250KHz	28	BCD only
MK 5009N	Counter Time Base	2MHz	16	Single, TTL compatibility

CIRCLE NUMBER 75

24-channel, 8-bit a/d comes in just two 32-pin DIPs



Micro Networks, 324 Clark St., Worcester, MA 01606. (617) 852-5400. P&A: See text.

Now, you can pack 24 channels of analog data acquisition and 8-bit analog-to-digital conversion into less than five square inches of board space. Using hybrid-circuit technology, Micro Networks has developed a complete 8-bit, 24-channel data-acquisition system that is packaged in two 32-pin dual-in-line packages.

The fundamental building block of the system is the MN7100, by itself an 8-bit, 8-channel system. Another system component, the MN7110, provides the multiplexing and logic for 16 more channels. With additional MN7110s and a few standard TTL ICs, you can expand the system to over 256 analog-input channels.

Unlike most other data-acquisition systems, these thin-film hybrid circuits are available in versions that can be operated over the full −55 to +125-C military temperature range.

Both the MN7100 and the MN-7110 are packed in hermetically sealed, 32-pin DIPs and fabricated with thin-film chip-and-wire hybrid construction. In addition, the MN-7100 is laser-trimmed during manufacture, which eliminates the need for user-supplied offset and gain-adjusting trimmers.

Also, while data-acquisition systems employing these DIPs are small, they have all the features of their larger counterparts. Input channels may be randomly addressed or controlled from the internal sequential-address counter, and both channel-address inputs and outputs are provided. All digital inputs and outputs are TTL-compatible, and either internal or external clocks can be used. Other specifications are 90,000-channel/s throughput, guaranteed ±1/2-LSB linearity over temperature, and low power consumption. The analog-input range is ±10 V with a typical input impedance of 10 MΩ.

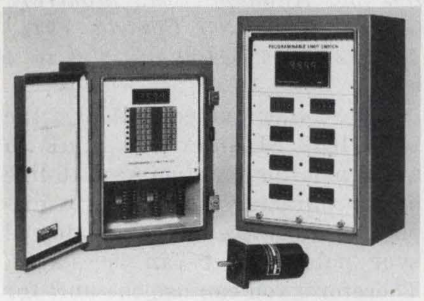
These circuits are particularly intended for microprocessor-based systems. However, these units do not offer their own three-state outputs. So when operating with a bus-oriented μP like the 8080, you must provide additional three-state buffers to isolate the data-acquisition system from the other peripherals. The data-acquisition system may be accessed as a memory location via DMA to avoid tying into the μP's data bus.

The commercial 0-to-70-C versions of the MN7100 and MN7110 are priced at $140 and $49, respectively, in 100 quantities.

The −55 to +125-C military versions are priced at $280 for the MN7100H and $118 for the MN-7110H in 100 quantities.

CIRCLE NO. 306

Magnetic cams slice to tenth of a degree



Astrosystems, 6 Nevada Dr., Lake Success, NY 11040. Don Wade (516) 328-1600. $1000-$3000 (1-9).

With Solid-State Limit Switches you get position programming and control without the use of cams, followers or mechanical switches. The switches consist of a magnetic position-sensing device and an electronics package, which provides control signals at selectable rotary positions. Coded-key or thumbwheel-switch programming lets you change settings. These units feature accuracies to 0.1° and operate bidirectionally with virtually no backlash or hysteresis. Control signals can be supplied as relay contacts, logic levels or open-collector outputs. A display and BCD output indicates shaft position for initial-setup and monitoring purposes. For dual-limit units a control signal tells you when the transducer reading is between two programmed values. For set-point units a control signal is provided when the transducer output is greater than the programmed value. In addition to the control signals a front-panel light for each limit or set point indicates the output status. Transducers are supplied in NEMA-12 and waterproof packages. Zero-reset, offset and no-motion options are available.

CIRCLE NO. 322

CIRCLE NUMBER 77 ▶

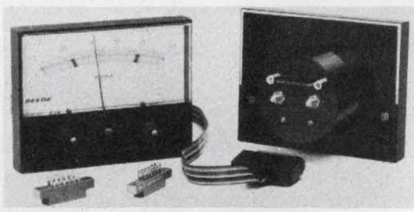
Quadrature oscillator gives more for less

Burr-Brown, International Airport Industrial Park, P.O. Box 11400, Tucson, AZ 85734. G. Athey (602) 294-1413. $9.85; stock to 4 wk.

When you need sine and cosine outputs, the 4423 quadrature oscillator offers three unique characteristics: First, you can resistively program frequency from 0.002 Hz to 20 kHz; second, it comes in a DIP; and third, you get an uncommitted op amp. In addition, the hybrid device features performance comparable with $50 modular quadrature oscillators: frequency stability is better than ±100 ppm/°C and quadrature accuracy is better than ±0.01%/°C; sine-output distortion is less than 0.2% over 0.002 Hz to 5 kHz and less than 0.5% from 5 to 20 kHz. The unit can be used as a self-contained 20-kHz oscillator, without external components or adjustment. For the range of 2 to 20 kHz, you need but add resistors to program frequency. From 0.002 Hz to 2 kHz, you program the frequency with two resistors and two capacitors.

CIRCLE NO. 323

Optoelectronic unit eases on-off control



Beede Electrical Instrument, Penacook, NH 03301. (603) 753-6362. From $40; stock.

An optoelectronic switching device, called the Meter Switch, combines analog indication with on-off control in a compact unit no larger than an ordinary panel meter. This bang-bang-type controller features optical isolation that eliminates the need for conditioning the input signal and protects against noise and ground-loop problems. Isolation gives you flexibility in selecting input-signal transducers. The device's output can control SCRs, Triacs and is also CMOS and TTL compatible.

CIRCLE NO. 324

Add alphanumerics to your μP terminal

Matrox Electronic Systems, P.O. Box 56, Ahuntsic Stn., Montreal, Quebec, H3L 3NG Canada. (514) 481-6838. $169 (100 qty); 2 to 4 wks.

Like other video RAMs, the MTX-1632 SL interfaces a μP to a TV monitor, producing a 16-line by 32-character alphanumeric display. The device accepts external sync pulses so it can be slaved. Therefore, you can use the unit for video mixing. Each character position corresponds to a memory location. Thus the μP is free to manipulate data for display. The unit doesn't require external refresh and features 550-ns access time, TTL compatibility, character blanking and single-supply operation.

CIRCLE NO. 325

5-or-6-digit counters take wide input range

Master Electronic Controls, P.O. Box 25662, Los Angeles, CA 90025. (213) 393-3177. $3 (1000 qty); stock.

Two series of 5-and-6-digit counters, the C05 and C06, include units that accept eight input levels. These devices operate from 6 to 110 V dc and from 24 to 230 V ac, with allowable variation from the nominal voltage of ±10%. The devices count at a speed of 600 counts per minute and require on and off times of 50 ms. The counters can be operated over a wide range of temperature and humidity conditions with a life expectancy of 1-million operations. They can be panel or surface mounted, have black numerals on a white background, and weigh 5 oz.

CIRCLE NO. 326

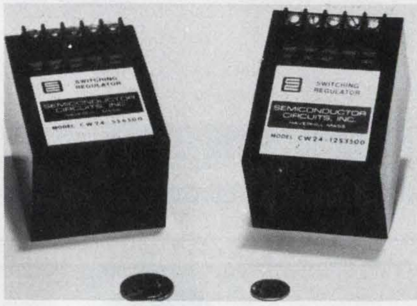
Small switcher supplies lots of watts

Trio Labs, Inc., 80 Dupont St., Plainview, NY 11803. (516) 681-0400. From $350; stock.

Single outputs of 125 W come from the dense Model 600's 3.28 × 7.55 × 6.78 in. You get up to 87% efficiency with a ridethrough of 30 ms and a low-line of −30%. This compact unit also contains overload and overvoltage protection. The standard switcher can be upgraded to meet environmental MIL specs. Standard outputs are 5, 12 and 15 V dc.

CIRCLE NO. 327

Efficient dc converters take wide input range



Semiconductor Circuits, 306 River St., Haverhill, MA 01830. (617) 373-9104. $30.95 to $99.95; stock to 4 wks.

Input-voltage ranges of up to 200% of nominal makes these dc/dc converters a good choice when operating from poorly regulated input power sources such at batteries, motor-generators, and fuel cells. Efficiencies of up to 85% conserve input power. SW units are plug-ins for PC boards, while CW units are chassis mountable. Thirty models are available with nominal inputs ranging from 12 to 24 V and outputs from 5 to 24 V. Models that deliver output currents up to 3 A boast line-and-load regulation of 0.3%, output-ripple and noise of 7-mV rms and need no derating over −25 to +71 C. Models with higher output currents feature line-and-load regulation of 0.5%, output ripple and noise of 13-mV rms and need no derating over 25 to +60 C. Storage temperature for all models is −25 to +85 C.

CIRCLE NO. 328

30 Ah crammed into lithium cell

Power Conversion, 70 MacQuesten Pkwy S., Mount Vernon, NY 10550. S. Chodosh (914) 699-7333. From $10; stock to 2 wks.

Lithium batteries boast the highest energy per weight and volume. The 550-5A provides 30 Ah at a 1-A drain for an energy density of 135 Wh/lb. The 10-oz cell measures 1.64 × 5.5 in. Additional features include shelf life of over 5 yr, operation down to −65 F, nominal output of 2.8 V (double that of ordinary batteries) and high rate-discharge performance. The cells are available with a positive button terminal or positive and negative solder tabs.

CIRCLE NO. 329

μP molded supplies don't feel the heat

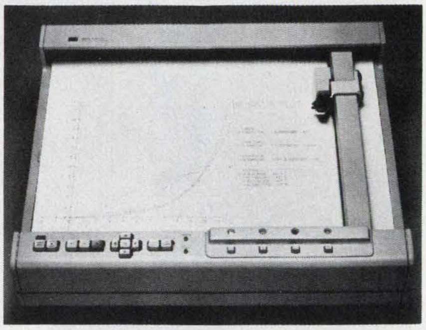
Dynamic Measurements Corp., 6 Lowell Ave., Winchester, MA 01809. (800) 225-1151. $130 to $155 (unit qty); stock to 4 wks.

Solid molding in hard epoxy permits full-power operation (30 W) with no derating up to +40-C ambient for MPS single, dual and triple dc supplies. With models tailored to specific μPs you get line-plus-load regulation within 0.03% for 5-V outputs, and within 0.1% for 9, 10, 12 and 15-V outputs. Positive and negative outputs track within 100 ppm/°C, and max. output-voltage error is +1%. 5-V outputs are current limited and all others fold back to 20 mA. The modules measure 5.1 × 4.25 × 3 in.

CIRCLE NO. 330

Superplotter draws dashed lines in four colors, doubles as printer with five type fonts

Hewlett-Packard, 1501 Page Mill Rd., Palo Alto, CA 94304. J. Peter Nelson (415) 493-1501. $4200; April, 1977.



Now you can have a μP-based X/Y plotter that automatically, under program control, selects any four different-colored pens. The Model 9872 provides crisp plots at higher speeds and with greater resolution than now available, and accommodates paper up to 11 × 17 in. The plotter is designed to be used with HP's 9825 and 9831 desktop computers. Four-color plotting in solid lines and seven dashed-line fonts, five built-in character fonts, user-defined characters and symbol-mode plotting can be combined to produce clear, easy-to-read plots. 38 different μP instructions provide such features as point digitizing, labeling and character sizing, directly through the plotter's IEEE-488 interface. The 9872's resolution is 0.008 mm, and writing speed is program-controlled from 10 mm/s to 360 mm/s in each axis. The four pens are stored in a "stable" and are picked up by the plotter arm. The pens are automatically capped after return to the stable. Five different character fonts are stored in the plotter: ANSI ASCII, 9825A ASCII, and three European sets. Character size, slant and direction are variable under program control. Window plotting can be done automatically by merely defining the limits of the desired window. User-defined characters, such as a complex logotype, can be stored in the desktop computer controlling the 9872, and written with a single command. To aid in precise positioning of the plotter arm, the Model 9872 contains a digitizing sight that can be put in the pen carriage automatically, or manually.

CIRCLE NO. 305

Batteries last 2000 h in pocket calculator

Unitrex of America Inc., 689 Fifth Ave., New York, NY 10022. (212) 688-3400. $30.

For the outdoorsman, the Model LCD 2000 pocket calculator features a liquid-crystal display that's easy to read in the sun. For the energy conscious it offers 2000 hours of operation from each set of three silver oxide batteries. In addition to the four basic functions, the super-thin Model LCD 2000 offers chain and mixed calculations, square root, automatic constant, %-key and memory. A budget model (LCD 8RM at $25) gets less battery life, but features a π-key.

CIRCLE NO. 331

Sonic pen automatically inputs coordinates

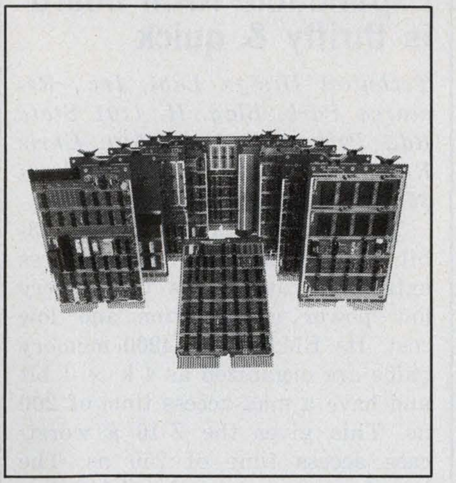
Science Accessories Corp., 970 Kings Highway W., Southport, CT 06490. Rolf Kates (203) 255-1526. $1475.

To convert coordinate location into binary computer inputs, the Graf/Pen NT211 sonic digitizer employs two solid-state "ears" and a stylus that emits ultrasonic pulses. You position the stylus anywhere on a surface up to 36 × 48 in. The NT211 then automatically converts the sensor distances into X-Y coordinates, correcting for sound velocity variations with temperature. Up to 140 points/s can be converted, with a resolution of 100 points/in.

CIRCLE NO. 332

MDB SYSTEMS presents... The LSI-11 Connection

GP Logic Modules · Peripheral Controllers · Communications Interfaces · Special Purpose Modules · Accessory Hardware Plus: DEC's own LSI-11 Microprocessor Module.



Here are some MDB Systems connections to LSI-11 microprocessors:

☐ General Purpose Interfaces:
Parallel for programmed I/O and DMA.
Do-it-yourself dual and quad wire wrap for any DIP design.

☐ Device Controllers for most major manufacturer's
Printers
Card equipment
Paper tape equipment
Plotters

☐ Communications/Terminal Modules
Asynchronous Serial Line
Synchronous Serial Line

☐ MDB Backplane/Card Guide Assembly (8 Quad slots)
Rack mount chassis 5¼″ front panel.

☐ Special Purpose Modules and Accessories
System monitoring unit provides front panel switch addressing, power on/off sequencing; line frequency clock.

☐ Bus extenders/terminators.
E-PROM and PROM modules.
Bus connectors for backplane assemblies.

MDB Systems products always equal and usually exceed the host manufacturer's specifications and performance for a similar interface. MDB interfaces are software and diagnostic transparent to the host computer. MDB products are competitively priced; delivery is usually within 14 days ARO or sooner.

MDB also supplies interface modules for DEC PDP*-11 Data General NOVA* and Interdata minicomputers.

MDB

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· Adjustment accuracy: 0.3%!
· Replaces additional voltmeter

«Power-Boost»
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Watt/Liter Power Ratio
· Cooling sections incorporated in housing yield optimum volume/power ratio

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Output:		
	0– 7,5 V/3 A (5 A)*	
	0–17 V/1,5 A (2,5 A)	
	17–40 V/1,25 A (2,1 A)	

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CIRCLE NUMBER 86

DATA PROCESSING

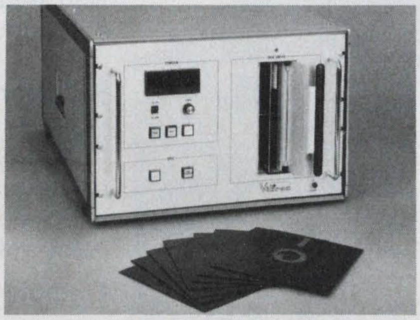
Expandable RAM board is thrifty & quick

Technical Design Labs, Inc., Research Park, Bldg. H, 1101 State Rd., Princeton, NJ 08540. Chris Rutkowski (609) 921-0321. From $574 (1 kit); 2-4 wks.

The Model Z-16 is a 16-k × 8-bit static RAM board that features extremely fast access times, very low power consumption and low cost. Its EMM Semi 4200 memory chips are organized as 4 k × 1 bit and have a max access time of 200 ns. This gives the Z-16 a worst-case access time of 250 ns. The board conforms to the S-100 bus standard (used in Altair 8800, Imsai 8080, etc.). Three nonregulated supply voltages are used, drawing typically 105 mA from the +8 V, 200 mA from the +16 V, and 20 mA from the −16 V supply. The Z-16 is organized in four blocks of 4 kbytes each, which can be individually switch-protected. The board will be compatible with TDL's Memory Management Board which will handle 256-kbytes in one system. Modules are available either as kits or as assembled and tested units.

CIRCLE NO. 333

Brushless torque meter checks floppy discs



Vibrac Corp., 11 Alpha Rd., Chelmsford, MA 01824. Bruce C. Chrane (617) 256-6581.

The Model 200 floppy-disc tester is designed to provide a fast and accurate means to measure both the starting and the running torque of diskette cartridges within their protective envelope, using a Vibrac optical brushless torque transducer. The Model 200 displays running torque on a 4-1/2-digit panel meter, in either Newton-cm or oz-in.

CIRCLE NO. 334

Programmer has version for many popular PROMs

Technitrol Inc., 1952 E. Allegheny Ave., Philadelphia, PA 19134. (215) 426-9105. From $935; see text.

Versions of the Model 107K programmer are now available for many PROMs, including Intel, National, Signetics, Harris, Fairchild, and Intersil units. The 107K features hex keyboard entry, autocopy between selectable min and max address, verify while reading or writing, and stop-on-error. Technitrol offers a general computer interface as an option. The version for 1702A PROMs is normally in stock.

CIRCLE NO. 335

Interface kit marries punch/reader to LSI-11

EECO, 1441 E. Chestnut Ave., Santa Ana, CA 92701. Dennis McLaughlin (714) 835-6000. $250.

Interfacing between DEC LSI-11 computers and EECO punched-tape readers and reader/punches is easy if you use the Model E-9000-LSI-RP kit. It contains a circuit card, interconnecting 10-ft cables, test tape and instruction manual. Existing PDP-11 software can be used to program the interface for specific applications. The circuit board plugs into the computer backplane bus. Jumpers permit you to select the peripheral device address and interrupt vector.

CIRCLE NO. 336

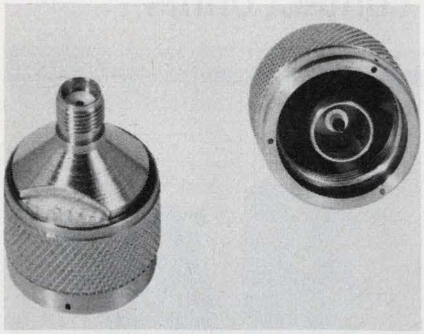
4 and 8-channel MUX integrates with Nova

MDB Systems Inc., 1995 N. Batavia St., Orange, CA 92665. (714) 998-6900. $1250 to $2250; 1 to 2 wks.

The Model 8063 multiplexer for Data General's Nova interfaces four to eight asynchronous data sets or terminals that have RS-232C output. The system can be expanded to 64 channels sharing the same device address. The 8063 is not only completely compatible with DG 4060 software, but offers additional software-controlled features including data overrun and line-break detection.

CIRCLE NO. 337

SMA adaptors now boast 1.15 VSWR, dc-18 GHz

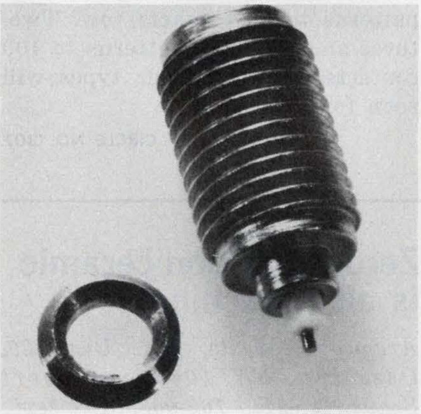


Cablewave Systems Inc., North Haven, CT 06473. Don Winn (203) 239-3311. $10.91 (500); stock.

Adaptors from SMA to type N, TNC and BNC offer improved mechanical and electrical performance; e.g. SMA to type N has a VSWR of 1.05 + 0.005 f (GHz) from dc to 18 GHz. The new version is identified by the suffix-101 instead of -001. Prices remain unchanged from the -001 series.

CIRCLE NO. 338

Hermetically sealed SMA connector passes 18 GHz



Tek-Wave Inc., 3 Delaware Dr., New Hyde Park, NY 11040. Sanford S. Lehrfeld (516) 328-0100. $4.50 (100-250); stock-4 wks.

Using a solderless gasket, the series 10-2045-1470 feedthrough connector achieves a hermetic leak rate of less than 1×10^{-8} ml/s. The glass-sealed units meet all requirements of MIL-C-39012, and can withstand soldering temperatures in excess of 250 C. From dc to 18 GHz, the VSWR is 1.1 + 0.005f (GHz). The connector has a 36UNS-2A thread, and the length is 0.444 in.

CIRCLE NO. 339

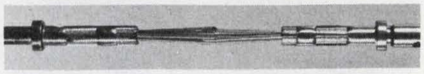
Wire-brush connector contacts mate easily, provide low contact ohms

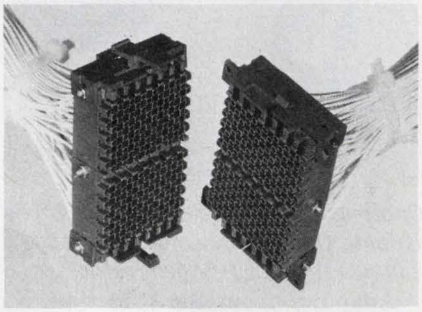
Bendix, Electrical Components Div., Sidney, NY 13838. (607) 563-9511.

The Bendix bristle-brush-bunch (B^3) contact, a new advance in contact design, combines the features of very low mating and disengaging forces and highly redundant current paths with a minimum of constrictive contact points and resultant nonuniform current densities.

Multiple-wire brush contacts (usually about seven wires/brush) on each half of a contact pair intermingle with sufficient normal force between the wires to provide good wiping action and low-resistance contact points. Each wire end in a contact bunch is cut at a precise burr-free angle to enable smooth intermingling and eliminate the butting of wires when contacts mate. As the engagement depth increases, cantilever action provides contact pressure between engaging wires.

Wire strands (6 to 8 mil dia.) are gold plated (50×10^{-6} in.) and crimped into contact holders in male and female configurations. Average initial contact resistance is about 6 mΩ and in tests increased to only 11.7 mΩ after 20,000 cycles





of mating—a very high amount of matings for the usual connector. Engaging force is under 0.8 oz/contact; thus, a 200-contact connector can fully mate with less than 10 lb of force and disengage with even less, perhaps 6 lb.

Bendix plans to introduce many types of connectors using the B^3 contacts. Available now are a mother/daughter board line, types MB and DB, containing two-row patterns to 60 contacts/row. Two, three and four-row patterns to 100 contacts/row and other types will soon follow.

CIRCLE NO. 307

Spray on rf shielding, up to 100 dB

Emerson & Cuming, Canton, MA 02021. Jeanne B. O'Brien (617) 828-3300.

Eccoshield ES is a highly conductive silver-based surface coating, formulated for rf-shielding applications. Adhesion to metal, plastics, ceramics, wood and concrete is excellent, and the spray produces a surface resistivity substantially less than 1 Ω/sq. Successive coats decrease surface resistivity further. A 6-oz areosol can normally covers about 30 ft^2. By applying Eccoshield ES to joints and seams of metal housings, it is possible to obtain greater than 100-dB insertion loss from 15 kHz to 10 GHz.

CIRCLE NO. 340

Zero-expansion ceramic is also machinable

Aremco Products, Inc., Box 429, Ossining, NY 10562. Herbert Schwartz (914) 762-0685. See text; stock.

Can you use a ceramic that survives the temperature drop from a 2000-F furnace into ice water? The Aremcolox 502-1300 boasts a zero thermal expansion coefficient over its useful temperature range of 2200 F, and is machinable to boot. Brazing fixtures, hot-gas nozzles and the like can be made with conventional carbide-tipped tools, and need no firing. Off-the-shelf rods range from 1/2 to 4 in. dia. Plates are 1/2 thick, and up to 5-3/4-in. square. A typical 12-in. rod, 1 in. dia. costs $17.15.

CIRCLE NO. 341

new count/time data system

NEW Count/Time Data System (C/TDS) counts switch closings, totalizes ON/OFF time on **up to 248 channels.** With it and your own switches you have everything you need for a sophisticated production or statistical activity monitoring system—with on-board printout, plus tape records, calculator or computer feeds. Even provides time-of-event data on selected channels!

Keyboard sets all channel inputs, crystal clock timing, reset intervals, channel scale, outputs and more. Counts 10 events/channel/sec. The C/TDS is like a giant event recorder, but with output tabulated by channel the way you want it. It's a low cost way to replace a roomful of counters, recorders, timers, and man-hours. Request Bulletin B130 from Esterline Angus Instrument Corporation, P.O. Box 24000, Indianapolis, IN 46224. Tel. 317-244-7611.

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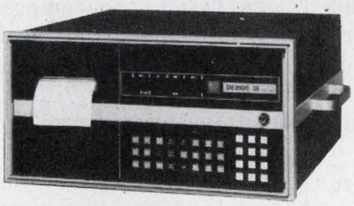
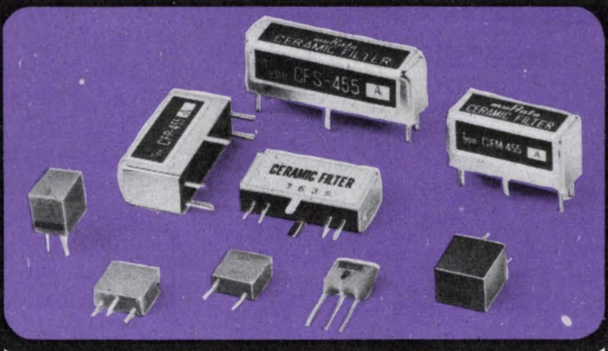


CIRCLE NUMBER 90

piezoelectric ceramic I.F. filters



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CIRCLE NUMBER 92

We're making MOS history . . . you can, too!

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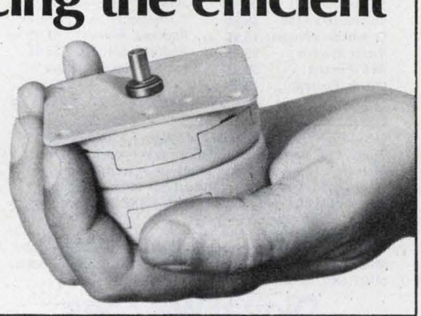
AMERICAN MICROSYSTEMS, INC.

CIRCLE NUMBER 91

Introducing the efficient little 82900 stepper motor



It gives you an edge on compactness, torque and price.

It's new. It's bidirectional. It has a 7.5° step angle. It gives you maximum pull-in/pull-out torque of 23 oz-in @ 200 pps. It's rated at 12.38w @ 5vdc and runs at lower than average temperatures.

The 82900 has a lot to offer, particularly in impact and non-impact printers, small X-Y plotters and computer peripherals. It's powerful, compact and moderately priced. And it's reliable. So reliable — in fact — that it can also be used to control pumps and valves in medical instruments and similar devices. In many applications it can replace larger, bulkier steppers at much lower cost.

Standard construction provides 2-phase operation (requiring simplified, low-cost circuitry), a 7.5° step angle and roller bearings. However, 4-phase operation, a 15° step angle or sleeve bearings can be furnished as options.

Write for information today!

A. W. HAYDON CO. PRODUCTS

NORTH AMERICAN PHILIPS CONTROLS CORP.

Cheshire, Conn. 06410 • (203) 272-0301

FOR IMMEDIATE NEEDS CIRCLE 131
FOR INFORMATION ONLY CIRCLE 132

Flat cable assemblies come in rainbow colors

AP Products Inc., Box 110, 72 Corwin Dr., Painesville, OH 44077. (800) 321-9668.

AP has come up with a faster, easier and less expensive way of interconnecting PC boards through flat ribbon cable with the company's family of Great Jumper PC connectors. The fully tested flat-ribbon cable/connector assemblies are available in a wide variety of configurations including several line widths, a choice of conductors, and a selection of opposite-end terminations. The Rainbow cable is color-coded line-by-line on the front, and color-striped in groups of ten on the reverse, and is intended for use with single-ended Great Jumpers. Double-ended and daisy-chained configurations include PC-board connectors, standard double-row (0.100-in. center) socket connectors and card-edge connectors.

CIRCLE NO. 390

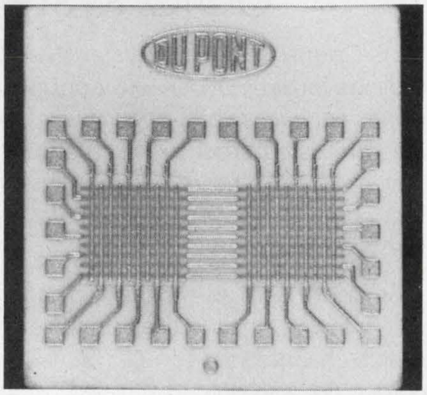
Mass termination kit expedites prototyping

T&B/Ansley Corp., 3208 Humboldt St., Los Angeles, CA 90031. (213) 223-2331. $395; stock.

Mass termination with the Blue-Macs Kit can really speed up your PC-board prototypes. The Model DK-1 kit provides an assortment of over 100 Blue-Macs insulation-displacing connectors. They include DIP plugs and sockets, PCB solder transition connectors, wrap-post solder connectors, and PC-board solder tail as well as wrap-post tail headers. With its 100-ft roll of 28 AWG stranded 50-conductor cable and precision crimping tool, the kit enables you to prototype almost any mass termination system in seconds, without wire stripping.

CIRCLE NO. 391

Thick-film multilayer ink uses no gold



Du Pont Co., Wilmington, DE 19898. (302) 774-2358. Stock.

A cost-effective alternative to precious-metal thick-film structures is now available in the form of type-9923 copper composition conductors for deposit on alumina or type-9949 substrates. After nitrogen firing, the composition has a 1.5-mΩ/square max resistivity, and can be readily soldered. Adhesion on alumina is 4 to 5 lb (90° wire-pull test), and remains over 3 lb after 150-C firing. On the low-K type 9949, adhesion is also high, and thus provides a complete material system for multilayer interconnects. Composition 9923 gives a resolution of 7-mil lines and spaces. The compositions fire at 900 C in commercial nitrogen furnaces for 45 to 50 minutes, and no preliminary burnoff of organics is required.

CIRCLE NO. 342

IC mounting pads form and spreads leads, too

Bivar Inc., 1617 E. Edinger Ave., Santa Ana, CA 92705. Edward Muldoon (714) 547-5832. See text; stock.

A new selection of 45 different IC mounting pads and spreaders for both circular and DIP devices has been added to the Bivar product line. The nylon pads and spreaders improve component mounting, and spread leads to desired configurations, acting as both tools and fixtures. The new selection includes mounts to spread circular IC leads to DIP patterns, and circular lead spreaders to 0.300, 0.350, 0.400 dia and 0.100-in. grids. Typical price in lots of 10,000 is $19 per thousand.

CIRCLE NO. 343

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George Rostky
Editor-in-Chief

Electronic Design

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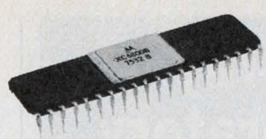
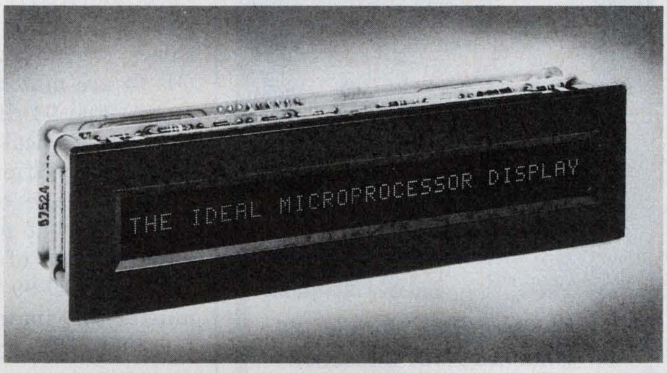


Your microprocessor, our displays...



...made for each other.

Your microprocessor-based system should have an alphanumeric readout device. In addition to the ability of your product to present alphanumeric information, such displays are extremely useful for debugging and for data recall during programming.

Burroughs' SELF-SCAN® panels readily interface to the I/O devices of the popular microprocessors, including the MC 6800, Intel's 8080 and 4040 series, National's IMP, and many others. An "off-the-shelf," inexpensive, dc-dc converter uses your system's low voltage (+5 or +12V) to supply the display. Your software programming effort to control the display represents a small portion of the overall program development.

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To learn more about the ways our displays and your microprocessor were made for each other, write to Burroughs Corporation, Electronic Components Division, P.O. Box 1226, Plainfield, New Jersey 07061. Or call one of our special sales/applications numbers:

East Coast	(201) 757-5000
West Coast	(714) 835-7335
London, England	(01) 240-1479

SELF-SCAN panel displays are available from our distributors: Hamilton/Avnet, Cramer Electronics, Arnold Barnes Associates. For overseas inquiries, write Burroughs ECD International, 11-15 Betterton Street, Drury Lane, London.

MC6800 chip photo courtesy of Motorola Corporation.

You can see the difference

Burroughs

CIRCLE NUMBER 95

INTEGRATED CIRCUITS

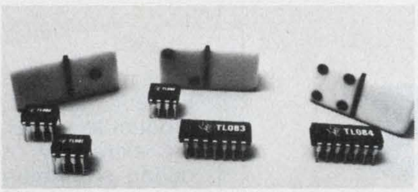
Dual amp replaces 1458 with improved specs

Precision Monolithics, 1500 Space Park Dr., Santa Clara, CA 95050. Donn Soderquist (408) 246-9222. From $3.70 (100-up); stock.

A dual matched high performance operational amplifier, the OP-14, provides improved specifications over the industry standard 1458 amplifier. Input-offset voltage and common-mode rejection ratios of the two op amps in the OP-14 are matched to within 1 mV (max) and 94 dB (min). Key maximum specifications for the individual amplifiers include input-offset voltage of 0.75 mV, input offset current of 2 nA, and input bias current of 50 nA. All units come in TO-99 packages and are pin-for-pin improved replacements for 1458/1558 types.

CIRCLE NO. 344

JFET-input op amps come in five models

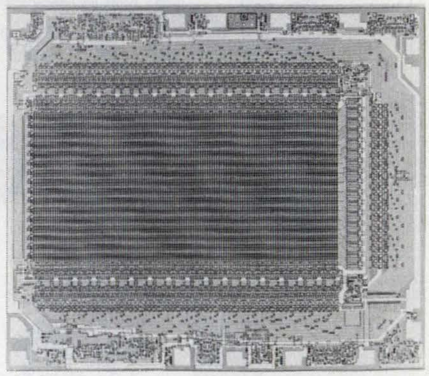


Texas Instruments, P.O. Box 5012, Dallas, TX 75222. Dale Pippenger (214) 238-2011. From $0.52 (100-up); stock.

A line of five BiFET operational amplifiers, the TL080 series, includes single, dual and quad circuit types. The op amps incorporate matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. The single op amp circuits, TL080 and TL081, have offset-voltage null capability and the 081 is also frequency compensated. The dual circuits, TL082 and TL083, both include internal frequency compensation. The TL083 also has offset-voltage null capability. All four devices complement the previously announced TL084 quad op amp. The TL080, 81 and 82 are offered in 8-pin plastic DIPs and TO-99 metal-can packages. The TL083 and TL084 are available in 14-pin plastic DIPs. All units operate over a 0-to-70-C range.

CIRCLE NO. 345

Bipolar 4-k RAMs access in only 100 ns



Fairchild Camera and Instrument Corp., 464 Ellis St., Mountain View, CA 94042. (415) 962-3816. From $24 (100-up); stock.

Available in two versions, the 93481 and 93481A dynamic bipolar RAMs provide 4096 bits of storage and use only a single 5-V supply. The faster version of the new device, the 93481A, has a maximum access time of 100 ns and a 240-ns cycle time. The standard 93481 has a maximum access time of 120 ns and a 280-ns cycle time, both over the range of 0 to 70 C and with a 5-V ±5% supply. Organized as 4096 × 1 bits, all the RAMs consume 350 mW active, 70 mW standby, and 500 mW in page mode. Access and cycle times in the page mode are 75 ns for the 93481 and 65 ns for the 93481A. Provided on the RAM are an independent data latch pin and two chip select pins, as well as seven addresses, ground and power, separate data-in and data-out, write enable, and a single timing control input. The 93481 and 93481A are available in 16-pin ceramic DIPs.

CIRCLE NO. 346

Bipolar PROMs access in only 40 ns

Signetics, 811 E. Arques Ave., Sunnyvale, CA 94086. Ralph Kaplan (408) 739-7700. From $15.50 (100-up); stock.

A 4-k bipolar PROM with an access time of only 40 ns, typical, is organized as 1024 4-bit words. The PROM comes in an 18-pin ceramic DIP and with either open collector outputs (82S136) or three-state outputs (82S137). Both commercial and military temperature range parts are available.

CIRCLE NO. 347

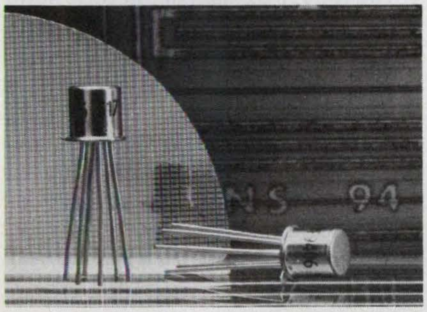
Six-decade counters have BCD preset inputs

Mostek, 1215 W. Crosby Road, Carrollton, TX 75006. Don Ward (214) 242-0444. $6 (100-up); stock.

Designated MK 50398N/399N, a series of PMOS counter circuits housed in 28-pin DIPs features six-decade synchronous up/down counting. Each counter can be preloaded and operate from a single power supply. The six-decade counting stages may be loaded digit-by-digit with parallel BCD input data and have an asynchronous clear function. Multiplex scanning of the decode outputs is controlled by the scan oscillator input, which is self-oscillating or can be driven by an external signal. Input count frequency is dc to 1 MHz. The MK 50398N presents seven-segment output data from the counter contents while the MK 50399N presents BCD output data.

CIRCLE NO. 348

Matched transistor pair has 50 μV differential

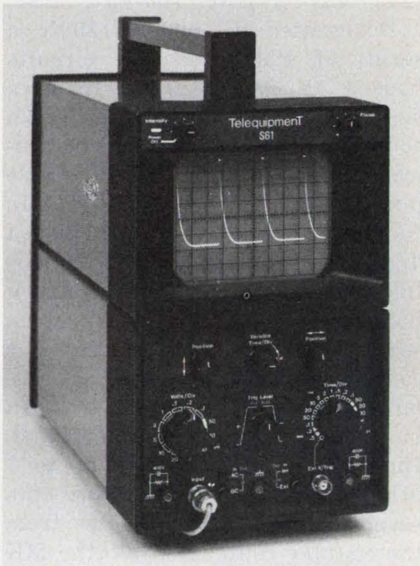


National Semiconductor, 2900 Semiconductor Dr., Santa Clara, CA 95051. Jerry Robertson (408) 737-5000. For the LM194, $14 (100-up); stock.

Matched to within 50 μV of each other, the npn transistors in the monolithic LM194 have a noise figure that is almost unmeasurable —only 1.8 nV/$\sqrt{Hz}$ at 100 μA. The "Supermatched Pair" also has a guaranteed 0.1 μV/°C drift, a common-mode rejection ratio of 124 dB, a minimum current gain of 500 and a current-gain match of 2%. All specifications apply over a collector range of 1 μA to 1 mA. Available in a six lead TO-5 metal can, the transistor pair comes in two operating range versions. The LM194 has a guaranteed range of −55 to +125 C and the LM394 operates over 0 to 70 C.

CIRCLE NO. 349

5-MHz scope enters low-cost market



Tektronix, P.O. Box 500, Beaverton, OR 97077. (503) 644-0161. $375.

The S61 single-trace, 5-MHz Telequipment oscilloscope costs only $375. The S61 is completely solid state (except for the CRT) and fully backed by a one-year warranty. The 6.5-kg (14.3 lb) features a full 8 × 10-cm display. Triggering features include variable level, polarity controls and automatic mode, which free runs in the absence of a trigger signal.

CIRCLE NO. 356

Transient recorder captures waveforms

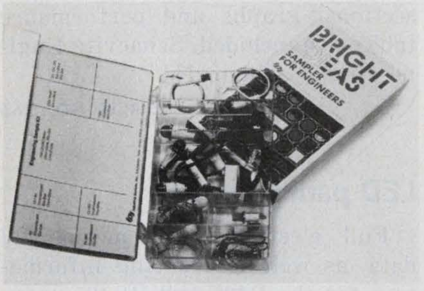
Datalab Inc., 222 Milwaukee, Suite 102, Denver, CO 80206. (303) 321-4601. $1500; 4-6 wks.

Model 901 transient recorder can turn your general scope into a low-cost storage unit, or your X-Y and strip-chart recorder into high-speed graphic devices. The 1024 shift-register MOS memory stores the waveform before and after an event by converting the analog signal into an 8-bit digital value at a 200-kHz rate. In addition to its ±0.5-V analog outputs, the 901 can be controlled from, and has standard RS232/parallel interfaces to, micro and minicomputers allowing use as a front-end for computer-based systems.

CIRCLE NO. 357

COMPONENTS

Indicator-light kit contains 24 units



Industrial Devices, 7 Hudson Ave., Edgewater, NJ 07020. (201) 224-4700. $10 (unit qty); stock.

An indicator-light sampler kit for engineers and designers contains working samples of a large variety of IDI indicator lights for breadboarding or building working prototypes. The kit consists of 24 complete indicator and pilot lights, all different. There are 16 different styles in seven colors for five operating voltages from 6 to 250 V. The units have five different mounting-hole sizes. Included are incandescent, neon and solid-state LED units with both wire-lead and solder-terminal types.

CIRCLE NO. 358

Thumbwheel switch only 8-mm thin

EECO, 1441 E. Chestnut Ave., Santa Ana, CA 92701. (714) 835-6000. $2 (1000 up); 6 wks.

EECO 1800 series thumbwheel switches feature extra-slim 8-mm-wide switch modules and switch assemblies that can be snapped into panels without tools or screw holes. Across-the-room legibility is available with 0.234-in. high characters. The switches are available in a number of 10-position codes including BCD, BCD with complement, BCD complement only, decimal and repeatings. Options include direct-wire or connector termination, gloss or matte finish, decimal points, custom dial markings, stops and diode provision. Contacts are gold-plated, the housing is self-extinguishing nylon and the circuit board is flame-resistant glass epoxy. Operating temperature range is −20 to 65 C. Initial contact resistance is 0.1 Ω max.

CIRCLE NO. 359

4-digit-LCD displays multiplexed inputs

UCE Inc., 20 N. Main, Norwalk, CT 06854. (203) 838-7509. $13 (1000 qty); stock to 6 wk.

In the Model 3624, the inputs to this four-digit liquid-crystal display are multiplexed. Characters in the unit are a variation of standard digits with heights of 0.5 in. Each digit is electrically isolated with separate backplanes to allow sequential seven-segment-digit driving. Generally, four digits are considered the crossover point in terms of parts count in multiplex vs latch drive. A latched option of the instrument, the 4LDD-7, offers drive and display and accepts either BCD or pulse-counting inputs.

CIRCLE NO. 360

Magnetic contact feels vibrations

Mountain West Alarm Supply, P.O. Box 10780, Phoenix, AZ 85064. (602) 263-8831. $2.50; stock.

Although the S9 Magna-Vibe is basically a sensitive magnetic contact for use in closed-circuit burglar-alarm systems, it can be easily converted to also act as a vibration detector by simply adding a supplied sensitivity adjustment screw. Its four sets of contact surfaces scrub and polish themselves during each opening and closing. The one simple moving part has been estimated to have an almost limitless life even if operated thousands of times a day. Heavy-duty contacts are designed for very low resistance, no pitting or oxidation.

CIRCLE NO. 361

New Literature

TV controllers

Physical and electrical characteristics of video-random-access-memory (VRAM) TV controllers are given in a catalog. Matrox Electronic Systems, Montreal, Quebec H36 3N5.

CIRCLE NO. 362

Digital displays

Digital measurement and display devices for use with microwave antenna measurement systems are described in a 32-page catalog. Scientific-Atlanta, Atlanta, GA

CIRCLE NO. 363

Pressure transducers

Applications and specifications for the Model SA-E soil and Model SA-P pore pressure transducers are described in an illustrated two-page data sheet. Sensotec, Columbus, OH

CIRCLE NO. 364

Hardware components

General specifications and finishes of electronic hardware components, drawings, and tabulations indicating sizes, lengths, diameters, etc., are contained in a 60-page booklet. Accurate Screw Machine, Nutley, NJ

CIRCLE NO. 365

Transducers

A 24-page catalog and selection guide for linear and angular displacement transducers covers the theory of the LVDT. Cut-away sections, graphs and performance tables are included. Schaevitz Engineering, Camden, NJ

CIRCLE NO. 366

LED panel lamps

Full electrical and mechanical data, as well as ordering information for the P405 and PR405 snap-in LED panel lamps, are provided in a data sheet. Data Display Products, Los Angeles, CA

CIRCLE NO. 367

Hybrid support capability

Technical background information on the design, manufacture and QA aspects of the company's products for military and aerospace programs are given in a 12-page brochure. Amperex Electronic, Slatersville, RI

CIRCLE NO. 368

Rf/audio connectors

A right-angle rf/audio connector, which offers quick connect/disconnect for coaxial cables and twin leads, is featured in a two-page catalog. Connector Corp., Chicago, IL

CIRCLE NO. 369

Computers

"Computers in Engineering" discusses the use of computers in various fields of technical analysis and design and their value in data-acquisition, reduction and processing. Digital Equipment, Communication Services, Northboro, MA

CIRCLE NO. 370

Wire

"A World of Wire" describes various products available for both precision electrical-conductor and electromechanical applications. Production, QC, customer-engineering assistance and R&D capabilities are shown. International Wire Products, Wyckoff, NJ

CIRCLE NO. 371

Switches

Eighty-four pages cover the company's snap-action, contact, selector, rotary, thumbwheel and lever-wheel switches as well as keyboards and keyboard switches. Also included is a price list. Cherry Electrical Products, Waukegan, IL

CIRCLE NO. 372

Connectors

Technical data on the company's RAPMATE 354 series connectors are featured in a four-page folder. Malco, Montgomeryville, PA

CIRCLE NO. 373

PROM programmers

Features, specifications and ordering information for a portable PROM programmer can be found in a two-page data sheet. PROM Programmers, Mountain View, CA

CIRCLE NO. 374

Rf instruments

A 62-page catalog features instruments for rf power measurement. Bird Electronic, Cleveland (Solon), OH

CIRCLE NO. 375

Connectors, terminal strips

Blade-contact rack-and-panel connectors and barrier terminal strips are featured in a four-page bulletin. Beau Products Div., Laconia, NH

CIRCLE NO. 376

Components

Fully described and illustrated in a catalog's 164 easy-to-read pages are over 4500 practical products. Edmund Scientific, Barrington, NJ

CIRCLE NO. 377

Strip-chart recorders

A 32-page Rustrak strip-chart recorder catalog includes data on a miniature 24-channel event recorder, a miniature three-channel analog recorder and a line of 4-in. servo recorders for OEM and laboratory use. Measurement & Control Systems Div., Gulton Industries, East Greenwich, RI

CIRCLE NO. 378

Cooling systems

A 20-page illustrated catalog covers cooling systems. A product/specification cross-reference is included. Zero Corp., Burbank, CA

CIRCLE NO. 379

Beryllia packages

"Cermatrol Products," an illustrated 24-page handbook, covers beryllia components and includes 38 engineering drawings of tooled microelectronic packages. National Beryllia, Haskell, NJ

CIRCLE NO. 380

Data-acquisition systems

The Digitem System 2000, a new family of data-acquisition systems, is described in an eight-page brochure. FX Systems, Kingston, NY

CIRCLE NO. 381

Design Aids

Solar radiation chart

A wall chart shows world-wide annual solar radiation in kJ/cm^2. Sensor Technology.

CIRCLE NO. 382

Rectifier cross-reference

A cross-reference on full-wave, single-phase bridge-rectifier circuits from 1.8 to 30 A lists over 250 part numbers by manufacturer, along with the corresponding IR replacement. International Rectifier.

CIRCLE NO. 383

Zener diodes

Low, medium and high-powered zeners as well as JEDEC series and transient absorption (TAZ), voltage-reference and chip zeners are shown in a wall chart. Siemens.

CIRCLE NO. 384

Epoxies

Major properties and uses of more than 50 specially formulated epoxy and related compounds are covered in a four-page product selector. Techform Laboratories.

CIRCLE NO. 385

Digitizing equipment

A pocket-sized folder provides a capsule review of digitizing equipment and capabilities and presents definitions for common digitizer terms. Science Accessories Corp.

CIRCLE NO. 386

Standoffs and spacers

Standardized standoffs and spacers are featured in a wall chart. Keystone Electronics.

CIRCLE NO. 387

Programmable memory

A comparison chart shows currently available PROMs and FPLAs. The chart includes a user guide. Data I/O.

CIRCLE NO. 388

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quick ads

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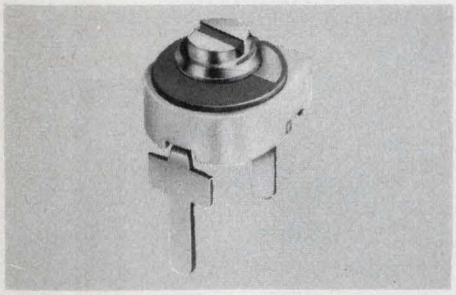

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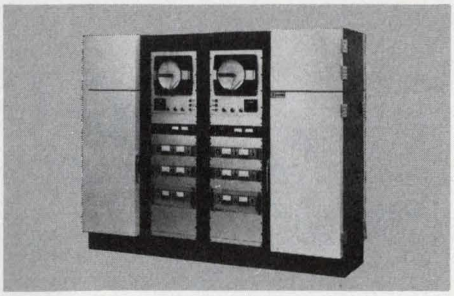
TRIMMER CAPACITORS 251



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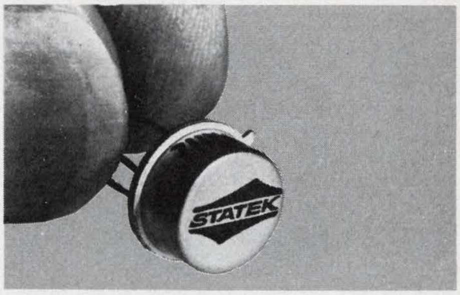

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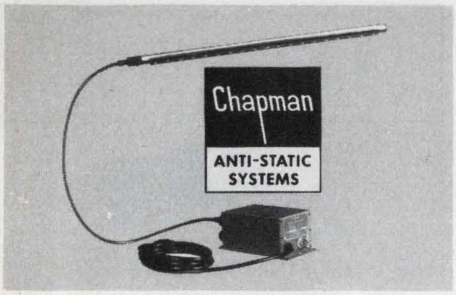
QUARTZ CRYSTALS 257



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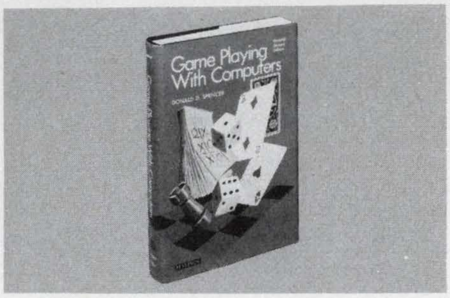

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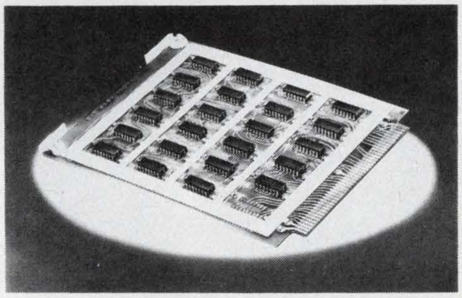

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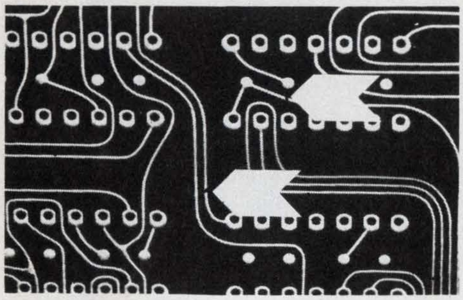

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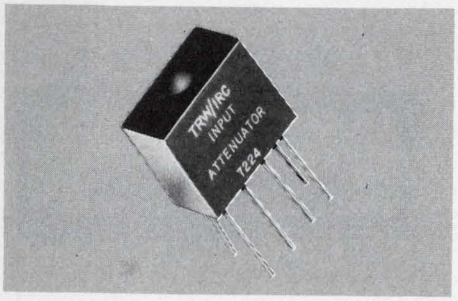

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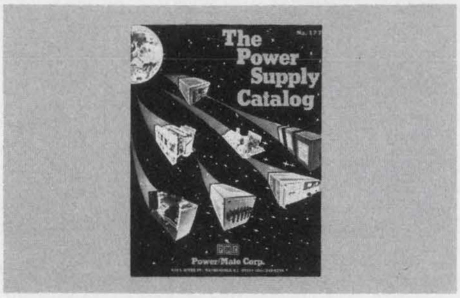

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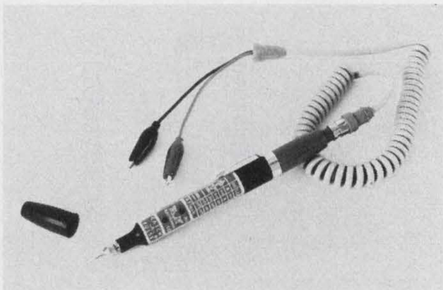

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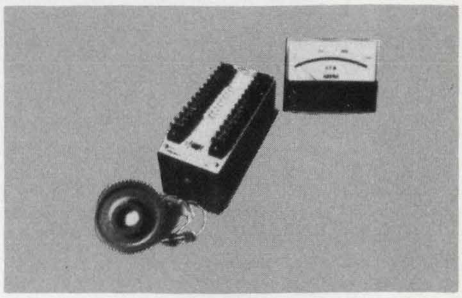

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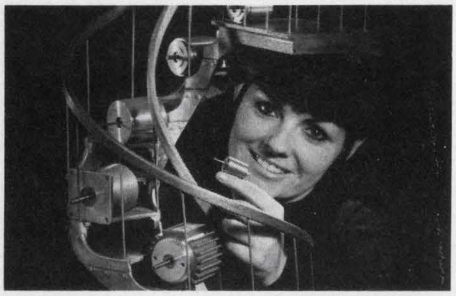

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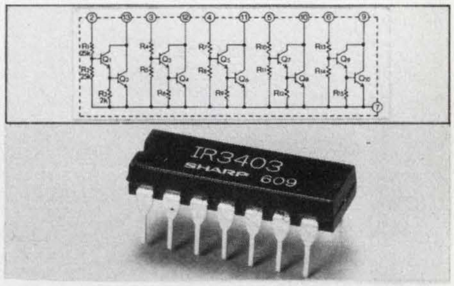

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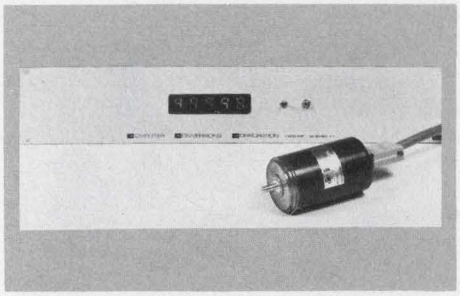

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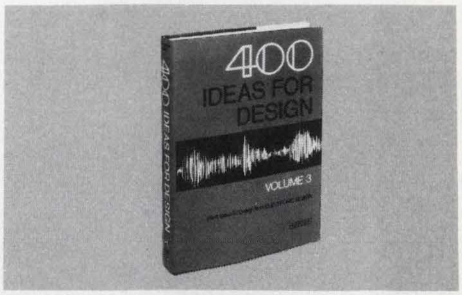

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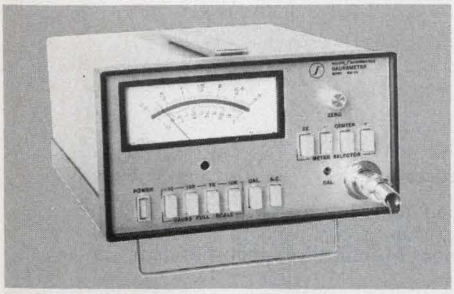

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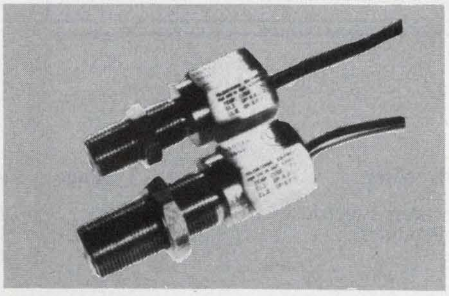

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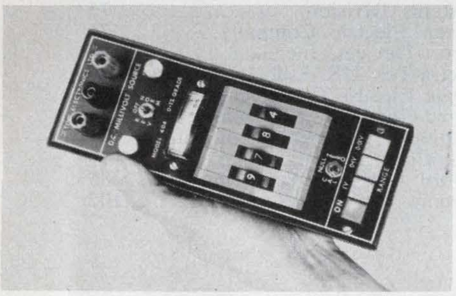

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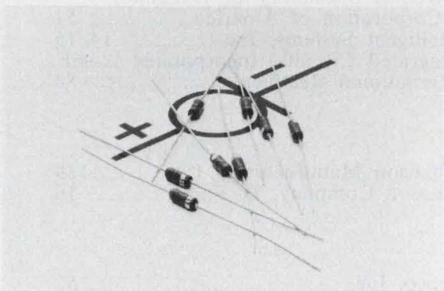

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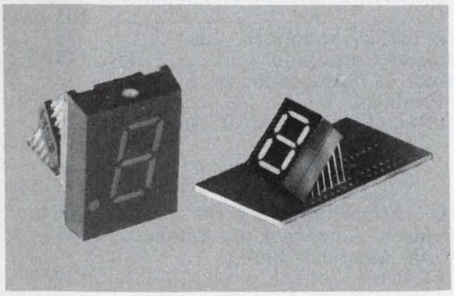

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Product Index

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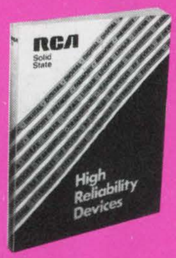

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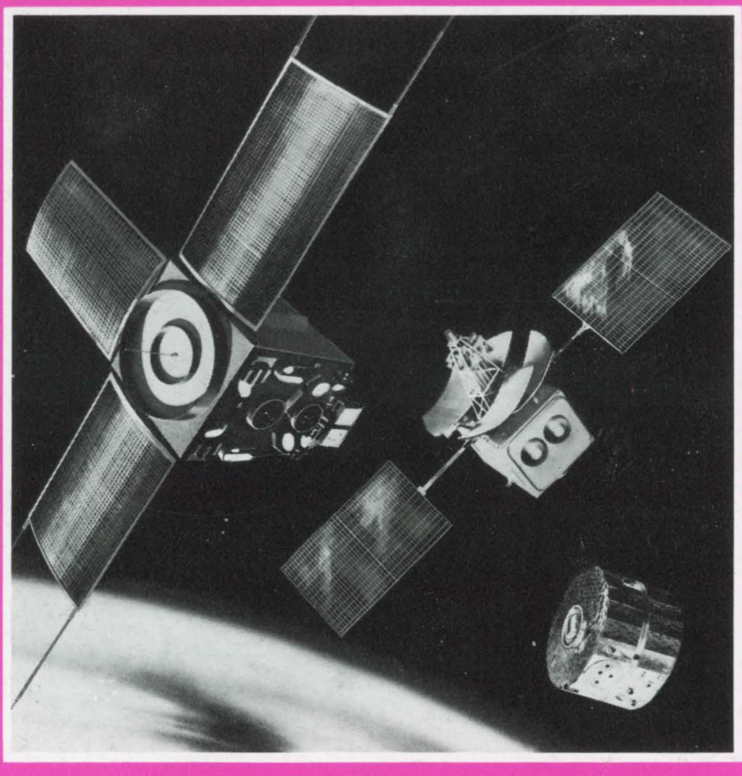
Satellite	OSCAR-6	ITOS Series D; F; G; H	Atmospheric Explorer Series C; D; E	SATCOM Series F1; F2
Time in orbit (mo.)	32	85.5	49.5	16.5
Number of COS/MOS devices	90	168	7,200	1,652
Device-hours	2,073,600	2,585,520	85,536,000	9,812,880
Number of failures	0	0	0	0
Failure rate (%/1000 hours)	0.045	0.035	0.001	0.0092
MTTF (hours)	2,360,000	29,000,000	96,000,000	10,750,000

Total device hours: 100,000,000 (Data at 60% confidence, usage thru Nov. 1, 1976)

Failure rate: 0.00092%/1000 hrs. MTTF: 108,000,000 hrs.



Write: RCA Solid State. Box 3200, Somerville, NJ 08876; Sunbury-on-Thames, Middlesex TW16 7HW, England; Ste.-Anne-de-Bellevue, Quebec, Canada; Fuji Bldg., Tokyo, Japan.

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