EDN®

PROCESSOR UPDATES PG 107

A CAHNERS PUBLICATION

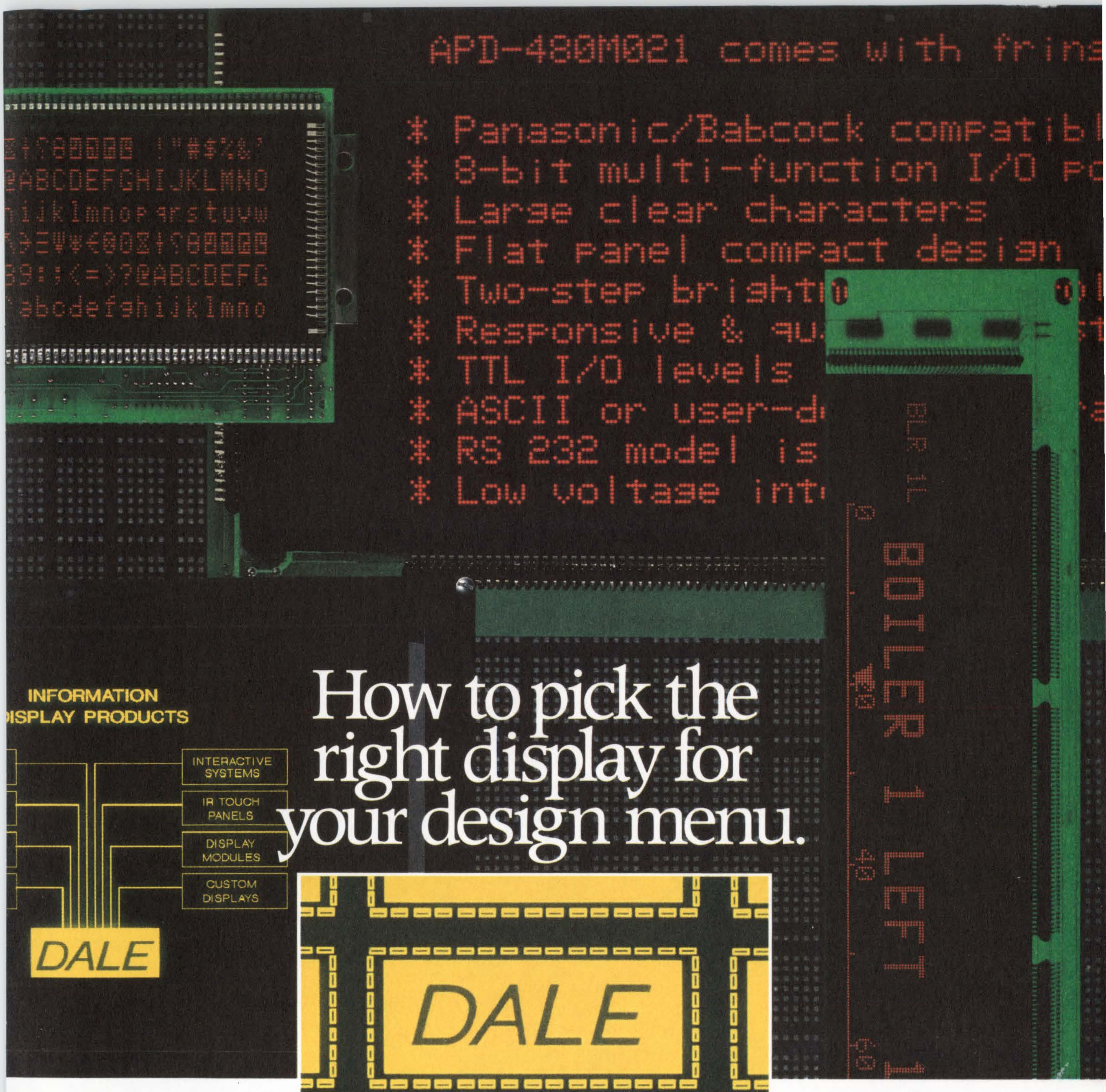
April 23, 1992

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS WORLDWIDE

ecial Report

Pen computers: new electronic tools for the workplace pg 136


LabWindows
LabWindows
LabWindows Instrumentation System
TRG
Signal
Source
Signal Spectrum



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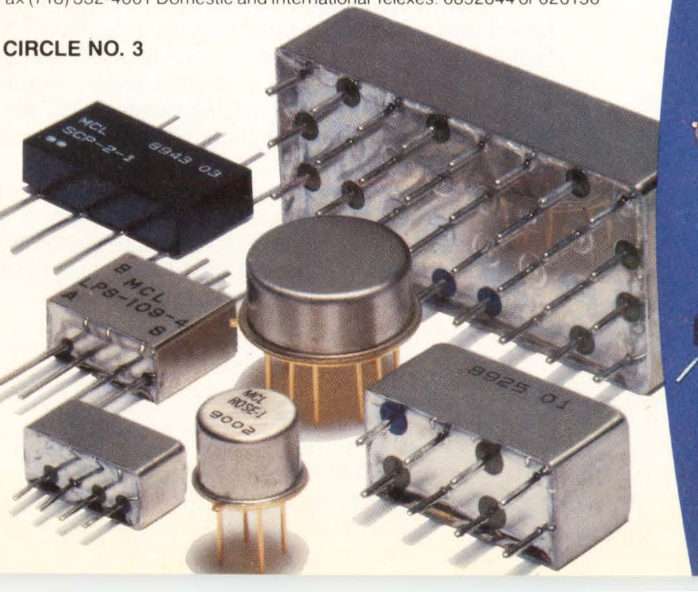


F134-1 REV. ORIG.

EDN

MAGAZINE EDITION

APRIL 23, 1992 VOLUME 37, NUMBER 9

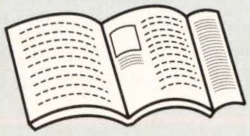
ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS WORLDWIDE

On the cover: Whether users are on a construction site or business appointment, pen-based computers can go along. (Photo courtesy NCR). . . . **PAGE 136**

Continued on page 7

Foldout contents

Turn to the last information-retrieval service card in the back of this magazine and you'll find a foldout table of contents. Now, instead of flipping back and forth from this table of contents to the articles you want to read, you can have the convenient foldout open at all times while you're reading EDN. Use the foldout contents to mark off articles you'd like your colleagues to read or to remind yourself to copy stories for your files.



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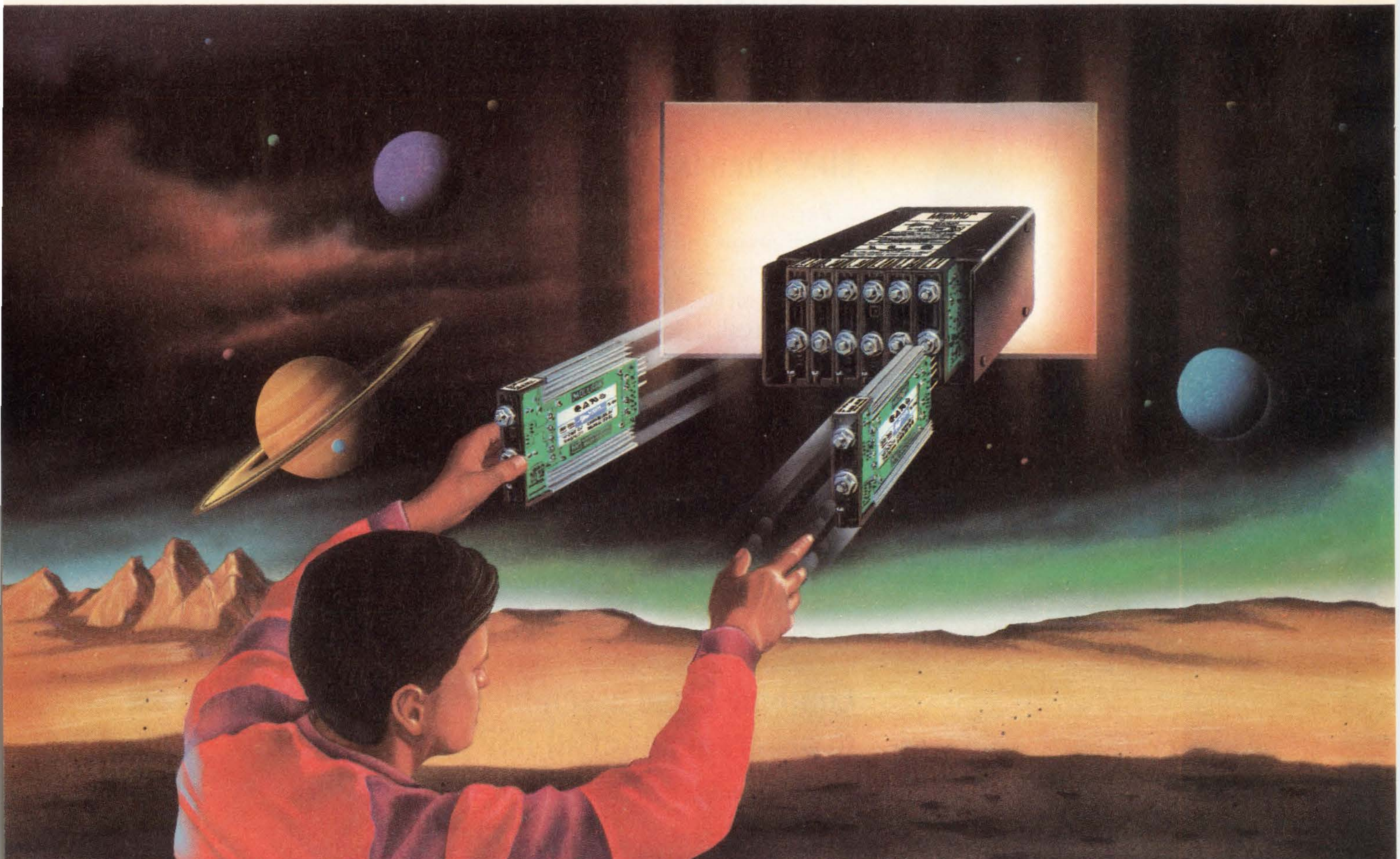
POWER To Configure



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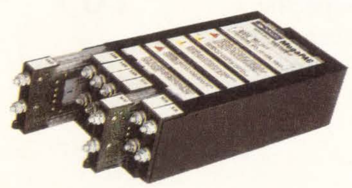

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Component Solutions For Your Power System

CIRCLE NO. 5

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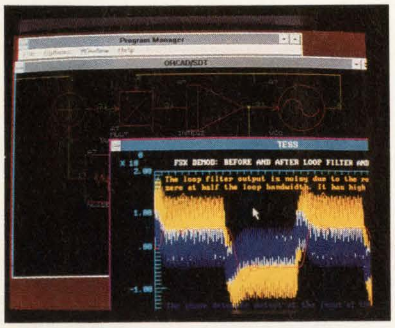
MAGAZINE EDITION

APRIL 23, 1992

Continued from page 5



With easy-to-use commands and block-diagram formats, control-system simulation software lets you sidestep writing a lot of program code and makes it easy to modify your model until you get it right. . . . . **PAGE 79**

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Express Request

TECHNOLOGY UPDATES

PRODUCT UPDATES

PROCESSOR UPDATES

Continued on page 9

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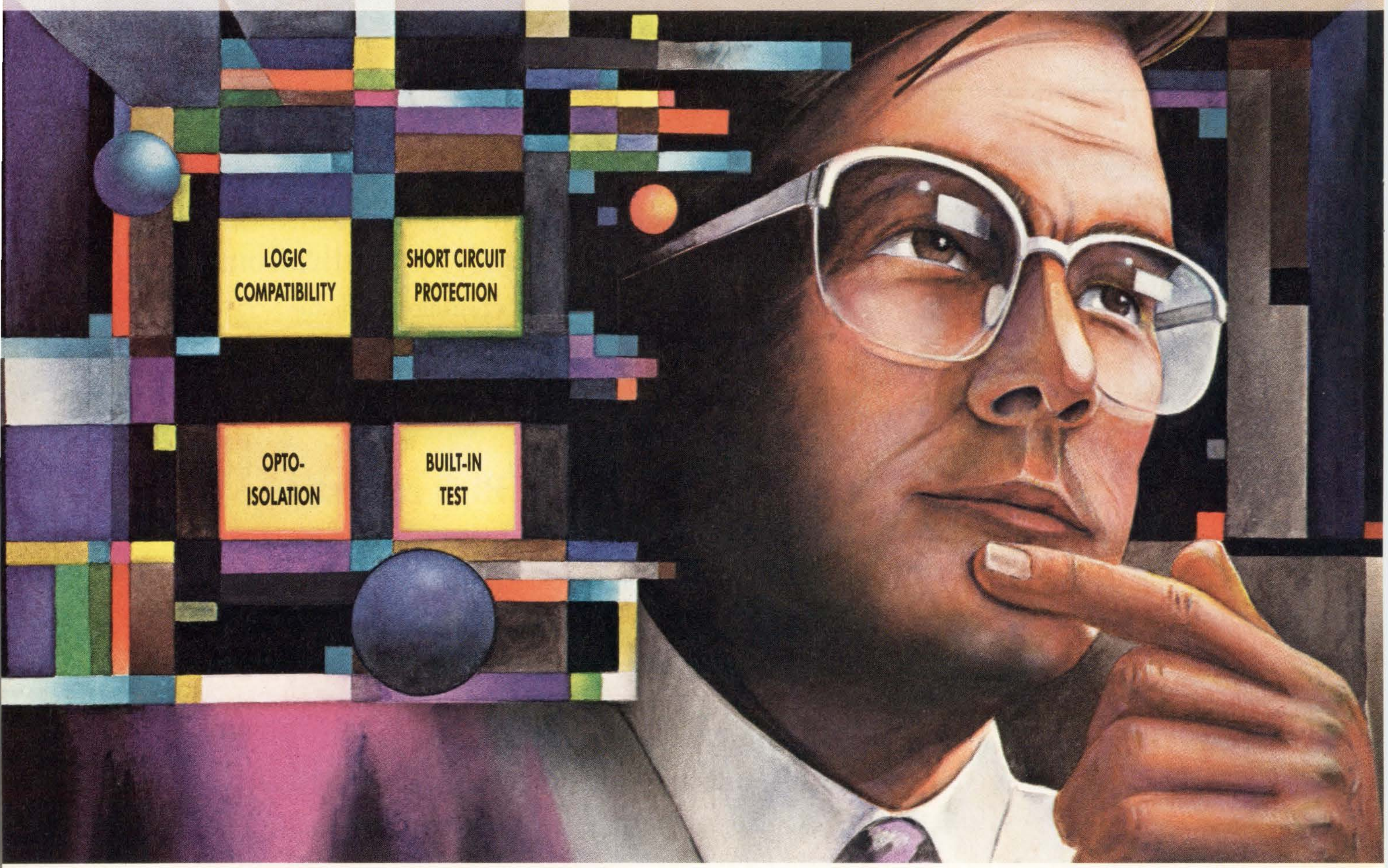
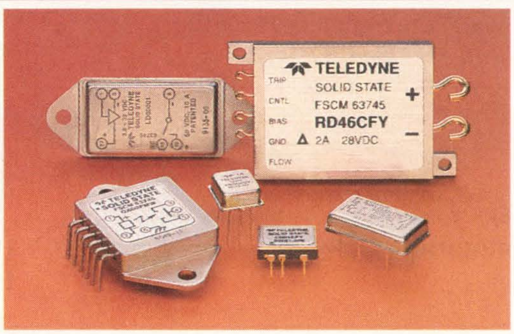
WHY RE-INVENT THE WHEEL?





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CIRCLE NO. 6

EDN
MAGAZINE EDITION

APRIL 23, 1992

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EDITORIAL

Don't blame the kids

PROFESSIONAL ISSUES

Managing stress for success

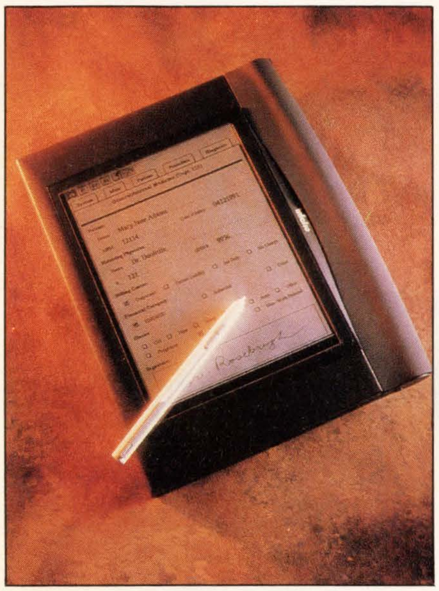
NEW PRODUCTS

DEPARTMENTS

INSIDE EDN

A summary and analysis of articles in this issue

Small computers, the components they comprise, and nonintuitive uses for all of these products constitute this issue's focus. Senior Technical Editor Gary Legg takes the holistic approach in his Special Report on pen-based computing by discussing entire computers. These small machines and their unique user interfaces may open many new computing markets.



As Gary writes, the intuitive appeal of pen-based computing is undeniable. People are used to writing on a surface with a pen. What's new is that the surface responds when it's part of a pen-based computer. How well the surface responds is another matter entirely. For a close look at the technology behind the response—handwriting recognition—see the Special Report's sidebar.

In addition to the pen interface, Gary also investigates the possible uses for lightweight, battery-powered, portable computers and postulates just how pervasive this technology might become.

Liquid-crystal displays are a key component of pen-based computers and are the topic of Technical Editor Dave Pryce's Technology Update. In his overview, Dave looks at both active- and passive-matrix displays and investigates the advantages and disadvantages of both technologies.

Another key component of small computers is the disk drives used for mass storage. Each drive contains at least one small motor, and each motor requires a controller. The latter is the topic of Technical Editor J D Mosley's Technology Update. In particular, she reviews sensorless motor-control ICs. Sensorless motor control reduces costs and improves reliability by eliminating sensors from the motor assembly. However, these chips impose certain conditions on the motor start-up sequence, as J D discusses in her report. You'll find several suggested methods for satisfying these conditions in the article.

Last but certainly not least, this issue contains the second and last installment of Technical Editor Doug Conner's month-long hands-on FPGA series. In this article, Doug discusses his experiences with FPGA design verification and simulation. He also discusses how this project has transformed him from a skeptic into a firm believer in the benefits of simulation.

Steven H Leibson
Executive Editor

Soon, Eight Ho
Computing Will

(actual size)

AMD Introduces The World's First 386 Microprocessor With 3-Volt Technology.

Two standard dry-cell batteries. There's really nothing special about them. Aside from the fact that they can run a powerful, portable 386 computer for a full eight hours. Provided, of course, that portable is built around a low-voltage Am386™ microprocessor.

The 25MHz DXLV and the 25MHz SXLV are available in PQFP packaging.

Thanks to the low-voltage Am386 microprocessors, laptop, palmtop and notebook computer designs will become smaller, lighter, and more powerful than ever before.

With battery life of up to eight hours or more. That's a full day's worth of 386 performance—the per-

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formance you need to run sophisticated applications like Windows™ 3.0.

And rest assured, the low-voltage Am386 microprocessors are proven compatible and comply fully with JEDEC standards for low-power, 3-volt computing. We can even supply you with the 3-volt EPROMs your systems will need. Other 3-volt system logic is also readily available.

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CIRCLE NO. 8

HOW ENGINEERING SEES OUR NEW 32-BIT INTEGRATED PROCESSOR.

Actually, a bullet doesn't do it justice. But you get the picture. Motorola's new 68330 integrated microprocessor is fast.

And well it should be. After all, it gets its firepower from a 68020-based core processor that's optimized to run on a 16-bit data bus. So you get 32-bit microprocessor performance with the economy of a 16-bit memory system.

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68000 CPUs Architectural Integration	000	020	030	040
68EC000 EMBEDDED Performance/Cost	EC000	EC020	EC030	EC040
68300 INTEGRATED Functional Integration	302	330	331	332	340

Motorola's 68000 families let you choose the performance and integration that's right for your application.

As the simplest and lowest priced member of the 68300 family, the '330 is an ideal companion to your favorite peripheral circuits. Even if you've already combined them into an ASIC or custom circuit.

What's more, the 68330's Systems Integration Module comes already loaded with system glue logic. Saving you the trouble of designing in functions like clock

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HOW PURCHASING SEES IT.

generation, chip selects and interrupt control.

And, since the '330 is fully binary software compatible with all members of the 68000 and 68300 families, it provides a seamless migration path, reams of reusable code, popular operating systems and familiar development tools.

All of which can save you a lot of trouble, while lowering overall system costs and raising your accountants' morale.

So if you're looking for 32-bit performance at a 16-bit system price, call 1-800-845-MOTO. Ask for a free 68330 product sample,* and discover a high-caliber value.

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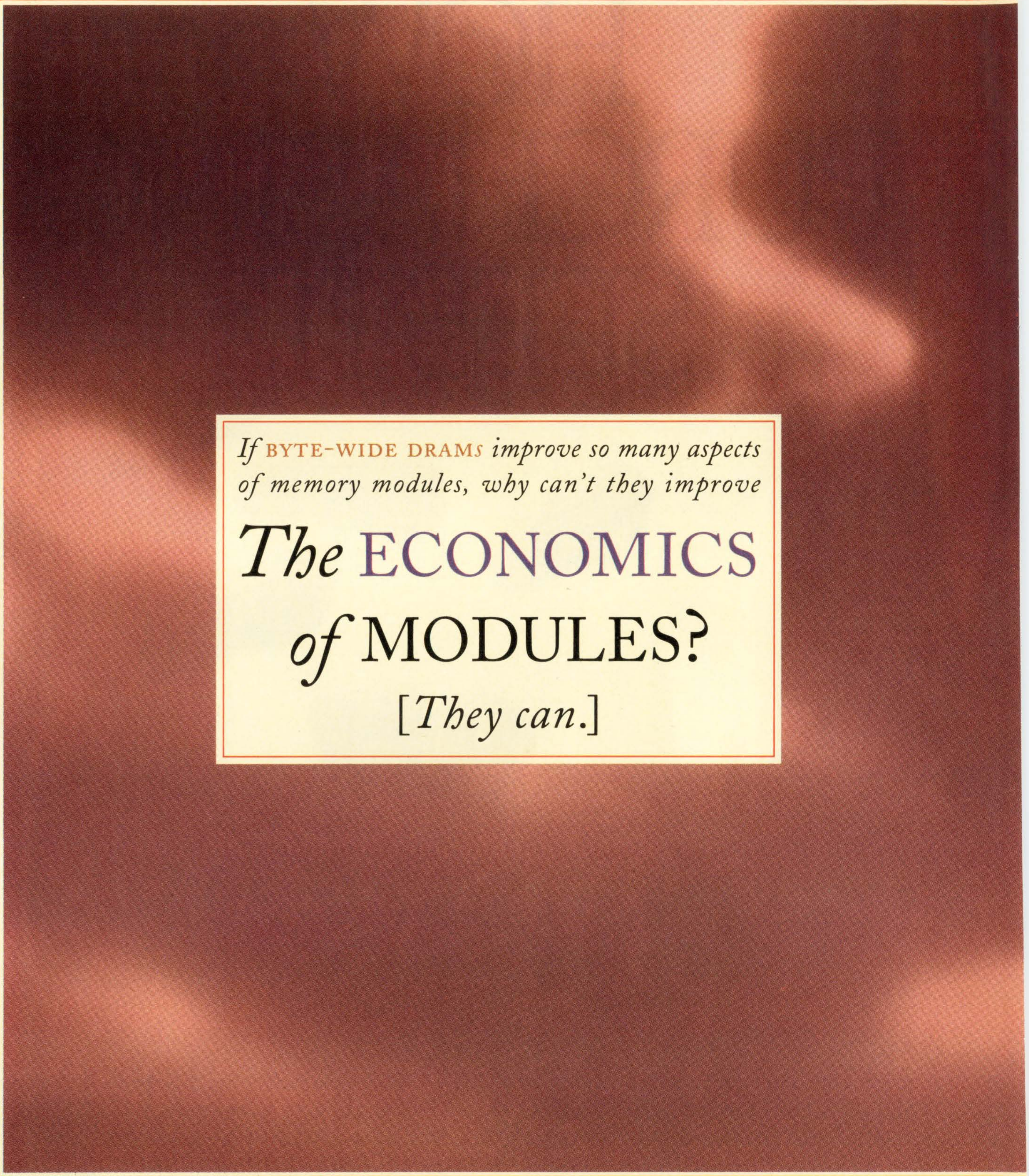


Byte-wide DRAMs in memory modules. When you compare a 4-meg byte-wide with the normal combination of 1-megs and 256K's, you find that one chip can replace six.

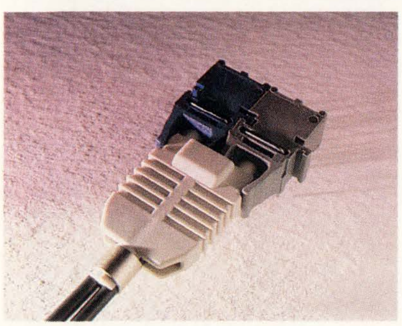
Now that in itself sounds pretty good. And it gives you lots of design advantages.

Far lower use of board real estate. Greater reliability. And —what's critical for laptops—far lower power consumption.

But now byte-wides also give you an advantage in *cost*—on x36 modules like the 256Kx36 and 512Kx36.

Because the single byte-wide costs less than the six chips it replaces.

HP's 50 MBd Plastic Fiber-Optic Data Links. Anything else would be twisted.



Our new data links are so fast and cost-effective, it would be crazy to stick with twisted pair.

Sure, optical fiber is immune to noise, but who can afford it? With HP's new high-speed plastic fiber links, the answer is anyone.

That's because our new links rely on plastic optical fiber cable which keeps costs way below glass fiber, while offering far greater voltage isolation and noise immunity than twisted pair wire.

A quick turn for the best.

With data rates soaring to 50 MBd, HP's plastic fiber links offer the fastest solution for designing computer, telecommunications, or industrial applications. So you can avoid bottlenecks, and design in data multiplexing.

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You can choose interlocking horizontal or vertical mounts for greater mechanical design flexibility. The analog in/out provides the electrical design flexibility you need to meet your cost and performance goals.

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CIRCLE NO. 17

EDITED BY SUSAN ROSE

Merger promises big signal-processing boost

Comlinear Corp and Electronic Decisions Inc have merged with the intent of bringing a new signal-processing technology called acoustic charge transport (ACT) to market. The resulting company keeps the Comlinear name. Electronic Decisions has spent nine years developing the ACT technology, mostly for military applications. ACT uses traveling acoustic waves in GaAs material to move charge packets across a chip's surface. Each packet contains an analog-signal sample so the ACT device spreads time-separated samples in space and effectively creates an analog sampling delay line or shift register. ACT is not a digital technology. Instead, it uses analog sampling that has a dynamic range of approximately 80 dB and introduces no sampling noise.

Electrode taps placed down the length of the ACT device can measure these spatially separated samples without disturbing them. The resulting readings combine through programmable attenuators to produce a weighted output. The net result is a programmable transversal or convolving filter with bandwidths that range from 150 to more than 500 MHz. Electronic Decisions has operated prototype 128-tap ACT devices at sample rates ranging from several hundred MHz to more than 1 GHz. A DSP system performing the same function would have to perform roughly 50 billion operations/sec to perform comparable signal processing.

This technology has already proven useful for very-high-speed, signal-processing applications beyond the reach of DSP, but the company also plans to drive the cost of ACT devices down for use in high-volume applications. For now, only an $8500 development kit is available. The first commercial parts will appear later this year. Comlinear Corp, Fort Collins, CO, (303) 225-7435, FAX (303) 226-0564.—Steven H Leibson

Software demystifies system needs

If you have a specific data-acquisition application but aren't sure how to implement it, your computer can now give you that information. A free interactive program called DAQ Designer questions you about your application's analog and digital signals, the type and number of sensors, and any signal-conditioning requirements. The program then analyzes your answers and recommends specific plug-in, data-acquisition boards, signal-conditioning products, cable assemblies, and software packages that will suit your application. The program requires a computer running DOS 3.0 or higher with a minimum 80286 µP, at least 640 kbytes of RAM, and a VGA monitor. National Instruments, Austin, TX, (800) 433-3488; (512) 794-0100. Contact Jerry Roddiguez.

—J D Mosley

DSP boards pack unusual I/O ability

Even though DSP coprocessor boards for the 16-bit ISA bus are common, the DT3801 series of TMS-320C40-based boards are noteworthy. These boards use all of the 320C40's I/O facilities: six communications ports and a 6-channel DMA. The units also include large amounts of memory. As a result, the boards can perform many I/O operations simultaneously and with little impact on the host PC.

The DT3809, which has a 12-bit ADC, takes 1 Msample/sec on one channel, 800 ksamples/sec on 16 single-ended or eight differential channels at unity gain, or 320 ksamples/sec on its multiple channels at software-selectable gains of 2, 4, and 8. The DT-3808, which has an 8-channel simultaneous S/H capability, makes 160,000 16-bit A/D conversions/sec. The boards also include two 200k-point/sec, 16-bit DACs and have 4 Mbytes of dynamic RAM, 512 kbytes of static RAM (SRAM), 256 bytes of non-volatile SRAM, and 8 kbytes of configuration RAM. The volatile memory is organized in 32-bit words. The board design allows adding still more memory on daughter boards or additional ISA bus boards.

Prices range from $7195 to $7595. A developers' software kit costs $2995, and an emulator for the DSP µP costs $8000. Data Translation Inc, Marlboro, MA, (508) 481-3700.

—Dan Strassberg

Software converts FPGAs to ASICs

If you design with programmable logic from Actel, Altera, or Xilinx, you can use Gould AMI's Netrans software to convert your design to a masked gate array. The software provides the netlist translation from the FPGA to the company's netlist format, including libraries, design syntax, and test-vector conversions. The company's design-optimization tools also analyze your design for potential ASIC design flaws and ensure test-vector compatibility with the company's in-house production testers. The software runs on Sun-4 workstations with CAE software from Cadence, Dazix, Mentor Graphics, and Viewlogic. The cost is $15,000 for support of one FPGA vendor and $5000 to add additional FPGA vendors. Gould AMI, Pocatello, ID, (208) 233-4690.—Doug Conner

Low-power 486 chip fits 386SL sockets

You can drop 486 power into 386SXL sockets to boost processing power for laptops and other low-power applications with Cyrix Corp's Cx486SLC. The device is the first 3V, 25-MHz, 486-compatible μP. It lets users or vendors upgrade their systems by substituting an existing 386SL with the chip. According to the company's benchmarks, the μP is 2.5 times faster than 386SX-25 and 386SL-25 chips, delivering a Landmark (version 2) rating of 78 MHz. The company also claims it is 1.7 times faster than the IBM 386SLC chip.

The μP is code compatible with the 486. However, it is not a copy of the 486 design. It supports a 1-kbyte unified cache (2-way set associative), rather than the 8 kbytes of the 486's unified cache. The chip has a 16-bit external memory bus, instead of the 486's 32-bit bus. Additionally, the Cyrix part has a 16-bit multiply that supports 386 graphics applications, such as Pen-based systems. Operating at 5V, chip power dissipation is typically 2W. That figure drops to less than 0.5W when operating between 2.7 and 3.3V.

The company is developing other versions of the 486 to replace the 386. Expected are faster 16-bit versions, including 33- and 40-MHz parts. The μP comes in a 100-lead quad flatpack. Initial pricing is $119 (1000); sample qty available. Cyrix Corp, Richardson, TX, (214) 234-8387, FAX (214) 699-9857.—Ray Weiss

Try your ASIC before you buy it

If you know from the start you need a mask-programmed ASIC, not a field-programmable gate array (FPGA), you probably don't want to go through the task of designing an FPGA and then later translating the design to an ASIC. But an FPGA lets you validate your design before you risk time and money on a gate array. Now you can have it both ways.

Gould AMI's Netransplus service takes an ASIC design and translates it into an FPGA so you can validate the design quickly and inexpensively before committing to the ASIC's nonrecurring engineering costs. The difference in going from an ASIC to an FPGA instead of the other way around is significant: You design to take advantage of the ASIC structure, not the FPGA. You'll avoid design inefficiencies that sometimes occur in an FPGA to ASIC conversion. The FPGA may sacrifice some performance because the design isn't optimized for it, but the ASIC will have superior performance and reach completion faster than translating from an FPGA.

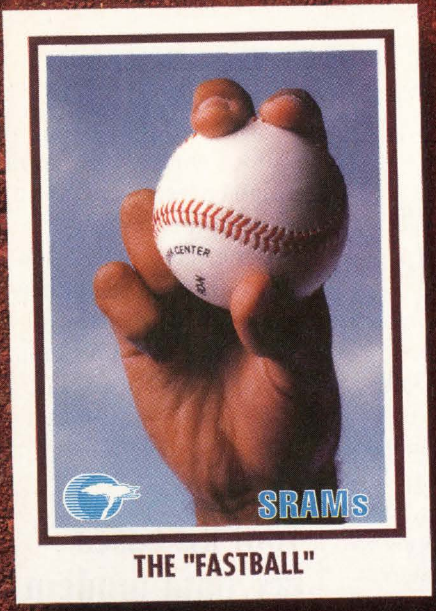
The company translates the netlist typically in two days and ships it back to the customer for FPGA prototyping and testing. As soon as the design has been verified by the customer, ASIC samples are available in an average of three weeks. Initially, the software will convert into Actel FPGAs. Translation for a 1000- to 2000-gate design costs $4000. Gould AMI, Pocatello, ID, (208) 233-4690.—Doug Conner

12-bit, fast monolithic ADCs arrive

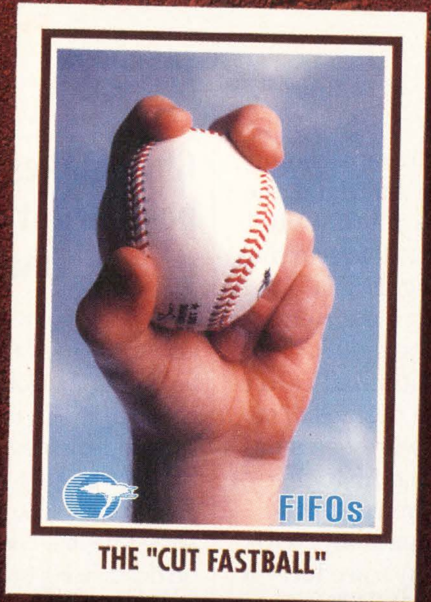
The SPT7912 from Signal Processing Technologies is the first monolithic 12-bit A/D converter capable of sampling 30 Msamples/sec. As a result, a 500-kHz input results in a S/N ratio of 67 dB. The converter also includes on-chip track-and-hold circuitry. At $250 (100), this IC's price is significantly less than that of comparable hybrid and board-level converters, which sell for $500 to $1000. The chip also comes in a 10-Msample/sec version, the SPT7910, which sells for $150 (100). Both chips include ECL-and TTL-compatible versions and power dissipation under 1.4W. These ICs suit high-resolution, high sample-rate applications such as digital communications, radar receivers, biomedical electronics, portable instruments, and professional video equipment. Signal Processing Technologies, Colorado Springs, CO, (719) 540-3999, FAX (719) 540-3970.—J D Mosley

IGBT announcements follow settlement

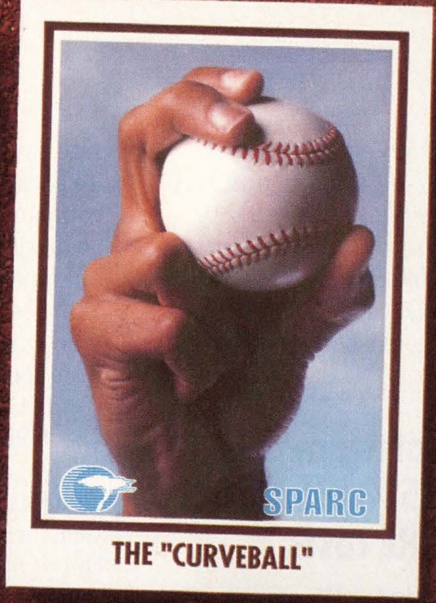
Now that a patent infringement suit with International Rectifier Corp (El Segundo, CA) is settled, Harris Semiconductor is adding new types of IGBTs (insulated-gate bipolar transistors) to its existing line. Six of the devices have built-in antiparallel rectifier diodes, breakdown ratings from 400 to 600V, and can carry collector currents from 6 to 24A at 90°C. The built-in rectifier of these devices is a very fast recovery type, which has a reverse-recovery time of 60 nsec at the device's rated collector current. Prices for the devices range from $8.89 for the HGTG24N60D1D, which is a 24A/600V device with a 96A peak current rating, to $1.49 for the HGTP6N50E1D, a 6A/500V device. Characterization data, which includes maximum operating frequency for a range of current and switching losses, is available for all six IGBTs. Three additional IGBTs are rated for higher continuous-current/breakdown-voltage combinations of 34A/



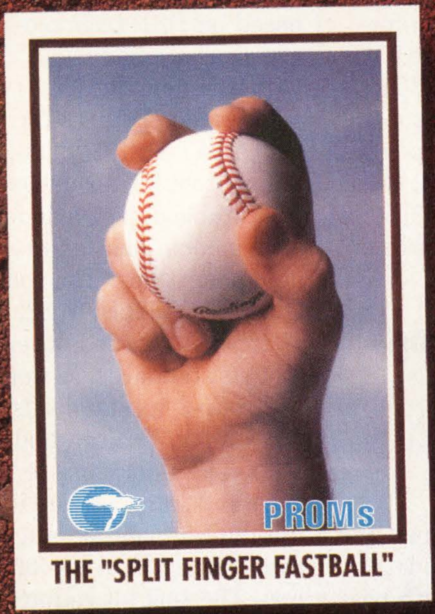
Scorching access times and a wide range of densities make our SRAMs untouchable. 12 ns 256Ks, 8 ns 64Ks, 4 ns 16Ks and more.



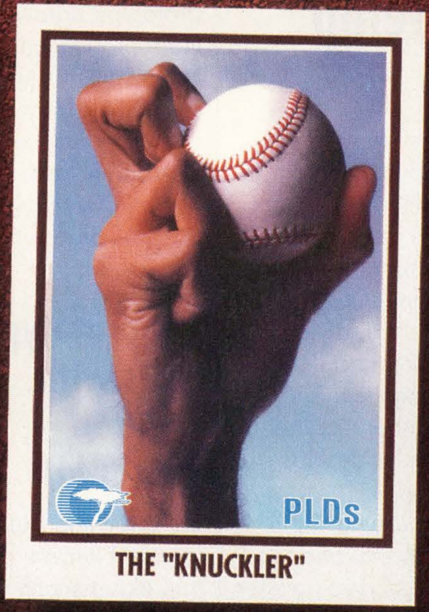
At 70 MHz, with read/write clocks and synchronous flag features, our FIFOs and Bi-FIFOs move data in and out quickly.



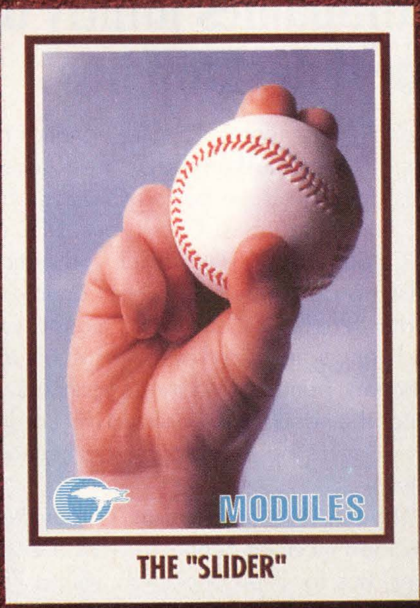
Let 'em just try to keep up with the hottest SPARC multiprocessing concept going.



The fastest access in every PROM density. Broad options make these hard to beat.

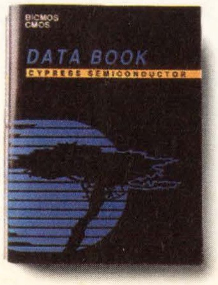


PLDs allow crafty designers to mix Gate Array density with 40 MHz performance; even support 125 MHz state machines.



Just when you thought the board was full, multichip modules slip 1 MB SRAMs into a 1/8" space.

PLAY HARDBALL WITH THE COMPETITION.



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1000V ($18.22), 20A/ 1000V ($8.93), and 32A/ 600V ($17.46) (1000). Harris Semiconductor, Melbourne, FL, (800) 442-7747, ext 1124.
—Anne Watson Swager

Software cuts 15% off ASIC NRE costs

Gould AMI says its Access software tools help you slip your ASIC design into production smoothly. To back up that claim, the company is offering a 15% reduction in nonrecurring engineering (NRE) charges for customers who run the software and produce optimized tester-compatible designs. The $5000 software helps designers avoid ASIC design flaws and test pattern incompatibility with the company's production testers. Gould AMI, Pocatello, ID, (208) 233-4690.—Doug Conner

Companies jointly develop local desktop bus

Digital Equipment Corp and Signetics have jointly developed a local desktop bus, called Access Bus. The companies developed the bus specification around the Signetics I^2C (Inter-Integrated Circuit) bus. DEC uses the bus in its DECstation 5000 entry-level workstations to interconnect desktop peripherals. The bus can interconnect low-bandwidth peripherals, such as a mouse, keyboard, or joy stick, and specialized peripherals, like digitizers, tablets, modems, printers, and image scanners. Using the bus eliminates the need for specialized I/O cards. Rather, the bus provides a simple plug-and-play mechanism for desktop devices.

The bus links as many as 14 devices. It uses a 4-pin shielded modular connector with a 2-wire (serial and clock lines) bus for interconnection, with a 78.5-kbit/sec transfer rate. The hardware base for the bus is in place; the I^2C bus is a common peripheral on Signetics 8051 microcontrollers and is available on more than 120 integrated circuit components. The bus is an open standard, with no licenses or royalties required.

Computer Access Technology Corp is the first vendor to develop a product for the bus, via a joint development and marketing relationship with Signetics. The company's first product will be a bus controller board for PC/AT buses. Due in September, the board will provide a desktop bus for peripherals. The company will also provide a consulting service for computer and peripheral vendors. Computer Access Technology, Sunnyvale, CA, (408) 732-8910; Digital Equipment Corp, Andover, MA, (508) 689-1000; Signetics, Sunnyvale, CA, (408) 991-2000.

—Ray Weiss

Chip makes pc-board traces programmable

Next week Aptix Corp will introduce a RAM-based field-programmable interconnect device that can make a resistive connection between any two of its nearly 1000 I/O pins. At the same time, the company will be announcing prototype boards incorporating these parts and several associated CAE tools. These products will force you to rethink the way you build prototype hardware. For more information, see EDN News Edition's April 30 issue and the May 7 issue of EDN magazine. Aptix Corp, San Jose, CA, (408) 428-6200, FAX (408) 944-0646.—Steven H Leibson

Cut prototyping costs with infrared sensor kit

Elf Atochem Sensors' $99 infrared sensor kit lets you experiment with passive infrared-detection technology and save time in prototype development. The hardware package includes two boards—an LED module with voltage regulator and 9V battery clip, and a detector module with Fresnel-lens, amplifier/filter, comparator, sensitivity adjustment, and 9V battery clip. You can modify the boards to trigger mechanisms such as timers and pulse counters. The kit comes with application notes, a schematic of the detector's low-power circuit, articles on polymer infrared applications, and several design tips. Elf Atochem Sensors, Valley Forge, PA, (215) 666-3500. Contact Ed Tom.—J D Mosley

Tool kit eases fax/data-modem product development

Putting together products based on DSP technologies has become easier with a modem tool kit from Analog Devices Inc. The ADAT-DSI01 "data-pump" tool kit furnishes relocatable object code for data-modem and fax-modem algorithms. The code supports V.32bis, V.32, V.22bis, V.22, and other modem standards, as well as Group-3 fax standards V.17, V.29, V.27ter, and V.21. The algorithms receive and transmit data in full-duplex mode at data rates from 300 to 14,400 bps. The tool kit requires you to use the company's AD20msp501 and AD20-msp502 fax/data-modem chip sets. The $1500 tool kit includes the software, documentation, and a license. For designers who want additional software, a complete modem-design kit is available from Digicom Systems. The kit supplies code for modem control, error correction, and data compression. Digicom also supplies a test board that includes the

DSP chip, RAM, and a direct-access arrangement circuit.

Analog is taking the tool-kit approach with other suppliers that will provide algorithms for image and speech compression and speech recognition. In addition to Digicom, the company has signed up Lernout and Hauspie Speech Products (Ypres, Belgium) for speech-recognition, text-to-speech, and speech-encoding algorithms; Xing Technology (Arroyo Grande, CA) for image- and audio-compression algorithms; and Euphonics, Inc (Boulder, CO) for Dolby sound-encoding algorithms. Analog Devices Inc, Norwood, MA, (617) 461-3752. Digicom Systems, Milpitas, CA, (408) 262-1277.—Jon Titus

Libraries bolster analog and mixed-signal ASICs

New libraries and macrocells available as part of Harris Semiconductor's Fastrack ASIC design system enhance the system's analog and mixed-signal designs. The HDI4000 200V bipolar, dieletrically isolated, device-level library suits telecommunications, high-voltage switching, and power-control applications. Specific circuit applications include subscriber-line interfaces, high-voltage preamplifiers, high-current-amplifier output stages, and analog switches with high standoff voltage and low current. The HDI4000 library features fully complementary, bipolar devices capable of operating at breakdown voltages ranging from 80 to 200V. Resistors, MOS capacitors, JFETs, and zener diodes are all available. Typical f_Ts are 300 MHz for npn and 80 MHz for pnp transistors.

In addition to this new library, the company has added user-modifiable hard-coded macrocell functions to its 20 and 40V device-level libraries. The company created these macrocell libraries, the HDI1000HC and HDI2000HC, from its 20 and 40V tile arrays, respectively. The macrocells are more compact than those contained within the tile arrays, but users can modify the hard-coded cells for specific design requirements. Each library consists of 26 and 22 analog hard-coded cells, respectively. These cells include op amps, comparators, S/H functions, voltage references, mixers, and multipliers. These two libraries are available as part of the Analog Fastrack design system, for which nonrecurring engineering (NRE) costs begin at $60,000.

The company has also announced a July debut of a BiCMOS cell library for high-integration, mixed-signal ASICs. The HBC1000 library will combine complementary-bipolar analog, sampled-data CMOS for switched-capacitor networks, and high-speed and high-density logic. The initial release will include a variety of functions, including a set of core amplifier cells, a programmable amplifier, a switch family, a 5-μsec ADC, and sampled-data filter macros. This library is available as part of Mixed Signal Fastrack. Typical NRE cost involving the mixed-signal library is $145,000. Harris Semiconductor, Melbourne, FL, (800) 442-7747.

—Anne Watson Swager

Software tools estimate packaging performance

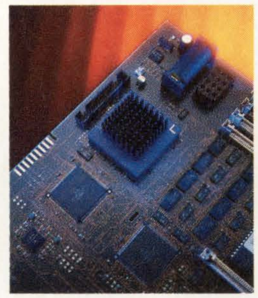
When simulating your high-speed ASIC, don't forget the effect your package has on performance. Two software tools released at Nepcon in Anaheim, CA, in late February by Ansoft Corp can help predict transmission-line effects on lead frames and packaging. The ParICs physical IC modeler release 2.8 accepts 2-D leadframe designs in several CAD formats and automatically generates 3-D models. It also has modeling for standard DIP and surface-mount packages. The company's Maxwell 3-D field simulator release 1.2 accepts the ParIC models and calculates the package's capacitance and inductance. The field simulator can also handle magnetic components, connectors, through-holes, vias, and gull-wing leads. The modeler runs on DOS-based computers and Sun workstations; prices begin at $10,495, depending on platform and options. The field simulator runs on Sun, HP, Apollo, and IBM workstations. An annual license for the simulator is $18,000; a perpetual license is $45,000. Ansoft Corp, Pittsburgh, PA, (412) 261-3200 .—Richard A Quinnell

Disk-drive chip set is user configurable

Disk-drive designers can now get a chip set that blends a stock part's cost and availability with the flexibility of a custom part. Micro Linear's 3-chip set includes the ML4610 disk-head amplifier ($2 (100,000)), the ML6006 36-Mbps read-channel filter and equalizer ($6), and the FC3560 read-channel chip. The amplifier and filter ICs are both stock parts; the read-channel chip is a semicustom IC based on an analog tile array. The device includes a pulse detector, four gated servo peak detectors, a bandgap reference, a frequency synthesizer, and oscillators as analog building blocks. It also offers an 800-gate digital gate array. You customize the device by connecting blocks with the metal layers. You can receive your initial IC within eight weeks; subsequent revisions take four weeks. The customized device's price varies with package type and number of blocks used, but a preconfigured version, the ML6010, sells for $7 (100,000). Contact Pam Gopalan, Micro Linear Corp, San Jose, CA, (408) 433-5200.—Richard A Quinnell

MOTOROLA.
THE NeXT™ CHOICE.

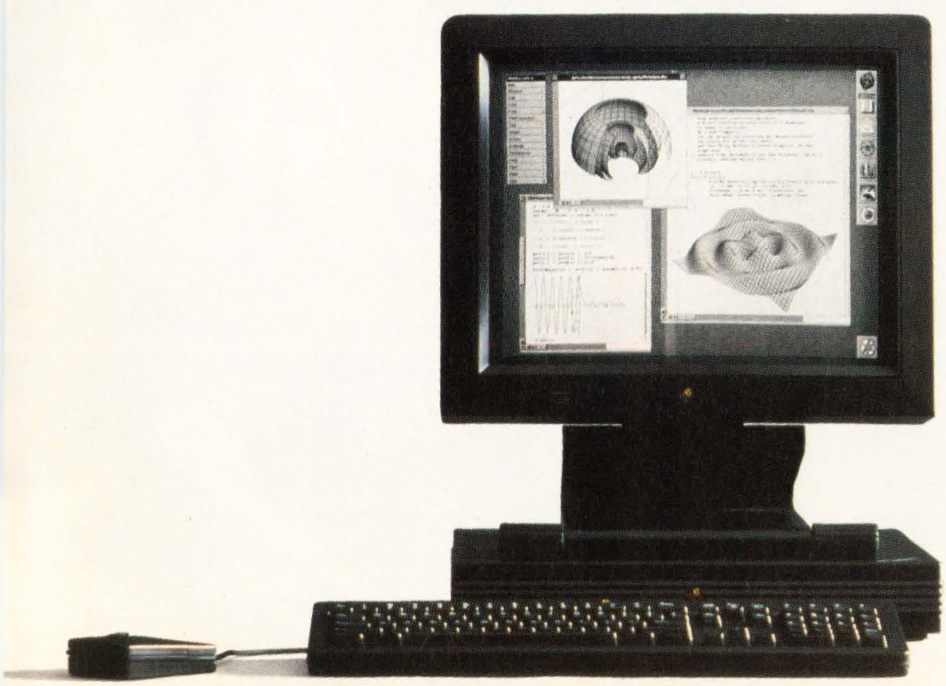
There's a very good reason why the machine shown here is called NeXTstation™ Turbo. Its speed. *Incredible* speed, thanks to NeXT's decision to upgrade to Motorola's lightning-fast 33MHz 040 processor. NeXT was determined to design a machine that offers both speed and an unprecedented number of system features at an affordable price, and they did it. With system solutions from Motorola, an industry leader in advanced ASIC.



The 33MHz 040 processor is only one of the Motorola contributions that turned NeXT's vision into reality. Among the essentials NeXT wanted for the NeXTstation Turbo was super-fast memory transfer, so they chose Motorola's CMOS ASIC for their NeXT-designed VLSI chips. The result is the Turbo Memory Controller (TMC), capable of supporting up to 128MB of fast, interleaved RAM, with prefetching.

The NeXTstation Turbo also boasts a Peripheral Controller (PC) which NeXT designed with Motorola's CMOS ASIC technology, enabling the Turbo system DMA architecture to offload I/O functions for maximum system output - a NeXT key objective. And still another benefit NeXT gained by using Motorola high-density CMOS gate arrays is JTAG Scan Design, which allows utilization of Motorola Mustang™ ATPG software to achieve a dramatic reduction in design cycle time.

In designing the NeXTstation Turbo, NeXT's primary goal was to be able to offer customers the most machine for the least money. Working with Motorola, they achieved it. Indeed, the NeXTstation Turbo offers state-of-the-art solutions that come from good old fashioned teamwork.



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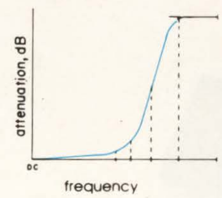
• meets MIL-STD-202 tests • over 100 off-the-shelf models • immediate delivery

low pass, Plug-in, dc to 1200MHz

LOW PASS



Model No.	Passband MHz loss < 1dB	Stopband, MHz loss > 20dB	Stopband, MHz loss > 40dB
PLP-5	DC-5	8-10	10-200
PLP-10.7	DC-11	19-24	24-200
PLP-21.4	DC-22	32-41	41-200
PLP-30	DC-32	47-61	61-200
PLP-50	DC-48	70-90	90-200
PLP-70	DC-60	90-117	117-300
PLP-90	DC-81	121-137	167-400
PLP-100	DC-98	146-189	189-400
PLP-150	DC-140	210-300	300-600
PLP-200	DC-190	290-390	390-800
PLP-250	DC-225	320-400	400-1200
PLP-300	DC-270	410-550	550-1200
PLP-450	DC-400	580-750	750-1800
PLP-550	DC-520	750-920	920-2000
PLP-600	DC-680	840-1120	1120-2000
PLP-750	DC-700	1000-1300	1300-2000
PLP-800	DC-720	1080-1400	1400-2000
PLP-850	DC-760	1100-1400	1400-2000
PLP-1000	DC-900	1340-1750	1750-2000
PLP-1200	DC-1000	1620-2100	2100-2500

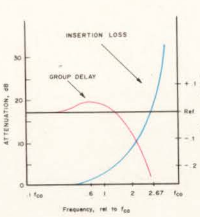
Price, (1-9 qty), all models: plug-in $14.95, BNC $32.95, SMA $34.95, Type N $35.95

Surface-mount, dc to 570MHz

Model No.	Passband MHz loss < 1dB	Stopband, MHz loss > 20dB	Stopband, MHz loss > 40dB
SCLF-21.4	DC-22	32-41	41-200
SCLF-30	DC-30	47-61	61-200
SCLF-45	DC-45	70-90	90-200
SCLF-135	DC-135	210-300	300-600
SCLF-190	DC-190	290-390	390-800
SCLF-380	DC-380	580-750	750-1800
SCLF-420	DC-420	750-920	920-2000

Price, (1-9 qty), all models: $11.45

Flat Time Delay, dc to 1870MHz

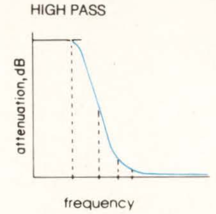


Model No.	Passband MHz loss < 1.2dB	Stopband MHz loss > 10dB	Stopband MHz loss > 20dB	VSWR Freq. Range, DC thru 0.2fco X̄	VSWR Freq. Range, DC thru 0.6fco X̄	Group Delay Variations, ns Freq. Range, DC thru fco X̄	2fco X̄	2.67fco X̄
PBLP-39	DC-23	78-117	117	1.3:1	2.3:1	0.7	4.0	5.0
PBLP-117	DC-65	234-312	312	1.3:1	2.4:1	0.35	1.4	1.9
PBLP-156	DC-94	312-416	416	0.3:1	1.1:1	0.3	1.1	1.5
PBLP-200	DC-120	400-534	534	1.6:1	1.9:1	0.4	1.3	1.6
PBLP-300	DC-180	600-801	801	1.25:1	2.2:1	0.2	0.6	0.8
PBLP-467	DC-280	934-1246	1246	1.25:1	2.2:1	0.15	0.4	0.55
▲BLP-933	DC-560	1866-2490	2490	1.3:1	2.2:1	0.09	0.2	0.28
▲BLP-1870	DC-850	3740-6000	5000	1.45:1	2.9:1	0.05	0.1	0.15

Price, (1-9 qty), all models: plug-in $19.95, BNC $36.95, SMA $38.95, Type N $39.95
NOTE: ▲: -933 and -1870 only with connectors, at additional $2 above other connector models.

high pass, Plug-in, 27.5 to 2200MHz

HIGH PASS

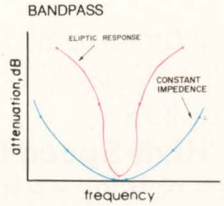


Model No.	Stopband MHz loss < 40dB	Stopband MHz loss < 20dB	Passband MHz loss < 1dB	VSWR Passband Typ.
PHP-25	DC-13	13-19	27.5-200	1.8:1
PHP-50	DC-20	20-26	41-200	1.5:1
PHP-100	DC-40	40-55	90-400	1.8:1
PHP-150	DC-70	70-95	133-600	1.8:1
PHP-175	DC-70	70-105	160-800	1.5:1
PHP-200	DC-90	90-116	185-800	1.6:1
PHP-250	DC-100	100-150	225-1200	1.3:1
PHP-300	DC-145	145-170	290-1200	1.7:1
PHP-400	DC-210	210-290	395-1600	1.7:1
PHP-500	DC-280	280-365	500-1600	1.8:1
PHP-600	DC-350	350-440	600-1600	2.0:1
PHP-700	DC-400	400-520	700-1800	1.6:1
PHP-800	DC-445	445-570	780-2000	2.1:1
PHP-900	DC-520	520-660	910-2100	1.8:1
PHP-1000	DC-550	550-720	1000-2200	1.9:1

Price, (1-9 qty), all models: plug-in $14.95, BNC $36.95, SMA $38.95, Type N $39.95

bandpass, Elliptic Response, 10.7 to 70MHz

BANDPASS



Model No.	Center Freq. (MHz)	Passband I.L. 1.5 dB Max. (MHz)	3 dB Bandwidth Typ. (MHz)	Stopbands I.L. > 20dB at MHz	Stopbands I.L. > 35dB at MHz
PBP-10.7	10.7	9.6-11.5	8.9-12.7	7.5 & 15	0.6 & 50-1000
PBP-21.4	21.4	19.2-23.6	17.9-25.3	15.5 & 29	3.0 & 80-1000
PBP-30	30.0	27.0-33.0	25-35	22 & 40	3.2 & 99-1000
PBP-60	60.0	55.0-67.0	49.5-70.5	44 & 79	4.6 & 190-1000
PBP-70	70.0	63.0-77.0	68.0-82.0	51 & 94	6.0 & 193-1000

Price, (1-9 qty), all models: plug-in $18.95, BNC $40.95, SMA $42.95, Type N $43.95

Constant Impedance, 21.4 to 70MHz

Model No.	Center Freq. MHz	Passband MHz loss < 1dB	Stopband loss > 20dB at MHz	VSWR 1.3:1 Total Band MHz
PIF-21.4	21.4	18-25	1.3 & 150	DC-220
PIF-30	30	25-35	1.9 & 210	DC-330
PIF-40	42	35-49	2.6 & 300	DC-400
PIF-50	50	41-58	3.1 & 350	DC-440
PIF-60	60	50-70	3.8 & 400	DC-500
PIF-70	70	58-82	4.4 & 490	DC-550

Price, (1-9 qty), all models: plug-in $14.95, BNC $36.95, SMA $38.95, Type N $39.95

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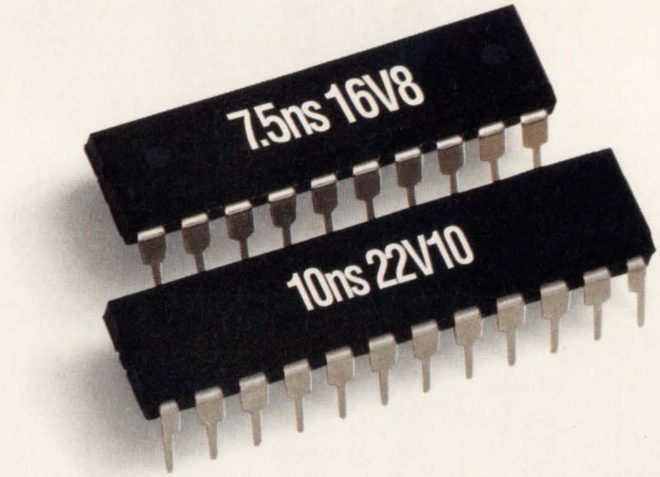
F132-2 REV. A

Low Delays.



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CIRCLE NO. 20

Concerning the fastest state/timing acquisition card

I would like to set the record straight regarding logic-analyzer acquisition speeds. An EDN News Break (February 17, 1992, pg 24) contained a Hewlett-Packard claim that the 16550 card is now the fastest state/timing acquisition card on the market. This is not true. The Paladin card from American Arium exceeds the HP acquisition-speed specification by exactly two times in both state (200 MHz) and timing (1 GHz), and the memory depth is significantly deeper (128 kbits/channel). Paladin plugs into the ML4400 logic-analyzer mainframe.

Jeff T Acampora
Director, Sales & Marketing
American Arium
Tustin, CA

A baudy affair

The letter (EDN, August 19, 1991, pg 33) from Chris Rogers, an engineer at SCI Technology in Huntsville, AL, discussing the correct use of bits per second (bps) and baud, has stirred up a veritable fire storm. The editorial response, penned by EDN Technical Editor, Chris Terry, was printed unsigned. Among the comments we have received were letters from Gerald Edelman, a senior scientist at ITT Aerospace and Communications Div in Nutley, NJ; John H Humphrey, a general partner at Telequality Assoc, in Golden CO; and P F Gascoyne of West Hanney, UK. Other comments appeared in the EDN BBS's /Soapbox special-interest group.

Chris Rogers's letter, our reply, and all of the communications we have received agree on one point: Speakers and writers are wrong to use baud when they mean bps—a common mistake. Nevertheless, there were several errors in our *Ed Note*. The most serious was our statement that with the V.29 quadrature-amplitude-modulation (QAM) scheme used in 9600-bps facsimile and leased-line modems, the communications channel transmits 600 baud. In fact, from the definition of baud, a V.29 modem transmits 2400 baud.

The correct definition of baud is the number of symbols/sec transmitted over a communications channel. V.29 QAM manipulates both the amplitude and phase of the carrier so that a symbol can represent any 1 of 16 values. In other words, each symbol represents four bits of data—$2^4=16$. If you divide 9600 bps by 4 bits/symbol, you get 2400 symbols/sec or 2400 baud.

Because amplitude and relative-phase measurements don't depend on a signal's instantaneous polarity, each cycle of a modem's carrier frequency can transmit two symbols—one in each half cycle. Therefore, to transmit 9600 bps with 4 bits/symbol, the carrier frequency must be at least 1200 Hz. In fact, in V.29, the carrier frequency is about 50% higher, a value still well within a dial-up voice-grade line's normal bandwidth of 250 to 3250 Hz.

You might infer from this channel bandwidth and from the fact that you can send two symbols per cycle, that a dial-up voice-grade line could support transmission at 6000 baud. In fact, though, reader Gascoyne points to textbook proofs showing that the theoretical maximum on a 3-kHz line is in the neighborhood of 3000 baud. Moreover, before the advent of adaptive line equalization, the practical maximum was 1200 baud.

Apparently, if you try to send more than 3000 symbols/sec on a 3-kHz-bandwidth line, the signal bandwidth extends so far beyond the band edge that even adaptive equalization can't compensate for the line's attenuation and phase shift. With a normal level of line noise, the result is an unacceptable error rate.

A BBS caller objected to the way we used the term, PSTN (public switched telephone network) in the article, "ISDN-based concurrent design" (EDN, March 1, 1991, pg 80) that prompted all the correspondence on baud vs bps. This objection appears to be unfounded. As far as we know, even though ISDN (integrated-services digital network) services are now utilized by public switched dial-up networks, the PSTN acronym predates ISDN. PSTN refers to channels whose characteristics are based on those of the older analog network.

Reader Humphrey took reader Rogers to task for subtracting the overhead of asynchronous communication when he determined the rate of information transfer over a 9600-bps channel. Humphrey points out that asynchronous modems offer synchronous-communication options that do away with most of the overhead. Moreover, depending on the redundancy of the data, modems that include data-compression firmware can sometimes transmit at data rates higher than the 57.6 kbps often quoted for ISDN channels. Humphrey objects to using data rates to compare PSTN and ISDN channels. Such arguments, he observes, fail to acknowledge the tremendous investment in the existing telephone network.

Dan Strassberg,
Technical Editor
EDN Magazine
Newton, MA

Shuffling royalties robs small recording artists

Concerning Steve Leibson's editorial, "Buy this and you're a thief" (EDN, November 7, 1991, pg 55), I'd like to add an angle he didn't mention.

In addition to being an electrical engineer, I'm also a musician who has a small recording studio. If Congress approves the bill that will add royalty fees to digital-audio-tape recorders and blank tapes, then I'll be paying royalties to other people for my own original works!

Now, who's the thief? I may never produce something that generates royalties that I'll collect, but I can still dream, can't I? Something rubs me the wrong way when a well-established artist like Michael Jackson gets richer from my personal creativity merely because I choose to record my work on the highest quality medium available to me.

I consider these proposed royalties to be *anticompetitive.* Now that technology has given small studios and even the average home recording artist the means to compete against the big boys, the recording industry is running scared and is trying to shut us down and keep us out of the race.

Bill Fox
Pataskala, OH

Correction

EDN's VXI Source Guide (October 10, 1991, pg 73) listed an incorrect address, phone number, and FAX number for Giordano Associates. The firm has moved; the updated information is

Giordano Associates Inc
5 Century Dr
Parsippany, NJ 07054
Phone (201) 292-0079
FAX (201) 292-9416

The value of a sense of humor

It was with great delight that we here at Togai Infralogic read Jon Titus's commentary, "You've got to have fun (EDN, February 3, 1992, pg 33). As Mr Titus so aptly points out, having fun and learning to laugh and make light of certain situations does indeed help one keep things in perspective.

Working in the engineering community often forces one to conform and pay utmost attention to detail. As such, there can be little room for light-hearted and carefree thinking. Having a sense of humor is critical to the success of so much that we do, and you have reaffirmed this quite nicely.

Many of the great thinkers of our time and before have been able to achieve their goals by maintaining balance and wit. Becoming an adult does not mean losing sight of the creative and imaginative—these [qualities] are what keep us young at heart and keep us going! Einstein, Edison, and Avogadro exemplify the gift of humor and its payoffs.

Camerone A Welch, Director
Corporate Communications
Togai Infralogic Inc
Irvine, CA

Reader finds PLDs are too costly to use

Charles Small's editorial (EDN, October 10, 1991, pg 49) on PLDs was right on the money! I have always felt that it cost too much to get involved in the process for a small company. I would love to get into this field to design some chips for our company, but being a small company, it is just not cost effective. Let's see some movement by the producers of this logic to get us involved. They will make their profit on the sale of even more chips when the rest of us can get in.

Ed Osborne
Vibrac Corp
Penacook, NH

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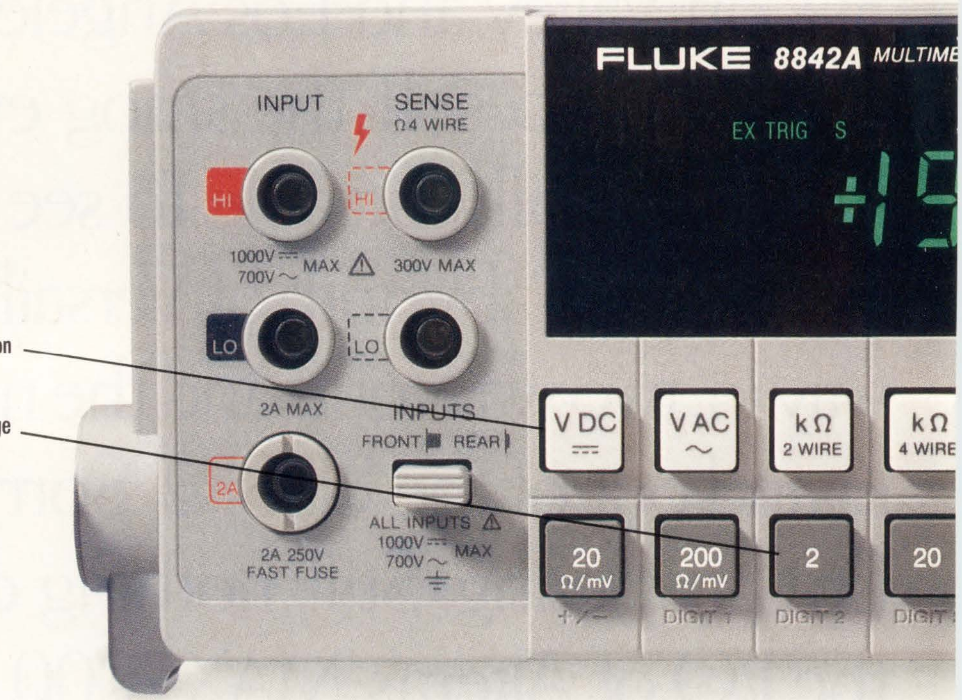

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Feature	Fluke 8842A	HP 34401A
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Common Mode Noise Rejection	>140 dB	140 dB
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dV Ranges	Six: 20 mV – 1000V	Five: 100 mV – 1000V
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Basic One Year DC Accuracy	±0.003%	±0.0035%

Then there's interference. Will common or normal mode noise

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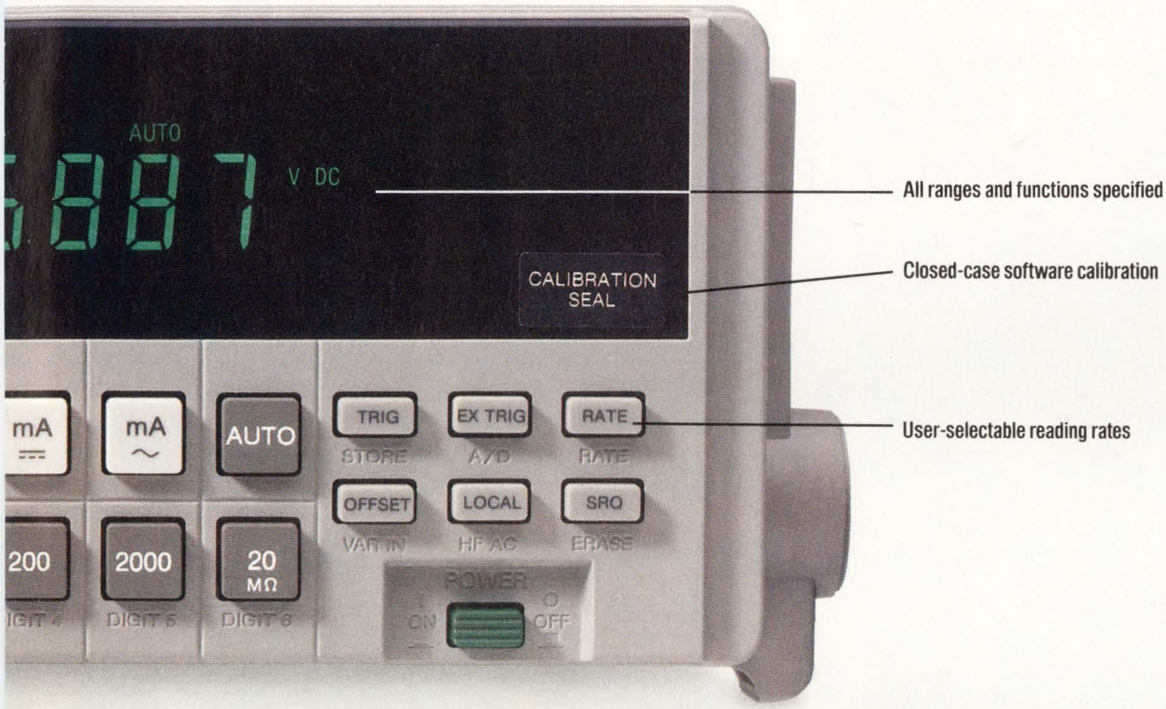

M is actually a 5½ digit DMM.

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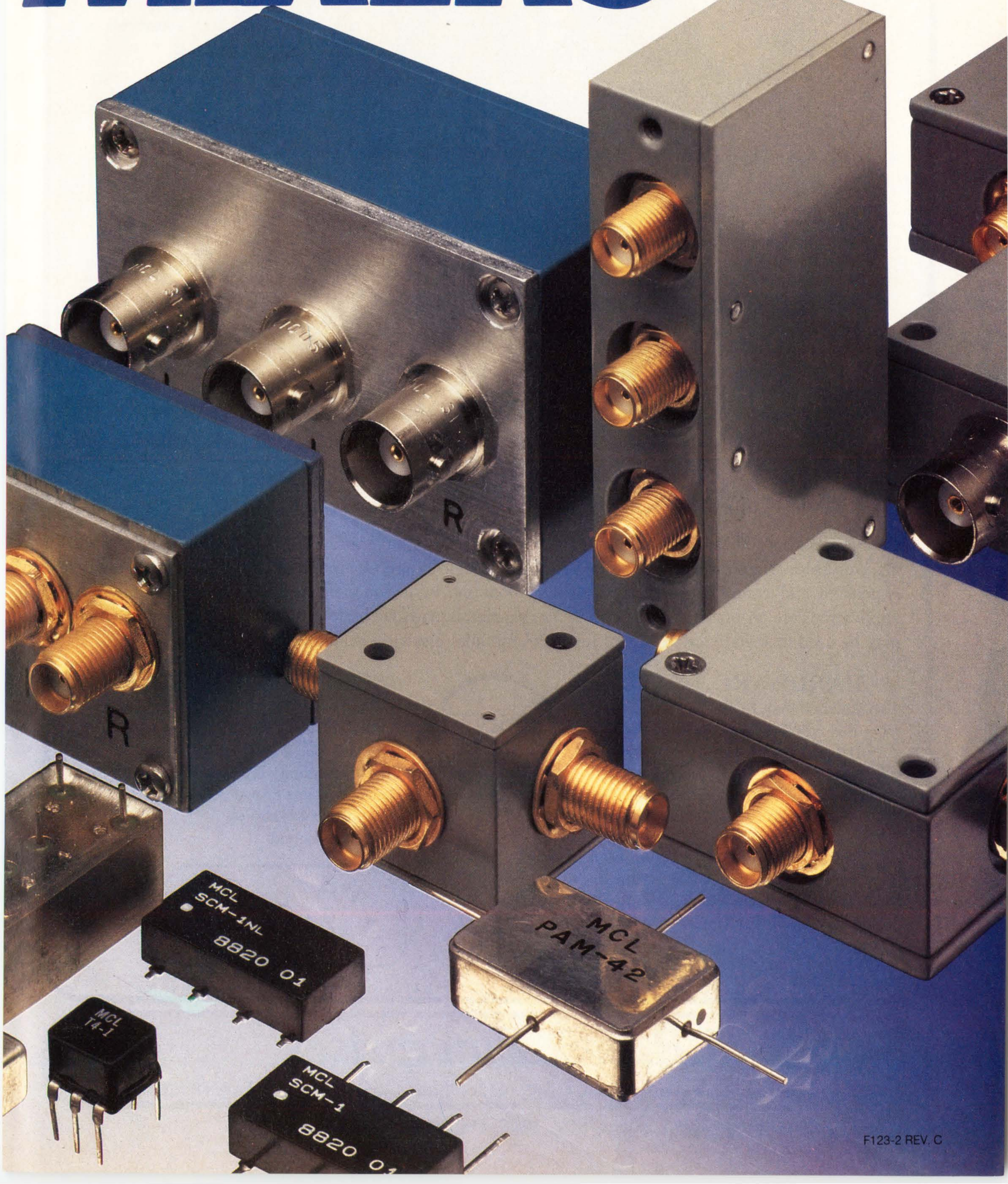

Don't blame the kids

Here in the US, we've read stories about how poorly our students have done on standardized tests when compared with students in other countries. Educators, politicians, and parents are clamoring for more money, more homework, longer school years, and longer school days. Kids, they say, just aren't learning what they're supposed to. They're spending too much time watching television and fooling around. Blaming the kids is easy.

The answer isn't so simple. It's surprising that, as part of the solution to the current education "crisis," no one is calling for enforcing minimum performance standards for teachers, administrators, and book suppliers. It would be interesting to compare the tests from teachers in Japan, Germany, and the US. How do US educators compare with their colleagues overseas? After all, it's these people who are supposed to mold our kids' education.

Teachers are the key to a solid educational structure. Yet we don't test that structure for its soundness, and we demand little—if any—accountability. Likewise, it's the knowledge that teachers have and how they impart it to their students that makes all the difference. It's often surprising what teachers teach. For example, I had one teacher tell me that no nuclear weapons were used in World War II. It is not the teachers alone who are at fault. Recently, the *Wall Street Journal* listed many errors in high-school history books. A review panel of noneducators found more than 5200 other errors while examining less than two dozen history texts.

So what's a parent to do? Start by asking your children what they're learning, and ask them to explain it. Don't ignore the opportunity to meet with teachers during school open houses. Don't hesitate to question teachers about what your children are learning, and about how the teachers are teaching it. Read your kids' textbooks—even one chapter is a start. Sit in on a class. Press for uniform teacher testing and minimum standards.

If you're brave, take on the issue of tenure for public-school teachers. The issue isn't how tenure protects "academic freedom," but how it protects lifetime employment. Dumping tenure for public-school teachers is worth the fight. Without giving school boards the ability to fire poor teachers, testing teachers only identifies the problems, it doesn't remove them. Academic freedom is important, and we should protect it, but we shouldn't use it as an excuse for protecting poor teachers who deny students a good education. It's time to empower school boards to test teachers and to throw out the poor ones.

Jon Titus
Editor

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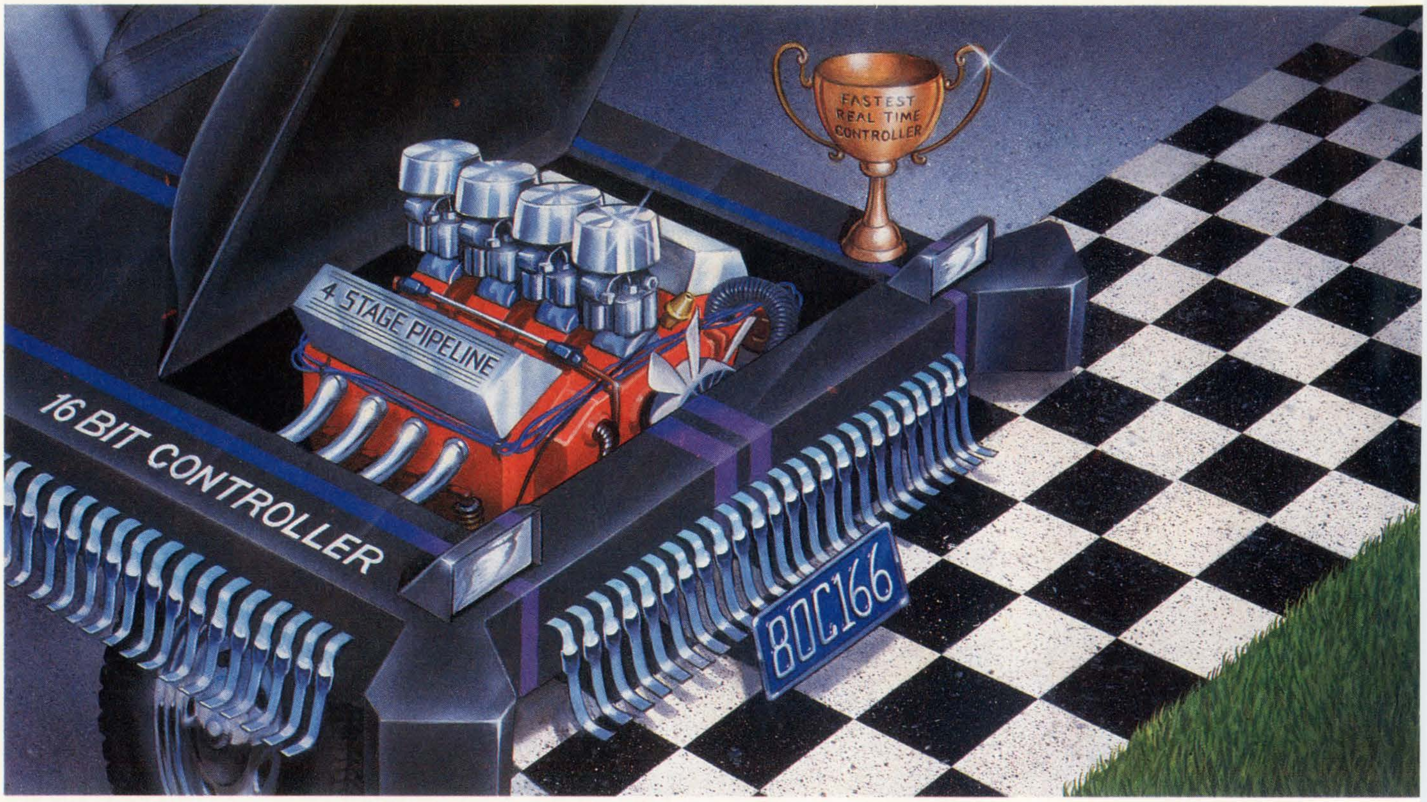

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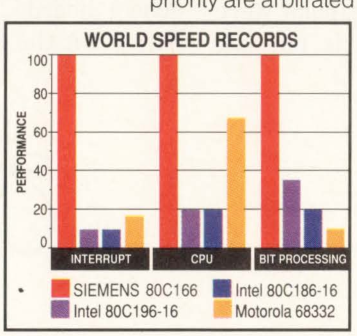

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CIRCLE NO. 32

SENSORLESS MOTOR-CONTROL ICs

Spin chips whirl into nondrive applications

J D MOSLEY, Technical Editor

Spin chips use the back EMF of a brushless dc motor to control its speed, thus eliminating any need for the expensive Hall-effect sensors normally used to adjust commutation. Although this increased integration implies simpler designs, these chips require new techniques for starting the motors they control.

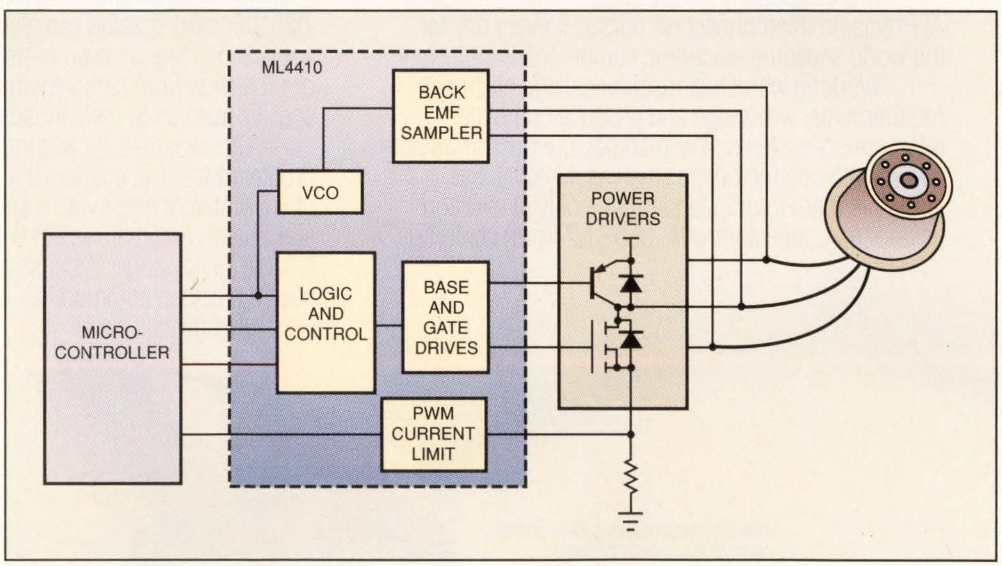
The benefits presented by emerging technologies inevitably host an assortment of new design challenges, and motor-control technology is no exception. As disk-drive form factors shrink to 2.5 and 1.8 in., the motors that power those drives and the circuits that control the motors have similarly dwindled in size. In fact, much of the control circuitry for these tiny motors is now available as a single IC, often referred to as a spin chip.

The sensorless and brushless dc motors that you can control with spin chips have applications beyond the disk-drive market in automotive and consumer electronics. Fans, VCRs, process controllers, robotics, and an assortment of toys are just a few of the logical targets for these motors.

The appeal of dc motors lies in the elimination of mechanical commutators and brushes. Without the specters of arcing and brush wear, these motors offer high efficiency and rapid acceleration for high-speed operation. However, most of these motors use magnetoresistive Hall-effect sensors to replace the mechanical commutators that previously provided rotor positioning. These Hall-effect sensors reduce a motor's MTBF, and therefore its reliability, because they require additional control-signal wires and connectors within the motor.

Hall-effect sensors also introduce increased sensitivity to temperature variations, RFI, and circuit noise. And because these sensors are built into the motor, the motor's size, cost, and power consumption also increase. Furthermore, even a small error in positioning a Hall sensor within a motor can diminish the motor's drive performance.

Although using spin chips helps avoid



Spin chips perform back-EMF sensing functions in motor-control applications. The chips, such as Micro Linear's ML4410, work in conjunction with microcontrollers and power drivers to eliminate any need for Hall-effect sensors.

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problems incurred by using Hall-effect sensors, you face new problems when starting the motor. Spin chips control a motor's speed by monitoring the motor's back EMF in order to determine how to vary the current in the motor windings. The set of voltages being applied to a motor's three terminals indicates the commutation state.

Changes in back EMF dictate the application of drive voltage and the switching of commutation states. When the back EMF approaches the applied voltage, the motor speed approaches a maximum steady-state value. The six output-state combinations provided by a typical spin chip are illustrated in **Fig 1**.

However, at start up, there is no back EMF being generated by the motor for the control chip to reference. Accordingly, the start-up logic developed by the various IC manufacturers frequently differentiates the spin chips that are currently available.

That sounds logical

Some of these ICs require the control of an external μP to initiate motor rotation. The SSI32M595

Table 1—Sensorless motor-control ICs

Manufacturer	Model	Output current	Supply voltage	Power consumption	Price	Comments
Allegro	A8901SLB	1A	4.5 to 6.5V	10 mA max	$7.01 (1000)	Programmable start-up current; diagnostics mode; sleep mode; serial port.
	A8902SLB	1A	5 to 6V	10 mA max	$7.35 (1000)	Programmable start-up; dynamic braking; sleep mode; serial port; diagnostics.
Cherry	CS-5143	1A	4 to 18V	8 mA max	$3.40 (1000)	Full-wave commutation; start-up circuitry; sleep mode; output-protection circuitry.
Harris	SP600	0.5A	5 to 18V	2.05 mA max	$6.10 (1000)	Half-bridge 500V dc driver for PWM motor-drive and power-supply applications.
Hitachi	HA13481S	2A	10.2 to 13.8V	38 mA max	$3.50 (1000)	Start-up circuit; speed discriminator; suits 4- and 5-MHz clocks.
	HA13501S	1.2A	4.25 to 5.75V	15 mA max	$4.25 (1000)	Digital servo system; digital ready circuit; start-up circuit; motor on/off control.
	HA13508S	2A	10.2 to 13.8V	38 mA max	$4.45 (1000)	Braking function; ready signal; start-up circuit; suits 4- and 5-MHz clocks.
	HA13517F	1A	4.25 to 5.75V	30 mA max	$5.25 (1000)	10-bit serial interface; soft-switching matrix; power monitor; latch delay; booster.
	HA13601F	2A	4.25 to 6.5V	12 mA max	$4.45 (1000)	Power-off brake circuit; start-monitor circuit; current-limit circuit; digital servo system.
Micro Linear	ML4410	0.15A	4.5 to 14V	50 mA max	$5.35 (100)	Linear or PWM motor-current control; μP interface for start-up; delayed braking.
	ML4411	0.15A	4.5 to 14V	50 mA max	$5.35 (100)	Architecturally similar to ML4410, but improved braking and brown-out recovery.
Philips/ Signetics	TDA5140A	0.6A	4 to 18V	<5 mA	$2.25 (OEM)	Full-wave motor control; start-up circuitry; three outputs.
	TDA5141	1.8A	4 to 18V	<5 mA	$2.45 (OEM)	Full-wave motor control; start-up circuitry; three outputs.
	TDA5142	0.15A	4 to 18V	<5 mA	$2.15 (OEM)	Braking function; start-up circuitry; full-wave motor control; six outputs.
SGS-Thomson	L6232A	2.5A	10.5 to 18V	6 mA max	$6.13 (1000)	User-configurable cutoff time; brake function; triple half-bridge driver.
	L6238	2.5A	10.5 to 18V	5 mA max	$14.50 (1000)	Integrated start-up algorithm; master/slave synchronization; digital PLL; PWM/linear.
	L6243	2.5A	10.5 to 18V	6 mA max	$7.50 (1000)	Parking function for hard-disk head actuator; linear control; thermal protection.
Silicon Systems	SSI32M595	10 mA	4.75 to 5.25V	<5 mA	$5 (1000)	3600-rpm speed control using 2-MHz clock; dynamic braking.
	SSI32M7010	0.75A	4.75 to 5.25V	<10 mA	$4 (OEM)	Low-voltage head-retraction and braking; commutation transient suppression.
	SSI32M7011	0.75A	4.75 to 5.25V	<10 mA	$4 (OEM)	Immune to brown-outs and load transients; reduced dv/dt on commutation.
	SSI32H6810	0.7A	5V	<1 mA	$4.50 (OEM)	Low power-down mode (<1 mA); low-voltage head-retraction and braking.
	SSI32H6811	0.7A	5V	<1 mA	$5 (OEM)	Dual DACs; serial port; low-voltage head-retraction and braking.
Unitrode	UCC3301	1A	3.5 to 5V	<20 mA	$7.05 (1000)	2.5- and 1.8-in. hard-disk drive applications; parking-delay circuit; standby current.

SENSORLESS MOTOR-CONTROL ICs

from Silicon Systems is an example of such an IC. The μP must generate a stream of pulses to advance the motor at start-up, but usually within one revolution the motor has attained sufficient speed for the IC's back-EMF sense logic to detect the motion. At that point, the μP's function is complete and the control IC spins the motor up to speed and regulates commutation.

Other ICs don't need μP support to initiate motor rotations. For example, the TDA5140A spin chip from Philips and Signetics has three commutation circuits to handle the three possible start-up states of a motor and to avoid initial motor oscillations that can occur with other less sophisticated control ICs.

The TDA5140A uses a start-up oscillator to generate a pulse that sets the IC's motor-drive outputs to the next state. If the motor rotates forward and generates sufficient back EMF for the IC to detect a zero crossing within a time period equal to 30° of the energizing cycle, then the commutation-delay circuit that normally controls motor speed brings the motor up to speed. **Fig 2** illustrates the normal commutation phases in a motor's windings.

To prevent the IC from mistaking a flyback pulse for a true zero crossing of the back EMF, this spin chip inhibits acknowledgment of any zero crossing for a time period defined by an external timing capacitor. A flyback pulse results whenever one of the chip's outputs switches off, which happens immediately prior to a back-EMF period.

This control IC also provides for two other start-up states. If the motor starts up by rotating in reverse, a phase-error commutation circuit detects the incorrect EMF phase and prevents further reverse rotation. And if the motor stalls when the IC applies a start-up pulse, the IC will torque the motor to the next state with a second pulse from the start-up oscillator.

To keep the motor rotating, the control IC has to compensate for any variation in the commutation delay that occurs between the zero crossing point and the point at which the IC energizes the motor. This delay is greatest when the motor first begins to accelerate, but each state commutation provides another burst of current to accelerate the motor. As the time between the zero crossings decreases, the commutation delay also decreases until either the motor reaches its peak speed or the control IC assumes its regulatory tasks.

Adaptive commutation is the method by which control ICs deal with inconsistent commutation delays. Although adaptive commutation techniques vary, most manufacturers use two external capacitors that charge and discharge to reflect the time between zero crossings.

One method uses each capacitor alternately to measure and divide successive crossings. Another method uses the initial charging capacitor (CAP-CD) to measure and divide the time between zero crossings and the initial discharging capacitor (CAP-DC) to store the commutation delay interval.

Cherry Semiconductor's CS5143 spin chip implements adaptive commutation using the second method. To obtain a device that clearly illustrates the motor's activity during commutation, you can call the company and request an adaptive commutation wheel. This wheel is actually a tool that presents winding states and polarity changes as an 8-pole, 9-coil, 3-phase, dc spindle motor rotates in 15° increments.

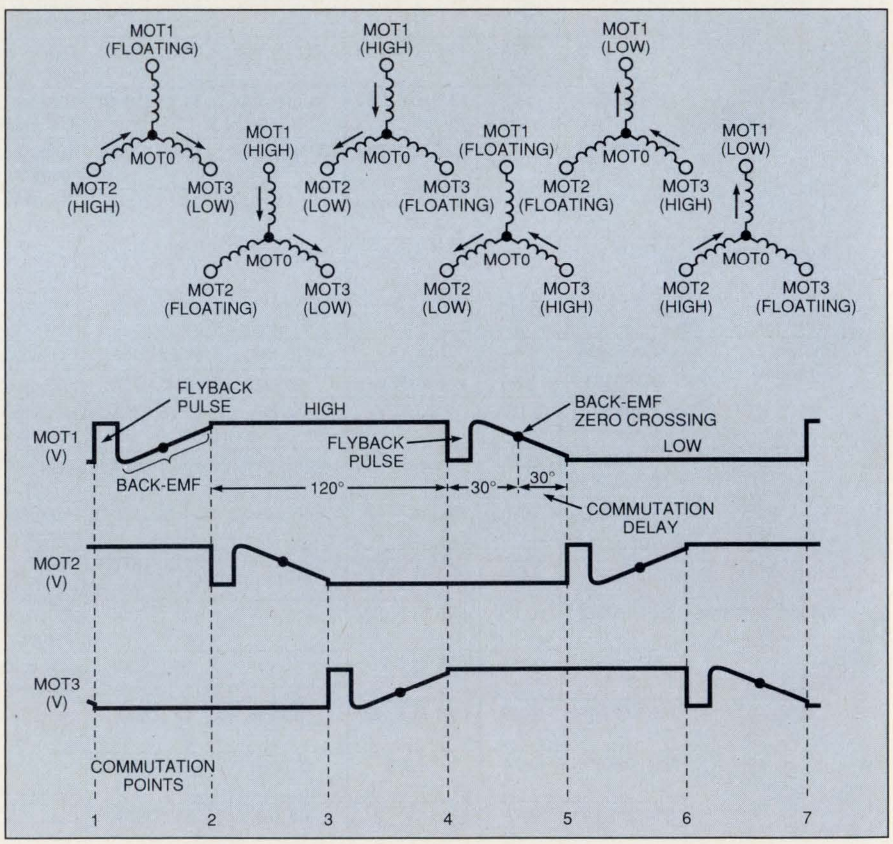

Fig 1—Spin chips offer six possible output states to energize motor coils. The directional arrows indicate current flow through the windings. Each zero crossing point is indicated as a centerpoint on the back-EMF slopes of the three voltage waveforms. Notice the flyback pulse that occurs when each IC output switches off.

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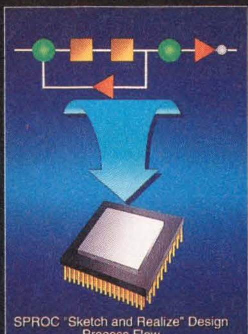
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CIRCLE NO. 36

A Flash of Brilliance.

SENSORLESS MOTOR-CONTROL ICs

Once the motor reaches the desired speed, the control IC needs to apply current to each motor winding when back EMF is strongest in order to generate maximum torque for maximum energy efficiency. PLL circuits provide one way to synchronize commutation that is unaffected by motor and load conditions. SGS-Thomson's L6238 spin chip uses a digital PLL to sample back EMF from the floating, unenergized motor winding to determine when to advance or delay commutation.

To accommodate a range of motor speeds, once during each revolution the PLL can accept a reference frequency to which it will lock the motor. For disk-drive applications, you can achieve master/slave synchronization among multiple drives by making a disk-feedback signal of the reference frequency for all of the drives.

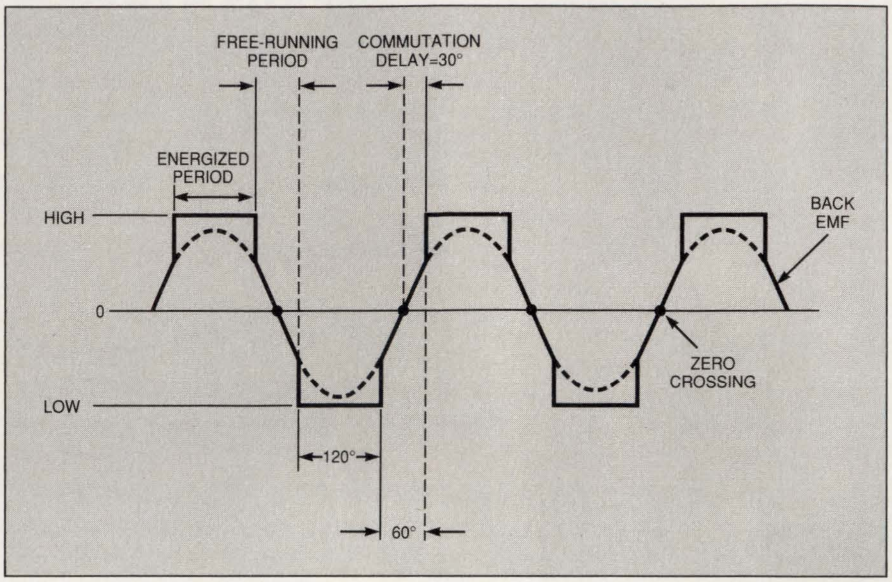

Fig 2—Commutation for each stator phase consists of a sequence of alternating energized periods separated by a nonenergized period during which the back-EMF zero crossings occur.

For more information . . .

For more information on the sensorless motor-control ICs discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you read about their products in EDN.

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FAX (508) 853-5049
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East Greenwich, RI 02818
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Harris Corp
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MS-CB1-25
Melbourne, FL 32901
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Philips Components
Box 218
5600MD Eindhoven
The Netherlands
(040) 791111
Circle No. 704

SGS-Thomson Microelectronics
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FAX (602) 867-6290
Circle No. 705

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FAX (408) 991-2242
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You will also want to consider whether the control IC uses PWM or a linear signal to control the motor's speed. PWM is the more energy-efficient technique, which is an important consideration for portable applications. However linear speed control introduces less noise into the circuit, which reduces the chance of introducing unwanted errors in disk-drive applications. Micro Linear's ML4411 spin chip provides both linear and PWM current-control circuits so that you can switch from one type of speed control to the other as your application performs different functions.

Stop in the nick of time

Eventually you will need to make the motor stop, and the braking method offered for any given spin chip may affect your design. Hitachi's HA13508S uses an active braking scheme that shorts the motor's windings to stop its rotation. In contrast, Allegro's 8902 actually delays the motor's stopping action

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PEAK CURRENT	50A	50A	50A	50A
OPERATING FREQUENCY	50kHz	25kHz	50kHz	25kHz
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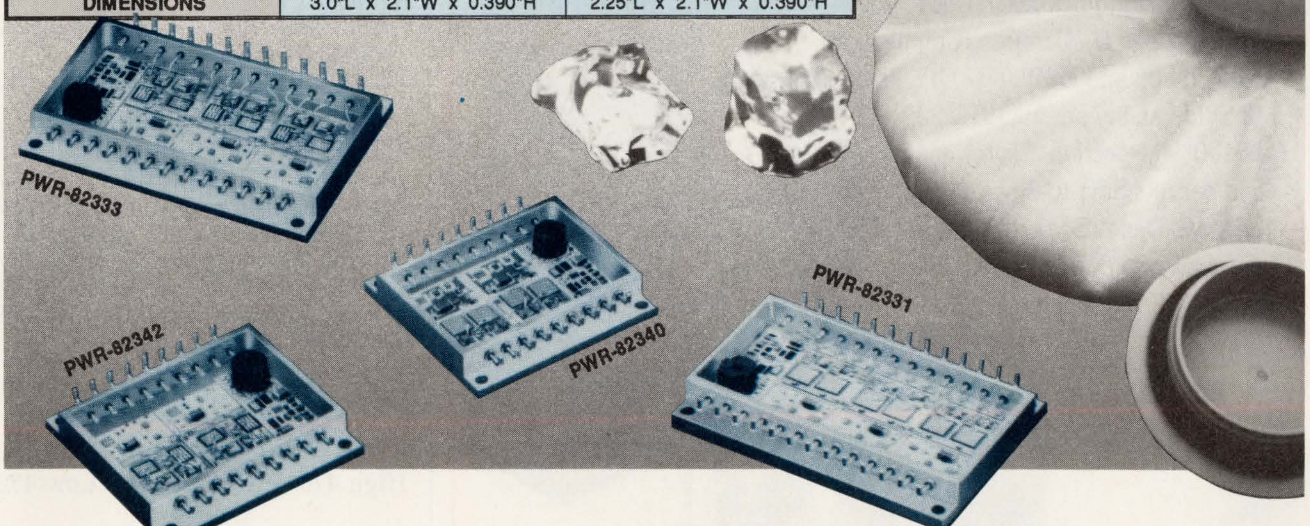

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to provide time for an orderly power-down situation in the event of a sudden loss of supply voltage. The power to delay the motor's arrest is actually generated by the motion of the motor itself. This power is stored in an external charge-pump storage capacitor that discharges to provide the spin chip with enough energy to create a braking delay that can last as long as 100 msec.

Although spin chips provide size-, weight-, and cost-reduction benefits over Hall-effect sensors, they aren't necessarily the right option for your next design. Besides their uncertain operation during motor start-up, spin chips offer no motor-positioning capability, no simple way to change rotational direction, and no speed control below a couple hundred rpm. However, these ICs are relatively new products and their manufacturers are still busy improving their performance and increasing their features. EDN

Acknowledgment

Special thanks to Denis Galipeau of Cherry Semiconductor for developing the models and data referenced in this article which illustrate the nuances of adaptive commutation.

References

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2. Philips Components, "Full-wave sensorless drive ICs for brushless DC motors," Technical Publication IC-008, June 1990.

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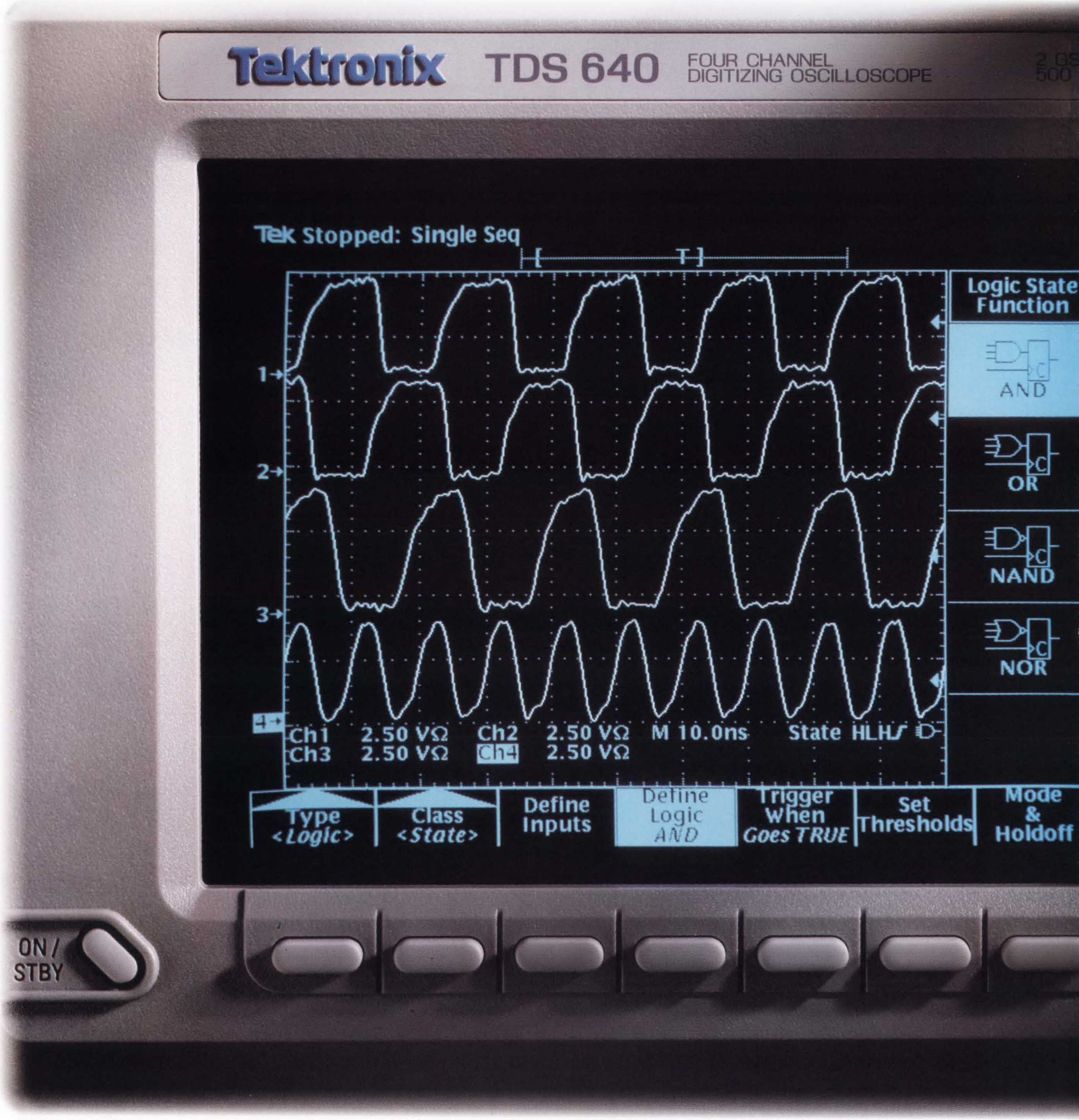
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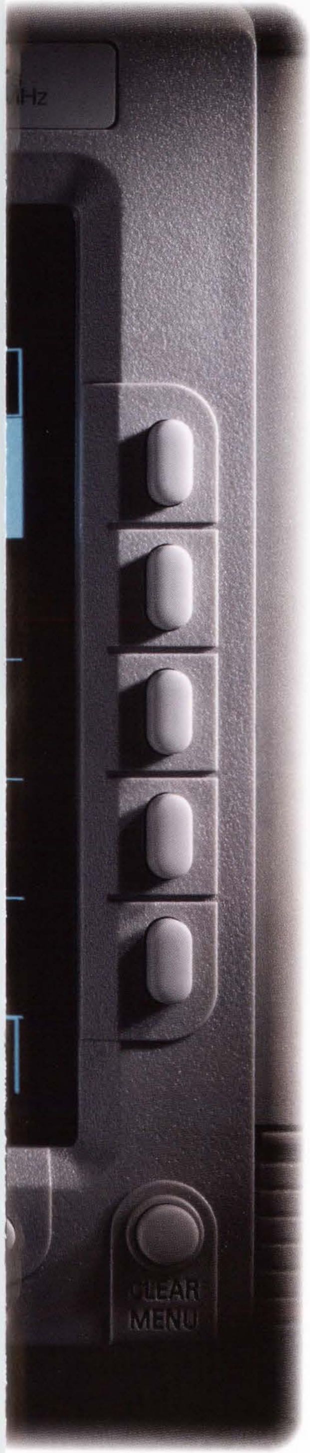

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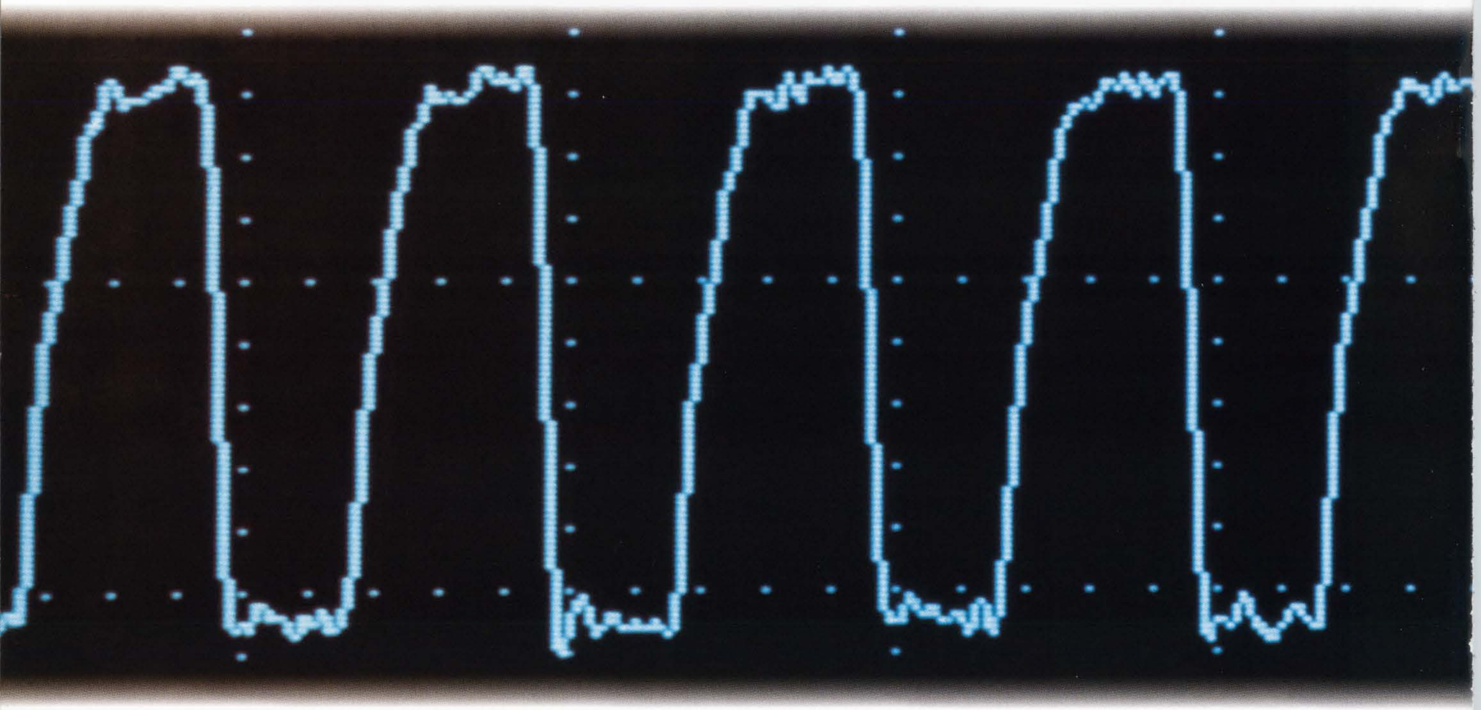

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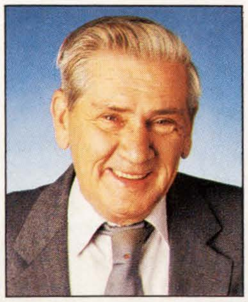
LIQUID-CRYSTAL DISPLAYS

High-resolution panels target laptop computers

DAVE PRYCE, Technical Editor



As the demand for elegant, high-performance displays increases, manufacturers are improving existing technologies and devising new ones.

The burgeoning market for large, high-resolution LCDs is driven by the demands of avionics and medical instrumentation and—most of all—the nearly insatiable appetite of laptop- and notebook-computer manufacturers. These applications require dot-matrix displays that can provide considerable amounts of information. Notebook computers, for example, typically use LCDs that provide VGA-standard resolutions of 640×480 pixels. Avionics and medical displays typically require resolutions of tens of thousands of pixels.

Although electroluminescent and gas-plasma displays compete with LCDs in high-resolution flat-panel applications (**Ref 1**), the LCD is rapidly becoming the dominant technology because of its intrinsic advantages. LCDs are thin, lightweight, rugged, and—except for backlighting—operate at low power.

From the simple twisted-nematic display, manufacturers have progressed to modern LCD fabrication technologies such as supertwist; double, monochrome, and film supertwist; and active matrix. (For an in-depth look at these technologies, see **Ref 2**.) These technologies have greatly improved the contrast and viewing angle of LCDs. The improvements, together with advanced backlighting techniques, are further strengthening the LCD's position as the flat panel of choice for large-area high-resolution displays.

Companies are devising other new technologies in addition to advanced fabrication technologies. One company, In Focus Systems, is using active addressing to drive passive LCDs. Active addressing would let passive supertwist-nematic LCDs achieve the speeds video applications require. The same company is also trying a subtractive process to achieve color LCDs. The company says this process yields brighter, higher-contrast images than does the prevalent additive process. Another company, Tektronix, is developing an active-matrix technology it calls plasma-addressed liquid crystal (PALC). PALC panels provide effective gray-scale performance at video rates and have the potential to be manufactured in large sizes.

The majority of LCDs used in laptop and notebook computers are passive-

Several sizes of color LCDs are available from Sharp Electronics. The displays include both passive and active-matrix types.

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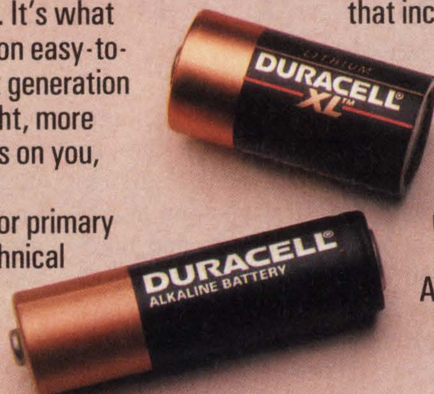

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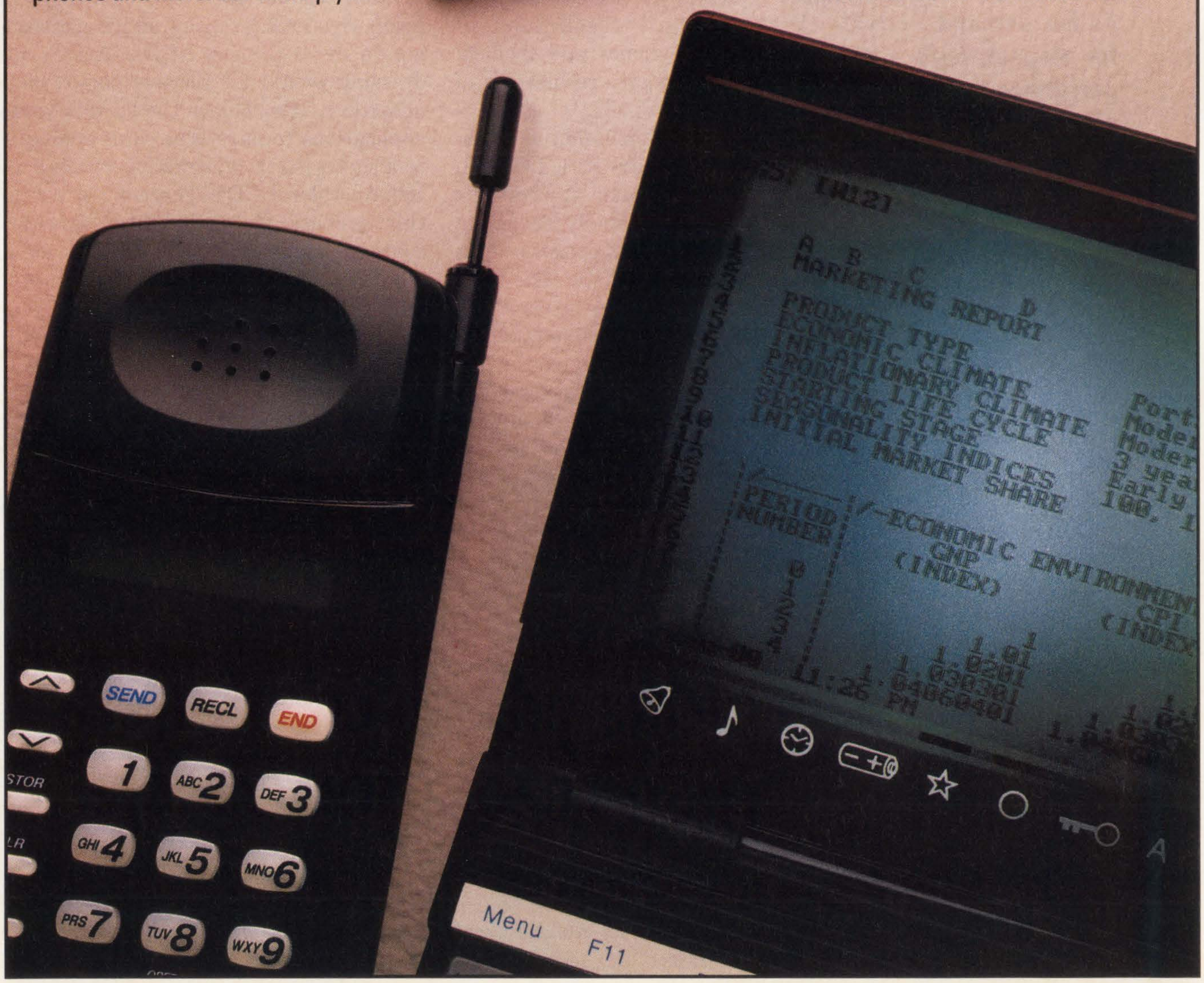

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LIQUID-CRYSTAL DISPLAYS

matrix displays. In these displays, the drive and control circuitry directly drive the rows and columns of pixels that make up the dot matrix. Although not perfect, passive-matrix LCD panels provide bright, high-contrast, high-resolution images in either black and white or color. Passive-matrix displays have the advantage of relatively low cost, which contributes greatly to their popularity.

Compared with passive displays, active-matrix displays offer the advantages of faster response times and higher contrast and brightness. In an active-matrix display (**Fig 1**), each pixel is driven by its own thin-film transistor, usually an FET made from amorphous silicon. The row and column drivers address the individual transistors to turn the pixels on or off. Although the interface circuitry for this type of display is multiplexed, an individual thin-film transistor statically drives each pixel. This arrangement preserves the simplicity of multiplexing and minimizes the resolution-contrast tradeoff associated with most passive LCD technologies.

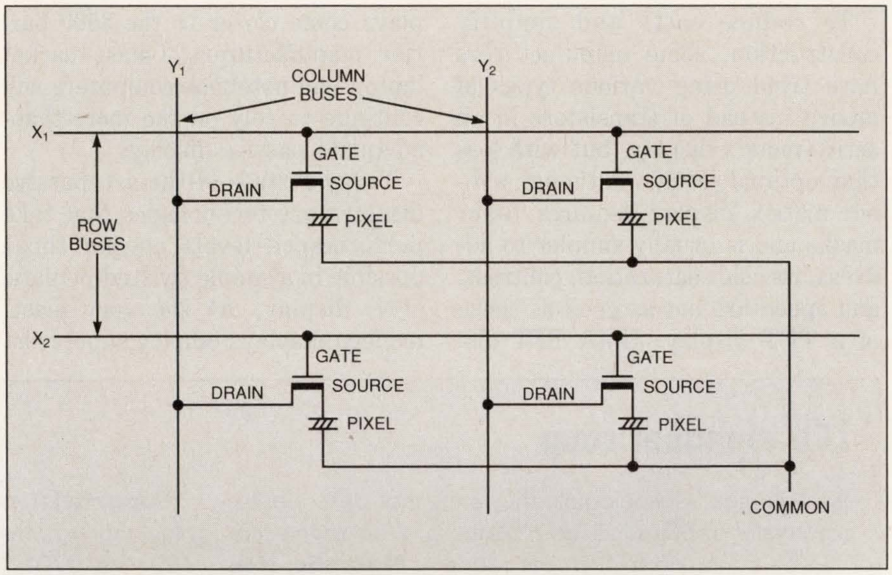

Fig 1—In an active-matrix TFT display, a thin-film transistor drives each pixel. The transistors are usually FETs connected so that the drain leads form column-selecting terminals and the gate leads form row-selecting terminals.

Active-matrix LCDs can achieve video-speed response times of less than 50 msec, brightness levels that often exceed 50 cd/m^2, and contrast ratios of 40:1 or higher. Despite such impressive performance, active-matrix LCDs suffer from a cost penalty that takes them out of the mass market. Thin-film transistor (TFT) active-matrix displays require a minimum of eight masks to produce what is analogous to a huge integrated circuit. The low yields and slow throughput for large-area TFT displays result in production costs that mandate OEM prices of about $2000 for a typical 9-in. display. Such prices eliminate these displays from the mass market, which uses passive displays that sell for well under $500 in OEM quantities.

Speed, brightness, and contrast

Speed—Depending on construction, displays vary greatly in their ability to respond to input signals. Passive displays such as TN, STN, and DSTN types exhibit a slower response than do active-matrix displays, which use thin-film transistors to control the action of the individual pixels.

Speed requirements depend on your application. For text applications on a PC, response times of 250 to 500 msec are usually satisfactory. However, if you use a mouse to drag a cursor across the screen, you'll need a response of about 175 msec to prevent smearing. For animation, an even faster response of 125 msec is desirable. For real-time video applications, a response time of 50 msec or less is mandatory. Thus far, the only liquid-crystal displays capable of video-speed response are active matrix types, which exhibit speeds in the 30- to 50-msec range.

Brightness—High-resolution displays come in a wide range of brightness levels, depending on the LCD's construction and type of backlight. Brightness is usually measured in foot lamberts or candelas/square meter (1 fL = 3.425 cd/m^2; cd/m^2 = 0.292 fL). A brightness of 25 cd/m^2 is usually adequate for most environments. Some active-matrix TFT displays exhibit a brightness as high as 60 to 80 cd/m^2.

Contrast—Essentially, the ratio of the on-pixel to off-pixel brightness. In high-resolution displays, contrast ratios range from about 10:1 to as high as 100:1. Although the way the human eye perceives contrast depends on several factors, ratios of 7:1 or higher are adequate in most cases. Above a ratio of 20:1, the eye perceives little difference.

LIQUID-CRYSTAL DISPLAYS

To reduce costs and simplify construction, some manufacturers have tried using various types of diodes instead of transistors in an active-matrix display, but with less than optimal results. Although a diode-matrix display requires fewer masks and is usually simpler to address, its color saturation, contrast, and speed are not as good as those of a TFT display. Until TFT displays come closer to the $500 barrier, manufacturers of mass-market laptop and notebook computers will continue to rely on the more-than-adequate passive displays.

Today's state-of-the-art passive displays use technologies that take performance levels beyond those possible in a simple twisted-nematic (TN) display. At the very least, modern displays employ supertwist technology (STN), and most employ advanced technologies such as double supertwist (DSTN), film supertwist (FSTN), or monochrome supertwist (MSTN). For an explanation of the various technologies, see **box** "LCD alphabet soup."

Companies such as Epson, Hitachi, Sharp, and Toshiba all offer LCD panels that use variations of these technologies to produce dis-

LCD alphabet soup

As with most technologies, the terms that describe liquid-crystal displays include a plethora of acronyms that can be confusing to first-time readers. **Nematic, (N),** which is common to most of the acronyms, denotes a threadlike structure—the typical shape of a liquid-crystal molecule. The following list defines and describes several of the most commonly encountered acronyms:

Active matrix (AM)—A type of display that contains a matrix of active elements to control the on-off state of each pixel. A few active-matrix displays use 2-terminal diodes as the active elements, but most use 3-terminal thin-film transistors to form the matrix. See TFT description.

Double-supertwist nematic (DSTN)—Similar to the supertwist LCD, a DSTN display obtains nearly twice the contrast by adding a color-compensating glass cell layer to provide an almost pure black-and-white image. The main disadvantage of a double-supertwist display is its need for a high-power backlight to compensate for transmission losses the added layer causes. The additional glass cell also increases the cost of the display.

Film-supertwist nematic (FSTN)—Similar to a double-supertwist display except for the replacement of one of the optical-compensating glass layers with an ultrathin polymer film. Compared with a double-supertwist display, a film-supertwist LCD has slightly less contrast but offers the advantages of a wider viewing angle and a lower-power backlight.

Monochrome-supertwist nematic (MSTN)—The monochrome-supertwist display replaces the expensive compensator cell of the double-supertwist LCD with an optical retarder made from a less expensive polymer material. Basically identical to the film-supertwist display in construction and characteristics, an MSTN LCD features a high-contrast black-and-white image and a wide viewing angle.

Supertwist nematic (STN)—A liquid-crystal display that rotates the plane of polarization between 180 and 270°. A simple twisted-nematic display imposes a 90° twist on the plane of polarized light passing through the display. In addition, an alignment layer in a supertwist display provides a pre-tilt of 10 to 20°. The pre-tilt and increased twist give supertwist LCDs contrast ratios as high as 10:1 and viewing angles as wide as 40°. Despite these advantages, many people find the characteristic blue tinge of a supertwist display unacceptable.

Thin-film transistor (TFT)—A display that incorporates an active matrix of thin-film transistors to control the turn-on and turn-off of each pixel. These expensive, state-of-the-art displays typically have a viewing angle of 45°, a contrast ratio greater than 40:1, and response times as fast as 40 msec. By including red, blue, and green filters, a thin-film-transistor LCD can reproduce bright, high-contrast color images.

Twisted nematic (TN)—The basic liquid-crystal display in which the material imposes a 90° rotation, or twist, to the plane of polarized light passing through the display. Conventional twisted-nematic LCDs typically exhibit a contrast ratio of 3:1 and a viewing angle of less than 20°.

In addition to these acronyms, there are others that are peculiar to certain manufacturers. For example, Epson uses the terms FTN for film-compensated STN displays and NTN for neutralized STN displays, the latter being similar to a double-supertwist display. In Focus Systems uses the term TSTN for its triple STN displays. In this case, the T for "triple" does not apply to the amount of twist but to the number of separate LCDs used in the display. No doubt other companies have—or will—generate their own acronyms to add to the confusion.

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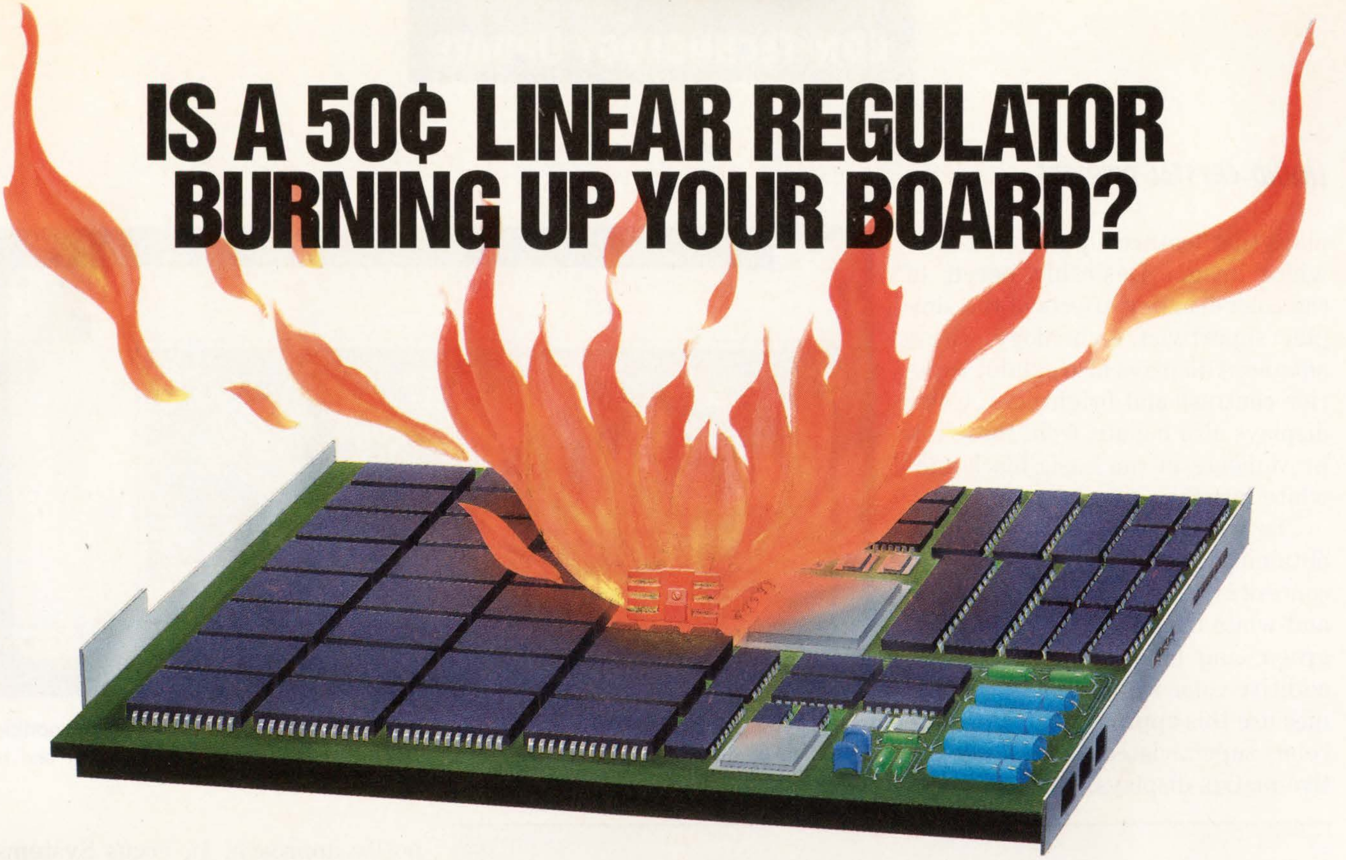

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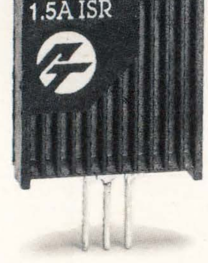

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plays that feature a pure black-and-white image. Desirably bereft of the color-fringing effects of the simpler supertwist technology, these advanced displays also exhibit superior contrast and brightness. Color displays also benefit from these improvements in the basic black-and-white image.

The widely accepted approach to obtaining color from an LCD is to concentrate first on a good black-and-white image, and then add red, green, and blue filters to form an additive color system. Most companies use this approach to make their color supertwisted-nematic or active-matrix displays. Taking the opposite approach, In Focus Systems stacks magenta, cyan, and yellow cells to exploit the inherent birefringence (coloration) of an image, using a subtractive color process much like that used in photography. The company says the subtractive process yields brighter, higher-contrast images than does the additive process.

Designed for use in palm-top computers, the TCM-9108A from Epson has a CGA-compatible resolution of 640×200 pixels. The LCD consumes 130 mW, weighs 190 grams, and is 6.3-mm deep.

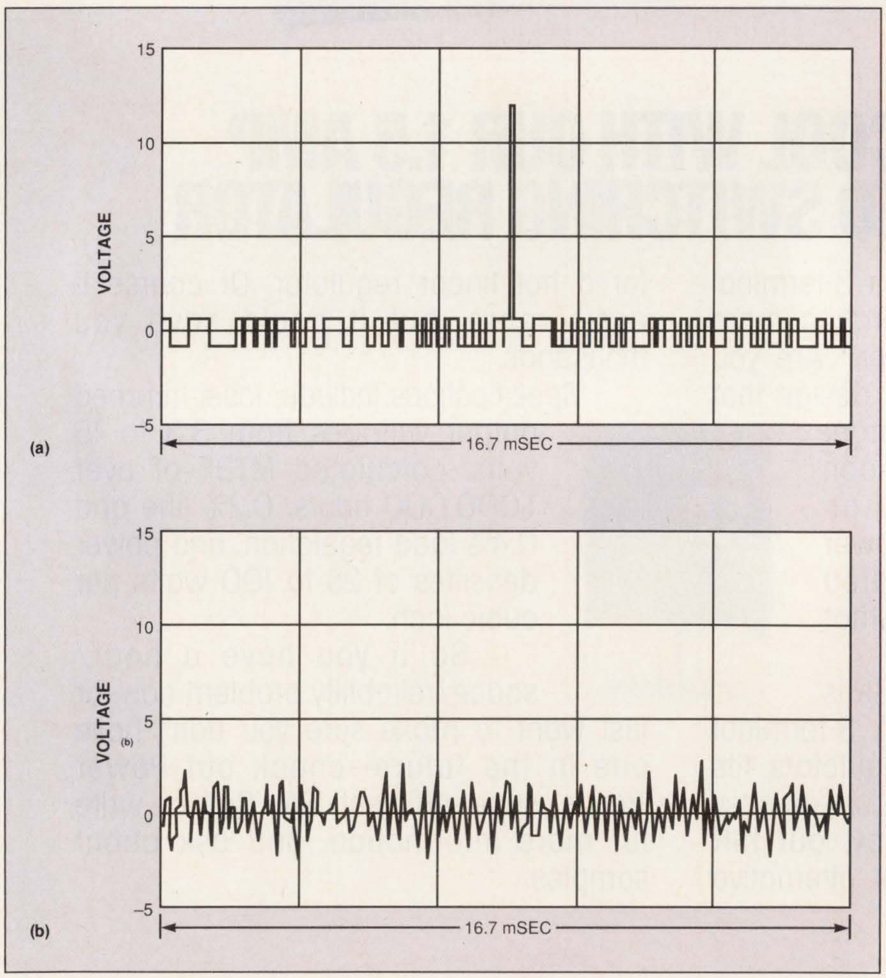


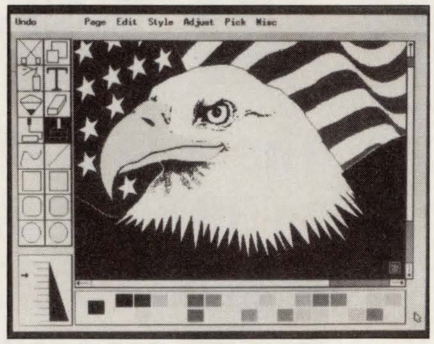
Fig 2—A technique called active addressing allows the use of fast-response liquid-crystal material in a passive display. In effect, active addressing replaces the once-per-frame pulse (a) with smaller, more constant row pulses (b). The rms voltage of both waveforms is identical. With less time between pulses, the pixel On states do not decay as rapidly and the display's contrast has the same high value as that of a slow-responding STN panel.

In Focus Systems is also working on an active-addressing scheme for passive displays that will provide the video-speed performance of active-matrix displays. Manufacturers can attain video-speed supertwist-nematic displays by using thin cell gaps and low-viscosity liquid-crystal mixtures. However, the brightness and contrast ratio of these displays are unacceptably low compared with standard, slower-responding supertwist-nematic panels. An effect known as frame response is responsible for this poor performance. Frame response is an unwanted optical transient introduced by the liquid crystal when it responds to the large row-select pulse generated by the multiplexed LCD drive instead of to the desired rms value of the pixel waveform.

Fig 2 illustrates the difference between **(a)** the standard 1/240-multiplexed addressing waveform,

which has a large row-select pulse, and **(b)** the 1/240-multiplexed pixel waveform used in active addressing. Both graphs show one 16.7-msec frame period. The rms voltage of **Fig 2a** is identical to that of the standard LCD drive waveform of **Fig 2b**. In effect, active addressing replaces the once-per-frame pulse with smaller, more-constant row pulses. Because less time elapses between pulses, the pixel On states do not decay as rapidly and the display's brightness and contrast ratio have the same high values as those of a standard, slower-responding supertwist-nematic panel.

Although standard products are not yet available, In Focus Systems has used active addressing in a 240×240-pixel supertwist-nematic prototype display that exhibits bright, high-contrast images at video rates. Active addressing requires a sophisticated algorithm that allows the simultaneous driving of multiple rows and columns to provide exact control over any pixel without loss of contrast. One of the keys to producing commercial active-addressing products is reducing the software algorithm to silicon as part of the driver circuitry.



The TLX-1832S-C3M black-and-white display from Toshiba features a VGA resolution of 640 × 480 pixels, a brightness of 50 cd/m^2, and a contrast ratio of 12:1. Using flexible TAB (tape-automated-bonding) driver chips, which fold behind the display area, reduces the panel's overall dimensions to little more than the size of the LCD glass.

Tektronix is looking into an active-matrix technology it calls plasma-addressed liquid crystal (PALC). Using this technique, the company has built a 5×5-in. display containing 90,000 pixels arranged in a 300×300 array. Progressively scanned lines are addressed at 35 kHz and updated at 67 Hz. The panel provides gray-scale performance at video rates. According to Tektronix, PALC advantages include reduced row-driver count, a low column-driver capacitive load, a wide operating voltage range, and the potential for manufacture in large sizes.

As evidenced by the high-quality displays now appearing in laptop and notebook computers and in other applications, manufacturers of large-area, high-resolution LCDs are clearly making significant

Table 1—Representative liquid-crystal displays

Company	Part Number	Image	Screen size (in.)	Resolution (pixels)	Comments	Unit cost
Epson America Inc.	TCM-A9108	Black and white	7.4	640×200	Low-power palm-top computers.	$240
	EG-9005DNS	Black and white	10.3	640×480	PCs, POS terminals.	$444
	EG-0101NLW	Black and white	13.1	1024×768	PCs, workstations.	$1436
Hitachi America Ltd	TM26D01VC	Color (TFT)	10.3	640×480	50-msec response, 80-cd/m^2 brightness.	$3200
	LMG5261	Black and white	9.5	640×480	Uses Micro-tab construction to minimize order size.	$500
	LMG9060	Black and white	10.0	1024×768		$1200
In Focus Systems	LCD1600M	Color	10.5	640×480	Uses subtractive birefringent effect.	$1400
	LCD5000M	Color	10.5	640×480	Uses three color cells: magenta, yellow, cyan.	$2050
	1600-GS	Black and white	N/A	640×480	Projection panel, 16-level gray scale.	$1695
	7600-XGA	Color	N/A	1024×768	Projection panel, uses three color cells.	$7995
	TVT-3000	Color (TFT)	N/A	640×480	Projection panel, 100:1 contrast.	$5995
Optical Imaging Systems	CT4040	Color (TFT)	5.6	1024×768	Industrial/military grades; 4-in. square, 40:1 contrast.	$9800 to $11,800
Sharp Electronics Corp	LQ9D011	Color (TFT)	8.4	640×480	512 colors, 80-msec response time, 60-cd/m^2 brightness.	$3550
	LM64C031	Color	8.5	640×480	Eight colors, 550-msec response time, 40-cd/m^2 brightness.	$1695
Toshiba Electronic Components	TLX1832S-C3M	Black and white	9.7	640×480	Depth=6.5 mm, weight=320 grams.	$506

Note: NA = Not applicable; POS = Point of sale.

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strides. Screens are brighter and have higher contrasts than previously possible, and OEM costs—at least of passive displays—are meeting the needs of the mass market. Moreover, expected yield improvements in TFT active-matrix displays, new means for generating color, and new drive methods hold promise for the future. EDN

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Article Interest Quotient
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High 482 Medium 483 Low 484

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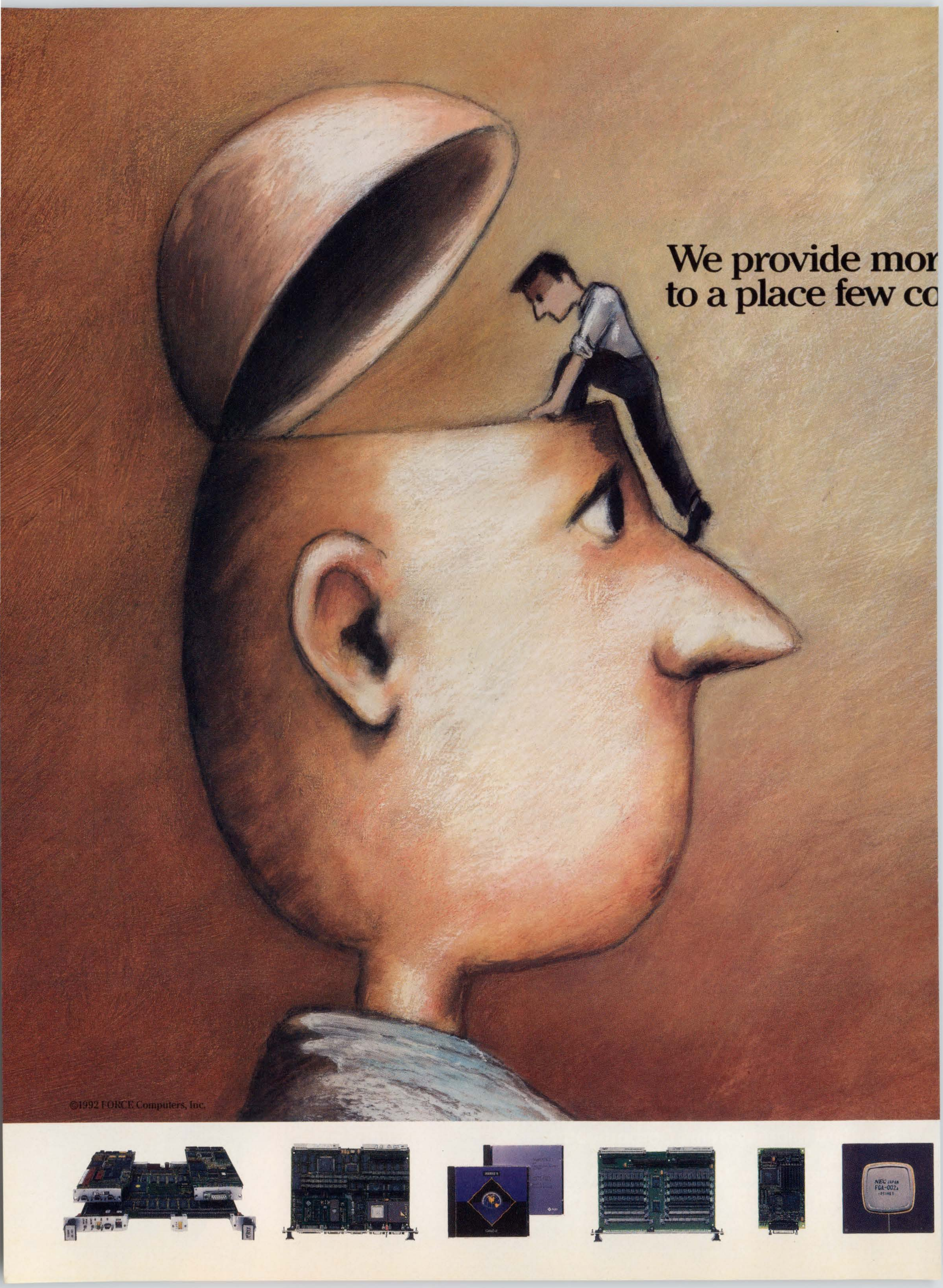
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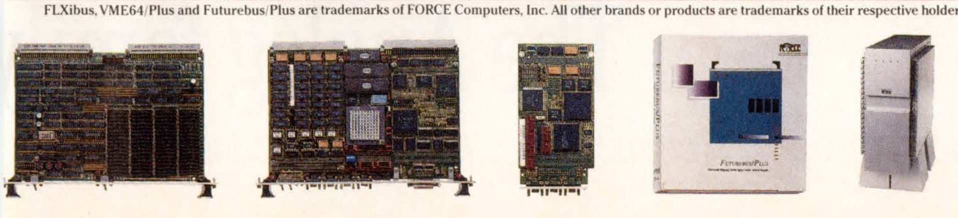

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Whether it's current noise or voltage noise you're concerned about, there's a simple way to make sure your system keeps humming along. Get your low noise op amps from Analog Devices.

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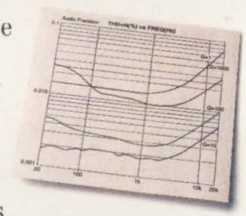

THIS WILL MAKE MEDICAL EQUIPMENT DESIGNERS FEEL BETTER.

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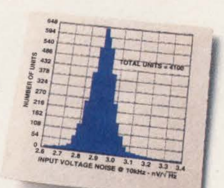

For those who want low voltage noise, but not at the expense of current noise, the AD743 and the

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ormance of your entire system.

higher speed AD745 offer the best combination of specs — 3.2 nV/√Hz and 6.9 fA/√Hz. If your emphasis is vice versa, then the AD645 has the specs you want — 0.6 fA/√Hz for current noise, and 9 nV/√Hz for voltage noise.

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The world's lowest current noise (0.11 fA/√Hz) monolithic op amp, the AD549, has 60 fA of input bias current — which is ideal for interfacing with very high

Model	Voltage Noise nV/√Hz @1 kHz typ	Current Noise fA/√Hz @1 kHz typ	Vos mV max	Supply Current mA typ	Input Bias Current max	SR V/μs typ
AD829	2.0	1.5	0.5	5	7 μA	230
OP-27/OP-37	3.0	400	.025	3	40 nA	2.8/17
AD743/745	3.2	6.9	0.5	8	250 pA	2.8/12.5
OP-275 (dual)	6	1500	1	4	350 nA	22
AD645	9	0.6	0.25	3	1.5 pA	2.0
AD712 (dual)	18	0.01	0.7	5	75 pA	20
AD548/648 (dual)	30	1.8	0.25/0.3	.34	10 pA	1.8
AD549	35	0.11	0.5	.60	60 fA	3

impedance sources. The AD548 (single) and AD648 (dual) deliver low bias current (10 pA), extremely low current noise (1.8 fA/√Hz) and low power consumption at a highly attractive price. And the industry-standard OP-27 and OP-37 offer ultralow noise (3 nV/√Hz at 1 kHz) and precision dc performance.

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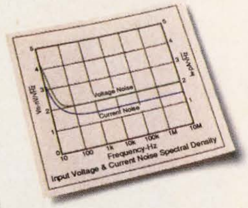

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Or for more information on our low noise op amps, write to Analog Devices, P.O. Box 9106, Norwood, MA 02062-9106.

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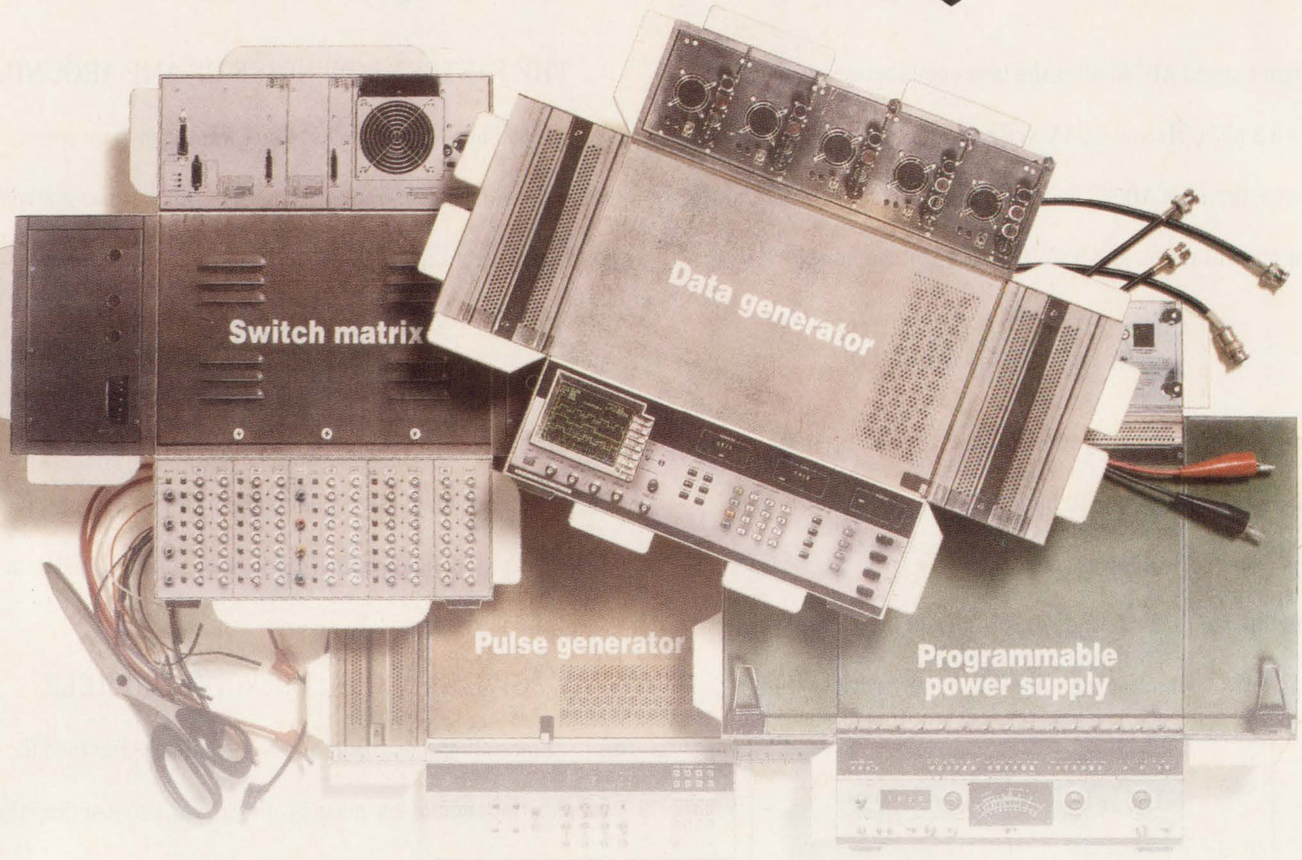

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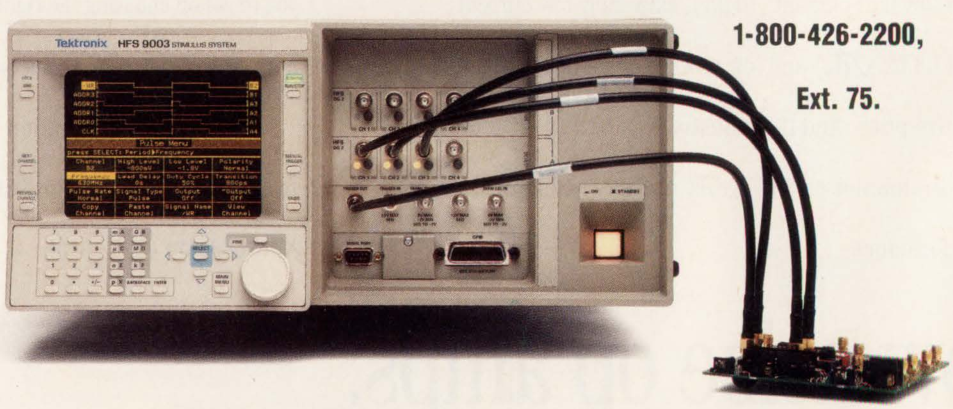

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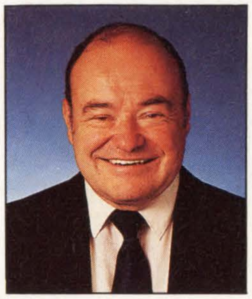
CIRCLE NO. 48

85W-188515

CONTROL-SYSTEM SIMULATION

Simulation software gains sophistication

JOHN GALLANT, Technical Editor



Control-system simulation has come a long way since the seventies. State-of-the-art simulation packages are now refined enough to model the complexities of the real world.

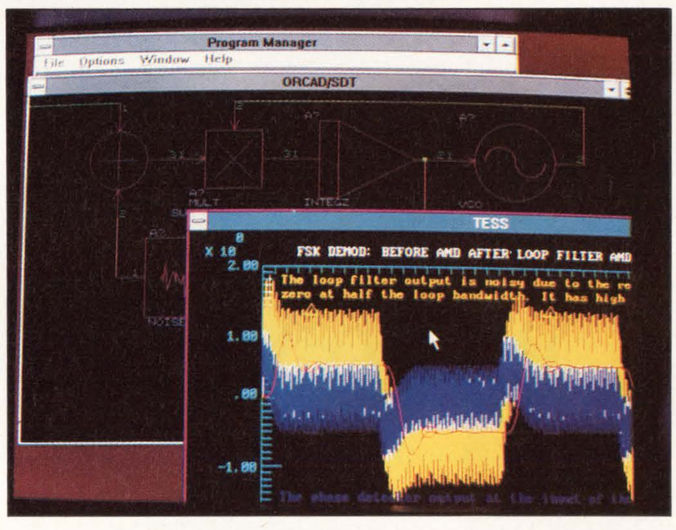
Until recently, you were lost—or destined to do an awful lot of extra work—if you needed to simulate conditions not present in the idealistic electronics world. Now, however, control-system simulation packages are acknowledging the needs of those of us who have to design electronics for the real world. Although these packages aren't ready to replace the engineers who use them, they are providing the means to compensate for the vagaries of reality.

Computer simulation used to require writing a program in Fortran or assembly code. To modify the model, you often had to write and debug new code before you could even perform the simulation. Today's control-system simulation packages remove this drudgery and let you concentrate on the task of computer modeling.

Modern simulation packages let you interconnect block diagrams on a workstation terminal. They let you employ multiple inputs and outputs that can have multiple feedback loops. Their simple command structures let you run time-domain, FFT, and logic-analysis simulations. If you don't like the results, a few keystrokes or mouse clicks modify the model so you can rerun the simulation until you get it right. Control-simulation software packages are making it easier for you to conceptualize and analyze designs before committing them to hardware.

However, computer simulation is still an art. The computer doesn't do all of the work for you—you have to make informed judgments and give the computer what it needs to run a worthwhile simulation. You have to create a block-diagram model that is complex enough to simulate real-world conditions, yet not so complex that it makes analysis difficult.

To help you create suitable baseline models, modern simulation packages have libraries of familiar control blocks such as summers, amplifiers, multipliers, differentiators, integrators, and filters. In addition, these libraries have more complex blocks to simulate nonlinear functions and other real-world nasties (ie, conditions that are difficult to simulate on a computer). These packages also have means for you to create user-defined blocks to simulate conditions not covered in the libraries.



You can model a phase-locked-loop FSK demodulator using an optional OrCAD schematic editor and Tesoft's Tesla simulator running under Windows 3.0.

CONTROL-SYSTEM SIMULATION

Consider Tesla from Tesoft Inc. The $695 Tesla simulator software package runs on a computer with an 80286 µP or better; 640 kbytes of RAM; an EGA, CGA, or Hercules monitor; and DOS version 2.1 or later. Tesla lets you interconnect analog and digital blocks using a command-line format **(Fig 1b)** similar to Spice. Digital library functional blocks include logic gates, flip-flops, phase-frequency detectors, adders, counters, and 1-shot multivibrators.

Fig 1a shows a block diagram of an FM modulator driving a phase-locked loop (PLL) demodulator. The modulator consists of a 1-kHz square-wave function generator (FCNGEN) driving a VCO centered at 100 kHz. The PLL consists of a multiplier, an integrator with a built-in zero (INTEGZ), and a VCO. The control voltage of the VCO also drives a 4-pole Chebyshev lowpass filter (CHEBL) to produce the demodulated output voltage.

Fig 1b is a Tesla-language circuit file for the model shown in **Fig 1a**. Each line begins with an element name to define the block. The next two numbers in the line define the input and output nodes, respectively, for the block. Following the block's functional name, you assign a series of parameters to characterize the block. You can insert online comments after a semicolon.

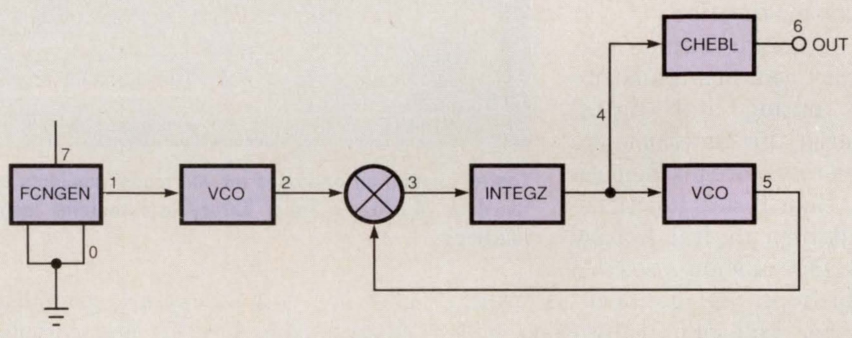
The package's analog functional blocks include VCOs, logarithmic amplifiers, rectifiers, voltage comparators, phase modulators, sample and hold, A/D and D/A converters, multiplexers, and demultiplexers. A delay function lets you simulate time delays required for a µP to calculate a control algorithm.

After writing a netlist that interconnects the model's blocks, you can use a range of simulated test and measurement equipment to analyze the model. Tesla's test equipment includes a bit-error-rate generator, a 5-function sweep generator having AM and FM, a Gaussian noise source, a sine-wave oscillator with phase adjustment, and a pulse generator. Measurement equipment includes a bit-error-rate checker, an rms voltmeter, and a coherent phase meter.

A "NONLIN" command lets you generate a piecewise linear transfer function by defining as many as 10 input-vs-output voltage pairs. The function lets you model dead bands in bang-bang control systems as well as voltage-limiting characteristics. In addition, version 1.1 of Tesla, which was released in March of 1991, has a general-purpose mixer block that models intercept points and LO (local oscillator) and RF feedthrough. An RF amplifier block includes the 1-dB compression point and second- and third-order intercept points.

Tesla can interconnect as many as 9999 nodes. A "Plot 1 2" command plots the voltage at nodes 1 and 2, and "Plot M1 M2" plots the FFT of the waveforms at both nodes. You can save simulation data on your hard-disk drive and restore the data for future analysis. If you're proficient with Microsoft's Fortran version 4.1 or later, an optional $495 MODGEN package lets you create user-defined blocks, which Tesla compiles as additions to its library.

An optional $195 OrCAD/SDT package lets you capture a schematic created using OrCAD. The package contains a library of Tesla icons that mirror the blocks in Tesla's library. You interconnect the icons using a mouse when running OrCAD. After creating a block diagram, the package generates a Tesla circuit file for simulation under Tesla.



(a)

```
*
*       DEMO CIRCUIT - FM MOD, PLL DEMOD
*
F1 0 0 1 7 FCNGEN FCN=2 V=.5 F=1E3   ;1KHZ SQUARE WAVE
V1 1 2 VCO V=1 W0=6.283E5 K0=6.28E4  ;F0=100KHZ, KV=10KHZ/V
M1 2 5 3 MULT
I1 3 4 INTEGZ T=40E-6 FZ=FZERO       ;TIME CONSTANT=40USEC
V2 4 5 VCO V=1 W0=6.283E5 K0=6.28E4
C1 4 6 CHEBL N=4 F=7E3 RIP=.1        ;4 POLES, 7KHZ CUTOFF, .1DB RIPPLE
```

(b)

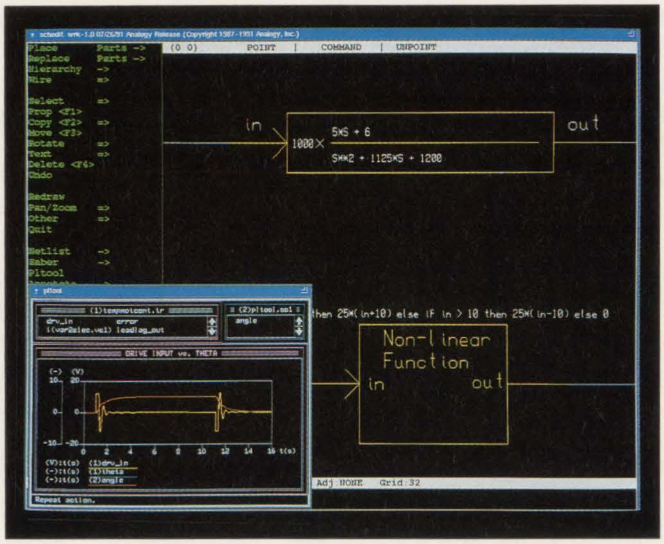
Fig 1—This FM modulator and phase-locked-loop demodulator block diagram (a) has a Tesla circuit file (b) that bears a remarkable likeness to a Spice circuit file.

Tutsim, from Tutsim Products, runs on a DOS-compatible computer with an 8088 µP or better. The simulation package runs with a CGA, EGA, or Hercules monitor and requires 512 kbytes of RAM for the $695 professional version. The package displays the time or transient responses of block-diagram models. A companion $445 Fansim package, which requires an additional 384 kbytes of RAM, provides analyses in the frequency domain. Fansim not only generates FFT and Bode responses, but can take the ratio of two FFT functions to calculate the poles and zeros of the intervening transfer function.

Although Tutsim's library contains a mixture of analog and digital blocks, its functions are innately more mathematical than Tesla's functions. Tutsim's digital library consists of logic gates and flip-flops you connect to create higher-scale digital functions. Tutsim's baseline functions include summers, amplifiers, differentiators, and integrators. The package also defines a variety of z-transform functions. These functions let you construct digital filters and as many as seven embedded μPs to calculate control algorithms.

Tutsim's signal-source blocks include a pulse generator, a sinewave oscillator, random noise, and a chirp waveform. Flow-control functions include conditional if-then-else, conditional switching, and conditional latching. Real-world control functions include electrical resistance, capacitance, and inductance; a proportional-integral-derivative (PID) controller; magnetic hysteresis; gear backlash; variable time delay; and a gear-ratio algorithm. You can supply input-vs-output voltage pairs to simulate a nonlinear function in a piecewise linear manner.

You can also create user-defined blocks using an optional $435 C-language or $900 Fortran-language package. An optional $149 OrCAD SDT IV package passes a symbol table of Tutsim's blocks to OrCAD, allowing you to capture graphical models using OrCAD and compile them in a Tutsim circuit file. If you've ever seen mathematical models created for analysis by an analog computer, then an OrCAD model of Tutsim on a terminal will probably look pretty familiar.



Control-simulation packages let you model nonlinear and s-domain functions. Analogy's Saber library also contains many real-world functions.

If you have access to a Sun-4, SPARC, DEC VAX, or an HP 9000 series 300 or 400 workstation, you may want to consider The Math Works' Simulab ($3995) for control-system simulation. Simulab is a shell for the company's Mat Lab numeric computation system. Mat Lab features extensive math functions, 2-D and 3-D graphics, and optional specialized analysis toolboxes. Because Simulab runs under the OSF/Motif X-Windows graphical user interface, you can interconnect graphical block diagrams or differential equation models by pulling down icons with the point and click of a mouse. Versions are also available for Microsoft Windows 3.0 and the Macintosh computers.

Simulab's block library contains linear and nonlinear blocks for both continuous and discrete time analysis. Signal sources include function generators and Gaussian noise sources. You can obtain a time-response reading at any node or pass the node's data into a Mat Lab file for analysis. The models employ report-quality graphics, which you can paste directly into a word-processor or desktop-publishing program.

Simulab simulates nonlinear dynamic equations by linearizing the canonical state-space equations

$$x = Ax + Bu$$
$$y = Cx + Du$$

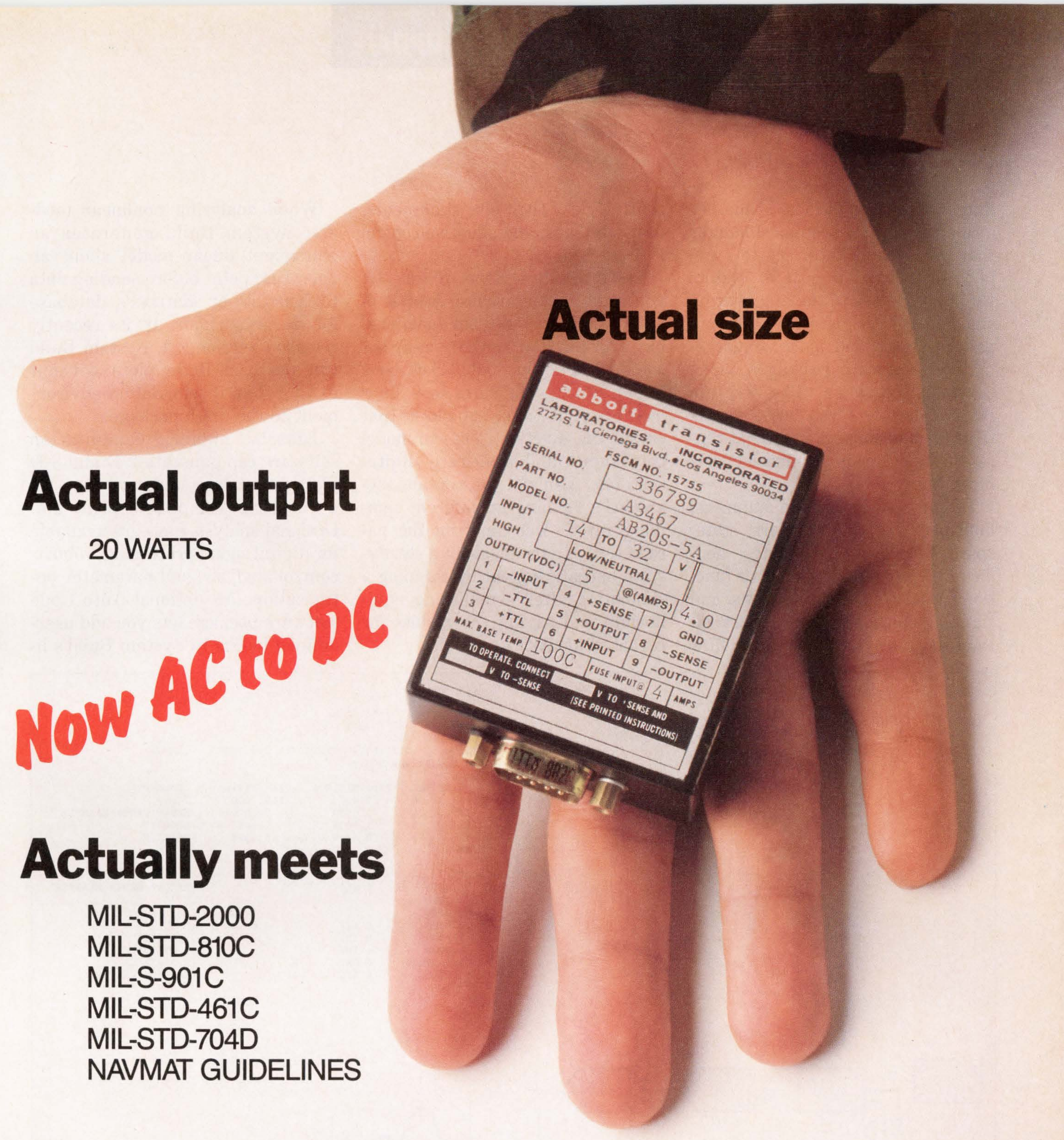
about a specified operating point. Because you can easily interact with Simulab's block diagram, you can change the model's parameters to investigate the effect of different parameter values on a simulation.

Simulab lets you trim parameters about a steady-state condition. The feature makes repeated analysis easier by eliminating the long run time for a simulation to reach its steady state. You specify initial condition vectors and variables that must match to simulate the steady-state condition. You can also create hierarchical models based on groups of blocks for top-down or bottom-up designs.

Make your own blocks

You can extend Simulab's block library by creating user-defined blocks using C- or Fortran-language programs or using standard Mat Lab M-files. You can also store models in standard Mat Lab M-files for porting among different computers. Simulab can also access Mat Lab's optional toolboxes, which perform robust-control analysis, parametric optimization and analysis, digital signal processing, and piecewise curve fitting using spline polynomials.

System Build from Integrated Systems Inc, starting at $9000 for



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CONTROL-SYSTEM SIMULATION

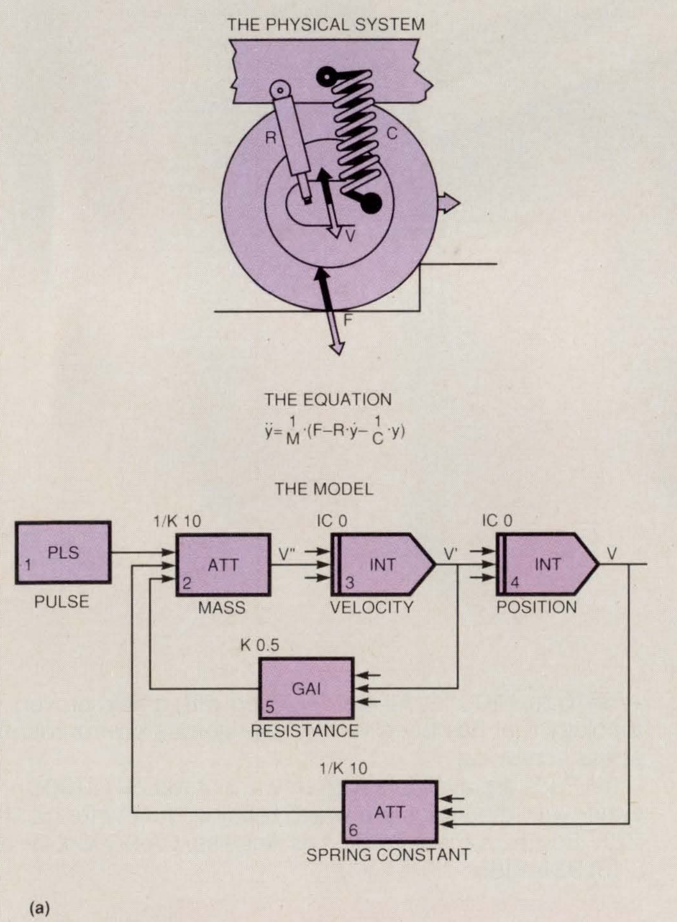
Sun or HP workstations, is another graphical control-system simulator that provides an interface to a numeric computation system. System Build has access to the engineering analysis and design tools of the company's Xmath and Matrixx mathematical software packages via a common database. The System Build editor lets you use a mouse to select and connect icons that represent functions in a comprehensive block library.

Library blocks include summers, multipliers, PID controllers, state-space equations, logic gates, nonlinear elements, trigonometric functions, transcendental functions, and signal generators. A state-transition-diagram block manages flow control via if-then-else statements, decision trees, and adaptive control logic.

The program's "Super Blocks" let you combine hierarchical models of many sub blocks into one functional block for top-down or bottom-up designs. When you double-click on a Super Block, you move to a finer level of detail, to the sub blocks that create the function. You can model continuous and multirate digital systems. A model can contain several μPs running at different sampling rates. You can trim the parameters of a model about a steady-state operating point by stopping a simulation after establishing equilibrium and saving the results for repeated analysis.

When analyzing nonlinear models, System Build generates an equivalent linear model about an operating point before sending data to Xmath's or Matrixx's database for linear analysis. In its recently released version 2.4, System Build can perform Bode plots without exiting from its simulation environment to the math package.

Xmath's numeric computation software can generate 2-D and 3-D plots for analysis and hard copy via a Postscript-compatible print file. Optional analysis tools are available for digital signal processing, robust-control analysis, and parameter optimization. An optional Auto Code software package lets you add user-defined blocks to System Build's li-

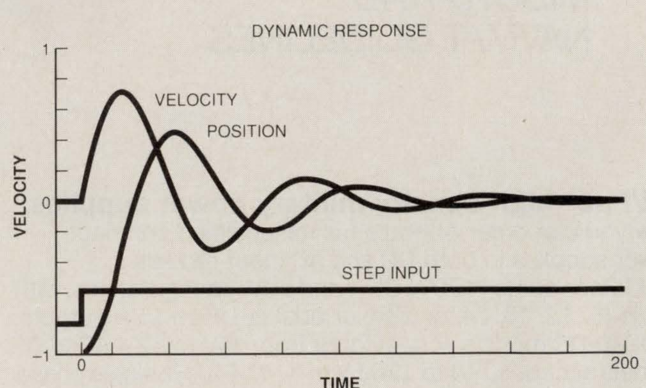


(a)

```
Model File : TUTWAY.SIM
Date:  02 / 28 / 1989
Time:  16 : 51
Timing:    0.5000000 ,DELTA  ;  200.0000    ,RANGE
PlotBlocks and Scales:
Format:
     BlockNo, Plot-MINimum , Plot-MAXimum ;  Comment
Horz:     0 ,    0.0000    ,  200.0000    ; Time
  Y1:     1 ,   -1.0000    ,    9.0000    ;SECOND ORDER EXAMPLE
  Y2:     3 ,   -1.0000    ,    1.0000    ;VELOCITY
  Y3:     4 ,    0.0000    ,   20.0000    ;POSITION
  Y4:       ,              ,              ;

MODEL:
  10.0000        1 PLS                     ;SECOND ORDER EXAMPLE
 200.0000
   1.0000
  10.0000        2 ATT      1     6    -5  ;MASS
   0.0000        3 INT      2              ;VELOCITY
   0.0000        4 INT      3              ;POSITION
   0.5000000     5 GAI      3              ;RESISTANCE
  10.0000        6 ATT     -4              ;SPRING CONSTANT
```

(b)



(c)

From a physical system, you can derive a differential equation that you can convert into a model (a) using a simulation package. This Tutsim program listing (b) produces the dynamic response (c) for the mathematical model for a second-order equation.

CONTROL-SYSTEM SIMULATION

brary via algorithms written in C, Fortran, or Ada languages.

Although these control-system simulation packages are flexible enough to model most conditions, simulating many workaday components requires some effort. For example, if you want to simulate a dc motor, you must generate a feedback macro that includes all of the motor constants such as armature impedance, torque constant, back-EMF constant, damping, and moment of inertia. It would be nice if feedback macros for common system components were included in libraries.

The template library for Analogy Inc's Saber simulator offers a large selection of building blocks that model real-world components. To simulate a dc motor, you simply call a dc-motor template that accepts all of the motor constants in SI or English units. You can stipulate the beta, saturation current, transit time, and junction capacitance of a bipolar transistor template to simulate an often-used transistor such as a 2N2222. A single-pole, double-throw relay template includes the effects of pull-in and drop-out voltage, relay coil resistance and inductance, and the "make" and "break" times for contact switching.

Saber's extensive library is primarily oriented toward automotive and aerospace designs. A mixture of analog and digital blocks matches the capabilities of the aforementioned simulation packages. In addition, functional blocks simulate mechanical, electrical, hydraulic, and optical devices such as nonlinear electromagnetic devices, wires, fuses, A/D and D/A converters, optical encoders, and lamps. Saber runs on a Sun, HP 9000, or DEC workstation and costs from $15,000 to $100,000.

In September of 1991, Analogy Inc introduced an analog hardware description language (AHDL) that replaces the company's MAST modeling language for creating custom control blocks. The $1950 graphical AHDL package, called Design Star, features pop-up menus and schematic capture. Design Star lets you describe Saber's 4500 simulation and control blocks in the time, s, and z domains.

Mix functions and circuits

All of the simulation control packages mentioned here have extensive block libraries that permit functional system analysis. Once you're satisfied with a system's response, you still must translate a design to hardware. The $30,000 Mixed Signal Simulator from Contec allows you to model analog portions at the functional level and at the circuit level using the company's version of Spice—Contec-Spice—on a Sun workstation. A model can mix transfer functions for behavioral modeling and a Spice circuit description to evaluate a circuit design's effect on the system's response. The ability to mix functional blocks with circuit blocks can reduce the simulation time for circuit analysis.

Control-system simulation packages aren't limited to just modeling engineering and physical systems. For example, a business application could be an economic model that includes the cyclic effects of demand, production delays, and accumulated inventory. You could even employ feedforward loops to model the impact of planning or forecasting. Although these software packages are flexible enough to provide analysis for a variety of disciplines, the numerical results are only as good as the simulation. The tools still require users competent enough in their particular discipline to delineate and include all the important effects of the real world. EDN

For more information . . .

For more information on the control-system simulation packages discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you read about their products in EDN.

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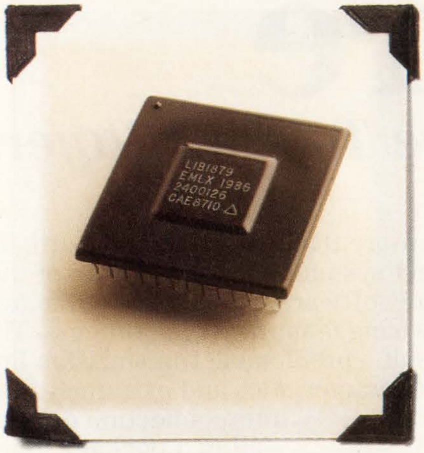
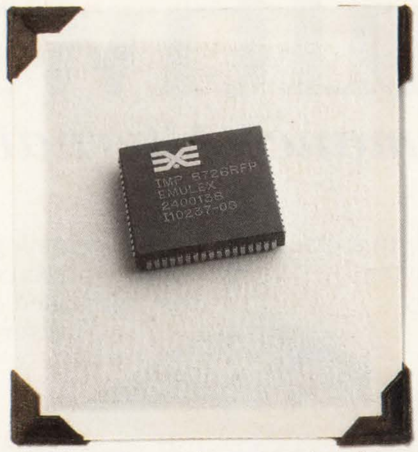
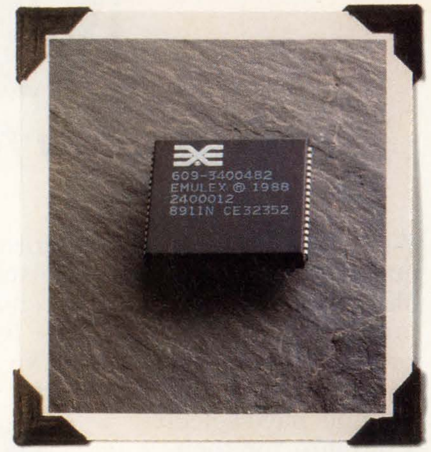


1986-MAC100. We introduce a combined disk formatter and buffer controller in a single disk controller chip.



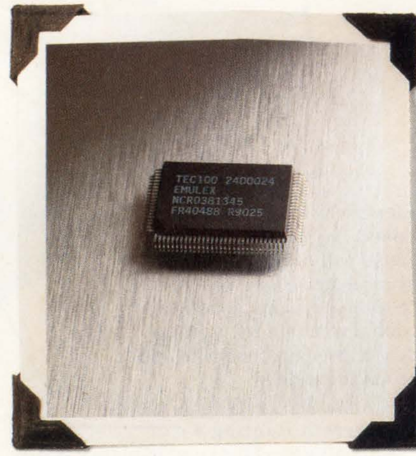
1987-ESP100. The industry's first high-performance SCSI chip is born at Emulex.



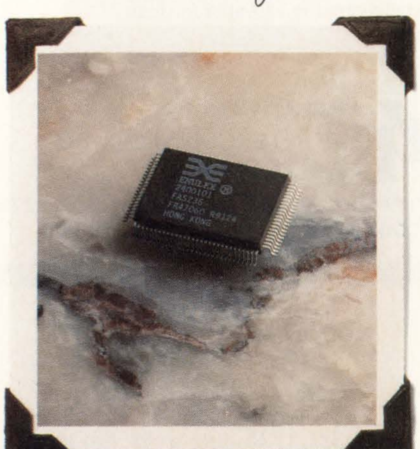
1988-ESP200. Second-generation SCSI arrives with SCSI-2 support and Parity Pass-Through.

1988-MAC200. Our advanced merged architecture controller is the first to include an automated Data Flow feature for faster data handling.

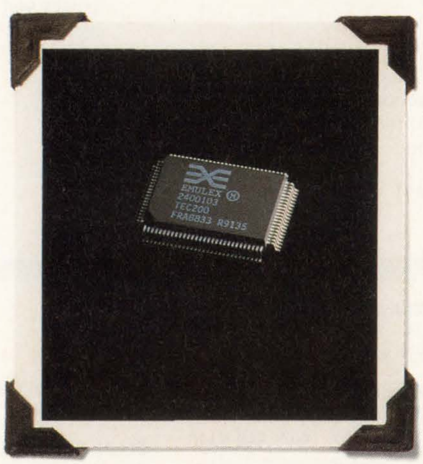
1989-BC200. A dynamic 4-Port DMA controller for DRAMs is created.



1989-TEC100. EMD combines disk, buffer, and SCSI controllers in a single chip.



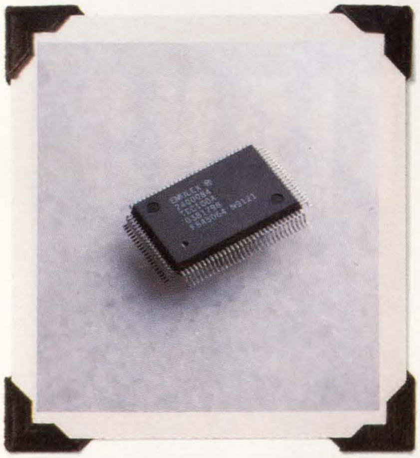
1990-FAS236. We deliver the first Fast SCSI chips with a 16-bit DMA Port.



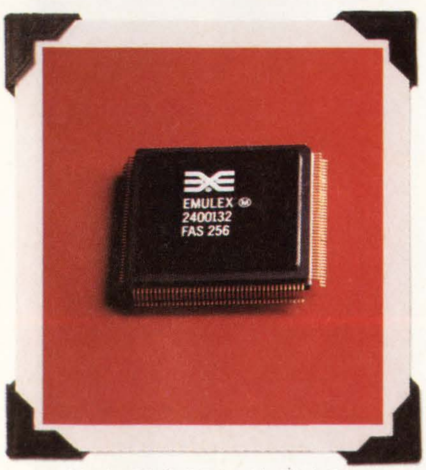
1991-TEC 200. Our second-generation TEC becomes the industry's first Fast single-chip disk controller.

1991-TEC256. The first Fast and Wide SCSI disk controller also boasts the fastest disk data rate and highest system bandwidth.

1988-ESP2X6. We give SCSI a 16-bit split-bus architecture for greater efficiency and throughput.



1990-TEC 100A. Mid-to-low capacity SCSI drives get a reduced-price version of the TEC100.



1991-FAS256. 16-Bit Fast and Wide SCSI brings SCSI-2 support to host adapters and peripherals including drive array applications.

1992-Emulex Chips. A whole new generation of firsts is due.

WE CREATED A FAMILY OF FIRSTS. WE'RE NOT DONE YET.

In all honesty, we've been building a history of innovative microcontroller products for disk and system applications right from the start.

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We've continued to lead the evolution of SCSI power—in speed, single-chip integration, full SCSI-2 support, Fast and Wide architecture, and more. Plus, we've created matching disk controller and buffer controller devices.

And now we're preparing to launch a new generation of products—a whole new family of microcontrollers...to again pioneer new industry standards in SCSI and other bus interfaces.

Look for our announcements to start soon.

Or if you can't wait, call us. We'll send you a preview of the big picture—so you can begin to spec for the future...*now.*

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CIRCLE NO. 54

THE SHOCKING REASON THE TELECOMMUNICATIONS INDUSTRY TURNED TO OMRON.

Recently, the telecommunications industry needed a new breed of low-signal relay — a relay that could withstand a shocking 2,500 volts, almost double the present standard, yet small enough for dense PCB mounting. They turned to Omron.

Omron responded with the G6N relay. It not only withstands a 2.5KV surge between coil and contacts, its footprint is almost 40% smaller than the previous standard. The G6N is the latest product to join Omron's family of low-signal relays for telecommunications, computer peripherals, office automation and more.

Why did the telecom industry turn to Omron? Because we not only have the broadest line of relays, switches and photomicrosensors in the industry, we also have a proven

track record of innovation. Last year alone, we invested over $170 million in R&D, employed over 1,000 R&D engineers and introduced nearly 100 new products. The telecom industry was also impressed with our highly-automated manufacturing systems, which enable us to provide products of consistent quality in high volumes. The G6N, for example, undergoes 100% automated inspection on 13 critical performance parameters.

With more than 90 affiliates and subsidiaries, 1,500 sales locations and 17,000 employees worldwide, Omron also met the telecom industry's need to provide product and service support around the globe.

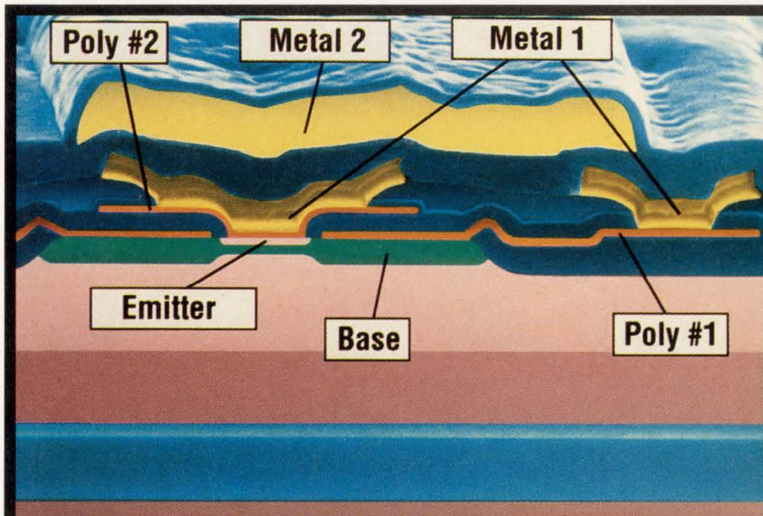
Omron's ability to meet the rigorous demands of the telecom industry may come as a shock to some people. But it effectively demonstrates our ability to meet the control demands of any industry, both now and in the future. For complete information on our broad line of control components, call us at 1-800-62-OMRON.

OMRON®

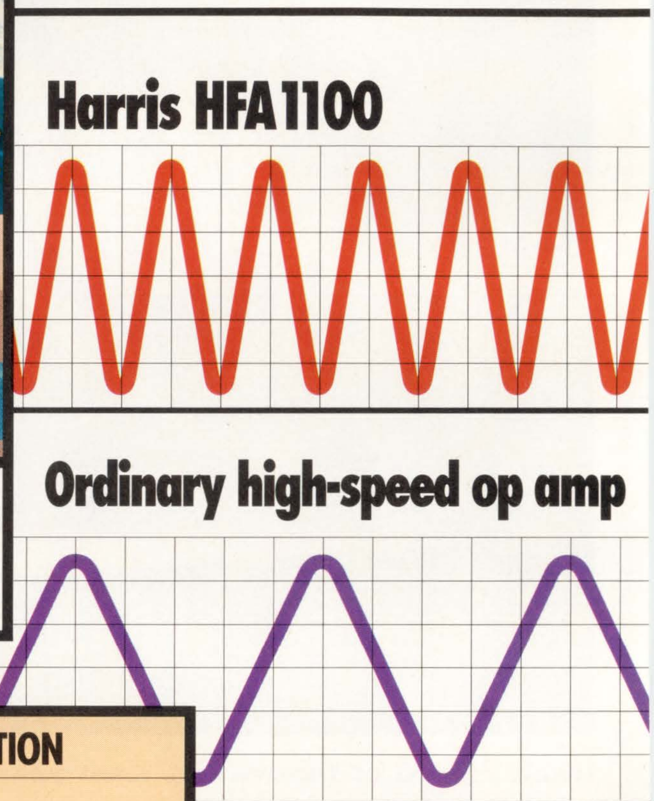
WE HAVE THE FUTURE IN CONTROL.

CIRCLE NO. 55

HARRIS GENERATES ASTOUNDING



This HFA1100 family's fast performance is made possible by Harris' unique UHF-1 process. The shallow structure of UHF-1 transistors is the result of bonded wafer technology.

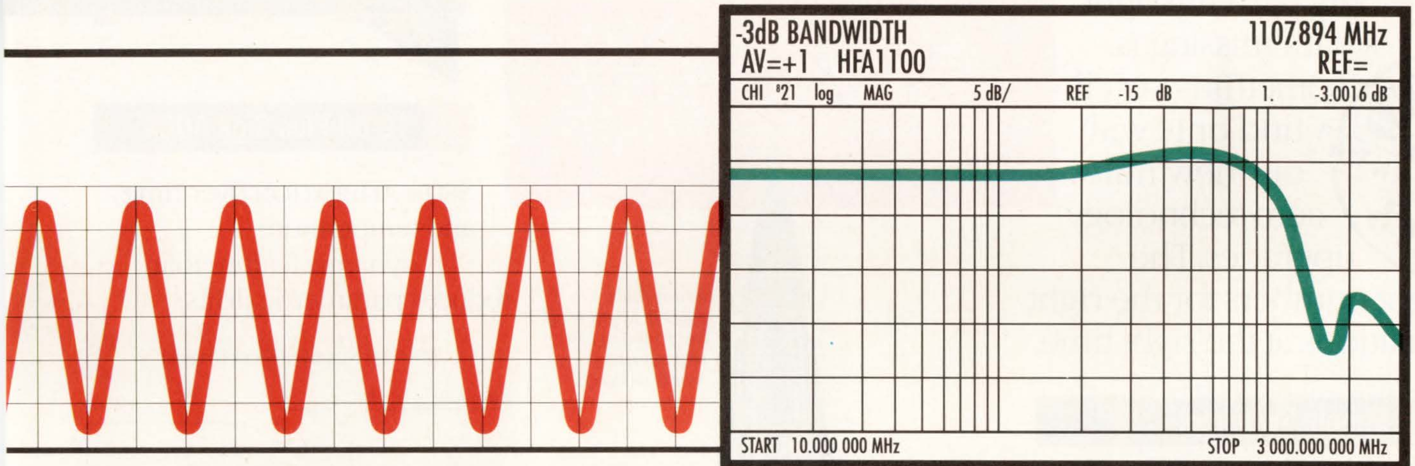


PRODUCT	CONFIGURATION
HFA1100 op amp	Standard pinout
HFA1120 op amp	Output offset adjust
HFA1130 clamped op amp	User-defined output clamp
HFA1110 buffer	Standard buffer pinout
HFA1112 buffer	Standard op amp pinout

Once again, the latest breakthrough in ultra-high-speed op amps comes to you from Harris.

This time, it's the HFA1100. Three times as fast as the old record holder. And just what fast-thinking engineers like you have been waiting for. Quickly imagine what you can do with a bandwidth so huge. Providing excellent phase linearity and a remarkable gain flatness of 0.14 dB to 100 MHz. And your creativity

INNOVATIONS WITH FREQUENCY.



APPLICATIONS

- High-Resolution Displays
- RF Transmitters/Receivers
- Medical Imaging Systems
- Radar Systems
- Flash A/D Drivers
- Video Switching and Routing/Line Drivers
- Fiber Optics

	HFA1100/20/30	HFA1110/12
-3dB Bandwidth	870 MHz	700MHz
Slew Rate	2500V/µsec	2500V/µsec
Settling Time (0.1%)	11 ns	7 ns
High Current Output	60 mA	60 mA
Temperature Range	-40°C to 85°C	-40°C to 85°C
Packages	8-pin PDIP, CerDIP, SOIC	8-pin PDIP, CerDIP, SOIC
Prices (100s)	$9.95	$5.95

needn't stop with standard products. Because the UHF-1 process is available in semicustom, as part of Harris' industry-leading FASTRACK™ design system.

So rev up your oscilloscopes. And get your hands on some HFA1100s today. Just call 1-800-4-HARRIS, ext. 1173.

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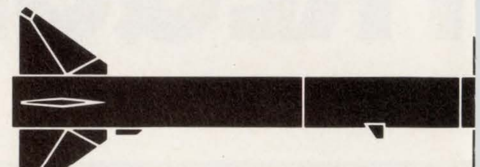
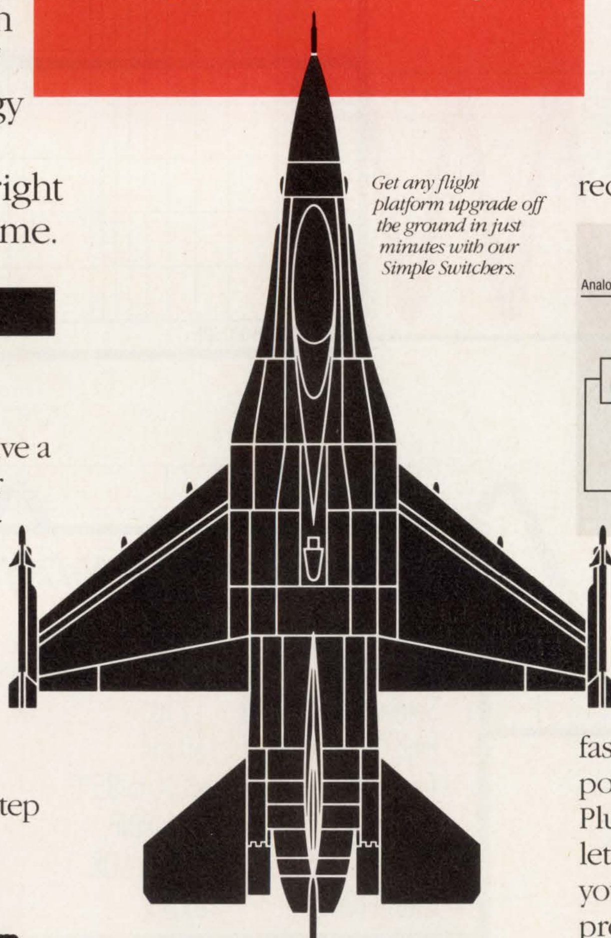
MIL/AERO UPGRADES #3 #24 #49

Whoever said there's "strength in numbers" was only partially right. What's missing is something you'll find only with our new mil/aero technology upgrades. The right numbers for the right situations at the right time.





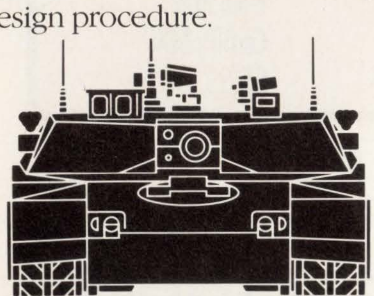
Get any flight platform upgrade off the ground in just minutes with our Simple Switchers.

#3 Simple Switchers

SIMPLICITY advanced to the n[th] degree.

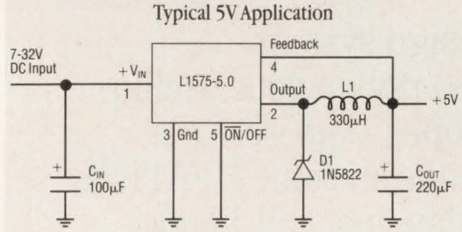
Simple Switchers™ can drive a 1A load at 88% efficiency for one-fifth the cost of a DC-to-DC power converter. With just four external parts.

In fact, our LM1575K family of regulators—ideal for MIL-STD-704D/1275A systems—is easily customized in 30 minutes with our free software kit and three-step design procedure.



For target acquisition and turret control, set your sights on our self-calibrating ADC1241.

Typical 5V Application

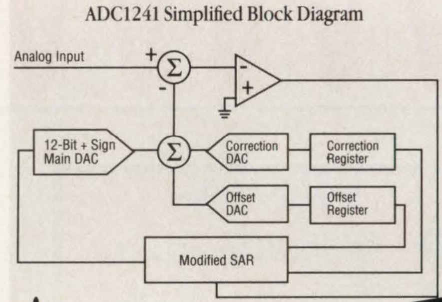


#24 12-Bit Plus Sign ADCs

SELF-CALIBRATION over time and temperature.

A dynamic feature that reduces parametric drifts,

ADC1241 Simplified Block Diagram



improves linearity and zero errors, and eliminates the need for external adjustments.

The ADC1241 is also fast (7.7μs) and extremely power conscious (40mW). Plus, its ±5V power supply lets you tap into the power of your existing logic and microprocessor supplies.

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SILENT yet swift.

FACT Quiet Series™ cuts through device noise with guaranteed specs for dynamic

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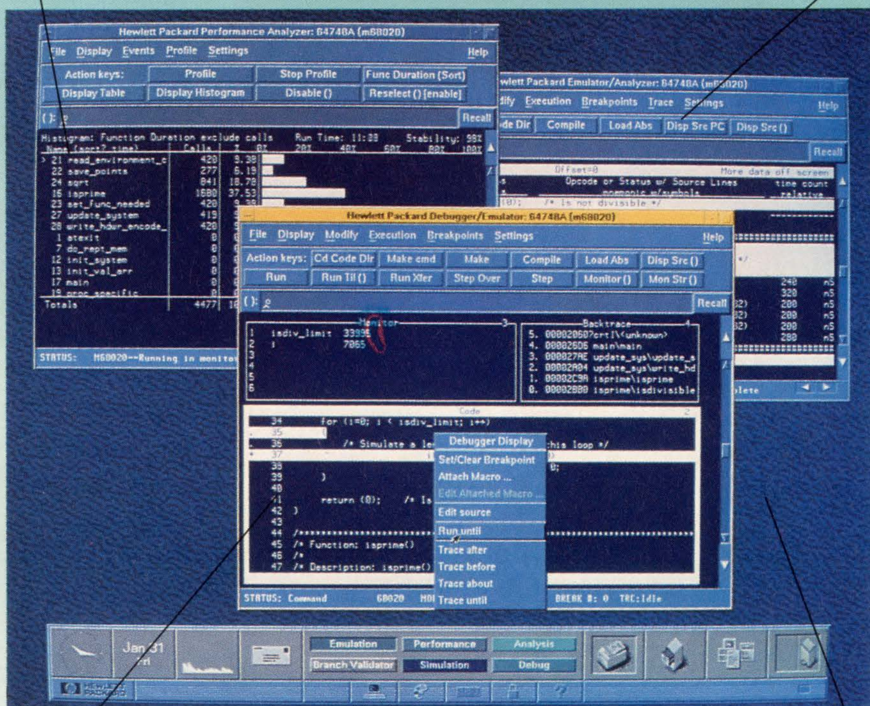
If you're looking for easier embedded debugging, try our new environment.

Real-time software performance analyzer profiles your code and speeds optimization.

User-configurable tools offer intuitive operation and share common look and feel.



Full-featured C debugger runs in-circuit with our emulator.

Concurrent real-time analyzers and debuggers provide simultaneous, linked views of target.

The new HP 64000 embedded debugging environment makes it easy.

If easier embedded debugging is what you're looking for, the HP 64000 can point you in the right direction, with a new graphical user interface that has pull down menus for workstation hosted products. Point and click measurements. And rapid action keys to speed up routine tasks.

For most popular processors, the interface is always the same. So you don't have to learn new commands for different jobs.

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80960KA/KB	80C186XL	80C186/188
		80286/C286
PLATFORM SUPPORT		
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(1)Also support for AMD, Texas Instruments, Zilog, National Semiconductor, ATT, NEC, Hitachi and Mitsubishi; call for more information.

There is a better way.

HEWLETT PACKARD

CIRCLE NO. 59

Analog IC combines five functions for battery power management

Many system designers are extending the lifetime of their battery-powered systems by incorporating power-management logic. The ML4860 power-control IC integrates many of the analog elements needed to execute the logic's commands; it also provides voltage regulators and other power functions commonly found in battery systems. If the device's combination of power functions is not a perfect match to your system's needs, you can arrange for some modifications. The device is based on a semistandard analog array that the manufacturer can easily adapt.

The standard ML4860 chip provides the basic elements of a 100-kHz dc/dc converter and buck regulator on chip (**Fig 1**), allowing you to create a 3A, 5V regulated power supply from a 5.5 to 20V dc source. You need add only two power-switching transistors and some passive components. The voltage can come from a battery, an ac adapter, or both. When you use an adapter, the device will automatically drive an external power switch to disconnect the battery from the system.

In addition to the buck regulator, the device provides boost and linear regulators to generate a 12V and a second 5V source. The 12V source has an on/off control. You can therefore use the 12V source for in-system programming of EEPROM devices, then turn off the programming voltage to prevent inadvertent data changes.

The device supports your power-control logic by providing several control and output signals. For example, it generates a 2.5V reference and compares that signal internally against the battery. It provides a Battery Low signal if the battery voltage falls below 2.5V. It also supplies the reference signal on a separate pin.

Your power-management logic can also control the ML4860 chip. The device offers both a standby mode and a sleep mode. In standby mode, it turns off all of its functional blocks except the Low Battery indicator and the second 5V source. The sleep mode also turns off the indicator. Because the second 5V source always remains active, you can use it to power your power-management logic when you turn off the rest of the system. The device consumes 4 mA when active, but only 75 μA in sleep mode.

You will probably want to use n-channel transistors to switch power in your system because they are less expensive than p-channel types of similar resistance. Your system's power-control logic signals, however, cannot drive n-channel power transistors directly. The ML4860 has three translators for giving your logic signals the drive they need to handle n-channel devices. The output signals for battery switching and the buck regulator also handle n-channel transistors. The device comes in a 28-pin plastic leaded chip carrier and costs $4.95 (1000).—**Richard A Quinnell**

Micro Linear Corp, 2092 Concourse Dr, San Jose, CA 95131. Phone (408) 433-5200. FAX (408) 432-0295. Contact Jon Klein.

Circle No. 730

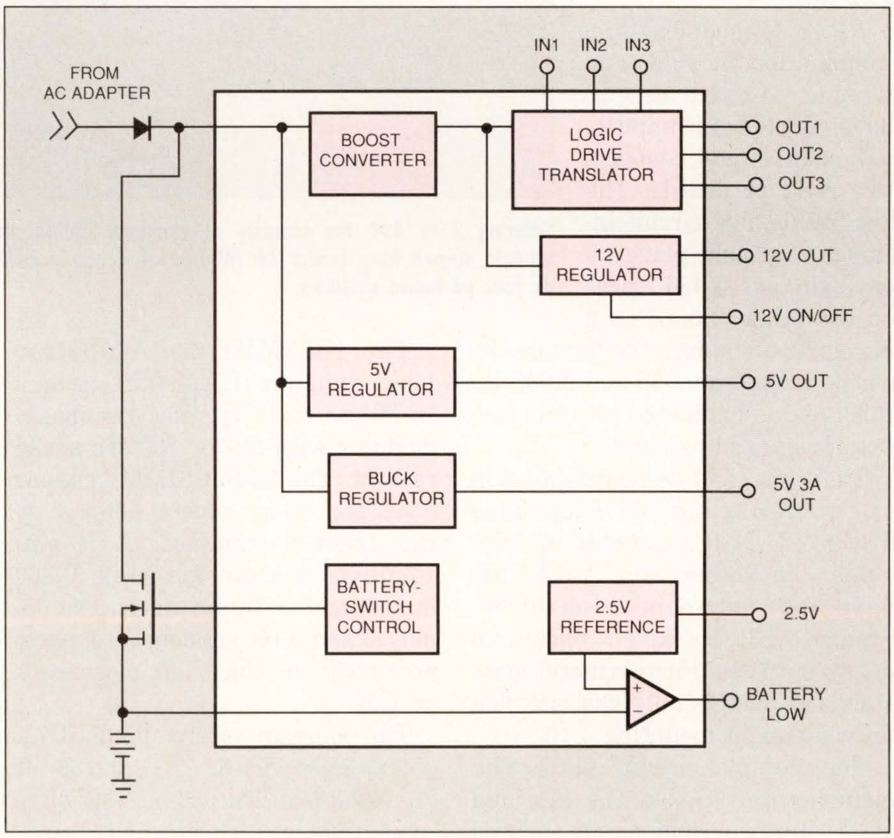


Fig 1—Systems with power-management logic still need analog circuits to execute commands. The ML4860 device combines many circuits like this in one IC.

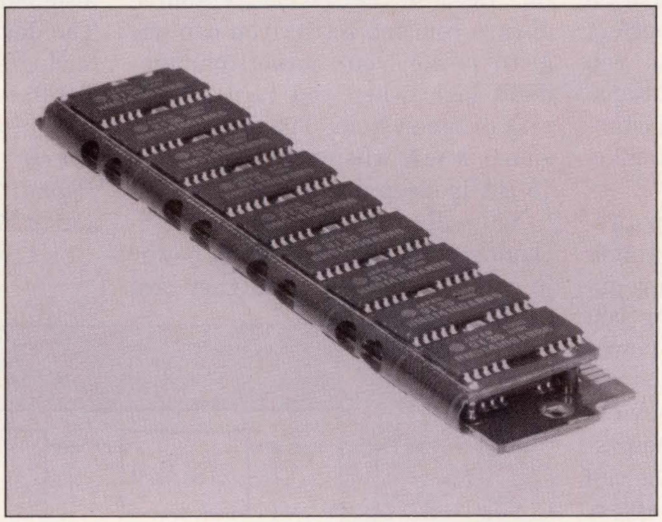
Memory modules use TSOP ICs and store 16 Mbytes on JEDEC SIMMs

The FRAMM (flexible-rigid assembly memory module) memory packaging scheme, from Memory X Inc, can pack 16 Mbytes of dynamic RAM onto a module compatible with industry-standard JEDEC 30- and 72-pin SIMMs (single in-line memory modules). The modules employ TSOP (thin small-outline package) memory ICs and maximize use of the space between SIMM modules mounted in adjacent sockets. You can choose modules that have the ×8- and ×9-bit organization used in many personal computers, or the ×33- and ×36-bit organization used in workstations from Sun and IBM.

FRAMM modules use a combination of rigid and flexible pc-board assemblies, as the name implies. A flexible circuit connects two rigid pc boards. The 2-sided flexible circuit includes a ground plane on one side and signal traces on the other. Based on a dielectric of kapton, the flexible circuit is between 0.005 and 0.008 in. thick and is laminated into the layers of the rigid assembly.

The twin rigid pc boards used in the FRAMM module each have TSOP DRAM ICs mounted on both sides. Therefore, the FRAMMs have four component surfaces. Standard SIMMs have a maximum of two surfaces. Furthermore, most standard SIMMs only use one side for component mounting.

The flexible circuit allows the manufacturer to fold the flex and align the two rigid circuit boards adjacent to each other on parallel planes. Rigid standoffs connect the two pc boards. One of the pc boards includes the external contact area, which is generally the finger contacts for mounting the module in a SIMM socket. The company also offers the modules with the pins required for SIP (single in-line package) sockets. The company will customize the connection to meet customers' specific application needs.



Offering 2 to 4× the capacity of standard SIMMs, the FRAMM module shown here packs 16 Mbytes of dynamic RAM mounted on four pc-board surfaces.

The FRAMMs use 4-Mbyte× 1-bit dynamic RAMs to reach a 16-Mbyte capacity. You can choose modules with 60- or 80-nsec speed ratings. The 72-pin SIMM versions meet the 36-bit pinout defined by the JEDEC standard. A 72-pin, 16-Mbyte module measures 0.850 in. tall and 0.350 in. thick. The 30-pin, 8- and 9-bit versions also measure 0.350 in. thick but measure 1 in. tall.

The company offers standard 72-pin modules with 32-, 33-, and 36-bit organizations. The 33-bit version is compatible with IPX and ELC models of Sun's SPARCstations. The 36-bit version is compatible with IBM workstations. Prices for the 72-pin modules range from $629 to $699 (100) for 80-nsec modules and from $689 to $769 (100) for 60-nsec versions.

The 30-pin modules cost $629 (100) for 8-bit 80-nsec modules and $699 (100) for the 9-bit version. The 60-nsec modules sell for $689 and $769, respectively. The 8-bit modules are compatible with systems from Apple Computer that can accept 16-Mbyte SIMMs. Memory X offers the 9-bit modules in SIMM and SIP configurations that you can use in sockets commonly found in IBM-compatible PCs and many other products.

The standard products discussed here are available now. Expect the company to extend the FRAMM technology to use higher-capacity DRAMs and also static RAMs. Currently, the FRAMMs don't compare favorably with standard SIMMs on a dollar-per-Mbyte basis, but the FRAMMs save invaluable pc-board real estate and memory sockets. The company will also design custom modules using the FRAMM technology for unique applications.—**Maury Wright**

Memory X Inc, 3954 Murphy Canyon Rd, Suite D-104, San Diego, CA 92123. Phone (619) 292-1151. FAX (619) 292-0774.

Circle No. 732

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PLAIN PAPER

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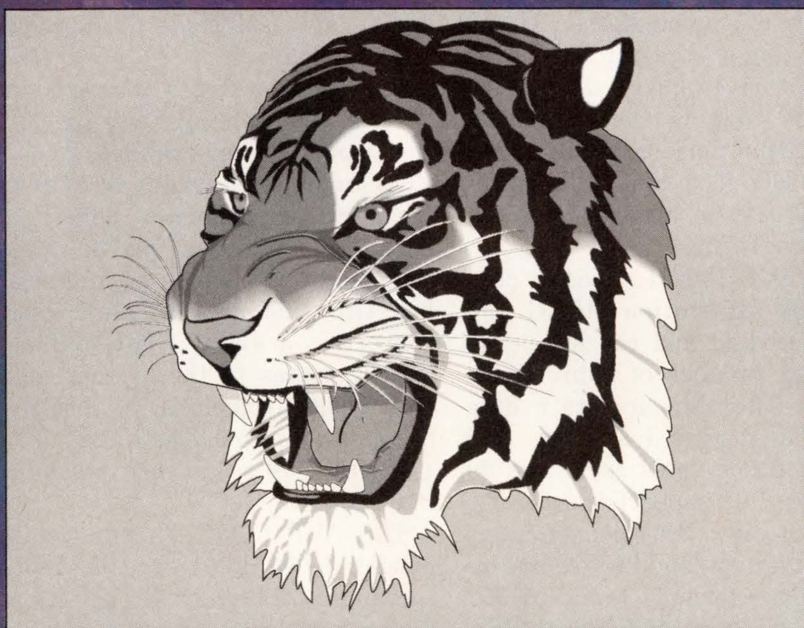

On a much larger scale.

At last. A personal output device that combines the best features of a desktop laser printer with the ability to produce large format drawings. It's called ProTracer — a 360 dpi desktop printer/plotter that produces A, B, as well as C-size output.

ProTracer's speed and quiet operation come from the latest Canon inkjet technology and an Intel i960 processor. Drawings that take up to half an hour to print on a pen plotter take only five minutes on ProTracer!

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Optional Printer Accessories

HP-GL emulation card	$399
PostScript language emulation card	$499
2 MB memory upgrade	$299
4 MB memory upgrade	$499
8 MB memory upgrade	$899
Sheet feeder I (100 sheet)	$149
Sheet feeder II * (100 sheet)	$129
PacificTalk (AppleTalk interface module)	$199

*Sheet feeder I is required for use

At Pacific Data Products, we're devoted to customer service. We offer a 60-day money back guarantee of satisfaction, one year and optional extended warranties, and free lifetime technical support. Should you require a replacement unit while under warranty, one will be rushed to you immediately to minimize your downtime.

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CIRCLE NO. 60

Video codec chip set provides MPEG, P*64, and JPEG compliance

Designers can move one step closer to building low-cost multimedia systems using AT&T's AVP-1000 video codec (coder/decoder) chip set. The set includes a system-controller IC, two encoder chips, and a decoder IC. You can use the chip set to build a system that complies with MPEG (Motion Picture Experts Group), JPEG (Joint Photographic Experts Group), and CCITT P*64 (an international videoconferencing standard) standards. The chip set includes interfaces to AT&T's DSP and communication ICs, further simplifying system designs.

Compression and decompression of full-motion video has limited the development of multimedia systems. Board-level products exist that can perform this video codec chore, but the boards have been too big or expensive to make multimedia a widespread success. This codec chip set can help solve size and cost problems. Compatibility with MPEG standards will make the ICs useful in desktop multimedia applications, and CCITT P*64 compatibility will fit the chips into videoconferencing applications.

Fig 1 depicts a typical system design that uses the AVP-1000 chip set. The AVP-1400C multimedia communications protocol controller handles audio and video traffic on the system bus. Based on the company's Pacer RISC architecture, the controller relieves the host processor of system-level tasks such as multiplexing, synchronization, buffer management, error detection/correction, and communication functions. For example, the chip can multiplex and demultiplex compressed MPEG or P*64 audio, video, and user data.

The controller chip can combine and synchronize multiple communication channels. It also includes an interface to communication ICs, so you can connect the chip set to links ranging from T1 lines to ISDN. You can also connect the company's DSP3210 multimedia DSP μP to the AVP-1400C. The chip set requires the DSP3210 to handle JPEG and audio processing.

The AVP-1400D decoder chip provides full-motion MPEG and P*64 decoding and can handle an arbitrary number of bidirectional frames. The chip accepts a data stream as fast as 4 Mbits/sec and handles frame rates as fast as 30 frames/sec. It supports resolutions ranging to the CIF (common intermediate format) and SIF (source intermediate format) levels of 352 pixels × 288 lines and 360 pixels × 288 lines, respectively. The chip can also handle MPEG still-frame decoding at resolutions as high as 1024 × 1024 pixels.

The decoder accepts data through the host bus or through a serial bus. It outputs raster-scanned 24-bit RGB (red, green, blue) or YCrCb (an alternate colorspace definition based on luminance) pixels via a dedicated pixel bus or via the host bus. Other features include a color converter, a 4-kbit FIFO buffer, and interfaces to the system controller and dynamic RAM that require no glue logic. The IC requires 1 Mbyte of 70-nsec RAM to handle P*64 and MPEG.

The AVP-1300E encoder chip handles P*64 H.261 encoding and, therefore, mainly targets videoconferencing applications. However,

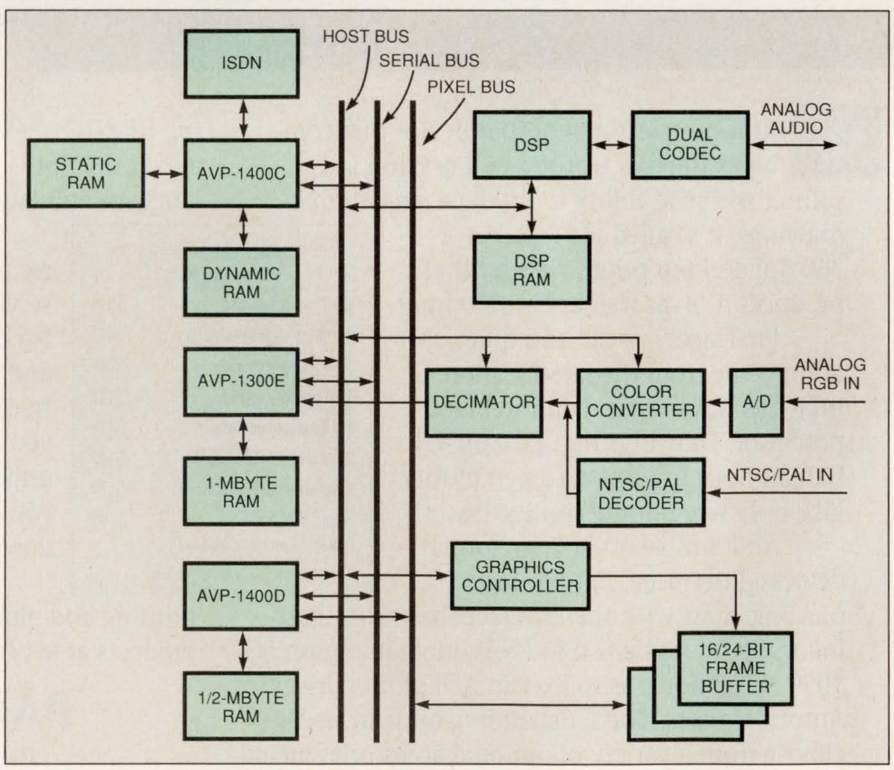
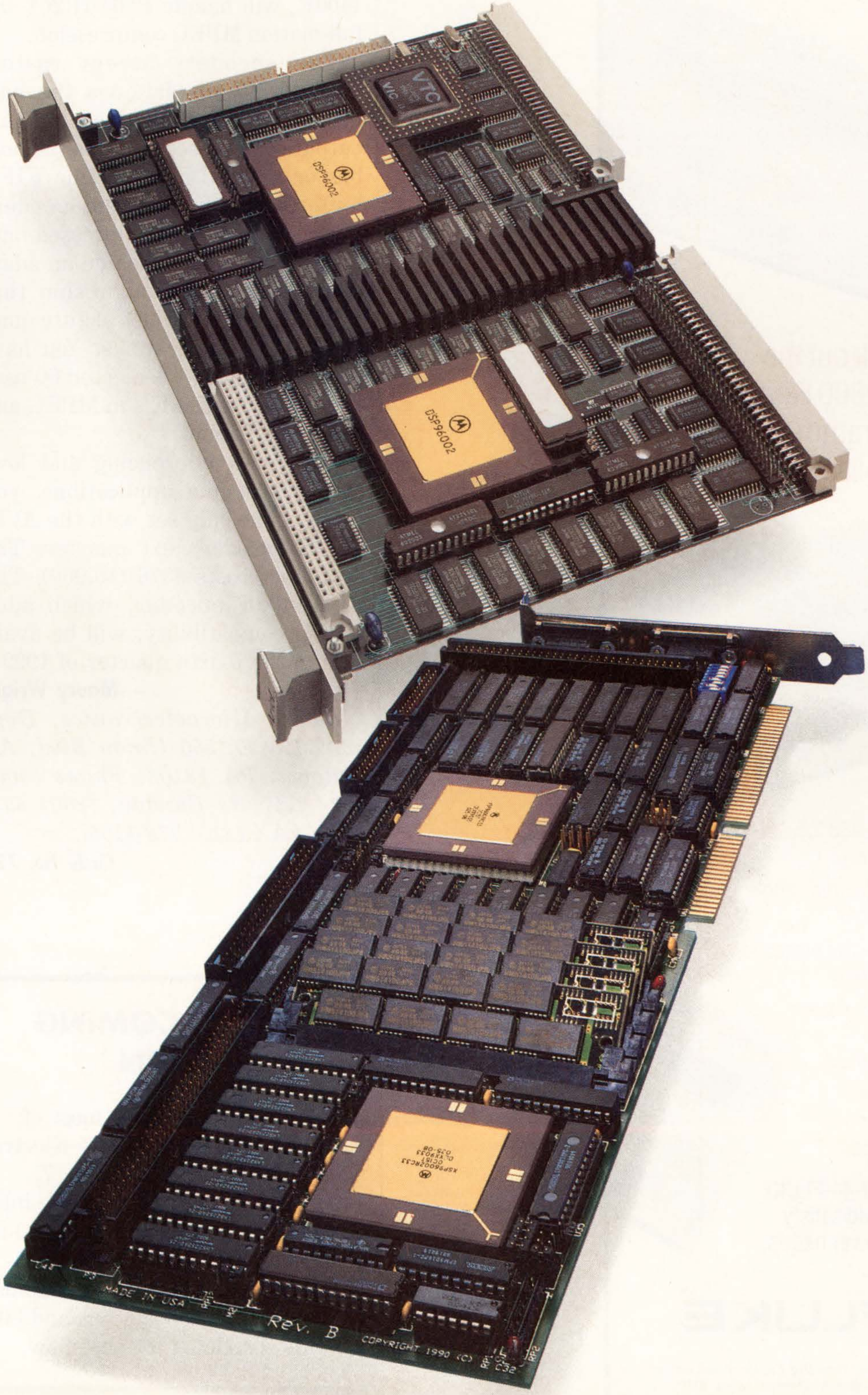


Fig 1—MPEG compression and decompression key the feature set of the AVP-1000 video codec chip set. The set includes a controller IC, a decoder chip, and an encoder IC.

Only Ariel Delivers
100 MFLOPS DSP96002
Signal Crunching Across The Board



ISA, EISA, or VMEbus, Ariel processor boards unleash all the power of Motorola's DSP96002. Both the MM-96 for ISA/EISA and V-96 for VMEbus combine lightning-quick speed with large memory arrays, versatile I/O with 120 Mbyte/sec. total bandwidth, and the ability to deliver almost unlimited signal-crunching power via Ariel's two exclusive high-speed expansion buses. And Ariel's steadfast commitment to service and support ensures that once you've become an Ariel customer, you'll never work alone.

To find out more about the MM-96 and V-96, or any of Ariel's broad range of DSP products for Motorola, Texas Instruments, and AT&T DSP chips, you can send us a fax, leave us a message on the BBS or E-mail, or just give us a call.

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CIRCLE NO. 61

the IC can also handle MPEG intracoded frame compression for working on high-resolution images and digital editing. You can define the resolution in multiples of 16 to a maximum of 720 pixels × 576 lines. A follow-on encoder, the AVP-1400E, will handle P*64 H.261 and full-motion MPEG compression.

The encoders accept raster-scanned YCrCb data via the host bus or a dedicated video bus and output compressed data via the host bus or a serial bus. On-chip FIFO buffers absorb picture-dependent fluctuations in the compressed data rate. The ICs also include an adaptive buffer-control algorithm that enables users to adjust picture quality in P*64 applications. You have to add 1 Mbyte of dedicated 60-nsec DRAM to use the ICs in MPEG and P*64 applications.

For videoconferencing and low-cost multimedia applications, you can buy the chip set with the AVP-1300E encoder next quarter. The 3-chip set costs $376 (10,000). The AVP-1400E encoder, which adds MPEG compatibility, will be available in the fourth quarter of 1992.

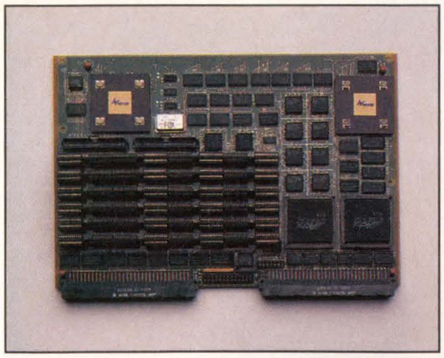
—**Maury Wright**

AT&T Microelectronics, Dept 52AL040420, 555 Union Blvd, Allentown, PA 18103. Phone (800) 372- 2447; in Canada, (800) 553-2448. FAX (215) 778-4106.

Circle No. 731

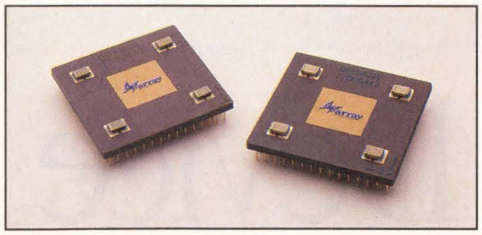
WHAT'S COMING IN EDN

To help you make the most of your trip to Boston for the Electro show, EDN Magazine's May 7, 1992, issue will provide all the info you need to plan your agenda. Our Electro/92 preview includes product reviews and highlights of some of the 60 technical sessions and 800 exhibits scheduled for the show.



400 MOPS FOR 6U VMEbus SYSTEMS

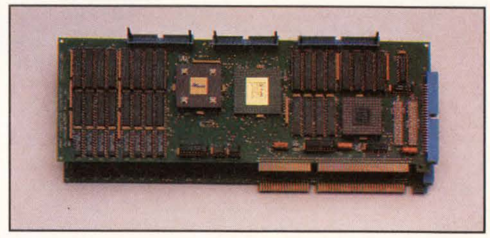
This 6U VMEbus board performs 400 million operations per second and is optimized for frequency domain processing such as FFTs and finite impulse response (FIR) filters using fast convolution. The FDaP features a private 32-bit, 20 MHz high-speed data I/O bus and extensive double buffering for continuous processing of real-time data. An additional 32-bit complex output provides phase/magnitude data. The a66540 is available in 25 MHz and 40 MHz versions. A single 40 MHz version can execute a 1K point FFT in 132.7 µs and a 64K point FFT in 13.1 ms. These times are nearly halved for real input. Multiple FDaPs can be cascaded to achieve almost linear improvement in FFT performance. Plug 400 MOPs into your system by calling **array** Microsystems' Hotline: 719-540-7999.



THE DaSP/PaC CHIPSET:

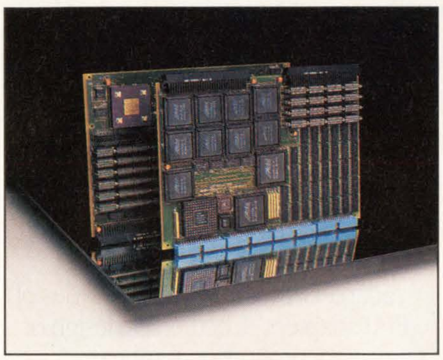
The heart of the world's fastest DSP product family

The Digital array Signal Processor (DaSP) executes 16 high-level instructions, including FFT butterflies, windowing, complex multiplies, and general-purpose functions. The Programmable array Controller (PaC) manages the entire system, including address generation for the DaSP and memory, and I/O up to 80 MHz. Using a single chipset, for example, a 1024 point FFT requires only 12 instructions and can execute in only 131 µsec; a complex FIR filter, using 28 instructions, processes at a 2.3 MHz rate. For even higher performance, you can cascade the chipset. Both utilize a 144-pin PGA format and are available in 30 and 40 MHz versions. To receive complete technical information, call **array** Microsystems' Hotline: 719-540-7999.



PC-FDaP PERFORMS 250 MOPS!

The a66550 Frequency Domain array Processor (FDaP) brings high performance FFT processing to any PC-AT compatible computer. The two board set will fit into two full size PC-AT slots, operate on the 16 bit PC-AT (ISA) bus, and allow real or complex input from either the high speed connectors on the back panel or from the PC-AT bus. The FDaP accommodates an optional complex I-and-Q to magnitude-and-phase converter for post-FFT processing. Available in two memory configurations, the a66550 handles complex FFTs up to 32K points and real FFTs up to 64K points. The a66550 can compute a 1024 point complex FFT in just 210 µs. For complete technical information, call **array** Microsystems' Hotline: 719-540-7999.



CORNERTURN PROVIDES QUANTUM LEAP IN 2D IMAGE PROCESSING PERFORMANCE

The a66545 Cornerturn™ board, used in conjunction with the a66540 FDaP board for real-time two-dimensional image processing, is the first capable of processing an entire 256 x 256 pixel frame of image data in 15.2 milliseconds. This equates to a continuous, real time rate of 65 frames per second. For 512 x 512 images, the board set transforms images in 71 milliseconds, or 14 frames per second. Designed for medical imaging, radar, sonar, machine vision, and other real-time 2D image processing applications, the board set features performance of 400 MOPS at a clock rate of up to 40 MHz. The Cornerturn accepts 32-bit complex I/O data through 10 MHz double-buffered external I/O connectors or through the VMEbus and stores it in one of four on-board frame store memory buffers. For technical assistance, call **array** Microsystems' Hotline: 719-540-7999.

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arraysoft, a complete DSP software development system supporting **array** Microsystems' a66 Family of Products, provides a menu driven user interface allowing easy access to a suite of powerful development tools at the click of a mouse. This development system features a DaSP/PaC code generator, assembler, disassembler, window generator, full DaSP/PaC program control, on-screen display of data, and board-level diagnostics. For technical information or original program assistance, call **array** Microsystems' Hotline: 719-540-7999.

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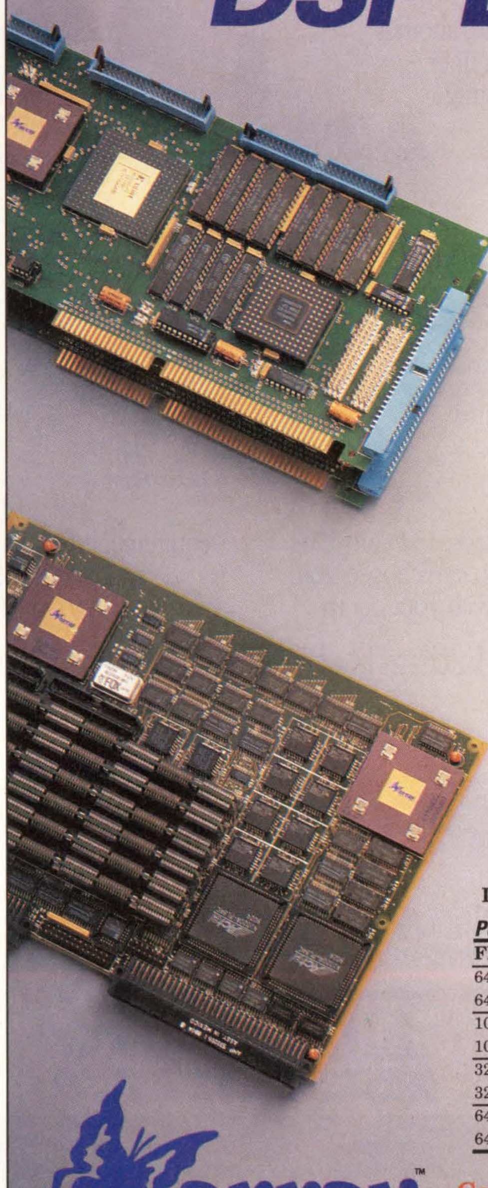


PC-AT DSP
1K FFT/126µs

DSP engine for the 16-bit PC-AT Industry Standard Architecture (ISA) bus

Performance Benchmarks

FFT size	a66550/32K @25MHz
64 Real	7.2 µs
64 Complex	10.9 µs
1024 Real	125.9 µs
1024 Complex	209.9 µs
32K Real	5.90 ms
32K Complex	10.49 ms
64K Real	15.73 ms
64K Complex	N/A

VME DSP
1K FFT/79.6µs

DSP engine for industry-standard VMEbus

Performance Benchmarks

FFT size	a66540A @40MHz	a66540A Cascade Sys.
64 Real	5.1 µs	2.9 µs
64 Complex	5.0 µs	3.7 µs
1024 Real	79.6 µs	29.6 µs
1024 Complex	132.7 µs	59.1 µs
32K Real	3.69 ms	0.91 ms
32K Complex	6.56 ms	1.82 ms
64K Real	7.37 ms	1.82 ms
64K Complex	13.11 ms	3.64 ms

array™ MICROSYSTEMS

Call the DSP Hotline: 1-719-540-7999

1420 Quail Lake Loop, Colorado Springs, CO 80906

Windows-based tool simplifies programming 186 μCs and peripherals

Coding a new microcontroller (μC) is often a painful trial-and-error process, absorbing loads of time and generating lots of mistakes. Now, for the Intel 80C186 line of μCs, there's an easier way to come up to coding speed: use ApBuilder, a graphical on-line reference and code-generation package. With this MS-Windows-based tool, engineers have both a visual programming tool for coding chip peripheral functions and an interactive on-line reference that's free of charge.

With ApBuilder, processor- and peripheral-programming documentation is on line and easily accessible. You can look up critical hardware details as you go, without having to sort through hard-to-read manuals. Even better, you can access a set of definitions for each instruction operation, including detailed instruction timings (in clock cycles and μsec). The software even generates different instruction-code examples based on selected addressing parameters.

ApBuilder is an on-line programming aid, supplementing a Windows-based text or program editor for coding. If you need help coding, you just pop open the ApBuilder window and get your answers. In addition, you can use the package to generate assembly-language code to program the 186 peripherals. ApBuilder will generate the code from dialog-box controls that you set. You can then paste this code in the Windows' Clipboard, return to your editor, retrieve it, and place it in your source code.

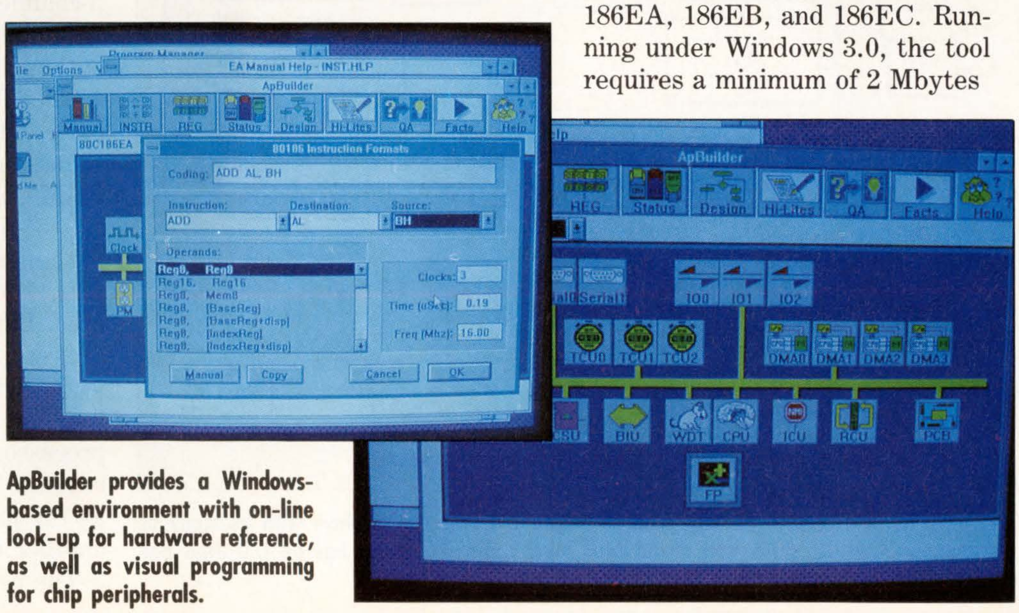
ApBuilder obsoletes old-fashioned, hard-to-use text-based interfaces. This tool runs in full color on MS-Windows and is highly interactive. Its interface is easy to use, consisting of an active menu—a menu bar made up of operation icons and a block diagram of the 186 μC. This diagram blocks out the major components of the CPU and serves as a selection device. You simply click on a block that's the portion of the processor you're interested in, and then pick an ApBuilder process function by clicking on its menu icon. This interface is easy to pick up and eliminates pull-down menu-selection lists.

ApBuilder breaks down the 186 into functional units: CPU, ICU (interrupt controller), TCU (timer control units), clock (power management), DMA, BIU (bus interface unit), RFU (DRAM refresh control unit), and PCB (peripheral control block—RAM peripheral registers). Any of these can be selected by clicking on the block. ApBuilder icon functions include

- A 186 hypertext manual
- An instruction editor and reference
- A register editor that presents the peripheral registers and provides a visual mechanism to program them
- A high-level programming mechanism to set peripheral functions
- Hi-lite: compact definitions for each μC block
- Q&A: common questions and answers for each block
- On-line help.

ApBuilder makes programming the 186 in assembly language easy; you can look up instructions, do trial coding with different addressing modes, and see their exact execution times. Also, μC peripherals are easy to program at a global level. And, if you want to get down into the bit mud, you can pull up the individual peripheral registers and program them visually.

The Windows-based tool supports the 80C186 product line, the 186EA, 186EB, and 186EC. Running under Windows 3.0, the tool requires a minimum of 2 Mbytes



ApBuilder provides a Windows-based environment with on-line look-up for hardware reference, as well as visual programming for chip peripherals.

of memory, although 4 Mbytes is preferable. It requires a VGA monitor (or better) for graphics.

—**Ray Weiss**

Intel Corp, Embedded Processor Group, 5000 W Chandler Ave, Chandler, AZ 85226. Phone (800) 548-4725; (602) 554-2388.

Circle No. 733

4-bit μC drives fluorescent display and 64 I/Os

Four-bit microcontrollers (μCs) are the versatile "Swiss Army knives" of embedded systems, delivering a range of specialized peripherals and I/O arrangements at a low cost. NEC's μPD7523x is the latest addition to its 4-bit μC line. Aimed at electronic control and display applications like VCRs, CD players, and microwave ovens, this chip integrates as much as 32-kbyte program and 1-kbyte data memory with 76 I/O pins, an 8-bit A/D converter, five timers, and a high-power fluorescent-display controller.

The μPD2723x suits industrial and control applications with fluorescent displays, which are used heavily in applications with access to standard power. The chip features a fluorescent-display controller to drive directly as many as 24 segments with as many as 16 digits. Using this chip, engineers can program as many as eight dimming levels. In addition, a keypad scanner works in conjunction with the display, picking up keypad data entry and setting an interrupt for processing.

The 4-bit processor runs with a 6-MHz clock, delivering a 0.67-μsec minimum instruction cycle time. However, processor clock rates can be varied under program control for different application requirements. For low-power, low-speed applications, the chip can drop back to a 32-kHz subsystem clock—delivering a 122-μsec instruction-execution rate. Engineers can also program it to run with intermediate clock rates of 1.5 MHz or 750, 375, or 93.8 kHz.

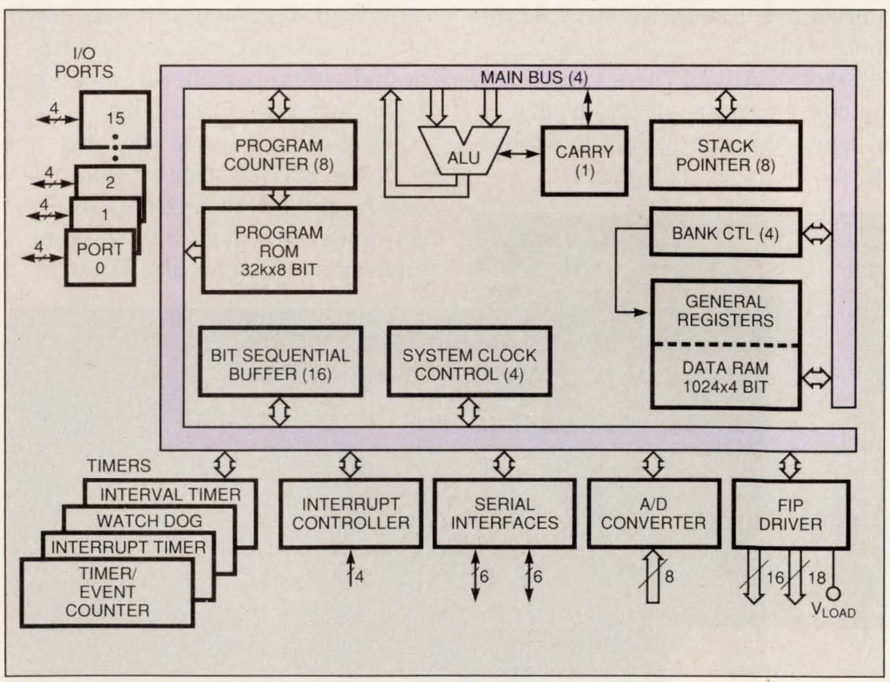
Like a true 4-bit μC, the processor provides a large number of peripheral options, including 76 I/O lines. Software can program as many as five 4-bit ports for pull-up termination resistors. Two n-channel, open-drain 4-bit ports can have pull-up resistors as a production mask option. For pull-down termination resistors, seven 4-bit p-channel open-drain ports can provide pull-down resistors as a mask option.

The 4-bit μC supports a 4-bit data path and ALU, driven by 8-bit instructions. Data memory—1-kbyte RAM—is partitioned into four 256×4-bit memory banks, a 32×4-bit general register area, and a 128×4-bit peripheral hardware area. Bank switching minimizes addressing problems. Banks are selected with a memory-bank register. For fast context switching, the processor provides four general register banks; to switch context, all the program has to do is select another register bank.

The registers are held in the

NEC μPD7523/6/7/8 μC

Clock	6 MHz, also 32.8-kHz subsystem clock; can program lower-speed clock 1.5 MHz, 750, 375, and 93.8 kHz
Instruction cycle	0.67 to 1.91 μsec or 122 μsec with subclock
Registers	Eight 4-bit registers, 15-bit program counter, 8-bit stack pointer
Memory	1k×4-bit RAM; 16-, 24-, or 32-kbyte ROM/PROM
Timers	Interval/watchdog, event counter, three timer/counters (one with 14-bit PWM output)
I/O	64 lines (16 in, 24 out, 24 in/out—include 12 lines for driving LEDs)
Special	Fluorescent-display-tube driver (handles 9 to 24 segments, 9 to 16 digits, 8 levels, key scan interrupt), max high output of 40V for two pins
Interrupts	Four external, edge programmable
Serial	Two channels
Miscellaneous	8-bit A/D converter
Power	2.7 to 6V
Package	94-pin quad flatpack (20×20 mm)
Price	16-kbyte ROM, $6.15; (50,000), 32-kbyte EPROM, $15 (10,000)



The μPD7523x 4-bit μC directly supports vacuum-fluorescent displays with as many as 24 segments and 16 digits with 8 dimming levels. The μC series has 64 I/O lines and an 8-bit A/D converter.

RAM; there are eight 4-bit general-purpose registers per bank, but they can be paired as needed for 8-bit processing. Instructions are 8 bits wide and are held in on-chip memory, either production ROM or prototyping EPROM. Program memory sizes for the μPD75236, μPD75237, and μPD75238 are 16, 24, and 32 kbytes, respectively.

—**Ray Weiss**

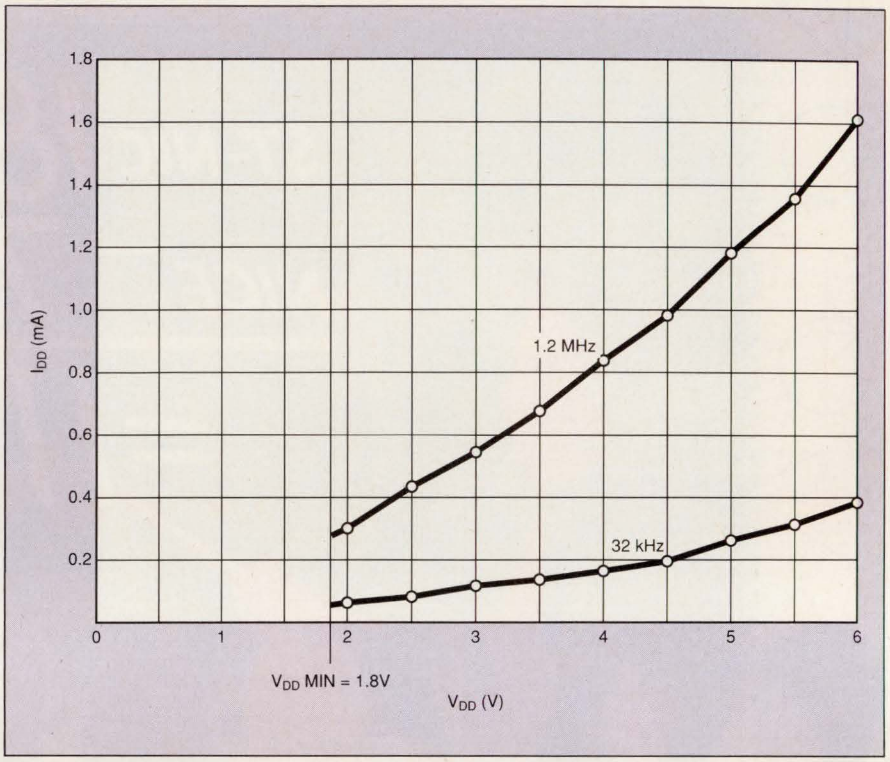
NEC Electronics, Box 7241, Mountain View, CA 94039. Phone (415) 960-6000. **Circle No. 734**

Static 8051 runs at 1.8V and draws 2.5 mA at 3 MHz

Engineers don't have to sacrifice their old favorite—the venerable 8051 μC—for low-power applications. The Signetics 80CL51 is a static implementation that needs as little as 1.8V on the power rails. A standard 8051, the 80CL51 is a static design in a 40-pin package.

Running at 3 MHz, the chip draws less than 2.5 mA at 1.8V. Power dissipation drops even further as the clock rate scales back; at 32 kHz, power drain is less than 0.05 mA at 1.8V. The static design's operating frequency runs from 32 kHz to 12 MHz with the internal oscillator (and to dc with an external clock oscillator). For comparison, at a normal 12 MHz and 5V supply, the 80CL51 draws about 10 mA of current.

The chip supports two power-control modes: idle or power-down mode. In idle mode, the clock continues to run, preserving CPU status, but the timer and interrupt peripherals lose status. The RAM and special-function registers (SRFs) are still valid. In power-down mode the clock is stopped and only RAM is preserved. The 8051's idle mode is exited via an interrupt or reset; power-down mode, via reset.



The 80CL51 cuts power dissipation by lowering chip voltages and processor clock rates. It can run at 1.8V with clock rates down to dc.

For more system options, the vendor added eight interrupts, each of which can cause an exit from power-down mode. At 1.8V with a 3.58-MHz clock, current consumption is 2.5 mA, 1.0 mA, and 10 μA for standard, idle, and power-down modes, respectively.

Signetics' 80CL51 chip

Clock	12 MHz
Instruction cycle	12 clocks
Memory	128-byte RAM; 4-kbyte EEPROM; 64-kbyte instruction-address space; 64-kbyte data-address space
Timers	Two 16-bit timer/event counters
I/Os	32 lines
Interrupts	10 external (8 can wake up processor)
Serial	Standard UART
Miscellaneous	Piggy-back version for debugging
Power	1.8 to 6V; at 1.8V, draws 2.5 mA at 3 MHz, 0.5 mA at 32 kHz
Package	40-pin DIP, plastic very-small-outline package
Price	$3.20

The 80CL51 is a ROM part. A piggyback version supports application prototyping and debugging. Built around a bond-out chip, the package has a connection on top for a standard EPROM/RAM to "ride piggyback." The chip uses the external memory as it would on-chip memory—there is no additional delay for accessing external program memory. The socket supports as much as 16 kbytes of EEPROM, making it easy to debug. Not only can users change their code, but they can add additional debug code, including a monitor.

The piggyback version provides two serial options: a standard UART and an I^2C serial bus. Engineers can use the I^2C bus to link to a host processor and debug via a ROM monitor. However, you need special hardware to convert the special serial bus into a standard RS-232C interface.—**Ray Weiss**

Signetics/Philips Components, 811 E Arques Ave, Sunnyvale, CA 94088. Phone (408) 991-2000. FAX (408) 991-2311. **Circle No. 735**

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- *High strength molded terminations*

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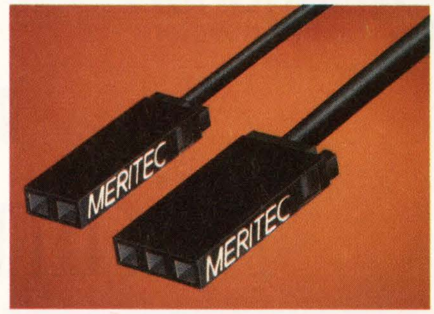

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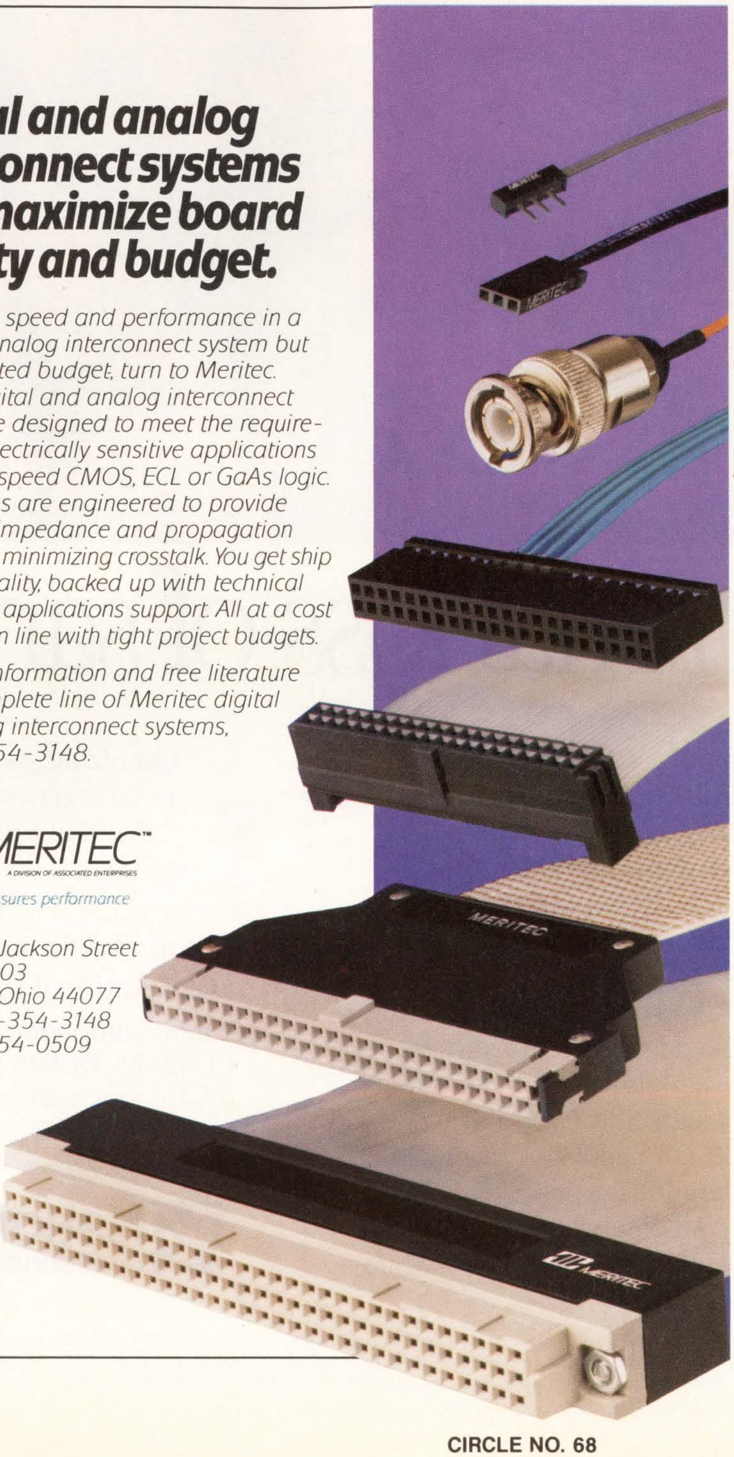

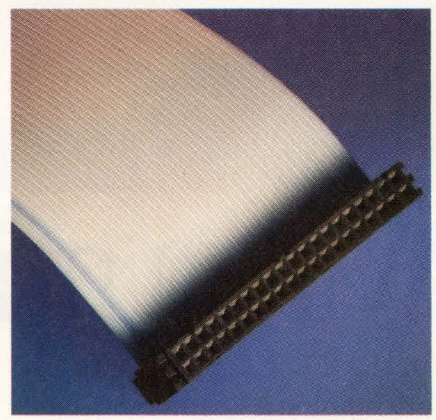

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- *Low crosstalk*

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CIRCLE NO. 68

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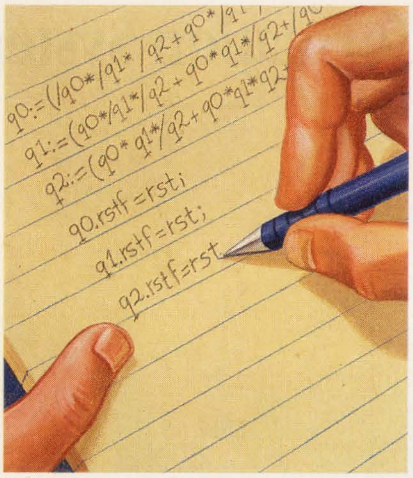

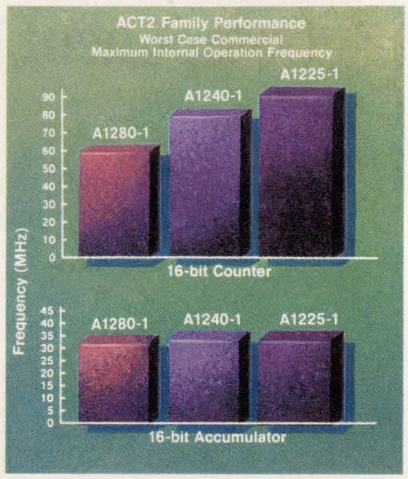

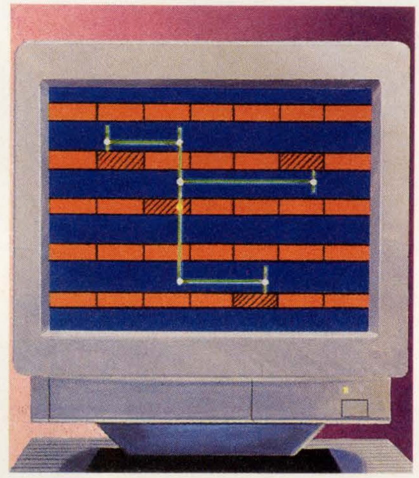

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GAs The Same Way
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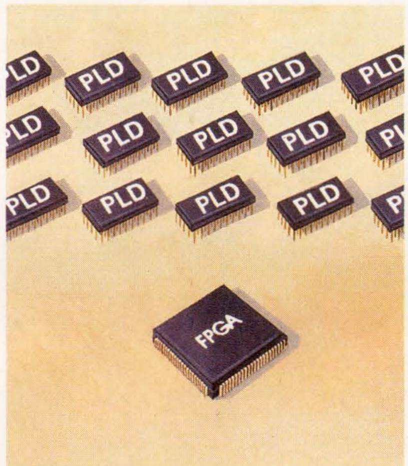

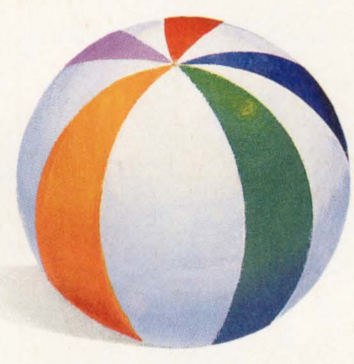

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The FPGA Design Guide

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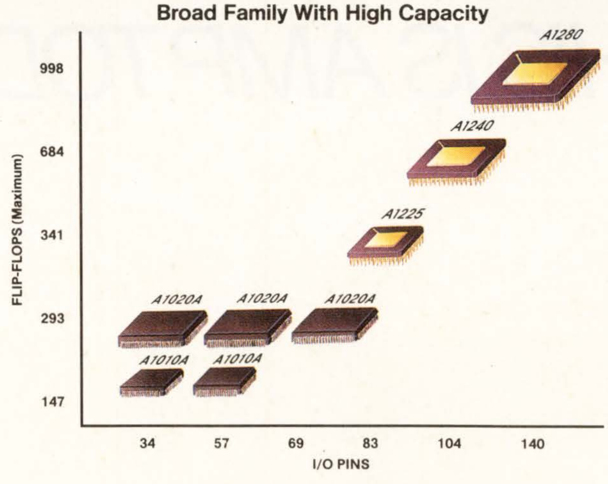
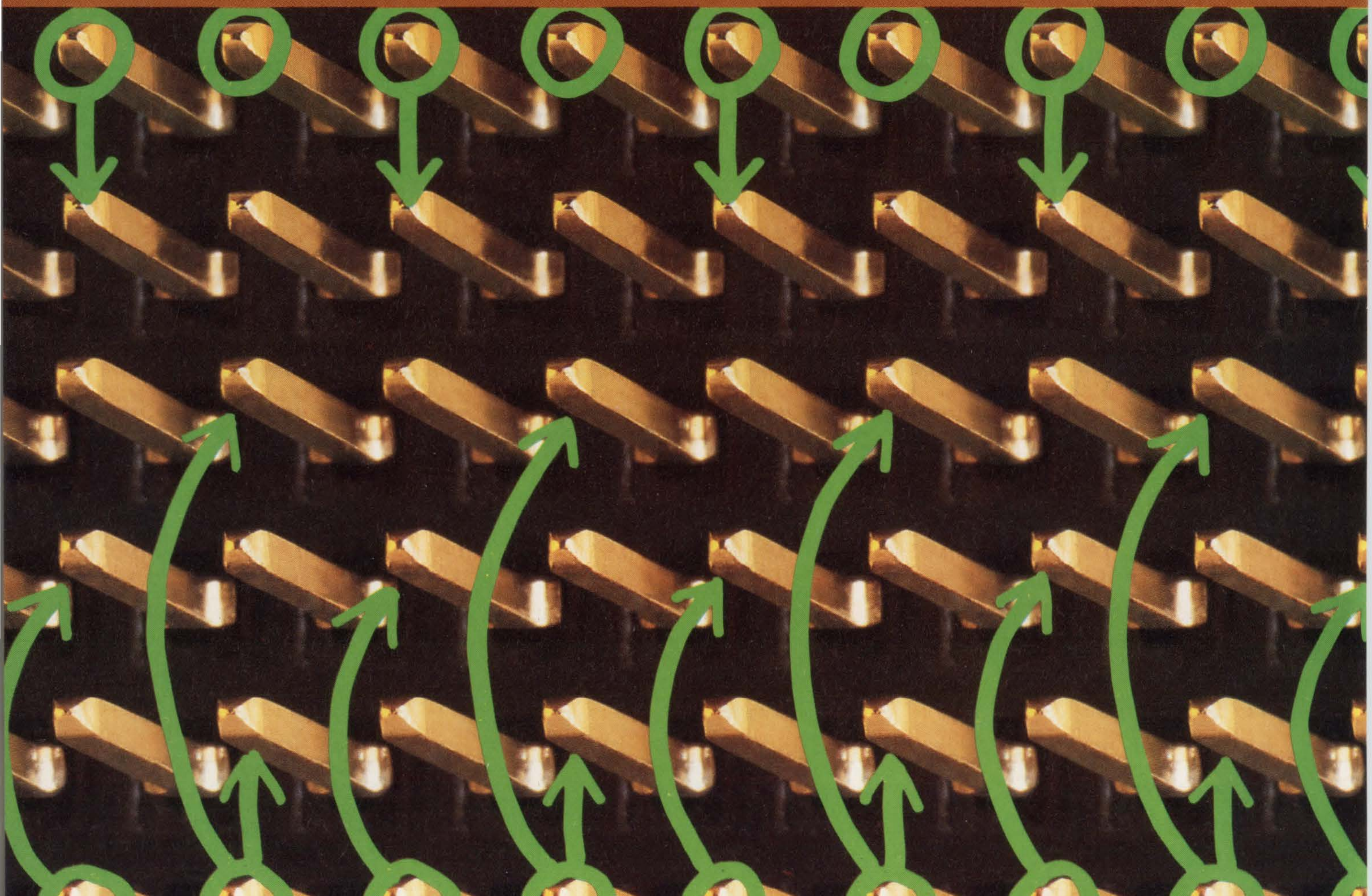


Actel

Risk-Free Logic Integration

CIRCLE NO. 73

Our six-row connector lets you change the ground rules.



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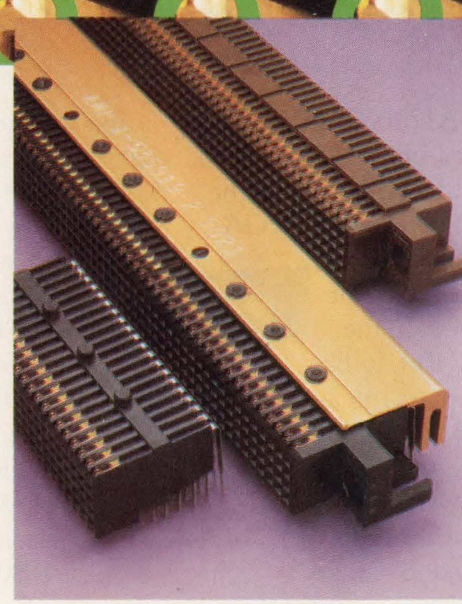
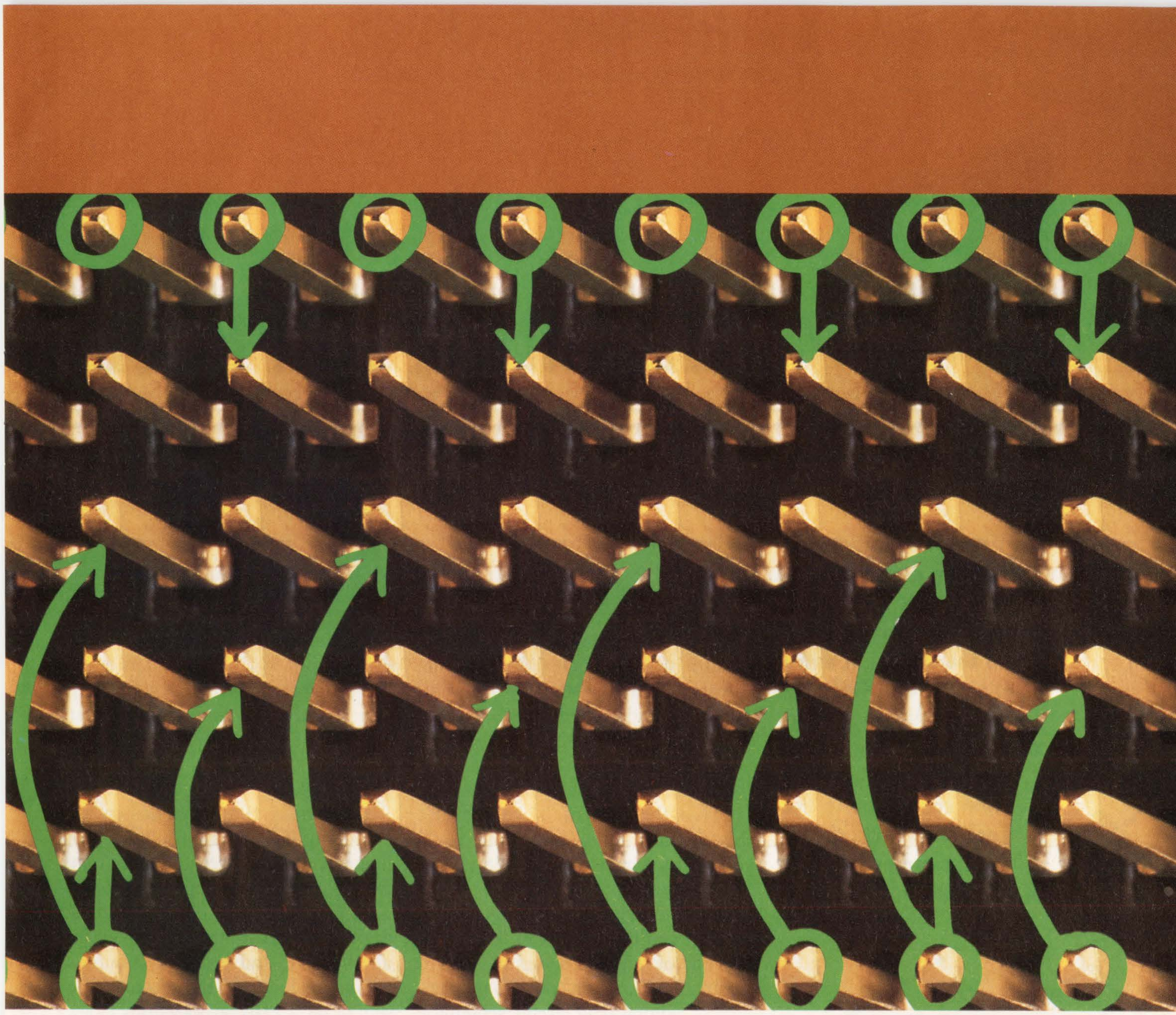


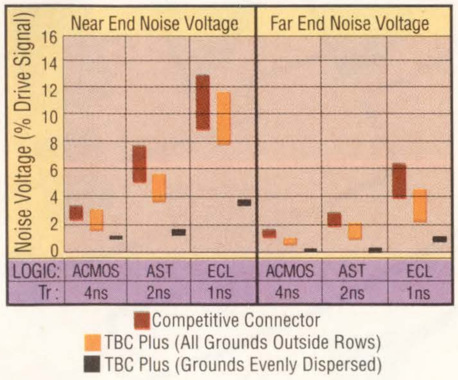


AMP TBC Plus connectors give you complete freedom in ground and signal assignment, so you can write your own 'ground rules' for outstanding electrical performance in high-speed, high-density backplane applications.

Because they are true 6-row connectors and you assign ground where you need it, near end and far end noise voltage figures in the <10 ns risetime range are far below connectors that limit ground to the outer rows or 'planes' (TBC Plus performance is even better when configured the same way!).

Our economical twin-beam receptacle design is unique in offering greatly reduced inductance in the outermost 'long' row of pins, and matched propagation delay in all lines.

Note performance of AMP TBC Plus connectors with evenly dispersed 'checkerboard' grounding: some competitive styles don't allow this.



Capacitance is a mere 2pf, max, line-to-line.

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AMP

CIRCLE NO. 72

Hands-on FPGA Project

Migrating to FPGAs: *any designer can do it*

Part 1 of this 2-part hands-on design project (in the April 9 EDN) discussed the overall circuit and the schematic entry of this FPGA (field-programmable gate array) design project. Part 2 concentrates on the steps from simulation to the final functioning circuit. The project took 29 working days from start to finish.

DOUG CONNER, Technical Editor

In the April 9 issue I discussed the first part of my journey into FPGA design. The schematic part of the design wasn't much different from ordinary SSI or MSI TTL design. Because logic simulation is seldom used in SSI or MSI TTL design, it was a new experience for me and was the greatest worry when I started the project. If you haven't been using logic simulation, you'll find this phase of verifying your FPGA design a big change.

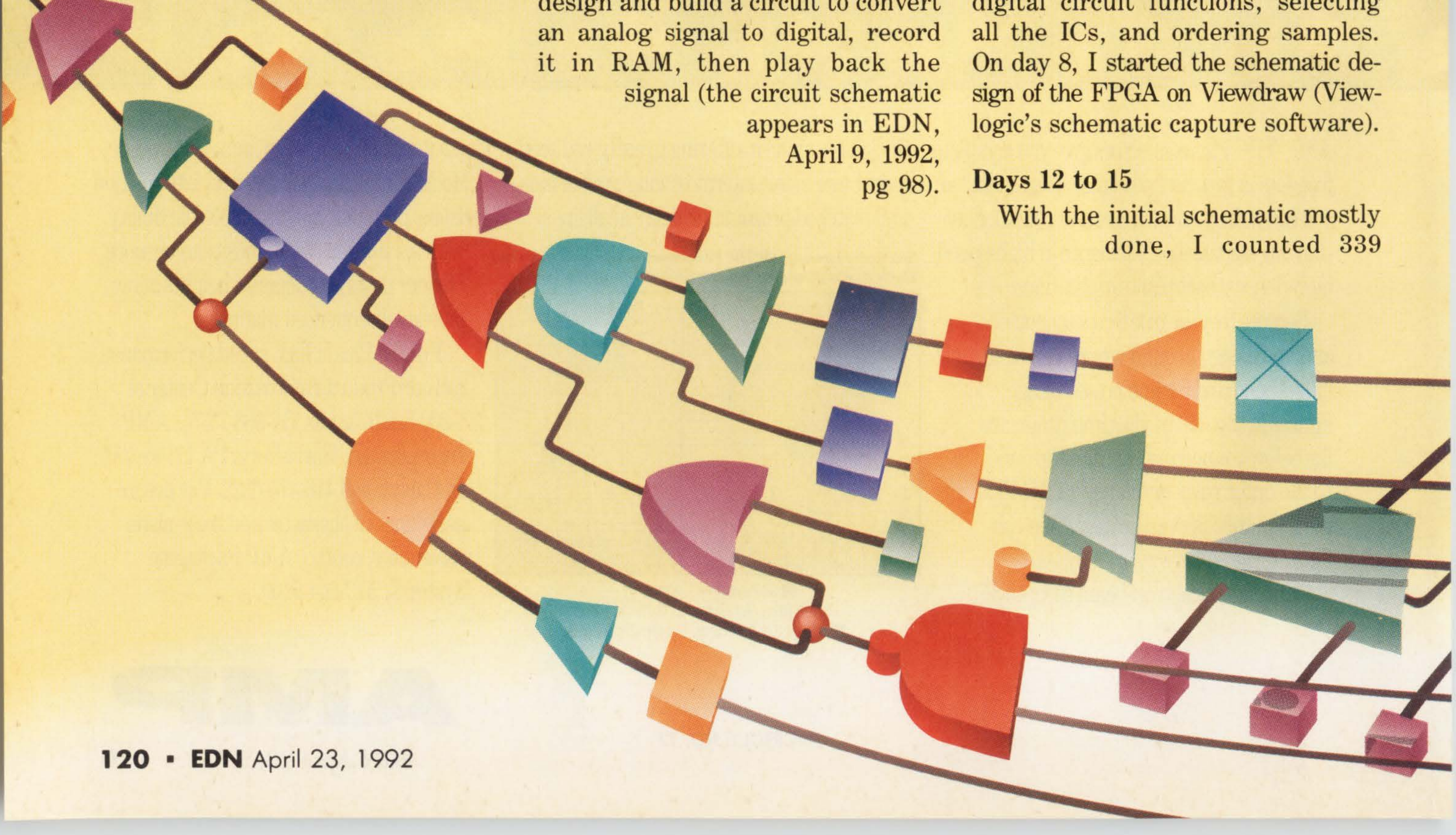
For the project, I had decided to design and build a circuit to convert an analog signal to digital, record it in RAM, then play back the signal (the circuit schematic appears in EDN, April 9, 1992, pg 98). All digital functions would be performed in the FPGA. I wanted to keep the analog portion of the circuit simple, yet be as fast as possible. I began the project by blocking out the design and figuring out what the overall circuit should do.

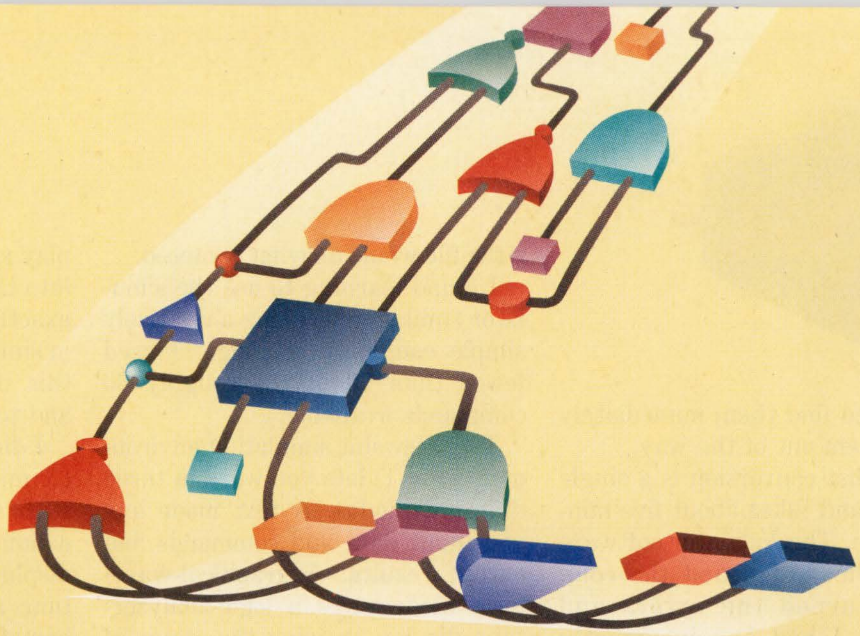
Days 1 to 11

Performing the initial design and selecting the analog parts took longer than I expected. I spent the first eight days doing the preliminary analog design, blocking out the digital circuit functions, selecting all the ICs, and ordering samples. On day 8, I started the schematic design of the FPGA on Viewdraw (Viewlogic's schematic capture software).

Days 12 to 15

With the initial schematic mostly done, I counted 339





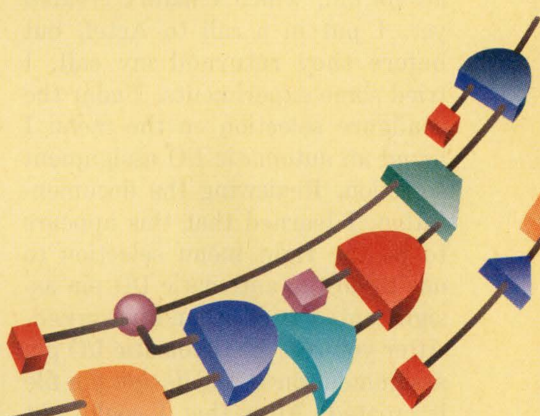
used modules. That's too big for the 295 modules on an Actel 1010 device and only 60% of the 547 modules on a 1020 device. I decided to bring triggering inside the FPGA and made a few more changes to take advantage of the capacity of the 1020 device.

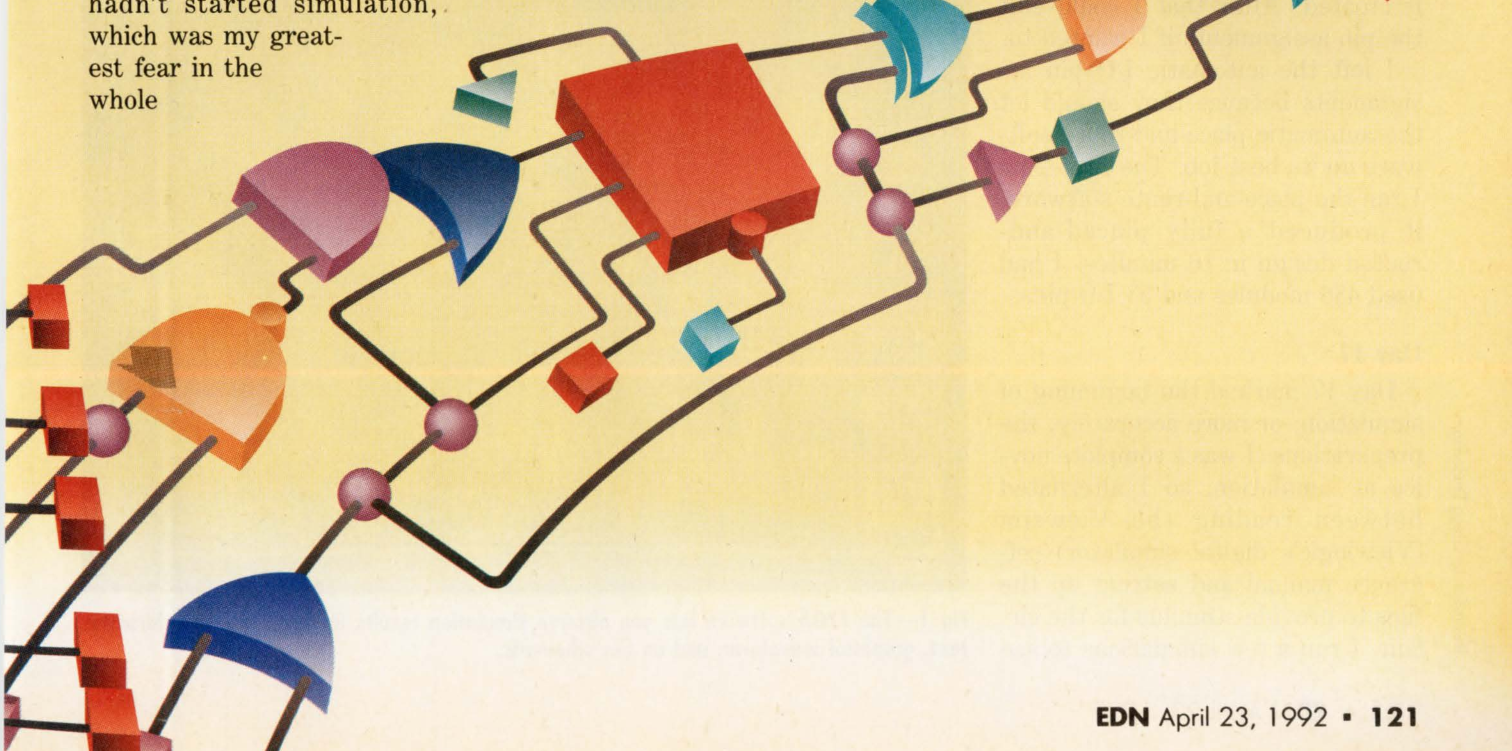
By day 14, the FPGA schematic was mostly complete, letting me update the overall circuit schematic. I spent some time drawing timing diagrams to make sure all the read, write, trigger match, and other control logic would work.

I needed to have this project done in two weeks, and at this point I hadn't started simulation, which was my greatest fear in the whole project. The schematic-entry tools were working fine, but I kept finding design problems that had to be solved or improvements I considered necessary. I initiated 12-hour workdays and 6-day work weeks.

Day 16

Even though I wasn't quite finished refining the schematic, I elected to run the netlist converter (makeadl) and do a trial place and route. I couldn't afford to get bogged down in software problems during the real place and route.





Hands-on FPGA Project

I wanted to find them immediately and get them out of the way.

The netlist conversion is a single command and takes about five minutes to run. The Validator software checked the design and the computer returned the errors and warnings: I had one incorrectly named net, four fan-out errors, and ten fan-out warnings. I corrected the errors and went on to try an auto-pin placement.

The autopin software under the Pin Edit menu wouldn't run because it needed a file named *design*.pin, which I hadn't created yet. I put in a call to Actel, but before they returned my call, I tried some experiments. Under the configure selection on the menu I found an automatic I/O assignment selection. Reviewing the documentation, I learned that this appears to be the right menu selection to use to do the automatic I/O pin assignment. I tried it, and it worked. After you run the automatic I/O pin assignment once, the *design*.pin file is created. After that I could edit the pin assignments if I wanted to.

I left the automatic I/O pin assignments because they should let the automatic place-and-route software do its best job. The first time I ran the place-and-route software, it produced a fully placed-and-routed design in 16 minutes. I had used 486 modules and 57 I/O pins.

Day 17

Day 17 marked the beginning of simulation, or more accurately, the preparations. I was a complete novice at simulation, so I alternated between reading the Viewsim (Viewlogic's digital simulator) reference manual and setting up the files to provide stimulus for the circuit. I ran a few simulations to see if the file would do what I wanted.

I found learning to use the simulator similar to learning a relatively simple computer language. I used fewer than 20 of the roughly 60 commands available.

The Viewsim simulation environment (**Fig 1**) lets you work in three different modes. A text mode lets you input data and commands and output results. A graphical-waveform mode gives a logic-analyzer-type display showing the states of signals. You can bus signals together, such as data and address lines, so you can view many signals at once. You can also create stimulus in the graphical-waveform mode, although I didn't use that method on the project. The third method is to drop down into the schematic and see the actual data values on every node. You can even push down through the levels of hierarchy into macros so you can see what is happening inside a counter or the SAR macro (a soft macro I created).

I created my input commands and data in text files, viewed results with the waveform graphical display and occasionally dropped down into the schematic display to verify exactly where a problem identified in simulation was occurring. I found this method similar to debugging and testing real hardware.

I did not use any expect-data files to make automatic comparisons with simulation results. I visually examined the waveform graphical displays to get the most information. Although I reduced the number of signals displayed in the photographs to make them easier to read, in practice I crammed as many signals as I could onto the graphical waveform display for maximum information.

For those who haven't used digital simulation before, I can offer some comments on my experience. You have to set the initial conditions for all inputs (high, low, high-impedance, or unknown) for every input or I/O pin on the FPGA. Setting the inputs for control lines and changing them during simulation is straightforward. For bidirectional data lines such as the ones connecting to the RAM in this design, you need to drive them with

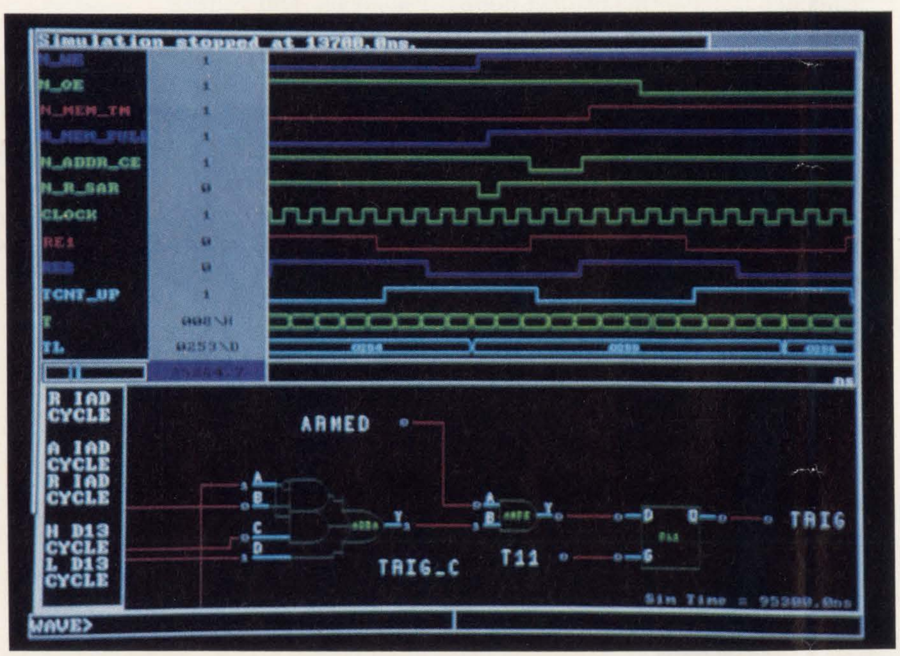


Fig 1—The FPGA software lets you observe simulation results in three different formats: text, graphical waveform, and on the schematic.

Illustration by Gregg Dinderman

the correct data during RAM reads, and release them during RAM writes. Even after you've set up the proper conditions on all external inputs and I/O lines, you're still not done. You may have to initialize internal conditions. Some of the initializing may be covered by reset logic you've designed into your circuit, and some of it may not.

For example, the address counter (**Fig 11** in Part 1, pg 98) is a free-running counter. When the simulation starts (and in the real hardware) the address is in an unknown state. After each count cycle, the hardware progresses from some initial state n to $n+1$, then $n+2$, and so on.

When you start simulation, the counter is in an unknown state and will stay there. To get useful simulation results, you have to force the counter into a known state, and then it will begin counting. I forced the counter's outputs to an initial state, then released the outputs, and the counter ran properly. You should label all counter output nets so that you can force them to known states during simulation.

Simulation is slow compared with real hardware, so you need to keep the clock-cycle count low if you want to make many simulation runs. Most of my simulation runs were a few hundred clock cycles or fewer. I don't believe a simulation ever took more than five minutes to run; a typical simulation run took about two minutes. For reference, the design is 1514 gates by standard gate-array counting measures. I ran the software on a 33-MHz 486 PC with 8 Mbytes of RAM.

To run the 15-bit counter through all 32,768 cycles would have taken nearly 400,000 clock cycles. Rather than having the simulator run for a day and generate reams of data, I forced counters to states near where some event should happen (or shouldn't happen, but might), released the counter, and let it count through the cycles I wanted to see. Then I forced the counter to the next event of interest (**Figs 2** and **3**).

My approach to simulating the design was twofold. First I tried to identify every part of the circuit where I had concerns, list them, and then make simulation test cases to verify that the function per-

Table 1—FPGA and other products used on this project

Manufacturer	Product	Price	Description
Actel	ALS-115	\$2950	All Actel software used on the project plus Viewlogic's schematic capture software.
	ALS-017	\$2950	Viewlogic's Viewsim for 3000 gates or fewer with Actel libraries.
	A1020A-PL84C	\$36.25 (100)	FPGA.
Analog Devices	AD565AJD	\$17.60 (100)	12-bit DAC.
	AD684JQ	\$23.50 (100)	4-channel, 1-μsec S/H amplifier.
Hewlett-Packard Co	HRPG-A-SCA#16C	\$15.75 (100)	Panel-mount rotary optical encoder, 120 counts per revolution.
Linear Technology Corp	LT1220CN8	\$3.85 (100)	Very-high-speed op amp.
	LT119AH	\$6.35 (100)	Dual comparator (commercial version LT319A is \$1.95 (100)).

Editor's analysis

All things considered, my opinion based on this project is that designing with an FPGA is actually easier than designing with SSI and MSI logic. You can use the same schematic design approach you are familiar with. You don't have to use simulation to design with FPGAs, but I'd highly recommend it. My first attempt at simulation wasn't perfect, but it got me close. Finding the last few bugs in hardware and correcting them was not a problem. Correcting the bugs did not even necessitate pc-board changes.

I no longer wonder what applications FPGAs are useful for, but rather what applications still make sense for small- and medium-scale integration TTL and CMOS logic. High-current bus drivers are one; extremely simple logic circuits are another. Some high-speed logic will favor SSI and MSI devices, but a number of FPGAs are available with the capability of loading and operating 16-bit counters in the 50- to 100-MHz speed range.

Price is perhaps the biggest barrier to FPGAs' taking over the low- to medium-volume logic market. At \$36.25 (100) for the device I used, it's competitive with SSI and MSI devices, especially if you factor in the cost of pc-board space and the flexibility to make design changes easily. As you move to higher-density and higher-speed FPGAs, you'll pay a premium over SSI and MSI parts.

formed as expected. These cases include counters, magnitude compares, optical-encoder signal decode, and others. Second, I simulated the FPGA as a whole, performing entire sequences of clearing, arming, recording, and playing back the data. Other simulation sequences tested the trigger-level and trigger-position-adjust operations.

My concerns on this design were mostly functional. Counters have to count, so I simulated all major transitions. In fact, it's a good idea to test all macros you create or alter separately. And because macros contain relatively few gates, they simulate quickly. Even though I tested the counter macros that I modified, I still tested the entire counter in the full schematic.

Because I had already run a place and route on the design, I could export the as-routed delays to the simulator and have a more accurate simulation. But I didn't want to use the as-routed delays at that time because I was still fixing a few bugs, and the unit-delay simulation provided a faster turnaround. I could change a schematic, recompile the simulation, and simulate in about five minutes. The turnaround time with as-routed delays requires a netlist transfer, design validation, place and route, and exporting the delays to simulation. The total time for doing all those things is about half an hour.

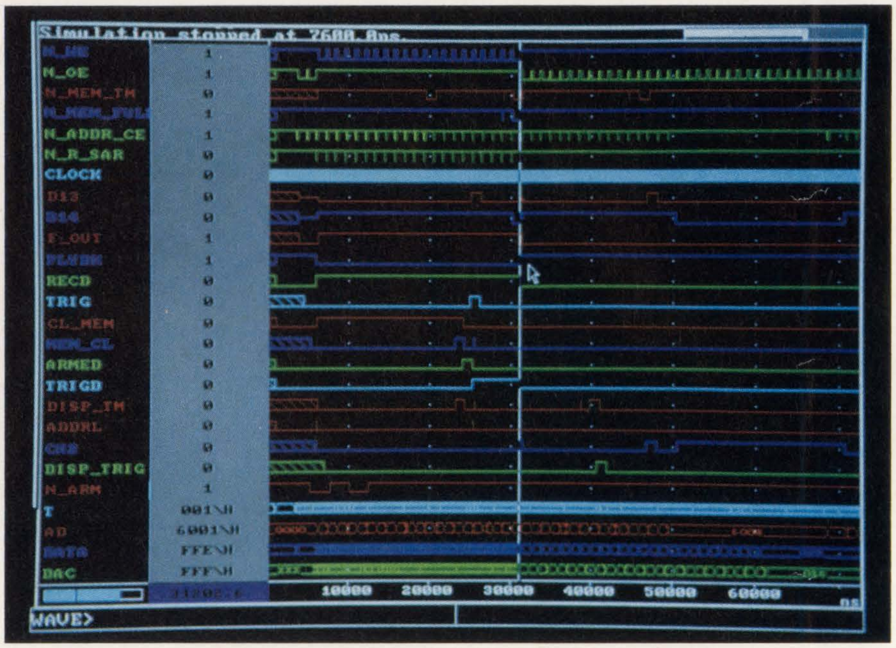


Fig 2—This sequence takes the design through reset, clearing memory, arming, triggering, completing data acquisition, playback with capture trigger marker, and end of data marker. To see more details, you need to zoom in as shown in Figs 3 and 4.

Fig 3—I've zoomed in to show a portion of the display in Fig 2 where the Memory Cleared (MEM_CL) signal indicates the memory has been cleared, and the FPGA changes its state to Armed. A short time later I force the trigger signal (TRIG) high, which causes the FPGA to change its state to Triggered (TRIGD).

Day 18

I spent lots of time on day 17 reading the simulation reference manual to understand the simulation commands and trying to figure out how to test my circuit with the available commands. By day 18 I was writing command files containing series of commands that initialize the FPGA and start taking it through its paces.

It seems incredible, but in two days I was able to learn enough to make simulation a useful tool. One of the attractive aspects of simulating an FPGA is that I didn't have to worry about simulation models. Anything I can design into the FPGA is covered by the simulation library. For this design, all the digital logic was in the FPGA, so I didn't see any need for board-level simulation.

Here are some of the bugs I found in one day (I corrected the bugs on the schematics in Part 1):

- D-14 needed to be gated so it only inhibited ADDR_CE (address count enable) on playback, not during record.
- &DISP_TM needed more delay so it wouldn't reset immediately when initiating CL_MEM. I had put in a delay, but simulation indicated it needed to be longer than I thought.
- The circuit was changing the compare multiplexer from compare 1 to compare 2 when the address changed during T2, instead of at the beginning of T1 (when it should happen).

I had been dreading simulation. I assumed I'd be bogged down in learning to use difficult software. Instead, I find myself a simulation convert—learning the software is reasonably easy. The bugs jump right out once you start exercising the circuit functions. It's just as much fun as debugging hardware, and you don't have to put probes on difficult-to-reach pins.

Day 19

I made a few changes to the successive-approximation logic and decided to create a soft macro (called SAR). I ran more simulation, and then I ran the place-and-route software and generated as-routed delay information for simulation. I spent a couple of hours making a final check of what remained to be simulated before I was ready to call simulation done.

The list of what was left to simulate seemed long, but because I was more familiar with the simulation commands and had simulation command files to perform most of the major functions on the FPGA, it went faster. I put simulations together quickly by calling initialization routines I'd already written, adding some commands, or modifying an existing command file.

I made some changes to the schematic and compressed the design onto fewer sheets. I then wanted to delete the excess pages, but couldn't find a utility for deleting schematic sheets. Instead, I deleted them from DOS.

A few hours later while simulating the design, things weren't quite right. I traced the problem to a 2-input multiplexer with the correct data going in, the correct data on the select pin, and unknown data on the output. I expected to find another output driving the net, but a double-check of the schematic indicated that that wasn't the problem.

This was my first, and only, serious problem with the simulation tools. It lasted for about two hours. Finally, I made the connection that perhaps the schematic sheets I deleted were not completely gone. It turns out that when you save a schematic sheet, the software creates a wirelist description file in the WIR directory. I deleted the files in the WIR directory for the schematic sheets I had deleted earlier, recompiled the simulation file, and was back on track. Of course, the simulation tools weren't really at fault, but I never did find anything in the documentation about how to delete schematic sheets properly.

I continued on to simulate the as-routed delays, exporting the delay information after a place and route into the simulator. The relatively short place-and-route time (approximately 15 minutes) is really useful when you make a design change and want to get back into a simulation with accurate timing.

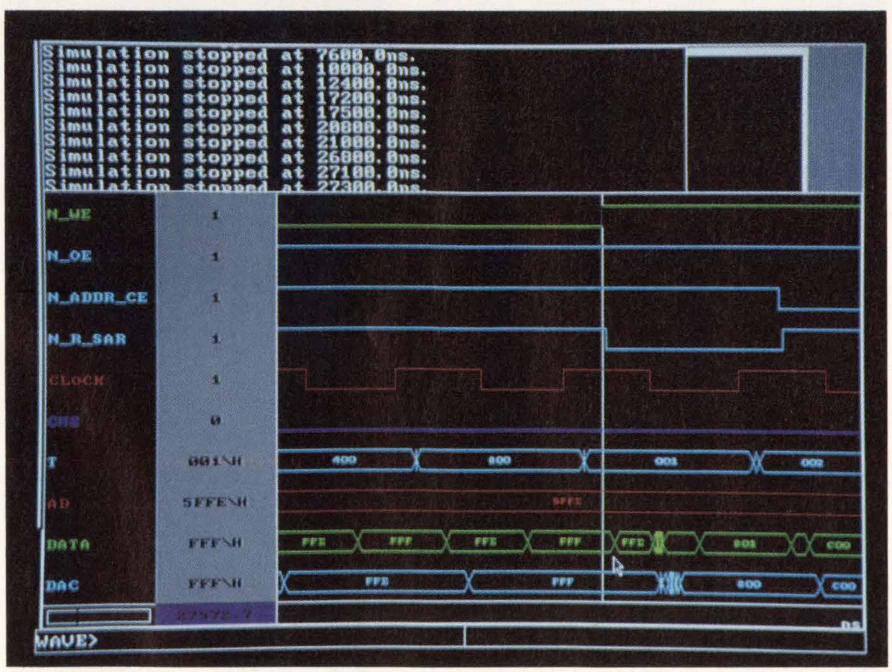


Fig 4—Zooming in still further on Fig 2, you can see the data written to RAM when the negative Write-Enable line (N_WE) goes high. Here I'm looking at the hold time on the Data bus.

Day 20

On day 20, my schedule called for having the design done and a functioning prototype board in one week, leaving me a week to tie up any loose ends before the article was due. However, I still hadn't got the design to the point where I wanted to freeze the FPGA pinouts. After that, I needed to lay out the prototype board, build the board, program the FPGA, and get the circuit working.

Later that day, while running through my simulation test cases, I discovered a serious error: The FPGA would never write the memory-full signal to D14 because of a setup timing error. The problem was very easy to fix, but it made me wonder how many other errors remained.

I made a few minor changes and tried to run a unit-delay simulation, which didn't work. All the timing is in even clock cycles, but unit delay simulation should give each logic module a 1-nsec delay. I'm reasonably sure what the problem is, but don't know how to fix it.

Once you run the place and route software and export as-routed delays, the simulation software shifts from unit delay to zero delay per interconnect. It then looks up the real delay for each interconnect in a file. Because I've changed the schematic, the software apparently knows it can no longer use the as-routed delay file, but it isn't resetting the simulation to unit delays. I could have called Actel and found out how to fix the problem, but I elected just to run the place-and-route software, export the delays, and get on with simulation. I was at the point where I needed the timing accuracy anyway. (After I finished the project, I called Actel and got the answer to my problem. After you export the as-routed time delays, the software creates a file named *design*.VAR in your work-view directory. You need to delete that file and run *export wirelist* in the schematic window to return to the unit-delay simulation.)

My particular design had very few cases of critical timing because I was running at low clock rates. My requirement was 2 MHz, and 10 MHz was my goal for the digital. The analog part of the design could play back at more than 2 MHz, but the record mode probably couldn't go beyond 2 MHz and still settle properly during conversion. With this extremely loose timing, I didn't have to make any changes for speed in the design; I was more concerned about saving gates.

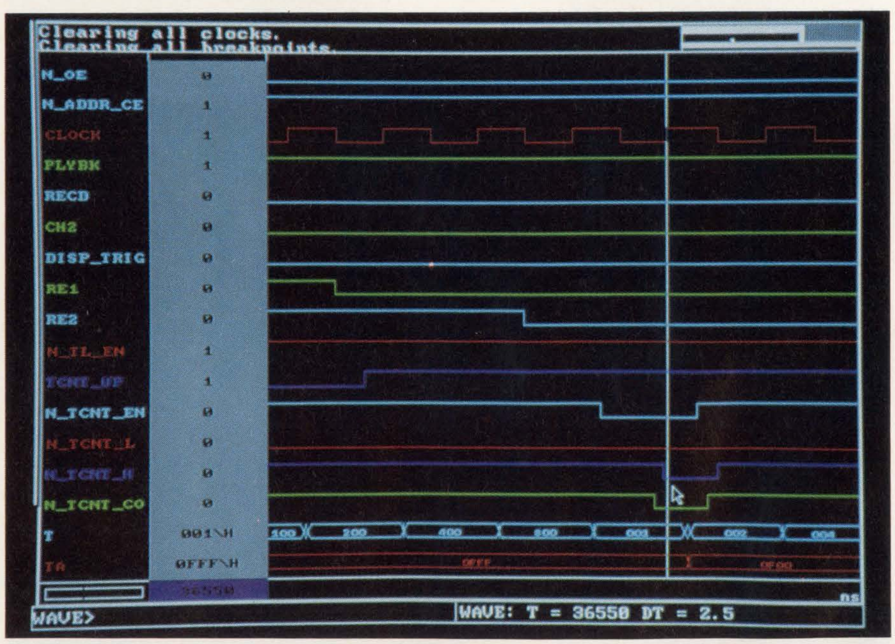
When designing faster circuits, you need to be sure critical networks don't end up with long interconnect delays. These long delays happen when two interconnecting modules are spaced far apart on the FPGA. The automatic place and route software attempts to place the design into the modules with a minimum of long interconnects. For this FPGA, long-vertical tracks are the worst, and long-horizontal tracks are the next worst. My design ended up having 16 long-vertical and 54 long-horizontal tracks.

The way you protect critical networks from long delays is with a network-criticality assignment. You can assign networks a criticality value of fast, medium, or uncritical. Fast or medium criticality keeps nets off long interconnects. You can designate as many as 5% of the nets fast and 15% medium. Assigning nets uncritical when they can tolerate long delays lets the routing software connect them with long tracks when necessary.

In my design, I designated fast criticality for the write-enable circuit because the tightest timing is at the end of a write cycle to the RAM. The RAM requires a zero hold time on the data when write-enable goes inactive. Initially, the design had a <10-nsec hold time in simulation, which should be okay. The fast criticality assignment widens the margin. Eventually, I added extra gating just to be sure my timing margin stayed on the proper side of zero.

Day 21

By day 21 I was still simulating. But since the circuit was in reasonably good shape, I started to push



Here I pushed the clock up to see where the circuit fails. At 20 MHz the signal enabling the upper 7-bit counter for the horizontal trigger position (N_TCNT_H) has only 2.5-nsec setup time before the rising edge of the clock, insufficient for the counter. You can see the Trigger Address bus (TA) does not make the transition from 0FFF to 1000 but goes to 0F00.

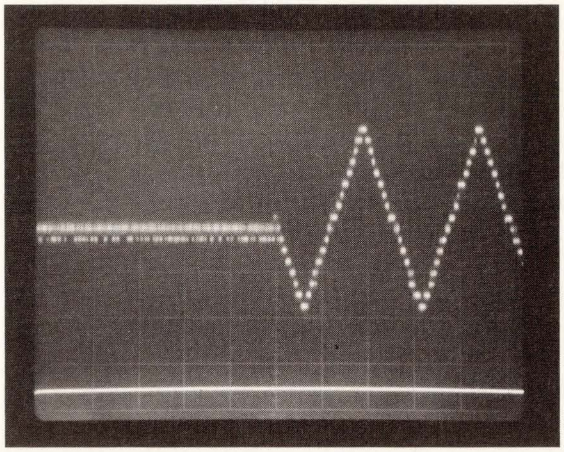


Fig 5—The waveform illustrates the record and playback circuit capturing a signal that changes from ground to a 1-kHz, 40-mV p-p triangle wave. The waveform was photographed during playback at twice the record speed using 0.2 msec/div and 10 mV/div. You can clearly see the 2.5-mV quantization levels. The pulse on the lower trace marks the capture-trigger location.

the speed. I had been working with a 2.5-MHz clock because that is all the speed I needed to have. I pushed the circuit up to 10 MHz, and then to 20 MHz.

At higher clock speeds, the simulator often puts out a warning that the circuit is not yet stable. What this means is that the results of the last data or clock transition are still propagating through the circuit.

An example of a relatively long path where I would get a circuit-not-yet-stable warning is in the trigger-level compare circuit. The 4-bit magnitude-compare soft macro was listed in the data book as having four module delays. The 2-bit compare had three module delays. The last bit to change in the compare will always be IDAC10, so this part of the circuit showed seven module delays through the comparator, plus three more modules to the TRIG signal for a total of ten module delays. Actually, the AND gate was combined with the latch when I compiled the design, so there were nine module delays.

Typical module delays, including interconnect, range from <6 nsec to approximately 11 nsec for a fanout of eight. Long tracks can push the delay to approximately 35 nsec. Using 10 nsec as a round number, the delay from a magnitude-compare input change to the trigger-signal output was 90 nsec. Because I hadn't specified any of the nets in the trigger-level compare circuit as being critical, long tracks could show up anywhere, even inside the soft macros. Because I had two clock cycles of 500 nsec each before I needed valid data for the nominal design condition, I wasn't concerned. Even if every module had a long track connection, the delay would be about 315 nsec. Of course, the as-routed simulation or the static timer would show just how long it takes to get through a given path.

When I simulated the circuit at 20 MHz and stopped it to view the data one 50-nsec clock cycle after a data bit had changed going into the trigger-level compare circuit, I would get a circuit-not-yet-stable warning. The simulator was still giving me the correct results at that instant, but it was also warning me that even if all clocks and external inputs freeze in their present state, some outputs have yet to reach their final state.

The simulation indicated that my FPGA would work at 12.5 MHz. If I needed the circuit to work at 20 MHz, I'd need to go back and start assigning fast and medium criticality to the appropriate nets or change the design.

With simulation complete, I spent the second half of the day laying out the circuit for the prototype board.

Days 22 to 24

Finally I got to the point where I was ready to freeze the pinouts. I had left them floating so that the place-and-route tools would have maximum flexibility to place and

The analog-circuit performance

The dc offset of the circuit from analog input to analog output is −5 to −7.5 mV. The dc gain error is within ±1 bit (2.5 mV) over the ±5V range, although the component specifications indicate you shouldn't expect better than ±2 bits. For better dc accuracy, you could trim the offset with an op amp on the input. Transition noise is approximately ±0.75 bit. I haven't been able to characterize the ac accuracy of the system to 12-bit accuracy.

The circuit is useful for examining signals to about 20 kHz with its 167-kHz sample rate. Filtering to avoid aliasing is a necessity if the circuit is used to examine signals with frequencies beyond 80 kHz. The 32k-word RAM provides 0.197 sec of storage with a 2-MHz clock speed. By slowing the clock speed to 12 kHz the circuit can sample at 1 kHz for more than 32 secs. During playback, you can increase the clock speed to 12 MHz for a flicker-free display on an analog oscilloscope.

route the design efficiently with a minimum of long tracks.

I had no more time for improvements. The only changes I could allow now were to fix bugs if I found them. As I transferred the FPGA pinout list to the full-circuit schematic, I discovered I hadn't brought out two signals—ARMED and TRIGD (triggered). I added the output pads, reran the place-and-route software, and got the signals. I used up 92% of the logic modules and 63 of the 69 I/O pins available.

On day 24, I assembled the prototype circuit. The prototype board was complete, except for an empty socket where the FPGA belongs. I created the fuse file for programming a chip, which took only a few minutes. Normally, you'd have the unit that you use to program the chip connected to your computer. When you're ready to program a device, you just put it in the programmer and run the software. I didn't have a device programmer, so I went to Actel to program my first chip. I didn't measure the time required to program a part, but I estimate it takes about 10 minutes.

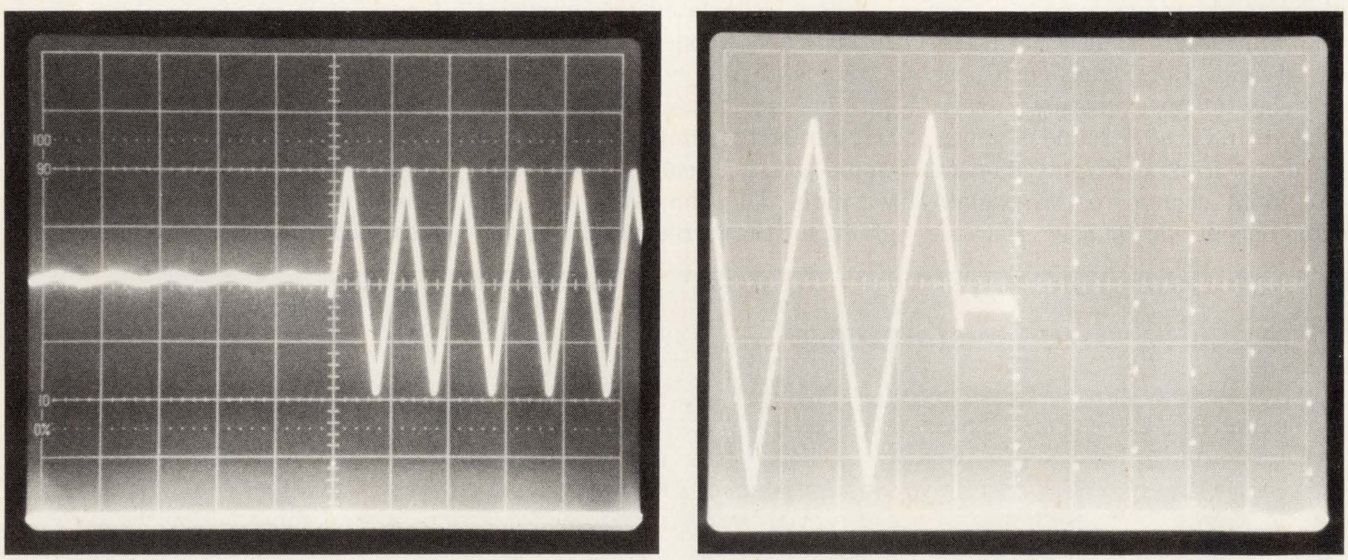
I plugged the part in the socket and powered up the prototype. I brought my power supplies and function generator with me to Actel and borrowed a scope. The circuit showed signs of life, but I couldn't get a good trigger from the display-trigger signal (DISP_TRIG). Gradually I came to the conclusion that the problem was the scope and not DSIP_TRIG. I asked for another scope and found that the circuit could perform all the basic operations. I don't know whether I was more surprised by my first FPGA design working, or that I handwired the prototype correctly.

I went back to my office for further testing, where I discovered a bug. As I turned the optical rotary encoder to adjust horizontal trigger position or trigger level, it occasionally jumped, rather than scrolling smoothly. The problem happened perhaps once in a hundred increments. The cause was a simple mistake: I had not synchronized the signal coming from the rotary encoder before using it in the circuit.

The rotary-encoder decode logic sets the count-up or -down signal correctly and then enables the counter for one clock cycle each time both rotary-encoder inputs are low. As the initial circuit was designed, the count-enable signal was set up for a random length of time before the clock. Most of the time the counter counted, sometimes it didn't, and other times it jumped because part of the count logic had sufficient setup time, and part of it didn't.

I ran the problem in simulation and it behaved just like the real thing. As I reduced the setup time below 5 nsec, jumps occurred on some count transitions. As setup time dropped below 2.5 nsec, the circuit just didn't count.

Adding a flip-flop to synchronize the signal solved the problem. If I were concerned about metastability, I would have added a second flip-flop. The effects of metastability in this application were not catastrophic and should be very infrequent with the long clock cycles.



(a) (b)

Fig 6—The record-playback circuit provides 2.5-mV resolution on a ±5V signal. The two scope photos here show the voltage range and resolution. In (a) you can see the circuit has captured an 8V p-p, 500-Hz triangle waveform when I switched out an attenuator on the function generator. The waveform is being played back at twice the record speed (1 msec/div and 2V/div). The same waveform in (b) is being played back with the oscilloscope settings changed to 20 mV/div and 0.5 msec/div.

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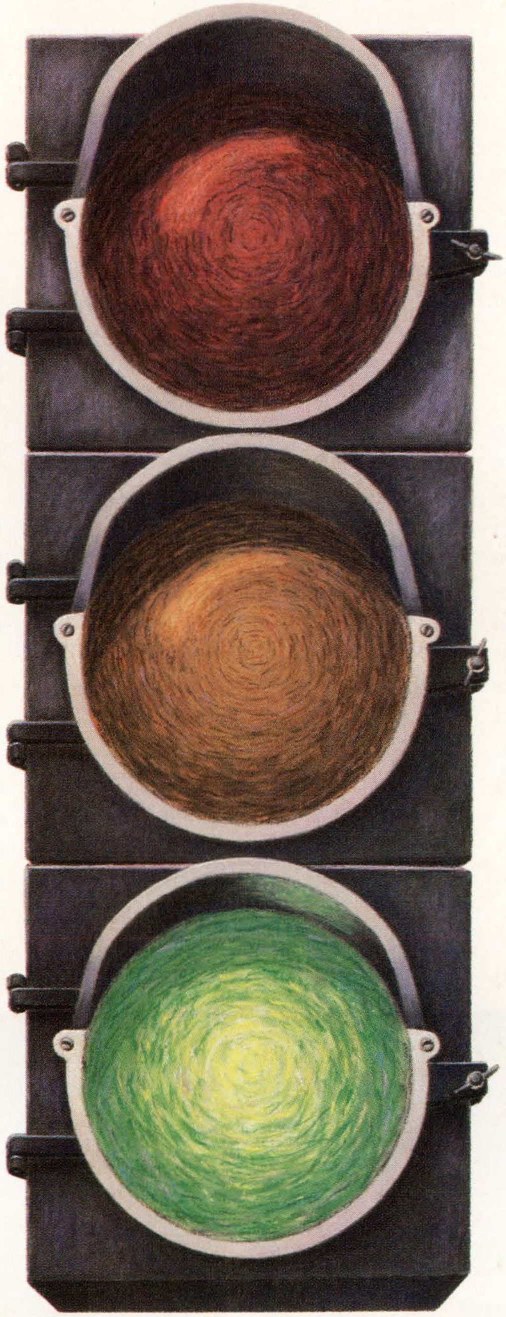

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Incidentally, I did not incorporate any debounce circuits for the switches because I previously concluded they were not necessary for this design. When switching the clock frequency, I assumed a reset was necessary.

Days 25 to 28

I added the flip-flop required to synchronize the encoder inputs to the schematic, then placed and routed the design. On this place-and-route run, all I/O pins were fixed. I resimulated all FPGA functions with special attention to make sure the bug was fixed. I also verified all other functions to make sure the place-and-route changes did not adversely affect other functions. Simulation indicated the FPGA should fully function at 12.5 MHz.

I spent the remainder of the day working over the analog portion of the circuit to get the best performance I could.

I went back to Actel to program a new chip. The problem was solved; the circuit now appears to work properly.

I spent more time on the analog. Digital is either right or it's wrong—analog can always get better. By the end of the day I decided I had done all I could for the analog and decided to take the weekend off.

By Sunday afternoon I couldn't stay away, so I spent an hour using the circuit to capture signals. I found a bug. The circuit was supposed to capture signals with 25% pretrigger data and 75% post trigger data. About half the time it worked correctly, and the other half of the time it captured signals with 75% pretrigger data. I couldn't believe I didn't notice this problem earlier.

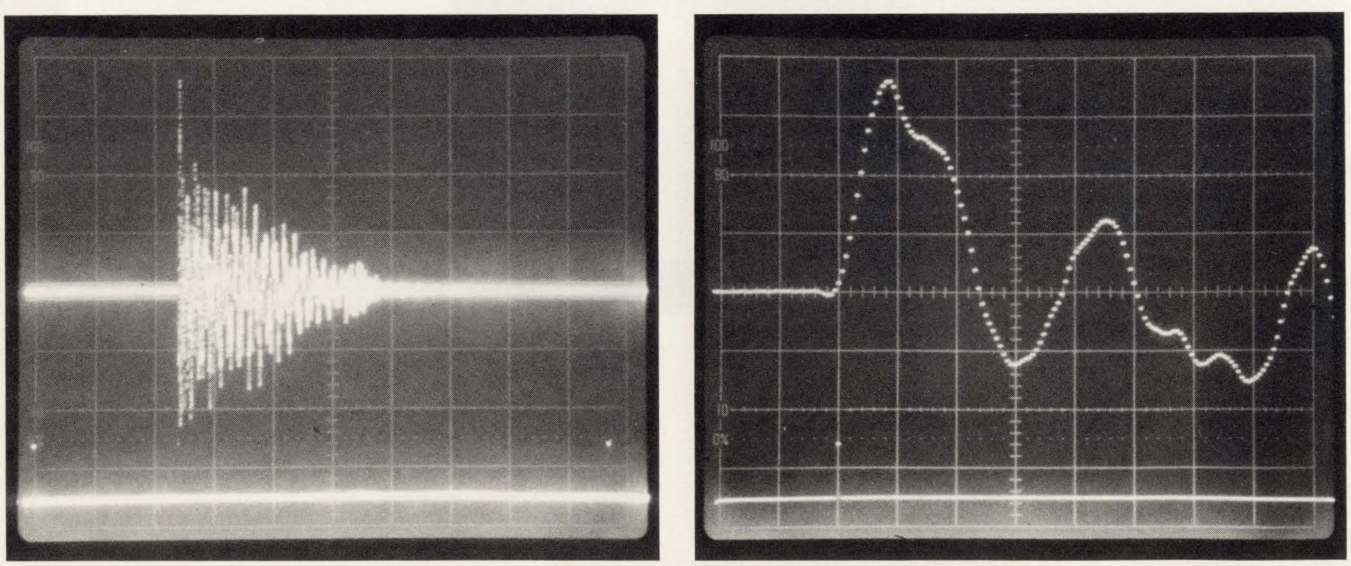
I was sure the error must be in how I computed the memory-trigger match signal (&MEM_TM), but it took me a while to see the problem. A simple logic error. The cases I tested earlier in simulation all worked properly. I added new test cases, and the bug showed up in simulation. I fixed the error by adding an XOR gate and reverifying the circuit in simulation.

I carefully tested the hardware one more time to make sure I couldn't find any more bugs. I went through the steps of placing, routing, and verifying that all simulations ran correctly. This time I sent my fuse files for programming the FPGA to Actel by modem. They programmed the part and mailed it back.

Day 29

The FPGA arrived. I plugged it in, and the circuit was fully operational. The project was finished. **Figs 5, 6,** and **7** show the circuit in operation.

The circuit was designed for recording with a 2-MHz clock rate. The clock-speed limit was set by the analog circuitry performing conversion. During playback, the circuit could run much faster. At 16 MHz, all playback functions appeared to work properly. Simulation indicated that the circuit was operating on the ragged edge at 16 MHz. At 20 MHz, some of the counters were



(a) (b)

Fig 7—The 32k-word record length provides 197 msec of data at 6-μsec intervals. The signal in (a) is an acoustic noise amplified from a microphone. The upper trace is the full record length. The lower trace shows the data beginning and end markers. The circuit captures the signal with 25% pretrigger data. Photo (b), 20 msec/div, 0.5V/div, shows the same waveform played back at 100 μsec/div. The capture trigger location is visible on the lower trace.

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occasionally causing errors because the ripple carry had insufficient setup time, just as simulation indicated.

Hindsight is 20/20

The first step in simulation, and perhaps the most difficult and important one, is to make a list of all the cases that require testing. Simulation can only find problems when you look for them. My faulty logic for determining when to stop the counter to acquire 25% pretrigger data was tested using two different start addresses. Both of them worked correctly. The counter was free running and could start on any of its 32,768 values, so I didn't think it practical to test them all. Had I given more thought to the problem, I might have tested a few more critical cases to verify the logic and find the problem in simulation.

My error in not synchronizing the optical encoder inputs was a careless design oversight. Although the problem can be found with simulation—I verified it with simulation after I found it—this type of problem could probably have been avoided by taking more care in the design process. Anytime you have asynchronous signals coming into a synchronous system, they demand plenty of careful consideration to make sure they won't have undesirable effects.

I did not make the same kind of careful schematic check I normally do before having a circuit built. I thought simulation would provide a more thorough job finding errors than my going over the schematic a few more times. I also felt the time pressure to finish the project.

I think simulation did help me make a more thorough check of the logic than I could have done without it. Simulation however, should not be a substitute for carefully checking your schematic to identify potential sources of trouble. Once you've identified potential problem areas, simulation can help you test them.

Although I had hoped to be able to report a fully functioning circuit on my first silicon, reality turned out different. In retrospect, my experience on the project probably points out the strong points of FPGAs. I don't know how many days or weeks I would have had to spend on simulation to find the two bugs that slipped through. The problems were easy to find in real silicon and didn't take much longer to fix than when you find them in simulation.

I wouldn't want to push the approach of finding your mistakes in silicon too far. Simulation provides a better way to test a design over the full operating temperature and voltage ranges plus manufacturing process variations. I think of finding mistakes in silicon as a fall-back position after you've done the best you can in simulation.

The realities of schedules that don't allow weeks to simulate a design as completely as you'd like may force you into a corner if it is vital that first silicon be final silicon. I used as much time as I had for simulation—about four and a half days, which included learning to use the software, and then went on to try the real device. It would not have been worth another week of simulation to find the two problems I found in silicon. I'd have a different perspective if I'd designed a mistake into a mask-programmed gate array and spent $10,000 and lost a few weeks before I found my mistake.

Had I made a design mistake that left the FPGA with serious functional problems, I could have used the diagnostic probe capability on the FPGA. The diagnostic probes let you look at any two nodes in the FPGA with an oscilloscope or logic analyzer.

I started this project with no experience designing FPGAs and none in digital simulation. I wanted to see if designing a circuit using an FPGA was really simple enough for a designer familiar with 7400-series TTL design to jump into expecting to produce the first cir-

The analog-circuit performance

For more information on the FPGA and design tools used on the project, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you read about their products in EDN.

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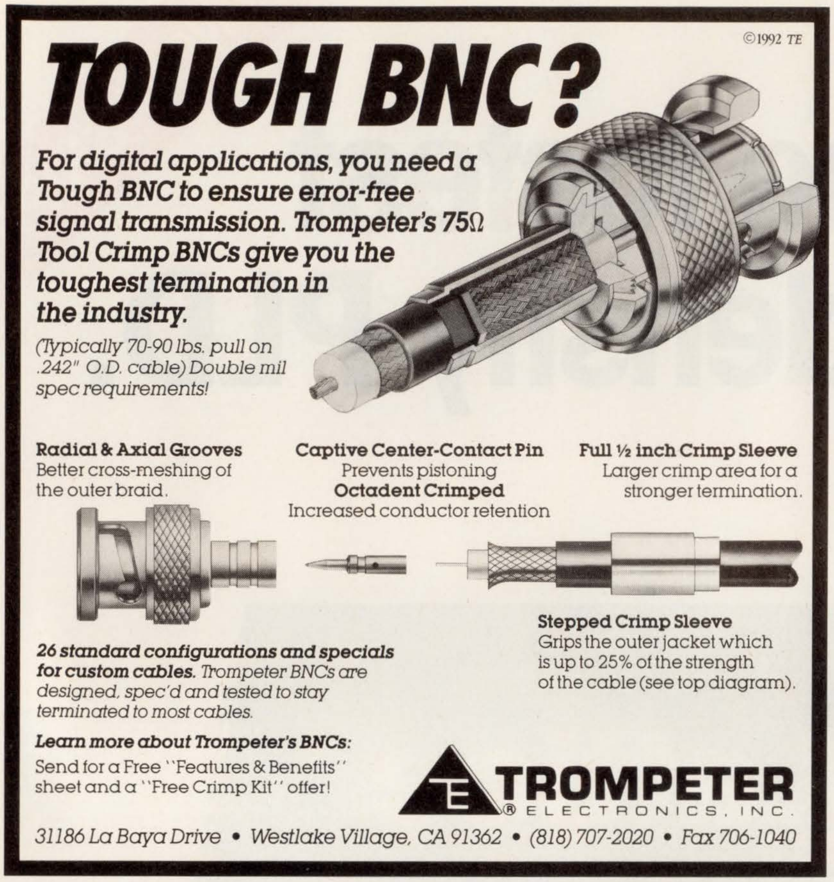

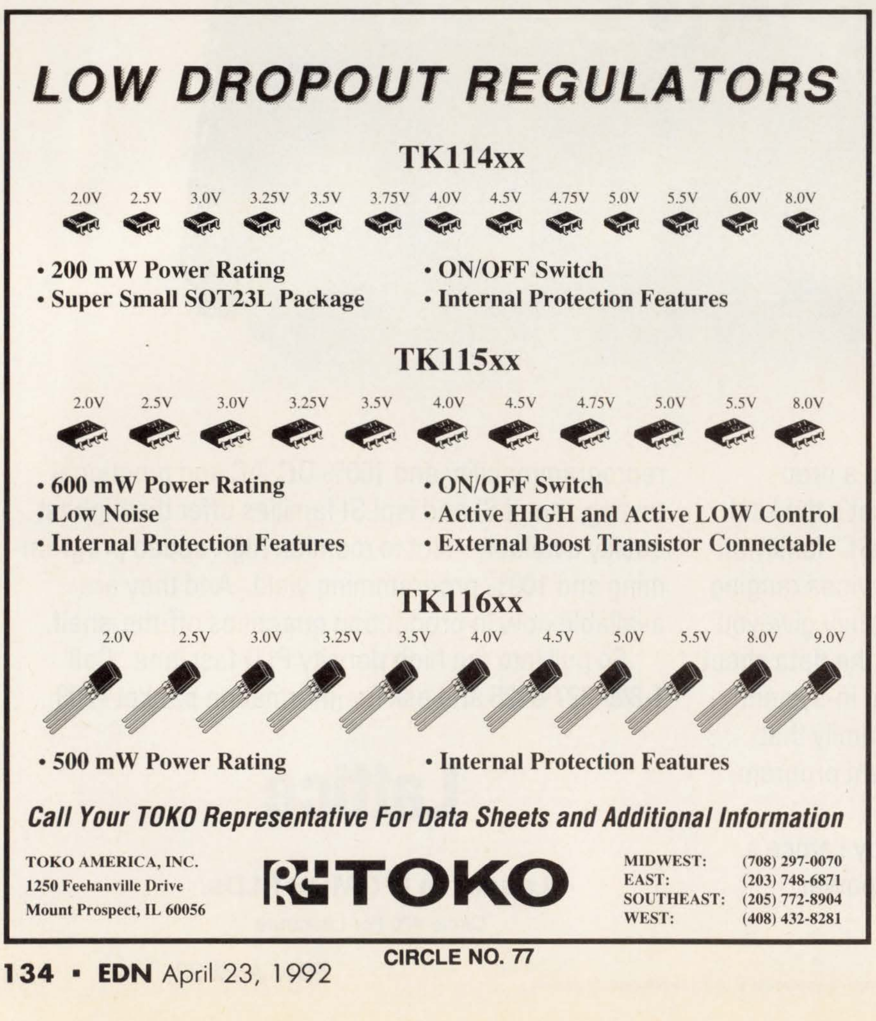

HANDS-ON FPGA PROJECT

cuit in a reasonable amount of time.

My conclusion based on the products I used on this project is that migrating to FPGAs is a step any design engineer should be able to make. You always have to stretch yourself when learning to use new tools, but the jump shouldn't consume great quantities of time while you come up to speed. In the course of this project, I've covered all the problems I had that were worth mentioning. There weren't many. In the end, my biggest problems were the normal system design issues of deciding what the circuit should do. Once I knew what I wanted to do, designing the circuit was relatively easy.

My biggest surprise was how well the software worked. I had a few problems, but frankly I expected more. My dread of simulation turned out to be unfounded. I actually look forward to using simulation on my next project. It's more enjoyable to find mistakes in simulation than in hardware.

For this project I chose a circuit that would not require high clock rates. As a result, I didn't spend any time refining the design to make it run faster. Had I needed the circuit to run faster, I'd have needed more time to refine the schematic and criticality file, and I'd perform more simulation runs. EDN

Acknowledgment

I'd like to thank the following companies for providing products for this project: Actel, Analog Devices, Hewlett-Packard, Linear Technology Corp, and Viewlogic.

Technical Editor Doug Conner is based in California. You can reach him at (805) 461-9669.

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MT4C16256 L	256K x 16 DW[1]	3Q92
MT4C16257 L	256K x 16 DC[2]	3Q92
MT4C1024 L	1 Meg x 1	Now
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MT4C1664 L	64K x 16 FPM[3]	Now
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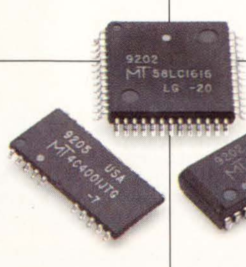

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5 Volt, Low Power, Low Voltage Data Retention SRAMs		
MT5C1001 LP	1 Meg x 1	Now
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MT5C1008 LP	128K x 8	Now
MT5C2561 LP	256K x 1	Now
MT5C2564 LP	64K x 4	Now
MT5C2565 LP	64K x 4 $\overline{OE}$[5]	Now
MT5C2568 LP	32K x 8	Now

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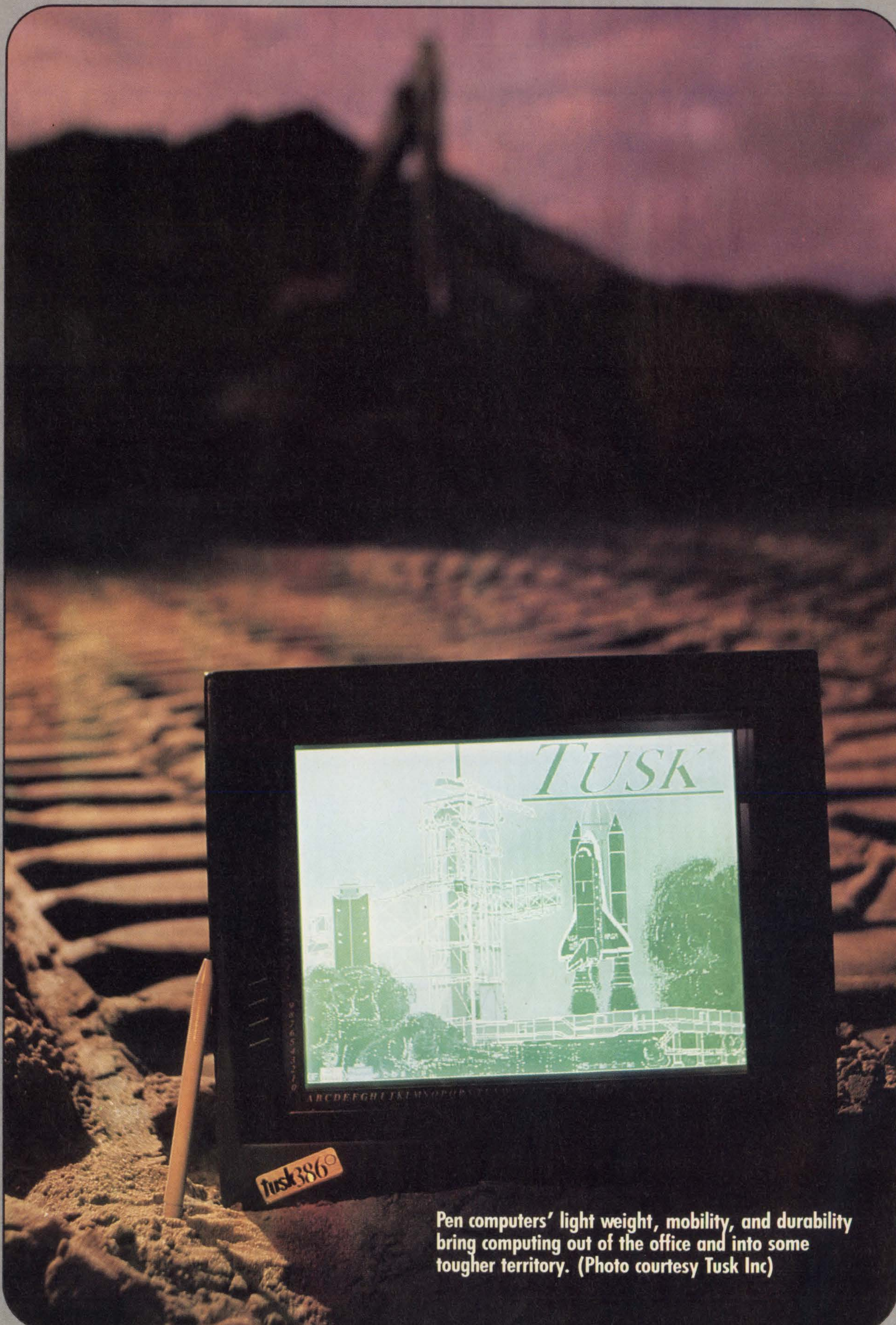


Pen computers' light weight, mobility, and durability bring computing out of the office and into some tougher territory. (Photo courtesy Tusk Inc)

Pen-based Computing

Pen computers still have problems recognizing handwriting, but their ease of use and mobility make them suitable in situations where conventional computers just won't do.

Gary Legg, Senior Technical Editor

On their way to becoming a huge overnight success, pen-based computers encountered a little problem: Although you can write directly on pen computers' displays with a pen-like stylus, the computers can't always read what you write. By most accounts, their ability to recognize handwriting has fallen considerably short of expectations.

Seemingly undaunted, pen-computer manufacturers now say that handwriting recognition isn't all that important. The real issue, they claim, is how well pen computers adapt to the whole range of users' needs. And they note that the pen, along with special software and handwriting recognition that is "good enough," makes it possible for computers to adapt to users and to real-world situations as never before.

But these same manufacturers are still striving for improved handwriting recognition, and their results, though imperfect, are nevertheless impressive. The best recognition algorithms achieve an accuracy of about 95% on carefully printed (not cursive) characters. That's good enough to make pen computers useful, but bad enough that they can still be frustrating to use. Consequently, most marketing efforts stress pen computers' intuitive appeal and mobility.

No experience required

The intuitive appeal is undeniable. Writing, marking, or drawing on a pen computer's display is almost as familiar as using pen and paper. In addition, special pen-based software eliminates much of the arcane "computerese" of keyboard commands, control codes, and file structures. The result, for people without computer experience, is a more familiar, intuitive, and perhaps acceptable way of working.

More important, though, is pen computers' mobility. Because you don't need a keyboard, you can use a pen computer while standing or even while walking around. The difference between the mobility of a pen computer and the mere portability of a laptop computer, which you can use only while sitting, is significant. The absence of a keyboard also increases ruggedness, making pen computers suitable for knock-about use in the rough-and-tumble real world.

The combination of intuitive use and mobility, say pen-computer developers, makes computing power available to the millions of mobile and/or blue-collar workers who, until now, haven't been able to use a computer on the job. Police officers, utility workers, insurance adjusters, field technicians, and truck drivers are just some of the potential (and current) pen-computer users. In many applications, pen computers replace paper forms, eliminating a data-entry step that would normally involve extra people and time.

To accommodate different needs, pen computers come in four basic types—palmtop, tablet, convertible, and omnitablet. All are small enough and light enough for at least some kind of mobile use, although some are more mobile than others.

The small, light palmtop, for example, is good for all-day use; it weighs barely more than a pound. The tablet type of pen computer is fairly light (usually between three and five pounds) and has a larger screen—big enough to display a computerized full-page business form. It's about the size of a notebook and about twice the size of a palmtop. The convertible pen computer comes with a detachable keyboard and doubles as a conventional laptop computer. The omnitablet is a somewhat hefty tablet that provides easy connection to a variety of devices.

Battery life an unknown variable

Battery life varies substantially from one pen computer to another. Poqet claims its palmtop computer will operate for 16 to 48 hours on two AA alkaline batteries. PI Systems claims 12 hours or more on eight AA batteries for its tablet Infolio. Some of the more powerful

Table 1—Pen-based computers

Company	Computer, type, price	Weight, dimensions	Processor/ clock frequency	Pen-based operating systems	Display (pixels)	Memory
Eden Group Ltd	VPI86, tablet, $3000 to $4000	4.4 lbs, NS	80386SX/16 MHz (optional 20 MHz) or Am386SX/20 MHz	Windows for Pen, Pen Point, Pen DOS	640 × 480, backlit	1 to 4 Mbytes RAM, 1 to 2 Mbytes flash EPROM
Grid Systems Corp	Gridpad, tablet, $2870 to $3570	4.6 lbs, 9.25 × 12.4 × 1.4 in.	NEC V20/9.54 MHz	Pen Right on MS-DOS	640 × 400, backlit	2 Mbytes RAM
Microslate Inc	Datellite 200S, tablet, $4395	5.0 lbs, 10.0 × 12.6 × 2.6 in.	80286/16 MHz (20 MHz optional)	MS-DOS with proprietary pen-capable shell	640 × 200, backlit	1 to 16 Mbytes RAM, 128 kbytes flash EPROM
	Datellite 300L, tablet, $5995	6.6 lbs, 10.0 × 12.6 × 2.6 in.	80386SX/16 MHz (20 MHz optional)	Windows for Pen, Pen Point, MS-DOS with proprietary pen-capable shell	640 × 480, backlit	4 to 16 Mbytes RAM, 128 kbytes flash EPROM
Momenta	Momenta Computer, convertible, $4995	Approximately 6 lbs, 10.4 × 11.9 × 2.4 in. (slopes to 1.2 in.)	80386SX/20 MHz	Momenta Software Environment (MSE) on MS-DOS	640 × 480, reflective (backlit optional)	4 to 8 Mbytes RAM, 250 kbytes flash EPROM
NCR Corp	NCR 3125 Notepad, tablet, $4765	3.9 lbs, 9.8 × 11.7 × 1.0 in.	80386SL/20 MHz	Windows for Pen, Pen Point, Pen DOS	640 × 480, reflective	2 to 20 Mbytes RAM, 8 Mbytes flash EPROM
PI Systems Corp	Infolio, tablet, $1895	2.9 lbs, 9.0 × 12.0 × 1.2 in.	Motorola 68331/ 16 MHz	Proprietary	640 × 480, reflective (backlit optional)	1 to 16 Mbytes RAM
Poqet Computer Corp	Poqet Pad, palmtop, $1995	1.2 lbs, 4.6 × 9.6 × 1.3 in.	NEC V20HL/3.5, 7, or 10 MHz software selectable	Pen Shell, Pen Right on MS-DOS	640 × 200, reflective	640 kbytes RAM
Samsung	Pen Master, tablet, less than $5000	4.9 lbs, 9.3 × 11.5 × 1.5 in.	80386SL/20 MHz	Windows for Pen, Pen Point, Pen DOS	640 × 480, backlit	4 to 20 Mbytes RAM
Tusk Inc	All Terrain Super Tablet, omnitablet, $5500 to $6500	6.5 lbs, 10.1 × 12.5 × 2.0 in.	80386SL/20 MHz (25 MHz optional)	Windows for Pen, Pen Point, Pen Shell	1024 × 768, backlit	8 to 32 Mbytes RAM

NS=Not specified

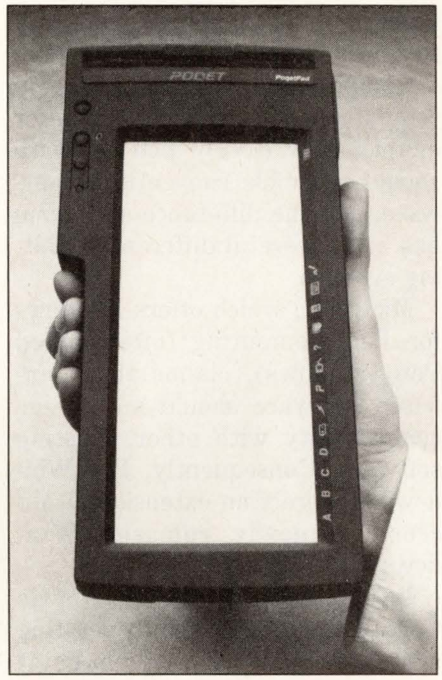
386-based systems may run for only three hours or so between battery changes or recharges. (Most of these systems use larger, rechargeable batteries.) Note, though, that it is difficult to compare operating times. Battery types and sizes vary from one pen computer to another, and there is no definition for the "typical" computer use that most manufacturers cite when quantifying battery life.

Although the hallmark of a pen computer is the pen itself, almost all pen computers have a keyboard connector. In addition, all pen computers have software that allows implementation of a "soft" keyboard on their screens; you operate displayed keys by touching them with the pen. This can be especially helpful if you get frustrated with the quality of character recognition.

Prices for pen computers range from less than $2000 to $6000 and up. The least expensive computers, PI Systems' Infolio (a tablet) and Poqet Computer's Poqet Pad (a palmtop), buck the trend toward the 386 processor. The Infolio uses Motorola's 68331, and the Poqet Pad uses NEC's V20HL. Grid Corp, which introduced mobile pen computing in 1989 with its 8086-based Gridpad, has recently discontinued its original product in favor of more expensive versions. Its lowest priced model now sells for $2870.

At the high end of pen computers' price range are products with hefty computing power and/or ruggedness for applications that aren't cost-sensitive. Tusk Inc and Microslate offer especially rugged units in the $6000 range.

Storage options	Interfaces	Options	Comments
2 PCMCIA card slots	Serial, parallel	LAN cards	May also be marketed by Tri Gem. Connects to external storage devices.
20-Mbyte hard disk, 1 or 2 PCMCIA card slots	Serial, keyboard, telephone	Barcode reader, modem, wireless communication	Grid has announced, and will soon be selling, an 80386-based pen computer and a 3-lb "wearable" computer.
3.5-in., 1.44-Mbyte floppy disk	Serial, parallel, keyboard, VGA, SCSI	Hard disk, RAM drive, modem, barcode reader, wireless communication	Ruggedized to military specifications. Used primarily for touch, not pen.
20- to 120-Mbyte hard disk	Serial, parallel, keyboard, VGA, SCSI	Floppy disk, RAM drive, modem, barcode reader, wireless communication	Ruggedized to military specifications.
40-Mbyte hard disk	Serial, parallel, keyboard, telephone	LAN adapter, wireless communication	Includes modem, fax, and detachable keyboard. Connects to external storage devices. Uses 10 AA batteries.
20-Mbyte hard disk, 1 PCMCIA card slot	Serial, parallel, keyboard, VGA	Modem, fax	Connectors to external devices are in optional extension unit that attaches to end of computer.
3 PCMCIA card slots	Serial, 96-pin expansion bus	Desktop docking module, modem, fax, wireless communication	Eight AA batteries run computer for as long as 12 hours.
2 PCMCIA card slots	80-pin bus (has signals for serial and parallel interfaces)		Withstands 100-G shock (3-ft drop to concrete) while operating. Two AA batteries run computer for as long as 16 hours.
60- to 120-Mbyte hard disk, 1 PCMCIA card slot	Serial, parallel, keyboard, VGA	Fax, modem	
Single or dual 60-, 80-, or 120-Mbyte hard disks; 3.5-in. floppy disk	ISA bus, serial, parallel, keyboard, VGA, telephone	Fax, modem	Ruggedized, EMI shielded; sealed, waterproof case.



Poqet Computer Corp's Poqet Pad, a so-called palmtop computer, weighs 1.2 lbs. It sacrifices screen area for increased battery life.

Pen adds little to cost

Pen computers' price tags aren't unduly influenced by the pen itself. Pen hardware (pen and digitizer) adds as little as $50 to a computer's manufacturing cost, or perhaps $200 to its end-user price. Manufacturers are using several different pen and digitizer technologies (see **box**, "The write stuff: pens and digitizers"). Each type has advantages and disadvantages; it's still too early to tell which will prevail.

Competition also exists in pen-computer software. Opinions differ on just how closely pen software should resemble conventional software, and the difference of opinion has led to several different operating systems.

Microsoft, which offers Windows for Pen Computing (often called Pen Windows), claims that pen-based software should not forego compatibility with other, existing software. Consequently, Pen Windows is merely an extension of Microsoft's newly released Windows 3.1.

In opposition to Microsoft is Go Corp, with its Pen Point operating system. Go designed Pen Point specifically for pen computing and claims a fresh, clean operating system without any of Windows' conventional-computing baggage. Similarly, Momenta started with a clean slate for the Momenta Software Environment (MSE) on its convertible pen computer.

A third approach to pen-computing software puts a user-interface shell with pen capabilities on top of MS-DOS. This scheme dominates in lower-priced pen computers that don't use the 386 processor, although it is also suitable for 386 models.

Because the pen-capable DOS shell preceded the dedicated pen operating system, shells are available mainly from companies with early experience in pen computing. Pen pioneer Grid, for example, runs its Pen Right shell on its own computers and has recently begun licensing the product to others. Pen DOS, a shell from Communication Intelligence Corp (CIC), and Pen Shell, from Nestor Corp, both sprang from efforts in handwriting recognition. Some pen-computer vendors also have their own, proprietary DOS shells.

OS choice depends on user

The choice of a pen-computer operating system depends largely on the intended user. Pen Point, for example, is good for new, unsophisticated computer users. Its ease-of-use features include a display of program options in the form of a book's familiar table of contents.

Pen Windows aims at the broader market that includes existing Windows software. It runs existing

The write stuff: pens and digitizers

Pen computers implement their electronic "pen and paper" in several different ways. The pen may be electrically tethered or untethered, and it may be electronically passive or active. The "paper" (digitizer) may sense pen contact or even the pen's mere proximity to the digitizer surface. Some digitizers can also sense a finger's touch and distinguish between pen and finger.

Digitizers come in two basic types—the overlay, which goes on top of the LCD screen, and the underlay, which goes below. Overlay digitizers, using either resistive or capacitive film, respond only to contact. Underlay digitizers are usually electromagnetic and can sense either pen contact or proximity. Both types satisfy handwriting recognition's resolution requirements of 150 to 250 dots per inch, and some digitizers go considerably beyond that requirement. (Pen computers' LCD screens display only about 75 dots per inch, however.)

Overlay digitizers go well with backlighting because they're transparent. With an underlay, backlighting is more complicated, because a grid of wires (usually in an opaque board) must go beneath both the LCD and the backlight. Careful component placement and signal phasing is necessary to prevent signals in the LCD and the digitizer from interfering with each other.

An electromagnetic digitizer has no problem sensing through the LCD and the backlight, but the gap between pen and digitizer presents a potential parallax problem. The alignment of the digitizer's grid wires with the display's pixel rows and columns was initially a problem, but manufacturers now compensate in firmware for any misalignment.

A pen computer needs either a hard writing surface, a soft pen, or both, so that long-term use of the pen won't damage the screen. For a computer with an underlay digitizer, the writing surface is usually a layer of plain glass that protects the LCD; with an overlay digitizer, the glass surface has a transparent coating, either resistive or capacitive, that is itself subject to wear. In either case, writing will be difficult if the surface is too smooth. Consequently, the glass needs to be slightly etched to provide a realistic pen-and-paper feel.

The wrong etch will cause problems, however, perhaps reducing display quality or retaining smudges from fingertips. In addition, if the glass is too rough, it will quickly wear out the pens that write on it. Developers of pen computers are still investigating different materials for pens and writing surfaces.

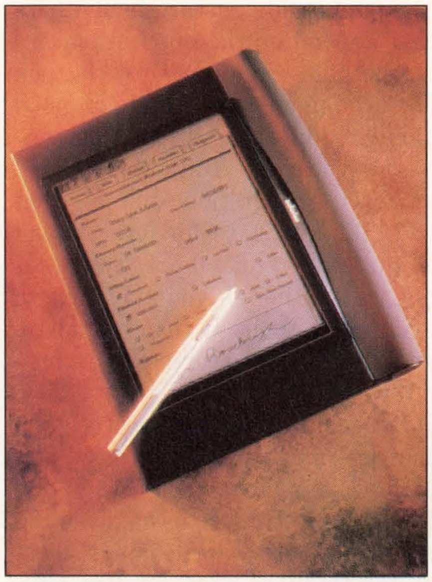
Windows application programs without changes; if a program uses a mouse, the pen simply replaces the mouse. Pen Windows is a good choice for users who need to run the same applications in both mobile and desktop computers. Pen Windows also comes with an installable shell to shield unsophisticated users from its arcane details.

Time will tell which operating systems are successful, but for now, Pen Windows seems to have the edge. Bruce Langos, director of strategic product planning at NCR, reports that the Microsoft OS is favored by about 60% of customers for NCR's 3125 tablet computer. Go's Pen Point gets the nod from 30% of NCR's customers, and CIC's Pen DOS gets the rest. Langos notes that Pen DOS has recently been gaining strength.

The most intense software competition, however, may be in the area of handwriting recognition. Because there's so much room for improvement, anyone who creates a better recognition package will probably reap enormous benefits. Although CIC and Nestor were involved in recognition before pen computing came along, the potential market for pen computers has, no doubt, increased their efforts. Both companies sell their recognition software separate from their DOS shells, and both emphasize their recognition business over their shell business.

Putting the OS before recognition

OS developers Microsoft and Go Corp take just the opposite approach. They develop and sell recognition software with their pen operating systems, but they stress their OS business. Both Pen Windows and Pen Point can operate with recognition software from other vendors. Grid, since its introduction of pen computers, has provided its own recognition algorithms. Momenta, likewise, sells its own recognition software on its Momenta computer.

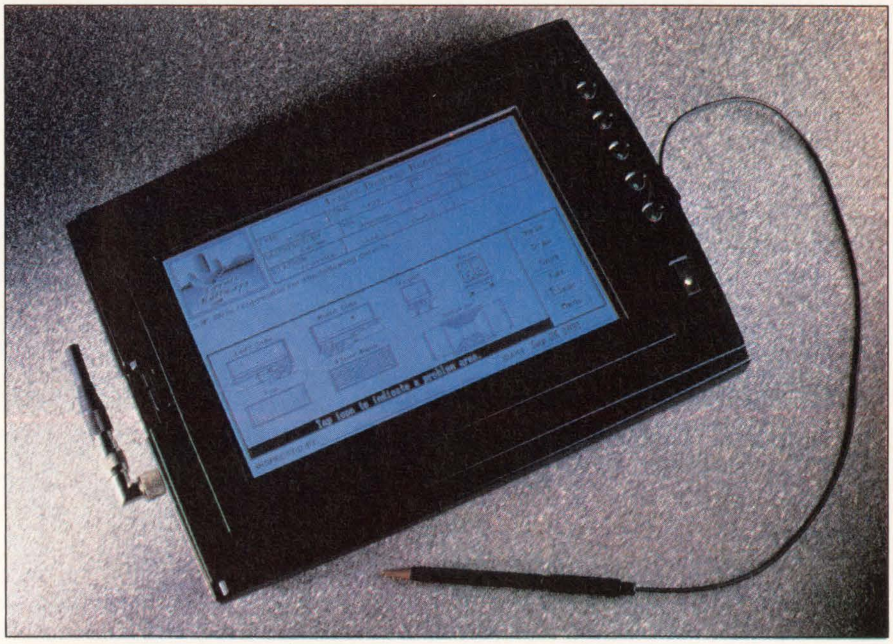


At 2.9 lbs, the Infolio pen computer from PI Systems is the lightest of the full-sized tablets.

Although existing handwriting-recognition software can be disappointing, it is nevertheless impressive. It will recognize neatly printed characters in real time, and most recognition packages can identify some unconnected script letters. Some systems can even adapt to users' individual writing styles. Recognition software can't decipher connected cursive writing, though, and it has accuracy problems even with neat printing (see **box**, "The problem of reading your writing").

However, if a software application requires only menu selections or a check-off type of user input, then a pen is definitely adequate and possibly preferable to a keyboard. A pen is also easier to use than a mouse for some pointing and selecting operations. With a pen computer, the pen is always in your hand; you don't have to move your hand from a keyboard to a mouse and back. As NCR's Langos notes, "Once you use the pen to maneuver icons, you'll wonder why you ever used a mouse."

In addition, a pen allows image input—signatures and sketches, for example—that a pen computer can



Grid Corp's Gridpad RF pen computer uses spread-spectrum radio transmission to access a Novell local-area network.

capture as "electronic ink." A physician's signature in electronic ink may be acceptable to a health insurance company, whereas a signature converted to ASCII text would not be. An architect could sketch changes to a computer-resident blueprint without ever needing handwriting recognition.

To gesture is to command

A pen also permits gestures—simple and intuitive strokes that convey commands to a pen computer. Examples of gestures include a hand-drawn caret "â" to begin a text insertion and a hand-drawn "x" to indicate a deletion. Go's Pen Point has 11 standard gestures; Microsoft's Pen Windows has 11 system-wide gestures and others that depend on the application.

All these advantages of the pen don't eliminate the need for good handwriting recognition, but they do alleviate it. And, in the final analysis, recognition isn't all that bad. It's adequate for interpreting commands and short text sequences, although you may have to print more carefully than you'd like, and you'll have to correct some misinterpreted characters.

Pen-computer vendors figure that users can live with those limitations, for now at least. While freely admitting that handwriting recognition has shortcomings, most of the vendors also express optimism about its future. As this article was in preparation, many of the recognition packages were just being readied for formal release at the spring Comdex computer exhibit. The released versions, according to their suppliers, will have many bugs worked out and will achieve significantly greater accuracy. The next few months, as actual customers put handwriting recognition to the test, will determine if those claims are valid.

Whatever happens with recognition, the essential requirement, which pen computers meet, is mobility. Users may prefer lighter computers, but at least they can use the current crop of pen computers while walking around.

Mobility implies more than in-

The problem of reading your writing

Pen computers do only a fair job of converting handwritten characters to computer-resident text. Plus, they require you to print, not write, and some restrict you to printing in little boxes. Too often, they make mistakes.

The main problem is the tremendous variability in the way people write. Not only do different people write differently, but an individual's writing varies with circumstances. We don't write the same way when we're tired, for example, as we do when we're rested. We don't write the same while standing as we do sitting.

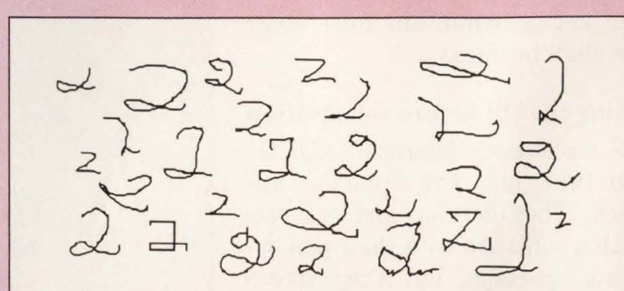
Developers of handwriting-recognition software are reluctant to disclose the methods they use, but they take many different approaches. Microsoft claims to have combined numerous approaches that have been investigated over the last 15 to 20 years and documented in technical literature.

Some recognition software adapts to your writing; with others, you must adapt to the software, perhaps forming some characters a certain way. Recognition accuracy improves if the software (often referred to simply as a recognizer) is adaptive. However, in order for a recognizer to adapt, you have to train it. You train a recognizer by printing some amount of text that the recognizer already knows.

Even with adaptation, recognition accuracy is limited. A good recognizer will correctly interpret about 95% of the characters you print. Sometimes—depending on the system, the user, and circumstances—accuracy is considerably lower.

That's the character-recognition accuracy. Word-recognition accuracy is worse. Assuming five characters per word, word accuracy is the character accuracy raised to the fifth power. Thus, a recognizer that correctly identifies 90% of the characters you print will, on average, correctly interpret only 59% of your words. The remaining 41% will be misspelled.

Humans wouldn't do much better at interpreting handwriting if they weren't adept at reading characters in context. On average, people looking at isolated characters can correctly identify only 96% of the characters



Extreme variability in hand-printed characters makes recognition by a computer difficult. These samples of the numeral 2, provided by Nestor Corp, illustrate the problem.

hand use, though. It also implies use in multiple locations, which, in turn, implies the need for connection with other computers and systems. Several pen computers meet this need with optional wireless communication. A few employ the concept of docking, in which a mobile pen computer is a drop-in component of a larger system.

Tusk, more than any other pen-computer company, seeks to capitalize on docking. Its All Terrain Super Tablet computer, an omnitablet, has a 200-pin connector that incorporates the entire ISA bus, enabling connection to virtually any type of external device.

What is perhaps more significant, though, is the ease of connecting the Tusk computer to a docking station. Docking is not the same as plugging in a bunch of cables; it is very much like inserting the computer into a slot. A specially designed connector on Tusk's computer makes that insertion almost effortless; thus, the docking concept is feasible even in cramped environments and for users who haven't the time, patience, or inclination to connect cables. Tusk president Chuck Krallman notes that one of his company's customers has installed docking stations on the dashboards of police cruisers.

Such mobile, knock-about use requires rugged hardware. All pen computers probably benefit from advances in reliability fostered by laptop computers, but some go well beyond that. A few companies, notably Tusk and Microslate, have gone to great lengths to ensure ruggedness.

The housing of Tusk's computer, for example, is made of Spectra, a material from Allied Chemical that is also used to make body armor. Tusk found that high shear strength was necessary to keep the housing from flexing and destroying internal components. Composite materials, such as Kevlar and carbon fiber, are high in tensile strength, but not shear strength; Spectra, on the other hand, can resist the extreme shear loading of fired bullets.

Tusk also used a special shock-mounting material for its om-

that they, themselves, have written earlier, according to Ted Fligor, director of sales and marketing at Nestor. With context, however, accuracy increases dramatically. Recognition software uses context, but not nearly as well as humans do.

To apply context at all, recognizers require assistance from the application programs they work with. A well-designed application program has a 2-way conversation with the recognizer; it passes preprocessing hints to the recognizer, and the recognizer passes back alternate character interpretations, each with a confidence value.

Fast enough for real time

The speed of handwriting recognition in pen computers is adequate, given that users must print carefully. In general, recognition takes considerable computing power, such as that of an 80386. Grid's recognition software runs on a 10-MHz V20, however, and Nestor's recognizer runs on the Poqet palmtop's 7-MHz V20.

User acceptance of imperfect handwriting recognition may depend less on recognition accuracy than on other factors, such as how easy or hard it is to correct misinterpreted characters. Whether or not users will be willing to adapt to a certain way of printing remains to be seen.

Future recognizers may benefit from implementations in hardware, and some may use neural networks. And, potentially, recognizers can take advantage of additional inputs. Existing recognizers accept only x/y coordinates and pen up/pen down information. Current pen-based hardware and operating systems can provide more, however—pen pressure, velocity, acceleration, and tilt, for example.

These extra parameters are already useful in specialized signature-verification systems, but they can confuse the existing general-purpose handwriting recognizers. Nestor's Fligor notes that a person always signs his or her name the same way, even when tired. That is, although the letters may look a little different, the velocity and pressure are always similar. In other writing, however, people write more slowly when they're tired.

No quick fix

The near-term outlook for handwriting recognition is uncertain. Some people in the pen-computing business claim to see rapid improvements, but others are more skeptical. As one source notes, "People have been working on this problem for 20 years. They're not going to solve it in the next two or three months."

nitablet's hard disk, screen, and mother board. On impact loading, the material flashes to a liquid and then back to a solid. The reaction is very localized and fast—on the order of milliseconds.

The Datellite pen computers from the Canadian company Microslate meet Canada's Department of National Defense military specifications. In testing, the computers tolerated 400-g shocks with the hard disk running. They also withstood ten days of humidity extremes.

So-called "enviro end caps" increase the Datellites' resistance both to shock and humidity. The ribbed caps seal against water and humidity and also act as rubber bumpers. If you drop a Datellite on a flat surface, only the end caps will make surface contact.

Such ruggedness, along with mobility and ease of use, seems to indicate a promising future for pen computers. Although most pen computers aren't as durable as Tusk's and Microslate's, their compact and keyboard-free forms provide a certain amount of inherent ruggedness.

The exact direction and timing of pen computers' success remain uncertain, however. In application-specific vertical markets, where there is plenty of demand for pen computers, prices need to fall. Several thousand dollars is a lot of money to spend on a computer that a truck driver, for example, would use to log deliveries. In the horizontal market of general-purpose computer use, cost is not such an issue, but, also, the demand for pen computers isn't strong.

Still, the pen is a cheap bonus and may find wide acceptance. Because its added cost is not very significant for 386-based systems, manufacturers of notebook computers can add it as a selling point. NEC's Ultralite SL/20P is just such an example; the computer is simply an Ultralite SL/20 with an added pen and digitizer. If there is great appeal for the pen, notebook computers may give way to convertibles. In addition, a consumer market for special-purpose palmtop pen computers will probably emerge.

In another scenario, the pen could find success via an indirect route, through what we might call a Trojan mouse. The mouse is already inside computer users' walls and is well accepted as a device for pointing and selecting. But the pen, easier and more intuitive to use, is not only good for pointing and selecting, but also has potential for

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writing. The mouse, having opened the door to point-and-click computer control, could find itself replaced by its more capable pen offspring.

If success for the pen does come in that manner, the term "pen computer" may simply disappear. We won't think of pen-based computers; there will simply be computers that have pens. Whether or not they have keyboards will depend on their intended use. EDN

Reference

1. Hathaway, Kevin, and Jeffrey Hawthorne, "An LCD to write on," *Information Display*, October 1991, pg 10.

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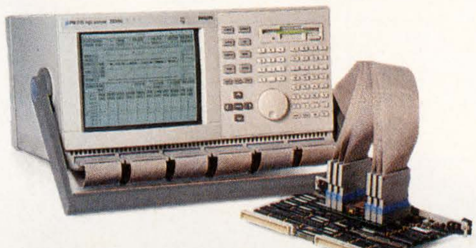

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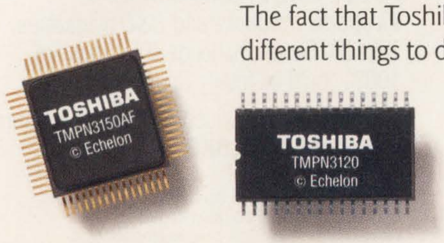

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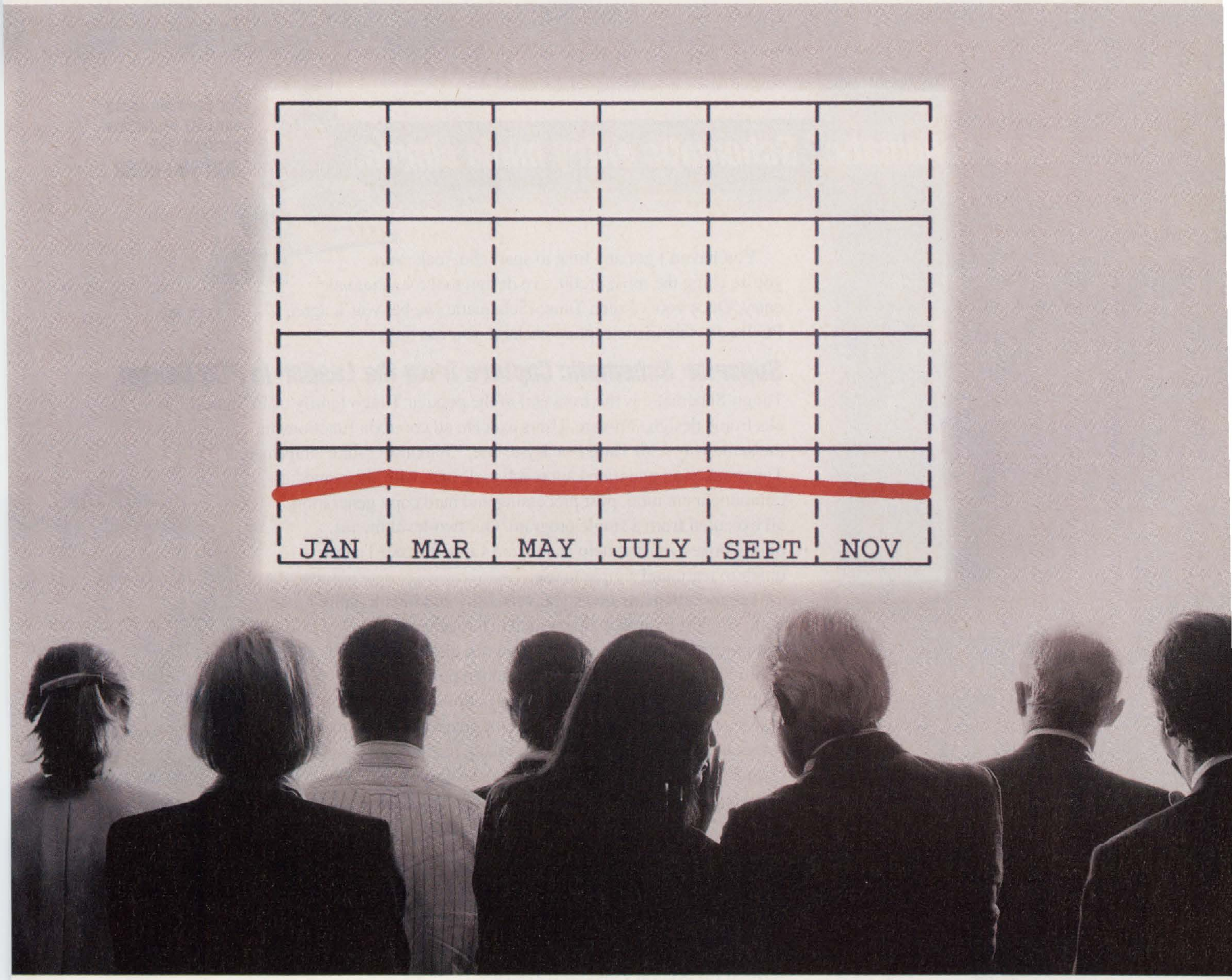

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CIRCLE NO. 83

Combine C and assembler to program powerful DSP processors

Steve Denny and Stephen J Roome, Data Sciences

Implementing a digital-signal-processing (DSP) algorithm on a powerful processor such as the AT&T DSP32C may seem intimidating. However, if you approach the task in a methodical manner and with the correct tools, the programming will be a straightforward exercise.

Engineers have traditionally programmed computationally demanding DSP algorithms in assembly language. Although DSP μPs' specialized architectures contribute to the chips' power, these architectures make the processors difficult to program in assembler. C compilers are generally available for current-generation DSP μPs, but the efficiency of the code they produce is well below that a skilled assembly-language programmer can obtain. By using the following common-sense, 3-stage approach to programming a DSP μP you can combine the advantages of both C and assembler.

DSP μPs share three characteristics **(Ref 1)**. First, they are reduced-instruction-set-computer (RISC) processors—that is, each instruction takes one instruction cycle and the instruction set is irregular. Second, they carry out several operations in parallel. And third, they are pipelined—an instruction's execution takes several processor cycles.

The μP vendor will have development software for one or more computers—usually including the IBM PC. Development software should include a C compiler, a macro assembler, a linker, libraries of common functions, a software simulator, and copious documentation.

Many third parties manufacture DSP boards based on the currently available DSP μPs **(Ref 2)**. Adding one of these to your setup provides an economical and immediately available test bed on which to try out your code.

Initially program in C

In the first stage, code your DSP algorithm in C while making no particular effort to obtain an efficient implementation. The straightforward manner in which you can code a mathematical description of an algorithm in C lets you concentrate on the important issues such as signal representation and buffering strategy. You should test your software as thoroughly as possible before proceeding to the next stage.

Here are some tips for the first stage:

- Use multiple source files and a make utility such

Listing 1—Straightforward C implementation of speech-processing algorithm

```
/*********************************************************************/
/*   Update the autocorrelation estimates.              Rev 1.0     */
/*                                                                   */

/*   Update the autocorrelation estimates for values of             */
/*   time-shift, m given by m = (4*i + cycle), for values           */
/*   of i from 'first_i' thru 'last_i'                               */

void update_Rxx(x, first_i, last_i, cycle)
   float x;
   short first_i, last_i, cycle;
{
      short i;

      for( i = first_i; i <= last_i; i++ )
         R[4*i+cycle] = ( GAMMA*R[4*i+cycle] ) + ( x*X[i] );
}
```

as Microsoft's Make. Multiple source files reduce compilation time, and a make utility ensures that the numerous compiler and linker parameters are correct or, at least, the same.

- Declare the return values of external functions. Functions you define in another source file can be a source of errors because the compiler will assume that these functions return integer values if you specify no return type.
- Use a lint program such as PClint. Lint is a type of C compiler that does not produce object code but checks for errors more comprehensively than a standard C compiler does. Lint performs strong type checking and also warns of code likely to be implementation dependent.
- Use static variables for easier debugging. C usually keeps variables on the stack. The C compiler adds a preamble to each function's executable code. The preamble allocates memory for stack variables when the function begins and releases stack memory on exit. Declaring a variable as static fixes it in memory.
- **Ref** 3, *C Traps and Pitfalls*, is particularly useful.

Interrupt routines

Your DSP software is likely to contain interrupt routines. You can write these routines in C if you follow this simple scheme. Write the interrupt routines as C functions that take no parameters and return no values. Then write an assembly-language interrupt-routine "shell" to call your C interrupt routines. The shell routine first switches to a new stack, saves registers if necessary, and then calls the appropriate C interrupt routine. (The DSP32C has shadow accumulators but no shadow registers. For more information on this DSP µP, see **Ref** 4.) When the C interrupt routine finishes, the shell restores the registers and stack and then executes the return-from-interrupt instruction.

Keep the following tips in mind when writing your interrupt routines. Do not share the stack between the main program and an interrupt routine. Because an interrupt can occur at any time, you cannot rely on the compiler's stack-usage conventions. Make no assumptions about the contents of registers when an interrupt routine runs. And be sure that the jump to the interrupt routine is an absolute jump rather than a jump relative to the current program counter.

Listing 2—More efficient C version of Listing 1's algorithm

```
/**********************************************************************/
/*   Update the autocorrelation estimates.              Rev 1.1     */
/*                                                                  */

/*   Update the autocorrelation estimates for values of             */
/*   time-shift, m given by m = (4*i + cycle), for values           */
/*   of i from 'first_i' thru 'last_i'                              */

void update_Rxx(x, first_i, last_i, cycle)
   float x;
   short first_i, last_i, cycle;
{
      static float      *first_ptr;
      register float    *in_ptr, *out_ptr, *last_ptr;
      in_ptr    = &X[first_i];
      first_ptr = &R[(4*first_i) + cycle];
      last_ptr  = &R[(4*last_i) + cycle];

      for( out_ptr = first_ptr; out_ptr <= last_ptr; )
      {
         *out_ptr = (GAMMA * *out_ptr) + ( x * *in_ptr );
         in_ptr++;
         out_ptr += 4;
      }

}
```

Improve efficiency of working routines

In the second stage, you improve the efficiency of your program by rewriting working C routines. You should apply the usual methods of improving the efficiency of a C program.

Replace array accesses by equivalent operations that use pointers. Use registers to hold frequently accessed variables. Examine the assembly-language output from the compiler. By counting the number of instructions, you can determine where the processor is spending time and thus where to direct your optimizing efforts. Studying the compiler's output will also reveal that the C compiler produces more efficient code for some high-level constructs than for other, equivalent constructs.

Pure C code can be quite efficient. However, to achieve an efficiency comparable to that of assembly language, you must move on to the third stage. In this stage, you compile the C program from the second stage and then hand-optimize the assembly language of time-critical and time-intensive routines.

One form of hand optimization is replacing a critical C-language routine with a C-callable assembly-language function or an assembly-language macro. The macro causes the compiler to insert the macro's assembler code in the program wherever it encounters the macro. Such in-line macros are faster than the equivalent C-callable assembly-language functions but require more code.

Write the initial version of the macro (or function) by optimizing the assembler output from the C compiler. In general, this optimization will consist of deleting superfluous read operations and re-ordering some of the code.

You can obtain further speed increases by exploiting the DSP µP's special instructions. DSP µPs have instructions for particular DSP operations, for example, a finite-impulse-response (FIR) filter tap. You can also speed processing by exploiting the processor's parallelism; in particular, increment pointers during the instructions that reference them.

To achieve maximum execution speed you must know when the processor inserts wait states. For example, the DSP32C can perform as many as four memory accesses during an instruction cycle. It inserts wait states during these memory accesses under two conditions: first, when accessing external memory that is not zero-wait-state memory and second, when making two successive accesses to the same physical memory.

You can easily categorize wait states arising from slow memory. Conflict wait states—wait states arising from the second condition—are more complex. You can determine the number of conflict wait states that occur while executing a section of code by using the software simulator. Using the simulator, you can investigate the effect of different memory configurations. One successful strategy for combating conflict wait states is arranging code, data, and coefficients in separate physical memories.

At the end of the third stage the resulting program will be as efficient as a well-written assembly-language implementation. The program, however, will be far more maintainable. And as a result of using this 3-stage approach, you will have learned the assembly language and characteristics of the DSP μP almost painlessly.

Listing 3—Hand-optimized version of the code produced by compiling Listing 2

```
/********************************************************************/
/*   Update the autocorrelation estimates.        Rev 2.0           */
/*                                                                  */
/*   This is an assembly language macro based on a hand optimised  */
/*   version of the compiler generated assembly language from the  */
/*   C of Rev 1.1                                                   */

/*   It updates the autocorrelation estimates for values of        */
/*   time-shift, m given by m = (4*i + cycle), for 'no_i' values    */
/*   of i from 'first_i'.                                           */

asm void update_Rxx(x, first_i, no_i, cycle, gamma)
{
% mem x; con first_i, no_i; mem cycle, gamma; lab LOOP;

      r1e = first_m
      r1e = r1 * 2
      r3e = r1 * 2   /* hold 4 * first_m in r3 */
      r4e = cycle
      r4 = *r4
      r2e = X
      r1e = r3 + r4
      r3e = r3 + r2  /* r3 = in_ptr */
      r1e = r1 * 2
      r1e = r1 * 2
      r2e = R
      r4e = r1 + r2  /* r4 = out_ptr */
      r16 = no_m
      r16e = r16 - 2 /* set up loop counter */


      r1e = gamma
      r2e = x
      r15e = 16         /* r15 is increment register = 16 */
      a0 = *r1 * *r4
LOOP: r4++r15 = a1 = a0 + *r2 * *r3++
      if ( r16-- >=0 ) goto LOOP
      a0 = *r1 * *r4     /* latent instruction ! */

% error

}
```

Programming the DSP32C in assembler

When you program the DSP32C in assembly language, three characteristics will become apparent: its RISC instruction set, the latencies arising from pipelining, and its parallelism **(Ref 5)**.

The RISC instruction set has a particularly annoying omission: The only way to transfer a number between the floating-point and fixed-point execution units is via memory. Because of the effect of latencies, the time required to execute six instructions will elapse during such a transfer.

The DSP32C has many different latency effects because of the pipelined nature of the processor. The most important of these effects are the following: when the floating-point processor writes a value to memory, the value cannot be read until four instructions later; when the integer processor loads a register from memory, the next instruction cannot reference the register (except as the address of a write by the floating-point processor); and when the processor executes a branch instruction such as "if," "call," or "goto," it also executes the subsequent instruction before the branch occurs.

To compare the efficiency of DSP code written in C with that of code written in assembler, examine these three implementations of a typical DSP algorithm. The algorithm is the Cox-Crochiere algorithm for speech-pitch estimation **(Ref 6)**.

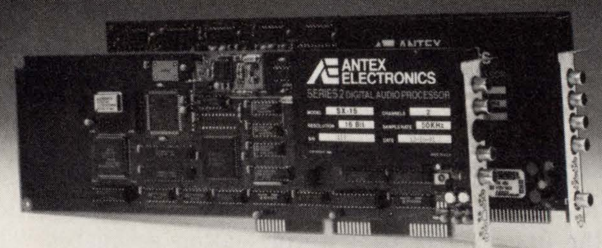
The Cox-Crochiere algorithm is an autocorrelation pitch detector structured for efficient implementation on a single DSP processor. The heart of the algorithm is the updating of 64 autocorrelation estimates. The algorithm updates each estimate every fourth sample according to the equation

$$RM_N = \Gamma \times RM_{N-4} + X_N \times X_{N-M},$$

where X_N is the Nth sample of a lowpass filtered version of the speech signal and RM_N is the autocorrelation estimate at time N and time-shift M. The autocorrelation estimates are updated in a 4-sample cycle. For example, in cycle 0 the estimates for m=28, 32, 36, . . . ,120 are updated.

Listing 1 (pg 153) is a partial listing of a straightforward C implementation of the algorithm. The code is compact and easy to understand; however, the resulting assembly language has a total of 53 instructions within the loop.

Listing 2 shows a more efficient C version. Pointer



PROGRAMMING DSP PROCESSORS

operations have replaced the equivalent array accesses. Registers hold the pointers. The resulting assembly-language code has 11 instructions within the loop.

Listing 3 is a hand-optimized version of the code produced by compiling the C code in **Listing 2.** Taking advantage of the DSP μP's special loop instruction, this version has only three instructions within the loop. EDN

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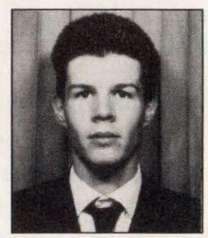
Authors' biographies



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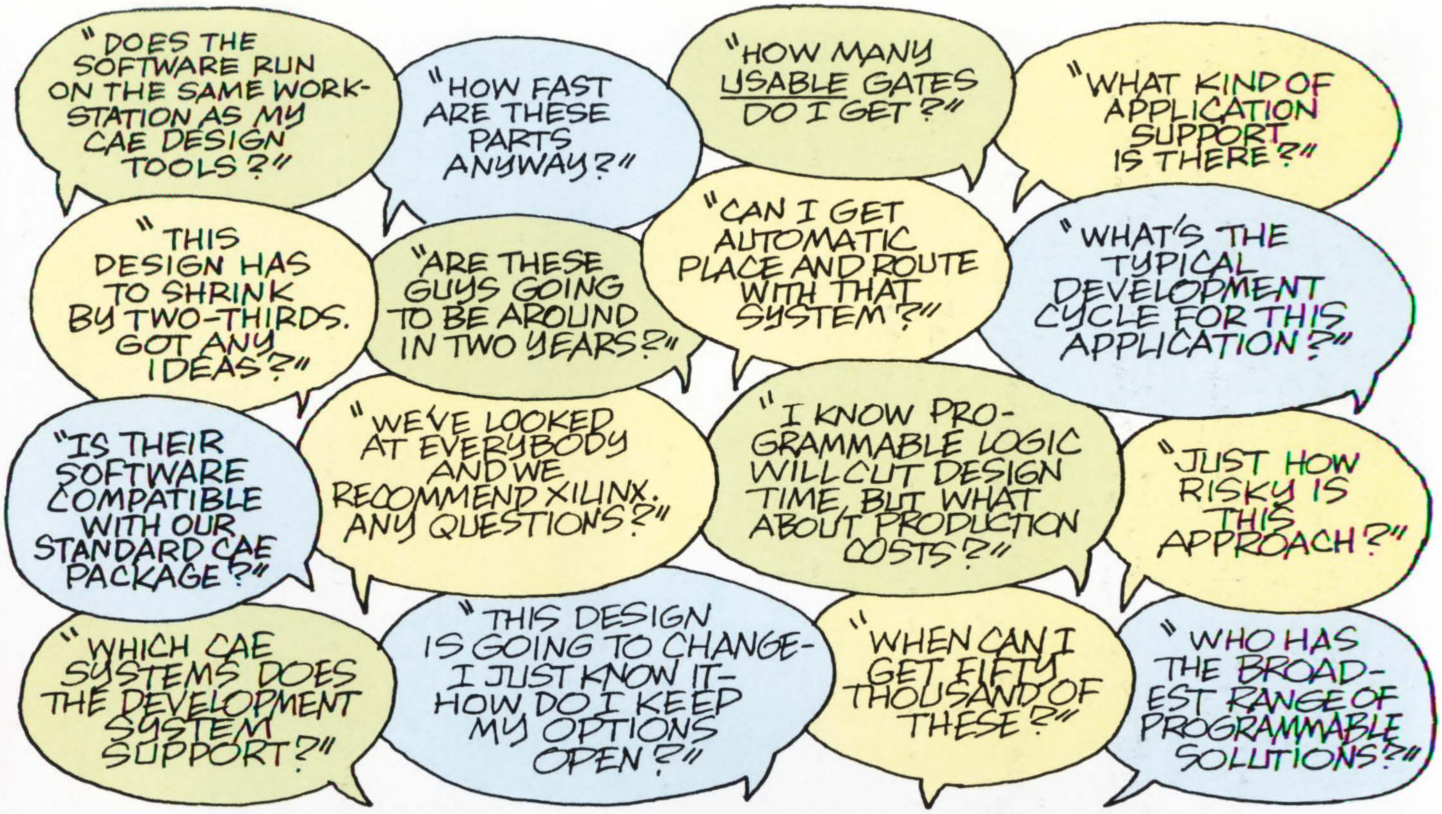

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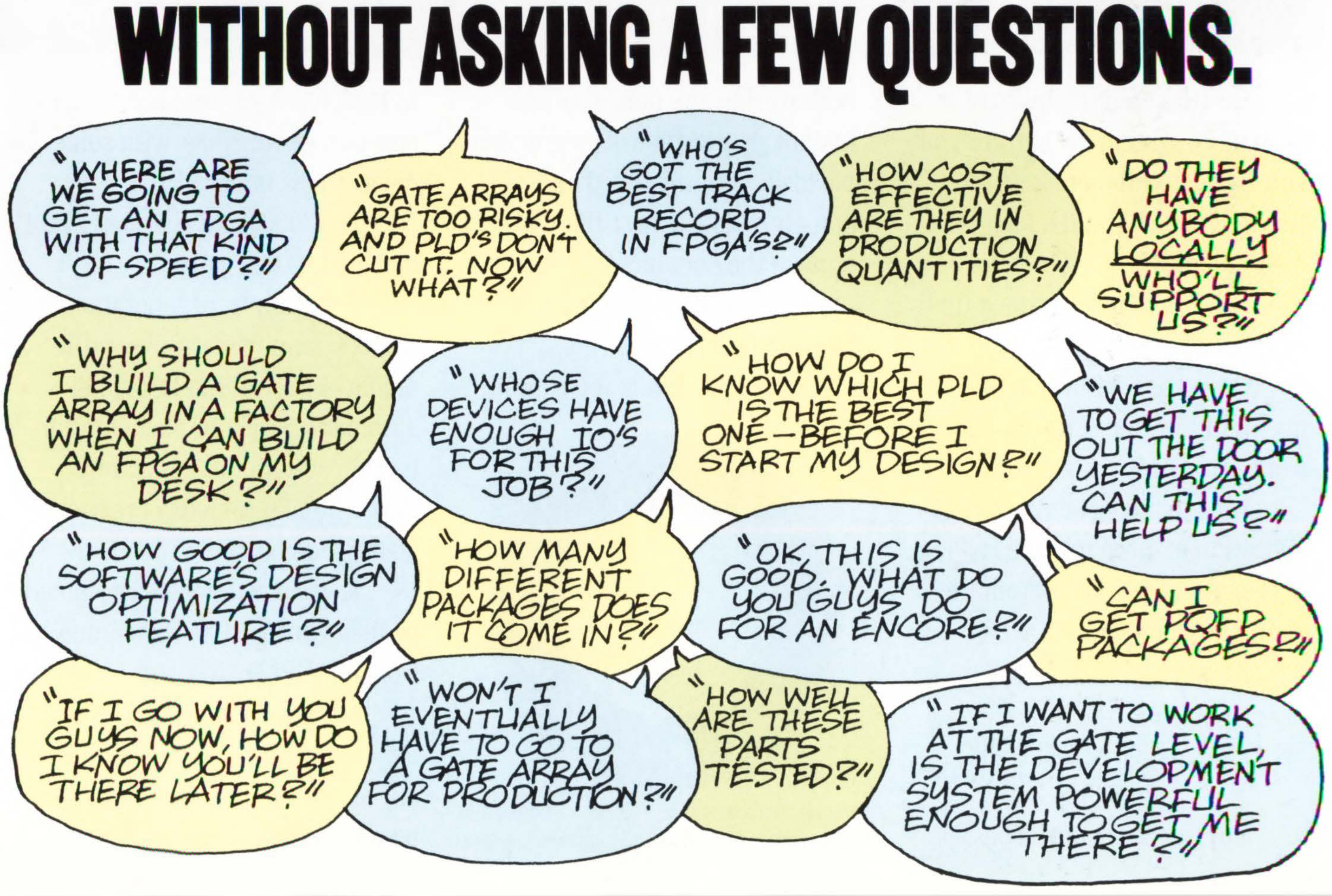

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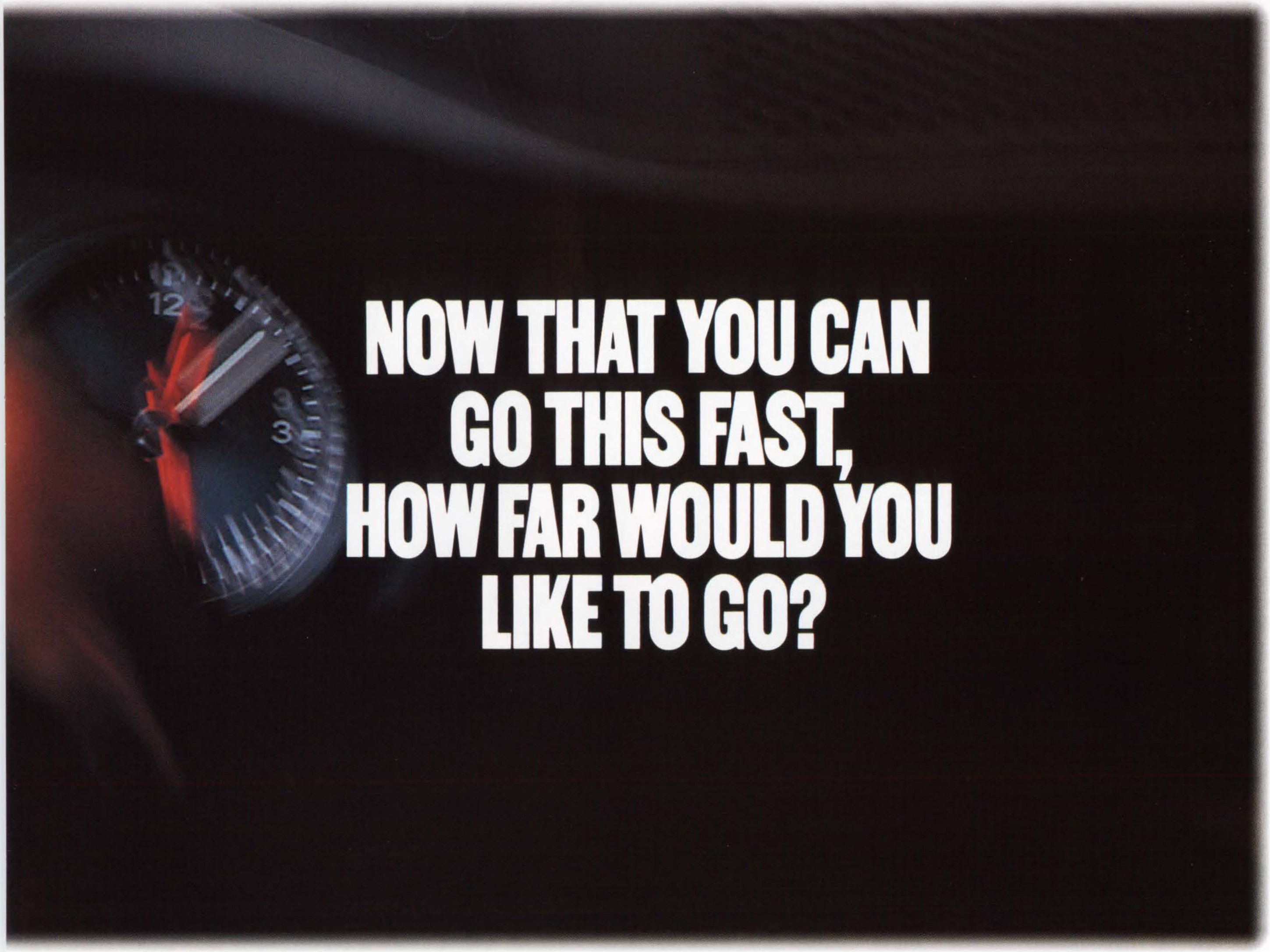

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	3000	4000	7200	3000	4000	7200
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16 bit L/U/D Counter	25	30	40	30	36	50
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24 bit Adder	16	31	17	20	29	20
16 ch, 32 bit DMA	na	20	na	na	25	na

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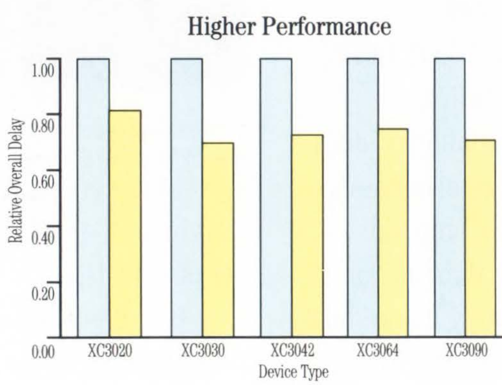

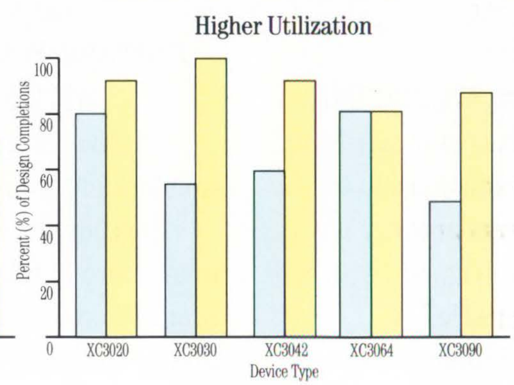

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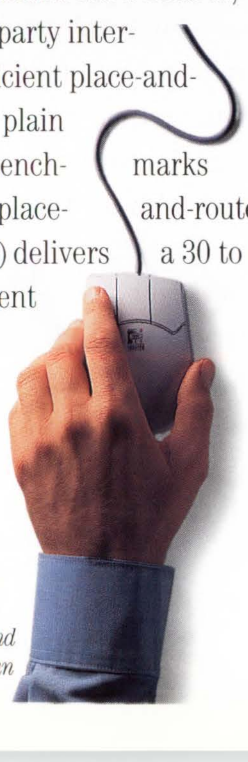

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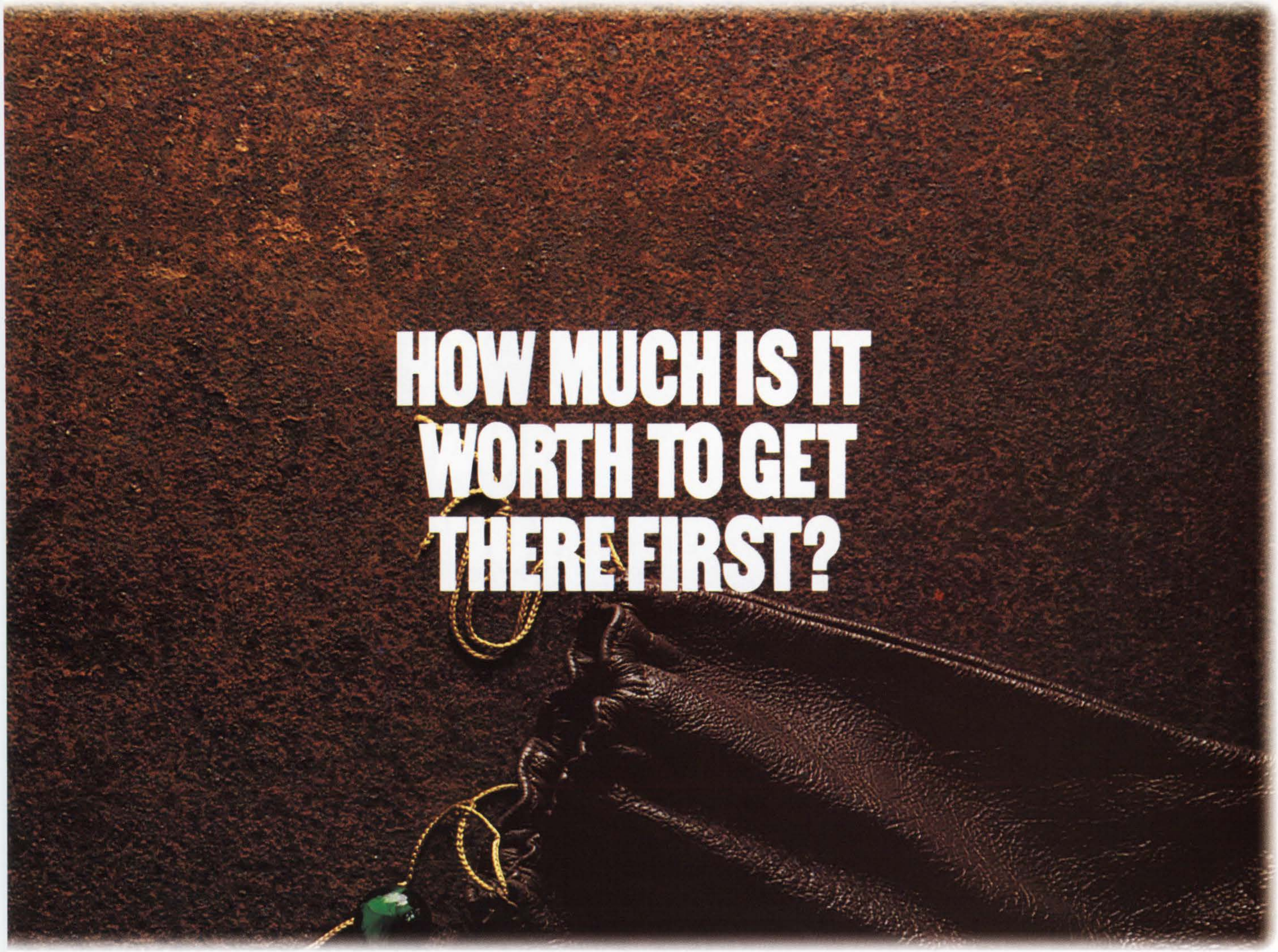

more highly integrated devices.

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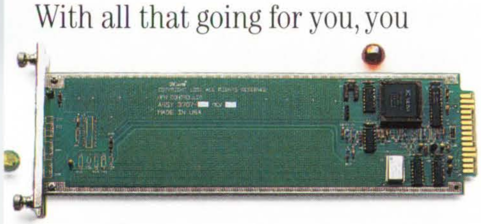

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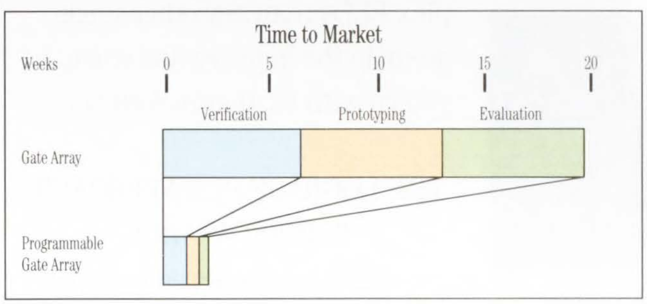

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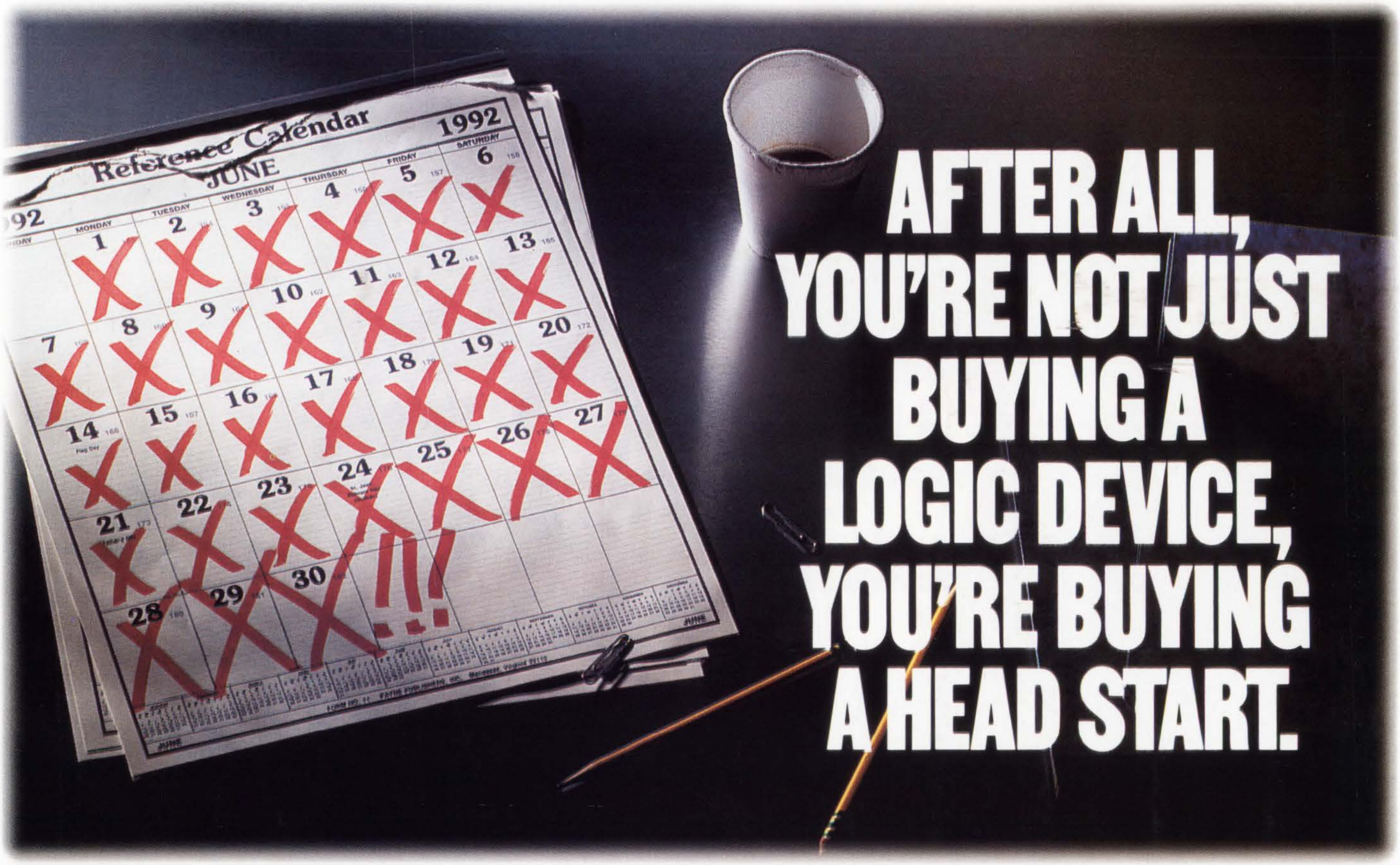

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Ada and generic FFT generate routines tailored to your needs

Fred H Carlin, Consulting Engineer

Ada's "instantiation" of generic packages—essentially generating application-specific code from templates by filling in parameters—makes customizing an FFT routine as easy as dimensioning an array.

A generic FFT (fast Fourier transform) written in Ada is easy to customize for specific applications. Ada performs the customization itself; its "instantiation" of generic "packages" produces code with properly sized arrays and with appropriate values for array limits.

Ada's "generic" mechanism eliminates rewriting and recompiling routines when requirements call for changes in array sizes. Using a generic package as a template, the Ada compiler generates new code tailored to the size you specify. If you specify multiple instantiations of a package, a good compiler will even make the different instantiations use common code to reduce overall program size.

Listings 1 through **5** are Ada routines that perform an in-place FFT; they include a sample-calling routine and a minimal complex-number package. Although the routines are in Ada, you can translate them into other languages. Because Ada code is easy to read and maintain, even programmers inexperienced in Ada should find the routines fairly easy to understand.

The software listings in this article are available on EDN's computer bulletin-board system (BBS). Phone (617) 558-4241 with modem settings 300/1200/2400,8,N,1. Access */freeware* SIG and specify *(r)ead* option followed by *(k)ey-word* search for "MS #360."

Two of the listings are program "specifications": **Listing 1** shows the complex-number package; **Listing 3** shows the generic FFT. An Ada program specification is a kind of contract that specifies what must be in the "body" of the program unit. (**Listing 2** is the body of the complex-number routine; **Listing 4** is the body of the generic FFT.) A specification states what subprograms, data types, and variables are available. By requiring designers to explicitly specify a program package's structure, a specification encourages top-down design and makes large projects easier to divide among several programmers.

The complex-number package shown is adequate just for the FFT program; it does not include operations such as root, power, magnitude, and argument of complex numbers. The package declares a "private" data type called *complex*, the details of which are hidden from programs that use the package. By hiding this information, Ada guarantees that programs don't rely on these internal details and thus are not vulnerable to changes in any future implementations of the complex-number package.

The only operations that are available to Ada private data types are assignment (:=) and tests for equality (= and /=). You can, however, define operators for addition (+), subtraction (−), multiplication (∗), and absolute value or magnitude (abs). As **Listing 1** shows, the complex-number package defines operators that accept complex numbers and return complex numbers. Thus, you can write

$$X := A + B;$$

where *A*, *B*, and *X* are all complex numbers.

The package defines two multiplier operators. The first allows scaling of a complex number, and the other multiplies two complex numbers together. The Ada compiler can always identify which "*" routine is intended because the routines' "profiles" are different; the first requires two complex numbers, the second requires a complex number on the left and a floating-point number on the right.

The rest of the specification gives the details of the complex type to the compiler. It instructs the compiler to implement the complex type as a record of two floating-point numbers, *Re* (real) and *Im* (imaginary), and to initialize this complex number to zero. Although required by the compiler, these details are in the private section of the specification and, thus, are invisible to other programs that use the complex-number package.

Listing 2, the body of the complex-number package, implements the subroutines and other details called for in the package specification. Because the body implements the specification, it can (and usually must) make use of the implementation details contained in the specification's private section.

Listing 3 shows the program specification for the *Fourier* package. This package utilizes the complex-number package, *cnum* (from **Listing 1**), and is itself a generic package. This generic package's formal parameter is the integer *N*, which specifies the size of the FFT array you want. The compiler will use the specification and body of the *Fourier* package as a template to produce a section of code tailored for this size.

Listing 1—Complex-number package

```
--***************************************************************
--*                                                             *
--*                   Complex Number Package                    *
--*                                                             *
--*                                                             *
--***************************************************************

package Cnum is

type complex is private;                          -- A new data type
function "+" (A, B: in complex) return complex;   -- Add complex
function "-" (A, B: in complex) return complex;   -- Subtract
function "*" (A, B: in complex) return complex;   -- Multiply

function cons (R, I: in float) return complex;    -- Construct
function "*"  (A: in complex;  B: in float) return complex;

function "abs" (x: in complex) return float;      -- Magnitude
procedure put  (x: in complex);                   -- To screen

private                                           --
type complex is record
   Re:         float := 0.0;
   Im:         float := 0.0;
   end record;

end Cnum;
```

The package specification for *Fourier* defines a new data type called *FFT_type*, an array of N elements indexed by an integer whose range is 0 to $N-1$. The array elements are complex numbers, as defined by the package *cnum*. Because this type definition is in the visible part of *cnum*, subprograms using the package can access the elements directly. The package also defines an exception type called *FFT_error*. This exception will be raised (or activated) when the FFT program detects an error condition.

Notice in **Listing 3** that procedure *FFT* has an

Listing 2—Complex-number procedures

```
--***************************************************************
--*                                                             *
--*                 Complex Number Procedures                   *
--*                                                             *
--*                                                             *
--***************************************************************

with math_lib; use math_lib;        -- Use floating point package
with text_io;  use text_io;         -- Use text in/out routines

package body Cnum is

function "+" (A, B: in complex) return complex is
begin
return (A.Re + B.Re, A.Im + B.Im);
end "+";

function "-" (A, B: in complex) return complex is
begin
return (A.Re - B.Re, A.Im - B.Im);
end "-";

function "*" (A, B: in complex) return complex is
begin
return (A.Re * B.Re - A.Im * B.Im, A.Im * B.Re + A.Re * B.Im);
end "*";

function "*" (A: in complex;  B: in float) return complex is
begin                          -- Multiply a complex number
return (A.Re * B, A.Im * B);   -- by a float (scale)
end "*";                       --

function cons (R, I: in float) return complex is
begin                          -- Construct a complex value
return  (R, I);                --  from two float numbers
end cons;                      --

function "abs" (x: in complex) return float is
begin                          -- Compute magnitude of complex
return sqrt (x.Re * x.Re + x.Im * x.Im);
end "abs";

procedure put (x: in complex) is
package flt_io is new float_io (float);
use flt_io;
begin                          -- Put a complex number to screen
put (X.Re, 3, 3, 0);
put (" + j");
put (X.Im, 3, 3, 0);
end put;

end Cnum;
```

Listing 3—Fourier package

```
--***************************************************************
--*                                                             *
--*                        Fourier.pkg                          *
--*                                                             *
--*                                                             *
--***************************************************************
with cnum;      use cnum;

generic
    N:              integer;                 -- Formal parameter

package Fourier is

type FFT_type is array (integer range 0..N - 1) of complex;

FFT_error:                  exception;

procedure magnitude_plot (X: in FFT_type);
procedure list_values    (X: in FFT_type);
procedure FFT (X: in out FFT_type; inverse: in Boolean := FALSE);
end Fourier;
```

FFT_type as both an input and output parameter and a *Boolean* type as an input parameter. The *Boolean* type specifies either a forward or an inverse transform; its default value is FALSE.

Listing 4, the body of the *Fourier* package, is the section of code that implements the contract contained in the specification. The body of *Fourier* contains the code for the subprograms *bit_reverse*, *max_magnitude*, *magnitude_plot*, *list_values*, and *FFT*. High-level details of all the subprograms except *bit_reverse* are in the specification of *Fourier*; thus, all the subprograms except *bit_reverse* are accessible

Listing 4—Fourier procedure

```
--*************************************************************
--*                                                           *
--*               Fourier.prc                                 *
--*                                                           *
--*                                                           *
--*************************************************************

with cnum;     use cnum;
with math_lib; use math_lib;
with text_io;  use text_io;

package body Fourier is

package flt_io is new float_io (float);
package int_io is new integer_io (integer);
use flt_io;
use int_io;

pi:  constant float   := 3.1415926535879;
L:   constant integer := integer (log (float (N)) / log (2.0));
min_angle_incr:
     constant float   := 2.0 * pi / float (N);

C:        array (0..N - 1) of float;    -- Cosine table

function bit_reverse (x: in integer; Length: in integer)
   return integer is
-- Length is number of bits to reverse
-- Performs bit reversal. Better coded in assembly
N:        integer := 2 ** (Length -1);  -- Value of high bit
XX:       integer := x;                 -- Number to convert
y:        integer := 1;                 -- Bit position value
YY:       integer := 0;                 -- Result

begin
for W in 1..Length            --
   loop
   IF XX >= N
      then
      YY := YY + y;
      XX := XX - N;
      end if;
   N := N / 2;
   y := y + y;
   end loop;
return (YY);
end bit_reverse;

function max_magnitude (X: in FFT_type) return float is
max_mag:          float := 0.0;        -- Result
mag:              float;

begin
for t in X'range                       --  Do table

   loop                                --
   mag := abs (X (t));                 -- Get magnitude
   if mag > max_mag
      then max_mag := mag;
      end if;
   end loop;
return max_mag;
end max_magnitude;


procedure magnitude_plot (X: in FFT_type) is
scale:            float;
plot_value:       integer;

begin
scale := max_magnitude (X);               -- Figure scale

for t in X'range                       --
   loop
   if scale > 0.01
      then plot_value
          := integer (56.0 * abs (X (t)) / scale);
      else plot_value := 0;
      end if;
   new_line;
   put (t, 3); put ("   "); put ("|");
   for i in 1..plot_value
      loop
      put ("=");
      end loop;
   end loop;
end magnitude_plot;

procedure list_values (X: in FFT_type) is
begin
put ("Harmonic   "); put ("Real      ");
put ("Imaginary              Magnitude");
for harmonic in X'range                --
     loop
     new_line;
     put (harmonic, 3);
     put ("(");
     put (X (harmonic));
     put (")");
     put (abs (X (harmonic)),  4, 3, 0);
     end loop;

  end list_values;

  procedure FFT (X: in out FFT_type; inverse: in Boolean := FALSE)
   is
  Q:        constant  integer := N / 4; -- Ninety degrees

  B_fly_dis:          integer;        -- Butterfly distance
  num_cells:          integer;        -- Number of cells


  upper, lower:       integer;        -- Pointer to B-flys
  r:                  integer;        -- Target & temp for
  ang:                integer;        -- Angle 2 pi / N
  W, T:               complex;        -- Complex
  scale_factor:       float;          -- Scaling factor

  begin                               -- FFT in place
  if inverse                          -- Scale inverse transform
     then                             --   by 1 / N
     scale_factor := 1.0 / float (N);
     for t in X'range
        loop
        X (t) := X (t) * scale_factor;
        end loop;
     end if;

  B_fly_dis := (N) / 2;          -- Distance between B-fly entries
  num_cells := 1;                -- Number of cells
  for pass in 1..L               -- Stage 1..L
     loop                        --
     upper := 0;                 -- Pointer to top of cell
     lower := B_fly_dis;         -- Pointer to center of cell

     for j in 1..num_cells       -- Number of cells
        loop                     --
        ang := bit_reverse (upper / B_fly_dis, L);
        if inverse               -- Construct W from cosine table
           then W := cons (C (ang),  C ((ang - Q) mod N));
           else W := cons (C (ang), -C ((ang - Q) mod N));
           end if;

        for m in upper..lower - 1     -- For each entry in cell
           loop
           T                  := W * X (m + B_fly_dis);
           X (m + B_fly_dis) := X (m) - T;
           X (m)              := X (m) + T;
           end loop;

        upper := upper + (B_fly_dis + B_fly_dis);   -- next cell
        lower := lower + (B_fly_dis + B_fly_dis);   --
        end loop;

     B_fly_dis := B_fly_dis / 2;  -- Halve distance between cells
     num_cells := 2 * num_cells;  -- Double number of cells
     end loop;

  for i in X'range                           -- Permute output
     loop                                    --
     r := bit_reverse (i, L);                -- Get target coordinates
     if r < i                                --
        then                                 --
        T     := X (i);                      -- And swap
        X (i) := X (r);                      --
        X (r) := T;                          --
        end if;                              --



     end loop;                               --

  end FFT;

  begin
  if N /= 2 ** L                        -- Must be power of 2
     then raise FFT_error;              --  entries
     end if;

  for i in C'range                      -- Construct Cosine table
     loop                               -- on startup
     C (i) := Cos (min_angle_incr * float (i));
     end loop;

  end Fourier;
```

outside the *Fourier* body. Subprogram *bit_reverse* is available only to code in the body of *Fourier* that follows the subprogram.

The end of **Listing 4** contains a small begin-end block. This unnamed block executes just once, on startup. It first checks to see that *N* is a power of two and then proceeds to build a cosine table. If *N* is not a power of two, the exception *FFT_error* is raised and program control returns to the calling program.

Putting it all together

The main calling routine is *fftest*, shown in **Listing 5**. This program creates a version of the *Fourier* package, *FT*, that generates 16-point transforms. Specific versions such as this are termed instantiations. The routine *fftest* then creates a 25% pulse wave of the complex array *X*. It then copies the array to *Y*, transforms the *Y* array, and presents a selection menu to the operator.

Listing 5—Calling procedure

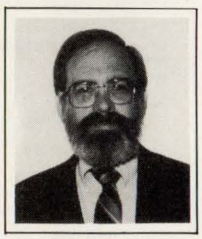
```
--***************************************************************
--*                                                             *
--*                        FFTest.prc                           *
--***************************************************************
with Fourier;
with cnum;     use cnum;
with math_lib;
with text_io;  use text_io;

procedure fftest is

package flt_io is new float_io (float);
package int_io is new integer_io (integer);

use flt_io;
use int_io;

package FT is new Fourier (N => 16);      -- N point transform
use FT;                                   --
X, Y:          FFT_type;                  --
selection:     integer;                   -- Operator selection

begin
new_line; put ("Create function     ");
for t in 0..((X'last) / 4)    -- 25 % wave
   loop
   X (t) := cons (1.0, 0.0);
   end loop;
Y := X;                                   -- Copy Input to Y
new_line; put ("FFT in progress. . .");
FFT (Y);                                  -- Do the transformation
loop
   new_line; put ("Selection ?");
   new_line; put ("  1. Magnitude plot of input");
   new_line; put ("  2. Magnitude plot of output");
   new_line; put ("  3. Table of values input");
   new_line; put ("  4. Table of values output");
   new_line; put ("  5. Copy output to input  ");
   new_line; put ("  6. Transform ");
   new_line; put ("  7. Inverse Transform ");
   new_line; put ("  0. Exit                 ");
   skip_line;
   get (selection);
   case selection is
      when 1 => magnitude_plot (X);
      when 2 => magnitude_plot (Y);
      when 3 => list_values (X);
      when 4 => list_values (Y);
      when 5 => X := Y;
      when 6 =>
         new_line; put ("FFT in progress. . .");
         Y := X;                        -- Copy Input to Y
         FFT (Y);                       -- Do the transformation
      when 7 =>



         new_line; put ("FFT in progress. . .");
         Y := X;          -- Copy Input to Y
         FFT (Y, TRUE);  -- Do the inverse transformation
      when 0 => exit;
      when others => null;
      end case;
   end loop;
end fftest;
```

The "elaboration" of *FT* is Ada terminology for the compiler's process of allocating data areas for *FT*, *X*, and *Y*. If the exception *FFT_error* occurs during elaboration, then program control returns to the program that called *fftest*, and this calling program has the option of intercepting the exception and executing some error-recovery code. In our example, however, the operating system called *fftest*, so the operating system will report an error.

An Ada implementation of the FFT makes it easy to create a working prototype. In addition, Ada's package structure provides for systematic program maintenance, so it is easy to upgrade program performance in an orderly way. For example, if you program a more efficient bit-reversal algorithm or get a special piece of hardware to provide this function, then you need only replace the subroutine in the body of *Fourier* (**Listing 4**) and recompile only the *Fourier* body. Similarly, if you program a more efficient transform (**Listing 4** is mostly a demonstration version), then all you need to do is replace the subroutine *FFT* in the body of *Fourier*, recompile the body, and relink the program.

If, however, you should decide that complex numbers are better represented in polar format (because, for example, you have a new piece of hardware), then you will need to change both the specification and the body of *cnum*, the complex-number package. And, because you will need to recompile *cnum*'s specification, you must also recompile everything that depends upon the specification—including *Fourier*'s specification (and therefore its body, too) and *fftest*. However, as long as the visible (nonprivate) part of *cnum*'s specification remains unchanged and the body of *cnum* properly implements the specification's functions and procedures, then neither *Fourier* nor *fftest* need be changed. EDN

Author's biography



Fred H Carlin, a consulting engineer in Goleta, CA, designs hardware and software for real-time data-acquisition and -processing systems. He has developed systems for medical diagnostics, environmental monitoring, and industrial control. Fred holds PhD and MS degrees from the University of California (Santa Barbara), an MBA from California State University (Fullerton), and a BS from California State Polytechnic (Pomona). He is a member of the IEEE and the Association for Computing Machinery. In his spare time, Fred enjoys sailing and navigating.

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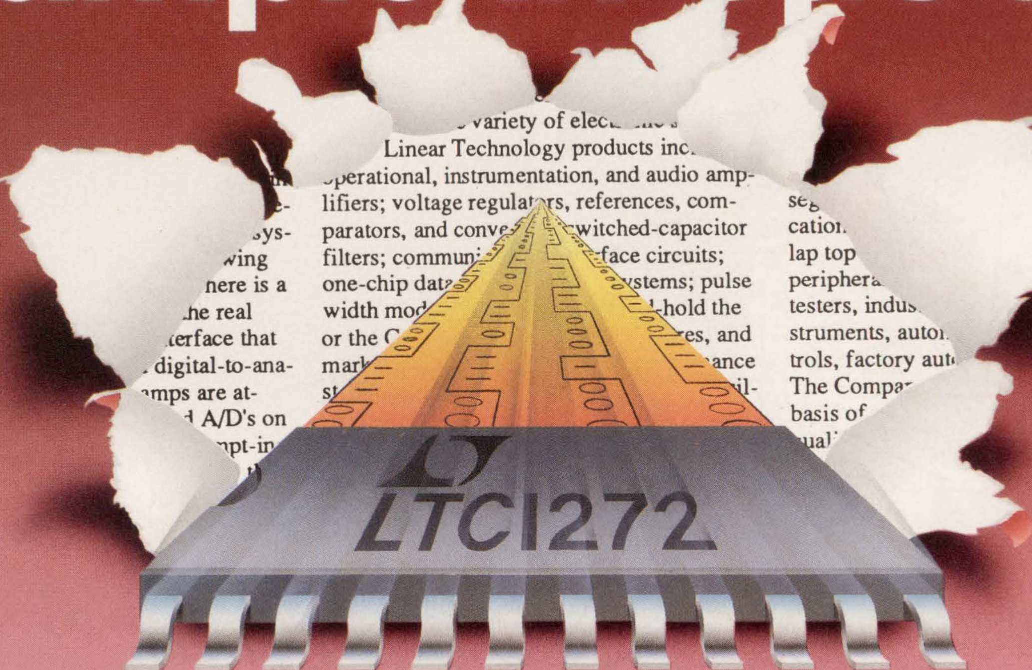

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Paralleled amplifiers drive loads quietly

Moshe Gerstenhaber and Mark Murphy,
Analog Devices Semiconductor, Wilmington, MA

By paralleling amplifiers, you can increase load drive while keeping output impedance low, reducing noise voltage. **Fig 1a** shows the classic stacked-amplifier circuit. This configuration halves noise and quadruples load drive. However, this approach has some obvious weaknesses:

- You need to set the correct gain for every amplifier and add ballast resistors to each output.
- The input range is limited because of the inherent offset of any of the amplifiers.
- The output impedance must be high to prevent any of the amplifiers from short circuiting.

The circuit in **Fig 1b** has half the noise voltage of an individual amplifier, quadruples the load drive, reduces the component count from twelve resistors to three, and has a gain-bandwidth product of 1 GHz. Although the topology in **Fig 1b** is generally applicable to all externally compensated amplifiers, **Fig 1b**'s particular components suit video applications.

The circuit increases drive by paralleling outputs. To understand how the circuit reduces noise, let the voltage noise, referred to the input, of the individual amplifiers be V_{N1}, V_{N2}, V_{N3}, and V_{N4}, and the total noise voltage be V_N. Because the circuit connects all inputs—inverting to inverting and noninverting to noninverting—and high-impedance nodes (pin 5s),

$$(V_N - V_{N1})g_M + (V_N - V_{N2})g_M + (V_N - V_{N3})g_M + (V_N - V_{N4})g_M = 0$$

$$\text{or, } V_N = \tfrac{1}{4}(V_{N1} + V_{N2} + V_{N3} + V_{N4}).$$

But because the noise voltage of the amplifiers is not correlated, and the noise-voltage spectral density for each amplifier is the same,

$$V_N = \tfrac{1}{4}\sqrt{(4V_{N1})^2}$$

$$\text{or, } V_N = V_{N1}/2.$$

This result also implies that all noncorrelated parameters such as input-offset voltage, input-offset voltage drift, CMRR, and PSRR, will also approach their true mean values, thus reducing effects arising from the variability of the devices.

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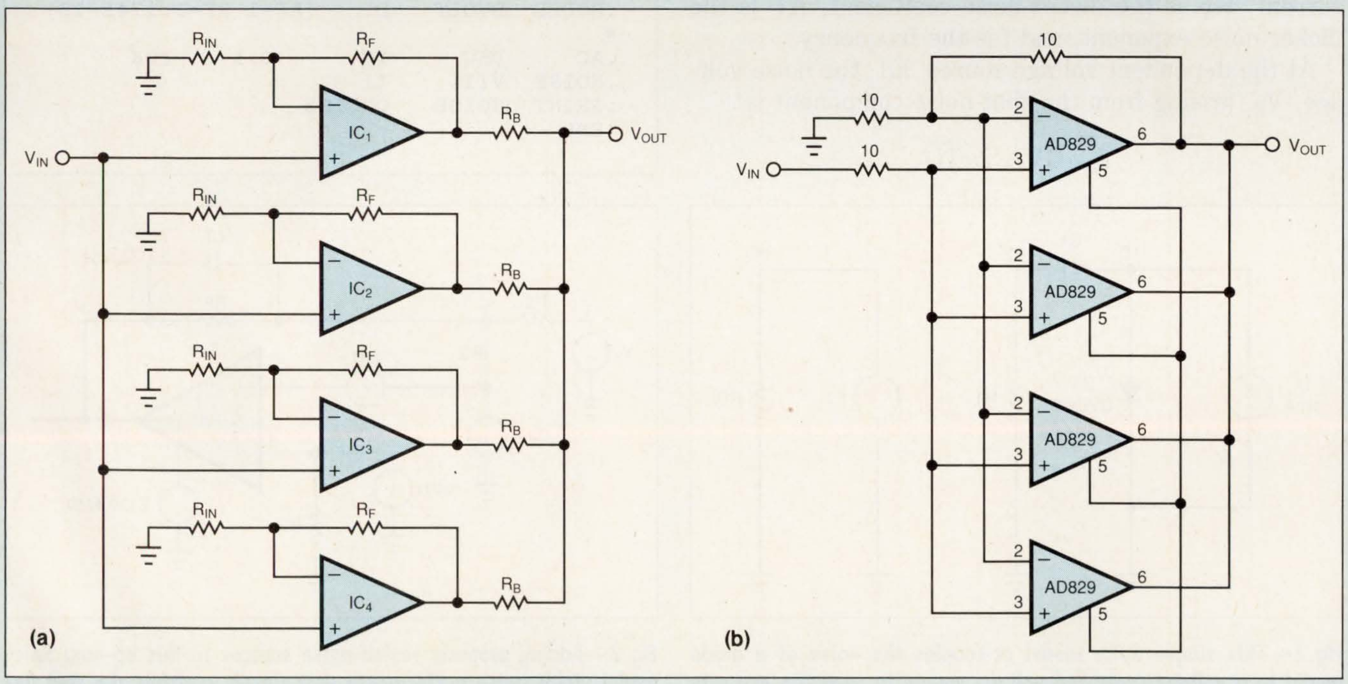

Fig 1—Paralleling amplifiers (b) increases total output drive and reduces output noise, surpassing the stacked approach (a).

Op-amp model includes 1/f noise

Richard Faehnrich, Bio-Imaging Research Inc, Lincolnshire, IL

Extracting the shot and flicker noise of a Spice diode model is an easy way to model 1/f noise. This method is superior to the usual trick of using the Johnson noise of a resistor inserted into a circuit via a dependent voltage or current source. The problem with the usual trick is that Johnson noise density is flat over frequency. Not including the 1/f noise can result in serious underestimates of the total noise that an amplifier will produce.

Fig 1 shows a 1-mA current source biasing a diode. C1 ac-couples the diode's noise to R1 so that the diode's dc voltage has no effect on the op-amp model. The resistor has a large value so that its inherent noise will not be significant. A voltage-controlled source, E1, having gain G, then injects the noise into the appropriate location in the amplifier circuit. **Listing 1** is a Spice model of this circuit.

The diode's model parameters are: IS = 1E-14, N = 1, RS = 0, AREA = 1, T = 300K, Vt = k*T/q = 0.0261. This diode model generates shot- and flicker-noise currents according to

$$i_N = 2q\ ID + KF\frac{ID^{AF}}{f},$$

where q is the electron charge, ID is the diode's bias current, KF is the flicker-noise coefficient, AF is the flicker-noise exponent, and f is the frequency.

At the dependent voltage source, E1, the noise voltage, V_O, arising from the shot-noise component is

$$V_O = GV_t\sqrt{2q/ID}.$$

Solving for G, controlled-source gain, yields

$$G = \frac{V_O}{V_t}\sqrt{\frac{ID}{2q}} = (2.149\times10^9)\ V_O\ .$$

Setting the flicker exponent, AF = 1, the noise voltage arising from the flicker component is

$$V_O = GV_t\ \sqrt{KF/IDf}\ .$$

Solving for KF yields

$$KF = \frac{V_O^2\ IDf}{V_t^2\ G^2} = (1.467)\frac{V_O^2\ f}{G^2}\ .$$

Listing 1—Noise-source Spice model

```
OPN.CIR - NOISE MODEL WITH 1/F NOISE
*
E1      1 0     11 0    43.0
RD      1       0       1E12
* INPUT NOISE VOLTAGE
I1      0       10      DC      0.001
D1      10      0       DVOLT
C1      10      11      100UF
R1      11      0       1E12
*
* DIODE MODEL
.MODEL  DVOLT   D       (AF=1 KF=3.174E-18)
*
.AC     DEC     10      0.1     10K
.NOISE  V(1)    I1
.PRINT  NOISE   ONOISE
.END
```

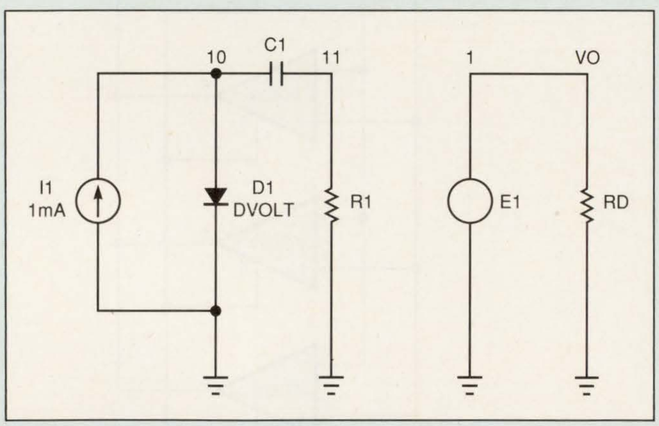

Fig 1—This simple Spice model ac-couples the noise of a diode model to a voltage-controlled voltage source to generate accurate noise voltages.

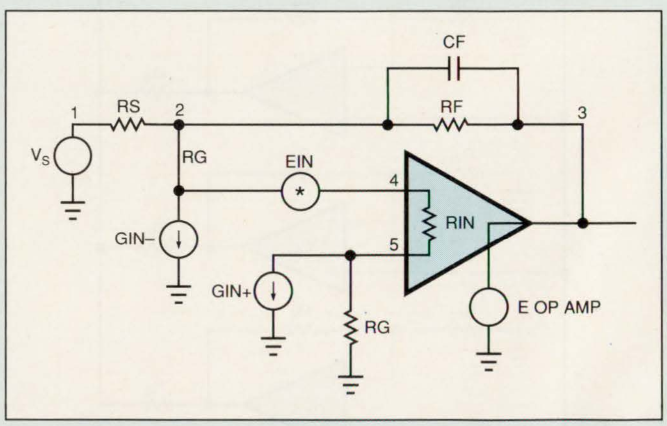

Fig 2—Adding properly scaled noise sources to this op-amp Spice model yields noise performance that closely matches the real device's data-book values.

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Listing 2 is a Spice model of the OP-02 amplifier circuit in **Fig 2**, which incorporates the noise source of **Fig 1** and **Listing 1**. Choosing 20 $nV/\sqrt{12\ Hz}$ at 1 kHz for an input-noise voltage value (which is far above the $1/f$ corner frequency where the noise density is flat over frequency), G is

$$G=(2.149\times10^{9})\ (20\times10^{-9})=43.0\ .$$

Next, for frequencies below the circuit's $1/f$ corner frequency (where the $1/f$ noise is much greater than the shot noise), choosing a value of 200 $nV/\sqrt{12\ Hz}$ at 0.1 Hz yields a flicker-noise coefficient, KF, of

$$KF=1.467\frac{(200\times10^{-9})\ (0.1)}{(43.0)^2}=3.174\times10^{-18}\ .$$

The results of a Spice simulation of **Fig 2**'s model, using the values above for the noise sources, closely match the noise data given in the OOP-2's manual, validating the choices of noise-voltage values.

If you need noise currents for your application, simply substitute voltage-controlled current sources for the voltage-controlled voltage sources. You can get a copy of **Listing 1** and **Listing 2**, as well as test data, from the EDN BBS. **EDN BBS /DI_SIG #1121** EDN

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Listing 2—Amplifier Spice model with noise sources

```
OPNOISE.CIR - OPAMP NOISE MODEL WITH 1/F NOISE
*
* CIRCUIT COMPONENTS
VS      1       0       AC      1
RS      1       2       1K
RF      2       3       10K
CF      2       3       10PF
RG      5       0       1K
*
* OPAMP MODEL
EIN     2 4     11 0    43.0
GIN-    2 0      21 0    0.859E-3
GIN+    5 0     31 0    0.859E-3
RIN     4       5       100MEG
EGAIN   3 0      5 4    100K
*
* INPUT NOISE VOLTAGE
I1      0       10      DC      0.001
D1      10      0       DVOLT
C1      10      11      100UF
R1      11      0       1E12
*
* - INPUT NOISE CURRENT
I2      0       20      DC      0.001
D2      20      0       DCURR
C2      20      21      100UF
R2      21      0       1E12
*
* + INPUT NOISE VOLTAGE
I3      0       30      DC      0.001
D3      30      0       DCURR
C3      30      31      100UF
R3      31      0       1E12
*
* DIODE MODELS
.MODEL  DVOLT   D     (AF=1 KF=3.174E-18)
.MODEL  DCURR   D     (AF=1 KF=4.467E-17)
*
.AC     DEC     10      0.1     10K
.NOISE  V(3)    VS
.PRINT  NOISE   INOISE  ONOISE
.END
```

Amplifier neutralizes ground leakage

Leonard Schupak, Navitech Consulting, Irvine, CA

For critical applications such as medical apparatus connected to patients, the circuit in **Fig 1** will neutralize, or absorb, several milliamperes of leakage current over a frequency range of 10 Hz to 200 kHz. The circuit will work with single-phase or 3-phase power systems, with or without a neutral connection (ground-leakage current flows through the *protective* ground, not the neutral). This circuit can bring your designs into compliance with UL-544 or other stringent safety regulations.

The capacitors C_{L1} and C_{L2} in **Fig 1** represent paths for ground-leakage current, I_L. Typically, various elements, such as insulated heat sinks, capacitively couple ground-leakage currents to the chassis ground.

The active circuitry begins with a ground-leakage current-sense transformer, T_1, having either one or two single-turn primaries, which is ac-coupled to an op amp, IC_1. IC_2, a precision bilateral constant-current source, converts IC_1's output to a current equal and opposite to the ground-leakage current. The circuit sums this opposing current into the protective ground, canceling the leakage current.

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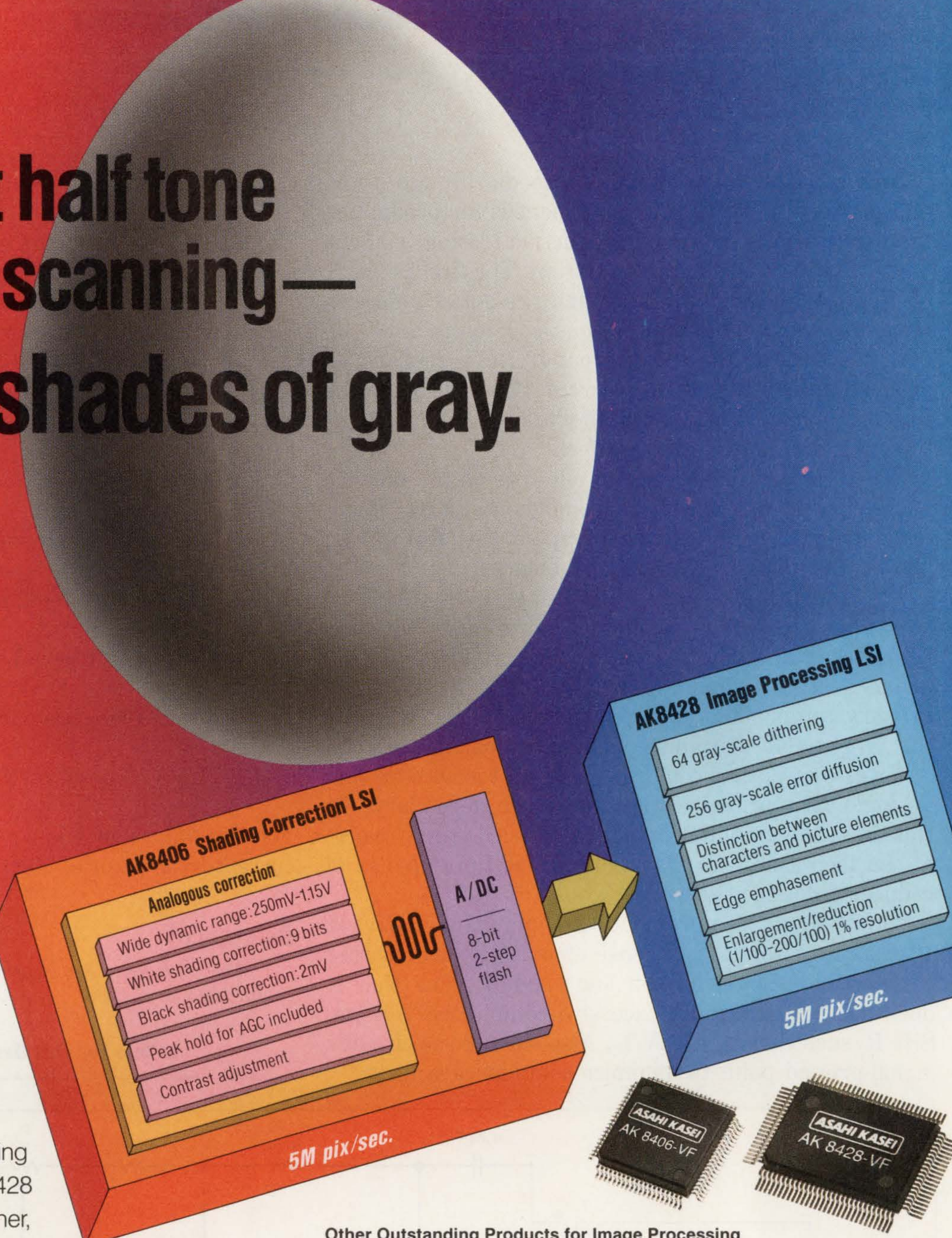

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CIRCLE NO. 90

In **Fig 1**, the opposing current feeds through a second primary of T_1. This arrangement is for production testing. If you do not need production testing, you can omit this second-primary connection. The first primary of T_1 must be low impedance and the sole connection between your equipment's chassis ground and the power system's protective ground. Be sure that all your equipment's leakage current flows through the first primary. Also, wrap the transformer's turns tightly to minimize leakage effects.

The accuracy of cancellation depends on the balance of the current source's bridge components. Error manifests itself as a finite output impedance **(Ref 1)**. R_1 allows you to adjust the bridge's balance.

The transformer in **Fig 1** is a 10:1 step-up unit. This step-up ratio is an excellent compromise between transformer and amplifier requirements. The input impedance at the summing junction, and its reflected primary component, yield reasonable values, whereas the large-value secondary minimizes leakage effects. A lower-cost circuit could use a small toroid core and a single-turn primary and single-turn secondary. In this case, the amplifier can have reduced gain because of the increased secondary current at the expense of reduced frequency response.

Power-supply requirements are minimal: ±10V at 10 mA. Resistor R_2 is a sense element for monitoring current and should have a low enough value that it does not necessitate an excessive compliance voltage. Size R_2 such that $R_2=0.5V/I_L$. Also, choose the circuit's signal-ground point to minimize compliance voltage.

Starting with the following definitions:

I_L = system leakage current
I_O = circuit output current
I_G = ground current
I_2 = transformer secondary current
N_1 = number of turns on transformer primary
N_2 = number of turns on transformer secondary
$N=N_2/N_1$ = transformer-turns ratio,

IC_1's output is

$$V_1=I_2\times R_1=(I_L+I_O)\times R_1/N.$$

I_O for this precision feedback amplifier circuit is

$$I_O=-(V_1/R_O)\times(R_3/R_2)\approx -I_L\times(1-(N\times R_O\times R_2)/(R_1\times R_3)).$$

I_G, the ground-leakage current, is

$$I_G=I_L+I_O\approx I_L\times(N\times R_O\times R_2)/(R_1\times R_3).$$

For the values in **Fig 1**, the circuit reduces leakage current by a factor of 1000. **EDN BBS /DI_SIG #1117**

EDN

Reference

1. *AN-29, Linear Applications Handbook,* National Semiconductor Corp, 1986.

To Vote For This Design, Circle No. 741

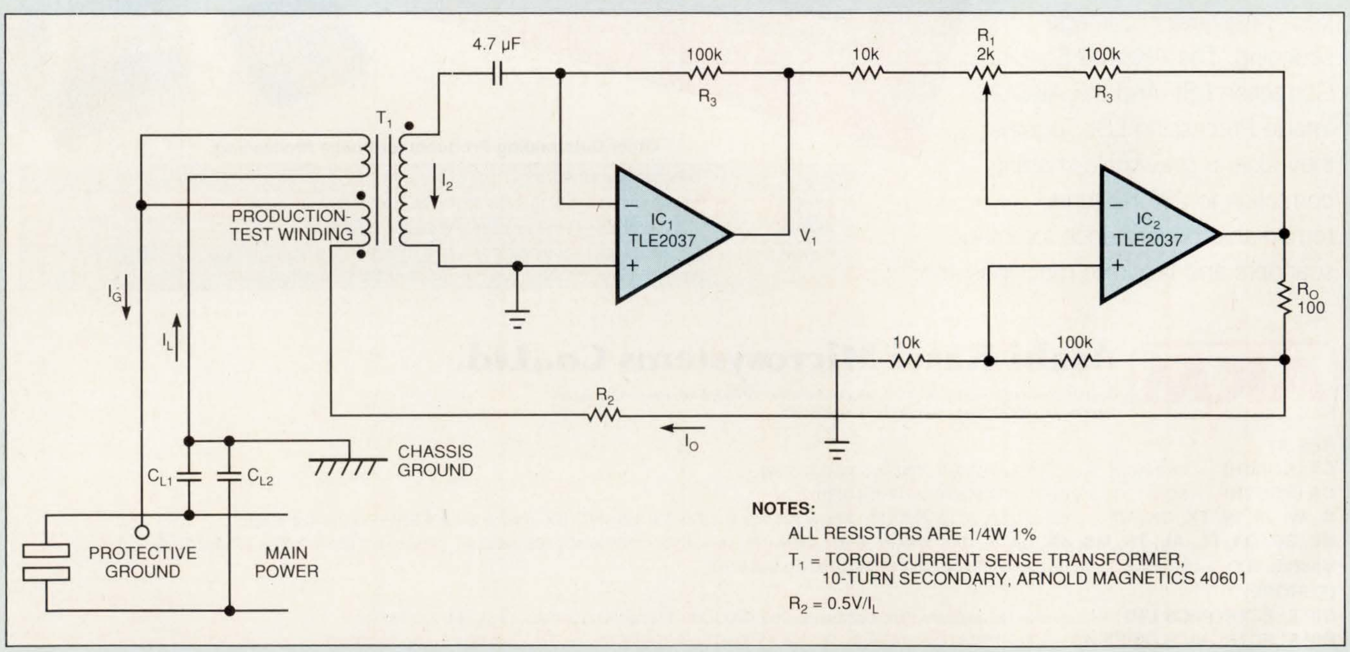

Fig 1—This amplifier circuit senses ground-leakage current, develops an equal and opposite current, and injects the opposing current into the protective ground, thereby neutralizing potentially life-threatening leakage.

Shaft encoder powers tachometer

Larry Rinehart, IXYS Corp, San Jose, CA

Unlike optical shaft encoders that keep an internal count of pulses from a rotary pulse generator, IC_1 in **Fig 1** outputs a delta value to be stored in an external counter upon command. Sampling this delta value at a known rate, instead of simply using it to count up or down, yields a tachometer.

IC_{2A} generates the sampling pulse for IC_1. Because IC_1's internal clock is asynchronous to the sample clock, IC_1's chip-select pin $\overline{CS}$, pin 1, must be active low for at least one clock period (the maximum latency), plus the chip access time, plus the data-setup time of the D/A converter, IC_3. For the components shown, $\overline{CS}$ must be low for at least 700 nsec.

IC_1 outputs a 2's-complement binary output that represents 8-bit, bipolar numbers. Unfortunately, to achieve a bipolar output, the D/A converter needs complementary-offset binary numbers. (The D/A converter also needs an output op amp to achieve bipolar outputs.)

Comparing the shaft encoder's output with the codes that the D/A converter requires reveals that adding 80_{HEX} to the encoder's output will make the devices compatible. Inverter IC_{4A} complements the most significant bit of the encoder's output, performing the conversion simply.

Achieving a ±2.5V analog-output range requires offsetting the D/A converter's output. Tying the converter's pins 14 and 16 to the output, pin 15, sets the converter's output range at 0 to 2.56V. The 1.25V reference provides an offset of half this range. R_1 centers the output. The LT1097 can swing to within 2V of either supply rail, allowing operation from ±5V at full accuracy. If you require a traditional ±10V output, you must operate the circuit from ±12V supplies and change R_2 from 10.0 kΩ, 1% to 39.2 kΩ, 1%.

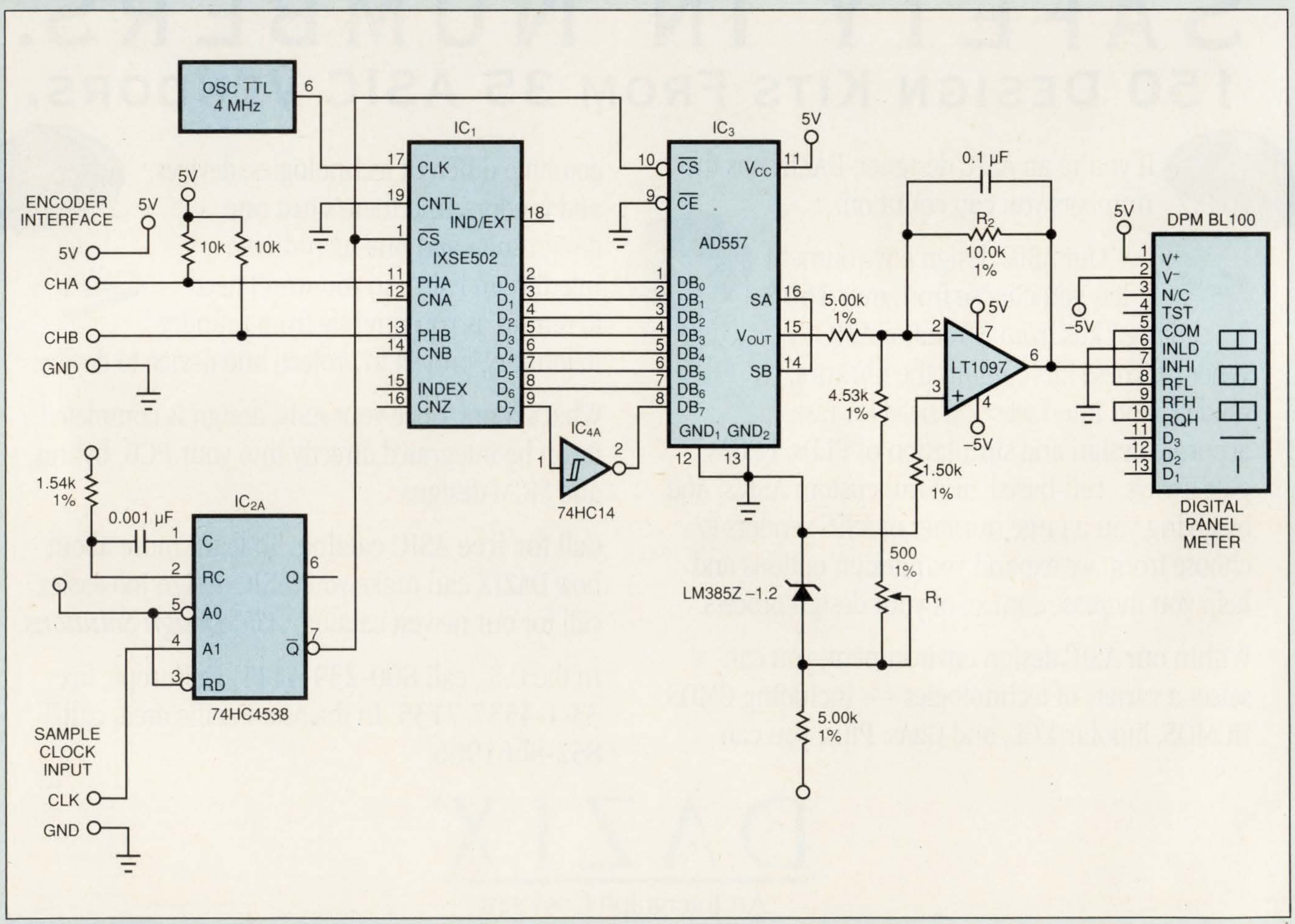

Fig 1—This simple circuit turns a shaft encoder into a tachometer and requires no controlling µP.

The function relating the circuit's output voltage to shaft speed is

$$V/rpm = 4(V_{FS} \times \text{encoder output})/(f_{SAMPLE} \times \text{encoder count depth}).$$

IC_1's count depth is 127. The sample frequency, f_{SAMPLE}, must be high enough so that IC_1 does not accumulate more than 127 counts between sampling. For the components shown, a shaft rotating at $\omega = 60$ rpm and a sample frequency, f_{SAMPLE}, of 1344 Hz produce an output voltage of 0.06V. The 3½-digit panel meter shown displays 1/1000 V/rpm, or, in this case, 60 (note that the decimal point is turned off).

EDN BBS /DI_SIG #1119

To Vote For This Design, Circle No. 742

Answering machine signals "beeper"

Dan Goldish, Raytheon Co, Marlboro, MA

The circuit in **Fig 1** will signal your pocket pager ("beeper") whenever your answering machine records a call. The circuit is less expensive than combination voice-mail/beeper services. The circuit connects in parallel with your answering machine's telephone line. After the answering machine finishes recording an incoming call, the circuit waits for a dial tone and proceeds to call your paging company. Your beeper will then beep or vibrate, displaying the telephone number of your answering machine.

The **listing** for the 8051's program, too long to print here, is available on the EDN BBS. The program initializes the Xecom XE2401 ultra-compact component data modem upon power-up. When the modem chip detects an incoming call, it increments an internal ring counter. You could use any Hayes-compatible modem by connecting the 8051's serial pins to the modem via level translators. The 8051, which knows how many rings will occur before the answering machine answers the call, interrogates the modem chip to determine if a person or the answering machine took the call.

EDN BBS /DI_SIG #1120

To Vote For This Design, Circle No. 743

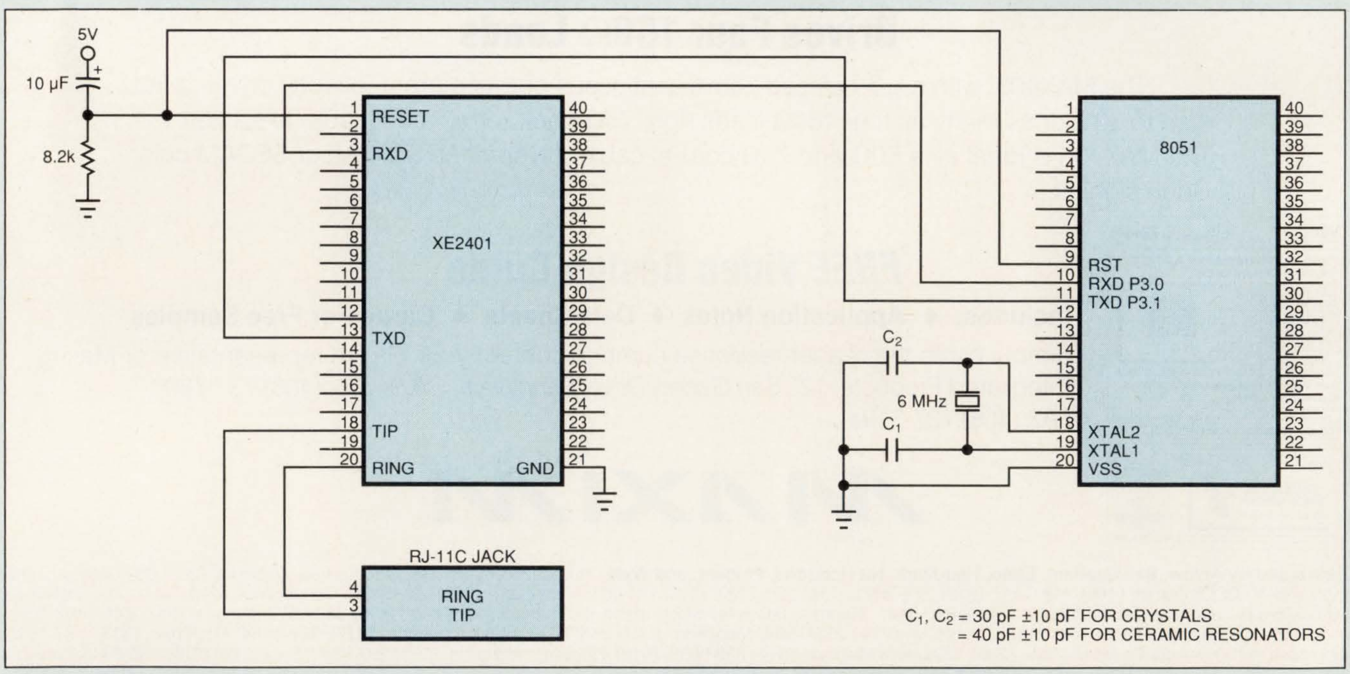

Fig 1—This simple 2-chip circuit will monitor a phone line to determine if a person or an answering machine takes a call. If the answering machine takes the call, the circuit will call the user's pager service after the answering machine finishes recording the call.

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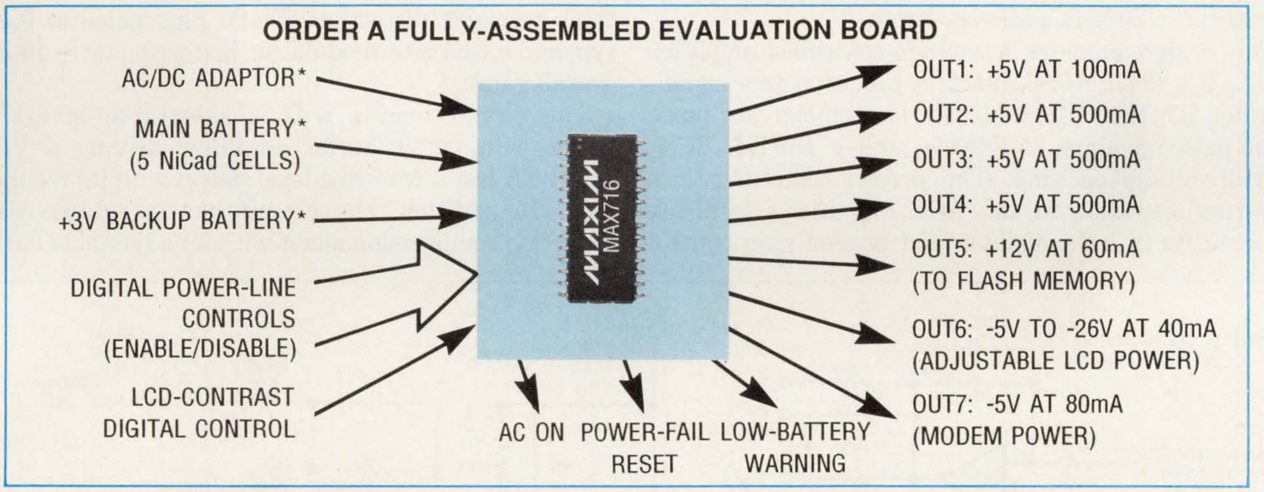

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* Not included with the Evaluation Board

CIRCLE NO. 93

AGC amp uses true-rms feedback

Richard Majestic, Voice of America, Annapolis, MD

The automatic-gain-control (AGC) amplifier in **Fig 1** features adjustable AGC time constants for both attack and release. The circuit's signal-to-noise ratio is 90 dB min, and the circuit operates transparently throughout the 20-Hz to 20-kHz audio spectrum.

The design employs a voltage-controlled-amplifier (VCA) IC, the PMI/SSM2122; a precision rms signal-rectifier IC, the PMI/SSM2110; two bipolar low-noise audio-path op amps, NE5534s; and a BiFET VCA-control-voltage op amp. The precision-rectifier IC's true-rms operation in the AGC amplifier's feedback loop results in a dependable and precise gain control that retains a semblance of the signal's dynamics while leveling the input signal over time.

The VCA is a high-performance device that has a dynamic range of 94 dB min typ over the audio range, total harmonic distortion (THD) plus noise of 0.01% typ, and 0.03% intermodulation distortion (at −10-dBu overall gain).

The circuit begins with a selectable inverting/noninverting input-buffer amplifier driving a VCA. The VCA has a true-rms level detector in its feedback loop. In addition, the circuit has selectable gain-reduction compression along with an adjustable output

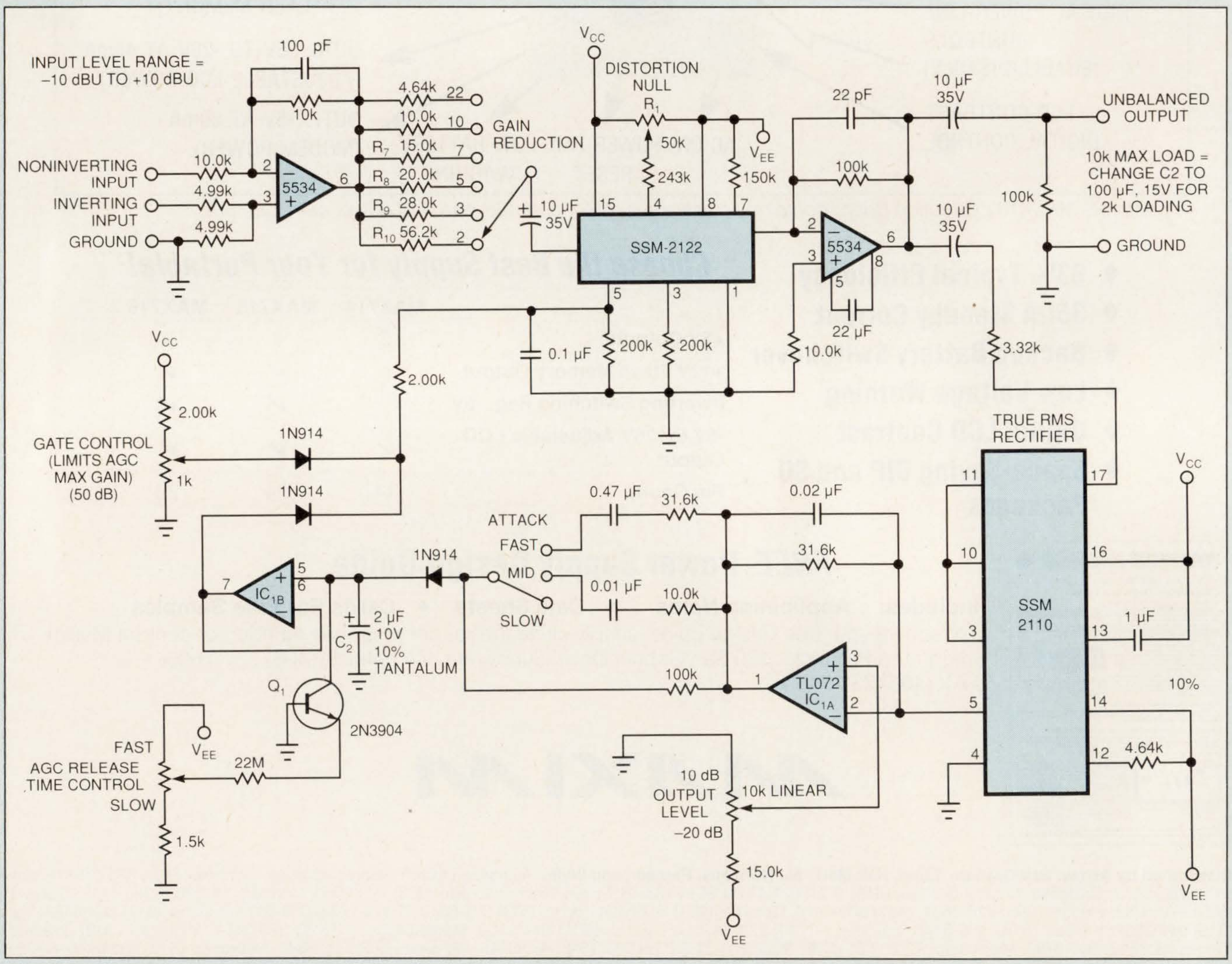

Fig 1—This automatic-gain-control amplifier features adjustable time constants for both attack and release, has a signal-to-noise ratio of 90 dB min, and operates transparently throughout the 20-Hz to 20-kHz audio spectrum.

level and a control for maximum gain limiting (also known as "gating"). If the input signal disappears, the maximum-gain limiting quashes the input's noise-floor rise as the circuit waits for an input signal to regulate.

The 6-position gain-reduction selector provides adjustable signal compression that helps steady the AGC amplifier's action. The selector blocks the irritating hole produced by transient signals impressed on the wanted signal and flattens the "pumping" characteristic of AGC amplifiers.

Op amp IC_{1A} and C_1 integrate the detected level while the remaining amplifier functions as the VCA's control-voltage buffer. Comparing the integrator's signal voltage to a reference voltage set by the output-level potentiometer determines the circuit's instantaneous output level.

Changing C_2's (the final integrator's) charging-time constant or charging current's waveform adjusts the gain-reduction attack and compression response. The adjustment range spans 20 to 200 msec. The constant-current discharge of C_2 controls the gain-correction release rate. Changing Q_1's emitter current adjusts C_2's discharge linearly via the AGC release-rate control. The adjustment range is 3 to 32 sec for recovery from a 6-dB gain-reduction event.

You trim the VCA's THD by adjusting the distortion-null control, R_1, for a minimum value while applying a −10 dBu, 1-kHz signal to the input and setting the circuit's output to 0 dBu.

EDN BBS /DI_SIG #1068 EDN

To Vote For This Design, Circle No. 744

Circuit amplifies without amplifiers

Miss Jhoti Vandana, SMC, Madras, Tamil Nadu, India

The circuit in **Fig 1** amplifies a dc signal using switches and charge-storage capacitors. The circuit has a fixed gain of 8 and averages the input signal over eight timing periods.

In operation, a 400-Hz sampling clock drives divider IC_3, a 74HC393. The divider's output selects a particular capacitor for charging from the input via analog switches IC_1 and IC_2. IC_1 couples the input sequentially to each flying capacitor while IC_2 provides a corresponding current-return path.

Both analog-switch ICs become inactive if their pin-6 (INH) inputs are low. In this case, the voltage across the eight series capacitors is eight times the average input voltage. If the switches are active, you can pick off the output voltage with a differential-input probe or amplifier. The clock frequency is not critical.

EDN BBS /DI_SIG #1071 EDN

To Vote For This Design, Circle No. 745

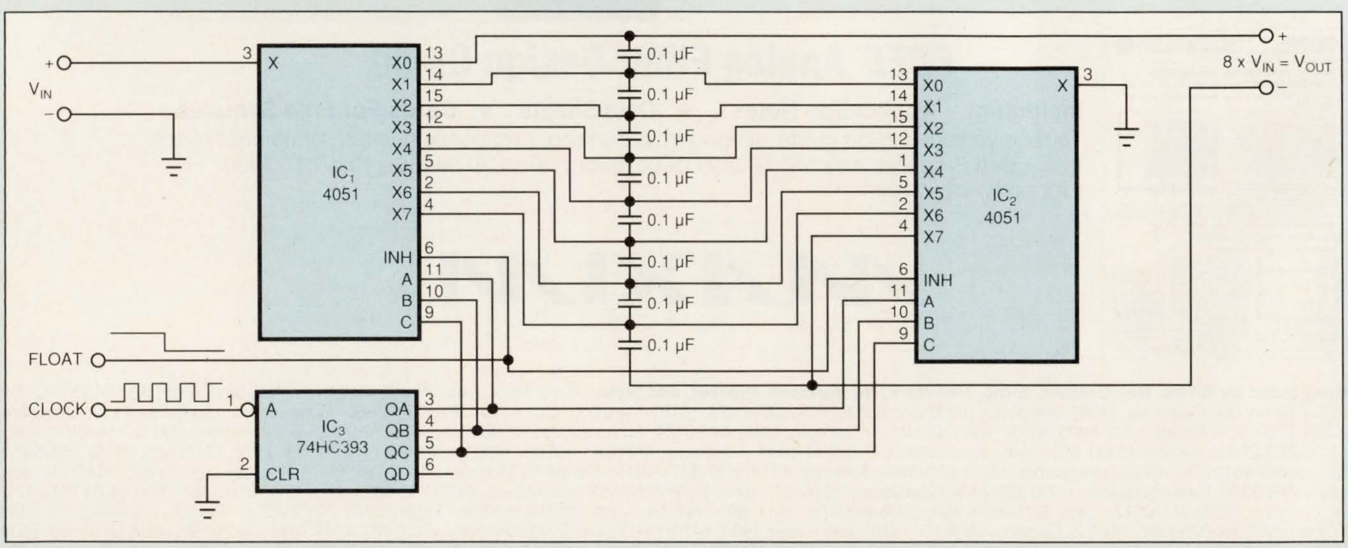

Fig 1—The stack of flying capacitors produces an overall gain of 8 for this novel "amplifier-less amplifier."

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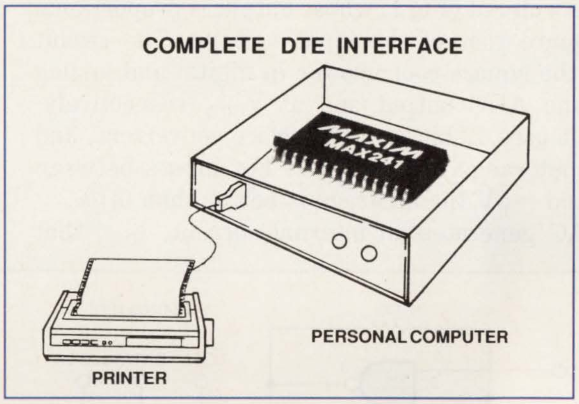

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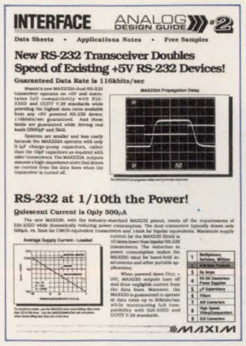
MAX233	2	2	None	No/No
MAX234	4	0	4x1μF	No/No
MAX235	5	5	None	Yes/Yes
MAX236	4	3	4x1μF	Yes/Yes
MAX237	5	3	4x1μF	No/No
MAX238	4	4	4x1μF	No/No
MAX239	3	5	2x1μF	No/Yes
MAX240	5	5	4x1μF	Yes/Yes
MAX241	4	5	4x1μF	Yes/Yes



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CIRCLE NO. 95

ADC/DAC combination finds square roots

Jeff Kirsten, Maxim Integrated Products, Sunnyvale, CA

Placing an ADC and DAC in an op amp's feedback loop forms a circuit (**Fig 1**) whose output is proportional to the square root of the input voltage. The circuit provides the square-root answer in digital and analog form at the ADC output and at V_{OUT}, respectively. The circuit uses 12-bit serial-interface converters, and has an input range of 0 to −5V. For inputs between −5 mV and −5V the accuracy is better than 0.1%.

The DAC generates an internal current, I_{DAC}, that represents the product of the applied digital code and the applied reference voltage, V_{REF}, as follows:

$$I_{DAC} = \frac{V_{REF}}{R} \times D,$$

where D equals the input code divided by 2^N, R is the internal R-2R ladder's equivalent resistance, and N is the converter's resolution in bits. Applying the same

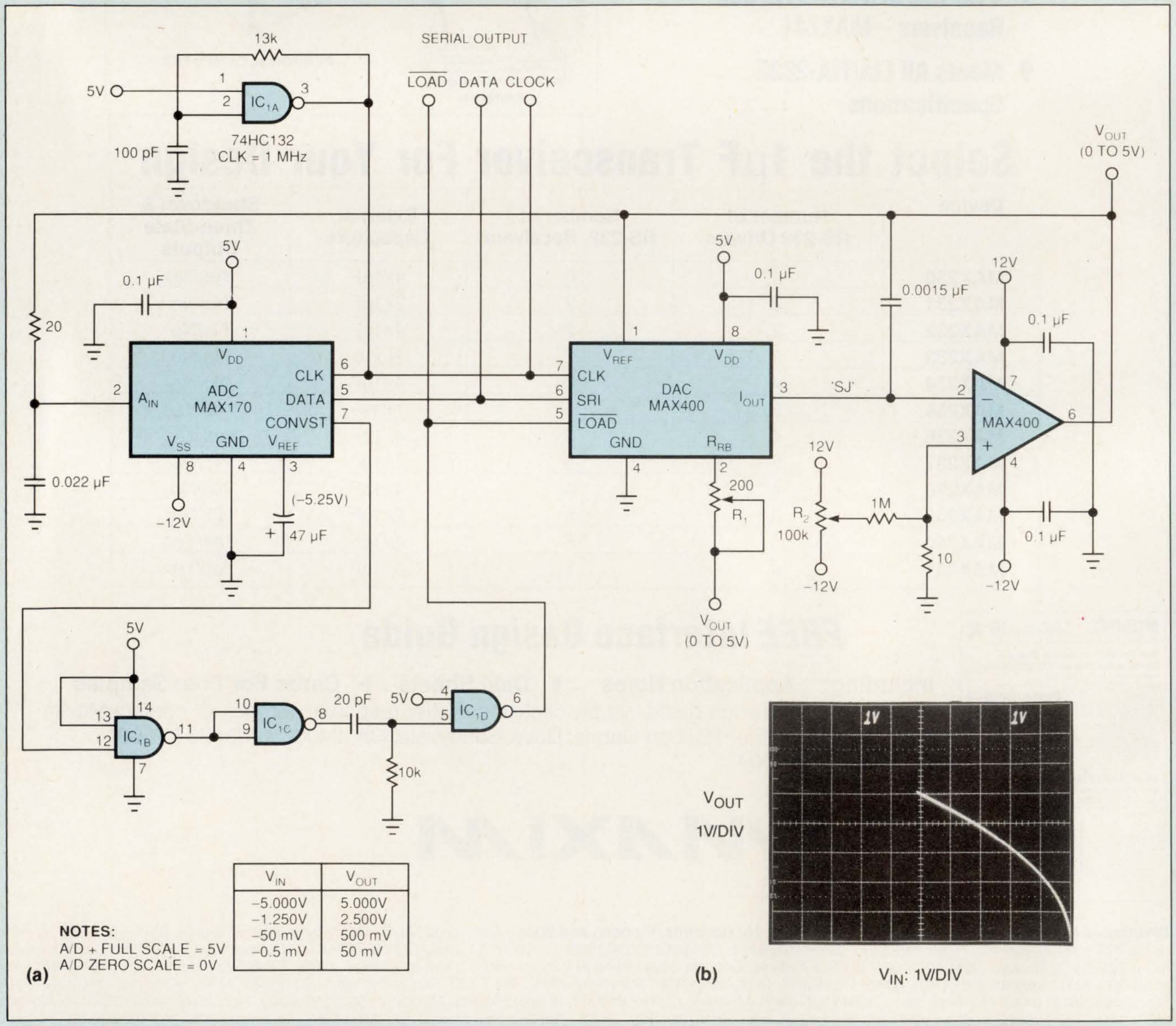

Fig 1—By placing an ADC and DAC inside an op amp's feedback loop, the circuit in (a) generates an analog and a digital signal, both of which are proportional to the square root of the voltage at V_{IN} (b).

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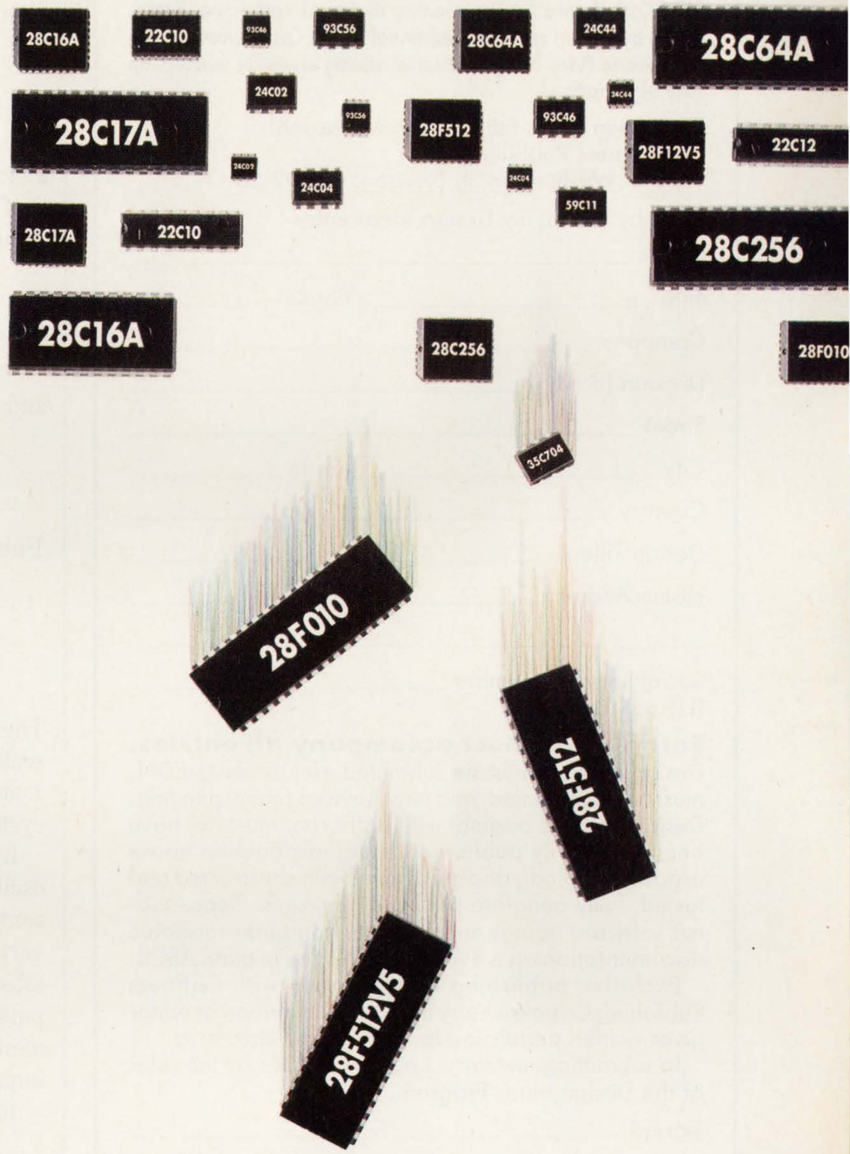

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CIRCLE NO. 96

ISSUE WINNER

The winning Design Idea for the January 2, 1992, issue is entitled "VFC consumes miniscule current," submitted by Jim Williams of Linear Technology Corp (Milpitas, CA).

ISSUE WINNER

The winning Design Idea for the January 20, 1992, issue is entitled "Active filter makes component selection easier," submitted by Michael Wyatt of SSO Honeywell Inc (Clearwater, FL).

value to the V_{REF} and D inputs makes I_{DAC} correspond to the square of that value: $V_{REF}=V_{OUT}$ by direct connection, and D approximately equals $V_{OUT}/5V$, which is the ADC's analog input divided by its full scale. After substituting these values into the above equation, the result is

$$I_{DAC} \approx \frac{V_{OUT}}{R} \times \frac{V_{OUT}}{5} = \frac{V_{OUT}^2}{5R}.$$

Because feedback forces the summing junction at pin 2 of the MAX400 op amp to zero volts, I_{DAC} equals the input current, $-V_{IN}/R$. Thus,

$$I_{DAC} = \frac{-V_{IN}}{R} \approx \frac{V_{OUT}^2}{5R}$$

and

$$\frac{V_{OUT}^2}{5} \approx -V_{IN}.$$

Finally,

$$V_{OUT} \approx \sqrt{5} \times \sqrt{-V_{IN}}.$$

The $\sqrt{5}$ factor is associated with the ADC's 5V full-scale level, and affects the output as the table in **Fig 1** shows. You can remove the factor by changing the system gain.

IC_{1A} and its associated components form a 1-MHz oscillator that clocks the two converters. The circuit configures the ADC to self start and continuously convert. The ADC's CONVST output at pin 7 goes high after each conversion, causing IC_{1D} to deliver a $\overline{LOAD}$ pulse to the DAC. R_1 provides for full-scale adjustments, and R_2 provides for an offset adjustment that improves the output accuracy for inputs between 0 and −100 mV. To calibrate the circuit, apply −5.000V at V_{IN} and adjust R_1 for 5.000V at V_{OUT}. Then apply −0.5 mV at V_{IN} and adjust R_2 for 50.0 mV at V_{OUT}.

To reduce the noise effects of digital coupling and 60-Hz fields, you should shield the op amp's summing junction by minimizing connector lengths between the inverting node, pin 3, and the DAC output and 0.0015-μF capacitor. Also, route serial-interface lines away from the node. **EDN BBS /DI_SIG #1073** EDN

To Vote For This Design, Circle No. 746

Text continued on pg 190

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Input/Output Voltage Range				
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±12V, Nominal	±7	±8.5	--	V
Gain	--	-1.0	--	V/V
Gain Error	--	±0.05	±0.5	%
Linearity Error	--	±0.005	±0.01	% FS
Sample Mode Offsett	--	±2	±7	mV
S/H Offset Error	--	±2.5	±25	mV
Gain Tempco Drift	--	±0.5	±15	ppm/°C
Sample Mode Offset Drift	--	±3	±15	ppm/°C
Pedestal Drift	--	±5	±20	ppm/°C
Acquisition Time				
10V to ±0.01% FS (±1 mV)	--	160	200	nS
Sample to Hold Settling Time				
10V to ±0.01% FS (±1mV)	--	60	100	nS
Sample-to-Hold Transient	--	100	--	mV p-p
Aperture Delay Time	--	10	15	nS
Aperture Uncertainty (Jitter)	--	±25	±50	pS
Output Slew Rate	200	300	--	V/μS
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Feedthrough	-69	-74	--	dB
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Registered PROMs form state machines

Dmitrii Loukianov, Coneco Ltd
Moscow, Russia

The text, circuit diagrams, and listings in **EDN BBS /DI_SIG #1122** present a general method of using Cypress CY7C225/235/245 registered PROMS as state machines.

To Vote For This Design, Circle No. 747

Self-modifying code speeds DSP32C interrupts

Steve Denny and Stephen J Roome, Data Sciences
Farnborough, Hants, UK

The documentation and listings in **EDN BBS /DI_SIG #1123** outline how to use self-modifying code to speed servicing multiple interrupts with an AT&T DSP32C DSP μP.

To Vote For This Design, Circle No. 748

Block floating-point FFT trades accuracy for speed

Vladimir Bochev, Bulgarian Academy of Sciences
Sofia, Bulgaria

For low-frequency audio applications, the "block" floating-point FFT method for the TMS320C25 in **EDN BBS /DI_SIG #1124** yields greater accuracy than other methods.

To Vote For This Design, Circle No. 749

Spice generates sine² pulse

Bashir Al-Hashimi, Matthey Electronics,
Stoke-on-Trent, England

The generalized Spice model in **EDN BBS /DI_SIG #1126** will generate a single sine² pulse, an important test waveform in communications.

To Vote For This Design, Circle No. 750

These Software Shorts listings are too long to reproduce here. You can obtain the listings from the Design Idea Special Interest Group on EDN's bulletin-board system (BBS): (617) 558-4241, 300/1200/2400/9600,8,N,1. From Main Menu, enter ss/DI_SIG, then rk*nnnn*, where *nnnn* is the number referenced above.

Feedback & Amplification

Respondents rise to challenge

Shu Zheng Ping's "Input accepts negative or positive pulses," EDN, August 19, 1991, pg 164, is a supposedly minimal-parts-count circuit. Although not specified, apparently the input pulse is ±6V and a propagation delay of 300 μsec is acceptable, based on the components shown. Isolation is not required, only that the circuit be able to handle "pulses of either polarity." The circuit in **Fig 1** will meet these specs and has a propagation delay of less than 1 μsec.

Brad Hanscom
NTI
355 N Sheridan St, #114
Corona, CA 91720

The circuit in **Fig 2** uses three inexpensive, general-purpose transistors to accept negative or positive pulses. The input is at zero level, transistors Q_1 and Q_2 are off, and Q_3 is on, yielding a zero output level. For a positive pulse, Q_1 switches on, switching Q_3 off, developing a positive level at the output. If a negative pulse arrives, Q_2 conducts to switch Q_3 off, also developing a positive output. You can scale this simple circuit for different supply and input voltages.

M S Nagaraj
ISRO Satellite Centre
Airport Rd, Vimanapuro Post Office
Bangalore, Karnataka, India

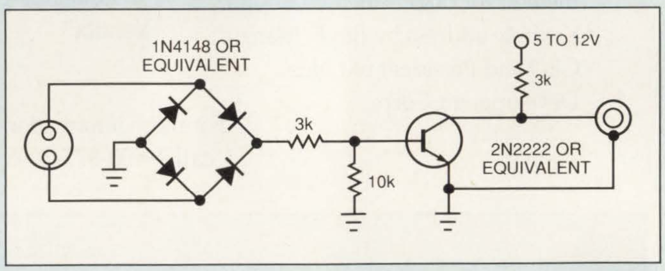


Fig 1—Paring parts count down to the bone, this circuit produces a unipolar output from positive or negative pulses.

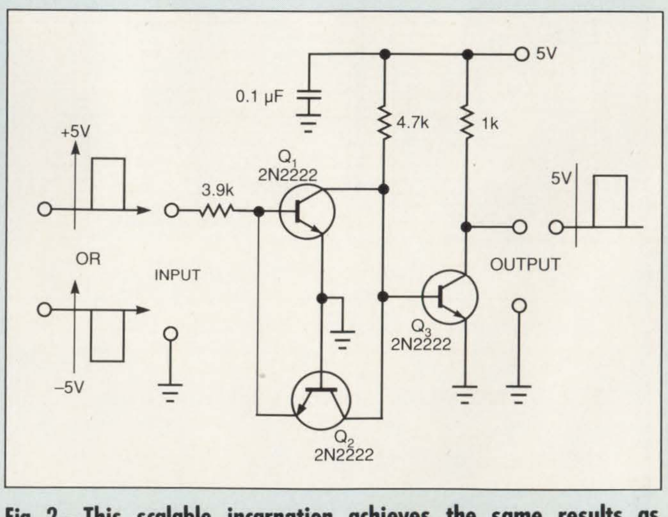
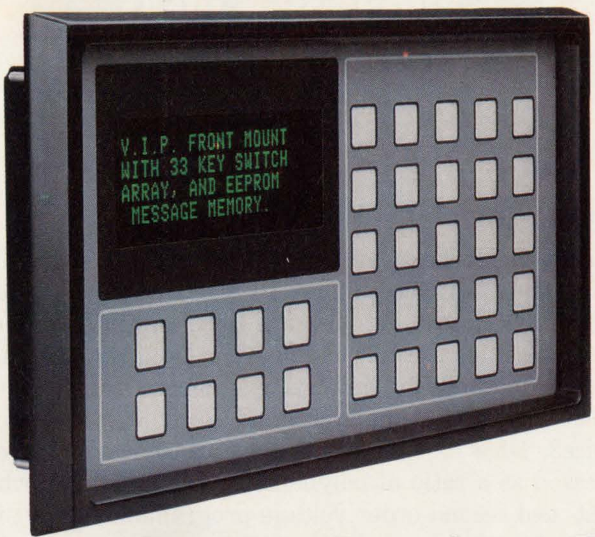


Fig 2—This scalable incarnation achieves the same results as Fig 1's circuit using a comparable number of inexpensive parts.



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Circle #57 Immediate

Circle #58 Reference

Corrections

Donald B Herbert, author of the comprehensive and interesting Software Shorts DI #1004, DI #1005, and DI #1006 (EDN, August 19, 1991, pg 166), reports that the titles are misleading. The programs actually provide methods for simulating s-domain transfer functions with both commercial and Berkeley versions of Spice2. DI #1004 simulates any transfer function expressed as a ratio of polynomials; DI #1005 describes first- and second-order voltage-programmable transfer functions models; and DI #1006 provides a specific example of simulating a motor-speed controller using the first-order voltage-programmable transfer-function model.

Author John A Haase has corrections to DI #1010 (EDN, September 2, 1991, pg 166). The circuit draws −9V from the center of the 2-battery string as well as −18V from the two batteries. The emitter of Q_1 connects to −9V; the emitters of Q_3 and Q_5 connect to −18V. The switch's left- and right-hand positions should carry 10V- and 5V-pulse labels, respectively.

Author Henry Yiu says that the equation in his DI #1013 (EDN, September 2, 1991, pg 160) needs a few more terms:

$$\text{dc offset} = 4 \times (\text{diode-drop offset}) + (\%\ \text{mismatch}\ C_1\text{-}C_2) \times ((\text{clock p-p voltage}) - 4 \times (\text{diode drop}))$$

Author Patrick H Conway wants to amend the math in his DI #973 (EDN, June 20, 1991, pg 162). The numerator of the right-hand side of the first equation should read NK_T/f instead of NK_Tf. Conway also supplies dimensions: the torque constant (stall torque) K_T is in newton-meters/volt; moment of inertia J is in newton-meter-sec^2 or kilogram-meters^2; and the viscous-friction coefficient (damping, back EMF, windage), f, is in newton-meters/radian/sec. Otherwise, he considered the Design Idea to have been very well edited.

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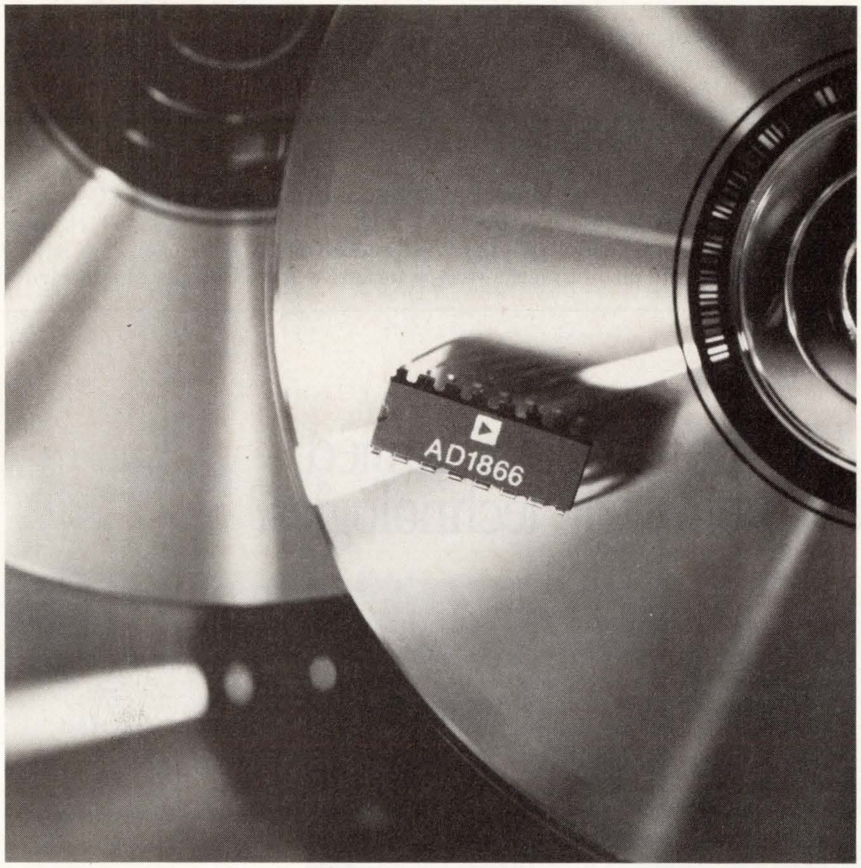
Analog Devices Inc, 181 Ballardvale St, Wilmington, MA 01887. Phone (617) 937-1428. FAX (617) 821-4273. **Circle No. 368**

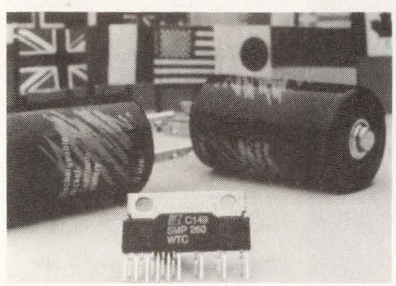


Laser-Diode Driver

- *Operates to 1.5 Gbps*
- *Provides 5- to 50-mA modulation*

A silicon bipolar IC, the IDA-07318 can drive laser diodes or LEDs in digital fiber-optic systems operating at speeds to 1.5 Gbps. The device suits data-communications terminals such as FDDI (100 Mbps) and FC (800 Mbps) as well as telecommunications such as SONET (OC-3 through OC-24). The IC features a 0- to 50-mA prebias and a 5- to 50-mA modulation current range. The driver operates from a single 5 or −5.2V supply and has a differential or single-ended input. In a hermetic 0.180-in.-square metal-ceramic surface-mount package, $50 (500).

Avantek, 481 Cottonwood Dr, Milpitas, CA 95035. Phone in US (800) 282-6835; in Canada, (416) 678-9430; in Europe, (49) 7031-140. **Circle No. 369**



Universal Power-Supply And Battery-Charger IC

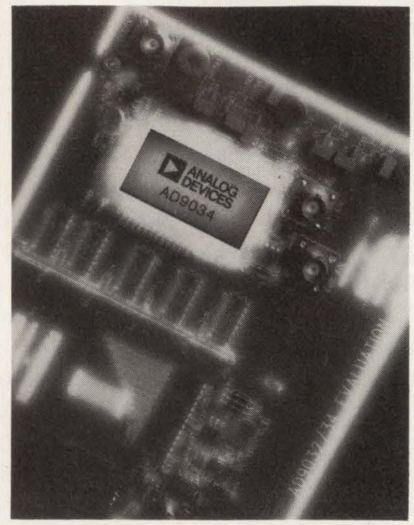
- *Delivers dc outputs of 60 or 30W*
- *Features fast current-mode control*

The PWR-SMP260 incorporates a high-speed current-mode controller, which is designed to minimize component count, size, and weight of power supplies and battery chargers. The device delivers dc outputs of 60W from rectified 220/240V ac inputs or 30W from universal 85 to 265V ac inputs. A companion IC, the PWR-SMP240, is rated at 40 and 20W output from 220/240V ac and universal inputs, respectively. The current-mode controller contains an off-line preregulator, oscillator, bandgap reference, summing junction, PWM comparator, gate driver, and soft-start circuitry. Protection circuits include overvoltage, overcurrent, and thermal runaway. The programmable oscillator lets the designer select a maximum duty cycle of either 50 or 95%. A feed-forward circuit at the summing junction maintains constant-power battery charging for quick-charge applications. SMP260 and SMP240, in 23-pin plastic SIPs, $4.25 and $3.85, respectively, (1000).

Power Integrations Inc, 411 Clyde Ave, Mountain View, CA 94043. Phone (415) 960-3572. **Circle No. 370**

Dynamic-RAM-accelerator module. The CYM7232 DRAM (dynamic RAM) Accelerator includes a bus interface that supports 50-MHz, 32- or 64-bit address/data bus systems and provides transaction, handshake, and bus-parity signals. Internal FIFOs accept a 128-byte burst. The 128-bit DRAM interface has four parallel 32-bit error-detection and correction paths, a 156-bit pipeline data register, and a 128- to 64-bit multiplexer. The module works with SPARC, 80486, 680x0, i860, and R4000 µPs, and their related caches. CYM7232, in 400-pin PGAs, $327 (100). **Cypress Semiconductor,** 3901 N First St, San Jose, CA 95134. Phone (408) 943-2600. **Circle No. 371**

SBus DMA controller. Compatible with LSI Logic's L68453 chip, the NIM618 DMA controller chip is an alternative for SBus peripheral-card designers. Unlike the L68453, which is limited to 24-bit addressing, the NIM618 device can access any part of the 32-bit SBus address space. Controller, $35 (100). **Nimbus Technology,** 2900 Lakeside Dr, Suite 205, Santa Clara, CA 95054. Phone (408) 727-5445. **Circle No. 372**



High-speed, 12-bit ADC. The AD9034 ADC features 20-Msample/sec speed. Available in three performance grades, minimum SFDR (spurious-free-dynamic-range) specifications range from 70 to 74 dBc at 1.2 MHz and from 67 to 70 dBc at 9.6 MHz. All three grades offer a minimum S/N ratio of 65 dB at 1.2 MHz. Full-scale gain error is typically ±0.5%. The ADC includes a T/H amplifier, summing amplifier, reference, digital error-correction and timing circuitry. In 40-pin ceramic DIPs or flatpacks, from $715 (100). Delivery four to six weeks ARO. **Analog Devices Inc,** 7910 Triad Center Dr, Greensboro, NC 27409. Phone (919) 668-9511. **Circle No. 373**

4-Mbit EEPROM. The WE512K8-150 CMOS EEPROM comes in a standard 32-pin hermetically sealed DIP and has a JEDEC standard byte-wide pinout. Organized as 512k×8 bits, the EEPROM operates from a 5V supply and features 10-year data retention and a read access time of 150 nsec. Typical operating current is 80 mA at 25°C and 5 MHz, and standby current is 1 mA. Industrial grades, $1630; military grades, $1800 (100). **White Technology Inc,** 4246 E Wood St, Phoenix, AZ 85040. Phone (602) 437-1520. FAX (602) 437-9120. **Circle No. 374**

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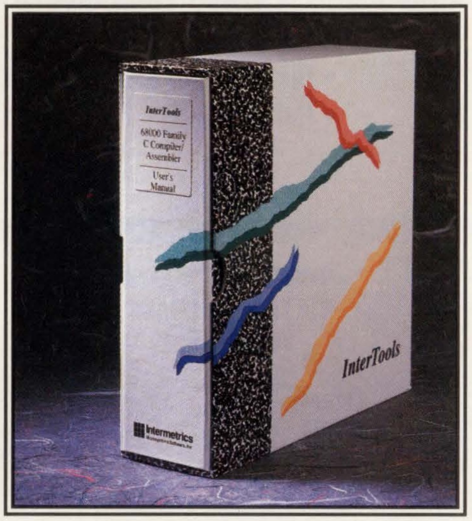

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CIRCLE NO. 148

Communications controller. Featuring an on-chip embedded RISC (reduced-instruction-set-computer) processor, the CL-CD1864 I/O controller can connect as many as eight full-duplex, asynchronous communications channels. Each channel can transfer data at rates to 64 kbps. The embedded processor minimizes the need for the host CPU to control the communications functions directly for every channel, thus increasing system efficiency. CL-CD1864, in a 100-pin quad flatpack, $33 (1000). **Cirrus Logic Inc,** 1463 Centre Pointe Dr, Milpitas, CA 95035. Phone (408) 945-8300. FAX (408) 263-5682.
Circle No. 375

Analog-digital array. The Quickchip-7 tile array features npn transistors with an f_T>12 GHz. The analog section contains 208 npn transistors, 56 pnp transistors, 32 Schottky diodes, and 848 resistors. The digital section, optimized for ECL designs, contains 336 npn transistors, 32 Schottky diodes, and 560 400Ω and 2000Ω resistors. The periphery of the chip contains 48 npn transistors, 24 1.35-pF capacitors, 64 ESD protection diodes, and 40 bond pads. Design start-up package, $15,000; prototypes (one wafer), $40,000. **Tektronix Microelectronics,** Box 500, Beaverton, OR 97077. Phone (503) 627-2515. **Circle No. 376**

Cache-TAG static RAMs. Featuring access times as low as 10 nsec, the 7C180 and 7C181 16-kbit cache TAG SRAMs eliminate wait states in 80386, 80486, and 68040 processors operating at speeds to 50 MHz. The 4k×4-bit SRAMs contain a 4-bit "TAG" comparator with a match output pin. The device compares the TAG RAM contents with current input data, and the result appears on the match pin. In 22-pin DIPs and 24-pin SOJ packages, and in speed ratings from 10 to 25 nsec, from $7.79 to $20.86 (100). **AT&T Microelectronics,** Dept 52AL040420, 555 Union Blvd, Allentown, PA 18103. Phone (800) 372-2447, ext 825; in Canada, (800) 553-2448, ext 825. FAX (215) 778-4106.
Circle No. 377

High-speed PLD. Based on the 22V10 architecture, the GAL22V10B-7 programmable logic device (PLD) features a maximum propagation delay of 7.5 nsec. The 24-pin device operates at a clock frequency of 111 MHz and has a typical current drain of 90 mA. In DIPs and plastic leaded chip carriers, $18 and $18.50, respectively (1000). **Lattice Semiconductor Corp,** 5555 NE Moore Ct, Hillsboro, OR 97124. Phone (503) 681-0118. FAX (503) 681-0347. TLX 277338. **Circle No. 378**

Analog interface circuit. Designed to meet the 11.4-kHz bandwidth required for multimedia audio processing the TLC32047 integrates several functions. Included are a bandpass switched-capacitor antialiasing filter, a 14-bit ADC, a 14-bit DAC, a lowpass output-reconstruction filter, signal-conditioning functions, control, timing, and a serial-port interface. TLC32047, from $15.33 (1000). **Texas Instruments,** Semiconductor Group (SC-92009), Box 809066, Dallas, TX 75380. Phone in US and Canada, (800) 336-5236, ext 3990; (214) 995-6611, ext 3990. **Circle No. 379**

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Synopsys	Sun-4 Interface to Mentor, Valid, Viewlogic	Design synthesis, test synthesis
Valid	Sun/Solbourne DECstation 3100 IBM RS6000	Design capture, simulation Design check GED, ValidSIM, RapidSIM
VIEWlogic	Sun-4 PC386	Design capture, simulation Design check

OKI Semiconductor

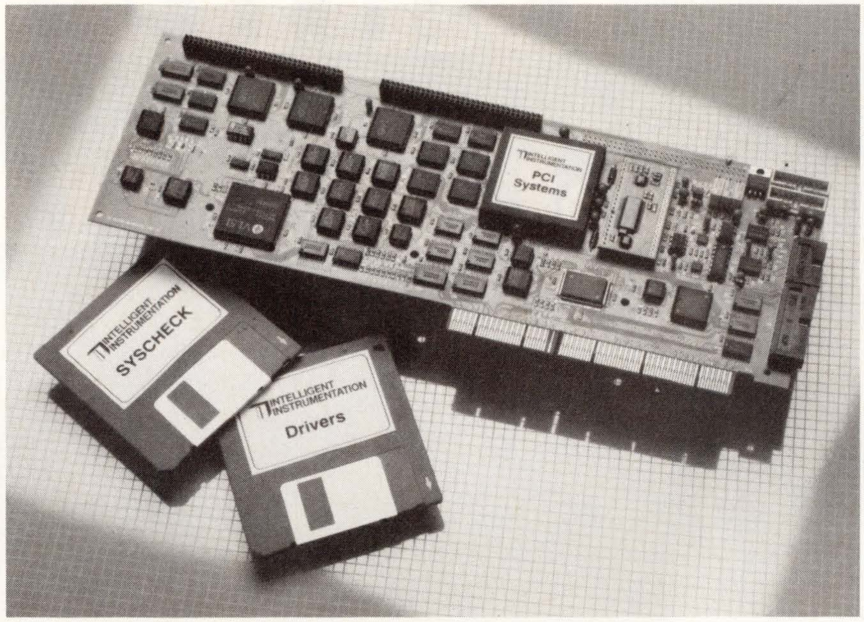
785 North Mary Avenue
Sunnyvale, CA 94086-2909
800-OKI-6388

TRANSFORMING TECHNOLOGY INTO CUSTOMER SOLUTIONS

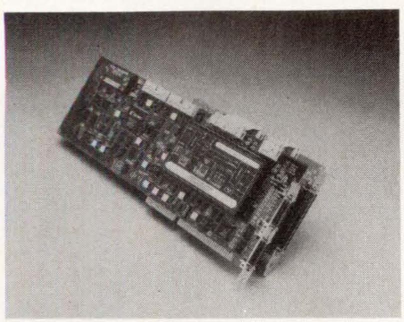
1-Msample/sec EISA Bus Data-Acquisition Board

- *Plug-on modules allow many configurations*
- *Permits burst-mode DMA to 16 Mbytes/sec*

The PCI-20501C-1 board plugs into the EISA bus. It includes a 12-bit 1-Msample/sec ADC preceded by a buffer amplifier that has a fixed gain of 1. The board has eight single-ended inputs and two DMA channels that can operate simultaneously. Of these, one is general purpose and one transfers ADC data to memory. Expansion modules, two of which can plug onto the board, accommodate additional channels and functions. The PCI-20501C-2 lacks an ADC (you use it with separate ADC boards), has a single general-purpose DMA channel, and holds three plug-ins. The general-purpose DMA channels operate at a sustained rate of 1 Mbyte/sec or a burst rate of 16 Mbytes/sec. The ADC DMA channel operates at 2 Mbytes/sec. Board with ADC, $2470; without ADC, $1495.



Intelligent Instrumentation, 1141 W Grant Rd, MS 131, Tucson, AZ 85705. Phone (602) 623-9801. FAX (602) 623-8965. **Circle No. 380**



High-Channel-Count, 1-Msample/Sec ADC Board

- *Configurable to 224 single-ended inputs*
- *Channel-list hardware programs rate and gain for all channels*

The DT2839 12-bit ISA bus data-acquisition board has a 1-Msample/sec ADC and 32 single-ended or 16 differential inputs. The DT2896 expander, also an ISA plug-in, adds 96 single-ended or 48 differential inputs. The ADC board, which allows use of two expanders, offers software-programmable gains of 1, 2, 4, and 8. Throughput ranges from 224 ksamples/sec to 1 Msample/sec, depending on the number of channels used, the gain, and whether you use expanders. Channel-list hardware supports the expanders and allows flexibility in configuring scans. The ADC board includes 16 digital I/O lines, two 130-kHz, 12-bit DACs with software calibration, two programmable clocks, and two 16-bit counter-timers. ADC board with software, $3495; expander, $995.

Data Translation Inc, 100 Locke Dr, Marlborough, MA 01752. Phone (508) 481-3700. FAX (508) 481-8620. TLX 951646. **Circle No. 381**

Phase-Angle Multimeter

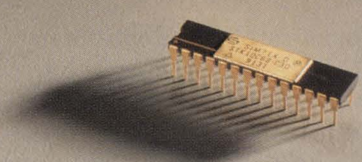
- *Operates from 0.1 Hz to 100 kHz*
- *Phase error is <0.05°*

The 6000 phase-angle multimeter uses a 28-MHz DSP56001 and a 20-MHz MC68020 μP to perform 2048-point FFTs on all of the signals gathered by its 18-bit ADC. Over its bandwidth—0.1 Hz to 100 kHz—the instrument measures with errors of <0.05° in phase, <0.05% in amplitude, and <0.01% in frequency. The unit, which generates harmonics at least 85 dB below full scale, simultaneously measures the phase, frequency, and rms amplitude of each signal harmonic, from the fundamental to the 50th. Beside a 20-character × 4-line vacuum-fluorescent display, the unit has a 4.5-in.-long, 101-element LED bar graph, which operates either as an adjustable-reference zero-center null meter or as a linear or logarithmically scaled (4½-decade) meter. $8485. Delivery, five weeks ARO.

Xitron Technologies Inc, 10255 Barnes Canyon Rd, Suite A102, San Diego, CA 92121. Phone (619) 458-9852. FAX (619) 458-9213.

Circle No. 382

Batteries not included.



Nonvolatile random access memory doesn't need batteries anymore. It doesn't need an extra chip either. All it needs is this. The nvSRAM from Simtek.

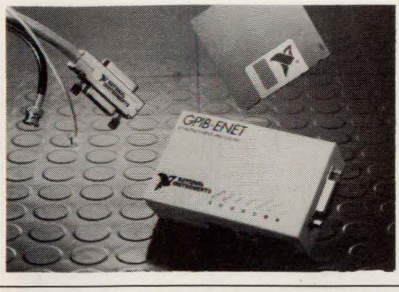
At 64K, the nvSRAM offers the density to handle virtually anything you can come up with. It's extremely fast, with access speeds ranging from 30ns-55ns. It doesn't depend on a battery for nonvolatility, so reliability is unsurpassed. And because it's a one-chip solution, precious little board space is required.

We think you'll find our nvSRAM is well suited to applications ranging from cellular phones to the most advanced military hardware. To prove it, we'll send you a free design kit. And we guarantee you'll get it within 48 hours of your request. So call Simtek at 1-800-637-1667 right now for your free design kit (For production quantities, call your local Arrow/Schweber Electronics branch). And find out why, when it comes to nonvolatile RAM, batteries are dead.

SIMTEK

719-531-9444 Fax 719-531-9481

CIRCLE NO. 151



Ethernet-to-IEEE-488 SPARCstation controller. The GPIB-ENET/Sun kit controls IEEE-488 instruments from any SPARCstation that can use Ethernet to access a TCP/IP (transfer-control protocol/internet protocol) network. The kit removes the usual 20m limitation on the length of IEEE-488 cabling and also allows one workstation to host as many as 64 IEEE-488 controllers, each driving 14 instruments (in other words, 896 instruments). $1595 to $1695 depending on your Ethernet wiring scheme with single-workstation software license. **National Instruments Corp,** 6504 Bridge Point Pkwy, Austin, TX 78730. Phone in US and Canada (800) 433-3488; (512) 794-0100. FAX (512) 794-8411. TLX 756737.
Circle No. 383

100-Msample/sec ISA bus DSO board. The Compuscope 250 plugs into the 8-bit ISA bus. It digitizes one channel to 100 Msamples/sec or two channels simultaneously to 50 Msamples/sec each. Resolution is 8 bits. Bandwidth is 50 MHz. Memory depth is 16 kbytes/channel. $3500 including software drivers. **Gage Applied Sciences Inc,** 5465 Vanden Abeele, Montreal PQ, H4S 1S1 Canada. Phone (514) 337-6893. FAX (514) 337-8411. **Circle No. 384**

Portable protocol analyzer/simulator. The Chameleon 1800 permits network testing and fault diagnosis at speeds to 2.048 Mbps. It decodes and analyzes ISDN (integrated-services-digital-network) primary-rate-interface data in real time and provides a graphical display of the network condition. Introductory price, $18,000. **Tekelec,** 26580 W Agoura Rd, Calabassas, CA 91302. Phone (818) 880-5656. FAX (818) 880-6993. **Circle No. 385**

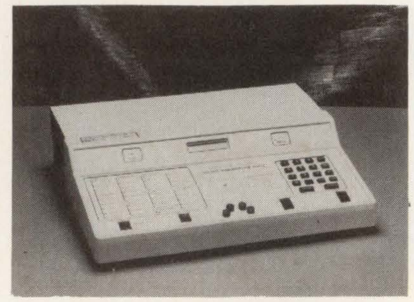
25A safety ground test set. The 5001A test set lets you test products in production for compliance with US, Canadian, and European electrical safety standards. It handles both the 25A ground-wire test and the 500V insulation-resistance test. Versions are available for 115V, 50/60 Hz, 4.5A and 230V, 50/60 Hz, 2.5A. A single receptacle lets you plug in finished products; there are terminals for component tests. $2600. Delivery, four to six weeks ARO. **Associated Research,** 905 Carriage Park Ave, Lake Bluff, IL 60044. Phone (800) 858-8378. FAX (708) 295-9165. **Circle No. 386**

Digital-readout ESD testers. The MZEC1 through MZEC4/XV testers are based on the vendor's MiniZap simulator. They simulate both the electrostatic discharges (ESD) and the victim equipment. The units handle tests in the traditional air-discharge mode as well as in the newer contact mode. Diagnostic capabilities facilitate pinpointing the true causes of ESD failures. From $6490. Delivery, 30 to 60 days ARO. **Keytek Instrument Corp,** 260

Fordham Rd, Wilmington, MA 01887. Phone (508) 658-0880. FAX (508) 657-4803. **Circle No. 387**

Temperature-monitoring system. The 575-ELX-Temp provides hardware and software for 16-channel, 16-bit-resolution measurements using thermocouples or semiconductor sensors or 7-channel measurements using isolated thermocouples or RTDs (resistance temperature detectors). The product is based on the firm's Easyest LX software and 575-2 data logger. $4150. **Keithley Metrabyte,** 440 Myles Standish Blvd, Taunton, MA 02780. Phone (508) 880-3000. FAX (508) 880-0179. **Circle No. 388**

Tester for discrete semiconductor devices. The model 8800 performs parametric and go/no-go tests on transistors, diodes, MOSFETs, JFETs, regulators, triacs, SCRs, and zeners in a range of packages. Using just four universal fixtures, it tests to 1200V and 5A with a resolution of 1 mV and ±0.1 nA. $6900. **Information Scan Technology Inc,** 487 Gianni St, Santa Clara, CA 95054. Phone (408) 988-1908. FAX (408) 980-1794. **Circle No. 389**

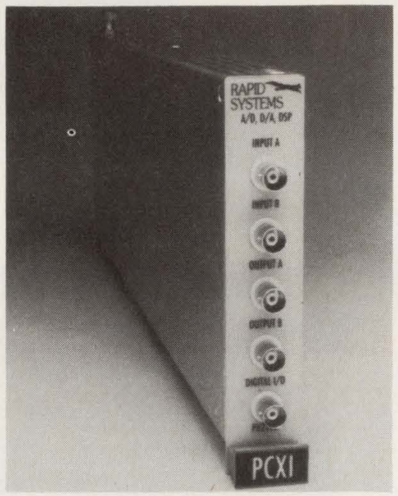


Data-acquisition-board drivers for Basic dialect. This set of software drivers works with the vendor's HTBasic and several ISA bus data-acquisition boards from National Instruments. Your program accesses the boards using familiar commands. The software automatically scales analog data into voltage units and stores the data in arrays of the Real data type. HTBasic Drivers, $75. **TransEra Corp,** 3707 N Canyon Rd, Provo, UT 84604. Phone (801) 224-6550. FAX (801) 224-0355. TLX 296438. **Circle No. 390**

Clamp-on multimeter. The 380911 meter measures ac current to 300A, ac voltage to 750V, dc voltage to 1 kV, and frequency from 10 to 1999 Hz. It also measures temperature and checks continuity and diode function. A data-hold button freezes readings. A 9V battery operates the unit for 200 hours. $99. **Extech Instruments Corp,** 335 Bear Hill Rd, Waltham, MA 02154. Phone (617) 890-7440. **Circle No. 391**

52-pin plastic-leaded-chip-carrier pin isolator. The PLeCSE-52-H works with instruments such as logic analyzers and in-circuit emulators. It accepts an IC and plugs into an IC socket on your target board. There is a switch for each device pin and test pins on both sides of each switch. Therefore the unit lets you isolate any or all of the device pins from the board. $223. **EDI Corp,** Box 366, Patterson, CA 95363. Phone (209) 892-3270. FAX (209) 890-3610. **Circle No. 392**

Handheld inductive-loop analyzer. The ILT II meter measures inductance, resistance, capacitance, and Q—the so-called quality factor—with 0.02% error from 10 to 100 kHz. The DSP-based unit incorporates built-in diagnostic routines. It has an RS-232C port and is programmable to permit enhancements in the field. AC-powered version, $2395; battery-powered version, $2595. **DVP Inc,** 2401 Research Blvd, Rockville, MD 20850. Phone (301) 670-9282. **Circle No. 393**



PCXI bus audio-analysis module. The PX2362 analyzer plugs into the PCXI (PC extended for industry) bus. The 2-channel unit, which has a bandwidth of 1 to 50 kHz, includes a 20-MHz µP with 256k words of dynamic RAM and 32 kbytes of zero-wait-state RAM. It averages signals and computes floating-point FFTs from 64 to 2048 points. $3495. **Rapid Systems Inc,** 433 N 34th St, Seattle, WA 98103. Phone (206) 547-8311. **Circle No. 394**

100-kHz to 100-GHz VXIbus power meter. The 4052 single-slot C-size module can incorporate as many as four channels. It measures power from 100 pW (−70 dBm) to 7W. In conjunction with microwave sweep generators and suitable directional couplers, it forms a scalar network analyzer. $3750. Delivery, six weeks ARO. **Racal-Dana Instruments Inc,** 4 Goodyear St, Irvine, CA 92718. Phone (800) 722-3262. FAX (714) 859-2505. **Circle No. 395**

In-circuit emulator for 8XC053/54. The POD-C054 works with the vendor's EMUL51-PC to provide full-speed µP emulation in configurations that have as much as 16 kbytes of memory. The emulator controls all nine of the ICs' pulse-width-modulated commands as well as the three digital-video outputs. A plug-in trace board is optional. $895. **Nohau Corp,** 51 E Campbell Ave, Campbell, CA 95008. Phone (408) 866-1820. FAX (408) 378-7869. **Circle No. 396**

5- and 10-Msample/sec 12-bit VMEbus ADC boards. The $4495 5-MHz ZPB1604 and the $3495 10-MHz ZPB1603 are 6U-size modules. The lower-speed unit has a spurious-free dynamic range (SFDR) of 80 dB and total-harmonic distortion (THD) of −80 dB. The faster board's SFDR is 72 dB; its THD is −68 dB. **Burr-Brown Corp,** Box 11400, Tucson, AZ 85734. Phone (602) 746-1111. **Circle No. 397**

In-circuit emulator for 68HC16Z1. The Mime-700 gives you flexibility in configuring the processor, yet does not interfere with the µP's function. The emulator, which allows 2 Mbytes of emulation RAM, supports full-speed zero-wait-state processor operation, and has an 8k-frame × 128-bit trace buffer with 48-bit time stamping. $14,659 with 256-kbyte emulation memory. **Pentica Systems Inc,** 19A Crosby Dr, Bedford, MA 01730. Phone (617) 275-4419. **Circle No. 398**

Portable PC-based data-acquisition system. The M-Tech 16-channel data-logging system housed in a portable PC based on a 25-MHz 80386 with 2 Mbytes of RAM, a 100-Mbyte hard disk, and a 640 × 480-pixel display. The 12-bit ADC, which is preceded by a 16-channel antialiasing filter, takes 150 ksamples/sec. From $12,985. **Onsite Instruments,** 855 Maude Ave, Mountain View, CA 94043. Phone (415) 964-9800. FAX (415) 964-9808. **Circle No. 399**

Qualifier/tester for Fast-SCSI disk drives. The PR4050 tester transfers data synchronously at 10 Mbytes/sec and can test disk drives and optical memories without your having to remove them from your system. It acts as a passive monitor or an active tester and can sometimes test drives without interfering with normal system operation. From $8750. **Pioneer Research,** 1745 Berkeley St, Santa Monica, CA 90404. Phone (800) 233-1745; (310) 829-6751, ext 202. **Circle No. 400**

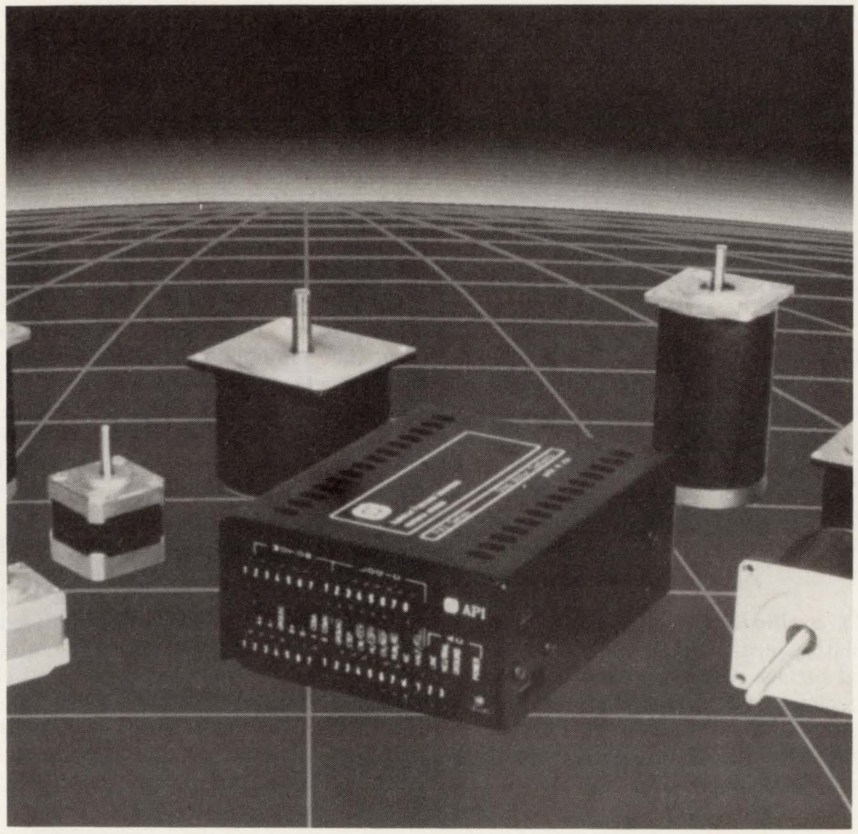
CIRCLE NO. 155

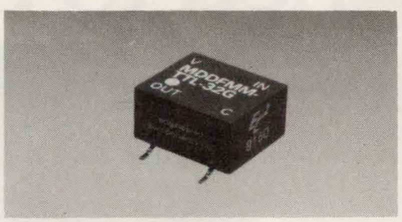
Step Motors

- *Operate from 115 or 230V ac*
- *Offer full- and half-step resolutions*

The dual-axis step-motor packages in the P42 Series operate from either 115 or 230V ac inputs. Each package offers full- and half-step resolutions, static torques ranging from 20 to 150 oz-in., and speeds in excess of 1800 rpm. Packages come complete with two motors, two drives, power supply, integral heat sink, mounting brackets, cabling, and connectors in a full enclosure. The package generates its own 5V logic power for internal optical isolation circuitry. The power section provides DIP-switch-selectable currents from 0.3 to 3.5A/phase to the motor windings and will drive motors rated as high as 5A/phase. $845 for a package containing two size 23 motors.

American Precision Industries Inc, 4401 Genesee St, Buffalo, NY 14225. Phone (716) 631-9800. FAX (716) 631-0152. **Circle No. 421**





Frequency Multiplier

- *Available in through-hole or surface-mount package*
- *Generates a TTL output*

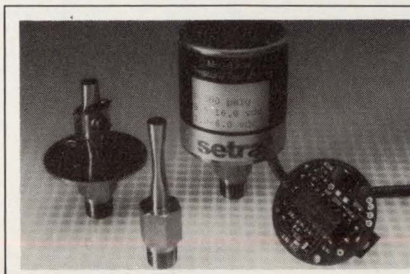
The MDDFMM-TTL frequency multiplier is available in through-hole or surface-mount (gull- or J-lead) packages. The unit provides a T^2L square-wave output at selected clock frequencies that are synchronized to a lower-frequency clock. In a typical application, the module can generate a clock that is a multiple of the system clock and phase-locked to the system clock. During a system-clock cycle, you can use the multiplier's clock to process additional information. If no synchronizing input is present, the module will free-run, providing a square-wave output that is accurate within ±2% of the desired frequency. The module generates 38 clock frequencies over a 2- to 100-MHz range; each output can drive 10 TTL loads. Less than $12 (100).

Engineered Components Co, Box 8121, San Luis Obispo, CA 93403. Phone (800) 235-4144; (805) 544-3800. **Circle No. 422**

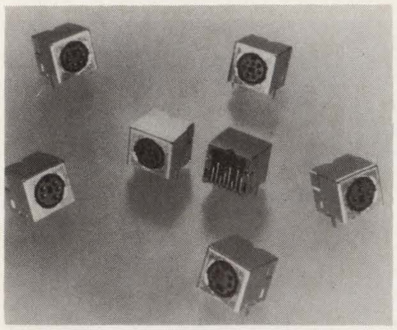
Pressure Transducer

- *Handles industrial environments*
- *Employs capacitive technology*

The Model 208 gauge-pressure transducer handles the extreme conditions encountered in industrial environments. The unit employs a sensing element consisting of a flattened stainless-steel pressure tube with parallel plates bonded to its two opposing external flats to form a sensitive capacitor. Pressure changes cause a minute change in distance between the plates to produce a measurable change in capacitance. An IC-based circuit converts the capacitance change to a dc signal. The unit maintains a ±0.25% accuracy and a 0.1% hysteresis. Full-scale pressure-measuring capability ranges from 25 to 10,000 psig. Less than $100 (OEM qty).



Setra Systems Inc, 45 Nagog Park, Acton, MA 01720. Phone (508) 263-1400. **Circle No. 423**



PC-board connectors. These surface-mount DIN connectors feature compliant contacts to minimize stress from thermal expansion. Housing material carries a UL 94V-0 rating. $0.77 to $2.52 for an 8-position model. **AMP Inc,** Box 3608, Harrisburg, PA 17105. Phone (800) 522-6752. **Circle No. 424**

ECL oscillators. E500 Series clock oscillators are available in through-hole and surface-mount versions. Output frequencies range from 24 to 180 MHz. Operating temperatures range from 0 to 70°C or from −40 to +85°C range. Stabilities down to 25 ppm are available. $43.90 for a 120-MHz model. Delivery, stock to seven weeks ARO. **Connor-Winfield Corp,** 1865 Selmarten Rd, Aurora, IL 60505. Phone (708) 851-4722. FAX (708) 851-5040. **Circle No. 425**

LED indicators. VL Series indicators are available in 0.236- and 0.314-in.-diameter, mounting-bushing sizes. A choice of two bezel styles is available for each bushing size. Available LED colors include red, yellow, or green. The units are available with optional sealing that meets IP67 requirements. $1.25 (1000). **MORS/ASC,** Box 544, Wakefield, MA 01880. Phone (617) 246-1007. FAX (617) 245-4531. **Circle No. 426**

Axial-leaded chokes. Series 90 chokes have 48 values ranging from 0.1 to 1000 μH. They are available with 10% tolerance as standard or an optional 5 and 3%. The chokes in an encapsulated package feature an epoxy coating. $0.11 (10,000). **Coilcraft,** 1102 Silver Lake Rd, Cary, IL 60013. Phone (708) 639-6400. **Circle No. 427**

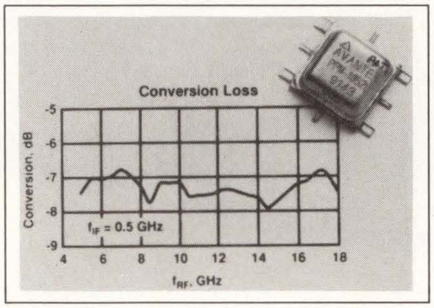
Zero-insertion-force connector. The DL5 260 ZIF connector can accommodate #18 through #36 AWG wire and is rated for 10,000 cycles. It's available with optional metal housings for the plug and receptacle to provide EMI/RFI shielding. The contacts are rated for 5A and handle 1200V ac voltage levels. Less than $100 (OEM qty). Delivery, 12 weeks ARO. **ITT Cannon,** 1851 E Deere Ave, Santa Ana, CA 92705. Phone (714) 757-8221. **Circle No. 428**

High-temperature capacitors. LMU Type capacitors are rated for 105°C operation. Capacitance values range from 330 to 1500 μF, and working voltage ratings range from 200 to 400V dc. Standard tolerance equals ±20%. $1.45 (1000). **Illinois Capacitor Inc,** 3757 W Touhy Ave, Lincolnwood, IL 60645. Phone (708) 675-1760. FAX (708) 673-2850. **Circle No. 429**

Lighted switch. Model 8128 spst illuminated momentary switches mount to the front panel. The units accommodate T-1 flange-based lamps. The switches can be mounted on 0.5-in. centers and have a life of 100,000 actuations. Switch contacts are rated for 30V dc or 115V ac; current rating equals 1A resistive or 0.25A inductive. \$8.50 (100). **Electro-Mech Components Inc,** 1826 N Floradale, South El Monte, CA 91733. Phone (818) 442-7180. **Circle No. 430**

Coaxial adapter. Model 9343 is a 50Ω mini-UHF female to mini-UHF female coaxial adapter. It covers a dc to 2-GHz range and operates from −65 to +165°C. The adapter has a brass, nickel-plated body and employs Teflon insulation and a gold-plated contact. \$3.95. **Pasternack Enterprises,** Box 16759, Irvine, CA 92713. Phone (714) 261-1920. **Circle No. 431**

0.25-in.-square mixer. Housed in a surface-mount package, the PPM-1852L double-balanced mixer spans a 5- to 18-GHz frequency band on the LO and RF ports. Conversion loss versus frequency is flat within ±2 dB, and maximum conversion loss equals 8 dB. VSWR at the LO and RF ports measures 3.5:1 and



2.5:1, respectively. \$146 (100). Delivery, stock to six weeks ARO. **Avantek Inc,** 481 Cottonwood Dr, Milpitas, CA 95035. Phone (800) 282-6835; (408) 943-3038. **Circle No. 432**

DIP sockets. Series SKD narrow DIP sockets feature 24- and 28-pin counts. Available with or without decoupling capacitors, the sockets have a mounted profile of 0.016 in. and feature a thermoplastic polyester housing, which carries a UL 94V-0 rating. From \$0.03 to \$0.10/contact. **Socket Express,** 100 Jersey Ave, Building B-202, Brunswick, NJ 08903. Phone (908) 247-9500. FAX (908) 247-9816. **Circle No. 433**

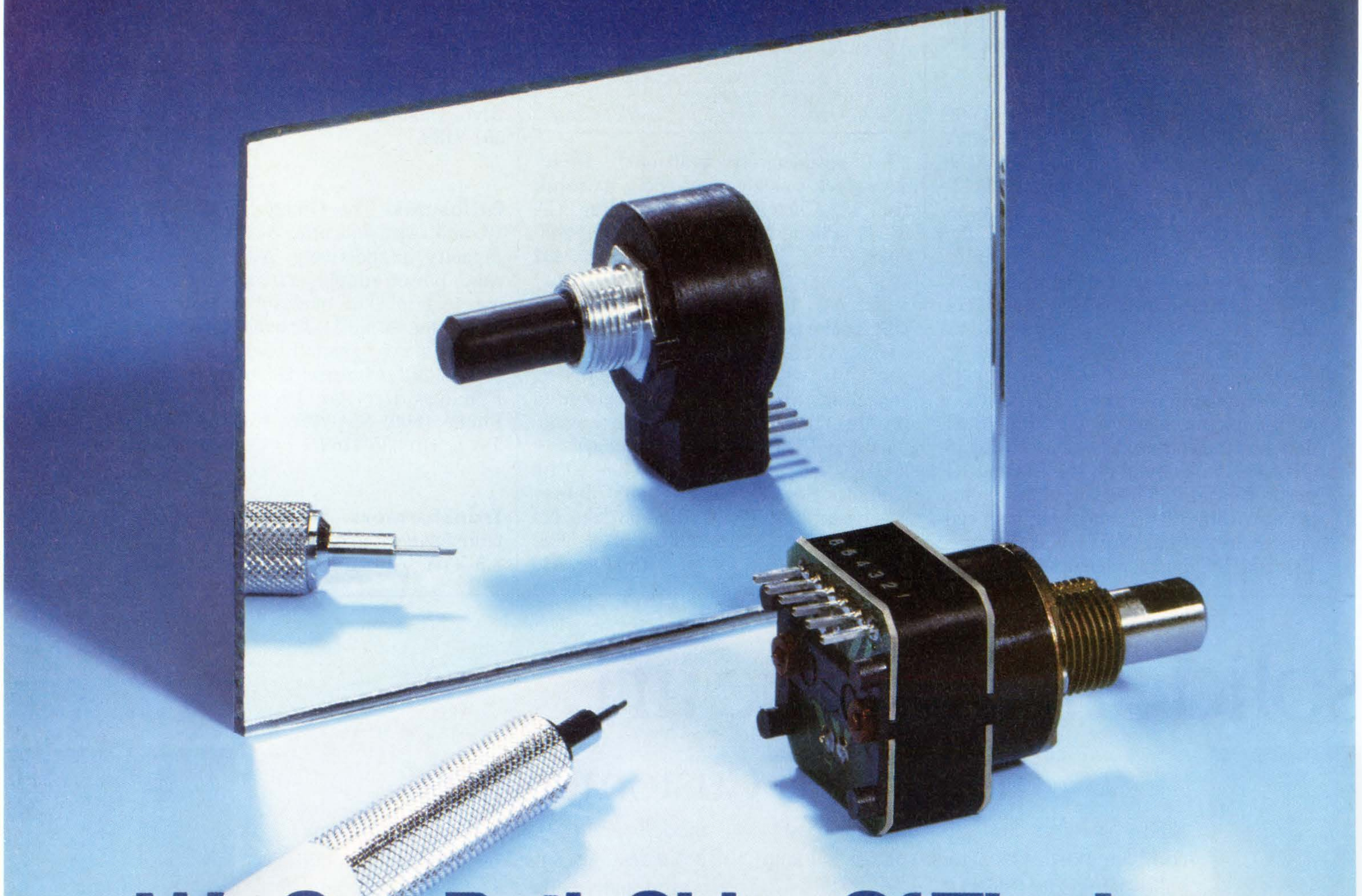
Power supplies. HD3003 Series 300W power supplies feature outputs of 5, 12, 15, 24, or 28V. They operate from 3-phase inputs and feature an internal EMI filter. Overload, overvoltage, and short-circuit protection are standard. You can run as many as five supplies in parallel without using external decoupling diodes. \$3100. **Rantec Microwave & Electronics Inc,** 24003 Ventura Blvd, Calabasas, CA 91302. Phone (818) 591-8189. **Circle No. 434**

Enclosures. The Omega Deskmate 8, 10, and 14 models offer 8-, 10-, or 14-slot capacity, respectively. All include card cage, power supply, wiring, and a cooling system. The enclosures have a 10-layer monolithic J1-J2 backplane as well as a J3 power-ground backplane. From \$2995. **Electronic Solutions,** 6790 Flanders Dr, San Diego, CA 92121. Phone (800) 854-7086; (619) 452-9333. TWX 910-335-1169. **Circle No. 435**

Transformers. HPI line frequency transformers are rated at 2, 2.75, and 3.5 kVA. All three models feature dual

OakGrigsby On Optical Encoders

1 OF A SERIES



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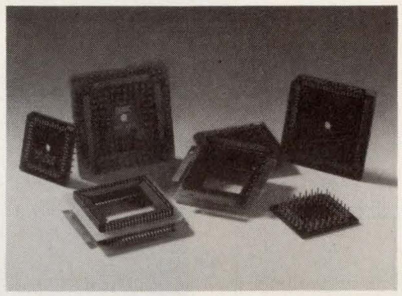
CIRCLE NO. 158

primaries with taps at 100, 115, and 230V and dual secondaries with 115 and 230V taps. Reinforced bobbins and high-temperature magnet wire are used in all models. The units feature a 95% efficiency, 5 to 7% regulation, and 4000V rms isolation. $368 to $450. **Signal Transformer Co Inc,** 500 Bayview Ave, Inwood, NY 11696. Phone (516) 239-5777. **Circle No. 436**

Terminal blocks. ELFT Series terminal blocks are available in versions with 2 to 24 positions. Pin spacings of 0.2 in. and 5 mm are available. The units accept wires from the top or bottom and feature a termination scheme that traps the wire and contact between nonrotating parallel surfaces. The blocks accept wire sizes ranging to #12 AWG. 8-position connector, $4 (small qty). **PCD Inc,** 2 Technology Dr, Peabody, MA 01960. Phone (508) 532-8800. FAX (508) 532-6800. **Circle No. 437**

Electrolytic capacitors. Type ILS aluminum electrolytic capacitors operate from −40 to +85°C. Capacitance values range from 0.1 to 100 μF. Standard tolerance values equal ±20 or ±10%. Leakage current measures 0.4 μA, and working voltage values range from 10 to 50V dc. $0.096 (1000). **Illinois Capacitor Inc,** 3757 W Touhy Ave, Lincolnwood, IL 60745. Phone (708) 675-1760. FAX (708) 673-2850. **Circle No. 438**



Surface-mount adapters. These surface-mount PLCC (plastic-leaded-chip-carrier) adapters interconnect a daughter card via a PLCC socket on a mother board. The phosphor bronze contacts feature 30 μin. of gold plating. The housing material accommodates all soldering processes. $15 (500) for a 68-pin unit. **McKenzie Technology,** 44370 Old Warm Springs Blvd, Fremont, CA 94538. Phone (510) 651-2700. **Circle No. 439**

Temperature controller. The Series 1400 controller provides alarm or temperature control. The front panel is splash proof. Inputs include thermocouple, RTD, and thermistor. Scales are calibrated in F and C. An LED deviation indicator shows when the temperature is below, at, or above the set value. From $99. **Love Controls Corp,** 1475 S Wheeling Rd, Wheeling, IL 60090. Phone (312) 541-3232. **Circle No. 440**

Polyester capacitors. Type RBE polyester box capacitors pass UL 94V-0 and Bellcore flammability specifications. Capacitance values range to 10 μF with voltage ratings ranging from 50 to 630V dc. The units are available with lead spacings of 5, 7.5, 10, 15, 22.5, and 27.5 mm. $0.20 (1000) for a 0.1-μF, 50V, 5-mm unit. **Aerovox,** 742 Belleville Ave, New Bedford, MA 02745. Phone (508) 999-1000. **Circle No. 441**

CIRCLE NO. 160

CAE & Software Development Tools

DSP Multimedia Environment

- *Real-time OS and multimedia modules*
- *Software-development tools for DSP3210*

The VCOS Multimedia Development Environment (VMDE) for the AT&T DSP3210 digital signal processor enables PCs to perform multimedia DSP tasks. The software includes modules for real-time speech coding, fax and data modems, MPEG and P*64 audio, and JPEG still-image compression and decompression. It also includes an operating system, VCOS, that allows real-time execution of those modules. VCOS consists of a DSP-resident kernel and a host-resident application server. Your application program makes calls to the appropriate multimedia modules; the VCOS application server (VCAS) then loads the necessary routines and data from PC memory into the DSP3210's on-chip memory, manages execution of the routines, and returns results to the application.

By caching critical code segments in the DSP's internal RAM, VCOS allows the DSP to run programs and access data directly out of host memory. The complete package includes a variety of software development tools and libraries. For PCs, the software requires an Ariel development board; for the Macintosh, it requires a board from Spectral Innovations. $3000.

AT&T Microelectronics, Dept 52AL040420, 555 Union Blvd, Allentown, PA 18103. Phone (800) 372-2447; in Canada, (800) 553-2448. FAX (215) 778-4106. **INQUIRE DIRECT**

C/C++ Development System

- *For developing small, fast Windows programs*
- *Contains tools for Windows 3.1*

Microsoft's C/C++ version 7.0 Development System for Windows helps you develop small, fast applications programs for Windows. The system contains development tools for the latest Windows release, 3.1. Its Windows tool kit includes a Windows debug kernel, Windows set-up tools, a new version of the Code View debugger, a faster Programmer's Workbench, and the Qualitas 386MAX memory manager to ease memory constraints during development. The C/C++ compiler conforms to the AT&T 2.2 specification; it generates correct object code from even the most complex or obscure expressions. Users of previous versions of C and C++, including Microsoft C, Borland C++, Watcom C, and Zortech C++, can upgrade for a reduced fee. C/C++ 7.0, $499; upgrade (in US only), $139.

Microsoft Corp, 1 Microsoft Way, Redmond, WA 98052. Phone (206) 882-8080. **Circle No. 401**

"Live" Electronic Handbooks

- *Reference books on disk*
- *Formulas compute with your plugged-in values*

With these electronic handbooks now on disk and CD-ROM, you can display equations, formulas, and diagrams. More importantly, you can interactively use that information for your own computations. Reference equations and formulas are "live," reflecting any changes you make in them by computing new results, much like a spreadsheet program reflects the results of an altered cell. Three of the handbooks are electronic versions of popular references from McGraw-Hill and CRC: *Machine Design and Analysis*, *Standard Handbook of Engineering Calculations*, and *The CRC Materials Science and Engineering Handbook*. A fourth book, *The Mathcad Treasury*, comes from the software supplier. Equations in the handbooks work automatically with the supplier's Mathcad software. If, for example, you change a parameter in a sample computation, a new answer automatically appears. Even if you alter a formula, a new answer reflects the changed formula. You can also cut and paste portions of the electronic books into a separate document. Individual books, $99 to $149; CD-ROM set, $199.

Mathsoft Inc, 201 Broadway, Cambridge, MA 02139. Phone (617) 577-1017. **Circle No. 402**

CAE & Software Development Tools

Design simulator. The Apex Plus simulator for analog and mixed-mode circuits combines features of the Intergraph Integrated Simulator (ISIM) and the Dazix Apex simulator. It is available on workstations from Intergraph and Sun Microsystems. $15,000. **Dazix,** 1 Madison Industrial Park, Huntsville, AL 35894. Phone (205) 730-2000. FAX (205) 730-8344. **Circle No. 403**

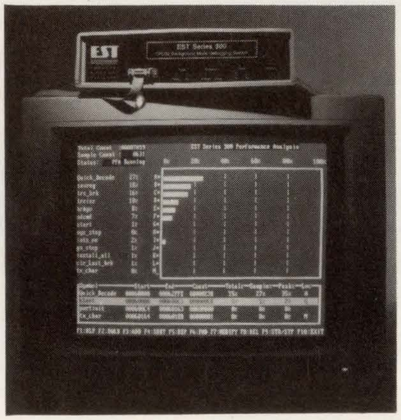
Software development kit. The C860 software development tool kit includes a DOS-based C cross-compiler that generates code for the 64-bit i860 μP. The kit also contains an assembler, a linker, utilities, and a source-level software debugger. $4000. **Intel Corp,** Literature Packet #BP45, Box 7641, Mt Prospect, IL 60056. In US and Canada, phone (800) 874-6835. **Circle No. 404**

Schematic editing utilities. SDT Utilities 1.0 provides automated schematic editing and annotation of OrCAD SDT schematics. An intersheet-reference feature marks schematics with source and destination sheet numbers for all off-sheet signals. The software runs on PCs. $99. **Robertson Engineering,** 3721 Arlen Ct, San Jose, CA 95132. Phone (408) 946-1200. **Circle No. 405**

Logic model generator. Spice2logic automatically generates ASIC cell functional models for simulation, synthesis, and timing-analysis tools. It currently produces Verilog, Synopsis, Ikos, Mentor, Viewlogic, and Orcad models, using an existing simulation environment, such as Verilog. $17,500. **Simquest,** 3235 Kifer Rd, Suite 300, Santa Clara, CA 95051. Phone (408) 739-7582. FAX (408) 738-2017. **Circle No. 406**

Disabled-employee software. Adapta-LAN provides helpful LAN features for disabled employees. With the software installed on a network, users have access to screen magnification, word prediction, visual beeps, and PC access via external switches. $2995. **Microsystems Software Inc,** 600 Worcester Rd, Framingham, MA 01701. Phone (508) 879-9000. FAX (508) 626-8515. **Circle No. 407**

CASE for OOA, OOD, and OOP. Objectmodeler is a CASE tool that aids in object-oriented analysis, object-oriented design, and object-oriented programming. It uses methods developed by Peter Coad, Ed Yourdon, and Grady Booch; it works with C++. $995. **Iconix Software Engineering Inc,** 2800 28th St, Suite 320, Santa Monica, CA 90405. Phone (310) 458-0092. **Circle No. 408**



Background-mode emulator. The Performance Plus Model of the EST Series 300 is a background-mode emulator for the Motorola 68332, 68331, 68340, and 68300. It provides software performance analysis through Motorola's background-mode debugging port. The emulator costs less than an in-circuit emulator and is less intrusive than a ROM monitor. $3050. **Embedded Support Tools Corp,** 10 Elmwood St, Canton, MA 02021. Phone (617) 828-5588. FAX (617) 828-7941. **Circle No. 409**

Data-acquisition tutorial. Direct View is a disk-based tutorial on I/O boards that simplifies learning about data acquisition. It covers transducer wiring, signal conditioning, board jumpers, A/D input ranges, interrupt levels, and more. Free. **Adac Corp,** 70 Tower Office Park, Woburn, MA 01801. Phone (617) 935-6668. FAX (617) 938-6553. **Circle No. 410**

Graphical-user-interface builder. User Interface Builder (UIB) for X-Windows-based C++ applications lets you develop graphical user interfaces (GUIs) that are dynamically switchable between OSF/Motif and Open Look. The software is tightly integrated with the supplier's C++ Object Interface library. Including library, $2995; binary, $995; source code, $25,000. **Solbourne Computer Inc,** 1900 Pike Rd, Longmont, CO 80501. Phone (303) 678-4626. FAX (303) 678-4716. **Circle No. 411**

Filter-synthesis software. A filter-synthesis option for the supplier's Design Center package synthesizes passive LC ladders. It lets you compute and evaluate inductor and capacitor values by selecting either minimum-inductor or maximum-capacitor configurations. A preference screen allows you to configure your filter synthesis for the kind of work you usually do. A Bode-plot menu lets you examine linearized phase and phase delay. $900. **Microsim Corp,** 20 Fairbanks, Irvine, CA 92718. Phone (800) 245-3022; (714) 770-3022. FAX (714) 455-0554. **Circle No. 412**

Project-management software for Windows 3.0. Project for Windows 3.0 incorporates the top 10 requests from users of earlier software. New features include a customizable tool bar; customizable views, menus, tables, and charts; and planning "wizards" that provide user help. The software also includes improved graphing and printing capabilities. $695. **Microsoft Corp,** 1 Microsoft Way, Richmond, WA 98052. Phone (206) 882-8080. FAX (206) 936-7329. TLX 160520. **Circle No. 413**

Schematic capture and simulation framework. Pads-View is an OEM version of Workview from Viewlogic. An integrated schematic capture and simulation framework, it lets you create discrete, partially integrated, and fully integrated designs and predict their performance. It comes in several versions with varying levels of capability. From $4000. **Pads Software Inc,** 119 Russell St, Suite 6, Littleton, MA 01460. Phone (508) 486-9521. FAX (508) 486-8217. **Circle No. 414**

Data-management software. Voice 2.0 (Virtual Office Information for Corporate Environments) is a document-management package that allows you to store, search, and retrieve data from optical disk. The software allows you to search files in their native formats. The software runs on PCs and comes with image-compression and print-accelerator plug-in boards. $9950. **Indus Mis Inc,** 340 S Oak St, West Salem, WI 54669. Phone (800) 843-9377; (608) 786-0300. FAX (608) 786-0786. **Circle No. 415**

68302 Model. The 68302 Smartmodel is a behavioral-level simulation model for Motorola's 68302 integrated multiprotocol processor. It enables hardware designers to develop, debug, and optimize the operation of 68302-based designs before committing to the time and expense of physical prototypes. Logic Automation requires you to purchase a Smartmodel licensing fee separately. Motorola 1-time fee, $4000. **Motorola Inc,** 6501 William Cannon Dr W, Austin, TX 78735. Phone (512) 891-3434. **Circle No. 416**

On-line math program help. Mathematica Help Stack documents the latest release of Wolfram Research's Mathematica software package. Its Macintosh Hypercard-based help stack categorizes and references all Mathematica commands. $99. **Variable Symbols Inc,** 2161 Shattuck Ave, Suite 202, Berkeley, CA 94704. Phone (510) 843-8701. FAX (510) 843-8702. **Circle No. 417**

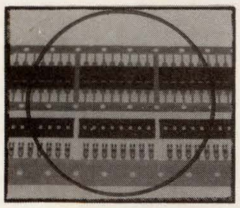
Software converter. Nth PortableGL allows application software developed on a Silicon Graphics workstation to run on any Sun SPARCstation. The software contains a graphics library that is call-string compatible with Silicon Graphics' IRIS GL version 4.0. $3600. **Nth Graphics,** 1908 Kramer Lane, Suite A, Austin, TX 78758. Phone (800) 624-7552; (512) 832-1944. FAX (512) 832-5954. **Circle No. 418**

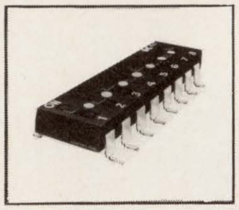
Analog-parts libraries. Analog Parts I and Analog Parts II are optional libraries for the supplier's Precise circuit simulator. Analog Parts I contains models from Device Modeling Technology; it covers 8500 devices from manufacturers in the US, Japan, and Europe. Analog Parts II contains models from Linear Technology, Burr-Brown, Motorola, and Texas Instruments. Parts I, $9500; Parts II, free. **Electrical Engineering Software Inc,** 4675 Stevens Creek Blvd, Suite 200, Santa Clara, CA 95051. Phone (408) 296-8151. FAX (408) 296-7563. TLX 171201. **Circle No. 419**

Character-Recognition API. The Scanworx application-program interface allows use of the supplier's Intelligent Character Recognition (ICR) software in applications. It includes the ICR software, documentation, and demonstration programs. $10,000 for 10 seats. **Xerox Imaging Systems Inc,** 9 Centennial Dr, Peabody, MA 01960. Phone (508) 977-2000. FAX (508) 977-5307. **Circle No. 420**

THE WORLD'S SMALLEST SURFACE MOUNT DIP SWITCH!

American Research & Engineering's strip molding process makes for a more reliable switch





It's More Reliable

Three simple components: two composite metal/plastic strips and one plastic molded cover replaces a 25 piece assembly to make a switch that's more reliable because it's more consistent.

SAME SIZE AS AN IC!

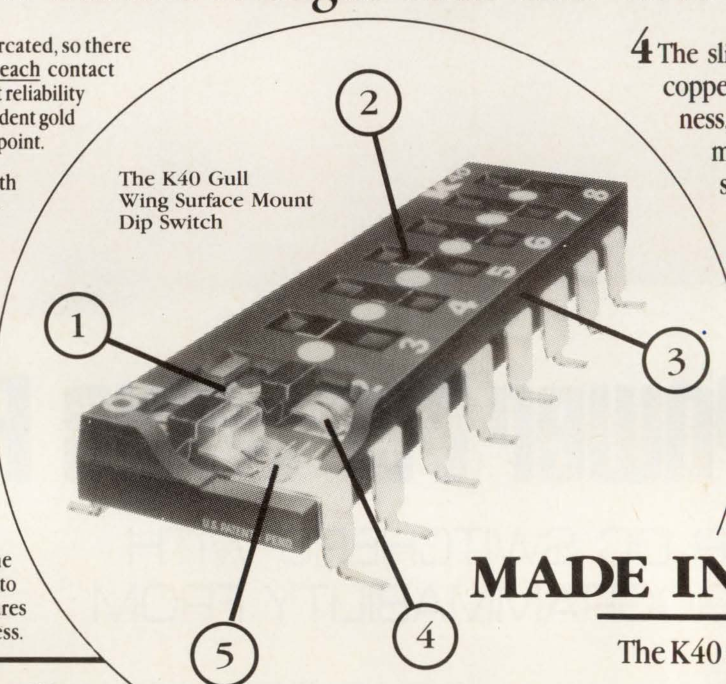
If you don't have automatic insertion equipment, we're banking that some day you will. In the meantime, your board will look neater, better and more professional. And if you have insertion equipment, you'll save the cost of hand insertion!

Three New Patent Designs That Use 40% Less Parts

1 The sides are split, or bifurcated, so there are two separate slides for each contact point. This doubles the contact reliability because you have two independent gold plated contacts at each switch point.

2 The switches are flush with the cover to eliminate accidental, on-off movement once the DIP is programmed. Simple.

3 The package is sealed. The lead frame is molded directly into the housing to provide a one piece, no leak construction. The cover is ultrasonically welded to the housing after the switch is assembled. There is no better construction. The surface mount housing is made of polyphenylene sulfide with a Kapton tape seal to withstand the high temperatures of the reflow soldering process.



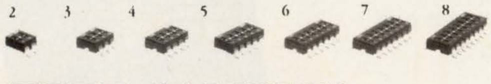
4 The slides are made from beryllium copper, heat tempered to a full hardness, spring formed, plated in a 100 micro inch nickel bath and then spot gold plated 30 micro inch deep at all the contact points. This is the best proven switch contact surface that money can buy.

5 Every one of the switch contact surfaces on the main lead frame are plated with 30 micro inch of gold over 100 micro inch of nickel.

MADE IN AMERICA

The K40 Surface Mount Dip Switches Are Provided On Tape and Reel per EIA Specifications or In Standard IC Tubes.

All K40 Dip Switches Are Available In Positions Two Thru Eight!



The K40 Standard Pin Dip Switch

The K40 standard pin DIP Switch was originally designed by American Research & Engineering in 1982 as the world's smallest DIP Switch. It was with its incredible small size and durability that the K40 standard pin DIP Switch led to the development of the new K40 Surface Mount DIP Switch lineup. Lead time for the K40 standard pin DIP Switch is seven to fourteen days and fourteen to twenty-one days for the K40 Gullwing DIP Switch. All K40 switches are manufactured at our plant in Elgin, Illinois.

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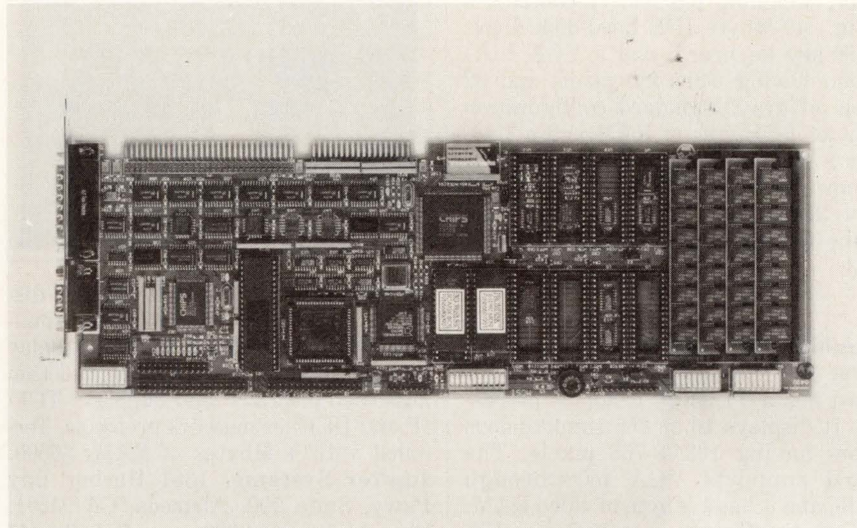
CIRCLE NO. 164

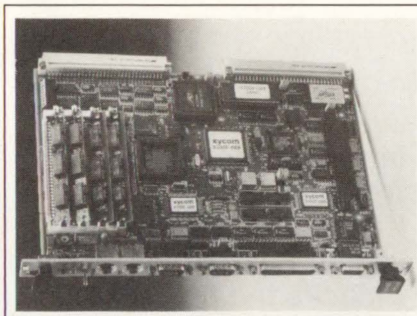
ISA Bus Single-Board Computer

- *Employs 25-MHz 80386SX μP*
- *A solid-state disk emulator simulates A, B, or C drives*



The IND-386SX single-board computer (SBC) for a passive ISA bus backplane uses a 25-MHz 80386SX μP and can optionally operate with the Chips and Technologies 38605SX Superstate μP. A 4-Mbyte solid-state disk emulator uses standard EPROMs, static RAMs, or flash EPROMs. The emulator simulates A, B, or C drives. The board can program flash EPROM in circuit. ROM space is available for user-defined bootup code and eight general-purpose switches let you specify field-selectable options. Standard features include two serial ports, a parallel port, dual floppy-disk ports, an IDE hard-disk port, a keyboard port, and as much as 16 Mbytes of dynamic RAM. A fully populated board consumes 6W. $895.

Micro Computer Specialists Inc, 2598-g Fortune Way, Vista, CA 92083. Phone (619) 598-2177. FAX (619) 598-2450. **Circle No. 442**



VMEbus Single-Board Computer

- *Employs a 25-MHz 80386sx μP*
- *Operates as a bus master and contains slot 1 functions*

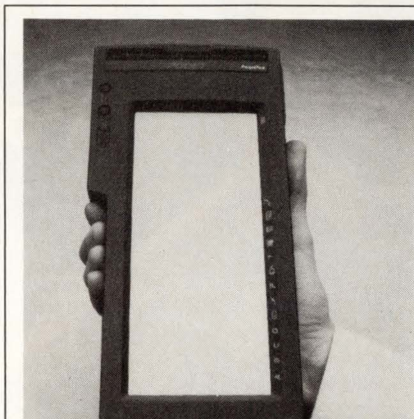
The XVME-688 VMEbus single-board computer features a 25-MHz 80386SX μP. It also has an 80387SX coprocessor socket, two serial ports, a parallel port, an IDE and floppy-disk-drive port, and a battery-backed time-of-day clock. The board contains 4 SIMM (single-in-line-memory-module) sockets to provide as much as 16 Mbytes of zero-wait-state dynamic RAM. A VGA graphics controller and 512 kbytes of video RAM provide 1024×768-pixel graphics. You can also connect the board to standard ISA bus peripheral boards such as Ethernet modules, modems, serial communications boards, and SCSI controllers. The board operates in temperatures from 0 to 65°C and noncondensing humidities from 0 to 95%. $1675; $1350 (OEM qty).

Xycom Inc, 750 N Maple Rd, Saline, MI 48176. Phone (800) 289-9266; (313) 429-4971. FAX (313) 429-1010. **Circle No. 443**

Pen Computer

- *Operates from 2 AA-size alkaline batteries*
- *7¼-in. display has 25 lines of 80 characters each*

The Poqetpad is a 1.2-lb, MS-DOS-compatible pen computer. It measures 9.65×4.59×1.26 in. and operates from 2 AA-size alkaline batteries. The handheld computer runs for a minimum of 16 hours on a pair of batteries. You can also power the unit from an optional ac adapter. The computer has a V20HL μP and 640 kbytes of RAM. A 1-Mbyte ROM stores the operating system, pen-support and handwriting-recognition software, and utilities. Its



two drives can accommodate two memory cards having as much as 4 Mbytes each. A 7¼-in. diagonal display has 25 lines of 80 characters each. $1995.

Poqet Computer Corp, 5200 Patrick Henry Dr, Santa Clara, CA 95054. Phone (408) 982-9500. FAX (408) 496-0575. **Circle No. 444**

Notebook computer. The DLT-2000 is a 20-MHz 80386SX notebook computer, weighing 6.8 lbs. It contains a 3½-in., 40-Mbyte IDE hard-disk drive; an 80-key keyboard; and a VGA LCD screen having 640×480 pixels and 32 levels of gray. Standard configuration includes 2 Mbytes of RAM and a 1.44-Mbyte floppy-disk drive. $6295. **DTK Computer Inc**, 17700 Castleton St, Suite 300, City of Industry, CA 91748. Phone (818) 810-8880. FAX (818) 810-5233. **Circle No. 445**

Graphics controller board. The Winsprint 200 ISA bus graphics controller board has a TI 34020 graphics processor. It displays 16 or 256 simultaneous colors having 1024×768 pixels. The board supports VGA passthrough mode, and it has 1 Mbyte of video RAM. $995. **Artist Graphics**, 2675 Patton Rd, St Paul, MN 55113. Phone (800) 627-8478; (612) 631-7800. **Circle No. 446**

Color X terminal. The MX600 Network Display Station supports from one to six 1280×1024-pixel displays. A single mouse and keyboard control all displays. A virtual screen mode treats multiple displays as a single large display surface. The unit has a thick and thin Ethernet interface and supports TCP/IP and DECnet network protocols. Terminal with 4 Mbytes of RAM, $6500. **Jupiter Systems**, 1351 Harbor Bay Pkwy, Suite 200, Alameda, CA 94501. Phone (510) 523-9000. **Circle No. 447**

Transparent intercrate link. The MB2-Mlink-II provides bidirectional DMA channels between two Multibus II crates. Dual DMA controllers and FIFO buffers transfer data over a cable at 10 Mbytes/sec. To send a message from one crate to another you provide an extra byte in the endpoint address to select the destination board. Link consisting of two boards and cable, $6995. **General Standards Corp**, 8302A Whitesburg Dr, Huntsville, AL 35802. Phone (205) 880-8787. FAX (205) 880-8788. **Circle No. 448**

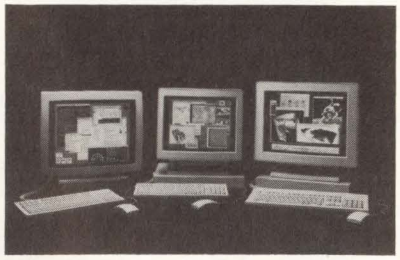
PWM motor driver. The PDH-X1 is a PWM servo-motor driver. The 5.2×4.8-in. stand-alone board's dc-dc converter has an 85-kHz switching rate that yields a dc to 20-kHz power bandwidth. The board delivers 5A continuous at 60V dc and 10A pk. $199 (OEM qty). **Western Servo Design Inc**, 44366 S Grimmer Blvd, Fremont, CA 94538. Phone (510) 266-6255. **Circle No. 449**

Color-graphics board. The Multiview 24 graphics board for the ISA bus produces 16.8 million colors. It provides 1024×768-pixel noninterlaced resolution and refresh rates as fast as 75 Hz. The board features a VGA passthrough mode and supports 8514/A-compatible

DOS software as well as Windows application software. $1999. **Radius Inc,** 1710 Fortune Dr, San Jose, CA 95131. Phone (408) 434-1010. **Circle No. 450**

Next computer ISDN interface. The ISDN (Integrated Services Digital Network) Extender provides Basic Rate access and an analog telephone connection for Next computers. It has an 8-pin modular connector for the ISDN Basic Rate line and a 6-pin modular RJ11 for the telephone line. The unit runs with application software for the Nextstep Release 3.0 operating system. The stand-alone unit measures 3×5×1 in. and weighs 6 oz. $349. **Hayes Microcomputer Products Inc,** Box 105203, Atlanta, GA 30348. Phone (404) 840-9200. FAX (404) 441-1238. **Circle No. 451**

Notebook computer. The NB2500 contains a 25-MHz 80386SXL and a SCSI port for connecting six external peripherals. A built-in battery provides more than 3 hours of operation, and an indicator bar visually displays the battery life. Other features include 4 Mbytes of RAM, a 1.44-Mbyte floppy-disk drive, and an LCD VGA screen. Unit with 40-Mbyte hard-disk drive, $1995. **Bi-Link Computer Inc,** 11606 E Washington Blvd, Whittier, CA 90606. Phone (310) 692-5345. **Circle No. 452**



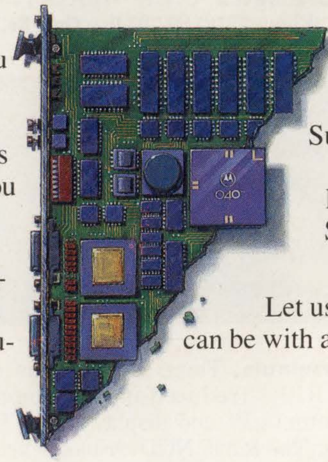
X terminals. Three X terminals employ RISC (reduced-instruction-set-computer) μPs and display 1280×1024 pixels. The $2895 NCD19r monochrome unit uses a Mips R3000 μP. The $5395 NCD17cr color unit uses Motorola's 88100 μP. The $4495 NCD19g gray-scale unit also uses the 88100 μP. Delivery, 60 days ARO. **Network Computing Devices Inc,** 350 N Bernardo Ave, Mountain View, CA 94043. Phone (415) 694-0650. **Circle No. 453**

Bubble-jet copier. The CJ10 desktop color copier uses bubble-jet technology. It produces 400-dpi resolution and 256 colors. Other features include an 8½×11-in. scanning area, a 90-sec copy or print speed, and a 90-sheet cassette paper feeder. You can scale prints from 50 to 200% in 1% increments. Less than $10,000. **Canon USA Inc,** 1 Canon Plaza, Lake Success, NY 11042. Phone (516) 488-6700. **Circle No. 454**

DSP interface board. An ISA bus interface board connects Data Translation's DT-Connect I/O products to Spectrum Signal Processing's DSP boards. It provides a path and a FIFO buffer between a DT-Connect port and Spectrum's DSP-Link interface. $800. **Quantawave,** 530 Boston Post Rd E, Marlborough, MA 01752. Phone (508) 481-9802. FAX (508) 624-0942. **Circle No. 455**

68040 VMEbus SBC. The MZ 8140 VMEbus SBC (single-board computer) contains a 25-MHz MC68040 μP. It provides as much as 4 Mbytes of dynamic

Why Settle for ½ an '040 Board?



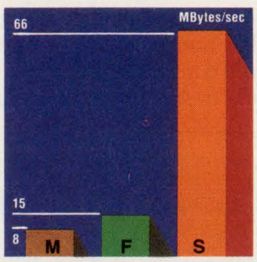
You've chosen the '040 because you need maximum performance in your VME system. But look carefully, because other Single Board Computers may only give you only half of what you expected from the '040.

Compare Synergy's SV430 performance to any other SBC. Compare bus speed, MIPs, support, flexibility, documentation, reliability, I/O intelligence or any spec you can think of. We think you'll find the same thing we did—the SV430 outperforms every other SBC on the market by as much as 150%.

Surprisingly, this kind of quality won't cost you any extra, because Synergy products lead in another important area—value. At Synergy, you don't have to pay a premium price for premium performance.

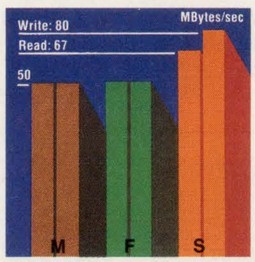
Let us show you just how far ahead your system can be with a Synergy processor board. Call us today, and get the *whole* '040 story.

Compare our specs. Synergy is superior across the board!



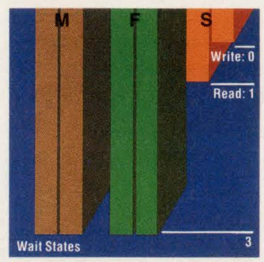
VME Transfers

VME64 doubles bus performance to 66 MB/s—and the SV430 is the only '040 board that has it. But we don't need VME64 to win this comparison. Even normal 32-bit transfers race at 33 MB/s. That's 200% faster than Force or Motorola.



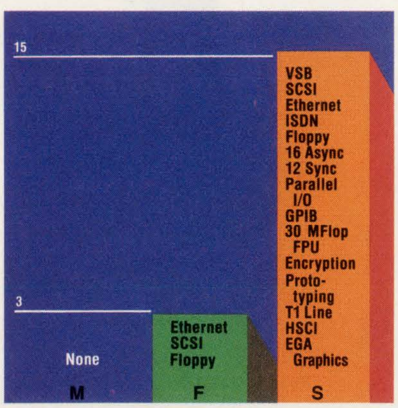
DRAM Burst Rates

A 25 MHz '040 is capable of accessing memory at 80 MB/s. The closer you are to this maximum, the more '040 performance you're gaining. SV430 bursts are 26% faster than Force and Motorola.



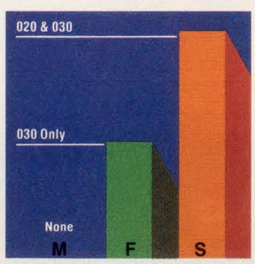
DRAM Random Accesses

Non-burst '040 performance is measured in wait states. Fewer wait states mean higher performance. The SV430 is not only 66% faster than Force or Motorola, it supports twice the on-board memory—32 MB.



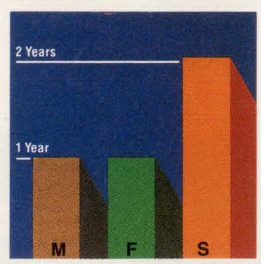
I/O Modules

Synergy's EZ-Bus modules are compatible with our entire line of SBCs. This means Synergy's current line of 12 intelligent I/O modules are immediately available for the SV430—today. No other vendor comes close for selection, functionality or availability.



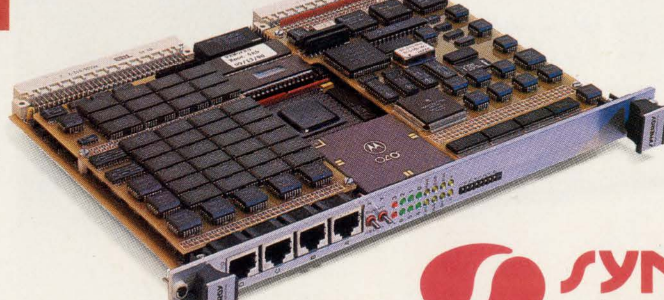
'020/'030 Compatibility

Software compatibility between Synergy SBCs means users have simple upgrades to the SV430 from our '020 and '030 SBCs. Force offers compatibility only from the '030 level, and Motorola offers "upward migration"—a polite phrase that means rewriting your code.



Product Warranty

Synergy backs the reliability of its SBCs with a two year standard warranty. Force and Motorola only offer you one.



Data from Motorola MVME165 data sheet dated 2/90, and Force CPU-40 data sheet A1 Rev. 1. DRAM measurements shown are with parity. VMEbus transfers are to a 60ns slave.

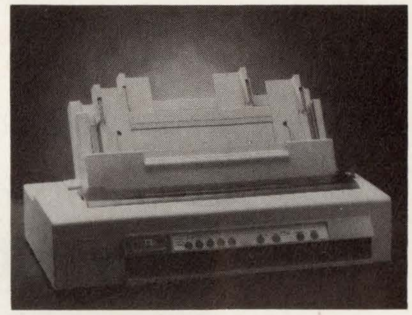
VME64 is a trademark of Performance Technologies, Inc.

SYNERGY microsystems

Synergy Microsystems, Inc., 179 Calle Magdalena, Encinitas, CA 92024 **(619) 753-2191** FAX: 619-753-0903

CIRCLE NO. 166

RAM (DRAM), two serial ports, as much as 1 Mbyte of EPROM, 2 kbytes of battery-backed static RAM, two timers, and a battery-backed real-time clock. The SBC includes the company's MXbus for I/O expansion. Board with 1 Mbyte of DRAM, $2995. **Mizar Inc,** 1419 Dunn Dr, Carrollton, TX 75006. Phone (800) 635-0200; (214) 446-2664. FAX (214) 242-5997. **Circle No. 456**



Bubblejet printer. The JR-670 CAD printer uses Canon's 360-dpi Bubblejet print engine. Dual-bin automatic sheet feeders accept A- through C-size paper. The printer handles HP-GL, CalComp 906/907, AutoCAD, and Epson LQ1050 print formats. Automatic head capping and cleaning facilities reduce maintenance time. $1995. **JRL Systems Inc,** 8305 Hwy 71 W, Austin, TX 78735. Phone (512) 288-6750. FAX (512) 288-7676. **Circle No. 457**

VGA color monitor. The HCM-433E 14-in. monitor is compatible with VGA, Super VGA, and IBM's 8514A standard. Its noninterlaced screen displays 640×480, 800×600, or 1024×768 pixels. The monitor features a 70-MHz video bandwidth, RGB analog video inputs, a 0.28-mm dot pitch, and a 56- to 86-Hz vertical scan rate. $649. **Hyundai Electronics America,** 166 Baypointe Pkwy, San Jose, CA 95134. Phone (408) 473-9200. FAX (408) 943-9567; (408) 943-9568. **Circle No. 458**

Removable hard-disk drives. The Mercury series is a line of half-height, internal and external removable hard-disk drives. Capacity ranges from 52 Mbytes to 1 Gbyte, and average access times range from 9 to 12 msec. The drives incorporate shock-mount isolators that can withstand a 300g impact. $1129 to $6559. **Mega Drive Systems Inc,** 489 S Robertson Blvd, Beverly Hills, CA 90211. Phone (310) 247-0006. FAX (310) 247-1667. **Circle No. 459**

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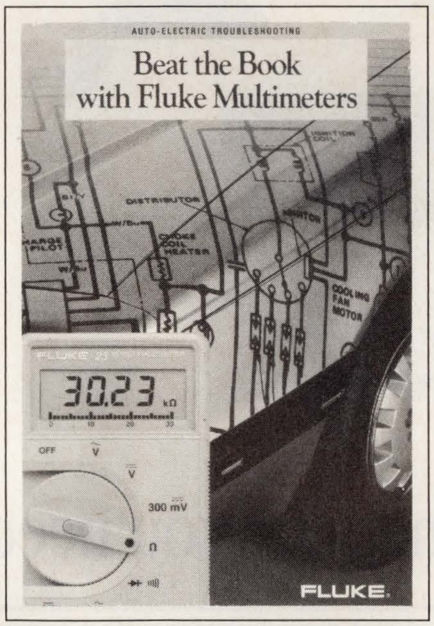
Phone:(708) 299-9311 FAX:(708) 635-1571. A1

Brochures on software development tools and ICEs. The 8-pg brochure on 8086, 80C186, and 80C286 software development tools presents a product overview, a feature list, and highlights and benefits of these tools. Illustrations and ordering information complete the publication. The 4-pg brochure deals with -186 and -188 ICEs (in-circuit emulators), providing an overview, product features and highlights, physical descriptions and characteristics, specifications, and ordering information. **Intel Corp,** 3065 Bowers Ave, Santa Clara, CA 95051. Phone in Canada and US (800) 548-4725; US only (800) 874-6835; (503) 681-8080.
Circle No. 351

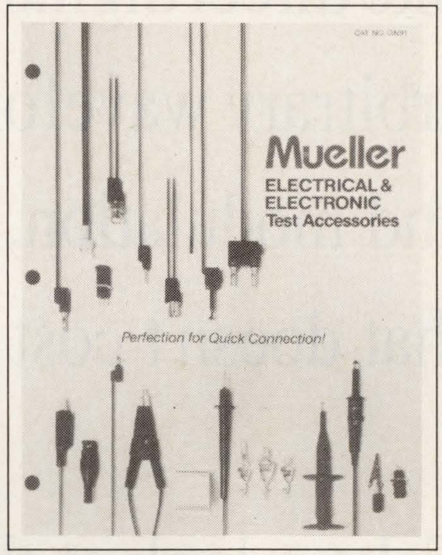


Diagnosing electrical problems in autos. *Beat the Book with Fluke Multimeters* is an application note on automotive electrical troubleshooting. It describes and illustrates time-saving procedures for servicing electrical systems safely, accurately, and cost effectively. The 16-page booklet presents four products, comprising two Series II meters, a DMM, and a digital thermometer. In addition to DMM pointers, the publication provides sections on automotive electrical diagnosis; charging, starting, ignition, and cooling systems; current drains and short circuits; and computer sensors. **John Fluke Mfg Co Inc,** Box 9090, Everett, WA 98206. Phone (800) 873-5853; (206) 347-6100. FAX (206) 356-5116. TLX 185102.
Circle No. 352

Modular-bus-system devices. The 1992 catalog features the modular A-Bus system of data-acquisition and control devices, including 86 boards, adapters, and accessories. It also describes a line of PCs for the data-acquisition and control devices, 15 software products, and several motion-control devices, including a robot arm. The theme of the 32-pg, 4-color publication is the Voyager flight past Jupiter, Saturn, Neptune, and other interplanetary bodies in the solar system. It includes several NASA photos of the Voyager journey. The catalog highlights the introduction of 28 networking, IEEE, and other protocol conversions, high-capacity I/O, A/D, and D/A boards, sensors, and other data-acquisition and control products. In addition to Odin, a proprietary A-Bus software system, the booklet lists software systems such as Omnipotence ECS for data-acquisition and control systems. **Alpha Products Co,** 303 Linwood Ave, Fairfield, CT 06430. Phone (203) 259-7713.
Circle No. 353

Directory of computer programs. The US Government Source-Code Directory lists more than 10,000 computer programs from the US government, universities, and companies such as IBM, Digital Equipment Corp, and AT&T. It comes in printed form or on an MS-DOS disk and catalogs design tools and engineering software. Directory sections include electronics, CAD/CAM, VHDL (VHSIC Hardware Description Language) models, signal processing, communications, databases, user interfaces, simulation, laboratory information systems, expert systems, mathematical analysis, and neural networks. $149 (printed or disk); $249 (both), plus $7.50 for handling. **Source Translation & Optimization,** Box 404, Belmont, MA 02178. Phone (617) 489-3727.
Circle No. 354

Monograph on active devices for engineering. The title of the initial publication in the AACE Monograph Series is *Active Devices for Engineering Applications.* Its purpose is to "give engineers . . . an organized way . . . to understand existing active devices and to design circuits that function with them with a minimum of tailoring and adjustment." This paper provides an approach to the design and analysis of active circuits that applies to presently available 2-port (typically 3- or 4-terminal) active devices. It develops several new techniques that extend the capabilities for the design of circuits, including high-power transmitting tubes. $11 (includes postage and handling). For sample page, send self-addressed, stamped business-size envelope. **AACE Inc,** Maryland Office, 2807 Jerusalem Rd, Kingsville, MD 21087.
INQUIRE DIRECT



Test accessories cataloged. The 44-pg catalog presents a line of electrical- and electronic-connection test accessories, covering more than 200 products. It describes test leads, BNC and banana plug leads, instrument/test interconnections, plunger clips, probes, alligator clips, insulators, and Kelvin clips. The catalog also discusses assembly tool kits and probe kits for oscilloscopes. **Mueller Electric Co,** 1583 E 31st St, Cleveland, OH 44114. Phone (216) 771-5225. FAX (216) 771-3068.
Circle No. 355

Dynamic specifications for data converters. Application Note AN-3 explains the dynamic specifications of data converters. It discusses how sampling ADCs and flash ADCs allow manufacturers to guarantee dynamic performance. The note reviews relevant A/D architectures and deals with dynamic frequency-domain specifications, including S/N ratio, THD, and effective bits. The 6-pg publication also explains the significance of the input bandwidth specification. **Datel Inc,** 11 Cabot Blvd, Mansfield, MA 02048. Phone (508) 339-3000. FAX (508) 339-6356.
Circle No. 356

Application note for subranging ADCs. Application note AN-5 covers the architecture, design, parameters, and testing of subranging ADCs. Part 1 of the app note describes the design considerations and problems of subranging ADCs. Part 2 deals with specifications, such as S/N ratio, total

Looking for a function generator

with all the bells and whistles,

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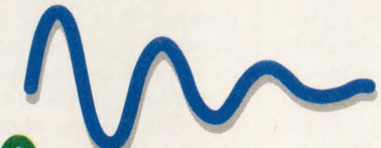
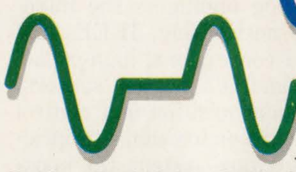


and modulation,



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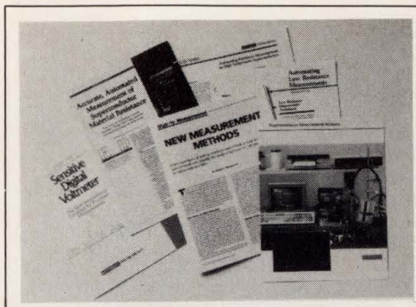
harmonic distortion, and differential phase and gain. Part 3 provides some classical data-converter tests. **Datel Inc,** 11 Cabot Blvd, Mansfield, MA 02048. Phone (508) 339-3000. FAX (508) 339-6356. **Circle No. 357**



Package on superconductivity research. This package of technical literature contains several articles, such as "Automating Resistance Measurements on High Temperature Superconductors." This article speaks about appropriate resistance-measurement techniques, system configuration, system noise control, software (including a listing of a superconductor resistance test driver), and techniques for measuring resistivity. "Automating Low Resistance Measurements" identifies the differences between normal range and low-level-resistance measurement. It includes tips on automating test procedures as well as schematics and electrical connection diagrams for system setups and sample test-program listings. The package also features three high-temperature superconductor measurement and test systems that use the vendor's nanovoltmeters, current sources, scanners, scanner cards, and micro-ohmmeters. **Keithley Instruments Inc,** 28775 Aurora Rd, Cleveland, OH 44139. Phone (800) 552-5115; (216) 248-0400. FAX (216) 248-6168. **Circle No. 358**

Brochure of data-delivery systems. This 12-pg brochure focuses on the vendor's data-delivery systems. It explains the content and operation of Data Destination, Data Hub, and Data Origin and related subjects. **Burr-Brown Corp,** Box 11400, Tucson, AZ 85734. Phone (602) 746-1111. FAX (602) 741-4245. TLX 066-6491. **Circle No. 359**

Technical journal. *News from Rohde & Schwarz,* Vol 31, No. 135 highlights the PSA 17 process controller, the TS 9955 test system for surveying digital radio-telephone and data networks, the GSM radio-communications test set CRTS 04 for testing base stations, the SMGL power-signal generator, and crisis-proof communications by shortwave. Application notes deal with television technology and ARB synthesis for the AMS arbitrary-waveform generator and the ADS dual arbitrary-waveform generator. Brief items describe the URV 35 level meter for service and design engineers, the ESVD test receiver for digital mobile radio networks, and the ZPM enhanced network system. Regular features are Booktalk, R&S software, R&S test hint, R&S reference, Newsgrams, Press comments, and Information in print. The final article reports on modular avionics systems. **Rohde & Schwarz,** Mühldorfstr 15, 8000 Munich, Germany. Phone (089) 4129-2625. FAX (089) 4129-3208. TLX 52370320. **Circle No. 360**

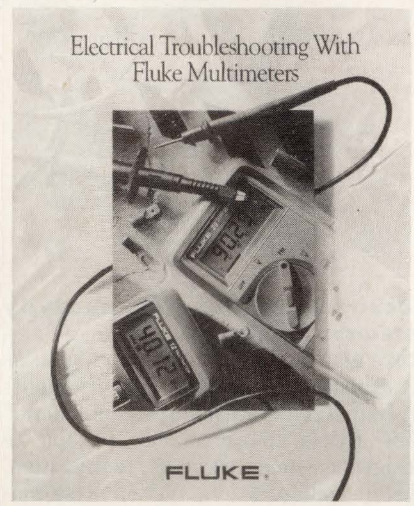
Data sheet for power-monitoring device. The 2-pg data sheet describes how the 8800 Powerscope power analyzer speeds power-disturbance monitoring. It explains how the analyzer helps engineers find the causes of power disturbances that affect CAD systems and automatic test equipment. **Basic Measuring Instruments,** 335 Lakeside Dr, Foster City, CA 94404. Phone (415) 570-5355. FAX (415) 574-2176. TWX 910-374-3059. **Circle No. 361**

Multichannel recorder presented. This 12-pg, 4-color brochure presents an 8- to 32-channel recorder. It describes features such as 64 event and 34 annotation channels, a built-in monitor, signal conditioning, and chart speeds as high as 500 mm/sec. Illustrations cover full-size chart samples, such as custom chart formats. **Astro-Med Inc,** Astro-Med Industrial Park, West Warwick, RI 02893. Phone (800) 343-4039; (401) 828-4000. **Circle No. 362**

Foldout for cartridge-tape subsystem. This 6-pg brochure presents the RSP-2150 tape-backup system. It provides a product overview and highlights features such as capacity, reliability, access time, and maintainability. Listings of product specifications complete the publication. **Metrum Information Storage,** Box 5227, MS 262, Denver, CO 80217. Phone (800) 638-7862; (303) 773-4574. **Circle No. 363**

Toroidal-power-transformer booklet. This 8-pg booklet deals with toroidal transformers. It describes the features of toroids and provides electrical and mechanical data for each product. Also featured are a guide on how to specify your own custom design and application notes for several rectifiers. **Powertronix Corp,** 703 Cayman Lane, Foster City, CA 94404. Phone (415) 345-6800. FAX (415) 345-7240. **Circle No. 364**

Handbook of data-acquisition and related products. The 260-pg *1992 Product Handbook* presents the company's line of data-acquisition, image-processing, chromatography, and line-scan products for IBM PCs and compatible computers, IBM PS/2, Macintosh II, VMEbus, MicroVAX, and the iSBX Bus. It updates product information and features new products, including the DT-Connect II Open Bus Interface standard and open-software architecture, DT-Open Layers for Microsoft Windows. The publication also describes Windows Dynamic Link Libraries, Global Lab Image Processing Library, and Global Lab Data Acquisition Library. The catalog covers more than 300 boards, software packages, modules, and accessories. **Data Translation,** 100 Locke Dr, Marlborough, MA 01752. Phone (508) 481-3700. FAX (508) 481-8620. TLX 951646. **Circle No. 365**



Booklet of multimeters. The 20-pg booklet, *Electrical Troubleshooting With Fluke Multimeters,* discusses several techniques for troubleshooting electrical systems. It contains sections on DMM safety and protection, basic electrical measurements, troubleshooting with the MIN MAX recording mode, power measurements and power factor, wiring and grounding, engine-driven generators, and motors and harmonics. **John Fluke Mfg Co Inc,** Box 9090, Everett, WA 98206. Phone (800) 873-5853; (206) 347-6100. FAX (206) 356-5116. TLX 185102. **Circle No. 366**

Guide to radiometry. *The Guide to Radiometry* explains how to measure ultraviolet, visible, and near-infrared spectral regions. The publication explains specialized accessories, including integrating spheres, optical attenuators, custom optical filters, and quantum-efficiency reference standards. The product section provides specifications and spectral response curves for germanium and silicon sensor heads and highlights the vendor's optical power and energy meters. A how-to page helps you select a suitable radiometer system. **Graseby Optronics,** 12151 Research Pkwy, Orlando, FL 32826. Phone (407) 282-1408. FAX (407) 273-9046. **Circle No. 367**

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Circle # 100

AMD 29K, RISC DESIGN CONTEST BROCHURE

AMD and Embedded Systems Programming magazine are sponsoring a 29K RISC microprocessor design contest. Show off your hardware or software design talents and you could win a free trip for two to Hawaii! Find out why Apple, Hewlett-Packard, Tektronix and Samsung power their embedded RISC designs using the 29K Family

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Free 130-page engineering catalog contains descriptions and technical data on IEC connectors, battery holders, RFI/EMI filters and internationally approved power cords. All components are available for off-the-shelf delivery from stock, and are detailed with specifications, ratings and engineering diagrams. All Power Dynamics products carry full worldwide safety agency approvals.

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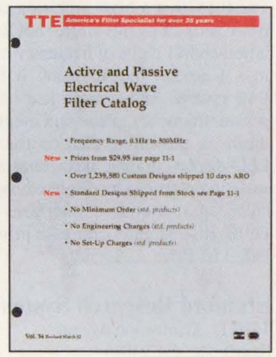
1,239,580 LC FILTERS

TTE's revised catalog, V34R, features a new section of stock filters. This standard series of filters is priced from $29.95 each, qty 1-9 stock delivery. The balance of the catalog contains information on Anti-Aliasing, Bessel, Butterworth, Chebyshev, Elliptical and custom designs all operating within the 0.1Hz to 500MHz range. General specs, attenuation curves, case drawings and mounting dimensions.



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Prem's new, full-line, 24-page catalog features domestic and international printed circuit power transformers, telecommunication magnetics, CRT products, and inductors for use in switch-mode power supply applications. Power transformers carry UL and CSA listings. International series includes UL, IEC, VDE, CSA and GOST approvals. Catalog includes cross reference chart to competitor's part numbers.

Prem Magnetics, Incorporated
3521 N. Chapel Hill Rd.
McHenry, IL 60050
815-385-2700 FAX:815-385-8578

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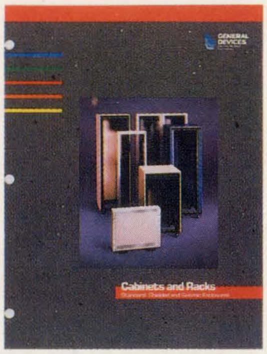
CABINETS AND RACKS



General Devices' 54-page Cabinets and Racks catalog features standard, shielded and seismic Vent Rak® cabinets for commercial and military applications. Knock-down racks and cabinets are also available. Components can be easily modified with low or very high level EMI/RFI shielding, seismic structural reinforcements, special airflow provisions, and custom panel openings/widths or cabinet depths.

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Power-One's new Reference Guide contains product information, corporate background and capabilities, application guide and a glossary of terms. Over 200 standards, switchmode and linear AC to DC power supplies available direct from Power-One or authorized distributors. Models are offered with outputs ranging from 2V to 250V, up to 2,000 watts. Single and multiple output models, all are design to meet UL, CSA, IEC, and VDE specs. Custom designs available.

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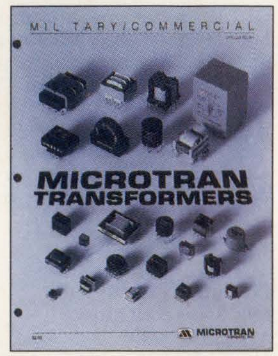

New 32-page catalog features audio, telecommunications, SMPS, DC-DC converter, power transformers and inductors in miniaturized, commercial, and MIL construction. Included are new Surface Mount FCC Part 68 coupling and UL, CSA, VDE, IEC certified split bobbin, flat profile, and international series of PC power and SMPS power transformers and inductors. Charts, schematics, outline drawings, and pricing are provided. Items are available off the shelf from distributors.

Microtran Co., Inc.
P.O. Box 236, Valley Stream, NY 11582
516-561-6050 FAX: 516-561-1117

Circle # 109

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The SR620 is a high precision counter / timer with 25 ps rms single-shot time resolution and 11 digits of frequency resolution in a 1 second measurement. It measures time interval, pulse width rise / fall time, period, frequency, phase and events. In addition to presenting data on the 16 digit LED display, graphic histograms and time variation plots can be displayed on X-Y oscilloscopes. Standard interfaces include GPIB, RS-232 and Centronics printer port.
U.S. List Price $4,500

Stanford Research Systems
1290 D. Reamwood Avenue
Sunnyvale, CA 94089
408-744-9040

Circle # 110

FRUGAL FRAME ENCLOSURE LINE

This new 20-page 4-color catalog features AMCO's Frugal Frame line of vertical consoles, reflecting a balance of quality and economy. Features include cost reduction by making cowlings an integral part of structure, new "deep texture" finish, new shadow box design effect, and acceptance of most AMCO standard accessories. Vertical panel openings are available in 21" to 78" heights, 19" wide, 25.5" and 30" depths.

AMCO Engineering Co.
3801 N. Rose, St.,
Schiller, IL 60176
800-833-3156. In IL 708-671-6670

Circle # 111

DS345 SYNTHESIZED FUNCTION GENERATOR

The DS345 offers digitally synthesized waveforms to 30 MHz with 1 μHz resolution. Outputs can be simple sine, triangle, ramp or square waves. Complex arbitrary signals with up to 16,300 points and sampling times to 25 ns can also be generated. Internally synthesized modulation capabilities include phase continuous linear and logarithmic frequency sweeps as well as amplitude, frequency, phase and burst modulation. Optional GPIB (IEEE-488)and RS-232 interfaces are available.

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E(E)PROM PROGRAMMERS

Reliable, fast and easy to use, Needham's Electronics E(E)Prom programmers are available in PC based or stand-alone models. Supporting 2716-4Megabit devices, Needham's programmers are capable of support for the latest in EPROM technology. Whether your needs are development or production, Needham's Rlectronics offers an affordable model to meet your programming requirements. All models are made in the USA by Needham's Electronics

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Circle # 113

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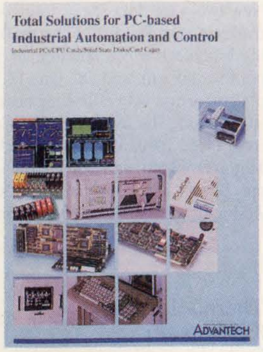
20-page, solution oriented reference guide detailing a complete line of PC-based industrial automation and control products: industrial PCs, 486/386/286 CPU Cards, RAM/ROM disks, rack mount keyboards and monitor enclosures. All of the latest technology at budget-conscious prices. Call for FREE reference guide:



American Advantech
1310 Tully Road, Suite 115
San Jose, CA 95122
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NEW IEEE-488 HARDWARE AND SOFTWARE

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Capital Equipment Corp.
Burlington, MA 01803
Literature: 800-234-4232,
Tech Support: 617-273-1818
FAX: 617-273-9057

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- Call progress tone receivers and transmitters
- MF trunk receivers and transmitters
- Key system/PBX enhancements
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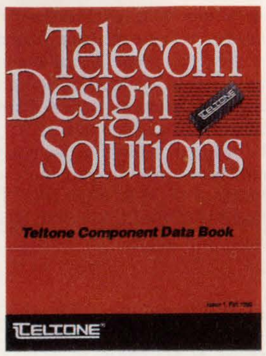

Teltone Corporation
22121-20th Avenue SE
Bothell, WA 98021-4408
800-426-3926 FAX: 206-487-2288

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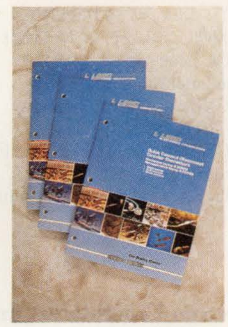
LEMO'S NEW CIRCULAR CONNECTOR CATALOG

LEMO's new circular connector catalog highlights expanded shell and insert designs. Insert configurations are available in single, multi or mixed designs including signal, coaxial, triaxial, high voltage, fiber optic and fluidic/pneumatic. Shell styles are available in standard chrome plated brass, anodized aluminum or stainless steel.



Lemo USA Inc
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Santa Rosa, CA 95406
800-444-LEMO; FAX: 707-578-0869

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SMS 60W MODULAR HV POWER SUPPLY

New 60W up to 60kV in a compact, lightweight 9″ × 5″ × 3″ module. Spellman's SMS series high voltage power supply provides 0.01% regulation, and 0.1% peak to peak ripple. The SMS is based on a resonant flyback circuit that provides over 75% efficiency and fast dynamic response. Units are available from 1KV to 60KV. Input is 28 V dc. Applications include X-ray, electron beam systems, Capillary Electrophoresis and OEM systems.

Spellman High Voltage Electronics Corp.
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516-349-8686 FAX: 349-8699

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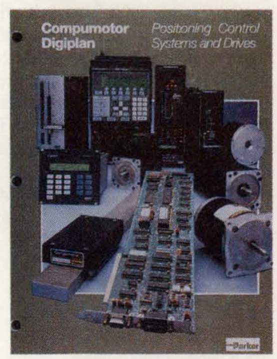
PROGRAMMABLE POSITION CONTROL

A complete 416 page engineer's guide with specifications, dimensions and performance data presents brushless servos, microstepping motor systems, indexers, linear motors and absolute encoders.



Hannifin Corporation, Compumotor Division
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Rohnert Park, CA 94928
800-358-9070 FAX: 707-584-8015

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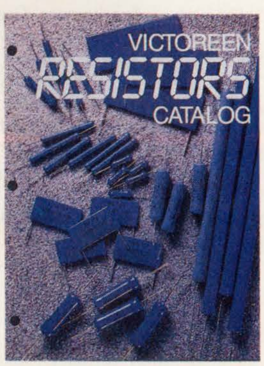

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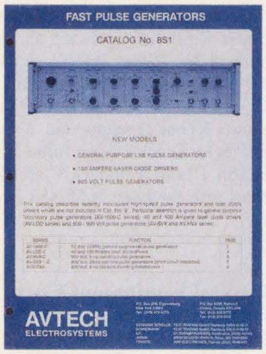
This new 8 page Catalog No. 8S1 describes recently introduced high-speed pulse generators and laser diode drivers which are not included in the 113 page General Cat. No. 8. Particular attention is given to general purpose laboratory pulse generators (AV-1000-C series), 40 and 100 Ampere laser diode drivers (AV-LDD series) and 800-900 Volt pulse generators (AV-SVX and AV-HVX series).



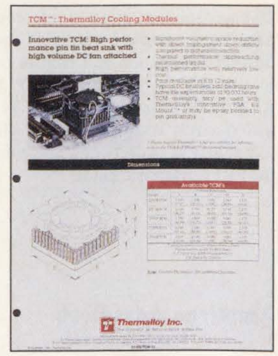
AVTECH ELECTROSYSTEMS LTD.

P.O. Box 5120 STN. F
Ottawa, Canada K2C 3H4
613-226-5772, FAX: 613-226-2802

Circle # 122

NEW PGA COOLING INNOVATION

New two-page data sheet describes Thermalloy s new TCM's™ (Thermalloy Cooling Modules), a combination of patented pin fin heat sink and DC fan. TCM's cool pin grid arrays with efficiency near recirculated liquid. The five standard TCM's cool Intel i486, i860, i960, AMD AM29000, Motorola 68040, and other PGA's. TCM's may be attached with Thermalloy's PGA E-Z Mount™ assembly or epoxy bonded.



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P.O. Box 810839,
Dallas, TX 75381-0839
214-243-4321 FAX: 214-241-4656

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NEW 1992 CRYSTAL OSCILLATOR CATALOG

- TTL clock osc. to 100 MHz
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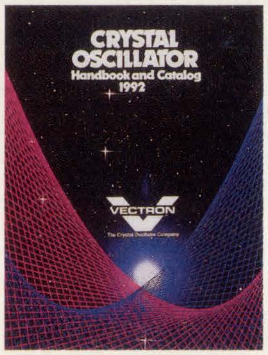


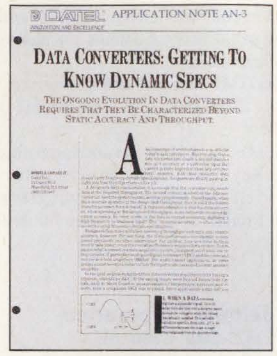
Vectron Laboratories, Inc.

166 Glover Avenue P.O. Box 5160
Norwalk, CT 06856-5160
203-853-4433 FAX: 203-849-1423

Circle # 124

A/D DYNAMIC SPECS

Application Note AN-3 reviews A/D architectures before explaining frequency domain specifications. Signal-to-noise ratio, total harmonic distortion, effective bits, and input bandwidth are discussed. Calculations for maximum frequencies that can be digitized or where harmonics will alias are shown in a six-page note entitled, "DATA CONVERTERS: GETTING TO KNOW DYNAMIC SPECIFICATIONS."



Datel, Inc.

11 Cabot Blvd.
Mansfield, MA 02048
508-339-3000, FAX: 508-339-6356

Circle # 125

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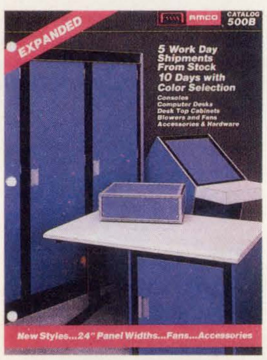


AMCO Engineering Co.

3801 N. Rose Street, Schiller Park, IL 60176
708-671-6670 FAX: 708-671-9469
or call 1-800-833-3156

Circle # 126

SCHURTER CATALOG

Schurter, Inc. now offers an expanded technical catalog detailing fuses, fuseholders, ac connectors and plugs, NEMA 5-15R outlets, power entry modules, and voltage selectors. Included is the recently acquired line of Feller PCC components which enhances the line of ac power entry products with 1-A to 20-A IEC 320 inlets, outlets, and plugs for "cold" or "hot" connections, snap-in and chassis-mount filtered power entry modules, and the FELCOM® power entry modules for custom configurations. Medical grade fuseholders are included.

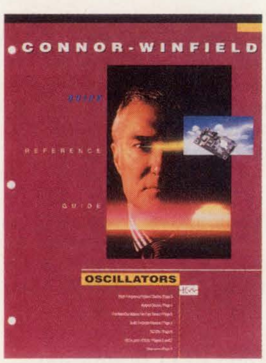
Schurter, Inc.

1016 Clegg Court
Petaluma, CA 94954
707-778-6311 FAX: 707-778-6401

Circle # 127

CONNOR-WINFIELD OSCILLATORS

Connor-Winfield introduces its 1992 Quick Reference Guide containing information on recent additions to its leading-edge crystal oscillator line including: CMOS square-wave models to 200 MHz, ECL 14-pin DIPS to 390 MHz, hi-frequency VCXO's to 200 MHz, 8-pin CMOS or ECL oscillators to 150 MHz, HCMOS tri-state SMD, 8-and 14-pin models to 70 MHz with many in-stock frequencies, and lppm 14-pin DIP TCXO models. Other models available from as low as 1 Hz to 650 MHz.



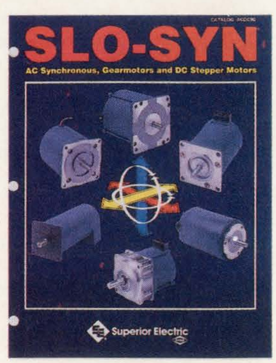
Connor-Winfield Corporation

1865 Selmarten Rd., Aurora, IL 60505
708-851-4722 FAX: 708-851-5040

Circle # 128

DC STEPPING & AC SYNCHRONOUS MOTORS

SLO-SYN® AC Synchronous, Gearmotors and DC Stepper Motors Catalog ACDC90 has AC Synchronous section that includes 72 rpm 3-phase types, 200 rpm types, and gearmotors with torque capability to 26 ft. lbs and ratios from 3:1 to 125:1. DC Stepper section describes motors with 1.8° full, 0.9° half and 0.0144° microstep capability. Operate to 20000 steps/sec. Holding torques to 5330 oz-in. Incorporates selection guide.



Superior Electric

383 Middle Street, Bristol, CT 06010
1-800-447-7171

Circle # 129

108 PAGE CATALOG

New 108-page catalog from PICO Electronics, Inc. is filled with electrical specifications for their line of ultra-miniature transformers, inductors and DC-DC converters. Transformers & inductors available as plug-in, surface mount or toroidal. Inductors offered with axial leads. More than 850 standard models of converters with single & dual outputs. Their small size (only 0.2″ high) makes their encapsulated packaging attractive. Included are low profile AC to DC power supplies, 0.5″ ht. to 200 Watts.

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453 No. MacQuesten Parkway
Mt. Vernon, NY 10552
914-699-5514 (NY) Toll Free: 800-431-1064

Circle # 130

ISOLATED SIGNAL CONDITIONING MODULES

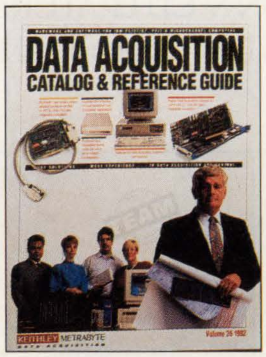
Selection guide details Burr-Brown's broad line of rugged, low-cost, high-performance Isolated Signal Conditioning products. Wide selection of modules and accessories offers a very reliable second source for both the popular 5B Analog I/O modules, and for the industry standard Digital I/O modules. These single-channel modules can reduce electrical noise, cut wiring costs, and protect the users' equipment from high voltage transients.

Burr-Brown Corp.
Call toll free 1-800-548-6132.

Circle # 131

1992 DATA ACQUISITION CATALOG AND REFERENCE GUIDE

From Keithley MetraByte-New Free 288 page full-color Data Acquisition Catalog and Reference Guide describes their complete line of Data Acquisition Hardware, Software and Systems for 1992. The catalog introduces many new products providing higher performance, lower power consumption and lower cost. Provides facts on all plug-in boards, Data Acquisition Systems and PC Instrumentation for use with IBM PC/XT/AT, PS/2 and Micro Channel computers. Also includes helpful selection charts and application notes.



Keithley MetraByte
440 Myles Standish Blvd., Taunton, MA 02780
508-880-3000

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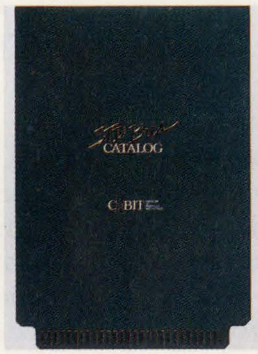

Cubit Div., Proteus Industries Inc.
340 Pioneer Way, Mountain View, CA 94041
415-962-8237

Circle # 133

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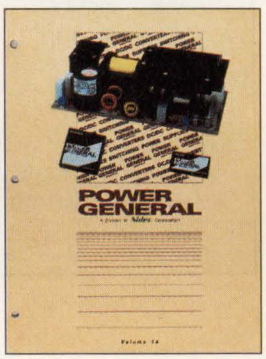

Power General
152 Will Drive
Canton, MA 02072
617-828-6216 FAX: 617-828-3215

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PTV 200W MODULAR HV POWER SUPPLY

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7 Fairchild Ave., Plainview, NY 11803.
516-349-8686 FAX: 516-349-8699

Circle # 135

COMPUTER BASED DMM

Brochure presents PREMA's new PC based measuring system that combines a high performance 7½ digit multimeter, 20 channel scanner and 386 based computer with instrument control software and IEEE-488 in one rack mountable cabinet. Precise measuring, storage and analysis with no programming or hardware integration. Also available is a full line catalog of PREMA DMMs, all of which are offered with a thirty day trial and two year warranty.

PREMA Precision Electronics, Inc.
4650 Arrow Highway Bldg. E-5,
Montclair, CA 91763
714-621-7292 FAX: 714-625-2098

Circle # 136

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Hewlett-Packard's new catalog features over 60 models of power supplies and electronic loads including 42 new models. Choose from single- and multiple-output configurations, most with built-in HP-IB(IEEE-488). HP's power products offer dependable performance for bench and system use. General reference information and selection indexes are also included.

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19310 Pruneridge Ave.
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800-452-4844, Ext. 2726

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21 Gray Oaks Ave., Yonkers, NY 10710
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Circle # 138

NEW PC SOFTWARE EXTENDS CAPABILITIES OF FLUKE HELIOS. DATA ACQUISITION FRONT ENDS

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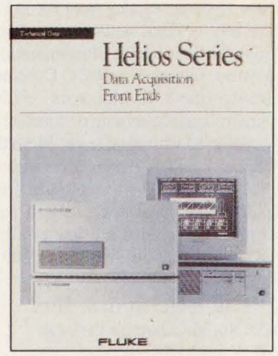

John Fluke Mfg.
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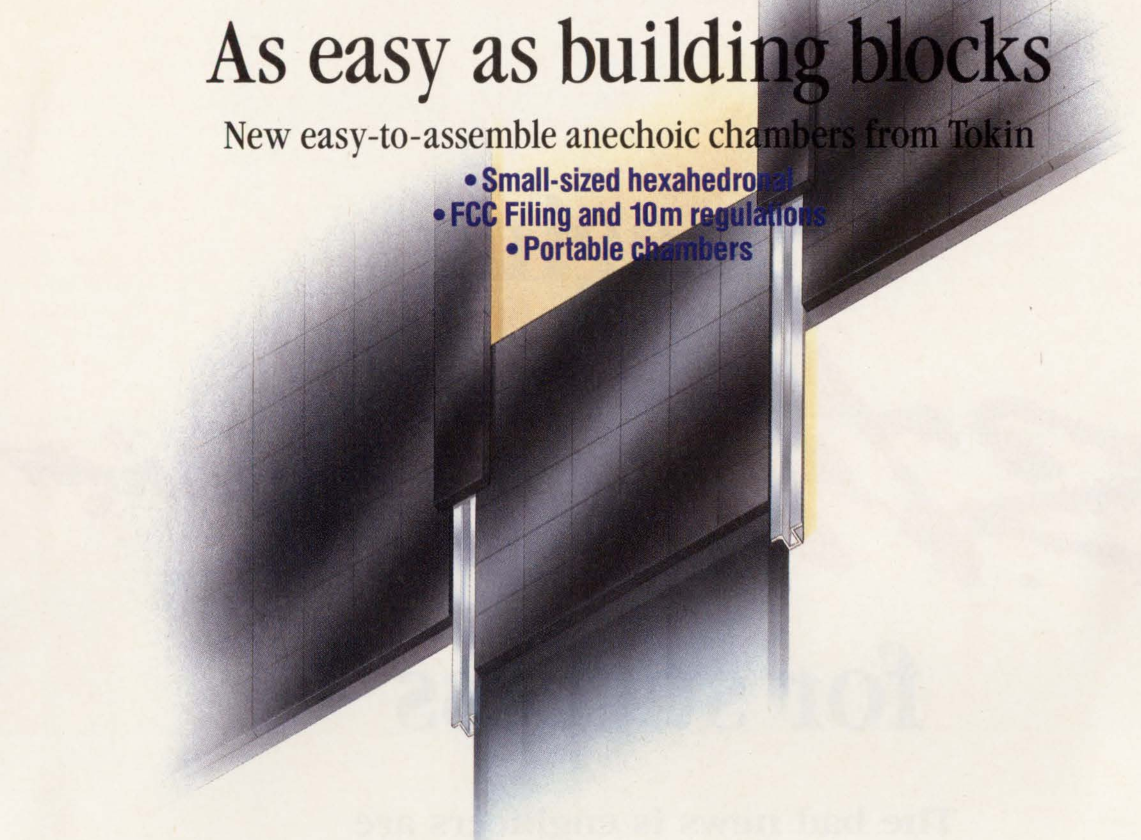

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CIRCLE NO. 175

Managing stress for success

The bad news is engineers are subject to pressures most people never face. The good news is you can handle those pressures productively.

Jay Fraser, Associate Editor

Stress costs American industry more than $200 billion every year in reduced productivity, absenteeism, and medical payments. Stress has been linked to strokes, heart attacks, hypertension, ulcers, diabetes, asthma, and many other diseases. Stress is the underlying cause of at least 75% of all visits to physicians. And you face stress every day of your life.

Because of the special demands of their profession, engineers have to deal with pressures that other people never experience:

- Technology changes so rapidly that engineers have to continually upgrade their knowledge and skills to remain valuable employees.
- Job security in high-tech firms is practically nonexistent. Expertise and seniority are no guarantees of employment. Engineers can lose their jobs overnight.
- Competition among high-tech companies is fierce. The pressure to develop products and get them to market as soon as possible is unrelenting.
- Some firms don't match engineers with projects very well. Too often, engineers are given jobs outside their speciality or below their skill level.

In addition, all the pressures that engineers are subject to become intensified whenever an organization downsizes.

However, the situation isn't as dire as it may appear. Many studies have shown that the amount of stress intrinsic to a job is not as important as how an individual handles the pressure.

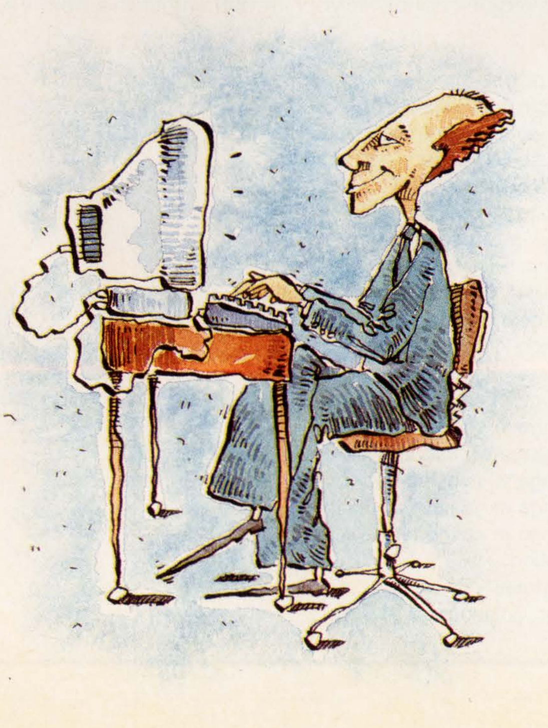
"Some individuals thrive on life in the fast lane and doing three things at once. That would overwhelm others," says Dr Paul Rosch, professor of medicine and psychiatry at New York College of Medicine and president of the American Institute of Stress. "Conversely, the same people would be under a great deal of stress if they had a dull, dead-end assembly-line job. It really has to do with the person and the job rather than the job itself. The important thing is the person/environment fit."

Dr Hans Selye, a pioneer in the study of stress and its physiological effects, wrote the book *Stress without Distress*. In it he defined stress as "the nonspecific response of the body to any demand made upon it." Selye pointed out that the body reacts in much the same way to an exhilarating run down a ski slope and a nasty argument with a coworker. Both pleasant and unpleasant experiences cause stress.

The widely used Holmes-Rahe scale enables you to determine how much stress you are under (see **box**, "The Holmes-Rahe scale of stress ratings"). Note that happy events, such as a marriage or the birth of a child, create a great deal of stress, and the home can produce just as much stress as the workplace.

A certain amount of stress is unavoidable in everyday life, and probably desirable. Stress sharpens the senses and spurs people on to

Illustrations by Courtney Granner/Lettering by Paul Kulhanek



greater achievement. Selye went so far as to call it "the spice of life." Stress actually makes people more efficient—up to a point. After that point, which differs for each individual, stress begins to hinder efficiency. And the more stress that is piled on, the faster efficiency drops. Selye called this excessive amount of stress "distress."

Most people mean distress when they use the word stress. To them, stress is the cause of tension, nervousness, and depression as well as the accompanying physiological consequences. Stress is inescapable, but it's important to remember that you don't have to be a passive victim of it. As Selye wrote "we can meet it efficiently...by learning more about its mechanism and adjusting our life accordingly."

Studies have shown that the most stress is created on the job when a person has a large amount of responsibility but little or no control over how the work is done. In one study, two groups of workers were given the same tasks to do under the same poor conditions. They were constantly subjected to loud, distracting background noises. The only difference was that the first group was supplied with a button that would stop the noise any time someone pushed it. The second group had no button.

The first group performed far better than the second, but it's significant that no one in the first group ever pushed the button. Just knowing they had control over their working conditions was enough to enable the first group to work more efficiently in a stressful situation.

Robert Karasek and Tores Theorell discovered a correlation between the development of stress-related illnesses and the amount of freedom people had to make decisions in their work. Even people in very challenging situations didn't show excessive psychological strain as long as they had the latitude to make their own decisions. Karasek and Theorell published their findings in a book entitled *Healthy Work*. They concluded, "The primary work-related risk factor appears to be lack of control over how one meets the job demands and how one uses one's skills."

"The crux of the matter is trying to determine what it is in your environment that's making you stressful, and trying to determine whether it's something you can exert some control over or whether you have to learn to avoid or accept," says Rosch.

The Type A personality

Some people are their own worst enemies when it comes to stress. They put excessive amounts of pressure on themselves. Psychologists designate these people as "Type A."

Type A people are aggressive, hostile, and driven. They overload their schedules, constantly race the clock, and distrust others. The im-

The Holmes-Rahe scale of stress ratings

Add up the numerical values of any life events you have experienced within the past 24 months. If your total score is more than 300 points, you have an 80% chance of a major change in your health within the next year.

Life event	Value
Death of spouse	100
Marital separation	73
Jail term	65
Death of a close family member	63
Personal injury or illness	53
Marriage	50
Fired at work	47
Marital reconciliation	45
Retirement	45
Change in health of family member	44
Pregnancy	40
Sex difficulties	39
Gain of new family member	39
Business adjustment	39
Change in financial state	38
Death of a close friend	37
Change to different line of work	36
Change in number of arguments with spouse	35
Mortgage over one year's net salary	31
Foreclosure of mortgage or loan	30
Change in responsibilities at work	29
Son or daughter leaving home	29
Trouble with in-laws	29
Outstanding personal achievement	28
Spouse begins or stops work	26
Begin or end school	26
Change in living conditions	25
Revision of personal habits	24
Trouble with boss	23
Change in work hours or conditions	20
Change in residence	20
Change in schools	20
Change in recreation	19
Change in church activities	19
Change in social activities	18
Mortgage or loan less than one year's net salary	17
Change in sleeping habits	16
Change in number of family get-togethers	15
Change in eating habits	15
Vacation	13
Christmas	12
Minor violations of the law	11

age that comes most readily to mind of a Type A person is the hard-nosed American businessman, but this kind of behavior is found widely among people in both genders and every profession.

Dr Meyer Friedman and Dr Ray Rosenman, two cardiologists, first identified and named Type A people. They also found that Type A people were three times as likely to develop coronary heart disease as others. Some doctors questioned how much Type A behavior contributed to heart disease when compared with other factors such as heredity and poor health habits. So Freidman and Rosenman decided to do another study.

They put together a group of 800 Type A men who had suffered heart attacks. The men were then given counseling to change their behavior. Friedman and Rosenman followed them for three years and found that modifying Type A behavior lessened their chances of having a second heart attack by 50%. Friedman wrote, "If changing behavior can have such a striking effect on people with well-established heart disease, it should be even more helpful to those who have not yet had a heart attack."

You can change your behavior, too. Even if you're not a Type A personality, it would probably do you good to lessen the tension in your life. Here are some steps you can take to reduce the stress you face on your job:

- Re-evaluate your goals. Do you really want to be president of the company? If your goals are unrealistic, pushing yourself to achieve them is only going to cause frustration. Choose attainable goals that you can reach in a reasonable amount of time.
- Analyze your job. Once you're certain of your goals, take a close look at the work you do. Is it leading you toward your goals or toward a dead end? If you feel you need to make changes in your job, talk to your boss and see if he or she can implement them. You may even discover it's time to look for a new job.
- Reschedule your work. Make sure most of your time and energy are devoted to your most important duties. Draw up a list of your tasks at work and see if you're finishing the most important ones first. If possible, work on one task until it's completed, then move on to the next. Don't dissipate your energies, concentrate them.
- Pace yourself. Keep your deadlines in mind. Don't work frantically on one project day and night until you burn yourself out. You may be rushing unnecessarily. But don't procrastinate, either. If you hesitate to tackle a large project because it seems overwhelming, break it up into smaller, more manageable tasks. Don't try to do everything at once and don't put things off.

You're not helpless

Making beneficial changes in your work life will lessen stress but will not eliminate it entirely. If you still feel you're under an excessive amount of pressure, you're not helpless. You can use other techniques to combat the pressure.

First, learn to relax. That's not as simplistic as it sounds. Thousands of people make their livings teaching others how to relax. Perhaps your company hires professionals to come in from time to time and conduct classes in relaxation techniques. Take advantage of those classes. If your company doesn't bring in professionals, the human resources department may be able to refer you to some.

The effectiveness of relaxation techniques differs widely among individuals. Some people find traditional methods such as meditation and yoga very useful. Other people prefer vigorous exercise. Others simply like to lose themselves in a good book.

"For some people, running or jogging is great. For others, it's boring as hell. The same thing is true for meditation," says Rosch. "The real trick is changing the way you perceive things—cognitive restructuring. For some people it's learning to be more assertive. For others it's time management. Like everything else in stress, it's not generic. Stress is a very personalized phenomenon and differs for each of us."

Applying modern technology to stress management has resulted in a technique called biofeedback. Biofeedback helps you control bodily functions, including heart rate, brain waves, and muscle tension, that were once considered completely involuntary.

In biofeedback a number of sensors are attached to your skin to measure your blood pressure, perspiration, body temperature, and other stress indicators. The sensors are connected to a machine with a display that enables you to monitor the sensors' ongoing readings. Through standard relaxation techniques, such as deep breathing, loosening muscles, and blanking out intrusive thoughts, you slowly learn how to relax and bring stress under control. Biofeedback is usually conducted in a hospital or clinic. Most people get the results they want after 10 to 15 sessions.

If you don't feel the need to seek professional help, you can do many things on your own to cope with the stress in your life.

Regular exercise can go a long way toward alleviating stress. The emphasis here is on regular. Experts recommend exercising for a minimum of one to one and a half hours three times per week. Exercise will relax your muscles and help you sleep better. Choose a

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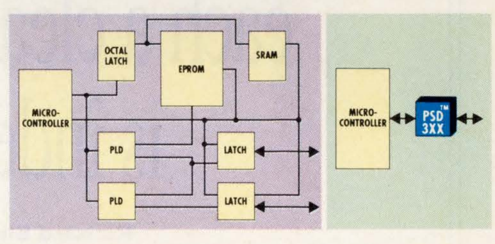

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form of exercise you enjoy so you won't think of it as a chore and intermittently force yourself to do it. Exercising at irregular intervals and overexerting yourself can actually increase stress. It also makes you prone to injuries.

Diet is also important in controlling stress. You should avoid foods with a high caffeine or salt content. Too much caffeine can make you nervous and irritable. Caffeine also causes blood vessels to constrict, which can give you a headache. Too much salt can drive up your blood pressure, which can lead to strokes, heart attacks, and kidney failure.

Foods such as candy, cake, and cookies contain processed sugars that elevate the level of your blood sugar quickly. This will temporarily make you feel that you have more energy, but your blood sugar will also plunge quickly, leaving you fatigued.

The best idea is to follow a sensible, balanced diet and eat three meals a day. Don't skip meals. That will make your energy level rise and fall erratically.

The key to stress management

Getting enough sleep and exercise and eating properly are ways of caring for your body, but the key to managing stress ultimately lies in your mind. Your mind needs rest and refreshment just as your body does. Don't dwell on your work 24 hours a day. Develop some outside interests. It doesn't really matter if it's chess or mountain climbing—find something to take your mind off your work.

Every once in a while, give your mind a longer break—take your vacations and holidays. Engineers are notorious for working odd hours and extra days. Try not to do it. Some companies require their employees to take their vacations within a specified time period. This has proven to be a wise policy. You can burn yourself out in a job you like as easily as in one you hate.

Talk to someone about the problems that are causing you stress. It doesn't do any good to keep your frustrations bottled up. Talk to someone in your family or to a close friend. If that's difficult for you, you may need to talk to a professional counselor.

Stress is a powerful force. If you let it rule your life, it can have a disastrous effect on your career, personal relationships, and health. However, you can bring stress under control and even harness it to work for you. How you handle stress is up to you. EDN

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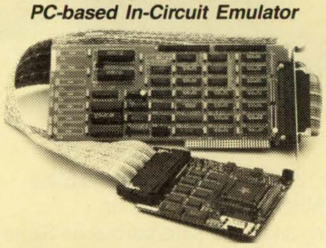

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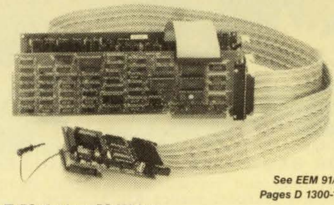

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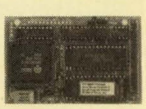

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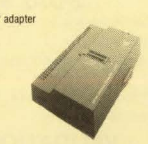

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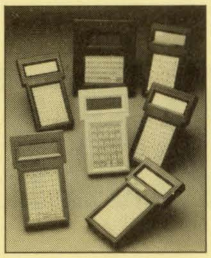

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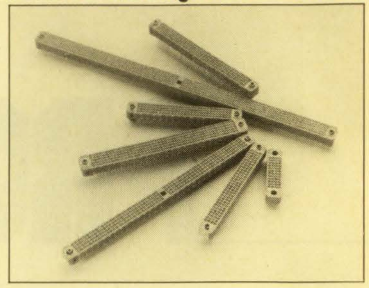

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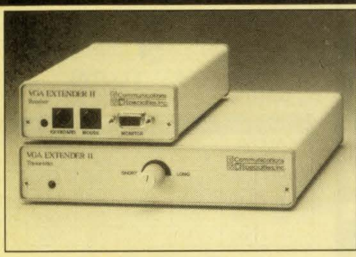

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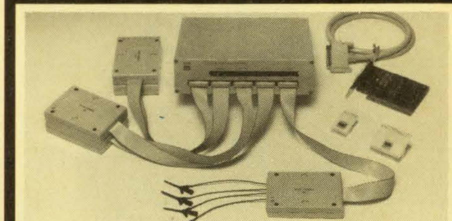

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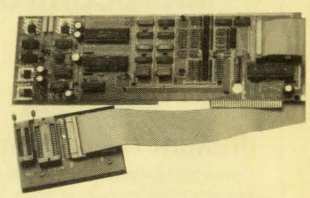

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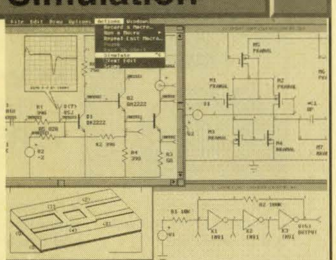

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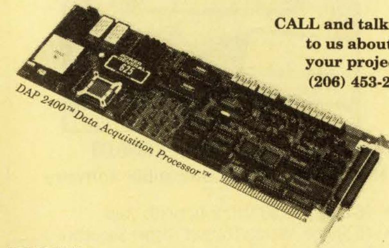

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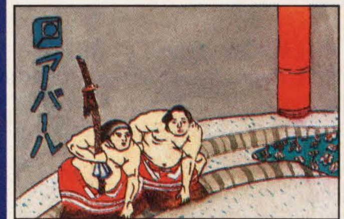

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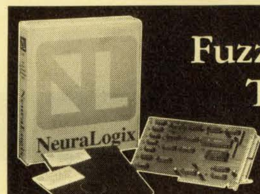

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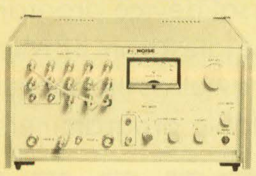

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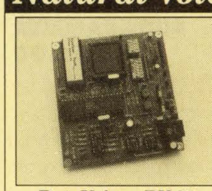

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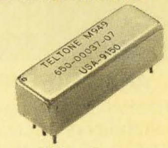

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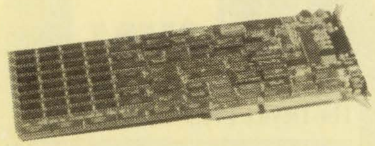

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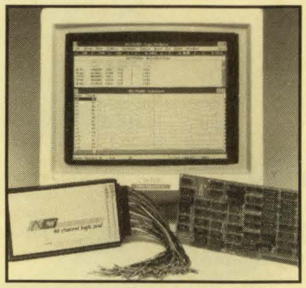

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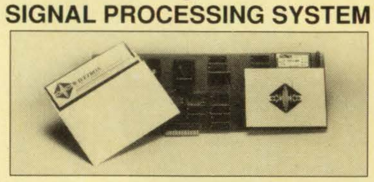

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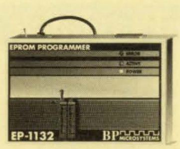

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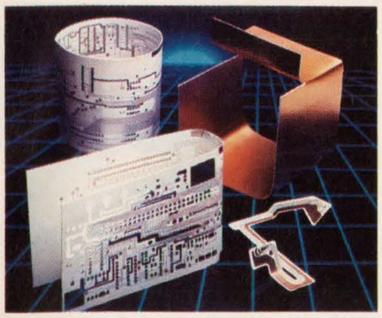

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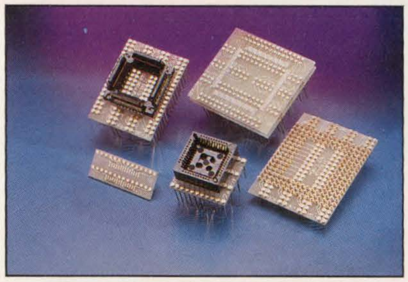

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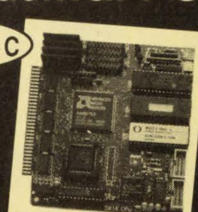

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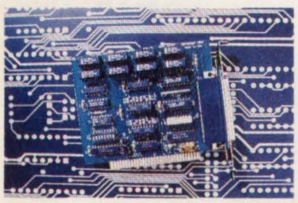

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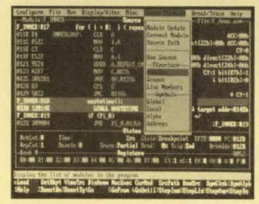

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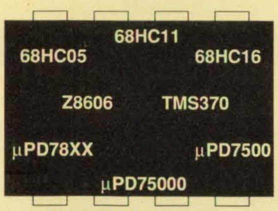

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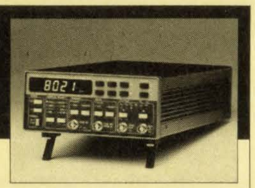

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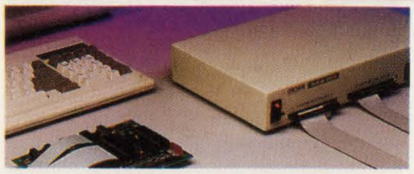

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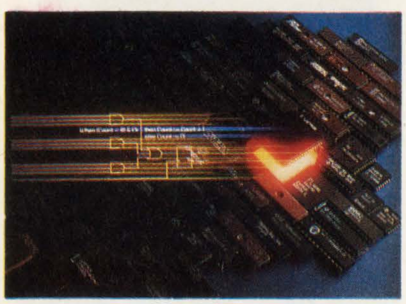

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Magazine Edition	May 21	Apr. 30	Analog ICs • Analog CAE • PC Board CAE Tools • Programmable-Logic Devices
News Edition	May 28	May 14	Communication ICs • CAE Software • Regional Profile: Texas, Oklahoma, Kansas
Magazine Edition	June 4	May 14	ASICs/PLDs • DSP Software CAE/Software/Interoperability Digital ICs & Semiconductors
News Edition	June 8	May 21	CAE SPECIAL ISSUE EDA/CASE Supplement • DAC Hot Products • Software Engineering • Diversity Special Series
Magazine Edition	June 18	May 28	Microprocessors • Electromechanical Devices • ICs & Semiconductors
SOFTWARE ISSUE	June 18	May 28	SOFTWARE ENGINEERING SPECIAL ISSUE (To be polybagged with the June 18th Magazine Edition issue)
News Edition	June 25	June 11	MILITARY ELECTRONICS SPECIAL ISSUE • DSP Hardware • Military Electronics Regional Profile: Florida, Alabama
Magazine Edition	July 6	June 11	INTERNATIONAL PRODUCT SHOWCASE—Vol. I Hardware & Interconnect Software • ICs & Semiconductors • Power Sources
Magazine Edition	July 20	June 25	INTERNATIONAL PRODUCT SHOWCASE—Vol. II Computers & Peripherals Components • CAE • Test & Measurement
News Edition	July 23	July 9	Engineering PCs & Workstations • CAE Software SIGGRAPH Hot Products Graphics Technology • Engineering Management Special Series • Regional Profile: Arizona, New Mexico
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EDN-INTERNATIONAL ADVERTISERS INDEX

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EDN-ACRONYMS & ABBREVIATIONS

A/D—analog to digital
AM—amplitude modulation
CGA—color graphics adapter
CMOS—complementary metal-oxide semiconductor
D/A—digital to analog
DOS—disk operating system
DSP—digital signal processing
DSTN—double-supertwist nematic, a type of liquid-crystal display
EGA—enhanced graphics adapter
EMF—electromotive force
FET—field-effect transistor
FFT—fast Fourier transform
FIR—finite-impulse-response
FM—frequency modulation
FPGA—field-programmable gate array
FSK—frequency shift keying
FSTN—film-supertwist nematic, a type of liquid-crystal display
IC—integrated circuit
LCD—liquid-crystal display
LO—local oscillator
MFLOPS—million floating-point operations per second
MS-DOS—Microsoft disk operating system
MSI—medium-scale integration
MSTN—monochrome-supertwist nematic, a type of liquid-crystal display
MTBF—mean time between failures
OS—operating system
PALC—plasma-addressed liquid crystal, a type of liquid-crystal display that uses plasma to switch pixels on and off
PC—personal computer
PID—proportional-integral-derivative
PLL—phase-locked loop
PWM—pulse-width modulation
RAM—random-access memory
RF—radio frequency
RFI—radio-frequency interference
RISC—reduced-instruction-set computer
rms—root mean square
rpm—revolutions per minute
SI—International System of Units
Spice—Simulation Program with Integrated Circuit Emphasis, a public-domain analog-circuit simulator from UC Berkeley
SSI—small-scale integration
STN—supertwist nematic, a type of liquid-crystal display
TAB—tape automated bonding
TFT—thin-film transistor, the transistor type used by active-matrix liquid-crystal displays
TN—twisted nematic, the basic type of liquid-crystal display
TTL—transistor-transistor logic
VCO—voltage-controlled oscillator
VGA—Video Graphics Array, a resolution standard for displays

This list includes acronyms and abbreviations found in EDN's Special Report, Technology Updates, and feature articles.

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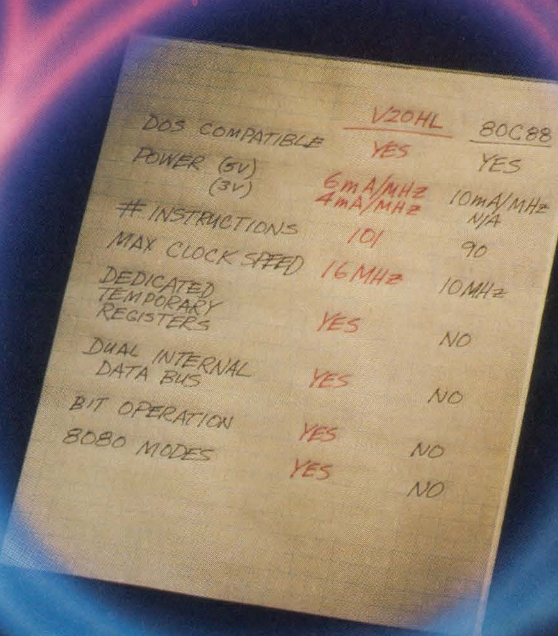

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Tape backup software provides speedy, easy-to-use disk insurance

I appreciate software with a sense of humor and was amused by my first error message from Novaback, a general-purpose tape-backup PC software package for SCSI-based tape units. When I tried to install the software from the E: 3½-in. floppy-disk drive in EDN's 80486-based All-Star PC (see EDN, March 15, 1990, pg 142), the installation program couldn't find its files and asked me, 'How would you like to solve this little problem?' With that one exception, I had no problems at all with this software. In fact, I completed the installation, configured the software, and backed up more than 100 Mbytes from my hard disk by the time I reached page 3 of the manual.

Novaback knows how to operate a large number of SCSI-based tape drives including units from Archive/Viper, Caliper/Sankyo, Cipher, Exabyte, Fujitsu, Hewlett-Packard, Kennedy, LMSI, Sony, Storagetek, Tandberg, Teac, Wangdat, and Wangtek. That repertoire includes ¼- and ½-in.-cartridge tape units, 4-mm DAT (digital-audio-tape) drives, 8-mm-cartridge tape drives, and even some 9-track reel-to-reel behemoths. The software works with the Always Technology IN-2000 or Adaptec's 1540 or 1640 SCSI host adapters for the PC. Because of its ability to control many different drives, this software is an excellent choice for companies configuring many types of PCs using several different tape formats. Your customers can learn and use just one software package, which should reduce your support headaches.

Backing up a hard disk to tape is like taking out an insurance policy, and you want the job done quickly and efficiently. That's how Novaback performs. You can operate the menu-driven program from the keyboard or with a mouse. EDN's All-Star PC incorporates an Exabyte EXB8200, which can store 2.5 Gbytes on one 8-mm videotape cartridge; I use the program to save the contents of my entire hard disk to tape every time. The speed is truly phenomenal. Although the All-Star PC has more than 1 Gbyte of disk storage, it currently contains "only" about 135 Mbytes of programs and data. Novaback and the Exabyte drive sock this pile of data away in less than 20 minutes.

For slower tape drives, you may want to save time by performing incremental backups, and Novaback allows you to do that. A configuration menu gives you the option to selectively back up read-only, hidden, and system files; subdirectories; and files modified since the last backup. You can also designate selected files to back up, and the software can also save trustee rights for directories residing on a Novell file server. An installable device driver included with the package lets you schedule automatic backups.

I view disk backups as something I need to do but I don't want to make a career out of the chore. In particular, I don't care to learn the arcane terminology that professional tape archivists and MIS managers have developed to sustain their priesthood. Novaback allows me to do exactly what I want, and it doesn't burden me with the details. Yet it can handle very complex operations, if I ever become that ambitious.—**Steven H Leibson**

Novastor Corp, 30961 Agoura Rd, Westlake Village, CA 91361. Phone (818) 707-9900. FAX (818) 707-9902. $225.

Support service sets the standard for all to meet

Once or twice a year, I experience a "paradigm shift": something absolutely stuns me and changes the way I view the industry. It happened recently.

I needed a new device driver so that the NEC Multisync Graphics Engine display card in EDN's All-Star PC could work with Microsoft Windows 3.0. About the same time, NEC Technologies started running some advertisements that included a fax technical support service number ((800) 366-0476). I tried using this service to solve my problem. Things will never be the same.

When I called NEC's Fast Facts line, a machine answered. However, this was no ordinary answering machine or phone mail system. Using a recorded message, the Fast Facts line told me that it could transmit several documents by fax and offered me the choice of ordering individual documents by number or a catalog of available documents. Because I didn't know any document numbers, I requested the catalog by pressing one button on my telephone's keypad. Then, the Fast Facts machine asked me to key in my own fax number, which I did. Within five minutes, my machine produced a 7-pg catalog from NEC. Less than five minutes later, I had selected, ordered, and received two installation guides, two application notes giving me customization information for flicker-free display modes, and a troubleshooting guide. I also had the phone number for a computer bulletin board where I could find the drivers I wanted and a number for a voice line for technical support, which I haven't needed.

In less than 10 minutes, I had obtained a wealth of new information and the location of the drivers I sought. Contrast this chain of events with your last technical support experience and perhaps you'll be struck, as I was, by the boost in support that this technology provides. I called NEC Technologies to find out more about the technology used. Surprisingly, it's off-the-shelf, commercial technology that's readily available from Faxback Inc (Beaverton, OR, (800) 873-8753, demo line (503) 690-6390).

NEC Technologies installed its system about a year ago but use of the service has only recently taken off because of the company's advertising campaign. The fax-based support service carries information about the company's display products, CD-ROM drives, desktop and laptop PCs, printers, hard disks, video cards, and professional video equipment. The service logged 12,000 calls last December, which represents 12,000 customers who received product and support information in minutes without speaking to an NEC employee or representative. This service sets a new standard for customer support, and I believe that companies must either adopt this style of support or they will simply cease to be competitive.

—Steven H Leibson

Learning the gentle art of effective delegation

OK, so now you're a manager. You're going to have to delegate tasks you formerly did yourself. The problem is, you know you're the best person for every job you're supposed to delegate.

If that scenario isn't familiar, perhaps you're not comfortable with the thought of abandoning the technical side of the business. Maybe you're just uncomfortable taking responsibility for the people who work for you. If you find yourself in one of these situations, *How to delegate effectively* is the book for you.

In its scant 49 pages, this booklet discusses just about everything a new manager needs to know. Even experienced managers should find useful information here. Author Weiss' style is very readable. He often employs fictional characters in short skits to illustrate his points. For example, to flesh out a section covering the correct way to handle an employee's reluctance to assume new responsibilities, Weiss allows his mythical manager, Roxanne, to converse with Val, another character in the book. These conversations are terrific—they move the book's discussion away from the abstract and give you some real words that you'll feel comfortable using.

The book's seven chapters span delegation from its roots (your objectives and those of your work unit) to checks and balances (making sure the work is done and done well). This book proves that managerial training books can be brief, interesting, and informative. It's part of the publisher's Successful Office Skills series and costs $4.

—Steven H Leibson

How to delegate effectively *by Donald H Weiss. American Management Association, 135 W 50th St, New York, NY 10020. Phone (212) 586-8100.*

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