

A CAHNERS PUBLICATION March 2, 1992

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Communications **Technology** 

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**Defining** standards for FDDI

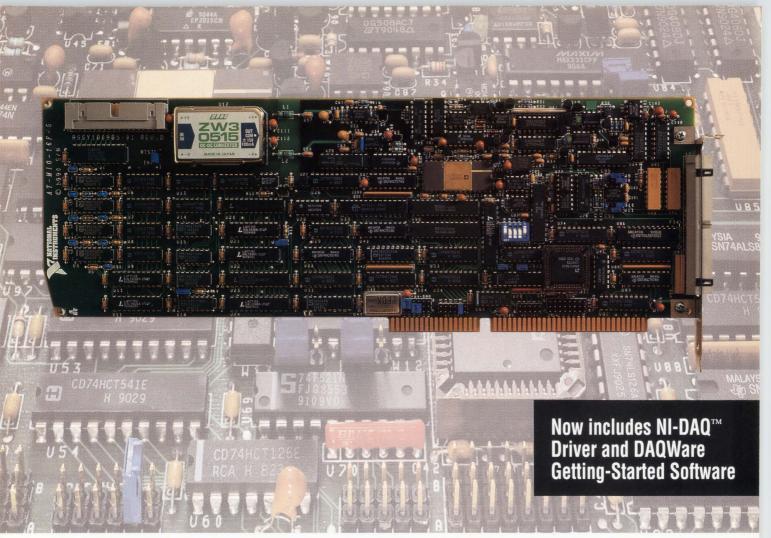
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OBJECTIVE: Develop an assured resistor supply, along with guidelines for performance and continual improvement.

<u>UNITS INVOLVED</u>: John Fluke Mfg. Co., Inc., Dale Electronics, Inc. and Ultronix.

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Today, three locations participate in the coordinated supply of a wide range of resistors. Requirements for wirewound resistors used in current shunt circuitry are a primary responsibility of Dale's Wirewound Division in Columbus, Nebraska, and Ultronix in Grand Junction, Colorado. Both standard and application-specific designs are involved, including special solid wire shunts produced by Ultronix using the percussive arc process.



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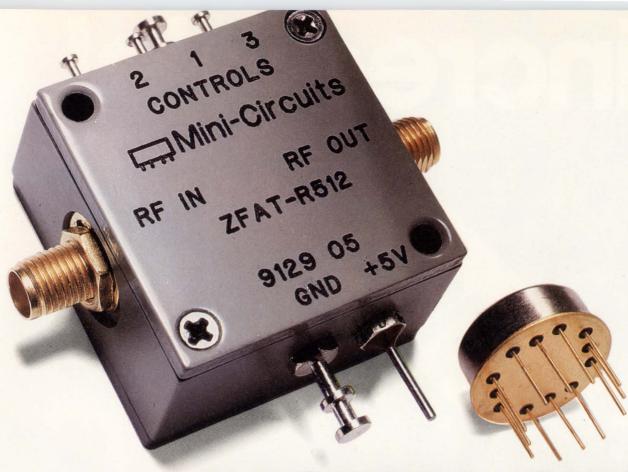
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MARCH 2, 1992

VOLUME 37, NUMBER 5



On the cover: EDN's Special Report examines the emerging test and measurement techniques that can make your measurements simpler and more accurate. Among the developments, consider a pair of probes that measures current in a conductor-not voltage across a component, as you might expect. (Photo courtesy Keithley Instruments) . . . . . . . . . . . . . PAGE 118



#### COMMUNICATIONS TECHNOLOGY SPECIAL ISSUE

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS WORLDWIDE

#### SPECIAL REPORT

#### New measurement techniques

Though the test and measurement field is noted for conservatism, it is far from idle; T&M companies are constantly developing new technologies. —Dan Strassberg, Technical Editor

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#### **DESIGN FEATURE**

#### Use spectrum analyzers' selectivity to precisely measure random noise

Because a spectrum analyzer makes a variety of measurements, it may be the most convenient, though not the most obvious, instrument

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to use when measuring noise.—Kevin Johnson, Hewlett-Packard Co

### **TECHNOLOGY UPDATES**

#### Shareware and freeware are a phone call away

In contrast to the cornucopia of shareware available for every other application area, electrical-engineering shareware is in short supply.—Charles H Small, Senior Technical Editor

Continued on page 7

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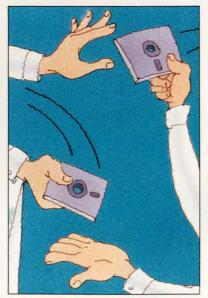


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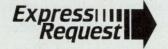
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Engineering shareware is easily accessible; the problem is you don't have a lot of programs to choose from. . . PAGE 49

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#### **TECHNOLOGY UPDATES**

### Opposing groups struggle to define standards for FDDI using copper wire

Although implementation of the FDDI over twisted-pair copper wiring is not yet a reality, the ANSI X3T9.5 committee may soon resolve the conflicting issues.—Dave Pryce, Technical Editor

### High-speed-CPU design: 40-MHz CMOS circuits send designers back to school

CPUs that run at 40 and 50 MHz are forcing CMOS designers to amass ECL design techniques to make circuits that function in this ethereal realm.

—John Gallant, Technical Editor

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### Smart-card applications' hidden problems add to designers' challenges

When you develop an application for smart cards, you have to tackle a few problems that you might not ordinarily expect.—*Gary Legg, Senior Technical Editor* 

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#### GaAs ICs see mainstream duty as µP glue logic

Designers that leave GaAs out of their toolbox for new communication products and products that use fast RISC or CISC  $\mu$ Ps could find themselves in the same situation as drivers who forget to stop by the service station occasionally.— $Maury\ Wright,\ Technical\ Editor$ 

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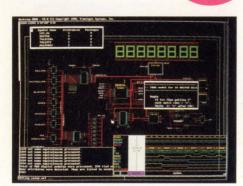
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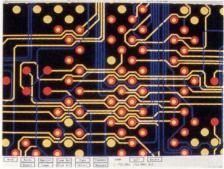
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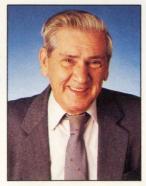
A summary and analysis of articles in this issue

Technical Editor Dan Strassberg has rounded up some unusual measurement techniques for this issue's Special Report. As Dan says, the only thing conservative about the test-and-measurement arena is its reputation. Some of the techniques he discusses in his report, such as electron- and ion-beam semiconductor probing, are anything but conservative.

Packard's Lake Stevens Division.

Companies trying to push 100-Mbps communications through unshielded twisted-pair wiring certainly face all sorts of noise problems. Technical Editor Dave Pryce's article about FDDI (fiber distributed-data interface) on copper wire looks at the technical and standardization issues surrounding this nascent technology. Be sure





**Dave Pryce** 



John Gallant

One of the problems Dan faced while writing this article was selecting the measurement techniques he would discuss. Several of the EDN magazine edition's editors helped Dan create a list of candidates. To companies offering products based on new measurement techniques that we may have omitted from the story, we suggest that you contact us. We've always got another issue just around the corner.

This issue is also our annual communications issue. Some of the techniques covered in Dan Strassberg's Special Report are quite valuable for communications applications, but you'll also find some additional, finely focused help with noise measurements in Kevin Johnson's contributed article on using spectrum analyzers for measuring random noise. Johnson works for Hewlett-

to read the sidebar that untangles competing signal-encoding techniques and their arcane terminology.

Noise also plays a major role in the design of high-speed digitalsystem design. In his Technology Update on high-speed CPU design, Technical Editor John Gallant takes a swing at the noise and timing problems associated with µP-based designs operating at 40 MHz and above. These high-speed circuits are borrowing more than a few design techniques such as phaselocked clocks from the communications realm. John also takes a look at the CPU modules that many semiconductor firms are now offering for their highest speed µPs.

> Steven H Leibson Executive Editor



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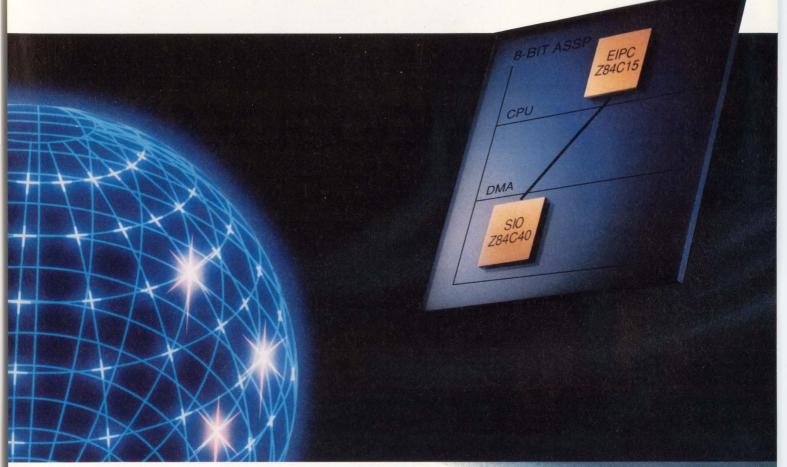
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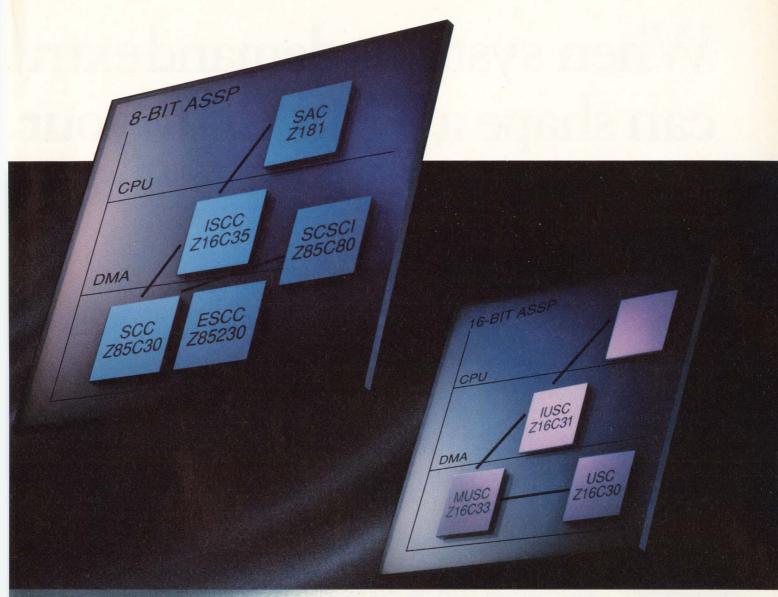
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(SIO™ controller) and the versatile industry standard SCC controller that's used in all Appletalk® networks . . . to the Enhanced SCC (ESCC™ controller), which boosts performance up to 10 times. Plus our Integrated USC (IUSC™ controller), which provides sophisticated buffer management capability, is perfect for handling fast, packetized data across networks. And you get simplified, faster system operation with an on-board DMA. Since all these controllers offer code compatibility in their families, you're also assured a quick, easy migration path.

There's no question that ASSPs are the best option for a rapidly growing number of designs. At Zilog we've been producing ASSPs and refining Superintegration™ design methodology longer and better than anyone, which is why we provide the largest library of familiar



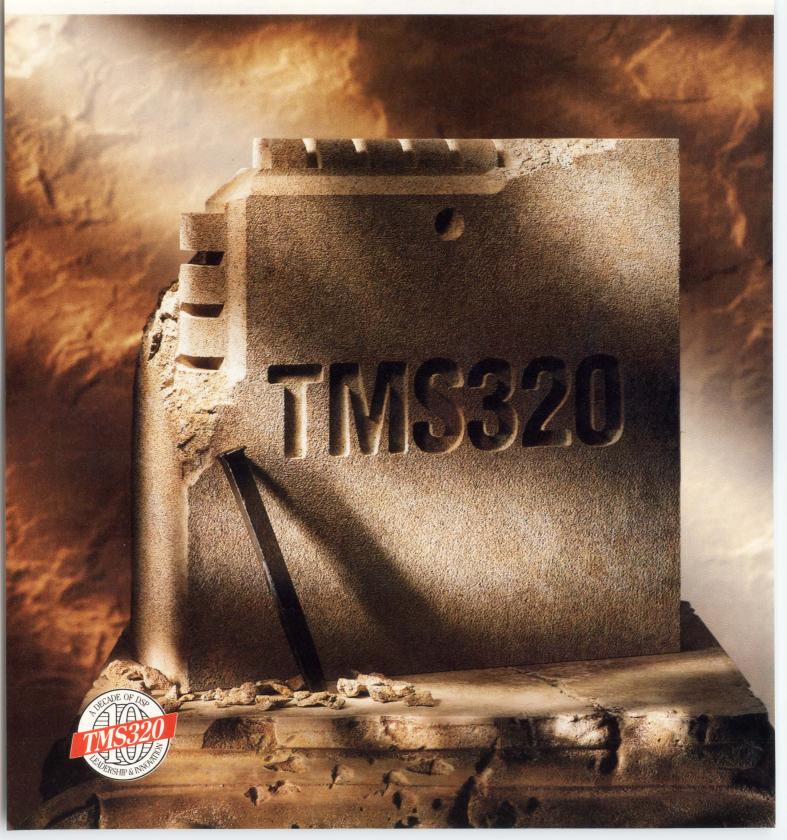
cores and cells in the industry. We're continually developing new members of Zilog's SCC and USC controller families, and, because we have the manufacturing control that comes from having our own fabrication facilities, you can rest assured that every exciting innovation will reflect the high standards of quality and reliability for which Zilog is known . . , and all the flexibility you need for today's complex designs.

To find out more about Zilog's Datacom families, or any of our rapidly growing Superintegration product families, contact your local Zilog sales office or your authorized distributor today. Zilog, Inc., 210 East Hacienda Ave., Campbell, CA 95008-6600, (408) 370-8000.





# When systems demand extra can shape a TMS320 to your



# -special DSPs, we needs.



hoosing the right DSP for your application is vital to your marketplace success. Only TI has the customizable capability and broad TMS320 family to help you get what you need.

What you want is what you get With our unique customizable digital signal processing (cDSP) capability, you can achieve the integration and product



and then integrate them all directly on proven TMS320 DSP chips. You can even change the mix of on-chip memory and peripherals. Yet device development cycles are shorter and costs are lower than with full-custom gate-level approaches.

Over the past five years, this innovative TI technology has created winning solutions for hundreds of high-volume market leaders.

#### **Broad TMS320 family**

Our more than 30 standard DSP solutions can meet the majority of your price/performance needs.

You can choose from our 16-bit fixedpoint DSPs that start at \$3 or from our 32-bit floating-point devices beginning at \$25.
There are family members delivering 50-MFLOPS performance, EPROM and OTP DSPs and

those optimized for specific applications, plus military versions.

When you want super-processing power, our parallel-processing TMS320C40 DSP allows direct processor-to-processor communications to achieve the MOPS, MBPS, MIPS and MFLOPS your design requires.

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To speed you to market faster, you can talk with TMS320 specialists, attend hands-on workshops, read over 2,000 pages of applications notes and contact more than 100 third parties and consultants.

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You will receive information on our cDSP capability, the complete TMS320 family of devices and our world-class support. What's more, we'll send you "Designing with DSPs is Easy" – an interactive disk that gives you a personal look at TMS320 support and the TMS320 Programmer's Interface.

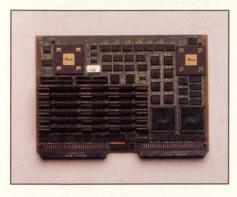
TEXAS INSTRUMENTS

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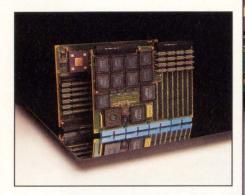
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#### 400 MOPS FOR 6U VMEbus SYSTEMS

This 6U VMEbus board performs 400 million operations per second and is optimized for frequency domain processing such as FFTs and finite impulse response (FIR) filters using fast convolution. The FDaP features a private 32-bit, 20 MHz high-speed data I/O bus and extensive double buffering for continuous processing of real-time data. An additional 32-bit complex output provides phase/magnitude data. The a66540 is available in 25 MHz and 40 MHz versions. A single 40 MHz version can execute a 1K point FFT in 132.7 µs and a 64K point FFT in 13.1 ms. These times are nearly halved for real input. Multiple FDaPs can be cascaded to achieve almost linear improvement in FFT performance. Plug 400 MOPs into your system by calling **array** Microsystems' Hotline: 719-540-7999.



#### CORNERTURN PROVIDES QUANTUM LEAP IN 2D IMAGE PROCESSING PERFORMANCE

The a66545 Cornerturn™ board, used in conjunction with the a66540 FDaP board for real-time two-dimensional image processing, is the first capable of processing an entire 256 x 256 pixel frame of image data in 15.2 milliseconds. This equates to a continuous, real time rate of 65 frames per second. For 512 x 512 images, the board set transforms images in 71 milliseconds, or 14 frames per second. Designed for medical imaging, radar, sonar, machine vision, and other real-time 2D image processing applications, the board set features performance of 400 MOPS at a clock rate of up to 40 MHz. The Cornerturn accepts 32-bit complex I/O data through 10 MHz double-buffered external I/O connectors or through the VMEbus and stores it in one of four on-board frame store memory buffers. For technical assistance, call array Microsystems' Hotline: 719-540-7999.



#### SOFTWARE DEVELOPMENT TOOLS LAST LINK IN COMPLETE SYSTEM SOLUTION

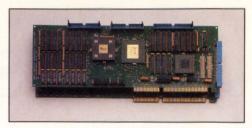
arrayso<sup>6</sup>/I<sub>10</sub>, a complete DSP software development system supporting array Microsystems' a66 Family of Products, provides a menu driven user interface allowing easy access to a suite of powerful development tools at the click of a mouse. This development system features a DaSP/PaC code generator, assembler, disassembler, window generator, full DaSP/PaC program control, on-screen display of data, and board-level diagnostics. For technical information or original program assistance, call array Microsystems' Hotline: 719-540-7999.



#### THE DaSP/PaC CHIPSET:

The heart of the world's fastest DSP product family

The Digital array Signal Processor (DaSP) executes 16 high-level instructions, including FFT butterflies, windowing, complex multiplies, and general-purpose functions. The Programmable array Controller (PaC) manages the entire system, including address generation for the DaSP and memory, and I/O up to 80 MHz. Using a single chipset, for example, a 1024 point FFT requires only 12 instructions and can execute in only 131 usec; a complex FIR filter, using 28 instructions, processes at a 2.3 MHz rate. For even higher performance, you can cascade the chipset. Both utilize a 144-pin PGA format and are available in 30 and 40 MHz versions. To receive complete technical information, call **array** Microsystems' Hotline: 719-540-7999.



#### PC-FDaP PERFORMS 250 MOPS!

The a66550 Frequency Domain array Processor (FDaP) brings high performance FFT processing to any PC-AT compatible computer. The two board set will fit into two full size PC-AT slots, operate on the 16 bit PC-AT (ISA) bus, and allow real or complex input from either the high speed connectors on the back panel or from the PC-AT bus. The FDaP accommodates an optional complex I-and-Q to magnitude-and-phase converter for post-FFT processing. Available in two memory configurations, the a66550 handles complex FFTs up to 32K points and real FFTs up to 64K points. The a66550 can compute a 1024 point complex FFT in just 210  $\mu s$ . For complete technical information, call **array** Microsystems' Hotline: 719-540-7999.

1420 Quail Lake Loop, Colorado Springs, CO 80906



**EDITED BY SUSAN ROSE** 

### 2-Gsample/sec DSOs become more affordable

Digital storage oscilloscopes (DSOs) that take 2 Gsamples/sec in real time and provide 0.5-GHz bandwidth are hardly garden-variety instruments. Those that offer such performance on four channels simultaneously are even more unusual. With the introduction of the TDS 640, Tektronix has changed the economics of high-performance real-time DSOs. The fixed-configuration 4-channel unit, complete with four active probes, an integral DSP  $\mu P$ , advanced triggering facilities, and a user interface that combines icons and text-based menus will cost \$20,980 with probes, \$19,000 without probes. A 2-channel unit, the TDS 620, will cost \$13,540 with probes, \$12,550 without probes. Tektronix Inc, Pittsfield, MA, (800) 426-2200.—Dan Strassberg

#### 4-Mbit flash memories offer block erase

The HN28F4001 flash memories incorporate two features that reduce control overhead in memory-card applications: block erase and self-completing commands. The block-erase capability lets you independently erase any of the device's 32 blocks. You can also erase either multiple blocks or the entire chip with a single command. Both erase and programming commands are selfcompleting, freeing the processor from the overhead of verifying the contents of each memory location. Once you have issued a self-completing instruction, the IC handles all of the prewrite and verify steps internally. When a command finishes, the device sets a bit in a status register to indicate the device's

readiness for additional commands.

The device is organized as 512k × 8 bits and runs on 5V for read-only operations; it needs 12V for programming. It has an access time of 120 nsec, a programming time of 10 usec/byte, and an endurance of 10,000 cycles. It is available in DIPs, SOPs, and TSOPs for \$49 (1000). Hitachi America, Brisbane, CA. Ask for literature package M13P005 at nearest sales location.

-Richard A Quinnell

#### Nonvolatile cachememory board adds speed to PCs

The PCDC-3 board from GTEK provides a 256-kbyte to 3-Mbyte non-volatile disk-cache memory for users of IBM PC/AT-compatible PCs. The disk-cache board includes its own BIOS, which inte-

grates itself into the PC's data-storage subsystem with no loss of MS-DOS memory. The board caches read and write operations and includes a battery with a 10-year rated life to ensure data integrity. The board's nonvolatile design does not require it to write cached data to disk, even on power down. The board only writes data to disk with a DOS command, or when the least recently used caching algorithm needs to flush the cache to read new data. A 10-MHz 80286based PC can write a full sector of data to the board in 200 usec. The board can substantially speed up performance in graphically intensive applications. A board configured with 256 kbytes of cache memory costs \$499. GTEK Inc, Bay St Louis, MS, (601) 467-8048, FAX (601) 467-0935.—Maury Wright

## PC manufacturer adds chassis and RAM disk

Diversified Technology's CRM series of industrial-grade 19-in. rack-mount chassis includes a 14-slot PC/AT-compatible passive backplane. Optionally, you can specify the chassis with 10- to 16-slot passive EISA backplanes. Power options include a standard PC-grade supply, 250 and 350W quick-disconnect industrial-grade supplies, or 24 or 48V dc input supplies. The chassis features

filtered forced-air cooling, fold-down front panel, and shock-mounted drive bays. Prices for a chassis range from \$970 to \$2000. The company has also announced the CRR806 PC/ AT-compatible RAM-disk board that can accommodate a mixture of static RAM (SRAM), EPROM, and flash memory. A board configured with 4 Mbytes of flash memory and 8 Mbytes of SRAM costs \$2700. Diversified Technology, Ridgeland, MS, (601) 856-4121, FAX (601) 856-2888.

-Maury Wright

# ICs' standard supply voltages dip to 3V

Portable computer systems are driving what may become an industrywide shift to 3V as the supply voltage for ICs. SMOS Systems now offers two gate-array families and a standard-cell library for designers needing 3V ASICs. The SLA9000L and SLA10000L are low-voltage extensions of existing gate-array families. The SLA9000L family offers arrays with as many as 20,000 usable gates and gate delays of 1.3 nsec (2input NAND). The SLA10000L has 100,000 gates and delays of 0.48 nsec.

The SSC5000L standard-cell library uses 0.8µm double-metal design rules and can accommodate designs as large as 100,000 gates. The library includes TTL74-series logic, 1- and 2-port RAM, ROM, and multipliers. The gate delay on a 2-input NAND is 0.48 nsec. The library and the gate-array families handle supply voltages from

2.7 to 3.6V. Nonrecurring engineering charges for the gate-array designs begin at \$15,000. SMOS Systems, San Jose, CA, (408) 954-0120, FAX (408) 922-0578.

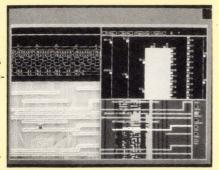
-Richard A Quinnell

## Tool set brings guided probing to ICs

In the world of pc-board test, guided probing long ago earned its stripes as a troubleshooting aid by minimizing the number of measurements needed to localize faults. However, if you were probing the innards of an IC to pinpoint why it didn't work, using either mechanical probes or an electron-beam (E-beam) probing system, the only intelligence you could rely on was your own. Indeed, some companies considered probing for IC faults to be such a specialized task that they allowed only a few people to

do it. Now, however, a tool set called IDA (Integrated Diagnostic Assistant) promises to change that situation drastically.

Like guidedprobe tools for pc boards, this tool set methodically directs a probe operator through the circuit under test starting at the output pins. By using CAE data, auto-



The IDA's windowed display shows (clockwise from top left) logic-analyzer waveforms, a diagnostic display, the layout of the device under test (DUT), and a scanning electron micrograph of the DUT.

mating repetitive operations, and eliminating guesswork, the tool set lets operators with only modest skills and no familiarity with the device under test pinpoint problems. Using the tool set, you can compare measured waveforms with simulated ones. Moreover, the tool set communicates with an E-beam prober's navigational software so that pertinent areas of the IC schematic and layout appear on a workstation screen beside a magnified view of the chip surface. The tool set also maintains a log of each probing session. Networking ability gives an operator at a remote workstation full control over the probing process. The software costs \$225,000. Schlumberger Technologies, San Jose, CA, (408) 437-5129.—Dan Strassberg

#### Op amp delivers 100V and 30A at 100V/µsec

High-power electromechanical and audio applications can literally get a boost from the PA05 power op amp. The 250W device operates with power-supply voltages to 100V and can source or sink as much as 30A. Further, the amp has a 100V/µsec slew rate and exhibits less than 0.02% THD operating at 200W over a 30-Hz to 30-kHz frequency range. The device has a 360-kHz power bandwidth, and at dc it exhibits an open-loop gain of at least 94 dB. Several features, including 4-wire output-current sensing, thermal protection, and an external shutdown input pin, let the amp safely operate at high power levels. The device costs \$189 (100). Apex Microtechnology Corp, Tucson, AZ, (602) 742-8600, FAX (602) 888-3329, TLX 170631.

-Steven H Leibson

#### High-level-language and ICE debugger supports 68040 µP

Huntsville Microsystems has added a  $68040\text{-}\mu\text{P}$  mode¹ to its HMI-200 series of in-circuit emulators (ICEs). The emulator provides zero-wait-state real-time emulation for 68040, 68EC040, and 68LC040  $\mu\text{Ps}$  operating at speeds as fast as 25

MHz. The emulator offers four break and trigger points that you can individually configure to respond to address, data, or status bit patterns, or to events monitored by 16 external trigger inputs. The ICE hardware is closely coupled to the Sourcegate high-levellanguage debug software. You can buy versions of the product for IBM-compatible PCs and Apollo and Sun workstations. The Sourcegate software supports C, Pascal, and Ada compilers from most of the major compiler suppliers. The emulator with Sourcegate costs \$25,000 for PCs and \$26,000 for workstations. Huntsville Microsystems Inc, Huntsville, AL, (205) 881-6005, FAX (205) 882-6701.—Maury Wright

# 10-bit converters fill in gaps in performance

Although vendors initially seemed to skip over 10-bit converters in migrating from 8 to 12 bits and up, they now are continuing to fill in the cracks. Texas Instruments and Analog Devices have both announced 10-bit devices for two entirely different applications. Texas Instruments' TLC1550IFN is a low-cost (\$6.27 (1000)) successiveapproximation converter with a 10-bit bus that requires just one read instruction to retrieve the conversion result. This feature

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Products bearing the SPARC trademark are based on an architecture developed by Sun Microsystems, Inc.

eases the read requirements of microprocessor peripheral applications because earlier 10-bit converters had only an 8-bit bus requiring two read cycles to retrieve the 10-bit result. The device's 3-state parallel port lets it interface directly with most DSP  $\mu$ Ps and  $\mu$ P system data buses. The IC converts in 6  $\mu$ sec and dissipates 10 mW.

On the other end of the speed scale, Analog Devices' AD773 can take 18 Msamples/sec. It is optimized for video applications, featuring typical differential gain and phase specifications of 0.4% and 0.2°, respectively. The \$55 (100) device features a fast-settling track-and-hold amplifier, high-impedance reference input, and CMOS/TTL-compatible outputs. The typical S/N plus distortion ratio is 56 dB for 1-MHz sine-wave inputs. The device typically dissipates 1.2W. Analog Devices Inc, Norwood, MA, (617) 329-4700, FAX (617) 821-4273. Texas Instruments, Dallas, TX, (800) 336-5236, ext 3990; (214) 995-6611, ext 3990.

-Anne Watson Swager

## DSP World call for papers

DSP Associates has issued a call for papers for the "International Conference on Signal Processing Applications and Technology & DSP World Expo." The conference will take place at the Hyatt Regency in

Cambridge, MA, November 2 to 5, 1992. The 400word papers should address DSP-based applications and technology, including telecommunications, speech processing, image processing, control systems, automotive engineering, VLSI and DSP architectures, radar and sonar applications, consumer electronics, and other applications. The deadline for submitting papers is April 30, 1992. DSP Associates, 18 Peregrine Rd, Newton Centre, MA 02159, (617) 964-3817, FAX (617) 969-6689.—Susan Rose

#### Multiple wire backplanes trim board size

I-Con Industries's Multiwire Futurebus + backplanes reduce the weight and thickness of interconnections in high-speed digital applications. By using 4-mil-diameter wires rather than etched circuits for routing signals, a multiple-wire board looks, feels, and solders like a multilayer board.

Each wire is coated with 1.2 mils of polyimide insulation, which lets the wires cross over one another without requiring physical separation. As a result, you can reduce a 3-to 5-layer multilayer board to a single-plane multiple-wire board. Depending upon impedance specs, you can reproduce a typical 20-layer board of stripline construction as a 0.062-in. Multiwire card, resulting in

as much as a 40% reduction in board thickness.

Standard multiple-wire backplanes come in Future-bus + A, B, and F profiles, with data widths of 64 and 128 bits. Available in 5-, 9-, and 14-slot configurations, a standard 14-slot backplane sells for \$2800. You can also order custom sizes. I-Con Industries Inc, Euless, TX, (817) 283-5361.—J D Mosley

# Chip speeds FFT frequencydomain processing

The a66311 Reconfigurable Array Store operates at 40 MHz and processes frequency-domain data sets at a rate of 400-million operations/sec for 2k complex words and smaller FFTs. The chip's I/O bandwidth can support

data rates for real-time processing of signals clocked at tens of megahertz. You can cascade this multiport ASIC memory chip for higher throughput. The IC has 64 bits of pipelined static RAM that you can configure as four  $1k \times 16$ -bit, two  $1k \times 32$ -bit, two  $2k \times 16$ -bit, or one  $2k \times 32$ -bit memories.

The ASIC is the most recent installment in the company's \$1340 (1000) DSP chip set, which comprises one digital-array signalprocessor, one programmable-array controller, and three reconfigurable data arrays. The chip set performs 1-kbyte complexpoint FFTs with a doublebuffered I/O and 2-kbyte complex-coefficient store. Array Microsystems Inc, Colorado Springs, CO, (719) 540-7999.

—JD Mosley

## Tools and testers tackle dense pc boards

A suite of hardware and software products from Teradyne Inc meets the challenges of what the firm calls RCT (reduced-contact testing) of high-density pc boards with limited nodal access—especially those populated by surface-mount devices and complex ASICs. Three testers, the 576-channel L323RCT and L353RCT and the 1152-channel L357RCT, test at clock rates to 40 MHz, perform combinational (functional and in-circuit) testing, and provide much deeper pattern memory than traditional board testers. The systems use VXIbus modules to implement analog functions. The \$400,000 base-price L323RCT is much smaller and less expensive than earlier systems; system prices top out at about \$1 million.

Accompanying the testers are several software packages that run on DEC VAXstations speed up functional-test development and provide accurate diagnostics for boards despite limited nodal access. A package for Mentor workstations produces test vectors during board design. Teradyne Inc, Boston, MA, (617) 422-3567, FAX (617) 422-3440.—Dan Strassberg

# Why Settle for ½ an '040 Board?

You've chosen the '040 because you need maximum performance in your VME system. But look carefully, because other Single Board Computers may only give you only half of what you expected from the '040.

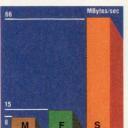
Compare Synergy's SV430 performance to any other SBC. Compare bus speed, MIPs, support, flexibility, documentation, reliability, I/O intelligence or any spec you can think of. We think you'll find the same thing we did—the

SV430 outperforms every other SBC on the market by as much as 150%.

Surprisingly, this kind of quality won't cost you any extra, because Synergy products lead in another important area—value. At Synergy, you don't have to pay a premium price for premium performance.

Let us show you just how far ahead your system can be with a Synergy processor board. Call us today, and get the *whole* '040 story.

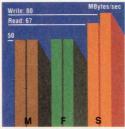
### Compare our specs. Synergy is superior across the board!



#### VME Transfers

VME64 doubles bus performance to 66 MB/s—and the SV430 is the only '040 board that has it. But we don't need VME64 to win this comparison.

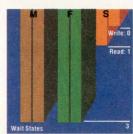
Even normal 32-bit transfers race at 33 MB/s. That's 200% faster than Force or Motorola.



#### DRAM Burst Rates

A 25 MHz '040 is capable of accessing memory at 80 MB/s. The closer you are to this maximum, the more '040 perform-

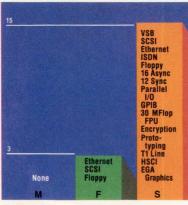
ance you're gaining. SV430 bursts are 26% faster than Force and Motorola.



#### DRAM Random Accesses

Non-burst '040 performance is measured in wait states. Fewer wait states mean higher performance. The SV430 is not only 66%

faster than Force or Motorola, it supports twice the on-board memory — 32 MB.

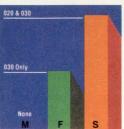


#### I/O Modules

Synergy's EZ-Bus modules are compatible with our entire line of SBCs. This means Synergy's current line of 12 intelligent I/O modules are immediately available for the SV430—today. No other vendor comes close for selection, functionality or availability.

Data from Motorola MVME165 data sheet dated 2/90, and Force CPU-40 data sheet A1 Rev. 1. DRAM measurements shown are with parity. VMEbus transfers are to a 60ns slave.

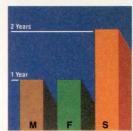
VME64 is a trademark of Performance Technologies, Inc



#### '020/'030 Compatibility

Software compatibility between Synergy SBCs means users have simple upgrades to the SV430 from our '020 and

'030 SBCs. Force offers compatibility only from the '030 level, and Motorola offers "upward migration"—a polite phrase that means rewriting your code.



#### Product Warranty

Synergy backs the reliability of its SBCs with a two year standard warranty. Force and Motorola only offer you one.



# FLIFRS



# dc to 3GHz from \$1145

### lowpass, highpass, bandpass

- less than 1dB insertion loss greater than 40dB stopband rejection surface-mount BNC, Type N, SMA available
- •5-section, 30dB/octave rolloff •VSWR less than 1.7 (typ) •rugged hermetically-sealed pin models •constant phase
  - meets MIL-STD-202 tests
     over 100 off-the-shelf models
     immediate delivery

#### low pass, Plug-in, dc to 1200MHz

Model No.	Passband MHz loss < 1dB	Stopbar loss > 20dB	nd, MHz loss > 40dB	Model No.	Passband MHz loss < 1dB	Stopba loss > 20dB	nd, MHz loss > 40dB
PLP-5 PLP-10.7 PLP-21.4 PLP-30 PLP-50 PLP-70 PLP-90 PLP-100 PLP-150 PLP-200	DC-5 DC-11 DC-22 DC-32 DC-48 DC-60 DC-81 DC-98 DC-140 DC-190	8-10 19-24 32-41 47-61 70-90 90-117 121-137 146-189 210-300 290-390	10-200 24-200 41-200 61-200 90-200 117-300 167-400 189-400 300-660 390-800	PLP-250 PLP-300 PLP-450 PLP-550 PLP-600 PLP-750 PLP-800 PLP-800 PLP-1000 PLP-1200	DC-225 DC-270 DC-400 DC-520 DC-680 DC-700 DC-720 DC-760 DC-900 DC-1000	320-400 410-550 580-750 750-920 840-1120 1000-1300 1080-1400 1100-1400 1340-1750 1620-2100	400-1200 550-1200 750-1800 920-2000 1120-2000 1300-2000 1400-2000 1750-2000 2100-2500

Price, (1-9 qty), all models: plug-in \$14.95, BNC \$32.95, SMA \$34.95. Type N \$35.95

#### Surface-mount, dc to 570 MHz

SCLF-21.4	DC-22	32-41	41-200	SCLF-190	DC-190	290-390	390-800
SCLF-30	DC-30	47-61	61-200	SCLF-380	DC-380	580-750	750-1800
SCLF-45	DC-45	70-90	90-200	SCLF-420	DC-420	750-920	920-2000
SCI F-135	DC-135	210-300	300-600				

Price, (1-9 qty), all models: \$11.45

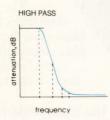
#### Flat Time Delay, dc to 1870 MHz

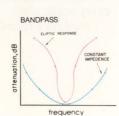
	Passband MHz	Stopt MH			WR ge, DC thru	Group Delay Variations, ns Freq. Range, DC thru				
Model	loss < 1.2dB	loss	loss	0.2fco	0.6fco	fco	2fco	2.67fco		
No.		>10dB	> 20dB	X	X	X	X	X		
PBLP-39 PBLP-117 PBLP-156 PBLP-200 PBLP-300 PBLP-467	DC-23	78-117	117	1.3:1	2.3:1	0.7	4.0	5.0		
	DC-65	234-312	312	1.3:1	2.4:1	0.35	1.4	1.9		
	DC-94	312-416	416	0.3:1	1.1:1	0.3	1.1	1.5		
	DC-120	400-534	534	1.6:1	1.9:1	0.4	1.3	1.6		
	DC-180	600-801	801	1.25:1	2.2:1	0.2	0.6	0.8		
	DC-280	934-1246	1246	1.25:1	2.2:1	0.15	0.4	0.55		
	DC-560	1866-2490	2490	1.3:1	2.2:1	0.09	0.2	0.28		
	DC-850	3740-6000	5000	1.45:1	2.9:1	0.05	0.1	0.15		

Price, (1-9 qty), all models: plug-in \$19.95, BNC \$36.95, SMA \$38.95, Type N \$39.95 NOTE: ▲ -933 and -1870 only with connectors, at additional \$2 above other connector m

frequency

LOW PASS





#### high pass, Plug-in, 27.5 to 2200 MHz

Model No.		lband Hz loss < 20dB	Passband MHz loss < 1dB	VSWR Pass- band Typ.	Model No.		band Hz loss < 20dB	Passband MHz loss < 1dB	VSWR Pass- band Typ.
PHP-25 PHP-50 PHP-100 PHP-150 PHP-175 PHP-200 PHP-250 PHP-300	DC-13 DC-20 DC-40 DC-70 DC-70 DC-90 DC-100 DC-145	13-19 20-26 40-55 70-95 70-105 90-116 100-150 145-170	27.5-200 41-200 90-400 133-600 160-800 185-800 225-1200 290-1200	1.8:1 1.5:1 1.8:1 1.8:1 1.5:1 1.6:1 1.3:1 1.7:1	PHP-400 PHP-500 PHP-600 PHP-700 PHP-800 PHP-900 PHP-1000	DC-210 DC-280 DC-350 DC-400 DC-445 DC-520 DC-550	210-290 280-365 350-440 400-520 445-570 520-660 550-720	395-1600 500-1600 600-1600 700-1800 780-2000 910-2100 1000-2200	1.7:1 1.8:1 2.0:1 1.6:1 2.1:1 1.8:1 1.9:1

Price, (1-9 qty), all models: plug-in \$14.95, BNC \$36.95, SMA \$38.95, Type N \$39.95

#### bandpass, Elliptic Response, 10.7 to 70 MHz

	Center	Passband	3 dB	Sto	opbands
Model No.	Freq. (MHz)	I.L. 1.5 dB Max. (MHz)	Bandwidth Typ. (MHz)	> 20dB at MHz	> 35dB at MHz
PBP-10.7 PBP-21.4 PBP-30 PBP-60 PBP-70	10.7 21.4 30.0 60.0 70.0	9.6-11.5 19.2-23.6 27.0-33.0 55.0-67.0 63.0-77.0	8.9-12.7 17.9-25.3 25-35 49.5-70.5 68.0-82.0	7.5 & 15 15.5 & 29 22 & 40 44 & 79 51 & 94	0.6 & 50-1000 3.0 & 80-1000 3.2 & 99-1000 4.6 & 190-1000 6.0 & 193-1000

Price, (1-9 qty), all models: plug-in \$18.95, BNC \$40.95. SMA \$42.95. Type N \$43.95

#### Constant Impedance, 21.4 to 70 MHz

Model No.	Center Freq.	Passband MHz loss < 1dB	Stopband loss > 20dB at MHz	VSWR 1.3:1 Total Band MHz
PIF-21.4 PIF-30 PIF-40 PIF-50 PIF-60 PIF-70 PIF-70	21.4 30 42 50 60 70	18-25 25-35 35-49 41-58 50-70 58-82 models; pluc	1.3 & 150 1.9 & 210 2.6 & 300 3.1 & 350 3.8 & 400 4.4 & 490	DC-220 DC-330 DC-400 DC-440 DC-500 DC-550

BNC \$36.95. SMA \$38.95. Type N \$39.95

CIRCLE NO. 20

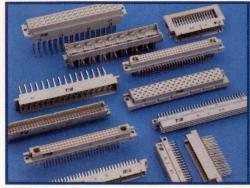
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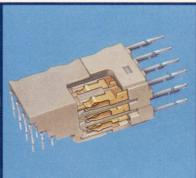
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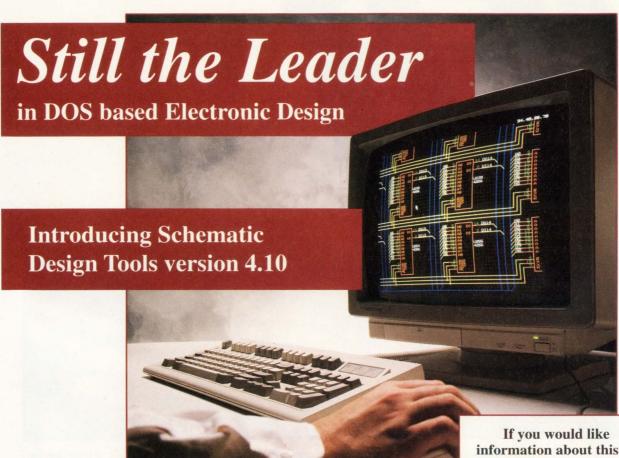
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#### **EDN-SIGNALS & NOISE**

### "Cookbook" formulas aren't always reliable

The article, "Phase compensation extends op amp stability and speed" (EDN, September 16, 1991, pg 181), left its analytical path when it discussed the standard approach used for driving capacitive loads (Fig 2). "Cookbook" formulas don't provide understanding, and many times lead to problems.

You can analyze the circuit as follows: Recognizing there are in fact two feedback loops, it's simpler to analyze them one at a time. Replacing  $R_2$  and  $R_1$  with their Thevenin equivalents gives a  $\beta$  network with a gain of -6 dB and an impedance of  $R_{eq} = R_1 \tau R_2$ , or  $5 \text{ k}\Omega$  (Fig A). The op amp is now easily recognizable as a standard Miller integrator whose unity-gain frequency is given by  $\frac{1}{2}\pi R_{eq}C_C$  (Fig B).

Now, you can analyze the outer loop, using the equivalent op amp just discussed (Fig C).  $R_{\rm C}$  does in fact decouple the load from the op amp, but it also introduces a pole with  $C_{\rm L}$ . You must position this pole far enough away so that the  $1/\beta$  curve intersects the open-loop-gain curve before it starts falling at -12 dB/octave, due to the second pole. Fig D shows the plot for the properly compensated amplifier.

Using this analysis provides much more insight into the operation of the circuit and removes much of the need for empirical development.

Herb Perten
Phillips Scientific
Mahwah, NJ

(Author's reply): Herb Perten's analysis adds useful insight into this phase compensation technique. However, the analysis neglects the output impedance that forces the empirical analysis.

This occurs in the step between Fig C and Fig D. There, derivation of  $f_p = \frac{1}{2} R_c C_L$  neglects the amplifier

output resistance,  $R_0$ . As mentioned in the article, this cannot be done for the level of  $R_0$  normally used with this phase compensation. I'm afraid we are stuck with the empirical analysis.)

### Two makers of DSP boards not mentioned

Two firms that make DSP coprocessor boards were inadvertently omitted from the Special Report on pg 108 in the September 16, 1991, issue of EDN:

Pentland Systems Ltd 1 Cochrane Sq, Brucefield Park, Livingston W Lothian EH54 9DR, Scotland Phone (506) 464666 FAX (506) 463030

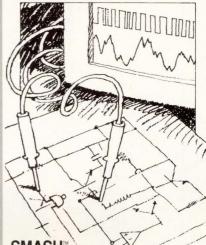
In the US: GD California Inc 5627 Stoneridge Dr, Suite 301 Pleasanton, CA 94588 Phone (510) 847-9660 FAX (510) 847-9663

Ziatech, the other firm, manufactures a 56001-based DSP coprocessor board for the STD-32 bus: Ziatech Corp 3433 Roberto Ct San Luis Obispo, CA 93401 Phone (805) 541-0488 FAX (805) 541-5088

#### HAVE YOUR SAY

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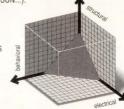
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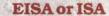
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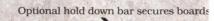
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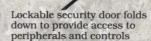
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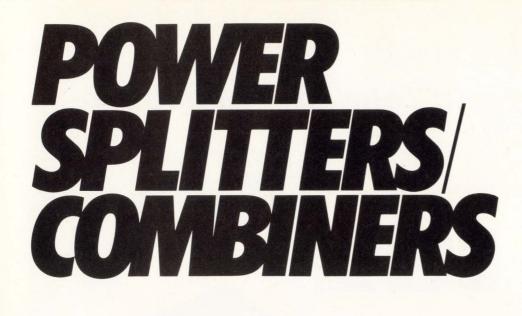
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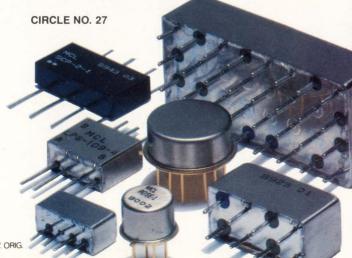
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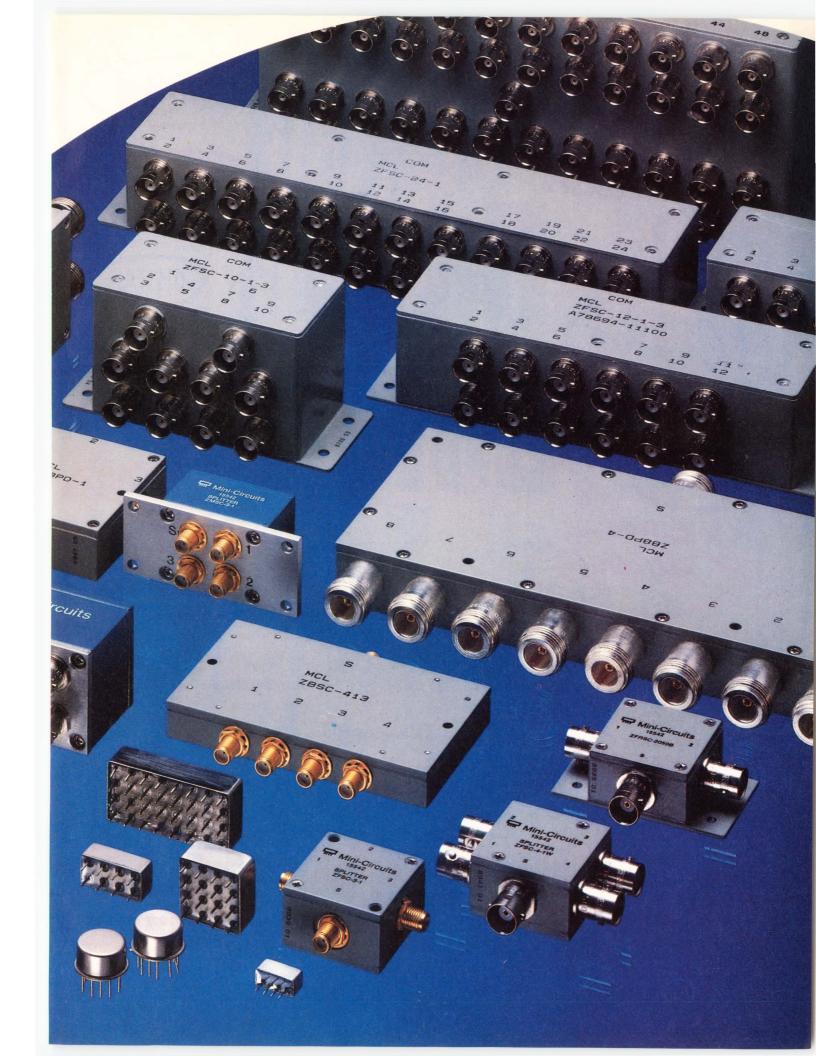
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**CIRCLE NO. 28** 

#### ASK EDN

#### **EDITED BY JULIE ANNE SCHOFIELD**

#### Once again, a reader is stumped for spare parts

I have an in-house test system that uses a number of Signetics S8233 quad digital multiplexers. Raytheon also made this part as an RM8233. Signetics has sold the rights to Lansdale, who will manufacture the part for me for \$45 each, with a minimum buy of 675 parts. This seems excessive for spare parts. I could use one or two dozen. Can you help locate some somewhere? Clancy Sloan Maxwell Laboratories Inc San Diego, CA

Please contact Ask EDN if you have any 8233s you can spare.

#### Of mice and standards

We are working on a new type of mouse interface and are having trouble finding any industry standard protocols, or even finding out if any exist. We think we would like our product to be Microsoft Mouse compatible, but we can't seem to find anyone who can define the protocols. Is it possible that mouse interfaces are defined by whomever is making the mouse?

Jim Fletcher President Gaslight Video Orange, CA

Mice vendors reverse-engineer either Microsoft's hardware interfaces (bus or serial) or the write drivers that emulate Microsoft's mouse driver. In either case, there's no standard other than the de facto, largely undocumented standards originated by Microsoft.

The best reference we've seen is Logitech's *Technical Reference Manual* for its mouse products. Corporate head-quarters is

Logitech Inc 6505 Kaiser Dr Fremont, CA 94555 (415) 795-8500.

#### Readers dispute B in BNC

So far, half a dozen readers have written regarding the item about what BNC stands for in the January 2, 1992, Ask EDN. Michael W LaBoone of WYFF

Inc (Greenville, SC), Jim Stewart of J K Microsystems (San Pablo, CA), Marc Ressler of Harry Diamond Lab Radar (Adelphi, MD), and Tom Reyenga of Tinker Air Force Base (Oklahoma City, OK) all agree that the N stands for Paul Neill and the C stands for Carl Councelman. The four also insist that the B stands for bayonet—not baby. In fact, Stewart says that he can't imagine that two men who made such a classy connector that it lasted 40 years would use the term "baby" to describe it.

Reyenga gave the best argument for why the B is for bayonet: "As you wrote, the N and C stand for Neill and Councelman's connectors. The smaller version, however, had two types that were different in their fastening techniques. One was like most large connectors and was threaded. It was identified as a TNC connector—a threaded small NC type connector. The other had a single push-twist fastening method similar to some bayonet techniques, and so became a BNC connector." However, we're not ready to concede defeat until we hear from Neill or Councelman ourselves.

Also, thanks go to George Barnard of Fairchild Space/WTSC (Greenbelt, MD) for referring us to the dictionary for the proper pronunciation of the prefix "giga" and leaving us with no doubt as to how to pronounce his first name. And thanks to Robert H Bushnell of the Metric Practice Committee of the US Metric Association for alerting us to his group's specified pronunciation of riggs.

For the record, we at EDN are perfectly aware that the "official" pronunciation for "giga" is jig-ah, not gig-ah. But the official pronunciation is not everyone's pronunciation. Similarly, many Americans say kuh-lom'-eter instead of the official kilo-meter.

Further, we know that capital K means kelvin (not kilo), but to avoid confusion, we append an unauthorized degree symbol, °K, to avoid confusion. And the "official" abbreviation for seconds is "s," which we render as "sec."

#### More missing parts

I am looking for a microprocessor from Texas Instruments, the SBP9989. This chip was popular some 10 years ago. For a special project we need to have one SBP9989, but TI can't deliver them anymore. I checked with the local Texas Instruments office and with the headquarters of TI in Europe, but they assured me that this microprocessor is not available anymore. Does anyone know where I can get one or more?
Jeroen van der Wateren
Project Engineer
Chess Engineering BV
Haarlem, The Netherlands

How 'bout it, readers?

## Searching for a heavyweight sensor

I'm looking for information about weight sensors. More specifically, I am looking for a weight sensor that detects in the 500- to 1000-lb range with  $\pm$  10-lb accuracy. The sensor's measurements would have to be repeatable.

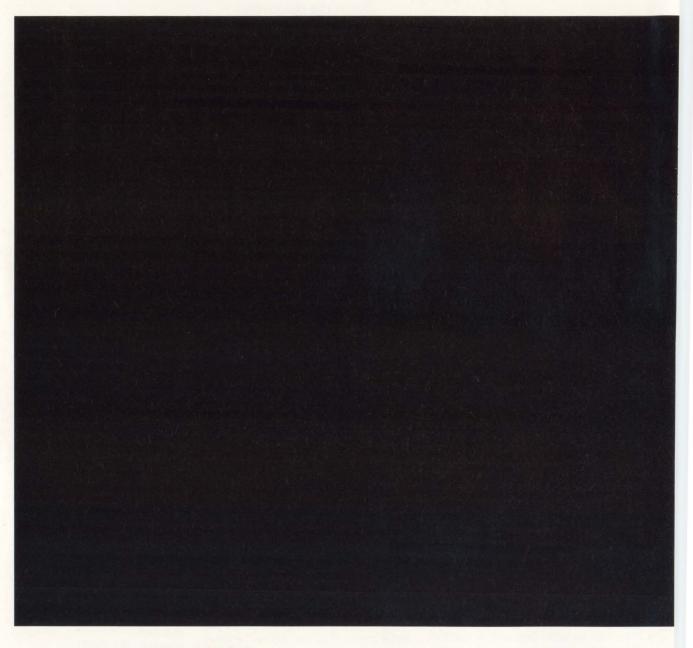
Larry Woods Moline, IL

Although there may be other types of transducers that measure weight, what you're probably looking for is a load cell. Load cells are units containing straingauge bridges. You will also need a signal conditioner to provide the excitation to the gauge and to amplify its output. And you'll probably need an A/D converter (usually an integrating type of ADC) to convert the amplifier's output into numeric readings. Specialized digital panel meters combine the signal-conditioning and ADC functions with a display. The following are two companies that offer such meters:

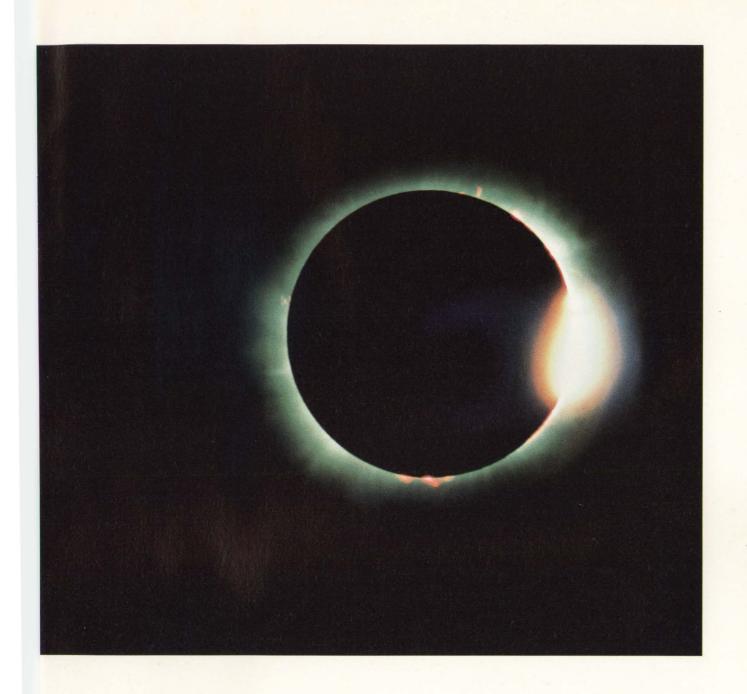
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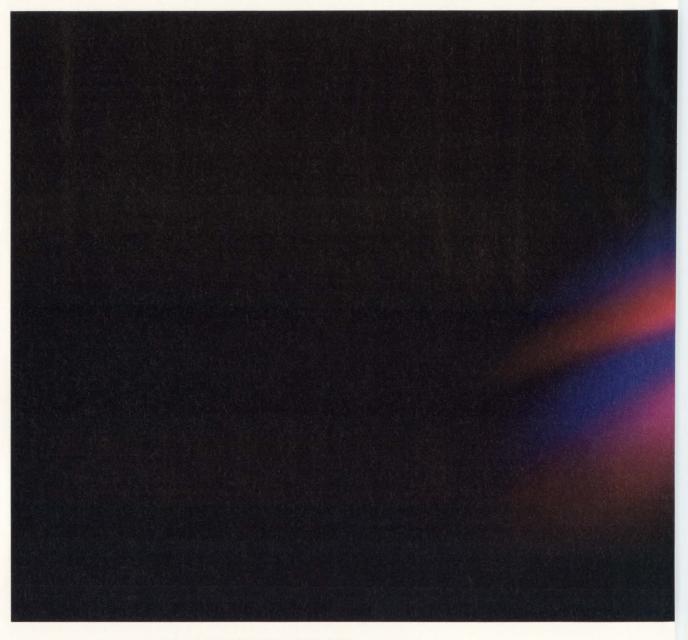
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- On-Chip Cache Control For separate external instruction & data caches of up to 256KBytes each.
- ☐ **Five-stage pipeline** Closely approaches execution rate of one machine cycle per instruction.
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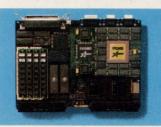
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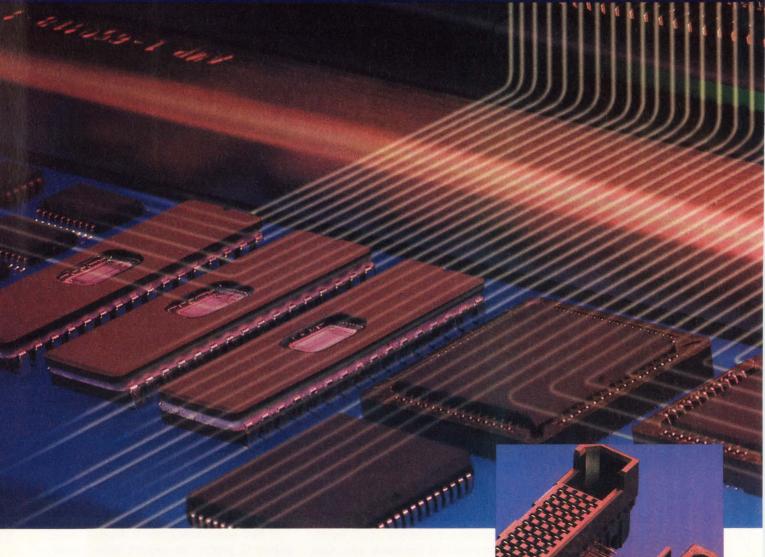


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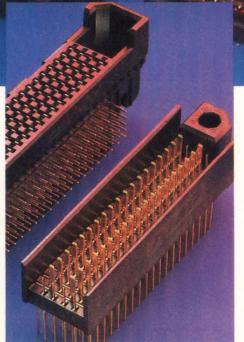
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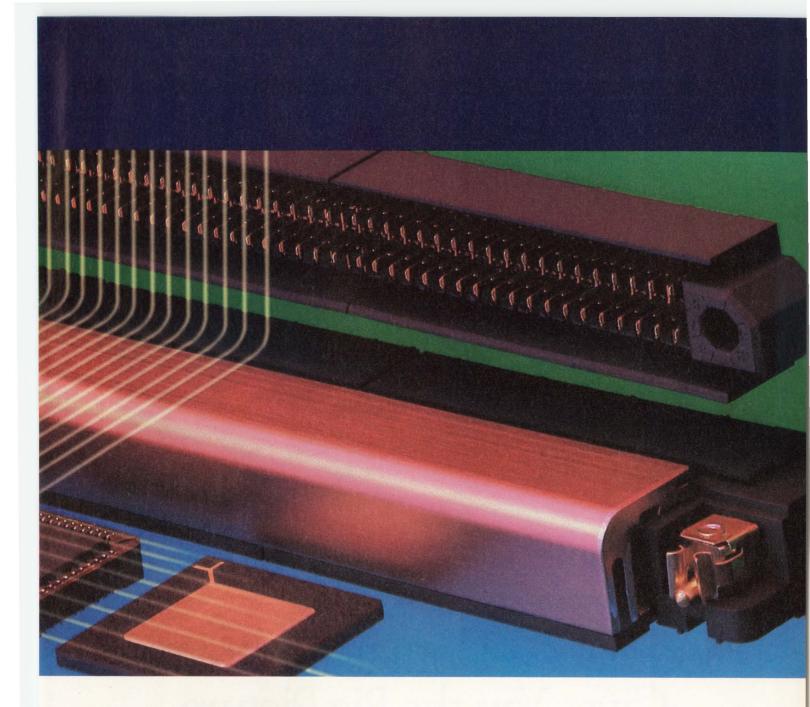
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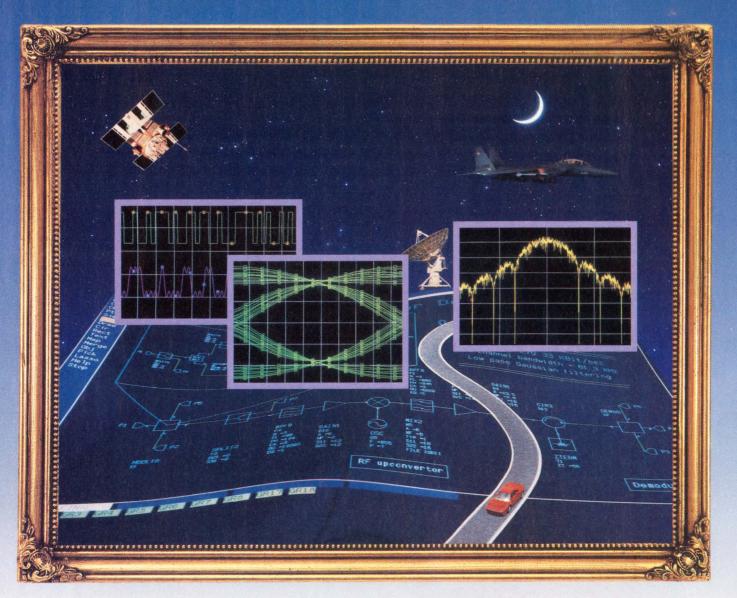
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Breaking the Barriers...



CIRCLE NO. 41

## Shareware and freeware are only a phone call away

CHARLES H SMALL, Senior Technical Editor



In sharp contrast to the cornucopia of shareware and public-domain software (freeware) available for every other application area, electrical-engineering shareware and freeware are in short supply.

Unlike business and recreational software, you hardly ever get something for nothing when it comes to electricalengineering software. The lack of engineering shareware and freeware is surprising when you consider the altruistic torrent of free programs that flowed among engineers upon the advent of programmable scientific calculators in 1974. Inexplicably, as electrical engineers do more and more of their work on computers, they don't seem to be sharing software. Instead, engineers must pay high prices for commercial versions of the specialized software they need to do their jobs.

Other segments of computing support bulletin-board systems (BBSs) that carry literally tens of thousands of shareware and freeware programs. You can access electronic bulletin boards directly via voice-grade phone lines if you have a personal computer and a modem.

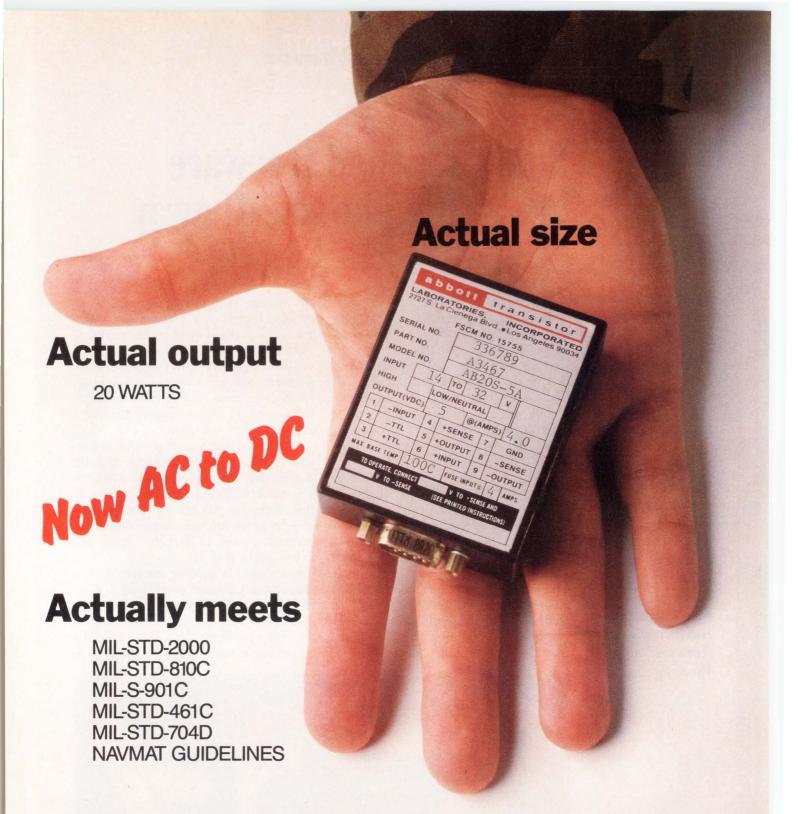
Or you can post messages and files to bulletin boards over commercial, voicegrade, or packet-switching networks.

Among the welter of programs posted on BBSs, engineers can find lots of management software—project planning, scheduling, time keeping, and billingbut not much professional-quality engineering-design software.

Public-domain software and shareware both appear on computer bulletin boards, but the two classes of software are quite different. Freeware is just that; software you can use for free and give away to anyone. Some significant programs, such as Berkeley Spice, are in the public domain.

Shareware is another matter. A true shareware package comprises a complete program and documentation that shareware authors distribute for free (charging perhaps only a nominal media fee) in ready-to-run form. One major ad-





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#### ENGINEERING SHAREWARE AND FREEWARE

vantage of shareware is that you get to try the program before buying it. Shareware is not free; if you like the shareware, you are supposed to send the author a "registration" fee. In other words, shareware works on the honor system.

Small software companies without the wherewithal to market their products through retail or professional channels depend primarily on a community of enthusiastic users who like to pass software around. Electronic bulletin boards provide the primary medium of exchange for such software, although specialized shareware distributors also exist. One distributor who specializes in technical software is Sector Systems Co (416 Ocean Ave, Marblehead, MA 01945, (617) 639-2625).

Intermittent "networks" link many of the computer enthusiasts' dial-up bulletin boards. You can post a message or file on one bulletin board, and then that bulletin board will automatically dial up other bulletin boards and may pass along your message or file. These bulletin boards can later spread your message or program even further.

Electronic bulletin boards also host lively computer conferences. Some of these conferences are on technical subjects such as artificial intelligence, computer languages such as C and Forth, and engineering tools such as scientific calculators and Spice. Conferees exchange tips and help each other solve problems. For those unable to attend professional conferences in person, electronic conferences can prove vital for professional development.

Despite the advantages of free software and professional help, engineers do not frequent computer bulletin boards. Apparently, engineers lack either the impulse or the means to share software. Given that knockoff modems are selling for \$50, the means are easy to acquire.

Maybe engineers—or their employers—are prejudiced against shareware and freeware. Such prejudices are unfounded. Just like commercial software, some shareware is very bad, but some is very good. In fact, many authors wrote their shareware programs to make up for deficiencies in commercial products. Maybe some users prefer to have a large company support the software that they buy and are put off by the one-man-shop aura of shareware.

#### Going into business

Suppose you have a hoard of software and are seized by the impulse to share it with the world. Shareware professionals advise prospective authors to consider carefully whether to release software as freeware or as shareware. If you release a program as shareware, you become, in effect, a small software company. If your software is not complete and professional, users will not adopt it. If you have crippled your shareware in an effort to force users to register or are not prepared to support your shareware, the word will quickly get around the BBSs and your program will be shunned. Releasing your program to the public domain relieves you of the responsibility of marketing and supporting it.

If you do develop a good program and are prepared to support it in a professional manner, the hordes of enthusiasts lurking around BBSs will be waiting to snap it up. Most BBSs charge for connection time. However, users who upload files usually get some free connection time. Therefore, enthusiasts will spread your shareware around even if they don't have the slightest idea what it is for. Still, you should post your offering on several major BBSs and send it to shareware resellers. which advertise in the back pages of computer magazines. Then expect

to wait at least a year and a half before registration fees begin rolling in.

This article cannot possibly list all electronic bulletin boards—literally tens of thousands exist. Ref 1 is a comprehensive, exhaustive guide not only to shareware, but also to communications software, selected electronic bulletin boards, and major BBS conferences. Refs 2 and 3 are additional sources of shareware and BBSs.

The free EDN BBS ((617) 558-4241,300/1200/2400,8,N,1) is fast becoming the premier electronic bulletin board for electrical-engineering shareware. The EDN BBS is also a gathering place for engineers who are contributing to public-domain libraries of software in a variety of areas, including DSP, CAE, Spice, scientific calculators, and fuzzy logic.

The EDN BBS has a forum called soapbox for expressing opinions as well as a mailbox for posting and answering questions to EDN's popular *Ask EDN* column. The EDN BBS also hosts design round tables where engineers participating in reader-supported projects can exchange design tips as well as hardware and software solutions.

#### References

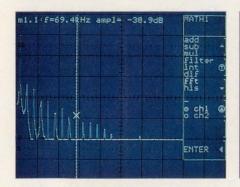
- 1. Callahan, Mike and Nick Anis, *Dr File Finder's Guide to Shareware*, Osborne McGraw-Hill, Berkeley, CA, 1991, ISBN 0-07-881646-7, 1019 pgs, \$39.95. Sample shareware programs on disk included.
- 2. The Alternative Software Bulletin (general-purpose shareware source), Binary Press, Box 757, Brooklyn, MI 49230.
- 3. *INFO-MAT Magazine* (BBS compendium), BBS Press Services Inc, 8215 SW 21 St, Topeka, KS 66615. Phone (913) 478-3157. BBS (913) 478-3088.

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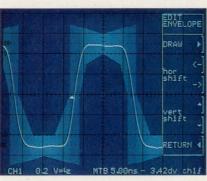
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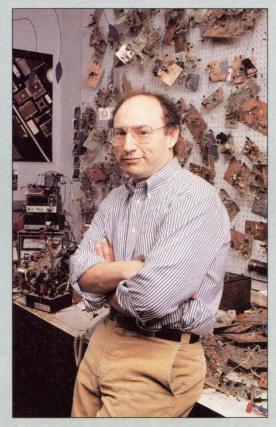
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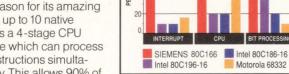
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#### **Communications Technology**

## Opposing groups struggle to define standards for FDDI using copper wire

DAVE PRYCE, Technical Editor



Although implementation of the Fiber Distributed Data Interface over twisted-pair copper wiring is not yet a reality, the ANSI X3T9.5 committee may soon resolve the conflicting issues.

Originally conceived about 10 years ago, the Fiber Distributed Data Interface (FDDI) has evolved into a completely specified set of operating parameters and protocols and a standardized group of components and equipment. (Although the benefits of FDDI are well known, the reader may want to refer to **Refs 1** and **2** for detailed information on the complete FDDI system and some representative components.) As specified by the X3T9.5 committee

of the American National Standards Institute (ANSI), an FDDI LAN can extend over a circumference of 100 km while connecting as many as 500 nodes in 2-km spacings. Of even greater importance in this age of busy networks, an FDDI LAN speeds data along at 100 Mbps.

In contrast with the high-speed capability of FDDI, Ethernet (IEEE 802.3) operates at only 10 Mbps, and Token Ring

(IEEE 802.5) operates at 4 or 16 Mbps. Moreover, Ethernet and Token-Ring LANs are limited to distances of 2.5 and 1.2 km and node spacing of 0.5 and 0.46 km, respectively. Despite these obvious disadvantages, Ethernet and Token Ring have an extremely powerful advantage—they both can operate over twisted-pair copper wire.

Actually, Ethernet has several options for transmission media, including 10Base-2 for thin coaxial cable, 10Base-5 for thick coaxial cable, 10Base-T for un-

shielded twisted pair (UTP), and 10Base-F for fiber cable. However, most Ethernet LANs use either thin coaxial cable (RG-58) or UTP. Token Ring uses either shielded twisted pair (STP) or UTP. IBM has a large installed base using STP.

Most office buildings and factories have a huge installed base of LANs using UTP and STP that company executives are reluctant to scrap. The complexity and cost of installing optical



Implementing the company's Copper Distributed Data Interface (CDDI), Crescendo Communications' Model 1000 Workgroup Concentrator allows FDDI transmission at 100 Mbps over unshielded twisted-pair wiring.

FDDI is usually prohibitive. For these reasons, the ANSI X3T9.5 committee has been struggling to define a standard for FDDI using twisted-pair wiring. For reference, Fig 1 shows the basic FDDI configuration, which uses counter-rotating dual rings. Although significant differences exist, the topology is essentially compatible with the IEEE 802.5 Token-Ring standard.

The first proposed standard to the ANSI committee came from a group of companies that defined and published an



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#### IMPLEMENTING FDDI

open method for transmitting data at 100 Mbps over shielded twisted pair. These companies, referred to as "The Gang of Five," are Advanced Micro Devices (AMD), Chipcom Corp, Digital Equipment Corp (DEC), Motorola, and Synoptic Communications. Because of its large installed base, IBM quickly endorsed the STP concept.

The intent of the group was to provide interoperable products that could be quickly brought to market. Although all five companies agreed to endorse the eventual standard produced by the X3T9.5 committee, much of their original effort is moot in light of the latest proceedings.

More recently, the Unshielded Twisted-Pair Development Forum (UDF) proposed a standard that allows 100-Mbps transmission using unshielded twisted-pair wiring. Sometimes called "The Gang of Seven," these companies are Apple Computer, AT&T Microelectronics, British Telecommunications, Crescendo Communications, Fibronics International, Hewlett-Packard, and Ungermann-Bass. National Semiconductor has also expressed support for UDF.

#### Proposal satisfies STP and UTP

At several meetings held from August through December 1991, UDF presented preliminary research and test results. In the meeting held on December 10, 1991, UDF proposed that the TP-PMD (Twisted Pair-Physical Medium Dependent) working group draft an FDDI specification for both shielded and unshielded twisted pair, and recommended suitable encoding schemes.

The proposed schemes are MLT-3, for data-grade shielded and unshielded twisted pair, and CAP-32, for voice-grade unshielded twisted pair (also known as DIW), as the best choices for the standard. DIW is the designation for internal wiring that contains four pairs of un-

shielded twisted wires. The UDF intends to find a scheme that will support 100-Mbps data rates in accordance with the existing FDDI specification. Present goals are to provide

- Support for UTP DIW (voice grade) wiring at distances of 50 to 100 meters, compliant with FCC Part A.
- Support for UTP data-grade wiring at a minimum distance of 100m, compliant with FCC Part B.
   The principal key to satisfying

PR-4, 2B1Q has a dc component and has most of its energy spectrum lying below 32 MHz. Although more complicated than PR-4, 2B1Q has potential EMI advantages because of its lower-frequency energy spectrum.

3. CAP-32—(Carrierless Amplitude/Phase). A 2-dimensional scheme similar to QAM (Quadrature Amplitude Modulation). CAP-32 has six levels whose spectrum lies entirely between 0 and 30 MHz. Like 2B1Q, CAP-32 is more compli-

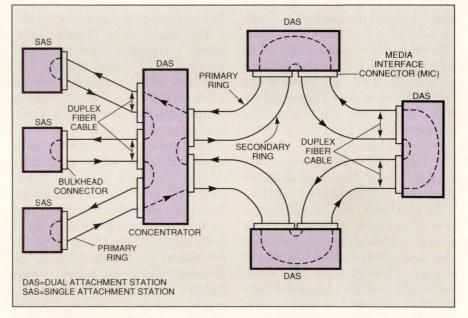


Fig 1—An FDDI network uses a counter-rotating dual ring that includes fault tolerance and the ability to accommodate both single-attachment and dual-attachment stations.

these objectives is the choice of an encoding scheme that can meet EMI specifications over the target distances. At various times, all of the following encoding schemes were candidates for use with FDDI over twisted pair:

- 1. PR-4—(Partial Response Class 4). A 3-level scheme whose energy spectrum has nulls at 0 and 62.5 MHz and an energy peak at 32.5 MHz. The advantage of PR-4 is its simplicity.
- 2. **2B1Q**—A technique that maps bit pairs into two levels, **2B1Q** is the line code specified for North American Basic Rate ISDN. Unlike

cated than PR-4 but has significantly better EMI characteristics. Considered a powerful code, CAP-32 is used by the telecommunications industry and is supported by AT&T Microelectronics. CAP-32, however, is the most complex of the schemes and potentially the most expensive to implement.

4. MLT-3—(Multi-Level Transitional). Although UDF member Crescendo Communications originally proposed the PR-4 scheme, it now supports MLT-3. According to Crescendo, MLT-3 provides 6 dB less EMI than does PR-4 and adequate FDDI performance over UTP

#### IMPLEMENTING FDDI

at lower cost. Moreover, because MLT-3 is essentially a 3-level form of the 2-level NRZI (non-return-to-zero-inverted) scheme, it may be able to use existing FDDI chip sets with the addition of only a few discrete components.

The reason for carefully choosing an appropriate encoding scheme is that the power needed to drive signals 100 meters over copper wire can generate EMI levels that far exceed FCC specifications. Standard FDDI transmission uses NRZI and 4B/5B encoding, which maps 4 bits of data to 5 bits of code to achieve a 100-Mbps data rate. Standard FDDI sends much of its information at frequencies between 30 and 80 MHz but, because the transmission is over fiber-optic cable, EMI is not a problem. The choice of MLT-3 and CAP-32 as the encoding schemes helps to alleviate the EMI problem inherent with copper wiring by minimizing the frequency content above 30 MHz.

In particular, MLT-3 offers several advantages. Among these are a very efficient power spectrum that keeps more than 80% of the energy below 30 MHz. MLT-3 exhibits EMI margins of greater than 6 dB below the FCC A limit on DIW and greater than 16 dB below on data-grade wiring.

#### Scrambling minimizes EMI peaks

Another problem not entirely eliminated by the choice of the encoding scheme is the existence of concentrated energy peaks. To minimize these peaks, designers often use scrambling to spread the signal more evenly throughout the encoding scheme's frequency spectrum. In tests conducted independently by AT&T, Crescendo, Hewlett-Packard, and Northern Telecom. scrambling reduced the spectrum peaks of NRZI, MLT-3, and PR-4 codes and cut EMI by 20 dB. Although scrambling multiplies errors by 2x, designers eliminate this ef-

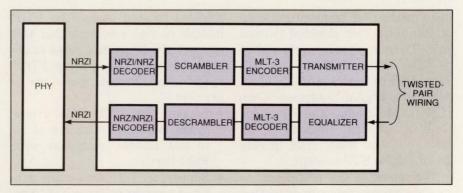


Fig 2—This functional block diagram illustrates a typical method for implementing the FDDI Physical Medium Dependent (PMD) protocol using scrambled MLT-3 coding over copper wire.

fect by raising the signal level 2.1 dB.

The Fig 2 block diagram illustrates a typical method for implementing the Physical Medium Dependent (PMD) protocol using scrambled MLT-3 coding. Such a method can use commercially available integrated circuits.

Customers are pushing chip manufacturers such as AMD, AT&T, Motorola, National Semiconductor, and Hewlett-Packard for decisions on producing the chips needed to support FDDI on twisted pair. However, the silicon suppliers are still at the mercy of the ANSI decision-making committee, which has yet to firmly establish an accepted standard. The next ANSI meeting, scheduled for February 1992, may resolve this issue. In the meantime, chip suppliers no doubt have silicon warming up on the back burner that can take advantage of the best-possible guess of the committee's thinking.

Exhibiting a singular dedication to supporting FDDI transmission over UTP, Crescendo Communications recently introduced its Workgroup Concentrator and an SBus adapter for use with Sun workstations called Copper Distributed Data Interface (CDDI). The technology allows 100-Mbps transmission over unshielded twisted-pair wiring. The CDDI-based products, which are compatible with current FDDI standards, passed inter-

operability tests at Advanced Micro Devices' Networking Test Center. CDDI meets FCC standards for class A applications over data-grade wiring as long as 100 meters.

Although the products are priced lower than fiber-optic hubs and adapter cards, their greatest advantage is their ability to use existing unshielded wiring rather than requiring the installation of expensive fiber-optic cables and connectors. You can also use the Workgroup Concentrator and CDDI SBus adapter with shielded twisted-pair wiring already installed for IBM Token-Ring LANs to upgrade from 16 to 100 Mbps.

The availability of 100-Mbps FDDI capability for STP and UTP will enable customers to take advantage of existing LANs and upgrade to FDDI without any change in the wiring infrastructure. Because most intelligent-network installations are unshielded, this capability will allow users to protect their current networking investments while providing a versatile, upward migration path.

Until now, the high cost of FDDI has restricted its use primarily to backbone applications, which link a number of lower-bandwidth LANs such as Ethernet and Token Ring. The use of UTP for FDDI networks will provide significant reductions in both wiring and component costs. In existing installations, system in-

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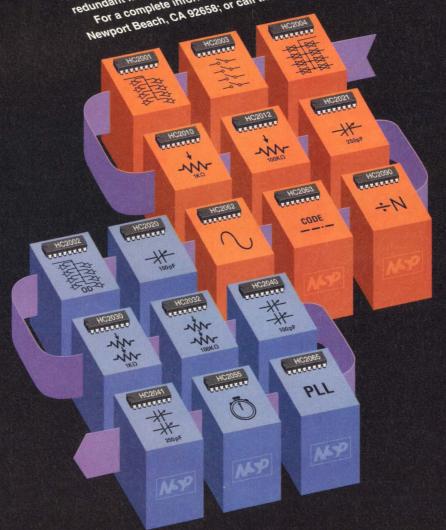
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#### IMPLEMENTING FDDI

tegrators will be able to simplify wiring and minimize costs by taking advantage of existing UTP wiring.

Proponents contend that, in new installations, the use of UTP wiring can provide as much as a 2× cost reduction compared with shielded twisted pair, and a 5× reduction compared with optical fiber. This reduction in wiring costs, together with savings at the component level, promises to make FDDI cost effective in PC and workstation LANs as well as the traditional backbone applications.

Taking the opposite tack to that of the twisted-pair working group, other ANSI X3T9.5 working groups are exploring low-cost alternatives to FDDI's fiber-based PMD (Physical Medium Dependent) layer. Relative to copper-based implementations, a low-cost fiber PMD offers several advantages, including longer transmission distances. As mentioned earlier, the twisted-pair PMD proposals currently under evaluation are limited

to distances of 50 to 100 meters. The low-cost fiber proposal currently under consideration would extend that distance to 500 meters.

Other advantages include greater EMI/RFI immunity, a higher level of security, and compatibility with existing FDDI PHY (Physical Layer) and MAC (Media Access Control) devices. The drive to develop a lower-cost, fiber-based PMD focuses on two key points: the cost of the fiber connector and the cost of the fiber-optic transceiver. So far, the most significant progress is the working group's selection of a low-cost alternative to the MIC (Media Interface Connector). The group also expects to achieve economies in transceiver costs because of the reduction of node distance from 2 km to 500 meters.

Exactly how all of these various proposals and current activities will shake out is not yet certain. It may be that a single approach will ultimately dominate. Much depends on the success of the various ANSI

working groups in attaining the best cost/performance tradeoff to satisfy the greatest number of users. One thing is clear, however. The benefits of FDDI performance will soon extend beyond backboneonly applications to PC and workstation LANs.

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- 2. Prvce, Dave, "Fiber-Optic Transceivers," *EDN*, March 1, 1991, pg 61.

Article Interest Quotient (Circle One) High 470 Medium 471 Low 472

#### For more information . . .

For more information on the FDDI activities discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following companies directly, please let them know you read about them in EDN.

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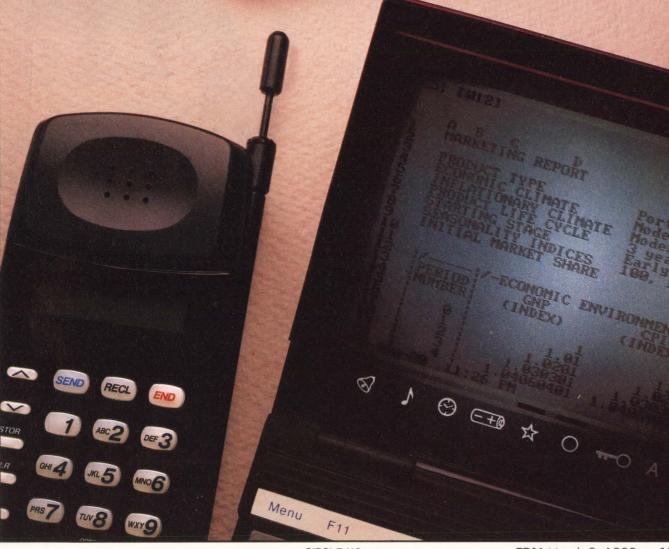
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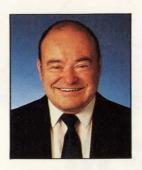
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DATA I/O

HIGH-SPEED-CPU DESIGN

## 40-MHz CMOS circuits send designers back to school

JOHN GALLANT, Technical Editor



CPUs that run at 40 and 50 MHz are forcing CMOS designers to amass ECL design techniques to make circuits that function in this ethereal realm. Microstrip, strip line, characteristic impedance, trace delays, matched-line terminations, and clock skew. If confronted with this list of terms, most CMOS designers working with 25-MHz or slower clock speeds would sing an old Fats Waller tune: "Never heard of such stuff." However, as CMOS-CPU speeds reach beyond 40 MHz, designers must learn techniques in which these terms are part of the common lexicon.

High-speed CMOS circuit design entails minimizing clock skew and transmission-line effects, eliminating extraneous noise and crosstalk, and managing heat dissipation. Fortunately, the nov-

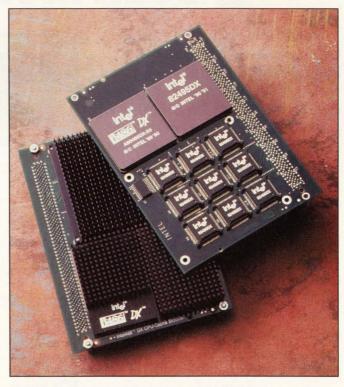
ice can take advantage of an array of advice and guidelines accumulated by high-speed designers in other technologies particularly ECL.

Everything changes for CMOS design at 40 MHz. High CPU speeds necessitate clocks having fast rise and fall times. Because a CPU initiates each event based on clock-edge transitions, slow rise and fall times increase the ambiguity of an event's time of occurrence. Minimizing the uncertainty of clock-edge transitions is the system designer's primary concern when dealing with CPUs operating at 40 MHz or faster.

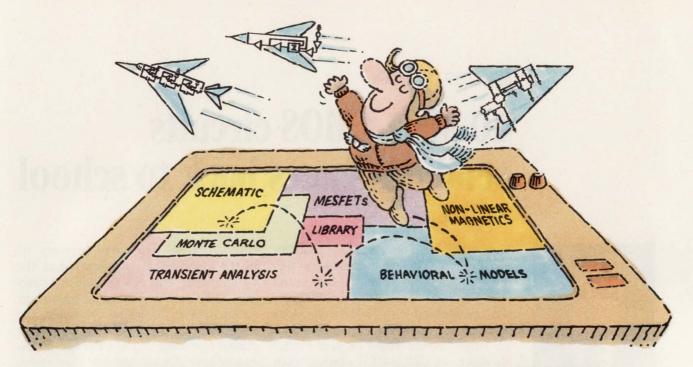
The number-one headache in high-speed design is clock skew. The system clock must be distributed to every IC in the system that is operating at the CPU speed. The ICs include not only the CPU but also multiple secondary cache RAMs, the cache controller, the main-memory controller, and any other ASICs operating at the CPU speed. Because these ICs can number 15 or more, you'll need buffers to distribute the crystal clock reference.

#### Don't let buffers skew you

Clock skew is the time differential between edge transitions for different buffered outputs. Buffers generate three types of clock skew: intrinsic,



Multiple high-speed chips on a single board require adequate heat sinks. The Intel 486 DX cache module dissipates a maximum of 21W and requires a minimum air flow rate of 200 LFM (linear ft/min).



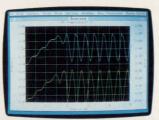
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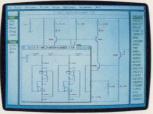
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#### HIGH-SPEED-CPU DESIGN

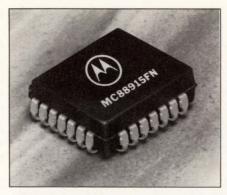
pulse, and extrinsic. Intrinsic skew is the differential between outputs on the same IC. In systems operating slower than 25 MHz, you could often use a 74ALS244A octal line driver as a clock buffer. Although these drivers don't specify the intrinsic skew, you can estimate the skew by subtracting the maximum from the minimum specified propagation delay—approximately 3 nsec.

Because 3-nsec intrinsic skew is unacceptable at 40-MHz clock rates, vendors offer clock drivers having specified intrinsic skews of 1 nsec or less. Integrated Device Technology's 49FCT805 (\$8.40 (1000)) is a CMOS dual 1- to 5-line driver having a maximum intrinsic skew of 700 psec. Motorola's MC10H641 (\$15.10 (100)) is a PECL (pseudo emittercoupled logic) 1- to 9-line driver having a maximum intrinsic skew of 500 psec. (PECL is ECL that operates from 0 to 5V.) Texas Instruments' 74ACT11208 (\$6.50 (1000)) is a CMOS dual 1- to 4-line driver that has a maximum intrinsic skew of 1 nsec. All of these drivers can sink 24 mA.

Clock buffers also generate pulse skew. Pulse skew is the difference in propagation delay between a lowto-high transition and a high-to-low transition for a single buffer output. Pulse skew affects the output clock's duty cycle, which is an important specification for most highspeed CPUs. For example, the period of a 80486 µP's 50-MHz clock must have maximum rise and fall times of 2 nsec and a minimum clock high or low time of 7 nsec. Severe clock skew can occur when the crystal oscillator has an uncontrolled duty cycle or when the buffer's pulse skew is large.

#### PLLs align outputs to input

When large clock fan-outs require multiple driver ICs, the skew variations between parts add to the clock skew. A new class of clock driver has emerged in the past cou-



A PLL clock driver can multiply a low-frequency input clock by 2 before clock distribution. Motorola's MC88915 CMOS PLL clock driver operates as fast as 40 MHz and has an output as high as 80 MHz.

ple of years that reduces pulse skew and part-to-part skew, which is a variety of extrinsic skew. These clock drivers contain a phase-locked loop (PLL). The external crystal oscillator drives the signal input to the PLL's phase-frequency detector, and a feedback signal from one of the chip's output buffers drives the detector's reference input.

Because the PLL adjusts the phase of the output buffers to the phase of the external crystal oscillator, part-to-part skew variations between multiple PLL clock drivers are virtually eliminated. In addition, by using a VCO whose frequency is double the crystal frequency and a divide-by-2 circuit to drive the output buffers, the PLL clock driver can maintain a 50% duty cycle and thereby eliminate pulse skew.

Avasem Corp offers three CMOS PLL clock drivers. The AV9170 (\$7.15 (1000)) contains one PLL, which can externally drive an octal buffer, such as a 74HC244. You feed back one of the buffer outputs to the reference input on the IC to complete the loop. The AV9127 (\$6.87 (1000)) and AV9129 (\$6.95 (1000)) contain four independent PLLs that operate from a single external crystal source of 14.318 MHz. The chips generate all the necessary clock frequencies for 8088,

80286, 80386, and 80486  $\mu$ Ps. The PLL drivers have an intrinsic skew of 1 nsec for all Q output buffers.

Motorola's MC88915 (\$15.10 (100)) is a CMOS PLL clock driver that has a specified intrinsic skew of 500 psec for its five buffered Q outputs. The chip can provide outputs at twice and one-half the Q output frequency. The maximum Q output frequency is 40 MHz, and the maximum output frequency is 80 MHz.

Triquint Semiconductor has three families of PLL clock drivers that operate with input frequencies of 25, 33, 40, or 50 MHz. The GA1110 (\$33.20 (100) for 50-MHz version) provides six buffered outputs having an intrinsic skew of 250 psec at the same frequency as the input. The GA1486 (\$29.80 (100) for 50-MHz version) is similar to the GA1110 but provides five buffered outputs of one polarity and one buffered output of the opposite polarity. The GA1210 (\$37.40 (100) for 50-MHz version) gives you the option of using an input frequency that is twice the output frequency.

Triquint fabricates its PLL clock drivers in GaAs, which enables the loop VCO to run at 400 to 500 MHz. The VCO drives state-machine logic, which adjusts the feedback division ratio and provides a means of adjusting the edge displacement for any buffered output by multiples of the VCO period. You can adjust a clock edge to be earlier or later than the edge of the reference feedback signal. The edge adjustments are n×2 nsec when the VCO frequency is 500 MHz.

Although the latest generation of clock-driver ICs can keep clock-buffer skews manageable, you must still pay attention to extrinsic skew and transmission-line effects. Extrinsic skew is external to the buffers. It is the time differential that occurs when you send a fast-rise-time signal on board traces that have different lengths and capaci-

#### HIGH-SPEED-CPU DESIGN

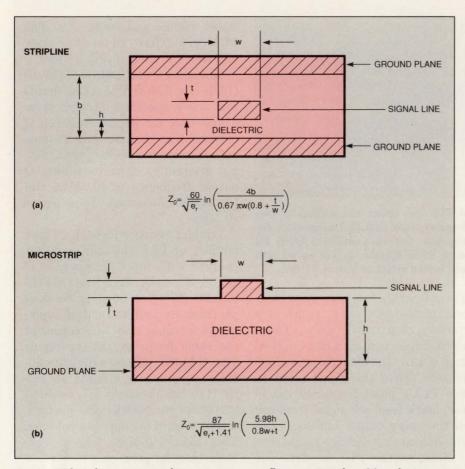


Fig 1—PC-board transmission lines come in two flavors—strip line (a) and microstrip (b). The clock driver must drive a line's characteristic impedance ( $Z_0$ ), which is a function of the trace geometry and the board's relative dielectric constant, (e<sub>R</sub>).

tive loads. To compensate for extrinsic skew, you must distribute high-speed clock lines on a board using controlled-impedance microstrip or strip line (Fig 1).

Sending a fast-rise-time signal over a pc-board trace from point A to point B requires a finite transit time, called trace delay. In CPU designs operating slower than 25 MHz, the rise time of a signal is generally slow enough so that all devices on a single trace behave as lumped elements connected to a single wire. However, if a signal's rise and fall times are comparable to a trace length's transit time-which is often the case for designs operating at greater than 40 MHz-devices on the line receive the signal at delayed time intervals. Unless the trace is a controlled-impedance

transmission line, severe ringing can occur. This ringing can exceed a logic threshold, thereby creating timing havoc.

In low-frequency digital designs, you usually think of connecting one IC to another IC on the pc board. In high-frequency digital designs, you must think of a bucket brigade in which the output of an IC drives a transmission line, which in turn drives the input to another IC. Transmission lines were initially employed only at microwave frequencies, but ECL designers have used these principles for years to interconnect high-speed digital circuits. Ref 1 is an excellent compendium of digital transmission-line basics, tips, and techniques. Although the handbook is ECL orientated, the information is applicable to

high-speed CMOS designs as well.

Ref 1 includes a rule of thumb for predicting whether a pc-board trace will exhibit transmission-line effects. You can consider a trace to be a transmission line when the length of the trace is equal to or greater than the signal rise time divided by twice the loaded-trace transit time:

$$L_{\text{MAX}} = t_{\text{R}}/2t'_{\text{PD}} \text{ ft} \qquad (1)$$

where  $t_R$  is the pulse rise time in nsec and  $t'_{PD}$  is the loaded-trace transit time in nsec/ft.

Ref 1 shows how to calculate the unloaded-trace transit time for a conductor and how to modify the time to account for capacitive loading. The unloaded transit time depends on a board's relative dielectric constant and trace geometry and is typically about 2 nsec/ft. Capacitive loading includes not only the input capacitance for CMOS gates located on the trace but also socket capacitances and platedthrough-hole capacitances. Capacitive loading can produce a loadedtrace transit time of approximately 3 nsec/ft.

Assuming a clock rise time of 1 nsec for the high-speed clock and a 3-nsec/ft loaded-trace transit time, Eq 1 indicates that all trace lengths greater than 2 in. will exhibit transmission-line effects. To reduce the ringing these effects would cause, you must terminate each trace using its characteristic impedance. Ref 1 describes how to calculate the characteristic impedance and discusses the pros and cons of series, parallel, and diode terminations.

To compensate for extrinsic skew you should lay out the pc board so that each distributed clock line has the same unloaded-trace transit time. Ref 1 provides some good guidelines for board layout, but you should simulate your layout on a computer using Spice models before committing the design to hardware.

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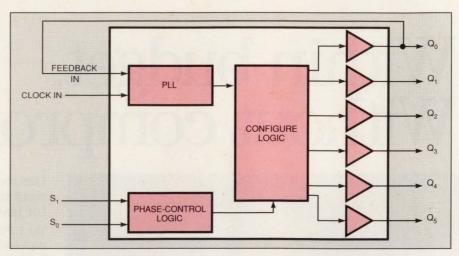
#### HIGH-SPEED-CPU DESIGN

Enhanced versions of the Spice circuit-analysis program from Microsim Corp (Irvine, CA) and Meta-Software (Campbell, CA) let you interconnect circuit elements via transmission lines.

Vendors of high-speed CPUs often supply Spice modeling parameters for the on-chip line receivers and buffers that externally interface with high-speed lines. These vendors also provide lumped-parameter models, including parasitics, for specific packaging configurations. You can use the models as subroutines for the main Spice circuit model.

In addition to Spice modeling, automatic design tools are also becoming a necessity in high-speed design. You must still physically lay out the board based on the Spice model simulation. Then, EDA tools from companies such as Mentor Graphics Corp (Beaverton, OR) will automatically route lines and place components on a pc board. The tools use algorithms that determine minimum and maximum line lengths, multilayer-pc-board restrictions, impedance terminations, and EMI and crosstalk susceptibility.

CPU vendors are aware of the new design challenges confronting the CMOS designer as clock rates increase. Multichip modules, for ex-



Including a PLL in the clock driver reduces part-to-part skew to values as small as the loop phase error. Triquint Semiconductor's GA1xxx family also has a 500-MHz VCO that can advance or retard distributed clocks in 2-nsec increments.

ample, can ease extrinsic skew and transmission-line effects. Intel offers its 50-MHz 80486 DX µP on a multichip module that also has an 82495 DX cache controller and as many as nine 82490 DX cache SRAM (static RAM) chips. The nine SRAM chips provide 256 kbytes of secondary cache RAM. The \$1314 module measures 6.1 × 4.38 in. Surface mounting lets the 50-MHz CPU bus on the module transfer burst data at 160 Mbytes/sec.

The 486 cache module confines the critical 50-MHz signal lines to a small physical area, thereby reducing transmission-line effects.

The large secondary cache lets you design a hierarchical bus system in which the module's resident CPU bus operates at 50 MHz and the secondary cache system connects to an external main memory bus operating at 25 MHz. You can connect the main memory bus to an 8.33-MHz EISA bus via standard logic-interface chips.

The hierarchical bus system doesn't completely get you out of the woods, however. You must still design a 50-MHz clock-distribution system to drive the CPU, cache controller, and nine cache SRAM chips. You must also design an

#### For more information . . .

For more information on the high-speed CPU products discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you read about their products in EDN.

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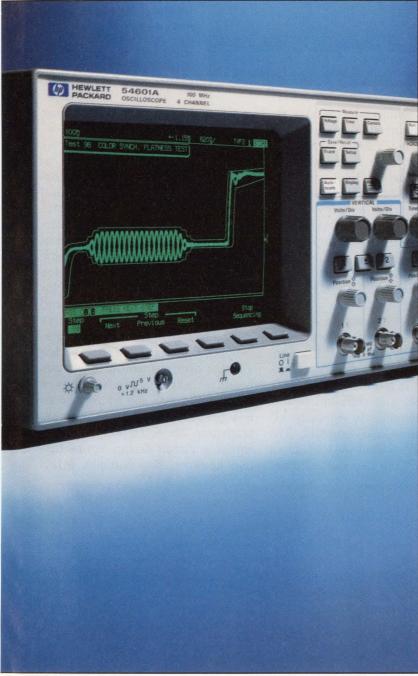
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#### HIGH-SPEED-CPU DESIGN

ASIC for the main memory-bus controller using state-machine logic that operates at 50 MHz. Ref 2 describes how to design the clock system; Ref 3 details designing the memory-bus controller.

Cypress Semiconductor now offers the entire SPARC chip set on multichip modules, called SPARCore modules, that interface with the Mbus at 25, 33, or 40 MHz. Two of the modules, the \$1450 CYM6001K and the \$1675 CYM-6003K, contain a CY601 integer unit, a CYC602 floating-point unit, and two 16k×16-bit CY7C157 cache SRAMs. The CYM6001K also has a CY7C604 cache controller/ memory-management unit; the CYM6003K has a CY7C605 cache controller/memory-management unit. The CYM6002K module has twice as many chips-10-as the other modules, so it can create a dualprocessor for multiprocessor applications (Fig 2).

In all three modules, the chips are surface mounted on a 5.78 × 2.75-in. pc board having a vertical microstrip MBus connector from AMP Inc. The connector lets you stack modules in multiprocessor applications. The modules save you engineering time in 40-MHz applications by employing dual power and ground planes and impedance-matched traces that minimize clock skew. Each clock-distribution line has diode terminations to reduce ringing.

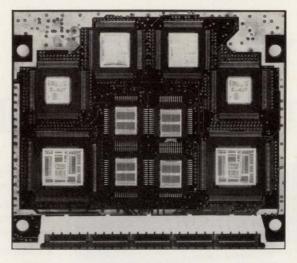


Fig 2—Multichip modules relieve some design burdens by matching the trace characteristics of high-speed components on a single plug-in module. The CYM6002K module contains 10 ICs and connects directly to the Mbus via an impedance-controlled connector.

Cypress Semiconductor also recently announced a miniaturized version of the CY6002K SPARCore module that uses advanced multichip-module technology. The \$2648 CYM6122L is a dual-processor module that employs tapeautomated bonding to mount 10 ICs on a substrate having impedancematched traces. The module measures  $3.3 \times 2.5$  in. and can operate at frequencies of 40 MHz and greater.

Although clock skew and transmission-line effects are the primary concern of high-speed CPU design, they aren't the only concerns. High-speed circuits require good grounding practices and sufficient power-supply decoupling to eliminate extraneous noise and crosstalk. The rise and fall times of the CPU clock are fast, and the rise and fall times

on the address and data lines must be just as fast to keep up.

Output buffers for wide address and data buses can experience severe ground bounce when many bits change simultaneously. Ground bounce occurs in CMOS circuits when the high power-supply current that occurs during a logic transition flows through any parasitic inductance between the device package and the ground trace. Inadequate device decoupling and grounding can cause excessive ground-bounce noise on the bus lines.

Synchronous circuits have an advantage over asynchronous circuits because excess ground-bounce noise on the data and address buses is a concern only during the clock-transition time. High-speed synchronous circuit design can be taxing, however. For example, MIPS

#### On-chip CPU tricks ease clock distribution

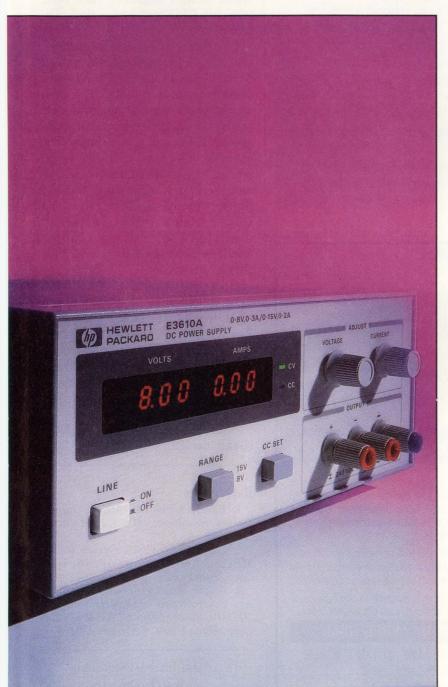
To help system designers resolve high-speed pc-board difficulties, MIPS Computer Systems Inc has incorporated some on-chip design features into its recently announced R4000 RISC CPU. The R4000 is the first of an expected wave of  $\mu$ Ps that perform internal 64-bit arithmetic. The CPU has an on-chip PLL clock driver that drives two output buffers to generate two system clocks—RCLK and TCLK.

You supply an external master clock to the CPU. The PLL multiplies this clock by 2 to drive its internal pipelines.

You can program the RCLK and TCLK clocks to be equal to or one-half or one-third of the master clock rate. A 50-MHz master clock generates a 100-MHz internal pipeline clock and programmable RCLK and TCLK clocks of 50, 33, or 25 MHz.

To reduce ringing, you can program the rise and fall times of the RCLK and TCLK clocks to match the characteristics of external loaded transmission lines. You can also advance or retard RCLK and TCLK to equalize extrinsic clock skew.

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#### HIGH-SPEED-CPU DESIGN

Computer Systems' R4000 has a 128-bit data bus that transfers data to as much as 4 Mbytes of external secondary cache SRAM. Although the R4000 architecture enables the chip to transfer data 64 bits at a time, minimizing the noise caused by 64-bit transitions occurring in a 2-nsec time interval can challenge even the most experienced highspeed design engineer (see box, "On-chip CPU tricks ease clock distribution").

One final concern is heat dissipation. The high performance gained by high-speed CMOS CPUs doesn't come without a penalty. The penalty is power dissipation and its attendant heat generation. All highspeed CPUs are power hogs. For example, the Intel 486 DX cache module dissipates as much as 21W and requires a minimum 200 LFM (linear ft/min) air-flow rate. The MIPS R4000 CPU typically dissipates 13W, and the Cypress Semiconductor 40-MHz CYM6003K SPARCore module dissipates as much as 14W and requires a minimum 250 LFM air-flow rate.

Although these power dissipation figures are high, they do not exceed the capabilities of thermal-management devices. In fact, ECL devices have been dissipating this much power for years and keep on ticking. Ref 1 has a chapter devoted to thermal considerations in ECL circuit design. EDN

#### References

- 1. Blood, William B, MECL System Design Handbook, 4th Ed, Motorola Inc. 1988.
- 2. Jolly, Rich, Clock Design in 50-MHz Intel 486 Systems, AP-453, Intel Corp, Santa Clara, CA, June 1991.
- 3. Taufik Ma, Designing a Memory Bus Controller for a 50-MHz Intel 486 DX CPU Cache System, AP-458, Intel Corp, Santa Clara, CA, June 1991.

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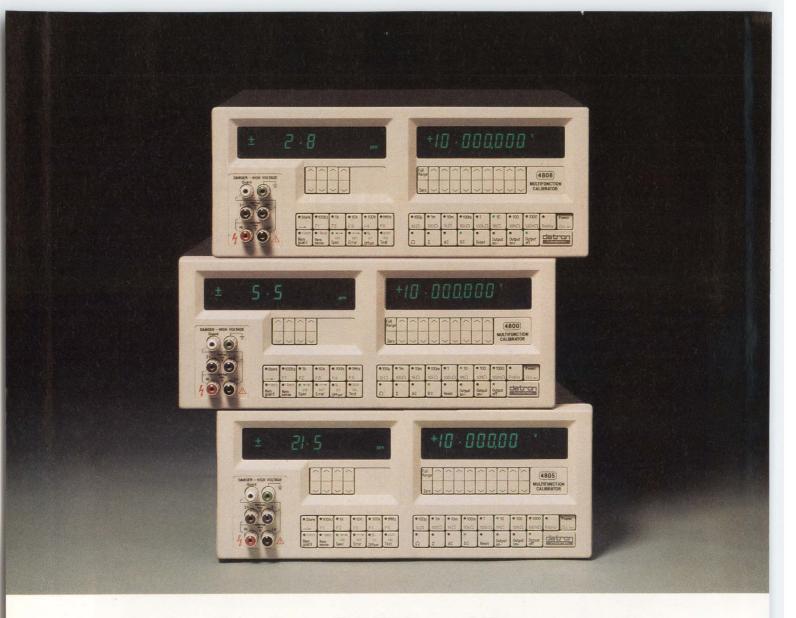
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## Smart-card applications' hidden problems add to designers' challenges

GARY LEGG, Senior Technical Editor

Hardware and software design come last when you develop an application for smart cards. First, you have to tackle a few problems that you might not ordinarily expect.

Developing a smart-card application looks easy enough; you can get a demo running in an afternoon for only a few hundred dollars. Beware, though: There's much more to it than meets the engineering eye. Once you start developing a real application, you can become entangled in issues that have little or nothing to do with electronics. And, in a real application, the electronics isn't trivial, either.

Smart-card applications appear simple because the cards are simple. Despite the nifty packaging—smart cards are the same size and shape of standard credit cards—the microcomputer inside each card is just an 8-bit device with some ROM-resident software. In theory, you can create a smart-card system by buying a few cards and some kind of a card reader or terminal. All you have to do—in theory—is write some

terminal-resident software that communicates with the card's operating system.

But before you buy your first smart card, you'll have to consider an array of confusing choices (see box, "Pick a card"). And even if you find that a smart-card solution seems ideal from a technical standpoint, you might discover that market factors negate its technical advantages. Smart cards have met little success as bank cards and credit cards, for example, because magneticstripe cards and their associated equipment are so well established.

There are, however, application areas where smart cards are well suited technically and don't face entrenched competition (see **box**, "Joining the card game"). In some cases, though, licensing costs may be a factor in determining whether or not you want to use smart cards.

Anyone who manufactures either smart cards or equipment that provides an electronic interface to smart cards must pay licensing fees to Innovatron, a French company that holds the basic smart-card patents. Innovatron negotiates each case separately, but you have basically two choices: You can pay a large up-front fee and a small per-unit royalty, or you can opt for a smaller up-front fee and higher royalties.

Neither option is attractive. A large



Applications of smart cards in Europe include controlling access to cellular-phone services. Smart cards provide security and other benefits that magnetic-stripe cards do not. (Photo courtesy Gemplus Card International)

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#### **EDN-TECHNOLOGY UPDATE**

#### SMART-CARD APPLICATIONS

up-front fee is a strong deterrent to entering an uncertain market with new technology. On the other hand, higher royalties preclude the low price per card that is essential to market acceptance.

Innovatron did not respond to our request for information about fee structures, but several US sources claim that an up-front fee can be \$100,000 or more. We were unable to obtain specific figures for royalties, but the selling price per card in very high volumes (millions) can be as low as \$3, including royalties. Cards with memory only (no processor) can sell for as little as \$1. A magnetic-stripe card, in contrast, can go for as little as 17 cents.

If you don't manufacture your own smart cards or the electronic equipment that reads and writes to them, you won't pay licensing fees directly. Vendors who sell you cards or equipment will charge prices that reflect fees they have already paid.

But licensing fees can—indeed should—affect how you design

your hardware. Ben Haag, business manager for smart-card acceptor devices at Amphenol Corp (Hamden, CT), explains that Innovatron's fees for smart-card equipment reflect the equipment's value. If the equipment is a large, expensive system, you'll pay a lot; if it's a small, inexpensive subsystem, you'll pay less.

Only the original seller pays a fee; resellers do not. Thus, there is an advantage to producing simple and inexpensive smart-card interface devices that can then be incorporated into larger equipment. Most smart-card companies offer card "couplers"—small devices capable of both reading and writing to cards—that connect to larger systems with a cable. These devices typically sell for \$150 to \$700.

#### Getting personal

If you get by the marketing and licensing challenges of a smart-card application, you still face a job that's far from pure engineering. Smart cards require what the indus-

try refers to as personalization, only a part of which involves electronics.

When you personalize a smart card—which you must do before you issue it to a customer or an individual card user—you do much more than simply load it with an account number and a personal identification number (PIN). In fact, much of personalization is not for the individual card holder, but for the particular application. You want your card to show—not just electronically, but physically—what its purpose is and who issued it.

A bank card, for example, must be printed—sometimes in four color—with the bank's name and other information. Personalization can also involve embossing, imprinting, a signature panel, a magnetic stripe, ultraviolet printing (visible only under black light), a photograph, and even a hologram.

In all likelihood, you'll buy your smart cards from a company that will do the personalization for you. In most cases—an exception being situations that involve extremely

#### Pick a card

The term "smart card" is applied to many different things, some of which aren't smart and some of which aren't cards.

According to the most commonly accepted definition, a smart card is the size and shape of a credit card and has electrical contacts on its surface that connect to an embedded microprocessor. Smart-card pretenders include devices without a microprocessor—memory cards, for example—and devices that are in other physical forms—tags and keys, for instance.

The smart-card standard specifies eight electrical contacts, although most cards use only six. The pattern of contacts may look different from card to card, but the positions of individual contacts relative to each other are fixed. However, the pattern itself can be in two different locations on the card—in the upper left corner and midway down the left side.

Cards with contacts in the corner will become obsolete this year. For cards issued in most countries, the corner location conflicts with the location of a magnetic

stripe, a necessary feature for compatibility with existing bank-card and credit-card systems. Only French and American cards have a magnetic stripe on the back; cards used in other countries have a stripe on the front.

Some cards have no electrical contacts at all. GEC Card Technology Ltd makes a card that communicates and receives its power by radio transmission. A coil of wire in the card develops a voltage across it in the presence of an inductive RF field; on-card circuitry rectifies and regulates the voltage to provide power to the card's smart-card IC. Electronic tags and tokens in various forms work the same way.

Optical-storage cards take the form of a credit card, but don't have a smart card's "smarts." Their advantage is massive storage. The Laser Card from Laser Card Systems Corp (Mountain View, CA) can store 2.86 Mbytes of data. True smart cards are limited to a few kilobytes.

#### **EDN-TECHNOLOGY UPDATE**

#### SMART-CARD APPLICATIONS

high volumes—you probably won't consider doing any of the personalization yourself, except possibly the electronic part.

#### Unexpected delays

Even so, personalization is a common snag. John Taskett, vice president of Micro Card Technologies, explains that engineers who have completed a smart-card design often have to wait for someone else in their company to prepare or approve artwork to be printed on the card. "As soon as the marketing guys and management see what you plan to print on your card," Taskett says, "it starts going around and around. I cannot tell you how long it takes to get artwork approval. I've seen it take nine or ten months."

Even the electronic part of personalization is an extra step compared to projects that don't use smart cards. Typically, each smart card contains unique information about the card issuer and the individual card holder. With other applications, you can duplicate a chip's EPROM or EEPROM code with a gang programmer; with smart cards, you can't.

To perform electronic personali-



Smart-card couplers are part of every application-development kit. This handheld reader/ writer comes with an \$895 kit from IX Systems (formerly Smart Card International).

zation yourself, you'll need, at a minimum, some PC-based software and a card coupler. If you want high speed, too, you'll need special personalization hardware. You can get what you need—software, hardware, and training—from smartcard vendors.

In comparison to personalization, technical issues can be (but often aren't) simple. For example, you don't need to write any of the software that goes inside a smart card; cards come from their vendors with ROM-resident operating systems designed specifically for smart-card operations. The operating systems place great emphasis on security and have been thoroughly tested. Writing your own OS could make your cards and your application vulnerable to fraudulent access.

Most smart-card vendors say that only in rare circumstances would you want to develop your own code for a smart card. For example, if

#### Joining the card game

You don't have to be European to work with smart cards, but it helps. In Europe, many government monopolies, such as banking and communications, have mandated smart-card applications. Elsewhere, and in any competitive environment, you usually have to apply smart cards where they won't run up against entrenched competition. In general, this means new application areas. Some recent applications include:

**Subscriber card for pay TV.** Smart cards run descrambling algorithms to control access to pay TV transmissions. To guard against piracy, one French TV system uses a new scrambling key every ten seconds. Subscribers' smart cards change keys in synch to allow reception.

Benefits transfer. The state of Wyoming uses

smart cards to transfer benefits to participants in its supplemental food program for women, infants, and children (WIC). Recipients use the cards, which replaced a system of paper coupons, at state-authorized WIC food retailers. The cards assist in record keeping and, by incorporating personal identification numbers (PINs), help ensure that only intended recipients will receive benefits.

Access control. Smart cards control access to facilities and computer systems in numerous locations. To gain access, you need not only a password, but also a unique personal card that contains that password. Unlike passwords stored in a magnetic-stripe card, fraudulent users can not read passwords stored in a smart card.

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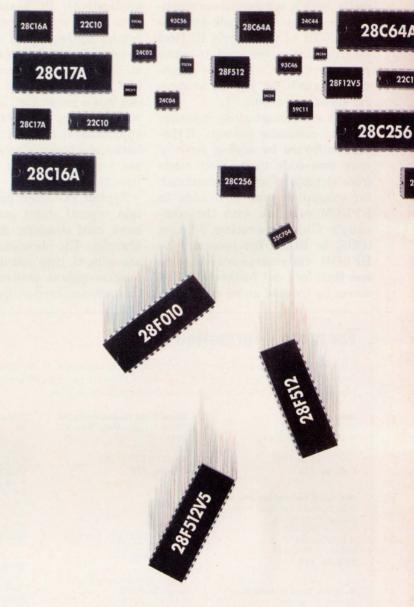
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#### SMART-CARD APPLICATIONS

you have a sensitive, proprietary algorithm, you'd probably work directly with a semiconductor manufacturer to get your code into the mask ROM of your card's IC (Ref 1). You might also want to write your own code if a standard smartcard OS can't give you the processing speed you need.

With some smart cards, however, you can customize proven, off-the-shelf software by adding some of your own code to it. With cards from Gemplus Card International, for example, your own code in EPROM can link with the company's Chip Operating System (COS) in ROM. You program the EPROM via smart-card contacts and then lock out further EPROM access by blowing an on-chip fuse.

Smart cards' canned software is especially easy to use in PC-based applications. PC-based kits from smart-card vendors contain the essential hardware and software for developing simple applications or, at the very least, learning about and evaluating smart cards. You can use a smart card much as you would a floppy disk. For an in-house application that doesn't require artistic card personalization, you can use a smart card just as it comes from the vendor.

Typical PC-based packages contain several smart cards, one or more card couplers, and software libraries. The libraries, usually for use with C, help you develop computer-resident control software that accesses card-resident OS func-

tions. (PC-based development systems from smart-card chip manufacturers are different; they're primarily for use in developing your own smart cards from scratch. They help you develop card-resident ROM code, and usually include an incircuit emulator.)

In the US, you can buy PC-based kits from Micro Card Technologies, IX Systems, Schlumberger, Gemplus, and Datacard. Prices range from \$400 to around \$2500, depending on what's in the kit.

Unfortunately, most applications require an interface to equipment other than a PC—a vending machine or a pay phone, for example. It's here that you meet your technical challenge; not only may the equipment be complicated, but you

#### For more information . . .

For more information on the smart-card products discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you read about their products in EDN.

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#### **EDN-TECHNOLOGY UPDATE**

#### SMART-CARD APPLICATIONS

have to comply with ISO standard 7816. What's worse, you'll often have to design your system to take an incredible amount of abuse from the environment, unsophisticated users, and sometimes even from vandals.

#### Smart cards for dummkopfs

"You have to tolerate people putting a ruler into a smart-card slot and shorting all the contacts together," says Micro Card's Taskett. "Or inserting a smart card when it's charged up with static electricity. Or pulling a card out of a connector when it's running." You also have to make sure that all electrical signals and protocols follow the ISO standard and that signals come up in the right order. If you have a high signal on your clock pin and don't have V<sub>CC</sub>, Taskett notes, some smart cards' microprocessor chips "will smoke."

Assuming you're up to all the previously mentioned challenges, you're now ready to start learning about smart cards. One of the first things you'll learn is that smart cards' raison d'etre is security. One of the next things you'll learn is that smart cards' operating systems are different from those of computers. In a smart card's OS, many functions—perhaps half—deal with security.

The leading smart-card chip makers, Motorola and SGS-Thomson, have always emphasized security in features of their smart-card ICs and in their manufacturing, storage, and transporting procedures (Ref 1). Recently introduced chips from Siemens (the SLE 44C200) and Philips (the 83C852) even incorporate cryptographic hardware. Both are capable of performing the compute-intensive calculations needed for public-key encryption and decryption (Ref 2). Previously, most smart-card applications were limited to the easier, but less secure, Data Encryption Standard (DES).

Cryptography is becoming increasingly common in smart-card applications and increasingly in demand by potential customers. Encryption helps protect financial data, PINs, and passwords that would otherwise be vulnerable to electronic eavesdropping. In addition, when encryption and decryption occur inside the smart card, potential bugging locations are limited to the card's embedded chip—a difficult proposition.

Depending on the nature of your smart-card project, you may need to learn the basics of cryptography before you begin. Micro Card, for example, stresses that cryptographic essentials are a necessity for users of its TB family of high-security smart cards. The company offers—and strongly recommends—a three-day training session (at \$325 per day) that includes cryptography. For its less secure Scot family of cards, the company offers a 2-day session that it says is helpful, but not essential.

When you finally get around to engineering choices, you'll find a variety of cards and development systems available. True smart cards, those with embedded microprocessors, range in price from about \$3 for simple types in very high quantities (millions) to around \$15 for more elaborate ones in small quantities (thousands). Development systems run from a few hundred dollars to a few thousand.

You'll also find a variety of smartcard hardware devices, ranging from interface boards to telephones to terminals for electronic funds transfer (EFT). Vendors that offer system-level products often are subsidiaries or divisions of large, diversified companies. Schlumberger, for example, has only a small smartcard operation in the US, but is the largest European supplier of smartcard telephones.

Although smart cards have been slow to catch on, especially in the

US, it's not too early to start planning your own application. A growing market presence is leading to greater market acceptance, which in turn is lowering prices. And lower prices are the key to an avalanche of smart cards. The 1994 expiration of Innovatron's smart-card patents can only contribute to further price cuts.

"You will see lots of cards by 1994," says Taskett, "and you will also see the prices crash. A \$2 microprocessor-based smart card will be common for large users." For a card that has a microprocessor, a magnetic stripe, a hologram, "and everything else," says Taskett, "that's a heck of a deal."

#### References

1. Legg, Gary, "Smart cards gear up for belated success," *EDN*, October 24, 1991, pg 51.

2. Königs, Hans-Peter, "Cryptographic Identification Methods for Smart Cards in the Process of Standardization," *IEEE Communications Magazine*, June 1991, pg 42.

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GaAs ICs

## ICs see mainstream duty as μP glue logic

MAURY WRIGHT, Technical Editor



Designers that leave GaAs out of their toolbox for new communication products and products that use fast RISC or CISC µPs could find themselves in the same situation as drivers who forget to stop by the service station occasionally.

GaAs (gallium arsenide) ICs are simply ICs—not significantly different than TTL, CMOS, ECL, or other varieties of ICs. You normally choose ICs based on how well the functions, power requirements, size, and cost of a particular device fit a design requirement. The same is true for GaAs devices. Off-the-shelf digital GaAs ICs work well in communication applications and in designs that use 33-MHz and faster μPs. GaAs chips have familiar IC functions, such as RAM and PLDs, and, most important, are not cost prohibitive as many people believe.

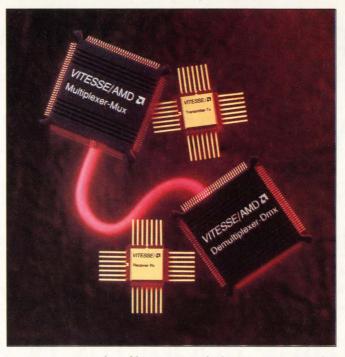
Certainly, generalizations, such as low power associated with CMOS or high speed associated with ECL, can help guide your search for a particular IC. GaAs chips can be characterized

generally as faster than CMOS ICs and less power hungry than ECL ICs. CMOS ICs require significant power increases as speed increases. Therefore, GaAs devices can prove a better choice than CMOS in some applications.

ECL ICs don't offer the level of integration or level of power that GaAs chips have. Vitesse Semiconductor just produced a 1-million-transistor GaAs IC. The company's FX series of gate arrays includes ICs with more than 190,000 gates. Furthermore, the company plans an addition to the FX family in the first half of this year that will feature 350,000 gates.

Meanwhile, Bipolar Integrated Technology (Beaverton, OR), a leader in the field of ECL ICs, will only have a 200,000-gate ECL array available this year. And the ECL arrays that are available from other vendors typically feature less than 100,000 gates. The Vitesse arrays also offer gate-delay and gate-power specs that are less than half of the corresponding specs of leading ECL arrays.

GaAs ICs and discrete components are already established in some areas of the electronics industry. Most people know that the technology has been extensively used in military, space, and other specialized applications where circuit performance was critical and cost wasn't an issue. Many such applications require devices that operate at micro-



You can use coaxial or fiber optics with the Vitesse G-Taxi chip set to achieve 1.25-Gbit/sec data communications over distances as far as 10 km.

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#### GaAs ICs

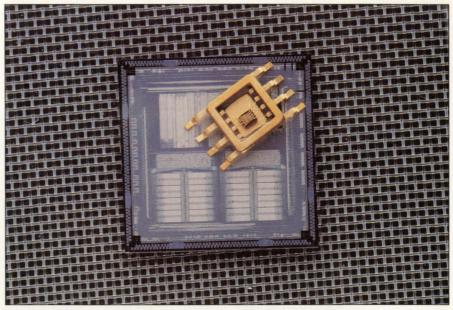
wave frequencies, and GaAs ICs are the only available choice. Berson & Associates (Mountain View, CA, (415) 968-2101) publishes an annual data book that lists and summarizes all such microwave ICs and their manufacturers.

#### Phones use analog GaAs

Analog GaAs ICs and discrete components have infiltrated much more common ground, such as consumer electronics. According to John Day, president of market-research firm Strategies Unlimited (Mountain View, CA), virtually all cellular telephones use GaAs circuits (for example, in their amplifiers). Day says you will also find GaAs devices in satellite television receivers that target consumers and in large-screen televisions.

Analog designers accepted GaAs devices more readily than digital designers could because of the nature of analog components. For example, a basic set of parameters defines an analog amplifier or a transistor regardless of the technology or substrate used to produce the device. GaAs analog ICs and components, therefore, could easily be mixed into designs early on. Early attempts at digital GaAs circuits, however, resulted in requirements for multiple nonstandard powersupply voltages, and incompatibility with other digital IC technologies.

For at least two years, Vitesse Semiconductor and Triquint Semiconductor have made GaAs ICs for mainstream digital applications. The ICs exhibit the speedy specs from their GaAs heritage but balance speed with power consumption, size, and compatibility with other technologies. Unfortunately, the trade press and the manufacturer's marketing organizations have often camouflaged the availability of such products by concentrating coverage on the substrate



A 400,000-transistor GaAs IC from Vitesse demonstrates the company's progress in VLSI circuits compared with the SSI IC in the foreground.

rather than other specs. The headline "GaAs memory" and "Industrystandard 4-nsec static RAM" can actually apply to the same product. The GaAs spec used as an eye catcher should be relegated to the back page of the data sheet for this new generation of ICs.

#### ICs fit communication markets

You can segment the available digital GaAs ICs by three target applications—µP peripherals and support chips, data communications, and telecommunications. The available products range from SSI components such as logic gates to VLSI chip sets and ASICs.

Triquint and Vitesse both offer GaAs ASIC capabilities ranging from gate arrays to full custom ICs. Fujitsu acts as an alternate source for the Vitesse Fury series of gate arrays, and Thomson-CSF offers a second source for all Vitesse ICs. Robert Nunn, Vitesse's director of marketing, claims that ASICs jump started the standard product business. Nunn relates that Vitesse developed a manufacturing process that could add VLSI and low power to the speed GaAs offered but

needed ASIC customers to help define key markets for standard products.

#### PCs use GaAs

Convex Computer (Richardson, TX) designed an entire super-minicomputer with Vitesse GaAs ASICs and standard products. Compaq Computer (Houston, TX) even used a Vitesse ASIC to handle µP support logic in the 50-MHz 486-based Systempro PC. Day says GaAs technology will find increased usage around fast µPs because clock timing is critical, and GaAs clock chips help eliminate clock skew.

Off-the-shelf GaAs ICs for μP applications include devices ranging from clock ICs to memories. For example, Vitesse (and therefore Thomson-CSF) offers the VS12-G422T 256×4-bit static RAM (SRAM). The memory IC includes TTL-compatible inputs and outputs, and is pin compatible with industry-standard silicon SRAMs that use the -422 and -122 designators. You can specify the Vitesse IC with access speeds of 4, 5, or 6 nsec. The fast access speed makes the RAM useful in cache memory.

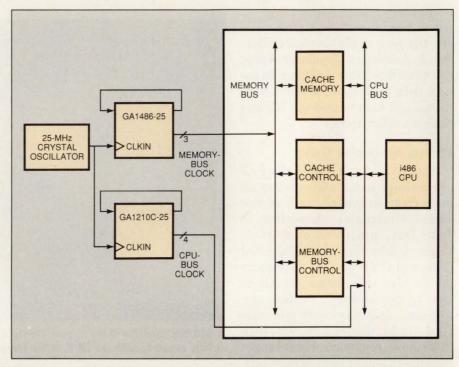
#### GaAs ICs

signal processing, and video applications.

A design requirement of 4-nsec access speed would not limit you to GaAs ICs however. You can buy an equally fast IC from Cypress Semiconductor, the CY10E422, which is built with ECL technology. But the ECL IC includes ECL inputs and ECL outputs. The Vitesse VS12G422T costs \$125 (100), and the Cypress CY10E422 costs \$23.70 (100). Vitesse also offers a 4-kbit, 5-nsec GaAs SRAM that includes ECL inputs and outputs.

Triquint Semiconductor has concentrated its µP-related products around clock circuits and programmable logic. The products originated from Gazelle Microcircuits before Gazelle and Triquint merged. Fig 1 depicts two of the ICs, the GA1210E clock doubler and 2-phase clock generator and the GA1486 clock generator and buffer, used in an application with an Intel 486 µP. The block diagram shows the µP along with a second-level external cache.

The GaAs clock ICs each include six buffered clock outputs with zero propagation delay (250 psec) input



CPUs such as the 50-MHz 486 require precise timing with no clock skew. The Triquint clock chips shown offer zero-propagation-delay clock buffers and 500-psec maximum

to output and a maximum of 500 psec of skew between outputs. The GA1210E and GA1486 clock ICs come in 25- to 50-MHz versions; 50-MHz versions cost \$37.40 and \$29.80, respectively (100).

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Meanwhile, Triquint's GA22V10 programmable logic device offers pin compatibility with industrystandard 22V10s and comes in 5.5-, 6-, and 7.5-nsec operating speeds. The IC features a 3-nsec setup time and can operate with external signals as fast as 125 MHz. The IC. however, is not user programmable—the programming operation requires a laser. Robert Gunn, vice president of sales at Triquint, points out that the company will provide programmed parts in three to five days from a standard JEDEC PLD description file. According to Gunn, Triquint also tests each part it programs at full-rated speed.

You can obtain a user-programmable 7.5-nsec BiCMOS PAL22-V10C from Cypress Semiconductor. The Cypress device requires a maximum of 190-mA supply current compared with 225 mA for the Triquint GaAs IC. But Triquint's GA22V10 costs \$26 (100) for the 7.5nsec version compared with \$33.75

#### For more information . . .

For more information on the GaAs ICs discussed in this article, circle the appropriate numbers on the Information Retrieval Service card, or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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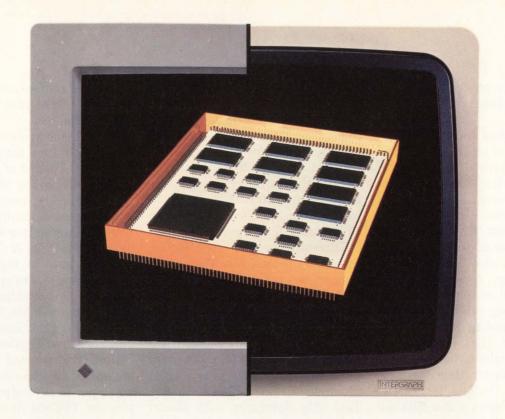
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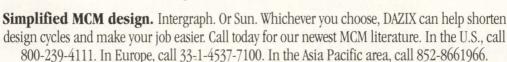


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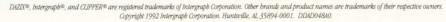


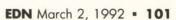
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(100) for the Cypress IC. And you can buy even faster ICs from Triquint.

While available GaAs CPU-support chips focus on silicon alternatives with improved performance, VLSI GaAs data-communication products offer capabilities not found in other technologies. Triquint's Hot Rod chip set, for example, implements a point-to-point datacommunication link that can operate at 1 Gbit/sec. A 2-chip set costs \$440 (100) and is compatible with coaxial or fiber cables. The chip uses 4B/5B encoding defined by the FDDI (Fiber Distributed-Data Interface) standard, but operates substantially faster than the 100-Mbit/sec rate defined for FDDI. Triquint also offers a 200-Mbit/sec version of the IC.

Vitesse has also been busy in the area of data communications. The company just introduced the G-Taxi

chip set that implements the Fiber Channel point-to-point data-communication interface defined by ANSI committee X3T9. The G-Taxi chip set (Fig 2), can operate at the Fiber Channel spec of 1.25 Gbits/sec. You can use the chip set to design communication links that range in length from 100m using coaxial, to 10 km using fiber optics.

Currently, samples cost \$1000 for the 4-chip G-Taxi set. The optical components can add another \$900 to \$3000, based on how long of a point-to-point link you design. Vitesse's Nunn believes that the chip set and optics combined will cost less than \$1000 for OEM users by the end of this year. AMD (Sunnyvale, CA) offers a similar Taxi chip developed with silicon technology that runs at 25% of the 1.25-Gbit/sec Fiber-Channel maximum speed. AMD worked in partnership with Vitesse in designing

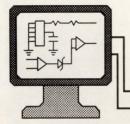
the G-Taxi chip set and has a license to sell the GaAs chip set under the AMD name.

The telecommunications area also promises to be a major market for GaAs ICs. The list of VLSI components available for telecommunications currently consists of crosspoint switches, multiplexers, and demultiplexers. Triquint also offers an extensive list of building-block SSI ICs, such as logic gates that suit any design, but specifically target telecommunications. The Triquint building-block logic was designed by Gigabit Logic before Triquint acquired Gigabit Logic.

Both Triquint and Vitesse offer crosspoint switches that can switch any input to any output. For example, the VSC864 from Vitesse has 64 inputs and 64 outputs and can switch digital communication signals at speeds as fast as 200 Mbits/sec. The IC costs \$1300 (100) and

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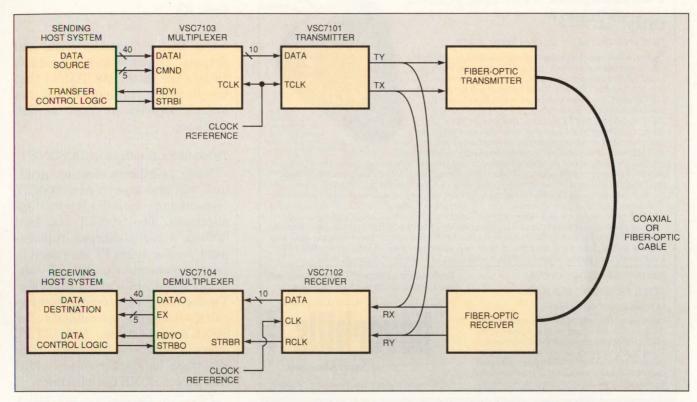
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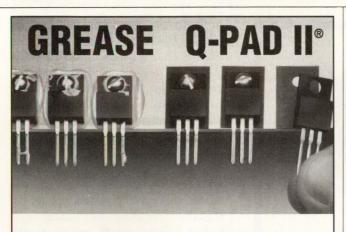
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#### **EDN-TECHNOLOGY UPDATE**

#### GaAs ICs

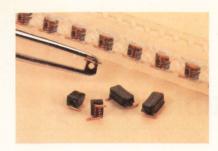
offers ECL-compatible inputs and outputs. Triquint's switch products include the \$200 (100) TQ8016 that has 16 inputs and outputs and can switch signals as fast as 2.6 Gbits/sec.

#### **Telecommunication with SONET**

Many telecommunication products will find uses in new SONET (synchronous optical network) applications. The SONET standard defines a turbo-charged replacement for the aging T1 lines used in telecommunications. SONET networks will operate at 2.4 Gbits/sec. Vitesse offers some multiplexer circuits designed specifically for SONET applications. And, AT&T offers a number of building-block ICs, such as clock recovery chips that target SONET applications.

The few companies currently building mainstream GaAs ICs are just the beginning. Fujitsu just built an IC-fabrication facility that can handle 4-in. GaAs wafers. You can bet that it won't be used strictly to build Vitesse-compatible gate arrays. Texas Instruments, planning to be a player in the GaAs market, wants to offer a GaAs µP. So don't leave GaAs out of your design toolbox. Simply use GaAs ICs as you would use any other technology. GaAs will probably never replace silicon the way some early prognosticators predicted, but count on it being important in many mainstream areas of the electronics industry.

Article Interest Quotient
(Circle One)
High 488 Medium 489 Low 490



#### Surface mount "Springs" have tight tolerance, high Q

Coilcraft's SMD "Spring" inductors are ideal for high frequency RF applications, combining the low cost and high Q of air core designs with the convenience of surface mounting.

They cover the inductance range from 2.5 to 43 nH with minimum Q values of 100 to 145 at 150 MHz. Tolerance is ±5% and self resonance is typically greater than 3 GHz.

High temp jacketing assures mechanical stability and very close tolerance. it also forms a flat top, making the parts suitable for automatic placement and reflow soldering. They're available packaged in standard 12 mm EIA tape and reel.

For more information, contact **Coilcraft**, 1102 Silver Lake Road, Cary IL 60013. 708/639-6400.

CIRCLE NO. 73



#### Tuneable coils feature compact 5 mm size, low drift

New "Uni-5" tuneable coils from Coilcraft are ideal for applications above 100 MHz where space is at a premium.

For electrical and mechanical stability, the winding is precision molded in a single piece of polypropylene only 8 mm high. Tin plated brass cans are available for integral shielding and additional mounting stability. Tuning of the international standard 5 mm size coils is done via a .187" long threaded aluminum core with a slotted head.

Inductance values range from 18 nH to 270 nH with Q's from 100 to 190 at 100 MHz.

For more information contact **Coilcraft**, 1102 Silver Lake Road, Cary IL 60013. 708/639-6400.

CIRCLE NO. 74

### Higher performance EMI filtering for high speed data lines

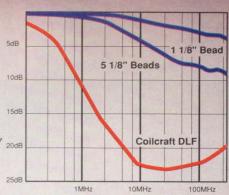


All these ferrite beads can't equal the EMI suppression of a single Coilcraft Data Line Filter.

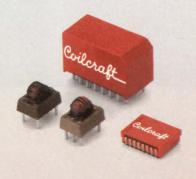
Our new DLFs are the most effective, low-cost way to eliminate common mode EMI from digital signals, logic level power lines, and inter-equipment cables.

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Attenuation (50 Ohm System)



Coilcraft Data Line Filters are easier to install and usually take less board space than beads or baluns. And they're far less expensive than filtered connectors—around 2¢ per dB per line.

For details on our complete line of Data Line Filters, circle the reader service number. Or call **800/322-2645** (in IL 708/639-6400).

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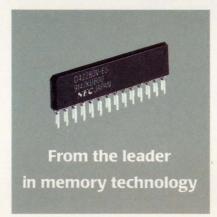
NTSC or PAL signals digitized at 8 bits. Their write/read cycle time is 30ns. Access speed is 25ns. Featuring FIFO operation, asynchronous write/read, and a complete static interface, our 2M field buffers are avail-

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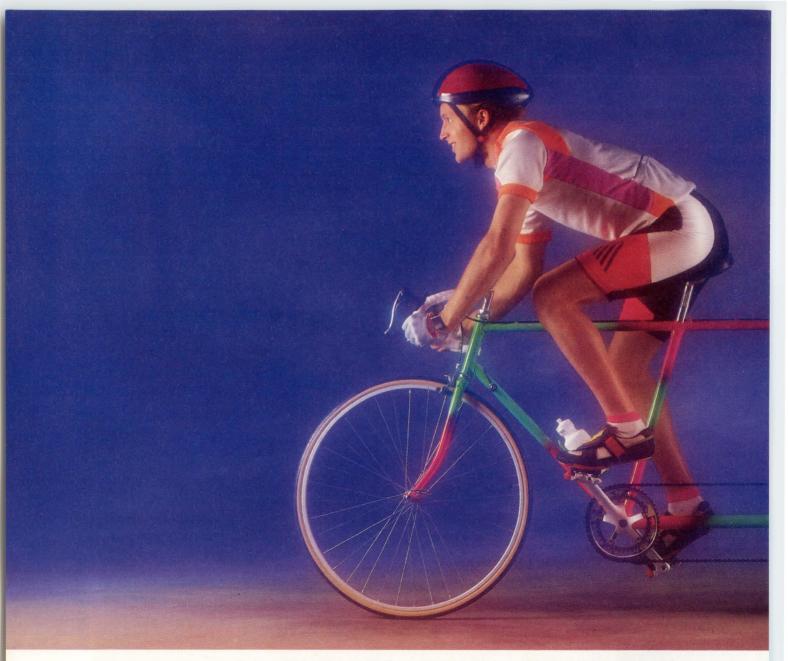
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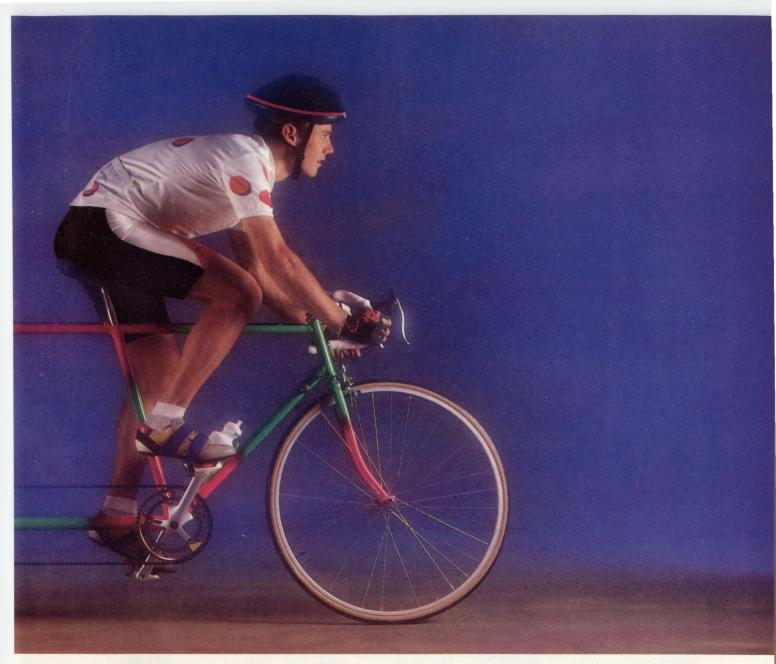
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- 4K realtime trace buffer;
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   RS232 serial cable, external input probes and manual.

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## Generator places 60-psec rise-time pulses within 75 psec at 3 GHz

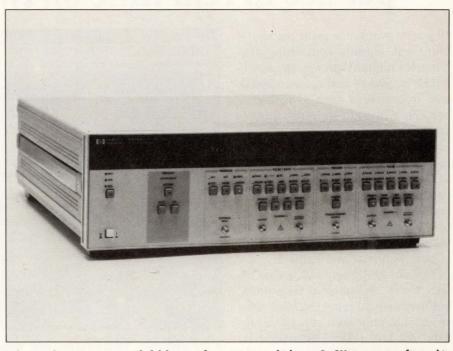
When you examine the fidelity and timing specifications of Hewlett-Packard's 8133A pulse generator, you may conclude that the unit provides just what you are looking for. The price ranges from \$27,100 to \$45,900, depending on options.

The instrument, whose output frequency extends from 33 MHz to 3 GHz, places its pulses with an error typically <75 psec (150 psec maximum) with respect to the edge of a trigger input. You can vary the pulse delay with respect to the trigger from -5 to 15 nsec. The maximum jitter in this placement is 5 psec rms; the typical jitter is <2 psec rms.

The rise and fall times of the generator's square waves and 150-psec to 10-nsec-wide pulses are 100 psec maximum—60 psec typical—measured from 10 to 90%. Measured from 20 to 80%, which some competitors use in their specifications, the worst-case and typical transition times are 60 and 40 psec, respectively. The generator produces pulses and square waves whose amplitudes into a  $50\Omega$  load are 0.1 to 3V.

You can obtain simultaneous normal- and inverted-polarity outputs. If you connect your  $50\Omega$  load to ground, you can vary the output offset from -2 to +4V. For work with ECL circuits, you can connect the  $50\Omega$  load to -2V. In this case, you can vary the offset from -3 to +3V.

Another feature that's unusual is the generator's optional second output that has some of the attributes of a data generator. Data generators usually have many channels and back each channel with pattern memory; but unlike pulse generators, they rarely offer much control over pulse parameters, such as delay and amplitude.



Pulses and square waves of fidelity at frequencies as high as 3 GHz emanate from this pulse generator. The unit can accommodate a channel that provides many of the attributes of a data generator.

This generator's optional second channel provides a 64-bit pattern memory. Though not deep by datagenerator standards, this memory suits testing devices and systems for pattern sensitivity. Moreover, you can connect two or three of the generators in a master/slave configuration, thereby obtaining a 6-channel generator. Instead of choosing a data generator as the instrument's second channel, you can choose a second pulse channel.

A related convenience—for example, for eye-pattern testing of high-speed communications channels—is the generator's ability to produce pseudo-random binary sequences. The length of these sequences can be as great as  $2^{23}-1$  periods.

The instrument's designers sacrificed one convenience for the sake of maintaining the unit's output fi-

delity: If you want to vary the rise and fall times of the output pulses, you must connect accessory filters between the output connector and the cable that drives your load. Making the rise and fall times variable from the front panel would degrade the generator's peak performance.

Aside from transition times, you can control just about every other aspect of the unit's output from its panel. A display provides warnings under conditions that degrade performance, such as when you select a pulse width that would produce a duty cycle approaching or exceeding 100%. Estimated delivery time is six weeks ARO.—Dan Strassberg

Hewlett-Packard Co, 19310 Pruneridge Ave, Cupertino, CA 95014. Phone (800) 752-0900.

Circle No. 731

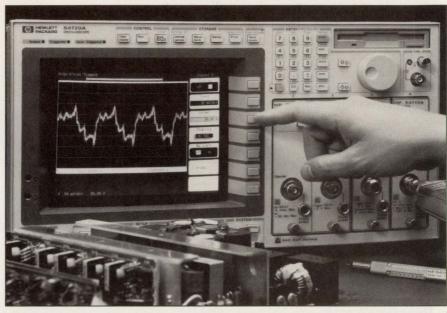
## Modular scope takes 4G 8-bit samples per sec in real time on two channels

If you've wanted a good picture of transient signals containing frequencies higher than approximately 0.5 GHz, you've had to use specialized instruments such as scan converters. Although such instruments are faster than most digital storage oscilloscopes (DSOs), they are also more expensive. Hewlett-Packard's 54720A DSO solves this problem for single-shot signals to 1 GHz by taking 4G 8-bit samples/sec on each of two channels. The 54710A scope takes 2G 8-bit samples/sec on each of two channels. See **Table 1**.

You can find many DSOs that offer *effective* sampling at GHz rates, but in nearly all cases the high rates are usable only with repetitive signals. All but a few DSOs (that is, the 547xx's and competitive units that take from 1 to 2 Gsamples/sec) acquire signals much more slowly (usually at 200 Msamples/sec or less). By capturing data at different points on many repetitions of identical waveforms, the slower scopes can reconstruct the signals as if the sampling rate were much greater.

Model	Number of channels	Sampling rate for each channel (in Gsamples/sec)		
54720A	2 4	4 2		
54710A	2	2		
54710A (with upgrade)	2	4 2		

But repetitive sampling doesn't work with signals that don't repeat or that repeat only once in a blue moon—metastable states are a good example. If you try to view such signals with a repetitive-sampling



A high-resolution, touch-sensitive, color display; a numeric keypad; a floppy-disk drive; a numeric keypad; and room for four single-width (or two double-width) plug-in modules distinguish the HP 54720A's front panel.

scope, you may not live long enough to acquire the samples you need to get a good idea of what's going on.

To capture transients, you need fast real-time sampling, but suppliers differ on the number of samples per cycle a scope must take to provide adequate waveform reconstruction. Although, in theory, you can reconstruct a signal that you have sampled slightly more than twice in each cycle, a rate of 4 samples/cycle is more practical and 10 or more samples/cycle are better yet. Using the DSP technique of reconstruction filtering, a scope can do a respectable job of waveform reconstruction at the lower 4-sample/cycle rate. This ratio limits the 54720A's single-shot bandwidth to 1 GHz. For repetitive signals, both the 54720A and the 54710A have a bandwidth of 1.5 GHz.

Other specifications worth noting are measurement of time intervals

with less than 30-psec error and a resolution of less than 1 psec; timing jitter of less than 5 psec rms; triggering on glitches as narrow as 500 psec; less than 300-µV rms noise; 9-bit resolution at 500 Msamples/sec; and 12-bit resolution with averaging. The scopes offer 32k words of memory on two channels and 16k words on four. They have high-resolution color displays.

The 54720A scope costs \$42,900, and the 54710A DSO costs \$29,900. Prices for plug-in modules range from \$2400 to \$4700, and a 2.5-GHz active probe with power supply costs \$3500. Delivery takes approximately 16 weeks ARO.

—Dan Strassberg

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## Software designs and checks board layouts

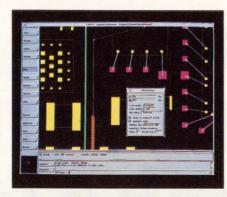
The Allegro CBD (correct-by-design) suite of tools facilitates board design by interactively checking design, electrical, and physical rules. As a result, the tools potentially eliminate iterative post-design verification and validation.

Post-design verification is inefficient because it lets you make errors. Even if you've properly defined the verification-rules set, you need to find, flag, and fix the errors and rerun the verification suite. The CBD system, however, finds the errors as you make them, thereby allowing the final design to meet all of your predefined constraints.

Electrical, physical, and thermal constraints are programmed into formats or templates in the Constraints Editor. The constraints can be of three types: always enforced, deferred until the design is batchmode checked, or not enforced. Even though the tools support batch-mode operation, if you don't defer rule checks, you can avoid batch-mode checks. In addition, you can lock constraints to prevent users from overriding them.

Each of the tools in the Allegro suite reads and writes the constraint files in an EDIF (Electronic Design Interchange Format). Consequently, if you define the constraints properly, you can avoid difficulties such as settling delays, timing skew, and signal reflections and crosstalk. The router avoids crosstalk, for example, by computing forward and backward crosstalk as it adds line segments, and rerouting those segments that cause the net to violate your thresholds. Similarly, the software can prevent skew errors.

To ease constraint development, you can also group signals, components, or other features. Further, you can define technology-depend-



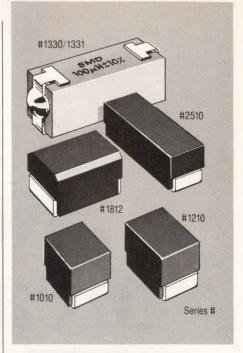
By ensuring that all constraints are observed within interactive and automatic tools, Allegro's CBD system breaks the design-and-then-analyze routine and lets you design correctly the first time.

ent or -independent constraints for particular conductor, dielectric, and positive- and negative-plane layers. Technology independence lets the software impose the constraints on boards fabricated using printed-circuit, hybrid, multiwire, or any of the multichip-module technologies. In contrast, you can also define constraints that are only valid in a particular implementation.

Because the constraint files are external to the software, you can read new constraints into an existing design. Unless you've explicitly turned off the capability, reading in new constraints may cause the Allegro software to modify your design to meet the new constraints. Alternatively, errors may set error flags.

The software is a free upgrade to Allegro customers who have a maintenance contract. Depending on software configuration, new users can purchase the software for \$12,500 to \$60,000 to run on Sun, DEC, IBM, and HP-RISC workstations.—Michael C Markowitz

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EDN March 2, 1992 • 117

## New Measurement Techniques

Though the test and measurement field is noted for conservatism, it is far from idle; T&M companies are constantly developing new technologies. These technologies may garner less attention than new µP architectures, but their effects on the industry can be just as profound.

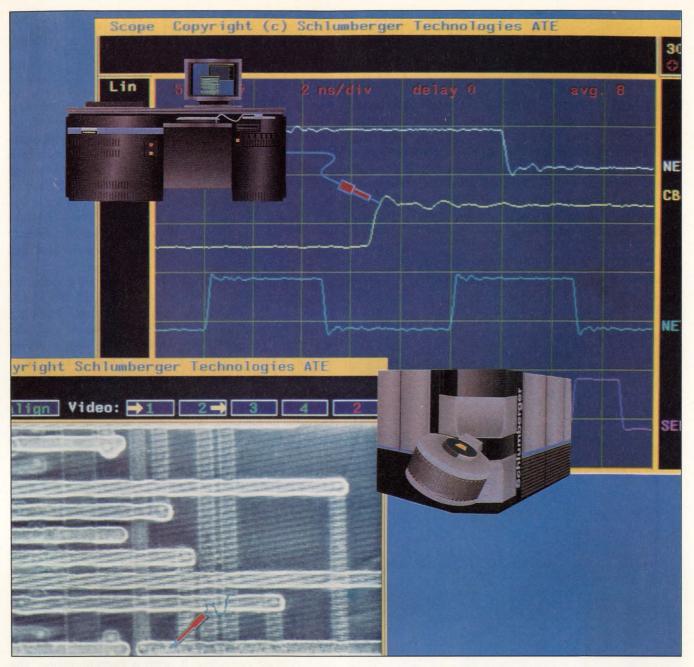
#### Dan Strassberg, Technical Editor

hen you think of test and measurement, maybe what comes to mind is a portion of our industry that time has passed by. If the term "test and measurement" conjures up images of crusty oldtimers suspicious of change . . . concerned only with limits of error measured in parts per billion . . . holed up in dusty labs . . . tinkering with antediluvian paraphernalia such as unsaturated standard cells housed in mahogany cases, then the field has passed you by. Although T&M people are indeed conservative—and rightfully so—and T&M technology doesn't move as rapidly as that in some other parts of electronics, instrument designers and T&M companies are constantly on the prowl for new ways to make measurements simpler and more accurate. In this report, EDN investigates some of these new techniques and a few of the products that implement them.

We'll look at systems that use electron and ion beams

to probe the innards of complex ICs, at a meter that measures current in a printed-circuit trace noninvasively, at digital scopes that overcome what you might think are fundamental limitations of sampled-data systems, and at products that make measurements in other novel ways. The subject area is too broad for in-depth coverage, so unlike most EDN Special Reports, this one will give you a fairly quick overview. We do hope, though, that by hitting the high spots, we'll whet your curiosity enough so that you'll want to learn more. One way to start is to contact the companies listed in the manufacturers' box. Every technique in this report is represented in products that are available now, and today isn't too soon to start thinking about the benefits you can derive from the techniques. However, the payoff from some of the techniques is sure to lie at least a few years down the road.

Four of the nine techniques covered address the



problem of debugging and testing complex ICs. In this area, we will look at electron-beam (E-beam) and focused-ion-beam (FIB) probing. We'll also look at a scheme that improves the observability of the internal workings of an ASIC. This scheme—named Crosscheck for the firm that developed it—does not require significant changes in the way the specifying engineer develops the device's design. And we'll look at  $I_{\rm DDQ}$  testing—a method for detecting faults in CMOS digital ICs that does not require you to propagate the faults back to the I/O pins of the device under test. (The IC's quiescent drain current,  $I_{\rm DDQ}$ , reveals the faults.)

Of these four technologies, E-beam and FIB probing are the best established. In the US, E-beam systems are available from Advantest and Schlumberger; FIB systems come from FEI, Micrion, Schlumberger, and Seiko.

Commercial ICs that embody Crosscheck's technol-

On the windowed display of a Schlumberger E-beam prober's workstation, you can simultaneously view a scanning-electron-microscope picture of a portion of the chip's surface and the voltage waveforms recorded at designated points within the displayed area. Insets show the prober and ATE system you use to stimulate the DUT. (Photo courtesy Schlumberger Technologies)

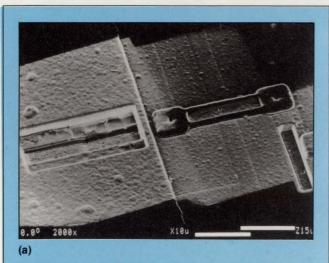
ogy are starting to appear. To make an IC testable, Crosscheck depends on specialized structures placed inside the chip. The firm does not manufacture ICs itself, but has licensed its technology to a handful of semiconductor companies: Harris, LSI Logic, and Raytheon in the US; and Fujitsu, NEC, Oki, and Sony in Japan. Crosscheck also sells test-development and fault-diagnostic software for use with ICs that incorporate its technology.

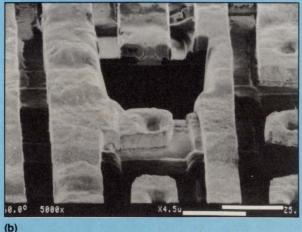
Though used without fanfare by several large IC houses since the '70s,  $I_{DDQ}$  testing is just starting to

give rise to commercial products. Although a few tester manufacturers, including Hewlett-Packard, provide the hardware necessary to implement  $I_{\rm DDQ}$  tests, and AT&T Microelectronics offers software that generates  $I_{\rm DDQ}$  test vectors, the technique's value is not yet acknowledged universally.  $I_{\rm DDQ}$  partisans point to impressive advantages in fault coverage, test-development time, and test time; conventional techniques still lead in fault localization.

#### DSOs foster measurement innovation

Among the measurement techniques discussed here, three are related to digital storage oscilloscopes (DSOs). One technique is the use of digital signal proc-





FIB probers can remove material from ICs, and when you hold chips at an angle to the ion beam, the systems also produce spectacularly clear 3-D images. In (a), repeated writing with the beam has removed material from the rectangular areas at the left center and lower right. In (b), near the top, just to the left of center, the metallization contains a void parallel to the chip's surface. This conductor appeared quite normal until the beam cut into it. (Photos courtesy Micrion Corp)

essing (DSP) ahead of a DSO's acquisition memory. This technique allows high-speed sampling even at low sweep speeds and does away with (or at least minimizes) aliasing, a phenomenon that can sometimes cause misleading waveform presentations. Tektronix's TDS 520 and 540 are two of the first commercial instruments to use the technique, which also appears in the even newer and lower-cost TDS 400 series. Besides the benefits of oversampling, the technique greatly increases the scopes' vertical resolution at low and moderate sweep speeds.

A competing technique is the use of acquisition memories as deep as 1 Msample. A group of new scopes from LeCroy offers this feature. (In units having a maximum sampling rate of 5 Msamples/sec or less, several firms compete. The lower-speed, deep-memory products have been on the market for several years.)

The third type of scope is the analog logic analyzer—a cross between a logic timing analyzer and a DSO. The instrument was introduced a few years ago by Outlook Technology. Biomation, which acquired Outlook, improved the product and reintroduced it as the K1600.

Time-interval analyzers (TIAs) have been around for over a decade, though, as **Ref 1** points out, they were considered specialized instruments until about four years ago. A technique called continuous measurement, popularized by Hewlett-Packard, has expanded the capabilities of TIAs and has been responsible for much of the heightened interest in the instruments.

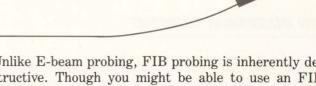
Last, Keithley Instruments has developed a noninvasive current-measurement technique and used it in a recently introduced digital multimeter (DMM). Although Keithley's 2001 may not be the first instrument to measure current in a conductor without cutting the conductor or encircling it with a current probe, the 2001 appears to be the first multifunction general-purpose meter to perform that feat.

# E-beam and FIB probing

Before the invention of the IC, all electronic circuits were made of discrete components. Back then, someone commented that electronics engineers didn't realize how fortunate they were—no other engineering discipline had a tool that came close to providing the kind of detailed insight available from an oscilloscope. As ICs replaced discrete components, and then began to increase in complexity, that fortuitous situation started to give way. No longer was it easy—no longer was it always even possible—to look within a circuit and get a picture of what was going on.

In a microelectronic world where mechanical-probe

# **EDN-SPECIAL REPORT**





The size of E-beam probers covers a fairly extensive range. This unit from Advantest is at the upper end of the range; the smallest units are about one fourth as large. This unit lets you create test setups that combine the prober with a VLSI IC tester that can stimulate the IC under test while you probe it.

access to circuit features is at least inconvenient (and often is simply impossible), E-beam and focused-ionbeam probers overcome that difficulty by replacing the mechanical probes with beams of electrons or gallium ions. These complex probing systems and the sophisticated software that drives them are restoring the kind of circuit visibility that EEs took for granted in discrete-component days. Of course, you pay a steep price for this high level of internal-node visibility: The least expensive beam probers cost more than a quarter of a million dollars. Systems costing three quarters of a million are not uncommon. And even if you could afford to have one of these probing systems on your lab bench, it wouldn't fit; the smallest ones are about twice the size of a washing machine. The good news is that beam probing loads critical circuit nodes far less than a scope probe would. Moreover, beam probers can often provide much more information than a scope would-if you could hook up a scope.

E-beam probers provide visibility. Not only do they perform the functions of a scanning electron microscope, they offer modes such as voltage-contrast imaging. This mode lets you highlight a node of interest and follow the circuit metallization—for example, to detect breaks. In another mode, you can view waveforms, just as you could on a sampling oscilloscope.

FIB systems can do even more. They can cut away portions of an IC and let you view the inside of the chip, as opposed to merely the surface features. They can also deposit metal. By using FIB systems' ability to make "cuts and jumps," you can find out whether a proposed chip-design modification really produces the desired effect. The reason that E-beam and FIB are considered complementary, rather than competitive, technologies is that FIB's capabilities exact a price.

Unlike E-beam probing, FIB probing is inherently destructive. Though you might be able to use an FIB system to safely observe a chip for a short time, if you continue, you'll remove enough material to impair or destroy the chip's function.

The navigational software that drives beam-probing systems adds to the systems' gee-whiz character. For example, on the windowed display of a Schlumberger prober's workstation, you can simultaneously view a scanning-electron-microscope picture of a portion of the chip's surface, the corresponding sections of the chip layout and schematic, and the voltage waveforms recorded at designated points within the displayed area. Moreover, as you move the chip with respect to the beam to probe different points, or zoom in to observe a particular feature in greater detail, the displays change in synchronism. After witnessing a demonstration, only a confirmed cynic or someone seriously jaded from an overdose of high technology could fail to come away with the impression: "I have seen the future, and this is it."

Beam-probing-system manufacturers aren't resting on their laurels, though. For example, this year will see guided-probe fault diagnosis come to E-beam probers. Schlumberger makes automatic test systems for ICs and circuit boards as well as beam probers. The company will soon announce software tools that work with its hardware to automatically locate prob-



You get the benefits of a high sampling rate even at low sweep speeds from Tektronix's TDS 500 scopes. Pre-acquisition-memory averaging keeps the Nyquist frequency high and improves the resolution of small signals while still providing quick response to changing signals.

lems in ICs. Using guided-probe technology to isolate pc-board faults is not new, but using the technique to localize IC faults is. Although the new tools don't replace human operators, they should greatly increase operator productivity. The idea is that you can apply test vectors to an IC positioned on a beam prober just as you can to a board on a board tester. Based on the test results, you can progressively home in on the areas of the chip where problems exist. Without the intelligence added by the software tools, locating IC faults often involves intuition and guesswork.

# Crosscheck

Crosscheck is a means of designing and building ICs that let you observe internal-node states. The biggest payoff from the technique is for complex ASICs. If you were to create an otherwise similar IC using conventional techniques, finding out what was going on inside the device would be much harder. The technique calls for you to modify a chip in ways that, mostly, affect neither its performance nor its interface with other devices. Nor does Crosscheck affect the steps that the specifying engineer must take to provide a design to the foundry that builds the IC.

The heart of Crosscheck's technology is a group of tiny p-channel field-effect transistors (FETs) built into an IC's silicon substrate. These FETs form a miniature switching matrix that lets you determine the logic states at internal circuit nodes. Because the test circuits that the matrix drives have a high input impedance, the FETs can have high on-resistances, and hence can be quite small. A 4-pin IEEE-1149.1 test



A 1-Msample memory doesn't make LeCroy's 9300 scopes large or odd in appearance. Casual observers may even miss the small slot at the lower right that accepts credit-card-size memory cards that store waveforms and setups.

port lets you control the matrix and observe the internal logic levels.

The nonrecurring engineering fee you'll pay to an IC company for an ASIC embodying Crosscheck is comparable to that for a device that is similar but lacking in testability features. Although the recurring cost of Crosscheck devices may be slightly greater than that of parts that haven't been designed for test, the technology should still yield increased profits. The bottom-line benefits stem from reduced time-to-market, which results from quicker verification that the devices perform as intended. The increased unit costs reflect the slightly increased device area (although the percentage of extra area declines as the device complexity rises) and from the additional package pins used by the testability port.

# IDDQ testing

 $I_{\rm DDQ}$  testing is named for the measured parameter, which is the quiescent drain current of the CMOS IC under test. Under quiescent conditions, a CMOS IC's drain current (the current it draws from the power supply) is normally measured in microamperes. Under the right conditions, however, failures within the IC can cause much higher drain currents.

CMOS logic uses pairs of complementary n- and pchannel MOSFETs as its active circuit elements. These devices have insulated gates; a layer of oxide separates a device's gate from its channel. Most failures within CMOS ICs are the result of minute pinholes in the insulating oxide layer. If there is a pinhole in the oxide of a FET whose channel is connected to the negative supply rail (that is, the supply terminal you normally connect to ground) and you drive the FET's gate to the positive supply rail, a relatively large current will flow between the positive and negative rails. Similarly, if there is an oxide failure between the gate and the channel of a FET whose channel connects to the positive rail and you drive the gate of the FET to the negative rail, a relatively large current will flow from rail to rail. As long as you continue to stimulate a fault, the larger-than-normal current will continue to flow.

By monitoring an IC's power-supply current, you avoid a significant problem that plagues more-conventional methods of testing complex digital ICs—propagating faults back to I/O pins. In a sense, then,  $I_{\rm DDQ}$  testing takes aim at the same problem that Cross-check addresses: observability. But Crosscheck is much more a technique for design verification, whereas  $I_{\rm DDQ}$  is mainly for testing devices whose design you're confident is OK.

# **EDN-SPECIAL REPORT**

 $I_{\rm DDQ}$  partisans claim some impressive advantages for the technique. Take these results obtained using an automatic test-pattern-generation package called Gentest from AT&T Microelectronics. Gentest runs on Sun workstations and sells for about \$150,000. For one test circuit (35 inputs; 320 outputs; 1728 flip-flops; 16,065 gates), Gentest took approximately eight hours to produce a set of conventional test vectors that provide 89.7% coverage of stuck-at faults. The same software took 38 sec to produce a set of  $I_{\rm DDQ}$  vectors that provide 100% fault coverage. (Stuck-at faults are ones that prevent internal nodes from leaving a logic 1 or a logic 0 state.)

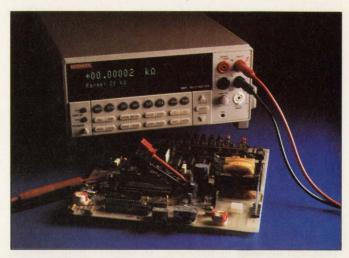
There are only 88 vectors in the  $I_{\rm DDQ}$  set, far fewer than the number in the conventional set. AT&T says that a production IC tester should be able to output 100k vectors/sec (limited by the ICs' settling time), so test time should be quite short. The result of using  $I_{\rm DDQ}$  tests on circuits like this one should be a dramatic reduction in test-development time as well as faster testing and, hence, lower cost for each device.

Not everyone is sanguine about such reports. Establishing  $I_{\rm DDQ}$  test limits for a particular part apparently requires some experimentation and testing thousands of samples. Also, many old hands at testing digital ICs automatically become skeptical at the first mention of 100% fault coverage. Nevertheless,  $I_{\rm DDQ}$  partisans are confident that the test world will eventually come around to their point of view. They stress, for example, the technique's ability to reveal faults that don't cause devices to function incorrectly but do indicate process problems that can presage early failures.

# DSOs with advanced features of two kinds

Digital oscilloscopes have changed the electronics engineer's world forever. That isn't to say that they have wiped out analog scopes—users in electronics and other industries continue, year after year, to order large numbers of the more traditional instruments. One reason for analog scopes' continued popularity is engineers' mistrust of DSOs. Despite DSOs' many advantages (see Ref 2), most have quirks that make them more likely than analog units to produce misleading displays.

DSOs are sampled-data systems. They recreate the waveforms you see on their screens from series of digitized samples of instantaneous input-signal voltages. Although some DSOs work in real time at all sweep speeds, ones that use a technique called random equivalent-time sampling at the higher sweep speeds are more common. Equivalent-time sampling lets a



Measuring current without interrupting the circuit or encircling a conductor with a current probe is just one of the Keithley 2001's claims to fame.

scope digitize repetitive waveforms at high effective rates—even when the sampling rate required to accurately reconstruct the input signal exceeds the maximum at which the sampler can operate. As you lower the sweep speed, almost all such scopes eventually switch back to real-time sampling. It is in this mode, at low sweep speeds, that aliasing can cause most DSOs to display nonexistent signals.

The well-known Nyquist theorem says that to prevent aliasing you must sample a signal more than twice during the period of the highest frequency component whose amplitude is great enough to interest you. All DSOs have acquisition memories of finite depth. When a conventional DSO operates in the real-time mode, as you slow its sweep speed, the finite memory depth forces the scope to slow its sampling rate. As the sampling rate decreases, so does the signal frequency above which aliasing can occur. (This frequency—half the sampling rate—is called the Nyquist frequency,  $f_{\rm N}$ .)

Tektronix's TDS 400 (from \$5995) and 500 (from \$9490) series DSOs overcome this problem by sampling at a high rate regardless of the sweep speed. The 500 series scopes use digitizers that can take 250 Msamples/sec, and you can use as many as four digitizers to sample one signal as fast as 1 Gsample/sec. However, the scopes' waveform memories—which hold as many as 50,000 samples/channel—are not deep enough for all of the samples acquired during, say, a 50-msec sweep. Using a single digitizer, if every sample went into memory, such a sweep would involve 12.5 million samples.

In this example, if the scope discarded 249 samples out of every 250, the memory problem would go away, but so would the advantages of fast sampling. The solution that Tektronix's engineers devised was to ac-

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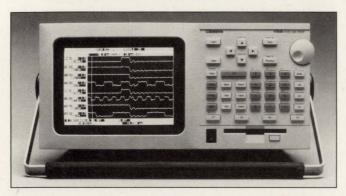
cumulate (sum) a series of samples *before* placing them in waveform memory. Although the scopes have 8-bit digitizers, the waveform memory can hold 16-bit words. The scopes appropriately scale these long words before displaying them.

## Not just faster-higher resolution

A benefit of the technique is that it produces enhanced resolution—16 bits vs 8—which lets you view signals so small you couldn't normally see them. Because the sampling rate remains high, the Nyquist frequency also remains high. This technique is different from the averaging feature that many DSOs offer to reduce random noise superimposed on waveforms. Such DSOs do their waveform averaging after the samples are already in memory. To acquire long sweeps, they must slow their sampling rates, just as when averaging is not in use. The slower sampling reduces the Nyquist frequency and slows down display updates, thus the display often responds sluggishly to signal changes.

An obvious, but heretofore prohibitively expensive alternative to averaging ahead of a scope's waveform memory is to use a deeper memory. (Remember, a fast DSO's waveform memory is not the relatively inexpensive dynamic RAM found in all PCs, but costly high-speed static RAM.) Until Tektronix introduced the DSA 602 in 1989, if you wanted a DSO with bandwidth of 100 MHz or more and memory deeper than a few thousand words, LeCroy was the only game in town.

Now that Tektronix is competing with LeCroy in high-speed DSOs that have memory depths in the tens of thousands of words, LeCroy has upped the ante. Its 9300 DSOs and two plug-ins for its 7200 (mainframe price: \$17,000) have memories of 1 Mword/channel. The 2-channel, 300-MHz version of the 9300 series scope with a memory of 1 Mword/channel sells for \$9990.



The eight on-screen traces should be your first clue that Biomation's K1600 is no ordinary scope. In fact, the firm calls it an analog logic analyzer—a logic timing analyzer whose analog capabilities let it resolve anomalies in waveforms on any channel or on all 16 channels simultaneously.

Those willing to forego the deep memory can save even more; a version with 10 kwords/channel (still more than what the majority of DSOs offer) sells for \$4990. As an added feature, all of LeCroy's scopes now let you store waveforms and setups in credit-card-size plug-in memory cards.

The 9300 scopes take a maximum of 100 Msamples/sec. Filling the 1-Mword memory during the previous example's 50-msec sweep requires operating the digitizer at 20 Msamples/sec. At that speed,  $f_{\rm N}$  is 10 MHz vs 125 MHz for the Tektronix TDS 500 series scope with the optional 50-kword memory and with one digitizer in use. Note, however, that 1 Mword of memory is deep enough to retain the original sampled data; pre-acquisition-memory averaging loses it because averaging destroys the original data by combining adjacent samples. Regardless of which of these two scopes you choose,  $f_{\rm N}$  will be at least 1000 times as high as the 10 kHz you'd have to accept if you used a conventional DSO with a 1-kword memory.

# **Analog logic analyzer**

As logic gets faster and faster, the line of demarcation between the digital and analog worlds becomes less and less clear. Troubleshooting fast logic usually involves both a logic analyzer and a high-speed scope. The idea that you'd really like to use a single instrument and a single set of probes to make either type of measurement on any or all channels is what's behind Biomation's K1600 analog logic analyzer. In an earlier incarnation (from Outlook Technology, a firm that Biomation acquired), the product was called a logic oscilloscope. The 16-channel benchtop unit has a 4-bit (16-level) ADC for each channel and a 1-ksample/channel memory. It sells for \$14,950.

The analyzer can take 100 Msamples/sec simultaneously on all of its 16 channels or, through multiplexing, 200 Msamples/sec on eight channels, 400 Msamples/sec on four channels, or 800 Msamples/sec on two channels. The vertical amplifiers have a bandwidth of 350 MHz, so in the real-time-sampling mode you can take advantage of the full bandwidth only if you multiplex the unit's inputs to sample two channels at 800 Msamples/sec. With repetitive signals, however, equivalent-time sampling improves the time resolution to 50 psec and lets you use the full bandwidth on all channels. Moreover, with equivalent-time sampling, the voltage resolution increases to six bits (64 levels).

The unit's ability to resolve more than two voltage levels is, of course, the most obvious feature that sets it apart from logic-timing analyzers. The things that set the instrument apart from nearly all DSOs, besides



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the number of channels, are logic-analyzer-like features such as the ability to display an 8-character label for each trace and the logic-analyzer-style triggering. (Among general-purpose DSOs, Tektronix's TDS 500 series also incorporates many logic-analyzer-like triggering features. A mode in which the TDS scopes trigger on undersized pulses—so-called runt pulses—can be particularly helpful in tracking down elusive logic malfunctions.)

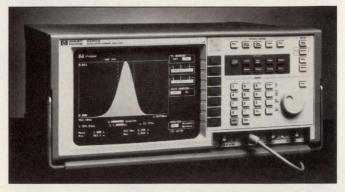
Adding to the K1600's flexibility is its ability to behave as a digital instrument. You can specify the 1 and 0 thresholds from  $-40\mathrm{V}$  to  $+40\mathrm{V}$  in 0.1V steps, and you can replace the waveform displays with binary or hexadecimal representations. With 3-state devices, you can display the intervals during which outputs are in the high-impedance state as cross-hatched regions. The instrument incorporates a 9-in. monochrome display, but you can obtain a high-resolution color presentation by connecting a color monitor of the type that normally accepts an MS-DOS PC's VGA  $(640 \times 480\text{-pixel})$  output.

# Continuous-measurement timeinterval analyzers

Hewlett-Packard's 1987 introduction of a line of products the firm calls modulation-domain analyzers changed forever the industry's perception of time-interval analysis. (EDN avoids using the abbreviation MDA for any type of time-interval analyzer because in a large part of the test-equipment industry, MDA has—for decades—referred to manufacturing-defects analyzers, a type of pc-board tester unrelated to time-interval measurements.)

Conventional, pre-1987 TIAs provide information on the statistical distribution of a large number of frequency or interval measurements made in rapid succession. The HP products pioneered in providing information on how the measured quantities vary over the course of a sequence of measurements. In other words, the instruments provide a picture of how interval durations or frequencies vary as a function of time.

One of the keys to providing this capability is a technique called continuous measurement. The technology of frequency and interval measurements is inextricably tied to that of binary counters. HP's continuous-measurement technology (Ref 3) addresses the problem of accurately reading the contents of a binary counter "on the fly," that is, while the counter continues to receive new inputs. The analyzers work by capturing a snapshot of the current count each time they recognize the occurrence of an event that meets criteria you have established. With this technology, following an event, there is no dead time before the analyzer



Finding out how frequencies and time intervals vary as a function of time is possible with time-interval analyzers, such as Hewlett-Packard's 53310A. The unit's continuous-measurement technology is the key to its capabilities.

can capture the next event. As with any frequency-or time-measurement instrument, however, there is a maximum specified input rate.

HP's family of modulation-domain analyzers includes four members priced from \$9500 to \$32,000. They directly accept input frequencies as high as 500 MHz (18 GHz with a prescaler). The lowest priced unit, the 53310A, accepts direct inputs as high as 200 MHz.

# **Noninvasive current measurement**

Keithley Instruments' 2001 digital multimeter is a complete bench or system DMM having 7½-digit resolution, accuracy commensurate with that resolution, wideband true-rms ac-measurement capabilities, high measurement speed, and advanced triggering features. Although that range of capabilities, coupled with a price lower than that of many comparably accurate DMMs (\$2695), should spark plenty of interest, another feature is the reason for the instrument's appearance here: The 2001 incorporates a novel measurement mode that lets it do the seemingly impossible: It measures the ac or dc current in a conductor by using a pair of test probes across the conductor. The measurement is noninvasive; it doesn't require cutting the conductor or encircling it with a current probe.

The secret behind this capability lies in the meter's computational power as well as in some novel analog technology. To make a noninvasive current measurement, you usually use the meter by clamping a pair of Kelvin clips (which have two wires per clip) onto the conductor whose current you want to measure. Until you close a clip on a conductor, its two jaws are isolated from each other. The clips allow the meter to force a current pulse through the conductor (using one jaw on each clip) and to simultaneously measure the amplitude of the resulting voltage pulse (using the mat-



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ing jaws). By dividing the voltage pulse amplitude by the current forced, the meter calculates the conductor's resistance. The meter then determines the current in the conductor by dividing this calculated resistance into the ac or dc voltage measured across the conductor. As long as the forced current pulse doesn't cause the circuit under test to misbehave, and as long as the conductor's resistance doesn't approach zero too closely, the meter can make the noninvasive current measurement with less than 1% error.

This technique is sure to prove invaluable in such areas as the application of power supplies. In such work, connecting an ammeter between a supply and its load can be more than inconvenient; it can affect the supply's point-of-load regulation enough to degrade the performance of the equipment that receives the power. Moreover, using the supply's remote-sense feature to restore the regulation often creates its own problems, such as poor dynamic response. In such situations, the 2001 can save the day. If you place its probes as little as six inches apart across a 14-gauge conductor, the meter can measure the current with an error of less than 1%.

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> Article Interest Quotient (Circle One) High 476 Medium 477 Low 478

# Manufacturers mentioned in this article

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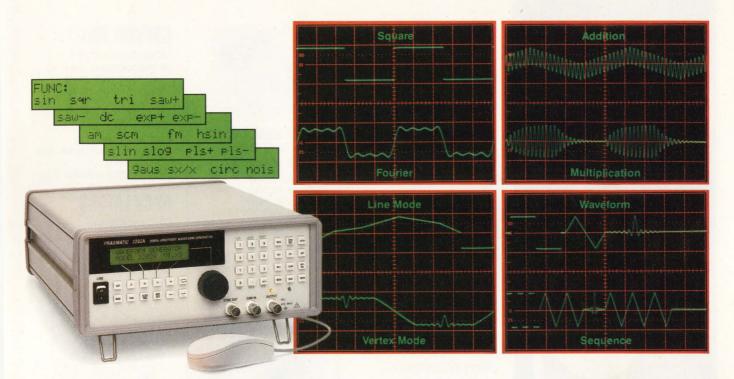
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# **EDN-DESIGN FEATURE**

**Communications Technology** 

# Use spectrum analyzers' selectivity to precisely measure random noise

Kevin Johnson, Hewlett-Packard Co

Because a spectrum analyzer makes a variety of measurements, such as signal power, frequency, flatness, and distortion, it may be the most convenient, though not the most obvious, instrument to use when measuring noise.

You may have used power meters, voltmeters, noise-figure meters, and even oscilloscopes to make noise-level measurements, but a spectrum analyzer offers at least one distinct advantage over these other instruments: frequency selectivity. Most of the other noise-measurement techniques only provide a reading of the total noise power across the measuring instrument's entire bandwidth. A spectrum analyzer's frequency selectivity not only allows you to measure noise at one precise frequency but, by measuring the noise level at several frequencies, it also allows you to determine the "shape" of the noise in the frequency domain.

A spectrum analyzer's frequency selectivity allows it to measure noise levels independently of spurious signals that may accompany the noise. Other noise-measurement methods that are not frequency-selective measure the total power of all signal components. The frequency selectivity and the large dynamic range of most spectrum analyzers will allow you, for example, to measure the phase or amplitude noise sidebands of a carrier directly without using a detector to eliminate the carrier.

Spectrum analyzers are usually designed to measure the spectral components of deterministic signals, not noise. For this reason, you must pay special attention to instrument settings and readings when you use a spectrum analyzer to measure noise. Many spectrum analyzers have a noise-level function that will help you automate noise measurements. Some have a noise-level function that will pause to make a special noise measurement during each sweep at a marker frequency that you select. Others will automatically use correction factors to adjust for the spectral characteristics of noise. In either case, a spectrum analyzer's noiselevel function can save you considerable time and effort when you're measuring noise. However, you must first understand what your analyzer's noise-level function does before you can measure noise correctly.

Spectrum analyzers fall into two categories: instruments with postdetection digitizers and instruments with predetection digitizers. Older instrument designs generally have postdetection digitizers. Newer designs employ fast A/D converters as predetection digitizers.

Most spectrum analyzers with postdetection digitizers (Fig 1) measure the average voltage envelope of signals within the operator-selected resolution bandwidth and calculate power by treating the signal as a single tone instead of measuring the power directly. The IF (intermediate frequency) section of a spectrum analyzer with postdetection digitizing is particularly well suited for accurately measuring the level of a single tone in the presence of noise. However, because

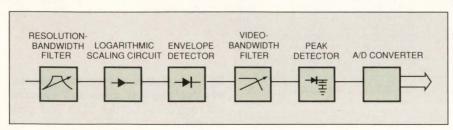


Fig 1—A spectrum analyzer with postdetection digitizing employs hardware filters and a slow A/D converter in its intermediate frequency section.

## NOISE MEASUREMENTS

these spectrum analyzers are not optimized for measuring noise, you must apply correction factors to their amplitude readings.

Spectrum analyzers with predetection digitizers (Fig 2) have an all-digital IF section; an analog antialias filter limits the bandwidth of the IF signal, and an A/D converter measures samples of the IF signal at a rate that is greater than 2× the bandwidth of the signal. In a spectrum analyzer with predetection digitizing, the resolution-bandwidth filter, IF detector, videobandwidth filter, and video detector are all mathematical algorithms, so their characteristics are precisely known. Spectrum analyzers with predetection digitizing can automatically calculate noise levels from the digitized data.

### Factors that affect measurement accuracy

Five factors affect the accuracy of random-noise measurements made by any spectrum analyzer. These factors are resolution bandwidth, IF-detection characteristics, video-detection characteristics, averaging, and spectrum analyzer noise.

The analyzer's resolution-bandwidth setting determines the noise frequencies of interest just as it does for deterministic signals. You can model noise as an infinite number of frequency components, each contributing an infinitesimal amount of power. Each of these components has random amplitude and phase. Using this model, the noise level measured by an analyzer with an infinitesimally narrow resolution-bandwidth setting will be zero. At the other extreme, the noise level measured by an analyzer with an infinitely wide resolution-bandwidth setting will be infinite. Although these extremes are strictly hypothetical, this noise model illustrates two important principles: the total power measured is directly proportional to the analyzer's resolution-bandwidth setting and the randomnoise power at a specific frequency must be expressed as a density such as noise power per unit bandwidth.

By convention, noise-power measurements are usually normalized to a 1-Hz bandwidth. If the noise is reasonably flat within the resolution bandwidth, the noise-power density at the frequency of interest is the total power you measure divided by the analyzer's

noise-power bandwidth. The noise-power bandwidth normalization factor, in dB, is

normalization factor =  $10*LOG(1/(BW_n))$ ,

where  $BW_n$  is the noise-power bandwidth. You simply add  $10*LOG(BW_d)$  to renormalize the result to any desired bandwidth ( $BW_d$ ).

A spectrum analyzer's noise-power bandwidth, or equivalent noise bandwidth, is an ideal rectangular filter bandwidth that has the same power response to flat noise as the analyzer's resolution-bandwidth filter (Fig 3). The instrument manufacturer usually specifies the noise-power bandwidth of the analyzer's filter, but you can also calculate it by displaying the shape of the filter, on a linear power scale, and finding the area under the curve.

For spectrum analyzers with postdetection digitizers, the noise-power bandwidth is between 1.5 and 1.11 times the resolution bandwidth, depending on the shape factor and order of the filter. The filter's shape factor is the ratio between the 60-dB bandwidth and the 3-dB bandwidth of the filter. The smaller the shape factor, the greater the selectivity and the closer the filter is to an ideal rectangular filter. For example, the HP 3585B is a spectrum analyzer with postdetection digitizing that has 5-pole resolution-bandwidth filters with shape factors of 11:1 and noise-power bandwidths that are 1.11 times the resolution bandwidth.

The algorithmic resolution-bandwidth filters in analyzers with predetection digitizers can have much smaller shape factors than the circuitry-based filters in analyzers with postdetection digitizers. For example, the HP 3588A resolution-bandwidth filter has a shape factor of 4:1 and a noise-power bandwidth that is 1.06 times the resolution bandwidth.

#### Hardware filters have accuracy limits

The typical resolution-bandwidth accuracy of a spectrum analyzer with postdetection digitizing is  $\pm 20\%$  (+0.8, -1.0 dB). Therefore, when you make noise measurements with these spectrum analyzers, large errors will frequently result if you calculate the noise-power bandwidth using the nominal value of the resolu-

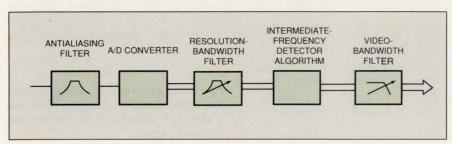


Fig 2—A spectrum analyzer with predetection digitizing uses a fast A/D converter and algorithms for the filters and peak detector.

# **EDN-DESIGN FEATURE**

tion-bandwidth setting. Unless you measure the bandwidth error, you must use the accuracy specification supplied by the instrument vendor. A distinct advantage of analyzers with algorithmic resolution-bandwidth filters is that the resolution bandwidth and noise-power bandwidth of each filter are precisely known and do not vary from instrument to instrument.

After passing the signal through the resolution-bandwidth filter, a spectrum analyzer uses an envelope detector in the IF section to produce a "video signal." Spectrum analyzers with postdetection digitizing use circuitry to implement the IF detector. These circuit-based detectors produce different readings for random noise and single tones with the same power because narrowband white noise has an envelope that can be described by the "Rayleigh distribution" (Ref 1). Consequently, a spectrum analyzer with postdetection digitizing operating in its linear voltage-display mode will underestimate noise power by a factor of 12.8% or 1.05 dB.

The log-scaled display mode of such spectrum analyzers will also introduce errors in noise measurements. In a logarithmic-display mode, a logarithm-scaling circuit shapes the IF signal before that signal is applied to the detector. Shaping compresses the noise signal peaks. The average of the logarithmic voltage envelope is given by:

$$\int_{0}^{\infty} 20*Log(R)*P(R)dR = 0.5.$$

where R is the normalized instantaneous signal voltage and P(R) is the probability distribution of the envelope of the narrow-band noise signal. The answer (0.5) was found by numerical integration. A single tone having the same rms power has a log-scaled envelope with a value of

$$20*LOG(\sqrt{2}) = 3.0.$$

Thus if you use a video-bandwidth filter to average the log-scaled signal, or if you find the log-scaled signal's average by computing the mean of many samples, then a spectrum analyzer with postdetection digitizing will underestimate noise power by 2.5 dB.

#### True rms readings effectively measure noise

Spectrum analyzers with predetection digitizing implement the IF detector with a mathematical algorithm that provides a true estimate of the rms power for any type of signal. No matter what the distribution of the noise signal, the total noise power is detected accurately without correction factors.

The output of the IF detector is called the "video

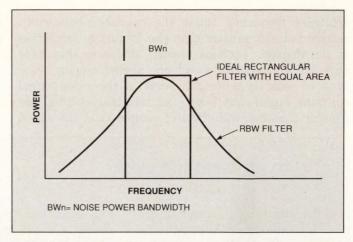


Fig 3—A spectrum analyzer's noise-power bandwidth, or equivalent noise bandwidth, is an ideal rectangular filter bandwidth that has the same power response to flat noise as the analyzer's resolution-bandwidth filter.

signal." A spectrum analyzer with postdetection digitizing usually passes the video signal through a videobandwidth filter and a peak detector. It then samples the resulting signal with an A/D converter. The A/D converter's sample rate restricts readings in a single sweep to a finite number of frequency points (usually 1000). A peak detector allows an analyzer to measure and display signal peaks even if they occur between samples. Spectrum analyzers with predetection digitizers do not need a hardware peak detector because the A/D converter sample rate is much greater than the largest resolution bandwidth of the analyzer.

For both analyzer types, the effective sample rate decreases when the actual sweep time is greater than the instrument's minimum sweep time. For example, at twice the minimum sweep time an analyzer takes two samples for every display point. Because the analyzer will display and store only one of these samples, the effective sample rate is decreased by a factor of two. The effective sample rate is the number of displayed frequency points divided by the sweep time.

Three basic schemes help choose which samples to display and, in the case of the analyzer with postdetection digitizing, what type of hardware peak detection to employ in front of the A/D converter. These videodetection schemes are positive peak detection, sample detection, and normal or "Rosenfell" detection. Some spectrum analyzers have only one type of video detection, whereas others allow you to choose between two or more video-detection modes.

When the spectrum analyzer is sweeping, positive peak detection ensures that the CRT always displays the signal peak. Without peak detection, you cannot accurately measure the amplitude of a single tone of

### **NOISE MEASUREMENTS**

arbitrary frequency unless the resolution-bandwidth setting is much greater than the frequency resolution of the display. For this reason, analyzers that have only one video-detection scheme always employ some type of peak detection. However, if the video signal contains significant power at frequencies that are greater than half the effective sample rate, the signal will be undersampled. The combination of positive peak detecting and undersampling will cause the noise level to appear higher than it really is.

There are two ways you can avoid the noise bias caused by undersampling and positive peak detecting in a spectrum analyzer. The first method is to reduce the analyzer's video bandwidth to a value that is much

# How to measure the noise

The noise-level function available in some spectrum analyzers automatically applies an IF-detector correction factor and an approximate resolution-bandwidth normalization factor to the marker readings, yielding a good estimate of the noise-power density. Furthermore, some noise-level functions actually make the measurement for you, automatically controlling the video detection mode, the video bandwidth filter selection, and the averaging method to ensure the measurement is set up correctly. If you measure random noise without using a noise-level function, then you should use the correction factors presented in this article to correct the amplitude readings. The following measurement examples illustrate how to apply the correction factors.

**Example 1:** Suppose you want to use a spectrum analyzer with postdetection digitizing that has a 5-pole, 30-kHz resolution-bandwidth filter to measure a random noise signal that is much larger than the analyzer's noise floor. If the analyzer has a sample video-detection mode, select this mode to eliminate the bias caused by the video peak detector.

If the analyzer does not have a sample detection mode, set the video bandwidth to 300 Hz or less. This setting will average the video signal enough to eliminate the bias. Either use the analyzer's video-average function or average sev-

eral readings manually to reduce the variance of the measurement further. Correct and normalize the amplitude readings as follows:

where -45.2 is the resolution-bandwidth normalization:

$$10*LOG(\frac{1}{1.11*30 \text{ kH}_2})$$

and 2.5 is the IF detection correction factor (LOG mode). To renormalize the result to any desired bandwidth (BWd), add 10\*LOG(BWd).

One of the greatest sources of error in a noise measurement made by a spectrum analyzer with postdetection digitizing is the uncertainty of the resolution-bandwidth. To reduce this uncertainty, measure the 3-dB bandwidth of the resolution-bandwidth filter and replace the nominal value in the example above with the measured value.

**Example 2:** Suppose you want to use a spectrum analyzer with predetection digitizing to measure random noise in a 17.1-kHz resolution bandwidth. Assume the noise floor of the analyzer is only 6 dB below the total noise level measured with the signal present. Select the sample video-detection mode to eliminate the bias caused by the

video peak detector. Use a narrow video-bandwidth filter or video averaging to reduce the variance of the measurement to the desired level. Correct and normalize the amplitude readings as follows:

where -42.6 is the resolution-bandwidth normalization:

$$10*LOG(\frac{1}{1.06*17.1 \text{ kH}_2})$$

and -1.3 is the analyzer noise correction:

$$10*LOG(1-10^{\frac{-6}{10}}).$$

Again, to renormalize the result to any desired bandwidth (BWd), add 10\*LOG(BWd).

Because a spectrum analyzer with predetection digitizing employs a true-rms IF-detection algorithm, there is no IF-detection correction factor for random noise or any other type of complex signal. In addition, this type of analyzer's noise-power bandwidth is precisely known and is repeatable. You can therefore make accurate noise measurements without directly measuring the 3-dB bandwidth of the resolution-bandwidth filters.

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less than the resolution-bandwidth setting. When you use a video bandwidth that is at least 100 times less than the resolution bandwidth, the signal at the output of the video bandwidth filter will be at a nearly constant level and the peak detector bias will be small.

The second way to avoid noise bias is to reduce the combination of the video and resolution bandwidths so that the signal at the input of the peak detector has a bandwidth that is much less than half the effective sample rate. If the signal is sufficiently oversampled, the peak detector bias will be small.

Many analyzers with postdetection digitizing allow you to set the video detection scheme to a "sample" mode that bypasses the hardware peak detector. The sample mode may undersample the noise, but it will give you an accurate estimate of the noise level because the readings will not be biased by peak detection. However, because the peak of the video signal might not be displayed in the sample mode, you cannot accurately measure the level of a single tone unless the resolution bandwidth is much greater than the display's frequency resolution.

Some analyzers have a third video detection mode that attempts to solve the problems of positive peak detection and sample detection. In this mode, the analyzer alternately displays positive and negative peaks of the video signal if the signal "looks" like noise. It displays only the positive peaks if the signal looks like a single tone. The analyzer assumes that the signal being measured is noise if the signal "rose and fell" between samples. Consequently, this type of video detection is commonly called "Rosenfell" detection. It is the default or normal peak-detection mode in spectrum analyzers that incorporate it. Rosenfell detection correctly displays single-tone levels and average noise levels.

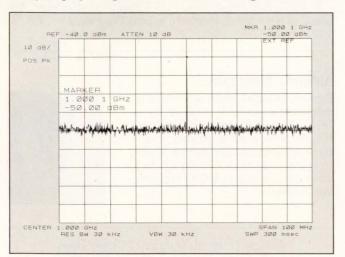


Fig 4—Positive peak detection accurately measures tone levels but biases the measured noise level.

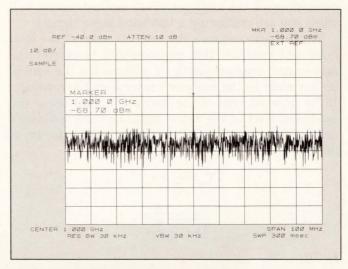


Fig 5—Sample detection measures noise levels without bias but doesn't measure tone levels accurately.

Figs 4, 5, and 6 illustrate the effect of each videodetection scheme when the video signal is undersampled. Positive peak detection is employed in Fig 4. Note that the level of the tone is measured accurately but peak detection biases the measured noise level. Sample detection is employed in Fig 5 and the noise level is unbiased, but the level of the tone is not measured accurately. In Fig 6, Rosenfell detection is employed. The Rosenfell display shows the tone and the average of the noise level correctly.

Many spectrum analyzers have a video-averaging feature that allows you to average the results of many sweeps. The confidence level of the average reading is proportional to the square root of the number of samples. Thus, the average of 100 samples is ten times better than a single sample. You can also make an average measurement using a narrow video filter. If the video bandwidth setting is less than the resolution-bandwidth setting, then the variation in the noise readings will decrease by a factor directly proportional to the square root of the video bandwidth divided by the resolution bandwidth. A video bandwidth setting will give effective averaging for most noise measurements.

Settings alone will not give you accurate noise measurements. You must also compensate for the inherent noise in the spectrum analyzer. To estimate the power of a random noise signal accurately, the noise level you measure should be at least 10 dB above the analyzer's internal noise. If this is not the case, the internal noise of the analyzer will combine with the noise signal, causing the noise measurement to be too high. You can eliminate this problem by using a preamplifier to boost the level of the noise signal until it is well above the

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noise floor of the analyzer. This method works well when you are measuring a baseband noise signal.

You can also measure the internal noise of the analyzer and then use that measurement to correct the noise-signal measurements by subtracting the contribution made by the analyzer's noise from the readings. If the internal noise of the analyzer is x dB below the combined level of the noise signal and the analyzer's noise, then you can calculate the correction factor as follows:

$$T_{np} = S_{np} + A_{np}$$

$$\frac{S_{np}}{T_{np}} = 1 - \frac{A_{np}}{T_{np}}$$

In dB:

$$\frac{S_{np}}{T_{np}} \!\!=\! 10 \! * \! LOG \! \left( 1 \! - \! 10^{\frac{-x}{10}} \right)$$

where:

 $T_{np}$  = total noise power,

 $S_{np}$  = signal noise power, and

 $A_{np}$  = analyzer noise power.

For example, if the analyzer noise is 10 dB below the total noise measured, then the correction factor is -0.46 dB. If the analyzer noise floor is only 3 dB below the total noise, then the correction factor is -3 dB.

If the noise you want to measure is a baseband signal, then you can measure the internal noise of the analyzer by simply measuring the instrument's noise floor with no signal present. Make sure the same range setting is used for both measurements. If the noise you want to measure is near a large single tone, as is the case when measuring the phase or amplitude noise of a carrier, then the phase noise of the analyzer's local oscillator may also contribute to the analyzer's total internal noise.

You can measure the analyzer's total internal noise by using a source that is much "cleaner" than the analyzer's local oscillator. Set up the clean source so that it has the same frequency and amplitude as the carrier you want to measure and then use the analyzer to measure the noise at the desired offset from the carrier. The measured noise is the combination of the analyzer's phase noise and the analyzer's noise floor.

Because of their sensitivity, dynamic range, and frequency selectivity, spectrum analyzers are good candidates for making noise-power density measurements.

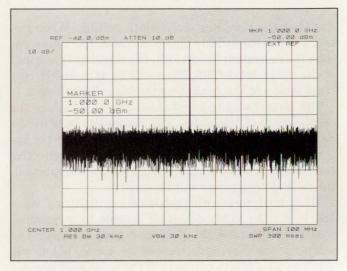


Fig 6—Rosenfell detection measures both the tone and the average noise level correctly.

However, most spectrum analyzers are not optimized for making noise measurements, so you must be careful to set up the measurement correctly and apply any needed correction factors. Spectrum analyzers with predetection digitizers have all-digital IF sections that make measuring noise-power density easier because they employ true rms detection schemes and have resolution bandwidths that you can set precisely. However, you must still configure the instruments properly if you want accurate readings.

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Author's biography

Kevin Johnson is a manufacturing development engineer at the Lake Stevens Div of Hewlett-Packard Co in Everett, WA. He holds a BS in physics from Boise State University and an MSEE from Colorado State University. In his spare time, he enjoys hiking and mountain biking.



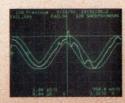
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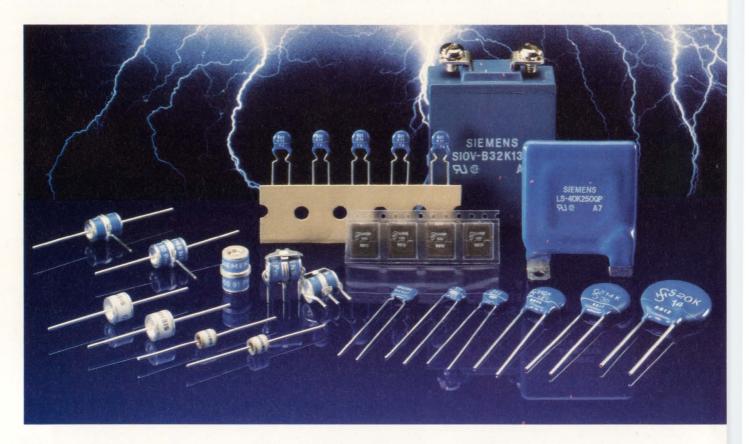


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# **EDN-DESIGN IDEAS**

**EDITED BY CHARLES H SMALL & ANNE WATSON SWAGER** 

# Tester checks capacitors on loaded pc boards

Nathan B Price and Peter J Kindleman, Congruent Design Inc, Guilford, CT

The capacitance-measuring circuit in Fig 1 can check loaded pc boards because it impresses only a 0.5V test voltage and, hence, will not turn on semiconductors. The circuit employs delta-sigma conversion, which charge-balances an unknown input current against a reference current. That is, the circuit cycles the reference current on and off so that, on average, it equals the input current.

 $C_1$  sets the clock frequency of  $IC_1$ , an LTC1043 self-clocking switch array, at 50 kHz. The upper portion of  $IC_1$  alternately charges the unknown capacitance  $C_{\rm X}$  to 0.5V and then discharges  $C_{\rm X}$  into  $IC_2$ 's summing junction (a virtual ground). The bottom half of  $IC_1$  performs a similar function with the reference capacitor,  $C_{\rm REF}$ , discharging  $C_{\rm REF}$  through electronic switch  $S_1$  into the same summing junction. Note that  $C_{\rm X}$  and  $C_{\rm REF}$  have opposite polarity with respect to ground when switched into the summing junction. If  $C_{\rm X}=C_{\rm REF}$ , the net current into the summing junction will be zero.

Integrator  $IC_2$  senses any error between  $C_{REF}$ 's and  $C_X$ 's currents.  $IC_2$ 's output, via comparator  $IC_3$  and

flip-flop  $IC_4$ , "dithers"  $S_1$ 's duty cycle to equalize the two capacitors' current flows. The value of integrating capacitor  $C_2$  does not enter into the measurement;  $C_2$  just scales  $IC_1$ 's output to keep voltage excursions within comparator  $IC_3$ 's input range. Nor does comparator  $IC_3$ 's threshold affect the measurement. Because the same reference voltage and oscillator frequency generate both  $C_X$ 's and  $C_{REF}$ 's input currents, only  $S_1$ 's duty cycle determines the unknown capacitance as a fraction of the reference capacitance.

The CLK signal is a high-speed clock (relative to  $IC_1$ 's clock) from a  $\mu P$ . The output NAND gate ANDs  $S_1$ 's variable-duty-cycle pulse with CLK. A  $\mu P$  can count the number of CLK pulses, obtaining a count that is proportional to  $S_1$ 's duty cycle. Depending on the range of unknown capacitances to be measured, you may want to have a range of switch-selectable  $C_{REF}S$ . EDN BBS /DI\_DIG #1089

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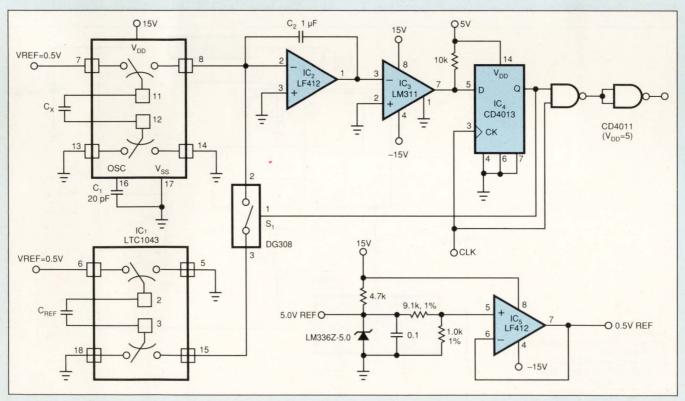


Fig 1—This charge-balancing circuit uses a 0.5V reference source to measure capacitances on loaded pc boards. The low reference voltage will not turn on semiconductors.

# AC supply lights cold-cathode fluorescents

Jim Williams, Linear Technology Corp, Milpitas, CA

Cold-cathode fluorescent lamps provide the highest-efficiency light source for applications such as backlighting LCDs. These lamps require high-voltage ac. A supply for these lamps should be very efficient and should deliver a sine-wave output to minimize RFI.

The circuit in **Fig 1** meets these requirements. Efficiency is 75% for an input-voltage range of 4.5 to 20V; if you drive the lamp from a separate low-voltage supply (eg, 5V), efficiency is about 82%. Additionally, users can vary a lamp's intensity smoothly from off to full intensity.

In operation, applying power drives the switching regulator's (IC<sub>1</sub>) feedback pin,  $V_{\rm FB}$ , below the device's internal 1.23V reference, causing full duty-cycle modulation at IC<sub>1</sub>'s  $V_{\rm SW}$  pin (trace A, Fig 2). L<sub>2</sub> conducts current (trace B, Fig 2), which flows from L<sub>1</sub>'s center tap, through the transistors, into L<sub>2</sub>. IC<sub>1</sub> conducts L<sub>2</sub>'s current to ground in switched fashion.

L<sub>1</sub> and the transistors compose a current-driven Royer converter, which oscillates at a frequency set by L<sub>1</sub>'s characteristics and the 0.02-μF capacitor. L<sub>2</sub>, as switched by  $IC_1$ , sets the magnitude of the  $Q_1/Q_2$  tail current, and hence  $L_1$ 's drive level. The 1N5818 diode maintains  $L_2$ 's current flow when  $IC_1$  is OFF.  $IC_1$ 's 40-kHz clock rate is not synchronous with the Royer converter's ( $\approx$ 60 kHz), accounting for trace B's (**Fig 2**) waveform thickening.

The 0.02- $\mu$ F capacitor combines with L<sub>1</sub>'s characteristics to produce sine-wave voltage drive at Q<sub>1</sub>'s and Q<sub>2</sub>'s collectors (traces C and D, respectively, of Fig 2). L<sub>1</sub> furnishes voltage step-up, and about 1400V p-p appears at its secondary (trace E, Fig 2). Current flows through the 33-pF capacitor into the lamp.

On negative waveform cycles,  $D_1$  steers the lamp's current to ground.  $D_2$  steers positive waveform cycles to the ground-referenced  $562\Omega/50\text{-k}\Omega\text{-potentiometer}$  chain. The positive half-sine appearing across these resistors (trace F, Fig 2) represents ½ the lamp's current. The  $10\text{-k}\Omega/1\text{-}\mu\text{F}$  pair filters this signal and presents it to IC1's feedback pin. This connection closes a control loop that regulates lamp current. The  $2\text{-}\mu\text{F}$  capacitor at IC1's Vc pin provides stable loop compensation. The loop forces IC1 to switch-mode modulate L2's

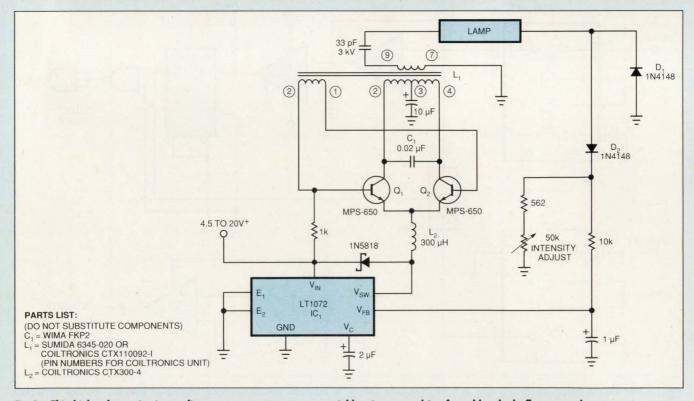
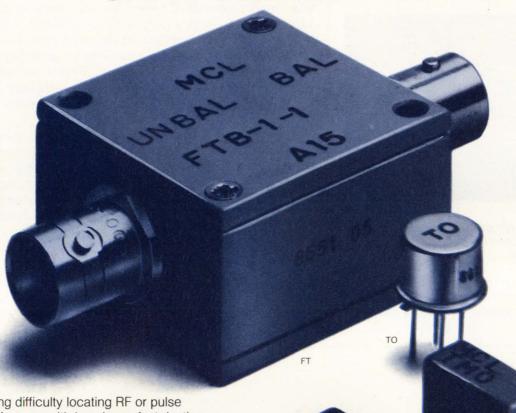


Fig 1—This high-voltage circuit supplies a constant-current, user-variable, sine-wave drive for cold-cathode fluorescent lamps.

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\*units are not QPL listed

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CIRCLE NO. 91

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#### **NSN GUIDE**

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T1-1T	5950-01-153-0668	
T2-1	5950-01-106-1218	
T3-1T	5950-01-153-0298	
T4-1	5950-01-024-7626	
T9-1	5950-01-105-8153	
T16-1	5950-01-094-7439	
TMO1-1	5950-01-178-2612	

T. TH. TT

MCL NO.	NSN
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TMO2.5-6	5950-01-215-4038
TMO2.5-6T	5950-01-215-8697
TMO3-1T	5950-01-168-7512
TMO4-1	5950-01-067-1012
TMO4-2	5950-01-091-3553
TMO4-6	5950-01-132-8102
TMO5-1T	5950-01-183-0779
TMO9-1	5950-01-141-0174
THOUGH	FOFO O4 400 4FOO

bent lead version style KK81 average current to whatever value is required to maintain a constant current in the lamp. The potentiometer varies the constant current's value, and hence the lamp's intensity. This constant-current drive allows 0-

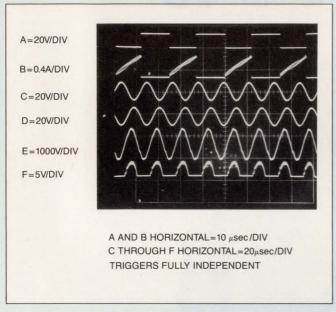


Fig 2—The circuit in Fig 1 produces a sinusoidal 1400V output (trace  $\mathbf{E}$ ).

to 100% intensity control with no lamp dead zones or "pop-on" at low intensities. In addition, lamp life is enhanced because current cannot increase as the lamp ages.

You must keep several points in mind to observe this circuit's operation safely: You can monitor  $L_1$ 's high-voltage secondary only with a wideband, high-voltage probe fully specified for this type of measurement. The vast majority of oscilloscope probes will break down and fail if you use them for this measurement. Tektronix probe type P-6009 (acceptable) or types P6013A and P6015 (preferred) are examples of probes you can use safely.

Another consideration involves observing waveforms. IC<sub>1</sub>'s switching frequency is completely asynchronous from the Royer converter's switching. As such, most oscilloscopes cannot simultaneously trigger and display all the circuit's waveforms. A dual-beam oscilloscope (Tektronix 556) produced **Fig 2**. Singlebeam oscilloscopes having alternate sweep and trigger switching (eg, Tektronix 547) will also work, but are less versatile and are restricted to four traces.

EDN BBS /DI\_DIG #1091

EDN

To Vote For This Design, Circle No. 747

# IBM PC board adapts to different buses

Vladimir Bochev, Center of Informatics and Computer Technology, Sofia, Bulgaria

The simple logic circuit in Fig 1 tells an IBM PC board whether it is plugged into an 8- or 16-bit slot. The flip-flop senses the MEMR or MEMW signals available only from the small connector in an AT backplane. These signals normally indicate a 16-bit transfer. You then use the output of the flip-flop for chores such as disabling  $A_0$  and enabling 16-bit buffers. You will also need to enable signals such as SBHE and MEMCS16 (or IOCS16). If you plug a board bearing Fig 1's circuit into an 8-bit-only slot, the flip-flop will never set and the board will function as an 8-bit board.

EDN BBS /DI\_SIG #1088

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To Vote For This Design, Circle No. 748

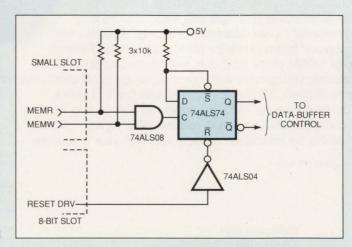


Fig 1—This simple circuit senses 16-bit transfers when plugged into an AT backplane and configures the board for 16-bit transfers. In an 8-bit-only backplane, the board functions as an 8-bit-only board.

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CIRCLE NO. 92

### Models for worldwide AC operation

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Windjammer blowers are UL component recognized, CSA and TÜV certified. Complete specifications are available from AMETEK, Lamb Electric Division, 627 Lake Street, Kent, OH 44240. Tel: 216-673-3451. Fax: 216-673-8994.

# AMETEK

EDN March 2, 1992 • 143

# **EDN-DESIGN IDEAS**

Feedback & Amplification

# **Design Entry Blank**

\$100 Cash Award for all entries selected by editors. An additional \$100 Cash Award for the winning design of each issue, determined by vote of readers. Additional \$1500 Cash Award for annual Grand Prize Design, selected among biweekly winners by vote of editors.

To: Design Ideas Editor, EDN Magazine Cahners Publishing Co 275 Washington St, Newton, MA 02158

I hereby submit my Design Ideas entry.

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Entry blank must accompany all entries.

Design entered must be submitted exclusively to EDN, must not be patented, and must have no patent pending. Design must be original with author(s), must not have been previously published (limited-distribution house organs excepted), and must have been constructed and tested. Fully annotate all circuit diagrams. Please submit software listings and all other computer-readable documentation on a 5½-in. IBM PC disk in plain ASCII.

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In submitting my entry, I agree to abide by the rules of the Design Ideas Program.

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#### **ISSUE WINNER**

The winning Design Idea for the December 5, 1991, issue is entitled "Single-chip  $\mu P$  suppresses unwanted tone," submitted by John Miller of Frontier Engineering Inc (Oklahoma City, OK).

#### **ISSUE WINNER**

The winning Design Idea for the December 19, 1991, issue is entitled "Circuit adjusts duty cycle, not frequency," submitted by Yongping Xia of Dept of Electrical and Computer Engineering, West Virginia University (Morgantown, WV).

# Readers rebut "Name Withheld"

In EDN, September 2, 1991 in the Design Ideas Feedback and Amplification section, one Name Withheld by Request (for obvious reasons) seems to be dissatisfied with your publishing fine Design Ideas from "foreigners." Mr/Ms NWR received a good and interesting reply from Charles H Small and Anne Watson Swager.

I would like to add that to the best of my knowledge, there are *very few* individuals today who can *really* claim to be "native" Americans. The *only* indigenous American must, in my opinion, be the American Indian, whom the "superior white man," with (luckily) poor result, has tried to "exterminate."

In fact, the great majority of contemporary Americans are of very diverse origins. And—besides—who said that only an "American" can come up with a good idea? As far as I have learned, a great many of the great "American" scientists were naturalized "foreigners."

The sentiments displayed by NWR are unfortunately popping up everywhere. In every country there will be some self-righteous people assuming that they are superior to all others. In these days of historical turmoil we should cooperate in exterminating ideas like that. Otherwise we might well experience another Holocaust (or Armageddon, if you like).

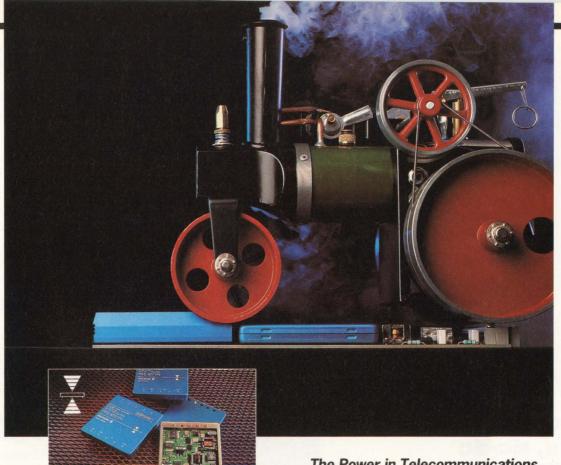
We are all fellow citizens of the world, regardless of race, color of the skin, creed, political persuasion, or whatever. Only that way may we survive—not by trying to oppress each other.

I'm happy to stand by my opinion with my name displayed. Anyway, if you daren't put your name to an opinion, is it *really* worth expressing?

Gjermund Austvik BT Systems AB Argongatan 30 S-431 53 MOLNDAL Sweden 31 86 62 70

What a strange attitude from "Name Withheld." Your reply is to be applauded. Perhaps he (I bet it *is* a he) would also like to see the ideas being restricted to those using chips and computers designed and manufactured in the USA only. That should narrow the field a hit

Alex Gray, Information Technology Mgr British Broadcasting Corp Walton Hall Milton Keynes MK7 68H, UK 0908 274033



## The Power in Telecommunications

# The squeeze is on

Slimming is an obsession in the electronics industry as engineers face the task of making thinner cards to fit even more functions into standard racks. Once again Ericsson can help.

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Having set the standard for DC/DC converters in 1983, Ericsson's new series represents a remarkable leap forward in power supply technology. The PKE needs no power derating over its entire ambient temperature range of -45 to +85 °C. Quite simply, no one else achieves this in so little space. And you can choose from versions with one, two or three regulated outputs.

Perhaps most surprisingly, performance is in no way compromised by the size reduction. In fact, the PKE is even better than the PKA. A wide input voltage of 38 to 72 VDC is complemented by 1500 VDC isolation, 80-85% typical efficiency and two million hours MTBF at +45 °C ambient.

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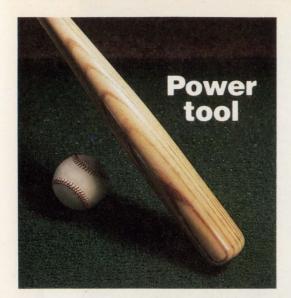
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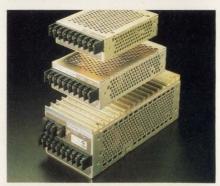
Field-proven in a broad spectrum of applications and certified by the world's safety agencies, here are versatile, rugged power tools for your design needs. Choose voltages up to 48V dc; power up to 3000W; ac or dc input. Features include active soft-start, remote voltage control, overvoltage protection, current limiting and built-in EMI filtering. The 600W and 1500W models provide for current-share paralleling. Kepco's switchers are also available in low-cost open frame and pc-card styles for OEM applications.

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- ☐ 5V-48V dc output
- ☐ 24 and 48V input (60V available on some models)
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- ☐ MIL STD 461B EMI filtering
- ☐ Tested to MIL STD 810D

**Kepco Group ERD Power Supplies** 

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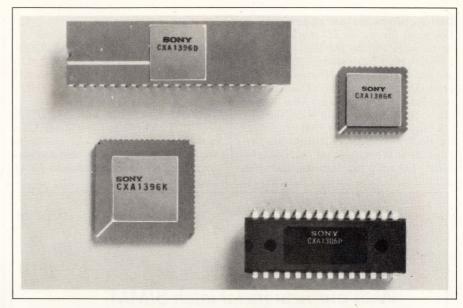
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# **Integrated Circuits**

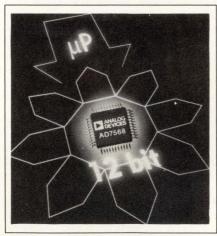
# 9-Bit Flash A/D Converters

- Conversion rates of 75 or 125 Msamples/sec
- Accept analog inputs to 150 MHz A family of four 8-bit flash A/D converters is available in speed ratings of 75 or 125 Msamples/sec with a guaranteed error rate of 10<sup>-9</sup> times per second. The converters, which can accept analog inputs to 150 MHz, are available in a range of package choices. The two 75-Msample/sec converters are the CXA1386P 28-pin plastic DIP and the CXA1386K 44-pin ceramic leadless chip carrier. The 125 Msample/sec converters are the CXA1396D 42-pin ceramic DIP and the CXA1396K 68-pin ceramic leadless chip carrier. Typical power consumption is 470 mW for the CXA1386P/K, and 870 mW for the CXA1396D/K. Fabricated in the



company's ECL-3 process, the converters operate from a -5.2V supply. Depending on speed rating and package style, from \$79 to \$175 (10).

Sony Corp of America, Component Products Co, Box 6016, Cypress, CA 90630. Phone (714) 229-4331. Circle No. 355



# Octal 12-Bit D/A Converter

- Operates from a 5V supply
- Has a serial interface

The AD7568 is an octal 12-bit D/A converter. In addition to eight fully independent 12-bit current-output DACs, the device features a serial interface and 4-quadrant multiplication. The serial interface reduces circuit-board complexity by eliminating multiconductor data buses and complex decode logic. The converter can operate from a single 5V supply while consuming 1 mW of power, extending battery life when

using the device in portable equipment. Integral nonlinearity of 0.5 LSB (max) and differential nonlinearity of 0.9 LSB (max) guarantee monotonic performance over the operating temperature range of -40 to  $+85^{\circ}$ C. Other specifications include a settling time of 500 nsec to 0.01% of full-scale range, THD of -83 dB, and channel-to-channel isolation of 76 dB. The AD7568, in die form or 44-pin quad flatpack, from \$23 (1000).

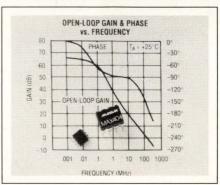
Analog Devices Inc, 181 Ballard-vale St, Wilmington, MA 01887. Phone (617) 937-1428. Circle No. 356

# Optimized Video Op Amp

- 80-MHz bandwidth
- 500V/µsec slew rate

Optimized for dynamic performance in video and other high-speed applications, the MAX404 features an 80-MHz bandwidth and a 500V/µsec slew rate. Operating from ±5V supplies, the op amp's differential gain/phase is 0.05%/0.01°. Unlike current-feedback amplifiers, which are limited to low-gain, noninverting

applications, the op amp has a symmetrical differential input that works in most high-speed applications. Open-loop gain is 66 dB and CMRR is 70 dB. As a  $75\Omega$  back-terminated coaxial-cable driver, the amplifier has a bandwidth of greater than 65 MHz, ensuring that video signals such as NTSC, PAL, or SECAM are within the op amp's slew-rate



capability. Output current is a minimum of 50 mA. The MAX404 comes in an 8-pin DIP and an SO package. From \$2.21 (1000).

Maxim Integrated Products, 120 San Gabriel Dr, Sunnyvale, CA 94086. Phone (408) 737-7600.

Circle No. 357

# **Integrated Circuits**

Data-compression coprocessor. Designed for use on PC mother boards or network cards, the 9705 data-compression chip can compress 2.5 Mbytes/sec and decompress 6 Mbytes/sec. Compression ratios average 2:1 but can extend to 18:1 on some files. Able to operate at clock speeds to 50 MHz, the 9705 can support more than 1500 concurrent full-duplex sessions in multitasking applications. When used on LAN adapter cards, the chip can increase the effec-

tive data transmission by  $18 \times$ . \$24 (50,000). Stac Electronics, 5993 Avenida Encinas, Carlsbad, CA 92008. Phone (619) 431-7474. FAX (619) 431-0880. Circle No. 358

**Ethernet LAN chip set.** The T7231 and T7213 implement a low-power LAN from the PC/XT and PC/AT bus interface to the network. The chip set supports the IEEE 802.3 standard for an

Ethernet AUI (Attachment Unit Interface) and twisted-pair wire (10Base-T) media. The T7231, which comes in a 132pin quad flatpack, integrates the LAN controller, XT/AT interface logic, memory arbitration, and bus transceivers. The T7213, which is available in 28-pin DIPs and SOJ packages, integrates the physical layer media interface and encoder/decoder. Approximately \$30/pair (10,000). AT&T Microelectronics, Dept 52AL040420, 555 Union Blvd, Allentown, PA 18103. Phone (800) 372-2447, ext 815; in Canada, (800) 553-2448, Circle No. 359 ext 815.

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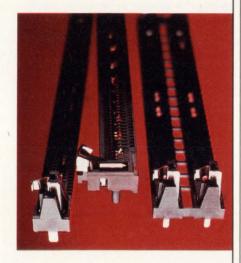
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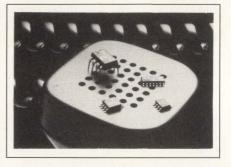


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Low-voltage serial EEPROMs. The 24LHxx serial EEPROMs operate over a range of 2 to 6V and achieve an endurance level of 1,000,000 erase/write cycles and a data-retention time of more than 40 years. The 24LCxx devices operate over a 2.5 to 5.5V range and achieve an endurance level of 100,000 erase/write cycles. In DIPs and SOICs, from \$0.58 to \$3.84 (10,000). Microchip Technology Inc, 2355 W Chandler Blvd, Chandler, AZ 85224. Phone (602) 963-7373. (Grde No. 360

**Time-base generator.** Combining two functions, the 32D4662 time-base generator supports constant-density recording and eases the design of small disk drives. The device provides a programmable reference generator having 1% resolution and multiple DACs for channel-filter and data-rate control. The 32D4662 operates from a 5V supply and comes in a 24-pin SO package. Approximately \$4 (10,000). Silicon Systems, 14351 Myford Rd, Tustin, CA 92680. Phone (714) 731-7110. FAX (714) 669-8814.

Cache RAM for 486-based systems. The CY7B173 14-nsec, 256-kbit cache RAM delivers zero-wait-state performance for 486-based systems operating at 50 MHz. Organized as  $32k \times 9$  bits, the chip also integrates decoding

# **Integrated Circuits**

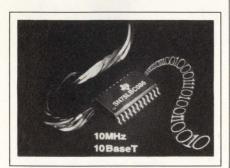
logic that simplifies expansion from one bank of four devices (128 kbytes of cache) to two banks of four devices (256 kbytes of cache) with no performance penalty. In a 44-pin plastic leaded chip carrier, \$69 (100). Cypress Semiconductor, 3901 N First St, San Jose, CA 95134. Phone (408) 943-2600.

Circle No. 362

15V step-up regulator. Operating from an input voltage range of 4 to 11V, the MAX733 provides an output of 15V at 125 mA. The regulator, which has a switching speed of 170 kHz, uses PWM current-mode control and features an efficiency of 85%. The MAX733 comes in 8-pin DIPs and 16-pin SOIC packages and is available in commercial, industrial, and military temperature grades. From \$3.23 (1000). Maxim Integrated Products, 120 San Gabriel Dr, Sunnyvale, CA 94086. Phone (408) 737-7600.

Circle No. 363

**Exclusive-OR CMOS PLD.** Using an exclusive-OR architecture, which is efficient for implementing data-path functions, the GAL20XV10B-10 CMOS PLD features a propagation delay of 10 nsec and a typical  $I_{\rm CC}$  of 75 mA. The 24-pin device can operate to 100 MHz. In 10- and 15-nsec DIPs and plastic leaded chip carriers from \$9.50 to \$19.80 (100). Lattice Semiconductor Corp, 5555 NE Moore Ct, Hillsboro, OR 97124. Phone (503) 681-0118. FAX (503) 681-3047. TLX 277338. **Circle No. 364** 



### Ethernet 10Base-T transceiver.

Compliant with the 802.3 10Base-T standard, the SN75LBC086 differential driver/receiver is designed for medium attachment units used in 10-MHz Ethernet applications. A patented squelch circuit improves on the data-path noise rejection required by the 802.3 standard, as well as providing jabber control, collision detection, and link-test functions required by the standard. Available in a 24-pin DIP, \$8.40 (1000).

**Texas Instruments Inc**, Semiconductor Group (SC-91085), Box 809066, Dallas, TX 75380. Phone (800) 336-5236, ext 700. Outside US and Canada, (214) 995-6611, ext 700. **Circle No. 365** 

Timing control unit. The CY7C325 timing control unit (TCU) eliminates the need to create complex state machines by controlling the clock signal sent to the company's CY7C601 SPARC

microprocessor ( $\mu P$ ) or CY7C611 RISC (reduced-instruction-set computer) controller. The TCU stretches the low portion of the clock sent to the  $\mu P$  until it is ready. The number of stretched cycles in the TCU is controlled by a 4-bit binary-count input generated by the address decode logic. In plastic-leaded-chip-carrier packages, \$29 (100). Cypress Semiconductor, 3901 N First St, San Jose, CA 95134. Phone (408) 943-2600. Circle No. 366



Australia (02) 654 1873, Austria (0222) 38 76 38, Benelux +31 1858-16133, Canada (514) 689-5889, Czechoslovakia 0202-2683, Denmark (42) 65 81 11, Finland 90-452 1255, France (01)-69 41 28 01, Germany 08131-25083, Great Britain 0962-73 31 40, Greece 01-862-9901, Hungary (1) 117 6576, Israel (03) 48 48 32, Italy (011) 771 00 10, Korea (02) 784 784 1, New Zealand (09) 392-464, Portugal 01-80 9518, Norway 02-649050, Singapore (065) 284-6077, Spain (93) 217 2340, Sweden 040-9224 25, Switzerland (01) 740 41 05, Taiwan (02) 7640215, Thailand (02) 281-9596, Yugoslavia 061 621066.

Our DSP development tool kit hammers the competition on performance.



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for debugging, and an EZ-LAB™ Evaluation Board that lets you test your code in real time at 12.5 MIPS.

Now, if all that's not enough to hammer the competition, we also hit them on compatibility. The ADSP-2100 family is a complete line of code-compatible fixed-point

DSP processors, so programs you develop with the EZ-KIT can be easily ported and used on your next design.

The low cost and high performance of our EZ-KIT opens the possibility of using DSP to a whole new range of applications – even yours. For more information, or to charge a kit by phone, call us at (617) 461-3771.



The EZ-KIT includes our EZ-LAB™ Evaluation Board with preprogrammed demos, and microphone and speaker jacks; software which includes an assembler; a simulator for the ADSP-2101 and ADSP-2105; a comprehensive DSP Lab Book; an Applications handbook with sample source code; and a discount coupon for our 3-day System Programming and Development workshop.



Analog Devices, One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106. Distribution, offices and applications support available worldwide

Authorized North American Distributors: Alliance Electronics 505-292-3360 • Alliae Electronics 817-595-3500 • Anthem Electronics 408-453-1200 • Bell Industries 213-826-6778 • Future Electronics 514-694-7710 • Hall-Mark Electronics 214-343-5000 • Newark Electronics 312-784-5100 • Pioneer Standard 216-587-3600 • Pioneer Technologies Group 1-800-227-1693

The code compatibility of the ADSP-2100

fixed-point DSP processors lets you

easily migrate within the family, even as

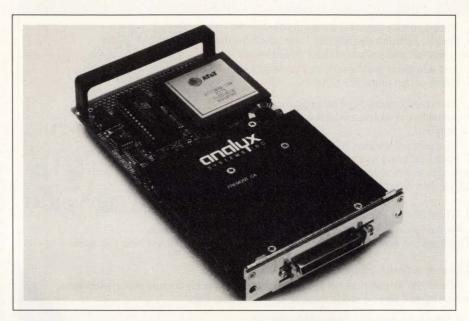
your designs get more complex

# **Test & Measurement Instruments**

# Data-Acquisition System For SBus

- Includes two 12-bit ADCs and four 18-bit DACs
- 128-kbyte dual-ported RAM

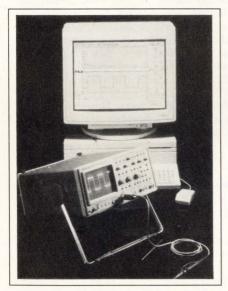
The model ADDA-1218 is an isolated data-acquisition subsystem in the diminutive SBus format of Sun Microsystems' SPARCstations. The board includes a pair of 12-bit ADCs that convert in 6 µsec; differentialinput amplifiers having softwareprogrammable gains of 1, 2, 4, and 8; a multiplexer that has 16 differential inputs; four 18-bit DACs; three TTL outputs; and a 128-kbyte dual-ported memory. The entire analog I/O section is ohmically isolated from the bus. You control A/D conversions by writing to one register. The unit then places a sequence of results into its RAM. At the same time, the board's DACs can



produce waveforms from data previously written elsewhere in RAM. Single unit, \$2495; with ADCs only, \$1995; with DACs only, \$1895.

**Analyx Systems Inc,** Box 14644, Fremont, CA 94539. Phone (510) 656-8017. FAX (510) 657-0927.

Circle No. 367



# Macintosh-Based Oscilloscope Software

- Works with IEEE-488-based scopes and digitizers
- Includes analysis and presentation package and text editor

Superscope/488 is a software package for the Macintosh that lets you control IEEE-488-based scopes and digitizers. The package also lets you—without programming—use the

Mac to store and display the acquired data, process and analyze the data, and create presentations using the raw or processed data. The package includes a text editor, which enables you, in effect, to keep your lab notebook on the Mac. Software package, \$990; instrumentation library, \$290.

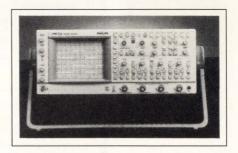
**GW Instruments,** 35 Medford St, Somerville, MA 02143. Phone (617) 625-4096. **Circle No. 368** 

# 100- And 200-MHz Analog/Digital Scopes

- Capture 200 Msamples/sec
- Waveform memory expandable to 32 ksamples

The four members of the PM 338x and PM 339x series provide two 100-and two 200-MHz-bandwidth units. All units can display four traces at once. One scope in each bandwidth category has four full-sensitivity channels with attenuators and trigger inputs. The other scopes have two full channels and two channels that you can use to view external trigger sources. The instruments

function either as analog scopes or as 200-Msample/sec DSOs. DSO memory is 8 ksamples. Expansion to 32 ksamples allows storing more than 200 512-point records. A math option allows calculations such as integration, differentiation, and FFTs. The scopes trigger on pulses



as narrow as 2 nsec and capture glitches as brief as 5 nsec, even at slow sweep speeds. \$4490 to \$6490.

John Fluke Mfg Co Inc, Box 9090, Everett, WA 98206. Phone (800) 443-5853; (206) 347-6100. FAX (206) 356-5116. Circle No. 369 Philips Test and Measurement, Bldg TQIII-4, 5600MD, Eindhoven, The Netherlands. Phone local office. Circle No. 370

# Clear Out Excess Inventory!

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Thousands of students and teachers in A: local school systems, as well as community, technical and four-year colleges need metal, electric, electronic parts and supplies for training

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CIRCLE NO. 98

# RTXC & RTXC/MP

Written in C, portable by design	Intel 80x86, 80x96, 8051 Motorola 68HC11/16, 68xxx TI TMS320C30/C40 Zilog Z80, Zx80 Analog Devices 2101 Inmos T2xx, T4xx, T8xx		
Dynamic priorities Task Management Timer Management Memory Management Semaphores Message mailboxes FIFO queues Resource Management	From 8-bit microcontrollers to multiple 32-bit processors : same API !		
Virtual single processor with RTXC/MP!	(distributed) Debugger System generation tool Workload monitor		
Transputer networks C40 networks VME networks	Message based Transparent Distributed operation!		
Free demo and evaluation kit New version 3.0	No royalties Source code included 3 months free upgrades and support		

Intelligent Systems International Interleuvenlaan 23, B-3001 Leuven, Belgium Tel.(+32)16 29 01 28. Fax.(+32)16 29 03 63

(List of distributors for USA and Japan on request)

# **EDN-NEW PRODUCTS**

**Test & Measurement Instruments** 



Test system for telecommunications pc boards. The 3079CT tester is optimized for testing items produced in large quantity, such as ISDN (Integrated Services Digital Network) line cards. When compared with earlier testers, the system's design and serialtest language reduce the number of lines of code for testing complex telecommunications boards by more than two orders of magnitude. From \$220,000. Hewlett-Packard Co, 19310 Pruneridge Ave, Cupertino, CA 95014. Phone (800) 752-0900. Circle No. 371

**Enhancement modules for digital** scopes. Working with the vendor's 54600 series of 100-MHz DSOs, the 54655A and 54656A modules provide semiautomatic mask-template testing; the 54657A and 54658A store as many as 100 waveforms. You communicate with the 54656A and 54658A via an RS-232C port; with the others, you use IEEE-488. All units except 54656A, \$750; 54656A, \$800. Hewlett-Packard Co, 19310 Pruneridge Ave, Cupertino, CA 95014. Phone (800) 752-0900.

Circle No. 372

Programmable antialiasing filters. Filter 488 is a 4- or 8-channel differential-input unit that you can control via the IEEE-488 bus or an RS-232C port. You can select 8-pole Bessel, Butterworth, Chebychev, or elliptic response, and you can set the cutoff frequency from 0.05 Hz to 50 kHz in increments as small as 0.002 Hz. You can also program the unit's gain to ×1,  $\times$  10, or  $\times$  100. 4-channel unit, \$1995; 8-channel unit, \$2995. IOtech Inc, 25971 Cannon Rd, Cleveland, OH 44146. Phone (216) 439-4091. FAX (216) 439-4093. Circle No. 373

Test and debug adapters for 68EC000. These adapters provide interfaces between 68EC000 µPs and test instruments. Adapt-A-Pods let you attach 68000 emulator pods to plastic-

**Test & Measurement Instruments** 

leaded-chip-carrier (PLCC) devices. The adapters attach to ICs soldered to pc boards. Bug Katchers, which fit between PLCCs and target boards, accept leads from scopes and logic analyzers. Passive preprocessors let you use Hewlett-Packard logic analyzers more conveniently with the 68EC000. Adapters, from \$185; preprocessors, \$1500. Emulation Technology Inc, 2344 Walsh Ave, Bldg F, Santa Clara, CA 95051. Phone (408) 982-0660. FAX (408) 982-0664. TLX 981866. Circle No. 374

**Development tools for V series** μ**Ps.** These tools, which support NEC's V25, V25+, V33, V35+, V40, V50, V53, and V70, provide nonintrusive emulation, bus analysis, symbolic debugging, and code-coverage testing. \$13,493 to \$23,391. **Hewlett-Packard Co**, 19310 Pruneridge Ave, Cupertino, CA 95014. Phone (800) 752-0900. **Circle No. 375** 



**16-channel digital recorder.** The Datagraf II acquires a total of 80 ksamples/sec with 12-bit resolution. It is compatible with 45 types of signal conditioners. The unit can perform a range of mathematical operations on acquired data. From \$12,995. **Gould Inc,** 8333 Rockside Rd, Valley View, OH 44125. Phone (216) 328-7000. **Circle No. 376** 

System with pretrigger recording and FIFO storage. You can add a pretrigger card to the Presys 1000 15-bit, 1-Msample/sec A/D conversion system. The card works with the system's FIFO memory to provide a picture of data taken prior to a critical event. \$3500. Preston Scientific, 805 E Cerritos Ave, Anaheim, CA 92805. Phone (714) 776-6400. Circle No. 377

**Data-smoothing software.** Data Smoother V2.0 for MS-DOS PCs works with equally spaced data points. You can enter data from the keyboard or read it from files on disk. You can view and print the data in numeric or graphi-

cal form before and after smoothing. The size of data sets is limited only by the memory available. \$49.95. **Dynacomp Inc**, 178 Phillips Rd, Webster, NY 14580. Phone (716) 671-6160.

Circle No. 378

1-GHz capture system for logic analyzer. The Paladin capture system works with the vendor's ML4400 analyzers. In its basic mode, the system captures 100 channels at 100 MHz or 50 channels at 200 MHz, either synchronously or asynchronously. In the split mode, the system provides 80 synchronous and 20 asynchronous 100-MHz channels. In the high-speed mode, the unit provides 10 1-GHz or 20 500-MHz asynchronous channels. \$13,950 with 100 probes. American Arium, 14281 Chambers Rd, Tustin, CA 92680. Phone (714) 731-1661. FAX (714) 731-6344.

Circle No. 379

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# I Trust My Job to Sola



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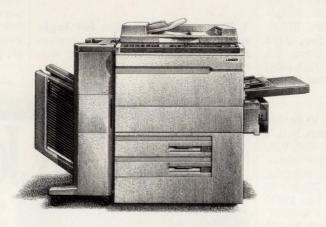
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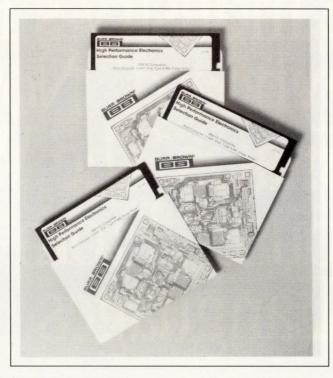
#### **CAE & Software Development Tools**

#### Parts-Selection Aid With Spice Models

- Disk with component models, cross references
- Helps in selecting Burr-Brown linear products

The High Performance Selection Guide helps designers find the right Burr-Brown linear components for their designs. The guide comes on an IBM PC-compatible disk; it contains more than 1000 component models, an industry cross-reference section, sales-office listings, applications literature, and price and ordering information. This update of the guide contains more than 70 Spice models of the supplier's op amps,

difference amps, and instrumentation amps. You can specify as many as 30 parameters when searching



for a part. You can also search for parts without knowing a complete part number; type in a partial number, and the search program will do the rest. New features include editing search parameters so that you do not have to reenter them for every search. The disk lets you access 11 product categories: analog circuit functions, analog-to-digital converters, digital-to-analog converters, dc/dc converters, instrumentation amplifiers, isolation amplifiers, multipliers, operational amplifiers, references, sample/hold amplifiers, and voltage-tofrequency converters. Free.

**Burr-Brown Corp**, Box 11400, Tucson, AZ 85734. Phone (800) 548-6132; (602)

746-1111. FAX (602) 889-1510. BBS (602) 741-3978 300/1200/2400 8,N,1. Circle No. 380

#### Mouse Cursor Software

- Improves visibility of mouse cursor
- Designed for LCD screens

Version 8.1 of Microsoft's Mouse and Ballpoint mouse software has enhancements for LCD screens and lets you customize the size and color of on-screen mouse pointers. The software improves the visibility of cursors on screens of portable computers. You can choose from among three cursor sizes and three colors (normal, reverse, and transparent) in both MS-DOS and Windows. You can also make the cursor more visible by opting to increase its size automatically during movement. You specify how fast the cursor must be moving for the enlarged cursor to appear and how soon after movement ends for the cursor to return to normal size. After installation, the software automatically loads previously specified pointer

settings when you begin your next Windows session. The software is available under different terms for users of the Microsoft Mouse and the Microsoft Ballpoint Mouse. It is sent free of charge to registered Ballpoint licensees; users of Mouse and nonregistered users of Ballpoint can receive a copy by calling Microsoft. For Mouse users with versions earlier than 8.0, \$25; free to other users.

Microsoft Corp, 1 Microsoft Way, Redmond, WA 98052. Phone (800) 426-9400; (206) 882-8080. FAX (206) 883-8101. Circle No. 381

#### Printed-Circuit Design Software

- Features metric/English translation
- Offers photo plotting and sub-mil resolution plotting

Version 1.2 of Premier PCB provides enhancements to a package

that includes schematic capture and interactive and automatic pc-board layout. Features include the ability to translate output files from English to metric and from metric to English via the Gerber laser photoplot option. You can also plot from databases that use units smaller than one mil. The software lets you translate the Premier schematic binary netlist into an ASCII format compatible with Spice circuit simulators. An EDIF (electronic design interchange format) netlist writer option lets you generate an EDIF version 2 0 0 netlist file from a Premier schematic database; with an EDIF netlist reader option, you can convert a netlist to a Premier database. The product is free to customers covered by product maintenance and warranty.

Cadam Inc, 1935 N Buena Vista St, Burbank, CA 91504. Phone (818) 841-9470. Circle No. 382

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The keyboards that *Personal Computing* called "the industry's best" are now available for your OEM Systems, just as they are for IBM. And that includes our new series of keyboards with integrated pointing devices that put all keyboard and mouse functions in a standard layout. These affordable new keyboards are available in 23 languages and can be easily customized to match your system. Give your system a competitive edge worldwide with a world-class keyboard. Call (33) 38 83 4308 in Europe or (606) 232-6814 in the U.S.A. You'll find we speak your language.



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#### **EDN-NEW PRODUCTS**

#### **Computers & Peripherals**

#### 25-MHz i486SX Computer

- Has 4 Mbytes of RAM and 80-Mbyte hard-disk drive
- 128-kbyte cache RAM is organized as 2-way set-associative unit The ME486-SX/25 25-MHz i486SX computer has 4 Mbytes of RAM, a 128-kbyte cache RAM, and an 80-Mbyte hard-disk drive. It also has both a 51/4-in. and a 31/2-in. floppydisk drive. The desktop unit runs DOS 5.0 and has an extended VGA color card and monitor. You can expand the system RAM to 32 Mbytes on the mother board using 70-nsec SIMMs (single in-line memory modules). The 128-kbyte cache RAM, which is expandable to 256 kbytes, uses 25-nsec RAMs and is organized as a 2-way set-associative unit. The computer uses selectable shadows for system and video functions. The mother board has eight 16-bit expansion slots. The extended VGA



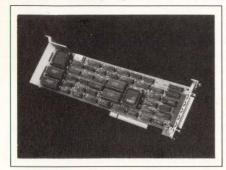
card displays 256 colors having a resolution of  $1024 \times 768$  pixels. The 14-in. monitor has a dot pitch of 0.28 mm. \$1999.

**Micro Express,** 1801 Carnegie Ave, Santa Ana, CA 92705. Phone (800) 989-9900; (714) 852-1400. FAX (714) 852-1225. **Circle No. 351** 

#### Micro Channel Architecture Board

- Communicates at 38.4 kbaud on 16 channels
- Features surge protection on all channels

The ACL MC16 is a serial communications board for the Micro Channel Architecture bus. The 16-bit board communicates at 38.4 kbaud on 16 serial ports simultaneously. You can also program the board



for a 115.2-kbaud rate. The board runs with Unix, Citrix Multiuser, OS/2, and DOS operating systems. It uses a 16-MHz μP and communications chips having on-chip FIFO buffers. Each channel has surge protection to suppress excessive voltage transients on the line. \$1695.

**Star Gate**, 29300 Aurora Rd, Solon, OH 44139. Phone (800) 782-7428; (216) 349-1860. FAX (216) 349-2056. **Circle No. 352** 

#### 80386 controller module

- Features expandable RAM
- Suitable for network, measurement, industrial PCs

The PX1212 33-MHz PCXI controller module has a single-board computer enclosed in a metal chassis for EMI shielding and cooling. It provides two serial ports, one parallel port, a keyboard connector, and an optional hard- and floppy-disk drive. The RAM is expandable to 32 Mbytes, and the unit runs MSDOS, Unix, OS/2, and Windows 3.0 software. \$2995.

**Rapid Systems Inc,** 433 N 34th St, Seattle, WA 98103. Phone (206) 547-8311. **Circle No. 353** 

#### Pocket-Sized 2400-BPS Modem

- For use with laptop and notebook computers
- Communicates full duplex over dial-up or 2-wire phone lines

The Viva 2400 Pocket is a portable modem for DOS-compatible laptop and notebook computers. It measures  $4.75 \times 2.375 \times 1$  in. and weighs 6.5 oz. The unit communicates in full-duplex mode over a dial-up or 2-wire leased phone line. The unit automatically dials a call, answers incoming calls from a remote system, redials a busy number, and dials an originate-only modem. The unit operates with Smartcom II version 2.1, Symphony, Wordstar 2000, PC Talk, Mite, Crosstalk, or Sidekick communications software packages. Four LEDs indicate the modem's status. You can turn off its 9V battery to conserve power. \$139.

Computer Peripherals Inc, 667 Rancho Conejo Blvd, Newbury Park, CA 91320. Phone (800) 854-7600; (805) 499-5751. FAX (805) 498-8848. Circle No. 354

## The new Tektronix 224 is as powerful as they come. And goes!



With this new 60 MHz digital oscilloscope, Tektronix takes handheld performance to an even higher plane! The 224 packs more power per pound than any other product and — with its on-board rechargeable batteries — goes wherever duty calls.

With its exclusive IsolatedChannel™ architecture, you can make two-channel floating measurements without the risk of shock or damage to delicate electronics. Such standards as Tek's sharp, bright CRT, rapid update rate and wide viewing angle make measuring fast and efficient. And the 224's familiar front panel and fully automated features keep it simple.

You get advanced capabilities like video line triggering and 10 MS/s digitizing per channel for excellent single-shot performance, plus time-correlated single-shot waveforms for easy comparison. With CAT200 software you can even control the 224 over phone lines from halfway round the world.

**Call 1-800-426-2200 Ext. 83 to get the full story.** We'll show you more of the 224 — and ways it's giving bench performance wings!

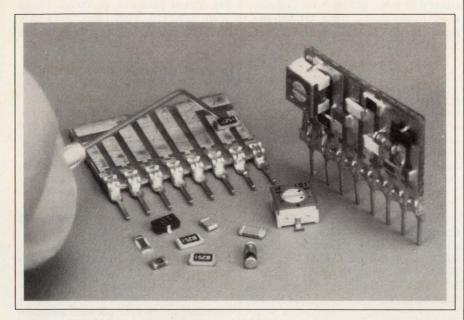
**Tektronix** 

Test and Measurement

CIRCLE NO. 103

#### **EDN-NEW PRODUCTS**

**Components & Power Supplies** 



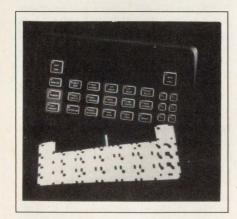
#### Universal SMD Breadboards

- Have universal designs
- Feature pre-installed SIP pins
  Surfboards allow designers to prototype surface-mount circuit designs easily. The boards accommodate a variety of component sizes
  and shapes on solder-coated copper
  foils that have multiple componentpositioning options. Foil trace designs do not conform to any indus-

try standard-part footprint or

conductor spacings, so the boards are truly universal designs. The boards feature pre-installed SIP pins that interface with other surface-mount and through-hole circuits. Sample assortment kit containing two each of the line's 60 circuit models, \$99.

Capital Advanced Technologies Inc, 309-A Village Dr, Carol Stream, IL 60188. Phone (708) 690-1696. Circle No. 383



#### **Electroluminescent Lamps**

- Have a 3000-hour lifetime
  Measure only 0.01 in. thick
- Durel 3 electroluminescent lamps measure from 0.008 to 0.01 in. thick. Time to half bright-ness (without the use of a compensating

inverter) measures as high as 3000 hours. The units are available in three standard versions: low-voltage models for battery powered applications; standard lamps for general automotive and commercial backlighting usage; and low-frequency versions for sign applications powered from 120V ac. The lamps are available in standard colors of green, blue-green, white, and orange-yellow. In ac applications, the lamps draw 1 mA/in.2 and have a 0.025W/in.2 power consumption. From \$0.30 to \$2/in<sup>2</sup>. Delivery, four to six weeks after approval date of

**Durel Corp**, 645 W 24th St, Tempe, AZ 85282. Phone (602) 731-6200. **Circle No. 384** 

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#### **Tektronix**

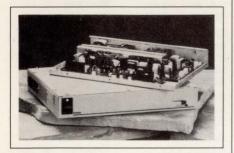
Test and Measurement

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Power modules. UVS Plus Series units provide both voltage-regulation and line-conditioning service. They are available in three models rated at 1000, 1250, and 1500 VA. The modules hold the output within 3% of specified value and also provide brownout protection down to 88V ac. During an extended power interruption, the components' interactive computer interface provides a signal 1.5 cycles after utility loss. This allows a soft landing for the system. You can configure the modules to act as V/F converters or as ac/dc converters. The modules have a ride-through capability of several cycles. The units come in open-frame (R) and closedframe (L) versions. \$1090 to \$1790. Falcon Electric Inc, 320 W Clary Ave, San Gabriel, CA 91776. Phone (818) 287-6116. FAX (818) 285-0102. Circle No. 386

**Chokes.** Series 90 axial-lead chokes cover the 0.1 to 1000 μH inductance range. Standard tolerance equals 10%, but 3 and 5% parts are available. The chokes are EIA color-coded and are available bulk packed, in conventional tape-and-reel, or in ammo packs. \$0.11 (10,000). **Coilcraft**, 1102 Silver Lake Rd, Cary, IL 60013. Phone (708) 639-6400. **Circle No. 387** 

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Hybrid connector. The Optilec connector contains two optical fibers and as many as six electrical contacts. It accepts 200/230- and 200/250-µm allglass-fiber sizes as well as 250-, 500-, and 1000-µm plastic-fiber sizes. The device features size 22 electrical contacts. It mates with a simple squeeze-pushclick action. Optical insertion loss for a 200/230-µm glass fiber is 2 dB max. Connector with two fiber-optic terminals and six electrical contacts, \$5 (OEM qty). Aurora Optics Inc, Bldg 17-408, 1777 Sentry Pkwy W, Blue Bell, PA 19422. Phone (215) 646-0690. FAX (215) 646-4721. Circle No. 389

Programmable controllers. The PYZ4 and PYW4  $\mu$ P-based temperature/process controllers feature a  $\pm 0.5\%$  accuracy. The PYZ4 is a single-display model and the PYW4 features a dual display. The controllers accept J, K, R, B, S, T, E, and N thermocouples, PT100 RTDs, and 4- to 20-mA, or 1 to 5V inputs. Each unit provides a variety of output choices—relay, 24V dc (pulsed) for an SSR (solid-state relay), and 4 to 20 mA. \$200. Total Temperature Instrumentation Inc, Box 1073, Williston, VT 05495. Phone (802) 863-0085. FAX (802) 863-1193.

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DC/DC converters. The MP7008 and MP7101 dc/dc converters accept 4.5 to 35V inputs. The 7008 outputs 3.3V at 1A, can be TTL-controlled, and has an 80% efficiency. The MP7101 also outputs 1A and features thermal shutdown and current-limiting protection. \$17 (100). Modupower Inc, 1400 Coleman Ave, H-18, Santa Clara, CA 95050. Phone (408) 496-5796. FAX (408) 496-0204. Circle No. 391

**Crimp-style connectors.** Type ZL wire-to-wire crimp-style connectors are rated for 10A. They are available in 2-, 4-, 8-, 12-, or 16-position versions and have a 5-mm contact pitch. Standard contacts are tin-plated brass. (Phosphor-bronze is optional). The housings are rated for UL 94V-0. Mated pair, from \$0.10 to \$0.30 (OEM qty). **JST** 

Corp, 1200 Business Center Dr, Suite 400, Mount Prospect, IL 60056. Phone (800) 947-1110; (708) 803-3300. FAX (708) 803-4918. Circle No. 392

**Coaxial adapter.** The PE9266 is an MHV-male to MHV-female right-angle adapter. It has a brass nickel-plated body and utilizes PTFE insulation. The unit provides a silver-plated contact and has an operating range of -65 to  $+165^{\circ}$ C. Maximum voltage and current ratings are 5000V and 5A, respectively. \$29.95. **Pasternack Enterprises**, Box 16759, Irvine, CA 92713. Phone (714) 261-1920. FAX (714) 261-7451.

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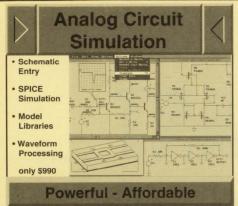
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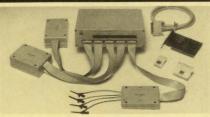


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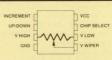
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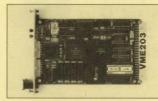
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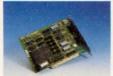
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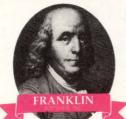
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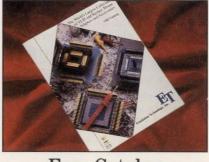


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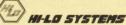
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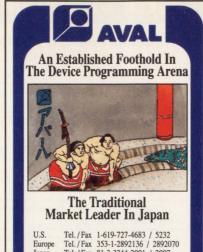
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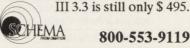
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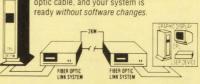
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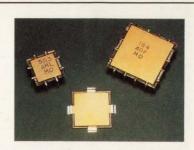
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Issue	Issue Date	Ad Deadline	Editorial Emphasis
News Edition	Mar. 19	Mar. 5	DSP Software • Communications • Regional Profile: New York, New Jersey, Pennsylvania
Magazine Edition	Mar. 30	Mar. 5	Microprocessors • Analog Circuits • CAE • Test & Measurement
SOFTWARE ISSUE	Mar. 30	Mar. 5	SOFTWARE ENGINEERING SPECIAL ISSUE • (To be polybagged with the March 30th Magazine Edition issue)
News Edition	Apr. 2	Mar. 19	ICs & Semiconductors • Multimedia Software/Development Tools • Engineering Management Special Series
Magazine Edition	Apr. 9	Mar. 19	CAE • EDN Hands-on Special Project—Part I: Field-programmable Gate Arrays • Software • Memory Technology
Magazine Edition	Apr. 23	Apr. 2	Portable Computer Design • EDN Hands-on Special Project—Part II: Field-programmable Gate Arrays • Electromechanical Devices • Computer Peripherals
News Edition	Apr. 30	Apr. 16	ASICs SPECIAL ISSUE • FPGAs and EPLDs • CICC Hot Products • ASICs • Regional Profile: Northern California
Magazine Edition	May 7	Apr. 16	Communications/Networks • Test & Measurement • Surface-Mount Components • Power Sources • Electro Show & Products Issue
ELECTRO SHOWGUIDE & PRODUCT SPOTLIGHT		Apr. 3	A free page available to all advertisers running a full page in 2 out of 3 Electro issues
News Edition	May 14	Apr. 30	Graphics Technology • Computers & Peripherals
Magazine Edition	May 21	Apr. 30	Analog ICs • Analog CAE • PC Board CAE Tools • Programmable-Logic Devices
News Edition	May 28	May 14	Communication ICs • CAE Software • Regional Profile: Texas, Oklahoma, Kansas
Magazine Edition	June 4	May 14	ASICs/PLDs • DSP Software • CAE/Software/Interoperability • Digital ICs & Semiconductors
News Edition	June 8	May 21	CAE SPECIAL ISSUE • EDA/CASE Supplement • DAC Hot Products • Software Engineering • Diversity Special Series
Magazine Edition	June 18	May 28	Microprocessors • Electromechanical Devices • ICs & Semiconductors
SOFTWARE ISSUE	June 18	May 28	SOFTWARE ENGINEERING SPECIAL ISSUE (To be polybagged with the June 18th Magazine Edition issue)
News Edition	June 25	June 11	MILITARY ELECTRONICS SPECIAL ISSUE • DSP Hardware • Military Electronics • Regional Profile: Florida, Alabama
Magazine Edition	July 6	June 11	INTERNATIONAL PRODUCT SHOWCASE—Vol. I • Hardware & Interconnect • Software • ICs & Semiconductors • Power Sources
Magazine Edition	July 20	June 25	INTERNATIONAL PRODUCT SHOWCASE—Vol. II • Computers & Peripherals • Components • CAE • Test & Measurement
News Edition	July 23	July 9	Engineering PCs & Workstations • CAE Software • SIGGRAPH Hot Products • Graphics Technology • Engineering Management Special Series • Regional Profile: Arizona, New Mexico
Magazine Edition	Aug. 6	July 16	Microprocessor Development Tools • ICs & Semiconductors • Technical Article Database Index • EDN's "Innovation Crusade"—Finalists Coverage • Reader Vote Contest: All advertisers in the issue qualify
News Edition	Aug. 13	July 30	DSP ICs • EDN's "Innovation Crusade"—Finalists Coverage • Telecom Software • Engineering Management Special Series
Magazine Edition	Aug. 20	July 30	MILITARY ELECTRONICS SPECIAL ISSUE • Military Computers Design • Test & Measurement • Memory Technology • Components
News Edition	Aug. 27	Aug. 13	Embedded Software • Software • Regional Profile: Washington DC, Maryland, Virginia
Magazine Edition	Sept. 3	Aug. 13	ASICs SPECIAL ISSUE • CAE Tools & Techniques • Computer Peripherals • Computer Buses • Sensors & Transducers • Buscon Show Coverage
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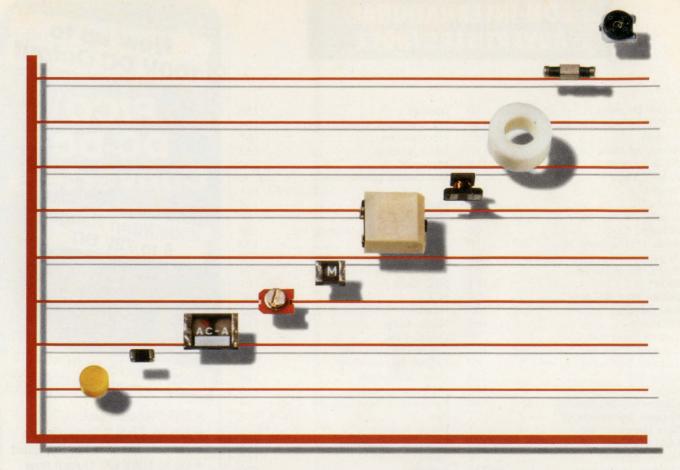
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## EDN-ACRONYMS & ABBREVIATIONS

ADC—analog-to-digital converter ANSI—American National Standards Institute

ASIC—application-specific integrated circuit

BBS—bulletin-board system; a computerized database and communications forum accessible by modem BW—bandwidth

CAE—computer-aided engineering CDDI—Copper Distributed Data Interface

CISC—complex-instruction-set computer

CMOS—complementary metal-oxide semiconductor

CPU—central processing unit

DIW—internal voice-grade wiring DMM—digital multimeter

DSO—digital storage oscilloscope

DSP—digital signal processing E-beam—electron beam

ECL—emitter-coupled logic

EDA—electronic design automation

EE—electrical engineer

EISA—Extended Industry Standard Architecture

 $\begin{array}{ll} EMI-electromagnetic interference \\ f_N-a & sampled-data & system's \\ Nyquist & frequency-half & the sampling & rate \\ \end{array}$ 

FCC—Federal Communications Commission

FDDI—fiber distributed data interface; a standard that defines a 100-Mbps fiber-optic interface for computer networks

FET—field-effect transistor

FIB-focused ion beam

GaAs—gallium arsenide; a substrate used as an alternative to silicon in semiconductor manufacturing I/O—input-output

 $I_{\rm DDQ}$  —the quiescent value of a MOS IC's drain current,  $I_{\rm DD}$ 

IC s drain current, I<sub>DD</sub>

IEEE-1149.1—the Institute of Electrical and Electronics Engineers' standard for boundary-scan testing

IF—intermediate frequency

JEDEC—Joint Electron Device Engineering Council

LAN—local-area network

LFM—linear feet/minute; a dimension for the air-flow flux rate. Multiply the flux rate by a suitable cross-sectional area to obtain the air flow in cubic ft/minute.

MAC—Media Access Control

MDA—manufacturing-defects analyzer

MIC—Media Interface Connector MOS—metal-oxide semiconductor MOSFET—metal-oxide-semiconductor field-effect transistor

MS-DOS—Microsoft Disk Operating System

NRZI—non-return-to-zero-in-verted

OEM—original equipment manufacturer

PC—personal computer pc—printed circuit

PECL—positive emitter-coupled logic; ECL referenced to +5V rather than ground

PHY—Physical Layer

PLD—programmable logic device

PLL—phase-locked loop

PMD—Physical Medium Dependent

RAM—random-access memory RFI—radio-frequency interference RISC—reduced-instruction-set computer

rms-root mean square

SONET—synchronous optical network; a telecommunications standard for a network that will replace the T1 standard

Spice—simulation program with integrated-circuit emphasis; a public-domain analog-circuit simulation program developed at UC Berkeley SRAM—static random-access

SSI—small-scale integration; relatively simple integration, for example, including basic logic gates

STP—shielded twisted pair T&M—test and measurement

TIA—time-interval analyzer
TTL—transistor-transistor logic

UDF—Unshielded Twisted Pair Development Forum

UTP—unshielded twisted pair

VCO—voltage-controlled oscillator VGA—the IBM Video Graphics Array display standard for personal computers

VLSI—very-large-scale integration; complex integration such as that found in a microprocessor

This list includes acronyms and abbreviations found in EDN's Special Report, Technology Updates, and feature articles.



#### **EDN-HANDS ON!**

#### Product reviews from EDN's editors and readers

#### How America shaped, and was shaped by, electricity

In Electrifying America: Social Meanings of a New Technology, David E Nye relates the history of electricity in America not by describing the works of great inventors or following the paths of captains of industry. Instead, Nye shows us the electrification of America through the eyes of the average Joe: farmers, housewives, factory workers, city dwellers, and school children. He describes how electricity seeped into and redefined American culture.

The author presents electrification not as an external force but as an internal process shaped by the choices people made. People chose not to live in cities with collective electrical services but to live in suburban homes with individual appliances. They preferred the automobile to the electric trolley, alternating to direct current, Edison lamps to Brush arc lights, and metered to unmetered service.

Electrification took half a century and began with three separate electrical systems. The first was private and served downtown businesses and only the most wealthy homes. The second was a municipal system for lighting city streets. The third system was the private system that powered the streetcars. The highest demand on this system was during the day when workers commuted to and from work and city dwellers traveled about doing errands. To balance the electrical load, streetcar power companies built amusement parks at the end of their lines and began selling electricity to communities along their routes.

Using myriad details from archival sources, Nye describes the creation and evolution of the streetcar suburb, the amusement park, the "Great White Way," the assembly line, the electrified home, and the industrialized farm. He also covers

the beginnings of the electrical-engineering profession and the IEEE and the science of home economics.

Contrary to people's expectations, electricity didn't always live up to its promise to make life easier. Three studies done in the 1920s found that women spent between 51 and 64 hours a week doing housework; studies made two generations later showed that housewives still work the same amount or more. Nowadays, of course, women and men split household tasks 50/50.

The book has more than 80 photographs and illustrations showing pictures of young women holding and gazing at light bulbs as if they were Fabergé eggs, 2000 flat irons taken in exchange for electric flat irons, lighting exhibits at World Fairs, and Coney Island circa 1919.

An ad for the Sears electric belt—which the retailer claimed would tone up the system, drive out disease, fortify the body against cold and sickness, and cure the "peculiar diseases" of men—is an example of early electrical medicine and people's faith in what they considered to be a magical fluid.

The author tends to make the same point two and three times in a chapter and isn't the most electrifying writer. But he does present the information clearly, and I learned something new on every page.—Julie Anne Schofield

Electrifying America: Social Meanings of a New Technology, 1880 to 1940, by David E Nye, The MIT Press, Cambridge, MA, 1990. \$29.95. ISBN 0-262-14048-9.

## Inexpensive fold-out cards put programming data at your fingertips listings. The card also furnishes information on CONFIG.SYS files and on the MS-DOS Debug commands, although I doubt that many

or programming information in a convenient format, take a close look at the fold-out cards from SSC Inc. The company offers handy cards that cover C, C++, MS-DOS, RS-232C, Unix, Fortran, and other languages and topics. The cards cost \$3 to \$4.50 each. The company also sells pocket reference booklets about languages and programming topics, as well as reference books and cassette courses. I bought several of the  $3\frac{1}{2} \times 8\frac{1}{2}$ -in. cards covering C, RS-232C, and MS-DOS 5.0. Each card—printed on sturdy cover-stock paper—folds open into a sheet of panels.

Typical of the cards is the one on MS-DOS 5.0. Even though I routinely use only a few MS-DOS commands, I've found the 20-panel reference card helpful for deciphering complex batch files and program listings. The card also furnishes information on CONFIG.SYS files and on the MS-DOS Debug commands, although I doubt that many people still use Debug. Likewise, the 8-panel ANSI C card provides a lot of helpful information. It saves me from searching through references when I use things such as enumerated data types or unions.

Some time ago, when I was setting up RS-232C ports, testing communication software and modems, and working with ASCII communications, the RS-232C card (eight panels) would have saved me a great deal of time. The card supplies lists of all RS-232C signals, pin designations for 25- and 9-pin connectors, definitions of terms, cable hookups, and handshaking information. For handy and useful information, I recommend these cards highly.—Jon Titus

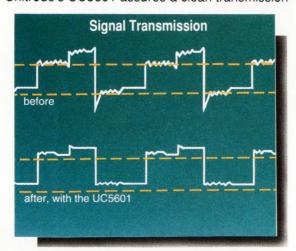
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