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your own part Directory entries pg 104 pg 108

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

Special Report: Achieve blazing data transit with FDDI pg 88

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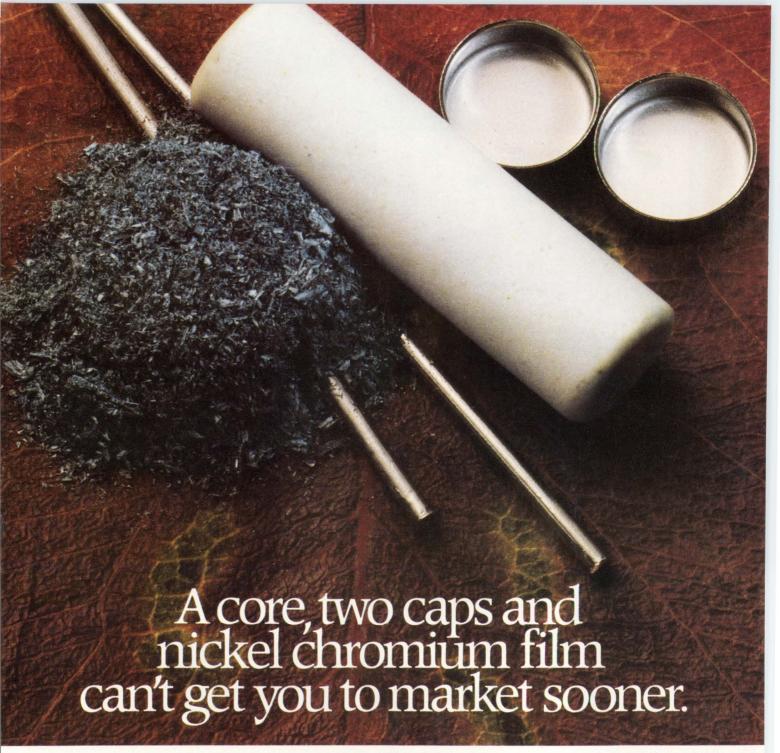
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October 1, 1991

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS



On the cover: Light traveling along fiber-optic highways lets FDDI (Fiber Distributed Data Interface) LANs transmit data at 100 Mbps. See our Special Report on pg 88. (Photo courtesy Interphase Corp)

SPECIAL REPORT

FDDI stations

88

Increasing network demands are straining the throughput of first-generation LANs. To meet high-performance requirements, network designers are starting to adopt the 100-Mbps Fiber Distributed Data Interface (FDDI). Unfortunately, FDDI stations don't come cheap.—John Gallant, Associate Editor

DESIGN FEATURE

EDN's DSP-chip directory

104

The tools needed to develop applications that use digital signal processing (DSP) continue to improve. Now, a choice of operating systems and interfaces to host operating systems is making DSP available to more applications.—David Shear, Contributing Editor

TECHNOLOGY UPDATES

SCPI instruments will ease ATE development 39

Engineers who want to minimize test-system development time and maximize system flexibility should use SCPI instruments whenever possible.—Maury Wright, Regional Editor

Serial EEPROMs: Serial memory offers cheap frills

57

You don't need a byte-wide interface or large devices to add a little nonvolatile memory to your system. Serial EEPROMs are an inexpensive option that offer a few extras.

-Richard A Quinnell, Regional Editor

Continued on page 7

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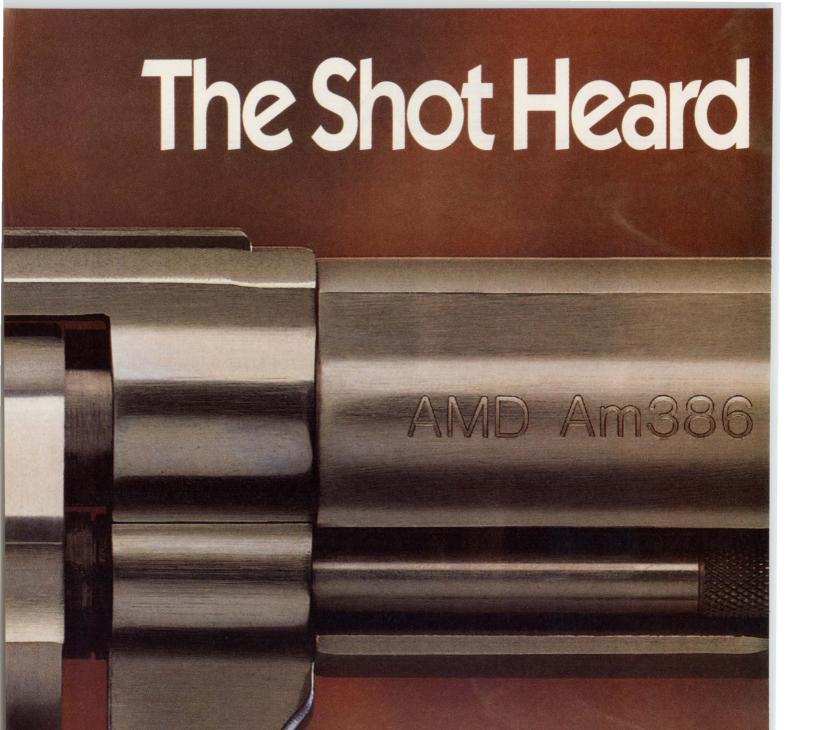
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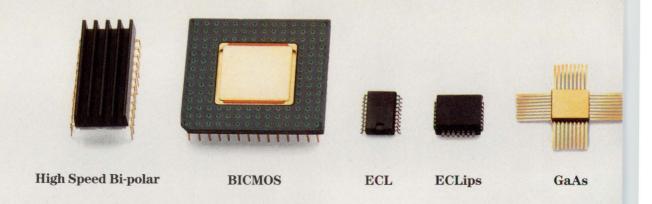
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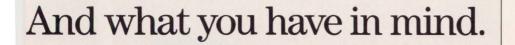
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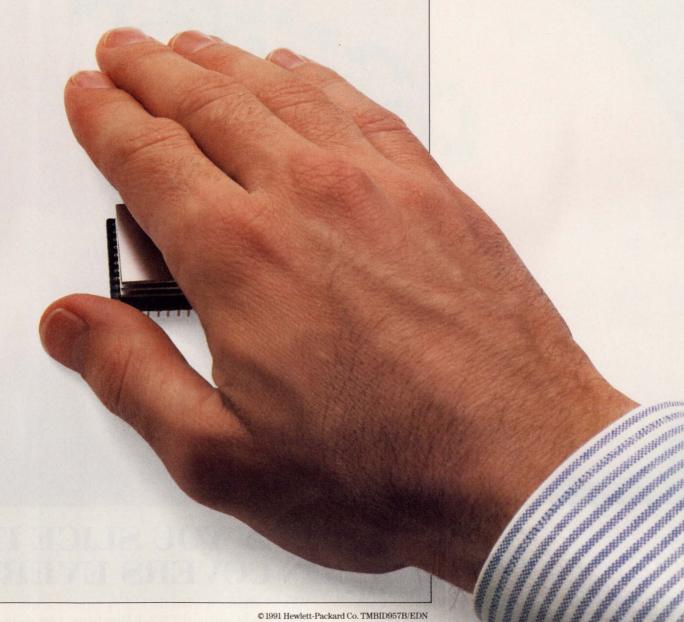


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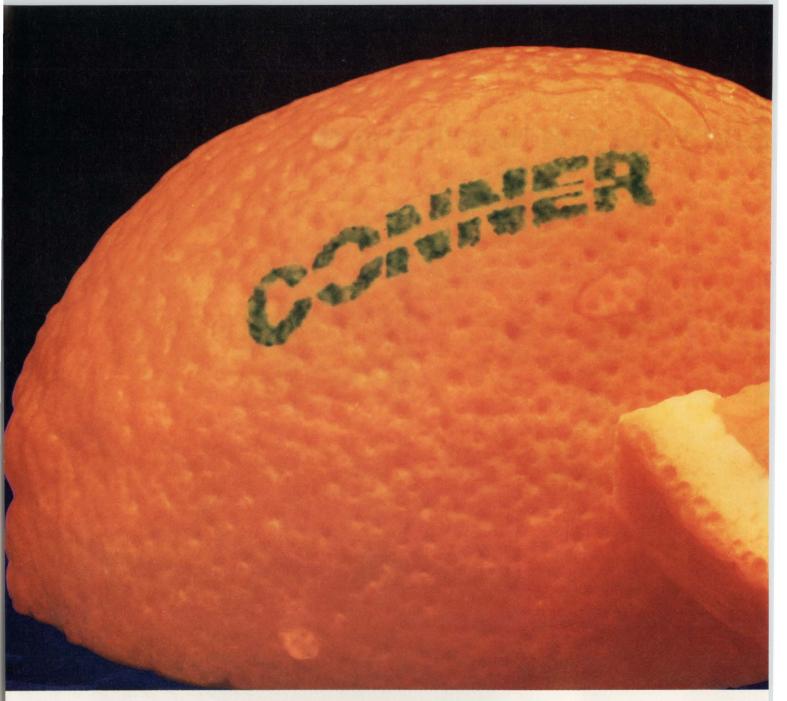
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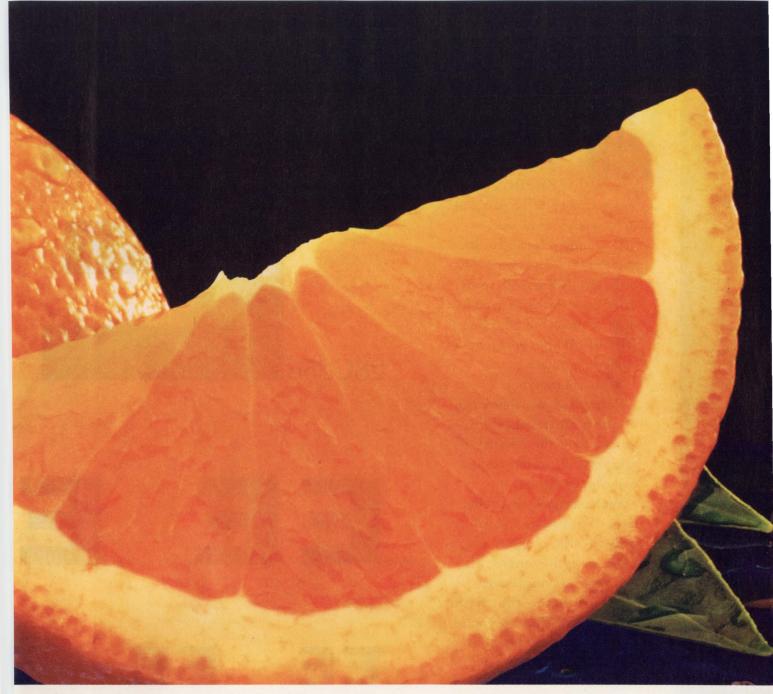


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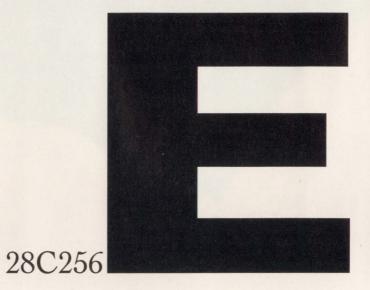
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NEWS BREAKS

EDITED BY SUSAN ROSE

VME BOARD TOPS 1.1 BOPS PERFORMANCE

A single V-C40 VME board from Ariel Corp sets a VME peak-performance mark—as much as 1.1 billion operations per second (BOPS). Additionally, it can move data at rates as high as 1.3 Gbytes/sec. The 6U VME board holds as many as four TI TMS320C40 32-bit floating-point DSP processors along with as much as 64 Mbytes of local dynamic RAM, and 8 Mbytes of static RAM (2 Mbytes per CPU). You can hook up processors and multiple boards in a number of multiprocessing configurations. Each board has six special byte-wide DMA communications ports, three of which are brought off board for 12 communications links, each capable of moving 20 Mbytes/sec. The board has a proprietary 24-bit bus for linking to analog converter cards. The board functions as both a VME bus master and slave and costs \$20 per million operations. Ariel Corp, Highland Park, NJ, (908) 249-2900, FAX (908) 249-2123.—Ray Weiss

PALM-SIZE INDUSTRIAL PC OPERATES FROM -40 TO +85°C

Suitable for use in rugged environments that present extreme temperatures, the 5012 Micro PC needs no keyboard, monitor, or disk drives to operate. With DOS embedded in its ROM, this computer includes two 512-kbyte solid-state data-storage locations that you can populate with RAM and EPROM. Housed on a pc-board, the computer comes with a built-in EPROM programmer, 1 Mbyte of dynamic RAM that you can expand to 2 Mbytes, a watchdog timer, battery backup for RAM, and a battery-backed calendar/clock. This board also contains ports for a printer, a keyboard, a speaker, and two serial ports. The basic board costs \$495, and you can order enclosures starting at \$45. Octagon Systems Corp, Westminster, CO, (303) 430-1500, FAX (303) 426-8126.—J D Mosley

MULTIPLY-ACCUMULATE UNIT ENHANCES SERVO CONTROLLER

An embedded multiply-and-accumulate unit (MAU) highlights a range of features of the HPC46100 16-bit microcontroller from National Semiconductor. Running off a 40-MHz system clock, the MAU provides 32-bit results from 16-bit, signed-integer multiply-and-accumulate operations in 400 nsec. Peripheral functions such as an 8-bit ADC with 5-usec conversion, three independent timers with separate frequencyand duty-cycle control registers, a programmable UART, and 1 kbyte of onboard RAM tailor the microcontroller to such embedded servo applications as found in automotive-chassis and hard-disk drive control. The ADCs convert as many as eight singleended channels or four differential-channel pairs. You can trigger the converters for single readings, or you can perform these operations continuously. Eight dedicated registers let you store single-channel data for average reading calculations. The onboard UART can operate in synchronous or asynchronous modes and offers multiple character widths and stop bits, status reporting, error detection, an addressing mode, and diagnostic testing. The μC is upward-source-code-compatible with the HPC family of controllers and includes such other features as watchdog logic, vectored interrupts, and HALT and IDLE power-down modes. Available development tools for the \$23 (1000), 14×14 -mm, 80-pin device include a development system. serial hook hardware, logic-analyzer interface board, HP logic-analyzer disassembler, and cross-development system. The device comes in a plastic quad flatpack. National Semiconductor, Santa Clara, CA, (408) 721-5185.—Michael C Markowitz

EDN October 1, 1991

NEWS BREAKS

COLOR PANEL-MOUNT DISPLAY INCLUDES 80386SX PC

Computer Dynamics's Color Displaypac includes an IBM PC-compatible 80386SX single-board computer and a color LCD with infrared touch screen in a panel-mount package. The integrated package measures $11.5\times8.5\times2$ in., and the display screen is 10.4 in. wide. The display provides VGA color graphics and includes a fluorescent backlight. The single-board computer includes as much as 4 Mbytes of dynamic RAM, two RS-232C serial ports, keyboard and printer ports, and hard- and floppy-disk interfaces. The computer can boot MS-DOS from an onboard RAM/ROM disk. A configuration with 1 Mbyte of memory and a 16-MHz μ P costs \$6174. Computer Dynamics, Greer, SC, (803) 877-8700, FAX (803) 879-2030.—Maury Wright

MPLD COMBINES AS MANY AS 40 ALTERA EPLDS

Altera's Mask-Programmable Logic Device (MPLD) can replace as many as 40 of the company's erasable programmable logic devices (EPLDs) or up to 700 of its macro cells. Offered as a synthesis service, the company will take EPLD designs at the netlist level and synthesize them into a single mask-programmed device. The company guarantees results from working designs using EPLD circuits, letting engineers prototype, and even put out as initial products, EPLD-based designs. For size reduction, they can then have the design reduced to a single, foundry-programmed mask-based chip. The conversion process is automated and the company will guarantee layout timing as well as 95%—or better—fault coverage for supplied test vectors. Prototypes will be delivered within 6 weeks of receipt of the design. The cost is \$0.06 per macro cell for production units; \$20,000 to \$60,000 for design conversions (NRE). Production units are delivered within 10 to 12 weeks. Initially, Classic and MAX 5000 EPLDs are covered, with MAX 700 devices added by the fourth quarter of 1991. Altera Corp, San Jose, CA, (408) 984-2800, FAX (408) 435-1394.—Ray Weiss

SOLID-STATE RELAYS SUIT LOW-CURRENT APPLICATIONS

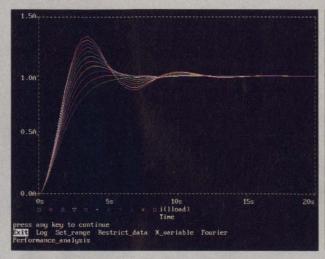
The LH1500 family of <1A solid-state relays from AT&T Microelectronics each comprise a photodiode array, various switch control circuits, and DMOS switches. The relays use an LED for actuation control and an IC for the switch output. The family consists of 21 products, ranging in price from \$1.25 to \$4.75 (1000) and includes all the common switch forms: normally open, normally closed, and combinations of each. Each relay features 3750V of isolation, thereby meeting European standards and exceeding US standards. The relays are constructed on a dielectrically isolated process, which provides for breakdown voltages between 140 and 440V. Typical on-resistance varies from 2 to 23Ω . Special features of some of the relays include current limiting, make-before-break switching, and dual packaging. The relays come in either 6- or 8-pin DIPs or surface-mount gull-wing packages. Sample quantities are available now; production quantities will be available by the fourth quarter of 1991. AT&T Microelectronics, Allentown, PA, (800) 372-2447.—Anne Watson Swager

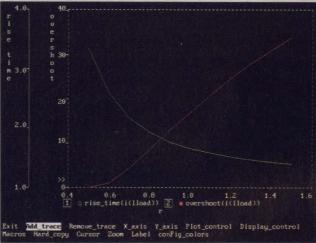
CMOS PLDs ACHIEVE 7.5-NSEC SPEED

Intel Corp's faster versions of its \$10 85C244 24-pin and \$6.10 (1000) 85C220 20-pin PLDs have programmable I/O structures, letting them emulate a variety of 20- and 24-pin PLD architectures. They have a 7.5-nsec input-to-output propagation delay and support clock frequencies as great as 74 MHz using external feedback. The parts consume 105 mA at maximum operating frequency and come in plastic leaded chip carriers. Intel Corp, Santa Clara, CA, contact local sales office.—Richard A Quinnell

18 EDN October 1, 1991

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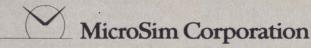
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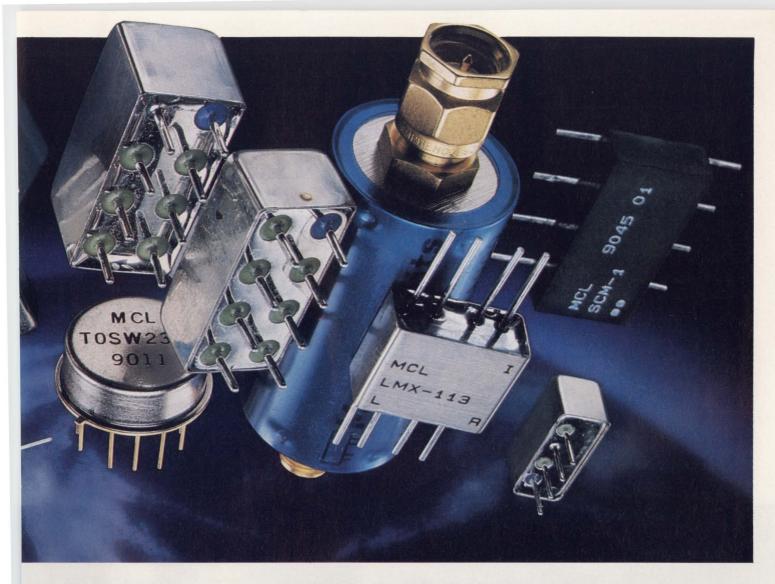
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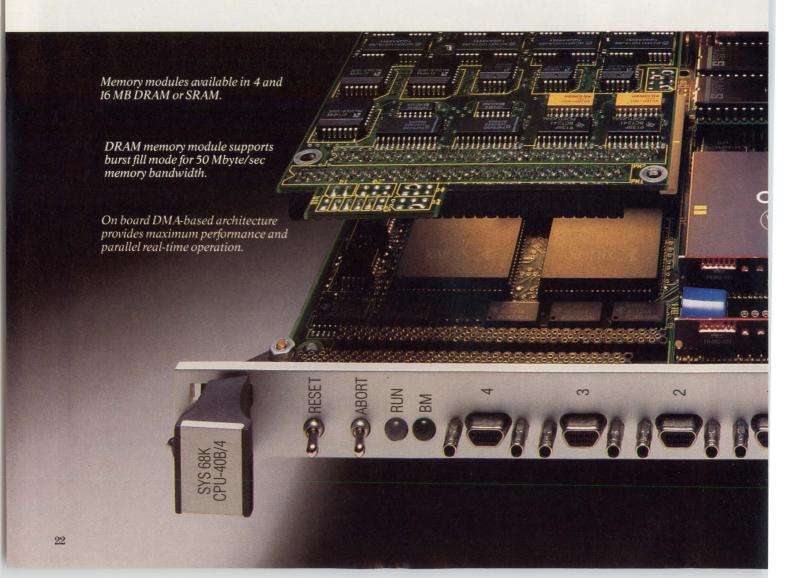
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CPU-40 PERFORMANCE CHARACTERISTICS

Data from	CPU	CPU	CPU	CPU	VMEbus	SCSI*	Floppy Disk*	Ethernet*	Shared RAM*	VMEbus
Transfer to	Shared RAM	EPROM	Serial I/O Timers	SCSI, Ethernet Controller, Floppy Disk	Shared RAM	Shared RAM	Buffer RAM	Dual-port RAM	VMEbus	VMEbus
Transfer Speed	53.7 MB/sec	16 MB/sec	2 MB/sec	2 MB/sec	5 MB/sec	4 MB/sec	500 KBit/sec	10 MBit/sec	15 MB/sec	15 MB/sec
Local 68040 CPU Operation	100%	100%	100%	100%	70%	80%	100%	100%	75%	100%

*DMA v FPS

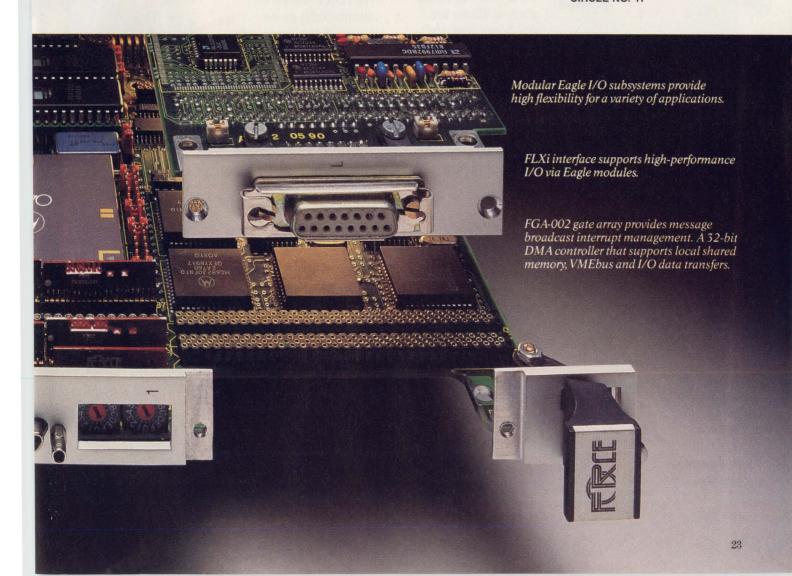
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CIRCLE NO. 11



People say boundary in low cost, high quality Now you can test that



Increasing device complexity. Rising pattern development costs. High density packaging.
Disappearing nodal access. These are the board test problems boundary scan was created to solve. Which is fine in theory. Only problem is there hasn't been any way to put boundary scan

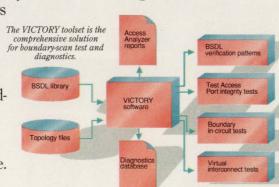
to the test. Until now.

Find common manufacturing faults without test pattern libraries or physical test access with boundary-scan design and VICTORY software.

VICTORY – the first software to automate boundary-scan testing.

Introducing VICTORY™ from Teradyne: the only software toolset ready to help you turn boundary-scan theory into a practical advantage. From the moment your first boundary-scan device is designed in,

VICTORY starts to simplify the testing of complex digital boards. And the more boundary-scan parts you have, the more time and money you save.



Delivers high faultcoverage.

Whether you're testing one boundary-scan part or boundary-scan networks, VICTORY software automatically gives you 100% pin-level fault coverage. Using the IEEE 1149.1 and BSDL standards, it takes VICTORY only a

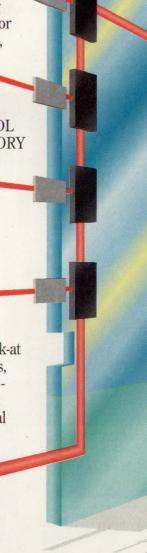
only a minute or two to generate test patterns. It would take a programmer days.

meaning when you use VICTORY's Access Analyzer to optimize board layout for testability and cost-efficiency.

engineering takes on neu

even weeks to deliver the same fault coverage for conventional designs.

Now you can find stuck-at faults, broken wire bonds, wrong or missing components—even open input pins—all without manual diagnostic probing.
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feedback you need to eliminate defects where it's most cost-effective—at the source.

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Boundary-Scan Intelligent Diagnostics identify faults by type and location without physical probing – even on high-density SMT assemblies

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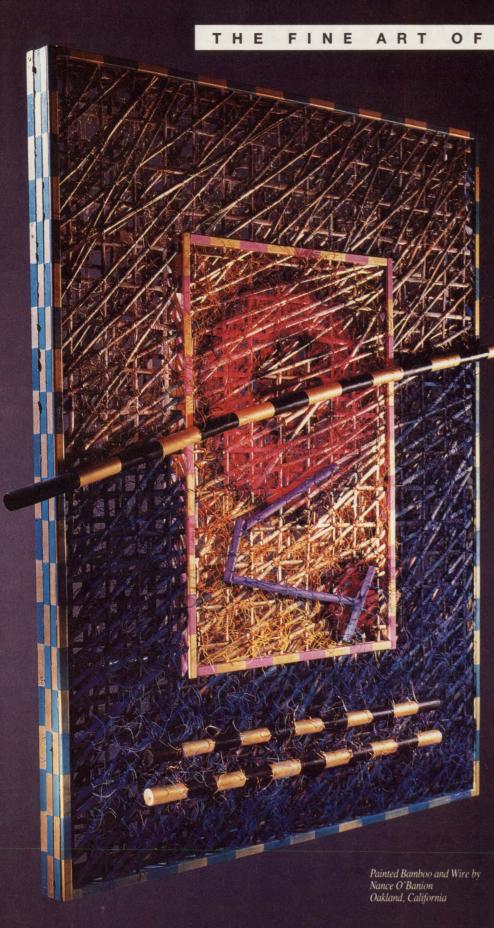
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SIGNALS & NOISE

Juggling equation for better solution

Just as my subscription to EDN is reinstated, Peter Anderson shocks me with the equation on pg 31 of EDN (May 23, 1991), [which uses N to characterize a triode]. For example, the dual triodes 12AU7, 12BH7, and 5687 all have values of a μ of 20, but only one may work properly in a circuit.

The value of μ is the ratio of $g_m \cdot MDSU / \cdot MDNM/to g_p$ or the product g_mr_p. You can double g_m and gp or halve rp by doubling the plate current, and the μ is unchanged. The point is that using the smallsignal equation

$$I_p = g_m V_g + g_p V_p,$$

where I_p is plate-current change and V_g and V_p are voltage changes, [would make a better basis for a Spice model.] The equation is related to the equation noted by Peter Anderson, but expresses the operating characteristics of a tube, a bipolar, or a FET device in a much more useful form. The above equation expresses the way we have to operate a [tube,] anyway. We set the plate current, then adjust the bias voltage with degeneration as needed to give that plate current.

Keats A Pullen Jr, PE Kingsville, MD

Engineer should look for higher paying job

The author of the letter "Engineers' salaries should be professional" (EDN, March 14, 1991, pg 26) suggests that, as a member of the engineering profession, he ought, by that very fact, to be paid a commensurate salary.

The thought is very lofty, but the fact of the matter is that salaries. like most economic matters, are ultimately a question of supply and demand. I really can't imagine a doctor or a lawyer saying, "Gee, guys, I'm a professional. You ought to pay me more."

If you feel you are worth more, then put it on the line and look for a higher paying job. Finally, your salary is a measure of your own capabilities combined with your marketing ability. The professionalism of the engineering profession has nothing to do with it.

Ted Ruel Controls Inc Logansport, IN

Battery of tests showed his true learning skills

I appreciated Charles Small's editorial, "Intelligences theory reshapes thought" (EDN's Software Engineering Special Supplement, June 20, 1991, pg 9). His article proves to be profoundly true in my case. I thought I was stupid until I received the results of a battery of tests in the Navy that showed I was not stupid—I just couldn't spell!

Engineers are a unique bunch who, if they cannot spell, will conceptualize, innovate, and design a software program to do it for

Charles Cutler Bear Medical Systems Inc Riverside, CA

Phone number changed

The phone number for Information Storage Devices Inc (EDN, July 4, 1991, pg 93) has been changed. The new number is (408) 428-1400.

NEXT IN EDN October 3

Look to EDN News Edition's October 3 issue for a Product Watch on ICs for automatic test equipment and a Career Opportunities article on multimedia.

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News Flash

SPORTS

The 90 Nanosecond Workout

An Exhaustive Look At High Tech **Training Equipment**

PAGE 2B

SCIENCE AND TECHNOLOGY

Virtual Reality Close But No Cigar

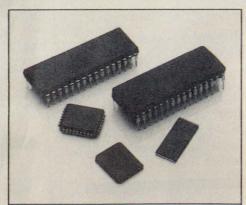
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FANTASTIC F



How Fast Is A Flash? A Direct Comparison

Density	AMD	Fastest Competito			
256K	90ns	120ns			
512K	90ns	120ns			
1 Mbit	90ns	120ns			
2 Mbit	90ns	150ns			

AMD Ships 2 **PLCC Flash**

SUNNYVALE - The computer industry takes a giant leap forward in performance with the help of the new Flash memory family from Advanced Micro Devices, Inc.

Flash memory is a high-density, reprogrammable, non-volatile technology that has a bright future in computation, laser printers, network and telecommunications hardware. Many military systems use Flash technology in radar and navigational applications. Flash memory also has the potential to eliminate mechanical hard disks and

the need for cumbersome batteries. These are two of the biggest and heaviest obstacles in laptop and notebook

computer applications.

Today, Flash memory is the most cost effective replacement technology for UV EPROMs and EEPROMs in applications that require in-system programming. Flash memories can literally be reprogrammed in a flash —

hence the name. Standard, But With A Little More Flash AMD's Flash memory famil effectively etches in silicon the de-fact standard for this burgeoning technolog that is compatible with Intel's initia Flash architecture.

Because AMD Flash memories an pin-for-pin compatible with the nov standard architecture, AMD is positioned as an alternate source for design engineers and purchasing agents

alike.

"Alternate source may be an inadequate term," said Jerry Sanders. chairman and CEO of Advanced Micro Devices. "Given our speed and feature set, our customers think of us as a superior resource."

Indeed, AMD's Flash memory family offers designers significant performance advantages (see chart), with speeds almost twice as fast as the nearest competitor.

Engineer Spontaneously Combusts At Meeting



EDN October 1, 1991

FromAMD

FOOD

Chips And Salsa

A Business Person's Guide To Silicon Valley Restaurants

MORNING EDITION

ASHE Megabit, 90ns, **Memories**

The AMD Flash family offers gners and purchasers many aging options. Particularly popular of its 1 Mbit part. designers and purchasers many packaging options. Particularly popular is AMD's advanced 2 Megabit, PLCC

is AMD's advanced 2 Megabit, PLCC part. Other packaging options include PDIP, CDIP and LCC in 256K, 512K, 1 Mbit and 2 Mbit capacities. TSOP packages will be available in the second half of this year. (LCC not currently available in 2 Mbit.)

AMD's 2 Mbit Flash memories come complete with embedded program and erase algorithms on board. These automatic algorithms speed upthe design process and considerably shorten time to market. Previously, engineers were required to develop tedious and time-consuming algorithms to implement insystem reprogrammability. AMD's system reprogrammability. AMD's automatic algorithms also allow several Flash memories to be written or erased at once, without tying-up the CPU. The system is now free to perform other asks while these operations are in

The Ultra-Violet Blues
Flash technology is particularly
suited to applications requiring
reprogramming in place, because these
devices can be reprogrammed in seconds,
and within the posterior and the control of the c

and within the system.

To update the code on a UV EPROM, the part must first be removed from the system. Once removed, erasure can take up to a full 20 minutes. After reprogramming, the part is then plugged back into the system. The process can result in damage to other components,

costly service calls, and headaches. Flash memories, on the other hand, can be bulk erased in about one to two can be but crased in about one to two seconds, without system disassembly. Reprogramming can then be accomplished via floppy disk, over phone lines, or even ISDN

ident To Speak

Stop the presses!

Advanced Micro Devices makes big news again—this time with an enhanced family of Flash memory devices.

That's good news for veteran and new Flash users alike.

Because our Flash devices are pin-for-pin compatible with Intel's existing Flash memory architecture, they establish the de facto industry standard.

Our standards, however, are a bit higher.

And so are yours.

That's why our Flash Memory family offers densities, speeds and packaging options that improve performance and save board space. For instance, our advanced 2 Mbit PLCC part with a scant 90 nanosecond delay.

You can also choose from Flash devices in 256K, 512K and 1 Mbit densities. As well as packaging options that fit your design best, including CDIP, PDIP, LCC, TSOP, and PLCC.

And you'll find implementation faster and easier than ever, because we've included automatic programming algorithms on all our 2 Mbit devices, and soon on our 1 Mbit parts. too. So you'll spend less time writing code, and take less time getting products to market.

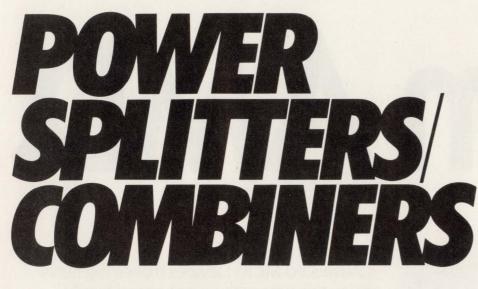
To keep up to date with all the latest and greatest in Flash memory, call AMD today at 1-800-222-9323. And start making some headlines of your own.



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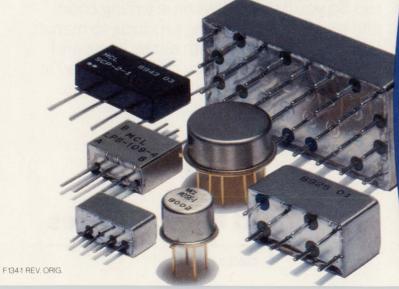
For detailed specs and performance data, refer to the MicroWaves Product Directory, EEM or MIni-Circuits RF/IF Signal Processing Handbook, Vol. II. Or contact us for our free 68-page RF/IF Signal Processing Guide.

CIRCLE NO. 14

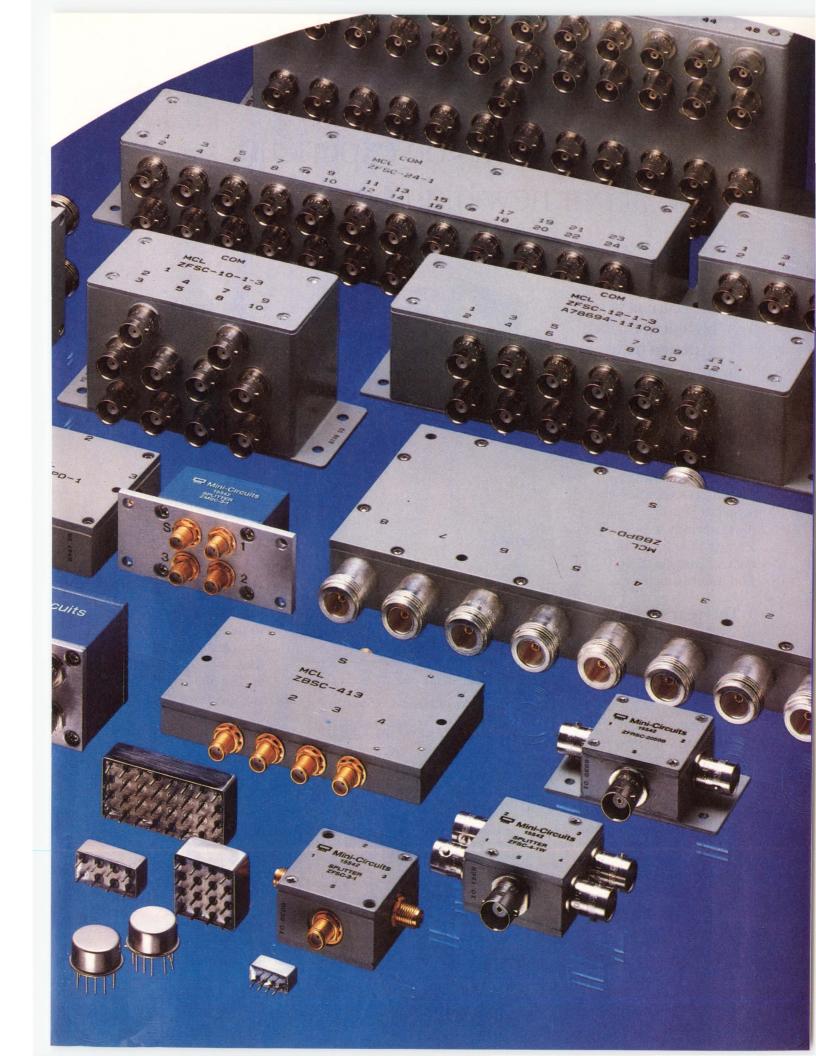
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- Modelling with SPICE
- Designing with new micropower op amps

Data Acquisition and Conversion



 One-chip data acquisition systems

• Understanding ADC specs for DSP

New solutions for

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- Designing with Simple Switchers
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National's Linear Circuit

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Sept. 26	Newark, CA	Oct. 24	Richardson, TX
Sept. 30	Montreal, QC	Oct. 25	La Jolla, CA
Oct. 1	Boxborough, MA	Oct. 28	Cleveland, OH
Oct. 2	Rochester, NY	Oct. 29	Indianapolis, IN
Oct. 3	Edison, NJ	Oct. 30	Dayton, OH
Oct. 4	Ft. Washington, PA	Oct. 31	Dearborn, MI
Oct. 7	Schaumburg, IL	Nov. 1	Schaumburg, IL
Oct. 8	Ft. Wayne, IN	Nov. 4	Englewood, CO
Oct. 9	Dearborn, MI	Nov. 5	Scottsdale, AZ
Oct. 10	Toronto, ON	Nov. 6	Woodland Hills, CA
Oct. 11	Minneapolis, MN	Nov. 7	Los Angeles, CA
Oct. 14	Orlando, FL	Nov. 8	Costa Mesa, CA
Oct. 15	Reston, VA	Nov. 12	Burnaby, BC
Oct. 16	Linthicum, MD	Nov. 13	Bellevue, WA
Oct. 17	Newton, MA	Nov. 14	Beaverton, OR
Oct. 21	Longmont, CO	Nov. 15	San Jose, CA

Oct. 22 Houston, TX

EDITORIAL

More diagrammatic programming tools for engineers



Little known or appreciated outside the world of tool and die makers, machine tools were nevertheless crucial to industrial development. Now, engineering software assumes the crucial role of the machine tool of the next industrial revolution.

Engineering software is too important and too different from ordinary software to be left solely to programmers. Give a carpenter a problem, and he thinks of solving it with hammers and nails. Give a programmer a problem, and he thinks of solving it with written-out lines of code. Unfortunately, engineers do not think or express themselves in terms of language. Instead, they use visual symbols.

Although we associate programming with text files, that association is not a fundamental given. In reality, programmers' fixation on text is an artifact of the teletypewriter output of early computers. Today, textual programming is no longer mandatory; even inexpensive computers can handle complex graphics and symbols. Few good software tools take advantage of these capabilities to let engineers construct programs visually.

Proponents of textual ASIC and FPGA software tools say that the increasing complexity of today's devices is forcing engineers to abandon diagrammatic systems for textual ones. This false imperative rests on an unproven foundation. Text is not inherently more comprehensible, lucid, compact, and rigorous than diagrams are. Few developers seem to consider the possibility that more complex devices may lead to more powerful diagrammatic design systems.

Good engineers are in the 99th percentile for spatial ability, and good programmers are in the 99th percentile for linguistic ability. Thus, we often find software kluges masquerading as tools that let users mix textual and diagrammatic design. Such tools best suit designers who are exceptional in both spatial and linguistic areas, and not enough such people are available to do all the engineering that needs to be done.

Therefore, everyone who has a hand in developing software tools for engineers should become familiar with Harvard researcher Howard Gardner's Theory of Multiple Intelligences. Gardner has written several popular books on the subject, and his theories provide the scientific underpinning for the notion that engineers need visual—not textual—design tools. Engineering-tool companies need to research the mental activity of creative engineers and then develop new visual metaphors that support the ways engineers think.





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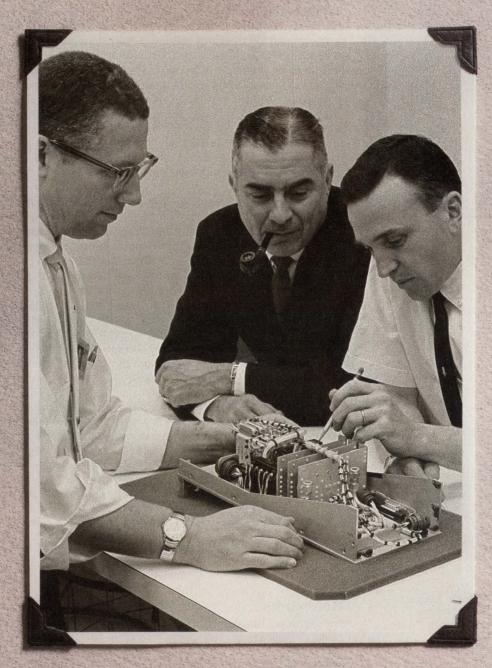
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2. Gardner, Howard, "The Mind's New Science: A History of Cognitive Revolution," Basic Books, New York, NY, 1987. ISBN 0-465-0435-5.

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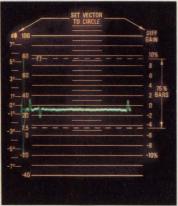
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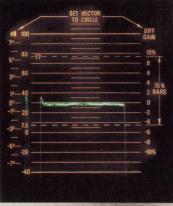
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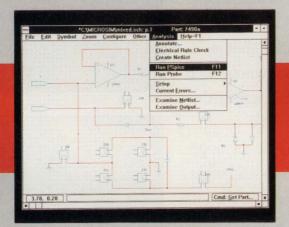


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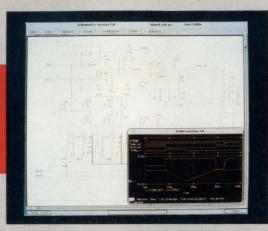
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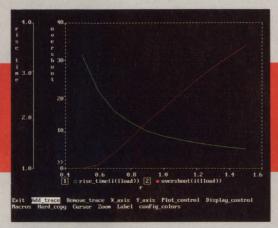
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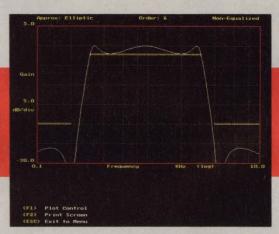
Probe provides interactive viewing of PSpice simulation results with high-resolution graphics including these features: Performance Analysis (new!), multiple Y axes (new!), flexible plot control, simultaneous display of analog and digital waveforms, fast Fourier transforms, and more.

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Performance Analysis: rise time and overshoot derived from multiple waveforms with stepped resistance



Bode plot in Filter Designer

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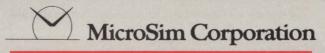
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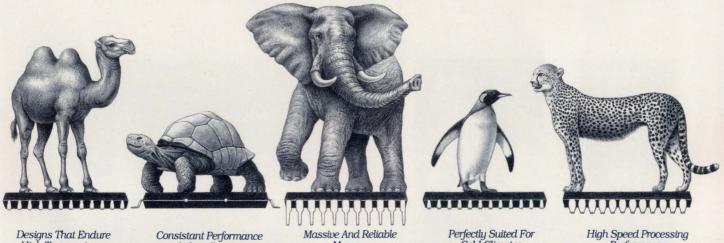
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	CXK581100YM	100/120	TSOP (reverse)	L/LL	B/X	Now
	CXK581001P	70/85	DIP 600mil	L/LL		Now
	CXK581001M	70/85	SOP 525mil	L/LL		Now
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SCPI instruments will ease ATE development

Engineers who want to minimize test-system development time and maximize system flexibility should use SCPI instruments whenever possible.

Maury Wright, Regional Editor he SCPI (Standard Commands for Programmable Instruments, pronounced "skippy") standard promises to simplify the programming of automatic test systems. Companies complying with the standard will ensure that similar instruments from different manufacturers have similar command languages. Thus, a programmer would need to learn how to program a voltmeter, frequency counter, or other instrument only once.

Most major instrument makers plan to use SCPI in all their new products.

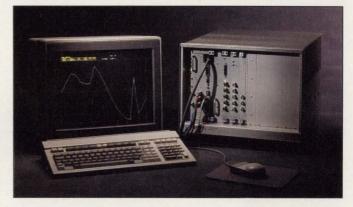
SCPI-compatible GPIB (General-Purpose Instrument Bus) and VXIbus test instruments have started to ship, but most types of SCPI instruments are still scarce. If you can find a SCPI version of a test instrument that you need now, buy SCPI compliance should be a determining factor when you choose instruments for a test system, and SCPI products cost the same as their non-SCPI counterparts.

The SCPI standard defines an extensible command language for the remote control of instruments. The language was developed independently of the front-panel terminology specific to individual instruments. The language uses a consistent style and English-like mnemonics, both of which make the language readable and easy to use. For example, the following command will read the dc voltage from any SCPI instrument that can measure voltage:

MEASure: VOLTage: DC?

The language's keywords can be written out in full or abbreviated to the 3- or 4-character strings indicated by the capital letters. Strings of keywords make up SCPI commands.

The creators of the SCPI standard sought to develop a language that offered what they termed vertical, horizontal, and functional compatibility. Vertical compatibility means that two instruments of the same generic instrument type, such as two digital oscilloscopes from different manufacturers, will have compatible command sets. A



The SCPI VXIbus arbitrary waveform generator from Hewlett-Packard, the \$8000 E1445A, is one of a variety of HP instruments that comply with the SCPI standard.

single software driver could control either instrument.

Horizontal compatibility refers to a situation in which two different types of instruments can perform the same measurement. For example, both frequency counters and digital oscilloscopes can measure the frequency of a signal. The horizontal-compatibility goal mandates that the same frequency-measurement command will properly instigate a frequency measurement in either type of instrument.

Functional compatibility refers to the



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The SCPI standard

compatibility of specific features in different types of instruments. For example, the same frequency and sweep commands can control a spectrum analyzer and a RF source because both types of instruments can sweep in frequency.

SCPI allows instrument updates

Designers who use SCPI-compatible instruments exclusively will realize several benefits. First, updating an ATE (automatic-testequipment) system with the best voltmeter available will require minimal changes in system and test software. Second, the time required to develop software for new ATE systems should drop because SCPI leads to reusable code. Third, programmers will be more efficient when using SCPI instruments because of the three types of compatibility and the fact that the language is easy to read and consistent in style.

SCPI poses no larger challenge to the first-time user than do the one-of-a-kind command sets currently common in instruments. Senior Electronics Engineer Mike Hanus of Sundstrand Power Systems

	Put subsystem mands
Keyword	Parameter form
INPut	
:ATTenuation	<numeric_value></numeric_value>
:AUTO	<boolean> ONCE</boolean>
:COUPling	AC DC
:FILTer	
[:LPASs]	
[:STATe]	<boolean></boolean>
:FREQuency	<numeric_value></numeric_value>
:HPASs	
[:STATe]	<boolean></boolean>
:FREQuency	<numeric_value></numeric_value>
:GAIN	<numeric_value></numeric_value>
:AUTO	< Boolean > ONCE
:GUARd	LOW FLOat
:IMPedance	< numeric_value >
:LOW [:STATe]	FLOat GROund <boolean></boolean>

(San Diego, CA) recently worked with a SCPI instrument for the first time. Hanus replaced a test set's programmable power source with a SCPI version. He reports that the software driver for the new source took no longer to write than did the original driver and that he wouldn't have had to write a new driver had the first source been SCPI compatible. Hanus says the experience has prompted him to write more modular code with the goal of reusing portions of his code for SCPI-compatible instruments.

The SCPI standard is independent of any physical interconnection specification. You will most often hear the term SCPI associated with VXIbus-based instruments and instruments that use the GPIB defined by the IEEE-488.1 specification. But SCPI works equally well on instruments connected to a controller via an RS-232C serial interface or any other interface.

Although the SCPI standard doesn't specify a physical interface, it does mandate the use of features defined in the IEEE-488.2 specification. The IEEE-488.2 standard defines controller functions, data formats, and status reporting—basically a common set of house-keeping commands for instruments. (See **Ref 1** for more information on the IEEE-488.2 specification.)

Alan Hoffman, director of engineering at IOtech, points out that SCPI offers a way for manufacturers to standardize the commands used for board-level PC instruments. IOtech offers a line of GPIB controller cards for IBM PCs. The Power488 and Power488CT cards also feature SCPI-compatible test-and-measurement capabilities. The

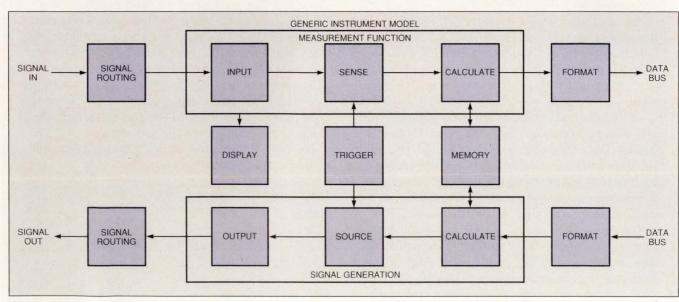


Fig 1—The generic instrument model depicted here guided the development of the tree-structured SCPI standard.

The SCPI standard

Power488 costs \$495 and includes 40 digital I/O lines in addition to the GPIB controller and driver software. The \$595 Power488CT adds counter/timer features.

SCPI's creators based the language on the generic instrument model in Fig 1 (see box, "SCPI Consortium controls standard," for a history of SCPI's creation). The SCPI standard defines a tree-like structure that has more than 20 ma-

jor subsystems as the main branches. The squares in Fig 1 correspond to major subsystems of the SCPI language. Additional major subsystems handle special instrument capabilities such as calibration and diagnostics. The box, "Major SCPI subsystems," lists the major command subsystems.

Look at **Table 1** for a sample of a SCPI command subsystem taken directly from the specification. The INPut command lets you program the conditioning an instrument applies to an incoming signal. Keywords in square brackets indicate default paths through the SCPI tree structure. A program can use one or more of the command options for the instrument in use.

Instruments don't need to implement commands from every SCPI subsystem. Instrument designers can choose the subsystems they

SCPI Consortium controls standard

A consortium of leading test-and-measurement instrument vendors defined SCPI and still controls the evolution of the standard. The consortium considers the standard to be "free and open"—any test equipment manufacturer can use SCPI commands in an instrument free of charge. The consortium continues to add to the SCPI standard to account for additional types of programmable instruments.

Customer demand led to the creation of SCPI. Sophisticated customers recognized that the time test programmers spent writing drivers for each new incompatible instrument was wasted. Hewlett-Packard reacted to the need for standardization among its varied instruments by creating its Test and Measurement Systems Language (TMSL), which the company introduced in August 1989. Simultaneously, a group of instrument vendors was contemplating a similar project. And for once in this intensively competitive electronics industry, the best possible thing happened. Hewlett-Packard contributed its TMSL work and joined the group of companies that went on to form the SCPI Consortium.

The consortium refined Hewlett-Packard's work and added capabilities. Tektronix contributed its Analog Data Interchange Format (ADIF) standard. ADIF provides a standard way to store analog data such as waveforms. In addition, ADIF includes environmental data such as scaling information, instrument settings, and time and date stamps.

The consortium moved quickly and published the first version of the SCPI standard in April 1990. The second version was published in June of this year, and the consortium plans to publish an updated spec annually. The consortium meets every two

months to discuss proposed additions to the SCPI standard. A private forum on the Compuserve dialup service includes up-to-date information on proposals, meeting schedules, and newly approved commands.

The founding members of the consortium are Bruel & Kjaer (Naerum, Denmark), John Fluke Mfg Co (Everett, WA), Hewlett-Packard Co (Loveland, CO), Keithley Instruments Inc (Cleveland, OH), National Instruments Corp (Austin, TX), Philips (Almelo, The Netherlands), Racal-Dana (Irvine, CA), Tektronix Inc (Beaverton, OR), and Wavetek Inc (San Diego, CA). The consortium now has more than 20 members.

Any company can join the SCPI Consortium. Sponsor memberships cost \$20,000 annually and include one seat on the consortium's board of directors. A contributing membership costs \$5000 annually and includes the right to vote on proposed additions to the standard. Five contributing members are elected to the board of directors each year. The \$750 associate membership grants access to the private SCPI Compuserve forum only. SCPI Consortium meetings are open to the public, and anyone can propose additions to the standard.

For more information on SCPI and to buy copies of the standard (\$50), contact

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The SCPI standard

need to control an instrument's features. The SCPI standard requires only that an instrument implement the SYSTem command subsystem.

Joe Mueller, a project manager at Hewlett-Packard and the company's representative to the SCPI Consortium, points out that SCPI allows for 100% control of an instrument's features. A typical instrument might implement 100 to 200 total SCPI commands, according to

Mueller. The average user may need no more than a dozen commands to develop a specific test program.

The most frequently used commands are those in the MEASure

Major SCPI subsystems

The following list describes the major subsystems that make up the main branches of the SCPI tree. The beginning capital letters indicate the subsystem's abbreviated form.

CALCulate—The CALCulate subsystem includes commands that control data-processing functions performed on data typically acquired by a SENSe command. For example, a CALCulate command can control the conversion of data from the frequency domain to the time domain.

CALibration—Commands in the CALibration subsystem control system-calibration functions.

DIAGnostic—The DIAGnostic subsystem includes all the service and diagnostic commands for routine maintenance and repair.

DISPlay—Commands in the DISPlay subsystem control the selection and presentation of textual, graphical, and TRACe information.

FORMat—The FORMat subsystem commands set the data format for transferring numeric and array information.

INPut—INPut subsystem commands control the characteristics, such as the attenuation, of a sensor's input ports.

INSTrument—INSTrument subsystem commands are used for instruments, such as a dual-channel power supply, that support multiple logical instruments.

MEASure—The MEASure subsystem defines a set of high-level instructions that are used to acquire data. This subsystem includes the most commonly used SCPI commands. The concept of horizontal compatibility defined in the SCPI standard is implemented in the MEASure subsystem.

MEMory—The MEMory subsystem commands manage the semiconductor memory instruments use to store various types of data.

MMEMory—MMEMory commands manage massstorage devices, such as disk drives, that are inside instruments or directly connected to instruments. OUTPut—Commands in the OUTPut subsystem

control the characteristics of a source's output port. For example, an OUTPut command can set the output source impedance of a signal.

PROGram—The PROGram subsystem commands provide control of one or more user-programmed tasks resident in an instrument.

ROUTe—ROUTe subsystem commands control instruments primarily designed to route signals. These commands also control signal routing on instruments that offer routing capability as a front end to input and output ports.

SENSe—The SENSe subsystem includes commands that directly set device-specific features before taking a measurement. An example of such a feature is an instrument's filter bandwidth.

SOURce—SOURce subsystem commands set device-specific features, such as modulation controls, on a signal source.

STATus—The STATus subsystem commands add status-reporting structures to those defined in IEEE-488.2.

SYSTem—The SYSTem subsystem includes the functions not related to instrument performance, such as the characteristics of an instrument's communications interface. This subsystem forms the command base required in all instruments.

TEST—The TEST subsystem extends standard instrument self-test procedures beyond those defined in IEEE-488.2.

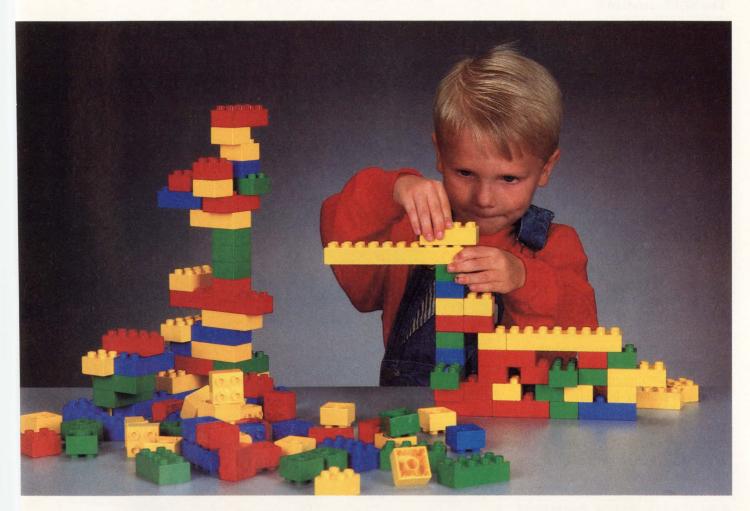
TRACe—Commands in the TRACe subsystem control the definition and manipulation of trace data.
TRIGger—The TRIGger subsystem commands

serve to synchronize instrument actions with other events.

UNIT—The UNIT subsystem provides a way to change the units of measure associated with an instrument feature.

VXI—Commands in the VXI subsystem include the administration functions associated with VXIbus-based systems.

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The SCPI standard

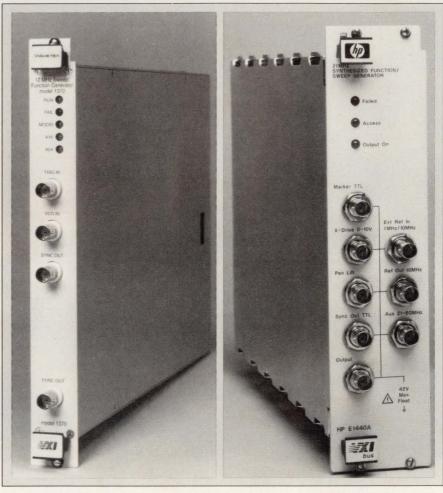
subsystem. The MEASure subsystem enjoys special status although it is a major branch on the SCPI tree with the more than 20 other subsystems. The MEASure subsystem implements the horizontal compatibility the SCPI specification defines.

Hewlett-Packard's Mueller offers an example that illustrates the horizontal compatibility SCPI makes possible and the philosophy behind it. He describes the compatibility of an integrating digital voltmeter with a sampling digital voltmeter. A test programmer could use SCPI's capabilities to program the sampling meter to take 4012 samples to measure dc voltage.

A program that commanded the integrating meter to take 4012 samples, however, might receive an error as an answer because the integrating meter doesn't take samples. The instrument designer could be clever and use SCPI to design the integrating meter so that it would take a meaningful measurement after such a request. The SCPI standard doesn't require instrument manufacturers to take such precautions, however.

Mueller suggests a way to write the test program that ensures an accurate measurement from SCPI-compliant instruments. The reason the programmer set the number of samples was to limit the amount and frequency of the ac voltage rejection present in the dc voltage measurement. You could use a higher-level SCPI command to instruct either meter to account for 60-dB rejection at 52 Hz, for example. The instrument would then take the measurement in the best possible way.

The thousands of possible SCPI command combinations will always make exact compatibility of instruments impossible. No two instruments—not even two voltmeters—



The synthesized sweep/function generator, Model 1378, from Wavetek demonstrates that SCPP's concept of vertical compatibility works. The command set of the VXIbus instrument on the left is compatible with that of the Hewlett-Packard E1440A sweep/function generator on the right.

have the exact same measurement capabilities. But SCPI does provide the means to achieve the vertical, horizontal, and functional compatibility of the specification.

Unfortunately, little evidence now exists that indicates how well SCPI will work in practice. Hewlett-Packard offers a line of VXIbus instruments and a few GPIB instruments that use SCPI. But HP had a head start on the industry because much of SCPI was derived from the company's Test and Measurement System Language (TMSL).

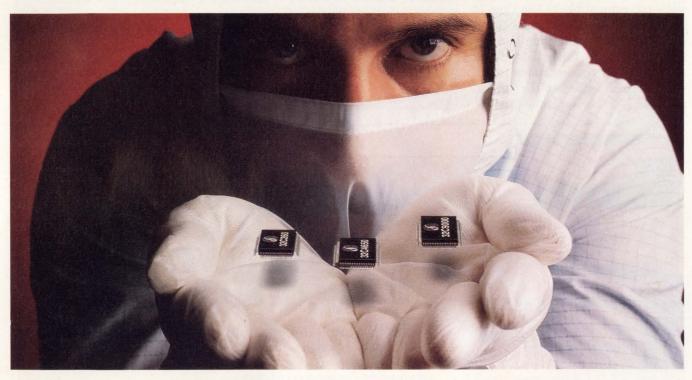
Other companies that now offer SCPI products include the Fluke

(Everett, WA) and Phillips (Almelo, The Netherlands) conglomerate. Between these two companies you can buy SCPI-compatible frequency counters, programmable power sources, and signal-switching systems. Finally, Wavetek, San Diego offers a line of VXIbus instruments for signal generation.

Thus far, the best example of SCPI success can be found in the compatibility between the Wavetek 1378 Synthesized Sweep/Function Generator (\$3295) and Hewlett-Packard's E1440A generator (\$5750). The products have a similar

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The SCPI standard

set of signal-generation capabilities and clearly demonstrate vertical compatibility. Bill Lee, Wavetek design engineer and the company's SCPI Consortium representative, points out that the SCPI standard includes explicit commands that let the companies implement all the desired functions. Thus, the instruments were compatible.

Both Hewlett-Packard and Wavetek also offer VXIbus arbitrary-function generators based on SCPI. The function generators were not compatible at the time of introduction. Both companies found the SCPI standard lacking in a few key areas required to exploit all the capabilities of the instruments. So each company added to the spec in different places and planned to pro-

pose the new commands to the SCPI Consortium as formal SCPI changes. Both companies worked on the new commands in secret because neither wanted to disclose features of an unannounced product.

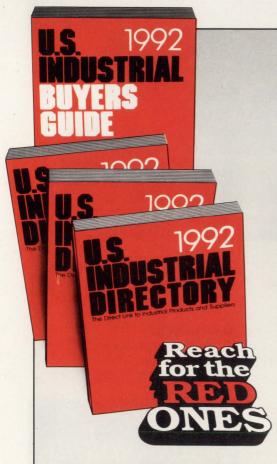
Wavetek engineers added com-

mands to the TRACe subsystem to perform additional waveform functions. Hewlett-Packard engineers added similar capability in the SOURce subsystem. The resulting products were not vertically compatible. Both companies presented their propos-

For more information . . .

For more information on the SCPI-based products discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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als to the committee, and a compromise ensued. Soon you will see revision B instruments from both companies that support the SCPI

Acronyms used in this article

ac-alternating current ADIF—Analog Data Interchange Format

ATE—automatic test equipment dc-direct current

GPIB—General-Purpose Instrument Bus

PC—personal computer

SCPI—Standard Commands for Programmable Instruments

TMSL—Test Measurement System Language

VXIbus-VMEbus extension for instrumentation

Consortium-approved compromise. The revision B function generators will be vertically compatible.

You can expect other conflicts to arise because of the competitive nature of the electronics industry and the constant influx of new products with new features. Also, the SCPI standard is admittedly short of commands that can control certain types of instruments, such as logic analyzers.

The SCPI Consortium, however, adds to the standard every two months. The consortium features an unprecedented level of cooperation in such a competitive industry. SCPI seems to be an idea with no drawbacks. Most major instrument vendors plan to use SCPI in all their new products, many of which will

be introduced over the next year. Shortly, designers who don't buy SCPI instruments exclusively will find the price, development time, and extensibility of their test systems lacking compared with SCPIbased systems. EDM

Reference

1. Leibson, Steven H, "IEEE-488.2 products are just now appearing," EDN, April 25, 1991, pg 91.

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Serial Channel			2			1	2
A/D Converter						8-Bit, 8 Channel	8-Bit, 16 Channel
Interrupts			4 Exte 16 Int			9 External 19 Internal	9 External 47 Internal
I/O Ports	1-Bit I/O Common		47 I 4 Input			58 I/O 8 Input Only	50 I/O 16 Input Only
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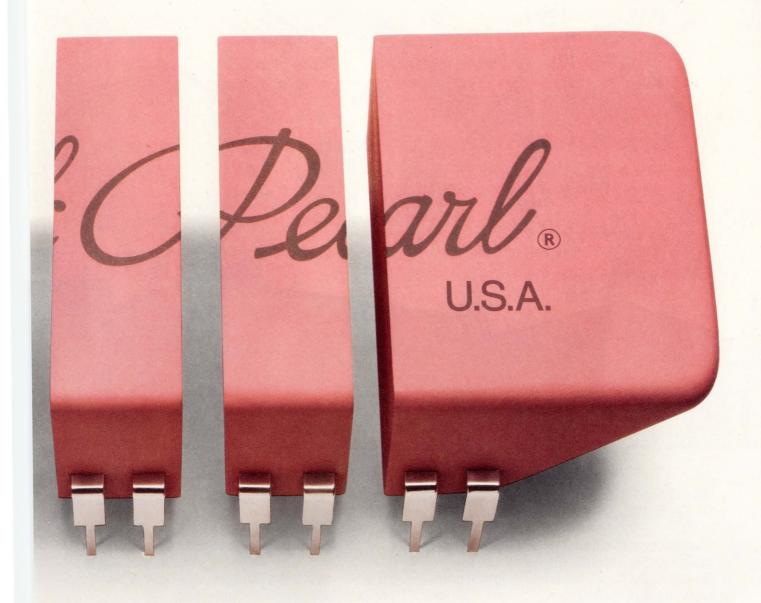
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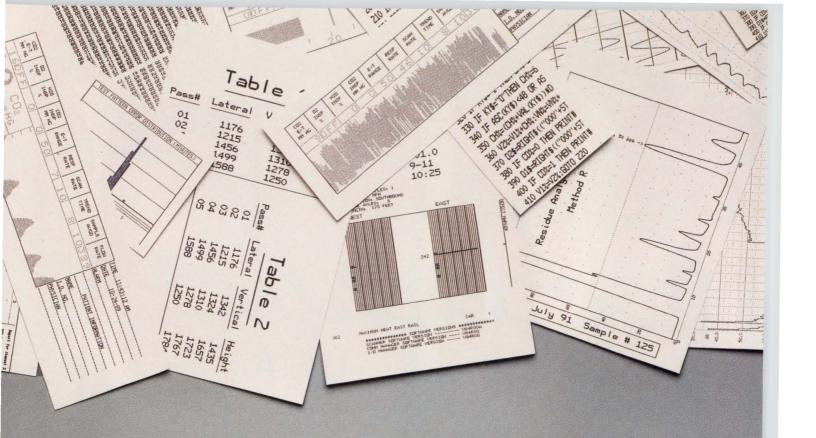
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SERIAL EEPROMS

Serial memory offers cheap frills

You don't need a byte-wide interface or large devices to add a little non-volatile memory to your system. Serial EEPROMs are an inexpensive option that offer a few extras.

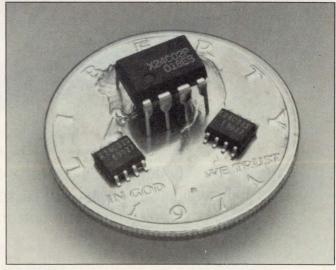
Richard A Quinnell, Regional Editor Serial EEPROMs provide an opportunity to add nonvolatile memory to your system at very low cost, both in terms of price and system resources. Newer devices also have the ability to protect your data, speed the data-transfer rate, and operate at lower voltages.

As the name implies, you interact with a serial EEPROM by clocking addresses, data, and commands into a single data line. A complete interface requires from two to five wires, depending on the type of device you use. The most common interface type, Microwire (developed by National Semiconductor), uses four lines. Some devices add a status pin to bring the total to five. Alternatively, you can reduce the number of lines needed by tying together the data input and output lines (see box, "Interfacing alternatives"). The Philips

interintegrated circuit (I²C) bus, running a close second to Microwire in availability, uses only two lines. Other available interfaces include UART-compatibles and those that work with Motorola's serial-pipeline interface (SPI).

The compact nature of the serial interface is vital if you're trying to produce a minimal system and still provide nonvolatile memory. For many microcontrollers, the CPU's address and data buses are not available outside of the IC, in order to conserve I/O pins. Most microcontrollers offer parallel ports, however, and designers needing off-chip memory use those ports to generate the needed address and data bits. Interfacing to a conventional memory device would consume at least 8 bits of the parallel port, versus the 2 to 5 bits for serial memory. Using a microcontroller with on-chip EEPROM is a possibility, but CPU vendors such as Zilog admit that a 2-chip design is less expensive than a CPU with onboard EEPROM.

In addition to offering a compact interface, the serial EEPROMs themselves are compact. Almost all of them, regardless of their bit density, are available in 8-pin DIPs, and many come in small-outline (SO) packages. The variety of bit densities having a common physical interface gives you the option of changing the amount of memory in



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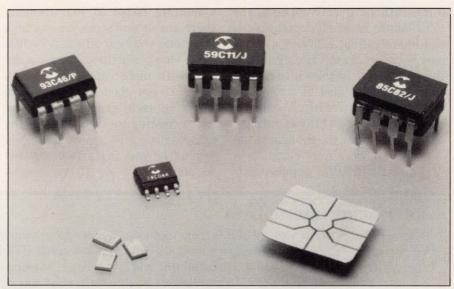
Serial EEPROMs

your design to increase capacity or decrease cost without affecting board layout or wiring. If you use devices having the I²C interface, you may not need to change software, either, because the I²C command protocol uses a fixed-length address field.

Nothing in life is free, however, including the serial EEPROM's advantages. There are a number of design considerations you must confront before deciding to incorporate serial EEPROM in your design. For example, using a serial interface extends the time required for memory access. In addition to the time needed to shift the data in and out, you must include the time to clock in a command code and an address for each transaction. Further, the serial protocols aren't always amenable to the use of byte-oriented serial peripherals. Therefore, vou'll have software overhead for converting the serial data to parallel, and vice versa. Finally, storing data in an EEPROM requires a considerable amount of time, on the order of 10 msec (Ref 1).

Page mode speeds data storage

Manufacturers of serial EEPROMs have implemented a number of improvements addressing the first of these considerations: access time. Some offer clock rates as fast as 1 MHz, for example, reducing the time required for shifting data out. Manufacturers have also reduced the command and address overhead by giving some of the serial EEPROM the ability to perform both page-oriented write transactions and sequential reads. Devices



Packaging options abound for serial EEPROMs. Microchip Technology, for example, offers DIP, small-outline (SO), chip-on-board (COB), and bare die for its products.

with the sequential-read capability let you specify a single address, then read all the data between that address and the end of memory without further addressing.

Access time is not the only consideration, however. Serial EEPROMs, like all EEPROMs. have a limited service life. EEPROMs store their data on a floating gate in each memory location. During erasing and writing, charge moves to or from the gate using quantum mechanical tunneling through the surrounding insulators. Each time an EEPROM cell is erased or written to, some electrons may become permanently trapped in the insulator. Over time, these trapped electrons build up enough charge to prevent the cell's proper operation. Using an EEPROM, therefore, requires careful attention to system design in order to minimize the number of erase/write cycles needed at a given memory location.

Manufacturers specify the lifetime of an EEPROM in terms of endurance: the minimum number of erase/write cycles a cell is guaranteed to provide. Read cycles do not affect a cell's endurance. As shown in **Table 1** (see pg 64), the endurance ratings of available serial EEPROMs range from 10,000 to 1 million cycles. Realize, however, that these are minimums; you may get a much greater lifetime in your application.

Endurance ratings vary

Ratings expressed by different manufacturers aren't always directly comparable, though, because their test methods differ. The differing conditions result in differing test results. Operation at elevated

Acronyms used in this article

CPU—central processing unit

DIP—dual in-line package

EEPROM—electrically erasable read-only memory

EIAJ—Electronic Industries Association of Japan

I²C—interintegrated circuit

JEDEC—Joint Electron Device Engineering Council

SO-small-outline package

UART—universal asynchronous receiver/transmitter

Serial EEPROMs

temperatures greatly speeds the cell's failure rate and decreases the endurance rating. Allowing a cell to rest between erase/write cycles, on the other hand, enables it to release some of the trapped electrons and extends its effective life. Therefore, when examining endurance ratings, be sure you know the conditions under which devices were rated.

If the EEPROM's endurance is

a limiting factor in your designs, there are several steps you can take to extend your circuit's service lifetime. One possibility is to use a device with more capacity than you need. If you check for cell failure following each write operation, or use a counter to keep track of the erase/write cycles you've used, you can move your data into another section of memory if one section

starts failing, then resume operation.

Alternatively, you may wish to use a nonvolatile RAM that offers a serial interface, such as the Catalyst CAT24C44 (\$1.50) and the Xicor X24C4 (\$1.11). These devices operate like a serial RAM, but have an EEPROM array backing the RAM array. If you need a nonvolatile copy of the data in RAM, you simply signal the device to copy the

Interfacing alternatives

Although there are a variety of interface methods for serial EEPROMs, only two are widely distributed: Microwire from National Semicondutor and the interintegrated circuit (I²C) from Philips. Each method has its own strengths and weaknesses.

Several fundamental differences exist between the two interfaces, the most obvious being the number of signals required. The Microwire interface uses four signals: data in, data out, chip select, and a shift clock. You activate the device by asserting chip select and clocking in an opcode and data address (if applicable). You then clock data in or out as applicable. The I²C bus uses only two wires, a clock and a data line. The I²C protocol calls for the bus master to send a slave address to activate the device desired, then the opcode and data. The slave device acknowledges reception of the address and each byte of opcode and data, then supplies any data requested. The I²C protocol prevents any contention on the shared data line.

You can reduce by one the number of I/O lines needed to connect to a Microwire device by tying the data-in and data-out lines together. This reduction is possible because the data-out line remains in a high-impedance state unless supplying read data. The danger in this approach is that the data-out line begins by supplying a dummy-zero bit as soon as the last address bit of the read command has entered the data-in line. If that address bit is high, the resulting bus contention may prevent the device from reading the address properly, or may result in excessive current being drawn into the device. Placing a current-limiting resistor in the connection between the data-in and data-out lines can help prevent damage, but may slow the data bus.

The two interfaces also differ in the way they indicate device status. Because EEPROMs require a relatively long time to complete erase or write

operations (worst case can be as long as 10 msec), most serial EEPROMs offer a method of indicating when the operation is complete. Using this status indication can speed your overall access to the memory; you don't have to wait for the worst-case time period to elapse before using the EEPROM again.

The Microwire interface requires you to poll the data output line following an erase or write instruction. The line changes state to indicate the device's readiness. Some older devices use the interface developed by General Instruments. They communicate with a Microwire-like serial protocol, but have separate busy/status lines. They are handy if you wish to use an interrupt to signal the processor to the memory's readiness, rather than poll a status line. I²C-compatible devices don't offer any specific signal—they simply fail to acknowledge a command string if they are still busy.

The speed of the interface and depth of memory are other differences. The I²C specification limits the serial clock rate to 100 kHz. Further, its fixed addressing protocol limits the total amount of memory that can reside on a single bus to 16 kbytes. The fixed protocol is not entirely a disadvantage, however. It enables you to make your interface software independent of the EEPROM's bit density, letting you increase or reduce memory without changing software. Microwire devices have a variable-length address, dependent upon their bit density.

The Microwire interface has no clock and addressing limits. Clock rates as high as 3 MHz are available, and the number of devices on a bus is limited only by your bus driver's capability. Recall, though, that each Microwire device needs a chip-select signal, so you'll need additional I/O ports to handle the additional memory.

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Serial EEPROMs

RAM into EEPROM. Similarly, you can load the RAM from the EEPROM array. This dual-array structure lets you make many changes to the contents of memory, using the EEPROM only when needed.

Another system consideration when choosing to use serial EEPROMs is the relative lack of standards for them. For example, the devices use a variety of interface protocols. Even with devices using the same protocol, there may be timing differences between manufacturers. Packaging is also nonstandard. The DIP versions of the EEPROMs are uniform, but surface-mount packages are diverse. There are two sizes of SO packages available, based on either the JEDEC or EIAJ standards. Although, by sizing the solder pads properly, you can accommodate either size device, the problem

doesn't end there. The pinout of the SO packages is not standardized. Two pinout patterns are available, corresponding to the direction the manufacturers' die fit within the SO package. If you are looking at alternate sources for your design, therefore, be sure to check the package size and pinouts.

If you can get past the design considerations, you'll find that serial EEPROMs offer a range of special features. During the last two years, manufacturers have added features to increase the versatility of serial EEPROMs. One such feature is selectable word size. Many serial EEPROMs are organized as a series of 16-bit-wide registers, with some available in 8-bit widths. To give you more flexibility in choice, manufacturers now offer devices with a selectable organization, controlled by the logic level at an I/O pin.

Another frill is the ability to write-protect a section of memory. Most serial EEPROMs will protect memory from inadvertent write access when the supply voltage is low. Further, they have a software command to disable write access to a part. Both of these features are designed to prevent inadvertent writes to the memory when power is unstable and logic behavior is unpredictable. The newer write-protection feature is the ability to lock out a portion of memory during normal operation. Parts from International CMOS Technology, for example, have a pin-controlled write protect that prevents writing to the entire memory, letting you use it as a ROM. Some parts from Microchip, on the other hand, protect only the top half of memory, allowing you free access to the lower half. This type of write-protect scheme lets you create calibration tables or con-

For more information . . .

For more information on the serial EEPROMs discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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Serial EEPROMs

figuration data, then lock them into the EEPROM.

A more flexible version of the write-protect scheme comes in the form of a programmable write-protect. This scheme, offered by several companies including Exel, National Semiconductor, Samsung, and SGS-Thomson, lets you select the beginning address of protected memory, thus protecting only the amount of memory you desire. This protection can be temporary or, by programming a special register, made permanent.

A unique data-protection scheme is available from Catalyst Semiconductor in its CAT33C704/804 series. These devices offer programmable write protection. Then, by programming the device with a password, you can convert the write-protected area of memory to read-protected memory, accessible only with the proper password. The remaining section of memory becomes write-protected. This secure-access feature is particularly useful if your EEPROM is to contain proprietary information, serial numbers, or access codes that you want to deny to the user.

Another relatively new feature of serial EEPROMs is low-voltage operation. Manufacturers have extended the operating voltage range of some serial EEPROMs to include typical battery voltages. Many now come in 3V versions, with some tolerating as low as 2.5V. Others, like the Exel parts, offer full operation to 3V and allow read-only operation as low as 2V.

Reference

1. Leibson, Steven H, "Nonvolatile, in-circuit-reprogrammable memories," *EDN*, January 3, 1991, pg 88.

Article Interest Quotient (Circle One) High 518 Medium 519 Low 520

		1	Organ-	Interface	Serial	Supply	y current	Endur-	Data reten-	Operating voltage			Price
Company	Part	Size (bits)	ization (bits)	compat- ibility	clock	Active (mA)	Standby (µA)	ance (cycles)	tion	range ¹ (volts)	Package styles ²	Special features	(10,000) (DIP)
Atmel	AT93C46	1k	64×16	Microwire	1 MHz	3	100	10k	10	5	DIP, SO	100k/100 year endurance option	\$0.77
	AT93C46-3	1k	64×16	Microwire	1 MHz	2	100	10k	10	3	DIP, SO	100k/100 year endurance option	\$0.96
	AT24C02	2k	256×8	I ² C	100 kHz	1.5	150	10k	10	5	DIP, SO	100k/100 year endurance option	\$0.99
	AT24C02-3	2k	256×8	I ² C	100 kHz	1	150	10k	10	3 to 6	DIP, SO	100k/100 year endurance option	\$1.51
	AT24C04	4k	512×8	I ² C	100 kHz	1.5	150	10k	10	5	DIP, SO	100k/100 year endurance option	\$1.70
	AT24C04-3	4k	512×8	I ² C	100 kHz	1	150	10k	10	3 to 6	DIP, SO	100k/100 year endurance option	\$2.46
Catalyst Semi-	CAT32C101	1k	64×16 or 128×8	Microwire	700 kHz	1	2	10k	10	2 to 4	DIP, SO	100k/100 year endurance option	\$1.69
conductor	CAT33C101	1k	64×16 or 128×8	Microwire	700 kHz	2	50	10k	10	3	DIP, SO	100k/100 year endurance option	\$0.85
	CAT33C201	1k	64×16 or 128×8	General Instruments	700 kHz	2	50	10k	10	3	DIP, SO	100k/100 year endurance option	\$0.79
	CAT59C11	1k	64×16 or 128×8	General Instruments	250 kHz	5	100	10k	10	5	DIP, SO	100k/100 year endurance option	\$0.63
	CAT93C46	1k	64×16 or 128×8	Microwire	700 kHz	3	100	10k	10	5	DIP, SO	100k/100 year endurance option	\$0.77
	CAT93C46A	1k	64×16	Microwire	700 kHz	3	100	10k	10	5	DIP, SO	100k/100 year endurance option	\$0.77
	CAT24C02	2k	256×8	I ² C	100 kHz	3	40	100k	100	5	DIP, SO	Page mode	\$1.13
	CAT24C02Z	2k	256×8	I ² C	100 kHz	3	0	100k	100	5	DIP, SO	MEN SHE SHE SHE	\$1.40
	CAT24LC02	2k	256×8	I2C	100 kHz	3	50	100k	100	3 to 6	DIP, SO	30.45 E 44E V	\$1.40
	CAT35C102	2k	128×16 or 256×8	Microwire	1 MHz	3	100	10k	10	5	DIP, SO	100k/100 year endurance option	\$1.13
	CAT35C202	2k	128×16 or 256×8	General Instruments	1 MHz	3	100	10k	10	5	DIP, SO	100k/100 year endurance option	\$1.44

Notes

1. Operating voltages have $\pm 10\%$ tolerance unless a range is shown.

2. DIPs listed are 8-pin, dual in-line packages unless noted, SOs are 8-pin, small-outline packages unless noted, and COB means chip on board.

Table continued

The FS700 LORAN-C frequency standard

10 MHz cesium stability

\$4950

Cesium long term stability at a fraction of the cost

Better long-term stability than rubidium

Not dependent on ionosphere position changes, unlike WWV

Complete northern hemisphere coverage, unlike GPS.

The FS700 LORAN-C frequency standard provides the optimum, cost-effective solution for frequency management and calibration applications. Four 10 MHz outputs from built-in distribution amplifiers provide cesium standard long-term stability of 10^{-12} , with short-term stability of 10^{-10} (10^{-11} optional). Reception is guaranteed in North America, Europe and Asia.

Since the FS700 receives the ground wave from the LORAN transmitter, reception is unaffected by atmospheric changes, with no possibility of missing cycles, a common occurrence with WWV due to discontinuous changes in the position of the ionosphere layer. Cesium and rubidium standards, in addition to being expensive initially, require periodic refurbishment, another costly item.

The FS700 system includes a remote active 8-foot whip antenna, capable of driving up to 1000 feet of cable. The receiver contains six adjustable notch filters and a frequency output which may be set from 0.01 Hz to 10 MHz in a 1-2-5 sequence. A Phase detector is used to measure the phase shift between this output and another front panel input, allowing quick calibration of other timebases. An analog output with a range of \pm 360 degrees, provides a voltage proportional to this phase difference for driving strip chart recorders, thus permitting continuous monitoring of long-term frequency stability or phase locking of other sources.



FS700: The optimum frequency management system



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Table 1—Representative serial EEPROMs (continued)

		Size	Organ- ization	Interface compat-	Serial clock		Standby	Endur- ance	Data reten- tion	Operating voltage range ¹	Package		Pric (10,00
Company	Part	(bits)	(bits)	ibility	rate	(mA)	(μA)	(cycles)	(years)	(volts)	styles ²	Special features	(DIF
Catalyst Semi-	CAT93C56	2k	128×16 or 256×8	Microwire	1 MHz	3	100	10k	10	5	DIP, SO	100k/100 year endurance option	\$1.1
conductor (continued)	CAT93LC56	2k	128×16 or 256×8	MIcrowire	250 kHz	2	50	10k	10	3	DIP, SO	100k/100 year endurance option	\$1.2
	CAT24C04	4k	512×8	I ² C	100 kHz	3	40	100k	100	5	DIP, SO	Page mode	\$2.2
	CAT24C04Z	4k	512×8	- 12C	100 kHz	3	0	100k	100	5	DIP, SO		\$2.5
	CAT24LC04	4k	512×8	I ² C	100 kHz	3	50	100k	100	3 to 6	DIP, SO		\$2.5
	CAT33C104	4k	256×16 or 512×8	Microwire	250 kHz	2	50	10k	10	3	DIP, SO	100k/100 year endurance option	\$2.5
	CAT33C704	4k	256×16 or 512×8	Synchro- nous	1 MHz	3	200	10k	10	3	DIP, SO, COB	100k/100 year endurance option, password protection	\$4.5
	CAT33C804A/B	4k	256×16 or 512×8	UART	9600 Baud	3	200	10k	10	3	DIP, SO, COB	100k/100 year endurance option, password protection	\$5.6
	CAT35C104	4k	256×16 or 512×8	Microwire	1 MHz	3	100	10k	10	5	DIP, SO	100k/100 year endurance option	\$2.5
	CAT35C704	4k	256×16 or 512×8	Synchro- nous	3 MHz	3	200	10k	10	5	DIP, SO, COB	100k/100 year endurance option, password protection	\$3.6
	CAT35C804A/B	4k	256×16 or 512×8	UART	9600 Baud	3	200	10k	10	5	DIP, SO, COB	100k/100 year endurance option, password protection	\$4.0
	CAT24C08	8k	1024×8	I ² C	100 kHz	3	40	100k	100	5	DIP, SO	Page mode	\$2.9
	CAT24C08Z	8k	1024×8	I ² C	100 kHz	3	0	100k	100	5	DIP, SO		\$3.
	CAT24LC08	8k	1024×8	I ² C	100 kHz	3	50	100k	100	3 to 6	DIP, SO	MARK THE STATE OF	\$3.
	CAT24C16	16k	2048×8	12C	100 kHz	3	40	100k	100	5	DIP, SO	Page mode	\$3.
	CAT24C16Z	16k	2048×8	12C	100 kHz	3	0	100k	100	5	DIP, SO		\$3.
	CAT24LC16	16k	2048×8	I ² C	100 kHz	3	50	100k	100	3 to 6	DIP, SO		\$3.
Exel - Micro-	XL93LC06	256	16×16	Microwire	1 MHz	2	2	100k	10	5	DIP, SO	Read operation to 2V, auto-increment	\$0.4
electronics	XL93LC06-3	256	16×16	Microwire	250 kHz	2	2	100k	10	2.7 to 5.5	DIP, SO	Read operation to 2V, auto-increment	\$0.5
	XL93C46	1k	64×16	Microwire	1 MHz	2	2	10k	10	5	DIP, SO	Read operation to 2V	\$0.5
	XL93C46-3	1k	64×16	Microwire	250 kHz	2	2	10k	10	2.7 to 5.5	DIP, SO	Read operation to 2V	\$0.5
	XL93CS46	1k	64×16	Microwire	1 MHz	2	2	10k	10	5	DIP, SO	Read operation to 2V, programmable data protection	\$0.
	XL93CS46-3	1k	64×16	Microwire	250 kHz	2	2	10k	10	2.7 to 5.5	DIP, SO	Read operation to 2V, programmable data protection	\$0.
	XL93LC46	1k	64×16	Microwire	1 MHz	2	2	100k	10	5	DIP, SO	Read operation to 2V, auto-increment	\$0.5
	XL93LC46-3	1k	64×16	Microwire	250 kHz	2	2	100k	10			Read operation to 2V, auto-increment	\$0.
	XL35LC102	2k	128×16	Microwire	1 MHz	2	2	100k	10	5		Read operation to 2V, auto-increment	\$1.
	XL35LC102-3 XL90C21	2k 2k	128×16	Microwire	250 kHz	3	100	100k	10	2.7 to 5.5	DIP, SO	Read operation to 2V, auto-increment Read operation to 2V	\$1.3
	XL90C21 XL93C56	2k	128×16	Microwire	1 MHz	2	4	10k	10	5	DIP, SO	Read operation to 2V	\$0.9
	XL93C56-3	2k	128×16	Microwire	250 kHz	2	4	10k	10	2.7 to 5.5	DIP, SO	Read operation to 2V	\$1.3
	XL93LC56	2k	128×16	Microwire	1 MHz	2	2	100k	10	5		Read operation to 2V, auto-increment	\$0.9
	XL93LC56-3	2k	128×16	Microwire	250 kHz	2	2	100k	10	2.7 to 5.5	DIP, SO	Read operation to 2V, auto-increment	\$0.9
	XL90C41	4k	256×16	Microwire	1 MHz	3	100	10k	10	5	DIP, SO	Read operation to 2V	\$1.2
	XL93C66	4k	256×16	Microwire	1 MHz	2	4	10k	10	5	DIP, SO	Read operation to 2V	\$1.2
	XL93C66-3	4k	256×16	Microwire	250 kHz	2	4	10k	10	2.7 to 5.5	DIP, SO	Read operation to 2V	\$1.8
	XL93LC66	4k	256×16	Microwire	1 MHz	2	2	100k	. 10	5		Read operation to 2V, auto-increment	\$1.2
	XL93LC66-3	4k	256×16	Microwire	250 kHz	2	2	100k	10	2.7 to 5.5	DIP, SO	Read operation to 2V, auto-increment	\$1.3

Notes:
1. Operating voltages have ±10% tolerance unless a range is shown.
2. DIPs listed are 8-pin, dual in-line packages unless noted, SOs are 8-pin, small-outline packages unless noted, and COB means chip on board.

			Organ-	Interface	Serial	Supply	current	Endur-	Data reten-	Operating voltage			Price
Company	Part	Size (bits)	ization (bits)	compat- ibility	clock rate	Active (mA)	Standby (µA)	ance (cycles)	tion (years)	range ¹ (volts)	Package styles ²	Special features	(10,000 (DIP)
Inter- national	93C46A	1k	64×16	Microwire	2 MHz	3	50	10k	40	5	DIP, SO	3V version available, hardware write protect	\$0.60
CMOS Technology	93C56A	2k	128×16	Microwire	2 MHz	3	50	10k	40	5	DIP, SO	Hardware write protect	\$1.65
	93CX56	2k	128×16	Microwire	1 MHz	4	50	10k	40	2.5 to 6	DIP, SO	Hardware write protect	\$2.25
	93C66A	4k	256×16	Microwire	2 MHz	3	50	10k	40	5	DIP, SO	Hardware write protect	\$2.30
	93CX66	4k	256×16	Microwire	1 MHz	4	50	10k	40	2.5 to 6	DIP, SO	Hardware write protect	\$2.90
Microchip	93C06	256	16×16	Microwire	1 MHz	4	100	100k	10	5	DIP, SO		\$0.53
Technology	24C01A	1k	128×8	I ² C	100 kHz	3.5	100	100k	10	5	DIP, SO	Sequential read, page mode	\$0.98
	24LC01	1k	128×8	I ² C	100 kHz	2	100	100k	10	2 to 5.5	DIP, SO	Sequential read, page mode, hardware write protect	\$1.05
	59C11	1k	64×16 or 128×8	General Instruments	1 MHz	4	100	100k	10	5	DIP, SO	Sequential read, page mode, hardware write protect	\$0.55
	85C72	1k	128×8	I ² C	100 kHz	3.5	100	100k	10	5	DIP, SO	Sequential read, page mode	\$1.03
	93C46	1k	64×16	Microwire	1 MHz	4	100	100k	10	5	DIP, SO	Sequential read, page mode, hardware write protect	\$0.55
	24C02A	2k	256×8	I ² C	100 kHz	3.5	100	100k	10	5	DIP, SO	Sequential read, page mode, hardware write protect	\$1.02
	24LC02	2k	256×8	I2C	100 kHz	2	100	100k	10	2 to 5.5	DIP, SO	Sequential read, page mode, hardware write protect	\$1.10
	85C82	2k	256×8	I ² C	100 kHz	3.5	100	100k	10	5	DIP, SO	Sequential read, page mode	\$1.07
	93C56	2k	128×16 or 256×8	Microwire	2 MHz	4	100	100k	10	4 to 5.5	DIP, SO	Sequential read	\$1.05
	24C04A	4k	512×8	I ² C	100 kHz	3.5	100	100k	10	5	DIP, SO	Sequential read, page mode, hardware write protect	\$1.44
	24LC04	4k	512×8	I ² C	100 kHz	2	100	100k	10	2 to 5.5	DIP, SO	Sequential read, page mode, hardware write protect	\$1.52
	85C92	4k	512×8	I ² C	100 kHz	3.5	100	100k	10	5	DIP, SO	Sequential read, page mode	\$1.52
	93C66	4k	256×16 or 512×8	Microwire	2 MHz	4	100	100k	10	4 to 5.5	DIP, SO	Sequential read	\$1.28
	24LC16	16k	2048×8	I ² C	100 kHz	2	100	100k	10	2 to 5.5	DIP, SO	Sequential read, page mode, hardware write protect	\$3.56
National Semi-	NM93C06	256	16×16	Microwire	1 MHz	0.4	25	500k	40	2 to 5.5	DIP, SO	5V-only version available	\$0.63
conductor	NM93CS06	256	16×16	Microwire	1 MHz	0.4	25	500k	40	2 to 5.5	DIP, SO	Sequential read, pro- grammable write pro- tect, 5V-only version	\$1.57
	NM59C11	1k	64×16 or 128×8	General Instrument	1 MHz	0.4	25	500k	40	5	DIP, SO		\$0.82
	NM93C46	1k	64×16	Microwire	1 MHz	0.4	25	500k	40	2 to 5.5	DIP, SO	5V-only version available	\$0.75
	NM93C46A	1k	64×16	Microwire	1 MHz	0.4	25	500k	40	5	DIP, SO		\$0.82
	NM93CS46	1k	64×16	Microwire	1 MHz	0.4	25	500k	40	2 to 5.5	DIP, SO	Sequential read, pro- grammable write pro- tect, 5V-only version	\$1.82
	NM95C12	1k	64×16	Microwire	1 MHz	0.4	25	40k	10	5	14-pin DIP, 14-pin SO	8 onboard DIP switches	\$3.10
	NM24C02	2k	256×8	I ² C	100 kHz	0.4	25	500k	40	5	DIP, 14- pin SO	Page mode	\$0.90

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Operating voltages have ±10% tolerance unless a range is shown.
 DIPs listed are 8-pin, dual in-line packages unless noted, SOs are 8-pin, small-outline packages unless noted, and COB means chip on board.

Table 1—Representative serial EEPROMs (continued)

Company	Part	Size (bits)	Organ- ization (bits)	Interface compat- ibility	Serial clock rate		Standby (µA)	Endur- ance (cycles)	Data reten- tion (years)	Operating voltage range ¹ (volts)	Package styles ²	Special features	Price (10,000 (DIP)
National Semi-	NM24C03	2k	256×8	I ² C	100 kHz	2	60	500k	40	5	DIP, 14- pin SO	Page mode, hardware write protect	\$1.05
conductor (continued)	NM93C56	2k	128×16	Microwire	1 MHz	0.4	25	500k	40	2 to 5.5	DIP, SO	5V-only version available	\$1.19
	NM93CS56	2k	128×16	Microwire	1 MHz	0.4	25	500k	40	2 to 5.5	DIP, SO	Sequential read, pro- grammable write pro- tect, 5V-only version	\$3.07
	NM24C04	4k	512×8	I2C	100 kHz	2	60	500k	40	5	DIP, 14- pin SO	Page mode	\$1.45
	NM24C05	4k	512×8	I ² C	100 kHz	2	60	500k	40	5	DIP, 14- pin SO	Page mode, hardware write protect	\$1.60
	NM93C66	4k	256×16	Microwire	1 MHz	0.4	25	500k	40	2 to 5.5	DIP, SO	5V-only version available	\$2.25
	NM93CS66	4k	256×16	Microwire	1 MHz	0.4	25	500k	40	2 to 5.5	DIP, 14- pin SO	Sequential read, pro- grammable write pro- tect, 5V-only version	\$5.00
	NM24C08	8k	1024×8	I ² C	100 kHz	2	60	500k	40	5	DIP, 14- pin SO	Page mode	\$2.85
	NM24C09	8k	1024×8	I ² C	100 kHz	2	60	500k	40	5	DIP, 14- pin SO	Page mode, hardware write protect	\$3.05
Oki Semi- conductor	MSM16881	1k	64×16 or 128×8	Microwire	250 kHz	3	100	10k	10	5	DIP, SO		\$0.80
	MSM16911	1k	64×16 or 128×8		250 kHz	3	100	10k	10	5	DIP, SO		\$0.80
	MSM16812	2k	128×16 or 256×8	Microwire	1 MHz	3	100	10k	10	5	DIP		\$1.50
	MSM16912	2k	128×16 or 256×8	General Instruments	1 MHz	3	100	10k	10	5	DIP	5.多卷度。	\$1.50
Samsung	KM93C06	256	16×16	Microwire	250 kHz	5	100	100k	10	5	DIP, SO		\$0.42
Semi- conductor	KM93C07	256	16×16	Microwire	250 kHz	5	100	100k	10	5	DIP, SO		\$0.43
	KM93C46	1k	64×16	Microwire	250 kHz	5	100	100k	10	5	DIP, SO		\$0.45
	KM93C46V	1k	64×16	Microwire	250 kHz	5	100	100k	10	2.7 to 5.5	DIP, SO		\$0.47
	KM93C56	2k	128×16	Microwire	1 MHz	1	50	100k	10	2.7 to 5.5	DIP, SO		\$0.80
	KM93CS56	2k	128×16	Microwire	1 MHz	1	50	100k	10	2.7 to 5.5	DIP, SO	Programmable write protect	\$1.00
	KM93C57	2k	128×16 or 256×8	Microwire	1 MHz	1	50	100k	10	2.7 to 5.5	DIP, SO		\$0.82
	KM93C66	4k	256×16	Microwire	1 MHz	1	50	100k	10	2.7 to 5.5	DIP, SO		\$1.30
	KM93CS66	4k	256×16	Microwire	1 MHz	1	50	100k	10	2.7 to 5.5	DIP, SO	Programmable write protect	\$1.50
	KM93C67	4k	256×16 or 512×8	Microwire	1 MHz	1	50	100k	10	2.7 to 5.5	DIP, SO		\$1.32
SGS- Thompson Micro-	ST93C06	256	16×16 or 32×8	Microwire	1 MHz	2	50	1M	10	5	DIP, SO		\$0.50
electronics	ST24C01	1k	128×8	I ² C	100 kHz	5	100	1M	10	5	DIP, SO	Page mode, sequential read	\$0.62
	ST93C46A ST93CS46	1k	64×16 or 128×8 64×16	Microwire Microwire	1 MHz	2	50	1M 1M	10	5	DIP, SO,	Page mode, program-	\$0.84
	31930340	''	04210	Microwite	1 101112	2	30	IIVI	10	3	14-pin SO	mable write protect	φυ.σ-
	ST93CS47	1k	64×16	Microwire	1 MHz	2	50	1M	10	2.5 to 5.5	DIP, SO, 14-pin SO	Page mode, program- mable write protect	\$1.10
	ST24C02A	2k	256×8	I ² C	100 kHz	2	100	1M	10	5	DIP, SO	Page mode, sequential read, programmable write protect	\$0.84
	ST25C02A	2k	256×8	I ² C	100 kHz	2	100	1M	10	2.5 to 5.5	DIP, SO	Page mode, sequential read, programmable write protect	\$1.10
	ST93CS56	2k	128×16	Microwire	1 MHz	2	50	1M	10	5	DIP, SO, 14-pin SO	Page mode, program- mable write protect	\$0.94

Notes:

1. Operating voltages have ±10% tolerance unless a range is shown.

2. DIPs listed are 8-pin, dual in-line packages unless noted, SOs are 8-pin, small-outline packages unless noted, and COB means chip on board.

1		1	Organ-	Interface	Serial	Supply	y current	Endur-	Data reten-	Operating voltage			Price
Company	Part	Size (bits)	ization (bits)	compat- ibility	clock		Standby (µA)	ance (cycles)	tion (years)	range ¹ (volts)	Package styles ²	Special features	(10,000 (DIP)
SGS- Thompson Micro-	ST93CS57	2k	128×16	Microwire	1 MHz	2	50	1M	10	2.5 to 5.5	DIP, SO, 14-pin SO	Page mode, program- mable write protect	\$1.40
electronics (continued)	ST24C04	4k	512×8	I ² C	100 kHz	2	100	1M	10	5	DIP, 14- pin SO	Page mode, sequential read, programmable write protect	\$1.85
	ST25C04	4k	512×8	I ² C	100 kHz	2	100	1M	10	2.5 to 5.5	DIP, 14- pin SO	Page mode, sequential read, programmable write protect	\$2.40
Signetics	PCF8581	1k	128×8	I ² C	100 kHz	1.6	10	10k	10	5	DIP, SO	Page mode, sequential read	\$0.94
	PCF8581C	1k	128×8	I ² C	100 kHz	1.6	10	10k	10	2.5 to 6	DIP, SO	Page mode, sequential read	\$0.94
	PCF8582B	2k	256×8	I ² C	100 kHz	1.6	10	500k	10	5	DIP, SO, 16-pin SO	Page mode, sequential read	\$0.99
	PCF8582C	2k	256×8	I ² C	100 kHz	1.6	10	500k	10	2.5 to 6	DIP, SO, 16-pin SO	Page mode, sequential read	\$0.99
Xicor	X24C01	1k	128×8	I ² C	100 kHz	1	50	100k	100	5	DIP, SO	3.3V and 3.5 to 5.5V versions available	\$0.65
	X24C01A	1k	128×8	I ² C	100 kHz	1	50	100k	100	5	DIP, SO	3.3V and 3.5 to 5.5V versions available	\$0.77
	X24C02	2k	256×8	I ² C	100 kHz	1	50	100k	100	5	DIP, SO	3.3V and 3.5 to 5.5V versions available	\$0.94
	X24C04	4k	512×8	I ² C	100 kHz	1	50	100k	100	5	DIP, SO, 14-pin SO	3.3V and 3.5 to 5.5V versions available	\$1.55
	X24C08	8k	1024×8	I ² C	100 kHz	1	50	100k	100	5	DIP, SO, 14-pin SO	3.3V and 3.5 to 5.5V versions available	\$2.40
	X24C16	16k	2048×8	I ² C	100 kHz	1	50	100k	100	5	DIP, SO, 14-pin SO	3.3V and 3.5 to 5.5V versions available	\$3.36

Notes:

- 1. Operating voltages have ±10% tolerance unless a range is shown.
- 2. DIPs listed are 8-pin, dual in-line packages unless noted, SOs are 8-pin, small-outline packages unless noted, and COB means chip on board.

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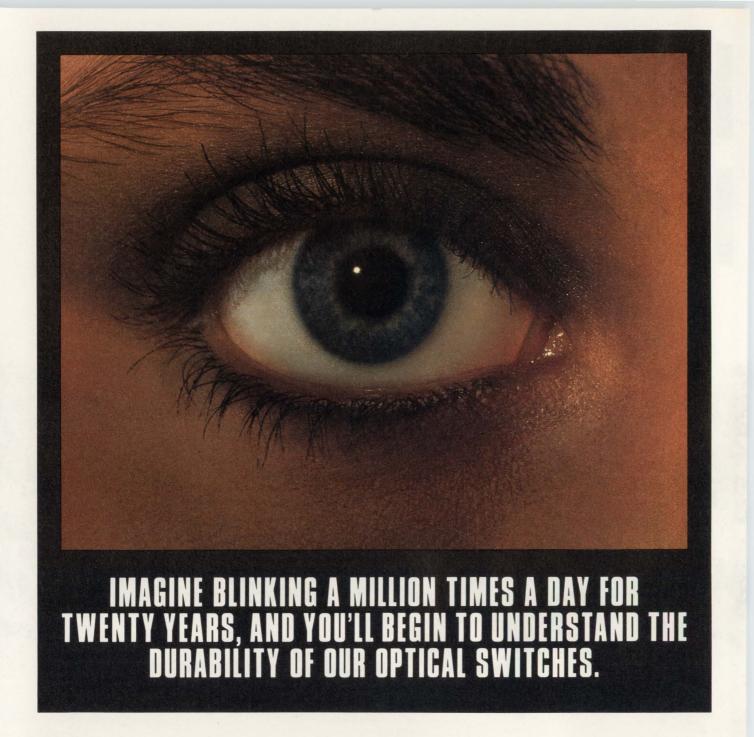
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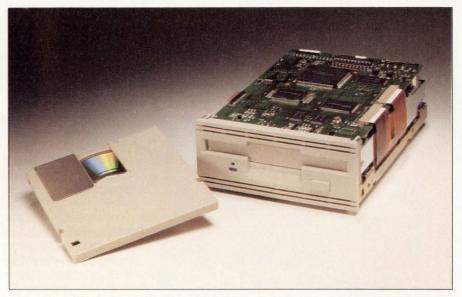
3½-in. optical drive offers MO and read-only modes

he OD-3000 optical disk drive lets designers buy optical technology in the increasingly popular 3½-in. form factor. The multifunction drive uses read/write MO (magneto-optical) technology and reads O-ROM (optical read-only memory) disks, whose features are similar to those of 5½-in. CD-ROM disks. The drive stores 128 Mbytes on a removable optical disk that looks much like a 3½-in. floppy disk.

MO technology gives the OD-3000 several advantages compared with $5^{1/4}$ -in. products that use other types of rewritable optical media. MO technology uses magnetic-flux transitions to store data on the physical medium. The optical system writes to the disk using a laser beam to change the magnetic polarity of data bits on the disk. Likewise, the optical system reads data by sensing the reflection of the laser beam from the surface of the disk. Disks that use MO technology can withstand 10 million write cycles and still record data reliably. Other rewritable optical technologies typically limit media to 10,000 write cycles.

The drive can also read O-ROM disks that store prerecorded information, much like CD-ROM drives do. Mass duplication of O-ROM disks uses a stamping production technology. This technology is similar to the process used to make CD-ROM disks and audio record albums. Therefore, manufacturing costs of prerecorded O-ROM disks should soon drop to less than \$2 each.

Both CD-ROM and O-ROM disks store data via pits in the physical



A 42-msec seek time and 10-msec latency spec make the OD-3000 multifunction optical drive useful in some primary-storage applications.

medium's surface. O-ROM offers some advantages compared with CD-ROM technology, however. CD-ROMs employ a long spiral track; O-ROM disks feature a format with tracks and sectors, like magnetic disks. The track-andsector configuration results in superior seek times for computer applications. O-ROM technology also leads to a third type of medium that you can use with the OD-3000. Partial-ROM disks have O-ROM and rewritable technology mixed on a single surface. Users can add their own information such as graphics to the rewritable sections of a partial-ROM disk.

The OD-3000 features a 3000-rpm rotational speed, which minimizes latency during seek operation. The drive's average rotational latency is 10 msec. The drive's optic components are in two different physical

locations to minimize seek time. The semiconductor laser, photodiode detector, lens, and prism are fixed in place away from the actuator arm. Only minimal optical components that provide focus and tracking functions reside on the actuator, resulting in a lower-mass actuator. The drive has a 42-msec seek time compared with specs greater than 60 msec for some optical drives.

Other key specs include 11W power dissipation during read/write operations and 2.6W when the drive is inactive. A Reed-Solomon error-correction scheme results in less than 1 error bit per 10¹² bits. The drive can read data continuously from disk at 640 kbytes/sec and write data continuously at 203 kbytes/sec. Write operations require the erase, write, and verify passes common to all rewritable optical drives and

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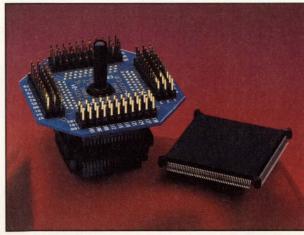
account for the slower speed. The drive features a 128-kbyte buffer on the SCSI-2 controller. The controller can transfer buffered data to the host at 2 Mbytes/sec in asynchronous mode and at 5.3 Mbytes/sec in synchronous mode. The drive's MTBF spec is 30,000 power-on hours.

The key to the acceptance of 3½-in. optical drives will eventually be price. The OD-3000 costs \$1050 (1000) and the rewritable disks cost \$60 each. The company hopes to drop the prices by 50% or more within the next 18 months.

—Maury Wright

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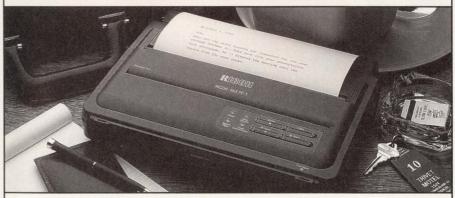
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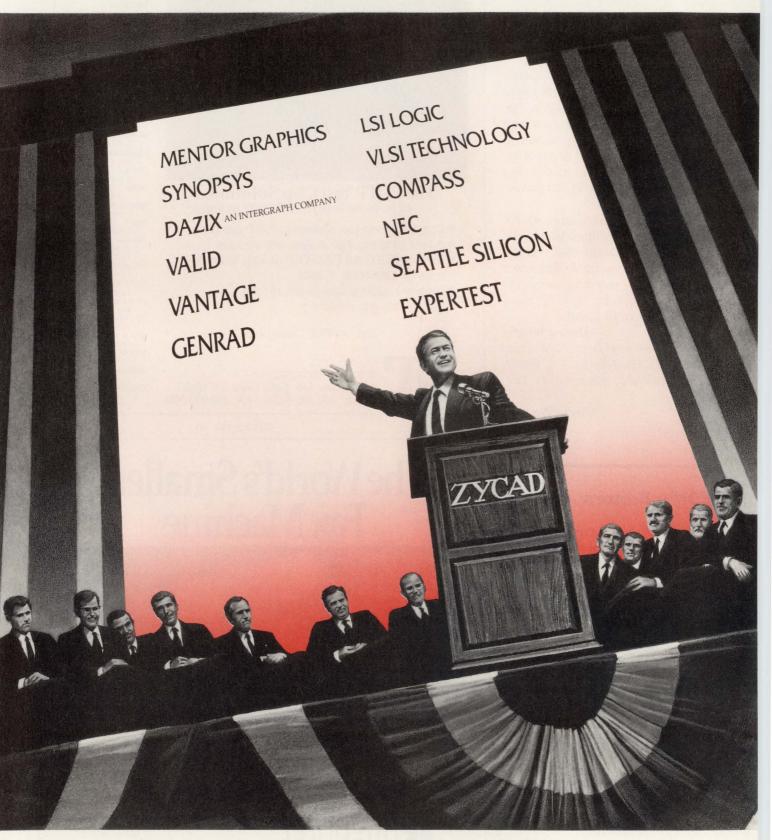
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And Who's Leading It?



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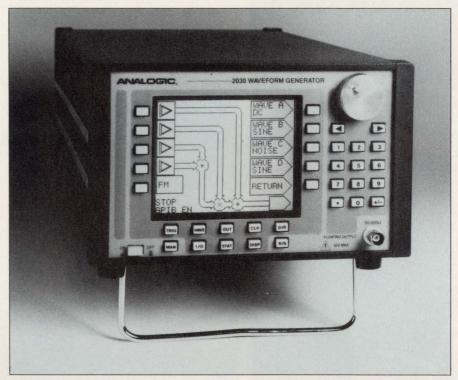


Generator owes accuracy and versatility to DSP and arbitrary-waveform technology

nalogic Corp's 2030 harnesses technology not yet widely used in function generators to make daunting waveform-generation tasks seem rather straightforward. You can set it up to produce complicated waveforms with no more difficulty than you can get classical generators to output sine, square, and triangular waves. Moreover, the waveforms that the unit produces exhibit unusually low distortion and few artifacts. The firm accomplishes this feat by using digital technology-DSP technology-and playing tricks such as predistorting the samples fed to the unit's D/A converter to compensate for sampling effects and for the inherently nonideal transient response of the anti-imaging filter that follows the DAC.

Hidden within the half-rackwidth enclosure is a Motorola 56001 DSP μP . The μP earns its keep; it executes algorithmic routines stored in ROM and fills the generator's dual-ported memory with samples that represent the output waveforms. The algorithms are much more compact than are pointby-point signal representations; therefore the generator can store an extensive waveform repertoire. If the individual waveforms stored this way don't meet your needs, you can add the waveforms to each other and multiply them by one another. Moreover, to remove artifacts that would otherwise appear, before routing the calculated waveforms to the DAC, the µP convolves them with the reciprocal of the output filter's impulse response.

This technique and other numeric



Adding and multiplying waveforms to produce even more complex waves is a snap with the block diagrams that appear on the bit-mapped, backlit LCD screen of the 2030 function generator. You make your selections using soft keys next to the screen.

sleights-of-hand let the generator produce a long list of modulated and swept-frequency waves-in addition to dc and the familiar sine, square, ramp, triangular, pulse, and pseudo-random-noise waveforms. The modulated waveforms include double-sideband AM (amplitude modulation) with full and suppressed carriers; single-sideband AM, also with full and suppressed carriers; FM (frequency modulation); phase modulation; exponentially decaying waves; the $\sin(x)/x$ function; and both linear and logarithmic sweeps.

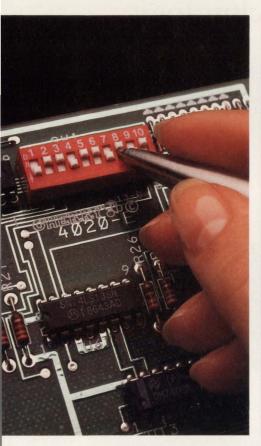
The sine-wave distortion level, although dependent on amplitude

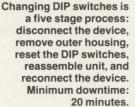
and frequency, is 80 dB below the output level at or below 100 kHz, regardless of amplitude. There are four amplitude ranges, from 10 mV to 10V full scale into an open-circuit. You can set the amplitude with 4-digit resolution, and you can select either 50Ω or 600Ω output resistance.

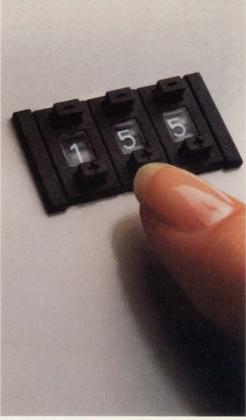
The generator's frequency range starts at 0.001 Hz and extends to 20 MHz for sine waves and to 5 MHz for pulses and for square, triangular, and ramp waves. Pulse rise time is approximately 15 nsec at and below 100 Hz; 10.0 to 10.4 µsec from 100 Hz to 1 kHz; 1 to 1.04 µsec from 1 kHz to 10 kHz; and 46

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to 50 nsec from 10 kHz to 5 MHz. Peak pulse and square-wave overshoot is 0.1% at and below 100 kHz and 0.2% above. You can set the output frequency of any waveform with a resolution of 1 part in 10⁷ (0.1 ppm).

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Because it incorporates the technology of a 12-bit-resolution arbitrary-waveform generator, the instrument can synthesize signals that are not in its library and that are not producible by manipulating the library functions. The vendor doesn't emphasize this arbitraryfunction-generation capability, however. To use it, you must load waveform-definition files from an external source, such as a PC, via the unit's IEEE-488 or RS-232C ports. The generator includes both ports as standard equipment. The ports let you use terse commands to recall any of 15 complete setups from nonvolatile memory. You can retrieve the setups manually by pressing a few keys. The unit costs \$3995.

—Dan Strassberg

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PRODUCT UPDATE

Raster image-accelerator IC renders fonts in real time

The D7001 IC renders outline fonts in real time for graphics display and printer applications. The device is the first IC in the company's RIDA (raster image device accelerator) family of ICs that accelerate the rendering of graphic objects. It can produce outline fonts scaled to any size fast enough for laser printers to print at speeds of 17 pages/minute and slower. The IC can also be used in mother board graphics applications to directly drive WYSIWYG display and printer engines.

The IC accepts Bezier curves, B-spline curves, and vectors. You can use the chip in Truetype, Post-script, and Intellifont page-description-language applications. Multiple filling algorithms handle both Roman characters and Kanji glyphs, and on-chip hardware compensates for pixel dropouts—a key feature for Kanji applications in which slight changes affect the meaning of glyphs. Scaling capabilities enable the chip to produce fonts ranging in size from 0.25 to 999.99 points.

Currently, most display and printer controllers use software or

firmware to render fonts. The D7001 provides 1000-to-1 font-rendering acceleration compared with firmware- and software-based designs. The IC treats outline fonts as objects rather than using graphics primitives.

The IC uses on-chip parallel processors with pipelined hard-wired instruction sets (Fig 1). When producing 300-dpi-resolution fonts at 12 points, the IC can render more than 7500 cps. Such a speed lets you implement a printer controller without the traditional 1- or multiple-line font cache. In fact, the IC can essentially render fonts in real time and requires only an 8-kbyte single-character font cache.

The D7001 comes in a 144-pin quad flatpack. Samples cost \$35. Expect production quantities to be available by year's end for \$25 (1000). The company hopes to offer a companion IC next year that can accelerate the drawing of graphic images.—Maury Wright

Destiny Technology Corp, 300 Montague Expressway, Suite 150, Milpitas, CA 95035, (408) 262-9400, FAX (408) 262-0221.

Circle No. 730

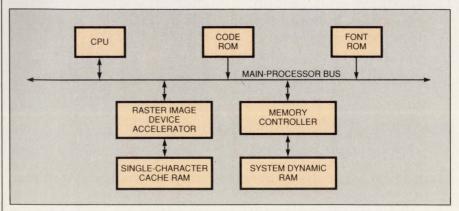
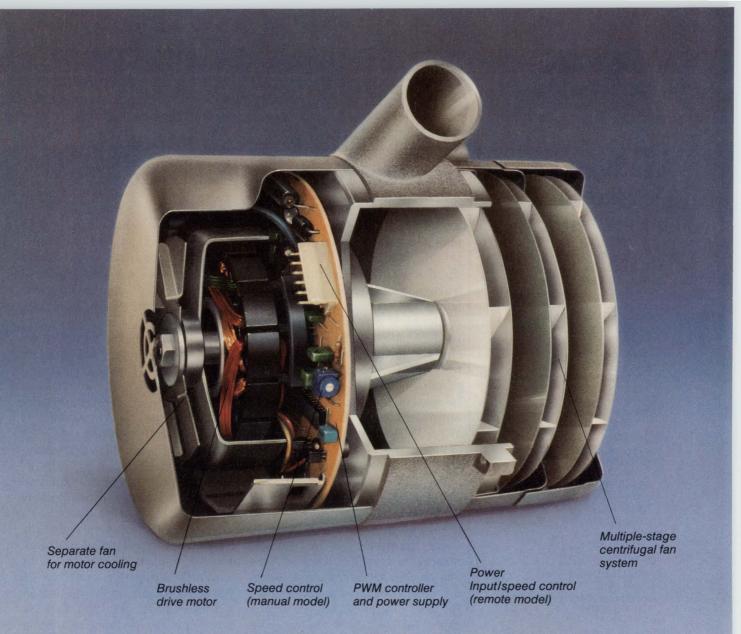


Fig 1—A parallel-processor architecture lets the D7001 render outline fonts in sizes ranging from 0.25 to 999.99 points. The IC can keep up with 17-page/minute printers and requires only a single-character font cache.



Now, high performance vacuum/pressure blowers that operate from 120 VAC

Compact units feature brushless dc motors with integral controller and variable speed capability

These new Windjammer® blowers combine electronics, motor, and fan system in a compact, costeffective package that operates from a standard 120 VAC input. An exclusive Lamb Electric design, they were developed from demanding, limited space applications such as business machines, medical equipment and materials



handling applications.

Just 5.7" in diameter, the blowers have 1-, 2-, or 3-stage fans for performance from 75" H₂O vacuum at 0 CFM to 125 CFM at 0" H₂O. With one version, a 0 to 10 VDC signal

from a sensor or other device will control motor speed and adjust air performance from 0 to 100%. Or, a second model provides manual speed control by means of a potentiometer located in the blower housing.

These blowers also feature low noise performance and are UL/CSA component recognized. Get complete details by contacting AMETEK, Lamb Electric Division, 627 Lake Street, Kent, OH 44240. (216) 673-3451. Fax: 216-673-8994. Telex: 433-2140. Cable: LAMETEK.

AMETEK

IC tester offers 200-MHz testing for analytical applications

The Logic Master ATS test station provides characterization of new chips, failure analysis, quality assurance, and low-volume production tests for devices requiring clock rates as high as 200 MHz. Proper device characterization requires clock rates and accuracy comparable to a production tester.

Although production testers can perform characterization and other applications, they often have two drawbacks. First, they are expensive—the demand for high clock rates, high accuracy, and high throughput place requirements on production test systems that are difficult to achieve at any price. Because the high throughput capability of a production tester is not used during characterization, the cost of a production tester is difficult to justify. Second, because production test-system software is designed for test engineers, it's not always easy for a design engineer to use when evaluating a new chip design.

This test station is priced at \$2600 to \$3200 per pin. It offers 200-

MHz clock rates without multiplexing channels and data rates as high as 400 Mbits/sec. Standard system accuracy is ± 500 psec. The system has 50-psec edge-placement resolution and ± 100 -psec stability and linearity, allowing you to fine-tune the calibration for special applications.

The test system uses the highest performance for the pin drivers and uses custom GaAs drivers and receivers. Other parts of the tester use ECL standard-cell devices, CMOS gate arrays, and FPGAs.

The GaAs drivers let you program driver rise and fall times between 1 and 3 nsec for 5V swings. For 600-mV signal swings, the rise and fall times are programmable from 500 psec to 1 nsec. Each driver and comparator is independent and can have its own drive and compare levels set with 10-mV resolution between -1.5 and +6.5V for drive high and -2.5 and +4.5V for drive low. Dual threshold comparators let you perform timing-window comparisons.

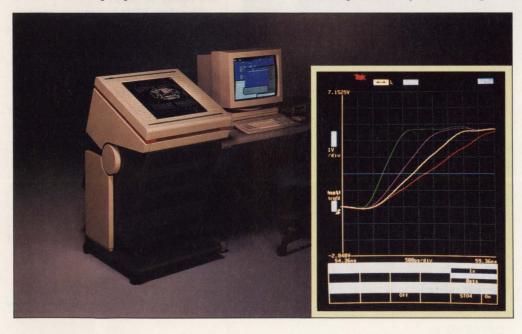
The tester also provides dynamic

current loads for testing output pins under real-world load conditions and for testing the time required for 3-state outputs to switch to their high-impedance state. Two optional parametric measurement units (PMUs) are available for the tester. One is a "per-pin" PMU that uses comparators to test voltage or current levels to programmed limits. The other PMU analyzes and measures absolute current or voltage levels.

The tester operates with dual formats for channels running at twice the clock or data rate of other channels. This feature is useful when you need to test microprocessors and other devices with multiple phase clocks.

The system is hosted by a Sun workstation and has an Ethernet port for network operation. A 502-Mbyte hard disk is standard.

Software included with the tester provides simulator pattern conversion, system setup, pattern generation, and graphical waveform editing. The system has built-in soft-



As many as 448 channels of 200-MHz testing is possible with the Logic Master ATS. The drivers have programmable slew rates so you can use the optimum value for your test setup.



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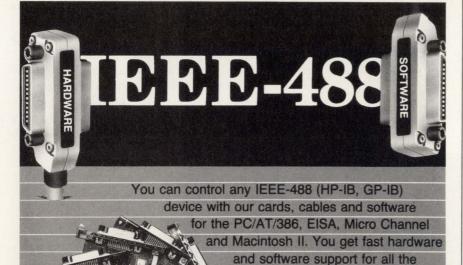
UPDATE

ware for measuring standard device parameters such as setup, hold, and propagation-delay times. Software is also available for translating test programs written for mainframe testers.

The test station is available in two versions. The ATS 1 supports 16 to 224 I/O channels and has 12 timing generators providing 24 timing edges. The ATS 2 supports 16 to 448 I/O channels and has 24 timing generators. Each channel in either system can select timing edges from 12 timing generators. A 128-I/O-channel system with 128k-deep pattern memory costs \$360,000.—Doug Conner

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JUST ASK

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	Min	N	lax	Units												
Continuous Input Current (I _{IN})	10 50		10 50		10 50		10 50		10 50		10 50		50	mA _{DC}		
Input Current (Guaranteed On)	10			mA _{DC}												
Input Current (Guaranteed Off)		1	00	μA _{DC}												
Input Voltage Drop at (I _{IN}) = 25mA		3.	.25	V _{DC}												
(-55° to	+ 105° unless	otherwise no	FB00KB	Units												
	,	·		Units												
Part Number Bidirectional Load Current (I _{LOAD})	,	·		Units A _{DC} /A _{PK}												
Part Number Bidirectional Load Current (I _{LOAD}) DC Load Current (I _{LOAD})	FB00CD	FB00FC	FB00KB													
Part Number Bidirectional Load Current (I _{LOAD}) DC Load Current (I _{LOAD}) Bidirectional Load Voltage (V _{LOAD})	FB00CD ±1.0	FB00FC ±0.50	FB00KB ±0.25	A _{DC} /A _{PK}												
Part Number Bidirectional Load Current (I _{LOAD}) DC Load Current (I _{LOAD}) Bidirectional Load Voltage (V _{LOAD})	#1.0 2.0	#0.50 1.0	#0.25 0.5	A _{DC} /A _{PK}												
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	#1.0 2.0 ±80 80	#80 FB00FC ±0.50 1.0 ±180 180	### ##################################	A _{DC} /A _{PK} A _{DC} V _{DC} /V _{PK} V _{DC}												

Notes: 1. A series resistor is required to limit continuous input current to 50mA (peak current can be higher).

2. Rated input current is 25mA for all tests.

3. Loads may be connected to any output terminal.
4.ON resistance shown is for the bidirectional configuration. The DC ON resistance is 1/4 of these values

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FDDI.

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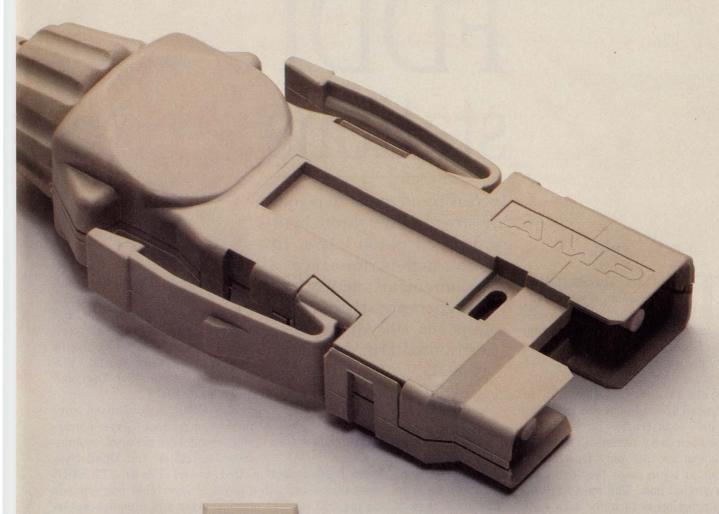
The X3T9.5 Task Group, under the procedures of ANSI Accredited Standards Committee X3, has reaffirmed approval of the Media Interface Connector (MIC) for the proposed FDDI (Fiber Distributed Data Interface) Physical Layer Medium Dependent (PMD) document.

More good news! AMP has the complete fiber optic interconnection system—the AMP OPTIMATE Fixed Shroud Duplex System—that meets all FDDI PMD requirements. And includes all the physical components you need to make your fiber optic network a reality.

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THIS IS AMP TODAY.



FDDI stations

Increasing network demands are straining the throughput of first-generation LANs. To meet high-performance requirements, network designers are starting to adopt the 100-Mbps Fiber Distributed Data Interface (FDDI). Unfortunately, FDDI stations don't

John Gallant, Associate Editor

come cheap.

ocal-area networks (LANs) are becoming as congested as our nation's highways. Packet data traveling on Ethernet LANs must share a single 10-Mbps pathway. Packet data on a Token Ring LAN migrate at 4 or 16 Mbps. These posted speed limits can cause severe data-traffic jams during peak activity periods. The slow-downs are not only frustrating,

but in some cases they can bring network activity to a virtual halt. The most expedient option to alleviate congestion is to move data faster—an option that, if employed in highway management, would have disastrous consequences.

In 1982, the X3T9.5 committee of the American National Standards Institute (ANSI) recognized these impending logjams and set about defining a set of protocols that lets packet data whiz over a LAN at 100 Mbps. This super highway is the Fiber Distributed Data Interface (FDDI). The ANSI X3T9.5 standard for FDDI defines a dual counter-rotating ring LAN that uses a fiber-optic medium and a token-passing protocol. (For definitions of FDDI terms, see box, "Glossary of FDDI terms.")

An FDDI LAN can stretch 100 km and connect more than 500 nodes spaced by as much as 2 km. In contrast, first-generation LANs such as Ethernet, defined by IEEE standard 802.3, and Token Ring, defined by IEEE standard 802.5, operate over a more limited distance. Ethernet can stretch only 2.5 km and connect as many as 1024 nodes spaced by as much as 0.5 km. Token Ring can stretch only 1.2 km and connect as many as 96 nodes spaced by as much as 0.46 km. FDDI's long distance specification coupled with its 100-Mbps data transmission rate make it suitable as a fast-

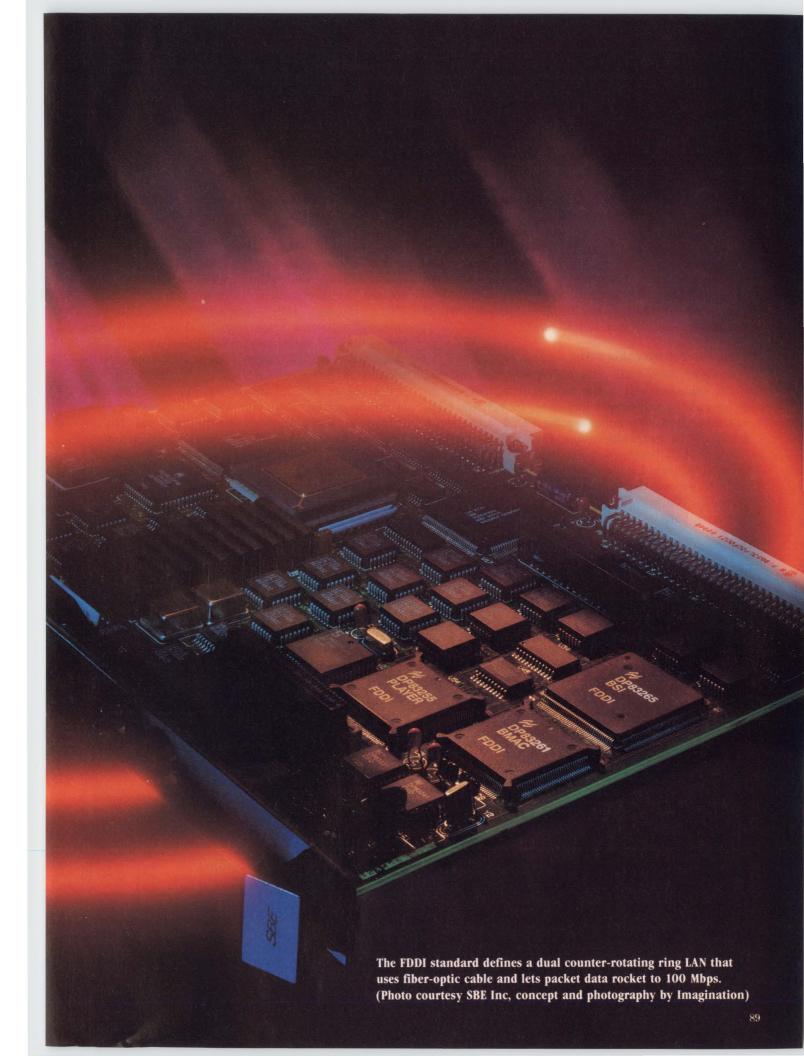
throughput backbone that can transport data between existing LANs via gateways, bridges, and routers (Fig 1). Any network manager who is experiencing or projecting network traffic overloads should consider the pros and cons of FDDI.

The FDDI specification conforms to a general, 7-layer hierarchical model for network communications called the Open Sys-

tems Interconnection (OSI) model (Fig 2). The FDDI spec describes both a physical layer that corresponds to the OSI model's physical layer and a media-accesscontrol (MAC) sublayer that corresponds to the lower half of the OSI model's data-link layer. The spec also describes a Station Management (SMT) network supervisory function, which falls outside of the OSI model. The SMT function is implemented in software. This software resides on each station of the ring and creates logical paths between the physical layer and the MAC sublayer to permit SMT-to-SMT communications between stations. SMT software connects and disconnects the station to the ring, monitors network operations for reporting status to the host computer, isolates network faults, and detects conditions such as duplicate addresses that would inhibit ring operation.

Realizing that there would be considerable discussion about the types of fiber, connectors, and other interconnect hardware, the ANSI X3T9.5 committee decided to break the specification for the OSI physical layer into two sublayers—the Physical Medium Dependent (PMD) sublayer and the Physical (PHY) sublayer. The lower of the two sublayers, PMD, specifies the transmission wavelength to be 1300 nm. Both LEDs and lasers can emit light of this wavelength.

The PMD sublayer spec recommends 62.5/125-µm



The ANSI X3T9.5 FDDI standard defines a dual counter-rotating ring LAN that uses a fiber-optic medium and a token-passing protocol.

(core diameter/cladding diameter) multimode cable and has advice on using 50/125-, 85/125-, and 100/140- μm cable. The dispersion in multimode 62.5/125 micron cable is small enough to ensure FDDI's $10^{\text{-9}}$ bit error rate. Debate continues over cable size. The PMD document is written so that any size cable capable of 1300-nm transmission conforms to the FDDI standard as long as the cable also meets the optical power, channel bandwidth, and distance requirements.

Trying to reduce cable costs

However, fiber-optic cable isn't cheap, and the cost of the cable, as well as the light-emitting source, increases as the wavelength increases. In fact, the high-cost associated with implementing FDDI is the major drawback to its proliferation. Codenoll Technology Corp, an FDDI-node-controller vendor, has proposed using an 830-nm LED emitter and 830-nm multimode cable to reduce the high materials cost of an FDDI network. The wavelength does not meet the FDDI standard, but the company claims that the only effect

of the wavelength change is the shortening of the maximum allowable distance between nodes from 2 to 0.5 km.

A working group of the ANSI X3T9.5 committee is trying to lower FDDI costs by developing a PMD spec that uses less-expensive shielded twisted-pair (STP) copper wire as the medium while maintaining FDDI speeds. The specification would specify a much shorter distance between nodes—probably less than 100 m—and replace optical transceivers and connectors with lower-cost STP connectors. STP is also attractive because many facilities already have STP copper wire installed for Ethernet LANs.

Because an ANSI standard for STP communication is not expected until late 1992, five companies—Advanced Micro Devices, Chipcom Corp, Digital Equipment Corp, Motorola Inc, and Synoptics Communications Inc—recently defined and published an STP standard for 100-Mbps data. Products conforming to this standard, which is open for public use, will be able to communicate with each other.

Copper wire costs much less than fiber cable, but

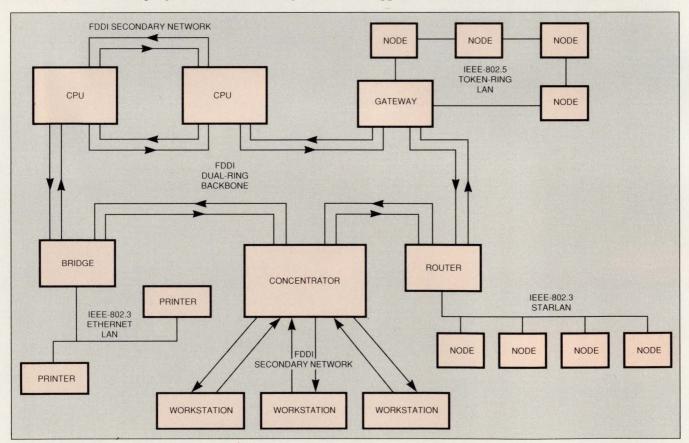


Fig 1-A 100-Mbps FDDI backbone can interconnect multiple disparate LANs using gateways, bridges, and routers.

metal-based networks are susceptible to electromagnetic interference and are less secure than fiber-optic communications—two of FDDI's big pluses. In addition, because FDDI's ring topology demands that each station operate as a repeater, nonstandard PMD implementations can't be used on the FDDI backbone.

Group encoding limits bandwidth

PHY, the upper sublayer of FDDI's physical-layer specification, defines a 4B/5B group-encoding scheme for representing 4-bit data and control symbols. The scheme doesn't use Manchester encoding, which is typical of other LAN protocols. Manchester encoding would require a 200-MHz clock to transmit 100-Mbps data. The 4B/5B group-encoding scheme requires the transmission of a 5-bit code word for each 4-bit symbol, thereby achieving a 125-Mbps rate. The code word is converted to a nonreturn-to-zero-inverted (NRZI) signal for network transmission. The PHY sublayer also defines how to decode the 4B/5B NRZI signal from the network into symbols that the station can recognize.

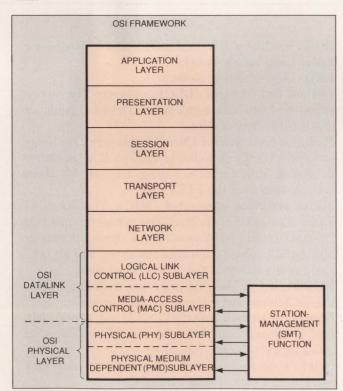


Fig 2—The FDDI specification defines three sublayers that correspond to the data-link and physical layers of the 7-layer OSI model. FDDI also specifies an SMT function, which supervises sublayer and ringmanagement operations.



FDDI specifies a media interface connector (MIC) to attach a station to the dual ring. Formation Inc's Fibernet fv1000 node controller for the VMEbus has two MIC connectors. The controller can operate as :1 dual- or single-attachment station.

Because an NRZI signal has no transitions when all zeros are present in the data, the 4B/5B encoding scheme guarantees that data have no more than three consecutive zeros. Although the encoding scheme uses less bandwidth than Manchester encoding, clock recovery is more difficult. Therefore, instead of using one master clock to generate data as the IEEE 802 standards specify, PHY sublayer specifies that each station in the FDDI ring regenerate the data with a frequency-stable reference to prevent frequency-jitter from accumulating around the ring. Each station has a phase-locked loop, which clocks the received data into an accordion buffer, and a crystal-controlled frequency source, which clocks the data out of the buffer.

MAC sublayer delivers frames

The FDDI media-access-control (MAC) sublayer defines the token-passing protocol for data transmission over the ring. The MAC spec defines packet-frame fields such as headers, trailers, addresses, and cyclic redundancy checking (CRC). An FDDI information-packet frame comprises a preamble having 16 or more IDLE (5-bit group code of all 1s) symbols, a 2-symbol

The PHY sublayer must decode a 4B/5B NRZI signal from the network into symbols a station can recognize.

start-of-frame field, a 2-symbol frame-control field that identifies the packet type, a 16- or 48-bit destination address, a 16- or 48-bit source address, the information field, a 32-bit CRC field, a 1-symbol end-of-frame field, and a frame-status field. The maximum packet size is 4500 octets. (Ethernet has 1514 octets max, and Token Ring has 8191 octets max.)

Stations wanting to transmit data over the ring must first obtain a unique 6-symbol token. The Timed Token Rotation (TTR) protocol requires each station to measure the time elapsed since it last received this token. An initialization procedure guarantees fairness by establishing a target token-rotation time (TTRT) that each station must observe. When a station has the token, it can transmit synchronous data during the TTRT. If the next station receives the token before the previous station's TTRT expires, the station can transmit frames asynchronously during the leftover time.

The MAC sublayer is responsible for controlling the flow of data. Each station's MAC sublayer monitors a

packet's destination address, copies the packet into the station's memory if the packet is addressed to the station, and then relays the packet to the next station on the ring. The sending station's MAC sublayer deletes the packet once it comes full circle.

Chip set implements FDDI sublayers

Three vendors currently offer chip sets that implement the FDDI MAC and PHY sublayers—Advanced Micro Devices, National Semiconductor, and Motorola. These chip sets interface directly to the logical-link-control (LLC) sublayer of the OSI model's data-link layer. All vendors offering stations that connect to an FDDI network employ one of these chip sets. The stations implement the SMT functions in software or firmware. Most stations employ the media interface connector (MIC) defined in the FDDI PMD specification. The MIC is a shrouded fiber-optic coupling in which a male plug terminates the cable and a female receptacle resides on the FDDI module. Some stations employ an ST connector to reduce cost. The ST connec-

Glossary of FDDI terms

ANSI: American National Standards Institute.

Backbone network: A primary network that interconnects two or more secondary networks via gateways, bridges, and concentrators.

BNC: Baby n connector.

bps: Bits per second.

Concentrator: A node on the FDDI ring that provides connections for multiple FDDI stations to communicate with other stations on the dual ring.

Connection management (CMT): That portion of the SMT software that controls station insertion and removal as well as the connection of a station's PHY and MAC sublayers.

CRC: Cyclic redundancy checking.

Data-link layer: The OSI layer that implements data transfer between two stations on an FDDI network.

Dual-attachment station (DAS): A station that provides two physical attachments to accommodate the dual counter-rotating FDDI ring.

Fiber Distributed Data Interface (FDDI): A standard for a 100-Mbps token-ring LAN based on a fiber-optic medium. The ANSI X3T9.5 standard employs a dual counter-rotating ring, which provides fault tolerance. FDDI conforms to the OSI model.

IEEE: Institute of Electrical and Electronics Engineers.

LAN: Local-area network. LED: Light-emitting diode.

Logical link control (LLC) sublayer: The upper sublayer of OSI's data-link layer. The LLC sublayer controls the flow of data.

Media access control (MAC) sublayer: The lower sublayer of OSI's data-link layer. The MAC sublayer is responsible for scheduling frames for data transmission over the FDDI ring.

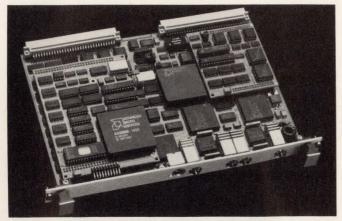
Media interface connector (MIC): The specified FDDI fiber-optic connector. The connector has two 2.5-mm ceramic ferrules within a shrouded assembly. An MIC plug terminates the cable, and an MIC receptacle resides on the FDDI attachment.

Network layer: The OSI layer responsible for routing, switching, and internetworking access.

Nonreturn to zero inverted (NRZI): A signal code that represents a logical 1 by a polarity transition and a logical 0 by no transition.

Octet: A data unit comprising eight bits. An octet represents a pair of data symbols.

Open Systems Interconnection (OSI) model: A general, 7-layer model that defines a hierarchy of services necessary to exchange information between



You can configure some FDDI node controllers, such as the V/FDDI 4211 Peregrine board for the VMEbus, as single- or dual-attachment stations. The Interphase Corp board uses the Advanced Micro Devices FDDI chip set.

tor is a spring-loaded twist-and-lock coupling similar to a BNC connector.

FDDI permits two types of stations: Class A and Class B. Class A stations are dual-attachment stations (DAS), which have dual physical layers that connect to the primary and secondary rings in FDDI's dual counter-rotating ring topology. All the stations attached to the FDDI's dual-ring backbone must be Class A stations. A Class A station on the dual-ring backbone

can function in one of three ways: as a node controller that adapts a computer or peripheral to the ring, as a concentrator that acts as the hub of a star topology when connecting multiple FDDI stations to the ring, or as an internetworking module, such as a gateway, bridge, or router. Class B stations are single-attachment stations (SAS) and have a single physical layer. They attach to a concentrator's SAS port (Fig 3) and can be node controllers or internetworking modules.

Although the FDDI specification doesn't prohibit Class A stations from transmitting data on both the primary and the secondary ring, this mode of operation isn't wise. Theoretically, you could double the data-transmission rate to 200 Mbps by using both rings, but you would defeat one of FDDI's most attractive features. FDDI's secondary ring is meant to provide fault tolerance, which is a critical need in high-performance applications. If a fault occurs in the primary ring, the SMT ring-management protocol recognizes that the TTRT is violated and notifies the network manager. The SMT software isolates the fault

computers. The International Organization for Standardization (ISO) defined the model in 1979 as a framework for defining network protocols.

PC: Personal computer.

Physical (PHY) sublayer: FDDI's upper sublayer that corresponds to the OSI model's physical layer. This sublayer is responsible for delivering symbols from the MAC sublayer to the FDDI network.

Physical layer: The OSI layer that permits the physical connection of a station to a LAN.

Physical Medium Dependent (PMD) layer: FDDI's lower sublayer that corresponds to OSI's physical layer. The PMD sublayer specifies optical power, cable specifications, the MIC connector, and optical bypassing.

RAM: Random-access memory.

Ring management (RMT): That portion of the SMT software that manages a station's MAC sublayer. RMT software detects faults, such as duplicate addresses, at the MAC layer.

Shielded twisted pair (STP): Describes copper wire commonly used in LANs.

Simple Network Management Protocol (SNMP): Software for managing a TCP/IP network.

Single-attachment station (SAS): A station that

offers one attachment to an FDDI network. **Station:** An addressable node on an FDDI network that is capable of transmitting, repeating, and receiving information.

Station management (SMT): Describes the supervisory software that monitors an FDDI station and controls station activity.

ST connector: A fiber-optic connector employed in many fiber-optic LANs. The AT&T connector contains a ceramic ferrule encased in a twist-and-lock assembly similar to a BNC connector.

Target token-rotation time (TTRT): The maximum time an FDDI station has to transmit data on the ring. The TTRT is established by the lowest bidding station during an initialization process.

TCP/IP: The US Department of Defense's Arpanet suite of protocols for implementing the transport and network layers of the OSI model.

Token: A unique 6-symbol frame that circulates around the FDDI ring. A station must have the token to transmit data.

4B/5B: The symbol encoding method specified by the FDDI standard in which each set of four bits is encoded as five bits.

and wraps the upstream primary ring into the downstream secondary ring to reconstruct a ring network.

Multiple failures on the ring can segment the network. In these rare cases, the network manager may have another ring-reconstruction option at his or her disposal. The PMD specification provides for an optional optical bypass switch that can be activated to bypass a Class A station completely. Activating the optical bypass switch would let the network manager service the faulty station off line.

FDDI stations can be node controllers, concentrators, or internetworking modules. Node controllers are adapter boards for popular computer buses, such as the ISA bus, VMEbus, and Multibus (Table 1). One of the three commercially available FDDI chip sets provides the PHY and MAC sublayers for the station. The board's PMD hardware determines whether the node controller is an SAS or a DAS. A node controller generally has a microprocessor unit and enough RAM to run the LLC sublayer and offload communications tasks from the host computer.

Some node controllers contain EPROM for SMT

firmware; others download the SMT software into the onboard RAM. All of these boards communicate with the host at the network layer of the OSI model. Although the ANSI committee has not yet drafted protocols for the network layer, the TCP/IP suite of protocols is the most popular method for transferring files. FDDI node controllers support other network-layer protocols as well.

Concentrators play a crucial role in an FDDI network by letting you connect multiple stations to an FDDI backbone via one DAS port (**Table 2**). FDDI defines four types of concentrator ports: A, B, S, and M ports. The A and B ports provide the DAS connection to the dual ring. The M (master) and S (slave) ports let you cascade concentrators and SAS stations in tree topologies. A concentrator can have as many as 255 M ports. These ports can connect to the primary or secondary FDDI ring or to an S port on another concentrator.

Concentrators are either computer bus boards or stand-alone chassis containing expansion boards. Because a concentrator is a critical link for connecting

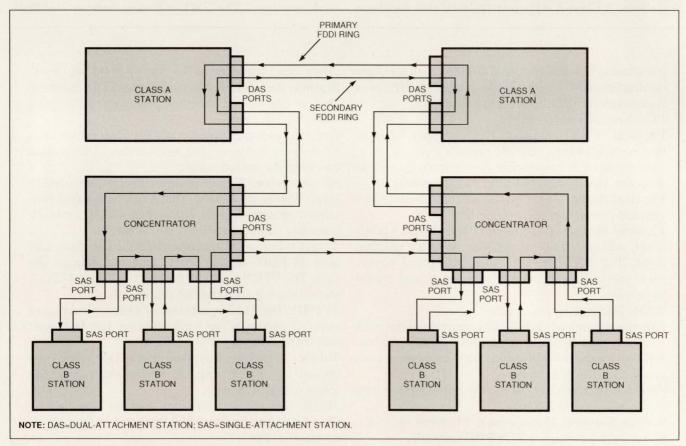


Fig 3—You can attach multiple Class B stations to an FDDI dual ring by using a concentrator. Class A stations have dual-attachment-station (DAS) ports, which connect directly to the dual ring.

Table 1—Representative FDDI node controllers

Company	Model	Computer Bus	Protocol support	Micro- processor unit	FDDI chip set	Connector type	Power	RAM buffer	Inter- operability tests ¹	Price	Features
CMC	1150 Series	VMEbus (6U)	TCP/IP (onboard SMT firmware)	Am29000	AT&T (PHY), AMD (MAC), CMC (LLC)	ST (SAS or DAS)	32.5W	2 Mbytes	ANTC	\$11,245 to \$11,955	Link-level firmware interfaces to host-based TCP/IP. Micr processor unit can implement network and transport-layer protocols on board Integrated SMT an SNMP software.
	1050 Series	VMEbus (9U)	TCP/IP (onboard SMT firmware)	Am29000	AMD	ST (SAS or DAS)	140W	1 Mbyte	ANTC, UNH	\$8950 to \$9950	Integrated SMT and SNMP software. Link-level firmware interfaces to host- based TCP/IP.
Codenoll Technology Corp	Code- net- 9540	EISA or ISA bus	TCP/IP	None	AMD	MIC (SAS)	10W	128 kbytes	None	\$4995	Optional support for 830-nm fiber. Option bypass switch support.
	Code- net- 9543	EISA or ISA bus	TCP/IP	None	AMD	MIC (DAS)	15W	128 kbytes	None	\$7495	Optional support fo 830-nm fiber. Optio bypass switch support.
Concurrent Technologies	CL 386/ DAS	Multibus II (6U)	TCP/IP (end of 1991) (onboard SMT firmware)	80386	AMD	MIC (DAS)	45W	4 Mbytes	None	\$7140 (100)	Optical bypass control. Two RS- 232C serial ports.
CXI	CX- MBII	Multibus II (6U)	GOSIP, TCP/IP (onboard SMT firmware)	80386	AMD	MIC (DAS)	NA ²	4 Mbytes	NA	\$11,280 to \$12,280	Optical bypass control. Implement Intel's iNA 960 Ne working software.
Digital Equipment Corp	FDDI Con- troller 400	XMI bus	XTP, TCP/IP (onboard SMT firmware)	68020	Digital (licensed to AMD and Motorola)	MIC (SAS)	65W	1 Mbyte	ANTC, UNH	\$19,900	Operates in VAX 6000 and VAX 900 computers.
	FDDI Con- troller 700	Turbo Channel bus	TCP/IP (onboard SMT firmware)	68000	Digital (licensed to AMD and Motorola)	ST, BNC (SAS)	20W	1 Mbyte	ANTC, UNH	\$4500 to \$6000	Operates in VAX 6000 and VAX 900 computers. Board supports shielded twisted-pair connections.
Formation Inc	Fiber- net fv1000	VME bus (6U)	TCP/IP (onboard SMT firmware)	Am29000	AMD	MIC (SAS or DAS)	35W	2 Mbytes	ANTC	\$8500 (SAS) \$9500 (DAS)	Optical bypass control. VRTX operating system. Optional Sun OS drivers.
Interphase Corp	M/ FDDI 2211	Multibus I	SNMP, TCP/IP, XTP (onboard SMT firmware)	Am29000	AMD	ST BNC (SAS or DAS)	42.5W	1.0 Mbytes	ANTC, UNH	\$8995 (SAS) \$10,995 (DAS)	Connection for dua PHY and dual MAG operation using tw boards. Board supports shielded twisted-pair copper wire.
	V/ FDDI 4211 Pere- grine	VMEbus (6U or 9U)	SNMP, TCP/IP, XTP (onboard SMT firmware)	Am29000	AMD	ST BNC (SAS or DAS)	NA	1.0 Mbytes	ANTC, UNH	\$8995 (SAS) \$10,995 (DAS)	Connection for dua PHY and dual MAG operation using tw boards. Board supports shielded twisted-pair copper wire.
SBE Inc	VCOM 100	VMEbus (6U)	TCP/IP, XTP (onboard SMT firmware)	68030	National Semicon- ductor	ST (SAS)	32.5W	4 Mbytes	ANTC	\$4500 (100)	Runs Synernetics' implementation of SMT. Two RS-232 serial ports. An optional mezzanine board provides DA operation.
Summit Microsystems Corp	smFd- AT201	ISA bus	Onboard SMT firmware	None	AMD	ST (DAS)	10W	128 kbytes	ANTC	\$5950	Host-to-RAM block transfer rate is 3.0 Mbytes/sec (sustained).

Notes: 1. ANTC=Advanced Networking Test Center; UNH=University of New Hampshire.
2. NA=not applicable.
3. See box, "Glossary of FDDI terms," for definitions of other abbreviations.

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multiple stations to the ring, some concentrators have fault-tolerant power supplies and let you insert and remove boards on the backplane while the power is on—a process called live insertion. In addition to the FDDI PMD, PHY, and MAC sublayers and the SMT function, concentrators also provide the Simple Network Management Protocol (SNMP) software for managing a TCP/IP network.

Internetworking modules let you integrate multiple disparate LANs onto an FDDI backbone—in effect creating a hybrid network (**Table 3**). A bridge is the

oldest method for transparently interconnecting two networks. Bridges communicate at the data-link layer of the OSI model. An FDDI bridge reads each destination field in an FDDI frame to infer a destination address for the frame. By comparing this information with an address table, the bridge determines whether to ignore the frame or forward it to a station on an interconnected network.

Routers operate at the network layer of the OSI model. Routers forward data packets not based on the destination address but according to a network identi-

Table 2—Representative FDDI cond	centrators
----------------------------------	------------

Company	Model	Housing	Fault- tolerant power supply	Live insertion	Protocol support	Number of ports (max)	Power	Connector type	Inter- operability tests	Price	Features
Codenoll Technology Corp	Codenet- 9041	EISA or ISA bus boards	No	No	SNMP, TCP/IP	12	10W	MIC (SAS or DAS); ST optional	No	\$1995 (soft- ware); \$2795 (1-port card); \$4995 (2-port card)	Optional support for 830-nm fiber. Runs on VRTX software.
Digital Equipment Corp	DEC concen- trator 500	Standalone chassis	Yes	No	Protocol independent	18	120W (AC power)	MIC FC/PC, ST, BNC (DAS)	ANTC, UNH	\$9000 to \$52,500	Supports shielded twisted pair and thinwire.
Interphase Corp	Fiber hub 800	Standalone chassis	Yes	Yes	SNMP	8	NA	MIC (SAS or DAS)	No	From \$12,000	Supports shielded twisted-pair and 830-nm fiber.
Network Systems Corp	FDDI concen- trator	Standalone chassis	No	No	SNMP	16	150W	MIC or ST	ANTC	\$3000 (chassis and mother- board) \$2200 (2-port board)	Optional optical- bypass switch.
Summit Microsystems Corp	smFD- AT301	ISA bus boards	No	NA	Onboard SMT firmware	12M ports, 2 DAS ports	10W	ST	ANTC	\$12,900 (DAS plus four M ports); \$6950 (4-M-port card)	
Synoptics Communica- tions Inc	3000-05	Standalone chassis	Optional	Yes	SNMP (on- board SMT firmware)	40 SAS ports; 1 A/B port	460W supply	MIC	No	\$4495 (housing); \$14,995 (network-manage-ment module); \$7495 (4-M-port FDDI card); \$4995 (4-M-port STP card)	Backplane accepts cards for connection to FDDI, Ethernet, and Token Ring modules. Optical bypass support. Three MAC sublayers permit dual homing to identify redundant links.

Notes: 1. NA=not applicable; ANTC=Advanced Networking Test Center; UNH=University of New Hampshire.

2. See box, "Glossary of FDDI terms," for definitions of other abbreviations.

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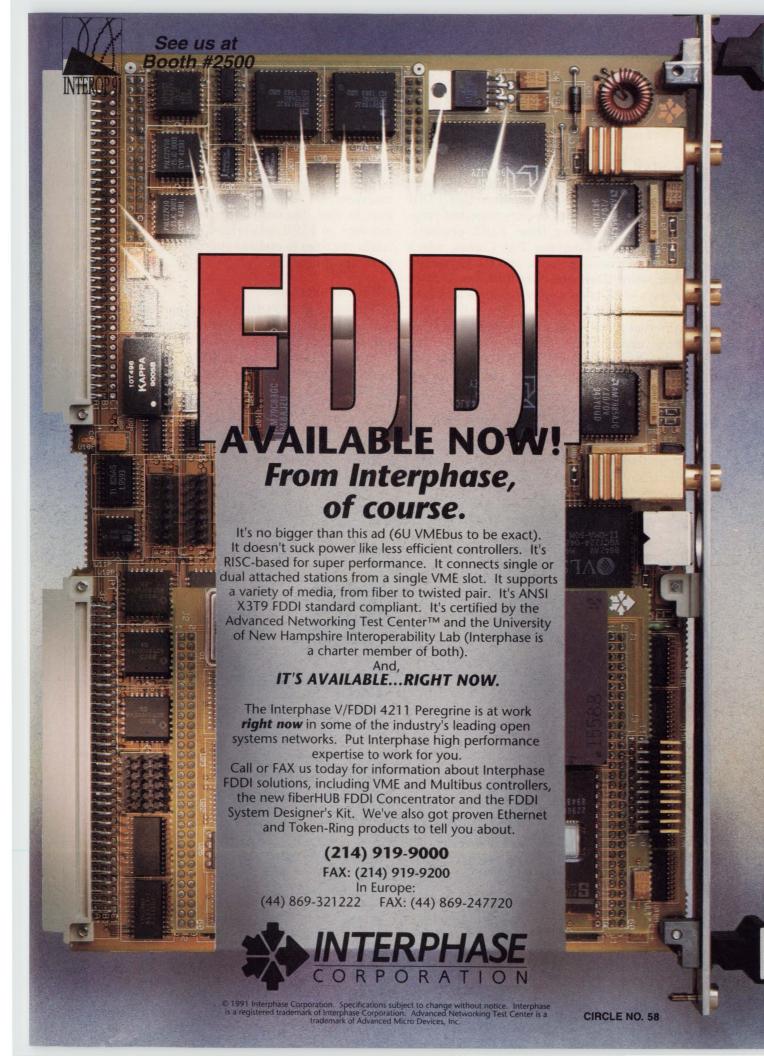
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*Propagation Delay

fier. Routers are more versatile than bridges: They also perform packet fragmentation and reassembly, packet control, and priority routing. In some cases, both bridge and router functions are appropriate for internetworking. In these cases, a hybrid bridge-router can provide routing services for two or more networklayer protocols or can implement a transparent datalink connection.

Company	Model	Product description	Network Support	Power	Inter- operability tests ¹	Price	Features
Cisco Systems Inc	AGS+	Router	Appletalk, DEC net, Novell, IPX, Token Ring, Ethernet, Cheapernet, DDN X.25, Apollo Domain, Ultranet	500W	ANTC, UNH	\$12,300	Routes 16 protocols over an FDDI network. Supports 9600-bps, 48-kbps, 56-kpbs, 64-kbps, T1, E1, and fractional T1 wide-area networks. Maximum aggregate forwarding rate is 75,000 packets/sec.
Digital Equipment Corp	DEC bridge	Bridge	Ethernet, Appletalk	390W	ANTC, UNH	\$25,000 to \$45,000	Supports dual-homing to identify redundant links. Supports Internet protocol fragmentation. Single-mode fiber option permits 40-km distance between stations.
Fibercom Inc	Ring Master 7200	Bridge	Token Ring, Ethernet, DECnet, Novell	NA ²	NA	\$15,000	Maximum forwarding rate is 20,000 packets/sec. Filtering rate is 500,000 packets/sec. Supports Internet Protocol fragmentation. Self learning for as many as 4000 addresses. Supports spanning tree algorithm.
Fibronics International Inc	FX8210	Bridge	Token Ring, Appletalk, DECnet, Novell, Ethernet	250W	ATNC, UNH	\$14,990	Down-line loadable across networks. Performs protocol-translation bridging. Comes with Interview Network Management System software.
	FX8210B Brouter	Bridge- router	Token Ring, Appletalk, DECnet, Novell, Ethernet	250W	ANTC, UNH	\$27,000	Down-line loadable across networks. Protocol- translation bridging Interview Network Management System.
In-net Corp	Fiber Talk 5000	Bridge	Token Ring, Ethernet, DECnet	360W	ANTC	\$17,500	Down-line loadable across networks. Filtering rate is 100,000 packets/sec. Forwarding rate is 6000 packets/sec.
	Fiber Talk 3000 Channel Bridging Unit	Gateway	Ethernet	360W	ANTC	\$35,000	Down-line loadable across networks. Connects an IBM 360/370 mainframe computer to an FDDI ring. Software provides Telnet Virtual Terminal, File Transfer Protocol, and Electronic Mail services.
Network Systems Corp	6400 Family	Bridge- router	Ethernet, DECnet, Appletalk, Novell, T1, T3	500W	ANTC	\$30,000	400-Mbps, 6-card backplane. Ethernet forwarding rate is 15,000 packets/sec/port. Supports the Spanning Tree Algorithm. Dynamically learns packet addresses.
	6600 Family	Bridge- router	Ethernet, DECnet, Appletalk, Novell, T1, T3	500W	ANTC	\$23,000	FDDI-to-FDDI bridge. Single-board chassis. Ethernet forwarding rate is 15,000 packets/sec/port. Supports the Spanning Tree algorithm. Dynamically learns packet addresses.
	6800 Family	Bridge- router	Ethernet, DECnet, Appletalk, Novell, T1, T3	500W	ANTC	\$46,000	Supports the Spanning Tree algorithm. Deletes undeliverable packets on the network after a preset period. Dynamically learns packet addresses. 800 Mbps, 16-card backplane.
Synernetics Inc	LANplex 5004	Bridge- concentrator	Ethernet, Token Ring	NA	ANTC, UNH	\$25,500	Backplane has three FDDI paths, three Token Ring paths, three Ethernet paths, and a VMEbus that operate in parallel. Backplane accepts four plug-in modules. Connects as many as 24 Ethernet segments to an FDDI network. Modules support line insertion.
	LANplex 5012	Bridge- concentrator	Ethernet, Token Ring	NA	ANTC, UNH	\$32,900	Backplane has three FDDI paths, three Token Ring paths, three Ethernet paths, and a VMEbus path that operate in parallel. Backplane accepts 12 plug-in modules. Connects as many as 24 Ethernet segments to an FDDI network. Modules support line

Notes: 1. ANTC=Advanced Networking Test Center; UNH=University of New Hampshire. 2. NA=not applicable.



Because FDDI is a fairly new LAN standard and multiple versions of the SMT function exist, the issue of interoperability is a concern. To ensure that FDDI stations from various vendors operate together properly, two groups are testing these FDDI products. Both the Advanced Networking Test Center, which Advanced Micro Devices sponsors, and the University of New Hampshire (Durham, NH) have test centers that run a suite of tests on vendor products they connect to an FDDI cable installation. The test centers try to ensure that there is one worldwide FDDI rather than multiple versions that don't interoperate.

If you already have an FDDI LAN installed and need an analyzer to troubleshoot the network in real

time, Digital Technology Inc offers the Lanhawk-5700 Network Analyzer family. The portable 5733 and 5732 analyzers cost \$28,300 to \$50,000 and passively couple into the ring. The analyzers monitor, analyze, and collect data on FDDI networks. They also let you collect traffic statistics to evaluate ring performance and maximize ring utilization.

Nice—but expensive

The high cost of FDDI networks necessitates a waitand-see attitude, but if projected trends for the 1990s pan out, network administrators may soon be upgrading existing LANs to the 100-Mbps standard. For example, PCs are emerging that exceed the power of

Manufacturers of FDDI products

For more information on FDDI products such as those described in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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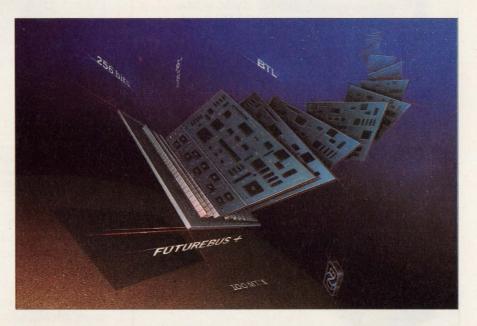
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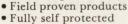


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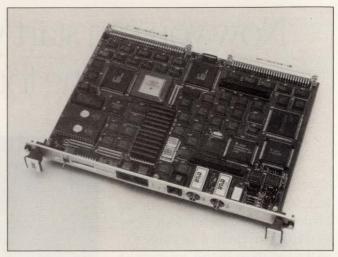
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FDDI stations



The FDDI chip set from National Semiconductor implements the VCOM-100 VMEbus node controller. The SBE Inc board has a microprocessor unit and enough dynamic RAM to execute SMT software as well as the network- and transport-layer protocols.

80386-based computers. These PCs can manage a sea of documents and images that were traditionally the province of mainframes and minicomputers. Many applications must send the images and data to multiple locations on a LAN that has insufficient bandwidth to handle such bit-heavy traffic. In addition, multimedia applications, which integrate voice, data, and video, require a bandwidth way beyond what Ethernet and Token Ring networks can offer.

Many analysts say FDDI deployment will occur in multiple stages. In the early stages, FDDI backbones will interconnect smaller token-ring LANs that employ existing STP copper wiring for horizontal distribution. In the later stages, companies having intensive graphics and CAD communications needs will invest in a full fiber-optic LAN. The attendant drop in FDDIproduct prices will encourage the widespread use of FDDI networks. EDN

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EDN'S DSP-Chip Directory

The tools needed to develop applications that use digital signal processing (DSP) continue to improve. Now, a choice of operating systems and interfaces to host operating systems is making DSP available to more applications.

David Shear, Contributing Editor

This year there are many new DSP parts that add to the array of optional word formats, peripherals, and memory sizes. Naturally these family members are created to fit an existing or perceived market. In the past, if your application didn't fit easily within an existing device, you were out of luck. Now, almost all DSP manufacturers have programs that will let you configure your own DSP $\mu P.$ You can select from the available peripherals and memory options, or you can use an ASIC approach and put a gate array on the DSP chip.

Before DSP μ Ps can move into general use, however, it is essential that the functions of the algorithm developer and the end-user-application developer are separated. It is hard enough for algorithm developers to keep up with DSP algorithm development. It is rare for them to have the luxury of maintaining expertise in the creation of end-user applications that use the latest whiz-bang graphical user interface.

Likewise, the end-user-application developer must be able to concentrate on his applications. He must not be distracted with new algorithms and DSP $\mu Ps.$ That is the algorithm-developer's domain.

Ideally, a DSP operates as if it is just another peripheral. When the end-user-application developer uses a hard disk, he doesn't have to know how the data is

stored on the disk. He just wants to use the hard-disk function: store data and retrieve it later.

Using a DSP must be the same. The algorithms must be available via a well-defined and standard method. If the end-user application needs a modem or a fax, speech or an image compressed, or whatever, the developer must be able to call the DSP as if he were sending data to a disk.

Right now, if an engineer creating an end-user application wants the application to use a DSP μ P, he must devote a significant amount of effort (and time) to create the DSP portion of the project. At the same time, he has less time to develop his product. It doesn't make sense—in terms of time and effort—for him to spend months, or more, getting up to speed in DSP.

New software interfaces

Soon, software interfaces between your DSP μP and the end-user application will let you develop DSP code that the end-user-application developer can use off the shelf. A separate group, or even a separate company, can use the DSP functions that you create. OSPA (Open-Signal Processing Architecture) from Spectron Microsystems (Santa Barbara, CA) and VCOS from AT&T are two current interfaces.

OSPA is a set of interfaces and protocols that lets

your DSP μP communicate with an end-user application. You must use the Spox real-time, multitasking operating system on the DSP μP .

Spox was introduced by Spectron Microsystems three years ago. It was first introduced to run on TI's TMS320C30. Spox has grown in acceptance to include Motorola's DSP96002, Analog Devices' ADSP-21020, and TI's TMS320C40.

Spox runs on the DSP μP while the Spox Server runs on the host. The DSP functions that you write interface to the end-user application via the Spox Server. Host- and DSP- μP independence is achieved if you create OSPA-compatible DSP programs and use the Spox server. Your DSP μP can be transported to any computer that has a Spox Server for the host operating system.

Separate the experts

David Wong, president of Spectron Microsystems, says that Spox and OSPA separate the functions of the end-user-application developer and the algorithm developer (**Fig 1**). By using high-level commands and data-stream conventions described by OSPA, you can develop the application software and the real-time DSP functions independently.

Even if the end-user application moves to another host computer, the Spox server for the new host operating system lets you transport your DSP μ P. You can also use more powerful DSP μ Ps as they become available to create more capable DSP solutions. The end-user-application developer will then be able to use the more capable DSP solution without modifying his code.

The near industry-wide acceptance of OSPA and Spox places them in a great place to become the standard. The host independence of OSPA and the DSP-µP independence of Spox further strengthens their positions.

VCOS is another approach to separate your efforts from the end-user application. Frank Ferro, DSP Mar-

keting Manager at AT&T, says that VCOS is not intended to be an operating system that is all things to all people. It is an approach to implement AT&T's 32-bit floating-point DSP3210 on the mother board of a PC or workstation.

The major emphasis of VCOS is to make the hardware implementation of the DSP3210 inexpensive and the software easy to create. The DSP3210 interfaces directly to Motorola and Intel μP buses and shares the host memory. This approach does away with the cost of high-speed static RAM (SRAM).

The VCOS kernel is a small program (fewer than 400 32-bit words) that runs on the DSP $\mu P.$ It handles execution control, caching, and buffer I/O. The VCOS Application Server runs on the host, loads and links the DSP tasks, and performs all memory-management functions. A debugger and library are also included to ease development.

The DSP program is loaded into the internal RAM of the DSP μ P. The internal RAM is used to run the program, usually in sections. The DSP μ P has access to the host memory where it can store data. Taking over the slower host bus reduces the performance of both the DSP μ P and the host μ P. But AT&T claims that the performance of both is not reduced significantly.

Two workstations already have DSP μPs on the mother board: Next Inc's Next and Silicon Graphics' Iris Indigo computers both have Motorola's DSP56001.

Many chip vendors feel that it is too early to place the DSP μP on the mother board, and that add-in boards should be used for some time. The workstation market will see DSP chips on the mother board first. The workstation market traditionally has proprietary systems and can make its own decisions about how to implement a DSP μP . Apple also has considerable control over what will end up on the mother board of its Macs. The PC market is different—with so many different manufacturers, it will take some time before a consensus is reached.

Acronyms used in this article and in the chip directory

ADC—analog-to-digital converter

ALU—arithmetic and logic unit

ASIC—application-specific integrated circuit

CMOS—complementary metal-oxide semiconductor

CPU—central processing unit

CQFP—ceramic quad flat pack

DAC—digital-to-analog converter

DIP—dual in-line package DMA—direct memory access

DSP—digital-signal processing EPROM—erasable PROM FFT—fast Fourier transform

FIFO—first in, first out FIR—finite-impulse response

IC—integrated circuit

IIR—infinite-impulse response I/O—input-output

JTAG—Joint Test Action Group

μP—microprocessor
NMOS—n-type metal-oxide semiconductor

OSPA—Open-Signal Processing Architecture

PC—personal computer

PGA-pin-grid array

PLCC—plastic leaded chip carrier

PLL—phase-locked loop

PQFP—plastic quad flat pack PROM—programmable read-only

memory

QFP-quad flat pack

RAM-random-access memory

ROM—read-only memory

SOP—small-outline package

Spox—real-time multitasking operating system

EDN's DSP-chip directory

It is doubtful that the next year will bring a DSP μP to the mother board of a majority of computers. But watch for a number of announcements along these lines. Within a few years, applications will require these high speed devices.

DSP in real time

If you need a real-time operating system that can run directly on the DSP μP in embedded applications, you have the choice of Spox for floating-point chips and VRTX32 for Motorola's fixed-point DSP56001. Bryant Wilder, Motorola's DSP operations manager, says that VRTX32/DSP56000 from Ready Systems (Sunnyvale, CA) is the only real-time operating system available for fixed point DSP $\mu Ps.$ It is basically the same as the other versions of VRTX32, which have been available on a number of μPs for many years. Users of VRTX32 can use their existing tools and experience and just add the DSP56000 version.

High-level-language options grow

Whichever operating system you choose, you will still be able to take advantage of the productivity gains from using a high-level language. By far, the most common high-level language for DSP μ Ps is C. Nearly all of the floating-point DSP μ Ps have an ANSI C compiler. You can also use an Ada compiler. Eric West, C40 Marketing Manager at TI, says that the company plans to develop a Fortran compiler for the C30 and C40.

C is not standing still. ANSI C (more appropriately called Standard C) allows program transportability. But there are an ever growing array of C variations,

Numerical C, Concurrent C, C++, C^* , and GNU C, to name a few.

Numerical C is intended to make C more applicable to calculation-intensive applications, like DSP. Tim Counihan, strategic marketing manager for DSP at Analog Devices, says that Analog Devices is actively supporting Numerical C. He feels that the standard is well enough defined to produce a product. He does admit that Analog Devices will probably have to make some changes by the time a standard is available. The Numerical C Extensions Group (NCEG) is working within ANSI (X3J11.1) on a technical report, not a standard, so an actual standard is still in the future.

Other DSP-µP manufacturers are not supporting Numerical C yet. They are waiting for either their customers to request it or a standard to be available. TI says the company will definitely support Numerical C when it becomes a standard.

All of the C compilers for DSP µPs claim to be optimizing compilers. It is difficult to determine how well the optimizing compilers will work in your application. You will often have to optimize some sections of your high-level code by hand. On one recent project, a DSP consulting group was able to prototype the system with C code in a matter of hours. This C version proved the concept, but would only run at 12 frames/sec. The customer needed 15 frames/sec. The group spent three months optimizing the code to meet the 15 frames/sec requirement.

The Comdisco (Foster City, CA) DSP Procoder is an option to the company's Signal Processing Worksystem (SPW). The SPW is a block-diagram-based devel-

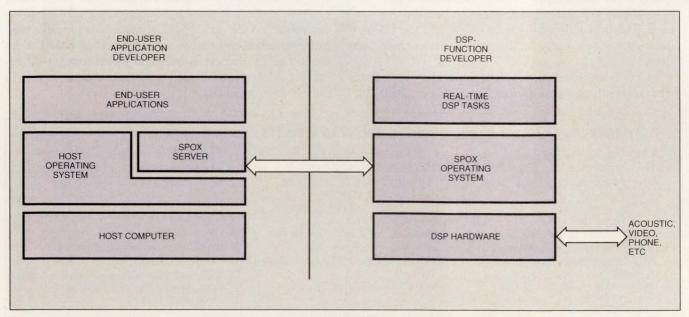


Fig 1—Separating the DSP function developer from the end-user application developer lets each expert concentrate on his speciality.

EDN's DSP-chip directory

opment system. The DSP Procoder will take a block diagram of a DSP algorithm and create assembly code. Comdisco claims the resulting code is production-quality. The DSP Procoder presently uses Motorola's DSP56001. Other fixed-point DSP μPs will be used in the future.

Multiprox is another option for SPWs used to partition a block diagram to run on multiple processors. When used with the Code Generation System, you can automatically produce C code for multiple floating-point DSP $\mu Ps.$ The generated code includes the interprocessor-communication code to pass data between the processors. The TMS320C30, TMS320C40, and DSP96002 are supported.

Need quadruples performance every 18 months

As soon as you finish designing a product, you will often be called upon to start the next generation. Rick Rinehart, floating-point DSP marketing manager at Texas Instruments, points out that the market window today averages about 18 months. The market window is the length of time from when a company introduces a product until they begin ramping down production. Each new generation of a product needs about a four times increase in performance to remain competitive. The improvements in design and processes used to build ICs will double performance every three years. Rinehart feels the only way to meet the quadrupling performance needs of their customers is with parallel processing.

Making products that can see, talk, and listen is difficult. Much of that type of development is possible

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today, but it requires expensive parallel processing systems. Prices will continue to drop until today's expensive systems become tomorrow's low cost peripherals. For example, the TMS32010 started sampling at \$500. Now you can buy them in single quantities for \$4.90.

Article Interest Quotient (Circle One) High 494 Medium 495 Low 496

Key to abbreviations used in block diagrams

AB—combined program and data address bus

ACC—accumulator

ADC/DAC—analog-to-digital and digital-to-analog converter

ADDR GEN—address generator

ALU—arithmetic logic unit BIT MANIP—bit manipulation

BS—barrel shifter

CDB—control data bus CM—cache memory

CPUB—CPU bus

DAB—data address bus

DB-combined program and data bus

DDB—data data bus

DM—memory for data only

DMAAB—DMA address bus

DMADB—DMA data bus

DMAC—direct-memory-access

controller

FX—fixed-point

FP-floating-point

GDB—global data bus

HOST INTER—host interface

IDB—instruction data bus

INT—external interrupt

MAC—multiplier accumulator

MULT—multiplier

PAB-program address bus

PDB—program data bus

P/DM—memory for program and data

PIO-parallel I/O

PM-memory for program only

PPCP—parallel processor communication port

PRAB—peripheral address bus

PRDB—peripheral data bus REG—register

REGB—register bus

SIO—serial I/O

TIM—timer

XAB—external address bus XDB—external data bus

XDAB—external data address bus

XDDB—external data data bus XIOAB—external I/O address bus

XIODB—external I/O data bus

XPAB—external program address bus

XPDB—external program data bus

ADSP2100 FAMILY

16-BIT FIXED-POINT CMOS DSP μP

AVAILABILITY: The ADSP2100/A, 2101, 2102, 2106, 2111, 2112 are in production now. The 21msp50 and the 21msp51 are now sampling.

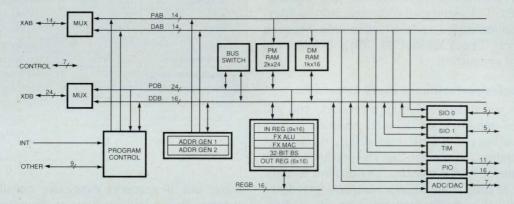
COST: ADSP2100, \$45 (1000); 2101, \$36 (1000); 2102, \$34 (5000); 2105, \$9.90; 2106, \$11.39 (25,000); 2111, \$48 (1000); 2112, \$46 (5000); 21msp50, \$57 (1000); 21msp51, \$40 (25,000).

Analog Devices Inc 1 Technology Way Norwood, MA 02062 (617) 461-3074 Circle No. 671

SECOND SOURCE: None.

DESCRIPTION: The ADSP2100 family ranges from the 2100 with no on-chip memory and an off-chip Harvard architecture to the 21msp51 with program and data ROM, data RAM, and peripherals, including an analog-to-digital and digital-to-analog

converter and host interface port on-chip. The data memory has a 16-bit width, but the program memory has a 24-bit word width to control the parallel operations. Low-voltage versions are now sampling.



FEATURES: 60-, 77-, 80-, 100-, 125-, and 167-nsec cycle-time versions.

Separate on-chip program and data buses. On-chip memory: The 2100/A has no on-chip memory. The 2101 has a $2k \times 24$ -bit program RAM and a $1k \times 16$ -bit data RAM. The 2102 has a $2k \times 24$ -bit program ROM or RAM and a $1k \times 16$ -bit data RAM. The 2105 has a $1k \times 24$ -bit program RAM and a 512×16 -bit data RAM. The 2016 has a $1k \times 24$ -bit program ROM or RAM and a 512×16 -bit data RAM. The 2111 and 21msp50 have a $2k \times 24$ -bit program RAM and a $1k \times 16$ -bit data RAM. The 2112 has a $2k \times 24$ -bit program ROM or RAM and a $1k \times 16$ -bit data RAM. The 21msp51 has a $2k \times 24$ -bit program ROM, and a $1k \times 16$ -bit data RAM, $2k \times 24$ -bit program ROM, and a $1k \times 16$ -bit data RAM.

Separate program and data buses brought off the chip only on the 2100/A. All other parts combine program and data buses off the chip.

Off-chip memory capacity: The 2100/A has $32k \times 24$ -bit program and $16k \times 16$ -bit data memory capacities. All others have $16k \times 24$ -bit program and $16k \times 16$ -bit data memory capacities

Boot memory controller loads program from external byte-wide EPROM (except 2100/A).

On-chip peripherals: The 2100/A has no on-chip peripherals. The 2101 and 2102 have two serial I/O ports and a timer; the 2105 has one serial I/O port and a timer. The 2111/2 have two serial I/O ports, a timer, and a host interface port. The 21msp50 has two serial I/O ports, a parallel I/O

port, a timer, and a 16-bit ADC/DAC (linear codec).

Multiplier/accumulator accepts 16-bit fixed-point input and creates 32-bit fixed-point results within a 40-bit accumulator. 16-bit ALU. 32-bit bidirectional barrel shifter. 40-bit accumulator.

Multiplier/accumulator, ALU, and shifter are separate blocks connected by the 16-bit R-bus and the data bus.

Zero-overhead looping.

Only the 2100/A has a 16 × 24-bit on-chip cache.

Direct, indirect, immediate, circular, and bit-reversal addressing modes.

Two address generators.

No on-chip DMA. Serial port and codecs have auto buffer, which transparently transfers data to and from memory.

16-level hardware stack. Status stack limits interrupts to four levels of nesting on the 2100/A, seven levels on the others.

Four external interrupts on the 2100/A; three external interrupts on others.

The 2100/A has only hardware wait states. Others have only software-programmable wait states.

No on-chip emulation port.

Only the 21msp50 has power-down mode to CMOS standby levels. The 2101, 2105, 2106, 2111, and 2112 have an idle mode, which lowers power until an interrupt is detected.

Packaging: 2100/A, 100-pin PQFP and 100-pin PGA. 2101/2,
68-pin PGA and 68-pin PLCC. 2105/6, 68-pin PLCC. 2111,
100-pin PQFP and 100-pin PGA. 21msp50/1, 100- and 132-pin PQFPs, 144-pin PGA.

HARDWARE

SUPPORT

SOFTWARE

Full-featured in-circuit emulator.

Low-cost in-circuit emulator board.

Demo board.

Evaluation packages.

Third-party support: Contact Analog Devices for a list of third-party vendors.

C compiler.

Simulator.

Macroassembler/linker.

Application libraries.

Upcoming Numerical C.

16-BIT FIXED-POINT CMOS DSP μP

AVAILABILITY: The DSP16, 16A, and 16C are in production. The DSP1610 and 1616 are sampling with production starting

COST: DSP16, \$9.60; DSP16A, \$16.70; DSP1610, \$125;

DSP1616, \$35 (10,000).

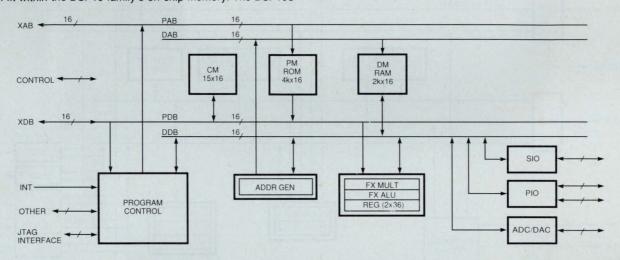
SECOND SOURCE: None.

AT&T Microelectronics Dept 52AL040420 555 Union Blvd Allentown, PA 18103 (800) 372-2447, ext 802; in Canada, (800) 553-2448, ext 802

Circle No. 672

DESCRIPTION: The members of the DSP16 family have long been the fastest fixed-point DSP chips. The DSP16A has a 25-nsec cycle time. The DSP16A and DSP16C also have the largest on-chip program memory at 12k×16 bits. Many applications that would require external ROMs with other DSP chips can fit within the DSP16 family's on-chip memory. The DSP16C

has an A/D and a D/A converter on chip. The DSP16C also has a 4-pin JTAG interface, which assists in testing tightly packed boards. A 3.3V version of the DSP16A is available. The DSP1610 and 1616 are enhanced versions intended for digital cellular telephones.



FEATURES: 25-, 33-, 55-, and 75-nsec cycle-time versions. The DSP16C has 38.5- and 76.9-nsec cycle-time versions.

Separate on-chip program and data buses.

On-chip memory: The DSP16 has a 2k×16-bit program ROM and a 512×16-bit data RAM. The DSP16A and -16C have a 12k×16-bit program ROM and a 2k×16-bit data RAM. The DSP1610 has a 512×16-bit boot ROM and an 8k×16-bit dual-port RAM. The DSP1616 has a 12k×16-bit ROM and a 2k × 16-bit dual-port RAM.

The program ROM on the DSP16 can be replaced with as many as 64k words of external memory.

The program ROM on the DSP16A and 16C can be replaced or augmented with as many as 64k words of external mem-

The DSP1610/1616 can access two external 64k address spaces.

Parallel and serial I/O port.

The DSP16C has an on-chip codec.

The DSP1610 and 1616 have an on-chip timer.

The multiplier accepts 16-bit fixed-point data and creates 32-bit

fixed-point results within a 36-bit accumulator.

32-bit ALU.

Only the DSP1610 and 1616 have a 36-bit barrel shifter and bit-manipulation instructions.

Two 36-bit accumulators.

Zero-overhead cache looping as many as 127 times.

15-word instruction cache.

Immediate, register-indirect, and circular addressing modes. No on-chip DMA.

Single-level hardware stack is software expandable into main memory.

One external interrupt.

DSP1610 has hardware and software wait states. DSP1616 has software wait states.

DSP1610 and 1616 have on-chip emulation ports.

The DSP16A, 16C, 1610, and 1616 have power-down mode.

The DSP1616 will run from 3.3 to 5V.

Packaging: DSP16 and 16A, 84-pin PLCC or 133-pin PGA. DSP16C, 100-pin PQFP. DSP1610, 132-pin PQFP. DSP1616, 100-pin PQFP or PLCC.

HARDWARE -

SUPPORT

SOFTWARE

Development system with in-circuit emulation. Evaluation board that plugs into a PC.

Assembler/linker.

Simulator.

Application library.

Third-party support includes filter-design packages. Contact AT&T for a list of third-party vendors.

DSP56156

16-BIT FIXED-POINT CMOS DSP μP

AVAILABILITY: Now.

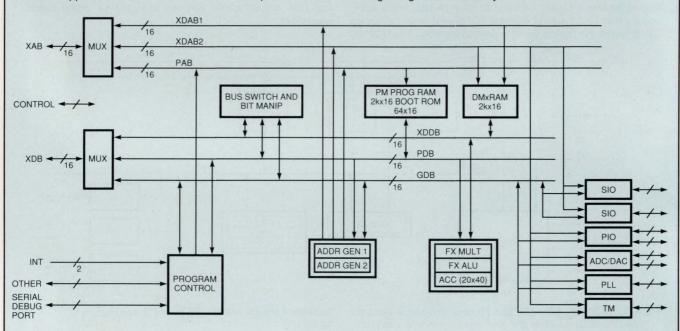
COST: 40 MHz, \$104.50 (180); 60 MHz, \$135.85 (180).

SECOND SOURCE: None.

Motorola Inc Microprocessor Products Group 6501 William Cannon Dr Austin, TX 78735 (512) 891-2030 FAX (512) 891-3874 Circle No. 673

DESCRIPTION: The 56156 is a 16-bit subset version of the 56001. It is intended for cellular telephone and other communication applications. It has a built-in codec and phases-locked

loop. Development tools are similar to the 56001 and the 96002. The 56156 has been available to select customers and is now moving into general availability.



FEATURES: 33- and 50-nsec cycle-time versions.

Three address buses and three data buses.

On-chip memory includes a $2k \times 16$ -bit program RAM and a $2k \times 16$ -bit data RAM.

ROM-based version (DSP56156ROM) contains a $12k \times 16$ -bit program ROM.

Separate external program and data memory spaces. Each can address 64k × 16-bit locations.

Can load program from external EPROM.

Asynchronous and synchronous serial I/O ports.

Parallel port can interface with a host µP.

Has on-chip PLL.

On-chip, sigma-delta voice-band codec.

Multiplier accepts 16-bit data and returns 40-bit results to 40-bit accumulator.

ALU performs arithmetic operations on 40-bit data and logical operations on 16-bit data.

No barrel shifter.

Two 40-bit accumulators.

Zero-overhead looping.

Immediate, direct, indirect, circular, and bit-reversed addressing modes.

No DMA support.

Two external vectored interrupts.

Has on-chip emulation.

Low-power mode.

Packaged in a 112-pin CQFP.

HARDWARE SUPPORT SOFTWARE

Application-development system includes in-circuit emulator. Contact Motorola for a list of third-party vendors.

Macro cross-assembler.

Linker.

Application-development board.

24-BIT FIXED-POINT CMOS DSP μP

AVAILABILITY: Now.

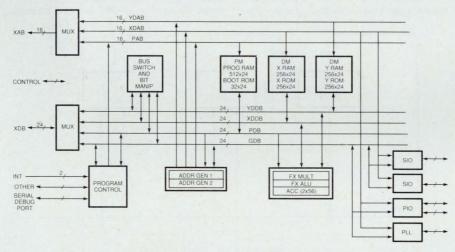
COST: DSP56001: 27 MHz, \$52.00 (180) and 33 MHz, \$62.40 (180); DSP56002: in PGA, \$166 (180) and in CQFP, \$91 (180).

SECOND SOURCE: None.

Motorola Inc Microprocessor Products Group 6501 William Cannon Dr Austin, TX 78735 (512) 891-2030 FAX (512) 891-3874 Circle No. 674

DESCRIPTION: The 56001 provides one 24-bit data word and two 56-bit accumulators. This extended precision lets the chip process 16-bit data more easily than the 16-bit machines can. The 24-bit word width eases scaling, and the 56-bit accumu-

lators prevent overflow. The 24-bit data width suits digital audio applications. The 56002 is a high-speed, low-power, low-voltage version of the 56001, which is 100% software compatible, and includes a PLL and on-chip emulation.



FEATURES: 60- and 74-nsec cycle-time versions.

Three address buses and four data buses.

Separate address buses for program ROM and the two data

Separate data buses for program ROM, the two data RAMs, and global data.

On-chip memory includes a 512×24 -bit program RAM, a 32×24 -bit boot ROM, dual 256×24 -bit data RAMs, and dual 256×24 -bit data ROMs.

ROM-based version (56000) available.

Three separate memory spaces (X, Y, and P). Each can address 64k × 24-bit locations.

Can load program from external EPROM.

Asynchronous 8-bit serial I/O port.

Synchronous 8- to 24-bit serial interface.

Parallel port can interface with a host µP.

56002 has on-chip PLL.

Multiplier accepts 24-bit data and returns 48-bit results to 56-bit accumulator.

ALU performs arithmetic operations on 56-bit data and logical operations on 24-bit data.

No barrel shifter.

Two 56-bit accumulators.

Zero-overhead looping.

Immediate, direct, indirect, circular, and bit-reversed addressing modes.

Two address generators.

No DMA support.

System stack is 15-levels deep, but can be read by program to extend stack into main memory.

Two external vectored interrupts on 56001, three on 56002.

Hardware and software-programmable wait states.

Only the 56002 has on-chip emulation.

Low-power mode.

56002 operates on 2.0 to 5.5V power supplies.

Packaging: 56001, 132-pin CQFP or 88-pin PGA. 56002, 132-pin PGA, CQFP, or PQFP.

HARDWARE -

SUPPORT

SOFTWARE

Application-development system includes in-circuit emulator. Contact Motorola for a list of third-party vendors.

C compiler.

GNU C compiler and source-level debugger.

Macro cross-assembler.

Linker/librarian.

Simulator.

Code translator from TMS320C10 to 56001.

Third-party support includes filter-design software, and VRTX32/DSP56001 real-time operating system.

μPD77C25

16-BIT FIXED-POINT DSP μP

AVAILABILITY: The 77C25 is available now. A 3V operation version is planned for 1992.

COST: 77C25, \$9 (5000); 77P25, \$45 (1000); 77P25C, \$20

(1000).

SECOND SOURCE: Oki Semiconductor (Sunnyvale, CA)

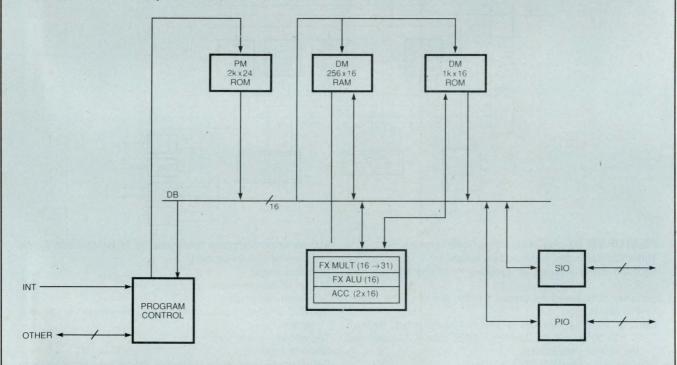
also makes the 7720.

NEC Electronics 401 Ellis St Mountain View, CA 94039 (800) 632-3531;

(415) 965-6158 FAX (800) 729-9288 Circle No. 675

DESCRIPTION: The 77C25 is an upgrade of the 7720, which was one of the first successful DSP chips. The basic architecture is out of date and its memory can't be expanded off chip. The

manufacturer says there is still interest in new 77C25 designs because of the chip's low cost. The 77P25 is an EPROM version of the 77C25. The 77P25C is a one-time-programmable version.



FEATURES: 100- and 122-nsec cycle time.

Single address bus only for program memory.

Pointers address data memory.

Single data bus for both program and data.

On-chip memory: The 77C25 has a $2k \times 24$ -bit program ROM, a 256×16 -bit data RAM, and a $1k \times 16$ -bit data ROM. The 77P25 has the same memory as the 77C25, but replaces ROM with EPROM.

No external memory expansion.

One 8-bit serial I/O port.

Parallel I/O port.

Multiplier accepts 16-bit fixed-point data and produces 31-bit fixed-point results within two 16-bit accumulators.

16-bit ALU.

No barrel shifter.

Two 16-bit accumulators.

No zero-overhead looping.

No address generators.

No on-chip DMA controller.

4-level stack stores the program counter during subroutines and interrupts and is not expandable.

Single external interrupt.

No wait states.

No on-chip emulation port.

No low-power mode.

Packaged in 28-pin DIP, 28-pin PLCC, 44-pin PLCC, and 32-pin SOP.

HARDWARE

SUPPORT

SOFTWARE

Evaluation kit for application development also functions as incircuit emulator.

Assembler/linker.

Third-party simulator available.

24-BIT FIXED-POINT CMOS DSP μP

AVAILABILITY: 100- and 122-nsec versions available now.

COST: \$27 (1000).

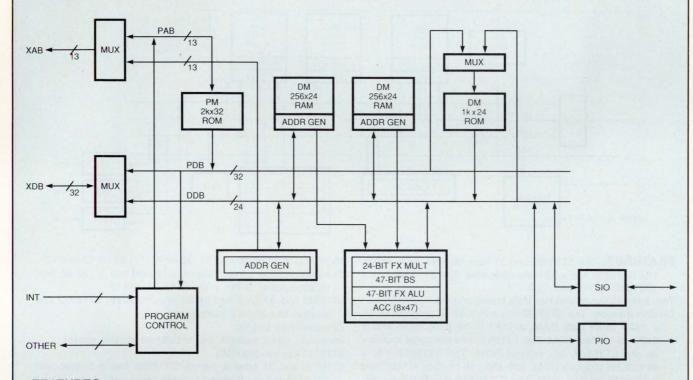
SECOND SOURCE: None.

NEC Electronics 401 Ellis St Mountain View, CA 94039 (800) 632-3531; (415) 965-6158 FAX (800) 729-9288; (415) 965-6130

Circle No. 676

DESCRIPTION: The 77220 is a scaled-down version of the 32-bit floating-point 77230. The chip size and pin count are reduced by using 24-bit data and removing the floating-point exponent hardware. The 24-bit word width suits the digital audio market. The instruction set is a subset of the 77230 and is

source-code compatible with the floating-point device. The vendor says the 77220's architecture is optimized for adaptive filter applications. The 77P220R EPROM version and the 77P220L one-time-programmable version are for prototyping and low-volume applications.



FEATURES: 100- and 122-nsec cycle-time versions.

Separate on-chip program and data buses.

On-chip memory includes a $2k \times 32$ -bit program ROM, dual 256×24 -bit data RAMs, and a $1k \times 24$ -bit data ROM.

Off-chip memory can be expanded to $8k \times 32$ -bit program memory and $8k \times 24$ -bit data memory.

One serial I/O port.

Parallel I/O port can be used as host µP interface.

Multiplier accepts 24-bit fixed-point data and creates 47-bit fixed-point results within a 47-bit accumulator.

47-bit ALU.

47-bit bidirectional barrel shifter.

Eight 47-bit accumulators.

Direct, indirect, immediate, circular, and bit-reversal addressing modes.

Three address generators.

No on-chip DMA.

Hardware stack is eight levels deep and is not expandable.

Two external interrupts.

No supported wait states.

No on-chip emulation port.

No low-power mode.

Packaged in a 68-pin PGA or 68-pin PLCC.

HARDWARE -

SUPPORT -

SOFTWARE

Evaluation kit and PC evaluation board.

Assembler/linker.

Simulator.

C compiler available by mid 1992.

ST18930/31/32/42

16-BIT FIXED-POINT CMOS DSP μP

AVAILABILITY: Now.

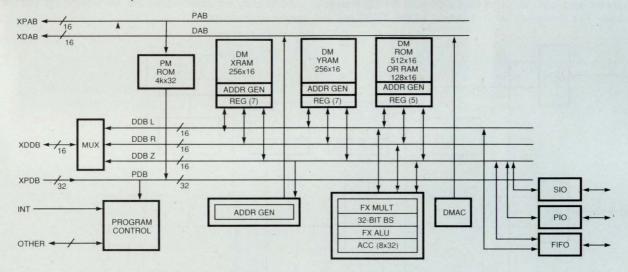
COST: ST18930, \$15 (10,000); ST18931, \$75 (100); ST18942, \$35 (10,000); ST18R942, \$80 (100). The ST18932 is only available for ASIC designs.

SECOND SOURCE: None.

SGS-Thomson Microelectronics 1000 E Bell Rd Phoenix, AZ 85022 (602) 867-6340 Circle No. 677

DESCRIPTION: The ST18 family consists of four devices. The ST18930 and 31 are CMOS versions of the NMOS original with a few enhancements and twice the speed. The ST18932 is a core for custom DSP μ Ps. The CMOS ST18942 offers

further enhancements in its arithmetic capabilities, addressing modes, and I/O functions. All family members can operate on complex and double-precision data. The ST18932 and 42 have a 32-bit ALU and 16-bit data buses.



FEATURES: The ST18930 and 31 have 80-nsec cycle times. The ST18932 has a 50-nsec cycle time. The ST18942 has a 100-nsec cycle time.

Two address buses and four data buses on chip.

On-chip memory: The ST18930 has a $3k \times 32$ -bit program ROM, a 192×16 -bit data RAM, a 128×16 -bit data RAM, and a 512×16 -bit data ROM. The ST18931 has the same memory as the ST18930, but without ROM. The ST18942 has a $4k \times 32$ -bit program ROM, two 256×16 -bit data RAMs, and a 512×16 -bit data ROM. The ST18R942 is a ROMless version of the ST18942 and has two 256×16 -bit and one 128×16 -bit data RAMs.

64k × 32-bit external program memory (except ST18930).

The ST18930 and 31 have $4k \times 16$ -bit external data memory space. The ST18932 has $8k \times 16$ -bit external data memory. The ST18942 and ST18R942 have $64k \times 16$ -bit external memory.

Only the ST18942 has both a serial I/O port and a parallel I/O port.

ST18932 and 42 multipliers accept 16-bit fixed-point data and return 32-bit fixed-point results to 32-bit accumulator. The ST18930 and 31 return 16-bit results.

In complex mode, the multiplier multiplies two complex numbers in two cycles.

16-bit ALU in ST18930 and 31. 32-bit ALU in ST18932 and 42.

16-bit bidirectional barrel shifter in ST18930 and 31. 32-bit bidirectional barrel shifter in the ST18932 and 42.

ST18930 and 31 have two 16-bit accumulators. ST18932 and 42 have four 32-bit accumulators.

Zero-overhead looping.

Immediate, direct, indirect, and circular addressing modes. ST18942 has on-chip DMA.

ST18930 and 31 have a 1-level, ST18932 has a 2-level, and ST18942 has an 8-level hardware stack for interrupts and subroutines. All can be expanded into main memory with software.

Three external interrupts on the ST18930 and 31 and eight on the ST18932 and 42.

Hardware and software-programmable wait states.

Only the ST18932 has on-chip emulation port.

Low-power mode.

Packaging: ST18930, 48-pin DIP and 52-pin PLCC. ST18931, 124-pin PGA. ST18942, 160 PQFP. ST18R942, 160 PQFP and 144-pin PGA.

HARDWARE -

SUPPORT

SOFTWARE -

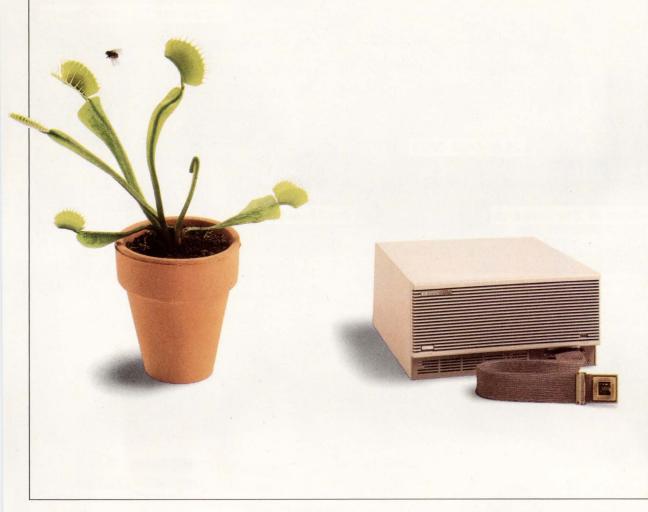
Hardware-development system provides in-circuit emulation of as many as three DSP chips in real time.

Stand-alone emulator board connects to PC.

EPROM module. A ROMless version with EPROMs on a small board that plugs into a ROM-version socket.

Macroassembler/linker. Simulator.

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16-BIT FIXED-POINT CMOS DSP μP

AVAILABILITY: The C10, C15, C16, C17, E14, E15, E17, P15, P17, P14, LC15 (3.3V), and LC17 (3.3V) are available now. The C14 will be available in the fourth quarter of 1991.

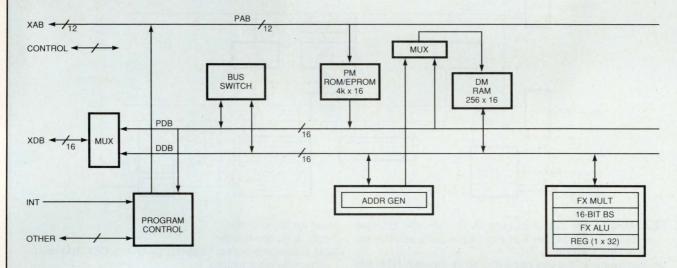
COST: C10 (20 MHz), \$4.90; C10 (25 MHz), \$6; C14, \$9; E14, \$45; P14, \$22; C15 (20 MHz), \$7; C15 (25 MHz), \$6; E15 (20 MHz), \$35; E15 (25 MHz), \$45; P15, \$20; C16, \$9; E17, \$38; P17, \$20 (1000).

SECOND SOURCE: Microchip Technology (Chandler, AZ) for the C10, C14, and E14. No second source for other parts.

Texas Instruments Inc Semiconductor Group, SC-001 Box 809066 Dallas, TX 75380 (800) 336-5236, ext 700 Circle No. 678

DESCRIPTION: This first generation of the vendor's DSP family was introduced in 1982. Although this family is difficult to use and slower than similar devices, the chips' cost—which has dropped to \$3 in high volumes—and the large body of associated software and expertise will keep this family going.

Newer family members have additional memory and peripheral options. EPROM (TMS320E1X) and one-time-programmable (TMS320P1X) versions are also available. 3.3V versions of the C1X family are now available.



FEATURES: 114-, 160-, 200-, and 280-nsec cycle-time versions. Separate on-chip program and data buses.

On-chip memory: The C10 has a 1.5k×16-bit program ROM and a 144×16-bit data RAM. The C14, C15, and C17 have a 4k×16-bit program ROM and a 256×16-bit data RAM. The E14, E15, and E17 have a 4k×16-bit program EPROM and a 256×16-bit data RAM. The C16 has an 8k×16-bit program ROM and a 256×16-bit data RAM. P1X versions are one-time programmable.

Program and data buses are combined off chip.

 $4k \times 16$ -bit total external memory, except the C16, which has $64k \times 16$ -bit external memory, and the C17, which has no external memory.

On-chip peripherals: The C10, C15, and C16 have parallel I/O. The C14 has serial and parallel I/O. The C17 has two serial I/O ports, parallel I/O, and a compander.

Multiplier accepts 16-bit fixed-point data and creates 32-bit fixed-point results within a 32-bit accumulator.

32-bit ALU.

16-bit left barrel shifter.

Single 32-bit accumulator.

No zero-overhead looping.

No DMA.

4-level hardware stack except the C16, which has an 8-level hardware stack.

Single external interrupt.

No wait states.

No on-chip emulation.

LC1X devices operate at 3.3V.

Packaging: C10, 40-pin DIP or 44-pin PLCC. C14, 40-pin DIP or 44-pin PLCC. C15, 40-pin DIP or 44-pin PLCC. C16, 64-pin QFP. C17, 40-pin DIP or 44-pin PLCC.

HARDWARE -

SUPPORT

SOFTWARE

In-circuit emulator.

Evaluation module.

Software-development system.

Many third-party support tools. Contact Texas Instruments for a list of third-party vendors.

Assembler/linker.

Simulator.

Application library.

Many third-party support tools.

TMS320C2X/320C5X

16-BIT FIXED-POINT CMOS DSP μP

AVAILABILITY: The C25, C26, and E25 are available now. The C50 and C51 are sampling now and will be in production in the fourth quarter of 1991.

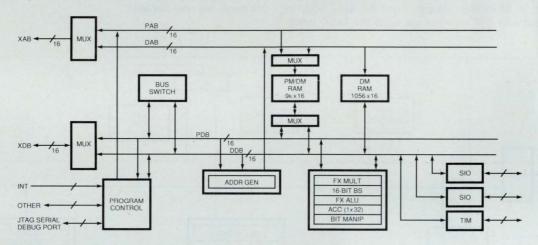
COST: C25 (33 MHz), \$14; C25 (40 MHz), \$15; C25 (50 MHz), \$17; E25, \$55; C26, \$16; C50, \$130; C51, \$40 (1000).

SECOND SOURCE: None.

Texas Instruments Inc Semiconductor Group, SC-9053 Box 809066 Dallas, TX 75380 (800) 336-5236, ext 700 Circle No. 679

DESCRIPTION: These chips make up the second generation of the vendor's DSP family. They offer higher performance than the first-generation chips and are easier to use. For many applications, the C25's price has dropped to a point where the chip is replacing the C1X. The C5X parts are enhancements to the

C25. They use the same basic core architecture as the C25, but have double the performance level, additional on-chip peripherals, and expanded memory. An EPROM version of the C25, the E25, is also available.



FEATURES: The C2X chips come in 78-, 98-, and 125-nsec cycle-time versions. The C5X chips come in 35- and 50-nsec cycle-time versions.

On-chip memory: The C25 has a $4k \times 16$ -bit program ROM and a 544×16 -bit data RAM. The C26 has a $1.5k \times 16$ -bit program RAM with boot ROM to load programs from external memory and a 544×16 -bit data RAM. The C50 has a $9k \times 16$ -bit program/data RAM and a 1056×16 -bit dual-access RAM. The C51 has an $8k \times 16$ -bit program ROM, a $1k \times 16$ -bit program/data RAM, and a 1056×16 -bit dual-access RAM.

Program and data memory are combined off chip.

The C2X and C5X can address 64k×16-bit programs and 64k×16-bit data memories.

The C25 and C26 have one serial port each. The C5X has two serial ports.

Multiplier accepts 16-bit fixed-point data and creates 32-bit fixed-point results within a 32-bit accumulator.

32-bit ALU.

The C5X has a separate 16-bit parallel logic unit for manipulating bits without affecting the contents of the accumulator.

16-bit left barrel shifter.

Single 32-bit accumulator.

Next-instruction-repeat looping. Only the C5X has zerooverhead block looping.

Immediate, direct, indirect, and bit-reversal addressing modes. C5X also has circular addressing.

No DMA

8-level expandable hardware stack.

C5X has a 1-level-deep shadow RAM, which stores some registers

C2X has three external interrupts; C5X has five.

Hardware wait states. C5X also has software-programmable wait states.

The C5X has an on-chip emulation port.

The C2X is source-code compatible with the C5X.

The C5X has a JTAG interface.

The C25 and C26 have an idle mode. The C5X has a power-down mode.

Packaging: C25 and C26, 68-pin PGA or PLCC. C50, 132-pin QFP.

HARDWARE -

SUPPORT

SOFTWARE

Both the C2X and C5X have an in-circuit emulator. Both also have a software-development board for PCs. Many third-party support tools. Contact manufacturer for a list of third-party vendors. C compiler for both C25 and C5X. Source-level debugger for C5X. Assembler/linker. Simulator. Application library.

Many third-party support tools.



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P.O. BOX 350166, BROOKLYN, N.Y. 11235-0003 TEL 718-934-4500 EXTENSION 231 FAX 718-332-4661

32-BIT FLOATING-POINT CMOS DSP μP

AVAILABILITY: The ADSP21020 is available now.

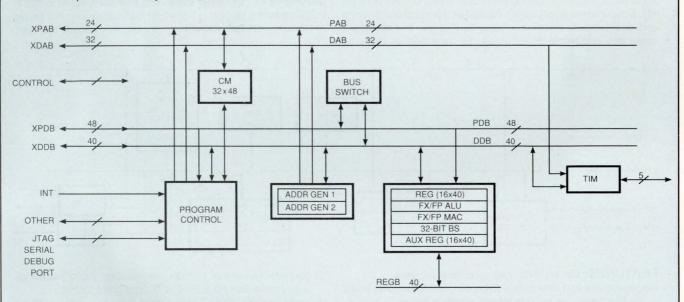
COST: \$147 (1000).

SECOND SOURCE: None.

Analog Devices Inc 1 Technology Way Norwood, MA 02062 (617) 461-3074 Circle No. 680

DESCRIPTION: This device is the vendor's first floating-point DSP μ P. It has an off-chip Harvard architecture and is similar to the fixed-point 2100 family. On-chip emulation supported via

a JTAG port. The device conforms to the IEEE-754 floating-point standard.



FEATURES: 40-, 50-, and 66-nsec cycle-time versions.

One 32-bit and one 24-bit address bus.

One 40-bit and one 48-bit data bus.

Seven 40-bit additional buses in the CPU.

Separate program, and data buses (off-chip Harvard Architecture)

 $4G \times 40$ -bit external data memory and $16M \times 48$ -bit external program memory.

One 32-bit timer.

IEEE-754 32-bit and 40-bit floating-point format.

Multiplier accepts 32-bit and 40-bit floating-point data and returns 32-bit or 40-bit results. 32-bit fixed-point operands produce 64-bit fixed-point products. The multiplier also incorporates dual 80-bit fixed-point accumulators.

ALU accepts 32-bit and 40-bit floating-point data and returns 32-bit or 40-bit results. 32-bit fixed-point operands produce 32-bit results.

Parallel multiplier and ALU operate in single cycle.

32-bit bidirectional barrel shifter.

32 40-bit register-based accumulators.

Zero-overhead looping.

32 × 48-bit instruction cache.

Cache optimizes performance by selecting only 3-bus-operation instructions for storage in cache. Cache can be frozen to keep often-used instructions in cache.

Register, direct, indirect, immediate, relative, circular buffer, and bit-reversed addressing modes. Two independent address generators.

The hardware stack is 20 deep and can be expanded into main memory.

Four external vectored interrupts.

Four bidirectional I/O flags.

Hardware and software programmable wait states.

JTAG support of in-circuit emulation.

Idle state for low-power mode.

Packaging: 223-pin PGA, plastic and ceramic. PQFP available in 1992.

HARDWARE -

SUPPORT

— SOFTWARE

Full-speed in-circuit emulator.

Demo board for PCs.

Evaluation package.

Third-party support: Contact Analog Devices for a list of third-party vendors.

Optimizing ANSI C and Numerical C compilers.

Source-level debugger for ANSI C and Numerical C.

Simulator, assembler, linker, PROM splitter.

Application libraries.

Third-party support includes Spox, filter-design packages with code generation, and block-level algorithm development packages.

DSP32C/3210

32-BIT FLOATING-POINT CMOS DSP μP

AVAILABILITY: The DSP32C is available now. The DSP3210 is sampling now with production by the fourth quarter of 1991.

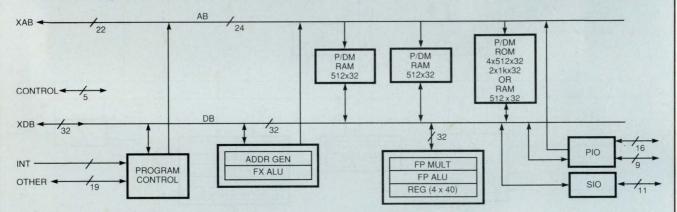
COST: DSP32C, \$70 (1000). DSP3210, \$50 (100,000).

SECOND SOURCE: None.

AT&T Microelectronics Dept 52AL300240 555 Union Blvd Allentown, PA 18103 (800) 372-2447; in Canada, (800) 553-2448 Circle No. 681

DESCRIPTION: The DSP32C has one of the simplest architectures of the 32-bit floating-point DSP chips. It uses a single 4M-word linear-memory space instead of the separate program and data memory common in other DSP chips. The single address bus and single data bus can be accessed as many as

four times per cycle. Each internal memory can be accessed as many as two times per cycle. The DSP3210, along with the VCOS operating system, is intended for use on the mother board of PCs and workstations, where it shares memory with the host.



FEATURES: 80- and 100-nsec cycle-time versions.

Single address and data buses. Each can be accessed as many as four times per cycle to imitate separate buses.

DSP32C has three on-chip 512×32 -bit RAMs. Optional ROM-based DSP32C replaces one RAM with a $4k\times32$ -bit ROM. DSP3210 has two $1k\times32$ -bit RAMs and a 256×32 -bit boot ROM.

The DSP32C can address as much as $4M \times 32$ -bits of external memory. The DSP3210 can address 4 Gbytes of external memory.

All memory is a general resource; both program and data can exist anywhere.

Data addressable as 8-, 16-, or 32-bit words.

DSP3210 can load program from external EPROM.

The DSP32C has on-chip serial and parallel I/O. The DSP3210 has serial I/O, timer, DMA controller, and a 32-bit bus interface that is compatible with Motorola and Intel μ Ps.

The serial I/O is a double-buffered port that allows concurrent input and output of 8-, 16-, 24-, or 32-bit data widths.

The DSP32C has an 8- or 16-bit parallel I/O port that an external $\ensuremath{\mu P}$ can control.

Proprietary 32-bit floating-point format.

Single-cycle conversion to/from nonstandard DSP32 floating-point format from/to IEEE-754 floating-point format.

Multiplier accepts 32-bit floating-point data and creates 45-bit floating-point results.

Separate floating-point adder accepts 40-bit floating-point data and creates 40-bit floating-point results.

Fixed-point ALU accepts 16- or 24-bit data.

Does not have a barrel shifter.

Four 40-bit accumulators.

Zero-overhead looping. As many as 2048 repeats of a block with a maximum size of 32 words.

Immediate, memory-direct, register-direct, register-indirect, and bit-reversal addressing modes.

DMA can be used with both the serial I/O and the parallel I/O. No hardware stack.

1-level-deep shadow RAM of some registers.

Two external interrupts.

Hardware wait states. DSP3210 has software-programmable wait states.

No on-chip emulation port.

Only the DSP3210 has a low-power mode.

DSP32C packaged in a 164-pin PQFP, 133-pin PGA, or 68-pin PLCC (microcontroller version, no external memory).

HARDWARE -

SUPPORT -

SOFTWARE

In-circuit emulator.

IBM PC-based development board.

VME bus-based development board.

Many third-party support tools, including the HP64773 in-circuit emulator from Hewlett-Packard. Contact AT&T for a list of third-party vendors.

Optimizing C compiler.

Assembler/linker.

State simulator.

VCOS operating system.

Many third-party support tools.

Experience 32-bit RISC Performance in Your 16-bit System at a Cost That'll Thrill You

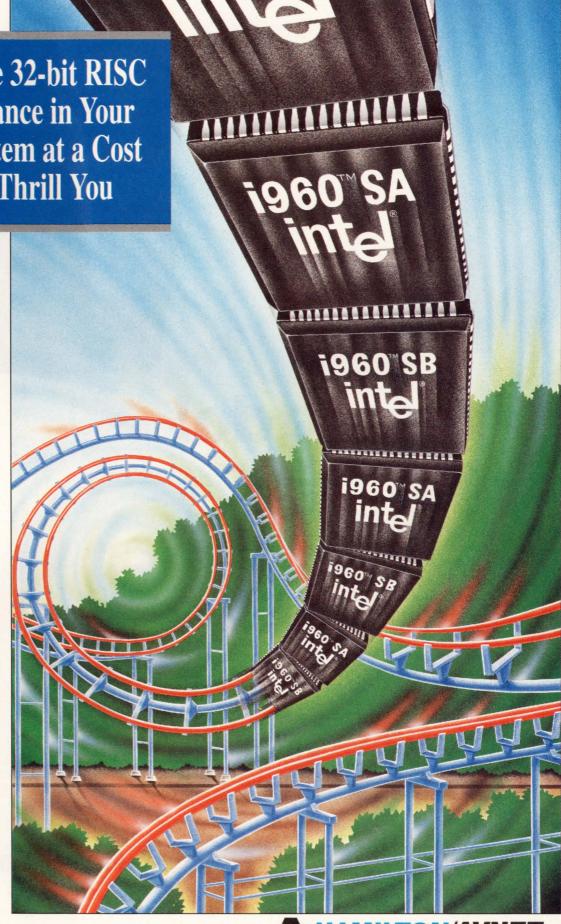
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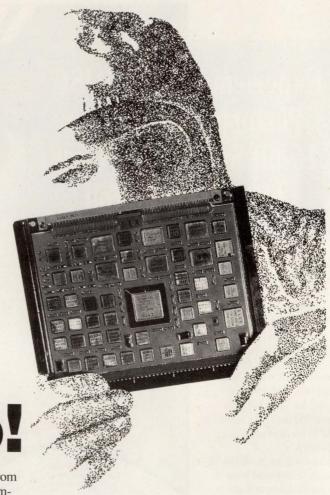
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Raytheon

32-BIT FLOATING-POINT CMOS DSP μP

AVAILABILITY: Available now. Enhanced revision available the first quarter of 1992.

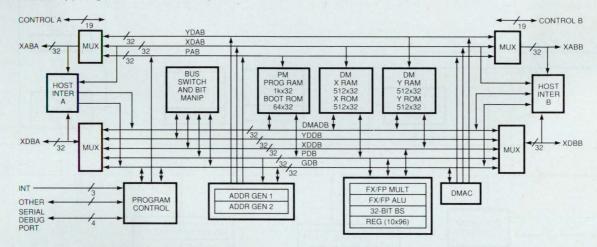
COST: 96002 (33 MHz), \$368; 96002 (40 MHz), \$441.

SECOND SOURCE: None.

Motorola Inc Microprocessor Products Group 6501 William Cannon Dr Austin, TX 78735 (512) 891-2030 FAX (512) 891-0400 Circle No. 682

DESCRIPTION: The 96002 is an architectural superset of the fixed-point 56001. The 96002 continues Motorola's emphasis on precision. The 96-bit accumulators will support future double-precision parts. The 32-bit floating-point device conforms to the IEEE-754 floating-point standard. The dual 32-bit external buses support glueless multi-96002 systems. The ex-

ternal buses can access external memory and peripherals or communicate with a host $\mu P.$ A revision of the 96002 provides some enhancements, including increased speed and letting the internal RAM act as an instruction cache. It will remain software compatible with the existing 96002.



FEATURES: 50-, 60-, and 74-nsec cycle-time versions. 50-nsec cycle-time version scheduled for the fourth quarter of 1991.

Three 32-bit address buses and five 32-bit data buses on chip. Separate address buses for program and the two on-chip RAMs. Separate data buses for program, the two on-chip RAMs, global data, and DMA.

On-chip memory includes a 1k \times 32-bit program RAM, a 64 \times 32-bit boot ROM, dual 512 \times 32-bit data RAMs, and dual 512 \times 32-bit data ROMs.

On-chip boot ROM loads program from external byte-wide EPROM.

Revised version will let the internal 1k×32-bit program RAM function like an instruction cache.

Two complete 32-bit external expansion ports for memory and I/O.

Three separate memory spaces (X, Y, and P). Each can address 4G words.

Each memory space is divided into eight 0.5G-word areas. Each can be programmed to either the A or B expansion ports.

Two host interfaces allow interface to μP or other 96002s. No other on-chip peripherals.

IEEE-754 32-bit floating-point format.

Multiplier accepts 32-bit floating-point data and returns 44-bit results. Multiplier accepts 32-bit integer data and returns 64-bit results.

32-bit bidirectional barrel shifter.

Ten 96-bit or thirty 32-bit register-based accumulators.

Zero-overhead looping.

Immediate, direct, indirect, circular, and bit-reversal addressing modes.

Two address ALUs.

Supports DMA. Uses its own internal bus and doesn't cyclesteal. Can use all of the addressing modes, including bit-reversal, with the DMA controller.

The stack is 15 levels deep and can be expanded into main memory.

Three external vectored interrupts.

Hardware and software-programmable wait states.

Serial debug port for in-circuit debugging.

Low-power mode.

Packaged in a 223-pin PGA. 256-pin CQFP available in 1991.

HARDWARE

SUPPORT

SOFTWARE

Hardware-evaluation system includes in-circuit emulator. Some third-party hardware products are available. Contact Motorola for a list of third-party vendors. Optimizing C compiler.

Assembler/linker.

Simulator.

Application library.

GNU C compiler and source-level debugger.

Third-party support includes optimizing C compiler, block-level diagraming language, filter-design software, and Spox.

μPD77240

32-BIT FLOATING-POINT CMOS DSP μP

AVAILABILITY: The 132-pin PGA package is available now.

The PQFP will be available in 1992.

COST: \$75 (1000).

SECOND SOURCE: None.

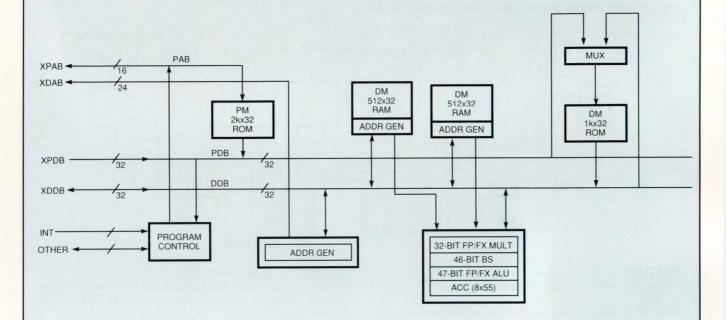
NEC Electronics 401 Ellis St

Mountain View, CA 94039

(415) 965-6158; (800) 632-3531 Circle No. 683

DESCRIPTION: The μ PD77240 is a 32-bit CMOS floating-point DSP chip. The internal instruction and data ROM are preprogrammed with math matrix routines. It has two external

buses: one for data addressing up to $16M \times 32$ -bit, and the other for instruction addressing up to $64k \times 32$ -bit. The vendor says the architecture suits adaptive filter applications.



FEATURES: 90-nsec cycle time.

Separate on-chip program and data buses.

On-chip memory: 2k×32-bit program ROM (preprogrammed), dual 512×32-bit data RAMs, and a 1k×32-bit data ROM (preprogrammed).

External memory expansion: $64k \times 32$ -bit program memory and $16M \times 32$ -bit data memory.

Separate external program and data buses.

The 77240 has no on-chip peripherals.

Proprietary 32-bit floating-point format.

Multiplier accepts 32-bit floating-point data and creates 55-bit floating-point results.

Multiplier accepts 24-bit fixed-point data and creates 47-bit fixed-point results.

47-bit ALU.

47-bit bidirectional barrel shifter.

Eight 55-bit register-based accumulators.

Direct, indirect, immediate, circular, and bit-reversal addressing modes.

Three address ALUs.

No on-chip DMA.

The stack is eight levels deep and is not expandable.

Two external interrupts.

No wait states.

No on-chip emulation port.

No low-power mode.

Packaged in a 132-pin PGA.

HARDWARE -

SUPPORT

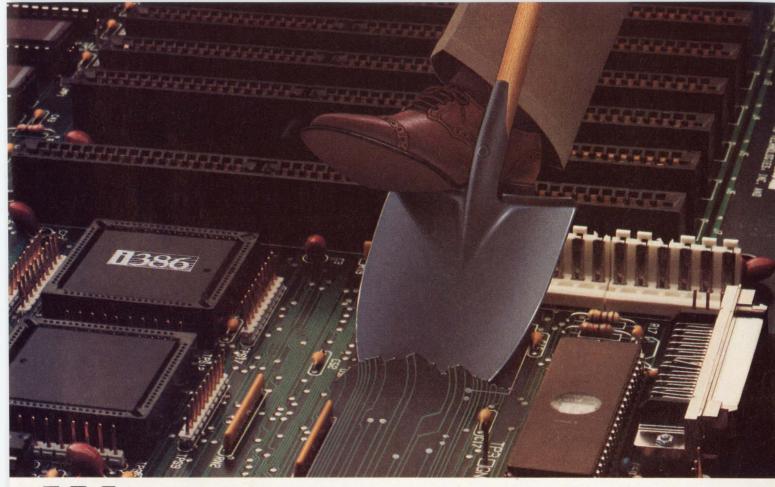
SOFTWARE

Evaluation kit, which includes an in-circuit emulator.

Assembler/linker.

Simulator.

C compiler scheduled for 1992.



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EDN October 1, 1991

CIRCLE NO. 67

127

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32-BIT FLOATING-POINT CMOS DSP μP

AVAILABILITY: The C30 and C30-27 are available now. The C30-40, C31, and C31-27 are sampling now.

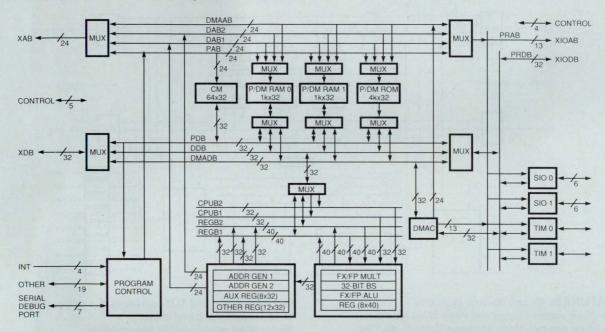
COST: C30, \$160; C30-27, \$125; C30-40, \$210; C31, \$70; C31-27, \$55 (1000).

SECOND SOURCE: None.

Texas Instruments Inc Semiconductor Group, SC-91011 Box 809066 Dallas, TX 75380 (800) 336-5236, ext 700 Circle No. 684

DESCRIPTION: This device is the floating-point member of the vendor's TMS320 family. It was the first sub-100-nsec 32-bit floating-point CMOS DSP. It is not code compatible with the fixed-point chips. The C30 is available in a slower, lower-cost version called the C30-27. The C31 is object-code compatible

with the C30 and C30-27, but has only one serial port, one parallel port, and one timer. This feature reduction decreases the chip size and pin count, which allows TI to offer a floating-point DSP for \$35 in high volume.



FEATURES: 50-, 60-, and 74-nsec cycle-time versions. Four 24-bit address buses and three 32-bit data buses. Two 32-bit and two 40-bit additional buses in the CPU. Separate program, data, and DMA buses.

Each internal RAM and ROM allows two accesses per cycle. Any of the separate memories can be used for program or data. Two on-chip 1k×32-bit RAMs and an on-chip 4k×32-bit ROM. 24-bit external memory-address bus provides 16M×32-bit total address space.

13-bit external-I/O address bus provides 8k × 32-bit I/O ports, which are mapped into the 16-Mbyte address space.

Two 8-, 16-, 24-, and 32-bit serial I/O ports. Two 32-bit timers. Proprietary 2's-complement 32-bit floating-point format.

Multiplier accepts 32-bit floating-point data and returns 40-bit floating-point result. 24-bit integers result in 32-bit fixed-point results.

ALU operates on 40-bit floating-point and 32-bit fixed-point data.

Parallel multiplier and ALU operations in a single cycle.

32-bit bidirectional barrel shifter.

Eight 40-bit register-based accumulators.

Single-instruction and zero-overhead block looping.

64 × 32-bit instruction cache.

Cache can be disabled when not needed and frozen to keep an often-used portion of code available in the cache.

Register, direct, indirect, immediate, relative, circular, and bitreversed addressing modes. Two address ALUs.

DMA controller allows concurrent I/O and CPU operation.

Hardware pointer to software stack.

Four external vectored interrupts.

Hardware and software-programmable wait states.

Serial debug port can provide in-circuit emulation.

Packaging: C30, 180-pin PGA. C30-27, 180-pin PGA. C31, 132-pin QFP.

HARDWARE -

SUPPORT

SOFTWARE

Full-speed in-circuit emulator for PCs and Sun workstations. Evaluation module plugs into a PC.

Significant third-party support. Contact Texas Instruments for a list of third-party vendors. Hewlett-Packard has a version of the HP64700 in-circuit emulator for the C30.

Optimizing ANSI C compiler. Source-level debugger and code profiler. (PC or Sun).

Assembler/linker. Simulator. (PC or Sun).

Application library.

Third-party support includes Spox, Ada compiler, filter-design packages, and block-level diagraming language.

TMS320C40

32-BIT FLOATING-POINT CMOS DSP μP

AVAILABILITY: Samples available now. Production quantities in 1992.

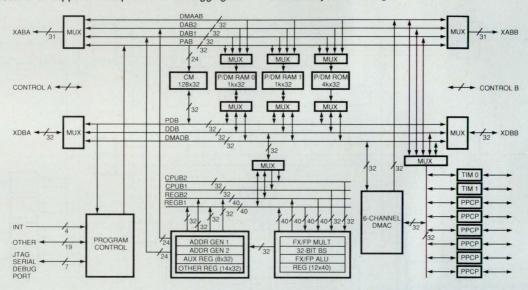
COST: Samples cost approximately \$500. \$250 (5000).

SECOND SOURCE: None.

Texas Instruments Inc Semiconductor Group, SC-9026 Box 809066 Dallas, TX 75380 (800) 336-5236, ext 700 Circle No. 685

DESCRIPTION: This device was designed for applications that require the performance of parallel processing. It is upward compatible with the C30, but adds six 32-bit FIFO dual-buffered communication ports, two complete 32-bit external buses, an analysis module that supports multiprocessor debugging via a

JTAG interface, and a 4G-word address space. The chip also features single-cycle conversion to and from the IEEE floating-point standard and a cycle time of 40 nsec. Each communication port can transfer data to and from another C40 at 20 Mbyte/sec without any external logic.



FEATURES: 40- and 50-nsec cycle time.

Four 32-bit address buses and three 32-bit data buses. Two 32-bit and two 40-bit additional buses in the CPU.

Separate program, data, and DMA buses.

Each internal RAM and ROM allow two accesses per cycle.

Any of the separate memories can be used for program or data. Two on-chip $1k\times32$ -bit RAMs and a $4k\times32$ -bit ROM.

Dual 32-bit external buses. Each has a 31-bit address, so the 4G-word memory is equally divided between the two buses.

Six independent 32-bit communication ports for glueless communications between C40s. Separate 8×32-bit FIFOs for input and output buffering.

No on-chip serial ports. Two 32-bit timers.

Proprietary 2's-complement 32-bit floating-point format.

Single-cycle conversion from and to the IEEE-754 32-bit format.

Multiplier accepts 32-bit floating-point data and returns 40-bit floating-point data. 24-bit integers result in 32-bit fixed-point results.

ALU operates on 40-bit floating-point and 32-bit fixed-point data.

Parallel multiplier and ALU operations in a single cycle.

32-bit bidirectional barrel shifter.

Twelve 40-bit register-based accumulators.

Single-instruction and zero-overhead block looping.

128 × 32-bit instruction cache.

Cache can be disabled when not needed and frozen to keep an often-used portion of code available in the cache.

Register, direct, indirect, immediate, relative, circular, and bitreversed addressing modes. Two address ALUs.

6-channel DMA controller for concurrent I/O and CPU operation.

Transmitting DMA can control the operation of the receiving

DMA, so setup for DMA transfer will not affect CPU. Hardware pointer to software stack.

Four external vectored interrupts.

Hardware and software-programmable wait states.

JTAG-based debug port controls the analysis module, which functions as an in-circuit emulator. Multiple C40s can be debugged via JTAG interface.

Packaged in a 325-pin ceramic PGA.

HARDWARE

SUPPORT

SOFTWARE

Development system includes in-circuit emulation via JTAG interface.

4-processor host-independent evaluation board.

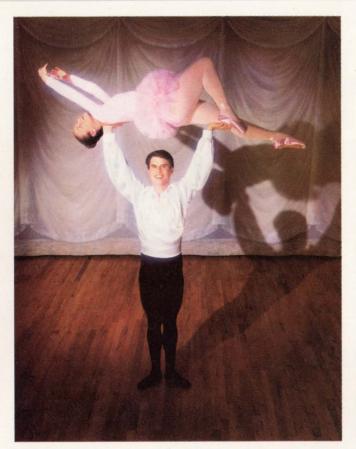
Optimizing ANSI C compiler with parallel-processing runtime support.

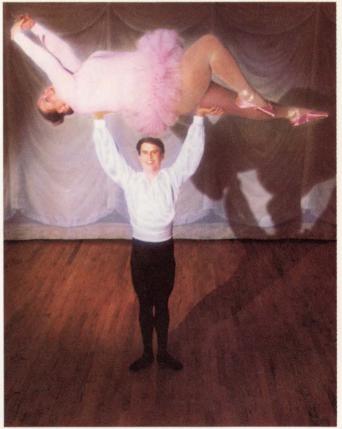
Source-level debugger. Assembler/linker.

Simulator.

Application library.

Third-party support includes Spox with drivers for parallel processing.





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15 New High Speed Op Amps.

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LT1228 is a high speed gain controlled amp with guaranteed operation down to $\pm 2V$ or 4V single supply and output swing to within 1V of the rails.

LT1122 is a JFET input op amp which slews $80V/\mu s$. LT1193 and 1194 are video differential input amplifiers with programmable or fixed gain powered from single 5V or \pm 5V supplies with \pm 50mA output drive.

Singles and duals are available in 8-pin DIP and 8-pin SOIC package, quads in 14-pin. For data sheets and a comprehensive 132 page application note contact Linear Technology Corporation, 1630 McCarthy Blvd., Milpitas, CA 95035. Or call 800-637-5545.

Parameter		1220	1224	1191	1223	1122	Units
S.R.	Slew Rate (Typ)	250	400	450	1000	80	V/µsec
G.B.W.	Gain Bandwidth (Typ)	45	45	90	100	14	MHz
t_s	Settling Time (to 0.1%) (Typ)	90	90	100	75	340*	nsec
Avol	Open Loop Gain (Typ)	50	7	45	28	450	V/mV
Vos	Offset Voltage (Max)	1	2	6	3	0.9	mV
Ios	Offset Current (Max)	0.3	0.4	1	-	.00005	μΑ
I_B	Bias Current (Max)	0.3	8	1.7	3	.0001	μΑ
en	Voltage Noise $(f = 10KHz)$	17	22	25	3.3	15	nV/√Hz
in	Current Noise $(f = 10KHz)$	3	1.5	4	2.1	.002	pA/√Hz
	Min Gain Stable	1	1	1	1	1	
Is	Supply Current (Max)	10.5	9	40	10	11	mA
li ence	Price (100's) \$ (PDIP)	3.85	2.85	2.40	2.85	2.50	

^{*12} Bit Settling Time



TOUGH PRODUCTS
FOR TOUGH APPLICATIONS.

32-BIT FLOATING-POINT CMOS DSP μP

AVAILABILITY: Now.

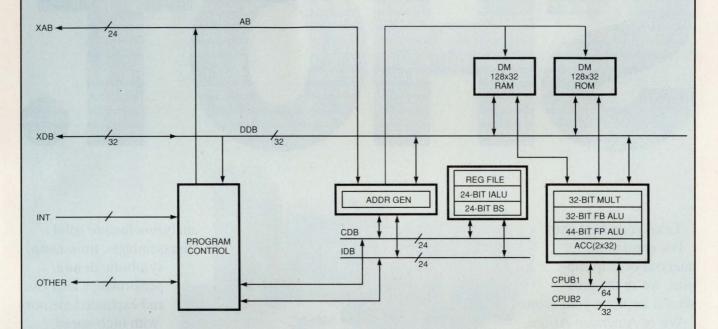
COST: 34325 (25 MHz), \$137; 34325 (20 MHz), \$124 (10,000).

SECOND SOURCE: None.

Zoran Corp 1705 Wyatt Dr Santa Clara, CA 95054 (408) 986-1314 FAX (408) 986-1240 Circle No. 686

DESCRIPTION: The ZR34325 is a vector-signal processor, which is a DSP chip that operates on complex data and large blocks of data with single high-level instructions. The instruction set includes a single instruction to calculate an FFT, FIR filter, IIR filter, and other complex functions. The highly specialized

architecture is optimized to perform these functions quickly. The architecture also eases programming because the programmer doesn't have to write code for complex DSP functions. The 32-bit floating-point data conforms to the IEEE-754 standard.



FEATURES: 80- and 100-nsec cycle-time versions.

Single address and data bus.

Vector instructions generally take longer to execute than to fetch, so little speed penalty is incurred with this simple bus architecture.

High-level instructions, such as those to calculate FFTs and FIR and IIR filters, simplify programming:

 256×32 -bit coefficient dual-port ROM and 128×32 -bit dual-port RAM on chip.

No on-chip program memory.

Internal memory can be directly accessed by external device. $16M \times 32$ -bit memory space.

No on-chip peripherals.

IEEE-754 32-bit floating-point format.

Multiplier accepts 32-bit floating-point data and creates 44-bit results.

Three ALUs: two floating point and one integer. 32-bit floatingpoint data can be added to 32 bits with one ALU and to 44 bits with the other.

24-bit bidirectional barrel shifter.

Two 32-bit accumulators.

No zero-overhead looping.

Direct, indirect, register, immediate, circular, and bit-reversed addressing modes.

Address generators for internal RAM and ROM.

On-chip DMA.

Slave mode opens chip to external access.

Hardware stack maintained in main memory.

Single external interrupt.

Hardware wait states.

No on-chip emulation port.

No low-power mode.

Packaged in an 84-pin PGA or 84-pin QFP.

HARDWARE -

SUPPORT

SOFTWARE

Hardware-development-system board. VME bus-based product for development. Third-party hardware available. Assembler/linker/simulator (MS-DOS and VAX/VMS). Application library (MS-DOS and VAX/VMS). Ada Compiler for VAX/VMS.













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Circle #44 for Logic Analyzer Information

Arium's ML4400 configurable

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Priced from \$9,785

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DESIGN IDEAS

EDITED BY ANNE WATSON SWAGER

High-frequency VCOs top 100 MHz

Di Paolo Franco Ericsson Fatme, Rome, Italy

VCOs that use surface-acoustic-wave (SAW) filters have higher operating frequencies and higher pull ranges than do circuits that use crystal oscillators. Figs 1 and 2 present two practical realizations of SAW-filter-

based VCOs. The circuits' operating frequencies are 140 and 181 MHz, respectively. The differences between the two figures stem from that fact that two types of SAW filters are available. Fig 1's circuit uses a SAW filter that has 180° of phase shift. The filter in Fig 2 has a phase shift of 0°. Both circuits draw about 20 mA and operate from a 5V supply.

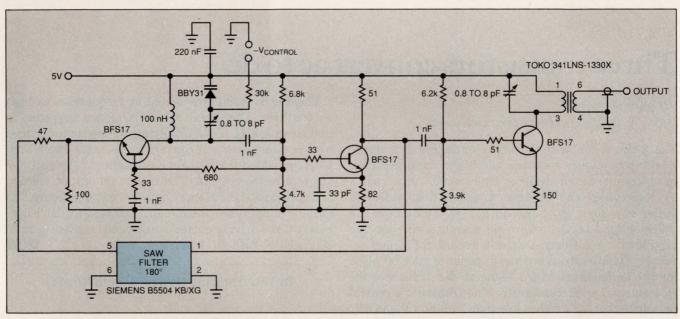


Fig 1—This oscillator is based on a 180° phase-shift SAW filter and has a free-running frequency of 140 MHz.

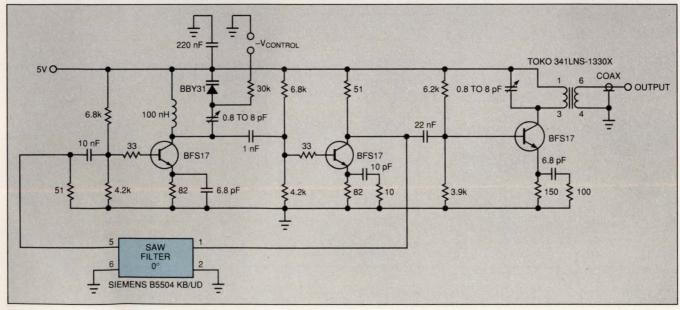


Fig 2—This oscillator is based on a 0° phase-shift SAW filter and has a free-running frequency of 181 MHz.

EDN October 1, 1991

DESIGN IDEAS

Each circuit's operating frequency is solely dependent on the SAW filter's passband center frequency, which can be higher than 1000 MHz. The SAW filters have a pull range near 500 ppm when the BBY31 varactor diode's control voltage, $V_{\rm CONTROL}$, varies by 4V.

These circuits' typical p-to-p voltage when driving a 50Ω load is 600 mV. The spectrum of the output signals is such that all the harmonics are below 25 dB with respect to the carrier. The variation with temperature when the circuits run in the free-running mode is 100 ppm, which is typical for SAW filters.

Crystal oscillators tend to be more stable over their operational frequency range than are SAW-based oscillators. However, that range is limited compared with the range of SAW-based oscillators. SAW filters are available with center frequencies starting at 120 MHz. The components cost of Fig 1 and Fig 2, without the SAW filter, is about \$1 each. SAW filters cost about \$25. EDN BBS DI #1030

To Vote For This Design, Circle No. 746

Three transistors convert ac to dc

Stephen Theobald
Bang & Olufsen, Harboøre, Denmark

The 3-transistor ac-to-dc converter in Fig 1 features a better frequency response and higher accuracy than most op-amp-based designs. The circuit runs from a 5V supply. Q_1 and Q_2 form a standard amplifier to buffer the input from the output. Q_3 bootstraps the collector load of Q_2 to provide current drive for the rectifier diodes. Current drive is essential for high accuracy. Q_2 also provides a low-impedance take-off point for the dc feedback to Q_1 . Using an RF transistor for Q_2 ensures a wide bandwidth. The transistor's critical parameter is C_{OB} , which is less than 2 pF at a V_{CE} of 2V.

The Fig 1 circuit was tested at frequencies as high as 300 kHz. The circuit's low-frequency response is limited to 1 kHz. By multiplying the capacitor values by a constant, you can convert frequencies lower than 1 kHz provided that the time constants of the rectifier stage prove acceptable. The maximum output voltage is approximately 800 mV before limiting occurs. R_1 ensures stability for the circuit. The resistor isn't necessary if the driving circuit's impedance is greater than 300Ω . EDN BBS DI #1033

To Vote For This Design, Circle No. 747

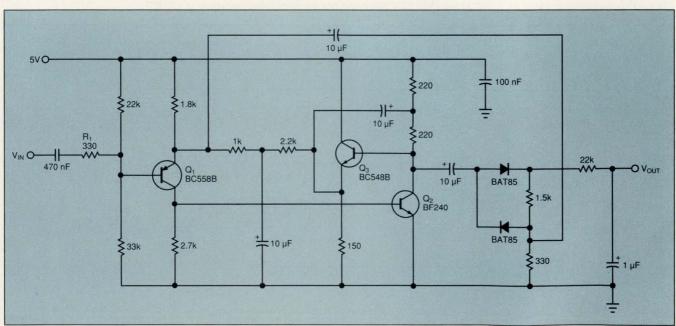


Fig 1—To ensure accuracy, Q_3 of this ac-to-dc converter bootstraps the collector load of Q_2 to provide current drive to the rectifier diodes.

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and-reel format (1500 units max, 24mm). All models are available for immediate delivery with a one-year guarantee.

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SPECIFICATIONS (typ)

	Absorptive SPDT YSWA-2-50DR ZYSWA-2-50DR			Reflective SPDT YSW-2-50DR ZYSW-2-50DR		
Frequency (MHz) Ins. Loss (dB) Isolation (dB) 1dB Comp. (dBm) RF Input (max dBm)	dc- 500- 500 2000 1.1 1.4 42 31 18 20	2000- 5000 1.9 20 22.5	dc- 500 0.9 50 20	500- 2000 1.3 40 20	2000- 5000 1.4 28 24 26	
VSWR "on" Video Bkthru (mV,p/p)	1.25	1.35	1.5	1.4	1.4	1.4
Sw. Spd. (nsec) Price, \$ YSV			3 in) 23.95 A) 69.95		3 -2-50DR (2-50DR (SI	

CIRCLE NO. 71

P.O. Box 350166, Brooklyn, New York 11235-0003 (718) 934-4500 Fax (718) 332-4661 Telexes: 6852844 or 620156

NEW PRODUCTS

SOFTWARE DEVELOPMENT TOOLS

Data-Transfer Program

- Converts Macintosh to DOS
- Requires no hardware or software modifications

The PC version of Common-Link, Mac-In-DOS, lets you format Macintosh disks in your IBM PC or compatible disk drive. The software runs under Microsoft Windows 3.0. No special hardware is needed to perform conversions. The software shows listings of two directories of files side by side on the screen. On one side are the Mac files resident on a Mac disk in the drive; on the other side are the DOS files in a selected directory on the hard drive or on a disk in another drive. Files are copied from one side to the other; conversions take place automatically. Because Mac files have three parts and DOS files have one, during Mac to DOS transfers, tutorial notes pop up with prompts to let the user select the appropriate conversion level. In DOS-to-Mac transfers, the DOS files are placed in a dummy Mac file. The software comes on a DOS disk and is loaded on the DOS computer. No hardware modification is needed for either machine, but both machines must have 1.44-Mbyte disk drives. \$199.

Pacific Micro, 201 San Antonio Circle C250, Mountain View, CA 94040. Phone (415) 948-6200. FAX (415) 948-6296. Circle No. 351

C Compiler And Source-Level Debugger

- Connect DOS or Unix computer to target hardware
- Software provides source-level debugging on target system

The Crosscode C compiler and Freeform source-level debugger are tailored specifically for Motorola MVME-165 VME CPU and 6800-series evaluation boards. The tools provide source-level debugging directly on the target system. The de-

bugger includes a transparentmonitor program for the evaluation boards. The monitor can retrieve the target system's register contents and other information for the debugger, thereby eliminating the need for a hardware emulator. You can use the debugger to connect any MS-DOS or Unix computer directly to the target hardware through an RS-232C cable. The tool can debug fully optimized code in real time and can run on a laptop. It is integrated with the compiler; the compiler includes an ANSI-standard C compiler, a macro relocating assembler, linker, librarian, download, symbol listing routines, and startup routine. The tools come bundled together. \$3490.

Software Development Systems Inc, 4248 Belle Aire Lane, Downers Grove, IL 60515. Phone (708) 971-8170. Circle No. 352

Visual Programming Tool

- Object-oriented, visual system
- Imports C, Pascal, Fortran code This version of Prograph 2.5 can graph code, including interfaces. It allows you to import existing C, Pascal, or Fortran code and build interactive front ends to existing applications. It incorporates a database engine for multiuser access to tables, indices, and data types. The software is compatible with the Macintosh System. The system lets you define program classes and modules graphically. Modules are defined as data-flow diagrams, using processing nodes. Prograph has an interface builder for the automatic generation of interface objects from a set of supplied System Classes. Prograph 2.5, \$495; C and Pascal interfaces. \$75 each; Fortran interface, \$149.

TGS Systems, 2745 Dutch Village Rd, Suite 200, Halifax, Nova Scotia, Canada B3L 4G7. Phone (902) 455-4446. Circle No. 353

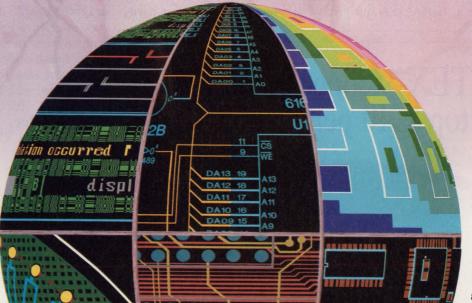
Memory-Management Software

- Manages multiple memory resources
- Compatible with MS- and PC-DOS

386Max and Bluemax memorymanagement tools are compatible with MS-DOS and PC-DOS. The tools enhance DOS's abilities by providing advanced automatic memory configuration and optimization. The software provides expanded and extended memory compatibility with LIM EMS 4.0, XMS 2.0, VCPI, and VDS. The software recovers available memory resources and automatically relocates resident software into previously unused memory regions. Automatic ROM caching improves system performance. Video RAM and ROM, other adapter RAM and ROM, and the system ROM BIOS are located within the reserved-memory region. Both tools automatically recover the monochrome area of DOS memory. The 386Max identifies and recovers unused filler patterns within the ROM BIOS: Bluemax automatically compresses the PS/2 BIOS and provides an additional 80 kbytes of contiguous reserved-memory RAM. Both tools configure Micro Channel Architecture adapters. The tools also perform ROM caching and resident software instancing and can swap the fastest system memory into the first megabyte of memory. The tools require 1 kbyte of memory. The tools come bundled with the ASQ system analyzer and memory-management tutorial and the 386Cache disk-cache program. The cache program loads its executable DOS into high DOS while leaving track buffers in conventional memory. 386Max, \$130; Bluemax, \$155.

Qualita Inc, 7101 Wisconsin Ave, Suite 1386, Bethesda, MD 20814. Phone (301) 907-6700. FAX (301) 907-0905. **Circle No. 354**

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NEW PRODUCTS

COMPUTERS & PERIPHERALS

Industrial 80486 Single-Board Computer

- Has eight SIMM sockets for as much as 32 Mbytes of DRAM
- Operates at 25 or 33 MHz

The QPC-5160 single-board computer (SBC) for a passive ISA bus

backplane contains an Intel 25- or 33-MHz 80486 μP . It also has eight SIMM (single-inline-memory-module) sockets for as much as 32 Mbytes of dynamic RAM (DRAM). Memory options are 1, 2, 4, 8, 16, or 32 Mbytes. In addition, the hard-

ware supports the LIM 4.0 specification. You can expand the memory to 64 Mbytes, using a piggy-back daughter board. The SBC's DRAM features page-mode and 2-way interleaved access modes, and the daughter-board's memory has a 4-way interleaved access mode. The company designed the SBC to withstand harsh industrial conditions. The board also features a shadow RAM. Board with 4 Mbytes of DRAM (25 MHz), \$3795; (33 MHz), \$4195.

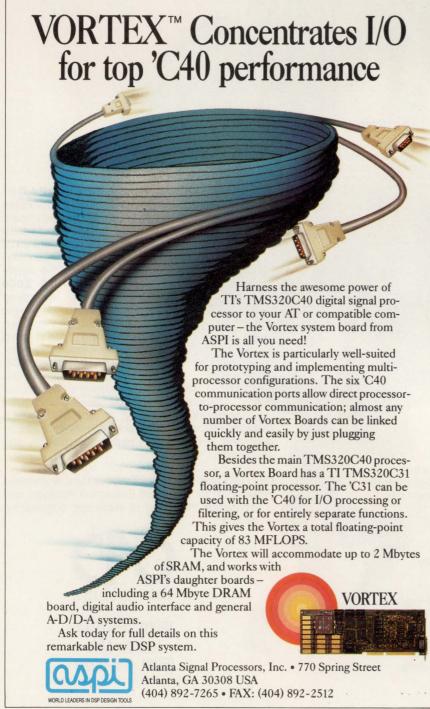
Qualogy Inc, 109 Bonaventure Dr, San Jose, CA 95134. Phone (408) 434-5200. Circle No. 355



QIC Tape Drives

- Connect to SCSI port on Macintosh computers
- Have capacities ranging from 150 to 525 Mbytes

The latest models of the Panther Tape Backup System are compatible with Apple's Macintosh Macplus, SE, SE 30, MAC II, IICX, IICI, and portable computers. Because the 51/4-in. drives employ the SCSI bus, you can attach them directly to the computer's SCSI port without using a host adapter board. The drives have capacities ranging from 150 to 525 Mbytes. The 525-Mbyte model can back up the entire tape in less than 45 minutes. Backup and restore rates range from 5 Mbytes/minute to 12 Mbytes/minute. The drives perform file-by-file and image backups, and they are compatible with the A/UX operating system. The



units use DC 6000 or equivalent tape medium, and the MTBF is 80,000 hours. Bit error rate is less than 10⁻¹⁵. 150-Mbyte drive, \$2145; 525-Mbyte drive, \$2695.

Tandberg Data Inc., 2649 Townsgate Rd, Suite 600, Westlake Village, CA 91361. Phone (805) 495-8384. Circle No. 356 that's expandable to 128 kbytes. You can install as much as 32 Mbytes of dynamic RAM, using single inline memory modules. The board has eight 16-bit ISA bus expansion slots and a socket for an 80387 coprocessor. A shadow RAM for the system BIOS and video BIOS increases the execution speed as much as three times. The

mother board runs Windows, OS/2, MS-DOS, Unix, Xenix, and Novell software. Performance figures include a 63.6 Landmark Speed (1.14), 8.55 Power Meter MIPS (1.5), and a Norton SI rating (4.5) of 48. \$855.

Pioneer Computer Inc, 49066 Milmont Dr, Fremont, CA 94538. Phone (415) 623-0808. Circle No. 358



386 Personal Computer

- Employs AMD's 40-MHz 80386 µP
- Has 4 Mbytes of DRAM and one 64-kbyte cache RAM

The 386WB-40SL ISA bus personal computer employs AMD's 40-MHz 80386 µP. The computer comes with 4 Mbytes of dynamic RAM, a 200-Mbyte hard-disk drive, a 14-in. super VGA monitor, a 1-Mbyte VGA Freedom Card, and 64 kbytes of cache RAM. The RAM is expandable to 64 Mbytes. In addition, the computer has FCC Class B approval, a parallel port, and two serial ports. Other features include a mouse, and DOS 4.01 and Windows 3.0 software. A 6month GE on-site service contract, which is optionally expandable to five years, is also available. \$2999.

Bell Computer Systems, 6615 Valjean Ave, Van Nuys, CA 91406. Phone (818) 909-3501. Circle No. 357

80386 Mother Board

- Employs AMD's 40-MHz 80386 μP
- Has 64-kbyte cache RAM expandable to 128 kbytes

The 386 Cache 40 Mini-AT mother board uses AMD's 40-MHz 80386 μ P. It has 64 kbytes of cache RAM

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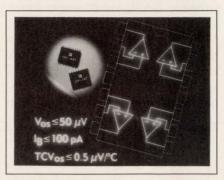
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201 Broadway Cambridge, MA 02139 USA

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NEW PRODUCTS

INTEGRATED CIRCUITS

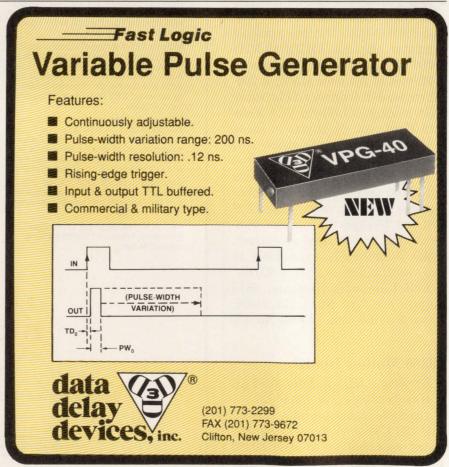


Quad Op Amp

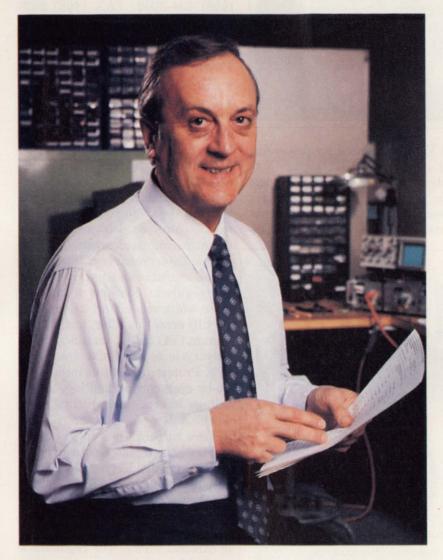
- Offset voltage is 50 μV
- Bias current is 100 pA

According to the company, the OP-497 is the industry's highest precision quad op amp. Guaranteed specifications at 25°C include 50 μV maximum offset voltage with offset drift of 0.5 $\mu V/^{\circ}C;$ maximum bias current of 100 pA (450 pA at 125°C), and 2000V/mV minimum open-loop

gain. The maximum per-channel supply current is 625 µA. The low offset voltage and high gain eliminate offset trims and additional gain stages in many designs. The superbeta input stage includes biascurrent cancellation circuitry that maintains low (pA) bias current over the full operating temperature range. This action contrasts with traditional FET-input amplifiers whose bias current is initially low but typically doubles for every 10°C rise in temperature. Other features include a supply-voltage operating range of ± 2 to ± 20 V, and a 120-dB PSRR and CMRR. The commonmode range extends to within 1V of the operating supply. The quad op amp is available in industrial and military temperature ranges. Package options include 14-pin plastic



"We saved over \$19,000 at the demo!"



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"The microfilm system we purchased for IC and semiconductor search and selection just wasn't working out. It was hard to use and there weren't enough people using it to justify the cost. So, we decided to evaluate CD-ROM-based systems.

"While all this was happening, our purchasing people found a new IC vendor. They wanted to know if the new vendor made equivalents for some of our most commonly-used components. They thought we could get a better price. It would take us hours to find equivalents on the microfilm system, so we decided to challenge a couple of new CD-ROM-based systems.

"The first demonstration was a flop. Their system didn't even include the new vendor. Needless to say, we weren't impressed.

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— Frank Lucas Test Engineering Manager Welch Allyn Data Collection Division



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DIP, 14-pin ceramic DIP, 16-pin SOIC, and 20-contact LCC. OP-487GP in 14-pin plastic DIP specified for industrial range, \$4.75 (100).

Analog Devices, PMI Div, 1500 Space Park Dr., Santa Clara, CA 95052. Phone (408) 727-9222.

Circle No. 359

SONET Chip Set

- For STS-3 and STS-12 applications
- Satisfies both SONET and SDH requirements

This 3-piece chip set, consisting of the VP15301, VP15311, and VP15323, satisfies both SONET (Synchronous Optical Network) and SDH (Synchronous Digital Hierarchy) standards. Optimized primarily for STS-3 and STS-12 applications at 155 Mbps and 622 Mbps, respectively, the chip set is usable

at other standardized rates and has been tested to comply with ANSI, CCITT, and Bellcore standards. The VP15301 is used for terminating the section overhead of SONET data streams. The VP15311 is used for terminating line overhead, and



the VP15323 is used for processing and aligning SONET payloads to system timing. The VP15323 can also process concatenated data streams for handling asynchronous transfers and for SDH compatibility. Package options, which vary by chip and application, include an 84pin plastic leaded chip carrier, a 144-pin plastic pin-grid array, and a 160-pin plastic quad flatpack. VP15301, VP15311 and VP15323, from \$56, \$90, and \$69, respectively (2000).

VLSI Technology, 1109 McKay Dr, San Jose, CA 95131. Phone (408) 434-3000. FAX (408) 263-Circle No. 360 2511.

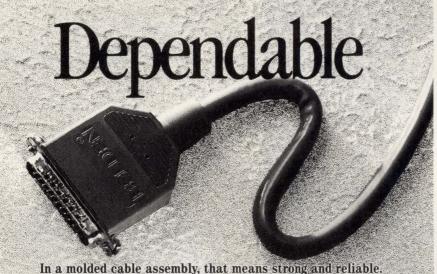
Power Switching Regulator

- Output switch handles 5A
- Duty cycle is adjustable

Featuring an output-switch rating of 5A, the MC34167 switching regulator comes in a 5-lead TO-220 power package, which simplifies heat sinking. The regulator operates at a fixed frequency of 72 kHz. Because the timing components are on the chip, you don't need an external resistor and capacitor to set the oscillator frequency. In addition to the oscillator and on-chip timing, the regulator contains a latching pulse-width modulator, a high-gain (80 dB) error amplifier, and a highcurrent (5A) output transistor. The duty cycle is adjustable from 0 to 95%. Protective features include cycle-by-cycle current limiting, undervoltage lockout, and thermal shutdown. A low-power standby mode reduces current drain to 36 µA. In addition, the regulator has an internal resistor divider, which sets the output at a nominal 5.05V, eliminating the need for an external divider and providing an extra 50 mV to compensate for a 1% voltage drop in external wiring. The regulator is available in two temperature ranges; the MC34167T for 0 to 70°C operation, and the MC33167T for -40 to +85°C operation. MC34167T. \$2.03; MC33167T, \$2.19 (10,000). Delivery, stock to six weeks ARO.

Motorola Inc, EL340, 2100 E Elliot Rd, Tempe, AZ 85284. Phone (602) 897-3615. FAX (602) 897-4193.

Circle No. 361



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NEW PRODUCTS

TEST & MEASUREMENT INSTRUMENTS

Enhancement For Jitter-Spectrum Analyzer

- Unit computes spectra of jitter in time measurements
- Instrument requires no external computer

When equipped with Option 040, the HP 5372A modulation-domain analyzer uses FFT techniques to determine the frequency spectrum



of the jitter in a series of time measurements. The unit requires no external computer and works with jitter that has a bandwidth as high as 2 MHz. When the data stream is nonrepetitive, the analyzer does not require a clock. HP 5372A, \$30,000. Option 040, \$2000 (if installed by factory in new analyzer). Option 040 field upgrade for existing analyzers, \$3000.

Hewlett-Packard Co, 19310 Pruneridge Ave, Cupertino, CA 95014. Phone (800) 752-0900. Circle No. 365

68HC11 Emulators

- Interface to MS-DOS PCs via 115.2-kbps RS-232C link
- Work with \u03c4Ps that generate a 3.3-MHz E-clock

There are two versions of the Icemaster 68HC11 in-circuit emulator: The Model 200 is a basic emulator: the Model 400 contains all of the basic unit's features and a 4k frame trace buffer, two real-time performance analyzers, and watchdog-timer support. Both emulators work with 68HC11s that generate a 3.3-MHz clock. You connect the instruments to an MS-DOS PC via an RS-232C link that supports host communica-



tion at speeds to 115.2 kbps. Both models have trace-on and trace-off triggers, 64 kbytes of emulation memory, 64k hardware breakpoints, and 64k write-access triggers. The emulators include symbolic and source-level debuggers that display dynamically annotated code in a source window. Model 200, \$1999; Model 400, \$4199; probe cards, from \$599.

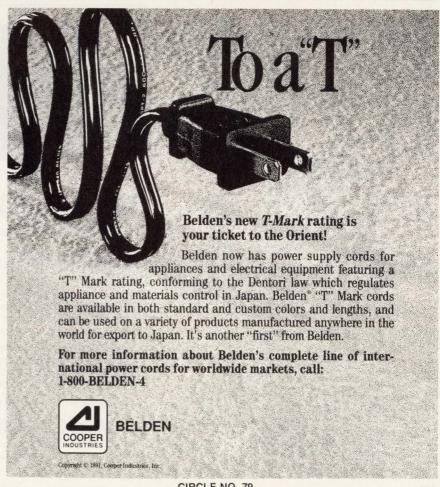
Metalink Corp. Box 1329, Chandler, AZ 85244. Phone (602) 926-0797. Circle No. 366

Pocket-Size 3.5-GHz Counter

- Operates as long as five hours from NiCd battery
- Measures $3.4 \times 3.8 \times 1$ in. and weighs 9 oz

The Model 3500 8-digit, 3.5-GHz frequency counter operates as long as five hours from a rechargeable NiCd battery. The unit, which offers a display-hold function, will operate while connected to its battery charger. Input resistance is 1 $M\Omega$ to 12 MHz; a second 50Ω input works from 10 MHz to 3.5 GHz. You can choose among three gate times, the longest of which gives 0.1-Hz resolution at 12 MHz. \$3500.

Startek International Inc, 398 NE 38th St. Fort Lauderdale, FL 33334. Phone (305) 561-2211. FAX (305) 561-9133. Circle No. 367



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CIRCLE NO. 80

NEW PRODUCTS

COMPONENTS & POWER SUPPLIES



Expansion Chassis

- Designed for EISA systems
- Includes a backplane

The PX1591 expansion chassis is designed for EISA/ISA systems. It includes a 13-slot, rack-mountable

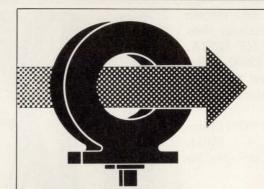
passive backplane and a 200W modular power supply. It also includes an expansion card module and one expansion card with the cables necessary to extend from the PCXI chassis to EISA/ISA desktop or rackmount PCs. The chassis provides EMI/RFI shielding, vibration protection, and industrial cooling with filtered fans. The unit accommodates as many as 10 function cards. \$2395.

Rapid Systems Inc, 433 N 34th St, Seattle, WA 98103. Phone (206) 547-8311. Circle No. 362

Voltage Suppressors

- Will handle 300A
- Respond in 1 nsec max

Transguard multilayer-ceramic, transient-voltage suppressors have



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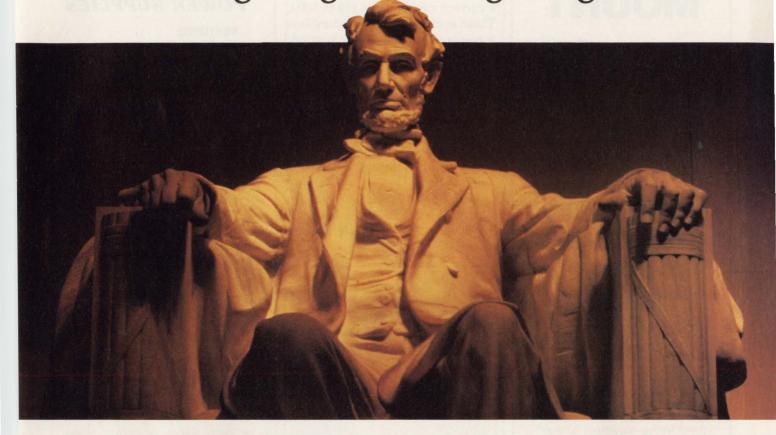
With a Pearson current monitor and an oscilloscope you can make precise amplitude and waveshape measurement of ac and pulse currents from milliamperes to kiloamperes. Currents can be measured in any conductor or beam of charged particles, including those at very high voltage levels.

A typical model gives an amplitude accuracy of +1%, -0%, 20 nanosecond rise time, droop of 0.5% per millisecond, and a 3 db bandwidth of 1 Hz to 35 MHz. Other models feature 2 nanosecond rise time, or a droop as low as 1% per second.

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1860 Embarcadero Road, Palo Alto, Calif. 94303, U.S.A. Telephone (415) 494-6444 · Telex 171-412 · FAX (415) 494-6716 Announcing a night to recognize greatness



EDN's Innovation and Innovator of the Year Awards Ceremony

n the night of November 19 during Wescon, EDN will present the 1991 Innovation and Innovator of the Year awards at the Mark Hopkins Hotel in San Francisco. You are invited to show the finalists that you support greatness in innovation by attending the awards ceremony that is the culmination of their hard work. Through its Innovation Crusade, EDN hopes to inspire

engineering professionals fact, select the winners, within the electronics you show commitment to quality and creativity plateaus of inspiration and creativity. fact, select the winners, you show commitment to quality and creativity in electronics and are driving this crusade. Bu

The dedication and involvement of EDN readers, like yourself, have made the Innovation Crusade and awards ceremony a reality. By taking the time to nominate your peers and, in

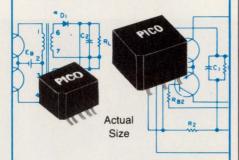
fact, select the winners, you show commitment to quality and creativity in electronics and are driving this crusade. But don't stop there ... order your ticket to the industry event of the year and show these innovators that greatness does not go unrecognized. All proceeds of the dinner will be donated to the EDN Scholarship Fund.

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These units have gull wing construction which is compatible with tube fed automatic placement equipment or pick and place manufacturing techniques. Transformers can be used for self-saturating or linear switching applications. The Inductors are ideal for noise, spike and power filtering applications in Power Supplies, DC-DC Converters and Switching Regulators.

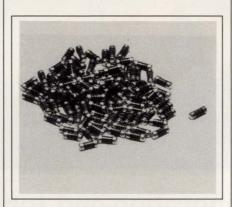
- Operation over ambient temperature range from -55°C to +105°C
- All units are magnetically shielded
- All units exceed the requirements of MIL-T-27 (+130°C)
- Transformers have input voltages of 5V, 12V, 24V and 48V. Output voltages to 300V.
- Transformers can be used for self-saturating or linear switching applications
- Schematics and parts list provided with transformers
- Inductors to 20mH with DC currents to 23 amps
- Inductors have split windings



COMPONENTS & POWER SUPPLIES

a current capability of 150 to 300A. These surface-mount varistors have a response time of 1 nsec max and are available in a variety of package sizes. These low-voltage devices have a circuit-operation capability ranging to 60 working volts. Clamping-voltage figures range from 15.5 to 30V. Transient-energy figures span a 0.3 to 1.2J range. \$0.45 to \$0.55 (1000). Delivery, six to eight weeks ARO.

AVX Corp, 3900 Electronics Dr, Raleigh, NC 27604. Phone (919) 878-6200. **Circle No. 363**



Surface-Mount Resistors

- Rated for 250 mW
- Have a 0.1% tolerance

SMM0204 MELF-type surfacemount resistors are rated for 250 mW at 70°C. Resistance values range from 1.2Ω to $2 M\Omega$ and tolerances range from 0.1 to 5%. Temperature coefficients vary from ± 15 to ±100 ppm/°C depending on resistance value and tolerance. The resistors measure 0.142×0.059 in. and have end caps that are reflow and wave solderable. The units are color-banded for easy identification and are available on 8-mm tape-andreel or bulk packaging. $10-k\Omega$ units with a 1% tolerance and a ± 50 ppm/ °C temperature coefficient, \$0.023 (10,000). Delivery, stock to six weeks ARO.

Dale Electronics Inc, 2300 Riverside Blvd, Norfolk, NE 68701. Phone (402) 644-4247.

Circle No. 364



UNIVERSAL VOLTAGE POWER SUPPLIES

FEATURES:

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HIGH EFFICIENCY
BUILT-IN- EMI FILTER
LOW OUTPUT RIPPLE
OVER VOLTAGE AND
SHORT CIRCUIT PROTECTION
SMALL FOOT PRINT



FOR NOTEBOOK PC

WATTS	MODEL	O/P1	O/P2	O/P3	O/P4	DIMENSION
30 W	PSA-093	9.5V/3A				149×75×45H
	PSA-161	16.5V/1.8	A			
	PSA-181	18V/1.65A				
	(7 MODELS)					
40W	PSA-4641	18V/1.4A	CHARGE	R 1A		166×80×45
	(3 MODEL)					
50W	PSA-124	12V/4.2				166×80×54
	PSA-242	24V/2.2A				
	CONTRACTOR OF THE					

FOR PC, HARD DISK & FLOPPY DISK DRIVES, INDUSTRIAL, TELECOMMUNICATION

WATT	IS MODEL	O/P1	O/P2	O/P3	O/P4	DIMENSION
40W	PSA-4031	5V/3V	12V/2A	-12V/0.5	5A	127×76×30
	PSA-4005	5V/6A				
	(8 MODELS)				
50W	PSA-5031	5V/5A,	12V/2.5A	-12V/0.5	5A	160×100×45
	(3 MODELS)				



ENSION	DIMEN	O/P3 O/P4		O/P1 O/P2		WATTS MODEL O	
80×48	144×80	5A	-12V/0	12V/2A	5V/4A,	PSA-5231	50W
•	1443	5A	-12V/0	12V/2A	5V/4A.	PSA-5231	50W

WALL	3 MODEL	OFI	O/FZ	OFF	OILA	DIMERION
150W	PSA-1500U	5V/15A	-5V/1A	12V/1A	12V/5A	198×97×38
	PSA-1503U	5V/30A				
	PSA-1509U	5V/15A	-5V/1A,	-12V/1A	12V/5A	1
	(10 MODELS	6)				
200W	PSA-2041U	5V/25A	-5V/2.5A	-12V/2.5	A12V/5A	203×114×51
	(3 MODELS)					

SAFETY:

- * ALL APPROVED BY UL/CSA/TUV (PSA-2041 IS IN PROCESS)
- * PSA-40XX AND PSA-50XX APPROVED BY UL/CSA/TUV/VDE



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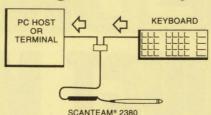
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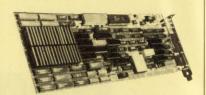
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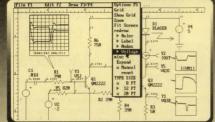
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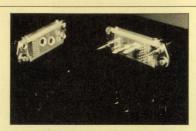
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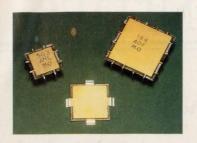
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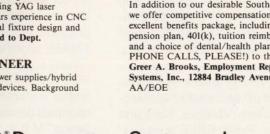
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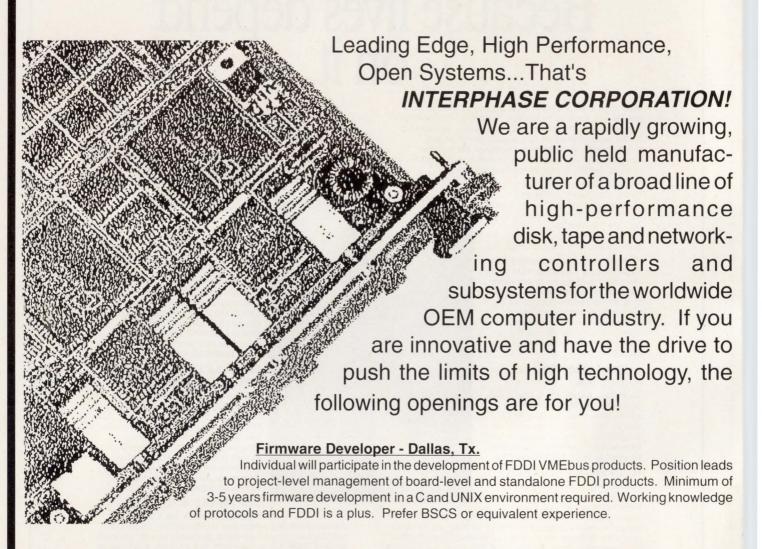
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Senior Hardware Design Engineer - Dallas, Tx.

Candidate will design and simulate ASIC devices and interface to ASIC vendors. Minimum of 3-5 years experience in board-level design and high speed CMOS design using ASIC technologies (gate array or standard cell). Knowledge and use of schematic capture, logic simulation and fault simulation tools (Verilog and/or Synopsys) desired. Working knowledge of μP and related architecture required. Disk, communication, VMEbus, Sbus and EISA bus experience are pluses. Prefer BSEE or equivalent experience.

Product Marketing Manager - Dallas, Tx.

Senior level candidate who can: formulate strategic plans, develop markets and size markets for *INTERPHASE's* EISA products, technologies, and protocols. Represent *INTER-PHASE* at various national and international forums, committees and working groups. Act as Product Line Champion within the corporation. 8-10 years applicable engineering and/or marketing experience with VAR, VAD, and dealer channels desired. Prefer BSEE, BSCS or equivalent experience. M.B.A. is a plus.

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Applications Engineer - Dallas, Tx.

Individual will provide second level technical assistance for customers and liaison between Customer Service and Engineering. Will maintain an in-depth product and system knowledge in order to identify and solve software and hardware problems. Assemble hardware, generate test scripts or programs (C, assembler, or shell language), and modify software drivers. Minimum of 3 years experience with C in an UNIX environment required. Systems administration experience a plus. Prefer BSCS or equivalent experience.

Systems Administrator - Dallas, Tx.

Candidate will be responsible for the administration of Engineering Service's UNIX based workstation network. Primary duties will involve VALID systems administration, training engineers, developing and maintaining on-line help, writing behavior models in C, supporting schematic entry, component packaging and simulation. Minimum of 2 years experience with UNIX, O/S administration, C programming, shell programming and networking required. Experience with PC-NFS, modeling and simulation desired. Prefer BSEE, BSCS or equivalent experience.

Software Engineer - Dallas, Tx.

Candidate will develop device drivers for various *INTER-PHASE* products. Experience with UNIX, Kernal I/O, TCP/IP or other protocol experience on super-minicomputer or mini-computer required. Minimum five years writing UNIX device drivers required. BSCS required. MSCS preferred.

Networking Programmer - Mountain View, Ca.

Individual will participate in the development of networking coprocessor products in a real-time environment. 3 years experience developing networking software in a real-time UNIX environment required. Working knowledge of TCP/IP, UDP and NFS/RPC desirable. Prefer BSCS, BSEE or equivalent experience. MSCS or MSEE a plus.

Software Performance Engineer - Mountain View, Ca.

Candidate will benchmark and test networking products as well as interface with all OEMs/customers regarding performance issues. Minimum of 5 years experience with UNIX and C programming and 2 years of performance evaluation and benchmarking. Prefer BSCS, BSEE or equivalent experience. MSCS or MSEE a plus.

Software Engineer - Mountain View, Ca.

Individual will install and patch install product related utilities, network management agents and user interfaces. Minimum of 3 years UNIX and C programming required. Experience with Bourne shell scripts, sed, awk, and systems administration desired. Exposure to NFS a plus. Prefer BSCS or equivalent experience. MSCS is a plus.

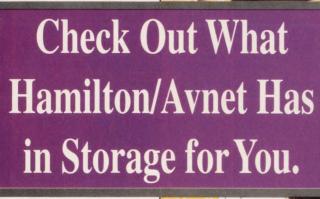
Systems Programmer - Mountain View, Ca.

Candidate will be resposible for integration of networking products into System V, Release 4 (VR4). VR4 driver experience and networking driver experience required. Knowledge of protocols is desired. Minimum of 4 years experience required. Prefer BSCS, BSEE or equivalent experience. MSCS is a plus.

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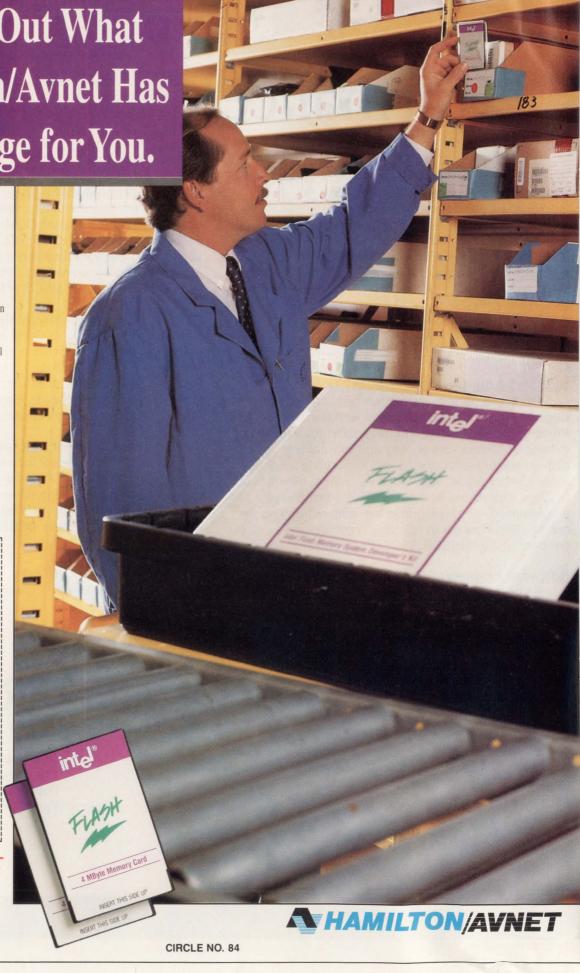
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