A CAHNERS PUBLICATION

OCTOBER 11, 1990

EDN®

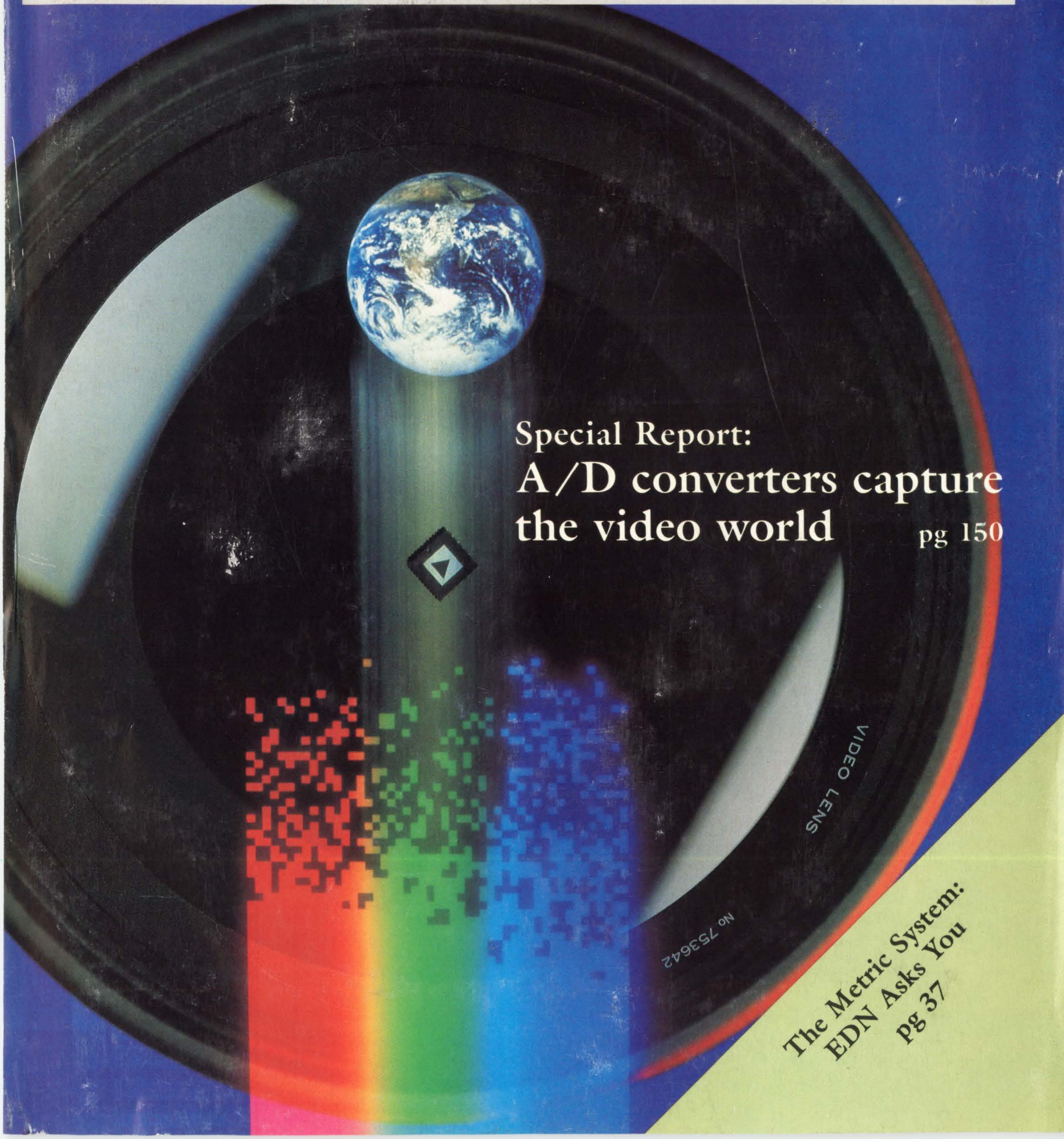
Software adds logic to make designs testable pg 59

Electronica to stress SMT and power electronics pg 112

DSP-chip directory pg 171

Real-time programming series—Part 3 pg 223

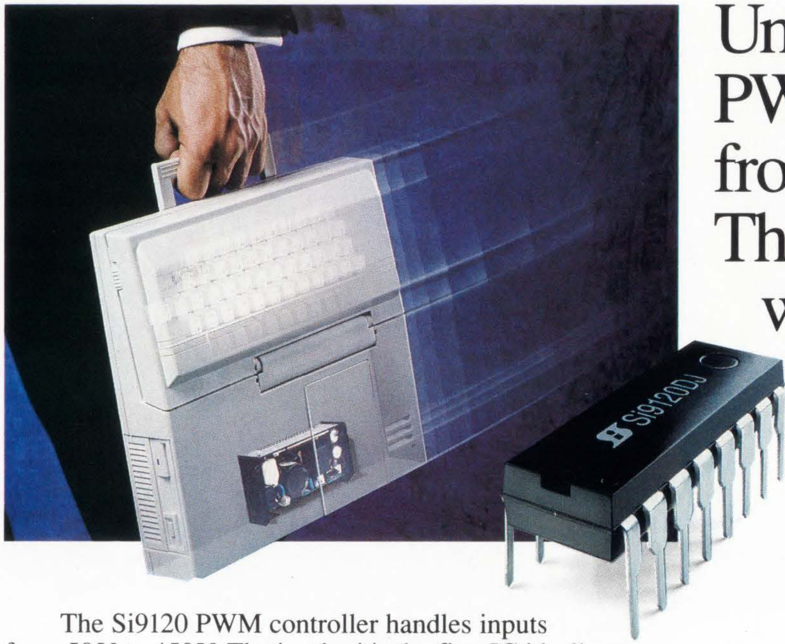
ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS



Special Report:
A/D converters capture the video world pg 150

The Metric System:
EDN Asks You
Pg 37

Get a handle on power supply design.



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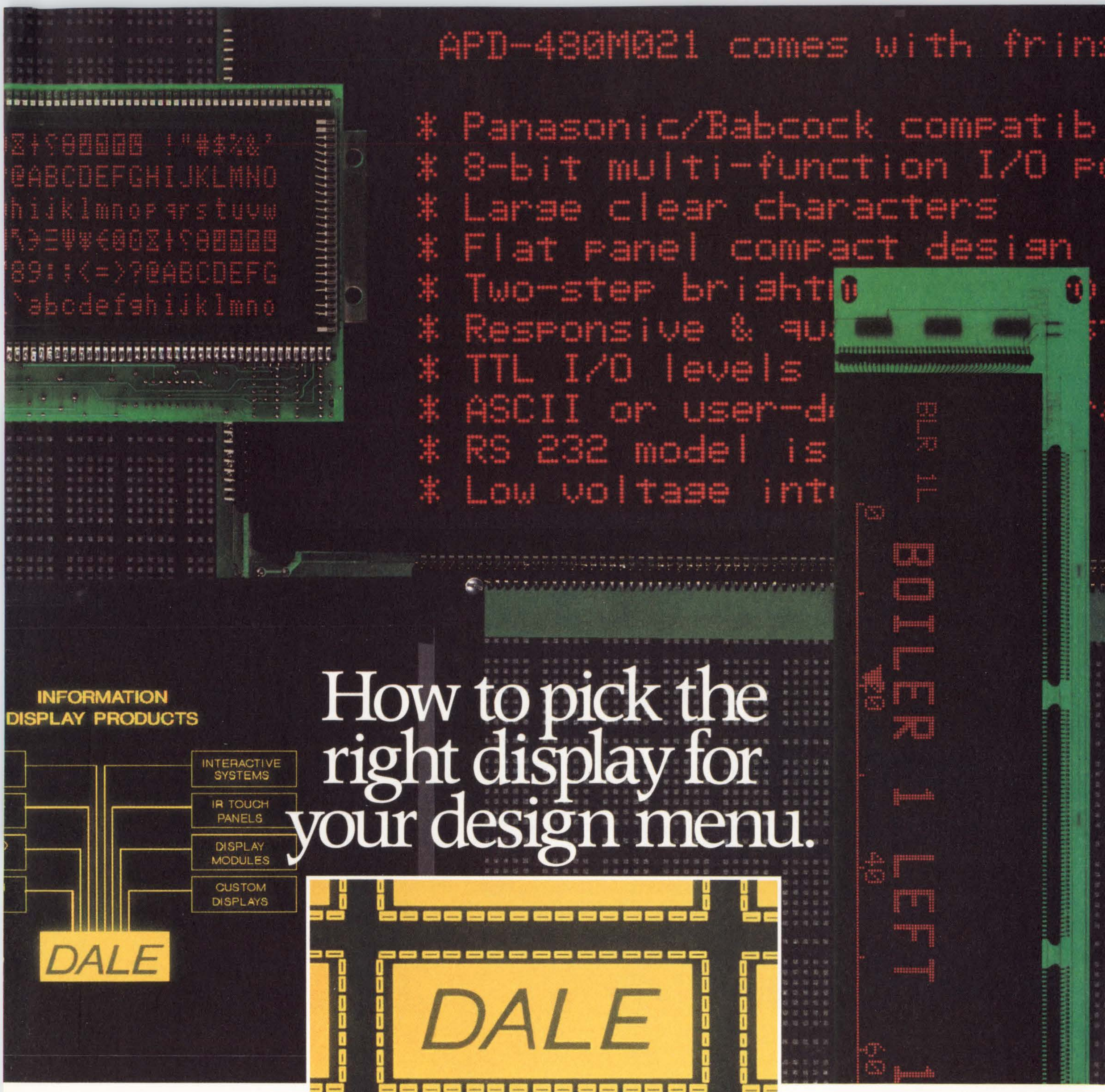

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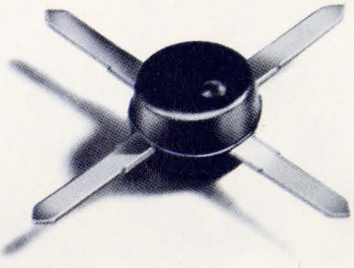

dc to 2000 MHz amplifier series

SPECIFICATIONS

MODEL	FREQ. MHz	GAIN, dB 100 MHz	1000 MHz	2000 MHz	Min. (note)	• MAX. PWR. dBm	NF dB	PRICE $ Ea.	Qty.
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MAR-2	DC-2000	13	12.5	11	8.5	+3	6.5	1.50	(25)
MAR-3	DC-2000	13	12.5	10.5	8.0	+8□	6.0	1.70	(25)
MAR-4	DC-1000	8.2	8.0	—	7.0	+11	7.0	1.90	(25)
MAR-6	DC-2000	20	16	11	9	0	2.8	1.29	(25)
MAR-7	DC-2000	13.5	12.5	10.5	8.5	+3	5.0	1.90	(25)
MAR-8	DC-1000	33	23	—	19	+10	3.5	2.20	(25)

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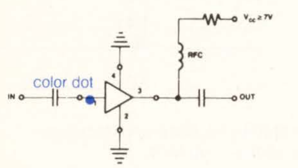

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EDN Magazine Edition®

Volume 35, Number 21

October 11, 1990

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

On the cover: *Today's video A/D converters are cheap, accessible, and offer greater performance levels than ever before. See the Special Report on pg 150. (Photo courtesy Analog Devices Inc; photography by Bryce Flynn)*

SPECIAL REPORT

Video A/D converters — 150

Choosing and incorporating a video A/D converter requires as much knowledge about video signals and digital video systems as it does about the converter itself. These video systems dictate the strict linearity requirements that converters must meet. *—Anne Watson Swager, Regional Editor*

DESIGN FEATURES

EDN's DSP-chip directory — 171

DSP μPs continue to become faster, cheaper, and more abundant. The recent availability of high-quality software tools eases debugging and maintaining your software today. And soon, parallel processing will let you achieve supercomputer performance.*—David Shear, Contributing Editor*

EEPROMs enhance microcontroller-based system performance — 213

The ability to update either the program memory or the data memory in an EEPROM can increase the performance of microcontroller-based systems, ease system-reconfiguration tasks, and improve overall flexibility.*—Richard Orlando, Xicor Inc*

Real-time programming—Part 3 — 223

To design a real-time application, you must prepare a requirements model for your system and then transform it into an implementation model. Part 3 of this series explains how to create verbal and graphical requirements models that formulate system behavior as clearly, completely, and correctly as possible.*—David L Ripps, Industrial Programming Inc*

Continued on page 7

BPA ABP

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EDN Magazine Edition®

October 11, 1990

***Large-area flat-panel displays** have found a home in a variety of computer, medical, and military applications. Manufacturers of the various display types are now vying for control of the market (pg 79).*

TECHNOLOGY UPDATES

Test-logic synthesis: Software adds logic to make designs testable **59**

Test-logic synthesis tools may not cause the barrier between design and test to crumble like the Berlin Wall, but at least the software will add some doors and windows to it.—*Michael C Markowitz, Associate Editor*

Large-area flat-panel displays: Diverse technologies vie for dominance **79**

A clear-cut winner has not yet emerged in the race to dominate the market for large-area flat-panel displays. Liquid-crystal types appear to be leading the pack—at least for now.—*Dave Pryce, Associate Editor*

Optoelectronic devices: Improvements unleash new application areas **95**

The current crop of optoelectronic devices offers better performance and wider operating capabilities than the components that were available even a year ago. As a result, you may now be able to replace your mechanical sensors and transformers with solid-state emitters and detectors.—*J D Mosley, Regional Editor*

Show preview: Electronica 90 **112**

This year's show will stress SMT, ASICs, and power electronics.—*Raymond Boult*

PRODUCT UPDATES

VMEbus and IBM PC NTDS interface boards **133**

Alternating voltage DVM **137**

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EDITORIAL 49

The combination of a PC and Windows 3.0 makes the small-computer market look bright despite today's sluggish electronics market.

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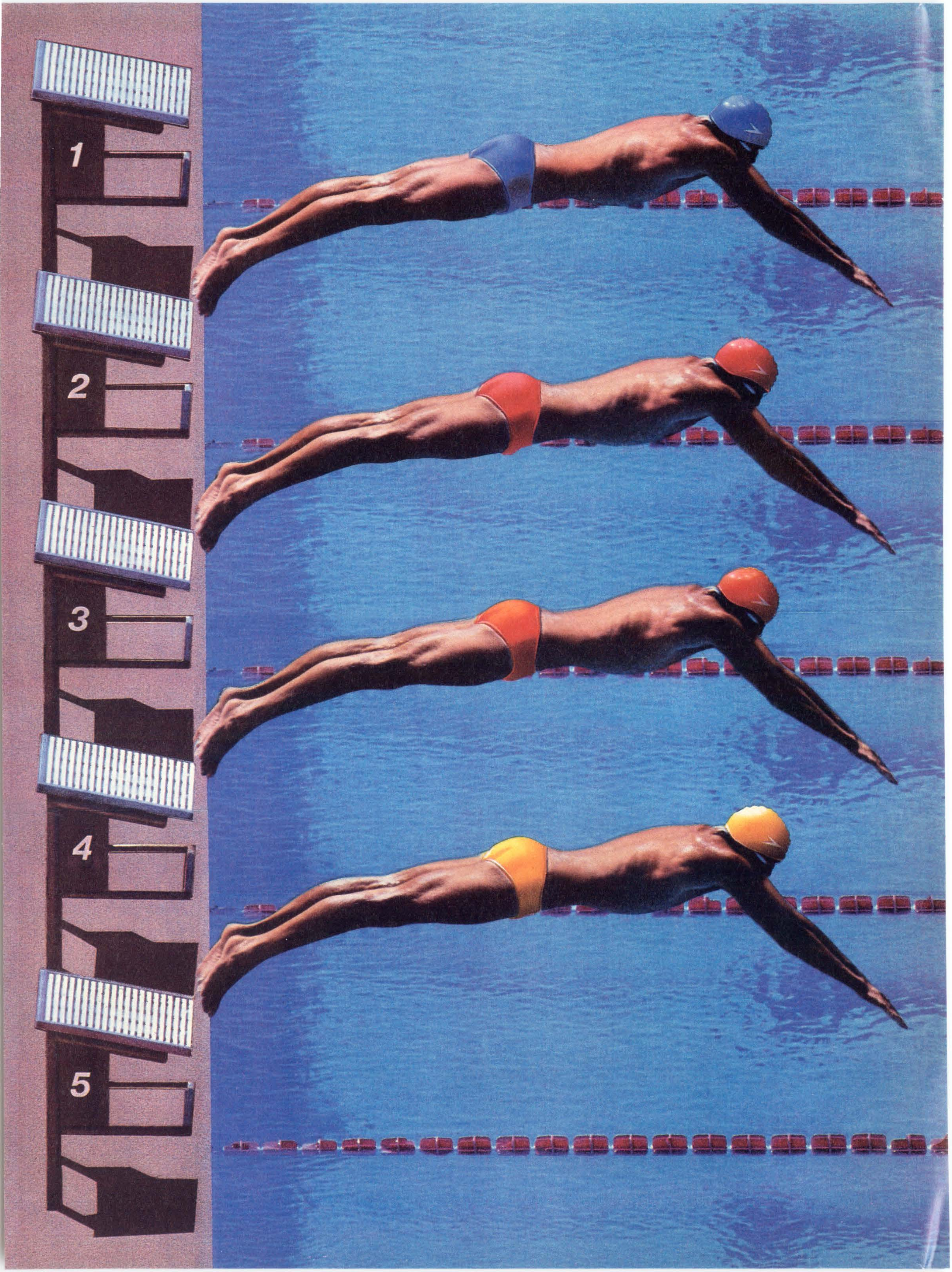
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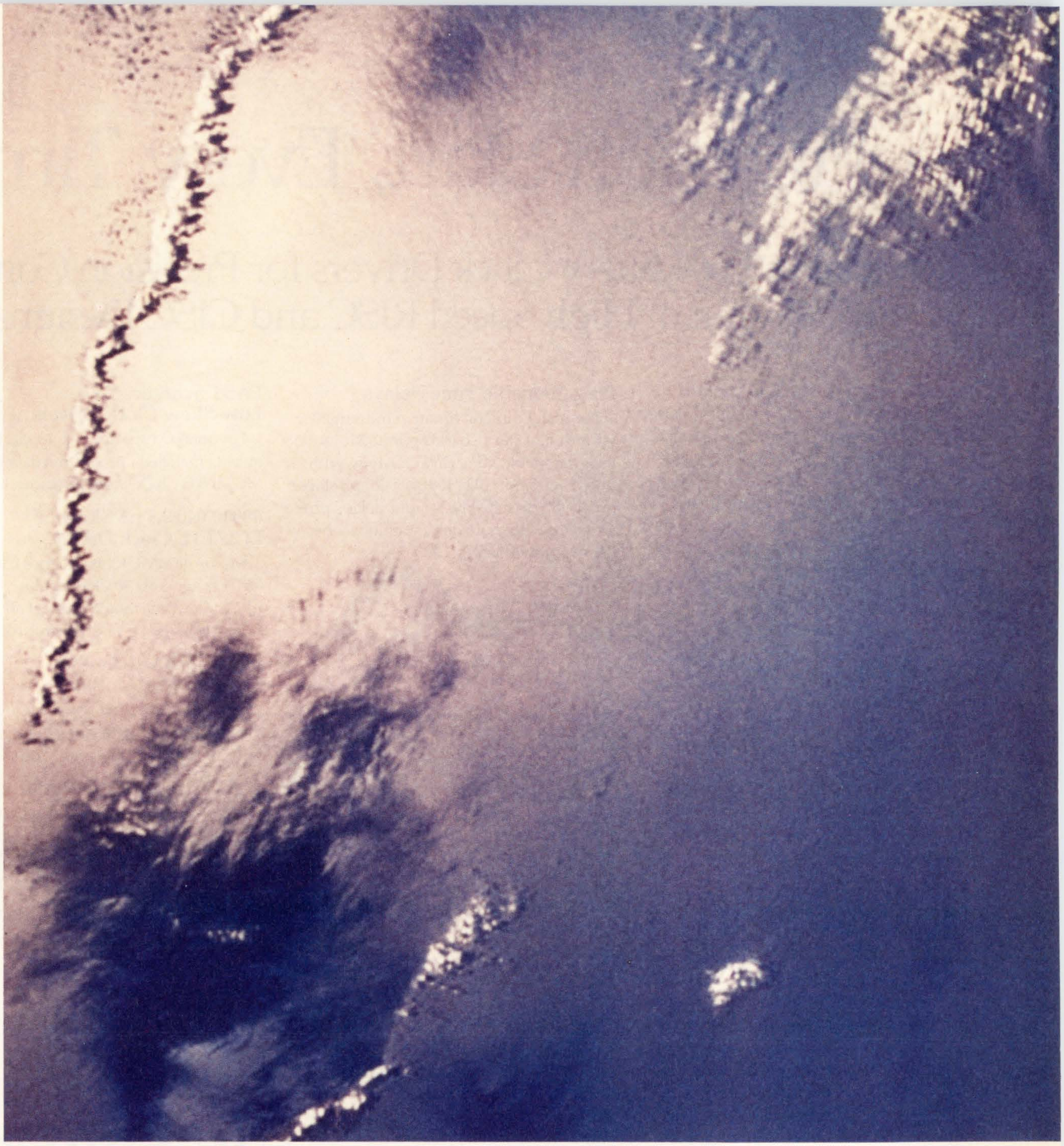
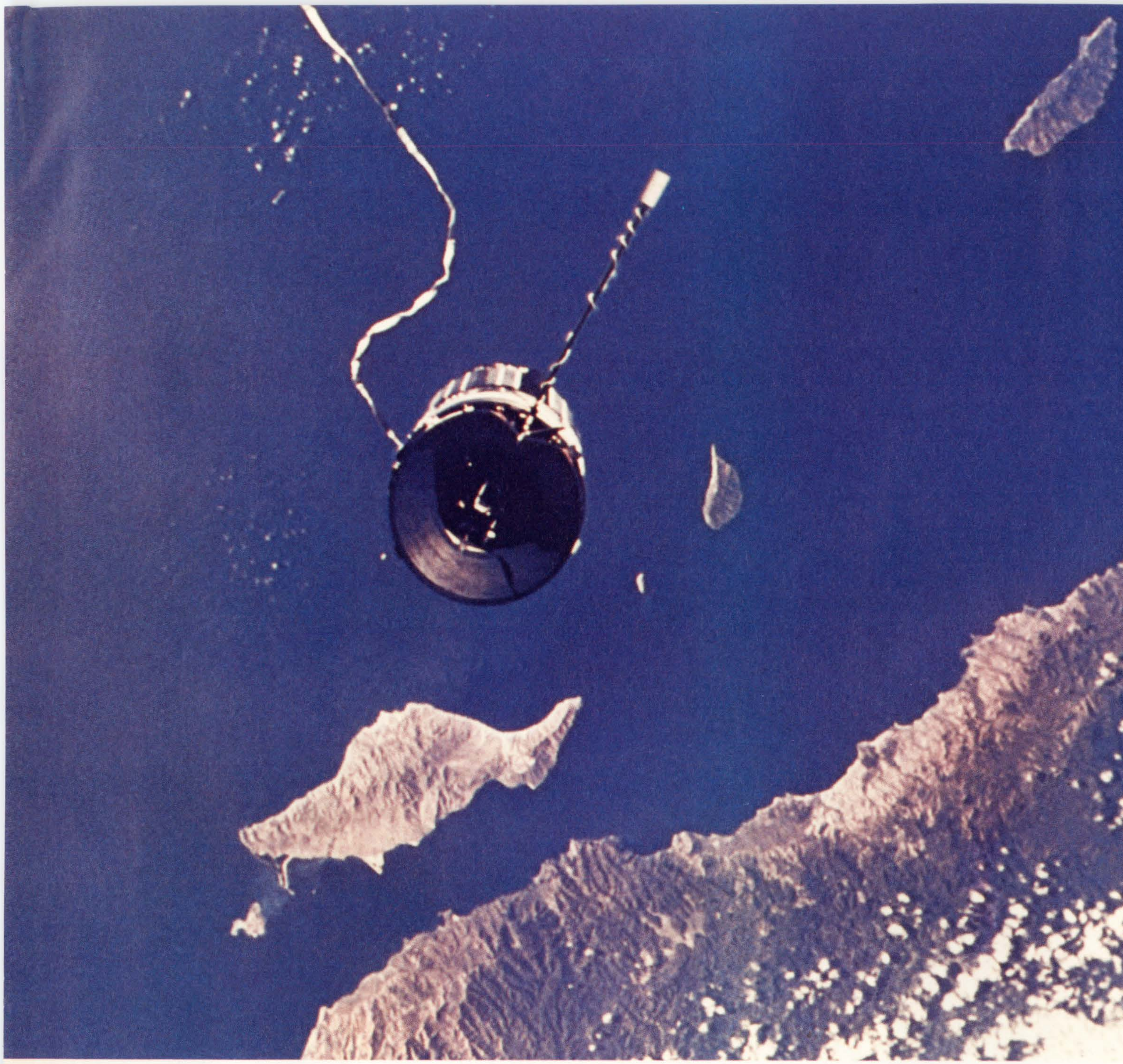


Even though we've been around the electronics industry for seventy-five years, we still have the same perspective.



CIRCLE NO. 137

HOW A STRATEGIC PARTNERSHIP WROTE A NEW CHAPTER ON SYSTEM PERFORMANCE:

DECstation 5000 AND LSI LOGIC.

Achieving 24.2 MIPS at 25 MHz was no small task. Even for Digital.

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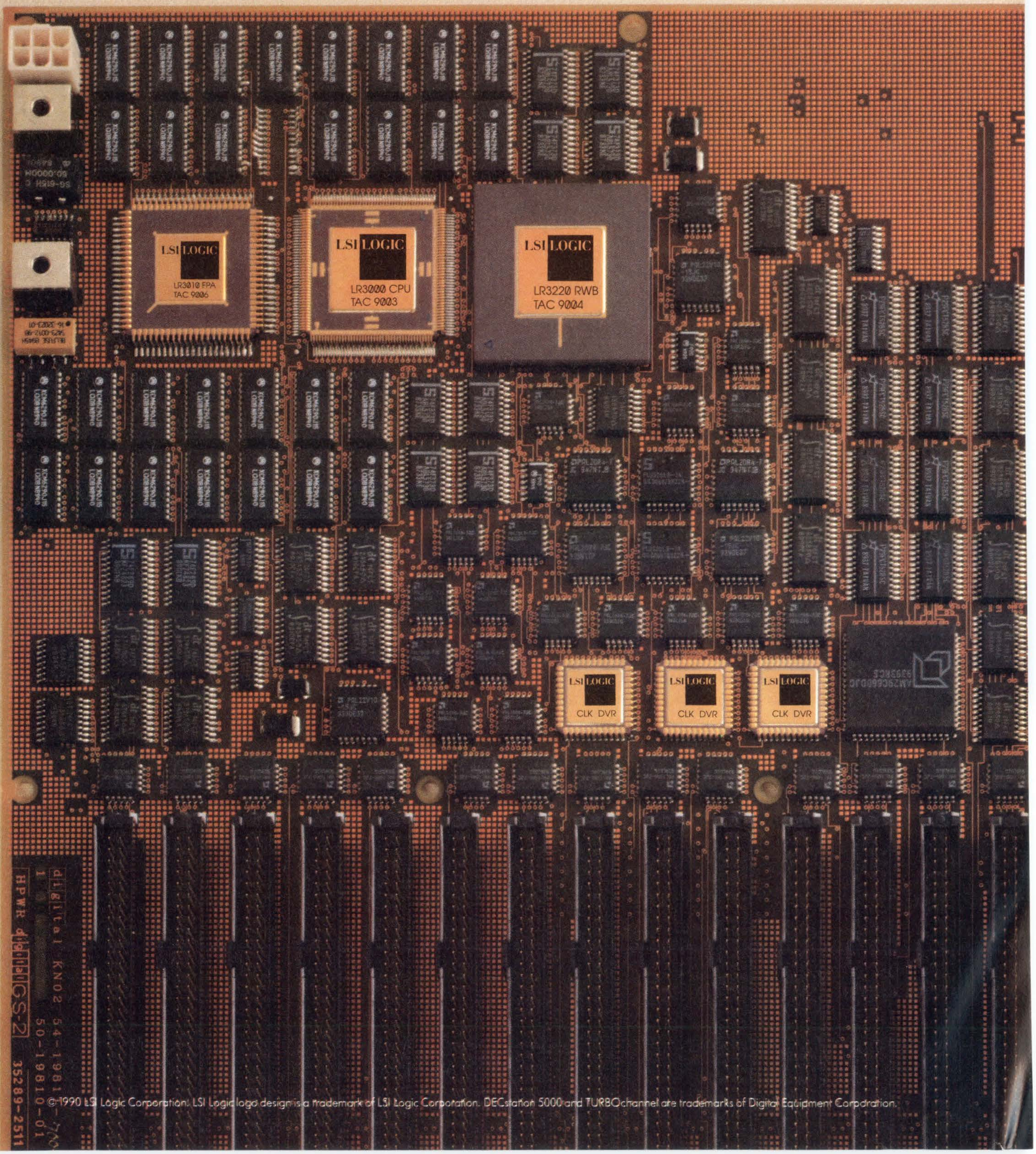
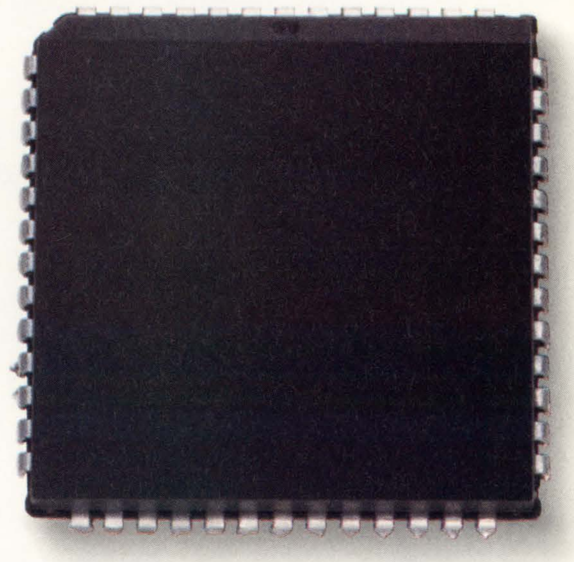
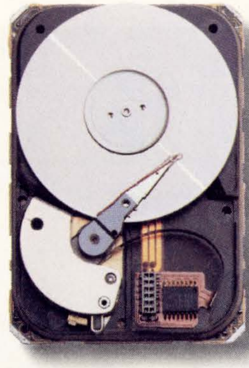


WHAT GOOD IS A BRAIN



WITHOUT A MEMORY?



To hear most people in the computer business talk, you'd think the only valuable part of a system is its microprocessor.

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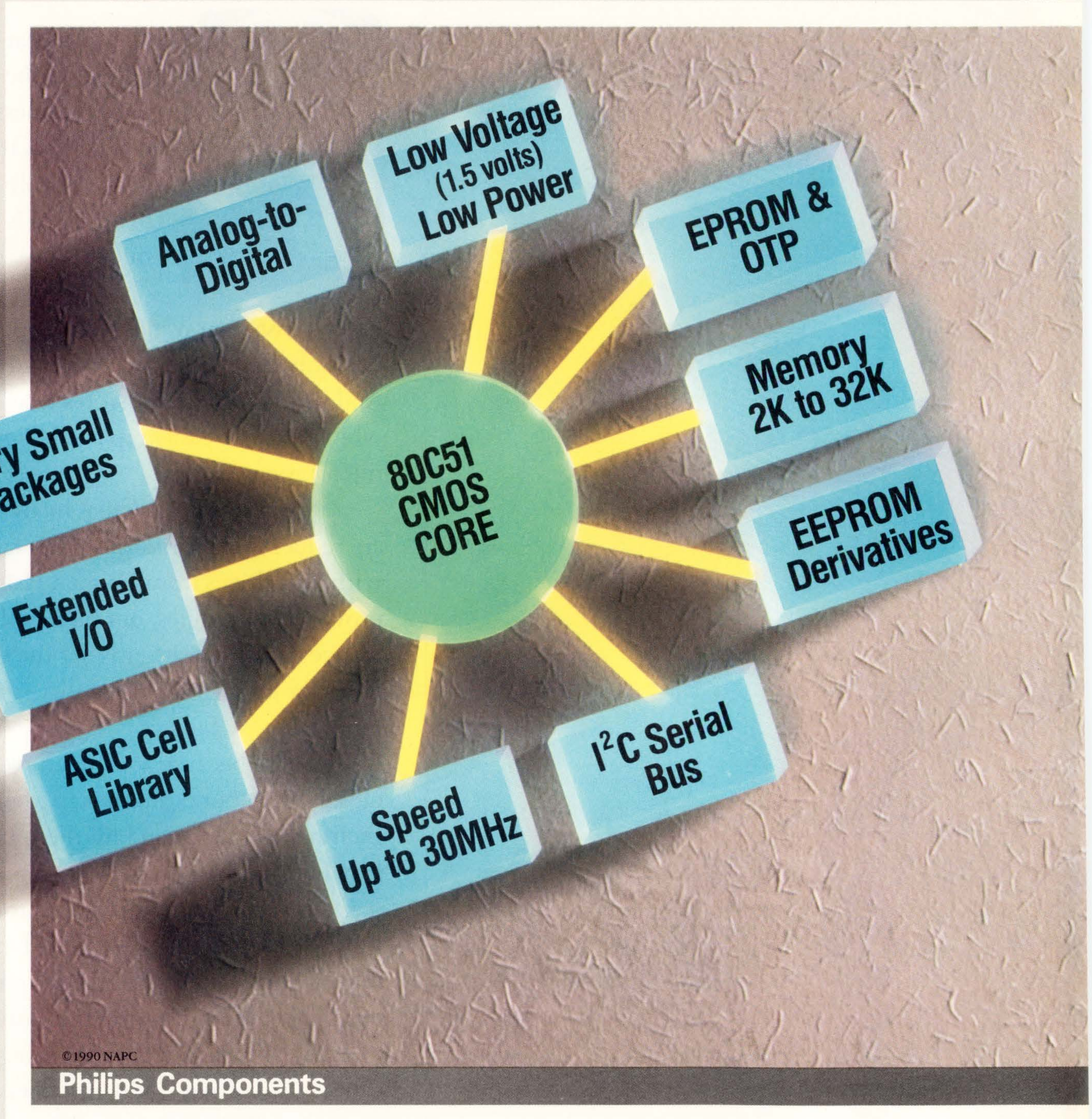

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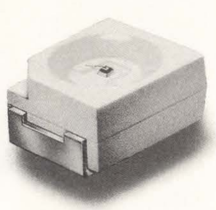

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CIRCLE NO. 140

NEWS BREAKS

EDITED BY JOAN MORROW LYNCH

AUDIO INTERFACE ENCODES, COMPRESSES DATA IN REAL TIME

Vigra's (San Diego, CA, (619) 483-1197) MMI-210 VMEbus compact-disk-quality digital-audio board is suitable for applications in professional studios, realistic flight simulators, and sonar signal processors. Firmware on the $3925 dual-channel board offers a choice of 4-bit ADPCM (adaptive differential PCM), 16-bit linear PCM, 8-bit μ-law, and 8-bit A-law data encoding and compression. A 1M-byte 3-ported memory array stores recorded data for subsequent playback. The board's audio data capacity varies based on the sampling rate and encoding scheme employed. For example, the board requires 960k bytes of memory to store 10 seconds of sound using 16-bit PCM encoding sampled at 48 kHz. Meanwhile, a 10-second recording sampled at 8 kHz using 4-bit ADPCM requires only 40k bytes of memory.—Maury Wright

LOW-COST INDUSTRIAL PC LINE OFFERS MANY I/O FUNCTIONS

The Micro-PC line of board-level computer components from Octagon Systems Corp (Westminster, CO, (303) 430-1500, FAX (303) 426-8126) delivers IBM PC compatibility for industrial systems in a small, low-cost package. PC compatibility allows you to develop and test your application on a PC and then transfer your code directly to the target system without change. The Model 5000 PC control card incorporates an NEC V20 μP running at 10 MHz; sockets for a 256k- or 1M-byte, single-in-line memory module and a 1M-bit flash EPROM or static RAM; a BIOS ROM; a watchdog timer; and the 8-bit PC-bus interface. The Model 5010 PC control card adds two serial ports and a parallel I/O printer port. Without memory chips, the Models 5000 and 5010 cost $195 and $345, respectively.

The company also offers many accessory I/O cards to support these two controllers. Its $295 Model 5400 EGA (enhanced graphics adapter) card provides standard PC video graphics. A $195 Model 5800 floppy/hard-disk card adds support for 5¼- and 3½-in. floppy-disk drives and hard-disk drives with IDE (integrated drive electronics) interfaces. For industrial applications you can add the $195 Model 5300 counter/timer I/O card and the $195 Model 5600 digital I/O card with 96 I/O lines. The family also includes the $395 Model 5328 motion-control card with a self-contained PID (proportional, integral, derivative) analog control system; the $345 Model 5329 motion-control card provides PID control for motor controllers that require pulse-width modulated signals.—Steven H Leibson

VMEBUS CPU STORAGE MODULES FORM A COMPLETE 80486 SYSTEM

Two VMEbus modules, collectively measuring 6×9×3.2 in. (two VMEbus slots), make up a complete IBM PC-compatible 80486-based computer system offering 20-MIPS performance. Radisys Corp (Beaverton, OR, (503) 690-1229) offers the EPC-5 (embedded PC) that targets applications as a front-end computer and operator interface for embedded-computer applications. The EPC-5 CPU module includes a choice of a 25-or 33-MHz 80486 μP. The module also features as much as 16M bytes of dynamic RAM, two RS-232C ports, a parallel port, a VGA graphics controller, a battery-backed clock, and a speaker. The mass-storage module furnishes a 3½-in. floppy-disk drive that can be accessed via the VMEbus front panel, and a slot for a 3½-in. hard disk drive. The company expects to ship the EPC-5 in November at a base price of $7495; the mass-storage modules start at $990.—Maury Wright

CASE TOOL INTEGRATES DESIGN, TESTING, AND DOCUMENTATION

The C Development Environment from Interactive Development Environments (San Francisco, CA, (415) 543-0900) integrates three widely used tools: IDE's Software Through Pictures (for structured analysis, design, and code-frame generation); Saber-C (for detailed coding, testing, and maintenance); and Framemaker or Interleaf TPS Coreplus (for technical publishing). The three tools share a common object-oriented database and a common window-based user interface. Saber-C provides extensive testing and debugging facilities and an incremental linker that minimizes edit-to-execute times.

You can transfer diagrams, listings, or text that you've created on one tool to one or both of the others via the user-interface windows that link the tools. Currently you have to issue separate compile/link and document-regeneration commands to pick up design or implementation changes, but IDE and the other tool vendors are exploring ways to further automate the propagation of changes from one tool to the others. Prices depend on the host configuration and start at $5000 for Software Through Pictures, $2495 for Saber-C, $2500 for Framemaker, and $2500 for Interleaf TPS Coreplus.—Chris Terry

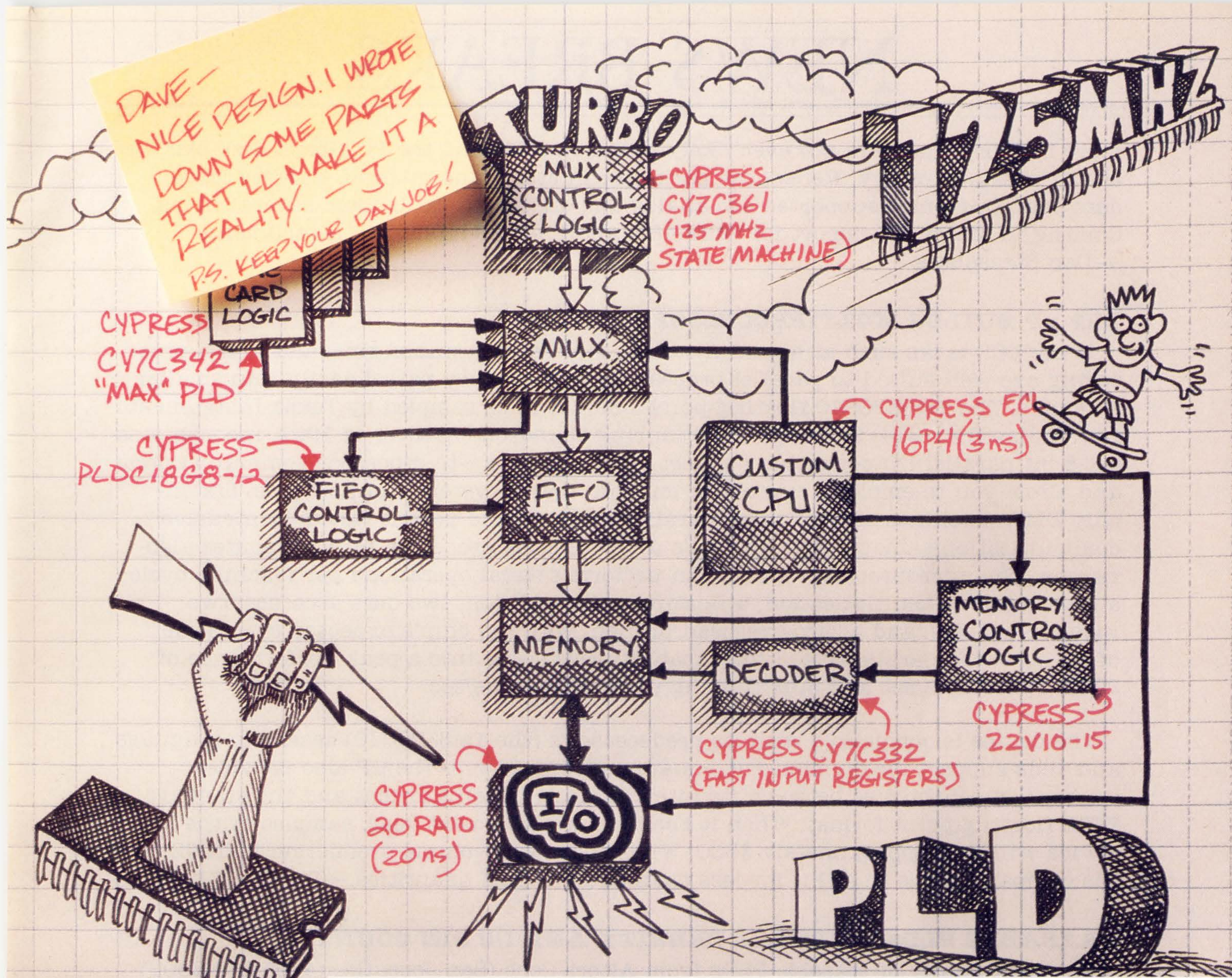
CHIP SET IMPLEMENTS CCITT H.261 IMAGE COMPRESSION

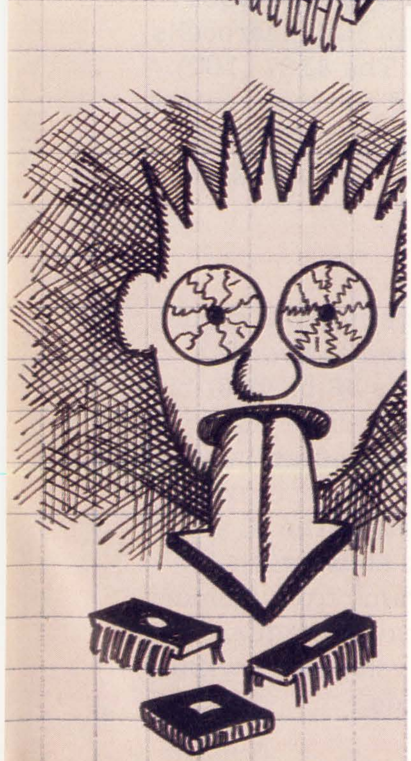
Computer handling of digitized images requires enormous amounts of bandwidth and memory. The sequence of images that makes up video adds to the computer's burden. A chip set from LSI Logic (Milpitas, CA, (408) 433-8000) helps reduce the burden to a more manageable size by compressing the image data. You compress a video image by reducing the amount of information it contains in two ways. First, you perform a frequency transform on a single image and quantize the spectrum, varying the quantization step-size to be coarser at the less important high frequencies. You then use variable-length coding to reduce the number of bits in the data. You handle subsequent images either the same way or by encoding only their variation from the previous image.

The set includes a discrete cosine transform processor (L64730), a quantization processor (L64740), a variable-length coder/decoder (L64750/51), a motion-estimation processor (L64720), and an interframe processor (L64760). The coder/decoder works in accordance with CCITT H.261 for video telephony. The chip set, including a BCH codec (L64715) for data transmission, handles data rates to 30 MHz and costs less than $700. The chips will be available in sample quantities in December and will be in production in the first quarter of 1991.—Richard A Quinnell

80386-BASED SOFTWARE SIMPLIFIES DATA ACQUISITION

Viewdac software for data acquisition, control, analysis, and display from Keithley Asyst (Rochester, NY, (800) 348-0033) takes full advantage of the capabilities of 80386- and 80486-based PCs. The package needs a well-equipped PC, though—one that has at least 4M bytes of RAM, an 80387 coprocessor, and 10M bytes of free space on its hard disk, and a display that conforms to IBM's EGA or VGA standards. The package will be priced at $2495, but you can get it at the introductory price of $1995 until December 31. The graphical user interface supports multiple windows and displays virtual instrument panels, but it makes intelligent use of text. You create applications by selecting functions that appear on menus, so you don't need to know a long list of commands. Bucking an overworked trend, the function descriptions appear in words, and not as a group of unfathomable icons. The software supports





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more memory than you are ever likely to put in a PC, and the PC's hard disk can act as virtual memory. Hence, the package can create and manipulate very large data sets. Currently supported are analog and digital I/O cards from several firms. Coming in March is support for IEEE-488- and RS-232C-interfaced instruments. —Dan Strassberg

DSP μP BUILDS MULTIPROCESSOR SYSTEMS

Many DSP tasks such as signal filtering, fast Fourier transforms, and image processing are well suited to parallel processing because they parcel easily into smaller subtasks. The TMS320C40 floating-point DSP μP, to be sampled by Texas Instruments Inc (Dallas, TX, (214) 995-6611 x700) during the second quarter of 1991, incorporates six 8-bit parallel I/O ports that support direct processor-to-processor communications and allow you to employ a variety of multiprocessor system architectures. Six on-chip DMA machines service these parallel I/O ports and permit fast, nonintrusive communications among your system's μPs while the processor's CPU executes algorithms. The microprocessor's CPU can perform several operations per machine cycle: a floating-point multiplication, a floating-point addition, two data accesses, two register updates, and a zero-overhead branch. With the chip's expected cycle time of 40 nsec, the parallel-execution capability translates into a peak performance of 200M operations/sec and 50M floating-point operations/sec.

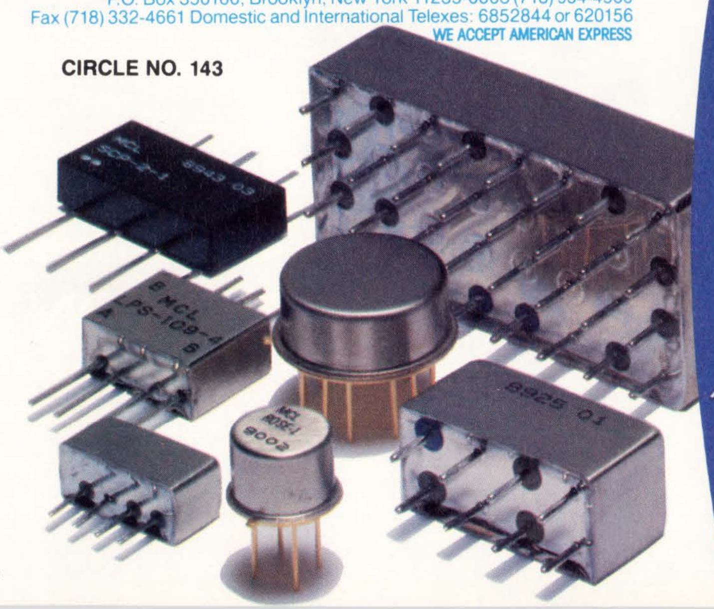
The device is compatible with its predecessor's (the TMS320C30) assembly language and adds support for division and square-root operations. The μP also provides conversion capabilities between its internal floating-point format and the standard IEEE floating-point format. When it becomes available next year, samples of the device will cost approximately $500. When it reaches volume production in 1992, the company plans to sell it for less than $100 in OEM quantities.—Steven H Leibson

ERASABLE PLDs INCREASE DENSITY AND I/O PIN COUNT

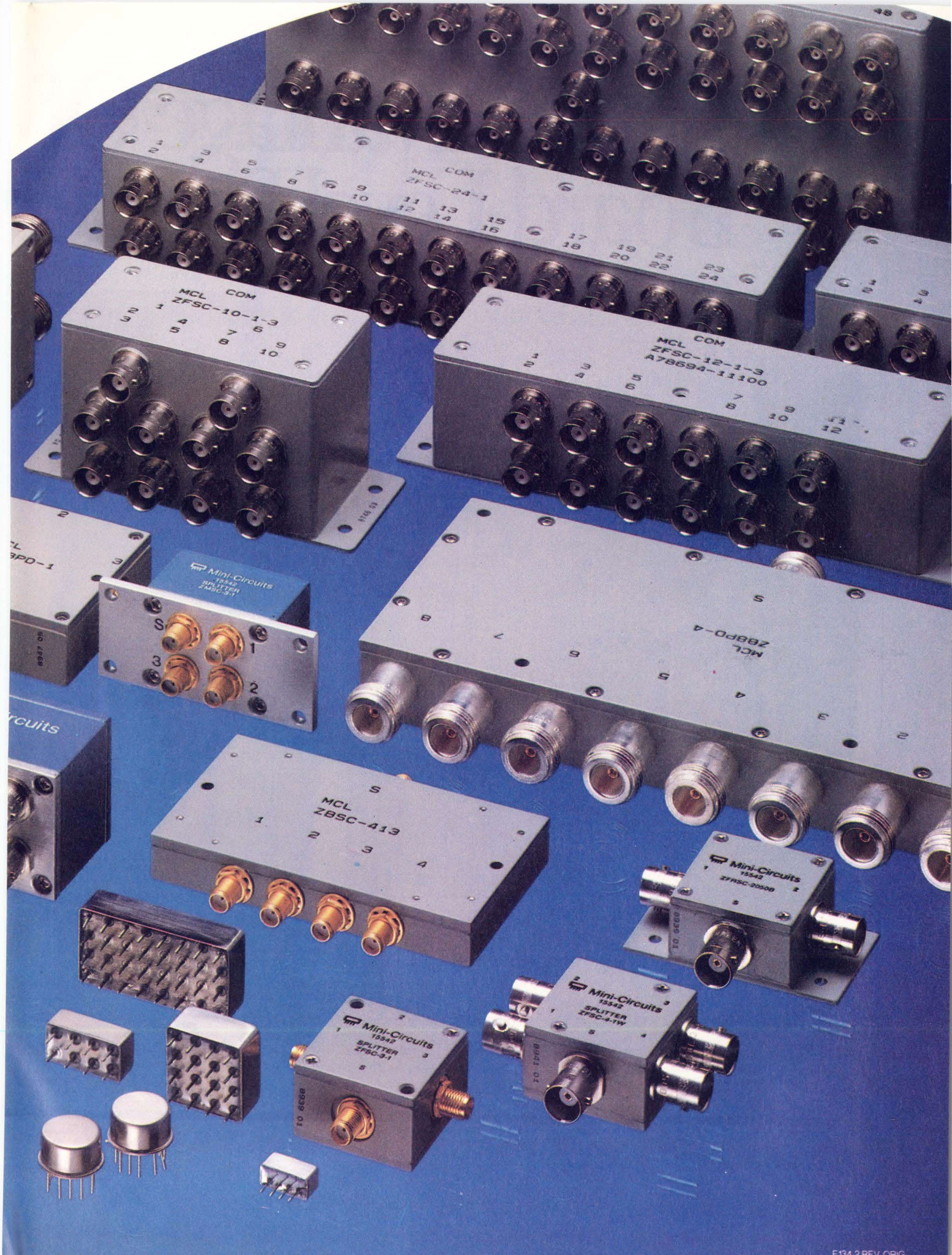
The Max family of erasable PLDs from Altera Corp (San Jose, CA, (408) 984-2800) now has two larger-capacity members. The $150 (100) EPM5192 offers 192 macrocells, a total gate-equivalent capacity of 7500 gates, in an 84-pin package. The $107 (100) EPM5130 offers 128 macrocells in a 100-pin windowed ceramic quad flatpack. Altera created the parts in response to customer demand for more I/O capability, because designers typically run out of I/O pins before running out of logic in PLD designs. —Richard A Quinnell

INTELLIGENT SCSI IC MOVES 10M BYTES/SEC

The $63 (1000) 53C710 SCSI I/O processor, a second-generation intelligent controller from NCR Corp (Dayton, OH, (800) 334-5454), can move 10M bytes/sec over the SCSI bus in synchronous mode and as many as 90M bytes/sec over its 32-bit host-bus interface when operated in a "cache-line burst mode." A slower bus-transfer mode operates at 40M bytes/sec. The device supports both "big-" and "little-endian" computer architectures. If a host CPU discovers that the SCSI controller is consuming too much bus bandwidth, it can kick the device off the bus by asserting the IC's "back-off" pin. The IC incorporates DMA controllers that move data between the SCSI bus and the host bus. These controllers also read control programs from memory on the host bus. The device uses a superset of the Scripts programming language developed for its predecessor, the 53C700. The company has also developed a Scripts compiler, written in C, for developing the controller's application code. —Steven H Leibson



F134-1 REV.A



F134-2 REV. ORIG

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COMPATIBILITY 88open CERTIFIED

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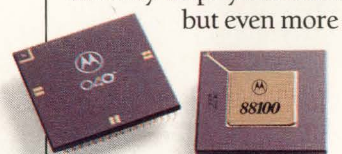
Once you've seen what Motorola brings to the table, we think you'll agree it's everything you need. Like the most complete line of VME products, services and engineering support available anywhere. Award-winning quality. Competitive pricing. All from the company that pioneered VME technology, and whose product line ranges from ICs to boards to full systems. And includes everything in between.

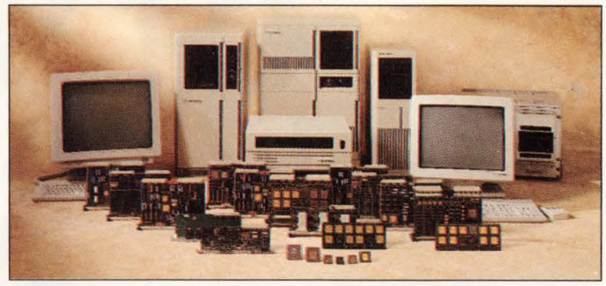
You decide exactly what you need from our more than 100 VME products at every level of price and performance. From CPU boards, like our new '040-based MVME165, to memory boards, to communications boards. And the industry's widest assortment of development tools, software resources, and technical support.

A partnership with Motorola not only helps you control costs, but even more importantly, speeds your time to market.



Our products include more functionality with a higher level of integration to accelerate your development efforts. And because of Six Sigma quality control you can be assured that our products will work right out of the box. It all adds up to the fact that getting you to market sooner is a promise only a company with the resources of Motorola can make good on.

Every Motorola product includes a built-in migration path, so your future product cycles are assured. Such as providing a way to upgrade from the 68020 to the 68030 to the 68040, or from a 68000 CISC board to an 88000 RISC board with a simple re-compile. Wherever you're headed, Motorola is going to be there.



And we'll support you during the entire development process. Every board in our product line includes a full suite of board diagnostics available in both a run-time and a source package. This degree of flexibility also extends to our nationwide customer service programs, which run the gamut from total on-site maintenance to self-maintenance support packages.

For more information, call us today at **1-800-624-8999**, ext. 230.

Once you discover the advantages of a partnership with Motorola, you'll see that it's no ordinary board-level decision. It could ensure the future of your company.

At Motorola, Openness Is Standard Procedure

These days, openness has become something of a buzz word, and everybody seems to have a different idea on what is and isn't "open." To us, it's no big mystery. Openness means open architectures, open software, open networking. And open standards like UNIX®, as indicated by our role in founding 88open. It means we're open to helping solve problems with your point of view in mind, not just ours. And it's been that way ever since we helped introduce VME back in 1982.

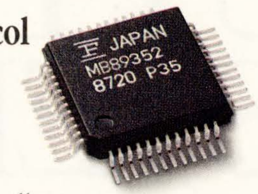
That's why Motorola is committed to supporting official and de facto industry standards, interoperable computing between multiple vendors, and non-proprietary open system architectures. It's why we created VMEexec:™ to facilitate the interoperability of different real-time software modules within a common UNIX environment. And it's why we support virtually every networking protocol, including XNS, TCP/IP, DECnet,™ MAP/TOP/OSI, SNA, BSC, X.400, and X.25.

This philosophy of openness is the same reason we offer as many VME boards, products and services as we do. It's to our mutual benefit, and after all, isn't that what partnerships are for?

MOTOROLA
Computer Group

 CIRCLE NO. 163

Fujitsu's new low-cost SCSI protocol controller is optimized for PC applications.



Up to now, if you needed a high-performance SCSI protocol controller (SPC) IC for your PC application, you were faced with two options. Neither of which met your needs.

You could use older products that can't keep up with your PC. Or you could use high-priced SPCs that were also high in pin count and cost.

Now, thanks to Fujitsu's MB89352, there's no need to compromise. Because its a low-cost, high-performance SPC that meets the stringent cost and size requirements of PC applications.

Which makes your life a lot easier. Because instead of having to choose between slower products and higher prices, the only choice you have to make is Fujitsu.

And in contrast to other devices with pin counts of 68 to 150, the MB89352 provides you with a modest pin count of 48. All of which meets your need for smaller, lighter, more compact systems.

But with a 2.7 Mbyte/sec. transfer rate, it packs all the power and speed your PC application needs. Today and tomorrow.

All in a 48-pin quad plastic surface-mount package no larger than a dime. Or a conventional 48-pin DIP.

But having the right SPC for your PC is only half of what you need to win the race to market. You also need the right development tools.

Which is why Fujitsu provides a complete SCSI host adapter with all the hardware and software you need to convert any IBM® PC/XT,™ AT® or compatible into an MB89352 evaluation system.

Including a real working software driver complete with source code listings. Giving you the edge to win the race to market.

To find out more about Fujitsu's new PC-based SCSI protocol controller, call 1-800-642-7616. We'll show you how to power your PC with a SCSI IC.

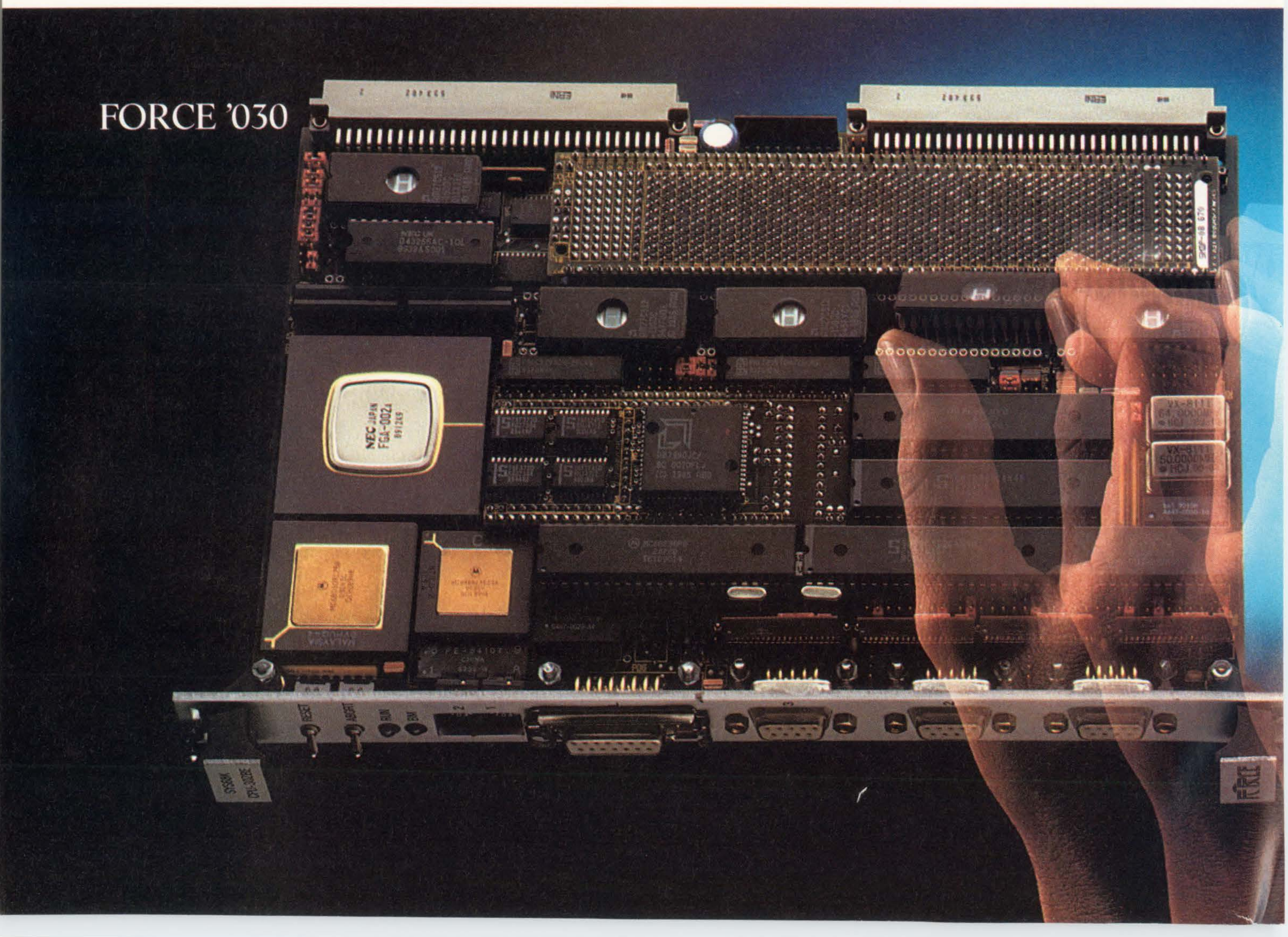
FUJITSU

Every step of the way.℠

FUJITSU MICROELECTRONICS, INC.
Integrated Circuits Division
3545 North First Street, San Jose, CA 95134-1804. 1-800/642-7616.

CIRCLE NO. 144

HOW TO TURN 040 WITHOUT LOSING A STEP.



Turning 040 doesn't mean you have to give up the code you lived by when you were 030. Although that's what some manufacturers expect you to do.

But not FORCE. We guarantee that applications written for our 68030 VME boards will run on our 68040 boards. That's because we've built compatibility into our 030 and 040 address maps and on-board device drivers.

In fact, no one makes it easier to move your software from 030 to 040. The competition can't even come close. Just ask them.

68030 CPU	COMPATIBILITY	68040 CPU
CPU-30	DMA, SCSI, Floppy, Ethernet, Serial I/O	CPU-40 + EAGLE I/O Module
CPU-31	DMA, SRAM, VSB, Serial I/O	CPU-41 + EAGLE I/O Module
CPU-33	DMA, DRAM, Serial I/O	CPU-40

Then ask us. We'll keep you from spending months writing new software drivers. So you can spend your time improving performance and functionality. Or getting to market months ahead of the competition.

What's more, you can start today on your 040 applications. Just develop them on a FORCE 030 board. When you're ready, we'll upgrade you to the highest performance 040 board you can buy.

So you can speed up your software without missing a step.

Of course, we have all the tools you need to get started. Choose from the broadest range of real-time operating systems and kernels, including PDOS, OS-9, VxWorks, VRTX32 and pSOS +. We even give you VMEPROM, free of charge.

You can also take advantage of XRAY and the entire Microtec family of software tools. Including cross, native and embedded development environments.

Our performance advantage even extends to UNIX.® With the industry's top-rated Unisoft UNIX 5.4.

Finally, you get the industry's best-rated documentation, integration support, regional technical staff and a full one-year warranty.

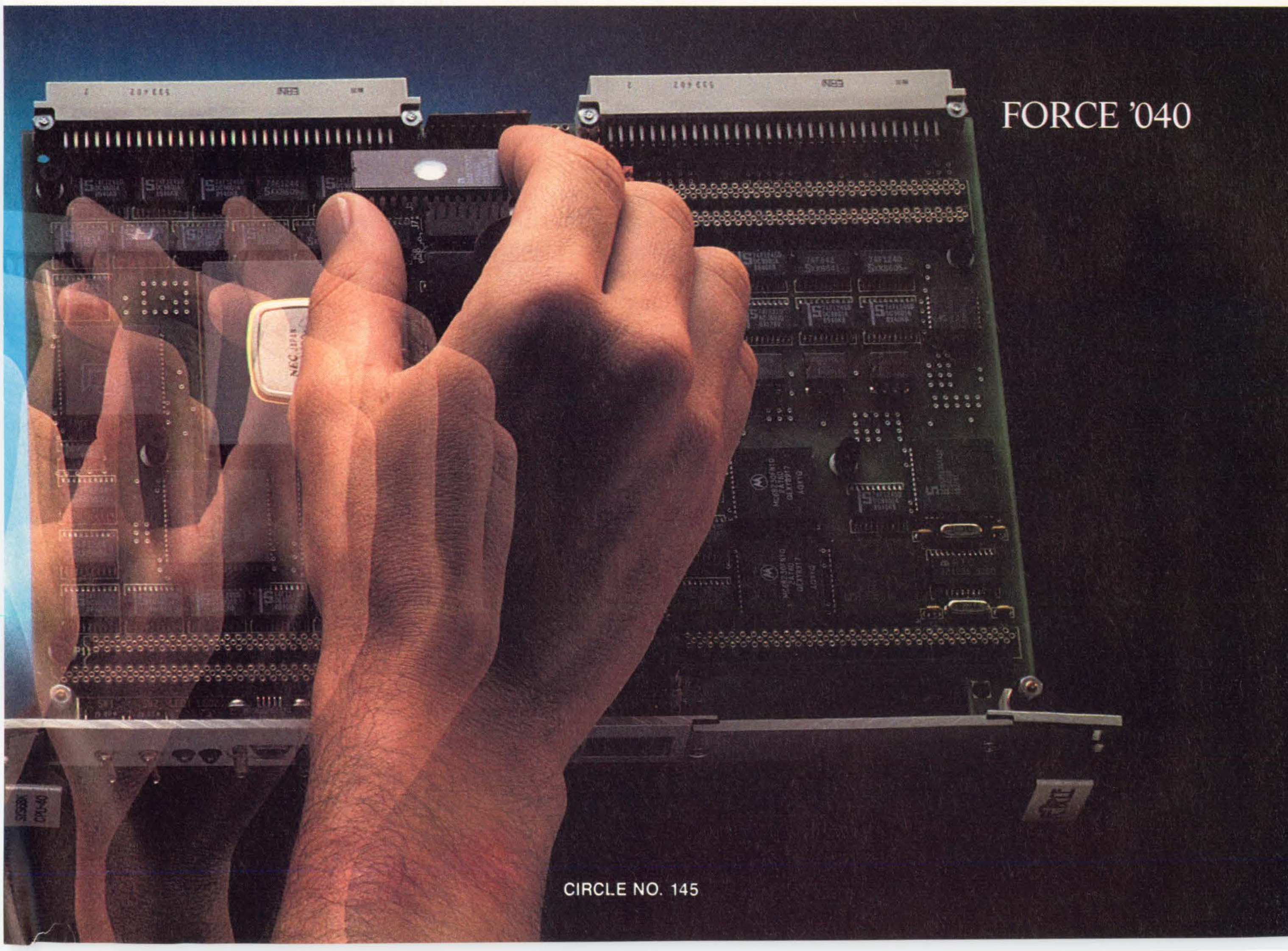
Here's your next step: call 1-800-BEST-VME ext. 40 for details on our 030 to 040 upgrade offer. Or fax a request to (408) 374-1146 for an immediate response.

Because turning 040 doesn't have to slow you down.

FORCE COMPUTERS®

VME at its best.

FORCE Computers, Inc., 3165 Winchester Blvd., Campbell, CA 95008-6557, (408) 370-6300 ext. 40



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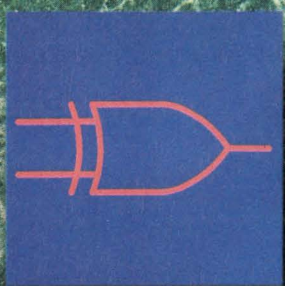


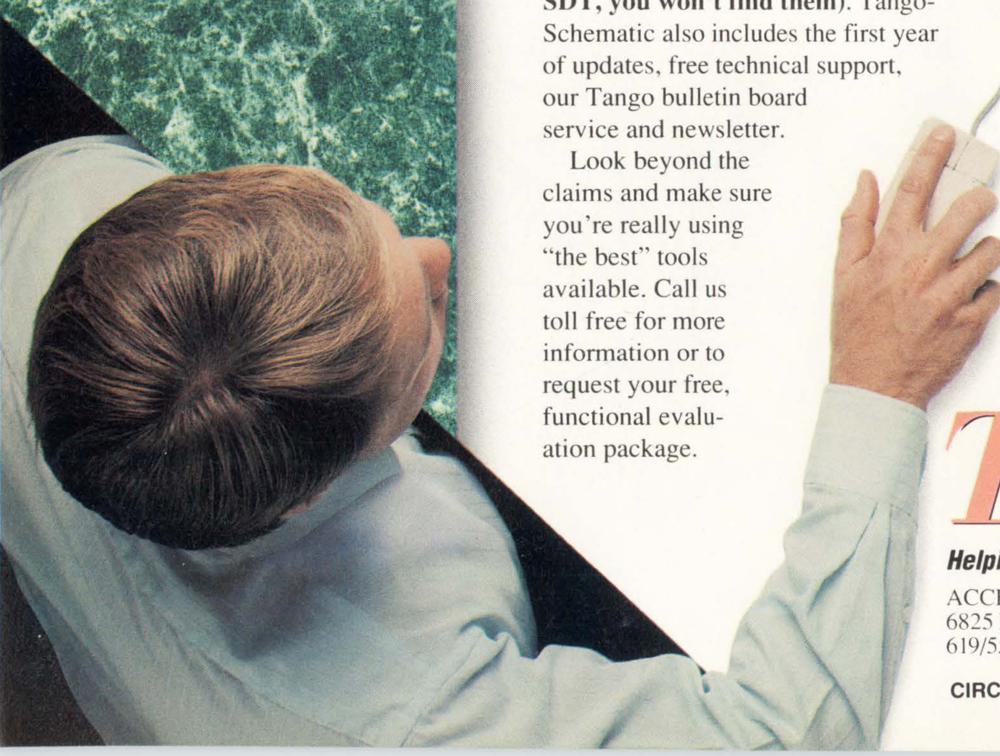
Tango-Schematic is the front end of the popular Tango family of PC-based electronic design software. Users execute all common functions with Tango's easy-to-use "Windows™-like" interface **(unlike OrCAD/SDT)**. Tango takes an integrated approach to design, with sheet and component creation, post processing and hard copy generation, all executed from a single program **(with OrCAD/SDT, you'll run as many as twenty different programs to access all functions)**.

Tango-Schematic's extensive device libraries from SEDCO contain over 10,000 commercial, true ANSI/IEEE and DeMorgan symbols, all verified for accuracy **(compared to about 6,000 symbols in OrCAD/SDT and they make no claims about accuracy, either)**.

Post-processing features include: forward and back annotation, design rule checking and sheet cleanup. Tango, EDIF 2.0, PSpice,™ P-CAD™ and other net list formats are supported.

Other examples of Tango's versatility include: support of homogeneous *and* heterogeneous components; unlimited zoom levels; display of hidden pins to enable splitting power and ground nets; and use of a unique *snap-to-pin* feature for guaranteed wire-to-component connections **(don't bother looking for these features in OrCAD/SDT, you won't find them)**. Tango-Schematic also includes the first year of updates, free technical support, our Tango bulletin board service and newsletter.

Look beyond the claims and make sure you're really using "the best" tools available. Call us toll free for more information or to request your free, functional evaluation package.



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CIRCLE NO. 146

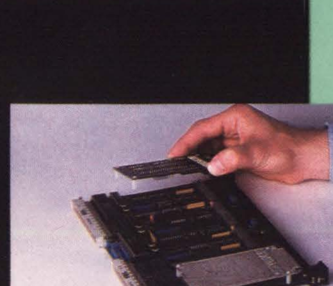
A Look at Today... A Vision of Tomorrow

68040 VME
33 MHz 0-Wait-State

Your Vision of High Performance at an Affordable Price is Now Real!

With the OB68K/VME40™ you no longer have to compromise on performance or price in your VME embedded control application. We start by giving you a very basic board which includes:

- 25-33MHz 68040.
- (8) 28-pin RAM sockets for up to 256KB of dual access 0-wait-state static RAM (32KB standard).
- (8) 32-pin sockets for up to 8MB of ROM.
- (2) asynch RS232C serial ports.
- (16) lines of parallel I/O.



You can configure it with just the right amount of RAM and ROM you need. And you do not have to sacrifice features. Our Omnimodule™ modular I/O connector allows you to implement a wide variety of serial, parallel, SCSI, GPIB, analog, digital and other I/O options - all fitting into one slot. Other features include:

- VTC's VIC068 VME interface chip with arbiter, interrupter, mailbox and more.
- Terminal monitor/ debugger/diagnostic firmware program included.
- 2 year limited warranty.
- Worldwide availability.

All of this gives you a high performance board at a price you can afford with the features you need.

To learn more about our OB68K/VME40 contact our Marketing Manager, Pete Czuchra at 1-800-638-5022 or (708) 231-6880 in Illinois.

Omnimodules™

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Fax No. 708-231-7042
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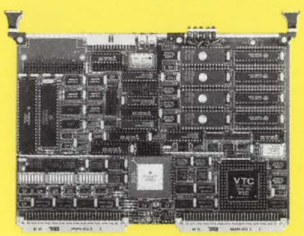
CIRCLE NO. 120

Our VME and Multibus Product Lines Stretch for Over 124 Miles

That's 854,738 uniquely configured boards to choose from and all from Omnibyte. You can choose from different processor types, RAM sizes, I/O options and other features to put together a board that gives you the features you need. With Omnibyte's quality, selection and 2 year limited warranty, you can count on finding exactly what your looking for.

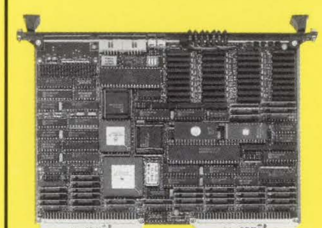
Here are just a few of the boards we offer:

OB68K/VME20™ VME SINGLE BOARD COMPUTER



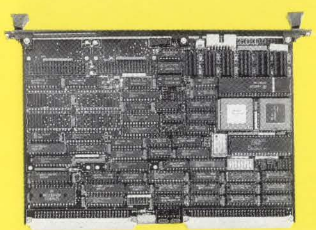
- 68020 16.66 - 33 MHz CPU
- (8) 28-pin RAM sockets for up to 265KB of dual-access zero-wait-state-static RAM
- (8) 32-pin sockets for up to 8MB of ROM, (4) sockets may be EEPROM
- (2) RS232C asynch serial ports
- (16) lines of parallel I/O
- (1) (OMNIMODULE socket for a wide variety of I/O (i.e. 2 serial ports, 20 parallel lines)
- VIC068 VME Interface Controller

OB68K/VSBC20™ VME SINGLE BOARD COMPUTER



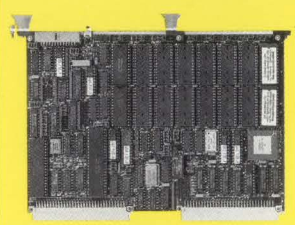
- 68020 16-33MHz, CPU
- 1-4 MB of dual-access, zero-wait-state DRAM with parity
- 68882 (optional)
- (2) 32-pin ROM sockets
- (2) RS232C serial ports
- (2) 8-bit parallel ports
- (1) OMNIMODULE socket for a wide variety of I/O (i.e. 2 serial ports, 20 parallel lines)
- 4 level bus arbiter (optional)

OB68K/VSBCI™ VME SINGLE BOARD COMPUTER



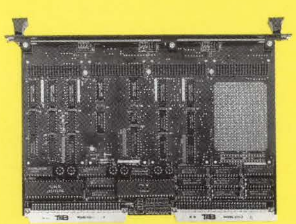
- 68000 12.5MHz 16/32 bit CPU
- 512KB of dual-access, zero-wait-state DRAM with parity
- (4) 28-pin ROM sockets
- (3) 16-bit counter/timers
- (2) Omnimodule™ I/O sockets for a wide variety of I/O (i.e. 4 serial ports, 40 parallel lines)
- DMA controller (optional)
- VME bus interrupt generator (optional)
- Optional 4 level bus arbiter
- Two year limited warranty

OB68K/VME1™ VME SINGLE BOARD COMPUTER



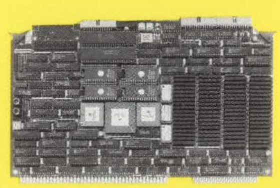
- 12.5 MHz 68000 CPU
- (8) pairs of 28-pin sockets for RAM or ROM
- (2) RS-232C serial ports
- (2) 8-bit parallel I/O ports
- System Controller

OB68K/VIO™ VME UNIVERSAL I/O BOARD



- (4) Omnimodule I/O sockets for a wide variety of I/O (i.e.8 serial ports, 80 parallel lines)
- One (1) interrupt per Omnimodule, two (2) optional

OB68K/MSBC30™ MULTIBUS I SINGLE BOARD COMPUTER



- 25-33 MHz 68030 CPU
- 4-32 MB dual access, zero-wait-state DRAM w/parity
- 68882 Math Co-Processor (optional)
- 2 channel DMA controller (optional)
- (2) RS232c sync/async serial ports
- (2) 8-bit parallel ports
- (1) OMNIMODULE™ socket
- (4) 32-pin ROM sockets

All our different configurations are built to give you the best in quality. And they are backed by our famous 2 year limited warranty. For more information call Pete Czuchra today. He'll help you pick the card you need.

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CIRCLE NO. 119

Don't attack free TV and opportunity for HDTV

What a terrible slap in the face! Jon Titus's editorial, "Nix broadcast HDTV" (EDN, April 12, 1990, pg 55) was so shortsighted I almost didn't believe what I was reading.

Does Jon realize what he is promoting? At the very least, the total destruction of the free broadcast system we hold so dear to our hearts in this country. Jon is basically promoting pay TV for everyone by forcing them into transmission media, such as fiber optics or dependence on the Bell System, which certainly would not be free. More and more viewers have become disenfranchised with the advent of cable because of the higher monthly costs these outfits are now charging. Does Jon think it would be any different with fiber-optic TV cable systems?

Jon is actually promoting the auctioning of the spectrum now occupied by TV broadcasters to the highest bidder. We the people have the rights to the spectrum, not the highest bidder. What other rights of ours does Jon propose bidding out? Statements like these are downright scary.

I doubt that Jon attended the recent National Association of Broadcasters convention in Atlanta. If he had, he would have seen the tremendous amount of new transmission technology that's being worked on for HDTV broadcasts. They may yet, with digital transmission and compression techniques, get an HDTV signal within a 6-MHz bandwidth. Time will tell. But even so, Jon states that "there will be little to watch but high-resolution versions of today's vacuous programs." What makes Jon think that programs transmitted into homes via optic fiber or the Bell System will be any less "vacuous"? Let the marketplace decide on programming, but don't take away free TV from the masses.

Why not attack the real reason for this type of programming? The cost-cutting, near-sighted Masters of Business Administration that run the networks and TV stations today are at the root of the programming problems. Don't attack the free TV system itself, and especially don't eliminate the opportunity for free HDTV broadcasts either. My God, that's un-American!

John Trautschold
Palatine, IL

(*Ed Note: John Trautschold missed the editorial's point. There is nothing free about the commercial broadcast spectrum. We support*

Tell us what you think about . . . the metric system

For years, EDN readers have registered their opinions on innumerable topics in letters that we've published in our Signals & Noise column. Now, we're taking that process one step further with an occasional series of reader surveys. Your response to these surveys will help us do a better job of serving you. Please take a minute or so to check off or jot down your answers.

You can respond to this survey right on this page or on a copy. Send us your response, and any other opinions or questions, by fax—(617) 558-4470—or by mail—EDN Surveys, 275 Washington St, Newton, MA 02158.

I work in:
- □ the US
- □ another country (please name) ____________

My work with measurement units is:
- □ all metric
- □ mostly metric
- □ about half metric, half English
- □ mostly English
- □ all English

I have to convert product information from English units to metric units:
- □ daily
- □ at least once a week
- □ at least once a month
- □ at least once a year
- □ never

I have to convert product information from metric units to English units:
- □ daily
- □ at least once a week
- □ at least once a month
- □ at least once a year
- □ never

The lack of English units in a product spec keeps me from buying a product:
- □ frequently
- □ occasionally
- □ seldom
- □ never

The lack of metric units in a product spec keeps me from buying a product:
- □ frequently
- □ occasionally
- □ seldom
- □ never

I think US electronics companies should switch to the metric system:
- □ immediately
- □ within 2 years
- □ in 2 to 5 years
- □ more than 5 years from now
- □ never

About ____ % of my company's business is in the US.
About ____ % of my company's business is outside the US.

If you would welcome a follow-up phone call by an EDN editor, please give your name and phone number. This information will not be shared with anyone else.

Name ____________________

Day phone ____________________

For non-US readers

The US-based companies I deal with—including those with local subsidiaries and sales offices—provide products based on:
- □ the "soft" metric system (mostly metric dimensions)
- □ the "hard" metric system (even for screw threads and connectors)
- □ both metric and English systems
- □ the English system only

The US-based companies I deal with—including those with local subsidiaries and sales offices—use metric units:
- □ for all their products
- □ for most of their products
- □ for some of their products
- □ for a few of their products
- □ for none of their products

stations by buying the products that they advertise, or by making donations. Anyone who thinks that TV and radio channels are free and belong to the people should attempt to get a license to broadcast on one. Today we auction off channels, but we don't put a monetary value on them. Try to compete and get the FCC to give you the license to WCBS's frequencies in New York City.

Yes, fiber-optic communications will be different—there will be more channels and thus more competition. And many of the transmissions will be "free." But no, it's not the Masters of Business Administration who control the drivel on broadcast TV. You do have a say in what you watch. To vote against today's programming, turn off your TV set.)

Omission

Due to an oversight, Orbit Semiconductor was omitted from the Special Report, "Fast-turnaround ASICs" (EDN, September 3, 1990, pg 124). Orbit produces mixed-signal CMOS arrays, standard cells, and full-custom designs on scheduled multi-project wafer runs. The company can put prototypes in your hands within 20 to 25 working days from sign-off, depending upon the fabrication schedule. Nonrecurring engineering charges for the initial prototype runs start at $1500 and provide a dozen tested parts in packages. For more information about Orbit's fast turnaround devices, contact Orbit Semiconductor Inc, Orbit Technical Marketing, 1230 Bordeaux Dr, Sunnyvale, CA 94089. Phone (800) 331-4617; in CA, (408) 744-1800.

Company not mentioned

In Brian Kerridge's article on Analog Spice simulation models (EDN, September 3, 1990, pg 79), ERA Technology Ltd was inadvertently omitted. This company is active in the fields of analog-device modeling and parameter extraction, working from hardware or data sheets, according to clients' specifications. Prices for modeling discrete devices range from £180 to £500, depending on device type.

The company offers three analog-simulation model libraries: discrete devices, communications ICs, and power-electronics ICs. The company's expertise covers simulation of switch-mode power supplies and high-power circuits. For example, the company has simulated a 6-MW power supply operating from an 11-kV, 3-phase ac source. Discrete devices, £3000, communications ICs, £6000, power-electronics ICs, £6000. (Discounts apply when you purchase more than one library.) You can reach ERA Technology Ltd at:
Cleeve Rd, Leatherhead
Surrey KT22 7SA, UK
Phone 0372 374151
FAX 0372 374496
TLX 264045

Realistic route to avoiding unsolicited calls

In response to Steve Leibson's editorial (EDN, January 4, 1990, pg 43), any solution to the problem of unsolicited junk telephone calls should be cheap, well defined, and enforceable—and most important, should place most of the burden on the originators of junk calls. My solution addresses all these points.

Technology: Establish a nationwide registry of numbers whose holders decline unsolicited calls. Marketers would be required to consult the registry and to avoid calls to listed numbers. They would dial the registry, define the range of telephone numbers, and download all restricted numbers in that range. Local telephone companies would then update the list. The software would be simple, and depending on volume, probably one or two 386-class machines with large hard disks and a bank of modems could serve the whole continent. By using a 900 number, the registry would force the marketers to pay for the system.

Telephone marketing is normal in business, so you could only allow residential numbers in the registry. We would also need to define who fits the category of telephone marketer—for example, someone who makes more than one unsolicited phone call a day.

Enforcement: Plant as few as ten decoy restricted numbers in each of 100 major cities, with caller ID on those numbers. Perhaps someone who knows more about telephony than I do has another suggestion.

Besides being realistic, cheap, and enforceable, this solution places most of the burden on marketers and creates a market for new dialing machines with appropriate memories and logic. Now all we need is the law. A uniform statute adopted by each of the states would be essential.

V Wesley Mansfield III, President
TennSoft Inc
Dunlap, TN

IT'S EASY TO HAVE YOUR SAY

EDN's Signals & Noise column provides a forum for readers to express their opinions on issues raised in the magazine's articles or on any topic that affects the engineering industry. You can use one of several easy ways to reach us. First, there's always the mail. Send your letters to Signals & Noise Editor, EDN Magazine, 275 Washington St, Newton, MA 02158. Or, send us a message via MCI mail at EDNBOS. Finally, EDN's bulletin-board system is ready for use—and it's free (except for the phone call). You can reach us at (617) 558-4241 and leave a letter in the EDITORS Special Interest Group. You'll need a 2400-bps modem and a communications program that is set for eight data bits, no parity, and one stop bit, or 2400, 8N1 in shorthand.

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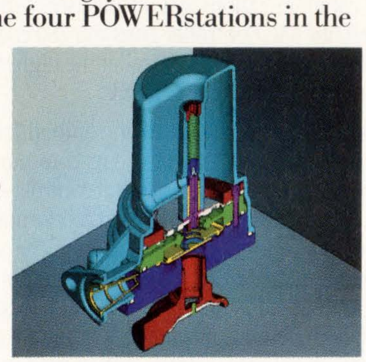

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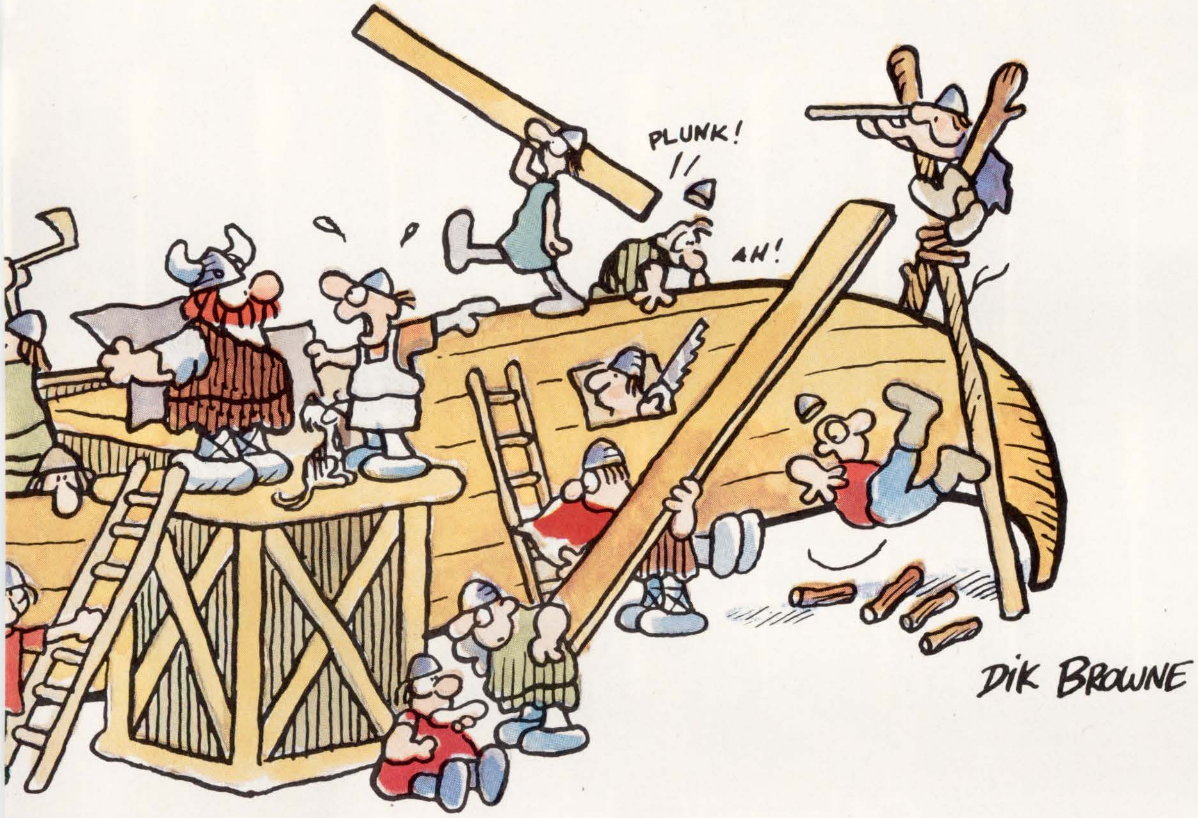

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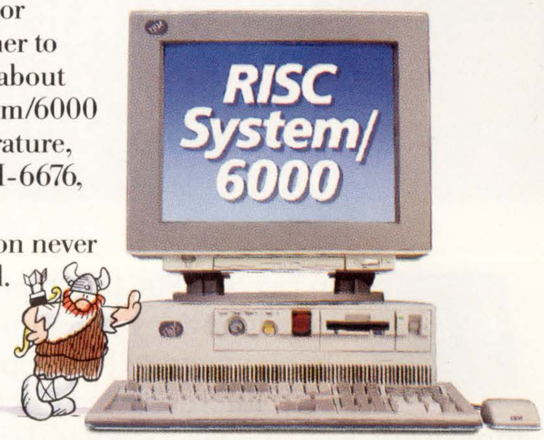

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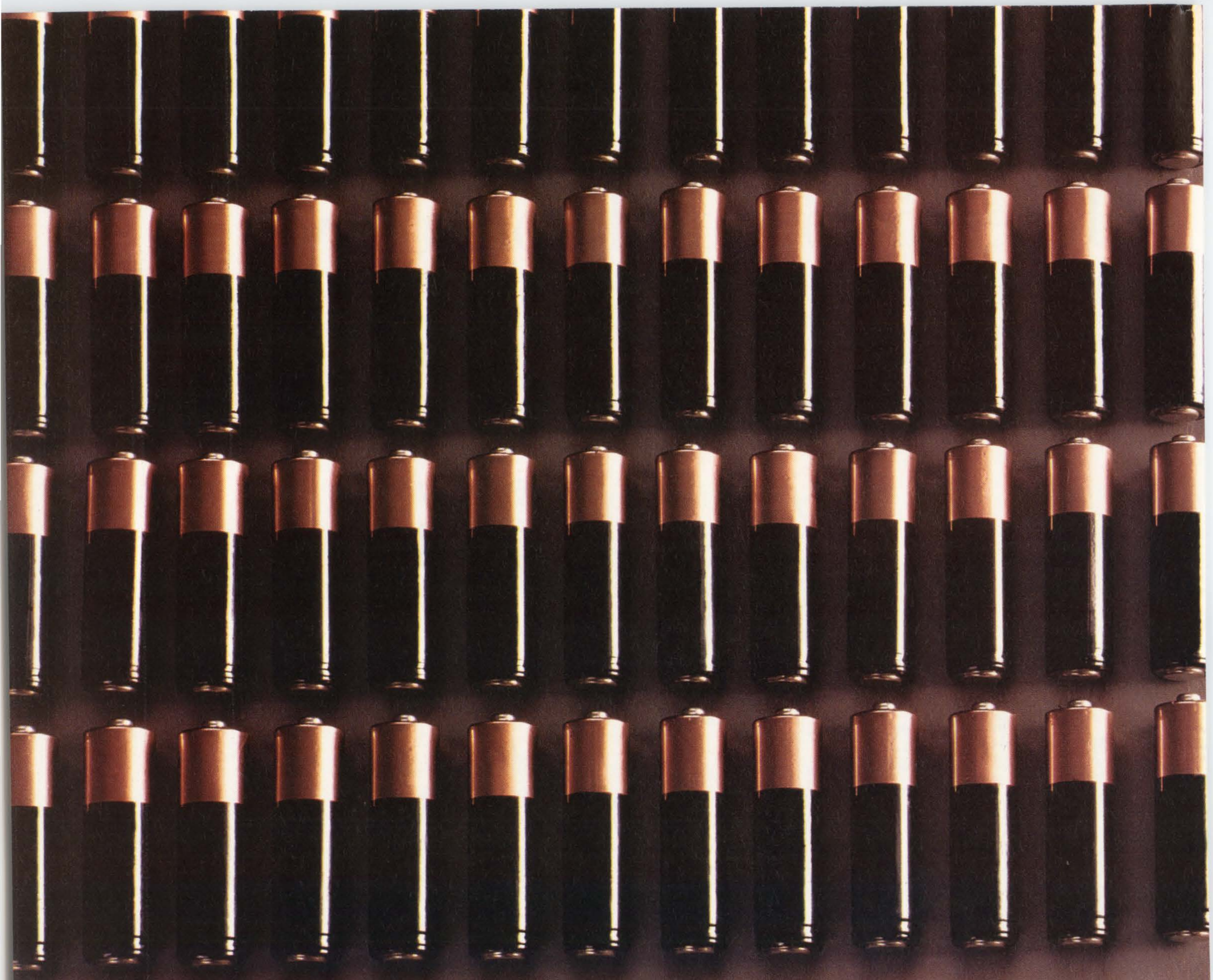

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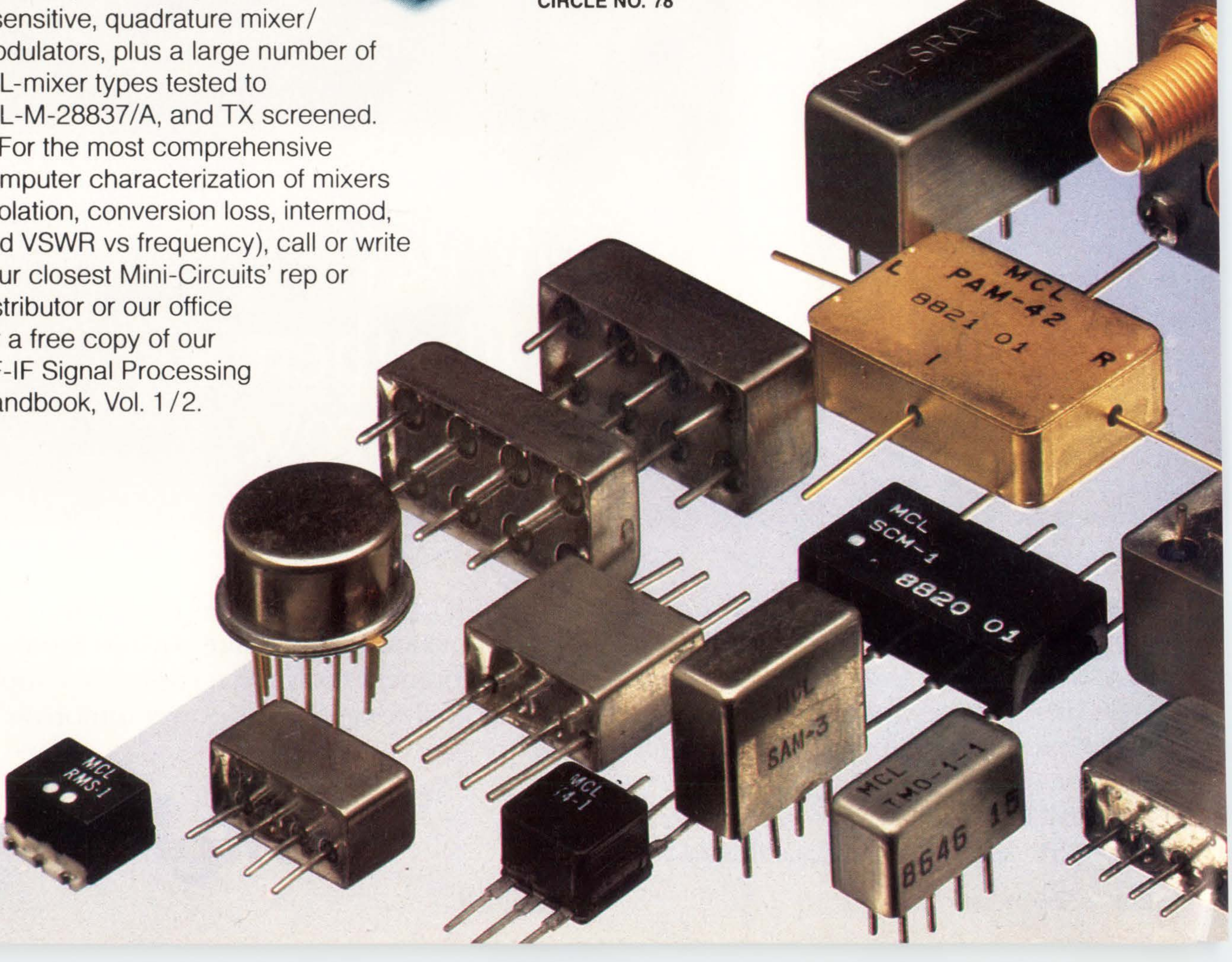

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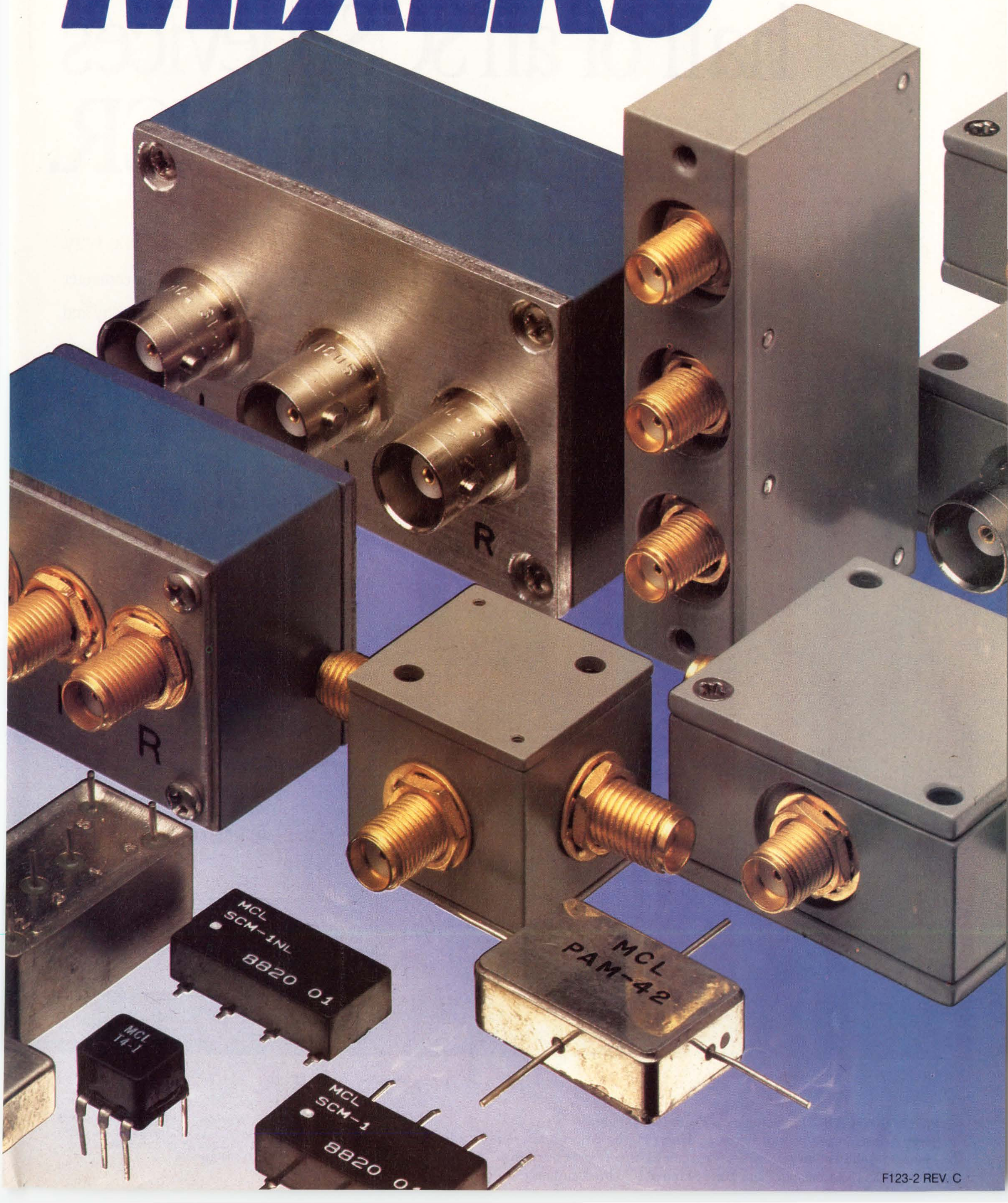

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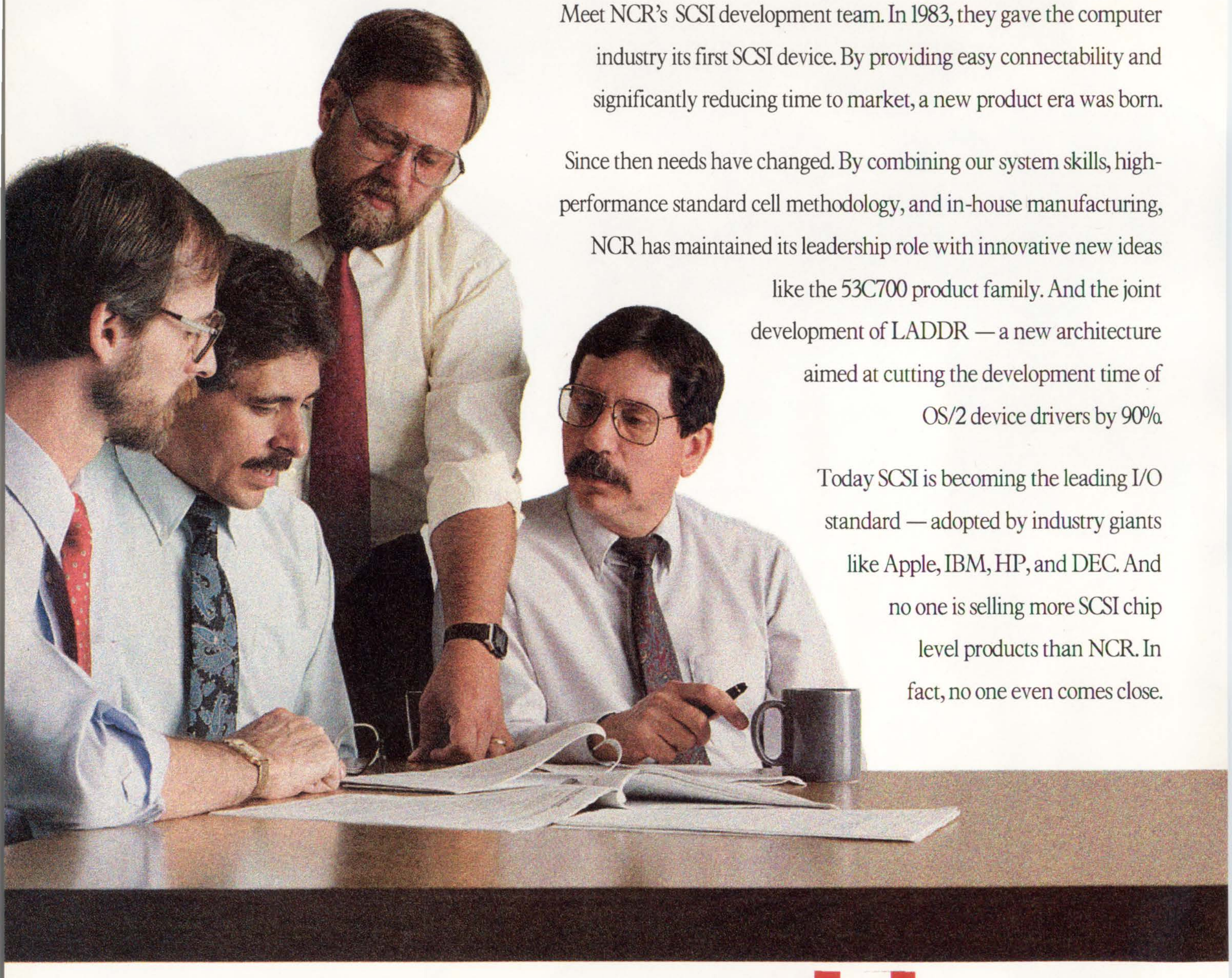

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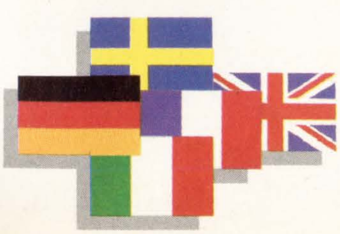

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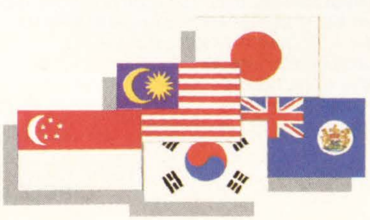

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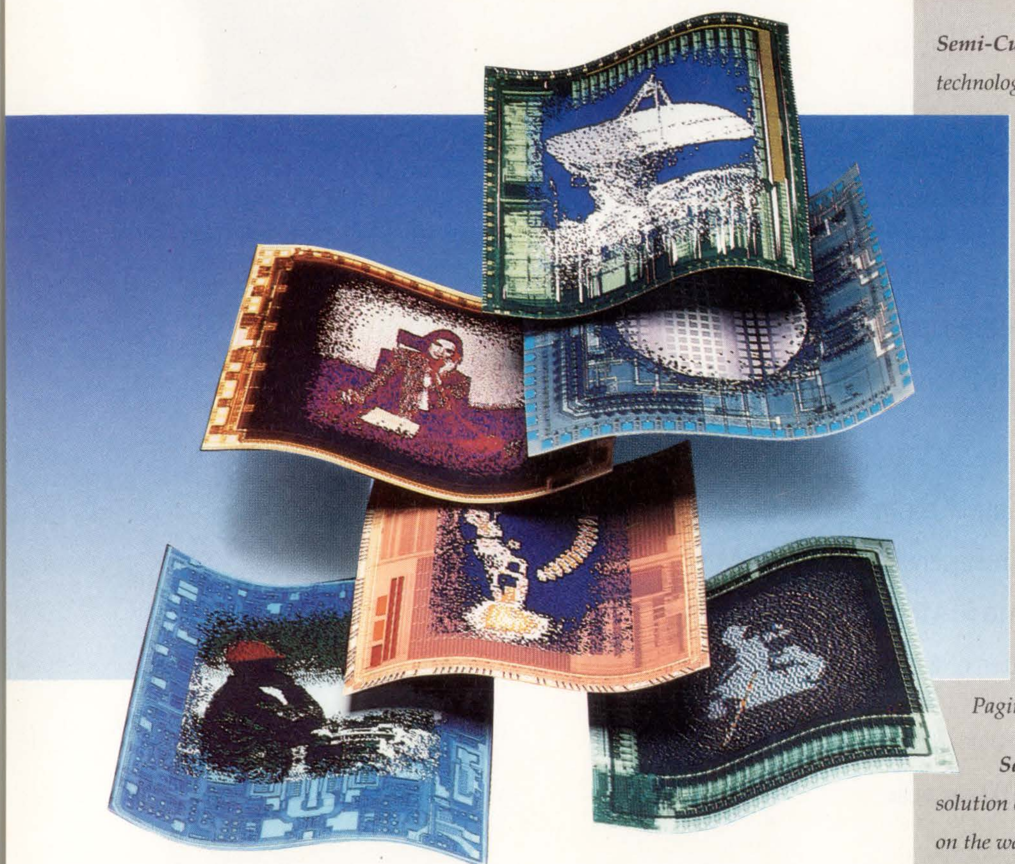

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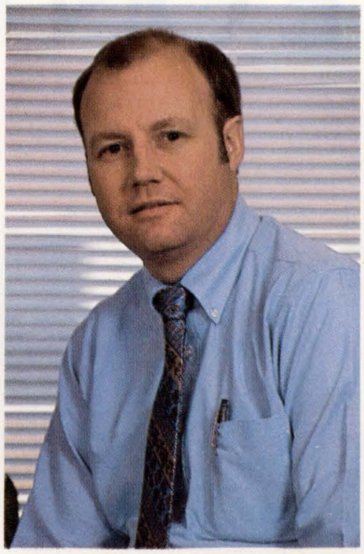
Praise the PC and pass the Windows



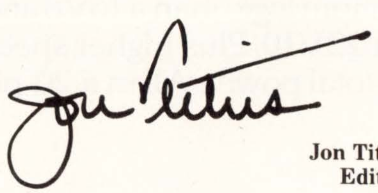
Those of us who live in New England no longer have to worry about the threat of a recession. Most of us are already in a recession and have been for some time. Local companies report lower earnings and losses, and fire workers. The housing market is a disaster. Massachusetts cannot balance its budget. In my town alone, the FDIC took over two banks. Luckily, there are bright spots in the USA and in specific markets. As I wrote in an earlier editorial (EDN, April 26, 1990, pg 49), telecommunications is a bright spot. Now, small computers is another.

When economic times are tough and interest rates are high, companies put off borrowing and spending large amounts of money on big and medium-sized computers. It's cheaper to upgrade a department's computer power by adding workstations or PCs and their attendant software, and by putting together—or adding to—a department network. I recently saw an 80386SX-based computer on sale for less than $1500. Faced with spending $50,000 for a few PCs and a network server or ten times that amount for a minicomputer upgrade, you can guess what most managers will decide. Such decisions spell hard times for mainframe and minicomputer manufacturers.

With the differences between high-performance PCs and workstations blurring, the workstation manufacturers may repeat the mistakes of the minicomputer suppliers. Unless these manufacturers realize their business is supplying "computing power" and not computer hardware, PCs will eat the workstation market.

Although low prices are a compelling reason to shift computer power from a central department to workers' desks, the availability of Microsoft's Windows 3.0 also makes the PC-purchase decision a sound one. In fact, if people are without computers, Windows may be the best reason to buy PCs and start people using them. Few users I know want to be bothered using MS-DOS or UNIX. In fact, they don't even want to know what an operating system is or what it does. Just serve up the database or spreadsheet, please. Windows does it, quickly and easily.

Yes, there are competitors of sorts: Desqview and OS/2, for example. But Desqview will never be as widespread as Windows, and OS/2 has many years to go before it succeeds MS-DOS, if it ever does. For example, today's version of OS/2 is incompatible with some older MS-DOS-based applications. Windows isn't without faults either. It has been reported that the program won't run on all PC clones because of hardware and software incompatibilities. Microsoft's Flight Simulator program used to be run as a test of compatibility. Perhaps Windows will take over that role. In the late '70s, the VisiCalc spreadsheet program fired people's interest in PCs. Now, Windows will keep people interested while it also draws new people and applications to today's powerful—and cheap—PCs. The PC vendors should have some good times ahead.



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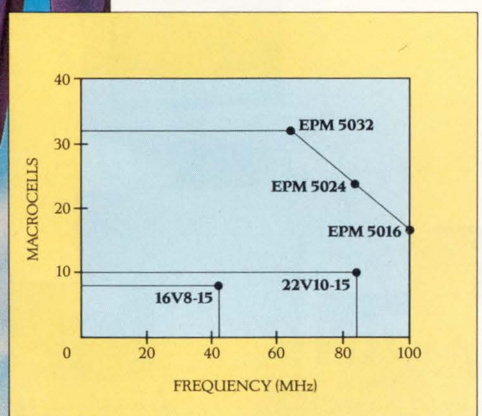

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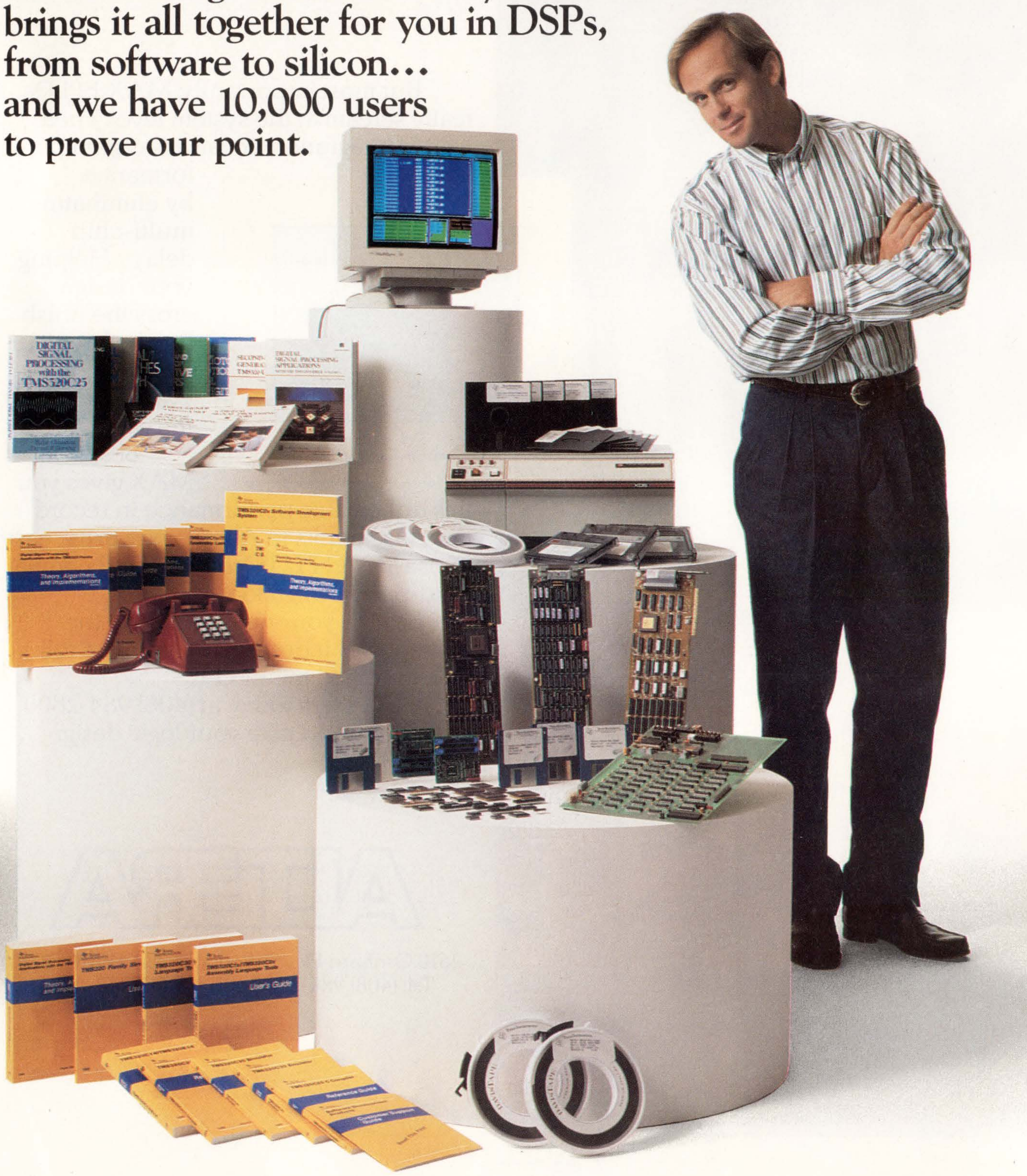

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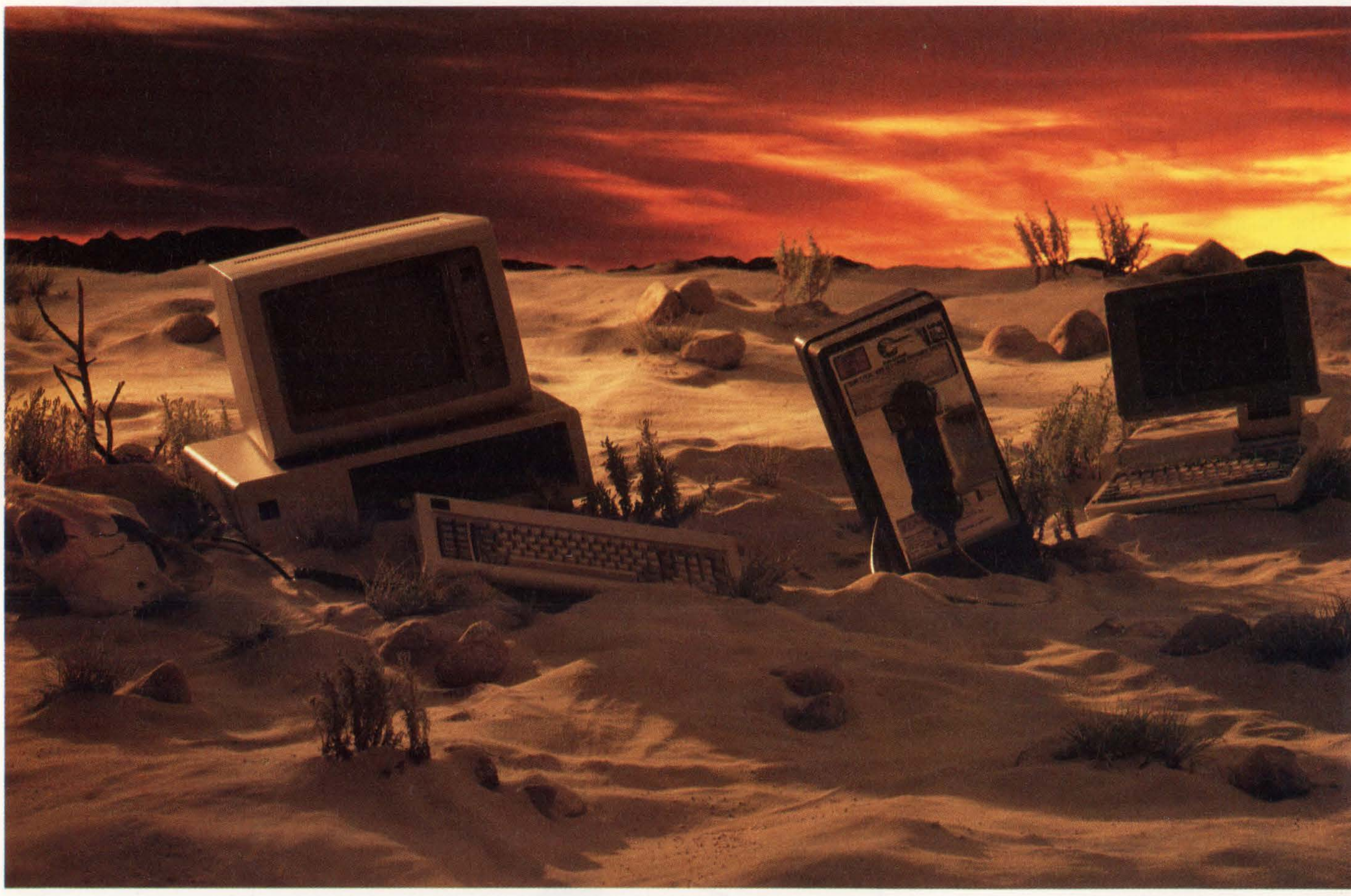

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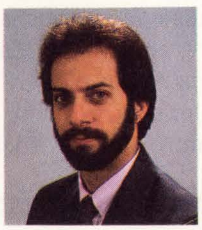
CIRCLE NO. 82

TEST-LOGIC SYNTHESIS

Software adds logic to make designs testable



Test-logic synthesis tools may not cause the barrier between design and test to crumble like the Berlin Wall, but at least the software will add some doors and windows to it.

Michael C Markowitz, Associate Editor

Two obstacles have slowed the adoption of design for testability. The first is the perception that adding logic to make a design testable diverts designers' attention from function design and slows product development. The second is test logic's attenuating effect on circuit performance.

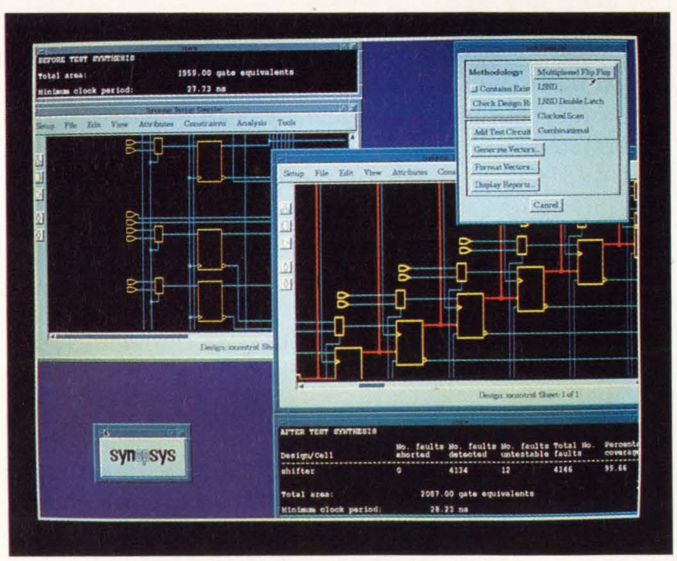
Test-logic synthesis can lessen any impact of test-logic design on product development by creating test and function logic. Unfortunately, if you're a talented designer, you'll have to live with somewhat slower circuits; test-logic synthesis tools can only be used to design circuits that are as efficient as those a gate-level designer might build.

The most basic test-logic synthesis tools build scan-testable circuits. In simple terms, scan-test synthesis converts sequential circuits into combinatorial circuits by arranging all storage elements (latches and flip-flops) into a shift-register chain.

You load the chain via the scan-in port by clocking data with a dedicated scan clock. Then the data ripples through the circuit's combinatorial logic and you latch it with the system clock. Finally, if you toggle the scan clock, it feeds the output data through the scan-out port so that you can evaluate it.

Partial scan is an approach in which some of the storage elements aren't part of the scan chain. To achieve high test coverage with partial scan, you still need to convert your sequential logic to combinational logic. To do this, toggle the system clock more than once. The data will ripple through combinatorial and sequential logic to the scan chain. While most scan-synthesis tools can build partial-scan circuits, most automatic test-pattern generation (ATPG) software tools can't generate vectors for sequential designs. As a result, partial-scan circuits are often difficult to test.

The sequential depth of a partial-scan design depends on the number of nonscannable flip-flops between scannable ones. The depth is important because it determines the number of times you need to toggle the system clock to propagate faults through a design.



After scan structures are added to a shifter *by Test Compiler (right), fault analysis reveals 99.66% fault coverage. The original shifter is on the left.*

Test-logic synthesis

Finding all the faults in your circuit depends on how you load the scan chain. Scan techniques differ in the types of storage elements and clocking schemes they allow (see **box,** "Choose from eight flavors of scan").

The tools that can add the logic to use scan test include Racal-Redac's SilcSyn Test Synthesis Module, Synopsys' Test Compiler, and Teradyne EDA's Scangen.

- The SilcSyn Test Synthesis Module uses only register transfer scan (RTS) and boundary scan.
- Test Compiler supports level-sensitive-scan design (LSSD), multiplexed-flip-flop scan, and hybrid scan.
- Scangen also supports LSSD, as well as scan path, scan set, and random-access scan.

One caveat: While both Scangen and Test Compiler offer the ability to create partial scan designs, neither Scangen's pattern generator nor Test Compiler can automatically create effective patterns for partial scan implementations.

Building a scan chain requires four pins. These four pins—Scan In, Scan Out, Clock, and a control signal—constrain the test patterns, causing them to be deep rather than wide. (Random-access scan demands more than four pins; addressing each storage element demands additional I/O for address lines.)

Deep, narrow patterns may create headaches for conventional IC testers whose memories are relatively short and wide. Therefore, if you can spare the pins by employing multiplexing or using spares, you can improve the efficiency of

Choose from eight flavors of scan.

The eight most popular versions of scan are level-sensitive scan design (LSSD), scan path, scan set, random-access scan, multiplexed flip-flop scan, hybrid scan, boundary scan, and register-transfer scan. Each version converts your sequential and combinatorial logic to a strictly combinatorial design. You make the conversion by building a chain of storage elements separated by combinatorial logic.

LSSD is probably the most popular scan technique. There are four primary rules that govern its use. Perhaps the most important rule is that you must connect all latches into a shift-register latch, then connect all shift-register latches into shift registers. In addition, all storage elements must be clocked dc latches. Observing these rules will help you build the scan chains correctly, force the design to be synchronous, and allow you to isolate data in the latches.

Another rule holds that multiple nonoverlapping clocks must control the latches. Data can only move from a latch through combinatorial logic to the next latch if nonoverlapping clocks clock the latches. These rules eliminate minimum circuit-delay system dependency and ensure that data at the input to a latch is stable while a latch clock is on.

Other scan alternatives are similar to LSSD. Scan path uses dual-clocked, dual-input D types rather than latches. One clock moves system data through the flip-flops; a second clock shifts data through the serially connected test inputs of the D types.

Scan set is a less invasive partial scan implementation that appends a scan-set register to your circuit. You load the register serially to drive logic values into your design at points where such control is otherwise difficult. Scan set is attractive because it doesn't restrict your selection of storage elements and it reduces circuit design interference. A disadvantage of scan set is that its pattern generation is complex and most of its register logic is only used during testing.

The penalties assessed by random-access scan are increased pin counts and extra logic for address decodes and addressable latches. This approach avoids the need for shift registers by making all latches randomly addressable. Whereas other scan approaches can use as few as four I/O ports, random-access scan requires at least six. These six are scan data-in, scan data-out, scan clock, test select, and two serial inputs for the X and Y addresses.

One of the simplest scan approaches is to use a flip-flop with a multiplexer at its input. You can connect flip-flops in a chain and use a test select pin to choose mission mode or test mode.

Hybrid scan builds a scan chain from unique storage elements. These elements are edge triggered in mission mode, like a D-type flip-flop, and level sensitive in test mode, like a latch. These storage elements are about 1.5 times the size of a typical D flip-flop.

Boundary scan uses a scan chain connecting the I/Os of an IC or functional block to provide control and observation of the device under test (DUT). Data enters the periphery through a Test Data In pin, circulates via boundary scan cells around the your testers by using multiple scan paths.

SilcSyn Test Synthesis Module, Scangen, and Test Compiler all give you a multiple-path option, but only the first two create multiple paths without significant manual intervention. Both of these tools require you to specify which scan chain a functional block's storage elements should belong to before they will create a scan path.

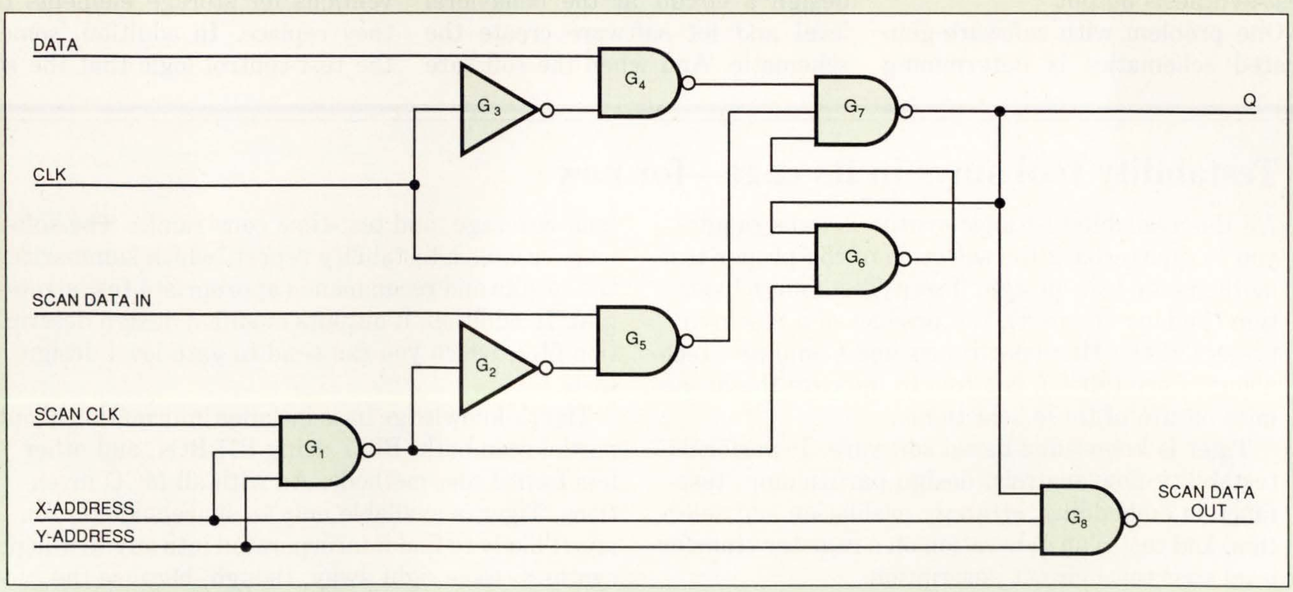
To create multiple paths in Test Compiler, you have to divide the storage elements in your design by the number of paths you want. Then you either mark elements for inclusion or exclusion from a particular scan chain. You have to repeat this process for each path you want to build. Finally, after creating these independent paths, you have to assemble the paths into a single circuit.

The major difference between Scangen and SilcSyn Test Synthesis Module or Test Compiler is the stage at which they begin to work on a design. Scangen is a testability insertion tool. It inserts scan-test logic into an existing design. Then, Teradyne EDA's ATPG software—included with Scangen—generates test patterns. The software replaces storage elements with the appropriate elements for the scan method you choose, then connects the scan chain. However, Scangen neither optimizes the design for speed and area nor creates schematics.

Scangen accepts a variety of structural-design input formats, such as EDIF (Electronic Design Interchange Format) 2 0 0; Mentor; the Tegas, Hilo, and Aida design

DUT, and exits via the Test Data Out pin. In addition to providing a method for testing a chip or a functional block, boundary scan can also test external wiring by applying test stimuli from the boundary scan cells on one chip and capturing the response at the input cells on the chip or chips it's connected to. (For a more detailed look at boundary scan, see **Ref 1**).

The above scan methods are most effective when you replace all storage elements with their corresponding scan elements. register transfer scan (RTS), on the other hand, is a partial scan technique. RTS demands that you insert scannable storage elements into global feedback paths so these paths can be broken during testing. Also, nonscannable-element clocks and resets must be inactive during testing. Although they use less chip area than full scan implementations, RTS and other partial scan approaches may present a difficulty, because you have to decide which storage elements you should make scannable.



To decode proper scan-latch addresses, *random-access scan requires addressable latches, pins for address lines, and address-decode logic.*

Test-logic synthesis

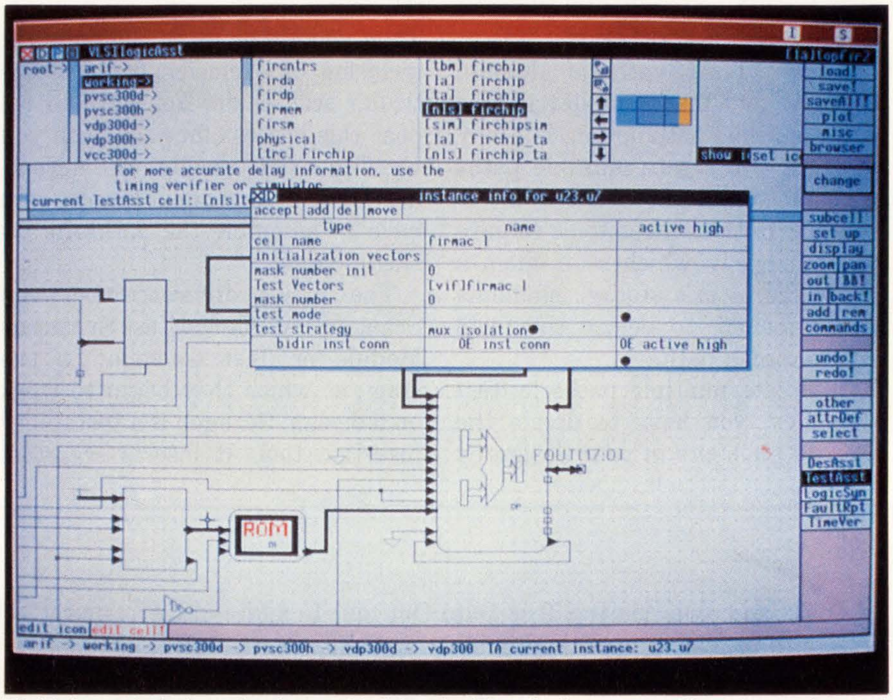
languages; LSI Logic, VLSI Technology, Fujitsu, and Toshiba design languages; and the vendor's Lasar and Vanguard netlist formats.

SilcSyn Test Synthesis Module and Test Compiler, on the other hand, are true logic-synthesis tools. Both can work with structural inputs such as EDIF, as well as Mentor, Valid, and LSI Logic design languages. In addition, SilcSyn Test Synthesis Module works with VHDL (VHSIC Hardware Description Language) and its own behavioral language inputs. Test Compiler can use behavioral inputs such as those in Verilog HDL, VHDL, Boolean equations, and state tables. To use some of its input formats, the Test Compiler software requires an optional interface.

You can, if you wish, disable the test-logic synthesis capability. If you create test logic, however, it becomes an integral part of the design and is therefore optimized with the whole circuit. SilcSyn Test Synthesis Module and Test Compiler can create schematics and test patterns for your design as part of their test-synthesis output.

One problem with software-generated schematics is determining the correspondence between function and logic. Finding the correspondence is far easier when you design a circuit at the gate level and draw its schematic than if you design a circuit at the behavioral level and let software create the schematic. And when the software synthesizes logic that isn't in your behavioral description, this correspondence is even more difficult.

To aid you, the synthesis programs retain your naming conventions for storage elements that they replace. In addition, some of the test-control logic that the soft-



Multiplexer isolation circuitry, *added by the Test Assistant, provides observation and control for deeply embedded nodes that might otherwise be untestable.*

Testability tool stays in its cage—for now

All the available test-logic synthesis tools require you to quarterback the selection of the proper test methods for your design. Tiger (Testability Insertion Guidance Expert), the product of a research project at the Microelectronics and Computer Technology Corp (MCC), is a tool to improve the hit-or-miss nature of those selections.

Tiger is knowledge-based software. It performs testability flow analysis, design partitioning, test-function embedding, strategy evaluation and selection, and test-plan generation on a register-transfer-level structural circuit description.

Using EDIF or VHDL circuit inputs, Tiger evaluates a design against performance, area-overhead, fault-coverage, and test-time constraints. The software creates a testability report, which summarizes the results and recommends appropriate test strategies. In addition, it outputs modified design description files, which you can send to gate-level design tools.

Tiger's knowledge base includes information about partial scan path, BIST using BILBOs, and other less formal test methods. As with all MCC inventions, Tiger is available only to shareholders. You aren't likely to find it incorporated into any test-logic synthesis tools right away, though, because the current version was written in LISP. A C++ version is in the works and should be available in late 1990.

ware adds is easy to identify. However, a significant portion of the other logic, because optimization software has merged it with the function logic, is difficult to pinpoint.

This loss of correspondence between your original design and the synthesized result may be disconcerting at first. Over time, however, two factors will ease your fears.

First, vendors will include concurrent-design and design-framework facilities in their software. These facilities allow you to specify an HDL (hardware description language) statement, gate, node, fault, or other descriptor in one file. Then the software will highlight the corresponding items in related files. Second, as you develop confidence in the software's conversion abilities, you'll have less and less need for these facilities.

Today, however, the synthesis software's ability to identify and remove redundant logic offsets the difficulty of identifying logic. Redundant logic is very difficult to test; therefore, it accounts for most of the untestable faults in designs. Scangen uses a test-design rules checker to identify redundant logic, but since it only adds scan logic, it can't eliminate the redundancy.

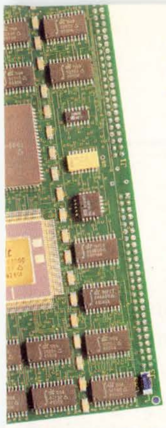
Scangen's test-design rules checker does more than just find redundant faults. It also makes sure that you've connected your scan chain correctly, that your clocking scheme doesn't violate scan requirements, and that your design doesn't use any uncontrolled feedback. Both SilcSyn Test Synthesis Module and Test Compiler also identify uncontrolled feedback paths, but none of the three tools can make these paths testable.

Perhaps the biggest difference between SilcSyn Test Synthesis Module and Test Compiler is in their approach to partial scan. Both tools allow you to exclude storage elements from the scan chain. Un-

Table 1—Test-logic synthesis software

Company	Product	Cost	Availability	Scan Methods	Redundancy id/removal	Other test methods	Automatic test pattern generation (ATPG)	Sequential ATPG
Dassault Electronique	Frenchip	$75,000	First quarter 1991	Full and partial boundary scan	Yes/Yes	Built-in logic-block observers (BILBOs) for built-in self test (BIST)	No	No
Racal Redac	SilcSyn Test Synthesis Module	$45,000 option to $60,000 SilcSyn ASIC design system	Third quarter 1990	Full and partial register-transfer scan and joint test action group (JTAG) boundary scan	Yes/Yes	None	Yes	Yes
Synopsys	Test Compiler	$25,000 option to $35,000 design compiler*	Dec 1990	Full and partial level-sensitive scan (LSSD), multiplexed flip-flop, and hybrid scan	Yes/Yes	None	Yes	No
Teradyne EDA	Aida ATPG Toolkit	$45,000	Now	Full and partial level-sensitive scan (LSSD), scan path, scan set, and random-access scan	Yes/No	None	Yes	No
VLSI Technology	Test Express	$35,000	Now	None	No/No	Multiplexer isolation and built-in self test (BIST) using linear-feedback shift registers (LFSRs) for RAMs, ROMs, and multipliers	Yes	No

Note: *Includes an EDIF 2 0 0 interface and one $1500 training voucher.



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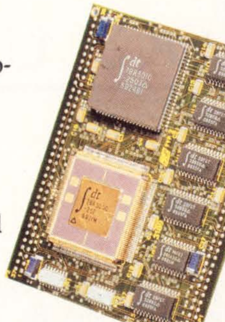
The IDT7RS101 and IDT7RS102 SubSystems are available in 12-, 16-, 20- and 25 MHz versions. They feature 64 KBytes and 16 KBytes each of instruction and data cache, respectively, an optional floating-point, and read and write buffers.



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MacStation™ Development System

The IDT7RS50 system provides a low-cost development environment for the Mac II. The MacStation system includes an R3000 add-in NuBus board, IDT/ux™, and a C compiler, and maintains the features and flexibility of the Mac.

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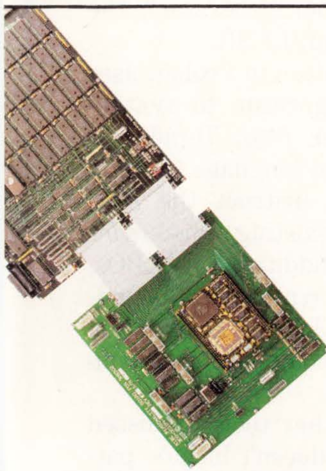

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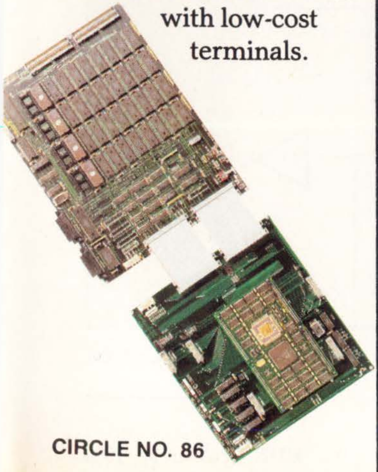

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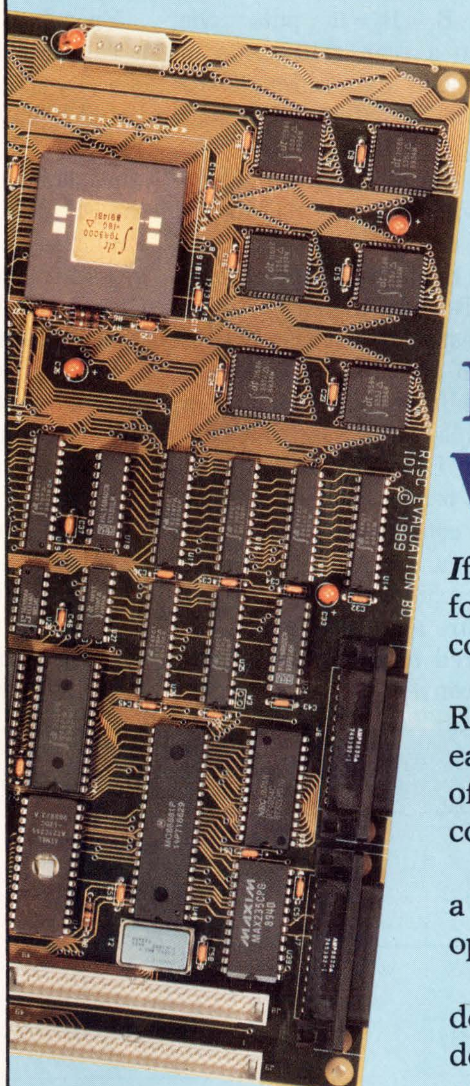

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fortunately, Test Compiler's pattern-generation software can't create high-fault-coverage test patterns for nonscannable sequential logic.

In contrast, SilcSyn Test Synthesis Module lets you specify a sequential depth so that the software can try partial scan approaches. A partial-scan test strategy might yield test results as efficient as those of a full-scan strategy on a smaller die. But creating the logic and patterns takes a heavy toll on CPU time.

A different synthesis approach is the basis of Frenchip, a logic-synthesis tool introduced at the 1990 Design Automation Conference by Dassault Electronique. In contrast to the scan approach of other tools, Frenchip uses a self-test technique based on built-in logic-block observers (BILBOs). Like the other true logic-synthesis approaches, Frenchip's finds and removes redundant logic.

A BILBO register **(Fig 1)** comprises a set of latches. These latches operate in four modes, determined by control signals B_1 and B_2. For normal operation as a parallel-input shift register, the control signal is $B_1 = B_2 = 1$.

Setting $B_1 = B_2 = 0$ puts the BILBO into a scan shift mode in which you feed data through the register from Scan In to Scan Out. Note that the NOR gate inverts the data before the latch stores it. Driving $B_1 = 1$ while $B_2 = 0$ initializes the register by resetting to zero.

The final mode, which you access by forcing $B_1 = 0$ while $B_2 = 1$, is the most interesting. In it the BILBO register can act either as a linear-feedback shift register (LFSR) or as a multiple-input shift register (MISR). An LFSR drives your circuit with a pseudorandom pattern; an MISR compresses circuit response into a characteristic signature. The circuit logic can compare this signature against a known reference stored either on or off the chip. You convert the register between LFSR and MISR via the Z_is. When these parallel inputs are all 0s and you have a nonzero value in the latches (as a seed for the pseudorandom number generator), the BILBO acts as an LFSR.

Frenchip, written in Prolog, uses a rule-based algorithm to synthesize logic either from Teradyne's Label behavioral language or from VHDL. If you instruct the software, it can use existing registers for the BILBOs. In addition to BILBOs, Frenchip also synthesizes boundary-scan and Joint Test Action Group (JTAG) compliant test controllers **(Ref 1)**.

Unlike the other tools discussed here, Frenchip doesn't include pattern-generation software. This omission isn't a serious handicap, however, because third-party ATPG software is available from many sources, including some of the vendors in this report. Be aware, though, that vendors tune ATPG-bearing synthesis tools for the types of patterns the ATPG soft-

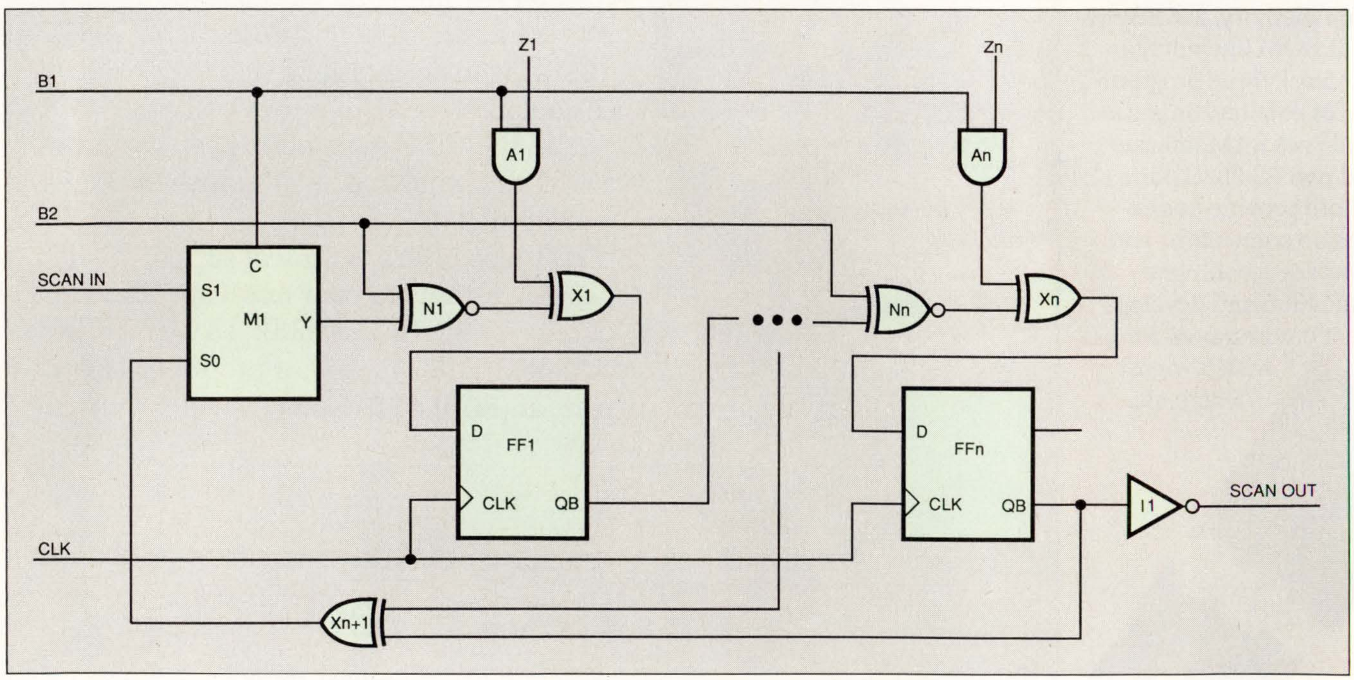


Fig 1—A built-in logic-block observer (BILBO) can initialize your logic, *function transparently, act as a scan register, or perform pseudorandom number generation and signature compression.*

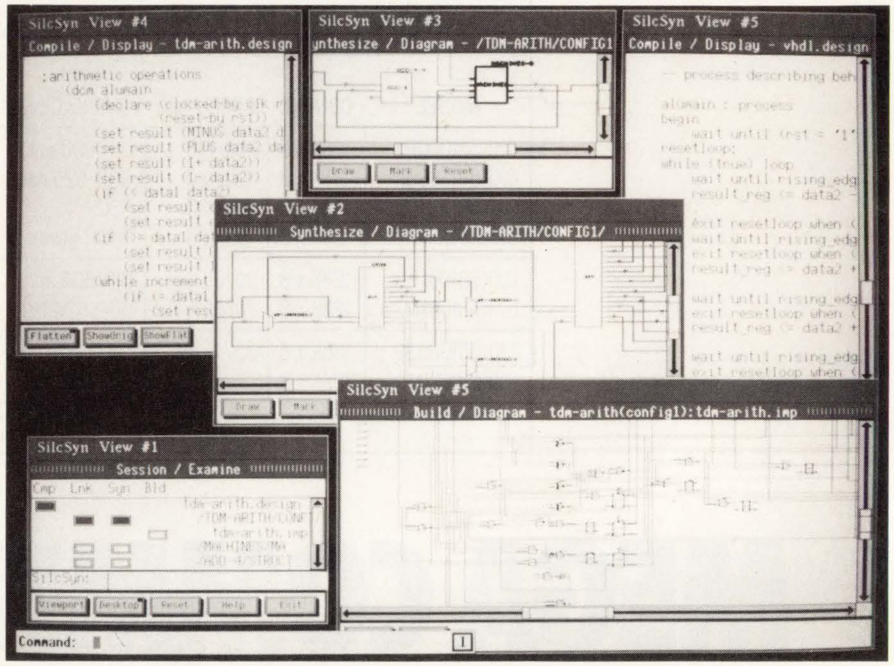
Test-logic synthesis

ware can generate. Being able to synthesize test logic is no guarantee that your pattern generator can create efficient patterns to test your design.

Test Express from VLSI Technology is another test-logic synthesis tool that relies heavily on BIST (built-in self-test). But although it synthesizes test logic, Test Express isn't a *true* logic-synthesis tool. It inserts test logic on an existing design, so it doesn't simultaneously optimize test and function logic. As a result, it can't eliminate redundant logic.

Using the company's internal netlist format (which is accessible through EDIF and Mentor-format translators), Test Express includes several function-test-logic compilers. These compilers build LFSRs and MISRs specifically for different function blocks. The software currently contains ROM, RAM, and multiplier BIST compilers.

Although VLSI Technology's cell libraries contain scan cells, such as LSSD latches, multiplexed flip-flops, and boundary-scan cells, Test Express doesn't yet synthesize the scan chains. However, the company offers interfaces to third-party tools



Synthesizing test logic and function logic at the same time, *as SilcSyn's Test Synthesis Module does, provides testable circuits that are optimized for performance and area.*

that do. Test Express does provide access to test points via multiplexer isolation.

Multiplexer isolation is an unstructured technique that provides control and observation of test points—as the name implies—with multiplexers. You select deeply embedded nodes for the test-logic-synthesis tool and it provides multiplexed access. If you put the chip into test mode, it brings these embedded nodes to the design's I/O.

Multiplexer isolation can help you test designs containing uncontrolled feedback paths. These paths are virtually untestable with scan techniques because you can't both con-

For more information . . .

For more information on the test-logic synthesis products discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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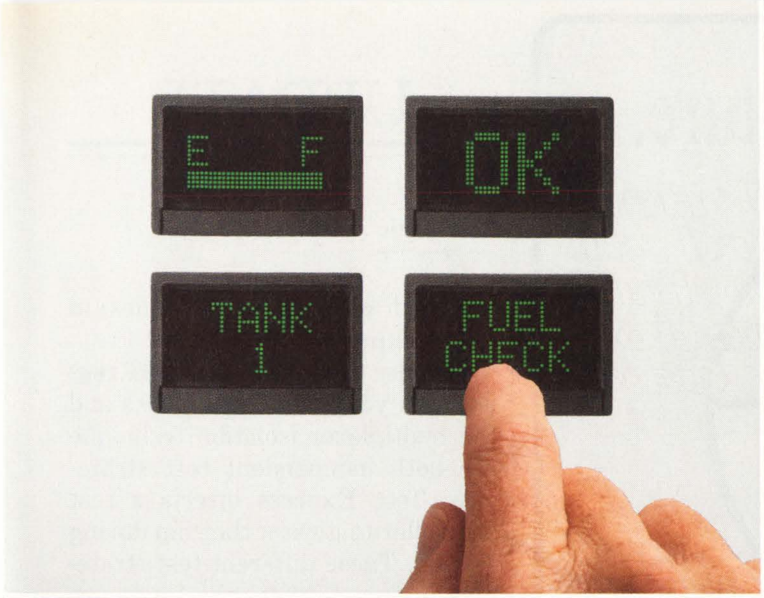
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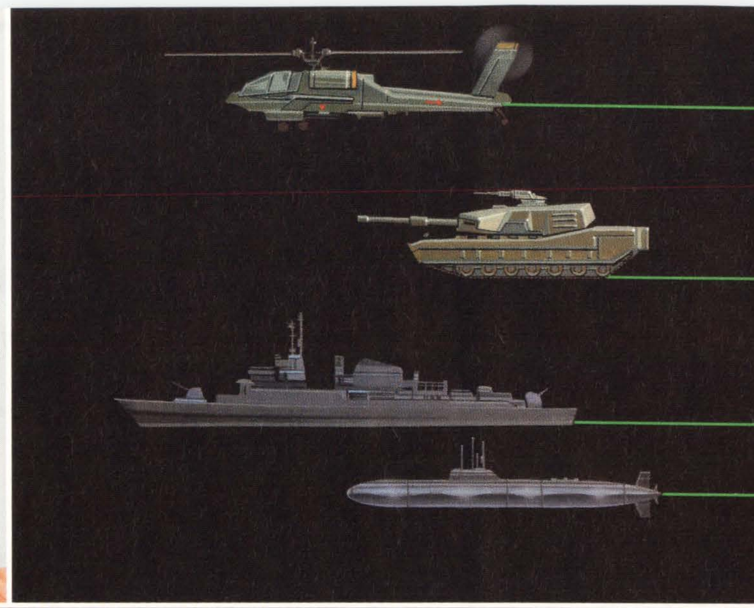

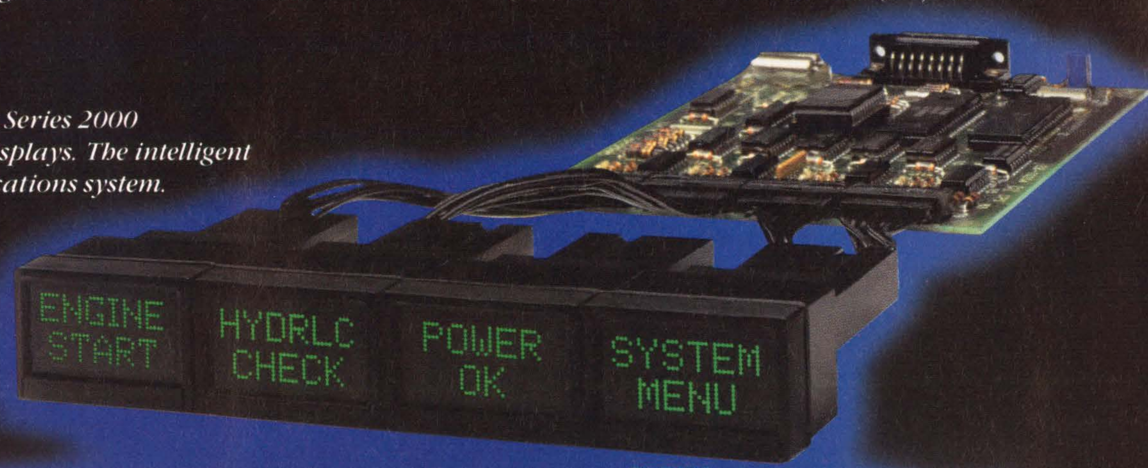
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Test-logic synthesis

trol and observe node values in these paths.

Because the creation of BIST registers in your functional blocks and the multiplexer isolation technique are both independent test strategies, Test Express inserts a test controller to govern the chip during testing. These different test strategies demand that the software provide schematics as an output.

Test Express's multiplexer isolation and BIST strategies allow you to test circuits containing multiple asynchronous clocks. These circuits, like those with uncontrolled feedback loops, are hard to test with synchronous circuit testers. Frenchip uses its BILBOs to test these problem designs. Of the scan-based test-logic synthesizers, only SilcSyn Test Synthesis Module can handle multiple-clock asynchronous circuits. Its test-logic synthesis strategy is to convert your design into a single-clock synchronous circuit in test mode.

These tools demonstrate the CAE industry's recognition that testability is a critical—and too-often overlooked—aspect of design. Judicious use of test-logic synthesis tools can give you more freedom to design circuits that are inherently testable. However, be wary of the marketing hype. CAE tools, like fine wine, often need to mature to allow their full capabilities to reach their peak. EDN

References

1. Quinnell, Richard A, "Adding testability also aids debugging," *EDN*, August 2, 1990, pg 67.

2. Bardell, Paul H, et al, *Built-in Test for VLSI*, John Wiley & Sons Inc, 1987.

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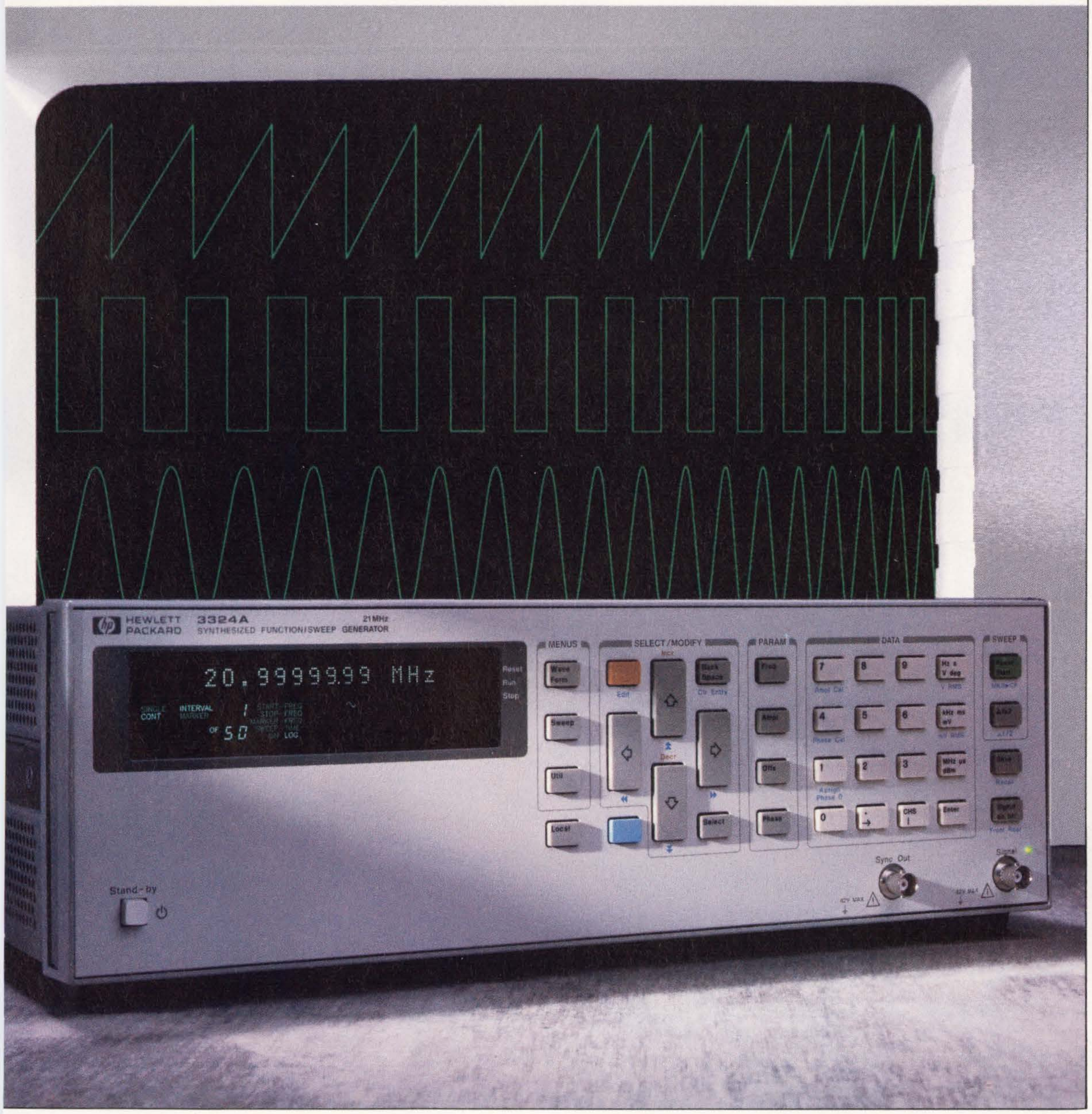

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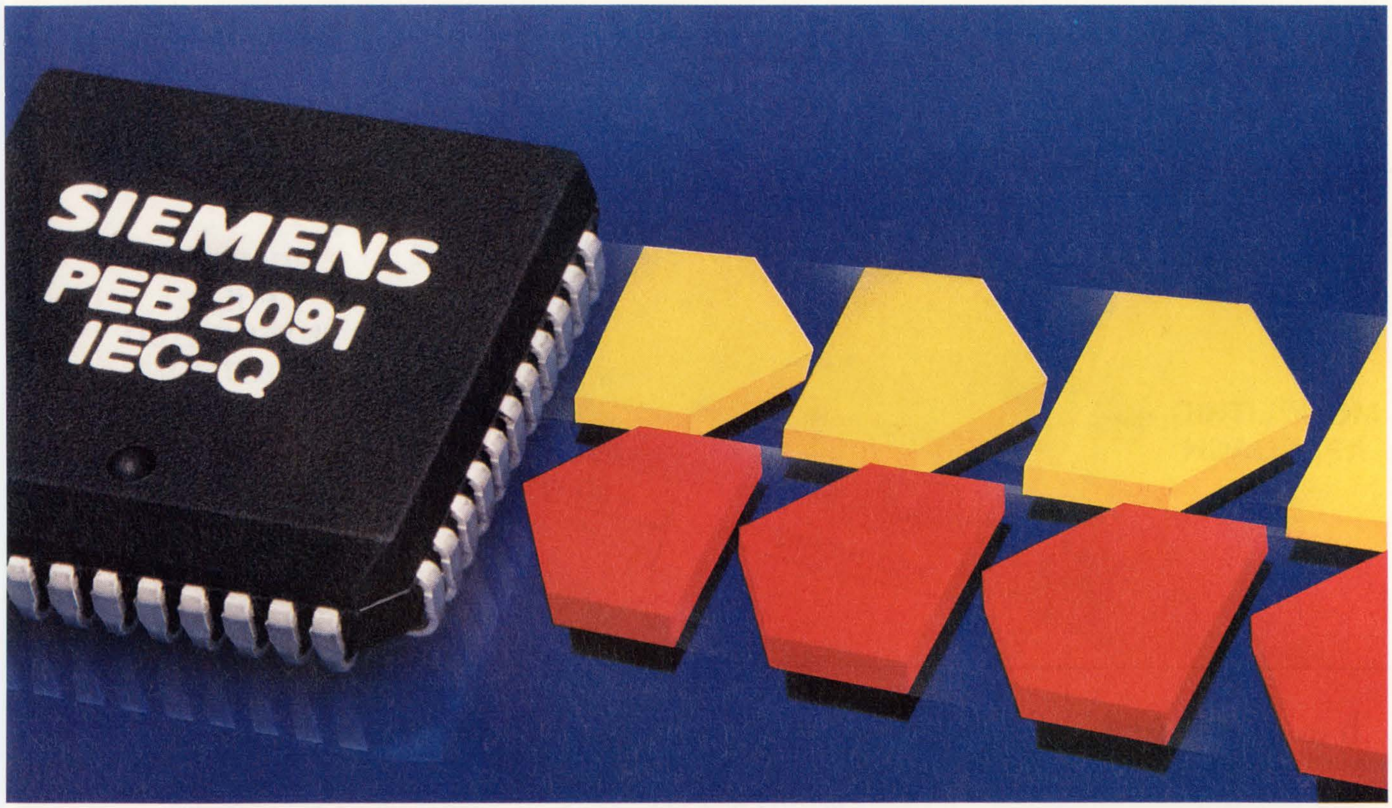

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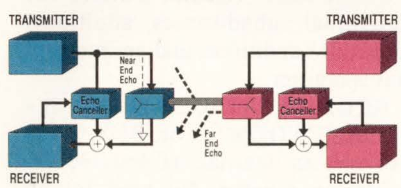

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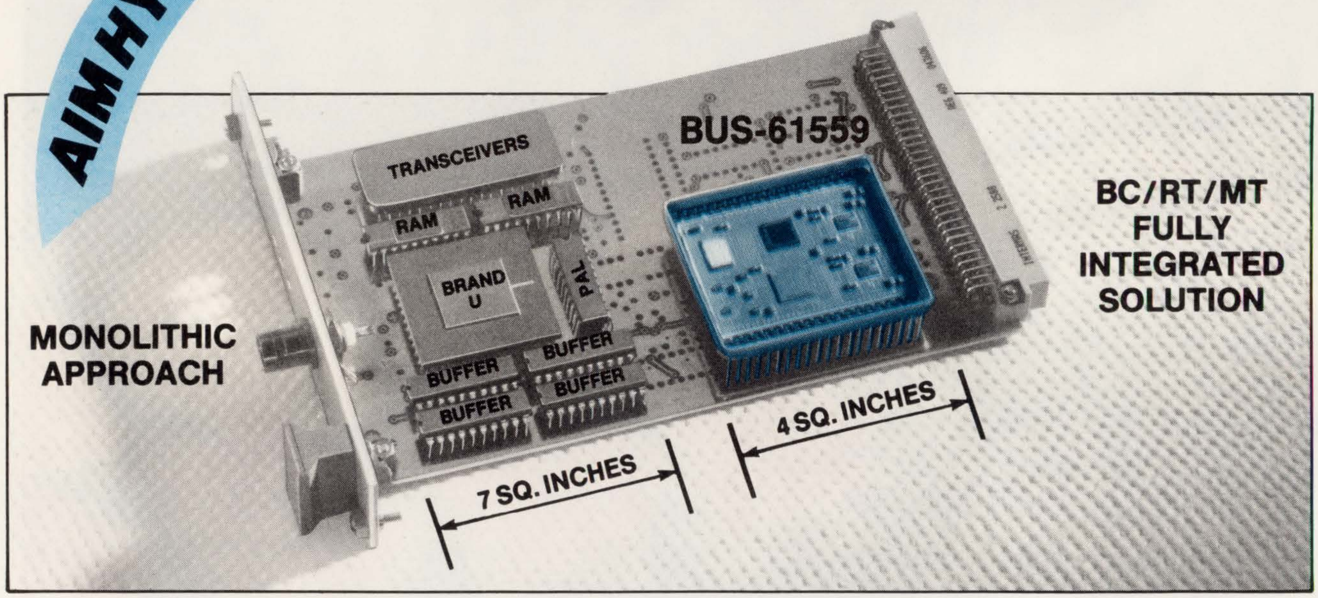

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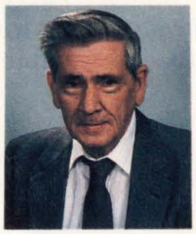
LARGE-AREA FLAT-PANEL DISPLAYS

Diverse technologies vie for dominance



A clear-cut winner has not yet emerged in the race to dominate the market for large-area flat-panel displays. Liquid-crystal types appear to be leading the pack—at least for now.

Dave Pryce,
Associate Editor

Flat-panel displays won't soon replace the omnipresent cathode-ray tube in traditional TV applications, but they continue to press ever closer to that goal. Indeed, a number of 6- to 18-in. flat-panel displays provide adequate resolution for such tasks. If not for their high cost, these displays would be quite acceptable.

While manufacturers strive to resolve this cost-performance obstacle, large-area flat-panel displays are finding a home in laptop computers, overhead projectors, and medical imaging and military equipment. These applications are less sensitive to mundane cost constraints and place great importance on high resolution. In many cases—notably laptop computers—the light weight and low-power consumption of a flat-panel display are as important as high resolution.

Flat-panel displays that can reproduce high-resolution text and graphics embrace three different technologies: electroluminescent, liquid crystal, and gas plasma. (See **box**, "The technology behind large-area displays" for a description of these technologies and the different types of displays within each.) Despite the obvious differences in technology and the more subtle differences in performance characteristics, these displays have one thing in common—relentless competition for the lion's share of a rapidly developing market.

There is not yet a consensus on which type will ultimately dominate the market. Historically, each of the display technologies has found wide acceptance in the marketplace, but the one that emerges as the eventual winner in the large-area-display market will have to offer a price/performance package that is acceptable to large-volume users. Although complete dominance is unlikely, liquid-crystal displays (LCDs) and electroluminescent displays appear to be the front runners, with LCDs presently enjoying a slight edge.

LCDs have intrinsic advantages

LCDs are popular because they are thin, lightweight, intrinsically rugged, and—except for backlighting requirements—they are low-power devices. Recent innovations in LCD technology, such as double supertwist and mono-

***Using third-party gray-scale controllers**, this 10-in. active-matrix LCD from Hitachi can display as many as 256 colors.*

chrome supertwist, have significantly improved the contrast and viewing angle of these displays. These improvements are particularly important for large-area displays used in high-resolution text and graphics applications. Active-matrix technology is also improving the performance of LCDs.

Several vendors, including Epson, Seiko, and Toshiba, offer monochrome LCD panels with viewing areas having diagonal measurements in the 8.5- to 11-in. range. Other vendors, notably Hitachi and Sharp, also have color LCD panels with diagonal measurements of about 10.4 in. Most of these displays feature a VGA-standard resolution of 640×480 pixels, which is suitable for high-performance applications. (See **box**, "Display standards" for a description of several standards that define pixel resolutions and color capabilities for high-resolution displays.)

LCDs using the older supertwist technology are popular in low-cost applications. Designers of high-performance laptop computers and workstations usually prefer double-supertwist or monochrome-supertwist displays because these types provide an almost pure black-and-white image. Monochrome-supertwist technology replaces the expensive glass layer of the double-supertwist display with an inexpensive, thin polymer retardation film. Because of lower production costs—and essentially identical performance—vendors increasingly use monochrome-supertwist technology instead of double supertwist.

A good example of a monochrome-supertwist display is Seiko's 10.9-in. G642G, which uses

The technology behind large-area displays

Of the various technologies available for fabricating flat-panel displays, only three are suitable for manufacturing dot-matrix displays that can reproduce sizable amounts of information with high resolution. These three technologies are electroluminescent, liquid crystal, and gas plasma. Each has distinct attributes and performance characteristics.

Electroluminescent display (ELD): ELDs employ phosphors such as manganese-doped zinc sulfide that luminesce when subjected to a high voltage. The typical electroluminescent display consists of a stack of thin-film layers that have been vacuum deposited on a glass substrate. Transparent dielectric layers sandwich the center phosphor layer. Perpendicular row and column electrodes form the two outside layers. ELDs feature a wide viewing angle and exhibit an amber-on-black display with high brightness and high contrast. Because these displays use a light-generating technology, they don't require space- or power-consuming backlights.

The two principal types of ELDs are ac thin-film (ACEL) and dc thick-film (DCEL) displays. DCEL panels are essentially resistive devices. ACEL panels, which contain dielectric layers, are essentially capacitive devices. Both types can produce approximately the same levels of brightness, contrast, and resolution. The differences are in claimed cost advantage and expected lifetime. Because of fewer process steps, DCEL panels are potentially less costly to manufacture. Older ACEL displays sometimes showed latent images, but symmetric drive techniques have solved this problem. A lifetime problem once associated with electroluminescent panels, particularly the dc variety, has been solved by using new materials and circuit techniques. The lifetime of today's electroluminescent panels is more than 10,000 hours—equal to that of a CRT.

The development of electroluminescent panels is proceeding at a rapid pace, but manufacturers have yet to put a color ELD into commercial production. The major stumbling block to the success of a color ELD has been the development of a blue phosphor of sufficient light intensity. Although the percentage of white luminance required from each of the primary colors is much less for blue than it is for red or green, this paradox remains a problem.

Liquid-crystal display (LCD): In a twisted-nematic LCD, a liquid-crystal mixture is sandwiched between two glass plates that are coated with a polarizer and lined with transparent electrodes. A low-voltage electric field aligns the nematic molecules (crystals) so that they either transmit or block the polarized light. LCDs are thin, durable, and lightweight. In their simplest form, these displays are also quite inexpensive and consume little power. The main disadvantages of the basic twisted-nematic LCD are low brightness, poor contrast, and reduced performance as display size increases.

Although all LCDs work on the same basic principles, there are a number of variations that greatly the company's retardation-control-film technology to create a "page white" effect. The display has a resolution of 640×480 pixels (dots), a dot size of only 0.30×0.30 mm, and a contrast ratio of 12:1. The display also features 16 gray-scale levels, an important feature in graphics applications.The display is less than 0.6 in. thick, weighs 750g, and dissipates approximately 2W. Most of this power is used by the fluorescent backlight; the display needs only about 350 mW. In sample quantities, the G642G costs $500.

Other displays that use polymer film to achieve a high-contrast black-on-white image include Toshiba's 9.75-in. TLX-1551-C3M and Epson's 8.8-in. EG9007. Both of these displays have a resolution of 640×480 pixels. The Toshiba panel sells for $604 (samples). The Epson panel costs $285 (100).

Distinguishing features of Epson's display include a weight of 680g and a thickness of 0.33 in. The extremely narrow profile of this display results from its flexible pc board, which is both compact and lightweight. With its side-mounted fluorescent backlight, the EG9007 dissipates approximately 3W. The display's 120-nsec response time compares with 300 msec for the typical large-area LCD and 50 msec for active-matrix LCDs.

Active-matrix technology

Many LCDs use monochrome-supertwist technology to improve performance; others use an active-matrix technology. In active-matrix displays, an active device behind each pixel switches the pixels on and off. Both 2- and 3-terminal active devices can control the pixels (**Fig 1**). One 2-terminal method uses

improve the performance of the basic twisted-nematic display (**Ref 1**). The types commonly used for large-area displays are supertwist, double supertwist, monochrome supertwist, and active-matrix. Because many viewers find the blue tinge of most supertwist displays unacceptable, the trend is toward the use of the latter three types.

To produce a high-contrast black-and-white image, double-supertwist LCDs use a color-compensating cell and monochrome-supertwist LCDs use an optical retarder made from a polymer material. These types of LCDs usually require a fluorescent backlight to compensate for transmission losses; other types can get by with a lower-power electroluminescent backlight. Conventional dot-matrix LCDs use a matrix-addressing technique to address the columns in parallel as the rows are addressed sequentially.

The more recent active-matrix displays use thin-film transistors or diodes to turn each pixel on and off. Featuring a wide viewing angle, high contrast, and a fast response time, active-matrix displays provide an elegant solution to the problems inherent in large, high-resolution LCDs. With the addition of red, green, and blue filters, an active-matrix display is an ideal vehicle for the reproduction of color images. Because of their greater complexity and lower production yields, however, active-matrix LCDs are quite expensive.

Plasma display panel: A plasma display panel contains a gas, usually neon, that glows when subjected to a high voltage. In a dot-matrix display, this voltage is applied between two sets of electrodes, which run perpendicular to each other to form rows and columns. Plasma displays exhibit an orange or red-orange color on a black background and have high brightness and a wide viewing angle. Although measurements can indicate otherwise, the human eye perceives this color combination to be lacking in contrast, particularly for graphics applications.

The three basic plasma technologies are dc refresh, ac refresh, and ac memory. The ac-memory display contains dielectric layers that separate the gas from the activating electrodes. The dielectric restricts the electrodes to capacitive coupling with the gas, a condition that lets the gas stay lit for a finite period—usually until another signal turns it off. This action provides an effective "pixel memory," thereby eliminating the need for screen refresh. Both ac- and dc-refresh types require refreshing at least once every 1/60 of a second to prevent observable flicker.

Notes

1. Flat-panel displays use a digital technology that requires a dot-clock signal to tell the host system how fast to read the individual pixel information from the system to the panel. Analog CRT displays do not need this signal.

2. The brightness of a flat-panel display is usually measured in footlamberts (fL) or in candelas per square meter (cd/m^2). These terms have the following relationships: fL = 3.424 cd/m^2 and cd/m^2 = 0.292 fL.

Large-area flat-panel displays

diodes with a metal-insulator-metal structure; another uses silicon nitride to provide a nonlinear impedance. The more common 3-terminal method uses amorphous silicon thin-film transistors to activate the pixels.

The 9.5-in. G644G from Seiko is a 2-terminal active-matrix display that uses the company's metal-semi-insulator technology. The display features a resolution of 640×480 pixels, a contrast ratio of 12:1, and a maximum response time of 50 msec. With a dot size of only 0.242×0.260 mm, the display produces images that are quite sharp. This lightweight (460g) display costs $1200 (samples). A companion device, the 10-in. G646G, has a 640×400-pixel resolution and costs $1000.

Not to be outdone by their monochrome siblings, active-matrix displays are also available in living color. A pair of 10-in. panels from Hitachi and Sharp are good examples of state-of-the-art LCD technology. These displays use thin-film transistors in a 3-terminal active matrix.

***Containing 921,600 pixels**, this 10-in. color LCD from Sharp Electronics has a VGA-compatible resolution of 640×3×480 pixels. The display uses an active-matrix technology with a thin-film transistor for each pixel.*

The TM26D01VC 10.4-in. panel from Hitachi is an 8-color display with an overall size of 8.5×11.2×0.6 in. Including the backlight, the display is about 0.8 in. deep. It features a resolution of (640×3)×480 pixels for a total count of 921,600 pixels. The pixels are arranged in vertical stripes of green, red, and blue. Each dot comprises three 0.11-(H)×0.33-mm (V) pixels, for a total dot size of 0.33×0.33 mm.

The display has a response time of 50 msec and a typical contrast ratio of 20:1. Six cold-cathode fluorescent tubes give the display a brightness of about 24 fL. Later this year, Hitachi will replace these tubes with two hot-cathode fluorescent tubes, which will reduce total power consumption from 17 to 12W and increase brightness to about 30

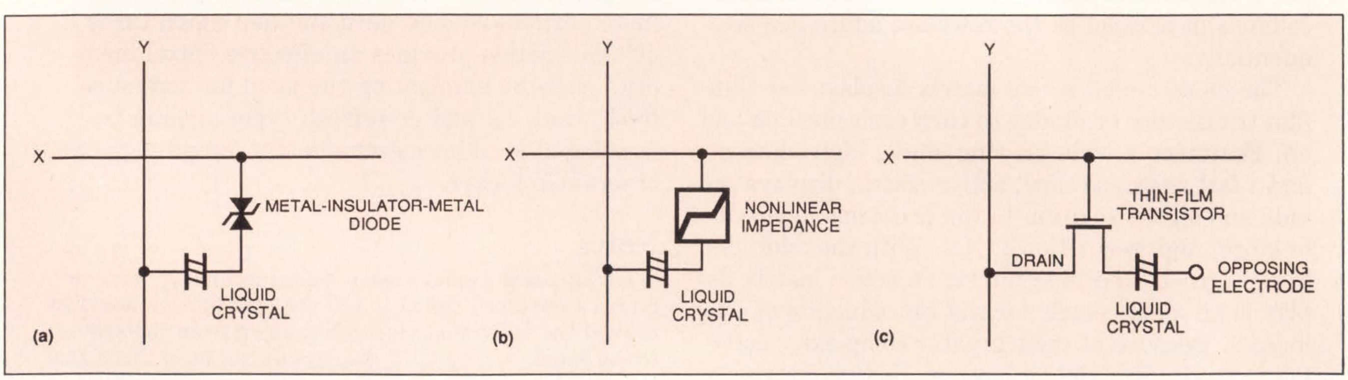


***Fig 1—Active-matrix LCDs use either 2- or 3-terminal devices** to switch pixels on and off. One 2-terminal method **(a)** uses diodes with a metal-insulator-metal structure. Another 2-terminal method **(b)** uses silicon nitride to provide a nonlinear impedance. The 3-terminal method **(c)** uses thin-film transistors in which the drain leads are connected to form column-selecting (Y) terminals and the gate leads are connected to form row-selecting (X) terminals.*

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GRAPHIC DISPLAYS/MODULES

Futaba Display	Futaba Module	Pixels (Row X Char.)	Brightness (FT-L)	Module Dimensions (in.)
GP1005B	GP1005B03	128X64	400	7.28X3.35X1.77
GP1010B	GP1010B01	176X16	200	7.32X2.16X1.70
GP1009B	GP1009A04	240X64	200	6.2X2.76X1.57
GP1006B	GP1006B05	256X64	200	9.84X3.35X1.77
GP1002C	GP1002C07	320X240	100*	7.10X6.30X1.60
GP1018A	GP1018A01	400X240	40	7.10X6.30X1.61

*Different Versions Available

DOT MATRIX/CHARACTER DISPLAY MODULES

Futaba Display	Futaba Module	Char. X Row	Dot Format	Char. Ht. (in.)	Module Dimensions (in.)
16LD03G	M16LD03B	16X1	5X7	0.433	8.90X1.95X.98
16SY11G	US16SY03E	16X1	14 Seg Alpha	0.200	4.92X1.32X.83
16MY0XX	US16MY02AA	16X1	14 Seg. Alpha	0.437	6.97X1.26X0.69
20SD03G	M20SD03	20X1	5X7	0.200	5.91X1.22X1.05
40SD04G	M40SD04	40X1	5X7	0.200	9.45X1.38X1.14
162SD03G	US162SD03XX	16X2	5X7	0.178	4.32X1.98X1.02
202MD01	M202MD01BA	20X2	5X7	0.443	10.75X3.0X1.28
202SD08G	M202SD08	20X2	5X7	0.200	6.10X1.69X1.18
402SD06G	M402SD06	40X2	5X7	0.200	9.45X1.69X1.18

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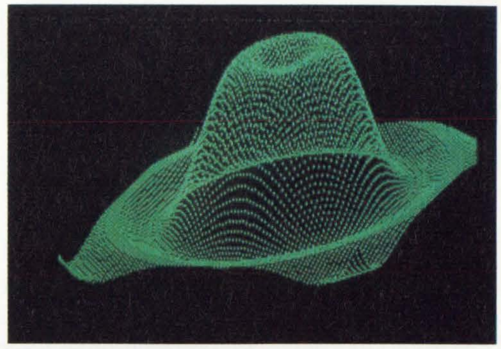

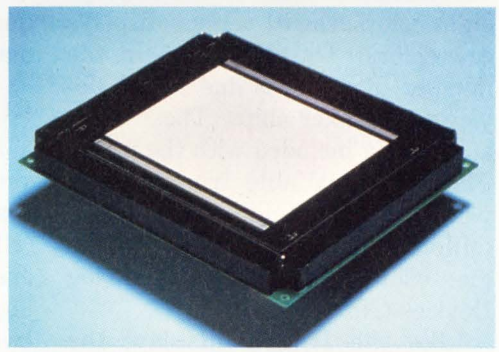

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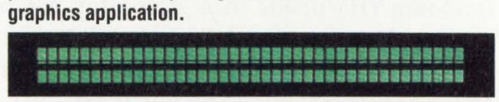
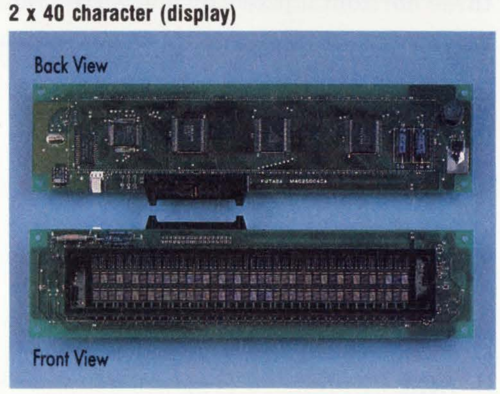


2 x 40 character (display)



2 x 40 character (module)

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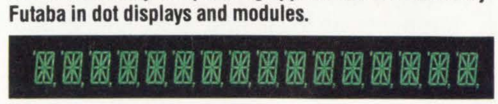

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CIRCLE NO. 52

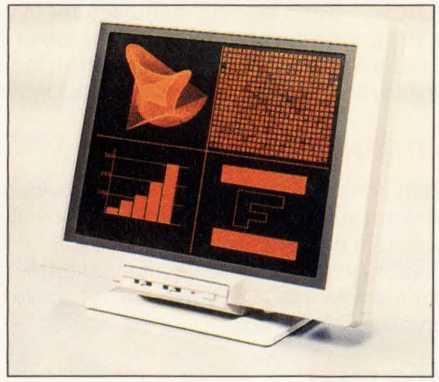
Large-area flat-panel displays

fL. With third-party gray-scale controllers, the 8-color display can produce as many as 256 colors. The TM26D01VC costs $3500 in sample quantities and will have an OEM price of approximately $2000. In addition to this 10-in. display, Hitachi makes 5- and 6.3-in. color displays.

Another 10.4-in. color display comes from Sharp Electronics. Similar to the Hitachi panel, Sharp's LQ10D01 and LQ10D02 feature a response time of 50 msec and a resolution of 640×3 (RGB)× 480 pixels. The 02 version displays eight colors; the 01 version displays 512 colors. The difference in the number of colors is due to the device's controller chips. These chips are usually included with the panel. They are available from several vendors, including Cirrus Logic (Milpitas, CA), Chips and Technologies (San Jose, CA), and Analog Devices (Norwood, MA).

Like the Hitachi display, the Sharp displays align the 0.11-(W)× 0.33-mm (H) pixels in a stripe format, rather than the delta (triangle) format. The stripe format employs three horizontal pixels by one vertical pixel for each dot. Compared to the delta format, the rectangular-based stripe format provides a more accurate display of graphics and text—an important factor for high-end laptop computers and workstations.

Sharp's LQ displays dissipate about 15W. The 2-tube hot-cathode-fluorescent backlight dissipates almost 14W of this total; the drive electronics dissipate the rest. Presently available as engineering samples, the displays cost $6300. Production is scheduled for the first quarter of 1991; the vendor estimates production pricing at $2000.



***This ac-memory plasma panel**, the FPF12000S from Fujitsu, has a 15-in. diagonal measurement. With a 1024×768-dot resolution, its orange-on-black display is suitable for graphics-intensive applications such as desktop publishing and CAD/CAE/CAM.*

ELDs are also in the race

Although the number of LCD vendors and products far surpasses that of electroluminescent displays (ELDs), ELDs are strong contenders in the developing market for large-area flat-panel displays. The two major domestic suppliers of ELDs are Planar Systems and Cherry Electrical Products. The Planar and Cherry electroluminescent panels are similar in performance and general appearance, but they differ substantially in technology. Planar manufactures ac thin-film (ACEL) panels; Cherry has chosen the dc thick-film (DCEL) approach.

Planar Systems is currently merging with Finlux, a previously competitive European supplier. The company offers a wide range of electroluminescent panels. Perhaps most notable is the 18-in. EL751214M monochrome display, which contains 880,000 addressable

Display standards

Several standards define the pixel resolution and color capabilities for high-resolution displays:

CGA—Color-graphics adaptor: Specifications include a resolution of 640×200 pixels in the 2-color graphics mode and 320×200 pixels in the 4-color graphics mode (from a palette of 16 colors). The 40-and 80-column text modes support all 16 colors.

EGA—Enhanced-graphics adaptor: Specifications include a resolution of 640×350 pixels with 16-color capability (from a palette of 64 colors). This standard supports at least nine text and graphics modes with resolutions from 320×200 to 720×350 pixels, including CGA emulation.

Hercules: A monochrome-only standard that provides resolution of 720×348 pixels for both text and graphics. In the text mode, this standard supports a universally accepted 25-row×80-column display.

VGA—Video-graphics array: Specifications include a resolution of 640×480 pixels in the 16-color mode and 320×200 pixels in the 256-color mode (from a palette of 262,144 colors). This standard supports at least 10 other text and graphics modes with resolutions of 320×200 to 720×400 pixels, including CGA and EGA emulation. VGA has become the de facto minimum standard for high-resolution graphics applications.

Some displays can provide resolutions of 800×600 pixels (Super VGA) or 1024×768 pixels (IBM 8514), but these standards are not always downward compatible with CGA, EGA, and VGA.

CIRCLE NO. 53

Large-area flat-panel displays

***This electroluminescent display**, the EL751214M from Planar Systems, features a diagonal measurement of almost 18 in. The monitor has a viewing angle of 160°, weighs less than 15 lbs, and takes up less than 50 in.² of work area.*

pixels with a matrix of 1024×864. This display features a viewing angle of 160°, a contrast ratio of greater than 20:1, and a pixel brightness of 20 fL. The terminal weighs approximately 15 lbs and dissipates about 60W of power.

The EL751214M is a complete terminal, which includes the power supply, interface, and enclosure. The terminal interfaces to IBM PC/XT and PC/AT, Macintosh II, and Digital Equipment Corp computers. With a selling price of $6500 to $10,000, this 12×14-in. panel is not for those with shallow pockets.

Cherry Electrical Products takes a different approach to manufacturing its electroluminescent panels. It uses a dc resistive technology rather than the ac capacitive technology used by Planar. Cherry maintains that DCEL panels are not only less expensive to make, but also offer advantages in power efficiency at high-frequency refresh rates. For example, a DCEL panel can accept video data to the display columns at rates as fast as 60M bps—a frame rate of 240 Hz for a 640×480-pixel display. According to Cherry, this high column-data rate increases luminance and power efficiency and allows gray-scale generation by means of frame-rate modulation.

Cherry offers several DCEL panels in sizes ranging from 4.7 to 9.8 in. and resolutions as high as 640×480 pixels. Its latest device, the 4.7-in. ELID-D000, has a viewing area of 3.68×2.94 in. and a pixel organization of 320 columns by 256 rows. Designed for portable and fixed-base instrumentation applications, this display features a brightness of 25 fL and a contrast ratio of 25:1.

Using a 12V regulated power

For more information . . .

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Large-area flat-panel displays

Using a 2-terminal active matrix, *this monochrome LCD from Seiko Instruments has a 10-in. diagonal viewing area and a resolution of 640×400 pixels.*

source, the display's built-in dc/dc converter automatically adjusts the voltages so that the panel's brightness will not vary during the first 10,000 hours of normal use. In single quantities, the ELID-D000 costs $600; in OEM quantities (10,000), it costs $215.

Despite the apparent leadership position enjoyed by LCDs and ELDs in the race for the large-area-display market, plasma displays are still strong contenders. Among the earliest of the flat-panel technologies, plasma displays are found in a range of simple to complex applications. They have not taken a back seat to the other technologies in the development of large-area displays capable of handling large amounts of information with high resolution.

Witness the FPF12000S ($5000) ac-memory plasma monitor from Fujitsu. With a 15-in. diagonal measurement and a resolution of 1024×768 pixels, this display suits office-automation and workstation applications. The entire monitor, including circuitry and casing, has a 3.5-in. profile and weighs 4 lbs. The monitor case includes a keyboard-connection terminal, a power switch and indicator lamp, and brightness and volume controls.

The monitor has the characteristic neon-orange-on-black display of a plasma panel. Its specifications include a brightness of 5 cd/m^2, a contrast ratio of 20:1, and a viewing angle of 160°. The unit consumes approximately 70W and has a 50,000-hour MTBF rating. Fujitsu offers large-area plasma displays ranging in size from 10 to 18 in. and with resolutions of 640×400 to 1024×816 pixels.

Several other companies also offer plasma displays. Panasonic, for example, makes a 10.5-in. dc plasma panel with a resolution of 1024×768 pixels. Because of plasma panels' inherent ruggedness, they have found acceptance in industrial and military applications. Plasma panels are widely used in laptop computers and workstations, but they may lose favor in these applications to the more aesthetically pleasing liquid-crystal and electroluminescent types.

The final winner in the race for dominance of the flat-panel-display market may enjoy only a narrow victory. Indeed, because of the variety of applications, all three technologies may coexist indefinitely. The one factor that could significantly alter respective market shares is the extent to which color panels become preferable to monochrome. Color LCDs seem to have a clear advantage over the other types. **EDN**

Reference

1. Pryce, Dave, "Liquid-crystal displays," *EDN*, October 12, 1989, pg 103.

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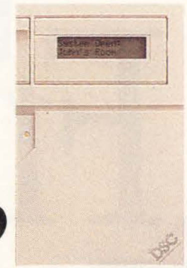

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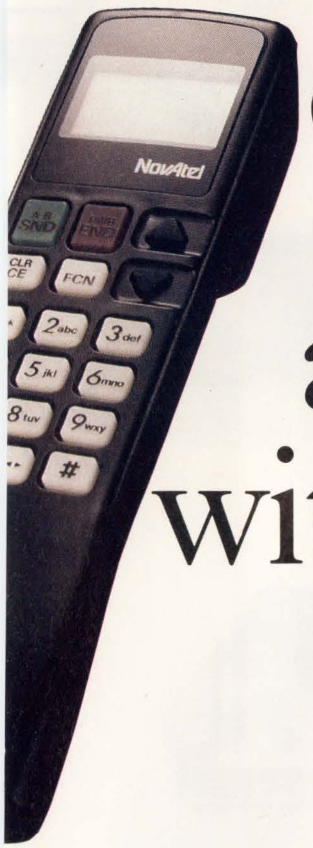

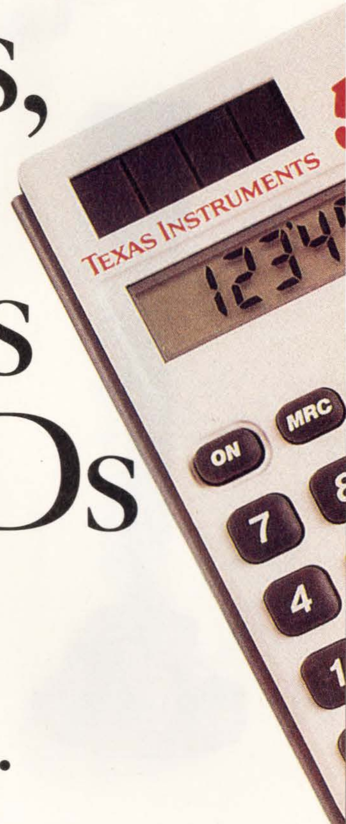

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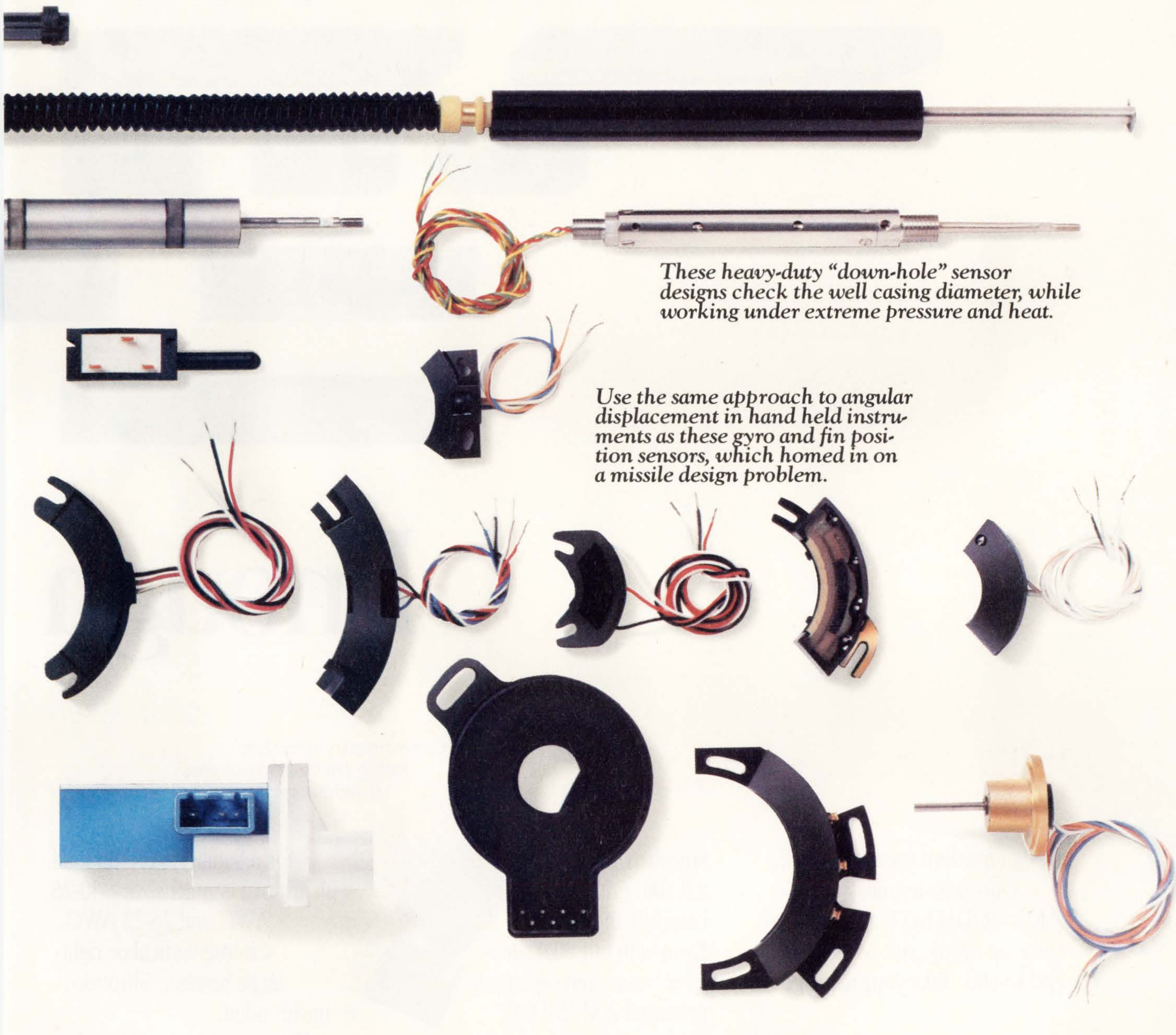

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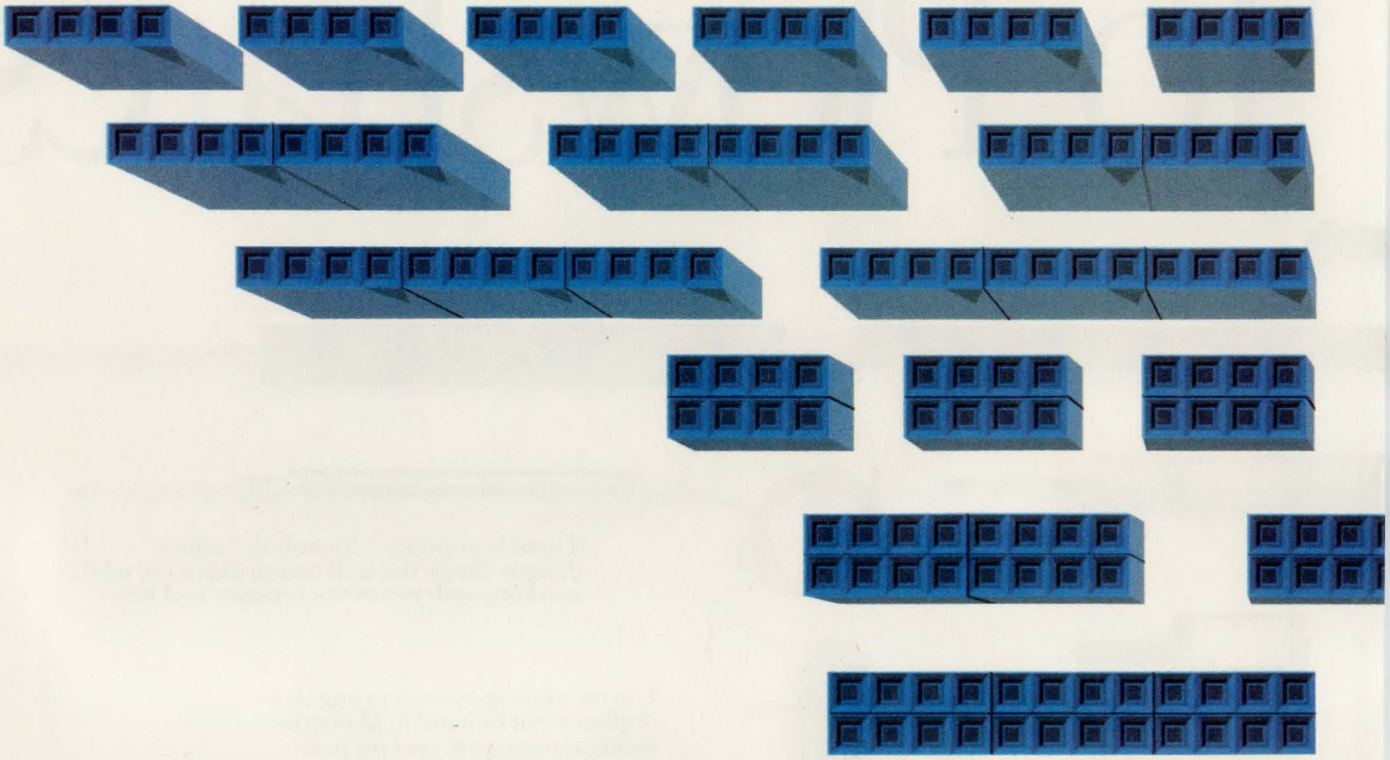

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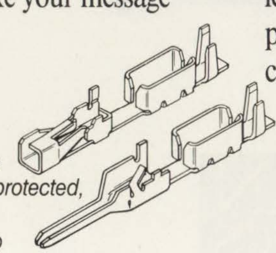

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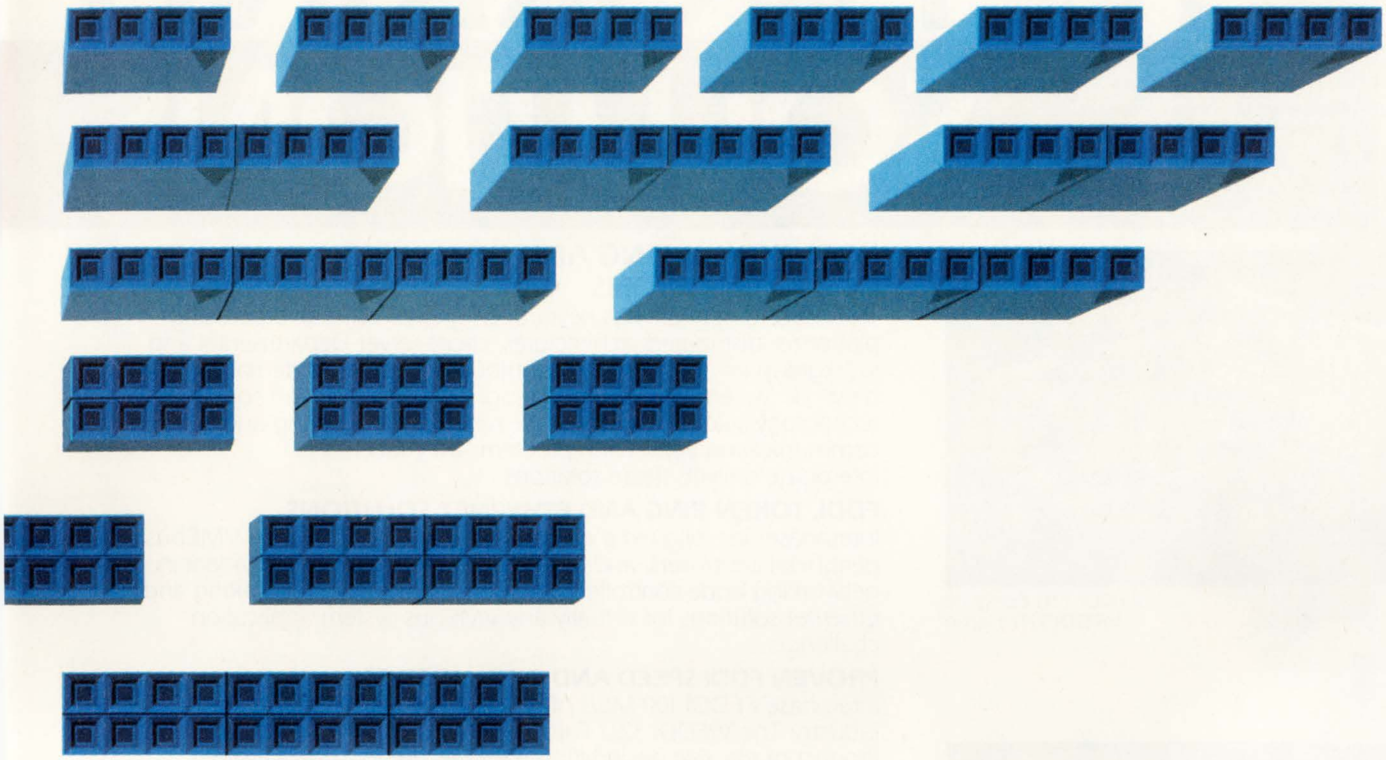

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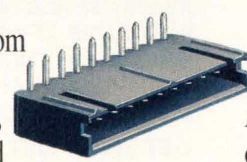

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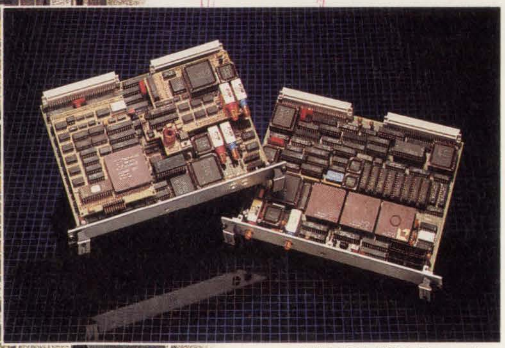
AMP Interconnecting ideas

CIRCLE NO. 56

NETWORKING SOLUTIONS



V/FDDI 4211 Peregrine
V/FDDI 3211 Falcon

FDDI, TOKEN-RING AND ETHERNET COMMUNICATIONS

The need to network has never been greater. Diverse processing platforms, distributed architectures, client-server, departmental and workgroup environments all contribute to increased demands on the network. System and network designers need a proven source of technology solutions for the wide range of networking and communication application problems they face.
Interphase delivers those solutions.

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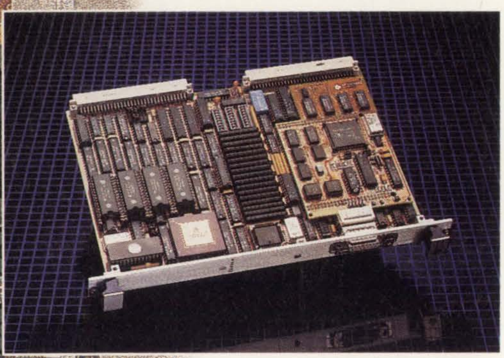
Interphase has long led the industry in high-performance VMEbus peripheral controllers, and that same leadership is now evident in networking node controllers. Interphase has FDDI, Token-Ring and Ethernet solutions for virtually any VMEbus system application challenge.

PROVEN FDDI SPEED AND INTELLIGENCE

Interphase's FDDI 100 Mb/s offerings are a logical choice for the industry. The V/FDDI 3211 Falcon received *UnixWorld* magazine's Product of the Year designation and was the industry's first 6U VMEbus FDDI solution. Interphase's newest FDDI product is the V/FDDI 4211 Peregrine, a RISC-based high-performance node controller capable of link level operation or on-board protocol processing. The Peregrine provides single or dual attach configurations, with SMT (Station Management Software) running on-board, all in one 6U VME slot.



V/Token-Ring 4212 Owl

TOKEN-RING RESULTS

The V/Token-Ring 4212 Owl is an ultrafast Token-Ring node controller based on the partitioned architecture of Interphase's proven Eagle class of controllers. The Owl facilitates connectivity of UNIX® systems, workstations, supercomputers or any other VMEbus system into an IBM® environment using IEEE 802.5 Token-Ring. This multiple processor design provides an elegant queued interface to the system supporting IEEE 802.2 LLC, and a flexible 4 or 16 Mbit interface to the Token-Ring network.

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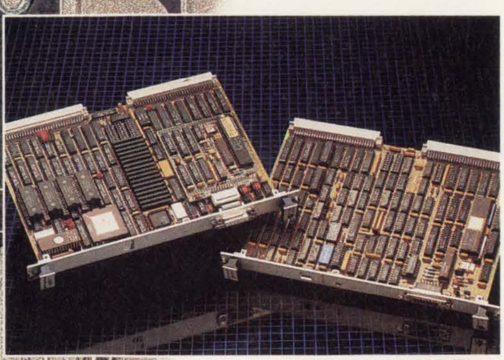

V/Ethernet 4207 Eagle
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CIRCLE NO. 57

OPTOELECTRONIC DEVICES

Improvements unleash new application areas

The current crop of optoelectronic devices offer better performance and wider operating capabilities than the components that were available even a year ago. As a result, you may now be able to replace your mechanical sensors and transformers with solid-state emitters and detectors.

J D Mosley,
Regional Editor

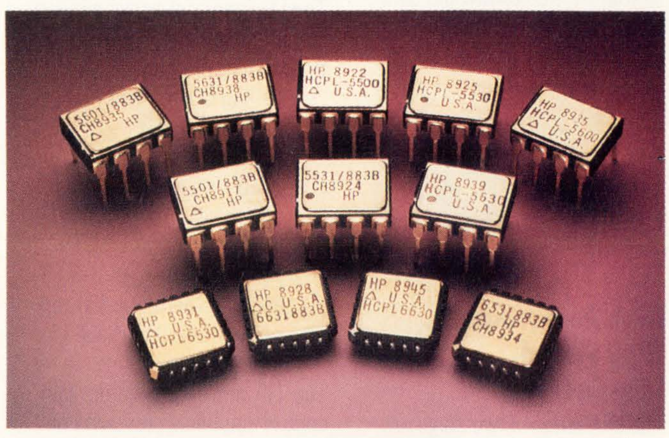
For as little as forty cents per component, optoelectronic devices can provide electrical isolation between circuits, let machines sense light and objects, and offer an alternative medium to copper wires for transmitting information. Technological advances, such as the use of aluminum gallium arsenide (AlGaAs) in LEDs, now make possible twice the power output of the older-generation gallium arsenide (GaAs) LEDs, in addition to yielding a pronounced improvement in coupling efficiency.

Improvements in packaging technology have produced new plastics that lower the cost of using optical sensors and emitters in harsh environments that previously necessitated expensive metal casings. And, by replacing phototransistors with photodarlingtons in optocouplers, manufacturers can now produce devices that provide circuit isolation from voltage surges as great as 2500V rms and offer current transfer ratios (CTRs) as high as 1000%.

As a result of these improvements, a new assortment of applications now exists for discrete optoelectronic devices in high-temperature, high-precision, or high-voltage industrial, military, and automotive products. Industrial applications include control systems that sense the location or orientation of objects, safety systems that use a "curtain of light" to prevent human injury, explosion-proof switches, and sensors that determine the flow and level of liquids. The automotive industry uses optoelectronics in solid-state ignitions, tachometers, and load-leveling circuitry.

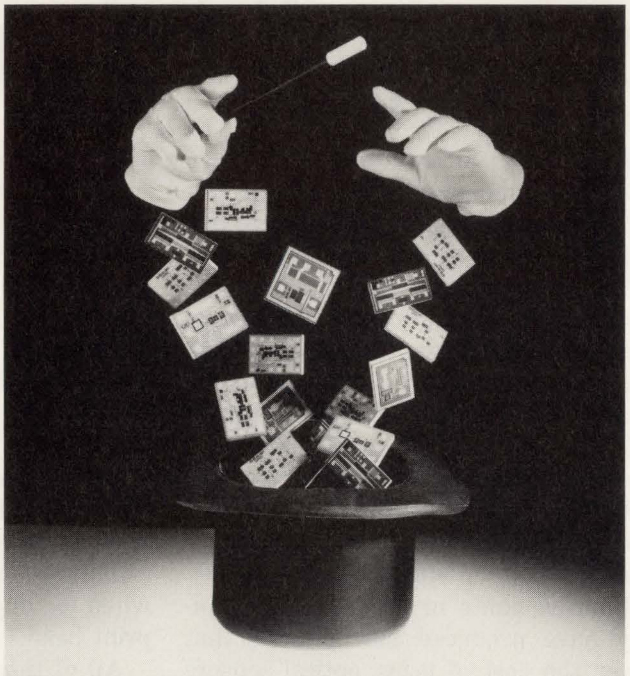
You'll also find optoelectronic components in such consumer items as television remote controls, smoke alarms, intrusion-alert security systems, and an ever-increasing variety of electronic toys. Vending machines have optical sensors to count and identify coins. Computer printers use these devices when feeding paper and positioning the print head.

All of these diverse applications that use discrete optoelectronic components rely upon objects either blocking a beam of light between a photoemitter and a photosensor or objects reflecting a light beam from an emitter to a sensor. Photoemitters are semiconductor light sources based on the principle that when



These hermetically sealed optocouplers *from Hewlett-Packard operate over the full military temperature range, from −55 to +125°C. Select from 8-pin ceramic DIPs or 20-lead ceramic LCCs.*

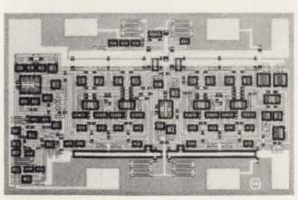
NOW PUT A LITTLE AVANTEK MAGIC IN YOUR SYSTEM



Avantek MagIC™ High Speed ICs Enable Superior System Designs

magIC™

The new MagIC™ series of silicon bipolar MSI integrated circuits offer the best performance available from silicon ICs yet. The broadband, high frequency performance of these high-speed silicon ICs make them cost-effective alternatives to more expensive GaAs ICs. Avantek MagIC silicon ICs are manufactured with Avantek's proprietary 10-15 GHz F_t, 25 GHz F_{max} Isosat™ process for unsurpassed integration and performance at microwave frequencies. Avantek's MagIC series ICs presently consists of four product families: low noise amplifiers, active mixers, variable gain control amplifiers, and prescalers. These low-cost, high-speed silicon ICs are Avantek's magic solutions to your RF, microwave and lightwave system performance and cost problems.



High Performance, High Speed, Low Cost...

The INA-series of two-stage low-noise amplifiers presently consists of three models, offering:

- 3 dB bandwidths to 2.8 GHz
- Gains as high as 32 dB
- Noise figures as low as 1.7 dB
- Prices as low as $22.00 each* in hermetic 70 mil surface mount package

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- RF and LO frequency range of .05 to 5.0 GHz
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*Price for 1000 piece quantities

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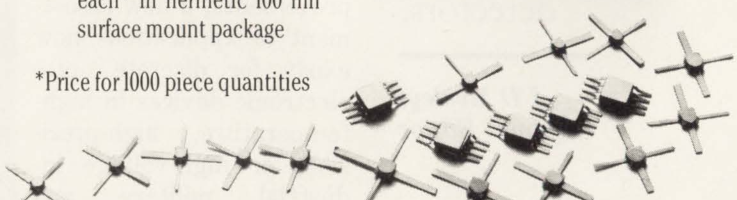


Magic Solutions in Silicon

AVANTEK

CIRCLE NO. 186

Optoelectronic devices

you forward bias a pn-junction diode, it emits light. Thus you have a light-emitting diode, or LED. (See **Table 1** for a comparison of various light sources.)

Though the color and wavelength of the light that an LED produces depend upon the bandgap energy of the semiconductor material used to manufacture the LED, production devices seldom offer wavelengths shorter than 500 nm. LEDs used in electronic applications typically emit invisible light near the infrared region so as to closely match the spectral response of silicon photosensors for maximum signal-transfer efficiency.

Silicon-doped GaAs LEDs emit light wavelengths of approximately 935 nm. Adding aluminum during the manufacturing process drops the spectral emission to around 890 nm, which closely matches the peak spectral-response range of a silicon phototransistor. The final result is a 30% improvement in coupling efficiency with AlGaAs LEDs.

Aluminum also reduces the reabsorption and the internal reflection of photons by the LED, resulting in improved surface emission. Furthermore, an AlGaAs LED can produce the same photon output using half the current required by a GaAs LED. This feature makes AlGaAs LEDs suitable for battery-operated applications. And driving the LED with less current will extend its operating life.

Hewlett-Packard Corp uses a transparent substrate AlGaAs proc-

Table 1—Representative manufacturers of LEDs, laser diodes (LD), and infrared emitters (IRED)

Manufacturer	Model	Type	Peak wavelength (nm)	Output power	Price	Features
AND	AND177RAG	LED	Red=660 Green=567	Red=900 mcd Green=150 mcd	$0.98 (1000)	Dual-color LED with common cathode
	AND190CRP	LED	660	125 mW	$2.61 (1000)	13,000 mcd at 20 mA; 4-degree radiation pattern
EG&G Vactec	VTE 1291	IRED	880	170 mW	$1.10 (1000)	Stable emission power over extended use
Electrophysics	IRE160	LED	880	100 mW	$16.25 (1)	
Hamamatsu	L3302	LED	850	1.5 mW	$275 (1)	Super luminescent, low coherent noise, optimal for optical gyroscopes
	L2376	LD	905	10 W	$137 (1)	High-speed response, high output power, high repetition rate
Harris	F5G1	IRED	880	100 mW	$0.75 (1000)	GaAlAs device
HEI	107-10	LED	940	75 mW	$4.15 (1000)	Available with transistor, Darlington amplifier, or Schmitt-trigger outputs
Hewlett-Packard	HLMP-8150	LED	645	176 mW	$10 (1000)	TS-AlGaAs technology, brightest LED Lamp available
Hitachi America Ltd	HL6711G	LD	670	5 mW	$55 (1)	Bright red beam
KCK America	CRS-10	LED	Red=630 Yellow=585 Green=565	55 to 70 mA	$90 per 1000 (100,000)	Surface-mount package (1210 size); bicolor combinations available
Laser Diode	SRD1300 SRD8300	LD LD	1270 to 1330 800 to 850	1 mW 1 mW	$4000 (1) $3000 (1)	High coupled output for fiber-optic gyroscopes Short 50-μm coherence length for fiber-optic gyroscopes
Marktech International	MT1018-BL	LED	470	160 mW	$15 (1)	Blue LED, silicon carbide die for increased brightness and reliability
	MTE108CL	IRED	890	180 mW	$6.40 (1)	TTL I/O for digital transmissions, plastic lens cover gives uniform light
Micro Switch	SEP8505	IRED	930	25 mW	$0.45 (10,000)	Transfer-molded T1 eliminates mold-parting line in optical area
Motorola Semiconductor	MLED71 MLED930	IRED IRED	940 900	90 mW 250 mW	$0.34 (1000) $0.78 (1000)	Molded lens; clear epoxy package GaAs; low 10-mA drive current
Optek Technology	OP224	IRED	890	150 mW	$1.04 (1000)	Small, hermetic package for high-density mounting
Philips Components	CQL80/D	LED	675	5 mW	$48 for 5000	Easily visible red light
Siemens Opto-electronics	L(X)K 382	LED	Red=635 Yellow=586 Green=565	300 mW	$0.60 to $0.64 (5k)	Also available in orange and deep green; provides diffuse, uniform light
Texas Instruments	TIL23	LED	940	100 mW	$1.45 (100)	Small-size permits matrix assembly in printed-circuit boards
Three-Five Systems	TEMT880	IRED	880	240 mW	$0.65 (100)	5 mm plastic package; high power output; silicon phototransistors

ess to produce LEDs that the company claims are the brightest available. Its HLMP-8150 has a viewing angle of 4°, a typical luminous intensity of 15,000 millicandela (mcd), and a minimum luminous intensity of 8000 mcd. A comparable GaAs LED is 12 to 15 times less bright, according to HP. Yet not every manufacturer believes that aluminum is a necessary ingredient for LEDs—Motorola has just developed a proprietary GaAs process that the company claims will minimize output-power degradation over time.

Another type of LED is the laser diode. Its physical dimensions and optical properties create a highly directional and nearly monochromatic beam of photons that makes this device well suited for applications involving precise alignment, fiber optics, and interferometry (the measurement of wavelengths, wave velocities, distances, and directions).

To convert the light emissions from any LED into electrical signals, an optoelectronic detector, such as a photodiode, phototransistor, or photodarlington, will absorb the incident photons and produce a proportional current flow. **Table 2** lists a representative sample of photoreceptors.

Photodiodes use a reverse-biased pn-junction and produce response times in the submicrosecond range. And as long as a photodiode doesn't exceed its avalanche voltage, it behaves as a constant current generator. Because the spectral response of a photodiode relates to the semiconductor material it is made of and the depth of its pn-junction, a manufacturer can match the sensor to a specific wavelength of light.

Phototransistors give you added sensitivity control by letting you apply a biasing voltage to the transistor's base. However, under low illumination, a phototransistor may exhibit a leakage current at its collector-base junction. This leakage is called dark current, and to minimize its effects you must plan your circuit so that nothing will cause the transistor's base-collector junction to become reverse biased. Lowering ambient temperature also reduces dark-current effects.

Available in five colors, *the Super Argus series of LEDs from Siemens emits 10 times as many photons as the manufacturer's standard LED series.*

Photodarlingtons use two cascaded transistors to amplify the sensor's output signal and provide higher gain for low-level light detection. However, because a photodarlington contains two transistors, this device is slower than a similar phototransistor and the effects of dark current will likewise be comparably worse.

When using a photoemitter and a photosensor to detect the presence or position of an object, you can arrange for the item to pass be-

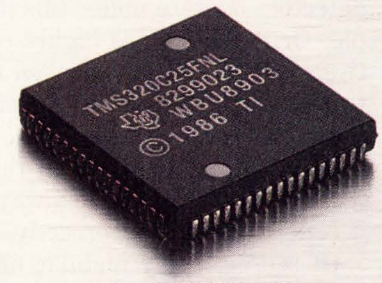
Table 2—Representative manufacturers of photodiodes (PD), phototransistors (PT), and infrared sensors (IS)

Manufacturer	Model	Type	Temperature range (°C)	Price	Features
EG&G Vactec	VTH2090	PD	−20 to 60	$43 (1)	10 mm × 10 mm detecting area
Electrophysics	7215	IS	−20 to 50	$1045 (1)	Imaging viewer makes IR sources visible for alignment and trouble-shooting
Hamamatsu	S1337	PD	−20 to 60	$30 (1)	UV to IR spectral response, high precision, large active areas
Harris	L14F1	PT	−55 to 150	$1.50 (1000)	Photodarlington device mounted in T018-type hermetic package
Hitachi America Ltd	HR8101	PD	−40 to 80	$7.35 (1)	Detects light wavelengths from 600 to 900 nm
Micro Switch	SDP8600	IS	0 to 100	$0.88 (10,000)	Integral voltage regulator, Schmitt Trigger logic output
Motorola Semiconductor	MRD701 MRD821	PT PD	−30 to 70 −40 to 100	$0.28 (1000) $0.62 (1000)	Low cost, miniature plastic package Infrared filter rejects visible light
Optek Technology	OP600A OPL800	PT IS	−65 to 125 −55 to 110	$0.87 (1000) $2.14 (1000)	Can mount on a printed-circuit board Includes a photo diode, linear amplifier, and a Schmitt Trigger on chip
Philips Components	CPF30	PD	−20 to 80	$55 for 1000	Planar technology
Three-Five Systems	TDET600	PT	−25 to 85	$0.50 (100)	T1 plastic package, spectral match for GaAs & GaAlAs emitters

Given enough time, the TMS320C25 can do almost everything the ADSP-2100 can.

The ADSP-2100.

- The ADSP-2100 computes a 1024-point complex FFT in less than 3 ms with a total memory requirement of less than 4k bytes. It also computes a 2 × 2 2D convolution in 1.2 μs and executes ADPCM in only 68 μs.
- The ADSP-2100 can access two words of external data every cycle.
- The ADSP-2100 supports zero-overhead loops of any length. So our looped code – which is the easiest to write – is also the fastest.
- The ADSP-2100's two dedicated data address generators can auto-increment/decrement by any offset value, and they have automatic circular buffer wraparound.
- The ADSP-2100 Assembler supports the easiest language in the business. So you code a multiplication/accumulation the same way you'd write the original algorithm. For example, the algebraic R = R + X*Y codes as MR = MR + MX0*MY0.



The TMS320C25.

- The TMS320C25 takes more than three times as long to compute the same size FFT, while it devours over 47k bytes of memory.[1]
- The TMS320C25 is limited to one access of external data every two cycles.
- The only zero-overhead loop the TMS320C25 can execute is one instruction repeated no more than 256 times.
- Circular buffers? The TMS320C25 doesn't support them.
- The TMS320C25 is programmed with 133 mnemonics like SPAC, BGEZ, MACD, XORX, and SBRK. A multiplication/accumulation is coded as MACD >FF03,*–. While this might not scare the XORX out of you, it's not the easiest thing to debug or maintain.

We're not saying the TMS320C25 is slow. But even if it were twice as efficient as it is now, it'd still be a lot slower at DSP than the ADSP-2100. The fact is, the ADSP-2100 is out in front of the TMS320C25 in performance, readability of code, and development tools.

Just how far out front? Get our free technical booklet and read about it. Or better yet, get an ADSP-2100 sample kit for only $49.95 and see for yourself. To request either, call DSP Marketing at 1-617-461-3771.

ANALOG DEVICES

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[1] EDN, "EDN's DSP Benchmarks," September 29, 1988.

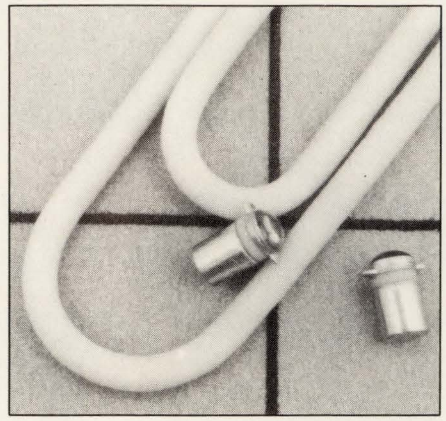
tween the optoelectronic pair and break a beam of light between them. Intrusion alarms and smoke detectors operate under this principle. Or if the item is highly reflective, such as a gear's polished metal teeth, you can bounce the photon beam off the object. The sensor will only receive a signal when the object is positioned in such a way that it reflects the beam correctly.

Of course, shiny metallic objects aren't the only things that reflect light. You may want to consider using an optoelectronic pair to determine fluid level in a reservoir. By bouncing the emitter's light beam off the surface of the liquid to reflect the beam back to a detector, your circuit can monitor the fluid's dissipation without contaminating the liquid or the sensor.

Another type of optoelectronic device is the optically coupled isolator, commonly referred to as either an optocoupler or an optoisolator (**Table 3**). This component provides electrically isolated signal transference by permitting an input signal to energize the device's internal infrared LED and passing the signal via photons to an internal photosensor, which in turn creates an output signal. In this way, optocouplers can protect low-current and low-voltage logic circuits (or human beings) from high-power lines, such as the 120V ac found in homes. Or you can use an optocoupler to prevent noise from traveling from one circuit to another, eliminating the need for a common ground when linking the two.

Again, using photodarlingtons instead of phototransistors provides CTRs as high as 1000% and circuit isolation from voltage surges as great as 2500V rms. Such isolation was previously provided by mechanical devices such as relays and isolation transformers. Mechanical relays generally provide better circuit isolation than optocouplers can offer. However, unlike relays, optocouplers have no moving parts, faster switching speeds, and longer operating life.

The optocoupler's small size, low cost, and solid-state construction make it useful in telephone switching equipment, industrial motors, and process-control solenoids. You can also use optocouplers as an interface between different families of digital logic circuits.



You can select from three sensitivity levels *when you design with these tiny NPN silicon phototransistors from Optek.*

For example, an H11K2 coupler in a surface-mountable 6-lead package from Harris Semiconductor costs $1.13 (1000) and has a 20-µsec typ turn-on time and 40-µsec turn-

Table 3—Representative manufacturers of optocouplers (OC), optical switches (OS), and interrupter/reflector modules (IRM)

Manufacturer	Model	Type	Temperature range (°C)	Price	Features
C&K/Unimax	LS	OS	–25 to 65	$1.75 (500)	External, adjustable slide tab reverses output logic level
EG&G Vactec	VTR24F1	IRM	–40 to 85	$3.20 (1000)	Detects diffuse and low-reflectance surfaces
Hamamatsu	S3599	OS	–25 to 60	$8 (1)	Background rejection of up to 10,000 lux; synchronous detection on IC
Harris	H11K1	OC	–55 to 100	$1.98 (1000)	Bidirectional dc and ac switching with single-polarity control signal
HEI	105-36	OS	0 to 70	$22.36 (1000)	Dual Schmitt-trigger output
Hewlett-Packard	HPCL-55XX	OC	–55 to 125	From $29	Hermetically sealed; dual-channel; ceramic LCC packaging
Marktech International	MTPC26010	OC	0 to 70	$3.40 (1)	Internal Faraday shield reduces effects of capacitive coupling
Micro Switch	HOA0902	OS	0 to 85	$4.34 (10,000)	Integrated quadrature logic controls speed and direction of output
Motorola Semiconductor	MC104 MOC70W1	OC OS	–55 to 100 –40 to 85	$0.74 (1000) $2.55 (1000)	25.3-mA (max) output collector current Dual-channel interrupters sense direction of motion
Optek Technology	HCC240	OC	–55 to 125	$9.36 (1000)	Surface mountable
Siemens Optoelectronics	6N135	OC	–55 to 100	$1.04 (1000)	Operates at 1M bps; TTL compatible; 2-MHz bandwidth
Texas Instruments	TIL193	OC	–40 to 85	$1.87 (100)	Four-channel devices in 8-pin DIP

The ADSP-2101

- The ADSP-2101 builds on the ADSP-2100 architecture, so it's upwardly code compatible. You can quickly port ADSP-2100 code to the ADSP-2101. Or use our C Compiler for a fast start.
- The on-chip memory of the ADSP-2101 integrates 64k bits of the fastest SRAM available today with an architecture designed for signal processing. This allows the processor to fetch two operands and the next instruction on every cycle for sustained performance.
- The ADSP-2101 has two full duplex serial ports, hardware companding, timer, low-power IDLE instruction, full-speed in-circuit emulator, and more.

And now with our ADSP-2101, there's just no comparison.

We're not saying all other DSP processors are slow and inefficient. But the ADSP-2101 is already enabling hundreds of DSP engineers around the world to create their next generation products. The fact is, our DSP processor family is out in front in performance, readability of source code, and development tools.

Get the facts on the ADSP-2101 by sending in the reply card. Or better yet, call DSP Marketing at 1-617-461-3771 and request a sample today.

ANALOG DEVICES

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Optoelectronic devices

off time for rapid switching. The maximum leakage current for this device is 200 nA, but it can carry as much as 150 mA rms ac and has a minimum breakdown voltage specification of 250V. Voltage isolation peaks at 3535V for surges and 3180V under steady-state conditions. The back-to-back photodarlingtons used in this component make it immune to the high levels of commutating dV/dt often encountered in the power-line-switching applications it suits. Commutating dV/dt is a phenomenon that causes a current spike, which turns a device on every time you try to turn it off.

Like the advances in semiconductor technology, evolving package styles have also resulted in device improvements. Plastic packages are not only less expensive than metal cans but may also provide functional improvements.

According to Optek, a typical plastic LED has approximately 40% more output power than a comparable metal-encased device. This difference is due in part to the metal case absorbing some of the device's photons and its two-sided glass lens reflecting some photons back into the device. In contrast, a plastic LED uses its surface as both a casing and a lens, so few photons become trapped within.

In general, plastic optoelectronic devices have larger, more thermally conductive leads than their metal counterparts. Plastic components typically have 0.020×0.020-in. copper-silver leads. Metal devices frequently contain leads that measure 0.017-in. in diameter and are composed of a nickel-iron alloy. As a result, plastic-enclosed devices offer a thermal path that is approximately 40% better, producing com-

For more information . . .

For more information on the optoelectronic devices discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you read about their products in EDN.

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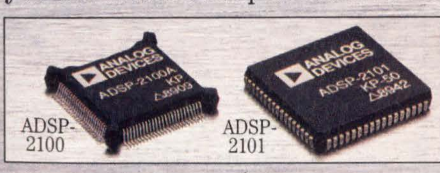

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ANALOG DEVICES

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UPDATE

Optoelectronic devices

parably higher power dissipation ratings.

However, metal cases still maintain an edge over plastic equivalents with respect to operating temperature. Metal parts typically have temperature specifications ranging from −55 to +150°C; plastic cases seldom offer specs permitting temperatures in excess of +100°C. Yet, new plastics that endure temperatures reaching 130°C are emerging and may soon nullify this advantage of metal-cased devices.

Keep track of the players

In addition to all these changes in optoelectronic technology, the industry itself has experienced a great deal of flux. In 1988, Optek Technology bought TRW's optoelectronic division. Optek jumped from $12.9 million in total assets to more than $48 million, making it one of the industry's leading manufacturers of photoelectronic devices and semiconductor chips.

General Instrument Corp, another major manufacturer of optoelectronics, has changed its name to Quality Technologies. General Electric's Solid State division became a *semiconductor sector* within Harris Corp. Clairex Electronics of Mount Vernon, NY and Electro Corp of Sarasota, FL are now Senisys in Plano, TX. However, history shows that consolidation and shakeout are part of the normal maturation process within the semiconductor industry. These changes typically result in financially stronger companies that focus on advancing the current state of technology, which may in the end benefit the user. EDN

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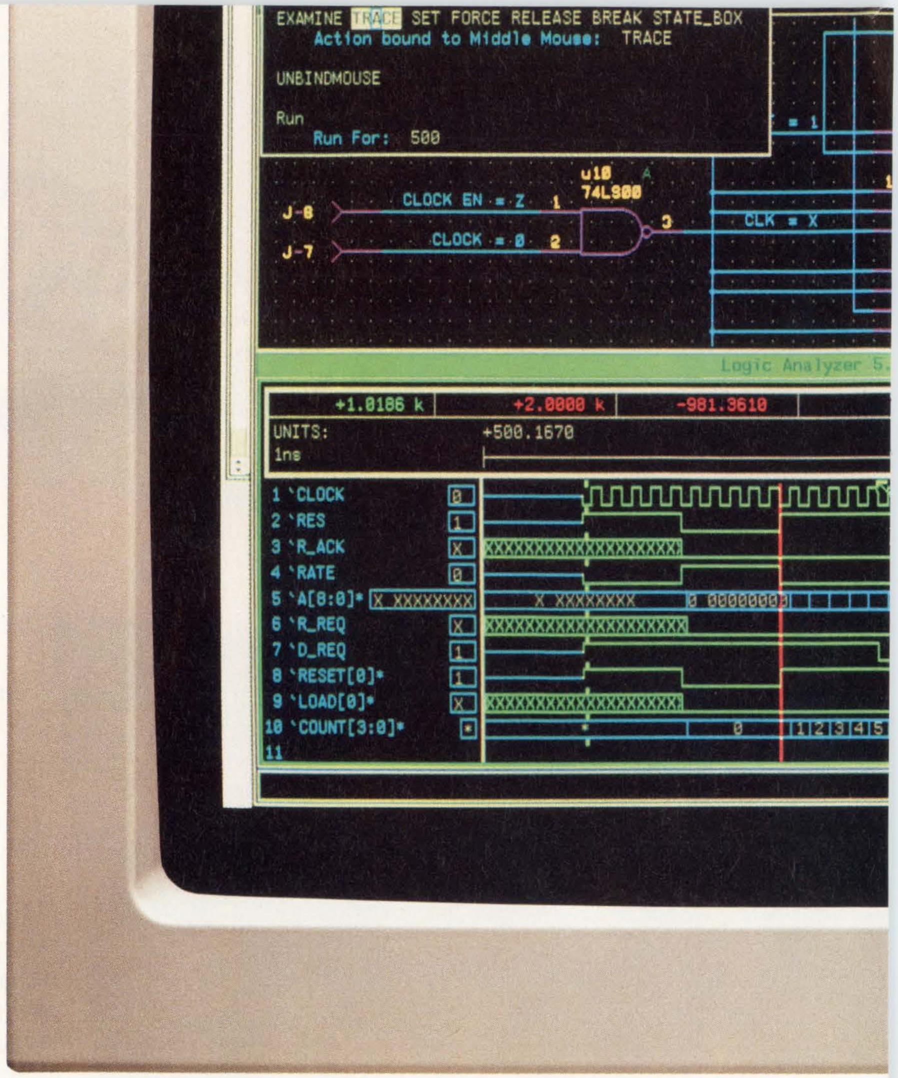

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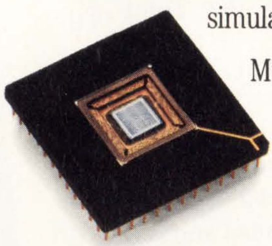

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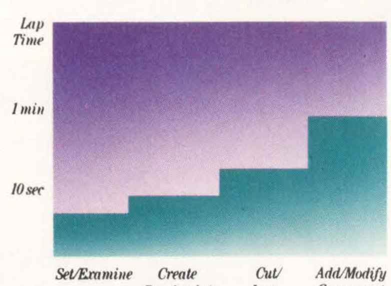

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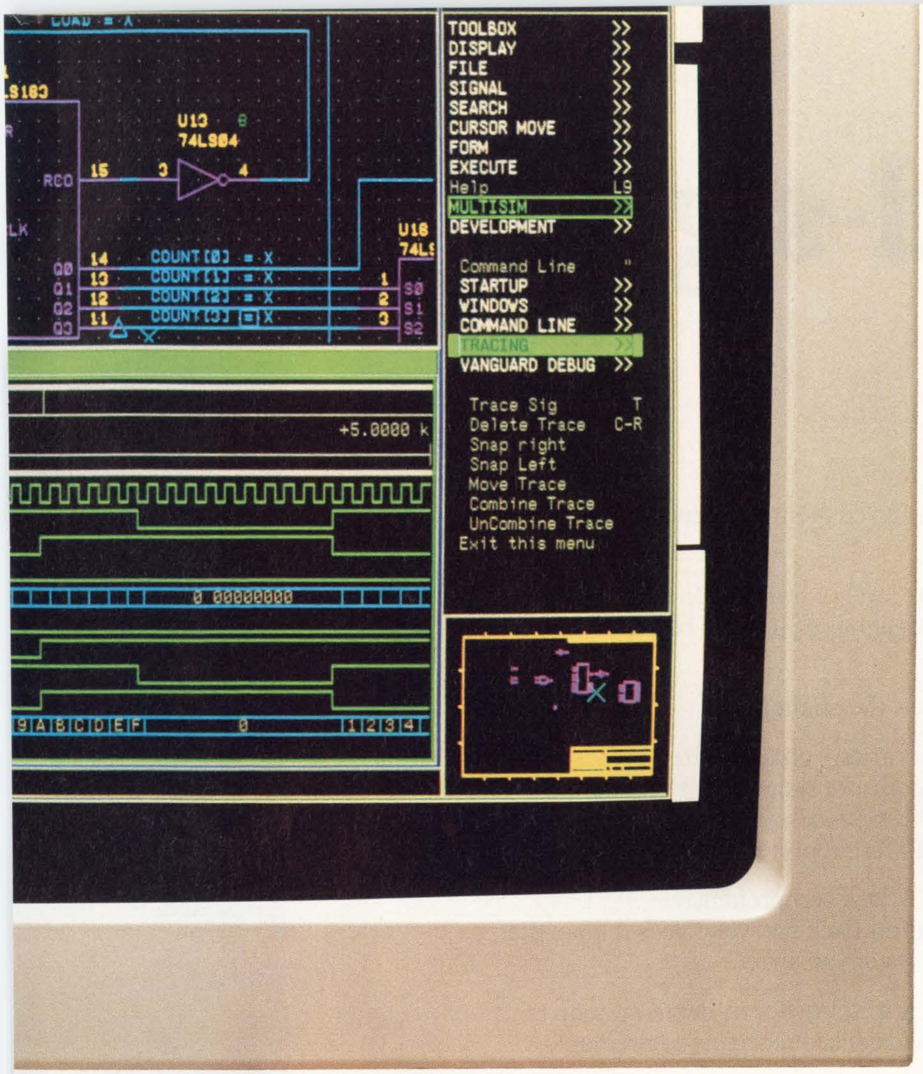

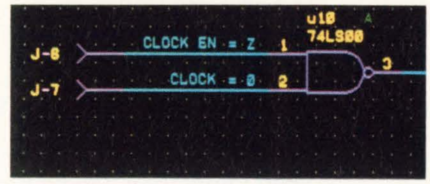

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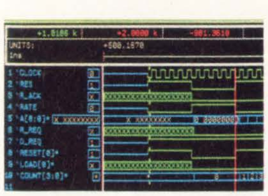

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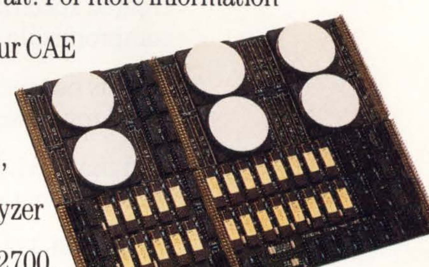

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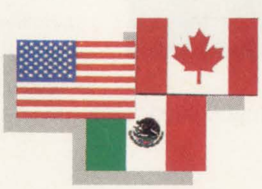

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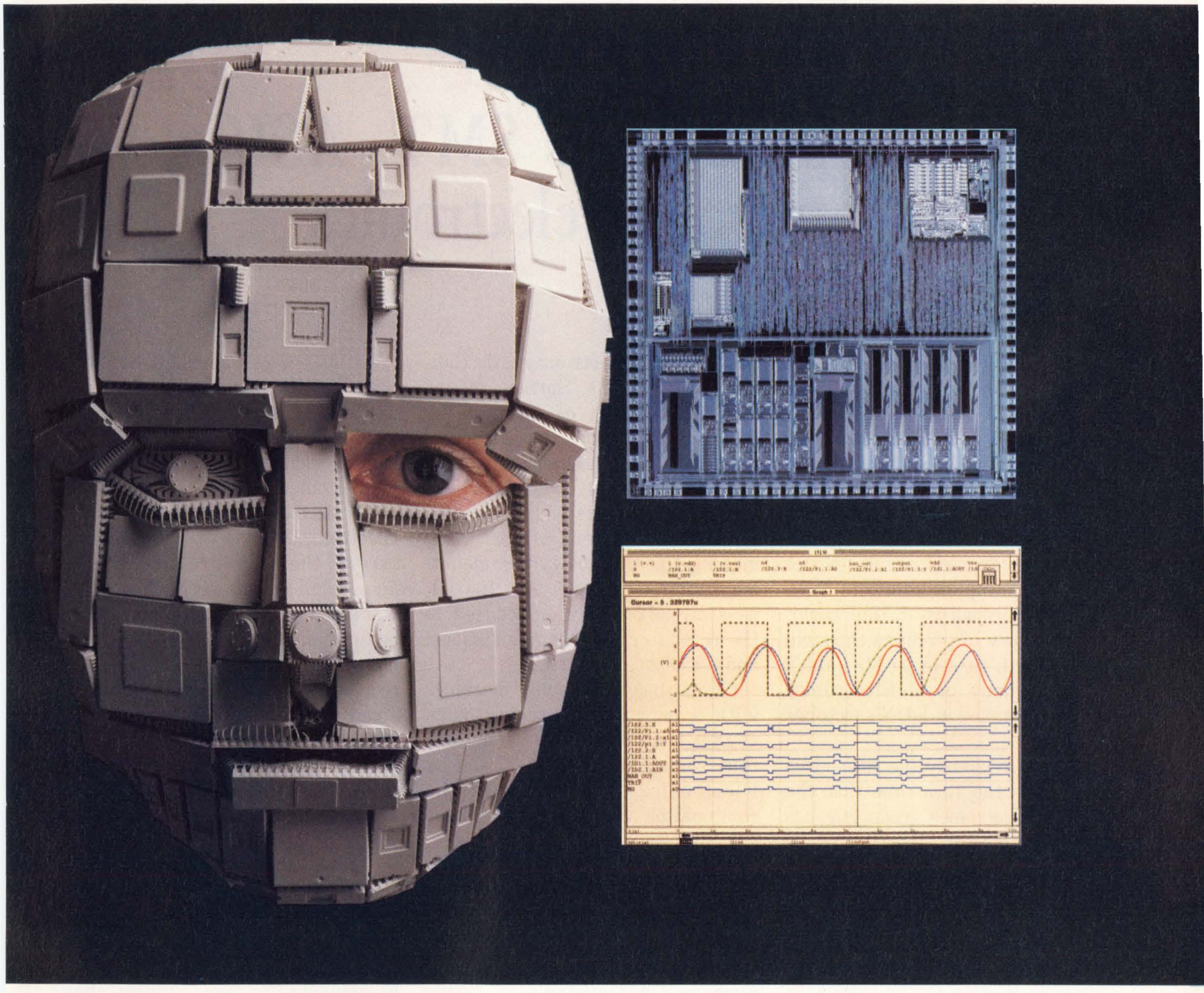

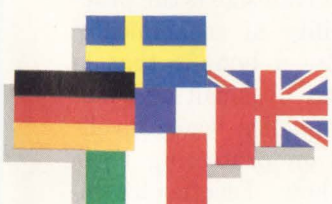

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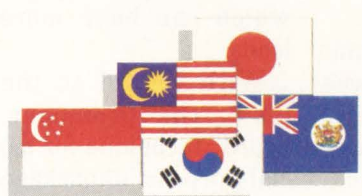

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SHOW PREVIEW

Electronica to stress SMT, ASICs, power electronics

Raymond Boult

For professionals in the fields of electronics components and assemblies, the place to be this fall is the Munich, Germany, Trade Fair Center. That's where the Electronica 90 show will be held on November 6 through 10. The organizers say the exposition will feature a diverse group of products from manufacturers all over the world. For a preview of products that will be exhibited, turn to pg 118.(You'll also find many more Electronica products detailed in EDN's October 25 issue.)

As was previously the case—this year marks the 13th time that the biennial Electronica trade fair has been held—the exhibition divides the products into three groups: electronic components in Section A, electromechanical components and subsystems in Section B, and equipment for development and quality control in Section C. The **chart** on pg 114 details where in the Trade Fair Center you can find the products that interest you the most.

What's the gist?

Several major themes will dominate the sessions and conferences at the show, including surface-mount devices (SMDs) and surface-mount technology (SMT); application-specific integrated circuits (ASICs); and electromagnetic compatibility (EMC). Surface mount will receive a lot of attention for some pretty obvious reasons. Forecasts from many electronics companies indicate that 50% of all electronics components will be suitable for SMT by the end of next year, making the technology the mounting technique of the '90s. Indeed, it is already firmly entrenched in the computer, telecommunications, and aerospace industries.

Circuit-board-assembly machines with a capacity of placing some 40,000 components per hour are thus something to look out for at Electronica 90. Moreover, the combination of SMT and multilayering can result in an 80% reduction in pc-board surface area, another advantage for miniaturization-conscious users. For SMT's potential to be fully realized, however, corresponding developments must take place in CAD systems to enable quick and easy design of circuit boards. This need is highlighted by the complexity of the latest ICs, the fine-pitch packaged versions of which can have more than 400 leads.

With regard to the future of SMT, the promising "chip-on-board" technique for mounting special-purpose unpackaged semiconductors makes use of either the "chip-and-wire" method or "flip chips" with built-in solder globules on the chip surface. Straws in the wind also indicate that new basic materials may soon be developed, which could revolutionize SMT.

As far as ASICs are concerned, Electronica 90 will give novices and experts the chance to update their knowledge of this technology. You will learn how complex projects can be implemented quickly and economically, notably by means of direct laser writing onto the chip instead of using costly masks. Dataquest, a market-research company, expects the European ASIC market to be worth $1.7 billion by 1993, double the 1987 figure; the value of ASICs incorporated into terminal devices in Germany alone by 1993 will amount to $400 million. ASICs' main technical advantage is, of course, that the complex functions of an entire pc board can be implemented on one compact chip, resulting in reduced transmission lengths and times when compared with discrete-component solutions. An additional advantage is the practical impossibility of economically copying ASICs—a benefit that is highly regarded by small and medium-sized companies whose livelihood depends on protecting their system know-how. Electronica 90 will give coverage to a specific type

Munich, Germany—site of Electronica 90.

of ASIC—programmable logic devices (PLDs).

The show will also feature practical solutions to problems involving electromagnetic compatibility (EMC) in microelectronic devices used in the aerospace, military, computer, telecommunications, industrial, medical, and automotive sectors. A British study predicts that the European market for products and services to control electromagnetic interference (EMI) will quadruple within the next 5 years to reach $800 million by 1994. Germany is expected to be the largest consumer (37%), followed by the UK (31%). These products include filters, suppressors, shielded enclosures, conductive coatings and sealing materials, test and calibration equipment, and special plug connectors. A variety of products related to EMI and sessions covering EMC will be featured at the trade fair.

Also slated for innumerable exhibitions and detailed coverage at Electronica will be passive components, power electronics, and analog ICs. The importance of passive components, including resistors, capacitors, coils, and their associated ferrite cores, is somewhat obscured by the current worldwide emphasis on the development of key active components, such as microprocessors and memory chips. Nevertheless, the passive-component market of about $20 billion is increasing at about 3% per year. Applications are primarily in the industrial (29.2%), telecommunications (20.9%), and consumer and automotive (16.2% each) sectors.

Although it's nonsense to speak of more powerful passive components, the requirements of increased miniaturization and economical positioning methods look set to influence at least the physical form of these devices. For instance, the relatively new insert mount technology, originally developed for the mobile-communications market, allows even higher component densities than SMT. Recent developments include 2.2-mm-long cylindrical resistors with a 1.1-mm diameter, which can be mounted and soldered vertically in pc-board holes.

In the field of power electronics, you'll be able to see components and ICs, such as triacs, thyristors, rectifiers, power transistors, and driver circuits. These devices are established in industrial automation and process control, as well as in the automotive and computer industries. Smart-power ICs combine power components with analog and logic functions (several hundred gates), and serve as links between microprocessors and medium-power (10W to 3 kW) electrical loads, such as lamps, motors, and power packs. These ICs can detect faulty switching, high and low voltages, short circuits, overloads, and overheating and can disconnect modules for safety reasons. Soon-to-be-introduced power modules, with software-configurable output stages, should increase the flexibility of these essentially application-specific devices.

Digital vs analog

Although the electronics industry as a whole is justifiably preoccupied with digital techniques, analog technology allows recording engineering variables, such as pressure, temperature, voltage, and current, and preparing their values for subsequent digital processing. Electronica 90 will provide visitors with the latest information on analog devices, including A/D converters (ADCs) and D/A converters (DACs), operational amplifiers, comparators, voltage/frequency and frequency/voltage converters, filters, and multiplexers.

Increases in complexity, speed, accuracy, and power efficiency are the trends that govern the development of analog components. The increased complexity of ADCs and DACs, for example, lets you integrate more and more functions, such as automatic self-compensation circuits or sample-and-hold amplifiers, on one chip. Meanwhile, programmable resolution and gain make the components themselves more user friendly. Furthermore, many DACs now feature first-in/first-out (FIFO) memories with associated control logic, as well as digital signal processor (DSP) interfaces.

In the case of op amps, the trend toward less complex, more user-friendly circuit designs is overshadowed by the need for higher accuracy, which implies better offset and drift characteristics. Nevertheless, analog components cannot escape the trend toward the integration of complex functions onto a single ASIC chip. Indeed, many semiconductor manufacturers already offer analog functions such as library elements and function blocks, which can be designed into complex ICs using an appropriate computerized workstation. A workstation also allows simulation of analog functions before the chip actually goes into production. There is, however, an economic limit to the integration of different technologies on a single chip, ensuring the availability of a range of analog ICs for the foreseeable future.

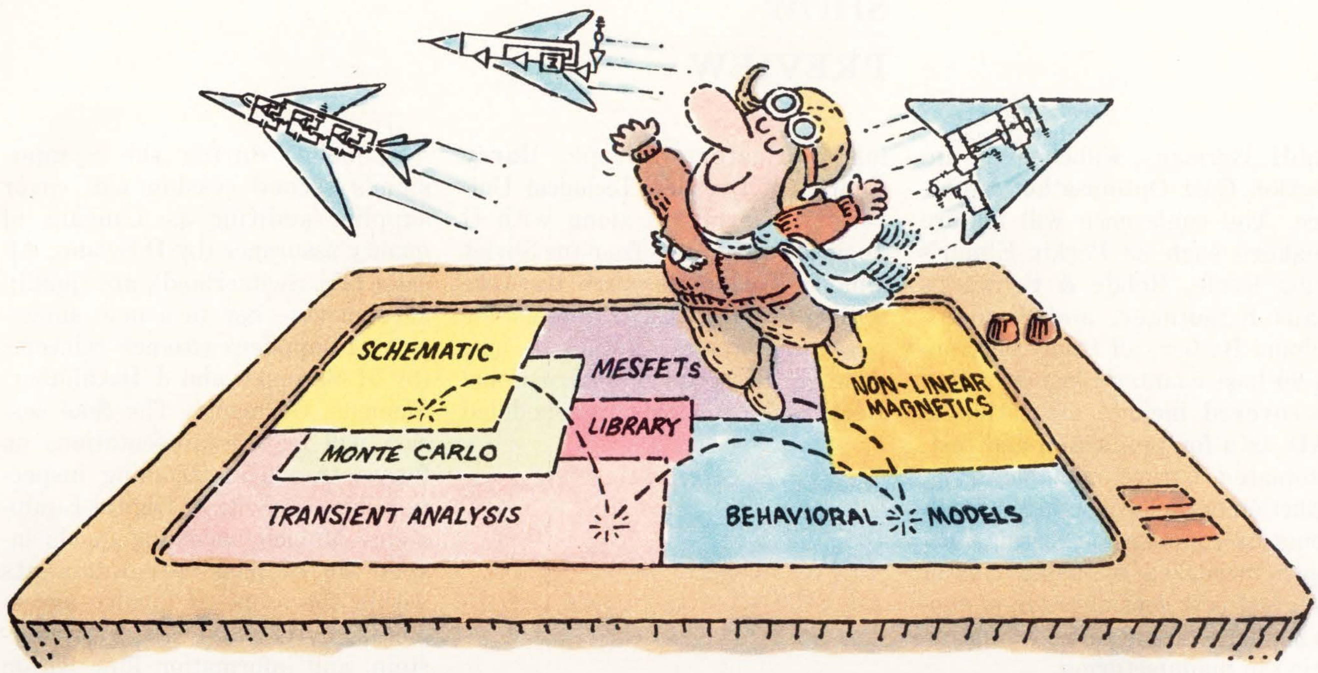
Along with the vast number of products on display, Electronica 90 will feature a program of sessions on a variety of topics of interest to electronics professionals. On Tuesday, November 6, you can attend the Installation and Connection Engineering and Inspection Cost Optimization conferences. Scheduled for Wednesday, November 7, are the International Power Electronics Congress, and the Microelectronic Sensors and Product Liability Conferences. And on November 8, the Quality Assurance Symposium and the Microsystems Engineering and Electromagnetic Compatibility conferences are scheduled. All conference speeches will be simultaneously translated into English or German, as appropriate.

Electronica 90, November 6–10, 1990

Section A	Section B	Section C
Electronic components	**Electromechanical components**	**Development and quality-assurance equipment**
Microelectronics Small-signal semiconductors Power electronics Optoelectronics PC-board systems Tubes Passive components Power supplies Electrical protection	Microwave technology Switches, keys Buttons, relays Interfacing elements Plug connectors Unloaded circuit boards Display and recording devices Sensor systems Regulating units Control systems	Measured data acquisition Sensor technology Measured data adaptation and transmission Data display Inspection and monitoring equipment for components and assemblies Laboratory and test-bay equipment Equipment for circuit and system design Information media and services
Halls 18, part of 19, and 21–25	**Halls 1–16**	**Halls 19 and 20**

Chaired by Professor E Schäfer of Aachen University, Germany, the Installation and Connection Engineering conference will focus on problems and solutions related to the further miniaturization of plug connections. Keynote speakers include Paul Gazzara of Thomas and Betts International, UK ("Future developments for grids below 2.54 mm"), Harald Jürschik of EPT, Germany ("Aspects of press-fit technology"), and Franz Leitl of S-Team Elektronik GmbH, Germany ("Transmission problems in connection systems of the future").

Dr Hans Otto Haller, of EVP



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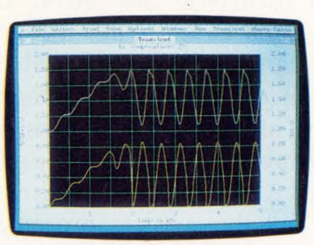
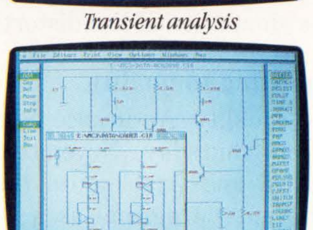


Transient analysis



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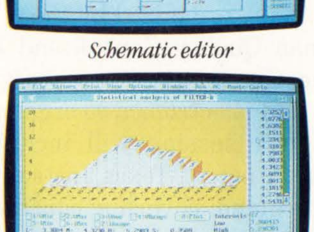

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spectrum

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GmbH, Germany, will chair the Inspection Cost Optimization conference. The conference will feature speakers such as Perkin-Elmer's Klaus Kerle, Rohde & Schwarz's Klaus Kundinger, and Siemens' Helmut Heiber, all from Electronica 90 host country Germany. Topics covered include utilization of CAD data for production and test, automated fixture manufacturing, reduction of time-consuming adjustments by combination testing, test depth increased by using cluster test, test cost consideration of digital simulation, and test cost optimization in manufacturing.

A truly international line-up

The second day of the Electronica 90 related-events program will feature the 5th International Power Electronics Congress. The Congress is divided into four sessions. Chaired by Mutsuo Nakaoka (Japan), Session 1 will cover integrated power semiconductors. A keynote speaker, Craig Varga of Siliconix Inc (USA), will present the simplified design of low-power universal input power supplies. That discussion will be accompanied by an overview of the automotive applications of intelligent power switches, presented by Ulrich Haase and Thomas Storck of Philips Components, Hamburg.

Session 2 will delve into power switching transistors. One of the highlights of Session 2 will be the presentation of "New IGBT (insulated gate bipolar transistor) modules with improved power loss in high-frequency PWM mode," by a group from Fuji Electric Co (Japan). That discussion will be followed by a European view of IGBTs in the presentation entitled "IGBT or bipolar transistor—facts on the application," by engineers from Siemens (Germany).

During Session 3 on thyristors, rectifier diodes, and capacitors, the spotlight will fall on newly "deregulated" Eastern Europe. Harry Conrad of Dresden Technical University (Germany) along with G Toomsoo and others from the Soviet Union's Tallinn Research Institute will cover fast GaAs diodes for power electronics. Not to be outdone, B Passerini of International Rectifier Corp (Italy) is scheduled to tell Congress attendees about new development trends with fast power rectifiers. To close Session 3, W Schnabel, of the Germany-based Siemens Matsushita Components Corp, will give the low-down on aluminum electrolytic capacitors for power electronics.

Three sessions on quality assurance will discuss the topic from the manufacturer and customer point of view.

Finally, new circuit concepts and line distortions will be focal points for a futuristic Session 4. Hong Zhang and Brian Mullhall from the UK's Surrey University will cover reversible rectifiers and integrated control of induction machines. Richard Probst of Germany's Spitzenberger & Spies GmbH will close a very full day with a presentation on the simulation of line distortions.

Committing to quality

The Quality Assurance Symposium on Thursday, November 8—the third and final day of the related-events program—is a 3-session affair, organized by the official German Quality Control and Electronic Components trade associations and Electronica 90 organizers. The first session will include H Schwerdtner of Texas Instruments Deutschland covering contractual quality assurance from the semiconductor manufacturer, and R Lünstedt of Hans Kolbe & Co detailing reliability requirements from the customer's point of view.

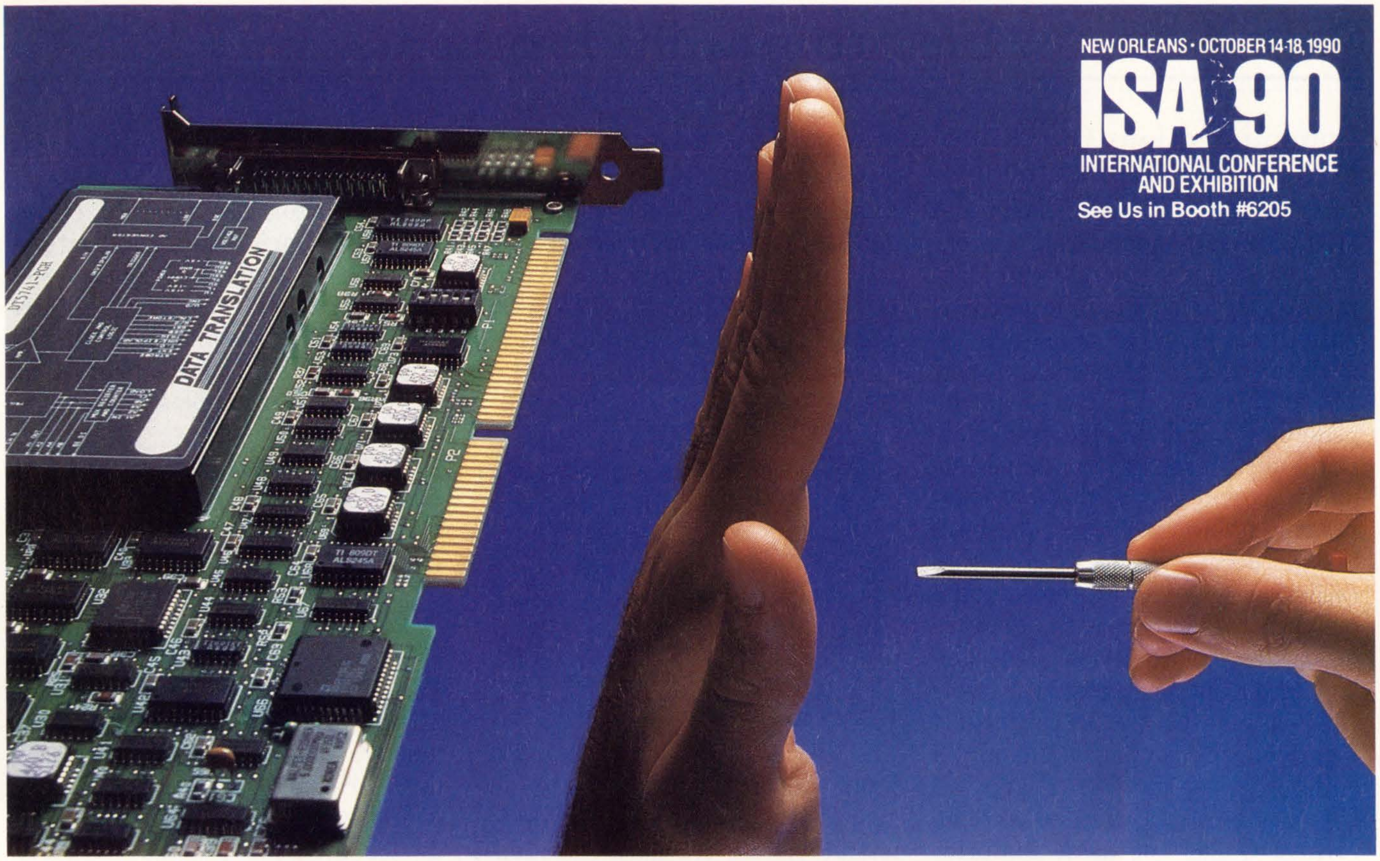
Speeches during the Symposium's second session will cover supplier auditing as a means of quality assurance (by D Swann, Alcatel ITS, Switzerland), and quality agreements—key to a new dimension of supplier/customer relations (by H Sarembe and J Bachhuber, Siemens, Germany). The final session will feature presentations on future trends in incoming inspection, by H-J Seitz of Digital Equipment, Munich; incoming goods inspection of passive components within the scope of quality agreements, by G Süssbrich of Roederstein; and information flow within a company and its influence on logistics quality, by H-U Rasche of Philips, Germany.

Also on the third day will be a conference on microsystems engineering that will cover intelligent sensor systems and installation and connection engineering. The electromagnetic-compatibility conference will go over commercial EMC regulations for Europe 92 and electronics in vehicles: requirements, procedures, and measuring techniques.

As for products on display at Electronica 90, Europe's "big three" electronics manufacturers—Siemens (Germany), SGS-Thomson (France-Italy), and Philips (The Netherlands)—will be present in force. These companies will exhibit many different products, including a new 16M-bit dynamic RAM and a new high-speed serial communications controller. Turn to pg 118 for a review of these and other products. EDN

Raymond Boult is an independent journalist based in Paris, France.

Article Interest Quotient
(Circle One)
High 515 Medium 516 Low 517



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—Fred Molinari, President

GLOBAL LAB™ *Data Acquisition* software with "Hands-Off" control for the DT2831 Series.

Put down that screwdriver! GLOBAL LAB™ *Data Acquisition* software fully supports the DT2831 Series "Hands-Off" design, so setup, installation, calibration, and maintenance are 100% mouse/menu-driven.

Once you've installed your DT2831 Series board, you can forget it. With GLOBAL LAB,™ all DT2831 operating parameters are controlled via software menus. No manual adjustments—no jumpers, no pots, no hassles! You get greater reliability, improved productivity.

In addition to supporting "Hands-Off" control, GLOBAL LAB™ provides numerous data acquisition, signal processing, and display functions. For advanced signal processing, ask us about GLOBAL LAB™'s add-on STATPACK™ Signal Processing Module.

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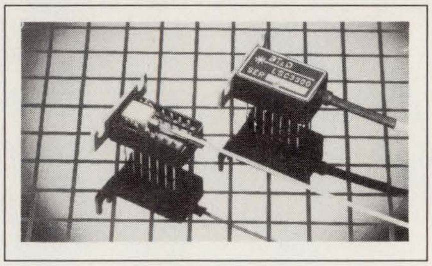
Communications Controller With Buffer Management

The MK5021Q single-channel HDLC serial communications controller (SCC) can operate with data rates as high as 7M bps. It performs buffer management internally to reduce the load on the host processor. The data buffer is based on independent transmit and receive circular buffers. The user can determine which portion of a 16M-byte address range the SCC's circular buffers will occupy. Buffers can be concatenated for long messages, and a programmable byte-swap feature ensures compatibility with most 8- and 16-bit microprocessors.

On-chip testing facilities include four loopback configurations and a self-test program for nearly all the device's major blocks. The MK5021Q has the same footprint and host-processor interface as the company's other controllers, and thus allows a common design approach for all data-communications requirements. $24.50 (1000).

SGS-Thomson Microelectronics, 20041 Agrate Brianza, Via C Olivetti 2, Italy. Phone 39 39 655 5597. Booth No 24 C14. **Circle No. 716**



Laser Module

The LSC3300 laser is a fiber-optic light source that operates in the 1280- to 1300-nm band. The device is suitable for telecommunications, LAN, fiber-optic-sensor, and instrumentation applications, for example, where extreme temperatures are not a factor. The internal semiconductor lasers are based on InGaAsP buried heterostructure technology. Typical output is 200 μW and modulation capability is 1G bps max. The device includes a photodiode for monitoring the laser output. In a 14-pin plastic package, £195 (500).

BT&D Technologies, Whitehouse Rd, Ipswich IP1 5PB, UK. Phone 44 473 42250. Booth No. 24 B17A. **Circle No. 717**

Isolated Dual Transmitter/ Receiver Interface Circuit

The NM232DD electrically isolated dual transmitter/receiver interfaces data-terminal equipment with data-communications equipment. The device includes two data-receive and two data-transmit channels, each of which is TTL/CMOS com-

SBE... At the Core of WAN Interface Solutions

The SBE VCOM-4 Multiprotocol Communications Controller . . . ***today's high-performance, cost effective WAN interface.*** For price-performance in a *single* VMEbus communications controller, nothing equals the new SBE VCOM-4.

This exclusive SBE card features *four* full-duplex, independently programmable serial channels. Yet, it takes up only one VMEbus slot and provides twice the throughput of conventional boards. A complete implementation of X.25 is available ported to the VCOM-4, which speeds your product to market.

The result: an unmatched WAN interface for VME-based hosts, front-end processors, and data/voice networking systems, including: ▪ Two channels at T1 speeds. ▪ All four channels can operate with *sustained* throughput at speeds up to 768 Kbps, interfacing to fractional T1 services or 56/64 Kbps lines. ▪ Each communications channel can be *independently* configured to support HDLC, SDLC, Bisync, Async.

Turn to SBE and the VCOM-4 for the core of your VMEbus WAN product design application. For fast action, contact SBE, Inc., 2400 Bisso Lane, Concord, CA 94520, or call **1-800-347-COMM.**

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CIRCLE NO. 63

SBE

Communications & Real-time Solutions

patible at the logic connections and EIA-232-D and CCITT V.28 compatible at the interface boundary.

A single 5V supply powers all functions on either side of the isolation boundary; no external components are needed. A low-power shutdown mode and high impedance state for receiver inputs are pin controlled. The isolation voltage level is 1500V rms for 1 sec. The operating temperature range is 0 to 70°C. In a 24-pin DIP, £24 (500).

Newport Components Ltd, Tanners Dr, Blakelands North, Milton Keynes, MK14 5NA, UK. Phone 44 908 615232. FAX 617545. Booth No. 1 A05. **Circle No. 718**

16M-Bit Dynamic RAM

Samples of this company's long-awaited 16M-bit dynamic RAM will be on display at Electronica. The 144-mm^2 silicon chip integrates more than 33 million components; it is fabricated using 0.6-μm CMOS technology. The chip is currently entering pilot production under reference number HYB 511610-60/80.

Siemens AG, Postfach 10 12 12, D-8000 Munich 1, Germany. Phone 49 89 2340. FAX 2342824. Booth No. 2 E07 and 23 A4.

Circle No. 719

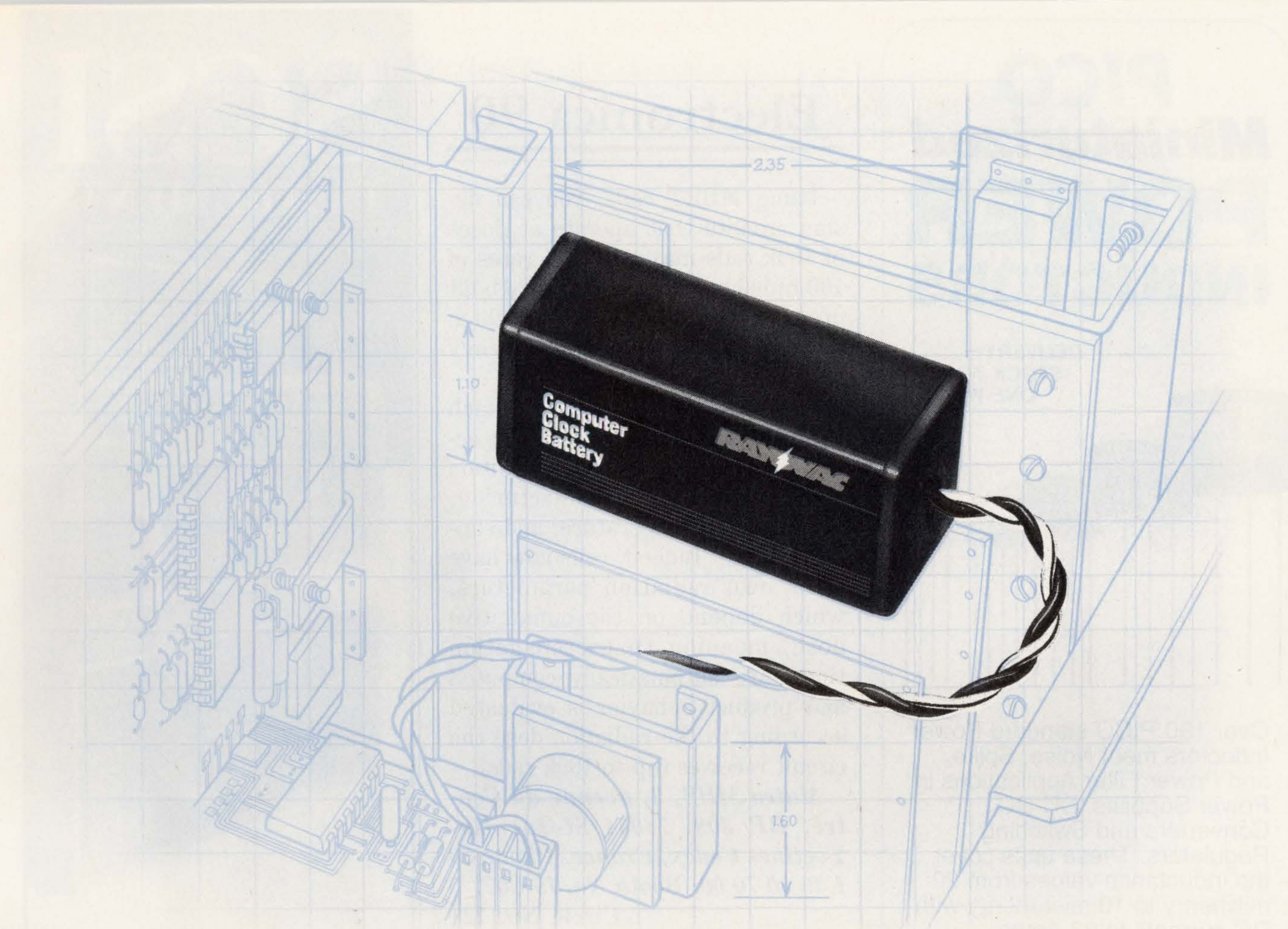
300-Baud Modem

The S3531 is a single-chip CMOS device for stand-alone use or for direct design into data-terminal equipment. The device furnishes full-duplex operation using Bell 103 or CCITT V.21 protocols; it also has a built-in RS-232C serial interface. The modem features transmit and receive filtering; answer/originate mode selection; and digital and analog loopback test modes. Applications include office automation, laptop computers, and alarm systems. 6 DM (500,000).

Austria Mikro System International GmbH, Schloss Premstätten, A-8141 Unterpremstätten, Austria. Phone 43 31 36 36 66-0. Booth No. 19 A12. **Circle No. 720**

Design Data Library For Rad-Tolerant Arrays

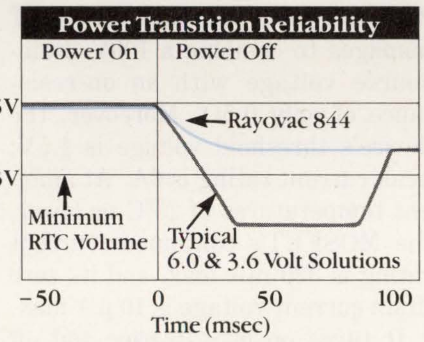
MBRT (MHS MB Series Radiation Tolerant) is a new computerized design-data library for a family of double-metal CMOS gate arrays with very low power consumption for radiation-tolerant applications. The MBRT library, which is supported by SDS and HILO tools on VAX or Sun hardware, covers a range of cells that can operate under harmful radiation. The n and p transistors on which the cells are based have an effective length of 1.5 μm. Operational frequencies can reach 35 MHz at 100k rads.



WHY MORE COMPANIES ARE PLUGGING US INTO THEIR DESIGNS.

Today the Rayovac 844 computer clock battery is specified by 23 system architects worldwide. Its proven reliability safeguards the configuration file memory in 286/386/486 personal computer products, especially in power-down situations.

Maintaining voltage is just one way the Rayovac 844 delivers superior reliability. It also offers long life, a 3-5 year span, plus safety no lithium battery can match.



The 844 ensures IC voltage above the critical 3.0V level maintaining clock stability and configuration file memory.

The 844 is compatible with industry standard chip sets: Chips & Technology; VLSI Technology; Western Digital; Zymos and Intel. And it's made in the U.S.A., with on-time delivery available around the world.

So plug added reliability and service into your design. Specify a Rayovac 844. Call Rayovac's Technical Sales & Marketing Department for complete information and battery specifications at 608-275-4694.

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CIRCLE NO. 64

Electronica 90

Using MBRT cells, you can design circuits that operate at doses of 100k rads max and dose rates of 100 rads/hour. The circuits are built on an epitaxial substrate, which avoids problems caused by heavy ion bombardment.

The characteristics of each MBRT library cell now take into account radiation effects, in addition to effects due to manufacturing, output load, temperature, and supply voltage. Indeed, cells now have their own radiation parameters, which depend on the cumulative dose, meaning that propagation times are automatically computed and product behavior is evaluated according to the radiation dose the circuit receives (up to 100k rads).

Matra MHS, 3, avenue du Centre, BP 309, 78054 St-Quentin-Yvelines Cedex, France. Phone 33 1 30 60 70 00. Booth No. 19 C07.

Circle No. 721

N-channel MOSFET

A MOSFET's on-resistance normally rises considerably as its voltage rating increases. The ZVNL110A N-channel MOSFET manages to combine a 100V drain-source voltage with an on-resistance of only 0.5Ω. Moreover, the device's threshold voltage is 1.5V; peak current rating is 6A. At ambient temperatures of 25°C or lower, the MOSFET's continuous current rating is 320 mA max, and its zero drain current voltage is 10 μA max.

It turns on in <15 nsec and off in <25 nsec for a 1A drain current. Input capacitance is 75 pF; rise and fall times are both <14 nsec. The 2.5×4.8-mm device can dissipate 0.7W within the −55 to +150°C operating range. 20p (100).

Zetex Semiconductors, Fields New Rd, Chadderton, Oldham, OL9 8NP, UK. Phone 44 61 627 4963. Booth No. 24 A24.

Circle No. 722

BROOKTREE'S IMAGE TECHNOLOGIES

Capture iT

Change iT

Capture an image, manipulate it, transmit it, display it—and do it all with Brooktree's Image Technologies. They'll give your system a visual edge in competitive markets.

In fact, Image Technologies can be the key differentiator in today's look-a-like world. At Brooktree, we're dedicated to creating the highly integrated devices designers need to set their systems apart with exciting imaging and graphics capabilities.

IMAGE ACQUISITION

Image Acquisition starts with our Bt251 Gray-Scale or Bt253 Color Image Digitizer chips. They're the easy, economical way to add image capture to your system, with flexible architectures and standard MPU interfaces.

And they link up to our new Bt261 30 MHz Line Lock Controller. It will change the way you bring video images into your system. It's flexible and fully programmable.

Program it to strip horizontal and vertical sync information from any incoming video signal it encounters. Program its sync noise gating to cope with noisy signals and to enable locking to horizontal sync.

In fact, you won't find a more flexible solution to the timing control section of your design. Or a better way to assure your Image Acquisition system is programmed for success.

IMAGE MANIPULATION

Once you capture an image, change it.

That's easy with our Bt281 real-time Color Space Converter/Color Corrector chip. It's programmable and lets you convert from any color space to any other, including YIQ, YUV, RGB and Y, R-Y, B-Y, while capturing or displaying the image.

So now you can optimize the color space of your frame buffer for image processing independent of the video signal you're digitizing and the CRT's RGB needs. The Bt281 handles everything.

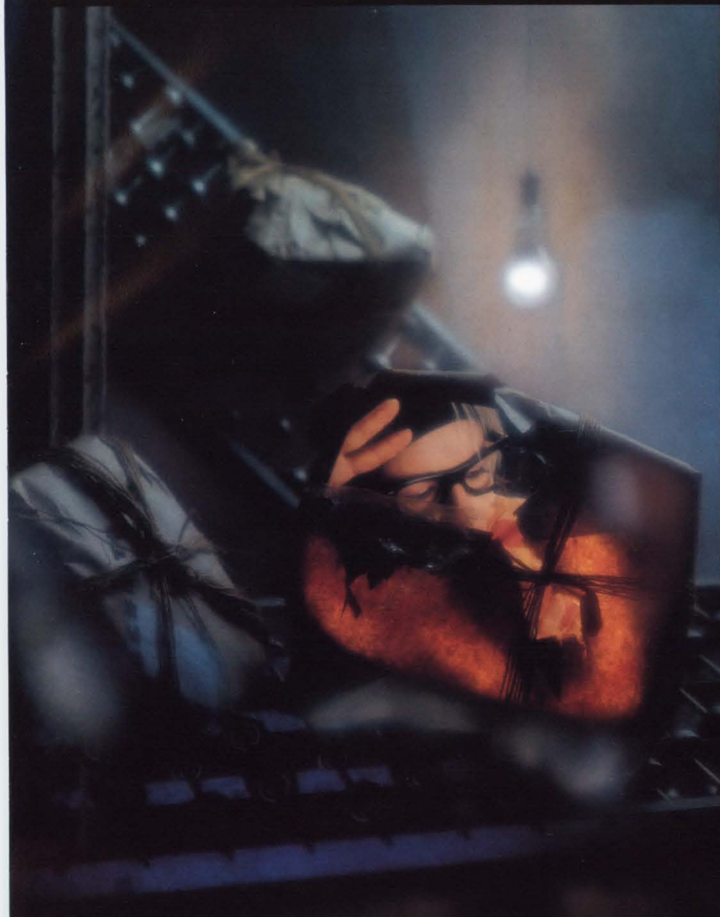
Since the Bt281 has programmable matrix coefficients and input look-up RAMs you can also use it for gamma correction, color correction or other image restoration techniques.

And if you think that's hot, you should see the Image Manipulation chips we'll be introducing this winter. Here's a hint: It will scale new heights.

IMAGE TRANSMISSION

How can you send your image from here to there? Digitally? In real time?

Enter two more pieces of Brooktree's Image Technologies story: The Bt291 and Bt294 VideoNet™ point-to-point Video Interfaces.



Send iT Display iT

Simply put, the Bt291 and Bt294 let you ship and receive live color digital video using an 8-bit interface.

Which means you can replace about a square foot of board real estate with two highly integrated devices. And take the rest of the week off.

The two devices have, respectively, input or output look-up table RAMs to simplify the interface to the frame buffer and to add or remove gamma correction and scale signal levels.

So if you're working with CCIR601, SMPTE RP125, EBU 3246-E or other digital video standards, we've done our parts. You take it from here.

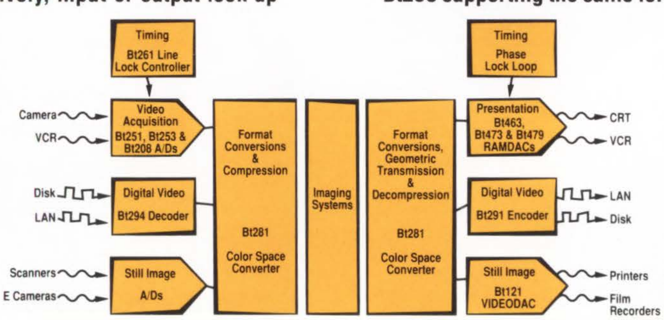


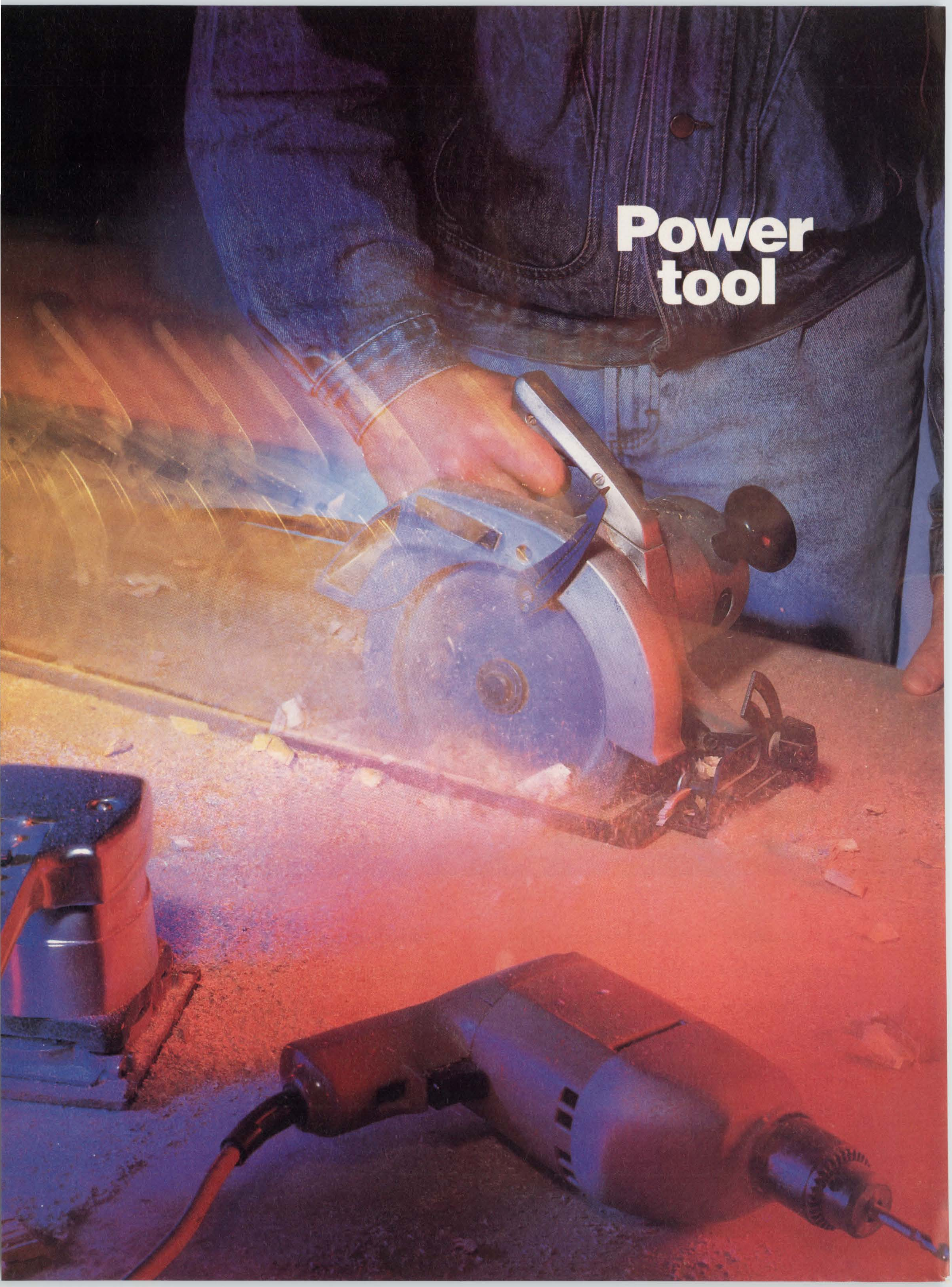
IMAGE PRESENTATION

When it comes to display technology, our true colors really shine. We invented RAMDACs. We understand the special needs of graphics systems designers. And we've never stopped innovating.

A perfect example is our Bt473, designed specifically for VGA true-color graphics. It has three 256x8 color look-up tables with 8-bit video D/A converters to support 24-bit true-color operation. And it can also support 8-bit pseudo-color, 8-bit true-color and 15-bit true-color operations. That makes it a perfect match for the Bt253 supporting the same formats.

Now our new TrueVu™ RAMDAC, the Bt463 is what's hot for designers of next-generation workstations eager to add windows capability, and delighted to do virtually everything with a single device. The Bt463 is the first monolithic true-color RAMDAC. That means it supports multiple display modes—both True Color and Pseudo Color—simultaneously. And with multiple windows, you get multiple colormaps, avoiding conflicts. Bt463 supports multiple plane depth, too, so a window can be 24, 16, 12 or 8 planes deep. And for a little frosting on the cake, it's flexible and easy to design in.

Power tool

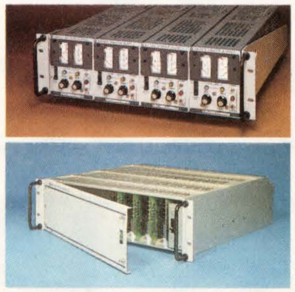


Power tools

KEPCO DIGITAL POWER CONTROLLERS

Choose your tools carefully for the work at hand. Choose a single unit ATE power supply and drive it with an SN digital analog interface to translate GPIB commands to useful voltage and current or choose a multiple-unit TMA-MAT system and drive up to 27 independent voltages and currents from a single GPIB address with full status monitoring and read back of actual values.

Kepco's power tools are carefully calibrated to provide you with just the right combination for the work you need to do.



dc, unipolar power

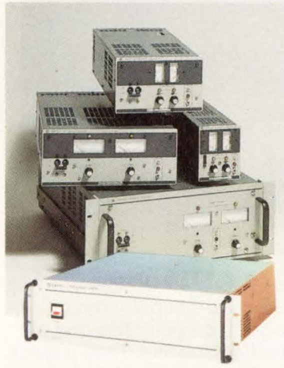
- ☐ Listen only, GPIB
- ☐ 12 bit control, 0-6V to 0-325V, unipolar dc
- ☐ Power: 50W, 100W, 250W, 500W, 1000W
- ☐ Control one, four or eight units, analog drive

SN/ATE

dc, bipolar power

- ☐ Listen only, GPIB
- ☐ 12 bit control ± 20V to ± 200V bipolar dc
- ☐ 100W, 200W, 400W
- ☐ Single unit, self-contained

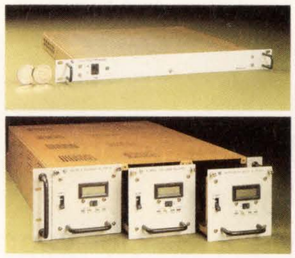
BIT/BOP



dc, unipolar power

- ☐ Listen, talk-verify, GPIB
- ☐ 12 bit control, 0-6V to 0-325V unipolar dc
- ☐ Power: 50W, 100W, 250W, 500W, 1000W
- ☐ Control one to sixteen units, analog drive

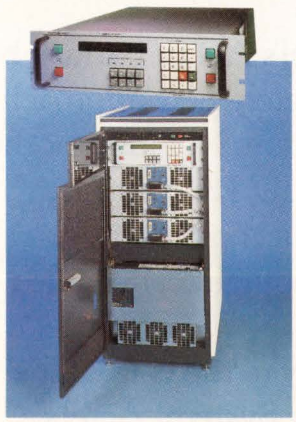
TLD/ATE



dc (selectable polarity) power

- ☐ Talk-listen, GPIB, full read back of both voltage and current
- ☐ 12 bit control, 0-6V to 0-150V Unipolar dc with polarity selection
- ☐ Power: 360W, 720W, 1080W
- ☐ 1-27 unit control, digital (bit-bus) drive

TMA/MAT



ac power

- ☐ Talk-listen, GPIB
- ☐ 12 bit control, 0-125V ac 47-2000Hz ac power
- ☐ 1KVA to 18KVA
- ☐ Expandable to 90KVA

RGB/BOP

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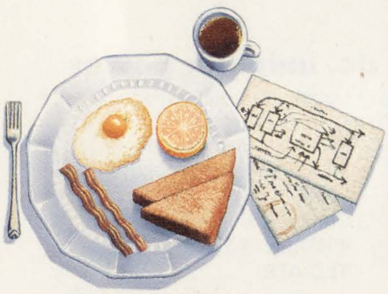
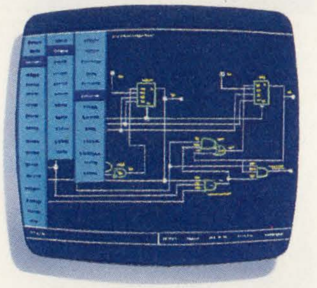
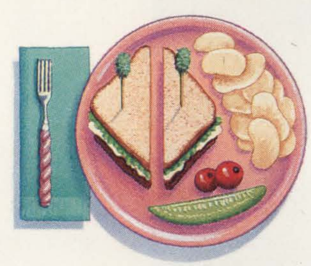


7:05 am : Breakfast
Suddenly, between bites, the answer to that new system design jumps right into your brain. But how to make it work in silicon? Use an Actel field programmable gate array!



8:50 am : Design
You warm up the design program on your 386 and put in the final touches. Then a quick rule check and 25 MHz system simulation with the Action Logic System software.

11:00 am : Place & Route
You watch the system place and route all 1700 gates (out of 2000 available) in under 40 minutes. 100% automatically! A final timing check. Then think of something to do until lunch.



12:00 pm : Lunch
Remember lunch? Normal people actually *stop working* and have a nice meal—right in the middle of the day! With Actel's logic solution, this could become a habit.

Actel Field Programmable Gate Array Systems.

They're a feast for your imagination.

Actel's ACT™ 1 arrays bring you a completely new approach to logic integration. Not just another brand of EPLD, PAL® or LCA™ chips. But true, high density, desktop configurable, channeled gate arrays.

They're the core of the Action Logic System, Actel's comprehensive design and production solution for creating your own ASICs. Right at your desk. On a 386 PC or workstation. With familiar design tools like Viewlogic,™ OrCAD,™ and Mentor.™

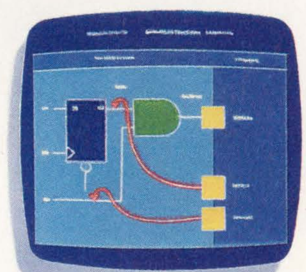
And do it in hours instead of weeks. Even between meals.

How? With features like 85% gate utilization. Guaranteed. Plus 100% automatic placement and routing. Guaranteed. So you finish fast, and never get stuck doing the most

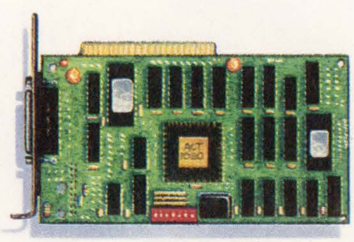
Actel FPGA Product Family		1010A	1020A
Equivalent Gates	Gate Array	1200	2000
	PLD/LCA	3000	6000
User I/O		57	69
System Clock (MHz)		20-40	20-40
Availability		NOW	NOW
Technology (micron)		1.2	1.2

Breakfast And
n By Dinner.

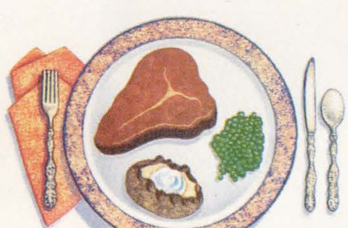
1:15 pm: Program
You load the Activator™ programming module with a 2000-gate ACT 1020 chip and hit "configure." Take a *very* quick coffee break while your design becomes a reality.



1:25 pm: Test
You do a complete, real-time performance check, with built-in test circuits that provide 100% observability of all on-chip functions. *Without* generating any test vectors.



4:00 pm: Production
Your pride and joy is designed, created, tested, and off to the boys in Production. And you're finished *way* ahead of schedule! Better think of something to do until 5:00.



6:00 pm: Dinner
Remember dinner? Normal people actually *go home* and eat with their families. On your way, start thinking about how Actel's logic solution can help you be brilliant tomorrow.

tedious part of the job by hand.

Design verification is quick and easy with our Actionprobe™ diagnostic tools, for 100% observability of internal logic signals. Guaranteed. So you don't have to give up testability for convenience.

In fact, the only thing you'll give up is the NRE you pay with full masked arrays. You can get started with an entry level Action Logic System for under $5000. Guaranteed.

And Actel FPGAs are even 883 mil-spec compliant.

You can be brilliant right now with 1200- and 2000-gate devices, and a whole new family of 8000-, 4000- and 2500-gate parts are on the way. Call **1-800-227-1817, ext 60** today for a free demo disk and full details about the Action Logic System.

It could make your whole day.

Actel
Risk-Free Logic Integration

Peak performance under extreme conditions.

NEC's SVH-Series chip tantalum capacitors scale new heights of performance and reliability for automotive and other tough applications.

Our SVH capacitors offer a failure rate of just 0.5% per 1,000 hours. If obstacles like excessive heat and humidity seem insurmountable, don't worry. SVH caps withstand 1,000 temperature cycles from −55°C to +125°C. Their humidity resistance is 85°C, 85% RH for 1,000 hours.

We offer 29 types with ratings from 0.1 to 33μF, and from 10 to 35V DC.

A top-quality team of chip tantalum caps.

Reliable NEC caps also come in a wide array of device types.
Our diversified lineup includes:

R-Series
- ☐ 96 types.
- ☐ 0.01 to 68μF; 4 to 35V DC.

R-Series Extended-Capacitance
- ☐ 58 types.
- ☐ Up to 15μF rating for A case (1.6 x 3.2 x 1.6mm).
- ☐ 0.1 to 100μF; 2.5 to 35V DC.

SVE-Series
- ☐ Built-in fuse; 21 types.
- ☐ 1.0 to 33μF; 10 to 50V DC.
- ☐ R-Series compatible.

Reward yourself with reliability.

NEC produces 2 billion tantalum caps per year—more than anyone else in the industry. Our path-breaking R&D effort covers everything from improving materials to enhancing design and production processes.
That's why we lead the industry with high-performance tantalum capacitors such as the ultra-reliable SVH-Series.

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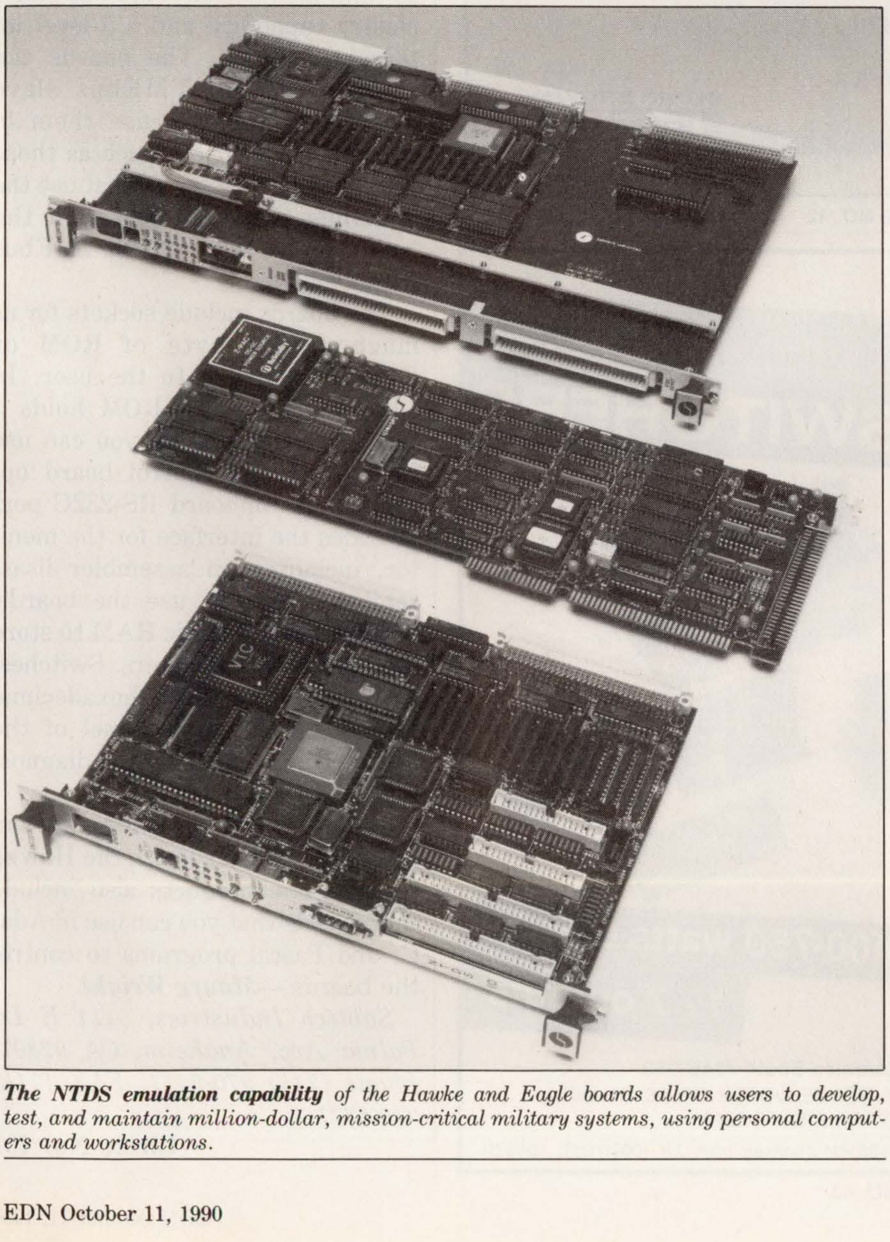
CIRCLE NO. 68

NEC

VMEbus and IBM PC NTDS interface boards emulate MIL-STD-1397B host or peripherals

The Hawke (VMEbus) and Eagle II (IBM PC/AT bus) NTDS (Navy Tactical Data Systems) interface boards allow you to emulate expensive host computers or peripherals with personal computers and workstations. The boards comply with the NTDS communications standards specified in MIL-STD-1397B. Built-in test features handle diagnostics on the boards. Both boards include software that you can use for interactive operations and software interfaces to high-level languages such as C.

NTDS computers and peripherals suitable for use in military mission-critical applications regularly cost a million dollars or more. The Hawke and Eagle II products emulate such systems, thus targeting applications in the hardware and software development, test, debug, and maintenance of NTDS products. The boards can act as passive monitors of NTDS communications and can actively participate in such communications.



The NTDS emulation capability *of the Hawke and Eagle boards allows users to develop, test, and maintain million-dollar, mission-critical military systems, using personal computers and workstations.*

The Eagle II and II+ products for IBM PC/AT and compatible computers offer compatibility with MIL-STD-1397B type B and C communications. Type B (also referred to as NTDS Fast) specifies binary voltage levels of 0V for a logical 1 and −3V for a logical 0, as well as 250k-word/sec data transfers on a single parallel cable. Similar type C (called ANEW) communications use 0V as a logical 1 and 3.5V as a logical 0. The Eagle boards can communicate over distances of 200 ft using differential transceivers in 16- and 32-bit modes.

Two independent 32-bit-wide data channels allow the Eagle boards to perform full-duplex communications. The $4050 Eagle II board includes 1k×32-bit FIFO buffers for both channels. Add $500 for the 2k×32-bit buffers on the Eagle II+. The boards can run at a 1M-word/sec data rate. As many as 32 boards fit in a single system.

MS-DOS-based software included with the boards allows you to interactively setup operations such as setting a board to bus monitor mode. A set of software drivers, including source code, comes with the boards; you can use the drivers with C and other languages.

The VMEbus Hawke board family includes models that support type A/B communications and type B/C communications. Type A communications (also called NTDS Slow) employ binary voltage levels of 0V for a logical 1 and −15V for a logical 0, and perform parallel data transfers on a single cable at 41,667 words/sec.

The Hawke boards include two channels for full-duplex operation, and dual 256k-byte video RAM buffers dedicated to FIFO operations. The 3-ported, video-RAM buffer design allows the onboard processor or processors elsewhere in a VMEbus system access to the buffer memory during operation. The boards can perform 8-, 16-, 24-, and 32-bit NTDS data transfers.

You can order the Hawke boards in 6U or 9U VMEbus sizes. Each model in the Hawke family costs $5000. The boards include a 68020 µP and include full VMEbus slot-1 master capability and a 7-level interrupt handler. The boards can also operate in VMEbus slave mode, and you can use them in popular workstations such as those from Sun Microsystems that use the VMEbus. You can program the boards for 8-, 16-, or 32-bit VMEbus data transfers.

The boards include sockets for as much as 1M byte of ROM or EPROM available to the user. In addition, a system ROM holds a monitor program that you can use to interactively control board operation. An onboard RS-232C port provides the interface for the monitor, including an assembler/disassembler. You can use the boards' battery-backed static RAM to store configuration parameters. Switches, LED indicators, and a hexadecimal display on the front panel of the boards aid in operation and diagnostics.

You get a Unix operating-system I/O driver standard with the Hawke boards. The products also include source code that you can use in Ada, C, and Pascal programs to control the boards.—***Maury Wright***

Sabtech Industries, 5411 E La Palma Ave, Anaheim, CA 92807. Phone (714) 970-5311. FAX (714) 970-5377.

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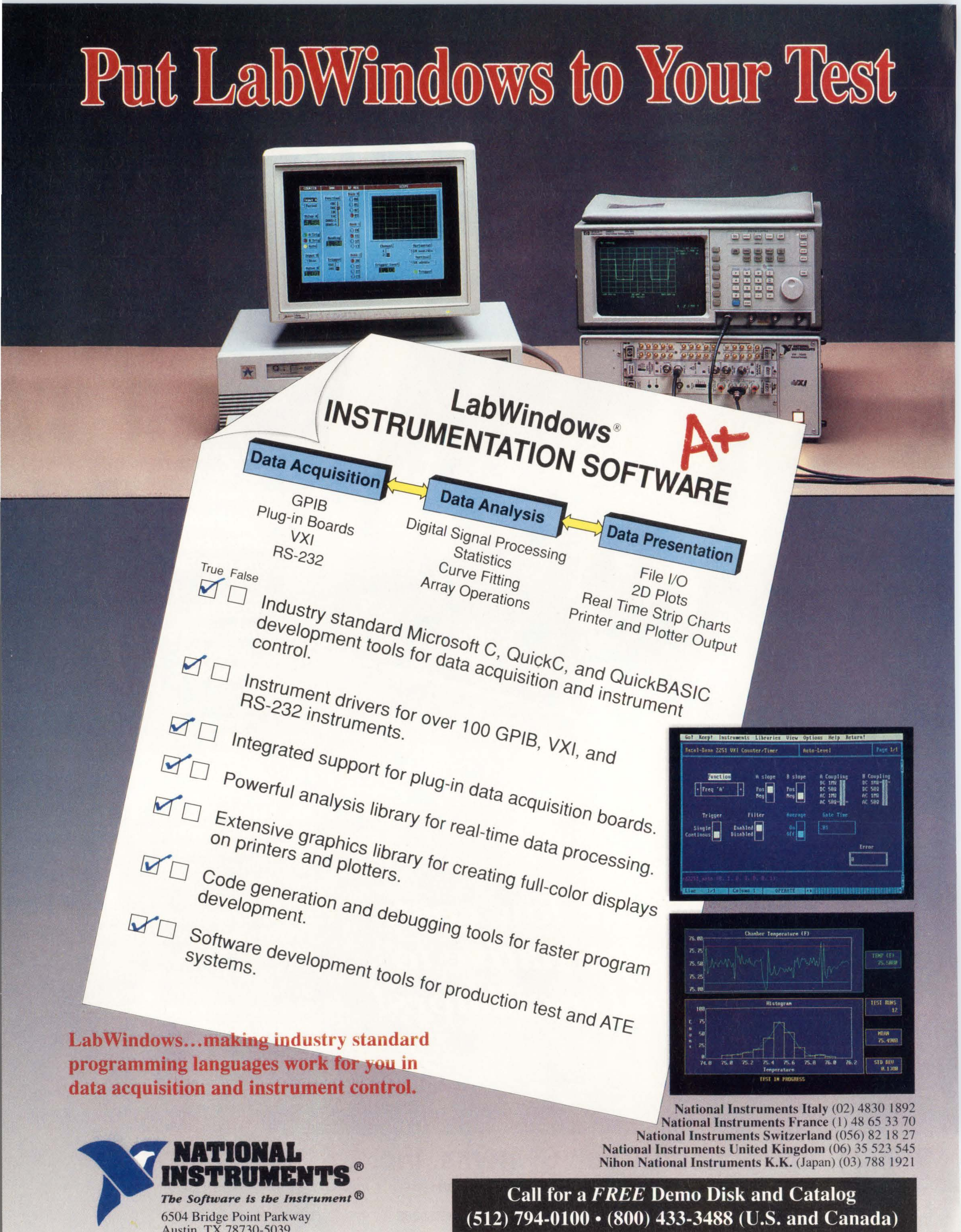
Tel: (215) 666-1900 • FAX: (215) 666-1099 **CIRCLE NO. 69**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CIRCLE NO. 70

Alternating voltage DVM calibrates top-end ac calibration instruments

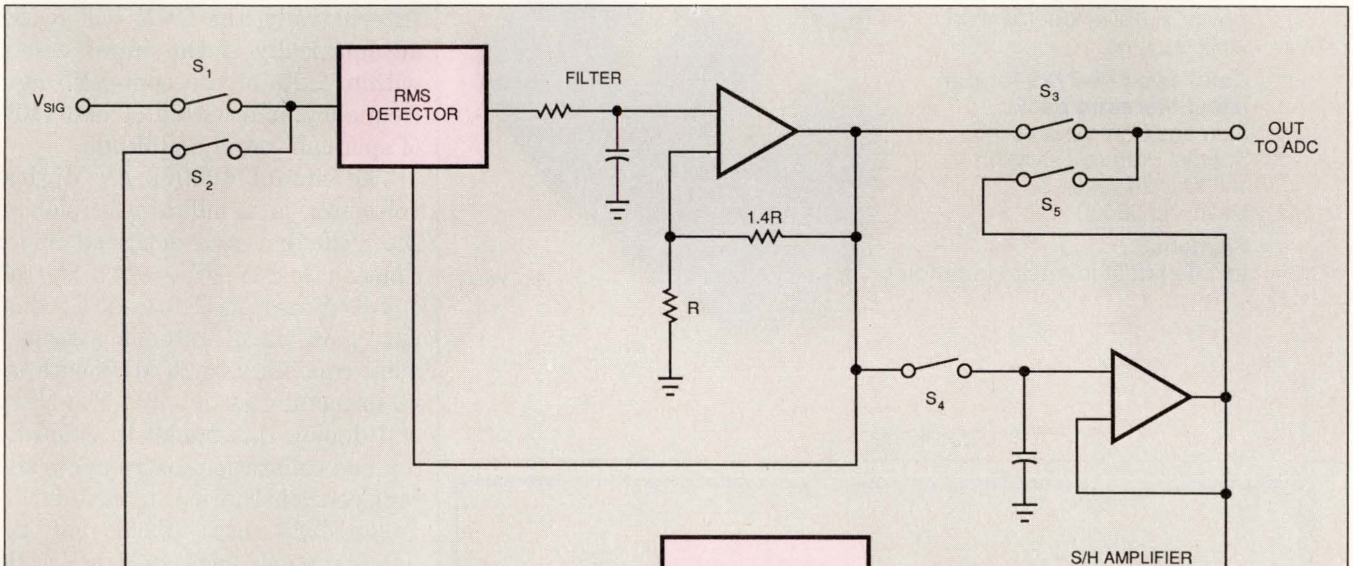
In a calibration hierarchy, the 4920's accuracy positions it between National Standards authorities, such as National Institute of Standards and Technology (NIST, Gaithersburg, MD) and top-end ac calibration instruments.

Used as a conventional DVM, optimal total-measurement uncertainty is ±38 ppm for inputs of 0.9 to 11V, and for input frequencies of 40 Hz to 30 kHz. If you make a measurement at a precalibrated spot in this frequency range, then measurement uncertainty improves to ±28 ppm. These accuracies hold for one year and ±5°C ambient change from the calibration point of the DVM itself. Generally, the DVM displays 7½-digit resolution on ranges from 300 mV to 1 kV, and for input frequencies of 1 Hz to 1.25 MHz.

For increased accuracy, you can select an ac/dc transfer mode of operation, which reduces total measurement uncertainty to ±14 ppm (NIST's uncertainty contribution to this number is ±7 ppm). In this mode, the DVM sequentially reads your unknown ac signal and a certified dc source. The DVM's solid-state rms detector is a dc-coupled design, which responds similarly to dc or ac inputs. In this mode, equal DVM errors exist in the instrument's signal path for both the ac and dc measurement. These errors cancel out, and the DVM displays the part-per-million difference between the unknown ac input and your dc reference. This transfer mode yields valid measurements when ac and dc inputs are within 1% of each other, between −30 and +10% of nominal range, and when ac frequency is 40 Hz to 30 kHz.

The 4920 exhibits several advantages over other calibration instruments that rely upon traditional thermal techniques. Portability and convenience are primary advances. Also important is the DVM's settling time of <2.5 sec to meet full accuracy specification for frequencies exceeding 100 Hz. Additionally, operation is programmable using an IEEE-488.2 interface.

Recalibration of the DVM itself is totally electronic. In order to



NOTES: FIRST MEASUREMENT = M_1 (S_1, S_4, S_3 CLOSED)
SECOND MEASUREMENT = M_2 (S_4 OPEN, S_5 CLOSED)
THIRD MEASUREMENT = M_3 (S_2 AND S_3 CLOSED)

$M_1 = G \cdot V_{SIG}(RMS)$, BUT $G = \frac{M_3}{M_2}$

THEREFORE, $V_{SIG}(RMS) = M_1 \cdot \frac{M_2}{M_3}$

***You can use the 4920 alternating voltage DVM** to simplify the awesome task of recalibrating premium ac calibration instruments.*

withstand the rigors of transportation, the instrument has no internal trimmers. Each range requires three calibration sources: 1 kHz at nominal range, 1 kHz at 30% of nominal, and 1 MHz at nominal (except 100 V/1 kV ranges). Generally, only national standards authorities such as NIST possess sources of sufficient accuracy for recalibration of the 4920. Even if your laboratory has the necessary sources, maintaining accuracy at this level is expensive. NIST currently demands around $800 per certified calibration point at these levels of accuracy.

In addition to the three calibration points per range for broadband calibration, you can calibrate spot voltage/frequency points. In operation, measurements derived from spot calibrations show an increase in accuracy of 10 ppm for frequencies from 10 Hz to 30 kHz. You can choose display readings with respect to broadband or spot calibrations. Alternatively, the DVM will switch automatically if the input comes within ±2% of the spot-calibrated frequency, and within 50 and 110% of spot-calibrated amplitude.

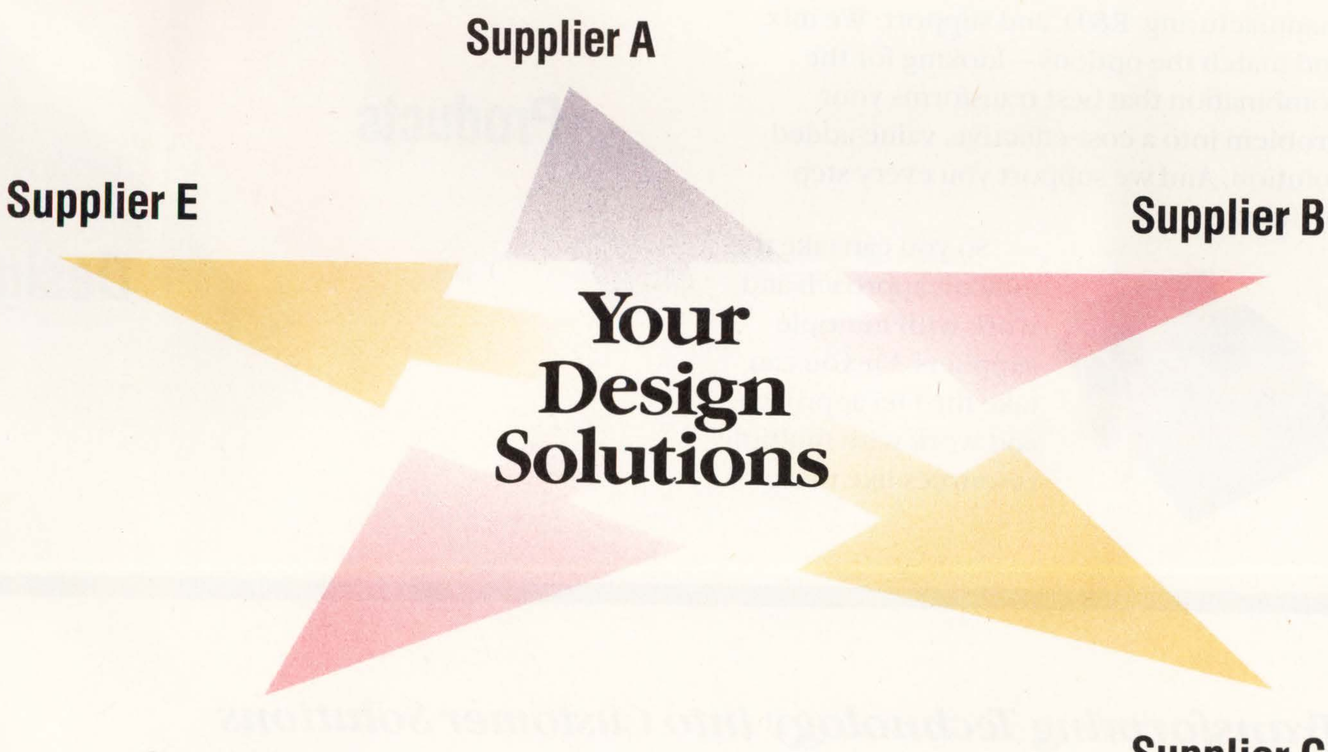
The model 4920M AV digital voltmeter is a military version of the 4920 that was designed under contract to the US Navy's Metrology Engineering Center at Corona, CA. This model extends measurement capability to 20 MHz with total uncertainties to 0.2%. The Navy will deploy this model to calibrate top-end calibration instruments and replace their thermal transfers.

The 4920 costs $9995. For optional ranges down to 1 mV, add $1495. The 4920M sells for $11,995.—***Brian Kerridge***

Datron Instruments, Hurricane Way, Norwich NR6 6JB, UK. Phone (603) 404824. FAX (603) 483670.

Circle No. 730

The difficult approach.



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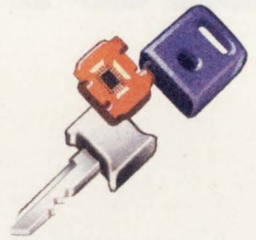
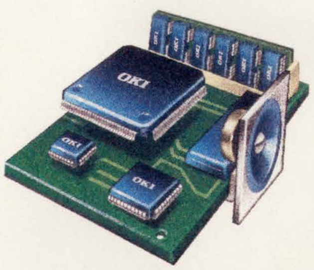


We begin by fully understanding your unique problem. Then, together, we explore Oki's wide-ranging resources in technology, product, design, manufacturing, R&D, and support. We mix and match the options—looking for the combination that best transforms your problem into a cost-effective, value-added solution. And we support you every step of the way.



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CIRCLE NO. 71

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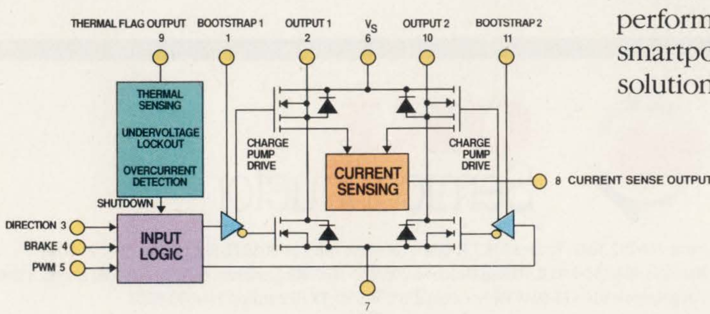

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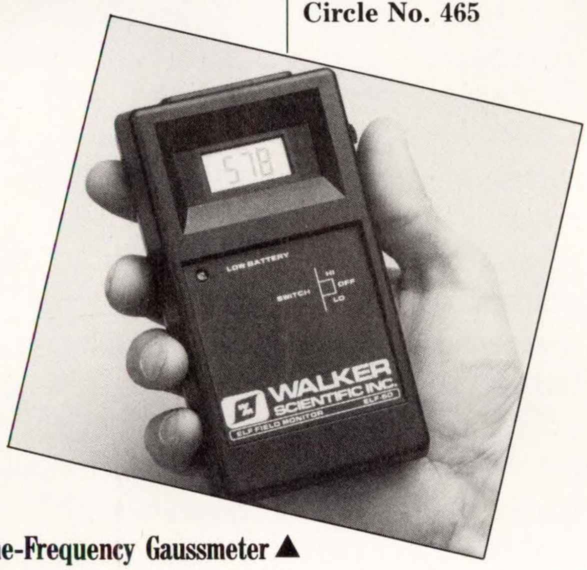
READERS' CHOICE

Of all the new products covered in EDN's **June 21, 1990,** issue, the ones reprinted here generated the most reader requests for additional information. If you missed them the first time, find out what makes them special: Just circle the appropriate numbers on the Information Retrieval Service card, use EDN's Express Request service, or refer to the indicated pages in our **June 21, 1990,** issue.

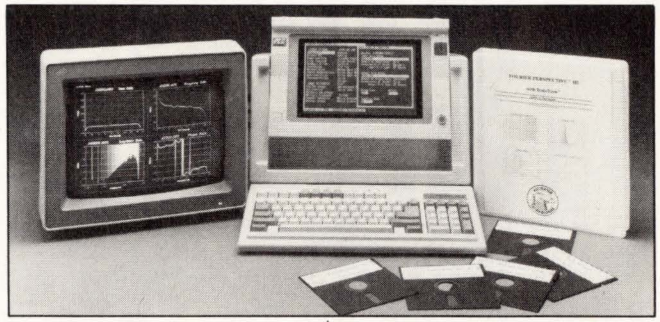


Line-Frequency Gaussmeter ▲

Capable of measuring from 1m Gauss to 20 Gauss at 50 or 60 Hz, the ELF-50D handheld meter registers the strength of magnetic fields generated by ac power lines and equipment connected to them. The unit, which includes a 3½-digit LCD and a low-battery indicator, operates for approximately 50 hours from a 9V alkaline battery (pg 312).
Walker Scientific Inc.
Circle No. 464

Dual Serial/Parallel Board

The DSDP-100 communications adapter provides an IBM PC/AT or compatible with additional ports that allow you to interface network file servers with multiple printers, plotters, and other serial and parallel devices. Each serial port uses a 16450 UART, which supports rates as high as 56k baud. Each parallel port allows bidirectional data transfer (pg 294).
Qua Tech Inc.
Circle No. 465

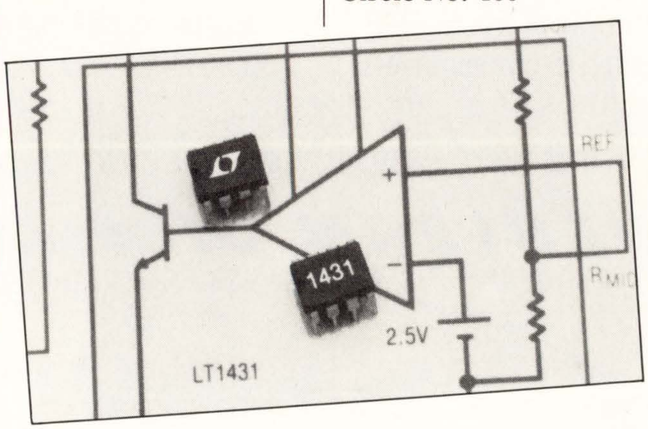


DSP Analysis Software ▲

Running on any IBM-compatible PC, Fourier Perspective III software graphically outputs results of common DSP functions. The software can operate on data sets as large as 65,520 points loaded from disk or captured at runtime from an A/D converter board. The software can perform single-dimension and inverse FFTs. Its signal-smoothing features consist of moving-average filtering and median-window filtering (pg 146).
Alligator Technologies.
Circle No. 467

Programmable Reference ▼

The LT1431 is a precision adjustable-reference and amplifier combination with a 100-mA current-sink capability. On-chip divider resistors let you configure the reference as a 5V shunt regulator with a 1% initial tolerance. By adding two external resistors, you can set the output voltage to any value between 2.5 and 36V. The unit is available in an 8-pin SO surface-mount package or an 8-pin miniature DIP that provide access to numerous internal functions (pg 306).
Linear Technology. Corp.
Circle No. 466



Silicon Accelerometer

The Model 3140 silicon-based accelerometer offers full-scale measurement ranges of ±2 to ±100g. The device's output is compensated to eliminate errors due to temperature. Its full-scale output is ±2V about a 2.5V offset level. Built-in features include signal-conditioning circuitry and a regulator, which allows the unit to operate from an unregulated power supply (pg 286).
IC Sensors.
Circle No. 468

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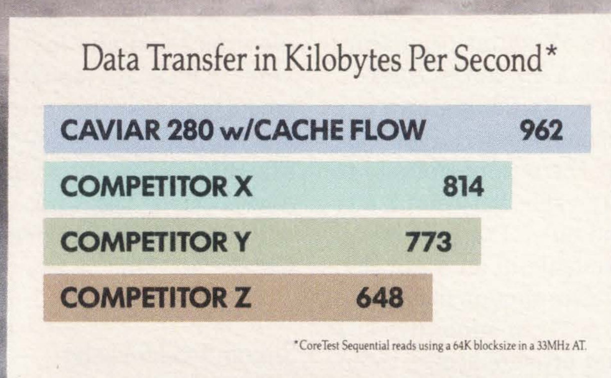

What's more, according to our incredibly conservative attorneys' interpretation of the benchmark data, the 80 Mb drive benchmarked an average access time of less than 18 milliseconds. And according to our engineers' interpretation, our attorneys are, indeed, incredibly conservative.

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EDN SPECIAL REPORT

Video A/D

Choosing and incorporating a video A/D converter requires as much knowledge about video signals and digital video systems as it does about the converter itself. These video systems dictate the strict linearity requirements that converters must meet.

Anne Watson Swager,
Regional Editor

Compared to just a few years ago, converters for video applications have become incredibly cheap—often around or even under $10—and accessible. In addition, manufacturers have overcome many of the performance limitations of early flash-converter designs. Joe Alig, an analog designer of post-production broadcast equipment at Digital F/X (Mountain View, CA), says, "Most converters have gotten so good that I just apply them."

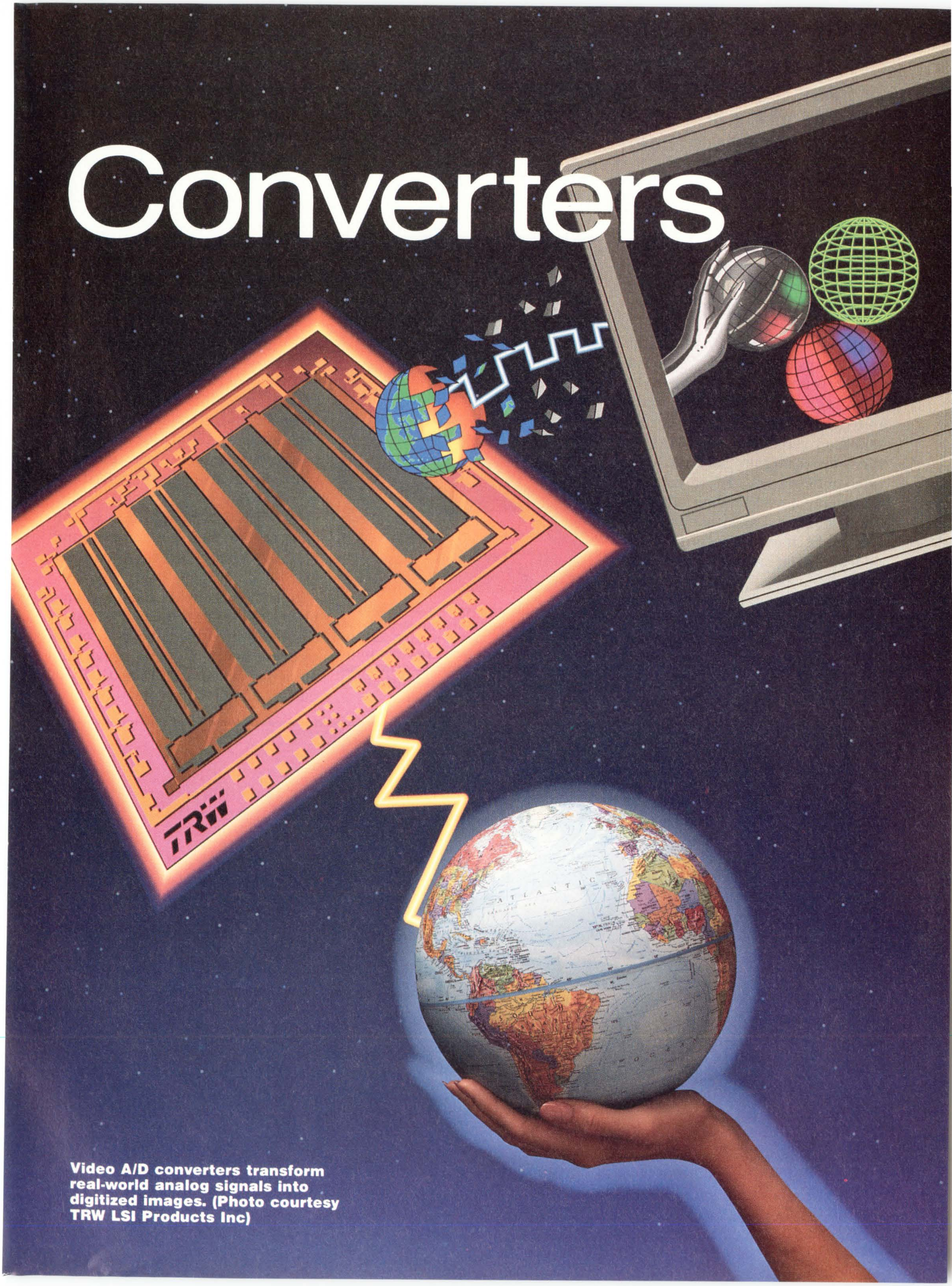
For its part in this advance in video-converter design, TRW LSI Products received an unlikely distinction last year—a television Emmy award. Since the company introduced its TDC1048—the standard 8-bit, 20M-sample/sec converter—many other companies have joined in with second sources, improved drop-in replacements, and proprietary products of their own. Complete video ADCs in hybrid form and multiple ADCs in single packages are also available.

Most manufacturers and users of ADCs agree that once you've established your video-capture system's configuration, finding an ADC and incorporating it are fairly straightforward tasks. Even so, don't think you can take any converter's performance specs for granted. Data sheets often conceal performance aspects that you can only truly evaluate when using the device in your system. Though the list is slowly growing, the number of manufacturers who specify their converters over the full operating-temperature and power-supply ranges is few. TRW is one company that does specify all of its converters under worst-case conditions. Datel also includes minimum and maximum specs over all conditions for its newer products.

Other potential problems with ADCs simply don't appear on data sheets. For example, few ADC data sheets quantify how much noise—known as clock kickback—the converter will introduce into the analog part of your system. An exception is Micro Power Systems' MP8780, which has a typical clock kickback pulse of 10 pA/sec. Ultimately, you will have to test the converter in your own system. Rusty Woodbury, a designer at IEV Visual Information Processing (Salt Lake City, UT) says he bats around 250—about one out of four of the ADCs he evaluates actually meets his design criteria.

The need to test converters isn't a new concept to experienced ADC users. If you're familiar with basic A/D converter specs and with the flash architecture upon which most video converters operate (see **box**, "Flash architectures split in half"), you'll be able to easily comb the data sheets of the converters in **Table 1** (pg 152). If you're new to video designs, however, evaluating and testing a few of the esoteric video specs

Converters



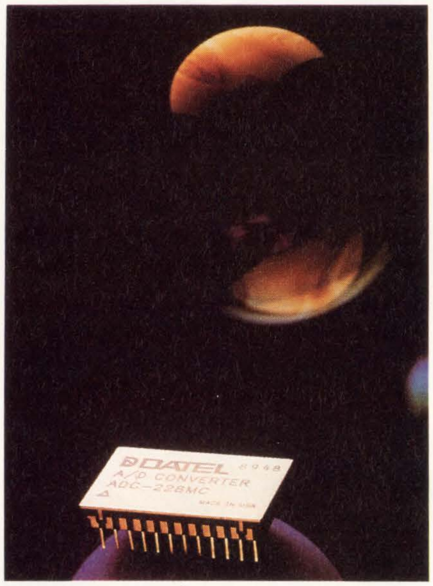
Video A/D converters transform real-world analog signals into digitized images. (Photo courtesy TRW LSI Products Inc)

Video systems have strict requirements for linear behavior because the amplitude and phase of a subcarrier signal convey color information.

such as differential gain and differential phase require a basic knowledge of video signal processing (see **box**, "A glossary of video terminology").

Defining the word "video" isn't exactly straightforward. Video can loosely refer to any higher-speed converter with sampling rates above 1M sample/sec. A tighter definition recognizes converters as video devices if they can digitize TV video information. These converters usually have sampling rates between 10M and 75M samples/sec. The more narrow definition excludes converters with high sampling rates (above 100M samples/sec) that are used in radar imaging systems and those with lower sampling rates (below 10M samples/sec) that also perform imaging functions.

One confusing aspect of video systems and signals is the various forms they can take. "Normal" video signals—anything but high-definition TV—can take two different forms: composite and component. Composite video is the standard signal transmitted from broadcast stations to your TV's BNC connector. It conforms to the same monochrome standard—RS-170—developed in the 1940s and later modified to handle color information. Variations of the standard exist according to geography. NTSC is the US standard, PAL is the standard in most of Europe, and SECAM is used in France and the USSR.



Some video converters also include a number of auxiliary video-processing functions. Datel's ADC-228 includes a wideband analog input buffer, a precision voltage reference, temperature-compensation circuitry, and a 3-state output buffer.

A composite video signal comprises defined intervals for line synchronization, a blanking interval, a color reference or burst signal, and an active video area (**Fig 1**). Sync pulses enable a receiver to lock to

Flash architectures split in half

The most familiar high-speed ADC architecture is the flash architecture. Flash converters contain 2^N-1 comparators, all of which are driven by the same input and, with the help of some decoding logic, convert the input to a digital output in one clock cycle. An 8-bit converter requires 255 comparators—a lot of die real estate—so the pure flash architecture isn't practical for resolutions of higher than 8 bits. The numerous comparators also consume a large amount of power.

To deal with these limitations, various modifications to the flash architecture exist in some of **Table 1**'s products—especially in those with sampling rates close to 10 MHz. Half-flash, 2-step flash, and subranging are several names that refer to a particular modified architecture, and more unique architectures will continue to appear. At this year's International Solid State Circuit Conference, many companies presented converter designs that had novel multistep architectures.

The basic 2-step approach comprises a coarse and then a fine conversion. The converter applies the result of the coarse conversion to a D/A converter and then subtracts the analog value from the input. The converter then applies the result of this subtraction to a second A/D converter to achieve the final result. For an 8-bit converter, the digital output of the coarse conversion represents the four most significant bits, and the digital output of the fine conversion represents the four least significant bits.

The advantages of this architecture include small size—two 4-bit comparators require half as many comparators as an 8-bit converter—and lower power consumption. The smaller die size translates directly to lower cost. Because of the multistep nature of the subranging conversion approach, these converters must have front-end S/H amplifiers. Most, but not all, manufacturers design these front-end S/H amps into their converters. A limitation of the architecture is speed. ADCs that sample at 100 MHz still require the full flash architecture.

the correct portion of the transmitted picture. The receiver then uses the black level to properly dc-bias the transmitted, ac-coupled signal. The blanking interval enables the CRT beam to cross the screen without producing unwanted images.

The active area of a video signal consists of luminance information and, if it's a color signal, chrominance information. The dc level of the active signal area carries the luminance (brightness) signal, which includes all the pictorial information and detail. Chrominance—both saturation and hue of color—is embedded into the luminance in the form of a 3.58-MHz subcarrier signal. The phase relationship between this signal and the color-burst signal determines the

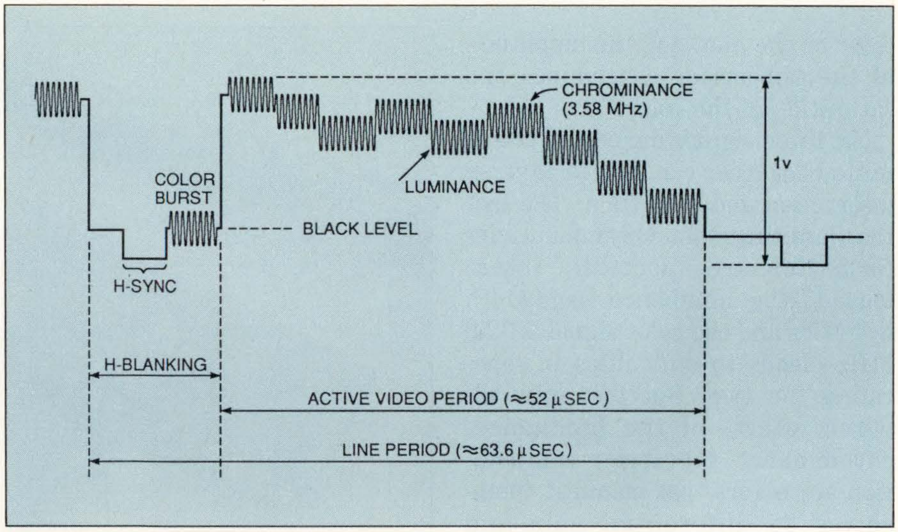


Fig 1—The composite color signal packs a lot of signal content into a 4-MHz bandwidth. The signal includes sync and dc level information that positions the beam on the CRT and helps determine a reference black level. The active video area contains both brightness and color in the form of a dc level and a 3.58-MHz subcarrier signal, respectively.

A glossary of video terminology

Chrominance signal—The 3.58-MHz subcarrier sidebands added to a monochrome TV signal to convey color information. The phase and amplitude components of the chrominance signal represent hue and saturation, respectively.

Composite color signal—The color-picture signal plus all blanking and synchronizing signals. It includes luminance and chrominance signals, vertical- and horizontal-sync pulses, vertical- and horizontal-banking pulses, and the color-burst signal.

Differential gain—The change in output amplitude of a small high-frequency sine wave at two stated levels of a low-frequency signal on which this subcarrier is superimposed.

Differential phase—The difference in output phase of a small, high-frequency, sine-wave signal at the two stated levels of a low-frequency signal on which it is superimposed.

Luminance signal—The portion of the color TV signal that carries the brightness information. It is part of the composite color signal and is made up of 0.30 red, 0.59 green, and 0.11 blue. It can produce a complete monochromatic picture. Also called the Y signal in its component form.

NTSC signal—A 3.58-MHz signal, the phase of which is varied with the instantaneous hue of the televised color, and the amplitude of which is varied with the instantaneous saturation of the color, as specified by the National Television System Committee. Used in the US and Japan.

PAL—Abbreviation for phase alternation line. It pertains to a color-TV system in which the subcarrier derived from the color burst is inverted in phase from one line to the next to minimize hue errors that may occur in color transmission. It consists of 652 lines per frame and 50 fields per second. Used primarily in Europe.

RGB—Red, green, and blue.

RS-170—TV standard for encoding monochrome video.

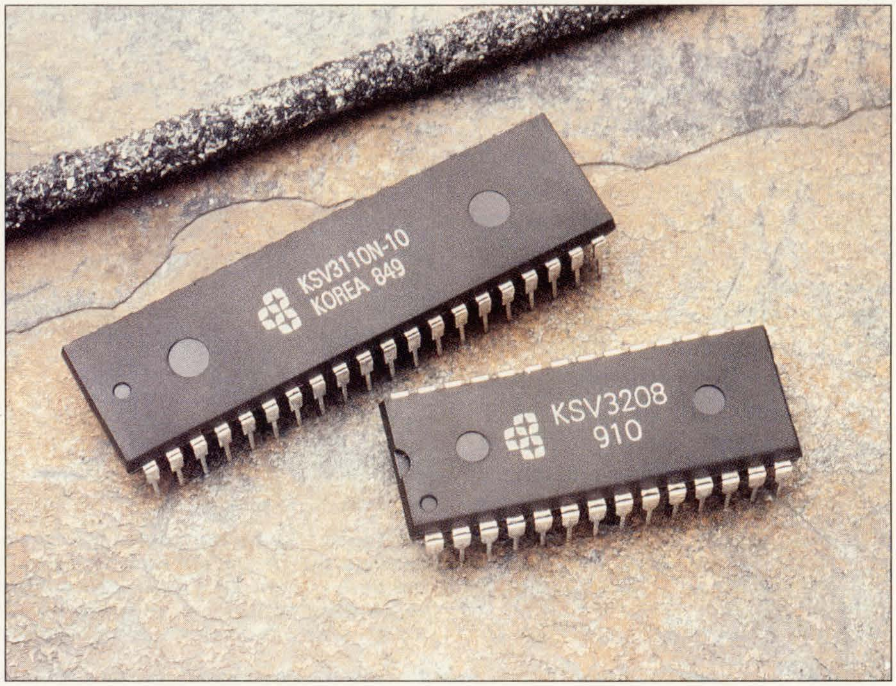
SECAM—Abbreviation for sequential couleur a'memorie (sequential with memory). It is a color-TV system with 625 lines per frame and 50 fields per second developed by France and the USSR and used in some countries that don't use NTSC or PAL systems.

YUV—In addition to RGB, a way of breaking chrominance and luminance into component form.

In component video processing, the system separates the timing from the chrominance and luminance signals prior to the A/D conversion.

color or the hue, and the amplitude of the subcarrier determines the saturation of the color.

All these signals mixed and transmitted together can lead to adverse interaction and distortion. The fact that luminance and chrominance information are spectrally interleaved—the luminance bandwidth is 4 MHz and the color signal is 3.58 MHz—leads to difficulties in separating the two. But the most adverse effects of the luminance-chrominance subcarrier combination are errors that manifest themselves as differential gain and phase. Because amplitude and phase carry color information, the viewer will see a color change if the signal-path circuitry causes any modulation of these quantities in the subcarrier or its sidebands. Thus, distortion-free processing of a color TV signal demands, most importantly, that the amplitude and phase of the chrominance signal not be affected by the luminance function. These demands translate to linearity requirements for video ADCs.



An ADC and DAC combination links two ends of the video-processing chain. Samsung's KSV3110 contains the equivalent of the KSV3208 8-bit A/D converter along with a D/A converter of either 7, 8, 9, or 10 bits. Both chips have an amplifier, clamping, and voltage-reference circuits.

Component processing

The other form "normal video" takes is component video. Most digital processing takes place at the component level, and some systems benefit from breaking down the composite signal—separating the timing, chrominance, and luminance signals—prior to the A/D conversion.

The standard that applies directly to component video processing is CCIR601, commonly known as D1 in the United States. This standard designates sampling rates for the various international systems. For PAL and SECAM, it specifies a sampling clock rate of 13.5 MHz, which corresponds to 720 active picture elements per line. For NTSC systems, the D1 standard proposes a 14.4-MHz clock rate, or four times the color information's 3.58-MHz frequency. Two types of component signals exist: RGB (red, green, and blue) and YUV. The Y in YUV is the luminance information, and the U and V are defined color combinations of red/yellow and red/blue, respectively.

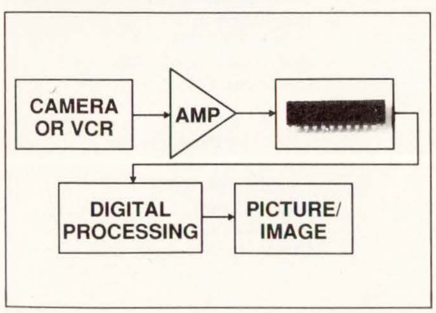
Plenty of examples of both composite and component processing exist, according to Ken Rockwell, an applications engineer at TRW. Some digital video systems' sole purpose is to get a composite signal from one place to the next. Microwave links often transmit digitized composite signals. TV stations with more state-of-the-art equipment use component video signals for the same purpose. Frame-grabber boards for PCs also tend to preseparate the composite signals and work solely with component signals.

The most important ADC specs differ slightly depending on whether you're handling composite or component data. Systems that digitize component video have more analog components on the front end to strip the sync pulses and to extract and recombine the chrominance and luminance. These analog components are susceptible to noise produced by the ADC's sampling clock. Thus, depending on your design and layout, ADCs that digitize component video may have more stringent noise requirements. Alternatively, systems that digitize the complete composite signal and perform the color decoding and sync separation digitally may have less stringent ADC noise requirements.

However, ADCs that digitize component video don't have to meet certain other specs. Differential gain and phase specifications lose significance for component signals because color information is no longer in the form of a subcarrier. Signal-to-noise ratio, or its equivalent effective number of bits, is probably the most important spec for an ADC that processes component signals.

Linearity is crucial for composite video applications because a converter's linearity is tightly coupled to its differential gain and phase. Poor linearity specs will result in poor differential gain and phase specs. Traditionally, 1% and 1° of differential gain and phase were acceptable levels for high-quality, broadcast-type video systems. The converters and the amplifiers that drove them had to have lower specs to meet this requirement.

Now, many video amps designed to drive converters have much tighter specs. According to Analog Devices, its customers are demanding more stringent differential gain and phase measurements. The company says that op amps that handle video signals should have gain and phase specs of 0.01% and 0.01° to meet overall system specs of 0.1% and 0.1°.



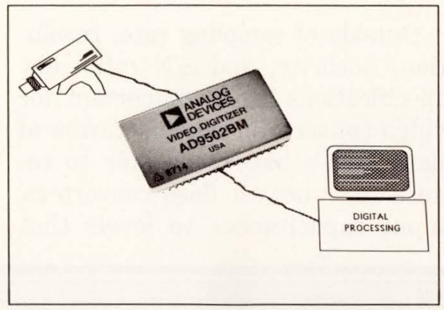
The converter is just one, but central, step in the processing of video signals for later digital manipulation. (Courtesy Micro Power Systems)

Analog Devices is also providing more information to its customers on how to test for differential gain and phase (**Ref 1**). Not all manufacturers of so-called video converters provide complete differential gain and phase specifications. Although the test setup is fairly straightforward, some manufacturers say the test is quite difficult to perform on ADCs. Also, differential gain and phase tests aren't absolute measurements; you must interpret the results visually.

Gain and phase levels are difficult to evaluate on paper because they don't necessarily add linearly. The measurements resemble harmonic distortion in that various parts of your circuit in series can cancel each other. For example, you get something for nothing if the differential gain and phase of your amplifier happen to cancel the differential gain and phase of your ADC. Unfortunately, the behavior of all these elements is unpredictable and requires bench measurements.

Conversion is just the first step

Though different specs are important for different types of processing, basic specs such as sampling rate and resolution must be met in all applications. The most common sampling rate for video designs is 20M samples/sec. A resolution of 8 bits is also standard for video systems. A number of available converters have resolutions of 6 bits, which users say is acceptable for lower-performance systems. However, as 8-bit converter prices come down, manufacturers say there is less demand for 6-bit devices.



For processing RS-170 monochrome signals, Analog Devices' AD9502 hybrid IC includes an amplifier, a sync detector and separator, a pixel-clock oscillator, and an 8-bit flash ADC.

Some higher-performance broadcast systems use 10-bit converters, such as TRW's TDC1020. These devices aren't plentiful, but more should be appearing soon. Analog Devices announced the 9020/9060 last year, and Datel has plans to announce both 10- and 12-bit, 20-MHz subranging ADCs later this year. Sony and Texas Instruments will also announce new video converters in January.

Adding more ADC resolution might benefit some systems, but the increased amount of digital memory required to store the additional bits seems to keep the standard video-ADC resolution at 8 bits. There are ways to get the most out of your ADC's resolution. The resolution of the active-video information increases by almost 30% if the converter doesn't also have to deal with the levels necessary to digitize the sync signals. Thus, you can strip out or simply ignore the horizontal and vertical sync pulses. Some devices in **Table 1** have provisions to do this. For example, Micro Power Systems' converters have selectable input ranges. Also, you can program the fourth pin of Plessey Semiconductors' SP94308 for different dc offsets on the input video.

Outside of sampling rate, resolution, linearity, and S/N ratio, few specifications are as important for video converters. Manufacturers of flash ADCs have been able to reduce their newest flash converters' input capacitances to levels that buffer amplifiers can more easily drive. And if power dissipation is a crucial issue, some of **Table 1**'s CMOS converters consume as little as 35 mA.

In addition to meeting the basic video specifications, many ADCs have video-specific features. Micro Power Systems' converters let you set the input voltage range within the converter's 0 to 5V power-supply range. Philips' TDA8708 and 8709 contain amplifiers with input clamp circuits and external gain control.

Manufacturers of video A/D converters

For more information on video A/D converters such as those described in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

Analog Devices Inc
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FAX (508) 339-6356
Circle No. 655

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FAX (415) 583-4207
Circle No. 658

ILC Data Device Corp
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FAX (516) 567-7358
Circle No. 659

Micro Networks Co
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FAX (508) 852-8456
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FAX (408) 562-3605
Circle No. 661

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(602) 897-3615
Circle No. 662

National Semiconductor Corp
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FAX (408) 980-4599
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FAX (508) 670-9001
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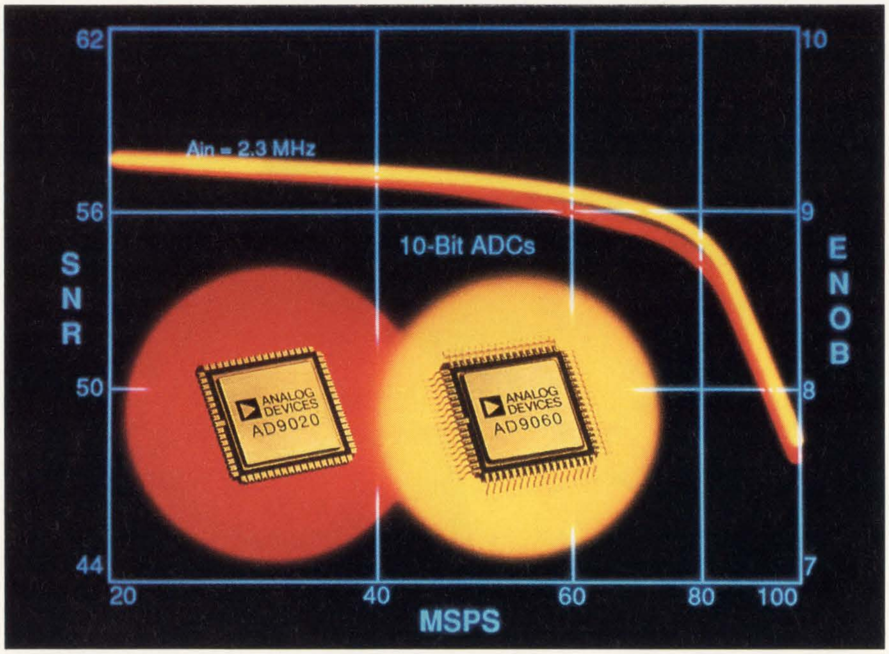

The AD9020/9060 are among the first converters to offer 10 bits of resolution coupled with high speed—a 75M-sample/sec sampling rate. Most video systems require only 8 bits, but some professional video systems require 10. (Courtesy Analog Devices)

Devices with two or three ADCs per package are available. Sipex's SP1072 is **Table 1**'s only dual ADC. A device with three ADCs, such as Brooktree's Bt253, lets you digitize YUV and RGB signals simultaneously. Siemens has plans to announce a similar 3-ADC part by the end of the year. Combining functions from both ends of the processing chain, Samsung's KSV3110 incorporates an ADC with a DAC. "Complete" converters, such as Datel's ADC-228, Sipex's SP1070, and TRW's TDC1068, combine video ADCs with an input buffer, references, and output registers. Add enough features, and you have a complete video digitizer such as Analog Devices' hybrid RS-170 AD9502 video digitizer for monochromatic signals.

The available analog-design expertise, the complexity of your system, and your anticipated volume of systems primarily determine whether you should design from scratch or buy a system-type chip. Although stand-alone ADCs are quite cheap and plentiful, integrating an IC with various other circuit blocks—sync detectors and color decoders—requires low-noise layout and design techniques. Keeping digitally generated noise away from the analog input circuits is a puzzle for any sampling-system designer.

All-in-one ICs offer board-space and design-time savings, but they, too, have limitations. Joe Alig doesn't like too many bells and whistles. "You may not want to use what the chip designers have done—it may impair performance." The chip designer may not have designed sensitive parts of the circuit—such as the separation of the luminance from the chrominance signal—in the way that's best for your system.

In addition to composite and component, high-definition TV is yet another form of video. HDTV has received much press lately, but US standards won't be firmly established until approximately 1993. Depending on the final standard, requirements of various HDTV-related components will vary. It does appear, though, that 10-bit converters and sampling rates much higher than those of today's standard video signals will be necessary.

A few manufacturers have introduced converters with 10 bits of resolution and sampling rates around 75M samples/sec. Although these new parts are stabs in the HDTV dark, you can expect more such parts to appear. Those designers looking for ADCs with high resolution and high speed will definitely benefit from ADC manufacturers' anticipation of increasing HDTV applications. EDN

Table starts on pg 160

References

1. *Analogue Dialogue*, Volume 24, Number 2, 1990, Analog Devices Inc.
2. "IEEE standard for performance measurements of A/D and D/A converters for PCM television video circuit," IEEE Std747-1984, IEEE, New York, NY.

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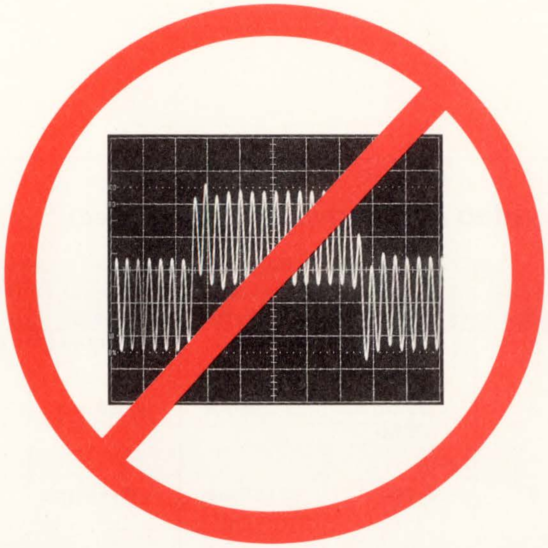

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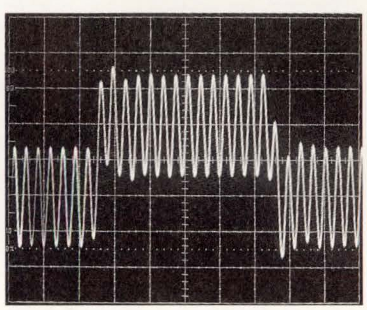

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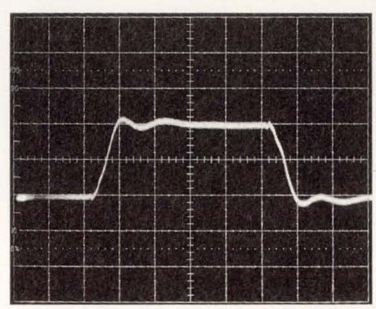

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CIRCLE NO. 92

Table 1—Representative video A/D converters *(continued)*

Manufacturer	Part n	Resolution (bits)	Maximum sampling rate (M samples/sec)	Differential linearity	Integral linearity	Differential phase	Differential gain	S/N ratio
Analog Devices	AD9020/9060	10	60/75 min	1 LSB max	1.25 LSB max	0.5° typ	1% typ	53 dB typ (F_{in}=10.3 MHz)
	AD9048	8	35 min 38 typ	½ LSB max	½ LSB max	1° max	2% max	44 dB typ (F_{in}=1.248 MHz)
	AD9502	8	NA	±2 LSB max	±1% FS typ	NS	NS	NS
Analog Solutions	ZAD1030/1025	10	30/25	±1 LSB max	±1 LSB max	NS	NS	45 dB typ (F_{in}=15 MHz)
Brooktree	Bt208	8	18 max	±1 LSB max	±1 LSB max	1° typ	2% typ	41 dB typ (F_{in}=5.75 MHz)
	Bt251	8	18 max	±1 LSB max	±1 LSB max	1° typ	2% typ	41 dB typ (F_{in}=5.75 MHz)
	Bt253	8	18 max	±1 LSB max	±1 LSB max	1° typ	2% typ	41 dB typ (F_{in}=5.75 MHz)
Burr-Brown	ADC603	12	10 max	¾ LSB	1 LSB max	NS	NS	68.2 dB typ (F_{in}=5 MHz)
	ADC620	12	20 max	½ LSB typ	¾ LSB typ	NS	NS	65 dB typ (F_{in}=9.9 MHz)
Comlinear	CLC920	10	20 min	0.1% FSR max	0.2% FSR max	0.5° max	1% max	59 dB typ (F_{in}=1 MHz)
Datel	ADS-130	12	10 min	±1 LSB max	±1 LSB max	NS	NS	69 dB typ (F_{in}=5 MHz)
	ADC-207	7	20 min 35 typ	±½ LSB max	±1 LSB max	1.5° typ	3% typ	NS
	ADC-208	8	20 typ 15 min	±1 LSB max	±½ LSB max	1.1° typ	2% typ	NS
	ADC-228	8	25 typ 20 min	±½ LSB max	±½ LSB max	1° typ	2% typ	55 dB typ (F_{in}=5 MHz)
	ADC-304	8	20 min	±½ LSB max	±½ LSB max	0.5° max	1.5% max	NS
Fujitsu Microelectronics	MB40576	6	20 min 30 typ	NS	±0.8% max	NS	NS	NS
	MB40578	8	20 min 30 typ	NS	±0.2% max	NS	NS	NS
Harris Semiconductor	CA3306	6	15 min	±0.25 LSB max	±0.25 LSB typ	NS	NS	NS
	CA3318	8	15 min	±1 LSB max	±1.5 LSB max	1° typ	2% typ	NS
Hitachi	HA19211BP/ HA19212P	8	30 typ 20 min	±0.5 LSB typ	2 LSB typ	0.5° typ	1% typ	NS
	HA19213NT	7	30 typ	±0.5 LSB typ	1 LSB typ	0.5° typ	1% typ	NS
	HA19214NT	10	20 typ 15 min	±0.8 LSB typ	±2.5 LSB typ	0.5° typ	1% typ	NS
ILC Data Device Corp	ADC-00110	12	10 min	±1 LSB max	±1 LSB max	NS	NS	68.5 dB typ (F_{in}=5 MHz)

Notes: Specifications cover commercial temperature ranges.
NA=not applicable *DDIP=double-wide DIP †FSR=full scale range
NS=not specified **TDIP=triple-wide DIP

Input-voltage range (V)	Power dissipation (W)	Power supply (V)	Packages	Price (100s)	Comments
±1.75	2.8	±5/5, −5.2	68-pin leaded ceramic, ceramic LCC	$165/$185	Very fast TTL and ECL 10-bit converters. Modified flash architecture uses only 128 comparators.
0 to −2.1	0.55	5, −5.2	28-pin DIP, 28-pin plastic leaded chip carrier, ceramic LCC	$20	Second source to industry standard 1048 with wider input bandwidth (70 MHz) and lower input capacitance (16 pF). Output is TTL compatible. Full flash architecture.
$1V_{p-p}$	1.75	±15 or ±12, 5	40-pin hybrid metal	$289	Complete video digitizer of RS-170, NTSC, or PAL camera signals. Includes video amplifier, S/H amplifier, sync detector/seperator, pixel-clock recovery, and dc restoration.
$1V_{p-p}$ or $2V_{p-p}$	13.9	±15, 5, −5.2	5×7-in. pc board	$1973	Digitally corrected, subranging architecture. Includes track and hold, timing, references, and latched outputs.
0 to 1	0.5 typ	5	24-pin DIP	$10	External zero and clamp control allows ac-coupled signals to be dc restored during each blanking interval.
0 to 1	0.75 typ	5	44-pin plastic leaded chip carrier	$39	Integrates 4:1 analog multiplexer look-up table RAM, and sync detector. Digitizes RS-170 signals.
0 to 1	1 typ	5	84-pin plastic leaded chip carrier	$52	Integrates three ADCs, analog multiplexer and sync detector. Digitizes RGB and YUV signals.
±1.25	6.1 typ	±15, 5, −5.2	46-pin hybrid DIP	$590 to $941	2-step subranging ADC with S/H amp and reference.
±1	7 typ	±15, 5, −5.2	46-pin hybrid DIP	$2399	Harmonic distortion and 2-tone imtermodulation distortion equals −70 dBc. Analog input bandwidth equals 100 MHz typ. 2-step subranging architecture includes S/H amp and reference.
±2	3.65 typ	±5	64-pin DIP	$99.50	Full flash architecture. Fully 883-compliant version also available.
±1.25	4.2 max 3.8 typ	±15, ±5	40-pin TDIP**	$439	2-step subranging ADC. Includes S/H amp, timing circuits, and error correction.
0 to 5	0.385 max 0.25 typ	5	18-pin DIP, 24-pin LCC	$30	Full flash architecture. Low-power CMOS. 16-MHz, −3-dB bandwidth.
0 to 5	0.745 max 0.66 typ	5	24-pin DDIP* or LCC	$50	Same architecture as ADC-207 with additional comparators.
0 to 5	1.6 max 1.4 typ	±15, 5	28-pin DDIP	$185	Includes an input buffer, buffered reference taps. Vendor trims and compensates device over the temperature range.
0 to 5	0.44 max 0.36 typ	5 or ±5	28-pin DDIP	$15	8-MHz, −3-dB input bandwidth. With single-supply operation, input range is 3 to 5V. 0 to −2V range obtainable with dual supplies. Full flash architecture.
4 to 5	0.27 typ	5	16-pin DIP, 16-pin flatpack	$3.20	Full flash architecture.
3 to 5	0.48 typ	5	22-pin DIP	$7.89	Full flash architecture.
1 to 5	0.07 typ	3 to 8	18-pin DIP, 20-pin SOIC	$7.30	Full flash architecture, low-power CMOS. Includes overflow bit.
0 to 7	0.15 typ	4 to 8	24-pin DIP	$31	Full flash architecture, low-power CMOS.
$2V_{p-p}$	0.25 typ	5	28-pin DIP, 44-pin quad flatpack, 30-pin shrink DIP	$7.95	Full flash architecture.
$1V_{p-p}$	0.2 typ	5	30-pin shrink DIP, 28-pin quad flatpack	$5.95	Full flash architecture.
$2V_{p-p}$	0.9 typ	±5	42-pin shrink DIP	$99	Half flash architecture with on-chip track/hold amplifier. TTL, ECL, or other threshold-compatible clock.
±2.5 or ±1	8	±15, 5, −5.2	46-pin plug in	$975	Half flash architecture with internal track/hold circuitry.

Table continued

Table 1—Representative video A/D converters *(continued)*

Manufacturer	Part n	Resolution (bits)	Maximum sampling rate (M samples/sec)	Differential linearity	Integral linearity	Differential phase	Differential gain	S/N ratio
Micro Networks	MN5820	8	20 min	±1.2 LSB typ	±0.4 LSB	NS	NS	46 dB min (F_{in}=2.5 MHz)
	MN5901	8	100 min	±0.6 LSB	±0.5 LSB	NS	NS	42 dB min (F_{in}=1 MHz)
	MN5903	6	70 min	±0.5 LSB max	±0.875 max	NS	NS	35 dB min (F_{in}=10 MHz)
Micro Power Systems	MP7684A	8	20 max	±½ LSB max	±1 LSB max	1° typ	2% typ	46 dB (F_{in}=4 MHz)
	MP7686	6	30 typ 35 max	±½ LSB max	±½ LSB max	1° typ	2% typ	36 dB min (F_{in}=5 MHz)
	MP8780	8	20 max	½ LSB typ at 14.4 MHz	1 LSB typ at 14.4 MHz	1° typ	2% typ	46 typ (F_{in}=2.4 MHz)
Motorola	MC10319	8	25 max	±1 LSB max	±¼ LSB typ ±1 LSB max	1° typ	1% typ	NS
	MC10321	7	25 max	±1 LSB max	±¼ LSB typ ±1 LSB max	2° typ	2% typ	NS
National Semiconductor	ADC0881	8	20 max	0.2% FS max	0.2% FS max	0.5° typ 1° max	1% typ 2% max	45 dB min (F_{in}=1.248 MHz)
	ADC0882	8	20 max	0.2% FS max	0.2% FS max	0.3° typ 1° max	0.7% typ 2% max	45 dB (F_{in}=1.248 MHz)
NEC Electronics	μPC659	8	20 max	±0.5 LSB max	±1.5 LSB max	0.8° typ 3° max	1.5% typ 3% max	NS
Philips Components-Signetics	TDA8703	8	40 min	±0.25 LSB typ	±0.4 LSB typ	0.8° typ	0.6% typ	7.1 effective bits (F_{in}=4.43 MHz)
	TDA8708/09	8	30 min	±0.3 LSB typ	±0.5 LSB typ	2° typ	2% typ	60 dB min (F_{in}=5 MHz)
	TDA8713	8	30 min	±0.25 LSB typ ±0.5 LSB max	±0.4 LSB typ ±1 LSB max	0.8° typ 1.5° max	0.6% typ 2% max	7.1 effective bits typ (F_{in}=4.43 MHz)
	TDA8715	8	50 min	±0.25 LSB typ ±0.25 LSB max	±0.4 LSB typ ±0.75 LSB max	0.4° typ 1.5° max	0.3% typ 2% max	7.2 effective bits typ (F_{in}=4.43 MHz)
Plessey Semiconductors	SP94308	8	20 min	±¾ LSB typ	±1 LSB max	1° typ	1.5% max	NS
	SP973T8	8	30 min	±½ LSB max	±1 LSB max	1° max	1% max	NS
Samsung Semiconductor	KAD0206	6	20 max	±0.8% max	±0.8% max	2° max	2% max	NS
	KSV3110	8	20 min	±0.2% typ	±0.8% typ	2° max	3% max	42 dB (F_{in}=1.02 MHz)
	KSV3208	8	20 min	±0.2% typ	±0.8% typ	2° max	2% max	40 dB min (F_{in}=1 MHz)
Siemens Components	SDA 5200	6	50 min	±¼ LSB max	±½ LSB max	NS	NS	NS
	SDA 8010	8	100 min	±0.5 LSB max	±0.6 LSB max	NS	NS	43 dB typ (F_{in}=30 MHz)
Sipex	SP1070	8	30 max 25 min	±¾ LSB max	±1 LSB max	1° typ	1% typ	44 dB min (F_{in}=2.234 MHz)
	SP1072	8	25 max	±1 LSB max	±1 LSB max	1° typ	1% typ	40 dB min (F_{in}=1.1 MHz)
	SP1078	8	60 max	±¾ LSB max	±1 LSB max	NS	NS	45 dB typ (F_{in}=2.234 MHz)

Notes: Specifications cover commercial temperature ranges.
NA=not applicable *DDIP=double-wide DIP †FSR=full scale range
NS=not specified **TDIP=triple-wide DIP

Input-voltage range (V)	Power dissipation (W)	Power supply (V)	Packages	Price (100s)	Comments
0 to 1; 0 to −1, ±1	0.858	5, −5.2	24-pin DDIP	$144	Includes full flash converter, reference, amplifiers, buffer, and input termination resistor. Competes with THC 1068.
±1	1.43	5, −4.5	24-pin DDIP	$70	Second source for Siemens SDA 8010.
±1	0.65	5, −5.2	16-pin DIP	$39	Full flash architecture. Second source for AD9000.
1.2 to $5V_{p-p}$	0.055 typ	4 to 6	28-pin DIP, 28-pin SOIC	$13	Full flash CMOS architecture. Programmable input range.
1 to $5V_{p-p}$	0.035 max	4 to 6	18-pin DIP, 18-pin SOIC	$6.61	Full flash CMOS architecture. Programmable input range.
1.2 to $5V_{p-p}$	0.05 typ	5	24-pin DIP, 24-pin SOIC	$8.90	Full flash CMOS architecture. Programmable input range.
1 to $2V_{p-p}$	0.618 typ	±5	24-pin DIP, 24-pin SOIC	$19	Wide tolerance on −5 supply. Full flash architecture.
−2.1 to 2.1	0.459 typ 0.668 max	±5	20-pin DIP, 20-pin SOIC	$7	Wide tolerance on −5 supply. Full flash architecture.
3 to 5	0.6	5	28-pin DIP, 28-lead plastic leaded chip carrier	$10 $8.50	Result of cross-licensing agreement with TRW LSI Products. Direct replacement for TDC1058. Full flash architecture.
0 to −2	0.7	±5	28-pin DIP, 28-lead plastic leaded chip carrier	$14 $12.75	Result of cross-licensing agreement with TRW LSI Products. Direct replacement for TDC1038. Full flash architecture.
$1V_{p-p}$	0.395 typ	5	24-pin SOIC	$12.10	2-step flash architecture. Includes clamping, S/H, and reference-generating circuits.
1	0.3	5	24-pin DIP, 24-pin SOIC	$8.16	Folding and interpolating architecture.
1	0.36	5	28-pin DIP, 28-pin SOIC	$18.93	Includes 1-out-of-3 input selector, video amplifier with clamp and external gain control. TDA8709 is for chrominance inputs in S/VHS applications.
1	0.29 typ 0.415 max	5	24-pin DIP, 24-pin SOIC	$24	All digital inputs and outputs are TTL compatible.
1	0.325 typ 0.425 max	5	24-pin DIP	$80	All digital inputs and outputs are ECL compatible.
$1V_{p-p}$	0.75 typ	±5	28-pin DIP	$9.68	6-MHz min analog bandwidth. Buffer and amplifier with an internal gain of 2.
$2V_{p-p}$	0.55 typ	5	18-pin DIP	$12.61	70-MHz, 3-dB typical bandwidth. Internal bandgap reference.
2.6 to 5	0.4 typ	5	32-pin SOIC	$8	Three different internal clamping functions. Internal 3.7 and 2.7V references.
0 to 2	0.55	±5	40-pin DIP	$27 to $35	Combines 8-bit A/D converter with a 7-, 8-, 9-, or 10-bit D/A converter.
0 to V_{ref}	0.88 typ	±5	28-pin DIP	$22	Includes reference, preamplifier, and input clamping circuit. Essentially the 8-bit converter section of the KSV3110.
−3 to 2	0.55 typ	5, −5.2	16-pin DIP	$50.16	Full flash architecture. ECL compatible.
±1	1.3 typ	5, −4.5	24-pin DIP	$100.68	Full flash architecture. ECL compatible. Wide large-signal bandwidth.
0.741, 1, 1.25, or 2.5	0.965 typ	5, −5.2	28-pin DIP	$190	Includes input amplifier, full-scale-range amplifier, 2.5V reference. Input amplifier is dc stabilized to overcome dc drift and warm-up problems. Pin-selectable RS170/RS343 gains.
±6 max	2.6 typ	±12, ±5	42-pin DDIP	$580	Dual flash ADCs with separate input buffer and limiter for each channel.
0 to 1, ±0.5, 0 to −1	0.561 typ	5, −5.2	24-pin DIP	$167	Hybrid package includes input amplifier and 2.5V reference.

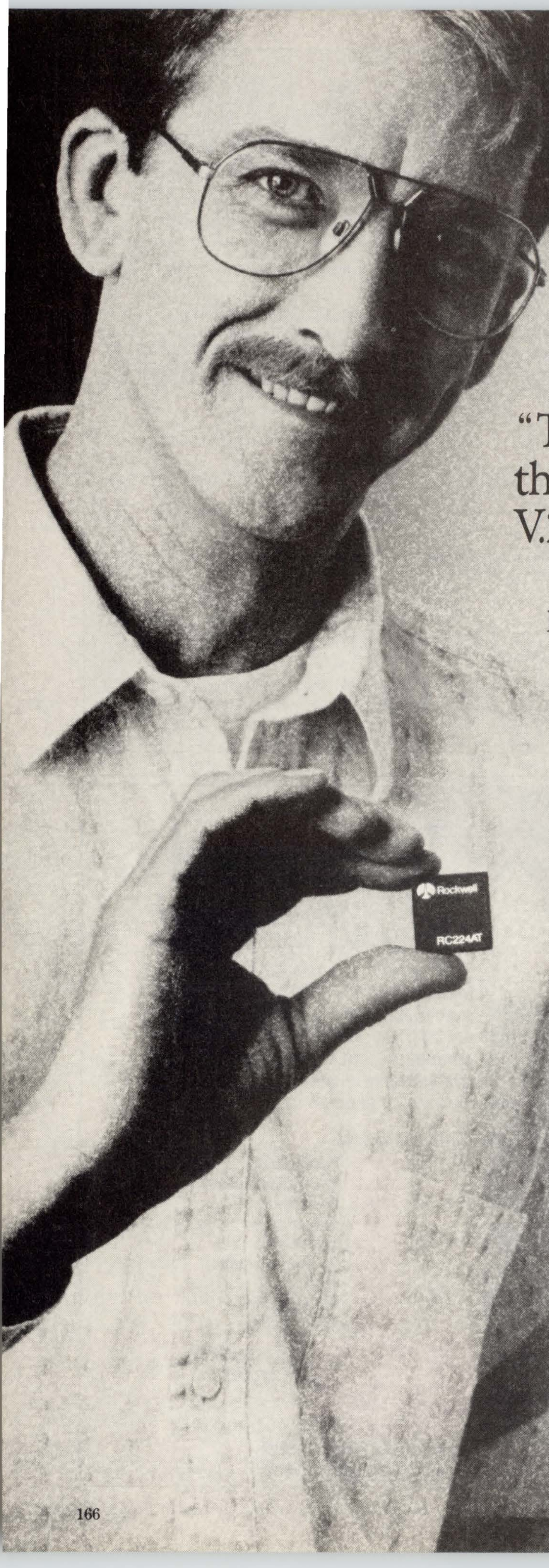
Table continued

Table 1—Representative video A/D converters *(continued)*

Manufacturer	Part n	Resolution (bits)	Maximum sampling rate (M samples/sec)	Differential linearity	Integral linearity	Differential phase	Differential gain	S/N ratio
Sony	CXA1016P/K CXA1056P/K	8	30 min 50 min	±½ LSB max	±½ LSB max	0.5° max	1.5% max	NS
	CXA1296P	8	20 min	±½ LSB max	±½ LSB max	0.5° max	1.5% max	45 dB (F_{in} =5 MHz)
	CXD1175AP/AM	8	35 typ	±½ LSB	+1.5/−1.0	0.7° typ	1% typ	41 dB (F_{in} =5 MHz)
	CX20220A-1 A-2	10 9	20 min	±1 LSB max ±1 LSB max	±1 LSB max ±½ LSB max	0.3° typ 0.5° typ	0.7% typ 1% typ	NS
Teledyne Components	4194	10	30 max	10-bit monotonic at 30 MHz	0.05% FSR† typ	NS	NS	NS
TRW LSI Products	TDC1020	10	20 min 25 typ	½ LSB typ 1 LSB max	½ LSB typ 1 LSB max	0.5° typ	1% max	55 dB typ (F_{in} =5 MHz)
	TDC1038	8	20 min	½ LSB max	½ LSB max	0.3° typ 1° max	0.7% typ 2% max	45 dB min (F_{in} =1.248 MHz)
	TDC1048	8	20 min	½ LSB max	½ LSB max	1° max	2% max	45 dB min (F_{in} =1.248 MHz)
	TDC1049	9	30 min	½ LSB max	½ LSB max	0.5° max	1% max	48 dB min (F_{in} =1.25 MHz)
	TDC1058	8	20 min	½ LSB max	½ LSB max	0.5° typ 1° max	1% typ 2% max	45 dB min (F_{in} =1.248 MHz)
	TDC1068	8	25 min	½ LSB max	½ LSB max	1° max	2% max	40 dB min (F_{in} =2.438 MHz)

Notes: Specifications cover commercial temperature ranges.
NA=not applicable *DDIP=double-wide DIP †FSR=full scale range NS=not specified **TDIP=triple-wide DIP

Input-voltage range (V)	Power dissipation (W)	Power supply (V)	Packages	Price (100s)	Comments
0 to −2	0.42 typ 0.55 typ	−5.2	28-pin DIP 44-pin LCC	$24.90/$49 $46/$69	30- and 50-MHz input bandwidths. Full flash architecture.
0 to −2	0.4 typ	5 or ±5	28-pin DIP	$15.90	Full flash conversion technique. Pin replaceable with TDC1048.
1.8 to 5V_{p-p}	0.09 typ	5	24-pin DIP/ 24-pin SOIC	$17.20/ $18	Half flash conversion technique. Low-power CMOS.
0 to −2	0.36 typ	−5	28-pin DIP	$100 $49.50	Subranging architecture, requires external S/H amplifier. Digital inputs and outputs are ECL compatible.
2.048	14 typ	±15, ±5	5×6-in. pc board	$2050	Operates in single-shot mode with single pulse convert command. Dual 6-bit flash architecture. Internal T/H amplifier.
+2 to −2	5 typ	5, −5.2	64-pin DIP, 68-pin pin-grid array	$98	Full flash architecture. Selectable output formats. Available in complete system in THC1070.
0 to −2	0.7 typ	5, −5.2	28-pin DIP, 28-lead plastic leaded chip carrier	$12.75	Drop-in replacement for TDC1048 with lower power and selectable output formats.
0 to −2	0.95 typ 1.95 max	5, −5.2	28-pin DIP, chip carrier	$23	Industry-standard video ADC since 1983. Selectable output formats.
0 to −2	3.5 typ	−5.2	64-pin DIP, 68-contact chip carrier, 68-pin pin-grid array	$94	Only 9-bit ADC available. Also internal to TDC1069.
3 to 5	0.575 typ	5	28-pin DIP, 28-lead plastic leaded chip carrier	$8.50	Next generation of TDC1048 with single supply and low cost. 60-MHz input bandwidth.
1V_{p-p}	1.6 typ	5, −5.2	24-pin DIP	$73	Complete ADC system with input buffer, 3-state output register, and reference.



Communication solutions from Rockwell.

The assignment was demanding. The integral modem for the company's new Laptop would have to be compact and inexpensive. With the complete '88 AT command set, plus the lowest possible power consumption.

"The features they packed into the world's first single-device V.22bis modem blew us away."

Fortunately, the engineers already know who to call: Rockwell International. They're aware that no matter what the application, Rockwell's new V.22bis family provides capabilities nobody else can supply.

They've read how Rockwell stunned the industry with its RC224AT—the world's first fully integrated single-device modem solution. And how this one compact component offers CCITT V.22bis and V.22, as well as Bell 212A and 103 compliance, plus value-added features such as power-saving Automatic Sleep Mode. Not to mention the assurance of a five-year warranty.

Their call to Rockwell also reveals how the V.22bis family can help with future projects. They learn about the capabilities of Rockwell's RC2324DP chip set.

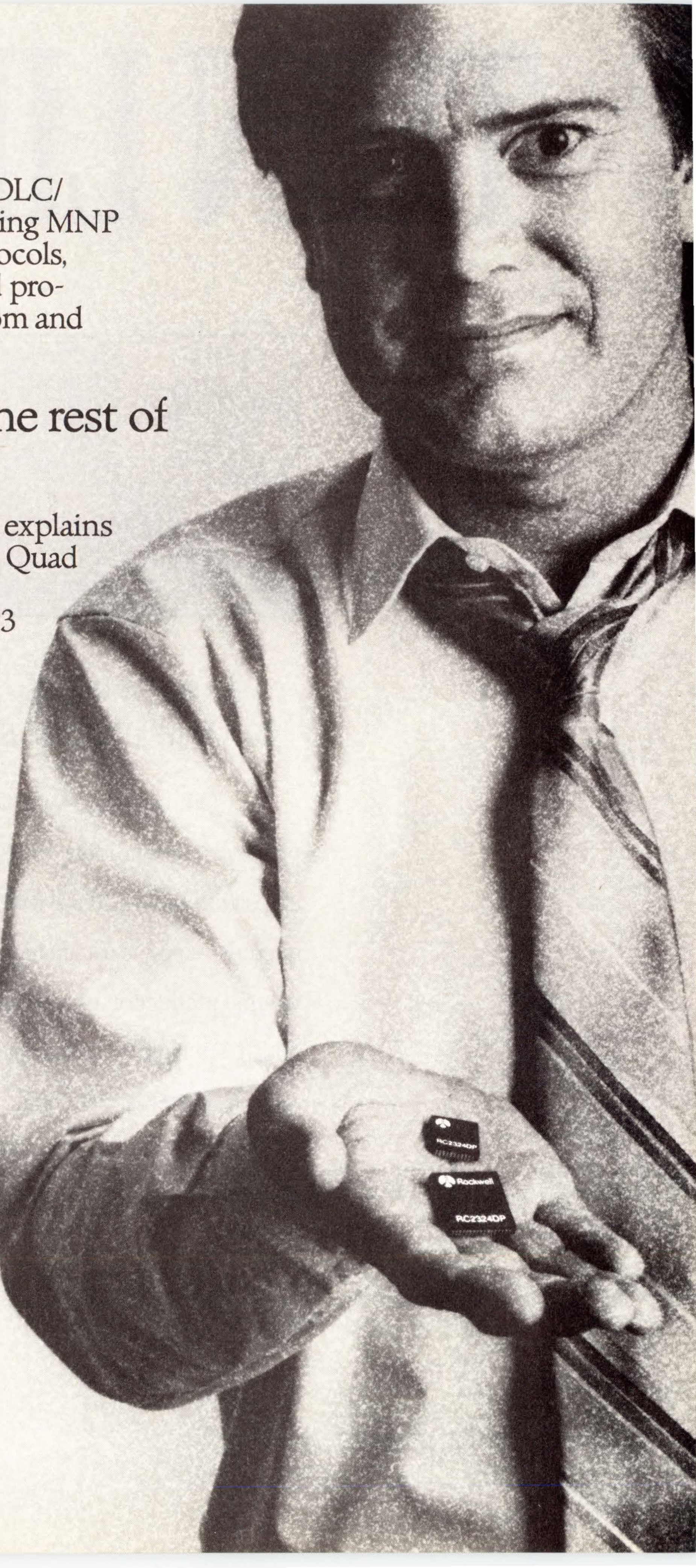
They hear how it provides HDLC/SDLC framing for implementing MNP 5™, X.25, LAPM and V.42 protocols, while offering unprecedented programming flexibility for custom and country-specific applications.

"And then we met the rest of the family."

A Rockwell technical advisor explains that it's the only chip set with Quad capability that meets CCITT V.22bis, V.22A/B, V.21 and V.23 requirements, as well as Bell 212A and 103 standards. He adds that the RC2324SME offers capabilities optimized for Europe, including MNP 5™ and V.25bis.

In no time, the Laptop project is ready for production. To management, the results—as well as the engineers responsible—couldn't look better.

Call the leader in modem technology. Rockwell *is* solutions.



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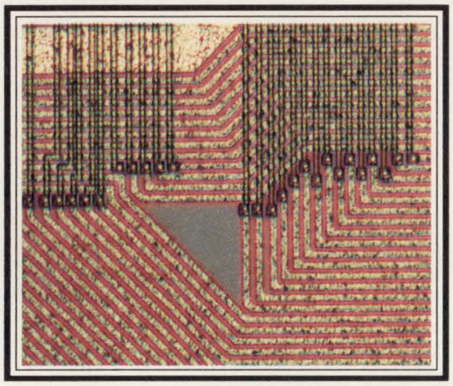
CIRCLE NO. 93

THIN LINES.



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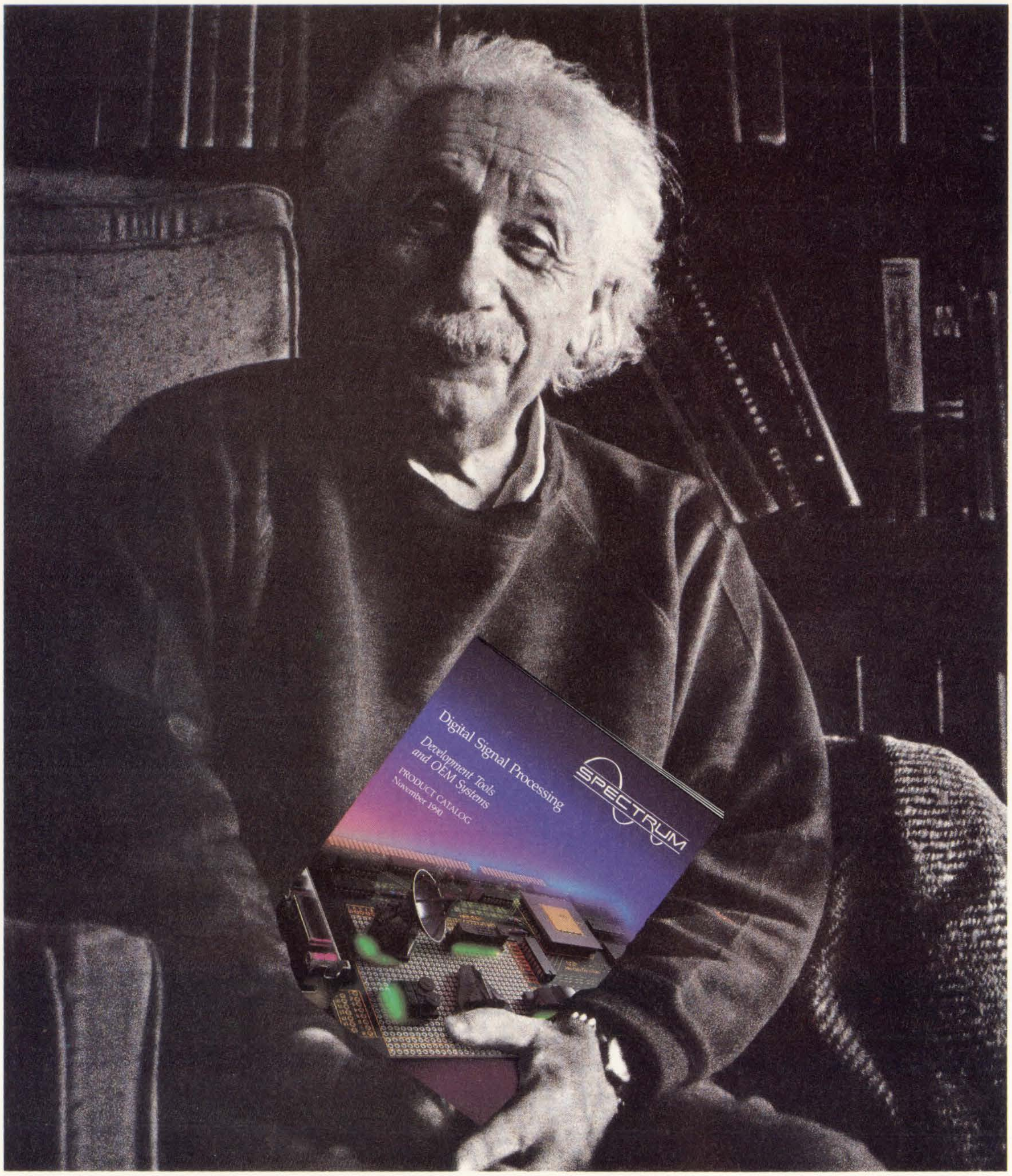

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EDN'S DSP-CHIP DIRECTORY

DSP μPs continue to become faster, cheaper, and more abundant. The recent availability of high-quality software tools eases debugging and maintaining your software today. And soon, parallel processing will let you achieve supercomputer performance.

David Shear, *Contributing Editor*

After years of being specialized curiosities, digital-signal-processor chips (DSP μPs) are finding their way into high-volume applications such as high-speed modems and digital cellular telephones. Every day, designers develop new applications for DSP chips. Adaptive servo controllers, speech-recognition systems, image systems, refrigerators, and robots are just some of the products that use them. Automobiles are beginning to use DSP chips for engine control, active suspension systems, and noise cancellation.

Paralleling the μP market

Close parallels exist between the history of the μP and that of the DSP chip. At first, there were many μPs looking for problems to solve. After that, the market split into small low-cost microcontrollers and high-end μPs.

The DSP-chip market has split in a similar fashion into high-volume, low-cost, 16-bit fixed-point chips and low-volume, high-end, parallel-processing floating-point chips. In the μP market, there was a shakeout, leaving only a few vendors. The DSP market is beginning to follow this path. Fujitsu is one of the most recent manufacturers to drop out of the DSP market. In fact, the DSP market is maturing to the point where the high-volume applications are defining the design of the chips.

Many applications now require DSP chips. Telecommunications equipment, high-speed modems, automobile-engine controllers, digital cellular telephones, and even refrigerators. In Japan, cramped living quarters sometimes force people to sleep close to the kitchen and, thus, the refrigerator. A DSP chip helps reduce the noise of the refrigerator's compressor via active noise cancellation.

When floating-point DSP μPs first came out, many people thought that designers would mostly use them when they were too lazy to use fixed-point chips or had insufficient time to create a fixed-point design. Using a fixed-point DSP chip is always more difficult than using a floating-point DSP chip because the programmer must contend with scaling.

Designers ended up using the floating-point DSP chips for high performance—especially in applications that required the power of parallel processing. Although some applications use a single floating-point DSP chip, single-chip designs often aren't fast enough. Multiple floating-point DSP μPs are used in many high-end applications such as graphics and imaging systems.

In fact, a growing market exists for high-speed floating-point DSP μPs with architectures that suit them for parallel processing, but few such chips exist. Texas Instruments' C30 floating-point DSP chip has some interchip communications capabilities. Motorola's 96002 has two expansion buses on the chip for nearly glueless connection of multiple DSP μPs in a linear array.

Texas Instruments' specifically designed the C40 floating-point DSP μP for parallel processing. The idea for the chip came about when Ray Simar, principal architect of TI's C30 family, observed that few applications used only a single C30. His coworkers also found few such applications. The C40 resulted from their observations. This floating-point DSP chip is an example of things to come. It performs 32-bit floating-point operations in 40 nsec, has 13 32-bit internal buses, and two complete 32-bit external buses. What really sets the C40 apart from other DSP μPs is a 6-channel DMA controller and six 32-bit communications ports that connect directly to other C40s without external logic. These 13M-byte/sec communications ports let you configure the C40 into large arrays without external logic.

You'll see more external buses

As DSP μPs get faster, you must transfer data into and out of them faster. If you can't get data transferred in and out of a fast DSP chip, you won't be able to

A growing market exists for high-speed floating-point DSP μPs with architectures that suit them for parallel processing, but few such chips exist.

realize the performance the chip has to offer. It is critical that the data-transfer speed be fast enough to keep the DSP working instead of waiting.

Dual buses will become more prevalent. With dual buses you can access two external memories at the same time. Motorola's 96002 and TI's C40 have two complete 32-bit external buses. Motorola's first floating-point DSP chips were the 96001 and the 96002. The 96001 was very much like a floating-point version of the 56001 fixed-point DSP chip but with a single external bus. The dual-bus 96002 excited a larger market than the now moth-balled 96001.

The format of floating-point numbers has been somewhat controversial. Motorola and Zoran say that it is essential for a chip's format to comply with the IEEE-754 floating-point standard. AT&T, NEC Electronics, Oki Semiconductor, and Texas Instruments agree that the format inside the DSP is not important. AT&T and TI have single cycle instructions to convert to and from the IEEE-754 format for those applications that require IEEE compliance.

Today's high-end is tomorrow's necessity

Multiple floating-point DSP μPs will not always be used only in high-end applications. A few years ago, a single 16-bit fixed-point DSP μP would have been too expensive to be used in a desktop PC. These DSP μPs are now less than $5 and have invaded desktop PCs in the form of modems and other specialized products. Parallel processing with multiple floating-point DSP μPs will follow this same path. In a few years, PC applications will require the performance these devices provide and by then floating-point DSP chips will be cheap enough to fill the need.

Fixed-point DSP μPs are far from dead. Just like microcomputers, they will always be in demand for such applications as telecommunications equipment, modems, and toys. Sixteen-bit fixed-point devices have such a high volume potential that Motorola—long a proponent of the 24-bit word length—will soon introduce a 16-bit DSP-μP family.

Manufacturers are keeping the older 16-bit fixed-point DSP μPs alive by surrounding the original DSP-μP core with a variety of peripheral and memory options. Even analog-to-digital and digital-to-analog converters (ADC/DAC) are being integrated on these DSP chips. Analog Devices, AT&T, and Oki all have an ADC/DAC on these DSP chips.

The 16-bit ADC/DAC on Analog Devices' ADSP21msp50 is specified in the data sheet to have a 65-dB S/N ratio. This spec seems disappointing because 16-bit ADCs can often approach a 96-dB S/N ratio. However, the 65-dB S/N ratio is not a limitation of the technology. Analog Devices says that it has specified 65 dB because that is the requirement of the high-volume telecommunications application the device was designed for. The company expects to see a S/N ratio of about 96-dB when it fully characterizes the part.

The 24-bit fixed-point DSP μPs are well suited to the digital audio market. In fact, that may be the only market for them—at least Texas Instruments thinks so. The company has a 24-bit fixed-point device, the TMS57000, that is not available to the general public. They sell it on a custom basis and feel they know all of the potential customers in the digital audio market so they haven't bothered to release it.

Consider the support tools

You aren't just buying silicon when you select a DSP chip—you also have to consider the chip's support tools. Almost all DSP μPs have an assembler and a simulator. Some have C compilers and source-level debuggers. All have some sort of hardware support, and many DSP chips have in-circuit-emulation circuitry.

The C compilers aren't yet intended for the DSP section of the code. They are intended for the code

Index to DSP μPs included in this directory

Supplier	Device	Type	Page
Analog Devices	2100 family	16-bit fixed point	174
AT&T	DSP16/16A/16C DSP32C	16-bit fixed point 32-floating point	175 188
Motorola	DSP56001 DSP96002	24-bit fixed point 32-floating point	176 193
NEC Electronics	μPD77C25 μPD77220 μPD77230/240	16-bit fixed point 24-bit fixed point 32-floating point	179 180 194
Oki Semiconductor	MSM699210/215	32-floating point	197
SGS-Thomson	ST18 family	16-bit fixed point	183
Texas Instruments	TSM320C1X TSM320C2X/5X TSM320C3X TSM320C40	16-bit fixed point 16-bit fixed point 32-floating point 32-floating point	184 187 198 201
Zoran	ZR34325	32-floating point	202

that describes control and management tasks—code that may be large in size but is rarely run. You still program the repetitive DSP tasks in assembly language. Some C compilers attempt to optimize the resulting code. The degree of optimization is not yet sufficient to allow a program to be completely written in C.

Some companies are attempting to make C more efficient for DSP applications. Analog Devices is proposing some extensions to C. Called DSP/C, this version of C would make C a vector language instead of a scalar language, as it is now. However, advances in high-level languages will not significantly affect the way you program DSP μPs within the next year.

Source-level debuggers are now available

Source-level debuggers are bringing DSP-chip software debugging out of the dark ages. Now you can watch your program run instead of watching the DSP chip execute instructions. Some of the source-level debuggers show you both the high-level-language source code and the assembly-language instructions that correspond to it.

Designing an in-circuit-emulation probe that can run at the high speed of the newest DSP chips is difficult. The most advanced DSP μPs have moved much of the in-circuit-emulation circuitry on the chip. Motorola's 96002 and TI's C30 have a serial port that provides access to in-circuit-emulation functions. TI has taken this approach further by including an analysis module that you can access via a JTAG interface on its C40. This feature lets you string many C40s together and effectively have a parallel-processing in-circuit emulator because events in one C40 can control other C40s. For example, you can have a breakpoint in one C40 halt other C40s.

The next major step in the evolution of electronics is making systems that can see, talk, and listen; comprehend this information; and then act accordingly in real time. The required computing power for such systems is enormous. An array of DSP μPs operating in parallel is well suited to these tasks. Furthermore, you can easily partition many DSP algorithms into parallel processes, which will make programming these complex systems manageable. As prices continue to drop, look for more DSP μPs to take on parallel-processing applications and eventually change the way you design systems. EDN

Article Interest Quotient (Circle One)
High 494 Medium 495 Low 496

Key to abbreviations used in block diagrams

AB—combined program and data address bus
ACC—accumulator
ADC/DAC—analog to digital and digital to analog converter
ADDR GEN—address generator
ALU-arithmetic logic unit
BIT MANIP—bit manipulation
BS—barrel shifter
CDB—control data bus
CM—cache memory
CPUB—CPU bus
DAB—data address bus
DB—combined program and data bus
DDB—data data bus
DM—memory for data only
DMAAB—DMA address bus
DMADB—DMA data bus
DMAC—direct memory access controller
FX—fixed-point
FP—floating-point
GDB—global data bus
HOST INTER—host interface
IDB—instruction data bus
INT—external interrupt
MAC—multiplier accumulator
MULT—multiplier
PAB—program address bus
PDB—program data bus
P/DM—memory for program and data
PIO—parallel I/O
PM—memory for program only
PPCP—parallel processor communications port
PRAB—peripheral address bus
PRDB—peripheral data bus
REG—register
REGB—register bus
SIO—serial I/O
TIM—timer
XAB—external address bus
XDB—external data bus
XDAB—external data address bus
XDDB—external data data bus
XIOAB—external I/O address bus
XIODB—external I/O data bus
XPAB—external program address bus
XPDB—external program data bus

2100 FAMILY

16-BIT FIXED-POINT CMOS DSP μP

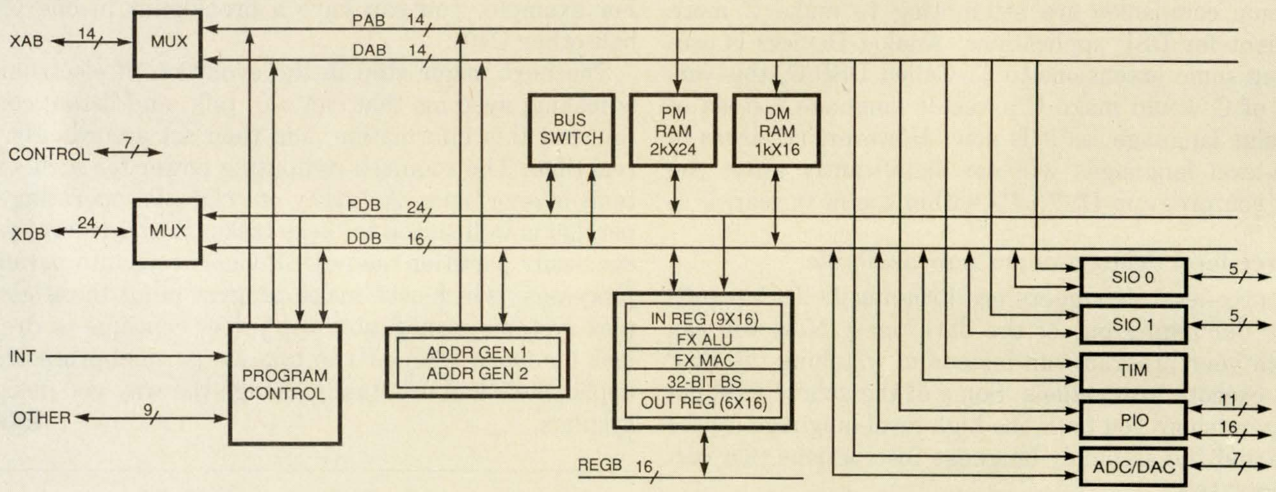
AVAILABILITY: The ADSP2100, -2101, and -2102 are in production now. The 2105 and 2111 are sampling now. The 21msp50 is scheduled to begin sampling this month.

COST: The 2100 costs $49; the 2101, $43; the 2102, $49; the 2105, $9.90; the 2111, $56; and the 21msp50, $70 (1000).

SECOND SOURCE: None.

Analog Devices Inc
1 Technology Way
Norwood, MA 02062
(617) 461-3074
Circle No. 674

DESCRIPTION: The ADSP2100 family offers a wide variety of options, ranging from the 2100 without any on-chip memory to the 21msp50 with program and data RAM and peripherals, including an analog-to-digital and digital-to-analog converter, on chip. The data memory has a 16-bit width, but the program memory has a 24-bit word width to control the parallel operations. A 32-bit floating-point version, the 21000, is in the works and will be based on the architecture of the 2100 family.



FEATURES: 62.5-, 80-, and 100-nsec cycle-time versions.
Separate on-chip program and data buses. On-chip memory: The 2100 has no on-chip memory. The 2101 has a 2k×24-bit program RAM and a 1k×16-bit data RAM. The 2102 has a 2k×24-bit program ROM or RAM and a 1k×16-bit data RAM. The 2105 has a 1k×24-bit program RAM and a 512×16-bit data RAM. The 2111 and 21msp50 have a 2k×24-bit program RAM and a 1k×16-bit data RAM.
Separate program and data buses brought off the chip only on the 2100.
The 2101, 2105, 2111, and 21msp50 combine program and data buses off the chip.
Off-chip memory capacity: The 2100 has 32k×24-bit program and 16k×16-bit data memory capacities. All others have 16k×24-bit program and 16k×16-bit data memory capacities.
Boot memory controller loads program from external byte-wide EPROM.
On-chip peripherals: The 2100 has no on-chip peripherals. The 2101 and 2102 have two serial I/O ports; the 2105 has one serial I/O port. The 2111 has two serial I/O ports and a parallel I/O port. The 21msp50 has two serial I/O ports, a parallel I/O port, and a 16-bit ADC/DAC.
Multiplier/accumulator accepts 16-bit fixed-point input and creates 32-bit fixed-point results within a 40-bit accumulator. 16-bit ALU. 32-bit bidirectional barrel shifter. 40-bit accumulator.
Multiplier/accumulator, ALU, and shifter are separate blocks connected by the 16-bit R-bus and the data bus.
Zero-overhead looping.
Only the 2100 has a 16×24-bit on-chip cache.
Direct, indirect, immediate, circular, and bit-reversal addressing modes.
Two address generators.
No on-chip DMA. Serial port has auto buffer, which transparently transfers data to and from memory.
16-level hardware stack. Status stack limits interrupts to four levels of nesting on the 2100, seven levels on the others.
Four external interrupts on the 2100; three external interrupts on others.
The 2100 has only hardware wait states. Others have only software-programmable wait states.
No on-chip emulation port.
Only the 21msp50 has power-down mode to CMOS standby levels. The 2101, 2105, and 2111 have an idle mode, which lowers power until an interrupt is detected.
Packaging: 2100, 100-pin plastic quad flatpack and 100-pin PGA. 2101, 68-pin PGA and 68-pin PLCC. 2102, 68-pin PGA and 68-pin PLCC. 2105, 68-pin PLCC. 2111, 100-pin plastic quad flatpack and 100-pin PGA. 21msp50, 100- and 132-pin plastic quad flatpacks.

HARDWARE — SUPPORT — SOFTWARE

In-circuit emulator. Low-cost in-circuit emulator board.
Demo board.
Third-party support: Contact Analog Devices for a list of third-party vendors.

C compiler. Simulator.
Macroassembler/linker.
Application libraries.
Upcoming DSP/C will enhance C for DSP applications.

16-BIT FIXED-POINT CMOS DSP μP

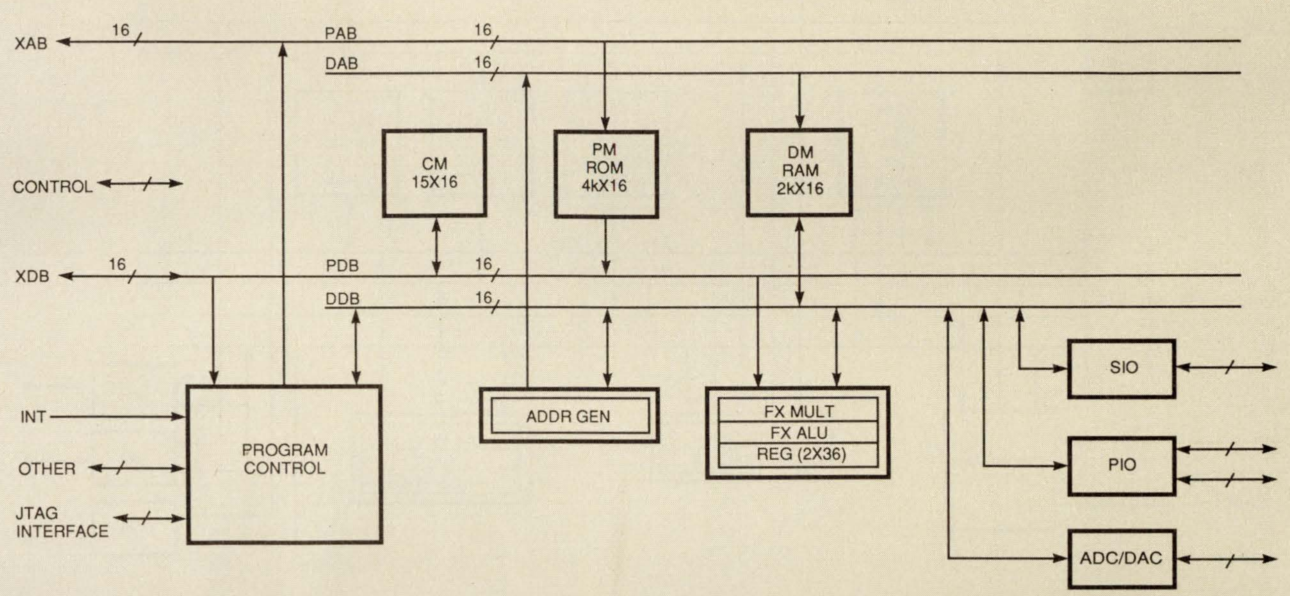
AVAILABILITY: The DSP16 and -16A are in production. The DSP16C is sampling, production is scheduled for the end of 1990.

COST: The DSP16 costs $9.60; the DSP16A costs $16.70 (10,000).

SECOND SOURCE: None.

AT&T Microelectronics
Dept 52AL300240
555 Union Blvd
Allentown, PA 18103
(800) 372-2447;
in Canada, (800) 553-2448
Circle No. 675

DESCRIPTION: The members of the DSP16 family have long been the fastest fixed-point DSP chips. The DSP16A has a 25-nsec cycle time. The DSP16A and DSP16C also have the largest on-chip program memory at 12k × 16 bits. Many applications that would require external ROMs with other DSP chips can fit within the DSP16 family's on-chip memory. The DSP16C has an analog-to-digital and a digital-to-analog converter on chip. The DSP16C also has a 4-pin JTAG interface, which assists in testing tightly packed boards. A 3.3V version of the DSP16A is available.



FEATURES: 25-, 33-, 55-, and 75-nsec cycle-time versions.
The DSP16C has 38.5- and 76.9-nsec cycle-time versions.
Separate on-chip program and data buses.
On-chip memory: The DSP16 has a 2k × 16-bit program ROM and a 512 × 16-bit data RAM. The DSP16A and -16C have a 12k × 16-bit program ROM and a 2k × 16-bit data RAM.
The program ROM on the DSP16 can be replaced with as much as 64k words of external memory.
The program ROM on the DSP16A and -16C can be replaced or augmented with as much as 64k words of external memory.
No direct off-chip data memory expansion.
Parallel and serial I/O port.
The DSP16C has an on-chip CODEC.
The multiplier accepts 16-bit fixed-point data and creates 32-bit fixed-point results within a 36-bit accumulator.
32-bit ALU.
No barrel shifter.
Two 36-bit accumulators.
Zero-overhead cache looping as many as 127 times.
15-word instruction cache.
Immediate, register-indirect, and circular addressing modes.
No on-chip DMA.
Single-level hardware stack is software expandable into main memory.
One external interrupt.
No wait states.
No on-chip emulation port.
The DSP16A and -16C have power-down mode.
Packaging: DSP16 and -16A, 84-pin PLCC or 133-pin PGA. DSP16C, 100-pin plastic quad flatpack.

HARDWARE — SUPPORT — SOFTWARE

Hardware:
Development system with in-circuit emulation.
Evaluation board that plugs into a PC.

Software:
Assembler/linker.
Simulator.
Application library.
Third-party support includes filter-design packages. Contact AT&T for a list of third-party vendors.

DSP56001

24-BIT FIXED-POINT CMOS DSP µP

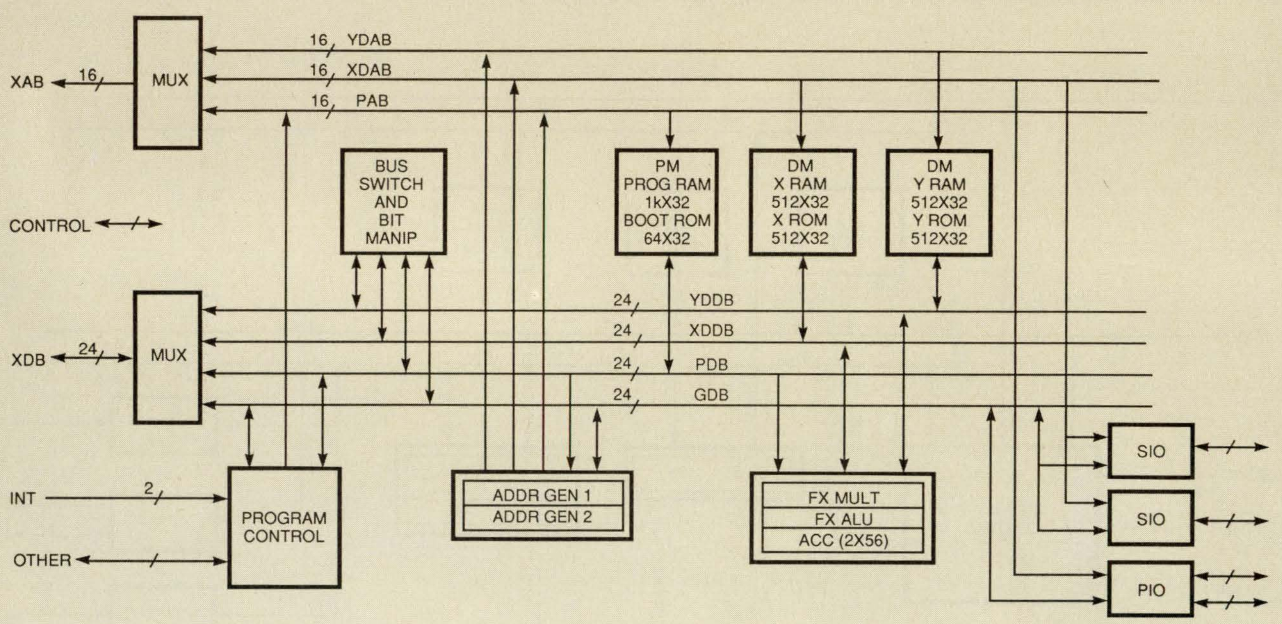
AVAILABILITY: Now.

COST: $56.

SECOND SOURCE: None.

Motorola Inc
Microprocessor Products Group
6501 William Cannon Dr
Austin, TX 78735
(512) 891-2030
Circle No. 676

DESCRIPTION: The 56001 provides a 24-bit data word and two 56-bit accumulators. This extended precision lets the chip process 16-bit data more easily than the 16-bit machines can. A 24-bit word width eases scaling, and the 56-bit accumulators prevent overflow. The 24-bit data width suits digital audio applications. The manufacturer will soon introduce a 16-bit version with an architecture similar to that of the 56001.



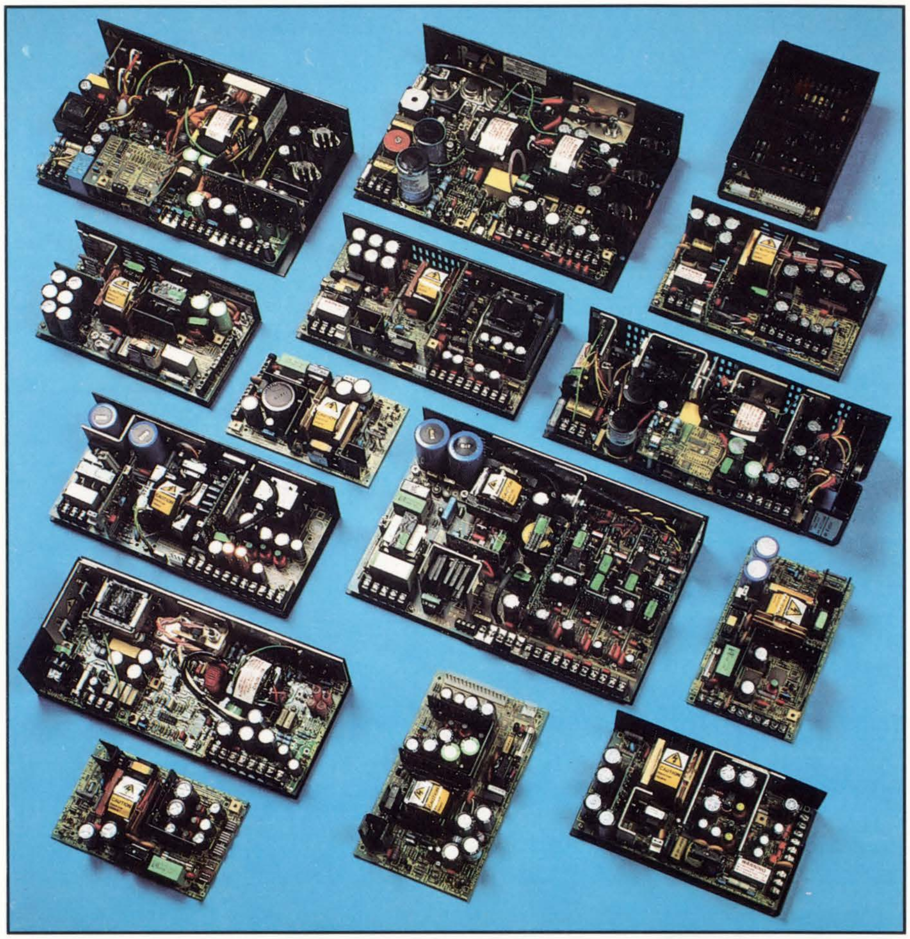
FEATURES: 74- and 97-nsec cycle-time versions.
Three address buses and four data buses.
Separate address buses for program ROM and the two data RAMs.
Separate data buses for program ROM, the two data RAMs, and global data.
On-chip memory includes a 512×24-bit program RAM, a 32×24-bit boot ROM, dual 256×24-bit data RAMs, and dual 256×24-bit data ROMs.
ROM-based version (56000) available.
Three separate memory spaces (X, Y, and P). Each can address 64k×24-bit locations.
Asynchronous 8-bit serial I/O port.
Synchronous 8- to 24-bit serial interface.
Parallel port can interface with a host µP.
Multiplier accepts 24-bit data and returns 48-bit results to 56-bit accumulator.
ALU performs arithmetic operations on 56-bit data and logical operations on 24-bit data.
No barrel shifter.
Two 56-bit accumulators.
Zero-overhead looping.
Immediate, direct, indirect, circular, and bit-reversed addressing modes.
Two address generators.
No DMA support.
System stack is 15 levels deep but can be read by program to extend stack into main memory.
Two external vectored interrupts.
Hardware and software-programmable wait states.
No on-chip emulation.
Low-power mode.
Packaged in a 132-pin ceramic quad flatpack or 88-pin PGA.

HARDWARE — SUPPORT — SOFTWARE

Hardware:
Application development system includes in-circuit emulator.
Contact Motorola for a list of third-party vendors.

Software:
C compiler.
Macro cross assembler.
Linker/librarian.
Simulator.
Code translator from TMS320C10 to 56001.
Third-party support includes filter-design software.

NEW.
Open frame, "N" Range switch mode power supplies from Farnell Advance.



The Farnell "N" Range of open frame, 50 to 500-watt, switch mode power supplies offers electronic designers a wide choice of single and multiple output units, featuring technically superior designs and the highest standards of production quality. Refer to the listing of available standard models and contact Farnell Advance, 32111 Aurora Rd., Solon, OH 44139 for specifications.

PHONE: (216) 349-0755.
FAX: (216) 349-0142.

FCC

FARNELL ADVANCE
POWER

Output Power	Output 1	Output 2	Output 3	Output 4	Output 5	Package Options	Dimensions including covers	Model No.
50 watts	+5V 6A	+12V 1A	+24V 1A	-5V 1A	-12V 1A	2,3	*a	N50R110
multi output	+5V 6A	+15V 1A	+24V 1A	-5V 1A	-15V 1A	2,3	*a	N50R201
55 watts	5V 11A	—	—	—	—	1,3,4	b	NS055005
single output	12V 4.6A	—	—	—	—	1,3,4	b	NS055012
	15V 3.7A	—	—	—	—	1,3,4	b	NS055015
	24V 2.3A	—	—	—	—	1,3,4	b	NS055024
	30V 1.8A	—	—	—	—	1,3,4	b	NS055030
	48V 1.15A	—	—	—	—	1,3,4	b	NS055048
	56V 1A	—	—	—	—	1,3,4	b	NS055056
55 watts	100V 0.55A	—	—	—	—	1,3,4	b	NS055100
multi output	+5V 3.5A	+12V 3A(S)	-12V 1A(S)‡‡	—	—	1,3,4	b	NA055P300
	+5V 3.5A	+12V 3A(S)	+24V 1A(S)‡‡	—	—	1,3,4	b	NA055P301
	+5V 3.5A	+15V 3A(S)	-15V 1A(S)‡‡	—	—	1,3,4	b	NA055P302
	+5V 6A	+12V 3A(S)	F12V 2A(S)	F24V 1A(S)	—	1,3,4	c	NA055P400
	+5V 6A	+12V 3A(S)	F12V 2A(S)	F5V 1A(S)	—	1,3,4	c	NA055P401
	+5V 6A	+15V 3A(S)	F15V 2A(S)	F24V 1A(S)	—	1,3,4	c	NA055P403
	+5V 6A	+12V 3A(S)	F12V 1A	F12V 1A	—	1,3,4	c	NA055P413
75 watts	5V 15A	—	—	—	—	1,3,4	*d	NS075005
single output	12V 6.25A	—	—	—	—	1,3,4	*d	NS075012
	15V 5A	—	—	—	—	1,3,4	*d	NS075015
	24V 3.2A	—	—	—	—	1,3,4	*d	NS075024
	30V 2.5A	—	—	—	—	1,3,4	*d	NS075030
	48V 1.6A	—	—	—	—	1,3,4	*d	NS075048
75 watts	56V 1.4A	—	—	—	—	1,3,4	*d	NS075056
multi output	+5V 8A	+12V 3A(S)	F12V 2A(S)	—	—	1,3,4	e	NA075P300
	+5V 8A	+12V 3A(S)	F12V 2A(S)	F24V 1A	—	1,3,4	e	NA075P400
	+5V 8A	+12V 3A(S)	F12V 2A(S)	F5V 1A	—	1,3,4	e	NA075P401
	+5V 8A	+12V 3A(S)	+12V 2A(S)‡	-12V 0.5A‡	—	1,3,4	e	NA075P402
	+5V 8A	+15V 3A(S)	F15V 2A(S)	F24V 1A	—	1,3,4	e	NA075P403
	+5V 8A	+12V 3A(S)	-12V 1A‡	-5V 1A‡	—	1,3,4	e	NA075P414
90 watts	+5V 10A	+12V 5A	-12V 2A	-5V 1A	+24V 1A	2,3	*f	N90R109
multi output	+5V 10A	+15V 5A	-15V 2A	-5V 1A	+24V 1A	2,3	*f	N90R132

CIRCLE NO. 150

FARNELL ADVANCE OPEN-FRAME SWITCH MODE POWER SUPPLIES

Output Power	Output 1	Output 2	Output 3	Output 4	Output 5	Package Options	Dimensions including covers	Model No.
110 watts single output	5V 22A or 30A(FC)	—	—	—	—	2,3,4	*g	NS110005
	12V 9.2A or12.5A(FC)	—	—	—	—	2,3,4	*g	NS110012
	15V 7.5A or10A(FC)	—	—	—	—	2,3,4	*g	NS110015
	24V 4.6A or 6.25A(FC)	—	—	—	—	2,3,4	*g	NS110024
	30V 3.7A or 5A(FC)	—	—	—	—	2,3,4	*g	NS110030
	48V 2.3A or 3A(FC)	—	—	—	—	2,3,4	*g	NS110048
	56V 2A or 2.6A(FC)	—	—	—	—	2,3,4	*g	NS110056
110 watts multi output	+5V 12A	+12V 6A(S)	-12V 3A(S)‡‡	—	—	2,3,4	h	NA110P300
	+5V 12A	+15V 6A(S)	-15V 3A(S)‡‡	—	—	2,3,4	h	NA110P302
	+5V 10A	+12V 1.5A(S)‡‡	+12V 3.5A(S)	-12V 0.7A(S)‡‡	—	2,3,4	h	NQ110P400
	+5V 12A	+12V 5A(S)	-12V 2A(S)‡‡	—	+24V 2A(S)‡	2,3,4	*i	NA110P400
	+5V 12A	+12V 5A(S)	-12V 2A(S)‡‡	-5V 1A‡‡	—	2,3,4	*i	NA110P401
	+5V 12A	+12V 5A(S)	+12V 3A(S)‡‡	—	-12V 2A(S)‡	2,3,4	*i	NA110P402
	+5V 12A	+15V 5A(S)	-15V 2A(S)‡‡	—	+24V 2A(S)‡	2,3,4	*i	NA110P403
	+5V 12A	+12V 5A(S)	-12V 2A(S)‡‡	-5V 1A‡‡	+24V 2A(S)‡	2,3,4	*i	NA110P500
	+5V 12A	+12V 5A(S)	-12V 2A(S)‡‡	-5V 1A‡‡	+12V 2A(S)‡	2,3,4	*i	NA110P501
	+5V 12A	+15V 5A(S)	-15V 2A(S)‡‡	-5V 1A‡‡	+24V 2A(S)‡	2,3,4	*i	NA110P503
140 watts single output	5V 28A	—	—	—	—	2,3,4	*g	NS140005
	12V 12A	—	—	—	—	2,3,4	*g	NS140012
	15V 10A	—	—	—	—	2,3,4	*g	NS140015
	24V 6A	—	—	—	—	2,3,4	*g	NS140024
	30V 5A	—	—	—	—	2,3,4	*g	NS140030
	48V 3A	—	—	—	—	2,3,4	*g	NS140048
	56V 2.5A	—	—	—	—	2,3,4	*g	NS140056
140 watts multi output	+5V 17A	+12V 7A(Q)	F12V 3A(Q)	—	—	2,3,4	*j	NA140P300
	+5V 17A	+12V 5A(Q)	F12V 3A(Q)	F24V 3A(Q)	—	2,3,4	*j	NA140P400
	+5V 17A	+12V 5A(Q)	F12V 3A(Q)	—	F5V 1.5A	2,3,4	*j	NA140P401
	+5V 17A	+12V 5A(Q)	F12V 3A(Q)	F12V 1.5A	—	2,3,4	*j	NA140P402
	+5V 17A	+12V 5A(Q)	F12V 3A(Q)	F24V 3A(Q)	F5V 1A	2,3,4	*j	NA140P500
	+5V 17A	+12V 5A(Q)	F12V 3A(Q)	F12V 1.5A	F5V 1A	2,3,4	*j	NA140P501
	+5V 17A	+15V 5A(Q)	F15V 3A(Q)	F24V 3A(Q)	F5V 1A	2,3,4	*j	NA140P503
180 watts multi output and 48 volt D.C. input	+5V 20A	+12V 5A(S)	-12V 5A(S)	+24V 2A(S)	-5V 1A(S)	2,3,4	*k	ND180P500
	+5V 25A	+15V 1A	-15V 1A	—	—	2,3,4	*k	ND180P810
200 watts multi output	+5V 30A	+12V 7A(Q)	F12V 5A(Q)	—	—	2,3,4	*l	NA200P300
	+5V 30A	+12V 7A(Q)	F12V 5A(Q)	F24V 3A(Q)	—	2,3,4	*l	NA200P400
	+5V 30A	+12V 7A(Q)	F12V 5A(Q)	—	F5V 1A	2,3,4	*l	NA200P401
	+5V 30A	+12V 7A(Q)	F12V 5A(Q)	F12V 1.5A	—	2,3,4	*l	NA200P402
	+5V 30A	+12V 7A(Q)	F12V 5A(Q)	F24V 3A(Q)	F5V 1A	2,3,4	*l	NA200P500
	+5V 30A	+12V 7A(Q)	F12V 5A(Q)	F12V 5A(Q)	F5V 1A	2,3,4	*l	NA200P501
	+5V 30A	+12V 7A(Q)	F12V 5A(Q)	F12V 5A(Q)	F5V 5A(Q)	2,3,4	*l	NA200P502
	+5V 30A	+15V 7A(Q)	F15V 5A(Q)	F24V 3A(Q)	F5V 1A	2,3,4	*l	NA200P503
	F5V 30A	F12V 5A	F12V 5A	—	—	2,3,4	*l	NA200R300
	F5V 30A	F12V 5A	F24V 3A	—	—	2,3,4	*l	NA200R301
	F5V 30A	F15V 4.5A	F15V 4.5A	—	—	2,3,4	*l	NA200R303
	F5V 30A	F24V 3A	F24V 3A	—	—	2,3,4	*l	NA200R304
240 watts single output	5V 48A	—	—	—	—	2,3,4	*m	NS240005
	12V 20A	—	—	—	—	2,3,4	*m	NS240012
	15V 16A	—	—	—	—	2,3,4	*m	NS240015
	24V 10A	—	—	—	—	2,3,4	*m	NS240024
	30V 8A	—	—	—	—	2,3,4	*m	NS240030
	48V 5A	—	—	—	—	2,3,4	*m	NS240048
	56V 4.5A	—	—	—	—	2,3,4	*m	NS240056
300 watts multi output (FC)	+5V 40A	+12V 5A	-12V 5A	+24V 5A	-5V 1A	2,3,4	*n	N300R113U
	+5V 40A	+15V 5A	-15V 5A	+24V 5A	-5V 1A	2,3,4	*n	N300R135U
	F5V 40A	F12-24V 6A(8Apk)	F12-16V 6A(8Apk)	F12-16V 6A(8Apk)	F5-15V 4A(5Apk)	2,3,4	*o	NF300R500
	F5V 40A	F12-16V 6A(8Apk)	F48-56V 5A	F12-16V 6A(8Apk)	F5-15V 4A(5Apk)	2,3,4	*o	NF300R505
300 watts multi output and 48 volt D.C. input (FC)	+5V 40A	+12V 5A	-12V 5A	+24V 5A	-5V 1A	2,3,4	*n	ND300R801
	+5V 40A	+12V 5A	-12V 5A	-50V 5A	-5V 1A	2,3,4	*n	ND300R505
500 watts multi output (FC)	F5V 60A	F12-24V 6A(8Apk)	F12-16V 10A (12Apk)	F12-16V 6A(8Apk)	F5-15V 4A(5Apk)	2,3,4,5	*o+	NF500R500
	F5V 60A	F12-16V 6A(8Apk)	F48-56V 5A	F12-16V 6A(8Apk)	F5-15V 4A(5Apk)	2,3,4,5	*o+	NF500R505

CODES

(S) = Semi regulated (otherwise output is fully regulated) See specification sheets for further detail.
(Q) = Quasi regulated (otherwise output is fully regulated) See specification sheets for further detail.
F = Output is supplied floating
‡‡ = Can be supplied in opposite polarity to special order.
‡ = Floating or in opposite polarity to special order.
* = Localized areas may exceed these dimensions (eg terminal cover). Consult full outline drawings.
(FC)=Forced air Cooling at 1 meter/sec is required.
1 = PCB only.
2 = Mounted on L chassis.
3 = Fully cased (add suffix 'M' to end of model number).
4 = Customized enclosure to special order.
5 = Fully cased with integral fan.

DIMENSIONS (in inches)

	LENGTH	WIDTH	HEIGHT
a	7.19	4.32	2.00
b	6.50	4.15	2.13
c	7.19	4.41	2.13
d	7.19	4.41	2.41
e	7.98	4.72	2.41
f	10.53	4.63	2.36
g	8.30	4.53	2.36
h	7.99	4.43	2.36
i	8.28	4.53	2.36
j	9.74	5.00	2.36
k	10.91	4.93	2.83
l	10.49	4.79	2.76
m	9.76	5.91	2.61
n	12.02	7.59	2.95
o	11.81	7.48	2.56
O+ If integral fan is required			4.06

Unless noted by "(FC)", power ratings are with convection cooling. Forced Cooling will increase output capacity by 25% on the average.

FARNELL ADVANCE POWER

Advance Power Supplies, Inc.
32111 Aurora Road
Solon, Ohio 44139
PHONE (216) 349-0755.
FAX: (216) 349-0142.

703-022

CIRCLE NO. 150

16-BIT FIXED-POINT DSP μP

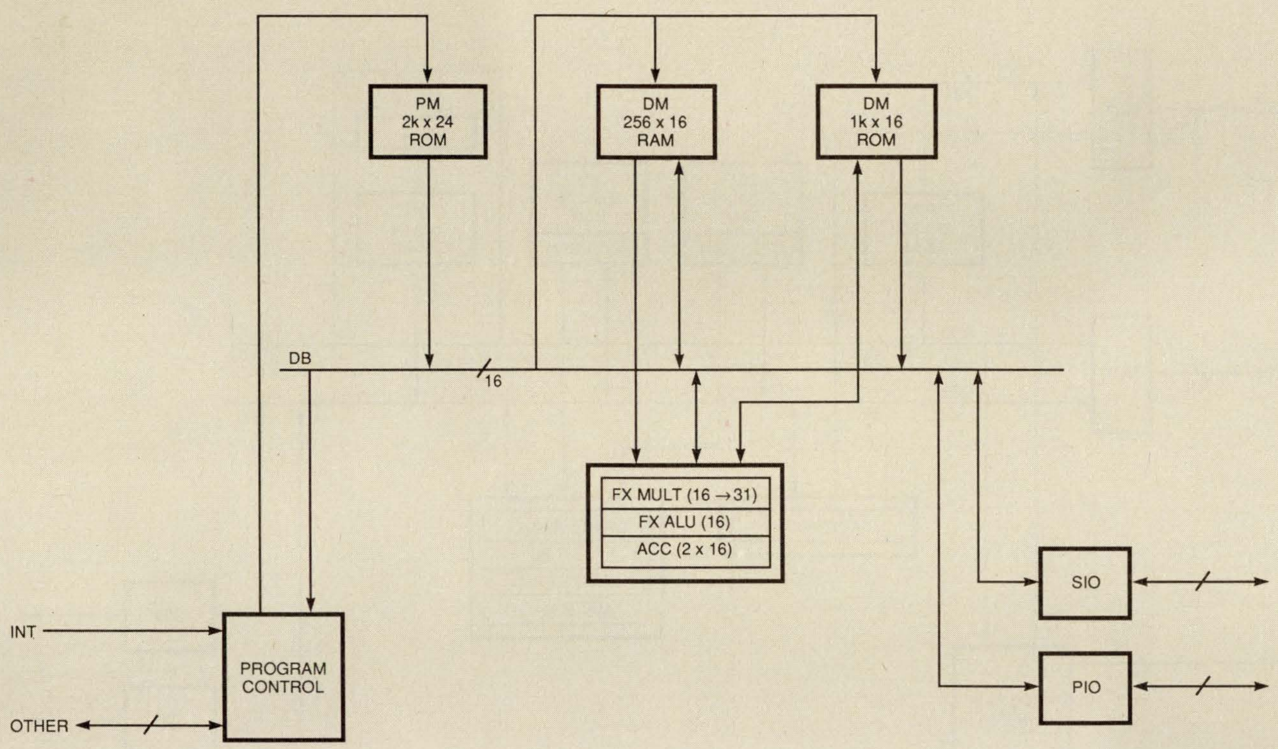
AVAILABILITY: The 77C25 is available now. A 28-pin PLCC version is scheduled for 1991.

COST: The 77C25 costs approximately $10 (5000); the 77P25 costs $45 (1000); the 77P25C costs $12 (1000).

SECOND SOURCE: Oki Semiconductor (Sunnyvale, CA) also makes the 7720.

NEC Electronics
401 Ellis St
Mountain View, CA 94039
(415) 965-6046
Circle No. 677

DESCRIPTION: The 77C25 is an upgrade of the 7720, which was one of the first successful DSP chips. The basic architecture is out of date and its memory can't be expanded off chip. The manufacturer says there is still interest in new 77C25 designs because of the chip's low cost. The 77P25 is an EPROM version of the 77C25. The 77P25C is a one-time-programmable version.



FEATURES: 122-nsec cycle time.
Single address bus only for program memory.
Pointers address data memory.
Single data bus for both program and data.
On-chip memory: The 77C25 has a 2k×24-bit program ROM, a 256×16-bit data RAM, and a 1k×16-bit data ROM. The 77P25 has the same memory as the 77C25 but replaces ROM with EPROM.
No external memory expansion.
One 8-bit serial I/O port.
Parallel I/O port.
Multiplier accepts 16-bit fixed-point data and produces 31-bit fixed-point results within two 16-bit accumulators.
16-bit ALU.
No barrel shifter.
Two 16-bit accumulators.
No zero-overhead looping.
No address generators.
No on-chip DMA.
4-level stack stores the program counter during subroutines and interrupts and is not expandable.
Single external interrupt.
No wait states.
No on-chip emulation port.
No low-power mode.
Packaged in 28-pin DIP, 44-pin PLCC, and 32-pin SOP. 28-pin PLCC coming in 1991.

HARDWARE — SUPPORT — SOFTWARE

Hardware: Evaluation kit for application development also functions as in-circuit emulator.

Software: Assembler/linker.
Third-party simulator available at end of 1990.

µPD77220

24-BIT FIXED-POINT CMOS DSP µP

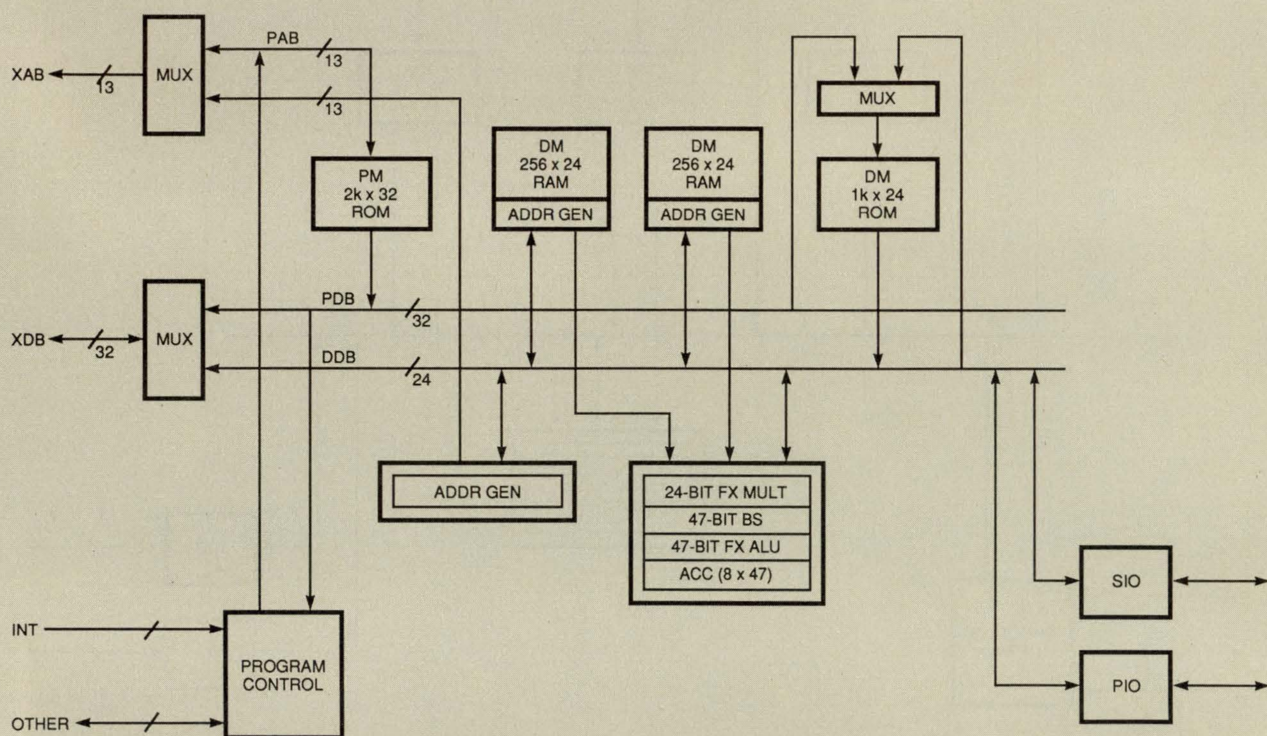
AVAILABILITY: The 122-nsec version is available now. The 100-nsec version is only available in the PGA package. Other packages will be available by the end of 1990.

COST: $30 (1000).

SECOND SOURCE: None.

NEC Electronics
401 Ellis St
Mountain View, CA 94039
(415) 965-6046
Circle No. 678

DESCRIPTION: The 77220 is a scaled-down version of the 32-bit floating-point 77230. The chip size and pin count are reduced by using 24-bit data and removing the floating-point exponent hardware. The 24-bit word width suits the digital audio market. The instruction set is a subset of the 77230 and is source-code compatible with the floating-point device. The vendor says the 77220's architecture is optimized for adaptive filter applications. The 77P220 EPROM version is for prototyping and low-volume applications.



FEATURES: 100- and 122-nsec cycle-time versions.
Separate on-chip program and data buses.
On-chip memory includes a 2k×32-bit program ROM, dual 256×24-bit data RAMs, and a 1k×24-bit data ROM.
Off-chip memory can be expanded to 8k×32-bit program memory and 8k×24-bit data memory.
One serial I/O port.
Parallel I/O port can be used as host µP interface.
Multiplier accepts 24-bit fixed-point data and creates 47-bit fixed-point results within a 47-bit accumulator.
47-bit ALU.
47-bit bidirectional barrel shifter.
Eight 47-bit accumulators.
Zero-overhead looping.
Direct, indirect, immediate, circular, and bit-reversal addressing modes.
Three address generators.
No on-chip DMA.
Hardware stack is eight levels deep and is not expandable.
Two external interrupts.
No supported wait states.
No on-chip emulation port.
No low-power mode.
Packaged in a 68-pin PGA or 68-pin PLCC.

HARDWARE — SUPPORT — SOFTWARE

Hardware: Evaluation kit and evaluation board.

Software:
Assembler/linker.
Simulator.

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CIRCLE NO. 96

TOKIN TECHNOLOGY UPDATE

TOKIN TROUNCES EMI

Please see us at Wescon/90® Electronic Show and Convention November 13–15/Anaheim, California #3184, 3186, 3188

It's the hottest game going: an all-star lineup of the finest EMC devices in the league—devices that get you through the current season, and many seasons to come.

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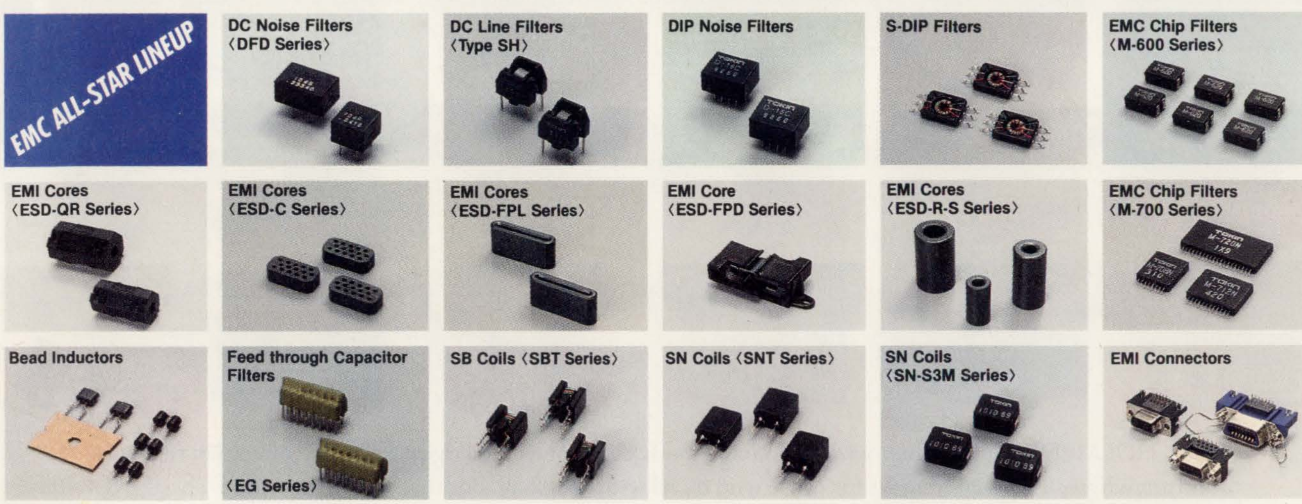
So for performance that truly excels, check the EMC rankings.

Then give us a call and let us know your needs.



TOKIN

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Tokin Europe GmbH
Knorrstr. 142, 8000 München 45, Germany
Phone: 089-311 10 66 Fax: 089-311 35 84

CIRCLE NO. 97

16-BIT FIXED-POINT CMOS DSP μP

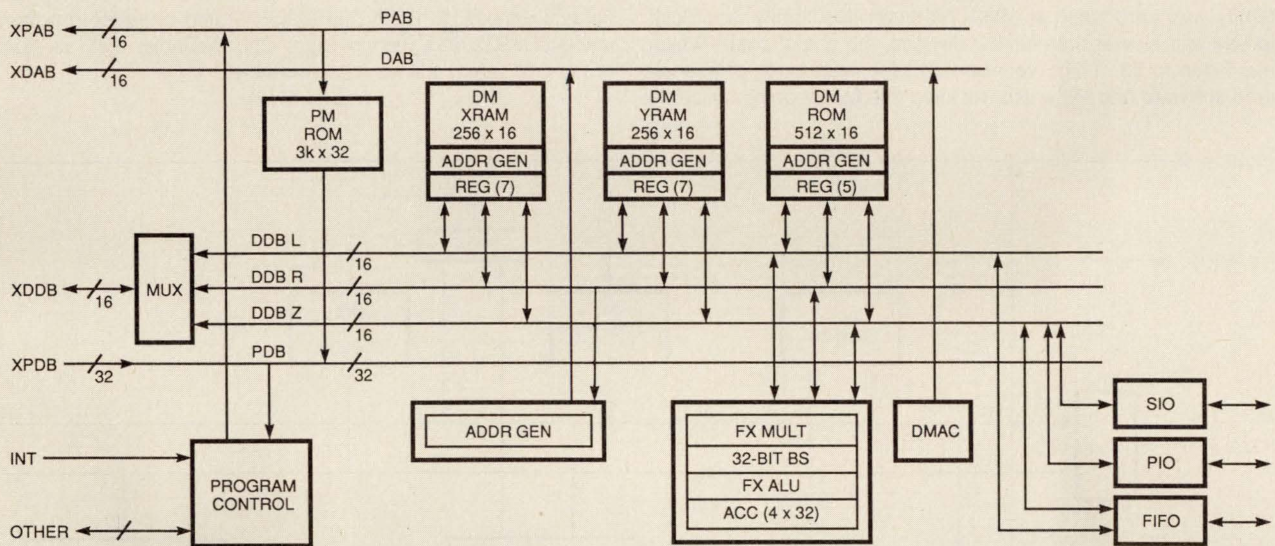
AVAILABILITY: Now.

COST: The ST18930 costs $15; the ST18931 costs $80; the ST18940 costs $35; the ST18941 costs $95 (5000).

SECOND SOURCE: None.

SGS-Thomson Microelectronics
1000 E Bell Rd
Phoenix, AZ 85022
(602) 867-6340
Circle No. 679

DESCRIPTION: The ST18 family consists of four devices. The ST18930 and -31 are CMOS versions of the NMOS original with a few enhancements and twice the speed. The CMOS ST18940 and -41 offer further enhancements in their arithmetic capabilities, addressing modes, and I/O functions. All family members can operate on complex and double-precision data. The ST18930 and -40 are ROM versions. The ST18931 and -41 are ROMless versions and have external EPROMs for program storage during software development. The devices are used in modems and in other DSP applications.



FEATURES: The ST18930 and -31 have 80-nsec cycle times.
The ST18940 and -41 have 100-nsec cycle times.
Two address buses and four data buses on chip.
On-chip memory: The ST18930 has a 3k×32-bit program ROM, a 192×16-bit data RAM, a 128×16-bit data RAM, and a 512×16-bit data ROM. The ST18931 has the same memory as the ST18930 but without ROM. The ST18940 has a 3k×32-bit program ROM, two 256×16-bit data RAMs, and a 512×16-bit data ROM. The ST18941 is a ROMless version of the ST18940 and has two 256×16- and one 128×16-bit data RAMs.
64k×32-bit external program memory can only be accessed by the ROMless versions.
4k×16-bit external data memory space.
Only the ST18940 and -41 have both a serial I/O port and a parallel I/O port.
Multiplier accepts 16-bit fixed-point data and returns 32-bit fixed-point results to a 32-bit accumulator.
In complex mode, the multiplier multiplies two complex numbers in two cycles.
16-bit ALU.
16-bit bidirectional barrel shifter.
Four 32-bit accumulators.
No zero-overhead looping.
Immediate, direct, indirect, and circular addressing modes.
Three address generators on the ST18930 and -31 and four on the ST18940 and -41.
The ST18940 and -41 have on-chip DMA.
8-level hardware stack for interrupts and subroutines. Can be expanded into main memory with software.
Three external interrupts on the ST18930 and -31 and five on the ST18940 and -41.
Hardware and software-programmable wait states.
No on-chip emulation port.
Low-power mode.
Packaging: ST18930, 48-pin DIP and 52-pin PLCC. ST18931, 121-pin PGA. ST18940, 84-pin PLCC. ST18941, 144-pin PGA.

HARDWARE — SUPPORT — SOFTWARE

Hardware:
Hardware development system provides in-circuit emulation of as many as three DSP chips in real time.
Stand-alone emulator board connects to an IBM PC.
EPROM module. A ROMless version with EPROMs on a small board that plugs into a ROM-version socket.

Software:
C compiler.
Macroassembler/linker.
Simulator.

TMS320C1X

16-BIT FIXED-POINT CMOS DSP μP

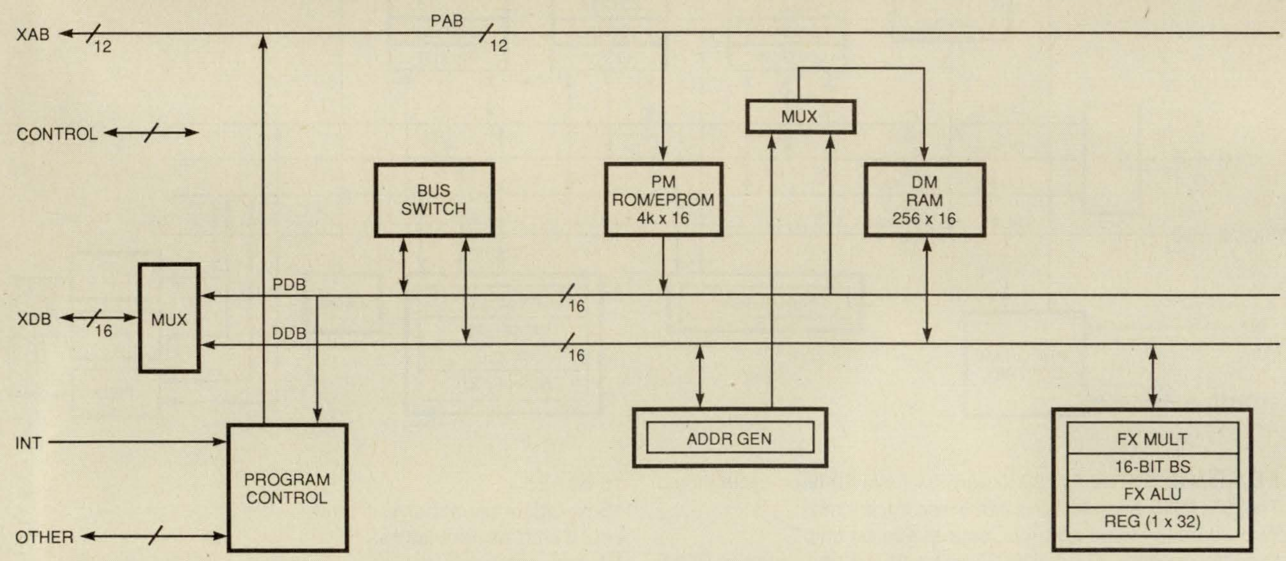
AVAILABILITY: The C10, C15, C17, E14, E15, and E17 are available now. The C16 is sampling now. Production is scheduled for the first half of 1991. The C14, P14, P15, and P17 will be available in 1991.

COST: C10 (14 MHz), $6; C10 (20 MHz), $8; C10 (25 MHz), $9; C14, $14; E14, $45; P14, $22; C15 (20 MHz), $9; C15 (25 MHz), $11; E15 (20 MHz), $35; E15 (25 MHz), $45; P15, $20; C16, $10; E17, $38; P17, $20 (1000).

SECOND SOURCE: Microchip Technology (Chandler, AZ) second sources the C10, C14, and E14. No second source for other parts.

Texas Instruments Inc
Semiconductor Group, SC-9026
Box 809066
Dallas, TX 75380
(800) 232-3200, ext 700
Circle No. 680

DESCRIPTION: This first generation of the vendor's DSP family was introduced in 1982. Although this family is difficult to use and slower than similar devices, the chips' cost—which has fallen to $3 in high volume—and the large body of associated software and expertise will keep this family going for some time. Newer family members have additional memory and peripheral options. EPROM (TMS320E1X) and one-time-programmable (TMS320P1X) versions are also available. 3.3V versions of the C1X family will soon be available.

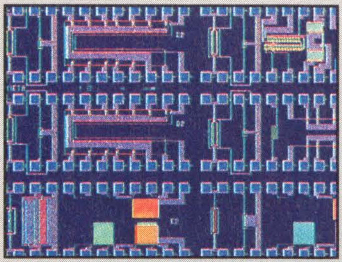
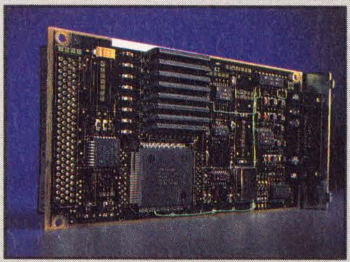


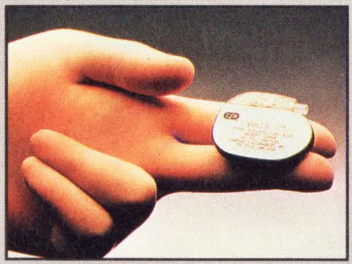
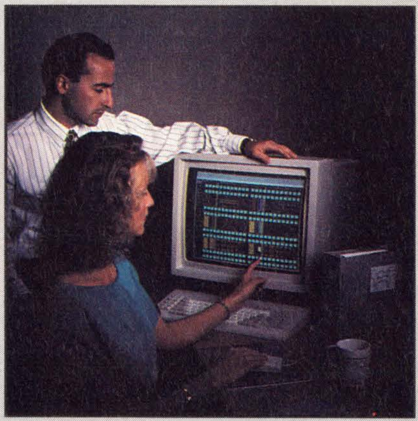
FEATURES: 114-, 160-, 200-, and 280-nsec cycle-time versions. Separate on-chip program and data buses.
On-chip memory: The C10 has a 1.5k×16-bit program ROM and a 144×16-bit data RAM. The C14, C15, and C17 have a 4k×16-bit program ROM and a 256×16-bit data RAM. The E14, E15, and E17 have a 4k×16-bit program EPROM and a 256×16-bit data RAM. The C16 has an 8k×16-bit program ROM and a 256×16-bit data RAM. P1X versions are one-time programmable.
Program and data buses are combined off chip.
4k×16-bit total external memory except the C16, which has 64k×16-bit external memory, and the C17, which has no external memory.
On-chip peripherals: The C10, C15, and C16 have parallel I/O. The C14 has serial and parallel I/O. The C17 has two serial I/O ports, parallel I/O, and a compander.
Multiplier accepts 16-bit fixed-point data and creates 32-bit fixed-point results within a 32-bit accumulator.
32-bit ALU.
16-bit left barrel shifter.
Single 32-bit accumulator.
No zero-overhead looping.
No DMA.
4-level hardware stack except the C16, which has an 8-level hardware stack.
Single external interrupt.
No wait states.
No on-chip emulation.
No low-power mode.
Packaging: C10, 40-pin DIP or 44-pin PLCC. C14, 40-pin DIP or 44-pin PLCC. C15, 40-pin DIP or 44-pin PLCC. C16, 64-pin quad flatpack. C17, 40-pin DIP or 44-pin PLCC.

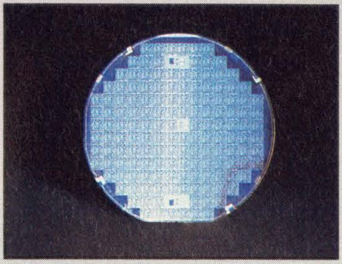
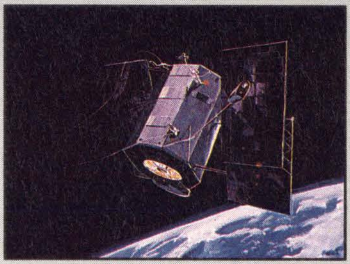
HARDWARE — SUPPORT — SOFTWARE

Hardware:
In-circuit emulator.
Evaluation module.
Many third-party support tools. Contact manufacturer for a list of third-party vendors.

Software:
Assembler/linker.
Simulator.
Application library.
Many third-party support tools.

HSPICE: From Concept to Creation

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Pacemaker photo courtesy of Cardiac Pacemakers, Inc. Satellite photo courtesy of NASA. Use of PC board courtesy of Sun Microsystems, Inc.

16-BIT FIXED-POINT CMOS DSP μP

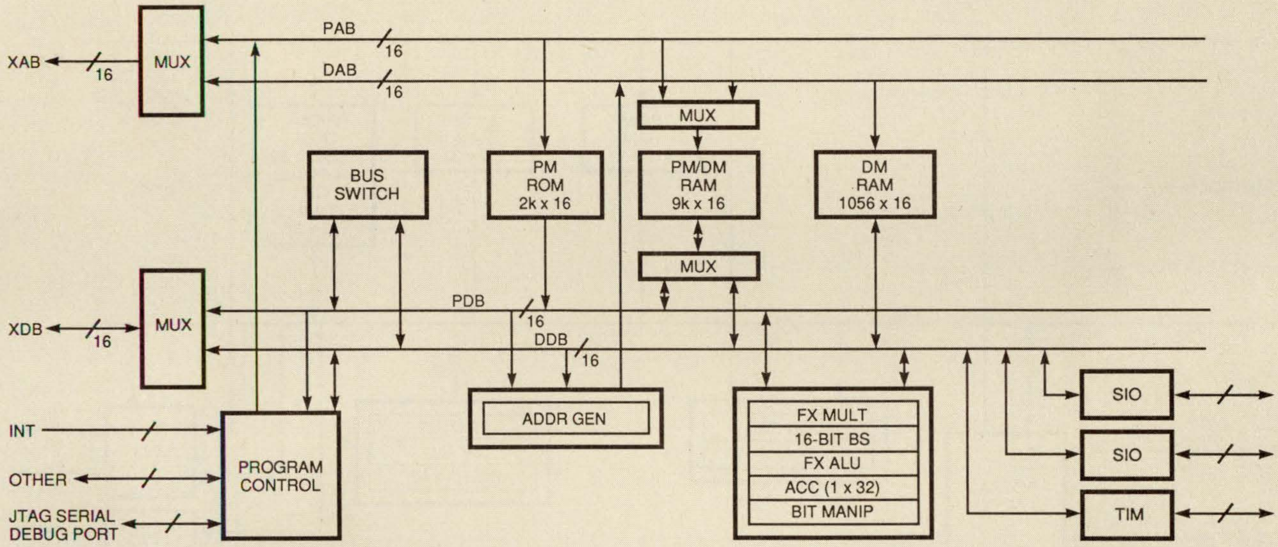
AVAILABILITY: The C25, C26, and E25 are available now. The C50 and C51 are sampling now and will be in production in 1991.

COST: C25 (33 MHz), $17; C25 (40 MHz), $18; C25 (50 MHz), $24; E25, $55; C26, $24; C50, $130; C51, $40 (1000).

Texas Instruments Inc
Semiconductor Group, SC-9026
Box 809066
Dallas, TX 75380
(800) 232-3200, ext 700
Circle No. 681

SECOND SOURCE: None.

DESCRIPTION: These chips make up the second generation of the vendor's DSP family. They offer higher performance than the first-generation chips and are easier to use. For many applications, the C25's price has fallen to a point where the chip is replacing the C1X. The C5X parts are enhancements to the C25. They use the same basic core architecture as the C25 but have double the performance level, additional on-chip peripherals, and expanded memory. An EPROM version of the C25, the E25, is also available.



FEATURES: The C2X chips come in 78-, 98-, and 125-nsec cycle-time versions. The C5X chips come in 35- and 50-nsec cycle-time versions.
On-chip memory: The C25 has a 4k × 16-bit program ROM and a 544 × 16-bit data RAM. The C26 has a 1.5k × 16-bit program RAM with boot ROM to load programs from external memory and a 544 × 16-bit data RAM. The C50 has a 2k × 16-bit program ROM, a 9k × 16-bit program/data RAM, and a 1056 × 16-bit dual-access RAM. The C51 has an 8k × 16-bit program ROM, a 1k × 16-bit program/data RAM, and a 1056 × 16-bit dual-access RAM. Program and data memory are combined off chip.
The C2X and C5X can address 64k × 16-bit program and 64k × 16-bit data memory.
The C25 and C26 have one serial port each. The C5X has two serial ports.
Multiplier accepts 16-bit fixed-point data and creates 32-bit fixed-point results within a 32-bit accumulator.
32-bit ALU.
The C5X has a separate 16-bit parallel logic unit for manipulating bits without affecting the contents of the accumulator.
16-bit left barrel shifter.
Single 32-bit accumulator.
Next-instruction-repeat looping. Only the C5X has zero-overhead block looping.
Immediate, direct, indirect, and bit-reversal addressing modes. C5X also has circular addressing.
No DMA.
8-level expandable hardware stack.
C5X has a 1-level-deep shadow RAM, which stores some registers.
C2X has three external interrupts; C5X has five.
Hardware wait states. C5X also has software-programmable wait states.
The C5X has an on-chip emulation port.
The C2X is source-code compatible with the C5X.
The C5X has a JTAG interface.
The C25 and C26 have an idle mode. The C50 has a power-down mode.
Packaging: C25 and C26, 68-pin PGA or PLCC. C50, 132-pin quad flatpack.

HARDWARE — SUPPORT — SOFTWARE

Hardware

Both the C2X and C5X have an in-circuit emulator.
Both also have a software-development board for the IBM PC.
Many third-party support tools. Contact manufacturer for a list of third-party vendors.

Software

C compiler for both C25 and C5X.
Source-level debugger for C5X.
Assembler/linker.
Simulator.
Application library.
Many third-party support tools.

DSP32C

32-BIT FLOATING-POINT CMOS DSP μP

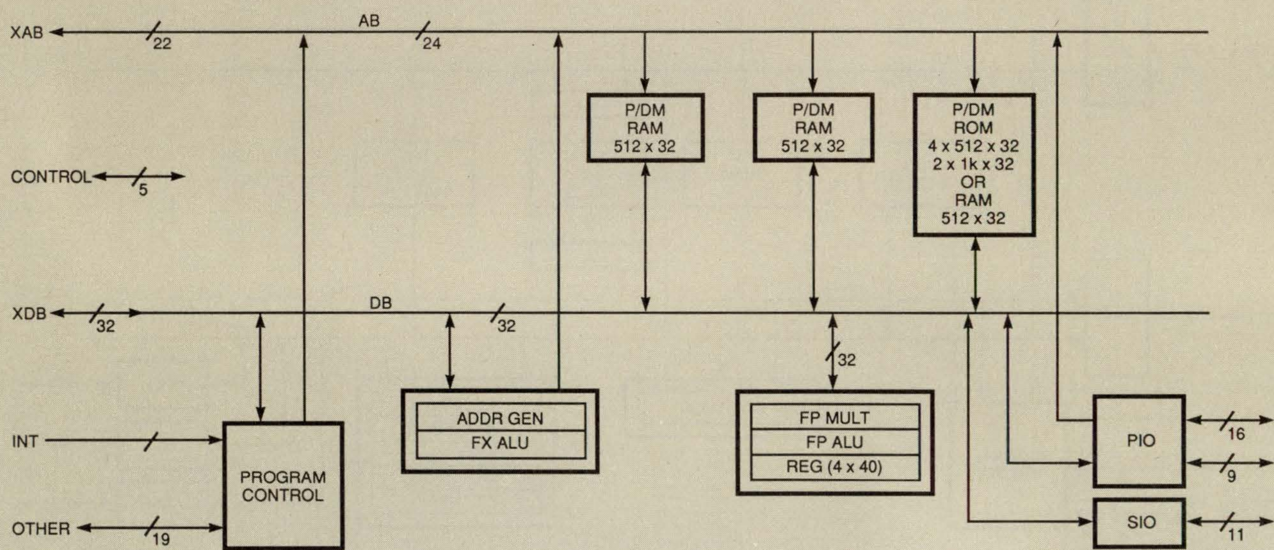
AVAILABILITY: Now.

COST: \$70 (1000).

SECOND SOURCE: None.

AT&T Microelectronics
Dept 52AL300240
555 Union Blvd
Allentown, PA 18103
(800) 372-2447;
in Canada, (800) 553-2448
Circle No. 682

DESCRIPTION: The DSP32C has one of the simplest architectures of the 32-bit floating-point DSP chips. It uses a single 4M-word linear memory space instead of the separate program and data memory common in other DSP chips. The single address bus and single data bus can be accessed as many as four times per cycle. Each internal memory can be accessed as many as two times per cycle. Although the architecture looks simple, the DSP32C can read an instruction, read two data values, and write a previous result in a single cycle. Data is addressable as 8-, 16-, or 32-bit words.



FEATURES: 80- and 100-nsec cycle-time versions.
Single address and data buses. Each can be accessed as many as four times per cycle to imitate separate buses.
Three on-chip 512×32-bit RAMs.
Optional ROM-based DSP32C replaces one RAM with a 4k×32-bit ROM.
Can address as much as 4M×32 bits of external memory.
All memory is a general resource; both program and data can exist anywhere.
Data addressable as 8-, 16-, or 32-bit words.
On-chip serial and parallel I/O.
The serial I/O is a double-buffered port that allows concurrent input and output of 8-, 16-, 24-, or 32-bit data widths.
Has an 8- or 16-bit parallel I/O port that an external μP can control.
Proprietary 32-bit floating-point format.
Single-cycle conversion to/from nonstandard DSP32 floating-point format from/to IEEE-754 floating-point format.
Multiplier accepts 32-bit floating-point data and creates 45-bit floating-point results.
Separate floating-point adder accepts 40-bit floating-point data and creates 40-bit floating-point results.
Fixed-point ALU accepts 16- or 24-bit data.
Does not have a barrel shifter.
Four 40-bit accumulators.
Zero-overhead looping. As many as 2048 repeats of a block with a maximum size of 32 words.
Immediate, memory-direct, register-direct, register-indirect, and bit-reversal addressing modes.
DMA can be used with both the serial I/O and the parallel I/O.
No hardware stack.
1-level-deep shadow RAM of some registers.
Two external interrupts.
Hardware wait states.
No on-chip emulation port.
No low-power mode.
Packaged in a 164-pin plastic quad flatpack, 133-pin PGA, or 68-pin PLCC (μC version, no external memory).

HARDWARE — SUPPORT — SOFTWARE

Hardware:
In-circuit emulator.
IBM PC-based development board.
VMEbus-based development board.
Many third-party support tools, including the HP64773 in-circuit emulator from Hewlett-Packard. Contact AT&T for a list of third-party vendors.

Software:
Optimizing C compiler.
Assembler/linker.
State simulator.
Many third-party support tools.

Text continued on pg 193

"The final design has the circuit board in the back, but the LEDs must be in the front.

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Saving costs while solving problems is something we've long done with our panel mount and circuit board LEDs. Over the years customers have asked us to pair, gang, piggyback, right angle mount, recess, bicolor, tricolor, slant, standoff, snap-mount, bin, do whatever you can imagine to them and we haven't been stumped yet!

So, the next time you think there's a remote chance of finding the right solution to an indicator design issue, remember that no one has more solutions than Dialight.

DIALIGHT CORPORATION

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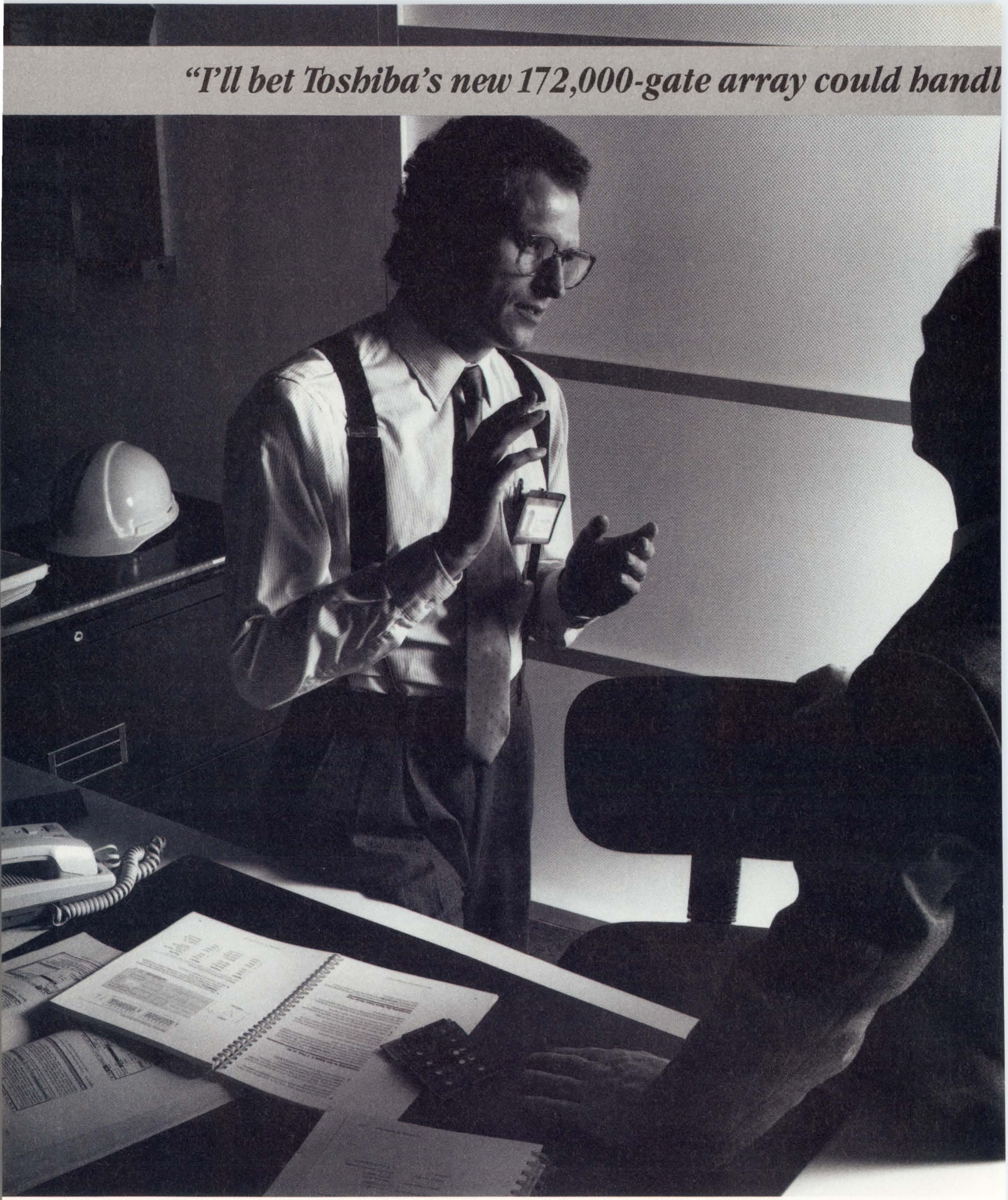
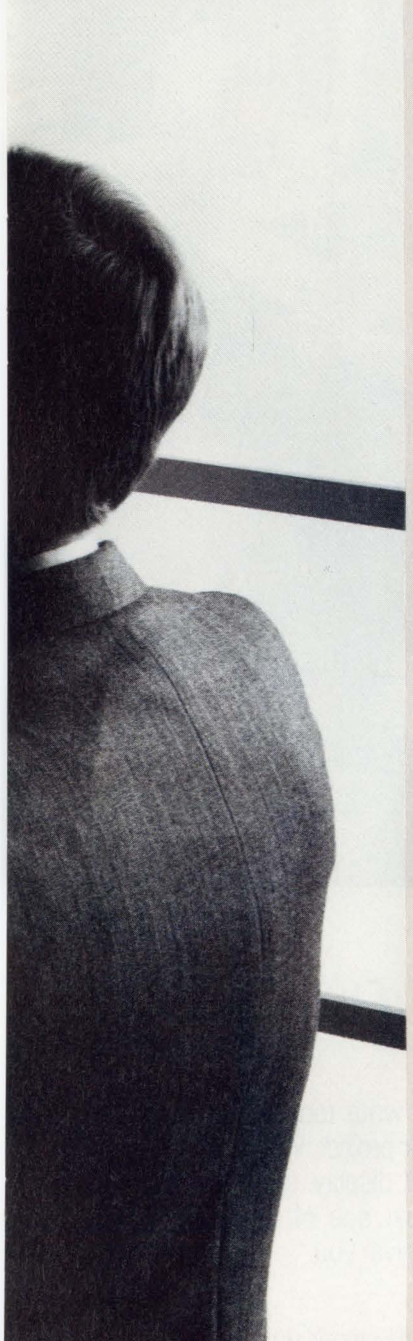
CIRCLE NO. 99


"I'll bet Toshiba's new 172,000-gate array could handl

t.”



“Think of what we could do with 33% more gates.”

“And think how much board space the increased density would save us.”

“Without sacrificing speed. It’s still under 400 picosecond gate delay.”

“I wonder how fast we can get our hands on one.”

“How fast can you dial that phone?”

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GATES	37,932 to 129,042	2,300 to 172,000
GATE LENGTH	1.0μ	1.0μ
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PART NUMBERS	5	14
AVAILABILITY	NOW	NOW
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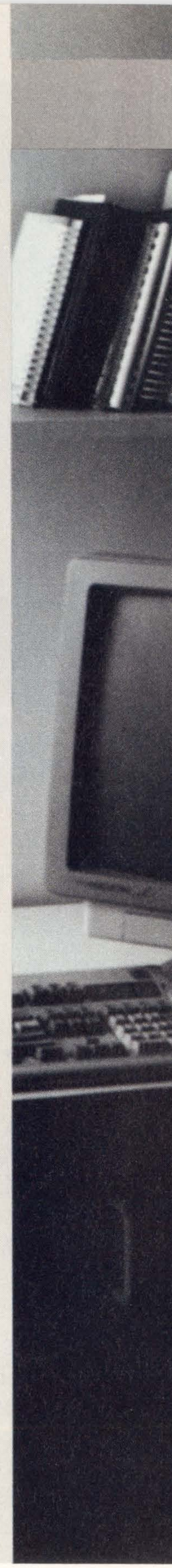

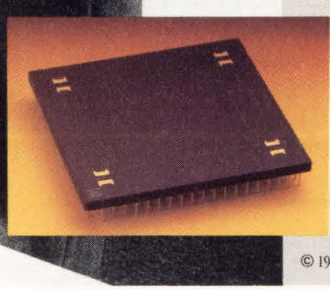

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CIRCLE NO. 100

MAS-89-011-1

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32-BIT FLOATING-POINT CMOS DSP µP

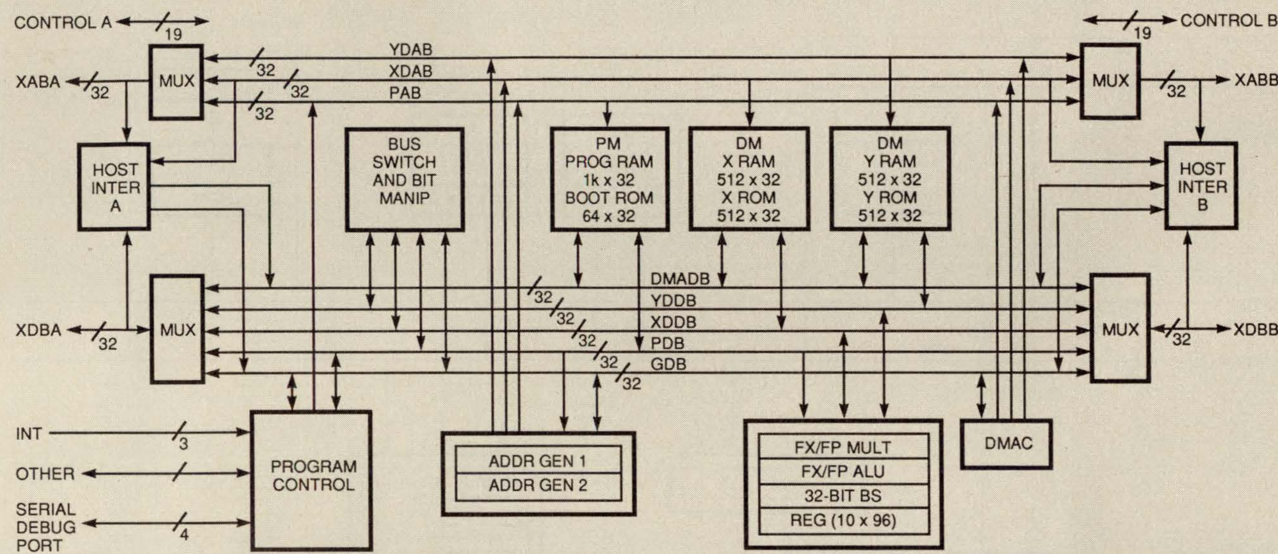
AVAILABILITY: Sampling. Production scheduled for this month.

COST: The 96002 (27 MHz) costs $650; the 96002 (33 MHz) costs $750.

SECOND SOURCE: None.

Motorola Inc
Microprocessor Products Group
6501 William Cannon Dr
Austin, TX 78735
(512) 891-2030
Circle No. 683

DESCRIPTION: The 96002 is an architectural superset of the fixed-point 56001. The 96002 continues Motorola's emphasis on precision. Full 32-bit integers are multiplied to a nontruncated 64-bit product. 32-bit floating-point numbers are multiplied to 44-bit products. The 32-bit floating-point device conforms to the IEEE-754 floating-point standard. The dual 32-bit external buses support glueless multi-96002 systems. The external buses can access external memory and peripherals or communicate with a host µP. The 96-bit accumulators will support future double-precision parts.



FEATURES: 60- and 74-nsec cycle-time versions. 50-nsec cycle-time version scheduled for 1991.
Three 32-bit address buses and five 32-bit data buses on chip.
Separate address buses for program and the two on-chip RAMs.
Separate data buses for program, the two on-chip RAMs, global data, and DMA.
On-chip memory includes a 1k × 32-bit program RAM, a 64 × 32-bit boot ROM, dual 512 × 32-bit data RAMs, and dual 512 × 32-bit data ROMs.
On-chip boot ROM loads program from external byte-wide EPROM.
Two complete 32-bit external expansion ports for memory and I/O.
Three separate memory spaces (X, Y, and P). Each can address 4G words.
Each memory space is divided into eight 0.5G-word areas. Each can be programmed to either the A or B expansion ports.
Two host interfaces allow interface to µP or other 96002s. No other on-chip peripherals.
IEEE-754 32-bit floating-point format.
Multiplier accepts 32-bit floating-point data and returns 44-bit results. Multiplier accepts 32-bit integer data and returns 64-bit results.
32-bit bidirectional barrel shifter.
Ten 96-bit or thirty 32-bit register-based accumulators.
Zero-overhead looping.
Immediate, direct, indirect, circular, and bit-reversal addressing modes.
Two address ALUs.
DMA is supported. Uses its own internal bus and doesn't cycle-steal. Can use all of the addressing modes, including bit-reversal, with the DMA controller.
The stack is 15 levels deep and can be expanded into main memory.
Three external vectored interrupts.
Hardware and software-programmable wait states.
Serial debug port for in-circuit debugging.
Low-power mode.
Packaged in a 223-pin PGA. 256-pin ceramic quad flatpack available in 1991.

HARDWARE — SUPPORT — SOFTWARE

Hardware

Hardware evaluation system includes in-circuit emulator.
Some third-party hardware products are available. Contact Motorola for a list of third-party vendors.

Software

Optimizing C compiler.
Assembler/linker.
Simulator.
Application library.
Third-party support includes optimizing C compiler, block-level diagraming language, filter-design software, and real-time operating system (SPOX).

μPD77230/240

32-BIT FLOATING-POINT CMOS DSP μP

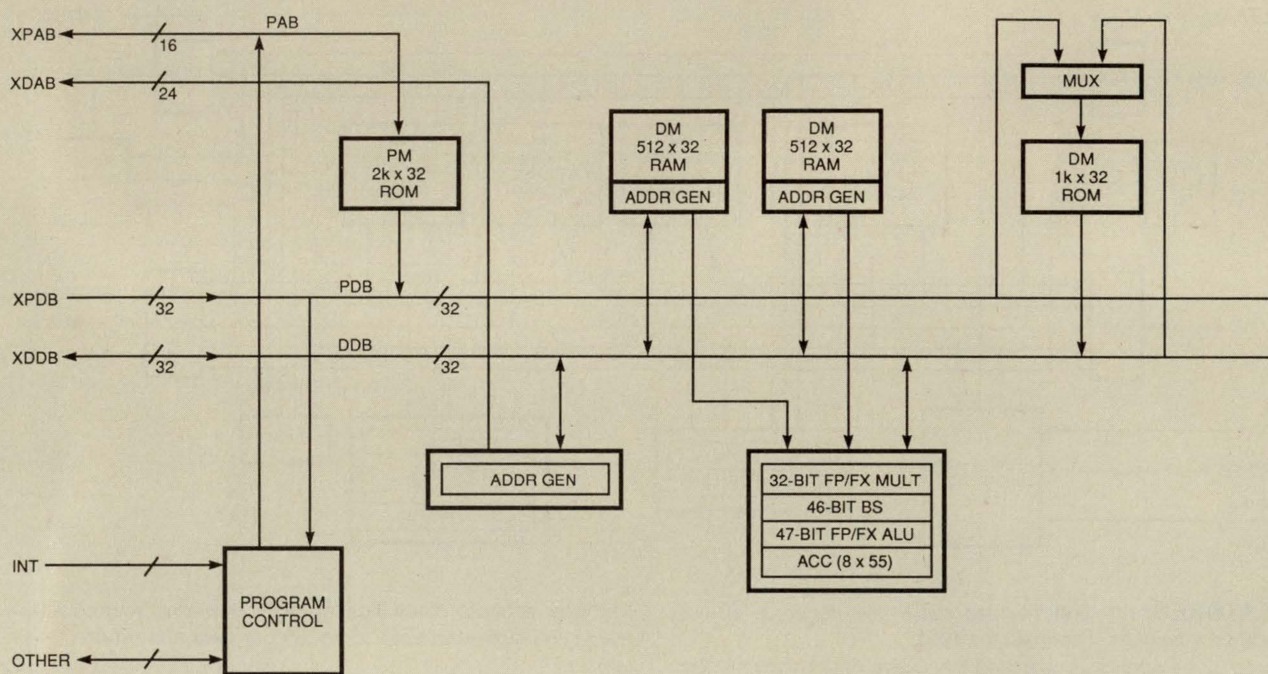
AVAILABILITY: The 77230 is available now. The 77240 is sampling now, and production is scheduled to begin in January 1991.

COST: The 77230 costs $74; the 77240 costs $90 (1000).

SECOND SOURCE: None.

NEC Electronics
401 Ellis St
Mountain View, CA 94039
Phone (415) 965-6046
Circle No. 684

DESCRIPTION: The 77230 and 77240 are 32-bit CMOS floating-point DSP chips. The 77P230 is an EPROM version of the ROM part for prototyping and small production runs. The 77240 is an enhanced version of the 77230. It has more on-chip RAM and can be expanded to 64k-word program memory and 16M-word data memory. The architecture suits adaptive filter applications.

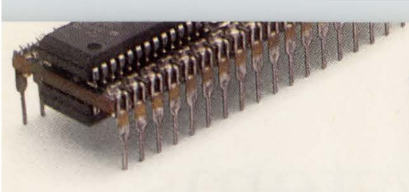


FEATURES: 77230 has 150-nsec cycle time.
77240 has 90-nsec cycle time.
Separate on-chip program and data buses.
On-chip memory: The 77230 has a 2k × 32-bit program ROM, dual 256 × 32-bit data RAMs, and a 1k × 32-bit data ROM. The 77240 has a 2k × 32-bit program ROM, dual 512 × 32-bit data RAMs, and a 1k × 32-bit data ROM.
External memory expansion: The 77230 can address 8k × 32-bit program memory and 8k × 32-bit data memory. The 77240 can address 64k × 32-bit program memory and 16M × 32-bit data memory.
The 77230 has serial and parallel I/O. The 77240 has no on-chip peripherals.
Proprietary 32-bit floating-point format.
Multiplier accepts 32-bit floating-point data and creates 45-bit floating-point results.
Multiplier accepts 24-bit fixed-point data and creates 47-bit fixed-point results.
47-bit ALU.
47-bit bidirectional barrel shifter.
Eight 55-bit register-based accumulators.
Zero-overhead looping.
Direct, indirect, immediate, circular, and bit-reversal addressing modes.
Two address ALUs on the 77230. Three address ALUs on the 77240.
No on-chip DMA.
The stack is eight levels deep and is not expandable.
Two external interrupts.
No wait states.
No on-chip emulation port.
No low-power mode.
Packaging: 77230, 68-pin PGA. 77240, 132-pin PGA.

HARDWARE — SUPPORT — SOFTWARE

Evaluation kit, which includes an in-circuit emulator.
Evaluation board.

Assembler/linker and simulator.
C compiler scheduled for 1991.

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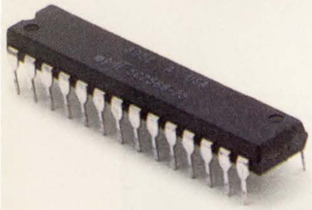
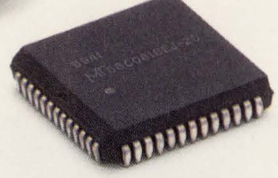
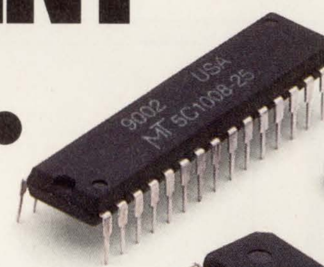
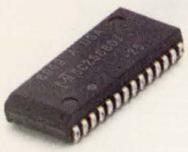



YOURS.

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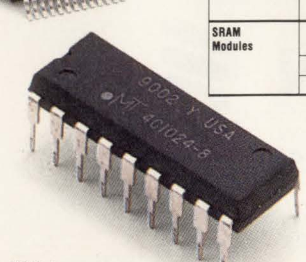
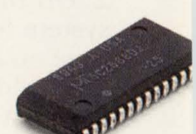
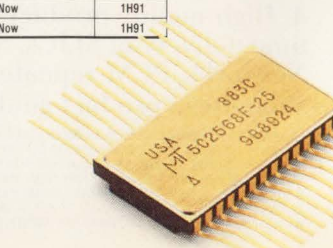
Component Product Family	Memory Size (Total)	Org. (Bits)	Speed (ns)	Package DIP	ZIP	SOJ	PLCC	TSOP	PQFP	Special Features	Availability	Military Qualified
SRAMs	1MEG	x1,x4,x8	25-45	X		X				x4 option: OE	Now	2H90
	256K	x1,x4,x8	20-45	X	X	X				x4 option: OE	Now	X
	64K	x1,x4,x8	12-45	X		X				x4 options: Separate I/O, OE	Now	X
	16K	x1,x4,x8	12-45	X		X				x4 options: Separate I/O, OE	Now	X
Cache Data SRAMs	288K	x9	14-34				X			486 Compatible, Self-timed write, Fast toe 7ns, 486 Burst and extended burst support	Samp: 1H91, Prod: 2H91	
	144K	x18	20-35				X		X	386/486 Compatible, Fast toe 8ns, Auto write completion, Parity bits	Now	
	128K	x16	20-35				X		X	386 Compatible, Fast toe 8ns	Now	
Synchronous SRAMs	288K	x18	15-25				X			Registered address, chip enables and write control; Data latch, Fast toe 6ns, Byte write capability	Samp: 2H90, Prod: 1H91	Samp: 1H91
	256K	x16	15-25				X					
SRAMs with Address Latch	288K	x18	15-35				X			Address, data and chip enable latches; Byte write capability, Fast toe 6ns, 3.0 Volt output buffer option	Samp: 2H90, Prod: 1H91	Samp: 1H91
	256K	x16	15-35				X					
	16K	x8	100	X		X				Intel 8051 and 8096 compatible	Now	X
	16K	x8	15-35	X		X				Compatible with high end micro controllers	Now	X
FIFOs	18K	2Kx9	15-35	X			X			Family options: 300 mil DIP package, Programmable flags	Samp: 1H91	2H91
	9K	1Kx9	15-35	X			X				Samp: 1H91	2H91
	4.5K	512x9	15-35	X			X				Samp: 1H91	2H91
DRAMs	4MEG	x1,x4,x8,x16	60-100	X	X	X		X		x4,x8 options: Write per bit x16 options: 2 WE/1CAS; 1WE/2CAS and 1WE/1CAS with write per bit	x1,x4 Samp: Now, Prod: 1H91; x8,x16 Samp: 1H91	Samp: 1H91
	1MEG	x1,x4,x16	70-120	X	X	X		X		x16 options: Byte write or write per bit	Now	X
	256K	x1,x4	100-120	X	X	X	X				Now	X
	64K	x1	100-150	X			X				Now	X
Quad CAS DRAMs	4MEG	x4	60-100			X				Separate CAS control for each DQ input/output, Enhanced write per bit capabilities	Samp: 1991	
	1MEG	x4	70-100			X					Now	
Pseudo Static DRAM	1MEG	x8	80-120	X		X		X		Unmultiplexed addresses, Simple refresh control	Samp: 2H90, Prod: 1H91	
Dual Port DRAMs (VRAMs)	1MEG	x4,x8	80-120		X	X				CMOS, Fully static SAM, Serial input, Split read transfer	Now	Samp: 1H91
	256K	x4	100-120	X	X					CMOS, Fully static SAM, Serial input	Now	X
Triple Port DRAMs	1MEG	x4,x8	80-120			X	X			CMOS, Two fully static SAMs, Transfer mask, Split t.ansfers, Functional superset of 1MEG VRAM	Samp: Now, Prod: 2H90	

Module Product Family*	Word Size (Words)	Org. (Bits)	Speed (ns)	Package DIP	ZIP	SIP	SIMM			Special Features	Availability	Military Qualified
DRAM Modules	2MEG,1MEG, 512K,256K	x36	70-120		X		X			Industry standard pin-out	256K, 512K: Now; 1MEG, 2MEG Samp: 2H90	
	4MEG,1MEG, 256K	x9	70-120			X	X			Industry standard pin-out	256K, 1MEG: Now; 4MEG Samp: 2H90	
	4MEG,1MEG, 256K	x8	70-120			X	X			Industry standard pin-out	256K, 1MEG: Now; 4MEG Samp: 2H90	
SRAM Modules	256K, 128K, 64K, 16K	x32	15-45		X					Industry standard pin-out with OE	16K, 64K: Now; 128K,256K: 2H90	1H91
	64K,32K	x16	30-45	X						Industry standard pin-out with OE	Now	1H91
	128K	x8	30-45	X						Compatible with 1MEG monolithic	Now	1H91

* Custom module and board-level product manufacturing services available.

MICRON
TECHNOLOGY, INC.

2805 E. Columbia Rd., Boise, ID 83706 (208) 368-3900

CIRCLE NO. 102

22-BIT FLOATING-POINT CMOS DSP μP

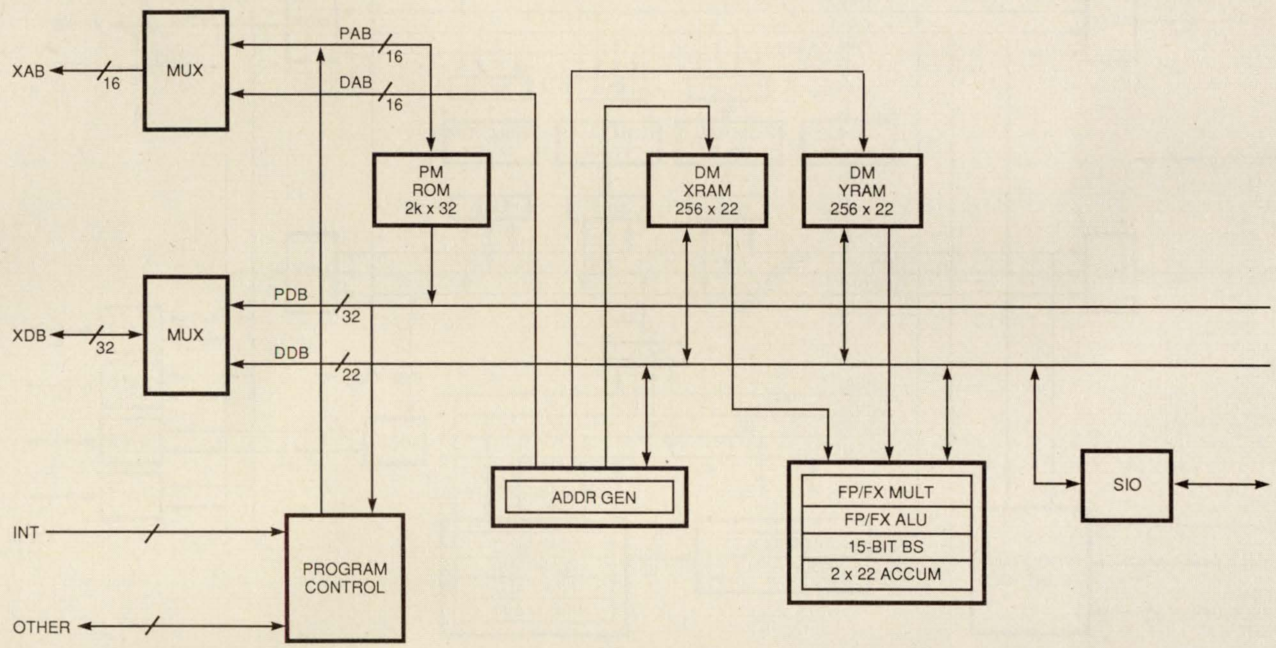
AVAILABILITY: Now.

COST: The 699210 costs $40; the 699215 costs $40 (10,000).

SECOND SOURCE: None.

Oki Semiconductor
785 N Mary Ave
Sunnyvale, CA 94086
(408) 720-1900
Circle No. 685

DESCRIPTION: This family operates on 22-bit floating-point data. The chip was designed for applications that need more resolution than 16-bit fixed-point DSP chips offer but do not need the capabilities of 32-bit floating-point devices. The vendor is keeping this family's older architecture alive by surrounding the proven DSP core with peripherals to create specialized chips. For example, the recently introduced MSM6994 is a specialized device for modems that combines the family's DSP core with various peripherals.



FEATURES: 100- and 125-nsec cycle-time versions.
Separate on-chip program and data buses.
2k × 32-bit program ROM and two 256 × 22-bit data RAMs.
External program and data memory can each be expanded to 64k words.
The instruction word is 32 bits wide, so external program memory also needs to be 32 bits wide.
Dual-access RAMs. Can read two values and write a third in one cycle.
8/16/22-bit parallel interface.
The 699215 has a serial I/O port.
Proprietary 22-bit floating-point format has 16-bit mantissa and 6-bit exponent.
Multiplier accepts 22-bit floating-point data and returns 22-bit floating-point result. 16-bit fixed-point data results in 31-bit fixed-point result.
ALU performs 22-bit floating-point arithmetic, 16-bit fixed-point arithmetic, and 22-bit logical operations.
15-bit bidirectional barrel shifter.
Two 22-bit accumulators.
Zero-overhead looping.
2-loop hardware counters, 12 and 4 bits, allow dual-loop function.
Double-precision operation possible on 16-bit integers.
No on-chip cache.
Immediate, direct, and indirect addressing modes.
Single address ALU.
No on-chip DMA.
Hardware stack is eight levels deep and is not expandable.
Three external interrupts.
No wait states.
No on-chip emulation port.
Low-power mode
Packaged in an 84-pin PLCC or 100-pin flatpack.

HARDWARE — SUPPORT — SOFTWARE

Hardware:
ADC/DAC board and DSP board plug into an IBM PC/AT.
In-circuit emulation board.
Stand-alone board to exercise code.

Software:
Macroassembler/linker.
Simulator.
Application library.
OSL compiler, a C-like high-level language.

TMS320C3X

32-BIT FLOATING-POINT CMOS DSP μP

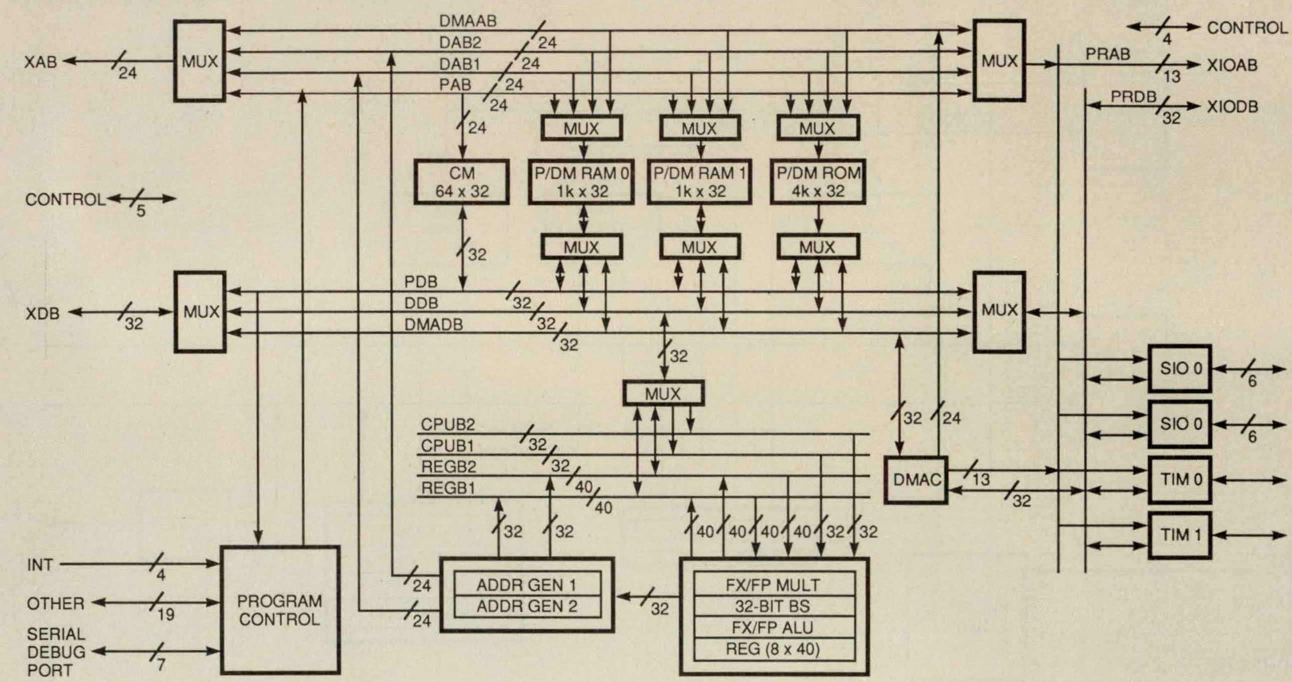
AVAILABILITY: The C30 and C30-27 are available now. The C31 will begin sampling in 1991.

COST: C30, $130; C30-27, $100; C31, $85 (1000).

SECOND SOURCE: None.

Texas Instruments Inc
Semiconductor Group, SC-9026
Box 809066
Dallas, TX 75380
(800) 232-3200, ext 700
Circle No. 686

DESCRIPTION: This device is the floating-point member of the vendor's TMS320 family. It was the first sub-100-nsec 32-bit floating-point CMOS DSP. It is not code compatible with the fixed-point chips. The C30 is available in a slower, lower-cost version called the C30-27. The C31 is object-code compatible with the C30 and C30-27 but has only one serial port, one parallel port, and one timer. This feature reduction reduces the chip size and pin count, which allows TI to offer a floating-point DSP for $35 in high volume.

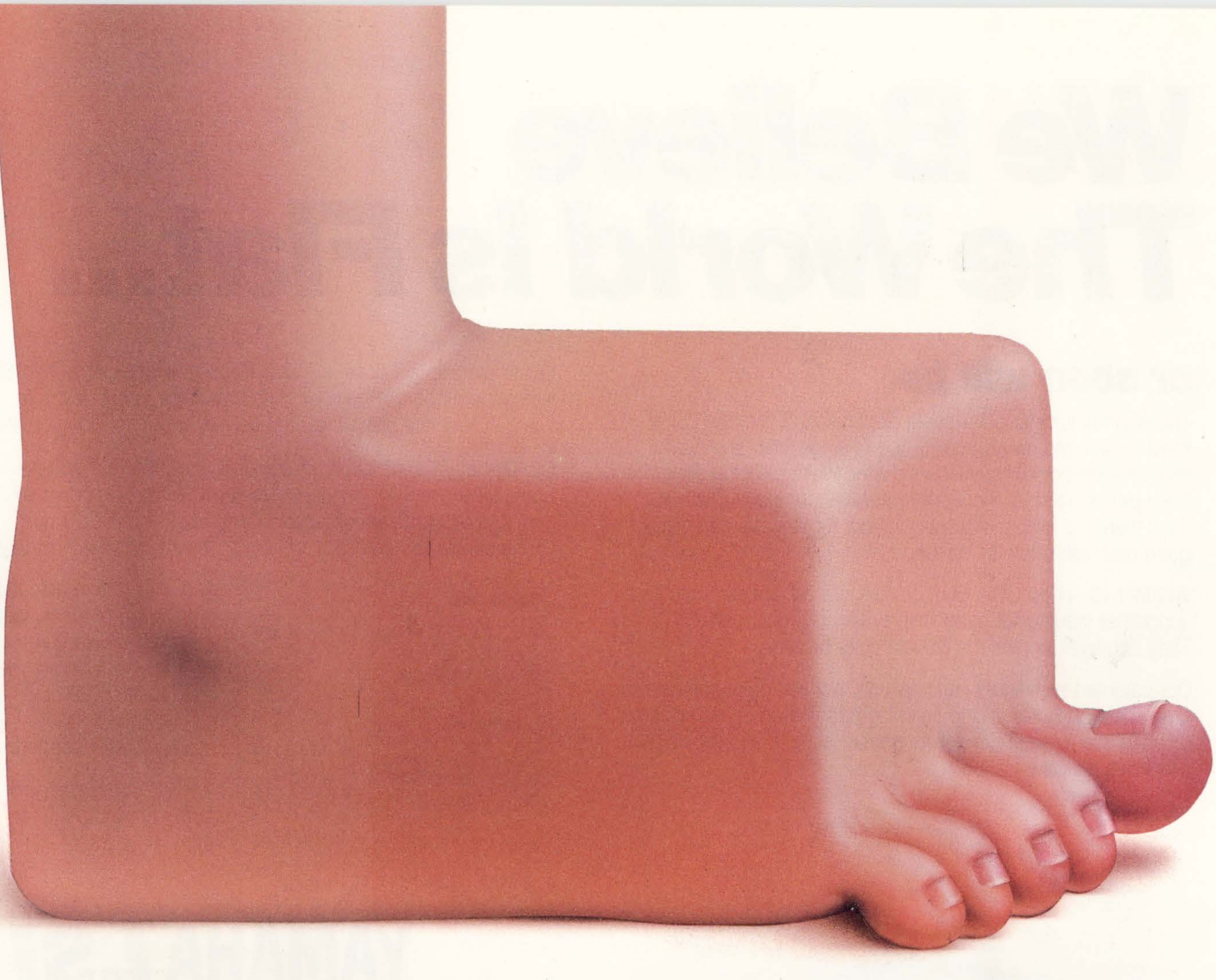


FEATURES: 60- and 75-nsec cycle-time versions.
Four 24-bit address buses and three 32-bit data buses.
Two 32-bit and two 40-bit additional buses in the CPU.
Separate program, data, and DMA buses.
Each internal RAM and ROM allows two accesses per cycle.
Any of the separate memories can be used for program or data.
Two on-chip 1k×32-bit RAMs and an on-chip 4k×32-bit ROM.
24-bit external memory-address bus provides 16M×32-bit total address space.
13-bit external-I/O address bus provides 8k×32-bit I/O ports, which are mapped into the 16M-byte address space.
Two 8-, 16-, 24-, and 32-bit serial I/O ports. Two 32-bit timers.
Proprietary 32-bit floating-point format.
Multiplier accepts 32-bit floating-point data and returns 40-bit floating-point result. 24-bit integers result in 32-bit fixed-point results.
ALU operates on 40-bit floating-point and 32-bit fixed-point data.
Parallel multiplier and ALU operations in a single cycle.
32-bit bidirectional barrel shifter.
Eight 40-bit register-based accumulators.
Single-instruction and zero-overhead block looping.
64×32-bit instruction cache.
Cache can be disabled when not needed and frozen to keep an often used portion of code available in the cache.
Register, direct, indirect, immediate, relative, circular, and bit-reversed addressing modes. Two address ALUs.
DMA controller allows concurrent I/O and CPU operation.
Hardware stack is maintained in main memory.
Four external vectored interrupts.
Hardware and software-programmable wait states.
Serial debug port can provide in-circuit emulation.
No low-power mode.
Packaging: C30, 180-pin PGA. C30-27, 180-pin PGA. C31, 132-pin quad flatpack.

HARDWARE — SUPPORT — SOFTWARE

Full-speed in-circuit emulator.
Software development system plugs into an IBM PC to give PC in-circuit emulation capability.
Evaluation module plugs into an IBM PC.
Significant third-party support. Contact manufacturer for a list of third-party vendors. Hewlett-Packard has a version of the HP64700 in-circuit emulator for the C30.

Optimizing ANSI C compiler. Source-level debugger.
Assembler/linker. Simulator.
Application library.
Third-party support includes real-time multitasking operating system (SPOX), Ada compiler, filter-design packages, and block-level diagraming language.



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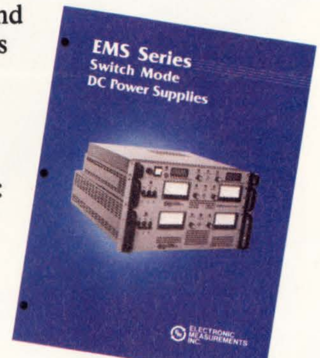

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CIRCLE NO. 103

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Our single-chip solutions are ideal for all new designs, especially laptops and portable devices. With four chips to choose from, you can have the distinct level of control and resolution you need.

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CIRCLE NO. 104

32-BIT FLOATING-POINT CMOS DSP μP

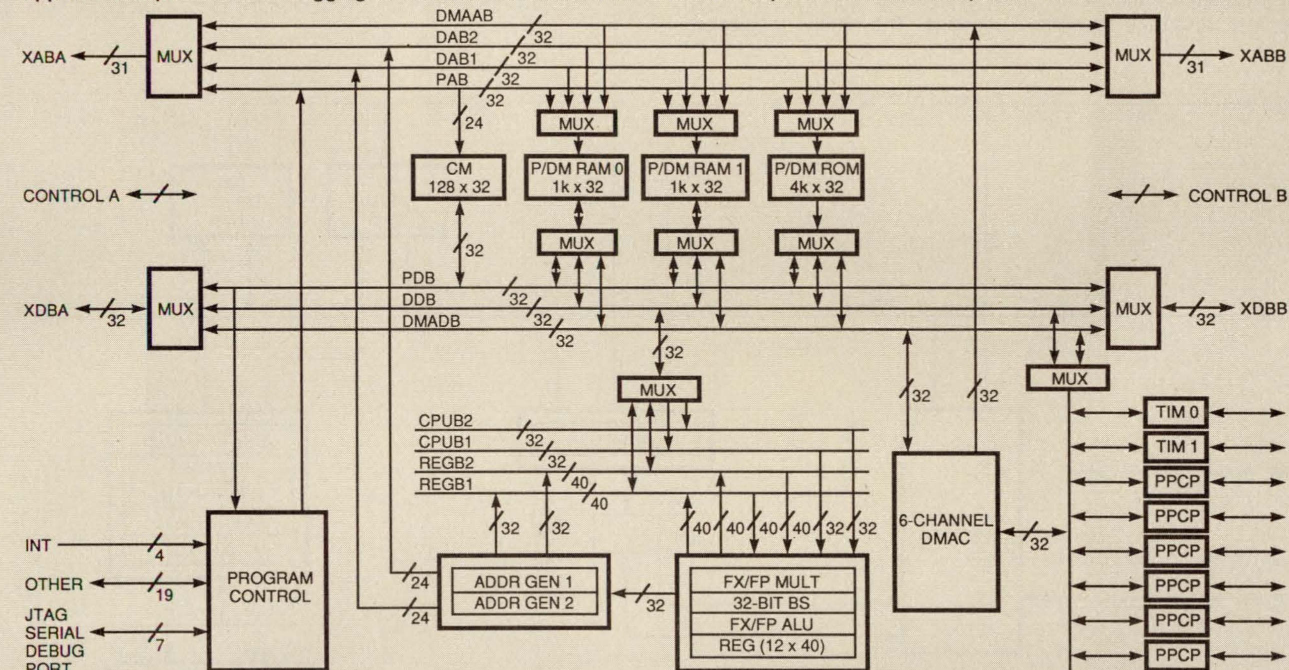
AVAILABILITY: Samples will be available the 2nd quarter 1991.

COST: Samples will cost approximately $500.

SECOND SOURCE: None.

Texas Instruments Inc
Semiconductor Group, SC-9026
Box 809066
Dallas, TX 75380
(800) 232-3200, ext 700
Circle No. 687

DESCRIPTION: This device was designed for applications that require multiple DSP chips. It is upward compatible with the C30 but adds six 32-bit FIFO-buffered communication ports, two complete 32-bit external buses, an analysis module that supports multiprocessor debugging via a JTAG interface, and a 4G-word address space. The chip also features single-cycle conversion to/from the IEEE floating-point standard and a cycle time of 40 nsec. Each communication port can transfer data to/from another C40 at 13M byte/sec without any external logic. The on-chip DMA has been expanded to six channels



FEATURES: 40-nsec cycle time.
Four 32-bit address buses and three 32-bit data buses.
Two 32-bit and two 40-bit additional buses in the CPU.
Separate program, data, and DMA buses.
Each internal RAM and ROM allow two accesses per cycle.
Any of the separate memories can be used for program or data.
Two on-chip 1k × 32-bit RAMs and a 4k × 32-bit ROM.
Dual 32-bit external buses. Each has a 31-bit address, so the 4G-word memory is equally divided between the two buses.
Six independent 32-bit communication ports for glueless communications between C40s. Separate 8 × 32-bit FIFOs for input and output buffering.
No on-chip serial ports. Two 32-bit timers.
Proprietary 32-bit floating-point format.
Single-cycle conversion from/to the IEEE-754 32-bit format.
Multiplier accepts 32-bit floating-point data and returns 40-bit floating-point data. 24-bit integers result in 32-bit fixed-point results.
ALU operates on 40-bit floating-point and 32-bit fixed-point data.
Parallel multiplier and ALU operations in a single cycle.
32-bit bidirectional barrel shifter.
Twelve 40-bit register-based accumulators.
Single-instruction and zero-overhead block looping.
128 × 32-bit instruction cache.
Cache can be disabled when not needed and frozen to keep an often used portion of code available in the cache.
Register, direct, indirect, immediate, relative, circular, and bit-reversed addressing modes. Two address ALUs.
6-channel DMA controller for concurrent I/O and CPU operation.
Transmitting DMA can control the operation of the receiving DMA, so setup for DMA transfer will not affect CPU.
Hardware stack maintained in main memory.
Four external vectored interrupts.
Hardware and software-programmable wait states.
JTAG-based debug port controls the analysis module, which functions as an in-circuit emulator. Multiple C40s can be debugged via JTAG interface.
No low-power mode.
Packaged in a 325-pin ceramic PGA.

HARDWARE — SUPPORT — SOFTWARE

Hardware:
Development system includes in-circuit emulation via JTAG interface.
4-processor host-independent evaluation board.

Software:
Optimizing ANSI C compiler with parallel-processing runtime support.
Source-level debugger. Assembler/linker. Simulator.
Application library.
Third-party support includes a real-time operating system (SPOX) with drivers for parallel processing.

ZR34325

32-BIT FLOATING-POINT CMOS DSP μP

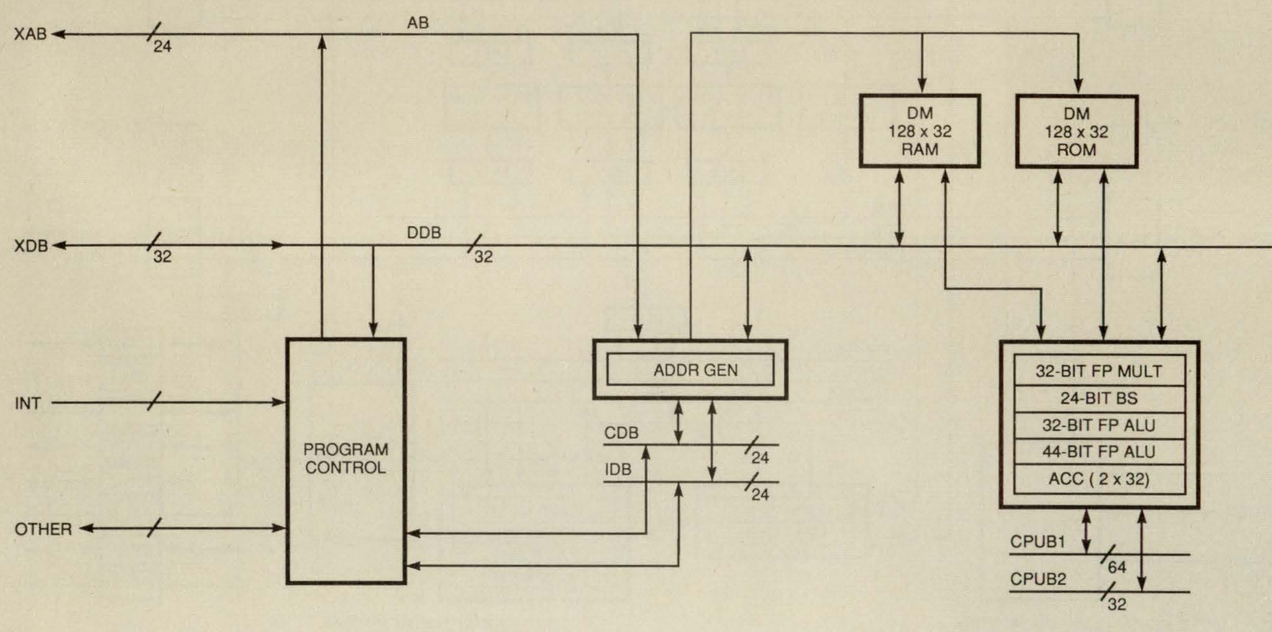
AVAILABILITY: Now.

COST: The 34325 (25 MHz) costs $137; the 34325 (20 MHz) costs $124 (10,000).

SECOND SOURCE: Harris Semiconductor (Melbourne, FL).

Zoran Corp
4401 Great America Pkwy
Santa Clara, CA 95054
(408) 986-1314
Circle No. 688

DESCRIPTION: The ZR34325 is a vector-signal processor, which is a DSP chip that operates on complex data and large blocks of data with single high-level instructions. The instruction set includes a single instruction to calculate an FFT, FIR filter, IIR filter, and other complex functions. The highly specialized architecture is optimized to perform these functions quickly. The architecture also eases programming because the programmer doesn't have to write code for complex DSP functions. The 32-bit floating-point data conforms to the IEEE-754 standard.



FEATURES: 80- and 100-nsec cycle-time versions.
Single address and data bus.
Vector instructions generally take longer to execute than to fetch, so little speed penalty is incurred with this simple bus architecture.
High-level instructions, such as those to calculate FFTs and FIR and IIR filters, simplify programming.
256×32-bit coefficient dual-port ROM and 128×32-bit dual-port RAM on chip.
No on-chip program memory.
Internal memory can be directly accessed by external device.
16M×32-bit memory space.
No on-chip peripherals.
IEEE-754 32-bit floating-point format.
Multiplier accepts 32-bit floating-point data and creates 44-bit results.
Three ALUs: two floating point and one integer. 32-bit floating-point data can be added to 32 bits with one ALU and to 44 bits with the other.
24-bit bidirectional barrel shifter.
Two 32-bit accumulators.
No zero-overhead looping.
Direct, indirect, register, immediate, circular, and bit-reversed addressing modes.
Address generators for internal RAM and ROM.
On-chip DMA.
Slave mode opens chip to external access.
Hardware stack maintained in main memory.
Single external interrupt.
Hardware wait states.
No on-chip emulation port.
No low-power mode.
Packaged in an 84-pin PGA.

HARDWARE — SUPPORT — SOFTWARE

Hardware-development-system board for IBM PCs.
VMEbus-based product for development. Does not include in-circuit emulation.
Third-party hardware becoming available.

Assembler/linker.
Application library.
Simulator.

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- ▼ Complex, sequential triggers, loaded without slowing the emulator or target.
- ▼ Access to the fully qualified trace buffer during full-speed emulation.
- ▼ High level language debug.
- ▼ Probe kits for 386, SX, 376 and 286 support.

Most in-circuit emulators require partially or completely functional hardware to operate correctly. MICE-V-486 has a unique *Isolation Mode*™, requiring only a working clock signal. Logic analyzer taps are conveniently located to give you access to critical timing information. *MICE-V-486 provides absolutely the fastest method for debugging non-functional 486-based hardware.*

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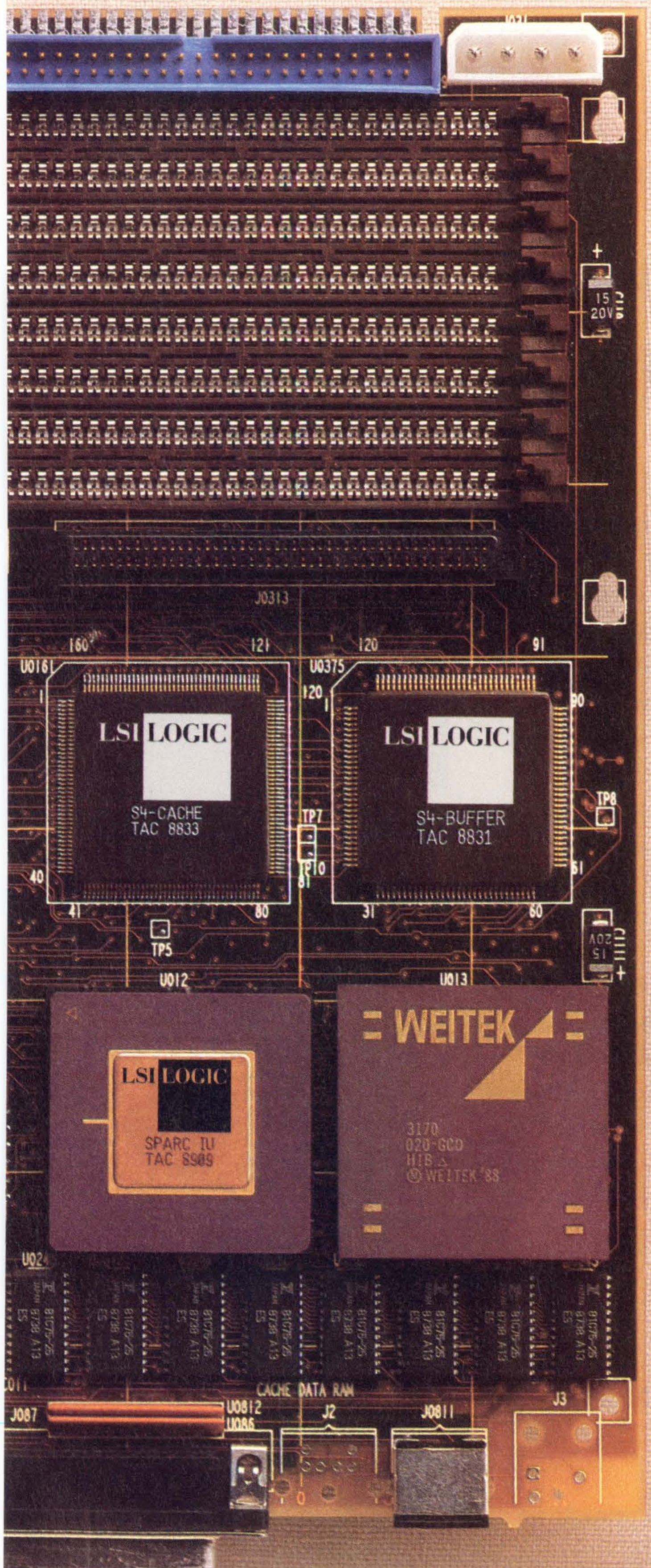
CIRCLE NO. 105



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MSM10S05XX	22K	208		120 to 208	108 to 208
MSM10S09XX	36K	272		144 to 272*	108 to 256
MSM10S11XX	47K	304		144 to 304*	132 to 301
MSM10S18XX	72K	384		144 to 304*	208 to 340
MSM10S23XX	92K	424		144 to 304*	240 to 340

[1]Other products are under development
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CIRCLE NO. 107

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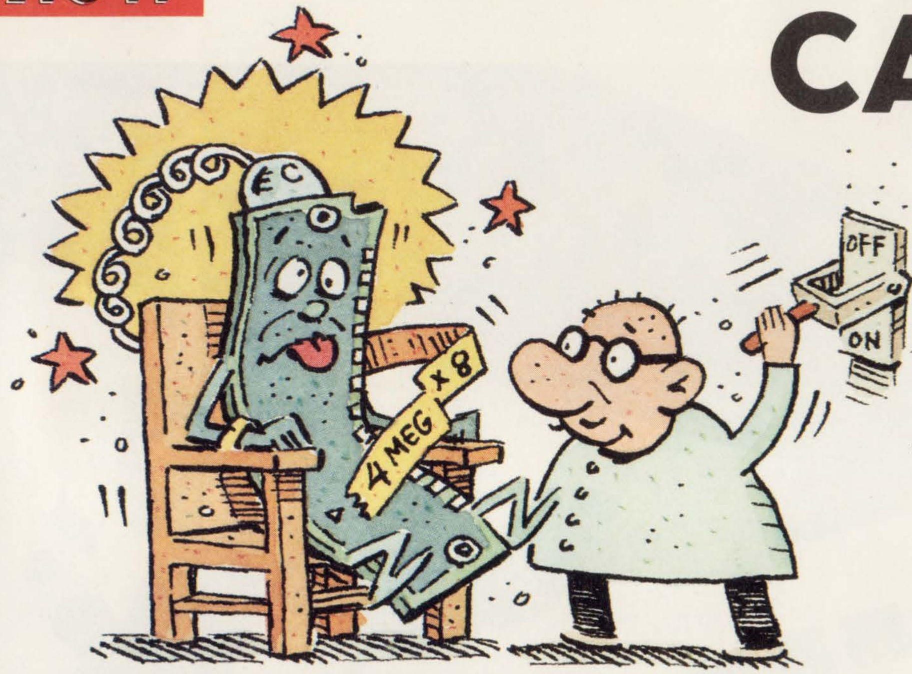

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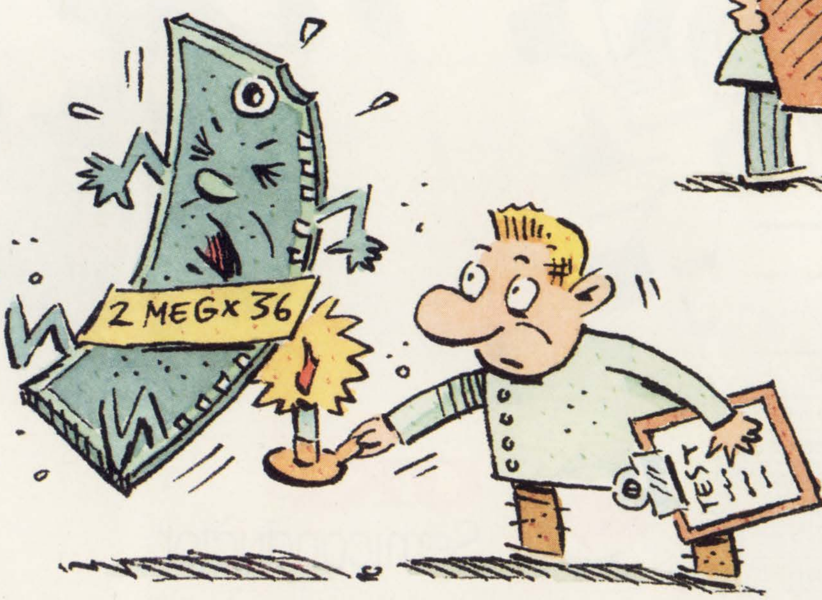

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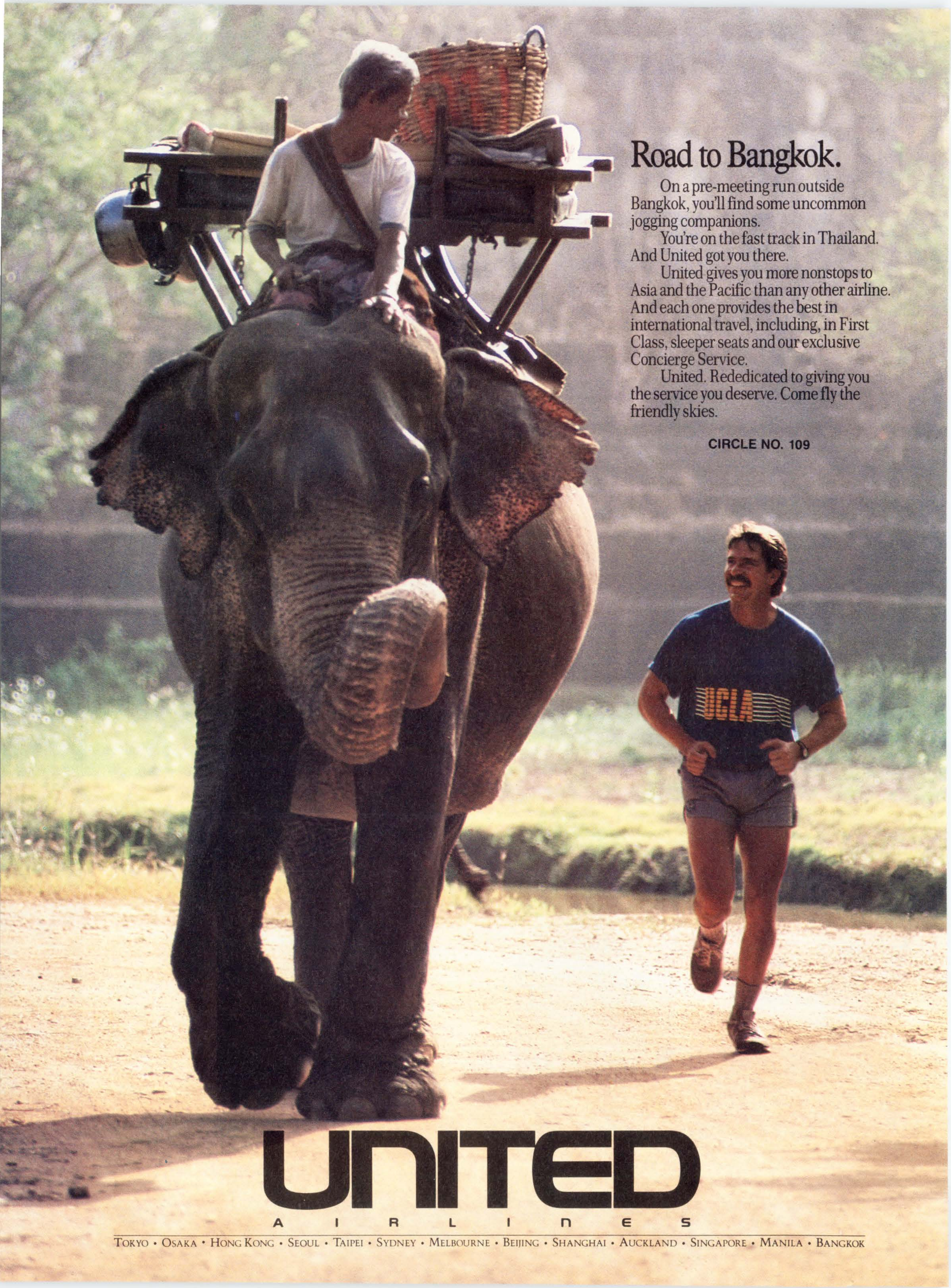
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EEPROMs enhance microcontroller-based system performance

The ability to update either the program memory or the data memory in an EEPROM can increase the performance of microcontroller-based systems, ease system-reconfiguration tasks, and improve overall system flexibility.

Richard Orlando, *Xicor Inc*

Many systems comprise a single-chip microcontroller (μC) and an external program memory—typically an EPROM. Today, the availability of 64k-bit EEPROMs makes them a viable replacement for EPROMs. EEPROMs' advantages are many. An EEPROM allows you to update system software without removing the memory device. This feature can be beneficial when you have to change the software at different stages of the manufacturing cycle or after the system is in the field. The EEPROM can accommodate self-modifying software, which will allow the system to tailor itself to the environment even if the environment changes. You can also use the EEPROM as a nonvolatile data-storage device for system parameters.

The task of integrating an EEPROM into a single-chip μC-based system is not trivial. This article will give an overview of the general design requirements for using EEPROMs in these types of systems. The discussion will cover some specific solutions to the problems encountered when implementing designs using the two predominant μC architectures, the Von Neumann and the Harvard.

Modern EEPROMs have several unique properties that you must take into consideration when doing any type of circuit design. The first of these properties is data integrity during power up and power down.

You can write to today's EEPROMs as easily as you can write to a RAM. However, if circuitry external to the EEPROM inadvertently generates the proper signals for a write operation (Chip Enable Low, Output Enable High, and Write Enable Low), problems can occur. Whenever the EEPROM recognizes these signals, it will initiate an inadvertent write cycle. Because this write operation is accidental, the data and address information are meaningless, and you wind up overwriting meaningful EEPROM data.

The fact that many single-chip μCs do not behave well during power up and power down compounds the inadvertent write problem. Holding the μC's Reset input low does not always guarantee the output states. All of the newest EEPROMs feature some kind of V_{CC} sensor that disables the chip when the supply voltage drops below a specified point, but even this scheme does not provide sufficient protection. To avoid the inadvertent write problem, you must add external circuitry to the EEPROM—a fix that general EEPROM literature covers in detail.

The software-data-protection feature found in the newest generation of EEPROMs provides an excellent solution to the inadvertent write problem. It allows the chip to initiate a write cycle only after a 3-step software sequence enables it. Because the chip powers

Many single-chip μCs do not behave well during power up and power down.

up in the disabled mode and disables itself after each write operation, you need no external hardware to protect the EEPROM during power up and power down. The chip can perform a write operation only when it is actually being given a valid write-enable command sequence followed by a valid write cycle.

An EEPROM characteristic that is even more troublesome than the inadvertent write characteristic is the manner in which the chip responds during the relatively long internal write cycle. The EEPROM's writing cycle is an actual byte or page-programming sequence, so the chip enters a read-disabled mode during the programming interval. Attempts to access data from the chip during the write cycle will most assuredly not yield the proper data until the write cycle is complete. If a single-chip μC, or any processor for that matter, tries to read an opcode out of the same EEPROM to which it is currently writing, the result can be disastrous. Even processors that use Hex FF as a restart opcode will continue trying to restart until the EEPROM finishes writing. Then, however, the current status of the system is lost during reinitialization.

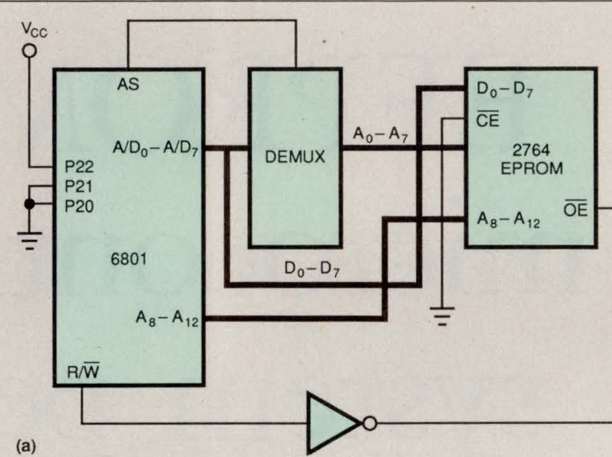
You can solve the disabled-read problem by using two EEPROMs for program storage. But make sure that each EEPROM contains a copy of the EEPROM write routine, which allows the processor to execute code out of one device while concurrently updating the other. Of course, this solution does increase your system's parts count.

Your system design must provide an area that allows you to execute code while you are writing to the EEPROM. System implementation will vary with the characteristics of the μC family you use. The Von Neumann and the Harvard methods are the two main μC architectures in vogue today, and each must be handled differently when it comes to adding external circuitry.

Simplifying the access operation

Uniform address space is the main characteristic of the Von Neumann architecture. The processor accesses a single address space, which contains both program storage and data storage. I/O devices are also mapped into certain locations. Although certain addresses are reserved for such things as internal RAM or ROM, the address space itself is uniform. The processor can read and write to program-storage locations as well as execute instructions from data memory. Motorola uses this single-chip architecture in its 68XX family.

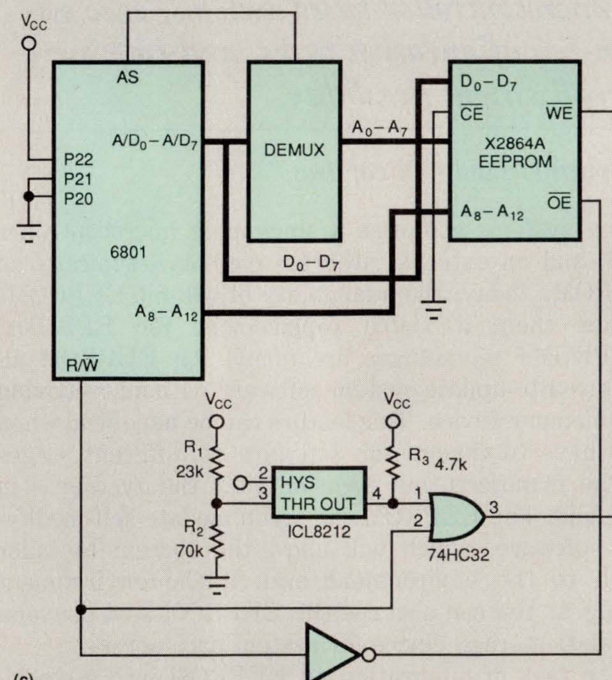
Fig 1a shows a typical 3-chip system based on a



(a)

	INSTRUCTION			NUMBER OF BYTES
WRITE-AND-WAIT:	STA	A O,X	;WRITE BYTE TO ;EEPROM	2
TEST:	CMP	A O,X	;CHECK FOR VALID DATA	2
	BNE	TEST	;WAIT	2
	RTS		;RETURN TO MAIN	1
			TOTAL BYTES	7

(b)



(c)

Fig 1—The classical approach to providing memory capability *for a μC employs an EPROM **(a)**. You only need 7 bytes of memory to store a simple write-and-wait routine **(b)** for the 6801. To replace the EPROM with an EEPROM **(c)**, you need to add power-up/power-down protection and develop a write enable signal.*

6801 μC, an EPROM, and a demultiplexer, which separates the multiplexed address and data bus (A/D_0 to A/D_7). Before replacing the EPROM with an EEPROM, you'll have to install the additional, external power-up and power-down protection circuitry and make provisions for a temporary memory space for instructions that the processor can execute during the write cycle. This memory space need not be large; it only has to hold the actual write-operation instructions and have a wait routine to hold up the processor until the EEPROM completes the write operation. The software is quite compact if you implement this design with second-generation EEPROMs (X2816C, X2864B, and X28256), which feature $\overline{DATA}$ polling or a toggle bit.

By using the $\overline{DATA}$ polling, you'll only need 7 bytes of memory to execute the software subroutine shown in **Fig 1b**. Because the 6801 has 128 bytes of internal RAM, you can load the program segment into RAM and follow with a branch to this subroutine when you need to perform a write operation, which yields the design shown in **Fig 1c**. The EEPROM implementation requires the addition of only the power-up/power-down protection circuitry and the Write Enable signal.

If the application uses all the internal RAM, you'll have to add a small external RAM or PROM to hold the subroutine. A 1k-bit PROM will be sufficient because you only need 7 bytes of storage capability (**Fig 2**). If the application requires a large amount of program storage, you can use two EEPROMs and load the write routine into each device. The main update program will determine which EEPROM will receive the byte to be modified; it jumps to the appropriate subroutine in the other EEPROM. You can use this technique to update either program bytes in the EEPROM or operational parameters.

The Von Neumann architecture is well suited for these types of applications because of its compatibility with the applications' requirements, specifically, the existence of the signals required for writing into the program address space. If the application allows you to use the internal RAM, you should write the 7 bytes of code into the RAM from the EEPROM before doing anything else. Because the EEPROM write-and-wait routine is position independent, you can also dynamically determine the routine's position in RAM based upon the location and size of the stack and other dynamic data structures in use.

Whether you use some or all of your system RAM, you must take care to either disable all interrupts or make sure to locate the interrupt-handling routine so that it can be easily accessed during the write cycle. This can be a tricky task in the case of the Non-Maskable Interrupt (NMI) on the 6801 because addresses $FFFC_{16}$ and $FFFD_{16}$ must always be available during the write routine in case an interrupt occurs during the write cycle. To solve this problem, point the interrupt vector to a temporary subroutine, which first determines if the EEPROM is involved in a write cycle. If it is, the interrupt-handling routine waits until the write cycle finishes and then jumps to the actual interrupt-handling procedure stored in EEPROM. The toggle-bit feature of EEPROMs is valuable here because the data that you wrote into the EEPROM may no longer be in the accumulator.

The toggle bit works as follows. During repeated read cycles to the chip, I/O_6 will toggle between 1 and 0 on each consecutive read cycle if the chip is performing an internal write cycle. The pseudo interrupt-handling routine shown in **Fig 3** will determine if a write operation is in progress and wait until the write cycle ends before jumping to the real interrupt service procedure. Since the code shown is re-entrant, there should be no problem with multiple interrupts during the EEPROM write cycle as long as the stack does not

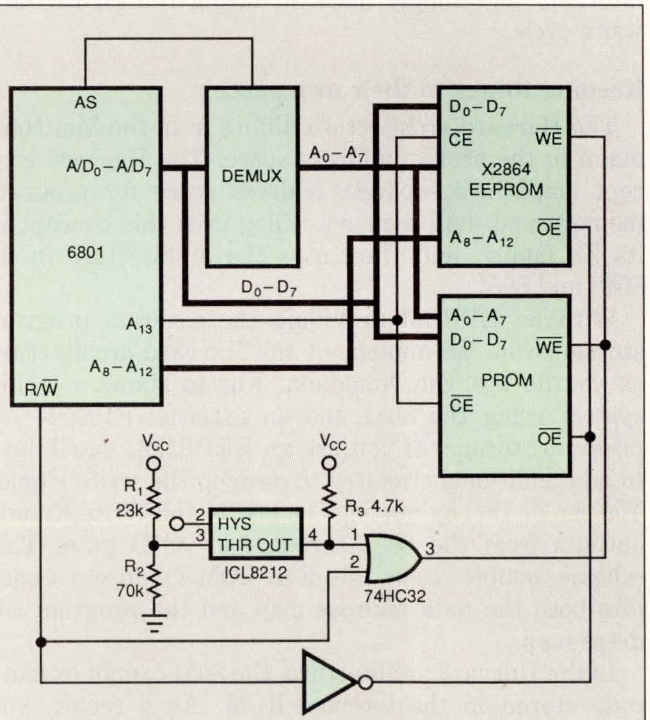


Fig 2—If you need some additional memory *to hold the write-and-wait routine for the 6801, you can use a small external PROM.*

The Harvard architecture differs from the Von Neumann architecture in the area of address space.

```
                                              NUMBER
                INSTRUCTION                   OF BYTES

NMI-VECTOR:  LDA   A          ;READ EEPROM          3
                   EEPROM
             CMP   A          ;COMPARE DATA         3
                   EEPROM     ;TOGGLE BIT ENSURES
                              ;DATA DIFFER IF
                              ;EEPROM IS BUSY
             BNE   NMI-
                   VECTOR     ;WAIT                 2
             JSR   REAL-NMI   ;WHEN CYCLE
                              COMPLETE              3
                              ;JUMP TO INTERRUPT
             RTI              ;RETURN FROM INTERRUPT 1

                              TOTAL BYTES  12
```

***Fig 3—To avoid interrupt problems** in the EEPROM, this pseudo interrupt-handling routine will determine if a write cycle is in progress and wait until the cycle is complete before jumping to the real interrupt service procedure.*

overflow. If there's a chance that too many interrupts might occur during the 10-msec write cycle, it might be advisable to use the toggle-bit signal as a maskable interrupt and simply mask it during the EEPROM's write cycle.

Keeping things in their own space

The Harvard architecture differs from the Von Neumann in the area of address space. The Harvard concept employs a separate address space for program memory and data memory. Zilog uses this concept in its Z8 family, and Intel uses the architecture in its 8048 and 8051.

With an EPROM providing the external program storage, you can implement the Harvard architecture as you do the Von Neumann. **Fig 4a** shows a 3-chip system using the 8051 and an external EPROM for program storage. If you use an EEPROM, you'll have to add additional circuitry to develop the write signal. You can do this by putting the PSEN and Write Enable outputs from the 8051 through an AND gate. This scheme double-maps the EEPROM's address space into both the data address map and the program address map.

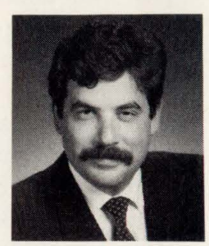
In the Harvard architecture, the 8051 cannot execute code stored in the internal ROM. As a result, you must add an external memory to provide temporary storage for the EEPROM's write-and-wait routine. You can use a small RAM, again double-mapped into the program and data address spaces, or a small PROM. The small write routine for the 8051 helps minimize the size needs of the external memory. **Fig 4c** shows the write-and-wait routine for the 8051.

Fig 4b shows the actual hardware implementation of an 8051/EEPROM system. The additional circuitry—an AND gate for the Write Enable derivation, the power-up/power-down protection circuitry, and the small external memory to hold the above write-and-wait routine—serves to convert the EPROM-based design into a EEPROM-based design. If the external memory is a RAM, you should copy the write-and-wait routine from the EEPROM to the RAM when you initialize the system and before you make any attempt to write to the EEPROM.

In the case of the 8051, it's possible to disable all interrupts by setting the EA to 0 prior to jumping to the EPROM's write-and-wait routine. If you need interrupt-processing capability during the EEPROM write interval, take care to ensure that the extra memory resides at the top of the address map (starting at address 0000) because you must locate the interrupt vectors at the lowest addresses in program memory in the 8051.

In older Harvard-architecture µCs such as the 8048, you can use essentially the same EEPROM-based system design as you did for the 8051. The only difference is that the write-and-wait routine is slightly longer for 8048-type devices because the high-order addresses must be set up on an I/O port prior to executing the write operation. **Fig 4d** shows a sample subroutine, which you can use to implement the write-and-wait operation for the 8048. EDN

Author's biography



Richard Orlando is director of marketing at Xicor Inc (Milpitas, CA). In this position, he is responsible for strategic and product planning. Richard holds a BSEE degree in computer systems engineering from the University of Massachusetts/Amherst and is a member of ACM, IEEE Computer Society, Eta Kappa Nu, and Tau Beta Pi. Richard's leisure activities include programming and music.

Article Interest Quotient (Circle One)
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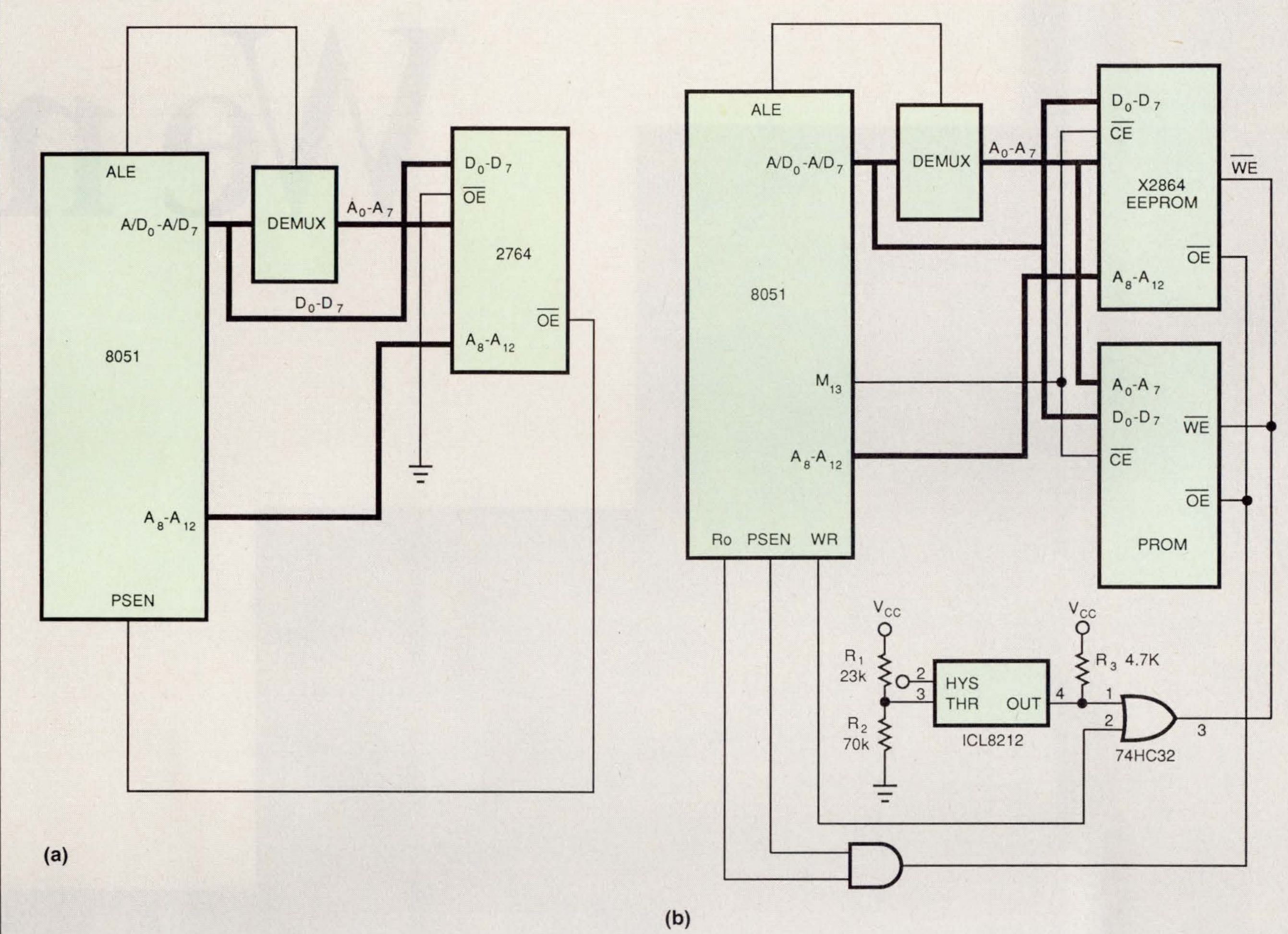


WRITE-AND-WAIT:	INSTRUCTION			NUMBER OF BYTES
WRITE-AND-WAIT:	MOVX	@DPRT,A	;WRITE BYTE TO EEPROM	1
TEST:	MOVX	A,@DPTR	;READ DATA	1
	MOV	R1,A	;STORE TEMPORARY	2
	MOVX	A,@DPTR	;READ DATA	1
	CJNE	A,R1,TEST	;IF EQUAL CYCLE COMPLETE	3
	RET		RETURN TO MAIN	1
			TOTAL BYTES	9

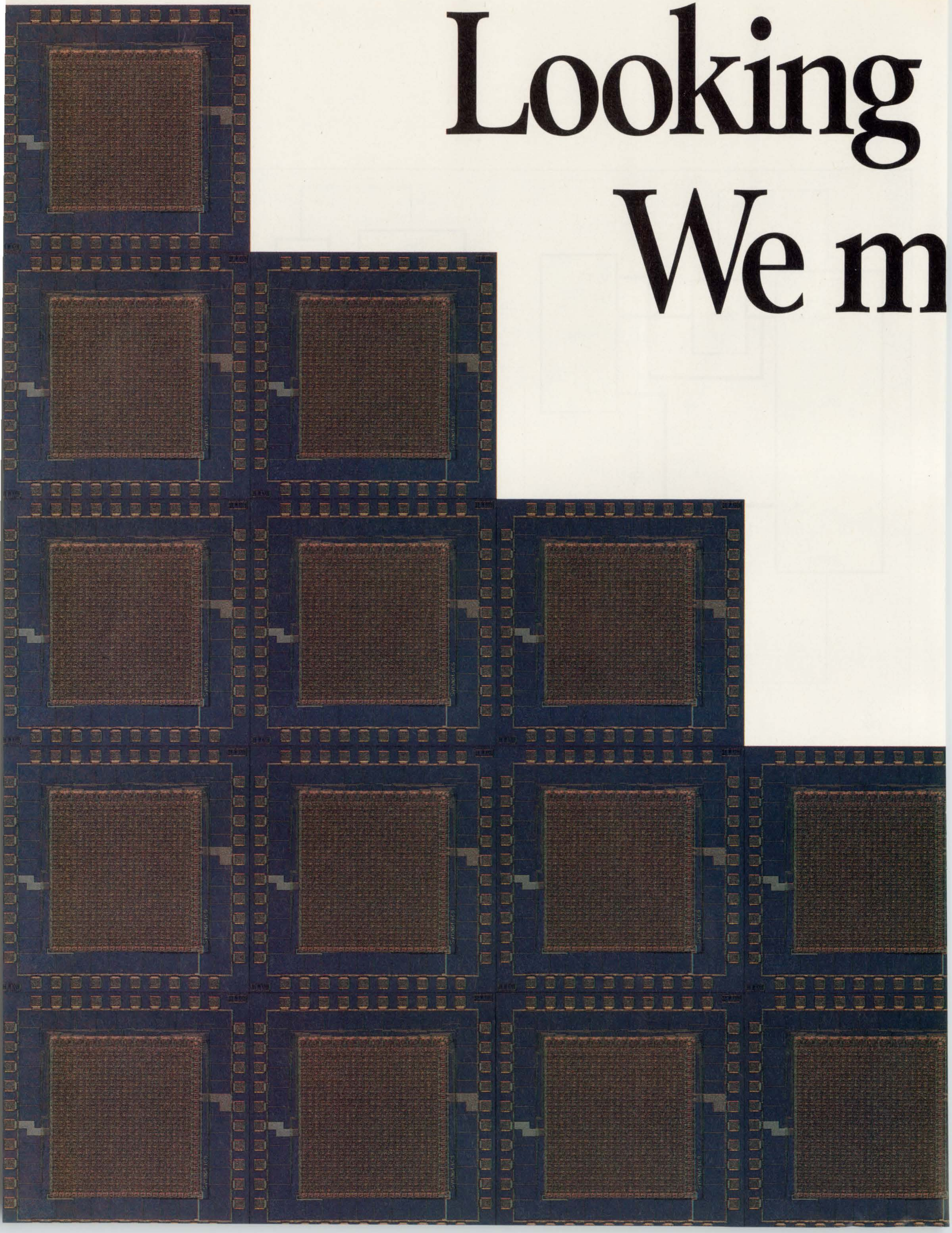
(c)

	INSTRUCTION			NUMBER OF BYTES
WRITE-AND-WAIT:	XCH	A,R2	;SWAP MSB OF ADDRESS	1
	OUTL	P2,A	;OUTPUT MSB OF ADDRESS	1
	XCH	A,R2	;SWAP DATA BACK	1
	MOVX	@RO,A	;WRITE BYTE TO EEPROM	1
TEST:	MOVX	A,@RO	;READ DATA	1
	XCH	A,R2	;SWAP TO R2	1
	MOVX	A,@RO	:READ DATA	1
	XRL	A,R2	;COMPARE DATA	1
	JNZ	TEST	;WAIT IF NOT EQUAL	2
	RETR		;RETURN TO MAIN	1
			TOTAL BYTES	10

(d)

Fig 4—An EPROM can provide external storage *capability for a Harvard-type μC like the 8051* ***(a)****. However, you can increase system performance by going with an EEPROM* ***(b)****. The additional EPROM can hold the write-and-wait routines shown in* **c** *and* **d** *for the 8051 and 8048 controllers, respectively.*

Looking
We m

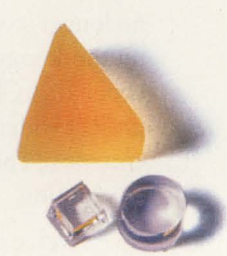


Imagine

Pure.

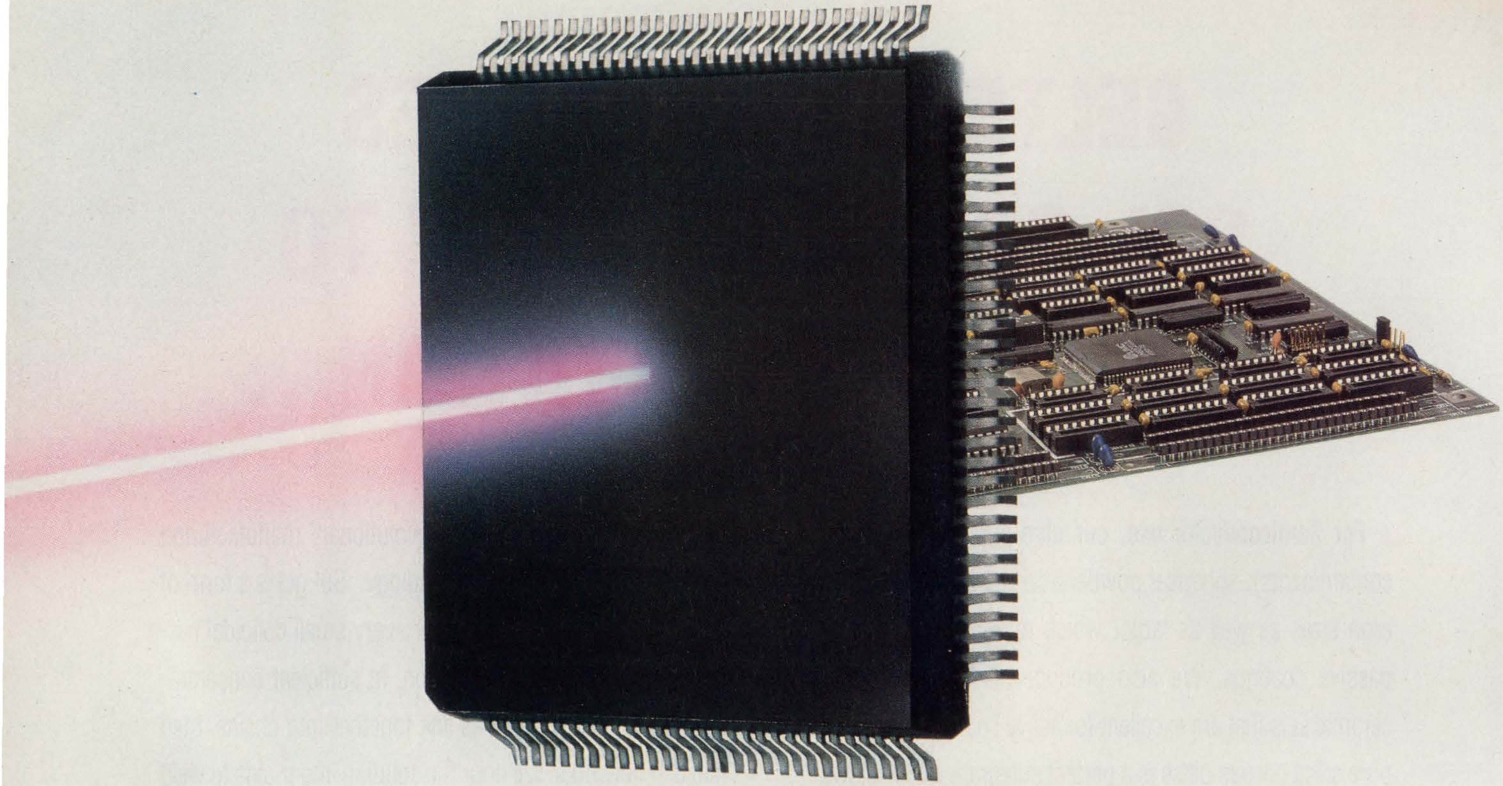
Imagine

Small.



Imagine

Silica.



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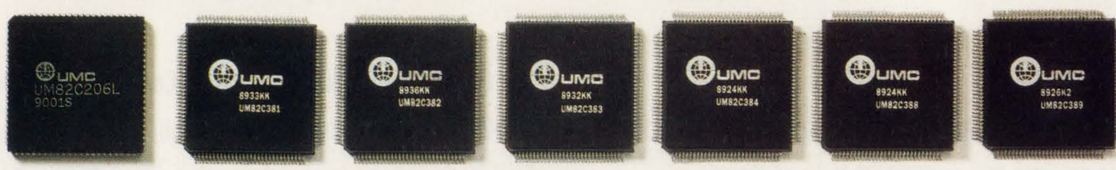

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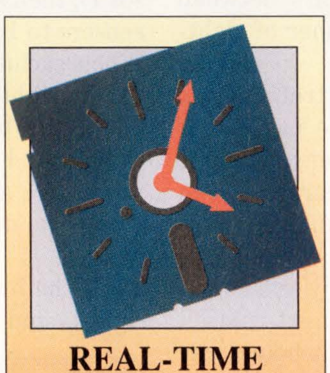
Developing real-time requirements

To design a real-time application, you must prepare a requirements model for your system and then transform it into an implementation model. Part 3 of this series explains how to create verbal and graphical requirements models that formulate system behavior as clearly, completely, and correctly as possible.

David L Ripps, *Industrial Programming Inc*

Developing a real-time application—or any other computer program—consists of translating a set of notions of what the system should do into a set of program modules that implement those notions. The translation normally proceeds in stages. In the early stages, vague notions of system behavior evolve into a formal statement of the specific system requirements. These requirements are often formulated as abstract models of the desired system behavior.

Ideally, the requirements model should express pure behavior. It should neither reflect the way the model is to be implemented nor bias the implementation in any way. Nevertheless, it would be senseless to include any requirements that cannot be met with any available means of implementation.



REAL-TIME PROGRAMMING PART 3

The requirements model can have a variety of formats, each aimed at clarifying some aspect of the system behavior. For example, some emphasize the flow and transformation of data, while others highlight the internal transitions caused by the arrival of inputs. Often several different formats jointly constitute the overall requirements model. As a minimum, the requirements model must show:

- The inputs to the system, differentiating continuously available inputs from transient ones.
- The various items of data that must be stored.
- The internal states that the system can attain.
- The actions that must be taken when the system is in a given state and a certain input arrives. Actions include changes in stored data, generation of outputs, and change of internal state.

The goal of the requirements model is to formulate system behavior as clearly, completely, and correctly as possible. "Clearly" means that there is no doubt as to what the system will do when it is presented with a given time profile of inputs. "Completely" means that all possible combinations of inputs have been considered. "Correctly" means that those who understand the purpose for which the application is being built agree that the actions are appropriate.

With such goals, the language used to express the inputs, stored data, internal states, and outputs is normally drawn from the problem arena and makes sense to people conversant with that field. Thus, the requirements for a telephone switch use the vocabulary of telephony. For problems arising from ordinary life, ordinary English is the language of choice.

Developing a verbal requirements model

As a way to illustrate the stepwise evolution of a requirements model, consider how to control access to a single-lane bridge that is shared by both lanes of

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a dual-lane road (**Ref 1**). Lights RB and LB control access to the bridge from the left-bound and right-bound directions, respectively. Traffic flow is light so that most of the time the bridge is in its initial (empty) state. In that state both lights are red (**Fig 1**).

For expressing real-time problems arising from ordinary life, ordinary English is the language of choice.

Start by writing the rules governing the system in purely verbal form:

1.1 If the bridge is not in use and a right-bound car approaches (as detected by sensor 1), then set the number of right-bound cars between sensors to 1, mark the bridge in use by right-bound traffic, and turn light RB green.

1.2 If the bridge is in use by right-bound traffic and a right-bound car approaches, then increase the number of right-bound cars between sensors by 1.

1.3 If the bridge is in use by right-bound traffic and a left-bound car approaches, then increase the number of left-bound cars between sensors by 1 but take no further action. (Light LB remains red.)

1.4 If the bridge is in use by right-bound traffic and a right-bound car leaves the bridge (as detected by sensor 2) and the number of right-bound cars between sensors is not 1, then decrement the number of right-bound cars between sensors by 1.

1.5 If the bridge is in use by right-bound traffic and a right-bound car leaves the bridge and the number of right-bound cars between sensors is 1, then turn light RB red, set the number of right-bound cars between sensors to 0, and mark the bridge not in use. If at that point the number of left-bound cars between sensors is not 0, then mark the bridge in use by left-bound traffic and turn light LB green, as in the next rule.

1.6 If the bridge is not in use and a left-bound car approaches (as detected by sensor 3), then set the number of left-bound cars between sensors to 1, mark the bridge in use by left-bound traffic, and turn light LB green.

1.7 If the bridge is in use by left-bound traffic and a left-bound car approaches, then increase the number of left-bound cars between sensors by 1.

1.8 If the bridge is in use by left-bound traffic and a right-bound car approaches, then increase the number of right-bound cars between sensors by 1 but take no further action. (Light RB remains red.)

1.9 If the bridge is in use by left-bound traffic and a left-bound car leaves the bridge (as detected by sensor 4) and the number of left-bound cars between sensors is not 1, then decrement the number of left-bound cars between sensors by 1.

1.10 If the bridge is in use by left-bound traffic and a left-bound car leaves the bridge and the number of left-bound cars between sensors is 1, then turn light LB red, set the number of left-bound cars between sensors to 0, and mark the bridge not in use. If at that point the number of left-bound cars between sensors is not 0, then mark the bridge in use by right-bound traffic and turn light RB green, as in the first rule.

One way to test a behavioral model for a real-time application is to ask whether the model provides the proper response when two or more asynchronous inputs are presented simultaneously. In this case, suppose the bridge is not in use and both a right-bound car and a left-bound car approach at exactly the same time. Both rules 1.1 and 1.6 should be applied, and their actions conflict. Each calls for marking the status of the bridge in a different way. Worse, each sends a car onto the bridge in opposing directions. Thus, this first attempt at a behavioral model fails because of the essential real-time nature of the problem. You can readily correct the model by requiring exclusive access to the bridge before the status or any other data is altered:

2.1 If the bridge is idle or in use for left-bound traffic and a right-bound car approaches (as detected by sensor 1), then set the number of right-bound cars between sensors to 1 and request exclusive access to the bridge. When exclusive access is granted, mark the bridge in use by right-bound traffic and turn light RB green.

2.2 If the bridge is in use by right-bound traffic or right-bound traffic is waiting for exclusive access to the bridge and a right-bound car approaches, then increase the number of right-bound cars between sensors by 1.

2.3 If the bridge is in use by right-bound traffic and a right-bound car leaves the bridge (as detected by sen-

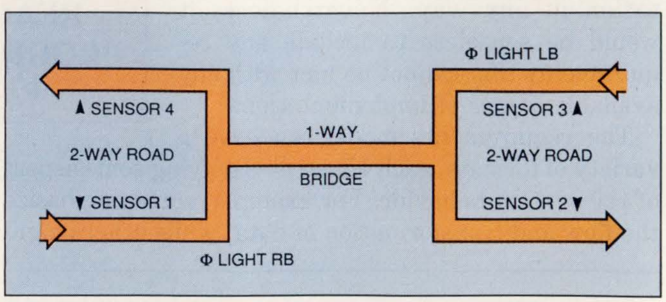

Fig 1—Access to a 1-lane bridge on a 2-lane road illustrates the application of a hypothetical traffic-control system that works in real time.

sor 2) and the number of right-bound cars between sensors is not 1, then decrement the number of right-bound cars between sensors by 1.

2.4 If the bridge is in use by right-bound traffic and a right-bound car leaves the bridge and the number of right-bound cars between sensors is 1, then turn light RB red, set the number of right-bound cars between sensors to 0, mark the bridge not in use by right-bound traffic, and release exclusive access to the bridge.

2.5 If the bridge is idle or in use for right-bound traffic and a left-bound car approaches (as detected by sensor 3), then set the number of left-bound cars between sensors to 1 and request exclusive access to the bridge. When exclusive access is granted, mark the bridge in use by left-bound traffic and turn light LB green.

2.6 If the bridge is in use by left-bound traffic or left-bound traffic is waiting for exclusive access to the bridge and a left-bound car approaches, then increase the number of left-bound cars between sensors by 1.

2.7 If the bridge is in use by left-bound traffic and a left-bound car leaves the bridge (as detected by sensor 4) and the number of left-bound cars between sensors is not 1, then decrement the number of left-bound cars between sensors by 1.

2.8 If the bridge is in use by left-bound traffic and a left-bound car leaves the bridge and the number of left-bound cars between sensors is 1, then turn light LB red, set the number of left-bound cars between sensors to 0, mark the bridge not in use by left-bound traffic, and release exclusive access to the bridge.

Note that it is no longer necessary to repeat the actions of rule 2.5 within rule 2.4 as was done in version 1 of this example (ie, "If at that point, the number of left-bound cars between sensors is not 0, then . . . , as in the next rule"). Those actions will automatically occur when exclusive access to the bridge is released and the other side is waiting for similar access.

You can make the model more precise by separating that information, which is to be stored as data from that which simply encodes an internal state. In particular, bridge status ("not in use for right-bound traffic," "not in use for left-bound traffic," etc.) just designates the internal state; it is not a stored variable. Thus, replace "If the bridge is in use by right-bound traffic" with "If in right-bound state Traffic Idle" and replace "mark the bridge in use by right-bound traffic" with "enter right-bound state Traffic Active."

In contrast, the number of left-bound cars between sensors must be stored and becomes the integer variable LB Cars. Similarly, "gain access to bridge" becomes "request semaphore variable Access to Bridge." Semaphores will be described in detail in Part 9 of this series. For now, it suffices to say that semaphores are variables that may be "free" or may be assigned to one requester or another. However, a given semaphore is never assigned to more than one requester at a time.

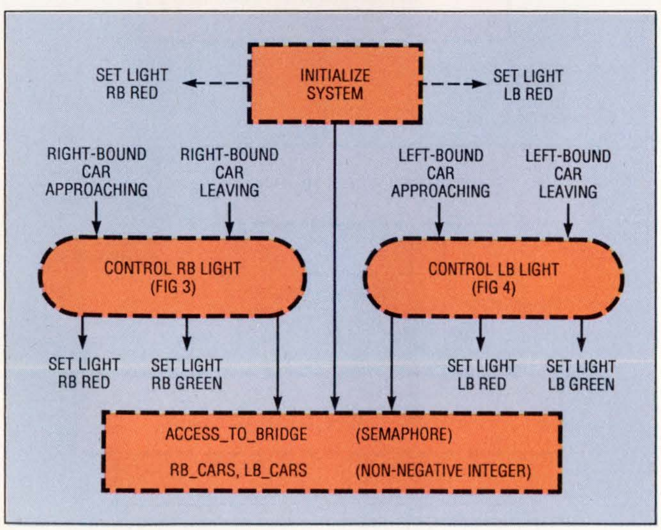

Fig 2—A graphical representation of control transformations recasts verbal descriptions into a more compact pictorial form that is easier to comprehend. Activities indicated in the diagram shown here refer to traffic control on the 1-lane bridge of Fig 1.

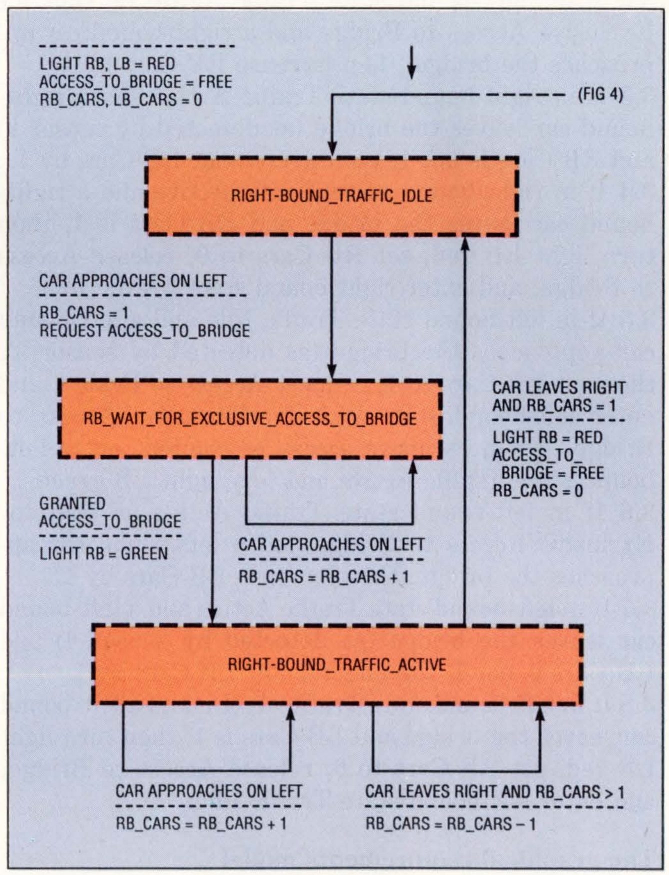

Fig 3—State-transition diagrams contain details that are hidden in control-transformation diagrams. This state diagram illustrates control of Fig 2's traffic light RB.

Thus, semaphores are used to achieve mutual exclusion.

To complete this demonstration of the evolution of a verbal requirements model, recast the verbal rules into a third and final version:

> The verbal expression of a behavioral model can be laborious to prepare and difficult to comprehend.

3.1 If in right-bound state Traffic Idle and a right-bound car approaches the bridge (as detected by sensor 1), then set RB Cars to 1, request Access to Bridge, and enter right-bound state Wait for Exclusive Access to Bridge. When exclusive access is granted, enter right-bound state Traffic Active and turn light RB green.

3.2 If in right-bound state Traffic Active or Wait for Exclusive Access to Bridge and a right-bound car approaches the bridge, then increase RB Cars by 1.

3.3 If in right-bound state Traffic Active and a right-bound car leaves the bridge (as detected by sensor 2) and RB Cars is not 1, then decrement RB Cars by 1.

3.4 If in right-bound state Traffic Active and a right-bound car leaves the bridge and RB Cars is 1, then turn light RB red, set RB Cars to 0, release Access to Bridge, and enter right-bound state Traffic Idle.

3.5 If in left-bound state Traffic Idle and a left-bound car approaches the bridge (as detected by sensor 3), then set LB Cars to 1, request Access to Bridge, and enter left-bound state Wait for Exclusive Access to Bridge. When exclusive access is granted, enter left-bound state Traffic Active and turn light LB green.

3.6 If in left-bound state Traffic Active or Wait for Exclusive Access to Bridge and a left-bound car approaches the bridge, then increase LB Cars by 1.

3.7 If in left-bound state Traffic Active and a left-bound car leaves the bridge (as detected by sensor 4) and LB Cars is not 1, then decrement LB Cars by 1.

3.8 If in left-bound state Traffic Active and a left-bound car leaves the bridge and LB Cars is 1, then turn light LB red, set LB Cars to 0, release Access to Bridge, and enter left-bound state Traffic Idle.

The graphical requirements model

As the previous sample suggests, the verbal expression of a behavioral model can be laborious to prepare and difficult to comprehend. Verbal rules also put a subtle bias into the implementation. For example, if the bridge is idle in both directions and cars approach from both sides simultaneously, the ordering of the statements suggests that you apply rule 3.1 before applying rule 3.5.

These deficiencies have led to the development of various graphical methods to show the behavior of real-time systems. The 3-volume set, *Structured Development for Real-Time Systems*, describes a series of techniques that you can apply manually to prepare a comprehensive set of graphical requirements models **(Ref 1)**. (Several companies currently offer alternative methods that employ a graphics workstation in place of paper and pencil. For a general review of computer-aided software engineering tools for real-time systems, see **Ref 2**.)

A full description of the graphical techniques is beyond the scope of this series. Nevertheless, you can get the flavor of the methods by recasting the verbal description into the "transformation schema" of Ward and Mellor **(Fig 2)**. The supporting state-transition diagrams appear in **Figs 3** and **4**.

In essence, each graphical method consists of a library of pictorial symbols that represent certain basic elements of the model. For the transformation schema **(Fig 2)**, dashed, rounded enclosures represent a transformation on transient binary information (events).

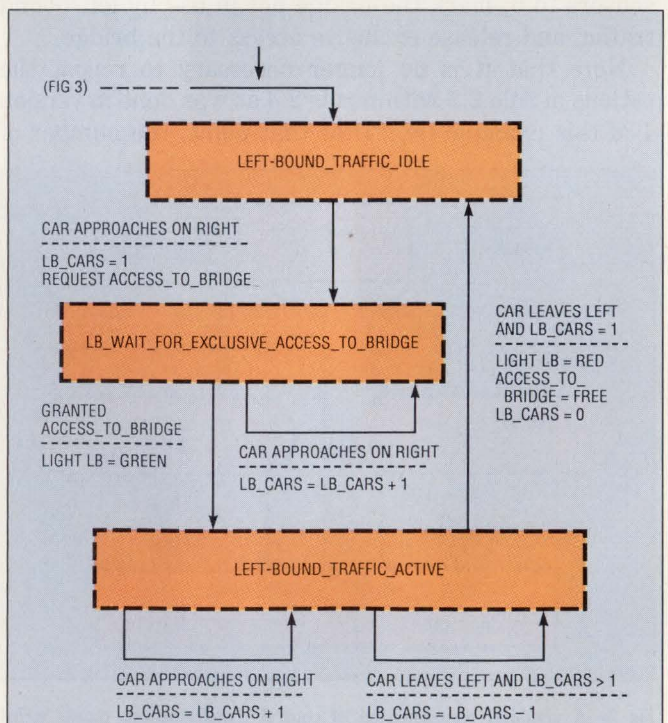

Fig 4—Details of traffic light LB appear in this state diagram.

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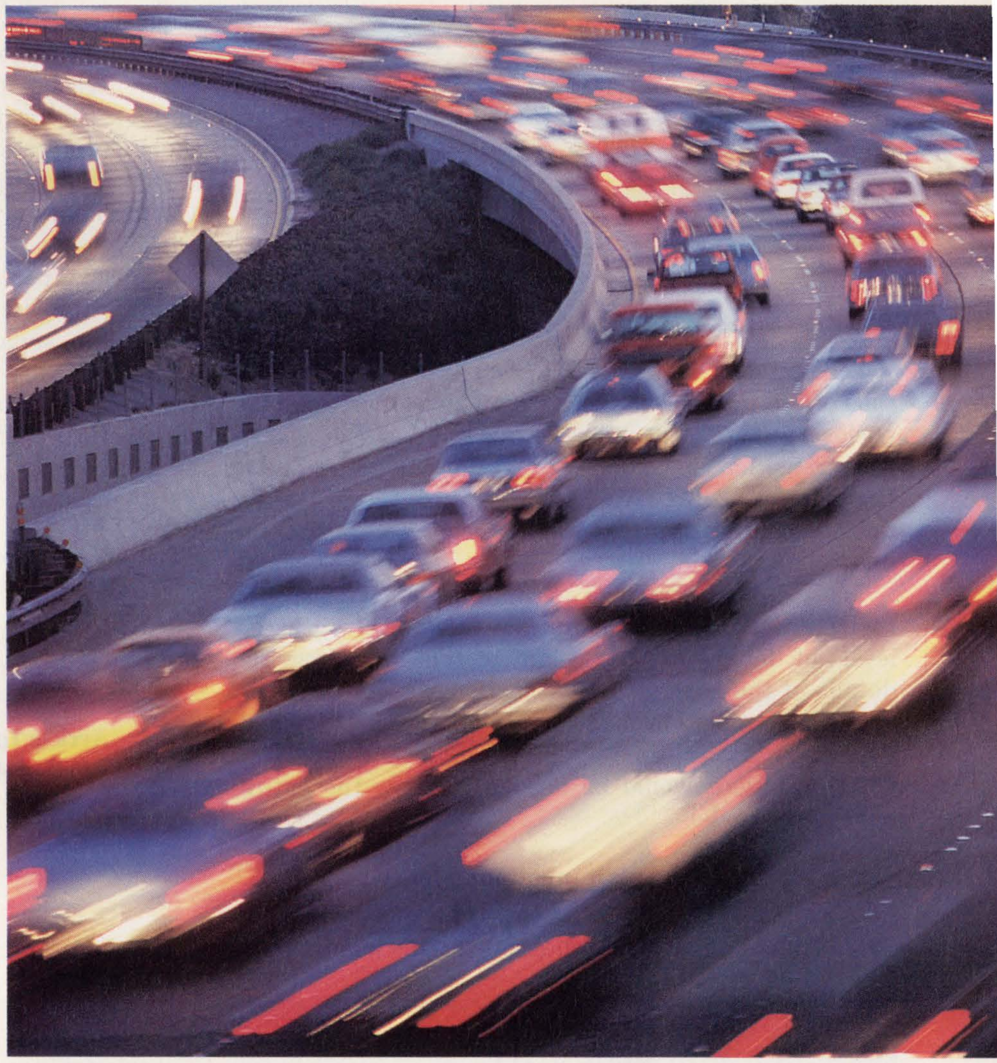

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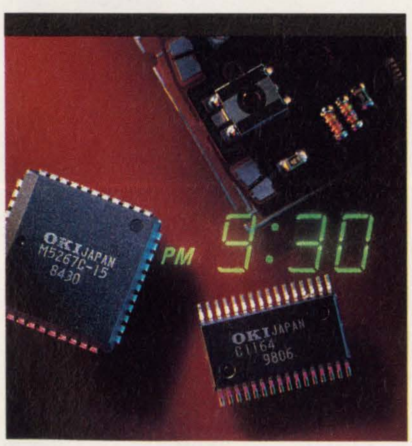

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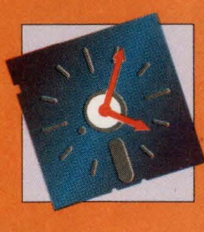
Lines entering the enclosure are input events; lines leaving the enclosure are output events. Rectangular areas show stored data; dashed lines delimit the area when binary data is stored; solid lines delimit the area when the data is not binary.



The premise of the requirements model is that it be independent of the means of implementation.

For the state-transition diagram that shows the details of the transformations (**Figs** 3 and 4), rectangular enclosures represent states. An arrow between states is a transition engendered by the event listed above the horizontal line next to the arrow. Actions taken during the transition are shown below the horizontal line.

The graphical methods permit the behavior model to be developed by elaborating successively greater levels of detail. You get a hint of this by hiding the details of the control transformation within the separate state-transition diagram. In more complex (and more typical) real-time applications, several layers of transformations would be needed to show the entire behavioral model.

Implementing the requirements model

The problem of designing a real-time application consists of first preparing a requirements model and then transforming it into an implementation model. The premise of the requirements model is that it be independent of the means of implementation. (When the single-lane "bridge" is a temporary road blockage, the requirements are often implemented by people, unaided by computers.) When the system is to be realized through a computer, the requirements model must pass through the next stage of transformation to become an implementation model. Methods of implementing a real-time application, once the specifications are in hand, is the main thrust of this series of articles.

The next part of this series will discuss the first hurdle: How to partition the overall requirements model into separate concurrent tasks. Subsequent parts will deal with techniques for coordinating these tasks, for communicating between them, and for providing other centralized services.

References

1. Ward, Paul and Stephen Mellor, "Structured Development for Real-Time Systems," Prentice-Hall, 1985, Vol 1, Section 7.9.

2. Falk, H, "CASE Tools Emerge to Handle Real-time Systems," *Computer Design*, Vol 27, No 1, January 1, 1988.

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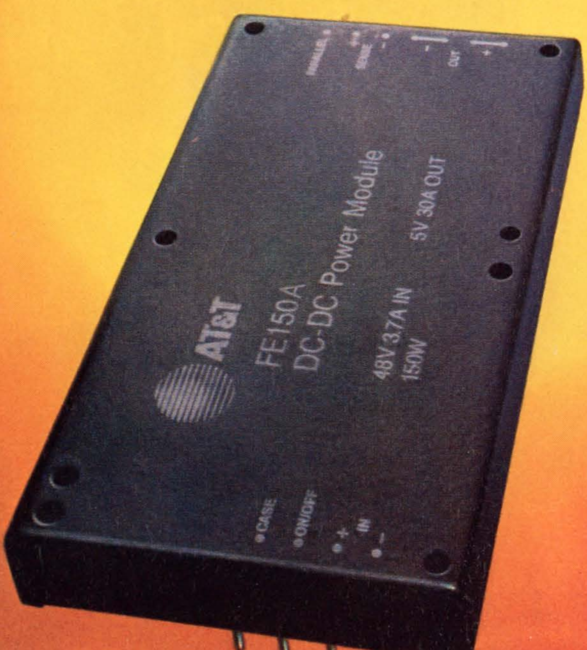

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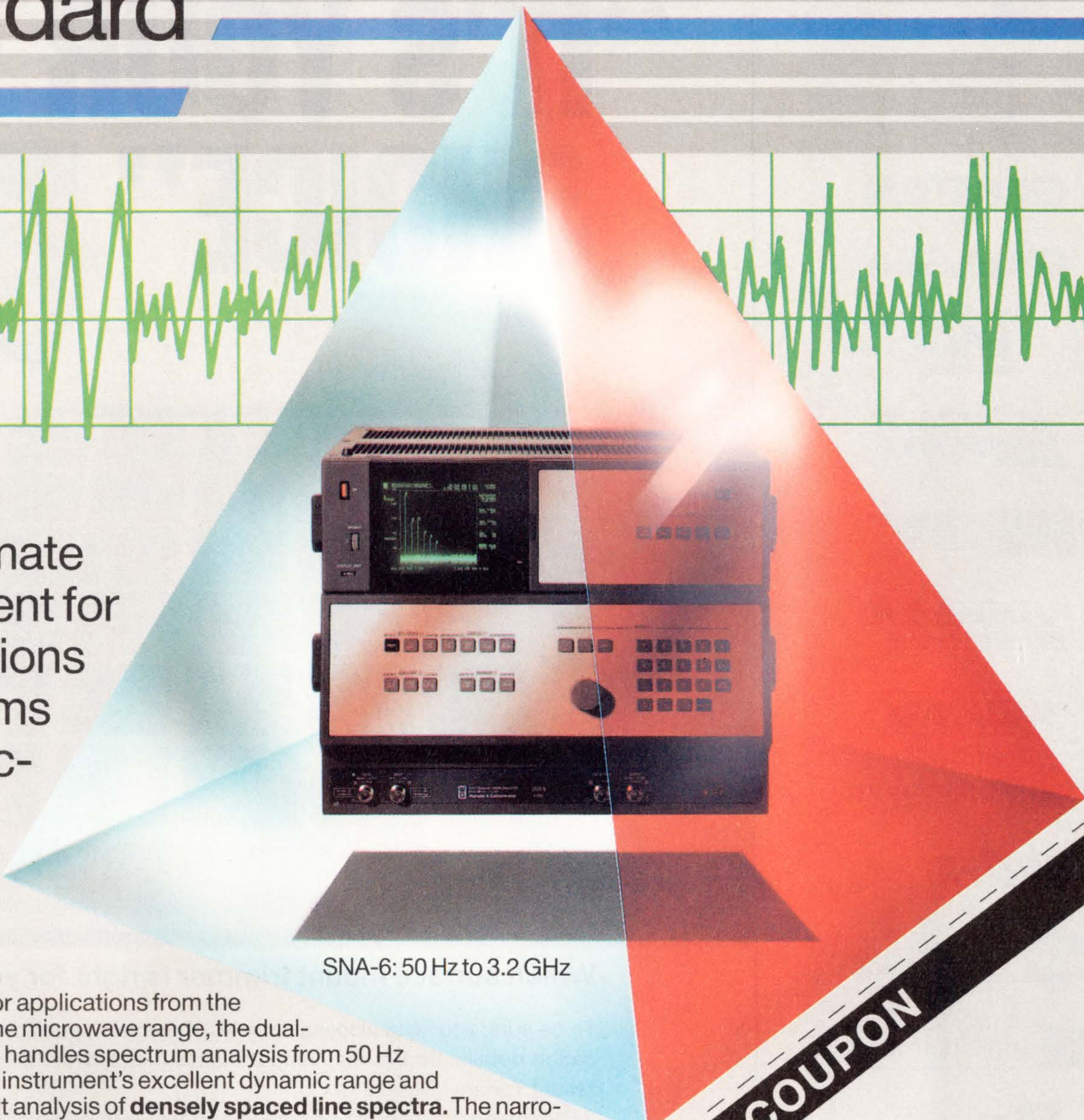

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Hall sensor detects ground faults

V Lakshminarayanan
Centre for Development of Telematics, Bangalore, India

The ground-fault circuit in **Fig 1** is economical and does not electrically contact the conductor it is monitoring. The circuit uses the UGN-3503T Sprague Hall-effect sensor, which senses relatively small changes in a magnetic field.

In operation, the sensor's linear output capacitively couples to an op amp. A Schmitt trigger makes the op amp's output logic compatible. When the circuit detects no leakage current, the transistor Q_1 is on (if the D flip-flop is reset) and the optocoupler's transistor is off. Consequently, transistor Q_2 is also off, and it supplies no gate drive to the triac.

In the event of a ground fault, the Hall-effect sensor will detect the current's magnetic field and develop an output voltage. The op amp amplifies this voltage, strobing the Schmitt trigger. The Schmitt trigger sets the D flip-flop, turning Q_1 off and the optocoupler's transistor on. The optocoupler turns on Q_2, triggering the triac. The triac energizes the "shunt-trip" coil of a circuit breaker (an internal, optional solenoid that trips the breaker), killing power.

Fig 2 shows how to mount the Hall-effect sensor in the air gap of a mild-steel flux collector. The collector is a bar of steel formed into a horseshoe shape. You can add isolation transformers to prevent any faults in this fault-detecting circuit from disturbing the protected circuit. (**EDN BBS DI #892**) EDN

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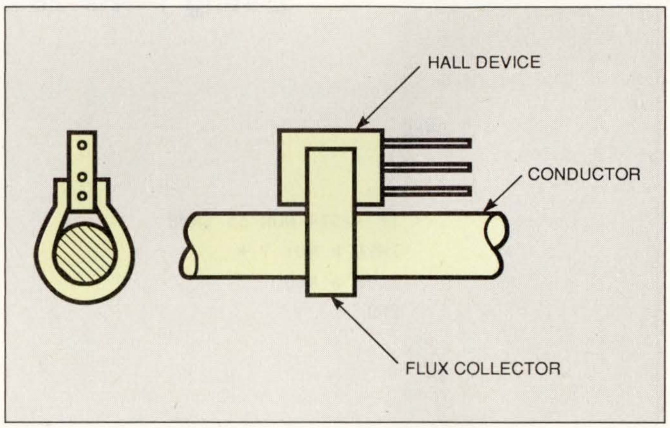

Fig 2—A simple mild-steel strap *collects flux for the Hall-effect sensor.*

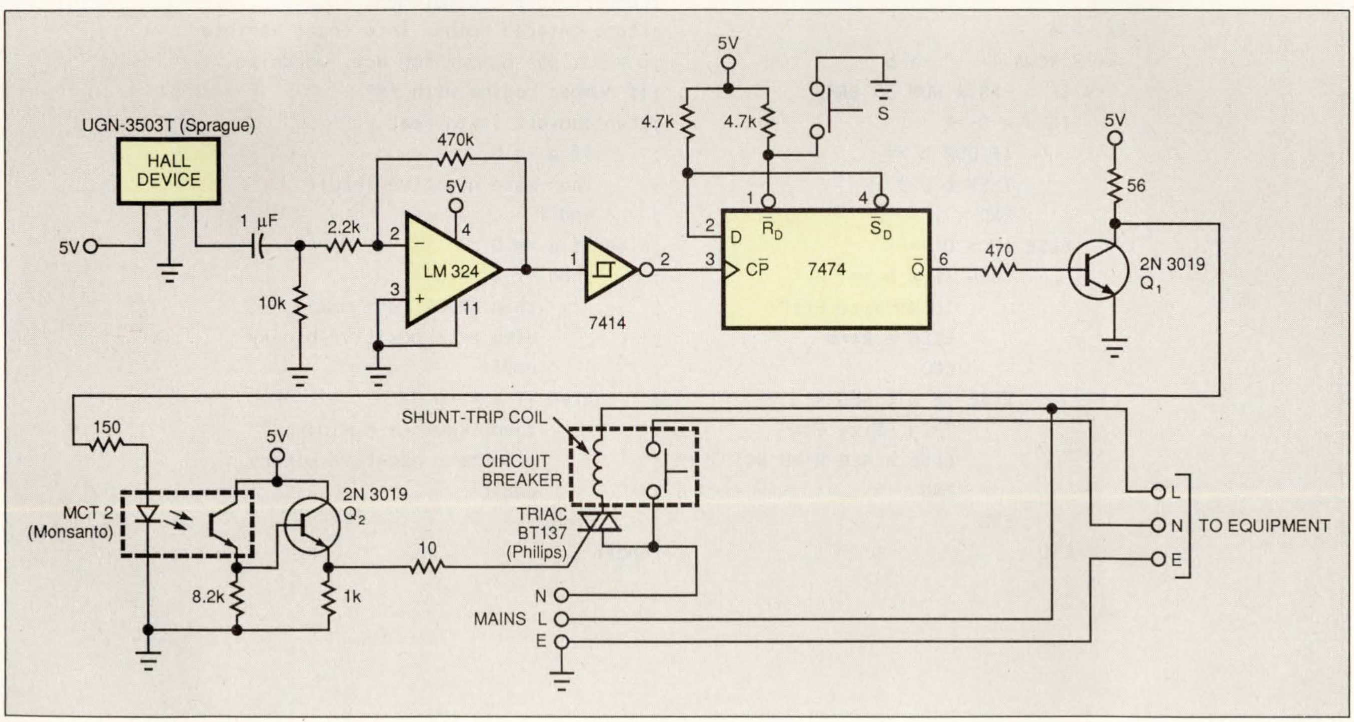

Fig 1—This ground-fault-detection circuit *amplifies and squares up the output of a Hall-effect sensor. When the circuit detects a ground fault, it energizes the "shunt-trip" coil of a breaker.*

Calculator performs 2's-complement math

Peter Kielbasiewicz
Hewlett-Packard Medical, Böblingen, Germany

The calculator programs in **Listing 1** make up for the Hewlett-Packard HP-28 calculator's lack of 2's-complement binary-conversion routines. The first program negates a number in 2's-complement form. The second program converts numbers from real to binary and binary to real. The currently defined binary-word size determines the positive and negative ranges for binary numbers. (**EDN BBS DI #896**) **EDN**

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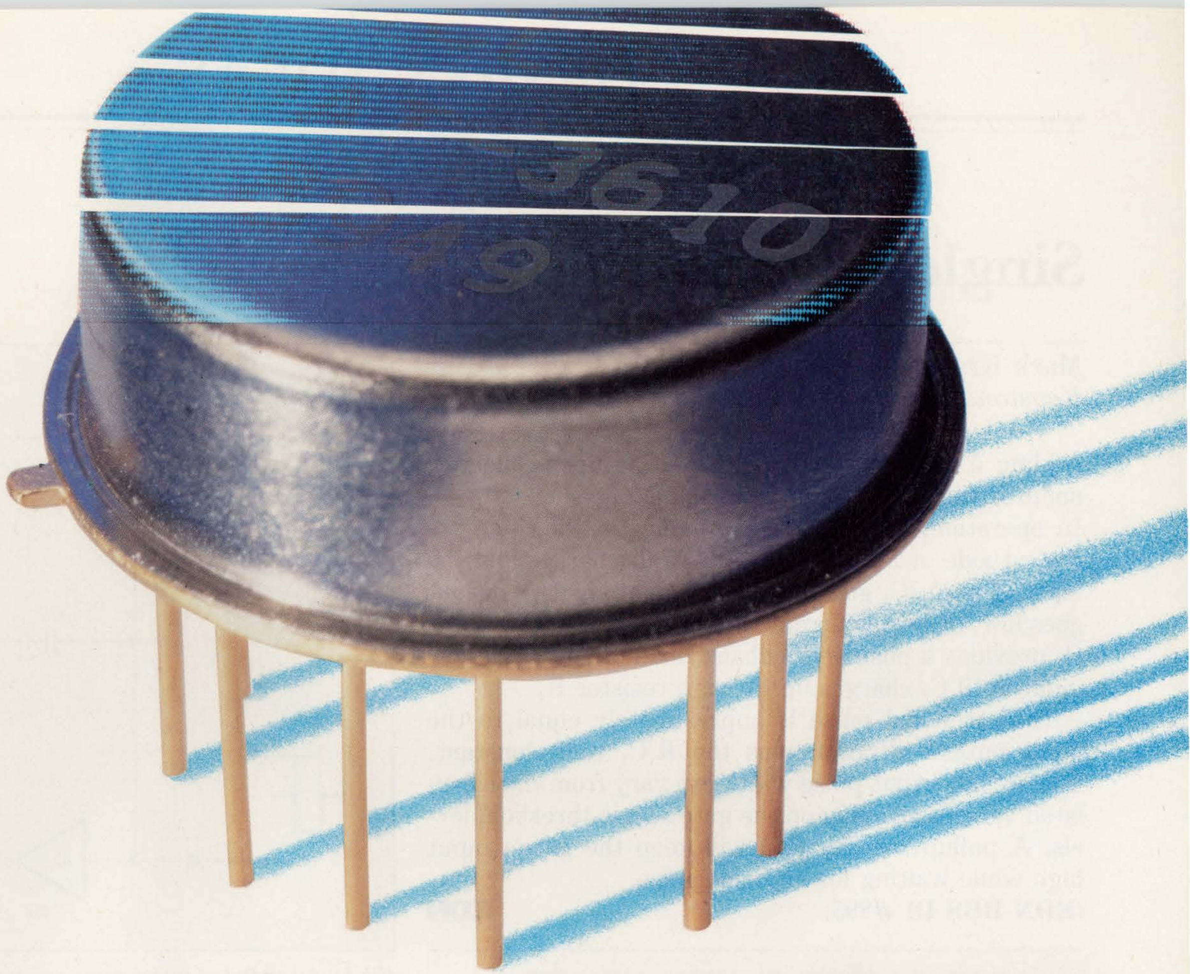
Listing 1—HP-28 binary-arithmetic routines

```
BNEG                              ;negate a number with
                                  ;respect to 2's complement
<< -> a                           ;store entered number into local varible
 << IF ->STR NUM 35 SAME          ;if number begins with '#'
    THEN a NOT 1 +                ;then make 2's complement
    ELSE a NEG                    ;else simply negate
    END
 >>
>>


BCONV                             ;convert between real & binary with
                                  ;respect to 2's complement
<< -> a                           ;store entered number into local varible
 << 2 RCWS 1 - ^ -> b             ;b = max pos number for act. wordsize
  << IF a ->STR NUM 35 SAME       ;if number begins with '#'
     THEN a B->R                  ;then convert it to real
          IF DUP b >=             ;     if a >= b
          THEN b 2 * -            ;     then make negative result
          END                     ;     endif
     ELSE IF a 0 >=               ;else if a >= 0
          THEN IF a b >=          ;     then if a >= b
               THEN "Size Err"    ;          then ERROR (a > max)
               ELSE a R->B        ;          else make positive binary
               END                ;          endif
          ELSE IF a b NEG <       ;     else if a < -b
               THEN "Size Err"    ;          then ERROR (a < min)
               ELSE a NEG R->B NOT 1 + ;     else make negative binary
               END                ;          endif
          END                     ;     endif
     END                          ;endif
  >>
 >>
>>
```



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1.0	**0.2**	**2.0**	**0.2**	**6.0**	**0.3**	**10.0**	**0.3**
1.5	0.32	3.0	0.4	9.0	0.6	15.0	0.6
2.0	**0.2**	**4.0**	**0.3**	**10.0**	**0.3**	**20.0**	**0.4**
2.5	0.32	5.0	0.5	13.0	0.6	25.0	0.7
3.0	0.4	6.0	0.5	16.0	0.6	30.0	0.7
3.5	0.52	7.0	0.7	19.0	0.9	35.0	1.0

bold faced values are individual elements in the units

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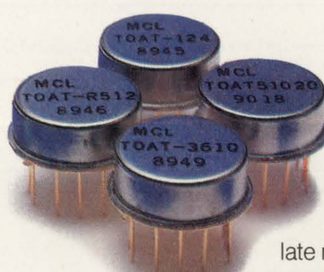

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Single gate stretches pulses

Mark Krasnov
Keystone Controls, Houston, TX

Adding a capacitor and a diode to an open-collector, noninverting gate produces a simple one-shot (**Fig 1**). In operation, when a negative-going pulse comes to the cathode of D_1, the capacitor C_1 discharges and the input of gate IC_1 goes low. Consequently, IC_1's output goes low, drawing current through LED D_2. Capacitor C_1 provides a positive feedback, maintaining IC_1's low input until C_1 charges up through resistor R_1.

The stretched pulse is approximately equal to the input pulse's duration plus the R_1C_1 time constant. The actual output-pulse width can vary from the calculated value depending on the gate's logic-threshold levels. A pullup resistor (R_2) will keep the gate's input high while waiting for an input pulse.
(EDN BBS DI #895)

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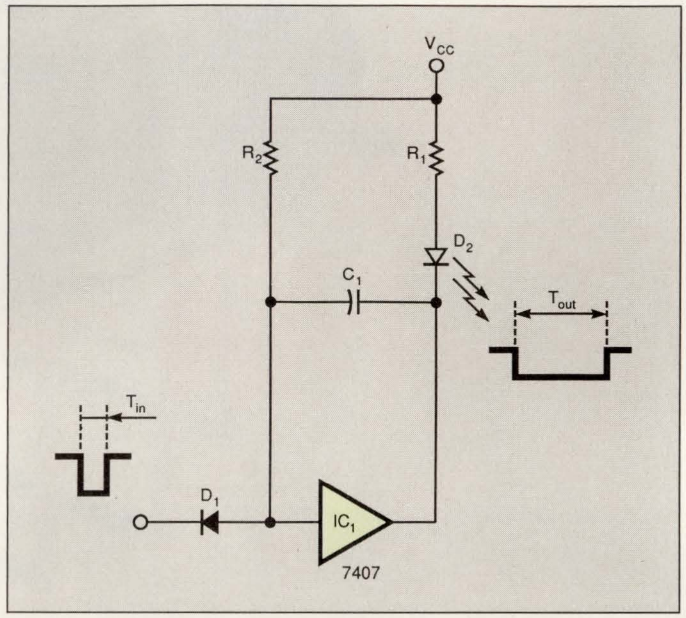

***Fig 1—A handful of inexpensive components** transforms a noninverting gate into a simple pulse stretcher.*

PLD decodes serial protocol

Richard Andelfinger
Photometrics Ltd, Tucson, AZ

Programming a synchronous, finite-state machine (FSM) into a Cypress Cy7C330 PLD achieves two goals for a serial-protocol decoder: eliminating a potentially unstable analog one-shot and allowing for variations in the protocol.

The serial protocol comes in over a single data line paced by a single clock line. The clock line carries bursts of between 12 and 16 positive-going edges (depending on protocol variations) separated by a gap **(Fig**

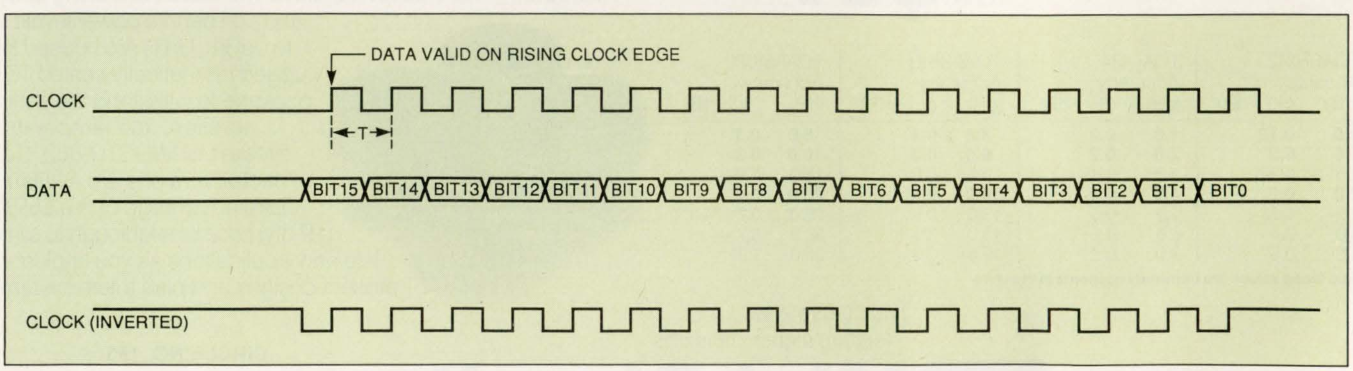

***Fig 1—This simple, serial protocol consists** of 12 to 16 data bits separated by a gap.*


TWO WAYS
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1). The gap divides the serial stream into words. The decoder has to allow for variable clock polarity, variable bit times, variable gap times, and the possibility of discarding the first bit of each word.

Internally, the PLD contains a programmable counter and a state machine. The programmable counter functions as a digital one-shot, detecting the interword gaps. Six of the PLD's pins constitute an input port to the PLD's programmable counter and internal logic. A 25-MHz system clock strobes the counter and the input-data clock resets it. Preset with the proper count, the counter will time out only during an interword gap.

The PLD's internal state machine **(Fig 2)** decodes the incoming data stream and drives external logic to capture the serial data stream, perform serial-to-parallel conversion, and clear the external logic's registers when appropriate.

The program for the PLD, which is too long to print here, is available on the EDN Bulletin Board System. See the end of this section for instructions on how to use the BBS. **(EDN BBS DI #894)** EDN

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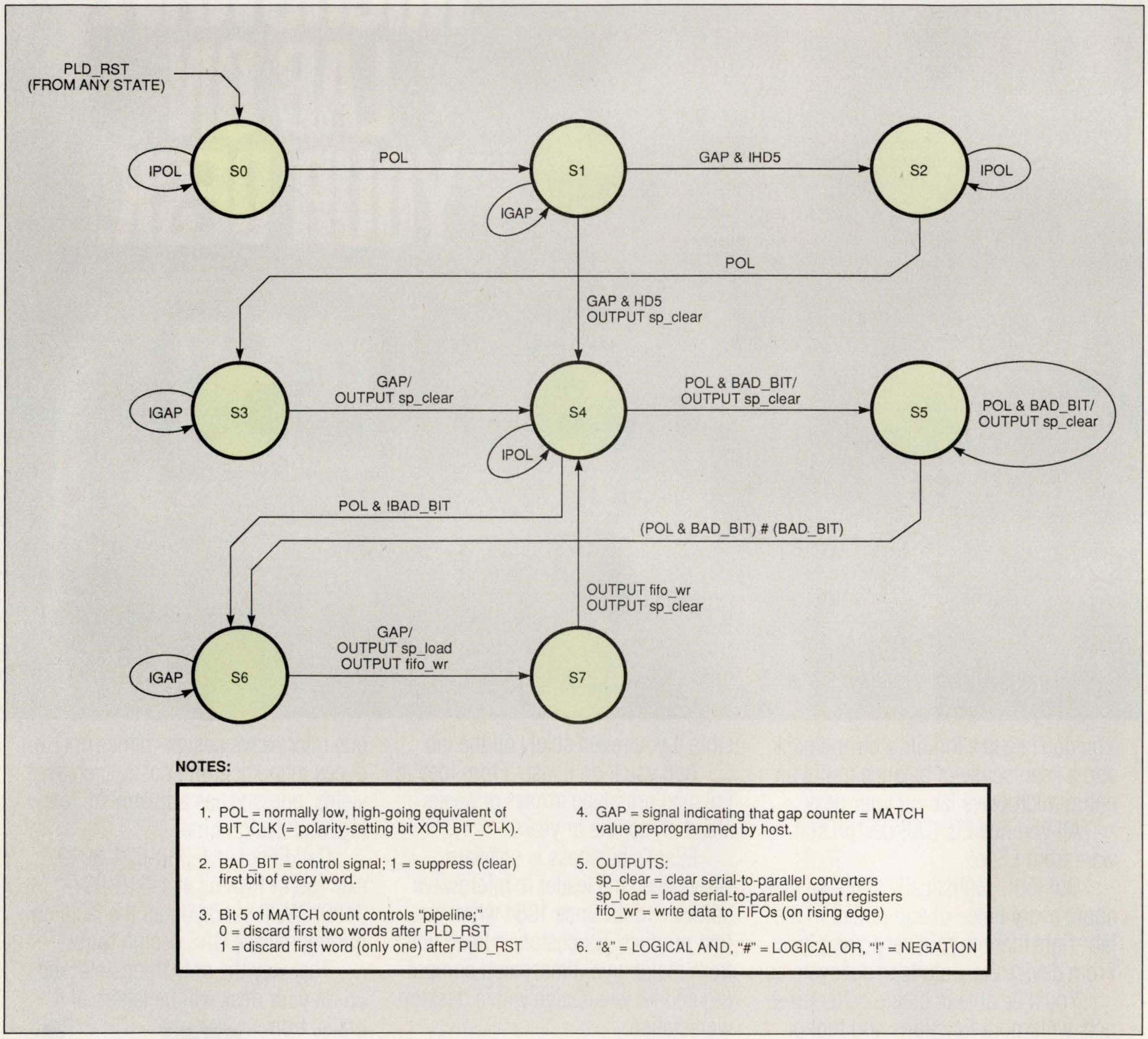

***Fig 2—A portion of a PLD configured as a state machine** decodes the incoming serial bit stream. Another portion of the PLD, configured as a gap-detecting timer, arms the state machine after timing out. A control-word bit, HD5, determines whether or not the state machine will discard the first bit of each word.*

DESIGN IDEAS

HP-15 program needs fewest keystrokes

Jon Vicklund
Ball Aerospace Corp, Boulder, CO

The program in **Listing 1** takes advantage of a Hewlett-Packard RPN calculator's stack operators to calculate the parallel resistance of two resistors using a minimum number of keystrokes.
(EDN BBS DI #893) **EDN**

To Vote For This Design, Circle No. 750

Listing 1—Minimal-keystroke parallel-resistance calculation for HP-15 calculator

R_1	; R_1 value
<ENTER> <ENTER>	; press enter twice
R_2	; R_2 value
<ENTER>	; enter
R↓	; roll down
+	; add
X⇄Y	; interchange X, Y
÷	; divide Y by X
÷	; divide Y by X
DISPLAY = REQ	

FEEDBACK AND AMPLIFICATION

Errata

The resistor R_2 in Greg Schafer's June 7, 1990 Design Idea "Cascaded video amps have high gain" should be 9965Ω, not 99.65Ω as written on page 138.

Tarlton Fleming
Maxim Integrated Products
120 San Gabriel Dr
Sunnyvale, CA 94086
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Text continued

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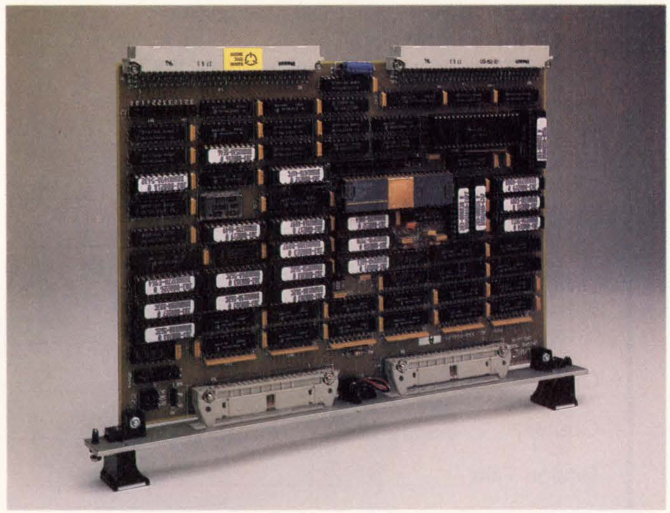

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To use the BBS, first call up and log onto the system. To get to the Design Idea Special Interest Group, first select "s", the SIGs option. Next select the "s" new-SIG option and ask for a list of SIGs by entering a "?". Enter the "/DI_SIG" name. Then select the "r" read-bulletin and "s" scan-bulletin options. You should now be able to scan the titles of available Design Ideas (DIs), optionally read an attached explanatory message, and optionally download an attached file. Note that the BBS assigns its own number to each message. You will find our DI number, along with a portion of the DI's headline, when you scan the list of bulletins. You can optionally use our DI number, or any portion of a DI's headline, to search for a particular Idea. To leave the DI editors a message, first get to the /DI_SIG, and then select the "w" write-message option.

Charles H Small and Anne Watson Swager
Design Idea Editors

Single op amp also does the job

In the Design Idea "Current sink widens VCO's frequency range," which appeared on pg 174 of the May 24, 1990, issue of EDN, the author uses an external current source to extend the VCO's range. As an extension of his idea, you can exploit the internal MOS, current-source transistor to do the job of his external transistor Q1. In this case, you need only an additional op amp to achieve almost the same linearizing effect.

Dr Rainer Lackmann, Dr Ing
Fraunhofer Institute
Finkenstr 61
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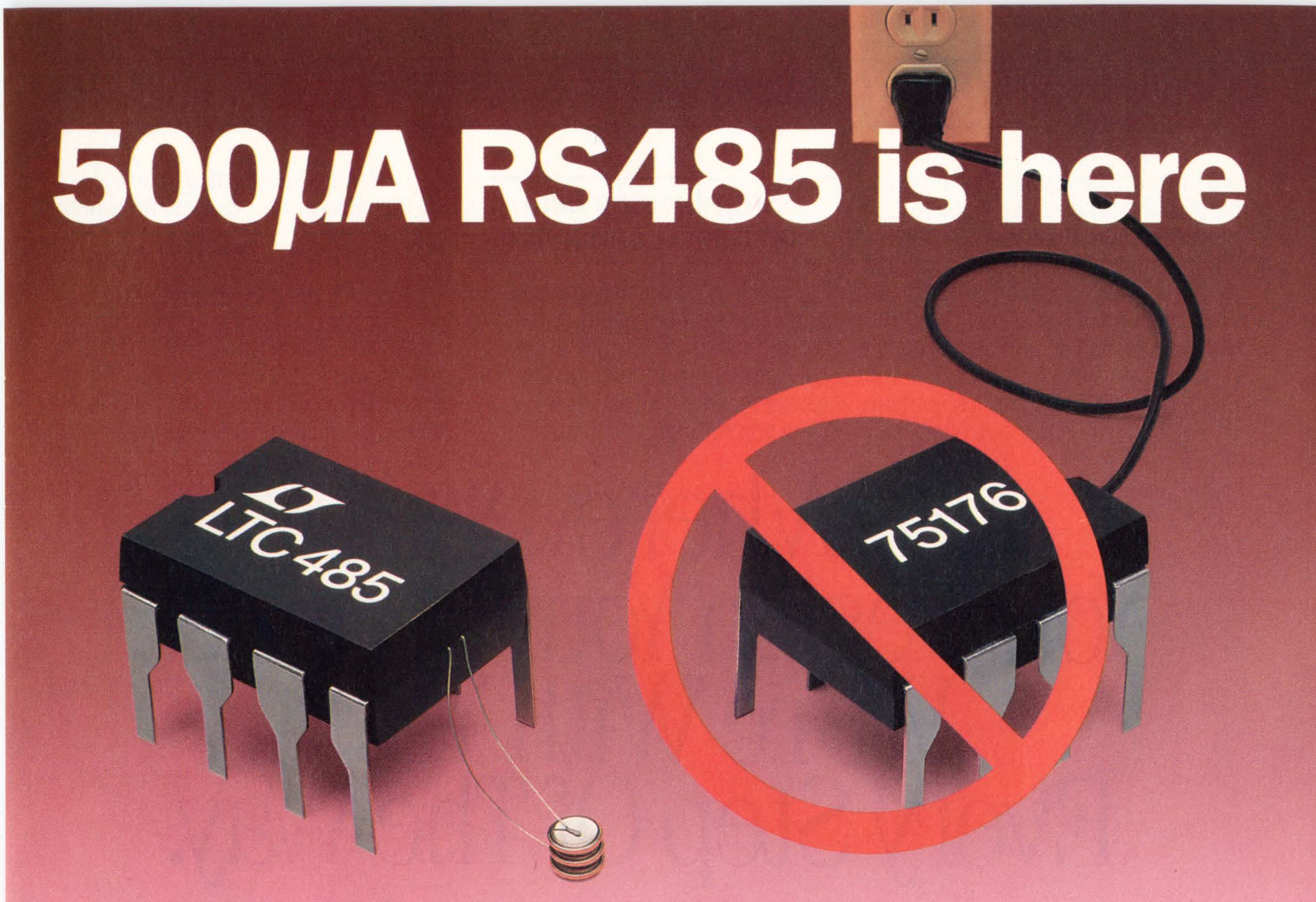
500μA RS485 is here



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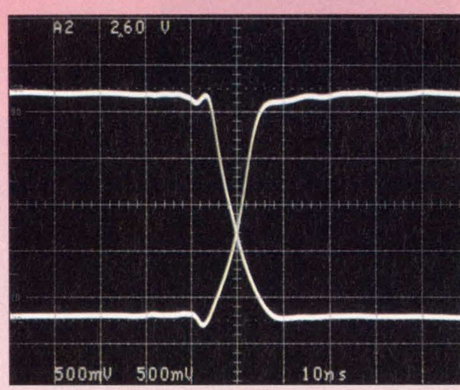

LTC485 differential driver output.

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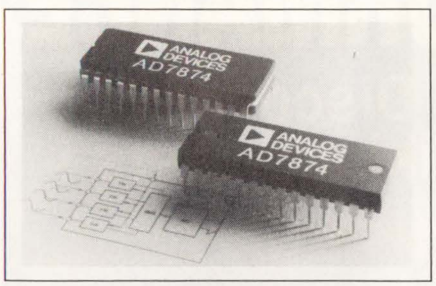
Precision Monolithics Inc, Box 58020, Santa Clara, CA 95052. Phone (408) 727-9222. FAX (408) 727-1550. **Circle No. 351**



4-Channel Sampling ADC

- *Simultaneously samples all channels*
- *Provides 34-μsec conversion*

The AD7874, which simplifies the design of multichannel systems and minimizes channel-to-channel errors, contains four (matched) track-and-hold amplifiers, a multiplexer, a clock, a 3V reference, and a 12-bit ADC. To preserve phase relationships, the device simultaneously captures four signals, converting all four within 34 μsec. At the AD7874's throughput of 29k samples/sec, the converter has a S/N ratio of 71 dB min and an aperture-delay deviation of 40 nsec max. Maximum spurious noise, intermodulation distortion, and total harmonic distortion are each −80 dB. Other specifications include ±1 LSB maximum differential nonlinearity, ±5 LSBs full-scale and bipolar zero error, and 80-dB channel isolation. The AD7874 is available in three temperature/performance grades. Package options include 28-pin DIPs and SOICs. From \$28 (100).

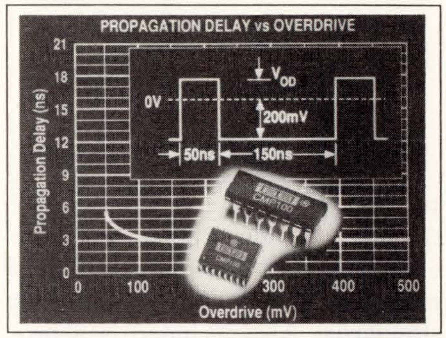
Analog Devices Inc, 181 Ballardvale St, Wilmington, MA 01887. Phone (508) 937-1428. **Circle No. 352**

20-Bit Audio ADC

- *Dynamic range is 108 dB*
- *Nonlinearity is ±0.2 LSB*

Using an oversampling, noise-shaping architecture, the ADC-20048 digitizes signals from dc to 20 kHz. The noise-shaping circuitry ensures smooth code transitions throughout the entire input-signal range, resulting in a typical differential nonlinearity of only ±0.2 LSB. The 20-bit converter samples analog signals at a 128× oversampling rate and uses digital filtering to eliminate the need for sample/hold amplifiers and antialiasing filters. Output data rates of 44.1 kHz or 48 kHz, and input ranges of ±3V or ±5V are pin-selectable. The ADC-20048 includes the AFE-20048 front end and the D20C10 decimator filter. The critical analog circuitry is assembled on a double-sided pc board inside the 2×3×0.4-in. encapsulated front-end module. The decimator filter is a custom CMOS chip packaged in a 48-pin DIP. Complete ADC-20048, \$199 (100). Delivery, four to six weeks ARO.

UltraAnalog Inc, 47747 Warm Springs Blvd, Fremont, CA 94539. Phone (415) 657-2227. FAX (415) 657-4225. **Circle No. 353**



Dual Comparator

- *Useful as an ATE pin receiver*
- *Propagation delay is 5 nsec max*

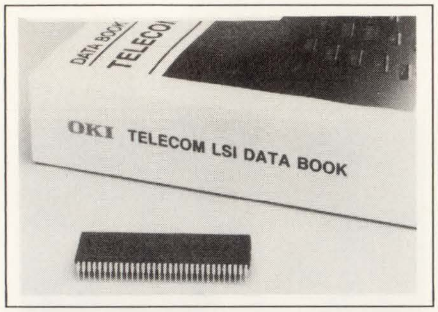
The CMP100 dual comparator combines high speed with a ±12V common-mode input range. Useful as a pin receiver in automatic test equipment (ATE) applications, the device features typical and maximum propagation delays of 3.6 and 5.0 nsec, respectively. Dual outputs, which are latchable and 10K ECL compatible, let you use the device as a sampling comparator. You can obtain a single-output window function by combining both outputs with an ECL NOR gate. The comparator can drive a 50Ω load connected to the −2V ECL reference level. The CMP100 is specified for the industrial temperature range and operates from ±5V supplies. Package options include 16-pin DIPs and 16-lead plastic SOICs. \$23.20 (100).

Burr-Brown Corp, Box 11400, Tucson, AZ 85734. Phone (602) 746-1111. FAX (602) 889-1510. TWX 910-952-1111. **Circle No. 354**

Front-End Processor

- *Includes transmit/receive functions*
- *Has 300- to 9600-baud capability*

When combined with a general-purpose DSP, the MSM6994 FEP (front-end processor) provides 300- to 9600-baud modem capabilities. The FEP supports eight standards, including V.32. Included on chip are A/D and D/A converters and a digi-



tal filter. A guard-tone generator eliminates the glue logic normally needed to switch between different standards. Also included is a programmable attenuator and a core DSP, which provides band-limiting filtering, carrier detection, and automatic gain control with call-progress tone detection. The A/D and D/A converters use a 2.592-MHz oversampling delta-sigma technique, which provides 80 dB of dynamic range and 13-bit accuracy. The FEP contains interfaces for both DSP and analog transmit/receive data, and for line network control. The MSM6994, which operates from a 5V supply, is available in 64-pin miniature DIPs, 64-pin flatpacks, and 68-pin plastic leaded chip carriers. \$23.50 (10,000). Delivery, six to eight weeks ARO.

Oki Semiconductor, 785 N Mary Ave, Sunnyvale, CA 94086. Phone (408) 720-1900. FAX (408) 720-1918.

Circle No. 355

Smart-Access Controller

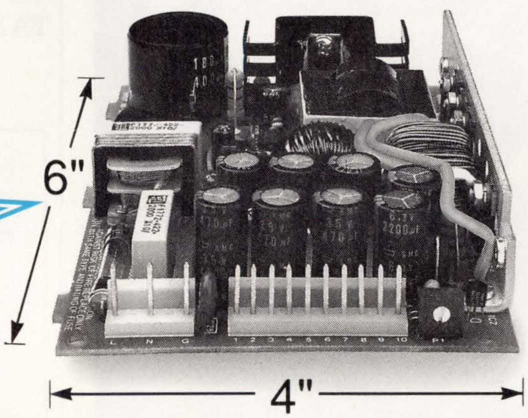
- *Combines an 8-bit μP with serial controller*
- *Includes two 8-bit parallel ports*

Called the Smart Access Controller (SAC), the Z80181 combines one channel of the Z8530 serial communications controller (SCC) with the Z180 8-bit μP. The SAC also contains two 8-bit parallel ports for I/O intensive applications and a Z84C30 4×8-bit counter/timer. The single-channel SCC supports all common asynchronous and synchronous protocols including Monosync, Bisync, synchronous-data link control, and high-level-data link control. The Z80181 contains all functions of the Z180 including an advanced Z80-code-compatible CPU with extra instructions, two 16-bit timers, and two UARTs with baud-rate generators. An on-chip memory-management unit expands the address space to 1M byte. Two DMA controllers provide high-speed data transfers between memory and I/O. The SAC operates at 10 MHz and has a data-transfer rate of 2.5M bps. The Z80181 comes in a 100-pin quad flatpack. \$22 (1000).

Zilog, 210 Hacienda Ave, Campbell, CA 95008. Phone (408) 370-8000. FAX (408) 370-8056.

Circle No. 356

UNIVERSAL 85-264 V INPUT 65 W SWITCHER



One To Four Outputs

1.125" Total Height

Never Worry About Input Voltage Again

The SRW-65 Series from Integrated Power Designs delivers 65W in a 6" x 4" x 1.125" package. The power supply accepts any input voltage within the range of 85 to 264 V AC without any modifications.

The New SRW Series Features

- ❑ Less than 1% P-P Ripple & Noise on All Outputs
- ❑ 0° to 50° Convection Cooled Operating Temp.
- ❑ 100% Burn-In with Power Cycling
- ❑ Snap-Lock or Screw-Down I/O Connectors
- ❑ Submitted for Testing to UL1950, CSA 22.2 No. 234-M, and EN 60950 (TUV)
- ❑ Level "B" Input Filter
- ❑ Over-Voltage Protection
- ❑ One-Year Warranty
- ❑ 75-80% Efficiency
- ❑ 21 Standard Models
- ❑ 20 mS Hold-Up Time

QUADS:	Output 1	Output 2	Output 3	Output 4
SRW-65-4001	+5V@5.0A	–5V@3.0A	+12V@2.0A	–12V@2.0A
SRW-65-4002	+5V@5.0A	+12V@1.0A	+12V@2.0A	–12V@2.0A
SRW-65-4003	+5V@5.0A	+24V@1.0A	+12V@2.0A	–12V@2.0A
SRW-65-4004	+5V@5.0A	–5V@3.0A	+15V@2.0A	–15V@2.0A
SRW-65-4005	+5V@5.0A	+24V@1.0A	+12V@2.0A	–5V@2.0A
SRW-65-4006	+5V@5.0A	+24V@1.0A	+15V@2.0A	–15V@2.0A
TRIPLES:				
SRW-65-3001	+5V@5.0A		+12V@3.0A	–12V@1.0A
SRW-65-3002	+5V@7.0A		+12V@2.0A	–12V@2.0A
SRW-65-3003	+5V@7.0A		+15V@2.0A	–15V@2.0A
SRW-65-3004	+5V@5.0A	–5V@4.0A	+12V@2.0A	
SRW-65-3005	+5V@5.0A	–5V@4.0A	+24V@1.0A	
DUALS:				
SRW-65-2001	+5V@7.0A			–5V@5.0A
SRW-65-2002	+5V@7.0A		+12V@3.0A	
SRW-65-2003	+12V@3.0A			–12V@2.5A
SRW-65-2004	+15V@2.5A			–15V@2.0A
SRW-65-2005	+5V@7.0A		+24V@1.5A	
SINGLES:				
SRW-65-1001	+5V@10.0A			
SRW-65-1002	+12V@5.4A			
SRW-65-1003	+15V@4.3A			
SRW-65-1004	+24V@2.7A			

Other output combinations available, please consult factory.

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9C Princess Road ❑ Lawrenceville, NJ 08648 ❑ Tel: (609) 896-2122 ❑ Fax: (609) 895-1738

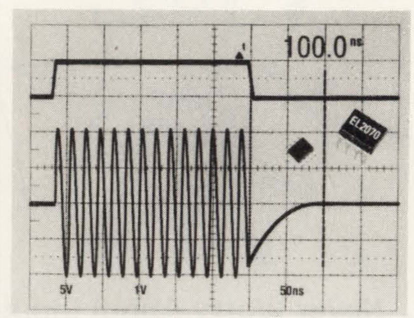
Programmable FIR Filter

- *Contains 16 16×12-bit MACs*
- *Provides 16 to 128 stages of filtering*

The PDSP16256 is a programmable, FIR filter. Targeted for use in high-performance digital receivers, the device contains 16 16×12-bit multiplier-accumulators that can be cycled to provide 16 to 128 stages of digital filtering at sample rates from 2.5 to 20 MHz. You can configure the IC either as one long filter or as two half-filters. The cascadable device permits filters of any length, limited only by accumulator overflow. A decimate-by-two option doubles the number of taps available and halves the output data rate for a given sample rate. Downloaded from a host CPU or a byte-wide EPROM, the PDSP16256 can store as many as 128 coefficients internally. A single EPROM can provide coefficients for a cascade of 16 devices, without additional support. The device is available in a 144-pin pin-grid array or a 172-pin quad flatpack. $395 (1000).

Plessey Semiconductor Corp, 1500 Green Hills Rd, Scotts Valley, CA 95066. Phone (408) 438-2900. FAX (408) 438-7023. TLX 4940840.

Circle No. 357



Video Amplifier

- *Has a −3-dB bandwidth of 200 MHz*
- *Output drive capability is 70 mA*

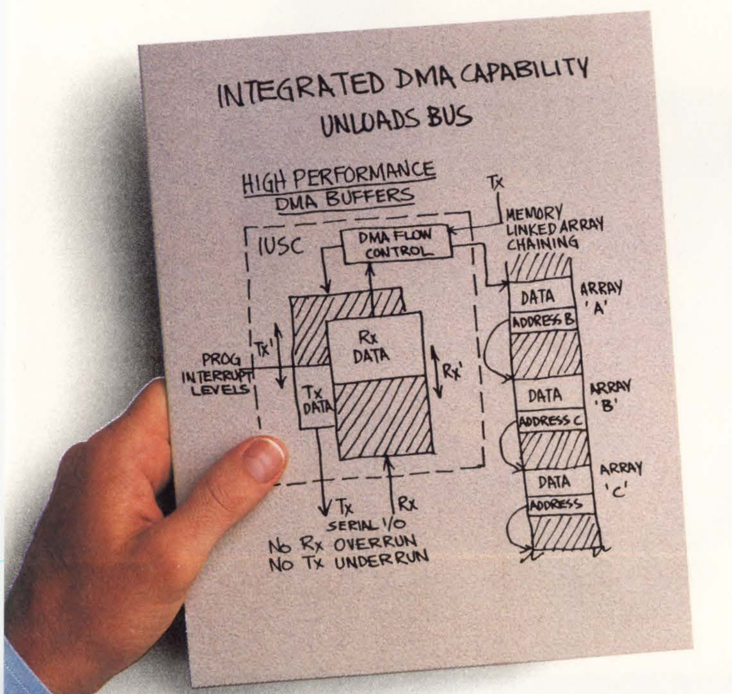
Designed for video distribution and line-driving applications, the EL2070 amplifier is an improved replacement for the CLC410 from Comlinear Corp. The amplifier features a −3-dB bandwidth of 200 MHz and a flat 0.1-dB bandwidth of more than 30 MHz. The device, which operates from ±5V supplies, has an output drive capability of 70 mA. Other specifications include differential gain linearity of 0.02%, differential phase linearity of 0.01°, and a settling time of 12 nsec to 0.05%. A disable pin allows multiplexing between multiple EL2070s to form selectable gain stages, selectable filters, or a routing switch. In an 8-pin DIP, $7.70 (100).

Elantec Inc, 1996 Tarob Ct, Milpitas, CA 95035. Phone (408) 945-1323. **Circle No. 358**

Z I L O G

The *INTEGRATED* USC. More buffer management. More system efficiency. Less cost.

Zilog's integrated universal serial communication controller (Z16C31™) combines two 32-bit full duplex DMA channels with a powerful single-channel USC cell. And that means efficient bus access, sophisticated buffer management, higher throughput, a greatly reduced CPU workload, and considerably lower cost for complex data communications applications.



Fast, multi-protocol operation.

Zilog's USC cell gives you 10 Mbits/sec speed for multi-protocol operation. It also gives you 32-byte RX and TX FIFOs for improved latency and up to 32-byte block moves. There's a Time Slot Assigner for multiplexing in ISDN/T1 applications, a flexible 16-bit bus interface — multiplexed or non-multiplexed — for easy CPU interconnect, and a daisy-chain interrupt structure for simpler interrupt handling. And, best of all, the USC can reduce the CPU workload as much as *60%*.

Integrated buffer management.

The IUSC's two 32-bit DMA channels provide for 32-bit addresses and 16-bit data word transfers... and they allow full duplex operation at 10 Mbits/sec. The two simple DMA modes, normal and buffered, mean your design can be tailored to common buffer management schemes. The two chained DMA modes, array chained and link array chained, reduce CPU overhead in advanced buffer management schemes. The daisy-chain DMA priority structure makes it easy to design multiple IUSC systems.

Versatility and reliability.

The IUSC's flexible, multi-protocol design lets you adapt your system to a variety of networks as interconnect standards evolve. The IUSC supports ten protocols and eight data encoding formats, including asynchronous, bit and byte synchronous, HDLC, isochronous, Ethernet and MIL-STD 1553B. And it all comes to you off the shelf, backed by Zilog's proven quality and reliability. To find out more about the IUSC or any of Zilog's growing family of Superintegration™ products, contact your local Zilog sales office or your authorized distributor today. Zilog, Inc., 210 Hacienda Ave., Campbell, CA 95008, (408) 370-8000.

Right product. Right price. Right away.

ZiLOG

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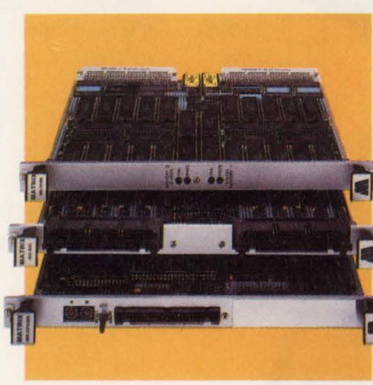


Single-Board Computers

- *Use either an 80386 or 80486 μP*
- *Fit in one VMEbus slot*

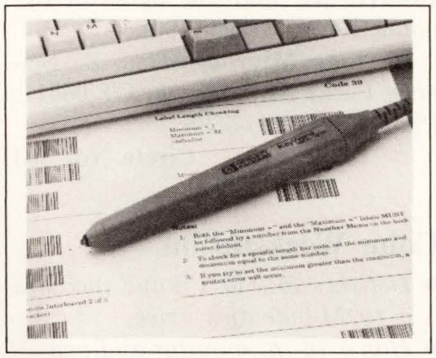
The 386SBC and the 486SBC self-contained single-board computers employ an 80386 and an 80486 μP, respectively. The 9U-size boards fit into a single VMEbus backplane slot. The boards are compatible with an IBM PC/AT computer running MS-DOS. They also run AT&T's Unix System V.4 operating system. By using one of the boards as a coprocessor, the card can run MS-DOS applications while the mother board runs Unix applications. The computers are available with 4M, 8M, or 16M bytes of RAM and 32k bytes of cache memory with zero-wait-state operation at both 25 MHz and 33 MHz. Both come with two RS-232C ports (COM 1 and COM 2), six RS-422 ports, one parallel printer port (LPT1), an Intel 82077 floppy-disk interface, a keyboard interface, and a time-of-day clock with battery. The boards also have an enhanced BIOS, which supports an onboard SEEQ 8005 Ethernet LAN controller, an onboard VGA graphics controller with 1024×768 pixels, and an onboard NCR 53C700 SCSI hard-disk interface with high-speed bus transfers. From $7500. Delivery, 60 days ARO.

Dynatech Computer Systems, Box 7400, Mountain View, CA 94039. Phone (415) 964-7400. FAX (415) 969-3359. **Circle No. 359**

Bar-Code Scanner

- *Provides keyboard emulation for IBM PS/2, PC/XT, and PC/ATs*
- *Self-contained device doesn't require external decoder box*

The Keywand bar-code scanner emulates the keyboard for IBM's PS/2, PC/XT, and PC/AT computers. The scanner combines a μP, bar-code decoding software, an optical program, a nonvolatile memory, a contact scanner, and a keyboard interface in a standard-size industrial handheld wand. Because all of its electronics are encased in a compact polycarbonate wand, the scanner doesn't require an external decoder box. The scanner has a sapphire tip that resists wear and is capable of reading through plastic laminates. You can program the scanner to read from a series of menu labels, which permit various decoding options and interface protocols. Once the scanner is programmed, the configuration is secure in its nonvolatile memory. The scanner recognizes all of the popular bar-code symbologies. $370.



Hewlett-Packard Co, 19310 Pruneridge Ave, Cupertino, CA 95014. Phone (800) 752-0900. **Circle No. 360**

PS/2 Coprocessor Board

- *Delivers 5 VAX MIPS and 3.1M flops*
- *An MC68020 μP brings its features to the PS/2 computer*

The micro785+ is a coprocessor board for IBM's PS/2 computer. It uses a Motorola MC68020 μP, which brings floating-point performance and a linear address space to the PS/2. PC-DOS performs all file operations. In addition, the board features 5 VAX MIPS (based on Dhrystones) and 3.1M flops (Whetstones/sec); a memory bank, which uses multibank and interleave technology; 1M, 2M, or 4M bytes of RAM; Silicon Valley Software compilers for C and Fortran languages; and a dual-ported 16k-byte memory architecture that gives programs running on the PS/2 direct access to the MC68020's memory space. As many as four boards can operate simultaneously in a single PS/2 computer. $2795.

Yarc Systems Corp, 27489 W Agoura Rd, Agoura Hills, CA 91301. Phone (818) 889-4388. **Circle No. 361**

VMEbus Accelerator Board

- *Uses four FC-110 digital fuzzy processors*
- *Fuzzy decision making can run in parallel on any μP*

The Fuzzy VME Accelerator Board can interpret vague and imprecise information and determine a solution to a problem with incomplete data. The card permits fuzzy decision making on VMEbus systems. The board can be configured with one to four of the company's FC-110 digital fuzzy processors. The processor has a reduced-instruction-set computer architecture that can deliver 10 MIPS. The board comes with the company's CASE tool kit: TILShell for knowledge-base development, a compiler that converts the graphical languages to machine code, and an FC-110 assembler and linker. Board with four FC-110 processors, $4500.

Togai InfraLogic Inc, 30 Corporate Park, Suite 107, Irvine, CA 92714. Phone (714) 975-8522. FAX (714) 975-8524. **Circle No. 362**

Single-Board Computers

- *Contain either dynamic RAM or static RAM as main memory*
- *Space is reserved for modules that turn boards into I/O servers*

The CVME960 and CVME961 are single-board computers for the

VMEbus. Both 6U boards use an 80960CA reduced-instruction-set computer μP, which features a 1k-byte on-chip instruction cache, a 1k-byte on-chip data RAM, and four 59M-byte/sec DMA channels. The CVME960 couples a 25-MHz μP to a memory system with 35-nsec static RAM (SRAM). The SRAM is dual-ported to the μP and the VMEbus. The CVME961 contains either 1M, 2M, 4M, or 8M bytes of dynamic RAM (DRAM), which is also dual ported to the host bus. Both boards use VTC's Vic068 VMEbus interface controller, which provides a complete master or slave interface on the bus. The boards also feature two asynchronous serial ports, a real-time clock with battery back-up, and 1M byte of EPROM. In addition, both boards reserve a 12.7-in.^{2} area for a Squall module. This I/O module plugs directly into the board. CVME960 with 25-MHz μP and 1M byte of static RAM, $3995. CVME961 with 16-MHz μP and 1M bytes of dynamic RAM, $1995 (100).

Cyclone Microsystems, 25 Science Park, New Haven, CT 06511. Phone (203) 786-5536.

Circle No. 363

Color Workstation

- *Delivers 15.8 MIPS and includes a 107M-byte disk drive*
- *Has a 16-in. monitor and two Sbus expansion slots*

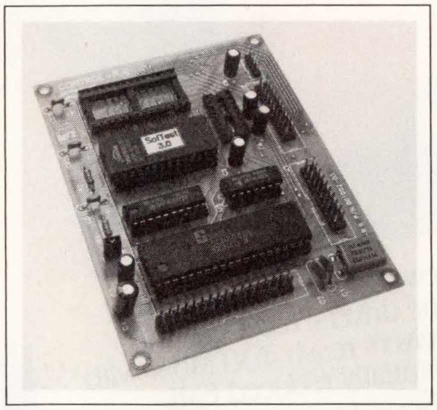
The SPARCstation IPC is a color desktop workstation. The reduced-instruction-set computer-based workstation delivers 15.8 MIPS and 1.7M flops. The station comes with a 207M-byte hard-disk drive as well as a 3½-in. floppy-disk drive. It also comes with a 16-in. color monitor and two Sbus expansion slots. The station has 8M to 24M bytes of memory that's expandable in 1M or 4M single in-line memory modules (SIMMs). The unit has audio inputs and outputs similar to other SPARCstations, and it has an Ethernet port as well as two serial ports. It is the first unit to conform to the SPARC Compliance Definition 1.0, which assures end users of compatibility among SPARC chips and systems. $9995 with the 207M-byte hard-disk drive; diskless version, $8995.

Sun Microsystems Inc, 2550 Garcia Ave, Mountain View, CA 94043. Phone (415) 960-1300. FAX (415) 969-9131. **Circle No. 364**

Microcontroller Module

- *Uses an 8031 μC and provides space for 8k bytes of RAM*
- *User has access to address, data, and control bus of the 8031*

The Control R II is a stand-alone



microcontroller module that employs an 8-bit 8031 μC. In addition to the μC's 128 bytes of internal RAM, the board has sockets for 8k bytes of static RAM. The user has access to the address, data, and control bus of the 8031 via expansion headers. Onboard jumpers allow the use of processors with ROMed languages such as 8052-Basic. Other features include 8k or 16k bytes of EPROM; an 11.0592-MHz crystal for generating baud rates; 14- or 16-bit parallel input and output; and a socket and capacitors for an optional Max 232 serial I/O connection. The board measures $3\frac{1}{2} \times 4\frac{1}{2}$ in. and operates from 5V. $64.95 without static RAM.

Sintec Co, Box 410, Frenchtown, NJ 08825. Phone (800) 526-5960; in NJ, (908) 996-3891.

Circle No. 365

Serial Communications Controller

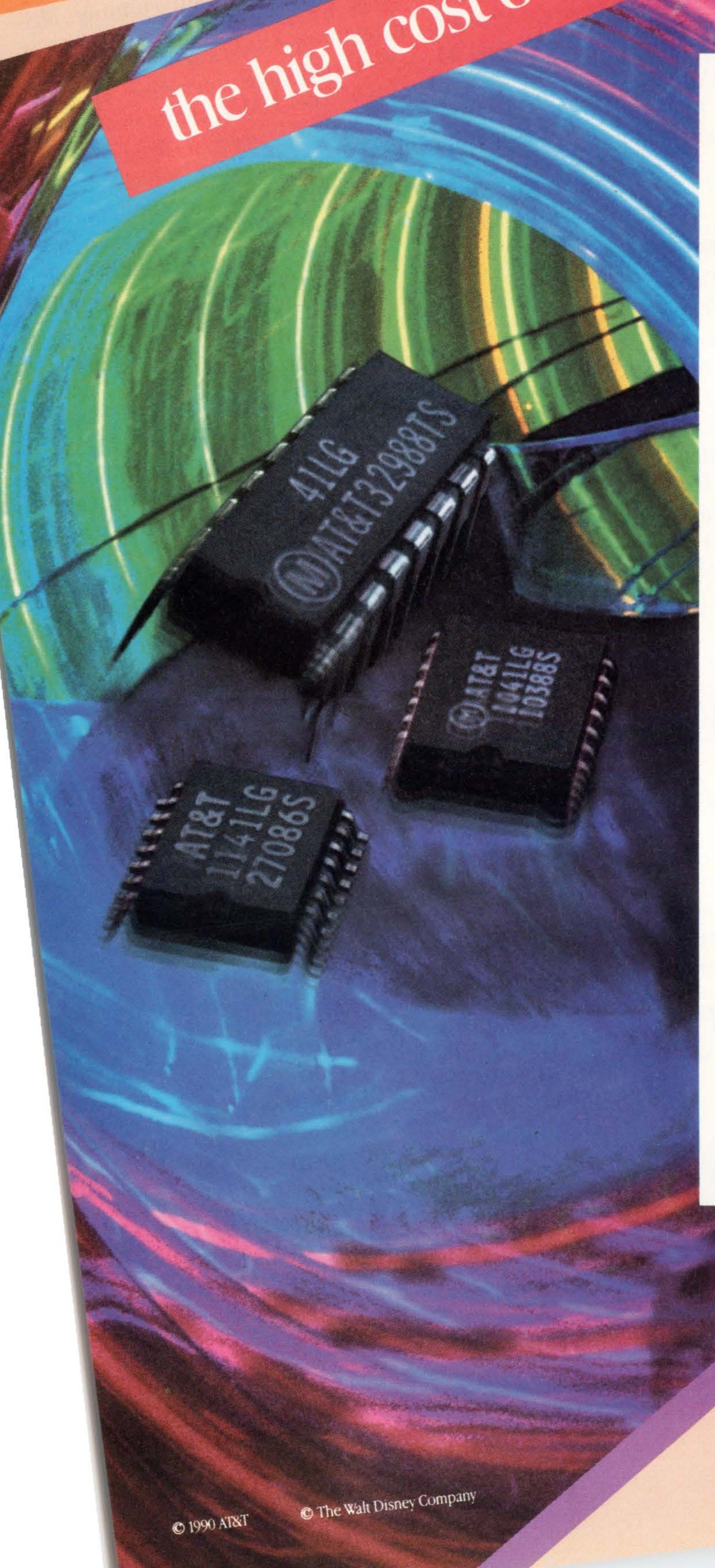
- *Uses an MC68302 controller on 3U Eurocard*
- *Contains 512k-byte data buffer and 2M bits of EPROM*

The GESICC-3 is a serial communications controller board for the G-64/G-96 bus. It uses a Motorola MC68302 serial communications controller (SCC) chip, 512k bytes of data-buffer memory, and 2M bits of EPROM for program storage. You can use the 3U Eurocard with any 80286-based system running MS-DOS or any 68000-, 68010-, or 68030-based system that runs the OS-9 real-time operating system. Six of the DMA channels on the SCC are dedicated to three communications controllers, which enable synchronous or asynchronous HDLC (high-level-data link control) or SDLC (synchronous-data link control) on each port. A seventh DMA channel provides data transfers to and from the host. The board also has a serial TTL output that you can convert to RS-232C, RS-422, or RS-485 outputs using the company's GESINT-X converters. The board comes with firmware that supports asynchronous data transfers. $995.

Gespac Inc, 50 W Hoover Ave, Mesa, AZ 85210. Phone (602) 962-5559.

Circle No. 366

AT&T's new datacom ICs take the high cost out of high speed.



AT&T's new 41 Series of differential quad line drivers/receivers and dual transceivers reach 400 Mb/s with substantially reduced EMI.

Our new datacom ICs do more than offer one of the industry's highest data rates and shortest propagation delays.

Their unique design can take you to 400 Mb/s on common twisted pair—at low EMI levels. This makes them an affordable alternative to fiber, when fiber's other benefits aren't needed.

In system use, they decrease EMI levels up to 30 db compared with standard 26LS TTL ICs. This sharply reduces cabinet design costs. And they meet ESDI standards, making them ideal for disk drive applications.

41 Series devices are pin-for-pin compatible with 26LS ICs—so they're easy to use. They help reduce board complexity and cost via on-chip termination and line-impedance-matching resistors. And they come in space-efficient, surface-mount SOJ and SOIC packages as well as standard DIPs.

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Call **1 800 372-2447** for our databook on 41 Series components, in stock today at Hamilton/Avnet and Schweber.

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CIRCLE NO. 111

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CLR-65	M39006/09	TLX
CLR-69	M39006/21	TXX
CLR-10/14/17	Mil-C-39006/18/19/20	XT
CRL-01/02	Mil-C-83500/01	W13
Module	Mil-C-83500	W14 (Mil Drwg. 89022)
	Silver Tubular	MTPH
	All Tantalum Module	TMX

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- Multiple independent local buses—processor and I/O
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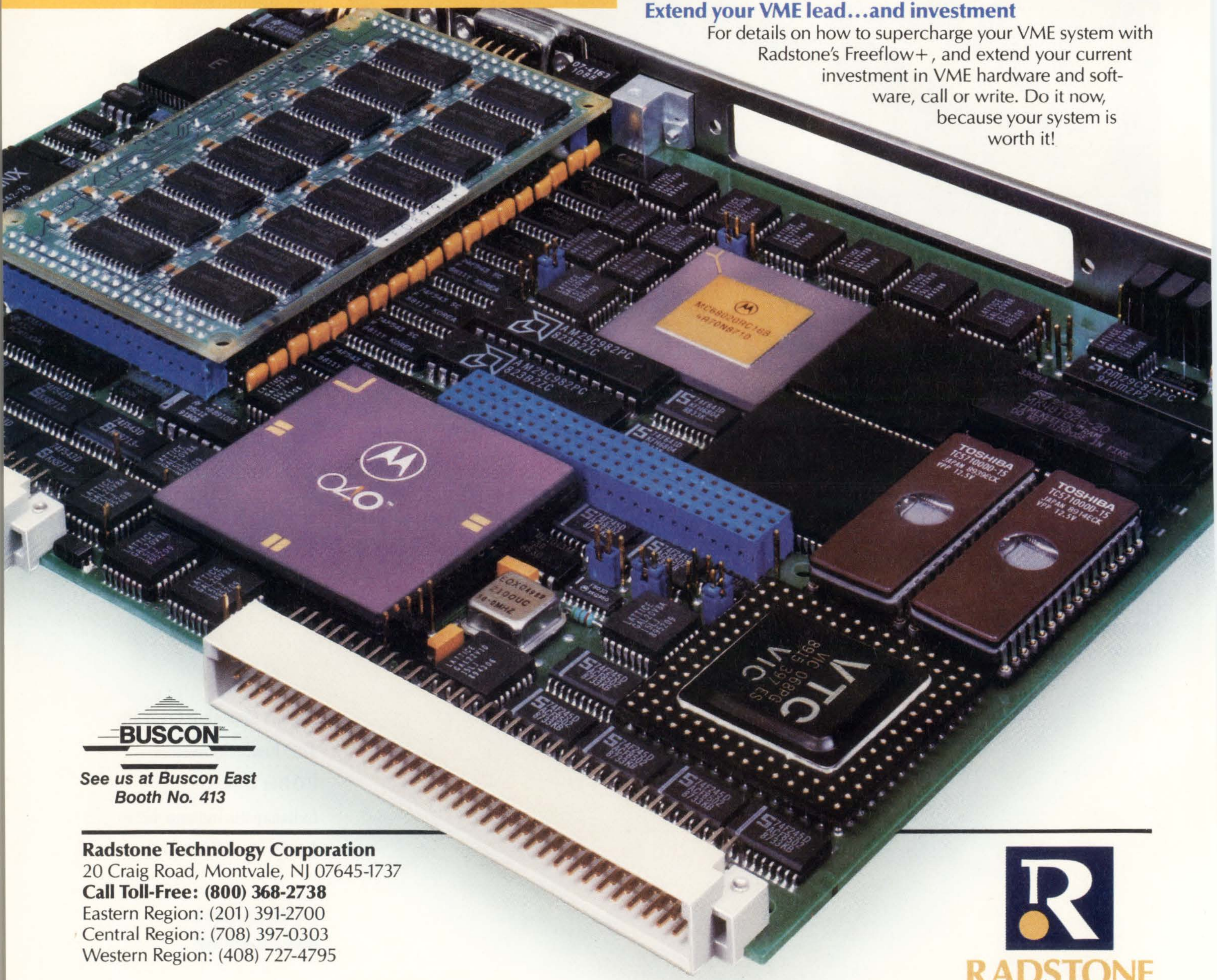
- ...and much, much more.

Radstone's Freeflow+ architecture takes VME to new performance levels. And now it's available with 040 processing punch. It's the very latest in Radstone's long line of leading edge commercial real-time VME board level products.

Extend your VME lead...and investment

For details on how to supercharge your VME system with Radstone's Freeflow+, and extend your current investment in VME hardware and software, call or write. Do it now, because your system is worth it!



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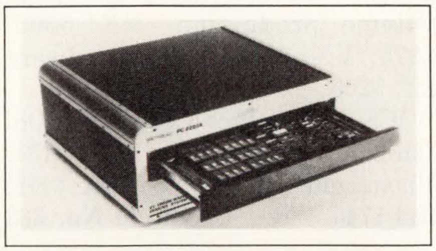


μV Eraser For EPROMs Mounted On Circuit Boards

- *Accommodates boards to 12×16 in.*
- *Erases EPROMs in 5½ minutes*

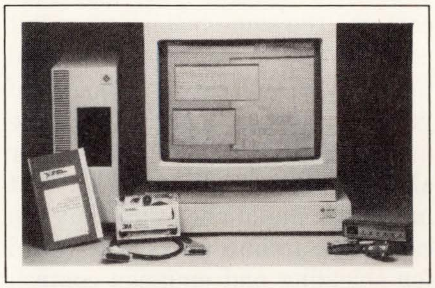
The Model PC-2200A Spectroline μV erasing cabinet works with pc boards as large as 12×16 in. Used in combination with an in-circuit programmer, the device allows you to solder μV-erasable, programmable devices into your board and reprogram them without removing them from the board. The unit maintains an irradiance of 18,500 μW/cm² at a wavelength of 254 nm over a 16×9¼-in. area. This intensity is adequate to erase EPROMs in 5½ minutes, though the unit permits you to set erasure times as long as 1 hour. An indicator shows you when the internal grid lamps are on. An interlock keeps the unit from operating when you open the drawer that accommodates the pc board whose devices you wish to erase. Internal fans maintain a constant temperature in the drawer. A bell signals the end of an erasure operation. $2645.

Spectronics Corp, 956 Brush Hollow Rd, Westbury, NY 11590. Phone (516) 333-4840. FAX (516) 333-4859. **Circle No. 378**

IEEE-488 Interface Kit For Sun-3

- *Lets you SCSI port to control 14 instruments*
- *Includes 64k-byte buffer*

The GPIB-Sun3-S kit provides the hardware and software you need to control as many as 14 IEEE-488 instruments from a Sun-3 workstation's SCSI port. This arrangement allows low-end workstations that can't accommodate plug-in cards to act as instrument controllers. The bus-controller unit, which has its own 8-bit microcontroller, contains a 64k-byte RAM buffer and mounts outside the workstation. The software consists of a set of high- and low-level functions that you install in the operating system as a Unix driver. The driver has true multitasking capabilities that permit multiple IEEE-488 programs, all using the same bus controller, to run concurrently. $1420.



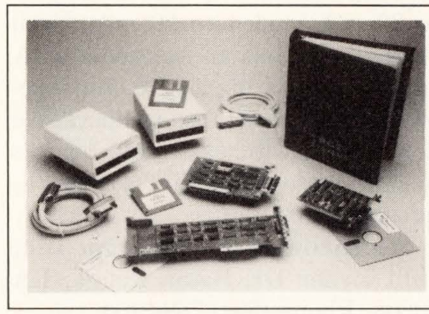
National Instruments Corp, 6504 Bridge Point Pkwy, Austin, TX 78730. Phone (800) 433-3488; (512) 794-0100. FAX (512) 794-8411. **Circle No. 379**

440-MHz Wattmeter And Antenna Tuner

- *Wattmeter has 30 and 300W ranges*
- *Measures 8×2.5×3 in.*

The MFJ-924 440-MHz antenna tuner with built-in standing-wave ratio meter/wattmeter measures 8×2.5×3 in. and handles 200W. The wattmeter has 30 and 300W ranges. The unit has SO-239 input and output connectors as well as a wing-nut post for ground. $69.95.

MFJ Enterprises Inc, Box 494, Mississippi State, MS 39762. Phone (800) 647-1800; in MS, (601) 323-5869. FAX (601) 323-6551. **Circle No. 380**



IEEE-488 Interfaces For ISA And MCA Buses

- *Each controls 14 devices*
- *Transfer data at 300k bytes/sec*

The PCI-803W and PCI-804W are IEEE-488 interfaces for the ISA and Micro Channel Architecture (MCA) buses. Both units can control 14 devices, support DMA, and transfer data at 300k bytes/sec. The interfaces operate as talkers or listeners, perform parallel or serial polling, and support service requests from devices on the bus. When you order the units as part of interface kits, the vendor includes driver software. The software supports popular languages and is compatible with application programs such as Labtech Notebook, Asyst, and DADisp. Kit for ISA bus, $395; for MCA bus, $495.

Burr-Brown/Intelligent Instrumentation, 1141 W Grant Rd, MS 131, Tucson, AZ 85705. Phone (602) 623-9801. FAX (602) 623-8965. **Circle No. 381**

Isolated Analog Input Card For IBM PC Bus

- *Isolation is 1500V between inputs and from inputs to bus*
- *Accepts four 10-kHz signals*

The MSI-4000 isolated analog- input card plugs into the IBM PC bus. It has four signal inputs; each is protected by a surge suppressor and can withstand 1500V to any of the other inputs or to ground. The board's A/D converter resolves 12 bits and handles signals with a 10-

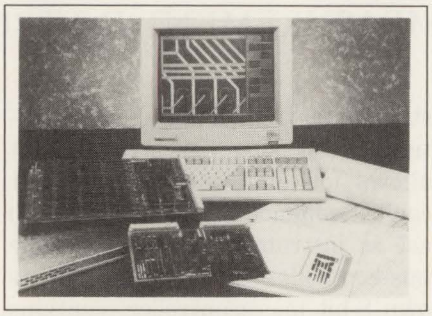
kHz bandwidth. Jumpers select input ranges of 0 to 0.1V, 0 to 5V, 0 to 10V, −5 to 5V, −10 to 10V, 0 to 20 mA, and 4 to 20 mA. Each channel also has an isolated 20-mA supply for exciting 2-wire transducers such as resistance-temperature detectors. Switches set the board's bus addresses and interrupt requests. $380 (100).

Microcomputer Systems Inc, 1814 Ryder Dr, Baton Rouge, LA 70808. Phone (504) 769-2154.
Circle No. 382

VXIbus Prototyping Tool

- *Includes C-size prototyping board*
- *Features ⅓-length card with interface circuits*

The VXI-5500 is a C-size prototyping card for the VXIbus. The interface occupies about one-third of the board area; the remainder of the



board accommodates circuits of your own design. The VXI-5523 contains the same bus interface but is one-third the length of a standard C-size VXIbus card. A board of your own design can plug onto the end of the VXI-5523. The vendor also supplies a hardware kit that includes a metal enclosure that you can place around any C-size board for shielding and emission control. The enclosure also contains slots for cooling. The kit includes conductive gaskets, bushings, and connector skirts. The vendor offers assistance in layout of VXI boards to facilitate a rapid transition from prototype to volume production. VXI-5500, $975; VXI-5523, $700; hardware kit, $200.

ICS Electronics Corp, 2185 Old Oakland Rd, San Jose, CA 95131. Phone (408) 432-9009. FAX (408) 943-1745. **Circle No. 383**

Programmers For PLDs, μCs, EPROMs, EEPROMs

- *One programmer supports all PLDs*
- *Another programs EPROMs and EEPROMs to 4M bits*

The Logic is a universal programmer for all PLDs. The Empro, which incorporates many of the features of the vendor's Unipro universal programmer, can program microcontrollers, EPROMs, and EEPROMs to 4M bits. Both units

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CIRCLE NO. 121

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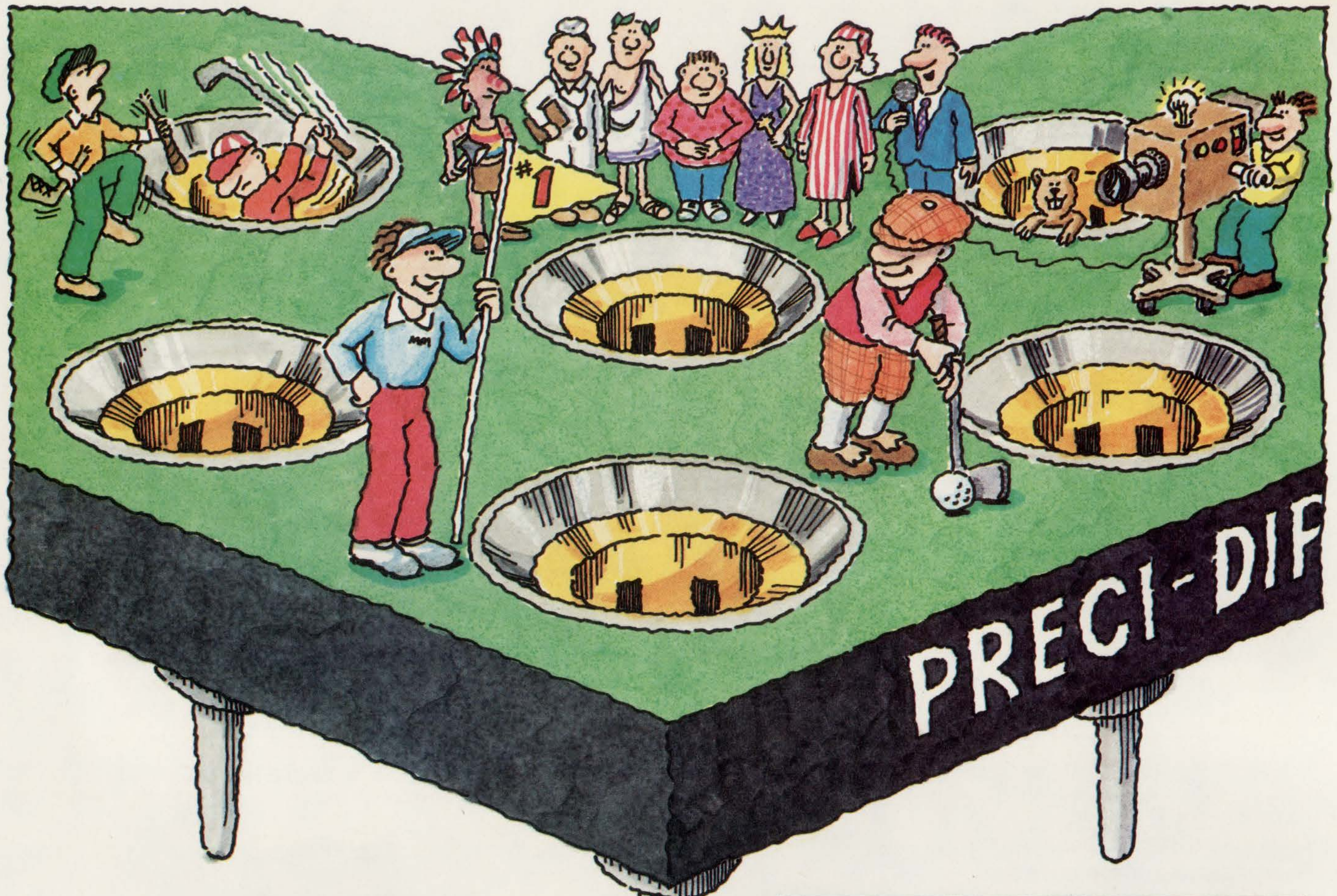

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Product	**Avg. Insertion/Extraction Force**	**Contact Type**
Preci-Dip	135 grams per pin	6 finger, coined
Brand A	141 grams per pin	6 finger, notched
Brand B	158 grams per pin	4 finger, stamped
Brand C	196 grams per pin	4 finger, machined
Brand D	206 grams per pin	4 finger, eyelet
Brand E	273 grams per pin	6 finger, stamped

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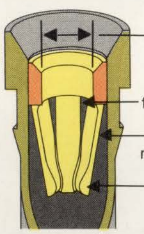
On the PGA socket tour, hacking up a delicate PGA package is a major hazard. To make the cut, you need a socket contact with a soft, gentle touch. That's why the leading pros prefer our 6-finger "coined" contact for its greater compliancy. Check the scorecard to see that Preci-Dip® posted the lowest score for insertion/extraction force. Our inviting .028″ dia. entry funnels down to smooth contact points for easy tap-ins. And to avoid the handicap of solder wicking and flux contamination, every Preci-Dip PGA socket is made using precision machined pins with closed bottoms.



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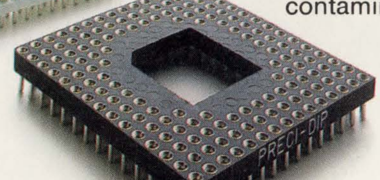

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CIRCLE NO. 165

TAKING THE LEAD

TAKING THE LEAD

require an IBM PC-compatible computer. The Empro includes software called Lops (library operating programmer system). Software for both units combines a command-line interface with windowing and pull-down menus. Both programmers carry the same price tag: $395.

Xeltek, 764 San Aleso Ave, Sunnyvale, CA 94086. Phone (800) 541-1975; in CA, (408) 727-6995. FAX (408) 727-6996.

Circle No. 384

2-Channel, 250-kHz PC-Based FFT Analyzer

- *Takes 1 to 500,000 samples/sec*
- *Averages two to 1024 spectra on each channel*

The R310 2-channel, real-time FFT spectrum analyzer is an IBM PC-based instrument that simultaneously samples both its channels as often as 500,000 times each second. It uses a hardware DSP engine to compute spectra in real time, and simultaneously displays the data in the frequency and time domains. Each channel has a 32k-word data buffer. The unit can average from two to 1024 spectra. Gain is programmable from 10 mV to 50V/div. The software displays both voltage and frequency on linear or logarithmic scales. Among the software features is automatic saving of spectra to disk. $1995.

Rapid Systems Inc, 433 N 34th St, Seattle, WA 98103. Phone (206) 547-8311. TLX 265017.

Circle No. 385

Microstrip Test Station

- *Operates from dc to 26.5 GHz*
- *Fits under wire bonders and on rackmount tablets*

The MTF26 microstrip test station permits accurate probing of microwave and millimeter-wave integrated circuits, discrete components, and hybrid assemblies operating from dc to 26.5 GHz. The unit handles devices as small as 0.12 in. square and as large as 4 in. square. The vendor claims that errors in measurements made with the unit are two orders of magnitude lower than errors in measurements made using earlier handlers. Repeatability is better than −46 dB. The unit fits under wire bonders and on rackmount tablets. Optional calibration standards ensure accuracy from 750 MHz to 26.5 GHz. $12,500; calibration kit, $2500; monocular optics, $2695.

Cascade Microtech Inc, Box 1589, Beaverton, OR 97075. Phone (503) 626-8245. FAX (503) 626-6023.

Circle No. 386

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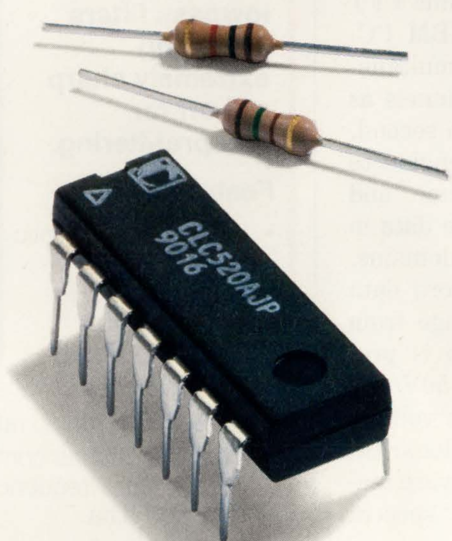
Now, high-speed AGC is easier than ABC.

Until now, AGC amplifiers were only partial solutions to high-speed automatic gain control. You also had to find a high-performance op amp, numerous passive components and the board space to mount them all.

Now all you need is the new CLC520 AGC+*Amp*, ±5V and two resistors. That's it.

You get a total high-speed AGC solution–with voltage-controlled gain and voltage output–in a single device. Plus outstanding performance: 160MHz signal-channel and 100MHz gain-control bandwidth. And unexpected flexibility... one resistor sets maximum gain between 2X and 100X, and the gain-control input gives you a 40dB range.

So don't settle for a partial AGC solution. Call about the CLC520 AGC+*Amp* and learn the ABCs of high-speed AGC.



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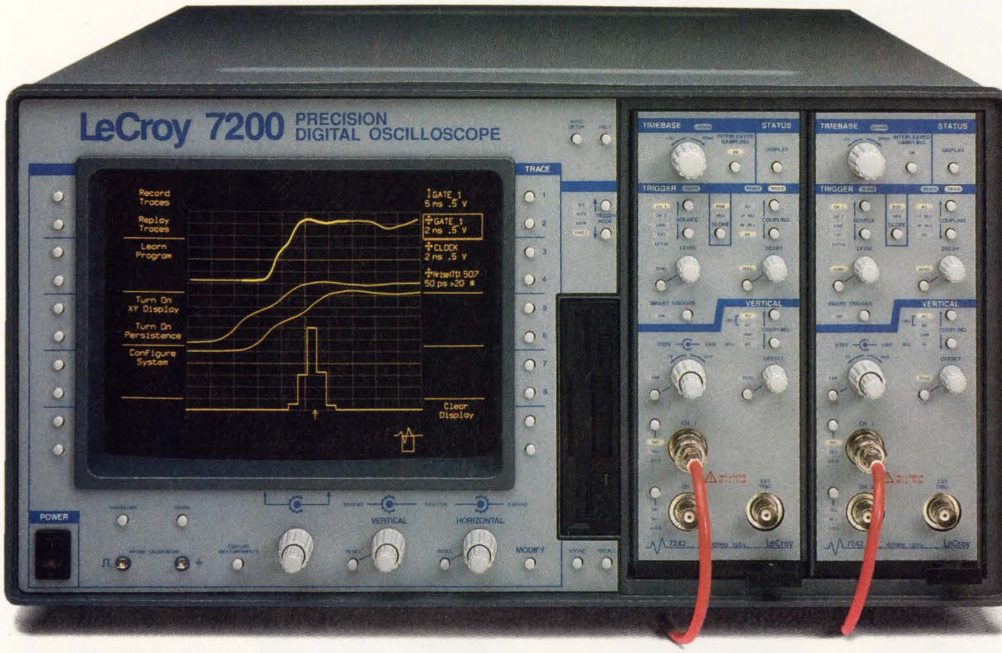
CIRCLE NO. 115

2 GIGS-A-CHANNEL!



Now get real-time sampling at up to 2 gigasamples/second using 8-bit ADCs on each channel. The 7200 is the digital oscilloscope with an analog personality – simply easy to use. Display your data in seconds instead of hours via instant auto-setups and built-in help.

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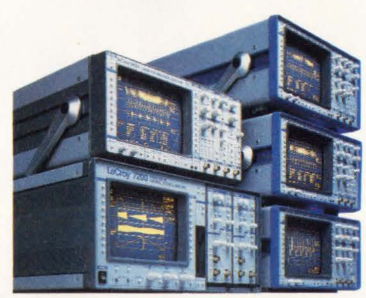
- **2 GS/sec on 2 ch. for transients**
- **1 GS/sec on 4 ch. for transients**
- **20 GS/sec on 4 ch. repetitive**



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Circle #116 for demonstration

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Since their introduction, Wren® disc drives have been among the most sought after in the industry. With their high capacity and sterling performance features, it's no wonder we've been hard-pressed to fill all the orders. Fortunately, that's now changed.

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Seagate

CIRCLE NO. 118

NEW PRODUCTS

CAE & SOFTWARE DEVELOPMENT TOOLS

ASIC Design Tool

- *Analyzes power consumption, skew, and critical paths*
- *Runs on the vendor's simulation accelerator*

Advanced ASIC Designer is a set of software tools that runs on the vendor's Mach and XP simulation accelerators. Powersim takes into account the switching activity and capacitance of all nodes, the operating voltage, and the constant leakage current. It then computes the instantaneous energy consumption at each time point for the whole circuit or any subcircuit. Pinskew determines your design's sensitivity to variations in the timing of input and output signals. By moving each signal independently forward and backward in time, the program can detect timing sensitivities that other test procedures could miss. Critical Pathfinder operates dynamically, using the circuit description and actual test vectors. The program provides data that helps you determine where delays occur and speed up a circuit. $60,000.

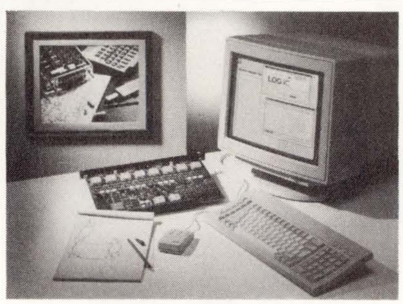
Zycad Corp, 1380 Willow Rd, Menlo Park, CA 94025. Phone (415) 688-7400. FAX (415) 688-7550.
Circle No. 387

Data-Protection Software

- *Automatically writes to two identical hard-disk drives*
- *Notifies you if either disk fails*

The Immunity software data-protection package runs under PC/MS-DOS 3.2 or higher on IBM PCs, PS/2s, and compatibles. The program requires that the computer be equipped with two identical hard disks; it can work with most standard disk controllers and coding schemes such as MFM, RLL, ESDI, and SCSI. The software intercepts all disk-write operations and writes the data in duplicate to the same physical sectors on both drives. If the primary drive fails, the program notifies you and automatically switches over to the secondary drive (or vice versa). Read operations are performed by whichever drive has its heads closer to the required data; the decreased seek time more than compensates for the extra time needed for writing to the second disk. The program sends all details of disk errors to an error log and includes disk-repair utilities to aid in troubleshooting and resynchronizing the disks after an error. Immunity version 2.41 uses only 5k bytes of main memory and is compatible with a number of DOS-based LAN operating systems. $345.

Unitrol Data Protection Systems Inc, 815 Hornby St, Suite 604, Vancouver, BC V6Z 2E6, Canada. Phone (604) 681-3611. FAX (604) 687-0814. **Circle No. 388**



VHDL Compiler For IBM PCs And Compatibles

- *Can implement VHDL descriptions as PLDs or gate arrays*
- *Provides automatic state reduction and assignment*

Hint is a preprocessor for the vendor's LOG/iC design tools. It accepts a subset of the VHDL-1076 (VHSIC hardware description language) standard, allowing you to describe finite state machines (FSMs) as well as sequential and combinatorial logic. The preprocessor translates your descriptions into

a format that is acceptable to the LOG/iC PLD or gate-array compilers. You can also use a mixture of VHDL and LOG/iC's FSM syntax. Hint automatically eliminates redundant states and assigns codes to those that remain after the reduction. Once Hint has successfully completed compilation of the VHDL descriptions, you can further process the results with the LOG/iC compilers. They perform logic reduction and create either output files containing programming and test data for PLDs or a net list for gate arrays. Hint runs on IBM PC/ATs, PS/2s, and compatibles; your computer must run DOS 2.0 or later and have at least 400k bytes of memory available to Hint. $2380.

Isdata Inc, 800 Airport Rd, Monterey, CA 93940. Phone (408) 373-7359. FAX (408) 373-3622.

Circle No. 389

Ethernet Network Analyzer For Macintosh

- *Works with most Ethernet controller cards*
- *Can be activated at any Macintosh node on a network*

Etherpeek is a software package that runs on any Macintosh II or SE/30 computer and helps you analyze the performance of an Ethernet network. The Macintosh must run System 6.0 or a later version. The program captures every packet that is transmitted on the network, regardless of address. It can display bar graphs to show the level of activity of each node, and you can scale the graphs to provide meaningful comparisons. To make recognition easier, you can replace protocol types and physical addresses with logical net and node numbers or with symbolic names. You can start and stop capture when a specified network event occurs, or filter the data to capture only packets that meet criteria you specify. Every packet is timestamped with a resolution of 1 msec. And, you can display the timestamps as an absolute 24-hour time of day, as a relative time since the last packet was received, or as a relative time since the beginning of your session. You can also generate diagnostic traffic on the network, specifying the contents of the packet to be sent, the number of times to send it, and the interval between transmissions. You can transport the program on floppy disk and run it from any Macintosh node on the network. $475.

Avant Garde Group, 2540 Camino Diablo, Suite 202, Walnut Creek, CA 94596. Phone (415) 937-7900. FAX (415) 937-2479.

Circle No. 390

Filter-Design Software

- *Handles all standard transfer functions*
- *Editor lets you fine-tune your design*

Advanced Filter Designer is a software package that runs on Macintosh computers, IBM PC/ATs, PS/2s, and compatibles. The algorithms apply classical approximations to your filter specification; you can synthesize Butterworth, Chebyshev, inverse Chebyshev, and elliptic (Cauer) transfer functions for lowpass, highpass, bandpass, and bandstop filters. You can also synthesize arbitrary transfer functions and delay-equalization filters. A built-in editor lets you insert, delete, and reorder filter stages and modify coefficient values to fine-tune a design. The program allows the design of both active-RC and switched biquad filter structures; the program can scale or resize the components to center the values in the preferred ranges. You can define arbitrary functions by specifying minimum and maximum transfer-function limits at a number of frequencies. The program then creates the final transfer function with numerical-optimization (nonlinear

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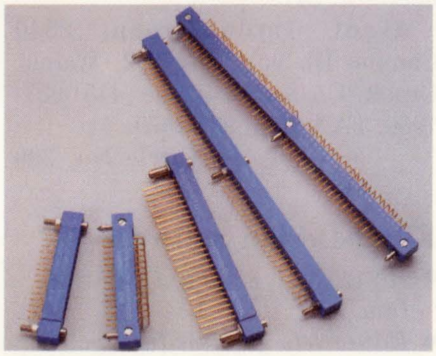
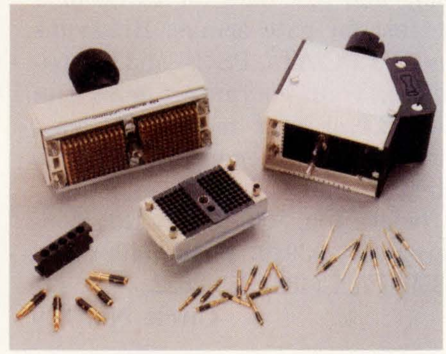
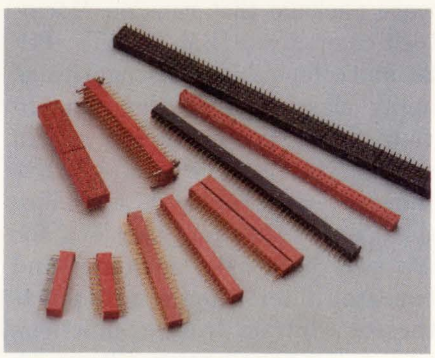


***KA Series:** 17-490 Contacts with D55302-Listed Qualified Models.*



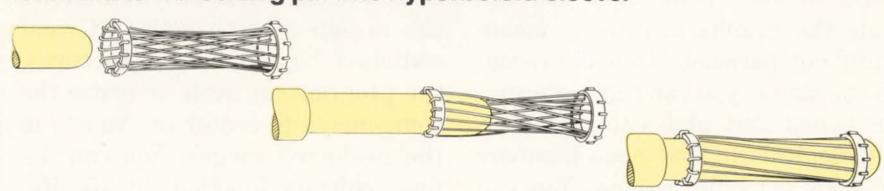
***N Series:** 70-700 Position Connectors with Ratings to 9 Amps.*



***KG Series:** 22-90 Position Board Stacking for .240 or .480 Heights Between Boards.*

***Y Series:** 3-500 Amp Discrete Pins and Mating Sockets.*

HYPERTAC®: Inserting pin into hyperboloid sleeve.



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programming) techniques. To run the program, the PC or compatible must have at least 512k bytes of memory, a math coprocessor, and an EGA or VGA color-graphics card. PC version, $1800; Macintosh version, $2700.

MicroSim Corp, 20 Fairbanks, Irvine, CA 92718. Phone (714) 770-3022. FAX (714) 455-0554.

Circle No. 391

C Cross-Compiler For i960 RISC Processors

- *Comes with instruction scheduler and a driver*
- *Generates COFF symbolic debug tables*

The Archelon C cross-development package runs on Sun 3 workstations or 16- or 32-bit IBM PCs and compatibles. It generates code for Intel's i960 family of 32-bit RISC (reduced-instruction-set computer) processors. The package consists of an optimizing ANSI C compiler, an ANSI C runtime library, an instruction scheduler, and a driver program. The optimizing compiler is compatible with Intel's i960 C compiler; optimizations include global common-subexpression elimination, automatic generation of leaf functions, automatic binding of variables to registers, constant folding, branch prediction, tail-recursion elimination, and peephole optimization. The output of the compiler is an assembly-code file and COFF (common object-file format) symbolic-debug tables. The instruction scheduler uses resource-usage and data-dependency information to minimize pipeline stalls. It can operate with either hand- or compiler-generated code. The driver program automates the generation of executable programs; it works in conjunction with Intel's ASM960 and LNK960 for assembly and linking. A single command allows you to initiate all compilation, assembly, and linking operations. 16-bit MS-DOS version, $750; 32-bit MS-DOS version, which requires an 80386/486-based host, $1250; Sun-3 version, $1500.

Archelon Inc, 460 Forestlawn Rd, Waterloo, Ontario N2K 2J6, Canada. Phone (519) 746-7925.

Circle No. 392

Action-Diagram Editor For PCs And Compatibles

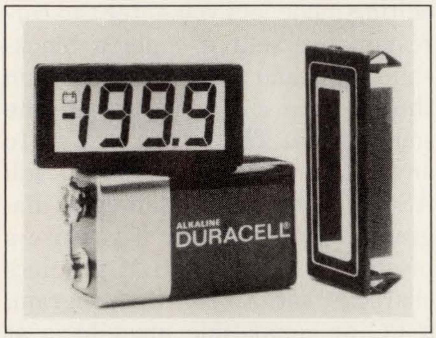
- *Graphics editor lets you build CASE action diagrams*
- *Text editor converts action diagrams to C or Pascal source code*

Stage # 1 is a tool for structured (top-down) software analysis and design. It lets you define the software structure from the topmost overview down to the lowest level of pseudocode. The graphics editor allows you to insert both single-pass and loop-structure bracket lines with automatic indentation according to the nesting level. It also lets you place both exit arrows and next-iteration arrows. When your design structure is complete, a text-editing mode lets you enter the corresponding source code; a block-shift command helps you maintain the indentation structure in the source code. The output can go to any printer that generates the full ASCII character set; however, diagrams will look better if you use a printer that has the IBM graphics character set. To run the program, a PC or compatible must have at least 256k bytes of memory (the vendor recommends 640k bytes). The package includes several utility programs, diagram templates, and examples. $189; orders placed before November 1, 1990, $159.

Mt St Helens Software, Box 3319, Pasco, WA 99302. Phone (509) 547-2582. **Circle No. 393**

NEW PRODUCTS

COMPONENTS & POWER SUPPLIES



LCD Panel Meters

- *Feature 0.5-in.-high display*
- *Draw a maximum of 100 mA*

The Lascar Series DPM-125/116 3½-digit digital panel meters feature a 0.5-in. LCD readout; Model 116 also features true digital hold. Both meters measure 1.89×0.94×0.26 in. and will mount into a SIP socket or on a panel using a snap-in bezel furnished with all units. The meters are accurate to 0.1%±1 count and operate over a 0 to 50°C range. Standard features include auto zero, auto polarity, 200-mV full-scale deflection, and 100 mA max current consumption. The displays also feature a low-battery indicator. On-card solder pads are readily accessible to make in-field decimal-point and operating-mode selection quick and convenient. $35.90.

Martel Electronics, Box 897, Windham, NH 03087. Phone (603) 893-0886. FAX (603) 898-6820.

Circle No. 367

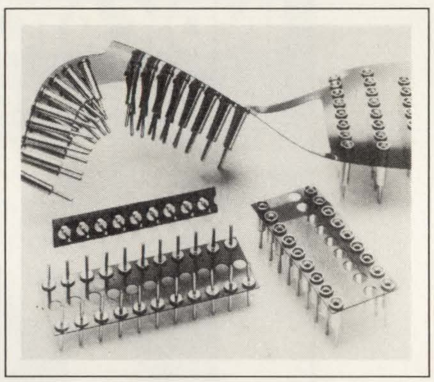
Laboratory Power Supplies

- *Output 30 kV*
- *Feature user-selectable outputs*

The Alpha III line of precision laboratory supplies includes the 3507, which outputs 5 kV; the 3707, which has a 15-kV output; and the 3807, which outputs 30 kV. Maximum output currents are 10, 3, and 1.5 mA, respectively; respective maximum ripple figures are 0.5, 1.5, and 3V. The front panel includes meters for current and voltage status as well as a Local or Remote switch that provides output control and allows you to select the protection mode. The series provides two protection modes: One is limited with automatic crossover between adjustable voltage and current limit, and the other is limited with adjustable voltage and current trip levels. An optional facility allows you to control the supplies with a computer through an RS-232C interface. Positive or negative outputs are user selectable. Load and line regulation equal 0.002 and 0.001%, respectively. From $2672.

International Power Sources Inc, 200 Butterfield Dr, Ashland, MA 01721. Phone (508) 881-7434. FAX (508) 879-8669.

Circle No. 368



Screw-Machine Sockets

- *Available on removable film carrier*
- *Come in DIP, SIP, and PGA configurations*

Aimed at low-profile, high-density applications, these IC sockets come affixed to a film carrier which is removed after the soldering operation. The devices are available in DIP, SIP, and pin-grid-array configurations. The sockets and carriers withstand temperatures ranging from −259 to +400°C—a range that's compatible with all soldering techniques. The free-standing

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	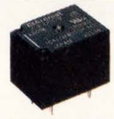		
Contact Arrangement	1A, 1C	1A, 1C, 2A, 2C	1A, 1C
Rated Load	10A 125VAC 6A 277VAC 5A 30VDC	5A 125, 277VAC 5A 30VDC	10A 125, 277VAC 10A 30VDC
Construction	Plastic sealed	Plastic sealed	
Terminals	PCB	PCB	
Coil Types	5, 6, 9, 12, 24, 48VDC	5, 6, 9, 12, 24, 48VDC	
Coil Power	360mW	530mW	
Electrical Life	100,000 operations	100,000 operations	
Approvals	UL/CSA/TÜV	UL/CSA/TÜV	
Dimensions	.866″ × .630″ × .646″	1.126″ × .504″ × .803″	
Directly Replaces	AZ-AZ4 Fujitsu — FBR100, FBR160 Guardian — 1575 Idec — RCN Magnecraft — W178 Midtex — 296 NEC — MR31, MR301 Omron — G4S, G5L Original — SRU, SRW P&B — T70	Fujitsu — FBR610, FBR620 Guardian — 1655, 1665 Idec — RG Midtex — 409 NEC — MR71, MR72 Omron — G2R Original — OMI-SU P&B — RKA Takamisawa — VB, VS	

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socket terminals enhance visual-inspection procedures, ease flux removal, and improve heat dissipation. The sockets have a 0.031-in. above-board profile. Male pins that mate with the sockets are also available to satisfy modular board-to-board interconnection needs. These pins are available in a choice of tin or gold platings. $0.035 to $0.07/line for sockets; $0.04 to $0.07 and $0.055 to $0.07/line for tin- and gold-plated male pins, respectively. Delivery, six weeks ARO.

AMP Inc, Box 3608, Harrisburg, PA 17105. Phone (800) 522-6752.

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Measuring only 0.37×1.7×1.0 in., OACM-UJ solid-state relays are UL recognized, CSA certified, and meet VDE requirements. Switching capacity of the units' spst NO output switch is rated for 6A at 12 to 280V ac. The units operate with 3 to 15V dc inputs. A dV/dt snubber network across the output limits the rise of voltage transients and guards against false triggering. The relays are available in random-voltage and zero-voltage turn-on versions; both versions provide 4000V rms isolation between the optically coupled input and output. $5.94 (500). Delivery, stock to six weeks ARO.

Potter & Brumfield Inc, 200 S Richland Creek Dr, Princeton, IN 47671. Phone (812) 386-2194.

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- *Is IBM compatible*

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Honeywell Inc, Keyboard Div, 4171 N Mesa St, El Paso, TX 79902. Phone (915) 543-5503.

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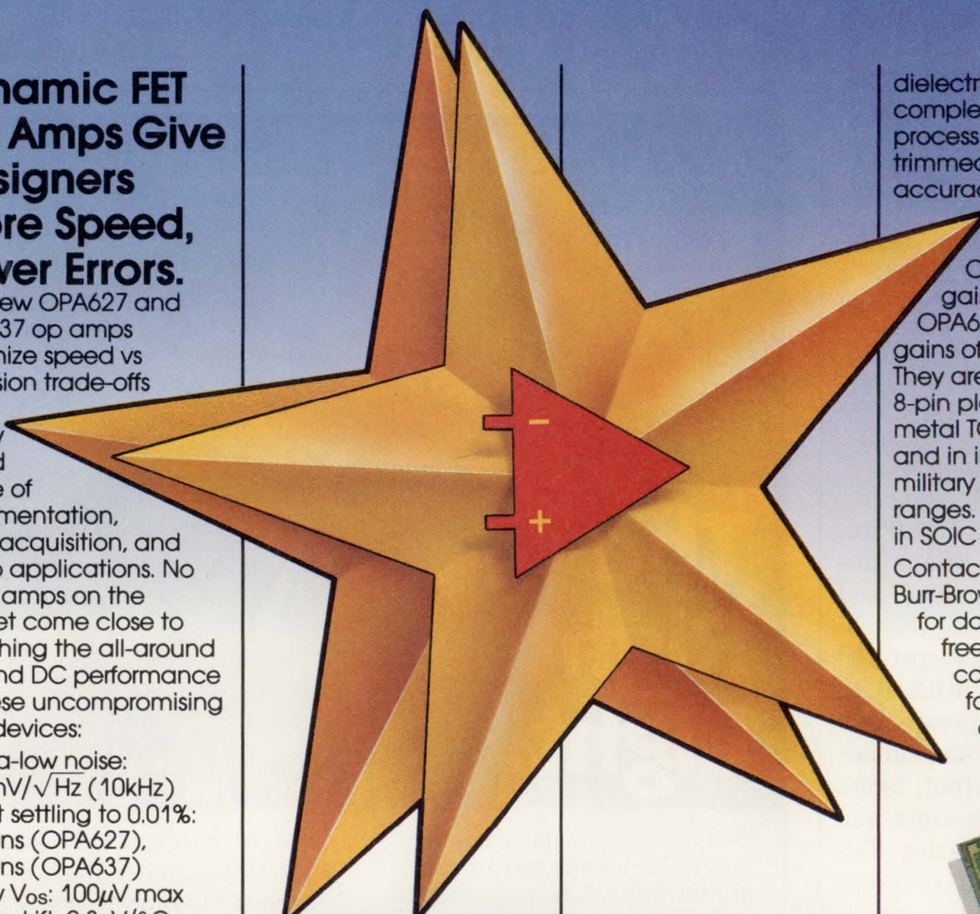
All-Star Performers



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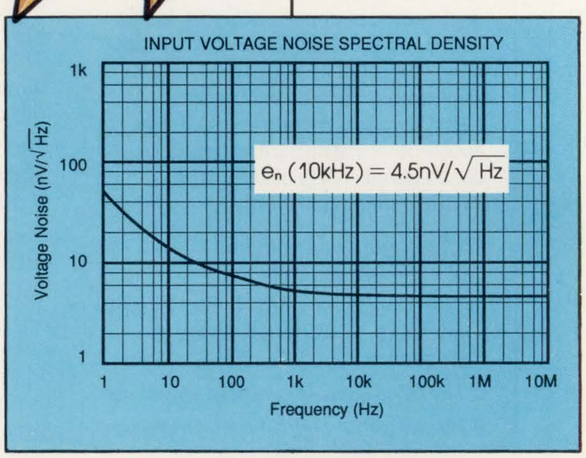

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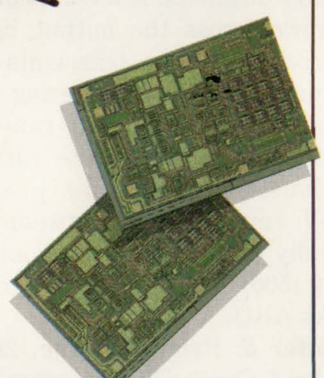

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JST Corp, 1200 Business Center Dr, Suite 400, Mount Prospect, IL 60056. Phone (800) 292-4243; in IL, (708) 803-3300. FAX (708) 803-4918.

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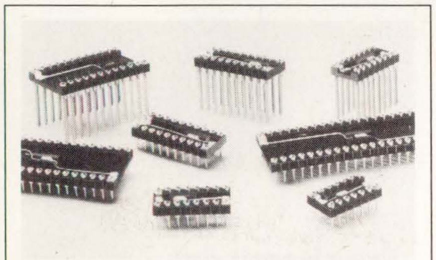

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- *Available with 0.300 and 0.600-in. pin spacings*
- *Offer a choice of terminations*

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Samtec Inc, Box 1147, New Albany, IN 47151. Phone (812) 944-6733. FAX (812) 948-5047.

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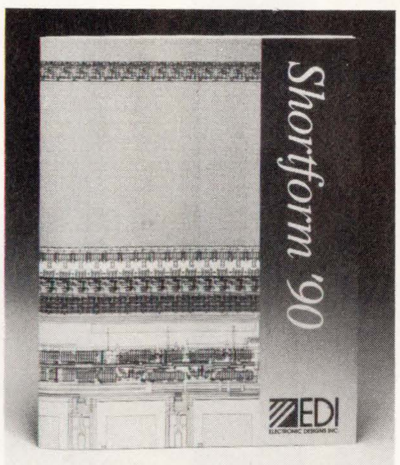
How To Design For Reduced EMI

Design and Layout of a Video Graphics System for Reduced EMI explains electromagnetic compatibility and how to reduce radiated emissions and EMI in the design of high-speed video graphics. The note describes how to incorporate a video RAM D/A converter into a PC or a plug-in board with minimum noise pollution. The note's four sections deal with International EMI regulatory bodies, system noise identification, personal-computer board layout and design, and practical examples of an IBM VGA-compatible board design and its associated FCC testing.

Analog Devices, Literature Center, 70 Shawmut Rd, Canton, MA 02021. **Circle No. 374**



Listings Of Standard Memory Products

This 1990 short-form catalog contains complete listings of the vendor's standard memory products. Tables include part numbers, features, speeds, current consumption, available package types, and scheduled availability of samples and production volumes. Covering both commercial and military products, the tables present 1M-bit monolithic dynamic RAMs, monolithic static RAMs, power-consumption levels, and "chip enable" configurations. A separate table lists the Standardized Military Drawing numbers of the nine memory devices that the vendor manufactures under approval of the Defense Electronics Supply Center.

Electronic Designs Inc, 42 South St, Hopkinton, MA 01748. **Circle No. 375**

Guide To Semiconductor Products

This 26-pg booklet discusses standard linear products, bipolar PROMs, low-power ECL gate arrays, linear semicustom and custom arrays, and small-signal transistors. The book also contains a complete standard linear cross-reference guide, qualified-product lists, surface-mount-device drawings, and packaging information.

Raytheon Co, Semiconductor Div, 350 Ellis St, Mountain View, CA 94043. **Circle No. 376**

Handbook Of Synchro Conversion Products

This comprehensive handbook covers subjects such as Fundamentals; Theories of Operation for Various Types of S/D and D/S converters; Measuring and Computing Performance Parameters, and Typical Applications and Interface Considerations. Designed as a practical tutorial and reference source, the handbook examines not only the vendor's approach to synchro conversion but also other generally accepted techniques. The section on product information is divided according to function; it offers data sheets for hybrid and discrete components, transformers, computer I/O cards, test instruments, and special-function products. A selection of application notes that supplement the handbook is also available.

ILC Data Device Corp, 105 Wilbur Pl, Bohemia, NY 11716. **Circle No. 377**

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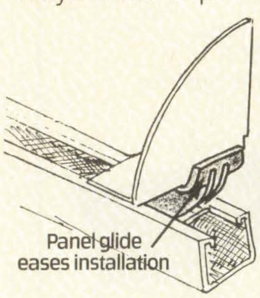

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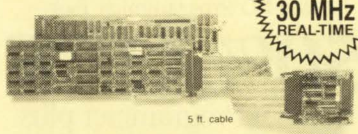

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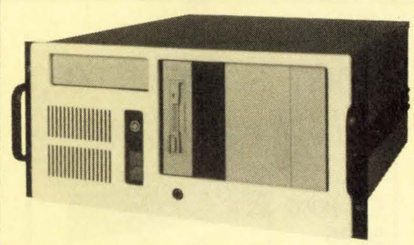

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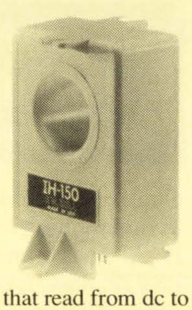

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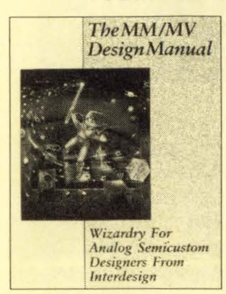

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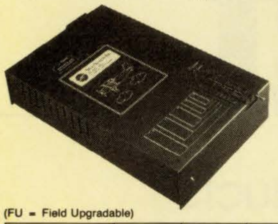

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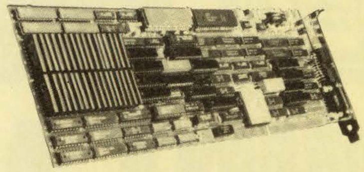

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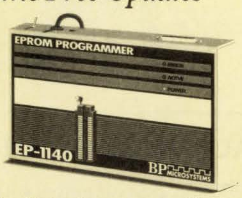

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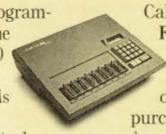

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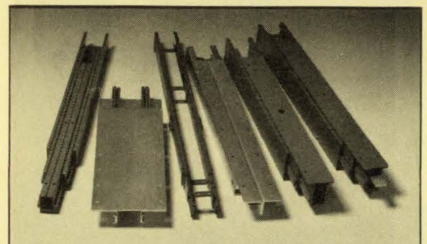

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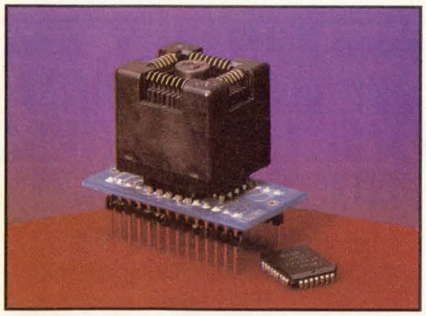

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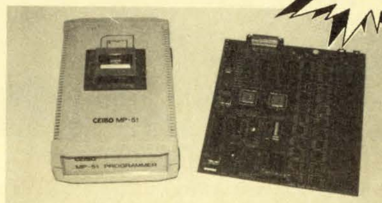

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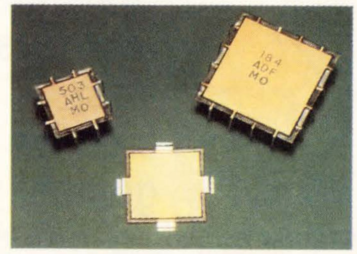

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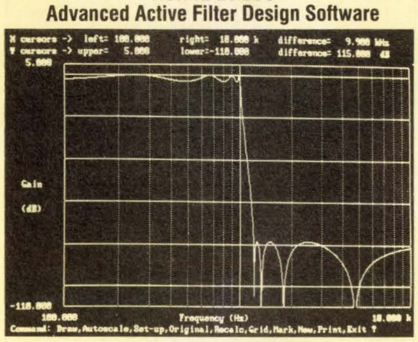

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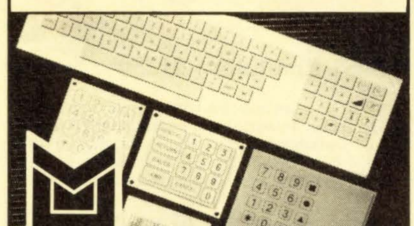

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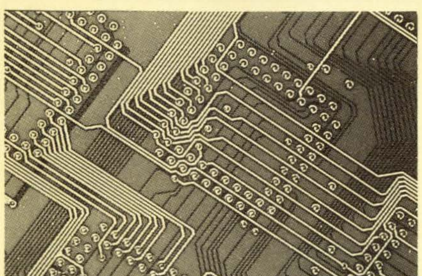

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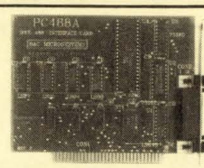

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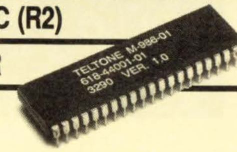

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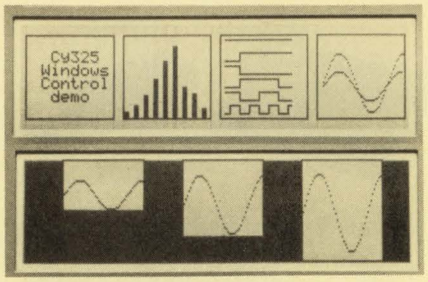

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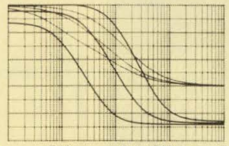

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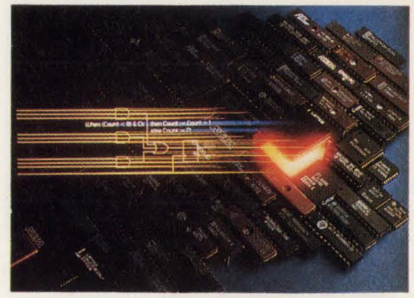

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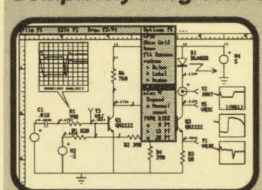

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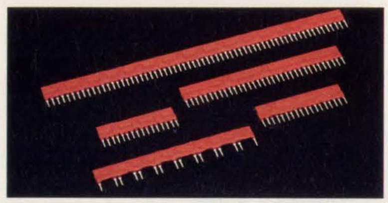

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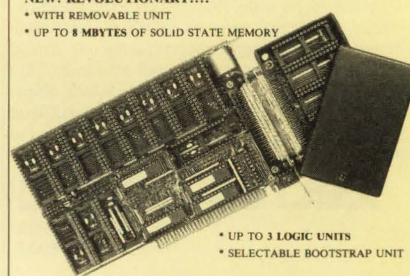

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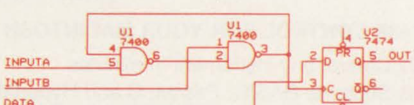

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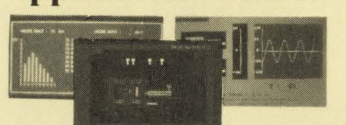

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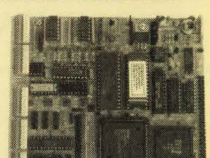

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Magazine Edition	Nov. 22	Nov. 1	17th Annual Microprocessor Directory, ICs & Semiconductors, Test & Measurement, Workstations
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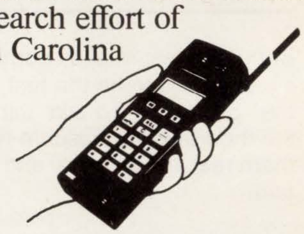

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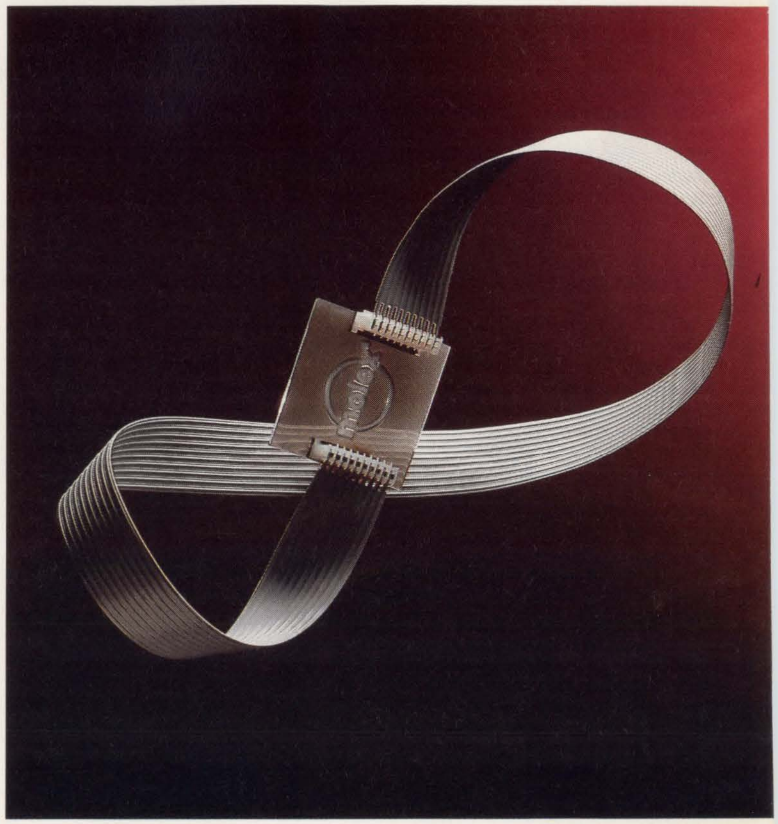

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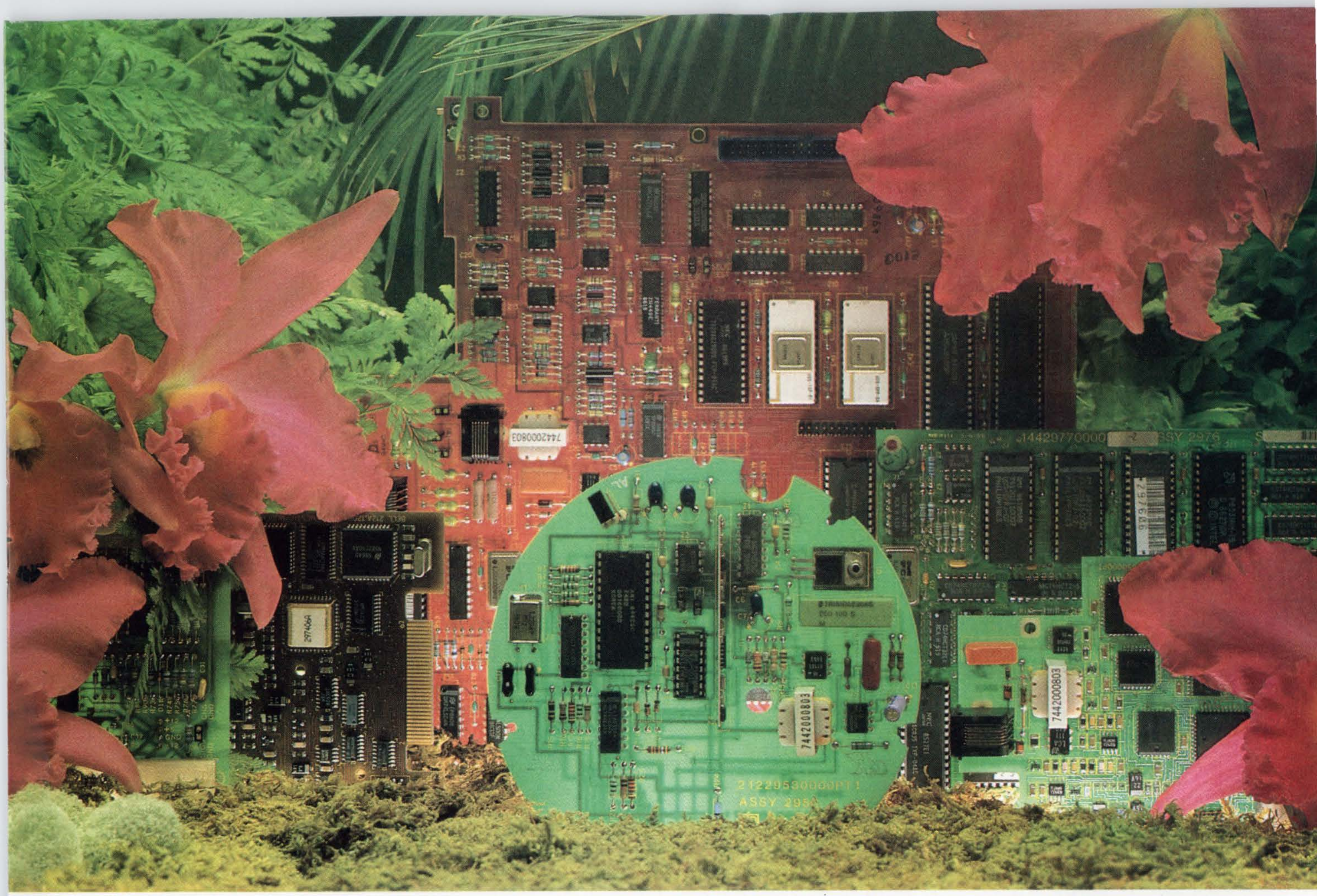

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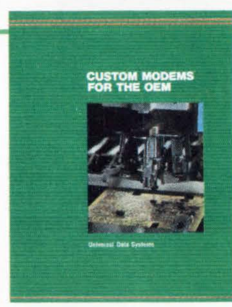

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