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OCTOBER 1, 1990

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ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

Special Report:
Making the transition to Futurebus+

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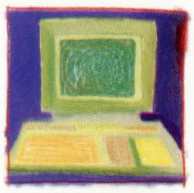
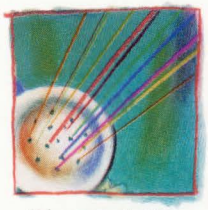

PC Collection


Peripheral Collection


Data Communications Collection


Industrial Collection


Telecommunications Collection


Graphics Collection

high-density versions.

Some of the most contemporary ASIC art is in data communications design. Where increasingly complex network requirements are creating new challenges for designers.

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For ASIC art with industrial strength, take the *Industrial Collection*™ to work with you. It offers everything you need to make your industrial application a memorable one. Whether you're designing controllers, instrumentation, process control or robotic systems.

At the heart of the collection is Fujitsu's family of DSP core controllers, which support fixed and floating-point operations and a variety of finite word lengths.

So you get controllers and vision systems that are inexpensive, fast and easily programmable.

Now that the industry is implementing the ISDN standard, what you need most is an ASIC that supports it. Which brings us to the *Telecommunications Collection*.™

The collection meets telecom design needs. Offering standardized building blocks such as DSP cores and other functions to implement standard protocols and enhanced features.

If you're a graphics designer, you know that 3-D graphics have turned into 3-D art. And the best way to create it is with the *Graphics Collection*.™

The Graphics Collection integrates functions onto a single device which are unavailable as standard products. Cutting your design time and honing your competitive edge.

In addition to getting SuperMacros for most of the 2900 family, the collection also provides you with RAM and ROM compilers and specialized graphics algorithms.

All in all, there's no better way to begin your next ASIC design than with a visit to the ASIC Gallery.

Stop by and tour the collections. Call 1-800-642-7616. We'll be happy to show you around.

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CIRCLE NO. 95

Welcome to the ASIC Gallery.™

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A is for art. And also for ASIC. We put them together to bring you the ASIC Gallery. Six masterful collections of applications-oriented products and services let you create your own design masterpiece.

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Each collection contains building blocks that let you design more compact, higher performance systems in far less time.

All in a CMOS environment using Fujitsu's high-speed .8μ channeled and channelless gate-array technologies as your foundation. Just choose the collection that's right for you.

The *PC Collection*™ lets you paint a PC portrait you'll be proud of. Using SuperMacros™ and compiled cells for 8086/8088/80186 and 80286-based PCs and laptops.

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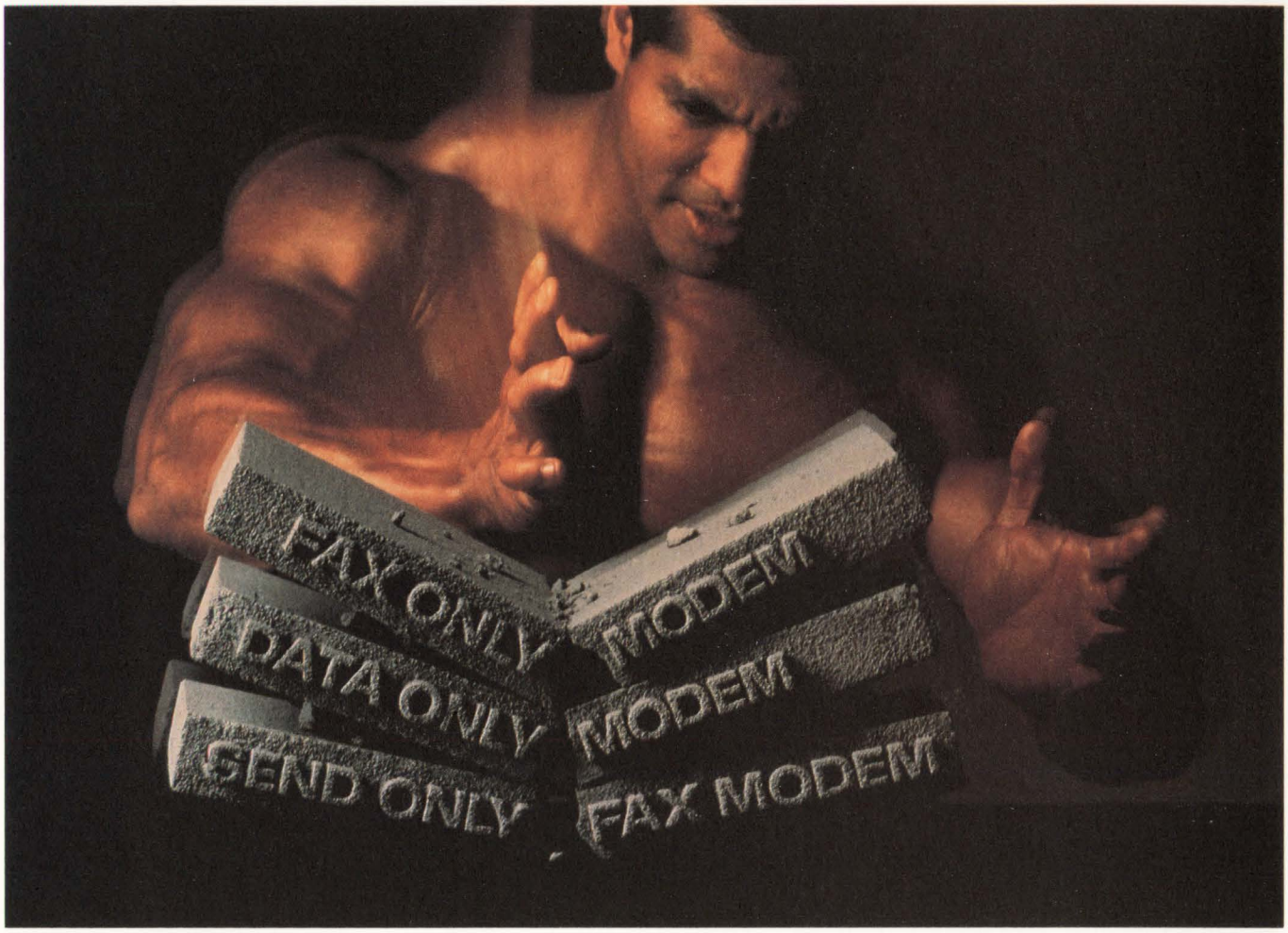
If your taste in ASIC art runs to peripherals, check out the *Peripheral Collection*.™ Its high level of integration incorporates greater functionality in a smaller footprint.

Plus you get support of industry standards like SCSI. As well as 8200 SuperMacros and RAM compilers in both high-speed and

You're invited to an exhibit of modern ASIC masterpieces.

EXAR Fax/Data Combo Breaks the Barrier



Break away from the competition

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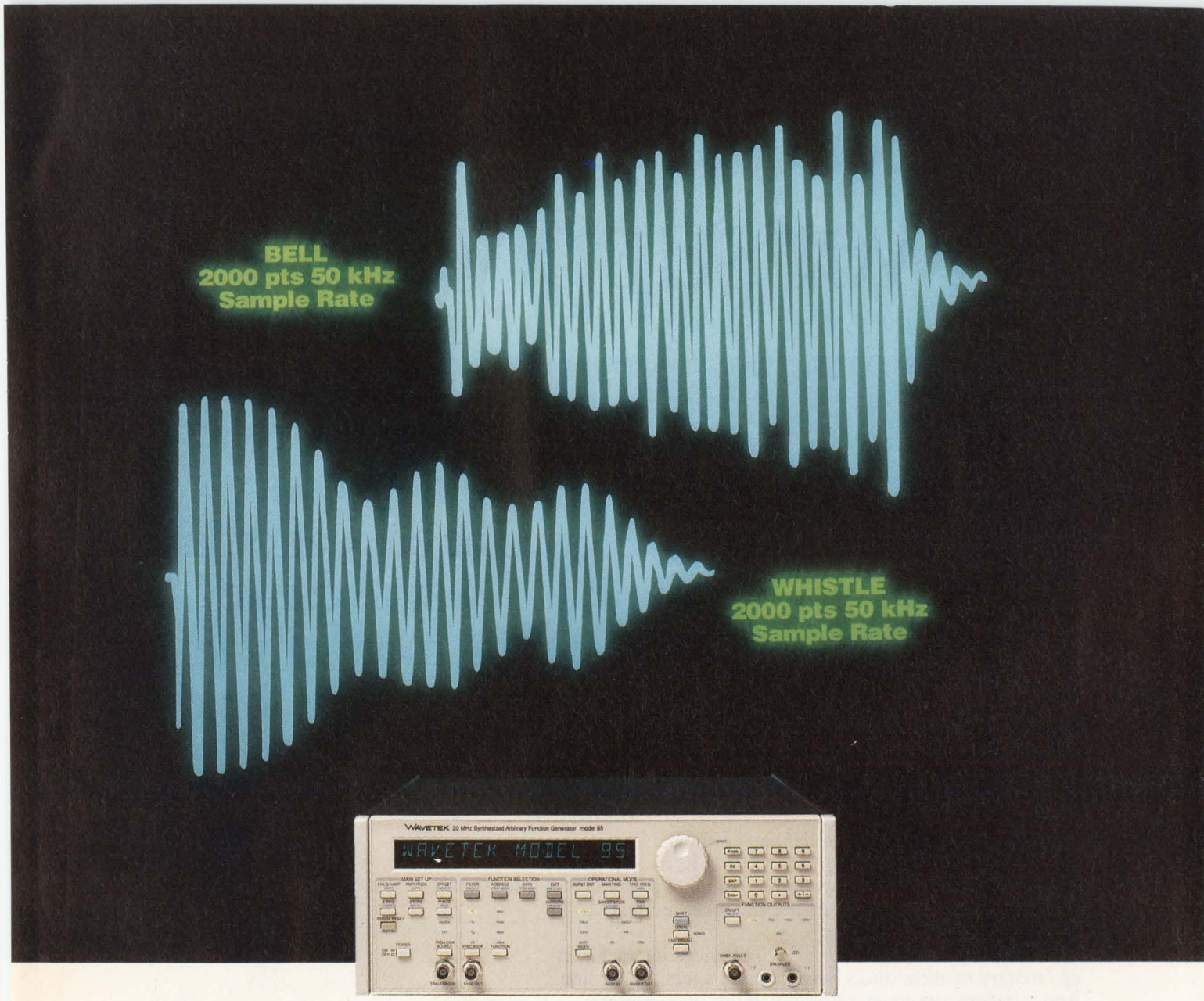

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EDN Magazine Edition

Volume 35, Number 20 October 1, 1990

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

On the cover: *Bridging the gap between Futurebus+ and other architectures is one way to get the new open-bus architecture to vendors. See the Special Report on pg 86. (Photo courtesy Force Computers Inc)*

SPECIAL REPORT

Futurebus+ 86

For some time now Futurebus+ touters have said that the architecture will lead us into the computing promised land. Though there is still work to be done, the journey may finally be ready to begin.—*John A Gallant, Associate Editor*

INNOVATION™ Driving Electronic Technology Into The Next Century

DESIGN FEATURES

Designers' guide to real-time Ada—Part 3 101

This article, the last in a series, describes the requirements that Ada runtime environments must meet and provides criteria for evaluating Ada vendors' runtime implementations.—*Benjamin M Brosgol, Alsys Inc*

Real-time programming—Part 2 115

Part 2 delves further into the nature of real-time programming. It addresses concerns that are unique to real time and describes how the programmer and the operating system handle these concerns.—*David L Ripps, Industrial Programming Inc*

TECHNOLOGY UPDATES

RISC hardware debug tools: Instruments spur RISC into the real-time race 43

RISC μPs' speed makes them candidates for the fastest embedded real-time systems. But designers may have to look to unfamiliar tools for debugging time-critical hardware/software interactions.—*Dan Strassberg, Associate Editor*

INNOVATION™ Driving Electronic Technology Into The Next Century

PC chip sets reduce chip count 57

IBM PC-compatible chip sets range from one to six chips and can give you caching facilities, a choice of buses, and power control.—*Chris Terry, Associate Editor*

Continued on page 7

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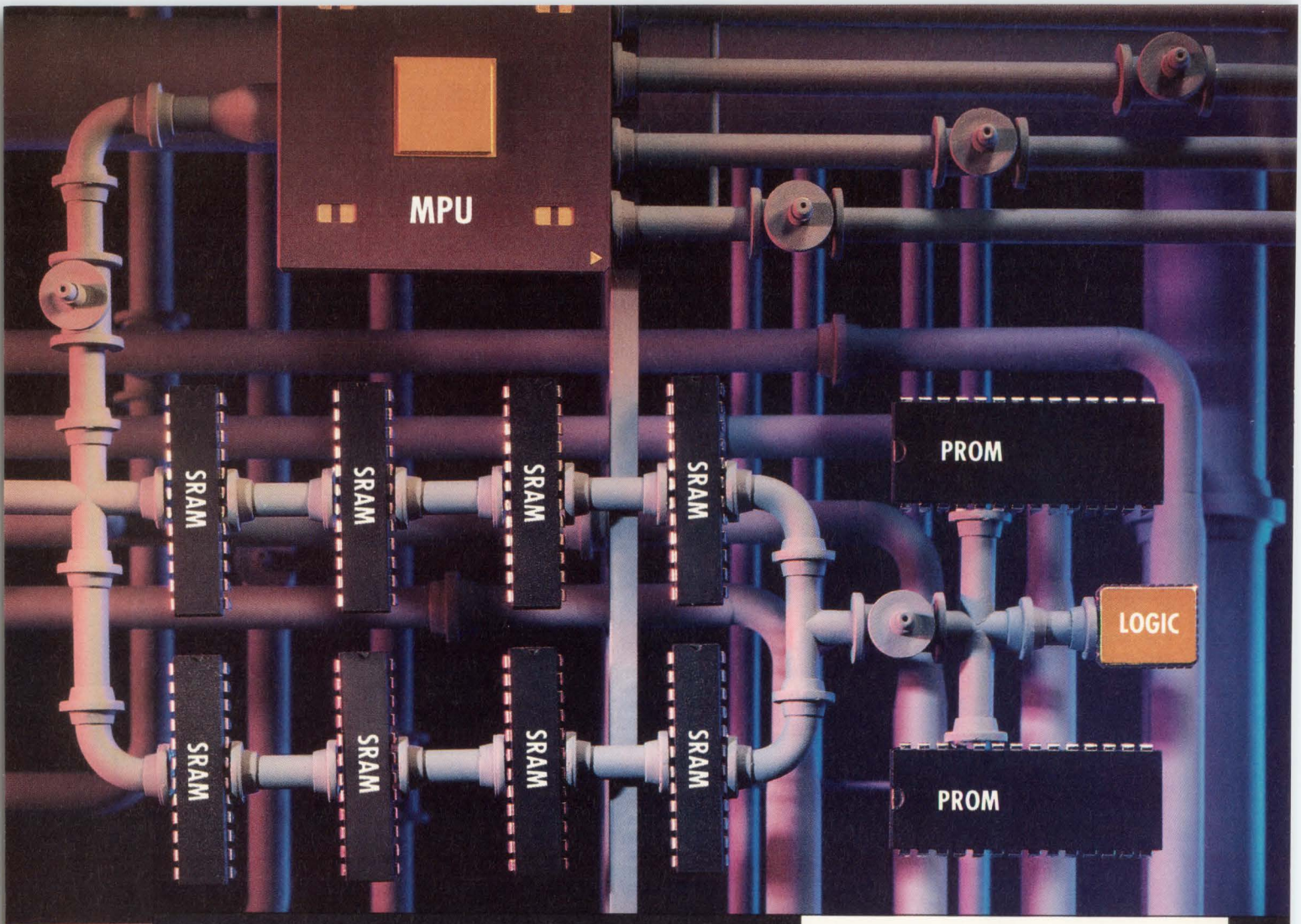

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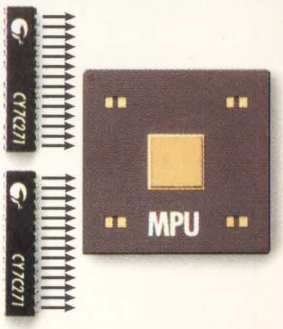

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250-MHz digital storage oscilloscope

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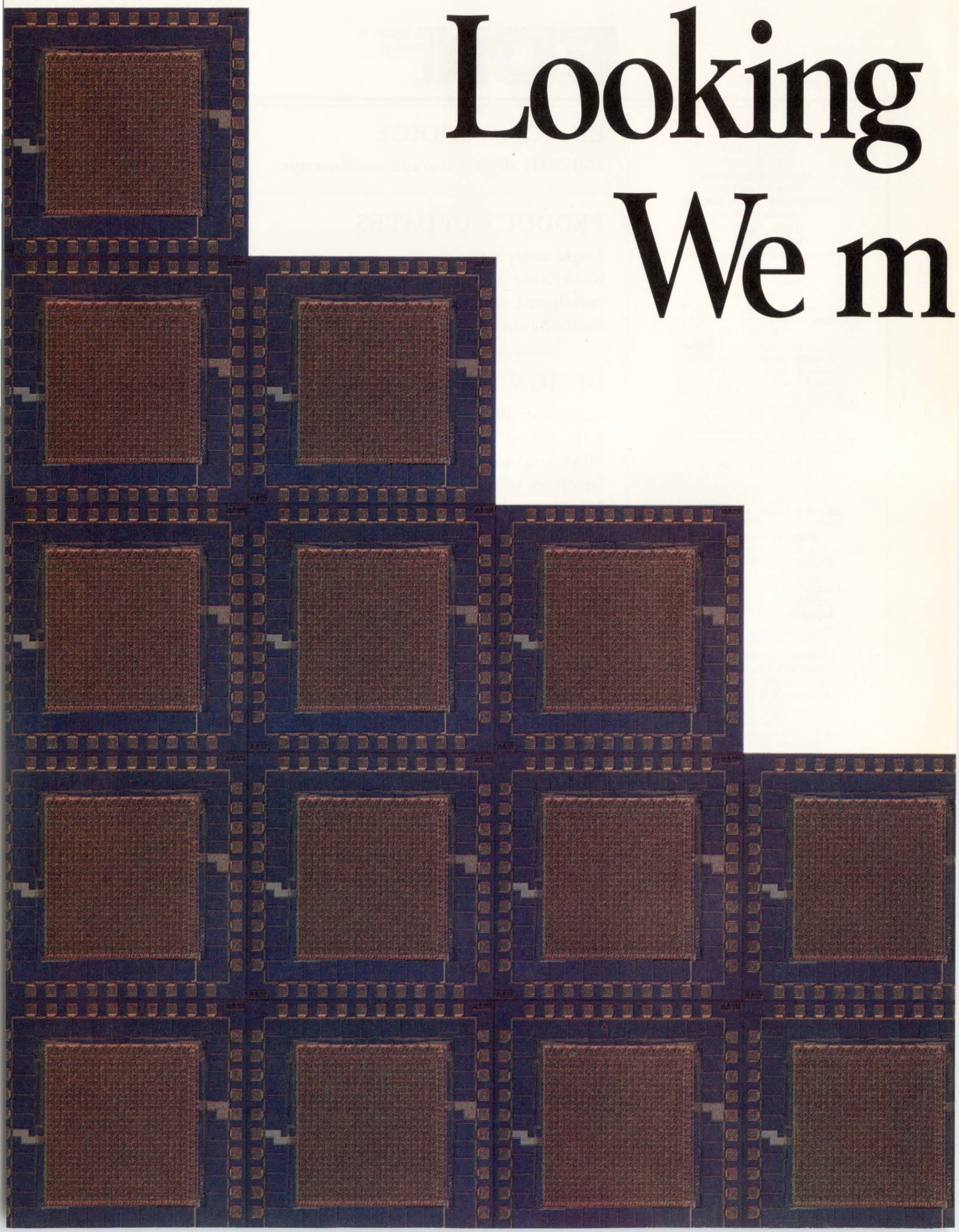

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Here's How To Develop Analog/Digital ASICs In Less Time, For Less Money.

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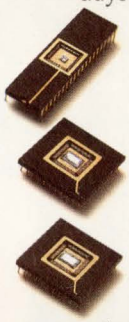

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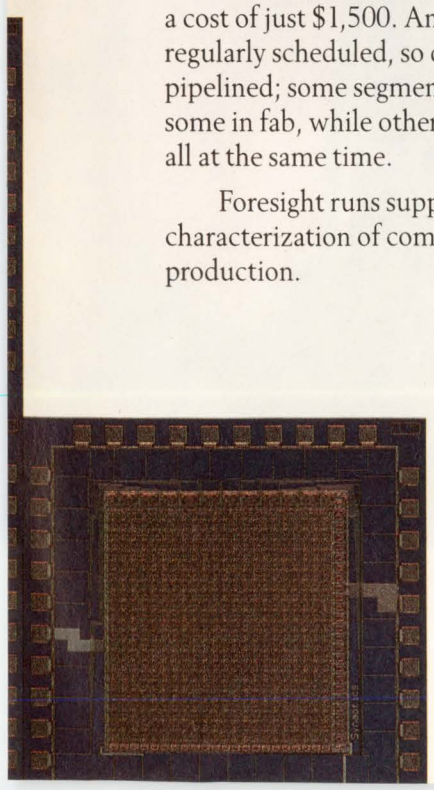

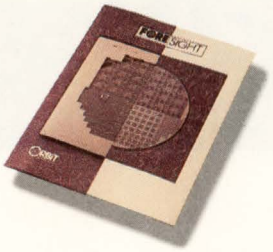

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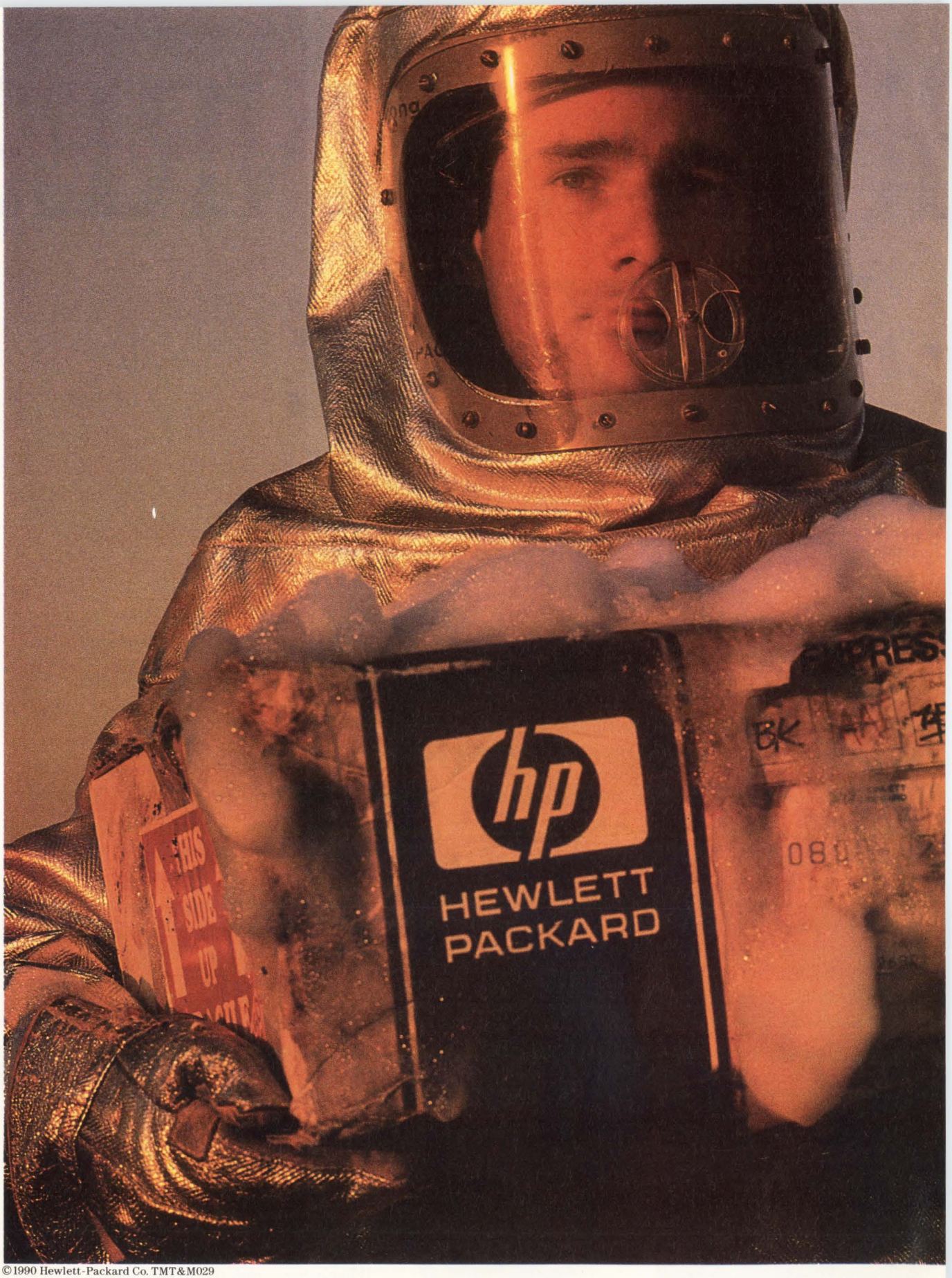
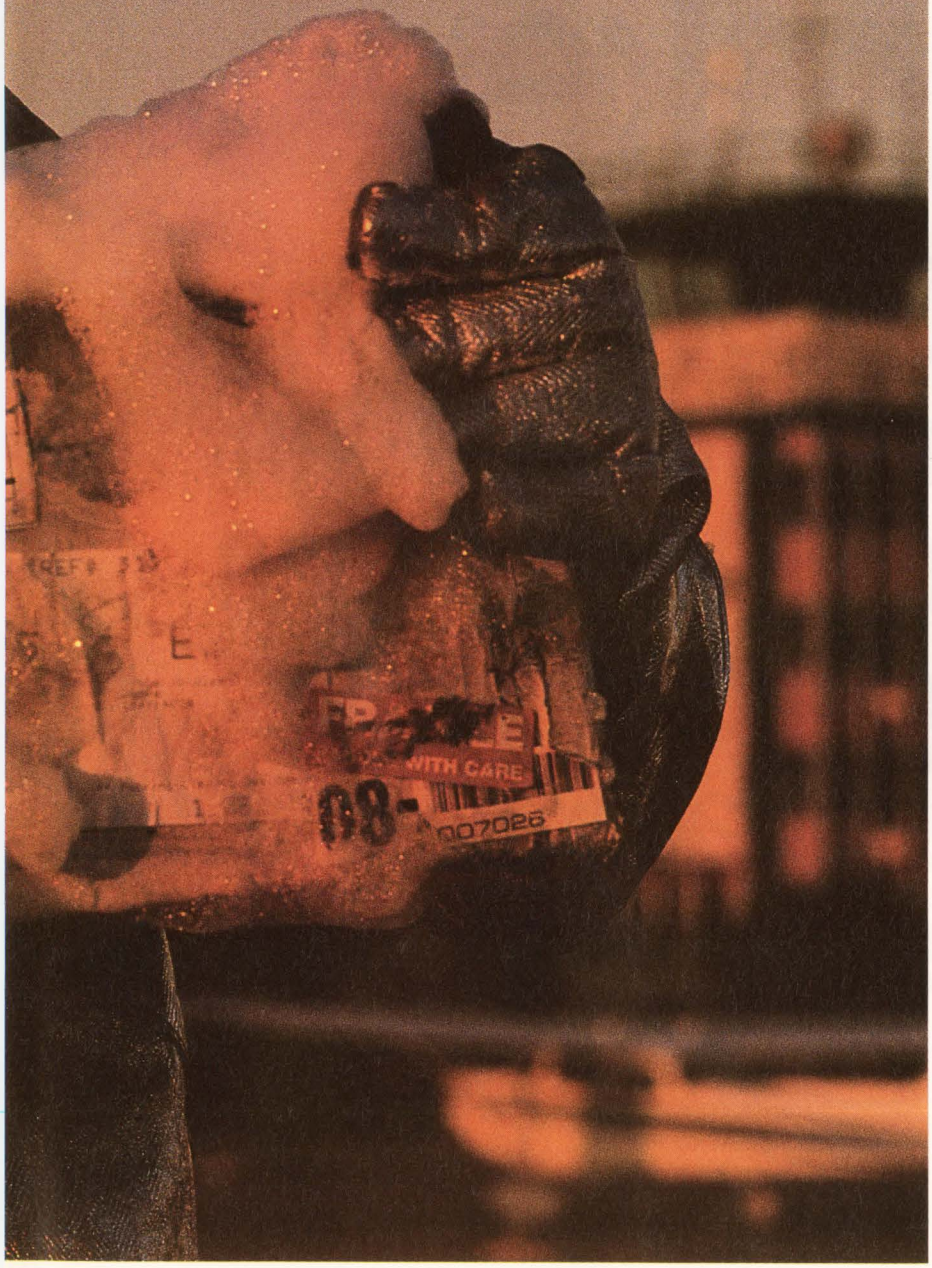


Did you hear about the optical attenuator that fell from the sky?



It hit the ground running.

"Roger, Falcon 20, you're cleared for landing. Braking action advisory. Ice on the runway." The veteran pilot of the cargo plane had landed at Link Field before, but the tower's report was a cold reminder that the airstrip ended in a 75-foot cliff.

On touchdown, the jet skidded out of control. Within seconds, it shot off the cliff like a ski jumper and tumbled down the steep embankment, cargo flying in all directions.

Minutes later, rescue teams were helping the pilot and co-pilot from the wreckage. The pungent smell of jet fuel filled the air, so crews sprayed fire-retardant foam on everything. Including an HP optical attenuator which was on its way to a customer.

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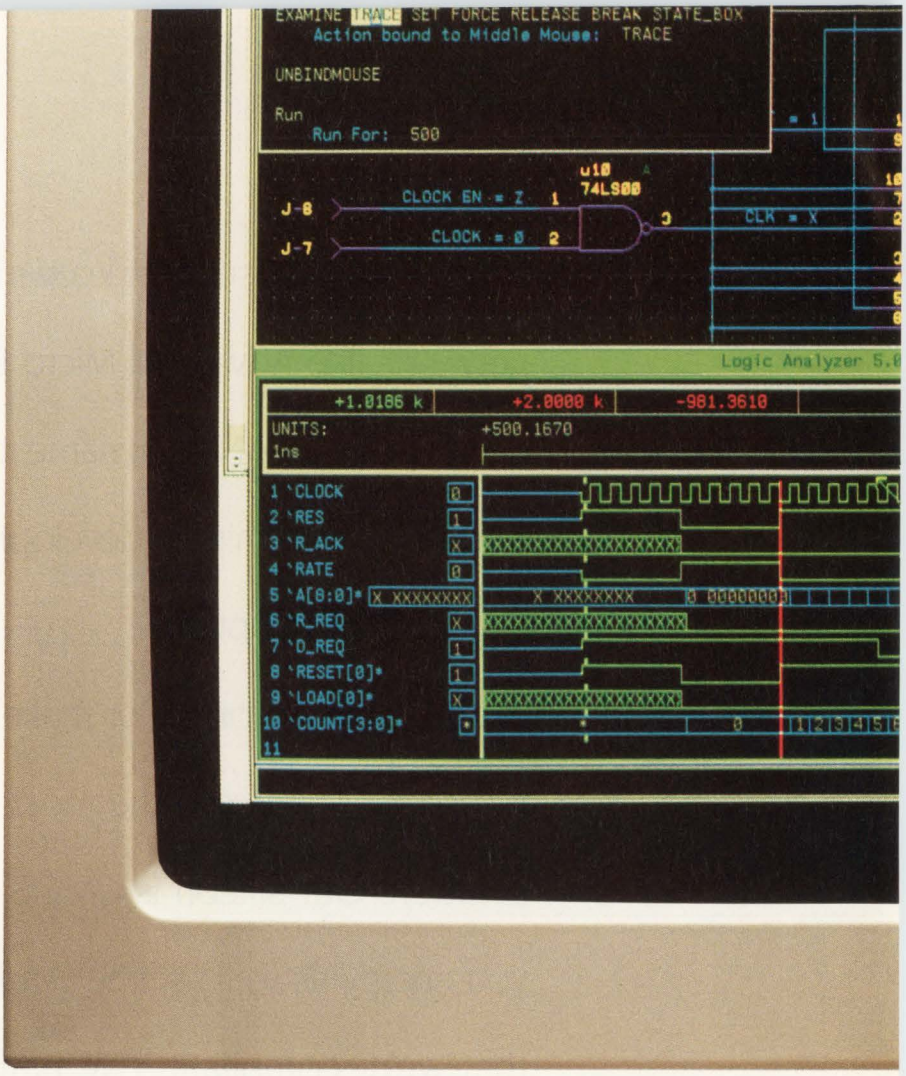
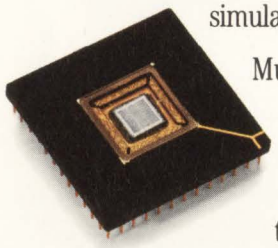


CAE for people to see how their

If your CAE tools are telling you too little too late, consider this news from Teradyne. Now you can capture and analyze complex ASIC and VLSI board designs with unprecedented accuracy and ease, using our Vanguard™ schematic entry software and LASAR simulator in Teradyne's MultiSim™ environment.



LASAR's accurate worst-case timing analysis means you won't be held up by faulty prototypes.

Here are CAE tools that work the way you like to work. They'll help you move quickly between schematic and simulation, and let you control simulation interactively. You'll get immediate feedback at every step.

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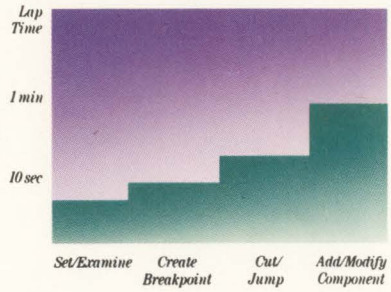
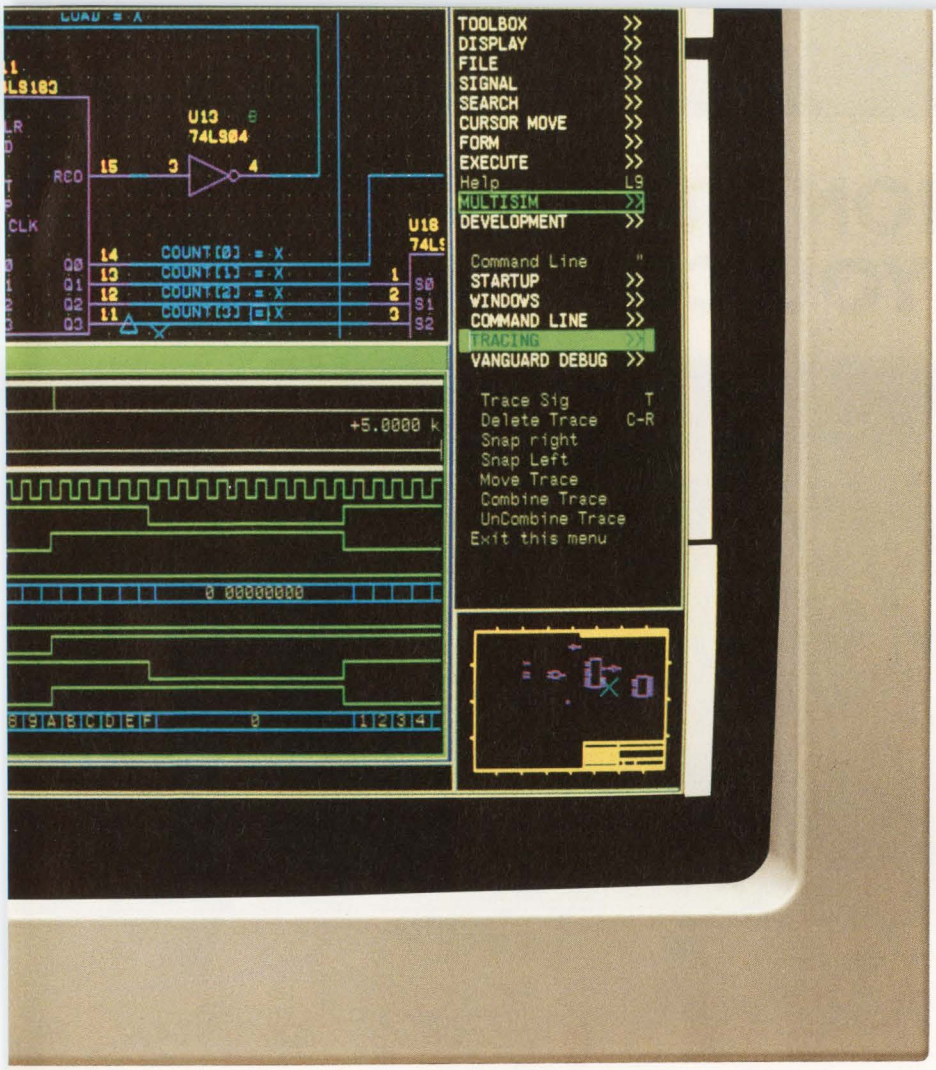
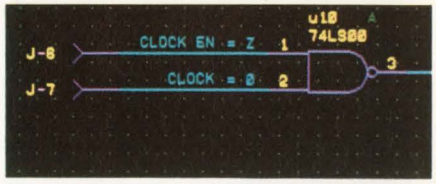


If you find a problem, fix it and see the results in seconds, because we eliminate compilation for most common design changes.

Best of all, with CAE tools from Teradyne you can be sure that what





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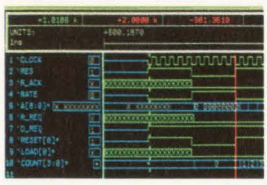
who can't wait designs work.

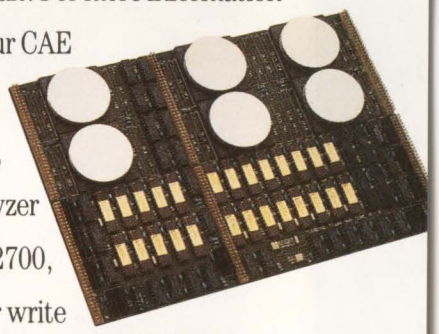
you see in design is what you'll get in manufacturing. How so? Because our LASAR system is more accurate than other event-based simulators. LASAR's worst-case algorithms precisely simulate the operation of gate arrays, high-speed micros and time-multiplexed buses, including the effects of process variations. You can zero-in on troublespots efficiently, and be confident that LASAR-verified designs will work—reliably and repeatably.



The same user interface and file format on PCs, Suns and VAXs simplifies training and communications when you're mixing platforms.

If you're in a hurry for results, you'll appreciate how easily Teradyne tools integrate into your current design process. EDIF, VHDL and commercial-tool interfaces let you build on existing databases. Then tie all your design and analysis tools running on PCs, Suns® or VAXs™ into one multiwindow design environment using Vanguard's graphical framework.

So don't wait. For more information about how our CAE tools can work for you, call Daryl Layzer at (617) 482-2700, ext. 2808. Or write Teradyne, 5155 Old Ironsides Drive, Santa Clara, CA 95054.



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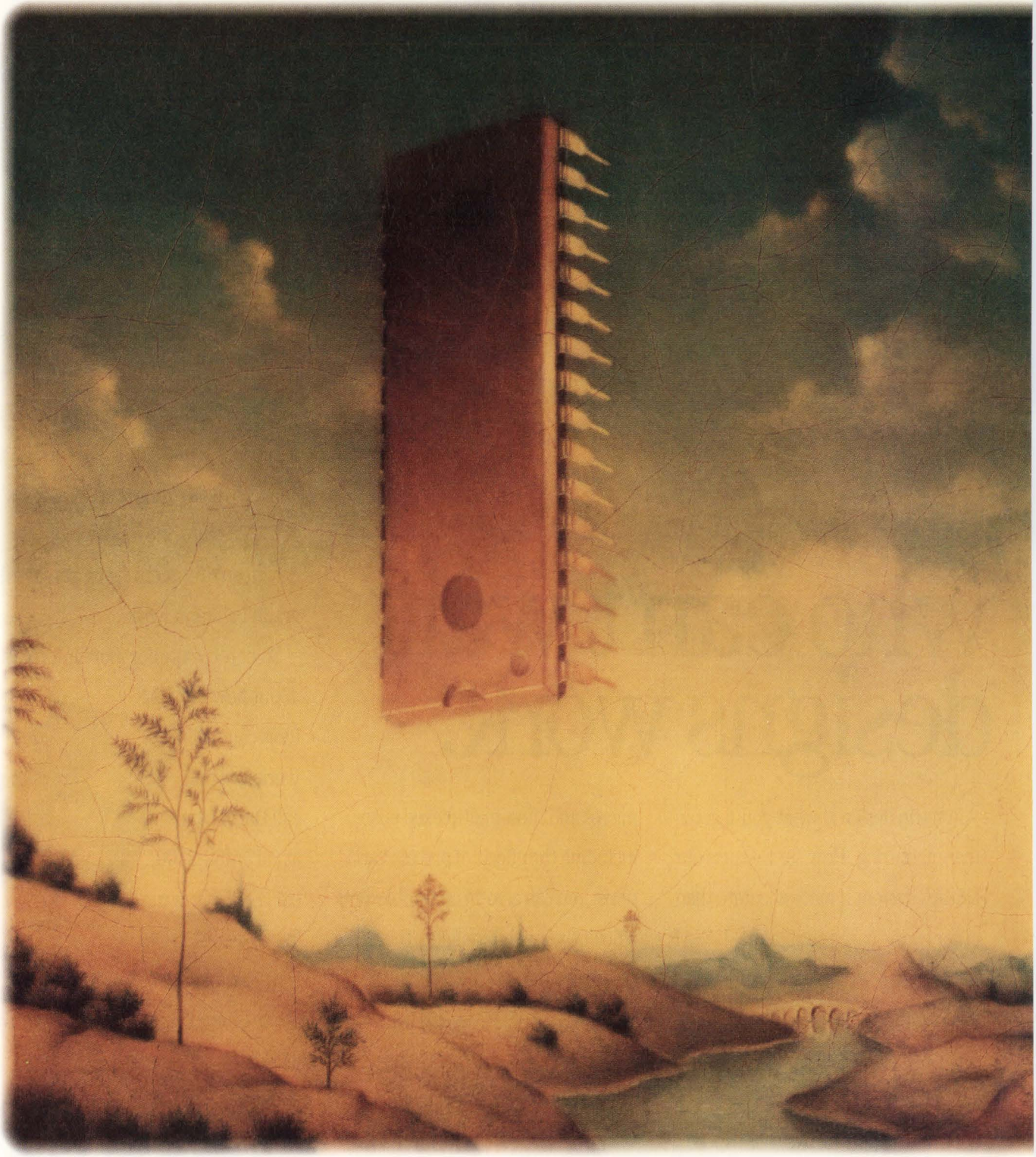

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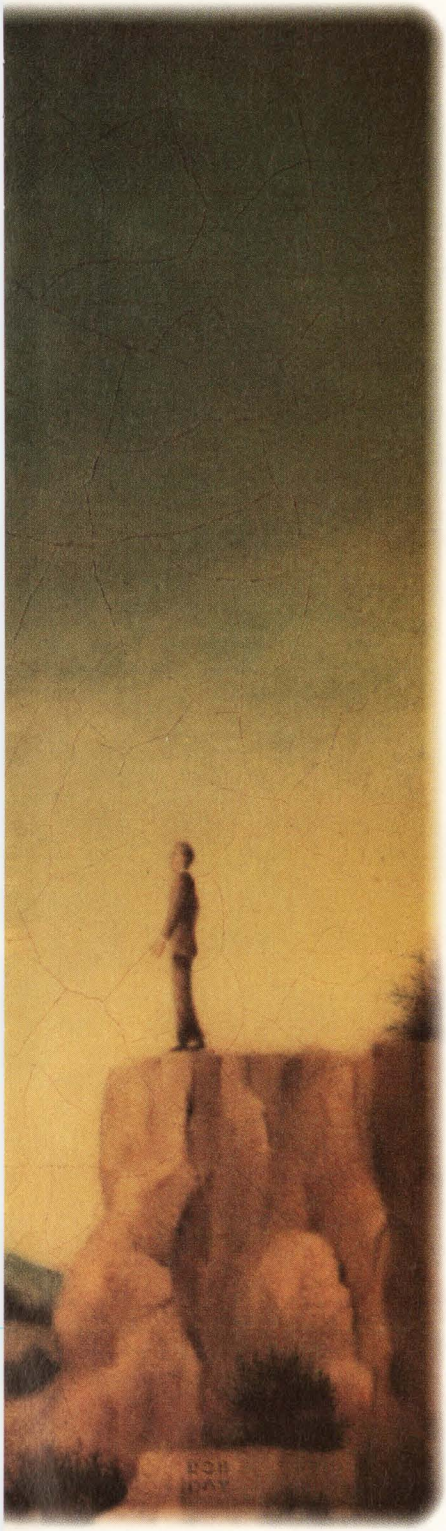

The recently introduced Samsung 1-meg SRAMs have a transistor count of 6.6 million.

In a day and age when makers of advanced microprocessors take understandable pride in the 1 million transistors on their chips, we think it's forgivable for us to be proud of the vastly greater number on these SRAMs.

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We offer the 1-meg slow SRAM in several speeds, several power ratings, and several package types. We're currently developing the part in the revolutionary TSOP packaging.

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CIRCLE NO. 41

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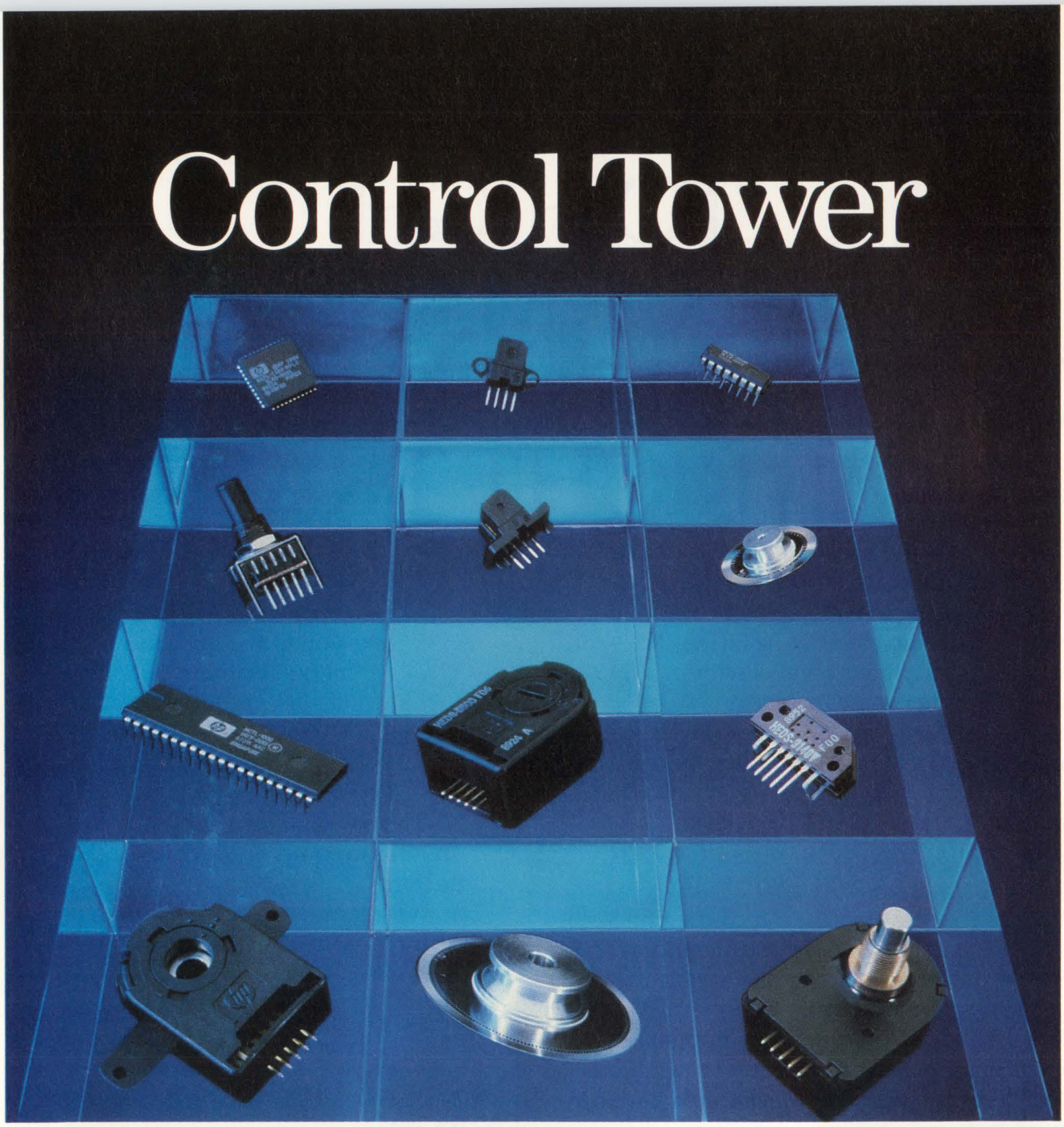

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CIRCLE NO. 42

NEWS BREAKS

EDITED BY SUSAN BUREAU

TRUE-COLOR DAC BOOSTS WINDOWING PERFORMANCE

Providing separate color maps to mix multiple graphics modes on a single display, the 170-MHz Bt463 TrueVu RAMDAC from Brooktree Corp (San Diego, CA, (619) 452-7580) lets you vary the pixel depth of each display window on a screen. The $317 (100) monolithic IC has a reconfigurable pixel port with all the logic necessary to manage arbitrary plane depths on a pixel-by-pixel basis. The device uses its multiplexed inputs to offer double and triple buffering for animation applications. You can vary the size of each color map from 16 to 512 addresses. To identify the individual characteristics of each window, a 4-bit word accompanying each set of pixel and overlay data specifies 24-plane true color, 8-bit pseudocolor, or 8-bit gray scale. Using this word to determine the conversion type, the IC converts every pixel from a virtual color-map index to a physical color-map index before sending the pixel to the chip's variable-sized look-up table.

The first 3-D graphics processing board to incorporate the Bt463 is the $8000 EG3-1280 from Matrox Electronic Systems (Dorval, Quebec, Canada, (514) 685-2630). This board plugs into EISA-bus computers and creates 1.3M transformed 3-D vectors/sec and 20,000 shaded polygons/sec in true color.—J D Mosley

INSTRUMENT PERFORMS 100-MHz STATE AND TIMING ANALYSIS

Tektronix (Portland, OR, (800) 245-2036) deplores using clock speed, channel count, and memory depth to sum up a logic analyzer's capabilities. The company claims that users who focus on just those specs inevitably wind up short-changing themselves. But width, depth, and speed are what the market is familiar with, and the Centurion 92A96, a card for Tektronix's DAS9200 logic-analysis system, can compete on those terms. The $17,950 board supports 100 channels (including four clock channels) and performs timing or state analysis at 100 MHz. Versions are available with 8k and 32k frames of memory. Fully synchronized operation of four cards yields the same specs on 288 channels—more than enough for the fastest RISC chip currently envisioned. Systems with 1536 channels are workable. Multiplexed operation supports 400-MHz timing analysis on 24 channels/card. You can switch between state and timing analysis without repositioning probes. The system will simultaneously display timing diagrams and disassembled code.—Dan Strassberg

CREATE UNIQUE GUIs FOR PC-BASED VIRTUAL INSTRUMENTS

Using the Virtual Instrument Developer Toolkit from National Instruments (Austin, TX, (512) 794-0100), you can customize a graphical user interface (GUI) for PC-based instruments that have no front panel of their own, such as VXIbus devices and remotely controlled IEEE-488-bus or RS-232C instruments. It lets a computer screen imitate the look-and-feel of physical instrument panels; it also lets you control the instruments from DOS. This $995 kit is an extension of the C programming language, using objects and verbs to create and define your GUI in an object-oriented format. It includes an instrument panel library, an object-definition compiler, and a library of images and fonts. Compatible with the manufacturer's existing LabWindows libraries, the toolkit lets you use digital readouts, waveforms, and simulated LEDs to display data. In addition, you can create a GUI that customizes one or more instruments for a particular application. For example, your GUI could perform like a spectrum analyzer by combining the capabilities of a function generator, a universal counter, and a digital multimeter.—J D Mosley

NEWS BREAKS

PROCESSOR INCLUDES CPU AND IBM PC/AT SUPPORT CIRCUITRY

Mother-board chip-set vendors have hinted at integrating an Intel-compatible CPU into a chip set. Now μP vendor AMD (Austin, TX, (512) 385-8542) has implemented a typical AT-compatible mother board on one chip. The Am286ZX/LX IC includes a 12- or 16-MHz 80286, dynamic-RAM control logic, two interrupt controllers, three counter/timers, a real-time clock with CMOS RAM, a bus controller, and EMS 4.0 (expanded memory specification) support circuitry. You need add only BIOS ROMs, dynamic RAM, a keyboard controller, and (optionally) a math coprocessor to have a complete mother board. The 12- and 16-MHz Am286ZX chips cost $69 and $85.50 (1000), respectively. The Am286LX ICs, which add power-saving features for laptop computer applications, cost $76.50 (12 MHz) and $89 (1000) (16 MHz).—Maury Wright

32-BIT μP TARGETS EMBEDDED SYSTEMS

The E1, a 25-MHz μP from Hyperstone (Konstanz, Germany, (7531) 67789), has separate 32-bit data and address buses and 18 global and 64 local registers. You can reconfigure the registers to a stack of variable frame length from 2 to 16. The majority of instructions are single cycle and operate on 16-bit data. Multiply and divide instructions require multiple cycles. Used with dynamic RAMs having a 40-nsec page-mode cycle time, the μP can achieve a 25-MIPS burst rate without external memory caches. Benchmarks yield 38,000 Dhrystones. The throughput results from a combination of pipelined load instructions, an internal 2-stage decode/execute pipeline, and a look-ahead instruction cache. Software tools include a cross-assembler and a debugger that run under MS-DOS; an emulator links to your PC through an RS-232C port. The E1 costs $150 (1000).—Brian Kerridge

VME, IBM PC BOARDS EMULATE NTDS HOST AND PERIPHERALS

Two NTDS (Navy Tactical Data Systems) interface boards allow you to emulate expensive host computers and peripherals with personal computers and workstations. The Hawke (VMEbus) and Eagle II (IBM PC/AT bus) from Sabtech Industries (Anaheim, CA, (714) 970-5311) suit applications in hardware and software development, test, debug, and maintenance of NTDS products. Separate versions comply with Types A, B, and C NTDS communications standards specified in MIL-STD-1397B. The boards come with software for interactive emulation and for interfacing with high-level languages such as C. The IBM PC-compatible boards cost $4000 to $4500; the VMEbus offerings sell for $5000.—Maury Wright

SIMULATOR GOES TO THE SOURCE OF THE PROBLEM

The 90.1 release of the Silos II simulator from Simucad (Union City, CA, (415) 487-9700) provides two enhancements to help you find sources of design errors. The first is what the company calls a 2-D, interactive-debug feature. When you discover a node transition to an incorrect state, you can interactively trace the transition backward in time to see which device input caused the transition. You can continue to trace backward, both in time and in signal path, until you find the initial cause of the problem. The second Silos II enhancement lets you observe short-duration spikes and the events they cause. Short-duration spikes can occur when two or more edge transitions happen at nearly the same time. When these spikes are shorter than the propagation delay of a device being simulated, some simulators fail to show their effect on the device's output. The new release is free to Silos II users with a current maintenance agreement. Silos II ranges from $5000 for personal-computer versions to $80,000 for mainframe versions.—Doug Conner

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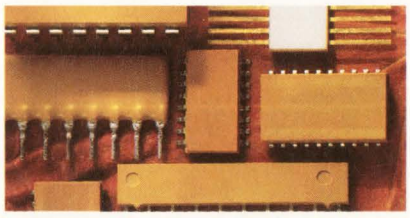

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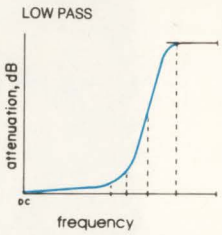

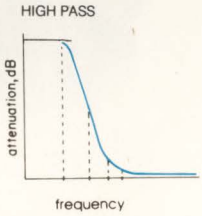

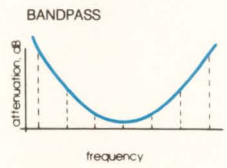

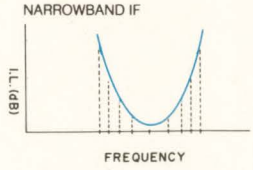

low pass dc to 1200MHz

MODEL NO.	PASSBAND, MHz (loss <1dB) Min.	fco, MHz (loss 3db) Nom.	STOP BAND, MHz (loss>20dB) Max.	(loss>40dB) Max.	(loss>40dB) Min.	VSWR pass-band typ.	VSWR stop-band typ.	PRICE $ Qty. (1-9)
PLP-10.7	DC-11	14	19	24	200	1.7	18	11.45
PLP-21.4	DC-22	24.5	32	41	200	1.7	18	11.45
PLP-30	DC-32	35	47	61	200	1.7	18	11.45
PLP-50	DC-48	55	70	90	200	1.7	18	11.45
PLP-70	DC-60	67	90	117	300	1.7	18	11.45
PLP-100	DC-98	108	146	189	400	1.7	18	11.45
PLP-150	DC-140	155	210	300	600	1.7	18	11.45
PLP-200	DC-190	210	290	390	800	1.7	18	11.45
PLP-250	DC-225	250	320	400	1200	1.7	18	11.45
PLP-300	DC-270	297	410	550	1200	1.7	18	11.45
PLP-450	DC-400	440	580	750	1800	1.7	18	11.45
PLP-550	DC-520	570	750	920	2000	1.7	18	11.45
PLP-600	DC-580	640	840	1120	2000	1.7	18	11.45
PLP-750	DC-700	770	1000	1300	2000	1.7	18	11.45
PLP-800	DC-720	800	1080	1400	2000	1.7	18	11.45
PLP-850	DC-780	850	1100	1400	2000	1.7	18	11.45
PLP-1000	DC-900	990	1340	1750	2000	1.7	18	11.45
PLP-1200	DC-1000	1200	1620	2100	2500	1.7	18	11.45

high pass dc to 2500MHz

MODEL NO.	PASSBAND, MHz (loss <1dB) Min.	fco, MHz (loss 3db) Min.	Nom.	STOP BAND, MHz (loss>20dB) Min.	(loss>40dB) Min.	VSWR pass-band typ.	VSWR stop-band typ.	PRICE $ Qty. (1-9)
PHP-50	41	200	37	26	20	1.5	17	14.95
PHP-100	90	400	82	55	40	1.5	17	14.95
PHP-150	133	600	120	95	70	1.8	17	14.95
PHP-175	160	800	140	105	70	1.5	17	14.95
PHP-200	185	800	164	116	90	1.6	17	14.95
PHP-250	225	1200	205	150	100	1.3	17	14.95
PHP-300	290	1200	245	190	145	1.7	17	14.95
PHP-400	395	1600	360	290	210	1.7	17	14.95
PHP-500	500	1600	454	365	280	1.9	17	14.95
PHP-600	600	1600	545	440	350	2.0	17	14.95
PHP-700	700	1800	640	520	400	1.6	17	14.95
PHP-800	780	2000	710	570	445	2.1	17	14.95
PHP-900	910	2100	820	660	520	1.8	17	14.95
PHP-1000	1000	2200	900	720	550	1.9	17	14.95

bandpass 20 to 70MHz

MODEL NO.	CENTER FREQ. MHz F0	PASS BAND, MHz (loss <1dB) Max. F1	Min. F2	STOP BAND, MHz (loss > 10 dB) Min. F3	Max. F4	(loss > 20 dB) Min. F5	Max. F6	VSWR 1.3:1 typ. total band MHz	PRICE $ Qty. (1-9)
PIF-21.4	21.4	18	25	4.9	85	1.3	150	DC-220	14.95
PIF-30	30	25	35	7	120	1.9	210	DC-330	14.95
PIF-40	42	35	49	10	168	2.6	300	DC-400	14.95
PIF-50	50	41	58	11.5	200	3.1	350	DC-440	14.95
PIF-60	60	50	70	14	240	3.8	400	DC-500	14.95
PIF-70	70	58	82	16	280	4.4	490	DC-550	14.95

narrowband IF

MODEL NO.	CENTER FREQ. MHz F0	PASS BAND, MHz I.L. 1.5dB max. F1-F2	STOP BAND, MHz I.L. > 20dB F5	F6	STOP BAND, MHz I.L. > 35dB F7	F8-F9	PASS-BAND VSWR Max.	PRICE $ Qty. (1-9)
PBP-10.7	10.7	9.5-11.5	7.5	15	0.6	50-1000	1.7	18.95
PBP-21.4	21.4	19.2-23.6	15.5	29	3.0	80-1000	1.7	18.95
PBP-30	30.0	27.0-33.0	22	40	3.2	99-1000	1.7	18.95
PBP-60	60.0	55.0-67.0	44	79	4.6	190-1000	1.7	18.95
PBP-70	70.0	63.0-77.0	51	94	6	193-1000	1.7	18.95

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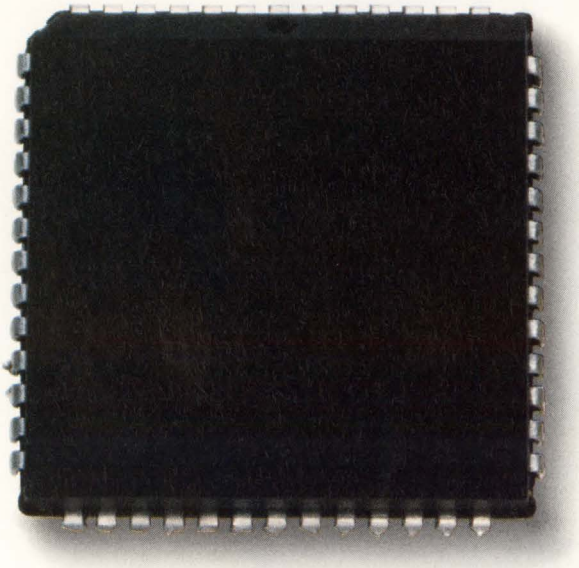

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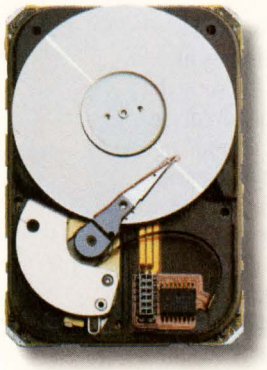

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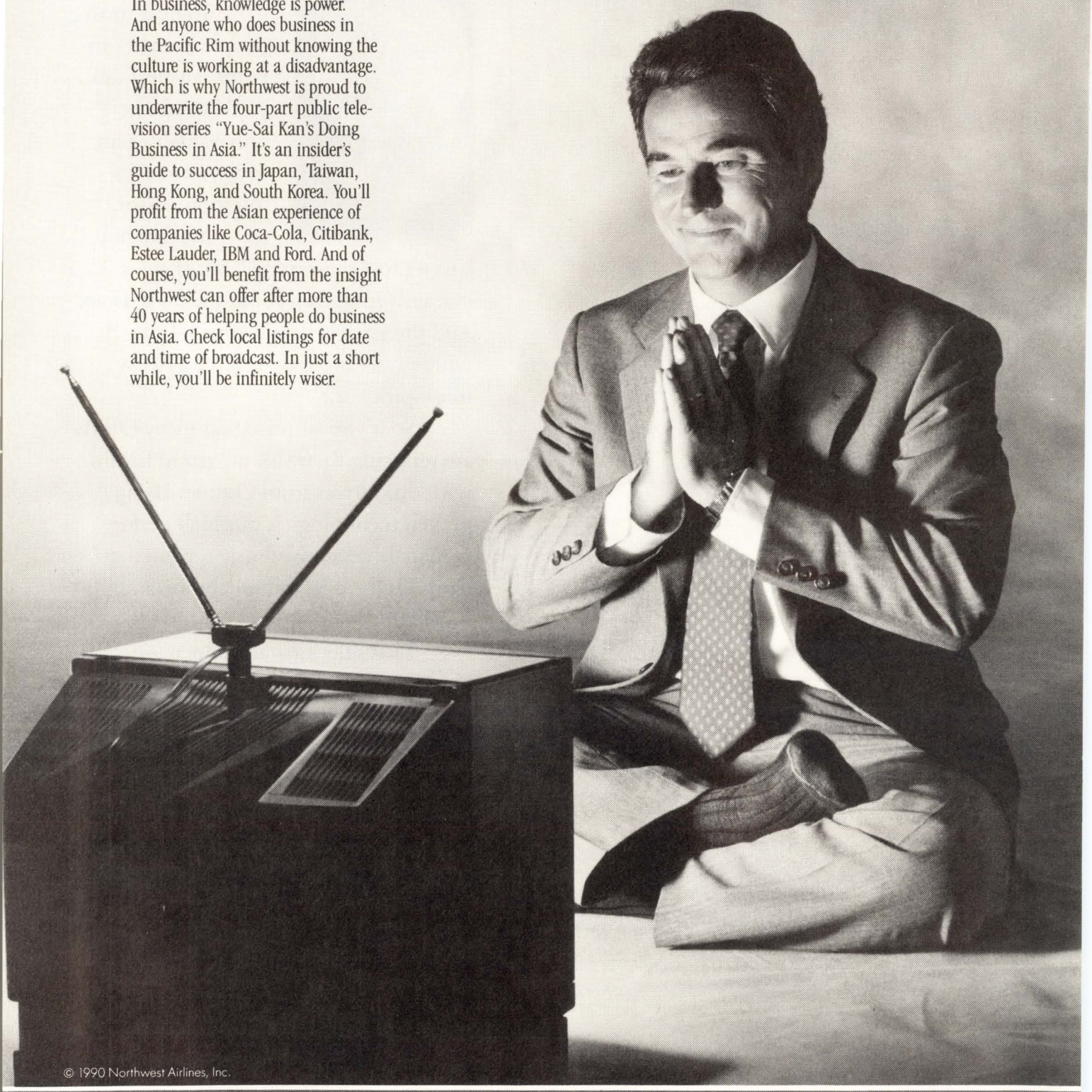

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SIGNALS & NOISE

Reader has minor quibble

The article by J D Mosley, "Mini disk drives strive for acceptance" (EDN, May 24, 1990, pg 95), is a very good overview of the new miniature disk drives. I have a very minor quibble, however, about the way the article compares power consumption between the 2-in. floppy-disk drive used in the Zenith MinisPort and the standard 3½-in. drive. On pg 97, J D states that "A comparable 3½-in. drive consumes 150% more power than the 2-in. drive . . . " That makes sense, and the numbers that follow confirm my understanding of just what "150% more" means.

The photo caption on pg 98, however, tries to reverse the formula, which doesn't work. What does " . . . consumes 150% less power than a comparable 3½-in. drive" mean? Negative power consumption?

Brooks Lyman, Designer
JRTD Inc
Concord, MA

(Ed Note: Sorry, I goofed.)

Violating laws of immigration and morality

In his letter (EDN, May 24, 1990, pg 39), William Geary seems to have missed the point of my response in support of Jon Titus's editorial, "Send alien graduates home" (EDN, October 27, 1988, pg 57).

If Bill wishes to label patriotism, moral fealty, and a responsibility to return at least what one takes as "thuggery," then so be it; this is (still) a free country. He attempts to make a political battleground where none exists. The issue in question is a moral one.

If a third-world country exports all of its talent, it will forever remain a third-world country, dependent on the rest of the world for its very existence. Compare this concept with Bill's references to freedom and human dignity. When a citizen of that country signs an agreement to acquire a skill elsewhere and return (presumably to the benefit of said country) but instead decides to "take the money and run," that individual is violating not only the immigration and emigration laws of both lands, but is also prostituting his/her moral obligation.

It is indeed a privilege to live in the US, a privilege many people gave their lives to secure and maintain. We have an overabundance of technologists. Third-world countries, on the other hand, need all the help they can get.

We are also a country of laws. These laws very liberally govern the flow of immigration into the US. These are the same laws that the "selfish opportunists," as Bill refers to Tesla, Einstein, et al, obeyed when they entered the US. They didn't come here under the guise of a temporary student visa. Nor were their native countries technologically depressed; quite the contrary. These people fled oppression. I did not attempt to make this point in my letter.

N Silber
ITT Aerospace Communications
Nutley, NJ

IT'S EASY TO HAVE YOUR SAY

EDN's Signals & Noise column provides a forum for readers to express their opinions on issues raised in the magazine's articles or on any topic that affects the engineering industry. You can use one of several easy ways to reach us. First, there's always the mail. Send your letters to Signals & Noise Editor, EDN Magazine, 275 Washington St, Newton, MA 02158. Or, send us a message via MCI mail at EDNBOS. Finally, EDN's bulletin-board system is ready for use—and it's free (except for the phone call). You can reach us at (617) 558-4241 and leave a letter in the EDITORS Special Interest Group. You'll need a 1200-bps modem and a communications program that is set for eight data bits, no parity, and one stop bit, or 1200, 8N1 in shorthand.

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CXK581100YM*	128K x 8	100/120	TSOP (reverse)	L, LL
CXK581001P	128K x 8	70/85	DIP 600 mil	L
CXK581001M	128K x 8	70/85	SOP 525 mil	L
CXK581020SP	128K x 8	35/45/55	SDIP 400 mil	
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ASK EDN

EDITED BY JULIE ANNE SCHOFIELD

Have you been stumped by a design problem so long that you don't know who to turn to? Are you having trouble locating parts? Finding companies? Can't interpret a spec sheet? Ask EDN.

This department will serve as a forum to solve nagging problems and answer difficult questions. EDN's editors will provide the solutions. If we can't solve a problem, we'll find an expert who can, or we'll print your letter and ask your peers for help. We can't answer every question, but we'll try to publish the ones that will help you most in your job.

Address your letters to Ask EDN, 275 Washington St, Newton, MA 02158. FAX (617) 558-4470; MCI: EDNBOS. Or, send us a letter on EDN's bulletin-board system. You can reach us at (617) 558-4241 and leave a letter in the /ask_edn Special Interest Group. You'll need a 1200-bps modem and a communications program that is set for eight data bits, no parity, and one stop bit, or 1200, 8N1 in shorthand. Turn to the Feedback and Amplification section of this issue's Design Ideas to learn how to use the bulletin-board system.

Reader seeks macro assembler

Where can I find a macro assembler for the 6805 μP family that runs on an Apple Macintosh? Thanks.
Antoine Elinik
Apelem
Nimes, France

Associate Editor Mike Markowitz took this question on and found a company that sells such a part for $149.95:

Microdialects
Box 30014
Cincinnati, OH 45230
(513) 271-9100.

Help the Navy

I recall that sometime in the last year, a company announced an IRIG-B (Inter-Range Instrumentation Group format B) time-code receiver completely contained on a single chip. (An IRIG-B converter receives a 1V p-p analog or RF signal and converts it to time of day in digital format based on Greenwich mean time.) I now have an application that requires such an IC and can't locate a source. Please help in any way you can.
David Fors
Electronics Engineer
Naval Weapons Center
China Lake, CA

Associate Editor John Gallant posed this question to three engineers who work for companies that produce time-code readers. They said that they had heard rumors that such a device existed but didn't know what company made it. If you do, please let us know.

Elusive software found

In the August 2, 1990, issue of EDN, a reader—Jon Sanserino—asked if anyone could help him locate a piece of software called Partlister. I have a copy of that software that I would be willing to let go for $25, including shipping costs and all documentation. I obtained that software to do part listings, but before I could even finish reading the documentation, my company went on another system. My software has sat on a shelf since that time.
James V Joyce
Bendix Avionics Div
Fort Lauderdale, FL

A need for RF transceiver

I need sources for RF transmitter/receiver building blocks and/or modules. The devices will be used for digital data transfer over 100 ft under the control of Motorola's 146805E2 microcontroller.
Joe Thomas
Weber Costello
Troy, MO

If any reader knows of such source, please drop Ask EDN a line.

EDN

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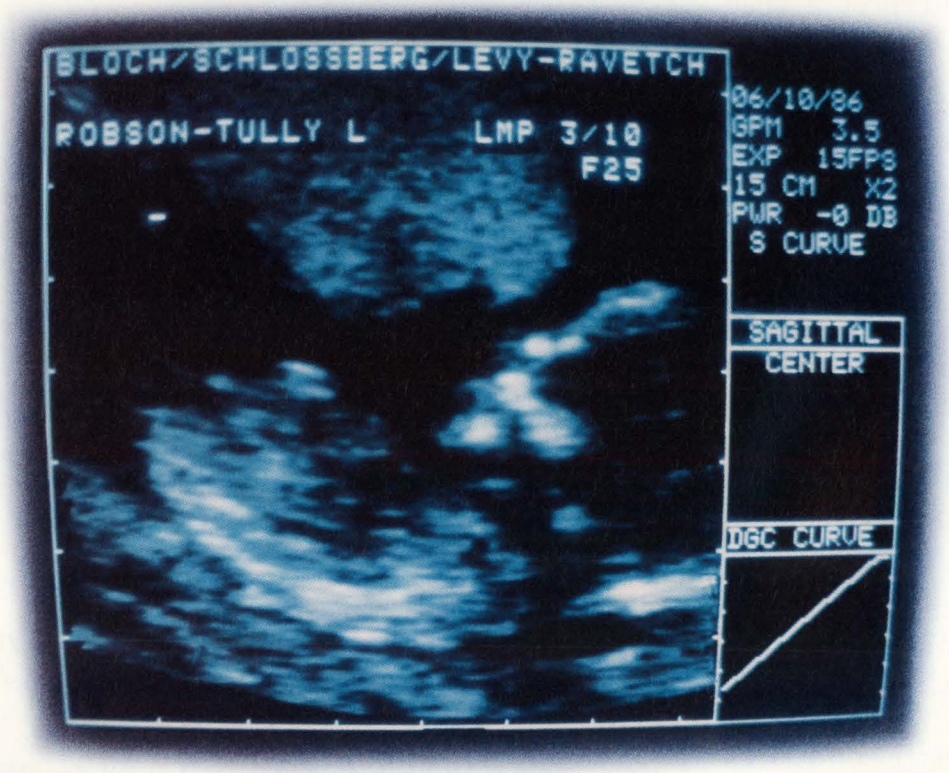

If you've been laboring under the assumption that Video RAMs have gotten about as fast as possible, Toshiba would like to introduce you to their new 1 Megabit creations.

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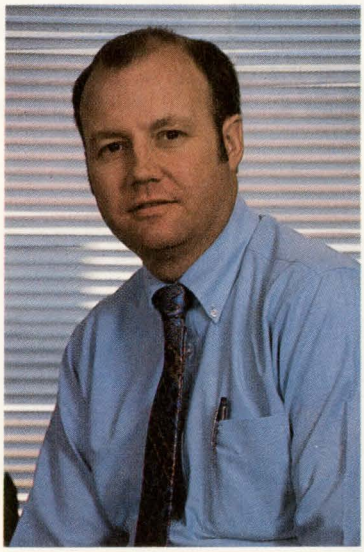
EDITORIAL

A BBS for readers only



EDN now offers a computer bulletin-board system (BBS) that lets you communicate with your fellow engineers and with EDN's technical editors. Access to EDN's BBS is free, except that you pay for the telephone call. You can reach the BBS at (617) 558-4241. You'll need a 1200-bps modem and a communication program that is set for 8 data bits, no parity, and 1 stop bit, or 1200, 8N1 in shorthand. The BBS offers many services, but we think you'll be most interested in the Special Interest Groups, or SIGs, that we have set up. In fact, the purpose of the SIGs is to enhance 2-way communication.

You'll find a SIG dedicated to our popular Design Ideas section. The DI_SIG provides a way to download complete software listings, executable code, pc-board layout files, and simulation data when contributors supply them. You'll also have the opportunity to read through other engineers' suggestions, circuit improvements, and modifications. We'll assign each Design Idea its own identification code, so you'll be able to scan through the DI_SIG bulletins and find what you want. If you make a modification that enhances a circuit or if you produce a software listing, your addition to the Design Idea bulletins helps all other DI_SIG users. Each SIG also lets you respond to bulletins and leave messages for the SIG's operator.

Some of the bulletins may have attached files of information or program code that don't fit in a short bulletin. The BBS lets you download such attachments so you can read, run, test, or examine them on your own computer. When you download files, you can select either ASCII, XMODEM, XMODEM-CRC, or YMODEM-CRC protocols. The ASCII selection lets you look at text files one screen at a time or transfer an entire ASCII file to your computer. (To do the latter, type 1C at the transfer prompt to select the continuous-transfer mode.) When you leave a DI_SIG bulletin, you can also leave an attachment file for our SIG operators to approve and add to the DI_SIG for other readers to access.

There are other SIGs worth scanning. The FREEWARE SIG contains utility, scientific, and engineering shareware programs and information. The EDITORS SIG lets you leave messages for EDN's editorial staff. If you have a technical question, you can also leave a message on the ASK_EDN SIG. In addition, when long software or other listings accompany feature articles, we'll tell you how to find them on the BBS. And, if you'd like to have a SIG set up just for microprocessors, digital signal processing (DSP), analog design, or another topic, let us know.

After you sign up, don't forget to register yourself in the BBS Registry, which is open—except for your password—to other users. The Registry can help you find a specific person, and it can help other users find you. Once you're logged into the BBS, you can see what's happening in the Information Center, the Classified Ads, and the Polls and Questionnaires. The EDN BBS also provides EMAIL for communications between users. Sorry, no quizzes or games; this is a professional bulletin board, of, by, and for engineers. The editors own it—the editors run it. As such, we won't share your name with advertisers and we'll keep the BBS free of promotional materials.

If you'd like a short instruction manual, please **Circle No. 801** on the bingo card and I'll send you a copy. We're also open to suggestions for improving and expanding the BBS. Enjoy.

Jon Titus
Editor

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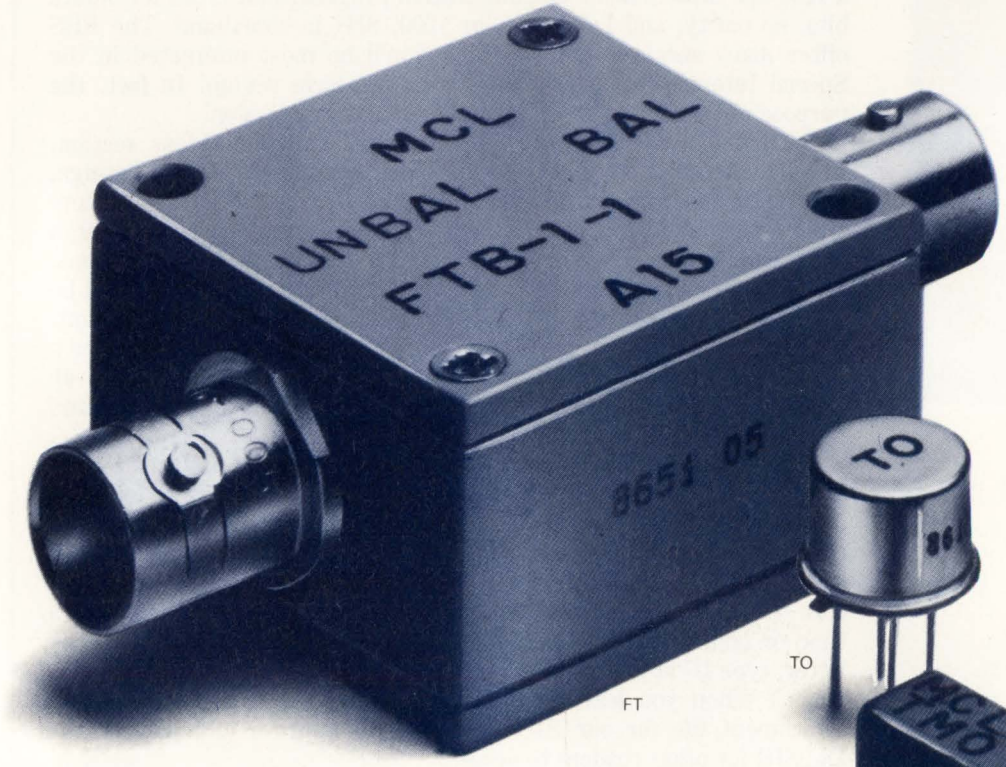

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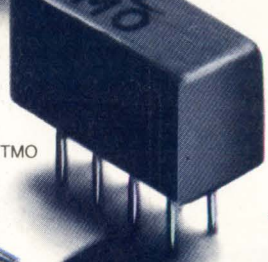

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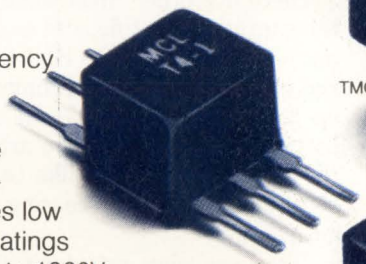

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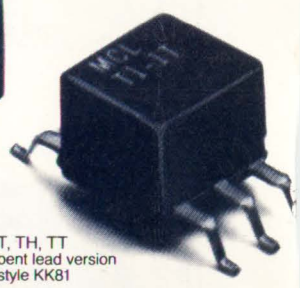
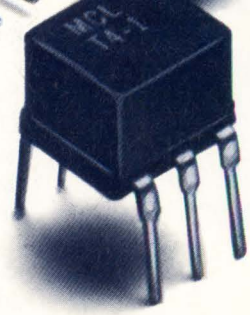
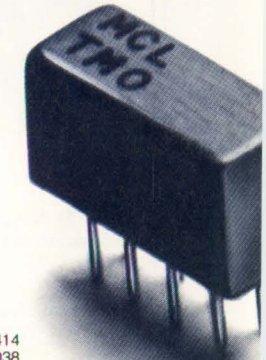
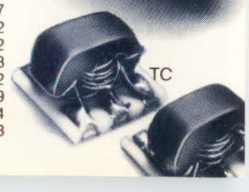


T, TH, TT
bent lead version
style KK81



T, TH, TT
bent lead version
style X 65





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T1-1	5950-10-128-3745	TMO2.5-6T	5950-01-215-8697
T1-1T	5950-01-153-0668	TMO3-1T	5950-01-168-7512
T2-1	5950-01-106-1218	TMO4-1	5950-01-067-1012
T3-1T	5950-01-153-0298	TMO4-2	5950-01-091-3553
T4-1	5950-01-024-7626	TMO4-6	5950-01-132-8102
T9-1	5950-01-105-8153	TMO5-1T	5950-01-183-0779
T16-1	5950-01-094-7439	TMO9-1	5950-01-141-0174
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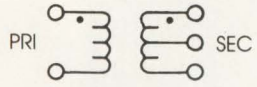
A* 	T	T1-1T	1	.05-200	.05-200	.08-150	.2-80	4.45
		T1-6T	1	.003-300	.003-300	.01-150	.02-50	6.95
		T2-1T	2	.07-200	.07-200	.1-100	.5-50	4.95
		T2.5-6T	2.5	.01-100	.01-100	.02-50	.50-20	4.95
		T3-1T	3	.05-250	.05-200	.1-200	.5-70	4.95
		T4-1	4	.2-350	.2-350	.35-300	.2-100	3.25
		T4-6T	4	.02-250	.02-250	.05-150	0.1-100	4.45
		T5-1T	5	.3-300	.3-300	.6-200	.5-100	4.95
		T8-1T	8	.03-140	.03-140	.10-90	1-60	7.95
		T13-1T	13	.3-120	.3-120	.7-80	5-20	4.95
		T16-6T	16	.03-75	.03-75	.06-30	.1-20	5.65
	TH	T4-1H	4	10-350	10-350	15-300	25-200	5.95
	TMO	TMO1-1T	1	.05-200	.05-200	.08-150	.2-80	7.95
		TMO2-1T	2	.07-200	.07-200	.1-100	.5-50	8.45
		†TMO2.5-6T	2.5	.01-100	.01-100	.02-50	.05-20	8.45
		†TMO3-1T	3	.05-250	.05-250	.1-200	.5-70	7.95
		TMO4-1	4	.2-350	.2-350	.35-300	2-100	6.25
		TMO5-1T	5	.3-300	.3-300	.6-200	5-100	8.45
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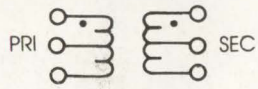
B* 	TT	TT1-6	1	.004-500	.004-500	.02-200	.1-50	6.95
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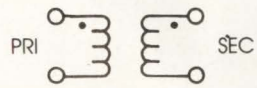
		TT2.5-6	2.5	.01-50	.01-50	.025-25	.05-10	6.45
		TT4-1	3	.05-200	.2-50	.2-50	1-30	5.95
		TT4-1A	4	0.1-300	0.1-300	0.2-250	0.3-180	6.95
		TT25-1	25	.02-30	.02-30	.05-20	.1-10	9.95
	TTMO	TTMO25-1	25	.02-30	.02-30	.05-20	.1-10	11.95
		TTMO1-1	1	.005-100	.005-100	.01-75	.05-40	11.45
		TTMO4-1A	4	0.1-300	0.1-300	0.2-250	0.3-180	13.95
C 	T	T1-1	1	.15-400	.15-400	.35-200	2-50	3.25
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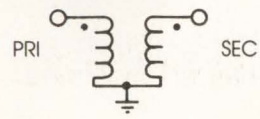
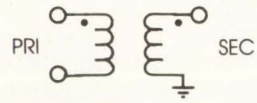
		T1-6	1	.01-150	.01-150	.02-100	.05-50	5.65
		T1.5-1	1.5	.1-300	.1-300	.2-150	.5-80	4.45
		T1.5-6	1.5	.02-100	.02-100	.05-50	0.1-25	5.65
		T2.5-6	2.5	.01-100	.01-100	.02-50	.05-20	4.45
		T4-6	4	.02-200	.02-200	.05-150	.1-100	4.45
		T9-1	9	.15-200	.15-200	.3-150	2-40	3.95
		T16-1	16	.3-120	.3-120	.7-80	5-20	4.45
		T36-1	36	.03-20	.03-20	.05-10	.1-5	6.95
	TO	TO-75	1	10-500	—	10-500	40-250	6.95
	TH	T1-1H	1	8-300	8-300	10-200	25-100	5.95
		T9-1H	9	2-90	2-90	3-75	6-50	6.45
		T16-H	16	7-85	7-85	10-65	15-40	6.45
	TMO	TMO1-02	1	1-800	1-800	2-500	—	9.45
		TMO1-1	1	.15-400	.15-400	.35-200	2-50	6.25
		TMO1.5-1	1.5	.1-300	.1-300	.2-150	.5-8	8.45
		†TMO2.5-6	2.5	.01-100	.01-100	.02-50	.05-20	7.95
		†TMO4-6	4	.02-200	.02-200	.05-150	.1-100	7.95
		TMO6-1	6	.3-200	.3-200	.5-150	5-50	7.95
		TMO9-1	9	.15-200	.15-200	.3-150	2-40	7.95
		TMO16-1	16	.3-120	.3-120	.7-80	5-20	7.95
D 	T	T2-1	2	.050-600	.050-600	.1-400	.5-200	3.95
		T3-1	3	.5-800	.5-800	2-400	—	4.45
		T4-2	4	.2-600	.2-600	.5-500	2-250	3.95
		T8-1	8	.15-250	.15-250	.25-200	2-100	3.95
		T14-1	14	.2-150	.2-150	.5-100	2-50	4.95
	TMO	TMO2-1	2	.050-600	.050-600	.1-400	.5-200	7.95
		TMO3-1	3	.5-800	.5-800	2-400	—	8.45
		TMO4-2	4	.2-600	.2-600	.5-500	2-250	7.95
		TMO8-1	8	.15-250	.15-250	.25-200	2-100	7.95
		TMO14-1	14	.2-150	.2-150	.5-100	2-50	8.45
	FT	FT1.22-1	1.22	.005-100	.005-100	.01-50	.05-25	35.95
		FT1.5-1	1.5	.1-400	.1-400	5-200	1-100	35.95
E 	FTB	FTB-1	1	.2-500	.2-500	.5-300	1-100	36.95
		FTB1-6	1	.01-125	.01-125	.05-50	.1-25	36.95
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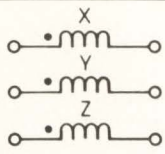
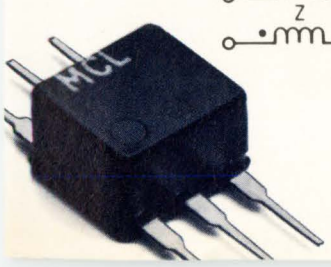
F 	T	T-622	1	0.1-200	0.1-200	0.5-100	5-80	3.25
		T626	1	0.01-10	0.01-10	0.2-5	.04-2	3.95



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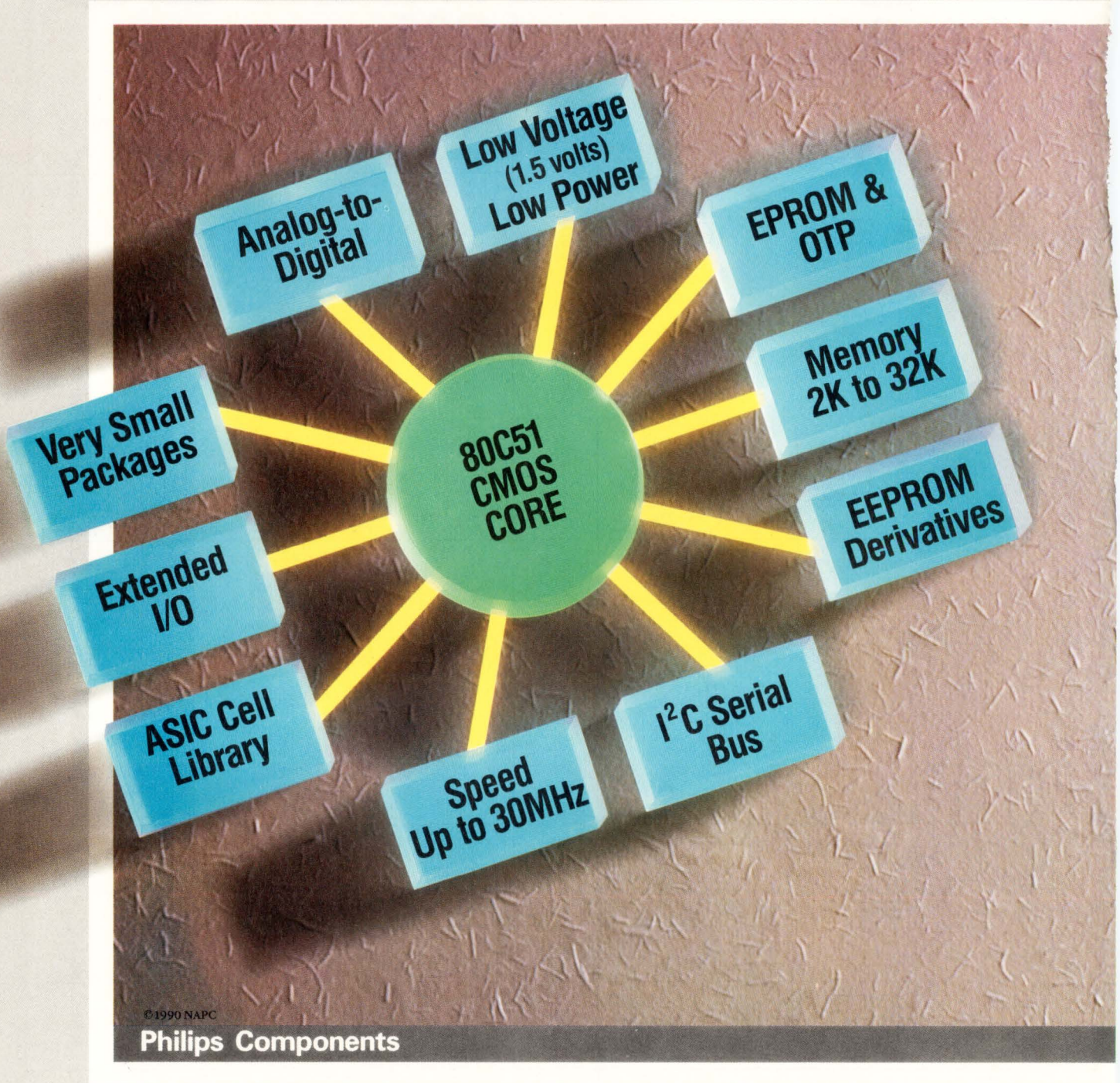

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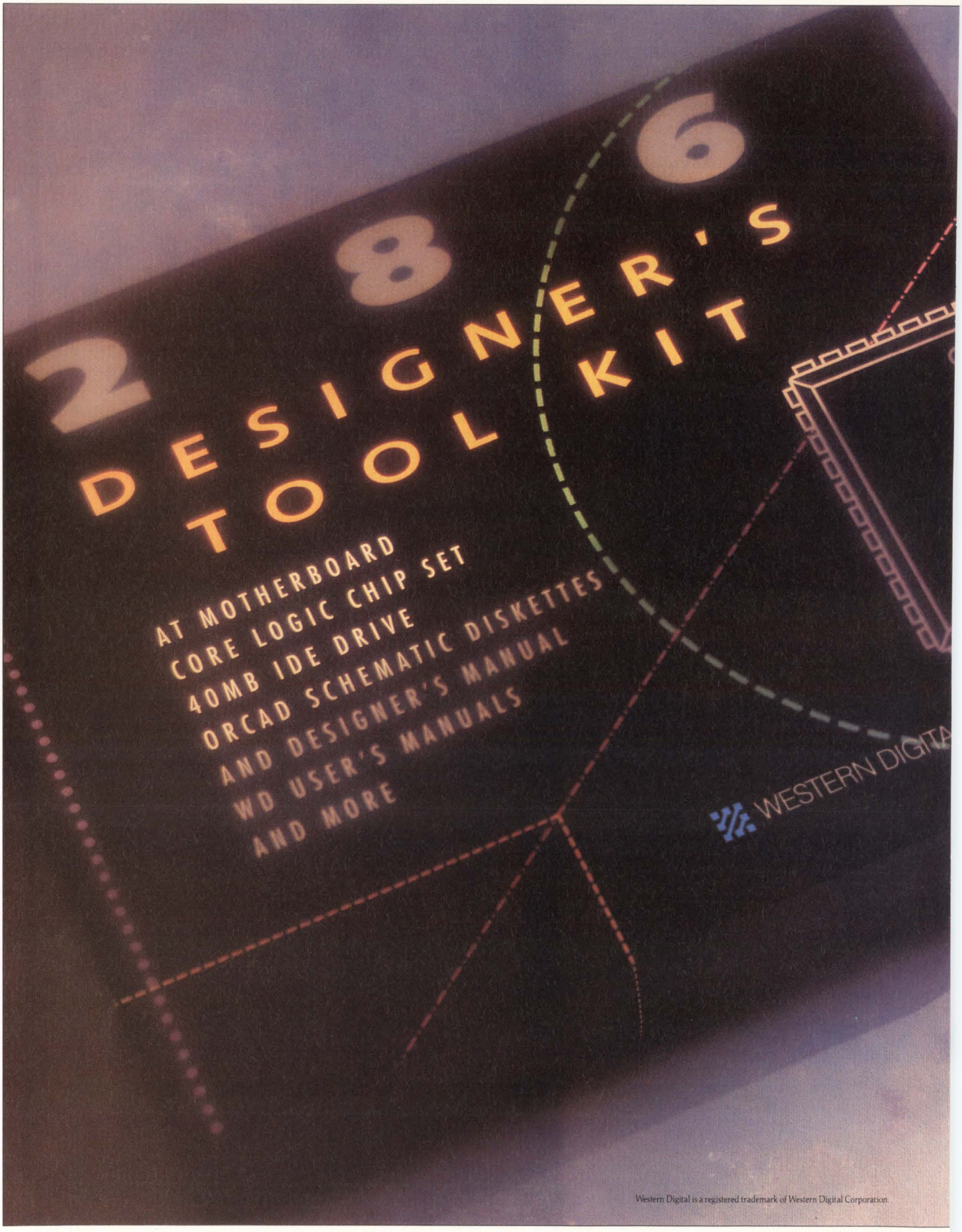
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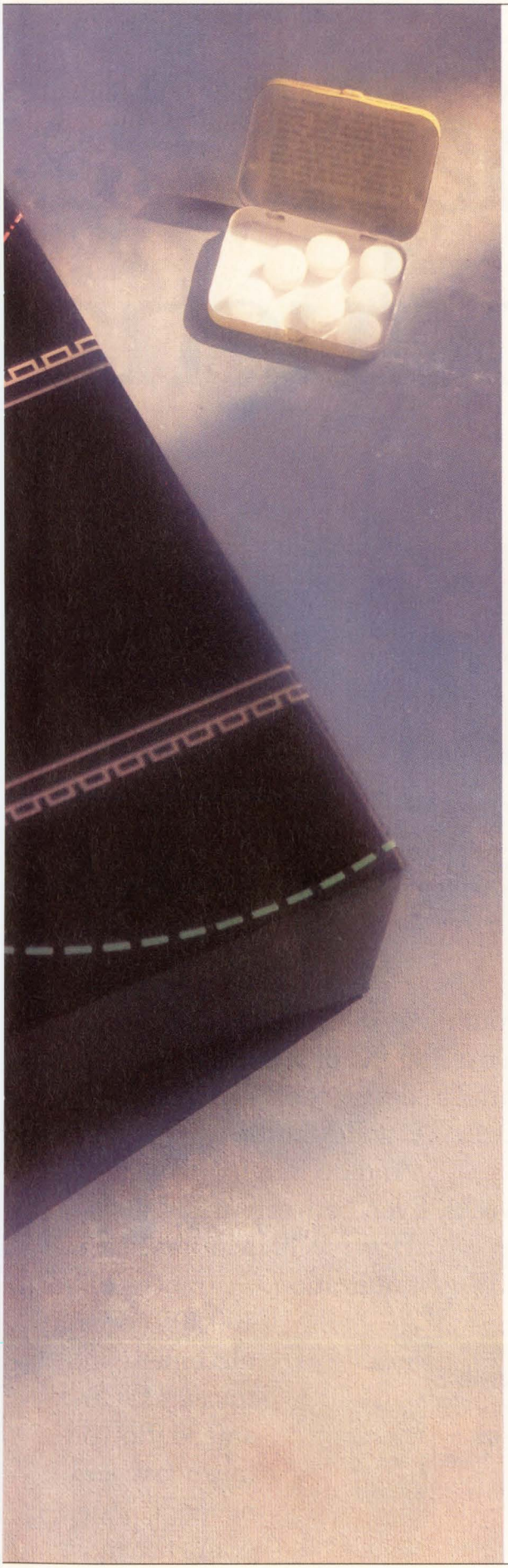

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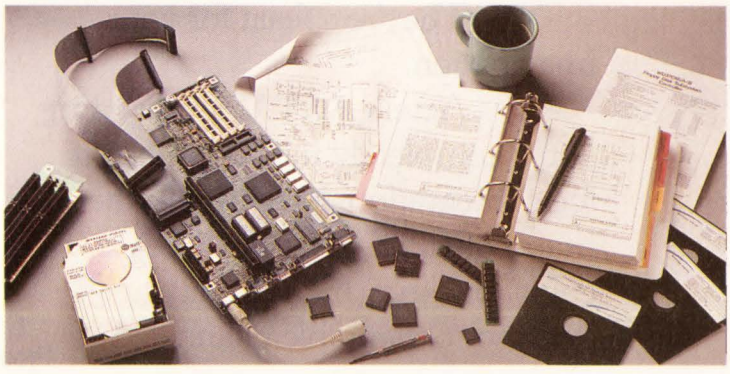

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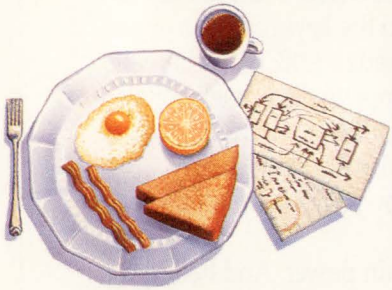
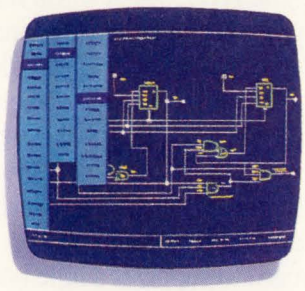
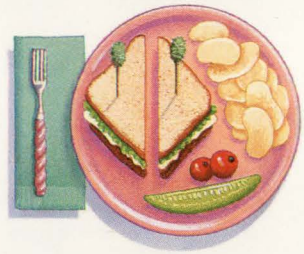


7:05 am: Breakfast
Suddenly, between bites, the answer to that new system design jumps right into your brain. But how to make it work in silicon? Use an Actel field programmable gate array!



8:50 am: Design
You warm up the design program on your 386 and put in the final touches. Then a quick rule check and 25 MHz system simulation with the Action Logic System software.

11:00 am: Place & Route
You watch the system place and route all 1700 gates (out of 2000 available) in under 40 minutes. 100% automatically! A final timing check. Then think of something to do until lunch.



12:00 pm: Lunch
Remember lunch? Normal people actually *stop working* and have a nice meal—right in the middle of the day! With Actel's logic solution, this could become a habit.

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Actel's ACT™ 1 arrays bring you a completely new approach to logic integration. Not just another brand of EPLD, PAL® or LCA™ chips. But true, high density, desktop configurable, channeled gate arrays.

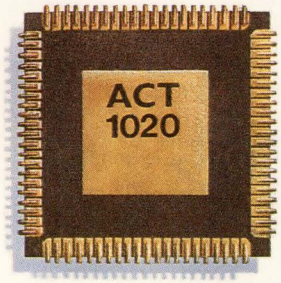
They're the core of the Action Logic System, Actel's comprehensive design and production solution for creating your own ASICs. Right at your desk. On a 386 PC or workstation. With familiar design tools like Viewlogic,™ OrCAD,™ and Mentor.™

And do it in hours instead of weeks. Even between meals.

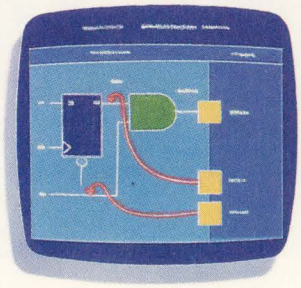
How? With features like 85% gate utilization. Guaranteed. Plus 100% automatic placement and routing. Guaranteed. So you finish fast, and never get stuck doing the most

Actel FPGA Product Family		1010A	1020A
Equivalent Gates	Gate Array	1200	2000
	PLD/LCA	3000	6000
User I/O		57	69
System Clock (MHz)		20-40	20-40
Availability		NOW	NOW
Technology (micron)		1.2	1.2

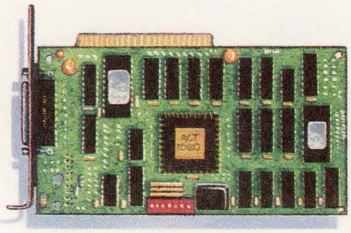
Breakfast And n By Dinner.



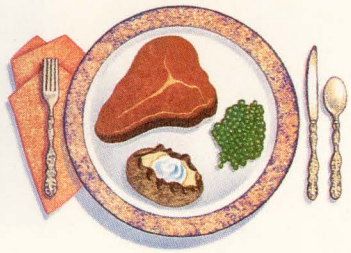
1:15 pm: Program
You load the Activator™ programming module with a 2000-gate ACT 1020 chip and hit "configure." Take a *very* quick coffee break while your design becomes a reality.



1:25 pm: Test
You do a complete, real-time performance check, with built-in test circuits that provide 100% observability of all on-chip functions. *Without* generating any test vectors.



4:00 pm: Production
Your pride and joy is designed, created, tested, and off to the boys in Production. And you're finished *way* ahead of schedule! Better think of something to do until 5:00.



6:00 pm: Dinner
Remember dinner? Normal people actually *go home* and eat with their families. On your way, start thinking about how Actel's logic solution can help you be brilliant tomorrow.

tedious part of the job by hand.

Design verification is quick and easy with our Actionprobe™ diagnostic tools, for 100% observability of internal logic signals. Guaranteed. So you don't have to give up testability for convenience.

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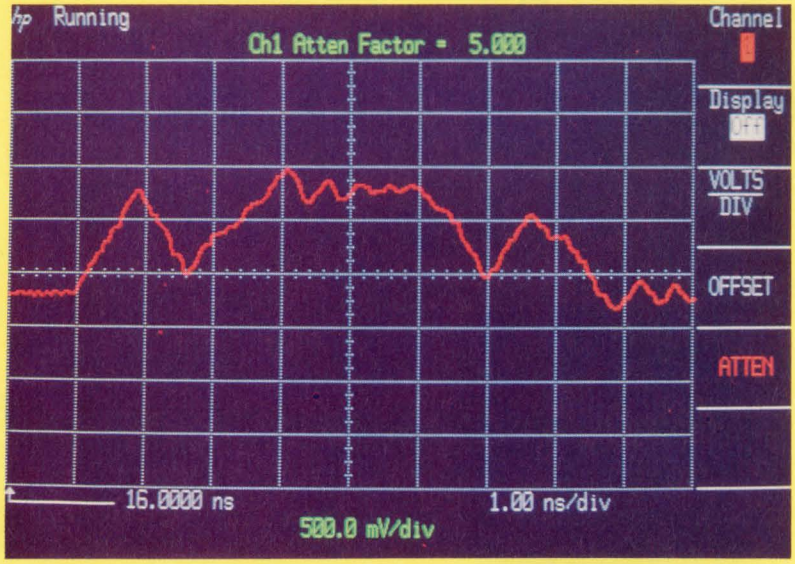

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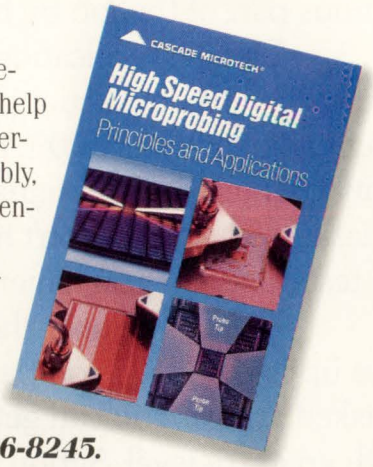

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RISC HARDWARE DEBUG TOOLS

Instruments spur RISC into the real-time race

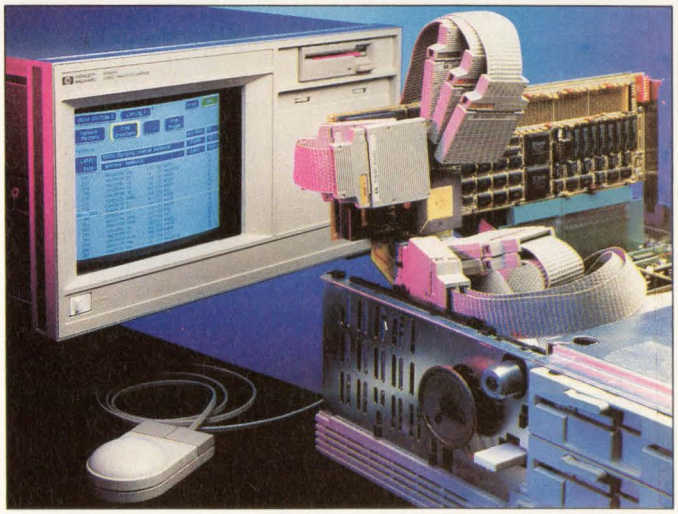
RISC μPs' speed makes them candidates for the fastest embedded real-time systems. But designers may have to look to unfamiliar tools for debugging time-critical hardware/software interactions.

Dan Strassberg,
Associate Editor

Most applications for RISC (reduced-instruction-set computer) μPs have been in computers and workstations, but embedded real-time systems based on RISC processors are starting to proliferate. Debugging embedded systems—in particular, exorcising the time-critical hardware/software interactions that cause them to misbehave—is distinctly different from debugging a workstation. Often, the software-based debugging tools useful for debugging a computer won't work in real time, so they can't handle the whole task of debugging an embedded system. Designers of RISC-based systems no longer need to depend solely on software debugging tools, however.

Hardware debugging tools—ICEs, logic analyzers, and ROM emulators—are becoming available for RISC-based systems. But these tools aren't necessarily what designers of earlier generations of embedded systems relied on. In a sense, many of these new hardware debugging tools are less sophisticated than those for systems based on CISCs (complex-instruction-set computers). One reason for the apparent backward step is that designing hardware debugging tools for RISC-based systems is anything but simple (see **box,** "RISC debug: perils, pitfalls, and pointers"). For designers of in-circuit emulators, for example, the extremely high clock rates and pipelined instructions of RISC processors are but two of the major challenges the ICs present.

Indeed, some tool vendors assert that without close cooperation between designers of RISC chips and designers of ICEs, in-circuit emulators won't exist for RISC μPs. These critics of ICE technology claim that without help from the chip designers, the complexity of designing an ICE for a RISC chip will preclude bringing the instrument to market until late in the chip's life cycle. But late in its life cycle, a chip forms the basis for few new designs and hence re-



If you don't yet have a prototype *of your target board, you can often obtain an evaluation board, such as this one for Motorola's 88000 family. The board plugs into the ISA bus, which lets you use a single PC for code development and debugging. Here, a Hewlett-Packard 16500 logic-analysis system puts the board through its paces.*

quires few debugging tools. So, according to these pessimists, without support from chip vendors, ICE vendors won't be able to make a profit from RISC tools and thus won't offer them.

Cooperation yields tools

Thanks to cooperation between a few chip vendors and ICE vendors, some RISC chips are getting ICE support early in their life cycles. Notable among these chips are Advanced Micro Devices' AM29000 and Intel's i960CA. AMD developed an active program of supporting tool vendors even before the availability of 29000 silicon. AMD's efforts have paid off with 29000 ICEs from such vendors as Hewlett-Packard, Step Engineering, and Embedded Performance (**Table 1**).

Intel, in a turnabout from its stance on its CISC chips, has also actively solicited tool vendors' support for its RISC chips. The firm is one of the few μP vendors with an in-house development-tool operation. That operation will compete with third parties in the i960 market. (Although Intel has seen third parties introduce many tools for its CISC chips, the company actively markets its own CISC tools and is a major supplier of such tools.)

To date, Intel's liaisons with hardware-tool vendors have produced just one offspring, Step's Express 960. The ICE connects to an IBM PC/AT computer via a parallel link and embodies an architecture that makes possible nonintrusive real-time emulation at frequencies as great as 25 MHz. The instrument's emulation processor doesn't replace the target processor; instead, the two μPs work in concert, executing the same code. The ICE's introductory price of $13,500 is less than half the cost of some ICEs for 32-bit CISC μPs. Delivery is 60 days ARO. Another major supplier of ICEs, Applied Microsystems

RISC debugging: perils, pitfalls, and pointers

In the design of hardware debugging tools for systems based on RISC μPs, the chips' high clock rates are just the beginning of the tool designers' problems. These problems also affect the users of such tools.

Although each processor presents its own challenges, certain features are generic. RISCs tend to perform several operations in parallel. This parallelism has encouraged many chip designers to use multiple external buses, which require IC packages with large numbers of pins. Pin-grid-array (PGA) packages are common; they are through-hole mounted and probing their leads is well understood—if not always easy. However, the high cost of PGAs has motivated designers to replace them with less expensive packages, such as plastic quad flatpacks. Unfortunately, these packages are surface mounted and have fine-pitch leads for which probing techniques are not as well developed.

The large number of pins requires that hardware debug tools have many channels. For example, compare the channel requirements for logic analysis of a popular CISC μP, Motorola's 68030, with those of a RISC. The 68030 requires probing 96 pins. A similarly thorough job of probing a RISC processor can require making contact with more than 200 pins—perhaps as many as 250. Obviously, adding channels raises an instrument's price, although not all RISC tools cost more than their CISC counterparts. For example, Step's Express 960 ICE costs less than half what you'd have to pay for some full-featured ICEs for 32-bit CISC μPs. From **Tables 1** and **2,** you can get an idea of the cost of RISC ICEs and of logic analyzers equipped for RISC debugging.

Where RISC designers have chosen to multiplex addresses and data onto a single external bus, the bus speed can make your head spin. Unlike CISC processors, whose bus cycles usually span several clock cycles, RISC bus cycles normally correspond to a single clock cycle. But where the bus is multiplexed, you can have addresses valid on, say, the rising edge of a square-wave clock and memory data valid on the falling edge. IC manufacturers have already announced RISC chips that use such schemes. The MIPS R3000 is one of them. Its maximum clock rate is 33 MHz, but its bus, in effect, operates at twice that speed. When debugging a system based on this chip, you must capture data going to or from memory just 15 nsec after you capture the address. Your debug hardware must sort out what is an address and what is memory data.

Passive probing can be precarious

Designers of RISC debugging tools must also be sure that the debug hardware doesn't alter the data by, for example, capacitive loading. When the chip's package geometry severely limits the space between

Corp (AMC), intends to introduce an i960 ICE in early 1991.

Earlier this year, AMC announced a new type of hardware development tool called the CodeTAP. This instrument performs many, but not all, ICE functions. The first CodeTAP is for an Intel CISC μP, the 80386, and costs $5000—a fraction of the price of a full-featured ICE for a high-performance μP. AMC will not comment on whether it has RISC CodeTAPs under development, but acknowledges that it began receiving inquiries about such products soon after announcing the CodeTAP 386.

Like AMC's CodeTAP, Intel's

Table 1—Representative RISC ICEs

Vendor	Model	Supported processor	Price[1]	Comments
Embedded Performance	SYS29K	Am29000 Am29005	$15,000	Other supported products include R3000, R3000A, and R3001. Host can be IBM PC/AT or workstation from Sun, DEC or HP.
Hewlett-Packard Co	64774B	Am29000	$38,000	Has 512k bytes of emulation memory; $33,000 without memory. Use HP9000 Series 300 as host.
Intel	ICE960KB	i960KA/KB	$16,495	Requires IBM PC or compatible computer with 640k bytes of RAM, 1M byte of expanded RAM, 20M-byte hard disk, and MS-DOS V3.3.
Step Engineering	Adapt II	Am29000 Am29027	$13,500	Step offers an extensive set of integrated hardware and software development tools for these ICs. Use PC or ASCII terminal as host.
	Express960	i960CA	$13,500	

Notes: 1. Approximate US list price of the minumum usable configuration. Vendor-supplied software required for ICE operation is included; cost of the host program-development system is not included.

pins, the debug tool—whether it's a logic analyzer or an ICE—must use passive probing to save space. But miniature passive probes that do not excessively load or distort 66-MHz signals are decidedly at the cutting edge of technology.

In addition to high-speed buses, a component central to RISC designs is cache memory. When the cache is on the CPU chip, as it is with many RISCs (Motorola's 88000 family is one exception), you can't get at points you will probably need to see during debugging. What you really need is a special "bond-out" version of the processor—one in which the chip vendor brings certain internal nodes to pins. Bond-out versions of CISC processors aren't as readily available as tool vendors would like (**Ref 1**), and RISC bond-out chips are even harder to come by.

For designers of RISC debug tools as well as for designers of RISC-based systems, pipelined instructions are another vexing μP feature. (The problem is not unique to RISCs—some CISC processors also use pipelines.) If the processor doesn't execute every instruction in the queue—for example, if it skips a sequence of instructions at a program's branch point—determining what the CPU is doing can challenge even an experienced troubleshooter. A related problem is understanding exactly what happens when the processor flushes the pipeline.

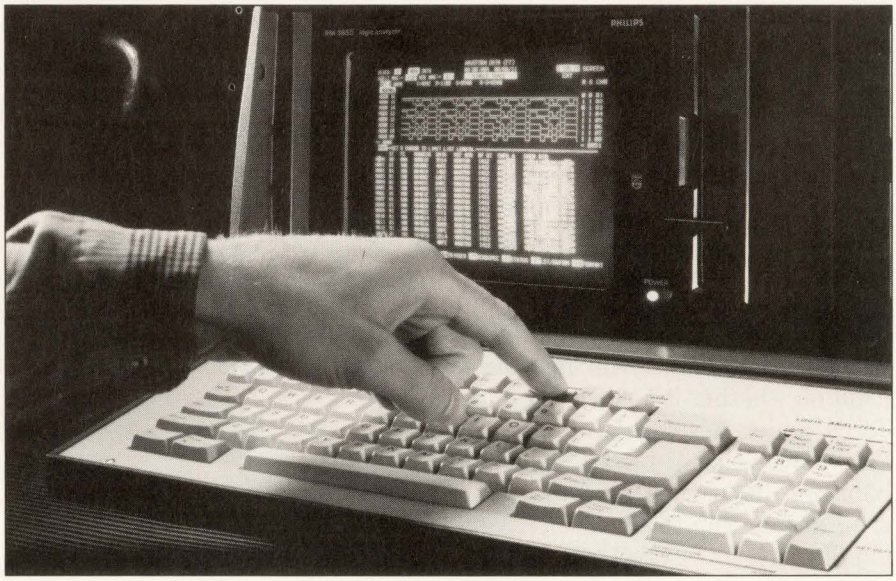
Underlying most of the RISC debugging process is the intimate relationship between the high-level-language compiler you use, the code it generates, and your system hardware—especially the CPU. There are very few instances where you'll use assembly language to code RISC software, so you'll be writing nearly all of your code in a high-level language. Although the output of any compiler is CPU specific, the efficiency with which a RISC performs a task depends critically on how efficiently the compiler uses the chip's resources. This compiler dependence is far greater with RISCs than with CISCs. Therefore, your selection of a compiler is extremely important. Equally important is the selection of software and hardware debugging tools that work well with the compiler and with each other.

As far as optimizing code is concerned, using a RISC can be a double-edged sword. The good news is that a RISC processor may very well give you so much computing power that you don't need to devote a lot of effort to software performance analysis and code optimization. The bad news is that these tasks are usually more complex with a RISC than with a CISC, especially if you have no experience in optimizing RISC code. Both chip and tool vendors point out that if your application demands that you optimize code, your entire tool set—not just your performance-analysis tools—will be a major factor in determining how smoothly you can accomplish the job.

RISC hardware debug tools

$4000 DB960CADIC in-circuit debugger is aimed at letting members of large development teams debug code modules prior to system integration. The small board—which has a stock i960CA chip, a ROM containing a retargetable debug monitor, and an RS-232C/RS-422 port—plugs into the target system in place of the μP. Connect the serial port to an IBM PC running the MS DOS version of Intel's C960 C compiler ($700), and you can do a great deal of source-level debugging.

Of course, if you have a 12-person development team, you may balk at building 12 prototypes of your target CPU board so that each team member can use an in-circuit debugger. Intel's solution to that problem



State-analysis at 100 MHz; *capacitive loading of 8 pF max; custom disassemblers for RISCs, including Intel's i960CA; and an integral IBM PC/AT-compatible computer make the PM 3655 logic analyzer from Philips/Fluke an excellent choice for RISC debugging.*

For more information . . .

For more information on the hardware debugging tools discussed in this article and related products for RISC-based systems, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you read about their products in EDN.

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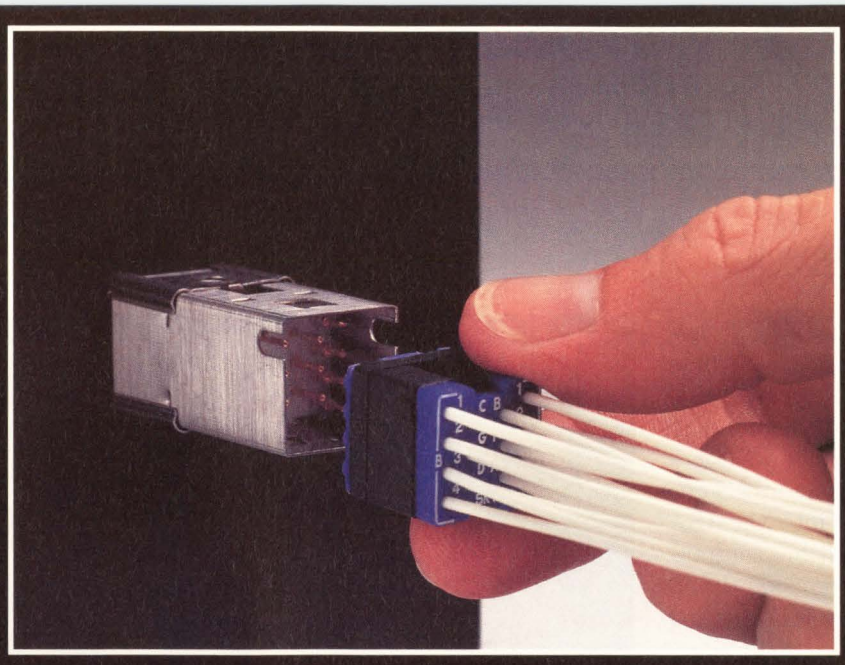

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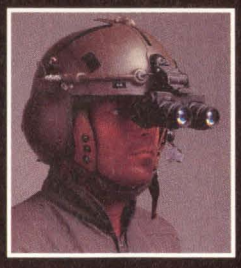

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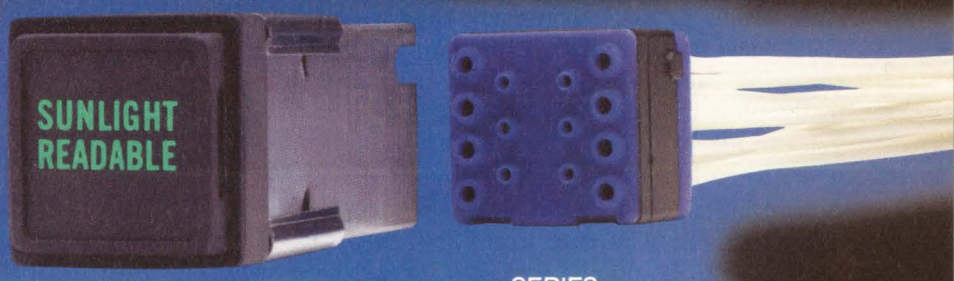

SERIES

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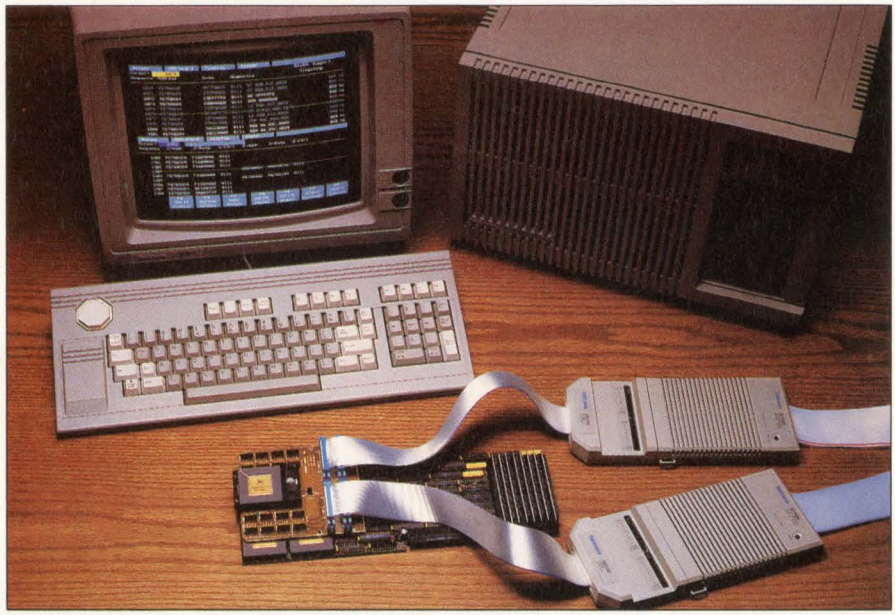
RISC hardware debug tools

is to have you use its $3500 EV 80960CA CPU evaluation boards in place of the additional prototypes. Both chip vendors and tool vendors offer such evaluation boards for a variety of RISC processors. Some of these boards plug into the ISA bus of IBM PC-compatible computers, thus letting you do code development and at least partial testing on one machine.

Something you can't do with an in-circuit debugger is real-time tracing. For that operation you need an ICE, and at the moment, RISC ICEs are scarce.

But just because a particular RISC has no ICE, don't assume that there are no hardware debugging tools for it. In many cases, you can obtain a logic analyzer with hardware and software that some vendors sell together under names such as "disassembler pod" or "analysis package." Many of these packages include disassemblers that feature user-definable mnemonics. (Some vendors refer to the processor-specific hardware units as preprocessors and the software as inverse assemblers.) Compared with ICEs, logic-analyzer-based RISC debug tools are rather plentiful (**Table 2**).

At least one vendor, Arium, offers a ROM emulator that works with its RISC-compatible logic analyzers. The emulator plugs into the ROM sockets of your target system, replacing the chips you would normally plug in. With the emulator, you can easily modify the code that will ultimately reside in ROM because that code temporarily resides in RAM. Arium's product uses high-speed static RAMs and connects to the firm's ML-4400 logic analyzer. All communication between the emulator and the target system occurs through the ROM sockets. The analyzer's serial port lets you download code from your host system,



To support the 88100, *Tektronix's DAS 9200 uses the 92DM35 support package. A single connector probes the 181-pin PGA. The analyzer monitors all cached and noncached program activity in real time at speeds as fast as 33 MHz.*

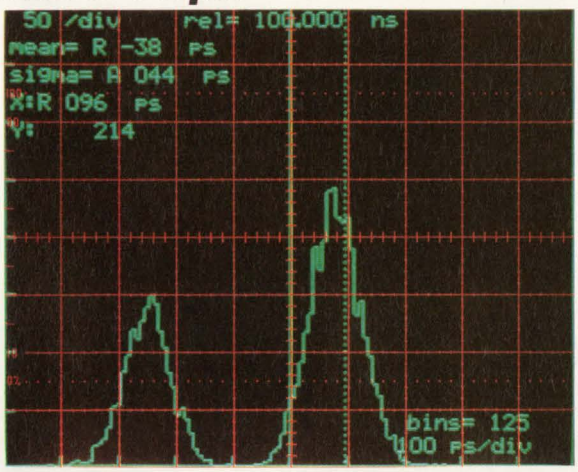
Table 2—Representative logic analyzers that support RISCs

Vendor	Model[1]	Max state-analysis speed	Supported processor	Price[2]	Comments
Arium	ML4400S	50 MHz	88100	$16,000	256k-byte ROM emulator $1995 extra.
		25 MHz	R3000	$9600	
Biomation	CLAS 4000	50 MHz	CY7C601 (SPARC)	$47,000	Packages support R3000, Am29000, 88100, 88200, i860, i960, and CY7C611.
Fluke	PM 3655/R	100 MHz	I960CA R2000	$13,200	400-MHz timing analysis $5500 extra.
	PM3585/90	50 MHz	See note 3.	$10,800	200-MHz timing analysis standard.
Hewlett-Packard Co	1650B[4]	35 MHz	88200	$9000	Preprocessors for i860 (PGA), 88100, 88200, and R3000[5]. Bus interfaces for Am29000, 88100, 88200, and i960CA.
Tektronix	DAS 9200	>33 MHz	88100	$40,000	Monitors M and P buses.
			I860		
VMEtro	PMA-030	25 MHz	88100 and 88200	$9000	Monitors M or P bus; for $18,000, monitors both. Require terminal or PC.

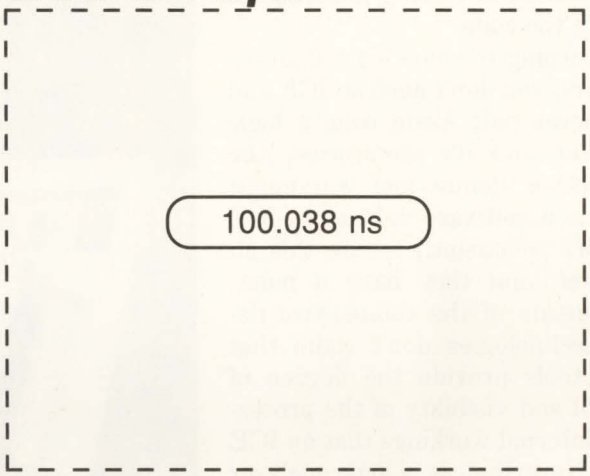
Notes: 1. In general, to specify a functioning logic-analysis system, your purchase order must list model numbers for a mainframe and a group of system components. This column shows only the mainframe model number.
2. These are approximate US list prices of complete systems equipped to work with the listed processor.
3. Introduction date of this product is October 1, 1990. Analyzer currently provides general-purpose RISC support.
4. In general, H-P's RISC accessories also work with the 1652B logic analyzer/scope and 16500A modular logic-analysis system.
5. Preprocessor for R3000 is offered by a third party. With R3000, analyzers support processor operation to 17.5 MHz.

A picture is worth a thousand points in a time interval measurement.

SR620 Output



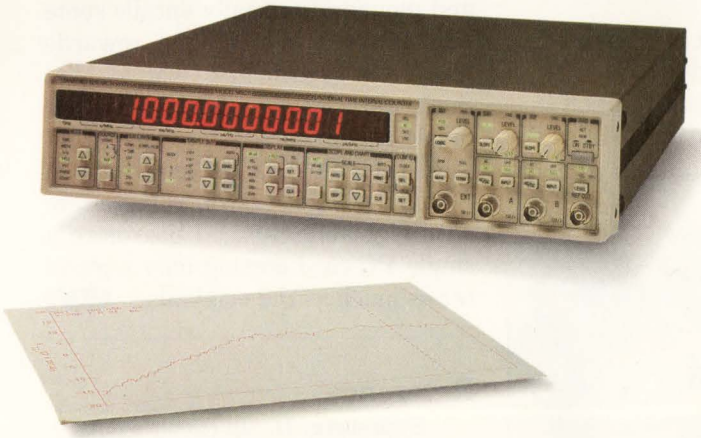
HP5370B Output



The SR620 brings graphic statistical analysis to time interval and frequency measurements. The SR620 shows you more than just the mean and standard deviation - multimode frequency distributions or systematic drift for example. Histograms or time variation plots are displayed on any X-Y oscilloscope, complete with Autoscale, Zoom, and Cursor functions. Hardcopy to plotters or printers is as easy as pushing a button.

Of course, the SR620 does everything else you'd expect from a high resolution universal counter, such as frequency, period, time interval, pulse width, rise / falltime, and phase measurements. The SR620 offers 25 ps single-shot time and 11 digit frequency resolution and complete statistical analysis, all for a fraction of the cost of comparable instruments.

For the whole picture, call SRS and ask about the SR620.



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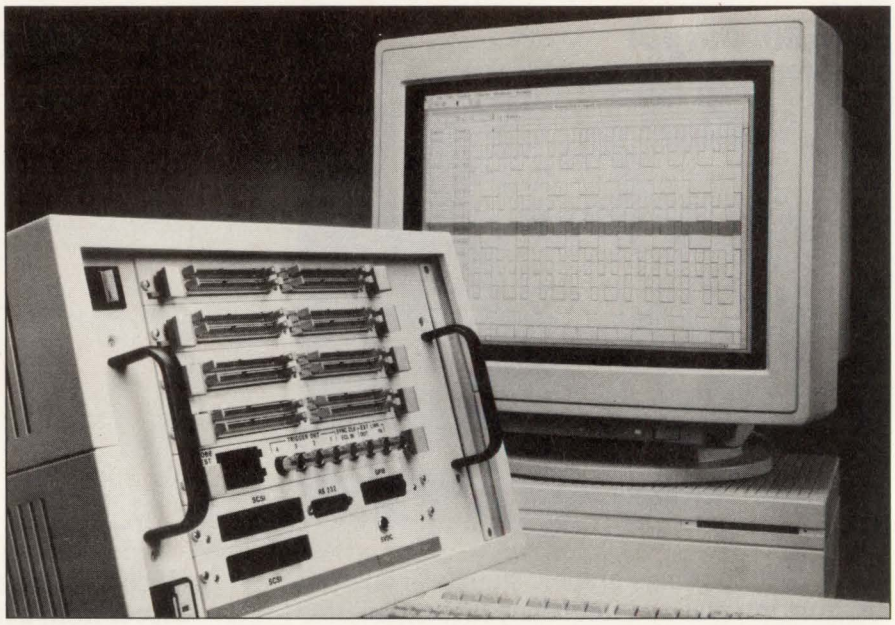
and you can also use the instrument's built-in editing functions to modify the code.

According to some logic-analyzer vendors, you don't need an ICE and you never did: Aside from a logic analyzer and its accessories, the only other debug tool you might need is a software debugger. ICE vendors vehemently refute this allegation, and they have a point: Proponents of the competitive debug technologies don't claim that their tools provide the degree of control and visibility of the processor's internal workings that an ICE does. Nevertheless, a logic analyzer can be an invaluable debugging tool, with or without an ICE.

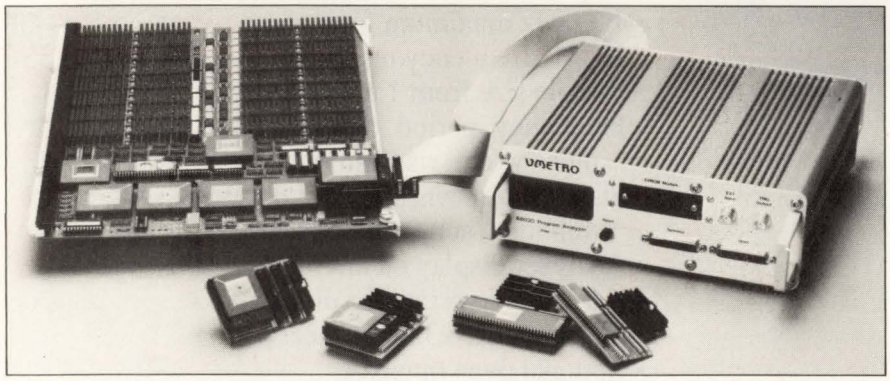


RISCs have high pin counts *and high speeds. Because of its modular architecture, Biomation's CLAS 4000 logic analyzer can have 384 channels. It performs state analysis at 50 MHz max and timing analysis at 200 MHz max. You can get the analyzer with analysis packages for the Motorola 88100 and the CY7C601 SPARC.*

Pick μP and tools together

There are few endeavors in electronics that evoke a unanimous response from dozens of engineers. In most respects, such diversity characterized the responses of the suppliers of hardware debug tools for RISC-based systems that EDN contacted for this article. But in one area, the respondents were unanimous. All agree that you should select the debugging tools you plan to use—that is, both the hardware and software tools—at the same time you select the μP and the high-level-language compiler. Before making any of your selections final, satisfy yourself that each element you select works well with all of the others.

Above all, if you are tempted to base an embedded-system design on a RISC μP, satisfy yourself that the potential for payoff justifies the risks. (Yes . . . the pun *is* intentional.) At this stage of RISC technology, you must still call any embedded-system design based on a RISC processor a pioneering effort, and pioneering usually entails some pain. Often, though, the rewards make the hardships worthwhile. Such was the case for a customer of one of the tool vendors EDN contacted. Using the RISC chip let him reduce a lighting-control system with eight CISC-based boards to a single PC card costing only a quarter as much as the originals. EDN



Billed as a real-time program analyzer, *VMEtro's PMA-030 is, in fact, a specialized logic analyzer. You can use it with an ASCII terminal or a PC acting as a terminal emulator, or you can use several units with a workstation running windowing software. The analyzer offers trace memory of 2k 92-bit samples. Among RISCs, it explicitly supports the 88100 and 88200.*

Reference

1. Strassberg, D, "In-circuit emulation: ICs and tools tame tough technology," *EDN*, October 26, 1989, pg 73.

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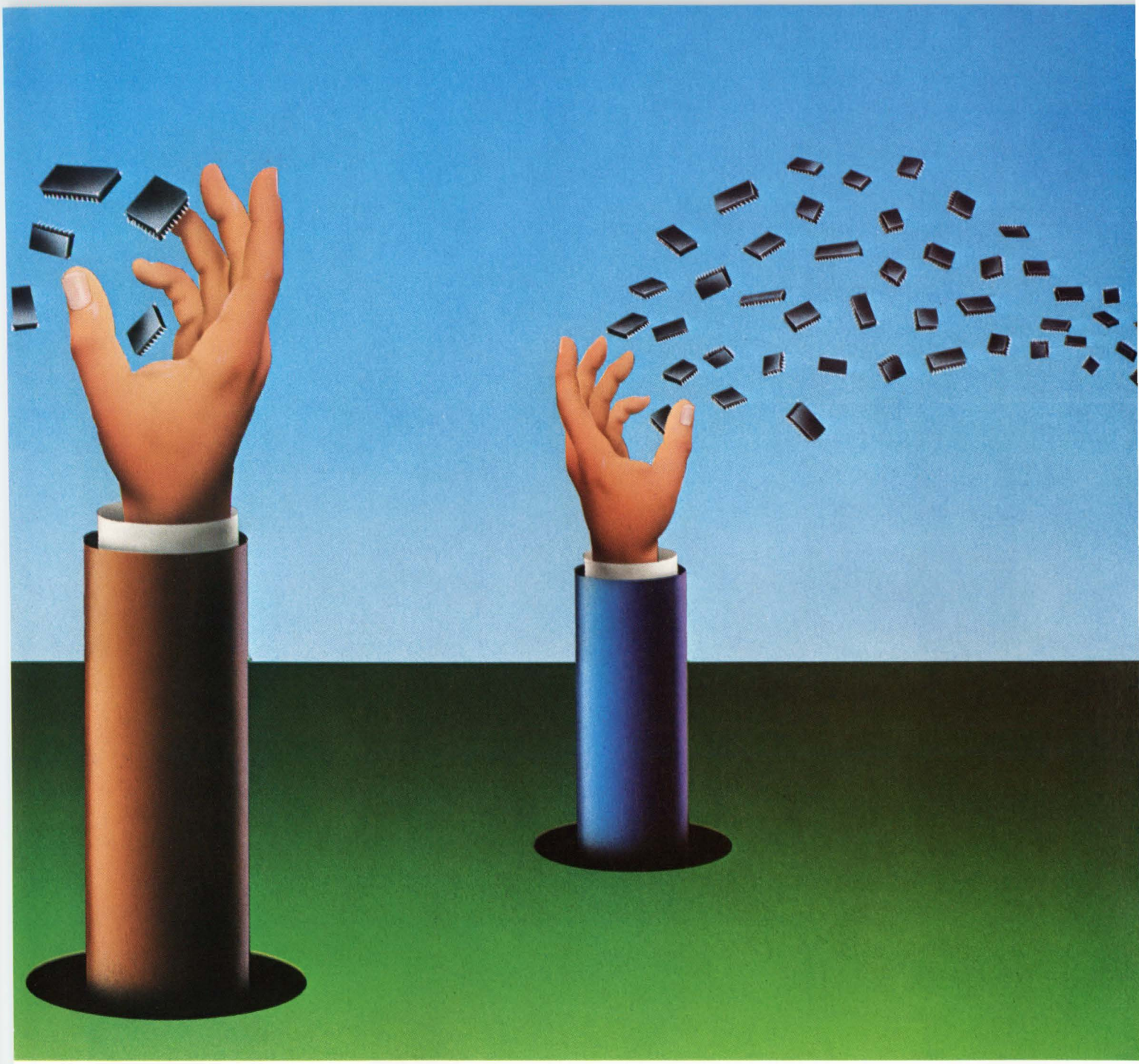

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			- 10	100	60		PAGE	20 SOJ
			- 12	120	50		MODE	20 ZIP
		256K x 4	GM71C4256A - 80	80	66mA	2mA	FAST	20 DIP
			- 10	100	55		PAGE	20 SOJ
			- 12	120	47		MODE	20 ZIP

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THE CHUNG JU REALITY

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"The semiconductor plant is scheduled to be completed by 1996. Goldstar said it was building it to meet soaring demand for memory products..."

"South Korea's Ministry of Trade and Industry put semiconductors at the top of a list of seven high technology industries that it has targeted for rapid development over the next five years..."

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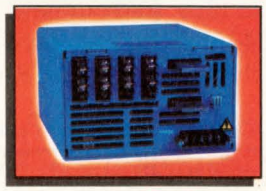

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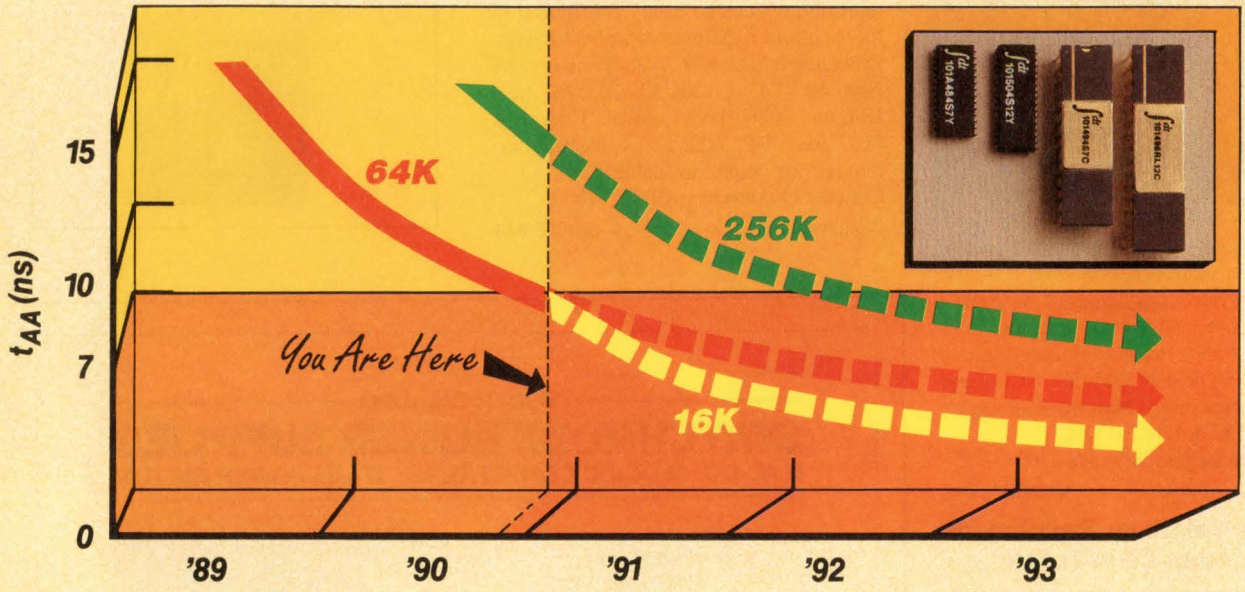

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IDT10490	64K (64K × 1) 10K ECL	8	420
IDT100490	64K (64K × 1) 100K ECL	8	320
IDT101490	64K (64K × 1) 101K ECL	8	420
IDT10494	64K (16K × 4) 10K ECL	7	700
IDT100494	64K (16K × 4) 100K ECL	7	500
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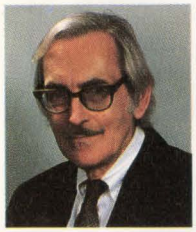
PC chip sets reduce chip count



IBM PC-compatible chip sets range from one to six chips and can give you caching facilities, a choice of buses, and power control.

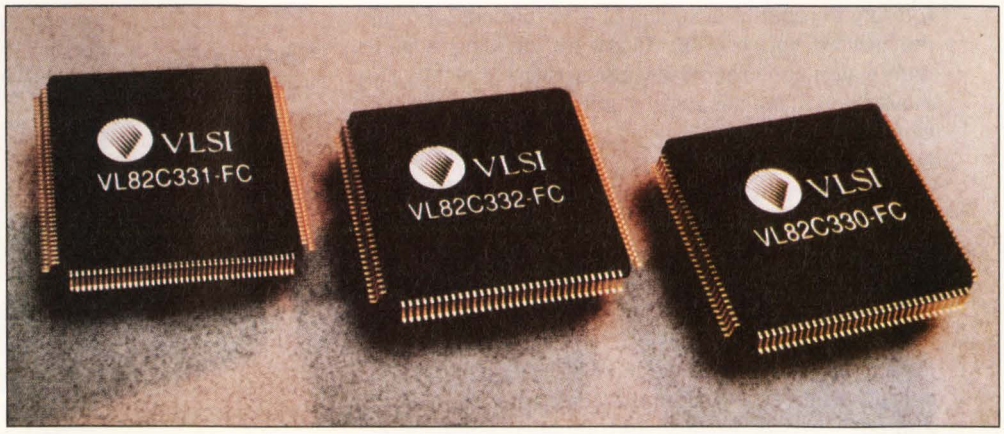
Chris Terry,
Associate Editor

In the six years since Chips & Technologies Inc first produced a VLSI chip set that incorporated all the mother-board logic of an IBM PC/XT, many competitors have added their contributions to the market. If you want to build an IBM PC-compatible computer, you have an almost embarrassingly wide choice of chip sets. You should consider three PC trends when choosing a chip set: one is reducing the price of an average, single-user, 80286-based system; another is the drastic reduction of board size, weight, and power consumption—for example, in notebook-sized and laptop computers; and the third is delivering more and more computing power with 80386- and 80486-based systems. Your chip-set choice thus depends on the application you have in mind.

At the low end, some OEMs are still finding a market for PC/XT clones. This market is diminishing, largely because the IBM PC/AT bus is more convenient and more flexible than the PC/XT bus and has become a de facto industry standard for medium-performance systems running at 12 MHz or less. Nevertheless, PC/XT clones still have a place in situations where low price is the prime consideration. VLSI Technology continues to offer its 2-chip Super-XT chip set at $25 (1000). The chip set lets users set the clock speed to 8 or 10 MHz and provides extended-memory management.

286 still has the lion's share

Intel regards the 80286 as obsolete and is trying hard to create more demand for the high-end 80386 and 80486. However, Charles Parr, marketing director for logic products at VLSI Technology Inc, points out that 12-MHz 80286-based machines still form the largest part of the PC-clone market. He believes that the 80286 will retain its supremacy in the home and office markets for some years to come. He says that 286-based machines have by far the best price/performance ratio in the under-16-MHz category and that their per-



This 3-chip set from VLSI Technology *supports the 80386DX processor at clock speeds of 12 to 33 MHz. The Topcat 386DX chip set can manage as many as 64M bytes of 32-bit memory (4M-byte DRAMs arranged in four banks) and can operate in both caching and noncaching modes.*

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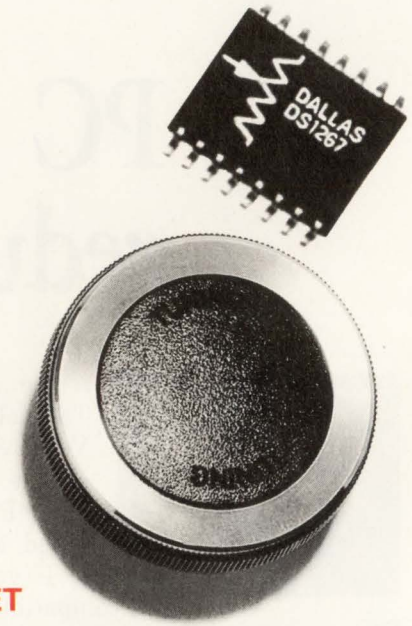

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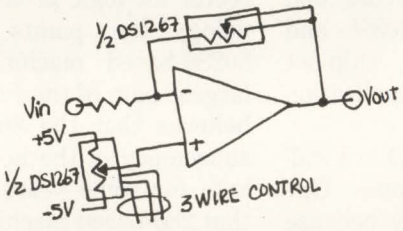

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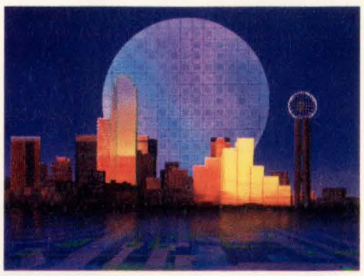

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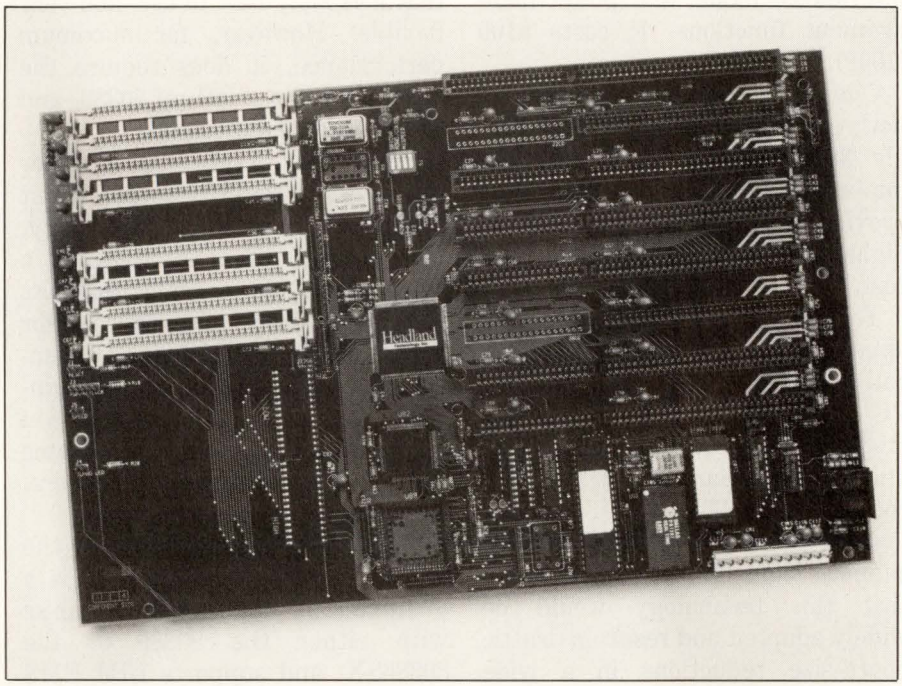
formance is quite adequate for most home and office applications.

Mark Griffin, a development analyst for Texas Instruments' PC Systems, concurs. He cites reports, both from the US and from Taiwan, which indicate that despite predictions that the 80386 would take a big bite out of the 80286 market, the 80286 is still the most-used processor, with 6.5 million units shipped in 1988, possibly declining to 4.5 million per year by 1994.

Just how long 80286-based machines will hold their own against competition from the more powerful 16-bit 80386SX and 32-bit 80386DX machines is still a matter for speculation. Corporate users, who are accustomed to using increasingly powerful computers as tools, are reluctant to tolerate average performance when superior performance is available. If they all shout loud enough and forcefully enough to bring 80386-based machines to their desks, the increased sales volume may quickly bring prices down to the point where 80286-based machines are no longer attractive even to those with tight budgets.

VLSI Technologies covers all the bases by offering a wide range of chip sets. For simple, 12-MHz PC/AT-compatibles, it offers the VL82CPCAT-12QC, a 5-chip set that costs $30 (1000). The VL82CPCAT-16QC version for 16-MHz systems costs $33 (1000). If you need still better performance, the company offers a 6-chip set, the VL82CPCPM-16/20QC, which provides page-mode memory management and other improvements over the 5-chip set. The 16-MHz version costs $38; the 20-MHz version costs $41 (1000).

Chips & Technologies also offers chip sets for 12- to 16-MHz PC/ATs. Its Neat 4-chip set allows zero-wait-state operation at 12 MHz and can operate at 16 MHz with 0.7 wait states if you're using inexpensive 100-nsec dynamic RAMs (DRAMs). The chip set's memory-management system allows single-bank page mode or 2-way and 4-way page-interleaved modes, as well as LIM EMS 4.0 (Lotus-Intel-Microsoft Expanded Memory Standard). The set costs $49 (1000).



Most vendors supply evaluation boards *for their chip sets. The HT21 board lets you evaluate Headland Technology's 80286 chip sets.*

The advent of laptop and notebook-sized computers has created a need to reduce the size and power consumption of the mother board. Several companies succeeded in cramming all the functions of the PC/AT mother board into a single VLSI chip. Texas Instruments, for example, recently released its Tact82411 208-pin chip, which is fabricated in 1-μm CMOS and can operate at clock speeds as high as 20 MHz. The chip's features include software configuration for wait states, command delays, and memory organization. It can operate in single-bank page mode, which lets you make use of less expensive DRAMs, or you can use 2- or 4-way with both 80286 and 80386SX processors at clock speeds as high as 25 MHz. Its memory-management features support 2- or 4-way page-interleaved mode, extended or expanded memory, and shadow RAM for BIOS and video use. This chip includes a number of power-saving features that suit it for laptop computers. These features include an interface to a power-management chip, a selectable clock that in standby mode can let the system run at only 1 MHz, and optional slow DRAM refresh. The single-unit price is $100.

Another single PC/AT support chip for both 80286 and 80386 processors is available from Headland Technology Inc. The Hit Single 386SX/286 is a 208-pin chip that requires only three external TTL chips and can operate at speeds as

high as 16 MHz in 80386 mode and 20 MHz in 80286 mode. Like the ACC Microelectronics chip, this chip supports shadow RAM, a hardware implementation of LIM EMS 4.0, page mode, 2- or 4-way page-interleaved mode, and power-management functions. It costs $100 (1000).

One of the chief advantages of both the ACC-2036 and the Hit Single 386SX/286, as well as other dual-mode chip sets, is that they provide an easy upgrade path to higher performance at a minimal cost.

The 208-pin single support chip appears to be the limit of economically feasible size reduction of PC/AT mother-board logic. Chip-on-board technology let Intel produce the WildCard, a 4×2-in. card containing an 8088 CPU, an 8087 math coprocessor, and all PC/XT support logic. Many people hoped that this technology would be widely adopted and result in drastic board-size reductions in a wide range of applications. In fact, the technology has turned out to be very expensive and is cost effective only for special-purpose computers. As a result, Intel is no longer offering the WildCard. Randy Bachman, a regional sales manager for Via Technologies Inc (Sunnyvale, CA), concedes that a market for boards that use this technology may exist, but says that no ASIC vendors are now selling dice for chip-on-board mounting.

Onward and upward

All of the chip-set vendors previously mentioned are offering chip sets for the 80386SX and 80386DX; many are offering or developing comparable chip sets for the next step—the 80486. One factor that may accelerate growth in the 386/486 market is the release of Microsoft's Windows 3.0. This operating system, which is DOS-based and supports a large proportion of the software already available for PCs, may kill any chance that OS/2 ever had of superseding PC-DOS. People who have tried Windows 3.0, either in beta test or after its release, say that it is fast, easy to use, and very flexible. However, for maximum performance, it does require the speed and bus width of 80386- and 80486-based computers.

Plenty of chip sets support either the 16-bit 80386SX or the 32-bit 80386DX. Headland Technology, for example, offers the GCK131, a set of three 160-pin chips that lets you use an 80387 math coprocessor and as much as 24M bytes of memory. The configuration and performance options are stored in EEPROM; this feature eliminates the need for switches or jumpers. The chip set costs $100 (1000).

VLSI Technology offers the Topcat series; the VL82C286 is a dual-mode 2-chip set that works with either the 80286 or the 80386SX, and supports LIM EMS 4.0 up to the maximum 32M bytes of memory. It costs $50 (1000). The 386DX is a 3-chip set that supports Weitek's (South Bend, IN) 3167 math coprocessor as well as Intel's 80387, and runs at clock speeds of 12 to 33 MHz. This chip set also stores the configuration and performance options in EEPROM, and has many features that reduce power consumption in laptop systems. The memory-management system lets you use as much as 64M bytes of onboard RAM and allows for timing compatibility with older software. You can also use slower add-in expansion cards because a proprietary feature prevents the false decoding of bus addresses. The chip set costs $75 (1000).

Texas Instruments offers the Tact83000, a 3-chip, cache-based set that works with the 80386SX at speeds as high as 33 MHz. The three chips are the PC/AT bus interface unit, the memory-control unit, and the data-path unit. The chip set and four other logic chips are all you need for a 16-bit PC. The 3-chip set costs $50 to $60, depending on quantity. By adding another data-path unit, you can expand the bus width to 32 bits for a system based on the 80386DX. The cost of the four chips ranges between $60 and $75. EDN

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For more information . . .

For more information on the IBM PC chip sets discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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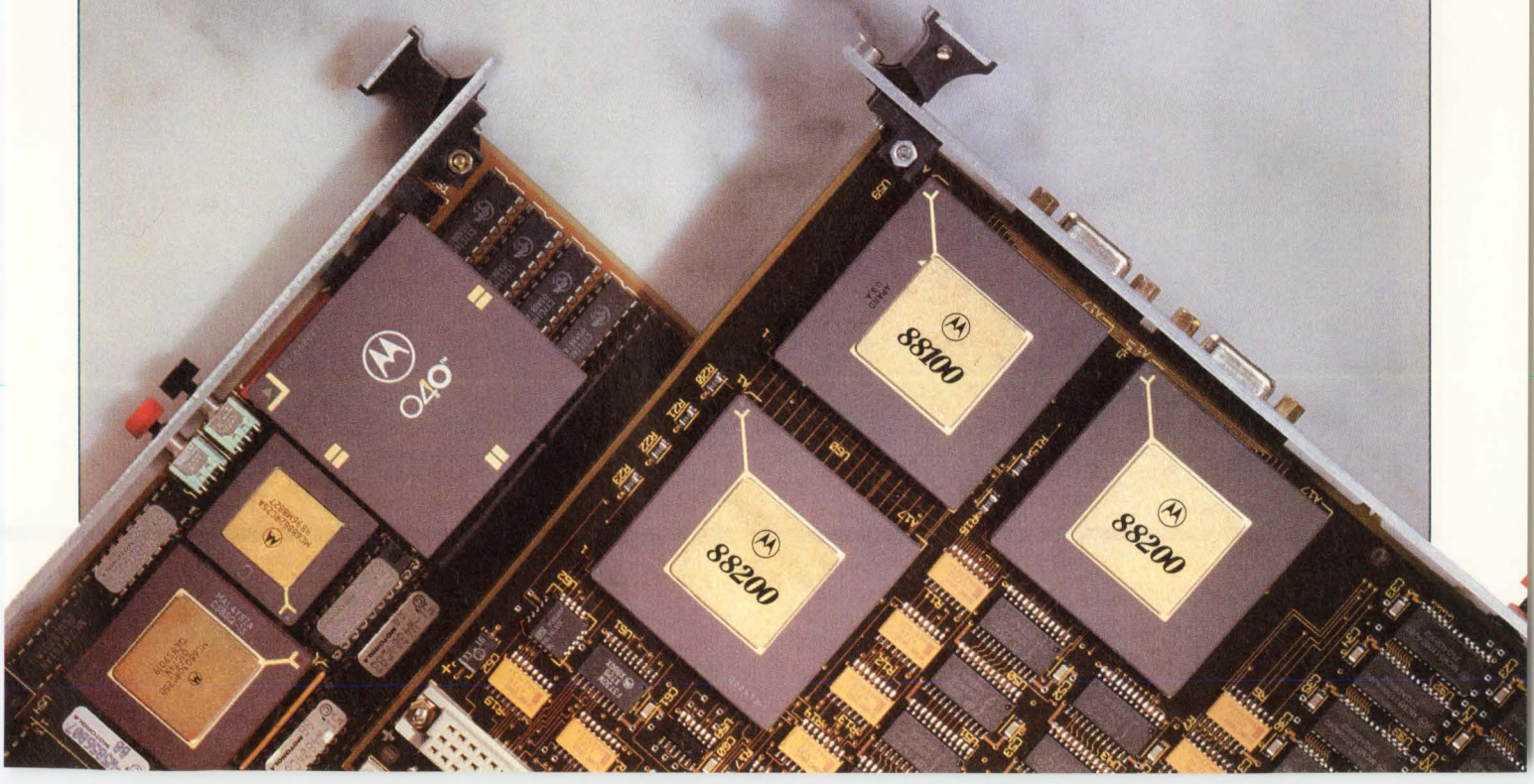

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EDN100190

250-MHz digital storage oscilloscope provides 1G samples/sec for $10,950

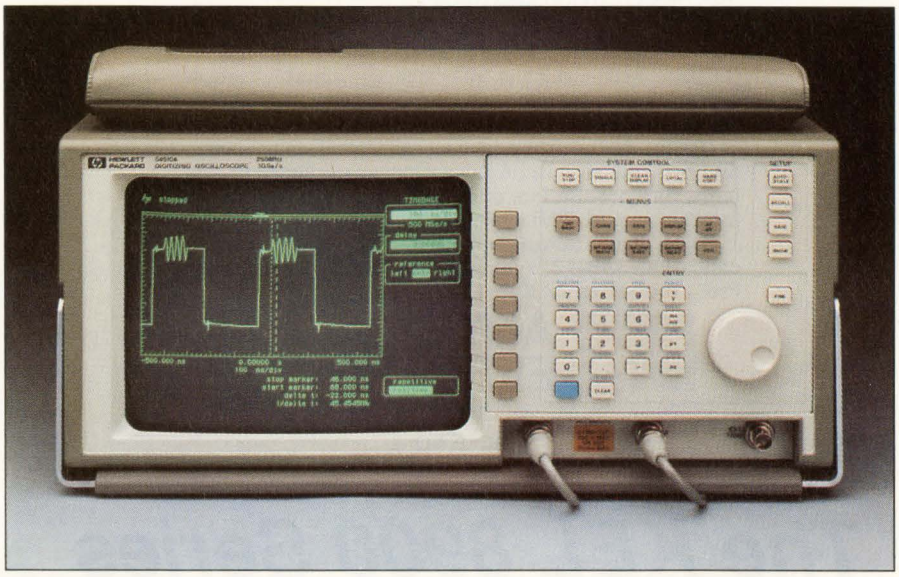
The HP54510A simultaneously samples two 250-MHz-bandwidth channels at 1G samples/sec. Although not the first DSO (digital storage oscilloscope) to offer this impressive, single-shot, real-time performance, at $10,950 the device is almost one-third the price of its competition. Despite its low price, this instrument does not compromise on single-shot performance or measurement accuracy.

The heart of this DSO is a hybrid consisting of two custom chips developed by the scope manufacturer. One chip is an 8-bit 1G-sample/sec flash A/D converter, and the other is an 8-bit × 8k-deep memory for storing the converter's output. The DSO uses two of these hybrids, one for each channel.

The manufacturer claims that the hybrid reduces memory space requirements by 98% and A/D and memory cost by more than 50% compared to its previous model, the HP54111D. These hybrids, combined with other custom chips for timebase and triggering, allow the manufacturer to put essentially the entire instrument on a single board.

Keeping instrument manufacturing costs down means little if performance has been compromised. This DSO offers single-shot measurement specifications such as voltage accuracy of 1.25% of full scale and timing accuracy on automatic measurements of 150 psec plus 0.005%.

You may be surprised to find that the scope manufacturer claims better timing accuracy than the 1-nsec time between samples. The DSO improves timing accuracy by limiting incoming bandwidth to 250 MHz, one-fourth the sample rate, before digitizing the signal. After digitizing the signal, the DSO is able to accurately reconstruct the bandwidth-limited signal and make measurements on the reconstructed signal. What matters on a DSO measuring single-shot events is not average values but variations between minimum and maximum values. In real-world single-shot applications, you don't get a chance to average—you only get one waveform to measure.



With a rate of 1G samples/sec, *the HP54510A DSO makes accurate measurements of single-shot events using waveform reconstruction.*

To demonstrate the capability of the filter-and-reconstruction method, the manufacturer made 1000 single-shot automatic measurements on a pulse from an accurately characterized pulse generator. The pulse had a width of 15.000 nsec, a period of 40.000 nsec, and a channel-to-channel delay of 9.000 nsec. Of these 1000 measurements, the minimum period value was 39.873 nsec, the maximum was 40.144 nsec, and the average was 40.001 nsec. Measurements of pulse width and delay exhibit similar accuracy. You might want to try the same single-shot measurements on competitive DSOs.

The DSO can also acquire successive single-shot waveforms at a rate of 400/sec. The instrument can store 290 single-shot acquisitions of 512 points each or use longer records and store fewer acquisitions. This capability is useful for pulse-and-response applications, such as sonar, where high resolution of the transmitted and received waveforms is needed despite relatively

EDN EDITORS' CHOICE

long time periods between events.

Although the DSO is designed for single-shot or real-time applications, it does operate in a repetitive-signal mode. In this mode, timing accuracy increases to 100 psec and bandwidth remains fixed at 250 MHz.

Like other members of the 54500 DSO family, this 22-lb portable scope performs 17 automatic pulse-parameter measurements, has an autoscale key for single keystroke setup, and features full IEEE-488 operation. Trigger control includes time-qualified pattern triggering, which can be used to find and trigger from glitches that are more than 1.75 nsec wide.

—Doug Conner

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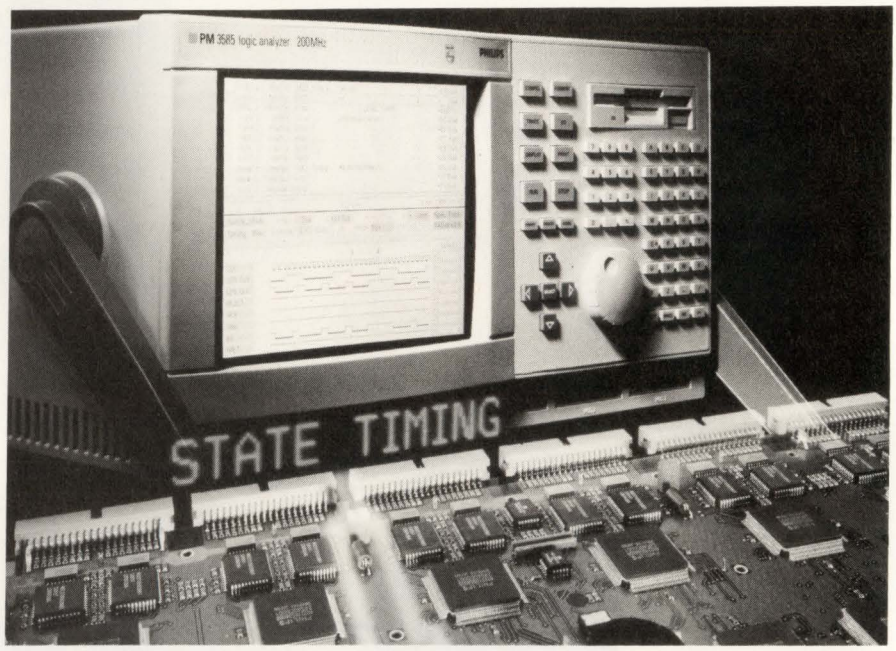
Logic analyzers let you use one probe set for timing and 50-MHz state analysis

Although there is probably no truly objective way to measure ease of use, Philips and Fluke are trying to establish one for logic analyzers. They use a stopwatch to clock the time you take to set up a few fairly standard tests using the pop-up menus of the PM3580 or PM3585 logic analyzer. Then they substitute a top-selling, comparably priced, competitive instrument and time the equivalent procedure. As you might expect, the Philips/Fluke products win handily. The reason for the dramatic difference lies both in the technology of the PM3580 and PM3585 and in the care the products' designers took to understand how engineers use logic analyzers.

You don't have to be a rocket scientist (or a logic designer) to realize that the analyzers' ability to do simultaneous state and timing analysis through a single set of probes saves the time you would need to connect a second probe set. Moreover, not having to put two probes on the pins of an IC in a high-density package (for example a quad flatpack) can save lots of frustration. Aside from that, using one set of probes spares the ICs from having to drive the capacitance of an extra set of probes. Especially in high-speed circuits, avoiding the extra capacitance eliminates a source of measurement errors. The capacitance of the analyzers' probes is 8 pF max.

It is highly likely that designers will use the new analyzers with ICs in high-density packages. The instruments' state-analysis speed is 50 MHz—fast enough for most reduced-instruction-set-computer processors, a class of high-speed devices with high pin counts. Moreover, the analyzers incorporate transitional timing, a feature that, in most applications, significantly extends the instruments' memory depth, and in this implementation, guarantees that memory depth is never sacrificed. You can equip either model with 32, 64, or 96 channels. The PM3585 performs timing analysis at 200 MHz and has 2k bits of memory per channel. The PM3580's timing-analysis speed is 100 MHz; it has 1k bits of memory per channel.



One set of probes *handles simultaneous 50-MHz state- and 100- or 200-MHz timing analysis with Philips/Fluke's PM3580 and PM3585 logic analyzers.*

The analyzers feature both alphabetic and numeric keypads. Therefore, you can type in information such as signal-name labels more easily than you can enter it on instruments that lack an alphabetic pad. (Designers of those instruments have invented some rather creative schemes to avoid the alphabetic pad. One such scheme was adapted from the user interface of a handheld label maker. On other units, you type on a Qwerty "keyboard" displayed on a touch-sensitive screen.)

As circuit speeds increase, digital designers are increasingly using logic analyzers and scopes together. These units don't overlook that requirement. The analyzers generate a TTL scope-trigger pulse on a BNC connector at any level of the trigger-sequence state machine. In addition, you can program any level to wait for an external trigger.

The PM3580/30 (32 channels) is $4250; the PM3585/90 (96 channels) is $10,950.—***Dan Strassberg***

John Fluke Mfg Co Inc, Box 9090, Everett, WA 98206. Phone (800) 443-5853, ext 77. FAX (206) 356-5116.

Circle No. 731

Philips Test and Measurement, Bldg TQIII-4 5600 MD, Eindenhoven, The Netherlands. Phone local office.

Circle No. 732

Z I L O G

Introducing Zilog's Smart Access Controller... Z180 intelligence and SCC communications together in one package.

Don't throw away your old software.

The Z80 family continues to be the most popular group of intelligent peripheral controllers on the market. With good reason. It's a tribute to our Superintegration™ technology and the performance of the controllers themselves. And since each new product in the family, like the SAC,™ is based on the same Z80/180 code you'll be able to migrate your existing software easily and effectively. We don't have to tell you how important that is.

Here's a list of the fast-growing family of Z80-based intelligent peripheral controllers. It's a list that's not likely to stop expanding any time soon... stay tuned.

INTELLIGENT PERIPHERAL CONTROLLERS

	System				Serial			Timers		Parallel	
	CPU	OSC	MMU	RAM	DMA	USART	UART	C/S	CTC	C/T	PIA	PIO
Z84C01	✓	✓							✓		✓	✓
Z84C50	✓	✓		✓		✓						
Z84C90		✓					✓	✓		✓		
Z80180	✓	✓	✓		✓		✓			✓		
Z80280	✓	✓	✓	✓	✓	✓				✓		✓
Z84013/C13	✓	✓				✓				✓	✓	
Z84015/C15	✓	✓								✓	✓	
Z84011/C11	✓	✓								✓	✓	✓
Z80181	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓

The Z80181™ SAC™ Controller is the Smart Access Controller™ that combines two powerful standards. You get Zilog's industry standard SCC™ controller for datacom connectivity together with the popular Z180 CMOS controller. And all that utility comes with the user-friendly Z80® code CPU compatible software.

High integration. High performance. Smart communicator.

The Superintegration™ SAC Controller packs the popular high performance Z180 architecture into a new cell suitable for many datacom and peripheral control applications. You get the SCC single-channel communication cell with two additional UARTS, a 4 x 8-bit counter timer (CTC) *and* onboard 16-bit I/O. The SAC Controller runs at 10 MHz and drives fast serial communications at 2.5 Mbits/sec. With the reduced 3 cycles per instruction, the SAC Controller gives you Z80 code performance 25% faster. That makes the SAC Controller the highest performance, low power embedded controller around.

The best cost/performance of any embedded controller out there.

Whatever your application — data communications, modems, FAXs, printers, terminals, industrial controls — the SAC Controller combination gives you the best cost/performance ratio. Everything you need for your system is on the chip. The SAC Controller brings you all the advantages of Zilog's Superintegration technology. Off-the-shelf and backed by our solid reputation for quality and reliability.

To find out more about the SAC Controller, or any of Zilog's rapidly growing family of Superintegration products, contact your local Zilog sales office or your authorized distributor today. Zilog, Inc., 210 Hacienda Ave., Campbell, CA 95008, (408) 370-8000.

Right product. Right price. Right away.

ZiLOG

ZILOG SALES OFFICES: CA (408) 370-8120, (714) 838-7800, (818) 707-2160, **CO** (303) 494-2905, **FL** (813) 585-2533, **GA** (404) 448-9370, **IL** (312) 517-8080, **NH** (603) 888-8590, **MN** (612) 831-7611, **NJ** (201) 382-5700, **OH** (216) 447-1480, **PA** (215) 653-0230, **TX** (214) 987-9987, **WA** (206) 523-3591, **CANADA** Toronto (416) 673-0634, **UNITED KINGDOM** Maidenhead (44) (628) 39200, **W. GERMANY** Munich (49) (89) 672045, **JAPAN** Tokyo (81) (3) 587-0528, **HONG KONG** Kowloon (852) (3) 723-8979, **KOREA** (82) (2) 552-5401, **TAIWAN** (886) (2) 741-3125, **SINGAPORE** 65-235 7155, **DISTRIBUTORS: U.S.** Anthem Electronics, Hall-Mark Electronics, JAN Devices, Inc., Schweber Electronics, Vargas Electronics, Western Microtechnology, **CANADA** Future Electronics, SEMAD, **LATIN AMERICA** Argentina — Yel.-(1) 46-2211, Brazil — Digibyte (011) 581-1945, Semiconductores Profesionales (5) 536-1312.

Rewritable 133M-byte optical drive features 30-msec average seek time

A low-mass read-write head on the Model RMD-5100-S rewritable optical drive results in an average seek time of 30 msec—competitive with medium-performance magnetic disk drives. The unit stores 133M bytes of data on 3½-in. disks and features a 30,000-hr MTBF. The drive includes a SCSI (Small Computer System Interface) controller and is compatible with the SCSI common command set.

The drive uses ANSI-standard 3½-in. rewritable optical disk cartridges. Furthermore, the unit fits in the industry-standard half-height 5¼-in. peripheral mounting slot commonly found on personal computers and workstations. The drive includes a 1-year warranty and features data reliability of less than one hard error in 10^{12} bits read, one soft error in 10^{10} bits read, and one seek error in 10^{6} seeks. A combination of CRC and a long-distance ECC ensures data reliability.

The optical drive produces a sustained transfer rate of 512k bytes/sec. An onboard buffer, however, allows the SCSI controller to perform burst transfers at 1.5M bytes/sec in asynchronous mode and 3M bytes/sec in synchronous mode. The SCSI controller also includes a jumper block that you can use to set the SCSI ID.

The 30-msec average seek time makes the device competitive with magnetic drives. Furthermore, the drive includes a scanning/short seek ability that makes data anywhere within a 128-track band available within 7 msec. A 128k-byte read-ahead cache reduces seek time to the 1-msec range on cache hits. Track-to-track seek time is 1 msec and maximum seek time is 60 msec. The drive spins disks at 2400 rpm, and therefore features an average rotational latency of 12.5 msec.

Compatibility with the 512-byte sector format proposed by ANSI as an interchange standard results in a cartridge capacity of 128M bytes. The drive also supports the 1024-byte sector format, proposed as an option by ANSI, to achieve maximum capacity of 133M bytes on a cartridge. The drive stores data on 10000 tracks at a density of 1.6 μm.

The RMD-5100-S weighs 4.41 lbs and dissipates 17W of power typ. It can operate over a temperature range of 10 to 45°C and a humidity range of 10 to 80%. It costs $2425 and samples are available.

—Maury Wright

Mass Optical Storage Technologies, a Nakamichi Co, 11205 Knott Ave, Cypress, CA 90630. Phone (714) 898-9400.

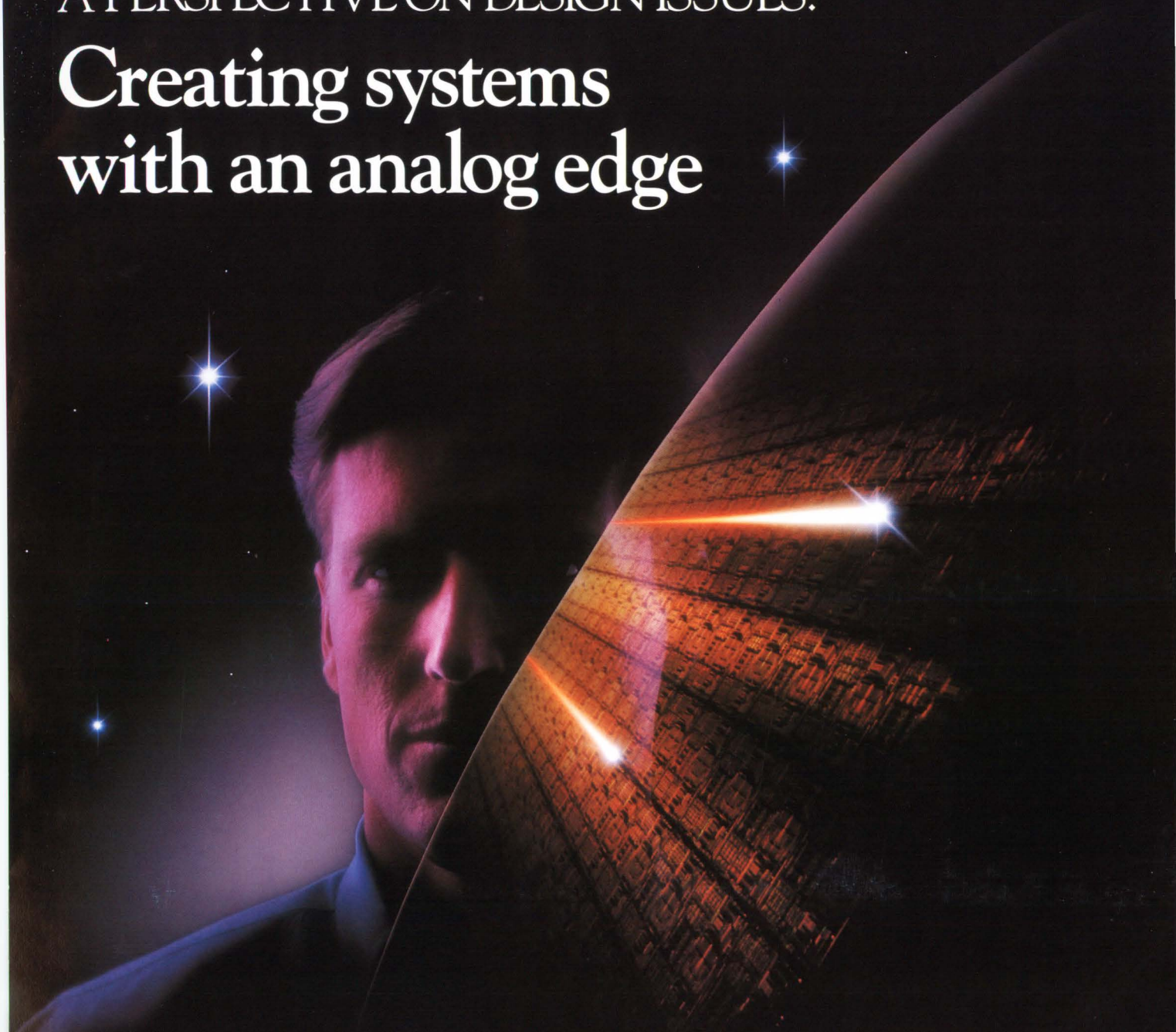
Circle No. 734

The 30-msec average seek time *of the RMD-5100-S optical drive makes the unit competitive with magnetic drives. Furthermore, the 133M-byte unit employs ANSI-standard 3½-in. media and fits in a standard half-height 5¼-in. drive slot.*

TEXAS INSTRUMENTS

A PERSPECTIVE ON DESIGN ISSUES:

Creating systems with an analog edge



IN THE ERA OF

MegaChip TECHNOLOGIES

Advanced Linear can help you raise system performance levels.

A leadership family of analog circuits from Texas Instruments is helping designers meet difficult design challenges.

The evidence is strong. Throughout the design community, systems using the new breed of Advanced Linear functions from Texas Instruments are achieving the keener performance edges that can spell marketplace success.

TI's new analog devices are enabling design engineers to link digital brains to analog worlds more effectively and efficiently than ever before. Some offer new standards of accuracy or speed while others are highly integrated devices combining analog and digital functions on a single chip. The result is superior system performance and design flexibility.

These Advanced Linear functions are the result of leadership process technologies that we at TI firmly believe are the key to the advanced analog devices your future applications will demand.

Intelligent power for automobiles

Designers in the automotive industry face a tough challenge: Handle high reverse voltages and achieve rapid load turnoff while providing fault protection, detection, and reporting and efficient load management. To provide the needed intelligent power devices, we developed one of our newest process technologies, Multi-EPI Bipolar. It is unique because it can combine rugged power transistors with intelligent control functions.

The resulting circuits are now providing reliable, cost-efficient control of solenoids and valves in such automotive applications as antiskid braking systems, electronic transmission controls, and active suspension systems.

Other industry segments are also benefiting from TI's Advanced Linear process technologies. Here are a few of the winning designs to which we have helped add an analog edge:

Toledo Scale

Challenge: Improve the accuracy of point-of-purchase scales by eliminating drift over time and temperature.
Solution: The TI TLC2654 Chopper op amp. Our Advanced LinCMOS™ process makes possible chopping frequencies as high as 10 kHz, reducing noise to the lowest in the industry.

Pulsecom

Challenge: Develop a linecard capable of driving low-impedance loads with greater precision.
Solution: Our TLE206X family of JFET-input, low-power, precision operational amplifiers. These devices offer outstanding output drive capability, low power consumption, excellent dc precision, and wide bandwidth. Fabricated in our Excalibur process, they remain stable over time and temperature.

Leitch Video

Challenge: Design a compact, cost-efficient direct broadcast satellite TV descrambler for consumer use.
Solution: TI's TLC5602 8-bit Video DAC. Our LinEPIC™ process combines one-micron CMOS with precision analog to satisfy the demands of the application for video speeds and low-power operation.

U.S. Robotics

Challenge: Build a modem for high-speed data transmission between computers; allow flexible operation and minimize data errors.
Solution: Our TLC32040 Analog Interface Circuit (AIC). A product of our Advanced LinCMOS process, the AIC combines programmable filtering, equalization, and 14-bit A/D and D/A converters with such digital functions as control circuitry, program registers, and a DSP interface.

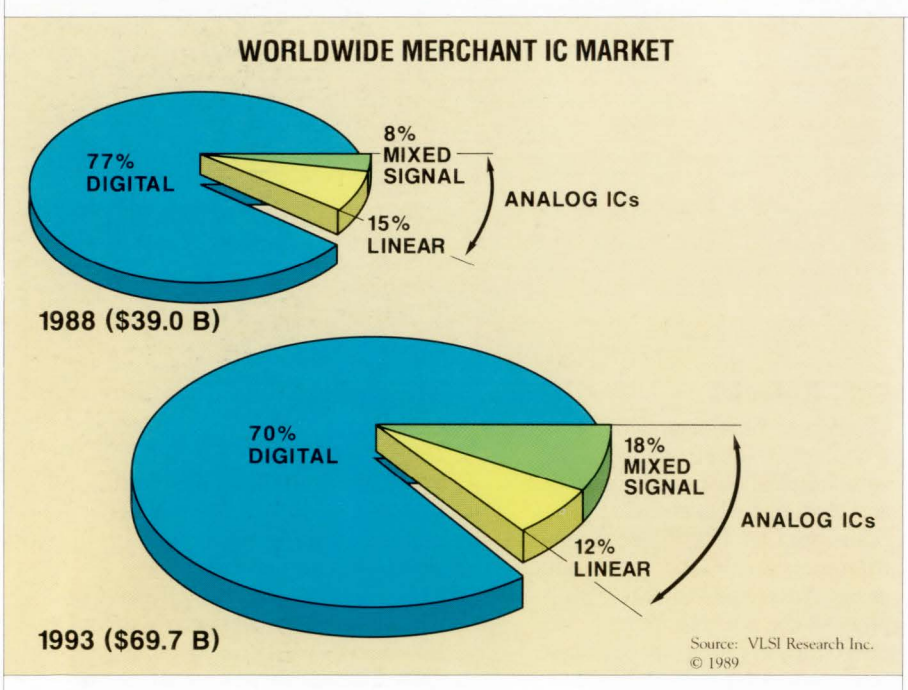
Xerox

Challenge: Cut component count and cost of copier systems while boosting reliability.
Solution: Our TPIC2406, a top-performance peripheral driver in a standard DIP package that is capable of driving heavy loads. It is fabricated using our Power BIDFET™ process which permits greater circuit density and incorporates CMOS technology for low total power dissipation.

Mr. Coffee

Challenge: Design an intelligent coffee maker that brews faster, maintains optimum temperature, shuts off automatically, and has a built-in cleaning cycle.
Solution: Our LinASIC™/LinBiCMOS™ capability permits us to combine both analog and digital library cells with custom analog cells. This results in cost-efficient integration of temperature monitoring, timing, and high-current outputs on a single control chip.

All of these examples point to one conclusion: TI's Advanced Linear functions are adding an analog edge to many system designs. They are contributing significantly to the enhanced system performance that marks a market winner.



Helping you implement your designs in a changing world.

An increasing share of the total analog market is being captured by mixed-signal devices. As they gain more widespread acceptance, they are driving the expansion of the overall analog market (*see above*).

Changes such as this are the order of the day in the IC marketplace. Texas Instruments continues to provide not only the high-performance circuits you need but also the depth of experience, support, and service fundamental to successful completion of your designs.

Experience: Building on three decades in ICs

We at TI can successfully meet your requirements for mixed-signal devices because we have acquired the necessary knowledge from 30 years of experience in developing both analog and digital functions. We have also drawn upon our digital ASIC strengths in developing our LinASIC capabilities.

Support: Speeding our chips to you

The faster we move new products through our design cycles, the faster you can get through yours. We employ a wide variety of design-automation tools and sophisticated software to speed our development process.

Service: Providing a surety of supply

However advanced our circuits may be, they are of little value if they are inaccessible to you. TI operates on the principle of global coverage, local service. We manufacture semiconductors in 13 countries and operate support centers in 22. We have product and applications specialists, designers, and technicians around the world. They are linked by one of the world's largest privately owned communications networks so that we can bring you our best — circuits and support — from wherever they may be to wherever you are.

Keeping our communications open

The relationship between you as customer and us as vendor is vital: You are our chief source for firsthand information that can help guide us in developing the circuits you will need for your future designs. We at TI welcome your comments and your suggestions.

TI's Leadership Analog Processing Technologies

LinBiCMOS — Combines Advanced LinCMOS, digital ASIC CMOS, and up to 30-V bipolar technologies to allow the integration of digital and analog standard cells and handcrafted analog components on a monolithic chip.

LinEPIC — One-micron CMOS double-level metal, double-level polysilicon technology, which adds highly integrated, high-speed analog devices to the high-performance digital EPIC process.

Advanced LinCMOS — An N-well, silicon-gate, double-level polysilicon process featuring improved resistor and capacitor structures and having three-micron minimum feature sizes.

Power BIDFET — Merges standard linear bipolar, CMOS, and DMOS processes and allows integration of digital control circuitry and high-power outputs on one chip. Primarily used for circuits handling more than 100 V at currents up to 10 A.

Multi-EPI Bipolar — A very cost-effective technology that utilizes multiple epitaxial layers instead of multiple diffusion steps to reduce mask steps by more than 40%. Used to produce intelligent power devices that can handle loads as high as 20 A and voltages in excess of 100 V.

Excalibur — A true, single-level poly, single-level metal, junction-isolated, complementary bipolar process developed for high-speed, high-precision analog circuits providing the most stable op amp performance available today.

If you would like a more detailed explanation of our Advanced Linear process technologies, please call **1-800-336-5236, ext. 3423**. Ask for a copy of our *Advanced Linear Circuits* brochure.

TEXAS INSTRUMENTS

End the connector compromise...

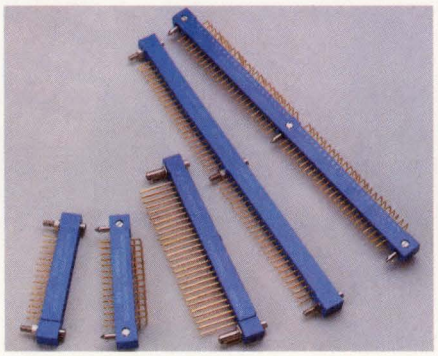
1. 1-700 LOW INSERTION FORCE CONTACTS
2. QUALIFIED TO D55302
3. SIGNAL TO 500 AMP POWER CONTACT RATINGS

...in PC-board connections.

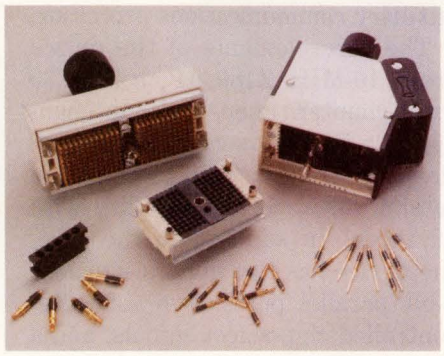
Only Hypertronics ends the compromise in printed circuit board connectors for electronic equipment. . . by replacing unreliable connections, and their field service problems, with Low Insertion Force (LIF) high-cycle reliability. Discrete Hypertac® contacts and multi-pin connectors eliminate the need for expensive and space-consuming jacking and camming mechanisms.

The unique wiping action of each Hypertronics connector maintains electrical continuity under extremes of shock and vibration (tested to 2 nanoseconds) with insertion forces as low as ½ oz.

Now you can have it all. . . in signal/power connections requiring up to 700 contacts. End the connector compromise by calling 1-800-225-9228, toll free.



KA Series: *17-490 Contacts with D55302-Listed Qualified Models.*

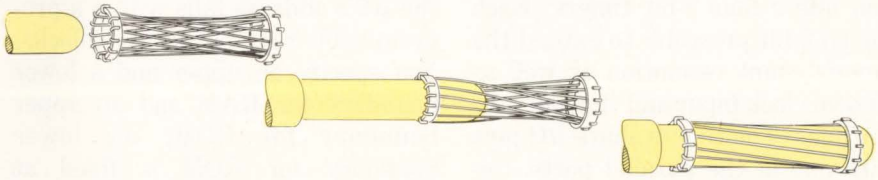


N Series: *70-700 Position Connectors with Ratings to 9 Amps.*

KG Series: *22-90 Position Board Stacking for .240 or .480 Heights Between Boards.*

Y Series: *3-500 Amp Discrete Pins and Mating Sockets.*

HYPERTAC®: Inserting pin into hyperboloid sleeve.



HYPERTRONICS CORPORATION

"New Horizons in Connectors"

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Controller combines multiprotocol serial communications with μP

The Z80181 Smart Access Controller (SAC) combines the features of three ICs with additional I/O ports. The resulting collage is an intelligent peripheral controller suitable for stand-alone operation or as an auxiliary communications processor.

The core elements of the device are a 10-MHz Z180 μP, a Z84C30 quad counter/timer, and one channel of a Z85C30 serial communications controller. The combination retains software compatibility with all three. In addition to the core, the device has two general-purpose 8-bit parallel ports, two software-controlled chip-select signals, and a clock oscillator.

Combining the equivalent of several LSI devices, *the Z80181 handles a variety of serial-communications tasks.*

The Z180 μP, a derivative of the Z80, augments the Z80 instruction set by seven, including a multiply instruction. Built into the μP are two asynchronous receiver/transmitters (UARTs), a clocked serial I/O port, two 16-bit timers, two DMA channels, and a programmable dynamic-RAM refresh circuit. The UARTs include baud-rate generators and modem control signals. An on-chip memory-management unit extends the Z180's address space to 1M byte, and a programmable wait-state generator simplifies your use of slow memory.

The Z84C30 counter/timer section offers four 8-bit timers. Each has an 8-bit prescaler to extend the timer's count resolution as well as its own clock input and timeout output lines. The timers share I/O pins with one of the parallel ports. Selecting the timer's I/O overrides the parallel port.

The Z85C30 serial communications controller channel handles both synchronous and asynchronous communications protocols. Supported protocols include bit- and byte-oriented synchronous and HDLC (high-level data link control). The device can handle data rates to 2.5M bps.

The parallel ports are bidirectional, and each I/O pin's direction is individually programmable. Port 1, which shares I/O pins with the timers, offers Schmitt-trigger input lines.

Two chip-select signals are available to simplify connection to external memory, one for RAM and one for ROM. Each signal asserts when the μP's address falls within a programmable range of 4k-byte blocks. You specify an upper and a lower boundary for RAM and an upper boundary for ROM; the lower boundary for ROM is fixed at 00000x. The ROM chip-select takes priority over the RAM chip-select if the ranges overlap, preventing the RAM chip-select signal from asserting.

With so many peripheral functions internal to a device, software debugging could be a real challenge. To assist your debugging efforts, the device offers a ROM-emulation mode. You can program the device to drive its data lines when reading from the on-chip peripheral registers, allowing a ROM emulator or logic analyzer to monitor internal transactions. In normal operation, the device's data lines would exhibit high impedance during internal activity.

The device operates at 10 MHz using either an external clock signal or a 20-MHz crystal. Both the serial communications controller and the clock/timer section connect internally to the system clock. The device comes in a 100-pin quad flatpack and costs $22.00 (1000).

—Richard A Quinnell

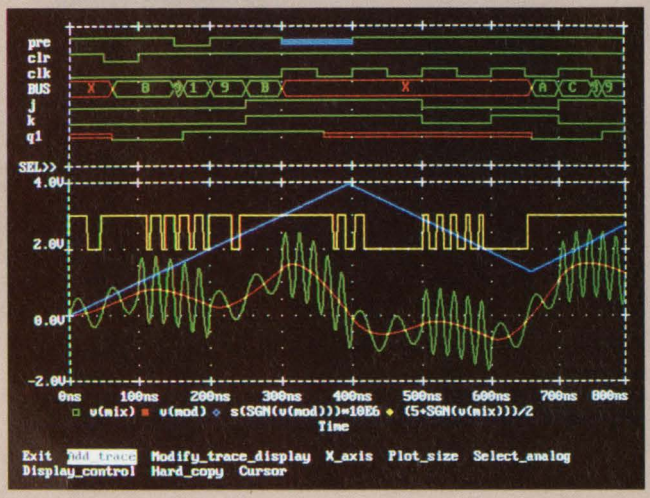
Zilog Inc, 210 Hacienda Ave, Campbell, CA 95008. Phone (408) 370-8000. FAX (408) 370-8027.

Circle No. 733

PSpice

MicroSim Corporation

The Standard for Circuit Simulation



Analog and digital waveforms with common time axis

MicroSim is the leader in Mixed Analog/Digital Simulation Technology

Two years ago, MicroSim introduced the technology for simulating mixed analog/digital circuits. Now, this capability is available in the Digital Simulation extension for PSpice. It does true mixed-mode simulation of circuits – including feedback loops between analog and digital sections.

PSpice's Digital Simulation option performs mixed analog and digital simulations. There are no performance compromises–digital components are processed at logic simulation speeds and analog waveforms are calculated with PSpice's usual precision. Analog and digital waveforms may be displayed together, with a common time axis (see photograph for an example).

Digital Simulation removes one of the greatest constraints on circuit simulation: the dichotomy between analog and digital.

PSpice with the Digital Simulation option:

- Is Easy to Use – In the circuit description, digital devices follow the same syntax as other PSpice devices. Simulating a mixed circuit is no different from running a transient analysis on an analog circuit.
- Has Efficient Algorithms – To get reasonable speed–and to allow reasonably large sections of digital circuitry–the core of theDigital Simulation option is an event-driven logic processing algorithm. It computes logic states and propagation delays very quickly.
- Includes an Extensive Library – The Digital Simulation option includes libraries for most TTL components. These include gates, flip-flops, latches, registers, and counters. Each component, in turn, includes models for many logic families including TTL, LS, ALS, H, F, L, S, AS, HC, HCT, and 4000 series CMOS. The component models describe not only the functionality of the device but also all its propagation delays.

Each copy of PSpice comes with our extensive product support. Our technical staff has over 100 years of experience of CAD/CAE, and our software is supported by the engineers who wrote it.

For further information about the Digital Simulation option or any other PSpice product, please call us **toll free** at (800) 826-8603 or, in California, (714) 770-3022. Find out for yourself why PSpice has sold more programs than all other SPICE-type programs combined and has become the de facto standard for circuit simulation.

20 Fairbanks • Irvine, CA 92718 USA • Telex 265154 SPICE UR

CIRCLE NO. 59

Four-channel arbitrary waveform generator samples at 2 MHz with 16-bit precision

The 4-channel Model 2201A arbitrary waveform generator includes three phase-coherent channels and a channel for a built-in noise generator. The unit can generate standard waveforms such as sine, triangular, and square waves and samples at 2 MHz; it features 16-bit precision. You can create waveforms with a mouse or from front-panel controls for the three phase-coherent channels.

The generator has 64k words of battery-backed static RAM for each of the three main output channels. You can program the phase difference between the three outputs with a resolution of 0.0055°. To create complex waveforms, you can set up the instrument to sum the output of channel 1 with channels 2 and 3. You can also concatenate the three outputs to produce waveforms with as many as 196,608 points.

The pseudorandom noise channel generates a signal with 150-kHz maximum bandwidth, and provides a noise sequence length of greater than one billion counts. The noise source features a maximum amplitude of 2.58V rms and a dynamic range of > -80 dB. You can set the instrument to output the noise signal or to superimpose it in the channel 1 output.

The unit supports waveform editing and creation in three ways. You can use front-panel controls to modify amplitudes of signal vertexes, and place and move vertexes. You can use a mouse, included with the instrument, to create and edit waveforms. The instrument supports editing functions such as move, normalize, truncate, resize, extend, shrink, zoom, and pin with the mouse. You need an external monitor or oscilloscope to perform waveform editing from the front panel or with the mouse. Finally, you can use software to create waveforms on an IBM-compatible personal computer and download the waveforms to the 2201A.

Mouse- and front-panel-based *waveform editing capabilities allow you to create complex waveforms for the Model 2201A without the help of an external computer. You can store the waveforms in removable credit-card-size memory modules that include 32k bytes of battery-backed static RAM.*

You can store waveforms in the static-RAM arrays dedicated to each channel. The unit includes an interface to credit-card-size, removable static-RAM memory modules. The modules feature 32k bytes of memory and a battery that makes them nonvolatile. You can use the cards to store libraries of waveforms. If you have sufficient volume requirements to support the programming process, you can also buy the modules with ROM.

Specs for channels 1, 2, and 3 include a horizontal and vertical resolution of 65,536 points. The unit features 10V p-p, square-wave rise and fall times of <150 nsec tested with 50Ω termination. You can also selectively apply a built-in analog 700-kHz, ninth-order Butterworth lowpass filter to the output.

The Model 2201A provides both IEEE-488 and RS-232C interfaces as standard features. The tabletop unit weighs 32 lbs and measures $17 \times 5\frac{1}{4} \times 16$ in.; it can also be rackmounted. The unit, including the mouse and one memory card, costs $9985.—***Maury Wright***

Pragmatic Instruments Inc, 7313 Carroll Rd, San Diego, CA 92121. Phone (619) 271-6770. FAX (619) 271-9567.

Circle No. 735

Faster.

ADSP-2101 – Talk about fast – this DSP microcomputer executes a 1024-point FFT in only 2.26 ms. That's faster than other DSPs that operate at almost twice the clock rate. And since our entire ADSP-2100 family is code compatible, your code will run fast on all of our DSPs.

AD9617 – The fastest slewing and settling op amp around slews at 1400 V/μs and settles to 0.02% in just 14 ns. And with a closed loop bandwidth of 200 MHz and harmonic distortion at 20 MHz of −59 dBc (max), it makes driving A/D converters easier than ever.

AD9712 – The only 12-bit, 100 MHz D/A converter on the market. Ideal for high-speed video and direct digital synthesis, its low glitch and low harmonics combine to deliver a spectrally pure output waveform.

AD9060 & AD671 – The fastest 10-bit and 12-bit monolithic A/D converters, respectively. The AD9060 guarantees encode rates up to 75 MSPS for unparalleled dynamic performance. The AD671 is twice as fast as any other 12-bit monolithic, converting in under 0.5 μs, thanks to our high-speed mixed-signal ABCMOS process.

Our Spectrum CAD Tool is 100 times faster than traditional SPICE programs, so it makes quick work of mixed-signal ASIC design cycle time.

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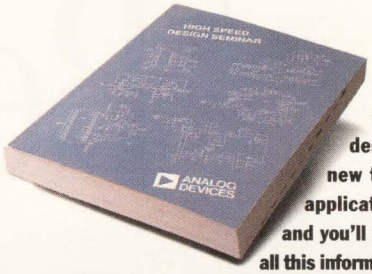
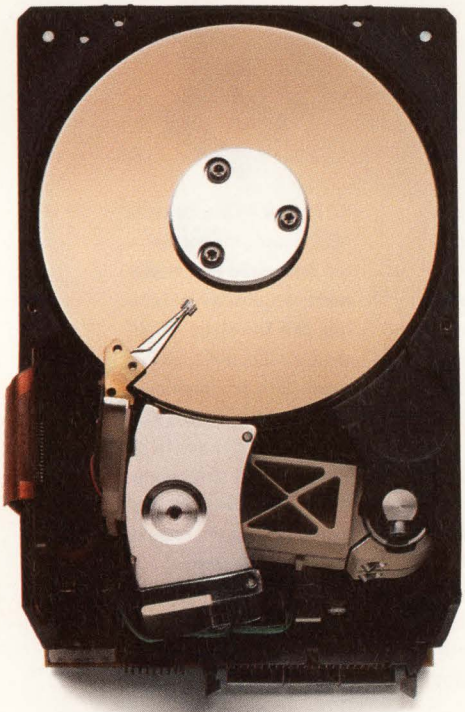
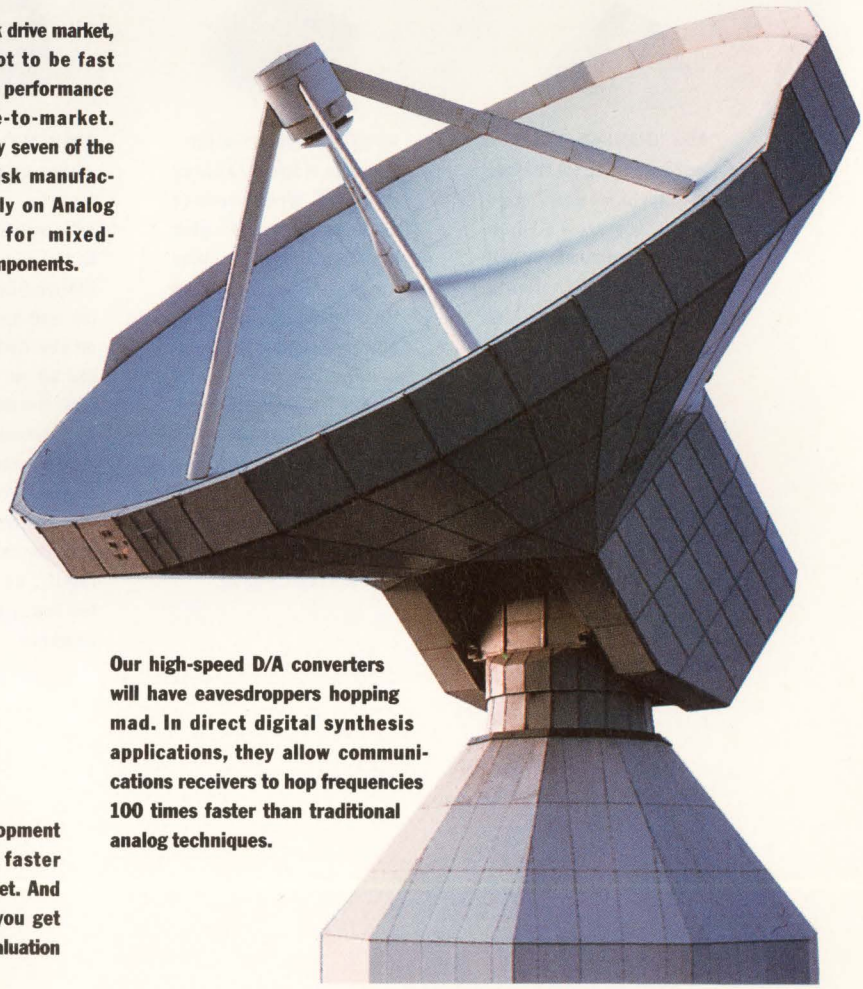


Tap into 25 years of experience at our high-speed and mixed-signal design seminars. You'll learn new techniques that'll get your applications to work more quickly, and you'll get design manuals that put all this information right at your fingertips.



In the disk drive market, you've got to be fast – in both performance and time-to-market. That's why seven of the top 10 disk manufacturers rely on Analog Devices for mixed-signal components.



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Faster development time means faster time-to-market. And that's what you get with our EZ-KIT, a complete design tool with a demonstration/evaluation board, DSP textbooks, and powerful, yet easy-to-use software.

Today, Analog Devices offers more high-performance mixed-signal components than anyone else. And we get them to you fast. So if you want mixed-signal ICs that'll help you design faster performing products, from a company that'll help you get your product to market faster, call us at 1-800-262-5643.

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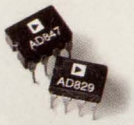
CIRCLE NO. 61

Better.



AD820/AD840 Series – If you're looking for the best in high-speed op amps, here they are – a whole family of components with the right combination of features to deliver high speed, precision, low noise, low input bias currents, low offset voltage and low drift performance. Our Complementary Bipolar process delivers gain-bandwidth products in excess of 750 MHz and slew rates in excess of 2000 V/μs.

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ADSP-2111 – Better integration on the best architecture in the industry. Adds an 8/16-bit host port to the two serial ports, timer, hardware companding and memory already on the ADSP-2101. And like all our DSPs, it's got fast, flexible arithmetic, wide dynamic range and a single cycle fetch of two operands (on- or off-chip). Plus it's code-compatible with the rest of our DSP family, so what's written today will be useful tomorrow.

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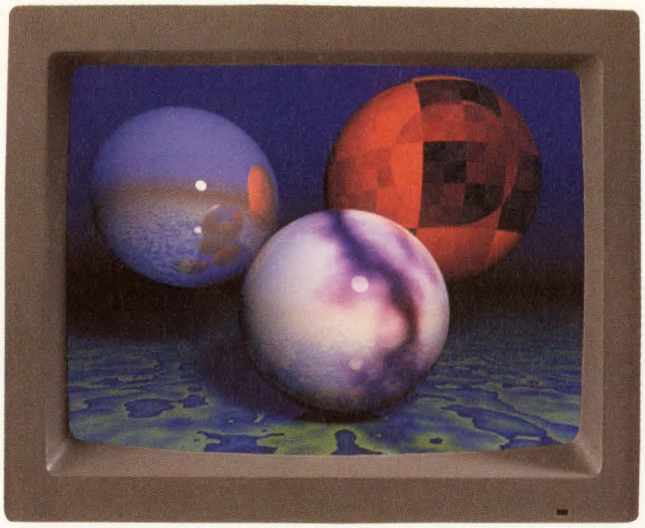
We're your best source for linear, digital and mixed-signal information. Annually, we publish over 20 books and newsletters, and scores of applications notes. And our *Analog Dialogue* enjoys a worldwide readership of over 100,000 design engineers.

'Try, try again' is a costly way for manufacturers to find the best design solution. So to help our customers find answers to tricky problems the first time around, technical application engineers are just a phone call away. In some instances, they're even located right on the customer's premises.



Picture this – a PC monitor that offers the same color and clarity as a high-end engineering workstation costing as much as 20 times more. Our pin-compatible RAM-DAC is literally redefining the low end of the PC monitor market.

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People are hearing a lot better, thanks to our fully integrated baseband processing subsystem, which controls, conditions and converts I and Q channels in both the data transmit and receive paths.

Today, Analog Devices offers a better line of high-performance mixed-signal components than anyone else. And no one has a better record for reliability, or more experience in analog, DSP and mixed-signal ICs. If you want mixed-signal components that'll help you design better products, the best thing to do is to call us at 1-800-262-5643.

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ADSP-2105—High performance DSP at an incredibly low price. So low, in fact, you can now consider DSP in a host of new applications. And since it's pin-compatible with the ADSP-2101, and code-compatible with all of our other DSP processors, upgrading is easy and inexpensive.

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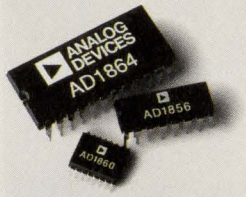

SOUNDPORT DACs—We've made these DACs cost-efficient by making them complete with output amplifier, reference and digital logic interface. Perfect for high-fidelity digital audio and multimedia applications, these mixed-signal ICs achieve SNRs as high as 108 dB and THDs as low as 0.0025%.

AD22001—One way to make a car less expensive is to make it with less parts. This component replaces a whole board of discrete analog and digital circuitry. It continuously monitors up to five automotive bulbs or indicators, along with the associated in-line fuse, and provides a digital status output.

More gadgets for less money, and make it work better—that's the only way to survive in consumer electronics, the most competitive market there is. That's why three of the top five Japanese electronics firms rely on us to meet their mixed-signal needs in applications ranging from CD players to video cameras.

We've got the phone lines buzzing. Via our CMOS and Bipolar processes, we're helping modem makers turn out products that cost less yet perform better. We got the call because we have the broadest portfolio of process technology for signal processing. A portfolio that includes not only CMOS and Bipolar, but BiCMOS, Complementary Bipolar, Flash and many others.

We're far from your local component boutique. Over half of our $540 million in revenues comes from international sales. And with manufacturing and stocking facilities on just about every continent, getting products to you quickly is a snap. Plus multiple manufacturing facilities allow us to take advantage of the right talent and processes for the job at hand.

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Automakers certainly understand that manufacturing efficiency is a critical key to lowering production costs. That's why we've developed high-performance ICs for several car companies around the world, as well as companies making DAT equipment, disk drives, digital mobile phones, modems, and HDTV.

Today, Analog Devices offers more cost-effective solutions to your high-performance mixed-signal needs than anyone else. Solutions that are surprisingly affordable, whether they're available off the shelf or developed for a specific application. To find out more about how we can help you develop products more efficiently, or for a free copy of our recent Mixed-Signal Technology white paper, call us at 1-800-262-5643.

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Futurebus+ is moving closer and closer to reality. When the bus's specifications are finalized, expect manufacturers to support the open-bus architecture immediately. (Photo courtesy Motorola Computer Group)

Futurebus+

Commercial implementations of the Futurebus+ are still probably a year away, yet the release of draft copies of the Futurebus+ documents has created considerable interest in this advanced, open-bus architecture. At last February's Buscon/90-West Conference in Long Beach, CA, the IEEE P896 committee, better known as the Futurebus committee, rolled out a series of documents for IEEE membership approval. The most notable of these documents are P896.1 and P896.2. P896.1 defines Futurebus+'s logical-layer specifications, bus-line definitions, bus-arbitration methods, the parallel protocol for data transactions, control and status registers for bus management, cache coherency, and message passing. Document P896.2 defines Futurebus+'s hardware physical layer and profile specifications.

The documents reflect the committee's multiyear effort to arrive at an open-bus standard that will support multiple generations of μPs and technologies without becoming obsolete (see **box**, "The long history of Futurebus+"). The bus has already been endorsed by the US Navy for mission-critical computers, and a large number of companies, including DEC, Sun Microsystems, Unisys, Motorola, and Force Computers, are developing Futurebus+ products pending the finalization of the specifications.

Futurebus+ is an evolved version of many earlier buses that has added features that supposedly make it independent of changing technologies. For example, the specification allows modules with big endian or little endian data representations to communicate with each other. These representations reflect the different byte-ordering conventions for μPs from different vendors. The specification forces bytes to be swapped before a transaction is possible.

A little endian representation reserves the least significant address byte of a register for the least significant data byte of a word; the big endian representation reserves the most significant address byte of a register for the least significant data byte of a word. For the module to automatically swap or order the bytes during a transaction, each module on the Futurebus+ must contain a bit in a status register that indicates whether the module uses a big or little endian representation.

Another feature of the bus is global addressing. Each logical bus module on the Futurebus+ gets assigned a unique geographical ad-

John A Gallant,
Associate Editor

For some time now Futurebus+ touters have said that the architecture will lead us into the computing promised land. Though there is still work to be done, the journey may finally be ready to begin.

Each module on the Futurebus+ gets assigned a unique geographical address, which is hard-wired into each slot on the backplane.

dress, which is hard-wired into each slot of the backplane. When a board plugs into a slot it senses the 5-bit number on lines GA[4..0]* to determine which slot it resides in.

The Futurebus+ arbitration process operates in parallel with data transfers on the bus. Each module in the system has a unique arbitration number that is used in a parallel-contention algorithm during competition to become the bus master. When two or more modules compete for the bus, the module with the largest arbitration number wins. The process has two modes of arbitration: unrestricted mode, which has 14-bit arbitration numbers; and restricted mode, which has 8-bit arbitration numbers. Because the arbitration cycle uses an 8-bit competition number, the unrestricted mode requires two arbitration cycles. The unrestricted mode provides eight priority bits, whereas the restricted mode is limited to two bits.

The module with the highest arbitration number at the end of arbitration competition becomes the master-

The long history of Futurebus+

The history of Futurebus+'s development follows a meandering course. It started with the IEEE's recognition of the P896 committee in 1979. The committee was set up to arrive at a bus standard that would accommodate new 32-bit processors such as Motorola's 68000 μP, which has a 16-bit data path and a 32-bit register set that requires a 32-bit backplane. The committee's efforts produced the Versabus, which became the basis for the VMEbus. After a few years of evaluation, the committee set a new goal—to develop a "processor-independent 32-bit bus" to handle all future μP systems. In 1982, the group became known as the Futurebus committee.

The Futurebus required arbitration for multiple masters and fast data-transfer speeds to handle faster μPs. In addition, the committee realized that a Futurebus backplane was going to require cache-coherency protocols that would allow multiple processors access to global data on the bus. It also considered how to use bus repeaters between multiple buses. Although the committee didn't complete the work in these areas, it published a partial specification in 1986 known as the IEEE STD 896.1 document, which defined hardware and timing.

RISC μPs influence directions

Subsequently, Motorola developed the 88000 RISC μP, which has a cache architecture and coherency protocols similar to the IEEE P896 committee's proposals. In 1988 an internal debate occurred within the VMEbus Trade Association (VITA) as to whether Futurebus could become VMEbus II to accommodate the new RISC processor. Instead of endorsing Futurebus, VITA established the Next Generation Architecture (NGA) subcommittee to investigate the future for VMEbus.

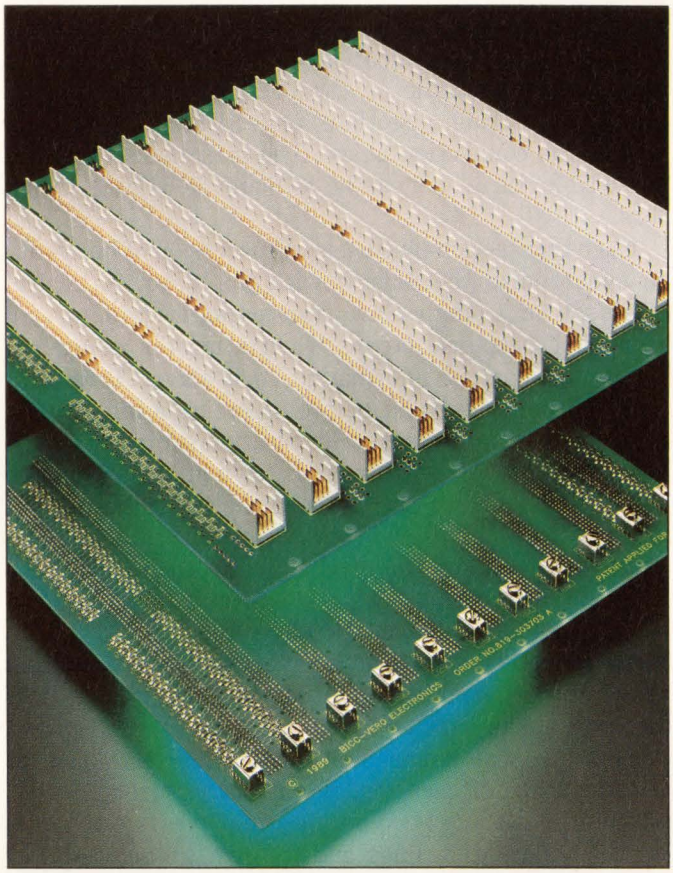
Meanwhile, the US Navy evaluated six 32-bit buses for mission-critical computers, and Futurebus came out the winner. However, because there was no industry support for Futurebus, the Navy was considering using Multibus II as an interim backplane standard until the mid 1990s. In December 1988, however, the IEEE Rugged Bus committee voted to merge with the Futurebus committee to define a highly reliable bus. This sequence of events was enough for VITA's NGA committee to adopt Futurebus as its new backplane architecture that month. The Navy then announced that it was indeed going to use Futurebus, and in February of 1989, the Multibus Manufacturers Group joined the IEEE P896 committee.

Because some members of the IEEE P896 committee are unlikely bedfellows, it's not surprising that the Futurebus generated concern over its impact on current products for the VMEbus and Multibus II. Even so, the committee members were able to define data-transfer protocols, bus widths, bus speeds, and a physical connection system. It became clear, however, that the new proposals were not consistent with the original IEEE STD 896.1 published in 1986. A complete rewriting of the specification was necessary. That new specification is known as Futurebus+. Currently, the 896.1 logical-layer specification and the 896.2 physical-layer and profile specification for Futurebus+ are in draft form awaiting IEEE members' approval.

elect and must wait until the current master is finished before becoming master and performing bus transactions. If a module with a higher priority number than the master-elect wants the bus while the master-elect is waiting to become master, it can initiate a new competition to establish a new master-elect.

The arbitration number also provides a round-robin bit and a 5-bit unique field for each module. Round-robin arbitration ensures a fair and equitable allocation of bus tenure between competing modules. Each module must record the priority level of the current bus master and set a round-robin bit when the module detects that the priority number is greater than its own. Each module clears a round-robin bit if it detects the priority number less than its own. If the priority number is the same, the bus is granted in a round-robin fashion according to the 5-bit unique number before the round-robin bit is cleared. In this manner, a module is inhibited from further arbitration competition as long as the round-robin bit is cleared.

When a master completes a transaction and no modules are requesting the bus, the master changes its status to parked, placing the bus in an idle state. To decrease the latency of arbitration when the bus is idle, a single competitor for the bus can immediately gain tenure of the bus by using the idle bus-arbitration mode.



***Backplanes that don't conform to hard metric dimensions** may become obsolete.) However, this prototype from Bicc-Vero, which conforms to P896.2, is available for developing products for experimentation and test.*

Data paths come in many flavors

Futurebus+ is an architecture that is scalable in many dimensions. One such dimension is the data-path width. Futurebus+ is basically a 64-bit data and address bus that employs a standard 64-bit multiplexed address/data pathway. However, it also provides for a 32-bit address/data subset pathway and a 128-bit or 256-bit data pathway. Futurebus+ is also scalable to accommodate dual or multiple parallel Futurebuses. Futurebus+ provides for locking mechanisms and cache-coherency mechanisms that allow several Futurebus+ chassis to be linked through cache repeaters.

Futurebus+ uses a compelled parallel protocol to transfer data between devices. The protocol requires a compelled reaction (an acknowledgment) either from the receiving device on each data transfer or at the end of a packet of data transfers between two modules. In a split-transaction mode, a module on the bus sends an address to another module, indicating that it wishes to transfer data. The module then relinquishes the bus until data transfer is possible.

The data transfer is completely asynchronous, which means that, as opposed to synchronous buses, the bus data-transfer rate is not locked into a specific clock frequency. Instead of issuing some initial control signals indicating that a master wishes to place information on the bus, the master places the information on the bus first. The bus transaction then takes place in three phases: a connection phase, which establishes the type of transaction with the desired slave; an optional data-transfer phase for transferring data; and a disconnection phase, which terminates the transaction and disconnects the slave.

Modules dance to the same tune

The participants in a packet-transfer transaction must all operate at the same rate. Before a transaction can occur, each module reads the transfer rates that each module in the system can support. The modules then set a transmit speed equal to the slowest speed

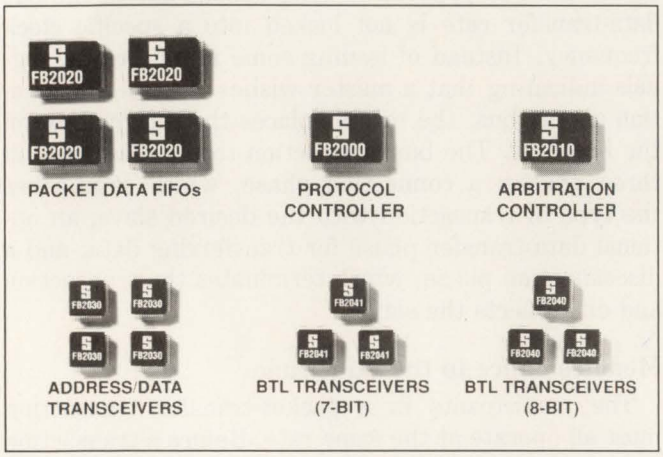
The data transfer is completely asynchronous, which means the bus data-transfer rate is not locked into a specific clock frequency.

a module on the bus can operate at and still accept a packet. The modules also set the fastest transmit speed that allows a module on the bus to accept a packet. The modules then negotiate a speed for a transaction during the connection phase. The master also sets the packet length, which can be as many as 64 data transfers.

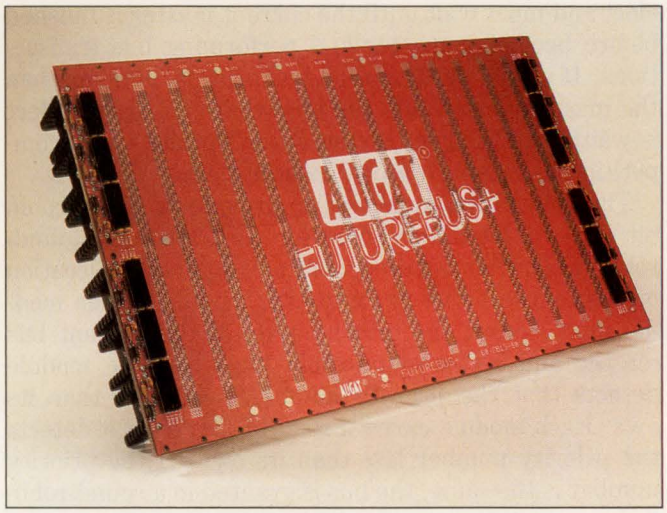
Each transaction phase uses a succession of bus beats to synchronize the master with the slave. A typical bus beat for a single slave transaction that requires a compelled response begins when a master issues address and control information to a slave. To assure that the lines are valid before asserting a high-to-low transition on a master synchronization signal, the master waits for the skew time of its own information lines to settle. The slave detects the synchronization signal and waits for the skew of its own receivers. The slave captures the information and activates the appropriate information lines back to the transmitter. After the slave waits for its information lines to settle, it asserts a low-to-high transition on a slave-synchronization line, which the transmitter acknowledges by issuing a third line handshake back to the slave.

This bus-beat handshake ensures the technological independence of each module on the Futurebus+ because each module need only account for its own skew on the information lines and its own timing requirements. When the packet mode is invoked, the data from the master to the slave occurs in packets of data before the slave is required to activate the slave-synchronization signal.

Many slaves have unique address ranges, but some may share areas of the same physical space. When a master accesses an address in one of these spaces, all of the slaves must activate a high-to-low transition on the slave-synchronization line because the line is wire-ORed. The slowest slave controls the release time for the broadcast transaction. A participating slave may induce the master to use this broadcast handshake, which can be used frequently in cache-coherent, shared-memory systems. When a cache detects that data is being transferred on the bus, the cache induces a broadcast handshake and reads the data, an operation known as snarfing.



The first step in getting a new bus architecture off the specification sheet is silicon support. *Philips/Signetics plans to develop complete Futurebus+ chip sets. The transceivers are currently available.*



Many Futurebus+ products are still under development. *This wire-wrapped backplane from Augat will not be released until there is final IEEE approval of the standard.*

Another mode of data transfer on Futurebus+ is split transactions, which allow modules with long data latencies to use the bus efficiently. For example, if a requester module wishes to retrieve data from slow memory, it enters the connection phase, informing a responder module of its wish. The requester then generates a disconnection phase and sends a 16-bit global identifier to the slave. When the responder's latency time expires, the slave negotiates for the bus to become a master and sends the data to the requester using the identifier. In this manner, the bus is free for other transactions while a responding module is gathering the data.

The Futurebus cache-coherency protocol permits as many as 32 processors to share memory on the bus. To reduce bus traffic, the Futurebus+ committee has adopted a copyback cache system instead of a write-through system. Some earlier bus architectures, such

as the VMEbus, support a write-through cache system that writes a cache line to main memory on each write to the cache. Although this cache scheme is simple to implement, in large processor systems it can swamp the backplane with cache write commands. A copyback cache scheme permits a μP to modify only its cache on a write command and not the main memory, thereby reducing traffic on the backplane. The Futurebus+ copyback scheme reads a 64-byte cache line from contiguous memory only when there is a read miss in the cache.

The copyback caching method requires an elaborate cache-coherency protocol to assure that multiple caches contain the same modifications to a specific portion of shared memory. The Futurebus+ cache-coherency protocol assumes that each module on the bus can read the tags associated with each cache line for all of the onboard caches on the bus. The protocol then assigns attributes to each cache line within a cache.

Futurebus+ uses these attributes in a MESI cache mode. MESI stands for the attributes of a cache line: Modified, Exclusive, Shared, and Invalid. To ensure cache coherency, the model requires that a μP first get permission to modify a cache line from all of the

Chip sets can make it real

If any bus is going to see the light of day, there must be silicon to support it. Currently, three vendors offer or are developing backplane drivers and logical-layer chip sets for the Futurebus+: National Semiconductor, Philips/Signetics, and Texas Instruments.

All of the vendors use Backplane Transceiver Logic (BTL) to maintain the projected transfer rates of the Futurebus+. The Futurebus committee expects Futurebus+ systems to perform a data transfer within 20 nsec in 1991 and within 10 nsec in 1995—independent of the width of the data pathway. Using these figures as a projection, modules using the compelled transfer mode, which requires a compelled response from a slave, will transfer 32-bit data at an approximate transfer rate of 100M bytes/sec in 1991; 256-bit systems will peak at 3.2G bytes/sec in 1995. The BTL driver was first designed by National Semiconductor to drive the low-impedance transmission paths needed to support these fast data-transmission rates.

The BTL driver reduces the capacitance of the driver by placing a Schottky diode in series with the open collector driver output. The diode resistance is typically less than 2 pF, and, allowing for 2 pF at the receiver end, the total loading can be kept under 5 pF. The BTL also uses a differential receiver, which detects 1V signals that swing about a 1.55V threshold and has resistors for impedance-matching the transmission line.

National Semiconductor is developing a number of second-generation BTL devices for the backplane. The Futurebus+ chip set includes 9-bit data transceivers that are latched and nonlatched handshake receivers with glitch filtering for eliminating wire-ORed glitches on the bus. The chip set also includes arbitration receivers for supporting the arbitration protocol and an arbitration controller, which implements Futurebus+'s round-robin protocol.

Philips/Signetics has already released a family of chip sets for implementing the Futurebus+ backplane. The first chips available are the FB2040 8-bit BTL transceiver, the FB20417 7-bit BTL transceiver, and the FB2030 address/data transceiver. The devices are fabricated in BiCMOS and feature propagation delays of 2 to 3 nsec and an output current of $I_{OL} = 100$ mA. The company plans to release a logical-level chip set in the fourth quarter. The set will include the FB2000 protocol controller, the FB21010 arbitration controller, and the FB2020 packet data FIFO.

Texas Instruments will introduce an octal latched transceiver with parity sometime during this quarter. The BCT979 is a BiCMOS device with BTL outputs with current capability of $I_{OL} = 100$ mA. The company is also planning to offer an arbitration controller, protocol controller, and cache-coherency controller in 1991. Rumors abound that other companies are also working on chip designs. If there is a wide variety of chip sets available when the Futurebus+ specification settles, it's bound to reduce the cost of developing Futurebus+ products.

Some transactions require cooperative actions between the caches during a transaction in order to maintain coherence.

other caches that have copies of the same line. The cache does this by generating a cache transaction that indicates the global memory address of the cached value.

Futurebus+ specifies a variety of possible cache transactions that can occur on the bus, such as copy-back, invalid read, shared read, modified read, invalid write, and invalidate—all of which define specific operations for the cache model. All caches are required to snoop the bus; that is, monitor each type of transaction on the bus. Some transactions require cooperative actions between the caches to maintain coherence, a process called intervention. For example, if one cache requests a cache line from shared memory and a second cache detects that it (the second cache) contains a modified version of the line, then that second cache must intervene and transfer the modified line in place of the line in shared memory.

In addition, all transactions on the bus that can be shared can also be snarfed. To snarf data, the cache converts the current transaction to a broadcast operation and captures the data on the bus. The broadcast operation allows the cache to obtain a shared copy of a cache line without an additional transaction. With many processors on the bus issuing transactions to both caches that have different cache-line attributes and to the shared memory, the permutation of possible bus events necessary to maintain cache coherency is large. Each cache controller requires service routines that will handle all possible combinations of events. Document P896.1 describes a number of the possible combinations.

To further complicate matters, Futurebus+ has an expansion provision that allows multiple Futurebus+ backplanes to be connected in a system. Multiple backplanes can be used in fault-tolerant applications. The backplanes connect through cache agents and memory agents that operate on a hierarchical cache-coherence protocol. The protocol allows the cache agent to snoop one of the buses and act as an observer for

Giving older buses a new lift

Whenever a new bus architecture arrives, there is talk about building bridges from it to existing architectures. The reason is simple: vendors want to preserve investments in existing product lines but still want to make use of the capabilities of the new bus. A bridge is little more than a communication scheme that allows the two buses to communicate with each other. Ideally, a bridge between the two buses should operate as if the boards for both buses are in the same backplane.

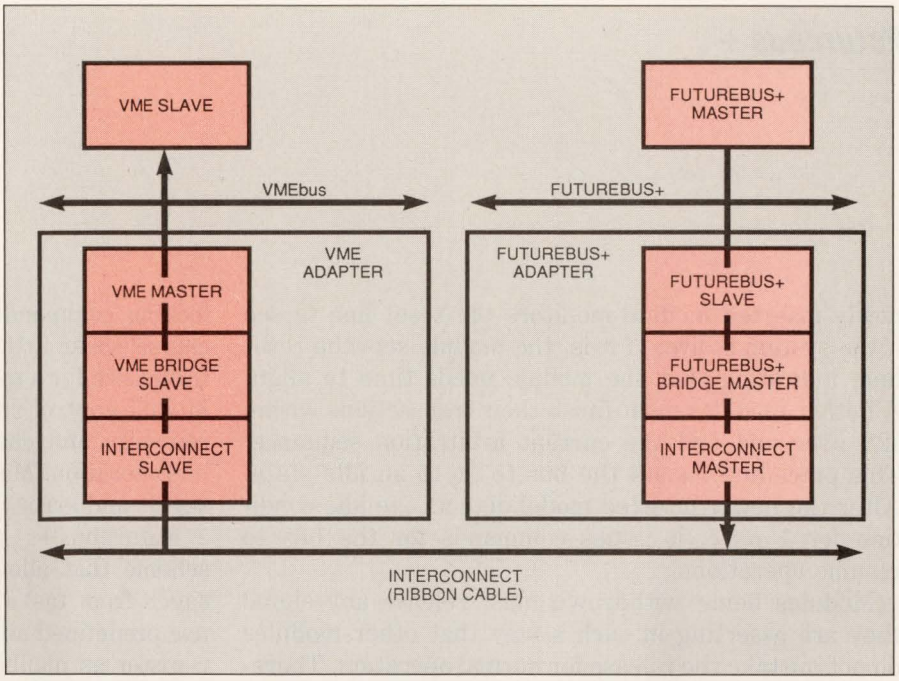
Ever since Futurebus+ started to grow in popularity, the VMEbus Trade Association (VITA) and the Multibus Manufacturers Group (MMG) have been trying to finalize specifications for bridges between Futurebus+ and either the VMEbus or Multibus. Both the VMEbus and Multibus have maximum data-transfer rates of 40M bytes/sec for 32-bit data transfers. Bus vendors would like to take advantage of the 100M-byte/sec, 32-bit data-transfer rate of Futurebus+. At wider data paths, Futurebus+ runs even faster.

Bridge translates bus cycles

Although VITA and MMG are trying to solve the same problem, their approaches are different. The VMEbus-to-Futurebus+ bridge consists of adapter boards for each bridge. The adapter boards are connected by a ribbon cable. The adapter boards have circuitry that translates the two buses' data-transfer protocols and bus cycles. Control and data paths between the buses and a set of protocols specify the routing of data between the buses. Each path is called a channel, and four channels are required—two data-access channels and two event channels.

A transaction example would be a write to memory across the bridge. If a module on the Futurebus+ wishes to write to memory on the VMEbus, the processor first becomes master by arbitrating for the Futurebus+. It communicates with a slave that resides on the Futurebus+'s adapter board. The slave interprets the transaction's address and passes the transaction through a bridge master to an interconnect master that communicates through the ribbon cable.

The interconnect master on the Futurebus+ adapter initiates a write cycle between the two adapter boards and passes the address, command, and data to an interconnect slave on the VMEbus adapter. The intercon-



The VMEbus to Futurebus+ bridge has adapter boards for each bus, *which interconnect through a ribbon cable. The circuitry in each adapter translates commands to be comprehensible for the bus cycles in each architecture.*

the other caches on the bus; the memory agent acts as a slave for global memory. The agents maintain a hierarchy of all the cache transactions that occur between caches and memory on the connected buses. The cache agent can split the transactions between a bus and a memory agent to eliminate latency and free the bus for other transactions. The memory agent keeps track of all the cache lines it is responsible for in the hierarchy.

The Futurebus+ specification allows for modules to be inserted and withdrawn while the system is in operation. During live insertion, newly inserted modules must align their logic-state machines with the other modules in the system before beginning operation. A

nect slave passes the information to the bridge slave, which transforms the write command so that a VMEbus master on the VMEbus adapter board can initiate a VMEbus write cycle. The VMEbus slave writes the data into memory and passes an acknowledge line back through the adapter boards to inform the Futurebus+ processor that the transaction is complete.

Although the VMEbus is limited to 32-bit data transfers, the existence of separate data and address buses in the VME backplane makes it possible to extend the width of the address and data path to 64 bits. The 64-bit VME extension, which has been adopted by the VMEbus bridge committee, is based on the work of Performance Technology Corp (Rochester, NY). The extension takes advantage of the fact that the VMEbus can transfer 256 bytes of data in block mode after specifying a single address on the first bus cycle.

The assumption is that all the subsequent addresses are sequential and can be determined by a counter. Because the address lines aren't used in the block-transfer mode, the 64-bit extension multiplexes 32 bits of data onto the address bus to produce a 64-bit data bus in block-transfer mode. The VMEbus bridge intends to use this feature to transfer 64-bit data between the two buses in block mode. DY-4 is teaming with Performance Technologies and Newbridge Microsystems to develop a chip set, called the Darf64, to implement the 64-bit extension.

Whereas the bridge between VMEbus and the Futurebus+ attempts to translate the data-transfer protocols for both buses practically on a cycle-by-cycle basis, the Multibus II bridge uses a more loosely coupled approach. The MMG feels that Multibus II already has many of the features of Futurebus+, such as message passing, geographical addressing, and automatic identification. Therefore, the MMG is primarily interested in gaining access data on Futurebus+'s high-speed cache-coherent memory bus.

The data-transport system uses the ISO 7-layered communications model and treats the Multibus II backplane as a local-area network. The network layer is implemented in software. The transport layer uses file-oriented services, such as streams and pipes, between different operating systems. The transport layer allows different operating systems to exchange data.

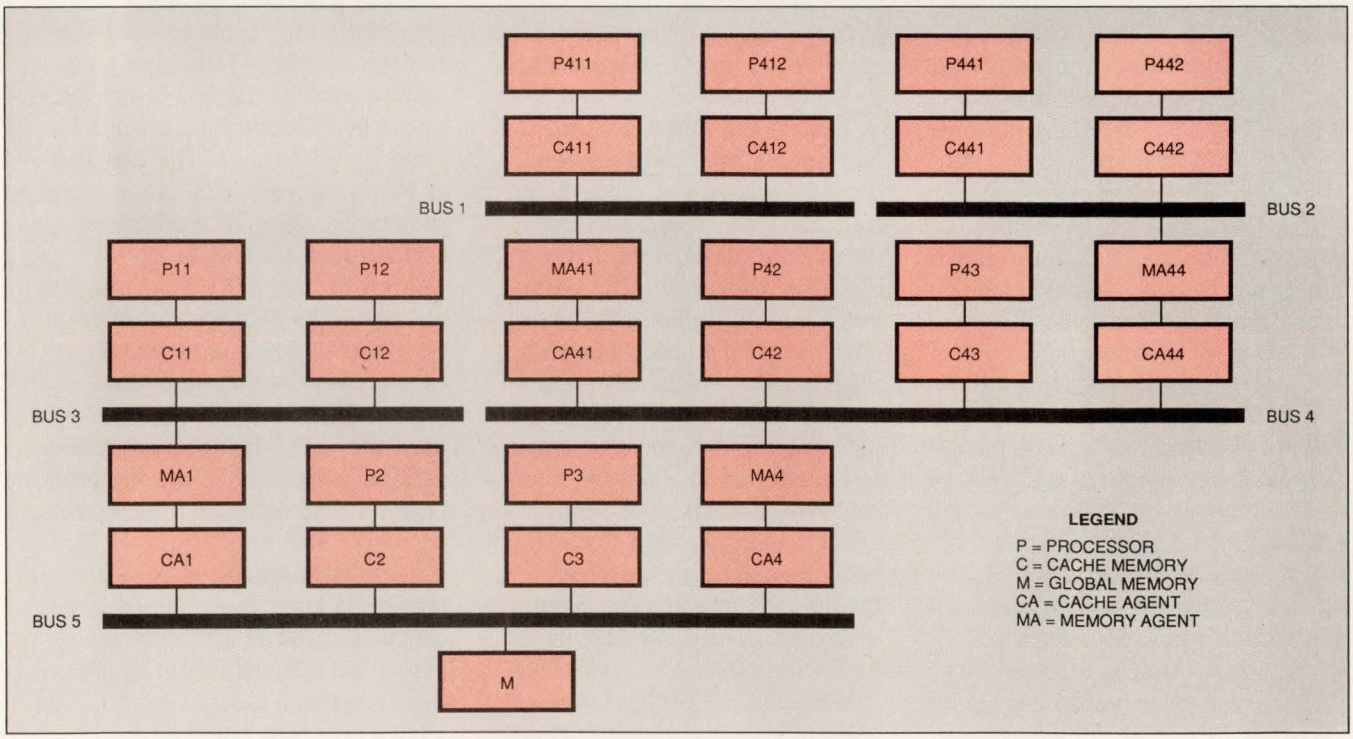
newly inserted module monitors the reset line to see if the system is live. If it is, the module sets the reset line, indicating that the module needs time to align. All other modules must finish their transactions within 128 μsec and end the current arbitration sequence. This procedure causes the bus to go to an idle state. After the newly inserted model detects the idle condition for 1 μsec, it issues commands for the bus to resume operations.

Modules being withdrawn must release any signal they are asserting in such a way that other modules do not mistake the release for normal operation. Therefore, each board requires live-withdrawal circuitry, which the operator informs via a switch that he is about to remove the board. The live-withdrawal circuitry performs the necessary housekeeping needed to perform a clean module withdrawal, such as copying and storing information.

A Futurebus+ module must also provide three types of control-and-status registers: module-capability registers, module-control registers, and module-status registers. Module-capability registers contain information on the module's capabilities for packet length, data-path width, bus mastering, split transactions, and locking commands. Other module-capability registers can select an arbitration time delay and the maximum frame size for a module that supports message passing. Module-control registers enable data in the capability registers and change control parameters that affect bus operation. Module-status registers indicate current status and error information.

Futurebus+ also provides a message-passing scheme that allows modules to send or receive messages from tasks running on other modules. Modules use predefined addresses within the control-and-status register as mailboxes to which a module can transfer a message frame. Because modules only write message frames to a mailbox, they are distinguishable from other Futurebus+ transactions. The message frame consists of a 2-byte header and a body that contains 64 bytes of frame data.

Each module has a mailbox structure that, to avoid deadlocks due to queues, contains three mailboxes. The specification defines a request mailbox and its associated queue for message frames that require an acknowledgment message to be returned to the requesting module. The module sends all acknowledgment message frames to the requesting module's response



Multiple processors on multiple bus segments communicate with global memory *using split transactions and cache and memory agents that implement the hierarchical cache-coherency protocols.*

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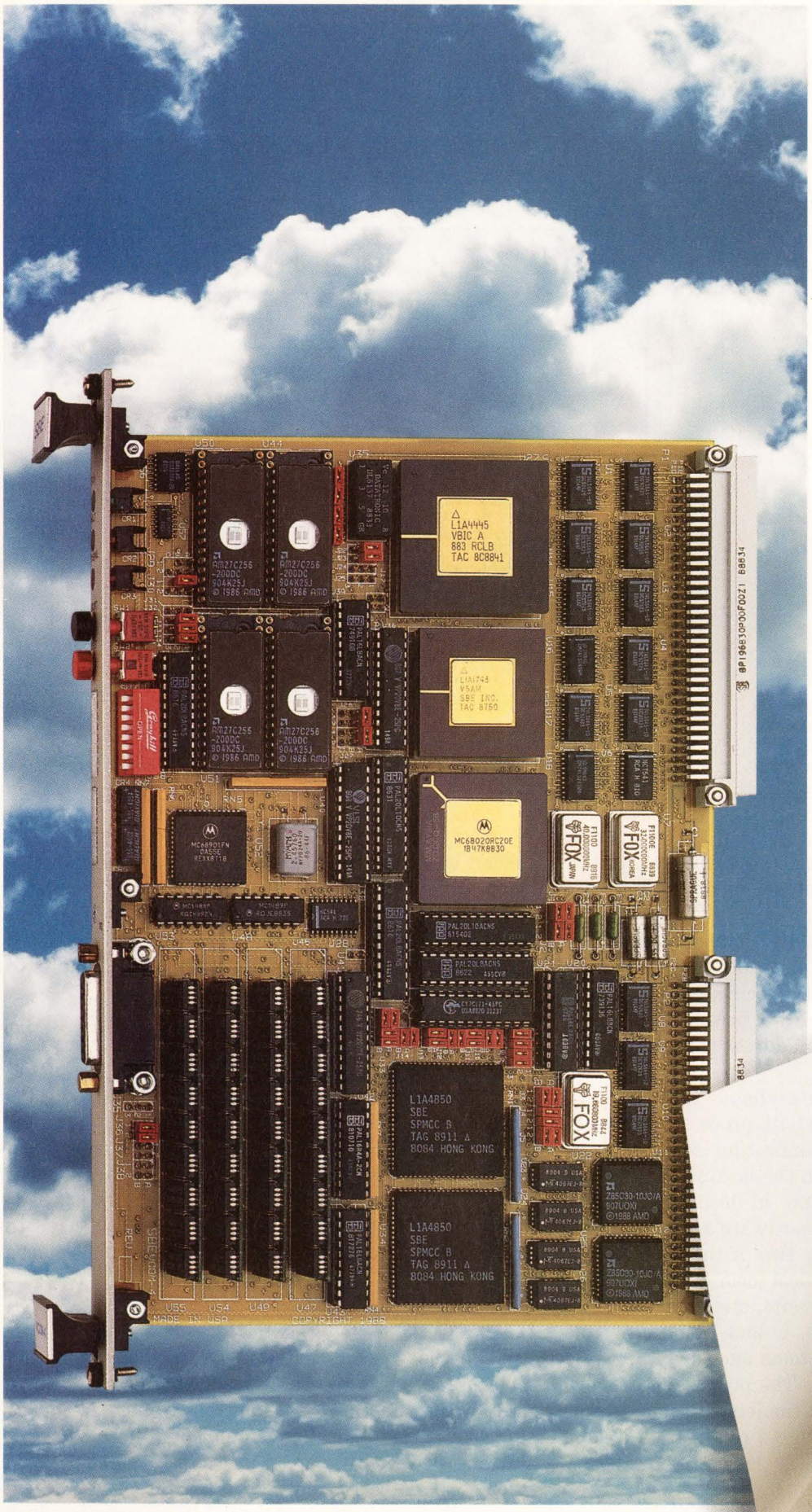

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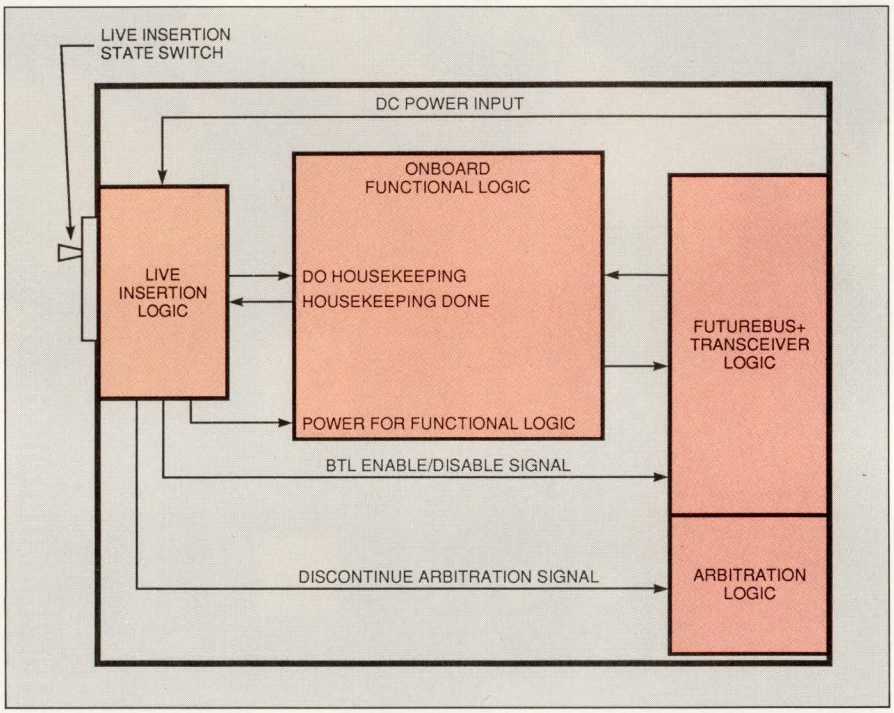

A functional design of a module for live insertion contains circuitry *that does the housekeeping chores to assure smooth board insertion and withdrawal without interfering with bus operations.*

mailbox. The modules also use the response mailbox and its associated queue for message frames that don't require an acknowledgment.

The modules are not allowed to induce a broadcast mode on messages received in either the request or the response mailbox, so the specification defines a third mailbox for this purpose—the broadcast mailbox. The broadcast mailbox has an address that is common to more than one module.

In conformance to the Futurebus+ philosophy of developing a backplane that is both processor and technology independent, the specification separates the logical-layer specification from the hardware specification. Currently, the committee, in document P896.2, has identified four different hardware configurations, called profiles. However, only two of them, A and B, have been defined for mechanical form factors, power-supply and signal-pin assignments, and environmental specifications. The other two, C and D, define cable interconnections between systems and an EISA-style hardware model, respectively. The purpose of the profiles is to give users different implementations to suit their needs. Boards plugged into a common backplane are guaranteed to be electrically and mechanically interoperable.

The specifications for Profile A and Profile B are similar: both support 32 and 64 bits of addressing. The major difference is the data-path widths. Profile A states that all backplanes must be wired to support a 64-bit data path with a default to 32 bits; Profile B defines a standard 128-bit data path, with defaults to 64 and 32 bits.

Profile B contains a subset of the logical-layer specifications of Profile A. Profile B calls for an I/O bus that is independent of the memory bus so that the Futurebus+ cache-coherency model doesn't extend to the I/O modules. Digital Equipment Corp intends to employ Profile B for I/O subsystems, which attach to a workstation through a bus bridge. The host's cache cycles do not pass through the bus bridge. Digital's intent is to have an I/O bus that, because it doesn't have to wait for cache latency times that occur on the host's memory bus, has a high throughput.

When will the standard settle?

When the specification was released in February, the consensus was to use 6U-wide (233.35-mm) Eurocards with a depth of 280 mm for Profiles A and B. However, since the draft was published there has been a strong drive within the Futurebus+ committee in favor of an all metric standard. The Eurocard is based on the hole patterns for a standard 19-in. rack, in which

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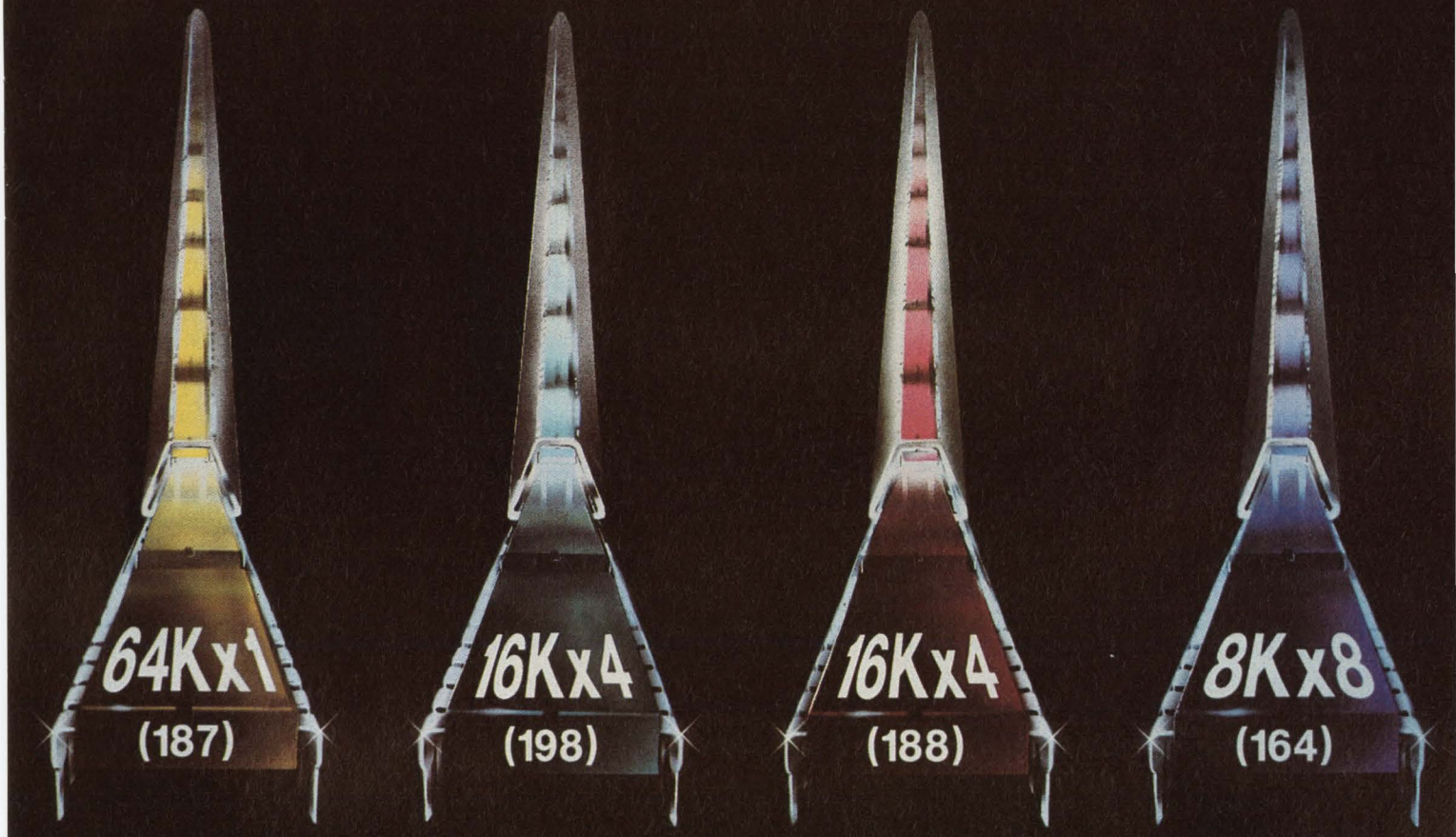

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a hole is made every 1.75 in. Therefore, the mechanical specifications for a Eurocard have a strange mixture of English and metric units, known as "soft metric" dimensions.

When the Futurebus+ committee met in Stockholm, Sweden, in May, it standardized on full metric dimensions, calling them "hard metric." This was done with an eye toward 1992, when Europe will become one market. The committee discarded the 96-pin Eurocard and its connector, which has 0.1-in. pin centers, in favor of a connector with 2-mm pin centers. The committee chose a panel height for Profile A and B of 300 mm. After leaving room for card guides, the new board is 265 mm wide and 300 mm deep. The committee also changed the board spacing of the card rack from 1 in. to 30 mm.

It's been this waffling on the specifications that has prevented proliferation of hardware for Futurebus+. In fact, Futurebus+ backplanes that Mupac and Bicc-Vero introduced a year ago are essentially obsolete because they conform to the soft metric dimensions in the P896.2 specification. However these companies still offer the products as prototype development tools for developers to learn and experiment with the complexities of Futurebus+.

Both companies are currently developing hard metric backplanes, which they will probably announce when the specification is finalized. In addition, Mupac is developing hard metric enclosures and prototype wire-wrapped boards. Augat is also developing hard metric backplanes, chassis, extender boards, and prototype boards, but will not offer them for sale until there is IEEE approval of the specification. EDN

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For more information . . .

For more information on the Futurebus+ products discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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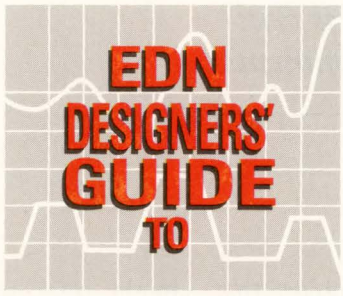


real-time Ada
Part 3

Ada runtime environments demand close scrutiny

The first two parts of this series on Ada presented an overview of the language and discussed concurrent and low-level programming. This article, the last in the series, describes the requirements that Ada runtime environments must meet and provides criteria for evaluating Ada vendors' runtime implementations.

Benjamin M Brosgol, *Alsys Inc*

Ada isn't just a pure and rarefied theory. Sooner or later, an Ada program must run in the real world on a real computer. Various methods exist for performing any one Ada function, and every Ada vendor has its own body of ideas on how to implement Ada.

The runtime model is the compiler vendor's mapping of the runtime data and processing of your program to an efficient implementation on your target hardware. Every Ada implementation must address such issues as memory-storage organization, data access, subprogram linkage, code-space minimization, and dynamic memory management, among other concerns. Ada vendors make decisions on how to deal with these issues, and real-time programmers must assess each vendor's implementation for use in their applications.

How a runtime model organizes memory storage is an important consideration when choosing an implementation because Ada offers a flexible memory model. The compiler can store runtime data in three different ways based on allocation and reclamation characteristics.

The simplest storage method, static storage, is preallocated at program-load time and only deallocated upon the program's termination. Because data objects declared within library packages are alive throughout program execution, they can reside in static storage.

A more advanced method is stack storage, which is allocated and deallocated in a last-in first-out fashion, so that the portion of memory in use at any moment is logically contiguous. Local-data objects declared in a subprogram or block are alive only during that particular subprogram's or block's execution and, thus, can reside on the stack.

Heap storage, the most flexible but hardest to implement storage method, is allocated and deallocated dynamically, either explicitly by the programmer or implicitly by the runtime executive. The memory portions

The size of the executing program is critically important in real-time environments.

in use are not necessarily contiguous. An object that an Ada "allocator" creates (using the *new* construct) must in general reside on the heap, because it is alive as long as some pointer or access value contains its address.

Room for maneuver

Within these general storage guidelines, an Ada vendor can make many implementation decisions that will affect the efficiency of a program as well as its ability to declare large data items.

To understand the basis for such decisions, first consider that a characteristic of general-purpose, block-structured languages like Ada is hierarchical program structures. These structures let you declare a subprogram locally within another subprogram. Hierarchical structuring organizes a program to reduce complexity.

A side effect of such a structure is that a subprogram might refer to data items not declared locally but rather in some outer, containing subprogram that is higher in the hierarchy. (In Ada, "program" is not a general term. The defined Ada term "program" refers specifically to the entire body of code running—hence the term subprogram in this context.) A subprogram may also refer to data items declared "globally," that is, in previously compiled library packages. A critical factor in determining the runtime efficiency of an Ada program is how the compiler sets up data accesses for global data, local data, and intermediate ("up-level") data declared in outer subprograms.

A main concern for an application programmer regarding an Ada vendor's implementation of static storage is if the upper bound on the size of the storage area is sufficient for handling programs with large amounts of global data.

This question arises because most processors have

Building and executing Ada programs

Constructing an executable Ada program is basically similar to the steps you would take with other languages. But Ada has a few unique requirements that enhance interface checking across separate-compilation boundaries.

When you compile an Ada program, you must identify not only a source file but also a "program library." As the term suggests, a program library is a database of information about compiled program units. The compiler and other tools in the Ada environment access and update this database. In a cross-compilation environment, the program library resides strictly on the host.

Three types of information correspond to each unit in the program library. The first is the "object code," which the linker will combine with other object modules to form the executable program. The second is the "interface information," which the compiler will use when subsequently translating other units. It guarantees that the Ada-language rules are enforced across separate-compilation boundaries. The third is the "dependence relationship" of the unit with previously complied units, such as through an Ada *with* clause.

Invoking the binder

Ada's unique *binder* is a prelink tool that determines which units will compose the executable program. When you invoke the binder, you identify the main subprogram (that is, the subprogram where program execution will begin) and the program library. Based on the relationships between units, the binder determines which object modules from the library are needed. Although binding and linking are conceptually different steps, in practice you would likely have the binder automatically invoke the system linker to produce the resulting executable program.

An important optimization for the binder is to eliminate from the executable program those subprograms that are not called. This elimination is likely to yield a significant reduction in code space, because even though an Ada *package* can contain a large number of subprograms, only a fraction of them may be required.

The binder also ensures that compilation for an executable program's constituent units is up to date, thus avoiding interface mismatches. For example, suppose that after compiling a procedure, ALPHA, that takes a parameter value of type FLOAT, you successfully compile another unit, BETA, that calls ALPHA with a floating-point value. Binding BETA will be allowed (**Fig A**).

However, if you subsequently modify ALPHA to take an INTEGER value instead, and recom-

instructions for fast accesses to data at an offset from a storage base—but are limited on the size of the offset. Thus, there is a tradeoff between execution speed and static-data capacity. Moreover, because the total static-storage requirements become known only at program-bind time (see **box,** "Building and executing Ada programs" for a description of Ada's unique *binder*), the compiler does not have the necessary information to choose optimally.

An effective way for an Ada vendor's implementation to solve this problem is to provide different strategies for dealing with "small" and "large" global data. Small data items can reside in the static-storage area and be accessed efficiently via a fixed offset from the base of this region. Large data, on the other hand, can reside in a different logical-data region. Accesses to large data use a reference to the actual object's location (**Fig 1**). This reference resides with the small data items at a fixed offset from the base of the static-storage region. Thus, an access to a large-data object may pay the price of one level of indirection, but it reduces the risk of the global-data requirements exceeding the processor's innate size limit on the static-data area. In some cases, compiler optimizations can eliminate the indirection overhead altogether.

Another concern for implementing static storage has to do with a real-time program that runs on a ROM-based target system: Can constant data and initial values reside in ROM, and can the program restart without requiring any downloading? Placing read-only data in ROM requires the compiler to separate statically known constants from other data. In Ada, you can declare a constant with a dynamically computed value; thus, not all Ada constants will necessarily be ROM-able.

When restarting programs, one has to decide how

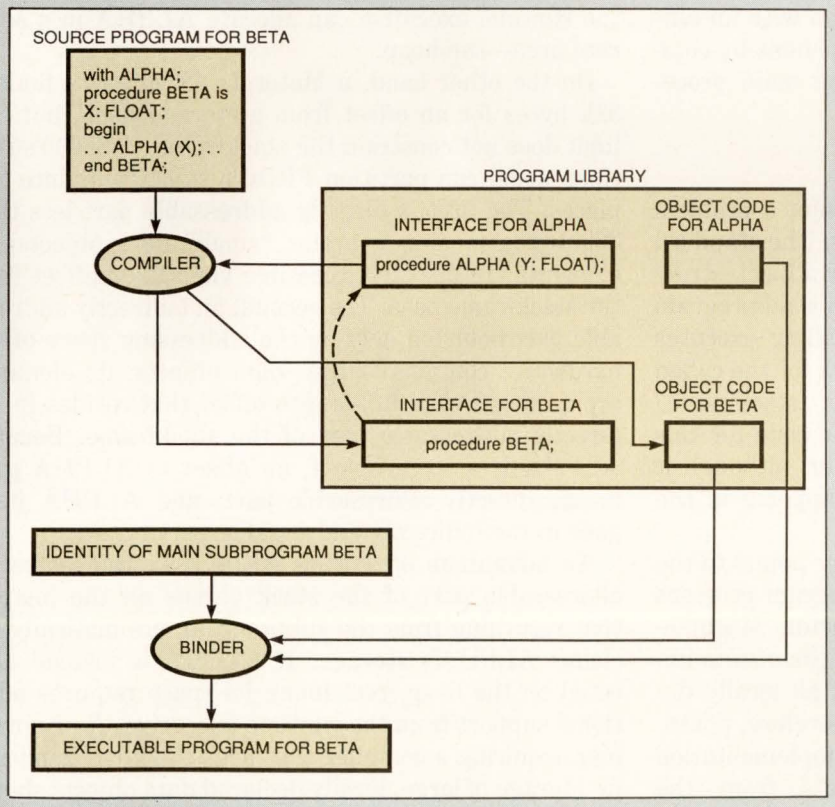


Fig A—Ada's unique binder links *compiled program units and checks all the interfaces between them.*

pile it, the dependent unit BETA becomes obsolete. Linking ALPHA and BETA would be an error, because the interfaces no longer match. In fact, the binder will reject any attempt to bind BETA. A bind will only succeed after you have corrected BETA (to pass an INTEGER) and recompiled it into the program library.

Program execution

Executing an Ada program proceeds in two steps. The first step, sometimes known as *package elaboration,* comprises the runtime processing associated with packages bound into the executable program (such as initializing global data and activating global tasks). The second step actually invokes the main subprogram.

Because Ada's designers wanted to encourage good programming practices, Ada offers the benefits of private types without causing needless overhead.

to reinitialize statically allocated data. Ada lets the programmer specify initial values for variables. The language also provides default initialization for objects of certain data types. An example of a declaration with an explicit initialization is

```
package P is
   ALPHA : array (1..3) of INTEGER := (10, 20, 30);
end P;
```

The example raises the question of how ALPHA acquires its initial values. The *binder* could arrange for initialization during program load. However, this tactic would make restarting the program on the target hardware without a download to the initialized static-data area impossible because, during program execution, the value contained in the variable ALPHA may change. Instead, the Ada implementation should initialize variables at runtime during the "package-elaboration" process, which precedes the invocation of the main procedure. The implementation should optimize this initialization by reserving the values for aggregate array (10, 20, 30) in the constant area. Program restart would then simply repeat the elaboration with an efficient block move, rather than with component-by-component assignment, before invoking the main procedure.

Capacity for local-data storage

Large locally defined data items present a problem similar to that of large global data items. The standard way to implement local-data storage for a block-structured language is a runtime stack. When a subprogram calls another subprogram, the act of calling executes code to claim space at the top of the stack for the called subprogram's local data—this space is a "stackframe" or an "activation record." Note that the code for this operation is invisible to the programmer; although it exists in the runtime image, it never appears in the high-level-language source.

Typically, a dedicated machine register points to the base of the stackframe and the subprogram accesses its local data via offsets from this register. Machine-architecture limitations on the size of these offsets imply, however, that direct addressing of all locally declared items might not be achievable. Therefore, potential users should check that an Ada implementation doesn't restrict local data to offsets from the stackframe's base. Instead, an Ada implementation should provide a strategy for indirect references to large data.

As it does with large data in static storage, the Ada implementation can reserve space at a fixed offset from the stackframe base to hold a reference to the large object. This reference may be either a full-sized offset (with respect to a particular storage base), a machine address, or some other form. An example of a large data item that an Ada implementation might have to handle is

```
procedure PROC is
   ALPHA : array (1 .. 40_000) of CHARACTER;
   ...  -- Other declared data
begin
   ...
end PROC;
```

ALPHA requires 40,000 bytes of storage, but Intel 8088/80186/80286 μPs, for example, have a size limit of 64k bytes for *procedure* PROC's stack segment. Thus, ALPHA should not reside on the stack; if it does, a distinct danger of storage overflow exists. The Ada compiler can instead reserve a 32-bit pointer in the stack segment to allow addressing of ALPHA. And the runtime executive can allocate ALPHA in a separate area—the heap.

On the other hand, a Motorola 68000 has a limit of 32k bytes for an offset from a storage base, but this limit does not constrain the stackframe. A 68000's runtime model can partition PROC's stackframe into two pieces. The first, a directly addressable part less than 32k bytes in size, contains "small" data objects; its elements are directly accessible via a fixed offset from the stackframe base. The second, an indirectly addressable part bounded only by the addressing space of the hardware, contains "large" data objects; its elements are accessed via a full-length offset that resides in the directly addressable part of the stackframe. Because ALPHA is a large object, an offset to ALPHA goes in the directly addressable part, and ALPHA itself goes in the indirectly addressable part.

An advantage of storing ALPHA in the indirectly addressable part of the stack versus on the heap is that returning from the subprogram automatically reclaims ALPHA's storage. If ALPHA is instead allocated on the heap, reclaiming its space requires additional support from the runtime executive. A programmer acquiring a compiler that uses the heap implicitly for storage of large, locally declared data objects should check that the heap space reserved for each object gets reclaimed on return from the subprogram in which the data item is declared. Such reclaiming is essential

for reducing the risk of "storage exhaustion."

For some machine architectures, the issue of where to allocate small or large data objects does not arise. An Intel 80386 in 32-bit mode, for example, can directly address even large objects from its stackframe base. So the 80386 has no need for either indirection on data accesses or special reclamation support.

One issue that all implementations of block-structured languages such as Ada must face is how to maintain data addressability when invoking a subprogram. For references to global data this addressability is not a problem, because a dedicated register typically points to the base of the global-data area. Similarly, maintaining addressability for local data is not a problem because a dedicated register generally references the base of the current stackframe.

For an up-level reference to a data item declared in an enclosing subprogram higher in the hierarchy, however, the situation is not quite so straightforward. For example, a recursive subprogram can have several stackframes alive at the same time, each with a separate copy of the subprogram's local data. If a lower-level subprogram, defined locally to the recursive subprogram, accesses the recursive subprogram's local data, the Ada implementation must ensure that the lower-level subprogram uses the correct stackframe.

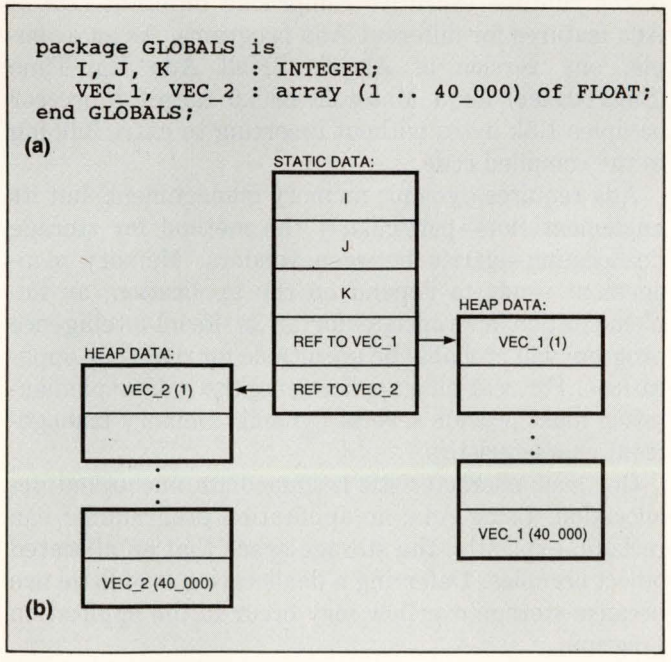


Fig 1—To guard against stack overflow, *an Ada implementation should be able to store large, local-data objects* ***(a)*** *in the heap. A pointer on the stack accesses such large objects indirectly* ***(b)****.*

(Note that Ada's scoping rules are more general than C's. In standard C, functions cannot be nested, and so up-level references do not arise.)

Compiler vendors can use one of two principal techniques to ensure the correct stackframe is used. One is a so-called "display vector," which is an array of addresses for the bases of the stackframes containing the referenceable data objects. This vector can reside in a set of dedicated registers or at an accessible area in RAM.

The alternative technique is to keep, at a known location in each stackframe, a static link to the stackframe of the immediately enclosing subprogram, which is the subprogram that is just one level higher.

Up-level references are likely to occur more frequently in Ada programs than in programs written in other languages, because of Ada's package facility. Typically, a programmer writes a package containing at least one subprogram that refers to data declared inside the package. If the package declaration occurs inside a subprogram, the data objects declared by the package have the same lifetime as the local data of the enclosing program. Thus, the package's subprograms may have to make up-level references to nonglobal, dynamically defined data.

These techniques for dealing with up-level references are not unique to Ada; they were developed more than 30 years ago for the first Algol compilers. On the other hand, Ada does allow important optimizations of subprogram linkage, and programmers should check whether a prospective compiler carries these out.

Two factors affect the efficiency of solutions to the up-level-reference problem. One is the cost of performing the up-level reference. The other is the cost of creating the environment (ie, the set of stackframe addresses for statically enclosing subprograms) when a subprogram gets called, and restoring the caller's environment when the subprogram returns. With both factors taken into account, the display-vector mechanism tends to be the more efficient mechanism on most machines.

In some high-order languages, the cost of subprogram calls is so high that programmers avoid using subprograms and instead construct large, monolithic units. This practice results in unmaintainable code with poor modularity. One of the principal design objectives of Ada was to make subprogram linkages extremely efficient by providing fast calls and returns and speedy parameter passing. This efficiency encourages programmers to write modular code, with subprograms

In some high-order languages, the cost of subprogram calls is so high that programmers avoid using subprograms and, instead, construct large, monolithic units.

corresponding to logically coherent processing steps and with explicit parameter passing (versus sharing global data) to reduce coupling between modules.

A compiler designer's decisions affect the efficiency of subprogram linkages, and an application programmer should check how Ada vendors implement them. The choices for calling-sequence and parameter-passing implementations are important, as is minimizing the time spent maintaining up-level addressability. A good Ada implementation can yield faster subprogram linkages than other languages, such as Pascal, because Ada doesn't use subprograms as runtime parameters and, thus, facilitates certain optimizations.

Ada's pragma INLINE also helps the language obtain fast subprogram linkages. This pragma eliminates the cost of calls and returns for short subprograms by expanding the subprogram, somewhat like a macro, at the point of call.

The first two articles in this series (EDN, September 3, 1990, pg 153, and EDN, September 17, 1990, pg 151) emphasized the important principle of data abstraction, which localizes the effect of maintenance modifications to data-structure definitions. To obtain this benefit in Ada, the programmer declares a private type in a package. Ada's rules guarantee that only subprograms explicitly defined along with the type can manipulate objects of that type. In many real instances, however, subprograms are short pieces of code that simply access an element of a data structure. Here, the cost of the subprogram's call and return may be greater than that of executing the actual subprogram body.

Because Ada's designers wanted to encourage programmers to use good programming practices without sacrificing efficiency, you should not be surprised to find that Ada does allow the benefits of private types without causing needless overhead. The pragma INLINE is the way to do this.

Keep program size to a minimum

The size of the executing program is critically important in real-time environments; understanding the kinds of implementation decisions that affect program size are, therefore, important too. Because an executing program consists of both compiled code and runtime-executive routines, a user should look at both components when judging the space efficiency of a compiler system. A compiler implementor can artificially reduce the size of the runtime executive by expanding various runtime services in line. For very small programs, this scheme may save space, but for more realistically sized applications, the expansions are likely to outweigh any savings from a small runtime executive.

At the other extreme, a compiler vendor attempting to minimize the size of compiled code can use out-of-line calls instead of in-line instructions. But this tack will, of course, result in a substantial time penalty. Thus, assessing code-space efficiency requires inspecting the sizes of both the compiled code and the runtime executive, preferably for real applications and not artificial benchmarks.

An important—in fact, essential—optimization for an Ada compiler is to eliminate from the executable image those subprograms for which no calls appear in the program. This elimination is especially useful in Ada, because a package used in an application may contain a large number of subprograms with only a small fraction actually getting invoked. The prelink (binder) tool in some Ada compiler systems performs this optimization.

If the compiler vendor's runtime executive is itself written in Ada, then eliminating unused subprograms in the runtime executive itself will reduce the size of the executive—a potentially useful side effect.

In addition to eliminating unused subprograms, a compiler vendor may also supply reduced-size versions of the runtime executive comprising different sets of Ada features for different Ada programs. As an example, one version of Alsys's SMall Ada Run-Time (Smart-Exec) for a Motorola 680x0 target processor occupies 1.5k bytes without resorting to extra inlining in the compiled code.

Ada requires dynamic memory management, but its implementation—particularly the method for storage deallocation—varies between vendors. Memory management tends to depend on the application; an implementation appropriate for an artificial-intelligence program will probably be unsuitable for real-time applications. For real-time applications, the Ada implementation must provide several dynamic memory-management characteristics.

One such characteristic is immediate unchecked deallocation. Using Ada, an application programmer can reclaim, explicitly, the storage space that an allocated object occupies. Deferring a deallocation is of little use because storage overflow may occur in the application program.

The Ada implementation must also provide support for the pragma CONTROLLED and for the 'STORAGE_SIZE representation clause. Ada programmers

should be able to ensure that they can reclaim the memory space occupied by an entire set of objects allocated for a particular "access type"—also known as the access type's collection—when their program's control leaves the scope of the access type. The Ada implementation can arrange this reclaiming through the pragma CONTROLLED, which is either explicitly provided by the programmer or automatically supplied by the Ada implementation for nonglobal access types. An alternative technique for reclaiming memory space is through a "representation clause," which associates a collection size ('STORAGE_SIZE) with an access type.

Although the Ada language allows an implementation to provide automatic "garbage collection" when storage is exhausted, such an approach is not appropriate in real-time applications. Automatic-reclamation schemes suffer from unbounded execution times, which could cause your program to miss a critical deadline. Similarly, "on-the-fly" incremental-reclamation techniques also incur too much overhead for real-time systems. Furthermore, the execution time for an allocation and for a deallocation must be predictable, so that the programmer can ensure that his or her program meets its real-time deadlines.

A potentially lethal bug for the kinds of long-running programs that are typical in real-time applications is the phenomenon known as storage leakage—gradually exhausting dynamic storage by failing to reclaim storage that is no longer used. If, in a program comprising a loop, even a small amount of storage is used but not reclaimed at each loop iteration, the program will eventually terminate with a STORAGE_ERROR exception. Part of the responsibility of preventing this error rests with the programmer, but the Ada implementation of the runtime executive must also be designed properly. In particular, when control passes out of any scope, whether normally or through a "propagated" exception, the runtime executive must completely deallocate any storage that it implicitly allocated during the execution of the scope (as well as storage from access types that are local to the exited scope). Similarly, storage for a terminated task must be completely reclaimed.

The Ada implementation should avoid fragmentation that can cause STORAGE_ERROR. In some cases, depending on the execution order of subprograms that allocate and deallocate memory, the heap can get fragmented. If it does, the total available space might satisfy a request from an allocator, but the largest contiguous free area could still be too small. Because automatic compacting would violate the requirement for predict-

Glossary of Ada terms

Allocator (*new*)—An Ada feature that dynamically creates an object and delivers an "access value"—or pointer—to designate the object.

Binder—The tool in an Ada compilation system that, when given the name of the main subprogram and the identity of a program library, determines the compilation units needed to compose the program and (as a user option) links them to form an executable program.

Heap—A storage area containing data objects whose allocation and reclamation is not necessarily last-in first-out. The heap, therefore, requires explicit reclamation support from the programmer or the runtime environment.

Package elaboration—The initializing step at program execution before the main subprogram is invoked.

Pragma—A directive to the compiler, typically for optimization.

Runtime model—The set of decisions made by the compiler vendor that governs the compiled code's and runtime environment's usage of target-machine resources.

Runtime stack—The data storage area for each task, managed in last-in first-out fashion, that is used at runtime for subprograms' parameters and local variables. At any point in program execution, a task's stack consists of a sequence of stackframes for subprograms whose execution is in progress.

Scalar—A data item having a numeric or enumeration type.

Scope—A region of program text in which a declared name has meaning.

Stackframe—The segment of a runtime stack containing the parameters and local data of a subprogram.

Subprogram linkage—The conventions for calling and returning from a subprogram, establishing data addressability, and passing parameters.

One issue that all implementations of block-structured languages such as Ada must face is how to maintain data addressability when invoking a subprogram.

able execution times, this issue is more in the domain of the application programmer. Nevertheless, some heap-management methods are less prone than others to storage fragmentation, so the application programmer should check the characteristics of an Ada implementation to see if fragmentation will be an issue. Note that some Ada implementations allow applications programmers to tailor storage-management algorithms or to monitor heap usage as the program runs.

Choosing an exception-handling approach

An Ada implementation's exception-handling facility should detect and respond to synchronous runtime events that occur infrequently (which are most often errors) and that do not require control to return to the point of occurrence. Examples include arithmetic and buffer overflows, and data-format errors. The runtime-system designer's main implementation decisions are how to detect where an exception is raised, and how to find an associated handler.

The choice depends on the tradeoffs that the runtime system makes. If the goal is to minimize the time spent in raising and handling exceptions (at the possible expense of subprogram linkages), then at each subprogram call, the runtime system passes an implicit parameter identifying the location of the handlers for exceptions that the called subprogram might raise.

On the other hand, if the goal is to optimize subprogram calls, the runtime system passes no exception-related information at subprogram invocation. Instead, the compiler and binder generate scope and handler tables. The exception manager code in the runtime executive interrogates these tables only when an exception is raised or propagated.

Because Ada's designers intended exceptions only for infrequent events, the table approach is preferable. Its efficiency in dealing with normal subprogram calls more than offsets its extra cost when raising or handling exceptions. Subprograms are such an important program-structuring technique that users should view them as essentially zero-overhead features. Thus, there should be no exception-related costs to subprogram calls.

The tasking features in Ada for real-time applications place demands on the design and implementation of the runtime system. The principal issues are time efficiency, space efficiency, and real-time functionality.

Certainly an important consideration is the speed of the Ada "rendezvous." The compiler can and should detect special cases and handle them in the most efficient way. One example of a rendezvous that needs special handling is the so-called synchronization rendezvous (**Fig 2**). The call DEVICE_1.READY is for synchronization, not data communication. If DEVICE_1 is suspended at its *accept* and then the higher-or equal-priority task DEVICE_CONTROLLER executes the *entry* call, no real need exists to switch contexts to the DEVICE_1 task. Instead, the runtime system can simply mark DEVICE_1 as eligible for execution, and DEVICE_CONTROLLER can continue immediately; no context swaps are involved.

There are several space-related issues associated with implementing tasking in an Ada runtime system. One is the size of the task control block—the repository of state information for a task during its execution. To support large numbers of tasks, the task-control block should be compact. Another issue is the size of each task's stack. The programmer should be able to specify stack sizes (through the 'STORAGE_SIZE representation clause), because a task will often not need much stack space. Moreover, once a task terminates, the runtime system should immediately reclaim all the task's resources.

A final tasking consideration is load insensitivity. The number of tasks in the program should not affect the speed of tasking operations.

Runtime functions

Real-time applications demand that the Ada runtime system support certain functions. For example, when a delay for a high-priority task expires, the runtime executive must immediately pre-empt any executing lower-priority task so that the awakening task can run. As another example, executing an abort statement must immediately place the aborted task in an abnor-

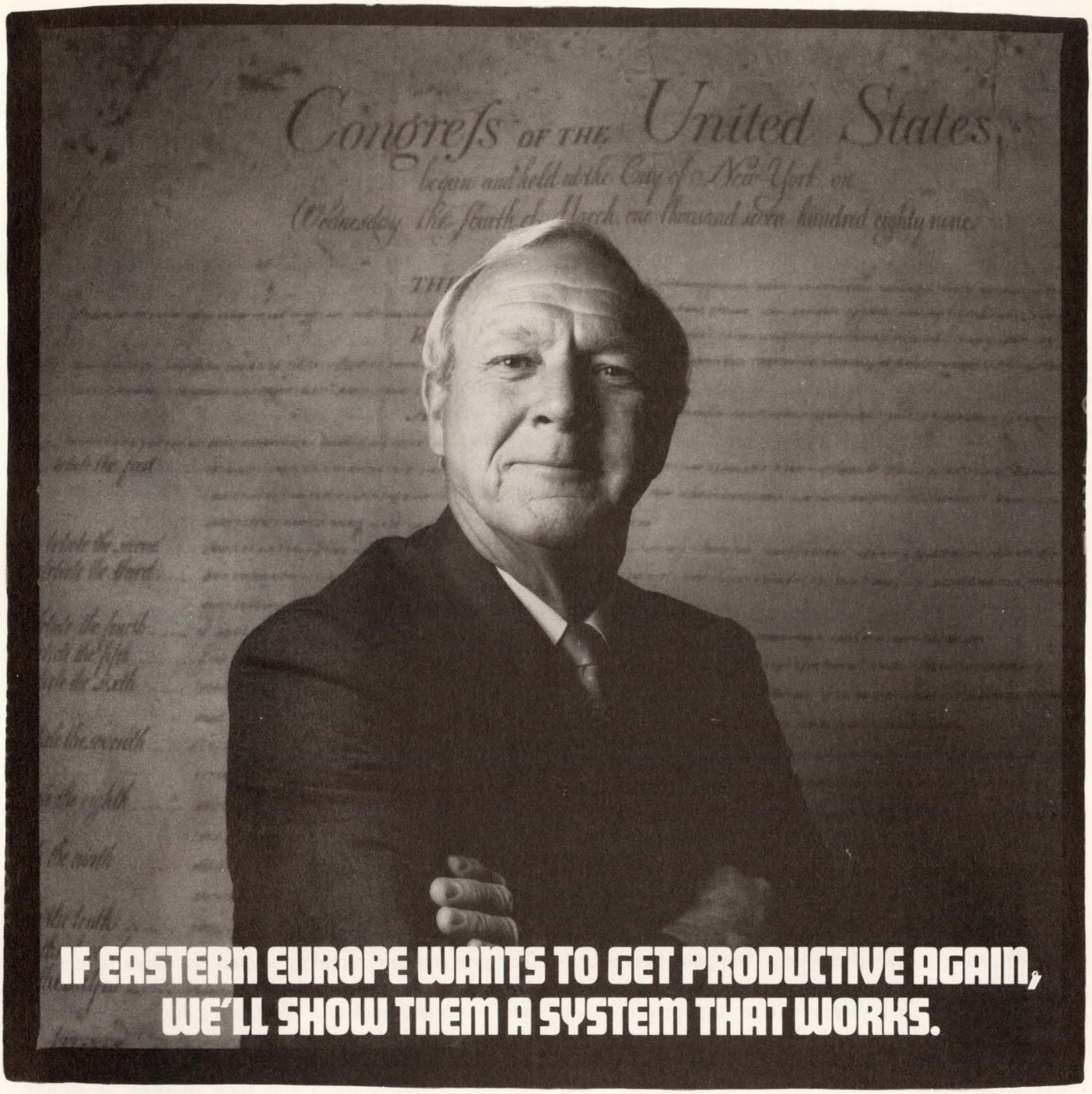
```
task DEVICE_1 is
   entry READY;
   ...
end DEVICE_1;

task DEVICE_CONTROLLER;

task body DEVICE_1 is
   ...
begin
   ...   -- Initialization
   accept READY;
   ...
end DEVICE_1;

task body DEVICE_CONTROLLER is
   ...
begin
   ...
   DEVICE_1.READY;
   ...   -- Continue, knowing that DEVICE_1 initialization has occurred
end DEVICE_CONTROLLER;
```

***Fig 2—The DEVICE_CONTROLLER task** executes a rendezvous for synchronization, not communication, purposes.*



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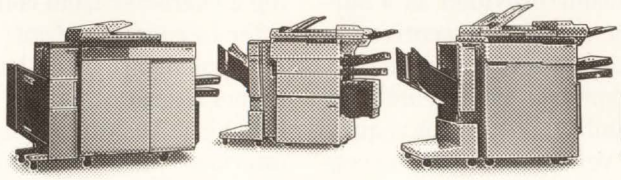

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A critical factor in determining the runtime efficiency of an Ada program is how the compiler sets up data accesses.

mal state. Deferring these operations could lead to missed deadlines, so an implementation that uses a polling scheme—waiting until synchronization points to identify the highest priority task eligible to run—is not appropriate for real-time applications. Users should also be able to control certain aspects of scheduling behavior, such as whether equal-priority tasks are time-sliced or run until blocked.

Recently, some developments have occurred in real-time scheduling theory that apply to Ada. The main developments are based on the rate-monotonic scheduling algorithm, which assigns priorities to periodic tasks so that the tasks with the shortest periods get the highest priorities. If rate-monotonic scheduling is used, then an application programmer can guarantee that the deadlines of all the periodic tasks will be met, provided that the total processor utilization is less than a bound given by a simple arithmetic formula. A real-time programmer can thus express an application using Ada tasks, with the runtime executive automatically multiplexing the tasks, rather than take the error-prone approach of developing a cyclic executive and performing explicit task switching.

One potential problem whenever tasks are not independent is *priority inversion*—the blocking of a higher-priority task by an executing lower-priority task. Certain kinds of priority inversion may be unavoidable, for example, in instances when tasks of different priorities are using a shared resource. Suppose that a low-priority task is accessing such a resource (for example, sending output to a display). If a high-priority task awakens, it will pre-empt the low-priority task and begin executing. However, if the high-priority task then tries to access the same shared resource, it will be blocked, the low-priority task will resume, and the high-priority task will only be able to continue when the low-priority task has finished with the resource. Although this is a form of priority inversion, it is needed to prevent uncontrolled accesses to shared resources.

Other forms of priority inversion may arise under certain scheduling algorithms. Several approaches are available for dealing with priority inversion, such as alternative scheduling mechanisms provided as a supplement to the vendor's Ada runtime executive, or stylistic guidelines for application programmers in composing tasks and assigning priorities. The stylistic approach has the benefit of portability; it does not require specific support from an Ada vendor's runtime executive.

The second part of this series described how you could program interrupt handling in Ada. In short, the challenge is to use Ada for interrupts but to avoid task-scheduling overhead. One approach is to differentiate between the immediate processing and the deferred processing associated with an interrupt. The CPU carries out immediate processing at hardware-interrupt-priority level where it performs hardware-specific actions. Deferred processing begins by invoking a "task entry" to an interrupt-handler task with the hardware-level interrupt's data.

An application programmer would want interrupt handling to be expressive and efficient, and have low interrupt latency. The programmer should be able to write interrupt handlers either in Ada or in assembly code; the time between the interrupt and the invocation of the user-supplied routine should be minimal; and the runtime system should also minimize the amount of time during which it disables interrupts.

Configurability and kernel interfaces

Configurability is the user's control over the target-system configuration; in particular, the matching of the runtime executive's software to the target board. Any facility for adapting the runtime executive should assume that the application programmer is familiar with the target board but not necessarily an expert on how the vendor's Ada runtime executive works. The programmer certainly should not have to modify the executive's source code. The availability of sample-board support *packages* illustrating how to configure the runtime system is essential. The user should be able to specify such configuration parameters as the amount of target RAM and such routines as simple (serial) host/target-communication routines, program-startup routines, console input-output routines, timer-management routines, and file and device input-output routines.

The configuration routines and the application code require access to a variety of low-level services, so a bare machine kernel should be available to perform functions such as installing interrupt handlers, obtaining absolute time, servicing an alarm expiration, reading a character from console input, and writing a character to console output.

Supplementing the bare machine kernel, a real-time kernel is also useful for low-level control over runtime behavior. An Ada package can provide the appropriate interface, including subprograms that enable and disable task scheduling, obtain or modify a task's priority,

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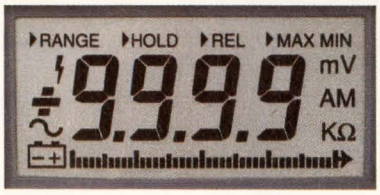

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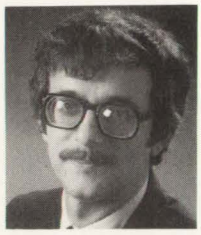
enable and disable interrupts, and read or write a byte from or to a port.

Ada provides a natural-language tool for real-time programmers, with features to express parallelism, interrupts, and low-level control. Its high degree of compile-time checking detects errors early. Language constructs alone, however, are not sufficient. To realize the potential benefits of Ada, users should check that compiler implementors meet hard runtime requirements in the areas of speed, compactness, capacity, predictability, and configurability. EDN

Author's biography



Benjamin Brosgol is vice president and technical director at Alsys Inc (Burlington, MA). He is in charge of the company's Ada training and consulting, has helped develop Ada compilers and computer-based training products, and is chairman of the Commercial Ada Users Working Group of the SIGAda professional society. Benjamin holds an MS and PhD in Applied Mathematics from Harvard University in Cambridge, MA, and is a member of both the IEEE and the Association for Computing Machinery.

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EDN's October 11, 1990, issue will feature a staff-written Special Report on video A/D converters. Part 3 of the real-time software programming series will discuss verbal and graphical requirements models for formulating operating-system behavior. EDN's DSP-chip directory will provide detailed descriptions of many DSP products. And we will preview the 1990 Electronica show.

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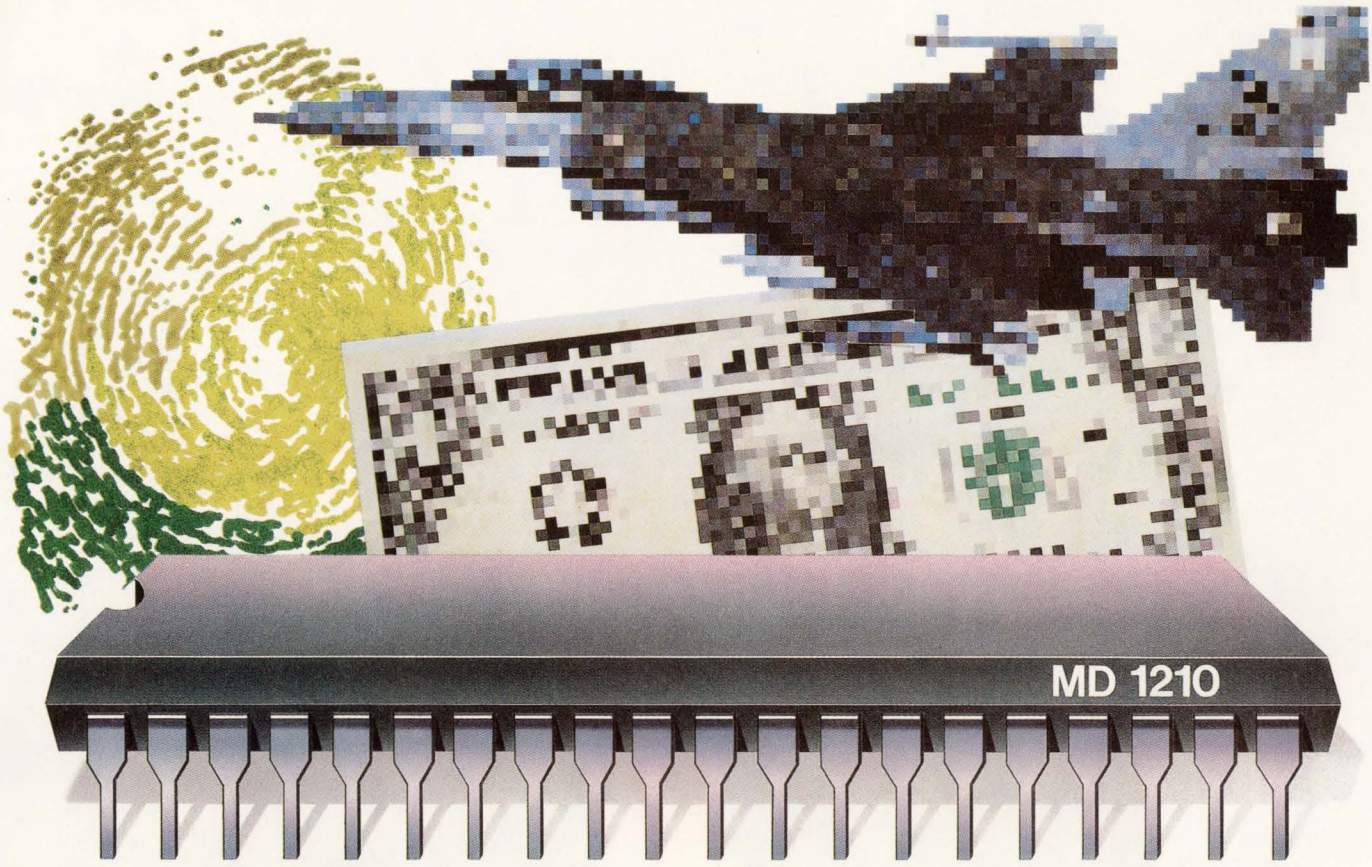

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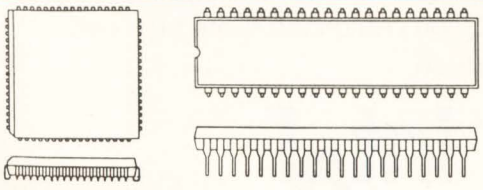

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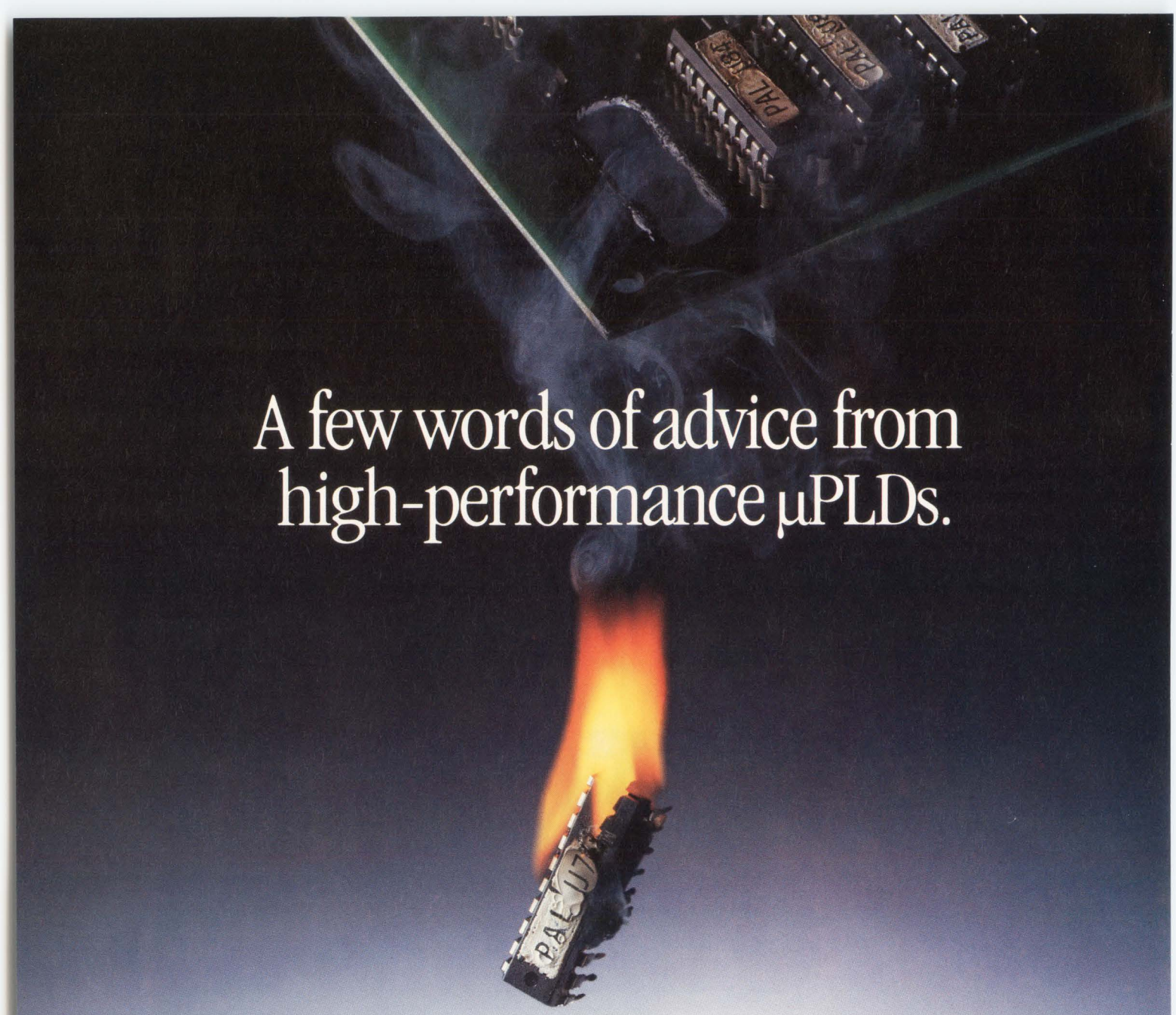

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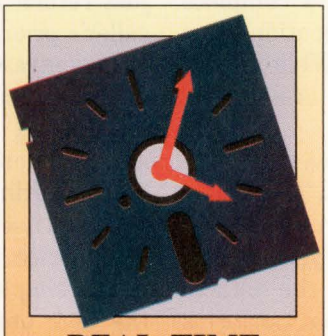
The multitasking mindset meets the operating system

Part 2 of this series delves further into the nature of real-time programming. It addresses some of the concerns that are unique to real time and describes how the programmer and the operating system handle these concerns.

David L Ripps, *Industrial Programming Inc*

One of the most difficult aspects of real-time work is getting into the right mindset. You must become accustomed to multitasking: to thinking in terms of multiple threads of execution running in parallel. An interrupt can occur between any two instructions within a task. This may require the operating system (OS) to suspend the currently executing task and start another. The suspension and later resumption are handled completely by the OS; they are "invisible" to the task. Nevertheless, this discontinuity can have several important side effects.



REAL-TIME PROGRAMMING PART 2

In a real-time application, the arrival of an interrupt is normally random with respect to the portion of code that happens to be executing. The interrupt must be serviced. This delays the interrupted code. As a result, the execution time for any portion of task code may be unpredictable. This is true even if the time to perform a given line of (uninterrupted) application code or to supply a given OS service is perfectly predictable. Random variations in performance are inherent in the nature of real-time programs.

Furthermore, under certain conditions, the small variations due to random interrupts can magnify into chaotic behavior. Suppose ordinarily there is barely enough time to perform some sections of a cyclic or repetitive application. Suppose, further, that the program takes a different path when one of these precarious sections is unable to finish in time. On most cycles, there is sufficient time and the program follows its normal path. Occasionally, an unfortunate combination of interrupts causes a time out and then the program diverges onto an alternate path. This variation, in turn, can affect the timing on the next cycle. The result can be a radically different pattern of behavior generated by a very small variation in the arrival time of an interrupt. For a discussion of chaotic phenomena in real time systems, see "Inner Rhythms" in James Gleick's book on chaos **(Ref 1)**.

A second side effect of a multitasking organization concerns any alterable data that is shared at the task level. Consider a concrete example. Task **U** is performing some calculations with a set of shared, alterable data. Without any warning, **U** is preempted by task **P**, which happens to be another user of the same data. If **P** were permitted to change the data, the results of the calculations performed by **U** would become unreliable.

The solution to such problems cannot be to disable interrupts. That technique can lead to the loss of any short-lived data whose arrival is signaled by an inter-

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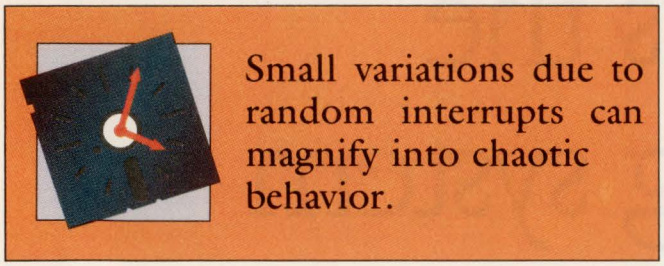
rupt. Nor can the general solution be to raise a task to the highest level of urgency so that no other task can pre-empt it. In a single-processor system, only one task can protect itself by being most urgent. In a multiprocessor system (that is, a system with two or more processors executing task code), even the most urgent



task may find itself sharing data with a less urgent task that is executing on another processor.

Luckily, there are facilities within a real-time operating system that enable a task to block temporarily other users of the same data (see the discussion of semaphores and controlled shared variables later in this article). But this is where mindset comes into play. The OS cannot automatically set up this type of protection. The designer of the task code must remember to ask for the protection before the first access of the data and must remember to release the protection after the last access.

Coordination and communication

Part 1 of this series defined a task as a complete program that is capable of independent execution. This is true, but it needs further refinement. While a task is *physically* complete and executable, it is not *logically* independent of the other tasks.

Each task performs a small part of the overall application, working in parallel with other tasks. At various points, the tasks must coordinate their activities. For example, a task that does an initial analysis of raw data must wait for the task that captures the data to build a complete set of values. The task that performs a deeper analysis, in turn, must wait for the results of the preanalysis. Similarly, when several tasks output reports on a shared terminal, each must wait until it can have exclusive access to the device. Otherwise, the intermixed display might be unintelligible.

Thus, tasks are not independent; they share common goals, common data, and common hardware. As a result, they must rely heavily on the OS to coordinate their individual executions. Planning the way tasks will coordinate and communicate is a major part of the design of a real-time application. These two concepts, coordination and communication, are common threads that are woven throughout the services provided by a real-time operating system.

Coordination and synchronization

Coordination is the blocking of a task until some specified condition is met. With this broad a definition of coordination, a task can coordinate with physical events as well as with itself and other tasks. For example, when a task pauses, it is blocked until the specified time elapses. The task is therefore coordinating with the physical clock.

Often a task coordinates with another task; the condition that task **W** is waiting for is set by another task, **C**. As you will see later, it is even possible for a task to become unblocked by a set of conditions that are supplied jointly by one or more tasks and by a physical device (the clock). Thus, coordination is a very general term for any self-imposed (that is, requested) suspension of the execution of a task. In every case, it is the OS that performs the requested suspension and eventual resumption of task activity.

The term "synchronization" is often applied to what this article is calling coordination. Some authors limit synchronization to task-to-task interactions and so would not apply the term to a pause.

Self-coordination

A few services provided by an OS are guaranteed to return immediately with the desired result; they never block the task. Examples are the services that just return information held by the OS, such as the caller's priority or the current time of day.

In contrast, any service that requires the allocation of a resource (such as memory) or that needs a task-level object to be free may be delayed until the resource or object becomes available. Such services involve coordination. In this case, the task is coordinating with itself, or more precisely, with the completion of a service it itself requested.

The simplest way to coordinate is merely to block the task until the service is finished. And in many cases, the simplest is best, especially if the task cannot perform further work until the service is done. Most real-time operating systems provide this coordination mode.

The problem with waiting until a service is completed is that there is no guarantee that the service will ever be completed or that the waiting time will not compromise other more urgent aspects of the task's work. Many critical real-time applications cannot risk any uncontrolled waits. Thus, the operating system, MTOS-UX, permits the basic coordination mode to be augmented by a maximum wait time. If the request

cannot be processed within that time, the request is timed out and the task continues. If this occurs, the OS informs the task of the failure. The interval can be zero to provide "fail unless immediately available."

"No coordination" is another mode that is available for many services. In this mode, the OS permits a task to send a message with no coordination if the sender does not care when the message is received.

Finally, there are times when a task needs a service performed but would like to defer coordination until later. Suppose task **R** wants to have three other tasks started now, but would also like to continue to do other work. Upon the completion of that other work, **R** is willing to wait for the termination of the three tasks it started. Such deferred coordination is permitted under MTOS-UX through the event flag machinery. As you will see later in this article, each start request would specify a different local event flag, an internal bit that can be set when the service is completed. Later, task **R** would ask the OS to block it until all three bits have been set.

Communication

Communication is the transfer of information between tasks. I/O covers the transfer of information between the external world and a task. Communication can proceed directly from one task to another. For example, when task **S** starts task **T**, **S** can transmit an argument to **T** (just as the caller can pass an argument to a procedure). Often, however, communication is best mitigated by a separate object, called a message exchange. This is a public queue to which any task can send a message and from which any task can receive a message.

Commonly, communication involves coordination. It is unusual to seek a message and not wait for it to arrive. However, the sender of a message may not need to wait for it to be received.

OS objects and their functions

A real-time operating system is an object-oriented program. The primary objects it deals with are executable objects (tasks), communication/coordination objects (message exchanges, event flag groups, semaphores, and controlled shared variables), and I/O objects (peripheral units). Objects can be created and destroyed. Each object has a set of functions that apply only to that class of objects. You can start a task executing; it is erroneous to request a message exchange to start executing.

One measure of the richness of a real-time operating system is the number of distinct types of objects it provides and the number of manipulations on those objects that it permits. By that measure, the illustrative OS chosen for this series of articles (MTOS-UX) is a very rich system. The objects and service functions supported by MTOS-UX are summarized very briefly in the next eight sections of this article. Each synopsis is greatly expanded in a later part of this series.

crtsk	Create task.
start	Start given task.
tstart	Start given task and transfer coordination to new task.
contsk	Connect given task to interrupt.
setpty	Set current priority of given task.
exeprc	Set (or reset) processor on which requesting task can execute.
getkey	Get key of given task.
gettid	Get identifier of task with given key.
getdad	Get address of data segments of requesting task.
exit	Terminate requesting task (without automatic restart).
trmrst	Terminate task with automatic restart after given interval of time.
dltsk	Delete requesting task.

Fig 1—Task control is a basic function of the operating system.

Task control services

One task can create another task. The creator specifies the basic attributes of the new object: its entry point, stack size, default priority, and so on. A newly created task is not yet executing; it is Dormant.

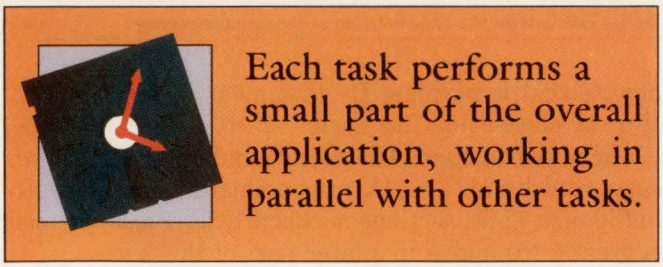
Any task (**R**) can request that any task (**T**) start executing. **R** can select the priority with which **T** will begin to run. **R** can pass an argument on to **T**. **R** can indicate what should happen if **T** is already executing, and thus cannot be restarted immediately. The choices are: (1) to queue the restart request or (2) to abort it. Finally, **R** can specify if it will: (1) continue to execute in parallel with **T**, (2) wait until **T** starts because of this request (in case **T** is not immediately available for restart), or (3) wait until **T** both starts and terminates because of the current request. As Part 4 will explain, there are cases in which all three types of coordination are required.

A task can dynamically change its own priority. It can also change the priority of another task. When a task finishes executing, it can simply terminate. This makes the task available for restart by another task. Alternately, a task can terminate now and be automatically restarted at a specified future time. This latter option is needed for cyclic tasks that perform some action periodically. In many real-time applications, tasks persist for the entire life of the system. Nevertheless, a task can request to be both terminated and then deleted. **Fig 1** provides a complete list of task services; the primary discussion will appear in Part 4 of this series.

Event Flags

Event flags broadcast information that can be employed in intertask coordination. Any task can create a public-event flag group. Each group contains 16 bits that can be independently set or reset by any task.

The individual bits represent information that is meaningful to the application. For example, setting bit 2 in group 'PNTS' might mean that the printer has been installed. (Any such logical significance of the bits is unknown to the OS, which just views the event flag group as 16 alterable bits.)



Any task can wait for an AND or OR combination of the bits within a given group. If an AND combination is specified, *all* of the selected bits must be set before the task continues; if an OR combination is specified, the task continues when *any* of the selected bits is set.

When a bit is set, all tasks whose AND or OR conditions are now satisfied become unblocked simultaneously. The task that sets a bit need not know the specific identities of the tasks that will use the information. Correspondingly, the task that uses the information does not have to know which task or tasks supply it. Thus, event flags are a mechanism for disseminating information to any or all tasks that may wish to know it.

Event flag bits remain at the last value supplied by a set or reset service call. The act of continuing a task that has been waiting for an event flag to be set does not automatically reset the bit. In other words, event flag bits are not "consumed" by being used for coordination. **Fig 2** lists event flag services; the primary discussion will appear in Part 7 of this series.

Semaphores and controlled shared variables

Tasks often share groups of alterable data, such as a set of variables that is maintained jointly by two tasks, **A** and **B**. While **A** is working on the data, **B** must not be allowed to alter any of the variables, and vice versa.

Semaphores are a traditional means to protect shared, alterable data. A task creates a semaphore for a given set of data. Thereafter, every task that needs access to the data first requests the OS to block it until the semaphore is free. If the semaphore is already free, the task continues; otherwise the task waits. Waiting for the semaphore is equivalent to waiting until no other task has access to the same data. When the task that has the semaphore is finished with the variables, it asks the OS to release the semaphore. If any tasks are waiting at that point, the most urgent one is then permitted to continue. If there are no tasks waiting, the semaphore is kept free until the next request for it.

Controlled shared variables (CSVs) are an extension of the simple semaphore concept. With a semaphore, a task can request only unconditional access to a given set of variables. All the OS requires is that the semaphore be free; the variables themselves do not have to satisfy any particular condition. With CSVs, a task can request that the exclusive access not occur until a specified relation between the variables is true. Thus, a task could stipulate that it needs exclusive access to the windows data for the system console, but only when a window of a given size is available. This extension avoids the inefficient task-level polling of the variables that would otherwise be required. **Fig 3** lists semaphore and CSV services; the primary discussion will appear in Part 9 of this series.

Message exchanges

Message exchanges facilitate communication among tasks. Any task can create a message exchange. Thereafter, any task can send a message to the exchange, and any task can receive a message from it. A message is queued at the exchange if no receiver is immediately available to take it. Directing messages to a separate

crefg	Create group of (global) event flags.
srsefg	Immediately set or reset event flags.
srslef	Immediately set or reset local event flags of given task.
sgiefg	Set event flags after given interval of time.
waiefg	Wait until event flags are set.
dlefg	Delete a group of (global) event flags.

Fig 2—Event flags broadcast information that is useful for task coordination.

Semaphores	
crsem	Create (counting) semaphore.
waisem	Wait for given (counting) semaphore to be free.
rlssem	Release semaphore.
dlsem	Delete semaphore.
Controlled Shared Variables	
crcsv	Create group of controlled shared variables.
usecsv	Wait for exclusive control over group of controlled shared variables.
waicsv	Wait for function of controlled shared variables to be true.
rlscsv	Release group of controlled shared variables.
dlcsv	Delete group of controlled shared variables.

Fig 3—Semaphores and controlled shared variables keep tasks from improperly altering shared data.

communication object (the exchange) makes it possible for multiple tasks to respond to messages held in a common queue. This design was inspired by the single line at a bank with several tellers.

MTOS-UX provides two different implementations of a message exchange. The first is called a mailbox. For this class of exchanges, there is no limit to the size of a message and no limit to the number of messages that can be queued awaiting a receiver. Both sender and receiver have full coordination capability, so that the sender can wait for the receiver and vice versa.

The second implementation is called a message buffer. It restricts messages to the size of an address (since the message is typically a pointer to a block of parameters or text). Each buffer has a finite capacity that is specified when the buffer is created. There are only two levels of urgency, equivalent to first-in, first-out and last-in, first-out queuing. The sender always deposits a message without coordination. If there is no message available, the receiver has only two coordination options: to return immediately without a message or to wait without limit for a message. Building in these fixed options—which are the ones most commonly selected when full coordination is available—makes the exchange services extremely fast. **Fig 4** lists message exchange services; the primary discussion will appear in Part 8 of this series.

Mailboxes

opnmbx	Open mailbox, creating it if it does not already exist.
sndmbx	Send message to mailbox.
rcvmbx	Receive first available message from mailbox.
clsmbx	Close mailbox.
dlmbx	Delete mailbox.

Message Buffers

crmsb	Create message buffer.
getmsb	Get identifier of message buffer.
putmsb	Post message to the beginning of buffer.
putmse	Post message to the end of buffer.
getmsn	Get message from buffer. Return if message is not available.
getmsw	Get message from buffer. Wait if message is not available.
dlmsb	Delete message buffer.

Fig 4—Mailboxes and message buffers facilitate communications among tasks.

Input/output

Input, output, and related functions provide a mechanism for communication between a task and the external world. This communication may be performed at the physical or logical level.

At the physical level, a task selects a particular device—a certain console, printer, disk drive, and so on—and performs a fully specified operation on that device. A typical function is to write a given block of text to a console or to read a given sector from a disk into a given input buffer. Once a task requests such a service, the OS performs all the details of the physical transfer, including handling any interrupts generated by the device.

Input and output can also be performed at the logical level via a file system. In this case, the task specifies a file, a function, and the associated input buffer or output data. The file system (not the task) determines the placement of the data on the disk. **Fig 5** lists physical I/O services.

Signals

A signal is a software interrupt that may be handled at the task level. Since a task can send a signal to another task, or to a group of tasks, signals are a means of intertask coordination or communication. A task may also elect to have a signal sent to itself upon completion of a requested service. Thus, signals are also a means of deferred coordination, an alternative to event flags. MTOS-UX defines 32 signals of which 17 are available for coordination or communication. The remaining 15 are dedicated to error recovery.

Each task selects its own response to the arrival of a signal. A common response is to execute a given task-level procedure and then return to the point of interruption. Other possibilities are: (1) to ignore the signal, (2) to terminate the receiving task, or (3) to halt the task and invoke the debugger to restart it. A task can determine its current responses and can alter them dynamically.

A task can pause until a signal arrives. It can also ask the OS to send a signal to itself or to another task after a given interval. Signal-handling capability is an inherent property of a task and need not be created. **Fig 6** lists signal services; the primary discussion will appear in Part 10 of this series.

Time and time of day

A task can pause for a given interval of time. During that time, the task is blocked from executing. The

Peripheral I/O

crpun	Create peripheral unit to run under given driver.
getstc	Get identifier of standard console for requesting task.
setstc	Install given unit as standard console of requesting task.
getuid	Get identifier of unit with given key.
pio	Perform I/O and related functions on given peripheral unit.

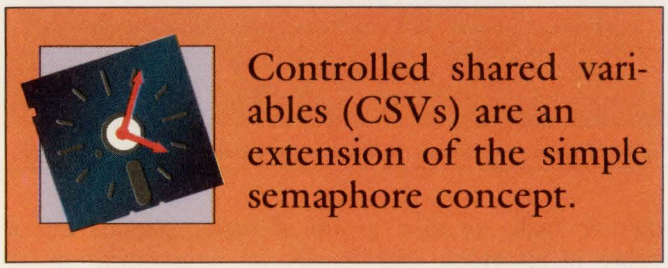
System

getidn	Get system identification data.

Fig 5—I/O functions provide communication between tasks and the external world.

pause can be canceled by another task that wants the task to resume immediately. To strengthen the use of pause/cancel-pause as a means of coordination, the original pause can be "forever."

Any task can submit an ASCII clock/calendar string to the OS. Thereafter, the OS will update the string every second. Any task can receive the current value of the string. A task can also pause until a given time of day. This can be a definite time, such as 12 noon, or an indefinite time, such as 30 minutes after the hour.



Various services have time-dependent options. For example, if requested to do so, the OS will set a given event flag after a specified interval or will send a given signal to a particular task after a specified interval. The option of limiting the wait for a service to a maximum interval has already been mentioned. So has the service that automatically restarts a periodic task. **Fig 7** lists time and time-of-day services; the primary discussion will appear in Part 6 of this series.

Shared-memory management

It is quite common for the sum of the maximum memory requirements of each individual task to far exceed the instantaneous needs of all the tasks taken together. For example, each of 20 tasks might need 10k bytes of work space at some time during their execution (for a theoretical worst-case total of 200k bytes). Yet, because of the way the memory needs are phased among the tasks, only 50k bytes are needed at any given time. These observations have led to the concept of memory sharing via pools.

A pool is a contiguous chunk of memory that is turned over to the OS to be allocated to individual tasks upon demand. The memory within each pool is divided into blocks of fixed size. MTOS-UX provides two types of pools. In one, a fixed-block pool, each allocation delivers exactly one block. In the other, a common memory pool, a task can receive a contiguous area of any desired size even if it spans several blocks.

With either type of pool, a task that seeks an allocation of memory that is currently not available is given the opportunity to wait until the request can be satisfied. All coordination options are available, including limiting the wait and deferring the coordination. **Fig 8** lists memory-pool services.

Invoking task services

In a traditional programming environment, OS services are requested via a procedure call. Consider the following C program, which outputs a message to the system console via a built-in service function.

```
inient ()
 {
  ...
  printf ("Application started\n\r");
  ...
 }
```

This program could be run under Unix, MS-DOS, or VMS. It also runs under MTOS-UX. In each case, the task need not be concerned with the details of how a given string is physically output. Physical I/O is the operating system's job.

MTOS-UX provides an implementation of the C formatted output function (*printf*), the character-oriented I/O functions (*getchar* and *putchar*), and some memory-allocation services (such as *malloc* and *free*). In these cases, the functions are completely specified in Kernighan and Ritchie (see Part 1 of this series, **Ref 2**).

Following this model, all OS services are requested

getsig	Get response to given signal.
setsig	Set response to one or more signals.
sndsig	Send signal to one task or group of tasks.
cansig	Cancel pending signals of requesting task.
sgisig	Send specified signal after given interval of time.
pausig	Pause until signal arrives.

Fig 6—Signal-handling functions allow task-level handling of software interrupts.

Time	
pause	Pause for given time interval.
canpau	Continue given task if it is paused for time interval.
getime	Get number of milliseconds since system was started.
Time of Day	
gettod	Get time of day clock/calendar string.
settod	Set time of day clock/calendar.
syntod	Wait for given time of day.

Fig 7—Time and time-of-day functions help with scheduling program actions.

by calling a corresponding service function, with options selected via call arguments. For example, function *pause* blocks a task for a specified interval. A 10-msec pause is requested by *pause* (MS+10), while *pause* (SEC+9) blocks for 9 sec. (A header file, MTOSUX.H, supplies the numeric value of literals such as MS and SEC.) The following program demonstrates the natural way in which standard C and proprietary OS functions are intermixed in a typical task.

```
#include "MTOSUX.H"          /* file of basic OS definitions */

inient ()
 {
  register long int time;

  do
   {
    printf ("\n\rEnter 1-9. Bell sounds after that many seconds: ");
    time = getchar ();              /* get users response */
    putchar (time);                 /* echo back */
    time -= '0';                    /* convert to binary */
   }
  while ((time < 1) || (time > 9));
  pause (SEC+time);                 /* pause for given interval */
  printf ("\07\n\rPause over.\n\r");
 }
```

Typical OS services: manipulating task priority

Looking at task priority will further illustrate how a task invokes OS services. The OS employs the task attribute *current priority* to allocate any shared resource for which demand exceeds supply. The range of the current priority is 0 to 255, with 255 being the most urgent and 0 being the least urgent. The allocation algorithm is simply that the highest-priority task gets the resource. First-come, first-served applies in case of equality. The resources include access to processors, peripheral units, allocated memory, messages, semaphores, and controlled shared variables.

There is no limit to the number of tasks at each level. At one extreme, all tasks may have the same priority; at the other extreme, all have different priorities.

The current priority is dynamic. A task may ask to have its priority changed to a given value, say, 125, via

```
#define mine 0L

setpty (mine, USEVAL, 125L);
```

A value of 0 (*mine*) within the first argument specifies that the priority of the caller is to be changed. (By supplying the identifier of a task in place of the 0, *setpty* can be used to change the priority of another task, but that is getting ahead of the story.) The priority may also be increased by a given amount (with a clamp at 255),

```
setpty (mine, ADDVAL, 10L);
```

or decreased by a given amount (with a clamp at 0).

```
setpty (mine, ADDVAL, -10L);
```

Almost all service procedures return a value to the requesting task. If one of the parameters is inappropriate, the function returns the value BADPRM (which is defined in MTOSUX.H as −1). If the parameters are correct, *setpty* returns the new value of the task priority, as an unsigned short integer. Thus, a task can determine its current priority by adding a 0 to its priority.

```
mypty = setpty (mine, ADDVAL, 0L);
```

Common Memory Pools

crcmp	Create common memory pool.
getcmp	Get identifier of common memory pool.
alloc	Allocate contiguous area from common memory pool.
dalloc	Deallocate area taken from common memory pool.
dlcmp	Delete common memory pool.

Fixed Block Memory Pools

crfbp	Create fixed block memory pool.
getfbp	Get identifier of fixed block memory pool.
alofbp	Allocate one block from fixed block memory pool.
dalfbp	Deallocate block taken from fixed block memory pool.
dlfbp	Delete fixed block memory pool.

Fig 8—Memory-allocation functions allow tasks to share a common memory pool.

Changing priority in alternate OSs

To be concrete, all of the preceding examples were drawn from the same OS. Nevertheless, they illustrate the almost universal techniques for obtaining services from a real-time OS. Note the similarity with the service to set priority within the proposed Microprocessor Operating System Interface (MOSI) standard (MOSI87, Sections 7.3 and E.7.2 (C binding)),

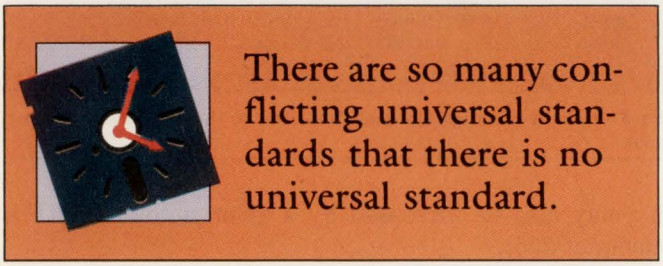
```
void oschpri (process_id, new_priority, &error);
```

where *process_id* selects the target task (process) and *new_priority* is the new priority value. A value of −1 for the latter indicates the default priority, and a value of 0 provides the largest allowable priority for that task. The meaning of other values is implementation dependent. The function does not return a value (is "void").

A corresponding function appears in the standard proposed by the IEEE (Realtime Extension for Portable Operating Systems (POS88, Unapproved Draft 2, Section 4.2.1)).

```
int rt_setpriority (pid, prio);
```

Here *pid* selects the target task, with 0 designating the caller, and *prio* is the new priority value. The new priority value is bound to a range associated with the current scheduling policy for the system. Negative values are specifically forbidden. The exact semantics of *rt_setpriority* are implementation dependent, including questions of appropriate privilege to change the priority of another task. Upon success, the function returns the former priority of the selected task.



There are even more OS "standards" that have been proposed or are still being developed. In addition to the efforts mentioned above, the VMEbus International Trade Association (VITA) is standardizing on the Open Real-Time Kernel Interface Definition (ORKID), Motorola is offering to make its Real-Time Executive Interface Definition (RTEID) a universal standard, and the Japanese are promoting The Real-Time Operating System Nucleus (TRON) as a world standard.

While the main point of this discussion is to show how services are obtained from an OS, the painful lack of agreement on even a simple service becomes apparent. There are so many conflicting universal standards that there is no universal standard. Furthermore, in many cases vital semantic details of the standard service functions are "implementation dependent." Thus, these standards are not even fulfilling their goal of promoting portability of real-time applications. An application behaves differently with different implementations of even the same standard.

The next program provides further examples of how OS services are invoked and shows how two tasks may cooperate to attain a single goal. That goal is the measurement of the idle time within an application.

```
#include "MTOSUX.H"

#define MAXTLY 2189460;  /* maximum value of tally for no tasks
                            running */

static long tally;       /* number of loops performed in
                            sample period */

smpent ()                /* sampling task: */
  {                      /* this must be the only task at
                            priority 0 */

    while (1)
      ++tally;           /* increment tally, which is reset by
                            reporting task */
  }


prtent ()                /* reporting task */
  {                      /* this must be the only task at
                            priority 255 */

    register long pcidle;      /* percent idle */

    while (1)
      {
        tally = 0;             /* clear tally, which is incremented
                                  by sampling task */
        pause (1+SEC);         /* pause during sampling period */
        pcidle = 100*tally/MAXTLY;   /* compute percent idle */
        printf ("Percent idle = %ld\n\r", pcidle);
      }
  }
```

The OS attempts to keep the processor busy all the time. Some processor time must be spent performing requested services, handling clock and peripheral interrupts, and doing similar housekeeping chores. All remaining time is potentially available for task work.

Companion disk offer

You can run all of the C examples in this series, plus applications of your own, on a PC computer with a set of demonstration disks available from Industrial Programming Inc. The disks contain a version of MTOS-UX for an IBM PC/AT or compatible. An application program is edited, compiled, linked, and loaded under MS-DOS. The MTOS-UX then takes over the hardware to execute the program in real time. At any time, you can enter an alt/dlt command to return control to MS-DOS.

The demonstrator requires an AT with a least 512k bytes of RAM and a hard disk with 2M bytes available for MTOS libraries and scratch storage. Program preparation requires the Microsoft C compiler/linker, version 5.0 or later. Microsoft tools are not included with the MTOS-UX demonstrator.

The demonstration version has all of the features and facilities of standard MTOS-UX. However, there is a limit of six of each type (six tasks, six mailboxes, six semaphores, and so forth). The disk set costs $25; unlimited versions are also available. For more details, call the IPI sales department at (800) 365-6867.

As long as there is any Ready task, the OS will let it execute. The processor falls idle only if all tasks are Blocked or Dormant.

We know that tasks always run in priority order. As a result, we can use a pair of tasks to measure the fraction of the potential task time that is unused during a sample period of, say, 1 sec. The sampling task (*smpent*) runs at the lowest priority and must be the only task at priority 0. It is always Ready. Because of its low priority, it runs only when there is no other Ready task. The sampling task just sits in a loop, incrementing a static variable, *tally*.

A second task (*prtent*) calculates and reports the results. This task runs at the highest priority level, 255. First it clears *tally* to 0, and then it pauses for the sampling period of 1 sec. At the end of the pause, it computes the percentage idle time as 100 times the actual value of *tally* divided by the maximum possible value, *MAXTLY*. *MAXTLY* is previously determined by noting the value of *tally* when no other tasks are permitted to be Ready during the sampling period. In this example, the percent idle time is reported directly; in practice, the values could be smoothed by numerical averaging before being reported.

To sum up, a real-time program consists of a set of parallel threads of execution (tasks) that are subject to random interruptions and preemptions. The consequences of such an organization must be constantly in the mind of the application programmer.

At times, the individual threads of execution must also be connected so they can cooperate to accomplish a common goal using common data, resources, and equipment. The OS provides the required coordination and communication services. The OS also permits the tasks to exercise control over their own execution and that of their fellow tasks. A task requests an OS service via a set of predefined functions. These are modeled after standard functions, such as C's *printf*. All high-level languages have equivalent function-calling facilities.

The major thrust of this series of articles is how to write a real-time program. But, before you can write a program, you must know what that program is supposed to do. Part 3 will discuss the development of real-time requirements as a first step toward program development. EDN

Reference

1. Gleick, J, *Chaos*, Penguin Books, New York, 1987.

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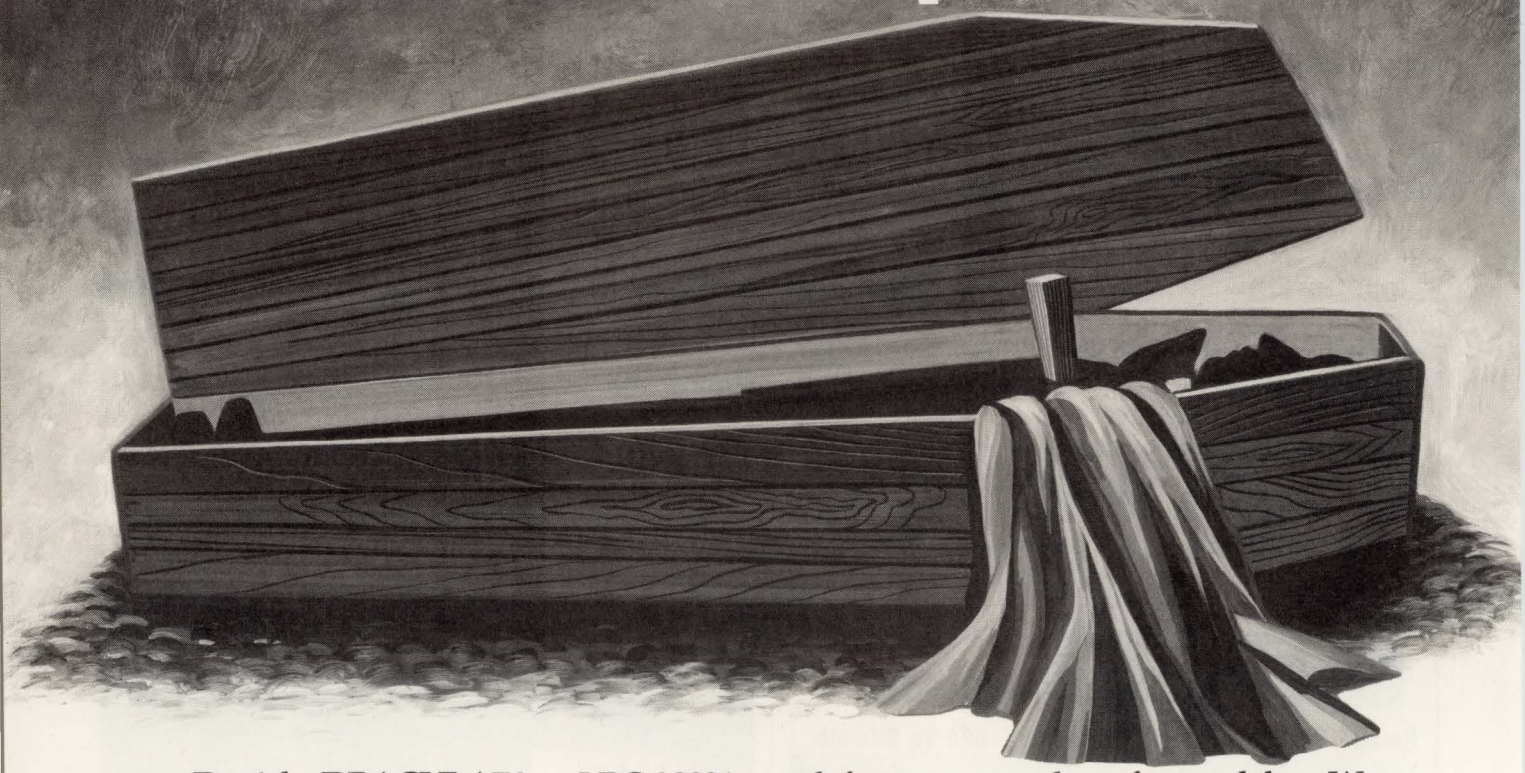

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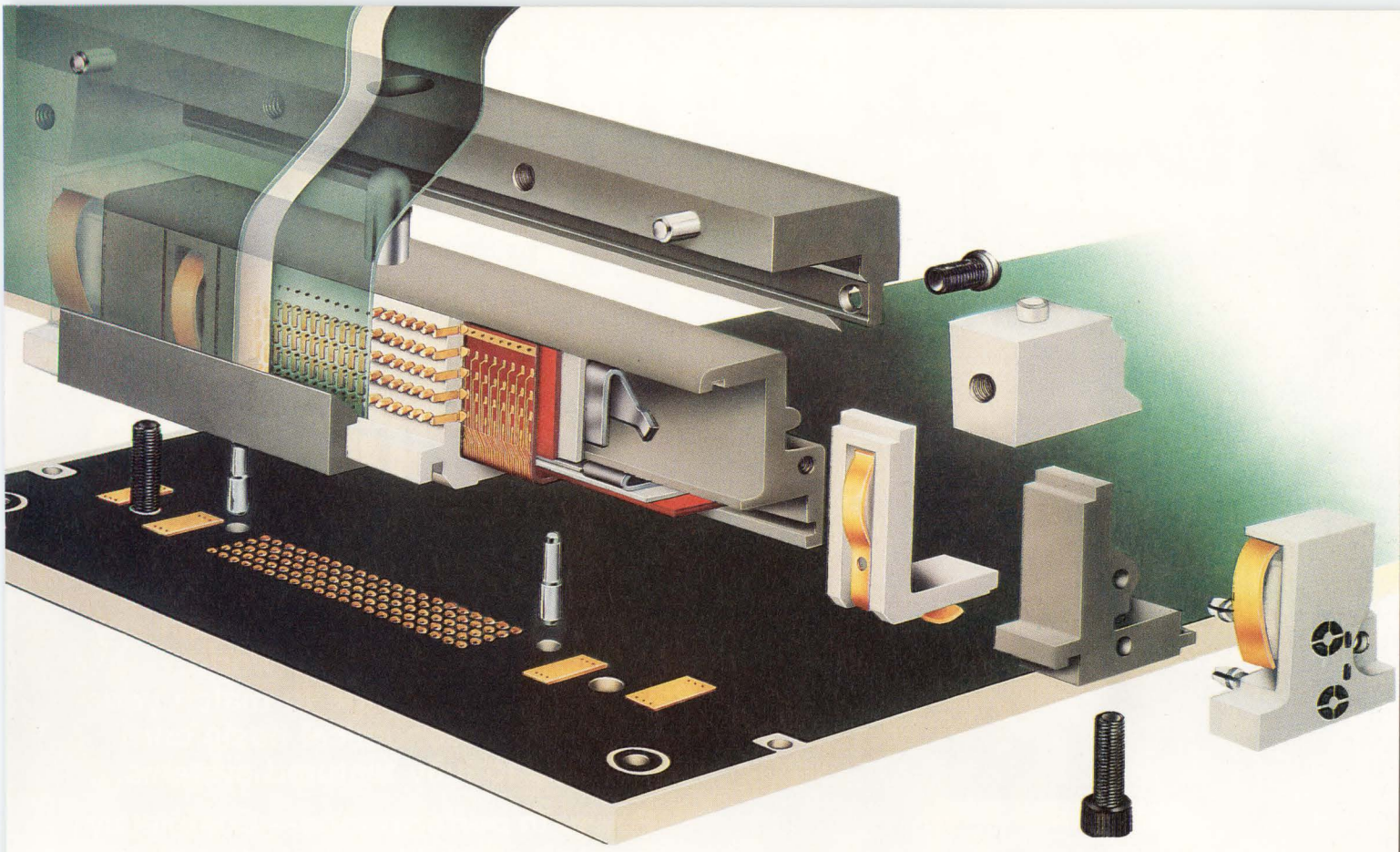

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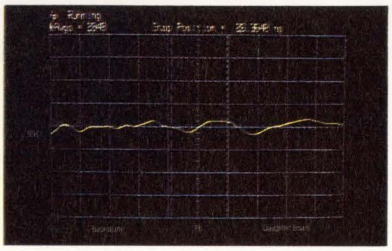

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CIRCLE NO. 73

EDITED BY CHARLES H SMALL

Scrambler disguises voice signals

Francesco Ruggiero
Consultant, Dallas, TX

The simple digital circuit in **Fig 1** incarnates a well-known audio-scrambling algorithm. Briefly, the scrambling begins with digitizing a bandlimited audio signal. Next, every other digital sample's sign bit gets complemented. When reconstructed, this scrambled signal contains the original signal's spectrum flipped around one-fourth of the sampling frequency. The resulting signal will be unintelligible.

Thus, for a signal bandlimited to 4 kHz and sampled at 8 kHz, the resulting spectrum will be flipped around 2 kHz, effectively interchanging the high and low portion of the audio spectrum. But, passing the scrambled signal back through the scrambler again restores the signal to its original form. In other words, the process is its own inverse.

The circuit's XOR gate complements every other sign bit while the TP3054 codec/filter combo handles the digitizing and reconstruction chores. To curtail distortion, limit the input level to 2.5V.

(EDN BBS DI #891) EDN

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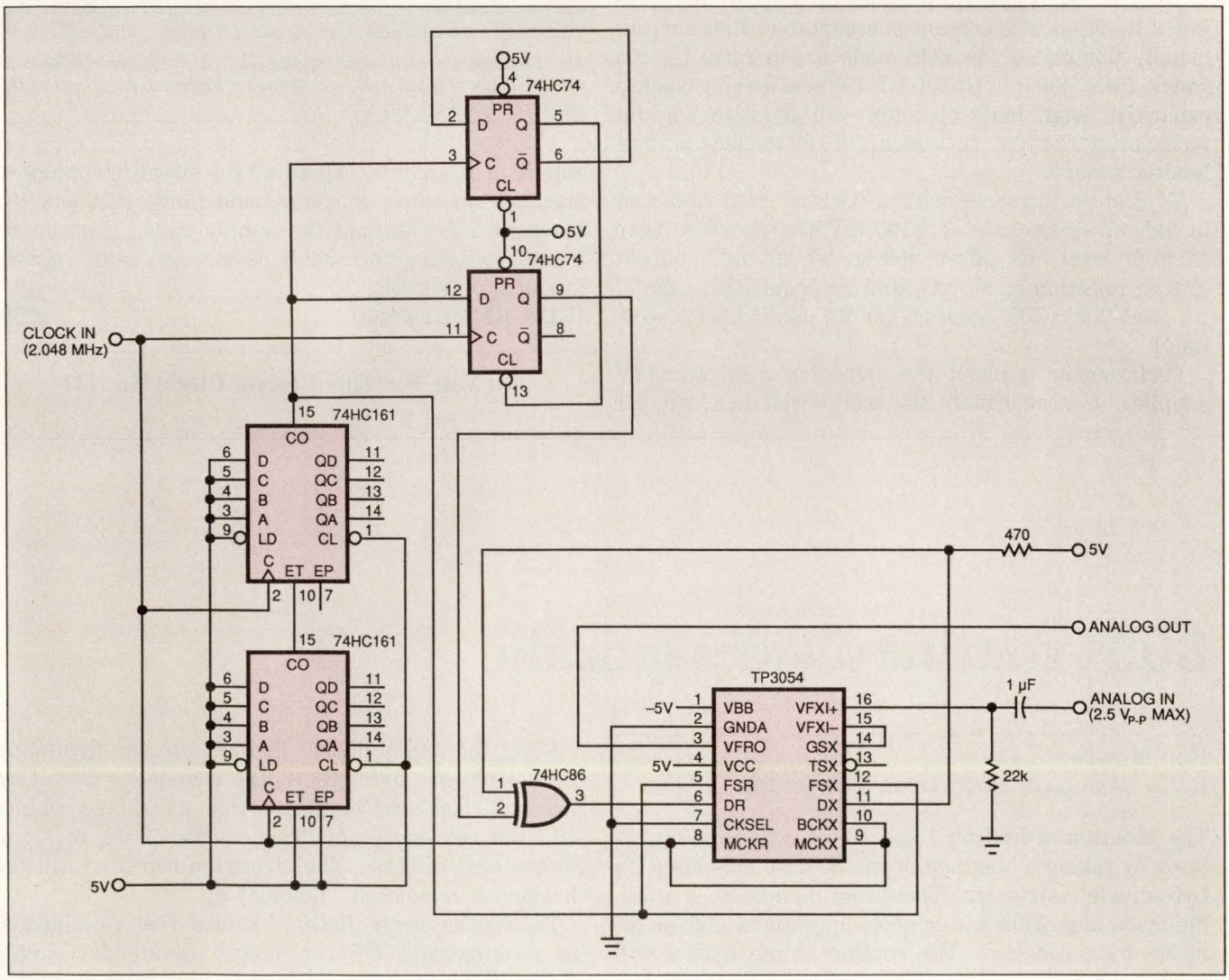


***Fig 1—This circuit can both scramble** and unscramble an audio signal.*

S/H circuit multiplexes op amp

Tarlton Fleming
Maxim Integrated Products, Sunnyvale, CA

The sample-and-hold (S/H) circuit in **Fig 1** costs only $3.50 (1000) because it switches its single op amp between two functions. The op amp buffers the input (V_{IN}) while the circuit is in sample mode and buffers the hold capacitor, C_H, while the circuit is in hold mode.

The two digital inputs are compatible with TTL and CMOS logic levels. Input $\overline{S}$/H controls the circuit's operating mode (low is sample), and $\overline{DISCH}$ is an optional control input whose low state commands a rapid and complete discharge of C_H.

You can use a general-purpose op amp for IC_1, provided its input bias current is acceptable. Bias current usually dominates the hold-mode droop rate. C_H can range from 100 pF to 0.1 μF. When driving such a capacitive load, most op amps will oscillate without an isolating resistor, such as R_1, of 100 to 200Ω in their feedback loops.

Typical performance with a 0.01-μF hold capacitor includes a droop rate of ≤100 mV/sec, aperture time of ≤100 nsec, an offset voltage of ≤5 mV, output charge injection of ≤5 pC, and an acquisition time of ≤1 μsec (for ±10% accuracy) or ≤5 μsec (±0.1% accuracy).

Performance is about the same for ±15 or ±12V supplies, and the system also works well on a unipolar supply of 10 to 30V. Whatever the supply's configuration, the op amp's common-mode range restricts V_{IN} to about 2V less than the supply rails. The control inputs' switching thresholds remain the same regardless of supply levels.

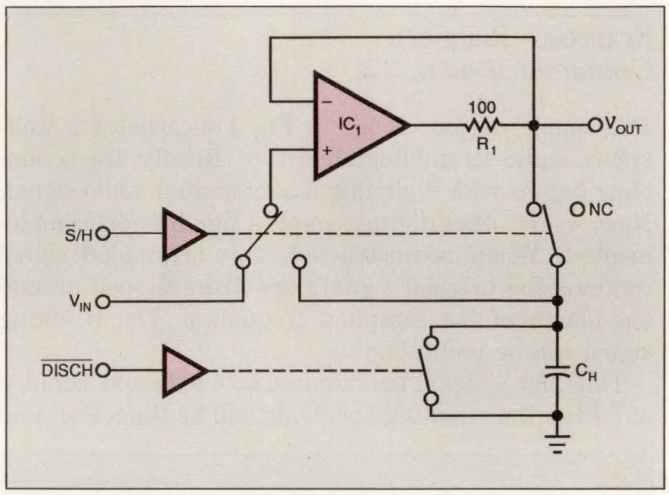


Fig 1—Elements of a quad analog switch *hardware-multiplex an op amp between input and hold-capacitor buffering functions in this economical S/H circuit.*

(EDN BBS DI #888) EDN

To Vote For This Design, Circle No. 747

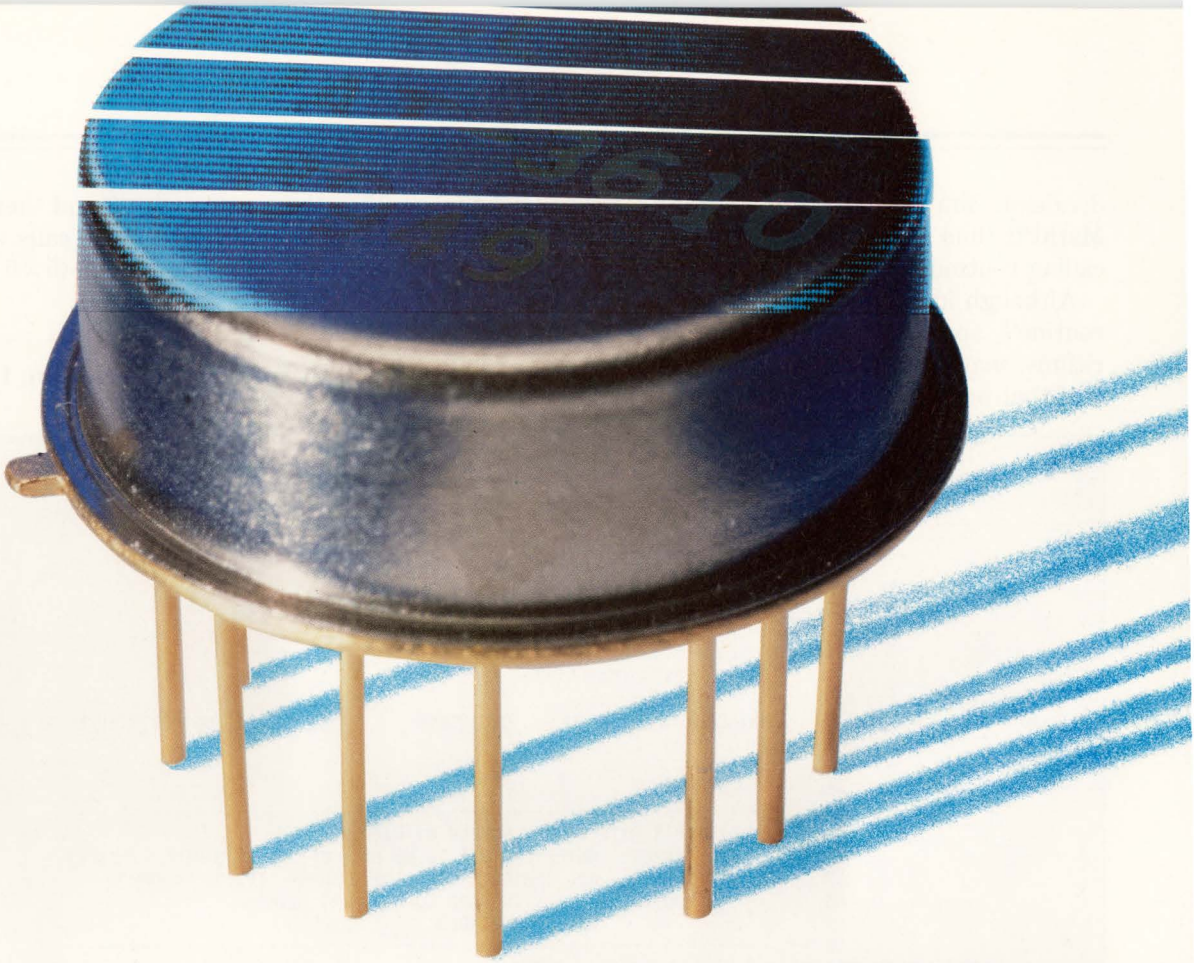
8051 routine divides quickly

Ron Mowrer
Rocky Mountain Instrument, Thermopolis, WY

The program in **Listing 1** speeds some division operations by taking advantage of the 8051 single-chip μP's byte-divide instruction. This program embodies a nibble-mode algorithm and handles operations such as division by a constant. The routine in the **listing** will work with any number of bytes in the dividend but restricts the divisor's range to 4 bits or less.

First, the nibble divisor divides into the dividend's most-significant byte. Next, the remainder from that division (which is never greater than a nibble) combines with the next-most-significant *nibble* of the dividend for the next division. The algorithm repeats until the dividend is completely "nibbled" up.

The routine in the **listing** handles 3-byte dividends. To accommodate different-length dividends, simply change the loop counter's initial value from 2, in line 165, to one less than the total number of bytes in your



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1.5	0.32	3.0	0.4	9.0	0.6	15.0	0.6
2.0	**0.2**	**4.0**	**0.3**	**10.0**	**0.3**	**20.0**	**0.4**
2.5	0.32	5.0	0.5	13.0	0.6	25.0	0.7
3.0	0.4	6.0	0.5	16.0	0.6	30.0	0.7
3.5	0.52	7.0	0.7	19.0	0.9	35.0	1.0

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dividend. You can alter the routine to either load the MathPtr (line 157) and byte count directly, or have the calling routine pass these parameters to this routine.

Although ideal for such tasks as dividing by 10, the routine's speed, compared to normal division algorithms, makes it attractive for dividing by larger divisors that break down into nibble divisors. For example, calling the routine with 5 and then 7 will equal a division by 35 (5×7) and three calls with a divisor of 5 is the same as dividing by 125 ($5\times5\times5$).

(EDN BBS DI #890) EDN

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Listing 1—Fast nibble-mode division routine

```
                    001     $ INCLUDE (REG451.PDF)
              =1    002 +1  $ NOLIST
                    136
                    137     PUBLIC  DivNib
                    138     EXTRN   DATA (MathPtr)
                    139
0010                140     MathBank        EQU     00010000B       ;PSW VALUE FOR REGISTER BANK 2
                    141
                    142     USING 2
                    143
                    144     ;---------------------------------------------------------------
                    145     ;  DIVIDE 3 BYTE BINARY NUMBER BY NIBBLE
                    146     ;       INPUT:  MathPtr = PTR TO MS BYTE OF 3 BYTE DIVIDEND/RESULT
                    147     ;               ACC = NIBBLE DIVISIOR ( 1H <= DIVISOR <= OFH )
                    148     ;       OUTPUT: RESULT IN SAME LOCATION AT MathPtr
                    149     ;               ACC = REMAINDER
                    150     ;---------------------------------------------------------------
                    151
                    152     DivNib:
0000 C0F0           153             PUSH    B               ;SAVE B & PSW REGISTERS ON STACK
0002 C0D0           154             PUSH    PSW
0004 75D010         155             MOV     PSW,#MathBank   ;SWITCH TO REGISTER BANK 2
0007 FB             156             MOV     R3,A            ;STORE NIBBLE DIVISOR
0008 A800      F    157             MOV     R0,MathPtr      ;R0 NOW PTR TO MS BYTE OF DIVIDEND (& EVENTUAL RESULT)
000A 7912           158             MOV     R1,#12H         ;R1 NOW PTR TO R2 THIS BANK SO CAN USE NIBBLE XCHD INSTRUCTION
000C E6             159             MOV     A,@R0           ;GET MS BYTE OF DIVIDEND
000D 8BF0           160             MOV     B,R3            ;PUT NIBBLE DIVISIOR IN B
000F 84             161             DIV     AB
0010 85F012         162             MOV     12H,B           ;MOVE REMAINDER TO R2 SO CAN USE NIBBLE EXCHANGE IN LOOP
0013 F6             163             MOV     @R0,A           ;MS BYTE NOW DONE, STORE IN DIVIDEND/RESULT
0014 08             164             INC     R0              ;BUMP PTR TO NEXT MS BYTE OF DIVIDEND
0015 7F02           165             MOV     R7,#2           ;LOOP COUNTER FOR REMAINING BYTES OF DIVIDEND
                    166     DN1:
0017 E6             167             MOV     A,@R0           ;GET NEXT BYTE OF DIVIDEND IN ACC (WE ONLY NEED MS NIBBLE)
0018 D7             168             XCHD    A,@R1           ;PUT REMAINDER STORED AT R2 IN LO NIBBLE OF ACC
0019 C4             169             SWAP    A               ;NOW REMAINDER IS IN HI NIBBLE OF ACC & NEXT MS NIBBLE OF
                                                            ;  DIVIDEND IS IN LO NIBBLE
001A 8BF0           170             MOV     B,R3            ;DIVIDE AGAIN BY DIVISOR NIBBLE
001C 84             171             DIV     AB
001D 85F012         172             MOV     12H,B           ;AGAIN SAVE REMAINDER TO R2 THIS BANK FOR LO NIBBLE EXCHANGE
0020 C4             173             SWAP    A               ;PUT NIBBLE RESULT IN HI NIBBLE AND STORE IN DIVIDEND/RESULT
0021 C6             174             XCH     A,@R0           ;  WHILE RETRIEVING ORIGINAL DIVIDEND BYTE (WE ONLY NEED LS
                                                            ;  NIBBLE)
0022 C4             175             SWAP    A               ;LS NIBBLE OF DIVIDEND BYTE TO HI NIBBLE OF ACC FOR XCHD
0023 D7             176             XCHD    A,@R1           ;REMAINDER TO LO NIBBLE OF ACC
0024 C4             177             SWAP    A               ;SWAP REMAINDER TO HI NIBBLE FOR NEXT DIVIDE
0025 8BF0           178             MOV     B,R3            ;DIVIDE AGAIN BY DIVISOR NIBBLE
0027 84             179             DIV     AB
0028 85F012         180             MOV     12H,B           ;AGAIN REMAINDER TO R2 THIS BANK FOR NIBBLE SWAP
002B D6             181             XCHD    A,@R0           ;STORE LO NIBBLE RESULT THIS BYTE IN DIVIDEND/RESULT
002C 08             182             INC     R0              ;BUMP PTR FOR NEXT DIVIDEND BYTE
002D DFE8           183             DJNZ    R7,DN1          ;FINAL TWO BYTES DONE?
                    184
002F 85F0E0         185             MOV     ACC,B           ;PUT NIBBLE REMAINDER FROM LAST DIVIDE IN ACC FOR CALLER
0032 D0D0           186             POP     PSW             ;RESTORE REGISTERS AND SWITCH BACK TO CALLERS REGISTER BANK
0034 D0F0           187             POP     B
0036 22             188             RET
                    189
                    190     END
```

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Inverters mimic interlocked switches

Tian Jin Qin
Shanxi Electronic Industry Research Institute, Taiyuan, China

The switching circuit in **Fig 1** acts like a bank of interlocked mechanical switches; pushing one of the buttons latches its corresponding output and unlatches any previously selected output. A pair of inverters forms a latch for each output.

Pressing button B_1, for example, applies a positive pulse, via resistor diode D_{1B}, to the input of the first output's, OUT_1, latch. This positive pulse will set OUT_1 high. Feedback locks OUT_1's pair of inverters in this high state. Meanwhile, the pulse will also pass through diode D_{1A} to the differentiator formed by C and R_2. The differentiator will shorten the pulse.

This shortened pulse goes to all the latches, resetting all of them *except* the latch that sees the longer setting pulse. Obviously, if you press more than one button at once, more than one output will latch at once.

(EDN BBS DI #889) EDN

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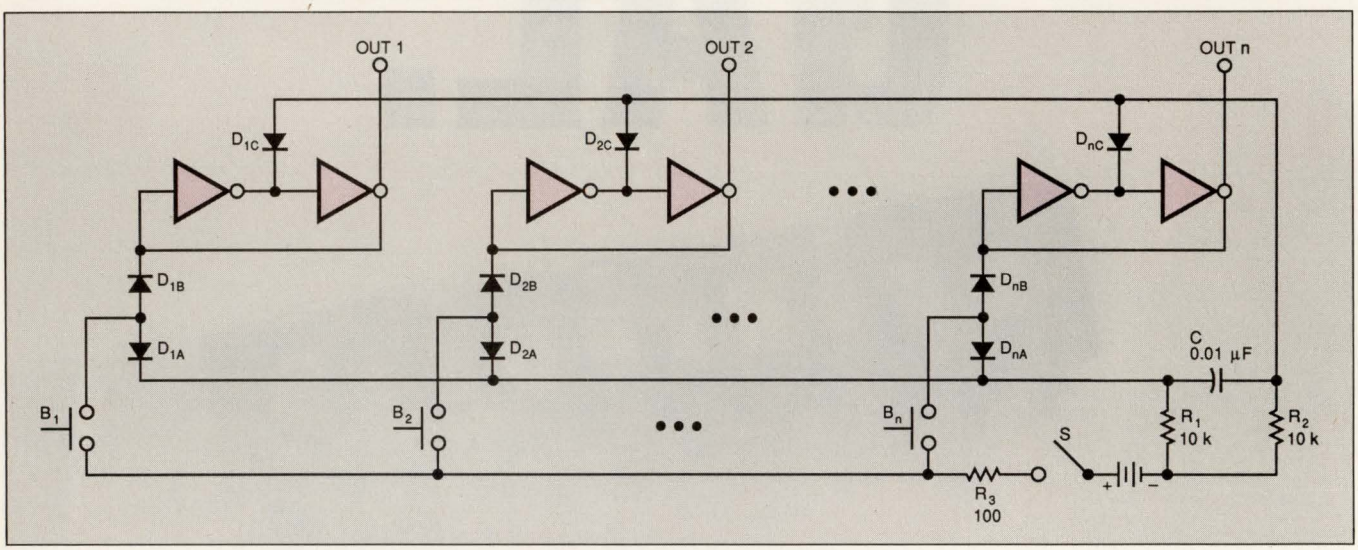

***Fig 1—This pushbutton array mimics** the action of an array of interlocked mechanical switches.*

Micropower clock quashes spurious modes

Norm Looper
Action Instruments, San Diego, CA

Although ceramic resonators are a good choice for low-power, low-frequency clock sources (if you can stand their 30-ppm temperature coefficient), they have troublesome, spurious-resonance modes. The circuit in **Fig 1** rejects all but the resonator's fundamental mode. This clock circuit works from −40 to +80°C and consumes only 2.8 mW.

The rising edge of resonator Y_1 toggles IC_{1A} low. AC-coupled positive feedback from IC_{1D} via C_1 and R_1 immediately confirms this state change at IC_{1B}, so that Miller loading, harmonic components, or below-minimum rise times at IC_{1A} cannot force a relapse of IC_{1C} to its previous state. This tactic also applies to resonator Y_1's falling edge because IC_{1C}, via C_2 and R_2, holds IC_{1B} high.

Choose time constants R_1C_1 and R_2C_2 to be equal and ranging from 60 to 75% of one-half of the clock's

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period. Ceramic capacitors (10% tolerance) with X7RK dielectric work well. With these time constants, the logic will be locked and unavailable to the ceramic resonator until just before it executes a legitimate transition. IC_{1D} and IC_{1C} are in parallel to isolate the resonator from external loads and, more importantly, from C_2. **(EDN BBS DI #887)**

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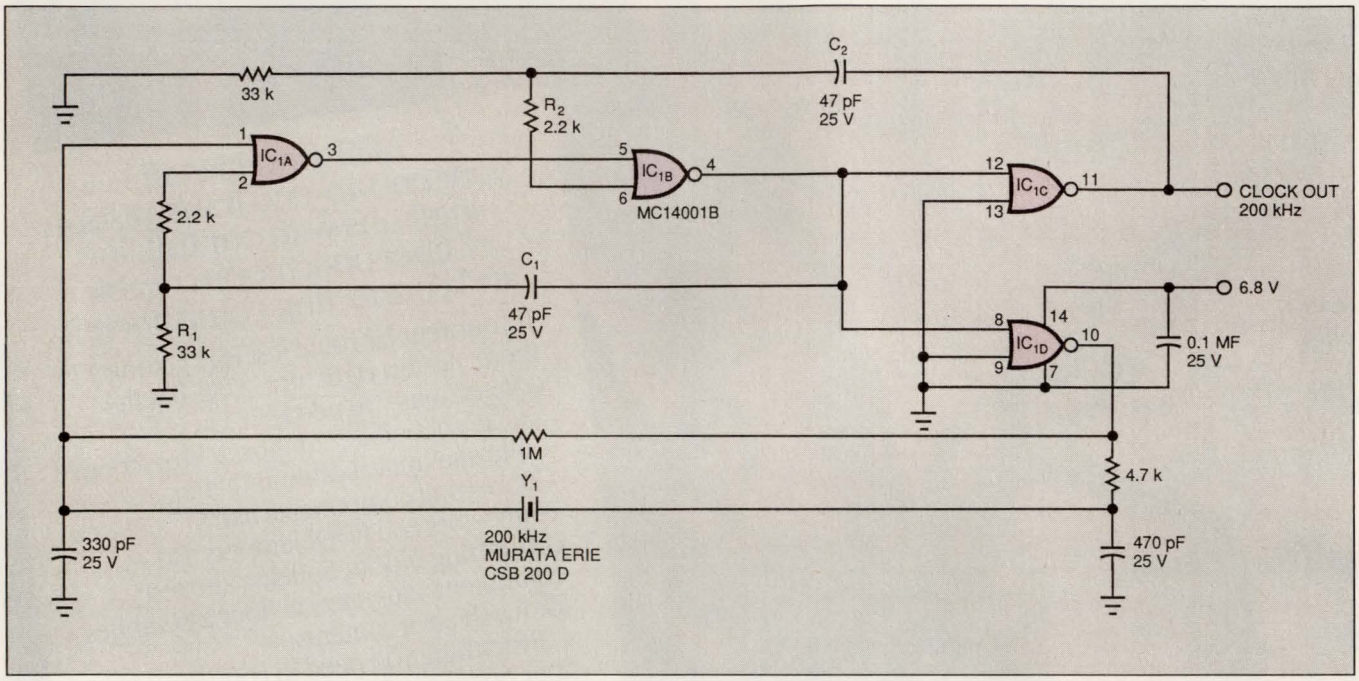

Fig 1—This clock circuit uses a ceramic resonator, *Y_1, to generate low-frequency clock signals. The circuit's logic eliminates the ceramic resonator's pesky spurious-resonance modes.*

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Charles H Small and Anne Watson Swager
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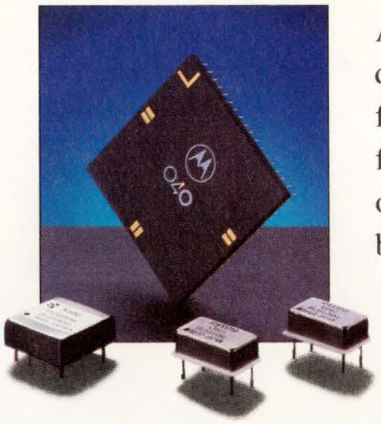

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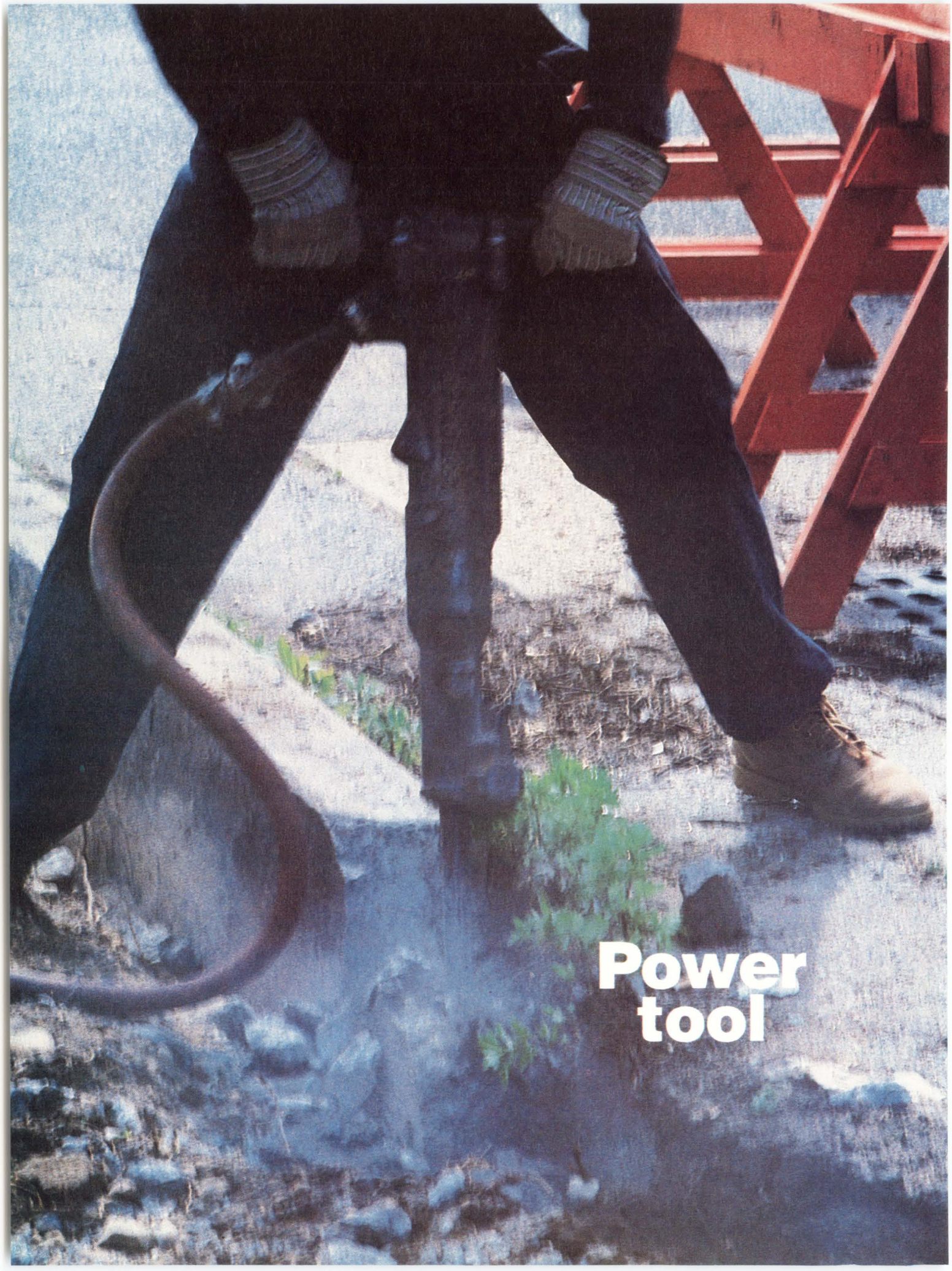
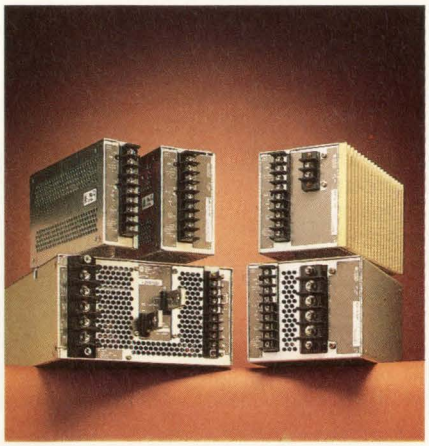

Power
tool

KEPCO ac-dc dc-dc SWITCHING POWER SUPPLIES

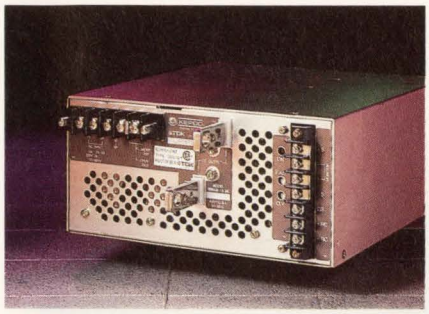
Field-proven in a broad spectrum of applications and certified by the world's safety agencies, here are versatile, rugged power tools for your design needs. Choose voltages up to 48V dc; power up to 1500W; ac or dc input. Features include active soft-start, remote voltage control, overvoltage protection, current limiting and built-in EMI filtering. The 600W and 1500W models provide for current-share paralleling. Kepco's switchers are also available in low-cost open frame and pc-card styles for OEM applications. Please request our catalog.



ac to dc power single output 50W, 100W, 175W, 300W, 1500W

- ☐ 3V-48V dc output
- ☐ jumper selectable inputs: 85-132 or 170-264V ac, 240-370V dc
- ☐ fully enclosed
- ☐ UL/CSA/TÜV
- ☐ Tested to MIL STD 810D
- ☐ FCC Class A EMI filtering

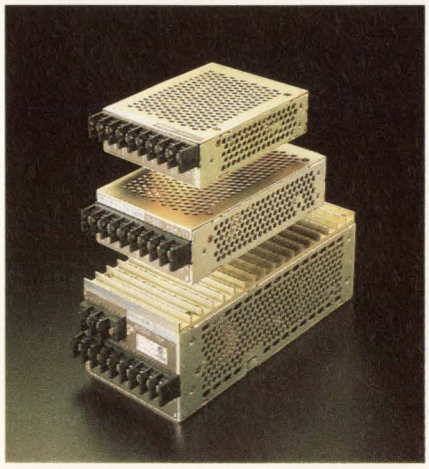
Kepco Group RAX Power Supplies



ac to dc power single output 600W

- ☐ 2V-48V dc output
- ☐ jumper selectable inputs: 85-132 or 170-264V ac, 240-370V dc
- ☐ fully enclosed
- ☐ UL/CSA
- ☐ Tested to MIL STD 810D

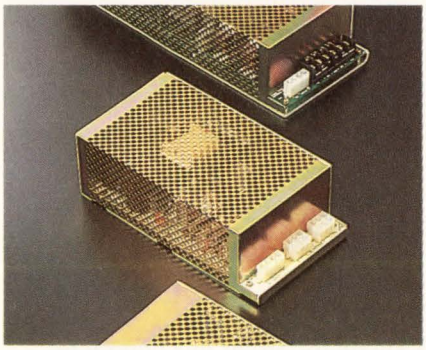
Kepco Group RBX Power Supplies



dc to dc power single output 30W, 60W, 150W

- ☐ 5V-48V dc output
- ☐ 24 and 48V input (60V available on some models)
- ☐ fully enclosed
- ☐ UL/CSA
- ☐ MIL STD 461B EMI filtering
- ☐ Tested to MIL STD 810D

Kepco Group ERD Power Supplies



ac to dc power single output 30W, 60W, 120W, 240W

- ☐ 5V-24V dc output
- ☐ jumper selectable inputs: 85-132 or 170-264V ac, 240-370V dc
- ☐ P-C card, L-chassis, optional enclosure
- ☐ UL/CSA/TÜV
- ☐ FCC Class B EMI filtering

Kepco Group ERX Power Supplies

Power tools

For your free copy of Kepco's new 56-page catalog, "Kepco Switching Power Supplies for the '90s" (#146-1692), call/fax/write Dept. LWT-12, Kepco, Inc., 131-38 Sanford Avenue, Flushing, NY 11352 USA
Tel: (718) 461-7000 • Fax: (718) 767-1102 • Easylink (TWX): 710-582-2631

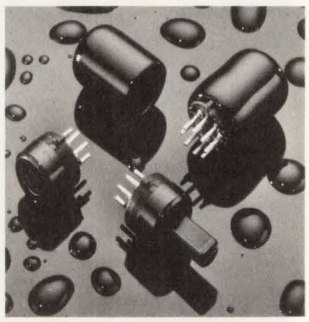
KEPCO. THE POWER SUPPLIER™

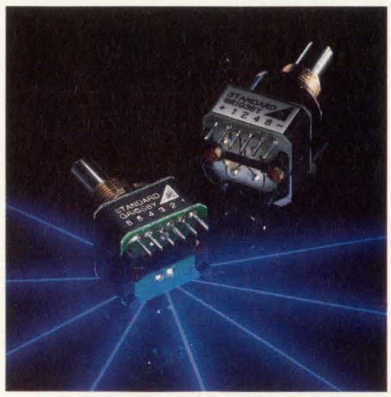
SEE US AT WESCON/90, KEPCO BOOTH 1784, 1786

CIRCLE NO. 77

Gold Terminals Extend TO-5 Switch Life. Gold-plated terminals, handling resistive loads of 500 mA/125 VAC, extend the life of Standard Grigsby's TO-5 rotary switch to an 5000 cycles (typ.). These compact switches mount easily into standard TO-5 transistor sockets or PC boards for wave soldering. Screwdriver or knob actuation available. 45° throw with 8 positions max. Positive detent switching action is standard. Contact pin surface is sealed and an optional boot is available to seal the shaft. Price: $1.39 in 10,000-piece lots. Delivery: 4 weeks. Contact Standard Grigsby, Inc., 88 N. Dugan Rd., Sugar Grove, IL 60554-0890. 708/556-4200 FAX 708/556-4216.

CIRCLE NO. 78

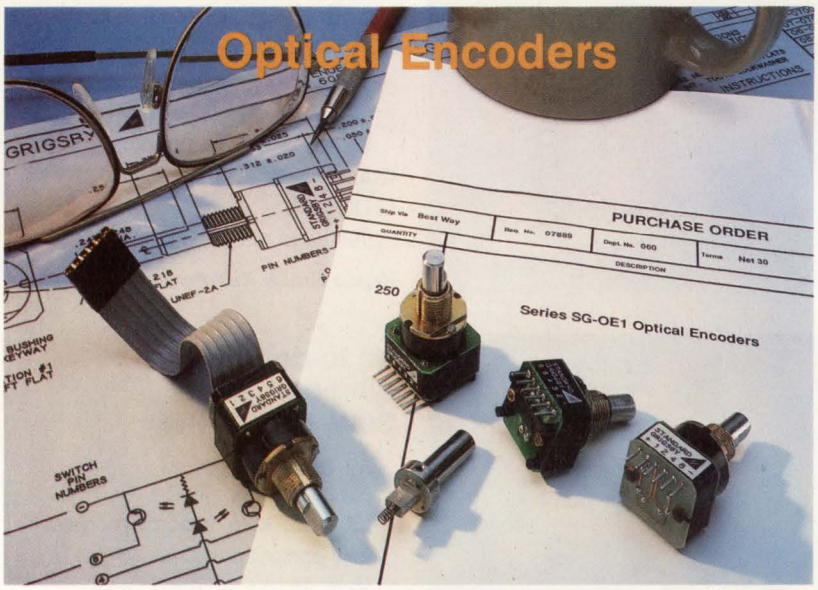




Choose Binary Or Gray Coded. Sugar Grove, IL—Binary and Gray coded optical encoders are available from Standard Grigsby, Inc. Ideal for use in robotics, medical instrumentation, communications, computer peripherals and avionics, the 16-position encoder is available with integral cable or connector. Users may specify custom shaft lengths and diameters.

Priced at $29.10 each in 100-piece lots, the encoders are available in 6 weeks. Standard Grigsby, Inc., 88 N. Dugan Road, Sugar Grove, Illinois 60554-0890. 708/556-4200 FAX 708/556-4216.

CIRCLE NO. 99



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- Reliable LED optical switching source
- Long life
- Low power consumption

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- Binary, gray, or custom codes
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- High res, 128-152 position option
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Raise your switching standards! Call us today for our complete **Optical Encoder** product catalog. 708/556-4200

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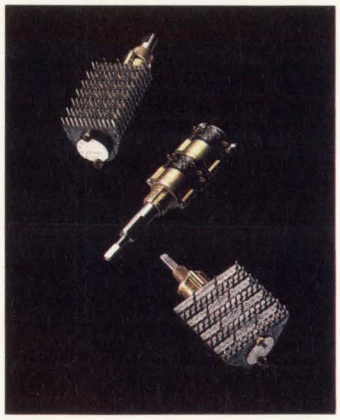


Multi-deck, Multi-options. Sugar Grove, IL—Standard Grigsby's multi-deck rotary switches offer reliability and long life, and retrofit other manufacturers. Measuring approximately ½″ in diameter, the switches are available with PC or solder lug terminations, fixed or adjustable stops; 30° or 36° indexing angles; commercial or military finishes.

Priced at $4.50 each in lots of 500, the switches are available in 6 to 8 weeks. For more information, contact Standard Grigsby, Inc., 88 N. Dugan Road, Sugar Grove, IL 60554-0890. 708/556-4200 FAX 708/556-4216.

CIRCLE NO. 103

NEW PRODUCTS

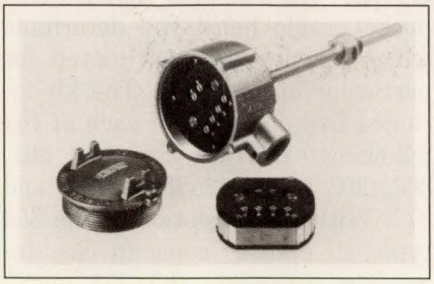
COMPONENTS & POWER SUPPLIES

Monolithic Pressure Sensor

- *Totally conditioned*
- *Has a 4.5V output*

The MPX5100D pressure sensor integrates a sensing element, offset calibration circuitry, temperature compensation circuitry, and signal amplification on a monolithic silicon chip. The unit has a 0 to 85°C compensated operating range and features a full-scale output that is calibrated from 0.5 to 4.5V. The device uses a patented silicon shear stress strain gauge, which measures 0- to 15-psi differential pressures. Zero pressure offset measures 0.5V and sensitivity equals 40 mV/kPa. Linearity over the full 0- to 15-psi range equals ±0.2% full scale. Temperature hysteresis and temperature effect on zero offset equal ±0.05% of full scale and ±25 mV, respectively. The sensor is available in the basic element package, as well as in single- and dual-ported versions. Sensors with customized outputs are also available. $45 (100). Delivery, stock to eight weeks ARO.

Motorola Inc, 5005 E McDowell Rd, Mail Drop Z201, Phoenix, AZ 85008. Phone (800) 752-3621; in AZ, (602) 244-4556. **Circle No. 363**



Temperature Transmitters

- *Feature ±0.1% accuracy*
- *Provide input/output isolation*

Models in the 84500 series of 2-wire temperature transmitters provide a 1500V I/O isolation and accept Pt100 RTD, Type K thermocouple, and Type J thermocouple inputs. The devices have ±0.1% span accuracy and zero and range selection via rotary switches with 20-turn potentiometers for fine adjustment. The transmitters operate with supply voltages of 10 to 36V dc. The units feature less than ±0.01%/°C zero and span drift and provide automatic upscale indication for sensor burnout. Pt100 RTD units are completely linearized and thermocouple models are voltage linear. The transmitters meet the EMI immunity standards outlined in SAMA PMC33. $198.50.

S-Products Inc, 35 Kings Hwy E, Fairfield, CT 06430. Phone (203) 331-9546. FAX (203) 335-2723. **Circle No. 364**

D-Size Backplane

- *Designed for VXIbus*
- *Will handle 350A at 5V*

This 100-MHz, D-size backplane is a 12-layer board designed to meet or exceed VXIbus Specifications Rev 1.3. All critical signal lines are matched to eliminate signal propagation skew. The design equalizes currents between all connector rows. Optional power and ground bus bars accommodate even high-current distribution, allowing the backplane to handle 350A at 5V. The unit features onboard termination and BUSGRANT and IACK jumpers between each J1 slot. ECL signals terminate at the end of the bus to minimize signal reflections. A set of onboard module-status LED indicators, controlled by slot 0, signals if a board is not plugged in or if a slot is empty. The backplane design provides a grounded area around each connector to ensure shielding integrity. $2099 for a 13-slot unit.

Dawn VME Products, 47073 Warm Springs Blvd, Fremont, CA 94539. Phone (415) 657-4444. FAX (415) 657-3274. **Circle No. 365**

Universal-Input Supplies

- *Feature power-factor correction*
- *Provide 1000W output*

F Series power supplies feature correction circuitry that delivers a typical power factor of 0.98. Autoranging circuitry allows the supplies to operate in any country without the need for jumpers or switches. The supplies are available in 800 and 1000W versions and provide outputs of 2, 5, 12, 15, 24, and 48V. Additional features and options include current sharing, soft start, overload and overvoltage protection, electronic inrush current limiting, remote sense, remote inhibit, remote margin, no-load operation, EMI input filter, and full safety-agency approvals. A forced current-share option provides the paralleling capability essential for redundant power systems. $808 (100). Delivery, 10 weeks ARO.

Unipower Corp, 2981 Gateway Dr, Pompano Beach, FL 33069. Phone (305) 974-2442. FAX (305) 971-1837. **Circle No. 366**

Low-Profile Connector

- *Measures only 0.283 in. high*
- *Has surface-mount contacts*

The FCN228 can connect two pc boards end to end. Measuring only 0.283 in. high, the connector features two rows of surface-mountable contacts that are located on one side of the connector and are spaced on 0.050-in. centers. Contacts solder mount to the top and bottom edges of a daughter card, allowing it to be plugged into the mother board in the same plane. The connector insulator employs polyphenylene sulfide plastic, which handles the 220°C temperatures encountered in infrared reflow soldering processes. The connectors are available in 26- and 60-pin versions. Contacts are rated for 24A at 250V ac. Contact resistance equals 35 mΩ,

and insulation resistance and dielectric withstanding voltage ratings equal $10^9\Omega$ and 500V ac, respectively. Operating range spans −55 to +105°C. $5.21 for 26-pin version; $9 (1000) for 60-pin version.

Fujitsu Component of America Inc, 3330 Scott Blvd, Santa Clara, CA 95054. Phone (408) 562-1000. FAX (408) 727-0355.

Circle No. 367

Shielded Inductors

- *Have inductance values ranging to 100,000 μH*
- *Comply with MIL-C-39010*

Series M39010 fixed shielded inductors comply with the moisture, shock, and vibration-resistance requirements of MIL-C-39010. You can place the units side by side on a pc board without any crosstalk problems. The units are available in three styles (M39010/1, /2, /3) and have inductance values ranging from 0.1 to 100,000 μH. The devices are available with iron, ferrite, and phenolic cores. They operate over a −55 to +105°C range and comply with failure rate S (0.001%/1000 hour) of MIL-C-39010. The units weigh 1g max and pass a 5-lb terminal pull test. $1.95 to $4.10.

Nytronics Components Group Inc, 700 Orange St, Darlington, SC 29532. Phone (803) 393-5421. FAX (803) 393-4123. **Circle No. 368**

EMI Filter

- *Attenuates 40 dB in the 100-kHz to 50-MHz band*
- *Has a 30W throughput*

AF461 Series EMI filters complement high-frequency dc/dc converters. The units will attenuate 40 dB in the 100-kHz to 50-MHz band, and they will bring standard converters into accordance with MIL-STD-4611B CE03 noise limitations. Units are rated for either 1.75 or 3.8A max input current with as much as 30W throughput with 16 to 40V dc. The units are available with an optional −55 to +125°C feature with full military screening. The filters are packaged in a hermetically sealed standard printed circuit or a flange-mount-type metal case that is less than 0.5 in. high and needs only 2.5 $in.^2$ of board space. $101 (100); $149 (100) for commercial and military-grade devices. Delivery, stock to 20 weeks ARO.

Advanced Analog, 2270 Martin Ave, Santa Clara, CA 95050. Phone (408) 988-4930. FAX (408) 988-2702.

Circle No. 369

Liquid-Crystal Display

- *Requires no controller chip*
- *Features an 8-line×16-character format*

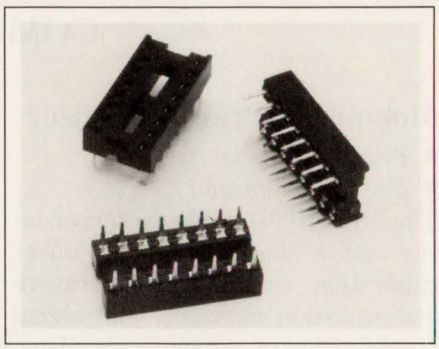
The F1016 LCD graphics module provides a simple interface at low cost. The module's driver has a built-in memory, which supports a direct 8-bit parallel interface with a μP. The device features a 4×2.7-in. viewing area, and it has an 8-line×16-character viewing format. The display's 0.85×0.85-mm dots have 0.05-mm spacing. The module employs supertwist technology in a reflective mode. It measures 5.5×4.3×0.56 in., has power-supply requirements of ±5V at 3.5 mA, weighs 150g, and operates over a 0 to 50°C range. $75 (100).

Seiko Instruments USA Inc, Liquid Crystal Display Dept, 2990 Lomita Blvd, Torrance, CA 90505. Phone (213) 517-7837. FAX (213) 517-7792. **Circle No. 370**

DIP Sockets

- *Withstand wave soldering*
- *Help prevent damage from oversized leads*

The series 200C devices are closed-bottom, stamped, single-beam-contact DIP sockets that allow you to insert ICs prior to wave soldering. A patented contact design protects against flux and solder contamination while allowing for proper drainage during cleaning. The units feature an open-entry design to facilitate manual and automatic IC insertion. An antioverstress feature protects the contacts and helps eliminate damage from oversized leads. The sockets are available with 8 to 48 pins and are designed to military standards. Contacts are either beryllium copper or phosphor bronze with selective gold or tin-lead plating. Socket tails are available in three lengths. $0.0026 to $0.004 per pin.



Augat Inc, Interconnection Products Div, Box 779, Attleboro, MA 02703. Phone (508) 222-2202. FAX (508) 222-0693. **Circle No. 371**

Epoxy Evaluation Kit

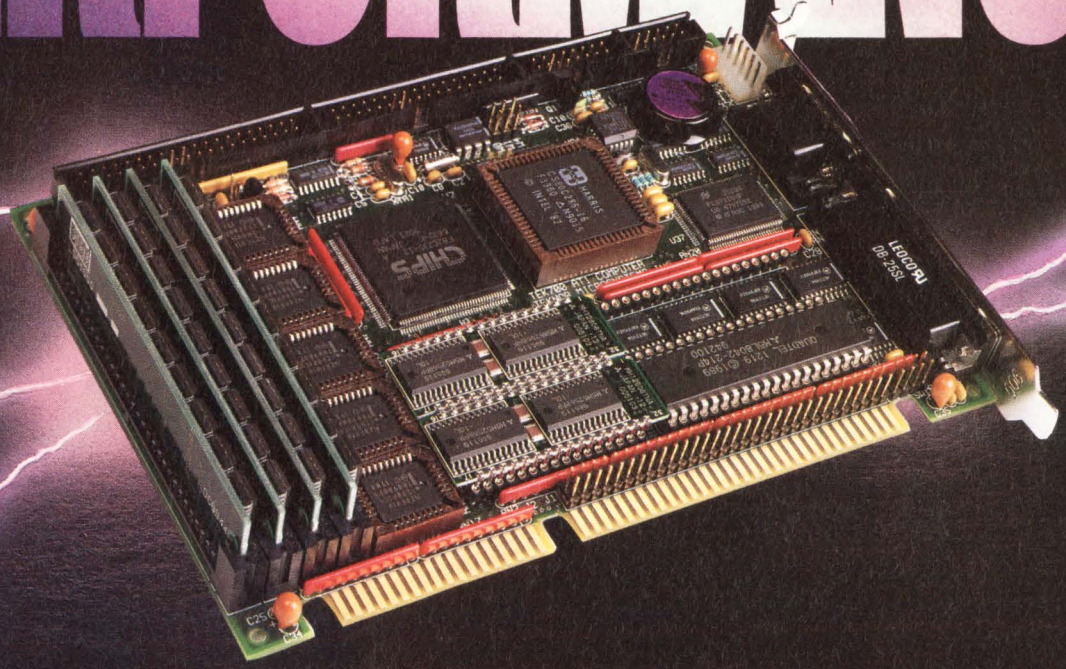
- *Epoxy comes in easy-to-mix packages*
- *Includes applications guide*

The 600-4EPO-1000 evaluation kit features seven of the most popular Epotek epoxies. An applications pocket guide helps you determine which epoxies are best suited for particular applications. The kit includes five packages of each of the following epoxies—Epotek 301, 302, 302-3, 320, 353ND, 354, and 377. With the exception of the 354 type, all epoxies come in easy-to-mix 4g packages; the 354 epoxy comes in an 8g package. All characteristics and features are presented in a table contained within the pocket guide. $129.85.

OFTI, 5 Fortune Dr, Billerica, MA 01821. Phone (508) 663-6629. FAX (508) 663-9351.

Circle No. 372

THE EXTREME PERFORMANCE



SO MUCH FROM SO LITTLE

High Level Of Integration. The TEK-AT1 features an 80C286 at up to 20 Mhz with system memory from 512 Kbytes up to 4 MBytes, two serial ports, one parallel port, a watchdog timer, a power failure detector, solid state disks with support for FLASH EPROMS, floppy and hard disk controllers.

Versatility. The TEK-AT1 can be used in a PC/AT passive backplane or as a stand alone computer for embedded applications.

Reliability. Teknor's products are built to operate in harsh environments. The TEK-AT1 can operate in extented temperature ranges and require very little power (sleep mode supported), typically less than 4 watts. The TEK-AT1 is backed by a two year warranty.

The solution: CALL 1 (514) 437-5682

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MICROSYSTEMS INC.

CIRCLE NO. 79

The right connection

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ROM Operating System

- *Provides functionality of MS-DOS version 3.2*
- *Can run ROM-resident application programs*

Version 1.28 of ROM-DOS now provides all of the functionality of MS-DOS version 3.2. This operating system can run directly from ROM (you don't have to download it to RAM); it occupies approximately 34k bytes of ROM and uses only 14k bytes of RAM. Enhancements include the ability to run, directly from ROM, any .COM or .EXE application programs that have been assembled so that the code is ROM-resident and only work space requires RAM. You can use a standard BIOS with ROM-DOS or, for embedded systems that do not need a full BIOS, the vendor supplies a mini-BIOS that supports a remote console (via a serial port), a hardware timer, and serial communication ports. Firmware, $6/copy (5000); developer's kit, $495; source-code license, $10,000.

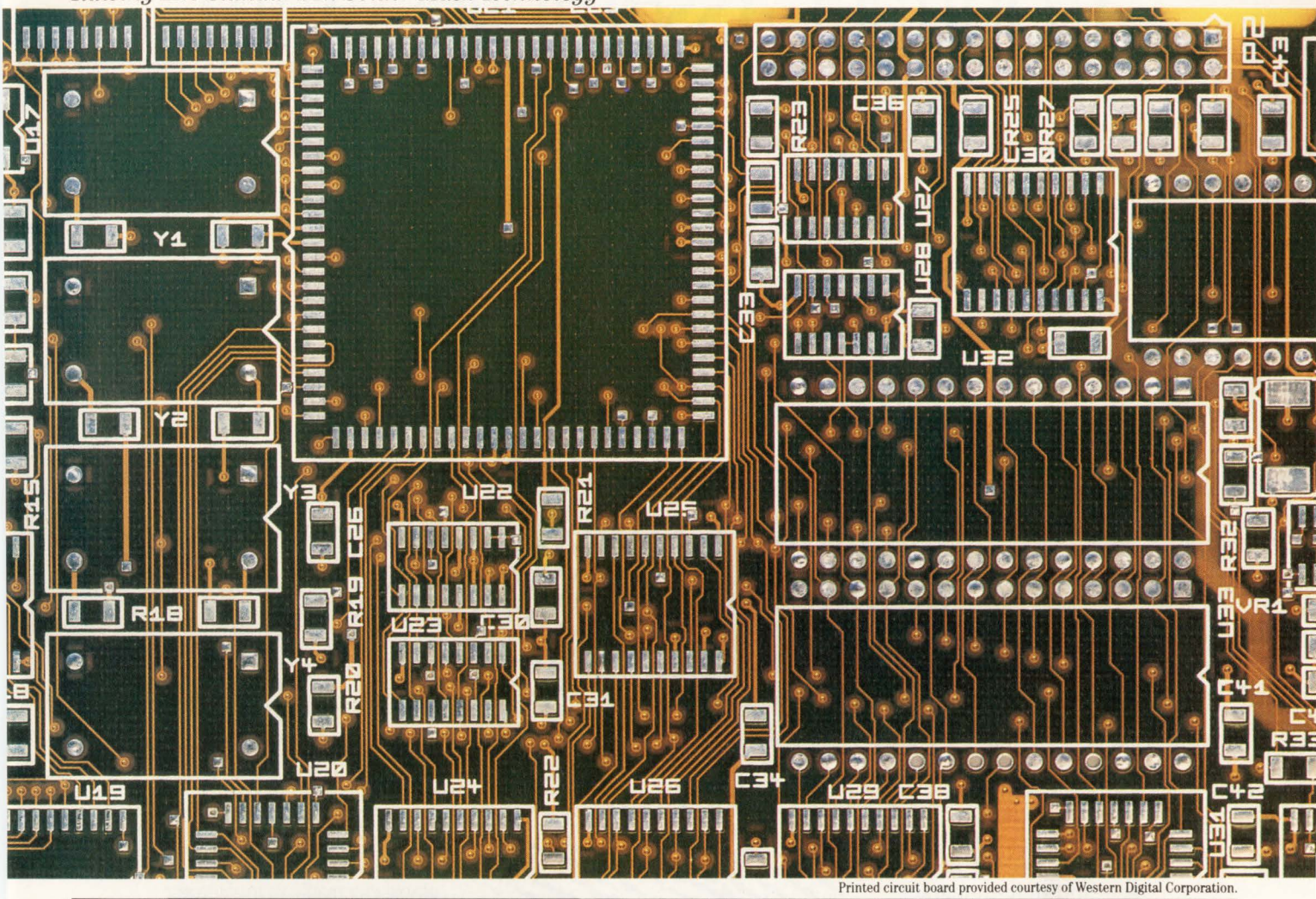
Datalight, 17505 68th Ave NE, Suite 304, Bothell, WA 98011. Phone (206) 486-8086. FAX (206) 486-0253. **Circle No. 351**

CASE Tool For Program Structures

- *Lets you create and modify program structures*
- *Provides a window-oriented user interface*

Diamond X-Tools (developed by AID GmbH, Nuremberg, Germany) is a set of CASE tools that work with Nassi-Schneiderman block charts, called Structograms. The structogram editor provides multi-window operations, pop-up menus, dialog boxes and selection lists, and context-sensitive, on-line help. You can write your programs in C, Ada, PL/M, Pascal, Fortran, Cobol, or Modula-2; the program automatically places your statements in preset areas of the various block types. The sourcetexters (supplied separately for each language) convert structograms into clear source code for compilation. You can call a syntax checker from within the structogram editor. It generates the source code via the sourcetexter; invokes the target compiler; reroutes the error listing and links it to the appropriate portion of the structogram currently on the screen; and highlights the statements that

Raising The Standard In Solder Mask Technology



Printed circuit board provided courtesy of Western Digital Corporation.

No Matter What Kind Of Solder Mask Technology You Need, Du Pont Has You Covered.

No one offers a wider range of proven, quality photoimageable solder mask products than Du Pont. More importantly, no one knows more about how solder mask technology can affect your design, fabrication or assembly process.

Our knowledge and experience in solder mask technology is reflected in three different solder masks. That means we can help you match the right technology to your application—whether it's conventional through-hole or high-density fine pitch surface mount.

For dry film, count on VACREL® to encapsulate dense circuitry, tent via holes, and permit more electrical functions in less PWB real estate.

In liquid solder mask, VAQS™ photoimageable liquid provides a thin coating that conforms to PWB topography to give you excellent encapsulation of circuitry.

Finally, the Du Pont VALU™ system—the newest technology in the industry—combines the cost-efficiencies and thinness of liquids with the design freedom and quality of dry film in one unique liquid/dry film combination.

And of course, all Du Pont solder mask products are available worldwide.

So, if you want to work with an objective partner who can offer you a variety of solutions to meet your solder mask needs, remember, no one has you covered like Du Pont.

For more information, call **1-800-237-4357.** Or write: Du Pont Electronics, Room G-51875, P.O. Box 80029, Wilmington, DE 19880-0029.

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In Wisconsin: 414/785-6359

Philips Circuit Assemblies

PHILIPS

PHILIPS

caused errors. A transformer module provides reverse-engineering facilities; it converts existing source code into a set of structogram files that the structogram editor can load, modify, and save. To run the tools, you'll need an IBM PC or compatible with 640k bytes of memory and a color or monochrome graphics adapter. From $895.

Software Design Tools Inc, Sunset/Vine Tower, Suite 1126, 6290 Sunset Blvd, Los Angeles, CA 90028. Phone (213) 463-5090. FAX (213) 463-4319. **Circle No. 352**

Bernoulli Driver

- *Takes advantage of Windows' removable-storage features*
- *Available as an upgrade*

The Bernoulli Driver 4.72 fully supports the removable-storage-device features of Microsoft's Windows version 3.0. This driver is included as part of the software package supplied to new purchasers of the vendor's Bernoulli Box drives. Users who have earlier versions of the device driver can upgrade it to version 4.72 for $15.

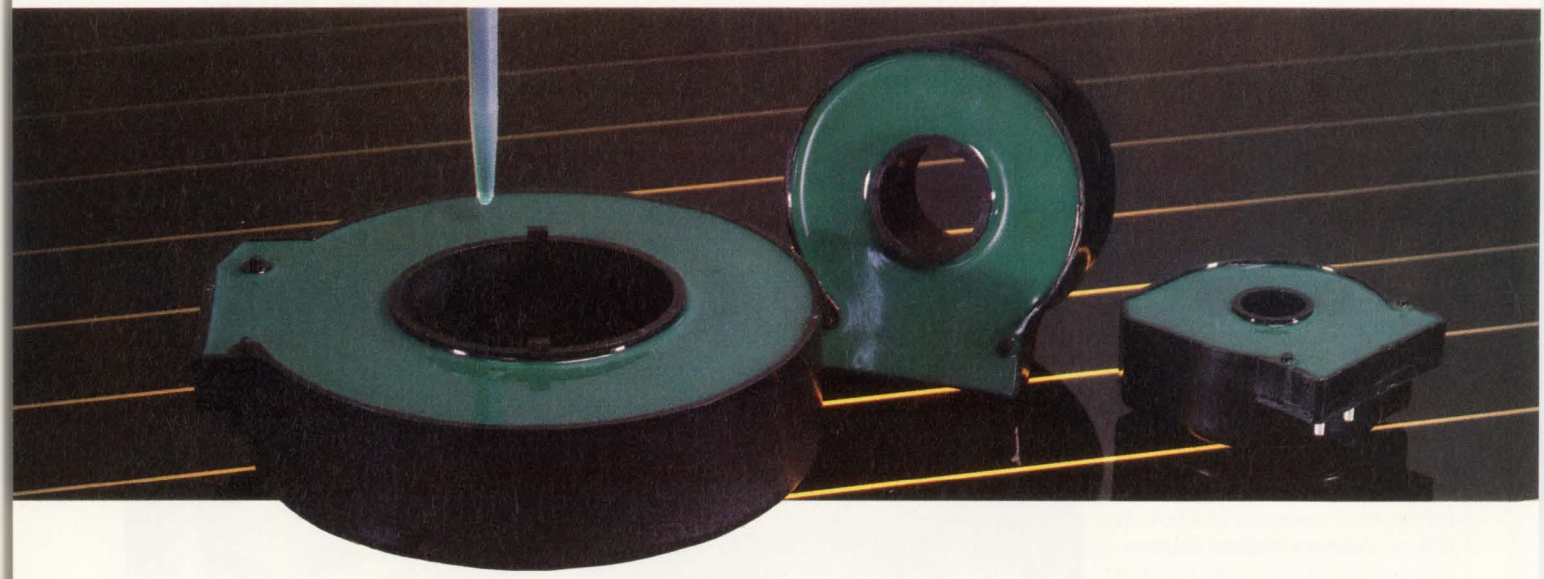
Iomega Corp, 1821 W 4000 St, Roy, UT 84067. Phone (801) 778-1000. **Circle No. 353**

Prolog Development System Interfaces With C Programs

- *Lets you link inference-based modules to C code*
- *Provides an X-Window-based user interface*

Quintus Prolog 3.0 is a Prolog software-development system that runs on Sun-3 and -4 workstations. It allows you to write, edit, run, and debug inference-based functions, which you can then embed in an application program written in C. You can use the product's

The Encapsulant Problem Solvers.



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CIRCLE NO. 81

backward-chaining inference engine directly in expert systems, or as a tool for developing new expert systems. Prolog's virtual-memory database for both facts and rules, and the dynamic data structures that are created and accessed through pattern matching, suit applications in which programs manipulate other programs and data represents information about other data. Such applications include computer-aided tools, non-numeric simulations, and intelligent user interfaces. The system provides a user interface that is based on the X-Window standard; this user interface supports the OSF/Motif look-and-feel. The package includes a window-based source-level debugger and makes use of the X resource manager to allow you to customize your windows. $10,000.

Quintus Computer Systems Inc, 1310 Villa St, Mountain View, CA 94041. Phone (415) 965-7700. FAX (415) 965-0551. **Circle No. 354**

3-D Imaging Software

- *Runs on Alliant FX/2828 supercomputer*
- *Uses ray-tracing algorithms*

Mental Ray is a 3-D ray-tracing software package that runs on Alliant's FX/2800 Series parallel supercomputers. The software uses 3-D ray-tracing algorithms to generate images that are almost indistinguishable from photographs. It accurately renders extensive detail seen in shadows, the effects of textures such as glass and chrome, and the influence of multiple light sources. The principle applications for the software are automobile and aerospace design, computational chemistry, scientific visualization, television and movie animation, and military simulation. The software was developed by Mental Images GmbH (Berlin, Germany) and is compatible with the Advanced Visualizer software from Wavefront Technologies (Santa Barbara, CA). You can create models using the Advanced Visualizer on a workstation, and then send them for enhancement to an Alliant supercomputer that acts as a high-performance rendering server. The vendors are developing interfaces to CAD standards such as IGES to allow the system to import images directly from engineering CAD systems. From $15,000, depending on host configuration.

Alliant Computer Systems Corp, 1 Monarch Dr, Littleton, MA 01460. Phone (508) 486-4950.

Circle No. 355

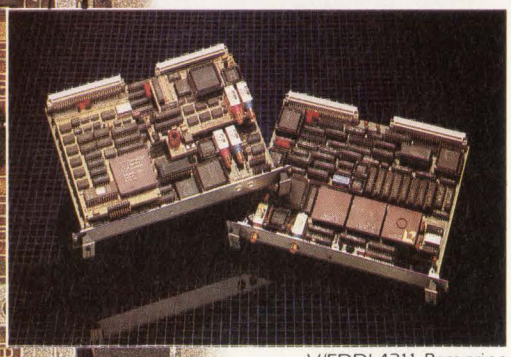
Graphics System Debugger

- *Supports IEEE floating-point format*
- *Provides redirection of output to log files*

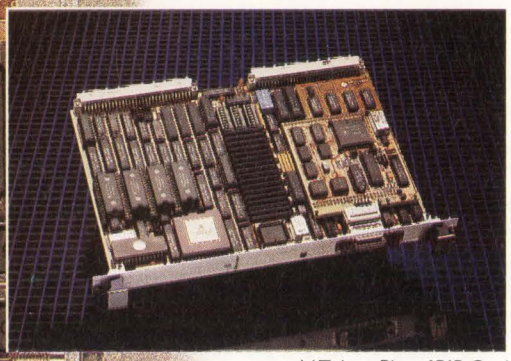
Gspot (Graphics System Processor Operating Tool) 1.0 is a symbolic debugger for TI's 34010 graphics system processor (GSP). The debugger runs on IBM PCs and compatibles, and you can configure it to work with any GSP-based hardware including TI's SDB board. You can install the debugger as a resident program while using another debugger for the host processor. You can return to Gspot either by pressing a hot key or by the action of breakpoints in the GSP program. Other features include symbolic debugging, C source-level debugging, a user interface similar to that of Microsoft's CodeView, online assembly, and a memory display/edit mode. The program also provides full TIGA support. $995.

Pixelab Inc, 4513 Lincoln Ave, Suite 105, Lisle, IL 60532. Phone (708) 960-9339. FAX (708) 960-9396. **Circle No. 356**

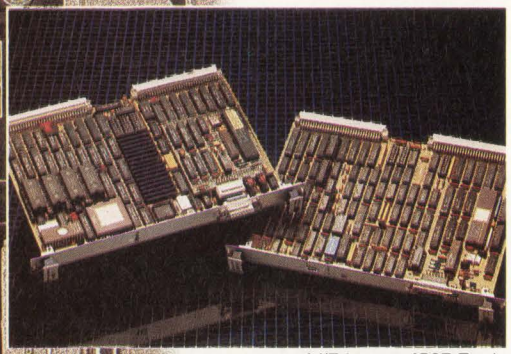
NETWORKING SOLUTIONS



V/FDDI 4211 Peregrine
V/FDDI 3211 Falcon



V/Token-Ring 4212 Owl



V/Ethernet 4207 Eagle
V/Ethernet 3207 Hawk

FDDI, TOKEN-RING AND ETHERNET COMMUNICATIONS

The need to network has never been greater. Diverse processing platforms, distributed architectures, client-server, departmental and workgroup environments all contribute to increased demands on the network. System and network designers need a proven source of technology solutions for the wide range of networking and communication application problems they face. Interphase delivers those solutions.

FDDI, TOKEN-RING AND ETHERNET SOLUTIONS

Interphase has long led the industry in high-performance VMEbus peripheral controllers, and that same leadership is now evident in networking node controllers. Interphase has FDDI, Token-Ring and Ethernet solutions for virtually any VMEbus system application challenge.

PROVEN FDDI SPEED AND INTELLIGENCE

Interphase's FDDI 100 Mb/s offerings are a logical choice for the industry. The V/FDDI 3211 Falcon received *UnixWorld* magazine's Product of the Year designation and was the industry's first 6U VMEbus FDDI solution. Interphase's newest FDDI product is the V/FDDI 4211 Peregrine, a RISC-based high-performance node controller capable of link level operation or on-board protocol processing. The Peregrine provides single or dual attach configurations, with SMT (Station Management Software) running on-board, all in one 6U VME slot.

TOKEN-RING RESULTS

The V/Token-Ring 4212 Owl is an ultrafast Token-Ring node controller based on the partitioned architecture of Interphase's proven Eagle class of controllers. The Owl facilitates connectivity of UNIX® systems, workstations, supercomputers or any other VMEbus system into an IBM® environment using IEEE 802.5 Token-Ring. This multiple processor design provides an elegant queued interface to the system supporting IEEE 802.2 LLC, and a flexible 4 or 16 Mbit interface to the Token-Ring network.

ETHERNET CHOICES

Interphase also offers two Ethernet design options. The V/Ethernet 4207 Eagle 32-bit protocol platform is the high-performance standard for the industry, and offers on-board TCP/IP support. The V/Ethernet 3207 Hawk is designed specifically for cost-sensitive VMEbus applications.

GET YOUR NET WORKING NOW

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CIRCLE NO. 82

NEW PRODUCTS

TEST & MEASUREMENT INSTRUMENTS

Portable, Wideband, Polyphase Power Analyzer

- *Offers 0.1% accuracy*
- *Works from 500 μA to 20A, 15 mV to 600V, and dc to 100 kHz*

The model 2500 wideband power analyzer captures instantaneous ac line voltage and current and computes virtually any related quantity with 0.1% accuracy. Examples of the computed values are watts, volt amperes, reactive volt amperes, power factor, phase angle, watt-hours, and volt-ampere hours. By connecting several analyzers, you can make measurements on polyphase power systems. The input frequency range is dc to 100 kHz. The voltage range is 15 mV to 600V, and the current range is 500 μA to 20A. The power range is 75 to 9999 μW. The unit contains low-pass, highpass, and bandpass filters. An optional 8-channel analog output drives a chart recorder. $1595; with polyphase capabilities, $1795; RS-232C, $275; IEEE-488, $295.

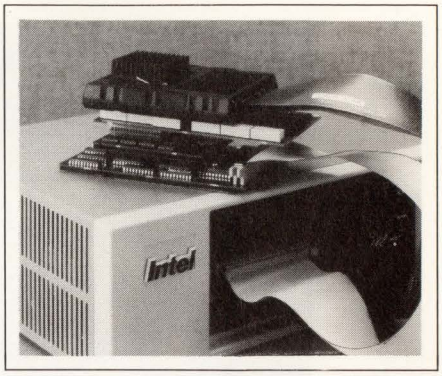
Xitron Technologies Corp, 10225 Barnes Canyon Rd, Suite A102, San Diego, CA 92121. Phone (619) 458-9582. FAX (619) 458-9213.

Circle No. 357

In-Circuit Emulator For 33-MHz i486

- *Has 8k-byte trace buffer and 2M-byte expansion memory*
- *Fully supports μP's protected mode*

The ICE-486 performs real-time in-circuit emulation of the i486 32-bit μP at speeds to 33 MHz. The emulator fully supports the chip's real and protected modes and provides visibility of the on-chip cache. Its 2M bytes of expansion memory allow debugging of large programs. Use of symbolic references and automatic translation of virtual addresses to linear and physical addresses speed debugging. An 8k-byte trace buffer selectively cap-



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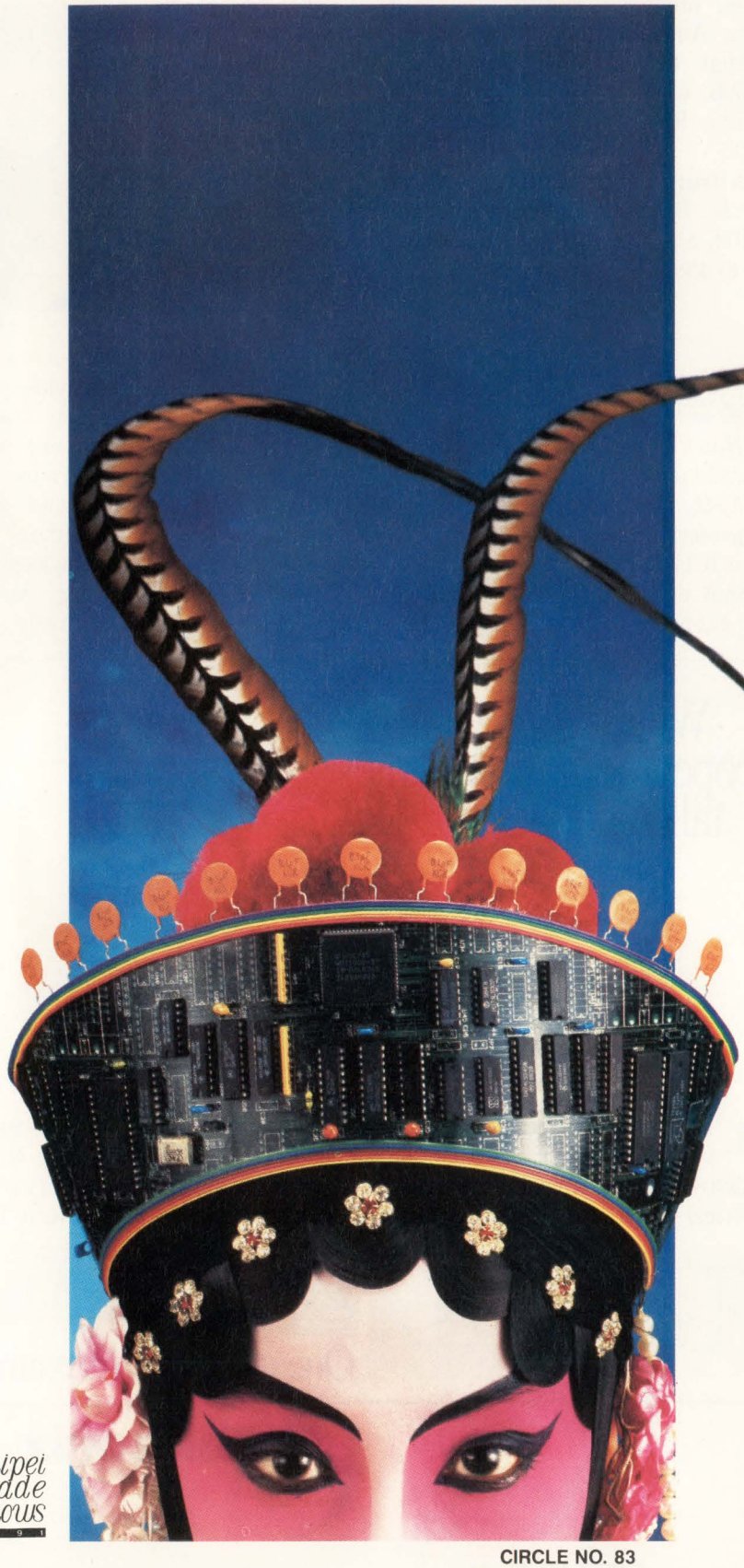

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Taipei Trade Shows 1991

CIRCLE NO. 83

tures bus activity or execution information. You can use the unit's event-recognition capabilities to set breakpoints on execution and bus events. The vendor offers a full set of tools for the i486 including a software debugger, a macro assembler, and compilers for C, Fortran, and PL/M. $49,500.

Intel Corp, Box 58130, Santa Clara, CA 95052. Phone (800) 548-4725. **Circle No. 358**

Miniature RS-232C-To-IEEE-488 Converter

- *Is the size of a DB-25 connector shell*
- *Supports data transfers to 19.2k bps*

The 500-Serial is about the size of the shell of a DB-25 connector—the industry standard for RS-232C. The tiny unit allows you to control from one to eight IEEE-488-interfaced

instruments from the RS-232C port of a computer that lacks an IEEE-488 port. The 5-mA operating current comes from the serial port's handshaking lines. Data transmission occurs at speeds as high as 19.2k bps. The unit supports the following IEEE-488 functions: SRQ, SPE, LLO, DCL, and GET. With the converter, the vendor supplies a 15-ft RS-232C cable and a 9- to 25-pin adapter that lets you use the converter with the serial ports of IBM PC/AT-compatible computers. An MS-DOS diskette contains programming examples. $299.

Keithley Instruments Inc, 28775 Aurora Rd, Cleveland, OH 44139. Phone (800) 552-1115; in OH, (216) 248-0400. FAX (216) 248-6168. **Circle No. 359**

BNC Attenuator Kit

- *Operates from dc to 1 GHz*
- *Includes 3-, 6-, 10-, and 20-dB units*

The TPI-100 BNC attenuator kit contains four 50Ω attenuators, a 50Ω feedthrough, and a 50Ω termination. The insertion loss of the attenuators is 3, 6, 10, and 20 dB. Because they use thick-film resistor networks, the attenuators work from dc to 1 GHz. The rectangular shape of the enclosures prevents the units from rolling off a workbench. The units are reportedly

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more rugged than more expensive units. An easily carried transit case houses the six pieces in the kit. $110.

Test Probes Inc, 9178 Brown Deer Rd, San Diego, CA 92121. Phone (800) 368-5719.

Circle No. 360

Source-Level C Interface For 80186 ICE

- *Supports an unlimited number of symbols*
- *Lets you view source, assembly, and mixed-mode code*

HyperSource is a windowed, C-language, source-level interface for the vendor's Mice-III-80186 in-circuit emulator. The interface displays source code, assembly code or source and assembly code interleaved. The software works with code files in Intel OMF (object-module format) or Easy OMF. The number of symbols is unlimited, and you can access all symbolic information, including the names of symbols of local and global scope. The register contents and a watch-variable window are updated after every breakpoint or single step. You can directly alter these quantities or use C operations to modify them after they increment. The interface software provides quick access to the stack trace, which contains information on all currently active modules and the exact sequence of routines whose execution caused the operating program to reach the current memory location. Versions of the software run on IBM PC/ATs and 80386-based PCs. Both versions need 2M bytes of RAM and cost $1750.

Microtek International, 3300 NW 211th Terrace, Hillsboro, OR 97124. Phone (503) 645-7333. FAX (503) 629-8460. **Circle No. 361**

Dielectric Constant Characterization Kit

- *Works with network analyzer and computer*
- *Includes probe and software*

The HP 85070A kit works with a network analyzer and a computer to measure the dielectric properties of materials used in electronics as well as of materials used in the food and chemical industries. The system measures the material properties as a function of frequency to 20 GHz. Measured quantities include the sample's complex permittivity and dielectric-loss factor. The IBM PC-compatible software runs under Microsoft Windows. $3950; complete systems including network analyzer and computer, from $36,000. Delivery, 12 weeks ARO.

Hewlett-Packard, 19310 Pruneridge Ave, Cupertino, CA 95014. Phone (800) 752-0900.

Circle No. 362

NEW PRODUCTS

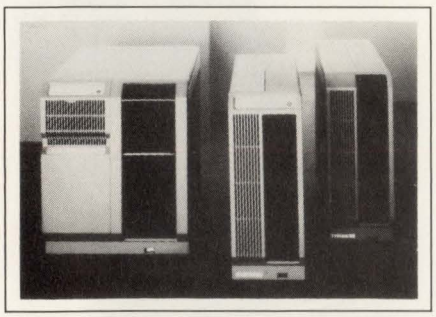
COMPUTERS & PERIPHERALS

Stereo Digital Audio Board

- *Simultaneously records and plays back two audio channels*
- *Utilizes TI's 320C10 DSP chip and has 80-dB dynamic range*

The Series 2/SX-8 is a stereo digital audio board for the 16-bit ISA bus. It lets the user perform high-fidelity, direct-to-disk recording. The board can simultaneously record and play back two separate audio channels with 16-bit resolution. It utilizes TI's 320C10 DSP chip, and it has a dynamic range of 80 dB. It has a frequency response of 20 Hz to 20 kHz. It achieves a S/N ratio of 75 dB, and its total-harmonic-distortion specification is 0.1%. You can control sampling rates, volume, bit resolution, antialiasing filtering, and data-file formats using the supplied software. The board can record data in either 16-bit PCM format or 4-bit ADPCM format for 4:1 data compression. You can operate two or more boards in tandem for multichannel recording. $1395.

Antex Electronics Corp, 16100 S Figueroa St, Gardena, CA 90248. Phone (213) 532-3092. FAX (213) 532-8509. **Circle No. 381**



File Server

- *Contains from one to four MC88100 RISC CPUs*
- *Delivers 100-MIPS performance*

The Triton 88 file server contains from one to four MC88100 RISC CPUs. A fully loaded system delivers 100-MIPS performance. In addition, the CPU board contains from two to eight MC88200 cache and memory units providing 32k to 128k bytes of cache memory for the CPUs. Each of the CPUs has access to as much as 128M bytes of shared memory on the CPU board. The system uses dedicated MC68020 μPs as I/O processors. The basic system can be expanded to accommodate as many as 14 I/O processors. Disk mirroring runs solely on the processors. The system also contains a link to a VMEbus for adding standard VMEbus boards. An uninterruptible power supply allows 3 minutes of soft shutdown when power disappears for more than 5 sec. 3-board system with 20-MHz CPU, $54,000.

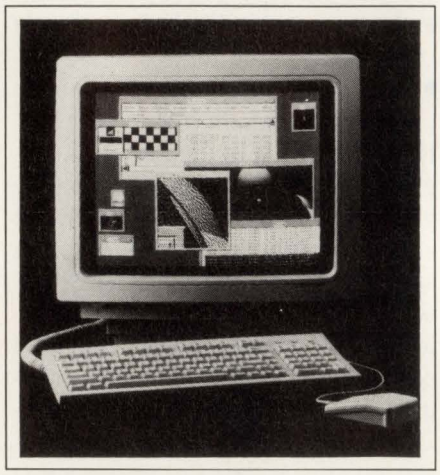
Dolphin Server Technology AS, Olav Helsets vei 6, Box 52, Bogerud, N-0621 Oslo 6, Norway. Phone +47 262 7000. FAX+47 262 7313. **Circle No. 382**

X-Windows Display Station

- *Has a 15-in. grayscale display with 1152×900 pixels*
- *Utilizes a 20-MHz 68020 μP and 2M bytes of DRAM*

The X-15 Turbo is an X-Windows display station in a small footprint. It has a 15-in. landscape display with grayscale. The display has 1152×900-pixel resolution and a refresh rate of 70 Hz. The station utilizes a 20-MHz MC68020 μP, and it has 2M bytes of RAM, which is expandable to 8M bytes in 1M-byte increments. Because the station doesn't have fans or disk drives, it runs silently. The unit comes with an optical mouse and a choice of industry-standard keyboards. The unit can operate on thick and thin Ethernet networks as well as on RS-232C or RS-422 serial communications links. The unit can support TCP/IP and DECnet protocols as an option. The company's X server software is either resident in firmware or downloadable from the host. $2975 with 2M bytes of RAM and grayscale.

Visual Technology Inc, 120 Flanders Rd, Westboro, MA 01581. Phone (508) 836-4400. FAX (508) 366-4337. **Circle No. 383**



X-Window Terminal

- *Contains a 19-in. screen with 1024×800 pixels*
- *Simultaneously accesses hosts running Unix, VMS, UL-TRIX*

The NCD19b X-Window terminal can simultaneously access host computers running Unix, VMS, or UL-TRIX operating systems. A 16-MHz MC68000 μP drives the text, windowing, and 2-D graphics displays. The unit contains a single gate array that performs more than 40 discrete functions such as graphics control, memory control, and display control. It comes with 2M bytes of dynamic RAM, which is upgradable to 5M bytes using single in-line memory modules (SIMMs). The unit comes with a 19-in. screen that has a resolution of 1280×1024 pixels. The terminal supports a variety of communications protocols including TCP/IP, SLIP, DECnet, and the company's XRemote for local and remote serial communications. It works with any graphics user interface including OSF/Motif,

Openlook, or Xview. $2295 with 2M bytes of RAM.

Network Computing Devices Inc, 350 N Bernardo Ave, Mountain View, CA 94043. Phone (415) 694-0650. FAX (415) 961-7711.

Circle No. 384

Expansion Units

- *Connect to the expansion port on T3100SX laptop*
- *Let user add PC expansion cards to the computer*

The WonUnder and WonUnder II are expansion units for Toshiba's T3100SX laptop computer. The WonUnder consists of a metal card carrier, which accommodates a PC expansion card that is 11 in. or less in length. An interface card plugs into the laptop's expansion port. Its small size lets the card fit in a Toshiba carrying case with the computer. The WonUnder II consists of an expansion chassis that can accommodate full-size PC expansion cards. An interface card attaches to the expansion port of the computer. The card comes with an interface cable and an external power supply. Both units permit the laptop computer to utilize PC expansion cards such as network cards, VGA cards, or additional memory cards. WonUnder, $379; WonUnder II, $479.

Connect Computer, 9855 W 78th St, Suite 270, Eden Prairie, MN 55344. Phone (612) 944-0181. FAX (612) 944-9298. **Circle No. 385**

Master Or Slave CPU Board

- *Uses V25 μP in an all-CMOS design for STD Bus*
- *Works as embedded controller or I/O board from −40 to +85°C*

The 8825 all-CMOS CPU board for the STD Bus uses an NEC V35 μP. Programmable gate arrays from Xilinx allow the board to function as either a master or slave on the bus. The board has the following embedded-controller features: an interrupt controller; two serial ports; 16 parallel ports; two 16-bit timer/counters; a real-time clock; a watchdog timer; and a battery-backed static RAM (SRAM). Four JEDEC sockets provide 512k bytes of EPROM and 256k bytes of SRAM. The board also has an SBX expansion connector for expanding the slave board's peripheral functions and an option for an analog I/O channel. You can digitize eight analog input channels with 12-bit accuracy. You can set the analog output at 4 voltage ranges with 8-bit accuracy. Communication with the host is either via interrupts or by a message. The host can transfer a message through the board's dual-port

Text continued on pg 161

Mixed-signal ASICs

NCR

Face it, a lot of designers have mixed feelings about mixed-signal ASICs.

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And in addition, NCR has a mixed-signal test environment created specifically to test Analog/Digital ASICs without compromising either domain.

All this has resulted in NCR being ranked #1 in worldwide cell-based mixed-signal ASIC suppliers*.

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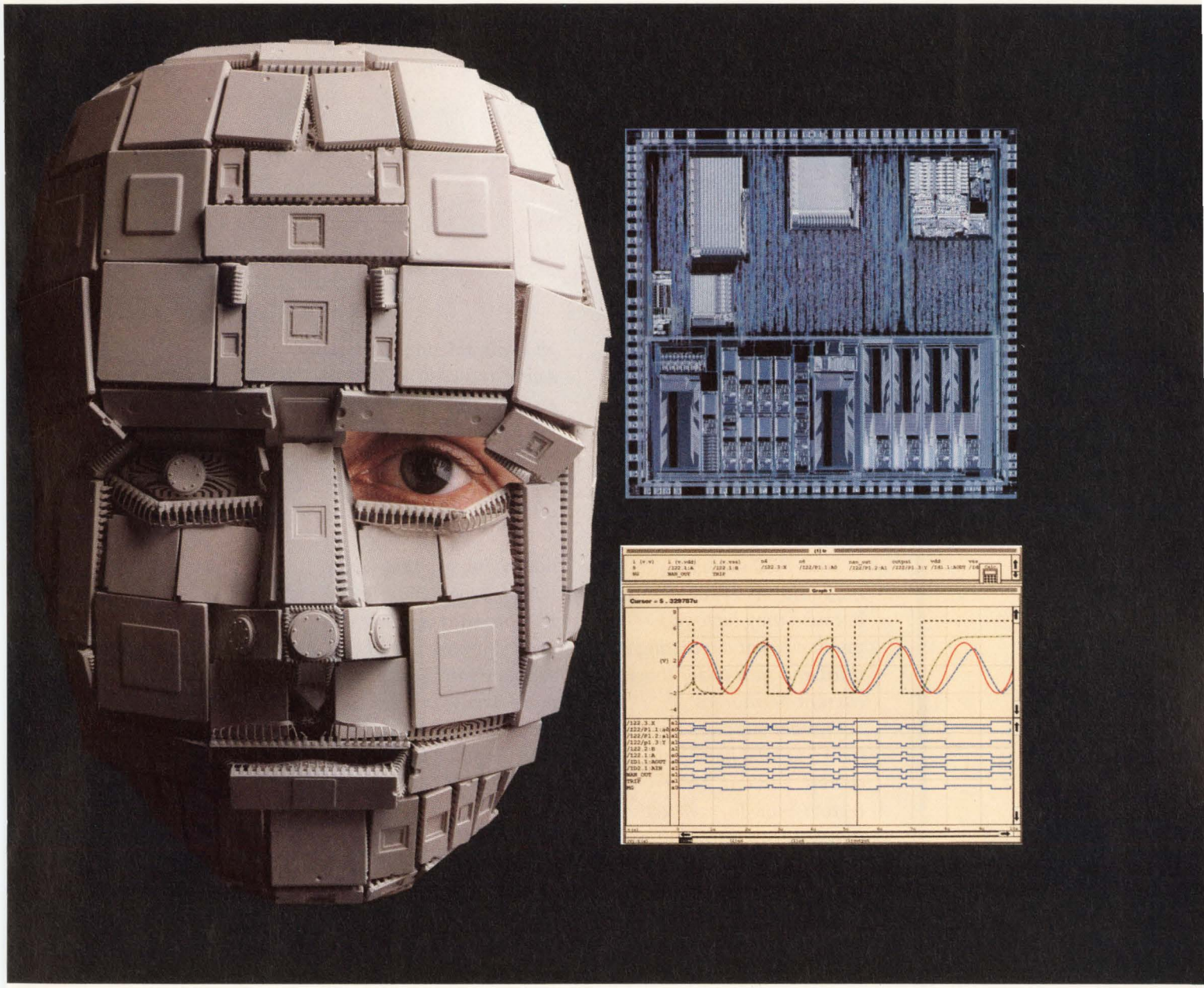

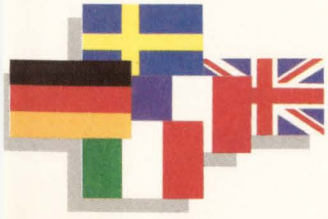

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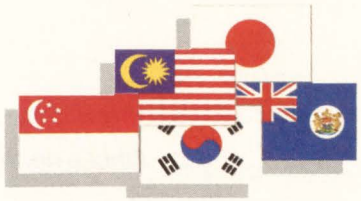


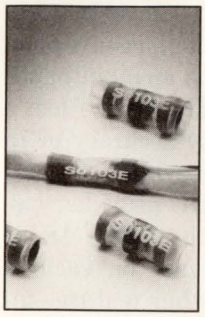
Asia/Pacific Sales Headquarters
2501 Vicwood Plaza
199 Des Voeux Road
Central Hong Kong
852 859 6044

CIRCLE NO. 86

3M Introduces Heat Shrinkable Cable Shield Terminators

Meet MIL-S-83519 for one-step soldering of ground wires to cable shielding

AUSTIN, Tex. – New 3M brand MIL-S-83519 shield terminators provide an insulated, environmentally protected strain relieved solder termination.



3M shield terminators are available in five diameters with and without pre-installed ground leads per MIL-S-83519.

A red thermochromic indicator is included in the solder flux. When sufficient heat has been provided for complete melting it becomes colorless, thus helping the technician know the soldered joint is complete.

Six alpha numeric characters in contrasting ink provide MIL spec markings that are clearly visible before and after application to assist quality control inspections.

Environmentally and mechanically protected solder connections are the result of a three part process:

1. The outer sleeve shrinks
2. The solder preform melts and flows, completing the connection
3. The thermo plastic insert melts to provide a seal

To aid in the correct application of these heat shrinkable shield terminators, 3M offers heating devices, MP-700 for hot air, ST-3000 for infrared.

The completed assembly provides thermal and electrical insulation, identification, strain relief, moisture sealing and chemical protection.

For more information contact a 3M Electrical Specialties Division representative or authorized distributor or call 1-800-322-7711.

3M Electrical Specialties Division
PO Box 2963
Austin, Texas 78769-2963

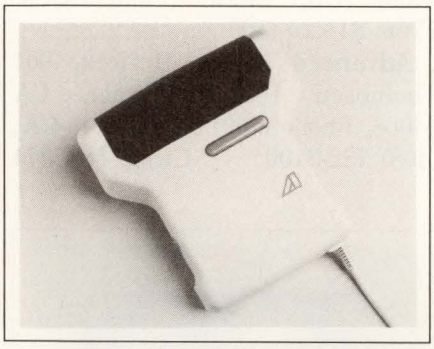
3M

CIRCLE NO. 16

COMPUTERS & PERIPHERALS

RAM. The board operates from −40 to +85°C. Basic configuration, $395; maximum configuration, $605.

Systek, 415 N Quay St, Suite 6, Kennewick, WA 99336. Phone (509) 735-1200. **Circle No. 386**



Handheld Grayscale Scanner

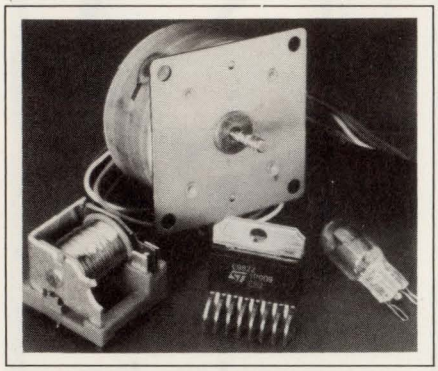
- *Renders 256 different shades of gray*
- *Scans images with 400-dpi resolution*

The NuScan PC Grayscale Scanner is a handheld grayscale scanner for IBM PCs and compatible computers. It can interpret 256 continuous tones of a photograph using a hardware method instead of a software method. It scans an image with 400-dpi resolution. The scanner comes with OCR software, which supports most common fonts, typefaces, and character sizes ranging from 8 to 36 points. A unique feature of the software is that it can append and merge functions, allowing the user to sew together text from multiple vertical or horizontal scanner passes. The software can read at 20 to 80 sec/page on 80286 or 80386 computers with a minimum of 2M bytes of memory. The scanner has a scan width of 4.1 in., and it can scan a page as long as 14 in. A window on the scanner permits visual scan alignment. The scanner measures 5.4 × 1.3 × 5.6 in., and it weighs 0.7 lbs. $399.

Asuka Technologies Inc, Von Karman Commerce Center, Suite 110, 17145 Von Karman Ave, Irvine, CA 92714. Phone (714) 757-1212. **Circle No. 387**

NEW PRODUCTS

INTEGRATED CIRCUITS



Smart-Power Chip

- *Rated at 750 mA/driver*
- *Includes diagnostic functions*

Featuring eight low-side drivers in a single 15-lead multiwatt package, the L9822 smart-power chip can deliver 750 mA continuously from each driver. All eight drivers can operate simultaneously. The device is controlled through a 4-wire serial bus, which is used both to load a control byte and read a status byte. This diagnostic feature allows a microcontroller to detect fault conditions due to overloads or open-circuit outputs. When an overload is detected, the device turns off the faulty driver to prevent damage. The chip's outputs are also protected by internal 34V zeners that suppress overvoltages caused by inductive loads. $3.50 (1000).

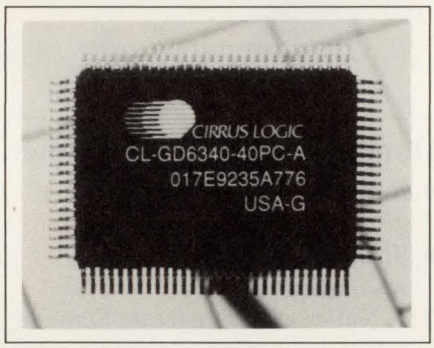
SGS-Thomson Microelectronics, 1000 E Bell Rd, Phoenix, AZ 85022. Phone (602) 867-6100. FAX (602) 867-6290. **Circle No. 373**

1M-Bit Flash Memory

- *Features small die size*
- *Has 90-nsec speed*

Fabricated in 1.0-μm CMOS, the Am28F010 1M-bit flash memory has a die size of about 45k mil^2. The next smallest competitive offering has a die size of about 60k mil^2, according to the company. The device also features an access time of 90 nsec; its nearest competitor has an access time of 120 nsec. The device is rated at 12V and organized as 128k × 8 bits. It is available in three temperature ranges. Package options include 32-pin DIPs, plastic leaded chip carriers, and LCCs. From $18.20 (100).

Advanced Micro Devices, 901 Thompson Pl, Sunnyvale, CA 94088. Phone (800) 222-9323; in CA, (408) 732-2400. **Circle No. 374**



Color LCD Interface Controller

- *Provides as many as 256 colors*
- *Has 64 shades of gray*

Used as an interface controller between a VGA controller and an LCD panel, the CL-GD6340 provides digital signals for a color or monochrome LCD and analog signals for CRT presentation. In accordance with the VGA standard specifications, the chip allows the simultaneous display of as many as 256 colors. The chip can also produce 64 shades of gray on monochrome panels. Although its primary application is expected to be in active-matrix thin-film-transistor LCDs, the interface controller supports other LCD panels such as multiplexed supertwist types. In addition to its ability to drive both an LCD panel and a CRT screen at the same time, the chip is also usable with other display technologies, including gas plasma and electroluminescent panels. Included in the CL-GD6340 is a complete RAM D/A converter with a color look-up table. 100-pin quad flatpack, $68 (100).

Cirrus Logic Inc, 1463 Centre Pointe Dr, Milpitas, CA 95035. Phone (408) 945-8300. FAX (408) 263-5682. **Circle No. 375**

Dual-Channel 18-Bit ADC

- *Conversion speed is 10 μsec*
- *Input bandwidth is 50 kHz*

Operating from a single 5V supply, the AT76C120 A/D converter features 18-bit resolution, a conversion speed of 10 μsec, and an input bandwidth of 50 kHz. The device has a guaranteed linearity accuracy of 15 bits and can resolve input signals of <10 μV. The ADC provides system designers with 96,000 18-bit conversion samples/sec on each of its two channels. Other features include a minimum S/N ratio of 86 dB and a 2's-complement format for the device's digital-output code. In a 24-pin plastic DIP, $25 (1000).

Atmel, 2125 O'Nel Dr, San Jose, CA 95131. Phone (408) 441-0311. **Circle No. 376**

"Kickstarter" Chip

- *Moves control to the keyboard*
- *Isolates ac power line*

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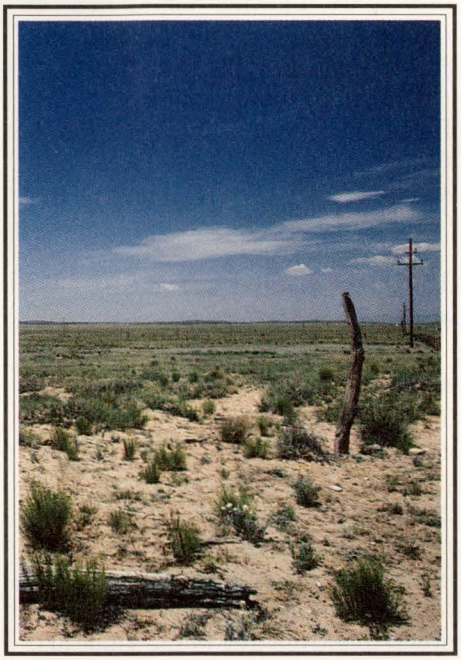

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is off, a pushbutton closure is detected by the chip, which then sources a small amount of energy from a 3V lithium battery. This energy lights an optoisolator to kick on a triac, which powers up the system. The chip also monitors a second pushbutton to reset a processor when the operator wants to intervene. The DS1239 also has provisions to monitor power. If the 5V power supply dips out of tolerance, a warning signal interrupts the processor, allowing for storage of information in nonvolatile RAM. $3.50 (1000).

Dallas Semiconductor, 4350 S Beltwood Pkwy, Dallas, TX 75244. Phone (214) 450-0448. FAX (214) 450-0470. **Circle No. 377**

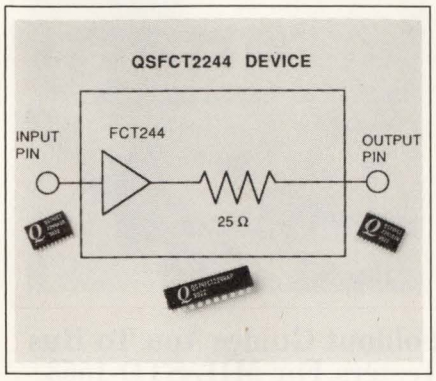
16k-Bit Quad-Port RAM

- *Has four 256 × 16-bit segments*
- *Handles clock rates to 20 MHz*

The PDSP16520 quad-port RAM contains a total of 16k bits of dual-port static RAM arranged in four 256 × 16-bit segments. These segments are supported by two 16-bit input buses and two 16-bit output buses, with each memory quadrant accessible from any of the input and output ports. In order to synchronize all events to a common system clock, the chip's address, data, and control inputs together with its data outputs are fully registered. The system clock initiates the memory cycles; data rates to 20 MHz are possible. Within this 20-MHz clock period, the circuit can read data from any two of the memory blocks as well as write new data to any two blocks. Separate inputs for both read and write addresses are available and, when both addresses specify the same location, the circuit reads the old data before writing new data. As a further aid to system integration, the user can program a delay between 0 and 15 clock cycles before the write operation specified on the input pin actu-

ally occurs. The PDSP16520 comes in a 144-pin pin-grid-array package. £150 (100).

Plessey Semiconductors Ltd, Cheney Manor, Swindon, Wiltshire SN2 2QW UK. Phone (793) 518000.
Circle No. 378



Logic Family With Built-In Resistors

- *Saves board space*
- *Reduces ground bounce*

A family of FCT2000A logic devices comes with built-in 25Ω series resistors to save board space and reduce ground bounce, undershoot, and ringing. Ground-bounce noise is limited to 0.8V, with similar reductions in the other parameters. The devices are particularly useful in high-speed, high-capacitance load applications such as static-RAM and dynamic-RAM arrays in RISC and CISC systems. Worst-case delays are 4.8 nsec for the FCT2244A buffer, 5.2 nsec for the FCT2373A latch, and 6.5 nsec for the FCT2374A register. Available in plastic DIPs, ZIPs, and SOIC packages. $3.38 to $5.96 (100).

Quality Semiconductor Inc, 2946 Scott Blvd, Santa Clara, CA 95054. Phone (408) 986-8326. FAX (408) 496-0591. **Circle No. 379**

14-Bit S/D Converter

- *Comes in a small-size package*
- *Has a velocity-output pin*

Based on a proprietary single-chip monolithic R/D converter, the hybrid SDC-14570 Synchro/Resolver-to-Digital Converter comes in a space-saving 1×0.8-in. package. The device also features a 4V velocity-output signal with a linearity of 1% that you can use to replace a tachometer. The converter is available with operating temperature ranges of 0 to 70°C and −55 to +125°C. You can also order the device with MIL-STD-883 screening. The converter comes in a hermetic 26-pin double DIP. From $330. Delivery, stock to 60 days ARO.

ILC Data Device Corp, 105 Wilbur Pl, Bohemia, NY 11716. Phone (516) 567-5600. FAX (516) 563-5699. **Circle No. 380**

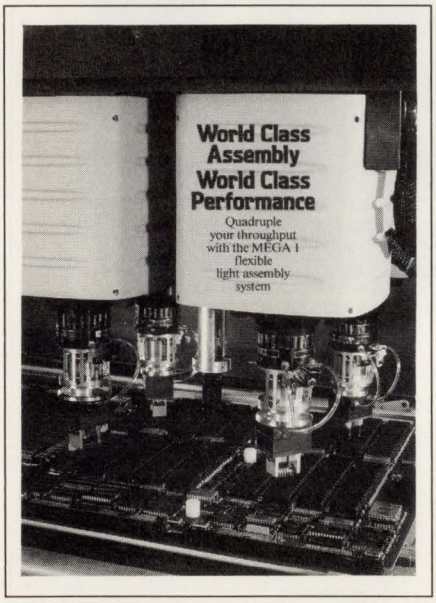
LITERATURE

Test-Instrument Brochure, App Note For Test Setup

These two publications provide complementary information on how to solve the problem of characterizing ICs with a stimulus-response setup. The 4-pg brochure *How are You Going to Test This?* describes the HP 8131A programmable pulse generator and the HP 54120 family of high-frequency digitizing oscilloscopes. Application Note 381, *A Test Setup for Characterizing High-Speed Logic Devices*, explains a characterization of a GaAs flip-flop using the instruments discussed in the brochure.

Hewlett-Packard, 19310 Pruneridge Ave, Cupertino, CA 95014.

Circle No. 388



Anticollision Software Presented

The 6-pg foldout brochure *World Class Assembly, World Class Performance* covers the Mega 1 robotic multiple-head system for complex assemblies in manufacturing applications, including electronics and automotive production. The publication explains how the software uses bidirectional linear motors, frictionless air bearings, and anticollision technology to operate as many as four robotic heads simultaneously. It also describes an optional vision system that allows single-move parts positioning. The brochure's 4-color photos illustrate the unit's programming, which uses the industry-standard C language.

Megamation Inc, Box 2328, Princeton, NJ 08543.

Circle No. 389

Publication Presents Gauging System

This 14-pg brochure features the Metro Program of incremental-length gauges for checking the accuracy of other gauges and inspection equipment. The 4-color publication provides specifications, descriptions, and illustrations.

Heidenhain Corp, 115 Commerce Dr, Schaumburg, IL 60173.

Circle No. 390

Charting Your Way To Data-Bus Products

This data-bus product-selection chart provides an at-a-glance guide to more than 30 characteristics of data-bus products for MIL-STD-1553 applications. Color-coded tabulations highlight the 2-sided chart, which lists single and dual transceivers, bit processors, remote terminal units, interfaces, card assemblies, and testers.

ILC Data Device Corp, 105 Wilbur Pl, Bohemia, NY 11716.

Circle No. 391

Reprint Explains Stability Testing

Stability Testing of Type K, N, J, and E Thermocouples at 538°C is a reprint of a paper presented at the American Society of Mechanical Engineers Cogen-Turbo III Symposium. The paper's tables, graphs, and references illustrate the discussion in the text.

Thermo Electric, 109 N Fifth St, Saddle Brook, NJ 07662.

Circle No. 392

Foldout Guides You To Bus Testers For MIL-STD-1553

The *Engineer's Guide To MIL-STD-1553 Modular Bus Testers* tells you how to use the 1553 Bus Tester, which tests and evaluates 1553A/B terminals and systems. The 6-pg foldout brochure describes the Tester's capabilities and shows you how to economically match testing requirements with the proper Bus Tester model.

Test Systems Inc, 217 W Palmaire, Phoenix, AZ 85021.

Circle No. 393

Military/Aerospace Relays Listed

The 32-pg catalog spotlights a range of relay lines for military and aerospace applications. The catalog covers time-delay, dry-reed, mercury-wetted, magnetic-polarized, and general-purpose relays. It also presents a line of relays that includes minigrid, TO-5 case, crystal-can, solid-state, RF and time-delay devices, power monitors, and voltage sensors. An index arranged according to military specifications and a cross reference to military part numbers help you select parts.

Struthers-Dunn Inc/Hi-G Co, Lambs Rd, Pitman, NJ 08071.

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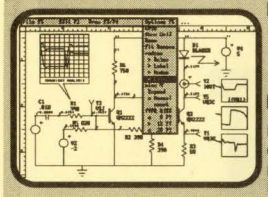

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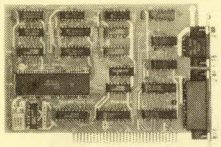
PC Communications Coprocessors



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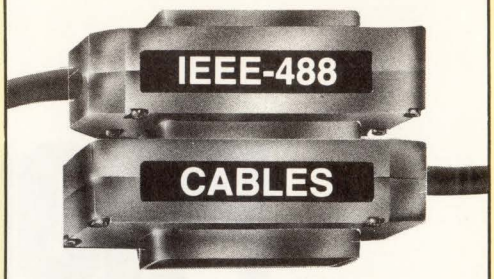

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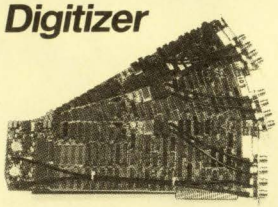

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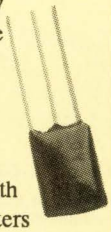

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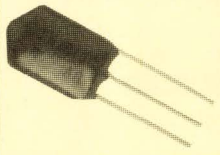

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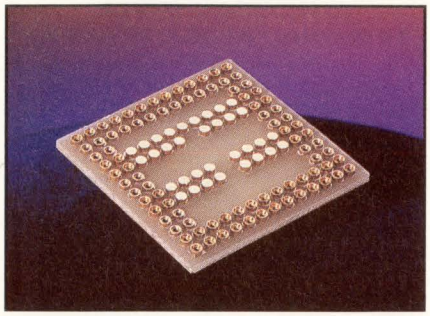

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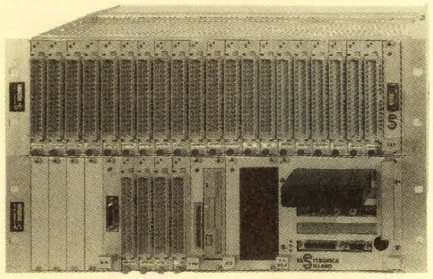

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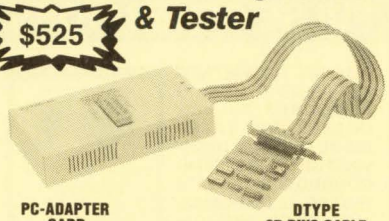

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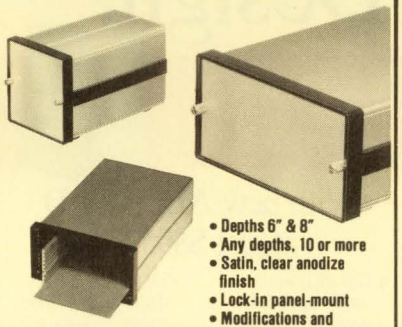

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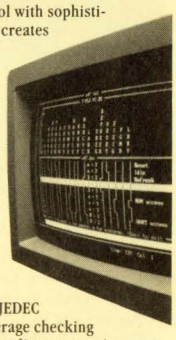

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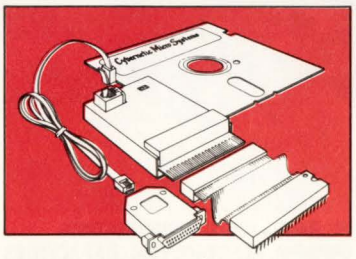

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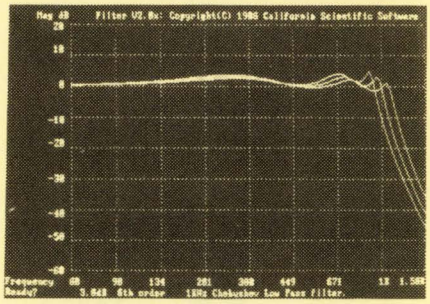

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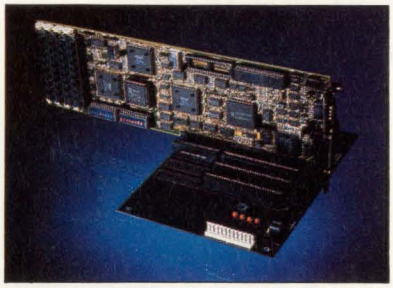

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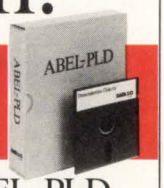

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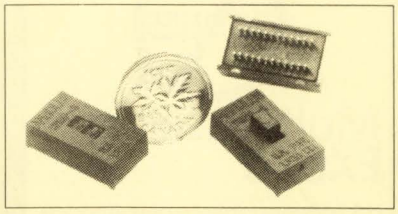

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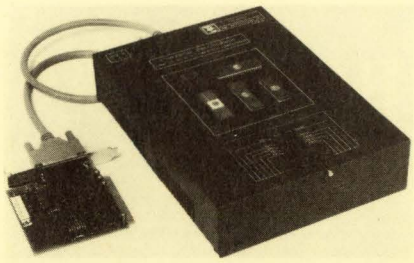

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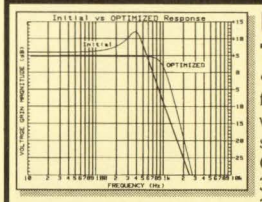

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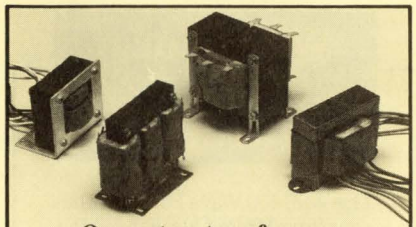

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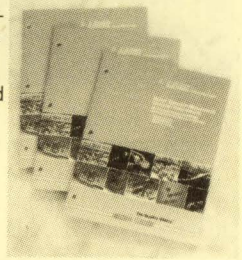

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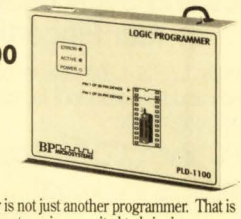

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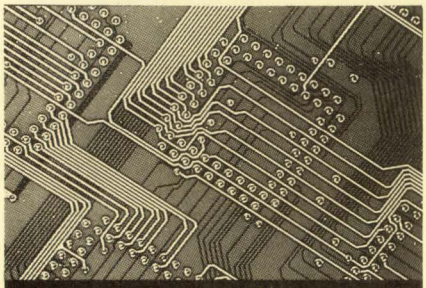

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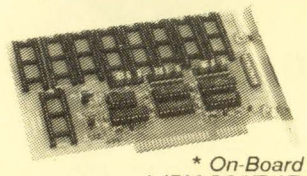

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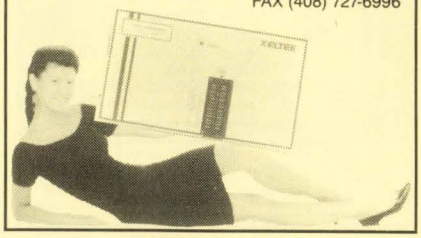

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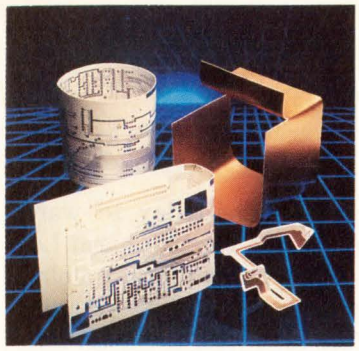

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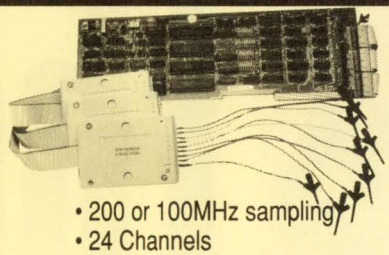

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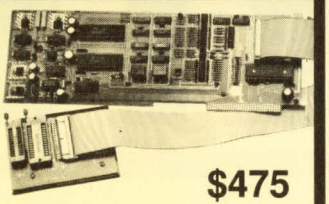

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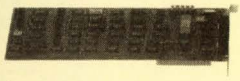

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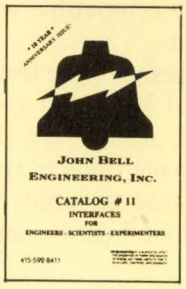

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KEEPER of the FAITH

Richard Stallman is leading a crusade to preserve your programming freedom.

Jay Fraser, Associate Editor

Photography by Kevin Bryan

"We've come here today to warn the public of the terrible harm Lotus and other companies are doing to the software industry," shouted the intense man with the long, tangled, black hair.

The crowd of about 300 people cheered and applauded.

"We can win. We're going to have to work hard and get lots of other people to join with us, but we can do it," he went on.

Again the crowd cheered and waved signs reading "Stop Software Monopolies," "Lotus Interruptus," and "A Real Company Competes. Wimps Sue!"

This protest rally took place on August 2 in Cambridge, MA at the headquarters of Lotus Development Corp. Lotus was targeted because two months earlier it had won a lawsuit against Paperback Software International of Berkeley, CA for copyright infringement. Lotus claimed Paperback's VP Planner illegally imitated the commands and user interface of its popular 1-2-3 spreadsheet. The people at the rally viewed Lotus's suit as an attack on programmers' traditional freedom to write programs that are compatible with existing software.

"There are people here from New Hampshire and Maryland and from companies all around the Boston area. It makes me think of the Minutemen," the man shouted. "So let this be the shot heard round the world!"

The crowd cheered once more.

"Now let's spend the rest of the afternoon marching around the Lotus building chanting our hex chant," he said, finishing his speech.

A picket line formed on the sidewalk and began a chant based on the hexadecimal counting system.

"1-2-3-4 Kick the lawsuits out the door!

5-6-7-8 Innovate don't litigate!

9-A-B-C Interfaces should be free!
D-E-F-0 Look and feel has got to go!"

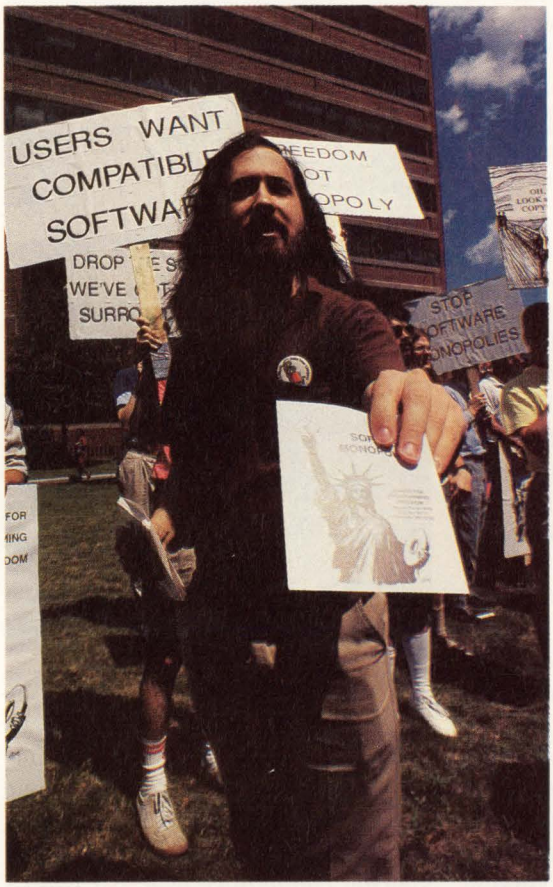
The speaker at the rally was Richard Stallman, 37, a gifted programmer and tireless crusader for the freedom of anyone who writes or uses software. He is the founder of the Free Software Foundation (FSF) and cofounder and president of the League for Programming Freedom.

Stallman spends most of his time in a cluster of cramped offices near MIT (Cambridge, MA). The floors and furniture are strewn with last week's newspapers, empty Chinese food take-out cartons, and paperback science fiction novels. Stallman himself looks like he never left the late 1960s. For an interview he's barefoot. His unruly hair falls halfway down his back. And he wears a loose, unbleached cotton shirt with a button pinned on it that reads "Keep Your Lawyers Off My Computer!"

Stallman clears a space on a couch, sits down, and folds his legs under him. As he talks about programming freedom he speaks calmly, but with the same intensity he displayed at the rally.

"Any kind of monopoly on any activity is automatically an affront to individual freedom," he says, "and those things can only be justified when there's a public gain that's worth the price. I totally reject the idea that people are entitled to be paid whenever anyone benefits from something they have done. And, by the way, the American legal system also rejects that idea. There is no basis for it except in right-wing ideology.

"The Constitution, when it establishes the basis for patents and copyrights, says very clearly that they are not an entitlement," he adds. "They are something that can be established to promote progress. In other words, they are a means of altering the behavior of the public for the public good. They are not a matter of fairness. No one is entitled to a patent, independent of whether the government sees fit to establish them."



Stallman discovered the world of programming when he was 12 years old. At summer camp he came across a computer manual that belonged to one of the counselors. There were no computers at the camp, but that didn't deter him. Stallman devoured the book and began creating programs in his mind. He has been hooked ever since.

While he was in high school Stallman wrote programs for IBM. He went to Harvard University (Cambridge, MA) and graduated with a BS in physics in 1974. By then he was already working at the Artificial Intelligence Laboratory at MIT.

The 1970s were the glory years of the AI Lab. A group of programmers who would become legendary gathered there under the extremely loose supervision of Professor Marvin Minsky, known as the father of artificial intelligence. These hackers, as they proudly called themselves, explored the outer limits of what computers could do. Steven Levy wrote of them in his book *Hackers: Heroes of the Computer Revolution*: "Beneath their often unimposing exteriors, they were adventurers, visionaries, risk-takers, artists . . . and the ones who most clearly saw why the computer was a truly revolutionary tool."

The hackers in the AI Lab produced everything from elegantly written languages to sophisticated computer games to the powerful LISP (List Processing) machine, the AI programmer's dream computer. Something else came out of the AI Lab, too—the hacker ethic. The hacker ethic was never codified or published or even written down. It evolved naturally from the temperaments and convictions of the people in the Lab, and it permeated the way they worked.

The hacker ethic is based on unlimited freedom of information and unhindered cooperation. If someone writes a program, the hackers believed, anyone else should be free to modify or expand it. In that way, programs will be refined and improved until the best possible version is created, and that program should also circulate freely. Working this way will prevent duplication of effort, promote creativity, and raise the level of programming for everyone.

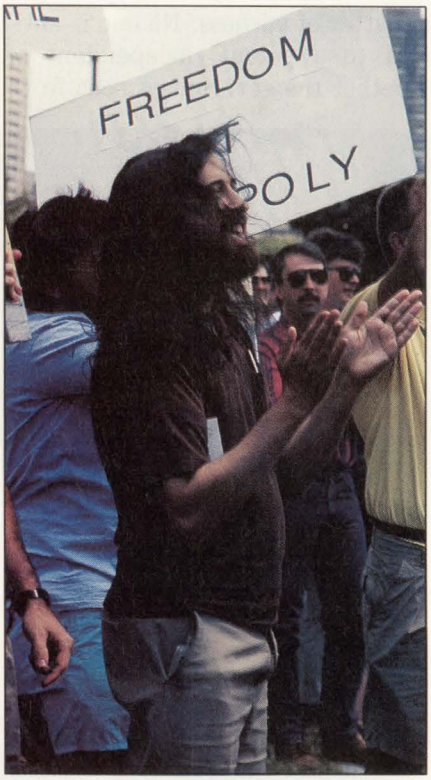
Richard Stallman is a true believer in the hacker ethic. While he was working at the AI Lab, he wrote a text-editing program called EMACS. He deliberately created it with an open architecture to encourage changes and additions, and he gave it away free as long as the people who received it promised to send him any improvements they made.

The development of the LISP machine eventually destroyed the original AI Lab. When a prototype of the computer was completed in 1979, the hackers who had worked on it agreed that they should start a company to manufacture and sell it. But they disagreed on what form the company should take. One faction wanted a small, loose-knit organization that operated in the same communal way as the AI Lab. The other faction wanted a larger, more conventionally structured firm with a professional management team brought in to take care of business matters. The two sides couldn't reach a compromise. They started different companies, LISP Machine Inc and Symbolics, and each came out with its own version of the LISP machine in the early 1980s.

The deep wound in the AI Lab never healed. What had once been a family eventually became two rival camps. The free flow of information stopped. Many of the hackers who remained were hired away by one company or the other. Work in the Lab practically ceased. The golden era was over.

Richard Stallman was the last of the original hackers to remain in the AI Lab. He was depressed and angered by its disintegration. He wasn't interested in going to work for someone else and he still held firmly to the hacker ethic, so there was only one thing for him to do.

"I decided that it wasn't worth continuing in the software field without being able to cooperate with people and to write and improve whatever program you want to improve," he says. "I decided that I would make a new software-sharing community even if I had to write all the software myself."



Early in 1984 Stallman resigned from MIT and founded the FSF. The goal of the organization is to develop a complete, Unix-compatible software system (called GNU for Gnu's not Unix) and give it away. The reason Stallman severed his ties with MIT was to make sure it would have no legal right to the software he intended to write.

The FSF has no members, just volunteers. It exists mainly on donations of money and equipment. Most of the money goes to hire programmers and technical writers. Stallman says the FSF has considerable support on campuses across the country and within the computer industry. For example, Hewlett-Packard recently donated $100,000 and six of its 68030 workstations to the FSF.

Approximately two-thirds of GNU has been written and parts of it have already been distributed. In order to make sure that GNU programs circulate freely, Stallman has protected them with what he calls a "copyleft." A copyleft is a legal instrument that gives people the freedom to change and distribute GNU programs at will, but prevents anyone from trying to copyright and sell or license a modified version.

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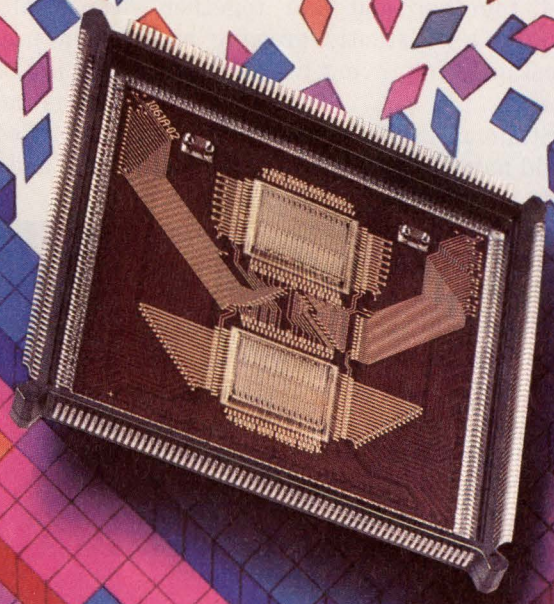

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"People have the opportunity to join into cooperation," says Stallman, "but once they've decided to join into cooperation they can't turn around and start being uncooperative with somebody else. So all the improvements people make sort of add together and add together, making a constantly growing and constantly improving body of software."

Stallman's skills as a programmer could have made him wealthy a long time ago. Instead he has chosen to earn just enough money from consulting work to get by on and to live an almost ascetic lifestyle. Recently, however, he was given $240,000 to use in any way he wants.

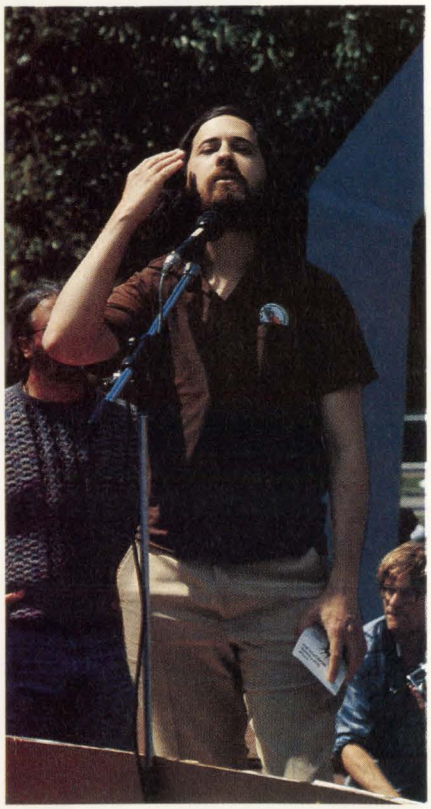
On July 17 the MacArthur Foundation in Chicago, IL announced that Stallman had been awarded a "genius fellowship" of $240,000. These grants are given to, in the words of the Foundation, "exceptionally gifted individuals" to free them from economic constraints so they can devote themselves full-time to their pursuits.

Stallman is pleased with the grant and a little amused by it. "The money by itself doesn't really change anything for me," he says. "I'm not materialistic in the way a lot of Americans are, wanting as many possessions as possible. What I want is to be as far away from any worries about a shortage of money as possible."

Stallman hasn't decided what he's going to do with the money yet. He may use some of it to support programmers he knows. He may use some to learn how to play Indonesian gamelan music. The only thing he has definitely decided on is to travel to the Soviet Union to accept an invitation to speak about free software.

Recently, much of Stallman's time and effort have gone into fighting the attempts of some companies to monopolize common user interfaces through copyrights. The demonstration in front of Lotus's headquarters was a protest against this new and controversial practice.

The case of Lotus vs Paperback Software was very important because although Paperback's program used a different code than that in Lotus 1-2-3, many of its commands and keystrokes were the same. Because of this similarity of "look and feel" the judge ruled that



Lotus's copyright had been violated. After its victory in court, Lotus immediately filed suit against two more small software companies. Also, Apple Computer is now suing Microsoft and Hewlett-Packard, alleging that those companies violated its copyright on the Macintosh computer interface. Stallman and others believe that a very dangerous precedent has been set.

"Restrictions like these can easily wipe out meaningful competition," says Stallman. "User interface copyrights can make it nearly impossible to compete with an established, standard product, because the users all know a certain set of commands. If you can't implement those commands, they won't want to relearn to switch brands.

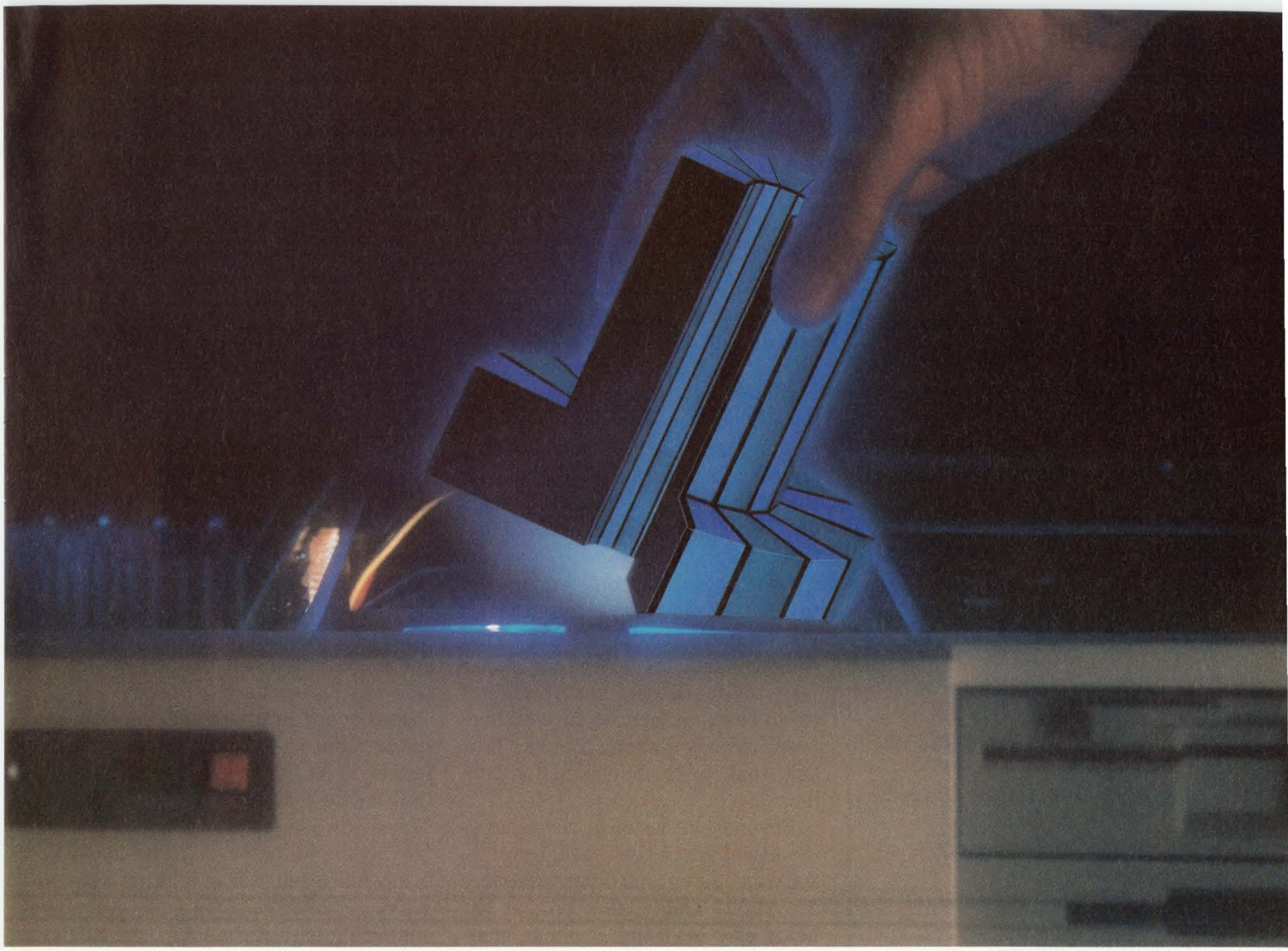
"Imagine what it would be like for someone to try to make a typewriter with the keys arranged in a funny layout," he explains. "You can see what that would be like—utter havoc. The point is that people probably wouldn't even bother trying because it's so obviously not feasible."

In Stallman's eyes, another equally serious threat to software developers' freedom is software patents. The US Patent Office began granting patents on software in 1981. Thousands of them have been issued so far, and they cover many common and widely used functions.

"Natural-order recalc" is just one example. This feature recalculates all of the entries in a spreadsheet when a user changes one. It's now covered by a patent. If someone wishes to incorporate it into a program, he either has to pay a licensing fee or risk a lawsuit. Most programmers don't realize how many common techniques are now restricted by patents, and being unaware that a patent exists is no excuse before the law. You can still be sued.

The proliferation of patents could make writing software ruinously expensive. Software developers would have to license patents from dozens or even hundreds of holders. That alone would be costly. But to find out which patents might be infringed, developers also would have to conduct patent searches.

"If you wanted to write a program, say 50,000 lines long, you



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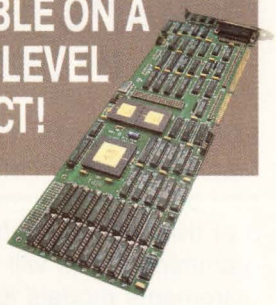

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might have in that program 100,000 basic components," says Stallman. "You'll have hundreds of techniques. You can have thousands of combinations of techniques that actually are meaningful associations. If you wanted to do a patent search for those it would cost you two or three thousand dollars each. Now you're talking about millions of dollars.

"And this would only enable you to find out what was patented, so you wouldn't use it," he adds. "That doesn't mean there'd be any other way to do things, and it doesn't mean that you can be sure. Whenever anybody's wrong there's a lawsuit that costs maybe half a million."

Beyond the issue of the sharply increased costs they would create, software patents and user-interface copyrights also strike right at the heart of everything Stallman cherishes most—the hacker ethic of cooperation, sharing, and a free flow of information.

To combat these threats, Stallman and two friends founded the League for Programming Freedom in October of 1989. In less than a year and with limited publicity the League has grown to 150 dues-paying members. Stallman receives about 20 letters each day seeking information about it.

"The League is an organization of programmers and users of computers who want to reverse the new monopolies that have recently been instituted—the user-interface copyrights and software patents," says Stallman. The League is growing rapidly "because people who didn't take the threat seriously now know that we can't expect the courts to understand the software field or respect the traditions of the field. People know it's up to them to solve the problem."

Stallman is guardedly optimistic about the future. "There's a good chance but not a great chance that the Supreme Court will overturn the lower court's decision," he says. The trend toward more software patents could also be reversed by other means. "It would be easy to reverse it. Congress could pass a law that patents don't apply to software," he explains. "The problem is that the few people who have something to gain from software patenting may be better organized and more aware of it than the many who have something to lose."

Is Richard Stallman making a futile attempt to recapture a lost utopia, or is he fighting a very important battle that he just might win? Time will answer those questions. Meanwhile he can usually be found in his cluttered office, writing programs for his free software system, answering inquiries about the FSF, and planning ways to mobilize public opinion in favor of programming freedom, still keeping the faith.

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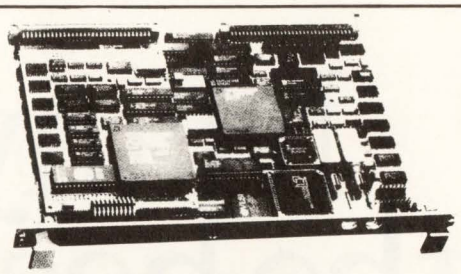

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- VMEbus architecture desired.
- C language programming experience required.
- BSEE or equivalent required. Emphasis on high-speed microprocessor development.

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- UNIX, Kernal I/O, TCP/IP or other protocol experience on super-microcomputer or mini-computer required.
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- C language programming experience required.
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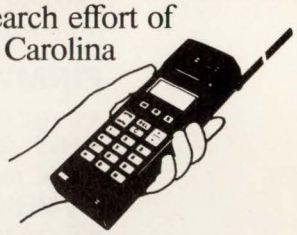

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Requires CAD experience, preferably on Mentor Workstations and microprocessor design knowledge. BSEE/CS with 2+ years IC experience.

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1-2 years experience; BS degree minimum. Experience in semiconductor environment strongly preferred. Must have familiarity with air abatement programs.

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Process Engineer
2-3 years experience in photolithography with ASM steppers preferred; BS/MSEE.

Fab Equipment Engineer
4+ years wafer fab experience required with specialty in wafer processing equipment; BS/MSEE.

Process Engineers
2-3 years experience in implant, thin films, diffusion, or etch in wafer fab area. BSEE/CE or Physics.

Qualified applicants should send a resume to: **Advanced Micro Devices, MS-556, 5204 E. Ben White Blvd., Austin, Texas 78741.** For product line openings, **attn: Paul Maack or Scott Saunders** and for manufacturing line openings, **attn: Ed Moore. You may also call 1-(800) 531-5202 or FAX your resume to (512) 462-5108.**

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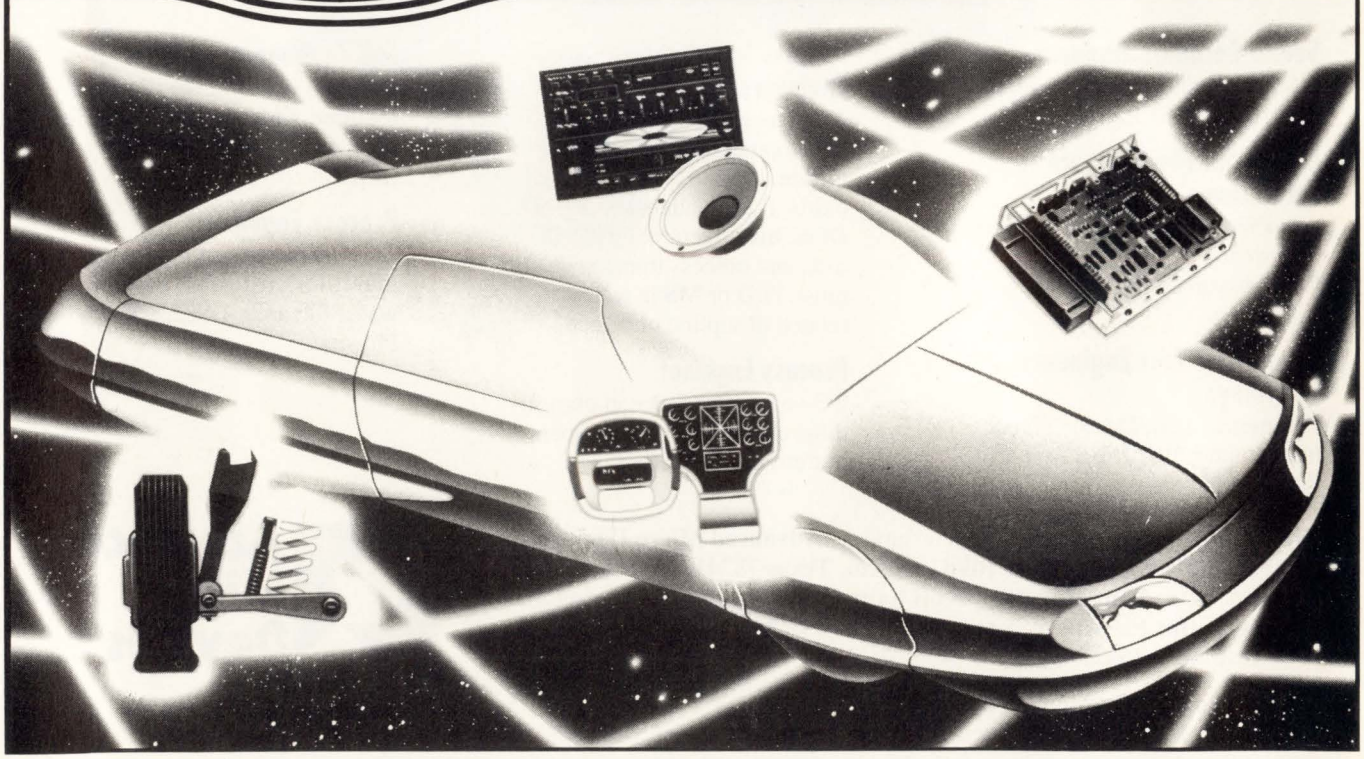

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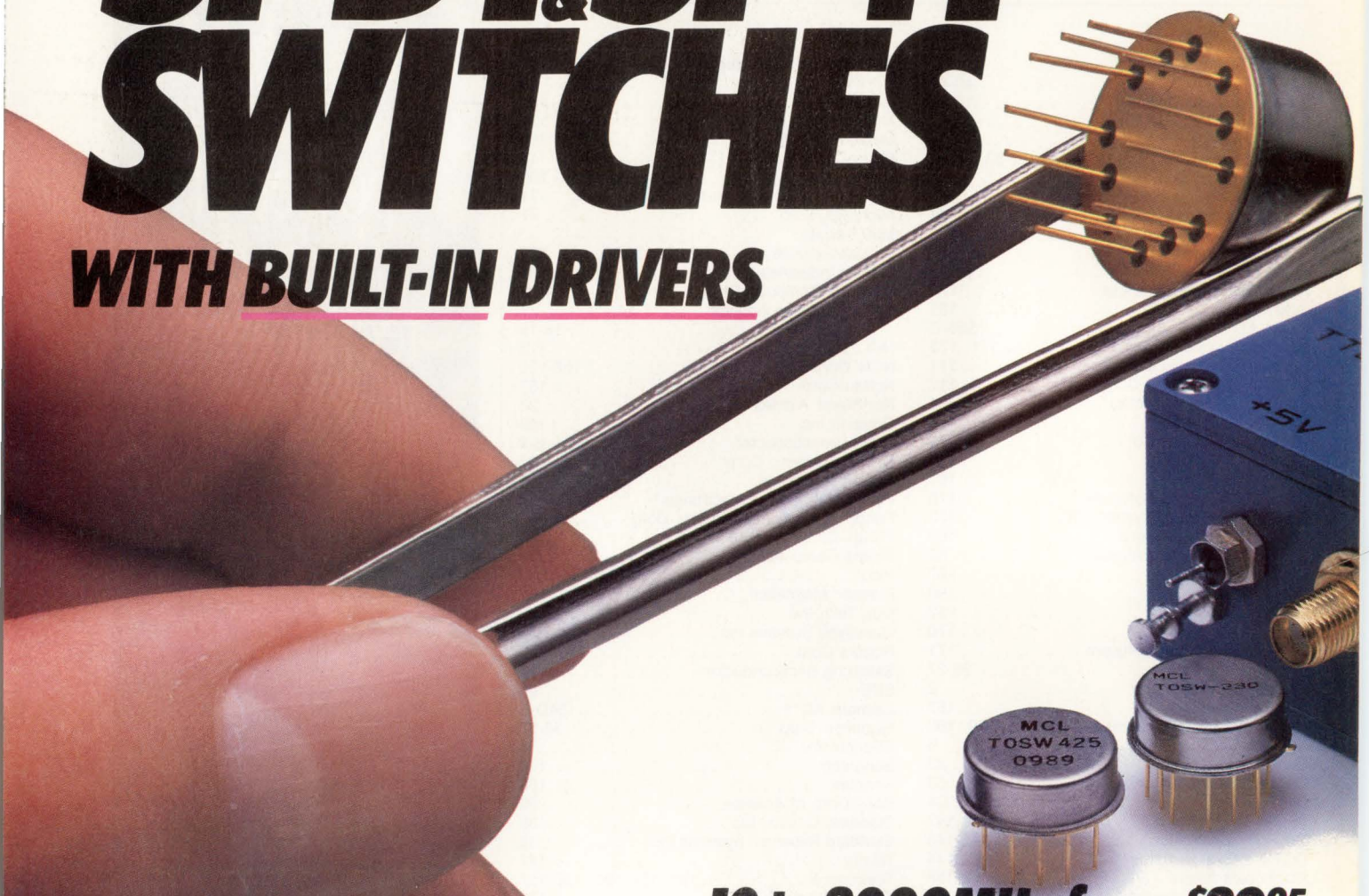

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Insert. Loss (dB)	typ.	max.	typ.	max.
10-100MHz	1.3	1.9	1.3	1.7
100-1500MHz	1.1	1.9	1.1	1.7
1500-3000MHz	1.8	2.7	1.8	2.5
Isolation(dB)	typ.	min.	typ.	min.
10-100MHz	60	40	60	40
100-1500MHz	40	28	40	30
1500-3000MHz	35	22	35	22
1dB Compression(dBm)	typ.	min.	typ.	min.
10-100MHz	17	6	17	6
100-1500MHz	27	19	27	19
1500-3000MHz	30	28	30	28
VSWR(ON)	typ.	max.	typ.	max.
	1.3	1.6	1.3	1.6
Switching Time (μsec) (from 50% TTL to 90% RF)	typ. 2.0	max. 4.0	typ. 2.0	max. 4.0
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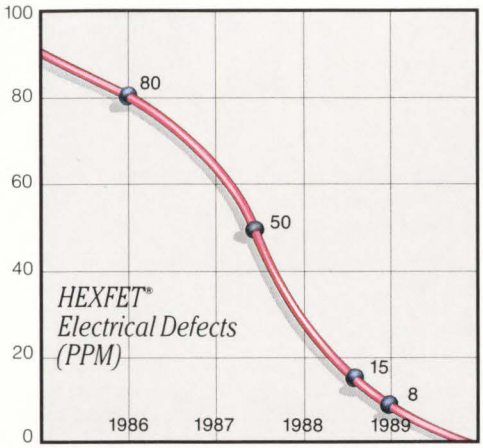

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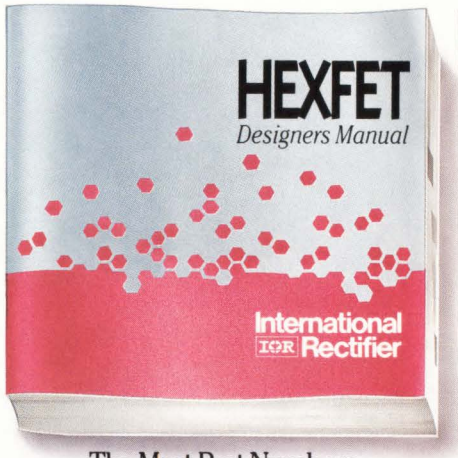

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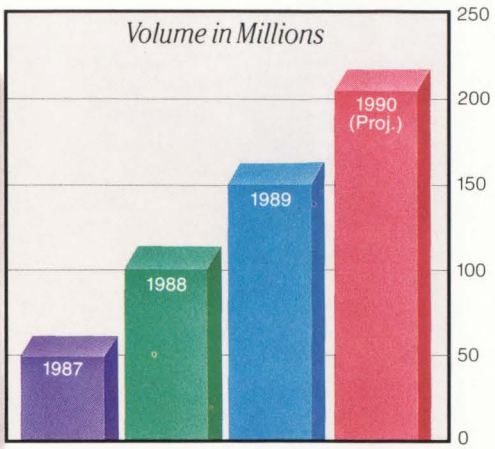

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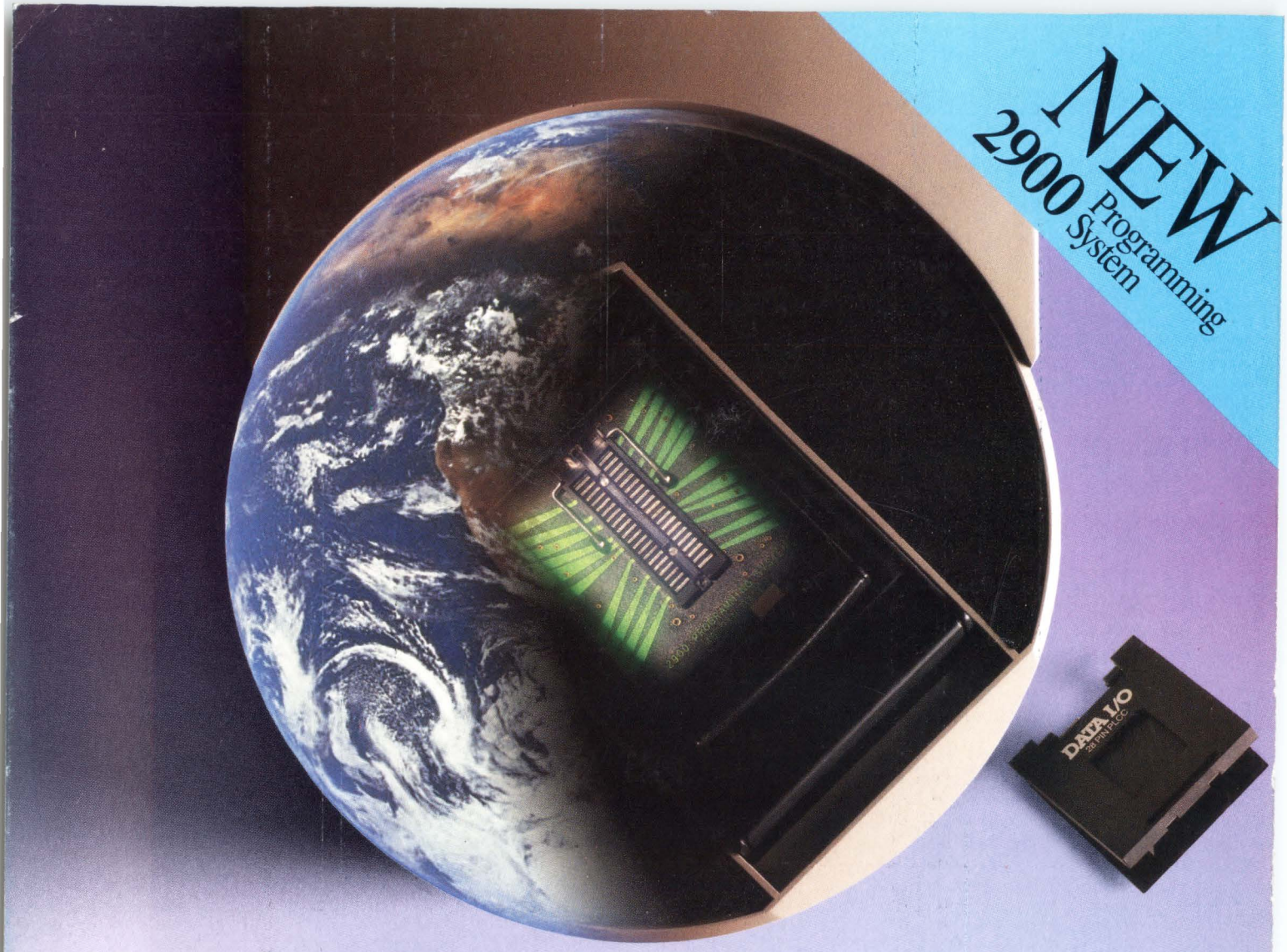

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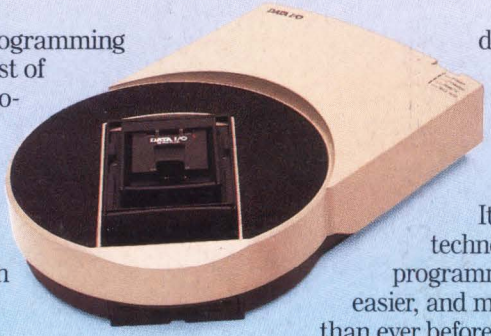

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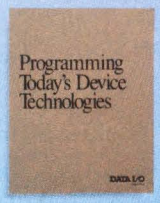

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