

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

## Processors let PCs construct realistic 3-D graphics



Zilog's universal serial communication controller, the USC (Z16C30"), provides higher throughput than any general purpose SCC. And it does it while reducing the CPU workload $60 \%$.

## Superintegration ${ }^{\prime \prime \prime}$ and the Communications Market.

Developed as an answer to the demand for more integration than ASICs could provide, Zilog's Superintegration ${ }^{\text {a }}$. technology bas resulted in a rapidly growiog also known as cation specific standard products (ASSPs), Working CPU cell-based integrated circuits, or have been combined and and Peripherals cores and cellons, yet they use the same enhanced for specific applications, yen sets you're already proven architectures with.
working wither
working with.
market needed SCCs with more speed. But market need taking performance away from that meant akde-off that was not acceptable. the CPU. A trade-Of iba of Superintegration Tbe es ation that provides enhanced SCCS, is a sound reliability. Consider performance and reliability. Consider for even the far-reacbing bated systems to be developed. more highly integrat this. Nobody bas a more complete

And consider this. Nobody has a meneric cores, system or I/O boltlibrary of proven, generic better qualified to develop ons than Zilog. Nobody

## More speed.

The USC is four times faster than any general purpose SCC. You get guaranteed data rates of $10 \mathrm{Mbits} / \mathrm{sec}$. But speed is not the only USC advantage.
More CPU power.
The USC requires less attention from the system CPU. That means more power for the system. The USC's lower overhead is due to easy initialization, auto-sequencing word transfers from deep FIFOs, fly-by DMA control, and reduced latency from an efficient, chained interrupt structure. More flexibility.

You've got two completely independent channels, as well as multi-protocol capability. Because the USC has two BRGs per channel you can transmit and receive at two different bit rates. And the USC's universal bus interface means you can cut the cost of GLU logic and expensive board real estate. More performance.

CMOS and Superintegration ${ }^{\text {tw }}$ bring more CPU power and higher data throughput. The USC carries a $12.5 \mathrm{MByte} / \mathrm{sec}$ bus bandwidth punch. Straight DMA connect and 32-byte FIFOs make the USC's systems simple, elegant and fast. Very fast. More reliability.

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[^0]
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SPECIFICATIONS

Pin Model Connector Version FREQ. RANGE INSERT. LOSS (db) dc-200MHz $200-1000 \mathrm{MHz}$ $1-4.6 \mathrm{GHz}$ ISOLATION (dB) $\mathrm{dc}-200 \mathrm{MHz}$ $200-1000 \mathrm{MHz}$ $1-4.6 \mathrm{GHz}$ VSWR (typ) ON OFF
SW. SPEED (nsec) rise or fall time MAX RF INPUT (bBm)
up to 500 MHz above 500 MHz CONTROL VOLT OPER/STOR TEMP PRICE (10-24)

KSW-2-46 ZFSW-2-46 dc-4.6 GHz typ max $0.9 \quad 1$ $1.0 \quad 1.3$ $\begin{array}{ll}1.3 & 1.7 \\ \text { yp } & \text { min }\end{array}$ $\begin{array}{ll}\text { typ } & \text { min } \\ 60 & 50\end{array}$ $30 \quad 40$
30 2(typ)
 +17
+27

8 V on, OV off $-55^{\circ}$ to $+125^{\circ} \mathrm{C}$

KSWA-2-46 ZFSWA-2-46 $\mathrm{dc}-4.6 \mathrm{GHz}$
typ max


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| :--- | :--- |
| $\mathbf{\$ 6 9 . 9 5}$ | $\$ 79.95$ |



Un the cover: With any one of three recently introduced processors, you can give your PC's graphics an added dimension. See pg 96 .

This cover art was produced by Diane Molina and Ben Deiman of Bendi Photographic Design on equipment from Austin Business Computers Inc. The image was created on an IBM PC/ATcompatible computer containing a 34010-based Truevision ATVista videographics card. The image started with $35-\mathrm{mm}$ color slides of the ATVista card and the T134020 graphics processor. It was then digitized with a Howtek slide scanner. Extrusions of the chips were made to look like buildings with TOPAS software from AT\&T Graphics Software Labs. The designer used Truevision Vista TIPS to create the textures. This photograph was provided courtesy Texas Instruments.

## SPECIAL REPORT

## Processors for 3-D graphics

Because of their enormous appetite for floating-point operations, 3-D graphics displays were previously limited to high-end workstations. With some powerful new processors, however, you can now bring workstation-quality 3-D graphics to such applications as PC add-in boards and embedded-graphics systems.-Margery S Conner, Regional Editor

## DESIGN FEATURES

## Electro/89

For three days in April, New York City will offer the electronicsengineering community much of interest in the form of Electro/89eastern US's largest design-electronics trade show and conven-tion.-Richard A Quinnell, Regional Editor
Electro/89 Products 127

## Designer's guide to dynamic RAMs-Part 1

Although designers often prefer dynamic RAMs (DRAMs) to their static counterparts, they sometimes shy away from using DRAMs because of the devices' added complexity. This article, part 1 of a 4-part DRAM series, sheds light on some of the complex issues surrounding DRAMs and describes the different DRAM architectures. The succeeding articles will cover memory-system architectures, DRAM controllers, and DRAM-board design. -Steve Gumm and Carl T Dreher, Texas Instruments

## Antialiasing filters reduce errors in A/D converters

The need for effective antialiasing filters closely matches the growing number of applications for A/D converters. These filters reduce converter errors by limiting the input signal bandwidth. To correctly specify the filter, you need to consider the appropriate frequency band and the filter's characteristics.-Robert W Steer Jr, Frequency Devices Inc

Continued on page 7

[^1]
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## REDEFINED

## THE WESTCOR STAKPAK ${ }^{\text {TM }}$. NEW GENERATION 250 TO 1200 WATT SINGLE OR MULTIPLE OUTPUT OFFLINE SWITCHER. 3.2 X 5.5 X 11.4 INCH CASE. FAN-COOLED.

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The StakPak's 8 module output section can be factory configured in virtually an infinite number of voltage, current and power combinations. Special models providing between 250 to 1200 watts and outputs from 2 to 95 VDC are available.

Other features include outstanding electrical performance; UL, CSA, VDE safety agency approval (in process); variable speed fan option for low ambient noise enviroments and 3 phase or DC input options. Indeed, with unprecedented power density, versatility and new features, the StakPak redefines power packaging. Please contact Westcor for a data sheet, pricing and additional information.


STANDARD 1200 WATT STAKPAK MODELS (110/220 VAC input)
Model Output Voltage (VDC) and Maximum Current (amperes) per Channel

Single Output
SP1-1801 2 © 240
SP1-1802 5 © 240
SP1-1803 12 100
$\begin{array}{ll}\text { SP1-1803 } & 12 \text { @ 100 } \\ \text { SP1-1804 } & 15 \text { @ } 80\end{array}$
or multiple output. Lower powe
StakPak models are available.

| Dual Output |  |  |
| :--- | :---: | :---: |
| SP2-1801 | 2@120 | 5 © 120 |
| SP2-1802 | 5 @ 120 | 5 @ 120 |
| SP2-1803 | 5 @ 120 | 12 @ 66 |
| SP2-1804 | 12 @ 66 | 12 @ 66 |
| SP2-1805 | 15 @ 53 | 15 @ 53 |


| Triple Output |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| SP3-1801 | 5 @ 180 | 12 @ 16 | 12 (4) 16 |  |  |
| SP3-1802 | 5 (13) 150 | 12 @ 33 | 12 (3) 16 |  |  |
| SP3-1803 | 5 (11)180 | 15 (1) 13 | 15 (13 13 |  |  |
| SP3-1804 | 5 (1) 150 | 15 @ 26 | 15 (3) 13 |  |  |
| Quad Output |  |  |  |  |  |
| SP4-1801 | 5 @150 | 12 @ 16 | 12 @ 16 | 5 (4)30 |  |
| SP4-1802 | 5 (1) 150 | 15 @ 13 | 15 (4) 13 | 5 (430 |  |
| SP4-1803 | 5 (10) 150 | 12 @ 16 | 12 (a) 16 | 24@8 |  |
| SP4-1804 | 5 (al 150 | 15 (a) 13 | 15 (3) 13 | 24@8 |  |
| Five Output |  |  |  |  |  |
| SP5-1801 | 5 (13) 120 | 12 @ 16 | 12 @ 16 | 5 (14)30 | 24@ 8 |
| SP5-1802 | 5 (1)120 | 15 @ 13 | 15 © 13 | 5 (1)30 | 24 (1) 8 |

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## TECHNOLOGY UPDATE

## Logic synthesis prepares for VHDL

Logic synthesis tools are the latest in a long line of CAE tools that are destined to shrink the product development cycle for ICs and ultimately convert gate-level designers to systems engi-neers.-Michael C Markowitz, Associate Editor


#### Abstract

RISC boards target 69 real-time applications Several manufacturers of CPU boards for real-time applications now offer powerful models based on RISC (reduced-instruction-set computer) $\mu$ Ps. You'll have to make the usual price/performance judgment before choosing a RISC-based board for a real-time appli-cation.-Maury Wright, Regional Editor


## PRODUCT UPDATE

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## Engineering Environment."



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# NEWS BREAKS 

EDITED BY JOANNE DE OLIVEIRA

## DEVFLOPMENT TOOL SIMPLIFIES CREATION OF USER INTERFACHS

The Microware Systems Corp (Des Moines, IA, (515) 224-1929) Rave (Real-time Audio/Video Environment) software-development tool simplifies the design of human interfaces for real-time applications such as process-control systems. The development tool, an extension to the OS-9 real-time operating system, allows you to combine audio and video signals, computer-generated graphics, and customizable menus to create a user interface. Rave consists of three software packages. The File Manager ( $\$ 300$ ) and the Graphics Support Library ( $\$ 175$ ) handle run-time chores and include drivers that interact with system hardware. You use the Presentation Editor (\$995) to create a user interface. All of the products will be available in May.-Maury Wright

## INTERFACE UNIT LINKS SCSI AND IFET-488 BUSTS

If your computer or workstation provides a SCSI port, you may have thought that only peripherals such as disk and tape drives could take advantage of it. Now, however, you can use a SCSI port to control external data-acquisition systems, measuring instruments, and other devices that operate on the IEEE-488 bus. The SCSI488 interface unit from IOtech Inc (Cleveland, OH, (216) 439-4091) lets a SCSI port control as many as 14 IEEE- 488 devices. Keep in mind that many computers and workstations provide only SCSI and RS-232C ports for communication with peripheral devices.

Because the interface is bidirectional, you can also use one IEEE-488 port to control as many as seven SCSI-based devices. Although the device's internal microprocessor controls the flow of information, it doesn't interfere with block-transfer operations, which can reach a speed of 800 k bytes $/ \mathrm{sec}$. You can buy the SCSI488 for $\$ 795$; it's available from stock.-Jon Titus

## PROTOTYPING BOARD KITS INCLUDE A RISC-IIKE 32-BIT $\boldsymbol{\mu} \mathbf{P}$

Intel Corp (Dept 9PO1, Santa Clara, CA, (800) 548-4725) now offers two kits that provide designers with a low-cost way to evaluate or prototype products based on the $20-\mathrm{MHz}, 32$-bit, 80960 KB RISC-like processor from Intel. The kits include working CPU boards, schematics, programmable logic equations, and a software debug monitor. You can choose from kits with slightly different 80960KB-based boards. The EVQT960F20 kit costs $\$ 1960$ and includes 128 k bytes of zero-wait-state static RAM and 128 k bytes of flash EPROM, which are installed on the CPU board. The board included in the $\$ 960$ EVQT960E20 kit hosts 128 k bytes of 2 -wait-state static RAM and sockets for 128k bytes of EPROM. The CPU boards include an onboard prototyping area and a connector that you can use to add external circuits. Shipments will start by midyear.-Maury Wright

## FAMILY OF 1- TO 10-MHz 12-BIT ADGs FFATURES LOW DISTORTION

Datel Inc (Mansfield, MA, (508) 339-3000) has announced a complete family of sampling A/D converters that operate at sampling rates of $1,2,5$, and 10 MHz . The ADS-112 ( $1-\mathrm{MHz}$ ), ADS-132 ( $2-\mathrm{MHz}$ ), ADS-131 ( $5-\mathrm{MHz}$ ), and ADS-130 ( $10-\mathrm{MHz}$ ) converters offer excellent dynamic performance. At the Nyquist frequency, the total harmonic distortion is -73 dB for the $1-\mathrm{MHz}$ and $2-\mathrm{MHz}$ devices and -69 dB for the $5-\mathrm{MHz}$ and $10-\mathrm{MHz}$ devices. The number of effective bits at the Nyquist frequency is 11.0 for the two lower-frequency devices and 10.6 for the two higher-frequency devices.

The ADCs, which also feature low noise and low nonlinearity specs, use a digitally corrected subranging architecture to achieve 12 -bit resolution. The design of these converters includes an internal sample/hold circuit, on-chip references, a clock, 3 -state outputs, and user-selectable output coding. Power dissipation ranges from 1.3W for the $1-\mathrm{MHz}$ part to 4.9 W for the $10-\mathrm{MHz}$ device. Pricing for commercial units is $\$ 259$ (24-pin ADS-112), \$346 (32-pin ADS-132), \$465 (40-pin ADS-131), and \$549 (40-pin ADS-130). Delivery, from stock to four weeks.-Dave Pryce

## FULL-HEIGHT 5¼-IN. WINCHESTER STORES 764M BYTES

The MK-358 Winchester disk drive from Toshiba (Irvine, CA, (714) 380-3000) offers an unformatted capacity of 764 M bytes. The 8 -platter drive dedicates one surface to servo control, but also relies on servo information embedded in each sector to ensure accurate tracking. The SCSI version of the drive costs $\$ 2645$ (1000); the ESDI version is $\$ 2495$ (1000). The SCSI version includes support for SCSI-2 features. Furthermore, the SCSI drive features an extensive command set that is stored on the drive and downloaded to RAM on power up. You can update the command set by downloading from a floppy disk. The company can easily implement custom command sets.-Maury Wright

## FVALUATION BOARDS AID IN RISC- $\mu$ P DFVFLOPMENT

Two boards from Step Engineering (Sunnyvale, CA, (408) 733-7837) can assist you in developing systems based on the AMD (Sunnyvale, CA) 29000 RISC (reduced-instruction-set computer) processor. The $\$ 3445$ Step PCEV (personal-computer evaluation vehicle) incorporates the $\mu$ P along with $512 k$ bytes of dual-ported video RAM, and plugs into the IBM PC/AT bus. The $\$ 1750$ Step STEB (stand-alone target evaluation board) includes a $29000 \mu \mathrm{P}, 512 \mathrm{k}$ bytes of RAM, two serial ports, and sockets for as much as 512 k bytes of ROM. The company ships the board with a ROM-based debugging monitor called MON29K. Step also offers a line of software-development products for the $29000 \mu \mathrm{P}$; the PCEV and STEB boards give you a ready target for code developed with those tools.-Steven H Leibson

## RRTARGRTABLE CROSS-MACROASSFMBLTR REDUCES TOOL PURCHASFS

If you're tired of buying yet another assembler every time you incorporate a new $\mu \mathrm{P}$ in one of your designs, or if you've been avoiding using a new $\mu \mathrm{P}$ because you don't have the software tools necessary to program it, the CASM retargetable crossassembler from AnyWare Engineering (Boulder, CO, (303) 442-0556) can solve your problem. The $\$ 195$ software package includes the cross-macroassembler, a linker, and a definition-file compiler. Definition files describe a particular $\mu$ P's instruction set and assembly-language syntax by using a proprietary, procedural programming language. The language eases the task of molding the assembler to complex, pipelined architectures, such as those in RISC processors, and to wide instruction words, such as those used in digital signal processors. CASM also includes definition files for the 8085, Z80, 8041, 8048, 8051, 8096, 6805, 68HCl1, 6502, and R2000 $\mu$ Ps and the NEC 7720 digital signal processor.-Steven $H$ Leibson


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## NEWS BREAKS: InTERNATIONAL

## DFCODFR FACILITATES 2-CHIP TELETEXT SYSTEMS

The MV1815 single-chip CMOS teletext decoder and one dynamic RAM are all that you need to put together a complete teletext system. Adding extra memory allows you to store as many as 254 teletext pages. Manufactured by Plessey Semiconductors (Swindon, UK, TLX 449637; in the US: Scotts Valley, CA, (408) 438-2900), the decoder includes all level 1 teletext functions and many level 2 functions. In addition, it has an on-chip data slicer, two separate page-acquisition circuits, and RGB colordisplay logic. Its character sets support 13 languages, including most European and Scandinavian languages. Engineering samples of the MV1815 are available now. Production parts, which are expected to sell for around $£ 5(100,000)$, will be available during the third quarter of 1989.-Peter Harold

## OPFRATING SYSTEM ADDS FAULT TOLFRANCE TO UNIX

Under an agreement between Integrated Micro Products (Consett, UK, TLX 537747; in the US: Santa Cruz, CA, (408) 429-1338) and Unisoft Corp (Emeryville, CA, (415) 420-6400), both companies will internationally market Integrated Micro Products' new FT-Unix fault-tolerant operating system. Because the operating system's fault tolerance is completely transparent, the system provides a standard Unix V. 3 software environment in which you can run unmodified application programs. Together with suitable hardware, FT-Unix supports the synchronization of two CPUs, mirroring of data on separate disks, redundant I/O and communications operations, and isolation and reintegration of hardware modules to support diagnostic and servicing operations. It also supports the use of uninterruptible power supplies. FT-Unix licenses will be less than twice the price of standard Unix V.3, and both companies will promote its adoption as an open standard.-Peter Harold

## SYSTEM TRANSLATES SPOKFN JAPANFSE TO SPOKFN FNGLISH

Matsushita has reportedly developed a translation system that can convert spoken Japanese sentences to the corresponding English sentences in approximately 5 to 10 sec . Unlike conventional voice-translation systems, which recognize only registered voices and require the speakers to divide sentences into clauses, this machine accepts natural speech from arbitrary speakers. Conventional machines are also fairly large; this system is the size of a typical workstation. It comprises a soundrecognition device, a general-purpose (Sun-3) workstation, and a sound-composition device.

The system performs its translation by converting spoken Japanese to a series of alphabetical phoneme symbols and transmitting them to the workstation, where a translating program analyzes and comprehends the sentence, translates it into English, and formulates the English verbalization. To do so, the system uses the translation program developed by Professor Masaru Tomita of Carnegie-Mellon University. The system can translate about 3000 short Japanese sentences (of two to four clauses) after 50 words have been entered in the dictionary. In testing the system, the firm has achieved an $80 \%$ recognition figure; the company plans to improve the accuracy of recognition to the $85 \%$ to $90 \%$ level. It also expects to offer high-speed performance and eventually to offer translation from English to Japanese. In addition, Matsushita reportedly aims to produce the world's first portable translation machine.-Joanne De Oliveira


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| LOW PASS Model $\quad$ *LP- | $\mathbf{1 0 . 7}$ | $\mathbf{2 1 . 4}$ | $\mathbf{3 0}$ | $\mathbf{5 0}$ | $\mathbf{7 0}$ | $\mathbf{1 0 0}$ | $\mathbf{1 5 0}$ | $\mathbf{2 0 0}$ | $\mathbf{3 0 0}$ | $\mathbf{4 5 0}$ | $\mathbf{5 5 0}$ | $\mathbf{6 0 0}$ | $\mathbf{7 5 0}$ | $\mathbf{8 5 0}$ | $\mathbf{1 0 0 0}$ |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: | ---: | ---: | ---: | ---: | ---: | ---: | ---: | ---: | ---: | ---: |
| Min. Pass Band (MHz) DC to | 10.7 | 22 | 32 | 48 | 60 | 98 | 140 | 190 | 270 | 400 | 520 | 580 | 700 | 780 | 900 |
| Max, 20dB Stop Frequency (MHz) | 19 | 32 | 47 | 70 | 90 | 147 | 210 | 290 | 410 | 580 | 750 | 840 | 1000 | 1100 | 1340 |

Max, 20dB Stop Frequency $(\mathrm{MHz})$
Prices (ea.): Qty. (1-9) $\mathrm{P} \$ 11.45, \mathrm{~B} \$ 32.95, \mathrm{~N} \$ 32.95, \mathrm{~S} \$ 34.95$

| HIGH PASS | Model | *HP- | 50 | 100 | 150 | 200 | 250 | 300 | 400 | 500 | 600 | 700 | 800 | 900 | 1000 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Pass Band (MHz) |  | start, max. end, min. | 41 | 90 | 133 | 185 | 225 | 290 | 395 | 500 | 600 | 700 | 780 | 910 | 1000 |
|  |  | 200 | 400 | 600 | 800 | 1200 | 1200 | 1600 | 1600 | 1600 | 1800 | 2000 | 2100 | 2200 |
| Min. 20dB St | quen |  | (MHz) | 26 | 55 | 95 | 116 | 150 | 190 | 290 | 365 | 460 | 520 | 570 | 660 | 720 |

Prices (ea.): Qty. (1-9) P \$14.95, B \$36.95, N \$39.95, S \$38.95

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- 75 ohms dB values, $3,6,10,15,20$ BNC only
- Price (1-9 qty.)

CAT (BNC) \$16.95 SAT (SMA) \$20.95
NAT (N) $\$ 23.95$
finding new ways
setting higher standards

## $\square$ Mini-Circuits

| *Freq. <br> (MHz) | Atten. Tol. (Typ.) | Atten. Change, (Typ.) over Freq. Range |  | VSWR (Max.) |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| DC-1500 MHz | $\pm 0.3$ | $\begin{gathered} \text { DC-1000 } \\ 0.6 \end{gathered}$ | $\begin{gathered} 1000-1500 \\ 0.8 \end{gathered}$ | $\begin{gathered} \mathrm{DC}-1000 \mathrm{MHz} \\ 1.3 \end{gathered}$ | $\left\lvert\, \begin{gathered} 1000-1500 \mathrm{MHz} \\ 1.5 \end{gathered}\right.$ |
| *DC-1000 MHz (all 75 ohm or 30 dB models) $\quad \mathrm{DC}-500 \mathrm{MHz}$ (all 40 dB models) |  |  |  |  |  |
| Model Availability |  |  |  |  |  |
| SAT (SMA) |  | AT (BNC) | NAT (N) |  |  |

## Precision 50 ohm terminations $\quad \$ 8.25$ (1-9)

DC to $2 \mathrm{GHz}, 0.25 \mathrm{~W}$ power rating, VSWR less than 1.1 BNC (model BTRM-50), TNC (consult factory) SMA (model STRM-50), N (model NTRM-50)

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| F |
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## FடபKE




6060B typical level accuracy vs. frequency at - 127 dBm .
Sample: 38 units. Solid line: worst case. Shaded: Typical (75\%).

Getting the performance you expect from your instruments can sometimes be a pain. But not when it comes to the Fluke 6060B RF signal generator. It delivers more performance than you thought you paid for, even at the extremes.

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The 1.05 GHz Fluke 6060B.

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| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ADS-112 | 1 MHz | 11.0 | -73 dB | 1.3 watts | 24 -pin DDIP | $\$ 259$ |
| ADS-132 | 2 MHz | 11.0 | -73 dB | 2.9 watts | 32 -pin TDIP | $\$ 346$ |
| ADS-131 | 5 MHz | 10.6 | -69 dB | 4.2 watts | 40 -pin TDIP | $\$ 549$ |
| ADS-130 | 10 MHz | 10.6 | -69 dB | 4.5 watts | 40 -pin TDIP | $\$ 775$ |

[^4]

# SIGNALS \& NOISE 

## Don't confuse the DFT with the FFT

I found Tom Springer's article "Sliding FFT computes frequency spectra in real time" (September 29, 1988, pg 161) to be interesting and informative. The concept of a recursive algorithm for calculating a discrete Fourier transform (DFT) became particularly important to our research group about a year ago, and I published an internal technical note whose results were identical (and whose title was nearly identical) to Tom Springer's. There were, however, a few inaccuracies in Tom's article that may tend to confuse any reader working through the algorithm derivations.

In particular, the term "FFT" was used throughout the article as a generic label for the discrete Fourier transform. Although the FFT label could be used to describe any fast Fourier transform (that is, any transform algorithm using fewer calculations than the canonical DFT implementation), it has generally been associated with the fast algorithm produced by eliminating redundant calculations through a binary factoring principle. The recursive algorithm described in the article is nowhere derived or related to the FFT, but is a direct derivation from the definition of the DFT.

The derivation in the colored box at the bottom of pg 164 begins with the definition of the DFT, and not the FFT, as it states. In addition, the derivation makes no distinction between the time-series function $x(n)$ and the frequency-domain function $\mathrm{X}(\mathrm{m})$. This problem is particularly confusing in the last and most important expression, where the frequency- and time-domain functions are mixed in the right-hand side of the equation.

Also, Fig 3 on pg 164 illustrates the $\mathrm{X}^{\mathrm{k}+1}(\mathrm{~m})$ frequency spectrum as being computed from an $\mathrm{N}+1$ point time series beginning at $k$ and end-
ing with $k+N$. The sequence should, of course, begin with $k+1$.

In addition to the caveats Tom mentioned, there are two others worth mentioning. First, because the computation is recursive, errors due to floating-point approximations will accumulate, the severity increasing with the size of the transform. Also, as with all DFT calculations, there is an implicitly applied windowing function. In the case of the sliding DFT, the windowing function is rectangular, with unity magnitude. The sliding DFT, as presented, will not accommodate other windowing functions. Randall Johnson,
Research and Technology
Development
De La Rue Printrak
Anaheim, CA

## Some thoughts on American education

Richard Simonelli and Jorgen Vinding raise valid points [about engineering education] in their letters (Signals \& Noise, EDN, September 29, 1988, pg 31). In his references to Hirsch and Ravitch and Finn, Jorgen Vinding shows more deep thought on the subject than the average engineer. The reference to Bloom will be appreciated by a large sample of educated Americans, who have read (at least in excerpts or interviews) about what the educational system has done to miseducate or de-educate students. Jorgen's recommendation that only 10 to $12 \%$ of a student's credits be in the humanities seems to me a bit low.

Ronald Khol makes the point (in Machine Design, October 20, 1988) that in Europe and Japan a degree from an American university is considered to be almost meaningless. He recommends that all students, regardless of their eventual fields of specialization, should have two


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.and more

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SIGNALS \& NOISE
years of intensive science and math. Such a requirement would be very good for journalism majors. It might reduce such ridiculous things as the wire-service science article that stated repeatedly that fluorocarbons release chlorine. Or the Time magazine article about Sprague, which stated that Sprague makes "capacitators," or the one about Gillette that claimed the company applies "silicon" (instead of silicone) to razor blades. Freshman chemistry these reporters obviously have not had.

Richard Simonelli is quite right that a formal, conventional liberal arts curriculum is not the only answer. In a large number of faculties, that is merely multiple exposure to socialist propaganda. My late wife had, in essence, a fine liberal education, though she had never had a college course. She read deeply of biography, history, and constitutional law, as well as news and business magazines, and she could discourse intelligently in these fields. Walter B Jones
Clear Lake City, TX

## PC-resident analog-I/O cards

This is a short note to compliment your publication for including the excellent article "PC-resident ana-log-I/O cards," by contributing editor Bill Travis, in the September 15, 1988, issue of EDN (pg 150).
In addition to being very well written, the article was the most complete examination of the present status of this technology that I've seen anywhere in the past couple of years.

Bill should, in my opinion, receive some special recognition for doing such an exceptional job on this complex and timely subject. Thanks to all, and keep up the good work.
James Bischof
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[^5]
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## Oops

The Special Report on power MOSFETs and IGBTs appearing in EDN's January 5, 1989, issue (pg 128) incorrectly listed Powertec Inc (Chatsworth, CA) as a supplier of those products. The company does not make MOSFETs or IGBTs; it manufactures power supplies only.

## Address update

"EDN's 15th Annual $\mu \mathrm{P} / \mu \mathrm{C}$ Chip Directory," which appeared in the October 27, 1988, issue (pg 164) included an incorrect address for Fujitsu Microelectronics Inc. The correct address, phone number, and FAX number are:
Fujitsu Microelectronics Inc
Advanced Products Div
50 Rio Robles, Bldg 3
San Jose, CA 95134
Phone (408) 922-9000
FAX 408-432-9070

## YOUR TURN

EDN's Signals and Noise column provides a forum for readers to express their opinions on issues raised in the magazine's articles or on any topic that affects the engineering industry. Send your letters to the Signals and Noise Editor, 275 Washington St, Newton, MA 02158. We welcome all comments, pro or con. All letters must be signed, but we will withhold your name upon request. We reserve the right to edit letters for space and clarity.

## 21st Century CMOS Technology, NOW

## 0.4 micron/6ns SCRAMs

## First of a New Generation of 3.3V Center-Pin Power and Ground Products.

Performance now offers two 6ns SCRAMs: P3C3148 1Kx 4 and P3C3147 4 Kx 1 . These SCRAMs are superfast Static CMOS Random Access Memories. Future superfast products, using center-pin power and ground with a 3.3 volt power supply, will include SCRAMs with 4 Kbit to 256 K bit densities and popular logic parts such as buffers, transceivers, latches, flip-flops, comparators, registers and gate arrays.
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As the 3.3 volt supply, low lead inductance product line emerges with 0.4 micron PACE III Technology, the uncompromised performance will overcome resistance to change and we will have a 'kinder \& gentler' speed.'

Tom Longo
Performance's PACE III Technology, whichfeatures 0.4 micron effective gate length, 0.75 micron line widths and 250 ps gate delay, offers a 40 percent speed improvement even with a 35 percent voltage reduction. Superfast 6ns SCRAM performance is available now with significantly lower power dissipation.

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## Tek's New ASIC Verification System.




# Big Tester Performance At A Benchtop Price. 

For a fraction of the price of large production testers, designers can now easily perform timing verification and margin analysis on their own ASICs, using a turnkey system with the critical timing of the million-dollar machines.

Tek's new LV 500 ASIC Verification System is a true designer's solution, integrated into a $50 \mathrm{MHz}, 256$-channel, 64 K deep benchtop system with a test head just 17 inches square. Using a simple menu structure and concepts familiar to the designer, the LV 500 combines elementary operation with astonishing performance, made possible by integrating all 256 bidirectional channels onto a single PCB. Results include:

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even for complex synchronous devices. The LV 500 lets you vary cycle length and timing for each of 16 clock generators


Familiar operation for example,
template-based test cycles replicate the everyday timing diagrams of your IC book.

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Thanks to its high degree of integration, the LV 500 rarely needs calibration. DUT fixturing is simplified. And capacitance loading is reduced to about 25 pF , further contributing to the system's accurate results. And it is compatible with virtually all logic simulators.

Don't wait for chips to fail in production -or worse, for products to fail in the field.
Start putting ASIC verification where it does the most good: in the hands of the designers themselves. For more information or a demonstration, contact your Tek sales representative. Or call 1-800-245-2036.

## "What if I told you there's a 15ns 64K SRAM available









"I'd say you've been reading too many supermarket tabloids."
"Seriously! You get high speed and quantity delivery, plus the ability to drastically cut your qual costs!"
"OK, I'll bite. Who's got 'em?"
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While others continue to talk speed, Toshiba now delivers 15 ns Static RAMs.
The exceptional access speed of the new 15 ns 64 K SRAM family is the result of a little technological wizardry and lots of $1.0 \mu \mathrm{CMOS}$ know-how. The bottom line is a 15 ns 64 K SRAM that dissipates less power and requires a smaller-sized die than more costly BiCMOS devices.

And, if you've been looking for ways to cut qualification costs on your 64 K SRAMs, look no further than Toshiba's 64 K SRAM family. By using an aluminum master slice common to all configurations within the 64 K family, the cost of qualifying individual parts is reduced by as much as $75 \%$ !

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| 16 Kx 4 | 64 K | 15 | 20 | 25 | 35 | Now |
| $16 \mathrm{Kx} 4(0 \mathrm{E})$ | 64 K | 15 | 20 | 25 | 35 | Now |
| 8 Kx 8 | 64 K | 15 | 20 | 25 |  | Now |
| 8 Kx 9 | 72 K | 15 | 20 | 25 |  | Now |
| 64 Kx 4 | 256 K | 20 | 25 | 35 |  | Early 89 |
| $64 \mathrm{Kx} 4(0 \mathrm{E})$ | 256 K | 20 | 25 | 35 |  | Early 89 |
| 32 Kx 8 | 256 K | 20 | 25 | 35 |  | Early 89 |
| 32 Kx 9 | 288 K | 20 | 25 | 35 |  | Early 89 |
| $16 \mathrm{~K} \times 12$ | 192 K module | 25 | 35 |  |  | Now |
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[^6]

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# New price performance level attained with algorithmic 12-bit + sign A/D converters. 

Micro Linear now has two 12 -bit + sign A/D algorithmic converters that incorporate autozeroing circuitry and self-calibration; the ML2230, and the ML2233.This approach has no trimming and less circuitry, resulting in a lower price and an A/D converter that maintains accuracy over time.

Priced at $\$ 15.95$ in 100 unit quantities, both the standard 24-pin DIP ML2230, and the 28-pin DIP ML2233, include an internal sample-and-hold and an easy to use microprocessor interface.


12-bit AID pricelperformance comparison including sample-and-hold cost.

Accuracy and Speed
Total conversion time is 31 microseconds, including the on-chip sample-and-hold acqui-
sition time. Both devices can digitize a -2.5 V .to +2.5 V sine wave at 12 kHz with a 73 db signal-to-noise ratio. Harmonic distortion is just $0.01 \%$.


The FFT plot of the ML2233. A two tone, -2.5 V to +2.5 V , low distortion sine wave input.
All errors of the sample-andhold are accounted for in the accuracy specification. Integral nonlinearity is $\pm 1 / 2 \mathrm{LSB}$ or $\pm 1$ LSB, there are no missing codes, and full scale and zero errors are less than $\pm 1$ LSB. This is over the temperature range, and with $\pm 5 \%$ tolerance on +5 V and -5 V power supplies.

## Versatility and Ease of Use

These 12-bit + sign A/D converters are designed for ease of use. The analog inputs can withstand 7 V beyond the supplies. The high impedance analog input is differential for noise immunity ạnd power supply rejection.


ML2230 block diagram
These devices support several interface techniques: interrupt, DMA or polling. The ML2230 is designed to interface to an 8-bit microprocessor bus by outputting the data result in two 8 -bit bytes. To interface to a 16 -bit bus, the ML2233 provides a 13 -bit data result. Both are designed to interface without additional components and are fully TTL and CMOS compatible. Bus timing parameters are compatible with the fastest microprocessors currently available.

## Call or Write for More Information

If your application calls for a 12 -bit A/D converter or if you would like more information on Micro Linear's complete range of linear devices, please call (408) 433-5200 ext. 900 or write:

Micro Linear, Dept.TB, 2092 Concourse Drive, San Jose, CA 95131.
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## Farewell.



It never once occurred to me in the last 20 years that I would someday write a farewell letter to you, the good and loyal readers of EDN. I never considered working for another publication because I always thought EDN was the best, even in earlier years, when it wasn't. Now, it truly is the best publication in the electronics industry. It has the most professional and the most knowledgeable editorial staff, serves the most exciting industry in the world, and has the most loyal readers of all.

But there comes a time when we must move on to new opportunities and challenges, which is what I'm doing. Though I feel bittersweet at the thought of leaving EDN, I'm pleased to become publisher of Test \& Measurement World-a magazine that serves the same exciting industry. I'm also pleased to continue my affiliation with Cahners Publishing. And making the transition that much easier is the fact that many of you are readers of Test \& Measurement World. I am most fortunate indeed.
Together we've faced many changes these past 20 years, the most significant being the microprocessor. That single development revolutionized not only every aspect of the electronics industry (and your job), but also every industry worldwide.

We positioned EDN to help you understand how to use and exploit the benefits of that and every other significant technical development. I believe that we've served you well-and you tell me I'm right in readership survey after readership survey.

EDN will continue to serve you well under the leadership of both Peter Coley, a good friend and supportive publisher, and my successor, Jon Titus, who is an outstanding editor.
I thank my entire editorial staff for their loyalty, support, and professionalism. And I thank you for all the same reasons. I wish for all of you, staff and reader alike, the sentiments of an old Navy saying, "May you have fair winds and a following sea."


Roy Forsberg
Vice President/Editorial Director

## Jesse H Neal

Editorial Achievement Awards 1987, 1981 (2), 1978 (2), 1977, 1976, 1975
American Society of
Business Press Editors Award 1988, 1983, 1981

## If you believe EPLDs are constrained by theirarchitecture, this should open your mind.

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When you combine the MAX architecture with a high speed, 0.8 micron CMOS process, you get high density devices with extraordinary performance.
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And see how easy it is to change your thinking about EPLDs.


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Whether it's a question of speed, bandwidth, power consumption or cost, our family of 8-bit A/D flash converters has the answer.

For example, if you need a monolithic high speed, ECL-compatible converter, there's our AD770 or AD9002.
The AD770 is our fastest ECL-compatible 8-bit converter, with a guaranteed sample rate of 200MSPS. And its 250 MHz full power bandwidth and SNR performance with high frequency input signals can't be beaten. The AD770 is available in commercial and extended temperature range versions.

The AD9002 has a guaranteed sample rate of 125 MSPS - yet its nominal power dissipation is a mere 750 mW - and it operates from a single -5.2 V power supply. The AD9002 is also available with MIL-STD-883 processing, making it ideal for a wide range of applications.

On the other hand, if it's a TTL-compatible 8-bit flash converter you need, there's our AD9012 or AD9048.
The AD9012 is the industry's fastest TTL-compatible converter, with a guaranteed sampling rate nearly twice that of its

## ECL COMPATIBLE



High Bandwidth,
ECL Compatible, 200MSPS

- 400 MHz Small-Signal Bandwidth
- 19pF Input Capacitance
- Bipolar or Unipolar Input
- $+5 \mathrm{~V} /-5.2 \mathrm{~V}$ Power Supplies

The AD770 200MSPS A/D Converter uses an advanced VLSI bipolar process and a proprietary design to achieve new levels of performance in sampling rates and signal bandwidths for flash converters. Full power bandwidth is 250 MHz .
The AD770 is ideal for high performance digital oscilloscope, radar, communications and electronic warfare systems. High input bandwidth permits undersampling of high frequency band-limited signals.
Multistage comparator design reduces the probability of errors due to metastable states or insufficient gain; decoding logic further reduces errors with a two-stage error-correcting architecture.
All inputs and outputs are ECL compatible, and analog inputs can be either bipolar or unipolar signals with up to 4 V range. High accuracy and minimum temperature drift are preserved with end point reference Force and Sense connections.
There are three grades available. JD and KD grades are specified over a 0 to $+70^{\circ} \mathrm{C}$ range; the SD grade is specified for temperatures from $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$. All standard grades are packaged in 40 -pin ceramic DIPs; contact the factory for other package options.


AD9002
Low Power,
ECL Compatible, 125MSPS

- 160 MHz Analog Input Bandwidth
- 17pF Input Capacitance
- 750mW Power Dissipation
- Single -5.2V Power Supply

Designs for radar, digital oscilloscopes, ATE systems, electronic warfare, communications/signal intelligence systems and a wide variety of other applications can be made easier with the AD9002 High Speed Monolithic A/D Converter.
An overflow bit indicating overrange signals can also be used to "stack" two AD9002 units to get 9-bit resolution of the digitized signal.
Input capacitance is typically 17 pF and only 22 pF maximum, simplifying the choice of a driving amplifier. Cooling requirements and power supply problems are also eased because of the low 750 mW dissipation of the AD9002.
Two grades are available; one has 0.5 LSB linearity, and the other has 0.75 LSB linearity. Both versions are offered for operation from $-25^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ packaged as 28 -pin DIPs or 28 -pin PLCCs. Military temperature range devices of $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ are available as ceramic DIP and LCC packages; they are compliant to MIL-STD-883 requirements.
nearest competitor. Plus the AD9012 offers excellent ac performance, low power operation and low input capacitance.
The AD9048 is an improved version of an industry-standard 8-bit TTL-compatible A/D converter, with the highest sampling rate, widest bandwidth, lowest input capacitance and lowest power. And the AD9048, as well as the AD9012, is available to MIL-STD-883.

There's no question about it - high performance characteristics are traits in our family of 8-bit A/D flash converters. So no matter what your requirement is for 8-bit analog-to-digital conversion, we have the solution.

If you want more information in a flash on our 8-bit flash converters, call your nearest Analog Devices sales office or our applications engineers. Answers for the AD770 are at (617) 935-5565. For the AD9002, AD9012 and AD9048, call (919) 668-9511.

# 8-Bit Flash Converters 

## TIL COMPATIBLE



AD9012
Low Power, Wide Bandwidth,
TTL Compatible, 75MSPS

- 160 MHz Input Bandwidth
- 16pF Typical Input Capacitance
- Power Dissipation<1W
- Minimum 46dB SNR

The AD9012 is a TTL compatible A/D converter fabricated in an advanced bipolar process which makes it possible to operate at typical conversion speeds up to 100MSPS.
For commercial and industrial applications, the AD9012 is an excellent choice for professional video, instrumentation, digital radio and PC-based video digitizing equipment.
In military applications, the requirement for mil-qualified devices can be met with MIL-STD-883 units in electronic countermeasures, missile guidance, radar, radar warning and other military systems equipment.
The AD9012 is available in two grades: one has 0.5LSB linearity, and the other has 0.75 LSB linearity. Both operate from $-25^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ and are packaged as 28 -pin DIPs or 28 -pin PLCCs. Military temperature range devices of $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ are available as ceramic DIP and LCC packages.


Low Power, Low Cost,
TTL Compatible, 35MSPS

- 15 MHz Typical Bandwidth
- Input Capacitance Typically 16pF
- 550mW Power Dissipation
- Industry-Standard Pinouts

As its name implies, the monolithic AD9048 Video A/D Converter is an ideal choice for real-time conversion of video signals. Its full power bandwidth is typically 15 MHz , with no missing codes, and is a guaranteed minimum of 10 MHz .
Low power dissipation of 550 mW typical makes the AD9048 adaptable and attractive for a broad range of applications. In addition to professional video systems and video imaging, it is an excellent choice for electro-optics, digital radio and electronic warfare systems, among others.
The AD9048 has industry-standard pinouts and is available over two temperature ranges, with two grades of linearity. Linearities of either 0.5 LSB or 0.75 LSB can be ordered for 0 to $+70^{\circ} \mathrm{C}$ commercial ranges, or $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ military temperatures. Commercial versions are in 28 -pin DIPs and PLCCs; military versions are in ceramic DIP and LCC packages. Both commercial units and MIL-STD-883-compliant devices are standard products.

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Ask about our Free Sample Evaluation Program. For a free power supply guide and to discuss your own low-power needs, contact Toko America, Headquarters and Midwest Branch (312) 297-0070; East Coast Branch (203) 748-6871; Southeast Branch (205) 830-0952; West Coast Branch (408) 432-8281.
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## TECHNOLOGY UPDATE

## Logic synthesis prepares for VHDL



Although logicsynthesis tools offer greater efficiency to system designers, the current generation still suffers from a lack of compatibility with other CAE packages.

## Michael C Markowitz,

 Associate EditorLogic synthesis tools are the latest in a long line of CAE tools that are destined to shrink the product development cycle for ICs and ultimately convert gate-level designers to systems engineers. These tools have the ability to increase your design productivity while minimizing the risks of introducing design faults. But despite the efficiency gains, danger still lurks: Logic-synthesis software is still new, and the CAE industry is undergoing a radical transformation-thanks to the Very-high-speed-integrated-circuit (VHSIC) Hardware Description Language (VHDL).
The increasing complexity of the current generation of PLD and IC designs has stretched the capabilities of the engineers who create them. The difficulty of effectively trading-off such considerations as performance and packaging while still trying to meet delivery deadlines prompted the development of logic-synthesis software. The software translates and optimizes a design far faster than you could manually.

One way you can utilize this time savings is to simulate and test the design more extensively. If you had more time you could run system simulations that would let you improve on the oft-quoted statistic that $50 \%$ of ASICs fail to perform in their target system. You
might also play "what if . . . " games to evaluate performance-area tradeoffs; most of the synthesis packages have options that let you limit parameters like gate count and critical-path speed.

There are two major obstacles to the widespread acceptance of logic synthesis. One hurdle is the confusion over what logic synthesis is and what it can do; the second is a lack of standardization.

At the most basic level, logic synthesis maps Boolean equations to a gatelevel representation of your design. A broader definition stretches the input medium to include high-level circuit descriptions, like register-transfer-level (RTL) descriptions and hardware-description language (HDL) implementations. Further, the broader definition of synthesis encompasses two separate op-erations-translation of the behavioral circuit description to a structural implementation and, subsequently, optimi-


You can specify a PLA with state equations, logically optimize it, and then implement it in compiled standard cells with the Genesil Logic Compiler.


## Logic synthesis

zation of the structure to eliminate redundancy and inefficiency. Optimization is where you can design for high speed, low real-estate utilization, or some combination of the two. Trading off these considerations is the part of logic synthesis where engineers can obtain their highest level of productivity enhancement today.

To help visualize the design process and where logic synthesis fits into it, refer to the " Y " chart model (Fig 1) adapted from the original suggested by Gajski and Kuhn (Ref 1). This model proposes three ways to represent a design. More complex designs can use all three representations at various times in their development. But you might design exclusively at the gate level for smaller integrated circuits or at the polygon level for discrete transistors.

The behavioral domain is the highest and most theoretical level at which you can represent a design. At this level, you are solely concerned with the function of the circuit from input to output. At the most abstract level, you can specify a design as a behavioral system. Refinement makes this specification more detailed as an algorithm; an RTL description; a set of Boolean equations; and, ultimately, as a set of differential equations. All of these representations define outputs as some function of the inputs and, possibly, time.

The structural domain specifies what elements you use to convert inputs into outputs and how you connect these elements to work toward their goal. Paralleling the refinement of the behavioral domain, the structural domain can be as abstract as a structural system. Providing more detail lets you define your circuit as a group of subsystems, which can include CPUs and memories. You could then refine your subsystems as modules, such


Fig 1-The Y chart is a three-part representation of a design that can help you understand the design process and how you can use CAE tools to achieve your design goals.
as ALUs and registers. The modules can be further specified as gates and flip-flops; the gates and flip-flops can then be specified as transistors.

Finally, the physical domain describes the actual geometric implementation of the circuit. You can, at the most general level, represent a design as a collection of physical partitions. By refining the description and providing more detail, you can describe the physical circuit as a cluster; a floor plan; a group of cells; and, most basically, as an assortment of polygons.

A series of concentric circles connect each of the levels of detail. The circles represent, at the most philosophical level, an architectural description of the design. Refining the design produces the algorithmic,
functional-block, logic, and circuit descriptions.

In the jargon of the industry, logic synthesis at its simplest is strictly the translation from one level of detail in the behavioral domain to the same level of detail in the structural domain. Broadening the view a little, some vendors of synthesis tools include optimization in their definition of logic synthesis. These routines eliminate redundancies and inefficiencies that the synthesis software creates. At the most extreme end, some vendors insist that true logic synthesis encompasses translation, optimization, and refinement. Thus-independent of what you put in-you ultimately finish logic synthesis with either a transistor- or gate-level representation of your circuit. As

## TECHNOLOGY UPDATE

## Logic synthesis

a result of the vendor-dependent definition of logic synthesis, it is critical that you query logic-synthesis vendors to discover their particular definition.

The other major obstacle to logic synthesis-the lack of standardiza-tion-is shared by almost all CAE packages. Engineers and their organizations are reluctant to commit to yet another tool and devote the resources necessary to integrate that tool into their operation when the input and output data formats are incompatible with the tools they are already using. The investment and risk of still another translator, not to mention the learning required to utilize a new tool, has restricted the incorporation of logic synthesis as it has worked against the widespread acceptence of CAE tools in general. But as discussed in the previous issue of EDN (Ref 2), VHDL is beginning to dismantle these standardization stumbling blocks.

With the emergence of VHDL as a standard for the documentation and design of integrated circuits and systems, CAE tools will be-


You can capture a hierarchical circuit using TTL logic from which the PLDS-MAX package synthesizes an EPLD programmimg file.
come more attractive to the legions of designers who have postponed jumping aboard the CAE bandwagon for fear of either being left with a dinosaur or committing to the wrong standard. Most logic syn-


The PLDesigner software partitions the circuit and chooses the most cost-effective solutions within the performance constraints that you set.
thesis vendors and, indeed, most CAE vendors are coming to the realization that VHDL is the biggest game in town and are making major efforts to enable their software to accept VHDL input and generate VHDL output.

Initially, VHDL will be primarily a documentation and transfer language, hence the necessity for front-end design tools that can create and output VHDL code from some other input format. The reluctance of designers to embrace new techniques over their well-worn, time-proven methods will impede VHDL's rate of acceptance. Additionally, if you are immersed in a design project, you have little time to spend learning a new way to de-sign-essentially by writing codeand if you are between designs and have more time, you might not have the motivation to learn a new design technique. Call it a Catch-22. But once the benefits become clearer and the reluctance to write code rather than draw or capture

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12,800 equivalent gates
CGA 40E12: 7,752 equivalent gates

CGA 1ME12: 4,584 equivalent gates and 1280 bits of RAM.
$\square$ Performance: Superior speed/ power performance- $<0.1 \mathrm{pJ} ; 300$ ps delay; $300 \mu \mathrm{~W}$ power dissipation (typical gate).
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## TECHNOLOGY UPDATE

## Logic synthesis

a design dissipates, VHDL will gather steam as a design language.

In the meantime, the decision to use logic-synthesis tools depends largely on your circumstances. If you design a large number of complex circuits, then the productivity enhancements offered by the current generation of logic-synthesis packages would probably outweigh the instability of the CAE marketplace and future enhancements to logic-synthesis tools. If you don't design circuits that could ultimately make their way into Department of Defense (DoD) systems, many of these logic-synthesis tools would probably serve your purposes quite well. On the other hand, if you only do a few designs, or are under DoD mandate to use VHDL either for
design or documentation, then you might want to wait for the VHDL dust to settle before jumping into logic synthesis.
If you decide that you must have logic-synthesis capability or just want to know what's available, you should know that some vendors target their logic-synthesis software to either PLDs or ASICs because of the different requirements of each technology. Some of the PLDspecific synthesis vendors have made a committment to VHDL; others are still waiting to see how the dust settles. Minc's PLDesigner will have a provision for VHDL input in the third quarter of this year.
Altera is targeting a fourthquarter introduction of VHDL capability for its PLDS-MAX soft-
ware. The company is planning to add some extensions that its software will accept to the VHDLlanguage inputs to give you greater flexibility in creating your design. PLDS-MAX will output your circuit in standard VHDL format without the extensions, so you can exchange data with other VHDL-compatible tools. OrCAD is developing a VHDL compiler for its OrCAD/ PLD that will let you program PLDs from a VHDL behavioral circuit description.

PLDesigner, PLDS-MAX, and OrCAD/PLD create JEDEC (Joint Electron Devices Engineering Committee) standard file outputs for programming PLDs. PLDSMAX generates Altera's ADF format netlist as well as a PLD pro-

| TABLE 1-LOGIC-SYNTHESIS PACKAGES |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| COMPANY | PRoduct | VHDL | PLDs/ASICs | capability | optimization | workstations | PRICE |
| ALGORITHMIC SYSTEMS | ASCYN LOGIC SYNTHESIZER | IN DEVELOPMENT | P, A | 1, 2, 3, 4 | LOCALIGLOBAL | PCIXT, PCIAT, VAX, APOLLO, MAC | \$3000 TO START |
| ALTERA | PLDS-MAX | Q4 '89 | P | 1, 2, 3, 4 | GLOBAL | PC/AT, PS/2 | \$4995 INCLUDING PROGRAMMING HARDWARE |
| DATA I/O | GATES | - | P, A | 1, 2, 3, 4 | LOCALGLOBAL | PC/XT, PC/AT, PS/2, 1386 , SUN-3 | \$4440 |
| MENTOR | PLDSYNTHESIS | Q3 '89 | P | 1, 2, 3, 4 | LOCAL/GLOBAL | APOLLO | \$14,900 |
| MINC | PLDESIGNER | Q3 '89 INPUT | P | 1, 2, 3, 4 | LOCAL/GLOBAL | PC/XT, PC/AT | \$4500 |
| NCR | DESIGN SYNTHESIS | H2 '89 | A | 1, 2, 3, 4 | LOCAL/GLOBAL | $\begin{aligned} & \text { APOLLO } \\ & \text { (MENTOR } \\ & \text { GRAPHICS) } \end{aligned}$ | \$51,500 INCLUDING NCR LIBRARIES |
| ORCAD | ORCAD/PLD | INPUT IN DEVELOPMENT | P | 1, 2, 3, 4 | GLOBAL | PC | \$495 |
| SEATTLE SILICON | FINESSE | IN DEVELOPMENT | A | 1, 2, 3 | GLOBAL | APOLLO (MENTOR GRAPHICS | \$59,000 WITH CHIPCRAFTER |
| SILC | SILCSYN | OUTPUT NOW INPUT SEPT ' 89 | A | 1, 2, 3, 4 | LOCALGLOBAL | $\begin{aligned} & \text { SUN, APOLLO, } \\ & \text { DEC } \end{aligned}$ | \$50,000 <br> TEST OPTION \$28,000 |
| SILICON COMPILER SYSTEMS | $\begin{aligned} & \text { LOGIC } \\ & \text { COMPILER } \end{aligned}$ | IN DEVELOPMENT | A | 1, 2, 3 | LOCAL | $\begin{aligned} & \text { SUN, APOLLO, } \\ & \text { DEC (MENTOR/ } \\ & \text { DAISY) } \end{aligned}$ | \$24,500 |
| SYNOPSYS | $\begin{aligned} & \text { DESIGN } \\ & \text { COMPILER } \\ & \hline \end{aligned}$ | IN DEVELOPMENT | P, A | 1, 2, 3, 4 | LOCAL/GLOBAL | SUN, APOLLO, DEC (MENTOR) | \$35,000 |
| TRIMETER | DESIGN CONSULTANT | JUNE '89 | A | 1, 2, 3, 4 | LOCALGLOBAL | SUN, APOLLO, DEC (MENTOR/ DAISY) | \$49,500 |
| VLSI TECH | $\begin{gathered} \text { LOGIC } \\ \text { SYNTHESIZER } \end{gathered}$ | INPUT Q3 '89 OUTPUT IN DEVELOPMENT | P, A | 1, 2, 3 | LOCAL/GLOBAL | SUN, APOLLO, DEC, HP, ELIXI, RIDGE | \$30,000 |
| XILINX | DS-23 | N/A | P | 1, 2, 3 | LOCALGLOBAL | PC/AT, SUN, APOLLO | $\begin{aligned} & \$ 1500 \\ & \$ 3000 \end{aligned}$ |
| NOTES: <br> 1=COMBINATORIAL LOGIC |  | 3=SYNCHRONOUS CIRCUITS 4=ASYNCHRONOUS CIRCUITS |  |  |  |  |  |



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## TECHNOLOGY UPDATE

## Logic synthesis

gramming file for use with its hardware and PLDs. The PLDesigner provides its output in several useful formats, although Minc currently has no immediate plans for providing VHDL output. Minc's output formats include EDIF (electronic design interchange format) standard netlists, and schematics that are compatible with Mentor Graphics, Daisy/Cadnetix, OrCAD, PCAD, Futurenet-Data I/O, Teradyne, and Intergraph CAE systems. As with other front-end tools, until PLDesigner provides its own facility for generating VHDL descriptions, you'll need to use an indirect approach to generate a VHDL description. An example of such an approach would be importing your schematics to a schematics package that does have VHDL generation capability.

PLD-specific tools can begin the logic-synthesis process with Boolean equations, truth tables, or state-machine descriptions. Additionally, the PLDesigner can utilize RTL descriptions as well as syn-chronous-waveform entry, a method that lets you enter as many as 64 input and output waveforms. A waveform compiler then builds state-machine equations; and, if the waveforms do not provide sufficient information, the software provides you with the location of the problem and suggests solutions. Finally, if your design is too large, the PLDesigner can automatically partition your design among multiple PLDs, which it selects from its own library of more than 2500 devices, based on constraints like cost, pin count, and which devices your company stocks.

Logic cell arrays (LCA) are a cross between PLDs and ASICs. Xilinx's DS-23 Automated Design Implementation Program is an adaptation of Exemplar Logic's synthesis tools optimized for LCAs. It accepts either schematics that


Logic synthesis tools have the capability to synthesize chips more complex then those they could generate even a year ago. This SCSI core is functionally equivalent to the NCR 53C80 SCSI chip but is fully synchronous. It has roughly 1000 gates, took six weeks to design rather than six months, and is 9\% smaller than the core of its asynchronous cousin.
you've created with your favorite schematic-capture tool or Boolean equations. The DS-23 requires another front-end tool to create the circuit description from which the Xilinx software synthesizes and optimizes an LCA-compatible circuit. Thus, the company is relying on the capabilities of other front-end tools for VHDL compatibility.

Other vendors of logic-synthesis tools target the ASIC market. Most of these vendors recognize the importance of VHDL to their customers and are making progress toward providing their tools with the capability to both accept and generate VHDL descriptions. Logic-synthesis tools that accept circuit descriptions in other HDLs have an easier conversion path to VHDL than others. These HDLs include Gateway Design Automation's Verilog; Praxis' Ella, which was developed by the British Royal Signals and Radar Establishment (RSRE), adopted by the British Standards Institution (BSI), and licensed to

Praxis; and other proprietary languages,
Silc Technologies SilcSyn ASIC Design System already provides VHDL output, and the company is committed to releasing a revision with VHDL-input support in September. The company wrote the original logic-synthesis software to accept their SilcSyn HDL and is modifying the tool for VHDL compatibility. As is common with all of the ASIC logic-synthesis tools, you can create your specification using either Boolean equations or truth tables.
SilcSyn has an optional $\$ 28,000$ test-synthesis package that incorporates partial scan test into the design to implement testable ASICs. The software synthesizes the partial scan function after the circuit translation process but before the optimization routine is run, so that the software minimizes the scan logic with the rest of the design. The cost of the increased testability is four I/O pins and about $10 \%$ addi-

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## Logic synthesis

tional real estate-a savings of between one-half and two-thirds that of full scan-path designs. After implementing the logic, the software creates Mentor's logfile-format test patterns.

NCR Microelectronics has integrated SilcSyn into their $\mathrm{KE}^{2}$ (Knowledge-based Engineering Environment) package. The company expects to offer both VHDL support and the test synthesis feature in the second half of this year. If NCR is your ASIC supplier, its Design Synthesis package maps your circuit description directly to NCR library elements. Silc Technologies has additional cell libraries from Toshiba, LSI Logic, Fujitsu, and Standard Microsystems, and has a proprietary library from GTE.

You can drive the Logic Consultant from Trimeter Technologies (which has reached an agreement to be acquired by Mentor Graphics) with Boolean equations, truth tables, schematics, or netlists. When Trimeter releases the Design Consultant in June, it will contain the Logic Consultant. The Logic Consultant will have the capability to utilize and generate VHDL descriptions as well as Verilog HDL descriptions. The software lets you exchange netlists and schematics with either Daisy or Mentor workstations or with other CAE toolsets utilizing EDIF. Another enhancement to the Design Consultant will be a graphic state-machine-diagram editor that lets you draw a state machine to use as the input to the logic-synthesis software.

Seattle Silicon and Silicon Compiler Systems have leveraged their experience in silicon compilers to present an approach that could ultimately fulfill the original promise of silicon compilation. That promise was to enable you to plug a highlevel circuit specification into a black box and receive a fully fabricated, tested, and ready-to-use piece of silicon.


The advantage to logic synthesis is that you can optimize a design for either high performance (top) or area efficiency (bottom). Synopsys' Design Compiler highlights the critical path, so you can visualize possible problem areas in the circuit.

Neither Seattle Silicon's Finesse nor Silicon Compiler Systems' Logic Compiler currently support VHDL. However, both companies are committed to supporting the langauge and are developing enhancements that will bring VHDL capabilities to their tools. Finesse offers the ability to incorporate scan as a test strategy at the description levelcurrently you can use Boolean equations, truth tables, and state-machine descriptions to drive both Finesse and the Logic Compiler. The ability of these silicon compilers to size drive transistors automatically according to loading is a feature that provides more flexibility, better matching between circuit stages, and more efficient realestate utilization than the typical standard-cell or gate-array alternatives.

Other vendors target their logicsynthesis tools to work with both PLDs and ASICs. Synopsys' Design Compiler and HDL Compiler
accept descriptions in many formats. In addition to Boolean equations and truth tables, you can use netlists in EDIF, LSI Logic's NDL, Mentor's MIF, Tegas format, or Cadence format as well as EDIF schematics or Verilog HDL to drive the Synopsys tools. The only HDL Synopsys currently supports is Verilog, but the company is committed to VHDL and plans to include VHDL support in a future release.

VLSI Technology's Logic Synthesizer accepts input from Boolean equations and a state-machine highlevel language. VLSI Technology is working to enable you to use truth tables, state diagrams, and PLA code files to drive its synthesis tools. The next release of the Logic Synthesizer will support the Ella HDL; the company's goal is to offer VHDL-input support in the synthesizer's third-quarter 1989 release. VLSI is planning VHDL output support, although it is unsure when that support will be available. The

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## Stanford Research Systems

## TECHNOLOGY UPDATE

## Logic synthesis

Logic Synthesizer is part of VLSI's multichip ASIC system-design package, which helps you partition your circuit according to size, power, and packaging requirements.

The Ascyn logic synthesizer, from Algorithmic Systems, has VHDL compatibility in development. The program supports Xilinx LCAs, gate arrays, and standard cells. Ascyn and Gates are the only two packages targeted for ASICs that run on the IBM PC/AT and compatibles, and Ascyn is the only package that runs on Apple's Macintosh family of personal computers.

Ikos Systems uses a simple logicsynthesis capability in its hard-ware-based Simulation System. Typically, if you find an error while you are simulating, you must exit the simulator, correct the circuit, recompile, re-enter the simulator, and resimulate. Because you must repeat this procedure every time you find a design error, simulation
is often the bottleneck in design. With the Simulation System, you can enter Boolean equations, or netlist corrections interactively within the simulator shell. The Simulation System can perform local optimization; but, because it is strictly a simulator, it does not back annotate your logic changes to the original netlist. The simulator creates a file that documents your changes so you can update your netlist or schematic after you've finished simulating.

There is little question that logic synthesis is a powerful addition to the repertoire of system-design engineers. It can save you from entering schematics or netlists on a gate-by-gate basis. Many tools let you design using techniques that you're familiar with, like Boolean equations, truth tables, and state diagrams. Although you may not be comfortable working at the behavioral level, that's where the technology seems to be ultimately headed. Logic-synthesis tools are leading the way.

Standing in the way, however, are all the classic arguments against CAE tools: the lack of compatibility among hardware, software, and user interface. The cavalry, VHDL, is about to ride over the hill. EDN

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## Article Interest Quotient <br> (Circle One)

High 518 Medium 519 Low 520

## For more information . . .

For more information on the logic-synthesis products discussed in this article, contact the following manufacturers directly, circle the appropriate numbers on the Information Retrieval Service card, or use EDN's Express Request service.

| Algorithmic Systems | Ikos Systems Inc | OrCAD Systems Corp | Synopsys Inc |
| :---: | :---: | :---: | :---: |
| 399 Pond St | 145 N Wolfe Rd | 1049 SW Baseline St | 1500 Salado Dr |
| Number C5 | Sunnyvale, CA 94086 | Suite 500 | Mountain View, CA 94043 |
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| (617) 849-0580 | Circle No 704 | (503) 640-9488 | Circle No 712 |
| Circle No 700 |  | Circle No 708 | Trimeter Technologies Inc |
|  | Mentor Graphics |  | 200 Hightower Blvd |
| Altera Corp | 8500 SW Creekside Pl | 3075 112th Ave NE | Suite 100 |
| 3525 Monroe St | Beaverton, OR 97005 | Bellevue, WA 98004 | Pittsburgh, PA 15205 |
| Santa Clara, CA 95052-8163 | Circle No 705 | (206) 828-4422 | Circle No 713 |
| (408) 984-2800 | Circle No 705 | Circle No 709 | Circle No 713 |
| Circle No 701 |  |  |  |
|  | Mine Inc 1575 York Rd | Silc Technologies Inc | VLSI Technology Inc 1109 McKay Dr |
| Exemplar Logic Inc | Colorado Springs, CO 80918 | 34 3rd Ave | San Jose, CA 95131 |
| 2550 Ninth St | (719) 590-1155 | Burlington, MA 01803 | (408) 434-3000 |
| Suite 102 Berkeley, CA 94710 (415) 849-0937 | Circle No 706 | Circle No 710 | Circle No 714 |
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|  | NCR Corp Microelectronics Div 2001 Danfield Ct | Silicon Compiler Systems | Xilinx Inc 2069 Hamilton A |
| FutureNet-Data I/O Corp | Fort Collins, CO 805 | 2045 Hamilton Ave | 2069 Hamilton Ave |
| 10525 Willows Rd NE | (303) 226-9530 | San Jose, CA 95125-6199 | (408) 559-7778 |
| Box 97046 | Circle No 70 | (408) 371-2900 | Circle No 715 |
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## /AVIX

## SMT Solutions Technical Information On Surface Mountable Voltage Suppressors.

Figure 1 • Energy Dissipation for Zener Diodes and Transguards
 Depletion Region
Transguard


## A Multilayer Approach to Transient Voltage Suppression

Electrical overstress, especially due to electrostatic discharge (ESD), has been a growing concern to designers and the trend toward surface mount technology (SMT) has placed severe size constraints on the components that provide this protection.
Low voltage transient suppressor applications have been dominated by specially designed zener diodes because of their clamping characteristics and smaller size. However, continuing advances in ceramic technology have made the AVX TransGuard possible-a high performance, low voltage surface mountable varistor that, unlike single plane devices, uses a multilayer structure. This structure offers significant improvement in electrical performance as well as in size and usability in SMT assemblies. (Table I)

## Clamping Characteristics

Multilayer construction and improved grain structure of TransGuards result in excellent transient clamping characteristics (in excess of 150 amps peak current) while maintaining very low leakage currents under DC operating conditions.


Table I. Comparison of Surface Mount Transient Suppressors

## Energy Dissipation

Varistors or semiconducting ceramics are in reality series/parallel combinations of Schottky diodes that support most energy dissipation in thin depletion regions at each Schottky barrier. Zener diodes have only a single thin depletion region at the surface, while varistors have many in series/parallel combination distributed throughout the whole ceramic volume (as seen in Figure 1). This results in superior energy dissipation per unit volume.

Please send me the AVX Technica paper " A Multilayer Approach to Transient Voltage Suppressors.'Please send me more information describing AVX MLC's.
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| 16 -BIT | $80 \mathrm{C} 86888,80 \mathrm{Cl186} / 188,80286,68000010,68008$, V2030 |
| 32 -BIT | $80386,68020(25 \mathrm{MHZ}$ ) |

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[^8]
# RISC boards target real-time applications 



> A RISC board can turbocharge your real-time system design, but it may also drain your budget.

Maury Wright, Regional Editor

Several manufacturers of CPU boards for real-time applications now offer powerful models based on RISC (reduced-in-struction-set computer) $\mu \mathrm{Ps}$. You'll have to make the usual price/ performance judgment before choosing a RISC-based board for a real-time application. But you also need to consider the relative performance merits of RISC technology and the effect that a RISC architecture will have on your softwaredevelopment tasks and the auxiliary hardware that surrounds the CPU. Furthermore, all of the available RISC processors are relatively new and expensive, and you currently have few choices of real-time operating systems and software-development tools for these processors.

The RISC boards available for realtime applications are primarily based on the VME Bus. RISC-board manufacturers claim that their products offer a way to build morepowerful real-time systems than you can build with CISC (complex-instruction-set computer) boards. For one thing, the board vendors suggest that you can use a single-processor RISC board in a real-time application that might previously have required a tightly coupled multiprocessor design. Furthermore, the manufacturers assert that the real-time

RISC offerings can also be used in multiprocessor configurations.

And finally, the board manufacturers spec their RISC boards' performance at 12 MIPS and higher, comparing that figure with CISC boards' performance of around 1 to 12 MIPS. Such a comparison isn't as straightforward as it may look, however: To implement a given task, you don't need to write as many instructions for a CISC as you do for a RISC.

## Architectures seek an AIT of 1

RISC proponents, in general, claim that the technology offers a greater potential for performance than can be achieved with CISC architectures. RISC processors employ a relatively simple instruction set implemented without microcode. On average, available RISC processors can execute one


The 3-board VME Bus module from Motorola, Model MVME188, hosts eight 88200 cache/MMU ICs and as many as four $25-\mathrm{MHz} 88100$ processors. One board hosts the 88000-family chips, one is the system controller, and one carries 16 M bytes of RAM.

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instruction per clock cycle-an AIT (average instruction time) of 1 . Sys-tem-dependent latencies, however, typically make it impossible to realize an AIT of 1 in a system. (For more information on RISC technology, see Ref 1).

When they compare RISC and CISC processors implemented at the same clock speed and in the same silicon technology, CISC advocates concede that CISC processors can't match the AIT performance of RISCs. But CISC proponents argue that a RISC processor must execute more instructions than a CISC processor must to accomplish the same task. The RISC side counters that compilers primarily use simple instructions and therefore closely match RISC-processor instruction sets.

In fact, a comparison of RISC and CISC performance is significant only in relation to a specific application. Despite all the industry chatter about RISC technology, it's not automatically your best choice. The right choice for your application will be based on your analysis of the available hardware and software products for both technologies, and not on marketing hype.

The RISC-vs-CISC debate will probably continue into the next decade. But one fact stands clear: The available RISC chips and boards are members of today's highestperformance class of 32 -bit $\mu \mathrm{Ps}$ and $\mu \mathrm{P}$-based boards (some CISC chips and boards are also members of that class). The available RISC boards are also members of the highestcost class-their prices range from $\$ 7000$ to more than $\$ 35,000$.

## RISC requires fast memory

To use a RISC $\mu \mathrm{P}$ or board for a real-time application and to exploit the performance potential that RISC technology offers, you must accept and work with two characteristics of RISC technology. First,


Burst-mode memory-read operations allow the 29000-based Ironics IV-9001 board to operate at 17 MIPS with a cost-effective dynamic-RAM array.
to develop software for RISC processors, you must employ high-level languages. Second, RISC processors require fast access to fairly large memory arrays.
The requirement to program in a high-level language derives from the nature of RISC architectures. Because of the instruction set and large register file, it's not feasible for you to write your own assemblylanguage code (as you could for CISC processors), even for small routines for which execution speed is critical.

Furthermore, RISC architectures enhance performance by implementing such features as delayed branch execution. By delaying the execution of branch instructions, a processor can avoid waiting for the next instruction to be loaded into the execution pipeline. Compilers take advantage of such architectural features by changing the sequence in which instructions execute.
Using a high-level language isn't always a drawback, as you might be tempted to think. Languages such as C and Ada have become in-
creasingly popular for any (RISC or CISC) 32 -bit real-time application. High-level languages simplify the software-development task and make it easier to manage the large amounts of code generated in 32 -bit real-time applications.

## Optimizers complicate debugging

High-level languages do complicate the debugging process, however. Today's RISC and CISC compilers can optionally generate code that's optimized for run-time efficiency. In optimizing the code, the compilers often shuffle the machinecode instructions, changing their sequence. Optimization is necessary to make any code run efficiently, whether on a RISC or a CISC processor, but it's more important for RISCs, because only optimized code will take full advantage of the unique architectural features of RISCs, such as delayed branch execution.

The source-code-level debugging packages available from most compiler vendors, however, operate only on unoptimized code. Therefore, you can't debug your code

## RISC boards for real time

when it's running at full speed (optimized) at the source-code level.
Unix-type programmers (programmers who create software for non-real-time applications) probably don't need to debug software after optimization. But in real-time applications, the code interacts directly with the real world via robots, instrumentation, motors, and other asynchronous I/O devices. If you used a source-level debugger on the unoptimized code, and then optimized the code, you might run into a problem. For example, a robot might perform actions in the wrong sequence because the compiler had shuffled the instructions. In such a situation, you may need to debug the actual optimized code.
You can debug optimized code for CISC processors at the assemblylanguage level. However, because of the architectural features of RISC processors (such as delayed branching and large register sets) and the level of optimization that RISC compilers perform, it's virtually impossible to debug assembly code for RISC processors. You simply can't correlate the assembly code with the source code. (For more information on RISC compilers, see Ref 2.)

## Source tools should improve

It's a good bet that vendors of compilers and real-time operating systems will soon offer improved debugging tools. For now, however, if you must fix software glitches in real-time RISC applications, you may have to resort to the trial-and-error method.
Memory architecture holds the other key to exploiting the performance potential that RISC chips offer. The clock speeds of available RISC $\mu$ Ps currently range from 20 to 25 MHz , but in the next couple of years you can expect to see RISC $\mu$ Ps with clock rates approaching 50 MHz . To attain an AIT ap-


A 1M-byte static-RAM array provides the SPARC-based Mizar MZ7170 with the deterministic response capability required in strict real-time applications.
proaching 1, a RISC $\mu \mathrm{P}$ needs to fetch a new instruction, and perhaps even new data, every clock cycle. Architectural features such as delayed branch execution serve no purpose unless the memory can supply instructions and data to the processor without latency.
A dynamic-RAM (DRAM) system can't accommodate a $20-\mathrm{MHz}$ RISC $\mu \mathrm{P}$ with the required mem-ory-access speed (at 1 instruction per clock cycle, that speed would be 50 nsec ). Even schemes-such as interleaved memory-that satisfy pipelined CISC architectures fall short of the every-cycle-access needs of RISC processors. Fast CISC $\mu$ Ps also need faster access than DRAMs can provide, but memory latency has more of an impact on RISC performance than on CISC performance.

## Cache latency varies

In general-purpose computer systems, designers implement staticRAM (SRAM) caches to provide the processors with fast memory access much of the time; the percentage of time is called the "hit rate." However, when cache misses (instances
when the required instruction or data is not present in the cache) occur, the processor suffers a latency period while a new line of data is added to the cache. The latency varies according to the $\mu \mathrm{P}$ and cache architecture, but it typically ranges from 5 to 20 clock cycles.

Real-time systems require what's termed a "deterministic" response to asynchronous real-world events. Typically, a system responds to an event by generating an interrupt to a $\mu \mathrm{P}$. The processor then invokes a routine to service the interrupt. Part of the system designer's task is to ensure that the processor can respond to and service such an interrupt in a certain maximum amount of time: the worst-case response time. Historically, designers of real-time systems have avoided cache-based architectures because of the latency caused by cache misses. The latency would raise the worst-case response time significantly.

Before choosing a RISC architecture for a real-time application, you must consider the RISC board's memory-system design. The available RISC processors each include

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architectural features that may fit one memory scheme better than another. Each of the available boards uses a specific memory implementation, so when you buy a board, you're choosing a memory system. The board's memory architecture will play a large part in determining your system's worst-case response time.

## Static RAM minimizes latency

For example, Mizar chose to employ static RAM for the entire RAM array on its SPARC-based MZ7170 board set. The 2-board VME Bus product includes 1M byte of static RAM and 4 M bytes of EPROM. A $20-\mathrm{MHz}$ version of the board costs $\$ 6995$, and a $25-\mathrm{MHz}$ version adds $\$ 500$. You can also add a $20-\mathrm{MHz}$ Texas Instruments 8847 FPU (floating-point unit) for $\$ 995$.

Mizar currently offers the Wind River Systems (Emeryville, CA) VxWorks real-time operating system and software-development tools for the MZ7170, and plans to have other real-time packages available late this summer. The MZ7170 has no memory-management unit (MMU). Jerry Fiddler, president of Wind River Systems, believes that real-time systems can't afford the latency that a MMU can add during address translation. In fact, when porting its operating system to a board that includes an MMU, Wind River bypasses the MMU.

## Software bypasses MMU

Harvey Goldman, vice president of marketing at Integrated Solutions, agrees with the no-MMU, nocache philosophy for real-time applications. According to Goldman, the company has ported its UniWorks real-time operating system to boards that have caches or MMUs, but has bypassed the cache or MMU features.

Integrated Solutions currently of-


The VME Bus-based RISC board from Tadpole Technology, Model TP880V, includes an 88100 processor and two 88200 CMMUs. The company makes a similar product, the TP880M, that's based on the Multibus II.
fers the Advantedge 2000 Series. These products include a singleboard computer based on a 16.67 MHz MIPS Computer Systems R2000 chip set. The board, which costs $\$ 10,000$, does not support a bus such as the VME Bus. It's truly suited for applications such as workstations. The company does plan to make the UniWorks real-time operating system available for the board during the first half of the year, however. You can also expect the firm to introduce a follow-up VME Bus-based product that's more suitable for real-time applications.
In general, real-time systems employ multitasking operating systems and application software. A CPU board that doesn't contain an MMU requires you to develop each
task of a set of software tasks for a single physical-address space. Therefore, the programmer must prevent different tasks from manipulating the same memory locations improperly. An MMU simplifies the programming tasks, but it may add latency in the form of ad-dress-translation time.

## Burst mode speeds memory read

The Ironics IV-9001 board employs the AMD 29000 RISC processor, and the 29000 includes an onchip MMU. The MMU performs translations in the instruction pipeline and eliminates latency concerns. Ironics also implemented a hybrid-cache-based memory architecture on the board. The $29000 \mu \mathrm{P}$ employs a Harvard architecture

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with separate operand and instruction buses. The chip also includes circuitry to improve the performance of DRAM arrays. The $\mu \mathrm{P}$ can fetch operands and instructions in burst mode without issuing an address for each word fetched.

On the IV-9001, Ironics employs the burst-mode fetch feature and an interleaved array of static-column DRAMs to feed both the instruction and the operand buses of the 29000 , each at speeds as high as 100 M bytes/sec. In fact, the DRAM array can supply instructions to the CPU at a rate of one instruction per cycle; memory latencies are caused only by memory-refresh operations and dual-port conflicts with operand accesses.

The board also includes a 16 k byte direct-mapped operand cache that minimizes accesses to the dynamic RAM for fetching operands. A cache miss to the operand cache causes a worst-case latency of seven cycles. Ed Schulman, Ironics' vice president of marketing, points out that because of the fast clock speed of the $29000 \mu \mathrm{P}$, the actual worstcase latency caused by the cache is acceptable for most applications.

## Daughter card hosts RAM

Ironics implemented the DRAM array on a daughter card for the VME Bus processor board; the company offers RAM cards with 2 M to 16 M bytes of memory. The IV-9001 costs $\$ 7995$, and a 2 M-byte RAM card adds $\$ 1995$. Ironics may also offer an SRAM daughter card in the future. The company offers the VRTX32 real-time kernel from Ready Systems (Palo Alto, CA) and the pSOS real-time kernel from Software Components Group (San Jose, CA) for the RISC board.

If you consider using a board based on the Motorola 88000 RISC processor, you may have to deal with an even more complex memory architecture. This RISC chip set in-


Based on the 16.67-MHz R2000 chip set from MIPS Computer Systems, the Integrated Solutions Advantedge 2000 single-board computer serves real-time and Unix applications.
cludes the 88100 CPU IC and the 88200 CMMU (cache and MMU) IC. The 88100 employs a Harvard architecture, and it's typically accompanied by one to four 88200 CMMUs for both instruction and operand buses. According to Motorola, the 88100 can be used without any 88200 CMMUs, but no vendors currently offer such a board-level product.

## Cache IC emulates static RAM

Motorola did, however, make some provisions in the CMMU IC for real-time applications. The 88200 includes a 4 -way, set-associative, 16 k -byte physical-address cache. You can program any or all of the four 4 k -byte segments in an 88200 to act as fast static RAM rather than as cache memory. Therefore, you can permanently load speed-critical sections of code into the memory segments that are set up as static RAM. The MMU portion of the IC performs address translations and adds no latency during accesses to the on-chip memory locations.

An 88100 CPU chip supports as many as eight 88200 CMMU ICs (four for instructions and four for operands). Therefore, the architecture potentially supports a total of 128 k bytes of fast memory for cache and SRAM use. Cache-read misses add a latency of seven cycles, and misses on writes add a 4 -cycle latency. Misses, however, cause the transfer of four consecutive words of data ( 16 bytes), not just the single word that caused the cache miss.
Motorola currently offers two 88000-based VME Bus products. The MVME181 includes an 88100 CPU and two 88200 CMMUs. A $20 \mathrm{M}-\mathrm{Hz}$ version of the board costs $\$ 8995$, and a $25-\mathrm{MHz}$ version costs $\$ 9995$. The board includes 8 M bytes of DRAM to feed the CMMUs.
Motorola also offers the MVME188 3-board set, which comes in three versions. You can specify the board set with one, two, or four 88100 processors, and each of the versions includes eight 88200 CMMUs. The versions cost $\$ 22,950$, $\$ 27,200$, and $\$ 33,500(100)$, respec-

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tively. One board of the set hosts the 88000 -family chips, a second board serves as a system controller, and the third board carries 16 M bytes of DRAM. A proprietary memory bus connects the boards.

## ICs support multiprocessing

The 88000 architecture inherently supports multiprocessing. In fact, the CMMU IC includes a buswatching feature, and the ICs maintain cache integrity in a multiprocessor configuration. Motorola of fers its VMEexec real-time operating system with the boards. The operating system supports multiprocessing. Software Components Group also plans to offer pSOS for the 88000 ; the product will probably be available early in the second quarter of this year.

Force Computer and Tadpole Technology also offer boards based
on the 88000 family. Tadpole's VME Bus-based TP880V costs $\$ 10,995$, and its Multibus-II-based TP880M costs $\$ 11,495$. The Tadpole boards feature similar architectures, and they each include an 88100 processor and two 88200 CMMUs. The boards come with 4 M bytes of DRAM and a 64 k -byte SRAM array that the 88100 can access without latency. In addition, pSOS will be available for both boards in the second quarter.

The Force offering, the CPU-81, also includes a single 88100 and two 88200 CMMUs (Fig 1). The board costs $\$ 8900$, has 4 M bytes of DRAM, and includes sockets for as much as 4 M bytes of ROM. Furthermore, Force offers a second board, the CPU-82, that mates to the CPU-81 via a 100 M -byte/sec bus (Fig 2). The CPU-82 costs $\$ 9900$ and carries an 88100 , three 88200 s,
and 12 M bytes of dynamic RAM.
Force labels the board set a "dyadic processor" and claims that the architecture eliminates all latency in computation-intensive applications. One of the three 88200 CMMUs on the CPU-82 is dedicated as an SRAM to store speed-critical sections of code. The CPU-81 and CPU- 82 will be available around the middle of the year. The company plans to offer pSOS, VRTX32, and OS-9 from Microware (Des Moines, IA) as real-time operating-system options.

## RISC prices are sky high

At present, cost may prove to be the ultimate key to how well a RISC board fits your application. To put it simply, the available RISC boards are very expensive. Memory prices are partly to blame for the high prices. But the newness and


Fig 1-A 4M-byte dynamic-RAM array and the 88000 chip set make up the CPU-81 board from Force Computers. The board also includes a 100M-bytelsec bus that can connect to a second processor and memory board (the CPU-82).

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sparse availability of the chips has also driven RISC-board prices up.

In fact, the price/performance ratio has kept some CPU-board vendors out of the RISC market. Heurikon Corp, for example, plans to stick with CISC-based products for the time being. Clarence Peckham, the firm's director of engineering, points out that Heurikon's HK32/V532 board, which is based on a $20-\mathrm{MHz}$ National Semiconductor $32532 \mu \mathrm{P}$, offers performance comparable to that of RISC-based boards. Furthermore, with 4M bytes of dynamic RAM, the HK32/ V532 costs about $\$ 5000$.
You can expect RISC chip prices to drop sharply in the next year, however. In particular, the price of SPARC processors should drop, because manufacturers are already producing the chips in volume for Sun workstations. Customers for

SPARC chips are also likely to benefit because of the large number of semiconductor companies that manufacture or plan to manufacture the chips. Bipolar Integrated Technology, Cypress Semiconductor, Fujitsu Microelectronics, LSI Logic, and Texas Instruments have all licensed the SPARC technology.

The MIPS Computer Systems R2000 and R3000 chip sets will also
be available from several vendors. Integrated Device Technology, LSI Logic, and Performance Semiconductor currently offer these chips. NEC Corp (Japan) and Siemens (West Germany) have recently licensed MIPS Computer Systems' RISC technology and plan to offer compatible processors in the future.
Thus far, Motorola plans to remain the only source of the 88000 .

## Consortium promotes standards

A number of companies have banded together to form the 88open Consortium (Wilsonville, OR), a nonprofit group that is leading the effort to set open hardware and software standards for 88000 products. For example, the Consortium's real-time and embeddedsystems committee is working to define a common BIOS for realtime systems. For information, contact John Barr, the committee chairman, at Motorola Computer X (a wholly owned subsidiary of Motorola). His phone number is (312) 576-8706.


Fig 2-The three 88200 CMMU ICs and the 88100 processor on the CPU-82 board from Force Computer can ensure deterministic processor response when the board is paired (in a dyad) with the CPU-81 board. The CPU-82 board also includes $12 M$ bytes of dynamic RAM.

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The company has taken great pains, however, to encourage all sections of the computer industry to use the 88000 family (see box, "Consortium promotes standards").

Your determination of whether to use RISC boards in your system application, as well as your choice of a particular RISC board, might well hinge on unquantifiable factors. Sure, you'll study the hardware and software available for RISC processors in making your decision, but you'll also be influenced by such factors as the industry momentum gathering behind a certain chip.

Ultimately, however, your decision between RISC and CISC boards will be reduced to two technical issues: You must decide whether you can tolerate programming in high-level languages and whether you can work with the complex memory architecture that RISC boards must have in order to be efficient. If you can, RISC boards are for you, if you can't, you should stick with CISC boards.

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## Article Interest Quotient

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## For more information

For more information on the RISC boards discussed in this article, contact the following manufacturers directly, circle the appropriate numbers on the Information Retrieval Service card, or use EDN's Express Request service.

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## $\mu \mathrm{P}$ packs workstation power and graphics ability in 1M-transistor chip

The 80860 microprocessor, with more than $1,000,000$ transistors, integrates a RISC core, a floatingpoint unit (FPU), a hardware shading unit, and an instruction and data cache. At 40 MHz , the chip achieves 80 M flops and can sustain 500,000 $4 \times 4$ matrix transformations/sec. In addition, the shading hardware can Gouraud-shade 50,000100 -pixel triangles/sec.
The chip comprises six basic units: the integer RISC core, the FPU, the graphics memory-management unit, the data and instruction caches, and the bus-control unit. The RISC core has a $32 \times 32$ bit integer register file. It decodes and executes load, store, integer, bit, and control-transfer instructions. It fetches floating-point as well as integer instructions and can operate in parallel with the FPU.

The FPU has a separate register file that you can configure as $8 \times 128,16 \times 64$, or $32 \times 32$ bits. Its separate adder and multiplier units both conform to IEEE STD 754. Both the adder and multiplier units can provide one result for every clock cycle. When pipelined, they operate at 2 results/clock cycle, yielding the 80 M flops rate. The graphics unit, which provides Gouraud shading and z -buffering as well as clipping capability, is discussed in more detail in the Special Report on pg 96.

The memory-management unit can translate addresses from linear logical space to linear physical space for both instructions and data, although this translation is optional. The processor stores translated address information in a table and caches the table in a 64 -entry, 4way associative memory. The page tables are compatible with those of


Combining a floating-point control unit and wide on-chip data and instruction caches, the 80860 can sustain an $80 M$-flops rate. The destination and source buses carry the operands used in pipelining the results of the FPU. $K_{i}$ and $K_{r}$ are constants; $T$ is a temporary register.
the 80386. These tables enable you to design a paged, virtual memory with user/supervisor protection, which is important in multitasking systems.

One-third of the chip's area is dedicated to data and instruction caches. The caches' aggregate bandwidth is $1 G$ byte/sec, a speed not possible with off-chip caching. The instruction cache is a 2 -way setassociative memory of 4 k bytes, divided into 32 -bit blocks. The 8 k byte data cache, which is a writeback cache, is also 2 -way set-associative and divided into 32 -bit blocks.

The bus-control unit works with conventional static-column dynamic

RAM. A pin indicates whether the next address takes place using the same page. The unit supports both pipelined and nonpipelined operation. Pipelining allows a new 64 -bit word to transfer every two cycles when the pipeline is full, even though the total number of cycles required for the transfer can number as many as six. Note that overall chip performance is often limited by the data-bus width. The 80860's 64 -bit external and 128 -bit internal buses lessen this possibility. \$750.-Margery Conner

Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051. Phone (408) 987-8080.

Circle No 734

## PRODUCT UPDATE

## Hardware modeling system creates simulation models of your ASICs

The LM-1000 hardware modeling system addresses some of the problems associated with doing systemlevel simulations of designs involving semicustom ICs. It lets you create a logic model of an ASIC when you have prototypes available. After you mount a device on a device adapter, the modeling method lets you create a functional software shell, in which you define the pinouts; a verification utility automatically checks software syntax and semantics.

For standard devices, the LM1000 hardware modeling system supports a library of over 600 logic models. Each includes a physical device mounted on a device adapter, shell software that defines I/O, and functional test vectors. Most of the models cost between $\$ 1000$ and $\$ 2000$.

Because the models utilize the actual physical device, they are by definition correct; as long as the shell software is correct, the model will perform as the actual devicebecause it is, essentially, the actual device. The shell also lets you control worst-case timing, including minimum, typical, and maximum delays. The pattern clock of the LM-1000 is continuously variable between 150 kHz to 25 MHz with a resolution of $1 \%$ and accuracy of $\pm 0.5 \%$. Timing resolution varies from 500 psec at 25 MHz to 50 nsec at 150 kHz ; accuracy is $\pm 3 \mathrm{nsec}$ or $\pm 1 \%$ of the pattern clock period, whichever is larger.
The LM-1000 currently supports, under OEM agreements, Verilog from Gateway, Hilo from GenRad, Validsim from Valid, the Vantage Spreadsheet from Vantage Analysis Systems, and Viewsim from Viewlogic, although the vendor


You can use the LM-1000 hardware modeling system to simulate the behavior of both standard and custom ICs in your system design-as long as silicon exists for all the pieces-without having to change either the simulator or the host you are already familiar with.
claims the LM-1000 is simulator independent and can easily adapt the hardware modeling system for any simulator. Because only a simulator function interface and some user utilities reside on the host computer, you can drive the LM-1000 from a variety of computers, including the Sun-3 and Sun-4; Apollo Series $3000,3500,4000$, and 4500 ; DEC VAXstation, MicroVAX and VAX; and IBM PC/386 and compatibles.
The base configuration for the hardware modeler allows for one 80 -pin device. Through expansion, you can build the pin capacity to 2560 total pins organized as eight slots by four lanes. This organization gives you as many as 3280 -pin devices, 16160 -pin devices, 8320 pin devices, or some combination
thereof. The LM-1000 supports pattern memory from 128 k patterns $\times 80$ pins to 2 M patterns $\times 320$ pins-you can expand memory with $128 \mathrm{k} \times 80$ - or $512 \mathrm{k} \times 80$-pin modules.
The LM-1000 starts at $\$ 50,000$ for the minimum unit and is available through Gateway Design Automation, GenRad, Valid Logic Systems, Vantage Analysis, or Viewlogic.

## -Michael C Markowitz

Logic Modeling Systems Inc, 1520 McCandless Dr, Milpitas, CA 95035. Phone (408) 954-5200.

Circle No 731

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| :---: | :---: | :---: | :---: |
| MODEL | CONFIGURATION | SPEED (ns) | PACKAGE |
| $\begin{aligned} & \text { CXX5863P } \\ & \text { CXX5863M } \\ & \text { CXX5863J } \end{aligned}$ | $\begin{aligned} & 8 K \times 8 \\ & 8 K \times 8 \\ & 8 K \times 8 \end{aligned}$ | $\begin{aligned} & 25 / 30 / 35 \\ & 25 / 30 / 35 \\ & 25 / 30 / 35 \end{aligned}$ | DIP 300 mil <br> SOP 450 mil <br> SOJ 300 mil |
| CXX5464AP <br> CXX5464AJ | $\begin{aligned} & 16 \mathrm{~K} \times 4 \\ & 16 \mathrm{~K} \times 4 \end{aligned}$ | $\begin{aligned} & 25 / 30 / 35 \\ & 25 / 30 / 35 \end{aligned}$ | $\begin{aligned} & \text { DIP } 300 \text { mil } \\ & \text { SOJ } 300 \text { mil } \end{aligned}$ |
| $\begin{aligned} & \text { CXX5465P* } \\ & \text { CXX5465J* } \end{aligned}$ | $\begin{aligned} & 16 \mathrm{~K} \times 4 \\ & 16 \mathrm{~K} \times 4 \end{aligned}$ | $\begin{aligned} & 25 / 30 / 35 \\ & 25 / 30 / 35 \end{aligned}$ | DIP 300 mil |
| CXX5164P CXX5164J | $\begin{aligned} & 64 K \times 1 \\ & 64 K \times 1 \end{aligned}$ | $\begin{aligned} & 25 / 30 / 35 \\ & 25 / 30 / 35 \end{aligned}$ | $\begin{aligned} & \text { DIP } 300 \text { mil } \\ & \text { SOJ } 300 \text { mil } \end{aligned}$ |
| $\begin{aligned} & \text { CXX5971P } \\ & \text { CXX5971J } \end{aligned}$ | $\begin{aligned} & 8 \mathrm{~K} \times 9 \\ & 8 \mathrm{~K} \times 9 \end{aligned}$ | $\begin{aligned} & 25 / 30 / 35 \\ & 25 / 30 / 35 \end{aligned}$ | $\begin{aligned} & \text { DIP } 300 \text { mil } \\ & \text { SOJ } 300 \text { mil } \end{aligned}$ |
| $\begin{aligned} & \text { CXX58255AP } \\ & \text { CXX58255AJ } \end{aligned}$ | $\begin{aligned} & 32 \mathrm{~K} \times 8 \\ & 32 \mathrm{~K} \times 8 \end{aligned}$ | $\begin{aligned} & 25 / 30 \\ & 25 / 30 \end{aligned}$ | DIP 300 mil <br> SOJ 300 mil |
| $\begin{aligned} & \text { CXX58258P } \\ & \text { CXX58258SP } \end{aligned}$ | $\begin{aligned} & 32 \mathrm{~K} \times 8 \\ & 32 \mathrm{~K} \times 8 \end{aligned}$ | $\begin{aligned} & 35 / 45 \\ & 35 / 45 \end{aligned}$ | DIP 600 mil DIP 300 mil |
| CXX54256P | $64 \mathrm{~K} \times 4$ | 35/45/55 | DIP 300 mil |
| CXX51256P | $256 \mathrm{~K} \times 1$ | 35/45/55 | DIP 300 mil |
| *0/E |  |  |  |

# PC-based precision counter offers high performance and low cost 

At $\$ 1495$, the GT200 is possibly the lowest-priced precision universal counter available. Its performance, however, is far from the lowest for IBM PC/XT-, PC/AT-based, or stand-alone counter/timers. This counter can measure frequencies with 10 -digit resolution/sec of gate time, and you can make timing measurements to $100-$ psec resolution without averaging. If this is more resolution than you need, you can trade it for speed measuring 7 digits of frequency resolution in 1 msec. For example, you can resolve a $10-\mathrm{kHz}$ signal to .001 Hz in 1 msec .

The instrument performs frequency, period, time-interval, de-lay-time-interval, ratio, totalize, gated-totalize, and pulse-width measurements; it can sustain operation at 2000 measurements/sec. This speed not only gives you the potential for higher system throughput, but also allows you to characterize dynamic signals.

For example, using this throughput you can quickly compute the drift rate and peak-to-peak jitter of a signal. Indeed, you can make multiple measurements and look at measurement statistics in the same amount of time you might need for single measurements on slower units. Because the counter's statistics software displays a running mean and standard deviation, and minimum and maximum count, you can see the sample results as they occur. This means that you don't need to wait for the instrument to finish taking all samples to see results.

The counter's two de-coupled input channels are specified for input frequencies of de to 75 MHz and accept signals from -5 to +5 V . To be sure you trigger on the correct


The IBM PC-based GT200 universal counter can simulate benchtop operation with its 12-digit display. You can also use the GT200 under program control for fully automated testing.
signal, you can use auxiliary inputs to arm the trigger. The auxiliary inputs also let you perform gated counting.

Input impedance and trigger threshold levels are programmable. You can select an input impedance of $50 \Omega$ or $1 \mathrm{k} \Omega$ in parallel with 30 pF . The trigger threshold is programmable from -4.375 to 5 V in 0.625 V steps. You can also use an automatic trigger mode to automatically set optimum input threshold levels.

If you need better stability than the standard 5 -ppm crystal oscillator provides within the range of 0 to $40^{\circ} \mathrm{C}$, you can select either the temperature-compensated or the
ovenized crystal oscillator. You can also use an external $10-\mathrm{MHz}$ reference.

The instrument's software supports two user interfaces. A virtual front panel simulates benchtop operation with mouse control of pulldown menus, including built-in statistics. You can also operate the counter under program control with simple English-like commands compatible with any programming lan-guage.-Doug Conner

Guide Technology Inc, 1940 Fallenleaf Lane, Los Altos, CA 94022. Phone (415) 961-9259.

Circle No 732

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CIRCLE NO 114

## Logic verifier handles ASICs and PLDs

The Personal Logic Design Verification System (PLDVS) allows you to perform functional tests and develop test programs for your ASICand PLD-based designs. The system comprises hardware and software that combine with your IBM PC/AT or compatible computer to form a test workstation.
The hardware portion of PLDVS includes plug-in cards for the computer and a generic socket adapter to receive the device under test. The adapter accepts devices with as many as 128 signal pins and is configurable to any device pinout and package style. You can program the system to simultaneously stimulate and read the signal pins, check for pin continuity, and monitor signal-drive current-all at rates as great as 200,000 vectors/ sec. The system double-latches signal readings using fixed TTL or CMOS logic thresholds.
The system has five power supplies available to operate the device under test. You can control each supply individually and set it anywhere between -12.5 V and +12.5 V .
The software portion allows you to create test programs using a Pas-cal-like language. You can enter test vectors in tabular form or generate them with algorithms. By using algorithms, you can quickly generate large numbers of test vectors, allowing you to exercise your design thoroughly. A 25 -line program, for example, generates 65,000 test vectors for a counter design.
The system software also includes a variety of utilities that allow you to design custom test-result displays. One utility, for example, automatically places pin readings at


This logic design verification system handles both ASICs and PLDs, allowing you to develop test programs and perform functional tests on your design.
a specified location on the computer's screen whenever the readings change.

When used with the company's Max + Plus logic design software, the design verification system accepts waveform descriptions for test vectors. The test results can also be displayed as waveforms. You can compare simulation results with actual device performance for the company's Max EPLDs.
The PLDVS costs $\$ 6595$, including software, interface, adapters, and documentation. The graphical interface design software costs an additional $\$ 3400$. Both require an IBM PC/AT or compatible computer. -Richard A Quinnell

Altera Corp, 3525 Monroe St, Santa Clara, CA 95051. Phone (408) 984-2800.

Circle No 730

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# Hitachi's HMCS400 Series of CMOS Microcontrollers The intelligent answer for small system control problems 

The raccoon has a remarkable ability to thrive in any type of environment. His sheer intelligence and ingenuity let him adapt to whatever circumstances he may find, and prosper with only minimal resources at hand.

Resourcefulness also characterizes Hitachi's HMCS400 series of CMOS microcontrollers. These sophisticated devices are optimized for real-time control tasks and include a great number of peripheral functions on-chip.

This new generation of 4-bit micros is a far cry from the old 4 - or 8 -bit designs you're used to. They execute efficient 10 -bit instructions in as little as $0.89 \mu \mathrm{~s}$, and include powerful on-chip peripherals such as large EPROMs, LCD and vacuum fluorescent drives, and multiple serial interfaces.

For example, our new HD4074408 has an 8 K one-time-programmable EPROM, a $512 \times 4$ bit RAM, 58 I/O lines, comparator inputs, PWM timer outputs and serial interfaces-all in a plastic package. Future devices will include A/D converters, phase lockedloop circuitry, DTMF generators, and much more.

Most importantly, Hitachi's ZTAT ${ }^{\text {TM }}$ technology gives you Zero Turn-Around Time. The on-board one-time user-programmable EPROM eliminates the need to wait three or four months for mask ROM devices. The very day you finish development, ZTAT gets you into production. And, you can implement software changes immediately, to stay one step ahead of everyone else.

Put all of Hitachi's HMCS400 series resources to work for you: Ceramic windowed devices for deve-
lopment, ZTAT devices for pilot and small-scale production, and mask ROM devices for large-scale production. And, a full complement of development support tools is available for use with IBM-PC*, DEC VAX*, and Hitachi systems.

Plus, when you consider all the on-chip integration, you also get the lowest-cost solution for your design. The packaging is one of the reasons why ZTAT only costs slightly more than mask ROM microcontrollers, and is a lot cheaper than ceramic reprogrammable devices.

Clearly, Hitachi's HMCS400 series is right for a broad range of today's small systems applications in automotive, consumer, handheld instrumentation, telecom, and industrial products.

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## SPECIAL REPORT



The shapes of things to come-realistic 3-D graphics images-will soon be showing up on personal-computer screens. One of three new processing products can give a PC add-in board or embedded graphics system the power to produce high-quality graphics. (Photo courtesy Intel Corp)

## Processors for

> Because of their enormous appetite for floating-point operations, 3-D graphics displays were previously limited to high-end workstations. With some powerful new processors, however, you can now bring workstation-quality 3-D graphics to such applications as PC add-in boards and embedded-graphics systems.

Margery S Conner, Regional Editor

Three-dimensional color graphics displays, which are capable of manipulating an image in real time and shading it realistically, require a processor to perform a great number of floating-point and integer calculations. Two recently introduced processors, the 80860 from Intel and the TMS34020 from Texas Instruments, are specifically tailored to produce 3-D graphics. A third chip, the G300 parallel processor from Inmos, makes it easier for you to design the company's fast Transputer (T800) into 3-D displays. With any of these three products, you can design workstation-quality graphics into a personal computer or other graphics application.

Beyond their ability to perform fast floating-point calculations, the three products have little in common. For example, unlike the 80860 and T800/G300, the 34020 requires a coprocessor (TI's 34082) to perform fast floating-point calculations. Both the 80860 and the T800/G300 combination have on-chip floating-point hardware, but the 80860 includes hard-wired shading algorithms; the T800/G300 does not. However, because 3-D graphics suits diverse applications, ranging from workstation displays to PC add-in boards to embedded military displays, there's no one correct design approach. The application determines the cost and size of the system you can build as well as which chip you'll choose. To decide which chip is best for your applica-
tion, you must first understand how graphics chips perform 3-D manipulations and shading.

In a 3-D color graphics display, the graphics application software stores graphical shapes in world coordinates, which are dimensionless Cartesian coordinates. The scale of a world-coordinate system depends on the application: 3-D applications can require thousands of units of resolution.

The graphics system processor must be able to rotate or tilt any graphical shape to conform to the viewing angle. These manipulations require the processor to perform a matrix transformation. To get an idea of the number of floating-point multiplications and additions the processor must perform, consider the following example. To move a point ( $\mathrm{x}, \mathrm{y}, \mathrm{z}$ ) to a new position ( x ', $y^{\prime}, z^{\prime}$ ), you must multiply it by a $4 \times 4$ transformation matrix:

$$
\begin{aligned}
& {\left[\begin{array}{lll}
x^{\prime} & y^{\prime} & z^{\prime} \\
w^{\prime}
\end{array}\right]=\left[\begin{array}{ll}
x y z w
\end{array}\right]^{*}\left[\begin{array}{c}
\text { abcd } \\
\text { efgh } \\
\text { ijkl } \\
\text { mnop }
\end{array}\right]} \\
& x^{\prime}=a x+e y+i z+m w \\
& y^{\prime}=b x+f y+j z+n w \\
& z^{\prime}=c x+g y+k z+o w .
\end{aligned}
$$



Fig 1-This rendering of a torus shows how a graphics-display system would draw the shape before applying a hidden-surface removal algorithm. At this stage, all the polygons that the application software uses to represent the shape are visible. (Photo courtesy Weitek Corp, Sunnyvale, CA)

To multiply the vector representing the pixel position by the transformation matrix, the processor must perform 28 floating-point operations: 16 multiplications and 12 additions. The $4 \times 4$ matrix transformation is basic to all 3-D manipulations, so it's a useful guideline for comparing different processors' floating-point capabilities. For example, a representative workstation, the Sun-4, transforms 150,000 vectors $/ \mathrm{sec}$.

The graphics application software doesn't store all of a graphical shape's pixels in memory; instead, it divides the shape into a series of polygons and stores only the vertices of the polygons. To transform a graphical shape, therefore, the system must transform the vertices of all the shape's polygons (Fig 1).

After the graphics system processor transforms all of the shape's polygons to the correct viewing angle, the processor performs a clipping test to ensure that the system will display only those pixels that fit into the viewing window. The viewing window can be any size you care to make it.

To display the graphical shapes created by the application program, the processor must convert, or transform, the world coordinates to screen coordinates. Screen coordinates are relatively small, and their size is determined by the physical display. The screencoordinate system for the IBM PC's VGA display, for example, is $640 \times 480$ pixels. The processor converts the coordinates by using a matrix transformation similar to those used for rotation and scaling. Up to this point, all the manipulations performed by the processor consist of floating-point operations.


Fig 2-When no shading algorithms are applied to this graphical rendering of a teapot, each polygon has only one color assigned to $i t$, so the teapot appears to have a nonsmooth surface.

The next step is for the system to move the graphical entities from 3-D memory to the $2-\mathrm{D}$ screen display. To move the images, the system must use a hidden-surface-removal algorithm, which is necessary to make an image look realistic. When you look at a real object, the visible surfaces obscure surfaces behind them from view. When you move an image stored in three dimensions to the 2-dimensional screen, therefore, you must remove the surfaces that would be hidden from view in a real 3-dimensional object. The hidden-surfaceremoval algorithm checks each pixel in a scene and determines whether it would be visible from that particular view, and thus should be displayed in the scene, or whether it would be obscured by another pixel, and so should not be displayed.

The hidden-surface-removal algorithm can be performed in integer arithmetic. However, even though the graphics processor doesn't have to use floatingpoint arithmetic, its calculations are no fewer or less time consuming.

## But first, scan convert

Before the graphics-system processor can apply a hidden-surface-removal algorithm, it must scanconvert the polygons to determine where their edges lie. Scan-conversion techniques rely on the fact that the color and visibility of adjacent pixels is usually very similar. The program calculates the horizontal limits of the polygon. Each pixel within the polygon must have its $z$ value and color determined and placed in the $z$ buffer and frame buffer, respectively. As a result of scan conversion, the system knows the color


Fig 3-This version of the torus shows how the wireframe version can look after hidden-surface-removal and shading algorithms have been applied. (Photo courtesy Weitek Corp)
on the edges of the polygon and the z coordinate of each pixel and its color. The graphics-display system needs to know a pixel's z coordinate in order to remove hidden surfaces by using the z-buffer algorithm, and it must be able to identify the polygon's edges and their colors to perform the shading algorithms.

The z-buffer algorithm is the most popular hidden-surface-removal algorithm. It compares the depth of each pixel under examination (that is, its $z$ coordinate) with the value currently in the $z$ buffer. If the current pixel's z coordinate is smaller than the previous one in that position, the processor updates the $z$ buffer with the new pixel's z value, and updates the frame buffer with the new pixel's color.

After performing hidden-surface removal, the graphics system can display a wire-frame representation of the graphical shape. However, to color each polygon with just one color gives a rough, unrealistic rendering of the object (Fig 2).

The next step, therefore, is to use a shading algorithm. In Gouraud shading, the simplest shading scheme, the algorithm uses linear interpolation to determine what the colors on each line should be (Fig 3 ). That is, if one edge is dark red, and the horizontally opposite edge is light red, fairly realistic shading would go linearly from dark to light red. At the halfway point, a Gouraud-shaded line has gone through half of the total color change.

Gouraud shading doesn't allow for the effect of a light source, however, a technique that produces an even more realistic image. The Phong shading technique creates the effect of a single light source. Rather than


Fig 4-With the application of a Phong shading algorithm, which simulates the effects of a single light source, the teapot takes on a much more realistic look.
linearly interpolating across a line of pixels, Phong shading determines the normal vector for each pixel, and calculates the angle of incidence for the light source (Fig 4). The processor still performs a linear interpolation, but it recalculates each pixel's color on the basis of the pixel's normal vector.

There are several different ways to implement the shading algorithms in your graphics system. Only one of the three processors suitable for 3-D graphics dis-play-Intel's 80860-provides the shading algorithms on chip. The others require you to implement the shading algorithms in software or to create an ASIC that can perform shading.
With over one million transistors on a single chip, Intel's 80860 integrates a RISC core, a floating-point unit (FPU), and a hardware shading unit. (For more information on the 80860's general processing capabilities, as well as a block diagram, see the Product Update on pg 87.) The on-chip FPU is capable of peak speeds of 80 M flops. Its Linpack number is 10 M flops (by comparison, a VAX 8650 has a Linpack rating of 0.7 M flops). Keep in mind that Linpack ratings are always considerably lower than peak speed ratings, because the numbers generated in the Linpack benchmark can't fit into most on-chip caches. However, the 80860's cache is big enough to hold an entire $4 \times 4$ matrix transformation. Therefore, it can perform the transformation at close to its peak speed of 80 M flops, which allows for 500,000 transformations $/ \mathrm{sec}$.

One of the most time-consuming parts of the process of rendering the image is the z-buffer check in the hidden-surface-removal algorithm. Even a flat shading

Even a simple shading technique such as the Gouraud scheme can run over 100 times more slowly than the 3-D matrix transformations.


Because it has more than 1,000,000 transistors, the Intel 80860 processor has the density to pack a RISC core, an 80M-flops floatingpoint unit, and shading hardware all onto one chip.
of a 3-D surface is much slower than a simple 2-D fill because the processor must check the buffer for each pixel. When the buffer check is combined with Gouraud shading, the shading process can run about 100 times slower than the transform rate. The 80860 has dedicated hardware that performs the z -buffer comparisons and computes the shading interpolation on all pixels in a 64 -bit word simultaneously. (A pixel may be 8 , 16 , or 32 bits long, so each 64 -bit word may have 8 , 4 , or 2 pixels.) The shading hardware gives you a choice between Gouraud or Phong shading. Its Gouraudshading speed is 50,000 polygons $/ \mathrm{sec}$. By comparison, the Sun-4 workstation's Gouraud-shading speed is 20,000 polygons/sec.

Although the shading agorithms are implemented in hardware on the 80860 , they still don't approach the speed of the FPU. If you can't stand letting the FPU idle while the shading hardware completes its tasks, you can put the FPU to work performing applicationsoftware tasks such as simulation calculations. In this scenario, the 80860 functions as a workstation on a board. Fig 5 illustrates the architecture for a PC plugin board that incorporates the 80860 .

Note that the 80860 can operate as a stand-alone microprocessor; it does not require you to use another processor as a host. However, the software for the 80860 is totally incompatible with that for previous Intel processors, so if you wanted to run MS-DOS, you'd need an Intel host processor. Samples of the 80860 are available now. The chip will be in production
in the third quarter of this year; it will cost $\$ 750$ in OEM quantities.

Although the 80860 has 3-D graphics capability, it lacks the display-control hardware that a graphics processor has, and thus shouldn't be considered a true graphics processor. Texas Instruments' 34020, however, is a true graphics processor: It has built-in signals that support direct control of the display. It doesn't have floating-point capability, however; for that function, you need to use TI's recently introduced 34082 floating-point unit. The 34082 has a 50 -nsec clock cycle; multiplication and addition occur in parallel, giving the chip a sustained floating-point speed of 40 M flops, and a Linpack figure of 5.2 M flops. It requires only 130 cycles for a full $4 \times 4$ matrix transformation, so it can perform more than 150,000 vector transformations/sec.

The 34082 has its own C compiler and assembler, and it can address as much as 256 k bytes of memory over a local bus. These capabilities allow you to write your own routines (such as a rotation algorithm) for the 34082 and store them in the 34082 's local memory. As host, the 34020 could command the 34082 to run its own routines from local memory, thus freeing the 34020 from having to oversee the operation of the 34082.

Because the 34020 's object code is compatible with that of the chip's precursor, the 34010, a wealth of supporting graphics software already exists for the 34020. An example of such software is the Texas Instruments Graphics Interface (TIGA). The interface runs on 34010/34020 graphics plug-in boards in MS-


Fig 5-To exploit the power of many of today's PCs, whose capabilities now approach those of workstations, the PCs' graphics displays will have to be able to support workstation-quality graphics. One way to design a PC-based system with workstation-quality graphics is to plug in an 80860-based 3-D graphics add-in board that runs application software while the host processor runs the PC's operating system.

DOS systems; it standardizes the way that application software and the host processor communicate with the $34010 / 34020$ graphics processor.
According to Karl Guttag, TI graphic-strategy manager and designer of the $34010 / 34020$ family architecture, you must be careful to balance the workloads between the host processor and the graphics processor. Because of the difference in power between the 34010 and the 80286, which is often the host in PC workstations, the 34010 often had to wait for the host processor, an inefficient scheme. In 80386 -based systems, the 34010 no longer has to wait for the host. To use the processors most efficiently in such systems, you must give more thought to which tasks you assign to which processor. According to TI, 80386/34010 systems are demonstrating speed increases beyond those you'd expect to obtain by simply adding the faster host processor. The speed increases result from the redistribution of processing tasks.

The 34020 makes no provisions for 3-D color shading. If your application requires shading, you have two choices: You can either implement the algorithm in software, or you can develop your own shading ASIC. In the past, only vendors of high-end workstations could justify the time and expense of developing a


When teamed with the TMS34082 floating-point unit, the TMS34020 32-bit graphics processor from Texas Instruments can perform more than 150,000 vector transformations/sec.
shading ASIC, but this situation will soon change. National Semiconductor (Santa Clara, CA), for example, plans to introduce hardware shading chips into its stan-dard-cell ASIC library this year.

Samples of the 34020 will be available this quarter; full production of the chip will start in the fourth quarter of the year. Samples cost $\$ 500$; in production quantities, the chip will cost $\$ 100$. The 34082 's volume price will be $\$ 150$. You can expect the quantity pricing for the 34020 to fall below $\$ 50$ in two years.

## Make your graphics system stand out in a crowd

You may be concerned that designs based on singlechip processors such as the Intel and TI ICs will make your system or board too generic. This has indeed been the case with low-resolution graphics boards. There's little to distinguish one VGA-compatible per-sonal-computer board from another, for example, so price has become the determining factor in a customer's decision to buy. That's a nice situation for the customer, but the board manufacturer will want to avoid it.

One way to distinguish your design from others is to develop your own chips to accelerate one part of the graphics pipeline. For example, you could develop hardware-shading ASICs. An add-in graphics-board company with experience in this technique is Matrox (Dorval, Quebec, Canada). According to Ray Snow, graphics-board marketing manager at Matrox, when the company evaluated the various graphics chips two years ago, it particularly liked the programmability

# If the shading portion of your graphics display is too slow, consider using a shading-accelerator ASIC. 

of the TMS34010. However, it wasn't happy with the chip's relatively slow software bit-block transfer (BitBlit) speeds. Matrox developed its own ASICs to perform all BitBlit operations, windowing functions, and polygon fills. This scheme gave the company the programmability it found so attractive, as well as higher hardware BitBlit speeds. As you might expect, the company is looking for ways to accelerate shading for its next-generation 3-D graphics board. (Incidentally, Texas Instruments obviously agreed with Matrox about the need for faster BitBlits; the company incorporated faster hardware BitBlits in the 34020.)

## Parallel processing speeds displays

The third product to consider for use in 3-D graphics systems is a 2 -chip set comprising the Inmos T800 Transputer and the G300 color video controller. Inmos's T800 Transputer chip is aimed at parallelprocessing applications. Parallel-processing applications are any applications that can be broken down into subtasks and performed by several different processors at the same time, accelerating the system speed. Graphics is a prime candidate for parallel processing. For one thing, the matrix manipulations necessary in graphics processing are very repetitive in nature. Further, parallel processing lets you develop several elements of a picture independently and bring them together just before displaying them on the screen.

The G300, which Inmos recently introduced, includes all CRT control signals and performs interface to the display; it also has a color look-up table and a video

DAC. It leaves the T800 free to calculate matrix transformations, therefore (Fig 6). The T800's on-chip FPU achieves a sustained rate of 1.5 M flops for a $3-\mathrm{D}$ transformation. It transforms 50,000 vectors/sec. The T800 costs $\$ 330$ (1000); the G300 is $\$ 100$ (1000).

Note this final, significant detail: These ICs, particularly the 80860 and the $34020 / 34082$, are extremely complex chips. You may well wonder how easy it will be to perform production tests on the boards you design with them. According to Bill Rash, marketing manager for Intel's 32 -bit microprocessor line, it's the manufacturer's job to ensure that the chip is good when it leaves the factory. However, the 80860 does have some limited capability to assist you in system production testing. You can load the 80860 's output buffers serially through a test pin with your test vectors, and thus exercise the surrounding board circuitry. (Unlike the 80386 , the 80860 does not have self-test capability. The 80386's self-test capability relies on the fact that the chip is microcoded; the 80860 is not.)

As you might expect from TI, which has taken a leadership position in developing scan-path test methods, the initial version of the 34020 does incorporate a scan-path test method for emulation support. At present, the test capabilities of the 34082 are limited to forcing all pins to high, low, or 3 -state, but the next version of the chip, due in 1990, will incorporate TI's full JTAG scan-path test method.

When you first see the prices of these processors, you may be taken aback. Consider, however, that these chips can give a graphics board or system the graphics


Fig 6-Because graphics is a natural application for parallel processing, the Inmos T800 Transputer, which is eminently suitable for parallel processing, is a good candidate for a node processor in a 3-D graphics subsystem. The company's IMSG300 chip takes care of video control, including video D/A conversion.


# Manufacturers of processors for 3-D graphics 

For more information on processors that implement 3-D graphics, such as the processors described in this article, contact the following manufacturers directly, circle the appropriate numbers on the Information Retrieval Service card, or use EDN's Express Request service.

## Inmos Ltd

1000 Aztec West
Almondsbury
Bristol, UK BS12 4SQ
(0454) 616616

FAX (0454) 617910
Circle No 650

## Intel Corp

3065 Bowers Ave
Santa Clara, CA 95051
(408) 987-8080

Circle No 651
capability of a Sun-4 workstation. In light of their capabilities, the chips are actually quite cost-effective.
What's more, although people tend to think that a PC's number-crunching capability is used mostly to run application software, it's actually the graphics display that causes most of the processing overhead. Similarly, as far as the user is concerned, it's the graphicsdisplay subsystem that determines how fast the computer runs. No matter how quickly a PC performs a function internally, it's the speed with which the results show up on the screen that makes the difference. Fast processors that can handle 3-D graphics, therefore, are not just luxury options anymore; they're going to become necessary parts of graphics systems for many PCs in the near future.

EDN

## References

1. Foley, J D and A Van Dam, "Fundamentals of Interactive Computer Graphics," Addison-Wesley, 1984.
2. Conner, Margery, "Graphics engines," EDN, March 4, 1987, pg 112.

## SIMPIE.



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$\square$ Memory-based host interface.
$\square$ On-chip DMAC.
$\square$ Basic ( 16 Kbps )/primary ( 64 Kbps ) interface.
LAP-B controller: $\mu$ PD72107
$\square$ Fully implements CCITT X.25/X.75; Layer 2.
$\square$ Memory-based host interface.
$\square$ On-chip DMAC.
$\square$ Baud rate: 4Mbps (max).
SS No. 7 controller: $\mu$ PD72307
$\square$ Fully implements CCITT Q.703; Layer 2.
$\square$ Memory-based host interface.
$\square$ On-chip DMAC.
$\square$ Baud rate: $4.8 \mathrm{~K}-64 \mathrm{Kbps}$.

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## Electro/89

> Addressing the present and future needs of design engineers, Electro / 89 features information on design, new technologies, and professional career issues.

Richard A Quinnell, Regional Editor

New York City is noted for offering something for every interest-at any hour of the day or night. For three days in April, the city will offer the electronics-engineering community much of interest in the form of Electro/89- eastern US's largest design-electronics trade show and convention.

An estimated 45,000 electronics engineers will converge on the Jacob Javits Convention Center, Tuesday, April 11 through Thursday, April 13, to see and hear about the latest developments in electronics technology. The show will feature more than 900 companies exhibiting their products and will offer 25 technical sessions and eight tutorials devoted to the present and future needs of electronics engineers and managers. New to the show this year will be a special exhibit area on design-automation tools.

In keeping with this year's theme, "Building a world class economy," the keynote speaker will be Dr John G Stoessinger, noted political analyst and professor of

international affairs at Trinity University in San Antonio, TX. Dr Stoessinger is a member of the Council on Foreign Relations and author of 10 books on world politics, including the Bancroft Prize-winning The Might of Nations: World Politics in Our Time. His topic will be "Toward new horizons in the world's economy" at the keynote breakfast to be held on Tuesday, April 11 at 9:00 AM in the Marriott Marquis. Tickets for the breakfast cost $\$ 20$.

## Tracks to professional enhancement

The conference's economic theme continues in one of the six tracks along which conference organizers have arranged the professional program activities. The economic track, Entrepreneurial Activities, comprises two professional sessions. Session 14 discusses venture capital, which is characterized as an ingredient of, but "only part of the success equation," and session 18


Jacob Javits Convention Center

15, and 24). They will lead you to "Microwave technology," (session 3), "Fiber optics networks," (session 7), and two sessions, ( 11 and 15) on aspects of highdefinition television.

The New Technologies track (sessions 6, 8, 13, 19, and 22) heads in the direction of tomorrow's engineering solutions. In session 6, you can learn the status and possible implications of high-temperature superconductors in electronics. Session 8 introduces you to the quantum world of "Nanoelectronics," where dimensions are small enough to allow adjacent circuits to interact because their electron wave functions overlap. You may come away from session 22 with new

## Electro shuttle bus stops

The Electro shuttle bus will operate on show days from 8:00 AM to 7:00 PM. Here is a list of the shuttle stops:

- Lexington Ave at 42 nd St, Grand Central Station
- 7th Ave between 51st and 52nd Sts
- 45th St, just west of Broadway
- 7th Ave at 31st St, Pennsylvania Station
- 41st St between 8th and 9th Sts (Port Authority Bus Terminal)
- 49th St and 8th Ave, northeast corner

If your interests lie outside the digital world, you
ay want to follow the tracks on communications, (ses-
ons 3,7 , and 10 ) or video technology, (sessions 11,
If your interests lie outside the digital world, you
may want to follow the tracks on communications, (ses-
sions 3,7 , and 10) or video technology, (sessions 11,
If your interests lie outside the digital world, you
may want to follow the tracks on communications, (ses-
sions 3,7 , and 10) or video technology, (sessions 11,
discusses hiring consultants to attain profitability.
The Automated Design/Semiconductor/Systems track (sessions $1,4,5,16,17,20$, and 21 ) will bring you up to date on a variety of circuit technologies, including PLDs, RISCs, and ASICs. If you're seeking timely practical advice, you might want to attend session 1 for a discussion of system-design techniques using ASICs, or session 4, which discusses highdensity PLDs and their design tools. You also might consider session 20, which deals with in-circuit board programming. Those contemplating their next design may be interested in session 16, which deals with the second generation of RISC.

## Microwaves, optics, and video

# ELECTRO PROFESSIONAL-PROGRAM SCHEDULE 

| TUESDAY APRIL 11, 1989 10 AM TO NOON | SESSION 1 <br> SUCCESSFUL SYSTEM DESIGN TECHNIQUES USING ASICs | SESSION 2 <br> CHALLENGES FOR THE ENGINEER IN THE NEXT DECADE | SESSION 3 MICROWAVE TECHNOLOGY | ELECTRONIC THEATER* DIGITAL VIDEO INTERACTIVE SYSTEMS | SESSION 4 <br> HIGH DENSITY PROGRAMMABLE LOGIC DEVICES AND THEIR DESIGN TOOLS | TUTORIAL <br> SUPERCONDUCTORS IN INSTRUMENTATION AND STANDARDS <br> 9 AM TO NOON |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1:30 PM TO 3:30 PM | SESSION 5 16/32 BIT MICROCONTROLLERSSOFTWARE AND HARDWARE FEATURES | SESSION 6 SUPERCONDUCTIVITY: TECHNOLOGYI APPLICATIONS | SESSION 7 FIBER OPTICS NETWORKS | ELECTRONIC THEATER ACM/SIGGRAPH REVIEW | SESSION 8 NANOELECTRONICS | TUTORIAL legal challenges TO MANAGING THE WORKPLACE <br> 1 PM TO 4:30 PM |
| WEDNESDAY <br> APRIL 12, 1989 <br> 10 AM TO NOON | SESSION 9 OPPORTUNITIES FOR EXPERIENCED ENGINEERS | SESSION 10 <br> NEW TRENDS IN MICROWAVE, <br> MILLIMETER-WAVE <br> AND PHOTONIC DEVICE TECHNOLOGY | SESSION 11 PROGRAM PRODUCTION IN HIGH DEFINITION TELEVISION | ELECTRONIC THEATER* HIGH TECH VIDEOS | SESSION 12 WOMEN IN ENGINEERING | TUTORIAL <br> INTELLECTUAL PROPERTY FOR ENGINEERS AND MANAGERS <br> 9 AM TO 12:30 PM |
| 1:30 PM TO 3:30 PM | SESSION 13 NEW APPLICATIONS FOR ELECTRO-OPTICAL COMPONENTS | SESSION 14 VENTURE CAPITALAN INGREDIENT BUT ONLY PART OF THE SUCCESS EQUATION | SESSION 15 TRANSMISSION SYSTEMS FOR HIGH DEFINITION TELEVISION | ELECTRONIC THEATER ACM/SIGGRAPH REVIEW | SESSION 16 RISC: THE SECOND GENERATION | TUTORIAL <br> FUNDING <br> TECHNOLOGY DEVELOPMENT IN SMALL FIRMS <br> 1 PM TO 4:30 PM |
|  |  |  |  |  |  | TUTORIAL FIBER-OPTIC COMMUNICATIONS 1 PM TO 4:30 PM |
| THURSDAY APRIL 13, 1989 <br> 10 AM TO NOON | SESSION 17 <br> WHAT SHOULD YOU KNOW ABOUT VHDL, EDIF AND IGES? | SESSION 18 MANAGING FOR PROFITABILITY-THE SMART USE OF CONSULTANTS | SESSION 19 ELECTROMAGNETIC INTERFERENCEPROBLEMS AND SOLUTIONS | ELECTRONIC THEATER* ACM/SIGGRAPH REVIEW | SESSION 20 IN-CIRCUIT BOARD PROGRAMMING | TUTORIAL HIGH-DEFINITION TELEVISION 9 AM TO 12:30 PM |
|  |  |  |  |  |  | TUTORIAL <br> NEURAL NETWORKS <br> 1 PM TO 4:30 PM |
|  |  |  |  |  |  | TUTORIAL TRANSFER |
| 1:30 PM TO 3:30 PM | SESSION 21 ADVANCED LOGICMEETING DESIGNER NEEDS | SESSION 22 PERSONAL COMPUTER FOR AUTOMATIC TEST AND MEASUREMENT | SESSION 23 MEETING THE NEEDS OF THE EE PROFESSION | SESSION 24 SPACE PHOTOGRAPHY | SESSION 25 OFF CAMPUS EDUCATION FOR THE WORKING ENGINEER | IMPEDANCE METHOD OF MEASURING QUALITY OF EMI GASKETED JOINTS AND SHIELDING EFFECTIVENESS OF JOINTS 1 PM TO 4:30 PM |

*NOON-1:30 PM EACH DAY: MISCELLANEOUS VIDEOS

## Worming your way into the Big Apple

Whether you're staying in the city or just coming in for the day, the Jacob Javits Convention Cen-ter-located on 11th Ave between W 34th and W 39th Sts-is easily accessible. Both public transportation and a free Electro shuttle have stops at the center. The shuttle also has stops near hotels and transit terminals.

If you're coming in by plane, take Carey Bus from Kennedy (\$8) or from LaGuardia (\$6) Airports, or NJ Transit from Newark Airport (\$6) to the Port Authority Bus Terminal. There you can catch either a crosstown bus or the Electro shuttle to the Javits Center. If you're coming by rail to Pennsylvania Station or Grand Central Terminal, you
can catch either a crosstown bus or an Electro shuttle near the station.

The Center is served by two crosstown buses, the M-34, which runs along 34th St, and the M-42, which runs along 42nd St. Both buses stop at every block from river to river and are identified with Javits Center signs. The M34 stops across the street from the center at 11th Ave. The M-42 stops at the north end of the center's internal roadway. The fare is $\$ 1$ in either coins or tokens and transfers to north/south bus routes are free.

If you're trying to get to Electro by car, you have a challenge ahead of you. There is no parking available at the Jacob Javits Con-
vention Center. Your best bet is to park at either the Manhattan Plaza Garage (on 42nd Street between 9th and 10th Avenues) or at the Port Authority Bus Terminal garage-accessible directly from the Lincoln Tunnel or from 40th Street. Once parked, catch either the Electro shuttle in the Port Authority terminal complex or the M-42 crosstown bus. Otherwise, it's a 10 -minute walk.

An alternative to downtown parking is available if there are no afternoon baseball games scheduled. Park at either Yankee Stadium or Shea Stadium, and take the subway to 8th Ave at either 34th or 42 nd. The fare is $\$ 1$.

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ideas for using a "personal computer for automatic test and measurement."

Because an engineer's career is not based on technology alone, you may wish to follow the Professional and Personal Concerns track (sessions 2, 9, 12, and 25). Session 2 focuses on personal career development and management. Session 9 explores "Opportunities for experienced engineers," and session 12 examines the special concerns of "Women in engineering." You may also want to hear EDN's Jon Titus, along with IEEE officers and the editors of other publications at session 23, "Meeting the needs of the EE profession."

In addition to the professional sessions, Electro/89 will offer eight tutorials, covering a variety of subjects. Some tutorials of particular interest to EDN readers are "Neural networks-Models and hardware implementation," held Thursday, April 13 at 1:00 PM, and "Fiber optic communications," scheduled for Wednesday, April 12 at 9:00 AM. Tutorials are not covered by the show's registration fee, however. They range in price from $\$ 70$ to $\$ 285$.

## Don't forget the exhibits

When you are done with the professional program, you'll still have time to explore the exhibitors' booths on the convention center's main floor. The exhibits are open from 9:30 AM to 6 PM on Tuesday and Wednesday, and 9:30 AM to 4 PM on Thursday. Included in the exhibits are products in a category new to Elec-tro-design-automation tools. A cluster of more than 50 exhibitors will provide an automated design center where you can try out new developments in this growing field.
Whatever your interests, Electro/89 in New York offers something to make your day. What New York has to offer at night is yours to discover.

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Article Interest Quotient (Circle One) High 494 Medium 495 Low 496

# The comfort of analog... the power of digital. 

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Find out more about the R.S.O. benefits by calling or writing Hitachi Denshi, America, Ltd., 175 Crossways Park West, Woodbury, NY 11797. 516-921-7200. LA area 213-328-6116. Dallas area 214-233-7623.


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cells and batteries in both sealed-lead and nickel-cadmium. All intended to help you develop a product that really works.

At Gates we believe that great ideas deserve to become great products. Maybe that's why we're the company the idea people turn to most. So, give us a call at 1-800-627-1700. And experience the power of your great idea.

# Programmable device combines features of PLDs and programmable gate arrays 

The PA7024 is the first member of a CMOS programmable-device family, PEEL (programmable electrically erasable logic) ARRAYS, which combines elements of both PLDs and programmable gate arrays. The foundation of the PA7024 is its logic-control cell (LCC).

Each LCC has four primary input lines and produces two independent output signals. LCCs contain registers that can operate as synchronous or asynchronous D, T, or JK flip-flops. The input signals for each LCC are four of 80 possible sum-ofproduct terms, selected by programming.

The four input signals can be used as data for the register or to clock and control the register. An LCC's two output signals are selectable from three of its input signals or the register's output signal. One

output of each LCC connects to an I/O cell, and the other is available for creating the sum-of-product terms.
The PA7024 has 20 I/O pins and two dedicated clock-input pins. Internal to the device are 20 LCCs, $20 \mathrm{I} / 0$ cells, and a global cell interconnected through a programmable logic matrix. The device allows you to define signals in PLD-like sum-of-product terms but, as with gate arrays, creating internally used sig-
nals does not force you to sacrifice an I/O pin.
The global cell controls selection and routing of clock signals to both the I/O cells and the LCCs. This cell can treat all cells as a single group with a common set of clocks or divide them into two independent groups. The internal clocks can operate as fast as 50 MHz . The propagation delay from one I/O pin through an LCC to another I/O pin is 23 nsec. $\$ 22.50$ (100). Samples will be available in the second quarter of 1989.
International CMOS Technology Inc, 2125 Lundy Ave, San Jose, CA 95131. Phone (408) 4340678. TWX 910-997-1531. No booth. Product to be reviewed at session 4.

Circle No 658

## $100-\mathrm{MHz}$ digital-storage oscilloscope travels to the field

The PM 3308 looks like a portable typewriter, but it's actually a fullfeatured digital-storage oscilloscope. It features a maximum sin-gle-channel sampling rate of 40 M samples/sec and a sample memory of 8 k bytes. The scope also has a battery-backed 180k-byte RAMdisk, allowing storage of as many as 100 setup menus and waveforms.

The oscilloscope has a $100-\mathrm{MHz}$ bandwidth and two input channels. It can display as many as four traces, however, allowing simultaneous display of input signals and computed traces. The computed traces can be based on addition, subtraction, multiplication, division, integration, and differentiation of signals.


In addition to displaying waveforms, the oscilloscope allows you to make a variety of waveform measurements. These include time between reference points, voltage differences, $p-p$ and $r m s$ voltages,
mean and average voltages across a trace, rise time, frequency, period, and phase. A glitch-capture capability registers the occurrence of transient signals that are as fast as 10 nsec . You can make all measurements either relative to a reference or as absolute values.
The unit features an electroluminescent display screen that folds down for transporting. It weighs 14.5 lbs and comes with a shoulder strap to make carrying it to field sites easier. The PM 3308 costs $\$ 7500$. Delivery, eight weeks ARO.
John Fluke Mfg Co Inc, Box C9090, Everett, WA 98206. Phone (800) 443-5853; in OR, (206) 3566433. TLX 185102. Booth No 1559.

Circle No 657

# Electro/89 Products 

## Emulator series supports 68020 processor with clock rates as fast as 25 MHz

The HMI-200 Series in-circuit emulators now include units that support 16 - and $25-\mathrm{MHz} 68020$ microprocessors. Both units are functionally identical, differing only in operating speed. Like other members in the series, each unit operates with either a terminal or host computer controlling the unit through an RS-232C data link. The emulators have two RS-232C ports; one attaches to the controller, and the other allows data transfers such as downloading data files from a second source or printing the trace buffer's contents. The ports support data rates to 19.2 k baud.

The units allow both single-step and real-time emulation of the processor. You can program as many as four complex break and trigger
points, using combinations of address, data, status, and external signal lines to specify the activating condition. You can also program four additional break points, using simple addresses and ranges. The units offer two $4 \mathrm{k} \times 136$-bit trace buffers, which store data having 32 bits of time-tag information.
The emulators offer a number of built-in functions. For example, you can use the break points singly or in a conditional sequence to stop emulation, to trigger acquisition of data to the trace buffer, to generate an output signal for external triggering, or to measure time between break points. You can also examine and modify memory and registers, search memory for data strings, test memory, and read and write
hex files in a variety of formats.
When connected to an IBM PCor Unix-based system, the emulators allow symbolic and source-level debugging, using the optional SourceGate software. The software supports C, PL/M, and Pascal compilers from several manufacturers. You can display source code only, source and assembly, or assembly only when reading the trace buffer.

The $16-\mathrm{MHz}$ version of the HMI200 base unit costs $\$ 10,500$, and the price of the $25-\mathrm{MHz}$ version is $\$ 16,000$. Delivery, six to eight weeks ARO.

Huntsville Microsystems Inc, Box 12415, Huntsville, AL 35802. Phone (205) 881-6005. TWX 510-600-8258. Booth No 971.

Circle No 654

## Data-acquisition mainframe communicates over IEEE-488 bus

The Model 556 data-acquisition mainframe allows you to connect a variety of digital and analog signals and controls to any computer that supports IEEE-488 communications. The mainframe can accept as many as 10 plug-in cards and present them to a host computer as a single remote instrument.

The device comprises a 10 -slot card cage, a power supply, and IEEE-488 interface control logic. The unit communicates on the IEEE-488 bus as a single instrument, regardless of the number of plug-in cards inserted. To control individual cards, you must send de-vice-dependent commands to the unit; that is, commands that include the card's location. The unit's control logic can read card identifiers,

allowing you to query the unit to determine your setup. The control logic is also compatible with testinstrument software such as LabView and Labtech Notebook.
The unit is self-contained, requiring no special controller cards in the
host computer. It supplies all needed power to the plug-in cards, providing as much as 800 mA at $\pm 15 \mathrm{~V}$ and 3 A at 5 V .
The manufacturer offers a choice of 28 boards for use in the mainframe. These boards have a variety of signal input and output characteristics and provide functions such as strain-gauge signal conditioning, thermocouple sensing, and data acquisition. You can also use boards for the Model 556 with other mainframes from the same manufacturer. The Model 556 costs $\$ 1395$.

Keithley Instruments Inc, 28775 Aurora Rd, Cleveland, OH 44139. Phone (800) 552-1115; in OH, (216) 248-0400. TLX 985469. Booth No 2826.

## Circle No 653

# YOU CAN SEE HOW <br> <br> CLEAR AND BRICHT THE PICTURE IS. 

 <br> <br> CLEAR AND BRICHT THE PICTURE IS.}

## WHAT YOU CAN'T SEE IS

## HOW FAST IT RESPONDS.

Fast response time, less than 5 ms , gives Finlux Electroluminescent displays video capability. In laptop PCs, the cursor is visible during all rapid movements or data changes.

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## The big little EL display

The display above is shown as large as life. Just 18 mm thin and weighing less than 500 grammes, this Finlux EL shows as much text as an 11" CRT: 25 lines of 80 characters, or full graphics. Finlux EL displays are available in a range of $320 \times 256$ to $640 \times 400$ pixels.

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Telecopy (408) 996.7547

## Electro/89 Products

## Universal device programmer handles all available technologies

The System 3000 simplifies your de-vice-programming operation by giving you a single set of hardware for all your programming needs. The system can handle more than 1600 device types, including PLDs, PROMs, EEPROMs, and microcomputers. The unit has 2 M bits of onboard RAM as standard and is expandable to 64 M bits, allowing it to handle high-density devices.
The programming section accepts DIPs with pin counts from 16 to 40 and widths from 0.3 to 0.6 in . An optional SMD chip station handles PLCC and LCC surface-mount devices with 20 - to 68 -pin packages. Each pin location in the programming section has programmable voltage, current, and rise-time out-

put characteristics as well as the ability to sense conditions such as open and short circuits.

System 3000 handles all available programmable device technologies, including NMOS, CMOS, bipolar, and fuse-link memories. It reads electronic identifier bytes, when available, and retains its configura-
tion on power-down, thereby making setup and use easier. A userinserted IC memory card contains all the device libraries and programming algorithms needed by the unit.

The unit features a built-in keyboard and CRT display that allow you to use it as a stand-alone programmer. Offering four interface ports-two RS-232C, an IEEE-488, and a handler port, the unit lets you communicate with a host computer or peripheral equipment. $\$ 9495$.

Stag Microsystems Inc, 1600 Wyatt Dr, Santa Clara, CA 95054. Phone (408) 988-1118. Booth No 2827.

Circle No 656

# IBM PC-based software supports PLD design and modeling 

The OrCAD/PLD and OrCAD/ MOD software tools allow you to design and simulate PLD functions on an IBM PC, PC/XT, PC/AT, PS/ 2 , or a compatible computer. The OrCAD/PLD design package is either integrated with schematic capture and simulation software or can function as a stand-alone design aid. It allows you a choice of methods for describing your design. You can use schematics, Boolean equations, truth tables, or procedural state-machine programs to define your circuit's operation. The program also supports indexed equations; as a result, counters, Gray code converters, addressable latches, and other structured designs are definable with a single equation.

The PLD package generates

standard JEDEC files for programming a device. It also features a logic simulator, allowing you to create test-vector files for later design verification. When used as part of an integrated design package, the software allows you to back-annotate your schematic with text files that describe the PLD's function; it also automatically updates the schematic files whenever programming changes are made.

The modeling program, OrCAD/ MOD, serves as an extension to the OrCAD/VST verification and simulation software. MOD allows you to create simulation models based on the PLD's definition and the JEDEC file. The program combines the design information with the structure and timing characteristics of specific PLD devices. The characteristics are stored in a library file that comes with MOD. The file contains more than 300 entries and offers utility programs for creating additional models. The software packages cost $\$ 495$ each.

OrCad Systems Corp, 1049 SW Baseline St, Suite 500, Hillsboro, OR 97123. Phone (503) 640-9488. TWX 910-240-2090. Booth No 360.

Circle No 655

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pendent repair or replacement. Closed bottom design prevents solder wicking and bridging. And, naturally, latching ears are protected against overstress, and module polarization is designed in.

Now the best part: MICRO-EDGE SIMM sockets are available in the style you need. We have $100^{\prime \prime}$ or .050 " centerlines in a wide selection of singles and duals, vertical and slanted. Plus options, including a
choice of gold or tin on contact mating surfaces.

Our very-low-insertion-force design and high-reliability contacts make
the 50 mil versions especially attractive Every version comes with the quality and support you expect from AMP.

For literature and product information, contact the AMP Information Center, toll-free, at 1-800-522-6752. AMP Incorporated, Harrisburg, PA 17105-3608.

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## Electro/89 Products



POWER SUPPLIES
Series 6A, 6B, and 6C power supplies feature a mainframe enclosure that provides the main output. The mainframe accommodates and powers as many as three auxiliary modules with 2 to 48 V outputs; the overall power ratings are 600 W for the 6 A series, 800 W for the 6 B series, and 1000 W for the 6 C series. The main output values range from 2 to 24 V ; a 5 V main output provides currents of 90 to 150 mA .

You can connect outputs with identical voltages in parallel, regardless of current ratings. When so configured, outputs automatically current-share in proportion to their current ratings. Standard supply features include overvoltage protection, remote sense, automatic thermal shutdown, and soft start. The units feature an EMI filter and also include reverse-voltage protection. $\$ 939$ to $\$ 1079$. Delivery, stock to eight weeks ARO.

Powertec, 20550 Nordhoff St, Chatsworth, CA 91311. Phone (818) 882-0004. TLX 277483. Booth No 313.

Circle No 659

## CONNECTORS

L Series low-insertion-force (LIF) connectors provide the combination of small size and low contact resistance required for plug-in power supplies. These rugged rack-andpanel connectors are available with contacts rated for $8,15,25,50$, and


200A. The L Series product line utilizes a hyperboloid-type LIF socket. In addition to LIF, the socket design provides inherent immunity to shock and vibration. Socket contact resistance ranges from 0.25 to $2.5 \mathrm{~m} \Omega$. The floatmounting socket design accommodates as much as 0.049 in . of radial misalignment in blind-mating situations. The connectors are available with solder cup, crimp, and flowsolder terminations, depending on the contacts selected. The L Series units meet the performance requirements of MIL-C-28748A. \$40 to $\$ 100$ (1000). Delivery, 14 to 16 weeks ARO.
Hypertronics Corp, 16 Brent Dr, Hudson, MA 01749. Phone (800) 568-9228; in MA, (508) 568-0451. FAX 508-568-0680. Booth No 503.

Circle No 660


## HEAT SINKS

Series 6760 heat sinks provide low thermal resistance in both naturalconvection and forced-air applications. The units feature aluminum
fins that are bonded to the mounting surface with epoxy. The nine standard units in the line have hole patterns that accommodate all standard power modules.
Forced-air models will accept muffin fans that have a 4.12 -in.square mounting-hole pattern. Mounting surfaces range from $7 \times 4.78$ to $16 \times 10.78 \mathrm{in}$., and ther-mal-resistance values range from 0.024 to $0.08^{\circ} \mathrm{C} / \mathrm{W}$. Natural-convection models are 3.13 in . high and are available in 7 - and 12 -in. lengths. The heat sinks have a 7.375 -in.-wide mounting surface and are available with or without mounting flanges. Thermal resistance ranges from 0.22 to $0.3^{\circ} \mathrm{C} / \mathrm{W}$. The 7 -in. natural-convection model, $\$ 39.37$ (100). Delivery, eight to 12 weeks ARO.
Aavid Engineering Inc, Box 400, Laconia, NH 03247. Phone (603) 528-3400. Booth Nos 2660 and 2662.

Circle No 661


## SIGNAL GENERATORS

Models 2040 and 2045 arbitrary waveform generators convert data from 8-bit bytes to analog voltages at the rate of 800 M points $/ \mathrm{sec}$. You can describe the desired waveforms as mathematical equations, graphics sketches, or line segments, or you can download them from a host computer. The generators feature 512,000 points of memory that you can divide into multiple segments and 78 k bytes of battery-backed RAM that stores files containing polynomial waveform definitions. You can trigger the output wave-

## Electro/89 Products

forms or you can synchronize them to an external source.

Both generators provide a pair of analog outputs. The 2040's outputs, which are in phase opposition, have internal impedances of $50 \Omega$ and supply a 1 V p-p signal to a $50 \Omega$ load. One output of the 2045 is obtained directly from the main D/A converter, and the other passes through a programmable $64-\mathrm{dB}$ attenuator and Bessel filter. Model 2040, \$13,500; Model 2045, \$14,500. Delivery, 90 days ARO.

Analogic Corp, 8 Centennial Dr, Peabody, MA 01961. Phone (508) 977-3000. FAX 508 531-1266. TLX 949307. Booth No 2812.

Circle No 663

## PROGRAMMING SYSTEM

LabView version 2, an upgrade of version 1.2, has a compiler that significantly reduces the execution

time, provides editing capabilities like rubberbanding, and offers graphics controls such as panning and zooming. This color, icon-based programming system simplifies engineering and scientific programming on Apple Macintosh computers by permitting you to design software-generated virtual instruments. You produce these instruments by drawing block diagrams that represent test and measurement functions. You then control the instruments via pictorial renditions of the types of switches, dials,
and levers you might actually find on 3-D versions of such equipment.

To reduce memory requirements and to further increase execution speed, LabView 2 adds multiple integer and floating-point data formats to 1.2 version's extendedprecision floating-point data type. LabView 2 can run all the applications you've developed under version 1.2 and is available to owners of version 1.2 at no cost. $\$ 1995$.

National Instruments, 12109 Technology Blvd, Austin, TX 78727. Phone (800) 531-4742; in TX, (800) 433r3488. TLX 756737. Booth No 524.

Circle No 662

## IBM PC-BOARD ROUTER

The HiWire-Plus Autorouter is a gridless, via-minimizing, multilayer, IBM PC-based autorouter. It lets you make trace-specific design


## Electro/89 Products


rules; for example, you can tell the autorouter to route power networks with $21-$ mil width and $11-$ mil spacing, some signal traces with 12 -mil width and 8 -mil spacing, and other signal traces with 5 -mil width and 5 -mil spacing. The HiWire Plus Autorouter completes board routing; it lets traces cross each other and violate other design rules during the early stages of routing.
In subsequent phases of routing, the Autorouter optimizes, rips up, and reroutes vias for each network.

During the final passes, the router centers traces in the routing channels and further optimizes vias. For critical traces, you can prewire before starting the autorouter. To operate the HiWire Plus Autorouter, you need the HiWire Plus CAD package and an IBM PC, PC/XT, PC/AT, or PS/2 with 640 k bytes of RAM. A utility program can translate FutureNet, OrCAD, Schema, and Tango netlists. $\$ 895$.

Wintek Corp, 1801 South St, Lafayette, IN 47904. Phone (800) 742-6809; in IN, (317) 742-8428. TLX 709079. Booth No 760.

Circle No 665

## PROCESS METER

The model 205-P digital process meter features $0.56-\mathrm{in}$. characters and includes a power supply. It provides a $3^{1 / 2}$-digit display span. Potentiometers allow you to achieve


2000 -count zero and span adjustments from the front of the meter's panel. The full-scale signal ranges of 4 to $20 \mathrm{~mA}, 0$ to $199.9 \mathrm{mV}, 1$ to $5 \mathrm{~V}, 0$ to 10 V , and 0 to 100 V are jumper selectable. The input is true differential and features 56 dB of normal-mode noise rejection. The meter operates either from 24,100 , 115 , or 230 V ac or from 5 or 7 to 32 V de power sources. All power options feature EMI filtering, which prevents power-line noise from disrupting the meter reading. The meters are housed in a polycarbonate plastic case that carries a

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Newport Electronics Inc, 630 E Young St, Santa Ana, CA 92705. Phone (714) 540-4914. FAX 714-546-3022. TWX 910-595-1787. Booth No 2113.

Circle No 664


## SIGNAL GENERATOR

The Model 2100A-7 synthesized function/pulse generator produces sine, square, and triangular waves as well as positive and negative pro-grammable-width pulses. It covers the frequency range of 0.01 Hz to 31.16 MHz (to 10 MHz for pulses) with 7-digit resolution and accuracy of 0.5 ppm . The main output provides open-circuit voltages that you can set from $10 \mu \mathrm{~V}$ to 30 V p-p. You can also obtain outputs whose amplitude accuracy is 0.05 dB , as an option.

An auxiliary output supplies TTL levels. The pulse rise and fall times are $<11 \mathrm{nsec}$. The unit sweeps the output frequency linearly or logarithmically between start and stop frequencies that you program. You can also vary the frequency by supplying a programming voltage. Below 30 kHz , the unit can produce bursts of 1 to 255 waveforms with start and stop points programmable in $1^{\circ}$ increments from -90 to $+267^{\circ} . \$ 4750$. Delivery, six weeks ARO.

Krohn-Hite Corp, Avon IndusText continued on pg 146


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## That was then.



The Fluke 6011A Signal Generator. This innovative product featured a crystal reference oscillator, and could output frequencies from 10 Hz to 11 MHz . It signalled Fluke's major entrance into the generator market, and continued the tradition of excellence Fluke had established with their multimeter and calibration product lines for years. Introduced in the 1970's, the 6011A was Fluke's first microprocessor-based signal generator, and had an incredible 0.15 dB amplitude accuracy specification ( 0.07 dB typical). Even today, for certain applications, the 6011A remains to be the best signal generator available.

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The Fluke and Philips alliance closes the gaps Fluke once had in its signal generator line. Today, you can choose from three times as many signal sources, generating a wider range of frequencies, and offering


6062 A Synthesized RF Signal Generator. 100 kHz to 2100 MHz frequency output range, with $\pm 1 \mathrm{~dB}$ amplitude accuracy to $1 \mathrm{GHz}, \pm 1.5 \mathrm{~dB}$ to 2.1 GHz . Includes amplitude, frequency, phase and pulse modulation. Featured is a fast-rise 15 ns pulse modulator using gallium arsenide technology. IEEE-488 is standard.
more functions. The entire range covers frequencies from 0.0001 Hz (almost DC) to 2 GHz , and includes synthesized RF, LF and MF signal generators, function and pulse generators, and video and audio pattern generators.


6060 B Synthesized RF Signal Generator. 10 kHz to $1050 \mathrm{MHz} ; 1 \mathrm{~dB}$ amplitude accuracy; - 60 dBc spurious. IEEE- 488 optional.


6071 A Synthesized RF Signal Generator. 200 kHz to 1040 MHz ; high spectral purity; AM, FM, ФM modulation; precision digital sweep.


PM $5190 X$ Synthesized Function Generator. 1 mHz to 2.147 MHz ; sine, triangle, square waveforms; T7L output


6061A Synthesized RF Signal Generator. 10 kHz to 1050 MHz ; 1 dB amplitude accuracy: low SSB phase noise ( $-123 \mathrm{dBC} / \mathrm{Hz}$ ). IEEE-488 standard.


PM 5193 Programmable Synthesizer/Function Generator. 0.1 mHz to 50 MHz , full 8 digit resolution, and eight standard waveform outputs. FM AM. GATE, SWEEP, and BUIRST modulation. Full IEEE-488 control


PM 5134 Function/Sweep Generator. 1 mHz to 20 MHz ; five waveforms; sweep, burst, single modes; 20Vp-p output.


PM 5132 Function Generator. 0.1 Hz to 2 MHz ; five waveforms; sweep, VCO modes; variable duty cycle.


PM 5705 Pulse Generator. 0.1 Hz to 10 MHz ; 15 V output amplitude; 10 ns rise time; external triggering


PM 5110 Low-Distortion LF Generator. 10 Hz to 100 kHz ; $\mathrm{O} .02 \%$ distortion: sine. square waveforms.


PM 5518 Color TV Pattern Generator. Covers every RF band from IF to IV/V. and cable TV. 70 patterns.


PM 5715 Pulse Generator. 1 Hz to $50 \mathrm{MHz} ; 6 \mathrm{~ns}$ to 500 ms riselfall times, 10 V amplitude.

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commercial and military tempera-ture-range versions. $\$ 50$ to $\$ 158$ (100).

Datel Inc, 11 Cabot Blvd, Mansfield, MA 02048. Phone (508) 3393000. TWX 710-346-1953. Booth No 1704.

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## MULTIMETER

The Model 199 digital multimeter measures dc and ac voltage, dc and ac amps, ohms, and decibels. By adding an 8-channel scanner option,
you can transform the instrument into a complete multichannel measurement system. The instrument's sensitivity specs are $1 \mu \mathrm{~V}, 1 \mathrm{~m} \Omega$, and 100 nA , and its best 1 -year dcvoltage accuracy is $0.007 \%$ of reading. You can take 150 readings/sec at a resolution of $41 / 2$ digits and store them in an internal buffer. You can trigger the readings externally.

The optional scanner, which you can install at your site, offers a switching speed of 400 channels/sec, including measurement time, 2-pole and 4-pole switching, and $<1 \mu \mathrm{~V}$ thermal offset in switch contacts. The low thermal offset lets the Model 199 accurately switch and measure low signal levels. Further, the scanner's 4 -pole switching mode provides Kelvin-type (4-wire) resistance measurements. The unit can switch and take measurements across 40 channels/sec. With scanner, $\$ 1395$; without scanner, $\$ 995$.

Keithley Instruments Inc, 28775 Aurora Rd, Cleveland, OH 44139. Phone (216) 248-0400. TLX 985469. Booth No 2826.

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## DISPLAY MODULE

The Model 4285-XX canned-message module combines an 8line $\times 32$-character de gas-plasma display with an infrared touchscreen. The module provides 16 k bytes of RAM, which can store as many as 127 canned messages; the memory is backed by an onboard
battery. The touch-screen IR switch matrix provides 128 switch locations. The alphanumeric display provides a 64-character ASCII character set as well as several European character sets in a $5 \times 7$ dot-matrix format.

The software can adjust the green or neon-orange characters to three brightness levels. The module accepts RS-232C or RS422 data at 1200 or 9600 baud. The unit supports CTS (clear to send) and DTR (data terminal ready) signals and can detect parity and rate errors in transmission. Options include mounting subpanels, drip-proofing, and EMI/RFI shielding. Neonorange or red display, $\$ 1089$; green display, $\$ 1242$ (100).

IEE Inc, 7740 Lemona Ave, Van Nuys, CA 91409. Phone (818) 7870311. FAX 818-902-3723. TLX 4720556. Booth Nos 2160 and 2162.

Circle No 671


## OP AMP

The AD846 op amp uses current feedback to provide a $46-\mathrm{MHz}$ gainbandwidth product at a gain of -1 and 31 MHz at a gain of -10 . Settling time to $0.01 \%$ equals 110 nsec for a 10 V step. The offset voltage


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measures $75 \mu \mathrm{~V}$, and the offset voltage drift is $3.5 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$; the openloop transimpedance measures 200 MHz . Although the quiescent current measures only 6 mA , the AD846 delivers as much as 65 mA of output current. Input voltage noise equals $2 \mathrm{nV} / \sqrt{\mathrm{Hz}}$; input current noise for the inverting and noninverting inputs measures $20 \mathrm{pA} /$ $\sqrt{\mathrm{Hz}}$ and $6 \mathrm{pA} / \sqrt{\mathrm{Hz}}$, respectively.
The total harmonic distortion of $0.0005 \%$ at 100 kHz makes the AD648 well suited for high-performance audio-circuit applications. To implement the AD648, you use the source and feedback resistors to set the dc transfer function. However, the feedback resistor alone determines the closed-loop ac response. This eliminates the usual design tradeoffs between required gain and achievable bandwidth. The device is available in plastic miniDIPs, hermetic ceramic DIPs, and hermetic metal cans. Two operating ranges are available: -40 to $+85^{\circ} \mathrm{C}$ and -55 to $+125^{\circ} \mathrm{C}$. From $\$ 7.45$ (100).

Analog Devices, Literature Center, 70 Shawmut Rd, Canton, MA 02121. Phone (617) 935-5565. Booth No 2518.

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The shoes are useful when board space is tight. The two shoes slip under the four outer pins of the PGA and the spring snaps onto the shoes rather than the frame. You then wave-solder the entire assembly to the board. Mounts are available for $11 \times 11-, 14 \times 14-, 15 \times 15-$, and $21 \times 21$-pin PGA packages. You can use this assembly for extrudedpin or radial-machined heat sinks. $15 \times 15$-pin mount, $\$ 0.40$ (1000).

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John Fluke Mfg Co Inc, Box C9090, Everett, WA 98206. Phone (800) 443-5853, ext 88; in WA, (206) 347-6100. TWX 910-445-2943. Booth No 1559.

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## DISPLAY MODULE

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#### Abstract

Although designers often prefer dynamic RAMs (DRAMs) to their static counterparts, they sometimes shy away from using $D R A M$ s because of the devices' added complexity. This article, part 1 of a 4-part DRAM series, sheds light on some of the complex issues surrounding DRAMs and describes the different DRAM architectures. The succeeding articles will cover memory-system architectures, DRAM controllers, and DRAM-board design.


## Steve Gumm and Carl T Dreher, Texas Instruments

When constructing a memory system, designers most commonly choose the dynamic RAM (DRAM) as the basic building block. The DRAM owes its popularity to the fact that it costs less than the static RAM (SRAM), yet has a higher bit density, an advantage that stems from the DRAM's simple, tiny memory cells. It's true that DRAMs require more housekeeping than SRAMs do: The term "dynamic" implies that the data in the memory cells must continually be accessed or refreshed to ensure that the stored data is valid. Nevertheless, DRAMs' lower cost and smaller size more than make up for any deficiencies.

A designer's first encounter with DRAMs can often be intimidating. The uninitiated engineer must confront such terms as "page-mode access," "static-column
mode access," and "nibble-mode access," as well as "refresh rate," and "precharge period." The designer also faces a host of timing parameters, which can be perplexing. Even after you understand these bewildering terms, you must choose from among a vast number of options the DRAM architecture that best suits your needs.
The most common type of DRAM, which is classified as $\mathrm{N} \times 1$, stores 1 bit of data in N addressable locations. Each device has a 1-bit input and a 1-bit output data bus. Current single-package bit densities for this family range from 16 k bits to 1 M bits; 256 k bits is the most popular. Other less-common types include the $\mathrm{N} \times 4$ and $\mathrm{N} \times 8$ DRAMs, which have 4 - and 8 -bit data buses, respectively. Although this discussion is restricted to $\mathrm{N} \times 1$ DRAMs, you can easily apply the information presented here to DRAMs with wider buses.

## The difference between SRAMs and DRAMs

Accessing data in a DRAM is different from accessing data in an SRAM. The DRAM has a multiplexedaddress arrangement, which conserves package space. To access data, a 256 k -byte DRAM requires 18 addresses $\left(2^{18}=256 \mathrm{k}\right)$. To accommodate these addresses on separate pins-along with the normal complement of pins for power, control, and I/O data-would require a 24 -pin package. The DRAM has nine address lines ( $\mathrm{A}_{0}$ through $\mathrm{A}_{8}$ ) and two strobe lines for accessing data. Essentially, the DRAM accesses a row and a column of an array by internally latching a row address with

Even though they require more housekeeping than SRAMs do, DRAMs' lower cost and component size more than make up for any deficiencies.
the Row Address Strobe (RAS) and a column address with the Column Address Strobe (CAS). Because both addresses are multiplexed onto the same pins, 256 k -bit DRAMs come in 16 -pin packages and 1M-bit DRAMs come in 18 -pin packages.
Besides multiplexed addressing, the most significant differences between SRAMs and DRAMs are their refresh and precharge requirements. A DRAM's memory cell consists of a storage capacitor. When a charge is placed on this capacitor for data storage, the charge must be periodically refreshed; otherwise, the capacitor will discharge, invalidating the stored data. Some of the older 16 k -bit DRAMs must be refreshed every 2 msec ; newer 1 M -bit DRAMs specify a $10-\mathrm{msec}$ refresh rate.
The DRAM's architecture simultaneously refreshes all of the column cells for a selected row every time the row is accessed. Furthermore, some DRAMs reserve the most significant bit (MSB) as a select bit for an internal multiplexer that selects data in two banks of arrays. In these DRAMs, the lower address bits access the memory cells in both banks simultaneously. This arrangement cuts the required number of refresh cycles in half. For example, a 64 k -bit DRAM, which has eight row- and column-address lines, requires a
refresh cycle for only 128 rows instead of 256 . Similarly, a 256 k -bit DRAM requires only 256 cycles, and a 1M-bit DRAM requires only 512 cycles.

Another peculiarity of the DRAM is precharge. Performing a memory-read operation from a DRAM cell causes its capacitor to discharge slightly. Therefore, data must be written back into the cell after each read operation. This write-back operation is called "precharge" and is automatically handled by the DRAM. The time it takes to perform this operation is called the precharge period, and you must account for it when you determine the read-cycle time for the DRAM.

An $N \times 1$ DRAM has two pins, $D$ and $Q$, for handling the input and output (I/O) data. In most of these DRAMs, the data-out line (Q) goes to the highimpedance state when inactive, so you can tie it to the data-input line (D) in order to handle bidirectional data. Other DRAMs require external 3 -state buffers to handle bidirectional data. In order to conserve package size, $N \times 4$ and $N \times 8$ DRAMs share a set of bidirectional pins.

Perhaps the most intimidating features of DRAMs are their timing diagrams. Most of the turmoil centers on the sheer number of timing specifications and the combination of abbreviations used to describe them.


Fig 1-A DRAM's internal architecture determines which of the variety of DRAM modes it can support. The TMS4256-12 DRAM, for example, has a 4-to-1 multiplexer that can access four memory arrays to support nibble-mode access.

## TABLE 1-PARAMETER ABBREVIATIONS

| PARAMETER | ABBREVIATION |
| :--- | :---: |
| COLUMN OR $\overline{\text { CAS }}$ | C |
| ROW OR RAS | R |
| LOW SIGNAL | LIGH SIINAL |
| ACCESS TIMES | H |
| HOLD TIMES | a |
| SETUP TIMES | su |
| PULSE WIDTH | su |
| READ OPERATION | WRITE OPERATION |
| CYCLE | rd |
| ADDRESSES | W |
| DATA | A |
|  | A |
|  |  |

The abbreviations listed in Table 1 will help you decipher the timing specifications. For example, the minimum pulse width during which the CAS line is low is abbreviated as " $\mathrm{tw}(\mathrm{CL})$." The w indicates pulse width, the C indicates $\overline{\mathrm{CAS}}$, and the L means "low." Similarly, the setup time for a row address is abbreviated as "tsu(RA)."

To accommodate a DRAM's timing requirements, the memory system requires a DRAM controller, which generates the control signals and interfaces the DRAM to the system's CPU. Some CPUs, such as the Z80, include a DRAM controller on chip. Most CPUs, however, require an external circuit that functions as the DRAM controller. The controller must coordinate the system access while guaranteeing that the DRAM is refreshed within its specified period. Ideally, the DRAM controller fools the system CPU into believing that it's communicating with an SRAM.

To use a DRAM effectively, you must pay attention to a number of timing parameters. The read cycle is probably the easiest of these parameters to understand, and it also demonstrates many of the DRAM's timing principles. Fig 1 shows the timing parameters for a 256 k -bit DRAM (the TMS4256-12).

## Reading and writing

A read cycle begins when the controller issues a row address and drives the $\overline{\text { RAS }}$ line low, thus strobing the address into the DRAM. The address must be stable for tsu(RA) seconds (row-address setup time) before the falling edge of the $\overline{\mathrm{RAS}}$ line, and it must remain stable for a minimum of $\operatorname{th}(\mathrm{RA})$ seconds (rowaddress hold time) after the falling edge (Fig 2a). The $\overline{\mathrm{RAS}}$ line must remain low during the entire read cycle. Because the $\overline{\mathrm{CAS}}$ line not only strobes in the column


Fig 2-The timing diagrams for a DRAM's read cycle illustrate many of the device's timing constraints. The timing parameters shown here are for the TMS4256-12 DRAM's $\overline{R A S}$ (a) and CAS (b) lines, which strobe a row and a column address, respectively, into the DRAM.
address but also enables the output buffer, it should be high when strobing the row address into the DRAM. Keeping the CAS line high ensures that the Q output is in a high-impedance state.

Next, the controller must issue a column address to the DRAM. Once the column address is stable for the minimum setup time of tsu(CA) seconds, the controller drives the CAS line low to strobe the address into the DRAM. The falling edge of the $\overline{\mathrm{CAS}}$ line should not occur any sooner than tRLCL (RAS-low to CAS-low time) seconds after the falling edge of the $\overline{\mathrm{RAS}}$ line (Fig 2b). Because the $\overline{\mathrm{CAS}}$ line also enables the output buffer, the WRITE line should be high in order to activate the read cycle when $\overline{\mathrm{CAS}}$ is low. After the falling edge of the CAS line, there is an access delay of $\mathrm{ta}(\mathrm{C})$ seconds before the output buffer is enabled.

To ensure that the output data is valid, you must observe one more critical timing parameter, $\mathrm{ta}(\mathrm{R})$. This parameter specifies the minimum time that must elapse after the falling edge of the $\overline{\text { RAS }}$ line before the output data is valid. Even though the controller satisfies the requirements for the other delays, such as $\operatorname{ta}(\mathrm{C})$, the output data is not valid until $\mathrm{ta}(\mathrm{R})$ seconds. For this reason, manufacturers quote $t(R)$ when specifying a DRAM's speed.

## The DRAM's multiplexed-address arrangement conserves package size.



Fig 3-Once the strobe lines load a row and a column address into the DRAM, the controller must wait until the data becomes valid (a) before it can read the data on the $Q$ bus. After reading the data, the controller resets the strobe lines high (b).

To understand the importance of the $\operatorname{ta}(\mathrm{R})$ parameter, consider the following example. The TMS4256-12 DRAM specifies a minimum time of 25 nsec for the tRLCL parameter, and it specifies $\operatorname{ta}(\mathrm{C})$ as 60 nsec . Therefore, data appears at the output 85 nsec after the falling edge of the $\overline{\mathrm{RAS}}$ line. However, the DRAM's $\operatorname{ta}(\mathrm{R})$ specification is 120 nsec . Even though data is available at the output 85 nsec after the falling edge of the RAS line, it is not valid until 120 nsec after the falling edge-an additional 35 nsec ( $\mathbf{F i g} \mathbf{3 a}$ ).

To terminate the read operation, the controller must bring the $\overline{\text { RAS }}$ and $\overline{\text { CAS }}$ lines high. Each line, however, must remain low for a minimum pulse width ( $\mathrm{tw}(\mathrm{RL}$ ) and $t w(C L)$, respectively) before returning to the high state. For the TMS4256-12 DRAM, $\mathrm{tw}(\mathrm{RL})$ and $\mathrm{tw}(\mathrm{CL})$ are specified as 120 nsec and 60 nsec, respectively. In addition, the RAS line should not return high until tCLRH seconds (CAS-low to RAS-high time) after the falling edge of the $\overline{\mathrm{CAS}}$ line. Similarly, the $\overline{\mathrm{CAS}}$ line should not return high until tRLCH seconds (RAS-low to CAS-high time) after the falling edge of the RAS line. For the TMS4256-12, tCLRH and tRLCH are 60 nsec and 120 nsec, respectively (Fig 3b).

Returning the $\overline{\text { CAS }}$ line high disables the DRAM's output buffer. However, the output line is not in a high-impedance state until tdis(CH) seconds (disable time after CAS-high) after the rising edge of the CAS line. A typical value for $\operatorname{tdis}(\mathrm{CH})$ is 30 nsec.

Driving the $\overline{\text { RAS }}$ and $\overline{\text { CAS }}$ lines high does not completely terminate the read cycle. The next cycle can't begin until the DRAM automatically writes data back into the previously accessed location during the pre-
charge period. The precharge period occurs while both the strobe lines are held high for a minimum specified pulse width, $\mathrm{tw}(\mathrm{RH})$ and $\mathrm{tw}(\mathrm{CH})$. For the TMS4256-12 DRAM, $\mathrm{tw}(\mathrm{RH})$ is 100 nsec and $\mathrm{tw}(\mathrm{CH})$ is 25 nsec. Because $\operatorname{tw}(\mathrm{RH})$ is longer, you must observe it when calculating the read-cycle time.
The only restrictions placed on the $\overline{\text { WRITE }}$ line during the read cycle are that it must be high for tsu(rd) seconds before the falling edge of the CAS line, and that it must remain high for th(CHrd) seconds after the rising edge of the $\overline{\mathrm{CAS}}$ line. Because the TMS425612 specifies these times as 0 nsec, the WRITE line must simply be high during the time that $\overline{\mathrm{CAS}}$ is low.
You can now piece together the timing parameters for determining the DRAM's minimum read-cycle time. Because $\operatorname{ta}(\mathrm{R})$ is longer than the sum of tRLCL and $\mathrm{ta}(\mathrm{C})$ for the TMS4256-12, it dominates this portion of the cycle. The remainder of the cycle consists of the $25-\mathrm{nsec} \operatorname{tw}(\mathrm{CH})$, the $100-\mathrm{nsec} \mathrm{tw}(\mathrm{RH})$, the 60 -nsec tCLRH, and 30 -nsec $\mathrm{tdis}(\mathrm{CH})$ minimum time periods. Because all of these time periods occur simultaneously, and $\mathrm{tw}(\mathrm{RH})$ is the longest period that must be maintained, the read cycle consists of the sum of $\operatorname{ta}(\mathrm{R})$ and $\operatorname{tw}(\mathrm{RH})$, or $120+100=220 \mathrm{nsec}$. Strictly speaking, you should add the maximum time allotted for the $\overline{\mathrm{RAS}}$ to make a transition between logic levels; this maximum time is specified as 5 nsec. Adding 5 nsec for each of the cycle's two transitions produces a minimum read-cycle time of 230 nsec (Fig 4).
Writing to a DRAM involves most of the same timing parameters that a read operation does. The primary difference between the read and write operations lies
in the timing parameters associated with the $\overline{\text { WRITE }}$ line. Essentially, you can use one of two methods to write to a DRAM-the early-write cycle or the de-layed-write cycle. Your choice of write cycle will depend on your application (see box, "Weigh early- vs delayed-write cycles").
The early-write and delayed-write cycles are distinguished by whether the WRITE line is asserted before or after the CAS line is asserted. During an early-write cycle, the controller drives WRITE low prior to driving CAS low. Fundamentally, the falling edge of the CAS line strobes the input data into the DRAM and acts as a reference for the address setup and hold times. During a delayed-write cycle, $\overline{\text { WRITE }}$ strobes the data into the DRAM after the controller asserts the CAS line low. The address setup and hold times are referenced to the falling edge of the $\overline{\text { WRITE line. }}$
During a delayed-write cycle, $\overline{\mathrm{CAS}}$ is low for a certain time while WRITE is high, so the output drivers are briefly enabled as if the DRAM were executing a read operation. Therefore, unless the memory array has separate input and output buses, the delayed-write operation can cause bus conflicts (Fig 5). In the earlywrite cycle, the output drivers are not enabled, because the controller asserts the WRITE line low before setting the CAS low. Therefore, you can tie the D input line directly to the Q output line in order to accommodate a bidirectional bus.
The WRITE line must remain low for at least the period specified by $\mathrm{tw}(\mathrm{W})$. (For the TMS4256-12,


Fig 4-Before the controller can execute two successive reads, it must wait for the DRAM to refresh the previously accessed cell during the precharge period. The minimum read-cycle time for the TMS4256-12 DRAM—230 nsec-includes a 100-nsec minimum precharge period.


Fig 5-The timing parameters for the delayed-write cycle are appealing for many applications. However, asserting $\overline{C A S}$ while the WRITE line is high causes the DRAM's output buffers to turn on, which, in turn, causes a potential bus conflict.
$\mathrm{tw}(\mathrm{W})$ is specified as 40 nsec .) During a delayed-write cycle, the WRITE pulse must also remain low for tw (CLW) and tw (RLW) seconds after the falling edges of the $\overline{\mathrm{CAS}}$ and $\overline{\mathrm{RAS}}$ lines, respectively. (For the TMS4256-12, tw (CLW) is 35 nsec , and tw (RLW) is 95 nsec.) Further, the falling edge of the WRITE line must occur at least tsu(WCH) and tsu(WRH) seconds, respectively, before the $\overline{\mathrm{CAS}}$ and $\overline{\mathrm{RAS}}$ lines return to their high states. Both these setup times are specified as 40 nsec for the TMS4256-12 DRAM.

In a delayed-write cycle, the data must be stable for at least $\mathrm{tsu}(\mathrm{D})$ seconds before the falling edge of the $\overline{\text { WRITE }}$ pulse, and it must remain stable for at least tw (WLD) seconds after the same falling edge. The TMS4256-12 specifies tsu(D) as 0 nsec and tw(WLD) as 35 nsec. Because there is no time limit on the $\overline{\text { WRITE }}$ pulse after the $\overline{\text { CAS }}$ line is driven low, the write operation can be delayed for as long as the refresh period demands.

## Don't forget to write

The difference between the early-write cycle and the delayed-write cycle lies mainly in the data setup and hold requirements. In the early-write cycle, the data must be stable for at least tsu(D) seconds before the falling edge of the CAS line. In addition, the data must remain stable for at least tw(CLD) seconds after this falling edge and also for tw(RLD) seconds after the falling edge of the $\overline{\mathrm{RAS}}$ line. The th(CLD) and $\operatorname{th}(\mathrm{RLD})$ specifications for the TMS4256-12 are 35 nsec

Besides multiplexed addressing, the most significant differences between SRAMs and DRAMs lie in the devices' refresh and precharge requirements.


Fig 6-In the early-write cycle, the DRAM controller drives the $\overline{\text { CAS }}$ line low after it sets the $\overline{\text { WRITE }}$ line low. Therefore, the $D R A M$ 's $Q$-output buffers remain in the high-impedance state.
and 95 nsec, respectively. Fig 6 shows a complete early-write cycle.
Like the read-cycle time, the minimum $\mathrm{tw}(\mathrm{RL})$ time exceeds the sum of the other overlapping timing parameters once the controller drives the $\overline{\mathrm{RAS}}$ line low. Therefore, you calculate the minimum write-cycle time ( $\mathrm{tw}(\mathrm{W})$ ), by simply adding $\mathrm{tw}(\mathrm{RL}), \mathrm{tw}(\mathrm{RH})$, and the edge-transition times. The minimum write-cycle time for the TMS4256-12 is $230 \mathrm{nsec}(120+100+2 \times 5=230)$. Because tw(RL) is the dominant write-cycle timing parameter, the minimum write-cycle time is the same for both the early- and the delayed-write cycles.

Before you can read or write to a DRAM, the DRAM controller must execute a power-up sequence that initializes the data in the DRAM. The sequence consists of a short delay followed by a number of write cycles, which charge the memory-cell capacitors. The TMS4256 specifies the delay as $200 \mu$ sec plus eight initialization cycles. If you don't include the power-up sequence in the design, a diagnostic test will erroneously detect failures in a perfectly good memory system.

## The pause that refreshes

The DRAM controller's highest priority task is to ensure that the DRAM experiences a complete refresh cycle during the specified refresh period. A refresh can occur through a read or write operation or through a specific refresh operation. The TMS4256-12 specifies a refresh period of 4 msec . Because the DRAM's inter-
nal architecture has two simultaneously addressed memory banks, the controller needs to refresh only 256 rows during the 4 -msec period.

When the controller accesses a row during the refresh cycle, it must adhere to the same timing constraints that it observes for the read and write cycles. Therefore, refreshing all the rows in the TMS4256-12 DRAM takes $256 \times 230 \mathrm{nsec}=58.8 \mu \mathrm{sec}$. This worstcase refresh-cycle time ( $58.8 \mu \mathrm{sec}$ ) occupies $1.5 \%$ of the allotted 4 -msec refresh period. Slower versions of the same DRAM have the same 4-msec refresh-period specification, but occupy a greater bandwidth because of the longer access times.

RAS-only refresh is one of a variety of methods for refreshing DRAMs. In this method, the controller holds the $\overline{\text { CAS }}$ line high while using the $\overline{\mathrm{RAS}}$ line to strobe a row address into the DRAM. The controller remembers which rows have been accessed during a refresh period to ensure that it services all the rows (Fig 7a). The DRAM's output drivers are never enabled during a refresh, because the $\overline{\text { CAS }}$ strobe is always high. The minimum time it takes to refresh an entire row is the same as the minimum read-cycle time.

The hidden-refresh method attempts to make refreshing transparent by inserting a refresh cycle when the CPU is decoding an op code after a memory read (Fig 7b). For many of today's high-speed $\mu \mathrm{Ps}$, this method is too slow to be practical. The controller initiates the refresh by strobing a row and a column address into the DRAM during a standard memory-read operation. However, instead of going high again at the end of the cycle, the CAS line remains low, latching the output data on the Q bus. Subsequently, the controller toggles the $\overline{\mathrm{RAS}}$ line, causing the DRAM to generate a row address internally. The DRAM contains an internal address generator that sequentially generates a row address on each rising edge of the RAS line when the $\overline{\text { CAS }}$ line is low. During this time, the DRAM ignores the external address bus. Because the DRAM's output drivers are activated throughout the entire cycle, hidden refresh consumes more power than RASonly refresh.

Automatic CAS-before-RAS refresh combines the best aspects of RAS-only refresh and hidden refresh. In this method, the controller initially asserts the $\overline{\mathrm{CAS}}$ line low before asserting the RAS line low. The DRAM's internal address generator then sequentially generates the row addresses after the controller has toggled the $\overline{\mathrm{RAS}}$ line. Because this method asserts the CAS line low when the RAS line is high, the DRAM's


Instead of refreshing the DRAM at selected intervals, burst refresh rejuvenates all the rows in one burst. Although this method furnishes the CPU with a longer period of uninterrupted access time, it produces a very long latency period if the CPU desires access to the DRAM during the refresh burst. Therefore, burst refresh is used only in applications in which the long uninterrupted access time is a must.

Some refresh methods even scrub the data in the DRAM, occasionally removing any soft errors incurred over time. DRAMs are more susceptible to soft errors than are SRAMs. Soft errors are often caused by alpha particles that are emitted by radioactive impurities in a DRAM's package. Although the probability of an individual soft error is small, the cumulative probability of an error increases as the memory size increases. During a scrubbing refresh cycle, the controller reads the accessed data and provides error detection and correction (EDC). The controller then rewrites any corrected data back into the DRAM.

Besides offering various refresh methods, modern


Fig 7-Three common methods for refreshing DRAMs include $R A S$-only refresh (a), hidden refresh (b), and automatic CAS-before-RAS refresh (b). The controller accesses the DRAM at selected intervals to implement these refresh schemes.

DRAMs provide an assortment of modes for accessing data in the storage cells. (Table 2 summarizes many of the advantages and disadvantages of the available DRAM access modes.) To enhance the access speed, all of these modes rely on the principle that it's not necessary to strobe both the row and the column addresses into the DRAM when you access small portions of consecutive memory space. By eliminating some of the address strobes, these access modes shorten the overall access time and reduce the overall precharge time. Because most DRAMs support only one option, the DRAM controllers for a particular design are often unique, preventing you from mixing DRAMs that have different access modes.

Page-mode memory access establishes a constant row address, while the controller strobes a series of

> Performing a read operation from a DRAM cell causes the capacitor to discharge slightly.
column addresses into the DRAM (Fig 8a). The controller strobes both a row and a column address into the DRAM on the first access, but from there on, it strobes only column addresses into the DRAM (by using the CAS line) during access periods. The maximum permissible time for $\mathrm{tw}(\mathrm{RL})$ (the maximum time for the $\overline{\mathrm{RAS}}$ line to remain low) determines the maximum number of columns that are accessible during one pagemode access period.

In page-mode access, the minimum cycle time for strobing a column address into the DRAM is the sum of the minimum $\mathrm{tw}(\mathrm{CH}) \mathrm{P}$ (the CAS-high pulse width in page mode), the minimum $\mathrm{tw}(\mathrm{CL})$ (the $\overline{\mathrm{CAS}}$-low pulse width), and the minimum time required for two edge transitions. For the TMS4256-12, this cycle time is 120 nsec . Because the maximum value for $\mathrm{tw}(\mathrm{RL})$
is specified as $10 \mu$ sec, the controller can address about 83 columns during a single page-mode access period.

In DRAMs that feature an enhanced page-mode option, the internal column-address latch is transparent when the CAS line is high. This arrangement gives the DRAM's column decoder direct access to the address when the latch is in its transparent state. An access cycle begins immediately, therefore, when a valid column address appears on the address bus. The transparent latch eliminates the column-address setuptime constraint. The falling edge of the CAS line latches the column address, and the rest of the cycle behaves as a standard page-mode cycle (Fig 8b).
Some DRAMs feature a static-column mode for highspeed read and write access. These DRAMs have a 3 -state input column-address buffer instead of a col-

## Weigh early- vs delayed-write cycle

Most DRAMs offer both earlyand delayed-write cycles. Which type of write cycle you choose will depend heavily on your application's timing parameters and system architecture. For example, consider a system design that uses a CPU, such as an $8086 \mu \mathrm{P}$, that has a multiplexed address/ data bus. The CPU communicates with external memory by placing a destination address on its I/O pins. After a suitable delay, it transfers data to or from memory by using the same I/O pins. An early-write cycle seems well suited for this application because it doesn't need 3 -state buffers for eliminating bus conflicts. In either case, you need a DRAM controller to coordinate the action between the two devices.

In the early-write cycle, the CPU initiates a write cycle by placing a row address on its I/O pins. The DRAM controller, which is located between the CPU and the memory, latches the address and begins an early-
write cycle by driving the DRAM's $\overline{\text { RAS }}$ and WRITE lines low. After the CPU places a column address on the bus, the controller latches the address. Before the controller can drive the $\overline{\mathrm{CAS}}$ line low, however, it must wait for the CPU to multiplex the data onto the I/O pins. Once the controller determines that the data is stable, it can then drive the $\overline{\mathrm{CAS}}$ line low for the minimum $\operatorname{tw}(\mathrm{CL})$ seconds. After this procedure, the controller can return the $\overline{\text { CAS }}, \overline{\text { RAS }}$, and $\overline{\text { WRITE }}$ lines to their high state.
Now consider using a delayedwrite cycle under the same circumstances. Once again, the CPU initiates a write cycle by placing a row address on its I/O pins. The controller latches the address and begins a delayed-write cycle by driving the RAS line low. Because the controller holds the $\overline{\text { WRITE }}$ line high, it can issue a low on the CAS line while it's waiting for the data to stabilize. By driving the $\overline{\mathrm{CAS}}$ line low, the
controller enables the DRAM's output buffers. Therefore, your system requires additional 3 state buffers in order to prevent bus conflicts. When the controller detects that the data from the CPU is stable, it writes the data into the DRAM by driving the WRITE line low for a minimum of $\mathrm{tw}(\mathrm{WL})$ seconds during the remainder of the cycle.
In this sample application, the difference between an earlywrite cycle and a delayed-write cycle is the difference between the DRAM's minimum tw(CL) and $\mathrm{tw}(\mathrm{WL})$ specifications. The TMS4256-12 DRAM specifies the minimum tw(CL) time as 60 nsec and the minimum $\mathrm{tw}(\mathrm{WL})$ time as 40 nsec . For this application, therefore, the delayed-write cycle is the cycle of choice, even though it will force you to use additional hardware, because it's 20 nsec faster than the earlywrite cycle. For slower DRAMs, the difference can be even more pronounced.

## TABLE 2-COMPARISON OF DRAM MODES

| MODE |  | advantages | disadvantages |
| :---: | :---: | :---: | :---: |
| $\begin{aligned} & \text { w } \\ & \frac{y}{x} \\ & \frac{1}{3} \\ & \frac{0}{2} \end{aligned}$ | EARLY-WRITE | CAN TIE DRAM INPUT TO OUTPUT; NO 3-STATE BUFFER NEEDED | SLOWER THAN DELAYED-WRITE |
|  | DELAYED-WRITE | FASTEST ACCESS | REQUIRES 3-STATE BUFFER |
|  | RAS-ONLY | LOW POWER; ALL Q buFFERS ARE IN HIGHIMPEDANCE STATE | EXTERNAL CIRCUIT MUST GENERATE ROW ADDRESS |
|  | HIDDEN | DRAM GENERATES ROW ADDRESS INTERNALLY, SIMPLIFYING DRAMCONTROLLER DESIGN; REFRESH IS HIDDEN DURING SLOW CPU CYCLES | Q BUFFER IS ON DURING REFRESH; HIGHER POWER THAN RAS-ONLY; USEFUL ONLY FOR SLOW CPUs |
|  | CAS-BEFORE-RAS | DRAM GENERATES ROW ADDRESS INTERNALLY, SIMPLIFYING DRAMCONTROLLER DESIGN; LOW POWER | REQUIRES DRAMS THAT SUPPORT THIS MODE |
|  | BURST | AFTER REFRESH BURST, MEMORY IS AVAILABLE FOR MAXIMUM REFRESH PERIOD (4 TO 15 mSEC ) | DURING REFRESH BURST, MEMORY IS UNAVAILABLE; REQUIRES SPECIAL DRAM CONTROLLER |
|  | SCRUBBING | PREVENTS SOFT ERRORS IN HIGH-RELIABILITY AND LARGE-MEMORY SYSTEMS | REQUIRES EXTERNAL EDC CIRCUITS; MEMORY ACCESS USUALLY SLOWER DUE TO EXTRA BUFFERS IN DATA PATH |
| U <br> 0 <br> 0 <br> $\sum$ <br> 0 <br> 0 <br> 0 <br> 0 | PAGE | LOW POWER; ALLOWS RANDOM ACCESS WITHIN ANY ROW; DOES NOT REQUIRE SPECIAL DRAMs | NEEDS SOPHISTICATED DRAM CONTROLLER; ACCESS USUALLY SLOWER WHEN CONTROLLER ACCESSES RANDOM ROWS |
|  | ENHANCED PAGE | FASTER THAN PAGE-MODE SINCE COLUMN DECODE OCCURS BEFORE CAS; LOW POWER; ALLOWS RANDOM ACCESS WITHIN ANY ROW; does not require SPECIAL DRAMs | NEEDS SOPHISTICATED DRAM CONTROLLER; ACCESS USUALLY SLOWER WHEN CONTROLLER ACCESSES RANDOM ROWS |
|  | STATIC-COLUMN | VERY FAST ACCESS; ALLOWS RANDOM ACCESS WITHIN ANY ROW | HIGH POWER BECAUSE Q BUFFERS ARE ON BETWEEN ACCESSES; REQUIRES 3-STATE BUFFERS; NEEDS SOPHISTICATED DRAM CONTROLLER, SPECIAL DRAMs; ACCESS IS USUALLY SLOWER WHEN CONTROLLER ACCESSES RANDOM ROWS |
|  | CYCLIC | FASTEST ACCESS FOR SYSTEMS DOING CACHE BURST FILL | NEEDS SPECIAL DRAMs, SOPHISTICATED DRAM CONTROLLER; IS SLOW IF ADDRESSES ARE NOT SEQUENTIAL |

umn-address latch. When the CAS line is high, this input buffer is in the high-impedance state. The controller initiates the first static-column access by asserting the RAS line and then the $\overline{\text { CAS }}$ line. Holding both lines low throughout the access period, the controller accesses the subsequent columns by altering the column address. This method eliminates the setup, hold, transition, and precharge times associated with toggling the $\overline{\text { CAS }}$ line (Fig 8c).

Because DRAMs inherently can't support both pagemode and static-column-mode access, you must choose the mode that best suits your system. Essentially, both modes provide the CPU with a low-cost cache memory by virtue of their fast access to a small block of the system's memory (there are many columns within a
single row). One factor in your choice is access-mode speed. Although static-column mode is faster than page mode (because static-column mode eliminates some timing restrictions), the controller must alter the column address quickly enough to realize the speed advantage.

Power consumption is another consideration. Because the output buffers are continually enabled during static-column access, a DRAM that uses static-column mode consumes more power than does a DRAM that uses page-mode access. In either case, when there are frequent row changes, both modes can often be slower than direct read and write cycles because of the extra overhead in the DRAM controller.

The TMS4256 DRAM's architecture offers the use

Ideally, the DRAM controller fools the system CPU into believing that it's communicating with an SRAM.


Fig 8-When designing a memory system, you must choose from a number of access-mode options before selecting a DRAM for a particular application. To implement page-mode (a), enhanced page-mode (b), or static-column mode (c) access, for example, you require a controller that's customized to support the mode you choose.
of nibble mode for reading and writing data. As shown in Fig 1, each of the DRAM's dual memory banks are further subdivided into dual 64 k-bit blocks. Furthermore, the DRAM contains a 4 -to- 1 multiplexer, which selectively enables one of the four 64 k -bit blocks. Bit $\mathrm{A}_{8}$ for the row and column addresses determines which block is initially selected. After accessing an initial block, the controller indexes the other three blocks by toggling the $\overline{\text { CAS }}$ line three times while maintaining a low on the RAS line. Each falling edge of the CAS line exercises the multiplexer-select lines circularly through the following sequence:

$$
\longrightarrow(0,0) \longrightarrow(0,1) \longrightarrow(1,0) \longrightarrow(1,1) \longrightarrow
$$

In this way, the controller can access 4 bits (a nibble) of data with one set of row and column addresses. Typically, the access time for the final 3 bits is 60 nsec/bit.


DRAMs offer two other modes of access: byte mode and serial mode. Byte mode is identical to nibble mode, except that in byte mode, the DRAM contains an 8 -to- 1 multiplexer. To select the initial block, the 8 -to- 1 multiplexer selects data from one of eight memory blocks based on address bits $\mathrm{A}_{8}$ and $\mathrm{A}_{9}$. Serial mode is similar to byte mode, except that in serial mode, the controller can sequentially access all of the columns for a particular row address by toggling the $\overline{\mathrm{CAS}}$ line. In serial mode, for example, a controller can access 512 bits in a 256 k -bit DRAM (arranged as a 512 -row $\times 512$-column array) by simply establishing a row address and toggling the $\overline{\text { CAS }}$ line 511 times (after the initial access).

## Some access-mode comparisons

In sum, your application will ultimately determine the access mode you choose. All the modes have advantages and disadvantages, and the tradeoffs they present are the familiar ones: performance vs cost and complexity. Page-mode access, for example, requires one row and a separate column address for each location in the DRAM, whereas nibble mode requires only one address and four $\overline{\mathrm{CAS}}$ strobes to access data. Therefore, nibble mode is faster than page mode for short, sequential read operations such as fetching 4 bytes of data for a 32 -bit CPU via an 8 -bit port. However, nibble mode requires a precharge period when the RAS line returns high after four successive reads.

Because page mode holds the $\overline{\text { RAS }}$ line low throughout the access period, it's well suited to long, uninterrupted data transfers. Although nibble mode may be faster than page mode for long data transfers, when the DRAM controller employs nibble mode it must supply a new set of addresses on every fourth transfer. In addition, page mode can randomly access the columns within a row, whereas nibble-mode access is sequential.

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Static-column mode offers all of the speed advantages of nibble mode and also provides the randomaccess capability of page mode. Although static-column mode is more difficult to implement, it's rapidly becoming the mode of choice for high-speed memory systems.

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# Antialiasing filters reduce errors in $\mathrm{A} / \mathrm{D}$ converters 

The need for effective antialiasing filters closely matches the growing number of applications for $A / D$ converters. These filters reduce converter errors by limiting the input signal bandwidth. To correctly specify the filter, you need to consider the appropriate frequency band and the filter's characteristics.

## Robert W Steer Jr, Frequency Devices Inc

The growing number of applications for analog-todigital converters (ADCs) in data-acquisition systems, image processing, and industrial controls is driving the need for antialiasing filters that reduce errors in many converter-based systems. By limiting the bandwidth of a converter's input signal, antialiasing filters inhibit the generation of false (aliased), low-frequency signals caused by too low a sampling rate ( $\mathrm{f}_{\mathrm{sr}}$ ).

Limiting the converter's input-signal bandwidth reduces the highest frequency $\left(\mathrm{f}_{\mathrm{m}}\right)$ whose amplitude is greater than or equal to the weight of an LSB (least significant bit). Lowering $f_{m}$ reduces the rate at which the ADC must sample the input signal to avoid aliasing errors or at least to limit them to an acceptable level. Putting a value on the term "acceptable" requires a
knowledge of the specific application and of sampling theory. (See box, "Sampling theory sets inviolable limits.") A converter whose sampling rate is finite may be capable of error-free conversions, but if you present such an ADC with an improperly band-limited input signal, the output will contain aliasing errors.

## Prefiltering lets a slower ADC do the job

At first glance, a faster A/D converter might appear to provide an obvious and immediate answer to the aliasing problem. However, if you can't accept lower resolution, you'll have to pay more for a faster ADC. Furthermore, regardless of how much you are willing to pay for a converter, you can't get one with unlimited speed or resolution. In addition, noise frequencies extend well beyond the sampling rate of present-day ADCs. The sampling-rate requirements imposed by broadband noise are important because aliased highfrequency noise components can "fold back" and appear as lower frequencies that you can't distinguish from valid sampled data. Moreover, the system itself can generate "spurs"-spurious high-frequency signals, which will introduce errors if aliased.

By precisely limiting the bandwidth at the input of the ADC, active lowpass filters can reduce the need for brute-force increases in conversion speed. The restricted bandwidth lowers the maximum frequency of signals and noise that reach the ADC's input, and hence reduces the sampling (conversion) rate needed to avoid aliasing. Lowpass filters can exhibit a virtually flat, non-attenuating passband response that extends from
dc to the cutoff frequency $f_{r}$. Beyond $f_{r}$, the gain can roll off steeply at rates that exceed -90 dB per octave. However, for technical as well as economic reasons, a filter with a flat passband response and the steepest available stopband roll-off characteristic isn't necessarily the best choice for a particular application.

By band limiting the ADC input, a prefilter (Fig 1), prevents the ADC from digitizing alias-producing signals. A properly chosen filter attenuates signal components at frequencies greater than $f_{m}$ to levels well below the quantizing threshold of the ADC. (Here $\mathrm{f}_{\mathrm{m}} \leq \mathrm{f}_{\mathrm{sr}} / 2$.) A binary-coded n -bit A/D converter digitizes

## Sampling theory sets inviolable limits

Signal sampling, such as that occurring during $\mathrm{A} / \mathrm{D}$ conversion, can generate lower frequency, inband error signals when the sampled signal contains higher frequency components at or above half the sampling frequency, that is, above $\mathrm{f}_{\mathrm{sl}} / 2$. Fig A illustrates the alias that would result from a single-frequency sine wave sampled at too low a rate.

The sampling theorem, which deals with sampling at a theoretical, mathematical level, states that a signal sampled at a rate, $\mathrm{f}_{\mathrm{sr}}$, equal to or greater than twice the maximum signal-frequency component, $\mathrm{f}_{\mathrm{m}}$, can be exactly reconstructed from the data samples. If frequency components greater than $f_{s k} / 2$ are present, they "fold back"into the 0 -to- $\mathrm{f}_{\mathrm{m}}$ frequency band. Fig B illustrates a simple graphical derivation of the folding frequency ( $f_{f}=f_{m} / 2$ ). Above $f_{f}$, aliasing commences as
the first harmonic spectrum begins folding over into the original spectrum.

Conversely, sampling rates less than $2 \mathrm{f}_{\mathrm{m}}$ introduce aliases in the sampled signal that begin at $\mathrm{f}_{\mathrm{sr}}-\mathrm{f}_{\mathrm{m}}$ and range about each harmonic of $\mathrm{f}_{\mathrm{sr}}$, extending to $\mathrm{nf}_{\mathrm{sr}} \pm \mathrm{f}_{\mathrm{m}}$. (Here, n equals the harmonic number.) Because you can't distinguish the aliases from the valid data sharing the de-to- $\mathrm{f}_{\mathrm{m}}$ passband, accurate retrieval of the original signal is impossible. In real-world situations, the input signals are usually nonsinusoidal, are often random, and always contain noise. The noise, randomness, and high-frequency components of such signals are all potential sources of aliasing.

The elimination of frequency components above $f_{s r}-f_{m}$ requires a lowpass filter-usually one with sharp cutoff characteristics. With zero attenuation in its
passband and infinitely sharp and deep attenuation beyond, the ideal filter of Fig Ca completely eliminates aliasing and passes all desired signals unattenuated. However, this ideal filter is not attainable. Fortunately, various filter designs approach this ideal closely enough to achieve control of aliasing.

The response of the real-world filter in $\mathbf{F i g} \mathbf{C b}$ more nearly represents the response of an actual, realizable antialiasing filter. The finite roll-off and attenuation floor allow higher frequency signal and noise components to arrive at the sampler input. In some cases, these components can cause aliasing. The quantizing threshold of the sampler-an A/D converter for purposes of this discussion-determines whether these signals will be digitized.


Fig A-Insufficient sampling can produce a false lower frequency, in-band signal (an alias).


Fig B-Frequency folding (aliasing) sets in when too low a sampling rate causes fundamental frequencies and harmonic spectra to overlap.
its analog input into $2^{n}$ discrete levels, with the nth or least-significant bit being the smallest resolvable level. The LSB has a weight of $1 / 2^{\mathrm{n}}$ of the full-scale input voltage range and each higher order bit carries twice the weight of its lower order neighbor.
An ADC with a unipolar input range generates $2^{n}$
output codes as you vary the input from 0 V to the full-scale voltage, $\mathrm{V}_{\mathrm{fs}}$. Ideally, the midpoint of each input increment occurs at an exact integer multiple of $\mathrm{V}_{\mathrm{fs}} / 2^{\mathrm{n}}$, and each output transition occurs at the exact midpoint of a given analog increment, or at a multiple of $\mathrm{V}_{\mathrm{fs}} / 2^{\mathrm{n}+1}$. Table 1 shows that the LSB threshold of a


Fig C-An ideal filter (a) removes all frequencies beyond its stopband edge. A real-world filter (b) can approach this ideal of infinitely sharp cutoff.

The role of an antialiasing prefilter is to minimize $A D C$ errors by attenuating highfrequency signals before they reach the $A D C$.


Fig 1-The prefilter limits the bandwidth to the $A / D$ converter's input to prevent digitizing signals above $2 f_{s r}$, which might become aliases.

10-bit ADC is 66 dB below $\mathrm{V}_{\mathrm{fs}}$, which corresponds to $\mathrm{V}_{\mathrm{fs}} / 2048$. Theoretically, the ADC will not digitize any signal below this level.

## The bandwidth-limited A/D converter

Determining the bandwidth limit to use with an ADC to achieve acceptable amounts of aliasing can be difficult because the signal and noise waveforms encountered in practice contain numerous frequency components with complex amplitude and phase relationships. These frequency components can combine in ways that conceal individual components, particularly those with higher frequencies.

Fortunately, many rules of thumb provide first-pass approximations of the required prefilter cutoff frequency for a given type of input signal. Some of these rules appear in Table 2. You should use these approximations only as starting points.

A perfect antialiasing filter simply does not exist no matter how you synthesize it. Indeed, even in theory, you cannot create a perfect lowpass filter; that is, one that has no passband attenuation, that has no passband phase shift (or whose passband phase shift varies

| TABLE 1-LSB WEIGHT VS FILTER ATTENUATION FOR A BINARY-CODED ADC |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| RESOLUTION OF BINARY-CODED A/D CONVERTER |  |  |  | DESIRED FILTER RESPONSE |
| A/D RESOLUTION (BITS) | $\begin{array}{\|c\|} \hline \text { LSB } \\ \text { WEIGHT } \\ 1 / 2 n \\ \hline \end{array}$ | APPRROXIMATE LSB WEIGHT | $\begin{array}{\|c\|} \hline 1 / 2 \text { LSB } \\ \text { WEIGHT } \\ \left(1 / 22^{n+1}\right) \\ \hline \end{array}$ | ATTENUATION AT ${ }^{f} \mathrm{~m}$ |
| 8 | 1/256 | $-48 \mathrm{~dB}$ | $-54 \mathrm{~dB}$ | $\geq-54 \mathrm{~dB}$ |
| 10 | 1/1024 | $-60 \mathrm{~dB}$ | $-66 \mathrm{~dB}$ | $\geq-66 \mathrm{~dB}$ |
| 12 | 1/4096 | $-72 \mathrm{~dB}$ | $-78 \mathrm{~dB}$ | $\geq-78 \mathrm{~dB}$ |
| 14 | 1/16,384 | $-84 \mathrm{~dB}$ | $-90 \mathrm{~dB}$ | $\geq-90 \mathrm{~dB}$ |

linearly with frequency), and whose stopband attenuation is infinite. What's more, the assumption of a sampling rate that exceeds all signal and noise frequencies rarely holds true in practice. Noise can attain frequencies higher than half of the conversion rate of any realizable ADC or other type of sampler.

In addition, all realizable filters require a brief (but finite) frequency span to reach a deep attenuation floor. Moreover, these filters can superimpose small amounts of noise and distortion on the signals they condition, and can thereby produce aliases. The practical prefilter fulfills its task in two ways: It reduces out-of-band alias-producing signals to less than the quantization threshold of the ADC, and it restricts the bandwidth of the ADC's input signal without introducing unacceptable distortion.

Fig 2 focuses on the passband and the stopband edge of four popular, realizable active filter designs. The filters' characteristics are discussed in detail further on. The passband is the range of frequencies over which the filter exhibits flattest gain and imposes least attenuation, typically 0 dB at and near dc . The passband of lowpass filters extends from dc to the stopband edge-the transition point where filter attenuation first increases sharply for a small frequency increase.

You can define the stopband edge and the passband
TABLE 2-APPROXIMATIONS OF PREFILTER CUTOFF FREQUENCY FOR VARIOUS INPUT WAVEFORMS

| INPUT SIGNAL | PREFILTER CUTOFF <br> FREQUENCY $\left(f_{c} \leq f_{m}\right)$ |
| :--- | :--- |
| PULSATING DC | RATE OF CHANGE (VISEC)//V |
| SINUSOIDAL | 1/PERIOD |
| COMPLEX PERIODIC | 20/FUNDAMENTAL PERIOD |
| SINGLE EVENTS | $1 /$ PULSE WIDTH |

ripple to comply with system accuracy requirements. (Passband ripple is the peak-to-peak variation in a filter's passband frequency response.) One popular method locates the stopband edge at the break (corner) frequency, $f_{c}$, where attenuation first becomes 3 dB that is, where, for a constant input amplitude, the filter's output amplitude is $70.7 \%$ of its amplitude at very low frequencies. In commercial filters, passband ripple usually exhibits typical values of $0.2,0.5$, or 1 dB. To allow comparison of filter types, Fig 2 normalizes the four filter responses to coincide at $\mathrm{f}_{\mathrm{c}}$.

An alternative method locates the filter's stopband edge at the passband ripple frequency $f_{r}$, the highest frequency at which the passband ripple remains within
the filter's passband-ripple (passband response flatness) specification. Applicable to curves 3 and 4 of Fig 2, this approach yields a narrower-but much flatterpassband than does the $3-\mathrm{dB}$ method. To repeat, you can locate the stopband-edge frequency at an attenuation level dictated by system tolerances.

Fig 3 views the responses of Fig 2 over a wider bandwidth to allow a comparison of filter roll-off characteristics and the definition of two key frequencies for curve 4 . For antialiasing applications, $f_{a}$, the frequency at which attenuation first becomes $6(n+1) d B$, is the next highest frequency of interest; n is the ADC resolution in bits. The final and highest frequency, $\mathrm{f}_{\mathrm{s}}$, the attenuation-floor frequency, locates the lowest fre-


Fig 2-The passband and stopband-edge characteristics of the four filter types differ greatly. The curves are normalized to -3 dB and are shown in an expanded view of the passband region.

In theory, you can exactly reconstruct a signal sampled at twice its maximum signal frequency.
quency at which the stopband response drops below a specified attenuation floor and remains there. The floor defines the minimum attenuation a filter imposes at and beyond $\mathrm{f}_{\mathrm{s}}$.

Three additional parameters can simplify filter selection. Bounded by stopband edge-frequency $f_{r}$ or $f_{c}$ and by $f_{s}$, the transition band, $\beta_{t}$, is, depending on the application, the range from $f_{s}$ to $f_{r}$ or from $f_{s}$ to $f_{c}$. This parameter measures the frequency span required to reach the attenuation floor. A narrower transition band provides faster roll-off and sharper, better-defined frequency discrimination.

The shape factor, $\Omega_{\mathrm{s}}$, is the ratio of the attenuationfloor frequency, $f_{s}$, to either $f_{r}$ or $f_{c}$ (In equation form,
$\Omega_{s}=f_{s} / f_{r}$ or $\Omega_{s}=f_{s} / f_{c}$.) Shape factor, which provides the designer with a scale factor, is a useful figure of merit for comparing filters and is another measure of a filter's attenuation steepness or roll-off rate.

A lowpass filter is said to be monotonic within a specified frequency band when its attenuation beyond the stopband edge increases with increasing frequency. Curves 1, 2, and 3 of Fig 3 illustrate monotonic responses. Curve 4 shows a nonmonotonic response. Illustrating this relationship, Table 3 tabulates the shape factor of each filter, based on the ratio of the frequencies occurring at -80 and $-3 \mathrm{~dB}\left(\Omega_{\mathrm{s}}=\mathrm{f}_{-80} / \mathrm{f}_{-3 \mathrm{~dB}}\right)$. The table includes comments about comparative behavior beyond the stopband edge.


Fig 3-The unique roll-off characteristics of each filter type determine the transition bandwidth as well as the shape and depth of the attenuation floor. Normalized to $-3 d B$, the curves are shown in a broadband view.

Table 3 shows that the Cauer elliptic filter (curve 4) rolls off fastest, the Chebyshev filter (curve 3) second fastest, the Butterworth filter (curve 2) third fastest, and the Bessel filter (curve 1) slowest. However, the attenuation of the Cauer elliptic filter is not monotonic because it varies in a cusp-like manner at frequencies above $\mathrm{f}_{\mathrm{s}}$. Note, however, that the 7 -pole, 6 -zero, elliptic filter rolls off faster than its 8 -pole monotonic companions.
In theory, the attenuation shown in the first three curves increases without limit as frequency increases, but the Cauer elliptic filter exhibits a finite attenuation floor. As shown later, the Bessel filter fills an important need, and the Cauer elliptic filter's exchange of
attenuation depth for faster roll-off is a worthwhile tradeoff for certain applications. Playing a key role in determining system bandwidth, transient response, and accuracy, the width and flatness of the $\mathrm{A} / \mathrm{D}$ converter's prefilter passband warrants a closer look. Fig 4 displays the same four curves normalized to their $-80-\mathrm{dB}$ frequencies.

With all filters normalized to -80 dB at the attenu-ation-floor frequency, $\mathrm{f}_{\mathrm{s}}$, Table 4 lists the passband of each filter and compares the ratio of the Cauer elliptic filter's passband to that of each of the remaining filters at both the $-0.1-\mathrm{dB}$ and the $-3-\mathrm{dB}$ corner frequencies. The choice of these corner frequencies was arbitrary, based on the assumed requirement for passband


Fig 4-A broadband view normalized to a common - $80 \mathbf{d B}$ attenuation floor more clearly illustrates the transition-band behavior of the four filter types.

The phase of a Bessel filter varies linearly with frequency within a ripple-free passband and delays passband frequencies by a constant amount of time.
amplitude ripple of 0.1 dB and 3 dB .
This table shows that the Cauer elliptic filter provides a $0.1-\mathrm{dB}$ passband approximately 12 times as wide as the Bessel filter's, five times as wide as the Butterworth filter's, and 1.5 times as wide as the Chebyshev filter's.
For a $-3-\mathrm{dB}$ corner, Table 4 shows that the width of the Cauer elliptic filter's passband is approximately four times that of the Bessel's, twice that of the Butterworth's, and 1.5 times that of the Chebyshev's. These ratios lead to the obvious conclusion that the Cauer elliptic filter surpasses the other designs for amplitudecritical applications.
Though carefully controlled frequency response is important in some situations, many applications require the prefilter to transmit pulses faithfully, with little or no distortion. To achieve pulse fidelity, the filter must combine the linear phase response typical of the Bessel filter and the flat amplitude response of the Cauer elliptic, Butterworth, or Chebyshev filters. Although a linear-phase filter maintains the proper phase relationship among the frequency components of a pulse, such a filter exhibits a gain roll-off in the passband that can modify the amplitude relationship among the frequency components and prevent the filter from producing an output that faithfully reflects its input.
Moreover, at frequencies at and beyond the stopband edge, the response of linear-phase filters rolls off more gradually than does that of their amplitude-oriented counterparts. The resulting wider transition band degrades frequency discrimination by allowing higherfrequency, out-of-band, alias-producing signals to reach the ADC's input.

Many compromise or "transitional" responses combine amplitude and phase or delay characteristics to meet specific requirements. Classical responses include those of Butterworth/Bessel, Paynter, equirippledelay, parabolic, and Gaussian realizations. Fortunately, the previously discussed Bessel, Butterworth, Chebyshev, and Cauer elliptic designs serve most antialiasing applications well.

## Classical filter designs up close

It is now appropriate to define the unique characteristics of each type of filter with the goal of making the best choice for a given set of system requirements. The Bessel, Butterworth, Chebyshev, and Cauer elliptic responses of Figs 2 through 4 are so-called classical responses that meet the needs of most antialiasing ap-

| TABLE 3-COMPARISON OF TRANSITION BAND AND STOPBAND PERFORMANCE |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| CURVE |  | SHAPE FACTOR |  | L-OFF |
|  | FILTER TYPE | $\Omega_{S}(\mathrm{f}-80 \mathrm{~dB} / \mathrm{f}-3 \mathrm{~dB})$ | RATE | MONOTONIC |
| 1 | 8-POLE BESSEL | 6.068 | SLOWEST | YES |
| 2 | $\begin{gathered} \text { 8-POLE } \\ \text { BUTTERWORTH } \end{gathered}$ | 3.162 | FASTER | YES |
| 3 | 8 -POLE, 0.1-dB CHEBYSHEV | 2.183 | NEXT TO FASTEST | YES |
| 4 | 7-POLE, 6-ZERO, 0.1-dB CAUER | 1.661 | FASTEST | NO |

plications. The phase of the Bessel filter varies linearly with frequency within a ripple-free passband. This filter delays signals at passband frequencies by a constant amount of time. The linear-phase characteristic fulfills one requirement for faithful pulse reproduction, that of preserving the phase relationship among the frequency components that comprise the pulse. With appropriate attenuation characteristics, the Bessel filter produces a delayed (but accurate) replica of its input signal.

Linear phase and overshoot-free step response come at the expense of passband flatness and slower roll-off in the region of the -3 dB corner frequency, $\mathrm{f}_{\mathrm{c}}$. The more gradual roll-off results in band limiting that is less sharp, or selective, than that of other types of filters. The roll-off of the linear-phase filter is, however, monotonic and approaches the slope of the Butterworth and Chebyshev designs: $-6 \mathrm{n} \mathrm{dB} /$ octave at higher frequencies. (In this case, n is the number of filter poles.)

The Butterworth filter, also known as a maximally flat-magnitude filter, exhibits a wider and flatter passband than does a Bessel design of the same order (the same number of poles). Continuing the comparison, the Butterworth filter rolls off monotonically, and much more sharply at the $-3-\mathrm{dB}$ corner frequency, $\mathrm{f}_{\mathrm{e}}$, than does the Bessel design. In exchange for sharper bandlimiting, the Butterworth filter's phase varies nonlinearly with frequency; the delay is no longer constant, and the step response exhibits a moderate amount of overshoot. These characteristics present no problems for amplitude-based applications.

The Chebyshev filter exchanges the flat, ripple-free passband characteristic of the Butterworth filter for an even sharper roll-off rate at the stopband-edge frequency, $\mathrm{f}_{\mathrm{r}}$. This design exhibits equal-amplitude ripple across the passband and a step response with even

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In real-world situations, the input signals
are usually nonsinusoidal, are often ran-
dom, and always contain noise.
more overshoot than that of the Butterworth design. In addition, passband delay is not constant-it increases with frequency. Again, the frequency-dependent delay is usually not a problem when you are primarily interested in the attenuation characteristics.

The Cauer elliptic active lowpass filter has the wide, nearly flat passband response and the extremely sharp roll-off characteristics that ideally suit amplitude-based antialiasing applications. This design exhibits equalamplitude ripple in the passband (typically 0.1 dB ) and extremely fast amplitude roll-off. (Equal-amplitude ripple means that there are several peaks and valleys in the passband amplitude response and that the ratio of the response magnitude at the maxima and minima is constant over all maxima and minima.) Compared with the preceding filter types, which can theoretically roll off without limit, the Cauer filter rolls off to a deep, finite, well-defined attenuation floor.

Transitional filters combine selected characteristics of classical responses to achieve specific band-shaping tasks. One practical example (Fig 5) combines the Bessel filter's linear-phase passband response with the Butterworth filter's sharper stopband roll-off. Many other combinations exist.

Without violating other system performance criteria, the correct antialiasing filter provides the passband, transition-band, and attenuation-floor characteristics required to adequately prefilter the signals supplied to an n -bit ADC. Alias prevention defines the transi-tion-band and attenuation-floor requirements; system
tolerances determine the required flatness of the passband.
System specifications define both the maximum allowable magnitude of passband ripple and the stopband edge frequency, $f_{c}$ or $f_{r}$. The stopband edge frequency defines the high-frequency limit of the passband and marks the beginning of the transition band.

To determine the type of filter required by a particular application, you must next deal with the following parameters simultaneously:

1. The number of bits, $n$, of the $A / D$ converter.
2. The sampling rate of the $A / D$ system, $f_{\mathrm{sr}}=\left(1 / \mathrm{t}_{\mathrm{sr}}\right)$, where $t_{s r}$ corresponds to the time from the start of one conversion to the start of the next one. This time interval, of course, depends on the ADC's conversion time, but it can also depend on other system parameters. Within the time interval, a successive-approximation ADC compares its analog input to the weighting of each bit and delivers an $n$-bit digital output that corresponds to the input's value at the time of sampling. This parameter affects both the conversion accuracy and the system's susceptibility to aliasing.

If no sample-and-hold circuit precedes the ADC , the duration of the A/D conversions must be short compared with the time required for the input signal to change by $1 / 2$ LSB. In essence, when there is no $\mathrm{S} / \mathrm{H}$ circuit, the sampling "window" of a successiveapproximation converter is the same as the duration of a conversion. With a given value of $\mathrm{f}_{\mathrm{sr}}$, an $\mathrm{S} / \mathrm{H}$ circuit at the ADC input dramatically shortens the sampling

| TABLE 4-COMPARISON OF THE PASSBAND AND ATTENUATION-FLOOR SHAPE OF THE FILTERS |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| RESPONSE CURVES |  | $\begin{array}{r} \text { STOPBA } \\ \text { AT } \\ -0.1 \text { AND }-3 \mathrm{~dB} \\ \hline \end{array}$ | EDGE (SE) ratio cauer se TO OTHER CURVES | PASSBAND/ ATTENUATION FLOOR |
| CURVE | RESPONSETYPE |  | CAUER/CURVES $1,2,3$ ( $\mathrm{F}_{\mathrm{r} 4} / \mathrm{f}_{\mathrm{rm}}$ ) |  |
|  |  | $\begin{aligned} & f_{c}\left(=f_{s} / R_{S}\right) A T \\ & -3 \mathrm{~dB}, \mathrm{f}_{\mathrm{s}}=1 \end{aligned}$ | CAUERICURVES $\left(\mathrm{f}_{\mathrm{c}} 4^{\prime} \mathrm{cn}\right)$ | COMments |
| 1 | BESSEL 8-POLE | $\mathrm{trra}^{\text {c }}$ 0.0506 | 11.9 AT -0.1 dB | NARROWEST/ THEORETICALLY UNLIMITED |
|  |  | $\mathrm{f}_{\mathrm{c} 1}=0.1648$ | 3.9 AT -3 dB |  |
| 2 | BUTTERWORTH 8-POLE | $\mathrm{f}_{\mathrm{r}}=0.1283$ | 4.7 AT -0.1 dB | WIDER/ THEORETICALLY UNLIMITED |
|  |  | ${ }_{\mathrm{c} 22}=0.3163$ | 2.0 AT -3 dB |  |
| 3 | 0.1-dB RIPPLE CHEBYSHEV 8 -POLE | $\mathrm{f}_{\mathrm{r} 3}=0.430$ | 1.4 AT -0.1 dB | NEXT WIDEST/ THEORETICALLY UNLIMITED |
|  |  | ${ }^{\mathrm{f}} \mathrm{CS}=0.4581$ | 1.4 AT -3 dB |  |
| 4 | 0.1-dB RIPPLE 7-POLE, 6-ZERO | $\mathrm{f}_{\mathrm{r} 4}=0.6020$ | 1.0 AT -0.1 dB | WIDEST/CUSP-LIKE WITH FIXED MINIMUM value |
|  |  | ${ }^{\mathrm{f}} \mathrm{c} 4=0.6339$ | 1.0 AT -3 dB |  |



The Butterworth filter exhibits a sharp, monotonic roll-off at the -3 dB corner frequency, but its phase varies nonlinearly with frequency.
window and allows conversion of signals having much higher rates of change and much higher frequency content.

For alias-free conversion, the sampling rate, $\mathrm{f}_{\mathrm{sr}}$, must exceed the highest in-band (passband) frequency, $f_{m}$, by no less than a factor of two: $\mathrm{f}_{\mathrm{sr}} \geq 2 \mathrm{f}_{\mathrm{m}}$. This equation relates the ADC's sampling rate to the maximum frequency present in the ADC's input signal at an amplitude greater than or equal to $1 / 2$ LSB.
3. A frequency span closely related to the transition band described earlier. The frequency band of interest in this case is that required for the filter's attenuation to increase from the value at the stopband edge to a value that attenuates signals above $f_{m}$ to less than $1 / 2$

LSB. Signals at frequencies above this band cannot produce aliases because, when they arrive at the ADC input, their amplitudes are too small.

Table 1 furnishes the values of the first parameter, the fractional and decibel ( dB ) weighting of $1 / 2 \mathrm{LSB}$ of an $n$-bit ADC. The right-hand column lists the attenuation required to reduce a signal at $\mathrm{f}_{\mathrm{m}}$ to below the ADC's threshold and, at the same time, defines the high-frequency bound of the transition band.

The value of the maximum frequency of interest, $f_{m}$, influences the value of the second parameter, $\mathrm{t}_{\mathrm{sr}}$ and its frequency equivalent, $\mathrm{f}_{\mathrm{sr}}$. When selecting $\mathrm{f}_{\mathrm{sr}}$, you may discover that you must choose between using a faster ADC and a prefilter-and you may actually need


Fig 5-This transitional filter approximates the linear phase (constant delay) of the Bessel response in the passband, combined with the sharper roll-off of the Butterworth filter beyond the passband.

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The Cauer elliptic filter has a flat passband and extremely sharp roll-off characteristics that suit amplitude-based, antialiasing applications.
both. If you add a prefilter, you may find that it slows the system response significantly; the system's response can become essentially the same as that of the prefilter. To make an intelligent selection of a conversion rate and a prefilter response, you must determine the highest signal frequency that's important to the system's operation. The ADC must sample at a rate equivalent to at least twice this frequency. You must also determine the amplitude of unwanted and potentially alias-producing artifacts (both signal components and noise) present in the system, and you must select a filter that attenuates the artifacts to a value no greater than one-half that of the ADC's LSB.

The third parameter is, in effect, the shape factor $\Omega_{\mathrm{s}} . \Omega_{\mathrm{s}}$ is equal to the attenuation-floor frequency di-
vided by the stopband-edge frequency. For the curves of Fig 3, the equation you use to obtain the shape factor is: $\Omega_{\mathrm{s}}=\mathrm{f}_{-80} / \mathrm{f}_{-3}$. Table 3 lists $\Omega_{\mathrm{s}}$ for the actual filter realizations discussed.

You can now select a filter type. Selection begins by comparing your requirements with the transitionband response of the devices listed in this table. Obviously, the linear-phase, 8 -pole Bessel filter exhibits the slowest roll-off rate and is best suited to applications requiring faithful pulse reproduction. Knowing the transition band and the tolerance on passband flatness, you can now select the filter type that best meets the system requirements.

Note that the 7 -pole, 6 -zero Cauer elliptic filter rolls off faster than its 8-pole cousins and yields the widest


Fig 6-Sampling imposes a $\sin (x) / x$ response on the sampled signal. Accurate reconstruction requires compensation for this effect.


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## The Cauer filter rolls off to a deep, finite,

 well-defined attenuation floor.passband. The Cauer filter's response suits applications requiring fast roll-off and the widest possible alias-free passband. The need for this type of filter grows as $f_{s \mathrm{sl}} / f_{m}$ approaches two.

Table 4 compares the passband of the four responses, normalized to -80 dB , and provides a figure of merit for amplitude response. With reference to the 0.1 - and $3-\mathrm{dB}$ stopband-edge frequencies, this table lists the ratio of the Cauer elliptic filter's passband to the passbands of the Bessel, Butterworth, and Chebyshev filters.

## An example is useful

To illustrate a typical design approach, consider the definition of a prefilter for use with a 12 -bit A/D conversion system that must digitize signals to 20 kHz without aliasing. The passband must extend from dc to 10 kHz and must exhibit no more than 0.1 dB of ripple.

Alias-free operation requires the attenuation of signals at and above the $f_{m}$ of 20 kHz by no less than $6(\mathrm{n}+1) \mathrm{dB}=6(12+1) \mathrm{dB}=78 \mathrm{~dB}$. The applicable filter parameters include a stopband-edge frequency, $\mathrm{f}_{\mathrm{r}}$, of 10 kHz , a passband ripple of 0.1 dB max, and a minimum attenuation floor of 78 dB at $\mathrm{f}_{\mathrm{s}}=20 \mathrm{kHz}$. The resulting shape factor is $\Omega_{\mathrm{s}}=\mathrm{f}_{-78} / \mathrm{f}_{-0.1}=20 \mathrm{kHz} / 10$ $\mathrm{kHz}=2$. The 7 -pole, 6 -zero Cauer filter easily meets these requirements.

The A/D converter must be able to sample at a minimum rate of $2 \mathrm{f}_{\mathrm{m}}$, or 40 kHz . This rate corresponds to a maximum A/D conversion time of $25 \mu \mathrm{sec}$, and a sampling window on the order of 10 nsec for 12 -bit accuracy.

## Other considerations

You should consider data reconstruction in the early phases of system design. Reconstruction is often necessary because the sampling rate and window modify a signal of frequency $f$ in the same way as does a lowpass filter with the $\sin (\mathrm{x}) / \mathrm{x}$ response shown in Fig 6. With $\mathrm{x}=\pi \mathrm{f} / \mathrm{f}_{\mathrm{ss}}$, and nulls occurring at $\mathrm{f}_{\mathrm{sr}}$ and its harmonics, the attenuation is equal to

$$
20 \log \left(\sin \left(\pi f / \mathrm{f}_{\mathrm{sr}}\right)\right) /\left(\pi \mathrm{f} / \mathrm{f}_{\mathrm{sr}}\right) .
$$

Thus, at $\mathrm{f}_{\mathrm{sr}}=4 \mathrm{f}$, the attenuation is

$$
20 \log (\sin (\pi / 4) /(\pi / 4))=0.9 \mathrm{~dB} .
$$

Accurate reconstruction requires compensation for the losses caused by this effect. There are many recovery mechanisms, including the zero-order hold (a
clocked digital-to-analog converter) and lowpass filters of various orders and complexity. All of these filters have the task of filling in the steps of the sampled waveform to smoothly replicate the original.

Certain filter parameters warrant attention. First, you must take care to ensure that the prefilter exhibits low distortion. The harmonics generated by a filter suffering from amplitude or rate limiting are likely sources of alias errors. You must therefore observe all of your chosen filter's specified restrictions on output loading and such signal characteristics as peak voltage and slew rate.

Then, because noise contributes to aliasing and also degrades system sensitivity and dynamic range, you need to know how much noise your filter can produce. Fortunately, present-day lowpass active filters exhibit noise performance suitable for most applications.

Next, you should consider such filter parameters as input impedance, output impedance, and the initial value and temperature coefficient of the filter's and ADC's input offset voltages. Changes in the first two quantities can produce system gain variations. The others can cause dc baseline shifts.

A final consideration concerns the reproducibility of your product. You should know or determine how closely you or the filter vendor can match the characteristics of supposedly identical filters. With this knowledge, you can ensure compliance with system specifications in both single and multichannel configurations.

EDN

## Reference

Vandoren, A, Data Acquisition Systems, 1982, PrenticeHall, Englewood Cliffs, NJ, pgs 27 and 29. Figs A, B, and C(a) reprinted with permission of Prentice-Hall.

## Author's biography

Bob Steer is president and treasurer of Frequency Devices Inc in Haverhill MA-but those are only his official titles. In his 20 years at the company, he has always been active as a design engineer. He holds a BSEE from Merrimac College and MS and ScD degrees from MIT. Prior to founding Frequency Devices, he held positions in academia as an associate professor and as chairman of an EE department. Bob's hobbies include boating and cycling.

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|  | CU2015SCPB-L | $1 \times 20$ | 15.1 | P | X |
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ELECTRONIC NONSENSE FOR ENGINEERS AND ENGINEERING MANAGERS



It's a sad fact that engineering schools give short shrift to the social graces. Yet, in your career, you're faced with the necessity of dealing with people, many of them highfalutin. This column, therefore, will give you the rudiments of etiquette, both to spare you embarrassment and to increase the likelihood of your keeping your job. This month, we'll explore how to act in a fancy restaurant.

1. Upon entering, show no signs of being impressed. Statements like, "Gosh, this is a beautiful, fancy place" are a no-no. Just raise your eyelids slightly and say something like, "Hmm-looks as though my decorator's been here."
2. Always carry a flashlight and a pair of scissors with you. Americans think dark restaurants are classy, so it's likely you won't be able to read the menu by the light of the small candle on the table. Using the scissors, cut out the price column from the menu. That way, the person you're with won't think you're price conscious. And never ask for a translation of items printed in French. Nod your head knowingly and order at random.
3. When you taste the wine the sommelier (wine steward)
brings, chew it a while, then spit it on the floor. Then, even though you have no idea how good or bad the wine is, say something like, "Hmm-an impish little wine" or "Hmm-it has an imposing character that stops just short of ostentation."
4. When you eat your meal, be ambidextrous. Switching the fork from hand to hand after cutting your meat reveals your roots.
5. Finally, if your waiter's name is Jacques or Pierre, impress him and your dining companion by using a little French. Here are three phrases that are sure to go over big. $\star$ Cette nourriture est abominable.
(set new-ree-tyur ett ah-bow-me-nah-bluh)
This food is delicious.
$\star$ Je pense que je vais vomir.
(zhe ponss kuh zhe vay voh-meer)
I think that I will return.
$\star$ Votre chef est un sacré imbécile. (voe-truh chef ett unh sah-cray em-bay-seal) Your chef is a real genius.

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President Bush has inherited the excruciatingly difficult task of reducing our country's $\$ 17$ zillion deficit. His " 1000 points of light" can only increase the debt-how much depends on the wattage of the lights. A plausible way to cut the deficit is to tax electronics end users who use circuits and systems that consume too much power, operate too fast, or use too many bits.

It's inarguable that our deficit is linked closely to our consumption of energy. Because we have 432 ready-to-go nuclear plants whose startups are blocked by picketers who yearn for a return to kerosene lamps, we must use fossil fuels to produce electricity, Ovshinsky notwithstanding. And because OPEC is poised to inflict another '70s-type punishment on us, we simply must reduce the power we consume. Some will say, "What's the problem? Now we have CMOS, so power consumption is going down." True. But what most people don't realize is that our supply of C is dwindling rapidly. There's still plenty of N in the hills, but NMOS has fallen out of favor. So we must import a high percentage of the C we use in making CMOS ICs-hardly a way to reduce the deficit.

The ever-increasing speed of modern systems is inextricably tied to the rising consumption of power. What's needed, then, is a tax system that penalizes excessive power consumption and its bosom buddy, high speed. I propose that President Bush issue guidelines on IC speed. For example, he could impose a limit on A/D-converter speed in the form of a maximum resolution-frequency product. In my opinion, $315 \mathrm{CM}(\operatorname{codes} \times \mathrm{MHz})$ is a reasonable figure. A 12-bit A/D converter, for instance, has 4096 codes. The 315-CM limit would restrict the converter's speed to 0.077 MHz , corresponding to a conversion time of $13 \mu \mathrm{sec}$.

Another factor tied to power consumption is bit count. The evolution of computer systems from 8 to 16 to 32 bits has been accompanied by significant increases in power consumption. The same is true for the everincreasing RAM capacities in modern computers. A side effect of this insatiable demand for more and more bits is bit pollution. A large portion of these zillions of bits goes unused, and so we have the problem of bit disposal and its resulting pollution. Land bitfills are becoming exhausted; bit incinerators use fossil fuels and pollute the atmosphere.

A presidential commission could determine a reasonable progressive tax on the number of bits in a system. Another source of revenue would be a tax on bit disposal. This disincentive would provide an impetus for developing trinary (base-3), quadrary (base-4) and quinary (Schweppes) computers, which use fewer bits to process a given amount of data. Some other ways to reduce the deficit:

- Sell Silicon Valley to the highest bidder
- Raise engineers' income taxes to $90 \%$ of gross income
- Eliminate all taxes on management personnel. Management deserves the credit for the healthy state of American electronics, despite engineers' blunders; eliminating taxes on these business geniuses will provide incentive for making companies healthier yet.
- Impose an application fee of $\$ 1,000,000$ per patent
- Restrict defense contractors' illegal overcharging to $20 \%$ of a contract's face value (unless the illegal overcharging is proven to be justified).


## COMPANY MARKFTS DATA-DFGRADATION SYSTEM

A new data-acquisition board, dubbed "BarfData," is available from Data Distortion Inc (Chesterfield, MA), a company that specializes in PC-based analog-signal degradation. The board features 16 poorly multiplexed analog-input channels, a signaldegrading instrumentation amplifier, a track-and-hold distorting amplifier, and a 12 -bit, nonlinear A/D converter. The input multiplexers are from the bottom of the barrel, and offer only $20-\mathrm{dB}$ channel-to-channel isolation and $1 \mathrm{M} \Omega$ each of on- and off-resistance. By the time a signal reaches the instrumentation amp, it's tainted by pollution from adjacent channels and severely attenuated by the multiplexers' high on-resistance. The instrumentation amp's specs are as repugnant as the multiplexers'; for example, gain accuracy is $\pm 48 \%$ and total harmonic distortion is -15 dB . The almost unrecognizable signal then goes to the track-and-hold amp, whose abominable pedestal, accuracy, and droop parameters introduce additional errors in the signal. Finally, the output A/D converter features nauseating differential and integral nonlinearity and misses at least 2011 of its 4096 codes. Explains Joe Signalicide, president of Data Distortion, "Any wimp can make a data-acquisition system whose output accurately represents the input codes; it's a real art form to take a perfectly pure input and turn it into a stench in the nostrils of the signalprocessing community."-Bill Travis

## FVERTYBODY ACQUIRFS FVGRYBODY

In a startling press conference on April 1, a spokesman from Insiders Inc, a Wall Street illegal-insider-information trader, announced that every electronics firm in the US has concluded a leveraged buyout of every other firm. According to Insiders' Boesan Ivesky, top-secret negotiations for the buyouts have been going on for the past three years. The ramifications of the buyouts are unclear at this moment; what's certain, however, is that every firm plans to fire every other firm's management team. The implications for design engineers in the acquir(ed)(ing) companies are equally unclear. Ivesky revealed, however, that the industry plans to adopt a free-agent system similar to the one used in professional sports. -Bill Travis

## IBM ANNOUNCES PS/1,000,000 SERIFS

Big Blue set the computer industry on its ear on April 1, when the firm announced its new, PS $/ 1,000,000$ Series of personal computers. Designed to prevent cloning, the family uses a bus architecture called TeraChannel-a 128-bit bus structure that's covered by 967 patents, 401 copyrights, and two Emmy awards. Additional clonethwarting measures include explosive cabinet bolts, an automatic videotape record of users, and a l-time user oath (with Bible) administered by the firm's authorized value-depleted resellers (VDRs). According to Mr Large Blue of IBM, Microhard is developing a PS/1,000,000-compatible operating system called OS/1,000,000. Immediately after IBM announced the series, a consortium of personal-computer manufacturers (led by Compaq) revealed plans for a counterattack. The firms plan to introduce a 256-bit, open-architecture system that uses Intel's new 8,000,986 microprocessor, a $250-\mathrm{GHz}$ IC that addresses $9,999,999,999,999,999$ Tbytes of memory.
-Bill Travis

# Avoid burned-out ICs . . . also, how much for trade secrets? 

## Dear Abbott:

I have this problem with CMOS logic ICs. Every time I wire up a breadboard, I end up with one or more burned-out ICs. I've tried fusing the power supply and bringing the voltage up gradually, but nothing seems to help. Do you have any idea what I'm doing wrong?
Worried, Santa Clara, CA

## Dear Santa:

Sure-you're not seasoning the CMOS ICs properly. It's a littleknown fact that these circuits require some "stroking" before you can use them in an application. The procedure is simple: Wear shoes with leather soles and scuff them about 20 times on a nylon rug. Then run a nylon comb through your hair about 10 times. Now you're ready to season the ICs. Just hold one row of pins against a ground plane and touch the other row (the row with the input pins) with your index finger. You should have no more problems.

## Dear Abbott:

I'm bewildered. First, we had the 150 V supplies for powering vac-uum-tube circuits. Then $\pm 15 \mathrm{~V}$ came along, and it seemed to be the ultimate solution. Now we have ICs that are powered from single 5 V supplies, and some say the voltage will drop even further, say to 3.3 V . What's your opinion about all these changes? Concerned in New Jersey

## Dear New:

Well, let's look at it from the standpoint of numerology. Consider the ratios of the successive powersupply voltage-span reductions150 V to 30 V , a ratio of $5 ; 30 \mathrm{~V}$ to 5 V , a ratio of 6 . Now hold on to

your hat. What's startling is that the ratio of 5 V to 3.3 V is 1.5151515 . . ., a never-ending number. Are you sitting down? There's more-it so happens that Ramus II, the father of astrological proctology, was born on May 6, 1515. If I were you, I'd run right out and play 5615 in the dailynumbers lottery.

## Dear Abbott:

My boss and I have this argument going. We have an application for a large number of extremely fast flip-flops. I want to use an ECL gate array, and my boss is set on using a GaAs array. Who do you
think is right? ECL Advocate, High Power, CA

Dear ECL:
You're both wrong. The 6SN7 dual triode makes the best flip-flop in the world. You and your boss have the same problem: You're hung up on the latest, trendiest technology, and you've lost sight of tried-and-proven techniques. Get off the fad bandwagon and take some time to smell the filaments.

## Dear Abbott:

I'm a circuit-design engineer in a defense-electronics firm, and I don't make enough money to make ends meet. The problem is, my wife likes Porsches, Perrier water, and expensive yuppie restaurants. So, I've begun selling some of our company's schematics to a bearded man named Boris. My question is, how do I determine how much to charge? Entrepreneur, Profit Motive, CA

## Dear Entrepreneur:

First, let's determine my share for not turning you in. I think $40 \%$ is equitable. The best way to set a price for stolen trade secrets is to charge by the IC count. That way, you'll have an incentive to maximize the number of ICs in the circuits you design. I feel $\$ 1000$ per IC package ( $\$ 10,000$ for gate arrays) is fair. You'll receive the number for my Swiss bank account in the mail.

Dear Abbott is pleased to answer questions from engineers who are either too dumb or too lazy to solve their own problems. Send selfaddressed stamped envelope and a blank, signed check.

# Use a negative capacitor for useful, banal applications 

## Bill Travis, Contributing Editor

It's been 21 years since this editor, employed as a bizarre-product development engineer at Sprague Electric Co (North Adams, MA), serendipitously invented the MinusCap (Ref 1). This component resembles an ordinary capacitor in every way, except that its value is negative (for example, $-1 \mu \mathrm{~F}$ ). Fig 1 shows the startling results of applying a step signal to a se-ries-RC integrator incorporating the MinusCap. Note that the output waveform has a negative time constant. This phenomenon is easy to explain-to preserve the negative exponent of $e$ in the expression $\mathrm{V}_{\text {out }}=\mathrm{V}_{\text {in }}\left(1-\mathrm{e}^{-\mathrm{trC}}\right)$, the time t assumes a negative value.
An interesting aspect of the output waveform in Fig 1 is the fact that two output voltages exist simultaneously. A useful, albeit banal, application comes to mind. If you connect a lowpass and highpass de-voltage filter to the output and buffer the outputs of the filters, you obtain a dual-voltage power supply. For example, assume the lower output voltage in Fig 1 is 5 V and the upper one is 15 V . A 5 V lowpass dc filter with reasonably steep skirts will, for all intents and purposes, completely attenuate the 15 V signal and pass the 5 V level. And vice-versa for the 15 V highpass de filter.
Some applications suggested in Ref 1 include predictions of future noise spikes, scope probes with zero shunt capacitance (made by connecting an equal-value

MinusCap in parallel with the probe's positive capacitance), and observations of future failures. The promise of a rosy future for the component, however, never bore fruit. The Department of Defense (DoD) seized all lab samples and notes, and put the material in the same storage facility that's housed the Lost Ark (Ref 2) since 1939 .

Because of the USSR's development this year of the negative inductor and the imaginary resistor, the DoD


Fig 1-This scope photo depicts the input and output waveforms of the $-1-\mu F$ MinusCap; pay no attention to the phospher burn marks.


Fig 2-It's up to you to figure out any useful applications for the MinusCap.
no longer considers the MinusCap to be a threat to national security. Development of paper, ceramic, and electrolytic negative capacitors is now underway at several manufacturers' facilities. At the mammoth EDN test lab, for example, this editor recently constructed some units that exhibit a $-1-\mu \mathrm{F}$ value and effective series resistance of $-0.1 \Omega$.
Fig 2a shows a delay line constructed with $25-\mathrm{mH}$ positive inductors and the $-1-\mu$ F MinusCaps. In Fig $\mathbf{2 b}$, you see the results of applying a 10 V step to the input of the line. The output step appears 3 msec before the application of the input. As seen in Fig 2c, the same results accrue when you apply a sinusoidal input to the input of the delay line (actually, the anticipation line)-the sinusoidal output appears at the output 3 msec before the application of the input. It's up to you to determine useful applications for such anticipation lines. One possibility is to detect changes in system logic states before they occur.

One final application possibility, one the DoD is studying very carefully, is in imaginary-frequency transmitters. The expression

$$
f=\frac{1}{2 \pi \sqrt{L C}}
$$

gives the frequency determined by an LC tank in an oscillator. If the value of C in the expression is negative, then the resulting frequency is, naturally,

$$
f=-j \frac{1}{2 \pi \sqrt{L|C|}}
$$

The reason for the DoD's interest in such imaginaryfrequency transmitters is the fact that their signals are detectable only by imaginary receivers, such as those the $\mathrm{D}_{0} \mathrm{D}$ often receives under defense contracts.

## References

1. Travis, W J, "The negative capacitor: A challenging new component," EEE, September 1968.
2. Jones, Indiana, "Discovery of the Lost Ark of the Covenant," Journal of Mythical Artifacts, July 1939.

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## ABERRANT DESIGN IDEAS

## Gausser/degausser brightens color monitors

## Ted Burton <br> Signetics

A small permanent magnet (the gausser), held in close proximity to the face of an operating color monitor, will produce a striking display of colorful patterns (Fig 1). Much to the chagrin of the gausser user, though, the colorful patterns turn into permanent color clouds when the gausser is removed.

Luckily for the gausser user, whose job might now be in jeopardy, it's easy to build a degausser from a $1000-\mathrm{ft}$ roll of 30 -gauge wire-wrapped wire. This degausser is not UL approved, it erases any magnetic medium within a foot or two, it uses potentially lethal


Fig 1-A simple magnet can really liven up your color monitor.
voltages, it interferes with pacemaker operation, and it probably causes cancer or hair loss in laboratory rodents. However, it also removes the cited color clouds.

Fig 2 shows how to build the degausser and turn it on by sticking its two leads into an ac outlet. You should sweep the powered-up degausser past the face of the monitor for several seconds, then turn it off by pulling the leads out of the ac outlet. If the degausser is left running longer than a minute, the degausser and its operator will most likely start to smoke or burn. (Ed Note: The thought occurred to this editor: Why use the gausser in the first place? But that's picayипе.)

EDN


Fig 2-In addition to killing innocent lab animals, this degausser gets rid of the colorful patterns on your monitor.

# Exploit Z80's hidden logarithmic mode 

Jim Williams<br>Linear Technology Corp

The popular Z80 microprocessor contains a very powerful embedded routine dedicated to high-speed logarithmic functions. Because it operates in real time, it is significantly faster than lookup tables or computational approaches. Furthermore, it's directly addressable in analog format. All Z80 chips have this capability, although manufacturers do not supply the necessary data to exploit it.

The circuit in Fig 1 is a complete, real-time logarithmic ratio computer that uses fully parallel, coprocessing Z80s in the embedded logarithmic mode. Connecting an analyzer between the Z80's ground pin (pin
29) and the $D_{1}$ data bus (pin 15) reveals the internal logarithmic instruction set. Figs 2a, 2b, 2c, and 2d show that the best performance occurs in the $300-\mathrm{nA}$ to $750-\mu \mathrm{A}$ range.

This designer (Ed Note: We must avoid writing in the first person at all costs), discoverer of the Z80's logarithmic mode, is ebullient. Everyone always told this designer that analog circuits were nowhere. Now this designer believes it. Microcomputers are great. You can do anything with them. Can you imagine what's possible with one of those 32 -bit babies? This designer will bet that you can get another decade with

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## ABERRANT DESIGN IDEAS

that 386 thing. After lunch, this designer is going to go over to Intel and apply for a job. This designer is also going to trade in his Tektronix 547 and 556 for a
development system. But it's going to to be tough to find one with those funny little dots on the CRT.

EDN


Fig 1-A couple of Z80s, configured as full parallel coprocessors, perform real-time logarithmic ratio computations.


Fig 2-After viewing these displays, this author now believes "microcomputers are great."

## 1 is impossible. 2 is undesirable. 3 is...



The choices don't appear to be very attractive, but the problem must be solved. An eight-second test time for all-code differential and integral non-linearity testing is out of the question for production testing. And it gets worse geometrically for higherorder converters: A 16-bit device would take 128 seconds.

What about your options? The A/D already spits out numbers ten times as fast as most testers can process them - especially with the single, general-purpose array processor typically used for this test. Testing less codes or reducing the amount of averaging would seriously diminish test quality.

Which leaves you with speeding up the tester. An option LTX has considered..

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As a result, the Hi.T system brings all-code test time down to just 800 milliseconds. So you no longer have to compromise full testing to meet production demands on A/Ds and other sophisticated mixed-technology devices.

The Digital Signal Accelerator system is just one of the many local computers Hi.T uses to remove testing bottlenecks. Local processing helps Hi.T's parallel analog resources perform instant DC measurements. And local processing throughout the

## Hi.T. High-throughput linear testing from LTX.

system cuts down the time it takes instruments to set up between tests.

The result: Hi.T, as you would expect, approaches testing speed limited only by the response time of the device itself. When you're looking for speed - in multiples - Hi.T is the obvious choice.

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open cover permits easy access to the paper supply and battery pack. $\$ 435$. Delivery, four to six weeks ARO.

Syntest Corp, 40 Locke Dr, Marlboro, MA 01752. Phone (617) 481-7827. FAX 617-481-5769.

Circle No 370


## SNA COMM BOARD

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The AdaptModem V. 32 is a multiprotocol communications board for the IBM PC, PC/XT, PC/AT, PS/2 models 25 and 30 , and compatible computers. Because the board is designed for IBM's Systems Network Architecture (SNA), it implements three communications protocols on one plug-in board: a full-duplex asynchronous modem and a synchronous modem, which conform to the CCITT V. 32 standard, and a Synchronous Data-Link Control adapter. The board also supports 9600 -bps communications for a vari-
ety of available AdaptSNA software packages for SNA communications protocols, including interactive 3270 , batch $3770 /$ RJE, cooperative processing LU6.2/APPC, and program-to-program LU0. Plug-in board, $\$ 1295$; AdaptSNA software packages, $\$ 245$ to $\$ 785$.

Network Software Associates Inc, 22982 Mill Creek, Laguna Hills, CA 92653. Phone (714) 7684013.

Circle No 371

## BOARD COMPUTER

- Has a CMOS $\mu P$ and peripheral devices
- Is housed on a single-height VME bus board
Implemented with CMOS devices, the VSBC-1 single-board computer for VME bus systems consumes only $3 W$ of power. The singleheight board has a $68 \mathrm{HC} 000 \mu \mathrm{P}$ that runs at a clock speed of 12.5 or 16.7 MHz , and a memory capacity of 1 M bytes of zero-wait-state


CMOS static RAM and as much as 512k bytes of 1-wait-state EPROM. I/O facilities include two serial ports that you can configure with piggyback modules to operate at RS$232 \mathrm{C},-422,-485$ levels or in a $20-\mathrm{mA}$ current loop mode, and a 16 -bit parallel port with additional handshaking lines. You can optionally have a SCSI bus interface that is controlled by an NCR53C90 SCSI bus controller. Other onboard peripherals include 16 - and 24 -bit timer/ counters, a real-time clock, and a watchdog timer. An onboard lithium cell provides battery backup for the real-time clock and static RAM.

The board's VME bus interface includes a 7 -level interrupt handler and a single-level bus arbiter. Software support includes the OS-9 and PDOS operating systems, and debug monitor firmware. From $\$ 590$ in OEM quantities.

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## 386SX MOTHERBOARD

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Wave Mate Inc, 2341 205th St, Suite 110, Torrance, CA 90501. Phone (213) 533-8190. FAX 213-533-5940.

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## PGA VERIFIER

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Pushing the leading edge of display technologies, the Supertex family of HVCMOS* drivers permit major breakthroughs in electroluminescent, gas plasma, LCD \& vacuum fluorescent displays. This advanced smart power technology also opens up a wide range of applications in medical ultrasound imaging, robotics, telecommunications, test systems, high performance printers, power supplies, motor controls and solid-state relays.

The Supertex high density HVCMOS drivers, listed below, feature high speed with low power consumption to produce bright, high-resolution images. Investigate HVCMOS . . . a most attractive alternative to cumbersome boards or hybrids.

For more information or custom designs, write or call: Supertex, Inc., 1225 Bordeaux Drive, Sunnyvale, CA 94088; TeI. (408) 744-0100; Telex 6839143 SUPTX and FAX (408) 734-5247.

|  | HV03 \& 05 | 220 \& 300V | 64 Channel, Serial to Parallel Converters with N-Channel Open Drain Outputs |
| :---: | :---: | :---: | :---: |
|  | HV04 \& 06 | 60 \& 80V | 64 Channel, Serial to Parallel Converters with Push-Pull Outputs |
|  | HV08** | 60 V | 24 Channel, 16 Gray Shade Level Driver with Source Follower Outputs |
|  | HV10-18 | 140 \& 160V | 4 \& 8 Channel Bilateral Analog Switches |
|  | HV30 | 180 V | 7 Segment Decoder with Open Drain Outputs |
|  | HV41 \& 42, HV45 \& 46 | -220 \& -300V | 32 Channel, Serial to Parallel Converters with P-Channel Open Drain Outputs |
|  | HV51 \& 52, HV55 \& 56 | 220 \& 300V | 32 Channel, Serial to Parallel Converters with N-Channel Open Drain Outputs |
|  | HV53 \& 54, HV57 \& 58 | 60 \& 80V | 32 Channel, Serial to Parallel Converters with Push-Pull Outputs |
|  | HV500 \& 501 | 100 V | 32 Channel, AC Plasma Driver with Push-Pull Outputs |
|  | HV6810** | 80 V | 10 Channel, Vacuum-Fluorescent Driver with Push-Pull Outputs |
|  | AN01, AP01, HT01 | 160 to 400 V | 3 Chip Set for 8 Channel Level Translation with Low Leakage Push-Pull Outputs |

## NEW PRODUCTS

## INTEGRATED CIRCUITS

## QUAD S/H AMPLIFIER

- Has 12-bit accuracy
- Acquisition time is 600 nsec The AD684 quad S/H amplifier features 12 -bit accuracy and a sampling rate to 100 k samples/sec. Each channel of the AD684 has a guaranteed maximum acquisition time of 600 nsec to within $0.1 \%$, and $1 \mu \mathrm{sec}$ to within $0.01 \%$ for a 10 V step. For simultaneous sampling, the AD684's entire error budget is completely encompassed in a 300 psec max aperture offset between channels. A proprietary error-correcting architecture compensates for hold-mode errors and ensures 12 -bit accuracy and repeatability. The AD684 has a maximum fullscale nonlinearity of $0.005 \%$, and its hold characteristics include a 500 nsec maximum settling time, 200 -

psec aperture uncertainty, and a 10nsec aperture delay. The IC operates from $\pm 12 \mathrm{~V}$ supplies and dissipates 530 mW max. Three temperature grades are available. From
$\$ 23.50$ (100).
Analog Devices, Literature Center, 70 Shawmut Rd, Canton, MA 02021. Phone (508) 935-5565

Circle No 351


## LOG GAIN/ATTENUATORS

- Provide control from -24 to $24 d B$
- Interface with 8 - and 16-bit buses The ML2008 and ML2009 amplify or attenuate analog signals to $\pm 3 \mathrm{~V}$ under $\mu \mathrm{P}$ control and are noiserated at $900 \mathrm{nV} / \sqrt{\mathrm{Hz}}$ at 1 kHz . The devices provide automatic signallevel control from - 24 to 24 dB in 0.1 dB steps. The ML2008 interfaces to an 8 -bit $\mu \mathrm{P}$ bus, using two write operations to store nine gainsetting bits and a power-down bit. The ML2009 has a single 9-bit data register, which you can program with one write operation when using a 16 -bit data bus. Both devices operate from $\pm 5 \mathrm{~V}$ supplies. 18 -pin

DIP or 20 -pin plastic chip carrier, $\$ 5.50$ (100).
Micro Linear Corp, 2092 Concourse Dr, San Jose, CA 95131. Phone (408) 433-5200.

Circle No 352

## VIDEO CONTROLLER

- Features video rates to 120 MHz
- Supports high-resolution graphics
The IMS-G300 video controller supports high-resolution color graphics applications with resolutions of $640 \times 480(\mathrm{VGA}), 1024 \times 768$, and $1280 \times 1024$ pixels. The highly integrated chip contains a $256 \times 24$-bit color look-up table, a programmable video-timing generator, a 32 -bit multiplexed pixel port, a triple video DAC with 8 -bit resolution, and an on-chip, phase-locked loop. The -G300 can handle video rates to 120 MHz and interlaced or noninterlaced video. The chip has four 8 -bit pixel ports, which accept data

directly from the video RAM array at $25 \%$ of the video rate. The pixel port has two software-selectable operating modes. Mode 1 sends the data via the 24 -bit color look-up table, permitting the selection of 256 colors from a choice of over 16 million. Mode 2 sends the 24 -bit data directly to the 8 -bit video DACs, allowing the diplay of 16 million colors at any one time. The devices come in 84-pin PGA or LCCC packages. An $85-\mathrm{MHz}$ part, $\$ 100$ (1000).

Inmos Corp, Box 16000, Colorado Springs, CO 80935. Phone (719) 630-4215.

Circle No 353


## 

Lighter...Smaller...More Powerful... for single and three phase applications where high efficiency, precise regulation and a high degree of packaging density are required.
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- Fully programmable and remote sense
- Complies with VDE 875-N and VDE 871-A
- 5-year warranty


THREE
PHASE TCR

- 3 power ranges 2,500 W5,000 W10,000 W
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from 0 to $6 \mathrm{~V} D C$ through 0 to 600 VDC
- Regulated and metered (V and A)
- CVICC with automatic crossover
- Complies with VDE 875-N and VDE 871-A
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## INTEGRATED CIRCUITS

## DUAL AUDIO DAC

- Features 20-bit resolution
- Has two independent channels The D20200 is a complete, dual, 20bit, D/A-converter subsystem. The module includes two 20-bit DACs, a stable bipolar reference, a serial CMOS/TTL-compatible digital interface, and two distortion-suppressing output deglitchers/amplifiers. It needs no external components or trimming to meet its specifications; you only need to connect $\pm 15$ and 5 V power supplies, a serial data source, and appropriate timing signals. The D20200 handles output signal amplitudes from 0 to -60 $d B$. Total harmonic distortion and noise is typically -90 dB at -20 dB output and -52 dB at $-60-\mathrm{dB}$ output. Differential nonlinearity is typically $\pm 0.0002 \%$ of FSR. The D20200's serial interface accepts digital word lengths from 16 to 32 bits, and it accepts simultaneous or multiplexed data at a $15-\mathrm{MHz}$ maximum clock rate. It converts at rates from de to 200 kHz per channel and accepts digital coding formats of two's-complement, offset binary, or complementary offset binary. $\$ 199$ (100).

UltraAnalog Inc, Box 14164, Fremont, CA 94539. Phone (415) 657-2227.

Circle No 354

## STATIC RAM

- Features access time as low as 55 nsec
- Operates over the military temperature range
Targeted for use in military and aerospace applications, the MS8128 SC $128 \mathrm{k} \times 8$-bit high-speed static RAM has an operating temperature range of -55 to $+125^{\circ} \mathrm{C}$ and can be screened to MIL-STD883C requirements. It is available with access times of $55,70,85,100$, 120 , or 150 nsec and has TTLcompatible inputs and outputs. The device is manufactured from four $32 \mathrm{k} \times 8$-bit RAMs packaged in ce-

ramic leadless chip carriers that are bonded to a single 32 -pin ceramic DIP substrate that also carries chip-select decoding logic and power-supply decoupling capacitors. Operating at a clock frequency of 1 MHz it consumes 150 mW of power from one 5 V supply; in standby mode, it consumes 2 mW . A low-power version, which consumes only $40 \mu \mathrm{~W}$ in standby mode, is available for applications that use battery backup. From $£ 145$ to $£ 290$ (100).

Hybrid Memory Products Ltd, Elm Rd, W Chirton Industrial Estate, N Shields, Tyne and Wear NE29 8SE, UK. Phone 091-2580690. TLX 53206. FAX 091-2590997.

Circle No 355
Mosaic Semiconductor Inc, 7420 Carroll Rd, Suite 200, San Diego, CA 92121. Phone (619) 271-4565. FAX 619-271-6058.

Circle No 356

## ANALOG MULTIPLEXERS

- $100 \Omega$ on-resistance
- 250 nsec switching times

Pin compatible with the industrystandard DG508A and DG509A, the DG408 and DG409 analog multiplexers offer improved specifications compared to earlier types. The on-resistance of the DG408/409 is only $100 \Omega$, leakage current is less than 0.5 nA , switching time is 250 nsec, and power dissipation is only 2.5 mW . The DG408 is an 8 -channel, single-ended device with a 3 -bit binary address. The DG409 is a 4 channel, differential device with a

2-bit binary address. In addition to specification improvements, the DG408 and DG409 feature reduced sensitivity to electrostatic discharge (ESD) and the ability to withstand $\pm 400 \mathrm{~V}$ on all pins (with respect to ground). Both TTLcompatible multiplexers conduct current equally well in both direc-
tions and allow operation with supply voltages to $\pm 15 \mathrm{~V}$ or with 12 and 0 V unipolar supplies. 16-pin DIP and small-outline packages, $\$ 4.68$ to $\$ 15.92$ (100).

Siliconix Inc, 2201 Laurelwood Rd, Santa Clara, CA 95054. Phone (408) 988-8000.

Circle No 357

## Electro/89

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BUGS FAST.
 hunting pair for your 8031/8051 projects. Plug the EMUL51-PC into your PC, XT, AT or compatible and find bugs that other emulators can't. Our powerful software makes it a snap to use.

- 48 bits wide 16 K deep trace buffer - 20 MHz real-time emulation
- Supports 80535, 80C451, 80C152, 80C452, 80C552/652, 80C51FA, DS5000 and more.
- Available in either "Plug-in" or "Box"


The EMUL51-PC comes with a 5-ft. cable, software and 1 year hardware warranty with free software updates. Trace board optional.
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the SRAM speed barrier with our family of leading edge, super high speed CMOS SRAMs.
We've applied the same state-of-the-art design and process technology used for our high quality DRAMs in development of our fast static RAMs - with some amazing results.
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And like all Micron memory products, our SRAMs are backed by the type of strong sales, customer service and technical support that keeps you on the leading edge.
For additional information on how you can break the SRAM speed barrier, call 208-386-3900. Micron, it's a name worth remembering.

| Part \# | Organization | Speed | Packages |
| :--- | :---: | :--- | :--- |
| MT5C2561 | $256 \mathrm{~K} \times 1$ | $\mathbf{2 5}$ ns | PDIP, CDIP, SOJ, LCC |
| MT5C2564 | $64 \mathrm{~K} \times 4$ | $\mathbf{2 5} \mathrm{~ns}$ | PDIP, CDIP, SOJ, LCC |
| MT5C2565 | $64 \mathrm{~K} \times 4 \overline{\mathrm{OE}}$ | $\mathbf{2 5 n s}$ | PDIP, CDIP, SOJ, LCC |
| MT5C2568 | $32 \mathrm{~K} \times 8$ | $\mathbf{2 5 n s}$ | PDIP, CDIP, SOJ, LCC |
| MT5C6401 | $64 \mathrm{~K} \times 1$ | $\mathbf{1 5 n s}$ | PDIP, CDIP, SOJ |
| MT5C6404 | $16 \mathrm{~K} \times 4$ | $\mathbf{1 5 n s}$ | PDIP, CDIP, SOJ |
| MT5C6405 | $16 \mathrm{~K} \times 4 \overline{\mathrm{OE}}$ | $\mathbf{1 5 n s}$ | PDIP, CDIP, SOJ |
| MT5C6406/7 | $16 \mathrm{~K} \times 4$ S.I/O | $\mathbf{1 5 n s}$ | PDIP, CDIP, SOJ |
| MT5C6408 | $8 \mathrm{~K} \times 8$ | $\mathbf{1 5 n s}$ | PDIP, CDIP, SOJ, LCC |
| MT5C1601 | $16 \mathrm{~K} \times 1$ | $\mathbf{1 5 n s}$ | PDIP, CDIP, SOJ |
| MT5C1604 | $4 \mathrm{~K} \times 4$ | $\mathbf{1 5 n s}$ | PDIP, CDIP, SOJ |
| MT5C1605 | $4 \mathrm{~K} \times 4 \overline{\mathrm{OE}}$ | $\mathbf{1 5 n s}$ | PDIP, CDIP, SOJ |
| MT5C1606/7 | $4 \mathrm{~K} \times 4$ S. I/O | $\mathbf{1 5 n s}$ | PDIP, CDIP, SOJ |
| MT5C1608 | $2 \mathrm{~K} \times 8$ | $\mathbf{1 5 n s}$ | PDIP, CDIP, SOJ |

*Slower speeds also available.

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That's because the 8050 is without a doubt the brightest, most readable display in its class.

It's the first 10 -inch, AC -memory, flat panel display to deliver $640 \times 400$ resolution with an extraordinary 44 foot-lamberts of brightness. Along with a contrast ratio of greater than 20:1. All in a package just over one inch thick.

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So if your application calls for the clearest images with maximum contrast, call us today at 1-800-556-1234, Ext. 238. Inside California call, 1-800-441-2345, Ext. 238. Or write Fujitsu Component of America, Inc., 3330 Scott Boulevard, Santa Clara, CA 95054-3197.

We'll brighten your day.

CIRCLE NO 40

FUJITSU
COMPONENT OF AMERICA. INC


## NEW PRODUCTS

## COMPONENTS \& POWER SUPPLIES



## DISPLAY MODULE

- Features VT320 emulation
- Includes touch-input system

The M320ST electroluminescent display module provides graphics capability and VT320 emulation with standard 80 -character $\times 25$-line text. It also features an infrared touch-input system, SealTouch, that provides a resolution of 2000
touch points. SealTouch firmware allows you to program button sizes, positions, and response. You can have as many as 120 pages with a maximum of 120 buttons $/ \mathrm{pg}$. You can define buttons as pop-up menus, multistate responses, or program them for touch sensitivity for applications requiring fail-safe operation. Complete terminal setup parameters are accessible on screen. The module includes an RS232 C , RS-422, or RS-485 serial communications port (or optional 4- to $20-\mathrm{mA}$ operation), a serial printer port, and an ASCII keyboard port. $\$ 3195$.
Digital Electronics Corp, 31047 Genstar Rd, Hayward, CA 94544. Phone (415) 471-4700. TLX 172073.

Circle No 360

## FIBER-OPTIC LINK

- Operates over 2 km
- Offers user-selectable inputs

This fiber-optic link provides an RFI/EMI-secure circuit for Electrospace Systems' MLP-1 phone and its associated PBX. The link consists of the F9765 and the F9766 and has a transmission capability of 2 km min. The F9765 is designed for use at the PBX end of the circuit and includes a male 25 -pin connector. The F9766 is located at the phone and features a female 25 position connector. The link has a $0.3-$ to $3.5-\mathrm{kHz}$ bandwidth and outputs 0 dBm into a balanced $600 \Omega$ load. Each unit consists of two pc boards. The first board holds the power supply and the digitizing and multiplexing circuitry, and the sec-

# Digital filters 

Manulactured by NPC
NIPPON PRECISION CIRCUITS LTD.

| DEVICE | PACKAGE |  | COMPOSITION | SAMPLING FREQ. OVER SAMPLING | TAPS | FILTER (dB)CHARACTERISTICS |  | DATA FORMAT |  | FEATURES |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | TYPE | PIN |  |  |  | PASSBAND <br> RIPPLE | STOPBAND ATTEN UATION | INPUT | OUTPUT |  |
| $\begin{array}{\|c\|} \hline \text { SM5803AP/ } \\ \text { APT } \\ \hline \end{array}$ | DIP | 28 | 2 channels | 8/4 times | 153+29+17 | $\pm 0.00005$ | 110 | Serial | Serial | For digital audio system |
| $\begin{gathered} \hline \text { SM5813AP/ } \\ \text { APT } \\ \hline \end{gathered}$ | DIP | 28 | 2 channels | 8 times | $153+29+17$ | $\pm 0.00005$ | 110 | Serial | Serial | For digital audio system |
| $\begin{gathered} \text { SM5802 } \\ A / B \\ \hline \end{gathered}$ | FPP | 60 | 2 channels | 2 times | 80 | $\pm 0.09 / \pm 0.01$ | 90 | Serial Parallel | Serial Parallel | High stopband attenuation Small passband ripple |
| SM5804 <br> A/B/C/D | FPP | 60 | 2 channels | 4 times | $80+15$ | $\pm 0.09 / \pm 0.015$ | 90 | Serial Parallel | Serial Parallel | High stopband attenuation Small passband ripple |
| SM5805 | DIP | 28 | 2 channels | 2 times | 121 | $\pm 0.001$ | 90 | Serial | Serial | For recording and playing |
| SM5806 | $\begin{aligned} & \text { DIP } \\ & \text { SOP } \end{aligned}$ | 28 | 2 channels | 2 times | 70 | $\pm 0.05$ | 60 | Serial | Parallel | For compact disk |
| SM5807 D/E/F | $\begin{aligned} & \text { DIP } \\ & \text { SOP } \end{aligned}$ | 16 | 2 channels | 4 times | $61+13$ | $\pm 0.05$ | 50/45 | Serial | Serial | For compact disk |
| $\begin{gathered} \hline \text { SM5814 } \\ A / B \end{gathered}$ | $\begin{aligned} & \text { DIP } \\ & \text { SOP } \end{aligned}$ | $\begin{aligned} & 22 \\ & 24 \\ & \hline \end{aligned}$ | 2 channels | 4 times | $105+21$ | $\pm 0.001 / \pm 0.01$ | 70/52 | Serial | Serial | 64 steps digital attenuation sharp cut-off characteristics |
| SM5820 | DIP | 40 | 1 channel | $\begin{aligned} & 52 \mathrm{kHz} \\ & (\max ) \end{aligned}$ | $\begin{gathered} 60 \\ (\max ) \\ \hline \end{gathered}$ | Mask Option |  | Parallel | Parallel | Semi custom |
| SM5831 | FPP | 64 | 4 on-chip multipliers | 15 MHz | 4, 7, 8 cascadable | On-chip coefficient register |  | Parallel | Parallel | For video signal |
|  | PGA | 68 |  | 25 MHz |  |  |  | High speed digital filter |  |  |

U.S. and Canada Sales Office

For complete product information and order, contact Jim Chang,
Director of Customer Service/Developments or, Greg Branch, Sales Director
ond holds the interface circuitry. A slide switch allows you to select link inputs of 115 or 230 V ac, 47 to 63 Hz . The link operates over 0 to $50^{\circ} \mathrm{C}$ and consumes 6 W . $\$ 1960$ per pair.

Versitron, 9005-8 Junction Dr, Annapolis Junction, MD 20701. Phone (301) 497-8600.

Circle No 361

## COOLING SWITCH

- Operates on logic-level inputs - Can operate to $70^{\circ} \mathrm{C}$

The Series 305 cooling-failure switch operates on 5 V dc input signals and responds to any change in temperature in 1 to 3 sec . The switch can generate a false signal when its own temperature exceeds


## ERK Series

- Switches at 200 KHz
- MAG-AMP Regulation
- AC $115 / 220 \mathrm{~V}$ (selectable)
- 100, 150, 200W Triple and Quad
- Safety: UL, CSA, TUV
- EMI: FCC/VDE 0871 Class "B"


## PRK Series

(Pictured Above)

- Switches at 60 to 300 KHz
- Input Range AC 85-132V
- 30, 50, 70W Triple Output
- Safety: UL, CSA
- EMI: FCC Class "B"


## MRE Series

- Switches at 300 KHz
- Universal Input AC85-264V
- Miniature size
- 15 and 30W Single Output
- Safety: UL, CSA, TUV
- EMI: FCC/VDE 0871 Class "B"

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a factory preset limit. Operating over a 5 to $70^{\circ} \mathrm{C}$ range, the switch features a self-heated glass-bead thermister, which compensates for ambient temperature, air speed, altitude, and relative humidity, and can sense a reversal in air flow. The switch is cooled by the same air stream that cools the host equipment, and measures $3 \times 0.5 \mathrm{in}$. From \$15.

Cambridge Aeroflo Inc, 900 Mt Laurel Circle, Shirley, MA 01464. Phone (508) 425-2346.

Circle No 362


## ULTRASONIC SENSORS

- Feature noncontact operation
- Withstand harsh environments

UC60 Series ultrasonic sensors offer a noncontact distance-sensing capability. The series is made up of the UC60-LN1A analog outputlevel sensor and the UC60-ZD1A switched-output zone-detection sensor. Both include adjustable sens-ing-zone features, built-in temperature compensation, short-circuit/ transient-protected outputs, and 10 to 30 V dc operation. The LN1A outputs distance measurements as an analog voltage or current. The ZD1A produces a switched output when an object enters a preset zone. Both units are built to with-

## EXTENDED TEAPERATURE

## MODULES CAN TAKE IT



# THE VF MODULESTOUSE IF HELL FREEZES OVER. 

If that day arrives and you need a clear readout, DeeCO's XT and XTB extended temperature display modules won't let you down.

From $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$, through 40 g shock and 2 g rms vibration, XT series modules can take the heat. And the cold. And whatever else you or the forces of evil throw at them.

And when you need clear sunlight readability, our XTB1 $\times 40$ high brightness extended temperature module delivers more than 600 fl of brilliant performance.

stand harsh environments and are encapsulated in stainless-steel cases that carry a NEMA $1,2,12$, and 13 rating. UC60-LN1A, $\$ 695$; UC60ZD1A, $\$ 595$.

Opcon Inc, 720 80th St SW, Everett, WA 98203. Phone (206) 3530900.

Circle No 363

## DC/DC CONVERTERS

- Provide 1.5W single- or split-rail outputs
- Have 500 V input-to-output isolation
EL1 isolated de/de converters have an output power rating of 1.5 W and are available in single- or dualoutput versions. Single-output ver-

sions have an output voltage of 5 , 12 , or 15 V , and dual-output versions have split-rail $\pm 5, \pm 12$, or $\pm 15 \mathrm{~V}$ outputs. They are available with nominal input-voltage ratings of 5,12 or 24 V . Their input-tooutput isolation voltage capability is 500 V dc, and they have an isolation resistance of $10 \mathrm{G} \Omega$. Line regulation is more than $\pm 0.3 \%$ for a $\pm 10 \%$ input voltage change, and zero- to full-load output regulation is more than $\pm 0.5 \%$. All versions have a Pi filter on the input to minimize input and output noise. The converters are housed in standard DIP packages that measure $32 \times 20 \times 10.5 \mathrm{~mm}$ and weigh 17 g . They have a -25 to $+71^{\circ} \mathrm{C}$ operating temperature range. £18.
Gresham Powerdyne Ltd, Gresham House, Telford Rd, Salisbury, Wiltshire SP2 7PH, UK. Phone (0722) 413080. TLX 477576. FAX 0722-336263.

Circle No 364
Dowty Electronics Corp, Box 250, Prospect St, Brandon, VT 05733. Phone (802) 247-6811.

Circle No 365

## CONNECTORS

- Have 15 contacts in a 9-contact shell
- Feature gold-plated contacts

Sigma-D crimp-insertable D-subminiature connectors provide 15 contacts in a 9 -contact shell. You can install the contacts by hand or with a machine. The brass contact pins and phosphor bronze sockets have gold over nickel plating as
standard. Other finishes are available as an option. The contacts have a $5 \mathrm{~A} / 500 \mathrm{~V}$ de rating. The connectors can accept \#26 or 28 AWG wire sizes. Contacts are available in reels or in loose pieces for hand crimping. Male connectors, $\$ 1.31$ ( 500 ); 10,000 -pin reel of contacts, $\$ 70$.
Vernitron Corp, Beau Products Div, Box 10, Laconia, NH 03247. Phone (603) 524-5101. FAX 603-524-1627.

Circle No 366

## SELECTOR SWITCHES

- Available in top- or side-adjust versions
- Sealed to withstand assembly processes
SS-10 rotary DIP selector switches are available in top- or side-adjust versions. Single- and dual-pole models are available with four or six contacts and three contact configurations, respectively. All surfaces are permanently sealed to withstand standard soldering and washing processes. The self-cleaning, gold-plated contacts have a $5 \mathrm{~V} /$ 100 mA resistive switching rating. Contact resistance equals $100 \mathrm{~m} \Omega$ max. The switches can carry 50 V dc at 100 mA . The rotational life equals 500 cycles min and the operating range spans -10 to $+60^{\circ} \mathrm{C}$. $\$ 1.70(100)$.
Mepcopal Co, 11468 Sorrento Valley Rd, San Diego, CA 92121. Phone (619) 453-0332. FAX 619-481-1123.

Circle No 367

## FAN SYSTEM

- Offers 12- and 15-fan capacity
- Design isolates vibration

The Airmatic 300 Fan Tray system features models with either a 12 -or 15 -fan capacity. The tray is configured from two structural foam halves, which include individual fan compartments to isolate noise and vibration. Rubber standoffs mounted to 8 points on the fan fur-
ther isolate noise and vibration. Each fan compartment is prewired, and each fan is terminated with a plug to ease fan replacement or additions in the field. Empty fan positions come with foam and a metal insert. All trays feature a brushed and anodized front panel, which includes easy-access handles. You can
order the trays with any number of fans from one to each tray's maximum capacity. 12-position tray with one fan, $\$ 302.47$.

Dacobas Inc, 1890 N Voyager Ave, Simi Valley, CA 93063. Phone (805) 526-7733. FAX 805-584-8371.

Circle No 368

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## NEW PRODUCTS

## TEST \& MEASUREMENT INSTRUMENTS

## CALCULATOR

- Performs 254 functions
- Works with simultaneous equations and complex numbers The TI-68 advanced scientific calculator performs 254 functions and handles complex numbers as easily as it handles real ones. It can simultaneously display the real and imaginary parts of a complex quantity. The $6 \times 3 \times 0.6-\mathrm{in}$. unit sports a 12 -character alphanumeric LCD that scrolls horizontally to display equations having as many as 80 characters. The calculator can solve five simultaneous equations; a plain-English prompting scheme guides you through equation entry. You can recall and replay the last equation entered, and you can edit equations after you've entered them. The calculator allows you ac-
cess to as many as 36 registers and lets you assign names to the registers. You can enter as many as 12 formulas; the formulas remain in memory even when the calculator is off. The unit also determines the real and complex roots of quadratic, cubic, and quartic equations. $\$ 65$.

Texas Instruments Inc, Box 53 , Lubbock, TX 79408. Phone (806) 747-1882.

Circle No 380

## AUDIO TEST SET

- Generates 8-ppm distortion sine waves from 1 Hz to 102.39 kHz
- Provides $0.03 \%$-inaccurate crys-tal-controlled frequencies
The 3100 B generator and 3200 B autoranging analyzer form an audio test set that measures amplitude
and phase vs frequency and intermodulation (IM) and total harmonic distortion (THD) vs frequency or amplitude. The analyzer measures phase from -180 to $+180^{\circ}$ with $0.1^{\circ}$ resolution to 40 kHz and ac voltages from $4 \mu \mathrm{~V}$ to 100 V with residual THD and IM of 20 ppm . The generator stores 91 front-panel setups and can produce sine waves from 1 Hz to 102.39 kHz with 8-ppm distortion and square waves from 1 Hz to 50 kHz with a rise time of $<1$ $\mu$ sec. As the frequency is crystal controlled, errors are less than $0.03 \%$ at fixed frequencies and on some sweeps. Generator, $\$ 4250$; analyzer, $\$ 5495$.

Sound Technology, 1400 Dell Ave, Campbell, CA 95008. Phone (408) 378-6540. TLX 357445.

Circle No 381

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## RISC DEVELOPER

- Supports 88000 RISC chips
- Traces system activity in real time to 50 MHz
The DS5000 development system provides in-circuit support for the 88100 RISC processor and the 88200 cache/memory management unit. The development system can perform 256 -channel logic analysis and provides 16 levels of unrestricted triggering. It traces all tar-get-system activity in real time to 50 MHz and captures trace data in 4 k - or 16 k -frame buffers. You can define trigger conditions for the cache, program memory, data memory, instruction memory, or combinations of all of them. By using a pair of buffers and filling one while routing the other's contents via DMA to the host processor's RAM, the development system can acquire data continuously. The development system works with MS-DOS-based hosts, including some Sun Microsystems units. $\$ 28,000$ to $\$ 40,000$. Delivery, six weeks ARO.
Hilevel Technology Inc, 31 Technology Dr, Irvine, CA 92718. Phone (800) 445-3835; in CA, (800) 541-2742. TLX 655316.

Circle No 382

## TEST TRANSLATOR

- Tranlates PLD test vectors
- Creates source files for GenRad testers
The JED2DTS software utility runs on DEC VAXs under VMS and on IBM PCs, PC/XTs, PC/ATs, and compatible computers. The utility
translates PLD test vectors created with the vendor's ATG (automatic test generator) software into DTS (digital test source) files for GenRad 227 x and 2282 in-circuit pe-board test systems. The DTS files include head, inhibit, disable, force, and main sections. If the number of vectors exceeds a user-defined limit, the utility creates multiple pattern bursts. PLD definition files let you customize the translation process. $\$ 1695$ including communication software for error-free file transmission to the tester.

Anvil Software Inc, 427-3 Amherst St, Suite 341, Nashua, NH 03063. Phone (603) 891-1995. FAX 603-891-1999.

Circle No 383


## DMM/THERMOMETER

- Offered with ${ }^{\circ} \mathrm{C}$ and ${ }^{\circ} \mathrm{F}$ readouts
- Measures ac current with clampon transformer
The ACA Series of multimeters includes three models, two of which measure temperature-one in ${ }^{\circ} \mathrm{F}$, the other in ${ }^{\circ} \mathrm{C}$. All three units incorporate a peak-hold function; the two that measure temperature also include data-hold and diode-check functions. All three models measure ac current via integral clamp-on


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transformers on full-scale ranges of 200 and 400 A . The unit that doesn't measure temperature also includes a 20 A ac current range. AC-cur-rent-measuring accuracy on all units is $1 \%$ to 100 A . All units measure ac and dc voltage and resistance and have four dc-voltage ranges. The unit that doesn't measure temperature has four resistance and two ac-voltage ranges. The other units have two resistance ranges and one ac-voltage range. $\$ 119$; $\$ 109$ without temperature measurement.

Extech Instruments Corp, 150 Bear Hill Rd, Waltham, MA 02154. Phone (617) 890-7440. TLX 940913.

Circle No 384

## BOARD TEST SOFTWARE

- Adds enhancements to 1800 Series testers
- Automatic test-program backup prevents program loss
A software update to the vendor's 1800 -Series board testers incorporates five features that expand test coverage and increase programming flexibility. These features include dual threshold measurements, which let you define both high- and low-voltage regions; HiCheck, which produces a 4-digit hexadecimal signature for all highregion measurements; digital filtering, which increases stability in a voltage measurement by averaging multiple sample readings; HiGuard, which improves guarded measurement accuracy by eliminating the thermal EMF of relay contacts; and differential measurements, which let you make voltage measurements that aren't referenced to system ground. The addition of program flow control and branching capabilities increases programming flexibility. $\$ 500$.

Zehntel Inc, 2625 Shadelands Dr, Walnut Creek, CA 94598. Phone (415) 932-6900. TWX 910-385-6300.

Circle No 385


## DIGITAL MULTIMETERS

- Have a 1-year dc voltage accuracy of 20 ppm
- Include an IEEE-488 interface and digital recalibration
The Model 5001 and Model 6001 are $6^{1 / 2}$-digit instruments that have a 24 -hour dc voltage stability of $\pm(4$ ppm of reading +2 ppm of full scale) and a 1 -year dc voltage accuracy of $\pm 20 \mathrm{ppm}$. The Model 5001 provides dc and true-rms ac voltage, dc and true-rms ac current, and 2 -wire resistance measurement functions. The Model 6001 has the same basic specification as the 5001, and also provides both temperature measurement using a $100-\Omega$ platinum resistance thermometer probe, and 4wire resistance measurement. Both instruments have dc voltage measurement ranges from 0.2 to 1000 V , ac voltage measurement ranges from 2 to 700 V rms, dc and ac current ranges of 2 mA and 2 A , and resistance measurement ranges of $200 \Omega$ to $12 \mathrm{M} \Omega$. The instruments provide measurement periods selectable between 50 msec and 10 sec and feature math functions, an IEEE-488 interface, and digital recalibration facilities. A 10 -channel input scanner option is available for both instruments. Model 5001, \$1495; Model 6001, \$1695.

Prema GmbH, Robert-KochStrasse 10, 6500 Mainz 42, West Germany. Phone (06131) 50620. TLX 4187666. FAX 06131-506222.

Circle No 386
Prema Precision Electronics Inc, 4650 Arrow Highway, Suite E5, Montclair, CA 91763. Phone (714) 621-7292. FAX 714-625-2098.

Circle No 387

## CABLE CUTTER

- Cuts round cables
- Handles 300-pair cable

The PA 1818 portable cable cutter is 12 in . long. It cuts round multiconductor cables containing as many as 300 signal pairs. It also cuts copper cables to 750 MCM (thousands of circular mils) and alu-
minum cables to 1000 MCM . The unit includes a folding safety latch and a release mechanism that enables you to move the tool to a different location. \$239.
Paladin Corp, 3543 Old Conejo Rd, Suite 102, Newbury Park, CA 91320. Phone (805) 499-0138.

Circle No 388


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 YOU CAN SEE FOR YOURSELF.Just send this ad, along with your business card, to Mike Hartman, our Marketing Manager. Along with our DESIGN GUIDE, he'll send you a sample EL lampboth free. After you kick it around for a while, you'll understand why we say - no other light can hold a candela to ours.


[^10]
## NEW PRODUCTS

## CAE \& SOFTWARE DEVELOPMENT TOOLS

## REAL-TIME KERNEL

- Runs in the 32-bit, protected mode of the 80386
- Allows a combination of local and global tasks
MTOS-UX/386 is a multiprocessing, multitasking, real-time operating system for 80386 -based computers. This OS normally runs in the 32 -bit, protected mode of the 80386 , and protects system resources such as block and memory pools, message buffers, controlled shared variables, and task resources. Also available is a version that uses the multisegmented memory model to run MS-DOS software. This model protects the kernel and the system resources by means of task privilege levels. You can increase the computing power of the system merely by adding up to 16 CPUs;
changing the number of CPUs does not require any change to the applications programs. The development kit includes test facilities, debugging tools, validation programs, configuration programs, a RAMdisk driver, a Unix interface, and a C-portable library. The symbolic debugger provides task-level debugging facilities. Because all versions of MTOS-UX have the same programmer interface, programs written in a high-level language will run under any version of MTOSUX, regardless of the processor type. Development kit prices start at $\$ 5000$.

Industrial Programming Inc, 100 Jericho Quadrangle, Jericho, NY 11753. Phone (516) 938-6600. TLX 429808. FAX (516) 938-6609.

Circle No 389


## CAE TOOL

- Handles double-sided SMT designs
- Handles multiple power planes and as many as 16 signal layers The MAXI/PC schematic-capture and pc-board layout package can execute double-sided, surfacemount designs with as many as 16 signal layers; it also handles multiple power and ground planes having


## New SLO-SYN" Servo Positioners


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The new 800 Series SLO-SYN ${ }^{\circledR}$ Closed Loop Servo Motion Controls are single axis, stand-alone positioners that can execute stored motion profiles with a velocity programming resolution of $8,000,000: 1$. They are ideally suited for industrial automation applications which require demanding precise control of positioning or velocity.
800 Series units can be programmed and directed through an RS232 serial port from PC compatible software, a "dumb" terminal or a hand-held programmer. For systems configured with discrete $\mathrm{I} / \mathrm{Os}$, they can be externally interfaced through 14 defined inputs and outputs. All controls feature real time adaptive gain control that automatically adjusts the gain to compensate for load changes. The high velocity programming resolution ratio permits speed changes in extremely small increments.
A complete file of SLO-SYN ${ }^{\circledR}$ Motion Control literature is available on request. It is must reading for anyone involved with motion control system design.
a resolution of $1 / 1000 \mathrm{in}$. High-speed automatic features include placement, gate- and pin-swapping, component renaming, back-annotation, and routing. The package runs on IBM PCs and compatibles. $\$ 995$.

Racal-Redac Inc, 238 Littleton Rd, Westford, MA 01886. Phone (508) 692-4900.

Circle No 390

## STABILITY ANALYZER

- Simplifies setup and operation of a network analyzer
- Includes modeling and synthesis package for loop analysis
The $\mathrm{S} 350 / 3577$ stability software package allows you to integrate your HP3577A Network Analyzer from Hewlett-Packard (Palo Alto, CA) with an IBM PC or compatible, a printer, and a plotter, to form a complete stability-analysis workstation. The menu-driven software simplifies the setup and operation of the HP3577A, so that you can quickly obtain Bode plots or Nyquist diagrams of control-loop circuits. You can store the data on disk for later analysis and circuit optimization. The software includes the vendor's proprietary K-factor modeling and synthesis package for loop optimization; the software also works with PC-MATLAB for matrix computations, and with ECA-2 for circuit modeling and analysis. From $\$ 5995$.

Venable Industries Inc, 3555 Lomita Blvd, Torrance, CA 90505. Phone (213) 539-2522. FAX 213-539-4139.

Circle No 391

## SIMULATION MODELS

- Library contains models for more than 4000 LSI/VLSI devices
- Models allow fault simulation at the board or system level
SmartModels is a library of behavioral models for more than 4000 LSI/VLSI devices. Previously available for logic simulation, the
vendor has now adapted all the models for use on Mentor Graphics' (Beaverton, OR) QuickFault fault simulator. The vendor plans to support other simulators that have a behavioral interface. Behavioral models are easier to write and faster to load than gate-level models; they also run faster and allow
you to simulate larger designs without increasing the memory requirements. SmartModels allow concurrent fault simulation; that is, you can divide the design into several parts and run each part on a different node of a network, or on parallel processors of a multiprocessor system. The original subscription serv-


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ice to SmartModels for fault simulation costs $\$ 7900$; the FLEX-Node service, which allows you to move licenses around a network, costs $\$ 9900$ (minumum, 3 FLEX-Node subscriptions).

Logic Automation, 19500 NW Gibbs Dr, Beaverton, OR 97006. Phone (503) 690-6900.

Circle No 392

## C LIBRARY

- Lets you build resident shared libraries
- Allows you to convert existing programs to TSR versions
/*resident_C*/ is a library of C routines for building terminate-and-stay-resident (TSR) programs. The C routines let you build interruptservice routines, such as timers that schedule a program to run at a particular time. You can also build resident shared libraries that can be accessed by any number of programs. The library also allows you to convert existing C programs to TSR status by adding a few function calls. Other routines included in the library let you save screens or windows so your TSR program won't disrupt the program that it interrupts. Versions of the library are available for the Microsoft (QuickC and C 5.0), Borland (Turbo C), and Lattice C compilers that run on IBM PCs and compatibles. The distribution disk includes demonstration programs that show you how to use the library and how to build shared libraries. Binary version, $\$ 99$; binary and source code, $\$ 198$.

Essential Software Inc, 76 S Orange Ave, Suite 3, S Orange, NJ 07079. Phone (201) 762-6965.

Circle No 393

## NET-LIST GENERATOR

- Allows you to reverse-engineer pc boards
- Copes with boards that contain high pin-count devices
The Net-Learn utility software for
the company's SI635 diagnostic test system lets you reverse-engineer pc boards by generating a connectivity net list for the board's components. You can then use the net list to construct a schematic diagram. The menu-driven software uses the system's in-circuit test capabilities to learn the pin-to-pin interconnec-
tions between all the devices on the pc board. Net-Learn combines as many as 128 test channels to cope with high pin-count devices. The utility employs a 2 -pass test strategy to generate the net list. During the first pass, the pe board under test is powered up, and the tester locates all pins that are connected


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to power or ground lines. The pc board is turned off during the second pass, and the utility determines the interconnections between devices. The system eliminates faulty net-list generation by checking for good probe contact before the learning process begins. To cope with board modifications or updates, the
software can perform a partial learn operation. You can use the ouptut files from Net-Learn to generate schematic diagrams for the pc under test. Around $£ 2100$.

Schlumberger Technologies, Instruments Div, Victoria Rd, Farnborough, Hampshire GU14 7PW, UK. Phone (0252) 544433. TLX

## 858245. FAX 0252-543854.

Circle No 394
Schlumberger Technologies, Instruments Div, 20 N Ave, Burlington, MA 01803. Phone (617) 2294825. TLX 910-250-745. FAX 617-229-4885.

Circle No 395

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CHECK THE ITINERARY ON THE OPPOSITE PAGE FOR THE DATE WE VISIT YOUR COMPANY.


# 1989 WESTERN EDN CARAVAN TRAVELING ELECTRONIC SHOW April 3 to May 5 (Central Edition) 

| DATE | time | SITE |
| :---: | :---: | :---: |
| April 3 Monday | $\begin{aligned} & \text { 9:00-12:00 } \\ & \text { AM } \end{aligned}$ | LOCKHEED ENGINEERING \& SCIENCES COMPANY 2400 Nasa Rd., Houston, TX |
| April 3 Monday | $\begin{aligned} & \text { 1:30-4:00 } \\ & \text { PM } \end{aligned}$ | COMPAQ COMPUTER CORPORATION 20555 FM 149, Houston, TX |
| April 4 Tuesday | $\begin{aligned} & \text { 9:00-11:00 } \\ & \text { AM } \end{aligned}$ | TEXAS INSTRUMENTS INC., Data Systems Group 12501 Research Blvd., Austin, TX |
| April 4 Tuesday | $\begin{aligned} & \text { 1:00-3:30 } \\ & \text { PM } \end{aligned}$ | IBM CORPORATION 11400 Burnet Road, Austin, TX |
| April 5 Wednesday | $\begin{aligned} & \text { 8:30-11:00 } \\ & \text { AM } \end{aligned}$ | TRACOR, INC. 6500 Tracor Lane, Austin, TX |
| April 5 <br> Wednesday | $\begin{aligned} & \text { 1:00-3:30 } \\ & \text { PM } \end{aligned}$ | TEXAS INSTRUMENTS INC., Data Systems Group 5701 Airport Road, Temple, TX |
| April 6 Thursday | $\begin{aligned} & \text { 8:30-10:30 } \\ & \text { AM } \end{aligned}$ | ROCKWELL INTERNATIONAL 1225 N. Alma Road, Richardson, TX |
| April 6 <br> Thursday | $\begin{aligned} & 11: 30-1: 00 \\ & \text { AM-PM } \end{aligned}$ | ROCKWELL INTERNATIONAL <br> Shiloh \& Renner Road, Richardson, TX |
| April 6 <br> Thursday | $\begin{aligned} & \text { 2:15-4:30 } \\ & \text { PM } \end{aligned}$ | E-SYSTEMS, INC., Garland Division 1200 Jupiter Road, Garland, TX |
| April 7 <br> Friday | $\begin{aligned} & 8: 30-11: 00 \\ & \text { AM } \end{aligned}$ | ELECTROSPACE SYSTEMS INC. <br> Greenville Ave. \& Terrace Dr., Richardson, TX |
| April 7 <br> Friday | $\begin{aligned} & 1: 30-3: 30 \\ & \text { PM } \end{aligned}$ | E-SYSTEMS, INC. <br> Farm Road 1570, Greenville, TX |
| April 10 Monday | $\begin{aligned} & \text { 9:00-11:30 } \\ & \text { AM } \end{aligned}$ | TEXAS INSTRUMENTS, INC. 8505 Forest Lane, Dallas, TX |
| April 10 Monday | $\begin{aligned} & \text { 1:00-3:30 } \\ & \text { PM } \end{aligned}$ | TEXAS INSTRUMENTS INC. <br> 13500 North Central Expressway, Dallas, TX |
| April 11 Tuesday | $\begin{aligned} & \text { 9:00-11:00 } \\ & \text { AM } \end{aligned}$ | LTV -Missiles \& Electronics Group 1902 West Freeway, Grand Prarie, TX |
| April 11 Tuesday | $\begin{aligned} & \text { 2:00-4:00 } \\ & \text { PM } \end{aligned}$ | RELIANCE COMM/TEC 2100 Reliance Pkwy., Bedford, TX |
| April 12 Wednesday | $\begin{aligned} & \text { 9:00-12:00 } \\ & \text { AM } \end{aligned}$ | GENERAL DYNAMICS Grants Lane, Ft. Worth, TX |
| April 12 Wednesday | $\begin{aligned} & \text { 2:00-4:00 } \\ & \text { PM } \end{aligned}$ | RECOGNITION EQUIPMENT INC. 2701 Grauwyler Rd. Irving, TX |
| April 13 Thursday | $\begin{aligned} & \text { 8:30-11:00 } \\ & \text { AM } \end{aligned}$ | TEXAS INSTRUMENTS INC. Data Systems Group 2501 S. Highway 121, Lewisville, TX |
| April 13 Thursday | $\begin{aligned} & \text { 1:30-4:00 } \\ & \text { PM } \end{aligned}$ | BOEING ELECTRONICS 7801 S. Stemmons, Corinth, TX |
| April 14 Friday | $\begin{aligned} & \text { 9:00-11:30 } \\ & \text { AM } \end{aligned}$ | TEXAS INSTRUMENTS INC. 6500 Chase Oakes Blvd., Plano, TX |
| April 14 Friday | $\begin{aligned} & \text { 1:00-3:00 } \\ & \text { PM } \end{aligned}$ | TEXAS INSTRUMENTS INC. 2501 W. University, McKinney, TX |
| April 17 <br> Monday | $\begin{aligned} & \text { 9:00-11:00 } \\ & \text { AM } \end{aligned}$ | IMPRIMIS TECHNOLOGY INC. 10323 West Reno Ave., Oklahoma City, OK |
| April 18 <br> Tuesday | $\begin{aligned} & 9: 00-11: 30 \\ & \text { AM } \end{aligned}$ | NCR CORPORATION 3718 N. Rock Rd., Wichita, KS |
| April 18 <br> Tuesday | $\begin{aligned} & 1: 30-4: 00 \\ & \text { PM } \end{aligned}$ | BOEING MILITARY AIRPLANE CO. 3801 South Oliver, Wichita, KS |
| April 19 Wednesday | $\begin{aligned} & \text { 9:00-11:30 } \\ & \text { AM } \end{aligned}$ | BENDIX KING <br> 400 N. Rogers Road, Olathe, KS |
| April 19 Wednesday | $\begin{aligned} & \text { 1:30-3:30 } \\ & \text { PM } \end{aligned}$ | WILCOX ELECTRIC, INC. 2001 NE 46th St., Kansas City, MO |
| April 20 <br> Thursday | $\begin{aligned} & \text { 9:00-12:00 } \\ & \text { AM } \end{aligned}$ | AT\&T BELL LABORATORIES 777 North Blue Pkwy., Lees Summit, MO |


| DATE | TIME | SITE |
| :---: | :---: | :---: |
| April 21 | 9:00-11:30 | EMERSON ELECTRIC |
| Friday | AM | Evans Ave., St. Louis, MO |
| April 21 | 1:30-3:30 | EMERSON ELECTRIC, Electronics \& Space Div. |
| Friday | PM | 8100 W. Florissant, St. Louis, MO |
| April 24 | 9:00-11:00 | MTS SYSTEM CORPORATION |
| Monday | AM | 14000 Technology Dr., Eden Prairie, MN |
| April 24 | 11:45-2:00 | IMPRIMIS TECHNOLOGY INC. |
| Monday | AM-PM | 5950 Clearwater Dr., Minnetonka, MN |
| April 24 | 2:45-4:30 | HONEYWELL, INC., Defense Systems |
| Monday | PM | 5901 So. County Road 18, Edina, MN |
| April 25 | 8:30-10:30 | HONEYWELL, INC. Military Avionics |
| Tuesday | AM | 6300 Olson Memorial Pkwy., Golden Valley, MN |
| April 25 | 11:30-1:30 | HONEYWELL, INC., Military Avionics |
| Tuesday | AM-PM | 1625 Zarthan Avenue, St. Louis Park, MN |
| April 25 | 2:30-4:30 | IMPRIMIS TECHNOLOGY INC. |
| Tuesday | PM | 7801 Computer Dr., Bloomington, MN |
| April 26 | 8:30-11:00 | CONTROL DATA CORPORATION |
| Wednesday | AM | 3101 East 80th St., Minneapolis, MN |
| April 26 | 12:30-2:30 | NCR COMTEN |
| Wednesday | PM | 2700 Snelling Ave., Roseville, MN |
| April 26 | 3:00-4:30 | UNISYS CORPORATION |
| Wednesday | PM | 2276 Highcrest Dr., Roseville, MN |
| April 27 | 8:30-11:00 | UNISYS CORPORATION |
| Thursday | AM | 3333 Pilot Knob Rd., St. Paul, MN |
| April 27 | 1:00-4:00 | IBM CORPORATION |
| Thursday | PM | Hwy. 52 \& Northwest 37th St., Rochesteer, MN |
| April 28 | 8:30-11:00 | ALLEN-BRADLEY COMPANY |
| Friday | AM | 1201 So. 2nd St., Milwaukee, WI |
| April 28 | 12:00-1:30 | GENERAL ELECTRIC, Medical Systems |
| Friday | PM | 16800 W. Ryerson Rd., New Berlin, WI |
| April 28 | 2:30-4:30 | GENERAL ELECTRIC, Medical Systems |
| Friday | PM | 3000 N. Grandview Blvd., Waukesha, WI |
| May 1 | 9:00-11:30 | ROCKWELL INTERNATIONAL, Collins Avionics Div. |
| Monday | AM | 400 Collins Road NE, Cedar Rapids, IA |
| May 1 | 1:00-3:30 | ROCKWELL INTERNATIONAL, Communications Div. |
| Monday | PM | 855 35th St. N.E., Cedar Rapids, IA |
| May 2 | 9:00-11:00 | NORAND CORPORATION |
| Tuesday | AM | 550 Second St. S.E., Cedar Rapids, IA |
| May 2 | 1:00-3:00 | LITTON INDUSTRIES, Clifton Precision |
| Tuesday | PM | 2734 Hickory Grove Rd., Davenport, IA |
| May 3 | 8:30-11:00 | SUNDSTRAND CORPORTION, Data Control Group |
| Wednesday | AM | 4747 Harrison Ave., Rockford, IL |
| May 3 | 1:30-3:30 | MOTOROLA, INC. |
| Wednesday | PM | 1501 W. Shure Dr., Arlington Heights, IL |
| May 4 | 8:30-10:30 | NORTHROP CORPORATION |
| Thursday | AM | 600 Hicks Road, Rolling Meadows, IL |
| May 4 | 11:30-1:00 | NORTHROP CORPORATION |
| Thursday | AM-PM | 2525 Buffe Road, Elk Grove Village, IL |
| May 4 | 2:00-4:00 | MOTOROLA, INC. |
| Thursday | PM | 1301 E. Algonquin Rd., Schaumburg, IL |
| May 5 | 9:00-11:30 | AG COMMUNICATION SYSTEMS |
| Friday | AM | 2500 N. Wolf Road, Northlake, IL |
| May 5 | 1:00-3:30 | ZENITH ELECTRONIC SYSTEMS |
| Friday | PM | 1000 Milwaukee Ave., Glenview, IL |

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## CAREER OPPORTUNITIES

1989 Editorial Calendar and Planning Guide

| Issue <br> Date | Recruitment Deadline | Editorial Emphasis | EDN News Edition |
| :---: | :---: | :---: | :---: |
| Apr. 27 | Apr. 6 | Communications Technology, Special Issue Communication ICs | Closing: Apr. 13 <br> Mailing: May 4 |
| May 11 | Apr. 20 | Analog Technology, Special Issue Computer Peripherals | Closing: Apr. 28 <br> Mailing: May 18 |
| May 25 | May 4 | Digital ICs, Computer Peripherals | Closing: May 25 |
| June 8 | May 18 | Components, Digital ICs | Mailing: |
| June 22 | June 1 | Semicustom ICs, Computer Boards | Closing: June 9 <br> Mailing: June 29 |
| July 6 | June 15 | Product Showcase Volume I, Power Supplies | Closing: June 22 <br> Mailing: July 13 |
| July 20 | June 29 | Product Showcase - Volume II, Components | Closing: July 21 |
| Aug. 3 | July 13 | Integrated Circuits, Computer Boards | Mailing: Aug. 10 |
| Aug. 17 | July 27 | Military Electronics, Special Issue Military Software | Closing: Aug. 4 <br> Mailing: Aug. 24 |
| Sept. 1 | Aug. 10 | Test \& Measurement, Integrated Circuits | Closing: Aug. 18 Mailing: Sept. 7 |
| Sept. 14 | Aug. 24 | Industrial Product Showcase, Digital ICs | Closing: Aug. 30 <br> Mailing: Sept. 21 |
| Sept. 28 | Sept. 7 | Integrated Circuits, Computer Peripherals | Closing: Sept. 15 <br> Mailing: Oct. 5 |
| Oct. 12 | Sept. 21 | DSP Chip Directory, Integrated Circuits | Closing: Sept. 28 <br> Mailing: Oct. 19 |
| Oct. 26 | Oct. 5 | Test \& Measurement, Special Issue, Computers \& Peripherals | Closing: Oct. 27 |
| Nov. 9 | Oct. 19 | CAE, Integrated Circuits | Mailing: Nov. 16 |
| Nov. 23 | Nov. 2 | 16th Annual $\mu \mathrm{P} / \mu \mathrm{C}$ Directory, Integrated Circuits | Closing: Nov. 9 <br> Mailing: Nov. 30 |
| Dec. 7 | Nov. 16 | Product Showcase - Volume I, Power Supplies | Closing: Nov. 22 <br> Mailing: Dec. 14 |
| Dec. 21 | Nov. 30 | Product Showcase Volume II, Components |  |

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Hardware/Circuit Design Engineers/Managers
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- Configuration Management - Cabinet Design


## Software Engineers/Programmers/Managers

opportunity to advance if you're experienced with:

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- ADA Language Architecture and Programming
- Embedded Programmable Processors ( 68000 or similar)

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GE Government Electronic Systems Division

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- User Support Services

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| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | $\begin{aligned} & 100 \\ & \mathrm{MHz} \end{aligned}$ | $\begin{aligned} & 1000 \\ & \mathrm{MHz} \end{aligned}$ | $\begin{aligned} & 2000 \\ & \mathrm{MHz} \end{aligned}$ | Min. (note) |  |  |  |  |
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