

EDN[®]

Micropower op-amp applications

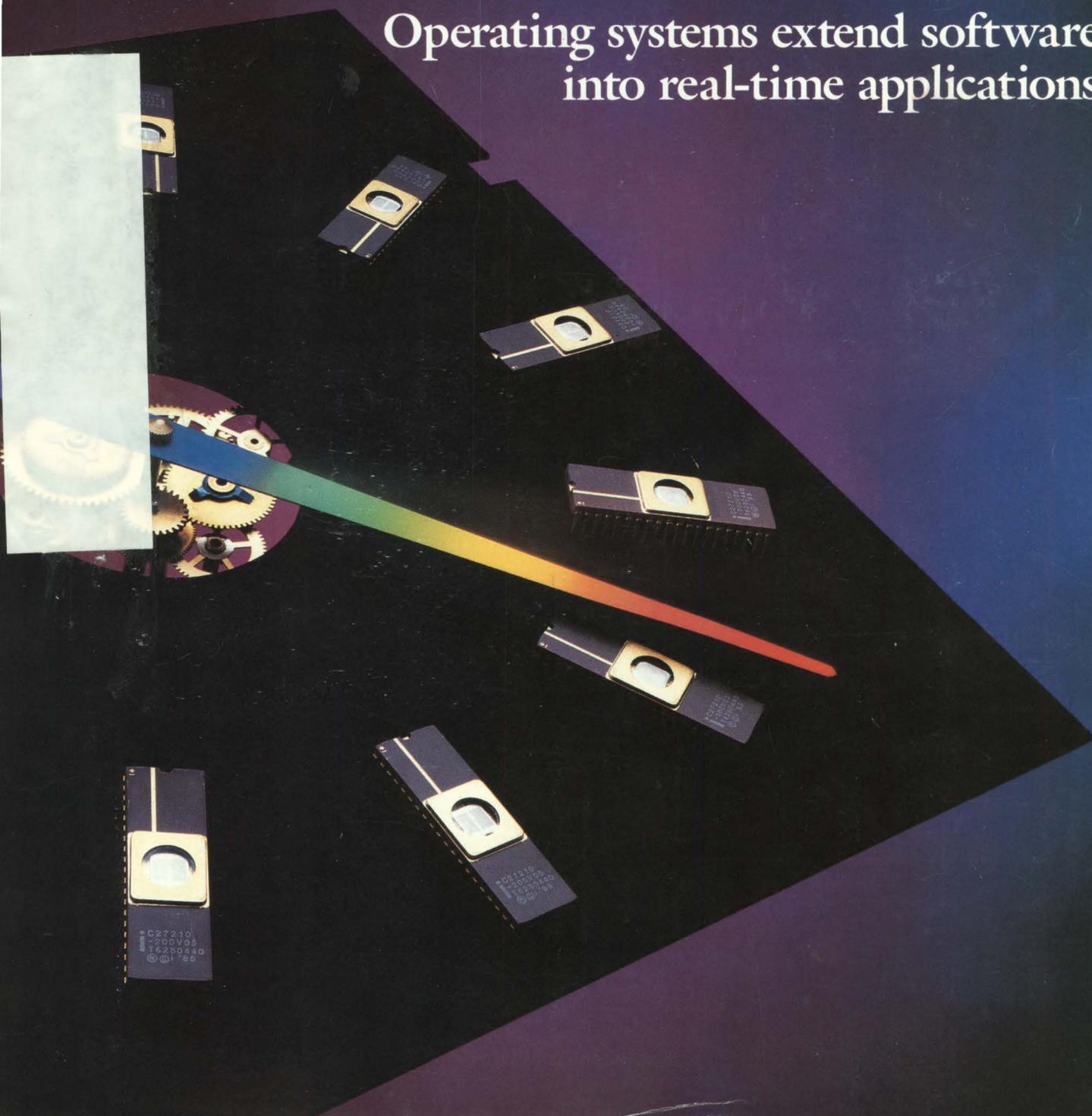
DC/DC converters for low-power circuits

1988 calendar of industry events

Telephone ICs

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* Patent pending
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CIRCLE NO 148

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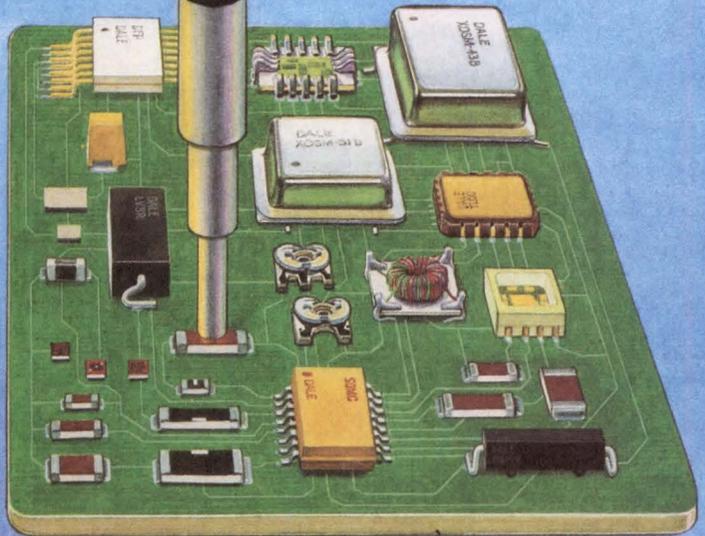
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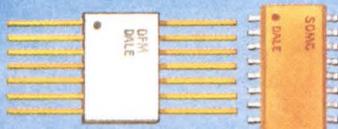
Dale makes your basics better

CIRCLE NO 1



Thick Film Networks

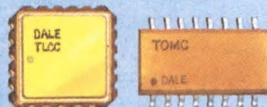
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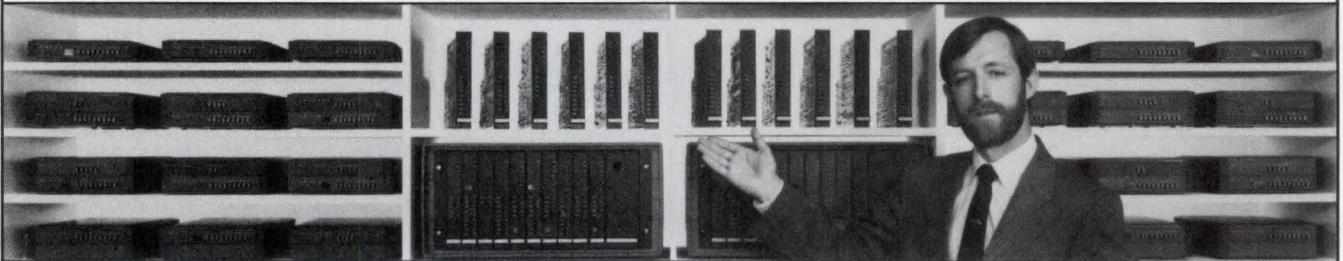


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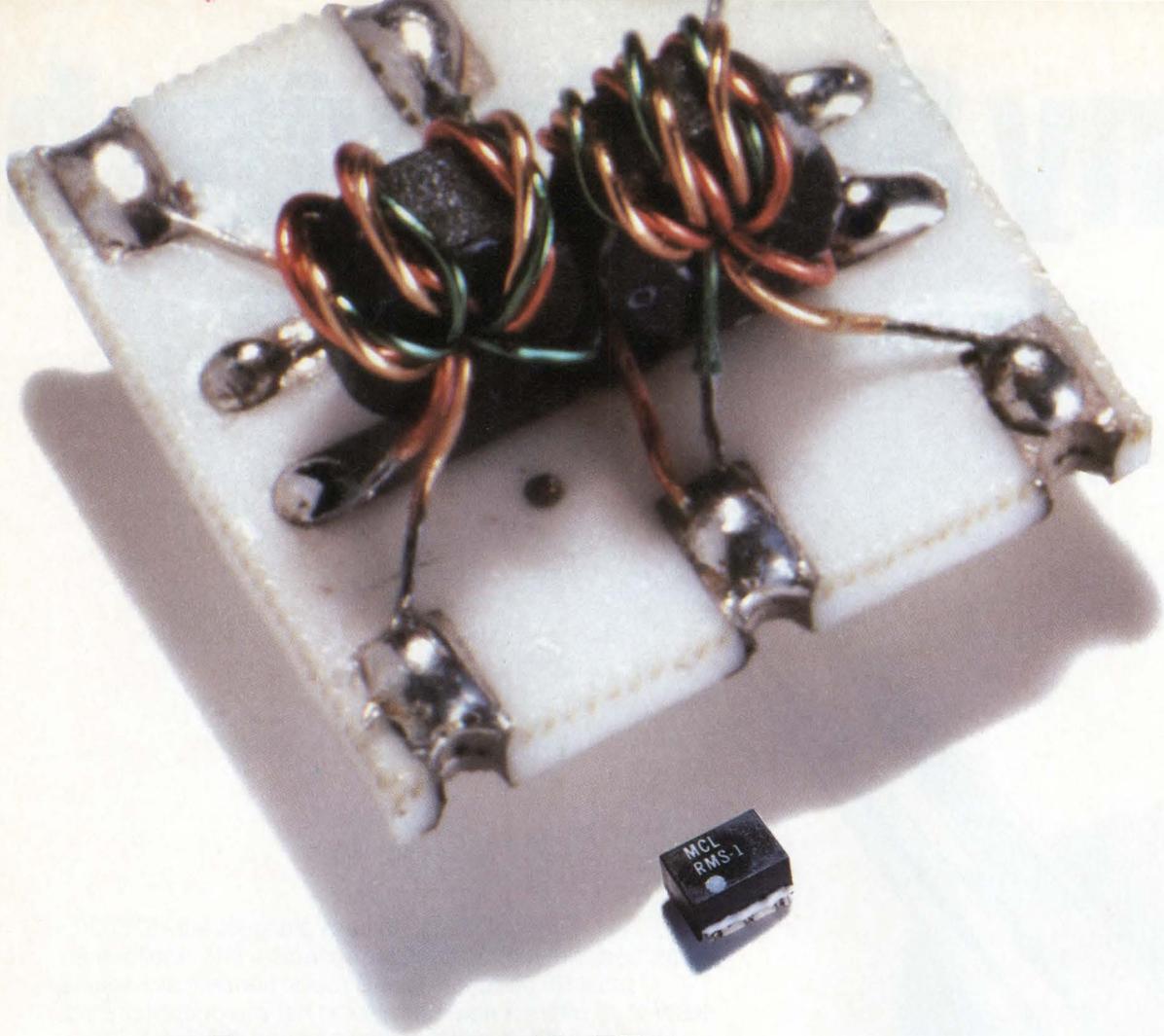
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Domestic and International Telexes: 6852844 or 620156

SPECIFICATIONS

FREQUENCY RANGE, MHz

LO, RF

IF

RMS-1

0.5 — 500

DC — 500

RMS-2

5 — 1000

DC — 500

CONVERSION LOSS, dB, Typ.

Mid-band ($10f_1 - f_{u/2}$)

Total range ($f_1 - f_u$)

5.5

6.2

6.5

7.0

ISOLATION, dB, Typ.

Low-band ($f_1 - 10f_1$)

Mid-band ($10f_1 - f_{u/2}$)

Upper-band ($f_{u/2} - f_u$)

L-R L-I

55 50

33 30

27 24

L-R L-I

55 50

35 30

25 20

PRICE (10-49)

\$6.95

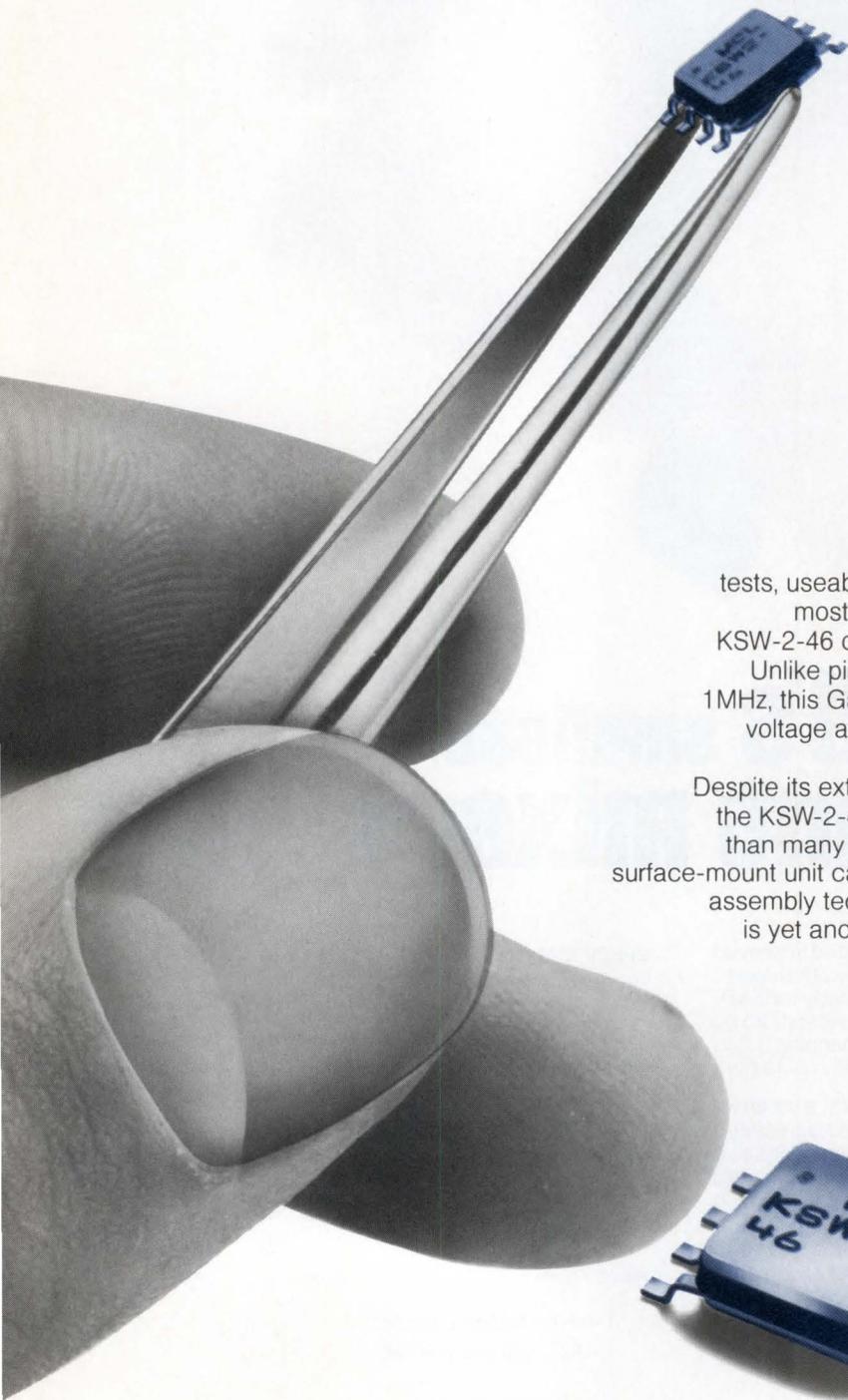
\$7.95

f_1 = lowest frequency in range

f_u = highest frequency in range

tiny SPDT switch

dc to 4.6GHz... \$32.95⁽¹⁻²⁴⁾

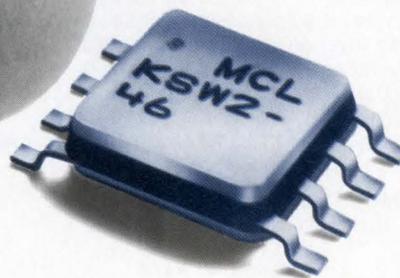


Tough enough to pass stringent MIL-STD-202 tests, useable from dc to 6GHz operation, and smaller than most RF switches, Mini-Circuits' hermetically-sealed KSW-2-46 offers a new, unexplored horizon of applications.

Unlike pin diode switches that become ineffective below 1MHz, this GaAs switch can operate down to dc with control voltage as low as -5V, at a blinding 2ns switching speed.

Despite its extremely tiny size, only 0.185 by 0.185 by 0.06 in., the KSW-2-46 provides 50dB isolation (considerably higher than many larger units) and insertion loss of only 1dB. The surface-mount unit can be soldered to pc boards using conventional assembly techniques. The KSW-2-46, priced at only \$32.95, is yet another example of components from Mini-Circuits with unbeatable price/performance.

Switch fast... to Mini-Circuits' KSW-2-46



SPECIFICATIONS

FREQ. RANGE	dc-4.6 GHz	
INSERT. LOSS (db)	typ	max
dc-200MHz	0.9	1.1
200-1000MHz	1.0	1.3
1-4.6GHz	1.3	1.7
ISOLATION (dB)	typ	min
dc-200MHz	60	50
200-1000MHz	45	40
1-4.6GHz	30	23
VSWR (typ)	1.3:1	
SW. SPEED (nsec)	2(typ)	
rise or fall time	2(typ)	
MAX RF INPUT (dBm)	+17	
up to 500MHz	+27	
above 500MHz	+27	
CONTROL VOLT.	-5V on, OV off	
OPER./STOR TEMP.	-50 to +100°C	
PRICE	\$32.95 (1-24)	

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setting higher standards

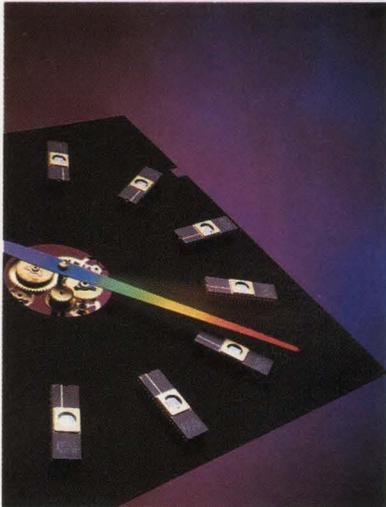
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CIRCLE NO 140

C 117 REV. A

EDN January 7, 1988



On the cover: Real-time operating systems are introducing order into chaos. See pg 114. (Photo courtesy Intel Corp)

DESIGN FEATURES

Special Report: Real-time operating systems

114



A real-time operating system can enable you to design and write a large real-time software system as a collection of simple, potentially reusable routines. But using a formal real-time OS means learning a completely new programming style.—*Charles H Small, Associate Editor*

DC/DC converters adapt to the needs of low-power circuits

145

High cost, quiescent current, and circuit complexity have often restricted switching power supplies to high-power applications, for which the switchers' high efficiency, wide input range, and reduced size and weight offset their drawbacks. Now, however, you can advantageously employ switchers in low- and medium-power applications.—*Len Sherman, Maxim Integrated Products*

Proper glitch capture requires knowledge of logic-analyzer limits

157

Using a logic analyzer to locate the source of intermittent malfunctions in digital systems can prove to be extremely frustrating. If you understand your analyzer's capabilities and limitations, though, you raise the odds of having the instrument furnish the information you need.—*Wolfgang Schweitzer, Kontron Messtechnik*

Integrated PLDs support Multibus II bus arbitration

165

The incorporation of buried state registers in PLDs makes the devices suitable for the design of sequential machines. Such devices thus provide compact packages for containing the bus-arbitration logic in Multibus II systems.—*Arthur Khu, Advanced Micro Devices*

Micropower op amp offers simplicity and versatility

181

An op amp whose input range includes both supply rails and whose output voltage swings within 100 mV of those rails can simplify a circuit by eliminating certain traditional components.—*Zahid Rahim, Signetics Corp*

Continued on page 7

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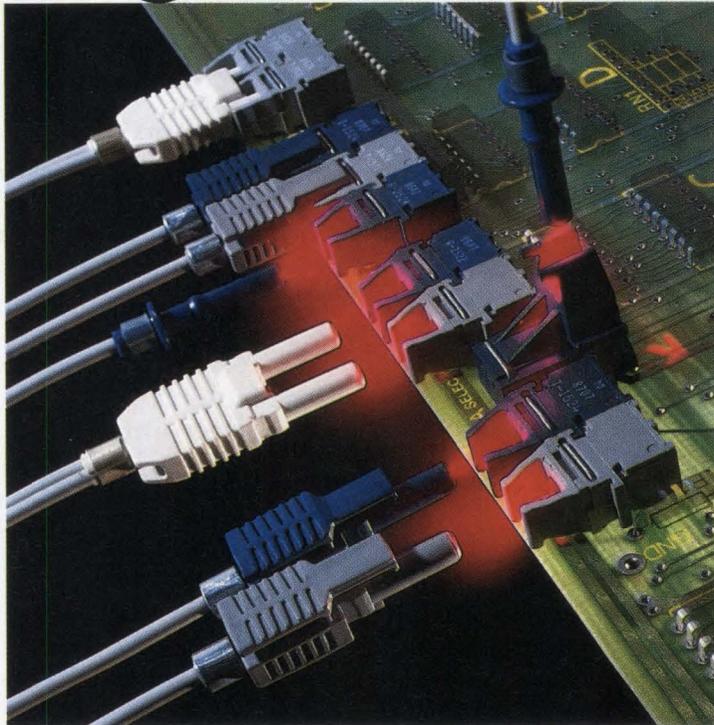


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*U.S. List price.

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PACKARD**

CIRCLE NO 137



Just-introduced telecomm ICs offer economical ways to upgrade telephone- and PABX-system designs (pg 55).

EDN magazine now offers Express Request, a convenient way to retrieve product information by phone. See the Reader Service Card in the front for details on how to use this free service.

Express Request 

TECHNOLOGY UPDATE

Telecomm ICs offer improved functions for telephone- and PABX-system designs 55

The latest offerings from telecomm-IC manufacturers not only continue the general trend toward higher integration by incorporating more functions than previous telecomm ICs did—they also substantially improve on those functions.—*Dave Pryce, Associate Editor*

Analog comparators achieve high speeds, but application challenges remain 75

High-speed analog comparators have always presented design challenges, and the state-of-the-art devices discussed in this article are no exception.—*David Shear, Regional Editor*

Raster printers profit from available technologies to suit diverse uses 87

Almost all computer applications today rely on hard-copy-output devices, and with the abundance of raster-printing technologies available, you can now match a raster printer with just about any application.—*Maurry Wright, Regional Editor*

PRODUCT UPDATE

500-kHz to 1-GHz hybrid amplifier	103
Frequency- and time-measuring analyzer	104
Scientific calculators	106

DESIGN IDEAS

Baseline restorer is voltage programmable	191
Program designs T flip-flop state machines	192
Circuit vocalizes dialed phone numbers	198
Signal edges set and clear D flip-flop	200
MOSFET switches memory-supply current	202

Continued on page 9

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EDITORIAL

47

As electronic systems become more complex, standards become less standard, which leads to trouble.

NEW PRODUCTS

Integrated Circuits	207
Components & Power Supplies	215
Computers & Peripherals	224
CAE & Software Development Tools	255
Test & Measurement Instruments	261

LOOKING AHEAD

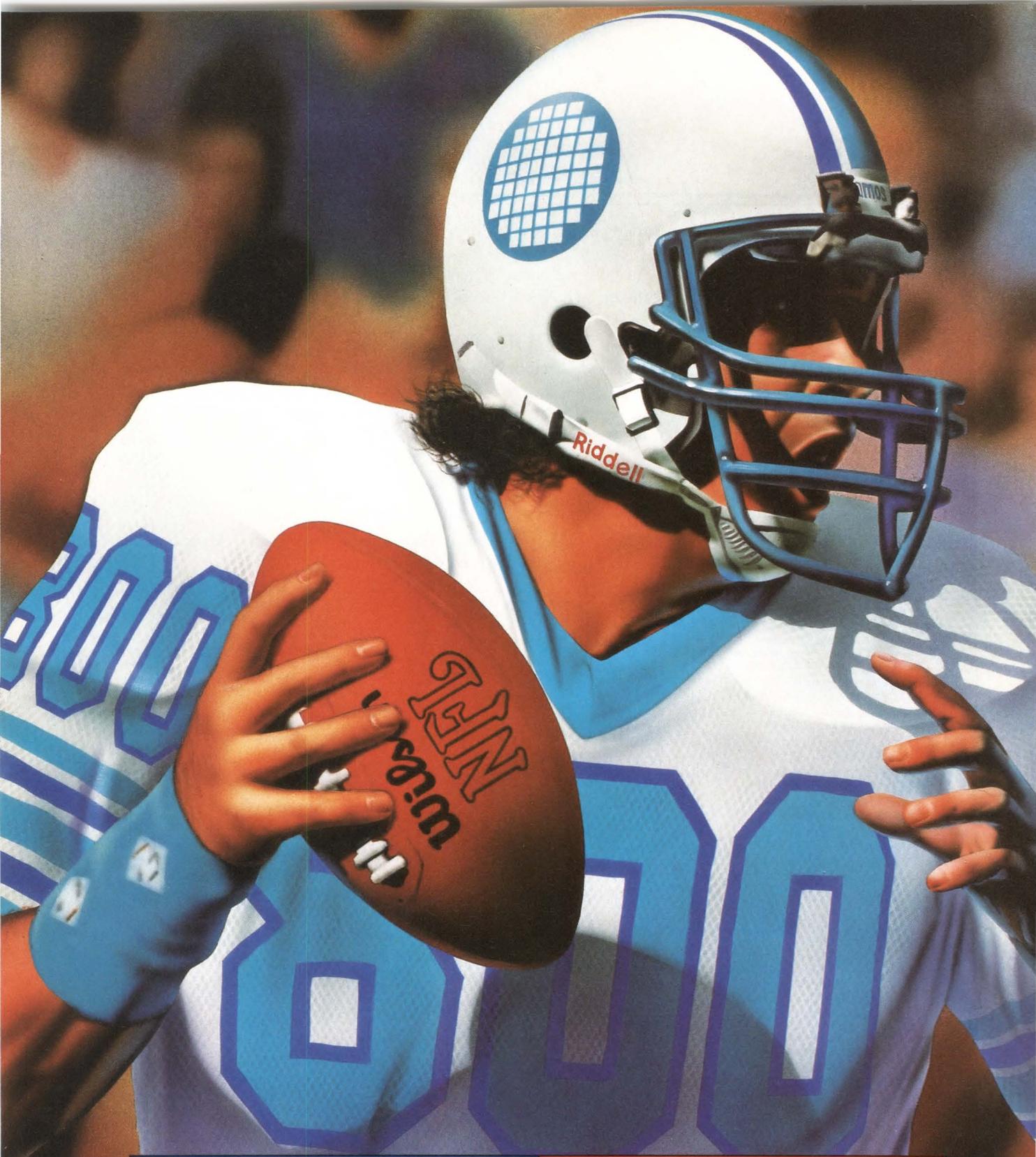
285

PC-board market to grow at 8% average rate per year. . . More US companies plan for crisis communications.

DEPARTMENTS

News Breaks	21
News Breaks International	24
Signals & Noise	33
Calendar	40
Readers' Choice	109
Leadtime Index	112
Literature	273
Business/Corporate Staff	275
Career Opportunities	276
Advertisers Index	282

Professional Issues will return next issue.



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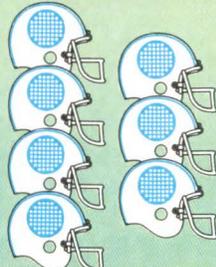
INTEL.
386/387 16 MHz
1.8 MEGAWHETSTONES.



MOTOROLA.
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1.5 MEGAWHETSTONES.



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MEGAWHETSTONES...
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IMS T414-20	32-Bit	20	9500	0.75 Million	Now	Q2 88	84 PGA
IMS T212-17	16-Bit	17	8000	-	Now	Q2 88	68 PGA
IMS T212-20	16-Bit	20	9500	-	Now	Q2 88	68 PGA
IMS M212-17	16-Bit	17	8000	-	Now	-	68 PGA
NETWORK SUPPORT PRODUCTS					AVAILABILITY		PACKAGE
Part No.	Description		Communication Speed		Commercial	Military	
IMS C004	Software configurable 32 way link switch		10 + 20 MBits/sec		Now	Q2 88	84 PGA
IMS C011	Link to system bus		10 + 20 MBits/sec		Now	-	24 Pin DIP
IMS C012	Link to system bus		10 + 20 MBits/Sec		Now	Q2 88	24 Pin DIP

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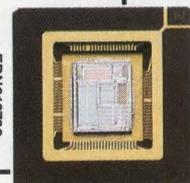
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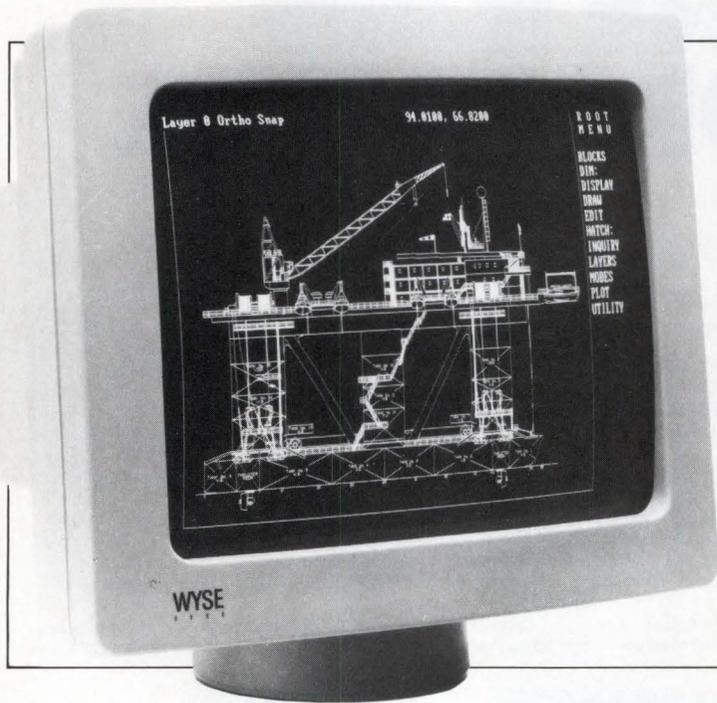
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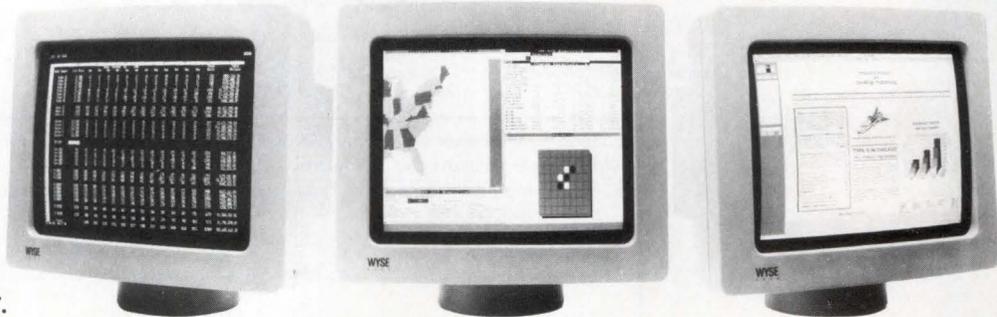
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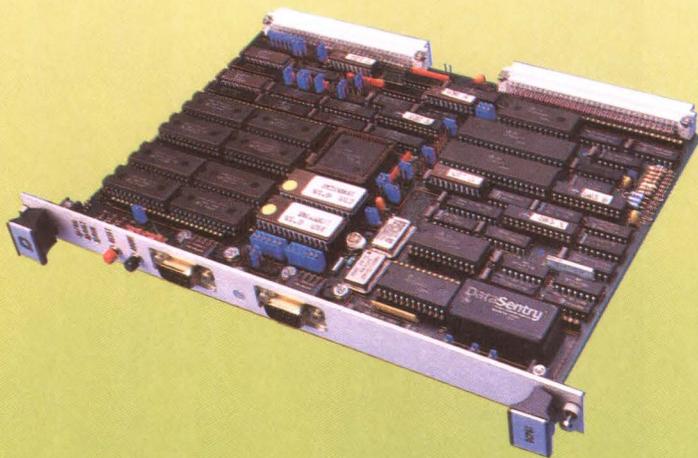
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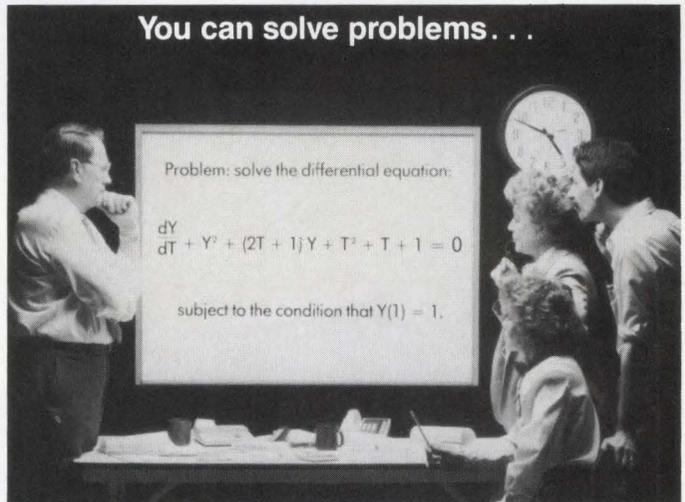
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```
(C1) DEPENDS(Y,T)$
(C2) DIFF(Y,T) + Y^2 + (2*T + 1)*Y + T^2 + T + 1;
(D2)  dY/dT + Y^2 + (2T + 1)Y + T^2 + T + 1
(C3) SOLN:ODE(D2,Y,T);
(D3)  Y = - %CT%e^T - T - 1
        %C%e^T - 1
(C4) SOLVE(SUBST([Y = 1, T = 1],D3),%C),NUMER;
(D4)  [%C = 0.5518192]
(C5) SPECIFIC SOLN:SUBST(D4,SOLN);
(D5) Y = - 0.5518192 T %e^T - T - 1
        0.5518192 %e^T - 1
```

and Numerically.

```
(C6) FORTRAN(D5)$
      Y = - (0.5518192*T*EXP(T) - T - 1)
          1 / (0.5518192*EXP(T) - 1)
```

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on a rough application concept?



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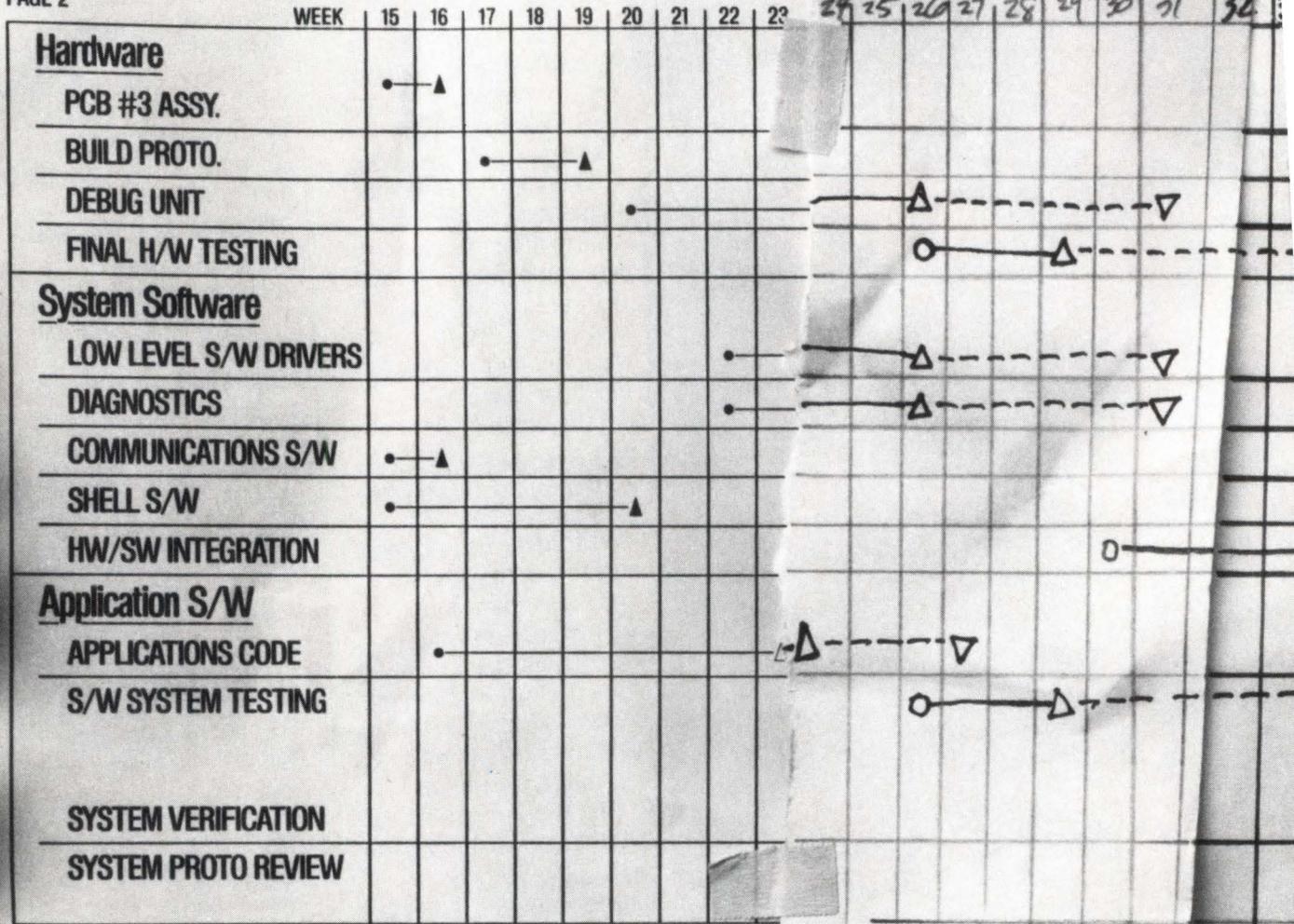
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CIRCLE NO 133

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PRODUCT DEVELOPMENT SCHEDULE

PAGE 2



Let's face it. Slipped development schedules and budget overruns can mean lost opportunities. Yet many traps that seriously delay a development schedule are quite complex, especially when they are compounded by problems that arise in cross development work.

Like not knowing whether the errors you are getting from your prototype processor are real. Or losing bugs in the cracks between your development system and the prototype.

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Our VALIDATE/ES DRIVER package includes easy-to-use (menu-driven and remote control) software that smoothly links the host functions to the ES 1800 emulator. This allows the upload and download of programs, symbol tables and command files.

```

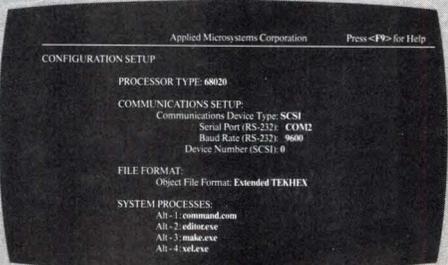
15: for (count = 1; count <= 100; count++)
16:
17:   beep k; /* "Beep" at user. */
18:   outscope k; /* Display --> SOFT SCOPE 2.0 */
19:   outlang k; /* Display --> C86 example */
20:   outcount/count; /* Display --> Count=xx */
21:   do_data k; /* Data reference demo. */
22:   delay k; /* Slow display down. */
23:
24: }
*/
*reg
AN=0000 SP=0066 CS=30D0 IP=0000
BX=0000 BP=0000 DS=30B7 FL=0000 =0D D0 D1 D2 D3 D4 D5 D6 D7
CX=0000 SI=0000 SS=3052
DX=0000 DI=0000 ES=0000
*asm 12
12: main ()
2FD3:0000 56 PUSH SI
2FD3:0001 57 PUSH DI
2FD3:0002 55 PUSH BP
2FD3:0003 8BFC MOV BPSP
2FD3:0004 5E CSD completed
  
```

pled with our ES 1800 emulator. You can use commands to examine variables on the fly, check contents of registers, and determine current position in code. And real-time trace is displayed as source level statements, machine instructions or bus cycles.

The packages also include a logic state analyzer probe, and provide up to 2 Megabytes of overlay memory plus full protect mode support for the 80286.

Source Level Debugging for Motorola Microprocessors

The window-oriented VALIDATE/XEL package combines our XEI source-level debugger, a simulator and the MCC68K compiler with our ES 1800



Also included are a logic state analyzer probe; the SCSI option for increasing download speeds by up to 30 times; plus up to 2 Megabytes of overlay memory.

To find out more about 8, 16 or 32-bit development solutions that save money in the long run, write Applied Microsystems Corp., P.O. Box 97002, Redmond, WA 98073-9702. Or call 1-800-426-3925 (In Washington, call 206-882-2000).

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```

1 count 0
2 ptr 04E724E72
3 ptr 04E724E72
4 rax[count] 0000

TRACE 0: 00000120 TURINGSTART

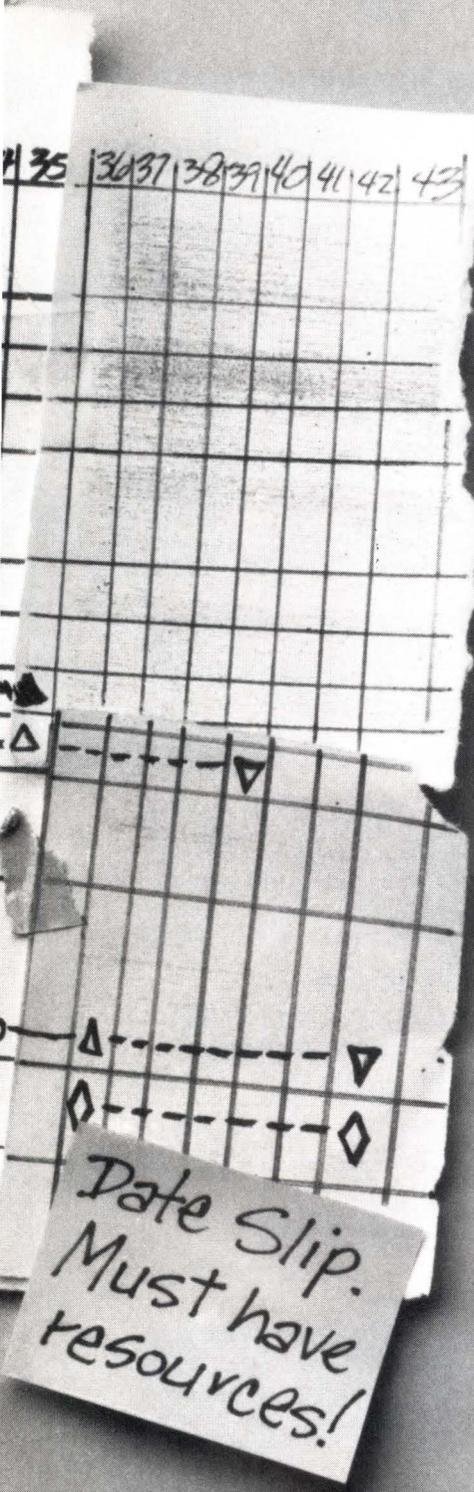
CODE
12 for (i = 0; ptr = &tape[i]; i < TAPE_SIZE; i++)
14   ptr++ = 0; /* Clean the tape */
15   state = E; /* Starting state */
16   count = 0; /* Initial count */
17
18   ptr = &tape[TAPE_SIZE / 2]; /* Start in the middle */
19   do {
20     switch (state) {
21       case E:
22         if (*ptr == 'T')
  
```

emulator. The package also includes a logic state analyzer probe and our well-known SCSI interface option, that significantly decreases download time.

In addition to up to 2 Megabytes of overlay memory, you get target control from your source code; powerful "C" language macros for code patching,



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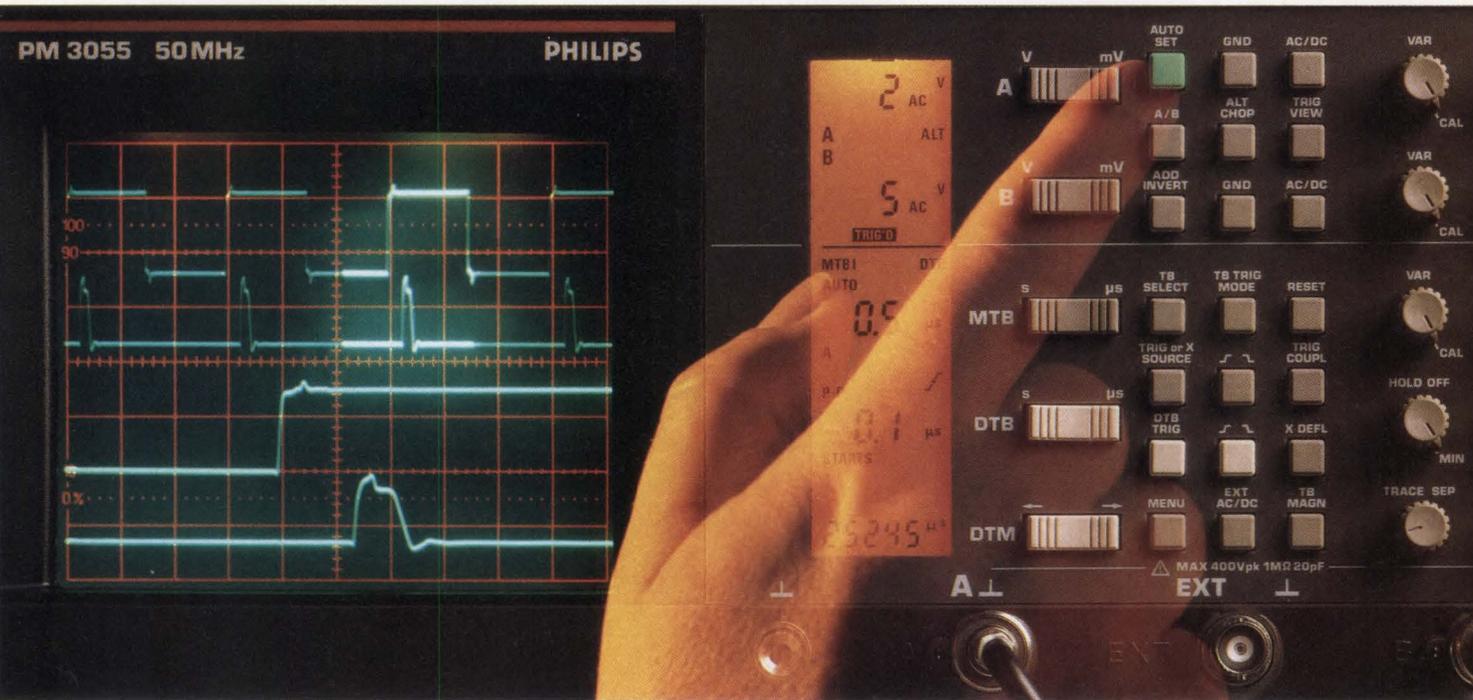
development tools available.

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NEWS BREAKS

EDITED BY JOANNE CLAY

SMD/SME DISK CONTROLLER FITS SUN WORKSTATIONS

Capable of controlling as many as four SMD/SME disk drives with serial data rates as high as 24 MHz and burst data rates in excess of 30M bytes/sec, the Rimfire 3220 VME Bus controller from Ciprico (Plymouth, MN, (612) 559-2034) also plugs directly into your Sun workstation without an intervening adapter card. The 3220 has the same 367×400-mm dimensions that Sun's triple-high, triple-wide plug-in cards have. This controller has an 80186 μ P for cache control, a 512k-byte configurable cache memory that prereads data across track and cylinder boundaries, and as many as seven circular command queues that provide a software interface for communication with Sun's SunOS or the Unix BSD 4.2 operating system. You can purchase single units for \$3495.—J D Mosley

MORE COMPANIES JUMP ONTO THE RISC BANDWAGON

MIPS Computer Systems (Sunnyvale, CA, (408) 720-1700), creator of the R2000 RISC-based μ P, has licensed Integrated Devices Technology (Santa Clara, CA, (408) 727-6116), Performance Semiconductor (Sunnyvale, CA, (408) 734-9000), and LSI Logic (Milpitas, CA, (408) 433-8000) to build the device. Performance Semiconductor and IDT will produce off-the-shelf products; LSI Logic will make the R2000 available as a standard product and also include it in its library for custom applications. All three licensees will be marketing MIPS Computer Systems' advanced RISC (reduced instruction set computer) software environment along with the chip set. The chip set consists of the CPU and a floating-point coprocessor. You can expect the devices to be in production by mid-1988.—David Shear

BYTE-WIDE STATIC RAM SPECS 85-NSEC ACCESS TIME

To cut down on the amount of clocking or timing logic in your next design, consider using the 256k-bit MCM60256 CMOS static RAM from Motorola (Austin, TX, (512) 928-6705). Organized as 32k 8-bit words, Motorola's 256k-bit MCM60256 CMOS static RAM has two separate chip-enable pins to accommodate either active-low or active-high signals. An optional low-power version of this chip also provides a power-saving mode. Housed in a 28-pin, 600-mil DIP, this memory device is pin compatible with the manufacturer's 2764 EPROM family. You can order these devices with 85-, 100-, or 120-nsec access times. Prices range from \$18.78 (500) for the 120-nsec, standard-power model to \$27.03 (500) for the 85-nsec, low-power version.—J D Mosley

HYBRID INCORPORATES PLD TO RESURRECT OBSOLETE IC

When National Semiconductor (Santa Clara, CA, (408) 721-5000) made its DM8512 flip-flop obsolete, the company inadvertently destroyed the original artwork, without which no more of the devices could be manufactured. Unfortunately, at least one company needed that IC to maintain existing government systems; a 20-pin PLD would not fit into the original 16-pin socket. To solve the problem, Cer-Tek (El Paso, TX, (915) 778-1555) incorporated both a 74LS74 and a PAL14H4 die in one package, creating a hybrid circuit that's compatible with the original device. National Semiconductor supplies preprogrammed PLD dies to Cer-Tek for the hybrid. L J Floyd, Cer-Tek's president, estimates that his company can create similar replacements for other obsolete parts for less than \$20 (1000).—Steven H Leibson

NEWS BREAKS

PIN-COMPATIBLE FLOATING-POINT CHIP SET

Integrated Device Technology (Santa Clara, CA, (408) 727-6116) has introduced a floating-point chip set that's pin compatible with the Weitek 1264/1265. The IDT721264/IDT721265 chip set uses a 30-nsec clock to perform 32- and 64-bit ALU operations at 16.7M flops, 32-bit multiplications at 16.7M flops, and 64-bit multiplications at 8.3M flops. Besides including the Weitek standard ALU functions, the chip set has an instruction that supports the Newton-Raphson algorithm. Each device comes in a 144-lead pin-grid array; the chip set costs \$406 (100).—David Shear

PATTERN GENERATOR TEAMS UP WITH YOUR LOGIC ANALYZER

The PI-6500 pattern generator from Pulse Instruments (Torrance, CA, (213) 515-5330) can provide any logic analyzer with stimulus and response capabilities. The pattern generator offers a maximum of 48 channels with 4k bits of pattern memory behind each channel. For applications requiring deeper pattern memory and fewer channels, you can chain groups of 16 channels together to obtain three channels with 64k bits each of pattern memory. The pattern generator's clock rates can vary from 760 Hz to 25 MHz, allowing you to generate timing sequences with 40-nsec resolution. The skew between any two channels is less than 4 nsec. The output levels are TTL compatible, and they can be 3-state.

You can define as many as 4k subpatterns from the basic pattern memory and then use those subpatterns in a pattern-control program. The triggering function can use the immediate mode or the latched mode; the latched mode waits one to 16 clock periods before triggering on the data. The trigger reactions require nine clock periods plus 170 nsec before the output changes state. The occurrence of a trigger event also produces as many as 256 different flag events that you can use to control your logic analyzer or other functions external to the pattern generator. The pattern generator has 256k bytes of nonvolatile RAM to store patterns and programs. An optional IEEE-488 or RS-232C interface card lets you generate patterns on a computer and send them to the pattern generator. The PI-6500 starts at \$7475.—Doug Conner

ADAPTER CONVERTS 68-PIN PGA TO PLCC

If you're developing a design that will incorporate a device in a 68-lead plastic leaded chip carrier (PLCC), but you can only obtain the device in pin-grid arrays (PGAs), the 308-1846-XX Series adapter from Methode Electronics Inc (Chicago, IL, (312) 867-9600) can solve your problem. The top of the adapter accepts a 68-pin PGA; PLCC leads protrude from the bottom. The adapter is available in 10x10 and 11x11 grid patterns and costs \$265 in production quantities.—Steven H Leibson

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CIRCLE NO 143

NEWS BREAKS: INTERNATIONAL

SUBASSEMBLY EASES SOLID-STATE CAMERA DESIGN

To simplify the design of cameras for surveillance and machine-vision systems, Philips' Component Div (Eindhoven, The Netherlands, TLX 51573) has introduced a camera subassembly that incorporates the company's monochrome solid-state image sensor. In addition to the image sensor, the subassembly includes all the drive, preprocessing, video-processing, and power-supply circuitry necessary to produce a 1V p-p composite-video output. To produce a complete camera, you need only add a suitable lens and camera housing. Options for the subassembly include interlaced or noninterlaced operation, automatic or computer-controlled gain, automatic iris control, internal or external synchronization, and switchable gamma compensation. Versions are available for 525- or 625-line TV systems that meet EIA or CCIR standards. Built on a semirigid pc board, the subassembly folds down to 89×40×45 mm. In OEM quantities, the subassembly starts at around DM 600.—Peter Harold

GRAPHICS ADAPTER DRIVES VIDEO MONITORS AND LASER PRINTERS

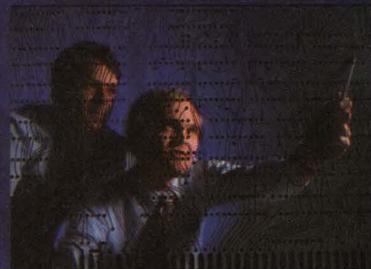
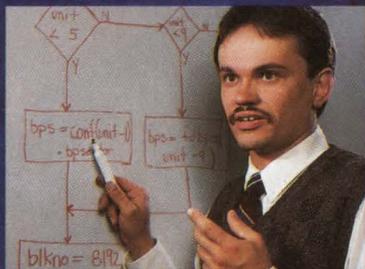
Based on a 20-MHz, 32-bit Inmos T414 or T800 Transputer, the Vincent graphics adapter from Simulation Technology (Oslo, Norway, FAX (02) 156051) provides IBM PC/AT computers with high-resolution graphics and image-processing capabilities. The \$6000 board has as much as 1.5M bytes of video RAM and a color look-up table; it allows you to display 256 gray-scale levels or 256 colors from a palette of 16M colors. Additional on-board RAM (as much as 4M bytes) provides program and data storage, as well as temporary buffers for image information. The board supports screen resolutions as high as 1600×1280 pixels, and most of the video-output characteristics—including the vertical and horizontal scan rates, the number of dots per line, and the number of lines per frame—are software programmable. The board has an AT-bus interface that can operate at 800k bytes/sec. The board's plug-in crystal oscillators allow you to operate it at dot rates as high as 120 MHz. In addition to its RGB video output, the board also has a Canon/PelBox interface for a laser printer or phototypesetter.—Peter Harold

As it appeared in the December 26, 1987, issue, the following item contained some inaccuracies, which made it misleading. The corrected version follows.

STEPPER-MOTOR DRIVERS EASE INTERFACE TO MICROCONTROLLERS

The MTC6017 stepper-motor driver from Mietec (Oudenaarde, Belgium, TLX 85739) is an H-bridge driver that's suitable for controlling the current in one winding of a bipolar stepper motor. Although it's similar to the industry-standard 3717-type driver, the MTC6017 has control codes for its two current-control inputs that maintain a direct (but nonlinear) relationship with the winding current, thereby simplifying control firmware. The driver also includes an on-chip 5V reference for the current-sense comparators. Another device, the MTC6018, targets microstepping applications; it provides a 6-bit on-chip D/A converter for winding-current control. The MTC6017 and MTC6018 will cost around \$2.20 and \$2.50, respectively. They're slated for introduction during the first and the second quarter of 1988, respectively.—Peter Harold

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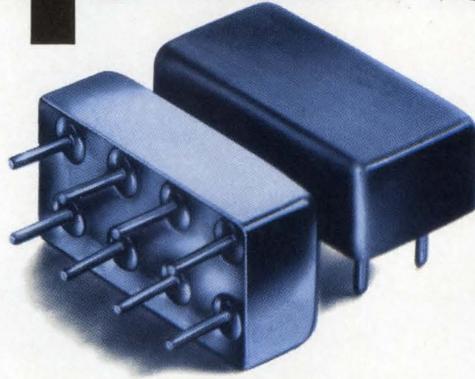
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MAN-2	0.5-1000	19	1.5	7	6.0	85	15.95
MAN-1LN	0.5-500	28	1.0	8	2.8	60	15.95
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††Midband $10f_L$ to $f_{U/2}$, $\pm 0.5\text{dB}$ †IdB Gain Compression ◊Case Height 0.3 In.
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LOW PASS	Model	*LP-	10.7	21.4	30	50	70	100	150	200	300	450	550	600	750	850	1000
Min. Pass Band (MHz) DC to			10.7	22	32	48	60	98	140	190	270	400	520	580	700	780	900
Max, 20dB Stop Frequency (MHz)			19	32	47	70	90	147	210	290	410	580	750	840	1000	1100	1340

Prices (ea.): P \$9.95 (6-49), B \$24.95 (1-49), N \$27.95 (1-49), S \$26.95 (1-49)

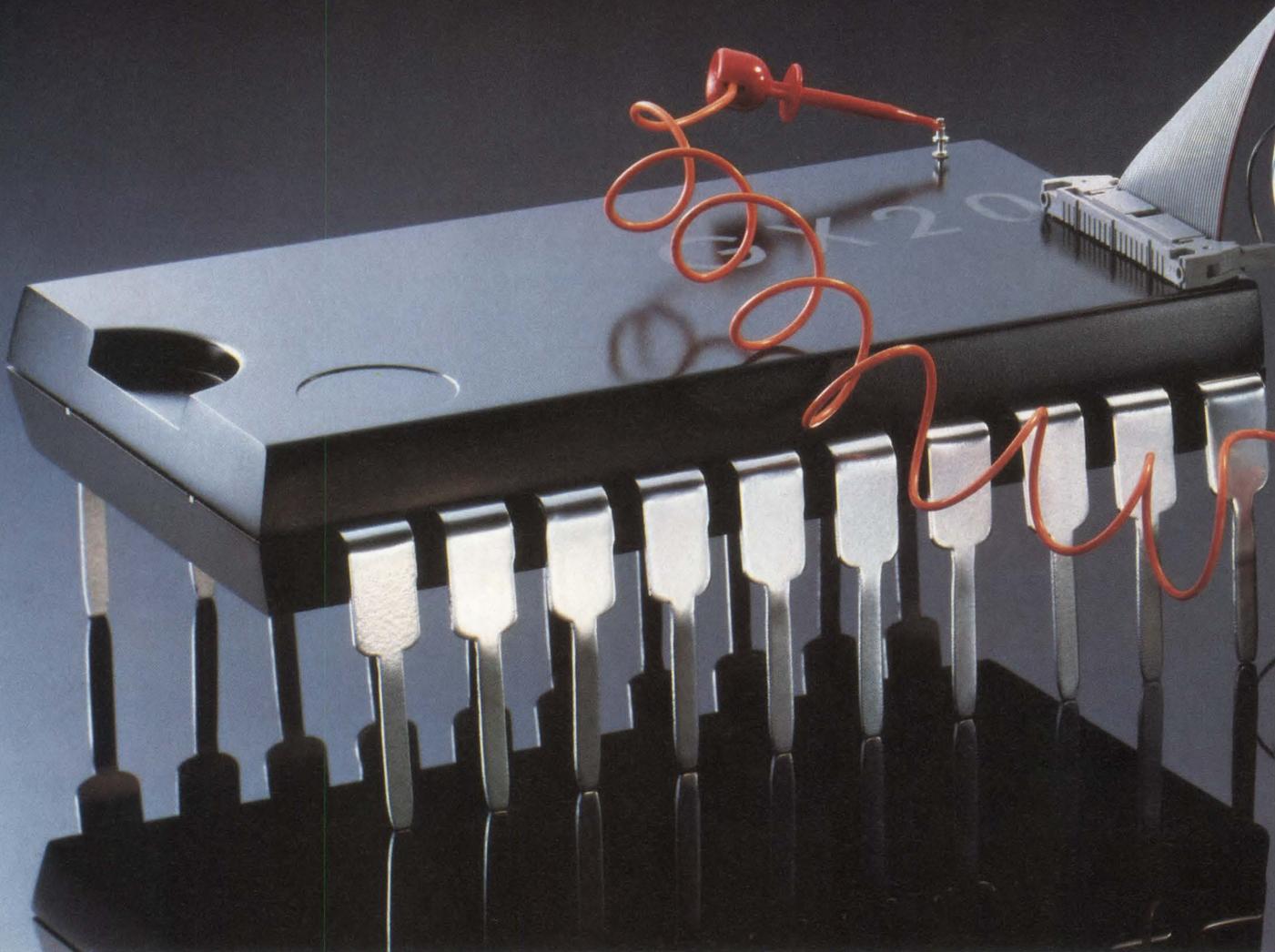
HIGH PASS	Model	*HP-	50	100	150	200	250	300	400	500	600	700	800	900	1000
Pass Band (MHz)	start, max.		41	90	133	185	225	290	395	500	600	700	780	910	1000
	end, min.		200	400	600	800	1200	1200	1600	1600	1600	1800	2000	2100	2200
Min. 20dB Stop Frequency (MHz)			26	55	95	116	150	190	290	365	460	520	570	660	720

Prices (ea.): P \$12.95 (6-49), B \$27.95 (1-49), N \$30.95 (1-49), S \$29.95 (1-49)

*Prefix P for pins, B for BNC, N for Type N, S for SMA *example: PLP-10.7*

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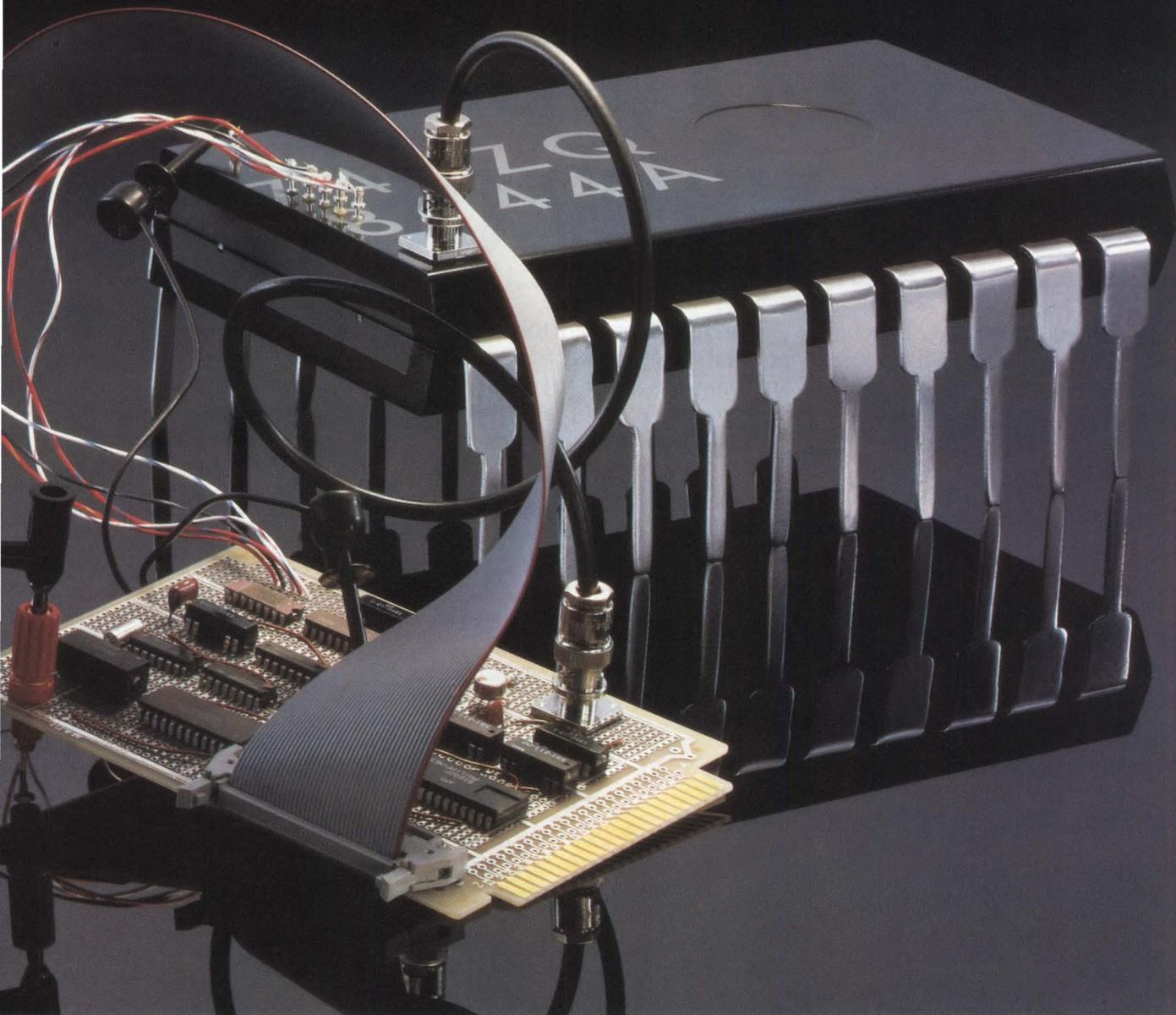
With AVLSI devices you won't get fast design feedback, unless you test individual components—the

"building blocks" of system silicon. And you won't comply with customer and industry requirements if you don't do complete "system" functional testing. With conventional test systems it means two of everything. Two testers, two test programs, two insertions, two data bases. And more than twice the time to get to market.

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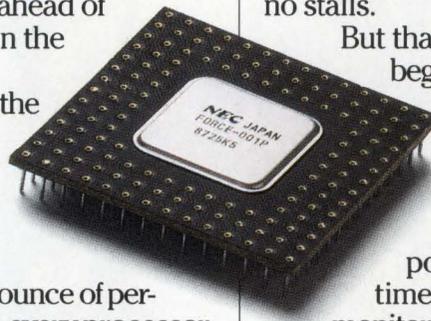
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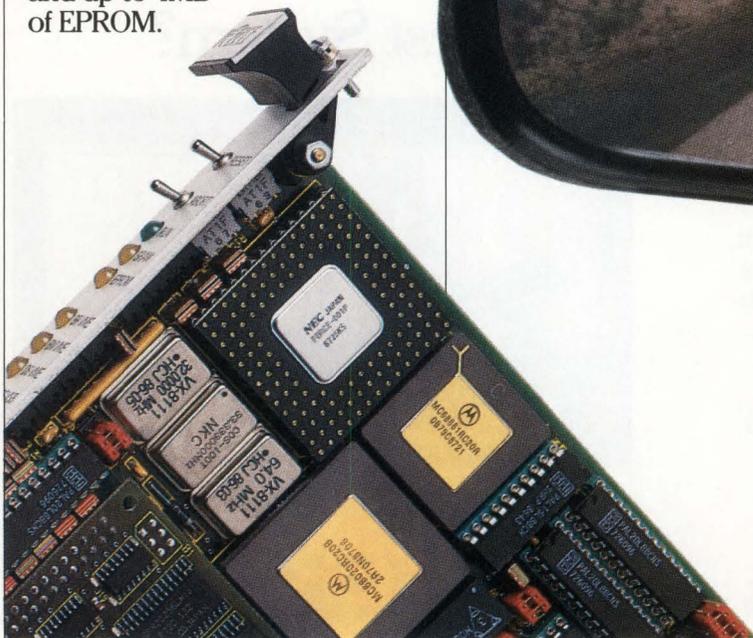
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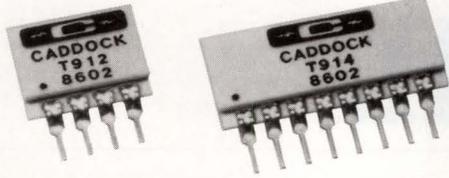
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Precision and Ultra-Precision Resistor 'Pairs' and 'Quads' deliver a selection of Ratio Tolerance to as tight as $\pm 0.01\%$ and Ratio Temperature Coefficient to 2 PPM/ $^{\circ}$ C combined with exceptional long-term stability.

Standard Type T912 and T914 Precision and Ultra-Precision Resistor Networks.

Standard models of the Type T912/T914 Precision and Ultra-Precision Resistor Networks combine all of these performance characteristics:

- **Absolute Tolerance:** 0.1% for all resistors.
- **Ratio Tolerances:** 0.1%, 0.05%, 0.02% and 0.01%
- **Ratio Temperature Coefficients:** from 10 PPM/ $^{\circ}$ C to 2 PPM/ $^{\circ}$ C.
- **Absolute Temperature Coefficient:** 25 PPM/ $^{\circ}$ C from 0 $^{\circ}$ C to +70 $^{\circ}$ C.
- **Ratio Stability of Resistance at Full Load for 2000 Hours:** within 0.01%.
- **Shelf Life Stability of Ratio for Six Months:** within 0.005%.

The standard part number below provides a selection of over 500 in-production models of Type T912/T914 precision and ultra-precision 'pairs' and 'quads':

Model Number: T912 - A 10K - 010 - 10

Ratio Code Letter:

A - T912 with $R_1 = 10R_2$
(Example: 1K - 10K)

B - T912 with $R_1 = 9R_2$
(Example: 1K - 9K)

No Letter - T912 with $R_1 = R_2$

No Letter - T914 with $R_1 = R_2 = R_3 = R_4$

Ratio Temperature Track: (0 $^{\circ}$ C to +70 $^{\circ}$ C)

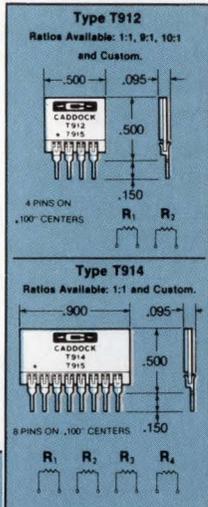
-10 = 10PPM/ $^{\circ}$ C -05 = 5PPM/ $^{\circ}$ C
-02 = 2PPM/ $^{\circ}$ C

Ratio Tolerance:

-100 = 0.1% -020 = 0.02%
-050 = 0.05% -010 = 0.01%

Standard Resistance Values (R_1):

1K	10K	40K	200K	500K
2K	20K	50K	250K	1Meg
5K	25K	100K	400K	

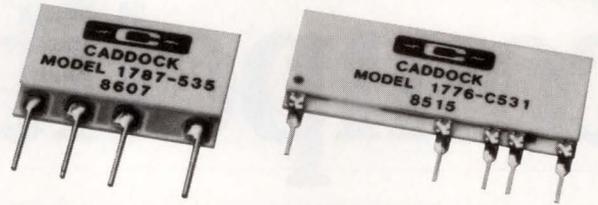
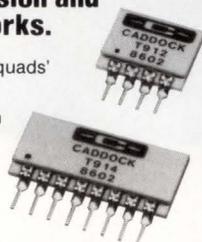


Custom Type T912 and T914 Precision and Ultra-Precision Resistor Networks.

Custom models of these precision 'pairs' and 'quads' can include these special performance features:

- **Resistance Values:** from 1K to 2 Megohms with maximum ratios of 250-to-1.
- **Absolute TC:** as low as 15 PPM/ $^{\circ}$ C.
- **Ratio TC:** as low as 2 PPM/ $^{\circ}$ C.

• For Type T912/T914 data, circle Number 201.

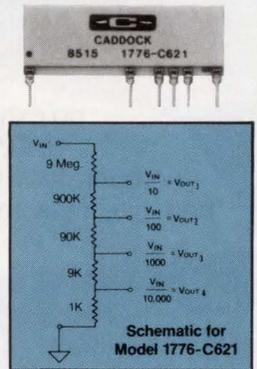


Precision Decade Resistor Voltage Dividers and Current Shunt Resistor Networks deliver many optimum combinations of precision and temperature coefficient performance for high accuracy range-switching circuitry.

Standard Type 1776 Precision Decade Resistor Voltage Divider Networks.

The Type 1776 Precision Decade Resistor Voltage Dividers provide a family of networks that includes 3, 4 and 5-decade voltage dividers with ratios from 10:1 to 10,000:1. Standard performance includes a wide range of specifications in particular combinations that meet the most often requested requirements.

- **Absolute Tolerances:** from 0.25% to 0.1%.
- **Ratio Tolerances:** 0.25%, 0.1% or 0.05%.
- **Absolute TC:** from 50 PPM/ $^{\circ}$ C to 25 PPM/ $^{\circ}$ C.
- **Ratio TC:** from 50 PPM/ $^{\circ}$ C to 5 PPM/ $^{\circ}$ C.
- **Voltage Coefficient:** As low as 0.02 PPM/Volt.



With 36 standard models to choose from, each circuit designer can specify the exact levels of performance required by each application.

• For Type 1776 data, circle Number 202.

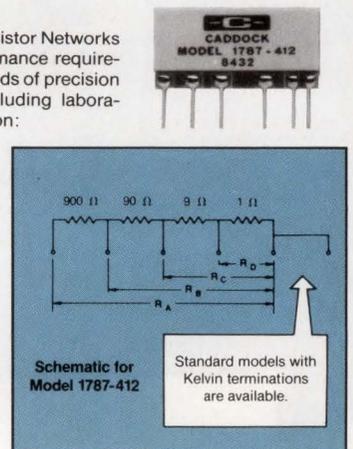
Standard Type 1787 Precision Current Shunt Resistor Networks.

The Type 1787 Current Shunt Resistor Networks achieve the combination of performance requirements necessary to meet the demands of precision current measurement circuits, including laboratory and bench-type instrumentation:

- **Resistance Values:** 1 ohm, 10 ohms, 100 ohms and 1000 ohms.
- **Absolute Tolerances:** 0.25%, 0.1% or 0.05%.
- **Absolute TCs:** 100 PPM/ $^{\circ}$ C, 80 PPM/ $^{\circ}$ C or 50 PPM/ $^{\circ}$ C.

There are now 12 standard models of the Type 1787 Current Shunt Resistor Networks available for 3 and 4-decade applications, and prototype quantities of many models are normally available from factory stock.

• For Type 1787 data, circle Number 203.



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Analog simulation tools

Several of our prospective customers asked that a circuit shown in EDN's May 14, 1987, Special Report (pg 138) on analog CAE be benchmarked as proof of the capability of Daisy's analog tools. According to David Shear, the article's author, all analog simulation tools would provide misleading results.

The circuit (pg 148) is a simple comparator, which, when breadboarded, exhibits instability in the form of oscillations around its switching threshold. The author correctly claims that most analog CAE systems would predict stable operation. However, the author's claim that the instability is due to the comparator's high source impedance and the lack of hysteresis is not strictly true.

In reality, all input signals and voltage rails are subject to noise. It's the noise that causes the device to oscillate when the input voltage reaches the required switching threshold, subject to the device's high input impedance, high open-loop gain, and consequent lack of hysteresis.

By introducing a noise source into the input waveform, you can reproduce the comparator's unstable operation. The accompanying Fig 1 depicts the schematic representation of the comparator circuit.

In Fig 2, the comparator output switches between positive and negative saturation when subjected to a noisy sawtooth input waveform; in other words, it's a "zero-crossing"

detector. On closer examination of the output, you see that the simulation successfully shows the many transitions expected around the threshold voltage.

This benchmark shows that an analog designer equipped with Daisy's analog CAE tools can successfully simulate a circuit to produce results comparable to those of a breadboard. It should be noted, however, that although analog CAE tools help the designer produce higher-quality designs, they don't replace engineering expertise. An inexperienced designer could produce misleading results with his simulation, but these tools will complement the skills and knowledge of an experienced designer.

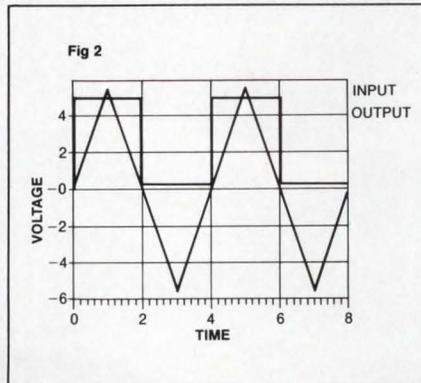
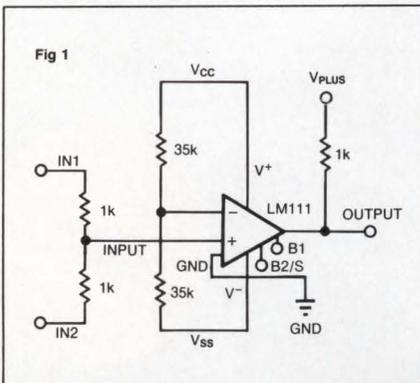
Dave Richards

*Analog Applications Specialist
Daisy Systems UK Ltd
Basingstoke, UK*

David Shear replies:

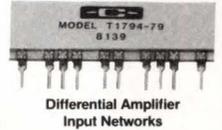
I don't believe that selectively placing noise into a circuit so that the results look like real-world results is the proper solution to the problem.

I would suggest that the addition of real-world parasitic capacitance that feeds the output back to the input would more closely match reality. Comparators have finite gain and wide bandwidth. When trying to resolve slow-moving inputs, they will, for a short time, be in a linear region. While they're in this linear region, if any of the output feeds back to the input (via the parasitic



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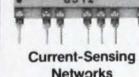
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- Ratio Tolerances: 1.0%, 0.50%, 0.25%, 0.20%, 0.10%, 0.05% and 0.025%.
- Absolute Temperature Coefficients: 50 PPM/^oC, 25 PPM/^oC and 15 PPM/^oC from 0^oC to +70^oC.
- Ratio Temperature Coefficients: 50 PPM/^oC, 25 PPM/^oC, 10 PPM/^oC and 5 PPM/^oC from 0^oC to +70^oC.
- For Type T1794 information, circle Number 204.



Type 1789 Custom Low Resistance Value Precision SIP Resistor Networks.



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- Resistance Values: from 0.5 ohms to 10,000 ohms.
- Absolute Tolerances: 1.0%, 0.50%, 0.25%, 0.20%, 0.10% and 0.05%.
- Ratio Tolerances: 1.0%, 0.50%, 0.25%, 0.20%, 0.10% and 0.05%.
- Absolute Temperature Coefficients: 100 PPM/^oC, 80 PPM/^oC and 50 PPM/^oC from 0^oC to +70^oC.
- Ratio Temperature Coefficients: 80 PPM/^oC, 50 PPM/^oC, 25 PPM/^oC and 15 PPM/^oC from 0^oC to +70^oC.
- For Type 1789 information, circle Number 205.

Caddock's high thru-put manufacturing capabilities provide cost-effective, on-time delivery of your custom resistor network requirements. Custom network designs are now in-production in quantities from 500 networks per year to as high as 500,000 networks per year.

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SIGNALS & NOISE

capacitance), oscillations will usually occur. Lowering the source resistance or using hysteresis often solves the problem.

However, the reason the comparator oscillated is not the issue. The point I was making is that the model did not predict the circuit's true operation. After building the prototype, we found a discrepancy. The model was in error. Now we are arguing about how to fix the model. Who is right? Again that is not the point.

Article neglected the IBM RT PC

I found the Special Report on workstations in the October 29, 1987, issue of EDN (pg 168) to be quite readable and generally accurate. However, I feel there is a serious omission in the list of systems shown in **Table 1** (pg 172).

Noticeable by its absence is the IBM RT PC. The RT PC's price is in the range shown, the processor is a RISC (reduced-instruction-set computer) chip developed by IBM, and the feature list certainly places the RT PC in the race.

Most impressively, however, we have found in our benchmarking that the current version of the RT PC has performance superior to most of the systems in the chart. The RT PC has performance that is generally superior to the fastest of the Motorola-based systems (25-MHz 68020 machines). The current RT PC really is a superior system that has received less notice than it deserves.

David Wilson
Workstation Laboratories
Humboldt, AZ

WRITE IN

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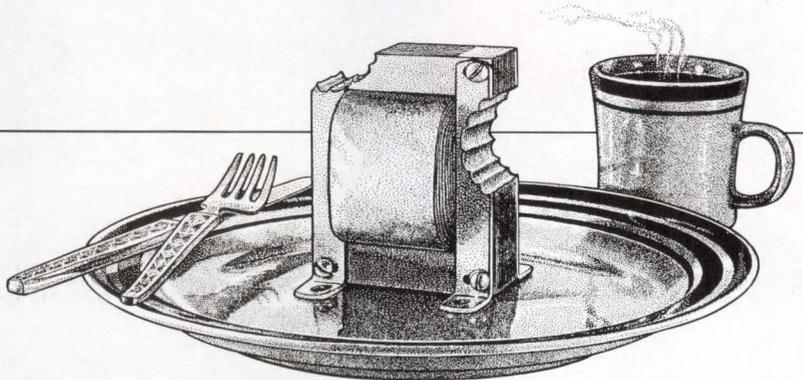
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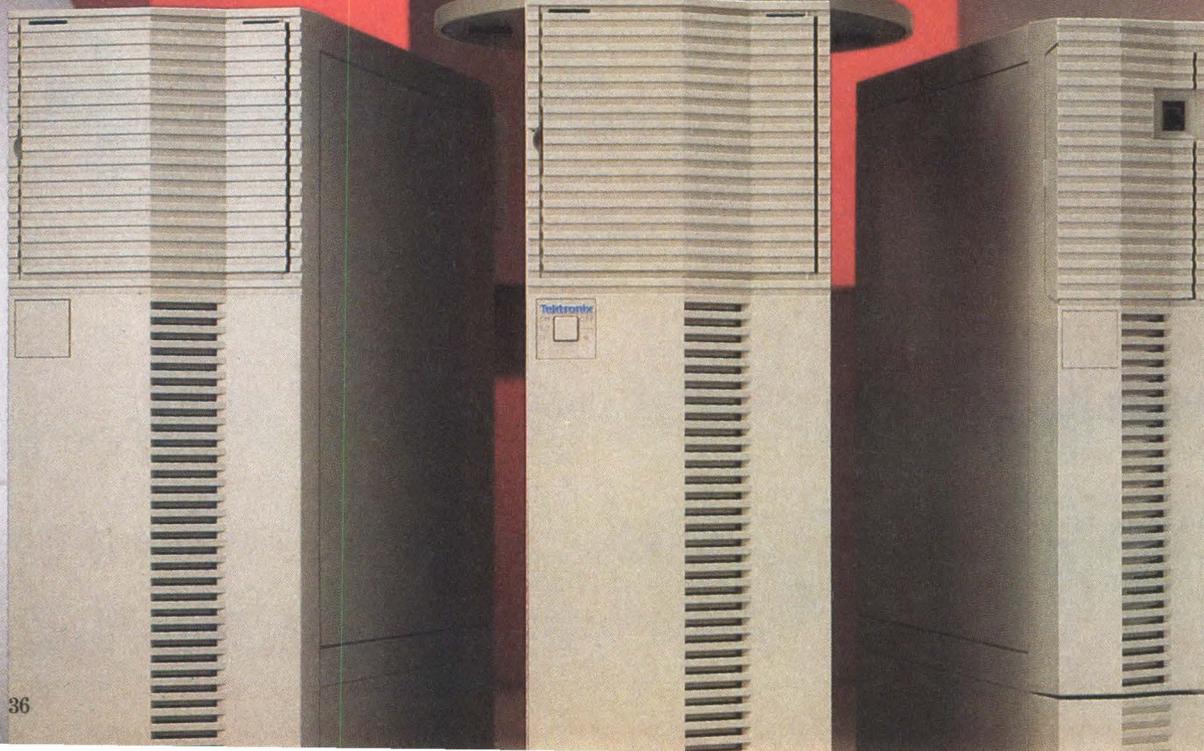
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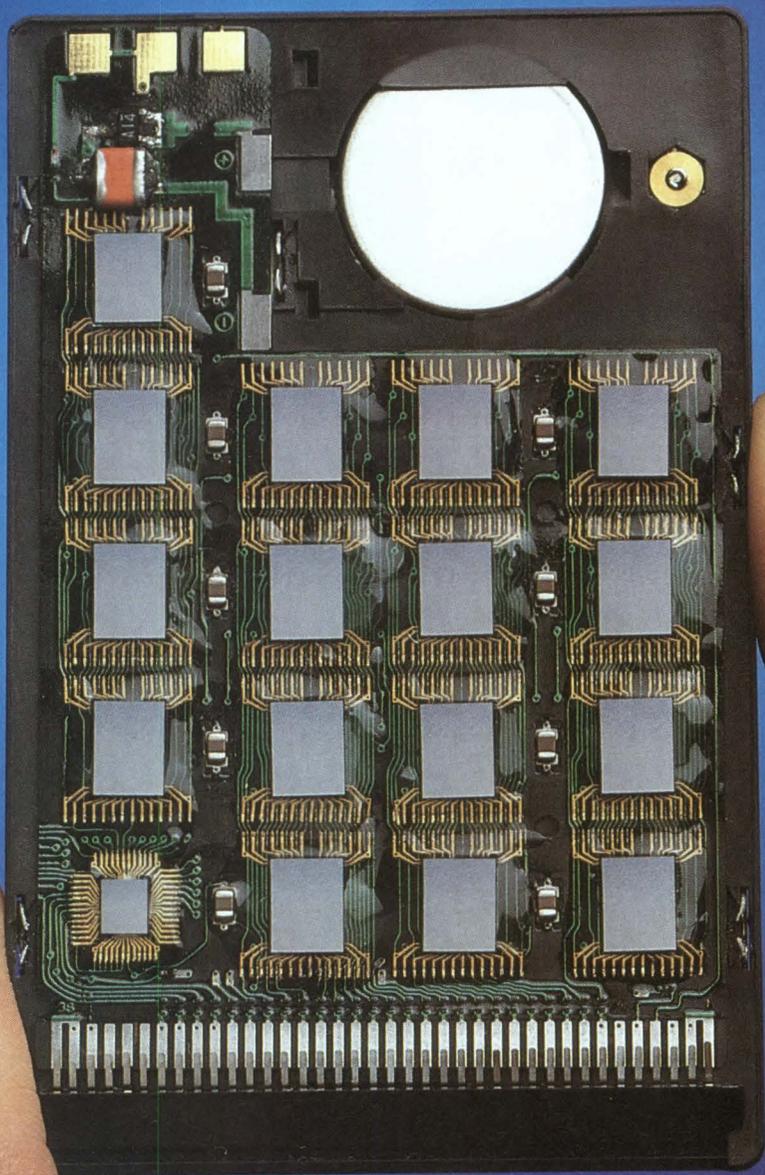
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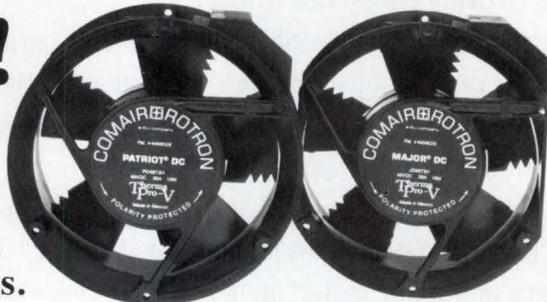
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CIRCLE NO 5

CALENDAR

Third Annual Technical Symposium on Optoelectronics and Laser Applications in Science and Engineering, Los Angeles, CA. SPIE, Box 10, Bellingham, WA 98227. (206) 676-3290. January 10.

ATE and Instrumentation Conference West, Anaheim, CA. MG Expositions Group, 1050 Commonwealth Ave, Boston, MA 02215. (800) 223-7126. January 12 to 14.

Third Annual Battery Conference on Applications and Advances, Long Beach, CA. Cecile Duong, Department of Electrical Engineering, California State University at Long Beach, 1250 Bellflower Blvd, Long Beach, CA 90840. (213) 498-4605. January 12 to 14.

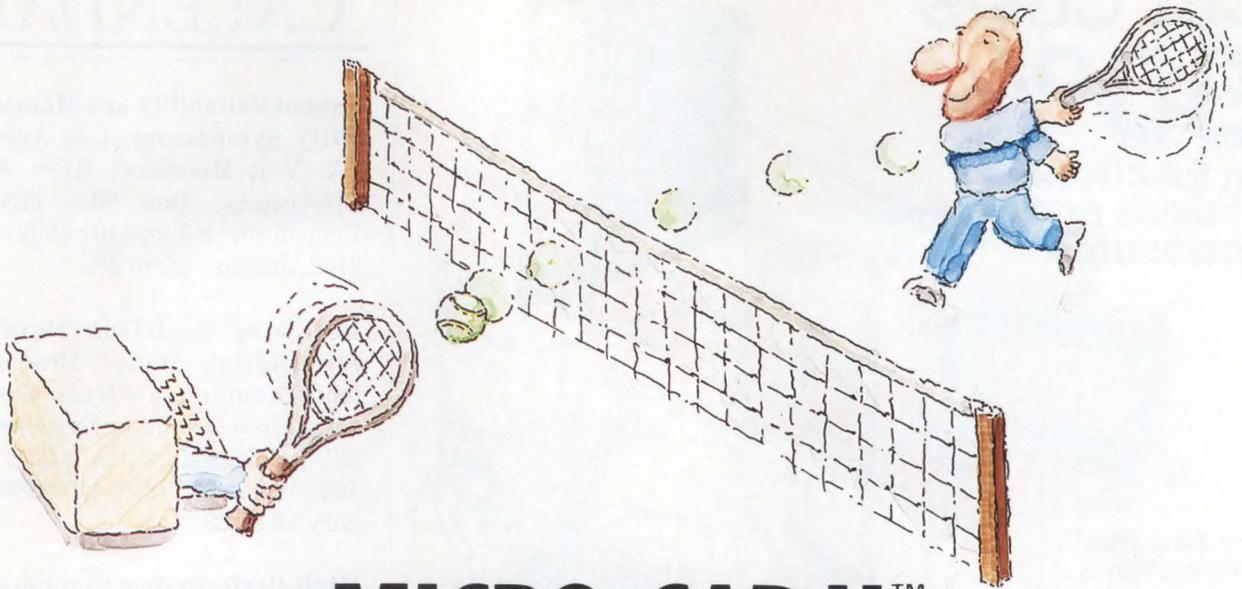
Designing Real-Time Hardware for Digital Signal Processing (short course), Los Angeles, CA. Integrated Computer Systems, Box 3614, Culver City, CA 90231. (800) 421-8166; in CA, (213) 417-8888. January 12 to 15.

Real-Time Operating Systems (short course), San Diego, CA. Integrated Computer Systems, Box 3614, Culver City, CA 90231. (800) 421-8166; in CA, (213) 417-8888. January 12 to 15.

Annual IEEE Design Automation Workshop, Apache Junction, AZ. Walling Cyre, Control Data, HQM 173, Box 1249, Minneapolis, MN 55440. (612) 853-2692. January 13 to 15.

Conference on Optical Fiber Communication (OFC '88), New Orleans, LA. Optical Society of America, 1816 Jefferson Pl NW, Washington, DC 20036. (202) 223-0926. January 25 to 27.

Neural Networks for Artificial Intelligence, Los Angeles, CA. Technology Transfer Institute, 741 10th St, Santa Monica, CA 90402. (213) 394-8305. January 25 to 27.

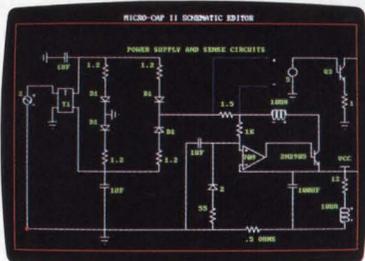


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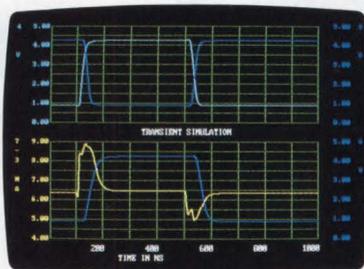
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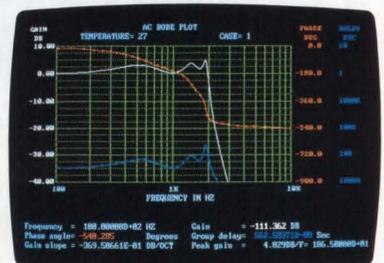
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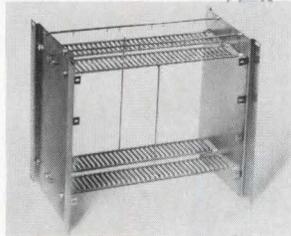
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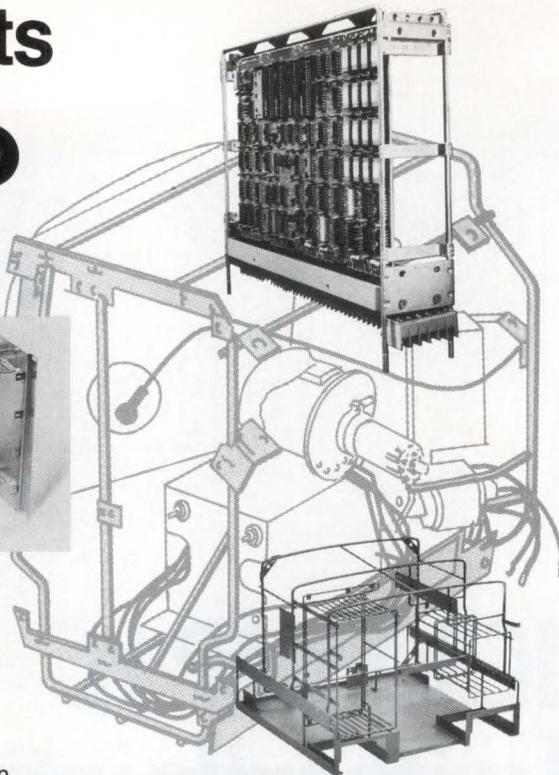
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CIRCLE NO 7

CALENDAR

Annual Reliability and Maintainability Symposium, Los Angeles, CA. V R Monshaw, RCA, Astro Electronics, Box 800, MS 55, Princeton, NJ 08540. (609) 426-2182. January 26 to 28.

Designing Real-Time Hardware for Digital Signal Processing (short course), Montreal, Canada. Integrated Computer Systems, Box 3614, Culver City, CA 90231. (800) 421-8166; in CA, (213) 417-8888. January 26 to 29.

High-Performance Computer Architectures (short course), Washington, DC. Integrated Computer Systems, Box 3614, Culver City, CA 90231. (800) 421-8166; in CA, (213) 417-8888. January 26 to 29.

APEC '88, New Orleans, LA. IEEE Power Electronics Council, 655 15th St, NW, Suite 300, Washington, DC 20005. (202) 639-4990. February 1 to 5.

Microwave Circuit Design I (short course), El Segundo, CA. UCLA Extension, 10995 Le Conte Ave, Los Angeles, CA 90024. (213) 825-3344. February 1 to 5.

High-Performance Computer Architectures (short course), Los Angeles, CA. Integrated Computer Systems, Box 3614, Culver City, CA 90231. (800) 421-8166; in CA, (213) 417-8888. February 2 to 5.

Microwave Circuit Design II (short course), Los Angeles, CA. UCLA Extension, 10995 Le Conte Ave, Los Angeles, CA 90024. (213) 825-3344. February 8 to 12.

Unix Technical Conference, Dallas, TX. Usenix Conference Office, Box 385, Sunset Beach, CA 90742. (213) 592-1381. February 9 to 12.

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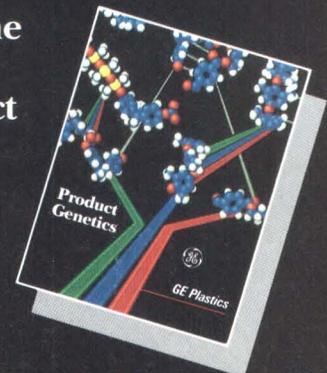
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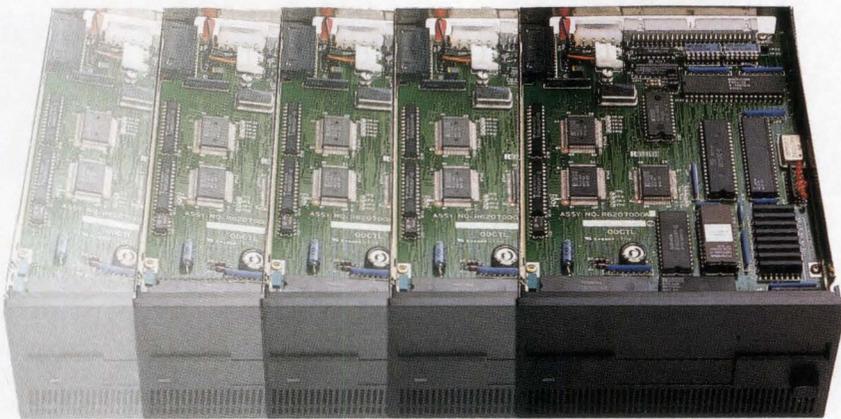
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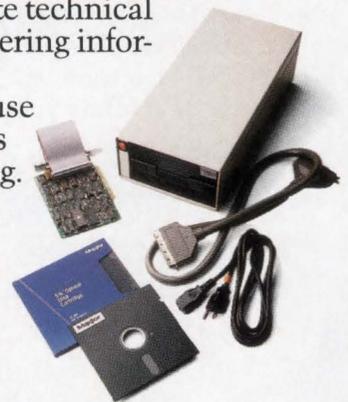
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CIRCLE NO 33

EDITORIAL

Standards aren't always standard



I'm glad my local hardware store stocks standard hardware. If manufacturers developed their own fittings, nuts, and bolts, mechanical repairs and projects would be impossible. The same is true in electronics. Standard component values and packages make designing circuits easier. However, as electronic systems become more complex, standards become less standard, which leads to trouble.

In the early days of microcomputers, the S-100 Bus became a de facto standard. However, that standard meant different things to different suppliers. Undefined bus signals and timing relationships often led to chaos as suppliers defined signals to meet their own needs. Users could spend days debugging a system after simply exchanging one CPU board for another. The IEEE finally standardized the S-100 Bus specification—just when the bus's popularity plummeted.

Even the availability of an industry-wide standard doesn't guarantee compatibility. Anyone who has connected RS-232C-based devices can attest to the standard's transformation into an ever-present nightmare. Almost everyone has his own interpretation of what RS-232C signals do.

More-complex standards lead to more-complex problems. For example, even on the fairly simple STD Bus, you can't always exchange one CPU card for another. Cards compatible with a 68000-based CPU board may not work with a Z80-based CPU card. Even the well-thought-out VME Bus has its problems. Why else would there be interest in setting up laboratories to test VME Bus products?

Software has its own set of problems. Although the Basic and C languages are fairly standard, there are enhancements and extensions galore. Such additions may make it difficult for users to make their individual versions compatible with future language standards. Even among so-called "MS-DOS-compatible" PCs, software-compatibility problems persist. Programs that run on one computer may not run on another.

The problem of standardization hasn't spared the automotive sector, either. Although General Motors established the Manufacturing Automation Protocol (MAP) standard, it has already made major revisions. MAP users may be comforted to know that the MAP Group Steering Committee says that there will be no major change in the standard for six years. However, the committee envisions "minor" changes, so although you won't see version 4 soon, you may find version 3.1 or 3.2 around the corner.

In sum, although standards are useful and good for the electronics industry, it's wise to use caution when adopting them and remember that they're only a starting point.

Jon Titus
Editor

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CA3318E/3318CE	8	15M	150	24	38.50/24.00
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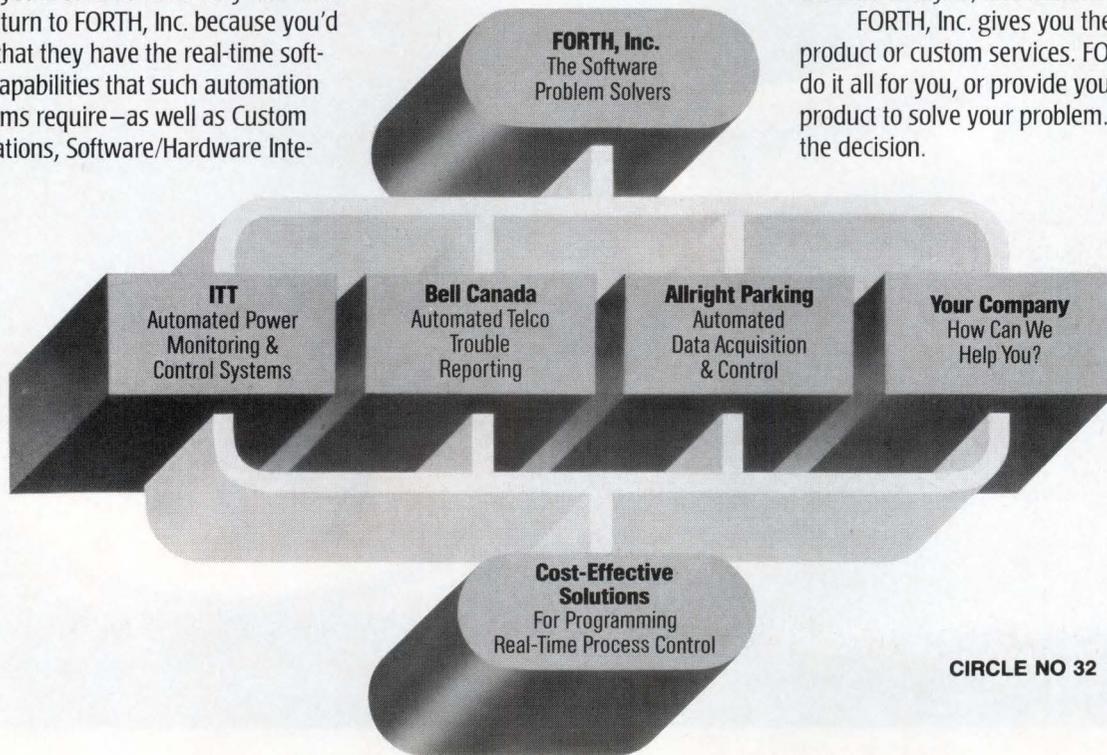
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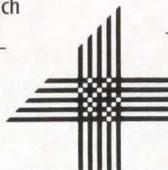
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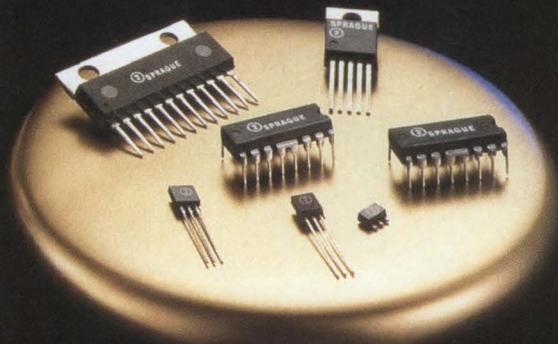
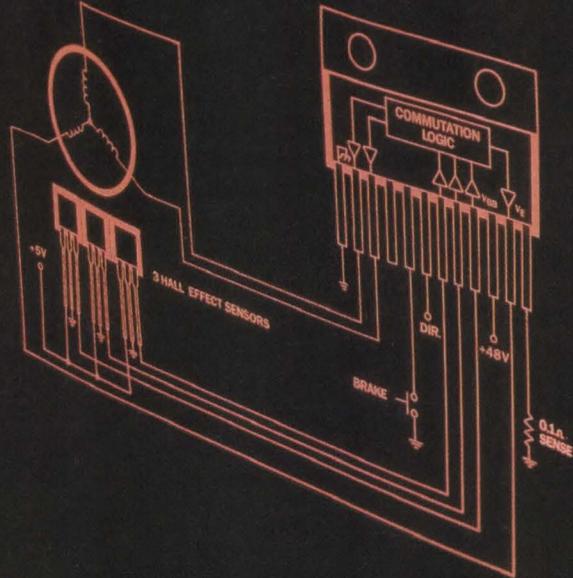
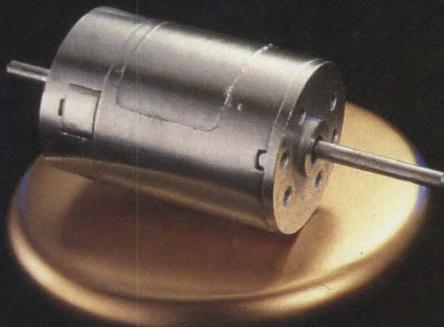
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TECHNOLOGY UPDATE

Telecomm ICs offer improved functions for telephone- and PABX-system designs

Dave Pryce, *Associate Editor*

The latest offerings from telecomm-IC manufacturers not only continue the general trend toward higher integration by incorporating more functions than previous telecomm ICs did—they also substantially improve on those functions. Many of these just-introduced telecomm ICs offer economical ways to upgrade your telephone and PABX designs.

In the last few years, ICs have taken over many telephone and PABX functions that were previously performed by electromechanical circuitry. In telephone handsets, for example, the bulky electromagnetic bell has gone the way of the dinosaur, relegated to extinction by monolithic tone ringers that drive a small permanent-magnet speaker or a piezoelectric transducer. Speech amplification, in conjunction with other functions on the same IC, has allowed designers to replace the carbon-granule microphone with a more reliable dynamic type. Monolithic pulse- and tone-dialer ICs now replace the archaic rotary dialing mechanism, and speakerphone ICs now let designers create compact systems that permit hands-free conversations.

For PABX applications, monolithic SLICs (subscriber-line interface circuits) provide a number of functions, including the replacement of the hybrid transformer that's normally required for the 2- to 4-wire conversion. For trunk-line and central-office applications, which have tougher specifications for longitudinal balance, you can find monolithic ICs that employ magnetic compensation to reduce the size and cost of the transformer. And at least two very recent ICs let you eliminate the



Forming the basis for a complete telephone, this module from Rohm includes a DTMF dialer, a speech network, and a tone ringer.

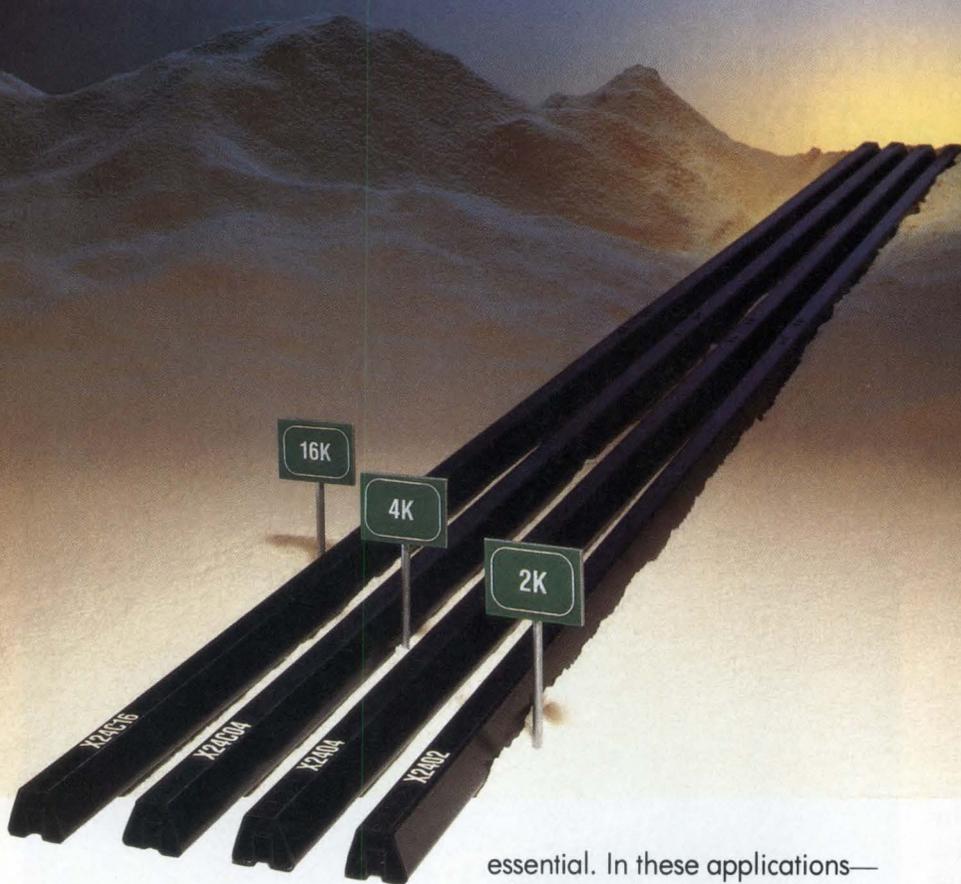
transformer in even the toughest applications.

Of the early tone ringers that replaced the electromagnetic bell in telephones, the most successful was probably the ML-8204 from Mitel, which was later offered by a number of alternate-source suppliers. Literally millions of these ICs were used in inexpensive telephones during the phone glut between 1983 and 1985. This chip had shortcomings, however. It couldn't easily drive a piezoelectric transducer, and it required an external bridge rectifier

and zener diode to interface with the phone line.

The ZN488E from Ferranti solves both of these problems, as well as providing other features. The ZN488E (Fig 1) includes an on-chip bridge rectifier for direct-line operation, and you can use this IC with either piezoelectric or magnetic transducers. A standard 560-kHz ceramic resonator controls the clock-oscillator frequency, and internal frequency dividers provide selectable output frequencies of either 1000 and 1250 Hz or 1167 and

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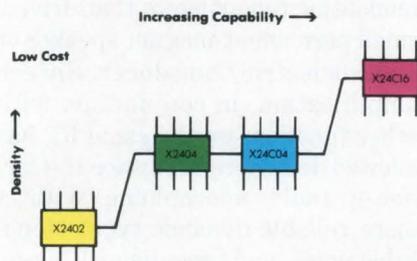
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1333 Hz. The IC switches between the selected frequencies at a 10-Hz rate to generate a warbling ringing tone. A key feature of the ZN488E is its excellent dial-pulse rejection, which is accomplished by means of internal digital filtering. Housed in an 8-pin plastic DIP, the device costs \$1.35 (1000).

Although it's not a tone ringer per se, the TCM1520A from Texas Instruments detects the ringing signal from the telephone line and converts it to an output suitable for driving an optocoupler or TTL, NMOS-logic, or CMOS-logic device. The TCM1520A will work with either isolated or nonisolated supplies. It's used principally in feature phones and autoanswer modems to activate other equipment after a specified number of rings. In a typical application, the device is activated by the telephone line ringing voltage of 40 to 150V at 16 to 68 Hz. The IC provides an inverting output for driving external logic. Packaged in an 8-pin DIP, the TCM1520A costs \$1.01 (100).

Listen to the tones

The replacement of the rotary dialing mechanism with pushbuttons has brought with it a number of

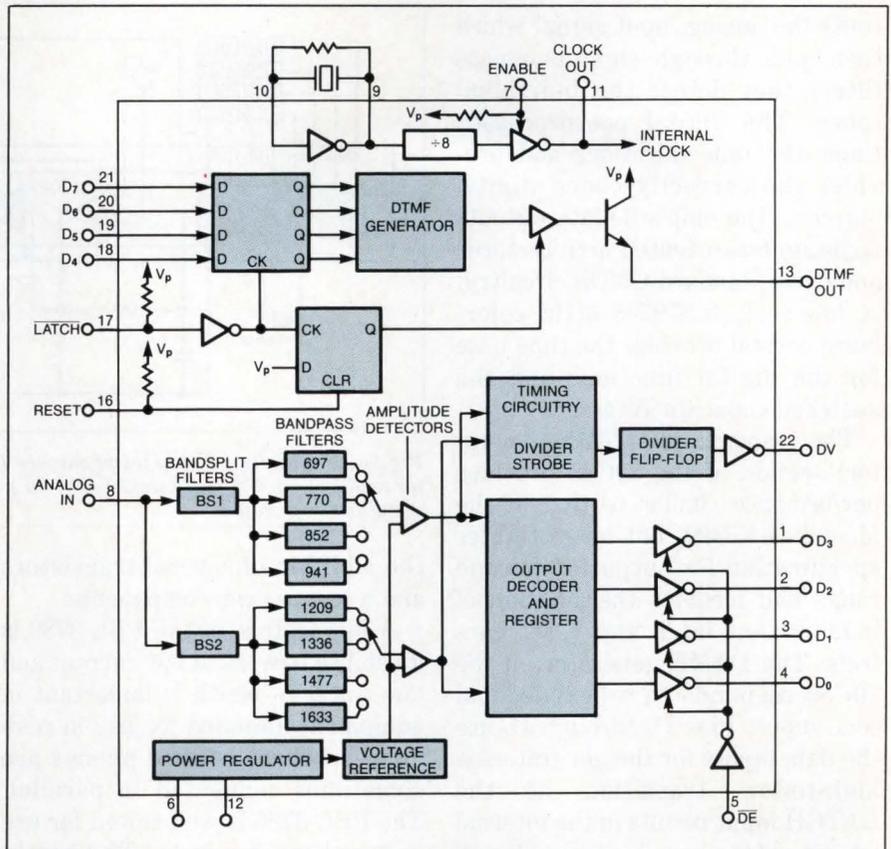


Fig 2—For DTMF transceiver applications, the SSI-20C89 from Silicon Systems generates and detects all 16 standard DTMF signals. The circuit provides a microprocessor interface for tone-signal generation.

monolithic ICs that replicate the dial pulses or generate DTMF (dual-tone multiple-frequency) signals (as in AT&T's Touch Tone phones). Al-

though pulse-dialing applications are rapidly fading as the telephone networks switch over to DTMF, a number of manufacturers such as Gould/AMI, Mostek, Plessey, and SGS still supply ICs for pulse dialing. The 2560-type device, for example, is still popular and is available from several suppliers. For DTMF applications, manufacturers of telephone ICs offer a variety of products, such as the PCD3310 from Philips and Signetics, which provides both pulse- and DTMF-dialing functions.

Silicon Systems offers a complete circuit for DTMF applications. Its SSI-20C89 chip is actually a transceiver that not only generates and detects all 16 standard DTMF codes but also provides a microprocessor interface. The DTMF receiver section of the SSI-20C89 (Fig 2) detects the presence of a valid tone pair on the telephone line, indicating a single dialed digit. Pin 8 ac-

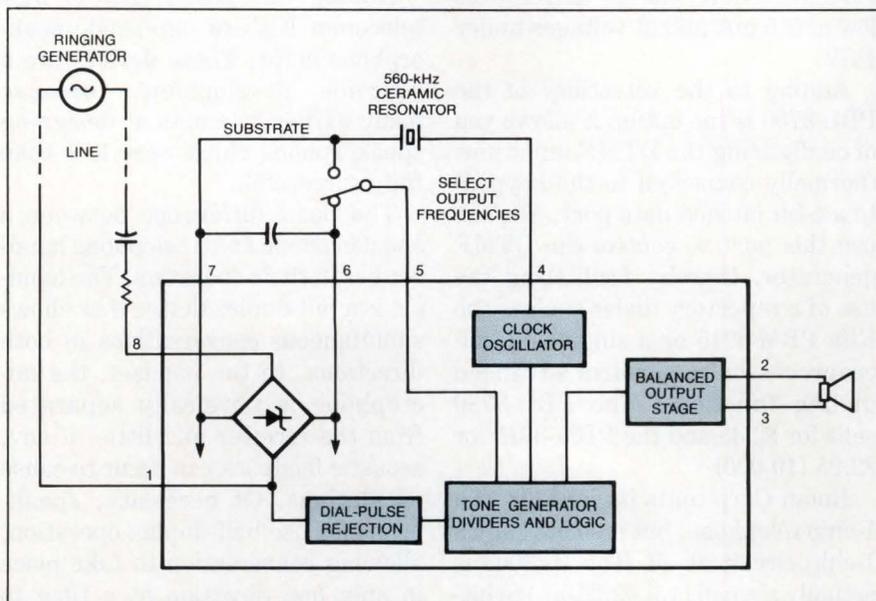


Fig 1—Able to drive either piezoelectric or magnetic transducers, the ZN488E tone ringer from Ferranti includes an on-chip bridge rectifier for direct-line operation.

TECHNOLOGY UPDATE

cepts the analog input signal which then goes through eight bandpass filters that detect the individual tones. The digital postprocessor times the tone durations and provides the correctly coded digital outputs. The chip's 3-state outputs facilitate bus-oriented architectures and drive standard CMOS circuitry. A low-cost, 3.579545-MHz colorburst crystal provides the time base for the digital functions and the switched-capacitor filters.

The transmitter (DTMF generator) section of the 20C89 provides performance similar to that of the Mostek MK5380, but has a tighter specification for output amplitude range and includes the addition of independent latch and reset controls. The DTMF generator on the 20C89 responds to a hexadecimal code input. Pins D₄ through D₇ are the data inputs for the generator. A high-to-low transition at the LATCH input results in the internal latching of the hexadecimal code and the generation of the appropriate DTMF tone pair. A high on the RESET pin disables the DTMF output, which will not be enabled again until the circuit latches in new data. The SSI-20C89 costs \$8.48 (1000).

ICs such as the SSI-20C89 are useful in consumer products such as telephone-answering machines. The DTMF receiver section, for example, allows the consumer to ring the answering machine from any DTMF telephone and activate a playback of the messages by simply pushing one of the telephone's dial buttons.

One-chip telephones

Exemplifying the trend toward incorporating multiple functions on a single chip, the PBL-3780 from Rifa (Fig 3) is essentially a 1-chip telephone. This multipurpose IC contains the DTMF generator for tone dialing, the speech network for 2- to 4-wire conversion and amplification of the signal from the microphone (and from the line to the receiver), and a simplified tone ringer. The tone-ringer section requires

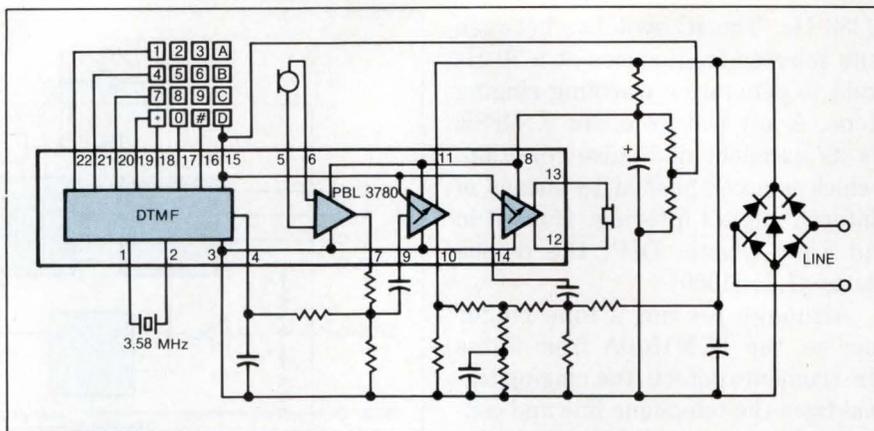


Fig 3—Essentially a 1-chip telephone, the PBL-3780 from Rifa includes a DTMF generator for tone dialing, a speech network for 2- to 4-wire conversion and signal amplification, and a simplified tone ringer.

the addition of several transistors and a few passive components.

A key feature of the PBL-3780 is its ability to work at low current and low voltage—which is important in equipment intended for use in residences, where several phones are sometimes connected in parallel. The PBL-3780 is well suited for use in telephone handsets. The benchmark for telephone handsets is the traditional, passive, type 2500 telephone set, which uses a transformer. Such telephones don't rely on electronics for speech transmission, and they're capable of functioning at currents of a few milliamperes. The PBL-3780 functions at currents as low as 2.5 mA and at voltages under 1.5V.

Adding to the versatility of the PBL-3780 is the option it allows you of configuring the DTMF input pins (normally connected to the keypad) to a 4-bit latched data port. You can use this port to control the DTMF generator, thereby facilitating the use of a repertory dialer such as the Rifa PBM-3915 or a single-chip microprocessor to perform advanced dialing functions. The PBL-3780 sells for \$2.48 and the PBM-3915 for \$2.25 (10,000).

Rohm Corp touts its BP3003 as a 1-chip telephone, but it's not really a 1-chip circuit at all. The BP3003 is actually a small (1.5×2.25-in.) printed-circuit module that includes three separate monolithic ICs, a ce-

ramic oscillator, and an assortment of transistors, diodes, and passive components. The monolithic ICs provide the basic functions of a DTMF dialer, a speech network, and a tone ringer. Because of its small size and low profile, this ready-to-use functional module fits easily into compact telephones. The BP3003 contains all of the electronics required for a complete telephone. The only components you need to add are the handset, a piezoelectric speaker, and the keypad. Evaluation samples cost \$25.

Speakerphone chips

Among this year's crop of new telecomm ICs are improved speakerphone chips. These devices are a welcome development, because many earlier attempts at designing speakerphone chips were less than fully successful.

The basic difference between a speakerphone and a telephone handset lies in their operation. The handset is a full-duplex device that allows simultaneous conversations in both directions. In the handset, the microphone is physically separated from the receiver and little, if any, acoustic feedback can occur to cause oscillations. Of necessity, speakerphones use half-duplex operation, allowing conversation to take place in only one direction at a time to prevent the proximity of the microphone to the speaker from causing

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any "howling," or self-oscillation.

Although you may still have difficulties with the physical placement of the microphone and the speaker in your speakerphone design, the newer speakerphone ICs can ease your task, because manufacturers now have a better understanding of the overall requirements of speakerphones and the functions the ICs must have to overcome the inherent problems in speakerphone design.

A second-generation speakerphone chip from Motorola, for example, offers a number of improvements over its predecessor. You can use the chip to design a high-performance speakerphone system. The MC34118 (Fig 4) is a voice-switched circuit that features background noise monitors for both the transmit and the receive paths, 4-point signal sensing for improved sensitivity, an improved attenuator-gain range of 52 dB between transmission and reception, and the ability to operate at low voltage (3 to 6.5V) for line-powered applications.

The MC34118 includes an on-chip microphone amplifier with an ad-

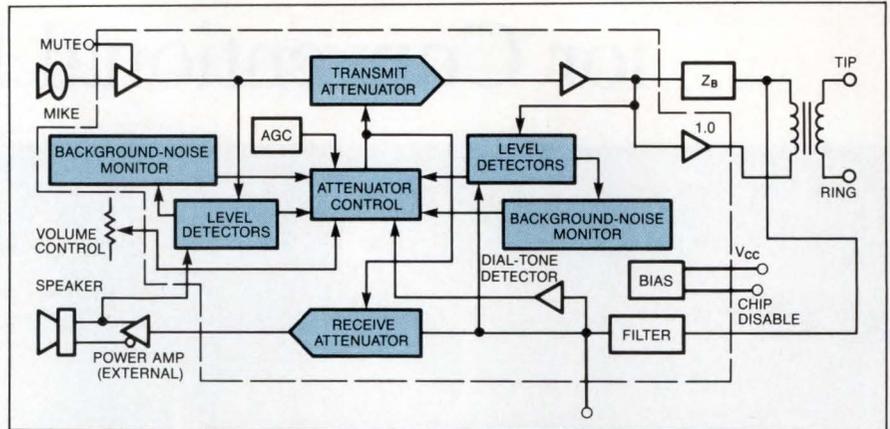


Fig 4—This second-generation speakerphone circuit—the MC34118 from Motorola—is a voice-switched circuit that includes background-noise monitors for both the transmit and the receive paths, 4-point signal sensing, and the ability to operate at low voltage.

justable gain and mute control, and a dial-tone detector to prevent the attenuation of the dial tone by the receiver's background-noise monitor circuit. The chip also includes two line-driver amplifiers that you can use to form a hybrid network in conjunction with an external coupling transformer. The chip requires you to add an external power amplifier to drive the speaker, as you often had to do with earlier Motorola speakerphone ICs. The MC34118

costs \$4.00 in a 28-pin DIP and \$4.24 (100) in a 28-pin SOIC package.

Rifa offers a selection of three speakerphone ICs, including two unconventional CMOS types that are essentially advanced building blocks for high-quality speakerphones. The CMOS types use resistor ladders and digitally controlled analog switches to perform the variable gain/attenuation functions. The PBL-3786 bipolar type is a more conventional analog circuit

For more information . . .

For more information on the telephone ICs discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or contact the following manufacturers directly.

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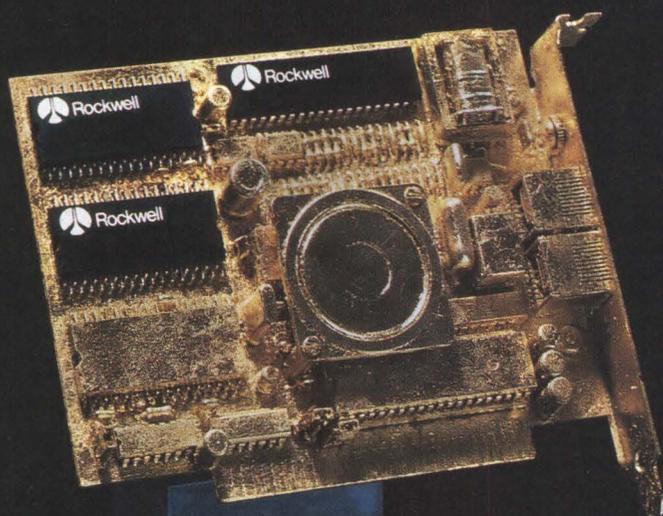
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that is optimized for line-powered circuits.

The PBL-3786 can operate at a supply voltage as low as 2.6V, which allows it to work on a wide range of telephone lines. The chip includes internal voltage regulation for its biasing and overvoltage protection, continuous speech-attenuation characteristics for soft-switching between transmit and receive modes, and a speaker amplifier with automatic volume attenuation. An unusual feature of the chip is its inclusion of a tone ringer, which most speakerphone chips don't include. The PBL-3786's tone ringer takes advantage of the built-in speaker amplifier. The chip sells for \$3.75 (10,000).

Subscribing to the line

The basic functions of a subscriber-line card at the telephone exchange are described by the BORS(C)HT standard. BORS(C)HT is not beet soup, but an acronym that stands for Battery, Overvoltage, Ringing, Supervision, (Codec), Hybrid, and Test. The most difficult of these functions to perform with a monolithic IC is the hybrid function, which traditionally uses a transformer for the required 2- to 4-wire conversion. This conversion includes changing from balanced transmission on the 2-wire side to a single-ended transmission on the 4-wire

side. The FCC requires the part that performs the hybrid function to exhibit longitudinal balance in order to reduce crosstalk on the lines, so the bulky transformer has been difficult to replace with an IC.

Typical SLIC dc-feed circuits supply 20 to 100 mA of current, depending on the length of the loop. To handle these large currents without saturating, the transformer employs magnetic laminates. The transformer must also have a large inductance value to satisfy return-loss and frequency-response specifications. To satisfy both these requirements, the transformer must be rather large.

One way to reduce the size of the transformer yet still meet the FCC specs for longitudinal balance is to use a technique called magnetic compensation. National Semiconductor (TP3200) and Texas Instruments (TCM4207A) offer monolithic ICs that are specifically designed to provide magnetic compensation. (For a complete description of the National Semiconductor device, see "Magnetic compensation gives new life to transformer-based SLICs," EDN, April 30, 1987, pg 149.)

The TP3200 and the TCM4207A ICs use the current in a tertiary winding on the transformer to cancel the dc flux (caused by loop current) in the main windings. This action prevents the transformer

from saturating and allows you to use a small ferrite core. Special circuits in the ICs measure the loop current by sensing the voltage across a matched set of battery-feed resistors and, with proper adjustment, exactly cancel the dc flux in the other windings. By using magnetic-compensation ICs, you can achieve a longitudinal-balance spec of greater than -60 dB.

Although they're not identical in construction and features, both the TP3200 and the TCM4207A provide not only magnetic compensation, but also all of the other functions normally required in a SLIC. Packaged in a 22-pin DIP, the TP3200 costs \$3.75 (1000). In a 24-pin ceramic DIP, the TCM4207A costs \$7.38 (1000).

Eliminating the transformer

Even though the technology of the transformer-based SLIC is a well-proven one, many designers would like to replace it with a monolithic IC. Unfortunately, until recently, no widely available monolithic IC could provide the required performance—particularly with regard to the specifications for longitudinal balance. Now, however, Motorola and Rifa offer devices that appear to be capable of doing just that.

The Motorola MC34120 (Fig 5) and the Rifa PBL-3762 achieve the

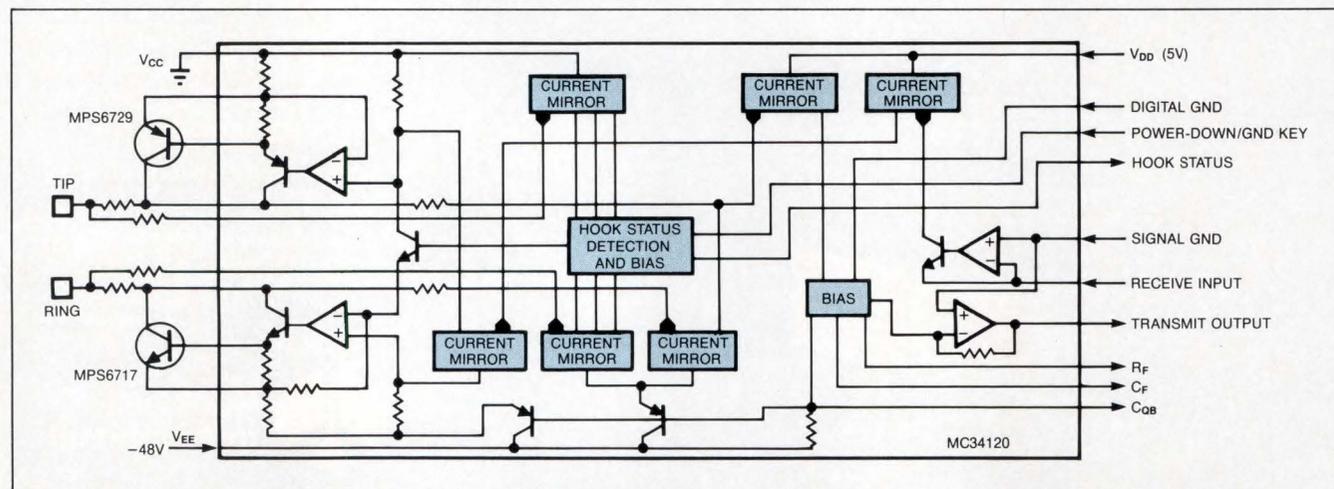


Fig 5—Because it provides all the basic functions for a subscriber-line interface, the MC34120, along with a codec, can replace the transformer in PABX systems and other applications.

1

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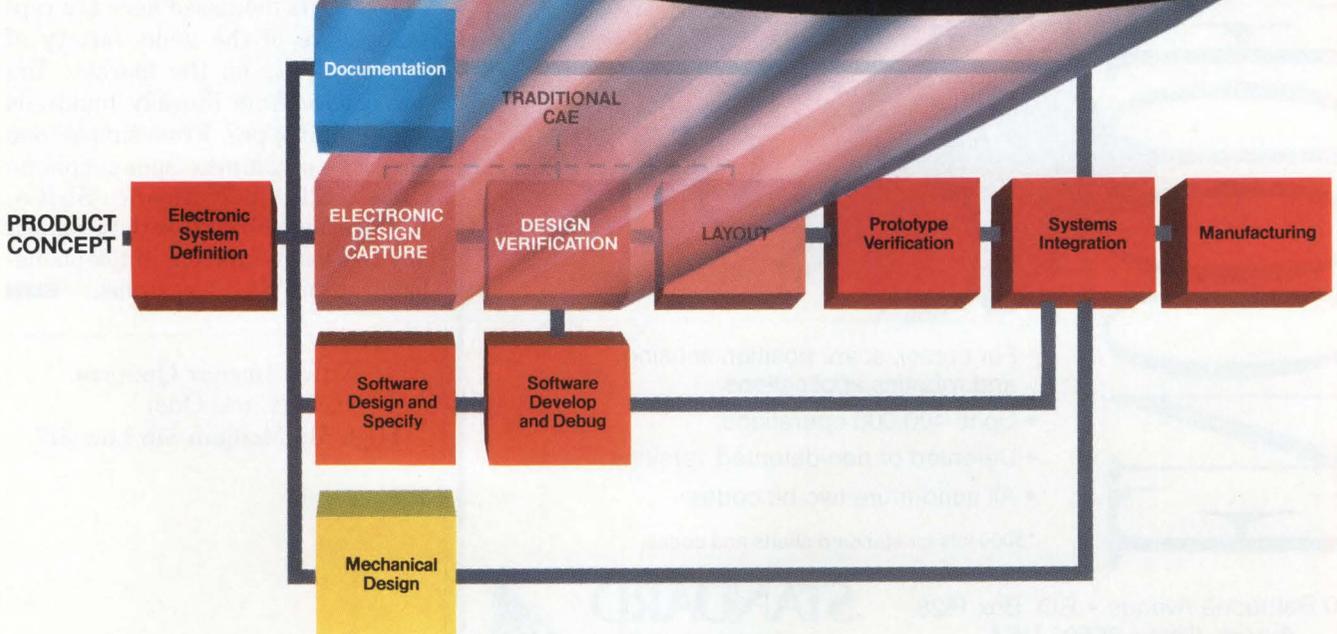
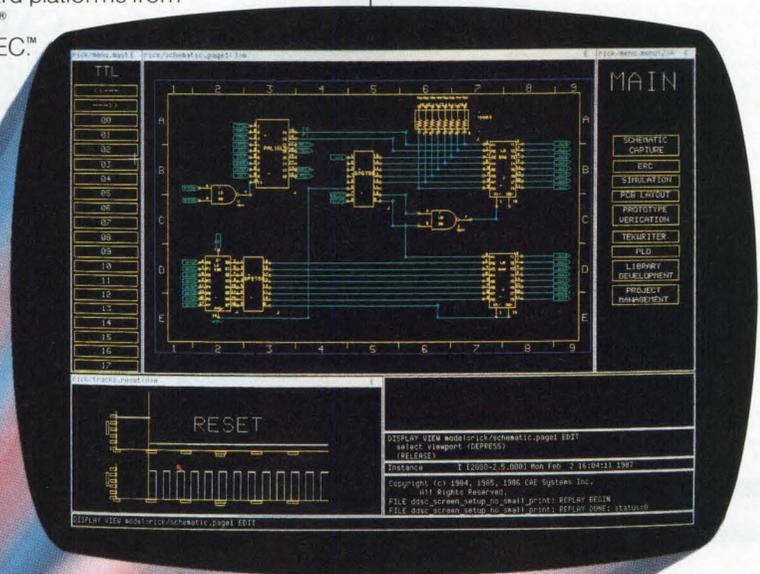
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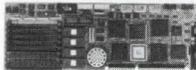
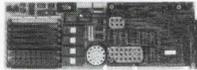
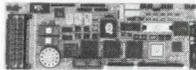


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CIRCLE NO 9

UPDATE

hybrid function by using a separate codec/filter circuit, and both devices carry impressive specifications for longitudinal balance. The specs are difficult to compare, however, because they're stated somewhat differently.

The MC34120's data sheet shows a 2-wire spec of -58 dB at 300 Hz and 1 kHz, and -53 dB at 3 kHz. The PBL-3762's 2-wire specs are -60 dB between 200 Hz and 1 kHz, -50 dB between 1 and 4 kHz, and -63 dB between 300 Hz and 3.4 kHz. Of the two devices, the Rifa device appears to have somewhat better specs in the 300-Hz to 3-kHz range, but it's not certain, because Motorola and Rifa obtained their results under different conditions. Rifa, however, claims that the PBL-3762 will meet or exceed all FCC specifications for longitudinal balance.

The first samples of the MC34120 are planned for March or April 1988; the company expects to offer them for \$6.80 (100) in either 20-pin DIPs or 20-pin SOIC packages. The PBL-3762 (in a 22-pin DIP) is in production; it costs \$8.95 (10,000).

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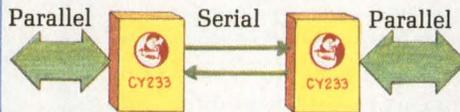
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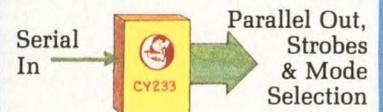
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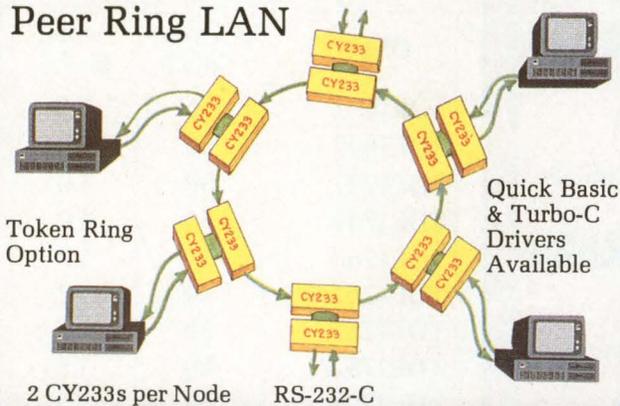
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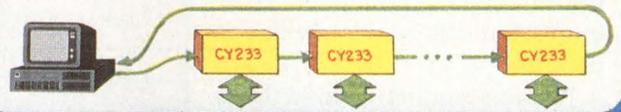


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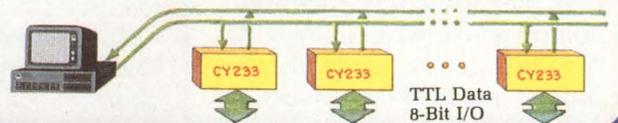
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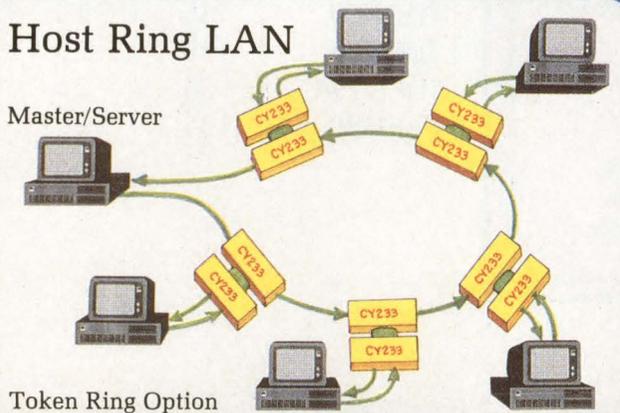


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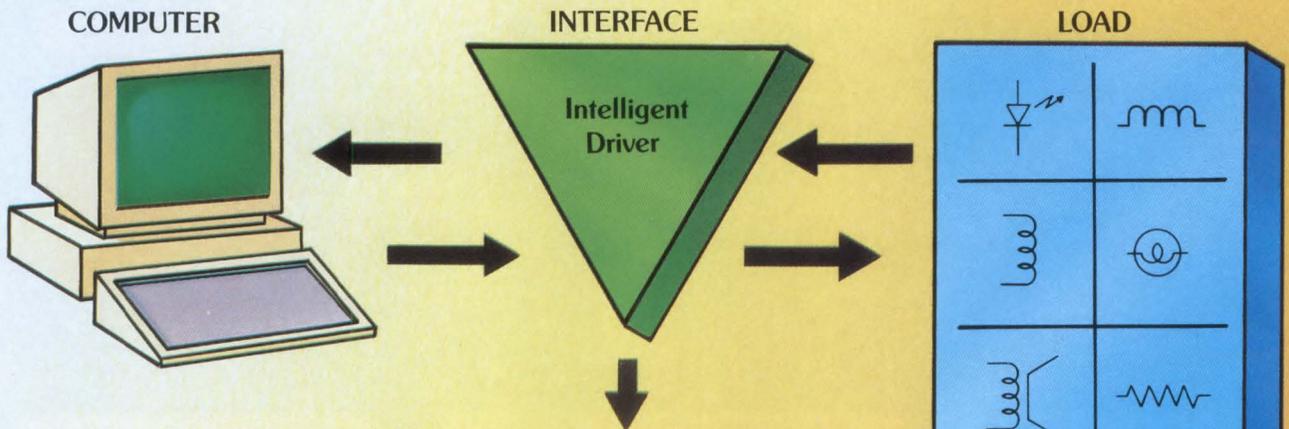
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TDE1787	50	1.2
TDE1787A	60	1.2
TDE1798	50	0.5
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TDE3237	36	0.3
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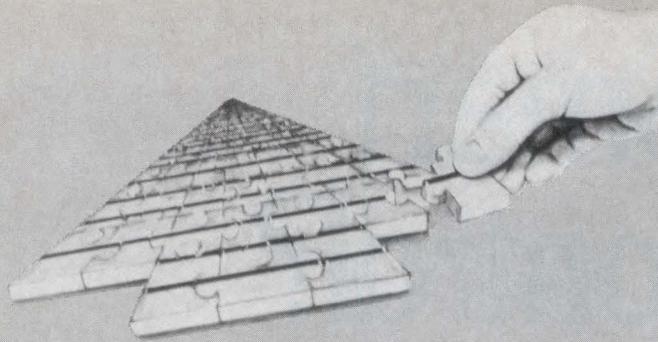
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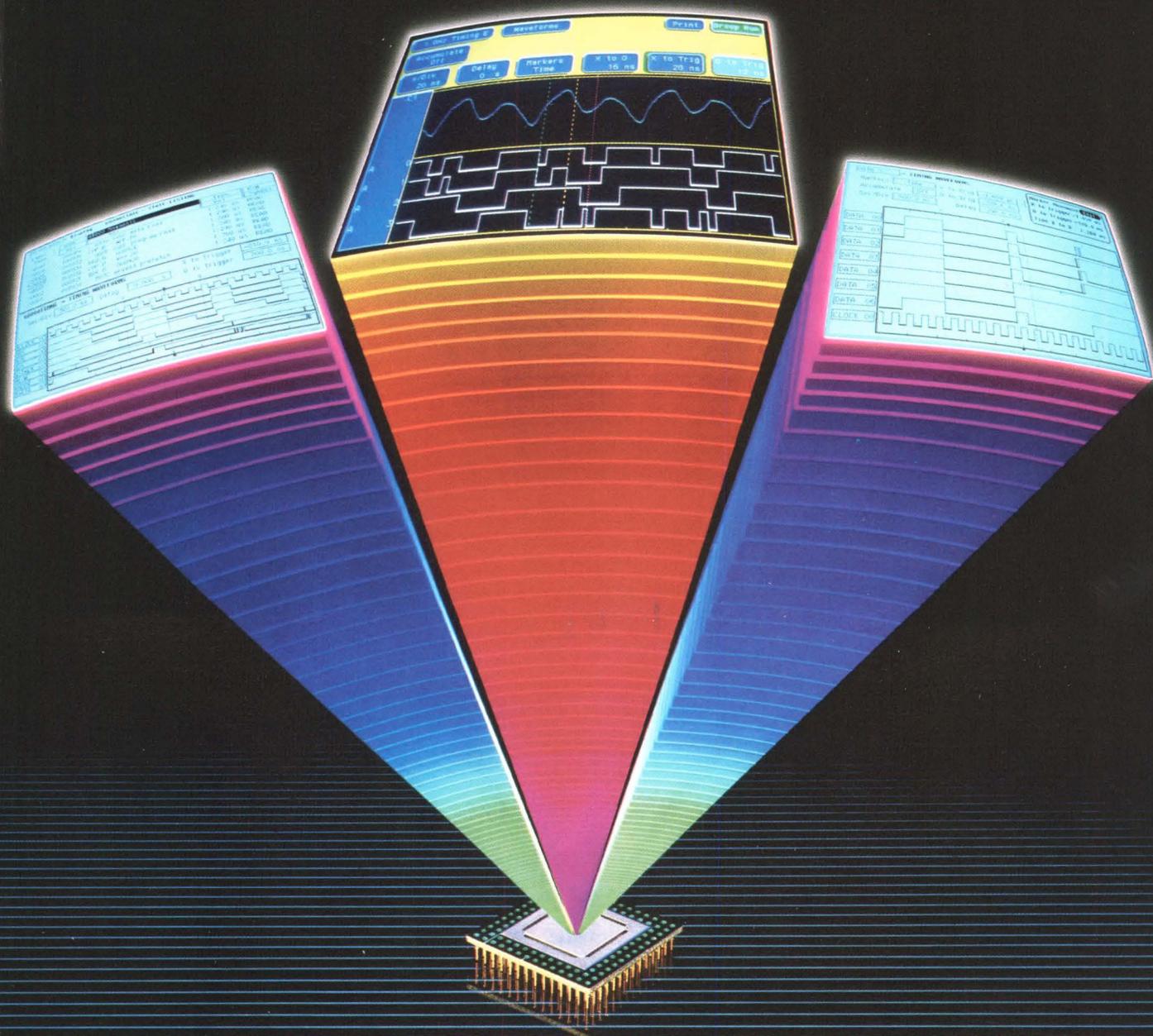
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What if...

Analog comparators achieve high speeds, but application challenges remain

David Shear, *Regional Editor*

High-speed analog comparators have always presented design challenges, and the state-of-the-art devices listed in **Table 1** (pg 76) are no exception. When applying them, you'll have to overcome such device limitations as inherent instability, varying propagation delays, low gain, high input bias current, narrow input-voltage ranges, input slew-rate limits, strange supply-voltage requirements, and high cost.

It's not that manufacturers haven't attacked these problems—it's simply that victory in one area generally involves a retreat in others. The biggest struggle involves combining in one device two conflicting parameters:

- High gain, to allow the comparator to resolve small differences at its input, and
- Wide bandwidth (or short propagation delay), to allow the comparator to operate at high speeds.

Two TTL-compatible devices illustrate the type of tradeoff that manufacturers of high-speed monolithic comparators are forced to make between gain and speed: The Signetics/Philips NE5105A has a gain of 18,000, but a propagation delay of 50 nsec; in contrast, VTC Inc's VC7696 has a propagation delay of 10 nsec but a gain of only 400.

Despite the sacrifices in gain or bandwidth that manufacturers make, the devices nevertheless exhibit a tendency toward instability. To minimize this tendency, you should, when laying out a comparator circuit, place a ground plane under the comparator and any associated parts. In addition, place power-supply bypass capacitors close to the device.

These precautions reduce the primary cause of oscillations: parasitic capacitance. As the output changes state, current flows to the input through this capacitance. The current in turn can alter the level at the input and cause the output to change state once again. That second, and inappropriate, change can again affect the input, with the result that the output bursts into oscillation.

In addition to employing layout techniques that minimize parasitic capacitance, you can take other approaches to eliminating oscillation. One is to make sure that the input signal is fast enough to drive the device through its linear region before oscillation can begin. This approach is fine if you have control of the incoming signal, but usually you don't.

As another approach, you can provide feedback from the comparator's output to its noninverting input to establish hysteresis. According to this approach, when the output changes state, the feedback signal forces the noninverting input through the active region to keep the output from oscillating.

Vendors, too, take steps to minimize the risk of oscillation. Most high-speed comparators, for instance, have a latch on their output. Although one function of such a latch is to support synchronous acquisition, it also helps to suppress os-

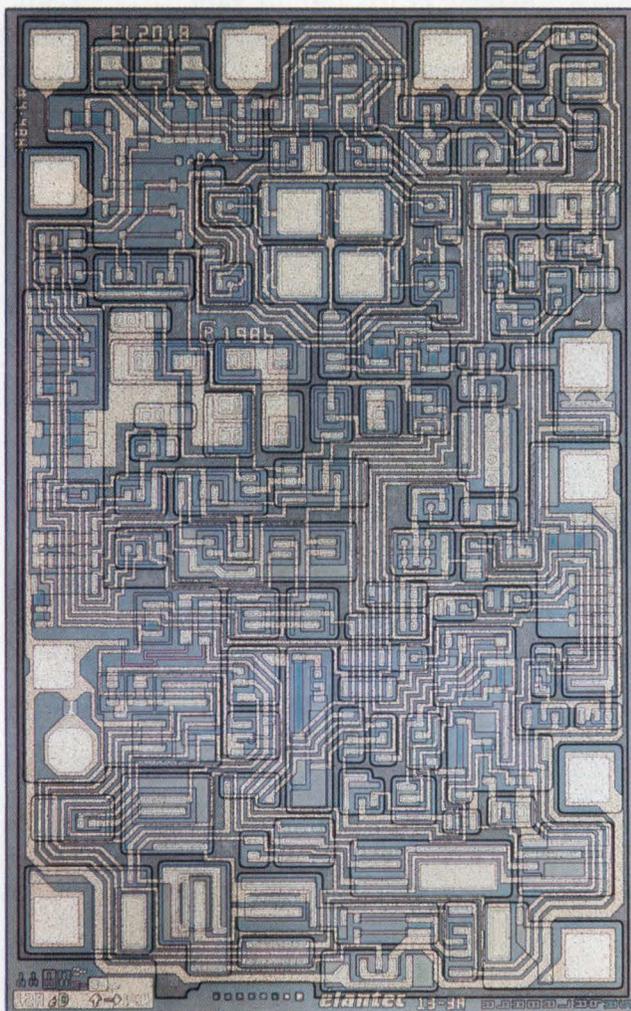


Fig 1—The large blocks of metal, which you can see in the left center of this die photo of Elantec's EL2018, are replaced by a second latch in the otherwise-identical EL2019. The second latch implements the EL2019's flip-flop.

TECHNOLOGY UPDATE

cillations. The latch gives you control over the output, which can change only when you allow a change. The latch effectively disconnects the input from the output, thus breaking the feedback path.

Latched comparators have two modes of operation, transparent and latched, which you control via a latch-enable input. To control the latch, the latch-enable pulse must be long enough to allow the latch to operate, but short enough so as not to re-establish input-to-output feedback and allow oscillation.

A latch gives you control

The EL2019 from Elantec simplifies control of the latch by using a master/slave flip-flop. The device is similar to the EL2018, which has a simple latched output rather than the flip-flop. From a manufacturing

standpoint, the only difference between the devices lies in the final stages of metallization (Fig 1).

The rising edge of the clock input controls the EL2019's flip-flop. Thus, you needn't worry about pulse width, as you would with the simple latch. With the EL2019, the pulse can be as long as you desire.

The EL2019's approach proves beneficial because it's usually much easier to find a clock edge in a circuit than it is to find a pulse with just the right timing. In a successive-approximation analog/digital converter, for instance, you can use the clock that controls the converter's successive-approximation register to latch an EL2019.

Achieve nearly infinite gain

The use of a latch creates a nearly ideal comparator—one whose gain

approaches infinity. Fig 2 shows the transfer function of a typical comparator using a latch and one not using a latch. The resolution of the latched comparator is limited by its own noise.

All comparators have a specified propagation delay: the time it takes a signal to get from the input to the output. You'll notice in Table 1 that propagation delays are often specified with an associated overdrive voltage: the input differential voltage in excess of the value required to cause an output transition.

For some comparators, a larger overdrive reduces the propagation delay, and manufacturers' specs can make it difficult to judge the devices' relative performance. In Table 1, each propagation-delay spec was measured using a 100-mV input signal, but with overdrive lev-

TABLE 1—REPRESENTATIVE HIGH-SPEED ANALOG COMPARATORS

MANUFACTURER AND DEVICE	COMPARATORS/PACKAGE	PROPAGATION DELAY/OVERDRIVE (nSEC MAX/mV)	VOLTAGE GAIN (V/V MIN)	INPUT BIAS CURRENT (μ A MAX)	INPUT OFFSET VOLTAGE (mV MAX)
ANADIGICS ACP10010	1	1.0/20	100	0.10	30
ANALOG DEVICES AD96685	1	3.5/10	—	10	2
AD96687	2	3.5/10	—	10	2
ELANTEC EL2018	1	30/5	15,000	0.30	3
EL2019	1	—	—	0.30	5
HARRIS HMD-11685-2	1	0.5/— (TYP)	10@100 MHz 1.5@2 GHz	0.10	—
HONEYWELL HCMP96850	1	3/10	4000 (TYP)	20	3
HCMP96870A	2	2.3/10	4000 (TYP)	20	3
HCMP96900	2	4.2/50 (TYP)	1000 (TYP)	20	3
PLESSEY SP93802	2	<1/10 (TYP)	20	9	3.5
SP93804	4	<1/10 (TYP)	20	9	3.5
SP93808	8	<110 (TYP)	20	9	3.5
PRECISION MONOLITHICS CMP-08	1	9.5/5	800	13	2.5
SIGNETICS/PHILIPS SE/NE5105A	1	50/5	18,000	1.2	0.25
VTC VC7690	1	1.8/10	400	20	5
VC7695	1	1.8/10	400	20	5
VC7696	1	10/10	400	10	3
VC7697	2	1.9/10	400	20	5
VC7698	2	10/10	400	10	3

TECHNOLOGY UPDATE

els ranging from 5 mV or less to as much as 50 mV.

When the propagation delay is optimized, the gain usually suffers. Therefore, you might have to sacrifice speed in gain-critical applications such as A/D conversion, for which the gain must be high enough to resolve the least significant bit. For an ADC that has a 10V input range using logic that requires 2V signals, the minimum gain is 410 for 10-bit resolution, 1639 for 12-bit resolution, and 26,212 for 16-bit resolution.

On the other hand, other applications might be more sensitive to speed than to gain. In automatic-test-equipment, line-receiver, and instrumentation applications, the input is often a relatively large signal, and a gain as low as 100 might be adequate. Although such applica-

tions might not demand high gain, they might well require fast comparators with small variations in propagation delay.

Such devices include those in the SP9380X family from Plessey. They have a gain of only 20, but a propagation delay of less than 1 nsec. The

analog front end (Fig 3) is a gain block that amplifies the signal to a level sufficient to allow the latch to determine the appropriate output. The latch circuitry is regenerative, so once the output latches, the gain of the device goes from 20 to nearly infinity. This approach allows the

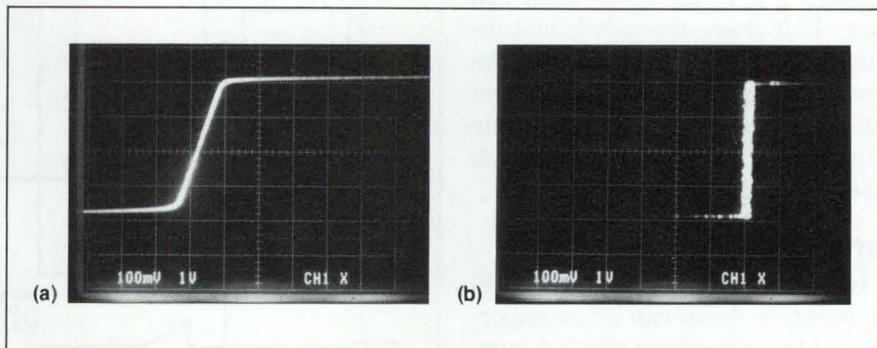


Fig 2—The transfer function of Elantec's EL2018 (a), operating in a transparent mode, shows the limitation of its gain as the input moves through the active region. In the latched mode, the EL2019 (b) has a gain limited only by the noise of the input. For both photos, the vertical scale is 1V/div, and the horizontal scale is 100 μ V/div.

COMMON-MODE-VOLTAGE RANGE (V MAX)	SUPPLY VOLTAGE (V)	OUTPUT COMPATIBLE	OUTPUT TYPE	POWER DISSIPATION (mW MAX)	PRICE	COMMENTS
+1/-2	+5/-5	ECL (SINGLE ENDED)	DIRECT	200	\$19.50 (1000)	
+5/-2.5	+5/-5.2	ECL	LATCHED	140	\$4.60 (100)	
+5/-2.5	+5/-5.2	ECL	LATCHED	280	\$6.40 (100)	
+12/-12	+15/-15	TTL/CMOS	LATCHED	400	\$4.50 (100)	3-STATE OUTPUT, POWER-DOWN MODE
+12/-12	+15/-15	TTL/CMOS	M/S FLIP-FLOP	420	\$4.50 (100)	3-STATE OUTPUT, POWER-DOWN MODE
+1.25/-2.25	+4.5/-3.5	ECL	LATCHED	1250	\$155 (100)	
+2.5/-2.5	+5/-5.2	ECL	LATCHED	125	\$6.19 (100)	
+2.5/-2.5	+5/-5.2	ECL	LATCHED	250	\$8.38 (100)	
+10/-3	+12/-7	ECL	LATCHED	720 (TYP)	\$15.31 (100)	
+2.6/-2.1	+5/-5.2	ECL	LATCHED	360	\$26.56 (1000)	GLITCH CAPTURE, ADJUSTABLE HYSTERESIS
+2.6/-2.1	+5/-5.2	ECL	LATCHED	360	\$46.04 (1000)	ONBOARD BANDGAP REFERENCE
+2.6/-2.1	+5/-5.2	ECL	LATCHED	640	\$69.05 (1000)	
+2.7/-3.0	+5/-5.2	ECL	DIRECT	210	\$3.35 (100)	8-PIN DIP WITH ECL OUTPUT
+3/-3	+5/-5	TTL	LATCHED	130	\$4.75 (100)	
+2.5/-2.5	+5/-5.2	ECL	DIRECT	300	\$7.21 (100)	8-PIN DIP WITH ECL OUTPUT
+2.5/-2.5	+5/-5.2	ECL	LATCHED	300	\$10.21 (100)	
+3.5/-3.5	+5/-5	TTL	LATCHED	300	\$7.21 (100)	
+2.5/-2.5	+5/-5.2	ECL	LATCHED	600	\$15.29 (100)	
+3.5/-3.5	+5/-5	TTL	LATCHED	300	\$10.71 (100)	

TECHNOLOGY UPDATE

comparator to achieve subnanosecond propagation delays with the low-gain front end and still be able to resolve low-level input signals.

Each comparator in the SP9380X family also has a glitch-capture circuit, which detects whether the output exceeds 20 mV (or the input exceeds 1 mV) for more than 900 psec. If it does, the glitch-capture latch sets and remains set until the device receives a reset pulse. You can easily look for glitches in a time window by controlling the latch reset.

Variations can be important

In some applications, changes in propagation delay can be as important as the delay spec itself. A comparator's propagation delay can vary with temperature, with input voltage, and between devices.

Analog Devices' AD96685/7 single and dual ECL-compatible comparators have a dispersion (the change in propagation delay throughout a range of input-overdrive levels) of 50 psec from 100 mV to 1V, and the propagation delay of Honeywell's HCMP96900 varies less than 100 psec (typ) despite changes in input voltage, input direction, and input overdrive.

Although Anadigics doesn't explicitly list a dispersion spec for its ACP10010 GaAs comparator, the data sheet does note that the propagation delay is 1.0 nsec with a 20-mV overdrive and 0.5 nsec with a 100-mV overdrive, implying a dispersion of 50% within the 20- to 100-mV overdrive range.

Even with constant overdrive levels, propagation delays vary from device to device—by an amount that's not always specified. One manufacturer that does provide this spec is Plessey. For its SP9380X family, the company specifies channel-propagation-delay matching of better than 100 psec for devices in the same package.

There's one more source of difficulty in interpreting propagation-delay variations, and it involves the

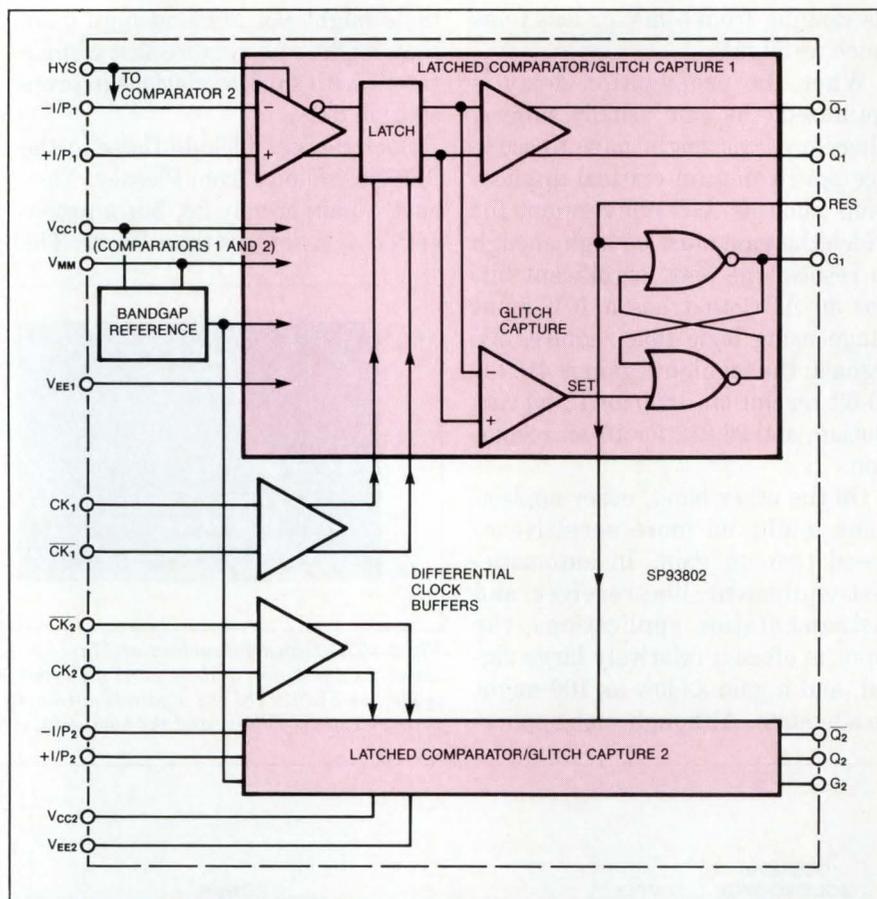


Fig 3—Each channel in the Plessey SP9380X dual, quad, and octal comparators includes a comparator, an output latch, and glitch-capture circuitry.

definition of the point at which you consider a transition to have occurred. For comparators with true/complement ECL outputs, you can determine the exact time of switching by using a test circuit that detects when the outputs cross. However, when only a single ECL output is available, as with the Anadigics ACP10010, it's more difficult to define the point at which the output transition occurs. You could define the exact time as the point at which the output voltage crosses the midpoint between the high and low output logic level; however, that 50% point depends on rise/fall times and might also depend on the load and other factors.

A comparator must track

Propagation delay and dispersion aren't the only factors you have to consider when evaluating whether a comparator is fast enough for your

application. Another important, though rarely specified, parameter is the input slew rate. If the comparator's front end can't keep up with the slew rate of the incoming signal, then errors will result. Honeywell's ECL-compatible HCMP96900 can handle inputs with slew rates to 1500V/ μ sec, and Elantec's EL2018/19 can track a 300V/ μ sec slew rate.

Input bias currents are high

Another challenge to your design is the input bias current. To meet this challenge, you might employ one of the few high-speed comparators that exhibit low bias currents. For example, the EL2018/19's input bias current is 0.30 μ A max, 0.10 μ A typ, and the GaAs comparators from Harris and Anadigics spec input bias currents of 0.10 μ A max.

Most high-speed comparators, however, have high input bias currents—in the range of tens of micro-

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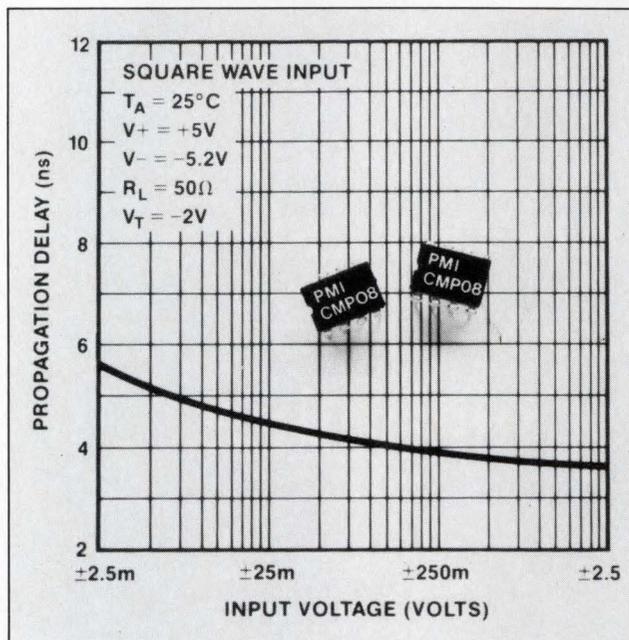
TECHNOLOGY UPDATE

amperes. Such high input bias currents usually require that you include a FET buffer on the input.

Not only do you often need a buffer, but you might also need a voltage divider on the input. A scan of **Table 1** shows that most high-speed comparators have a rather narrow common-mode-voltage range, in the neighborhood of $\pm 3V$. The GaAs comparators have a common-mode-voltage range that's even narrower. The Harris HMD-11685-2 can only accept signals from +1.25 to -2.25V. Unfortunately, your inputs are likely to be $\pm 12V$ max analog signals (from analog circuits powered by $\pm 15V$ supplies) or -2 to +8V digital signals (from circuits made of CMOS-logic, ECL, or TTL devices).

Wide input voltage range

To directly meet the needs of analog signals, the Elantec EL2018/19 devices can accept $\pm 12V$ signals when powered from $\pm 15V$ supplies, although their propagation delay is a relatively long 30 nsec. Honeywell's HCMP96900 is faster—4.2 nsec—but it nevertheless can accept



A comparator's propagation delay isn't constant. For example, Precision Monolithics' CMPO8 exhibits a variation in propagation delay with a varying input signal level.

input voltages of -8 to +13V, depending on the supply voltage. With a +12V and -7V supply (test conditions), the HCMP96900's common-mode voltage range is -3 to +10V. This range satisfies most ATE applications, but the device's 20- μA input bias current might still require that you use a buffer.

The HCMP96900 offers yet another

advantage: It can withstand an input voltage that's 1V higher than its supply voltage. Thus, you can power the comparator and external circuitry from one supply and use a simple diode clamp to protect the comparator's input. For such a clamp to effectively protect a comparator whose input can't withstand voltages in excess of the supply voltage, the external supply voltage has to be at least one diode drop less than the comparator's supply voltage.

Some unusual requirements

Powering a high-speed comparator can entail difficulties beyond those of meeting the requirements of an input-protection scheme. For example, the Harris HMD-11685-2 requires the nonstandard voltages of +4.5V and -3.5V, and the Honeywell HCMP96900 presents complex power-supply-voltage options. In contrast, Elantec's EL2018/19 is quite easy to power. It can accept any level from ± 5 to $\pm 15V$, and its output remains TTL compatible throughout that range.

The foregoing discussion illustrates the tradeoffs you face when designing with high-speed comparators. You might choose one model because its specs suggest more-

For more information . . .

For more information on the comparators described in this article, contact the following manufacturers directly or circle the appropriate numbers on the Information Retrieval Service card.

Anadigics Inc
 35 Technology Dr
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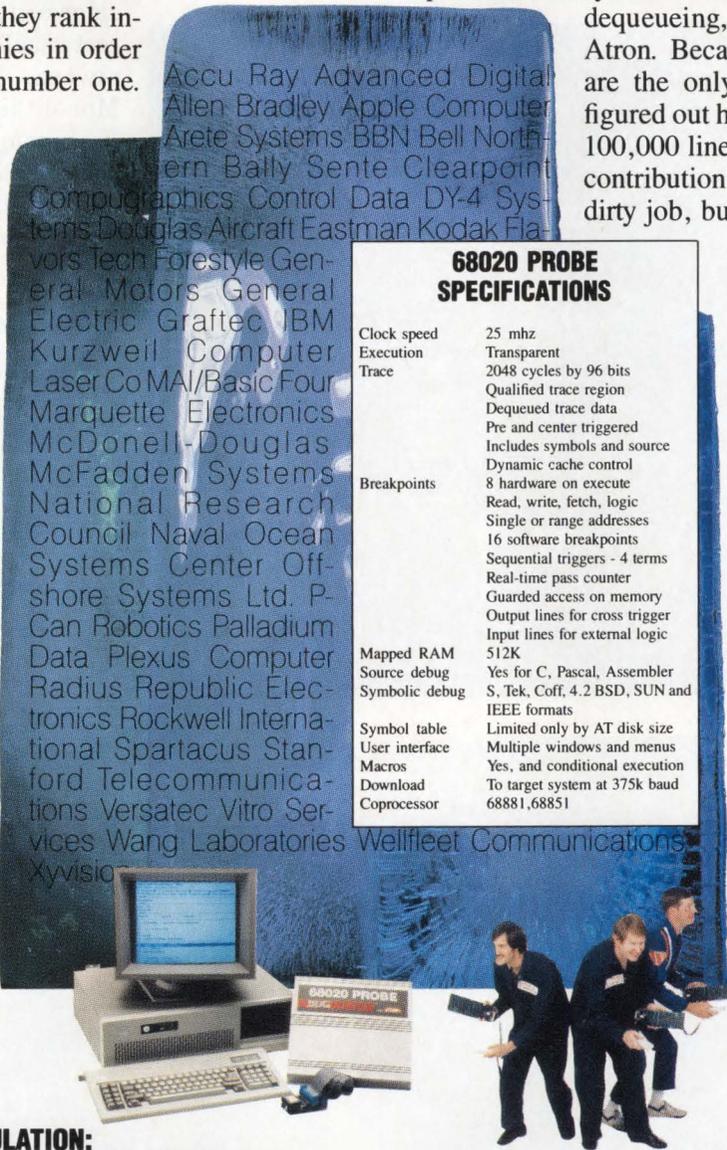
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Execution	Transparent
Trace	2048 cycles by 96 bits Qualified trace region Dequeued trace data Pre and center triggered Includes symbols and source Dynamic cache control
Breakpoints	8 hardware on execute Read, write, fetch, logic Single or range addresses 16 software breakpoints Sequential triggers - 4 terms Real-time pass counter Guarded access on memory Output lines for cross trigger Input lines for external logic
Mapped RAM	512K
Source debug	Yes for C, Pascal, Assembler
Symbolic debug	S, Tek, Coff, 4.2 BSD, SUN and IEEE formats
Symbol table	Limited only by AT disk size
User interface	Multiple windows and menus
Macros	Yes, and conditional execution
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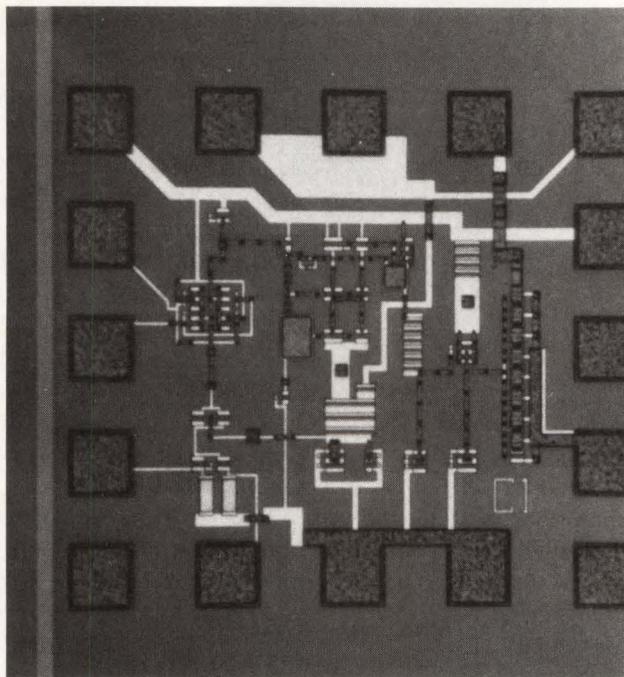
TECHNOLOGY UPDATE

than-adequate gain or speed margins for your application. But, that device might have high bias currents and a narrow input range,

requiring input buffers and voltage dividers, and in turn possibly reducing your circuit's speed to unacceptable levels. Moreover, special pow-

er-supply requirements might drastically increase the complexity of the external circuitry.

Don't forget that you have to consider cost, too: High speed and high cost usually go hand in hand, but not always. For example, Precision Monolithics' CMP08 is a 9.5-nsec, ECL-compatible comparator that costs \$3.35 (100), and the AD96685 from Analog Devices is a 3.5-nsec device costing \$4.60 (100). **EDN**



A 100-mV overdrive enables the ACP10010 from Anadigics to achieve a propagation delay of 500 psec. This GaAs comparator can maintain a gain of 100.

Reference

1. Fleming, Tarlton, "Design challenges attend application of monolithic voltage-comparator ICs," *EDN*, February 6, 1986, pg 45.

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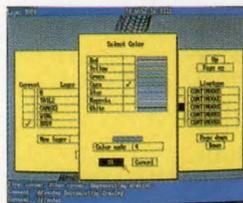
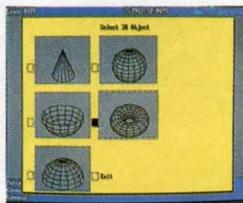
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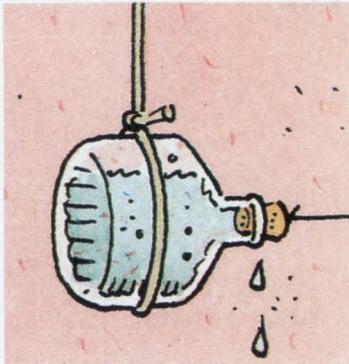
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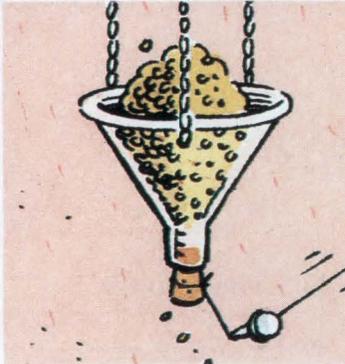
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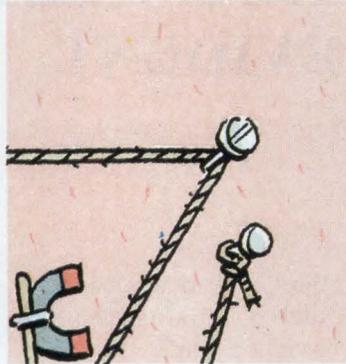
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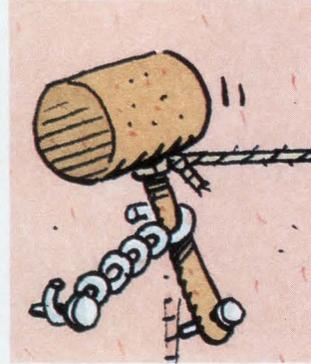
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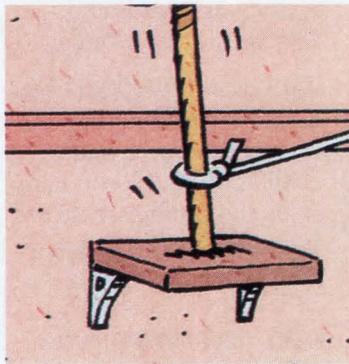
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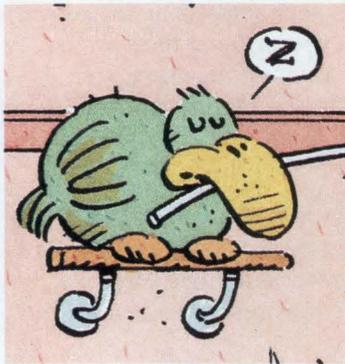
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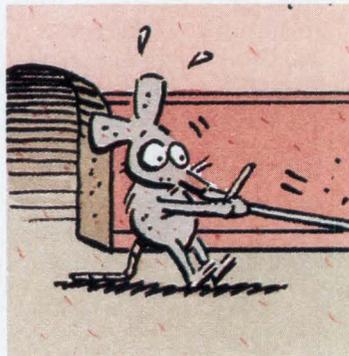
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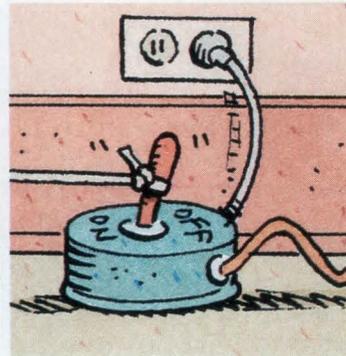
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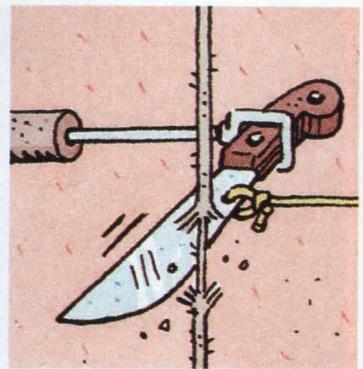
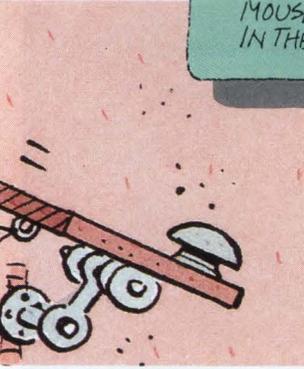


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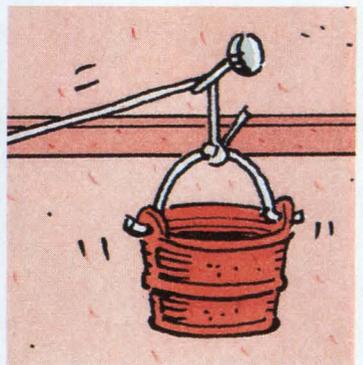
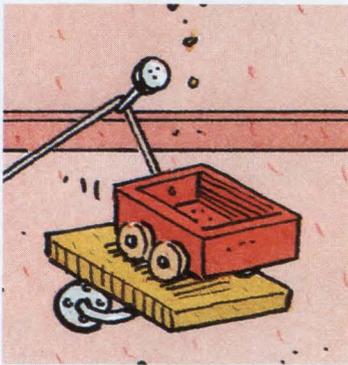
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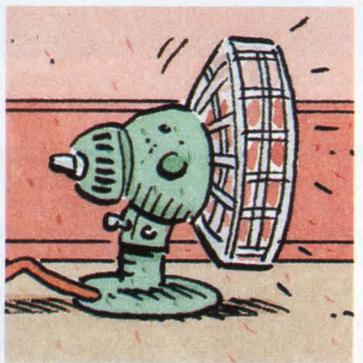
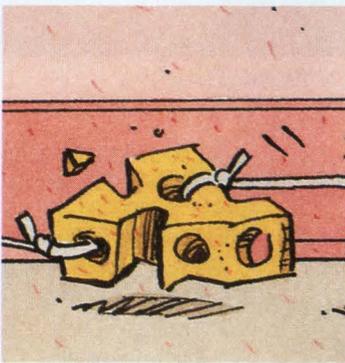
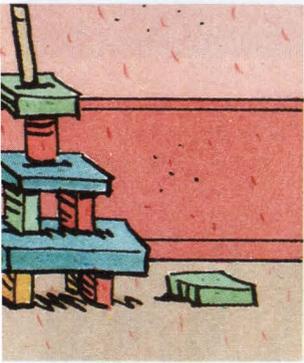
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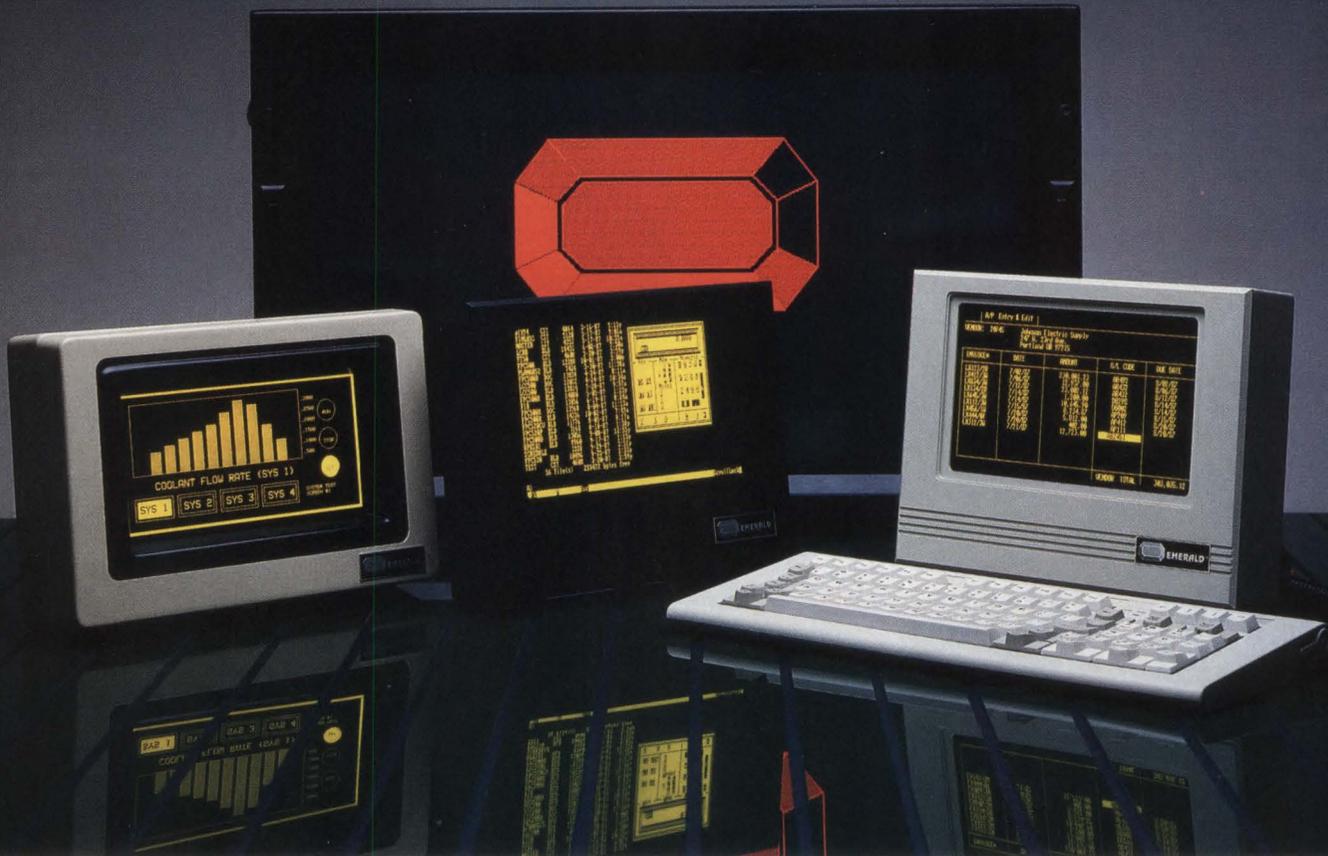
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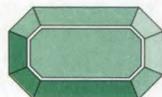
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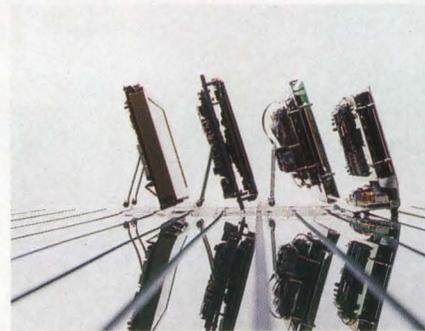
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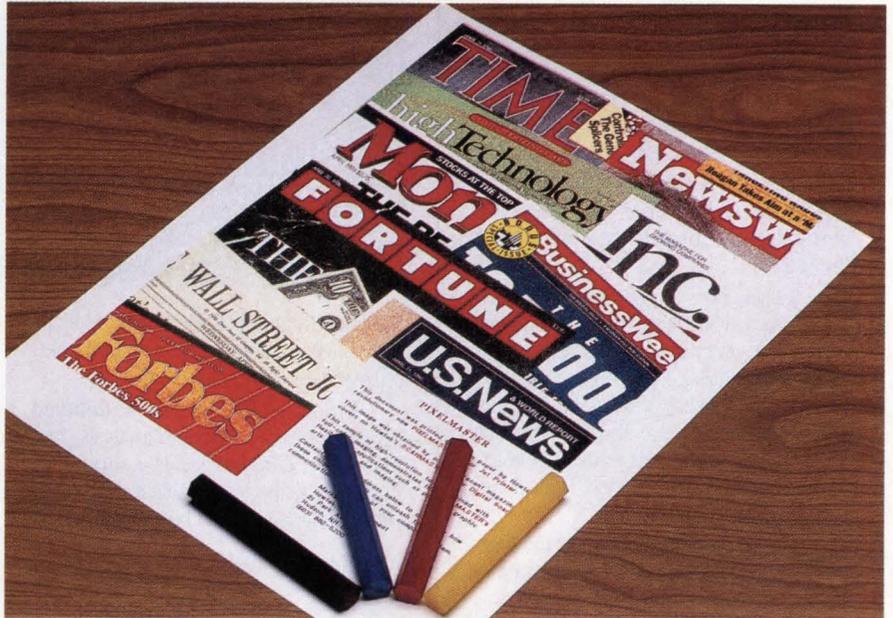
Almost all computer applications today rely on hard-copy-output devices, and with the abundance of raster-printing technologies available, you can now match a raster printer with just about any application. Not only do you have a choice of monochrome- and color-graphics capabilities, you can spend as little as a few hundred dollars to as much as several thousand. Still and all, for the time being, printer-control languages and application software may ultimately dictate your choice.

Whether you're choosing a raster printer for yourself or whether you want to integrate one in a particular system, you have the same choice of technologies: dot matrix, laser, LED, LCS (liquid crystal shutter), ink jet, thermal transfer, and electrostatic—not to mention other, lesser-known types. When it comes time to decide on a technology, such factors as output quality, printing speed, and cost as well as software are important.

In terms of units sold, dot-matrix-impact types dominate the market. These printers offer such features as 300-cps print speeds, letter-quality-print emulation, graphics, plotter emulation—and even color printing—for less than \$1000. Some dot-matrix printers even sell for less than \$200. Dot-matrix units will continue to retain their popularity in many applications strictly because of their low cost.

Laser prices are coming down

In the majority of applications, however, laser printers offer increased functions, and prices for entry-level versions have dropped to less than \$2000. Office Automation



Ink-jet technology and 240-dot/in. resolution allow the Howtek Pixelmaster to print images on plain paper.

Systems Inc (Oasys), for example, offers its 8-page/minute Laserpro Express for \$1895, and the 6-page/minute Laserline 6 from Okidata sells for \$1995. (Incidentally, the combined availability of near-letter-quality dot-matrix printers and low-cost laser printers has virtually eliminated the daisy-wheel printer market.)

Laser printers' advantages revolve primarily around their printing speed, output quality, and graphics capabilities. Models are available with 300×300-dot/in. resolution, and you can expect to see 400- and 600-dot/in. units within the next year. The quality of text possible with recently introduced laser printers far exceeds that of dot-matrix offerings.

The slowest laser printers print at speeds equal to the fastest dot-matrix units—and orders of magnitude faster than daisy-wheel printers. Nevertheless, you should beware

when considering laser printers' speed specs. Most manufacturers specify the theoretical maximum speed of a printer's engine. You may find that, in real life, your laser printer operates slower even on simple text-printing tasks. Printing complex graphics jobs can take several minutes per page.

Actually, choosing a laser printer for word-processing applications is a rather simple procedure. Most laser printers emulate popular dot-matrix and daisy-wheel printers and therefore you can drive them with virtually any text-oriented software package. Consequently, you should choose a printer for such text applications based on electromechanical design, ease of use, cost, and the output quality that your application demands.

The electromechanical, or engine, design is the factor most responsible for a printer's ease of use, speed, and printing quality, and it also

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influences cost. The majority (75% or maybe more) of the laser printers available use either a Ricoh or Canon engine. When evaluating a laser printer's engine, you have to evaluate characteristics such as its duty cycle, paper path, paper-output options, paper-feed options, and maintainability.

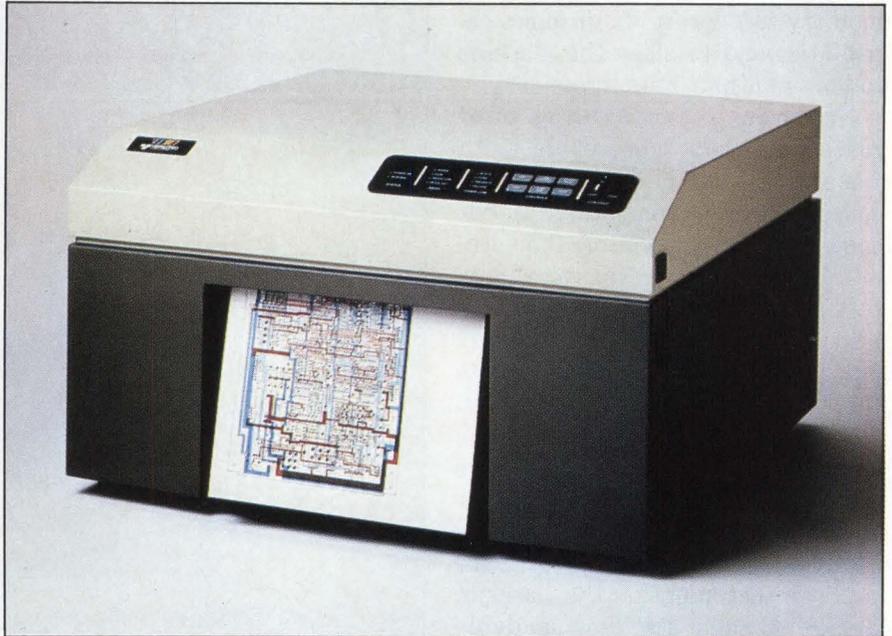
First, keeping your application foremost in mind, ascertain that the engine is rated to print the number of pages you require per month—not to mention its lifetime printing spec. Also, the straighter and simpler a printer's paper path, the less likely you'll be stuck with paper jams or wrinkled paper. Make sure the engine offers a face-down (colated) paper-output capability. Printers that handle envelopes without wrinkling them typically use a straight-through paper path for such hand-fed items.

Laser printers require different maintenance than traditional types of printers. For instance, you have to replace toner cartridges and drum units on a regular basis. Make sure that the installation of these consumables is straightforward. Some printer manufacturers promote the inexpensiveness of their consumables as a feature. Although toner and drum units do affect the cost of using a printer, these costs are negligible for most applications.

LEDs and LCSs charge drum

Printers that use engines based on LED or LCS technology compete directly with laser printers for applications such as word processing and graphics, and in fact, some manufacturers call LED or LCS printers laser printers to avoid confusion. All three types use a similar printing technology. A light source alters the charge of a photosensitive drum. The drum attracts toner particles with an opposite charge. The drum then transfers the toner to the paper, and the printer fuses the toner and paper with heat.

Laser printers employ a laser source and a rotating mirror to



Both electrostatic and thermal-transfer printers from Versatec target the CAE/CAD market for plotters.

strobe the lines of an image onto the drum surface. LCS printers use a single light source and a linear array of LCS elements to transfer each line of an image to the drum. LED engines include an array of LED elements that alters the drum's charge.

A number of new LED and LCS printers are available that suit word-processing and monochrome-graphics applications. For instance, Data Technology offers the \$1995 6-page/minute Crystalprint Series II and the \$2495 8-page/minute Crystalprint VIII. Both employ LCS technology. Fujitsu recently introduced the RX7100 LED printer, which prints 5 pages/minute and sells for \$1160 (100).

Advocates of LED and LCS technology claim that engines for such printers cost less than laser engines. Laser-printer manufacturers argue that, today, the cost difference is less than \$50. The LED and LCS units do lend themselves to simpler engine repairs, however.

Printer language guides choice

Printer technology notwithstanding, when choosing a printer for graphics applications such as desk-

top publishing, you have to consider the issue of software. Publishers of complex graphics packages can't support all the different printers available the way publishers of word-processing packages can. You'll be well-advised to choose a printer that emulates a de facto graphics printing standard.

More page-graphics application software supports the Hewlett-Packard Printer Control Language (PCL) than any other printer language, and HP holds a dominant share of the laser-printer market with its Laserjet family of printers. Moreover, the company developed PCL in levels, or layers, so that it could use the language in all its printer products. Simple dot-matrix printers only use the low levels of PCL; laser printers use the highest levels.

The 8-page/minute \$2595 Laserjet Series II printer is currently the mainstay of the Laserjet family. The standard model includes only 512k bytes of memory, but you can ask for an additional 1M-byte (\$495), 2M-byte (\$995), or 4M-byte (\$1995) board. The standard configuration isn't capable of full-page graphics output: You must add

TECHNOLOGY UPDATE

memory to improve its graphics capabilities and to allow the machine to hold multiple fonts in memory.

Numerous manufacturers offer raster printers compatible with Laserjet Series II PCL (typically called Laserjet+ compatibility), but some are more compatible than others. In certain cases, you can simply test a particular printer's compatibility with the software package you wish to use, but such simple tests don't prove complete PCL compatibility. **Ref 1** contains some sample programs that are effective for testing compatibility. A printer that passes such tests will be more likely to work with any software package that supports the Laserjet Series II and its downloadable fonts.

As is true of the Laserjet units, PCL-compatible printers from other manufacturers also require extra memory to handle downloadable fonts and graphics. The Oasys Laserpro Express offers PCL compatibility, but not a downloadable-font feature. The company's \$2295 Laserpro Express Series II accepts downloadable fonts; you must purchase the \$2795 Laserpro Silver Express or the \$3695 Laserpro Gold Express to add full-page graphics capabilities.

Okidata's Laserline 6 comes with just 272k bytes of memory, and you can only expand it to 676k bytes. So, even though the Laserline 6 accepts downloadable fonts, it can't print a full page of graphics. Data Technology's Crystalprint VII includes 1.5M bytes of memory, but the Crystalprint Series II only includes 512k bytes (albeit expandable to 1.5M bytes). The Fujitsu RX7100 contains 640k bytes of memory, and the company plans to offer expansions for a total of 3M bytes.

Postscript adds versatility

For some graphics applications, you may want to consider a printer with a higher-performance control language—the Postscript page-description language from Adobe Sys-



An extended version of the manufacturer's PCL (printer control language) includes color commands to control the Paintjet printer from Hewlett-Packard.

tems (Mountain View, CA), for example. Adobe developed the language and licenses it to printer manufacturers. Postscript provides software developers with a tool for creating, modifying, and printing graphical images. It also has a set of proprietary fonts and can scale those fonts to any size.

Typically the Postscript interpreter resides in the printer and offloads much of the graphics processing from the host. The cost of adding Postscript to a printer is approximately \$2000; it is the combination of royalties paid to Adobe and the added computing power required to run the language that results in the price premium.

Many graphics packages that take advantage of Postscript are emerging, and several printer manufacturers now offer Postscript-compatible printers. QMS and its subsidiary, The Laser Connection, both have Postscript-compatible printers available. The QMS-PS 810 has 2M bytes of memory and is compatible with both Postscript and PCL. Indeed, this \$5495 8-page/minute printer includes an Appletalk inter-

face in addition to the standard printer interfaces.

The Laser Connection sells the \$4995 PS Jet and the \$5495 PS Jet Plus, which include 1.5M and 2M bytes of memory, respectively. These printers offer essentially the same features as the QMS product. The Laser Connection also offers an add-on product that converts the Hewlett-Packard Laserjet Series II printer to a Postscript printer. The \$2495 kit includes a board that resides in a personal computer and a board that is installed in the printer. The company offers similar capabilities for other printers with Canon engines.

Several other printer companies have licensed Postscript for use in laser printers, including AST Research, NEC Information Systems, and Texas Instruments. Other companies will choose to acquire Postscript compatibility elsewhere.

Phoenix Technologies Ltd (Norwood, MA), for example, has announced its Page Printer Control System (PPCS), and Canon intends to use PPCS in a printer due out around midyear. Phoenix Techno-

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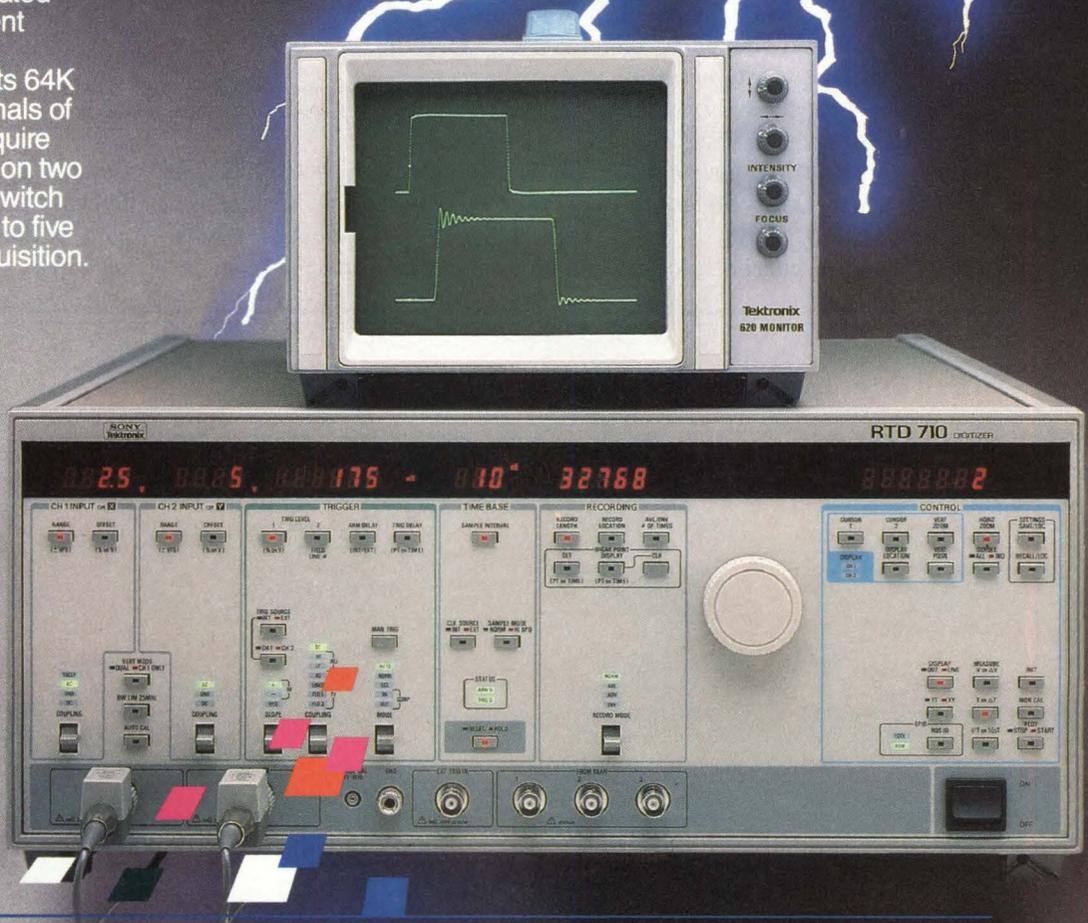
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logies cloned Postscript but of course had to use its own fonts and algorithms. Personal Computer Products Inc (San Diego, CA) has also introduced its Imagescript language, which emulates Postscript. Oasys has announced plans to offer a Postscript clone, developed in-house, as an option on its Express printers.

As you can surmise, the market for monochrome desktop graphics is booming, thanks to the combination of available graphics software, reasonably priced printer hardware, and standard printer-control languages. This is not yet the case for the color-graphics market, although color printers are emerging that will eventually bring color graphics to the desktop. Soon companies will even offer color laser printers. Still, no standards yet exist for color desktop graphics. Adobe plans on adding color to Postscript, but products may be a year away. In addition, manipulating color images requires more computing power and better software than do monochrome applications.

Hewlett-Packard currently offers



The 3M-byte memory capacity of the Oasys Laserpro Gold Express provides room for downloadable fonts and full-page bit-image graphics.

its Paintjet printer for \$1395. The printer employs ink-jet technology, produces 180×180-dot/in. resolution, and can also output near-let-

ter-quality text at 167 cps. Hewlett-Packard added extensions to PCL to control the Paintjet, and the printer primarily targets applications such

For more information . . .

For more information on the raster printers discussed in this article, contact the following manufacturers directly or circle the appropriate numbers on the Information Retrieval Service card.

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(408) 727-8899
Circle No 672

Fujitsu America Inc
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San Jose, CA 95134
(408) 432-1300
TLX 176207
Circle No 673

Hewlett-Packard Co
1820 Embarcadero Rd
Palo Alto, CA 94303
Phone local office
Circle No 674

Howtek Inc
21 Park Ave
Hudson, NH 03051
(603) 882-5200
Circle No 675

The Laser Connection
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Mobile, AL 36608
(205) 633-7223
Circle No 676

NEC Information Systems Inc
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Boxborough, MA 01719
(617) 264-8000
Circle No 677

Office Automation Systems Inc (Oasys)
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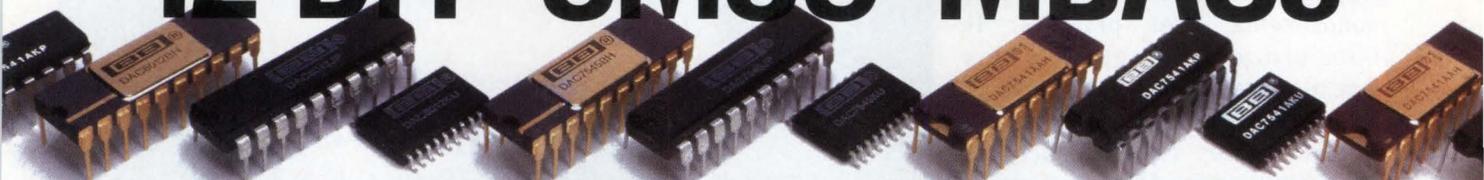
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CH		±1/2	±5	-25/+85	Ceramic DIP	12.95
GCH		±1/2	±1	-25/+85	Ceramic DIP	15.85
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as spreadsheet-program-generated charts. Although you can use plain paper with the Paintjet, the company recommends special paper or transparency media for best results.

Howtek is another vendor with a color printer for sale that uses ink-jet technology. The Pixelmaster is capable of generating color-page graphics comparable to those of monochrome laser printers. It mixes text and color graphics on a page at a resolution of 240 dots/in.

Furthermore, this printer prints on plain paper. The unit includes compatibility with PCL and extensions for color output. Although its resolution and print quality are sufficient for color desktop publishing, you may have a hard time finding a software package to drive it. An IBM PC/AT-class host would be very slow in generating a color-graphics image without help from dedicated hardware. The printer costs \$4500 with 512k bytes of memory; a 2.5M-byte version sells for \$5700.

Tektronix offers a thermal-transfer color-graphics printer that prints 300 dots/in. The 4693D can produce high-quality pages of graphics, but requires the use of coated paper. Tektronix presently offers the product with a card that interfaces to the Apple Macintosh II Nubus; the Macintosh II version with 4M bytes of RAM costs \$7995. The Tektronix printer suffers from the same lack of software and dedicated hardware as the Howtek product.

The Colorgrafix 100 printer from QMS is probably the closest to providing the computer power necessary for processing color images. QMS sells the \$16,995 printer with a 2-board dedicated controller. The boards fit in an IBM PC/AT or compatible and include a TI TMS 34010 graphics processor. The thermal-transfer printer's resolution is 300×300 dots/in. The controller's native language is an extension of the Direct Graphics Interface Specification (DGIS).



The LED engine that Fujitsu uses in its 5-page/minute RX7100 proves to be a low-cost alternative to a laser-based engine.

QMS has also signed the first licensing agreement for a color version of Adobe's Postscript language. QMS will introduce a color Postscript-based printer early this year and plans to ship it in the second half.

Besides word-processing and desktop publishing, you can also make use of some of these monochrome and color raster printers in CAE/CAD applications. For example, the monochrome page printers from both Oasys and QMS, as well as Howtek's color Pixelmaster, include support for Hewlett-Packard's plotter control language, HP-GL.

Oasys has recently introduced the 22-page/minute Laserpro 2200, which prints on 11×17-in. paper, for \$16,500. Don't expect laser technology to allow printing on paper much wider than 11 inches. The laser beam becomes distorted when aimed at the edges of the printer drum. LED or LCS printers, however, may continue to expand in terms of paper-width-printing capabilities.

Electrostatic plotter for CAD

Electrostatic plotters are also useful in CAE/CAD applications. Electrostatic devices essentially em-

ploy a raster-printing technology, but most people think of them primarily as plotters. Such plotters are popular because they print many orders of magnitude faster than pen plotters. In an electrostatic device, coated paper passes under an electrostatic head. The electrostatic head consists of a linear array of wire nibs.

The wire nibs in the electrostatic head place a charge on the coated paper. The paper passes through a toner bath and then a fusing process. The wire nibs in the electrostatic head determine the resolution. Typically, electrostatic plotters are capable of 400-dot/in. resolution.

Versatec's electrostatic plotters cover a broad range. The V-80 family plots on 11-in.-wide paper, and Series 7000 plotters plot on 22- or 44-in.-wide paper. Moreover, the company also offers electrostatic devices with color capability. These plotters use a single electrostatic head and four toner stations to produce color with four passes made on each plot. The 2500 Series produces color on 11-in. paper, and the 3000 Series is compatible with 22- and 44-in. paper.

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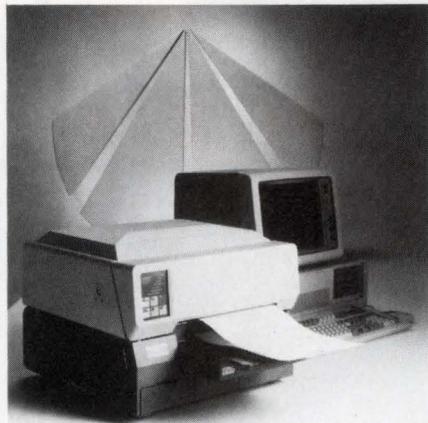
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PAGE 276**

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Liquid-Crystal-Shutter (LCS) technology charges the photosensitive drum in Data Technology's Crystalprint VIII page printer.

print raster data but often function in a vector world, Versatec offers a number of printer-control options. The company sells stand-alone rasterizing controllers, controllers that fit into a host such as a VAX or an IBM PC/AT, and controllers embedded in certain plotter models. Prices range from \$8000 for an 11-in. monochrome unit to \$52,000 for an E-size color unit that includes a rasterizing controller.

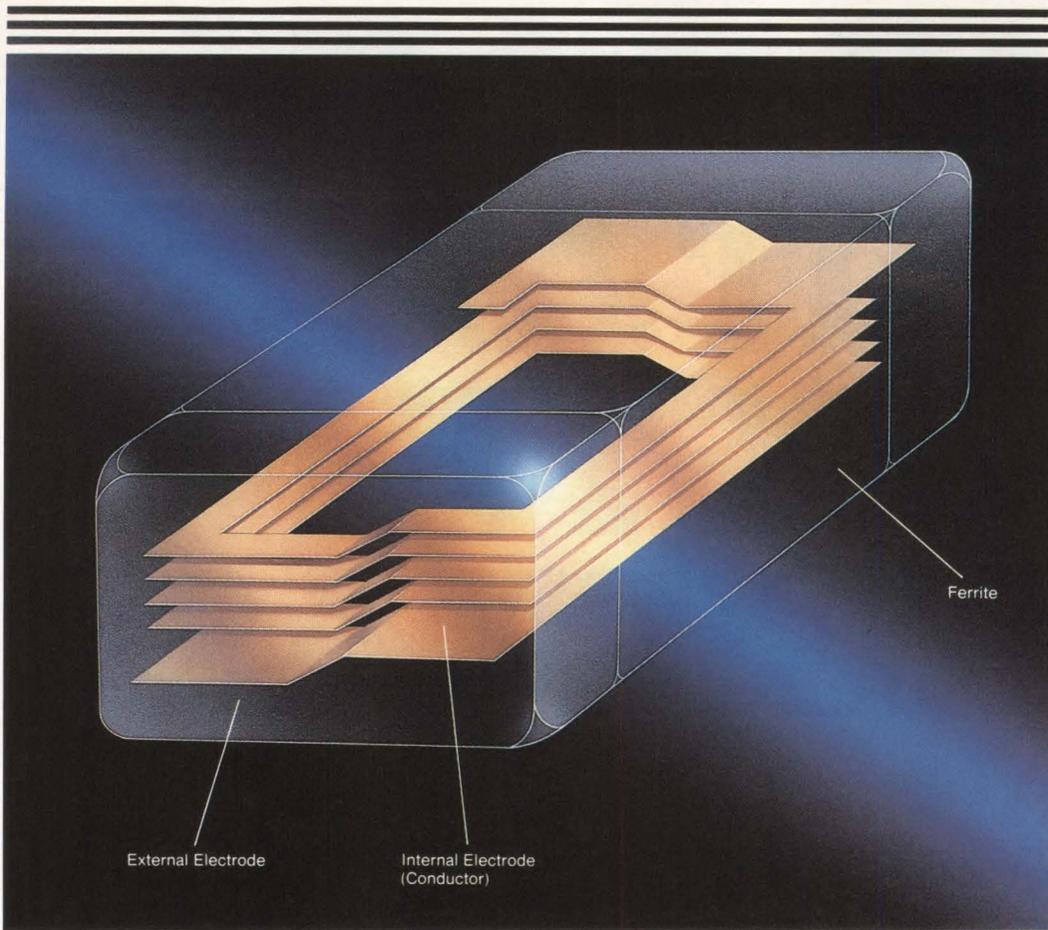
Rounding out its raster-printer offerings, Versatec has thermal-transfer color plotters for sale. The 2700 Series handles 11-in. paper. Typical configurations cost under \$9000. Although Versatec targets the 2700 Series for plotter applications, you can conceivably use these printers in other graphics applications. **EDN**

Reference

1. McCown, R, and H Clark, "Laser Metrics," *PC Tech Journal*, September 1987, pg 74.

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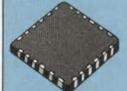
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F: 630kHz - 13MHz
Tolerance: \pm 2%
Attenuation: 20dB min.

Leadless EMI Filter (Wound Chip EMI Filter)

- NLL4532**
C: 33pF - 100,000pF
L: 1 μ H - 220 μ H

Multilayer Ceramic Chip Capacitor (High Frequency, Low Loss)

- FC1414**
C: 0.5 - 3,300pF
- FC2828**
C: 0.5 - 22,000pF
- FR1414**
C: 0.5 - 3,300pF
- FR2828**
C: 0.5 - 22,000pF

Ferrite Chip Bead

- CB201209**
Z α : 7, 10, 11 Ω
- CB321611**
Z α : 19, 26, 31 Ω
- CB322513**
Z α : 31, 52, 60 Ω
- CB453215**
Z α : 70, 120, 125 Ω

Multilayer Chip Inductor

- MLF3216**
L: 0.047 - 33 μ H
- MLF3225**
L: 39 - 220 μ H

NTC Chip Thermistor

- NTC CS3216**
R typical: 1.0 - 150k Ω at 25 $^{\circ}$ C
Temp. Range: -25 to +85 $^{\circ}$ C

Multilayer Chip LC Trap

- MXT4532**
F: fo \pm 2%

SM Active Delay Line



Multilayer Chip IFT

- MIA4532**
F: 455, 459, 464kHz
- MIF4532**
F: 10.7MHz

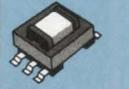
FDL

Delay time: 20 - 75 nsec.

Multilayer Chip Transformer

- MTT4532**
L: 10 - 200 μ H

SM Transformer/Inductor



- EE5**
- ER9.5**
- ER11**
- T2**

A variety of characteristics are available. Please specify when ordering.

Multilayer Chip LC Filter

- MXF4532H**
HPF (Tuner)
- MXF4532B**
BPF (FM radio)
- MXB5050B**
BPF (VCR)
- MXB5050L**
LPF (VCR)
- MXB5050D**
Delay Line (VCR)

A variety of characteristics are available. Please specify when ordering.

SM Step-up Inductor (Piezoelectric Buzzer)

- OL3.3 x 1.6**
 - OL3.3 x 2.1**
- Inductance values are representative, please specify value when ordering.

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MN5295/MN5290 & MN6290

High Speed:

MN5295: 17 μ sec Max. Conversion Time

MN5290: 40 μ sec Max. Conversion Time

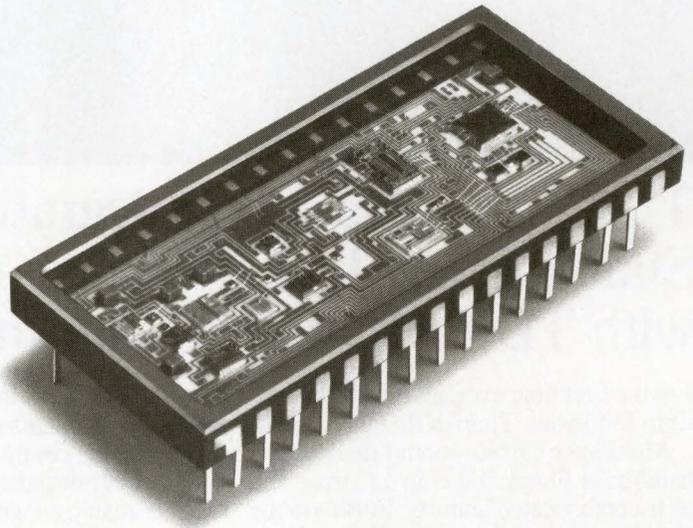
MN6290: 20kHz Min. Sampling Rate

Small 32-Pin Double-Wide DIP

14-Bit "No Missing Codes"

- 55°C to + 125°C Operation

MIL-STD-883 Screening



In the two speed classes of 16-bit A/D's that have emerged, only *one* supplier designs its devices to meet all of your military and aerospace requirements: Micro Networks.

In the high-speed (15-20 μ sec) class, our MN5295/96 are the fastest (17 μ sec), smallest (by 31%), and *only* devices to offer - 55°C to + 125°C operation and MIL-STD-883 screening.

In the general-purpose (40-50 μ sec) class, our MN5290/91 offer these same advantages; while our MN6290/91 add an internal T/H, plus FFT testing for improved performance, ease of specification, and significant space savings.

And most critical to your designs, these are the *only* devices that operate over the extended military temperature range with full military screening.

MN5295/MN5296

The newest in our expanding line of high-performance, military, 16-bit A/D's are at the top of their class.

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17 μ sec Max. (16 Bits)

Smallest Package by 31%:

Double vs. Triple DIP

Widest Temperature Range:

-55°C to +125°C

Only Devices Available with 883 Screening

In the top speed class, our MN5295/96 excel, providing outstanding 16-bit performance in a DIP package that is fully 31% smaller than any competitor's. No other supplier can meet your requirements for high-speed, high-resolution, military A/D's. When your design demands the best, demand Micro Networks MN5295/96.

MN5290/MN5291

They're the best in their speed class of workhorse 16-bit A/D's. Specify them for all your applications that don't require the added performance of our MN5295/96.

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40 μ sec Max.

Smallest Package by 31%:

Double vs. Triple DIP

Widest Temperature Range:

-55°C to +125°C

Only Devices Available with 883 Screening

Like our MN5295/96, our MN5290/91 A/D's are ideal for any design where you need true 14 or 13-bit performance over an extended temperature range. These devices were the first 16-bit military A/D's. Since their introduction, their broad acceptance and proven performance have made them industry standards.

MN6290/MN6291

In a class by themselves, these FFT-tested sampling A/D's are ideal for traditional data acquisition and DSP applications.

Single Package Sampling A/D

High Resolution/Sampling Rate:

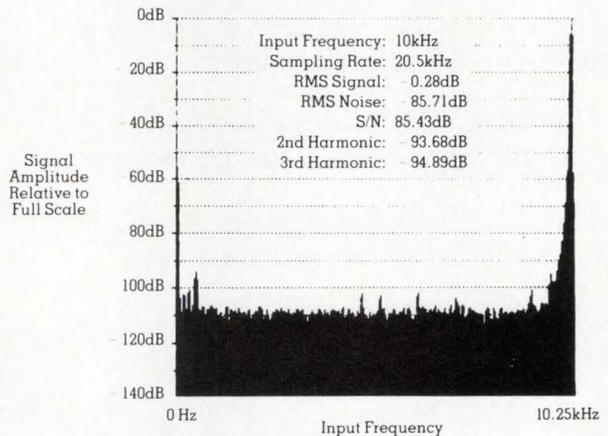
16 Bits @ 20kHz

Signal-to-Noise Ratio: 84dB

Harmonics: -88dB

Temperature Range: -55°C to +125°C

Available with MIL-STD-883 Screening



These devices eliminate the hassle of evaluating T/H specs that are difficult to understand and often don't relate.

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Hitachi MOS Memory Leadership Has Been Earned

The stag faces constant challenges from aspiring leaders of his herd. He maintains his leadership only by winning those battles—over and over again. Similarly, in the highly competitive MOS memory market, leadership must be earned . . . not just claimed.

Hitachi's MOS memory leadership is well documented. For example:

1983 Hitachi is ranked the number one CMOS RAM manufacturer by engineers in *Electronic Design's* Audit of Brand Recognition.

1984 Hitachi again is rated the leading CMOS RAM manufacturer in *Electronic Design's* study.

1985 Hitachi again is rated number one in CMOS RAMs, in *ED's* Brand Recognition Study.

1986 Hitachi is the first manufacturer that purchasing agents consider when buying CMOS RAMs, as reported by *Electronic Buyers' News*, Buyers' Preference Study.

1986 Hitachi rated the most preferred CMOS RAM vendor in *EBN's* Japanese Semiconductor Manufacturers' Benchmark Study. First in quality, customer service, technical assistance, trust, ease of doing business . . . and first in eight additional categories.

Marketplace recognition has been building over the years. This is due, in part, to our uncompromising QA programs, which have given our memory products a legendary reputation for quality and reliability. Our long-range investment in production technology is also important to our customers. It means that our products are in constant, dependable supply.

Supremacy Achieved



Hitachi's technology pushes MOS memory to new levels of performance. The new HM62256 is the latest achievement. At 85ns, it's the fastest 32Kx8 SRAM you can buy, yet it draws only 40mW power. And, you can choose either a standard 28-pin DIP, or Hitachi's new surface mount SOP (Small Outline Package). This packaging innovation permits double-sided surface mounting for board densities five times greater than standard DIPs... another Hitachi plus.

So, the next time someone claims they're "number one" in MOS memories, consider the facts. If you're like the survey participants mentioned above, you'll call Hitachi first. Contact us through your local Hitachi Sales Representative or Distributor Sales Office today.

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Wideband 500-kHz to 1-GHz hybrid amplifier includes internal decoupling capacitors

The LH4200 is a general-purpose 500-kHz to 1-GHz amplifier that includes internal decoupling capacitors to simplify its use. This device has been demonstrated to work even with extremely long power-supply leads. The only extra decoupling it requires is an electrolytic capacitor to guard against low-frequency oscillations.

The amplifier's input stage is a dual-gate GaAs FET, which provides low input capacitance and high transconductance. The dual-gate structure accepts the signal on input 1. Input 2 controls the gain of the amplifier. The amplifier has

maximum gain when input 2 is 1.5V. When input 2 is -2V, the gain is reduced by 60 dB. Thus, at 100 MHz, a full 60 dB of automatic-gain-control range is available.

The amplifier has a third input for use in series feedback. The output feeds back to pin 3 via a single resistor, which controls the overall power gain of the amplifier. The second and third stage of the amplifier are bipolar, providing high power output. At 10 MHz, the output is capable of delivering 12 dBm into 50Ω with 1 dB of signal compression.

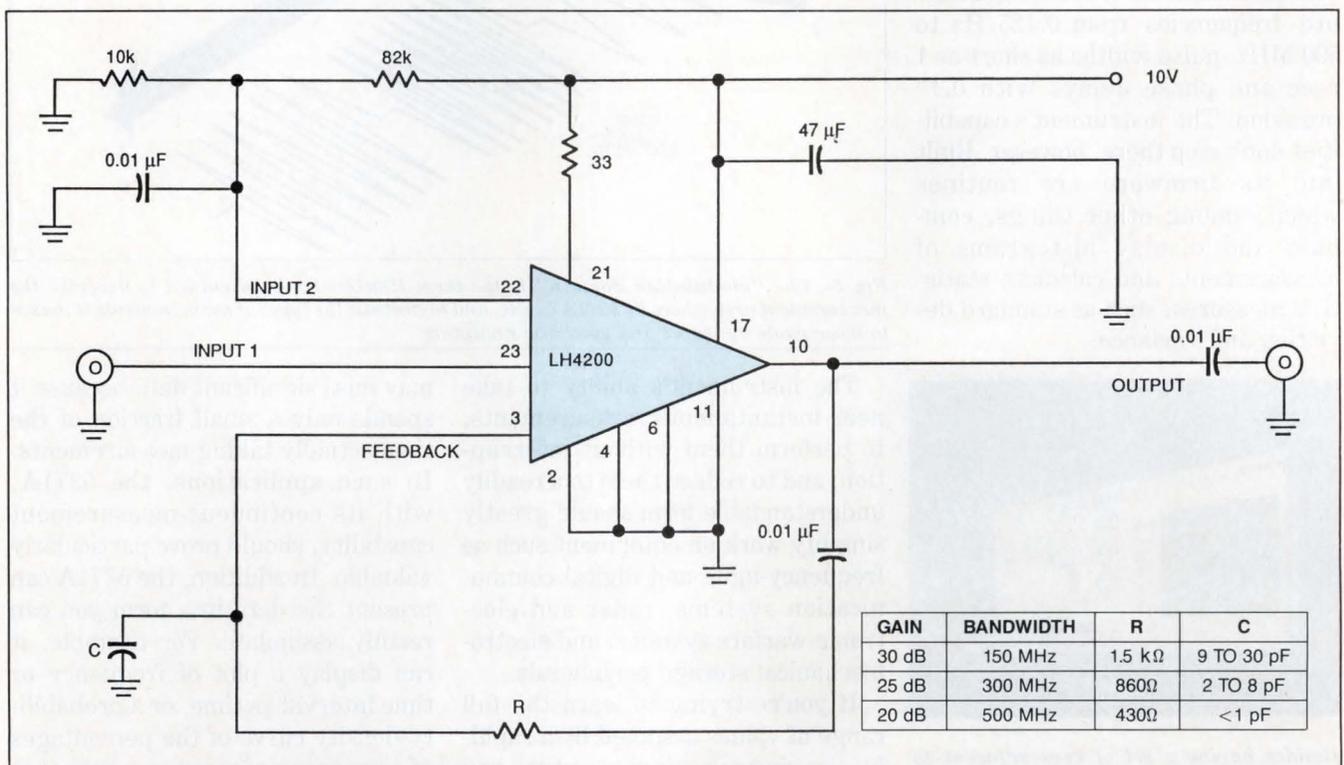
The ac-coupled amplifier has a

gain of 37 dB at 100 MHz and 3 dB at 1 GHz. You can cascade two amplifiers to get more than 60 dB of gain at 100 MHz.

The LH4200 has a noise figure of 3 dB at 50Ω and is powered from a single 10V supply; it requires 70 mA max of current. The amplifier comes in a 24-pin ceramic package. The commercial part (LH4200CD) costs \$54; the military version (LH4200C) costs \$66 (100).—*David Shear*

National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95052. Phone (408) 721-5856.

Circle No 733

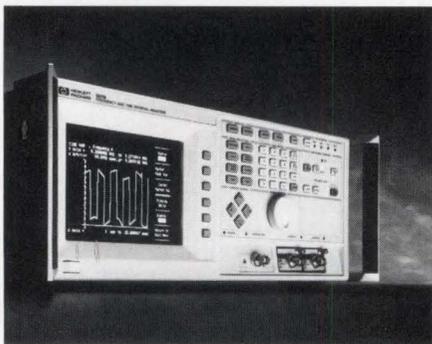


When you use the LH4200 as a feedback amplifier, you can control its gain with a single resistor in a series-feedback configuration. The accompanying table shows various gain/bandwidth options for the part. The only external decoupling required for this amplifier is the 47-µF electrolytic capacitor.

Analyzer constantly monitors and displays 500-MHz frequency and interval variations

The 5371A is an unusual frequency and time-measuring instrument because it makes continuous measurements with no dead time between samples, even when the sampling interval is only 10 nsec (10M samples/sec). In addition, without external equipment, it can give you a picture of the way time-related quantities (frequency, for example) vary as a function of time.

Although many counters let you connect an external recorder to obtain plots of the trend of a measured quantity, only the 5371A offers continuous-measurement capability and an integral graphics display, the vendor claims. The 5371A can measure frequencies from 0.125 Hz to 500 MHz, pulse widths as short as 1 nsec and phase delays with 0.1° precision. The instrument's capabilities don't stop there, however. Built into its firmware are routines which, among other things, compute and display histograms of measurements and calculate statistical measures, such as standard deviation and variance.



Besides having a set of keys adjacent to firmware-generated legends on the screen, the 5371A's front panel also provides cursor arrows and both keypad and rotary controls for data entry.

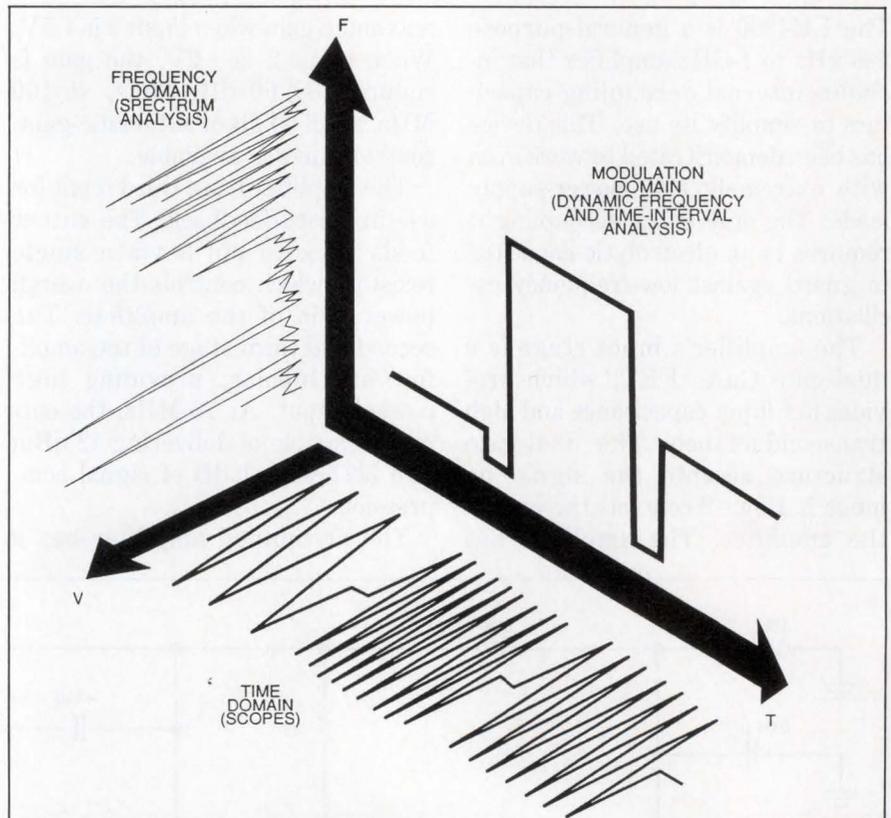


Fig 1—The “modulation domain” is the term Hewlett-Packard coined to describe the measurement area where its 5371A excels, and to contrast the types of measurements it makes to those made by scopes and spectrum analyzers.

The instrument's ability to take near-instantaneous measurements, to perform them without interruption, and to reduce them to a readily understandable form should greatly simplify work on equipment such as frequency-agile and digital communication systems, radar and electronic-warfare systems, and electro-mechanical storage peripherals.

If you're trying to learn the full range of values assumed by a rapidly changing measured quantity, you can find it frustrating, and possibly downright misleading, to use an instrument (such as a counter) that

may miss significant data because it spends only a small fraction of the time actually taking measurements. In such applications, the 5371A, with its continuous-measurement capability, should prove particularly valuable. In addition, the 5371A can present the data in a form you can readily assimilate. For example, it can display a plot of frequency or time interval vs time, or a probability-density curve of the percentages of a sequence of measurements that fall into several user-defined value ranges.

You can understand the 5371A's

UPDATE

significance by comparing it with oscilloscopes and spectrum analyzers. Think of three orthogonal axes representing voltage, frequency, and time (Fig 1). The scope displays voltage vs time (the time domain); the spectrum analyzer displays voltage vs frequency (the frequency domain); and the 5371A displays frequency vs time. The vendor calls this third measurement mode the "modulation domain." With tongue only slightly in cheek, the company's representatives suggest that "it's about time" you were able to make measurements in the modulation domain.

Because the 5371A's forte is measuring *variations* in time-related quantities, you have to be able to predict how much variability the instrument itself introduces into its measurements. With a 100-nsec measurement time (only 10× the period of the measured signal), curves on the data sheet show an uncertainty of ~100 kHz when you measure a 100-MHz input; when you increase the measurement time to 1 sec, the uncertainty drops to ~10⁻³ Hz—10 parts per *trillion* of the measured quantity.

In the preceding examples, the frequency display changes in 20-kHz increments at the 10-nsec sample time and in 2×10⁻²-Hz increments when the sample time is 1 sec. One year after calibration, crystal aging adds another 20 Hz of uncertainty to a 100-MHz measurement. The HP 5371A costs \$21,500.

—Dan Strassberg

Hewlett-Packard Co, 1820 Embarcadero Rd, Palo Alto, CA 94303. Phone local sales office.

Circle No 732

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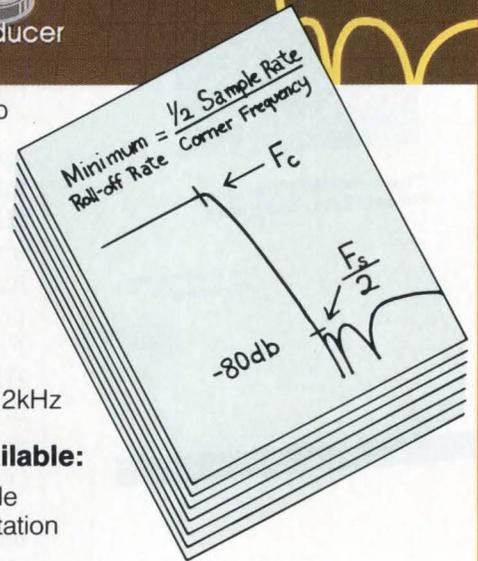
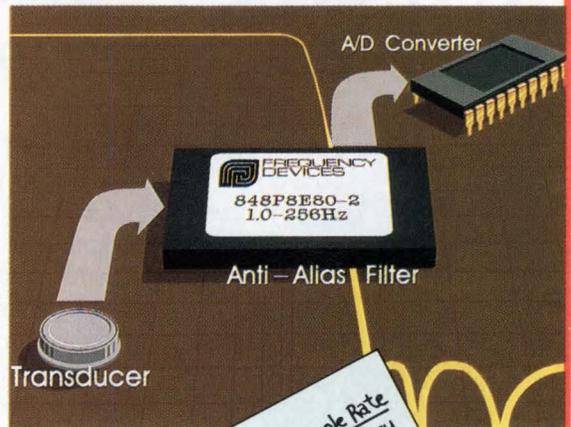
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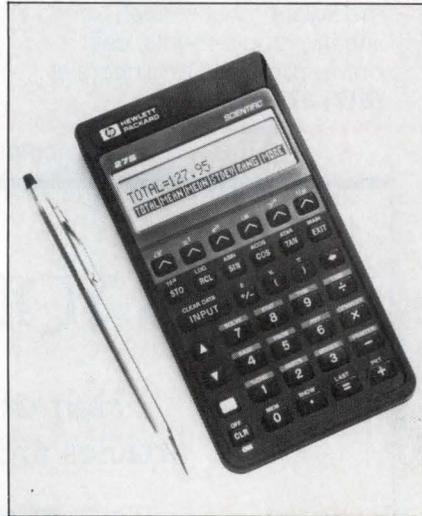
PRODUCT UPDATE

Two calculators suit manager and engineer

For the first time, the engineering manager can have a scientific calculator that also provides the financial functions usually found only on business calculators. The HP-27S (\$110) can perform "time value of money" operations (such as amortization) and forecasting operations, as well as the usual, basic scientific functions.

Meanwhile, the vendor has also upgraded the performance and user interface of its revolutionary HP-28C scientific calculator. The upgrade, designated HP-28S (\$235), has 32k bytes of user RAM (its predecessor had less than 2k bytes). Further, the HP-28S augments the HP-28C's unusual soft-key, menu-driven interface by allowing you to set up menus for your own functions.

Externally, the HP-28S differs only in graphics details from the HP-28C. Internally, the HP-28S has just two custom chips; the HP-28C had five.



Offering both scientific and financial functions, the HP-27S calculator aids the engineering manager who must do engineering design as well as figure out budgets.



With increased memory and an augmented user interface, the HP-28S scientific calculator supercedes the HP-28C.

Both the HP-27S and the HP-28S have an infrared light-beam printer interface for the HP 82240A printer (\$135). Interestingly, for the purpose of reducing costs, the vendor did not make the printer interfaces bidirectional. The calculators depend on careful timing, rather than a Busy signal from the printer, to avoid overrunning the printer's buffer. Thus, neither calculator has any facility for external storage or retrieval of programs or data; you must key in every program step or datum manually.—*Charles H Small*

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Circle No 731

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Three multiple-option packages, the 2465A Special Editions, are con-

Key Features	2465A DV	2465A DM	2465A CT	2465A	2445A
Probe Tip Bandwidth	350 MHz	350 MHz	350 MHz	350 MHz	150 MHz
No. of Channels	4	4	4	4	4
Horizontal Accuracy	2% (.001%*)	2% (.001%*)	2% (.001%*)	2% (.001%*)	2% (.001%*)
Max. Sweep Speed	500 psec	500 psec	500 psec	500 psec	1 nsec
Vertical Sensitivity	2 mV/div	2 mV/div	2 mV/div	2 mV/div	2 mV/div
Trigger Frequency	500 MHz	500 MHz	500 MHz	500 MHz	250 MHz
GPIB	Standard	Standard	Standard	Optional	Optional
Counter/Timer/Trigger/Word Recognizer	Standard	Standard	Standard	Optional	Optional
Digital Multimeter	Standard	Standard	Not Available	Optional	Optional
Video Trigger	Standard	Not Available	Not Available	Optional	Optional
Probes	4	4	4	2	2
Warranty	3 years on parts and labor, including CRT				

*with Counter/Timer/Trigger

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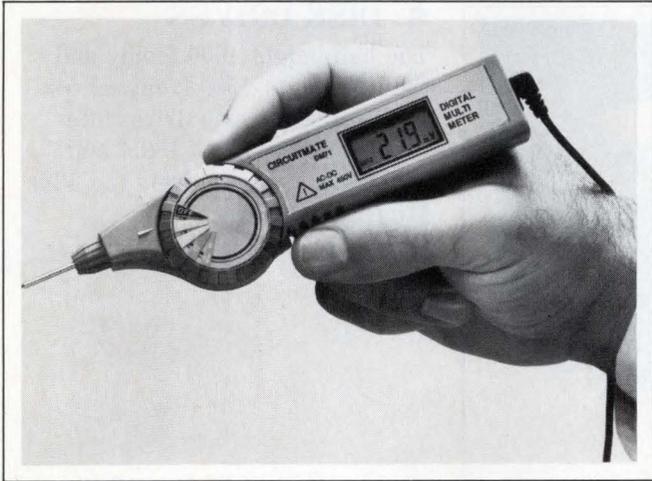
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▲ PEN-GRIP DMM

The DM71 handheld, pen-type digital multimeter (DMM) features a 3½-digit LCD. The autoranging meter has 0.7% accuracy max and possesses a data-hold function (pg 254).

Beckman Industrial Corp.
Circle No 605

CPU BOARDS

The 68020-based CPU-22/23 board facilitates message passing on the VME Bus and provides either 256k bytes or 1M byte of dual-port RAM (pg 83).

Force Computers Inc.
Circle No 601
Force Computers GmbH
Circle No 602

PASCAL DEBUGGER

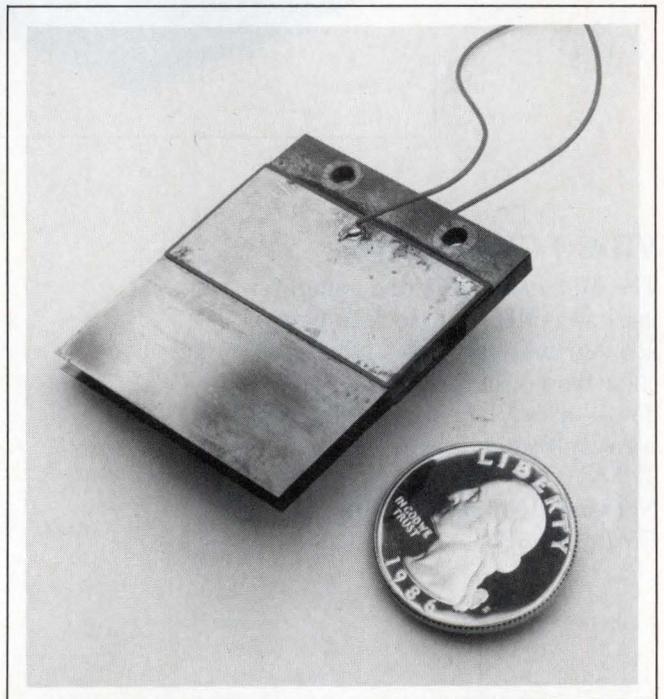
T-Debugplus version 2.0 is a symbolic run-time debugger for Turbo Pascal. It debugs programs that use CGA, EGA, or Hercules graphics modes (pg 245).

TurboPower Software.
Circle No 606

CHIP SET

The 5-member FE3500 chip set provides the core logic and the memory and I/O control necessary to implement a 16-bit, 80286-based, IBM PC/AT-type personal computer (pg 233).

Faraday Electronics Inc.
Circle No 604



▲ PIEZOELECTRIC FAN

The LP24HT, a dc-operated miniature piezoelectric fan, produces a planar air stream that emanates from the front tips of its resonating blades (pg 216).

Piezo Electric Products Inc.
Circle No 603

READERS' CHOICE

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◀ DISK DRIVES

The half-height 1600 family and the full-height 1500 family of 5¼-in. Winchester disk drives offer storage capacities of 180M and 765M bytes, respectively (pg 138).

Micropolis Corp.

Circle No 607

VIDEO GENERATOR

The Montest-AD8 video generator uses an 8-MHz dot clock to generate four test patterns—full raster, color bars, crosshatch, and windows—at any of eight user-selectable scan frequencies from 15.75 to 31.5 kHz (pg 302).

Network Technologies Inc.

Circle No 611

PLL SYNTHESIZER

The TBB200 CMOS PLL frequency synthesizer operates in single- or dual-modulus modes and is intended for use in radio communications equipment (pg 274).

Siemens Components Inc.

Circle No 608

Siemens AG

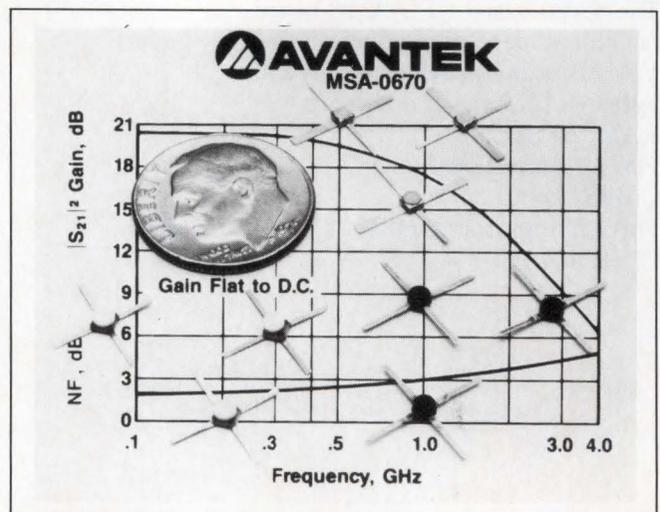
Circle No 609

FORMAT CONVERTER

The Interchange package transforms data from the 5¼- to the 3½-in. disk format and lets you transfer data from IBM PCs to PS/2 machines (pg 318).

SMT Inc.

Circle No 612



▲ AMPLIFIERS

These general-purpose monolithic microwave IC amplifiers are cascadable 50Ω gain blocks that can operate with power-supply voltages as low as 5V (pg 284).

Avantek Inc.

Circle No 610

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LEADTIME INDEX

Percentage of respondents

ITEM	Percentage of respondents							Average (weeks)	Last month's average (weeks)
	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Average (weeks)		
TRANSFORMERS									
Toroidal	0	16	63	16	5	0	9.3	8.7	
Pot-Core	7	7	65	14	7	0	9.4	10.0	
Laminate (power)	0	35	38	23	4	0	8.7	7.7	
CONNECTORS									
Military panel	0	15	38	39	8	0	11.5	11.2	
Flat/Cable	12	42	29	13	4	0	6.6	5.4	
Multi-pin circular	0	14	50	36	0	0	10.0	8.2	
PC (2-piece)	5	21	63	11	0	0	7.3	5.8	
RF/Coaxial	18	29	35	18	0	0	6.4	5.1	
Socket	14	41	38	7	0	0	5.3	3.6	
Terminal blocks	12	40	40	8	0	0	5.6	4.5	
Edge card	6	33	56	5	0	0	6.3	6.4	
D-Subminiature	13	29	50	8	0	0	6.2	4.5	
Rack & panel	6	41	35	18	0	0	6.8	7.4	
Power	6	41	29	24	0	0	7.2	7.4	
PRINTED CIRCUIT BOARDS									
Single-sided	5	57	33	5	0	0	5.1	5.9	
Double-sided	0	34	57	9	0	0	6.9	6.9	
Multi-layer	0	9	86	5	0	0	7.9	7.7	
Prototype	7	79	14	0	0	0	3.5	4.2	
RESISTORS									
Carbon film	40	30	27	3	0	0	3.6	3.3	
Carbon composition	38	31	28	3	0	0	3.1	5.0	
Metal film	23	40	34	3	0	0	4.4	4.4	
Metal oxide	19	44	31	6	0	0	4.8	4.9	
Wirewound	6	26	55	13	0	0	7.2	5.8	
Potentiometers	6	41	41	12	0	0	6.4	5.0	
Networks	14	45	41	0	0	0	4.7	5.7	
FUSES									
	32	42	21	5	0	0	3.8	3.8	
SWITCHES									
Pushbutton	11	44	30	15	0	0	6.0	4.8	
Rotary	0	48	35	13	4	0	7.3	5.3	
Rocker	12	44	32	12	0	0	5.7	5.2	
Thumbwheel	9	29	33	24	5	0	8.4	6.2	
Snap action	14	36	43	7	0	0	5.6	5.0	
Momentary	4	55	32	9	0	0	5.6	6.3	
Dual in-line	0	43	50	7	0	0	6.4	6.2	
WIRE AND CABLE									
Coaxial	36	36	28	0	0	0	3.3	3.7	
Flat ribbon	21	46	33	0	0	0	4.0	3.7	
Multiconductor	27	32	36	5	0	0	4.6	4.5	
Hookup	35	42	23	0	0	0	3.1	3.5	
Wire wrap	28	18	54	0	0	0	4.8	4.4	
Power cords	26	44	19	11	0	0	4.5	4.9	
POWER SUPPLIES									
Switcher	5	15	50	20	10	0	10.1	8.3	
Linear	6	19	44	25	6	0	9.5	7.8	
CIRCUIT BREAKERS									
	0	24	57	19	0	0	8.2	7.1	
HEAT SINKS									
	10	35	45	10	0	0	6.2	5.0	
RELAYS									
General purpose	8	33	42	17	0	0	6.9	5.6	
PC board	0	33	38	29	0	0	8.5	6.9	

ITEM	Percentage of respondents							Average (weeks)	Last month's average (weeks)
	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Average (weeks)		
RELAYS									
Dry reed	0	36	27	37	0	0	8.9	7.0	
Mercury	0	30	40	30	0	0	8.8	8.8	
Solid state	6	35	35	24	0	0	7.5	9.0	
DISCRETE SEMICONDUCTORS									
Diode	17	31	25	22	5	0	7.8	5.1	
Zener	12	29	24	29	6	0	8.8	5.5	
Thyristor	10	16	32	42	0	0	9.5	7.9	
Small signal transistor	4	38	29	21	8	0	8.8	5.7	
MOSFET	0	50	23	23	4	0	8.0	9.0	
Power, bipolar	0	40	40	20	0	0	7.5	8.0	
INTEGRATED CIRCUITS, DIGITAL									
Advanced CMOS	5	24	33	38	0	0	9.3	7.3	
CMOS	4	28	36	32	0	0	8.7	6.5	
TTL	19	39	27	15	0	0	5.7	5.9	
LS	18	39	25	18	0	0	5.9	5.2	
INTEGRATED CIRCUITS, LINEAR									
Communication/Circuit	0	38	25	37	0	0	8.9	8.5	
OP amplifier	11	26	37	26	0	0	7.8	7.1	
Voltage regulator	7	45	27	21	0	0	6.8	5.8	
MEMORY CIRCUITS									
RAM 16k	19	33	14	34	0	0	7.3	4.1	
RAM 64k	13	30	26	31	0	0	7.7	6.5	
RAM 256k	22	11	22	39	6	0	10.0	6.7	
RAM 1M-bit	8	17	25	42	8	0	11.1	11.8	
ROM/PROM	0	47	13	40	0	0	8.7	7.7	
EPROM 64k	8	33	21	38	0	0	8.5	6.5	
EPROM 256k	5	32	21	37	5	0	9.7	7.5	
EPROM 1M-bit	0	14	22	50	14	0	13.5	10.5	
EEPROM 16k	0	36	21	43	0	0	9.4	8.5	
EEPROM 64k	7	27	20	46	0	0	9.6	8.5	
DISPLAYS									
Panel meters	8	38	31	23	0	0	7.2	6.4	
Fluorescent	0	10	30	50	10	0	13.0	9.4	
Incandescent	12	38	0	50	0	0	8.9	6.9	
LED	8	46	23	23	0	0	6.8	5.4	
Liquid crystal	0	30	35	29	6	0	9.8	8.6	
MICROPROCESSOR ICs									
8-bit	8	40	20	32	0	0	7.8	6.8	
16-bit	10	33	9	48	0	0	9.1	7.0	
32-bit	6	35	18	41	0	0	8.9	9.8	
FUNCTION PACKAGES									
Amplifier	0	22	33	45	0	0	10.2	8.0	
Converter, analog to digital	7	13	40	40	0	0	9.8	7.9	
Converter, digital to analog	0	8	50	42	0	0	10.7	8.0	
LINE FILTERS									
	7	26	47	20	0	0	7.6	7.3	
CAPACITORS									
Ceramic monolithic	10	38	38	14	0	0	6.3	5.7	
Ceramic disc	13	33	37	17	0	0	6.5	5.7	
Film	15	27	35	19	4	0	7.5	5.9	
Aluminum electrolytic	12	34	30	24	0	0	7.2	7.1	
Tantalum	8	32	41	19	0	0	7.1	6.9	
INDUCTORS									
	5	27	50	18	0	0	7.6	6.3	

Source: Electronics Purchasing magazine's survey of buyers

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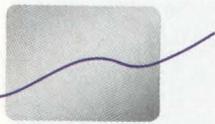
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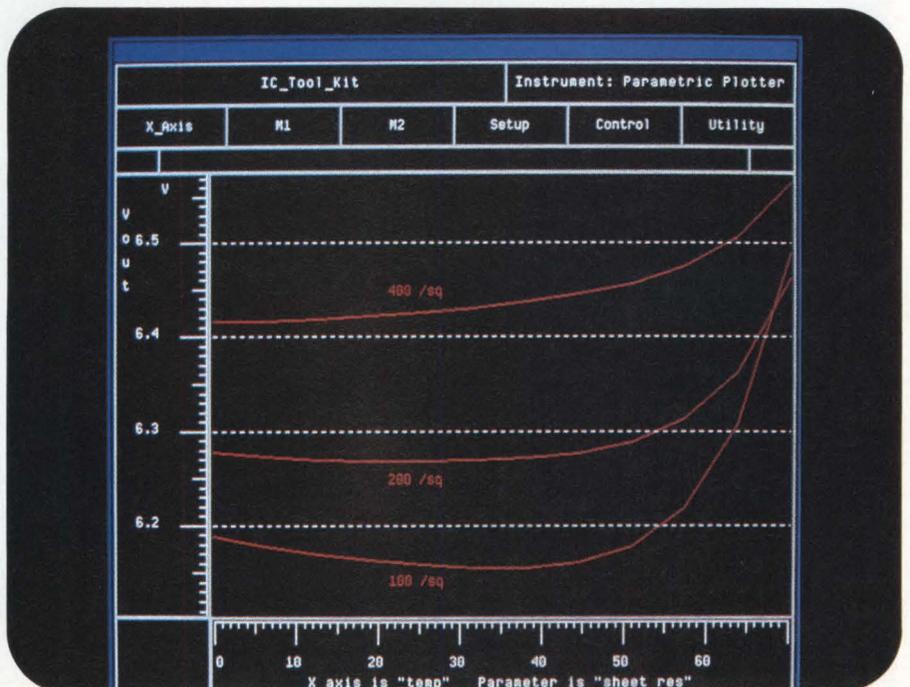


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EDN January 7, 1988



CIRCLE NO 109

113

Special Report



Real-time operating systems help speed software development by linking computer resources to your code modules. (Photo courtesy Ready Systems)



Real-time operating systems

A real-time operating system can enable you to design and write a large real-time software system as a collection of simple, potentially reusable routines. It can also help you avoid some difficult bugs common to real-time programming. But using a formal real-time OS system means learning a completely new programming style.

Charles H Small, *Associate Editor*

Two groups of software engineers face the need to adopt real-time operating systems: embedded-system, assembly-language programmers who are now confronting applications so large and complex that the projects demand formal programming methods (Ref 1), and high-level-language programmers who must use Ada. Although high-level-language programmers are comfortable with the complex tools, elaborate operating systems, and formal design methodologies needed for developing robust, maintainable software systems, and high-level-language and assembly-language programmers are familiar with the intricacies of real-time processing, both groups are entering unfamiliar territory when they begin to use real-time operating systems.

Using a real-time operating system to encase your application is like wearing armor into battle. The ar-

mored knight was better protected than an unarmored warrior. But the extra weight he was carrying also made him slower and less agile. A real-time operating system, especially when coupled with other, formal software-engineering methods, provides protection against the kinds of software disasters and blunders that unstructured development sometimes produces. Unfortunately, writing an *ad hoc* real-time system also extends the opportunity to write impenetrable "spaghetti" code (unstructured code) into another dimension—that of time.

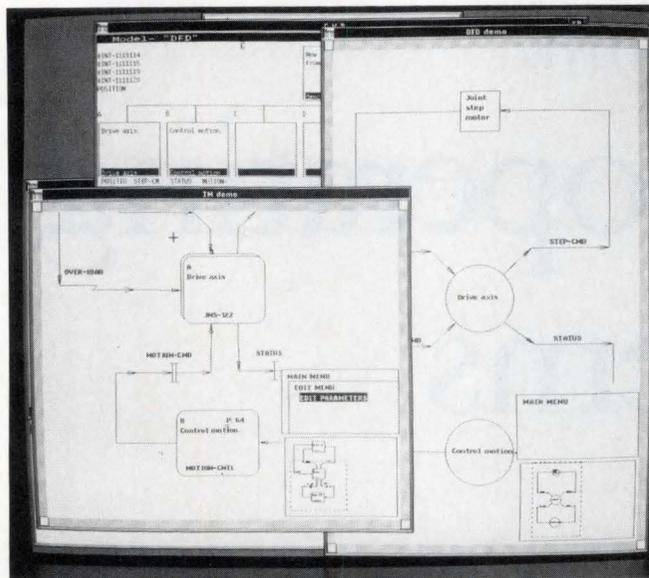
But a real-time operating system's protection comes at a price—extra CPU overhead. Also, submitting to the discipline of formal software-design methods means you will have to restrict the scope of your ingenuity and creativity to within the confines of the tool set the real-time operating system provides.

Real-time OS isn't just a check-off item

Many software engineers decide to write their own real-time executives. Who can blame them? A real-time executive is one of the most exciting projects a software engineer can undertake. And not every application needs a real-time operating system. Just because your application performs I/O operations does not mean you need an operating system. Further, if the state diagram for your application looks like a string of pearls, your application is batch oriented and will not benefit from concurrent processing. Further, some applications require such high throughput that they can't tolerate the overhead of any operating system, whether it's a real-time one or not.

Despite the attraction of writing your own real-time

After dividing your application into tasks, you'll need to set up intertask communication channels and protection mechanisms.



This display of a task map, data-flow diagram, and control map from Ready Systems' Cardtools CASE package documents a real-time software system.

operating system, you should consider adopting an available real-time operating system (Ref 2). A pre-written real-time operating system from an outside supplier does cost your company a license fee, but for the fee you get a reusable, and presumably debugged, system that you don't have to write. Thus, you can save some development time and debugging headaches. For example, even a small, embedded system doing a simple job may have to interface with a local-area network. Many real-time operating systems come with utilities and handlers for common local-area networks already written.

Industry observers report a disturbing trend among prospective first-time users of real-time operating systems to treat the real-time operating system as a check-off item (see **box**, "Considerations in operating-system selection"). No two available real-time operating systems are equivalent. Choosing an operating system demands close and careful examination.

Although all real-time operating systems are multitasking, not all multitasking operating systems are real-time systems. Unix, for example, takes far too long to answer interrupts and make a context switch to suit real-time applications. Its file structures suit program development but not on-line record keeping. Unix does not use re-entrant code; if 16 users invoke an editor, for example, Unix loads 16 copies of the editor. Hence, Unix consumes large amounts of memory. Further, it

has only rudimentary facilities for intertask communication and synchronization.

Two classes of real-time software exist: full operating systems (which include kernels) and stripped-down kernels themselves. Full operating systems are generally disk-based and are loaded into the host from disk every time you start up the host. Onboard ROMs, on the other hand, usually store kernels. The kernels are generally small in size, ranging from 2k bytes to as much as 100k bytes. For example, US Software's USX occupies fewer than 3k bytes.

Full operating systems have, in addition to their kernels, utilities such as file managers, debuggers, compilers, and editors, plus the myriad run-time utilities that high-level programmers need. Many of the full-blown operating systems, such as Technical Systems Consultants' UniFlex and Industrial Programming's MTOS-UX, mimic Unix but have different internal workings that suit real-time systems. Diab Systems' D-Nix is Unix compatible but can handle multiple μ Ps in real time. Integrated Solutions' UniWorks overlays Unix-compatible programs on Ready Systems' VRTX.

These distinctions are not clear-cut, however. Many full-blown operating systems such as Alcyon's Regulus, Microware's OS/9, and Intel's iRMX offer a subset of the operating system as ROMable kernels. And kernel makers such as Ready Systems and Software Components Group have file and debugger options that you can add to their basic kernels. Most do what JMI Software Consultants Inc has done for its C Executive—they offer run-time libraries you can use to call the real-time operating kernel's primitives from your high-level programs. Further, JMI has rewritten 300 common Unix run-time libraries so that they are re-entrant and ROMable and so they can be used in a real-time system. In other words, the kernel manufacturers are moving toward full-blown operating systems while the operating system makers are moving toward kernels.

Some real-time operating systems are targeted for specific μ Ps; others are available for a range of common μ Ps. Intel's iRMX works only with Intel μ Ps. Microware's OS-9 is written in assembly language for 68000-family μ Ps. JMI Software Consultants's C Executive is written in C, and the firm can adapt it for any μ P that has a C compiler.

Generic operating systems are, by definition, more portable than specially targeted systems. Assembly-language operating systems, on the other hand, can be faster and more compact than ones written in high-level languages. And an operating system targeted for a

Considerations in OS selection

You'll probably already have selected a μ P and system bus for your real-time system before you begin to look for a real-time operating system or kernel. When choosing a system, consider—at minimum—the following characteristics:

- Response time (interrupt latency)
- Kernel or full operating system
- Coprocessor support
- Multiprocessor support
- Other hardware support—clocks, timers, interface chips, buses
- Other μ P's supported
- Software drivers—terminal, I/O boards, disk, tape, networks, graphics
- Host development aids
- Target-system, ROM-resident monitor
- Debugger
- Performance analyzer (program profiler)
- License fees.

specific μ P can more easily take advantage of a given μ P's special features.

Some of the memory-protection hardware of advanced μ P's suits multitasking systems. This hardware can keep one task from corrupting the program or data of another task. Some advanced μ P's have special instructions for task switching, semaphore signaling, and debugging. But some features of advanced μ P's impede real-time processing.

For example, a numeric coprocessor can increase the number of registers and the amount of data that a real-time operating system must save and restore when doing a context switch. And context switching, like subroutine jumping, destroys the effectiveness of instruction-prefetch queues and cache memories. Further, no advanced μ P's come with features that handle common real-time operating-system overhead such as prioritized-list management.

Computer boards come with real-time OSs

As evidence of electronics engineers' growing interest in real-time operating systems, computer-board manufacturers are beginning to offer specially targeted real-time-operating-system ROMs along with their CPU boards. Along with its 68020-based VME boards, for example, Force Computers now offers a

customized, ROM-resident version of Eyring Research Institute's PDOS operating system at no extra charge. The 16-bit μ P versions will appear later. Force's subset of PDOS functions, dubbed the VMEPROM, includes a file manager and basic I/O modules, as well as RAM-disk support, a screen editor, disk utilities, and a debugger.

Dyad Technology Corp has a board with a version of Ready System's VRTX that's specially designed for the IBM PC. You can even get real-time operating systems for the smallest of computing engines: single-chip μ P's. Avocet Systems Inc, Intelligent Machinery Co, and Micro Computer Control have high-level language compilers and real-time operating-system kernels for μ P's such as the 8051 family. In particular, the Intelligent Machinery Co's imx/51 manual comes with numerous functional, clearly written examples that serve as a tutorial on real-time programming for the 8051 family.

Introduction to new tools and design methods

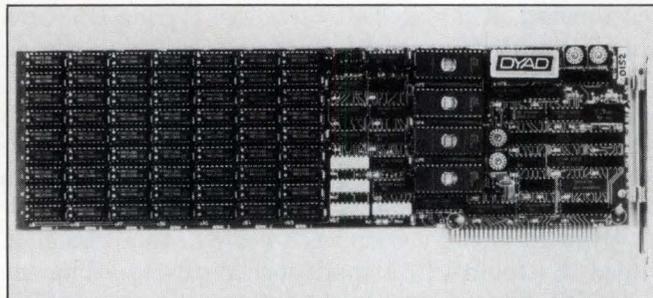
But simply deciding to adopt an operating system is only the beginning of the transformation you must undergo when switching from writing ad hoc, sequential code and operating systems to more formal, real-time coding. Real-time operating systems are but one weapon in a software engineer's panoply. The real-time operating system is an armature upon which you hang your application. No matter how robust the operating system's mechanisms may be, they can't make up for a poor design. Long before you actually begin to write routines that invoke the operating system's resources, you should perform a thoroughly documented, top-down design.

For example, to make effective use of an operating system's intertask-communication mechanisms, you should have a clearly thought-out data-handling protocol along with a complete data-flow diagram.

Real-time operating systems generally do not do much error checking and exception handling. Therefore, you must set up and enforce rules to ensure that your tasks pass properly formatted messages and parameters that are within specified ranges. You must also set up your own error-checking and error-recovery routines.

According to US Software, you should carefully chart all intertask communication before writing your programs. Such a chart will greatly reduce debugging and "thrash" time you might otherwise spend when checking out your system. The firm does not suggest that the communication chart can take the place of other design

Any real-time, multitasking OS that performs pre-emptive scheduling must occasionally turn off either its scheduler or the μ P's external interrupts.



With the aid of this plug-in, real-time operating-system board from Dyad Technology, you can get real-time performance from your IBM PC.

documentation, but rather that it's an adjunct to that documentation.

The firm recommends that the communication chart should include (as source and destination points) tasks, common-code routines, and user-interrupt routines. You should annotate the arrows between these points to indicate the direction of data flow as well as the type of communication (event parameters, accept or release, clear or set, mailbox, message type, wake-up call, etc) and any other useful information.

At present, only Ready Systems can supply computer-aided tools for formal design methods that apply specifically to real-time systems. Without Ready Systems's Cardtools, you will have to do your formal, top-down design, and documentation manually. Cardtools can produce software documentation in the style of DoD-STD-2167 (which is required in Defense work).

Cardtools is an elaborate suite of programs whose functions span three phases of a formal software-engineering project: software-requirements specification, high-level design, and detailed design. After these three phases, you are still left with coding and testing, integration and debugging, installation and operation, and maintenance.

Cardtools begins with a graphics-oriented diagram and text editor with which you can decompose functional and data specifications to any number of levels. Like all the programs in the Cardtools package, the specification tool saves all the data you enter in a common Cardtools database. And, because it is more than a passive graphics editor, it does completeness and consistency checks as well.

Next, the package's rapid-prototyping facility lets you set up user screens. It automatically generates source code for the displays. (In computer-aided software-engineering (CASE) circles, rapid prototyping generally means dummyping up the user interface. The

resulting dummy prototype often passes for a demonstration program.)

Another tool then prompts you for complete specifications for logical and numeric data definitions. Hopefully, by declaring I/O parameters early in the design cycle, you will be able to catch such errors as misrepresentation of data, out-of-range excursions, and design overkill.

An Ada-related tool allows you to build libraries of related functions into Ada "packages." This tool helps you follow the Ada programming style and additionally gets you thinking early on about reusable routines.

By this point in the sequence of applying the tools, the Cardtools database has acquired much information about your design. It can now automatically produce a data-flow diagram (but you can draw your own, if you wish). Nearly all software-engineering gurus recommend a comprehensive data-flow diagram as an aid to rational, reliable use of an operating system's communications and task-synchronization primitives.

Cardtools even has a program that will help relieve the principal source of anxiety for real-time software engineers—especially those unaccustomed to real-time systems; it provides an early estimate of the most important spec for a real-time system—its speed. The package's real-time performance-verification tool performs critical-path analysis on your design's multitasking architecture. The tool uses the specifications you entered in the Cardtools database to evaluate your system's timing response.

Last, a program-design-language (PDL) editor and analyzer accepts and checks structured-English (psuedolanguage) versions of your program's routines. Ready Systems claims that using a PDL editor before beginning to code in your real high-level language increases work at the design stage by 5% but trims 15% off the overall design effort.

Software engineers who must work with Ada should remember that Ada is not just a compiler. The Ada specification covers all phases of a project from specification to debugging. At present, Ada users have enough to worry about just to find an efficient compiler. But eventually, Ada tools will have to expand their coverage to meet all DoD specs.

Guidelines for task splitting

However you design your real-time system, manually or with CASE tools, the most important phase of the design is dividing the application into tasks. While no hard-and-fast rules apply to partitioning an application

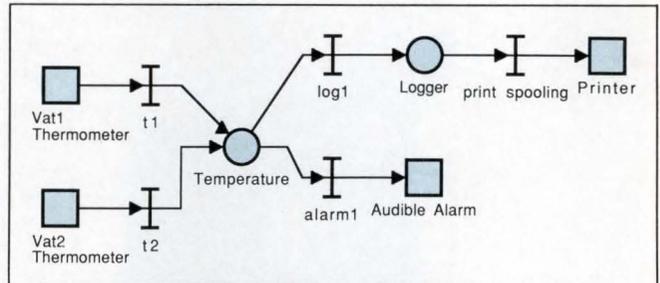
into tasks, some general guidelines apply. First, you should split the processing load into small tasks, each task having generally only one function. A task, therefore, is the smallest unit of execution that can compete on its own for system resources. A task inhabits a virtual, insulated environment that the real-time operating system provides. In this environment, the task can use—or, if necessary, can wait until it can use—any of the real-time operating system's resources without explicit concern for any other tasks in the system.

You should divide your tasks so as to minimize intertask communication. Too much intertask communication exacts a penalty in the form of too much operating-system overhead. Because intertask communication increases dependencies among tasks, intertask communication is at odds with the goal of partitioning software into autonomous tasks. If you find your application doing too much intertask communication, you may have partitioned your tasks poorly, or you may be trying to use a real-time operating system in an application it's not suited for.

Naturally, you must devote considerable thought to assigning priorities to tasks. Do not confuse priority with the amount of CPU time a task will consume. You could very well have a very-high-priority task that runs infrequently, and that, when it does run, runs for a short time before going back to sleep. Conversely, you could have a low-priority task that consumes the bulk of the CPU time but can tolerate interruptions at any time.

Similarly, don't confuse hardware-interrupt priority with software-task priority. You could have an input or output port with a high hardware priority—a high-speed data link, for example. But a simple hardware-interrupt handler could respond to the high-priority hardware interrupts and do no more than put the characters from the high-speed link into a buffer for later processing by a low-priority task. This situation is not uncommon because many I/O channels are "bursty" in nature; that is, they have short, intense bursts of communication interspersed with long periods of inactivity.

Generally, the system-clock interrupt has the highest priority for real-time operating systems that do time slicing. You may have to assign some other hardware interrupt a higher priority, but in so doing, you may disrupt your system's timing. Because the priority of tasks influences the performance of the overall system, be prepared to do some experimentation until you fine-tune your system's performance sufficiently.



*In this data-flow diagram of a real-time system, squares are external devices, I-beams are communications interfaces, and circles are tasks. The diagram was produced with a graphics editor, from *Andyne Computing*, that allows you to document the structure of a real-time system.*

In all cases, you must partition processing not only among tasks, but also between interrupt handlers and their respective tasks. The general rule is to make interrupt handlers as short as possible and to do as little processing as possible in the handler.

Dangerous calls for interrupt handlers

Even though your interrupt handlers must be as short and fast as possible so as to minimize the time the μP turns off interrupts during an interrupt service, interrupt handlers still interact frequently with the operating system and your higher-level tasks in the system. For example, the interrupt handler might have to acquire a memory buffer from a memory pool. Not all of a kernel's function calls are safe for an interrupt handler to make.

Generally, an interrupt handler can make with impunity any call that creates a structure. Interrupt handlers can write and read data as safely as any other software entity can, providing they obey the protocols you've set up for your system.

Any kernel function call that sends the operating system a signal that could change the state of a task can be dangerous if the handler does not first lock the system scheduler. You should use caution when employing such calls in an interrupt-service routine simply because interrupt-service routines occur asynchronously by nature, and they could cause unexpected behavior in the tasks they affect.

Even more dangerous for interrupt handlers to call are blocking commands that lock out high-level tasks from a memory area or a system resource. Further, you should not allow interrupt handlers to perform system calls that create or delete tasks.

After you've designed your real-time system, you will have to begin coding the individual modules and

asionally turn off either its scheduler or the processor's external interrupts—or both—to allow a task to execute what are termed "critical" code regions.

A critical region is any program sequence, in one of the system's tasks or within the operating system itself, which cannot tolerate being interrupted. Take, for example, the prioritized lists that operating systems must constantly update. If the operating system is in the process of ordering a list of prioritized tasks, it must not be interrupted by a task that wants to change its priority or by a task that wants to join the queue until it's finished ordering the tasks at hand.

Similarly, a task could be updating or accessing a shared area of memory. The task must be able to work with the shared memory without the risk that some other, higher-priority, task will interrupt and change the common memory before the lower-priority task is finished. Protecting these critical code regions obviously affects the system's ability to process interrupts in a timely fashion, because lower-priority tasks can lock out higher-priority ones.

Lengthening interrupt latency

Critical regions in the operating system and in your task's code both affect the most important specification for real-time systems: interrupt latency. If the operating system, or your tasks, have turned off interrupts or disabled task scheduling, a delay will occur before an interrupt is serviced or processing begins. Obviously, a maker of real-time operating systems can't supply a spec for how your critical regions will affect interrupt latency.

But the complexities of the inner workings of real-time operating systems make giving clear-cut, useful specs for interrupt latency difficult for makers of real-time operating systems to supply as well. Even if one particular maker *can* supply a useful spec for its system, the specs depend heavily on the hardware used (the μ P, memory, memory manager, coprocessor, etc) and the software test setup (the number of tasks in the test system and the synchronizing scheme selected, for example). This lack of uniformity of test conditions makes comparing latency specs for competing real-time operating systems next to impossible.

The performance of some real-time operating systems depends on how many tasks the operating systems are handling and what state the tasks are in. Pre-emptive, prioritized real-time operating systems must manage many lists and queues. These operating systems must constantly update their lists and queues in

response to external interrupts and operating-system calls from tasks. Depending on just how a real-time operating-system designer writes his code, the real-time operating system's overhead can increase as the number of tasks increases simply because the real-time operating system has more items to keep track of.

Other task-dependent effects on an operating system's interrupt latency can arise from the management of queues attached to common data structures and intertask-communications mechanisms. As the number of tasks waiting grows, the operating system's overhead for managing these resources can grow. These and other sources of variable interrupt latency can bedevil a user of real-time operating systems because most real-time systems must meet a minimum interrupt-response specification.

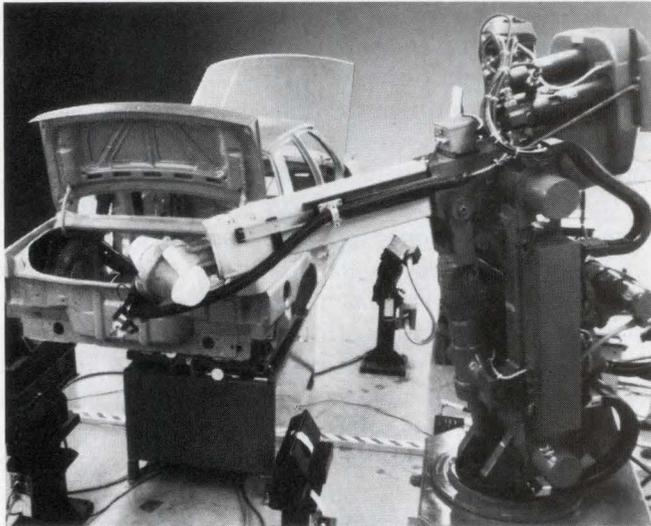
One real-time operating system sidesteps many of these problems by simply having no scheduler and little need for critical-code lockouts. The operating system, Forth Inc's PolyForth, has an extremely simple mechanism for task switching that entails minimal overhead. Further, it relies on self-scheduling tasks rather than a pre-emptive scheduler to initiate task switching and thus avoids scheduler overhead simply by having no scheduler. PolyForth's schema is easy to understand and you could easily copy it if you wished to concoct your own real-time operating system.

PolyForth's task switching starts from a simple idle loop. Each task in the system has a Long Branch—or Long Jump—instruction at the head of its task area. The argument of the Long Branch instruction is the address of the head of the next task in the idle loop. When all the tasks are quiescent, and the idle loop is running, the system's μ P simply jumps from task to task endlessly in round-robin fashion.

When the μ P receives an external interrupt, it vectors to an interrupt handler. Unlike more complex systems that interpose the operating system between an interrupt handler and its associated task, each PolyForth handler knows which task it must work with. The handler performs any time-critical processing needed by the external interrupt and, just before executing a Return instruction, changes the argument of its associated task's Long-Branch instruction from the next task's address to the entry point of a routine that wakes tasks up.

Whenever the idle loop finally jumps to a task that an interrupt handler (or, perhaps another task) has marked for awakening, the idle loop detours to the wake-up routine. The wake-up routine knows which

The complexities of real-time operating systems make it difficult for the OS vendors to give clear-cut, useful specs for interrupt latency.



Because robotic vision systems must respond to sensory inputs as they perform their tasks, they require real-time operating systems. (Photo courtesy Software Components Group)

task needs to be awakened because the task's address is on the μ P's return stack. The wake-up routine restores the task's registers and transfers control to the task's program so that the task can pick up where it left off in its program.

The task now has control of the μ P, and only external interrupts can temporarily take control away from it; no other task can pre-empt the controlling task. No other high-level task can get control of the μ P and begin running unless the currently running task voluntarily relinquishes control. In other words, PolyForth needs no scheduler because it is self-scheduling.

The Forth programmer has two ways of putting a task to sleep: The programmer can insert a Pause or a Wait command in the program's flow. If a task pauses, it puts itself to sleep and jumps to the next task in the idle loop. But it leaves its Long Branch instruction in the head of its task area, pointing to the wake-up routine. Thus, the next time the idle loop reaches the task, it will wake up. Alternatively, if the task executes a Wait, it puts itself to sleep and changes the argument of its Long-Branch instruction to the address of the next task in the idle loop. In this case, the idle loop will not activate the task; it will remain asleep until some external agent—an interrupt handler or another task—marks it for awakening.

Several characteristics of Forth facilitate this simple scheme; not all high-level languages could use this scheme as easily. Saving or restoring a Forth task—a context switch—takes little time because Forth uses

only three μ P registers. A Forth task initiates a context switch by executing a Forth word. (Executing a Forth word is equivalent to calling a subroutine in other languages; in fact, executing subroutines is the fundamental, native way in which Forth programs execute.) By initiating task switches with Forth words, rather than at the arbitrary behest of an operating system, a Forth task naturally breaks its execution after completion of a routine rather than being interrupted in the middle of doing something. Breaking at the end of a function decreases the amount of data that the context-changing routine must save, because well-written Forth words generally tidy up system resources before exiting.

And because no task can pre-emptively interrupt another task, the programmer need only worry about interrupt handlers corrupting resources (a data structure, common memory area, or intertask communication or synchronization mechanism) while the task is working with them. Thus, PolyForth does not need many of the complex critical-code-lockout and protection schemes of pre-emptive operating systems.

The success of PolyForth's schema rests on your ability to fine-tune your overall system by peppering each task with judiciously placed Pauses and Waits so that no one task can hog the system. As it does in many other areas, Forth leaves it to you to custom-make constructs and functions that other operating systems and languages come with. For example, you'll have to write your own arrays, semaphores, mailboxes, and servers.

On the other hand, some unique hardware is available for Forth. Most languages are customized for certain hardware. Like Lisp, however, Forth has hardware customized for the language. You can get a Forth μ P from Novix Inc (Cupertino, CA); an enhanced version of the Novix μ P is also available as a standard cell from Harris Semiconductor (Melbourne, FL). This μ P executes common Forth words in a single cycle. Further, it has no instruction queue, and it can also jump to an interrupt routine in a single processor cycle. The chip's architecture thus makes context switches and interrupt handling very fast.

At the heart, a kernel

At the heart of every real-time operating system except PolyForth is a real-time kernel. The kernel is a small set of programs that schedule tasks, manage resources, and provide mechanisms for intertask communication and synchronization (the Forth kernel exe-

cutes Forth). The kernel provides the mechanisms that you use to set up your system. It provides the means; you set the policy. For example, if the kernel has a prioritized scheduling mechanism, you set policy by assigning priorities to your individual tasks.

Protection or lack thereof

If a real-time operating system's kernel is to have high performance, then it must assume that the tasks you have written are correct. Otherwise, if your tasks can't be trusted to confine their reads and writes to authorized areas of memory and to pass properly defined parameters, the real-time operating system's kernel will have to spend extra time doing error checking and parameter validation.

Real-time operating systems' kernels also do not do exception or error handling. If one of your tasks requests a service call that the real-time operating system's kernel can't execute, the kernel will simply return an error code. Your tasks must be prepared to decipher these error codes and take appropriate action.

Semaphores

Real-time operating systems do provide a host of special function calls. The simplest, in theory at least, is the semaphore. A semaphore is a simple software mechanism for granting control of a shared resource to one task at a time. Conceptually, the classical semaphore is a counter with a queue attached. Tasks can perform only two operations—Signal and Wait—on a canonical semaphore. A Signal increments the counter and a Wait decrements it. If the counter's value is zero, any and all tasks performing a Wait join the queue and actually begin waiting until enough Signal operations occur to flush the waiting tasks from the semaphore's queue. Semaphore operations are good examples of critical regions. Some real-time systems use the classical semaphore; others have embellished it considerably.

Sometimes, a semaphore is implemented as a memory location or variable that contains a "token" only when the resource is available. The token functions as the key to a hotel room does. A task wanting to use the resource first must check the semaphore (or signal it, depending on which real-time operating system you use) either by reading the variable or by doing a system call to see if the token is available. (In the case of an operating-system call, the operating system functions as a hotel desk clerk, handing out keys and checking tasks in and out.)

If the task gets the token, it can use the resource. If

no token is available, the task can wait or do other processing until it gets the token. Simple systems require the blocked task to wake up repeatedly and poll the semaphore. More-sophisticated systems allow a task to put itself to sleep pending a wake-up call from the operating system. When finished with the shared resource, the task must return the token to the variable or to the operating system, as appropriate.

Microware Systems Corp's OS-9 has an extension to the classical semaphore that the firm calls an Event. The Event accepts the basic Signal and Wait commands of the classical semaphore; tasks can queue up in FIFO buffers while awaiting a blocked semaphore. Further, the Event has a counter just like a semaphore's. A successful signal-function call will cause the counter to count up by a fixed increment (you specify the increment when you set up the event). A successful Wait function call will reduce the counter's count by the specified increment.

The purpose of the counter becomes clear when you learn that the Wait function call requires an argument specifying a range for this event counter over which the Wait call will activate a given sleeping task. That is, after a successful signal call, the operating system will search the Wait queue and activate *all* waiting tasks whose prespecified range encompasses the new value for the event count. Thus, the Event resource can launch multiple tasks with one Signal.

Variations of the basic Signal call can jam a value into the event counter, increment it by a value other than the value fixed when the event was set up, or change the event counter's value temporarily (for one function-call cycle). This powerful, extended semaphore endows OS-9 with subtle intertask synchronization properties that experienced users can exploit creatively.

The exact nature of the token is not relevant to understanding the mutual-exclusion mechanisms. Operating-system designers have made use of the token differently. For example, Forth programmers use a zero as a token; if a task finds nothing in the mutual-exclusion location, then it writes its task-identification number into the location to take possession of the shared resource. If another task polls the location while the first task is in control of the shared resource, the polling task will not only know that the shared resource is busy, but will know which task is using it.

Digital Resources's FlexOS has an unusual, complex, and powerful meaning attached to the value of a token. When a task executes any FlexOS system call that could be followed by a Wait operation, the OS returns a 32-bit

Text continued on pg 126

Glossary of real-time-software terms

Programmers sometimes use old words in different ways, coin words, or—confusingly enough—use several different words to describe what's more or less the same thing. For example, "exchange," "port," "channel," "socket," and "message" are all synonyms for "mailbox." The following glossary explains some commonly used real-time-software terms.

Activity—Synonym for *task*.

CASE—Computer-aided software engineering.

Context switch—A context switch occurs when, in a fashion similar to a subroutine call and return, one program is frozen and everything important to that program is stored in main or off-line memory: usually μ P registers and pointers to private data structures (and coprocessor registers). Next, another program's registers and pointers are loaded into the μ P. In some multi-tasking systems, an entire program and its attendant data structures are overlaid in core memory from off-line memory (real-time programs can't generally tolerate such overhead; consequently, for real-time systems, all *tasks*, running or suspended, usually reside in RAM). And finally, execution of the second program begins, starting at the location pointed to by the restored program counter.

Critical region—Any sequential segment of a program's code that can't tolerate interruption. Generally, a *task* must bracket the critical region with a pair of system calls to first lock out, and when finished, enable, operating-system interrupts. If you want your system to continue to answer external interrupts while a task is in a critical region, make sure that your interrupt-

service routine is not able to corrupt any processing that any task may have undertaken while in any critical region.

Deadlock—A condition in which each of two tasks waits for the other indefinitely. Deadlock results when two *tasks* attempt to control the same two *resources* at once. Each task can be in possession of one resource while waiting for the other task to release the other resource; thus, the tasks will wait forever.

De-reference—Etymologically unsound (compare to "delouse," for example) but useful neologism current among C programmers; it signifies retrieving an object pointed to by a pointer as opposed to directly referencing the pointer itself.

Event—Term used by Micro-ware's OS-9 for a semaphore having some special extensions to the canonical *semaphore*. More generally, an event is anything that stimulates a program and eventually results in a *context switch*.

FIFO—First in, first out. Taken in strict order of arrival.

Hook—The means whereby you can add your own code to an operating system. A simple form of hook is a Jump from the operating system's ROM to a RAM location. If you don't use the hook, you must initialize the RAM location with a Jump right back into the next location after the hook in the operating system's ROM. If you use the hook, you simply start your code at the destination of the hook's Jump command and eventually Return to the operating system's ROM upon completion of your addition.

Kernel—A kernel can be loosely defined as the bare-minimum skeleton of an operating system

that can sustain real-time multi-tasking. A kernel usually includes simple I/O calls, a context switcher, a system-timer task, and *mutual-exclusion* mechanisms. It doesn't usually include file I/O, a debugger, complex I/O such as local-area networks, or any program-development aids.

Library/libraries—An ambiguous term that can refer, in either singular or plural form, to either an entire library of programs or a program from a library. Presumably, "library program" was shortened to "library" just as "peripheral device" was shortened to "peripheral." The terms lead to such confusing utterances as: "You take the libraries from the appropriate library and include them as needed."

Logical—As used by programmers, the term is a synonym of "virtual"; it refers to the opposite of "physical" or "real," not the opposite of "illogical." It denotes the way a program interprets something as opposed to the thing's physical reality in the system's hardware. For example, a program running in a memory-management system may think it begins execution at address zero when, actually, it doesn't: The memory-management hardware adds an offset to the logical address to produce the real, or physical address in memory. The OS-9 manual provides an example of the way programmers use the term: "Because all OS-9 files have the same physical organization, file-manipulation utilities can generally be used on any file regardless of its logical usage . . . text file, executable program-module file, data file, [or] directory."

Mailbox—A secure mechanism, or *object*, for communication be-

tween asynchronous tasks. More than just a simple shared memory area, a mailbox has a *mutual-exclusion* protocol which keeps more than one *task* from accessing the mailbox at one time. Many mailboxes have message-deposit and message-wait queues attached to their mutual-exclusion protocols that allow multiple readers and writers to queue up and wait at a mailbox. Some even accept a stack of messages.

Maintenance—That portion of the software design and debugging process that continues after the program gets shipped to a paying customer (as opposed to a beta-site customer).

Mutual exclusion—Allowing only one *task* to have access to a shared *resource*—either a physical device or a data structure—at any given time. Mutual-exclusion mechanisms can also protect non-reentrant code and make it a serially reusable resource.

Object—An abstract software-engineering concept. An object is the combination of a data structure and the program needed to manipulate the data structure, considered as a unit. An array created by the DIM command is an example of an object. External routines have no control over the object's code, and they can't manipulate its data structures directly. *Mailboxes*, *semaphores*, arrays, variables, and even *tasks* are all objects.

Object-oriented programming—A programming style said to make large complex programs manageable. Each data structure, along with its associated code, gets partitioned off from the rest of your program and becomes an *object*. You attempt to hide as much as possible of the

internal working of each of these objects from the rest of the program. Also, you should strive to make the interface for all your objects as uniform and simple as possible.

Pipe—Unix name for a large FIFO buffer masquerading as a pair of files. Asynchronous *tasks* can communicate large amounts of data through a pipe. The task writing to the tail of the FIFO buffer thinks it's writing into a file; similarly, the task reading from the head of the FIFO buffer thinks it's reading from a file. Actually, the pipe is usually a memory buffer. So that programmers need only master one set of I/O commands, elaborate operating systems such as Unix disguise this form, and all other forms of I/O, as read and write operations to files.

Pre-emptive—A pre-emptive *resource* services requesters in order of their priority, not their arrival.

Primitive—Synonym for service call or function call to the real-time operating system *kernel*.

Process—Synonym for *task*.

Re-entrant code—A program segment that does not modify itself locally. Because any number of asynchronous *tasks* can use this segment without interfering with each other, re-entrant coding helps make a real-time system compact.

Resource—Defined loosely, a resource can be any physical device, data structure, or mechanism for intertask communication or synchronization that the operating system manages (and perhaps guards from blundering or malicious programs).

Semaphore—A simple software mechanism for granting control of a shared *resource* to one *task*

at a time.

Supervisor—An ambiguous term. Some operating systems distinguish between the *kernel* and the supervisor (which sometimes includes the kernel). The kernel handles *task* scheduling while the supervisor handles I/O. Others use the term "supervisor" to refer to the portion of the kernel that schedules tasks.

Task—An abstract software-engineering concept. A task is an autonomous, asynchronous program that thinks it's running all by itself. How you divide a given software system into tasks is purely arbitrary.

Time slicing—The *supervisor* in a real-time operating system *kernel*, in response to a system-clock interrupt, deals out a defined segment of CPU time to a series of *tasks* in round-robin fashion. Pre-emptive schedulers generally do round-robin time slicing when a system has several ready-to-run tasks all at the same priority level.

Unit—An Intel iRMX term for the *token* that a *semaphore* returns to a calling *task* to indicate that the task has possession of the semaphore. Intel reserves the term "token" for the pointer that a calling task gets from the operating system after successfully acquiring an iRMX *object*. The distinction is that the unit's content has a meaning only for the operating system and not for the calling task; the task merely keeps the unit temporarily and returns it to the operating system when it's finished with the semaphore. On the other hand, the calling task uses the iRMX token to both take control of, and find, the iRMX object.

Virtual—Synonym of *logical*.

At the heart of every real-time operating system is a real-time kernel.

token to the calling task. The token has only one of the 32 bits set—in other words, it's a 1-bit bit mask.

The task does not know or care just which bit, of the 32 available, the operating system has set for that particular call. However, the operating system does keep track of which bit is set in each token possessed by each task. A given task can make as many as 31 requests, logically OR all of the tokens together, and pass the resulting bit mask to an operating-system Wait call. Note that the task does not simply take the token and begin using the resource. It must make an explicit Wait call. If the resource is available, the operating system will wake up the task immediately after the task makes its Wait call.

The power of this mechanism is the flexibility it gives you to suspend a task. Most real-time operating systems allow a task to wait for only two things at once: an event or a timeout (the event can be an unblocked resource, a message arrival, or an interrupt). A FlexOS task can wait for the first of 31 events to occur. The operating system also provides a software-interrupt mechanism for the cases in which the bit-map token approach proves cumbersome and time consuming.

Semaphores have three kinds of queues

Intel's iRMX semaphores can have more than one token available if the shared resource has more than one unit available. You could use such multiple-token semaphores to regulate a producer-consumer relationship of, for example, a memory pool having several buffers within it.

Intel's iRMX semaphores have further embellishments. Three different kinds of queues are attached to each semaphore. Tasks that find themselves blocked when they try to use a resource guarded by a semaphore can wait in a FIFO queue or a prioritized queue (the task with the highest priority goes to the head of the queue even if it was the most recent one to join). Further, iRMX semaphores include a unique prioritized mechanism that the firm calls a Region.

Regions are not, in Intel terminology, areas of memory. Rather, they are prioritized semaphores with special properties. Regions have only one token to give. While a given task has the Region's token and is in control of the shared resource, the task's priority can change dynamically. After the task gives up the token, its priority returns to its predefined level. The task holding the token has its priority raised to the level of the *highest-priority* task waiting in the queue for the Region.

The reasoning behind this seemingly arcane mechanism is simple if you consider the following example: Suppose a low-priority task gets control of the resource guarded by the Region. Next, while the resource is blocked, a high-priority task joins the Region's queue and waits for the low-priority task to give up the token. But before the low-priority task can finish using the resource, it gets pre-empted by a medium-priority task that is not waiting in the Region's queue.

In effect, the medium-priority task has blocked the high-priority task because the low-priority task can't run to completion. The Region mechanism owes its existence to this subtle but troublesome problem, which, unfortunately, is only one of many subtle problems that arise from even as seemingly straightforward and simple a real-time mechanism as a semaphore.

Deadlock and how to avoid it

The most commonly cited problem you might incur when coordinating multiple tasks with semaphores is deadlock, a condition in which each of two tasks waits for the other indefinitely. You risk deadlock if you allow your tasks to attempt to control more than one resource at a time. Imagine that you have two tasks and two shared resources. Each task captures control of one of the two resources. Then each task attempts to acquire the resource the other task controls. Failing to gain control, one task puts itself to sleep to await its turn at the resources the other task controls.

However, the other task will also fail in its attempt to gain control of the resource that the first task controls. Because it's blocked and asleep, the first task will never release its resource. Therefore, the second task has no choice but to put itself to sleep to await the release of the other resource. Both tasks are blocked forever unless you set a timeout before requesting resources. Even if you have set a timeout, your tasks must still resolve the deadlock when they wake up from their unsuccessful attempts to get the resources.

If you have no choice except to allow your tasks to control multiple resources, you can avoid deadlock by requiring tasks to request and release these resources in the same sequence and by dynamically adjusting the controlling task's priority in a fashion similar to Intel's Region. In other words, order your shared resources and assign them a number. Then, you must enforce the following discipline: Tasks must request control of the resources in ascending order and release them in descending order. That way, a task will be able to gain control of either an entire group of resources or none at

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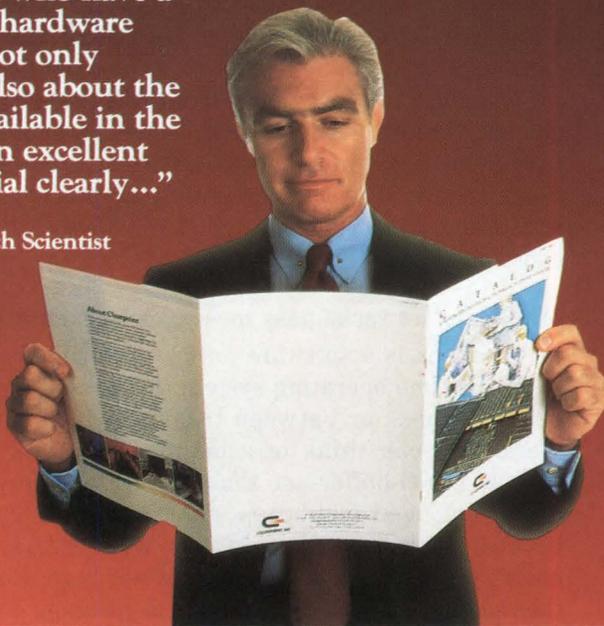
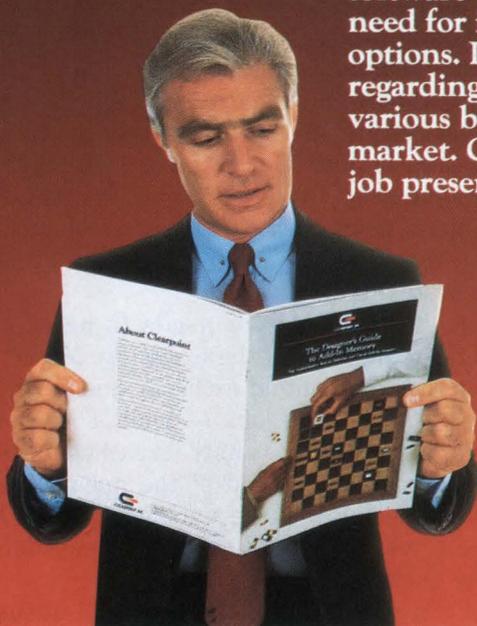
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The most commonly cited problem you might incur when coordinating multiple tasks is deadlock.

all. And because the controlling task's priority is momentarily adjusted up to the level of the highest-priority task that's waiting for the group of resources, lower-level tasks will not be able to block the waiting high-level task.

Semaphores allow independent tasks to share non-reentrant resources safely. Tasks could communicate by placing messages in a shared memory area protected by a semaphore. But most real-time operating systems have a special mechanism, called a mailbox, for passing short messages.

Mailboxes let tasks pass messages to each other

A mailbox is a software entity, normally controlled by a real-time operating system, for passing messages between tasks or between tasks and interrupt handlers. You can think of a mailbox as an extremely shallow FIFO buffer—so shallow that it holds only one item. You need mailboxes when you send messages between asynchronous tasks. The writing task posts a message to a mailbox whenever it needs to. Similarly, the reading task attempts to get the message out of the mailbox at a time appropriate for its program sequence. Naturally, the operating system must provide for mutual exclusion to ensure that the two tasks do not try to access the mailbox simultaneously.

Real-time-software engineers often employ mailboxes in pairs to effect a software simulation of a 2-wire handshake: The posting task uses one mailbox to send a message, and the receiving task uses another mailbox to acknowledge receipt of the message.

Also, if the reading task has not yet picked up the message previously posted by the writing task, the operating system must return an error code to the writing task. In other words, the writing task needs to know that its letter was picked up before it posts another message. Similarly, if the mailbox is empty, the reading task must get an error code so that it can go to sleep to await the receipt of a message. The mailbox can thus synchronize communication between asynchronous tasks.

Intel's iRMX extends the notion of the mailbox by incorporating three queues: a message queue, a writing-task queue, and a reading-task queue. Of course, the task-waiting queues can be either FIFO queues or prioritized queues.

Simple descriptions of how real-time operating systems' primitives work do not do justice to them. To use these primitives (such as mutual-exclusion mechanisms), a software engineer must adopt a mindset

entirely different from the one he uses for sequential programming.

To get an idea of just how different multitasking programming is from sequential programming, consider the four examples discussed in the following section. The examples show the coding of four different schemes for granting reading and writing privileges to a common data area or file. The examples are taken from Andyne Computing Ltd's PCMascot manual, which provides many more such examples. PCMascot is an implementation for the IBM PC of the Mascot real-time operating system (Ref 5).

One peculiarity of Mascot needs to be explained before you can understand the examples: Mascot combines the notion of a mutual-exclusion queue with that of a mailbox. A task can join a queue. The operating system will suspend the task until it reaches the head of the queue. Once at the head of the queue, the task awakens and owns the queue until it explicitly leaves the queue (even the task's going to sleep does not release the queue).

While it's in possession of the head of a queue, and only in that state, a task can wait on the queue. That is, the task suspends itself and will awaken only when another task stimulates the queue. Obviously, no other task can take possession of the head of the queue until the waiting task is awakened and decides to leave the queue.

To flesh out these examples with another real-time operating system, you would have to coordinate a semaphore and a mailbox. That is, a task would first have to request a semaphore. When it acquires the semaphore, it then must request a read from a mailbox—and perhaps wait for a message to be deposited in the mailbox. After a successful read, the task finally surrenders the semaphore.

The problem these examples solve is the general "readers and writers" problem. The solutions must satisfy two conditions: Any number of readers can simultaneously access the data, but any writer must have exclusive access to the data (there can be only one writer at a time). That way, readers need not be concerned that the data will mysteriously change as they are reading it (remember, each task in a multitasking system is under the delusion that it alone is running).

The four strategies for establishing precedence are:

- Taking readers and writers in strict order of arrival. Once a writer is writing, all readers and writers are excluded; a batch of consecutive read-



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Instrumentation

Using mutual-exclusion mechanisms requires a software engineer to adopt a mindset entirely different from the one he uses for sequential programming.

```

control queues:  mutex
                 read_count_cq

ida layout:     read_count
                 data_record

start_read ()
{
    JOIN mutex
    JOIN read_count_cq
    read_count++
    LEAVE read_count_cq
    LEAVE mutex
}

end_read ()
{
    JOIN read_count_cq
    read_count--
    If (read_count == 0)
    {
        STIM mutex
    }
    LEAVE read_count_cq
}

start_write ()
{
    JOIN mutex
    while (read_count > 0)
    {
        WAIT mutex
    }
}

end_write ()
{
    LEAVE mutex
}

```

Fig 1—These entry and exit routines accommodate readers and writers in strict sequence of arrival. Tasks gain entry to reading and writing routines (not shown here) by joining mutual-exclusion queues. Tasks sort out precedence, here and in Figs 2, 3, and 4 by keeping count of readers and writers and posting messages (STIM) to tasks waiting on queues.

ers has unrestricted access until the next writer arrives.

- Giving readers precedence over writers. Waiting readers have access before waiting writers do.
- Giving writers precedence over readers. Waiting writers have access before waiting readers do.
- Dividing readers into two classes: high-priority readers that have precedence over writers, and low-priority readers, over which writers have precedence.

The Mascot queues, by their nature, give requesting tasks strict FIFO access. Some other real-time operating systems, such as Intel's iRMX, would give you the option of prioritizing their semaphore and mailbox queues.

The examples in Figs 1 through 4 consist of two pairs of simple routines that reading and writing tasks must call before and after doing a read or write. The examples are written in a C-like pseudocode and are

stripped of many implementation details. The actual data manipulation in the shared-data area is application dependent and is not germane to these examples. Each of the examples begins with a declaration of mutual-exclusion control queues. Note that the "ida" (intercommunication data area) declaration in the program header is simply a declaration of the data constructs and variables that are local to these functions.

The routines in Fig 1 fulfill the first strategy and accommodate readers and writers in the strict sequence of arrival. To understand the action of the two pairs of procedures in Fig 1, assume that no read or write requests are under way and that the first request is a read request. *Starread* increments *reacount* by one and allows the reader to proceed. All subsequent read requests, up to the first write request, will have the same effect. Now suppose that a write request occurs while a number of readers are currently reading. When the writer reaches the head of the *mutex* mutual-exclusion queue, it will block all further readers from initiating reads.

The writing task in possession of the *mutex* queue then goes to sleep to wait for the last reader to call *enread*. The last reader's calling *enread* will decrement *reacount* to zero and use the STIM system call to send a message to the writing task, which has been waiting for just such a message (remember, the queue functions as a mailbox for the task at the head of the queue). The writing task then updates the common data area and finally exits through *enwrite*, releasing the *mutex* mutual-exclusion queue, and allowing other readers and writers their turn to proceed.

Fig 2 is the same two pairs of read- and write-access-control routines modified to allow readers precedence over writers. When you compare Fig 2 with Fig 1, you'll note that the listing in Fig 2 has an additional control queue, *writcq*, in which tasks waiting to write must queue up. Note the cause and effect here: Giving readers precedence over writers means that writers, not readers, must queue up.

Starread is exactly the same in Fig 2 as it is in Fig 1. *Enread* is almost identical—the only change is that the routine must now stimulate *writcq* when *reacount* becomes zero instead of *mutex*. The *starwrite* procedure is quite different because a writing task must first join the queue of waiting writers.

After reaching the head of the queue of writers, it must then wait until no more readers are reading. This situation is an example of a case in which you must exercise extreme care when setting up mutual-exclu-

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You must use precision when applying protection mechanisms to asynchronous tasks.

```

control queues: mutex
                read_count_cq
                write_cq

ida layout:     read_count
                data_record

start_read ()
{
    JOIN mutex
    JOIN read_count_cq
    read_count++
    LEAVE read_count_cq
    LEAVE mutex
}

end_read ()
{
    JOIN read_count_cq
    read_count--
    If (read_count == 0)
    {
        STIM write_cq
    }
    LEAVE read_count_cq
}

start_write ()
{
    JOIN write_cq
    JOIN mutex
    while (read_count > 0)
    {
        LEAVE mutex
        WAIT write_cq
        JOIN mutex
    }
}

end_write ()
{
    LEAVE mutex
    LEAVE write_cq
}

```

Fig 2—Somewhat similarly to those of Fig 1, these read- and write-access-control routines allow readers precedence over writers.

sion mechanisms. The writing task that has reached the head of the writers' queue, and is checking to see whether any active readers are left, must first gain control of the mutual-exclusion queue *mutex* before checking the *reacount* variable. If the writing task weren't preventing reading tasks from initiating a read during the interval in which the writing task was checking for readers, a reading task could overtake the writing task.

Now you have the explanation for the clumsy-looking series of LEAVE and JOIN function calls that bracket the writing task's WAIT function call (the task is waiting for a message from the last exiting reading task). The writing task must gain control of the mutual-exclusion queue *mutex* to check on readers, but must leave it so that readers can continue to read the resource as long as they wish—thus fulfilling the second scheme's requirements.

```

control queues: mutex
                read_cq
                read_count_cq
                write_count_cq

ida layout:     read_count
                write_count
                data_record

start_read ()
{
    JOIN read_cq
    JOIN mutex
    while (write_count > 0)
    {
        LEAVE mutex
        WAIT read_cq
        JOIN mutex
    }
    JOIN read_count_cq
    read_count++
    LEAVE read_count_cq
    LEAVE mutex
    LEAVE read_cq
}

end_read ()
{
    JOIN read_count_cq
    read_count--
    If (read_count == 0)
    {
        STIM mutex
    }
    LEAVE read_count_cq
}

start_write ()
{
    JOIN write_count_cq
    write_count++
    LEAVE write_count_cq
    JOIN mutex
    while (read_count > 0)
    {
        WAIT mutex
    }
}

end_write ()
{
    JOIN write_count_cq
    write_count--
    If (write_count == 0)
    {
        STIM read_cq
    }
    LEAVE write_count_cq
    LEAVE mutex
}

```

Fig 3—These routines give writers precedence over readers.

The third example, in Fig 3, gives writers precedence over readers. As in Fig 2's listing, in Fig 3 a control queue for tasks waiting to read, *readcq*, replaces the previous queue for tasks waiting to write. Also new to this schema is a counter (*writcount*) for the number of writers waiting to write, and a mutual-exclusion queue (*writcountcq*) to protect it.

In a fashion similar to the writing routine of Fig 2's example, a reader first joins the read queue *readcq* and then, after reaching the head of the queue, waits for a message from the final writer that all writers are



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Once they're written, all real-time systems require extensive debugging and fine-tuning.

```

control queues: mutex
                read_cq
                read_count_cq
                write_cq
                write_count_cq

ida layout:     read_count
                write_count
                data_record

start_hp_read ()
{
    JOIN mutex
    JOIN read_count_cq
    read_count++
    LEAVE read_count_cq
    LEAVE mutex
}

end_hp_read ()
{
    JOIN read_count_cq
    read_count--
    if (read_count == 0)
    {
        STIM write_cq
    }
    LEAVE read_count_cq
}

start_write ()
{
    JOIN write_count_cq
    write_count++
    LEAVE write_count_cq
    JOIN write_cq
    JOIN mutex
    while (read_count > 0)
    {
        LEAVE mutex
        WAIT write_cq
        JOIN mutex
    }
}

end_write ()

{
    JOIN write_count_cq
    write_count--
    if (write_count == 0)
    {
        STIM read_cq
    }
    LEAVE write_count_cq
    LEAVE mutex
    LEAVE write_cq
}

start_lp_read ()
{
    JOIN read_cq
    JOIN mutex
    while (write_count > 0)
    {
        LEAVE mutex
        WAIT read_cq
        JOIN mutex
    }
    JOIN read_count_cq
    read_count++
    LEAVE read_count_cq
    LEAVE mutex
    LEAVE read_cq
}

end_lp_read ()
{
    JOIN read_count_cq
    read_count--
    if (read_count == 0)
    {
        STIM write_cq
    }
    LEAVE read_count_cq
}

```

Fig 4—Using all the techniques developed in Figs 1, 2, and 3, these routines allow for two classes of readers: a high-priority class that takes precedence over readers and a low-priority class that doesn't.

finished. Note the similar sequence of getting and releasing the mutual-exclusion queue *mutex* while checking the variable *writcount*. *Writcount* is another classic example of a critical region that needs protection.

The read task still has more to do before it actually reads. It must get to the head of the queue that protects the variable holding the count of readers, and it must increment the count. The reader must lock out other tasks from the *reacount* variable because writing tasks use *reacount* for decision making—another critical region.

Reading tasks exit through *enread*. If a reading task is the last one to exit, it sends a message (via the *STIM* function call) to any waiting writing task. Writing tasks simply work their way to the head of the writing-task queue and increment the count of the number of writers kept in *writcount*. They then work their way to the head of the mutual-exclusion queue. Once at the head of the mutual-exclusion queue, they automatically block

any more read tasks from starting a read operation. When all the readers who were currently reading eventually finish, the writer gets a message posted at *mutex* by the last exiting reading task, and it begins writing. When exiting, the last writing task posts a message to the reading task (if one exists) that has been waiting for its turn.

The handshaking between reading and writing tasks is very subtle in this example. Readers can't proceed until all the writers are finished, and once one or more readers gets control of the common data area, writers must wait. Note the structure of the exclusion mechanisms that accomplish this handshaking. One mechanism, *mutex*, protects reads of two resources: *writcount* (by the reading task) and *reacount* (by the writing task). Yet reading and writing tasks have separate exclusion mechanisms, *reacountcq* and *writcountcq*, to protect writes to these same two resources (*reacount* and *writcount*). This example incisively illustrates the precision with which you must apply protection mecha-

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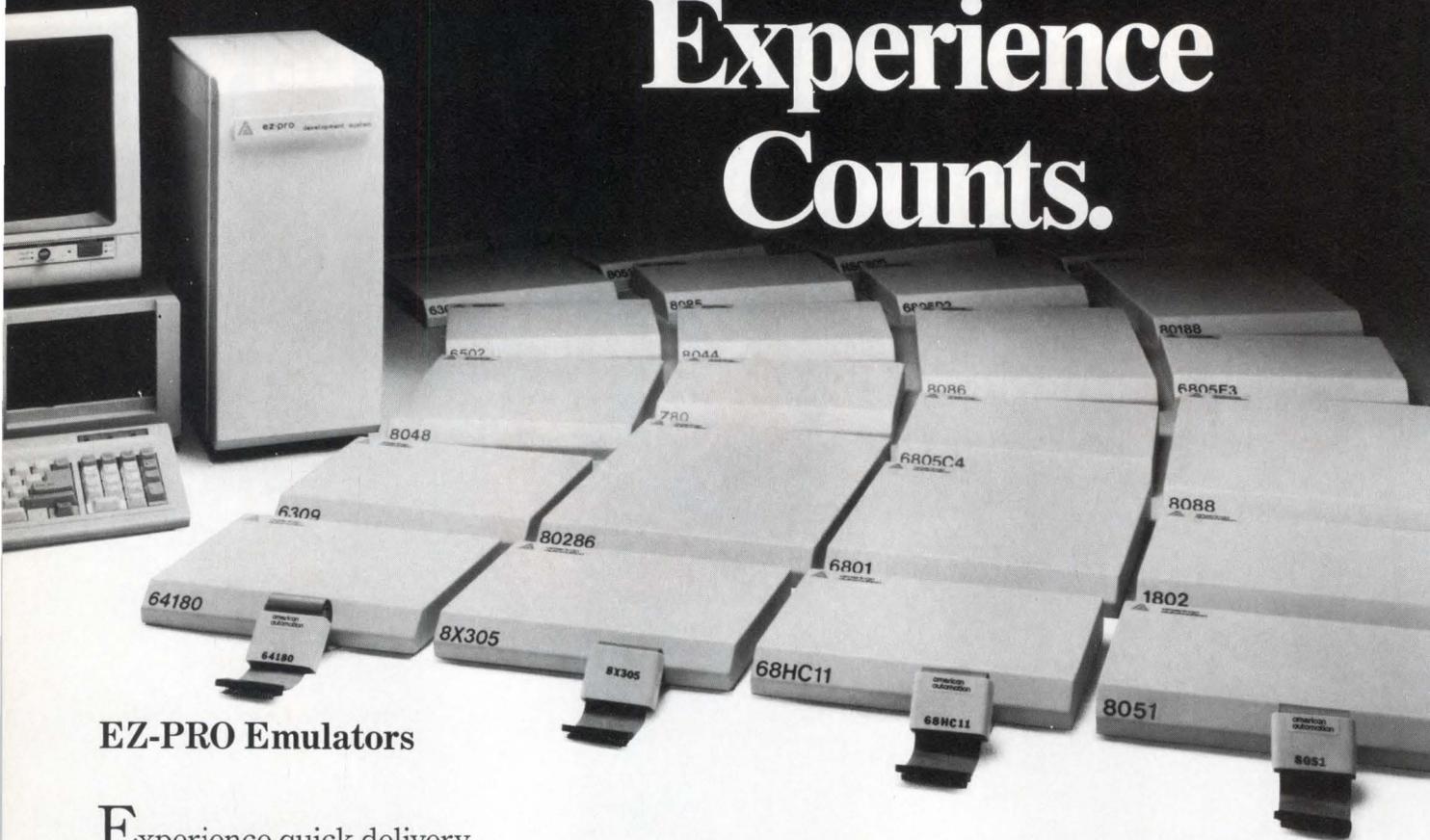
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Most real-time-software engineers pepper their code with extra routines that record information about a routine as it executes.

nisms when dealing with asynchronous tasks.

The last example, **Fig 4**, allows for two classes of readers, high-priority readers (*starhread*) and low-priority readers (*starhread*). High-priority readers zip through their entry routine, pausing only long enough to increment the count of readers. In a similar fashion, the last exiting reader kicks off any waiting writing task by sending a message, via the *STIM* function call, to the *writcq* queue (which, as before, serves as first a queue and then a mailbox).

Writing tasks, in the course of writing, block any low-priority reading tasks, which must wait until all writers finish. Note, however, that even low-priority readers, once they get going, increment the *reacount* variable, just as high-priority readers do; they thus block any subsequent writers until all readers finish. By now, you should realize that to write routines such as these, you need a solid design and a thorough understanding of real-time-programming intricacies.

Once they're written, all real-time systems require

extensive debugging and fine-tuning. At present, no completely integrated hardware-and-software debugging tools are available (**Ref 6**). You can obtain hardware and software tools separately, of course. High-level-language debuggers are available in several forms, and you can get real-time-OS debuggers. You can also find logic analyzers, in-circuit emulators, and software-performance analyzers (**Ref 7**), which can identify software bugs that baffle software-based tools. But you can't obtain a single integrated package that can simultaneously control a high-level language debugger, an operating-system debugger, and hardware-based tools.

Consequently, most real-time-software engineers will probably fall back on tried-and-true techniques of "instrumenting" their code. That is, they will pepper the code with extra routines that record pertinent information about a routine as it executes. The classic example of this technique of instrumenting a program with additional statements is the practice of debugging

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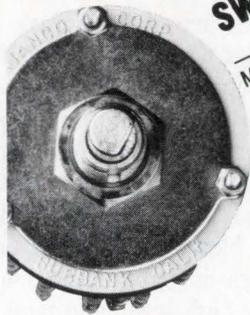
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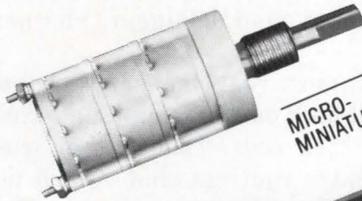
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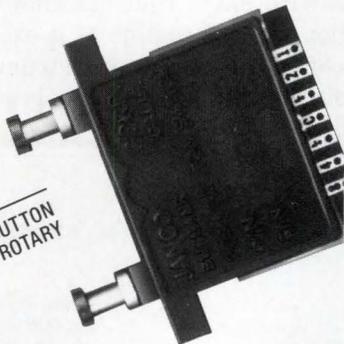


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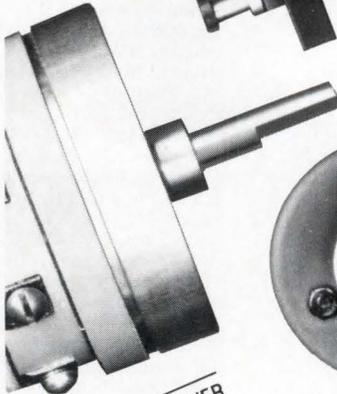
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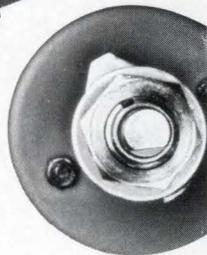
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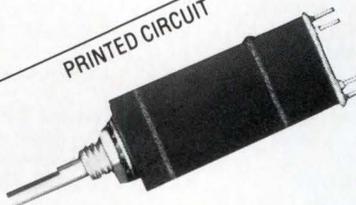
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a Basic program by inserting extra Print statements throughout the program.

To instrument their code, real-time-software engineers would probably do something that's better suited to real-time systems. For example, they might equip each task with routines that record the system clock's value in a debugging array at critical points in each routine's execution—routine entry and exit points, for example. Such extra code obviously distorts the real-time performance of the system, but it provides a quick way of identifying routines that are hogging the CPU.

EDN

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PART NO.	ORG.	PROCESS	SAMPLES	PROD.	SPEED SORTS AVAILABLE (ns)	PRG OPTIONS & COMMENTS
DYNAMIC RAMS						
TMM41256AP/AT/AZ	256KX1	NMOS	YES	YES	100 120 150	P,T,Z
TMM41257AP/AT/AZ	256KX1	NMOS	YES	YES	100 120 150	P,T,Z
TMM41464AP/AT/AZ	64KX4	NMOS	YES	YES	100 120 150	P,T,Z
TC511000P/J/Z	1MbX1	CMOS	YES	YES	85 100 120	P,J,Z
TC511001P/J/Z	1MbX1	CMOS	YES	YES	85 100 120	P,J,Z
TC511002P/J/Z	1MbX1	CMOS	YES	YES	85 100 120	P,J,Z
TC514256P/J/Z	256KX4	CMOS	YES	YES	85 100 120	P,J,Z
TC514258P/J/Z	256KX4	CMOS	YES	YES	85 100 120	P,J,Z
THM81000S/L	1MbX8	CMOS	YES	YES	85 100 120	S,L
THM91000S/L	1MbX9	CMOS	YES	YES	85 100 120	S,L
STATIC RAMS						
TMM2016BP	2KX8	NMOS	YES	YES	90 100 120 150	P24, 600 mil DIP
TMM2015BP	2KX8	NMOS	YES	YES	90 100 120 150 200	P24, 300 mil DIP
TC551718CPL	2KX8	CMOS	YES	YES	150 200	P24, 6T Cell Ultra Low Power
TC551718CFL	2KX8	CMOS	YES	YES	150 200	F24, 6T Cell Ultra Low Power
TMM2064P	8KX8	NMOS	YES	YES	70 100 120 150	P28, 600 mil DIP
TMM2064AP	8KX8	NMOS	1287	0388	70 100 120	P28, 600 mil DIP
TMM2063P	8KX8	NMOS	YES	YES	70 100 120 150 200	P28, 300 mil DIP
TMM2063AP	8KX8	NMOS	1287	0388	70 100 120	P28, 300 mil DIP
TC5565APL	8KX8	CMOS	YES	YES	100 120 150	P28, 4T Cell Low Power
TC5565AFL	8KX8	CMOS	YES	YES	100 120 150	P28, 4T Cell Low Power
TC5563APL	8KX8	CMOS	YES	YES	100 120 150	P28, 300 mil DIP/4T Cell
TC5564APL	8KX8	CMOS	YES	YES	150 200	P28, 6T Cell Ultra Low Power
TC5564AFL	8KX8	CMOS	YES	YES	150 200	P28, 6T Cell Ultra Low Power
TC55257PL	32KX8	CMOS	YES	YES	85 100 120	P28, 4T Cell Low Power
TC55257APL	32KX8	CMOS	YES	YES	85 100 120	P28, 4T Cell Low Power
TC55257AFL	32KX8	CMOS	YES	YES	85 100 120	P28, 4T Cell Low Power
TC551832PL	32KX8	CMOS	YES	YES	85 100 120	P28, Pseudo Static
TC551832SPL	32KX8	CMOS	1187	YES	85 100 120	P28, 300 MI DIP
TC551832FL	32KX8	CMOS	YES	YES	85 100 120	P28, Flat Pack
TC5518128P	128KX8	CMOS	YES	0188	100 120	P32, Pseudo Static
TC5518128F	128KX8	CMOS	YES	0188	160 190	P32, Virtually Static
HIGH SPEED STATIC RAMS						
TMM2018AP	2KX8	NMOS	YES	YES	25 35 45	P24
TMM2068AP	4KX4	NMOS	YES	YES	25 35 45	P20
TMM2088P	8KX8	NMOS	YES	YES	35 45 55	P28
TMM2089C	8KX9	NMOS	YES	YES	35 45 55	C28
TMM2089P	8KX9	NMOS	YES	YES	35 45 55	P28
TC5561P	64KX1	CMOS	YES	YES	1 * 70	P22, 4T Cell Low Power
TC5561J	64KX1	CMOS	YES	0188	1 * 70	J24, 4T Cell Low Power
TC5562P	64KX1	CMOS	YES	YES	35 45 55	P22, 4T Cell Low Power
TC5562J	64KX1	CMOS	YES	YES	35 45 55	J24, 4T Cell Low Power
TC55416P	16KX4	CMOS	YES	YES	25 35 45	P22
TC55416J	16KX4	CMOS	YES	YES	25 35 45	J24
TC55417P	16KX4	CMOS	YES	YES	25 35 45	P24, OE
TC55417J	16KX4	CMOS	YES	YES	25 35 45	J24, OE
EPROMS						
TMM2764AD-	8KX8	NMOS	YES	YES	150 200	D
TMM2764AD-	8KX8	NMOS	YES	YES	150 200	D
TMM27128AD-	16KX8	NMOS	YES	YES	150 200	D
TMM27128AD-	16KX8	NMOS	YES	YES	150 200	D
TMM27256AD-	32KX8	NMOS	YES	YES	150 200	D
TMM27256AD-	32KX8	NMOS	YES	YES	150 200	D
TC55256AD	32KX8	CMOS	YES	YES	150 200	D
TMM27512D-	64KX8	NMOS	YES	YES	200 250	D
TMM27512D-	64KX8	NMOS	YES	YES	200 250	D
TC557100D	128KX8	CMOS	YES	YES	200 250	D
TC557101D	128KX8	CMOS	YES	YES	200 250	D
ONE TIME PROGRAMMABLES						
TMM24128AP	16KX8	NMOS	YES	YES	200	PF
TMM24128AP	16KX8	NMOS	YES	YES	200	PF
TMM24256AP	32KX8	NMOS	YES	YES	200	PF
TC54256AP	32KX8	CMOS	YES	YES	200	PF
TMM24512P	64KX8	NMOS	YES	YES	250	PF
MASK ROMS						
TC55257P	32KX8	CMOS	YES	YES	200	F, P28
TC551000P	128KX8	CMOS	YES	YES	200	F, P28
TC552000P	256KX8	CMOS	YES	YES	200	P32
P = PLASTIC C = CERAMIC F = FLAT PACK D = CERDIP Y = DIE T = PLCC J = SOJ L = LEADED MODULE Z = ZIP -- = ±10% Vcc AVAILABLE S = SOCKET MODULE * = SELECTABLE SPEED SORT AVAILABLE † = IN DEVELOPMENT						

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WATTS	SINGLE	MULTI UP TO 5 OUTPUTS
1600		■
1500	■	■
1000	■	■
800	■	■
750	■	■
500	■	■

1600w 1500w 1000w 800w 750w 500w 400w 300w 220w 175w 135w 70w 40w 15w

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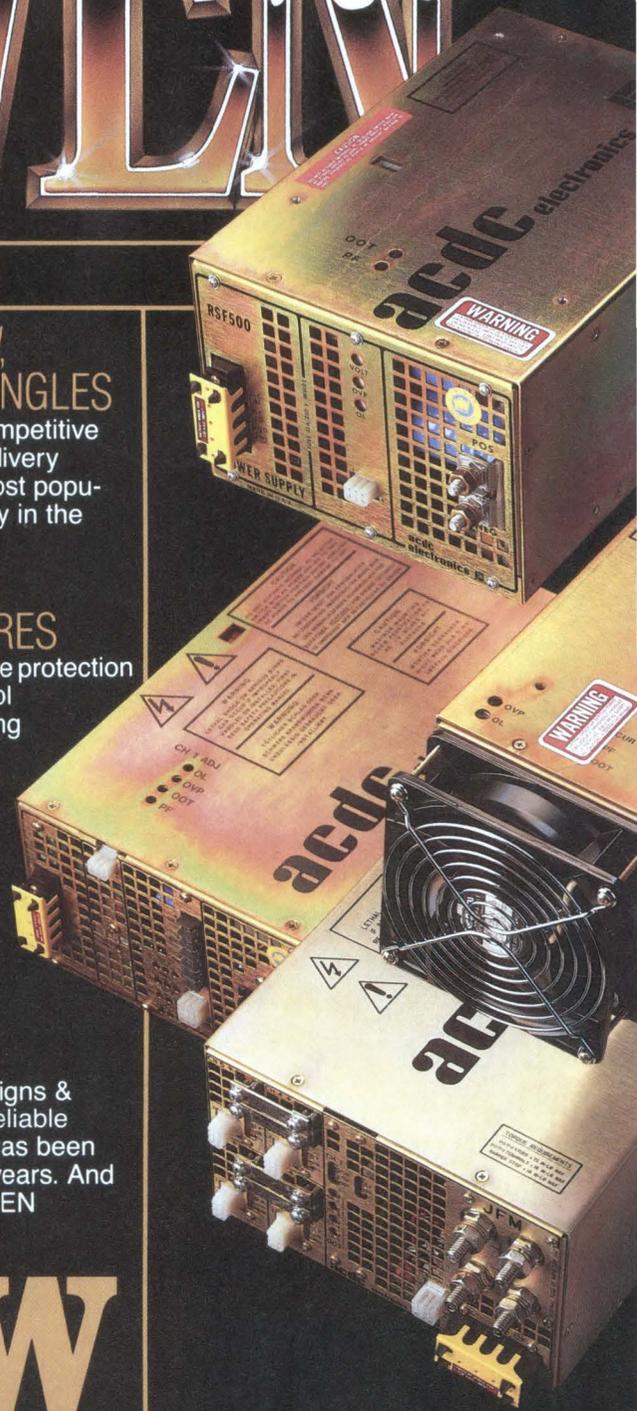
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Len Sherman, *Maxim Integrated Products*

Designers of dc/dc-conversion products are now addressing the special requirements of low- and medium-power applications. As a result, you can apply switching techniques' advantages in battery-powered portable equipment, telemetry devices, and consumer products.

A key requirement for designers of battery-powered products is that they minimize the number of cells used in the product. Substituting, for example, two large cells for a stack of six or seven smaller ones yields not only reductions in size and weight but also increased reliability and energy density. An efficient, low-power step-up voltage converter used in conjunction with a few high-capacity, low-voltage cells makes such a trade feasible, especially in an application where a stack of expensive rechargeable batteries would be the alternative.

The circuits shown in Figs 1 through 7 are all

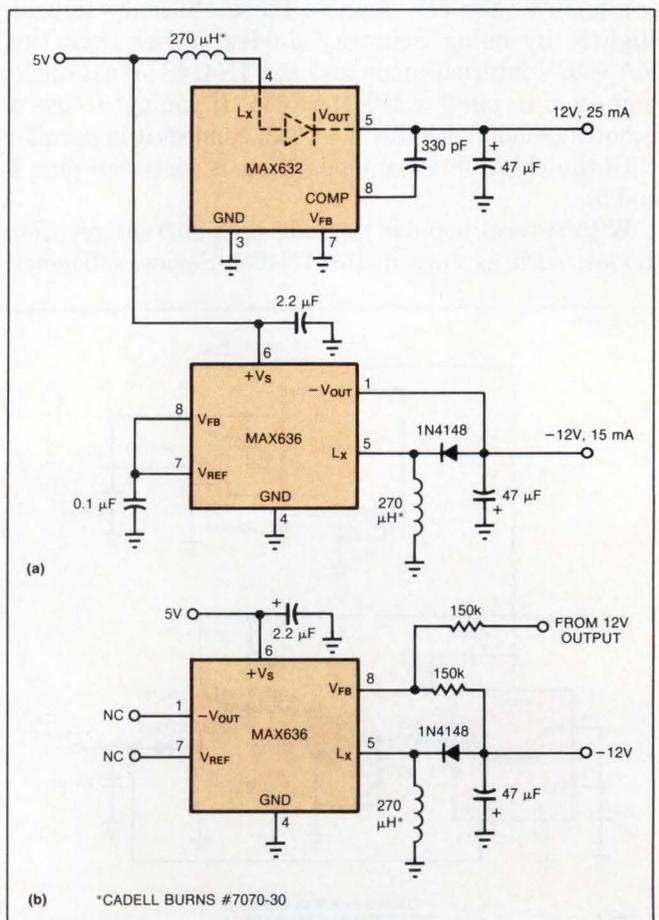


Fig 1—You can tailor this $\pm 12V$ supply to provide either independently regulated outputs (a) or a tracking negative output (b). The inductors don't exact too great a size penalty: Each measures only 0.6 in. long by 0.26 in. in diameter.

The flyback configuration keeps circuitry compact, and it adapts not only to voltage boosting but to buck and buck/boost configurations as well.

flyback-type switching dc/dc converters (the same type that generates 10- to 20-kV supplies for television, video display terminals, and oscilloscopes) that operate at 50 kHz (see **box**, "Flyback converters' internal operation"). The flyback configuration keeps the circuitry compact, and its versatility allows it to accomplish more than simple voltage boosting.

Derive $\pm 12V$ from digital system's supply

Often, a digital system powered by a 5V supply includes a few analog functions that require $\pm 12V$. The circuit shown in **Fig 1** uses two dedicated 8-pin converters—the MAX632 and MAX636—to derive 25 mA at 12V and 15 mA at $-12V$ from a 5V logic supply. You can configure the circuit for independently regulated outputs (**Fig 1a**) or for tracking regulation (**b**).

The positive converter's efficiency is 85%; the inverter's is 75%. You can improve these efficiency figures slightly by using Schottky diodes rather than the MAX632's internal diode and the 1N4148 signal diode connected to pin 5 of the MAX636. If you opt to use a Schottky diode with the MAX632, connect it in parallel with the chip's internal diode (that is, between pins 4 and 5).

With several popular types of high-current rectifier diodes, such as ones in the 1N4000 Series, efficiency

and overall performance are poor for high-frequency (greater than 10 kHz) dc/dc conversion. Many of these diodes were designed to pass high current only at 120 Hz; therefore, they waste energy at 50-kHz operating frequencies. In addition, these slow rectifiers might also allow the inductor's discharge voltage to reach excessive levels before the rectifier turns on and directs current to the load.

Small-signal diodes, such as the 1N4148, are fast enough and work well in applications that require less than 50 mA. High-speed rectifiers, such as the 1N4935, are suitable in applications that require as much as 1A. Schottky diodes provide the best performance with respect to speed and forward voltage drop, and they can significantly improve efficiency in low-voltage, high-current applications. However, you'll have to decide on the basis of your individual application whether their higher cost and relatively low reverse breakdown voltage eliminate the Schottky diodes from consideration.

External MOSFET increases power

If your application requires higher power than **Fig 1's** circuit provides (if, for instance, you need the power for a data-acquisition board or a high-level industrial controller), then you can modify the circuit by adding an

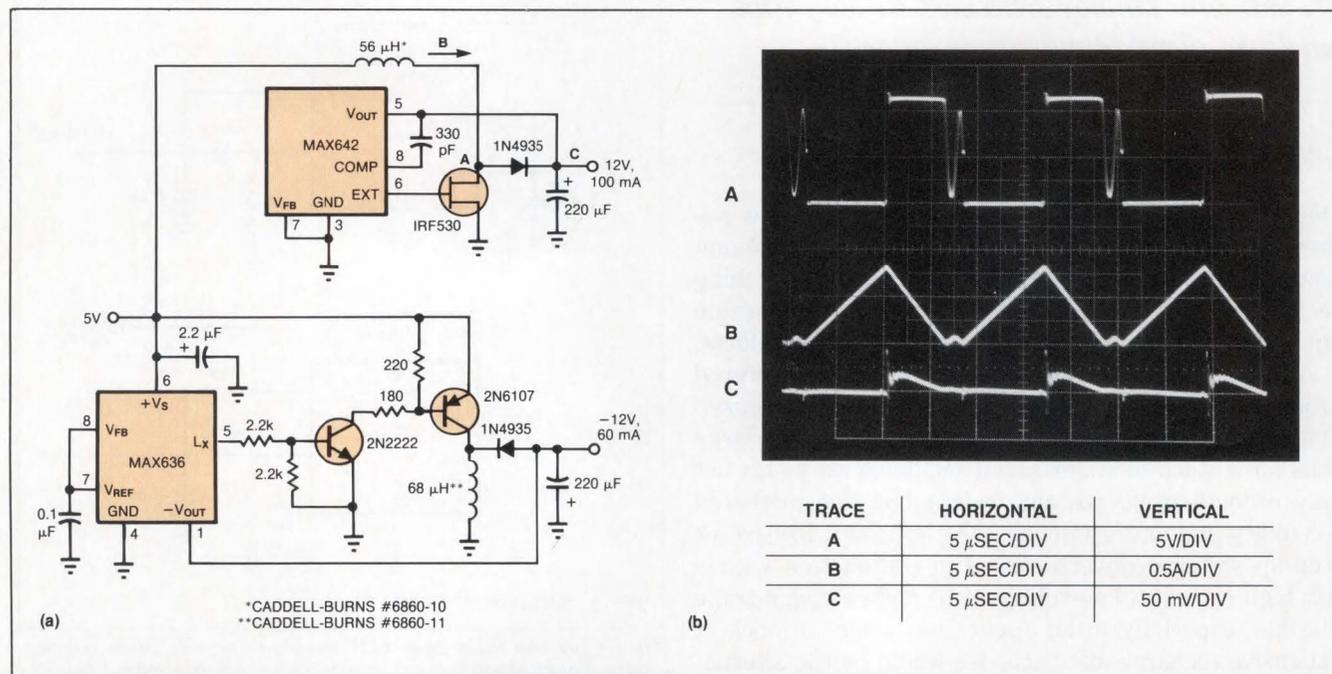


Fig 2—With the addition of a few external components (a), the circuit of **Fig 1** can supply currents of 100 mA at 12V and 60 mA at $-12V$. Traces A, B, and C (b) represent the switch voltage, inductor current, and output ripple for the 12V supply.

external power MOSFET, as shown in Fig 2a, and obtain 100 mA at 12V and 60 mA at -12V. The power MOSFET drops the 12V converter's efficiency to 80%, but driving the power MOSFET doesn't require any additional parts.

The scope photo (Fig 2b) shows some of the key waveforms in the step-up circuit. Trace A is the voltage waveform at the drain of the IRF530 MOSFET (under full load), trace B is the inductor current, and trace C is the ripple voltage at the 12V output. The ringing found on trace A near the end of each discharge cycle is normal and is due to the inductor's interaction with stray capacitance when the inductor current decays to nearly zero. As you can see from trace C, this ringing has no effect on the output waveform.

Compensate for IR drops

Not only might you need to derive $\pm 12V$ from a 5V supply, you might also need to derive a regulated 5V level from a nominal 5V supply that suffers from an unacceptable voltage drop because of IR effects in long power-distribution cables. You can efficiently boost the voltage back to a regulated 5V by using the circuit shown in Fig 3.

That circuit operates at input voltages as low as 4.5V. The transformer's 3.2:1 turns ratio allows the circuit to supply more than the MAX631's usual output current without requiring external power transistors. This circuit provides as much as 150 mA of output current at 5V. You can wind the transformer on a 14x8-mm pot core, or you can obtain the transformer by ordering the standard part number listed in the schematic.

When the MAX631's L_X switch turns off at each half

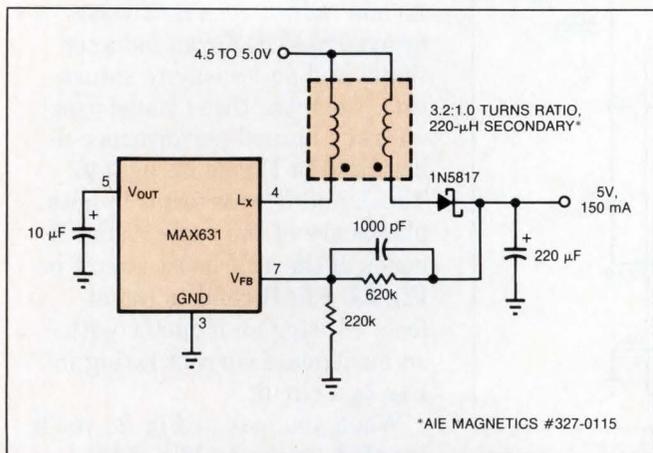


Fig 3—This simple circuit boosts a supply voltage that might have sagged substantially because of IR drops in long cables.

cycle of its 50-kHz clock, the reflected voltage in the transformer's primary generates a 9V supply voltage for the MAX631 at the V_{OUT} pin. Operating the MAX631 at 9V rather than at the 4.5V provided at the input increases the gate-source voltage of the internal MOSFET, consequently reducing the MOSFET's on-resistance. This circuit requires the external feedback resistors at V_{FB} because, unlike the previous circuits, this circuit doesn't allow you to use V_{OUT} as the feedback input for the regulator.

Derive 12V from 8 to 15V input

The simple boost converters of the previous examples are inadequate for some battery-powered applications. For example, the unregulated output of a 12V sealed lead-acid battery varies from worst-case peaks of 15V down to as little as 8V when it is deeply discharged. Therefore, you can't derive a regulated 12V output from a 12V lead-acid battery by using a simple boost converter, such as one of those illustrated in Figs 1 and 2, because a boost converter can't accept an input voltage that is greater than its output voltage. Conversely, a buck converter can't accept an input voltage that's less than its output; therefore, a simple buck converter won't work either. A buck/boost converter, as the name implies, is a combination of buck and boost circuitry that successfully addresses the challenge of

Text continued on pg 150

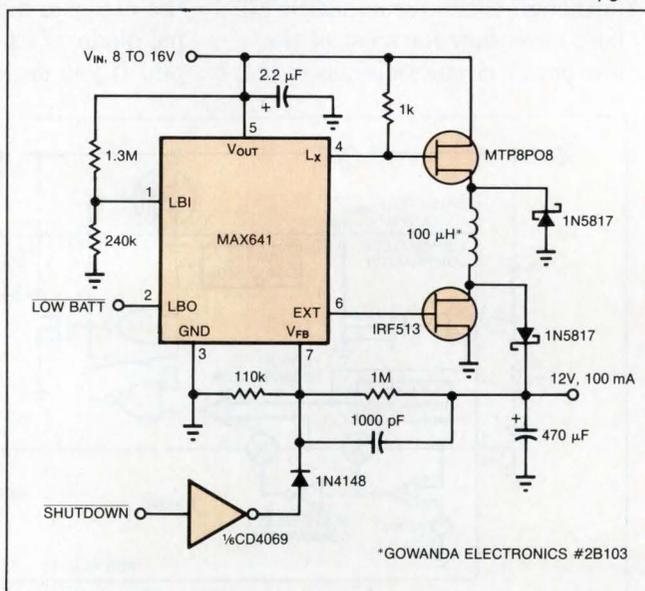


Fig 4—A buck/boost converter can accommodate wide input-voltage swings, such as the 8 to 15V swing typical of a 12V sealed lead-acid battery. The LOW BATT output indicates when input voltage drops below 8V. Pulling SHUTDOWN low turns off the circuit.

Flyback converters' internal operation

In a flyback converter, voltage applied to an inductor or transformer primary via a switch causes inductor current to rise for a fixed period of time. When the voltage is switched off, the magnetic field stored in the transformer collapses, causing the secondary to supply current to the load. With the MAX640 and MAX630 Series devices, this switching occurs at 50 kHz. You can use these devices to step up the voltage, step it down, or invert it just by changing the configuration of the switch (transistor), coil, and steering diode.

Fig A illustrates the MAX641's internal operation. When the output voltage drops below the preset (or externally set) value, the error comparator switches high and connects the internal oscillator to the L_X and EXT outputs. EXT is typically connected to the gate of an external n-channel power MOSFET (although the external MOSFET isn't necessary for most of the low-power circuits discussed in

the accompanying article). When EXT is activated, the MOSFET turns on and off at the oscillator frequency.

When EXT is high, the MOSFET switches on, and the inductor current increases linearly, storing energy in the coil. When EXT switches the MOSFET off, the coil's magnetic field collapses, and the voltage across the inductor changes polarity. The voltage at the catch diode's anode then rises until the diode is forward-biased, delivering power to the output. As the output voltage reaches the desired level, the error comparator inhibits EXT until the load discharges the output capacitor to a point at which the error comparator connects the oscillator to the L_X , and EXT generates output once again.

The MAX641 doesn't have a V_{IN} pin. Input power to start the dc/dc converter is supplied via the external inductor (and external diode, if used), to the V_{OUT} pin. If you use an external catch

diode, connect its cathode to V_{OUT} . Once the converter is started, it's powered from its own output voltage. This bootstrap design ensures that the external MOSFET has the maximum gate drive and, consequently, the minimum R_{ON} .

One external component that you must select is the inductor. Although the inductance of many types of coils, such as RF chokes and air-core inductors, frequently falls in the appropriate range for dc/dc converters (50 to 500 μH), these inductors typically saturate at only a few milliamps and therefore are not a good choice for your dc/dc-converter design.

A saturated inductor ceases to behave as an inductor. It can no longer store energy in its magnetic field, so the mechanism that normally limits the inductor current no longer operates; all that limits the current is the series resistance. This resistance is quite low; consequently, the current can rise to an excessive, and possibly destructive, level.

The scope photo in Fig B shows the switch voltage (trace A) and inductor-current waveforms (trace B) for an inductor that's well on its way to saturation. Compare these waveforms with the normal performance illustrated in Fig 2b on pg 146. The A and B waveforms in both photos are of the same A and B nodes of the 12V boost circuit in Fig 2a. Fig B reflects the effects of using an inductor with an inadequate current rating in Fig 2a's circuit.

When you look at Fig B, you'll see that, in the middle of the

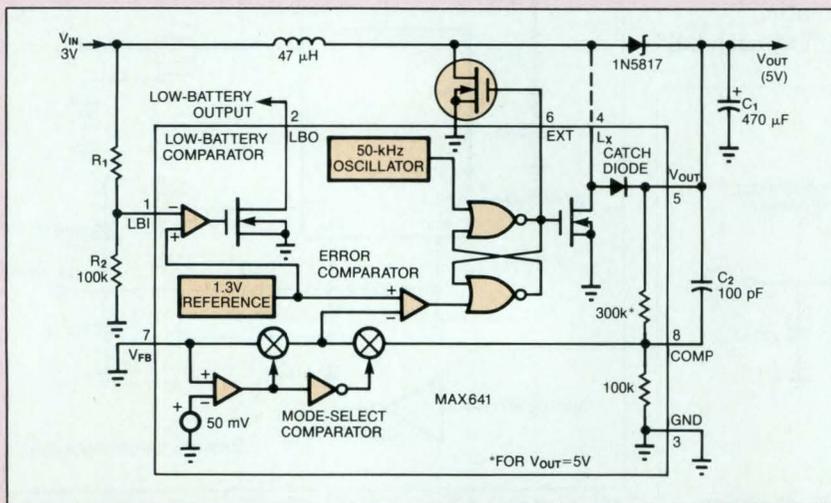


Fig A—This block diagram illustrates the MAX641's operation. For many low-power applications, the external MOSFET and Schottky diode are unnecessary.

charge cycle, above the 0.5A level, the current waveform's slope increases markedly, indicating the onset of saturation. At this point, the effective inductance of the coil decreases because the current through the inductor has risen to the saturation level. The rising edge of the switch-voltage waveform is much slower in **Fig B** than in **Fig 2b** because the inadequately rated inductor takes several microseconds to come out of saturation.

An inductor doesn't saturate as long as its operating current is less than its rated maximum current. At first glance, it would seem easy enough to specify the maximum current rating for your inductor, but what you have to watch out for in your dc/dc designs is that the peak inductor current is often four to six times the converter's average current output. In the case of flyback converters, this peak current flows not just under peak load conditions, but each

time the current switch turns on. For this reason, you must give careful consideration to the current rating of your converter circuit's inductor.

Besides the care required in the selection of inductors, another often-overlooked area of concern in dc/dc-converter design is that encompassed by grounding, shielding, and bypassing. The quality of ground connections is key to the performance of dc/dc converters. Because the peak current in an inductor or switch (transistor) can reach several amps, you must provide these points with very-low-impedance paths to the supply common. For example, in the inverting circuit of **Fig 2a**, the coil current typically exceeds 1A. For best results, use separate paths to ground for the high-current paths so that they are separated from the chip's power and feedback connections. If you don't have the option of separate traces, then use as heavy a sin-

gle trace as you possibly can to carry the high current back to the supply.

Loop instabilities, caused by interactive ground connections or stray capacitive pickup, can also severely limit the performance of an otherwise sound dc/dc-converter design. Some of the symptoms of these problems are high ripple voltages at the output, efficiency that's lower than expected, and "motorboating," or low-frequency oscillation.

Motorboating occurs when the control loop of the dc/dc converter produces pulses in periodic clusters of 10 to 20 pulses rather than at more or less random intervals. Motorboating can be caused by one or more of the following phenomena: stray pickup at the feedback node, unwanted feedback to the reference, and feedback via the ground or power-input pin.

If the cause is stray pickup at the feedback node, add a lead compensation capacitor (100 to 1000 pF) from the feedback terminal or COMP pin to the circuit output or reduce the size of your connections at the feedback input in order to reduce stray capacitance to ground. If unwanted feedback to the reference is the culprit, bypass the reference and power-input pins to ground (using 0.1 to 1.0 μF). If your circuit is suffering from feedback via the ground or power-input pin, bypass the power-supply input (1.0 to 10.0 μF). You should also separate high-ground-current connections from the reference, feedback, chip-ground, and chip-power connections.

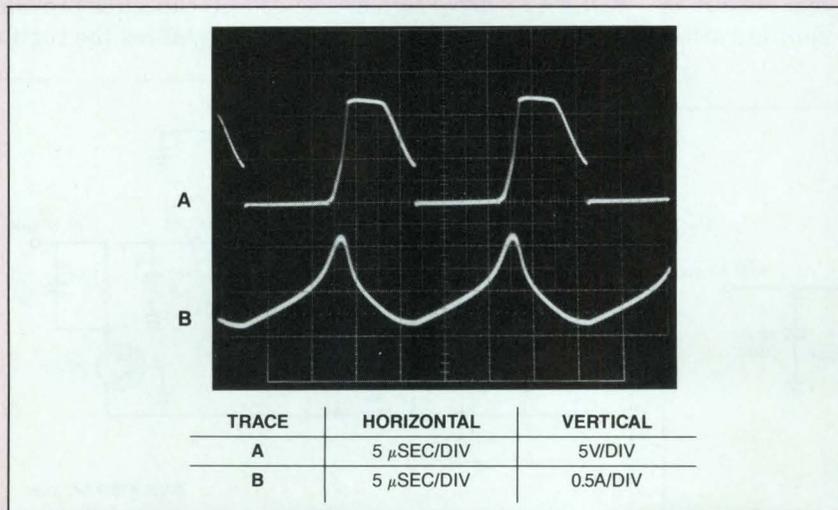


Fig B—The marked increase in the current waveform's slope (trace B) illustrates the onset of saturation for an inductor with an inadequate current rating. Trace A represents switch voltage.

You must sometimes develop 5V from a nominal 5V input that has sagged because of IR drops in long power-distribution lines.

the wide input-voltage swing associated with the sealed lead-acid battery.

The circuit of Fig 4 is a buck/boost converter that provides 100 mA at 12V and accepts 8 to 16V inputs. Both ends of the circuit's inductor are switched by separate power MOSFETs, which the MAX641 drives directly via its L_X and EXT outputs. These outputs operate out of phase, so the p- and n-channel FETs turn on at the same time. When both the n- and p-channel FETs turn off, the two Schottky diodes steer the coil's discharge current to the 12V output. A slight drawback of this circuit is that the converter's efficiency is less than that of a pure buck or boost converter, because the two MOSFETs and two diodes increase losses in the charge and discharge current paths. Nevertheless, the circuit still delivers 100 mA at a respectable 70% efficiency figure.

An additional benefit of this type of circuit is that you can control its operation with a TTL-level signal. Overriding the V_{FB} input with a high-level TTL signal (such as the diode-coupled inverter output in Fig 4) fools the MAX641's internal feedback circuitry into thinking that the output is too high, so the chip turns off both MOSFETs. The circuit's idle current is around 400 μA.

Obtain 50V from a 12V supply

If you need to generate voltages higher than the 5 and 12V levels of the circuits shown in Figs 1 through 4, consider a configuration such as the one shown in Fig 5. It provides a 50V output from a 12V input and is simpler than Fig 4's circuit: Because the output is higher than the input, a simple boost configuration suffices.

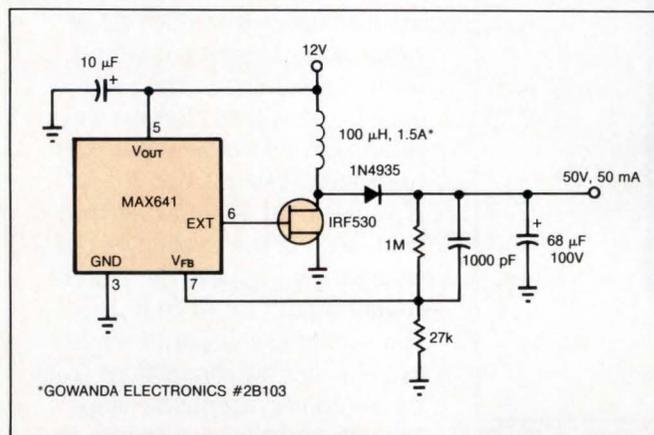


Fig 5—Only the power MOSFET, catch diode, and output-filter capacitor need to withstand high voltages in this 50V supply circuit.

The circuit uses an IRF530 n-channel MOSFET in conjunction with a MAX641 dc/dc controller. In this circuit, the 50V output is not connected directly back to the V_{OUT} pin because that pin has a maximum voltage rating of 18V. The circuit uses an external resistive divider network to provide feedback to the V_{FB} input. The V_{OUT} pin obtains power for the MAX641 directly from the 12V supply. The only components that must withstand high voltages are the MOSFET, the steering diode, and the output filter capacitor: They're rated at 100V, 200V, and 100V, respectively.

A different twist to high-voltage dc/dc conversion is the requirement to power low-voltage logic circuitry from a high-voltage source—for instance, the telephone system's -48V battery voltage. The circuit of Fig 6 uses a basic boost configuration to convert -48V to 5V. A small-signal, high-voltage pnp transistor shifts the feedback signal from the 5V output to the MAX641, whose ground terminal (pin 3) is tied to the -48V input. The output, at 5V with respect to ground, forces about 43 μA through the 100-kΩ sense resistor and the emitter of the 2N5401. This current is sent through the 30-kΩ input resistor at V_{FB}, placing this pin 1.3V above the ground pin (or at -46.7V). Because the internal reference of the MAX641 is a 1.3V bandgap reference, the 1.3V bias level at the feedback input closes the feedback loop.

This biasing scheme allows the EXT output to directly drive the n-channel MOSFET, switching the inductor to the -48V input without level shifting of the MOSFET's drive signal. The 330-pF capacitor provides feedforward compensation, which stabilizes the regula-

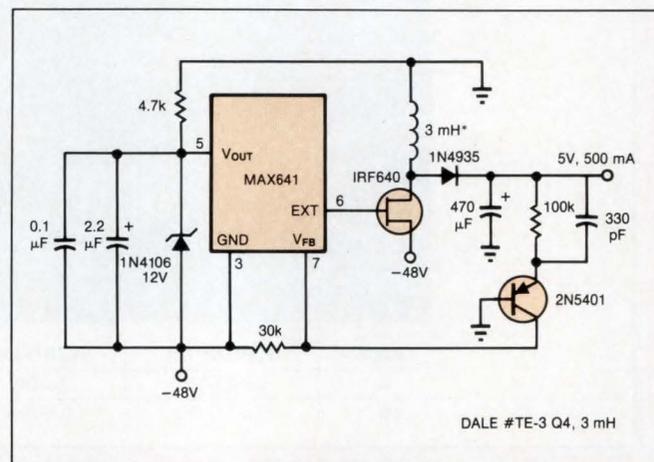
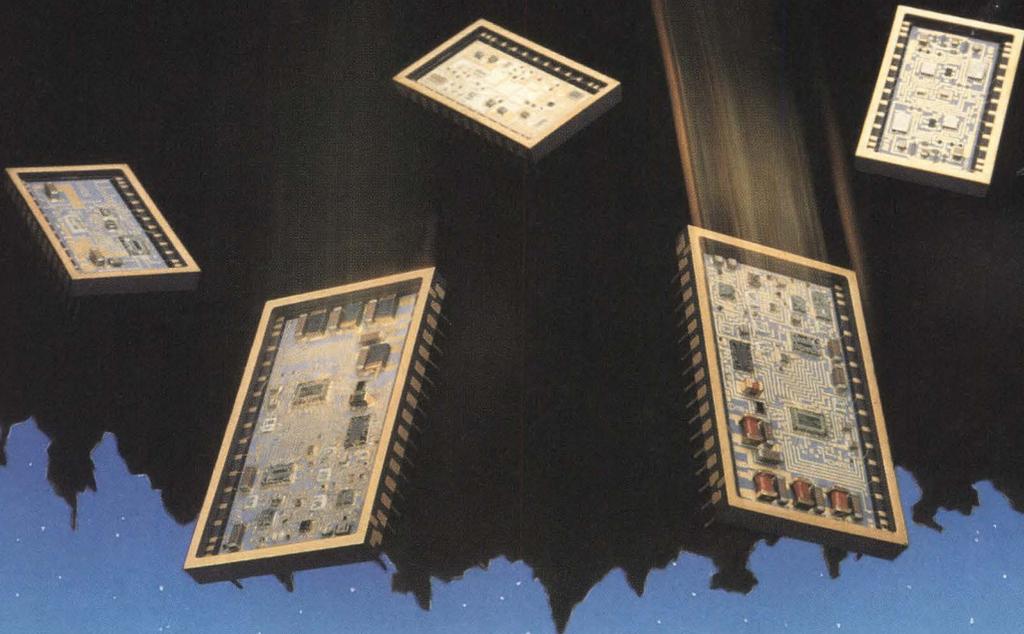


Fig 6—Telecomm applications often require you to develop your logic-level supply from -48V. Suitable for such applications, this circuit delivers 5V at 500 mA.

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A buck/boost converter can deal with the wide input-voltage swings associated with sealed lead-acid batteries.

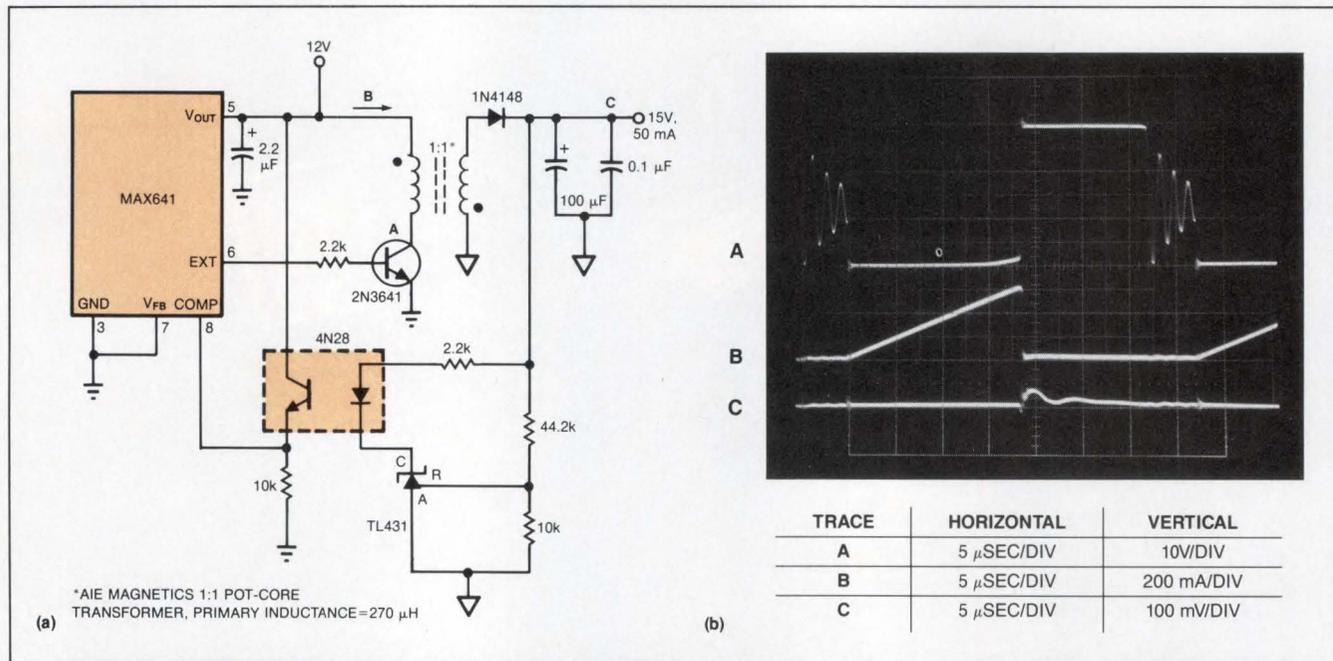


Fig 7—This circuit (a) provides 50 mA at 15V with an isolation rating of 500V—a function of the transformer and opto-isolator. In the scope photo (b), traces A, B, and C represent the switch voltage, primary current, and output-voltage ripple.

tor's control loop and improves the regulator's transient-load response.

Generating an isolated supply

In large analog systems and in industrial-control systems, you must often provide power that is electrically isolated from the main system's power source. This isolation is necessary to prevent ground loops, to protect measurement hardware from dangerous voltages, and to reject common-mode signals. The circuit in Fig 7a generates a regulated 15V, 50-mA output that is fully isolated from the 12V input supply. The circuit's output power is supplied by a 14×8-mm pot-core transformer, and the feedback signal returns to the unisolated side of the circuit via an opto-isolator.

Although the peak primary current of the transformer is within the ratings of the MAX641 converter IC's internal switch, you must use an external transistor to drive the transformer. The reason you need this external transistor is that when the transistor turns off, the 15V secondary voltage is reflected to the primary, placing 30V across the transistor. This 30V exceeds the MAX641's 18V rating. The transformer primary's voltage, current, and ripple voltage are illustrated in traces A, B, and C, respectively, of the Fig 7b scope photo.

To transmit the feedback signal across the isolation barrier, the 15V output is divided and compared with

the 2.75V reference of a TL431 shunt regulator. When the voltage at the TL431's reference input exceeds 2.75V, the TL431 draws current through the opto-isolator's photodiode. The opto-isolator's transistor then pulls the COMP input of the MAX641 high, turning off the EXT output. The COMP input connects to the MAX641's internal voltage divider, and thus the opto-isolator's transistor can control the MAX641. The components specified in Fig 7a provide an isolation rating of 500V.

EDN

Author's biography

Leonard H Sherman is a senior member of the technical staff at Maxim Integrated Products in Sunnyvale, CA. Leonard received his BSEE from MIT, and he has one patent to his credit. Leonard enjoys playing volleyball and collecting old hi-fi equipment in his spare time.



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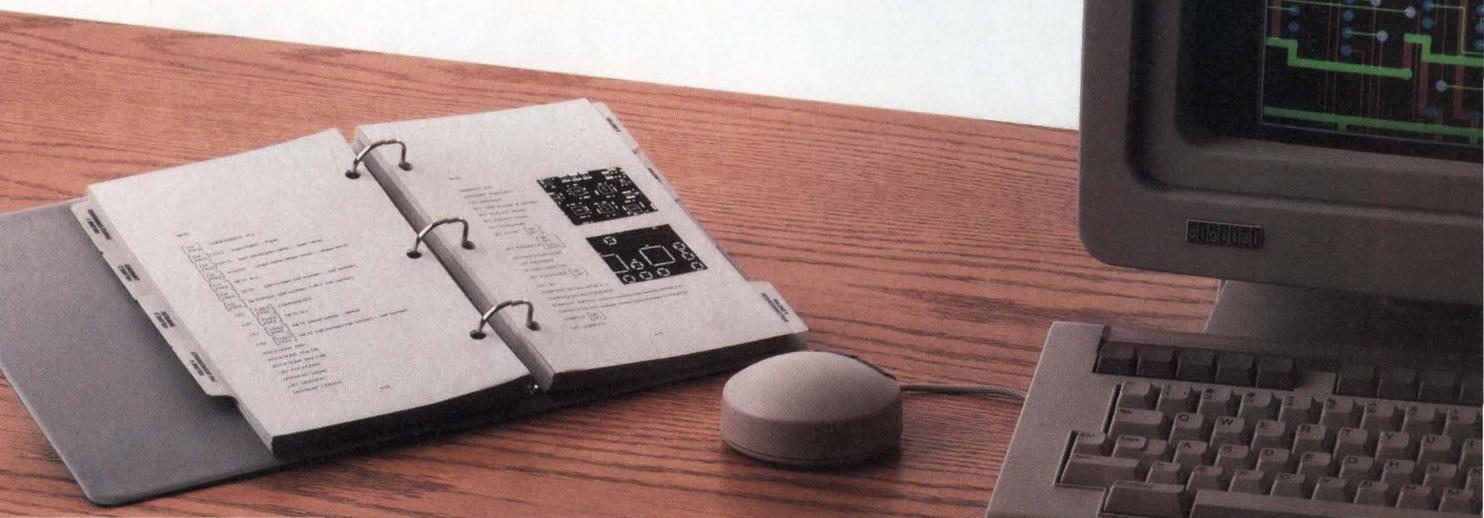
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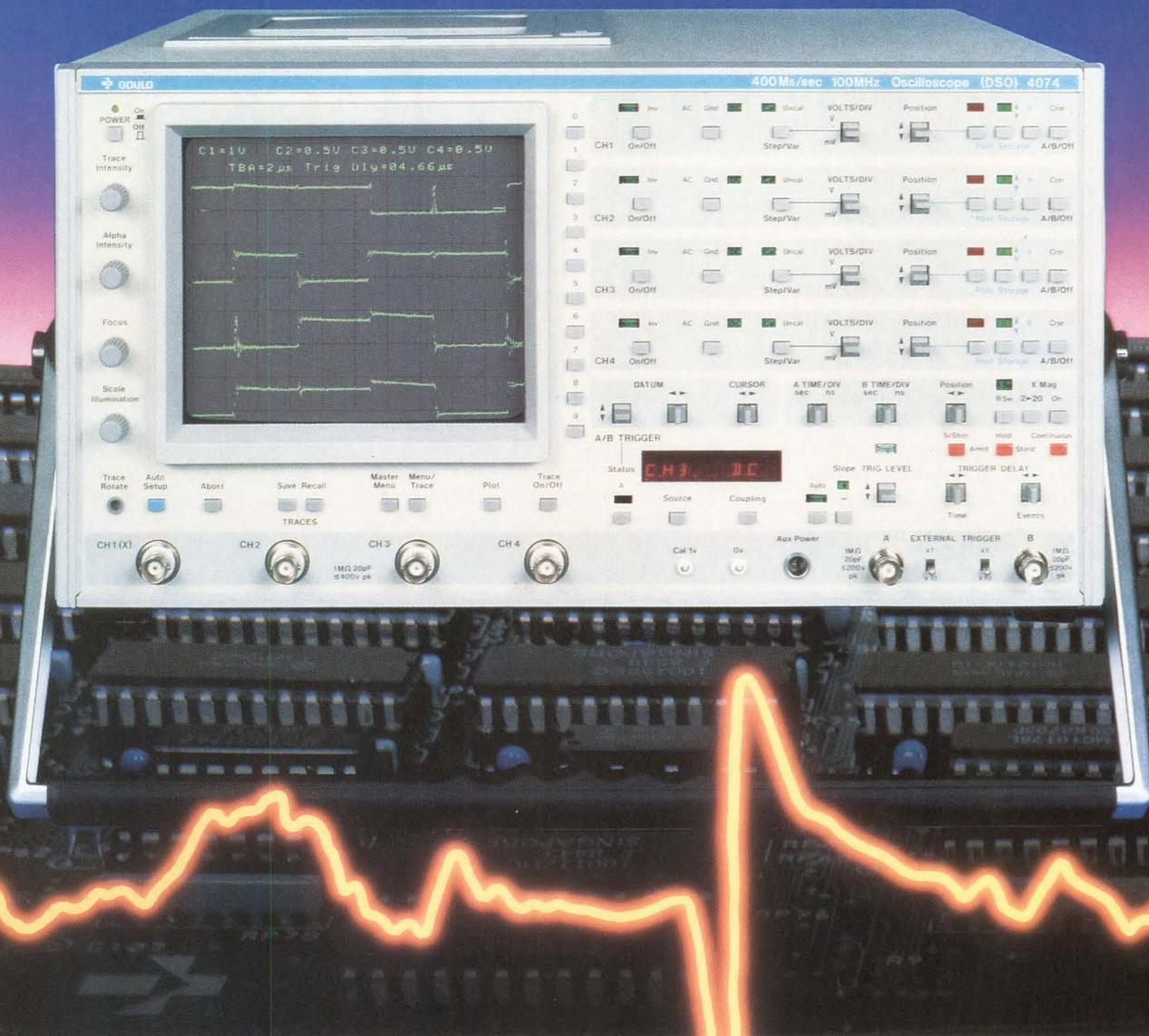


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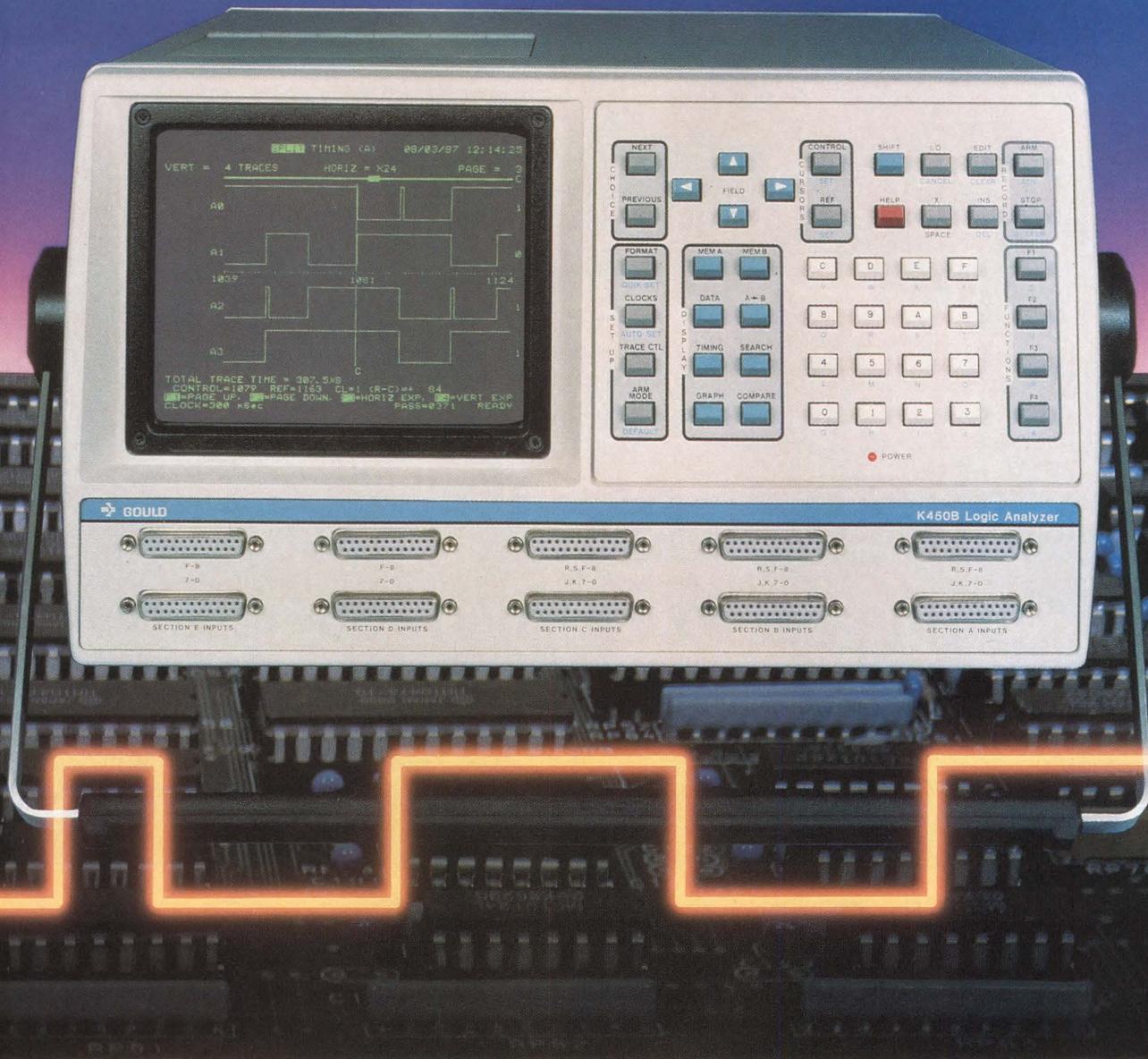




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Proper glitch capture requires knowledge of logic-analyzer limits

Using a logic analyzer to locate the source of intermittent malfunctions in digital systems can prove to be extremely frustrating. If you understand your analyzer's capabilities and limitations, though, you raise the odds of having the instrument furnish the information you need.

Wolfgang Schweitzer, *Kontron Messtechnik*

Logic analyzers are useful tools for tracking down the cause of intermittent malfunctions in digital systems. But because logic analyzers are sampled-data systems—that is, they acquire information only at discrete points in time—the information they yield can be misleading if more than one logic transition occurs between consecutive sample times.

Analyzer manufacturers have devised glitch-capture circuits that allow the instruments to indicate such transitions. Glitch capture is not infallible, however, and you should not assume that its use guarantees that you will find the transient pulse you are looking for. Moreover, logic analyzers vary in speed and in the way they capture, store, and present glitch information; some logic analyzers, in particular the very fastest, do not include special glitch-capture circuits. Therefore, if you want to use an analyzer to best advantage, you must understand how it operates, and, sometimes, how

to employ additional instruments, such as an oscilloscope, in conjunction with it.

Use internal clock for best resolution

Most modern logic analyzers can operate either as logic-state analyzers or as timing analyzers. When a logic analyzer performs timing analysis, it can use an internal sample clock and thus operate asynchronously from the system under test (SUT). An analyzer can also use a clock derived from the SUT and thereby operate synchronously with that system. In state-analysis mode, a logic analyzer always operates synchronously. Because an analyzer's internal clock should be able to run at a maximum rate that's considerably higher than that of the fastest clock in the SUT, using the internal clock yields the instrument's best timing resolution.

When you use a logic analyzer to investigate glitches, you will almost invariably use it as a timing analyzer; state analysis isn't intended for glitch capture, and if you try to capture glitches with a logic analyzer in state-analysis mode, you will discover some significant shortcomings.

For example, consider the use of a logic analyzer in its state-analysis mode to monitor a μ P-based system's state at the end of each instruction cycle. If each instruction cycle requires many clock cycles, then legitimate state transitions during each clock cycle can fulfill the glitch criterion, resulting in an inappropriate glitch indication from the logic analyzer.

Some logic analyzers allow you to operate a portion of their channels in state-analysis mode while you use the remaining channels for timing analysis. Sometimes,

If you try to capture glitches with a logic analyzer in state-analysis mode, you will discover some significant shortcomings.

augmenting a timing display with a state display can help you to determine if a glitch is the probable source of a system malfunction.

At first, glitch capture might seem unnecessary because if you don't use it and you make the sampling interval shorter than the narrowest glitch the SUT can produce, you can guarantee that you will catch all glitches. (The narrowest glitch is approximately equal to the propagation delay (t_{PD}) of the logic family used in the system under test.) However, with this scheme, a glitch is likely to look like a legitimate logic state on the analyzer's display.

Furthermore, because few systems operate at clock rates approaching the reciprocal of t_{PD} , attempting to set the logic analyzer's clock rate to greater than $1/t_{PD}$ is likely to require you to use a very-high-speed (and thus very expensive) analyzer, one that costs considerably more than an analyzer whose sampling rate you chose on the basis of the clock rate of the SUT. Another problem is that setting an analyzer's internal clock to a high rate to capture glitches limits the number of SUT states the instrument's memory can store.

Glitch-capture circuits arose as an alternative to the use of high-speed analyzers to detect glitches in low-speed systems. However, such circuits can't capture all glitches. Moreover, even though your analyzer might tell you that a glitch has occurred during a particular sampling interval, it cannot tell you the duration of the glitch, its amplitude, its shape, or its precise timing within the interval. That missing information may be exactly what you need to isolate the cause of the anomaly.

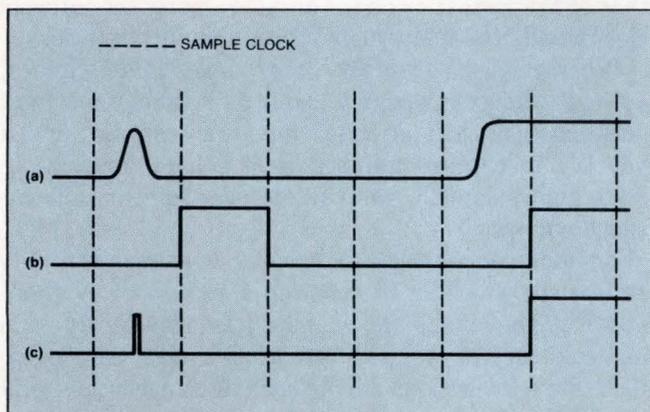


Fig 1—When a glitch occurs in the middle of a sample period (a), a latch-mode display (b) depicts it as a normal logic state existing for the entire subsequent sample interval. The second-order glitch-capture circuit and associated display (c) provide a more nearly accurate picture.

In addition to the effect of the sampling interval, several other factors influence a logic analyzer's glitch-capture capabilities:

- The ability of the analyzer's probes and front-end circuits to pass narrow glitches to the glitch detectors
- The response time and recovery time of the detectors
- The criteria the analyzer uses to recognize a glitch
- The amount of memory required to store glitch information and whether the analyzer sacrifices channel capacity or memory depth to obtain it
- Acquisition-speed limitations imposed by the speed with which the logic analyzer can write glitch information to its memory
- The format used to depict glitches on the display.

Bad timing can fool glitch detectors

In some analyzers, the glitch-capture circuitry for each channel consists of a simple latch that is set *the first time* the associated input signal changes state within a given sample interval. This scheme, however, exhibits two problems: First, two or more transitions through the analyzer's threshold should be required to cause the analyzer to record a glitch, but only a single transition is needed to set the latch. Second, an analyzer using a simple latch displays the glitch in a sampling interval subsequent to the one in which it was detected. (Some logic analyzers make it appear as though a glitch state exists for the *entire* interval following the one in which the glitch occurred.)

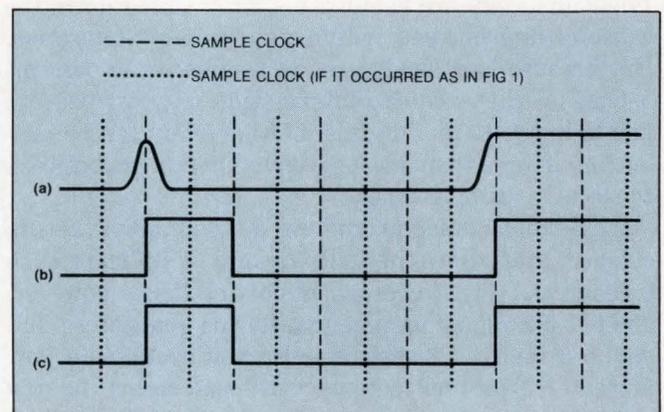


Fig 2—If sampling occurs at the same time as a glitch (a), the latch-mode display (b) looks just like the one resulting from sampling before the glitch. With second-order glitch capture, the display (c) looks the same as that caused by a normal state having a single-sampling-interval duration.

Some older logic analyzers—units with so-called latch-mode display—exhibit both of these glitch-capture and display defects. For the cases shown in **Fig 1b** and **Fig 2b**, such instruments produce similar displays. For the case shown in **Fig 3**, the glitch has the same polarity as the logic state at the next sample, and the latch-mode analyzer's display (**Fig 3b**) gives no indication of the glitch. **Fig 4** shows the same signal as that in **Fig 3** sampled at slightly different points. (Because sampling is asynchronous with the signal, the exact location of the sampling points is random.) In **Fig 4b**, normal sampling occurs in the middle of the positive glitch, but the latch detects what appears to it as a negative glitch. Therefore, the latch causes the analyzer to display a logical-0-state glitch. Although the glitch *does* show up, the display doesn't indicate whether a positive glitch preceded a normal 0-to-1 transition or a negative glitch followed such a transition.

Glitches can masquerade as normal states

Although they do not depict glitches as logic states lasting a full sample interval, many analyzers that incorporate second-order glitch capture still provide a potentially misleading display. For example, when such analyzers find a glitch, they display a narrow pulse in the middle of the sample interval during which they detected the anomaly. The pulse displayed has a state opposite that found on the data line at the sample time preceding the glitch.

Figs 1c, 2c, 3c, and 4c show examples of second-order glitch displays. Note that in **Fig 2c**, because normal sampling happened to take place at the same time as the glitch, the analyzer displays the glitch as a normal logical 1 with a duration of one sample interval.

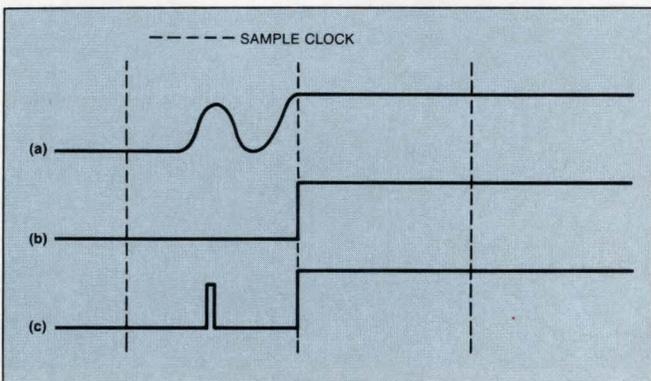


Fig 3—If the logic state at normal sample time is the same as that of a preceding glitch (a), the latch-mode display (b) completely fails to show the glitch. The second-order glitch display (c) does indicate the transient.

Fig 2c shows that the second-order display can present some glitches as normal logic states. More often, however, the second-order display implies a particular glitch amplitude, duration, and timing, although neither you nor the analyzer has much basis for drawing conclusions about the precise nature of these glitch parameters. To indicate the indeterminate nature of a signal during sampling intervals in which glitches are detected, some analyzers display glitches as shaded signals.

The situations illustrated in **Fig 3b** and **Fig 4b** (where the analyzer sometimes catches a glitch and sometimes misses it) or by **Fig 1c** and **Fig 2c** (where the analyzer sometimes displays the glitch as a glitch and sometimes displays it as a normal logic state) demonstrate the need to make repeated measurements when you suspect that your analyzer may be missing glitches or improperly displaying them. If you have a situation in which the glitch always occurs, but the logic analyzer sometimes fails to catch it, or sometimes displays it incorrectly, you ought to be able to find the glitch after a short period of repeating the measurement. If the glitch itself occurs only on rare occasions, you really need to use techniques that will display it correctly every time it occurs. Otherwise, you will probably spend an inordinate amount of time trying to spot it.

Determine what led to the glitch

Some analyzers offer the option of triggering on glitches or of halting data acquisition when they detect a glitch. Because a logic analyzer generates its display from data stored in its memory, a glitch-triggered display can be a very powerful tool for collecting the information you need to determine the cause of and cure

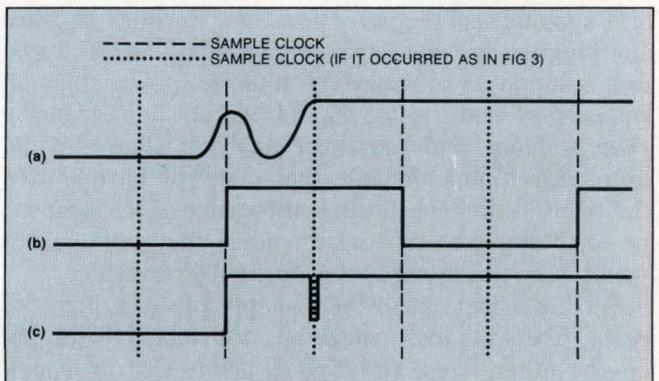


Fig 4—When normal sampling and a positive-polarity glitch occur simultaneously (a), the latch-mode glitch detector can be fooled into detecting a negative-going glitch (b) after the real glitch. The second-order glitch detector (c) provides a fairly accurate representation.

On some logic analyzers' displays, a glitch looks much like a legitimate logic state.

for intermittent malfunctions. Once you have determined approximately when the glitch is likely to occur, glitch triggering allows you to repeatedly run the SUT and halt data acquisition or trigger the logic analyzer so that it displays the sequence of events that preceded the glitch. However, before you rely too heavily on a logic analyzer's glitch-triggering capability, you should understand the circumstances that can cause the instrument to fail to trigger on a glitch.

To be truly useful in your detective work, a logic analyzer's glitch-triggering capabilities should allow you to trigger the analyzer whenever a glitch occurs on any of its inputs (that is, the logical OR of all the unit's glitch detectors). An even better arrangement lets you specify which inputs to include in the glitch-triggering expression. Although glitch triggering doesn't tell you a glitch's amplitude, shape, or precise timing, there's a good chance that the screen display it provides contains the information you need to isolate and correct the problem.

In μ P systems, check interrupt lines

In μ P-based systems and other synchronous logic, many lines are relatively insensitive to glitches; they respond to data only at system-clock edges, and clock edges represent a small percentage of total time. Furthermore, if it's to have an effect on the system, data on these lines usually must be present for tens of nanoseconds. Other lines—interrupt lines are a good example—can respond to signals that appear at any time. Frequently, these lines are sensitive to pulses only a few nanoseconds wide.

Sometimes, if you disable interrupts, you can determine whether a glitch on an interrupt line is the source of a system malfunction. Of course, in order to learn anything useful, you have to understand how the system is supposed to behave with interrupts disabled. If you suspect that a glitch on an interrupt line is causing your problem, and your logic analyzer allows a combined state/timing display, then once you have located the point in time when the troublesome glitch seems to be occurring, you can use the state analyzer to check whether or not interrupts are actually enabled.

Setting a logic analyzer's sample rate too high can cause glitches to masquerade as normal logic states, but on the other hand, insufficient bandwidth in a logic analyzer's glitch-capture circuits can cause the instrument to miss glitches.

Although a logic analyzer is a digital device, its ability to capture glitches depends strongly on circuit

elements that are primarily analog in nature. A logic-analyzer channel's input consists of a probe, a buffer/amplifier, a comparator, a line driver, and a delay line. (The vendor adjusts the delay line to compensate for timing skew between channels.) Together, these elements determine the width of the shortest pulse the analyzer can detect. For glitch capture to be effective, this pulse must be considerably shorter than the sampling interval used; otherwise, the analyzer will be unable to recognize when an input signal makes two or more transitions within a sampling period.

Sometimes, the logic-analyzer manufacturer finds it prohibitively expensive to include circuit elements that permit glitch capture at the logic analyzer's maximum sample rate. You should check your analyzer's specs to find out whether the glitch capture will function at all sample rates; if it doesn't, you should determine the maximum sample rate at which the glitch capture functions or the minimum glitch width that the analyzer's specs say it can detect.

With a little information about your analyzer's glitch-capture circuits, you can make a rough calculation of the probability that the instrument will be able to capture glitches under a particular set of conditions. The results of the calculation may disappoint you. Fig 5 shows the timing considerations involved in the calculation. If the analyzer is to be able to separate a glitch from a normal transition, the glitch must precede the sample time by the glitch-setup time, t_{GS} , plus the data-setup time, t_{SU} .

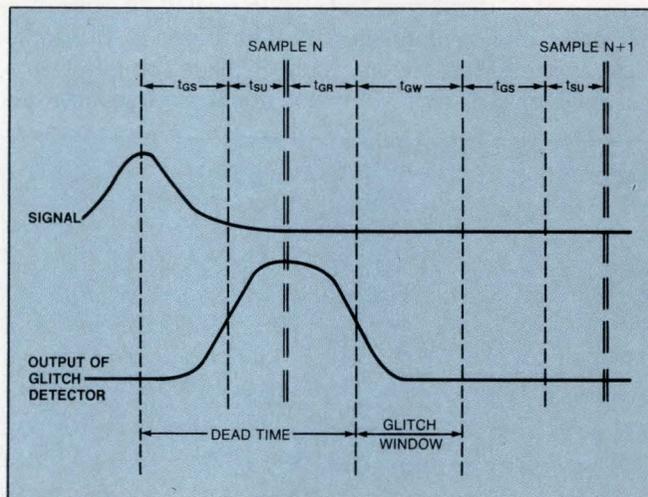


Fig 5—When an analyzer with glitch detection samples at a rate that approaches the reciprocal of the sum of the glitch detector's data-setup, glitch-setup, and glitch-reset times, the fraction of the time that the glitch detector can discriminate between a glitch and a normal logic state becomes very small.

If a glitch arrives soon enough, it will be detected, and the fact that it occurred will be stored in the analyzer's memory. Until it is reset, the glitch detector cannot recognize another glitch.

The glitch detector's reset time is denoted by t_{GR} . If you take the sum $t_{GS} + t_{SU} + t_{GR}$, you have a total dead time during which the glitch detector is unable to detect a glitch. If you now subtract the dead time from the total sample time, you have the glitch window, t_{GW} , the time when the analyzer can recognize glitches. If you then take the ratio of t_{GW}/t_{SAMPLE} , you have the fraction of time during which the analyzer can catch glitches—a rough measure of the likelihood that the analyzer can catch a glitch.

Storing the information that a glitch was detected on an input line in a particular sample interval takes more memory than simply storing the 1 or 0 state of the input. Memory isn't free, of course. So, rather than dedicating memory to storage of glitch data, most logic analyzers with glitch-capture capability allow you to obtain glitch memory from the analyzer's normal data memory.

Some instruments obtain glitch memory by reducing the number of operating channels; others reduce memory depth. When you aren't looking for glitches, you can use all the memory to store normal data. Both methods of obtaining glitch memory are compromises, and neither is perfect. If you reduce the number of channels, you will probably have to rearrange the probes that connect the analyzer to the system under test and stop displaying some channels that have potentially important data. With reduced memory depth, you may not be able to display enough states at once to obtain a good picture of what is going on.

Combine logic analyzer and digital scope

If your logic analyzer has glitch triggering and can trigger another device, then, after you've narrowed down to one or two the number of lines that might be susceptible to a glitch, you may want to examine the suspect lines with a digital storage oscilloscope. The scope, of course, has far fewer channels than the logic analyzer does, but it can display waveforms in detail—something the logic analyzer can't do.

Although the scope's trigger capabilities are less flexible than the logic analyzer's, you can compensate for that shortcoming by using the logic analyzer to trigger the scope. (You will almost certainly need a digital scope: The analyzer may produce its trigger output many sample periods after its input signals

satisfy the trigger conditions, and the scope therefore will have to display data it acquired before it received the trigger. Many digital scopes can provide the necessary signal delay; few, if any, analog ones can.) Although setting up both a scope and a logic analyzer to monitor the system under test may seem like a chore, the combination may reward you with a picture containing more information about the troublesome transient than you could obtain using either instrument alone.

If, at any point in your troubleshooting, you feel frustrated by a seeming lack of progress, a close examination of your system's schematic should be high on your agenda. It is important to understand which lines are likely to be susceptible to glitches, when they are susceptible, and the polarity and duration of glitches that can cause problems. For additional clues about the nature of the problem, you should consult device data books for detailed information about subtle properties of the ICs in your system.

The bottom line is that tracking down glitches isn't simple. You shouldn't assume that a logic analyzer that incorporates glitch-capture capability can always find the glitch you are looking for. If you fail to determine just what the analyzer can and can't do for you, you greatly increase the chances that your troubleshooting task will be tedious and unpleasant. Moreover, if you embark upon the task without a thorough understanding of the operation of your system and the characteristics of the components it uses, you may be setting yourself up for failure.

EDN

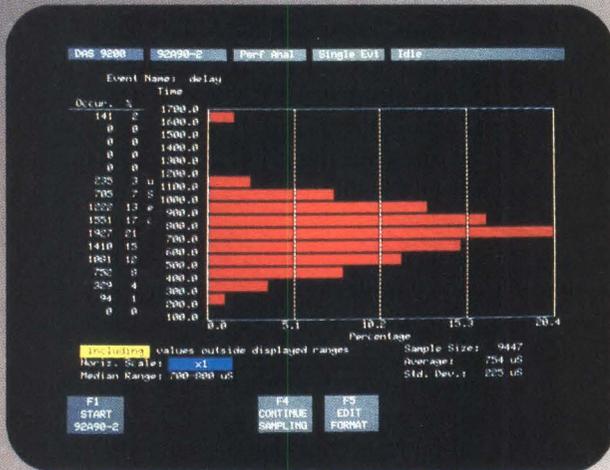
Author's biography

Wolfgang Schweitzer is a sales-support engineer in the international department of Kontron Messtechnik in Echting, West Germany. He is responsible for introduction and promotion of Kontron's line of μP -based instrumentation in northern Europe and Asia. Before he joined Kontron in 1981, he worked with Texas Instruments Germany. He is a member of Greenpeace and enjoys music, travel, skiing, and scuba diving.

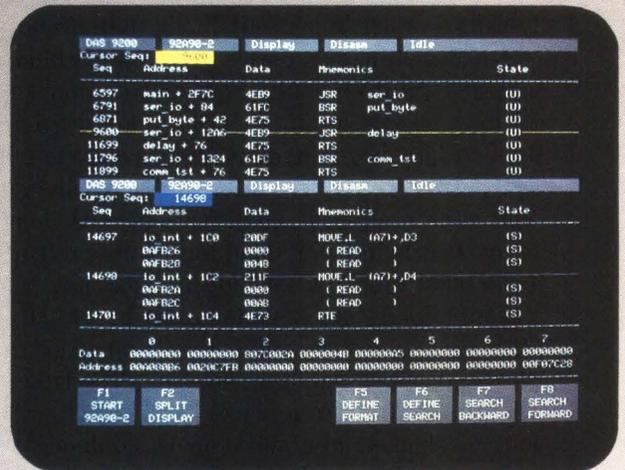


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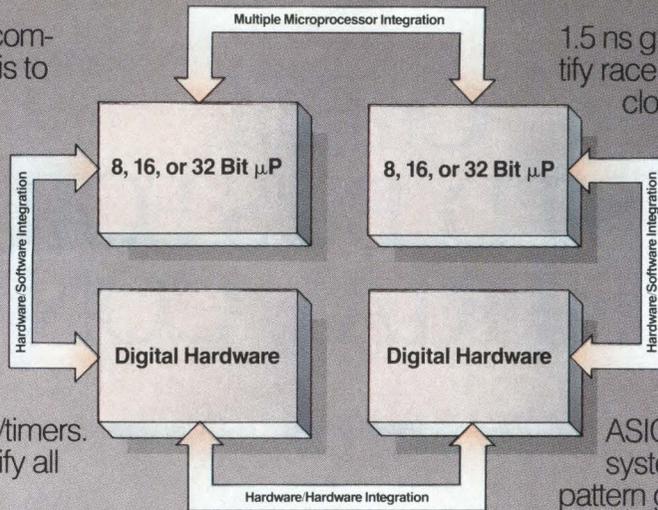
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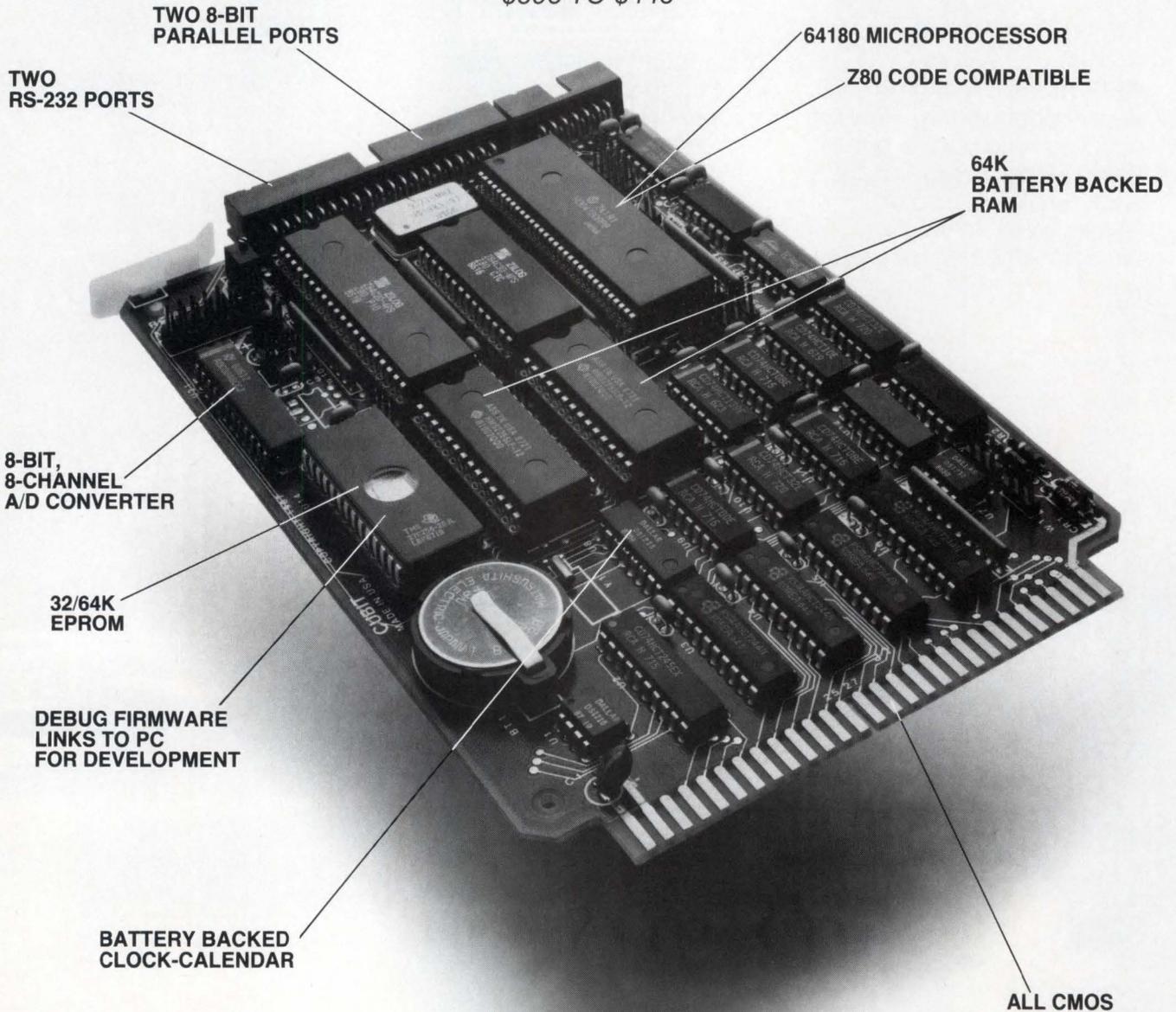


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CIRCLE NO 39

Integrated PLDs support Multibus II bus arbitration

The incorporation of buried state registers in PLDs makes the devices suitable for the design of sequential machines. Such devices thus provide compact packages for containing the bus-arbitration logic in Multibus II systems.

Arthur Khu, *Advanced Micro Devices*

In multiprocessor environments, data transfers occurring over a common bus must be coordinated so that only one peripheral at a time can place data on the bus. Any peripheral that needs to transfer data to another board in the system must request access to the bus, and it must contend for control of the bus with other requesting units. Bus-arbitration schemes determine which requesting unit gains control.

In a synchronous Multibus II system, bus arbitration is decentralized. Requesting boards use a back-off algorithm (see **box**, "Back-off algorithm for Multibus II bus arbitration") to mutually resolve concurrent bus requests, and lower-priority requesters defer to the requesting unit with the highest priority. This scheme makes a dedicated bus-arbiter unit unnecessary, thereby reducing the amount of logic in the Central Services Module (CSM), which every Multibus II system includes.

Because every Multibus II board that's capable of

controlling the bus must contain the same arbitration logic, it behooves the designer to integrate these functions into as few devices as possible to reduce cost and space requirements. Fewer devices also minimize the interconnections between ICs.

The bus-arbitration logic requires four interrelated state machines, which PLDs can readily implement. The AmpAL23S8 is particularly suited for this application because it contains six buried state registers (see **box**, "Compact building blocks for arbitration logic"). Therefore, you can implement all four state machines in one PLD, and you can use the AmpAL23S8 in tandem with an AmpAL22P10, programmed with the back-off algorithm, to contain most of the logic necessary to implement the Multibus II arbitration and transfer protocols.

Bus arbitration in a Multibus II system

In a Multibus II environment, a board that interfaces to the system bus is known as an agent. At system reset, the CSM (which also generates time-out and clock signals) assigns to each agent an arbitration-priority ID. You can set the arbitration priority of the board by reprogramming the ID that the CSM assigns.

Agents use this ID to arbitrate for control of the bus before transferring data. The agents monitor six arbitration signal lines, ARB0(L) through ARB5(L), to mutually determine the highest priority requesting agent to get first access to the bus. Note that the convention for denoting an active-low signal is to use an (L)—eg, ARB0(L).

When the bus-request line BREQ(L) is inactive—set

Multibus II bus-arbitration logic requires four interrelated state machines.

high, denoted by (H)—a requesting agent can drive the bus-request line and put its arbitration ID on the ARB lines. If more than one agent requests access to the bus simultaneously, the lower-priority agents defer to the highest priority agent in the requesting group. After this agent releases the bus, the other agents that generated bus requests concurrently are serviced sequentially, based on their priority. This series of arbitration operations, where bus control is granted sequentially to simultaneous requesters, is called a bus-request sequence.

The requesting group locks out all other bus requests until each agent in the group has gained access to the bus. (Note, however, that an agent assigned a high-priority ID—one that asserts ARB5(L)—can enter and participate in a bus-request sequence simply by putting its ID on the ARB lines, even when the BREQ(L) line is active.) Once the bus-request sequence is complete, the BREQ(L) line becomes inactive, and a new bus-request sequence can begin.

When an agent is contending for the bus, it needs to monitor several system control lines and operations.

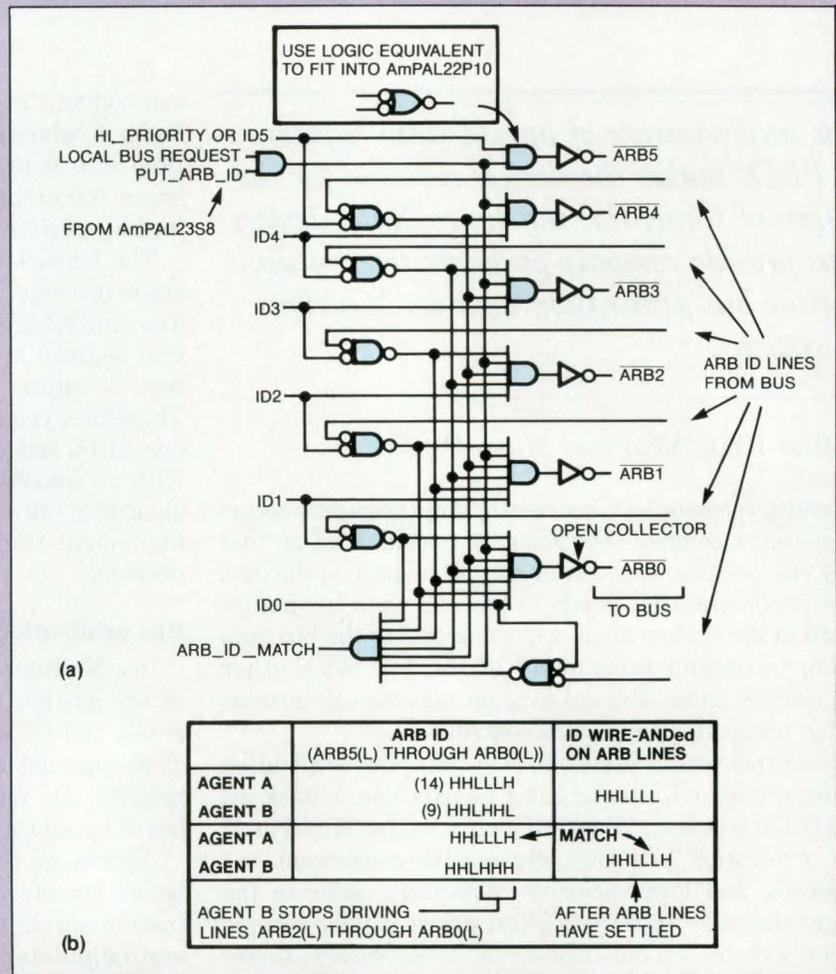
Back-off algorithm for Multibus II bus arbitration

All agents contending for access to Multibus II use the back-off algorithm. When an agent puts its arbitration ID on the bus ARB lines, the ID value is wire-ANDed with the other IDs driven onto the bus. Each contending agent monitors these ARB lines to determine whether it's the highest priority agent.

To make this determination, the contending agent compares each bit of its assigned ID (MSB to LSB) with the wire-ANDed value on the ARB lines. Combinatorial logic circuitry, which is present on each agent, forces the IDs of lower-priority agents to cease driving the ARB lines.

For example, if agent A has an arbitration ID (priority) of 14 and agent B has an ID of 9, then agent B stops driving the ARB2(L) line and all lines below ARB2(L).

The ARB lines are allowed three bus clock cycles to settle before they are used by the arbitration-monitor and -control state machines. An ARB ID MATCH command indicates that an agent has the highest priority and can take control of the bus on an EXCHANGE condition.



The back-off algorithm can be implemented with combinatorial logic circuitry (a). In the example of b, the lower-priority agent B backs off by ceasing to drive ARB lines 0 through 2.

Three state machines perform these monitoring functions:

- A transfer monitor, which tracks all transfer operations taking place on the bus
- An arbitration monitor, which monitors all arbitration operations occurring on the bus
- An arbitration controller, which controls the requesting agent's arbitration operation.

Once an agent becomes the bus owner, a fourth state machine comes into play:

- A transfer supervisor, which supervises the data-transfer operation.

These four state machines are programmed into the AmPAL23S8 and are very closely coupled. Each state machine uses the status of the others to determine its next state.

All agents capable of initiating data transfers use the transfer-monitor state machine to continuously monitor the bus to detect any data transfers taking place (Fig 1)

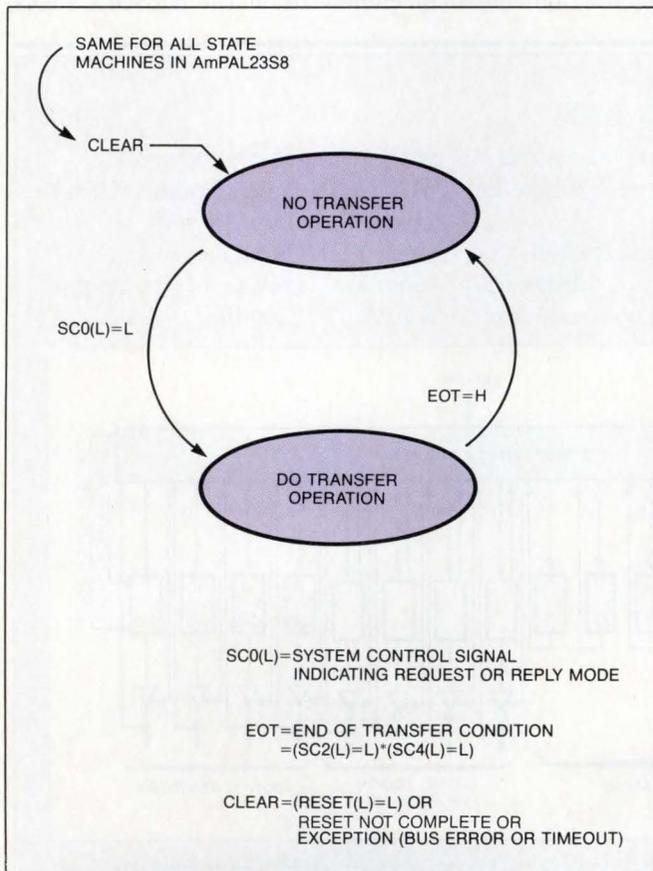


Fig 1—The transfer-monitor state machine monitors all data transfers taking place on the system bus. A transfer operation begins when SC0(L) goes low.

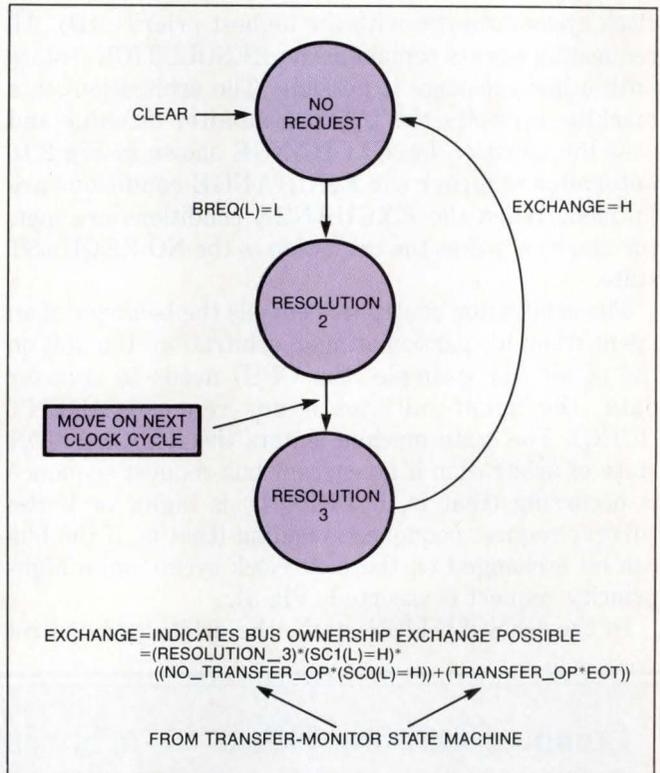


Fig 2—The arbitration-monitor state machine synchronizes the exchange of the bus.

1). Whether or not data transfers are taking place on the bus is a condition that the other three state machines use when contending for control of the bus. The transfer monitor, a 2-state machine, monitors three system control lines called SC0(L), SC2(L), and SC4(L). A transfer operation begins when SC0(L) goes low, causing the machine's transition to the state labeled DO TRANSFER OPERATION. The transfer-monitor machine remains in this state until the last data transfer for the current operation is complete. When SC2(L) and SC4(L) go low, the machine detects an end-of-transfer (EOT) condition and changes to the NO TRANSFER OPERATION state.

Arbitration monitor resolves conflicts

A bus-requesting agent must always monitor any arbitration operations taking place on the bus so that the agent can synchronize the granting and exchanging of bus ownership. To accomplish this function, the arbitration-monitor state machine counts three bus clock cycles after detecting that the BREQ(L) line has gone low (Fig 2). The state labeled RESOLUTION 3 occurs on the third bus clock (the ARB lines have three

If more than one agent requests access to the bus simultaneously, the lower-priority agents defer to the highest priority agent in the requesting group.

clock cycles to settle with the highest priority ID). All requesting agents remain in the RESOLUTION 3 state until a bus exchange is possible. The arbitration-state machine oversees the transfer-monitor machine and uses the equation for EXCHANGE shown in Fig 2 to determine whether the EXCHANGE conditions are fulfilled. When the EXCHANGE conditions are met, the machine makes the transition to the NO REQUEST state.

The arbitration controller controls the behavior of an agent when it's participating in arbitration. If a unit on the agent (for example, the CPU) needs to transfer data, the agent initiates a bus request (AGENT BREQ). The state machine enters the RESOLUTION state of arbitration if no current bus-request sequence is occurring (that is, if BREQ(L) is high), or if the current request sequence is ending (that is, if the bus can be exchanged on the next clock cycle) and a high-priority request is asserted (Fig 3).

In the RESOLUTION state, the arbitration-control

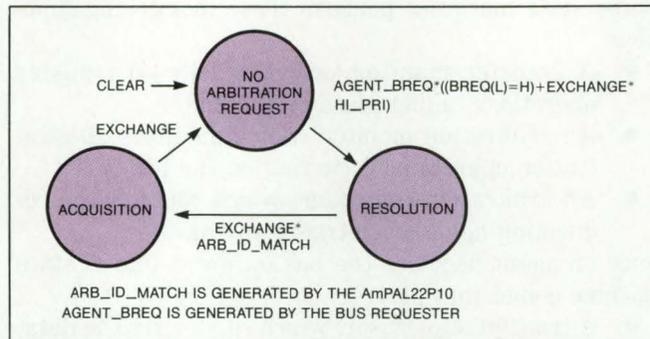


Fig 3—The arbitration-control state machine controls an agent's bus requests. An agent acquires ownership of the bus when the EXCHANGE condition is met and when the agent's ID matches the ID on the bus-arbitration lines.

machine sends a PUT ARB ID command to the combinatorial logic in the AmPAL22P10. Concurrently, the agent places its ID on the ARB lines. Using the status of the transfer- and arbitration-monitor machines, the arbitration-control machine waits in the RESOLUTION

Compact building blocks for arbitration logic

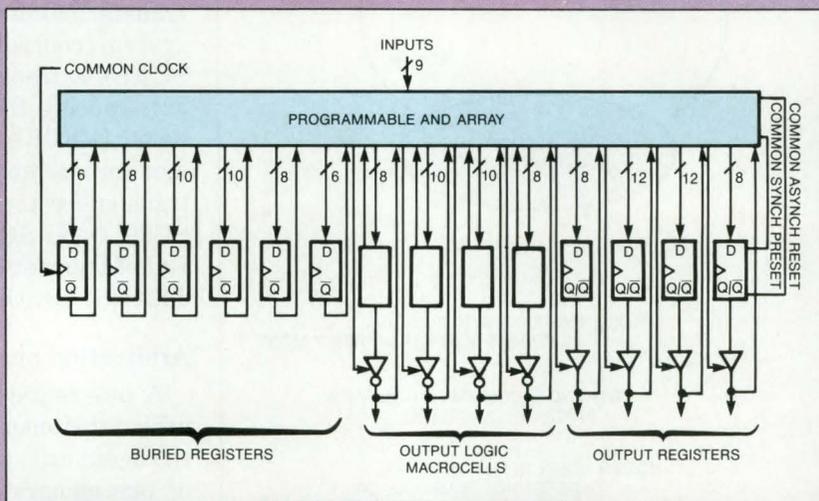
The AmPAL23S8 is a 20-pin programmable logic device capable of 33-MHz operation. It uses the sum-of-products (AND-OR) logic structure in conjunction with 14 on-chip state registers. The registers on the -23S8 provide a compact architecture for building the four state machines necessary to implement the bus-arbitration logic for Multibus II.

The device has six buried state registers, which give designers flexibility in designing sequence machines. The status of three of the four state machines for Multibus II is not needed by external units; therefore, the buried state registers provide convenient building blocks for these machines. The status of the fourth machine (the transfer-supervisor state machine) is required by other units; therefore, that machine can be

built around the I/O macrocells and output registers available on the chip.

Because the back-off algorithm only requires combinatorial logic, a programmable device

with a sum-of-products (AND-OR) logic structure is sufficient to implement the algorithm. The algorithm can be completely contained in a 24-pin AmPAL 22P10 chip.



Sum-of-products logic and 14 on-chip registers make the AmPAL23S8 suitable for use in Multibus II arbitration. You can use the six buried registers to build sequential machines.

state until the ID on the ARB lines matches its own ID (ARB ID MATCH) and the EXCHANGE condition is met. At least three bus clock cycles must occur in the RESOLUTION state before the agent can acquire bus ownership.

When the conditions are met, the arbitration-control state machine enters the ACQUISITION state and remains there until the bus transfers are complete. Fig 4's timing diagram shows the critical functions when two agents (A and B) simultaneously request control of the bus. Agent A has a higher priority than agent B.

An agent can park the bus

In the ACQUISITION state, the agent owns the bus and can perform data transfers. The bus owner can ensure that it retains exclusive use of the bus by

asserting SC1(L). This lock signal prevents other agents from gaining ownership of the bus while the current owner performs consecutive transfer operations. On the last data-transfer handshake sequence, the agent asserts the system control line SC2(L), effecting an EOT condition.

If another agent contends successfully for use of the bus, the current bus owner will transfer bus control to the other agent. If no other agents request access to the bus, the EXCHANGE condition, as defined in Fig 2, isn't met, and bus control remains, or is parked, with the current bus owner. This parked condition allows the agent to perform another transfer operation without contending for the bus, thus reducing the data-transfer setup time.

The transfer-supervisor state machine supervises the

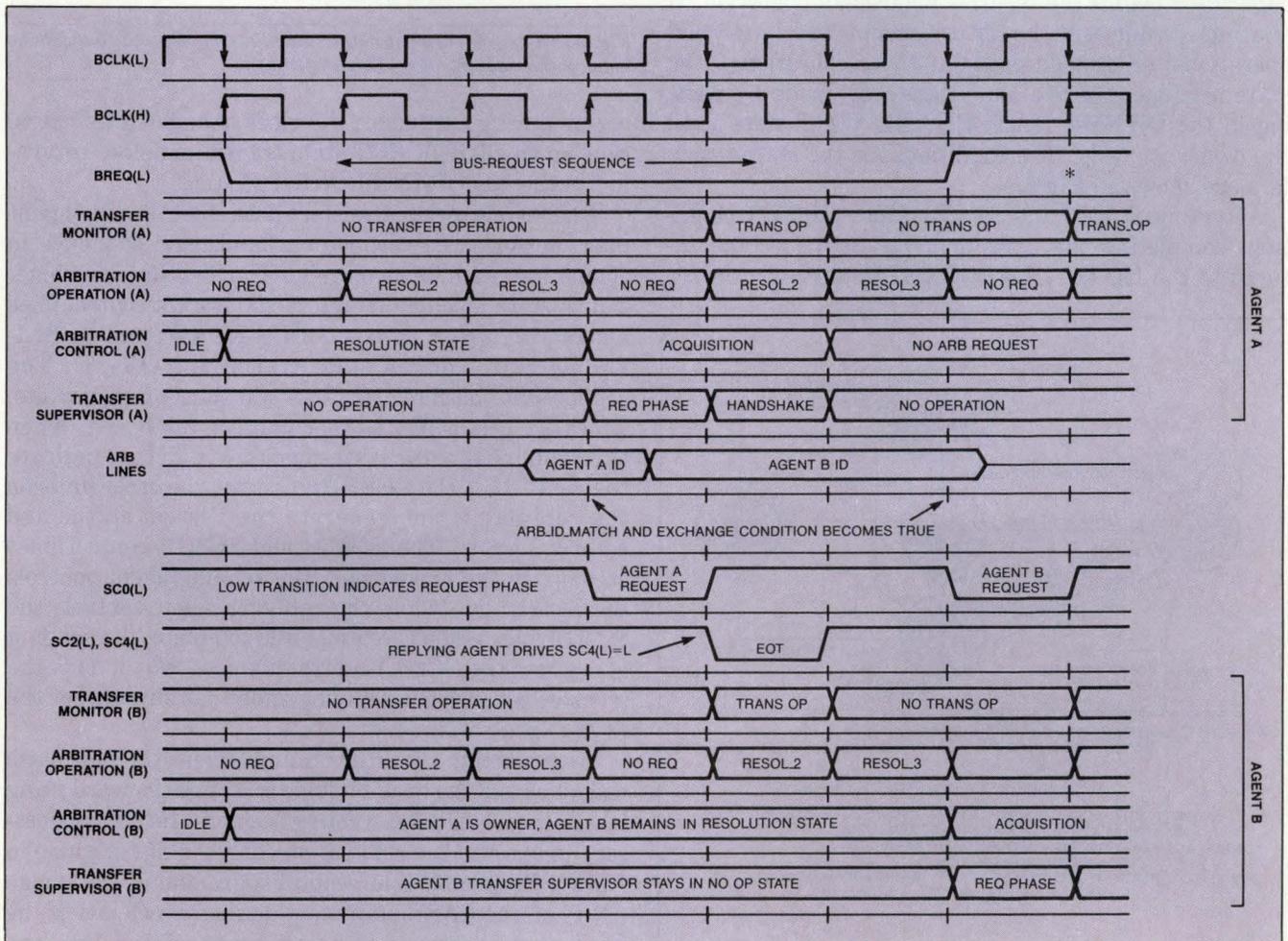


Fig 4—When two agents simultaneously request bus ownership, the higher priority agent (A in this case) assumes control first. When A releases control, ownership transfers to B in an orderly sequence.

When an agent is arbitrating for the bus, it needs to monitor several system control lines and operations.

agent while the agent performs data transfers (Fig 5). Other functional modules on the agent's board use the status of this machine to generate the proper control signals. For example, the machine enters the REQUEST PHASE state when the agent becomes the bus owner and asserts the operation parameters (such as an address to read from or write to). In the REQUEST PHASE state, read or write requests to a replying agent take place via the system control lines, SC0(L) through SC7(L), and addresses are set up on the address lines, AD0(L) through AD31(L).

An address-generating unit (for instance, the CPU) drives addresses or data onto the 32 AD lines. This unit generates the address when the REQUEST PHASE status appears on the transfer-supervisor state machine's registers. On the next clock cycle, the transfer supervisor begins the transfer handshake operation. If the bus owner isn't ready to accept data (on read operations) or provide data (on write operations), the state machine enters a handshake-wait mode by waiting in the OWNER HANDSHAKE WAIT state until the owner is ready. The conditions for the state transfers are shown in Fig 5.

Asserting SC2(L) and SC4(L) effects an EOT condition, completing the transfer. The state machine returns to the NO OP IN PROGRESS state. If an error

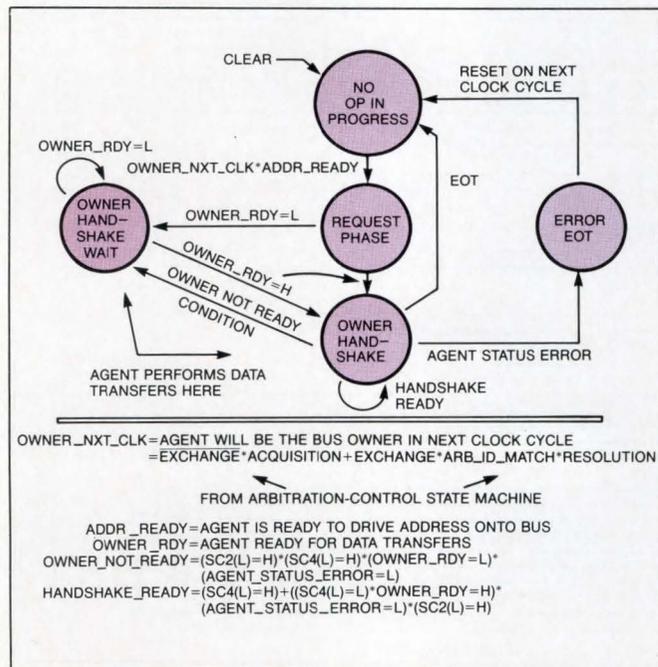


Fig 5—The transfer-supervisor state machine controls the data-transfer handshake protocol.

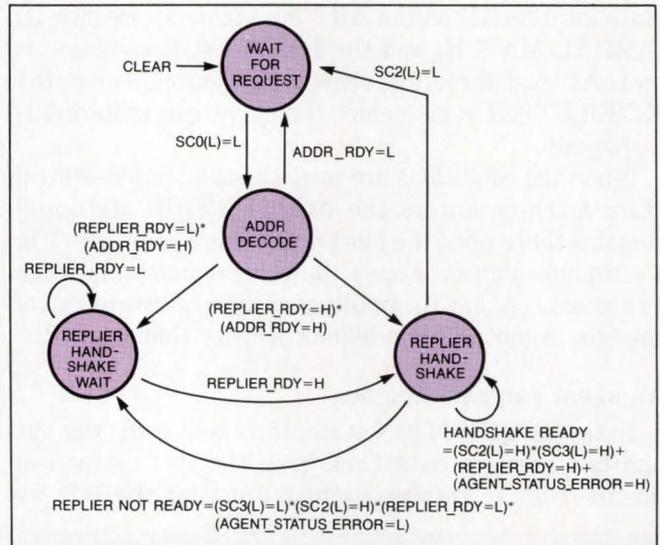


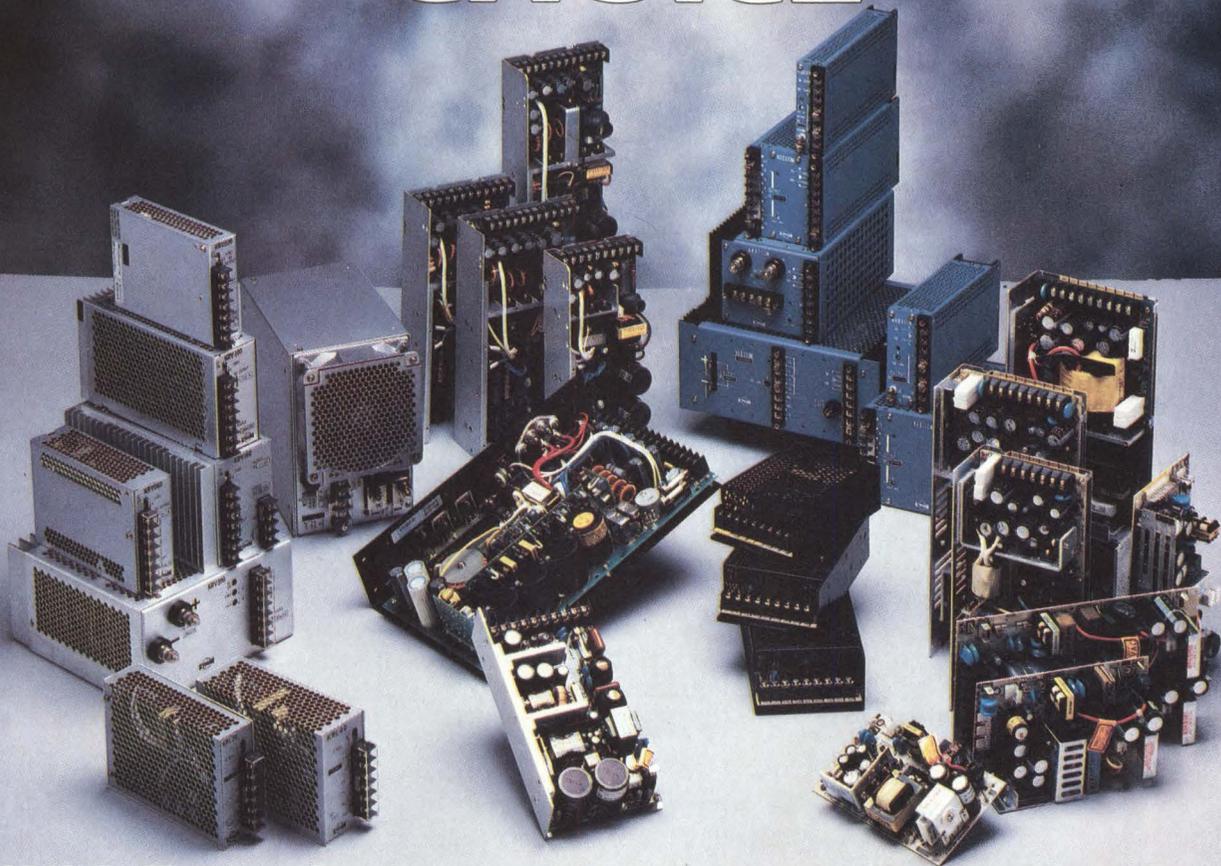
Fig 6—The repplier-transfer state machine manages the handshake logic in the replying agent to transfer data.

occurs during a transfer, the block transfer terminates, causing an ERROR EOT state transition before returning to the NO OP IN PROGRESS state.

When a bus owner transfers data, the replying agent must perform the responding handshake sequence in compliance with its own repplier-transfer state machine. This 4-state machine monitors six system control lines and two of its own signals, ADDR READY and REPLIER RDY, to control state transitions (Fig 6). The repplier state machine requires two status-register bits, which are accessible to other units on the board. When the repplier-transfer state-machine registers indicate the REPLIER HANDSHAKE state, the other units on the replying agent generate the system status and control signals. The SC3(L) and SC4(L) control lines accomplish the handshake. The sending agent controls the SC3(L) line while the replying agent controls the SC4(L) line. When the transfer is complete, the sending agent sets the SC2(L) control line low, which ends the transfer because the replying agent has already set the SC4(L) control line low.

Programming the PLDs to implement the four state machines and the back-off logic is straightforward using a high-level language. Listing 1 shows the steps necessary to execute the arbitration-control state machine in AMD's Programmable Logic Programming Language (PLPL). The CASE statement defines which one of the four state machines is being programmed into the AmpAL23S8. Note the correspondence of the statement sequence with the respective state diagram.

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Programming the PLDs to implement the four state machines and the back-off logic is straightforward using a high-level language.

LISTING 1—ROUTINE FOR ARBITRATION-CONTROL STATE MACHINE

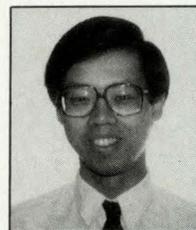
```
"ARB_OPER: 2-bit state machine in all requesting agents
that controls the arbitration operation -----"
case (arb_oper[1:0])
begin
NO_ARB)
begin "agent wants bus and there is no current bus req"
if (breq*(/bus_req + EXCHANGE*hi_pri)) then
begin
put_bus_request = 1; "assert bus request"
arb_oper[1:0] = RESOLUTION_STATE;
end;
else
arb_oper[1:0] = NO_ARB;
end;
RESOLUTION_STATE)
begin
put_arb_id = 1; "put arbitration ID on ARB lines"
if (EXCHANGE*arb_id_match) then
arb_oper[1:0] = ACQUISITION_STATE;
else
begin
arb_oper[1:0] = RESOLUTION_STATE;
put_bus_request = 1; "continue asserting bus request"
end;
end;
ACQUISITION_STATE)
begin
if (EXCHANGE) then
arb_oper[1:0] = NO_ARB;
else
arb_oper[1:0] = ACQUISITION_STATE;
end;
end;
end; "ARBITRATION OPERATION state machine"
```

Because logic equations specify the four state machines, the machines can operate in parallel in a PLD. Once the status of a state machine is updated, it is immediately available to the logic equations for the other state machines on the same PLD.

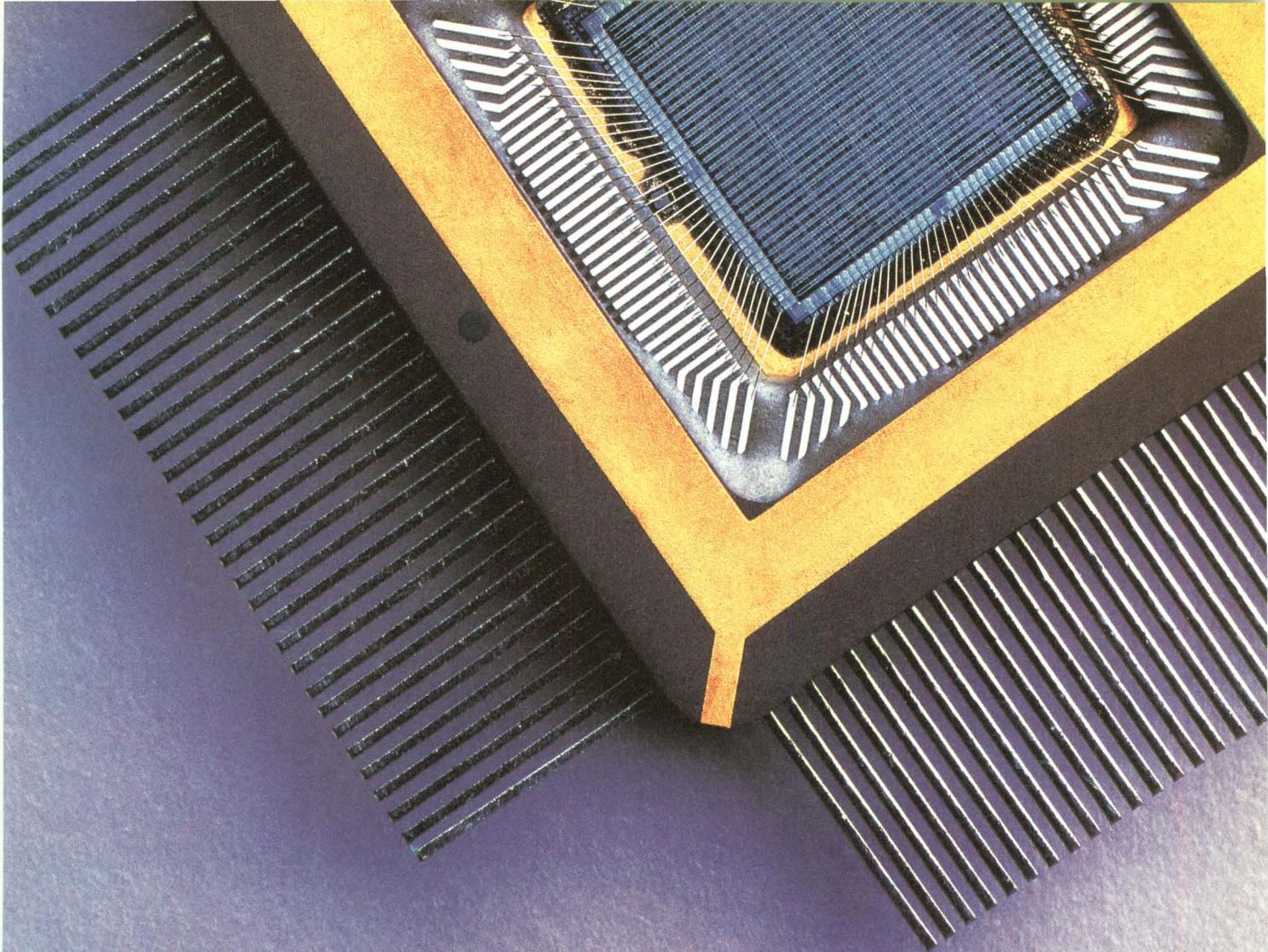
For example, if a transfer operation is detected on the bus (that is, SC0(L) is active), the transfer monitor moves to the DO TRANSFER state on the next clock cycle. The other state machines in the device immediately sense this state transition via output feedback. Any logic equation using the transfer-monitor status, such as EXCHANGE in the arbitration-monitor machine, is automatically updated for the next clock cycle. All of the other conditions are updated in parallel, making them current on the next clock cycle. **EDN**

Author's biography

Arthur Khu is a senior product planning engineer with Advanced Micro Devices in Sunnyvale, CA, and has worked with the company for three years. He presently researches and develops advanced logic-device architectures and design tools. Art holds a BS in math and computer science and an MS in computer science from Santa Clara University. In his spare time he enjoys racquetball and reading about technological history.



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Micropower op amp offers simplicity and versatility

An op amp whose input range includes both supply rails and whose output voltage swings within 100 mV of those rails can simplify a circuit by eliminating certain traditional components.

Zahid Rahim, *Signetics Corp*

Linear circuits intended to meet the stringent demands of medical and industrial instrumentation, remote data acquisition, and portable equipment must deliver precision at low voltages. A low-power, battery-operated op amp, for instance, requires precision dc characteristics to process low-level signals from high source impedances, low supply current to conserve power, and wide bandwidth to process audio-frequency signals. Because low-voltage applications produce low signal levels, the op amp should have a wide dynamic range at the input and output. Moreover, both it and its external circuit should function properly at the end-of-life battery voltage.

The NE5230 op amp is suited to such requirements. It operates from a supply voltage of 1.8 to 15V and performs well in systems powered by single 5V supplies. The op amp not only offers precision dc characteristics, its common-mode voltage can swing within 100 mV of either supply rail—a characteristic matched by few other commercially available op amps.

Furthermore, the bias-adjust terminal lets you adjust the op amp's slew rate from 90 to 250V/msec by varying the op amp's internal bias currents. The device

also offers decent performance in two other parameters of concern in low-power applications—noise and output-current drive. The NE5230's input voltage noise is 22 nV/ $\sqrt{\text{Hz}}$ at 1 kHz, and it can source and sink 5 and 11 mA, respectively, when operating from a 1.8V supply at 25°C. Other key specifications are listed in **Table 1**.

These attributes allow you to use the op amp in battery-powered applications such as half-wave and full-wave rectifiers, window detectors with rail-to-rail input ranges, temperature-limit alarms, sound-activated intrusion detectors, and supply-voltage splitters. An equally important application involves signal-conditioning circuits for bridge transducers—circuits that require no reference voltage or instrumentation amplifier.

Rectify signals without diodes

To keep costs low, battery-operated circuits for consumer applications should have a minimum component count. Fewer components also bestow the bonus of higher reliability. These considerations led to the half-wave-rectifier circuits of **Fig 1**. Neither circuit uses diodes. Because the op amp's input common-mode range extends beyond the supply rails, you can simply ground the noninverting terminal and thereby configure the amplifier as an inverter. You should also short the bias-adjust terminal (pin 5) to V^- to provide a maximum slew rate.

The amplifier behaves as a unity-gain inverter for negative inputs; positive inputs drive the output into saturation (**Fig 1a**). The NE5230's internal detectors prohibit the hard saturation that would occur in most op amps, however. Recovery from saturation is relatively fast. Operating from a 3V supply, the circuit can rectify

Battery-operated circuits for consumer applications should have a minimum component count, and fewer components also bestow the bonus of higher reliability.

signal amplitudes as high as $\pm 2.85\text{V}$ at frequencies well above 10 kHz. If the input signal has a reference level between 0V and V^+ , you can simply reference the amplifier's noninverting input to the same level. If required, resistors R_1 and R_2 can provide a gain other than unity.

To obtain a negative-polarity half-wave-rectified signal using a conventional op amp, you have to provide dual (bipolar) power supplies. The NE5230's rail-to-rail input range and near rail-to-rail output range, however, let you achieve this function using a single supply. Simply connect the supply's positive terminal and the amplifier's V^+ terminal to ground, and connect the supply's negative terminal to the amplifier's V^- terminal (Fig 1b).

The amplifier's common-mode range lets you reference the input signal to the positive rail (ground) by tying the noninverting and V^+ terminals together. (You can't do this with most op amps, and most op amps' output voltage must remain at least one V_{BE} voltage below the positive rail.) In short, you can use the amplifier with a single negative supply to condition the signal output from a variety of ground-referenced sensors. Again, if the input-signal reference is a voltage between 0V and V^- instead of ground, you should connect the amplifier's noninverting input to the same potential.

Overdriving most op amps (beyond the supply rail, for instance) saturates the input stage, causing a phase reversal within the amplifier that can reverse the feedback signal's polarity. Circuitry within the NE5230 prevents phase reversal for inputs as large as 2V beyond the supply rail. This feature allows the amplifiers of Fig

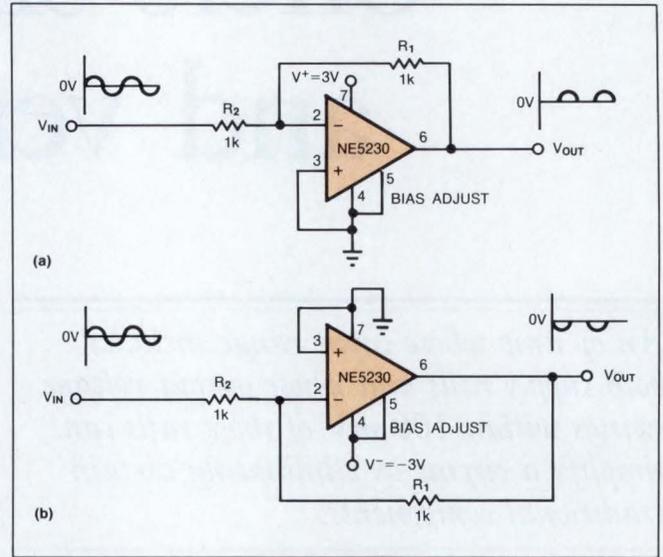


Fig 1—These positive (a) and negative (b) half-wave-rectifier circuits accomplish their job without the use of diodes. The resistors give you the option of gains other than unity.

TABLE 1—SALIENT SPECS FOR THE NE5230
($V^+ = 1.8\text{V}$; $V^- = \text{GND}$)

	BIAS CURRENT*	$T_A = 25^\circ\text{C}$	$0^\circ\text{C} < T_A < 70^\circ\text{C}$
SINGLE/DUAL SUPPLY VOLTAGE	—	1.8 TO 15V OR ± 0.9 TO $\pm 7.5\text{V}$	
SUPPLY CURRENT	LOW HIGH	110 μA 600 μA	250 μA MAX 800 μA MAX
OUTPUT SWING	ANY	1.6V	1.4V MIN
V_{os}	ANY	0.4 mV	4 mV MAX
I_b	LOW HIGH	20 nA 40 nA	150 nA MAX 200 nA MAX
A_{vo}	LOW HIGH	150V/mV 200V/mV	50V/mV MIN 100V/mV MIN
CMRR	ANY	95 dB	80 dB MIN
OUTPUT SOURCE CURRENT	HIGH	5 mA	4 mA (TYP) AT LOW BIAS
OUTPUT SINK CURRENT	HIGH	11 mA	5 mA (TYP) AT LOW BIAS
SLEW RATE	LOW HIGH	90V/mSEC 250V/mSEC	90V/mSEC 250V/mSEC
BANDWIDTH	LOW HIGH	250 kHz 600 kHz	—

*NOTE: THE NE5230 OPERATES AT LOW BIAS CURRENT IF THE BIAS ADJUST PIN (PIN 5) IS LEFT OPEN. SHORTING THE NE5230'S PIN 5 TO V^- PROVIDES MAXIMUM BIAS CURRENT. CONNECTING A VARIABLE RESISTOR BETWEEN PIN 5 AND V^- LETS YOU ADJUST THE AMPLIFIER'S BIAS CURRENT AND HIGH-FREQUENCY CHARACTERISTICS.

2 to produce half-wave rectification without external components for input signals referenced to 0V.

In Fig 2a, the amplifier output follows the input signal above 0V and goes into negative saturation for inputs below 0V. (The output clamps near 0V for negative inputs.) The circuit as shown can rectify signals of $\pm 2V$ at frequencies above 10 kHz. Inputs below $-2V$ will cause internal phase reversal, however, allowing the output voltage to rise. You can prevent this

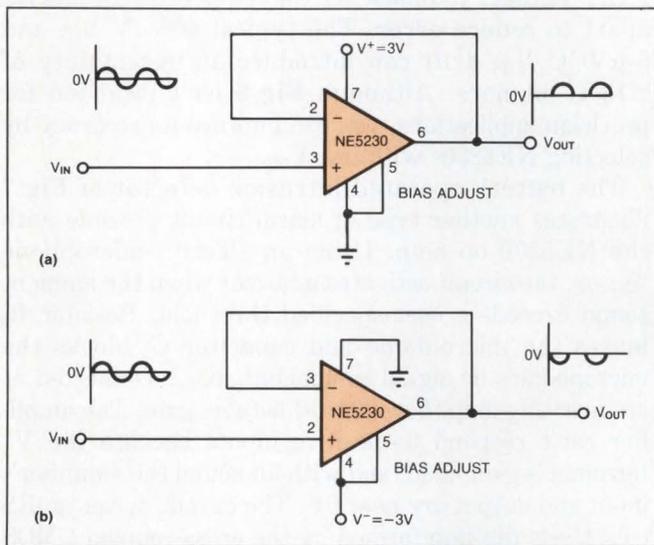


Fig 2—Requiring no external components, these op amp circuits perform positive (a) and negative (b) half-wave rectification for ground-referenced ac signals.

situation by adding a large resistor in series with the amplifier's input. To obtain a negative-polarity half-wave rectifier, simply reverse Fig 2a's supply-voltage connections (Fig 2b). Again, this circuit can rectify 0V-referenced signal amplitudes to $\pm 2V$ at frequencies above 10 kHz.

Fig 3's circuit performs full-wave rectification using a single positive power supply. When a negative input voltage causes IC₁ to clamp IC₂'s noninverting input to 0V, IC₁ delivers current through D₁ and R₃ to the signal source. IC₂ acts as an inverting amplifier for negative input signals. Positive input signals produce a differential voltage between the IC₁ inputs and create reverse-bias across D₁, placing IC₁'s output in negative saturation. This condition removes the 0V clamp at IC₂'s inverting input by breaking IC₁'s feedback loop. Consequently, IC₂ behaves as a follower during positive excursions of the input voltage.

Although D₁ is reverse-biased, clamp diodes at IC₁'s inverting input turn on and draw current through R₃. Accordingly, R₃'s value should be 500Ω or less to avoid a significant offset due to this parasitic current flow. (R₁ and R₂ can be large-valued resistors.) Fig 3b shows the circuit operating with a 5.7V p-p signal at 400 Hz. Similar to the way it rectified the half-wave circuits, the NE5230 performs negative full-wave rectification in Fig 4 using a single negative power supply. The same precautions apply as for Fig 3.

You can also use the NE5230 to monitor a signal and to detect fault conditions in which the signal is shorted

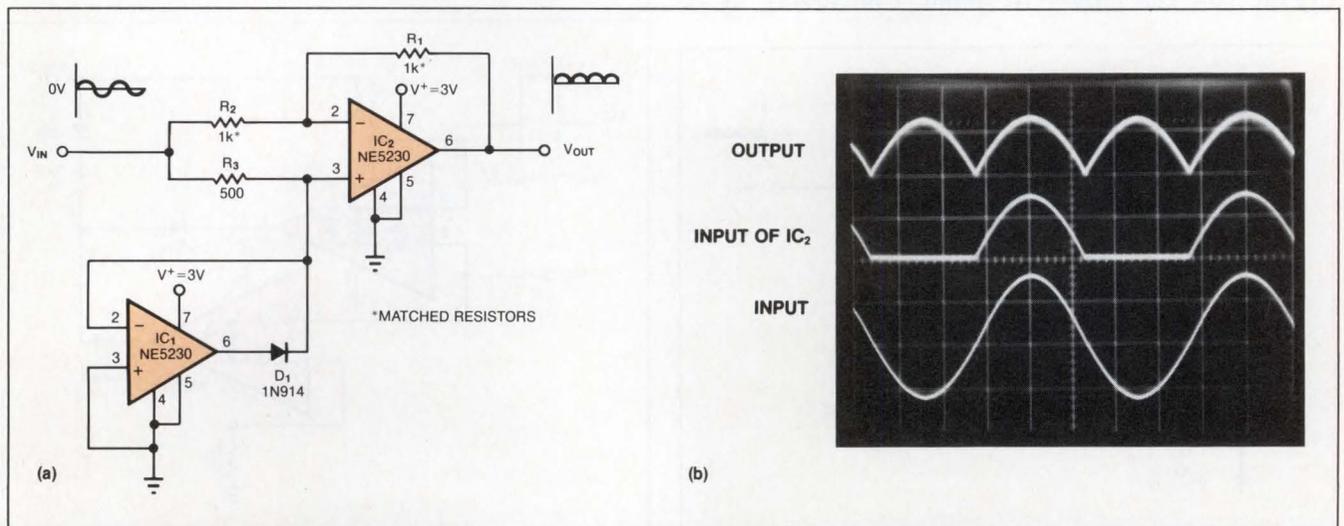


Fig 3—This absolute-value circuit (a) achieves full-wave rectification by clamping IC₂'s noninverting input to 0V when V_{IN} is negative, and removing the clamp when V_{IN} is positive. Thus, IC₂ alternates between an inverter and a follower every half cycle. The photo (b) shows circuit performance at 400 Hz for a 5.7V p-p input signal. The vertical scale is 2V/div, and the horizontal scale is 0.5 msec/div.

Overdriving most op amps saturates the input stage, causing a phase reversal within the amplifier that can reverse the feedback signal's polarity.

to either supply voltage. The window-detector circuit of **Fig 5** must have the same supply voltage as that of the remote signal source. Power-supply currents through R_1 and R_2 create small offsets essential to the circuit's operation.

Both op amp outputs remain in positive saturation for V_{IN} values between approximately 0 and 3V, which keeps the LED off. If V_{IN} shorts to V^+ , however, IC_1 saturates negatively (at 0V), turning on the LED. Similarly, IC_2 turns on the LED by saturating negatively when V_{IN} shorts to ground. As you can see, the op amp inputs' series resistors and clamp diodes limit the current drawn from the V_{IN} source.

Normally, building a 2-limit temperature alarm requires a temperature sensor and two op amps. The NE5230 itself becomes a temperature sensor, however, if you make use of the PTAT (proportional to absolute temperature) voltage at pin 5. This voltage is independent of the supply voltage and measures 14 mV at 27 °C. What's more, it changes predictably at a rate of 46.667 $\mu V/^\circ C$. For instance, at +85 and $-15^\circ C$, the pin 5 PTAT voltage is 16.7 and 12.04 mV, respectively.

The alarm circuit (**Fig 6**) uses these trip points to activate a buzzer when the ambient temperature moves outside of the -15 to $+85^\circ C$ window. The R_1/R_2 -divider voltage sets the upper temperature limit and the R_3/R_4 -divider voltage sets the lower one. When the ambient temperature exceeds $85^\circ C$, IC_1 's inverting-input voltage is more positive than that at the noninverting input, and the resulting saturated output (0V) causes the buzzer to sound. Conversely, IC_2 's

output sounds the buzzer when the ambient temperature drops below $-15^\circ C$, again by going into negative saturation.

The resistors that you use in the voltage dividers should have similar temperature coefficients to prevent a shift in threshold voltage as the temperature changes. On the other hand, the op amp's input-offset voltage (V_{OS}) has a greater effect on the circuit's accuracy. Because V_{OS} is a significant percentage of the small PTAT voltage, you must set the temperature limits far apart to reduce error. The typical 400- μV V_{OS} and 5- $\mu V/^\circ C$ V_{OS} drift can introduce an uncertainty of $\pm 15^\circ C$ or more. Although **Fig 6** isn't intended for precision applications, you can improve its accuracy by selecting NE5230s with low V_{OS} .

The battery-operated intrusion detector of **Fig 7** illustrates another type of alarm circuit possible with the NE5230 op amp. Using an electret-microphone sensor, the circuit activates a buzzer when the ambient sound exceeds a user-specified threshold. Resistor R_3 biases the microphone and capacitor C_1 blocks the microphone's dc signal component. IC_1 is connected as an inverting amplifier with adjustable gain. The amplifier can't respond to positive inputs because the V^- terminal is grounded, and without sound the amplifier's input and output are near 0V. The output drives an RS (reset-set) flip-flop formed by the cross-coupled CMOS Nor gates. Therefore, in the absence of sound the flip-flop's \bar{Q} output is high, and the buzzer is off. IC_2 's negligible standby current and the low quiescent cur-

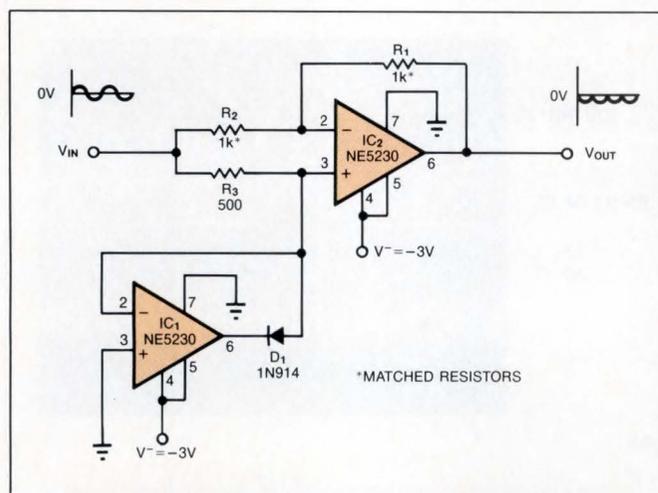


Fig 4—This circuit (obtained by reversing the power-supply connections in **Fig 3**) performs negative full-wave rectification using a single supply voltage.

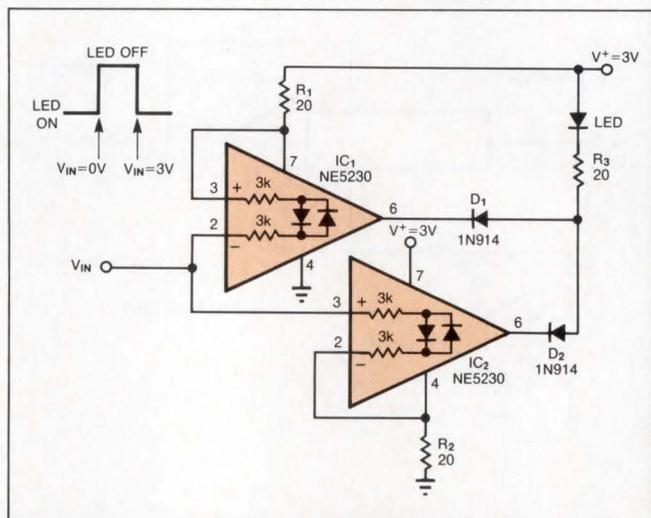


Fig 5—This window detector's rail-to-rail input range allows the circuit to detect faults in which the input signal becomes shorted to either rail.

rent of the microphone and op amp ensure long battery life.

Sound detector has adjustable threshold

Sound causes the microphone to produce an ac signal whose reference is ground on the other side of C_1 . (The capacitor you choose should have low leakage current.) This signal's negative excursions produce positive excursions at the flip-flop's S input. If the amplifier's gain (set by R_1) is sufficient, the signal at S will cross the gate's switching threshold and latch the Q output low,

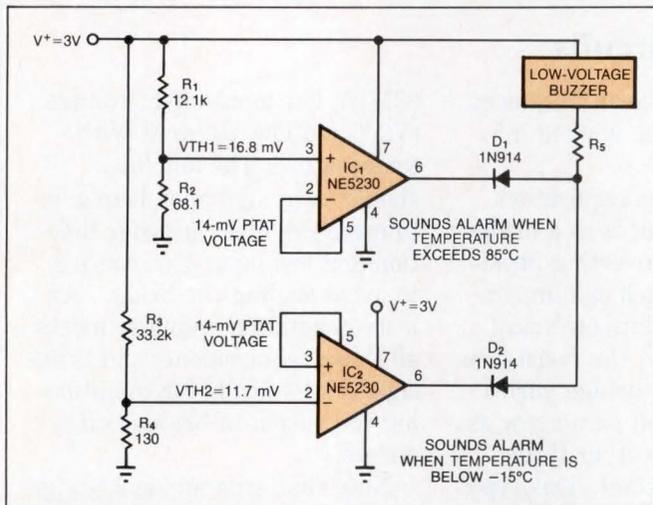


Fig 6—The op amp's bias-adjust pin (pin 5) is the PTAT (proportional to absolute temperature) voltage, which lets you use the amplifier as a temperature sensor. This circuit activates the buzzer when the temperature exceeds a user-specified limit.

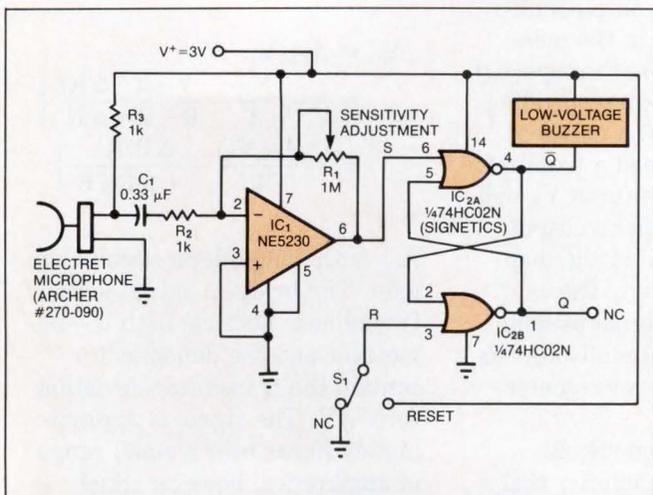


Fig 7—Ambient sound above a user-determined threshold activates this intrusion detector. Once triggered, the alarm will sound until you momentarily press the switch (S_1).

activating the buzzer. The buzzer will remain on until you reset the latch by momentarily pressing S_1 . Remember that high closed-loop gain settings will reduce the circuit's sensitivity to high-pitched sound by lowering the amplifier's -3 -dB bandwidth. If you need more sensitivity, you can cascade two op amps and split the required gain between them.

Circuits that process ground-referenced signals often require dual power supplies, but dual-voltage battery supplies can increase a system's size and cost. You can avoid this extra hardware in some cases by converting a single 3V lithium-battery output into a ± 1.5 V output (Fig 8a). The R_1/R_2 divider splits the 3V supply, and the op amp's 40-nA input-bias current offers a minimal load to the divider. The amplifier's output becomes the common terminal for all ground-referenced loads and signals.

The NE5230's low output impedance minimizes any offset voltage created by the connection of loads between the amplifier's output and V^- or V^+ . Moreover, the dual voltages track in magnitude as the battery cell discharges—a feature useful in applications that must maintain a precise voltage null despite fluctuations in the supply voltages. The Fig 8a circuit sources and sinks 15 and 24 mA, respectively.

To obtain higher load currents, you can connect two NE5230s in parallel (Fig 8b). The difference in offset voltages (ΔV_{OS}) appears across R_3 and R_4 . The standby current in one op amp increases by $\Delta V_{OS}/(R_3+R_4)$, but current in the other op amp decreases by the same

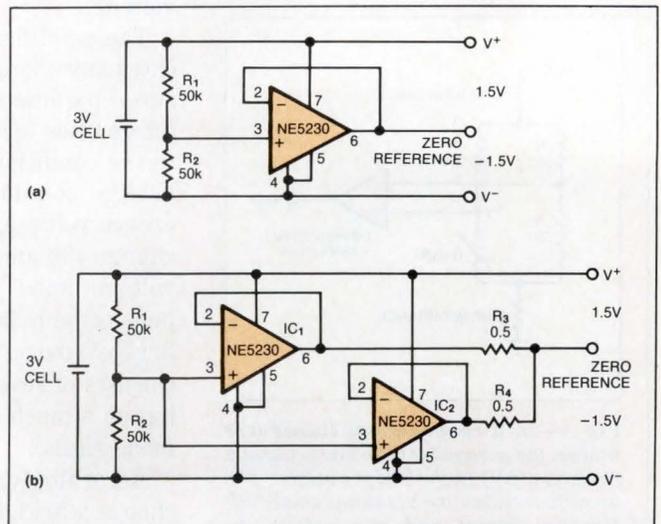


Fig 8—The circuit in a converts a 3V cell into a ± 1.5 V dual tracking supply. By connecting two amplifiers in parallel (b), you can nearly double the circuit's load-current capability.

The op amp becomes a temperature sensor if you make use of the PTAT (proportional to absolute temperature) voltage at pin 5.

amount, so the sum of the supply current through the two op amps remains constant.

Large load currents divide equally between the two op amps, and you would expect this circuit to provide twice the output current of Fig 8a, but the load-current capability is generally less because of mismatch in the op amp's output resistances and mismatch between R_3 and R_4 . The Fig 8b circuit sources and sinks 24 and 35 mA, respectively, when operating from a 3V supply.

Bridge transducers for precision applications usually

require an accurate low-drift voltage reference and a precision instrumentation amplifier (see box, "What you should know about bridge circuits"). The Fig 9 circuit, however, acquires and displays the bridge transducer's output without using a voltage reference or an instrumentation amplifier.

Op amp IC₁ buffers the fixed arm of the bridge and provides a reference potential for all ground-referred loads. Choosing this node as the reference potential converts the bridge's differential output signal to a

What you should know about bridge circuits

A bridge circuit, often known as a Wheatstone bridge, consists of a pair of series-connected resistors connected in parallel with a similar pair of resistors (Fig A). Bridge circuits are widely found in precision-null applications because the differential voltage ($V_1 - V_2$) across the bridge is 0V when the bridge is balanced.

What's more, this balanced condition is unaffected by voltage drops across line resistances or shifts in the reference voltage V_R . You can use such a balanced bridge to measure capacitance,

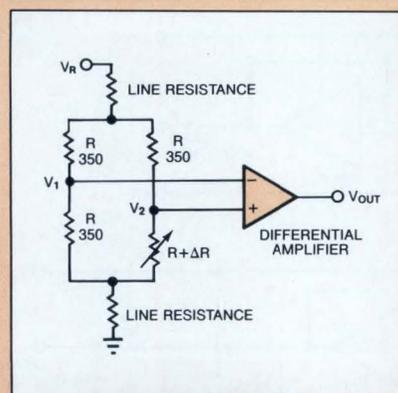


Fig A—In a conventional transducer bridge, the parameter of interest causes a variation (ΔV) in the bridge's output. The amplifier senses the resulting small differential signal and also rejects the bridge's relatively large common-mode voltage.

inductance, or its own frequency of excitation (when applied in place of V_R).

A more common application for a bridge circuit is as a bridge transducer for converting physical parameters such as temperature or pressure into electrical signals. Normally, the resistance in one arm of the bridge varies with the measured parameter as resistances in the other three arms remain constant. This type of application usually includes a differential amplifier to amplify the bridge's differential output voltage.

The amplifier's output indicates any change in the measured parameter with respect to a reference level corresponding to the condition of a balanced bridge. You do need a fixed reference voltage; shifts in V_R will change the amplifier's output voltage unless the bridge happens to be balanced. The bridge's output signal usually consists of several millivolts riding on a much larger common-mode signal.

Accordingly, you should choose a bridge amplifier that minimizes inaccuracies through high common-mode rejection

(CMR), low input-offset voltage (V_{OS}), and low V_{OS} drift with temperature. The amplifier should have high open-loop gain to ensure a linear transfer function and low input-bias current to avoid loading the bridge. An instrumentation amplifier meets all these requirements and is designed specifically for conditioning the output of bridge transducers.

Note that even an ideal bridge amplifier will have a nonlinear response because the bridge itself is inherently nonlinear. The following derivation shows why:

$$\begin{aligned} V_O &= A_{CL}(V_1 - V_2) \\ &= A_{CL} \left[\frac{V_R}{2} - \frac{V_R(R + \Delta R)}{R + R + \Delta R} \right] \\ &= - \frac{A_{CL} V_R}{4} \left(\frac{\Delta R/R}{1 + \Delta R/2R} \right). \end{aligned}$$

A_{CL} is the amplifier's closed-loop gain. The bridge's output signal is nonlinear because both the numerator and the denominator contain the transducer-deviation term ΔV . The signal is approximately linear over a small range of amplitudes, however. Such signals are held to low amplitude for that reason.



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CIRCLE NO 101

Bridge transducers for precision applications usually require an accurate low-drift voltage reference and a precision instrumentation amplifier.

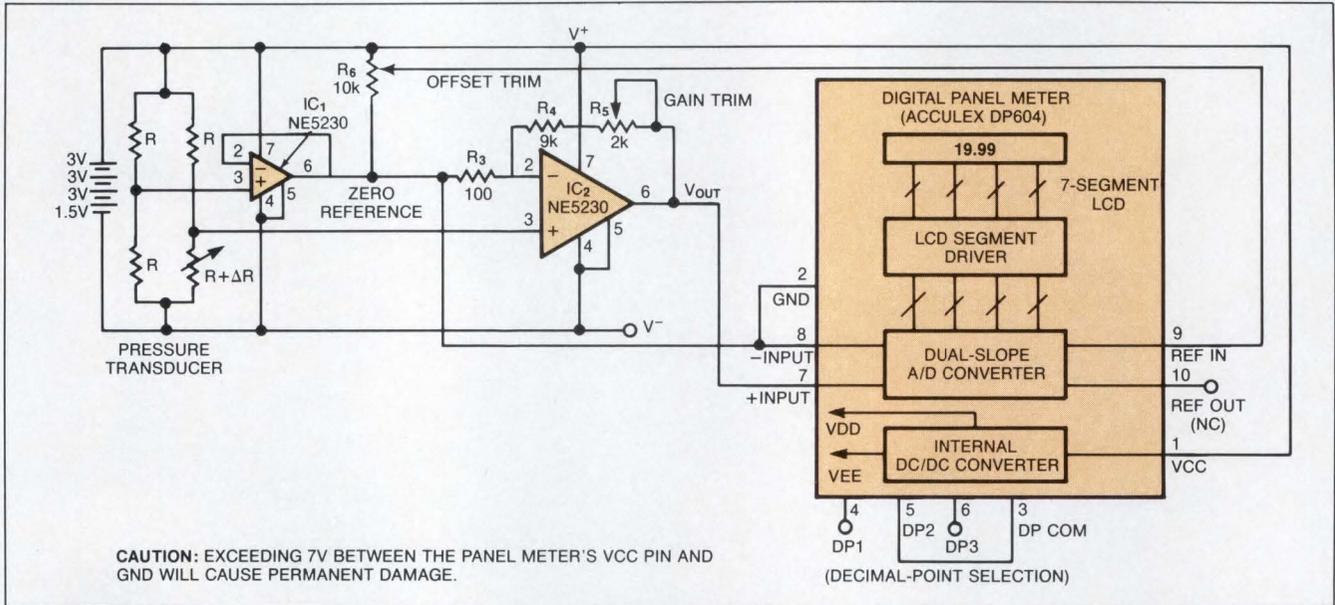


Fig 9—This bridge-transducer interface circuit conditions the bridge's output signal for ratiometric operation and eliminates the need for a reference voltage and an instrumentation amplifier.

single-ended signal referred to ground. This reference remains halfway between V^+ and V^- even if the battery discharges. The reference potential is thus a floating ground, often called an active guard.

Converting the bridge's differential signal to a ground-referred signal eliminates the bridge output's common-mode voltage, which also eliminates the need for common-mode rejection, usually obtained by adding an instrumentation amplifier. IC_2 amplifies the bridge's output signal, and R_5 lets you adjust the circuit's full-scale output level.

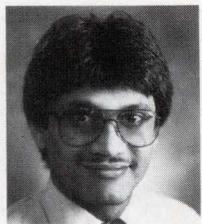
The IC_2 output V_{OUT} will change as the batteries discharge, but the V_{OUT}/V^+ ratio will remain fixed. This relationship lets you remove the effect of battery discharge by operating the panel meter's A/D converter in the ratiometric mode. Connect the wiper of R_6 to the converter's reference input to ensure that the signal and reference remain in proportion as the supply voltage changes. Finally, note that IC_2 amplifies its own input-offset voltage. You should null this effect by first balancing the bridge, and then adjusting R_6 for an all-zeros output at the panel meter. **EDN**

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Author's biography

Zahid Rahim is a design engineer with Signetics Corp in Sunnyvale, CA, and is responsible for the design of data-conversion and -acquisition ICs. He is a member of the IEEE and enjoys playing tennis and collecting coins.



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Article Interest Quotient (Circle One)
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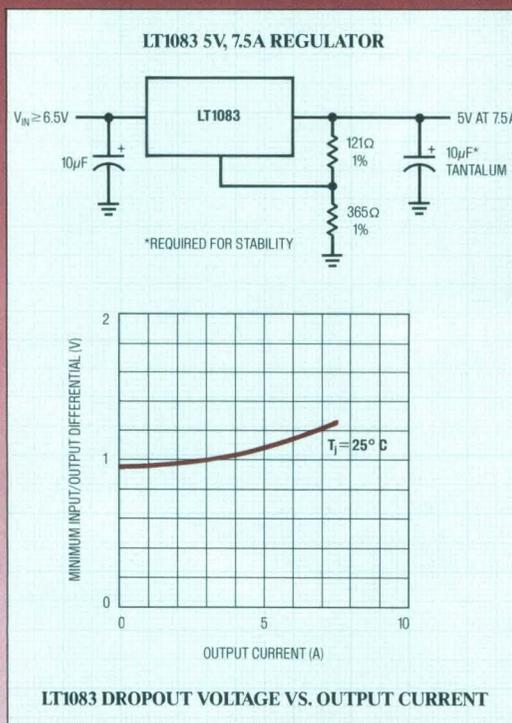


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DESIGN IDEAS

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Baseline restorer is voltage-programmable

Peter Henry

Precision Monolithics Inc, Santa Clara, CA

The Fig 1 circuit is a nonlinear, highpass filter that acts as an active baseline restorer (Fig 2). Baseline restoration improves the signal-to-noise ratio for pulse or ac measurements by counteracting the dc errors caused by amplifier drift and electromagnetic pickup. The circuit is particularly useful for signals derived from a high-impedance source such as the human body.

Unlike standard frequency-domain filters, this one acts on the slew rate rather than the frequency of the input signal. At V_{OUT} , the circuit restores the base level of input-signal pulses to an arbitrary level set by V_{REF} . You set the filter's slew-rate cutoff by adjusting $V_{PROGRAM}$, which in turn sets the currents I_1 and I_2 . (In applications such as analog adaptive filtering, you can set $V_{PROGRAM}$ using a voltage-output D/A converter, or you can remove $R_{PROGRAM}$ and set the currents using a current-output D/A converter.)

To understand the circuit operation, first note the action of the transistor current mirrors: Collector current in Q_2 (I_1) mirrors the collector current in Q_1 , and the transistors Q_5 and Q_6 mirror this current again. Transistors Q_3 and Q_4 each mirror the I_1 current as well, producing the current $I_2=2I_1$. This $2\times$ relationship assures symmetric operation, in which the restoration rates are equal for positive and negative excursions from the baseline.

Assume the capacitor C has charged to the input signal's baseline voltage. If the baseline level of V_{OUT} attempts to rise, the IC_2 output swings low, decreasing the current through D_1 . This action causes a flow of current from capacitor C and thus restores equilibrium by lowering the voltage on C . Conversely, a tendency for the baseline to fall causes charge to flow onto the capacitor.

The IC_2 op amp must have a high slew rate to ensure that the restoration circuitry keeps up with the pulses. The rate of restoration depends on the current available (I_1) to charge C . Using $V_{PROGRAM}$, you can set this current to any value between a few nanoamps and a few milliamps. Higher current lets the circuit reject higher slew rates.

EDN

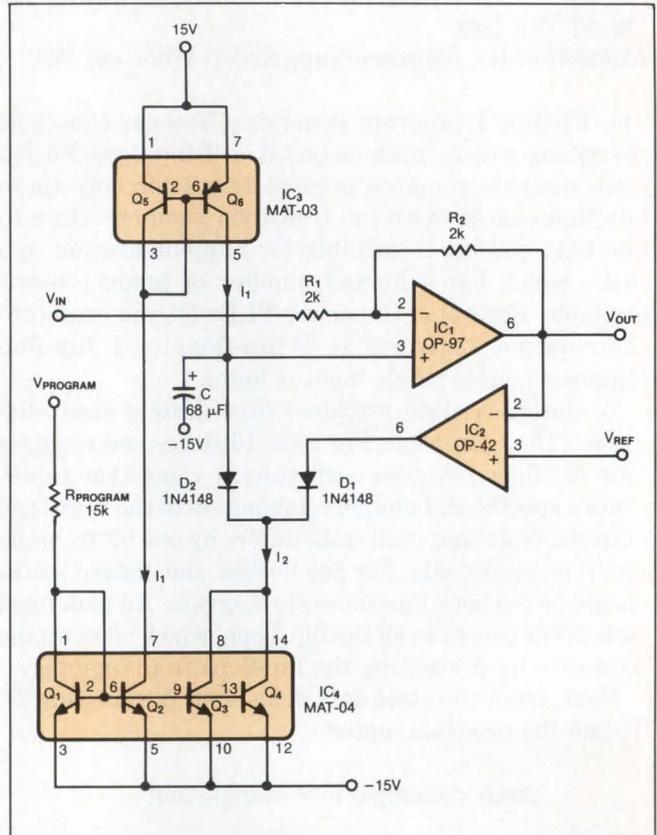


Fig 1—This circuit forces the bases of pulses in V_{IN} to the arbitrary level V_{REF} , and it rejects pulses on the basis of slew rate according to the voltage $V_{PROGRAM}$.

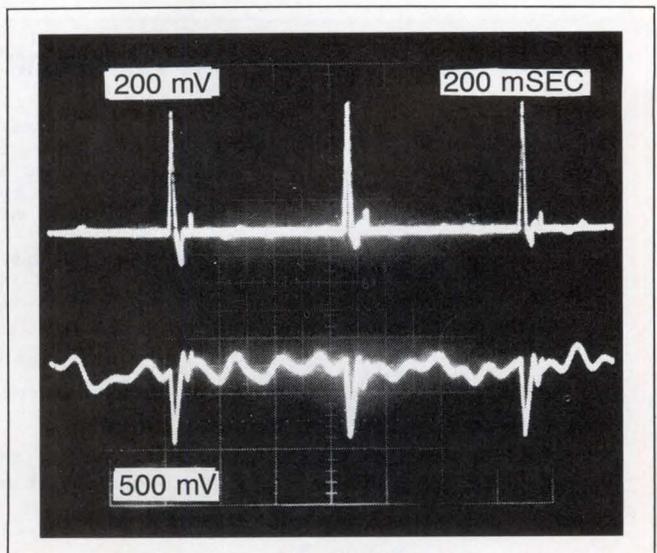


Fig 2—These waveforms show that the Fig 1 circuit's output (upper trace) inverts V_{IN} (lower trace) while filtering and restoring the signal's baseline voltage level.

To Vote For This Design, Circle No 749

Program designs T flip-flop state machines

David Van Ess
 Rothenbuhler Engineering, Sedro Woolley, WA

The Listing 1 program generates Boolean equations describing a state machine based on T flip-flops. Such a state machine requires product terms for only those bits that change with the transition from one state to another, making it suitable for implementation in a PLD, which has a limited number of product terms available. Several of the newer PLDs let you configure their output registers as T flip-flops (a T flip-flop toggles when its single input is high).

To design a state machine, first draw a state diagram. (The example in Fig 1 has 16 states and requires four flip-flops.) Assign each state a value that represents a specific and unique combination of the register's outputs. Note that each state differs by one bit from the states on either side. For any design, the unused states should be fed back into the state diagram. An undefined state feeds zeroes to all the flip-flops, which locks up the hardware by preventing the flip-flops from toggling.

Next, enter the state data in an input file (Listing 2). To run the program, enter

```
state <example.in> example.out
```

The output (Listing 3) contains unminimized Boolean expressions; you can minimize them using logic-description software such as Abel or CUPL. This state ma-

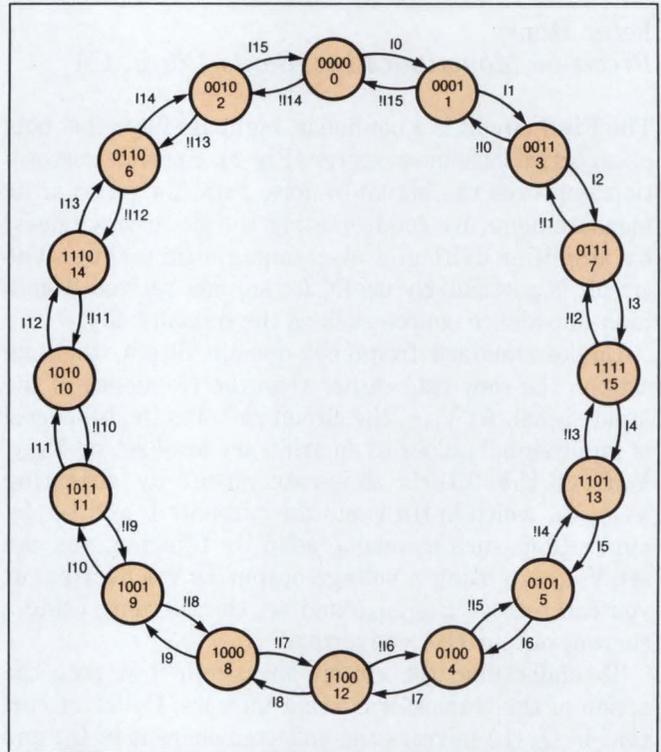


Fig 1—This diagram describes a state machine based on four T flip-flops. The state machine has 16 states; none are unused.

chine will just fit into an Intel 5C060 or an Altera EP600 PLD.

The Listing 1 program was compiled on an IBM

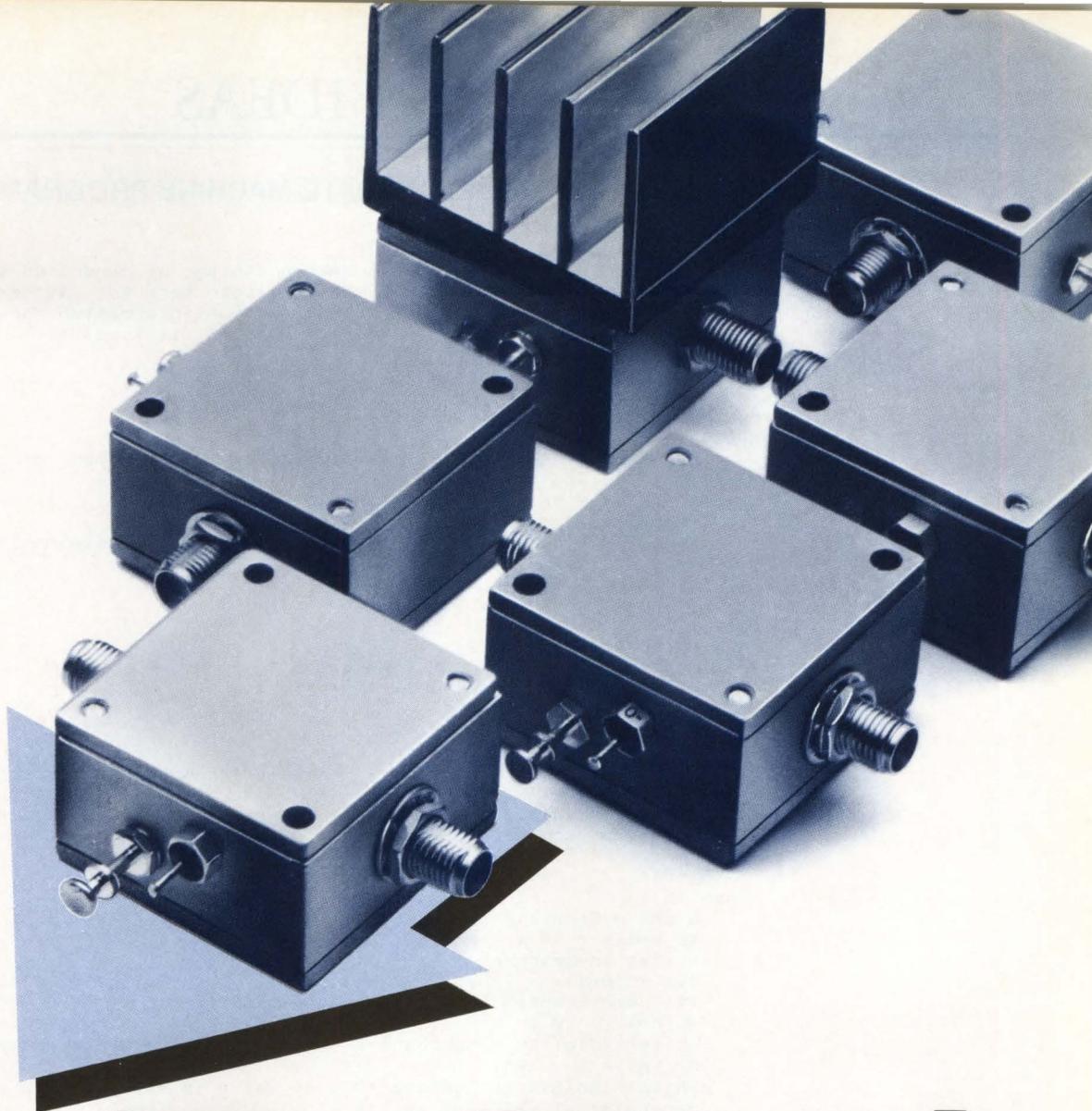
LISTING 1—T FILP-FLOP STATE-MACHINE PROGRAM

This program generates logic equations for state machines with up to 8 "T" registers. The output is the equation to implement it. Input is stdin, output is stdout, error is stderr. Below is an example of a 2 bit up/down counter. The first character of input must be that number of registers. All tabs and spaces are ignored. Upper, lower, or mixed case allowed.

```
2"very first character MUST be the # of registers
"this is a comment
at 0
on[ up ]1
on[!up ]3
at1
    on[ up ]2 "this comment must have a white space before it
on[!up ]0
AT2
ON[ up ]3
On[!up ]1 "this comment must have a white space before it
At 3
on [ up ] 0
on[!up ]2
End
```

*/

Listing continued on pg 194



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ZFL-1000H	10-1000	28	+20	5.0	219.00 1-9
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DESIGN IDEAS

LISTING 1—T FILP-FLOP STATE-MACHINE PROGRAM (Continued)

```
#include <stdio.h>
#include <ctype.h>
char *L_pnt[ 8 ], *R_pnt[ 8 ]; /*Keep storage of generated equations*/
char Term[ 32 ], *T_pnt; /* the logic term for "at" */
char Condition[81], *C_pnt; /* condition information for "on" */
int Reg_num; /* number of flipflops */

main( ){
    int at_val, on_val, c, x;
    char *malloc(), *append();
    void cal_term(), generate();
    Term[32] = '\0';
    Reg_num = getchar() - '0'; /* first character is the number of registers*/
    for( x = 0 ; x < Reg_num ; x ++ ){
        L_pnt[ x ] = R_pnt[ x ] = malloc( 4096 );
        if ( L_pnt[ x ] == NULL ) {
            fprintf( stderr, "ERROR: not enough memory available\n" );
            exit( 1 );
        }
    }
    while(1){
        switch( c = getchar() ){
            case ' ': /* comment line */
                while( (c = getchar()) != '\n' );
                break;
            case 'a': /* at stuff */
            case 'A':
                while( isdigit( c = getchar() ) == 0 ); /*remove white space */
                at_val = c - '0';
                while( isdigit( c = getchar() ) ) at_val = 10 * at_val + c - '0';
                cal_term( at_val );
                break;
            case 'o': /* on stuff */
            case 'O':
                C_pnt = Condition;
                *C_pnt++ = '[';
                while( (c=getchar()) != '[' );
                do( *C_pnt++ = (char)(c = getchar()); ) while( c != ']' );
                if( Condition[1] == ']' ) C_pnt = Condition;
                *C_pnt = '\0';
                while( isdigit( c = getchar() ) == 0 ); /*remove white space */
                on_val = c - '0';
                while( isdigit( c = getchar() ) ) on_val = 10 * on_val + c - '0';
                generate( at_val ^ on_val );
                break;
            case 'e': /* end stuff */
            case 'E':
                for( x = 0 ; x < Reg_num; x ++ ){
                    printf( "Q%c.t := ", 'a' + x );
                    if( L_pnt[ x ] == R_pnt[ x ] ){
                        printf( "\n\n" );
                    }
                    else{
                        *R_pnt[x] = '\0';
                        printf( "%s\n", L_pnt[x] );
                    }
                }
                exit(0);
            case ' ': /* leading white space */
            case '\t':
            case '\n':
                break;
            default :
                fprintf( stderr, "ERROR:Something is wrong with your input\n" );
                exit( 1 );
        }
    }
}

void cal_term( state ) /* generate the booleen expression for new "at"*/
int state;{
    int x;
    T_pnt = &Term[32];
    for( x = 0 ; x < Reg_num ; x ++, state >>= 1 ){
        *--T_pnt = ' ';
        *--T_pnt = 'a' + x;
        *--T_pnt = 'Q';
        *--T_pnt = ( state % 2 ) ? ' ' : '!';
    }
}
```

Listing continued on pg 196

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DESIGN IDEAS

LISTING 1—T FILP-FLOP STATE-MACHINE PROGRAM (Continued)

```

}
void generate( diff ) /* generate the logic for this "on" statement */
int diff;{
    int x ;
    for( x = 0 ; x < Reg_num ; x ++, diff >= 1 ){
        if(diff % 2 ){
            if(L_pnt[x] != R_pnt[x]) R_pnt[x] = append( R_pnt[x], "      + " );
            R_pnt[x] = append( R_pnt[x], T_pnt );
            R_pnt[x] = append( R_pnt[x], Condition );
            R_pnt[x] = append( R_pnt[x], "\n" );
        }
    }
}
char *append( old_string, add_string ) /* append one string to another */
char *old_string, *add_string;{
    while ( *add_string ) *old_string++ = *add_string++;
    return( old_string );
}

```

LISTING 2—INPUT FOR LISTING 1

" This state machine has 16 used states and 0 unused states.

```

at 0
    on [ I0 ] 1
    on [ !I14 ] 2
at 1
    on [ I1 ] 3
    on [ !I15 ] 0
at 2
    on [ I15 ] 0
    on [ !I13 ] 6
at 3
    on [ I2 ] 7
    on [ !I0 ] 1
at 4
    on [ I7 ] 12
    on [ !I5 ] 5
at5
    on [ I6 ] 14
    on [ !I4 ] 13
at6
    on [ I14 ] 2
    on [ !I2 ] 14
at7
    on [ I3 ] 15
    on [ !I1 ] 3
At8
    on [ I9 ] 19
    on [ !I7 ] 12
At9
    on [ I10 ] 11
    on [ !I8 ] 18
At10
    on [ I12 ] 14
    on [ !I10 ] 11
At11
    on [ I11 ] 10
    on [ !I9 ] 19
At12
    on [ I8 ] 18
    on [ !I6 ] 14
at13
    on [ I5 ] 15
    on [ !I3 ] 15
at14
    on [ I13 ] 6
    on [ !I11 ] 10
at15
    on [ I4 ] 13
    on [ !I2 ] 7

```

LISTING 3—OUTPUT FROM LISTING 1

```

Qa.t := !Qd !Qc !Qb !Qa [ I0 ]
      + !Qd !Qc !Qb Qa [ !I15 ]
      + !Qd Qc !Qb !Qa [ I15 ]
      + !Qd Qc !Qb Qa [ I6 ]
      + Qd !Qc !Qb !Qa [ I9 ]
      + Qd !Qc !Qb Qa [ !I8 ]
      + Qd !Qc Qb !Qa [ !I10 ]
      + Qd !Qc Qb Qa [ I11 ]

Qb.t := !Qd !Qc !Qb !Qa [ !I14 ]
      + !Qd !Qc !Qb Qa [ I1 ]
      + !Qd !Qc Qb !Qa [ I15 ]
      + !Qd !Qc Qb Qa [ !I0 ]
      + Qd !Qc !Qb Qa [ I10 ]
      + Qd !Qc !Qb Qa [ !I9 ]
      + Qd Qc !Qb Qa [ !I3 ]
      + Qd Qc Qb Qa [ I4 ]

Qc.t := !Qd !Qc Qb !Qa [ !I13 ]
      + !Qd !Qc Qb Qa [ I2 ]
      + !Qd Qc Qb !Qa [ I14 ]
      + !Qd Qc Qb Qa [ !I1 ]
      + Qd !Qc !Qb !Qa [ !I7 ]
      + Qd !Qc Qb !Qa [ I12 ]
      + Qd Qc !Qb !Qa [ I8 ]
      + Qd Qc Qb !Qa [ !I11 ]

Qd.t := !Qd Qc !Qb !Qa [ I7 ]
      + !Qd Qc !Qb Qa [ !I4 ]
      + !Qd Qc Qb !Qa [ !I12 ]
      + !Qd Qc Qb Qa [ I3 ]
      + Qd Qc !Qb !Qa [ !I6 ]
      + Qd Qc !Qb Qa [ I5 ]
      + Qd Qc Qb !Qa [ I13 ]
      + Qd Qc Qb Qa [ !I2 ]

```

PC/AT computer using a Datalight C package, but the program should compile on most C packages. This program could be augmented with a preprocessor that would do syntax checking, look for out-of-range state values, and pinpoint input errors. Moreover, such a preprocessor should allow string substitution and the use of macros, so you could refer to the states by a name instead of their assigned value.

EDN

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Circuit vocalizes dialed phone numbers

V Lakshminarayanan
Sneha Corp, Bangalore, India

A touch-tone telephone that includes the circuit of **Fig 1** produces a spoken report as you depress each key. By vocalizing the numbers and symbols of its keypad, the phone provides an audible confirmation that is useful to

the blind. The connections between circuit and telephone are in the figure's upper right corner.

The serial-interface, 2k-byte×8-bit ROM (IC₄) stores programmed sequences of instructions that are executed by the speech-processor chip IC₂ (manufactured by General Instrument Corp and available through Radio Shack). The applications brochure for IC₂ con-

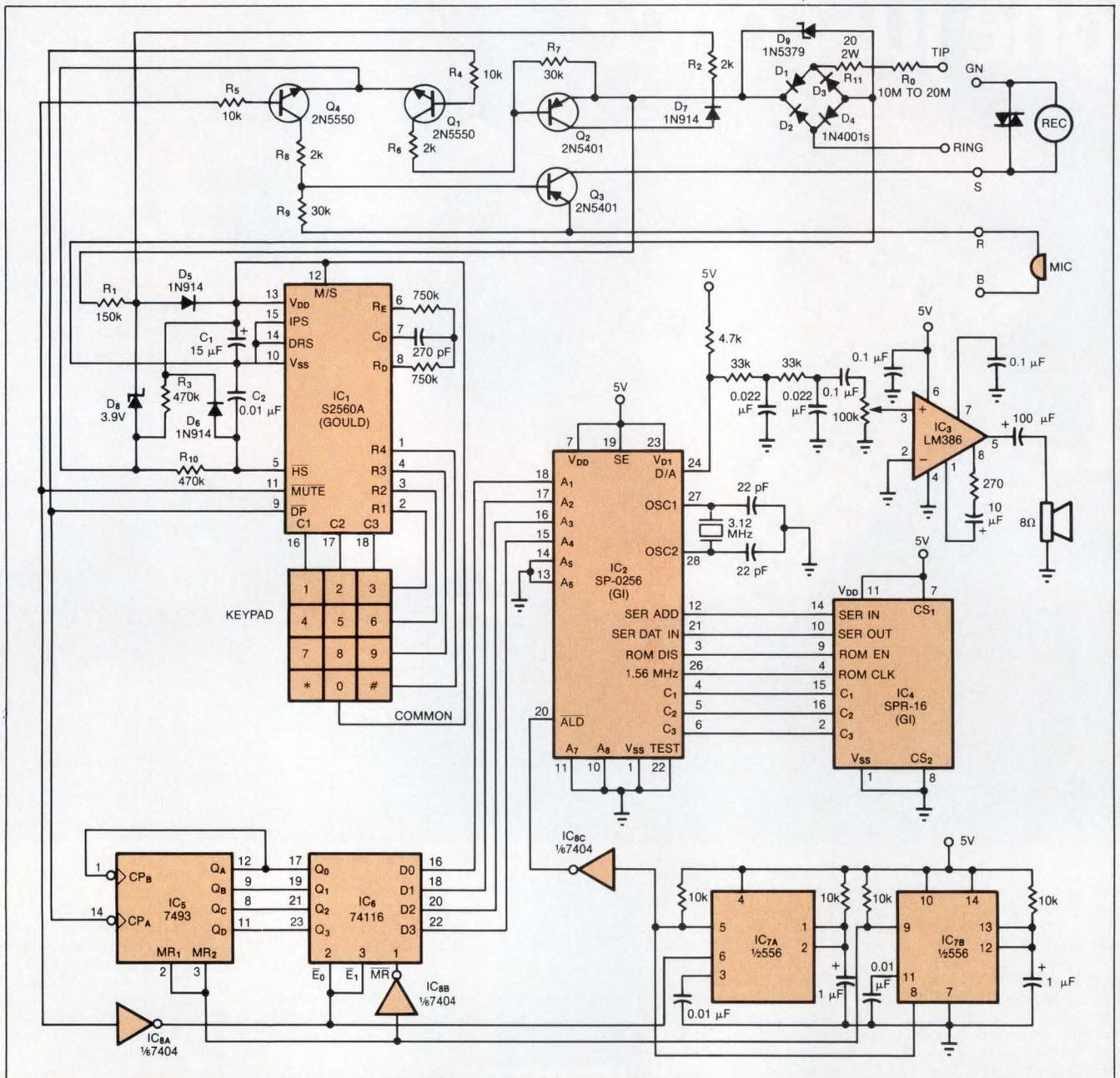


Fig 1—For each key you depress on a telephone keyboard, this circuit vocalizes the corresponding number or symbol.

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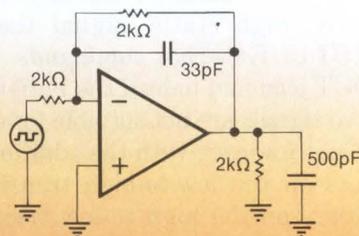
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DESIGN IDEAS

tains directions for composing the necessary instruction sequences.

When you depress a key, the tone-dialer chip IC₁

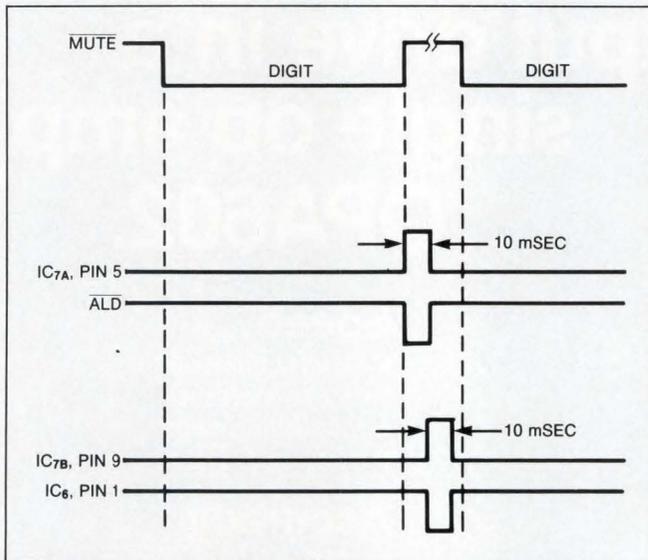


Fig 2—These timing waveforms for the circuit in Fig 1 show the relationship between the MUTE signal and the reset and latch-enable pulses.

issues the corresponding number of pulses at its \overline{DP} output. Counter IC₅ totals the pulses, and IC₆ latches the resulting 4-bit digital word. This word, converted to serial format by IC₂, becomes an address that selects a block of memory within IC₄.

IC₁'s MUTE output (which normally mutes the telephone receiver during dial pulsing) goes high during the pause interval between digits (Fig 2). Inverter IC_{8A} inverts this signal, and the resulting negative edge triggers the IC_{7A} timer (configured as a monostable multivibrator), which produces a 10-msec pulse at pin 5. This pulse latches the 4-bit address within IC₂ by driving IC₂'s ALD input low. The pulse also triggers IC_{7B} to produce another 10-msec pulse, which resets the IC₅ counter and the IC₆ latch.

Meanwhile, a microcontroller within IC₂ controls data flow from IC₄ and uses the data to create a pulse-width-modulated signal at IC₂'s pin 24. This signal undergoes passive filtering and amplification by the audio power amplifier IC₃ before producing an audible word at the speaker.

EDN

To Vote For This Design, Circle No 746

Signal edges set and clear D flip-flop

Dan Kuechle
Network Systems Corp, Minneapolis, MN

For a D flip-flop, set and clear (\overline{S} and \overline{C}) are level-sensitive control inputs. The Fig 1 circuit, however, lets you set and clear such a flip-flop using the transitions of selected signals.

In this example, the flip-flop IC_{1A} generates the active-high status signal that's labeled BUFFER FULL. External commands XFER IN and XFER OUT load and unload the buffer (not shown), but these two signals are not suitable for direct control of flip-flop IC_{1A}. However, with the addition of IC_{1B} as shown, IC_{1A} sets on the low-to-high transition of XFER IN and clears on the high-to-low transition of XFER OUT. (The narrow \overline{Q} pulse from IC_{1B} has a duration only twice the flip-flop's propagation delay, but this duration is sufficient to clear IC_{1A}.)

EDN

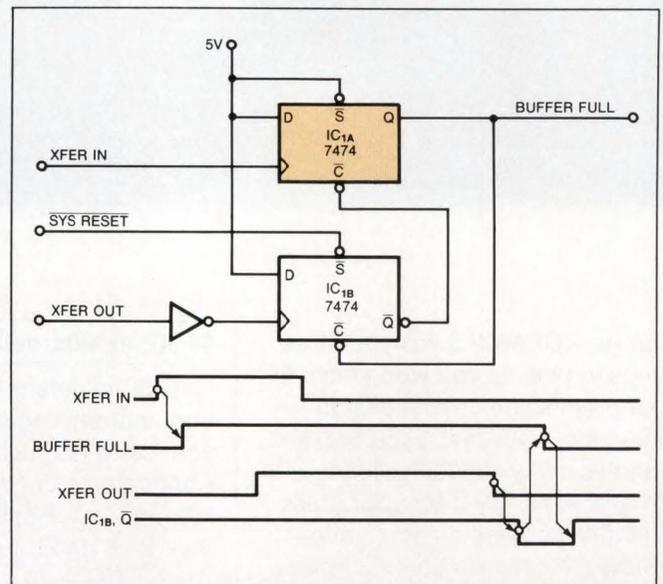
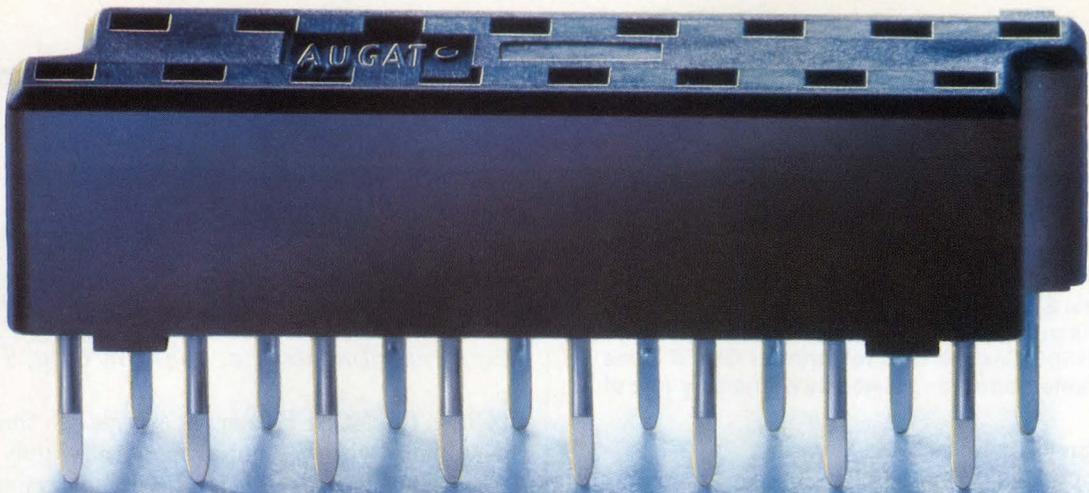


Fig 1—In this configuration, flip-flop IC_{1A} exhibits edge-sensitive set and clear controls: A low-to-high transition of XFER IN sets the device, and a high-to-low transition of XFER OUT clears it.

To Vote For This Design, Circle No 747



SPACE ACE

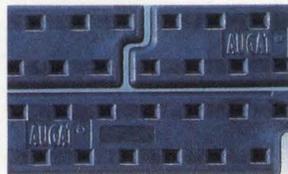
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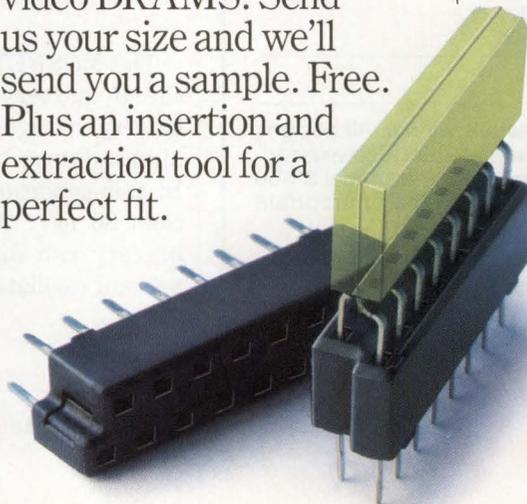
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Entry blank must accompany all entries. Design entered must be submitted exclusively to EDN, must be original with author(s), must not have been previously published (limited-distribution house organs excepted), and must have been constructed and tested.

Exclusive publishing rights remain with Cahners Publishing Co unless entry is returned to author or editor gives written permission for publication elsewhere.

In submitting my entry, I agree to abide by the rules of the Design Ideas Program.

Signed _____

Date _____

Your vote determines this issue's winner. All designs published win \$75 cash. All issue winners receive an additional \$100 and become eligible for the annual \$1500 Grand Prize. **Vote now**, by circling the appropriate number on the reader inquiry card.

ISSUE WINNER

The winning Design Idea for the October 1, 1987, issue is entitled "V/I converter has zero I_B error," submitted by Roberto Burani and Giovanni Stocchino of FATME SpA (Rome, Italy).

MOSFET switches memory-supply current

Steve Mowry

Texas Instruments Inc, Johnson City, TN

In Fig 1, the MOSFET serves as a switch that connects the memory with V_{CC} only when that supply voltage is present. The battery B_1 supplies standby current to the memory when V_{CC} falls below the battery voltage.

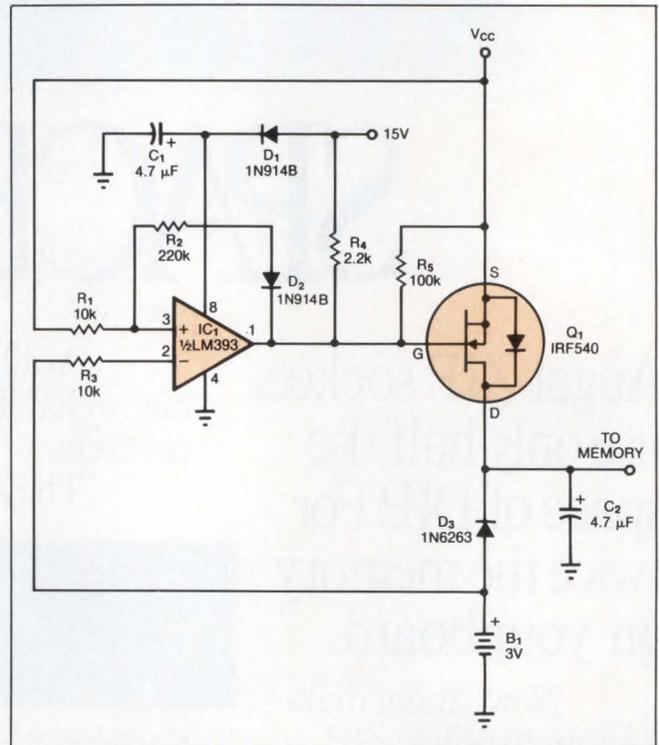


Fig 1—This circuit connects V_{CC} to memory when voltage is present; Q_1 can pass 1A while dropping less than 80 mV. The circuit provides battery backup when V_{CC} is not present.

The MOSFET Q_1 is off (open) when V_{CC} is less than the B_1 battery voltage. When V_{CC} rises above the battery voltage, the output of comparator IC_1 switches high and turns on Q_1 for operation in the inverted mode. In this condition, Q_1 can pass 1A while dropping less than 80 mV. As V_{CC} drops, Q_1 turns off before the battery can discharge. The components R_2 and D_2 prevent oscillation by adding hysteresis to the comparator.

EDN

To Vote For This Design, Circle No 748

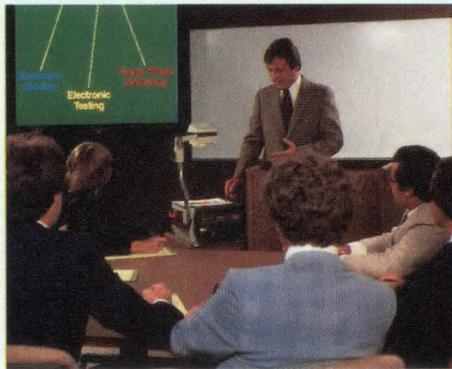


**Discover
Fluoronics Resources**

Fluorinert™ Liquids—products that power Fluoronics Resources

*Fluoronics Resources:

An exclusive 3M combination of innovative products backed by research and development, manufacturing expertise, technical data and service assistance built on more than 35 years' experience of pioneering in fluorochemistry.



3M has had a whole generation of experience in the development, manufacture and refinement of perfluorinated liquids. We first introduced these versatile liquids to electronics design, testing and production professionals in the fifties. Since then, Fluorinert Liquids have become the mainstays in electronic cooling, high reliability testing and vapor phase soldering.

Fluorinert Liquids, used as a direct contact heat transfer medium, offer a range of physical properties that make them particularly suitable for electronic uses. They are non-polar and exhibit no solvent action. They are colorless, low in toxicity, non-flammable and offer exceptionally high dielectric strength plus thermal and chemical stability. Most important, they have almost no chemical reactivity and they evaporate without leaving a residue on parts.

Buy the numbers

Our FC™ numbers — FC-40, FC-70, FC-77, etc. — are used to identify Fluorinert Liquids that offer certain physical characteristics to meet specific application needs. These FC numbers are solely 3M designations for various fluorochemical products.

Fluorinert Liquids are being used cost-effectively in cooling, high reliability testing and vapor phase soldering operations. When you are interested in applying these versatile liquids in your own production, 3M can provide an abundance of technical information and support.

Technical assistance: the main benefit of Fluoronics Resources

3M offers prompt assistance to help you solve many production and testing problems. We provide comprehensive technical recommendations for specific fluids. We consult with you on the proper application equipment and help you evaluate production methods and results. Our service bulletins bring you up to date on the most recent advances in vapor phase soldering and high reliability testing. Ask us about 3M's audiovisual materials and on-site application training seminars.

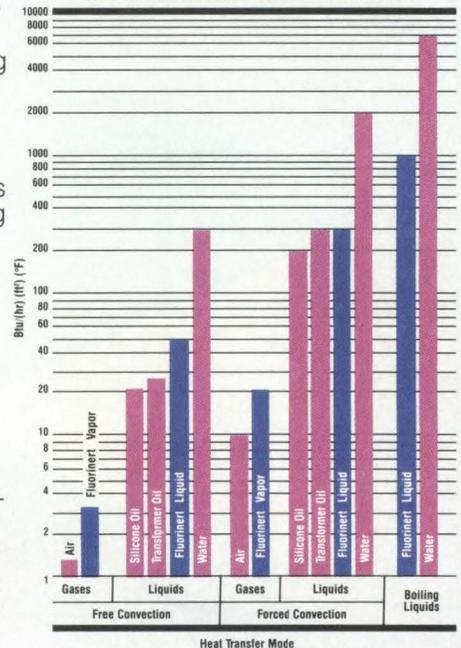
Discover Fluorinert™ Liquids' heat transfer capability

What are your needs? A precise degree of temperature control? Fast, uniform heat transfer? High dielectric strength? Fluorinert Liquids offer the broad range of physical characteristics required in most applications.

Fluorinert Liquids are an effective direct contact heat transfer medium whether used in a liquid or vapor state. Their unique properties enable you to use them in contact with sensitive components and substrates.

Major differences between the various products in the Fluorinert Liquids family can be seen in their boiling points. These can range from 56°C to 253°C. Should you need products with intermediate boiling temperatures, the 3M staff will work with you to fashion a product especially for your needs. It's an example of how 3M's Fluoronics Resources provide you with "customized" service to solve special problems.

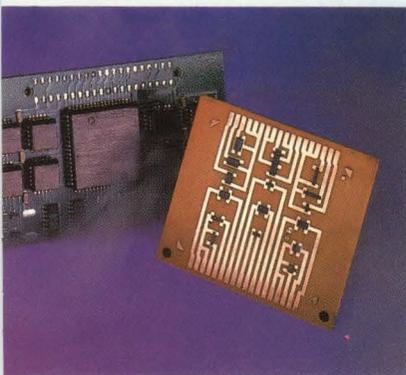
COMPARATIVE HEAT TRANSFER COEFFICIENTS



Fluorinert™ Liquids achieve accurate high reliability testing

It's a small world you work in. Where time ticks in nanoseconds and dimension is measured in Angstrom units. And as circuitry becomes more complex, a greater demand is placed on testing capability — not only in speed, but in higher reliability and accuracy.

Fluorinert Liquids meet those requirements by providing a controlled temperature environment and a high degree of electrical protection. They offer maximum compatibility between



the heat transfer medium and the device under test. Fluorinert Liquids reduce testing costs by reducing testing time substantially. They do this by rapidly reaching test temperature and providing precise and uniform temperature control. You'll minimize the number of faulty units by detecting defects before they become rejects.

These liquids provide cost-effective tests such as gross leak, thermal shock, liquid burn-in, ceramic crack detection, electrical environmental, temperature calibration and failure analysis/short detection.

Fluorinert Liquids are specified in the MIL-STD's for thermal shock and gross leak testing.

Discover higher yields in vapor phase soldering

Fluorinert Liquids have been the industry's fluid of choice since the vapor phase reflow soldering (VPS) process was introduced in 1975. There are a number of good reasons for this universal acceptance. VPS with Fluorinert Liquids produces highly reliable solder joints. The system reduces reject rates, increases production, and lowers production costs. With Fluorinert Liquids, you can be assured that your products will never be exposed to a temperature higher than the selected liquid's boiling point. (See above)

You'll avoid those problems usually associated with other systems — shadowing, uneven heating, and overheating. The liquids are non-flammable. Their low surface tension helps them evaporate quickly from the work pieces without leaving a residue.

VPS with Fluorinert Liquids is especially suited for boards with high mass or complex geometries. The liquid vapors completely surround the assembly and penetrate remote recesses to heat all surfaces evenly. The vapors are 15 to 20 times heavier than air so they can be contained easily within the work area. The system offers an oxygen-free, non-corrosive environment to minimize rejects from oxidation contamination.

Some typical applications using Fluorinert Liquids in VPS include surface mounted leaded or leadless components, through-hole leads and wire-wrap pins, lead frame attachment, reflow of electroplated solder or tin and miscellaneous metal joining.

VPS SELECTION GUIDE

Fluorinert Liquid	Boiling Point	Typical Solders
FC-43	174°C/345°F	70 Sn/18 Pb/12 In 100 In 58 Sn/42 In 58 Bi/42 Sn
FC-70, FC-5311 FC-5312	215°C/419°F	63 Sn/37 Pb 60 Sn/40 Pb 62 Sn/36 Pb/2 Ag
FC-71	253°C/487°F	100 Sn 95 Sn/5 Ag 60 Pb/40 Sn

Discover the unique cooling benefits of Fluorinert™ Liquids

As the package size decreases, your need for more efficient heat dissipation increases in proportion. 3M Fluorinert Liquids are very efficient as a direct contact heat transfer medium, with the added advantage of having the high dielectric characteristics needed to meet stringent demands of the diversified electronics industry. We offer 11 liquids with boiling points that range from 56°C to 253°C.

These stable liquids allow you to maximize power density and miniaturize your package. Yet they reduce failure rates and increase reliability.

Fluorinert Liquids are used in such demanding applications as:

- Radar transmitters • Power supplies
- High voltage transformers • Lasers
- Radar klystrons • Computer modules
- Computer memories • Fuel cells

Typical properties of Fluorinert Liquids used in cooling are:

Fluorinert Liquid FC-77 (English Units)	Liquid		Vapor
	Room Temp. (77°F)	Boiling Point (207°F)	Boiling Point 207°F @/ATM
Density lb./ft. ³	111	100	0.85
Thermal Conductivity Btu/(hr) (ft. ²) (°F/ft)	0.037	0.033	0.008
Specific Heat Btu/(lb.) (°F)	0.25	0.28	0.23
Viscosity c.p.	1.42	0.46	0.02
Coefficient of Thermal Expansion (ft. ³ /(ft. ³) (°F)	0.0008	0.0009	0.0015

Discover heating/curing with Fluorinert™ Liquids

Because they maintain their vapor temperature with absolute precision, Fluorinert Liquids can be used in many heating and/or curing operations. They serve as heat transfer media in solder mask and polymer thick film applications and for polymer processing. The non-corrosive vapors will not support oxidation. Ideal where solvent flash-off is a problem.

THERMAL SHOCK TEST CONDITIONS

Military Standard 883-1011			Military Approved Fluorinert Liquids	
Test Condition	Hot Test Step 1	Cold Test Step 2	Hot Test Step 1	Cold Test Step 2
A	100°C	-0°C	Water, FC-40	Water FC-40, FC-77
B	125°C	-55°C	FC-40, FC-70, FC-5311	FC-77
C	150°C	-65°C	FC-40, FC-70, FC-5311	FC-77
D	200°C	-65°C	FC-70, FC-5311	FC-77
E	150°C	-195°C	FC-40, FC-70, FC-5311	Liq. N ₂
F	200°C	-195°C	FC-70, FC-5311	Liq. N ₂

GROSS LEAK TEST CONDITIONS

Military Standards	Military Approved Fluorinert Liquids		
	Indicator Fluids	Detector Fluids	Absorption Fluids
MIL-STD 883-1014	FC-40, FC-43	FC-72, FC-84	Do not apply
MIL-STD 750-1071	FC-40, FC-43	FC-72, FC-84	FC-43, FC-75, FC-77
MIL-STD 202-112	FC-40, FC-43	FC-72, FC-84	Do not apply

Discover Fluoronics Resources

3M presents a unique short course in the use of Fluorinet™ Liquids for the electronics industry.

3M is now offering a series of "Applied Fluoronics" tapes demonstrating how Fluorinet Liquids are used in a number of applications. See first hand how these remarkable products can improve overall electronic production.

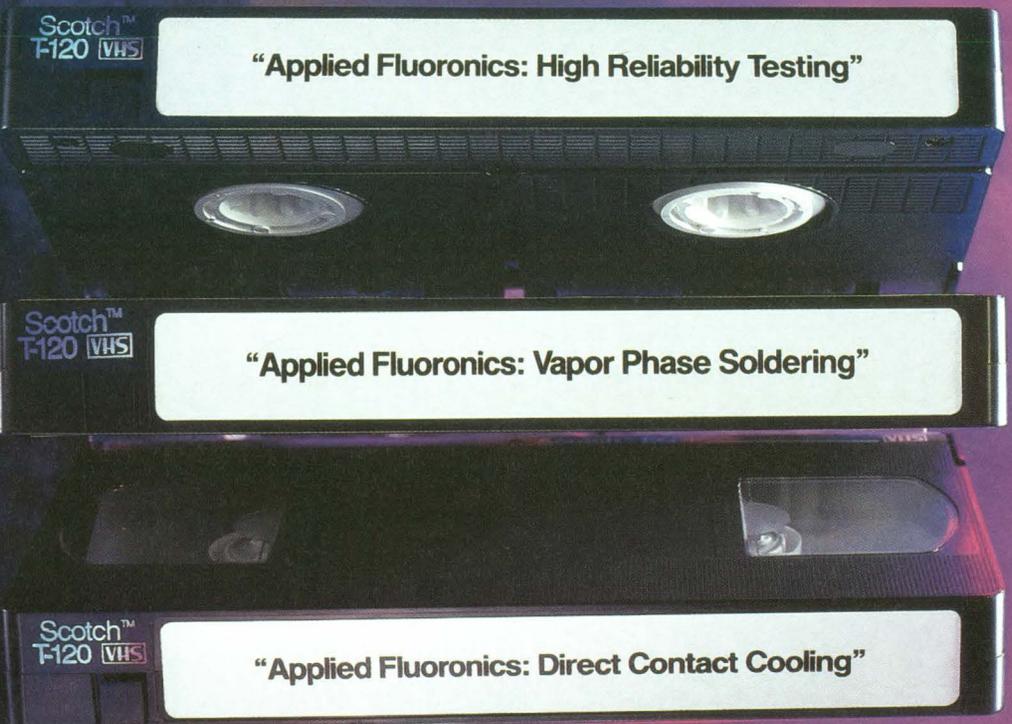
Three cassettes are available:

1. "Applied Fluoronics: High Reliability Testing"
2. "Applied Fluoronics: Vapor Phase Soldering"
3. "Applied Fluoronics: Direct Contact Cooling"

These informative VHS format tapes are available to qualified personnel in the electronics industry. Specify which cassette(s) you would like to view.

Write on your company letterhead, describing your general interest. Mail to: Fluoronics Resources, Industrial Chemical Products Division/3M, Building 223-6SE-04, 3M Center, St. Paul, MN 55144-1000.

For technical information or assistance on High Reliability Testing and Cooling, call 612/733-6282; for Vapor Condensation Heating assistance, call 612/733-7424.



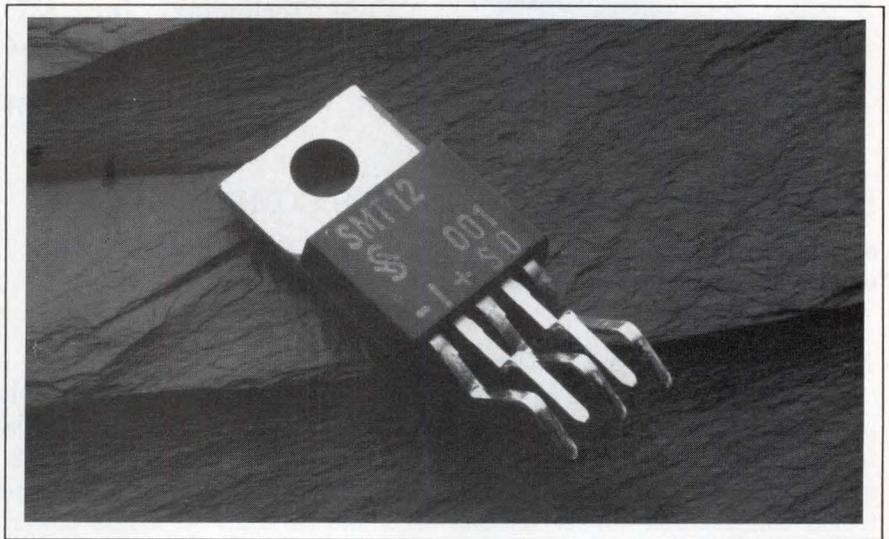
NEW PRODUCTS

INTEGRATED CIRCUITS

SMART SWITCH

- Has 35V/12A rating
- Features built-in diagnostic capability

Fabricated using SIPMOS technology, the BTS-412A is a smart MOS power switch that features built-in protection functions. SIPMOS technology integrates 5V-CMOS and high-voltage-CMOS structures with vertical power MOSFETs without using junction or dielectric isolation. Targeted at automotive and industrial applications, the device is fully protected against overloads, under-voltage, short circuits, and junction temperatures exceeding 150°C. Available in a TO-220 package, it operates to 35V and has a maximum load-current rating of 12A. In its off

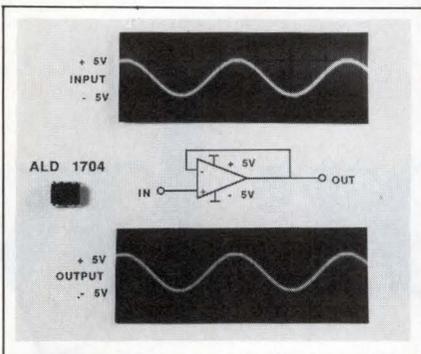


state, the device will block 45V at very low standby current consumption. \$6.25 (1000).

Siemens Components Inc, Power

Semiconductor Div, 2191 Laurelwood Rd, Santa Clara, CA 95054. Phone (408) 980-4545.

Circle No 351



offers four input offset-voltage grades: 10-mV 1704G, \$1.36; 4.5-mV 1704, \$1.51; 2-mV 1704B, \$2.57; and 0.9-mV 1704A, \$3.58 (100). A military ceramic DIP is available for all grades.

Advanced Linear Devices, 1030 West Maude Ave, Sunnyvale, CA 94086. Phone (408) 720-8737. TLX 510-100-6588.

Circle No 352

CMOS OP AMP

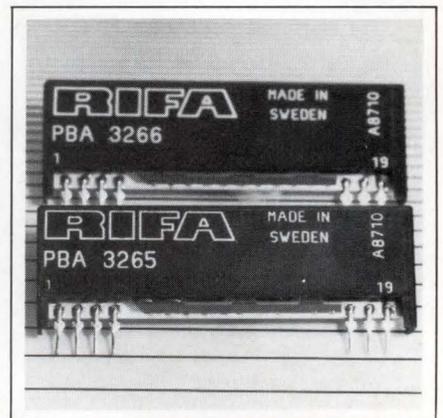
- Low-power alternative to J-FET op amps
- Has 5V/ μ sec slew rate

The ALD-1704 CMOS op amp provides a low-power and low-cost alternative to J-FET op amps. The device has a slew rate of 5V/ μ sec and a bandwidth of 2.1 MHz when operating from dual supplies of ± 3.25 to ± 6 V. Its power dissipation is 45 mW at a supply voltage of ± 5 V. The IC offers rail-to-rail input- and output-voltage ranges, and its output-current rating is 10 mA. The output is short-circuit protected to 15 mA. The manufacturer

DIGITAL FILTER

- Features 20-kHz cut-off frequency
- Has optional delay equalizer that corrects phase response

The PBA-3265 lowpass filter operates as a band-limiting, antialiasing filter in digital audio systems with 48- to 50-kHz sampling rates. The device's frequency response is stable to within 0.1 dB from dc to 20 kHz. Its stop-band attenuation is 80 dB min from 24 to 100 kHz. The PBA-3266 matching delay equalizer corrects the filter's phase response.



The resulting group-delay variation is constant within ± 30 μ sec for frequencies to 19 kHz. You can employ its built-in sin x/x compensation network to facilitate the use of the filter/equalizer combination as a reconstruction filter following a D/A converter. The sin x/x section is designed for a system that provides a 48-kHz sampling rate. Each circuit comes in a single-in-line package. PBA-3265, \$24.50; PBA-3266, \$29.50 (100).

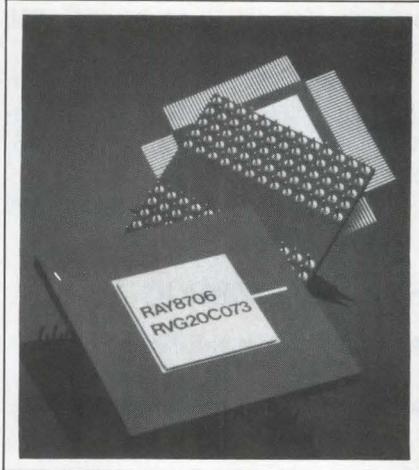
Rifa Inc, Box 3110, Greenwich, CT 06836. Phone (203) 625-7300.

Circle No 353

from 0 to 70°C and use ±5V supplies. They come in ceramic DIPs, plastic DIPs, and small outline packages. \$7.01 to \$8.47 (100).

Texas Instruments Inc, Semiconductor Group (SC-777), Box 809066, Dallas, TX 75380. Phone (800) 232-3200.

Circle No 355



CMOS GATE ARRAYS

- Have unloaded inverter delay of 0.4 nsec
- Feature 1.25-µm technology

RVG CMOS gate arrays incorporate rad hardening and have 5670 to 20,440 2-input gates. Representative arrays include the 5670-gate RVG5, the 10,360-gate RVG10, the 14,640-gate RVG15, and the 20,440-gate RVG20. The 2-input NAND gate has a delay of 0.95 nsec with a fan-out of 2; its typical power dissipation is only 8 µW/MHz. The gate

arrays feature symmetrical switching and edge delays, operate at 250-MHz flip-flop frequencies, and are TTL/CMOS compatible. Each I/O interface includes protection circuitry for a 2000V electrostatic discharge and is user programmable as an input, output, or bidirectional signal connection. You can select from an extensive macrocell library of SSI, MSI, and LSI functions.

Military and commercial NRE (non-recurring engineering) costs, from \$35,000; military devices, from \$150 (1000/year); commercial devices, from \$65 (10,000/year).

Raytheon Co, Semiconductor Div, 350 Ellis St, Mountain View, CA 94043. Phone (415) 968-9211.

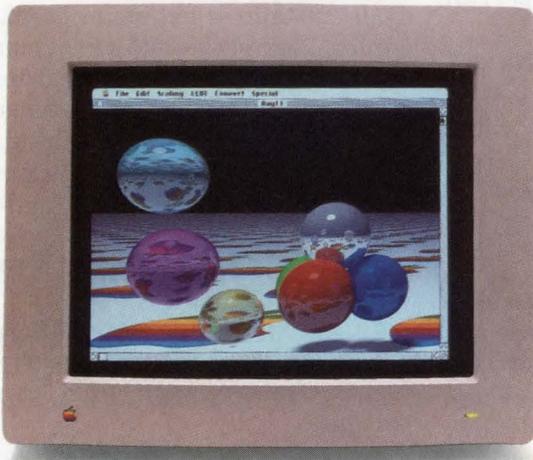
Circle No 356

CODEC/FILTER

- Is compatible with AT&T and CCITT telephone standards
- Features a low transmit idle-channel noise level

The M5913 CMOS codec/filter IC provides the A/D and D/A conversion and the transmit and receive filtering required to interface a full-duplex voice circuit to a time-division-multiplexed PCM digital telephone system. The device is compatible with AT&T's D3/D4 standard and with applicable

Brooktree®



Macintosh II. 640x480 resolution, displays 256 colors simultaneously from a 16.8 million color palette.

Bt453. Triple 8-bit 40 MHz RAMDAC with 256 color lookup table. Monolithic CMOS.

Brooktree Corporation, 9950 Barnes Canyon Road, San Diego, California 92121. 1-800-VIDEO IC or 1-800-422-9040, in California.

Apple® and Macintosh™ II are trademarks of Apple Computer Corporation.

CIRCLE NO 13

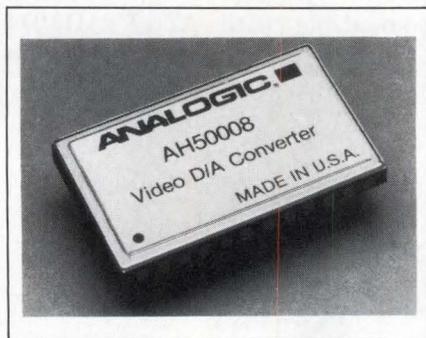
CCITT standards. It has a power-supply rejection ratio of -40 dB from dc to 150 kHz. You can operate the codec at either a fixed data-rate or in a variable data-rate mode. To ensure the integrity of the PCM highway, the unit contains power-on-reset circuitry and circuitry that permits detection of an interrupted clock. The device operates from $\pm 5V$ supplies and has a typical active power dissipation of 60 mW. Approximately \$6 (1000).

SGS Microelectronica SpA, Via C Olivetti 2, 20041 Agrate Brianza, Italy. Phone (039) 65551. TLX 330131.

Circle No 357

SGS Semiconductor Corp, 1000 E Bell Rd, Phoenix, AZ 85022. Phone (602) 867-6100. TLX 249976.

Circle No 358



8-BIT VIDEO DAC

- Accepts TTL inputs
- Provides 1V p-p output signal into 75 Ω

The AH50008 8-bit composite-video D/A converter serves both monochrome and color digital-display applications. The converter accepts 8-bit video data, as well as synchronizing and blanking commands, directly from TTL sources. The converter has RS170A- and RS343A-compatible outputs, which can provide a 1V p-p signal at a 90-MHz update rate into a 75 Ω coaxial cable and monitor. The output transitions are virtually glitch-free and require no additional processing. The device comes in a 24-pin hermetically sealed DIP and

operates from -55 to +100°C. \$50 (100).

Analogic Corp, Data Conversion Products, 360 Audubon Rd, Wakefield, MA 01880. Phone (617) 246-0300.

Circle No 359

SYNTHESIZER IC

- Allows direct synthesis of sine waves via a D/A converter
- Suited to fast frequency-hopping applications

The SP2001 is a digital frequency synthesizer that directly generates the 8-bit DAC code required to produce sine waves at frequencies between 5 kHz and 100 MHz. Because this method of generating sine waves eliminates the delays inherent in PLL synthesizers, the time it takes to hop between one frequency and another is affected only by the D/A converter's settling time; with a suitable D/A converter, you can achieve worst-case frequency-hop delays of about 17 nsec. This system also achieves close-to-carrier noise levels of -135 dBc/Hz. Fabricated in ECL technology, the unit requires -5.2 and -2V supplies. It comes in a 40-pin ceramic DIP. £375.

Plessey Semiconductors Ltd, Cheney Manor, Swindon, Wiltshire SN2 2QW, UK. Phone (0793) 36251. TLX 449637.

Circle No 360

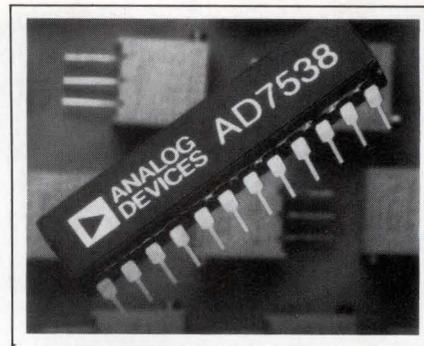
Plessey Semiconductors, 9 Parker, Irvine, CA 92718. Phone (714) 472-0303.

Circle No 361

CMOS DAC

- Provides 14-bit accuracy and resolution
- Is TTL/CMOS compatible

The AD7538 multiplying D/A converter provides 14-bit accuracy and resolution over its full temperature range. Its integral and differential nonlinearity are ± 2 and ± 4 LSB, respectively. Double-buffered data latches and μP compatibility allow



simultaneous updating in systems that use multiple DACs. Using standard chip-select and memory-write commands, the current-output DAC is parallel-loaded by a single 14-bit word. Applications include microprocessor-based control systems, digital audio, and precision servo control. You can obtain the device in a 24-pin plastic or ceramic DIP. \$10.50 to \$51.90 (100).

Analog Devices, Box 9106, Norwood, MA 02062. Phone (617) 329-4700. TWX 174059.

Circle No 362

16-DIODE ARRAY

- MIL-S-19500 qualified to JAN, JANTX, and JANTXV
- On qualified product list

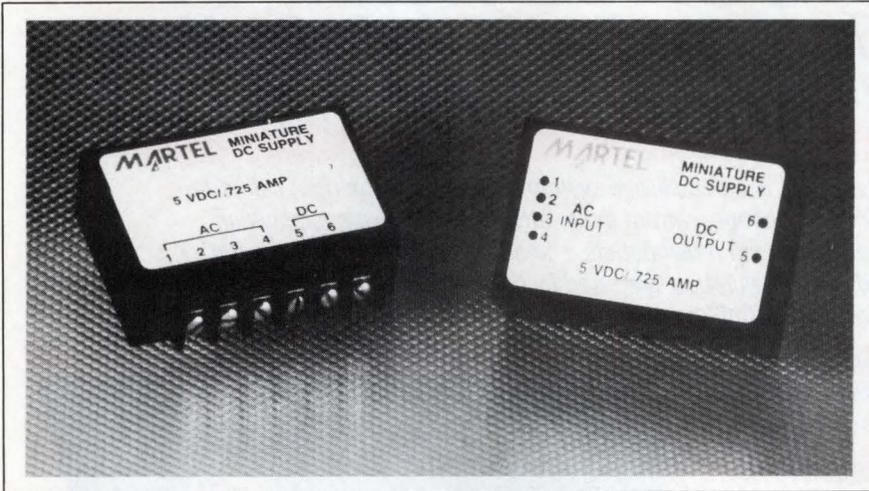
The 1N5772 16-diode array has eight common anodes and eight common cathodes brought out to two separate leads on a 10-lead flat pack. The other eight leads connect to the anode-cathode junctions of each of the eight series pairs. Each diode sustains a minimum breakdown voltage of 60V and a minimum current of 500 mA. Designed for high-speed military applications, the device meets the requirements of MIL-S-19500/474 and has typical switching speeds of less than 10 nsec. Its operating temperature-range is -55 to +150°C. JANTX version, \$21 (100).

Silicon General, 11861 Western Ave, Garden Grove, CA 92641. Phone (714) 898-8121. TWX 910-596-1804.

Circle No 363

NEW PRODUCTS

COMPONENTS & POWER SUPPLIES



POWER SUPPLIES

- Designed to meet UL and CSA standards
- MTBF rating exceeds 100,000 hours

Available in both pc-board and chassis-mount configurations, Series 3000 ac to dc power supplies measure 1×2×3 in. and provide a 0.7W/in³ power density. To achieve this high power density, the supply design employs an efficient semi-toroidal transformer that's matched with a proprietary, low-drop-out regulator. The supplies offer user-selectable input ranges of 105 to

125V ac and 210 to 250V ac and have outputs of 5V at 0.725A, 12V at 0.35A, and 24V at 0.175A. These miniature supplies feature line and load regulation of ±0.1%. Short-circuit and overvoltage protection are standard. The units are designed to meet UL and CSA standards for power supplies and have a MTBF rating of more than 100,000 hours. \$37 for pc-board version; \$42.95 for chassis-mount model (100).

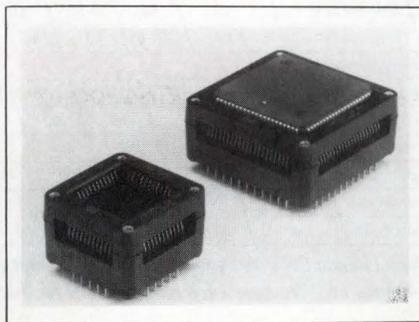
Martel Electronics, 27 Roulston Rd, Windham, NH 03087. Phone (603) 893-0886.

Circle No 364

SOCKETS

- Guided-entry and -alignment ribs ease device orientation
- Socket design provides more contact area at the leads

Designed for burn-in service, these sockets accommodate 44- and 84-pin plastic leaded-chip carrier (PLCC) devices. They have a locking mechanism that facilitates manual or automated loading and unloading, prevents damage to delicate leads, and insures positive lead contact. A simple push seats the PLCC firmly in the socket with an audible click. A second push ejects the device above

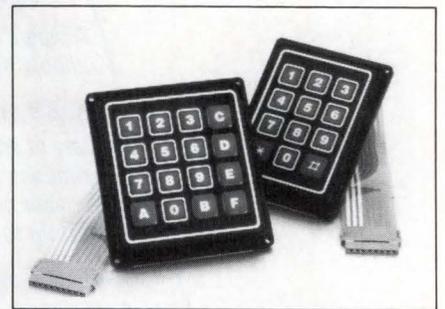


the socket edge for easy removal. Guided-entry and -alignment ribs ease the PLCC into proper orientation within the socket. An improved socket design provides more contact area at the top and sides of the leads to improve reliability. The sockets

feature quick visual polarization, and the side and bottom vents allow increased airflow for heat dissipation, as well as access for test probes. \$9.98 for the 44-pin unit; \$15.12 for the 84-pin version (1000).

3M, Dept EP87-109, Box 2963, Austin, TX 78769. Phone (512) 834-1803.

Circle No 365



MEMBRANE KEYPADS

- 2- and 5-million-cycle lifetimes
- Feature sealed splash-proof switches

The Series 4000 membrane keypads are available in 4×4 and 3×4 arrays with either embossed, detented or flat nontactile keys. Sealed splash-proof switches, a built-in static shield, and chemically resistant graphics overlays are standard. The 4×4 arrays have hexadecimal graphics; the 3×4 arrays have standard telephone keypad graphics. The graphics are mounted on a rigid base, which has a UL 94V-0 rating, and are available in red, black, and white. The circuit configuration is an X-Y matrix output. The keypads terminate via a 6-in. flex tail that includes male and female connectors. The lifetime measures 2 million cycles for detent-type pads and 5 million cycles for nondetent-type units. \$5.53 (1000). Delivery, four to five weeks ARO.

C&K Components Inc, 15 Riverdale Ave, Newton, MA 02158. Phone (617) 964-6400.

Circle No 366

LITHIUM POWER SOURCE NEEDS?

Electrochem Provides the Perfect Match Whatever Your Application

CELlection™ is our exclusive system for matching the right cell (size, termination, voltage, current drain, etc.) to your specific application. You provide us with a few details... and we do all the rest. You get a detailed recommendation, prepared by our expert Applications Engineering Staff. Call or write for your CELlection Starter Kit today.

Programmable Controllers

A single lithium cell provides reliable memory back-up.

CMOS Memory Back-Up

Variety of sizes and terminations means you get the right cell for your needs. Certain cells last up to 10 years.

Downhole Equipment

Electrochem's exclusive Performaxx cell packs specifically designed to power test and measurement instrumentation used in oil exploration and development market. Rugged, safe... packs operate well from 0°C - 150°C.

Medical Devices

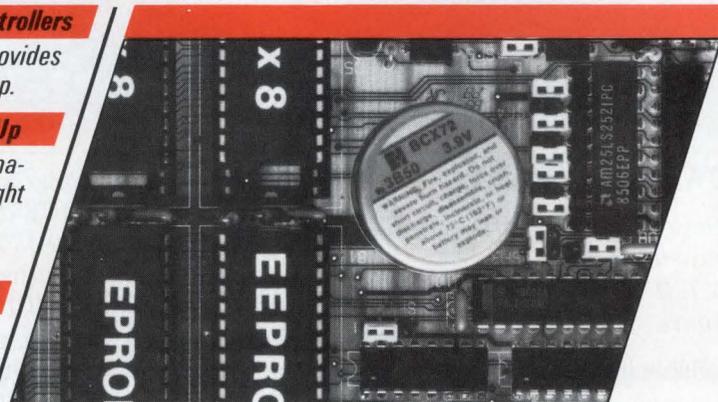
When you have to be sure, rely on Electrochem Quality Lithium power sources.

Metering, Security and Alarm Devices

Minimum space... maximum power... long life... three very good reasons to specify lithium batteries.

Your Next Application

Don't trouble yourself over what cell to specify. Let CELlection solve your design problems for you.



Electrochem Lithium Cell provides memory back-up.

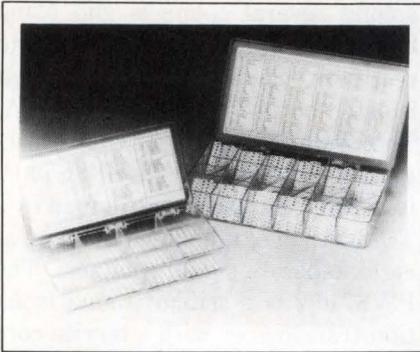
	CELL CHEMISTRIES							
	Carbon Zinc	Alkaline	Mercury	Li/SO ₂	Li/SOCl ₂	Li/BCX	Li/CSC*	Li/CuO
Construction								
Anode	Zn	Zn	Zn	Li	Li	Li	Li	Li
Cathode	MnO ₂	MnO ₂	HgO	SO ₂	SOCl ₂	SOCl ₂ /BrCl	SO ₂ Cl ₂ /Cl ₂	CuO
Electrolyte	NH ₄ Cl/ZnCl ₂	KOH	KOH	LiBr	LiAlCl ₄	LiAlCl ₄	LiAlCl ₄	var.
Voltage								
Open Circuit V	1.6	1.6	1.35	3.0	3.6	3.9	3.9	2.4V
Typical Load V	1.4-1.0	1.4-1.0	1.3	2.8-2.7	3.5-3.4	3.7-3.5	3.8-3.5	1.5V
Energy Density								
Ah/cm ³	0.08	0.13	0.23	0.18	0.20	0.26	0.23	0.35
Ah/kg	47	55	76	100	92	120	110	180
Wh/cm ³	0.1	0.2	0.4	0.5	0.8	1.1	0.9	0.5
Wh/kg	66	77	100	300	400	440	410	300
D Cell Capacity Ah	2	4	10	8	10	14	12	20
D Cell Capacity Wh	3	6	13	22	35	50	43	30

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0.18Ω for the bottom-side n-channel devices and 0.3Ω for the top-side p-channel devices, providing designers 6.1A/leg at 45°C. The sensing circuits on the HexSense dice are formed by isolating a number of cells on the HexFET die from the main-source metallization. Because each cell in the HexFET matrix is parallel and identical, sampling cur-

rent in one or several cells gives a scaled indication of the main current. The units are housed in low-profile (0.5-in.), 11-pin single-in-line packages. \$8.65 (1000). Delivery, four to eight weeks ARO.

International Rectifier, 233 Kansas St, El Segundo, CA 90245. Phone (213) 607-8939.

Circle No 368

CHIP KITS

- Ease problems in prototyping surface-mount circuits
- Include a complete selection of resistor and capacitor chips

The CR-1 chip resistor and CC-1 chip capacitor kits are designed to eliminate problems associated with prototyping surface-mount circuits. The CR-1 includes 1540 pieces composed of 10 chips of every 5% value from 10Ω to 10 MΩ. The 0805-size chips cover values ranging to 3.3 MΩ and have a 100-mW rating; above 3.3 MΩ, the 1206-size chips have a 125-mW rating. The CC-1 kit contains 365 pieces (both 0805 and 1206 sizes) composed of five chip capacitors of every 10% value between 1 pF and 0.33 μF. The kit contains NPO- (to 680 pF), X7R- (to 0.1 μF), and Z5U- (above 0.1 μF) type chips. \$49.95.

Communications Specialists Inc., 426 W Taft Ave, Orange, CA 92665. Phone (800) 854-0547; in CA, (714) 998-3021.

Circle No 367

MOSFET MODULES

- Current-sensing dice allow nearly lossless feedback circuits
- Electrically isolated bases allow direct mounting to heat sinks

CPY213E MOSFET modules provide nearly lossless feedback circuit designs. They include two n-channel HexSense die and two fast-recovery diodes paralleling two p-channel HexFET die in an H-bridge configuration. The on-resistance measures

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CF60-H	24	14-22	26-37.5	60-120
CF80-T	12	32-46	27-37	100-230
CF80-H	24	32-46	27-37	65-140
CF92-T	12	30-48	28-34	90-190
CF92-H	24	30-48	28-34	50-100
CF120-T	12	49-78	32-40	110-330
CF120-H	24	49-78	32-40	80-200

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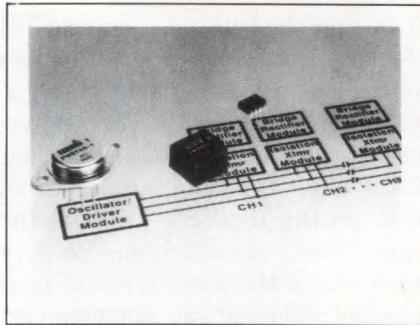
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CONVERTER SYSTEM

- Provides multiple channels of 7 to 20V dc at ± 30 mA
- Isolation guaranteed to 1500V ac

The PWS740 system provides multiple channels of 7 to 20V dc bipolar outputs with isolation 100% tested and guaranteed to 1500V ac. By sharing a common power driver



among several channels and using board-mounted transformers and rectifiers, you can generate bipolar isolated output as high as ± 30 mA. The system consists of three integrated components. The PWS740-1 is a 400-kHz oscillator/driver in a TO-3 package; it handles as many as eight separate signal channels. The PWS740-2 is a trifilar-wound isolation transformer with a ferrite core and is encapsulated in a compact plastic package. The PWS740-3 is a high-speed rectifier bridge housed in a plastic 8-pin DIP. When you're using two or more PWS740-1 modules, a sync pin synchronizes operation and eliminates troublesome beat-frequency switching noise. A TTL-compatible enable pin permits output shutdown. PWS740-1, \$12.75; PWS740-2, \$2.50; PWS740-3, \$1.25 (100).

Burr-Brown Corp, Box 11400, Tucson, AZ 85734. Phone (602) 746-1111. TLX 666491.

Circle No 369

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ACTUAL SIZE

NDK 1300 Series Compact Crystal Clock Oscillators

NDK's 1300 Series offers the widest range of CMOS- and TTL-compatible compact oscillators available. Frequencies from 28 kHz to 70 MHz with enable/disable std and dual-frequency output as an option. All in rugged, space-saving, half-size packages that are perfect for high density pc-board applications.

NDK 1300 Series Features

- Broadest range of available frequencies — 28 kHz to 70 MHz
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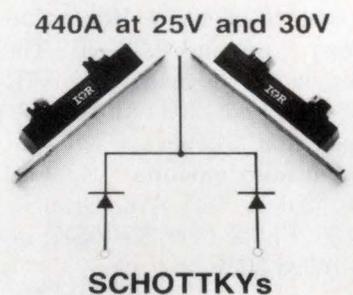
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RECTIFIER MODULES

- Handle peak reverse voltages of 25 and 30V
- Operating range of -65 to $+150^{\circ}\text{C}$

The 440CNQ025/030 center-tapped Schottky rectifier modules handle maximum working peak reverse voltages of 25 and 30V, respectively, at currents as high as 220A/leg. The modules have a maximum peak forward voltage drop/leg of 0.59V at 25°C , a maximum peak 1-cycle non-

Large, angled marking surfaces for easy labeling and readability.

Non-burning, heat and humidity-resistant insulating material.

Coding system protects against misconnection without loss of poles.

Available in 2 to 24-pin vertical and horizontal configurations.

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zinc-plated steel clamping mechanism for a secure connection.

The glass-filled polyester insulating material of BLA/SLA connectors is non-burning (UL94V0) and heat and humidity resistant to maintain pin-to-pin spacing in adverse operating environments.

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Weidmüller BLA/SLA connectors are available in 2 to 24-pole modules. They come in



Doubleheader version available for increased wiring density.

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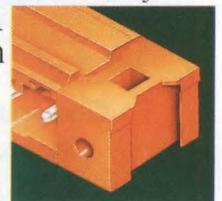
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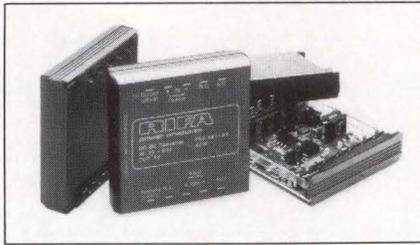
Write Weidmüller, Inc., 821 Southlake Boulevard, Richmond, Virginia 23236. Phone (804) 794-2877. Telex: 828376.

CIRCLE NO 111

repetitive surge-current rating of 4000A, and a maximum continuous peak reverse current/leg of 40 mA. The maximum capacitance/leg is 9200 pF, and dV/dT equals 1000 V/ μ sec. The operating range spans -65 to +150°C. 440CNQ025, \$26.13; 440CNQ030, \$28.14 (100). Delivery, eight to 10 weeks ARO.

International Rectifier, 233 Kansas St, El Segundo, CA 90245. Phone (213) 607-8837.

Circle No 370



The package's 0.78-in. height above the pc board allows mounting on boards that plug into racks on a 6TE (1.2-in.) spacing. The converter accepts dc input voltages in the range of 39 to 64V and has input-to-output isolation to 500V dc. Its predicted MTBF is more than 200 years at an ambient temperature of 45°C. The operating range is -45 to +65°C, but you can obtain another version, the PKA-4411-PI, which has an integral heat sink that extends its operating temperature range to 85°C. The extended temperature range version also has a 3x3-in. footprint, but its height is 1.39 in. A chassis-mount version with fast-on

terminals is also available. Approximately Swedish Krona 811 (100).

Rifa AB, Power Products Div, 16381 Stockholm, Sweden. Phone (8) 757-5000. TLX 10948.

Circle No 371

Rifa Inc, Greenwich Office Park 3, Greenwich, CT 06836. Phone (203) 625-7300.

Circle No 372

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- Provides 40W output power in a pc-board-mountable package
- Features 500V input-to-output isolation

The PKA 4411 PIL isolated dc/dc converter provides a 5V/8A output from a pc-board-mountable package that measures only 3x3x0.78 in.

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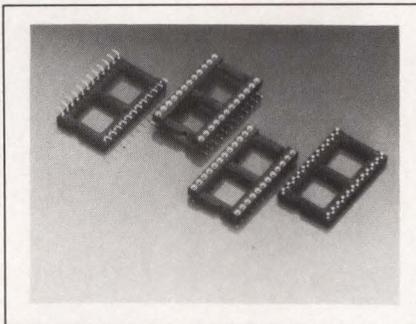
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screw-machined brass with tin plating over copper and nickel. Types 105 and 117, with 28 pins and tin plating, cost \$1.75 and \$1.65 (100), respectively. Delivery, four to six weeks ARO.

IEE Inc, Component Products Div, 7740 Lemona Ave, Van Nuys, CA 91409. Phone (818) 787-0311. TLX 4720556.

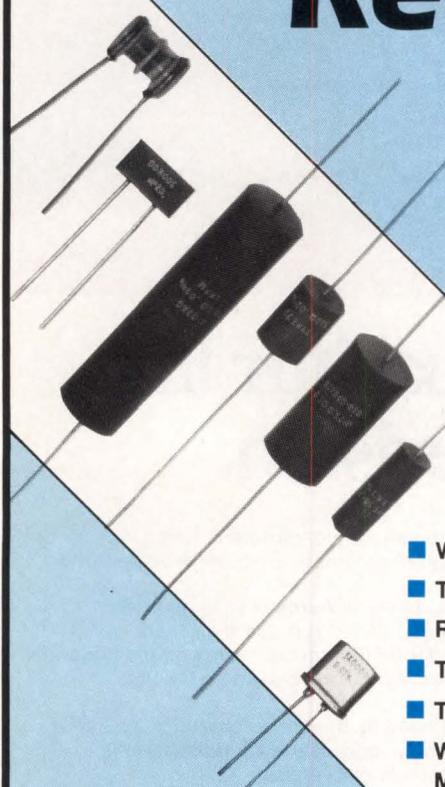
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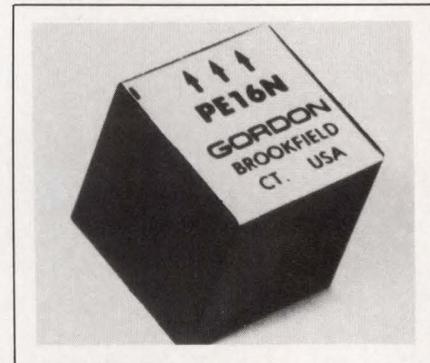
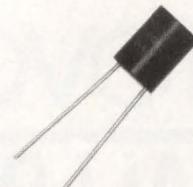
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- Designed to handle industrial environments

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Gordon Products Inc, 67 Del Mar Dr, Brookfield, CT 06804. Phone (203) 775-4501.

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The PCScan 2000 desktop scanner interfaces with the IBM PC, PC/AT, PC/XT, PS/2, and compatibles or with an Apple Macintosh Plus, SE, or Macintosh II computer. The device performs 8-bit gray-scale scanning and thus recognizes 256 shades of gray. You can set its resolution from 38 to 300 pixels/in. It typically takes 9.4 sec to scan a page. You can edge feed documents from 3.5×3.5 to 8½×14 in. into a front entry port; an optional automatic feeder with 35-sheet capacity handles paper sizes from 6×6 to 8½×14 in. A SCSI interface connects the scanner to external devices. Two scanner models are available: one with and one without hardware that supports the vendor's optical recognition (OCR) soft-

ware. Model with OCR hardware, \$2195.

DEST Corp, 1201 Cadillac Ct, Milpitas, CA 95035. Phone (408) 946-7100. TLX 299823.

Circle No 375



3½-IN. DISK DRIVES

- Have as much as 200M bytes of storage
- Support SCSI interface command set

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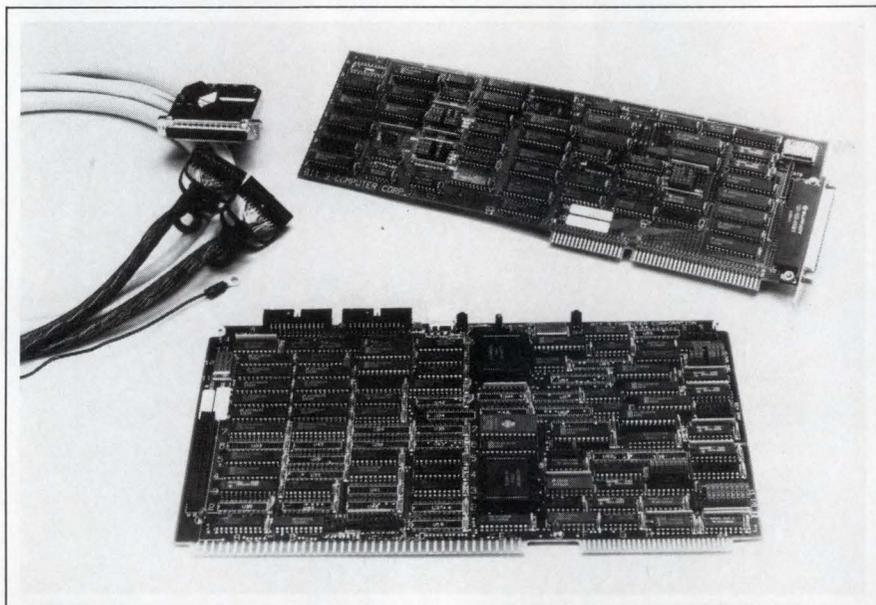
Control Data Corp, Box 0, Minneapolis, MN 55440. Phone (612) 853-5795.

Circle No 376

BUS ADAPTER

- Makes an IBM PC/AT the bus master of Multibus I
- Gives IBM PC/AT access to Multibus I devices

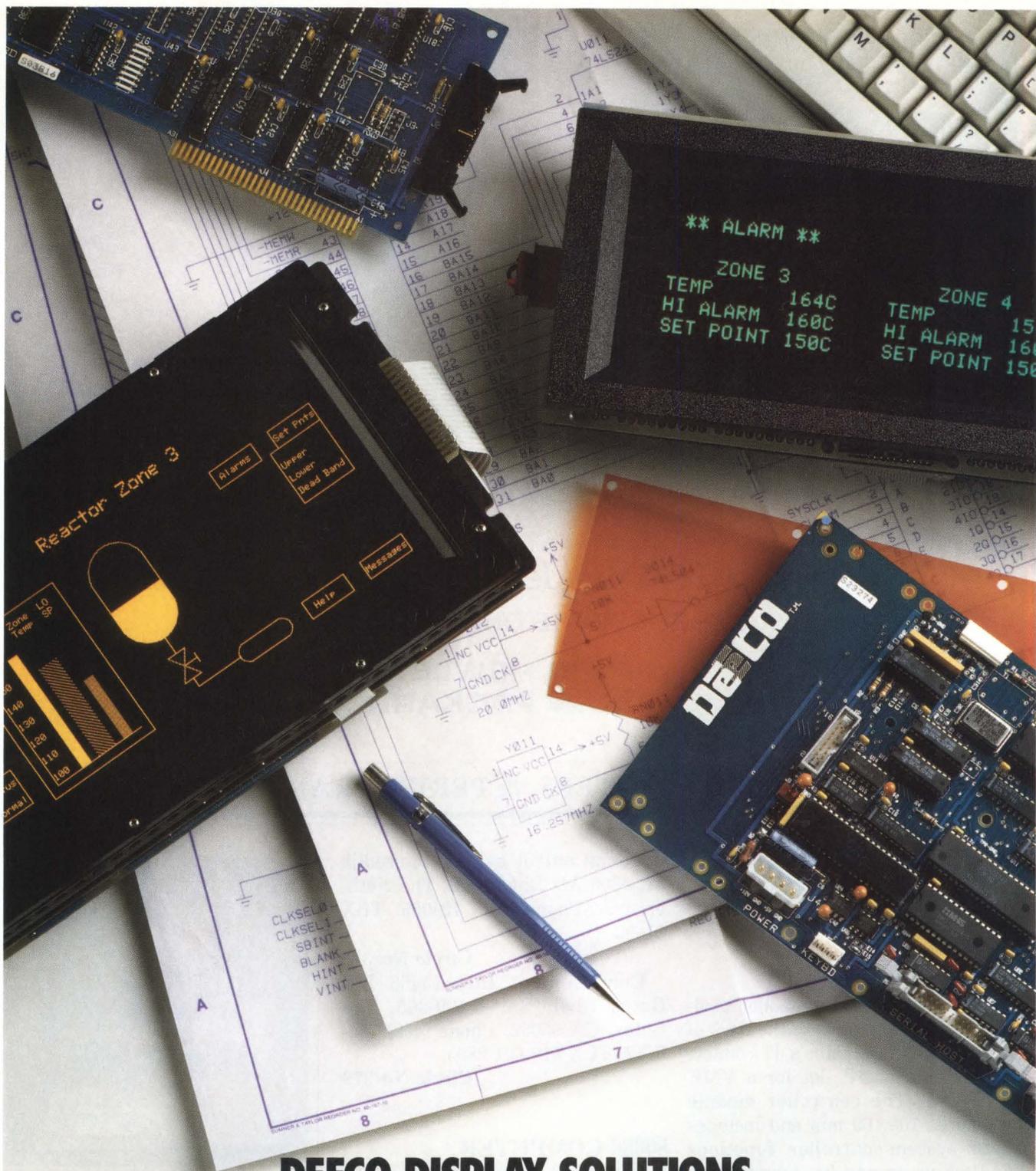
The 404 IBM PC/AT Multibus I Adapter makes an IBM PC/AT function as a processor on Multibus I. The adapter permits the IBM PC/AT to serve as the bus master in Multibus applications and lets you use the wide variety of high-performance devices compatible with Multibus I. The product consists of two printed circuit cards. One card fits inside the PC/AT, whereas the other fits inside a Multibus card cage. The two cards are connected by an EMI-shielded cable. As much as 15M bytes of Multibus memory can serve as PC/AT memory. The 16M bytes of Multibus address



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Bit3, 8120 Penn Ave S, Minneapolis, MN 55431. Phone (612) 881-6955.

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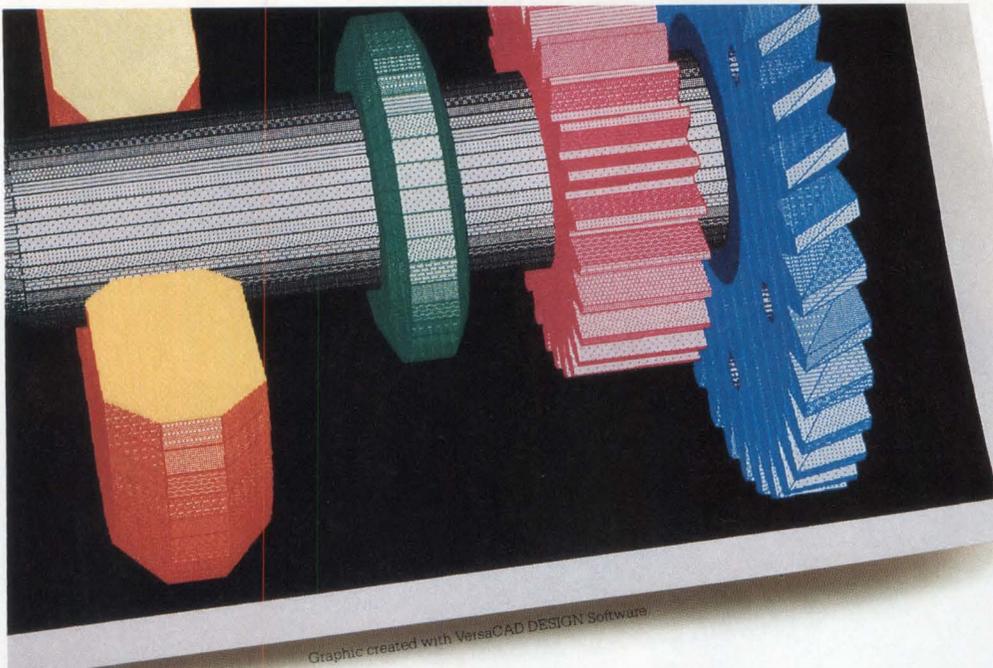
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COMPUTERS & PERIPHERALS

VME BUS CONTROLLER

- Frees an extra board slot in a VME Bus system
- Includes controller functions and termination networks

The CC-101 system-controller module, which you plug onto the back of a VME Bus backplane's J1 connector, frees a board slot for a VME Bus card. The controller module measures 100×60 mm and includes both system-controller functions and active or passive termination networks. The system-controller functions include generation of the 16-MHz VME Bus system clock and 2.9-MHz serial clock; a 4-level priority or round-robin bus arbiter; bus time-out generator; and power-on or switch-activated reset operations. The board consumes 800 mA with active bus-termination networks and 1.7A with passive termination networks. It has an operating range of 0 to 70°C. \$280.

CompControl bv, Stratumsedijk 31, 5600 AD Eindhoven, The Netherlands. Phone (040) 124955. TLX 51603.

Circle No 378

CompControl Inc, 15466 Los Gatos Blvd, Suite 109-365, Los Gatos, CA 95032. Phone (408) 356-3817. TLX 510-601-2895.

Circle No 379

80386 COMPUTER

- Uses IBM's Microchannel bus
- Is compatible with the PC/AT

The Premium/386 20-MHz 80386-based personal computer provides the multitasking benefits of IBM's Microchannel architecture and yet also features IBM PC/AT hardware and software compatibility. It is a single-user, multitasking machine suitable for CPU- and memory-intensive applications. You can obtain four models, all of which have seven



expansion slots, one 32-bit dedicated memory slot, three 16-bit PC/AT-compatible SmartSlots, one 8/16-bit standard PC/AT slot, and two 8-bit standard PC/XT slots. The SmartSlot architecture has three components: a dedicated 32-bit pathway from the processor to memory, a feature bus, and an arbitration bus. You can load coprocessors for graphics, communications, and disk control into the three

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CIRCLE NO 19

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COMPUTERS & PERIPHERALS

SmartSlots. Other features of the various models are memory capacities to 13M bytes, three user-selectable speeds, a disk controller, and hard disks of 40M- to 150M-byte capacity. A 1.2M-byte drive, a keyboard of 101 keys, two RS-232C ports, and one parallel port are standard on all the machines. The systems can each support as many as four drives. \$4695 to \$8995.

AST Research Inc, 2121 Alton Ave, Irvine, CA 92714. Phone (714) 863-1333.

Circle No 380

OPTICAL-DISK DRIVE

- Provides 810M bytes of storage capacity
- Runs Winchester-drive software

The Model 810 optical-disk drive emulates magnetic-disk drives. The drive can run, without modification, software and operating systems de-

veloped for Winchester devices. It provides 810M bytes of storage capacity on a 5¼-in. removable cartridge. The double-sided cartridge conforms to ANSI standards. The drive's dual- μ P architecture achieves 175-msec access times and data-transfer rates to 2.78M bps. The device has a SCSI host interface and is compatible with standard SCSI host adapters. A multitiered error-correction scheme provides a 1×10^{-12} corrected bit-error rate after error checking and correction (ECC) and a 1×10^{-16} undetected bit-error rate after ECC and cyclic redundancy checking (CRC). If you use the drive with an IBM PC/AT, you can employ system software that removes the 32M-byte disk-size limitation of DOS; this software occupies less than 10k bytes of host memory. In addition to the Winchester emulation mode, the drive also supports the write-once, read-many (WORM) mode. Single-drive

system, \$4995. Double-sided, 810M-byte cartridge, \$189. Delivery, 60 days ARO.

LaserDrive Ltd, 1101 Space Park Dr, Santa Clara, CA 95054. Phone (408) 970-3600.

Circle No 381

SCSI CONTROLLER

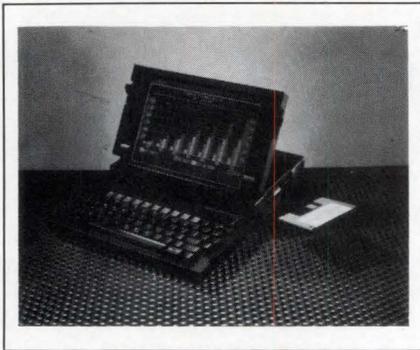
- Controls as many as seven devices
- Provides 10M-bps transfer rates

The SM911 SCSI controller card for PC and PC/AT buses can control as many as seven serially chained floppy-disk drives or hard disks providing as much as 2.8G bytes of storage. The 4×4½-in. card consumes <10W and transfers data at a 10M-bps rate. It comes with 50- and 34-pin connectors for the control of internal floppy-disk drives, and with a 25-pin connector for the control of an external SCSI drive. The card's internal ROMBIOS contains

software drivers for two 33M-byte drives. Software drivers provided on floppy disks support large SCSI disks, optical drives, tape drives, Xenix operating systems, and the Novell operating environment. The board contains diagnostic routines that test the SCSI bus for connected drives, prepare the drives for use or formatting, and ascertain the type and size of the SCSI device. \$159.

Tega Technologies Inc, 1040 E Chapman Ave, Orange, CA 92666. Phone (714) 771-5128.

Circle No 382



12-LB LAP COMPUTER

- Uses 80C286 μP
- Runs MS-DOS 3.2 Extended

The 1520 battery-powered lap computer is based on a 10-MHz 80C286 μP and runs on MS-DOS version 3.2 Extended. It will run OS/2 when that software becomes available. Its standard features include a 10-in. LCD; 1M bytes of RAM; two 1.4M-byte, 3½-in. internal floppy-disk drives; and as much as 512k bytes of user-installable ROM. The computer comes with a 72-key keyboard, weighs 12 lbs, and is enclosed in a 2.3×11.5×15.0-in. magnesium case. It has an RGB video port, a 25-pin external floppy-disk-drive port, an RS-232C port, a parallel port, a port for an external keyboard, and a port for an expansion bus. Options include 640×200- and 640×400-pixel gas-plasma displays, a 40M-byte hard disk, an 80287 coprocessor, a 2400/1200/300-baud internal modem, internal and external NiCd rechargeable-battery packs, and ex-

pansion cartridges that offer 3270, video-graphics-adaptor (VGA), and GridLink LAN support. \$3495.

Grid Systems Corp, 47211 Lakeview Blvd, Box 5003, Fremont, CA 94538. Phone (415) 656-4700.

Circle No 383



MULTIMETER

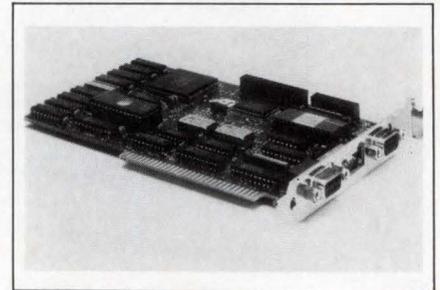
- Displays measurement data on a monitor
- Has adaptors that measure humidity, temperature, and rpm

The Multimeter Based Data Acquisition System is a multimeter with a built-in data bus that lets you display measured data on a computer monitor. The multimeter connects to an RS-232C-interface box, which in turn connects to your computer. The multimeter functions as a data recorder/analyzer or as automatic test equipment. It measures dc and ac voltage, dc and ac amperage, and resistance, and it checks diodes and transistors. Its dc-voltage measurement is accurate to within 0.5%. The multimeter operates from a 9V battery and has a built-in stand. The system's data-acquisition and communication software runs on an IBM PC, IBM PC/XT, IBM PC/AT, or compatible. You can enter the data manually or have it automatically entered. You can obtain optional adapters to measure humidity, temperature, dc or ac current, rpm, light level, and air velocity. You can select data-transmission rates from 9600 to 1200 baud. An optional data transmitter and data receiver enable you to send data at 1200 baud over ordinary telephone lines without the need for a computer. Mul-

timer, \$89; RS-232C interface, \$149; DB-25 cable, \$29; software, \$29; transmitter, \$269; and receiver, \$269.

Extech Instruments Corp, 150 Bear Hill Rd, Waltham, MA 02154. Phone (617) 890-7440.

Circle No 384



GRAPHICS CARD

- Displays all 17 IBM VGA modes on analog monitors
- Provides 800×560-pixel resolution

The VIP video graphics adapter (VGA) card works with the IBM PC, PC/XT, PC/AT, PS/2 Model 30, Compaq Portable PC, and compatibles. The card can display all 17 VGA modes on analog monitors. It can also display enhanced-graphics-adaptor (EGA) text and graphics on all IBM-compatible digital monitors. The card automatically switches to analog mode if you connect an analog monitor. Its Soft-Sense mode-switching feature switches your software to the correct mode. The card provides 800×560-pixel resolution max on multisync monitors and, in analog mode, can display as many as 256 of a possible 256,000 colors. The board also works with the color graphics adapter (CGA) and the Hercules monochrome graphics standard. The card comes with both 9- and 15-pin connectors for use with either digital or analog monitors. \$449.

ATI Technologies Inc, 3761 Victoria Park Ave, Scarborough, Ontario, Canada M1W 3S2. Phone (416) 756-0711.

Circle No 385

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ANALOGIC

DATA PRECISION

BYTEK's NEW 135 MULTIPROGRAMMER™ OFFERS 18/12 PROTECTION PLAN



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COMPATIBLE: The 135 offers Terminal and Computer Remote control, Data I/O* compatible+.

* Data I/O is a Registered Trademark of Data I/O Corporation.
+Some limitations may apply.

FLEXIBLE: The 135 can easily be expanded to program 40-Pin EPROMS, Bipolar PROMS, Logic Array Devices, EPROM Emulation, and 40 Pin Micro Devices.

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CIRCLE NO 20

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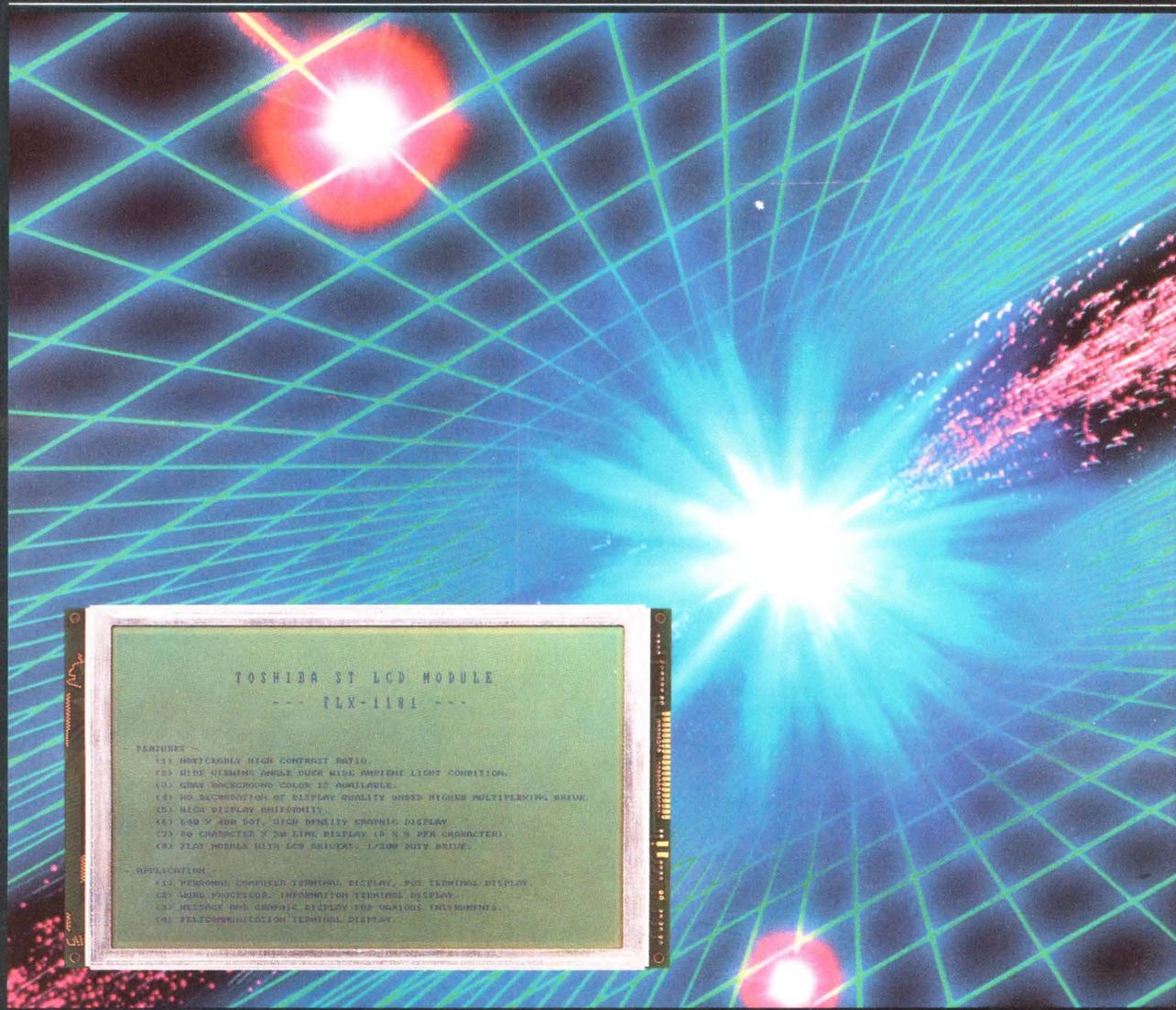
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EDN

EDN 1988 CALENDAR

A Guide to Electronics and Computer Industry Events



When your eyes need high quality displays,
you need the Toshiba ST LCD.

TOSHIBA

SUNDAY	MONDAY	TUESDAY	WEDNESDAY	THURSDAY	FRIDAY	SATURDAY
					1 NEW YEARS DAY	2
3	4	5	6	7	8	9
10	11	12	13	14	15	16
17	18 MARTIN LUTHER KING, JR. DAY	19	20	21	22	23
24 31	25	26	27	28	29	30

-5-8 21st Hawaii International Conference on System Sciences
Kona Surf Resort, Kailu-Kona (Ralph Sprague, Jr., Decision Sciences Dept., University of Hawaii, 2404 Maile Way, E-303, Honolulu, HI 96822, 808/948-7430)

-7-8 Simulation in Engineering Education
San Diego (SCS, P.O. Box 17900, San Diego, CA 92117, 619/277-3888)

-7 OEM Peripheral Conference
Hilton Towers, Irvine (Susie Ring, ICC, 3151 Airway Avenue, #C-2, Costa Mesa, CA 92626, 714/957-0171)

-10 3rd Annual Technical Symposium on Optoelectronics & Laser Applications in Science & Engineering
Viscount Hotel, Los Angeles (Jane Lybecker, SPIE, P.O. Box 10, Bellingham, WA 98227, 206/676-3290)

-12 PC Reseller Conference
Hilton International, London (Susie Ring, ICC, 3151 Airway Avenue, #C-2, Costa Mesa, CA, 92626, 714/957-0171)

-12-14 ATE & Instrumentation Conference West
Disneyland Hotel, Anaheim (MG Expositions Group, 1050 Commonwealth Avenue, Boston, MA 02215, 800/223-7126)

-13-15 Annual IEEE Design Automation Workshop
Gold Canyon Ranch, Apache Junction, Arizona (Walling Cyre, Control Data, HQM 173, Box 1249, Minneapolis, MN 55440, 612/853-2692)

-13-15 Computer Graphics '88
U.S. Grant Hotel, San Diego (Carol Every, Frost & Sullivan, Inc., 106 Fulton Street, New York, NY 10038, 212/233-1080)

-14 OEM Peripheral Conference
Sheraton, Munich (Susie Ring, ICC, 3151 Airway Avenue, #C-2, Costa Mesa, CA 92626, 714/957-0171)

-19 PC Reseller Conference
Hotel International, Zurich (Susie Ring, ICC, 3151 Airway Avenue, #C-2, Costa Mesa, CA 92626, 714/957-0171)

-19-21 Failure Avoidance/Failure Analysis For VLSI Circuits
Santa Clara (DM Data Inc., 6900 E. Camelback Rd., Suite 1000, Scottsdale, AZ 85251, 602/945-9620)

-19-21 PCB Expo 1988
Omni International Hotel, Orlando (Heidi Hogarth, 1790 Hembree Road, Alpharetta, GA 30201, 404/475-1818)

-20 Basic IC Technology Seminar
San Jose (ICE 15022 N. 75th Street, Scottsdale, AZ 85260, 602/998-9780)

-20-21 San Diego Electronics Show
Del Mar Fairgrounds, Del Mar, CA (Harry Schwartz, Epic Enterprises, Inc., 3838 Camino Del Rio North, Suite 164, San Diego, CA 92108, 619/284-9268)

-21 OEM Peripheral Conference
Hotel Executive, Milano (Susie Ring, ICC, 3151 Airway Avenue, #C-2, Costa Mesa, CA 92626, 714/957-0171)

-21 Status '88
San Jose (ICE 105022 N. 75th Street, Scottsdale, AZ 85260, 602/998-9780)

-22 How to Save Thousands of Dollars on Your Semiconductor Purchases and System Designs
Santa Clara (DM Data Inc., 6900 E. Camelback Rd., Suite 1000, Scottsdale, AZ 85251, 602/945-9620)

-24-27 Workshop on High-Level Synthesis
Rosario Resort, Orcas Island, Eastsound, WA (Ewald Detjens, Exemplar Logic, 1820 Carleton Street, Berkeley, CA 94703, 415/849-2020)

-25-26 Engineers Expo Career Open House
Melbourne/Orlando, FL (Engineers Expo, 2367 Auburn Avenue, Cincinnati, OH 45219, 513/721-3030)

-25-27 Conference On Optical Fiber Communication (OFC '88)
New Orleans (OSA Meetings Department, 1816 Jefferson Place, NW, Washington DC 20036, 202/223-0926)

-25-28 Tenth Annual Communications Networks Conference and Exposition
Washington Convention Center, Washington DC (Nancy Thayer, IDG Conference Management Group, P.O. Box 9171, Cochituate Road, Framingham, MA 01701, 617/879-0700)

-25-28 88th Annual Florida Computing Conference
Hyatt Orlando, Kissimmee, FL (David L. Britian, Florida Department of Education, Knott Bldg., Tallahassee, FL 32399, 904/488-0980)

-26 OEM Peripheral Conference
Marina Marriott Hotel, Ft. Lauderdale (Susie Ring, ICC 3151 Airway Avenue, #C-2, Costa Mesa, CA 92626, 714/957-0171)

-26 OEM Peripheral Conference
Hotel Paris Sofitel, Paris (Susie Ring, ICC 3151 Airway Avenue, #C-2, Costa Mesa, CA 92626, 714/957-0171)

-26-28 1988 Annual Reliability and Maintainability Symposium
Biltmore Hotel, Los Angeles (V. R. Monshaw, RCA, Astro Electronics, P.O. Box 800, MS 55, Princeton, NJ 08540, 609/426-2182)

-26-28 AFCEA West '88
Disneyland Hotel, Anaheim (AFCEA International Headquarters, 4400 Fair Lakes Court, Fairfax, VA 22033, 703/631-6125)

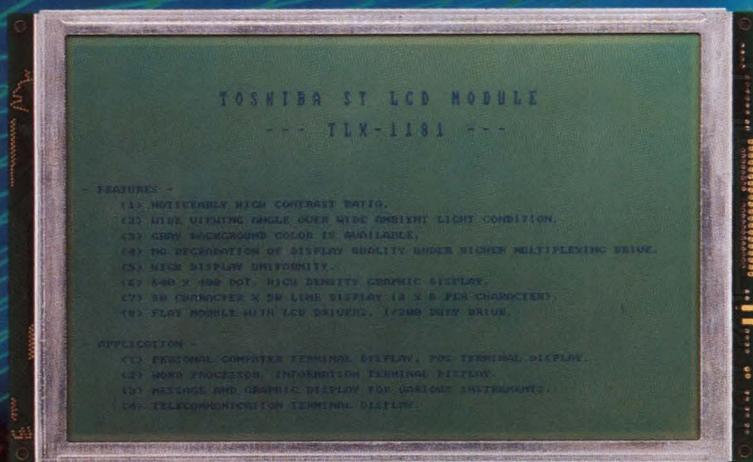
-26-28 Charlotte Manufacturing Productivity Conference & Advanced Productivity Exposition (APEX)
Charlotte Convention Center, Charlotte, NC (Nancy LePage, Society of Manufacturing Engineers, One SME Drive, PO Box 930, Dearborn, MI 48121, 313/271-0777)

-27-30 Expo Hospital
Nikko Hotel, Mexico City (Bill Warnes, Marketing International Corp., P.O. Box 4749, Arlington, VA 22204, 703/685-0600)

-27 Basic IC Technology
Scottsdale, AZ (ICE, 15022 N. 75th Street Scottsdale, AZ 85260, 602/998-9780)

-28 Status '88
Scottsdale, AZ (ICE, 15022 N. 75th Street Scottsdale, AZ 85260, 602/998-9780)

-31-Feb. 5 1988 Power Engineering Society Winter Meeting
Penta Hotel, New York (J.G. Derse, 1030 Country Club Road, Bedminster, NJ 07921, 201/725-4388)



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Model name	Number of dots	Duty	Dot pitch (mm)	Outline dimensions (mm)	EL Back Light (Option)	Recommended controller
TLX-1181*	640 × 400	1/200	0.35 × 0.35	276 × 168 × 12	Yes	T7779
TLX-932	640 × 200	1/200	0.375 × 0.375	293 × 97.6 × 14	No	T7779
TLX-561	640 × 200	1/200	0.35 × 0.49	275 × 126 × 14	Yes	T7779
TLX-711A*	240 × 64	1/64	0.53 × 0.53	180 × 65 × 12	Yes	T6963C**
TLX-341AK*	128 × 128	1/64	0.45 × 0.45	93.2 × 86.6 × 12	No	T6963C

*Under development, **Built-in controller

In Touch with Tomorrow
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CIRCLE NO 51

SUNDAY	MONDAY	TUESDAY	WEDNESDAY	THURSDAY	FRIDAY	SATURDAY
	1	2	3	4	5	6
7	8 WASHINGTON'S BIRTHDAY obsvd.	9	10 ASH WEDNESDAY	11	12 LINCOLN'S BIRTHDAY	13
14	15	16	17	18	19	20
21	22	23	24	25	26	27
28	29					

-1-5 4th International Conference on Data Engineering

Airport Hilton, Los Angeles (Benjamin W. Wah, Dept. of Elec. & Comp. Engineering, University of Illinois, Urbana, IL 61801, 217/333-3516)

-1-5 APEC '88 IEEE Applied Power Electronics Conference and Exposition

Fairmont Hotel, New Orleans (William W. Burns, III, Conference Chairman, Data General Corporation, E213 4400 Computer Drive, Westboro, MA 01580, 617/870-9182)

-3 Basic IC Technology

Orlando, FL (ICE, 15022 N. 75th Street, Scottsdale, AZ 85260, 602/998-9780)

-3-5 1988 SCS Multiconference: Modeling and Simulation on Microcomputers, Power Plant Simulation, Aerospace Simulation, Distributed Simulation, AI and Simulation, Multiprocessor and Array Processor Conference

San Diego, CA (SCS, P.O. Box 17900, San Diego, CA 92117, 619/277-3888)

-4 Status '88

Orlando (ICE, 15022 N. 75th Street, Scottsdale, AZ 85260, 602/998-9780)

-4 Computer Graphic Conference

Red Lion Inn, San Jose (Susie Ring, Conference Coordinator, ICC, 3151 Airway Avenue, #C-2, Costa Mesa, CA 92626, 714/957-0171)

-9-12 Mexico ComExpo 88

National Auditorium, Mexico City (Bill Warnes, Marketing International Corp., P.O. Box 4749, Arlington, VA 22204, 703/685-0600)

-10 Basic IC Technology

Newport Beach, CA (ICE, 15022 N. 75th Street, Scottsdale, AZ 85260, 602/998-9780)

-11 OEM Peripheral Conference

Crowne Plaza Hotel, Dallas (Susie Ring, ICC, 3151 Airway Avenue, #C-2, Costa Mesa, CA 92626, 714/957-0171)

-11 Status '88

Newport Beach, CA (ICE, 15022 N. 75th Street, Scottsdale, AZ 85260, 602/998-9780)

-16 ERA Communications Trade Fair

Mesa/Chandler Holiday Inn, Mesa AZ (Robert Myers, 1700 Westwood Blvd., Suite 101, Los Angeles, CA 90024, 213/879-7119)

-17 Basic IC Technology

Boston (ICE, 15022 N. 75th Street, Scottsdale, AZ 85260, 602/998-9780)

-17-19 IEEE International Solid-State Circuits Conference

San Francisco (Lewis Winner, 301 Almeria Avenue, Coral Gables, FL 33134, 305/446-8193/4)

-18 ERA Communications Trade Fair

Town & Country Hotel, San Diego (Robert Myers, 1700 Westwood Blvd., Suite 101, Los Angeles, CA 90024, 213/879-7119)

-18 IEEE Video Conferences: User Examples of AI

(IEEE Continuing Education Dept., 445 Hoes Lane, Piscataway, NJ 08854, 201/981-0060 ext. 412)

-22-23 Engineers Expo Career Open House

Baltimore/Washington Corridor (Engineers Expo, 2367 Auburn Avenue, Cincinnati, OH 45219, 513/721-3030)

-22-24 PCB Expo 1988

Red Lion Inn, Costa Mesa, CA (Heidi Hogarth, 1790 Hembree Road, Alpharetta, GA 30201, 404/475-1818)

-23-25 Buscon/88-West

Disneyland Hotel, Anaheim (Anne Weber, MultiDynamics, Inc., 17100 Norwalk Blvd., Suite 116, Cerritos, CA 90701, 213/402-1618)

-23-25 Nepcon West '88

Anaheim Convention Center, Anaheim (Jerry Carter, Cahners Exposition Group, 1350 E. Touhy Avenue, Des Plaines, IL 60018, 312/299-9311)

-23-25 Power Electronics '88 West

Disneyland Hotel, Anaheim (Anne Weber, MultiDynamics, Inc., 17100 Norwalk Blvd., Suite 116, Cerritos, CA 90701, 213/402-1618)

-23-25 Advanced Ceramics '88 Conference & Tabletop Exhibits

Hyatt Regency, Rosemont, IL (Nancy LePage, Society of Manufacturing Engineers, One SME Drive, PO Box 930, Dearborn, MI 48121, 313/271-0777)

-25 PC Reseller Conference

Ramada Hotel O'Hare, Chicago (Susie Ring, ICC, 3151 Airway Avenue, #C-2, Costa Mesa, CA 92626, 714/957-0171)

-25-26 Automated Manufacturing '88: Computers, Communications and Controls in the Factory

Don Cesar Beach Resort, St. Petersburg Beach, FL (Yvonne Chism, Frost & Sullivan, Inc., 106 Fulton Street, New York, NY 10038, 212/233-1080)

-28-March 2 1988 IEEE Network Operations and Management Symposium

Sheraton New Orleans Hotel, New Orleans (Dr. R. Bruce Kiebertz, AT&T Bell Laboratories, Room 14A-471, Whippany Road, Whippany, NJ 07981, 201/386-5371)

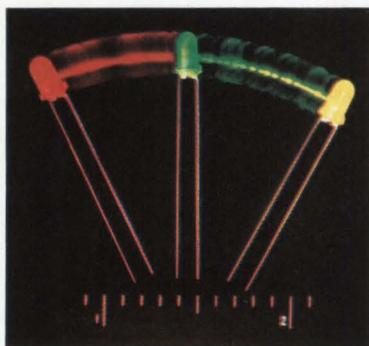
-29-March 3 1988 IEEE Computer Society COMPCON Spring '88

Cathedral Hill Hotel, San Francisco (COMPCON Spring '88, 1730 Massachusetts Avenue NW, Washington, DC 20036, 202/371-0101)



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SUNDAY	MONDAY	TUESDAY	WEDNESDAY	THURSDAY	FRIDAY	SATURDAY
		1	2	3	4	5
6	7	8	9	10	11	12
13	14	15	16	17 ST. PATRICK'S DAY	18	19
20	21	22	23	24	25	26
27 PALM SUNDAY	28	29	30	31		

-1-3 Semicon Europa

Zuspa Convention Center, Zurich (Bill Galarna, 805 E. Middlefield Road, Mountain View, CA 94043, 415/964-5111)

-4 Computer Graphic Conference

Sheraton National Hotel, Arlington, VA (Susie Ring, ICC, 3151 Airway Avenue, #C-2, Costa Mesa, CA 92626, 714/957-0171)

-7-10 FOSE '88, FOSE Software, FOSE Computer Graphics

Washington Convention Center, Washington, DC (Jackie Voight, National Trade Association, 800/638-8510, 703/683-8500)

-7-10 33rd International SAMPE Symposium/Exhibition

Anaheim Convention Center, Anaheim (Marge Smith, SAMPE, 843 West Glentana (Box 2459), Covina, CA 91722, 818/331-0616)

-8 Semiconductor Packaging

San Jose (ICE, 15022 N. 75th Street, Scottsdale, AZ 85260, 602/998-9780)

-8-10 Southcon/88

Orange County Convention/Civic Center, Orlando, FL (Alexes Razevich, Electronic Conventions Mgmt., 8110 Airport Blvd., Los Angeles, CA 90045, 800/421-6816, or 213/772-2965)

-8-11 1988 International Zurich Seminar on Digital Communications

Zurich (Secretariat IZS 88, c/o P. Gunzburger, Hasler AG, TDS, Belpstrasse 23, CH-3000 Bern 14, Switzerland 41-31-632808)

-9 OEM Peripheral Conference

Red Lion Inn, San Jose (Susie Ring, ICC, 3151 Airway Avenue, #C-2, Costa Mesa, CA 92626, 714/957-0171)

-9-11 Practical IC Fabrication

San Jose (ICE, 15022 N. 75th Street, Scottsdale, AZ 85260, 602/998-9780)

-14-15 Engineers Expo Career Open House

Huntsville, AL (Engineers Expo, 2367 Auburn Avenue, Cincinnati, OH 45219, 513/721-3030)

-14-18 4th International Conference on Artificial Intelligence Applications

Sheraton Harbour Island, San Diego (AI Conference, Computer Society of the IEEE, 1730 Massachusetts Avenue, NW, Washington, DC 20036, 202/371-1013)

-15-17 Failure Avoidance/Failure Analysis for VLSI Circuits

Orlando (DM Data, Inc., Ste 1000, Scottsdale AZ, 85251, 602/945-9620)

-15-18 PetroMex Petroleum/Petrochemical Equipment Expo

National Auditorium, Mexico City (William Warnes, Marketing International Corp., P.O. Box 4749, Arlington, VA 22204, 703/685-0600)

-16 ERA CIDtec

Edwards Air Force Base, CA (Bruce Myers, 1700 Westwood Blvd., Suite 101, Los Angeles, CA 90024, 213/879-7119)

-16-18 Twenty-first Annual Simulation Symposium

Tampa, FL (Alfred Jones, Computer Science Department, Florida Atlantic University, Boca Raton, FL 33431, 305/393-3675)

-17 ERA CIDtec

China Lake Naval Weapons Center, China Lake, CA (Bruce Myers, 1700 Westwood Blvd., Suite 101, Los Angeles, CA 90024, 213/879-7119)

-18 How to Save Thousands of Dollars on Your Semiconductor Purchases and System Designs

Orlando (DM Data, Inc., 6900 E. Camelback Rd., Suite 1000, Scottsdale, AZ 85251, 602/945-9620)

-21-24 Computer Standards Conference (COMPSTAN)

Sheraton National, Arlington, VA (Roger J. Martin, U.S. Dept. of Commerce, Natl. Bureau of Standards, Technology Bldg, 225, Rm. B266, Gaithersburg, MD 20899, 301/975-3295)

-21-24 Westec '88, The Western Metal & Tool Exposition and Conference

Los Angeles Convention Center, Los Angeles (Nancy LePage, Society of Manufacturing Engineers, One SME Drive, PO Box 930, Dearborn, MI 48121, 313/271-0777)

-21-24 Video Audio & Data Recording

University of York, England (The Conference Secretariat, Institution of Electronic and Radio Engineers, Savoy Hill House, Savoy Hill, London WC2R OJD, England)

-21-24 NCGA Computer Graphics '88

Anaheim Convention Center, Anaheim (Nancy A. Flower, National Computer Graphics Association, 2722 Merrilee Drive, Suite 200, Fairfax, VA 22031, 703/698-9600)

-22-23 Failure Analysis Avoidance

San Jose (ICE, 15022 N. 75th Street, Scottsdale, AZ 85260, 602/998-9780)

-23 IEEE Video Conferences: VLSI Microprocessors

(IEEE Continuing Education Dept., 445 Hoes Lane, Piscataway, NJ 08854, 201/981-0060 ext. 412)

-23-25 Conference on Office Information Systems

Hyatt Richeys Hotel, Palo Alto (Robert B. Allen, Room 2A 367, Bell CORE, Morristown, NJ 07960, 201/829-4315)

-23-25 Extending Database Technology

Cini Foundation, Venice (Prof. Stefano Cer, Politecnico di Milano, Dipart. de Elektronika, Piazza Leonard da Vinci 32, 20133 Milano, Italy, 02-2367241)

-24 ERA Electro-tech

Proud Bird Restaurant, Los Angeles (Bruce Myers, 1700 Westwood Blvd., Suite 101, Los Angeles, CA 90024, 213/879-7119)

-27-April 1 AEA/Wharton School General Management Program

Philadelphia (Mary Horngren Frost, AEA, 5201 Great America Parkway, Santa Clara, CA 95054, 408/987-4200)

-28 OEM Peripheral Conference

Sheraton Tara Hotel, Nashua, NH (Susie Ring, ICC, 3151 Airway Avenue, #C-2, Costa Mesa, CA 92626, 714/957-0171)

-28-31 IEEE Infocom '88

Sheraton New Orleans Hotel, New Orleans (Infocom '88, Computer Society of the IEEE, 1730 Massachusetts Avenue, NW, Washington, DC 20036, 202/371-1013)

-28-31 Interface '88

McCormick Place, Chicago (Peter B. Young, Interface Group, 300 First Avenue, Needham, MA 02194, 617/449-6600)

-28-31 World Congress on Computing

McCormick Place, Chicago (Peter B. Young, Interface Group, 300 First Avenue, Needham, MA 02194, 617/449-6600)

-29-30 Colour Information Technology

University of Surrey, England (The Conference Secretariat, Institution of Electronic and Radio Engineers, Savoy Hill House, Savoy Hill, London WC2R OJD, England)

-29-31 Electronic Imaging Conference West

Anaheim Hilton Hotel, Anaheim (MG Expositions Group, 1050 Commonwealth Avenue, Boston, MA 02215, 617/232-EXPO)

SUNDAY	MONDAY	TUESDAY	WEDNESDAY	THURSDAY	FRIDAY	SATURDAY
					1 GOOD FRIDAY	2 PASS-OVER
3 EASTER SUNDAY	4	5	6	7	8	9
10	11	12	13	14	15	16
17	18	19	20	21	22	23
24	25	26	27	28	29	30

- 4-8 Semicon Shanghai**
Shanghai Exhibition Center, Shanghai, China (Bill Galarnea, 805 E. Middlefield, Road, Mountain View, CA 94043, 415/964-5111)
- 6-8 Fabtech East Conference & Exposition**
Baltimore Convention Center, Baltimore (Nancy LePage, Society of Manufacturing Engineers, One SME Drive, PO Box 930, Dearborn, MI 48121, 313/271-0777)
- 7-10 West Coast Computer Faire**
Moscone Center, San Francisco (Peter B. Young, The Interface Group, 300 First Avenue, Needham, MA 02194, 617/449-6600)
- 8 PC Reseller Conference**
Loews Glenpointe Hotel, Teaneck, NJ (Susie Ring, ICC, 3151 Airway Avenue, #C-2, Costa Mesa, CA 92626, 714/957-0171)
- 10-13 Southeastcon '88**
Hyatt Regency Hotel, Knoxville, TN (Prof. Reece Roth, Dept. of Electrical Engineering, University of Tennessee, Knoxville, TN 37996-2100, 615/974-4446)
- 11-13 4th International Conference on HF Radio Systems & Techniques**
Savoy Place, London (IEE Conference Services, Savoy Place, London WC2R OBL, 01-240-1871, ext. 222)
- 11-13 1988 Computer Networking Symposium**
Sheraton National Hotel, Arlington, VA (George K. Chang, 6 Corporation Pl., Piscataway, NJ 08854, 201/699-3879)
- 11-14 1988 IEEE International Conference on Acoustics, Speech & Signal Processing (ICASSP '88)**
New York Hilton Hotel, New York (Aaron E. Rosenberg, AT&T Bell Laboratories, Room 2D528, 600 Mountain Avenue, Murray Hill, NJ 07974, 201/582-4985)
- 11-14 1988 International Reliability Physics Symposium**
Del Monte Hyatt Hotel, Monterey, CA (Alfred L. Tamburrino, RADC/RBRP, Griffiss AFB, NY 13441-5700, 315/330-2813)
- 11-15 10th International Conference on Software Engineering**
Raffles City, Singapore (Tan Chin Nam/Lim Swee Say, 71 Science Park, Singapore 0511, 65/772-0200)
- 11-15 Compeuro**
Vrije Universiteit, Brussels, Belgium (Jacques Tiberghien, Vrije Universiteit Brussels, Pleinlaan 2, 1050 Brussels, Belgium, 32-2-641-29-05)
- 11-15 International Specialist Seminar on the Design and Application of Parallel Digital Processors**
Lisbon, Portugal (IEE Conference Services, Savoy Place, London WC2R OBL, 01-240-1871, ext. 222)
- 12 Semiconductor Packaging**
Scottsdale, AZ (ICE, 105022 N. 75th Street, Scottsdale, AZ 85260, 602/998-9780)
- 12-13 MMA Meeting & Show**
Sheraton Centre, New York (Jim Mion or Annie Zdinak 333 Sylvan Avenue, Englewood Cliffs, NJ 07632, 800/237-0316, 201/569-6916)
- 13-15 Practical IC Fabrication**
Scottsdale, AZ (ICE, 105022 N. 75th Street, Scottsdale, AZ 85260, 602/998-9780)
- 13-15 Control '88**
London (IEE Conference Services, Savoy Place, London WC2R OBL, 01-240-1871, ext. 222)
- 14 OEM Peripheral Conference**
Toronto Airport Marriott, Toronto (Susie Ring, ICC, 3151 Airway Avenue, #C-2, Costa Mesa, CA 92626, 714/957-0171)
- 17-22 IIEPC 31st Annual Meeting**
Diplomat Hotel, Hollywood, FL (Virginia Perry, IIEPC, 7380 N. Lincoln, Lincoln Wood, IL 60646 312/677-2850)
- 18-19 Engineers Expo Career Open House**
Long Island (Engineers Expo, 2367 Auburn Avenue, Cincinnati, OH 45219, 513/721-3030)
- 18-20 50th Annual American Power Conference**
Palmer House, Chicago (Dr. Robert Porter, Illinois Institute of Technology, Chicago, IL 60616, 312/567-3202)
- 18-21 Eastern Simulation Conferences: Simulators V, The Simulation Profession, Tools for the Simulationist, Credibility Assessment, Simulation Languages, AI and Simulation**
Orlando, FL (SCS, P.O. Box 17900, San Diego, CA 92117, 619/277-3888)
- 19-22 1988 Instrumentation and Measurement Technology Conference (IMTC '88)**
San Diego Princess Hotel, San Diego (Robert Myers, 1700 Westwood Blvd., Suite 101, Los Angeles, CA 90024, 213/475-4571)
- 19-22 11th Annual IEEE Workshop on Design for Testability**
Vail, CO (T.W. Williams, IBM Corporation, PO Box 1900, Dept. 67A/021, Boulder, CO 80301-9191, 303/924-7692)
- 19-22 Analytica 88**
Munich Trade Fair Centre, Munich (Gerald G. Kallman, Kallman Associates, Five Maple Court, Ridgewood, NJ 07450-4431, 201/652-7070)
- 20-21 1988 IEEE National Radar Conference**
University of Michigan, Ann Arbor (Mr. Clarence Heerema, Environmental Research Inst. of Michigan, PO Box 8618, Ann Arbor, MI 48107, or Dr. Jack Walker, (313) 994-1200)
- 24-26 Semicon West**
San Mateo Fair Grounds, San Mateo, CA (Bill Galarnea, 805 E. Middlefield, Road, Mountain View, CA 94043, 415/964-5111)
- 24-29 1988 International Conference on Robotics and Automation**
Wyndham Franklin Plaza Hotel, Philadelphia (Dr. Theo Pavlidis, Dept. of Electrical Engineering, SUNY, Stony Brook, NY 11794, 516/246-3556 or Prof. R.P. Paul, University of Pennsylvania, Philadelphia, PA 19104, 215/898-1592)
- 25-28 2nd International Conference on Expert Database Systems**
Sheraton Premiere Hotel, Tysons Corner, VA (Edgar H. Sibley, George Mason University, ICSE Dept., 4400 University Drive, Fairfax, VA 22030)
- 25-29 Conference on Lasers and Electro-Optics (CLEO'88)**
Anaheim (OSA, Meetings Dept., 1816, Jefferson Place NW, Washington, DC 20036 202/223-0926)
- 26 Computer Graphic Conference**
Munich Sheraton, Munich (Susie Ring, ICC, 3151 Airway Avenue, #C-2, Costa Mesa, CA 92626, 714/957-0171)
- 26-28 Electronic Distribution Conference '88**
Las Vegas Hilton, Las Vegas (David Fischer, 222 S. Riverside Plaza, Ste. 2710, Chicago, IL 60606)
- 26-28 ATE 1988 Automatic Testing and Test Instrumentation**
Olympia, London (Network Events, Ltd., Printers Mews, Market Hill, Buckingham, MK18 1JX, UK, 0280 815226)
- 26-28 MILTEST 1988 Military Test Equipment**
Olympia, London (Network Events, Ltd., Printers Mews, Market Hill, Buckingham, MK18 1JX, UK, 0280 815226)

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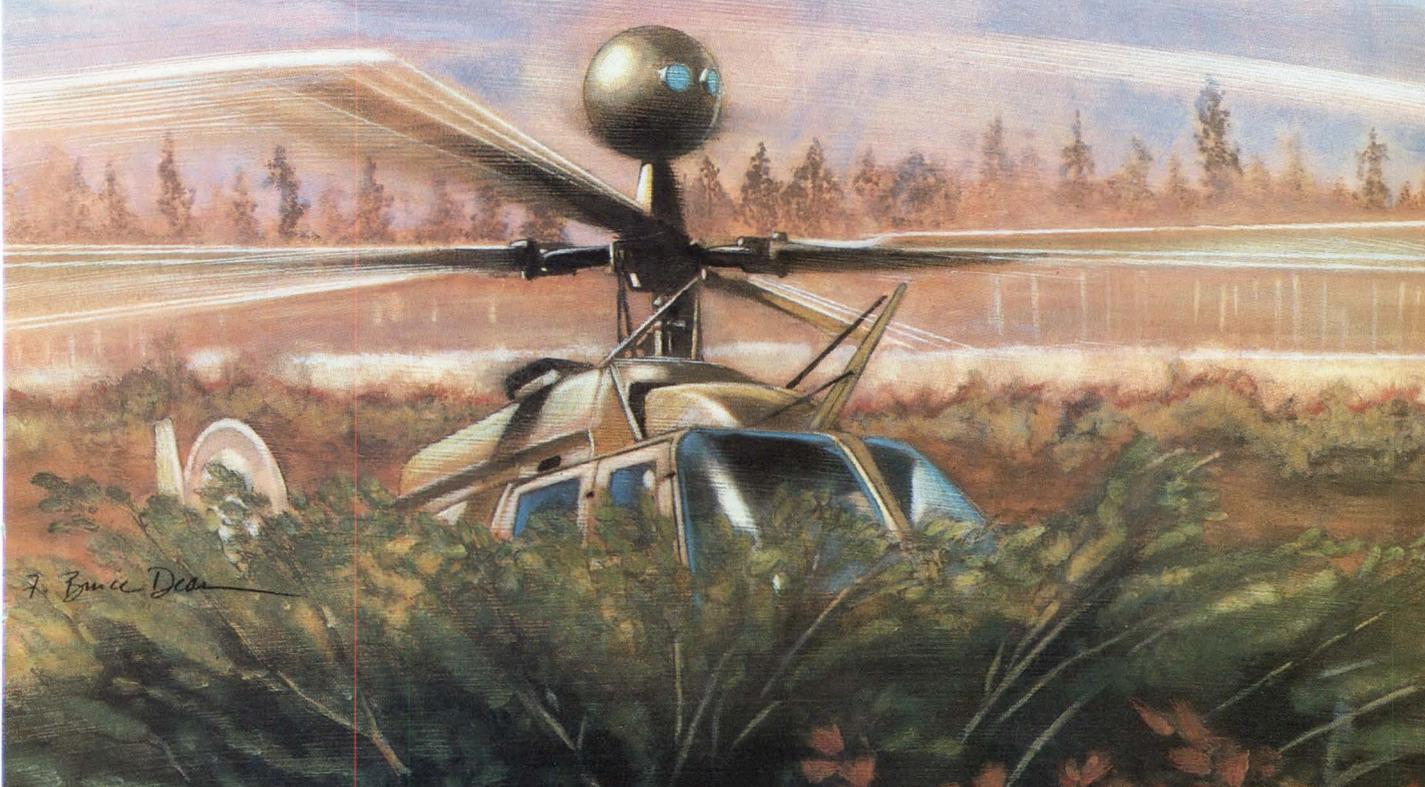
Abbott Transistor Laboratories, Inc. Power Supply Division, 2721 S. La Cienega Blvd., Los Angeles, CA 90034 (213) 936-8185. Eastern Office: (201) 461-4411, Southwest Office: (214) 437-0697, London Office: 0737-82-3273.

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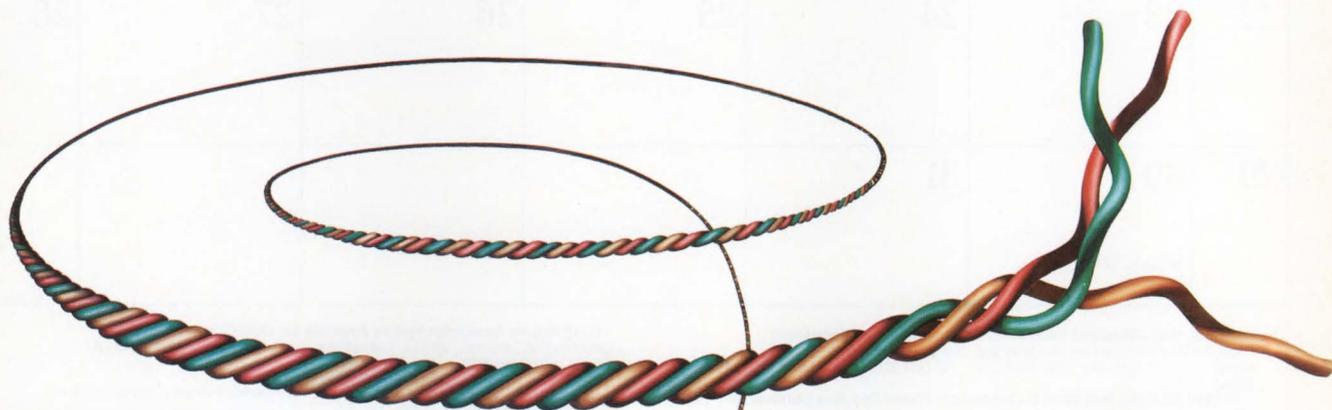
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CIRCLE NO 54

SUNDAY	MONDAY	TUESDAY	WEDNESDAY	THURSDAY	FRIDAY	SATURDAY
1	2	3	4	5	6	7
8	9	10	11	12	13	14
15	16	17	18	19	20	21
22	23	24	25	26	27	28
29	30 MEMORIAL DAY	31				

-2-5 SME 1988 Cleveland International Conference and Exposition

Cleveland Convention Center, Cleveland (Nancy LePage, Society of Manufacturing Engineers, One SME Drive, PO Box 930, Dearborn, MI 48121, 313/271-1500)

-2-5 1988 IEEE IAS Industrial & Commercial Power Systems Conference (I&CPS '88)

Baltimore Marriott Inner Harbor, Baltimore (Philip Hickman, El Comm Sales Associates, 1428 Meridene Drive, Baltimore, MD, 301/532-7565)

-3-5 Electronic Displays (ED88 Paris)

Palais des Congres, Paris (Network Events, Ltd., Printers Mews, Market Hill, Buckingham MK18 1JX, England, 0280 815226)

-4 Computer Graphic Conference

Hilton International, London (Susie Ring, 3151 Airway Avenue, #C-2, Costa Mesa, CA 92626, 714/957-0171)

-4 IEEE Videoconferences: Solid State Lasers

IEEE Continuing Education Dept., 445 Hoes Lane, Piscataway, NJ 08854-4150, 201/981-0060 ext. 412)

-4-5 Midwest Electronics Exposition

St. Paul Civic Center, St. Paul (MG Expositions Group, 1050 Commonwealth Avenue, Boston, MA 02215, 617/232-EXFO)

-4-6 The Artificial Intelligence and Advanced Computer Technology Conference/Exhibition

Long Beach, CA (Dr. Murray Teitell, Intelligent Choice, 1050 Duncan Ave., Ste. D, Manhattan Beach, CA 91109, 213/379-9680)

-4-6 Symposium AFCEA Exposition: Cooperation in C3I

Le Palais des Congres and Hotel Concorde La Fayette, Paris (John Spargo and Associates, 4400 Fair Lakes Court, Fairfax, VA 22033-3899, 703/631-6200)

-9-11 1988 38th Electronic Components Conference (ECC)

Bitmore Hotel, Los Angeles (Ron W. Gedney, Dept. T-10-B32-2, IBM Corp., 1701 North Street, Endicott, NY 13760, 607/755-3046)

-9-12 Comdex/Spring '88

Georgia World Congress Center, Atlanta (Peter B. Young, The Interface Group, 300 First Avenue, Needham, MA 02914, 617/449-4200)

-10 Computer Graphic Conference

Hilton International Paris, Paris (Susie Ring, 3151 Airway Avenue, #C-2, Costa Mesa, CA 92626, 714/957-0171)

-10-11 Failure Analysis Advancement

Boston (ICE, 15022 N. 75th Street, Scottsdale, AZ 85260, 602/998-9780)

-10-12 Electro '88

World Trade Center and Bayside Exposition Center, Boston (Alexis Razevech, Electronic Conventions Management, 8110 Airport Blvd., Los Angeles, CA 90045, 213/772-2965)

-11-12 WESCANEX '88 Digital Communications: Fibre, Satellite, Networks

University of Saskatchewan, Saskatoon, Saskatchewan, Canada (Don Barnett, Canadian Centre for Advance Instrumentation, 15, Innovation Blvd., Saskatoon, Saskatchewan, Canada, S7N 2X8)

-12-13 5th Workshop on Real-Time Operating Systems

Omni Shoreham Hotel, Washington, DC (Prof. John A. Stankovic, Dept. of Computer & Info Science, University of Massachusetts, Amherst, MA 01003, 413/545-0720)

-16 PC Reseller

Hilton International, London (Susie Ring, 3151 Airway Avenue, #C-2, Costa Mesa, CA 92626, 714/957-0171)

-16-19 1988 Custom Integrated Circuits Conference (CICC '88)

Rochester Riverside Convention Center, Rochester, NY (Laura Silzars, Convention Coordinating, 6900 SW Canyon Drive, Portland, OR 97225, 503/292-6347)

-17-19 PCB Expo

Red Lion Inn, San Jose (Heidi Hogarth, 1790 Hembree Road, Alpharetta, GA 30201, 404/475-1818)

-17-19 Failure Avoidance/Failure Analysis for VLSI Circuits

Boston (DM Data, Inc., 6900 E. Camelback Road, Suite 1000, Scottsdale, AZ 85251, 602/945-9620)

-18-21 AEA Executive Marketing Forum

Monterey, CA (Susan Puleo, AEA, 5201 Great America Parkway, Santa Clara, CA 95054, 408/987-4251)

-20 How to Save Thousands of Dollars on Your Semiconductor Purchases and System Designs

Boston (DM Data, Inc., 6900 E. Camelback Road, Suite 1000, Scottsdale, AZ 85251, 602/945-9620)

-20-22 RAINBOWfest

Hyatt Regency Woodfield, Schaumburg (O'Hare), IL (Ira D. Barsky, The Falstoff Building, 9509 U.S. Highway 42, PO Box 385, Prospect, KY 40059, 502/228-4492)

-23-26 Autocom Conference & Exhibits

Westin Hotel, Detroit (Nancy LePage, Society of Manufacturing Engineers, One SME Drive, PO Box 930, Dearborn, MI 48121, 313/271-1500)

-23-26 Supercomm '88

Georgia World Congress Center, Atlanta (Donald R. Pollock, U. S. Telecommunications Suppliers Association, 150 N. Michigan Avenue, Suite 600, IL 60601-7524, 312/782-8597)

-23-26 3rd International Conference on Ada Applications and Environments

Sheraton-Wayfarer Inn, Manchester, MA (Derek S. Morris, Dept. of EECS, Stevens Institute of Technology, Hoboken, NJ 07730, 201/420-5606)

-24-25 Engineers Expo Career Open House

Dayton, OH/NAECON (Engineers Expo, 2367 Auburn Avenue, Cincinnati, OH 45219, 513/721-3030)

-24-26 Hartford/Springfield Manufacturing Productivity Conference & Advanced Productivity Exposition (APEX)

Eastern States Exposition Center, West Springfield, MA (Nancy Le Page, Society of Manufacturing Engineers, One SME Drive, PO Box 930, Dearborn, MI 48121, 313/271-1500)

-24-26 18th International Symposium on Multiple-Valued Logic

Hotel Saratoga, Madrid (Enric Trillas, Consejo Superior, Investigaciones, Cientificas, Serrano 117, 28006-Madrid, Spain, (91) 6216264)

-24-27 ComExpo International Computer/Communications Expo

Venezuela Hilton Hotel, Caracas (William Warnes, Marketing International, PO Box 4749, Arlington, VA 22204 703/685-0600)

25-27 1988 IEEE MTT-S International Microwave Symposium

Marriott Marquis/New York Convention Center, New York (Charles Buntschuh, Narda Microwave Corp., 435 Moreland Road, Hauppauge, NY 11788, 516/231-1700)

-25-27 1988 International Workshop on Artificial Intelligence for Industrial Applications

Hitachi, Japan (Dr. Kotaro Hirasawa, Hitachi Research Laboratory, Hitachi, Ltd., 4026, Kuji-cho, Hitachi, Ibaraki, 319-12 Japan, or Prof. Alfred C. Weaver, Flight Data Systems, EH4, NASA - Johnson Space Center, Houston, TX 77058, 713/483-2801)

-29-31 1988 18th International Symposium on Multiple Valued Logic

Palma de Mallorca, Spain (Mr. Enric Trillas, Consejo Superior de Investigaciones, Cientificas, Serrano 17, 28008-Madrid, Spain)

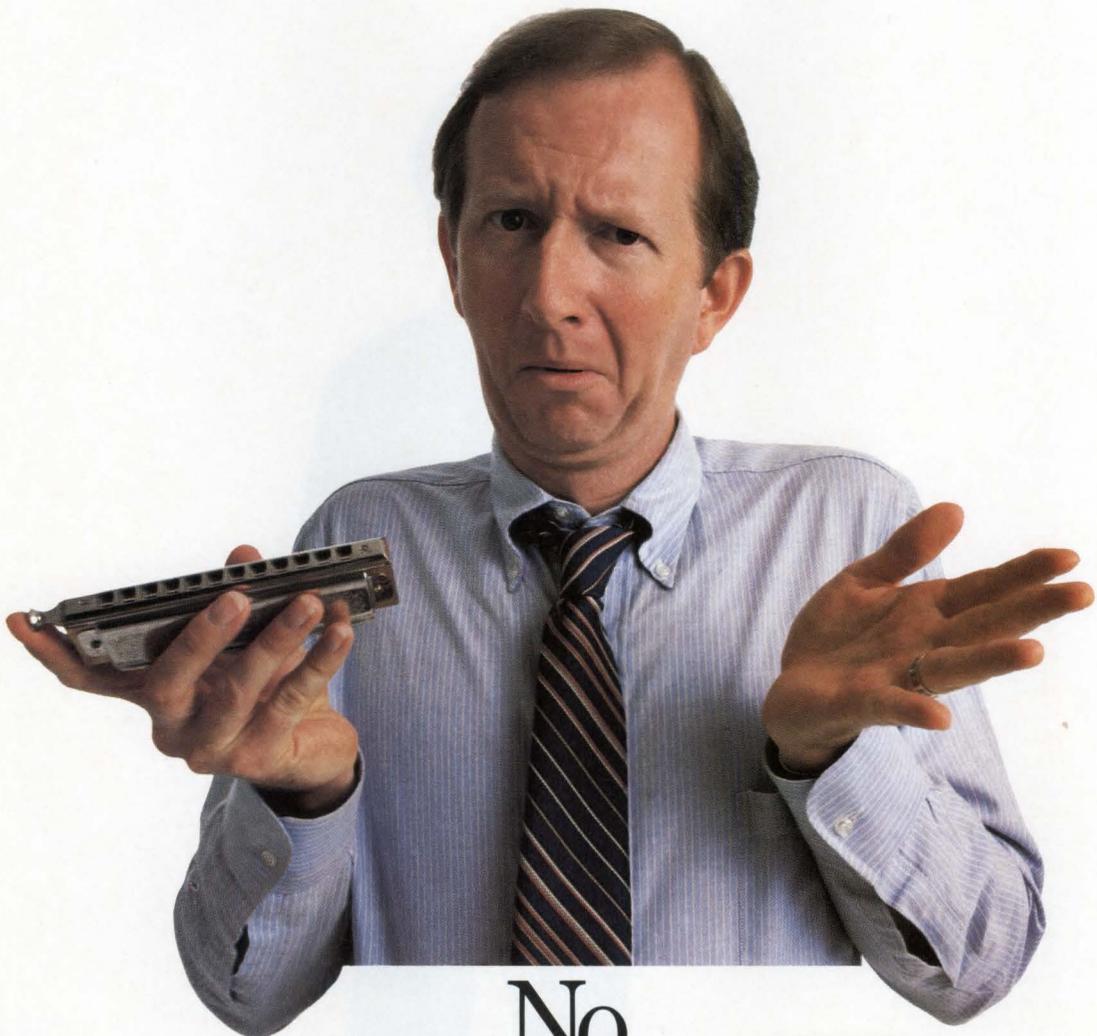
-30-June 2 15th International Symposium on Computer Architecture

Honolulu (H. J. Siegel, Supercomputing Research Ctr., 4380 Forbes Blvd., Lanham, MD 20706, 301/731-3700)

-31-June 3 National Computer Conference NCC/NCE

Los Angeles Convention Center (Matricia Smith, ISA Services, Inc., P.O. Box 12277, Research Triangle Park, NC 27709, 919/549-8411)

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SUNDAY	MONDAY	TUESDAY	WEDNESDAY	THURSDAY	FRIDAY	SATURDAY
			1	2	3	4
5	6	7	8	9	10	11
12	13	14 FLAG DAY	15	16	17	18
19	20	21	22	23	24	25
26	27	28	29	30		

-4-3 Pacific Northwest Advanced Productivity Exposition (APEX)
Tacoma Dome, Tacoma, WA (Nancy LePage, Society of Manufacturing Engineers, One SME Drive, PO Box 930, Dearborn, MI 48121, 313/271-1500)

-1-3 42nd Annual Frequency Control Symposium
Stouffer Harborplace Hotel, Baltimore (Frequency Control Symposium, PO Box 826, Belmar, NJ 07719)

-2-3 1st International Conference on Industrial & Engineering and Applications of Artificial Intelligence and Expert Systems
University of Tennessee Space Institute (Richard Roberts, University of Tennessee Space Institute, Tullahoma, TN 37388, 615/455-0631)

-5-9 IEEE Computer Society Conference on Computer Vision & Pattern Recognition
University of Michigan Campus, Ann Arbor (Ramesh Jain, Dept. of EECS, 3215 EECS Bldg, University of Michigan, Ann Arbor, MI 48109-2122, 313/763-0387)

-5-9 Human Factors and Power Plants Conference
Doubletree Inn at Fisherman's Wharf, Monterey, CA (H. E. Price, Essex Corp., 333 N. Fairfax Street, Alexandria, VA 22314, 703/548-4500)

-6-10 1988 IEEE IAS Pulp & Paper Industry Technical Conference
Hyatt Regency, Milwaukee (David T. Rollay, Conference Chairman, Allen-Bradley Co., 1201 South 2nd Street, Milwaukee, WI 53204, 414/382-2163)

-6-10 1988 AP-S International Symposium and URSI/USNC Radio Science Meeting
Sheraton University Inn and Conference Center, Syracuse (Prof. A. T. Adams, Chairman, Syracuse University, 111 Link Hall, Syracuse, NY 13210, 315/423-4397)

-7-8 Installation Engineering: Designing & Maintaining Successful Systems
Savoy Place, London (IEE Conference Services, Savoy Place, London, WC2R OBL, 01-240 1871 ext. 222)

-7-9 1988 International Symposium on Circuits and Systems (ISCAS '88)
Helsinki University of Technology, Espoo Finland (Dr. Olli Simula, Helsinki University of Technology, Dept. of Technical Physics, SF-02150 Espoo 15, Finland or Dr. Markku Renfors, Secretary Tampere University of Tech., PO Box 527, SF-33101 Tampere, Finland, +358 31 162696)

-7-9 ATE & Instrumentation Conference East
World Trade Center, Boston (MG Expositions Group, 1050 Commonwealth Avenue, Boston, MA 02215, 617/232-EXPO)

-7-9 Silicon Mountain Symposium
Colorado Springs (Jil Goebel, Colorado Springs MARCOM Network, PO Box 49014, Colorado Springs, CO 80949-9014, 303/576-7140)

-8-10 Caribbean ExpoCom
Caribe Hilton, San Juan, Puerto Rico (William Warens, LATCOM, PO Box 4749, Arlington, VA 22204)

-8-10 Symposium on the Engineering of Computer Based Medical Systems
Hyatt Regency Hotel, Minneapolis (John M. Long, Ed. D., 2829 University Avenue SE, Suite 408, Minneapolis, MN 55414, 612/627-4850)

-8-11 Communic Asia/Infotech Asia 88
World Trade Centre, Singapore (Gerald G. Kallman, Kallman Associates, Five Maple Court, Ridgewood, NJ 07450-4431, 201/652-7070)

-8-16 ACM/IEEE Design Automation Conference
Anaheim Convention Center, Anaheim (Design Automation Conference, PO Pistilli, MP Associates, 7366 Old Mill Trail, Boulder, CO 80301, 303/530-4562)

-12-15 Design Automation Conference
Anaheim Convention Center, Anaheim (MP & Associates, 7490 Clubhouse Rd., Suite 102, Boulder, CO 80301, 303/530-4333)

-12-15 1988 International Conference on Communications (ICC '88)
Wyndham Franklin Plaza Hotel, Philadelphia (G. William Ruhl, Bell Pennsylvania, 8th floor, 210 Pine Street, Harrisburg, PA 17101, 717/255-8643)

-12-18 1988 American Control Conference
Atlanta Hilton & Towers, Atlanta (Judy Book, General Chairman, 1373 Emory Road, Atlanta, GA 30306)

-13-14 Engineers Expo Career Open House
Albuquerque, NM (Engineers Expo, 2367 Auburn Avenue, Cincinnati, OH 45219, 513/721-3030)

-13-17 8th International Conference on Distributed Computing Systems
Fairmont Hotel, San Francisco (8ICDCS, Computer Society of the IEEE, 1730 Massachusetts Ave NW, Washington, DC 20036-1903, 202/371-1013)

-13-18 EP China '88
China International Exhibition Centre, Beijing, P.R.C. (Gerald G. Kallman, Kallman Associates, Five Maple Court, Ridgewood, NJ 07450-4431, 201/652-7070)

-14-16 2nd SAMPE Electronics Materials Processes Conference
Red Lion Inn, Seattle, Washington (Marge Smith, SAMPE, International Business Office, 843 West Glentana (Box 2459), Covina, CA 91722, 818/331-0616)

-14-16 NEPCON East 1988
Bayside Expo Center, Boston (Janet Schafer, Cahners Exposition Group, Cahners Plaza, 1350 E. Touhy Avenue, PO Box 5060, Des Plaines, IL 60018, 312/299-9311)

-15-17 1988 Vehicular Technology Conference
Holiday Inn-Center City, Philadelphia (John Galanti, Conference Chairman, Bell Atlantic Mobile Systems, 180 Mount Airy Road, Basking Ridge, NJ 07920, 201/953-2212, or Robert T. Swint, Arrangements Chairman, Bell of Pennsylvania, 215/466-3284)

-19-24 1988 International Symposium on Information Theory
International Conference Center, Kobe, Japan (Prof. Toshihiko Namekawa, Dept. of Communication Engr., Osaka University, 2-1, Yamada-Oka Suita, Osaka 565 Japan or Daniel J. Costello, Jr., Dept. of Electrical Engr., University of Notre Dame, Notre Dame, IN 46556, 219/239-7703)

-21-23 International Conference on Private Switching Systems and Networks
Savoy Place, London (IEE Conference Services, Savoy Place, London, WC2R OBL, 01-240 1871 ext. 222)

-21-23 PC Expo
Jacob K. Javits Convention Center, New York (Jim Mion or Annie Zdinak, 333 Sylvan Avenue, Englewood Cliffs, NJ 07632, 800/922-0324, 201/569-8542)

-21-23 Failure Avoidance/Failure Analysis for VLSI Circuits
Minneapolis (DM Data Inc., 6900 E. Camelback Rd., Suite 1000, Scottsdale, AZ 85251, 602/945-9620)

-24 How to Save Thousands of Dollars on Your Semiconductor Purchases and System Designs
Minneapolis (DM Data Inc., 6900 E. Camelback Rd., Suite 1000, Scottsdale, AZ 85251, 602/945-9620)

-27-28 Engineers Expo Career Open House
Cleveland/Akron/Canton (Engineers Expo, 2367 Auburn Avenue, Cincinnati, OH 45219, 513/721-3030)

-27-30 18th International Symposium on Fault-Tolerant Computing
Keio Plaza Hotel, Tokyo (Yasuo Komamiya, 2-4-8 Kikuna, Kohoku-ku, Yokohama 222, Japan, 044-911-8181)

-27-30 5th International Conference on Dielectric Materials, Measurements & Applications
University of Kent at Canterbury, England (IEE Conference Services, Savoy Place, London WC2R OBL, 1-240 1871 ext. 222)

-30-July 2 Semicon Osaka
The Intex Center, Osaka, Japan (Bill Galamea, Semiconductor Equipment & Materials Institute, Inc., 805 E. Middlefield Rd., Mountain View, CA 94043, 415/964-5111)

SUNDAY	MONDAY	TUESDAY	WEDNESDAY	THURSDAY	FRIDAY	SATURDAY
					1	2
3	4 INDEPENDENCE DAY	5	6	7	8	9
10	11	12	13	14	15	16
17	18	19	20	21	22	23
24 31	25	26	27	28	29	30

- 10-15 AEA/Santa Clara Management Development Program**
Santa Clara (Mary Healy, AEA, 5201 Great America Parkway, Santa Clara, CA 95054, 408/987-4229)
- 11-13 National FinCom**
Jacob K. Javits Convention Center, New York (Jim Mion or Annie Zdinak, 333 Sylvan Avenue, Englewood Cliffs, NJ 07632, 800/237-7601, 201/569-6474)
- 11-15 2nd IEE/BCS Conference on Software Engineering 88**
University of Liverpool, England (IEE Conference Services, Savoy Place, London WC2R OBL, 01-240-1871 ext. 222)
- 12-15 INTERMAG '88 - Fourth Joint MMM-Intermag Conference**
Hyatt Regency Vancouver and Hotel Vancouver, Vancouver, British Columbia (Diane Suiters, Courtesy Associates, 655-15th Street NW, Washington, DC 20005, 202/639-5088)
- 13-15 3rd International Conference on Power Electronics and Variable-Speed Drives**
London (IEE Conference Services, Savoy Place, London WC2R OBL, 01-240-1871 ext. 222)
- 17-22 AEA Manufacturing Strategy Program**
Santa Cruz, CA (Stepahany Nickel, AEA, 5201 Great America Parkway, Santa Clara, CA 95054, 408/987-4239)
- 18-19 Engineers Expo Career Open House**
Melbourne/Orlando, FL (Engineers Expo, 2367 Auburn Avenue, Cincinnati, OH 45219, 513/721-3030)
- 19-21 2nd Workshop on Software Testing & Verification**
Rimrock Inn, Banff, Alberta, Canada (Lee White, Dept of CS, University of Alberta, Edmonton, Alberta, Canada, T6G 2H1, 403/432-4589)
- 24-29 1988 Power Engineering Society Summer Meeting**
Hilton and Marriott Hotels, Portland, OR (S. A. Annestrand, Bonneville Power Adm., Box 3621, Portland, OR 97208, 503/230-4503)
- 25-27 Summer Computer Simulation Conference**
Seattle, Washington (SCS, P.O. Box 17900, San Diego, CA 92117, 619/277-3888)
- 25-28 Navy Micro/OA '88 Conference**
San Diego (NARDAC San Diego, NAS North Island, Building 1482, San Diego, CA 92135-5110)
- 31-August 12 AEA/Stanford Executive Institute for Management of High-Technology Companies**
Stanford, CA (Mary Horngren Frost, AEA, 5201 Great America Parkway, Santa Clara, CA 95054, 408/987-4285)

Your next destination:



The ACL Computer Age.

The future belongs to computers and peripherals built with RCA Advanced CMOS Logic (ACL).

The pressure is on to make your systems smaller, faster, cheaper.

Some of your competitors are doing just that by incorporating ACL into their new designs. If you want to stay on the fast track, you can't afford not to consider ACL for your new designs.

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Advanced CMOS Logic gives you high speed (less than 3ns propagation delay with our AC00 NAND gate) and 24 mA output drive current.

But unlike FAST, it gives you a whole new world of design opportunity for computers, peripherals, telecommunications and other speed-intensive applications.

ACL dissipates less than 1/8 Watt while switching, compared to 1/2 Watt for a FAST IC (octal transceiver operating at 5 MHz). And quiescent power savings are even more dramatic: ACL idles at a small fraction of the power of a FAST IC.

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In Europe, call: Brussels, (02) 246-21-11; Paris, (1) 39-46-57-99; London, (276) 68-59-11; Milano, (2) 82-291; Munich, (089) 63813-0; Stockholm (08) 793-9500.



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In addition, ACL offers balanced propagation delay, superior input characteristics, improved output source current, low ground bounce and a wider operating supply voltage range.

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For more information, call toll-free 800-443-7364, extension 24. Or contact your local GE Solid State sales office or distributor.

SUNDAY	MONDAY	TUESDAY	WEDNESDAY	THURSDAY	FRIDAY	SATURDAY
	1	2	3	4	5	6
7	8	9	10	11	12	13
14	15	16	17	18	19	20
21	22	23	24	25	26	27
28	29	30	31			

1-5 15th Annual Conference & Exhibition on Computer Graphics & Interactive Techniques (Siggraph '88)

Georgia World Congress Center, Atlanta (University of Waterloo, Department of Computer Science, Waterloo, Ontario, Canada, N2L 3G1, 519/888-4534)

•2 Basic IC Technology

San Jose (ICE, 15022 N. 75th Street, Scottsdale, AZ 85260, 602/998-9780)

•2-4 2nd SAMPE Metals & Metals Processing Conference

Souffer Hotel, Dayton, OH (Marge Smith, SAMPE, International Business Office, 843 West Glentana (Box 2459), Covina, CA 91722, 818/331-0616)

•2-4 1988 IEEE International Symposium on Electromagnetic Compatibility

Westin Hotel, Seattle (Donald Weber, Conference Chairman, 131 SW 156th Street, Seattle, Washington 98166, 206/244-0952)

•3 Mid-Term '88

San Jose (ICE, 15022 N. 75th Street, Scottsdale, AZ 85260, 602/998-9780)

•3-5 1988 IEEE 4th Workshop on Spectrum Estimation & Modeling

Spring Hill Conference Center, Minneapolis (Kevin Buckley, Chairman, Department of Electrical Engineering, University of Minnesota, Minneapolis, MN 55455, 612/625-7319)

•8-12 1988 IEEE International Conference on Systems, Man and Cybernetics

Beijing Shenyang, China (A. Terry Bahill, University of Arizona, Systems & Industrial Engineering, Tucson, AZ 85721, 602/621-6561)

•9 Basic IC Technology

Scottsdale, AZ (ICE, 15022 N. 75th Street, Scottsdale, AZ 85260, 602/998-9780)

•10 Mid-Term '88

Scottsdale, AZ (ICE, 15022 N. 75th Street, Scottsdale, AZ 85260, 602/998-9780)

•15-16 Engineers Expo Career Open House

Colorado Springs/Denver (Engineers Expo, 2367 Auburn Avenue, Cincinnati, OH 45219, 513/721-3030)

•16 Basic IC Technology

Boston (ICE, 15022 N. 75th Street, Scottsdale, AZ 85260, 602/998-9780)

•17 Mid-Term '88

Boston (ICE, 15022 N. 75th Street, Scottsdale, AZ 85260, 602/998-9780)

•23 Basic IC Technology

Newport Beach, CA (ICE, 15022 N. 75th Street, Scottsdale, AZ 85260, 602/998-9780)

•24 Mid-Term '88

Newport Beach, CA (ICE, 15022 N. 75th Street, Scottsdale, AZ 85260, 602/998-9780)

•30-September 1 MIDCON '88

Dallas Convention Center, Dallas (Alexes Razevich, Electronic Conventions Mgmt., 8110 Airport Blvd., Los Angeles, CA 90045, 800/421-6816)

30-September 2 ICO Topical Meeting on Optical Computing

Orsay, France (Prof. S. Lowenthal, Institut D'Optique B.P. 43, 91406 Orsay, Cedex, France)

31-September 2 Factory 2000: Integrating Information and Material Flow

Churchill College, Cambridge, England (The Conference Secretariat, Institution of Electronic and Radio Engineers, Savoy Hill House, Savoy Hill, London WC2R 0JD, England)

SUNDAY	MONDAY	TUESDAY	WEDNESDAY	THURSDAY	FRIDAY	SATURDAY
				1	2	3
4	5 LABOR DAY	6	7	8	9	10
11	12 ROSH HASHANAH	13	14	15	16	17
18	19	20	21 YOM KIPPUR	22	23	24
25	26	27	28	29	30	

- 7-8 Capitol Microcomputer User Forum**
Washington Convention Center, Washington, DC (Jackie Voight, National Trade Association, 800/638-8510 or 703/683-8500)
- 7-15 1988 International Test Conference**
Sheraton Washington, Washington, DC (Doris Thomas, ITC, PO Box 264, Mt. Freedom, NJ 07970, 201/267-7120)
- 8 OEM Peripheral ICC**
Newton Marriott, Newton, MA (Susie Ring, 3151 Airway Avenue, #C-2, Costa Mesa, CA 92626, 714/957-0171)
- 11-15 Electromagnetic Compatibility**
University of York, England (The Conference Secretariat, Institution of Electronic and Radio Engineers, Savoy Hill House, Savoy Hill, London WC2R 0JD, England)
- 11-15 14th European Conference on Optical Communication (ECOC 88)**
Brighton, England (IEE Conference Services, Savoy Place, London WC2R 0BL, England, 01-240 1871, ext. 222)
- 11-16 1988 International Symposium on Subscriber Loops and Services (ISLS '88)**
Sheraton Hotel, Boston (C. William Anderson, New England Telephone Co., 350 Cochituate Road, Room 206, Framingham, MA 01701, 617/879-9000)
- 12-13 Engineers Expo Open House**
Long Island (Engineers Expo, 2367 Auburn Avenue, Cincinnati, OH 45219, 513/721-3030)
- 12-15 1988 Petroleum & Chemical Industry Conference PCIC '88**
Dallas (Thomas Pearson, ARCO Oil & Gas Company, PO Box 2819, Dallas, TX 75221, 214/880-4782)
- 12-15 Fabricating Composites '88 Conference & Exposition**
Adam's Mark Hotel, Philadelphia (Nancy LePage, Society of Manufacturing Engineers, One SME Drive, PO Box 930, Dearborn, MI 48121, 313/271-1500)
- 12-15 1988 Annual International Test Conference**
Sheraton Washington, Washington, DC (ITC '88, Computer Society of the IEEE, 1730 Massachusetts Avenue NW, Washington, DC 20036-1903, 202/371-1013)
- 12-16 1988 2nd International Conference on Properties and Applications of Dielectric Materials**
Tsinghua University, Beijing, P.R. of China (Assoc. Prof. Zhu Deheng, Tsinghua University, Beijing, P.R. of China, 282451-2166)
- 13-15 Metal Matrix Composites '88 Conference**
Adam's Mark Hotel, Philadelphia (Nancy LePage, Society of Manufacturing Engineers, One SME Drive, PO Box 930, Dearborn, MI 48121, 313/271-1500)
- 13-15 Semicon East**
Bayside Expo, Boston (Bill Galarnea, Semiconductor Equipment & Materials Institute, Inc., 805 E. Middlefield Rd., Mountain View, CA 94043, 415/964-5111)
- 13-15 Failure Avoidance/Failure Analysis for VLSI Circuits**
Boston (DM Data Inc., 6900 E. Camelback Rd., Suite 1000, Scottsdale, AZ 85251, 602/945-9620)
- 15 OEM Peripheral ICC**
Frankfurt Sheraton, Frankfurt (Susie Ring, 3151 Airway Avenue, #C-2, Costa Mesa, CA 92626, 714/957-0171)
- 15-16 38th Annual Broadcast Symposium**
Washington Hotel, Washington, DC (Mr. Otto R. Claus, WBAL-TV, 3800 Hooper Avenue, Baltimore, MD 21211, 301/338-6455)
- 16 How to Save Thousands of Dollars on Your Semiconductor Purchases and System Designs**
Boston (DM Data Inc., 6900 E. Camelback Rd., Suite 1000, Scottsdale, AZ 85251, 602/945-9620)
- 18-21 IEEE Artificial Neural Networks Conference**
Sheraton International Conference Center, Reston, VA (Dr. Kamal Karma, 823 Fiegler Road, Gaithersburg, MD 20879, 301/984-7657)
- 19-22 Digital Processing of Signals in Communications**
University of Loughborough, UK (The Conference Secretariat, Institution of Electronic and Radio Engineers, Savoy Hill House, Savoy Hill, London WC2R 0JD, England)
- 20 OEM Peripheral ICC**
Stockholm Sheraton, Stockholm (Susie Ring, 3151 Airway Avenue, #C-2, Costa Mesa, CA 92626, 714/957-0171)
- 20-22 NetWorld**
Infomart, Dallas (Jim Mion or Annie Zdinak, 333 Sylvan Avenue, Englewood Cliffs, NJ 07632, 800/526-3247 or 201/569-6406)
- 20-22 PCB Expo 1988**
Radisson Hotel South, Minneapolis, (Heidi Hogarath, 1790 Hembree Rd., Alpharetta, GA 30201, 404/475-1818)
- 22 IEEE Videoconferences: Photonic Switching**
IEEE Continuing Education Dept., 445 Hoes Lane, Piscataway, NJ 08854-4150, 201/981-0060 ext. 412)
- 23-27 International Broadcasting Convention**
Brighton, England (IBC Secretariat, C/O Conference Services, IEE, Savoy Place, London WC2R 0BL, England, 01-240 1871, ext. 222)
- 26-27 North American Power Symposium**
Purdue University, West Lafayette, Indiana (G. T. Heydt, Purdue University, Dept. of Electrical Engineering, West Lafayette, Indiana 47907, 317/494-3520)
- 26-28 1988 34th IEEE Holm Conference on Electrical Contacts**
San Francisco Hilton & Tower, San Francisco (Registrar, IEEE Headquarters, 345 East 47th Street, New York, NY 10017-2394)
- 27 OEM Peripheral ICC**
Hilton International, London (Susie Ring, 3151 Airway Avenue, #C-2, Costa Mesa, CA 92626, 714/957-0171)
- 27-29 FABTECH West Conference & Exposition**
Anaheim Convention Center, Anaheim (Nancy LePage, Society of Manufacturing Engineers, One SME Drive, PO Box 930, Dearborn, MI 48121, 313/271-1500)
- 27-29 Finishing West Conference**
Anaheim Convention Center, Anaheim (Nancy LePage, Society of Manufacturing Engineers, One SME Drive, PO Box 930, Dearborn, MI 48121, 313/271-1500)
- 27-29 20th SAMPE International Technical Conference**
Hyatt Regency Hotel, Minneapolis (Marge Smith, SAMPE, International Business Office, 843 West Glentana (Box 2459), Covina, CA 91722, 818/331-0616)
- 27-29 Buscon '88 East**
Penta Hotel, New York (Anne Weber, 17100 Norwalk Blvd., Suite 116, Cerritos, CA 90701, 213/402-1618)
- 27-29 Power Electronics '88 East**
Penta Hotel, New York (Anne Weber, 17100 Norwalk Blvd., Suite 116, Cerritos, CA 90701, 213/402-1618)
- 27-30 AEA Executive Forum for Senior HR Professionals**
San Diego (Diane McIntyre, AEA, 5201 Great America Parkway, Santa Clara, CA 95054, 408/987-4227)
- 28-29 California Electronics Show**
The Pasadena Center, Pasadena, CA (Harry Schwartz, Epic Enterprises, Inc. 3838 Camino Del Rio North, Suite 164, San Diego, CA 92108, 619/284-9268)

SUNDAY	MONDAY	TUESDAY	WEDNESDAY	THURSDAY	FRIDAY	SATURDAY
						1
2	3	4	5	6	7	8
9	10 COLUMBUS DAY	11	12	13	14	15
16	17	18	19	20	21	22
23 30	24 31 HALLOWEEN	25	26	27	28	29

-2-5 Mexican IEEE Annual Convention & Expo
Plaza Hotel, Acapulco (William Warnes, LATCOM, PO Box 4749, Arlington, VA 22204, 703/685-0600)

-2-6 Industry Applications Society Annual Meeting
Pittsburgh Hilton, Pittsburgh (Charles E. Gray, General Electric Co., Two Gateway Center, Pittsburgh, PA 15222, 412/566-4173)

-2-6 1988 International Conference on Computer Design
Rye Town Hilton, Rye Brook, NY (ICCD 1988, 1730 Massachusetts Avenue NW, Washington, DC 20036-1903, 202/371-1013)

-2-6 Joint Power Generation Conference
Wyndham Franklin Plaza Hotel, Philadelphia (M.W. Migliaro, Ebasco Services, Inc., 2 World Trade Center, New York, NY 10048-0752, 212/839-2245)

-3-4 Engineers Expo Career Open House
Houston/Johnson Space Center (Engineers Expo, 2367 Auburn Avenue, Cincinnati, OH 45219, 513/721-3030)

-3-5 1988 IEEE Ultrasonics Symposium
McCormick Center Hotel, Chicago (William D. O'Brien, Jr., General Chairman, Bioacoustics Research Lab, University of Illinois, Urbana, IL 61801)

-4 Semiconductor Packaging
Boston (ICE, 105022 N. 75th Street, Scottsdale, AZ 85260, 602/998-9780)

-4-6 AUTOTESTCON '88
Hyatt Regency/Holiday Inn Downtown, Minneapolis (Lee C. Paulson, Honeywell, Inc., MN15-2733, 1625 Zarthan Avenue S., Minneapolis, MN 55416, 612/542-4841)

-4-6 1988 International Display Research Conference
Hyatt Islandia, San Diego (Ms. Hildegarde Hammond, Palisades Institute for Research Services, Inc., 201 Varick St., Room 1140, New York, NY 10014, 212/620-3388)

-4-6 Adhesives, Surface Coatings & Encapsulants 1988 (ASE)
Metropole Exhibition Centre, Brighton, England (Network Events, Ltd., Printers Mews, Market Hill, Buckingham, MK18 1JX, UK, 0280 815226)

-4-6 Electronic Imaging Conference East
World Trade Center, Boston (MG Expositions Group, 1050 Commonwealth Avenue, Boston, MA 02215, 617/232-EXPO)

-4-6 National CASECON
Jacob K. Javits Convention Center, New York (Jim Mion or Annie Zdinak, 333 Sylvan Avenue, Englewood Cliffs, NJ 07632, 800/922-0324, or 201/569-8542)

-5-7 Practical IC Fabrication
Boston (ICE, 105022 N. 75th Street, Scottsdale, AZ 85260, 602/998-9780)

-9-13 International Conference on Computer Languages
Castle Premier, Miami Beach (Pei Hsia, University of Texas/Arlington, Computer Science, 2100 Oak Bluff Drive, Arlington, TX 76001, 817/273-3785)

-10-12 PC Expo
McCormick Place North, Chicago (Jim Mion or Annie Zdinak, 333 Sylvan Avenue, Englewood Cliffs, NJ 07632, 800/922-0324 or 201/569-8542)

-11-13 Adhesives '88 Conference & Exposition
Hyatt Regency-O'Hare, Chicago (Nancy LePage, Society of Manufacturing Engineers, One SME Drive, PO Box 930, Dearborn, MI 48121, 313/271-1500)

-13-15 Northeast Computer Faire
World Trade Center, Boston (Peter B. Young, The Interface Group, Inc., 300 First Avenue, Needham, MA 02194, 617/449-6600)

-17-18 Engineers Expo Career Open House
Dayton/Cincinnati (Engineers Expo, 2367 Auburn Avenue, Cincinnati, OH 45219, 513/721-3030)

-17-19 ESC '88
Orlando, FL (Joseph Gauthier, 919B Willowbrook Dr., Huntsville, AL 35802, 205/881-0947)

-17-19 CONVERGENCE '88 International Congress on Transportation Electronics
Hyatt Regency Hotel, Fairlane Towne Center, Dearborn, MI (Oliver T. McCarter, Advanced Engineering Staff, APE-S1-Council, 30200 Mound Road, Warren, MI 48090-9010, 313/986-8048)

-17-19 4th International Conference on Satellite Systems for Mobile Communications & Navigation
London (IEE Conference Services, Savoy Place, London WC2R 0BL, England, 01-240 1871, ext. 222)

-17-21 4th Expert Systems in Government Conference
Washington, DC (ESIG '88, Computer Society of the IEEE, 1730 Massachusetts Avenue NW, Washington, DC 20036-1903, 202/371-1013)

-18-20 Boston Manufacturing Productivity Conference & Advanced Productivity Exposition (APEX)
Hynes Convention Center, Boston (Nancy LePage, Society of Manufacturing Engineers, One SME Drive, PO Box 930, Dearborn, MI 48121, 313/271-1500)

-18-20 TESTMEX 1988
Business Design Centre, London (Network Events, Ltd., Printers Mews, Market Hill, Buckingham MK18 1JX, UK, 0280 815226)

-18-20 Failure Avoidance/Failure Analysis for VLSI Circuits
Washington, DC (DM Data, Inc., Ste 1000, Scottsdale AZ, 85251, 602/945-9620)

-18-22 Ceramitec '88
Munich Trade Fair Centre, Munich (Gerald Kallman, Kallman Associates, Five Maple Court, Ridgewood, NJ 07450-4431, 201/652-7070)

-19-20 Semicon South West
Infomart, Dallas (Bill Galamea, Semiconductor Equipment & Materials Institute, Inc., 805 E. Middlefield Rd., Mountain View, CA, 415/964-5111)

-19-21 Canadian Communications and Energy Conference
Queen Elizabeth Hotel, Montreal, Canada (IEEE Canadian Region Office, 7061 Yonge Street, Thornhill, Ontario, L3T 2A6 Canada, 416/881-1930)

-20 IEEE Videoconferences: Photonic Switching
IEEE Continuing Education Dept., 445 Hoes Lane, Piscataway, NJ 08854-4150, 201/981-0060 ext. 412)

-21 How to Save Thousands of Dollars on Your Semiconductor Purchases and System Designs
Washington, DC (DM Data Inc., 6900 E. Camelback Rd., Suite 1000, Scottsdale, AZ 85251, 602/945-9620)

-21-23 RAINBOWfest
Hyatt Regency Princeton, Princeton, NJ (Ira D. Barsky, The Falsoft Building, 9509 U.S. Highway 42, PO Box 385, Prospect, KY 40059, 502/228-4492)

-23-26 1988 Military Communications Conference - MILCOM '88
Irvine Marriott, Irvine, CA (Robert North, TRW Electronic Systems Group, One Space Park, Redondo Beach, CA 90278, 213/536-2421)

-23-28 IPC Fall Meeting
Anaheim Marriott, Anaheim (Virginia Perry, IIPCE, 7380 N. Lincoln, Lincoln Wood, IL 60646)

-24-27 1988 Conference on Software Maintenance
Paradise Valley Resort, Scottsdale, AZ (Computer Society of the IEEE, 1730 Massachusetts Avenue NW, Washington, DC 20036-1903, 202/371-1013)

-24-28 AEA/Santa Clara Management Development Program
Santa Clara, CA (Mary Healy, AEA, 5201 Great America Parkway, Santa Clara, CA 95054, 408/987-4229)

-25-28 SYSTEC '88
Munich Trade Fair Centre, Munich (Gerald Kallman, Kallman Associates, Five Maple Court, Ridgewood, NJ 07450-4431, 201/652-7070)

-29-November 2 1988 International Telecommunications Conference (INTELEC '88)
Town & Country Hotel, San Diego (Chris Riddleberger, AT&T, Room 1a-306, 260 Cherry Hill Road, Parsippany, NJ 07054, 201/299-3428)

-31-November 2 AUTOFACT '88 Conference & Exposition
McCormick Place, Chicago (Nancy LePage, Society of Manufacturing Engineers, One SME Drive, PO Box 930, Dearborn, MI 48121, 313/271-1500)

SUNDAY	MONDAY	TUESDAY	WEDNESDAY	THURSDAY	FRIDAY	SATURDAY
		1	2	3	4	5
6	7	8 ELECTION DAY	9	10	11 VETERANS DAY	12
13	14	15	16	17	18	19
20	21	22	23	24 THANKSGIVING DAY	25	26
27	28	29	30			

-1-3 Toledo Manufacturing Productivity Conference & Advanced Productivity Exposition

SeaGate Centre, Toledo, OH (Nancy LePage, Society of Manufacturing Engineers, One SME Drive, PO Box 930, Dearborn, MI 48121, 313/271-1500)

-2-3 Failure Analysis Avoidance

Scottsdale, AZ (ICE 105022 N. 75th Street, Scottsdale, AZ 85260, 602/998-9780)

-2-4 1988 IEEE Nuclear Science Symposium

Sheraton Twin Towers (Edward J. Barsotti, Fermilab, PO Box 500, Batavia, IL 60510, 312/840-4061)

-2-6 Communications 88/ Turkey

Istanbul Hilton Convention & Exhibition Centre, Turkey (Gerald Kallman, Kallman Associates, Five Maple Court, Ridgewood, NJ 07450-4431, 201/652-7070)

-7-8 International Conference on Refurbishment of Power Station Electrical Plant

London (IEE Conference Services, Savoy Place, London WC2R OBL, England, 01-240 1871, ext. 222)

-8-10 Semicon Korea

Korea Exhibition Center, Seoul, Korea (Bill Galarnea, Semiconductor Equipment & Materials Institute, Inc., 805 E. Middlefield Rd., Mountain View, CA, 415/964-5111)

-8-12 Electronica

Munich Trade Fair Centre, Munich (Gerald Kallman, Kallman Associates, Five Maple Court, Ridgewood, NJ 07450-4431, 201/652-7070)

-10-11 2nd International Symposium on Interoperable Information Systems

Science Museum of Japan Science Foundation, Tokyo (Prof. Hideo Aiso, Dept. of EE, Keio University, 3-14-1, Hiyosi, Kohoku, Yokohama, Karagawa, 223 Japan, 044-63-1141 ext. 3320)

-12-18 ACM/IEEE Computer Society FJCC

Buena Vista Palace, Orlando, FL (FJCC Computer Society of the IEEE, 1730 Massachusetts Avenue NW, Washington, DC 20036-1903, 202/371-1013)

-13-17 Saudi Elenex '88

Riyadh Exhibition Centre, Riyadh, Saudi Arabia (Gerald Kallman, Kallman Associates, Five Maple Court, Ridgewood, NJ 07450-4431, 201/652-7070)

-14-16 ATE '88 (Paris) Automatic Testing and Test Instrumentation

Palais des Congres, Paris (Network Events, Ltd., Printers Mews, Market Hill, Buckingham MK18 1JX, UK, 0280 815226)

-14-18 Supercomputing '88

Hyatt Orlando, Kissimmee, FL (George Michael, Lawrence Livermore Labs., PO Box 808, L-306, Livermore, CA 94550, 415/422-4239)

-15-17 Wescon/88

Anaheim Convention Center, Anaheim (Alexis Razevich, Electronic Conventions Management, 8110 Airport Blvd., Los Angeles, CA 90045, 213/772-2965)

-15-17 Electronic Displays (ED88)

Kensington Exhibition Centre, London (Network Events, Ltd., Printers Mews, Market Hill, Buckingham MK18 1JX, UK, 0280 815226)

-15-17 Image Processing

Kensington Exhibition Centre, London (Network Events, Ltd., Printers Mews, Market Hill, Buckingham MK18 1JX, UK, 0280 815226)

-15-17 Interactive 1988

Kensington Exhibition Centre, London (Network Events, Ltd., Printers Mews, Market Hill, Buckingham MK18 1JX, UK, 0280 815226)

-18-21 Argentina ComExpo International Computer/Communications Expo

Buenos Aires, Argentina (William Warnes, LATCOM, PO Box 4749, Arlington, VA 22204, 703/685-0600)

-22-24 4th International Conference on Electrical Safety in Hazardous Areas

Savoy Place, London (IEE Conference Services, Savoy Place, London WC2R OBL, England, 01-240 1871, ext. 222)

-23-25 Semicon Japan

Tokyo International Trade Center, Tokyo (Bill Galarnea, Semiconductor Equipment & Materials Institute, Inc., 805 E. Middlefield Rd., Mountain View, CA, 415/964-5111)

-23-27 Elenex Turkey 88

Istanbul Hilton Convention And Exhibition Centre, Istanbul (Gerald Kallman, Kallman Associates, Five Maple Court, Ridgewood, NJ 07450-4431, 201/652-7070)

-28-30 International Conference on Overhead Line Design and Construction: Theory and Practice (up to 150 kv)

Savoy Place, London (IEE Conference Services, Savoy Place, London WC2R OBL, England, 01-240 1871, ext. 222)

-28-December 1 Global Telecommunications Conference - GLOBECOM '88

Diplomat Hotel, Ft. Lauderdale, FL (Richard Blake, Siemens Communications Systems, Inc., 5500 Broken Sound Blvd., Boca Raton, FL 33431, 305/994-7706)

DECEMBER 1988

EDN

SUNDAY	MONDAY	TUESDAY	WEDNESDAY	THURSDAY	FRIDAY	SATURDAY
				1	2	3
4 CHANU- KAH	5	6	7	8	9	10
11	12	13	14	15	16	17
18	19	20	21	22	23	24
25 CHRIST- MAS DAY	26	27	28	29	30	31

•12-14 1988 Winter Simulation Conference

San Diego, CA (John C. Comfort, Dept. of Mathematical Sciences, Florida International University, Miami, FL 33199, 305/554-2015)

•5-8 Annual Infomatics '88 Conference

Hong Kong (Don Avedon, International Information, Management Congress, PO Box 34404, Bethesda, MD 20817, 301/983-0604)

•6-8 Composites in Manufacturing '88 Conference & Exposition

Convention Center, Long Beach, CA (Nancy LePage, Society of Manufacturing Engineers, One SME Drive, PO Box 930, Dearborn, MI 48121, 313/271-1500)

•6-9 1988 IEEE International Conference on Decision and Control

Hyatt Regency Austin, Austin, TX (Michael P. Polis, National Science Foundation, 1800 G Street, Washington, DC 20550, 202/357-9618)

•7 IEEE Videoconferences: Supercomputers

(IEEE Continuing Education Dept., 445 Hoes Lane, Piscataway, NJ 08854-4150, 201/981-0060 ext. 412)

•7-9 Practical IC Fabrication

Orlando, FL (ICE 105022 N. 75th Street, Scottsdale, AZ 85260, 602/998-9780)

•11-14 1988 IEEE International Electron Devices Meeting

San Francisco Hilton, San Francisco (Melissa Widekehr, c/o Courtesy Associates, Inc., 655 15th Street NW, Suite 3000, Washington, DC 20005, 202/347-5900)

•12-18 International Conference on Computer Vision

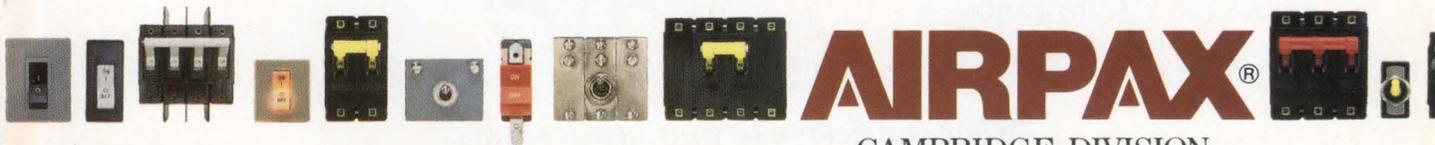
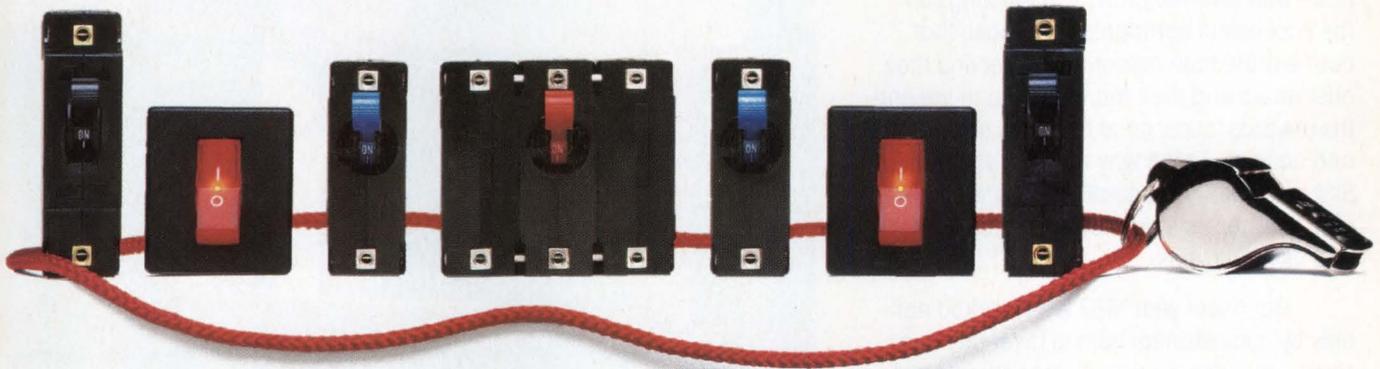
Tarpon Springs, FL (Ruzena Bajcsy, Computer & Info. Science Dept., University of Pennsylvania, 200 S. 33rd Street, Philadelphia, PA 19104-6389, 215/898-6222)

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CIRCLE NO 57

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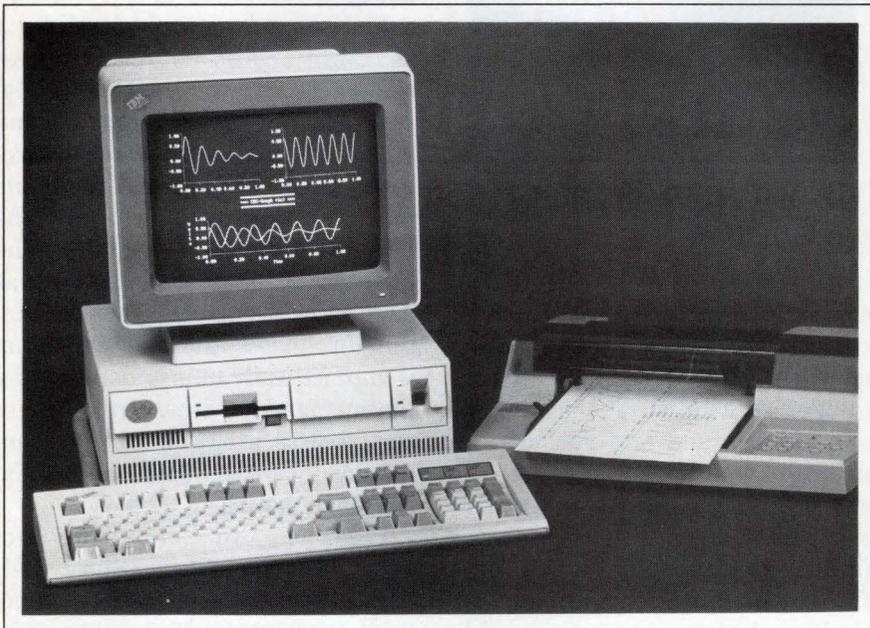


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PLOTTING SOFTWARE

- Produces high-resolution graphs on PS/2 microcomputers
- Converts graphics data to a format usable by the PS/2

Using the facilities of the machine's VGA (video graphics array) display board, CEC-Graph creates engineering graphics displays on the IBM PS/2 computer. The program is also compatible with the older CGA (color graphics adapter) and EGA (enhanced graphic adapter) display boards. Application programs written in Basic, Pascal, C, or Fortran can make use of the

package's ability to format, label, display, and plot graphics data. General-purpose commands permit the conversion of numeric or string data, acquired from GPIB- or RS-232C-based instruments, into the IEEE real-number format that is compatible with PS/2 programming languages. One command provides either a VGA display or directs the output to a plotter; the program automatically scales and labels graphs. \$95.

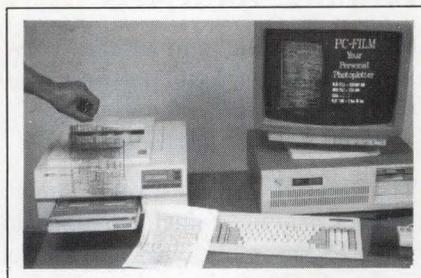
Capital Equipment Corp, 99 S Bedford St, Suite 107, Burlington, MA 01803. Phone (617) 273-1818.

Circle No 386

PHOTO-PLOT SYSTEM

- Makes rasterized image from Gerber file
- Creates prototype artwork on laser printer

The PC-Film photo-plotting package provides a rasterizer card that plugs into your IBM PC or compatible and software that interfaces the system to a 300-dot/in. laser printer. The system accepts a Gerber-type data file with as many as 255



apertures; converts such a file to a rasterized image; and transmits the rasterized image to a laser printer. The rasterizer card features 1.5M

bytes of onboard memory, which is sufficient to permit the creation of an 8x10½-in. image. You can use the system to create a paper plot to verify the accuracy of the Gerber file, and then create actual-size, pc-board artwork on film. A built-in feature that adjusts for film stretching and printer inaccuracies yields 4-mil accuracy at any point on a full page. The system will work with all word processors, and the vendor can supply direct-graphics drivers for AutoCAD, Ventura, and Publisher's Paintbrush software.

CAD Solutions Inc, 2880 Zanker Rd, Suite 103, San Jose, CA 95134. Phone (408) 943-1610.

Circle No 387

MENU BUILDER

- Lets you build custom menus for running applications
- Provides password facilities and lets you select screen colors

The Menu Works menu-building utility runs on IBM PCs, PS/2s, and compatibles equipped with hard disks. It facilitates operation of the PC for nontechnical users. You can set up a main menu that contains categories of programs, and sub-menus from which you can activate individual application programs. A password function lets you prevent unauthorized persons from running particular programs, viewing private menus, or changing the system configuration. The program lets you select any set of screen colors and automatically turns off the display if a user-defined period elapses without the occurrence of keystrokes. The utility eliminates the need to set up complex batch files; a single-keystroke selection from a menu lets you run as many as 15 separate programs and DOS commands. Special function keys display directories; give you immediate access to

on-line, context-sensitive help facilities; and let you set the time and date. \$59.95.

PC Dynamics Inc, 31332 Via Colinas, Suite 102, Westlake Village, CA 91362. Phone (818) 889-1741.

Circle No 388

8085 SIMULATOR

- Lets you debug 8085 software on your PC or compatible
- Provides on-line help

The VM85 training program runs on IBM PCs and compatibles and simulates the operation of an Intel 8085 μ P. You can write 8085 source code with any text editor and assemble the code with the CASM85 assembler program, which is included in the package. The simulator then loads the assembler-produced listing file and executes it. With the aid of the package's graphics displays, you can examine or alter memory locations, registers, and flags. You can single step through your program or you can set breakpoints and run the program at full speed until it reaches one of them. The simulator also lets you read from and write to I/O ports, and generate interrupts from the keyboard. To run the simulator, you'll need an IBM PC or compatible with at least one floppy-disk drive, 64k bytes of free memory, and DOS version 2.1 or higher. \$29.95.

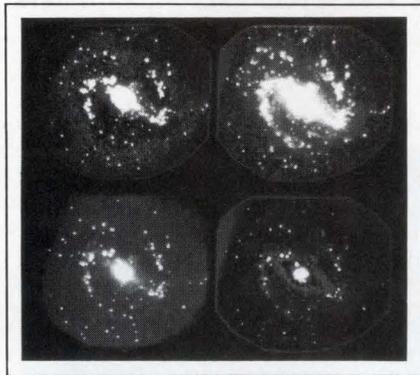
J-Tron Systems, Box 1232, Piscataway, NJ 08854.

Circle No 389

IMAGE SOFTWARE

- Lets you acquire images from video equipment and scanners
- Provides 250 image-manipulation and -analysis functions

The interactive DT/IDL image-processing software runs on a MicroVAX II workstation and provides easy access to 250 frame-grabbing, image-analysis, filtering, and plotting functions. The software performs typed or mouse-selected commands



immediately, but you can also group command sequences in files that automatically execute complex sequences. The interactive data language has English-like commands and syntax, and lets you use the package whether or not you are conversant in advanced mathematics or programming. The package's image-processing functions include frame-grabbing, convolution, FFT analysis, histogram creation, median filtering, zooming, plotting, and wrapping, rotating, or translating. You can create entirely new commands by combining the built-in commands, or you can write new function routines in any language supported by the VAX Calling Standard. To use the software, you need a MicroVAX II workstation equipped with an analog RGB monitor and the vendor's DT2651 High-Resolution Frame Grabber. \$3750.

Data Translation Inc, 100 Locke Dr, Marlboro, MA 01752. Phone (617) 481-3700. TLX 951646.

Circle No 390

ON-LINE MANUALS

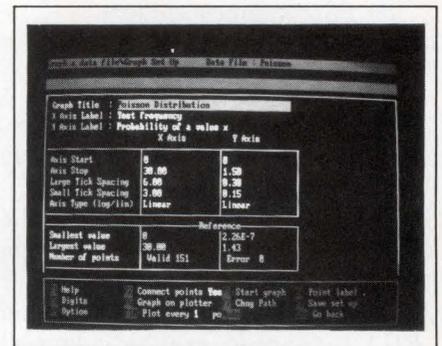
- Have hot keys that provide context-sensitive language help
- Available with reference databases for four languages

The Norton On-Line Programmer's Guides provide reference material for 8088 assembly language as well as for the Basic, Pascal, and C languages. You load a RAM-resident access program (which occupies 65k bytes) and a language database; while you're running an application

program, pressing Shift and F1 puts the language-database menu on the screen. You can call up the detailed reference entry or short definitions; or you can search for a key word or look for related cross-references. For the resident mode, you load the access program and guide before running any other program, and they remain available until you uninstall them. For the pass-through mode, you load the guide on the same command line as your application; when your application terminates, the access program is automatically uninstalled, freeing the memory for other programs to use. Access program and one language database, \$100; additional language databases, \$50 each.

Peter Norton Computing Inc, 2210 Wilshire Blvd, Suite 186, Santa Monica, CA 90403. Phone (213) 453-2361. TWX 650-226-1869.

Circle No 391



EQUATION PROCESSOR

- Evaluates keyboard-entered mathematical equations
- Automatically creates a data file for later use

Equator lets you enter equations from the keyboard of your IBM PC or compatible, evaluates them, and sends the results to a data file as well as to the screen or to a plotter. The program handles Greek and other special characters, extracts the value of common constants such as π or h (Planck's constant) from a table, and lets you assign values to variables. When producing a graph, the software automatically scales

the graph's axes to fit on the output medium that you select. In evaluating an equation, the program makes use of 36 operators and mathematical functions. You can also use previously evaluated equations as part of the current operation. The menu-driven command structure lets you define the equation and variables quickly and with minimal training. The program provides context-sensitive, on-line help. To run the program, your PC must have at least 512k bytes of RAM and run PC-DOS version 2.1 or higher. For plotting, you can use a Hewlett-Packard 7470 plotter or its equivalent, or a dot-matrix printer with graphics capability. \$79.

Pulse Research, Box 696, Shelburne, VT 05482. Phone (802) 985-2928.

Circle No 392

MATH SOFTWARE

- *Runs on the Apple Macintosh*
- *Provides wide range of math functions with graphics features*

MathView Professional is a stand-alone, interactive, mathematical package. It lets you evaluate and tabulate several variables simultaneously. You can plot as many as 10 functions simultaneously in Cartesian or polar coordinates, plot parametric relationships and raw data sets, and plot surfaces in three dimensions, with the option of removing hidden lines. Other functions include solving linear systems of equations or eigenvalues for symmetric matrices; computing direct and inverse FFTs; performing extensive matrix operations; solving nonlinear systems of equations, using either Newton's method or the Broyden algorithm; solving ordinary and partial differential equations; and computing integrals by various methods. In addition to providing a comprehensive set of descriptive statistical functions, the package lets you determine series coefficients and Chebyshev, Legendre, and Bessel elliptic functions. To run the package, you need a Macintosh equipped with at least 512k bytes of RAM, 128k-byte (or larger) ROMs, and two 800k-byte floppy-disk drives or a hard disk. \$249.95.

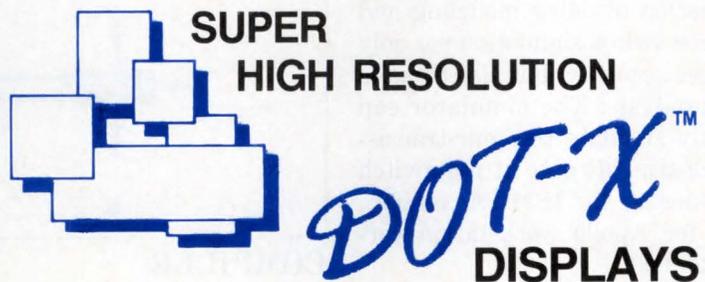
Brainpower Inc, 24009 Ventura Blvd, Suite 250, Calabasas, CA 91302. Phone (818) 884-6911.

Circle No 393

LOGIC SIMULATOR

- *Handles bidirectional, charge-sharing, and wired logic*
- *Can model both strong and weak transistors*

The DSIm event-driven, mixed-level simulator allows both switch- and gate-level simulation. Its features make it particularly suitable for



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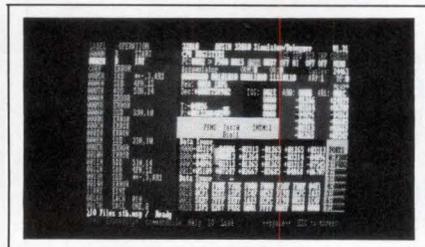
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CIRCLE NO 21

MOS simulation, but you can use it to simulate other digital logic families, too. The enhanced switch models can represent both strong and weak transistors, and can handle bidirectional, charge-sharing, and wired logic. Timing-violation models allow the program to detect setup and to hold violations at both the switch and the gate levels. A macro language lets you describe, in detail, a complex block of logic and to use this description as many times as you wish by calling the macro. According to the vendor, the combination of delay modeling and enhanced switch simulation not only increases accuracy, but also permits spike analysis. The simulator can correctly simulate the four-transistor exclusive-OR gate at the switch level. License for IBM PC version, \$2500; for Apollo workstation version, \$20,000.

Roche Systems Corp, 1705 N Rankin St, Appleton, WI 54911. Phone (414) 733-6077.

Circle No 394



DSP SIMULATORS

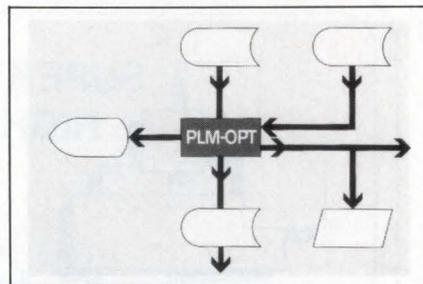
- Run on IBM PCs and compatibles
- Simulate TMS 32010 and TMS 32020 families of DSP chips

The AVSIM321 and AVSIM322 are software simulators/debuggers for the Texas Instruments 32010 and 32020 families of digital signal-processing chips. They run on an IBM PC or compatible and interactively execute object code under the control of a full-screen symbolic debugger. The screen display shows you the current instruction stream and the contents of registers, flags, and areas of data memory. You can ex-

amine and modify these at any time; by using an Undo key, you can back up, one instruction at a time, through recently executed instructions to determine where an error occurred. You can either issue commands from a menu structure or from a command line. \$379 each.

Avocet Systems Inc, Box 490, Rockport, ME 04856. Phone (207) 236-9055.

Circle No 395



COMPILER

- Provides support for 8051-family microcontrollers
- Is compatible with popular in-circuit emulators

The PLM-51 cross compiler, the A51 macro crossassembler, and a set of object format utilities run in an MS-DOS environment and cover all stages of software development for 8051, 8052, 8044, and SAB80515 μ controllers. All these software tools are compatible with popular in-circuit emulators, including Mice-II, Hitex, and Intel emulators. The cross compiler conforms to the Intel language definition. Because the cross compiler closely resembles PLM-80 and PLM-86, you can, with little modification, port software written for these compilers to 8051-family microcontrollers. Features of PLM-51 that suit it for use with the 8051 architecture include support for Boolean operations, control over placement of code and data items in the target system, and extensive code optimizations. The compiler produces output in either assembly-language or relocatable-object format. It comes with a run-time support library in relocatable format

and with register description files for the microcontrollers. The A51 assembler supports macroprocessing, public/external bit variables, and all the memory areas and special-function registers of the microcontrollers. It produces a relocatable output file that you can link to output files from the PLM-51 compiler. PLM-51 cross compiler, Sw Fr 1450; A51 assembler, Sw Fr 550; object format utilities, Sw Fr 650.

Sysoft SA, 6926 Montagnola, Switzerland. Phone 091 543195. TLX 79671.

Circle No 396

FORTRAN FOR 80386

- Provides all features of Fortran-77 and 4.2 BSD extensions
- Produces code that is globally optimized for speed or size

The NDP Fortran-386 globally optimizing compiler makes full use of the features of the 80386 μ P. It generates 80386 native code that runs under MS-DOS or Unix System V. The compiler simplifies the porting of existing applications to 80386-based machines by implementing all the features of ANSI Standard X3.9-1978 for Fortran-77, as well as the documented and undocumented extensions of the Berkeley 4.2 BSD f77 Unix compiler. The only limit on the size of programs, procedures, and arrays is 4G bytes or the amount of memory in the system. The compiler generates in-line code for a numeric coprocessor; it can make use of the vendor's mW1167 instruction set or of the numeric transcendentals of the 80387 coprocessor. The compiler outputs assembly language, which you can assemble and link with either Unix System V tools or the PharLap (Cambridge, MA) tools for MS-DOS. \$595.

MicroWay, Box 79, Kingston, MA 02364. Phone (617) 746-7341. TLX 503014.

Circle No 397

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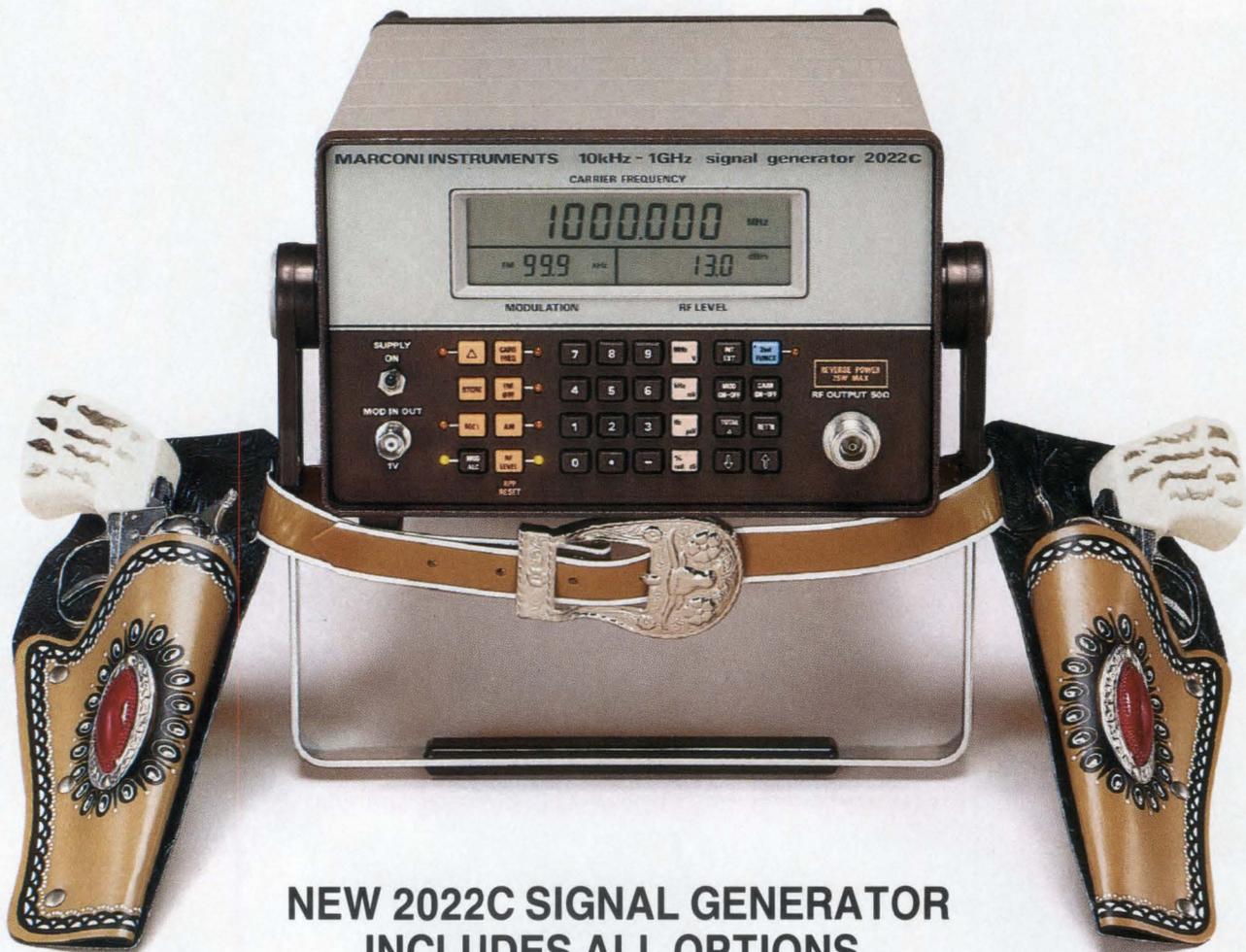
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CIRCLE NO 122

NEW PRODUCTS

TEST & MEASUREMENT INSTRUMENTS

8085 EMULATOR

- 64k bytes of overlay RAM are mappable in 1-byte blocks
- Supports devices clocked at 10 MHz with no wait states

The 8085-64K Icebox in-circuit emulator emulates all versions of the 8085 μ P at speeds as high as 10 MHz, without adding wait states. It can work with processor chips that are soldered in place. You can access the target system by clipping a cable onto the processor chip; you don't have to unplug a socketed processor to connect the emulator. The emulator is compatible with the vendor's TraceAlyzer real-time trace and performance-analysis option. The unit includes 64k bytes of overlay RAM, mappable in increments as small as 1 byte, anywhere in the target system's address space. The device has 65,536 hardware breakpoints; you can set breakpoints on read, write, or fetch

cycles. You can also set breakpoints individually or in groups. \$1395.

Softaid Inc, 8930 Rt 108, Columbia, MD 21045. Phone (800) 433-8812; in MD, (301) 964-8455.

Circle No 398



500-MHz ANALYZER

- Performs spectrum and vector network analysis
- Includes color graphics display

The HP 4195A combines the functions of a vector network analyzer and a spectrum analyzer in a single instrument that costs no more than a single-function instrument capa-

ble of operating in the same frequency band. The unit, which operates from 10 Hz to 500 MHz, includes a color CRT capable of presenting numeric data in tabular form or graphics displays in rectangular, polar, or Smith format. As a spectrum analyzer, its dynamic range is >70 dB; as a network analyzer, it exhibits an amplitude accuracy of ± 0.5 dB and a phase accuracy of $\pm 0.3^\circ$. Built into the instrument is a 3½-in. floppy-disk drive; you can use it to store setups (control settings), measured data, tables of frequencies to include in sweeps, and programs that execute custom functions. You write these programs in a language that resembles Basic. \$23,000; high-stability reference-oscillator option, \$850. Delivery, six weeks ARO.

Hewlett-Packard Co, 1820 Embarcadero Rd, Palo Alto, CA 94303. Phone local office.

Circle No 399

BUS ANALYZER

- Diagnoses faults in MIL-STD-1553 systems
- Includes 20M-byte hard disk

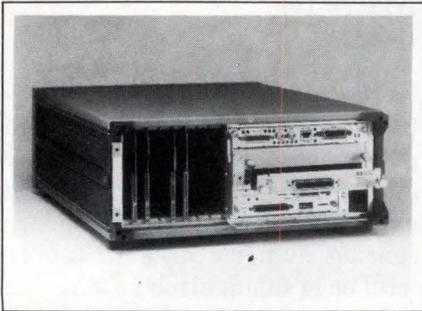
The ABA 500 is a portable or rack-mountable unit based on a 68000 μ P clocked at 8 MHz. It includes 1M bytes of RAM, a detachable keyboard, an electroluminescent display, and, optionally, a 20M-byte hard disk or a 5¼-in. floppy-disk drive. It can automatically test systems based on the MIL-STD-1553 bus, or units intended for connection to the bus, for compliance with the bus protocol. It can also act as a bus controller, as a remote terminal on the bus, or as a monitor of all bus traffic. When used as a monitor, it provides extensive diagnostic displays; for off-line analysis, it can store bus-traffic records as long as 2.3M bytes. RS-232C, IEEE-488, and Centronics-parallel interfaces



are standard, thus facilitating the unit's use in ATE systems. \$22,950 for rack-mount version; \$25,950 for portable version. Delivery, eight weeks ARO.

Interface Technology, 2100 E Alosta Ave, Glendora, CA 91740. Phone (818) 914-2741. TLX 494-5489.

Circle No 400



CONTROLLER

- Single unit houses CPU and instrument cards
- 7-in. rack mounts

The HP 6954A multiprogrammer is a 7-in.-high rack-mountable unit containing a computer identical to the HP 9000 Model 310 and eight slots in which you can place instru-

mentation cards from the HP 69700 family. Because of the 6954A's construction, many small dedicated automatic test systems, which previously required separate units for the CPU and the instrument cards, now fit in a single unit. The computer, which is based on a 68010 μ P, includes 1M bytes of RAM and a 20M-byte hard disk. If you add an optional keyboard and video display, you can use the unit for program development as well as for instrument control. As soon as you apply power, you can access a special version of the Basic language, which incorporates extensions for instrument control. When you use the computer as a dedicated controller, you can communicate with it via an RS-232C port that's included as a standard feature. An IEEE-488 interface lets you control external instrumentation. In the 69700 series of card-level instruments, 30 models are available, including new timebase and counter cards. Multiprogrammer, \$10,400; keyboard and CRT, \$595; expansion chassis for 14 additional cards, \$3800; instrument cards, \$415 to \$2350.

Hewlett-Packard Co, 1820 Embarcadero Rd, Palo Alto, CA 94303. Phone local office.

Circle No 401

Turn Good Ideas Into Good Articles

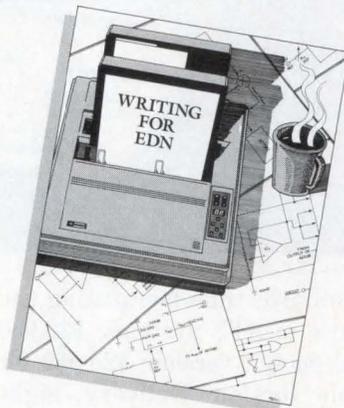
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68020 PROBE

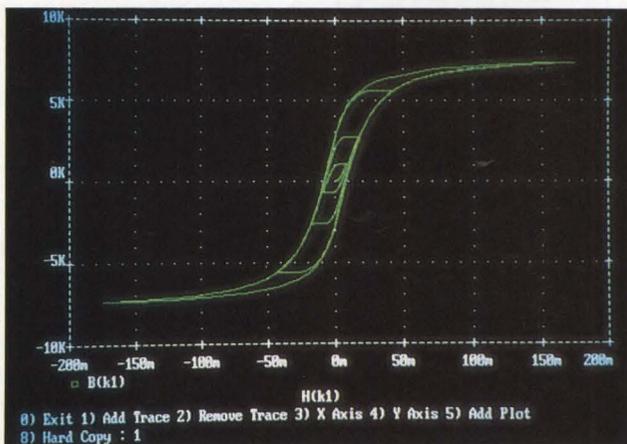
- Displays cache hits at 20 MHz
- Provides time-correlated trace in dual- μ P systems

The 68020 probe works with the vendor's SAW (software analysis workstation). It supports the 68020's onboard cache. You don't have to disable the cache to use the workstation. If you do not display cache hits, you can operate the μ P with a 25-MHz clock; if you display cache-hit cycles, you can use a 20-MHz clock. The disassembler provides symbolic disassembly and transfer-of-control filtering. It works with the 68020's dynamic-bus-sizing feature. The workstation

PSpice

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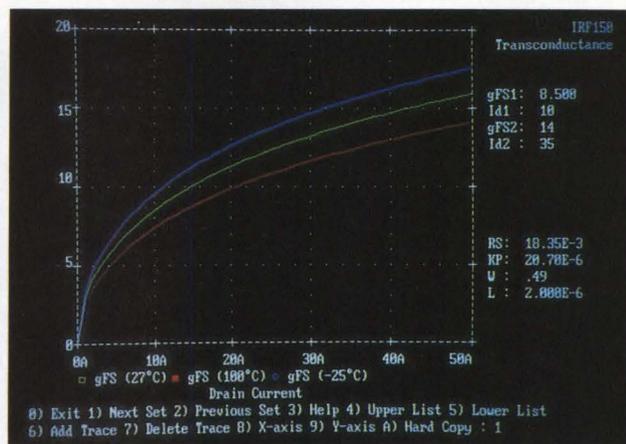
B-H curve from a core in the PSpice transformer library

Since its introduction four years ago, MicroSim's PSpice has sold more copies than all other SPICE-type simulators combined. Many of these customers work with power electronics. Why do so many power designers choose PSpice? Perhaps because every copy of PSpice includes these features:

- A non-linear magnetics model based on the Jiles-Atherton ferromagnetic equations. It models saturation, hysteresis, eddy current losses, and air gap effects. Instead of approximating the core by using separate equations for different operating regions and then "gluing" the results together, the PSpice model uses one set of equations which describes the core's entire behavior.
- A library of power MOSFET's. The MOSFET equations in PSpice have been enhanced to allow more convenient and accurate modeling of power devices.
- Ideal switches. Logarithmic interpolation for the ON/OFF transition avoids numerical problems.

Or perhaps because of these options available for PSpice:

- Monte Carlo analysis to calculate the effect of parameter tolerances on circuit performance.
- The Probe "software oscilloscope", allowing interactive viewing of simulation results. The left photograph above is a Probe display.



Characterizing a power MOSFET using Parts

- The Parts parameter extraction program, allowing you to extract a device's model parameters from data sheet information. The right photograph above shows a step in characterizing a power MOSFET.

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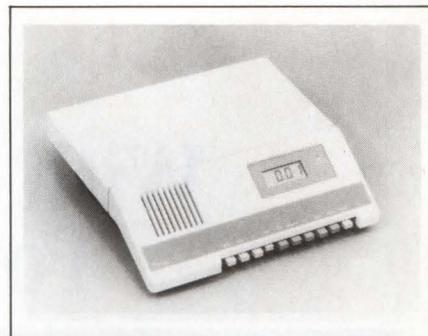
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(714) 770-3022 • (800) 826-8603 • Telex: 265154 SPICE UR

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can monitor the operation of software in real time to determine how many times every routine executes. It also allows symbolic tracing for branch analysis as well as assembly-level tracing. In dual-processor systems—for example, where a 68020 acts as a backup processor for a 68020 main processor, a dual display in trace mode allows you to time

correlate the interaction between the processors. SAW system, configured for 68020 code development and excluding the host IBM PC/AT, \$24,690; 68020 probe only, \$2500; disassembler, \$765.

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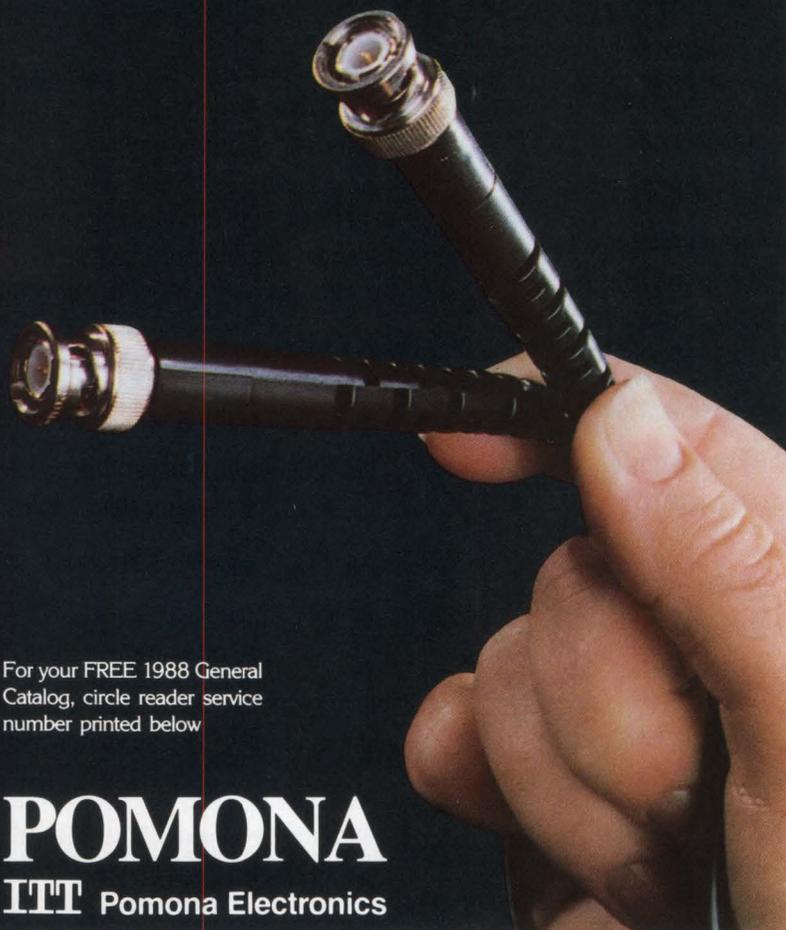
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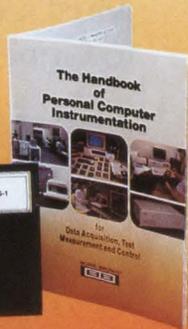
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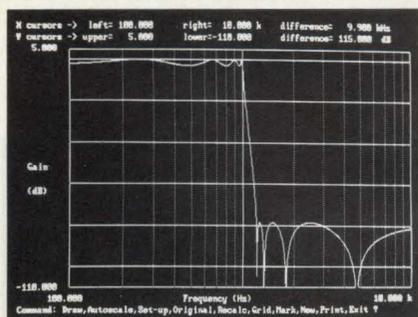
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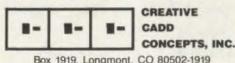
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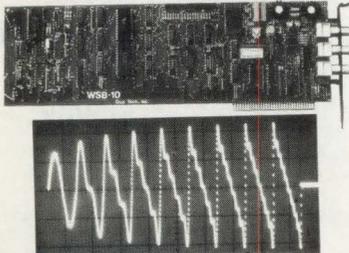
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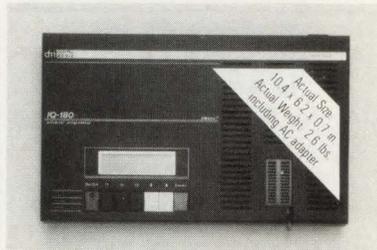


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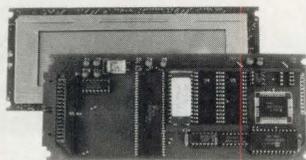
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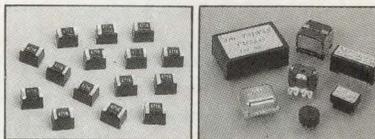


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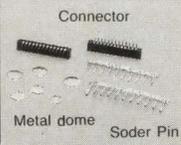
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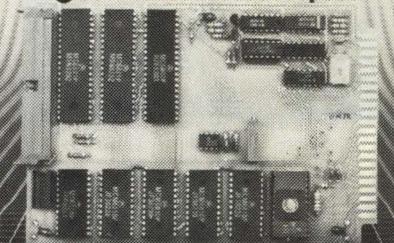
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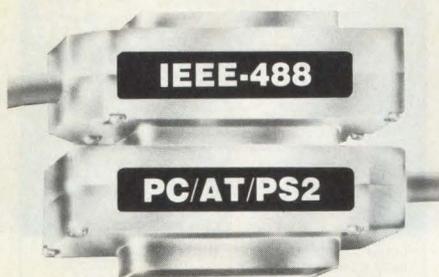
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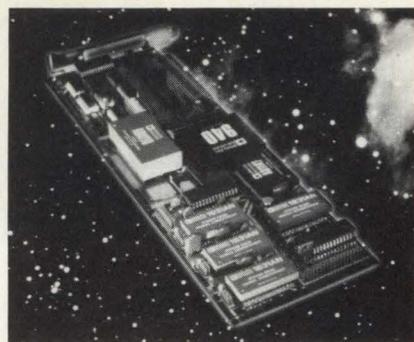
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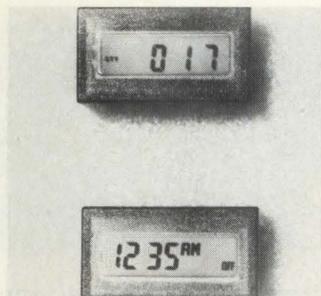
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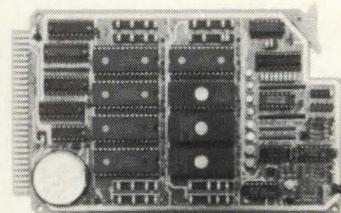
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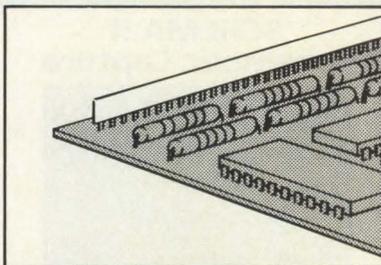
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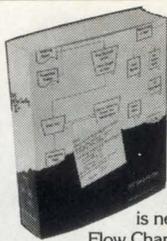


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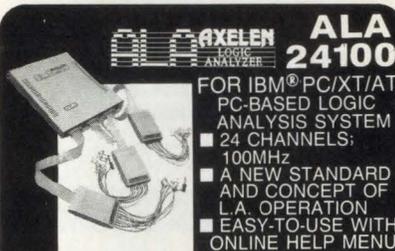
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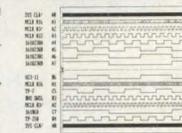
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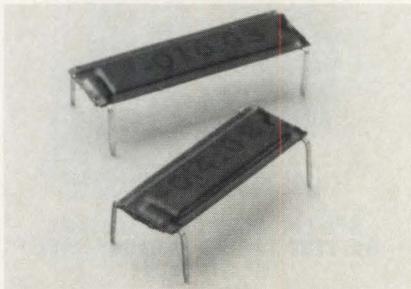
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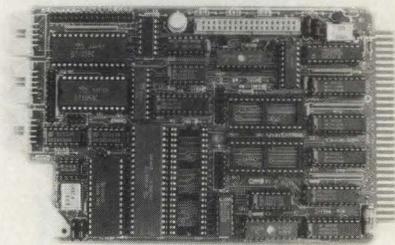
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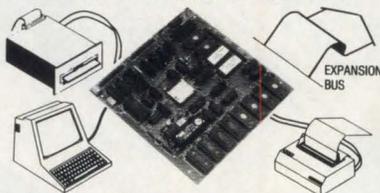
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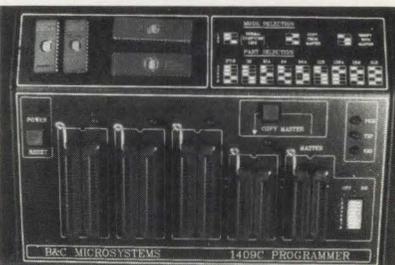
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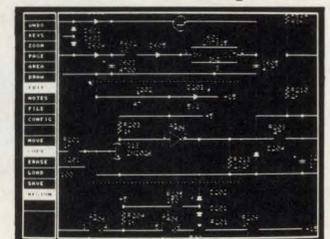
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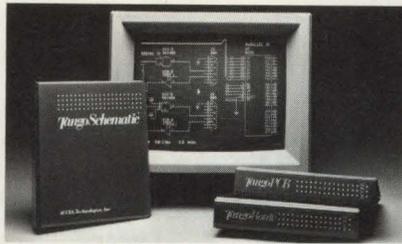


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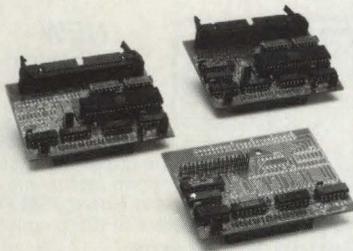
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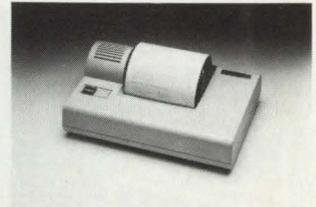


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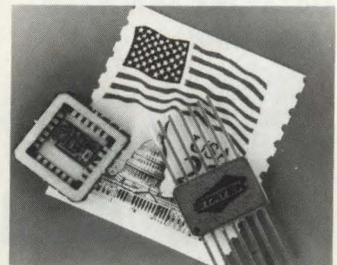
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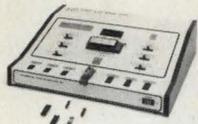
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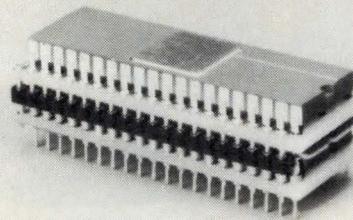
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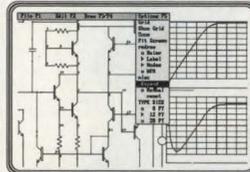


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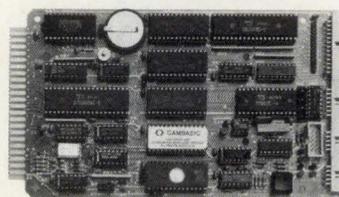


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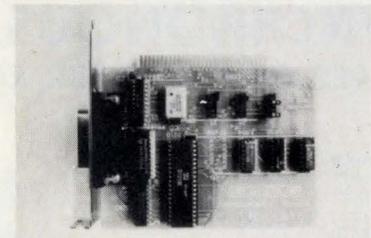


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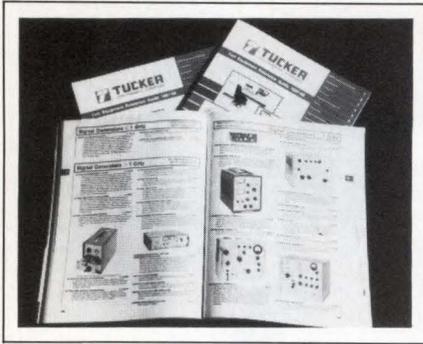
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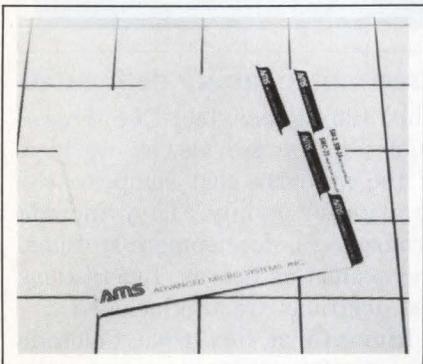


Comprehensive guide categorizes test equipment

The *Test Equipment Reference Guide 1987/1988* is a 375-pg catalog that contains technical specifications and prices for more than 4000 reconditioned test instruments, as well as new instruments, power supplies, coaxial components, waveguides and waveguide components, and a line of technical books. Many items are available for short-term rental or lease. The equipment categories include amplifiers, analyzers, avionics and telecommunications test equipment, frequency-measuring instruments, generators, bridges, calibration and standards, meters, oscilloscopes, power supplies, RFI/EMI, and microwave components.

Tucker Electronics Co., Box 461966, Garland, TX 75046.

Circle No 404



Guide covers motion-control and vision systems

This 1988 product guide presents data and prices for the vendor's single-board computers, memory I/O cards, intelligent motor-controller ICs/boards, dual-axis chopper de-

sign, and intelligent motor-controller boards/systems. Also included are high-power driver cards, video cross-hair generators/digitizers, programmable cross-hair generators, high-speed data-acquisition boards, digital speech generators, and an intelligent motor-controller board for the IBM PC/XT and PC/AT.

Advanced Micro Systems Inc., 31 Flagstone Dr, Hudson, NH 03051.

Circle No 405



Test-equipment catalog

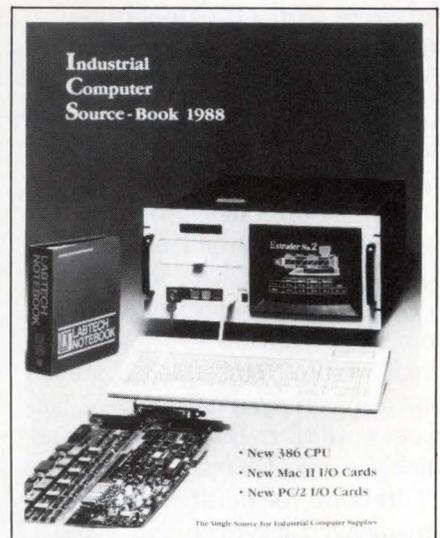
This 8-pg catalog describes the company's complete line of products, featuring new multifunction frequency counters and 2-MHz sweep/function generators. Other products featured are 3½- and 4½-digit handheld DMMs; a VOM (voltmeter, ohmmeter, ammeter); a high-accuracy, full-range 3½-digit capacitance tester; and a variety of other digital instruments and probes.

Mercer Electronics, 859 Dundee Ave, Elgin, IL 60120.

Circle No 406

Expanded list of products for IBM PCs

The 1988 *Industrial Computer Source-Book* features products for industrial and educational laboratories, factory automation, and pro-



cess measurement and control. The product offerings now include new 386 CPU cards, CMOS I/O cards, data-acquisition and -control products for VME Bus computers, Apple MACII A/D I/O cards, and PS/2 I/O cards. A variety of industrial computers, equipment, and components are available, as well as a large selection of 19-in. rack-mount accessories, including a rack-mount industrial PC/AT, keyboard, printer, and monitor. Further, a new 34-pg software section, as well as more than 120 updated scientific- and engineering software packages have been added.

Industrial Computer Source, 5466 Complex St, Suite 208, San Diego, CA 92123.

Circle No 407

Data-collection products presented

This 16-pg catalog features the vendor's DataQuest line of data terminals, transaction processors, automatic identification interfaces, and peripherals. It presents the key features, applications, benefits, and ordering information for each product. Illustrations and diagrams, as well as lists of the vendor's domestic and international offices, complete the brochure.

Burr-Brown Corp., Box 11400, Tucson, AZ 85734.

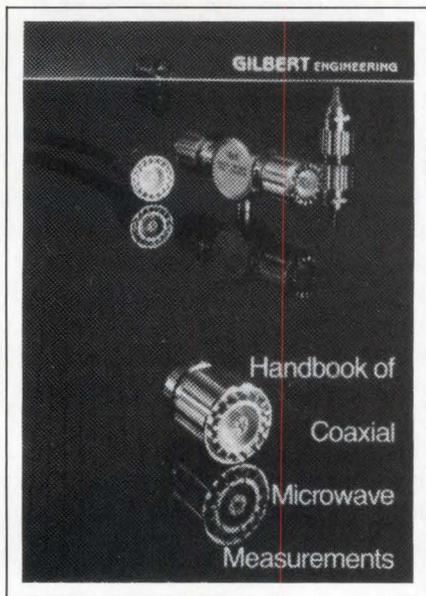
Circle No 408

Science- and engineering- software aids discussed

Lifeboat, a scientific- and engineering software guide, describes 100 packages designed for use in solving equations, analyzing data, breaking down numbers, and designing 3-D CAD/CAM. The products are listed side by side to make it easier for you to compare them and make a selection. The product categories include circuit design, embedded systems, data acquisition/signal analysis, languages/utilities, Basic, C, crossassemblers, and Fortran.

Lifeboat Associates Inc, 55 S Broadway, Tarrytown, NY 10591.

Circle No 409



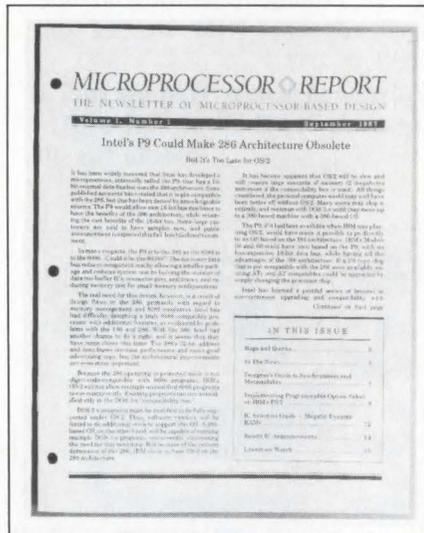
Handbook deals with microwave measurements

The 163-pg *Handbook of Coaxial Microwave Measurements* examines the theory behind microwave measurements and coaxial TEM (transverse electromagnetic wave) transmission lines. It includes chapters on traveling and standing waves, the Smith Chart, 2-port devices, discontinuities, general theory, and some laboratory-measurement equipment setups. It augments current manuals on automatic network analyzers by probing more deeply into microwave-measurement the-

ory. It costs \$10, but is available at no charge to qualifying professionals.

Gilbert Engineering, Box 23189, Phoenix, AZ 85063.

INQUIRE DIRECT



Newsletter for microprocessor designers

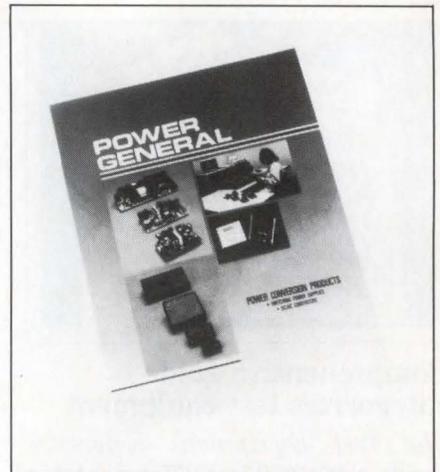
Written exclusively by design engineers, the monthly newsletter *Microprocessor Report* addresses the needs and concerns of designers of μ P-based hardware. It focuses on design techniques, product evaluation, and development tools for μ P-based design. It includes product descriptions, analysis, circuit examples, and bug reports. A monthly index of the most significant articles in journals and trade magazines, as well as design techniques for IBM's Micro Channel and Apple's Nubus, are regular features. The subscription rate is \$195/year, but for a limited time a charter subscription rate of \$135/year is available.

MicroDesign Resources Inc, 230 California Ave, Palo Alto, CA 94306.

INQUIRE DIRECT

DC-DC converter handbook

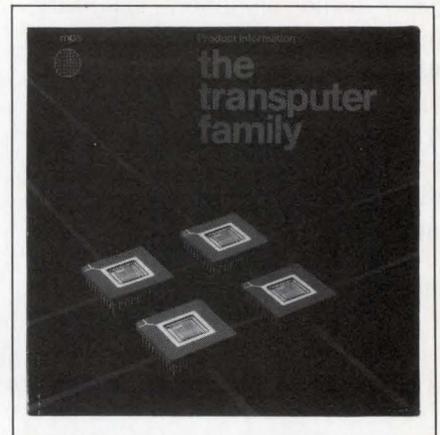
This 144-pg handbook presents the vendor's complete line of switching power supplies and dc/dc converters. Selection tables provide product descriptions and engineering



data on all models. The catalog contains glossaries of power-supply terminology, information about power-supply theory of operation, and application notes.

Power General, Box 189, Canton, MA 02021.

Circle No 412



Transputer family delineated

This 126-pg booklet, *The Transputer Family*, provides an overview of the products that comprise the Transputer family. They include Transputers, development systems, and evaluation boards. Illustrations and diagrams are also included.

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EDN is written for professionals in the electronics industry who design, or manage the design of, products ranging from circuits to systems.

EDN provides accurate, detailed, and useful information about new technologies, products, and design techniques.

EDN covers new and developing technologies to inform its readers of practical design matters that will be of concern to them at once or in the near future.

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EDN provides specific "how to" design information that our readers can use immediately. From time to time, EDN's technical editors undertake special "hands-on" projects that demonstrate our commitment to readers' needs for useful information.

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EDN News

Issue Date	Recruitment Deadline		
Feb. 4	Jan. 14	Semicustom ICs, Computers & Peripherals	Closing: Jan. 21 Mailing: Feb. 11
Feb. 18	Jan. 28	Materials & Hardware, CAE, Power Sources	
Mar. 3	Feb. 11	Communications, CAE, High-Speed Logic	
Mar. 17	Feb. 25	Graphics, Filters, Software/CAE	Closing: Mar. 3 Mailing: Mar. 24
Mar. 31	Mar. 10	Power Semiconductors, Memory/Graphics, Fiber Optics	
Apr. 14	Mar. 23	Communication Technology Special Issue, Communication Systems	Closing: Mar. 31 Mailing: Apr. 21
Apr. 28	Apr. 7	Software, Industrial Computers, Interface ICs	
May 12	Apr. 21	Analog Technology Special Issue, Analog Converters	Closing: Apr. 28 Mailing: May 19
May 26	May 5	CAE, Software, Sensors/Transducers	
June 9	May 19	CAE, Analog ICs, Test & Measurement	Closing: May 29 Mailing: June 16
June 23	June 2	Data Communications, DSP, Components	
July 7	June 14	Product Showcase—Vol. I, Power Sources, Software	Closing: June 23 Mailing: July 14
July 21	June 30	Product Showcase—Vol. II, CAE, Test & Measurement	
Aug. 4	July 14	Sensors & Transducers, Analog ICs, Graphics	Closing: July 21 Mailing: Aug. 11
Aug. 18	July 28	Military Electronics Special Issue, Displays, Military ICs	
Sept. 1	Aug. 11	Instruments, Op Amps, Computers & Peripherals	Closing: Sept. 1 Mailing: Sept. 22
Sept. 15	Aug. 25	Data Acquisition, Data Communications, Digital ICs	
Sept. 29	Sept. 8	DSP, Graphics, Optoelectronics	
Oct. 13	Sept. 22	Test & Measurement Special Issue, Instruments, Computers & Peripherals	Closing: Sept. 29 Mailing: Oct. 20
Oct. 27	Oct. 6	CAE, Computers & Peripherals, Integrated Circuits, Wescon '88 Show Preview	
Nov. 10	Oct. 20	Programmable Logic Devices, Integrated Circuits, Test & Measurements, Wescon '88 Show Issue	Closing: Oct. 27 Mailing: Nov. 17
Nov. 24	Nov. 3	Microprocessor Technology Directory Graphics, CAE	
Dec. 8	Nov. 16	Product Showcase—Vol. I, Power Sources, Software	Closing: Nov. 21 Mailing: Dec. 15
Dec. 22	Dec. 1	Product Showcase—Vol. II, Computers & Peripherals, Test & Measurement	

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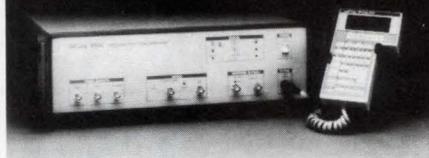
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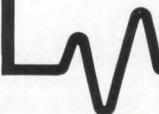
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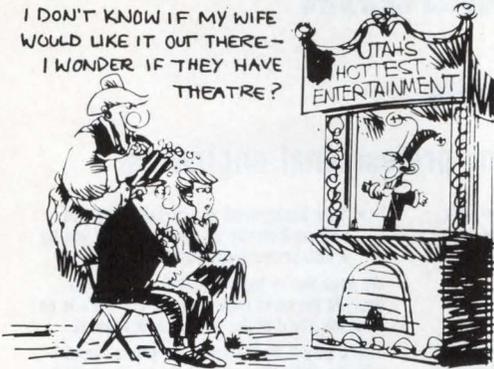
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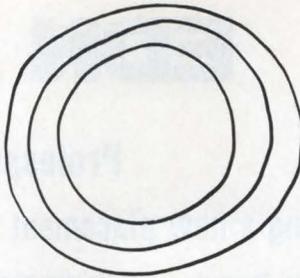
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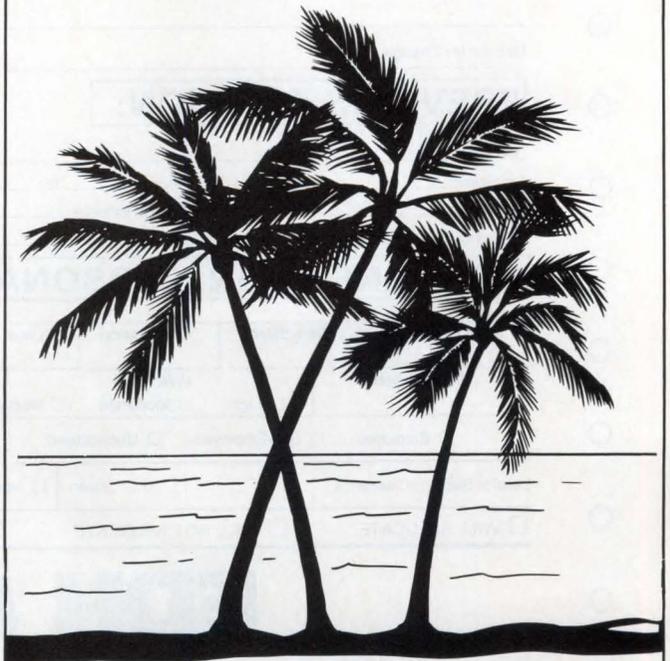
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ABC-Taiwan Electronics Corp	268	GE/RCA Solid State	48-49, 246-247	Sierra Power Systems	241
ACCEL Technologies Inc	271	Greatlink Electronics Taiwan Ltd**	187	Silicon Systems Inc	254
ACDC Electronics	144	Harris Microwave Semiconductor	180	Single Board Solutions	271
Aeroflex Laboratories Inc	197	Harris/Scientific Calculations Inc	153	Software Components Group	133
Aerovox Mallory	221	Heritage Systems Corp	268	Spectrum Software	41
Airpax Corp/Cambridge Div	253	Hewlett-Packard Corp	6, 69-74, 226-227	Sprague Electric Co	54
American Automation	136	Hilevel Technology Inc	223	Standard Grigsby Inc	64
Analog Design Tools Inc	113	Hitachi America Ltd*	100-101	Statek	269, 271
Analogic Data Precision	229	Honlex Industrial Co Ltd	268	Syltel	272
Applied Microsystems Corp	18-19	Hughes AircraftCo/ Connecting Devices Div	156	TDK Corp	97
Archimedes Software	131	Information Scan Technology Inc	272	TEAC Corp**	C2
AT&T Technologies	15-17	Inmos Corp	10-11	Tektronix Inc	36-37, 91, 107-108, 162-163
Atron Div of TL Industries	81	Integrated Circuits Inc	267	Tektronix-CAE Systems	63
Augat-Interconnection Systems	201	Intel Corp	142-143	Telegenix	42
Autodesk Inc	83	Intusoft	272	Teradyne Inc	28-29
Axelen Industrial Inc	270	I/O Tech	211-214	Test Probes Inc	265
B&C Microsystems	270, 272	ITT Cannon	79	Todd Products Corp	267
Beckman Industrial Corp	88	ITT Pomona Electronics	264	Torema USA	35
Belden Electronic Wire & Cable	C4	Janco Corp	138	Toshiba Corp	140-141, 231, 233
Bergquist Co	220	John Fluke Manufacturing Co Inc*	C2, 20, 187	TTE Inc	269
BP Microsystems	270	KEC Electronics Inc	171	United Technologies Microelectronics Center	179
Brooktree Corp	208-209	Kepeco Inc	173-178	Universal Data Systems	C3
Brown Kellogg Inc	271	Leader Instruments Corp	102	Vesta Technology Inc	270
Burndy Corp	44-45	Linear Systems**	88	Vishay Intertechnology Inc	222
Burr-Brown Corp	93, 199, 266	Linear Technology Corp	190	Weidmuller Inc	219
Buscon	68	Logical Devices Inc	267	WinSystems Inc	270
Bytek Corp	230	Loral Instrumentation	129	Wintek Corp	269, 272
Caddock Electronics Inc	32-33	LTX Corp	84-85	Wollongong Group	82
Cahners Exposition Group	283	3M Fluoronics	203-206	Wyse Technology	12
Canon USA Inc	217	Macsyma/Symbolics	14	Xicor Inc	56
Capital Equipment Corp	269	Marconi Instruments*	260	Zericon	272
Case Technology	139	Marion Systems Corp	267	Zilog Inc	195
Chinon America Inc	259	Maxtor	46		
Ciprico Inc	25	Measurement Systems Inc	40		
Clearprint	127	Micro Networks	98-99		
Comair Rotron Inc	40	MicroSim Corp	263		
Creative Cad Concepts Inc	267	Midwest Components	50		
Cubit/Proteus Industries Inc	164	Mini-Circuits Laboratories	3, 4, 26-27, 193		
Cybernetic Micro Systems	65	MK Hansen	269, 272		
Cypress Semiconductor	23	Molex Inc	286		
Dakota Digital	269	MWS Wire Industries	239		
Dale Electronics Inc	1	MX-Com Inc	268		
Dash, Straus, and Goodhue	2	NCI	271		
Data Display Products	235	NDK	218		
Data I/O Corp/Futurenet Div	8	NEC Corp	242-243		
Datel	151	NS Tech**	187		
Deltron Inc	220	Octagon Systems	272		
Digital Electronics Corp	225	Omaton Inc	270		
Digital Media Inc	268	Omron Electronics Inc*	95		
Diversified Technology	64	Patton & Patton	270		
Dotronix	257	Philips Test & Measuring Instruments Inc**	53		
Du Pont Electronics	38-39	Precision Monolithics Inc	189		
Dynatem Inc	13	Qua Tech Inc	268, 271		
EH Titchener & Co	42	Qualidyne Systems Inc	35		
Electrochem	216	Raytheon	59		
Emerald Computers	86	RLM Research	267		
Ferranti Semiconductors	34	Rockwell International	61		
Force Computers Inc	30-31	Rogers Corp	269, 270		
Forth Inc	53	Seagate Technology	111		
Frequency Devices	105				
Fujitsu Components of America Inc*	34				
Fujitsu Limited**	20				
Galiso Inc	269				
GE Plastics	43				

Recruitment Advertising

Corporate Directions	278
I-Omega	279
LeCroy	278
Modcomp	279
Opportunity Center	281

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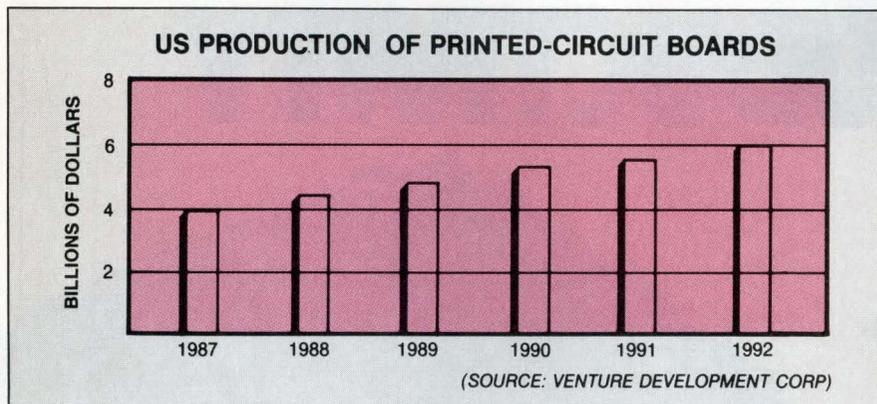
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LOOKING AHEAD

EDITED BY CYNTHIA B RETTIG



PC-board market to grow at 8% average rate per year

Because of the general electronics slump, open-market shipments of printed-circuit boards by US merchants have been declining since 1984. However, Venture Development Corp (VDC, Natick, MA) predicts a change for the better from now through 1992. The market-research firm suggests that this change may allow US merchants to recapture their former dominance of the US market. Assessed at \$4 billion in 1987, the US market for pc boards will grow at an annual average rate of 8% per year and reach \$6 billion by 1992. The US manufactures more than a third of the world's total supply of pc boards.

In comparison with the captive market, which VDC strictly defines as in-company sales (including division-to-division sales), the open market now commands a 52.6% market share. By 1992, the captive market's share should decrease to 41.7% as the open market's increases to 58.3%.

Although rigid circuit boards will retain their lead in terms of US board consumption, injection-molded pc boards will steadily increase their market share throughout the forecast period. The growth rate for injection-molded boards will exceed 50% annually. In consequence, these boards will start to eat into the market share of flexible pc boards.

In addition, multilayer pc boards will continue to replace double-sided boards in many applications. Multilayer pc boards are widely employed in data processing, communications, and aerospace/military/government applications. Use of the multilayer boards in such applica-

More US companies plan for crisis communications

Fifty-seven percent of the largest corporations in the US now have operational plans for crisis communications, according to a survey commissioned by Western Union Corp (Upper Saddle River, NJ). The survey polled the top Fortune 1000 industrial and Fortune 500 service companies. Companies listed the following as important parts of crisis management: news releases, telephone contacts, press conferences, electronic mail, and up-to-date lists of key contacts. The situations in which such communications are nec-

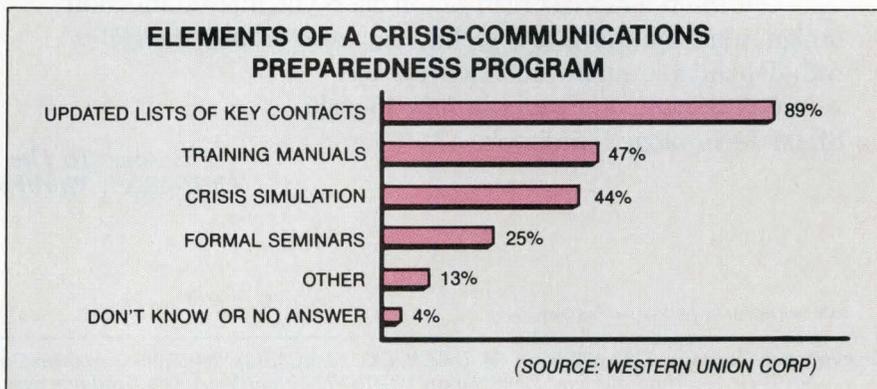
tions accounts for about 50% of US board consumption; by contrast, single-layer pc boards claim a small, and steadily decreasing, share of the US consumption of boards.

The use of surface-mount technology—which not only reduces a board's potential size but also increases its component density and improves its electrical performance—will increase during the forecast period. By 1992, more than half of all pc boards will employ at least some surface-mount components.

Currently, the data-processing and communications fields consume more than half of all US-manufactured pc boards. These two sectors are expected to increase their consumption at above-average growth rates through 1992.

essary include natural disasters, industrial accidents, mergers/takeovers, product recalls, and environmental problems.

The larger the company, the more likely it is to anticipate crises. Companies with over \$1 billion in revenues are considerably more likely to have crisis plans than are smaller companies. Although 75% of the larger companies have some plans and crisis teams in place, less than 50% of the smaller companies are prepared to face a crisis that would require extraordinary communications methods.



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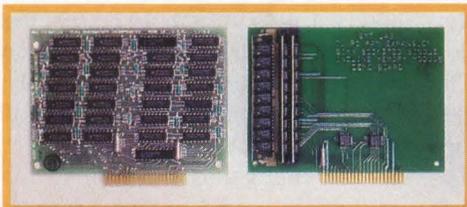
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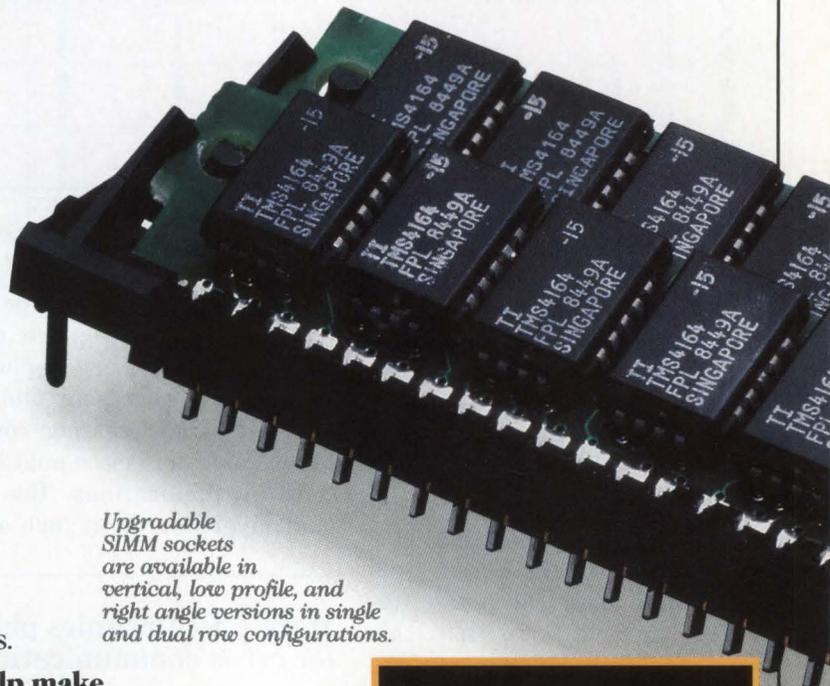
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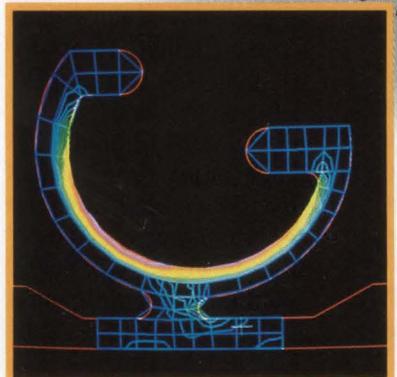
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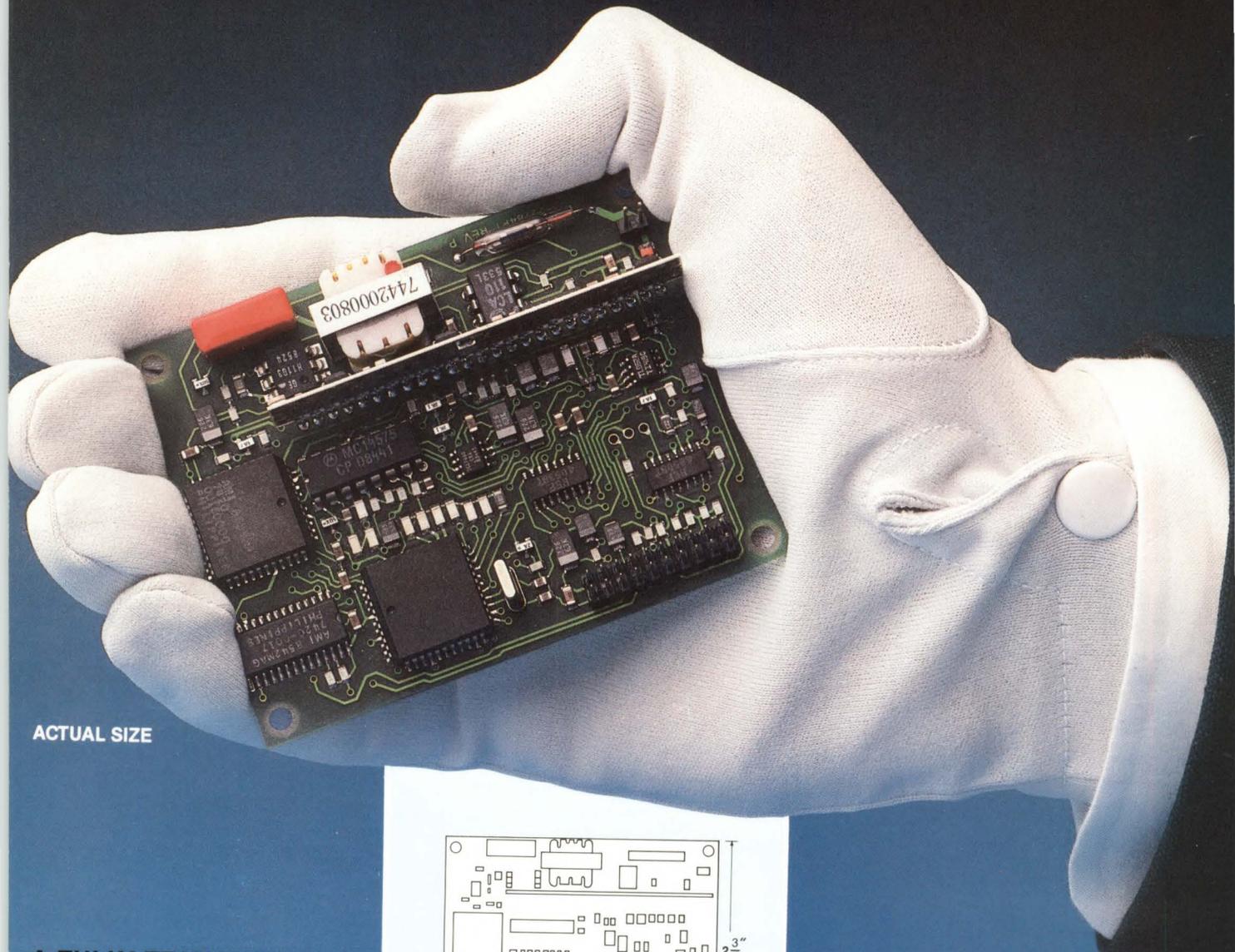
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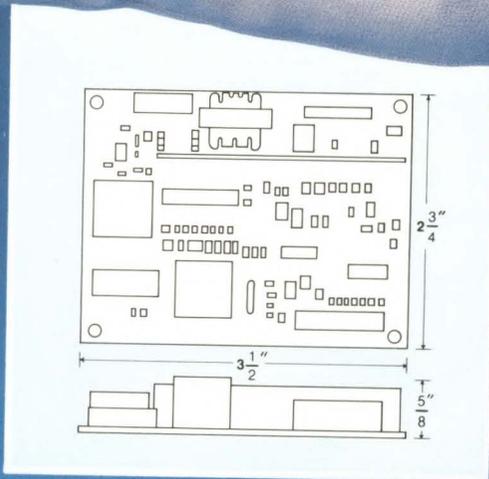
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