

EDN

Switched-capacitor ICs
offer more than filtering

Graphics boards benefit from
TMS34010 and 82786 chips

Tools for ASIC testing

Hands-on SMT project

Gate-array directory

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your designs to market



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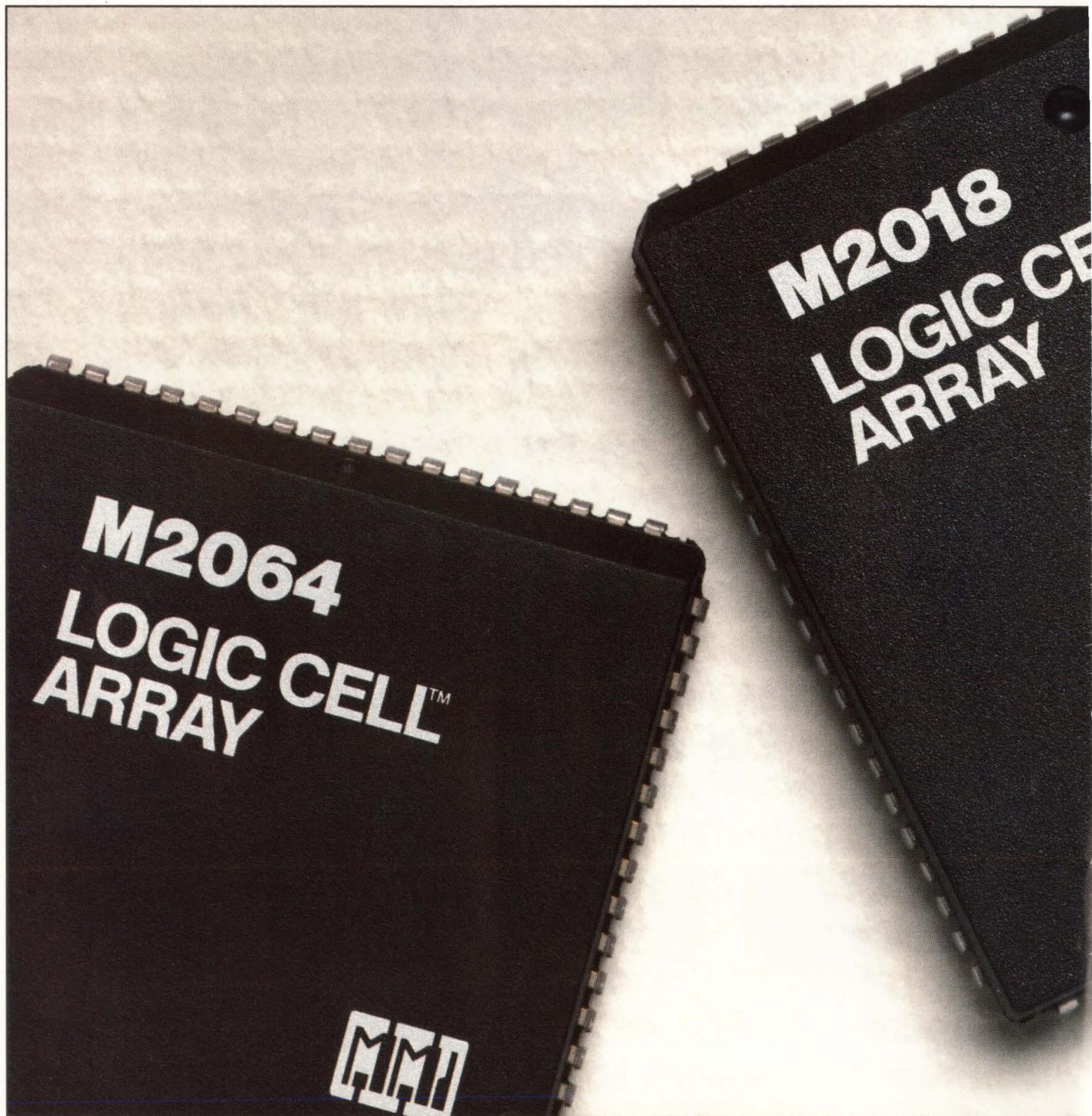
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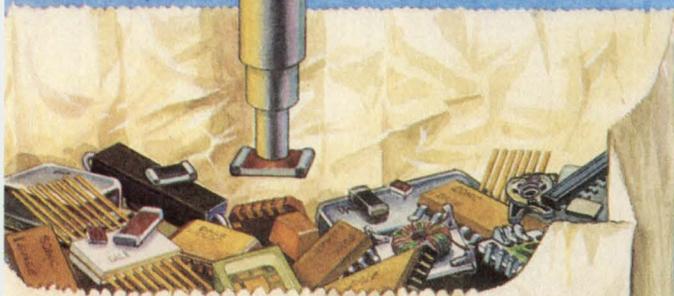
CIRCLE NO 229

Programmable gate arrays, what else?



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you've been
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without
the waiting?**

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Dale[®] Surface Mounted Components—for more choice in less space.

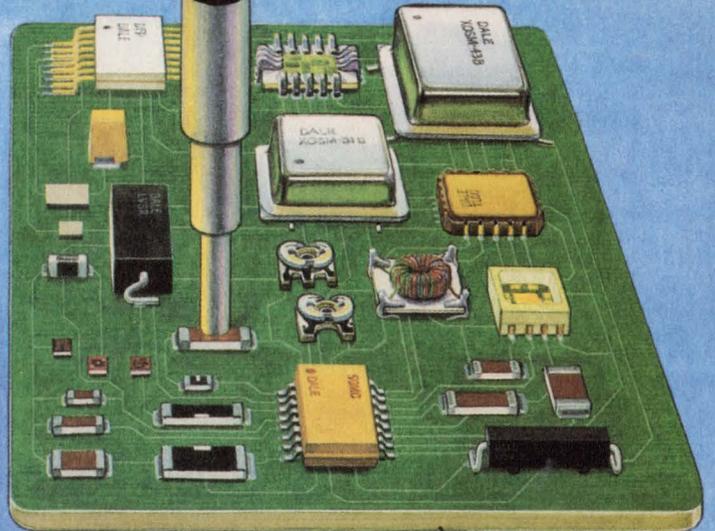
Pick Dale and place your surface mounted requirements in the hands of an industry leader. Dale's experience with surface mount technology began in 1970, when we introduced our first chip resistors. Today, Dale has a wide selection of basic surface mounted components to choose from. This choice offers you maximum flexibility in coordinating packaging and performance requirements.

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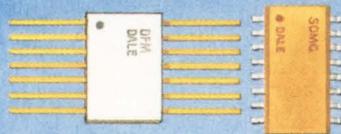
Dale's unique blend of experience, selection and excellent service provides you with what you need to accelerate your surface mount progress. The numbers to call are: **Thick Film Resistor Networks, Thermistors:** El Paso, TX: 915-592-3253; **Thin Film Networks, Thick and Thin Film Chips:** Norfolk, NE: 402-371-0080; **Wirewound Resistors:** Columbus, NE: 402-564-3131; **Trimmer Potentiometers, Oscillators:** Tempe, AZ: 602-967-7874; **Inductors, Transformers:** Yankton, SD: 605-665-9301.

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CIRCLE NO 17

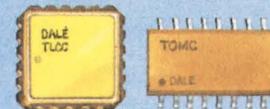


Thick Film Networks SOMC DFM DFP LCCC



Small outline molded dip package, ceramic chip carrier styles and flat pack (MIL-R-83401). All standard schematics. R/C styles available.

Thin Film Networks TLCC *TOMC



Chip carrier styles and small outline molded dip package. All standard schematics.

Thick Film Chips CRCW RCWP RCWPM



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Thin Film Chips



Commercial styles. Flow solderable. Single element and tapped, wire bondable.

Transformers

Custom designs available.

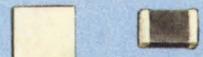


Chip Potentiometers ST



Standard, automatic or reverse adjustment. 100 ohms to 1 Meg.

Thermistors W H



NTC style. 5% & 10%, R₂₅ tolerance.

Chip Inductors *IMC



Molded style, 1 μ H to 1000 μ H. 10% & 20% tolerance.

Oscillators XOSM



Metal packages in two styles (XOSM-43, XOSM-51*). Compatible with most logics. 240 Hz to 60 MHz.

Wirewound Resistors LVSR *WSM



1, 2, 3, 5 watts including low value current sensing styles. "S" and Gull Wing leads.

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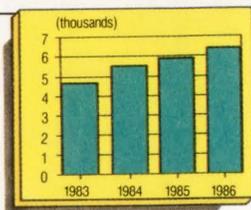
Standards Update

THE FEDS CRACK DOWN ON COMPUTERS THAT INTERFERE

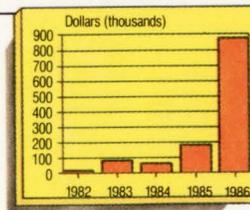
Last Fall's COMDEX show in Las Vegas had a new kind of visitor: A squad of Federal marshals was there to seize equipment the FCC had tagged as non-compliant and to serve notice that arrests may follow. The computers were found to be in violation of Part 15 of the FCC rules, which bans sales of most electronic hardware unless tested for compliance.

The event did not surprise most computer executives, some of whom paid their share of more than \$800,000 in fines issued by the FCC last year. Said one disgruntled manager, "These guys walk around here like Matt Dillon."

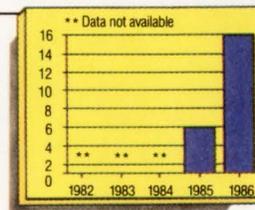
The need to comply has spawned a whole new kind of test business, companies specially skilled in designing and testing for compliance. One of these, the Boxborough, MA-based laboratory of Dash, Straus & Goodhue, combines testing, design and even legal services under one roof, permitting manufacturers to go to COMDEX with their



PART 15 INTERFERENCE COMPLAINTS



NOTICE OF APPARENT LIABILITY FINES

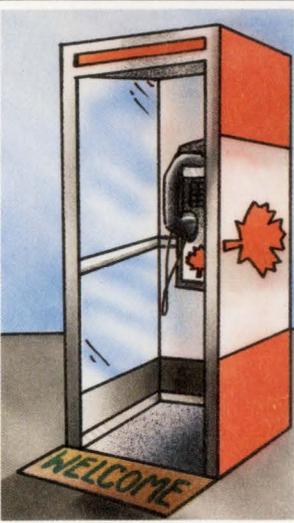


OF REFERRALS TO JUSTICE DEPT.

minds on sales, not sanctions. The company even offers a "Guaranteed Rate/Guaranteed Date" plan under which equipment is tested, modified for compliance, and retested per FCC standards for a fixed price guaranteed in advance. The laboratory has been accredited by the National Bureau of Standards for telecommunications and emissions testing, and can be reached at 617-263-2662.

Call Dash, Straus & Goodhue, Inc. at 617-263-2662.

CANADA LAYS OUT THE WELCOME MAT FOR TELECOM FIRMS



The Canadian government has swung its doors wide open for US telecom manufacturers. The open door policy is a welcome change for US manufacturers who have found most foreign markets closed to their goods. Canada's free trade telecom policy has allowed savvy manufacturers to increase their sales by up to 20%. But to sell north of the border, firms still need to follow a few simple steps. Most importantly, the equipment has to be registered under Canadian Standard CS-03, roughly equivalent to the FCC's interconnect regulations in Part 68. The government of Canada has already approved a number of firms in the United States to do the required telecom testing and submissions. One such firm, Dash, Straus & Goodhue of Boxborough, MA (617-263-2662), has seen a sharp rise in requests for Canadian approvals, especially

among the industry's most successful firms. "There seems to be a correlation between economic success and willingness to enter foreign markets," says firm founder Glen Dash.

Elsewhere in the world, telecom markets are opening. Dash, Straus & Goodhue is currently performing submissions for telecom equipment in both the United Kingdom and Japan. Other countries such as West Germany have shown reluctance to open their markets to US firms, though new efforts within the Common Market (EC Directive 86/361/EEC) may make one unified approval scheme throughout Western Europe a reality within two to three years.

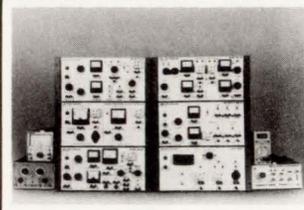
Call Dash, Straus & Goodhue, Inc. at 617-263-2662.

FCC in the 1950's. Willmar Roberts, its inventor, is a former Assistant Chief Engineer of the FCC Laboratory in Laurel, MD.

The antennas are renowned for their near-lossless characteristics. Compliance Design, the exclusive vendor of the Roberts brand, also offers a complete laboratory assembly package. The firm will supply antennas, masts, turntables, site design; and will even perform the crucial "site attenuation" tests the FCC requires. The Boxborough, MA-firm can be reached at 617-264-4668.

For telecom manufacturers, Compliance Design also supplies a Part 68 Workstation™ containing everything that's needed to comply with FCC, CS-03 (Canada) and EIA standards. The Workstation makes setting up Part 68 laboratories practical for just about everyone.

Call Compliance Design Inc. at 617-264-4668.



A DEATH PUTS THE BOSS IN JAIL

On February 13, Kenneth Oden, prosecutor for Travis County, TX, won a landmark case that sent shivers down corporate backbones nationwide. For the first time, company executives were sentenced to jail terms for negligence that cost a worker his life. The case highlighted a nationwide trend in which prosecutors are holding executives criminally liable for the death of a customer or employee.

For makers of EDP, medical and telecom equipment, safety on the job generally means getting their products UL® listed. Listing is a recognition that the product meets UL's standards for fire, shock, energy and mechanical hazards; listing is a legal requirement of certain municipalities. In those places, a death caused by a non-compliant product could give rise to the same charge of gross negligence which caused Travis County executives to be sentenced to jail.

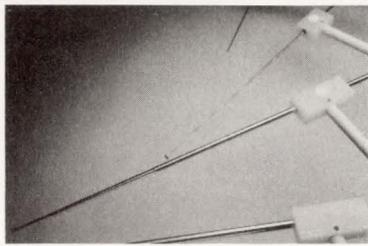
Overseas, marks such as Canada's CSA and West Germany's GS are required, and foreign courts have been even less tolerant of corporate negligence than have our own. With the profusion of worldwide standards, obtaining those marks has proven to be quite a chore. Fortunately, certain key test labs have set up liaison services which permit worldwide product approvals at one location. Dash, Straus & Goodhue is one such lab and is regularly visited by agents of UL, CSA and West German TÜV. Required marks for fourteen countries can be initiated from DS&G's location. Since the Travis County case, according to execs, its business has been brisk.

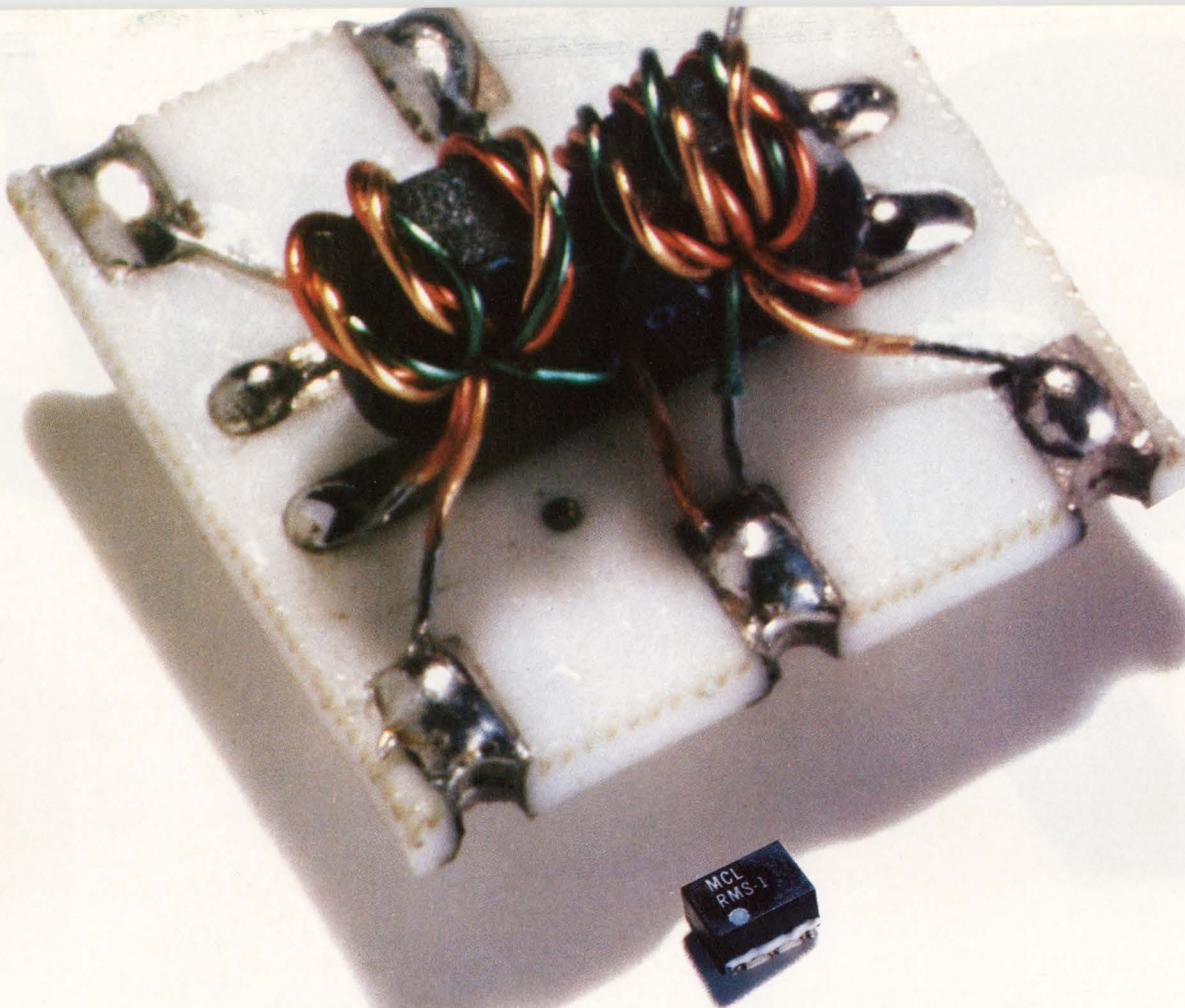
Call Dash, Straus & Goodhue, Inc. at 617-263-2662.



FED'S OWN INSTRUMENTS HELP MANUFACTURERS COMPLY

What kind of tools can best convince an agency that equipment complies? Why, their own, of course. Now the FCC's own designs are available through a company called Compliance Design. Key to emissions compliance is the use of the Roberts Antenna® developed for the





the world's smallest surface mount mixers **\$6.95** from

Tight packing density, lowered assembly costs, and improved reliability make surface-mount technology (SMT) highly attractive to systems and product manufacturers. If your design is ready for SMT, specify Mini-Circuits' new RMS series, the world's smallest (0.25 by 0.30 by 0.2 in.) double-balanced SMT mixers, spanning 0.5 to 1000MHz, from only \$6.95 (10-49 qty).

The tiny, non-hermetic package houses RF transformers, a ceramic-alumina substrate, and a four-diode assembly. A unique edge-plated design eases the job of making reliable solder connections to a printed-circuit board. A protective-barrier layer on top of the package's conductive layer retards the harmful effect of electromigration which may occur during soldering. The RMS can be attached to a pc-board by conventional manual soldering or with automatic equipment; mixers can be supplied in a tape-and-reel format for automated pick-and-place machines.

When you think SMT, think small, low-cost...
think Mini-Circuits RMS series.

SPECIFICATIONS

FREQUENCY RANGE, MHz

LO, RF

IF

RMS-1

0.5 — 500

DC — 500

RMS-2

5 — 1000

DC — 500

CONVERSION LOSS, dB, Typ.

Mid-band ($10f_l - f_{u/2}$)

Total range ($f_l - f_u$)

5.5

6.2

6.5

7.0

ISOLATION, dB, Typ.

Low-band ($f_l - 10f_l$)

Mid-band ($10f_l - f_{u/2}$)

Upper-band ($f_{u/2} - f_u$)

L-R L-I L-R L-I

55 50

33 30

27 24

55 50

35 30

25 20

PRICE (10-49)

\$6.95

\$7.95

f_l = lowest frequency in range

f_u = highest frequency in range

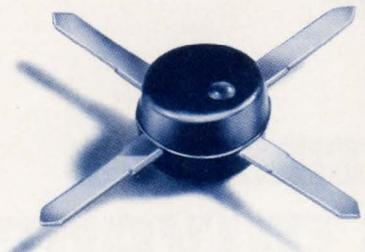
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from



dc to 2000 MHz amplifier series

SPECIFICATIONS

Model	Frequency MHz	Gain, dB (min.)	Max. Power dBm (typ)	NF dB (typ)	Price \$ Ea.	Qty.
MAR-1	DC-1000	13	0	5.0	0.99	(100)
MAR-2	DC-2000	8.5	+3	6.5	1.50	(25)
MAR-3	DC-2000	8	+8	6.0	1.70	(25)
MAR-4	DC-1000	7	+11	7.0	1.90	(25)
MAR-7	DC-2000	8.5	+4	5.0	1.90	(25)
MAR-8	DC-1000	21	+10	3.5	2.20	(25)

Unbelievable, until now... tiny monolithic wide-band amplifiers for as low as 99 cents. These rugged 0.085 in. diam. plastic-packaged units are 50ohm input/output impedance, unconditionally stable regardless of load*, and easily cascadable. Models in the MAR-series offer from 7 to 21dB gain, 0 to +11dBm output, noise figure as low as 3.5dB (5.5dB typical), and up to DC-2000MHz bandwidth.

*3:1 load VSWR for the MAR-8

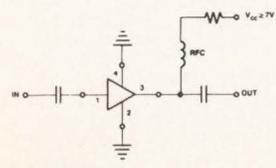
designers amplifier kit, DAK-1
5 of each model, total 30 amplifiers
only \$49.99

Also, for your design convenience, Mini-Circuits offers chip coupling capacitors at 12 cents each*

Size (mils)	Tolerance	Temperature Characteristic	Value
80 x 50	5%	NPO	10, 22, 47, 68, 100, 470, 680, 1000 pf
80 x 50	10%	X7R	2200, 4700, 6800, 10,000 pf
120 x 60	10%	X7R	.022, .047, .068, .1μf

* MINIMUM ORDER 50 PER VALUE

Typical Biasing Configuration



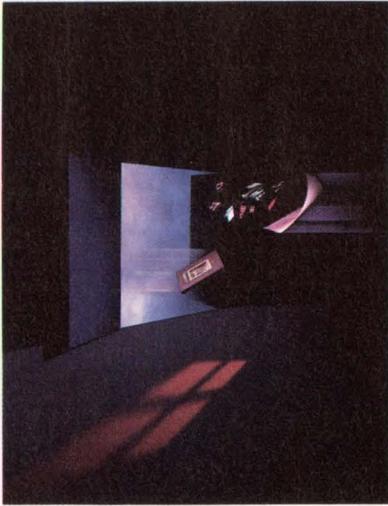
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C113 REV. B
EDN June 25, 1987

CIRCLE NO 206



On the cover: Product success is becoming increasingly dependent on short design cycles. To help your products reach market during a window that ensures profitability, gate-array vendors are offering fast turnaround from design verification to prototype devices. See pg 134. (Photo courtesy LSI Logic; concept and photography by Imagination)

DESIGN FEATURES

Special Report: Gate-Array Directory **134**

Fast turnaround techniques are making it possible to get your gate-array design to market faster. Furthermore, improvements in device technologies, as well as the relentless march toward increasing gate density, are resulting in faster operating circuitry.—*Jim Wiegand, Associate Editor*

Gate-array tables **144**

Gate-array vendors and services **157**

EDN's Hands-On SMT Project—Part 3 **209**

With the parts list completely converted to SMT components, we were ready to tackle the design of our SMT project board using a high-end, pc-board CAD system. What we learned about the features required to perform CAD-based SMT design applies to all CAD systems from low-end, PC-based tools to the most expensive workstations.—*Steven H Leibson, Regional Editor*

ASIC testing mandates new role for circuit designers **231**

No longer will you be able to check out new devices with standard benchtop tools—scopes, logic analyzers, and pulse generators. Today's ASIC devices are simply too complex to let you attack the test problem with rack-and-stack test instruments patched together from traditional GPIB lab instruments.—*Alan Whiteside and Clayton Mohr, Tektronix Inc*

Application dictates your choice of a multiprocessor model **241**

The three major hardware models for modular multiprocessing systems provide different levels of both hardware and software complexity. Your choice of a hardware architecture for such a system will depend largely on the amount of effort you're willing to expend on modifying the operating system.—*J Kent Peacock, Counterpoint Computers*

Variable-pulse modulator improves power-supply regulation **251**

A pulse regulator combines aspects of both pulse-interval modulation and pulse-width modulation to improve the regulation and the efficiency for switch-mode power supplies. The circuit is particularly useful in applications requiring line isolation.—*Wayne M Austin, GE/RCA Solid State*

Continued on page 7

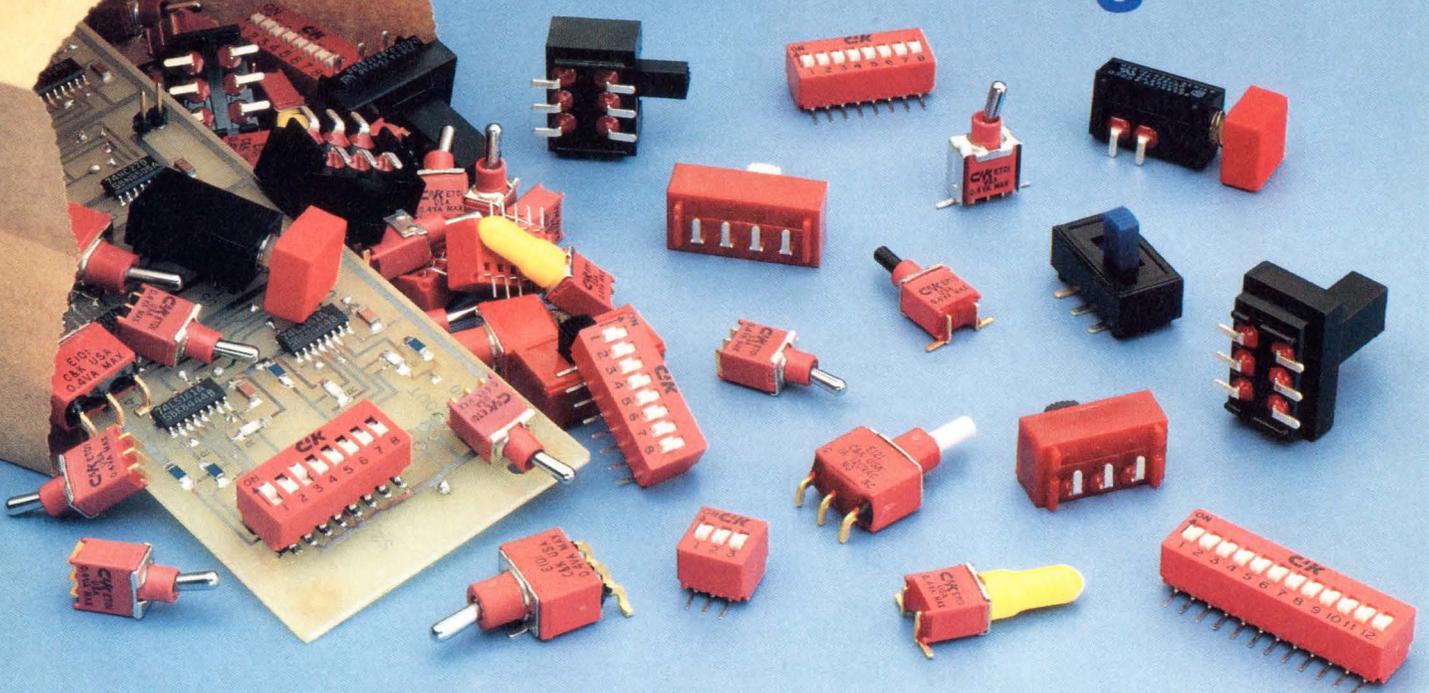


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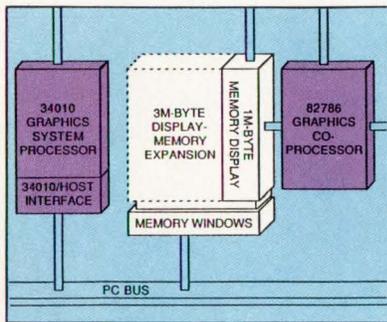


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CIRCLE NO 208





Intelligent graphics ICs are enhancing PC add-in boards' capabilities (pg 67).

TECHNOLOGY UPDATE

PC add-in boards rev up graphics engines with hardware and software enhancements 67

The latest add-in graphics boards for the IBM PC and PC/AT bus incorporate graphics engines, which give them faster response time and greater color and pixel resolution than the IBM Enhanced Graphics Adapter, often at a surprisingly low price.—*Margery S Conner, Regional Editor*

Comparisons reveal the pros and cons of designing with switched-capacitor ICs 83

Now that the telecommunications industry is no longer dictating the performance levels of switched-capacitor components, many more flexible models of these ICs are rapidly becoming available.—*David Shear, Regional Editor*

Beware of subtle electrical, thermal differences between through-hole components and SMDs 97

As SMT reaches the R&D lab, design engineers will have to pay attention to some subtle, yet important, electrical and thermal differences between equivalent SMT and through-hole components or risk unforeseen problems with their designs.—*Charles H Small, Associate Editor*

PRODUCT UPDATE

Semicustom linear arrays	111
Switching-regulator IC	114
Workstations and autorouter	118

DESIGN IDEAS

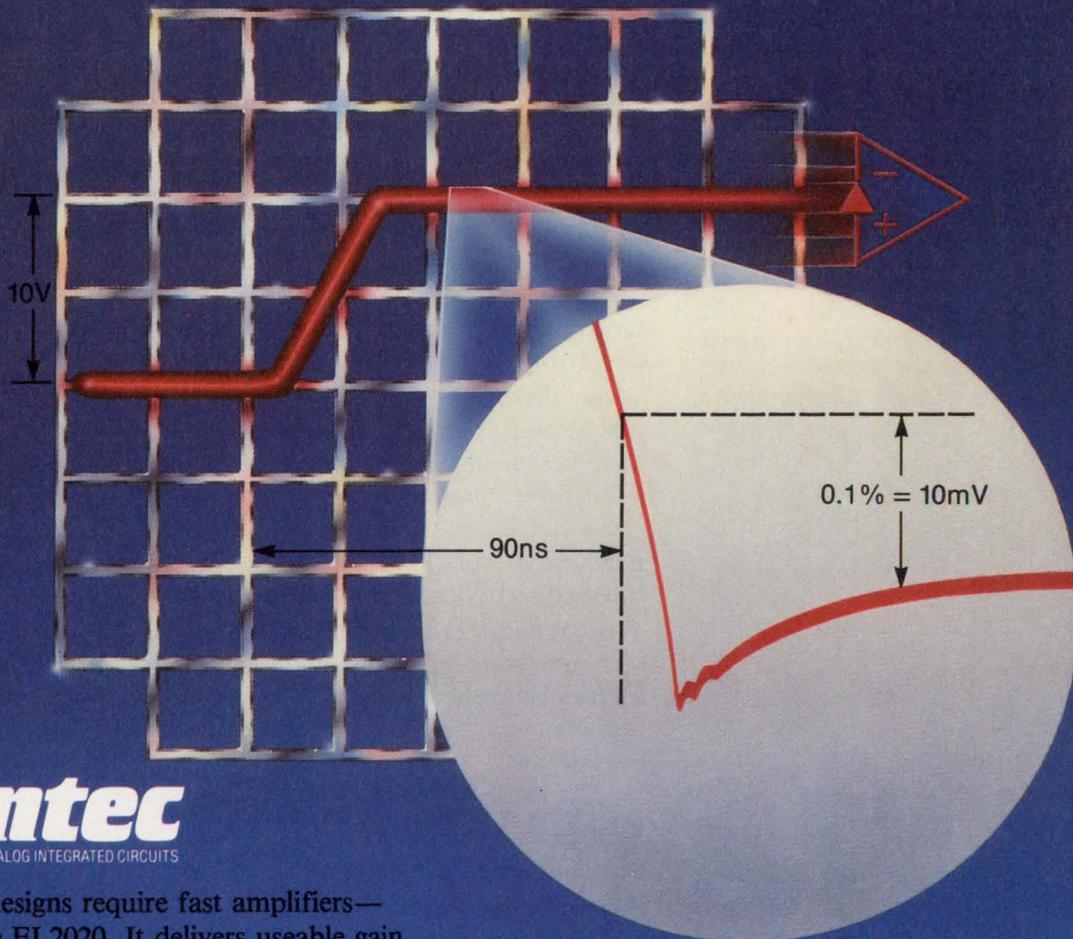
Electrostatic voltmeter uses BiMOS op amp	271
Complex-multiply code saves clock cycles	273
Circuit ensures proper RS-232C mating	274
Simpson's rule solves double integrals	276
Regulator has low drop-out voltage	280

Continued on page 9

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EDITORIAL

59

US trade would benefit from a re-evaluation of our export policies. Today's trade restrictions are inconsistent, costly, and out of date.

NEW PRODUCTS

Computers & Peripherals	282
Integrated Circuits	294
Components & Power Supplies	306
CAE & Software Development Tools	318
Test & Measurement Instruments	324

PROFESSIONAL ISSUES

335

Programmers gain control of their designs through changes in copyright law.—Joseph Iandiorio, Waltham, MA

LOOKING AHEAD

350

Military-ASIC market grows at 18% rate through 1991...Optical-storage market ready to burgeon.

DEPARTMENTS

News Breaks	21
News Breaks International	24
Signals & Noise	34
Calendar	46
Readers' Choice	122
Leadtime Index	124
Literature	328
Career Opportunities	338
Advertisers Index	348
Business/Corporate Staff	349

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STUNTED

YEARS FROM NOW, WILL YOUR MILITARY SUPPLIER BE JUST A BAD MEMORY?

It's no secret—there's a lot of uncertainty in the marketplace. You never know if the company you're dealing with today will still be around to service you tomorrow. And that's a chance you can't take—especially in the military market.

With INMOS, you're not taking any chances. We have a seven-year history of supporting all major military defense programs with static and dynamic RAMs. Our fabrication facilities are fully compliant with MIL-STD-883C; with military burn-in, performance testing and quality assurance conducted in Colorado Springs.

We have your future in mind with our new CMOS military SRAMs (with performance to 35ns over the full military temperature range) and military low power battery backup CMOS SRAM products. We're the only company in the world to produce 64K and 256K DRAMs with RAS access times down to 80ns, and we're going to keep on producing and servicing innovative military products year after year.

For military products you can depend on, count on INMOS—the beginning of a very good memory.

16K SRAMs		
Device	Process	Access Times
IMS1400M (x1)	NMOS	45, 55, 70ns
IMS1420M (x4)	NMOS	45, 55, 70ns
IMS1403M (x1)*	CMOS	35, 45, 55ns
IMS1423M (x4)	CMOS	35, 45, 55ns

64K CMOS SRAMs	
Device	Access Times
IMS1600M (x1)*	45, 55, 70ns
IMS1620M (x4)*	45, 55, 70ns
IMS1624M (OE, x4)*	45, 55, 70ns
IMS1630M (x8)*	45, 55, 70ns

MILITARY DRAMs		
Device	Process	RAS Access Times
IMS2600M (64Kx1)	NMOS	100, 120, 150ns
IMS2800M (256Kx1)	CMOS	80, 100, 120, 150ns
IMS2801M (256Kx1)	CMOS	80, 100, 120, 150ns

*Also available as Low Power Battery Backup CMOS SRAMs with I_{dr} of 10μA (typical I_{cc} at 2V at 25° centigrade). inmos,  and IMS are trademarks of the INMOS Group of Companies.

MIL-STD-883C RAMs



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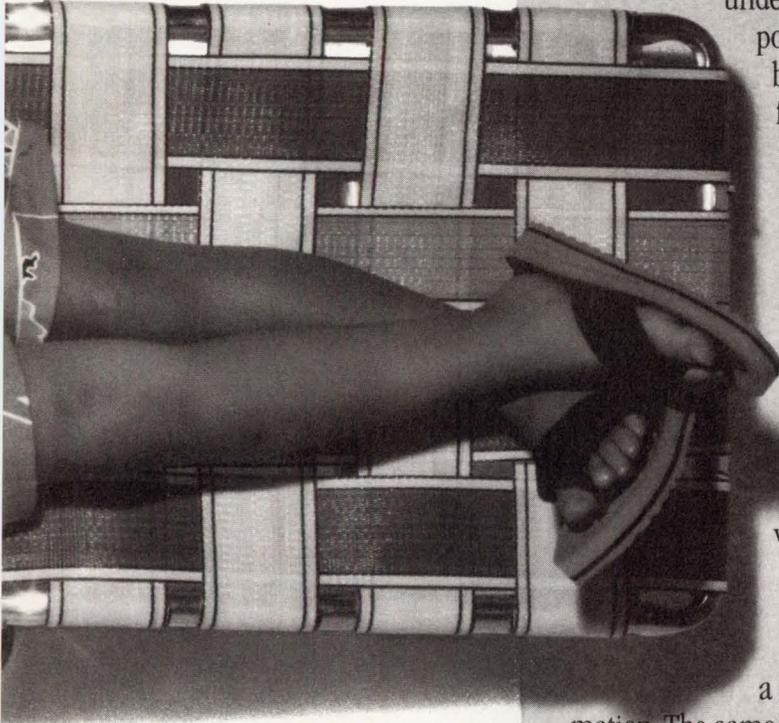
Valid on Sun. What could be more natural? After all, Sun is selling more UNIX workstations than any other vendor.

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And no other EDA vendor offers better CAE, IC CAD and PCB CAD tools on UNIX than Valid.

Together, we give Sun worshippers a golden opportunity for electronic design automation. The same opportunity Digital users enjoy.

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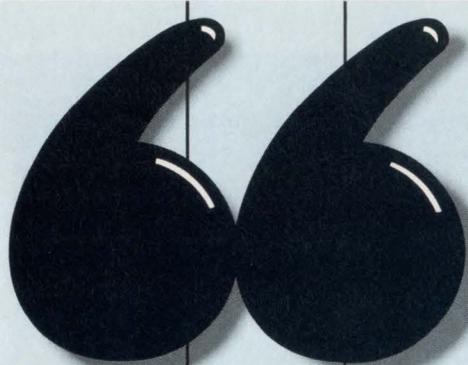
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SRAMS

MB81C86
-55, -70 64Kx4
MB81C84
-45, -55 64Kx4
MB81C81
-45, -55 256Kx1
MB84256
-10L/LL 32Kx8
MB84256
-12L/LL 32Kx8
MB84256
-15L/LL 32Kx8
MB81C71A
-25, -35 64Kx1
MB81C71
-45, -55 64Kx1
MB81C74
-25, -35 16Kx4
MB81C75
-25, -35 16Kx4 (w/OE)
MB81C79A
-35, -45 8Kx9
MB81C79
-45, -55 8Kx9
MB81C78A
-35, -45 8Kx8
MB81C78
-45, -55 8Kx8
MB8464
-12L/LL 8Kx8
MB8464
-15L/LL 8Kx8
MB8464A
-10L/LL 8Kx8
MB8464A
-12L/LL 8Kx8
MB8464A
-15L/LL 8Kx8
MB8464A
-80L/LL 8Kx8
MB8464A
-10W, -15W 8Kx8

MB8167A
-55, -70 16Kx1
MB8167
-35, -45 16Kx1
MB8167
-45W, -55W 16Kx1
MB81C67
-35, -45 16Kx1
MB81C69A
-25, -30, -35, -45 4Kx4
MB81C68A
-25, -30, -35, -45 4Kx4
MB8168
-55, -70 4Kx4
MB81C68
-45W, -55W 4Kx4
MB81C68
-55, -70 4Kx4
MB8422
-90, -120 2Kx8
MB8421
-90, -120 2Kx8
MB8417A
-12, -12L 2Kx8
MB8417A
-15, -15L 2Kx8
MB8417
-20, -20L 2Kx8
MB8416A
-12L, -15L 2Kx8
MB8416
-20, -20L 2Kx8
MB8416
-25W 2Kx8
MB8128
-10, -15 2Kx8
MB85402
-25 16Kx16

ECL RAMS

MB70801
-15 512x9

MB70802
-20 512x9
MBM7700H
-5 256x16
MBM100422A
-5, -7 256x4
MBM10422A
-5, -7 256x4
MBM100490
-15 64Kx1
MBM100490
-25 64Kx1
MBM10490
-15, -25 64Kx1
MBM100480
-15, -25 16Kx1
MBM100480A
-10 16Kx1
MBM100484A
-10 4Kx4
MBM100484
-15 4Kx4
MBM10480A
-10 16Kx1
MBM10484A
-10 4Kx4
MBM10480
-15, -25 16Kx1
MBM7750
-10 1Kx16
MBM100470
-10, -15 4Kx1
MBM100474A
-5, -7 1Kx4
MBM100474A
-10, -15 1Kx4
MBM10470A
-10, -15 4Kx1
MBM10474A
-5, -7 1Kx4
MBM10474A
-10, -15 1Kx1
MBM10415AH
1Kx1

PROMS

MBM7226RA
-20, -25 512x8
MBM7226RS
-20, -25 512x8
MB7123E/H
-35, -45 512x8
MB7124E/H
-35, -45 512x8
MB7115E/H
-35, -45 512x4
MB7116E/H
-35, -45 512x4
MB7117E/H
-35, -45 256x8
MB7118E/H
-35, -45 256x8
-5 256x16
MB7114E/H
-35, -45 256x4
MB7113L
LOW-PWR 256x4
MB7114L
LOW-PWR 256x4
MB7212RA
-20 32x8
MB7212RS
-20 32x8
MB7111E/H
-25, -35 32x8
MB7112E/H
-25, -35 32x8
MB7111L
LOW-PWR 32x8
MB7112L
LOW-PWR 32x8
MB7143E/H
-55, -65 8Kx8
MB7144E/H
-55, -65 8Kx8
MB7144Y
-45 8Kx8
MB7242RA
-20 4Kx8
MB7242RS
-20 4Kx8
MB7141E/H
-55, -65 4Kx8
MB7142E/H
-55, -65 4Kx8
MB7142E/W
-55, -65 4Kx8
MB7151E/H
-45, -55 4Kx4
MB7152E/H
-45, -55 4Kx4
MB7152Y
-35 4Kx4

MB7133E/H
-45, -55 4Kx4
MB7134E/H/Y
-35, -45, -55 4Kx4
MB7238RA
-20 2Kx8
MB7238RS
-20 2Kx8
MB7137E/H
-45, -55 2Kx8
MB7137E/H/SK
-45 2Kx8 (Skinny DIP)
MB7138E/H
-45, -55 2Kx8
MB7138E/H/SK
-45 2Kx8
MB7138Y/SK
-35 2Kx8
MB7113E/H
-55 2Kx8
MB7127E/H
-45, -55 2Kx4
MB7128E/H/Y
-35, -45, -55 2Kx4
MB7128E/W
-55 2Kx4
MB7232RA
-20, -25 1Kx8
MB7232RS
-20, -25 1Kx8
MB7131E/H
-45, -55 1Kx8
MB7131E/H/SK
1Kx8
MB7132E/H/Y
-35 1Kx8
MB7132E/H/Y/SK
1Kx8
MB7121E/H
-35, -45 1Kx4
MB7122E/H/Y
-30 1Kx4

DRAMS

MB85227
-10, -12 256Kx9
MB85226
-10, -12 256Kx9
MB85225
-10, -12 256Kx8
MB85224
-10, -12 256Kx8
MB85214
-12, -15 256Kx8
MB85213
-12, -15 256Kx8
MB85211
-12, -15 512Kx4
MB85210
-12, -15 512Kx4

MB85206
-10, -12 256Kx4
MB85205
-10, -12 256Kx4
MB85204
-10, -12 256Kx4
MB85203
-10, -12 256Kx4
MB81C4257
-10, -12, -15 256Kx4
MB81C4256
-10, -12, -15 256Kx4
MB81C4258
-10, -12, -15 256Kx4
MB81C4259
-10, -12, -15 256Kx4
MB81C1000
-10, -12, -15 1Mx1
MB81C1001
-10, -12, -15 1Mx1
MB81C1002
-10, -12, -15 1Mx1
MB81C1003
-10, -12, -15 1Mx1
MB85208
-17, -20, -25 32Kx8
MB85201
-10, -12 1Mx1
MB81C258
-10, -12, -15 256Kx1

MB85108A
-10, -12 256Kx1
MB85103A
-12, -15 64Kx8
MB85101A
-10, -12 64Kx4
MB81C466
-10, -12, -15 64Kx4
MB81464
-10, -12, -15 64Kx4
MB81461
-12, -15 64Kx4
MB8266A
-10, -12, -15 64Kx1
MB8265A
-10, -12, -15 64Kx1
MB8264A
-10, -12, -15 64Kx1
MB85237
-10 256Kx9 (CMOS)

NON-VOLATILE MEMORY

MBM2212
-20, -25 256Kx8
MB831000
-15, -20 128Kx8
MB831124
-35 128Kx8

MBM27C1000
-20, -25 128Kx8
MBM27C1001
-20, -25 128Kx8
MBM27C1028
-15, -20, -25 64Kx16
MBM27C1024
-20, -25 64Kx16
MB83512
-15, -20 64Kx8
MBM27C512
-20, -25, -30 64Kx8
MB27C256H
-10, -12 32Kx8
MB83256
-25 32Kx8
MBM27C64
-20, -25, -30 32Kx8
MBM27C64
-25X, -30X/W 32Kx8
MBM27C256A
-20, -25 32Kx8
MBM27C256A
-20W, -25W 32Kx8
MBM27256
-17, -20, -25 32Kx8
MBM27256
-20X, -25X, -30X 32Kx8
MBM27C128
-20, -25 16Kx8
MBM27128
-20, -25, -30 16Kx8
MBM27128
-25X/W, -30X/W 16Kx8
MBM28C64
-25, -35 8Kx8
MBM28C65
-25, -35 8Kx8
MBM2764
-20, -25, -30 8Kx8
MBM2764
-30X, -30W 8Kx8

4-BIT MICRO-CONTROLLERS

MB8840 SERIES
48-PIN FPT
42-PIN DIP
28-PIN DIP
MB8850/H/B SERIES
48-PIN FPT
MB88200/H/B SERIES
16-PIN DIP
16-PIN FPT
MB88210 SERIES
20-PIN DIP

MB88400/H SERIES
48-PIN FPT
MB88410/H SERIES
42-PIN DIP
48-PIN FPT
MB88420/H SERIES
64-PIN DIP
MB88500/H SERIES
48-PIN FPT
42-PIN DIP
MB88510/B SERIES
64-PIN DIP
42-PIN DIP
MB88520/B SERIES
64-PIN DIP
64-PIN FPT
MB88530 SERIES
42-PIN DIP
48-PIN FPT
MB88540 SERIES
70-PIN FPT
80-PIN FPT
MB88550 SERIES
80-PIN FPT
MB88560 SERIES
80-PIN FPT
MB88P500/H SERIES
48-PIN FPT
MB88700 SERIES
64-PIN FPT

8-BIT MICRO-CONTROLLERS

MBL8749
EPROM
40-PIN DIP
MBL8742
EPROM
40-PIN DIP
MBL8649
40-PIN DIP
MBL80C39
CMOS SINGLE CHIP MCU
MBL80C49
CMOS SINGLE CHIP
MBL8039
MCU 128B RAM
MBL8C49
2KB ROM 128B RAM
MBL8035
MCU 64B RAM
MBL8048
1KB ROM 64KB RAM
MBL8042
UNIVERSAL PERIPH. INTERFACE
MBL8051AH
256B RAM
MBL8031AH
4KB ROM 245B RAM

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MB80188
 NMOS MPU
 68-PIN LCC
MB8089/-2
 I/O 40-PIN DIP
MB8088/-2
 NMOS 40-PIN DIP
MBL80286
 NMOS MPU
 68-PIN LCC
MBL80186
 NMOS MPU
 68-PIN LCC
MBL8086/-1/-2
 MPU 40-PIN DIP

PERIPHERALS

MB8868A
 MOS UART
 (TR1602A
 COMPATIBLE)
MBL82288
 BUS CONTROLLER
MBL82284
 CLOCK GENERATOR
MBL82C43
 INPUT/OUTPUT
 EXPANDER (CMOS)
MBL8243
 INPUT/OUTPUT
 EXPANDER
MBL8289
 BUS ARBITER
MB89289
 BUS ARBITER
 (CMOS)
MBL8288
 BUS CONTROLLER
MB89288
 BUS CONTROLLER
 (CMOS)
MBL8287
 BIPOLAR OCTAL BUS
 TRANSCEIVER
MB89287
 BIPOLAR OCTAL BUS
 TRANSCEIVER
 (CMOS)
MBL8286
 BIPOLAR OCTAL BUS
 TRANSCEIVER
MB89286
 BIPOLAR OCTAL BUS
 TRANSCEIVER
 (CMOS)
MB89237A
 DMA CONTROLLER
 (CMOS)

MB89251A
 SERIAL DATA
 TRANSMITTER
 (CMOS)
MB89254
 PROGRAMMABLE
 INTERVAL TIMER
 (CMOS)
MB89255A
 PARALLEL DATA
 INPUT/OUTPUT
 UNIT (CMOS)
MBL8284A
 CLOCK GENERATOR
 & DRIVER
MB89284A
 CLOCK GENERATOR
 & DRIVER (CMOS)
MBL8283
 BIPOLAR OCTAL
 LATCH
MB89283
 BIPOLAR OCTAL
 LATCH (CMOS)
MBL8282
 BIPOLAR OCTAL
 LATCH
MB89282
 BIPOLAR OCTAL
 LATCH (CMOS)
MBL8259A/-2
 PROG. INTERRUPT
 CONTR.
MBL89259A/-2
 PROG. INTERRUPT
 CONTR. (CMOS)
MB88308/9
 CMOS OUTPUT
 EXPANDER
MB88306/7
 CMOS OUTPUT
 EXPANDER
MB88304/5
 NMOS 4/8-BIT I/O
 EXPANDER
MB4107
 DATA SEPARATOR
MB1412AC
 LS-TTL ERROR
 CHECKING/
 CORRECTION
 CIRCUIT (ECC)
MB1426
 16-BIT ECC
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 CONTROLLER

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MB89322
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 (6845 COMPATIBLE)
 (CMOS)
MB89321
 CRT CONTROLLER
 (6845 COMPATIBLE)
 (CMOS)
MB89311
 FLOPPY DISK
 CONTROLLER
MB88303P
 TELEVISION DISPLAY
 CONTROLLER
TELECOM
MB87006
 PLL
MB87004
 DTMF/PULSE DIALER
MB87003
 DTMF/PULSE DIALER
MB87001
 SYNTHESIZER
 SYSTEM BLOCK
MB6024
 CODEC
MB6022
 CODEC
MB6021
 CODEC
MB501/L
 TWO MODULUS
 PRESCALER
MB503/504/506
 TWO MODULUS
 PRESCALER
LINEAR
MB3712
 POWER AMP
MB3713
 POWER AMP
MB3722
 POWER AMP
MB3714A
 POWER AMP
MB3737
 POWER AMP
MB3730
 12W BTL
 AUDIO AMP
MB3731
 18W BTL
 AUDIO AMP
MB3752
 VOLTAGE
 REGULATOR

MB3759
 PULSE WIDTH
 MODULATION
 (PWM) CONTROL
MB3760
 PWM CONTROL
 CIRCUIT
**DSP (DIGITAL
 SIGNAL
 PROCESSORS)**
MB8764CR
 -001 88-PIN PGA
MB8764CV
 -001 84-PIN LCC
MB8764PR
 -001 88-PIN
 PLASTIC PGA
MB87064P
 42-PIN PLASTIC DIP
MB87064C
 42-PIN CERAMIC
 DIP
MB87069C
 64-PIN CERAMIC
 PGA
SCSI
MB87030
 SYNCHRONOUS S.P.C.
MB89351
 ASYNCHRONOUS
 S.P.C.
CONVERTERS
MB40547
 -7/-8 8-BIT UH
 SPEED A/D
MB40576
 6-BIT UH SPEED
 VIDEO A/D
MB40748
 -8/-9 10-BIT UH
 SPEED D/A
MB40776
 6-BIT UH SPEED D/A
MB40778
 8-BIT HIGH SPEED
 D/A
MB40788
 10-BIT UH SPEED
 D/A
MB88301A
 6-BIT PWM NMOS
 D/A
MB4052
 4 CHANNEL 8-BIT
 A/D

MB4053/63
 6 CHANNEL 8-BIT
 A/D SUBSYSTEM
MB4072
 8-BIT HIGH SPEED
 MULTIPLYING D/A
ETHERNET
MB8795
 ETHERNET
 CONTROLLER
MB87012
 802.3/ETHERNET
 CONTROLLER
MB502
 MANCHESTER
 ENCODER/DECODER
**CMOS GATE
 ARRAYS**
UH SERIES:
C2000UH
 20,160 GATES
UM SERIES:
C15006UM
 15,120 GATES
 + 6K RAM
C10012UM
 10,080 GATES
 + 12K RAM
UHB SERIES:
C12000UHB
 12,734 GATES
C8700UHB
 8,768 GATES
C6000UHB
 6,000 GATES
C4100UHB
 4,174 GATES
C3000UHB
 3,066 GATES
C2200UHB
 2,220 GATES
C1700UHB
 1,724 GATES
C1200UHB
 1,233 GATES
C830UHB
 830 GATES
C530UHB
 530 GATES
C330UHB
 336 GATES
AV SERIES:
C8000AV
 8,000 GATES
C6600AV
 6,664 GATES

C5000AV
 5,022 GATES
C3900AV
 3,900 GATES
C2600AV
 2,640 GATES
AVB SERIES:
C2000AVB
 2,052 GATES
C1600AVB
 1,674 GATES
C1200AVB
 1,245 GATES
C850AVB
 852 GATES
C540AVB
 549 GATES
C350AVB
 357 GATES
C4002AVM
 4,087 GATES
 + 2K RAM
C2301AVM
 2,375 GATES
 + 1K RAM
C1502AVM
 1,564 GATES
 + 2K RAM
**CMOS
 STANDARD
 CELLS**
AV SERIES:
 1.8μ 2-LAYER METAL
 16K RAM, 64K ROM,
 PLAs, REGISTERS
 SPECIAL LSI
 FUNCTIONS
 >13K GATES
 2 INPUT GATE
 EQUIVALENT

< 1.4ns TYPICAL
 < 2.2ns WORST CASE
AU SERIES:
 1.3μ DUAL-WELL,
 2 AND 3 LAYER
 METAL
 32K RAM, 128K ROM,
 PLAs, REGISTERS,
 MULTIPLIERS, ALU
 STANDARD LSI
 EQUIVALENT
 FUNCTIONS
 > 40K GATES
 2 INPUT GATE
 EQUIVALENT
 < 0.8ns TYPICAL
 < 1.3ns WORST CASE
**BIPOLAR LSTTL
 GATE ARRAYS**
EQUIVALENT GATES
 (2 INPUT GATES)
B240
 360 GATES
B350
 540 GATES
B350B
 528 GATES
B600
 924 GATES
B700B
 1,080 GATES
B1100
 1,680 GATES
B2000
 3,162 GATES
**BIPOLAR ECL
 GATE ARRAYS**
EQUIVALENT GATES
 (2 INPUT GATES)
ET750
 1,136 GATES

ET1500
 2,192 GATES
ET3000
 4,344 GATES
ET4500
 6,280 GATES
ET2009
 2,640 GATES
 + 9K RAM
ET3004
 3,960 GATES
 + 4K RAM
PACKAGING
**PLASTIC PIN GRID
 ARRAYS**
**FLAT PACK GULL
 WINGS**
**256-PIN CERAMIC
 GRID ARRAYS**
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 J LEADS (SOJ)**
**PLASTIC ZIG-ZAG
 IN-LINE (ZIP)**
SHRINK DIPs
SKINNY DIPs
SMALL OUTLINE DIPs
**SINGLE IN-LINE
 PACKAGE (SIP)**
**SINGLE IN-LINE
 MODULES**
**PLASTIC GRID
 ARRAYS (PGA)**
**CERAMIC GRID
 ARRAYS (PGA)**
PLASTIC LCCs
CERAMIC LCCs
PLASTIC FLAT PACK
CERAMIC FLAT PACK
**FLAT PACKS w/
 HEAT SINKS**
SMALL OUTLINE DIP



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OLD PALS

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Let's face it, when you tackle those really tough digital design jobs, you often need more help than your old pals can give.

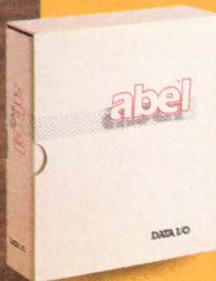
That's why we've invented the ERASIC (Electrically Reprogrammable ASIC)-to make those jobs a lot easier. It's the next generation PLD that programs like a traditional PLD, but performs like a Gate Array.

Like a conventional PLD, the ERASIC E² PLD is field programmable. But like a Gate Array, its logic structures are very flexible. And because it is based on E²CMOS technology, it's reprogrammable up to 10,000 times and consumes very little power.

So, if you've outgrown your old pals and are ready to move on, take a good look at the ERASIC, the next generation E² PLD.

IT'S FLEXIBLE

While it's pin-compatible with the best known 24-pin PLDs, the ERASIC E² PLD gives you a lot more, like multi-level logic and reprogrammability. Multi-level logic lets you cascade your logic up to 42-levels deep, giving you the ability to create complex internal logic circuits (even with buried Flip-flops) without using valuable I/O pins. Flexibility like this can make life a lot easier for the logic designer who's struggling with the limitations of old-fashioned AND-OR logic planes.

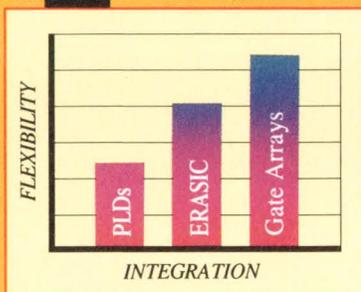


With ERASIC E² PLDs, you avoid restrictive architectures, wasteful power consumption and the problems of custom silicon. Simply put, it's a lot more fun at a lot less cost.

IT'S ABEL™ COMPATIBLE

The ERASIC is a snap to program, too. Using DATA I/O's popular ABEL™ and EXEL's MultiMap™ and MultiSim™ enhancement programs, you can implement true gate array-type logic, fast.

Plus, conversion of your existing PAL®-based designs can be as easy as changing the part number in your ABEL design file.



GET STARTED FAST

We've got all the tools you need to get your design going with the E² PLD that performs like a Gate Array.

Call today for the ERASIC brochure and data sheet and find out what a friend the ERASIC E² PLD can be.

Our location is 2150 Commerce Drive, San Jose, CA 95131. Telephone (408) 432-0500, TWX 910-338-2116, TELEX 171339.

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EXCELLENCE IN E²

CIRCLE NO 212

**FAST
CACHE.**

Introducing the MK41H80 TAGRAM™ from Thomson-Mostek. The industry's first and fastest integrated 16K CMOS cache tag SRAM dedicated for use in all high-speed processor environments.

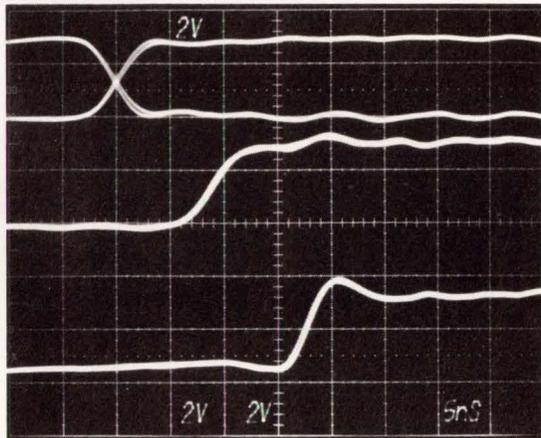
TAGRAM gives you a 4K x 4 CMOS SRAM and a 4-bit comparator integrated on a single chip. It's optimum for interface with 16-25 MHz processors, and is backed by 1.2μ double level metal full CMOS process technology – the same proven process used in all Thomson-Mostek 16K VF SRAMs.

TAGRAM comes in three speed grades: 20, 25 and 35ns. And every MK41H80 cache TAGRAM is available in 300 mil, 22-pin plastic and ceramic DIPs. What's more, TAGRAM's full-

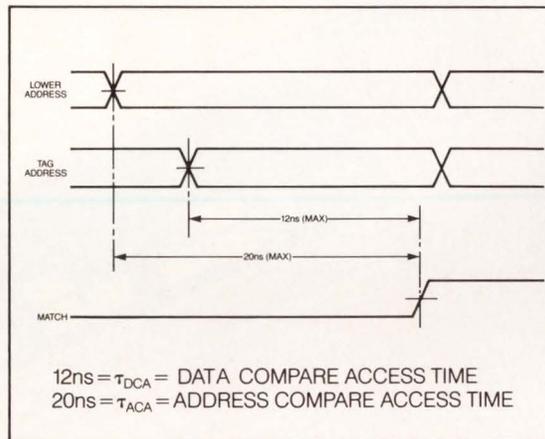
speed read access ensures that even copy-back designs can be implemented without ever having to wait. And it features Flash Clear – the function requested most often by cache system designers. So your cache can be wiped clean to all zeros in 40ns. Max.

High-performance cache applications demand high-speed solutions. If you'd like to realize a 30% reduction in access time compared to discrete solutions – plus a substantial reduction in the cost of component real estate – start increasing your cache flow with the newest member of our family. The MK41H80 TAGRAM.

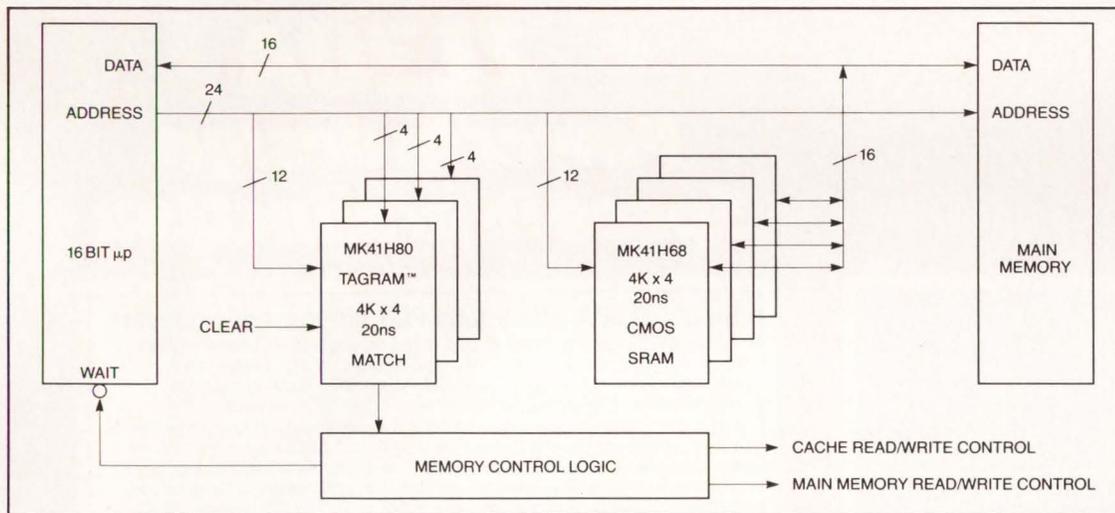
We're Thomson-Mostek. And we perform.



Actual MK41H80 TAGRAM Scope Trace Photograph



Match Access Timing



Direct Mapped Cache System Block Diagram

DEVICE	CONFIG	PINS	CE	CS	OE	CLR	MATCH
41H68	4Kx4	20	X				
41H69	4Kx4	20		X			
41H78	4Kx4	22	X		X		
41H67	16Kx1	20	X				
41H66	16Kx1	20		X			
41H79*	4Kx4	22	X		X	X	
41H80	4Kx4	22			X	X	X

Other available Fast Static RAMs from Thomson-Mostek

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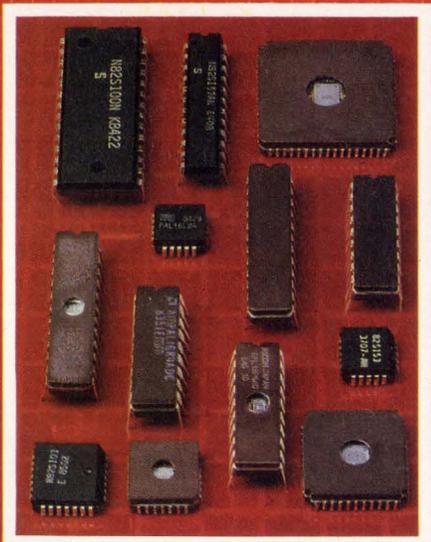


*To be announced. TAGRAM is a trademark of Thomson Components-Mostek Corporation.



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Speed in production



Stag's ZL30A offers total PLD programming support

Stag Microsystem's model ZL30A is the first dedicated Logic Programmer of its kind that not only supports programming of PLDs, EPLDs, and GALs*, in a variety of 20, 24, 28 and 40 pin DIP, but also supports programming of the latest surface mounted PLCC/LCC devices.

Stag's ZL30A contains features that have made it the industry standard in both engineering and production environments. Salient among these are:

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- Comprehensive device library
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*CUPL is a trademark of Assisted Technology

NEWS BREAKS

EDITED BY JOAN MORROW

DATA-SEPARATOR IC OPERATES AT 33M-BPS TRANSFER RATE

Adaptec Inc (Milpitas, CA, (408) 432-8600) now offers a data-separator chip that operates at data rates as fast as 33M bps. The AIC-6225 will be sold into controller applications for data-storage products. Controllers that use the chip will provide compatibility with all popular data-encoding schemes, such as MFM, 2,7 RLL, and 1,7 RLL. The chip can also be used in certain instrumentation applications. It ranges in price from \$11 (1000) for a 10M-bps version to \$28 (1000) for the 33M-bps part. The company plans to begin volume shipments in the 3rd qtr.—Maury Wright

HIGH-RESOLUTION GRAPHICS SYSTEM SUPPORTS 32 BITS / PIXEL

The Pixel Machine, a graphics accelerator add-on box for high-end graphics workstations, will be shown by AT&T (Holmdel, NJ) at Siggraph '87 (Anaheim, CA, July 27 to 31). It can operate at 820M flops and transform 200,000 vectors/sec. Capable of 1024x1024-bit resolution with 32-bit-deep pixels, the accelerator, when teamed with a Sun workstation, can support mechanical CAD/CAM, medical imaging, and animation, all in 3-D. The accelerator is based on AT&T's 32-bit floating-point DSP μ P, the DSP32. Its modular parallel design allows as many as 82 μ Ps in a system. The cost will vary from \$50,000 to \$100,000, depending on the number of DSP μ Ps.—Margery S Conner

SCSI PROTOCOL CHIP FEATURES ASYNCHRONOUS, SYNCHRONOUS MODES

Emulex Corp (Costa Mesa, CA, (714) 662-5600) and NCR Corp (Colorado Springs, CO, (800) 334-5454) have jointly announced availability of a SCSI protocol IC. The chip, the NCR 53C90 Enhanced SCSI Processor (ESP) and Emulex SCSI Processor (ESP), was developed by Emulex, will be manufactured by NCR, and will be sold by both companies. The IC operates in synchronous (4.8M-byte/sec) and asynchronous (4M-byte/sec) modes. The ESP includes a pipelined command queue and processes combinations of SCSI bus phases under state machine control. The chip costs approximately \$25 (1000) from either company; you can buy samples now.—Maury Wright

INEXPENSIVE TOUCH SCREEN FURNISHES TWO ACTIVE COMPONENTS

Shunning the typical LED-array approach to building optical touch screens, the engineers at Wells-Gardner Electronics (Chicago, IL, (312) 252-8220) built the Cyclops ES Series touch screen with one LED and one charge-coupled device (CCD) consisting of a linear array of photodiodes. The screen uses retroreflective material on two sides of the frame assembly to reflect light from the LED to the CCD element. The CCD measures the angle of reflected light, compares the angle to an average value, and generates an optical pattern in the unit's μ P. The unit determines X-Y positions via triangulation. A 4x9-in. flat-panel screen costs \$115 (10,000).—J D Mosley

X WINDOWS PORTED TO UNIX FOR 80386-BASED SYSTEMS

GSS*X/386 is a windowing, multitasking, and networking environment for 80386-based systems running Unix. GSS*X/386 is based on X Windows, a public-domain windowing standard for Unix systems developed by MIT and supported by companies such as IBM, Hewlett-Packard, and Sun. The environment allows you to run software (including another operating system, such as MS-DOS) as a task under Unix. This capability lets your 80386-based system run Unix, a true 32-bit operating system, and still retain access to the huge existing base of MS-DOS software. A \$595 developer's kit will be available from the manufacturer, Graphic Software Systems (Beaverton, OR, (503) 641-2200), in the 4th qtr of 1987.—Margery S Conner

NEWS BREAKS

LOW-COST MICROCODE DEVELOPMENT TOOL RUNS ON PCs

Coupled with the company's MetaStep microcode assembler, the MicroStep interface card from Step Engineering (Sunnyvale, CA, (408) 733-7837) transforms an IBM PC, PC/AT, or compatible computer into a microcode development system. Cables from the card plug into RAM, ROM, or PROM sockets in the target system, emulating the target's writable control store (WCS) memory. The product accommodates WCS memories to 4000 words of 128 bits and uses 25-nsec RAMs for emulation memory. Step sells the MicroStep interface card and control software for \$3695 and the MetaStep assembler for \$3000. Currently, the company offers a package including the interface card and assembler for \$6195.—Steven H Leibson

PC-BOARD DESIGN SYSTEM SUPPORTS SMT AND HSPICE SIMULATION

By using the latest release of PCB WorkSystem from Tektronix (Santa Clara, CA, (408) 727-1234), you can now design pc boards with SMDs on the top and bottom surfaces, and interstitial (blind and buried) vias for high component density. Color-coding and offset component alignment let you differentiate between the two surface layouts. The WorkSystem automatically routes as many as three traces per pad and provides user-selectable routing strategies. You can also define router passes, mix SMDs with through-hole devices on the board, and specify separate clearances between vias, traces, and pins. The PCB WorkSystem includes an Apollo Domain DN3000 workstation, Tektronix's Designer's Database Schematic Capture, Merlyn-P PCB physical-layout software, and a TTL library for \$49,900. Or you can order the PCB WorkSystem software with a VAXstation II/GPX workstation for \$100,000. An optional HSPICE Simulation System for analog-design verification costs \$18,000.—J D Mosley

THREE FAST, 16k-BIT STATIC RAMs DRAW LITTLE CURRENT

Featuring maximum standby currents of a measly 2 μ A, the three members of Vitelic's (San Jose, CA, (408) 433-6000) 16k-bit static-RAM family achieve access times as fast as 35 nsec. The V61C16, V61C67, and V61C68 have 16k \times 1-, 4k \times 4-, and 2k \times 8-bit architectures and cost \$3.71, \$3.24, and \$3.38, respectively. (Prices are for 55-nsec parts in plastic DIPs.) The company offers the RAMs in commercial (0 to 70°C), industrial (-40 to +85°C), and extended (-55 to +125°C) grades.—Steven H Leibson

CACHING CONTROLLERS IMPROVE IBM PC/AT DISK PERFORMANCE

The PM3011/50 and PM3011/70 IBM PC/AT-compatible caching disk controllers handle ST-506/412 and ESDI (Enhanced Small Device Interface) Winchester, respectively. Distributed Processing Technology (Maitland, FL, (305) 830-5522) offers the boards with 512k bytes of onboard RAM; you can expand the cache in 3M- or 6M-byte increments to 16M bytes. On cache hits, the controllers feature access times of 0.5 msec with no rotational latency. The basic boards cost \$600 (1000).—Maury Wright

LOW-COST STD BUS μ P BOARD RETAINS PC-DOS COMPATIBILITY

If you can fit your STD Bus MS-DOS application programs into 62k bytes of user memory, you may be able to save on the price of a μ P board. The STD Mini-DOS μ P board from Ziatech (San Luis Obispo, CA, (805) 541-0488) trades this reduced memory for a lower price (well under \$500 in OEM quantities). In addition to Ziatech's STD DOS and BIOS, the board contains a 5- or 8-MHz 8088, a 128k-byte PROM disk, two 8-bit parallel I/O ports, a serial port, a battery-backed configuration file and real-time clock, an 8256 MUART, and provision for an 8087 math coprocessor.—Margery S Conner

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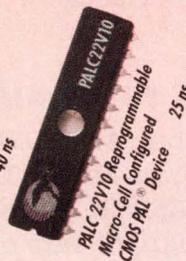
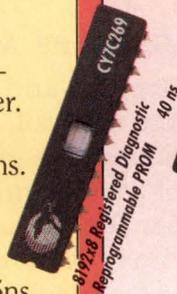
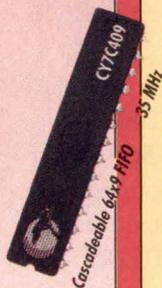
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NEWS BREAKS: INTERNATIONAL

OPTICAL-FIBER GATEWAY LINKS ISOLATED ETHERNET LANs

The Intracomm-7 communications gateway links geographically isolated Ethernet LANs together, via an optical-fiber wide-area network, so that the Ethernet LANs appear to operate as a single unified network. Manufactured by Logic Replacement Technology Ltd (Reading, UK, TLX 847395), the gateway is protocol independent, requiring only that the connected LANs conform to IEEE-802.3 specifications.

The bidirectional link operates at speeds as high as 2M bps, and the gateway can buffer as many as 128 Ethernet packets. Access security facilities are provided, and at one end of the link, you can connect a terminal to analyze network performance or to perform network management tasks. Priced at approximately £9000, the gateway includes Ethernet interfaces for both ends of the link and the optical-fiber modems.

—Peter Harold

ADD-IN FOR IBM PC/XT AND PC/AT ASSISTS DSP DEVELOPMENT

Equipped with four A100 DSP chips and a T212 16-bit Transputer, the B009 DSP evaluation board from Inmos Ltd (Bristol, UK, TLX 444723; in the US, (303) 630-4000) can perform 128-tap FIR (finite impulse response) filtering, using 16-bit data and coefficients, at a throughput rate of 2.5M samples/sec (10M samples/sec with 4-bit coefficients). You can cascade the boards to create more complex DSP systems. The D703 software package provides a library of common DSP algorithms and allows you to model your DSP system before committing it to hardware. An optional piggyback module for the evaluation board, with a T414 32-bit transputer and 1M byte of RAM, provides a host processor capable of supporting the company's Occam transputer development environment. A complete system supplied with both transputers and DSP and transputer development software sells for \$7500.—Peter Harold

SINGLE IC PROVIDES CLOSED-LOOP MOTOR SPEED CONTROL

The ZN410 universal motor speed controller IC from Ferranti Electronics Ltd (Oldham, UK, TLX 668038; in the US, (516) 543-0200) provides all the functions required for closed-loop phase control of ac motors. The IC has a tachometer input suitable for the direct connection of a magnetic coil speed sensor, and the chip produces negative firing pulses for a triac. Features include optional current limit or current trip, soft-start circuitry, and an on-chip shunt regulator, which allows you to power the IC from the line supply. The chip costs £0.81 (1000).—Peter Harold

CHARACTER RECOGNITION SOFTWARE DESIGNED FOR PCs

Ricoh Co has developed a character recognition program that allows a personal computer to function as an optical character reader with an accuracy of 99% for both handwritten and printed letters. The program, which was developed for Nippon Electric's PC-9801 and IBM's PC/AT, is designed to be used with an image scanner. The software sells for ¥200,000 (\$1429), and the scanner costs \$2129. The system lets personal computers read alphanumeric characters and codes at 20 characters/sec for printed letters and 7 characters/sec for handwritten letters.—Joan Morrow



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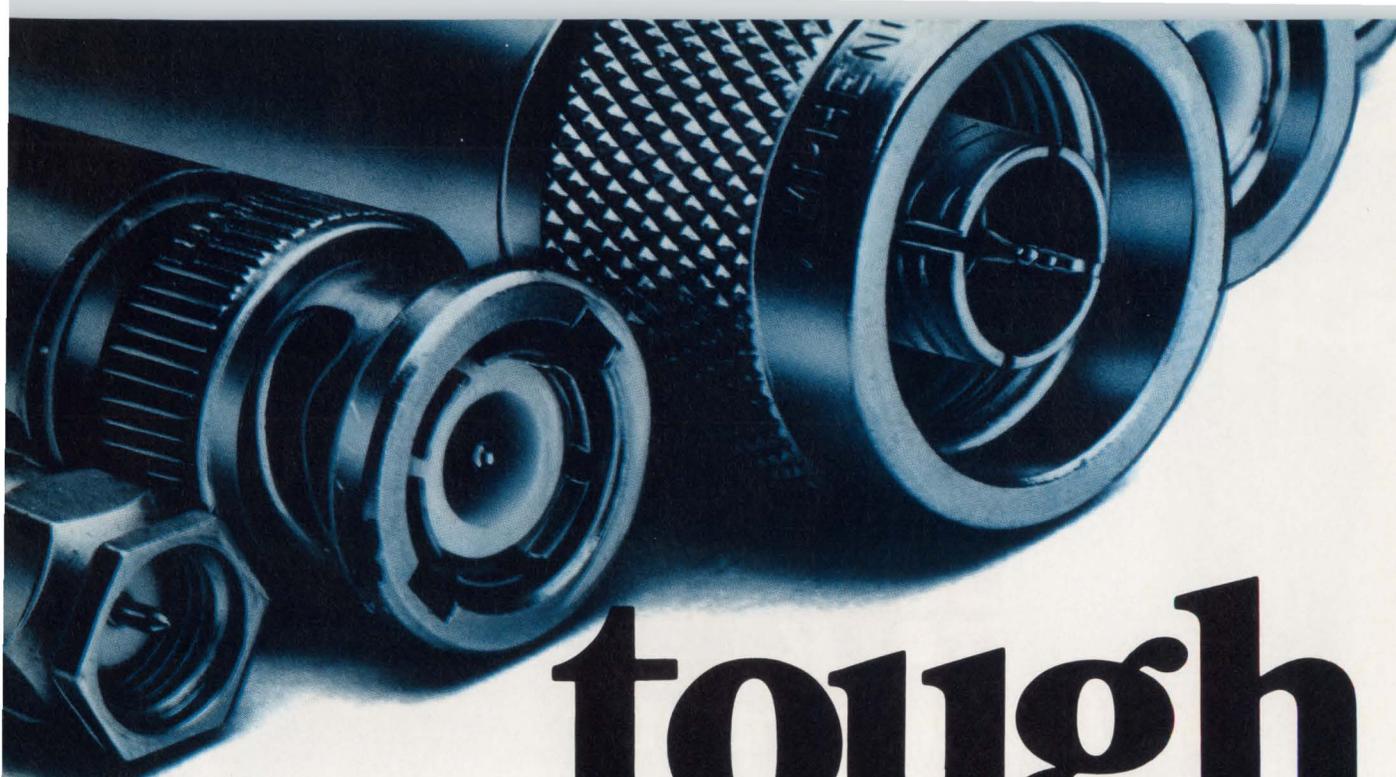
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		DC-1000	1000-1500	DC-1000 MHz	1000-1500 MHz
DC-1500 MHz	±0.3	0.6	0.8	1.3	1.5

*DC-1000 MHz (all 75 ohm or 30 dB models) DC-500 MHz (all 40 dB models)

MODEL AVAILABILITY

Model no. = a series suffix and dash number of attenuation.

Example: CAT-3 is CAT series, 3 dB attenuation.

■ denotes 75 ohms; add -75 to model no.

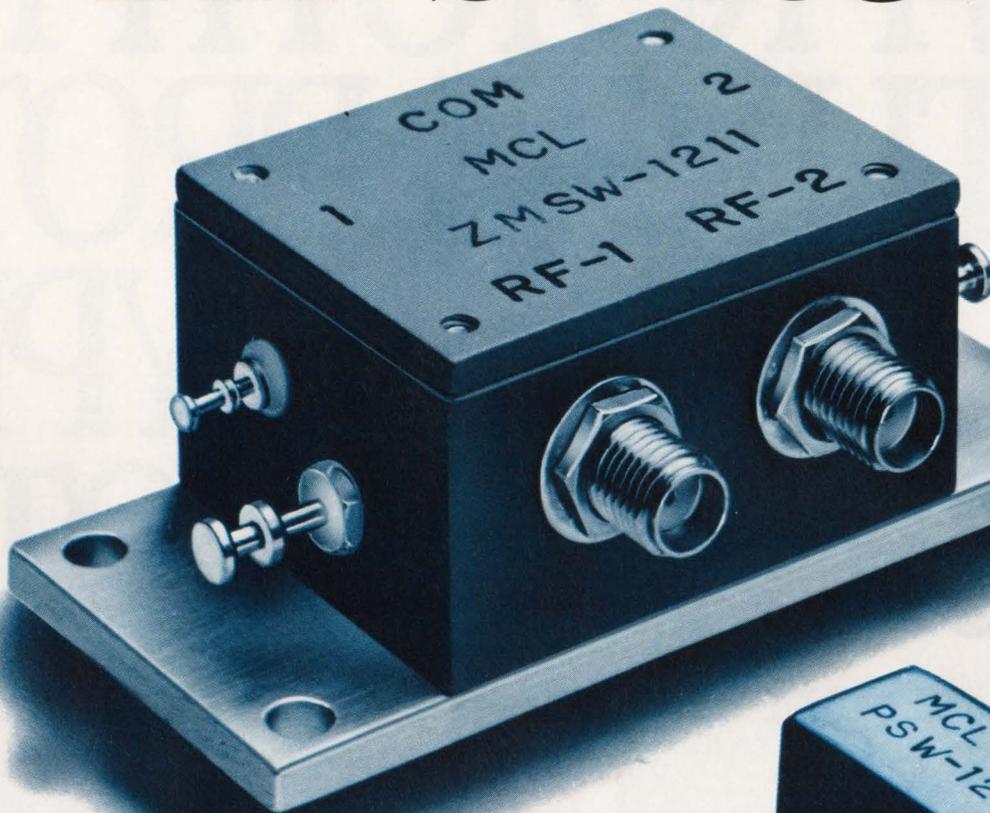
● denotes 50 ohms

ATTEN	SAT (SMA)	CAT (BNC)	NAT (N)	TAT (TNC)
1	●	●	●	●
2	●	●	●	●
3	●	●	●	●
4	●	●	●	●
5	●	●	●	●
6	●	●	●	●
7	●	●	●	●
8	●	●	●	●
9	●	●	●	●
10	●	●	●	●
12	●	●	●	●
15	●	●	●	●
20	●	●	●	●
30	●	●	●	●
40	●	●	●	●

PRICING (1-49 qty.): CAT (BNC)..\$11.95, SAT (SMA)..\$14.95
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C 92 REV. B

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INSERTION LOSS	
10-2000 MHz	1.7 dB max.
2000-2500 MHz	2.7 dB max.
ISOLATION	
10-500 MHz	40 dB min.
500-1000 MHz	30 dB min.
1000-2000 MHz	25 dB min.
2000-2500 MHz	20 dB min.
SWR	1.5 max. ("on" state)
SWITCHING SPEED	1 μ sec. (max.)
MAXIMUM RF INPUT	+20 dBm
CONTROL	+5 V (5 mA max.)
OPERATING TEMPERATURE	-54°C to +100°C
STORAGE TEMPERATURE	-54°C to +100°C

PRICE (6-24)	(1-4)
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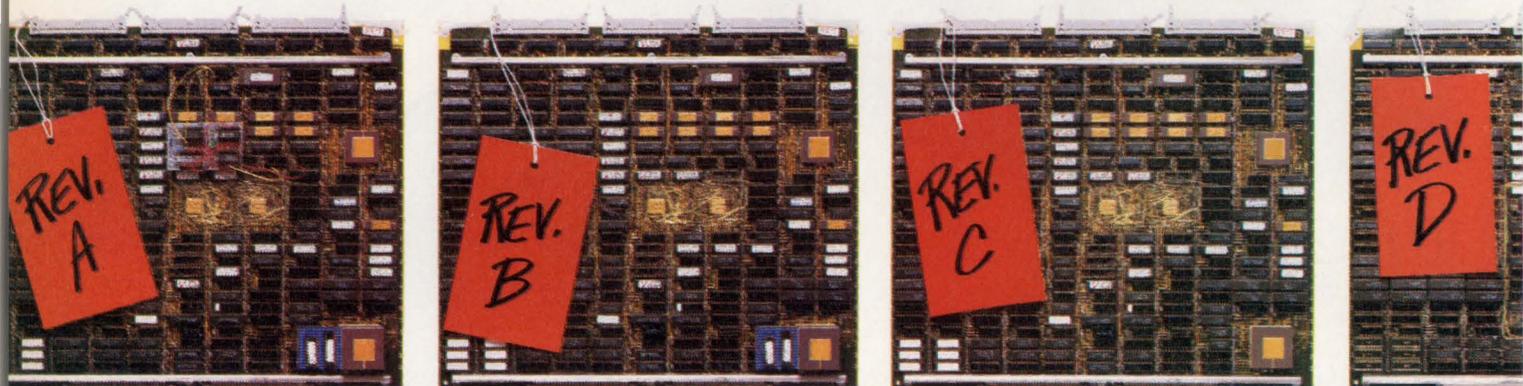
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CIRCLE NO 214

C80 REV. B

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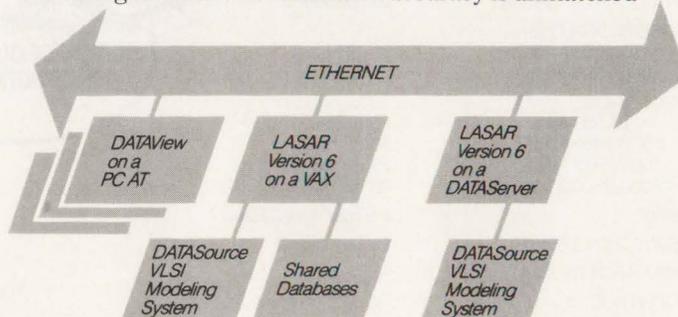
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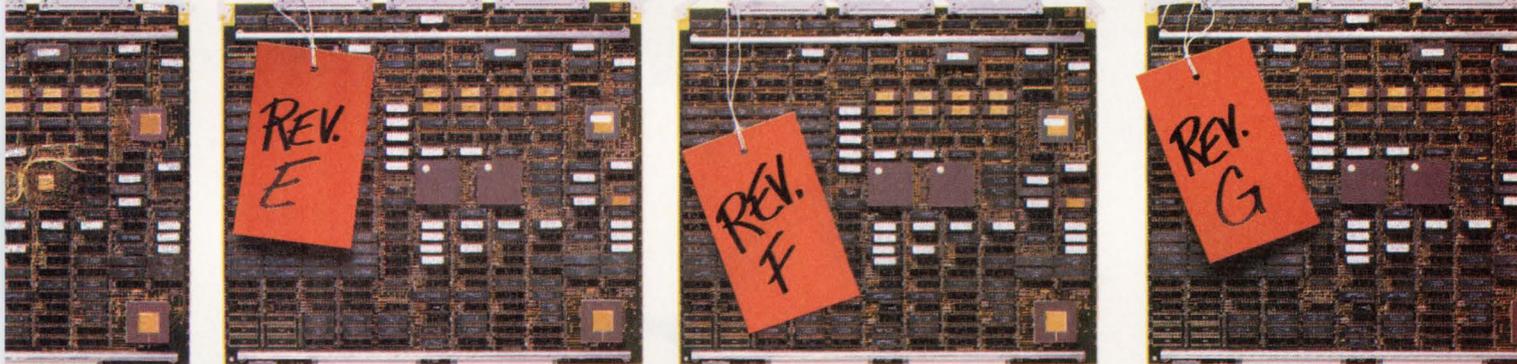
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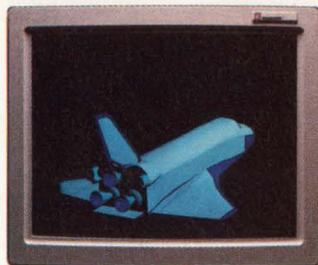
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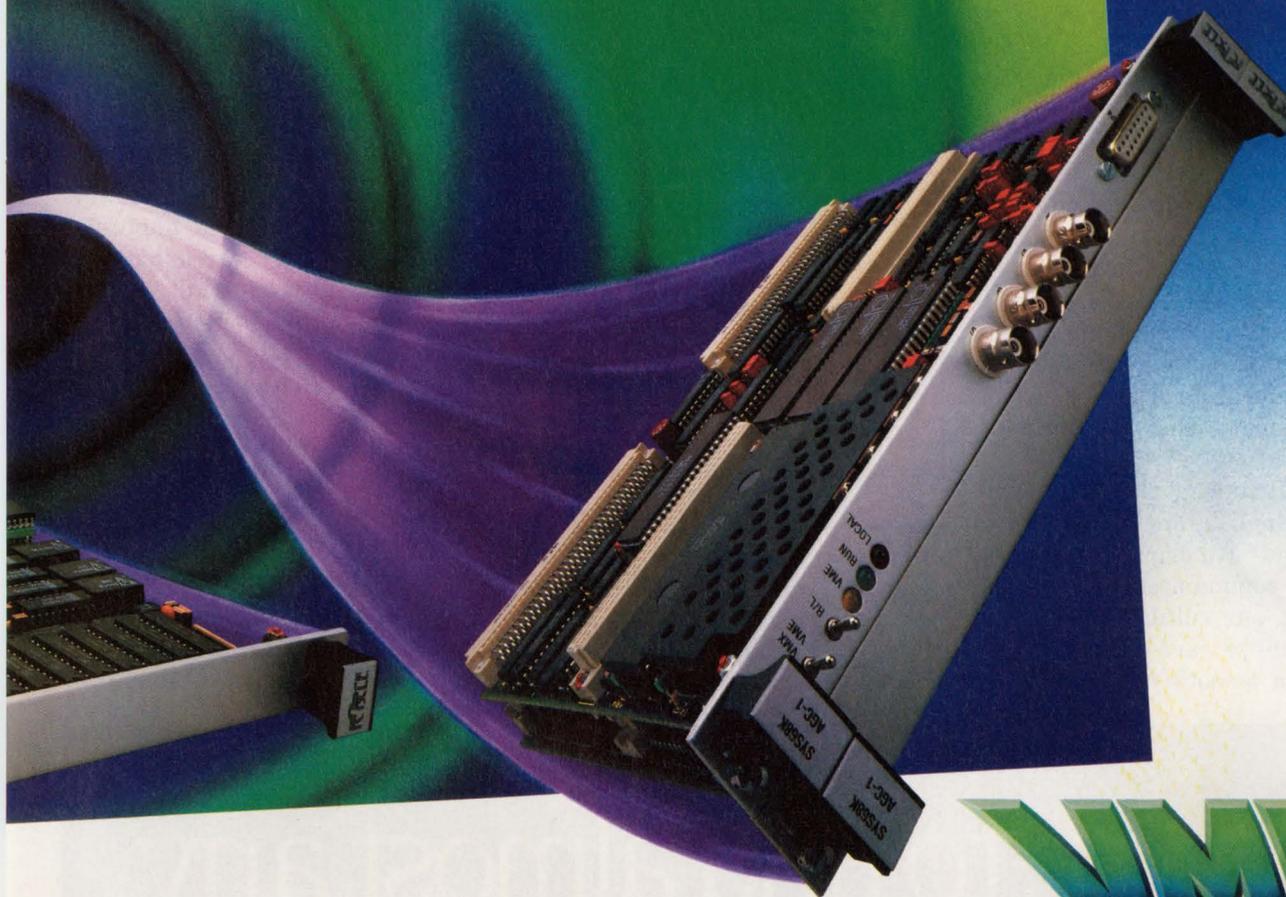


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	Interface	8xRS232/RS422	SCSI/SA 460	RS434 (RGB)
	Speed	RS232 : 38400 baud RS422 : 2 M baud	1.5 Mbit/sec	64 MHz pixel frequency 1600x1280 pixels
Software	Driver support	PDOS*, UNIX* V	PDOS*, UNIX* V	PDOS*, UNIX* V
	Unique SW packages	firmware based on real time kernel	hashing and caching firmware	GKS 2.0b
Availability		now	now	now

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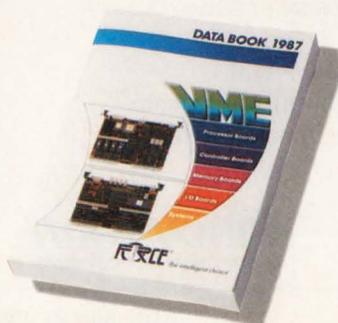
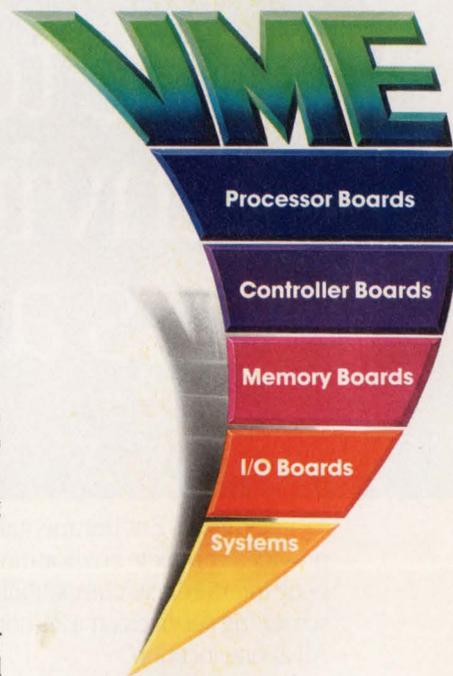
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CIRCLE NO 157

SIGNALS & NOISE

Learning Japanese promotes understanding

In the Professional Issues column in EDN's March 4 issue (pg 227), Pat Hill Hubbard brings out an important point regarding communication in a native language. Although it may be said that engineering is based on a "universal" mathematical language, the interaction and development of those who actually do the engineering is influenced by their environment. The flow of information about that environment is a function of communicative impedance, if you will. In other words, you can't assimilate what you don't understand.

The Japanese, through their study of English, are better able to understand American concepts, which are communicated within the context of our culture. The effort the Japanese are making has provided a smoother flow in their



direction.

For us, comprehension of Japanese designs and systems is a good start, but it may be even more important to appreciate the engineer-

ing/business approaches and philosophies that have yielded the successes of the Japanese. I feel that truly learning the Japanese language, which of necessity means learning the culture as well, would greatly facilitate that appreciation.

As both a working engineer and a graduate student, I find that free time is often at a premium. However, the sacrifice I (and hopefully other Americans) now make in taking a Japanese class will prevent that premium from increasing in the future.

Douglas J Hillman
Moog Inc
East Aurora, NY

A different opinion on switching losses

Charles H Small's article "Magnetic materials provide the final piece to the high-frequency switching-sup-

Text continued on pg 38

Where to find almost any test environment on Earth. Plus a few that aren't.

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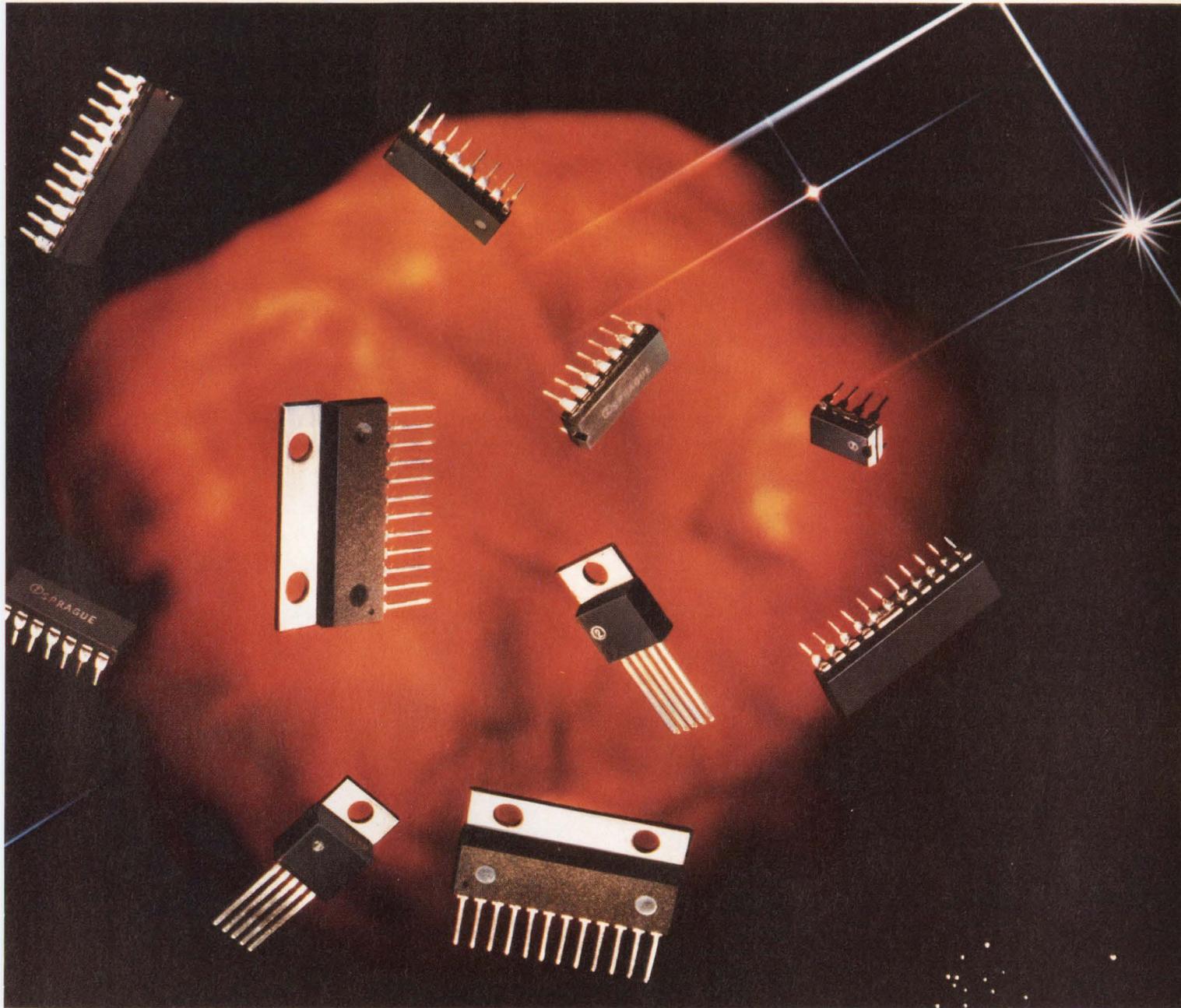
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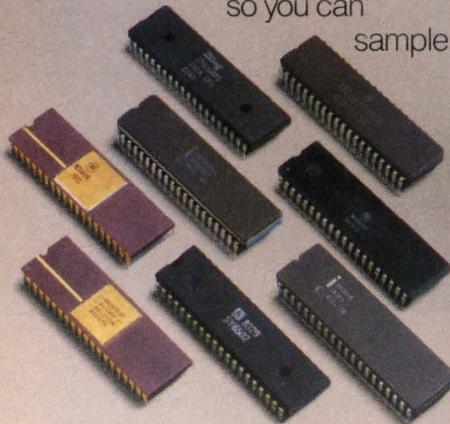
Introducing the Tek 1220 and 1225: the two newest members of the Tek 1200 Series of logic analyzers.

Nothing else in their price range delivers so much and makes it all so easy to use. Consider:

1 Powerful state, timing and disassembly analysis.

The 1220 and 1225 provide 32 or 48 data channels, respectively, in groups of 16-channels, with channel groups clocked independently or linked together — so you can

sample



data from as many as three circuit sections at once.

Tek currently provides support for the most popular microprocessors, with additional 8- and 16-bit personality modules to be

introduced continually.

2 A total of four 2K nonvolatile memories support each channel.

Acquire data in one memory and compare it to data in any of the three other memories.

Clock/calendar plus storage for up to eight test set-ups are also in battery-backed memory. Date and time of storage are included with each data memory, so it's easy to find and interpret results.

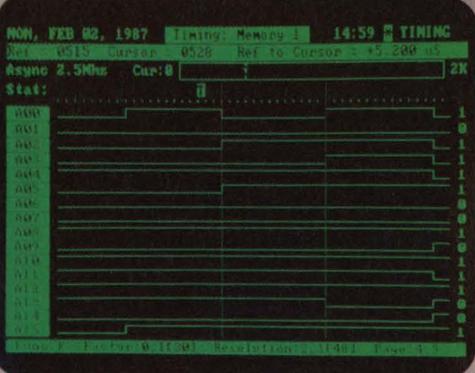


Loc	Addr	Data	Z80 Disassembly	Operation
0504	0503	3A0444	LD A, (4404)	4404=00
0508	0506	FE01	CP 01	
0510	0508	20FF	JR NZ, 040B	
IRIG	0000	C30001	JP 0100	
0515	0100	31FF7F	LD SP, 7FFF	
0518	0103	CDCB04	CALL 04CB	7FFD-0106
0523	04CB	ED4D	RETI	7FFD-0106
0527	0106	CDC802	CALL 02C8	7FFD-0109
0532	02C8	3E4F	LD A, 4F	
0534	02CA	D392	OUT (92), A	92=4F
0537	02CC	3E0A	LD A, 0A	
0539	02CE	D392	OUT (92), A	92=0A
0542	02D0	3E83	LD A, 83	
0544	02D2	D392	OUT (92), A	92=83
0547	02D4	DB90	IN A, (90)	90=01
0550	02D6	3E0F	LD A, 0F	
0552	02D8	D393	OUT (93), A	93=0F
0555	02DA	3E0C	LD A, 0C	
0557	02DC	D393	OUT (93), A	93=0C
0560	02DE	3E83	LD A, 83	

```

MON, FEB 02, 1987 State: Memory 4 14:28 IOBOARD
Loc Bh Bl Ah Al
(00937 differences in displayed bytes)
0510 88 50 1011101 0010001
0511 D4 50 1011101 0011010
TRIG D4 5C 1001101 0011101
0513 D6 7C 1110111 0010000
0514 DE 7E 1110110 0010001
0515 FA 6E 1110110 0110010
STRT 17 CB 0100100 1101101
0517 15 EB 0010010 1100000
0518 1D 53 0110001 1100001
0519 39 F9 0010001 1000100
0520 39 93 0001111 0000111
0521 39 50 0011101 0001000
0522 88 50 1011101 0001001
0523 D4 50 1011101 0011010
STRT FA 4E 1101010 1101101
0525 FA C7 1110100 1110000
0526 5B C7 0110100 1110001
0527 17 C7 0110100 1101010
STRT D6 5C 1001101 0011101
0529 DE 7C 1110111 0010000
Func: Scroll: Cur:0,1 Locate, TRIG:2 Cond:3 Diff:E

```



Use the optional interfaces to control the instruments via computer and attach inexpensive dot matrix printers for immediate documentation.

Left Set reference cursors on the timing diagram to measure pulse width or the time between pulse edges. Above State tables are displayable in binary or hex formats.

3 Triggering can be as simple or sophisticated as you choose.

Specify up to 24 trigger conditions. Conditionally branch with up to 12 levels of IF... THEN... ELSE statements. Cross-trigger between channel groups. Do state and timing analysis simultaneously.

Capabilities like these make the 1220/1225 more than hardware analyzers. They are capable tools for both software debugging and system integration.

4 Pop-up menus are easy to use. Logically arranged. And respond instantly on command.

Push one button for on-screen notes appropriate to the current display.

Above Pop-up menus, such as this main menu, are easy to understand and logically arranged.

5 This is affordable logic analysis in a league by itself.

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SIGNALS & NOISE

ply puzzle" (EDN, March 4, pg 79) was informative, but I'd like to point out that the limiting factor in high-frequency power-supply designs is the losses generated in the semiconductor switches—transistors and diodes—and not necessarily in the magnetic components. By "high-frequency designs," I mean designs in which the converters operate at 500

kHz and above. The high-speed transistors, control chips, and non-magnetic passive components can't easily handle these high frequencies.

Resonant-converter topologies employing zero-voltage or current-switching techniques are being used that do reduce switching losses in the semiconductors. These tech-

niques are enabling power converters to operate at higher switching frequencies. The question of whether it's the semiconductor or the magnetic losses that are predominant in a particular power-supply design is really a matter of that design's topology.

*Donelson C Lawry
Alexandria, VA*

Macros improve PLD design

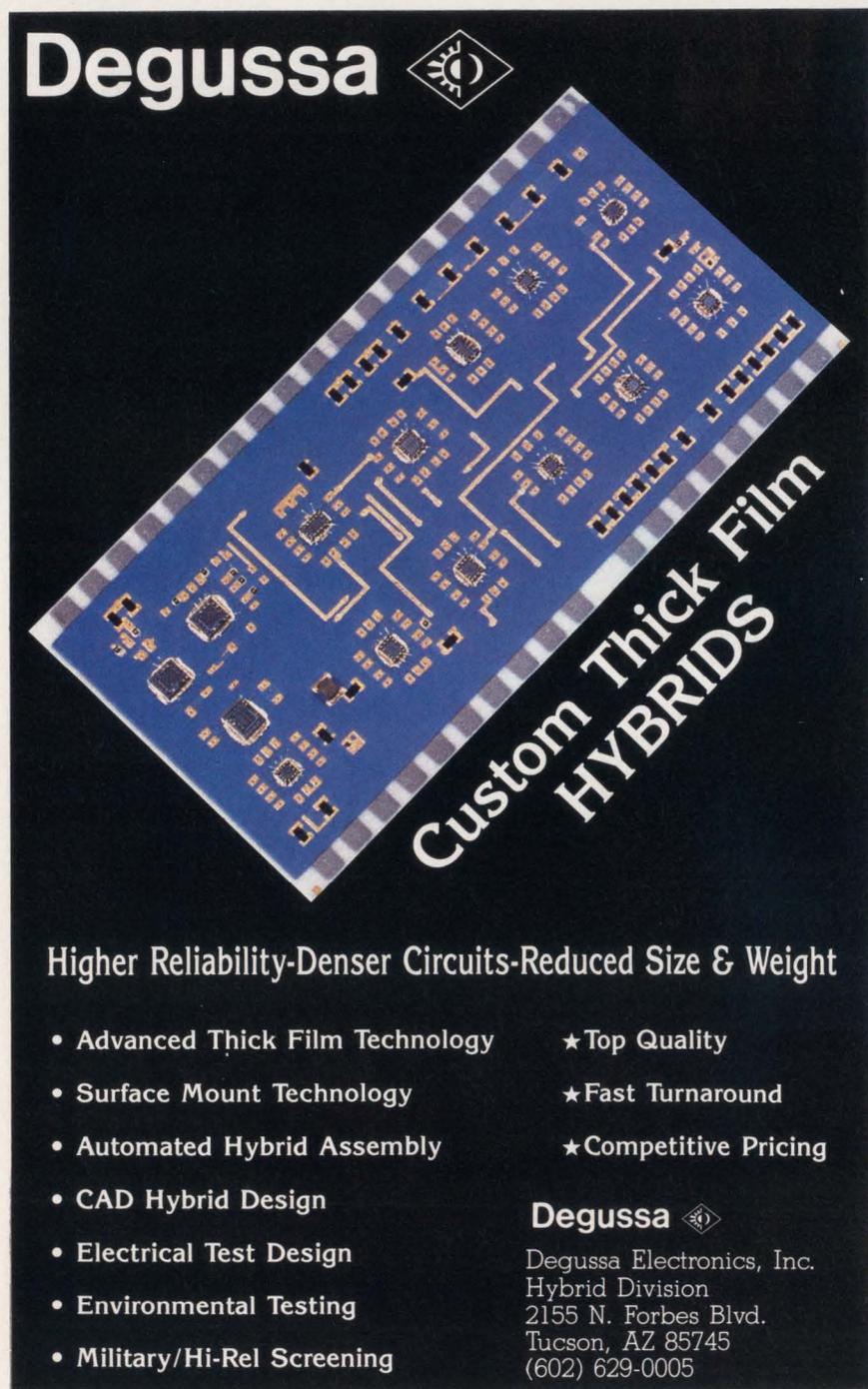
I'd like to comment on Charles H Small's observations in his Special Report on programmable-logic devices (EDN, February 5, pg 112) about the use of Altera's macros for improved PLD design productivity. I am concerned that the tone of his statements (on pgs 120 and 122) will raise concerns in potential customers regarding the integrity of the product.

I agree that when an engineer is designing at the basic programming-element, or fuse-map, level, extracting the maximum performance from a PLD does require intimate knowledge of the device itself. That is exactly why we offer the tools Mr Small described. We do that part of the work now. By using these predesigned, high-level functions, the engineer does not have to involve himself at the detailed device level. His efforts can be focused, more usefully, on solving his unique system-design problems.

*David A Laws
Altera Corp
Santa Clara, CA*

(Ed Note: It was not the purpose of the article to impugn the integrity of Altera's tools; instead, we think that TTL-to-PLD compilers are interim tools that engineers will use until they become more familiar with PLD design. The history of technology shows many instances in which older design techniques are temporarily adapted to a new technology. For example, when transistors first appeared, many technical articles

*Text continued on pg 42
EDN June 25, 1987*



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CIRCLE NO 21

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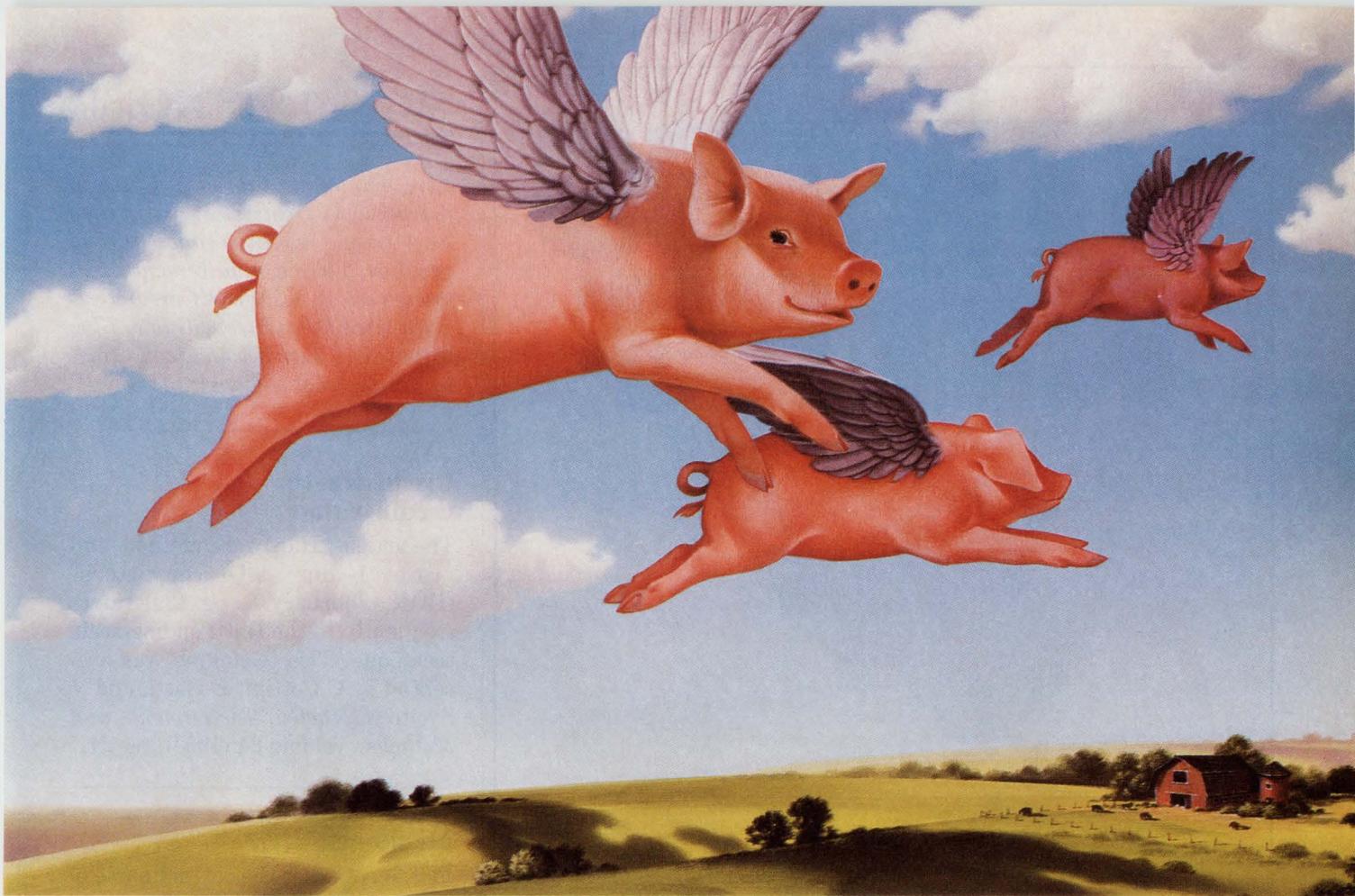
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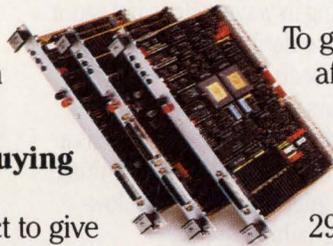
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MVME104	Same as MVME105, but with I/O channel interface	\$1,295
MVME106	Same as MVME105, but with 5 1/4-in. floppy interface	\$1,295
MVME107	Same as MVME105, but with SCSI bus interface	\$1,295
MVME133A	VMEbus SBC; 20-MHz MC68020 CPU; 20-MHz MC68881 FPU; 1 Mb shared DRAM; up to 512Kb EPROM; RS-232-C serial port; RS-485/RS-422 serial port; three 8-bit timers; real-time clock; system controller	\$3,585
MVME134	Same as MVME133A, but with 16-MHz MC68020 CPU and MC68851 PMMU (instead of MC68881 FPU), plus 4 Mb of shared DRAM	\$2,995

*Call for OEM discount schedule on volume orders.

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SIGNALS & NOISE

were printed that described how to design with transistors as if they were triode vacuum tubes having peculiar biasing requirements. Although we at EDN can't predict exactly what the future will look like, we're fairly sure it won't look exactly like the past.—Charles H Small)

Credit where credit is due

The article "Hardware methods improve 1-chip A/D converters" (EDN, February 5, pg 139) refers frequently to the Gatti sliding-scale technique. This technique was presented by C Cottini, E Gatti, and V Svelto in *Nuclear Instruments and Methods*, Volume 24 (1963), pg 241.

Misnomer

Please note that the correct name of the GaAs logic IC family discussed in the New Products section of EDN's March 4 issue (pg 197) is NEC UPG700. The products are manufactured by NEC and sold in the US by California Eastern Laboratories (Santa Clara, CA).

YOUR TURN

EDN's Signals and Noise column provides a forum for readers to express their opinions on issues raised in the magazine's articles or on any topic that affects the engineering industry. Send your letters to the Signals and Noise Editor, 275 Washington St., Newton, MA 02158. We welcome all comments, pro or con. All letters must be signed, but we will withhold your name upon request. We reserve the right to edit letters for space and clarity.

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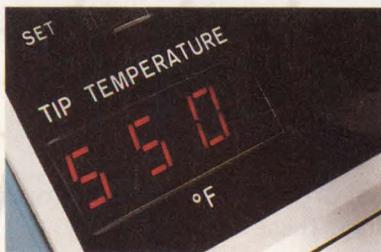
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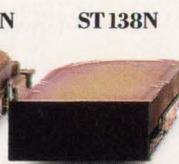
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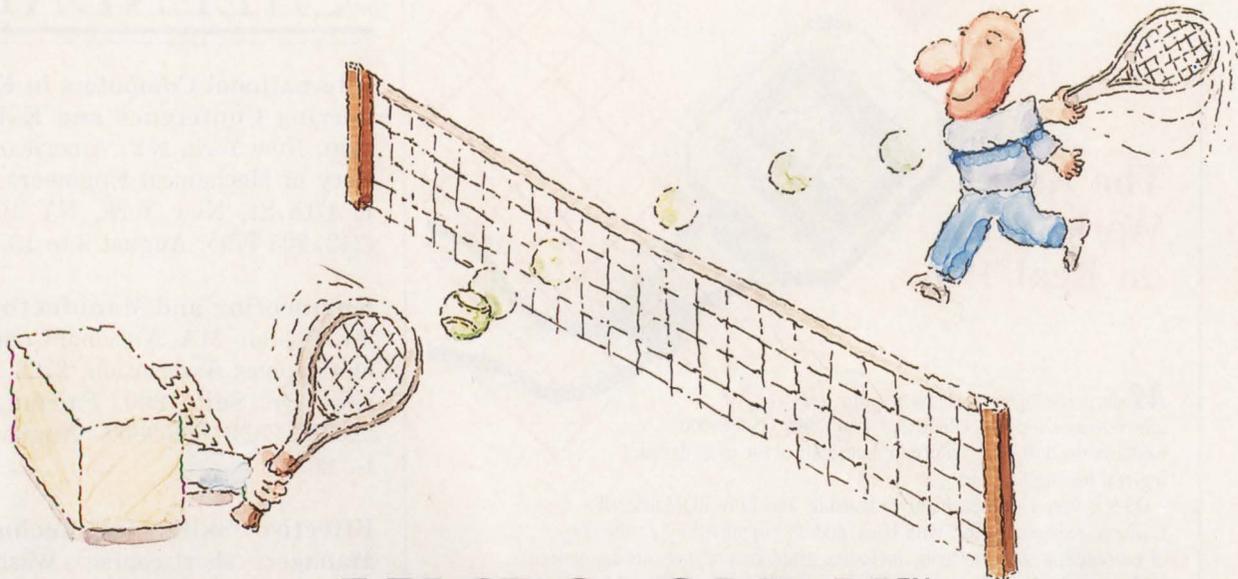
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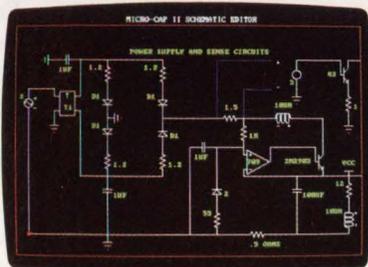


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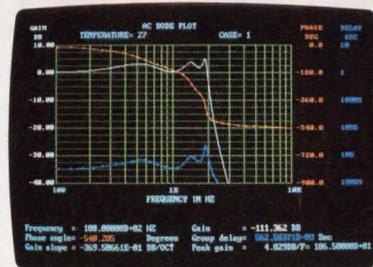
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International Computers in Engineering Conference and Exhibition, New York, NY. American Society of Mechanical Engineers, 345 E 47th St, New York, NY 10017. (212) 705-7795. August 9 to 13.

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Effective Skills for Technical Managers (short course), Washington, DC. Integrated Computer Systems, Box 3614, Culver City, CA 90231. (800) 421-8166; in CA, (213) 417-8888. September 1 to 4.

Modern Electronic Packaging, Seattle, WA. Technology Seminars, Box 487, Lutherville, MD 21093. (301) 269-4102. September 9 to 11.

PC Fab Expo, Minneapolis, MN. PMS Industries, 1790 Hembree Rd, Alpharetta, GA 30201. (404) 475-1818. September 15 to 17.

Effective Skills for Technical Managers (short course), Los Angeles, CA. Integrated Computer Systems, Box 3614, Culver City, CA 90231. (800) 421-8166; in CA, (213) 417-8888. September 15 to 18.

Invitational Computer Conference Computer Graphics Series, Fort Lauderdale, FL. BJ Johnson and Associates, 3151 Airway Ave, #C-2, Costa Mesa, CA 92626. (714) 957-0171. September 17.

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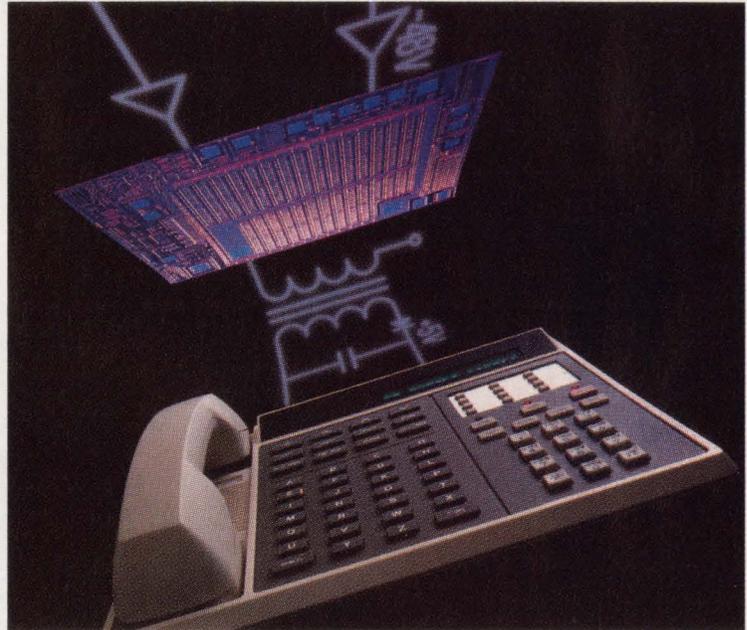


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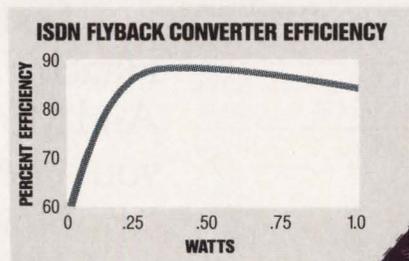
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VT20C50	1K x 4	Separate I/O; FC	15 ns
VT20C68	4K x 4	APD	20 ns
VT20C69	4K x 4	12 ns CS	20 ns
VT20C71	4K x 4	Separate I/O; OT	20 ns
VT20C72	4K x 4	Separate I/O; HZ	20 ns
VT20C78	4K x 4	APD; 10 ns OE	20 ns
VT20C79	4K x 4	12 ns CS; 10 ns OE	20 ns
VT20C98	8K x 8	APD	25 ns
VT20C99	8K x 8	Fast CE	25 ns
VT62KS4	16K x 4	15 ns CS	25 ns
VT63KS4	16K x 4	15 ns CS; OE	25 ns
VT64KS4	16K x 4	APD	25 ns
VT65KS4	16K x 4	APD; OE	25 ns

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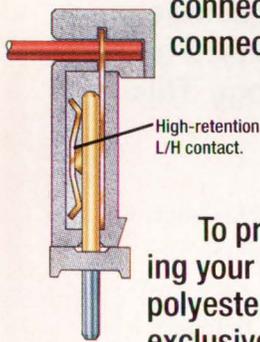
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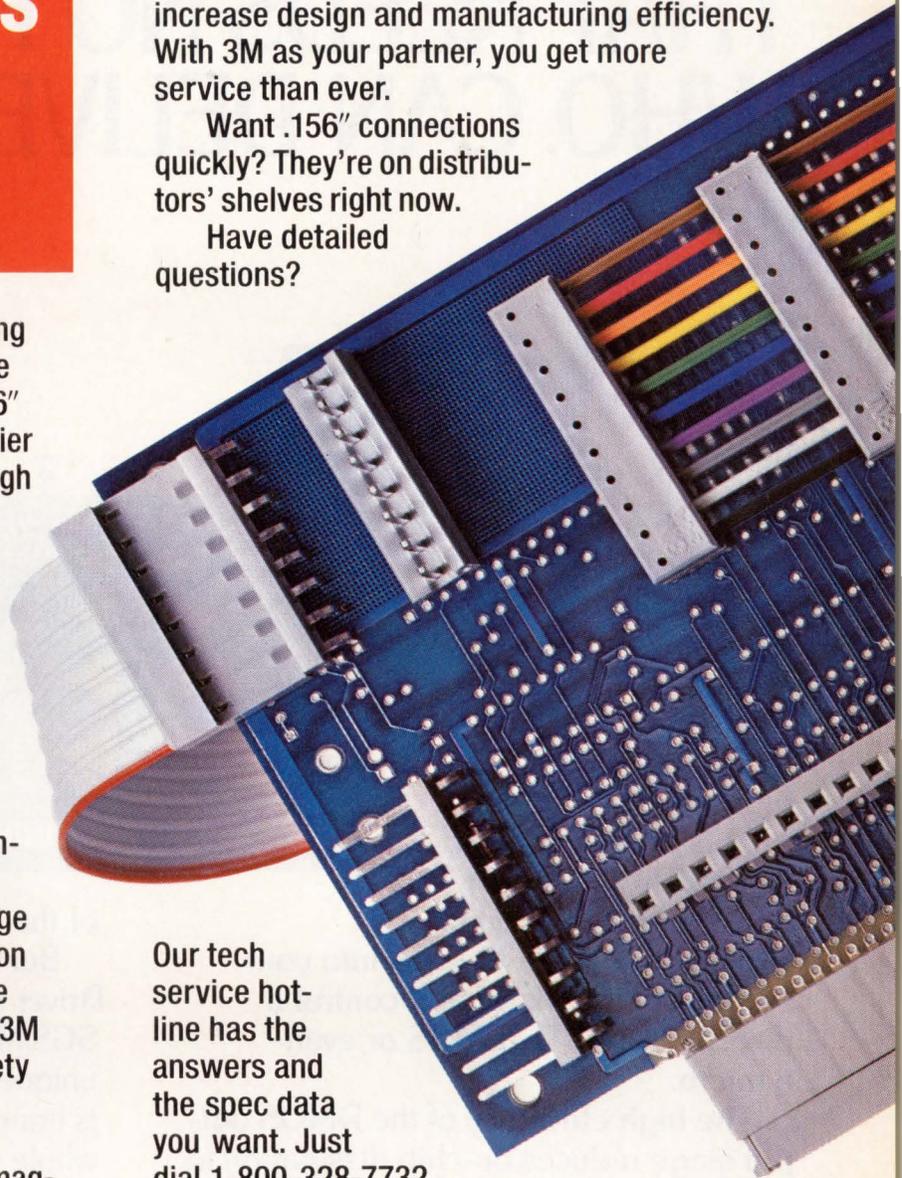
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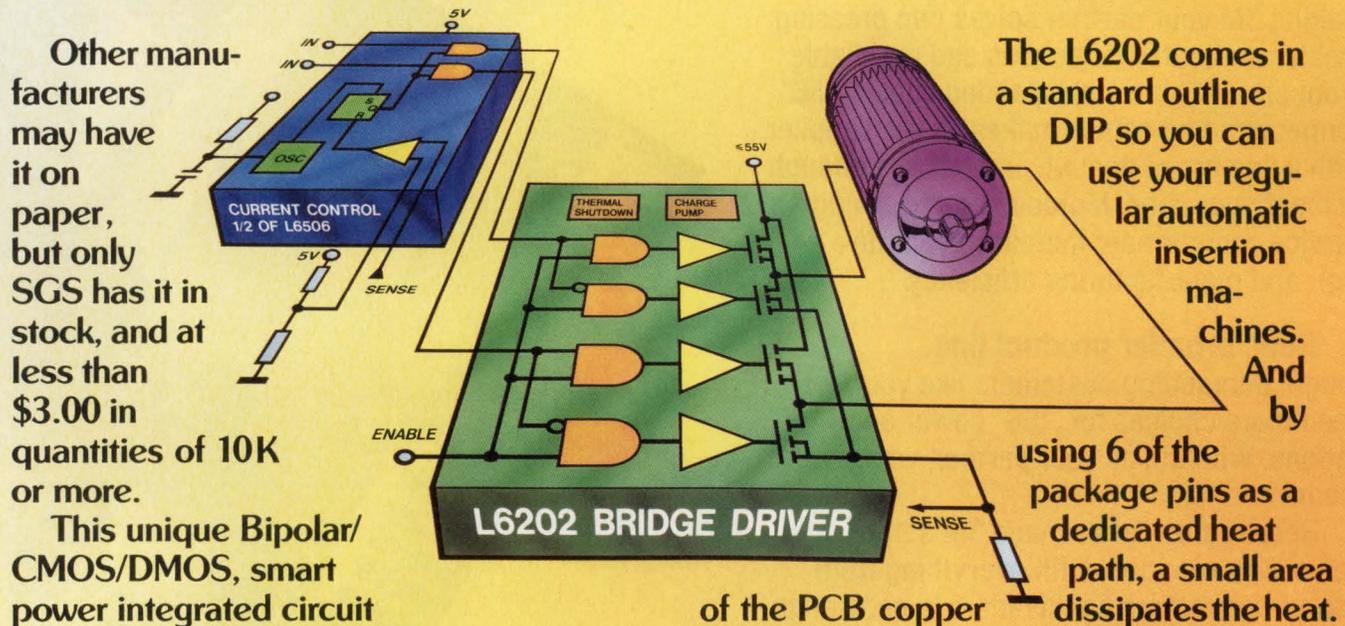
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EDITORIAL

Loosen export restrictions



Although many people clamor for increases in competition and export sales, the US government continues to burden us with unreasonable export restrictions. Such restrictions are aimed at depriving the Soviet Union of the Western world's high technology. However, today's restrictions appear inconsistent and capriciously applied. They gain us little added national security, and they choke exports. For example, you need an export license to ship US-made 16k-bit dynamic RAMs to Japan. As long as we apply such thoughtless restrictions, buyers won't shop in the US. Perhaps that's the result we should expect for an export program that's jointly administered by the Department of Defense and the Department of Commerce, whose goals are often at odds.

Export regulations can also be inconsistent. A small company I worked for sold an inexpensive μ P editor-assembler program and a debugger. The Commerce Department told us we'd need a license to send the software—paper tape and PROMs—to Eastern Europe. For inexpensive software it wasn't worth the effort. However, there were no restrictions on selling technical books overseas. Two such books contain complete listings for the programs. Anyone patient enough to type in 5k bytes of hexadecimal code could have the software almost for free.

Trade restrictions affect more than just a few high-tech products. The National Academy of Sciences estimates that export restrictions cost the US almost \$9 billion in trade and as many as 200,000 jobs each year. However, despite the lost jobs and trade, the policy has yielded few national-security gains.

High-tech items that embody sensitive technology will continue to require special regulations. But we can increase exports immediately by dropping export restrictions on formerly high-tech products that are now commodities—those that sell on price rather than on technology. If overseas buyers want our PC clones, dynamic RAMs, and disk drives, let's do business—cash on delivery.

Jon Titus
Editor

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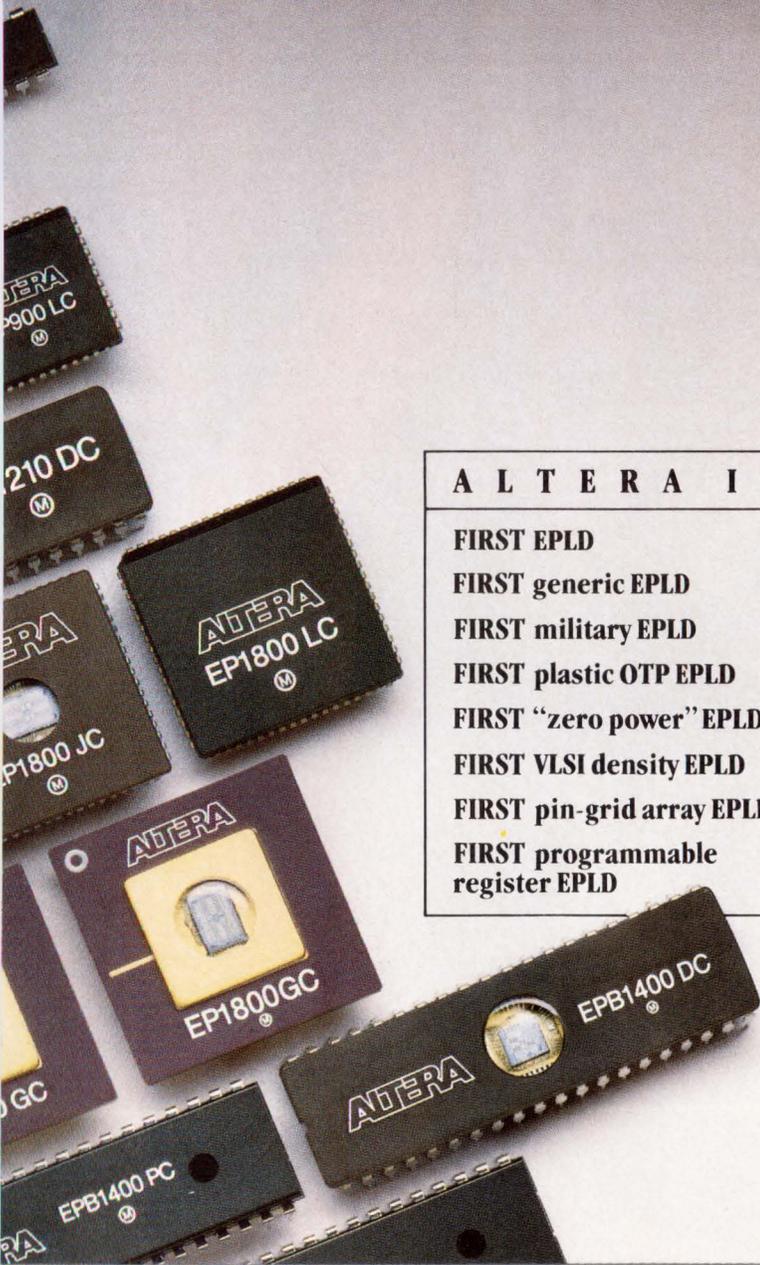


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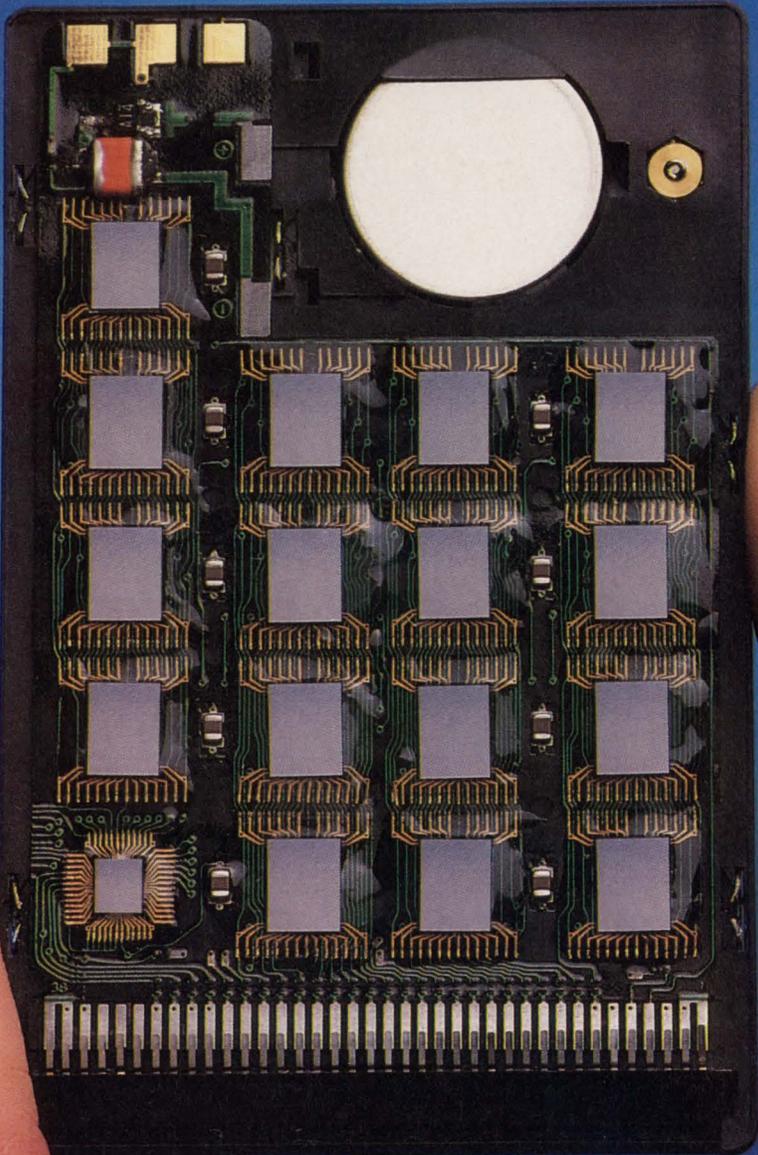
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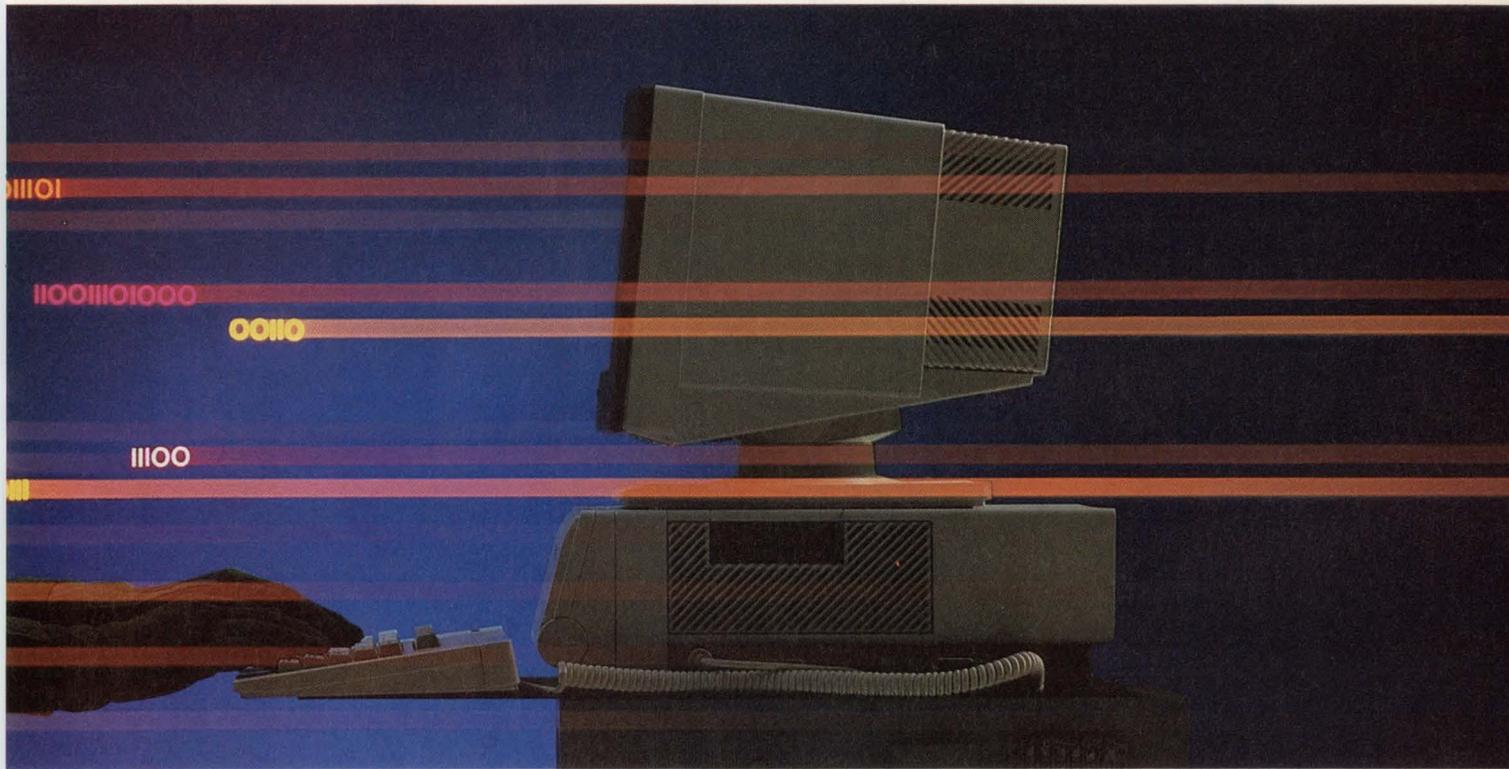
Built-in decision tree: Enter the board information in straightforward database format. Add stimulus routines. The 9100A then produces comprehensive test programs for Guided Fault Isolation (GFI) almost automatically. A special fault-tracing algorithm makes all the choices about the troubleshooting sequence.

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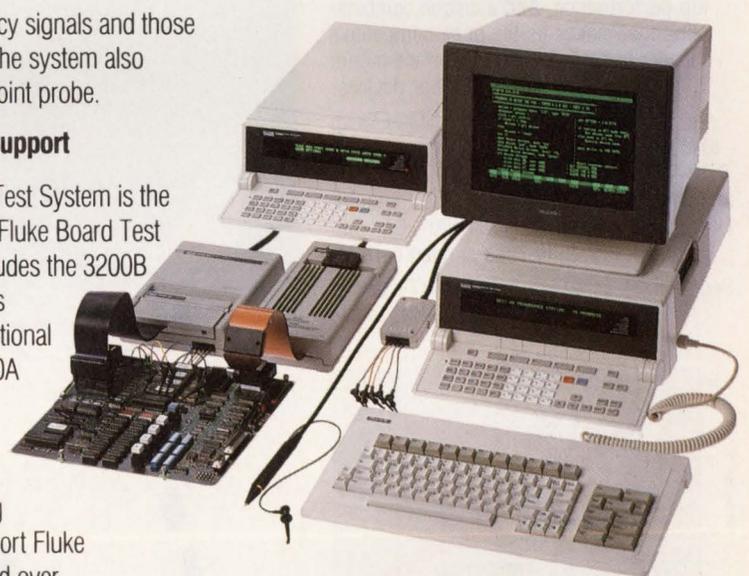
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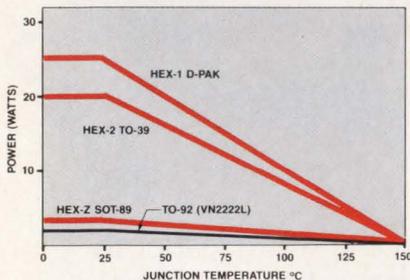
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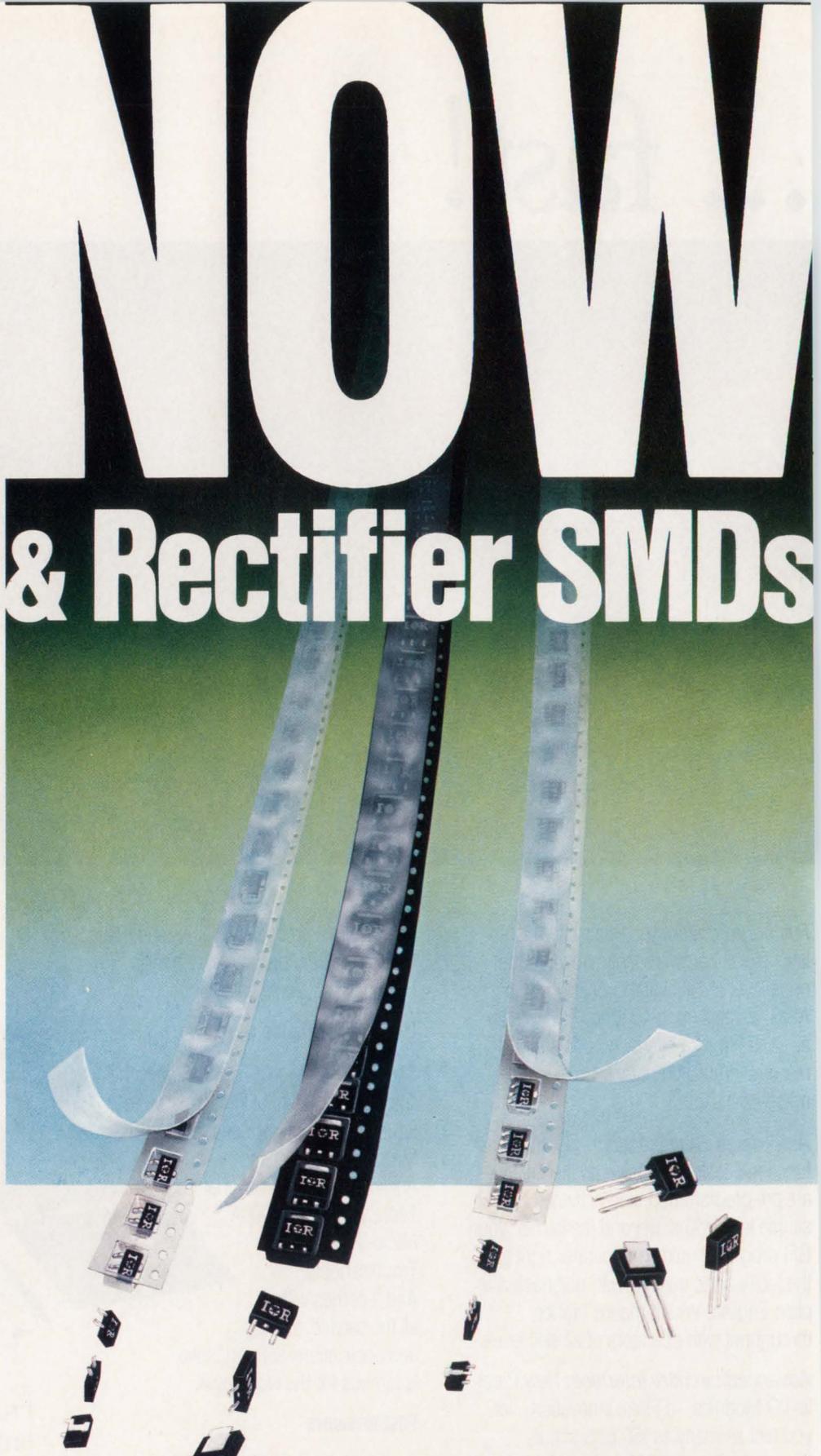
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TECHNOLOGY UPDATE

PC add-in boards rev up graphics engines with hardware and software enhancements

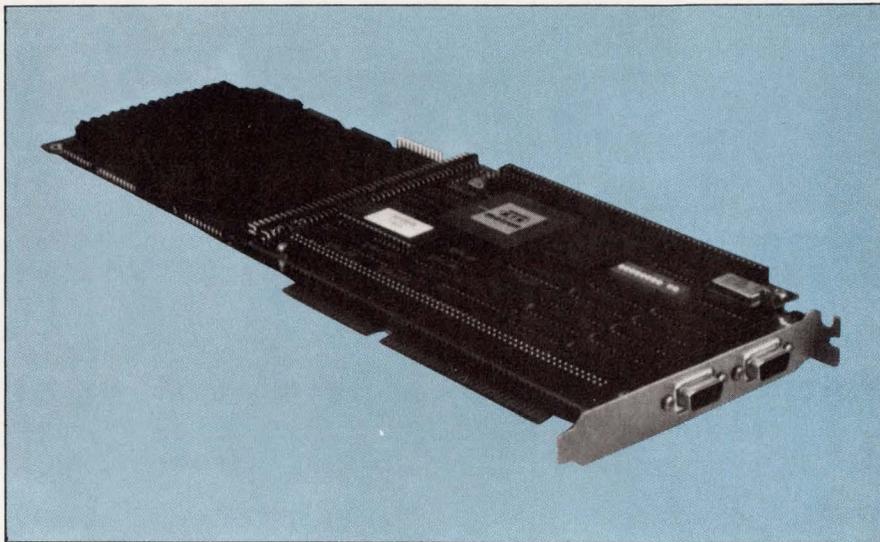
Margery S Conner,
Regional Editor

The latest add-in graphics boards for the IBM PC and PC/AT bus incorporate graphics engines, which give them faster response time and greater color and pixel resolution than the IBM Enhanced Graphics Adapter (EGA), often at a surprisingly low price. The EGA, which is currently the standard graphics add-in board for the IBM PC family, is nonintelligent; it provides 640×350-pixel resolution and 16 colors. Boards with graphics engines, however, can provide resolutions of as many as 2048×1536 pixels and 256 colors. All of the recently released boards incorporate either the Intel 82786 or the Texas Instruments TMS34010. However, you'll find that several manufacturers have added software and hardware enhancements that further increase their boards' capabilities.

The two chips each have their own strengths (see the Special Report on graphics engines, EDN, March 4, pg 112). In general, boards based on the 34010 are aimed at general-purpose applications, because the chip's programmability and resulting flexibility make it suitable for a wide variety of uses. On the other hand, boards based on the 82786 tend to target specialized applications that take advantage of the chip's fast hardware-windowing or dynamic-RAM-control capabilities.

Best of both worlds

In its Pepper SGT graphics board, Number Nine Computers took a novel approach to balancing the tradeoffs between software flexibility and hardware windowing speed: The board has both a 34010, which serves as the general-purpose



In its PG-1281 intelligent graphics add-in board, Matrox accelerated some of the 34010 μ P's commonly used graphics software routines by implementing them in ASICs. The company then took advantage of this proprietary hardware by developing its own software library.

graphics processor, and an 82786, which handles the windowing functions and dynamic-RAM control. At \$995, the board is competitive with models that have only one graphics processor.

"We felt that the two chips were so complementary in functionality that they were ideal in a single-board package," says William Frentz, vice president of marketing for Number Nine. "Because the Intel chip is an advanced display controller and the TI chip is a 32-bit μ P that's tailored for graphics, they're not really doing the same things—there's a slight overlap, but you get a different set of utilities out of each chip."

The board's multiport display memory permits asynchronous accesses by the 34010, the 82786, and the host μ P (Fig 1). The board can also map display memory to any part of the host μ P's memory: As much as 16k bytes at a time can be switched into a 64k-byte bounded area in host memory. This method

allows a system operating under MS-DOS, which has a 640k-byte memory limit, to access a display memory in excess of that limit. NNIO, the company's proprietary, EPROM-resident software interface, controls the three processors' access to the memory. NNIO also boosts the board's efficiency by selecting from the three processors the one best suited for a particular task.

The 82786 serves as the display-memory controller for the board, as well as controlling hardware windowing.

You can access the 32-bit 34010 processor through NNIO, or you can program it directly. NNIO contains the manufacturer's version of graphics routines for the chip; you can also write your own routines.

Optimized for MS Windows

Like Number Nine, Renaissance GRX has developed extensive proprietary software for its board. The



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software optimizes the company's Rendition board for Microsoft's MS Windows operating environment. Despite its wide acceptance by application-software writers, who eagerly await the emergence of a standard window environment, MS Windows has yet to gain wide acceptance by users, because without intelligent graphics hardware, the environment's response time is sluggish and its windowing capabilities are limited. (For more information on proposed graphics interface standards, see EDN's July 9 issue.)

Because intelligent graphics boards like Rendition can speed the response of software windowing environments, MS Windows' time may finally have come. Further, it will be easy to upgrade software applications written for the Windows environment to IBM's new operating system, OS/2. This fact may serve to increase its attraction for application-software writers. (For information on how IBM's new PS/2 may affect add-in graphics boards, see **box**, "Add-in graphics cards for the IBM PS/2".)

In a system with a nonintelligent graphics board, such as IBM's enhanced graphics adapter (EGA), the host μ P communicates through Windows by firing a string of

graphics commands (also called a display list) to the graphics adapter. The host μ P then waits for the adapter to acknowledge that the entire list has been accepted. The 34010-based Rendition board uses a dual-ported RAM buffer to hold the display list. At the same time that the host μ P fills the RAM from one end, the Rendition removes the commands from the buffer's other end. Renaissance has also written its own MS Windows driver for the board.

According to Renaissance, MS Windows runs 20 times faster on the Rendition board than on the IBM EGA. Applications can run 100 times faster by writing directly to RGDI, the board's software interface. RGDI contains entry points for TI's graphics-software library routines. (An example of a graphics subroutine is a software program that draws a graphics primitive, such as a line.) Renaissance has also written its own graphics routines, which it claims are faster than TI's. Most of TI's graphics routines are in C; Renaissance's routines are in assembly language. The company suggests a retail price of \$1195 for the board, but anticipates selling it for \$535 in OEM quantities.

The major reason that these man-

ufacturers are taking pains to add enhancements to their boards is that they're wary of getting involved with another commodity product like the EGA board: Because all the EGA clones are based on the same chip sets, they're differentiable only by price. By adding value in hardware or software or both, manufacturers can avoid making the same mistake with their intelligent graphics add-ins. Matrox, for instance, realized that merely placing a graphics processor on the bus and reselling TI's software would not differentiate its board from other basic intelligent-graphics-card models. In its PG-1281 graphics board, Matrox saw an opportunity to accelerate some of the 34010's commonly used graphics software routines by implementing them in application-specific ICs (ASICs). Then, to take advantage of this proprietary hardware, the company developed its own software library.

The PG-1281 includes an ASIC that accelerates raster operations; the chip also supervises host-to-graphics-processor communications; hard-wired vector generation; and hard-wired pan, scroll, and zoom capabilities. The implementation of the vector generation alone makes

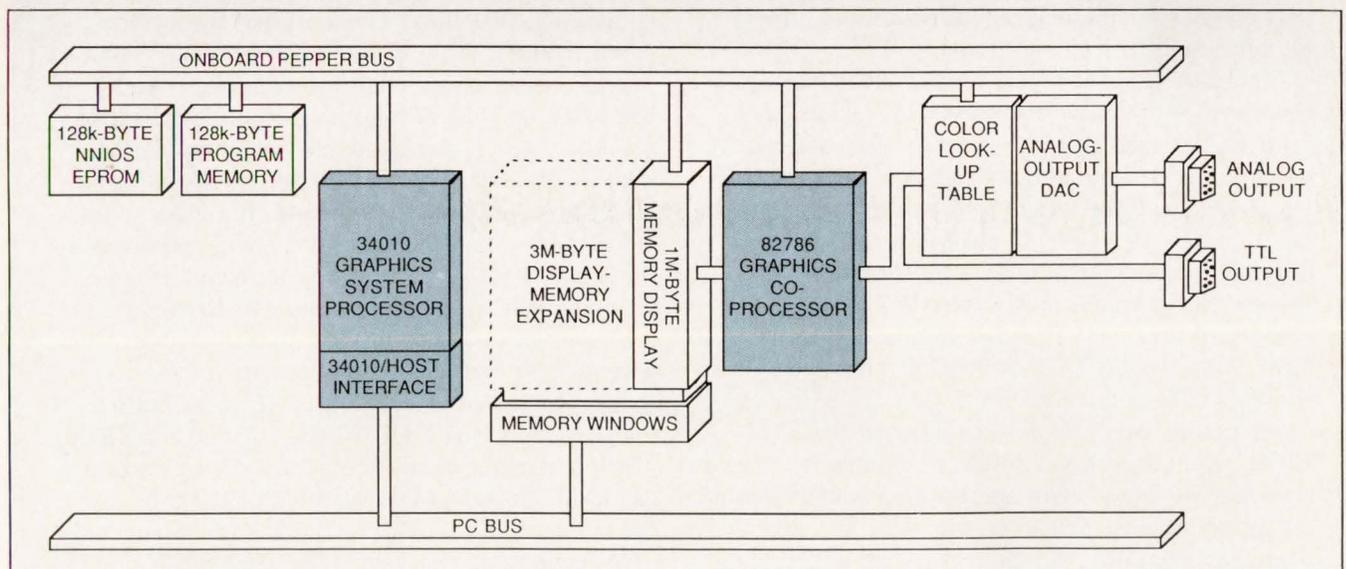


Fig 1—Combining the TI TMS34010 and the Intel 82786, the \$995 Pepper SGT board from Number Nine Computers uses the firm's proprietary software interface, NNIOS, to control communications among the two graphics engines, the host μ P, and memory.

TECHNOLOGY UPDATE

for a fourfold increase in speed over a standard 34010 implementation, according to the company.

An onion-like software shell

To support the custom hardware surrounding the 34010, Matrox surrounds the 34010 and its ASICs with a library of onion-like layers of C-callable routines. The library comprises more than 300 graphics routines and consists of four layers. The outermost and most abstract is the 3-D layer, which contains modeling transformations for 3-dimensional space. Below this layer is the 2-D

layer, followed by the screen layer, which generates all screen shapes. The screen layer transfers the shape parameters to the kernel layer, which is a direct interface to the display hardware.

If you call library routines from the 3-D layer, which is the most abstract and hardware-independent layer, the 3-D layer uses routines from the 2-D, screen, and kernel layers. If, however, you choose to write directly to the hardware, you call routines from the kernel layer.

The layers' routines operate under one of three command shells.

The PGM shell supports IBM's Professional Graphics Adapter (PGA) commands as well as Matrox commands used by other boards. The library shell provides a command interpreter that permits access to library routines. The custom shell gives you the option of writing a custom command interpreter that calls the graphics subroutines, so you can develop your own algorithms for the 34010.

Graphics add-in boards that use the Intel 82786 offer a different set of capabilities than those of the 34010-based boards. The 82786's

Add-in graphics cards for the IBM PS/2

For its Personal System/2, IBM has introduced two graphics-enhancement boards, one standard and one optional. If the PS/2 catches on, the boards will certainly become standard. The basic graphics-enhancement board for the PS/2 is the video graphics array (VGA), which, like the EGA, is nonintelligent. The high-performance board is the 8514/A display adapter, an intelligent add-in. Both boards use custom components.

The VGA, which will be the PS/2's standard graphics hardware, is essentially an EGA with either higher resolution (640×480 pixels and 4 bits/pixel) or more colors (320×200 pixels and 8 bits/pixel). Like the EGA, the VGA has no processing capability but relies on the host processor for display-memory manipulation. Its relatively simple circuitry will fit into a gate array.

For EGA chip-set manufacturers like Paradise Systems (South San Francisco, CA), cloning the IBM EGA board and its software was relatively easy—all of its components were discrete parts, and IBM made the adapter's BIOS extensions public. To make its VGA and 8514/A boards more difficult to clone, IBM is apparently not going to release the graphics hardware's BIOS.

Despite that fact, Paradise announced that it will have samples of a VGA-compatible chip set by this summer. The company admits that the software development won't be as easy as with the EGA BIOS, when a group of software engineers could go through the actual code and develop a specification for all possible responses of the code. Working only from the spec, programmers who had never seen the original code could develop a BIOS that per-

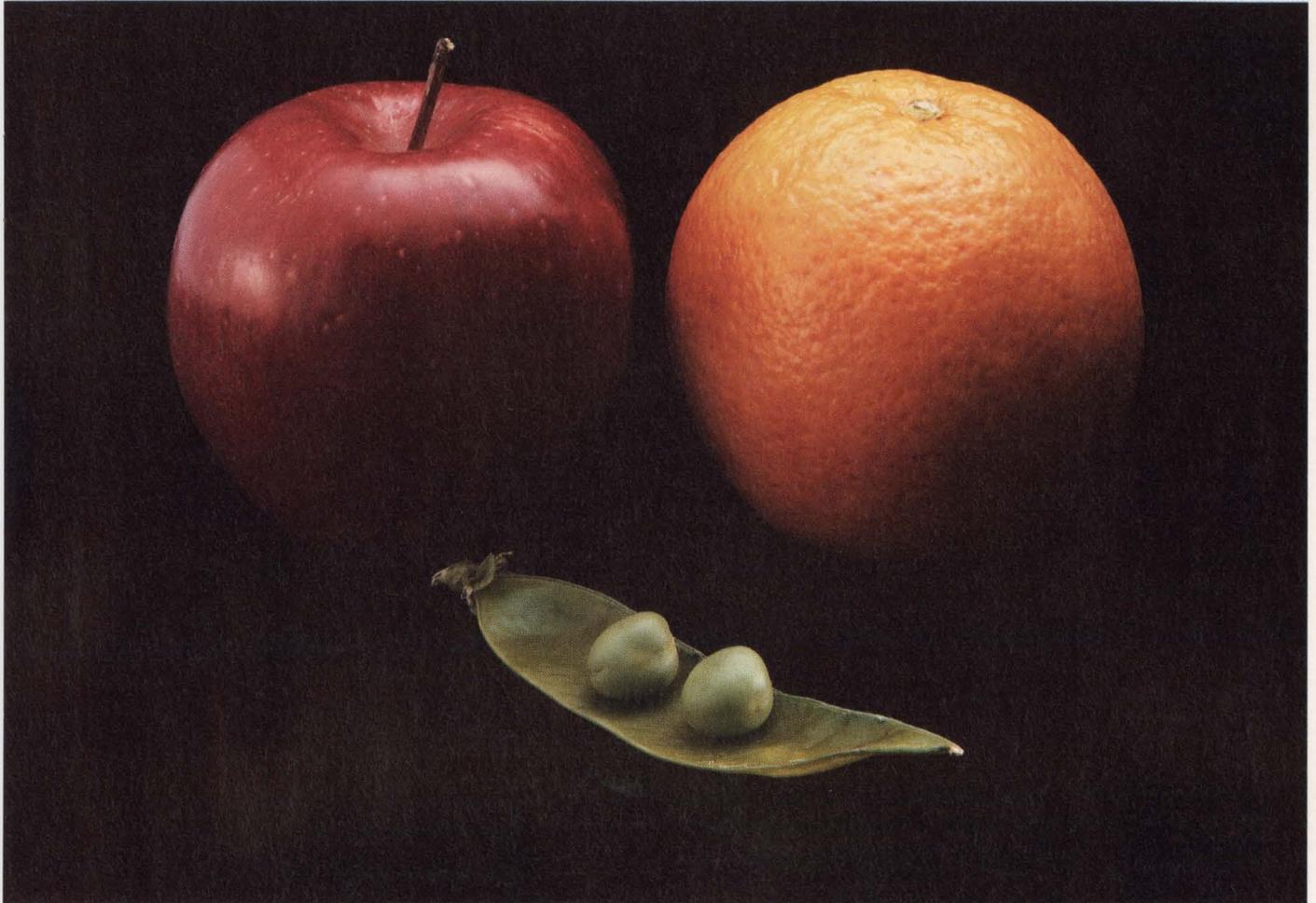
formed exactly as IBM's did, but had different coding. Developing the new BIOS without the original code will take a major effort in reverse engineering.

Paradise didn't wait for the announcement of the PS/2 to start developing its ASIC design. Six months before the announcement, the company's design engineers speculated about how IBM would implement its new graphics board. The engineers decided on the characteristics they thought were a given and left open the hazier sections until after IBM's announcement. They claim that this head start will allow them to have samples in 90 days instead of a year.

Emulating the IBM's 8514/A, the graphics-display option that takes advantage of the PS/2's microchannel, will require different technology. The 8514/A is capable of 1024×768 pixels and 4 bits/pixel (or 1024×768 pixels and 8 bits/pixel) of resolution and has some processing capabilities, such as line drawing and BitBlts, so it will probably be too complex to implement in a gate array.

Further, emulating the 8514/A will require a clone-maker either to invest in its own hardware version of the graphics processor or to mimic the processor's functions with a graphics engine. This development has Texas Instruments licking its chops over the prospect that companies that attempt to clone the IBM 8514/A will use the 34010, which is a prime candidate because it's programmable. It's reasonable to speculate that a board combining both the 34010 graphics processor and a VGA-compatible chip would far exceed the capabilities of IBM's own board.

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resolution is normally limited to 640×480 pixels and 8 bits/pixel for a noninterlaced color (or shades-of-gray) display. The UDC-800 board from Univision overcomes this limitation by using proprietary glue logic around the graphics processor to enhance the chip's addressing capability and increase the resolution to 2048×1536 pixels and 8 bits/pixel.

The board has a video-RAM-based, 3M-byte frame buffer, and it uses dynamic RAMs for the 500k-byte display-list memory, which is expandable to 1M byte. (The frame buffer is the memory that stores the screen's pixel information; the display-list memory contains the commands that drive the graphics engine.) Note, however, that the 82786 can perform hardware windowing only on 1-bit-deep pixels, and the UDC-800 makes use of 8-bit-deep pixels, so the board can't perform hardware windowing. To support its windowing functions, the board uses BitBlts, which are software bit-block transfers from off-screen memory to display memory.

Because of its high resolution, the UDC-800 must support video-display rates of 200 MHz. The video-display section, including the color look-up table, is implemented in discrete ECL. Although its resolution is sufficient to support 256 different

Expect longevity for PC add-in cards

You may wonder what effect IBM's announcement of the Personal System/2 will have on the market for add-in boards for the PC and PC/AT bus. Tom Van Overbeek, who was vice president of marketing at Morrow Computers (he now holds that position at Paradise Systems), thinks a parallel may exist between IBM PC/XTs and PC/ATs and the path of the machine they eventually replaced, CP/M-based S-100 systems.

Morrow Computers, now defunct, was at one time the largest shipper of desktop CP/M systems. When IBM announced the PC in 1981, the public perceived that the PC was clearly superior to the CP/M-based systems in many ways. The PC immediately became popular; even so, the fourth quarter of 1983 was the biggest sales period in Morrow's history. The CP/M machines continued to flourish for several years after the announcement of the IBM PC.

Just as it took a while for the PC to catch on, Van Overbeek suspects, it will take a while for PS/2 hardware and software to become dominant. He cites three reasons for his projection. First, it will be some time before adequate interface support for PS/2 hardware peripherals is available. Further, the established base of IBM PCs, PC/XTs, PC/ATs, and compatibles is 15 to 20 million. And finally, before they'll buy the PS/2, people will have to see a fairly extensive base of software support for the OS/2. This last reason may be the strongest of all: After all, you buy a record player to listen to records, not just to look at a slick new machine.

colors, the UDC-800 is currently configured only for shades of gray, because monitors that support this display and color resolution are at present prohibitively expensive.

The Vista VCS-2000 3-board set exploits the dynamic-RAM-control

capabilities of the 82786. The set comprises a graphics board with 1728×2200-pixel monochrome resolution and two data-compression/decompression boards that speed the image processing of digitized documents or drawings. One application

For more information . . .

For more information on the graphics boards discussed in this article or listed in the accompanying table, contact the following manufacturers directly or circle the appropriate numbers on the Information Retrieval Service card.

Emulex Corp
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(714) 662-5600
TWX 910-595-2521
Circle No 734

International Software Corp
528 Commons Dr
Golden, CO 80401
(303) 526-0388
Circle No 735

Matrox Electronic Systems Ltd
1055 St Regis Blvd
Dorval, Quebec H9P 2T4, Canada
TLX 05822798
Circle No 736

National Design Inc
12885 Research Blvd
Suite 105
Austin, TX 78750
(512) 335-1550
Circle No 737

Number Nine Computer Corp
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(617) 492-0999
TLX 3717799
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Renaissance GRX Inc
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Bellevue, WA 98004
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Tektronix Inc
Information Display Group
Box 1000
Wilsonville, OR 97070
(503) 235-7202
Circle No 740

Univision Technologies Inc
12 Cambridge St
Burlington, MA 01803
(617) 273-5388
TLX 988755
Circle No 741

Vectrix Corp
2606 Branchwood Dr
Greensboro, NC 27408
(919) 288-0520
TLX 574417
Circle No 742

Vermont Microsystems Inc
11 Tigan St
Winooski, VT 05404
(802) 655-2860
TWX 510-600-1184
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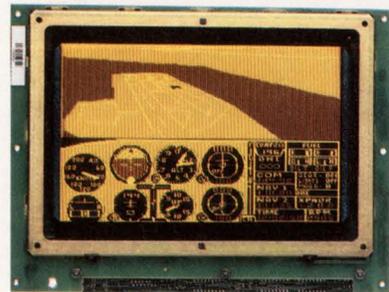
Verticom Inc
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Sunnyvale, CA 94089
(408) 747-1222
TLX 754044
Circle No 744

Vista Computer Systems Inc
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for the system is in document imaging systems. The display memory can hold the equivalent of as many as eight 8½×11-in. digitized draw-

ings or documents. The standard board has 2M bytes of display memory; you can expand the memory to a maximum of 8M bytes.

The 82786's dynamic-RAM-control capabilities were the deciding factor in Vista's choice of a graphics engine because the company wanted

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MANUFACTURER	MODEL	GRAPHICS ENGINE	ONBOARD MEMORY (BYTES)	RESOLUTION (BITS)	BUS	INTERFACE SUPPORT	PRICE AND COMMENTS
EMULEX	INTELLIGENT GRAPHICS CONTROLLER	34010	512k TO 4M	640×480×4, 960×720×4, 1024×768×4, 1024×1024×8, 1280×1024×8	PC/XT OR PC/AT	C, D, W	\$1499 TO \$2499; PRICE DEPENDS ON RESOLUTION
INTERNATIONAL SOFTWARE	VIEWMATE	82786	2M TO 5M	1240×950×1	PC/XT OR PC/AT	W	\$5400
MATROX	PG-1281	34010	512k TO 1.5M	1280×1024×4, 1280×1024×8	PC/XT OR PC/AT	C, CGI, E, G, M, P	\$3495; EGA IS OPTIONAL
NATIONAL DESIGN	GENESIS 1024	34010	512k TO 1.5M	1024×800×4	PC/XT OR PC/AT	CGI, D, W	\$1700; FOR 1.5M- BYTE MEMORY, ADD \$600
NUMBER NINE	PEPPER SGT	34010 AND 82786	1M TO 4M	1280×480×4, 640×480×8, 800×600×4, 1280×350×1	PC/XT OR PC/AT	C, CGI, E, G, H, N	\$995; EGA IS OPTIONAL
	PEPPER PRO 1280	34010	1M TO 8M	1280×1024×8	PC/AT OR RT PC	C, CGI, E, G, H, N, P	\$2995
RENAISSANCE GRX	RENDITION I	34010	512k	640×480×4, 1024×768×1	PC/XT OR PC/AT	C, CGI, E	\$1195
TEKTRONIX	PLOT 10 PC4100	34010	1M	640×480×8	PC/XT OR PC/AT	C, E, T	\$1800; FOR TERMINAL EMU- LATION, ADD \$995
UNIVISION	UDC-800	82786	3M	1024×1024×8, 1280×1024×8, 1024×1280×8, 1536×1280×8, 2048×1536×8	PC/AT	W	\$3495 TO \$6995; PRICE DEPENDS ON RESOLUTION
VECTRIX	PRESTO	34010	512k	1280×1024×4, 1280×1024×8, 1024×1024×4, 1024×1024×8, 1024×768×4, 1024×768×8	PC/XT OR PC/AT	C, D	\$1950 TO \$2650; PRICE DEPENDS ON RESOLUTION
VERMONT MICRO SYSTEMS	PAGEMANAGER 100	82786	512k	1024×1024×1	PC/XT, PC/AT, OR RT PC	C, G, W	\$2495
	IMAGE MANAGER 640	34010	512k	640×480×8	PC/XT, PC/AT, OR RT PC	C, W	\$1695
VERTICOM	DESKTOP 1280	82786	512k	1280×960×1	PC/XT OR PC/AT	C, E, G, P, W	\$1295
VISTA	VCS-2000	82786	1M TO 8M	1728×2200×1	PC/AT	W	\$3400 TO \$5000; PRICE DEPENDS ON MEMORY SIZE AND IN- CLUDES DATA COMPRES- SION/DECOM- PRESSION CAPABILITY

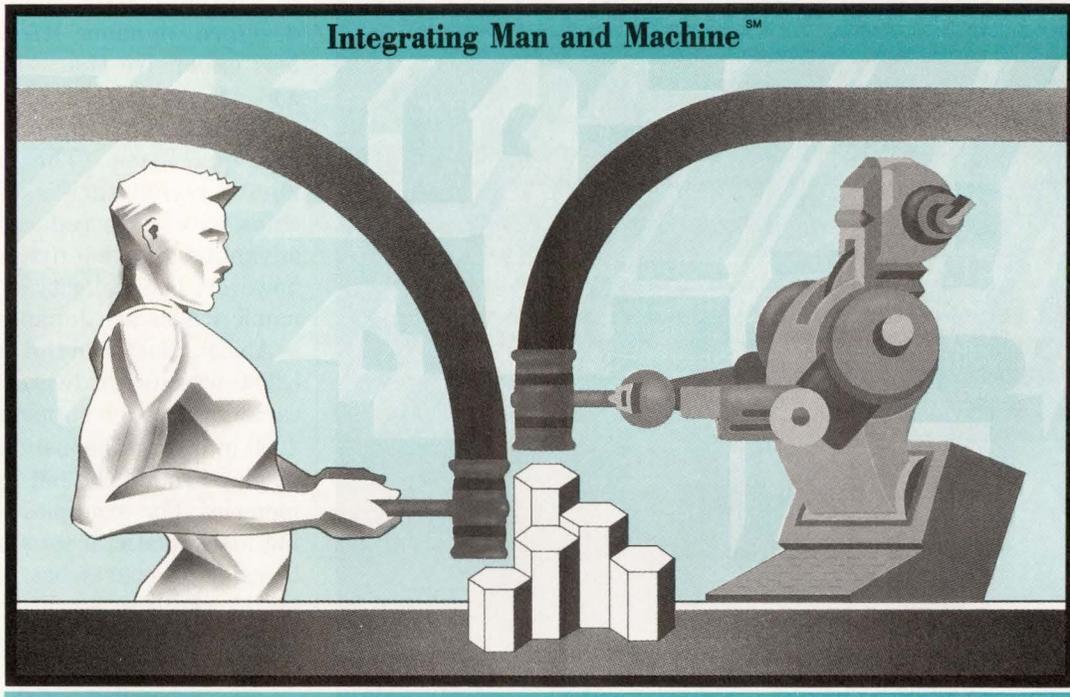
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to offer a graphics board that was capable of controlling a large memory. At the time the board was being designed, dynamic RAMs were far less expensive than video RAMs, and 1M-bit video RAMs were not (and still aren't) available in production quantities. (The US government's recent tariffs on Japanese chips have since reduced the price advantage of using dynamic RAMs, however: The majority of 1M-bit dynamic RAMs are Japanese.)

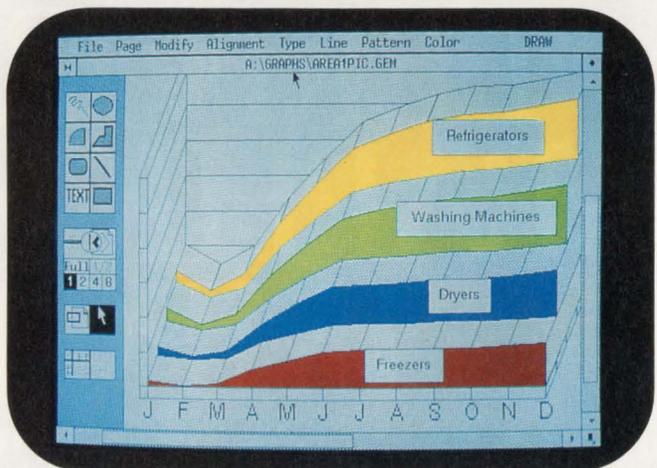
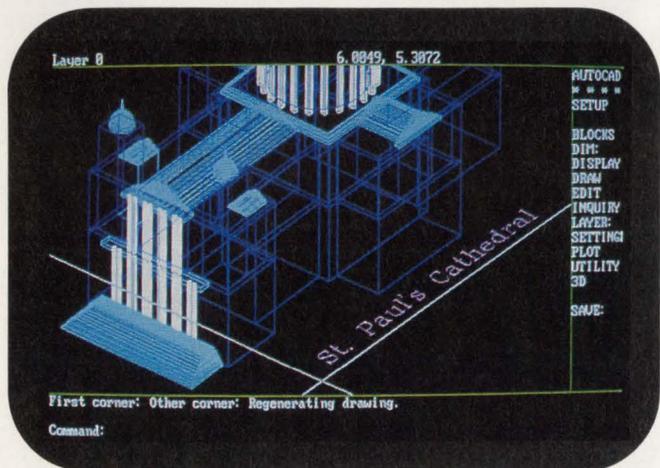
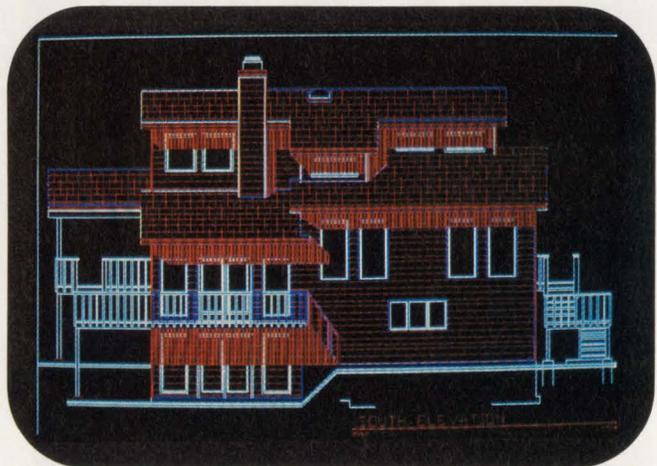
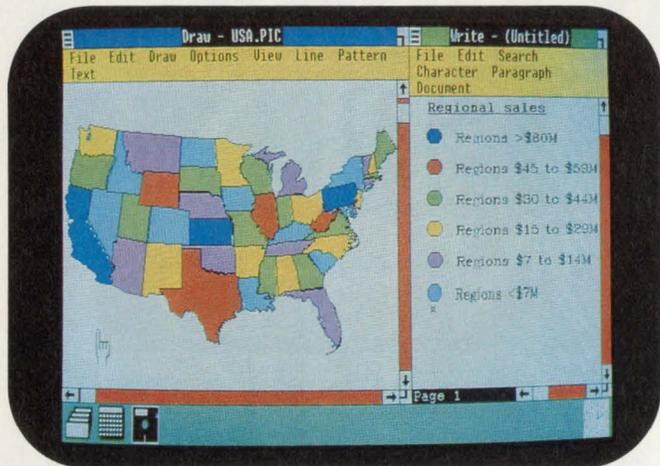
Another factor in the choice of the 82786 was its hardware windowing capability, which supports the VCS 2000 in instantaneously shifting the display around the 8M-byte display memory. For example, while viewing a schematic, a user might want to call up a parts list; these tasks might require scrolling and panning. The 82786 can handle such window manipulations at hardware speeds, regardless of the window's size (hardware windowing is based on pointers selecting the portion of memory to be displayed). Note that Vista and Univision chose opposite sides of the resolution/hardware windows coin: Univision's board has eight bits of pixel resolution and no hardware windowing; Vista's product has hardware windowing, but provides only monochrome display.

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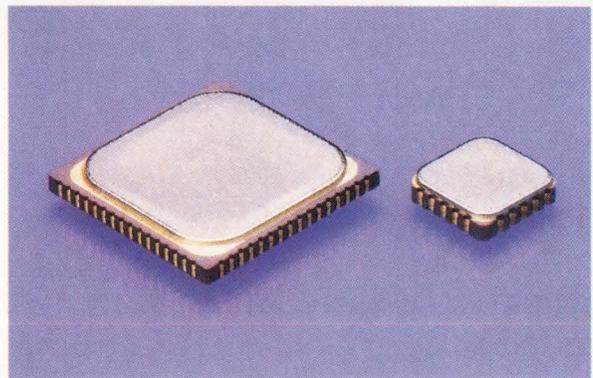
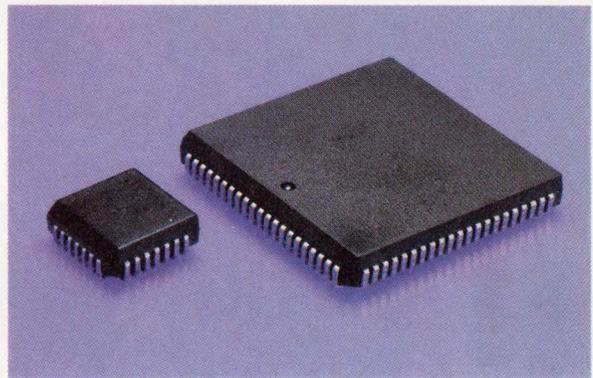
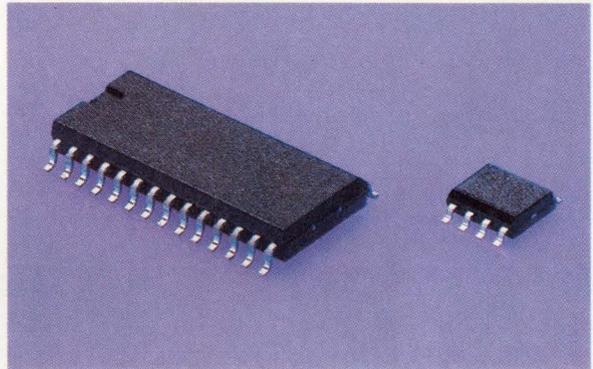
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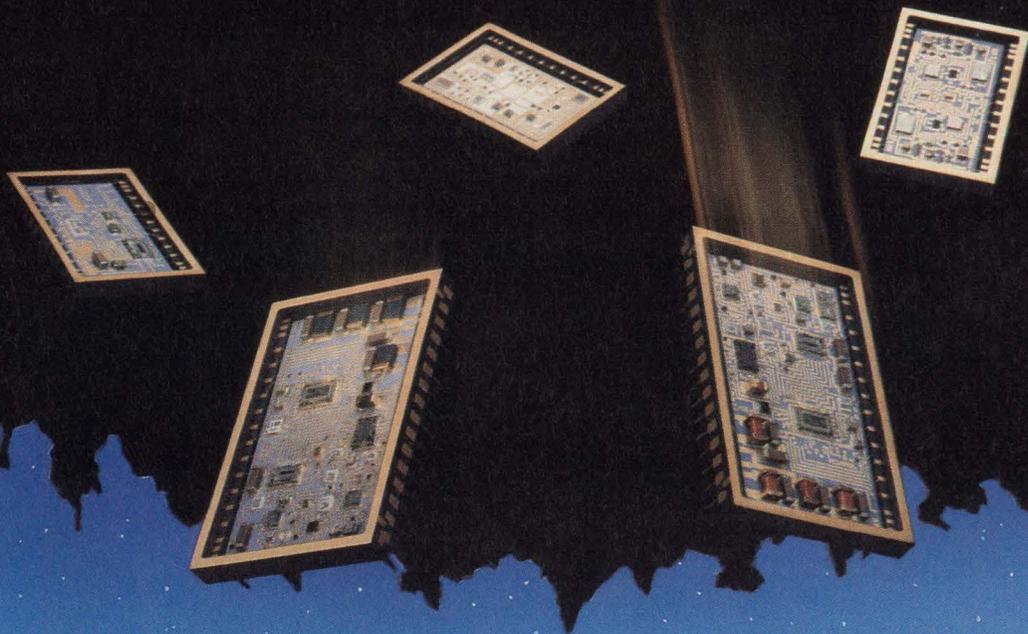
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Comparisons reveal the pros and cons of designing with switched-capacitor ICs

David Shear, *Regional Editor*

Now that the telecommunications industry is no longer dictating the performance levels of switched-capacitor components, many more flexible models of these ICs are rapidly becoming available. But although the options abound for different applications, you should consider some of the drawbacks involved in designing with switched capacitors. Disadvantages in performance may outweigh such advantages as the low cost and ease of design that switched-capacitor components can often claim. Your specific application will of course figure largely in your final choice; nevertheless, some general rules are relevant, and some pitfalls may send you running back to the corresponding conventional linear devices.

The most popular application of combining switches and capacitors is switched-capacitor-filter implementation. Some common characteristics of these devices are low-pass, highpass, Bessel, and Butterworth. Sometimes the manufacturer defines all the parameters, but in some cases, the user can specify some parameters according to his application. A filter's corner frequency is determined by a clock supplied to the filter. A corner frequency is the clock frequency divided by some number, usually 50 or 100. (For more detailed information on switched-capacitor filters, see **Ref 1** and **Ref 2**.)

The accuracy of the corner frequency is a major advantage of switched capacitor filters (see **box**, "Switched-capacitor filters"). The clock- to center-frequency ratio of Linear Technology's \$8.25 (100)



Combining in-circuit emulation with menu-driven software, the Filter Development System from Crystal Semiconductor allows anyone who can describe the parameters of a filter to test the design. It's used in conjunction with the CS7008 universal active filter.

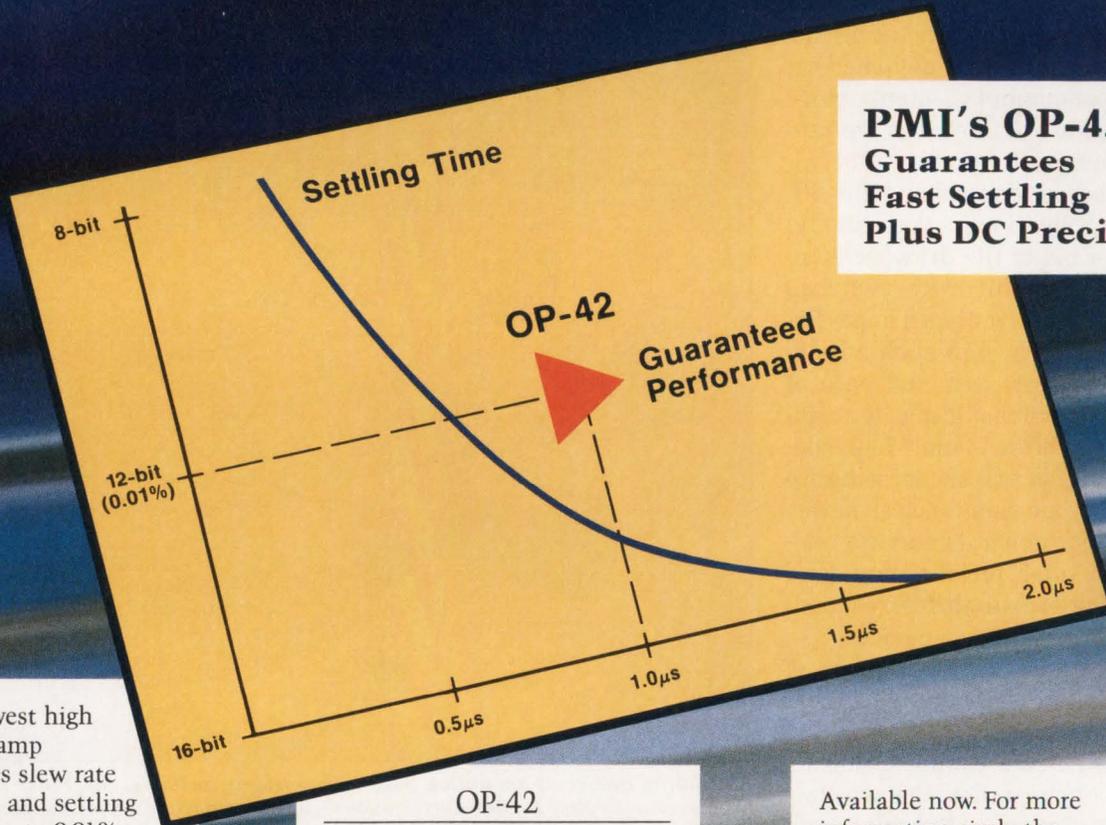
LTC1061 Triple Universal Filter Building Block is 50:1 or 100:1 with an accuracy of $\pm 1.2\%$. As long as the clock you use is also very stable, the $\pm 1.2\%$ accuracy is very stable over time and the full temperature range (better than ± 1 ppm/ $^{\circ}\text{C}$). The monolithic construction and use of capacitor ratios creates this outstanding stability. By varying the clock frequency, you can tune the corner frequency from less than 1 Hz to 40 kHz. For applications requiring frequencies of less than 1 Hz, these filters save you much both in cost and in pc-board real estate because they don't require the large

capacitors that a conventional filter needs for low-frequency applications.

Switched-capacitor filters are intrinsically easy to use in a design. Crystal Semiconductor's \$30 (100) CS7008 Universal Filter and the CDS7000 Filter Development System (\$3599) make designing a switched capacitor filter even easier. The CS7008 is a digitally configurable filter that you can use in the audio band for even-order filters up to the eighth order. To configure an actual filter, you can load the parameters from a PROM, from which the filter can self-load, or you can

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load the parameters via the universal filter's μ P interface from a host microprocessor.

The Filter Development System is an IBM PC-based system that includes an in-circuit emulator. Anyone who can define, via menus, the parameters of a filter can quickly test the filter in the target system.

Noise remains a concern

Noise has always been a concern when evaluating switched-capacitor filters. As the noise goes up, the signal-to-noise (S/N) ratio de-

creases. The output noise of EG&G Reticon's \$6.50 (50) RF5609A seventh-order elliptic lowpass filter is 2.5 mV rms whereas the company's \$5.25 (50) RU5622A 8-pole universal active filter specs 240 μ V rms. Linear Technology claims that the LTC1061 has a wideband rms noise level of less than 100 μ V rms. With a maximum input voltage of 3V rms and a wideband rms noise of 55 μ V rms, the resulting S/N ratio for the LTC1061 is 95 dB.

The total harmonic distortion (THD) provides a good indication of a device's linearity. The THD of

switched-capacitor filters will increase with increasing input-voltage swing. As a result, increasing the maximum signal (and the S/N ratio) also increases the THD. If your application requires that the THD be kept to a minimum, you must decrease the maximum input signal, which in turn decreases the S/N ratio. The current consensus is that a S/N ratio of about 80 dB results in a THD that's below the noise floor.

Unfortunately, the typical switched-capacitor filter also has an input offset voltage (V_{OS}) of a few hundred millivolts. Linear Technology's \$3.55 (100) LTC1062 fifth-order lowpass filter does not have the offset problem because that filter actually operates outside the dc path.

Chopper-stabilized op amps

Another application of switches and capacitors is the chopper-stabilized op amp (see **box**, "Chopper-stabilized op amps"). Using switched-capacitor techniques, this amplifier continuously recalibrates the input in order to subtract the input offset voltage. This technique results in an initial offset voltage of 5 μ V and a drift of 0.05 μ V/ $^{\circ}$ C. And you don't even have to trim to obtain these impressive offset specifications.

Of course noise plagues this application just as it does all the others, and it limits the dynamic range. **Fig**

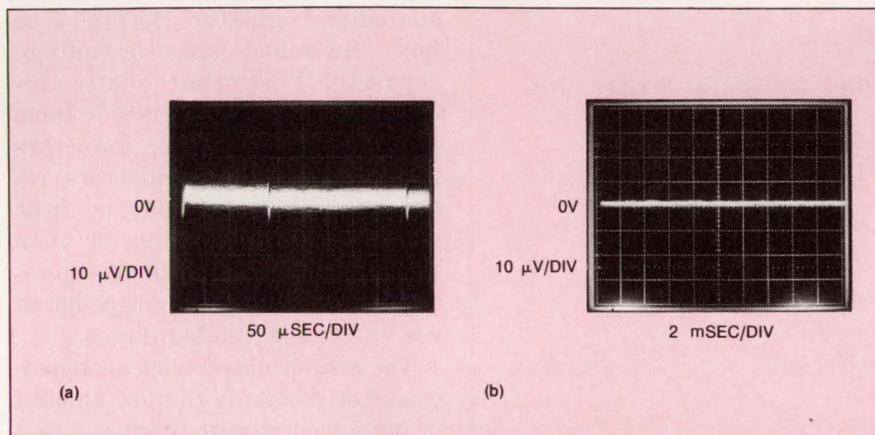


Fig 1—The noise of a chopper-stabilized op amp (a) is 10 μ V p-p with 16 μ V p-p switching spikes. The noise of a conventional OP-77 op amp (b) is on the order of 2 μ V p-p. For both cases, gain equals 1000.

Switched-capacitor filters

Switched-capacitor filters exhibit the following advantages and disadvantages in comparison to conventional filters.

Advantages:

- Good corner frequency accuracy (0.6%)
- Good corner frequency stability (1 ppm/ $^{\circ}$ C)
- Ease of design
- Small pc-board area
- Very low frequency (<1 Hz)
- Low cost
- Monolithic implementation.

Disadvantages:

- High noise (>10 μ V)
- Large V_{OS} (>100 mV)
- Aliasing problems
- High THD
- Low corner frequency (<40 kHz)
- Low voltage swing (<10V p-p)
- Requirement for system-generated clock frequency
- Clock required for analog function
- Limited dynamic range (<95 dB)
- May need post-filtering.

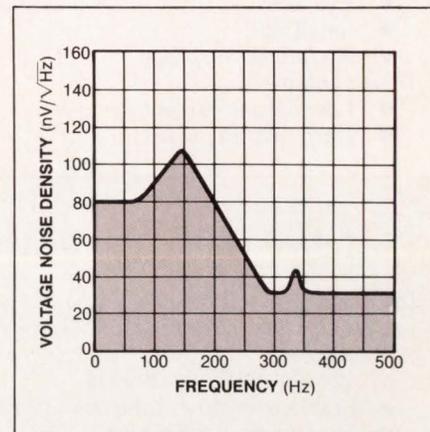


Fig 2—The 1/f noise of a chopper-stabilized op amp actually decreases at low frequencies, where a conventional op amp's noise increases at a 3-dB/octave rate.

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1 shows the noise from a precision monolithic op amp and the noise from a chopper-stabilized op amp. However, the chopping process actually reduces noise for the very low-frequency ranges. Fig 2 shows that the 1/f noise of a chopper stabilized op amp at very low frequencies does not follow the standard 3-dB/octave increase.

Chopper-stabilized op amps do not have very fast settling times or overload recovery time because they sample the signal at a rather low rate (around 400 Hz). The output

will approach the final value rather quickly and then step to the final value at the sample rate.

The chopper-stabilized op amp has a very long overload recovery time. If a chopper stabilized op amp reaches saturation, the external capacitors are driven to a supply rail, and the time it takes the capacitors to recover is usually in the hundreds of milliseconds. The overload recovery of a conventional op amp will be less than 10 μ sec.

Chopper-stabilized op amps have generally required external capaci-

tors on the pc board. However, some devices, like Maxim's \$5.65 (100) MAX 430/432, now have the capacitors within the package. The MAX 430/432 has the added advantage of working on $\pm 15V$ instead of the more standard $\pm 5V$. Also, it uses the standard 8-pin op-amp configuration, so you can replace an existing amplifier with a chopper-stabilized version without modifying your pc board.

Making a negative supply

Ease of design is a major advantage when you compare a switched-capacitor voltage converter to a switching-regulator design (see box, "Switched-capacitor voltage converter") because the latter requires the use of inductors or some form of magnetics. No inductors means less noise. The inductors create spikes when switched, and these spikes are typically noisier than those created by switching capacitors. Low cost and small pc-board real estate are also big pluses.

The main problem with switched-capacitor design is the low amount of output current it produces. You can use Intersil's \$1.40 (100) ICL7660 to supply 20 mA, for example, but the output will only be $-4V$ —instead of $-5V$ —because the output won't be regulated. The Maxim MAX 680 $+5V$ to $\pm 10V$ Voltage Converter (\$2.16 in 100s) creates a dual supply from a single 5V source, but it too is unregulated.

Linear Technology's \$2.95 (100) LTC1054 switched-capacitor voltage converter is a monolithic bipolar converter with a regulator. It's pin compatible with the ICL7660 and can supply 100 mA on the negative rail. The LTC1054 also includes a 2.5V bandgap reference and an error amplifier. If you want a regulated negative output, you can provide two external resistors for feedback from the output to the error amplifier.

Among the many other applications of switched capacitors, Linear Technology's \$2.95 (100) LTC1043

Chopper-stabilized op amps

When compared to monolithic op amps, chopper-stabilized op amps stack up like this:

Advantages:

- Low V_{OS} drift (0.05 $\mu V/^\circ C$)
- Low initial V_{OS} (5 μV)
- No testing needed
- No trimming required
- Low noise at low frequency.

Disadvantages:

- Higher noise
- Limited dynamic range
- External capacitors required
- Slow settling times
- Poor overload recovery (>100 msec).

Switched-capacitor voltage converters

Switched-capacitor voltage converters have the following advantages and disadvantages in comparison with switching regulators.

Advantages:

- Ease of design
- Low cost
- Small size
- No inductive spikes.

Disadvantages:

- Low output current
- Unregulated output.

Switched-capacitor instrumentation amplifiers

In comparison with conventional instrumentation amplifiers, switched-capacitor instrumentation amplifiers reveal the following characteristics:

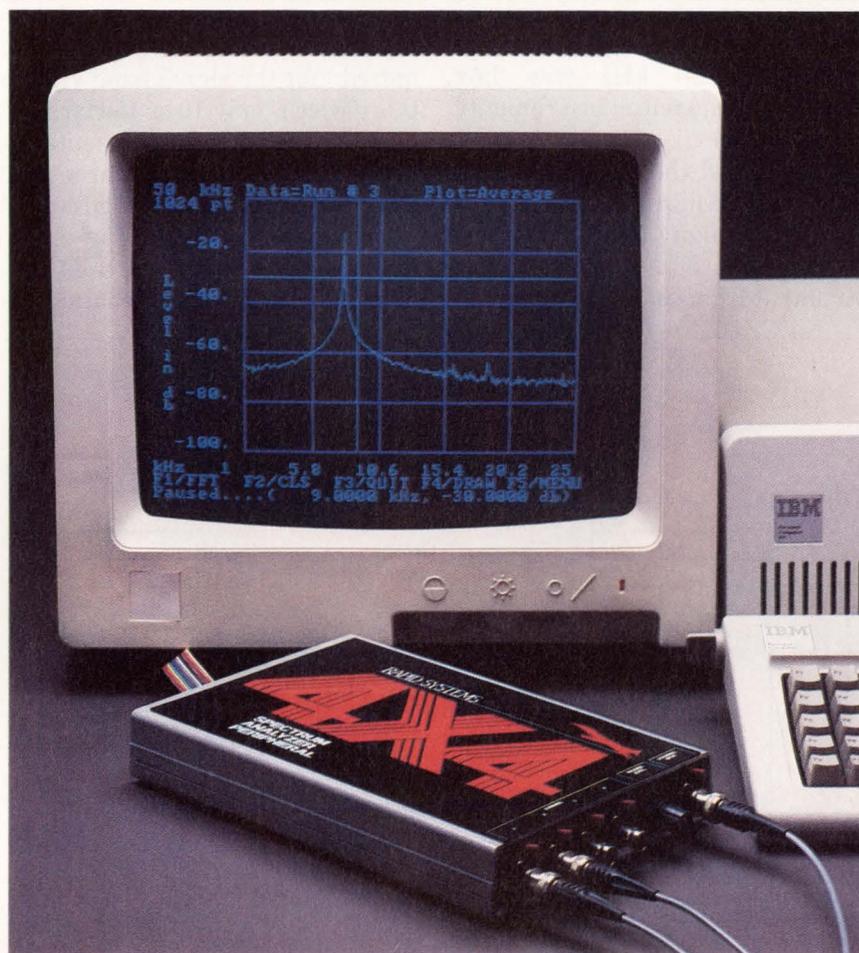
Advantages:

- 120-dB CMRR to 20 kHz
- Stable over time, temperature range
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- Low cost, no precision components.

Disadvantage:

- Low frequency (<15 Hz).

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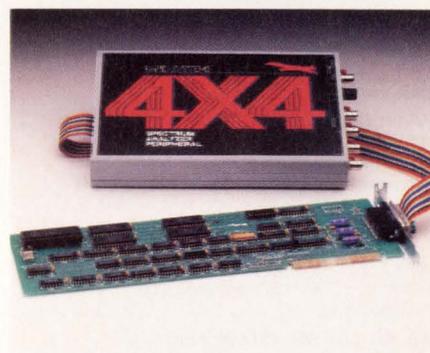
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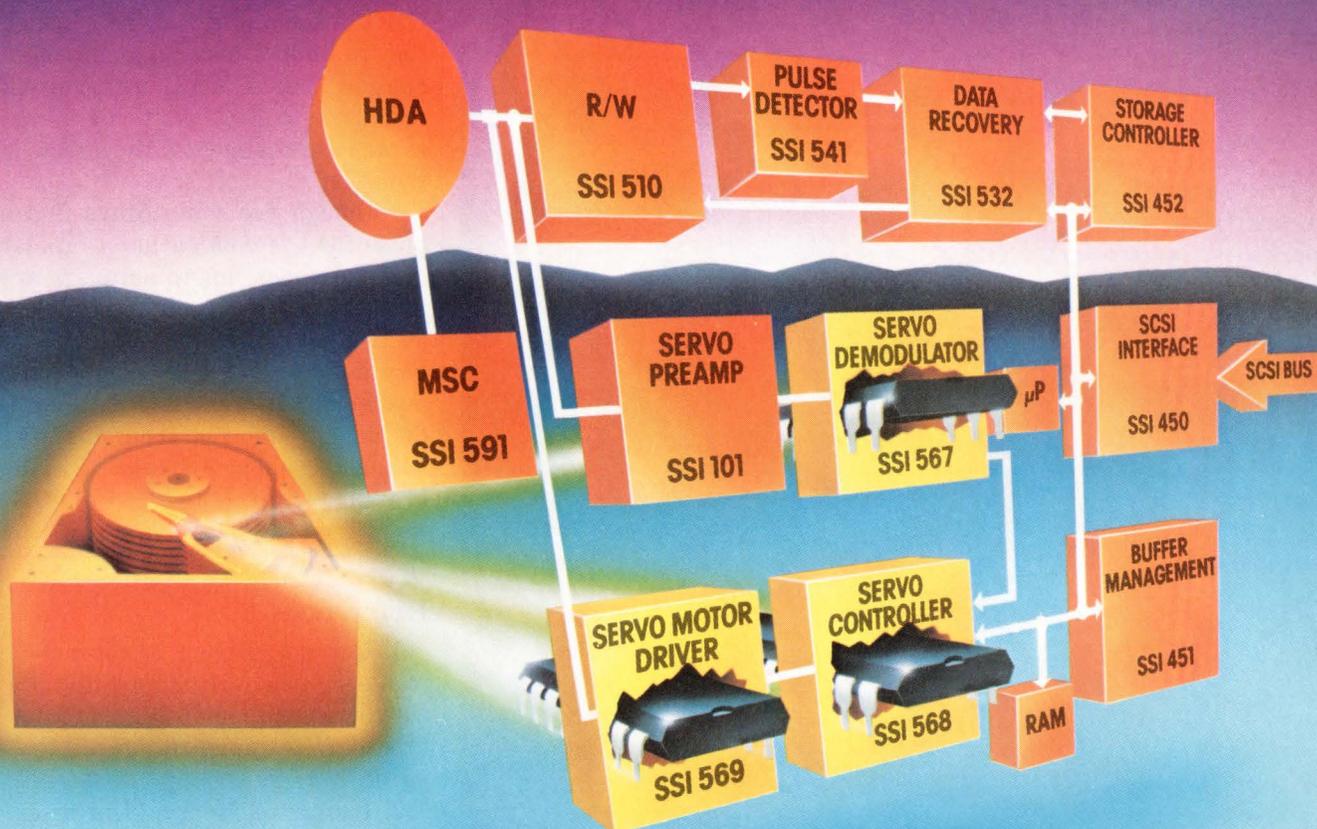
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tics of any device with substantial reduction of its V_{OS} . For example, Fig 3 shows a method of reducing the V_{OS} of a switched-capacitor filter. You can only use the LMC669 in an inverting configuration.

One inherent limitation of most switched-capacitor ICs lies in the CMOS technology with which they're built. Bipolar is much more rugged than CMOS, in terms of resistance to electrostatic discharge as well as resistance to the effects of radiation.

Although you will always find a place for the conventional bipolar linear devices, manufacturers are using switched-capacitor technologies to create other options. They are beginning to make new components available that are stable and reproducible, require no trimming, cost less, and could prove easy to include in your next design. **EDN**

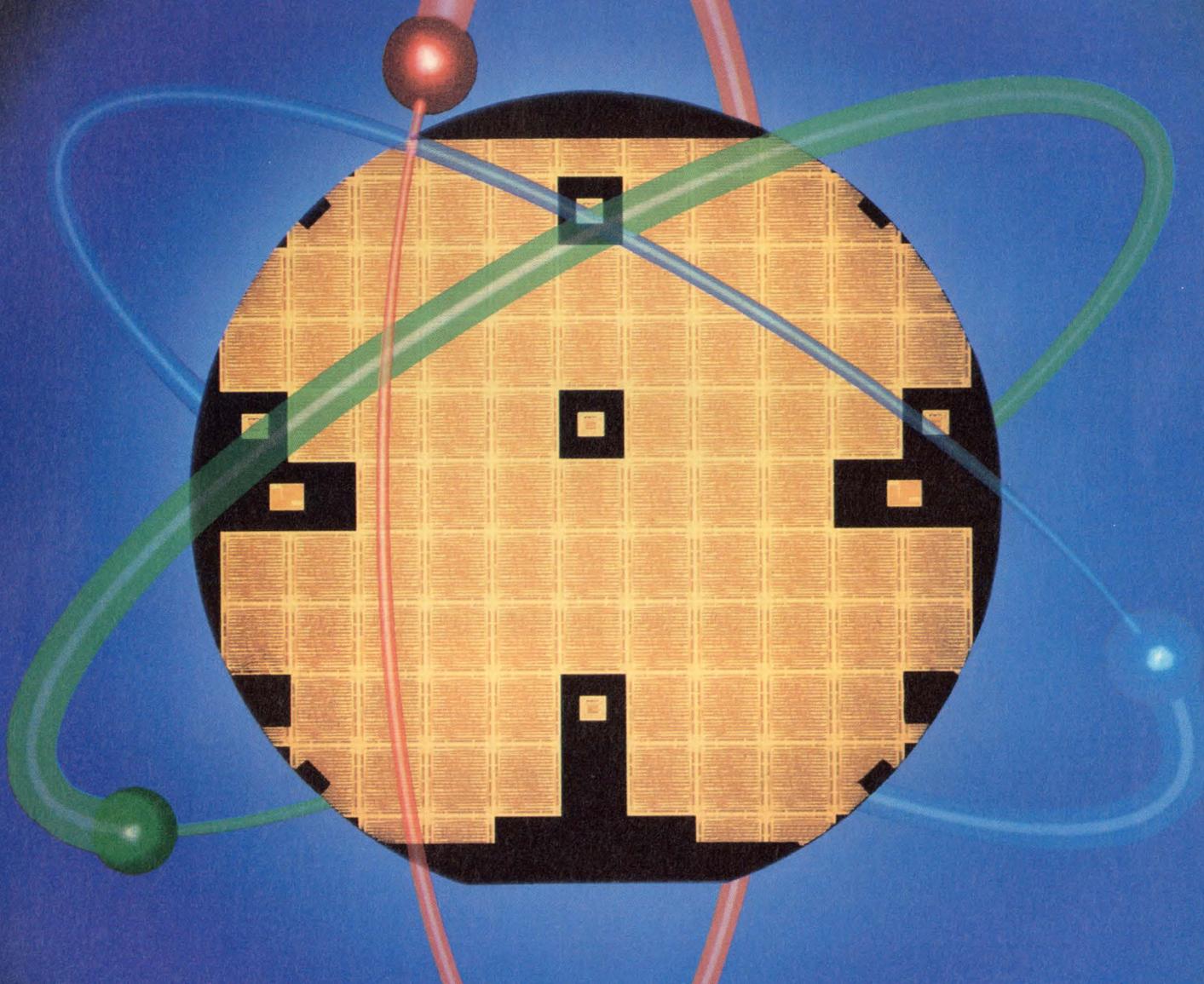
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1. Cormier, Denny, "Programmable switched-capacitor filter ICs cut component count in many filter types," *EDN*, June 26, 1986, pg 71.
2. Lacanette, Kerry, "Universal switched-capacitor filter lowers part count," *EDN*, April 3, 1986, pg 139.

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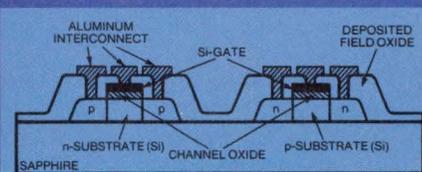
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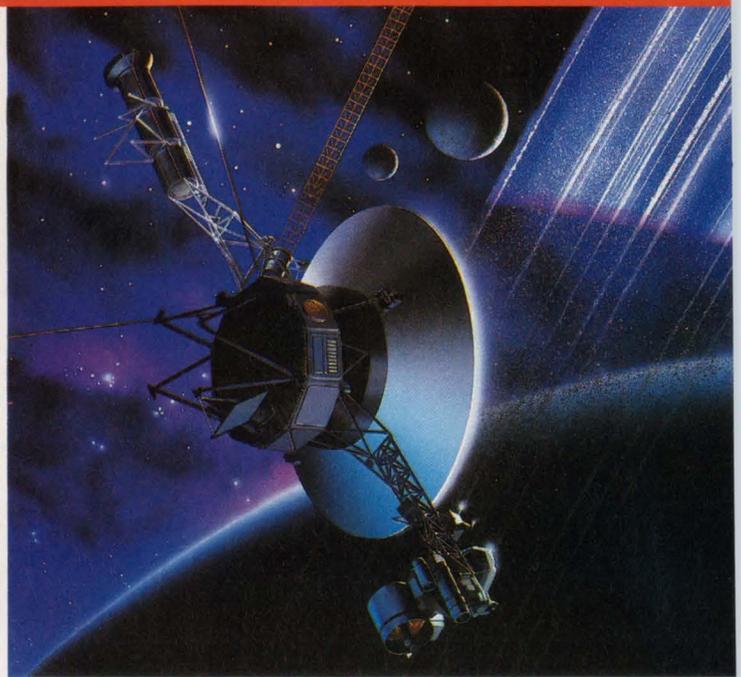
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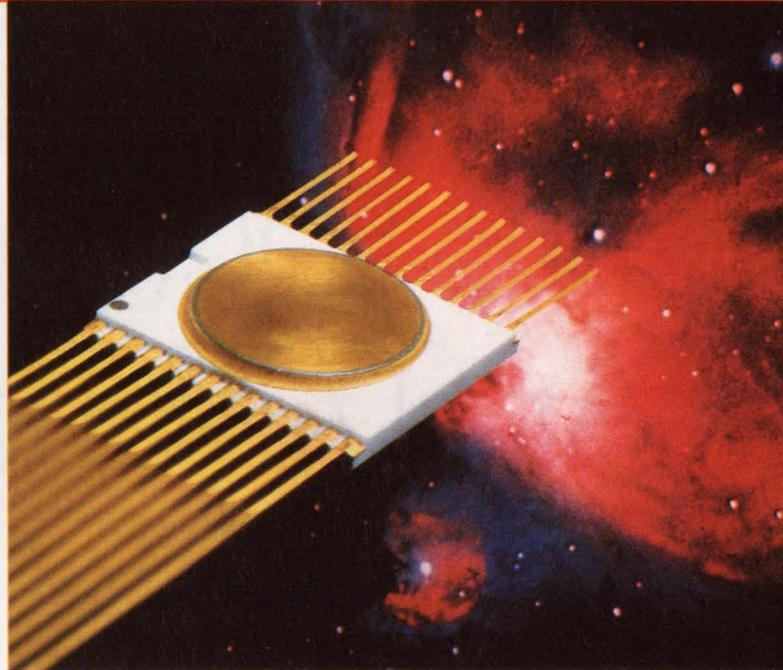
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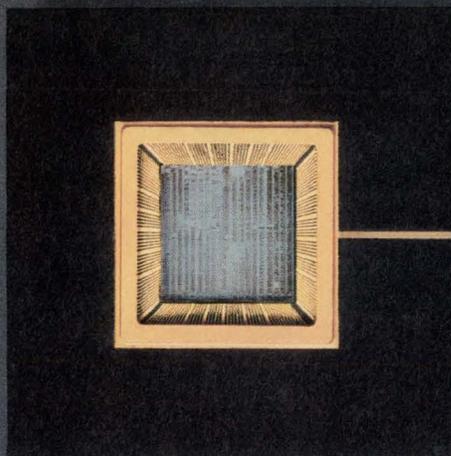
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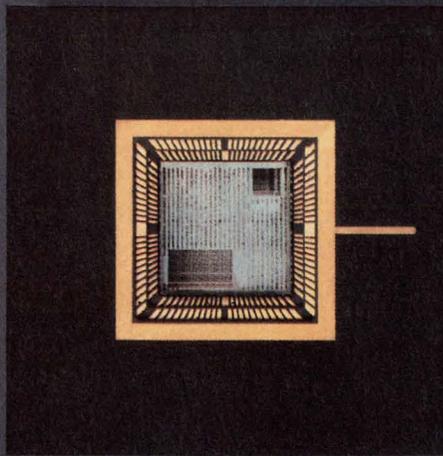
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Beware of subtle electrical, thermal differences between through-hole components and SMDs

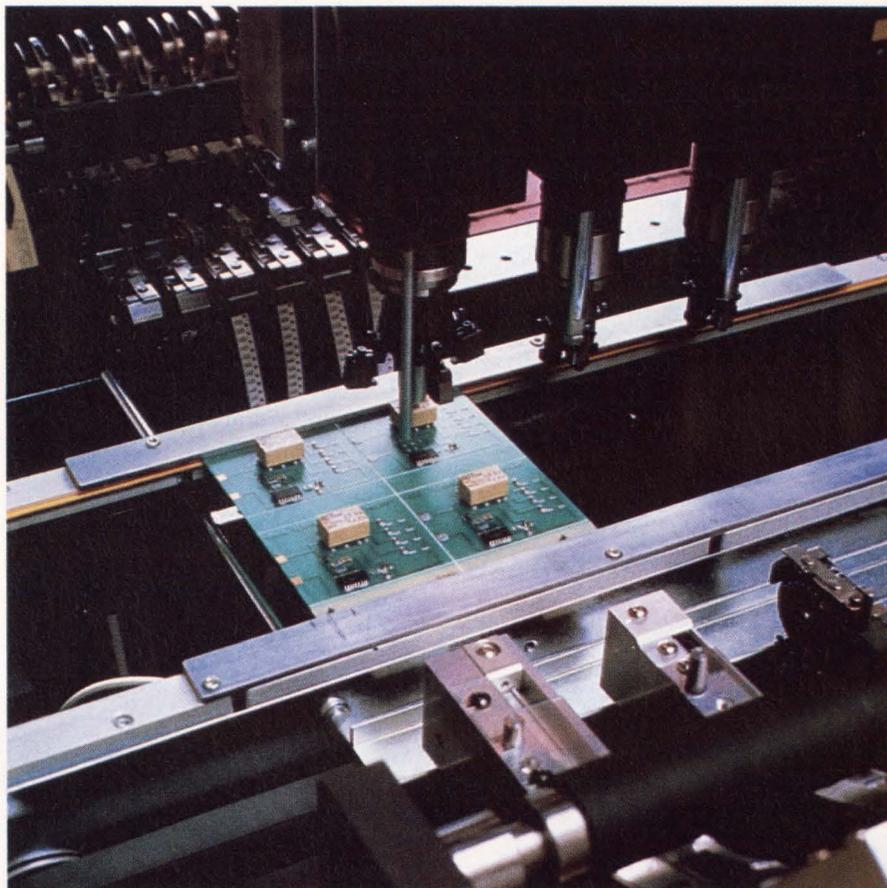
Charles H Small,
Associate Editor

Component manufacturers are shipping new surface-mount-technology (SMT) versions of old, existing through-hole components under the older parts' spec sheets, reflecting the needs of component and manufacturing engineers, not design engineers. As SMT reaches the R&D lab, design engineers will have to pay attention to some subtle, yet important, electrical and thermal differences between equivalent SMT and through-hole components or risk unforeseen problems with their designs. Design engineers can't afford to ignore SMT forever because many new, high-performance components are available only as surface-mount designs.

Although the engineering community has heard much about SMT and the difficulties the technology presents to pc-board designers and manufacturing and test engineers, little education has been directed toward design engineers. **Tables 1 and 2** list the measured parameters of equivalent through-hole and SMT packages.

Component makers aren't certifying the newly repackaged SMT components to existing specs in order to deceive anyone. Component and manufacturing engineers need parts that conform to in-house quality-assurance standards as closely as possible. Also, SMT components aren't easy to characterize because their small physical geometries and thermal mass tax existing measurement techniques.

The good news is that because of their smaller size, SMT components have less lead inductance and lead-to-lead capacitance than equivalent through-hole parts. Consequently,



Not all components change when designed into SMT packages. These relays, for example, have identical mechanical and electrical specs to their through-hole counterparts. (Photo courtesy Omron)

SMT components have faster rise times and exhibit less ringing than do their through-hole counterparts.

The bad news is that because of their smaller size, SMT components have poorer thermal performance than through-hole parts. Active SMT devices, for example, use smaller lead frames and less-massive pins. Consequently, an active SMT device cannot conduct heat out as well as a DIP can.

Designers ignored

Presently, most of the action in SMT revolves around pc-board layout and manufacturing because

SMT means new production machinery, layout standards, and test procedures. SMT soldering methods subject components to a higher degree of thermal stress than through-hole components. Most component engineers are intent on certifying packaging that suits automated assembly and that will withstand soldering and cleaning. There are three factors, however, that are propelling the electronics industry toward SMT—smaller products, faster circuits, and automated assembly—and these first two factors also affect design engineers.

Until component engineers com-

Surface mounted components do a lot more than merely reduce size

Today's demand for smaller and smaller electronic systems has fostered the creation of a large number of surface mounted chip components. This has resulted in the more efficient utilization of available PCB space with the net result of vastly reduced product size. That's the obvious advantage of surface mount. But there's more than just the obvious.

Improved electrical performance: Smaller, leadless components with shorter interconnections result in reduced stray capacitance and lower inductance allowing much faster operating speeds, faster rise times and higher frequency response.

Lowered manufacturing costs: Significant savings are achieved through elimination of the necessity for drilling

and plating thru holes in PCB's and by reduction in the overall PCB size and number of layers required.

Automated assembly: Surface mounted components permit the use of the latest automated assembly techniques leading to greater product consistency, higher reliability, better yields and a faster production capability.

Standardized designs: Component and packaging standards reduce product design efforts.

Shock and vibration resistance: Due to their low mass, small size, and strong solder interconnects, surface mounted components have exceptional resistance to shock and vibration.

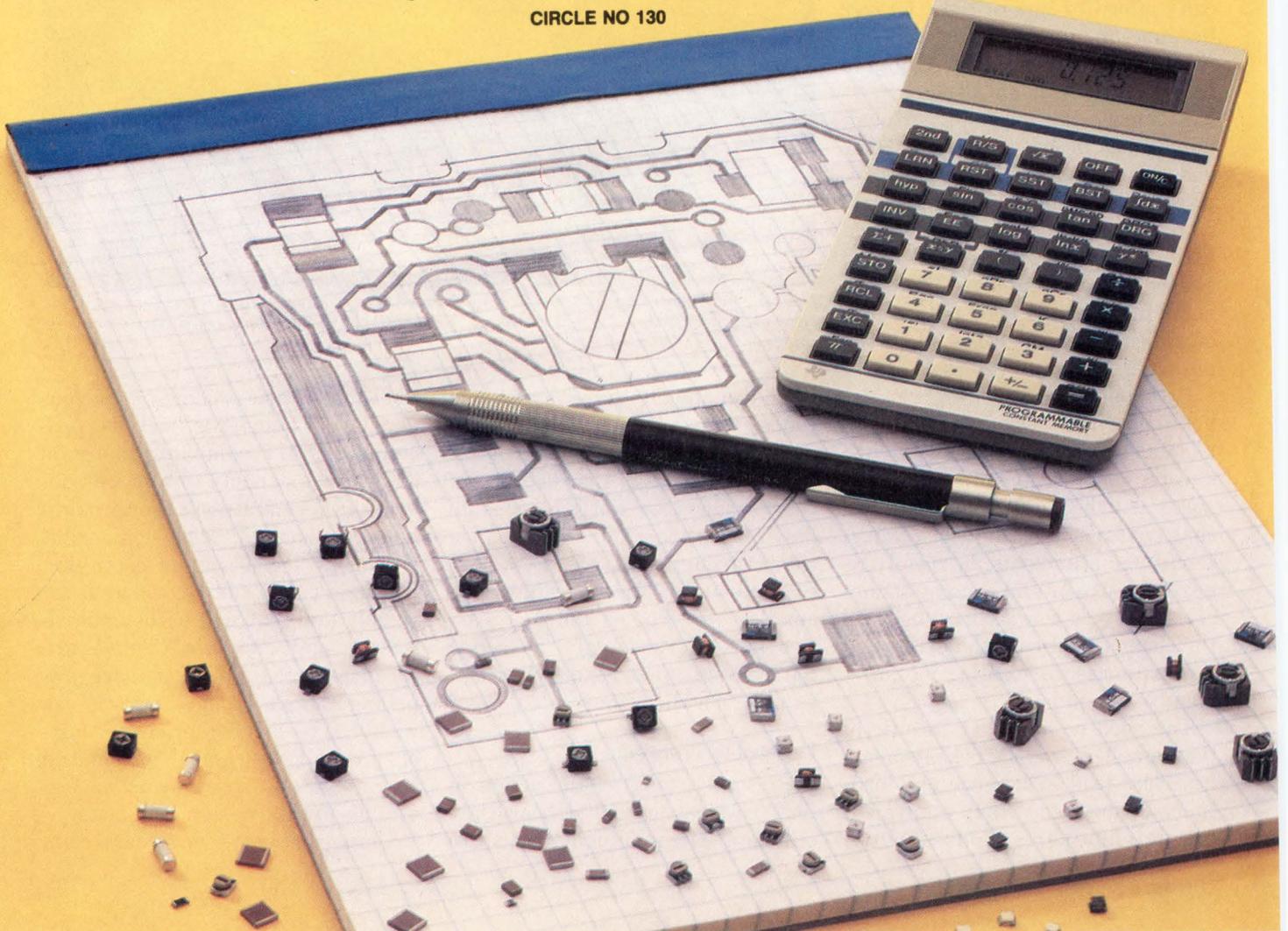
Product synergism: With a wide range of surface mounted configurations now available—ceramic capacitors, ceramic trimmer capacitors, fixed resistors, trimming potentiometers, inductors, ceramic resonators and ceramic filters—problems resulting from the integration of leaded and surface mounted devices have been significantly reduced.

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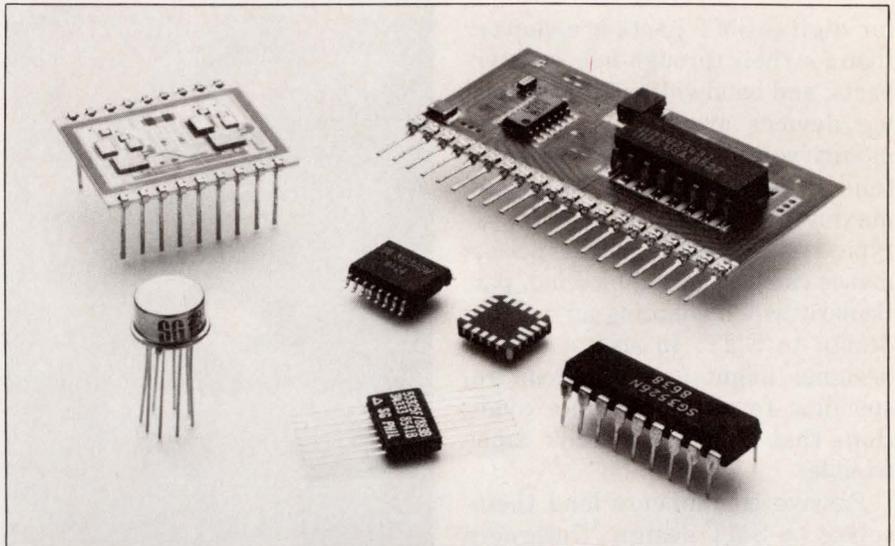
TECHNOLOGY UPDATE

plete the monumental job of thoroughly recharacterizing SMT versions of through-hole components, design engineers will have to investigate the performance of SMT components themselves before attempting an SMT-based design. For instance, component engineers recommend that design engineers request reliability data derived from MIL-spec testing, even if a design isn't destined for installation in a military system. The MIL-spec humidity tests are particularly enlightening. Because of the thermal stress that SMT devices encounter during soldering, the packages are subject to cracking. Devices lacking in hermeticity, when tested under high-humidity (85%) conditions, will quickly fail.

Thermal skills are lacking

Design engineers have never been as good at thermal analysis as they have been at electrical analysis. SMT will only make this situation worse. Computers will not be of much help at first because existing thermal-analysis software isn't set up for SMT components.

SMT designs will perforce pack more components into a given volume. Industry experts estimate that even the least-dense SMT design will be twice as dense as the same design executed with through-



SMT components promise smaller, faster circuits, but a host of subtle spec differences may trip up the unwary design engineer faced with converting through-hole designs to SMT. (Photo courtesy Silicon General)

hole components. Further, SMT components will probably run at higher speeds than ever before.

The greater density and higher speeds of an SMT design, coupled with the relatively poorer thermal performance of SMT packages vs through-hole designs, means that design engineers will have to do more thorough thermal testing of their SMT designs at the prototype stage than they have in the past. Even when recasting an existing through-hole design for SMT, designers may opt to substitute low-power CMOS parts for bipolar.

Power-supply designers report, for example, that power-handling components having a built-in thermal-shutdown feature may cycle on and off much faster than expected. The culprit here is the SMT power-handling device's lower thermal mass. A short-circuited regulator in a TO-3 package might take a second or more to cycle on and off. The SMT version of the same regulator might cycle on and off quickly enough to generate an audible tone when overloaded.

Beyond the obvious problems of dissipating the heat associated with the power-handling components, power-supply designers may find unwanted spurious oscillations because the parasitic capacitance and inductance associated with through-hole parts and through-hole pc boards no longer exists. Such designers will have to be especially careful as they switch from through-hole to SMT designs.

Fortunately, not all specs necessarily have to change when a part goes from a through-hole design to an SMT package. Equivalent through-hole and SMT digital devices have the same specifications for setup and hold times and fan-out, for example.

On the other hand, access times

**TABLE 1—14-LEAD PACKAGE CHARACTERISTICS
(14-LEAD DIP VS 14-LEAD SO*)**

R (mΩ)		L (nH)		C (pF)		
SO	DIP	SO	DIP	SO	DIP	
1.46	25	1.69	10.72	0.203	0.574	
0.83	17	1.23	7.87	0.089	0.381	
0.22	12	0.56	5.54	0.081	0.224	
0.22	6	0.42	3.59	0.079	0.229	
0.21	13	0.48	5.5	0.088	0.381	
0.72	18	0.88	6.8	0.224	0.585	
1.46	23	1.81	10.62	0.141	0.417	
1.46	24			0.222	0.588	
0.83	16			0.103	0.391	
0.35	14			0.074	0.228	
0.23	6			0.079	0.226	
0.22	13			0.079	0.382	
0.74	18			0.209	0.582	
1.45	24			0.143	0.385	
TOTAL =	10.4	229	7.07	50.64	1.814	5.573
PER PIN AVG =	0.74	16.36	1.01	7.23	0.13	0.4

*SO = SMALL-OUTLINE PACKAGE

(COURTESY: MOTOROLA INC)

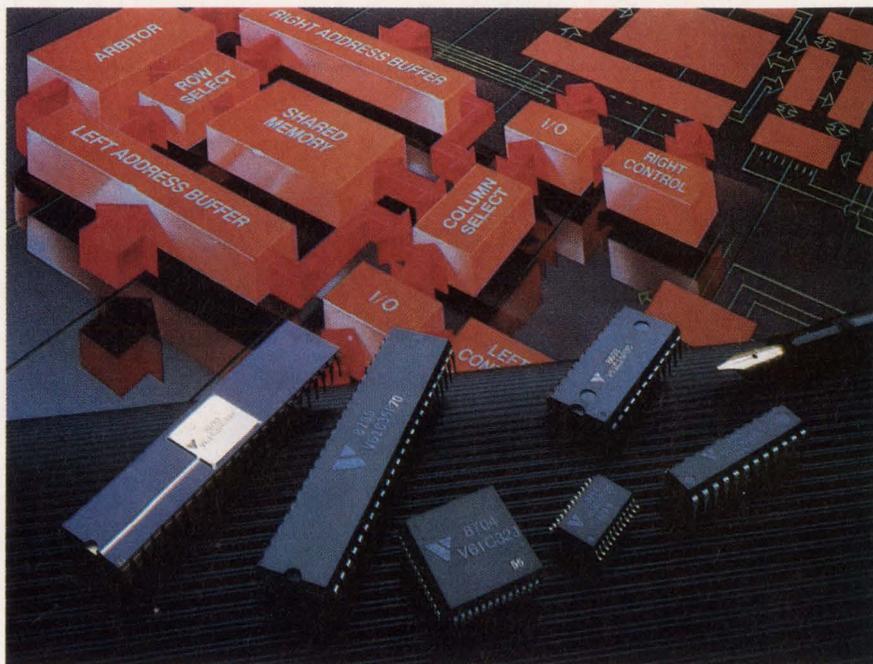
UPDATE

for digital SMT parts are shorter than for their through-hole counterparts, and bandwidths for SMT analog devices are higher. Surface-mount versions of existing parts tend to run at their spec sheets' maximum speeds rather than at typical speeds. This greater performance can be a mixed blessing, particularly when adapting an existing design to SMT. In such a case, a designer might find his circuit responding to glitches or race conditions that previously didn't cause trouble.

Passive components lend themselves to SMT design. Designers working with hybrid circuits have long enjoyed the superior performance of chip capacitors and resistors, and now these components suit pc-board applications. SMT capacitors and resistors depart less from their ideal models than do through-hole components. For example, SMT capacitors exhibit less equivalent-series inductance and equivalent-series resistance (ESL and ESR) compared with through-hole components. SMT resistors have lower inductance as well and come in handier, multiple-device packages.

Among passive components, only connectors present a problem to designers. Design engineers are just becoming aware of the deleterious ground-shift effect that a connector's inductance can have on the integrity of high-speed bus communications (see "Simple solution cures glitches on high-speed buses," EDN, April 30, 1987, pg 173).

Surface-mount designs threaten to increase both the number of I/O lines on a given board and the speed of the board's signals. The increased



When recasting an existing through-hole design to an equivalent surface-mount design, designers shouldn't assume that the new version of their design will work just like the old one. (Photo courtesy Vitelic Corp)

speed and density of surface-mount interconnections poses a challenge that SMT-connector designers must meet if their connectors are to maintain the controlled impedance necessary for high-speed buses.

Switches survive

Electromechanical components have made the switch to surface-mount technology virtually unchanged electrically and mechanically. SMT DIP switches, for example, are still on 100-mil centers. SMT relays have exactly the same design as through-hole versions. Toggle switches, too, remain unchanged.

The electromechanical industry has been in the process of reducing the size of electromechanical components for some time, but the transition to SMT is unlikely to initiate any further accelerated shrinkage for a couple of reasons.

First, the reliability of a mechanical component decreases as it gets smaller. Also, a switch that's designed for the human hand to operate can't shrink beyond a certain point or its design will be ergonomically unsound. Although electronics parts are shrinking, the human hand is not.

Further, switches, like relays, must often meet isolation and voltage-withstand specs. The dielectric constant of air and the switches' and relays' insulating materials determine the physical spacing of the devices' contacts. Switch makers are developing SMT switches with contacts on SMT spacings rather than the old through-hole spacings, but these switches aren't available yet.

Inductors in SMT packages are becoming available. Like electromechanical components, inductors have made the transition to SMT virtually unchanged in electrical performance. The only trouble SMT inductors present is possible unwanted cross-coupling from closely spaced components. **EDN**

**TABLE 2—40/44-LEAD PACKAGE CHARACTERISTICS
(40-LEAD DIP VS 40-LEAD PLCC*)**

	R (mΩ)		L (nH)		C (pF)	
	PLCC	DIP	PLCC	DIP	PLCC	DIP
MIN	3	4	3.2	1.4	0.1	0.1
MAX	6	7	3.5	19.1	0.3	3.0

*PLCC = PLASTIC LEADED CHIP CARRIER

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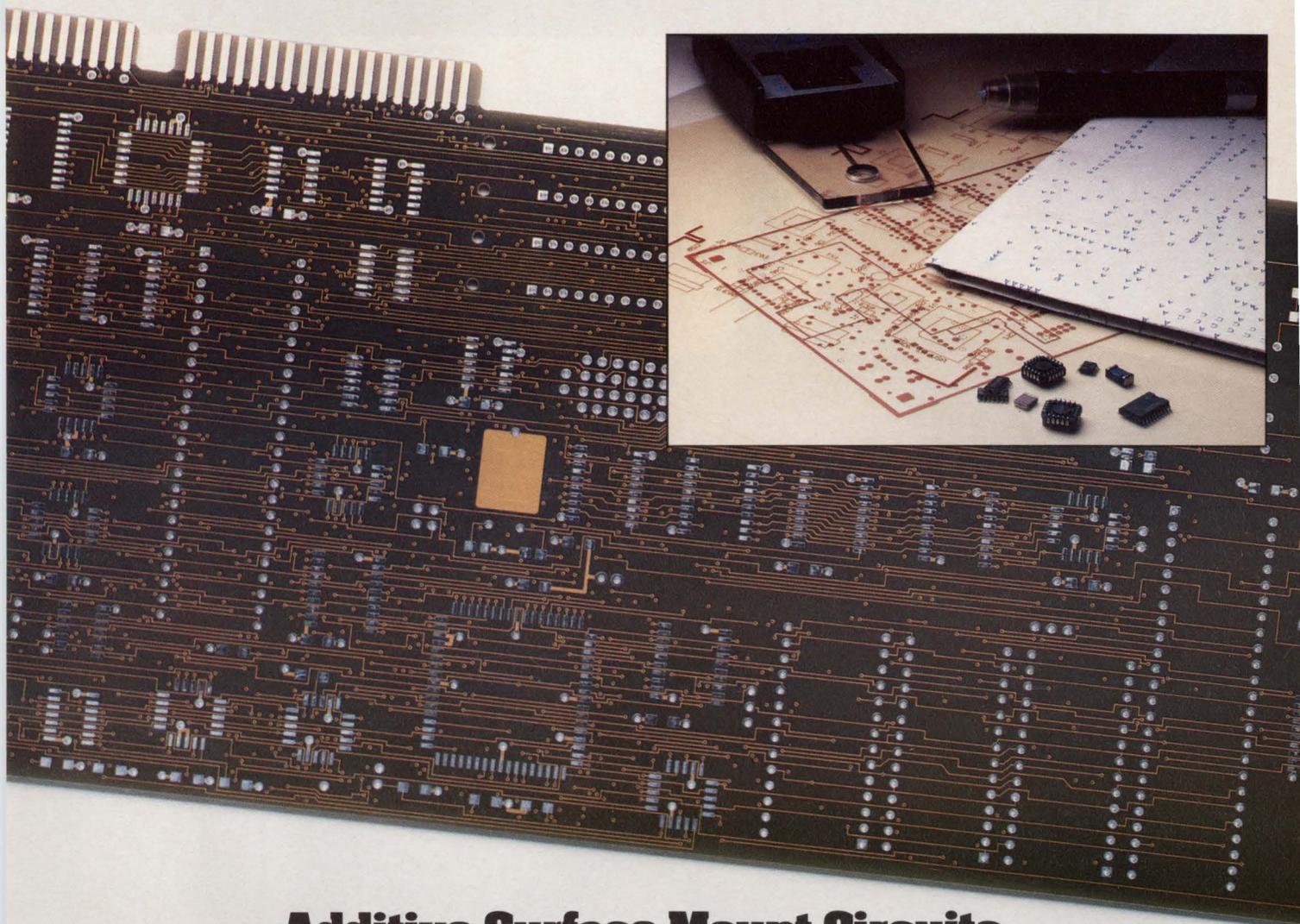
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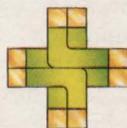
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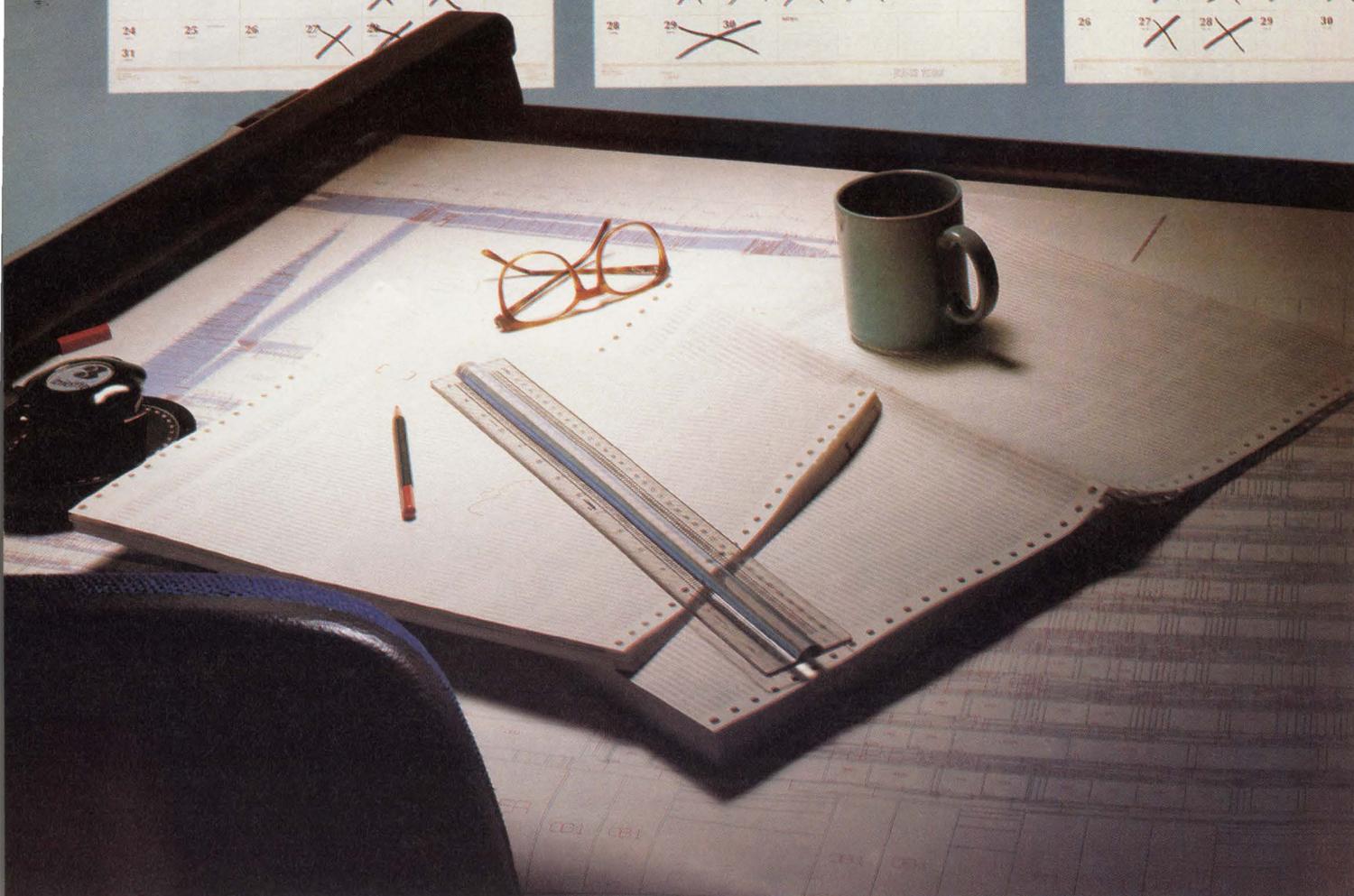
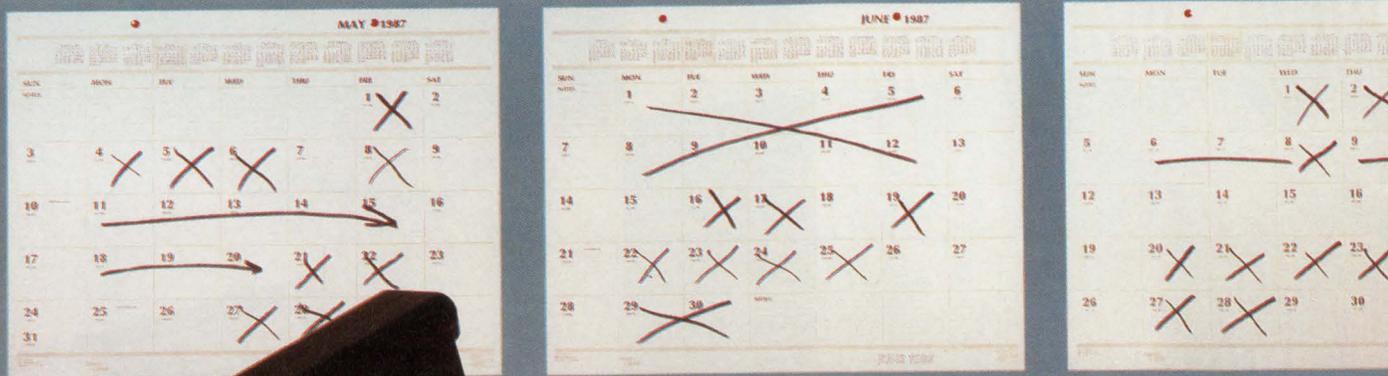
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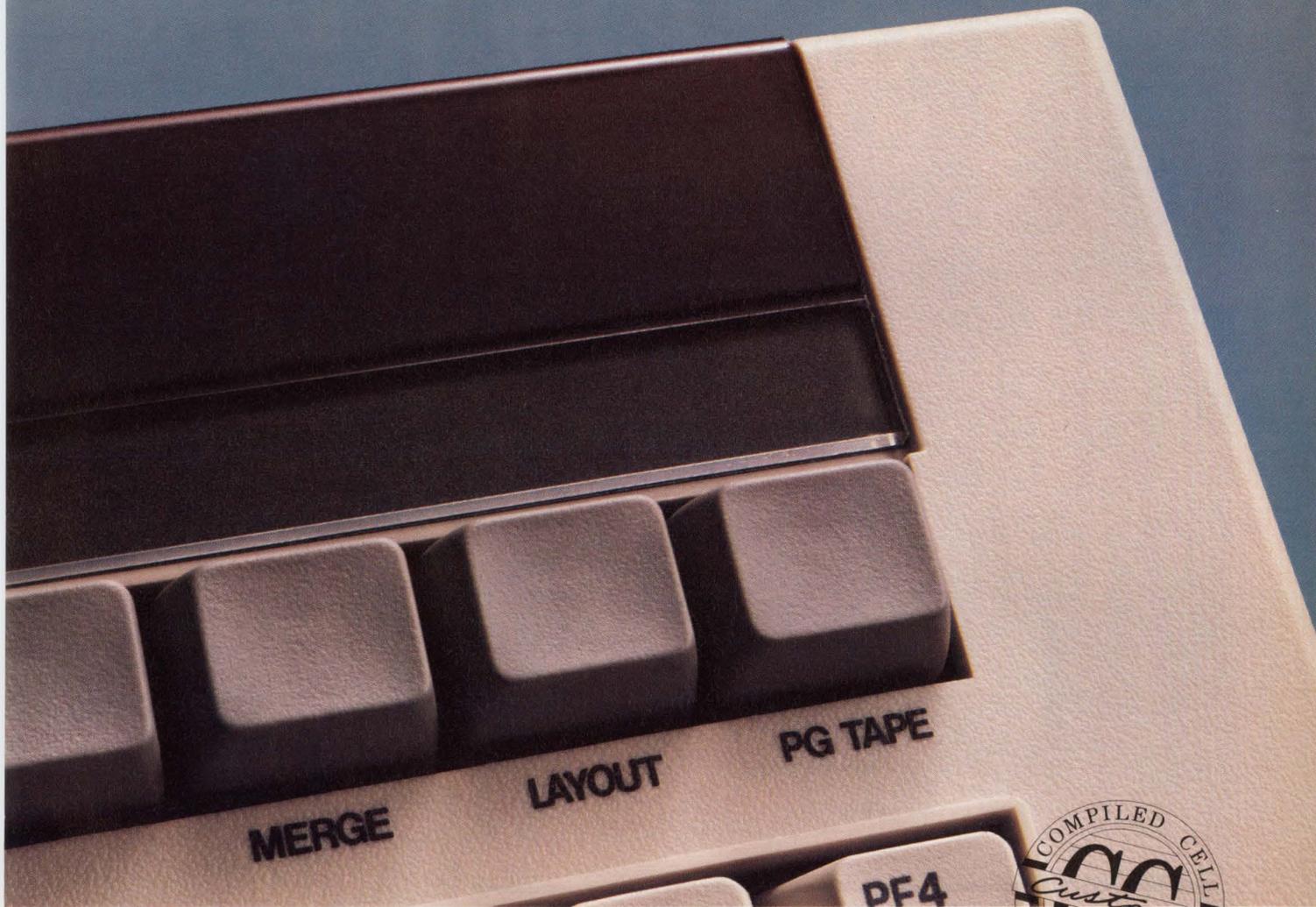
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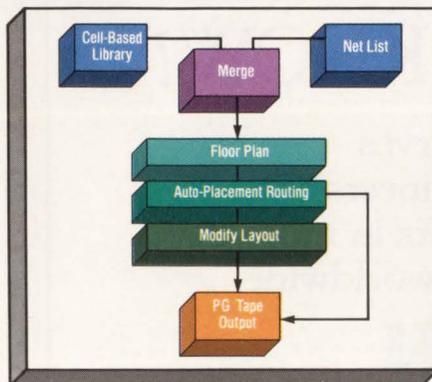
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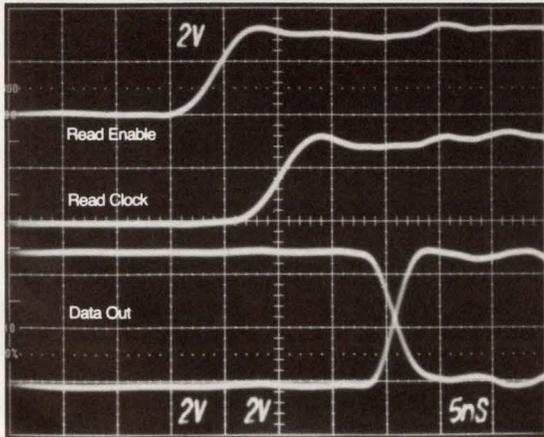
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For high performance like this, timing is everything. With its separate rising edge-triggered read and write clocks, the MK4505 assures that you can transfer data between two totally asynchronous systems with ease. Designed for use in applications where data is moving through the system on the leading edge of a clock, the MK4505 is dedicated to applications like digitized video and audio, image processing, A-to-D and D-to-A conversions, high speed data links, RADAR return sampling and fast bus watching.

The MK4505 is available in two versions: a Master (MK4505M) and a Slave (MK4505S). With the MK4505M, you get all the control signals necessary for reliable full speed, fully asynchronous width and/or depth expansion. Making the MK4505 cascadable to any depth, without a hodgepodge of extra logic taking up valuable space.

The MK4505M also gives you a very special feature not available in any other FIFO—a full complement of status flags, including Output Valid, Empty, Almost Empty, Half Full, Full, Almost Full, and Input Ready.



Actual MK4505 BiPORT FIFO Scope Trace Photograph

Almost Full, Full and Input Ready. So you know how much is—or isn't—available, *before* it's too late.

The Slave, MK4505S with dual write enable and dual read enable inputs, allows width expansion in an instant.

Finally—and even more incredible—is that, for all its high-performance capabilities, the MK4505 fits into one board-saving ultrathin 300 mil DIP. Proof that big things really do come in very small packages.

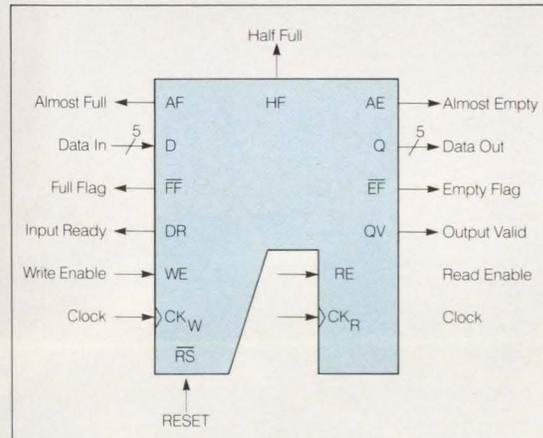
Sync again, IDT.

Of course, we don't claim to be the only FIFO manufacturer around. Just the best. And we've got the black-and-white facts to prove it.

	MK4505-25	IDT 7202-35
Cycle time	40 MHz	22 MHz
Access time	15ns	35ns
Almost full & Almost empty status flags	Yes	No
Free-running clock inputs	Yes	No
Separate read & write enable inputs	Yes	No
Package	300 Mil DIP	600 Mil DIP
Depth	1024	1024
Width	5-bit	9-bit
Width & depth expandable with no support logic	Yes	No
Fully authorized second sourcing	Yes	No

So if you're looking for a superfast, super-smart FIFO solution, get it in sync. With the MK4505 BiPORT FIFO from Thomson-Mostek. The people who also bring you the world's densest FIFO—the MK4503.

For more information on the MK4505, call or write Thomson Components-Mostek Corporation, 1310 Electronics Drive, Carrollton, Texas 75006, MS2205, 214/466-6836.



MK4505M Logic Symbol Diagram

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In addition to FIFO memories, Thomson-Mostek manufactures a broad selection of MOS and bipolar devices for both commercial and military applications: microcomponents, ASIC, memories, telecom/datacom and linear circuits as well as Discrete, RF and microwave transistors and passive components. BiPORT is a trademark of Thomson Components-Mostek Corp.

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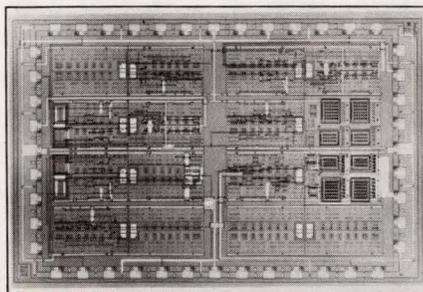
Semicustom linear arrays feature high-frequency vertical pnp transistors

Because they incorporate vertical pnp transistors, the ALA semicustom linear arrays offer better high-frequency performance and faster speeds than similar arrays that have lateral pnp transistors. All semicustom linear chips use vertical npn transistors, but most chips also use lateral pnp transistors, which have far poorer high-frequency performance than do their vertical npn counterparts. Typically, the gain-bandwidth product (f_T) of lateral pnp transistors is lower than that of vertical npn transistors by as much as two orders of magnitude—4 MHz and 400 MHz are common values for lateral pnp and vertical npn transistors, respectively.

The ALA arrays, however, are fabricated in what the vendor calls a "complementary bipolar integrated circuit" (CBIC) process, which gives the npn and pnp transistors similar characteristics. These arrays are also designed on a grid system, which provides easier interconnections for the IC designer.

At present, this semicustom-array family has three members: the ALA200 UHF (12V) array, the ALA300/301 HV (90V) array, and the ALA400 general-purpose (30V) array. All three consist of uncommitted vertical npn and pnp transistors, MOS capacitors, and diffused and/or ion-implanted resistors. All the inputs and outputs have ESD protection. The company plans to introduce a fourth array, which will combine analog and digital functions, later this year.

The ALA200 UHF array is the family's highest performance member; it provides an f_T of 4 GHz for the npn transistors and 2.5 GHz for the pnp transistors. The vendor typically fabricates the array with



The ALA200 UHF linear array is divided into 12 modules: eight standard, two power, one input, and one trim. Each standard module contains 12 npn and seven pnp transistors, as well as 84 implanted resistors. The other modules contain similar quantities of components, which vary slightly for each module. The array is laid out on a grid system, which facilitates the interconnection of components.

dual-layer or thick metal, but single-layer metal is available by special request. The top and bottom metal layers have a sheet resistance of $<0.03\Omega/\text{square}$ and a current-carrying capacity of 2 mA per micron of metal width. The standard 10- μm top and 6- μm bottom metal lines are capable of carrying a maximum of 20 mA and 12 mA dc, respectively. For applications in which higher dc currents must be carried, a thick gold layer is available with a sheet resistance of less than $0.01\Omega/\text{square}$ and a current-carrying capacity of 14 mA per micron of metal width.

The chip is divided into 12 modules: eight standard, two power, one input, and one trim. All 12 modules are symmetrically located within the array, so you can lay them out easily. Because the modules are on a regular grid system, you interconnect components by drawing lines on a clearly defined grid marked on a layout sheet.

The ALA200 contains a total of 133 npn transistors, 85 pnp transistors, 982 boron-implanted resistors, and 22 capacitors. The individual

resistor values vary from 50Ω to as much as $6\text{ k}\Omega$. The values of all the capacitors but two are programmable from 1 to 5 pF; the two exceptions, which are located on the perimeter of the chip, are fixed at 150 pF.

The ALA300/301 are higher-voltage chips with a 90V breakdown capability. The single-module version (ALA300) consists of 13 vertical npn and 15 vertical pnp transistors, three 6-pF capacitors, and 108 resistors located in 1k diffused and 10k ion-implanted resistor banks. The quad version (ALA301) has four times the number of components as the ALA300, but is otherwise identical. The typical f_T is 350 MHz for the npn transistors and 300 MHz for the pnp transistors.

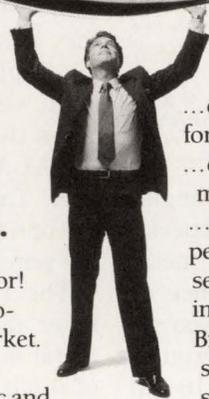
The interconnections are dual-layer metal. The top and bottom metal layers have sheet resistances of $0.03\Omega/\text{square}$ and $1.0\Omega/\text{square}$, and current-carrying capacities of 2 mA and 60 μA per micron of metal width, respectively. For higher current-carrying capacity, you can obtain thick metal interconnections that have a sheet resistance of less than $0.003\Omega/\text{square}$ and a current-carrying capacity of 20 mA per micron of metal width.

The third member of the family, the ALA400, is a general-purpose array with a 30V breakdown voltage. Its typical f_T is 350 MHz for the npn transistors and 300 MHz for the pnp transistors. The ALA400 is divided into 16 modules—12 standard, two power, and two JFET modules. Its npn transistors total 100, including four power types capable of handling $>70\text{ mA}$. The array also has a total of 100 pnp transistors, including four power types, four JFETs, and 14 capacitors. The resistor com-



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and a current-carrying capacity of 2
mA per micron of metal width. The
bottom metal layer has a sheet resis-
tance of $1\Omega/\text{square}$ and a current-
carrying capacity of $200\ \mu\text{A}$ per
micron of metal width. You can ob-
tain a thick-metal interconnect that
has a sheet resistance of $0.003\Omega/\text{square}$
and a current-carrying ca-
pacity of 20 mA per micron of metal
width.

Along with the semicustom linear
arrays, the vendor offers a library of
macrocells. This library includes op
amps, comparators, output buffers,
and voltage and current references.
The vendor offers the arrays in a
number of different packages, in-
cluding plastic and ceramic DIPs,
plastic SOJ and SOIC packages, and
plastic and ceramic chip carriers.

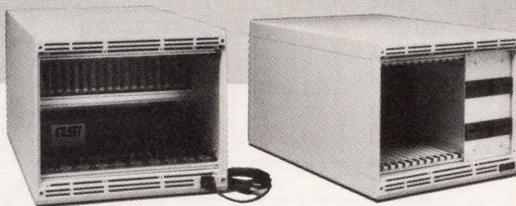
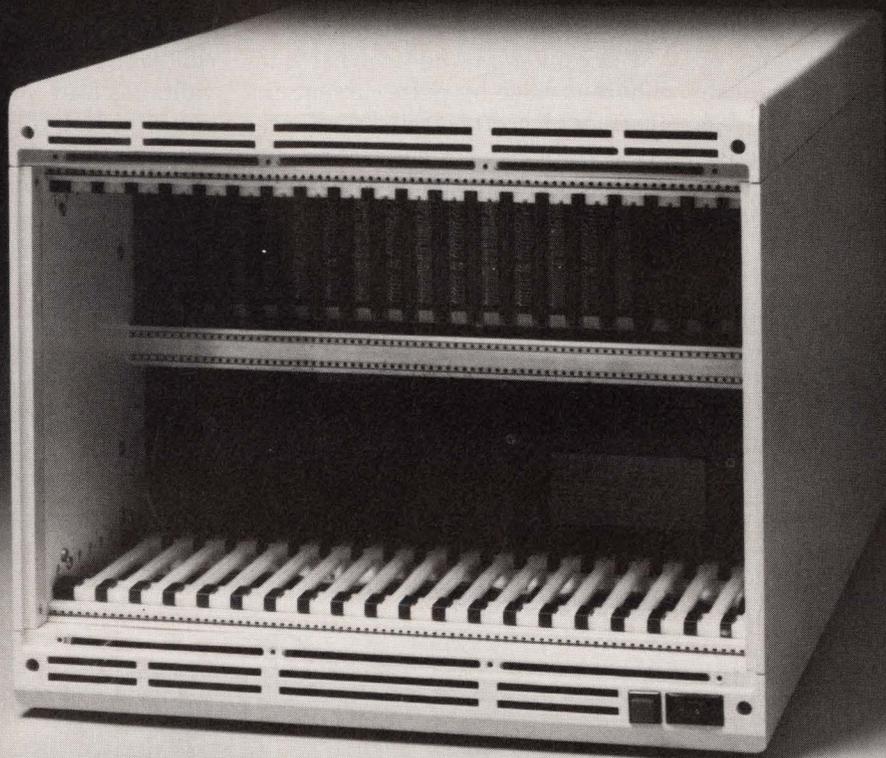
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sign-rule check and conductivity
verification, the generation of a
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either two dc-tested wafers or 25
dc-tested packaged parts. The com-
pany also quotes lower NRE
charges for customers that don't re-
quire all these services. Unit costs
for the chips (in quantities of 10,000)
are ALA200, \$14.35; ALA300,
\$1.40; ALA301, \$4.65; ALA400,
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Switching-regulator IC offers three methods of current-mode control

You can connect the CS-320/321 current-mode control ICs in any of three configurations that sense peak inductor current. The CS-320 has an output stage that is active high, and the CS-321 has an output stage that is active low. At present, they are the only current-mode control ICs that provide hysteretic and constant-off time control, as well as the less-precise constant-frequency type of control. (It's likely, however, that at least one other manufacturer is developing new current-mode ICs, which may be announced by

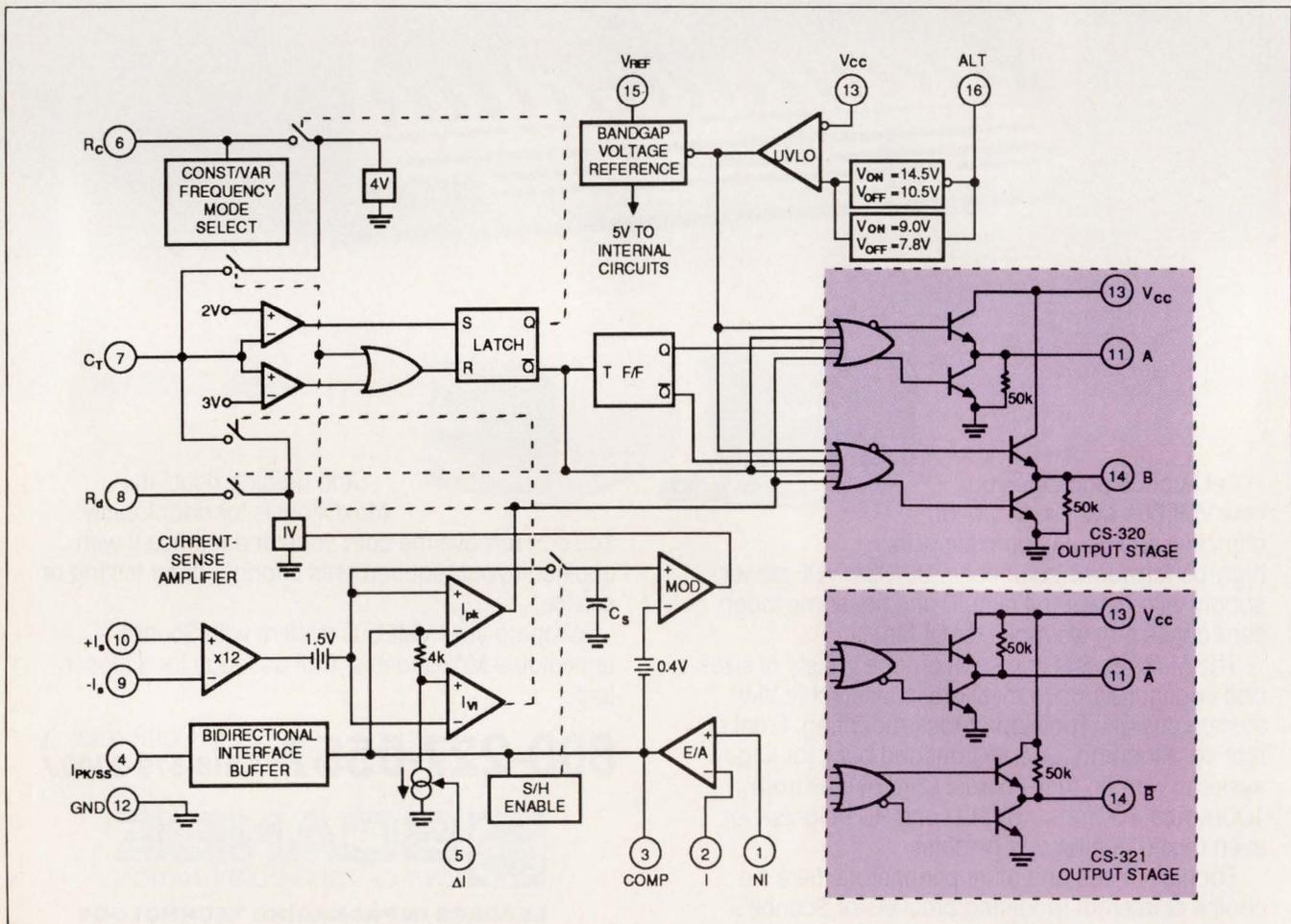
press time.)

Current-mode control provides inherent pulse-by-pulse current limiting, which effectively eliminates the 90° phase lag associated with the filter inductor or energy-storage inductor, and which makes it easy to apply output-current feed-forward information to quickly correct load transients.

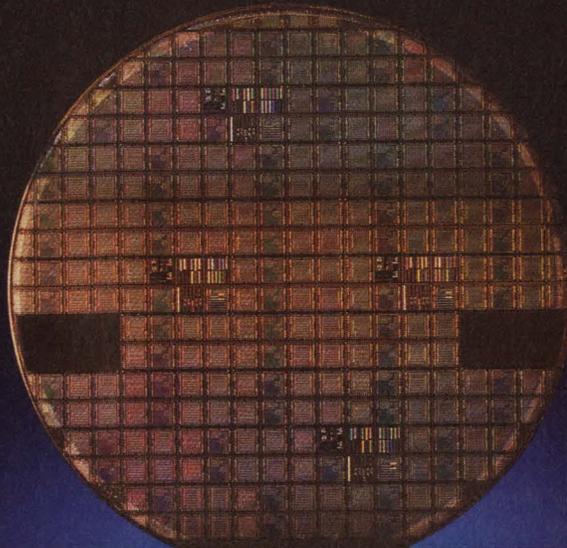
ICs dedicated to current-mode control of switching power supplies have been available for the past two or three years in the form of fixed-frequency types, such as Unitrode's

1842 Series. These current-mode control circuits offer significant advantages over voltage-mode control circuits, but your application may determine which method you choose. There are actually five different methods of current-mode control: hysteresis, constant-off time, constant frequency (with turn-on at clock time), constant-on time, and constant frequency (with turn-off at clock time).

Each of these methods involves the sensing of the inductor current. The first method senses both the



This power-supply-control IC provides three current-mode options: hysteretic, constant-off-time, and constant-frequency control. The IC's high-current totem-pole output is suitable for driving power MOSFETs.



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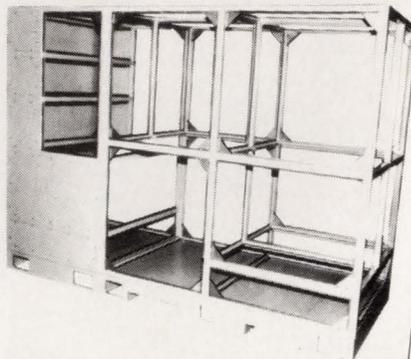
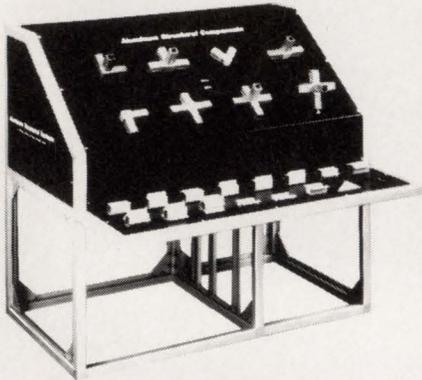
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UPDATE

peak and the valley currents. The second and third methods sense only the peak inductor current, and the fourth and fifth methods sense only the valley current.

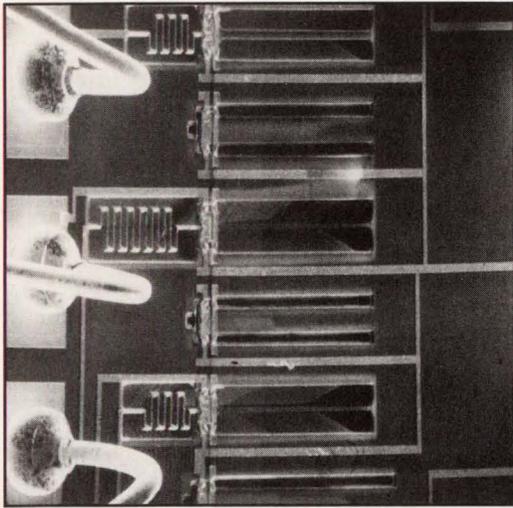
You can operate the CS-320/321 ICs at frequencies as high as 1 MHz. They provide a selectable UVLO (undervoltage-lockout) function that is optimized for either off-line bootstrap operation or low-voltage (eg, battery) dc inputs; the selectable start/stop thresholds are 14.5V/10.5V and 9.0V/7.8V, respectively. The ICs prevent runaway current conditions during overload by continually extending the off time. Their high-current totem-pole output stages allow them to drive power MOSFETs, and you can use their high-gain current-sense amplifiers to interface with current-sensing MOSFETs in which a few of the internal cells are brought out to a pin.

The ICs also feature a 5V band-gap reference that's trimmed to either 1% (industrial grades) or 2% (commercial grades); a precision timer circuit that lets you select maximum on/off times for any of the three modes of operation; and a synchronization capability, which lets you connect two or more controllers in parallel.

In 16-pin plastic DIPs, the CS-320/321 ICs cost \$3.47 (100) and \$2.87 (1000). Samples and small quantities are available from stock to 30 days. Production quantities will be available in September or October.—*Dave Pryce*

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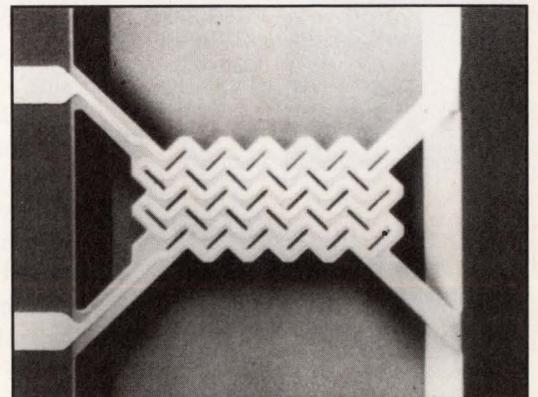
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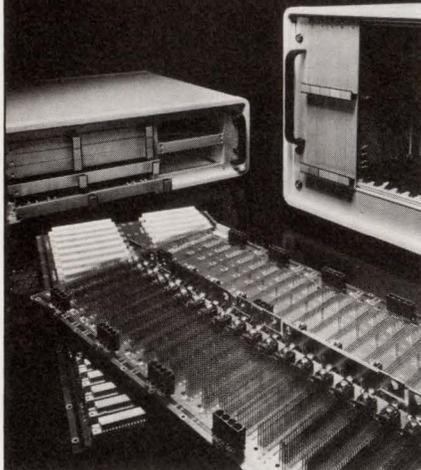


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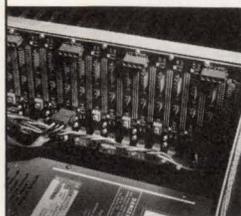
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PRODUCT UPDATE

Autorouter eliminates restrictions on grid size



The Design Automation Series comprises the DA1000 basic workstation, the DA3000 intermediate-range workstation, and the DA5000 high-end workstation. The DA1000 is a complete design station that comes with interactive graphics; component-placement tools; a hardware, 100% autorouting package for multilayer boards; and postprocessing software.

The DA3000 has the same capabilities, but adds increased graphics performance, more autorouting options, and a twofold overall improvement in performance over that of the DA1000. The top-of-the-line DA5000 offers all the features of the DA3000 and also comes with the variable-grid autorouter and a RISC-based hardware autorouting accelerator.

The DA1000 costs \$65,000; the DA3000, \$90,000; and the DA5000, \$120,000. The variable-grid routing package is a \$5000 option for the DA1000 and DA3000 workstations.

—Jim Wiegand

Calay Systems Inc, 2698 White Rd, Irvine, CA 92714. Phone (714) 863-1700. TLX 6711321.

Circle No 737

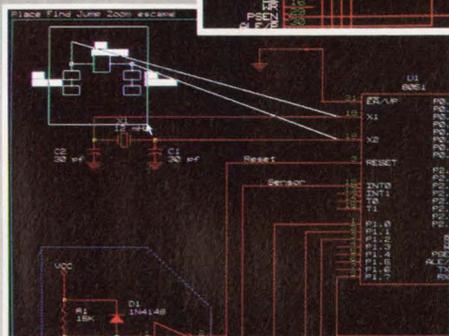
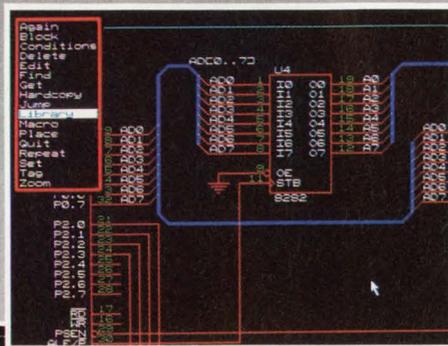
To lay out very dense pc boards, as well as those that include SMDs or other new-technology devices having nonstandard lead spacing, you can use the variable-grid router available for Calay's Design Automation workstations. This hardware router eliminates restrictions on grid size, letting you select grids of any resolution.

When you use the Design Automation family of pc-board-layout workstations in conjunction with the vendor's board-layout software packages and variable-grid autorouter, you can achieve 100% hardware autorouting of your pc boards. The variable-grid router eliminates restrictions on grid size, letting you select grids of any resolution. This feature is an important one for the layout of pc-board designs that include SMDs or other new-technology components having nonstandard lead spacing. In addition, because the router allows you to define extremely fine grid resolutions, you can use it to lay out very dense pc boards.

Schematic Capture

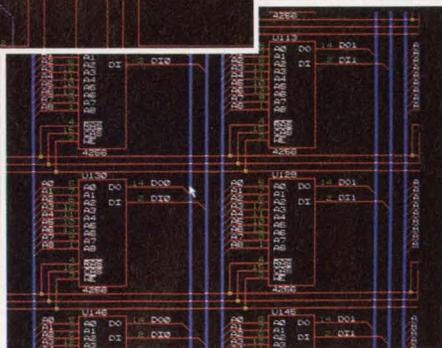
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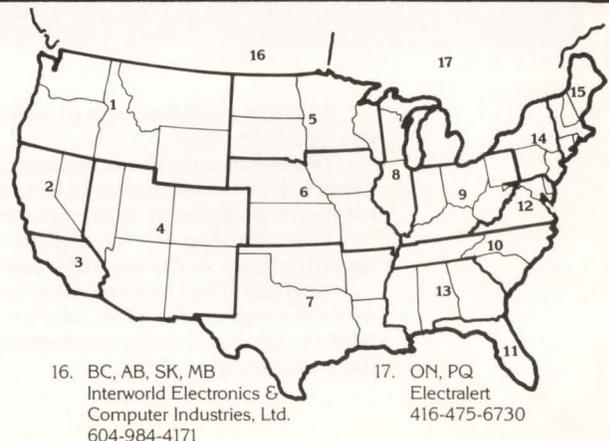
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Q: In which direction (A or B) is the bus heading when it's going forward? (This isn't a trick question.)



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And now that the industry has moved to more complex mixed-signal devices, we've answered with the LTX Ninety: an even more sophisticated version of the LTX77—the industry standard.



THE LTX *Ninety*

READER'S CHOICE



Michael A. Steuben © Discover Magazine 1/87, Time Inc.

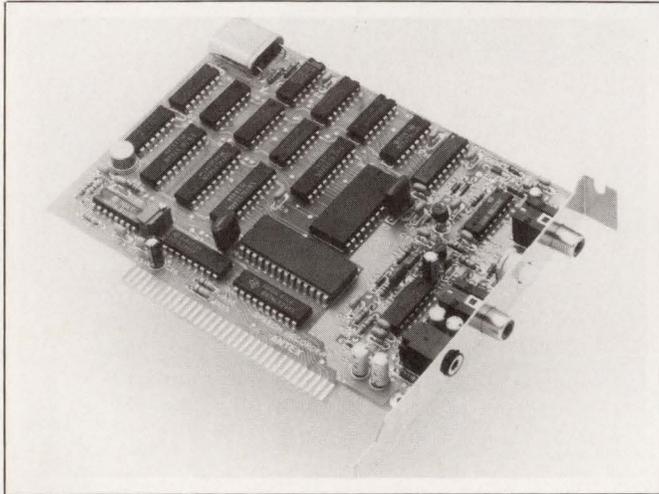
The LTX Ninety offers the best price performance available today, and is compatible with the LTX77. Like every LTX system, the Ninety is ultra fast, accurate and efficient—from program preparation to final test. Expanded memory means long test programs are no problem. And the list of add-ons goes on and on, including ISDN capability.

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READERS' CHOICE

Of all the new products covered in EDN's April 15, 1987, issue, the ones reprinted here generated the most reader requests for additional information. If you missed them the first time, find out what makes them special: Just circle the appropriate numbers on the Information Retrieval Service card, or refer to the indicated pages in our April 15, 1987, issue.

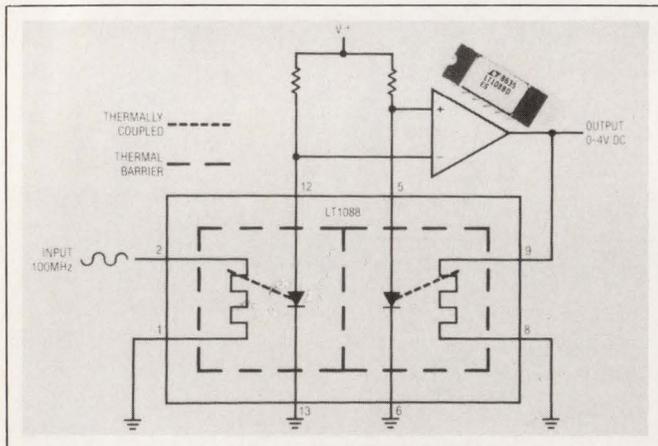


▲ VOICE PROCESSOR

The VP 600 voice processor converts audio input into a digital format for storage on a computer disk (pg 255).

Antex Electronics Corp.

Circle No 604



▲ RMS-TO-DC CONVERTER

The LT1088 is a thermal-type rms-to-dc converter that comes in a 14-pin, side-brazed DIP, assembled with proprietary techniques to achieve the required thermal characteristics (pg 244).

Linear Technology Corp.

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OPTICAL SENSOR

The SFH 910 slotted optical-sensor module has a GaAlAs infrared source and a photodiode detector separated by a 3.2-mm slot. It is suited for use in incremental angular resolvers or linear motion detectors (pg 228).

Siemens AG.

Circle No 601

Siemens Components Inc.

Circle No 602



▲ EMI PROBES

The 7405 probe set, comprising three loop probes, a ball probe, and a stub probe, detects E and H fields separately (pg 270).

EMCO.

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FEEDBACK ANALYZER

The Classical Controls Analysis Program (CCAP) is an interactive, menu-driven program that helps you analyze and design feedback-control systems (pg 280).

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PicoLogic™ Digital ICs	Part No.	Speed	Availability	PicoLogic™ Digital ICs	Part No	Speed	Availability
Gates				Arithmetic Operators			
Quad 3 Input NOR	10G000A	290 ps	In Stock	Dual 9-Bit Parity Generator/Checker and 8-Bit Equivalence Checker	10G045	800 ps	In Stock
Quad 2 Input NOR	10G001	290 ps	In Stock	Ultra-High Speed 4-Bit Adder	10G100	800 ps	In Stock
Quad Differential XOR/XNOR and Line Receiver	10G002	1.8 GHz	In Stock	Ultra-High Speed Carry Lookahead 4-Bit ALU (10181 ECL equivalent)	10G101	500 ps	In Stock
5, 4, 3, 2/3, 2 Input AO/AOI	10G003	600 ps	4 weeks ARO		10G181	2 ns	6 weeks ARO
Drivers/Receivers/Comparators				Monolithic FET and Diode Arrays			
Dual Complementary Driver/Comparator	10G012B	1.8 GHz	In Stock	15 mA Diode Array	16G010	—	In Stock
Dual 4:1 Fanout Buffer	10G011B	700 ps	In Stock	100 mA Diode Array	16G011	—	In Stock
Dual Differential MUXed Fanout Buffer	10G010	1.5 GHz	In Stock	Single Gate FET Array	16G020	15 GHz	In Stock
				Dual Gate FET Array	16G021	15 GHz	In Stock
Flip Flops and Registers				NanoRam™ Memory			
Dual Precision D Flip Flop	10G021A	2.7 GHz	In Stock	256 x 4-Bit Pipelined Static RAM	12G014	3 ns cycle time	Production Sampling
Quad MUXed Input D Flip Flop	10G023	2 GHz	In Stock				
Quad XOR Input Flip Flop	10G024	2 GHz	In Stock	Communication Products			
Octal Register/Shift Register and PN Code Generator	10G022	1.5 GHz	In Stock	8:1 Time Division MUX	10G040	1.5 Gb/s	In Stock
Register Files				1:8 Time Division DEMUX	10G041	1.5 Gb/s	In Stock
16 x 4 3-Port Register File	10G030	1 ns	6 weeks ARO	Clock and Data Recovery Circuit	16G040	2.0 Gb/s	In Stock
Multiplexers/Demultiplexers				16G040 Demo/OEM Board	90G040	—	In Stock
Quad 4:1 or Dual 8:1 MUX	10G046	600 ps	In Stock	Phase Frequency Comparator	16G044	1.0 GHz	In Stock
Quad 2:1 MUX	10G004	1.8 GHz	In Stock				
3:8 or Dual 2:4 Decoder/DEMUX	10G044	700 ps	In Stock	ASIC Products			
Counters/Prescalers				SC-1 Standard Cell Library Rundry Program	80 GSC1	—	Available Available
2-Stage Divider	10G060	2.5 GHz	In Stock				
4-Bit Synchronous Programmable Counter	10G061	1.6 GHz	In Stock	Prototyping & Support Products			
7-Stage Counter/Divider	10G065	3.0 GHz	In Stock	Universal Prototype Kit	90GUPK	—	In Stock
Variable Modulus Divider	10G070	2.0 GHz	In Stock	Universal Prototype Board	90GUPB	—	In Stock
				High Speed Socket (40L Package)	90GSKT-40L	—	In Stock

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LEADTIME INDEX

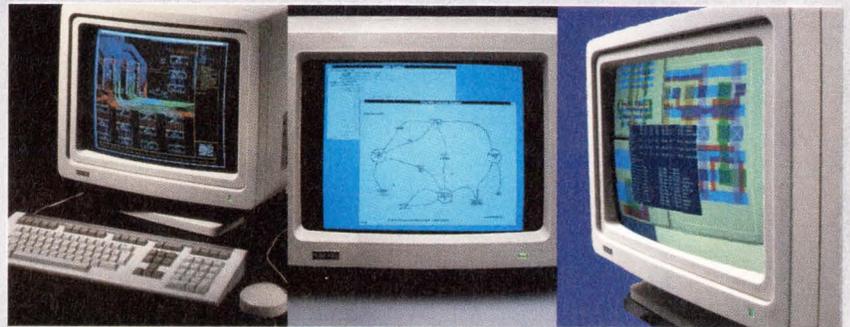
Percentage of respondents

ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Last month's average (weeks)	Average (weeks)
TRANSFORMERS								
Toroidal	11	11	22	56	0	0	10.7	7.6
Pot-Core	0	8	59	25	0	8	11.4	7.7
Laminate (power)	6	12	47	35	0	0	9.6	5.7
CONNECTORS								
Military panel	0	12	25	50	13	0	13.3	7.5
Flat/Cable	10	48	29	14	0	0	5.9	8.6
Multipin circular	6	38	19	25	12	0	9.7	10.1
PC	22	28	28	22	0	0	6.5	4.9
RF/Coaxial	9	46	18	27	0	0	7.1	5.0
Socket	21	26	37	16	0	0	6.2	4.1
Terminal blocks	18	45	23	14	0	0	5.3	3.0
Edge card	20	7	40	27	6	0	9.2	5.0
Subminiature	25	31	19	25	0	0	6.3	4.2
Rack & panel	18	27	28	27	0	0	7.2	4.3
Power	8	20	8	64	0	0	11.1	3.9
PRINTED CIRCUIT BOARDS								
Single-sided	0	50	39	11	0	0	6.3	3.9
Double-sided	0	38	54	8	0	0	6.8	5.7
Multilayer	0	25	50	25	0	0	8.6	7.2
Prototype	0	82	6	12	0	0	4.8	3.2
RESISTORS								
Carbon film	57	5	19	19	0	0	4.6	2.8
Carbon composition	41	5	27	27	0	0	6.5	3.1
Metal film	43	9	29	19	0	0	5.5	3.9
Metal oxide	21	36	21	22	0	0	6.1	3.7
Wirewound	22	22	30	26	0	0	7.1	5.1
Potentiometers	25	25	29	13	4	4	7.4	5.5
Networks	18	27	32	18	5	0	7.3	5.7
FUSES								
	40	32	20	8	0	0	3.8	2.6
SWITCHES								
Pushbutton	8	38	29	25	0	0	7.3	6.0
Rotary	7	31	31	31	0	0	8.3	6.2
Rocker	11	44	28	17	0	0	6.1	4.1
Thumbwheel	13	20	33	34	0	0	8.4	6.0
Snap action	7	57	14	22	0	0	6.2	7.3
Momentary	12	44	13	31	0	0	7.2	7.7
Dual in-line	17	33	25	25	0	0	6.9	7.9
WIRE AND CABLE								
Coaxial	34	40	13	13	0	0	4.3	4.0
Flat ribbon	26	56	11	7	0	0	3.7	3.1
Multiconductor	22	34	22	22	0	0	6.2	3.6
Hookup	50	30	10	10	0	0	3.3	1.5
Wire wrap	35	35	18	12	0	0	4.3	1.3
Power cords	33	33	17	17	0	0	4.9	4.7
Other	14	14	29	29	14	0	10.8	8.0
POWER SUPPLIES								
Switching	6	13	31	31	19	0	12.5	6.8
Linear	8	23	38	23	8	0	9.3	6.0
CIRCUIT BREAKERS								
	26	42	16	16	0	0	5.0	6.4
HEAT SINKS								
	21	46	16	17	0	0	5.3	2.7

ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Last month's average (weeks)	Average (weeks)
RELAYS								
General purpose	18	36	32	14	0	0	5.8	4.6
PC board	6	35	35	24	0	0	7.5	6.2
Dry reed	10	30	30	30	0	0	8.0	6.4
Mercury	17	17	33	33	0	0	8.3	6.3
Solid state	6	27	40	27	0	0	8.1	6.6
DISCRETE SEMICONDUCTORS								
Diode	22	45	11	22	0	0	5.7	3.8
Zener	23	41	13	23	0	0	5.8	4.7
Thyristor	8	23	38	31	0	0	8.5	6.1
Small signal transistor	24	33	19	19	5	0	6.7	5.0
FET, MOS	14	36	14	29	7	0	8.5	5.7
Power, bipolar	12	29	29	30	0	0	7.8	4.2
INTEGRATED CIRCUITS, DIGITAL								
CMOS	16	24	28	32	0	0	7.9	4.9
TTL	23	23	36	18	0	0	6.4	4.1
LS	27	23	32	18	0	0	6.1	3.8
INTEGRATED CIRCUITS, LINEAR								
Communication/circuit	0	27	46	27	0	0	8.7	6.9
OP amplifier	18	18	35	29	0	0	7.9	6.0
Voltage regulator	25	30	25	20	0	0	6.0	5.3
MEMORY CIRCUITS								
RAM 16K	20	27	27	26	0	0	7.1	3.9
RAM 64K	22	22	28	28	0	0	7.2	4.5
RAM 256K	16	31	37	16	0	0	6.3	4.2
ROM/PROM	11	45	22	22	0	0	6.6	3.5
EPROM	14	38	14	34	0	0	7.5	5.2
EEPROM	14	43	21	22	0	0	6.3	4.4
DISPLAYS								
Panel meters	0	31	46	23	0	0	8.2	6.5
Fluorescent	9	18	36	37	0	0	9.1	8.4
Incandescent	11	33	22	34	0	0	7.9	6.8
LED	13	31	30	26	0	0	7.4	5.5
Liquid crystal	0	21	50	29	0	0	9.1	6.8
MICROPROCESSOR ICs								
8-bit	19	19	25	31	6	0	9.0	4.3
16-bit	14	33	33	20	0	0	6.8	3.8
FUNCTION PACKAGES								
Amplifier	22	33	11	34	0	0	7.1	5.8
Converter, analog to digital	0	27	27	46	0	0	10.0	6.3
Converter, digital to analog	0	20	40	40	0	0	10.0	7.2
LINE FILTERS								
	0	43	21	36	0	0	8.5	5.1
CAPACITORS								
Ceramic	22	35	26	17	0	0	5.8	3.7
Ceramic monolithic	21	29	21	29	0	0	7.0	3.7
Ceramic disc	11	55	17	17	0	0	5.6	3.2
Film	10	21	27	37	5	0	9.8	3.9
Electrolytic	10	17	50	23	0	0	8.1	5.4
Tantalum	9	32	36	23	0	0	7.4	4.5
INDUCTORS								
	8	38	23	31	0	0	7.8	6.1

Source: Electronics Purchasing magazine's survey of buyers

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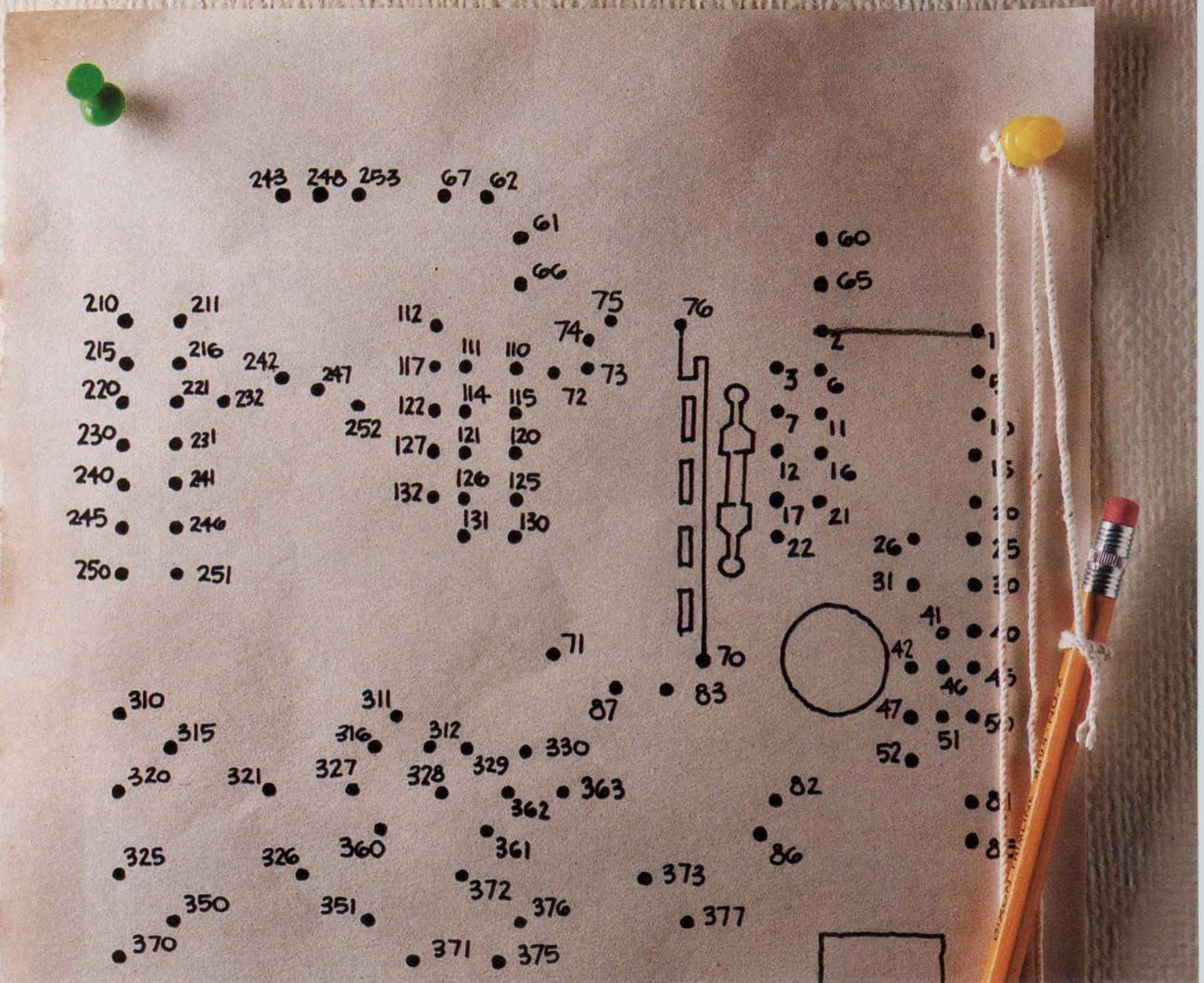
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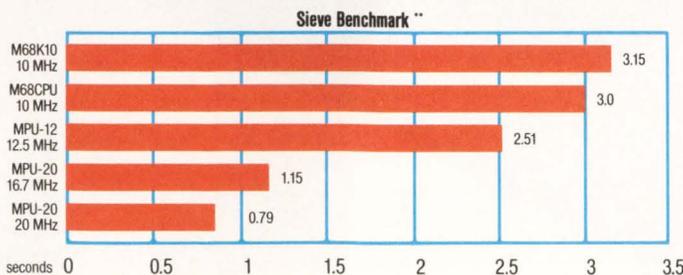
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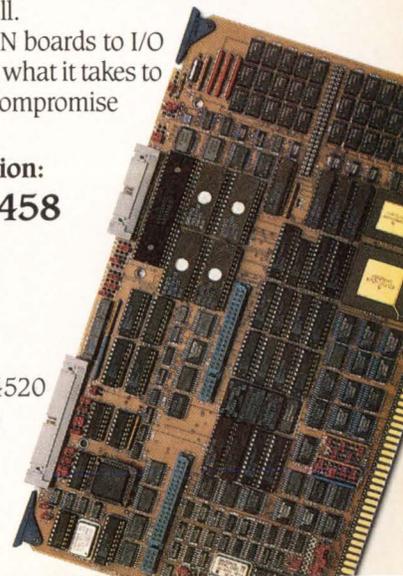
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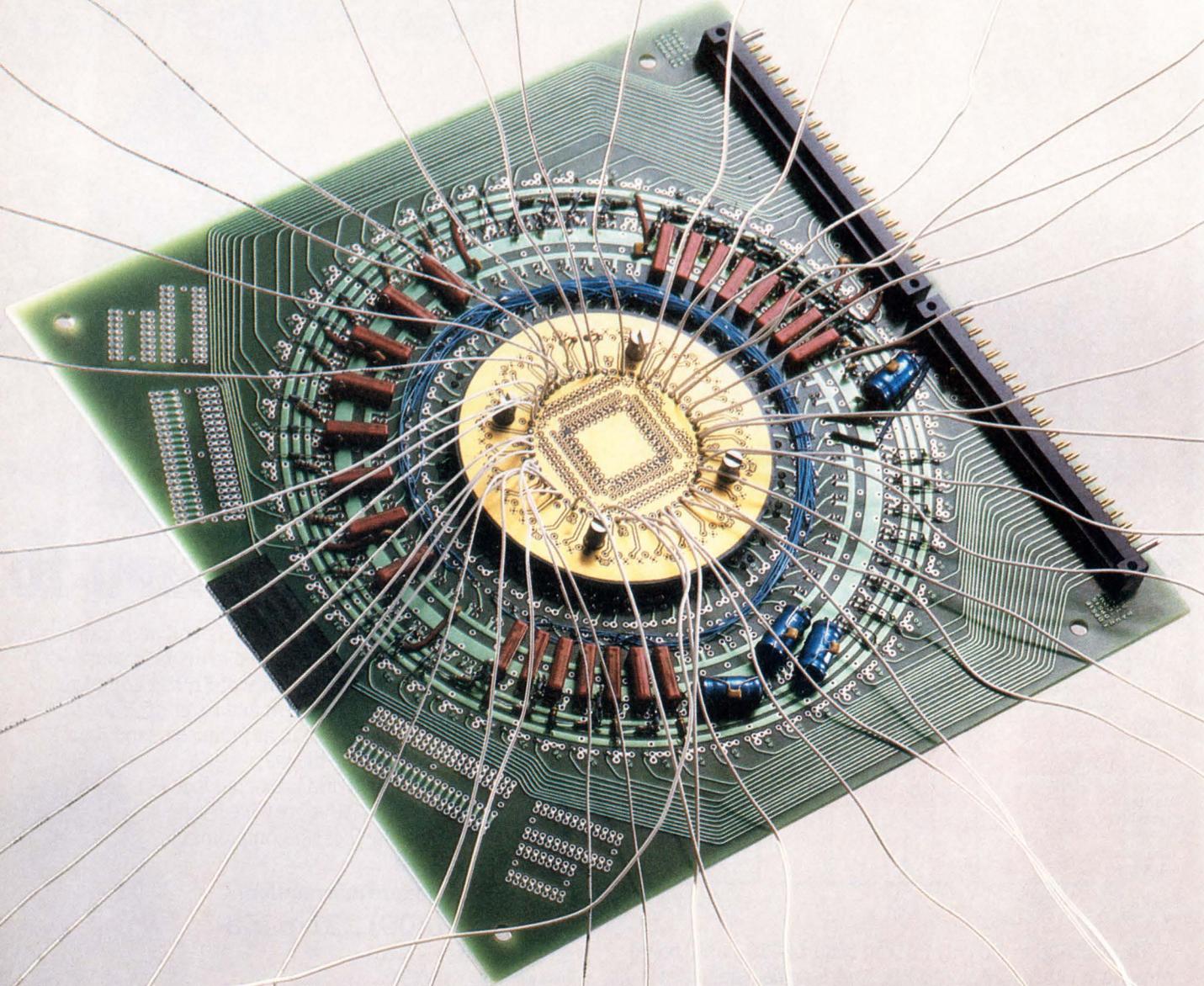
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Setting up the test is easy, too. Cadic test systems accept data directly from your logic simulator. The automatic pattern generation capability of the systems creates test vectors without time-consuming manual entry. Nothing more than a header change is required to download simulator outputs directly to vector file. The STM5100 also verifies timing characteristics and setup and hold times—all through simple menu-driven commands that take minutes to learn.

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STM4100 desktop digital VLSI test system.

For good reason. We've made the DUT-to-test-system connection by mapping the device's pins through software assignment. "SoftWire" is what we call this new approach to VLSI testing, and its advantages are many. First, by eliminating pin-by-pin hardwiring, you sharply reduce setup and programming time: from days to typically less than one hour.

Second, one diskette is all you deal with. Errors are correctable with a simple key-stroke instead of a solder gun. There are no delicate hard-wired test fixtures to store. Loss or damage ceases to be a worry. And you'll never have to chase after a matching test vector diskette again.

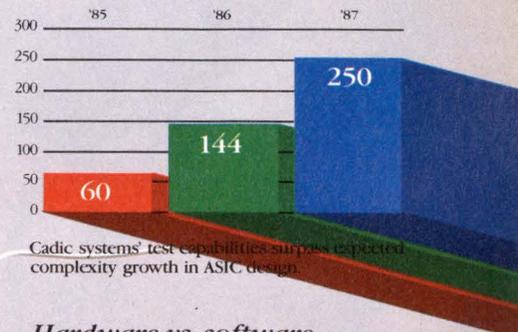
Third, because Cadic's SoftWire takes the place of a test fixture, loading and signal fidelity problems caused by extensive cabling between test system and DUT are eliminated.

Fourth, Cadic software is endlessly flexible. You can program the Cadic systems to test and verify PALS, PLAs, RAMs, ROMs, UARTs, MICROS, 7400s and custom/semi-custom ICs.

A 256-pin powerhouse.

The STM4100 and STM5100 not only test more types of ICs than any other tester; they test more complex ICs. Cadic test systems can test up to 256 pins, with each pin individually addressable. They can be assigned input, output or bidirectional status.

ASIC COMPLEXITY GROWTH.
Typical packaged ASIC pincount, by year.



Cadic systems' test capabilities surpass expected complexity growth in ASIC design.

Hardware vs. software comparison.

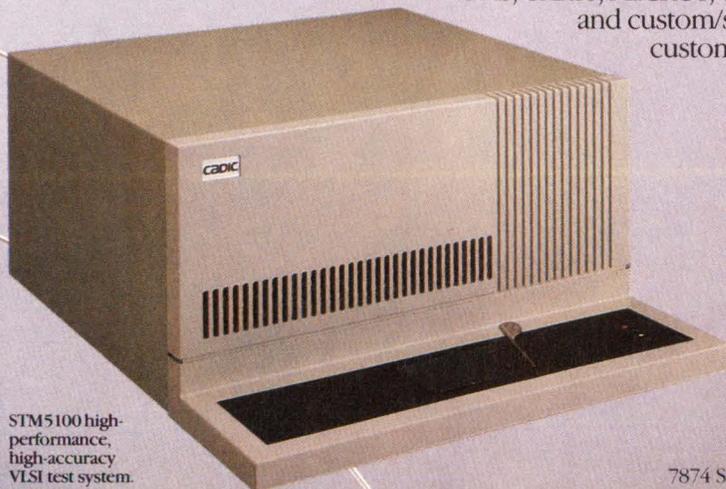
Because verification functions are performed in real time instead of slower post-test comparisons in software, Cadic's hardware comparator means speed. And uncommon power and flexibility.

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How do we know so much about testing VLSI devices? We design them ourselves. In fact, that's exactly what's inside the STM4100 and STM5100: application-specific integrated circuits (ASICs) designed, prototyped and verified by Cadic. They're how we stuffed so much capability into such small packages.

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And that's why more designers, like George Tobias and his team, are calling the one company that can meet all their needs in every ASIC category and can provide the full range of design tools, technical support, manufacturing capacity, and long-term commitment to ensure that those needs will be met on time, on budget, and in spec.

That one company is National Semiconductor.

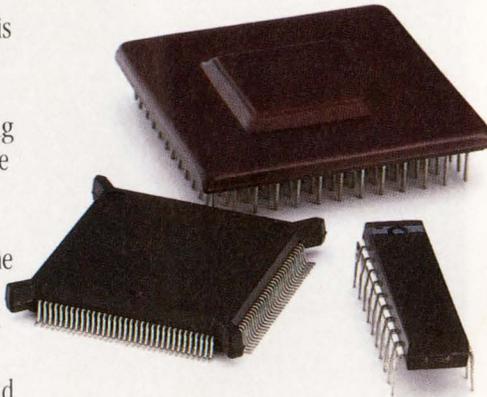
NO ONE OFFERS YOU MORE DESIGN FLEXIBILITY

National is the only company in the industry that can offer you a clear-cut upward-integration path from programmable logic devices to gate arrays to standard cells.

And we're the only company that can offer you a full range of capabilities *within* each of those categories.

Programmable logic. National has one of the most complete PLD listings available. We offer a variety of circuit types in a variety of process technologies, including bipolar, CMOS, and ECL.

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8700 equivalent gates, with higher densities in development, all with sub-nanosecond speeds.

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Or you can simply stay with your gate-array solution indefinitely, knowing that you can "tweak" your design relatively easily to maintain your competitive edge.

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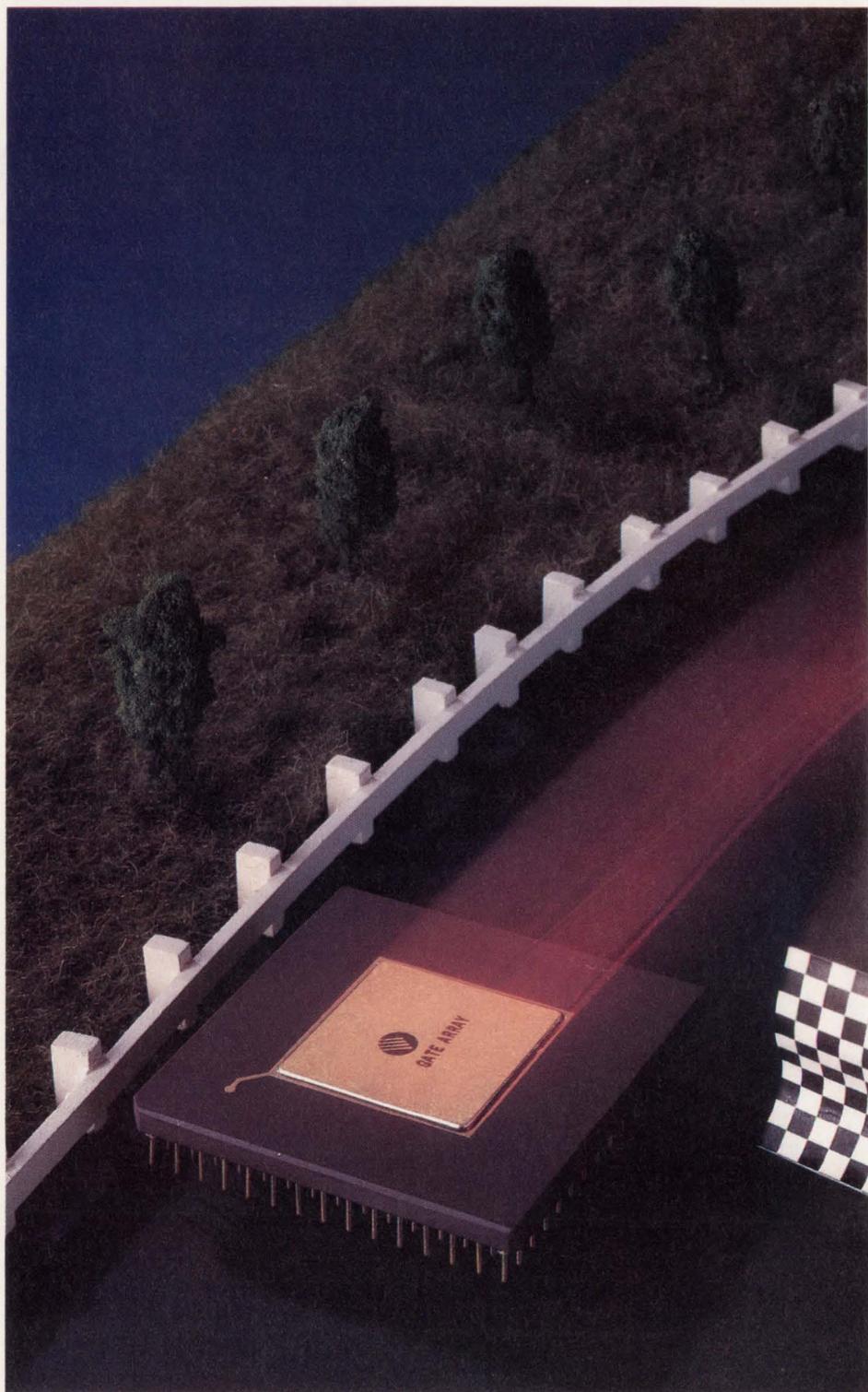
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Special Report

Gate-Array Directory



Gate-array development cycles are speeding up, helping you keep your designs on track and get your products to market first. (Photo courtesy VLSI Technology Inc)

Fast turnaround techniques are making it possible to get your gate-array design to market faster. Furthermore, improvements in device technologies, as well as the relentless march toward increasing gate density, are resulting in faster operating circuitry.

Jim Wiegand, Associate Editor

The triple muses of electronics—smaller, faster, and cheaper—are impelling IC manufacturers to offer devices of higher integration levels and faster operating speeds. Other vendors are using innovative techniques to reduce the time you have to wait to get the devices into your hot little hands. In some cases, you can receive prototype gate arrays three days from the time of design verification.

Time-to-market is more critical today than ever before. The profits to be made from your design are dependent, in part, upon the timeliness of your product introduction, and the lifetime of a product, especially an electronics product, continues to decrease at an accelerated pace. Although the folks in marketing are keen on getting products out the door sooner, they are no more likely to have a product well-defined at design time than they have been in the past.

The process of design is not one of steady, linear progress. You might take a wrong turn, go down a blind alley, and have to back up and start over again. System requirements are fluid; sometimes designs aren't frozen until after months of production. To accommodate this amorphousness, you need to implement design changes as quickly and inexpensively as possible.

Consider, for example, the lessons of μ P-system development. The speed and convenience afforded a designer who uses a μ P development system stems, in large part, from the fact that he can modify and test code on-the-fly. A development system with an in-circuit emulator (ICE) exploits RAM technology to provide the ease of modification and development essential to a timely delivery of operational hardware and software.

In contrast, a poor μ P-development engineer who is anachronistically tied to a mainframe would find that his assembly file is likely to be bumped to the end of the queue so that some bean counter's payroll program can run endlessly. And he's forced to download his code to an EPROM programmer, which may be in a different corner of the building or, worse, in an entirely different building altogether. In such a case, he has to resort to "sneaker-net" to insert his EPROM into the system for testing.

In the evolution of development methods for μ P-based design, storage mediums have changed from

One vendor's goal is to provide 1-hour turnaround times within the next three years.

ROM to EPROM to RAM (in the ICE), and flexibility and productivity have increased dramatically. Changes in ASIC technology have paralleled this evolution. Initially, designers used gate arrays to clean up the ubiquitous glue logic of digital designs. As the arrays' capabilities—in terms of speed, equivalent-gate count, and power consumption—improved, alternative means of design consolidation (programmable logic devices) became useful for lower levels of integration.

You can think of gate arrays as ROM-like devices because, to get the circuitry you desire, you must submit a net list to your gate-array vendor. The vendor

then develops the photo masks that customize his parts to your requirements. Traditionally, once your design has been verified and tested, it can take as long as 10 weeks to get your prototype parts for system testing.

On-the-fly technique aids turnaround

Xilinx Corp, in contrast, blurs the line between PLDs and gate arrays with its family of products. The XC2064 and XC2018 logic-cell arrays offer virtually instantaneous turnaround times. Static-RAM cells accomplish the gate interconnections, allowing you to modify your configuration on-the-fly, much as you

Compiler makes gate-array design manageable

VLSI Technology has developed a high-level silicon compiler that permits the conversion of existing standard cells to gate-array designs. You still get the benefit of the gate array—fewer mask steps—yet you also get the pre-defined functions that are the main advantage of standard-cell designs. The silicon efficiency of

standard cells is sacrificed, however.

Most gate arrays are at or below the 4000-gate level, and because of this relatively low level of complexity, they are designed at the gate level. A designer using a CAE system creates a net list from his gate-level description of the design, and

the net list provides the basis for the gate array.

Macrocells help

Trying gate-level design with gate arrays of more than 4000-gate complexity, however, is unwieldy and much too time-consuming. At this level of integration, macrocells are a necessity. They provide a higher level of functionality, and the

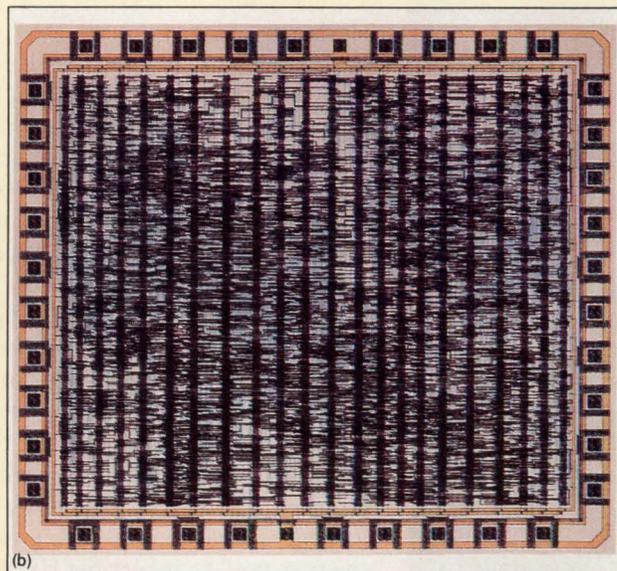
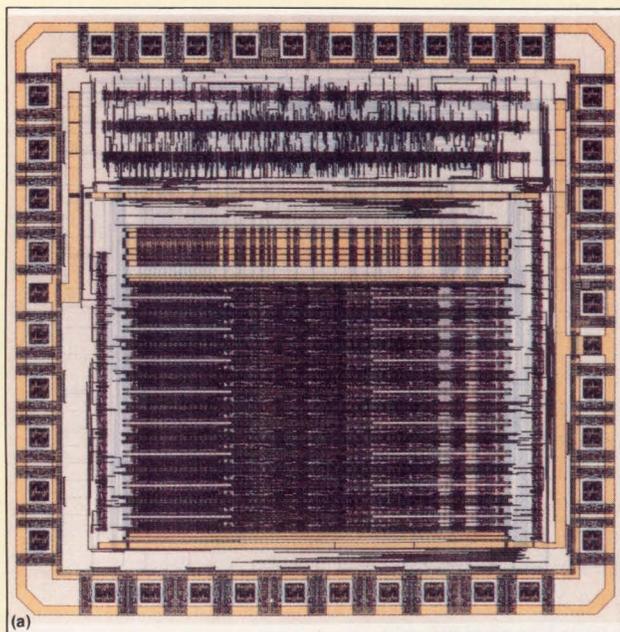


Fig A—All three of these RISC processors are derived from the same user input. They were implemented by VLSI Technology's silicon compiler, which lets you design your ICs in a technology-independent fashion: You can make the choice to use cell-based (a), standard-cell (b), or compacted (c) arrays at the end of the design cycle.

would when using an in-circuit emulator for μ P development. If you want the added development capabilities of an actual in-circuit emulator, you can buy one from Xilinx.

A major drawback of the parts, when compared with other gate arrays, is their capacity. The XC2064 and XC2018 have respective capacities of 1200 and 1800 equivalent 2-input gates. (They specify a flip-flop toggle frequency as high as 70 MHz max.) Other arrays are touting capacities nearly two orders of magnitude greater than these parts. However, if your application doesn't warrant such enormous capacities or need the

faster speed that these other parts can offer, and if you can easily download a program into these volatile storage devices within your system, then the Xilinx parts are certainly a viable option. Moreover, you can expect upcoming devices from Xilinx that will have capacities extended several times over.

Vaporize those connections

Laserpath uses another innovative approach to lessen the turnaround time for its ASICs. The parts start off as fully interconnected gate arrays, and the vendor selectively disconnects the gates using lasers to form

gate-level design is already provided for you.

At even higher levels of integration—10,000 gates and more—manufacturers have different strategies to make the design effort more manageable. VLSI Technology's silicon compiler creates functional blocks, which are equivalent in function but

can vary in form. The compiler takes into account device area, critical-path routing, and required functionality, and it then produces a net list for the gate array.

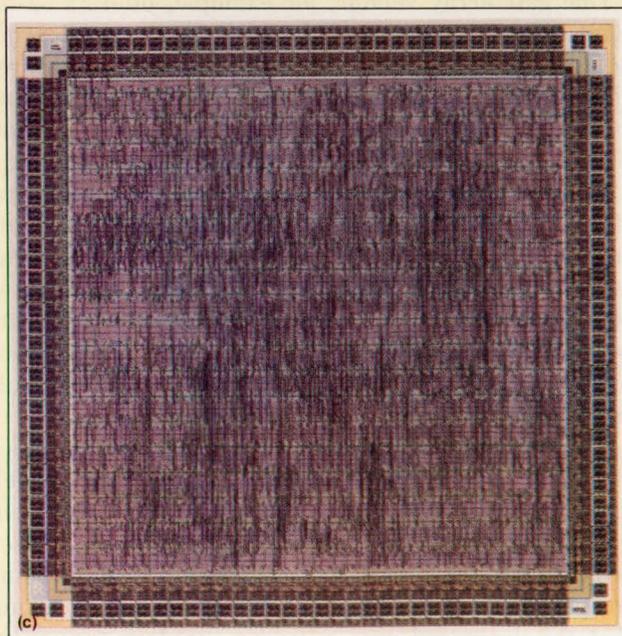
Efficient use of silicon

Using this method, a 16-bit counter that would have a defi-

nite height and width if manufactured as a standard cell can assume a wide variety of dimensions. This versatility allows you to use the available silicon as efficiently as possible within the constraints of the gate-array design methodology.

The photos of **Fig A** are of three 16-bit RISC processors generated by VLSI Technology's compiler. Your design interface with the vendor is the same in all three cases; the compiler generates a net list from the schematic that you develop using the vendor's schematic-capture package.

Fig Aa shows a cell-based implementation built around standard cells. **Fig Ab** depicts a standard-cell implementation: The increased regularity evident in the photo belies the increased difficulty of layout associated with this approach. **Fig Ac** presents a continuous-gate implementation. The cell-based chip occupies $\frac{1}{10}$ as much area as the continuous-gate IC; the standard-cell array occupies $\frac{7}{10}$ as much area as the continuous-gate implementation.



System requirements are fluid; sometimes designs aren't frozen until after months of production.

the circuits that you specify. Laserpath calls these parts "1-day gate arrays"; although currently turnaround takes one to five days, the manufacturer intends to have the turnaround time for all parts down to one day by the end of the year. One-day parts do command a premium price, of course. Laserpath's goal is to provide 1-hour turnaround times within the next three years.

The laser-disconnect parts are targeted at prototype applications, but Laserpath provides masked parts that are direct replacements for the laser-disconnect ones. The masked parts are suitable for volume production; they don't require the time-consuming disconnection step. Also, because the laser-disconnect parts are fully interconnected to begin with and are then disconnected at two different levels of metal, they carry an area penalty. First-generation parts typically consumed 80% more real estate than comparable masked parts. That overhead is now down to approximately 30%, but of course this greater chip area results in a higher price.

The vendor generates the masked parts from the same net list you develop for the laser-disconnect parts, which means you can migrate to masked parts for only the masks' additional NRE costs. Larry Jordan, Laserpath's vice president of marketing and sales, says the break-even point for conversion to masked parts is currently at around the 1000-piece level.

Laser-prototype and equivalent mask-programmed production devices range in size from 880 to 6000 equivalent 2-input gates, and the manufacturer lists the parts' internal gate delay as 3.12 nsec max. They are fabricated using 2- and 3- μ m silicon-gate CMOS technology and emulate LSI Logic's 7000 Series.

At one time, you could test your designs by building a breadboard and testing the breadboard rather than the gate array that would replace it in your system. The problem with a breadboard of SSI and MSI components is that it's difficult to accurately emulate the critical performance parameters of the gate-array design that you're attempting to test. Using the laser-disconnect approach, you have flexibility. You can test with prototypes that have the same performance as the production parts, if you want to go to production with the laser-disconnect parts, or you can test with prototypes that have virtually the same performance as the production parts, if you decide to change over to the masked parts for larger production runs.

Although getting products to market faster is the goal, countervailing forces are operating that could

extend the time it takes to get your devices into production. You now have to complete UL approval for products prior to production. With the Laserpath parts, you can submit a design to UL and FCC labs that is form, fit, and functionally equivalent to your production boards at a time when breadboard techniques would prohibit such a submission. By making it possible for development and agency approval to take place in parallel, Laserpath improves your product's time-to-market.

Whereas the device manufacturers discussed to this point are intent on decreasing the time it takes to get a gate array to market, other vendors of gate arrays are concentrating on increases in system operating speed. As you incorporate more circuitry into a single gate array, you encounter fewer of the lengthy delays associated with driving off-chip devices, thus realizing performance gains. (Off-chip delay times are greater than on-chip delays because of the greater capacitance associated with off-chip loads.) Capacities of more than 120,000 equivalent 2-input gates elevate the complexity of a system you can integrate into a single IC. With this kind of capacity, you can implement an entire RISC processor using one gate array.

Business doesn't have to be risky

One gate-array vendor, for example, offers a 32-bit RISC μ P and support peripherals as standard products. VLSI Technology Inc's VGT100 family features chips with equivalent-gate capacities ranging from 10,000 to 50,000 usable 2-input gates, enough to incorporate a μ P and peripheral circuitry all on one chip.

VLSI Technology achieves this high level of integration with a chip-layout approach it calls continuous gate technology. Using this approach, the company can attain 75% chip utilization, or 50,000 usable gates out of 66,550 raw gates. This utilization level is significant because it allows you to implement the same function using a smaller piece of silicon; this reduction should translate into a lower per-piece price for you.

This approach also eases placing and routing tasks. Rather than reserving open areas for routing channels as in the traditional gate-array approach, continuous gate technology provides routing channels over utilized cells. In addition, local routing for macrocells doesn't compete with global routing. VLSI Technology claims that this increased ease will also cut days from your turnaround time, although to date its parts have turnaround times comparable to the rest of the well-established gate-array manufacturers.

Along with high gate count, the VGT100 Series allows you to operate with system clock speeds as high as 70 MHz. The specified internal gate delay for a 2-input NAND gate driving two loads is 0.8 nsec. Wrought with 1.5- μm silicon-gate design rules, the parts operate from 5V supplies and typically dissipate 20 $\mu\text{W}/\text{gate}/\text{MHz}$.

LSI Logic's LCA10000 Series also uses a channelless interconnection scheme to achieve high gate density. This series features raw gate counts of 129,000 gates and estimated usable gates of 50,000. It's fabricated in 1.5- μm 2-layer metal HCMOS technology and provides speeds equivalent to 10K ECL: a 650-psec internal delay for a 2-input NAND gate driving two loads. The line comprises six arrays, ranging in size from 25,740 to 129,042 gates. Although these devices are channelless and feature the high gate counts associated with that architecture, they are cell-based arrays and therefore require more silicon, gate for gate, than do compacted arrays (Fig 1).

In addition, LSI Logic offers the LSC15 Series structured-cell arrays. These devices offer usable gate counts as high as 60,000 and the same 10K ECL performance that the LCAH10000 Series exhibits. The LSC15 arrays offer high-density static-memory elements of as much as 36k bits as well as multiport RAMs, ROMs, LIFO memories, and FIFO memories. The series' megafunction list includes 2900 Series' bit-slice building blocks, 8200 Series peripheral devices, a 6845 CRT controller, and generic logic functions. You can design your own master slices, which include a commonly used subset of these functions, surrounded by a LCA10000 Series gate array; the gate array allows you to tailor your predefined slices to individual applications. With the high density provided by these parts, and the consequent high speed of operation of systems that have all their functionality integrated onto a single chip, you can develop your own 16-bit controller using one of these gate arrays and operate it in the 30- to 50-MHz range.

Nonetheless, don't look for quick-turnaround prototype parts such as those discussed earlier. LSI Logic vice president Keith Lobo believes that fast-turnaround prototyping parts are unnecessary for two reasons. First, he believes that with today's typical turnaround time of six to eight weeks, the gate array doesn't create any bottleneck in design testing. In a typical situation, you have to wait a significant amount of time to get your pc boards laid out; then, you have to wait a couple of more weeks for the prototype boards to arrive.

Finally, you'll probably bring the boards up with application software which, very likely, isn't ready either.

Second, Lobo believes that a good deal of prototyping should be done via simulation. If the models are good enough—and he contends that his are—then a designer will get an accurate picture of how a circuit will work. Good simulation allows you to test not only the accuracy

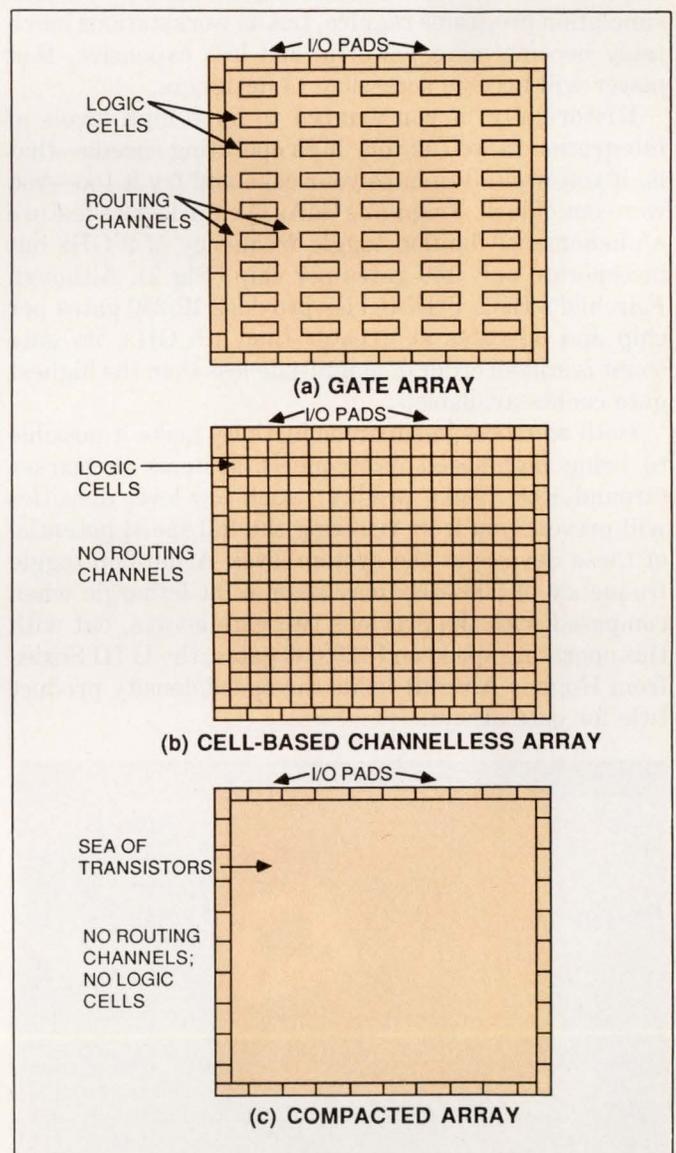


Fig 1—In the traditional architecture of a gate array (a), I/O pads surround columns of logic cells interconnected via the routing channels. Channel-free arrays (b) increase the gate count by filling the entire array with logic cells and by allowing you to use any part of the array for interconnections. The basic building blocks of compacted arrays (c) are p- and n-channel transistors, not logic cells.

Static-RAM cells accomplish the gate interconnections, allowing you to modify your configuration on-the-fly.

of your logic design but also the timing associated with that design.

The ultimate goal of those who design simulators is to eliminate the breadboard or prototype stage of the development cycle. Once designers realize this goal, simulators will fulfill the same function as in-circuit emulators do in μ P-based design. The biggest impediment has been the enormous computational power that simulation programs require, but as workstations inevitably become more powerful and less expensive, that power will become accessible to designers.

Historically, if you wanted to have high levels of integration as well as very high operating speeds—that is, if you wanted to have your cake and fry it too—you were out of luck. Triquint's GaAs Q-chip devices feature a phenomenal flip-flop toggle frequency of 2 GHz but incorporate only 140 gates per chip (Fig 2). Although Fairchild's ECL FGX-Series provides 12,250 gates per chip and operates at greater than 1.5 GHz, its gate count is still an order of magnitude less than the highest gate counts available.

Until advances in superconductivity make it possible to bring high-speed interconnect systems to market (around 1990, some predict), such low-level densities will prevent you from realizing the full speed potential of these devices at the system level. A flip-flop toggle frequency of 500 MHz may seem a bit lethargic when compared with the previous two gate arrays, but with this operating speed and 129,000 gates, the U III Series from Hughes Aircraft holds the speed/density product title for gate arrays.

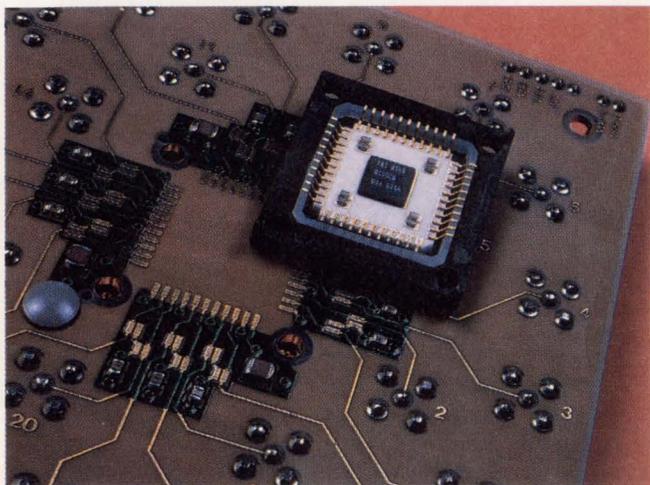


Fig 2—This gate array, a member of Triquint's Q-chip series, is a GaAs, ECL-compatible chip that blazes along at a 2-GHz flip-flop toggle frequency.

It should be obvious by now that you have a plethora of products to choose from. To help you choose, we've included the tables on the following pages, but don't expect an exhaustive account of all gate-array manufacturers. As of this writing, there are at least a hundred gate-array vendors.

Moreover, don't take the information in the tables too literally: Equivalent-gate and gate-utilization figures are approximations. If, for example, you multiply the equivalent gate count of some of the higher-performance gate arrays by the power-dissipation/gate figure, you will obtain an egg-frying 40W dissipation figure for the IC; in reality, the part will dissipate only 15W. The tabulated figures don't take into account configuration-dependent variations in the listed parameters.

Finally, you should be aware that it's time for a shakeout in this industry. The ASIC pie is only so big and, with more than 100 hungry vendors, some are sure to end up with a hollow feeling in their stomachs. After only six months, Monolithic Memories got out of the gate-array manufacturing business (although it maintains a second-source relationship with Xilinx). Choose a vendor that provides you with production options, and make sure that you can complete your designs and get them into production whether the vendor remains in business or not. If, for technical advantages, you choose an ASIC house without a second source, make sure that it's in the business to stay. Ask yourself certain questions: "How long has the company been in this business?" "Is it making money?" "Is it a division of a well-established company?"

EDN

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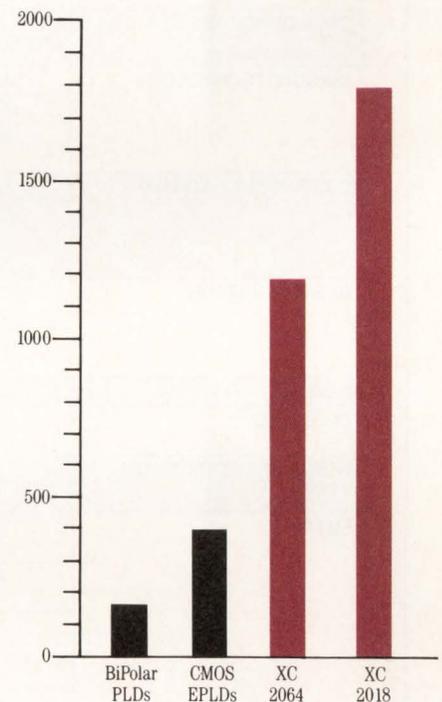
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The Programmable Gate Array CompanySM

MOS DIGITAL ARRAYS

MANUFACTURER	PRODUCT LINE	DRAWN TRANSISTOR CHANNEL LENGTH (μm)	CAPACITY			PERFORMANCE				
			NUMBER OF EQUIVALENT 2-INPUT GATES	TYPICAL GATE UTILIZATION (%)	NUMBER OF BONDING PADS (DEDICATED POWER)	INTERNAL GATE DELAYS WITH 2 LOADS, 1-mm METAL (nSEC)		OUTPUT-BUFFER DELAYS WITH 50-pF LOAD (nSEC)		MAXIMUM FLIP-FLOP TOGGLE FREQUENCY (MHz)
						TYP	MAX	TYP	MAX	
AMCC	Q6000	2	1394 TO 6206	85	74 TO 154 (4 TO 16)	1.3	—	8.2	—	50
	Q6000A	1.8	1395 TO 6206	85	74 TO 154 (4 TO 16)	1.0	—	6.4	—	50
AMD	7000	2	2000 TO 10,000	70 TO 95	232 MAX	1.4	2.4	5.7	9.7	50 TO 70
ARRAY TECHNOLOGY	DHS, HDC*	3	300 TO 2650	80	36 TO 94	1.4	3.2	6	—	35
BARVON RESEARCH	BC2XX	2	100 TO 10,000	—	20 TO 180 (2 TO 4)	1.6	1.8	10	15	75
	BC4XX	4	500 TO 5000	—	43 TO 93 (2)	2.5	5	18	25	55
	BC5XX	5	500 TO 5000	—	43 TO 93 (2)	3.5	6.5	25	35	45
CALIFORNIA DEVICES	DLM	3	200 TO 10,152	70 TO 95	30 TO 156	2	3.8	6	11.0	60
	CHA	2	210 TO 13,230	75 TO 95	30 TO 176	1.4	2.4	2.8	4.9	80
CIRCUIT TECHNOLOGY	MA8304	3	392	90	28 (2)	3	5	20	25	35
	MA2000	4	1120 TO 6864	90	48 TO 136*	4	6	20	25	25
	MA3000	3	1120 TO 6864	90	48 TO 136*	3	5	20	25	35
CUSTOM MOS ARRAYS	C2000	2.5	200 TO 3100	75 TO 95	40 TO 149	2	3	7	12	50
	C3000	1.9	1500 TO 10,500	70 TO 85	72 TO 240 (8)	1.1	1.9	5	9	90
	C5000	1.25	500 TO 25,000	70 TO 80	70 TO 280 (4 TO 24)	0.5	0.9	3.5	5	350
CUSTOM SILICON	HCA6200	2	2430 TO 4860	80 TO 95	100 TO 124 (12 TO 16)	1.9	—	5.6	10.3	85
	HCA6300	3	648 TO 2295	80 TO 95	40 TO 124 (2 TO 12)	2.5	—	8.2	15.6	70
EXAR	XR-30,000	3	156 TO 3025	80 TO 90	22 TO 98 (2)	3	6	15	—	35
FAIRCHILD	FGC	2	540 TO 8300	90	44 TO 208 (4 TO 16)	0.9	1.7	4	8	210
FERRANTI/INTERDESIGN	MH	5	70 TO 1600	90	18 TO 84	8	14	30	50	50
	MC	7*	140 TO 800	90	32 TO 68	8, 20*	12, 25*	50	75	20
FUJITSU	AVB	1.8	357 TO 2052	80 TO 90	38 TO 80 (4 TO 8)	1.4	2.05	3.9	5.8	85
	AVM	1.8	1024 TO 4096	80 TO 90	110 TO 120 (4 TO 8)	1.4	2.05	3.9	5.8	85
	AV	1.8	2640 TO 8000	80 TO 90	106 TO 160 (4 TO 12)	1.4	2.05	3.9	5.8	85
	H	2.8	440 TO 3900	>90	***	2.8	3.9	8	11.2	60
	VH	2.3	2600 TO 8000	>90	***	1.8	2.5	4.8	6.7	74
	UH	1.5	4000 TO 20,160	>90	220 (14)	1	1.45	3.5	5	120
	UHM	1.5	4000 TO 15,000	>90	219 (24)	1	1.45	3.5	5	120
	GENERAL ELECTRIC	IGC20,000	2	300 TO 13,500	80	44 TO 200	1.7	2.3	6	9
GENERAL INSTRUMENT	LA	5	560 TO 1440	—	38 TO 62 (2)	3.5	—	40	55	12
	UA	3	560 TO 1440	—	38 TO 62 (2)	2	—	20	35	16
GOULD AMI SEMICONDUCTOR	GB	2	1000 TO 10,000	95 TO 99	68 TO 208 (8 TO 16)	1.5	2.8	3	6	50
GTE	G5	4	504 TO 2024	—	42 TO 80 (2)	2.2	2.8	10.0	13	20
	G5000	3.5	120 TO 3000	80 TO 99	24 TO 100	2.2	2.8	10	13	20
HARRIS SEMICONDUCTOR	HGA-C	3	648 TO 2520	—	54 TO 100 (4)	3	5	7	10	75
HOLT	HI-5	4	240 TO 2185	—	40 TO 76 (4)	5	8	20	—	30*
	HI-3	6**	153 TO 1020	—	44 TO 68	15***	—	—	—	4.8***
HONEYWELL	HC3500R	1.8	3854	80 TO 85	112 (4)	2.4	8.2	4	10	30
	HC20,000	1.25	20,000	80 TO 90	284 (40)	0.8	1.7	7.9	15.7	100
HUGHES AIRCRAFT	U*	2	1040 TO 40,672	50*	48 TO 256 (8)	0.7	1.2	2.5	3	>200
	V	2	1500 TO 9750	80 TO 90	72 TO 180	1.2	1.4	4.5	5	70
	H	3	1500 TO 9750	80 TO 90	72 TO 180	1.8	2	4.5	5	45
	U-III SERIES	1.5	52520 TO 128296	50	268 TO 412 (8)	0.4	0.6	2.0	2.5	>500

I/O CAPABILITY					GENERAL			
NUMBER OF UNCOMMITTED SIGNAL LINES	NUMBER OF INPUT-ONLY LINES/ OUTPUT-ONLY LINES	I/O COMPATIBILITY C=CMOS T=TTL L=LSSTTL	MAXIMUM OUTPUT CURRENT (mA)	POWER-SUPPLY RANGE (V)	AMBIENT OPERATING-TEMPERATURE RANGE (°C)	PACKAGES P=PLASTIC DIP C=CERAMIC DIP L=LCC G=PIN-GRID ARRAY S=SURFACE MOUNT	NOTES AND REMARKS	
68 TO 146	6 TO 8/0	CTL	24	5	-55 TO +125	CLGS	LEADLESS CHIP CARRIERS AVAILABLE.	
68 TO 146	6 TO 8/0	CTL	24	5	-55 TO +125	CLGS	PLASTIC PACKAGES AVAILABLE FOR PRODUCTION RUNS ONLY.	
70 TO 216	0/0	CTL	12	3 TO 6	-55 TO +125	PCLGS	LIBRARY HAS 120 MACROCELLS AND 210 MACRO-FUNCTIONS. ALL CELLS BUILT AND TESTED.	
30 TO 86	0/0	CT	48*	4.5 TO 5.5	0 TO 70	PCS	*HCD ARRAYS=48 mA, DMS ARRAYS=4.8 mA.	
20 TO 180	0/0	CT	10	1.5 TO 10	-55 TO +125	PCLG		
43 TO 93	0/0	CT	6	1.5 TO 10	-55 TO +125	PCLG		
43 TO 93	0/0	CT	4	1.5 TO 10	-55 TO +125	PCLG		
30 TO 154	8/0	CTL	8	2 TO 6	-55 TO +125	PCLGS		
30 TO 174	8/0	CTL	16	2 TO 6	-55 TO +125	PCLGS		
26	0/0	CT	10	3 TO 7	-55 TO +125	PCLS		
48 TO 128	**	CT	10	3 TO 8	-55 TO +125	PCLGS	*6864-GATE ARRAY HAS 8 POWER PADS.	
48 TO 128	**	CT	10	3 TO 7	-55 TO +125	PCLGS	**1632 AND 2436-GATE DEVICES HAVE 16 INPUT AND 16 OUTPUT PADS DEDICATED.	
48 TO 149	0/0	CT	12	3 TO 6	-55 TO +125	PCLGS	*PLOC J-QUAD PACKAGE AVAILABLE.	
72 TO 232	0/0	CT	12	3 TO 6	-55 TO +125	PCLGS		
70 TO 280	0/0	CTE	40	3 TO 6	-55 TO +125	PCLGS		
54 TO 93	2 TO 53/0	CT	4	3 TO 6	-40 TO +85	PCLGS	CONNECT OUTPUTS IN PARALLEL FOR MORE DRIVE.	
33 TO 56	2 TO 55/0	CT	4	3 TO 6	-40 TO +85	PCLGS		
22 TO 98	0/0	CT	—	4.5 TO 5.5	0 TO 70	PCLGS		
40 TO 120	0 TO 60/0	CL	8	3 TO 6	-55 TO +125	PCLG		
18 TO 84	0/0	CTL	10	3 TO 15	-55 TO +125	PCLGS		
32 TO 68	0/0	CTL	10	3 TO 15	-55 TO +125	PCLGS	*METAL-GATE TECHNOLOGY. **V _{SS} =15V, V _{SS} =5V.	
38 TO 80	0/0	CTL	10*	4.75 TO 5.25	**	PLGS	*V _{OH} , I=-0.4 mA.	
110 TO 120	0/0	CTL	3.2*	4.75 TO 5.25	**	PLGS	RAM, ROM ON-CHIP.	
106 TO 160	0/0	CTL	3.2	4.75 TO 5.25	**	PLGS	**COMMERCIAL, INDUSTRIAL, AND MILITARY TEMPERATURE RANGES AVAILABLE.	
54 TO 80	0/0	CT	3.2	4.75 TO 5.25	**	PCLGS	***PACKAGE DEPENDENT	
106 TO 160	0/0	CTL	3.2	4.75 TO 5.25	**	PCLGS		
220	0/0	CT	6.4	4.75 TO 5.25	**	PCLGS		
219	0/0	CT	6.4	4.75 TO 5.25	**	PCLGS		
44 TO 200	0/0	CT	42	2 TO 5.5	-55 TO +125	PCLG	TURNKEY TRANSLATION TO STANDARD-CELL IC.	
38 TO 62	0/0	CT	1.6	3 TO 6	-40 TO +125	PCL		
38 TO 62	0/0	CT	1.6	3 TO 6	-40 TO +125	PCL		
68 TO 208	0/0	CT	8	2.5 TO 5.5	-55 TO +125	PCLGS		
42 TO 80	0/0	CT	12	3 TO 7	-55 TO +125	PCL		
22 TO 100	0/0	CT	—	3 TO 7	-55 TO +125	PCLS		
54 TO 100	0/0	C	3.2	1.5 TO 7	-55 TO +125	PCLG		
40 TO 76	0/0	CT	100	1.5 TO 18	-55 TO +125	PCLG	*TYPICAL. **METAL-GATE TECHNOLOGY.	
28 TO 62	0/0	CT	100	1.5 TO 18	-55 TO +125	PCLG	***AT 10V.	
112	0/0	CTL	8	3 TO 7	-55 TO +125	CLGS		
140	98/0	CT	5.9	4.5 TO 5.5	-55 TO +125	LG		
40 TO 248	0/0	CT	21	-0.3 TO +6	-55 TO +125	PCLGS	*CHANNELLESS ARCHITECTURE, ROUTING CHANNELS ASSIGNED OVER GATES.	
68 TO 172	0/0	CT	16	-0.3 TO +6	-55 TO +125	PCLGS		
68 TO 172	0/0	CT	16	-0.3 TO +6	-55 TO +125	PCLGS		
260 TO 404	0/0	CTL	21	-0.3 TO +6	-55 TO +125	PCLGS	CHANNELLESS ARCHITECTURE, ROUTING CHANNEL ASSIGNED OVER GATES, DOUBLE LAYER METAL.	

MOS DIGITAL ARRAYS (Continued)

MANUFACTURER	PRODUCT LINE	DRAWN TRANSISTOR CHANNEL LENGTH (μm)	CAPACITY			PERFORMANCE				
			NUMBER OF EQUIVALENT 2-INPUT GATES	TYPICAL GATE UTILIZATION (%)	NUMBER OF BONDING PADS (DEDICATED POWER)	INTERNAL GATE DELAYS WITH 2 LOADS, 1-mm METAL (nSEC)		OUTPUT-BUFFER DELAYS WITH 50-pF LOAD (nSEC)		MAXIMUM FLIP-FLOP TOGGLE FREQUENCY (MHz)
						TYP	MAX	TYP	MAX	
HUGHES AIRCRAFT (Continued)	U-SERIES DOUBLE LAYER	2.0	1040 TO 40672	50	48 TO 256 (8)	0.7	1.2	2.5	3	>200
	U-SERIES TRIPLE LAYER	2.0	1040 TO 40672	75	48 TO 256 (8)	0.6	1.0	2.5	3	>200
INTEGRATED CIRCUIT SYSTEMS	VGT10	2	600 TO 10,000	75	—	1	1.3	6	9	60
INTEGRATED LOGIC	CB-3000	3	800 TO 7300	85 TO 95	44 TO 174	2.5	5	6	11	75
	CA-2000	2	1100 TO 15,000	85 TO 95	44 TO 208	1.8	3.6	5.8	10	—
INTEGRATED MICROCIRCUITS	INTERCHIP A-F	7*	100 TO 650	80 TO 90	32 TO 69	12	17	80	150	3
INTEL	D15A	1.5	2550 TO 19,125	95	73 TO 290	0.7	1.4	3.3	6.6	65
	D15C	1.5	6196 TO 10,700	95	166 TO 240	0.7	1.4	3.3	6.6	65
INTERNATIONAL MICROCIRCUITS	G4000	6*	75 TO 600	—	25 TO 53	35	—	60	—	2
	G7000	3.5	135 TO 2535	—	28 TO 88	3	—	15	—	42
	G9000	2.5	1740 TO 5250	—	64 TO 104	3	5	7	—	45
	1M16000	2	820 TO 6024	—	60 TO 158	1.3	2	5	—	60
ITT VLSI DESIGN CENTER	ISDS	3	1008 TO 4400	75 TO 85	44 TO 90	3	8	17	22.5	30
LASER PATH	LP7000P	2	880 TO 6000	90	52 TO 138	1.3	2.6	8	16	70
	LP7000C	2	880 TO 6000	90	68 TO 186	1.3	2.6	8	16	70
	LP5000A	2	880 TO 6000	90	74 TO 180	1.3	2.6	8	16	70
LSI LOGIC	LL5000	3	504 TO 6000	75 TO 90	74 TO 180	2.5	4.5	5.5	9.6	—
	LL7000	2	880 TO 10,000	75 TO 90	68 TO 232	1.4	2.4	7	12	—
	LL8000	2	880 TO 3200	80 TO 90	72 TO 132	1.4	2.4	7	10.5	—
	LL9000	1.5	880 TO 10,000	75 TO 90	28 TO 232	1	1.7	4	7	—
	LCA10,000	1.5	26,000 TO 129,000	35 TO 55	168 TO 368	0.6	1.1	2.5	4.7	—
MARCONI ELECTRONIC DEVICES	MA2000A	3	1000 TO 7000	90	28 TO 136 (2 TO 8)	3.5	4.8	10	17	33
	MA8304	3	392	90	28 (2)	3	5	20	25	35
	MA2000A	3	1120 TO 6864	90	48 TO 136*	1.6	3.1	12	20	60
	MA4000	2	3904 TO 10,044	90	104 TO 168 (8)	0.9	1.6	6	10	100
	MA9000	3	2484 TO 4048	90	84 TO 102 (4)	1.7	3.4	12	20	50
MCE SEMICONDUCTOR	MGA*	5	220 TO 285	—	21 TO 50 (0 TO 4)	8	10	80	—	12
MITEL	MA-5	5	500 TO 1000	—	38 TO 48 (2)	4	5	—	—	15
	MA-4	4	500 TO 2000	—	38 TO 74 (2 TO 4)	3	4	—	—	20
MITSUBISHI	M60,000	2	500 TO 8000	85 TO 95	16 TO 209 (2 TO 19)	1.1	—	4	—	100
	M60,000	3	200 TO 4800	85 TO 95	16 TO 209 (2 TO 19)	2	—	6	—	40
MOTOROLA	HCA6300*	3	648 TO 4860	85 TO 95	33 TO 84 (0 TO 16)	2.5	4.75	8	15.2	40
	HCA6200*	2	648 TO 8500	85 TO 95	44 TO 168 (0 TO 12)	1.5	3.6	6	11.4	55
NATIONAL SEMICONDUCTOR	SCX6200	2	600 TO 8700	90	0 TO 220	0.8	1.2	7	12	110
	SCX6300	3	648 TO 6090	—	37 TO 160 (4 TO 16)	1.5	2.5	6	10	70
NCM	3000	7.5*	340 TO 480	80 TO 85	38 TO 48	10	15	21	33	5
	7000	3	780	80 TO 85	62	3	5	9	14	18
	7000	5	780	80 TO 85	62	5	8	12	18	10
NCR MICROELECTRONICS	62XXA 62A00	2	648 TO 8568	85	44 TO 168 (NONE)	1.6	3.0	5.6	10.3	85

I/O CAPABILITY					GENERAL				NOTES AND REMARKS
NUMBER OF UNCOMMITTED SIGNAL LINES	NUMBER OF INPUT-ONLY LINES/ OUTPUT-ONLY LINES	I/O COMPATIBILITY C=CMOS T=TTL L=LSSTL	MAXIMUM OUTPUT CURRENT (mA)	POWER-SUPPLY RANGE (V)	AMBIENT OPERATING-TEMPERATURE RANGE (°C)	PACKAGES P=PLASTIC DIP C=CERAMIC DIP L=LCC G=PIN-GRID ARRAY S=SURFACE MOUNT			
40 TO 248	0/0	CTL	21	-0.3 TO +6	-55 TO +125	PCLGS	CHANNELLESS ARCHITECTURE, ROUTING CHANNEL ASSIGNED OVER GATES, DOUBLE LAYER METAL.		
40 TO 248	0/0	CTL	21	-0.3 TO +6	-55 TO +125	PCLGS	CHANNELLESS ARCHITECTURE, ROUTING CHANNEL ASSIGNED OVER GATES, TRIPLE LAYER METAL.		
38 TO 136	0/0	CTL	8	4 TO 6	-40 TO +125	PCLGS			
44 TO 174	0/0	CT	3.2*	4 TO 6	0 TO 70	PCLGS	RAM, ROM, PLA ON CHIP.		
44 TO 208	0/0	CT	3.2*	4 TO 6	0 TO 70	PCLGS			
32 TO 69	0/0	CTL	8.5	3 TO 15**	-55 TO +125	PCLGS	*METAL-GATE TECHNOLOGY. **1.5V OPTION AVAILABLE.		
64 TO 210	0/0	CTL	12	4.5 TO 5.5	-55 TO +125	PCLGS	LSSD TESTING & SOLDER BUMP TECHNOLOGY AVAIL.		
103 TO 174	0/0	CTL	12	4.5 TO 5.5	-55 TO +125	PCLGS	COMPOSITE ARRAYS WITH 230 4-BIT STATIC RAM.		
33 TO 53	7 TO 9/0	CT	1	2 TO 15	-55 TO +125	PCLG	*METAL-GATE TECHNOLOGY.		
28 TO 88	8/0	CT	10	2 TO 10	-55 TO +125	PCLG			
64 TO 104	4/0	CT	10	2 TO 10	-55 TO +125	PCLG			
60 TO 158	6/0	CT	8	2 TO 7	-55 TO +125	PCLG			
48 TO 106	0/0	CT	10	3 TO 5.5	-55 TO +125	PCLGS			
44 TO 122	0/0	CTL	12	3 TO 6	-55 TO +125	PCLG			
60 TO 170	*0/0	CTL	12	3 TO 6	-55 TO +125	PCLG			
66 TO 168	*0/0	CTL	12	3 TO 6	-55 TO +125	PCLG			
74 TO 180	0/0	CT	12	3 TO 6	-55 TO +125	PCLGS			
68 TO 232	0/0	CT	12	3 TO 6	-55 TO +125	PCLGS			
72 TO 132	0/0	CT	20	3 TO 6	-55 TO +125	PCLGS			
68 TO 232	0/0	CT	12	3 TO 6	-55 TO +125	PCLGS			
168 TO 368	0/0	CT	12	3 TO 6	-55 TO +125	CLGS	CHANNEL-FREE ARCHITECTURE WITH HIERARCHICAL PLACEMENT. PROGRAMMABLE-SLEW-RATE OUTPUT BUFFERS.		
162 TO 228	0/0	CT	12	3 TO 6	-55 TO +125	CLGS	ARRAYS CONTAIN RAM, ROM, AND MEGACELLS SUCH AS ALUs AND MULTIPLIERS.		
28 TO 128	*	CT	10	3 TO 8	-55 TO +125	PCLGS	*1600- AND 2400-GATE ARRAYS HAVE 16 DEDICATED-INPUT AND 16 DEDICATED-OUTPUT I/O CELLS.		
26	0/0	CT	10	3 TO 7	-55 TO +125	PCLS			
48 TO 128	**	CT	10	3 TO 7	-55 TO +125	PCLGS	*6864 GATE ARRAY HAS 8 PWE PADS. **1632 AND 2436 GATE DEVICES HAVE 16 INPUT AND 16 OUTPUT PADS DEDICATED.		
96 TO 160	0	CT	10	4 TO 6	-55 TO +125	PCLGS			
84 TO 102	0	CT	10	3 TO 7	-55 TO +125	PCLGS	RAD HARD CMOS/SOS		
0	6 TO 24/ 6 TO 24	CT	25	3 TO 18	-55 TO +125	PCLG	*METAL-GATE TECHNOLOGY.		
—	ALL/ALL*	CT	12	3 TO 6.5	-55 TO +125	PCL	*PADS ARE EITHER INPUT OR OUTPUT.		
—	ALL/ALL*	CT	10	3 TO 6.5	-55 TO +125	PCL			
14 TO 190	0/0	CT	7*	3 TO 6	-20 TO +75	PCGS	CONNECT OUTPUT BUFFERS IN PARALLEL FOR MORE DRIVE.		
14 TO 190	0/0	CT	7*	4.5 TO 5.5	-20 TO +75	PCGS			
33 TO 84	0 TO 53/0	CT	4	3 TO 6	-40 TO +85	PCLGS	**"A" VERSIONS OFFER PROGRAMMABLE POWER PADS AND PARALLEL-OUTPUT CAPABILITY.		
44 TO 168	0 TO 66/0	CTL	10	3 TO 6	-40 TO +85	PCLGS			
20 TO 220	3 TO 12/0	CT	24	4.5 TO 5.5	0 TO 70	PCLGS			
37 TO 88	12 TO 66/0	C	25	2 TO 6	-55 TO +125	PCLG			
34 TO 42	4/0	CTL	1.6	5 TO 15	-55 TO +125	PCL	*METAL-GATE TECHNOLOGY.		
62	0/0	CTL	1.6	3 TO 10	-55 TO +125	PCL			
62	0/0	CTL	1.6	3 TO 10	-55 TO +125	PCL			
44 TO 168	0/0	CTO	24	3 TO 6	-40 TO +85	PCLGS	*COMMERCIAL, INDUSTRIAL, AND MILITARY RANGES AVAILABLE. PADS ARE USER-PROGRAMMABLE.		

MOS DIGITAL ARRAYS (Continued)

MANUFACTURER	PRODUCT LINE	DRAWN TRANSISTOR CHANNELLENGTH (μm)	CAPACITY			PERFORMANCE				
			NUMBER OF EQUIVALENT 2-INPUT GATES	TYPICAL GATE UTILIZATION (%)	NUMBER OF BONDING PADS (DEDICATED POWER)	INTERNAL GATE DELAYS WITH 2 LOADS, 1-mm METAL (nSEC)		OUTPUT-BUFFER DELAYS WITH 50-pF LOAD (nSEC)		MAXIMUM FLIP-FLOP TOGGLE FREQUENCY (MHz)
						TYP	MAX	TYP	MAX	
NEC ELECTRONICS	65XXX	1.5	400 TO 20,000	85 TO 95	54 TO 266 (2)	0.89	1.6	6	10.8	70
OKI SEMICONDUCTOR	MSM70,000	3	387 TO 4200	85	50 TO 188 (2 TO 8)	2.7	5	4.5*	8*	80
	MSM70H000	2	700 TO 10,000	85	50 TO 188 (2 TO 8)	2	4	4.5*	8*	80
	MSM70,000	1.5	100 TO 3000	85	50 TO 188 (2 TO 8)	1	2	4.5*	8*	80
PLESSEY SOLID STATE	CLA5000	2.5	640 TO 10,044	70 TO 80	40 TO 176 (4 TO 16)	1.6	3.5	2.9	5.8	100
	CLA3000	4	840 TO 6000	70 TO 80	44 TO 112	2.5	5	12	18	40
RAYTHEON SEMICONDUCTOR	RC1.5	1.5	3000 TO 7800	80 TO 90	—	1.6	4	—	—	100
RCA SOLID STATE	PA40,000	3	725 TO 1212	85	74 TO 102 (4)	3	5	6	9	40
	PA50,000	3	880 TO 6000	85	74 TO 180 (4)	2.5	3	6	9	40
SAHNI	LAXXX	3	100 TO 1200	75	20 TO 68	3	5	15	20	50
SGS SEMICONDUCTOR	HSG3000	3.5	272 TO 2550	—	36 TO 104 (4)	5	9	7.2	8.6	15
	HSG5000	3	880 TO 6000	—	74 TO 180 (8 TO 12)	2.5	4.5	5.5	6.2	25
	HSG7000	2	880 TO 10,000	75 TO 80	68 TO 252	1.4	2.4	0.7	1.2	70
SIEMENS AG	SCXB	2	1000 TO 10,000	90	40 TO 180 (4 TO 12)	1.5	3	3.5	7	100
SILICON SYSTEMS	—	3	< 10,000	—	< 40	2	7.4	10	14	40
SILICONIX	Si6000	2	500 TO 6200	90	48 TO 154 (4 TO 8)	1.7	3	6	12	50
SMOS SYSTEMS	SLA5000	3	3082 TO 5000	50 TO 90	108	2.7	4.6	13	22.2	37
	SLA6000	2	6000 TO 6206	50 TO 90	154	1.7	3.2	8.7	16.4	70
	SLA7000	1.5	7000 TO 16,250	50 TO 90	170 (8)	0.9	1.5	6.2	10.3	110
	SLA8000	1.2	8000 TO 38,016	50 TO 90	226 (8)	0.6	1.0	4.3	7.2	175
SOREP	RPS5000	2	500 TO 10,000	80 TO 85	48 TO 112	—	1.6	—	5.4	100
STC MICROTECHNOLOGY	7C	3	600 TO 1920	—	38 TO 96 (8)	—	5	—	13	50
	TMG3000	5*	50 TO 216	—	22 TO 44	13	—	—	—	5
	TMG4000	6	300 TO 1260	—	40 TO 78	5	12	—	—	33
TEXAS INSTRUMENTS	TAC-H	2.8	440 TO 3900	90	54 TO 68 (4)	4	—	12	—	60
	TAC-VH	2.3	2640 TO 8000	90	106 TO 160 (4)	2.5	—	7	—	75
THOMSON COMPONENTS MOSTEK CORP	TSGA	3	1152 TO 4080	98	68 TO 124 (4)	2.3	4.5	3.9	9.0	7100
	TSGB	2	1120 TO 9776	98	60 TO 192 (12 TO 16)	1.5	—	3.7	8.3	7200
	TSGC	1.2	1120 TO 9776	98	60 TO 192 (12 TO 16)	1.0	—	3.7	8.5	7200
TLSI	TA-X	5	300 TO 1260	70 TO 80	40 TO 78 (2)	6	10	—	—	10
	TA-500—2500	3	540 TO 2500	70 TO 80	40 TO 84 (2)	2	2.5	9	11	25
TOSHIBA AMERICA	TC22SC	2	470 TO 10,000	100	26 TO 184	1.5	3	5.75	11.5	100
	TC19G	1.5	3200 TO 10,000	80	128 TO 232	1	2	4	8	120
	TC17G	2	540 TO 10,000	80	48 TO 232	1.5	3	5.75	11.5	100
	TC11OG	1.5	5330 TO 129,042	40	84 TO 370	0.7	1.4	—	—	120
TRIQUINT SEMICONDUCTOR	Q-CHIP*	1	140	75 TO 100	44 (20)	0.15	0.20	0.20**	0.26**	2000
UNIVERSAL	ISO-2	2	99 TO 2400	—	22 TO 98 (2)	1.1	2	3	5.5	60
	ISO-3	3	99 TO 2400	—	22 TO 98 (2)	1.6	2.9	4.5	8.5	40
	ISO-5	5	99 TO 2400	—	22 TO 98 (2)	3.2	6.2	8	15	20
VLSI TECHNOLOGY	VCG	2	500 TO 8000	80 TO 95	44 TO 200 (4 TO 16)	1.1	—	4	5.1	50
	VGT10	2	1590 TO 10,648	75	64 TO 148 (8)	1.2	2.4	6.1	12.2	50
	VGT100	1.5	1590 TO 66,550	75	64 TO 356 (8)	0.8	1.6	2.3	4.5	70

I/O CAPABILITIES					GENERAL			
NUMBER OF UNCOMMITTED SIGNAL LINES	NUMBER OF INPUT-ONLY LINES/ OUTPUT-ONLY LINES	I/O COMPATIBILITY C=CMOS T=TTL L=LSSTL	MAXIMUM OUTPUT CURRENT (mA)	POWER-SUPPLY RANGE (V)	AMBIENT OPERATING-TEMPERATURE RANGE (°C)	PACKAGES P=PLASTIC DIP C=CERAMIC DIP L=LCC G=PIN-GRID ARRAY S=SURFACE MOUNT	NOTES AND REMARKS	
54 TO 256	0/0	CT	12	4.5 TO 5.5	0 TO 70	PCLGS	OUTPUT BUFFER TOGGLE FREQUENCY=50 MHz MAX.	
48 TO 172	0/0	CT	24	3 TO 6	-40 TO +85	PCGS	*20-pF LOAD.	
48 TO 172	0/0	CT	24	3 TO 6	-40 TO +85	PCGS		
48 TO 172	0/0	CT	24	3 TO 6	-40 TO +85	PCGS		
36 TO 160	4 TO 16/0	CT	6.4	3 TO 6	-55 TO +125	PCLG		
40 TO 108	4/0	CT	6.4	3 TO 6	-55 TO +125	PCLG		
90 TO 142	0/0	CTL	—	4 TO 6	-55 TO +125	LG		
58 TO 86	0/0	C	2.4	3 TO 6	-55 TO +125*	PCLGS	*-40 TO +85 TEMPERATURE RANGE AVAILABLE.	
56 TO 86	0/0	CT	2.4	3 TO 6	-55 TO +125	PCLGS		
20 TO 68	0/0	—	8	2 TO 6	0 TO 70*	PCLGS**	*-55 TO +125 TEMPERATURE RANGE AVAILABLE. **DIE ALSO AVAILABLE UNPACKAGED OR IN WAFERS.	
—	—	CT	4.8	3 TO 6	-55 TO +125*	PCLGS	*-40 TO +85 AND 0 TO 70 TEMPERATURE RANGES AVAILABLE.	
—	—	CT	6	3 TO 6	-55 TO +125	PCLGS		
68 TO 232	0/0	CT	12	3 TO 6	-55 TO +125	PCLGS		
38 TO 168	0/0	CT	8	3 TO 6	-55 TO +125	PCLGS		
<40	0/0	CT	25	4.5 TO 5.5	-55 TO +125	PCL		
48 TO 154	6/0	CTL	16	3 TO 7	-55 TO +125	PCLGS		
100	8/8	CTL	6	3 TO 7	0 TO 70	PCLGS		
146	8/8	CTL	6	3 TO 7	0 TO 70			
162	0/0	CTL	6	3 TO 7	0 TO 70			
218	0/0	CTL	6	3 TO 7	0 TO 70			
160	0/0	CT	6.4	4 TO 6	-55 TO +125	PCLGS		
38 TO 96	0/0	T	—	4.75 TO 5.25	0 TO 70	PG		
—	—	CT	4	3 TO 15	-55 TO +125	PCLG	*METAL-GATE TECHNOLOGY.	
—	—	CT	—	3 TO 10	-55 TO +125	PCLG		
54 TO 80	0/0	CT	2	4.75 TO 5.25	0 TO 70	PCLG		
106 TO 160	0/0	CT	4	4.75 TO 5.25	0 TO 70	PCLG		
64 TO 120	0/0	CT	4	3 TO 6	-55 TO +125	PCLGS		
56 TO 192	0/0	CTL	4	3 TO 6	-55 TO +125	PCLGS		
56 TO 192	0/0	CTC	4	3 TO 6	-55 TO +125	PCLGS		
37 TO 75	3/0	CT	4	3 TO 12	-55 TO +125	PCLGS		
40 TO 84	0/0	CT	4.8	2.5 TO 6	-55 TO +125	PCLGS		
26 TO 184	0/0	CT	8	4.75 TO 5.25	0 TO 70*	PCLGS**	*YOU CAN REQUEST EXTENDED TEMPERATURE RANGE. **FLATPACK PACKAGES AVAILABLE.	
128 TO 232	0/0	CT	12	4.75 TO 5.25	0 TO 70*	PCLGS**		
48 TO 232	0/0	CT	8	4.75 TO 5.25	0 TO 70*	PCLGS**		
84 TO 370	0/0	CT	12	4.75 TO 5.25	0 TO 70*	PCLGS**		
24	0/0	CT***	32	-3 AND +4, ±10%	0 TO 85	L	*GaAs TECHNOLOGY.**50Ω LOAD. ***ECL-I/O COMPATIBLE.	
18 TO 90	0/0	CT	10	3 TO 7	-55 TO +125	PCL	PROGRAMMABLE	
18 TO 90	0/0	CT	6	3 TO 8	-55 TO +125	PCL	SOURCE AND	
18 TO 90	0/0	CT	3	3 TO 15	-55 TO +125	PCL	DRAIN CONTRACTS.	
40 TO 118	0 TO 63/0	CT	10	4.5 TO 5.5	-40 TO +85	PCLGS		
56 TO 140	0/0	CT	12	4.5 TO 5.5	-55 TO +125	PCLGS		
56 TO 348	0/0	CT	12	4.5 TO 5.5	-55 TO +125	PCLGS		

BIPOLAR DIGITAL ARRAYS

MANUFACTURER	PRODUCT LINE	TECHNOLOGY	CAPACITY			PERFORMANCE				
			NUMBER OF EQUIVALENT 2-INPUT GATES	TYPICAL GATE UTILIZATION (%)	NUMBER OF BONDING PADS (DEDICATED POWER)	INTERNAL GATE DELAYS WITH 2 LOADS, 1-mm METAL (nSEC)		OUTPUT-BUFFER DELAYS WITH 50-pF LOAD (nSEC)		MAXIMUM FLIP-FLOP TOGGLE FREQUENCY (MHz)
						TYP	MAX	TYP	MAX	
APPLIED MICRO CIRCUITS	Q700	ECL	250 TO 1000	85	34 TO 76 (6 TO 8)	0.5 TO 0.9	—	2.95	—	125
	Q1500	ECL	1500 TO 1700	95	84 TO 120 (10 TO 28)	0.5 TO 0.9	—	2.1	—	125
	Q3500***	ECL	1300 TO 3500	95	76 TO 120 (16 TO 28)	0.7 TO 2.75	—	0.8	—	400
ADVANCED MICRO DEVICES	Am1850	ECL/TTL	1800	90	—	0.8	1.2	1.3	1.9	200
	Am3500	ECL/TTL	3700 TO 5200	95	124 TO 138 (20 TO 26)	0.4 TO 0.6*	0.95*	0.7	1.1	500
CHERRY SEMICONDUCTOR	GENESIS	I ² L	192 TO 288	70 TO 80	30 TO 34	50*	100*	25	50	2
CUSTOM INTEGRATED CIRCUITS	GAC8000	I ² L	7600*	—	64	20	**	**	**	10
CUSTOM SILICON	MCA600-1200ECL	ECL	652 TO 1192	70 TO 85	28 TO 72 (12)	0.7	1.2	2.0	3.8	160
	MCA2500 ECL	ECL	2472	70 TO 85	149 (28)	0.3	0.5	0.75	0.88	700
	MCA500-1300ALS	TTL	533 TO 1280	70 TO 85	28 TO 84 (4)	2.3	3	12	14	80
	MCA2800 ALS	TTL	2720	70 TO 85	149 (4)	0.8	1.1	6	8.2	125
	MCA2900 ETL	ECL TTL	2958	70 TO 85	149 (28)	0.7 & 1.1*	1.2 & 1.8*	0.8 & 3.2*	1.5 & 5.3*	125
FAIRCHILD	FGE	ECL	100 TO 2840	85	24 TO 300	0.3	0.4	0.4	0.6	1000
	FGX	ECL	12,250	85	384 (80)	0.15	0.19	0.5	0.7	>1500
FERRANTI/INTERDESIGN	ULA R	CML	130 TO 2000	70 TO 95	20 TO 80	2.9	5.2	8	14	80*
	ULA DS	CML	512 TO 10,000	95	42 TO 190	1.4	2.5	8	14	130**
FUJITSU MICRO-ELECTRONICS	H-BIPOLAR	LSTTL	360 TO 1680	90	44 TO 103 (4 TO 15)	1.25	—	4.5	—	150
	B2000-BIPOLAR	LSTTL	3162	90	136 (24)	0.95	—	3.5	—	200
	ET 3000	ECL	4200	>90	144 (28)	0.22	0.35	3.7	5.9	1100
HONEYWELL	HE2000	CML	2000	80 TO 95	140 (32)	0.3	1	1	2	660
	HT5000	CML	5000	85 TO 75	120 (24)	0.6	0.8	6	12	500
	HM1000R	CML*	1000	65 TO 75	60 (16)	0.7	1.5	4.4	5.7	400
	HE8000	CML	8000	85 TO 90	188 (56)	0.3	1	0.7	1	500
	HM3500	CML*	3500	80 TO 90	120 (32)	0.4	0.8	1	2	600
	MOTOROLA	MCA I-ECL	ECL	625 TO 1192	85 TO 95	46 TO 60 (8 TO 12)	0.8	1.2	2.1	3.1
MCA II-ECL	ECL	902 TO 2760	85 TO 95	54 TO 120 (8 TO 28)	0.3	0.5	0.6	0.9	770	
MCA I-TTL	ECL**	533 TO 1280	85 TO 95	57 TO 76 (7 TO 8)	1.4	3	9.8	14	80	
MCA II-TTL***	ECL**	1800 TO 2860	85 TO 95	120 (28)	0.9	1.15	5	7.5	250	
BIMOS****	CMOS/BIPOLAR	704 TO 6144	85 TO 95	202 (52)	0.9	1.15	1.25	3.5*	150	
MCA III-ECL	ECL*****	10,332	85 TO 95	256 (33)	0.15	0.175	0.2	0.3	1200	
NEC ELECTRONICS	μPB63XX	ECL	600 TO 5000	95	88 TO 172 (10)	0.25	0.375	1	1.5	500
RAYTHEON SEMICONDUCTOR	R-OI/SL	ISL	3500 TO 5000	60 TO 80	120 TO 150	1.2*	2	—	—	125
	R-JI/SL	ISL	800 TO 2400	60 TO 80	48 TO 96	2.3***	3	—	—	75
SIEMENS AG	SH 100C	OXIS II	400 TO 2500	90	40 TO 144 (6 TO 24)	0.45	0.6	—	—	750
SIGNETICS	TURBO ACE	ECL	600 TO 2700	80 TO 90	64 TO 144 (6 TO 16)	0.35	0.65	0.9	1.25	600
	LOW-POWER ACE	ECL	600 TO 2700	80 TO 90	64 TO 144 (6 TO 16)	0.45	0.65	1.1	1.5	400
TEXAS INSTRUMENTS	TAB	LSTTL	240 TO 1120*	—	40 TO 88 (2)	1.9	—	6.5	—	150
	TAL	TTL	320 TO 500	—	28 TO 36 (4)	6	6.8	9	11	25
	TAT	STL	540 TO 1008	—	56 TO 100 (8)	2.8	4.3	9.5	15	80

	I/O CAPABILITY					GENERAL				NOTES AND REMARKS
	TYPICAL POWER DISSIPATION PER GATE (mW)	NUMBER OF UNCOMMITTED SIGNAL LINES	NUMBER OF INPUT-ONLY LINES/ OUTPUT-ONLY LINES	I/O COMPATIBILITY T=TTL L=LSSTL E=ECL C=CMOS	MAXIMUM OUTPUT CURRENT (mA)	POWER-SUPPLY RANGE (V)	AMBIENT OPERATING-TEMPERATURE RANGE (°C)	PACKAGES P=PLASTIC DIP C=CERAMIC DIP L=LCC G=PIN-GRID ARRAY S=SURFACE MOUNT		
	1.8	8 TO 38	26 TO 28/0	TE	20 (TTL)*	-5.2 AND +5, ±10%	-55 TO +125	CLGS**	*ECL OUTPUT 50Ω. **LDCC AVAILABLE.	
	1.7	0 TO 60	46 TO 60/0 TO 38	TE	20	-5.2 OR -4.7 AND +5, ±10%	-55 TO +125	CLGS**	ECL 10K AND 100K SUITABLE. MIL-STD-883C SUPPORT OPTIONAL. YOU CAN SPECIFY CUSTOM MACROS.	
	1	76 TO 120	0/0	TE	20	-5.2 OR -4.7 AND +5, ±10%	-55 TO +125	CLGS**	***SPEED-POWER PROGRAMMABLE OPTIONS. QM1600S INCLUDES 1280 BITS OF RAM.	
	1.5	75	5/0	LEC	16	-5.2 TO +5, ±10%	0 TO 70	CLGS		
	1 TO 4*	76 TO 124	0 TO 58/0	LEC	32	-5.2 TO +5, ±10%	0 TO 70	G	*SPEED-POWER OPTION. Am3525 CONTAINS 1152 BITS OF RAM.	
	**	24 TO 28	0/0	TLEC	10	1 TO 12	0 TO 85	PCLS	*INJECTOR-CURRENT DEPENDENT. **PROGRAMMABLE.	
	**	62	0/0	TL	—	0.6 TO 5.5	-55 TO +125	PCL	*5-INPUT GATES. **PROGRAMMABLE.	
	4	18 TO 26	28 TO 34/0	E***	30 (50Ω)	-5.2 ±10%	0 TO 70	PCLG	*SPECS FOR ON-CHIP ECL AND TTL CIRCUITRY, RESPECTIVELY.	
	3	68	52/0	E**	30 (50Ω)	-4.2 TO -4.8	0 TO 70	G	**10K, 10KH, AND 100K ECL CIRCUITS.	
	2	12 TO 40	30 TO 30/0 TO 15	TL	24	4.5 TO 5.5	0 TO 70	PCL	***10K AND 10KH ECL CIRCUITS.	
	0.9	120	0/0	TL	8	4.5 TO 5.5	0 TO 70	LG		
	1.3	48 AND 40	72 AND 30/0	LE	30	-5.2 AND +5, ±10%	0 TO 70	G		
	2.5 TO 9	21 TO 220	0 TO 84/21 TO 64	TLEC	20	-4.5 TO -5.7	-10 TO +150	CLGS		
	2.0 TO 4.2	300	16/0	E	20	-4.5 TO -5.7	-10 TO +150	G	2ND HALF '87	
	0.025 TO 1*	38 TO 72	0/0	TLEC	64	4.5 TO 5.5	-55 TO +125	PCLGS	*FOUR SPEED-POWER OPTIONS.	
	0.08 TO 0.5**	40 TO 180	0/0	TLEC	64	4.5 TO 5.5	-55 TO +125	PCLGS	**THREE SPEED-POWER OPTIONS.	
	0.85	44 TO 88	0/0	TL	48	4.75 TO 5.25	*	PCGS	*MILITARY, INDUSTRIAL, AND COMMERCIAL TEMPERATURE RANGES AVAILABLE.	
	0.65	112	0/0	TL	16	4.75 TO 5.25**	0 TO 70	G	**2.1 TO 2.5V OPERATION POSSIBLE.	
	2.4	120	120/72	TE	16 TO 60	4.5 TO 5.5	0 TO 70	G***	***CERAMIC FLATPACK AVAILABLE.	
	3.3	140	0/0	E	4	-3.3 ±5%	0 TO 70	G		
	1	120	44/76	TL	8	5 AND 3.3, ±10%	-55 TO +125	LG		
	3	60	0/0	TLE	8	4.5 TO 5.5	-55 TO +125	LGS	*RAD HARD.	
	1.3	188	0/0	E	4	-3.3 TO -5.2	0 TO 70	E		
	1	120	0/0	TLE	8	-3.3 TO -5.2, 3.3 TO 5	-55 TO +125	LG		
	3.3	18 TO 26	28 TO 34/0	E	*	-5.2 ±10%	0 TO 70	CLG	*25Ω TO -0.2V.	
	2.6	22 TO 68	32 TO 52/0	E	*	-4.5 TO -5.2, ±10%	0 TO 70	CLG		
	1.8	13 TO 31	35 TO 36/9	TL	24	4.75 TO 5.25	0 TO 70	PCLS	**ALS I/O CELLS.	
	0.9	120	0/0	TL	8	4.75 TO 5.25	0 TO 70	LG	***INCLUDES 16x8 MULTIPOINT RAM.	
	0.022/MHz	202	0/0	TLEC	24 (25Ω)	-5.2 AND 5, ±10%	0 TO 70	G	*3.5 FOR CMOS AND TTL; 1.1 FOR ECL.	
	2	256	0/0	E	25Ω TO -2V	-5.2 ±5%	0 TO 70	G	*****AVAILABLE IN 2ND HALF 1986	
	3.3	—	—	TLEC	8	4.5 TO 5.5	0 TO 70	G		
	0.16	120 TO 150	0/0	TL	16	5**	-55 TO +125	LG	*1 nSEC WITH PULL-UP RESISTOR.	
	0.4	48 TO 96	0/0	TL	16	5**	-50 TO +125	CLG	**LOGIC CIRCUITRY NEEDS ONLY 1.5V. ***1.8 nSEC WITH PULL-UP RESISTOR.	
	2	42 TO 120	30 TO 60/0 TO 8	E	80	-4.5 ±10%	0 TO 70	G		
	8.5	28 TO 128	0 TO 30/0 TO 30	LE	*	-5.2 OR -4.7, ±5%	30 TO 125	GS**	*25Ω. **FLATPACK AVAILABLE.	
	4.25	28 TO 128	0 TO 30/0 TO 30	LE	*	-5.2 OR -4.7, ±5%	30 TO 125	GS**	ACE 33T20 HAS 320 BITS OF RAM, ACE 30T00 HAS 1280 BITS OF RAM.	
	0.8	40 TO 88	0/0	TL	24	4.75 TO 5.25	0 TO 70	PCLG	*3-INPUT NANDs.	
	1.2	28 TO 42	0/0	TL	8	4.75 TO 5.25	0 TO 70	P		
	0.67	38 TO 52	0/0	TL	8	4.5 TO 5.5	0 TO 70	PLG		

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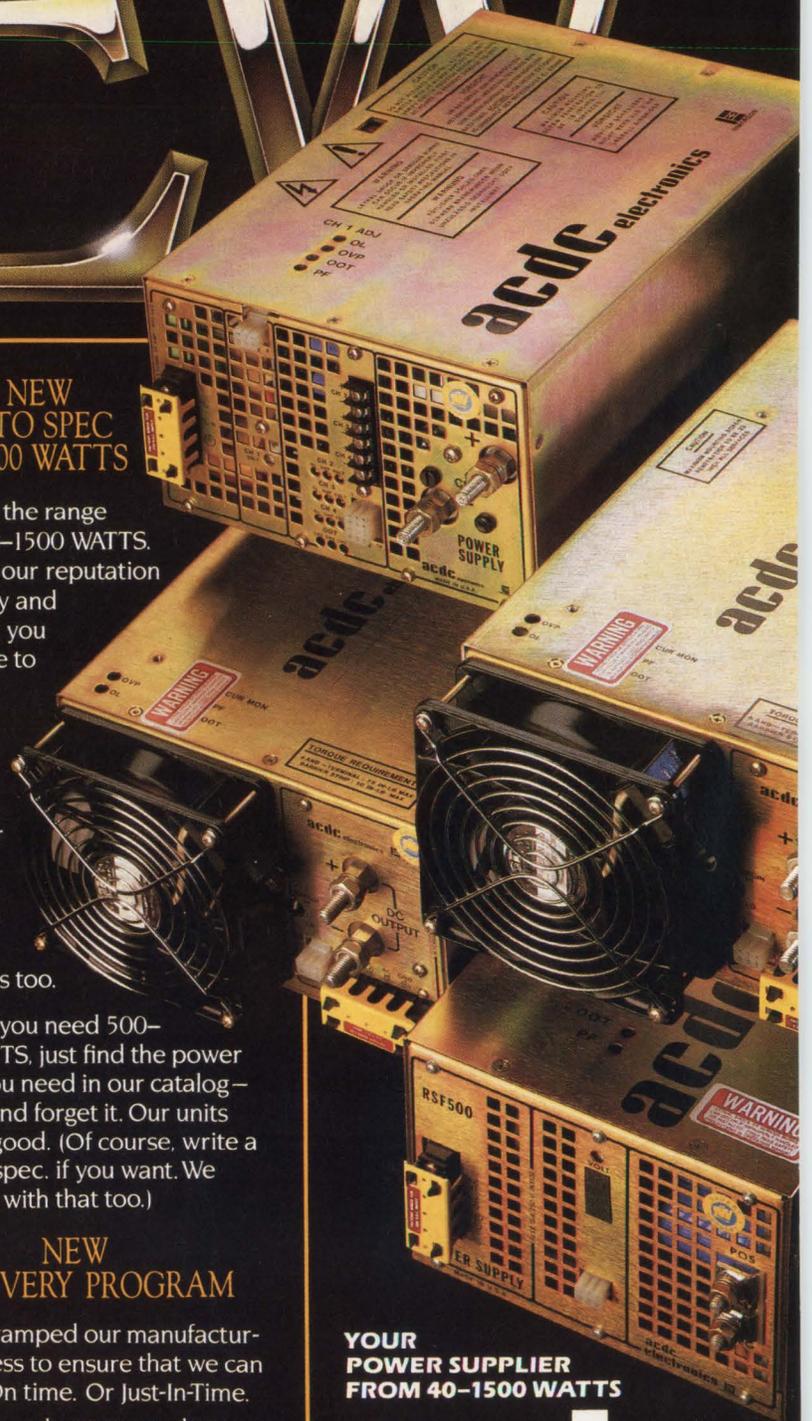
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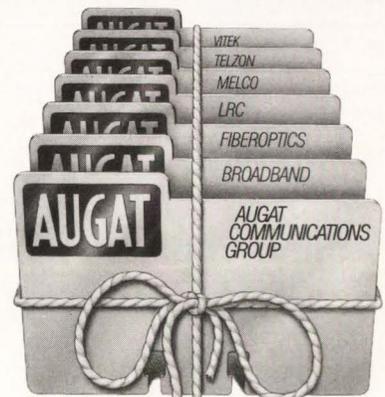
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EDN June 25, 1987

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CIRCLE NO 222

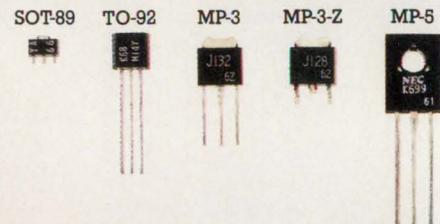
4V-driven power MOS FETs.

I _D (A)	V _{DSS} (V)				
	Package		30	60	100
0.5	TO-92		2SK679 (0.5Ω)		
	SOT-89		2SK680 (0.5Ω)		
1.0	SP-8		2SK681 (0.5Ω)		
	MP-3				2SK611 (3.0Ω) 2SK654 (1.3Ω)
		2SK738 (0.11Ω) 2SK801 (0.2Ω) 2SJ132 (0.25Ω)	2SK739 (0.17Ω) 2SJ133 (0.45Ω)	2SK612 (0.3Ω) 2SJ128 (0.8Ω)	
MP-5			2SK700 (0.6Ω) 2SK701 (0.4Ω)		2SK699 (0.8Ω)
				2SK704 (0.11Ω) 2SK705 (0.11Ω)*	2SK702 (0.2Ω) 2SK703 (0.2Ω)* 2SJ135 (0.25Ω)*
5	MP-25 MP-45*			2SJ134 (0.25Ω)	
6				2SJ137 (0.25Ω)* 2SJ139 (0.18Ω)*	
10				2SK689 (0.05Ω)* 2SJ136 (0.25Ω)	2SK737 (0.1Ω)* 2SK811 (0.1Ω)* 2SJ138 (0.18Ω)
12			2SJ141 (0.15Ω)*	2SJ142 (0.15Ω)* 2SK810 (0.1Ω)	
13				2SK591 (0.035Ω)* 2SK736 (0.08Ω)*	
14			2SJ143 (0.11Ω)* 2SJ140 (0.15Ω)		
15			2SK813 (0.06Ω)* 2SK817 (0.035Ω)*	2SK815 (0.06Ω)*	
16			2SK812 (0.06Ω)*		
19			2SK835 (0.014Ω) 2SK797 (0.014Ω)	2SK836 (0.025Ω) 2SK798 (0.025Ω)	
21					
26		MP-85			
27		MP-88			
40					

R_{DS(on)} typ, V_{GS}=10V

Streamline your driver and switching circuits.

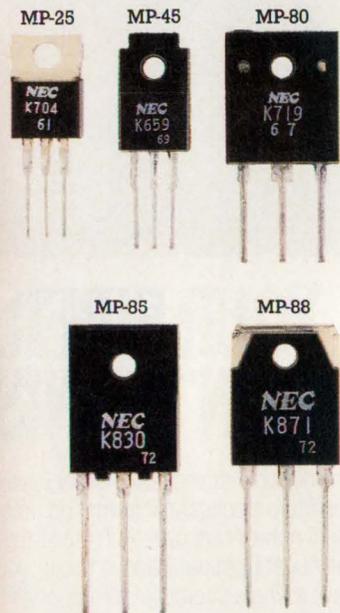
With NEC's new power MOS FETs. Featuring 4V gate-source bias, low on-resistance and reduced chip size.



High-voltage, low on-resistance power MOS FETs.

I _D (A)	V _{DSS} (V)					
	Package		250	450	500	900
3	MP-25 MP-45					2SK786 (6.0Ω) 2SK946 (4.5Ω)
4	MP-85 MP-88					2SK832 (3.2Ω) 2SK871 (4.5Ω)
5	MP-25 MP-80 MP-88		2SK854 (1.0Ω)	2SK855 (1.1Ω)		2SK719 (3.2Ω) 2SK833 (3.2Ω)
6	MP-88					2SK872 (2.0Ω)
8	MP-85 MP-88		2SK873 (0.9Ω)	2SK874 (1.0Ω)		2SK834 (1.2Ω) 2SK787 (1.25Ω)
10	MP-88		2SK735 (0.6Ω)	2SK819 (0.65Ω)		
12	MP-80		2SK799 (0.4Ω)	2SK773 (0.47Ω)		
	MP-85		2SK824 (0.4Ω)	2SK828 (0.47Ω)		
	MP-88		2SK875 (0.5Ω)	2SK876 (0.6Ω)		
15	MP-85		2SK826 (0.32Ω)	2SK830 (0.35Ω)		
	MP-88		2SK825 (0.4Ω)	2SK829 (0.47Ω)		
18	MP-80		2SK800 (0.32Ω)	2SK774 (0.35Ω)		
	MP-85	2SK820 (0.18Ω)	2SK837 (0.25Ω)	2SK838 (0.3Ω)		
	MP-88		2SK827 (0.32Ω)	2SK831 (0.35Ω)		
20	MP-80 MP-88		2SK720A (0.18Ω) 2SK821 (0.18Ω)	2SK784 (0.25Ω)	2SK785 (0.3Ω)	
22	MP-85		2SK822 (0.12Ω)			
25	MP-80		2SK707 (0.12Ω)			
	MP-88		2SK823 (0.12Ω)			

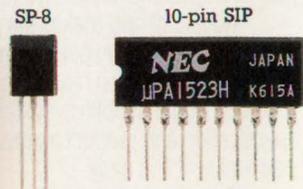
R_{DS(on)} typ, V_{GS}=10V

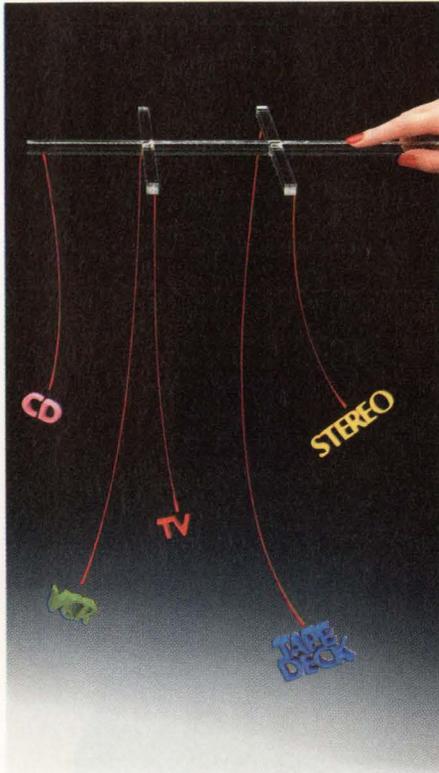


4V-driven power MOS FET arrays.

I _D (A)	V _{DSS} (V)					
	Package		30	60	80	100
2	10-pin SIP		μPA1520H (0.11Ω)	μPA1522H (0.17Ω)		μPA1526H (0.3Ω)
			μPA1570H (0.3Ω)	μPA1572H (0.4Ω)	μPA1524H (0.6Ω)	μPA1576H (0.8Ω)
			μPA1523H (0.4Ω)		μPA1527H (0.8Ω)	
5			μPA1552H (0.11Ω)			μPA1556H (0.2Ω)

R_{DS(on)} typ, V_{GS}=10V





Control the whole program.

NEC's programmable remote control transmitter ICs give you total control of home entertainment centers.

When king consumer kicks back, he wants total control over all the electronic entertainers in his castle. He wants TV, VCR, video disc, stereo, tape deck and CD all under the power of his magic wand. And means you need NEC's fully programmable ICs inside your infrared remote control transmitter.

Powerful 4-bit application-specific microcomputers, the μ PD6125 and 6126 are optimized for multi-function remote control units. They let you program transmission format freely and choose between 38kHz or 57kHz carrier frequency.

They have ample capacity to

handle all components. With 64 key inputs for the 6125. And 96 for the 6126. Both feature 1K \times 10-bit ROM, 32 \times 4-bit RAM, space-saving packages and low-power CMOS technology. Supply voltages range from 2V to 6V.

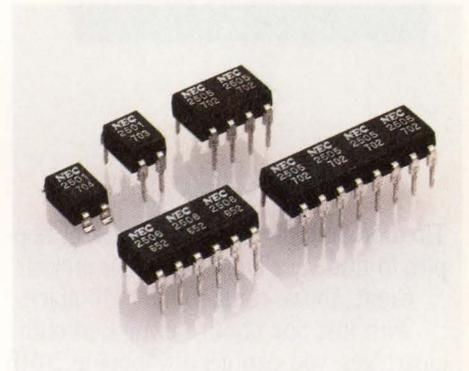
UNIFY YOUR SYSTEM.

A powerful remote control unit not only turns components on. It turns consumers on. It helps unify all the separate parts of your system into an irresistible whole. Find out how easy it is to control a larger share of the home entertainment market. With NEC's fully programmable remote control transmitter ICs.

Multi-channel photocouplers feature AC-input, high V_{CEO} and high CTR.

When your circuits need AC-input, high V_{CEO} or high CTR, just call NEC. We have the right multi-channel photocoupler design for you. We offer four series, each with 1-, 2-, 3- and 4-channel types. All come in DIPs for high-density

mounting. Lead-forming types are also available for surface mounting. Ensure ample isolation for your densely-populated boards with NEC's family of high-performance, multi-channel photocouplers.



Multi-channel photocouplers

Device	I_F (mA)	V_{CEO} (V)	I_C (mA)	BV (kV)	CTR (% typ)	Feature	Package
PS2501-1, -2, -3, -4	80	80	50	5 AC	300		4-, 8-, 12-, 16-pin DIP
PS2502-1	80	40	200	5 AC	2,000		4-, 8-, 12-, 16-pin DIP
PS2502-2, -3, -4			160				
PS2505-1, -2, -3, -4	80	80	50	5 AC	300	AC Input	4-, 8-, 12-, 16-pin DIP
PS2506-1	80	40	200	5 AC	2,000	AC Input	4-, 8-, 12-, 16-pin DIP
PS2506-2, -3, -4			160				

For further information, please contact:

■ USA Tel:1-800-632-3531. In California: Tel:1-800-632-3532. TWX: 910-379-6985.

■ Europe W. Germany Tel:0211-650302. Telex:8589960 NE D.
The Netherlands Tel:040-445-845. Telex:51923 NEC B NL.
Sweden Tel:08-732-8200. Telex:13839 NECSCAN S.
France Tel:1-3946-9617. Telex:699499 NEC EF.

Italy Tel:02-6709108. Telex:315355 NECEIT I.

UK Tel:0908-691133. Telex:826791 NECUK G.

■ Asia Hong Kong Tel:3-755-9008. Telex:54561 HKNEC HX.

Taiwan Tel:02-522-4192. Telex:22372 HKNEC TP.

Singapore Tel:4819881. Telex:39726 NECES RS.

■ Oceania Australia Tel:03-267-6355. Telex:AA38343 NECBCD.

NEC



40MB

You don't have to go to great heights to get great volume.



40MB

HP users, take heart.

Tired of shuffling through a stack of floppies to find your latest computer project?

Great. You've come to the right place.

With just one of our Bering Bernoulli cartridges, you can get a whopping 20MB of removable storage.

That's 25 times the storage you can get from a standard floppy. Or, about the same storage you can expect from one hard disk.

Which means our HP compatible storage systems can do much for those who need high capacity.

But that's just for openers.

Because Bernoulli cartridges are removable, you can take them anywhere. Or leave them right in your office.

You can lock them away in a safe. Or keep them from falling into the wrong hands. Something that's rather difficult to do with a hard disk.

Since a Bernoulli drive offers unlimited capacity, you won't run out of storage space the way you do with floppies or hard disks.

You won't have to worry about desk clutter, either.

And when it's time to backup your data, you simply slide in another cartridge. It's that simple.

Furthermore, Bernoulli aerodynamics result in less wear and a longer life for both drive and media.

So whether you're an HP9000 (Series 200/300/500), HP1000, HP3000 or Integral PC user, our high performance drives provide a complete solution for primary and backup storage.

For instance, you can get a dual 20MB TwinPac (5840-RM) or a single 20MB UniPac (5820-RM) removable drive.

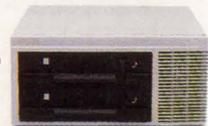
Both are fast, reliable, versatile and removable.

For higher capacities, our MultiPac drives feature a Bernoulli 20MB drive and a hard disk in one convenient package. Our 5204 model has a 40MB hard disk for a 60MB total drive. And our 5205 model includes a 57MB drive for those requiring a 77MB system.

Naturally, there's a lot more to know about our drives. So if you're interested, and you'd like more information, call or write today. It's a great way to go.

Bering Industries, Inc., 280 Technology Circle, Scotts Valley, CA 95066. Inside California, call 800 533-DISK. Outside California, call 800 BERING 1.

BERINGTM
A MOUNTAIN COMPUTER, INC. COMPANY



Innovative Storage for Hewlett-Packard.

UniPac, TwinPac and MultiPac are trademarks of Bering Industries, Inc. HP9000, HP1000 and HP3000 Integral PC are trademarks of Hewlett-Packard. © 1987 Bering Industries, Inc.



EDN GATE-ARRAY DIRECTORY

Advanced Micro Devices Inc

Bipolar arrays:
901 Thompson Pl
Sunnyvale, CA 94088
(408) 732-2400
Circle No 660

CMOS arrays:
5900 E Ben White Blvd
Austin, TX 78741
(512) 462-5815
Circle No 661

CUSTOMER/VENDOR INTERFACE

PREFERRED: Simulated net list.

ACCEPTABLE: Layout generated by customer's software.

DISCOURAGED: Functional block diagram, unsimulated schematic, layout generated by vendor's software, PG tapes.

DESIGN TOOLS

Customers use LDS software for schematic capture, simulation, timing analysis, layout, and test-program generation.

WORKSTATION SUPPORT

Daisy, Mentor, Valid, IBM PC.

DESIGN CYCLE

CUSTOMER PERFORMS USING OWN TOOLS: (Bipolar arrays) Logic design and simulation, timing analysis, test-pattern generation, and (optionally) placement and routing.

CUSTOMER PERFORMS USING VENDOR'S TOOLS: (CMOS arrays) Logic design, simulation, test-program generation, and checking.

VENDOR PERFORMS: Placement and routing, network-equivalence check, and post-layout simulation.

TRAINING

COURSE: You can attend a 4-day course in Austin, TX. Other training performed on individual basis.

DOCUMENTATION: Design manuals available; no commitment necessary.

SUPPORT FACILITIES

Austin, TX, and Sunnyvale, CA.

CYCLE TIMES

DESIGN: 1 to 3 weeks, CMOS; 4 to 6 weeks, bipolar.

PROTOTYPING: 5 to 8 weeks, CMOS; 4 to 6 weeks, bipolar.

INPUTS FOR COST ESTIMATE

Array and package type, volume, schedule, temperature range, screening requirements.

ALTERNATE SOURCES

CMOS: LSI Logic

Applied Micro Circuits Corp

5502 Oberlin Dr
San Diego, CA 92121
(619) 450-9333
Circle No 662

CUSTOMER/VENDOR INTERFACE

PREFERRED: Converted net list with vectors, circuit specification, and logic diagrams.

DESIGN TOOLS

Macromatrix design kit includes engineering-rules and design-rules checking, front annotation, and test-program formatting.

WORKSTATION SUPPORT

Mentor, Daisy, Valid, Tektronix/CAE, and Tegas 5 simulator.

DESIGN CYCLE

CUSTOMER PERFORMS USING OWN TOOLS: Schematic capture, simulation, and test-vector generation.

CUSTOMER PERFORMS USING OWN OR VENDOR'S TOOLS: Engineering- and design-rule checks, net-list generation, front-annotation calculation.

VENDOR PERFORMS: Layout, fault grading.

FUNCTION LIBRARIES

Q1500 Series ECL: Library includes 125 functions built from as many as 750 gates; users can define new functions using existing library elements; simulation parameters include ID, SUH, PD, FO.

Q700 Series ECL: Library includes 115 functions built from as many as five 2-input gates; users can define new functions using existing library elements; simulation parameters include ID, SUH, PD, and FO.

TRAINING

COURSE: A 5-day session is available in San Diego, CA; no design commitment needed.

DOCUMENTATION: Design manuals and application notes are available before design commitment.

SUPPORT FACILITIES

San Diego, CA.

CYCLE TIMES

DESIGN: 2 to 5 weeks.

PROTOTYPING: 5 to 8 weeks.

INPUTS FOR COST ESTIMATION

Logic schematics, product specifications, quantities, and delivery schedules.

PRODUCTION COMMITMENTS

None required.

ALTERNATE SOURCES

Signetics Corp and Thomson CSF; alternate sourcing effected through PG-tape transfer.

Array Technology

1297 Parkmoor Ave
San Jose, CA 95126
(408) 297-3333
Circle No 663

CUSTOMER/VENDOR INTERFACE

PREFERRED: Schematic or logic diagram.

DISCOURAGED: Net list.

DESIGN TOOLS

CAE software provides schematic-capture, net-list generation, simulation, layout, and Fairchild-Sentry test-program-generation capabilities. CAE access occurs through alphanumeric terminals.

WORKSTATION SUPPORT

Mentor Graphics.

DESIGN CYCLE

CUSTOMER PERFORMS USING VENDOR'S TOOLS: All logic design, simulation, test-program generation, and layout tasks.

VENDOR PERFORMS: Logic minimization, custom cell creation; any other steps at customer's option.

FUNCTION LIBRARIES

Library contains 74 functions built from as many as 47 2-input gates; users can define new functions using existing library elements or discrete gates; all elements have been built and tested; simulation parameters include ID, LD, SUH, VS, TS, PD, FI, and FO.

EDN GATE-ARRAY DIRECTORY

TRAINING

COURSE: A 5-day session is included in design fees; course is offered in San Jose, CA.

DOCUMENTATION: Design manuals are available upon design commitment.

SUPPORT FACILITIES

San Jose, CA.

CYCLE TIMES

DESIGN: 6 to 12 weeks.

PROTOTYPING: 3 weeks.

INPUTS FOR COST ESTIMATION

Gate count and package type.

PRODUCTION COMMITMENTS

Nonrecurring engineering charge is lower with design commitment.

ALTERNATE SOURCES

NCR Corp; alternate sourcing effected through PG-tape transfer.

Barvon Research Inc

1992 Tarob Ct
Milpitas, CA 95035
(408) 262-8368
Circle No 664

CUSTOMER/VENDOR INTERFACE

PREFERRED: Layout data generated by vendor's software.

ACCEPTABLE: Functional block diagram, simulated or un-simulated schematic or net list, layout data generated by customer's tools, PG tapes.

DESIGN TOOLS

Barvon provides tools accessible through timesharing on Control Data Corp's Cybernet; internal tools support cell compaction for chip-size reductions to 45%.

WORKSTATION SUPPORT

Apollo, Metheus, Valid, and Mentor workstations; layout data includes cell outlines only; internal cell data available after contract negotiation.

DESIGN CYCLE

CUSTOMER PERFORMS USING OWN TOOLS: Partitioning analysis, functional simulation.

CUSTOMER PERFORMS USING VENDOR'S TOOLS: Logic design.

VENDOR PERFORMS: All simulation, testability-analysis, test-program design, and post-layout analysis functions.

FUNCTION LIBRARIES

Library contains functions built from as many as 180 2-input gates; users can define new functions based on existing library elements; 85% of library cells have been built and tested; simulation parameters include ID, LD, SUH, VS, TS, PD, FI, and FO.

TRAINING

COURSE: A 3-day course is available in San Jose, CA prior to design commitment; \$1000.

DOCUMENTATION: Manuals available before design commitment; \$500, updated monthly.

SUPPORT FACILITIES

Santa Clara, CA.

CYCLE TIMES

DESIGN: 2 to 3 weeks.

PROTOTYPING: 5 to 6 weeks.

INPUTS FOR COST ESTIMATION

Gate count, memory requirements.

PRODUCTION COMMITMENTS

None required.

ALTERNATE SOURCES

None.

California Devices Inc

1051 S Milpitas Blvd
Milpitas, CA 95035
(408) 945-5000
Circle No 665

CUSTOMER/VENDOR INTERFACE

PREFERRED: Simulated schematic or net list using vendor's macrocells.

DESIGN TOOLS

CDI uses Hilo-3, SC MEDS, and Maskap V for simulation, physical design, and verification; design system runs on DEC VAX minicomputers.

WORKSTATION SUPPORT

Daisy, Mentor, Valid, and Tektronix/CAE.

DESIGN CYCLE

CUSTOMER PERFORMS USING OWN TOOLS: Partitioning analysis, logic design and simulation, timing analysis, testability analysis, placement and routing, network-equivalence check, and post-routing simulation.

CUSTOMER PERFORMS USING OWN OR VENDOR'S TOOLS: Above plus test-pattern generation and custom-cell creation.

VENDOR PERFORMS: Any design step at customer's option.

FUNCTION LIBRARIES

Library includes 200 functions built from as many as 208 2-input gates; users can define new functions using existing library elements or discrete gates; 100% of library cells have been built and tested; simulation parameters include ID, LD, SUH, VS, TS, FI, and FO.

TRAINING

COURSE: Four courses range from 1 to 5 days.

DOCUMENTATION: Design manuals available prior to design commitment.

SUPPORT FACILITIES

San Jose, CA, and Boston, MA.

CYCLE TIMES

DESIGN: 1 to 8 weeks.

PROTOTYPING: 3 weeks.

INPUTS FOR COST ESTIMATION

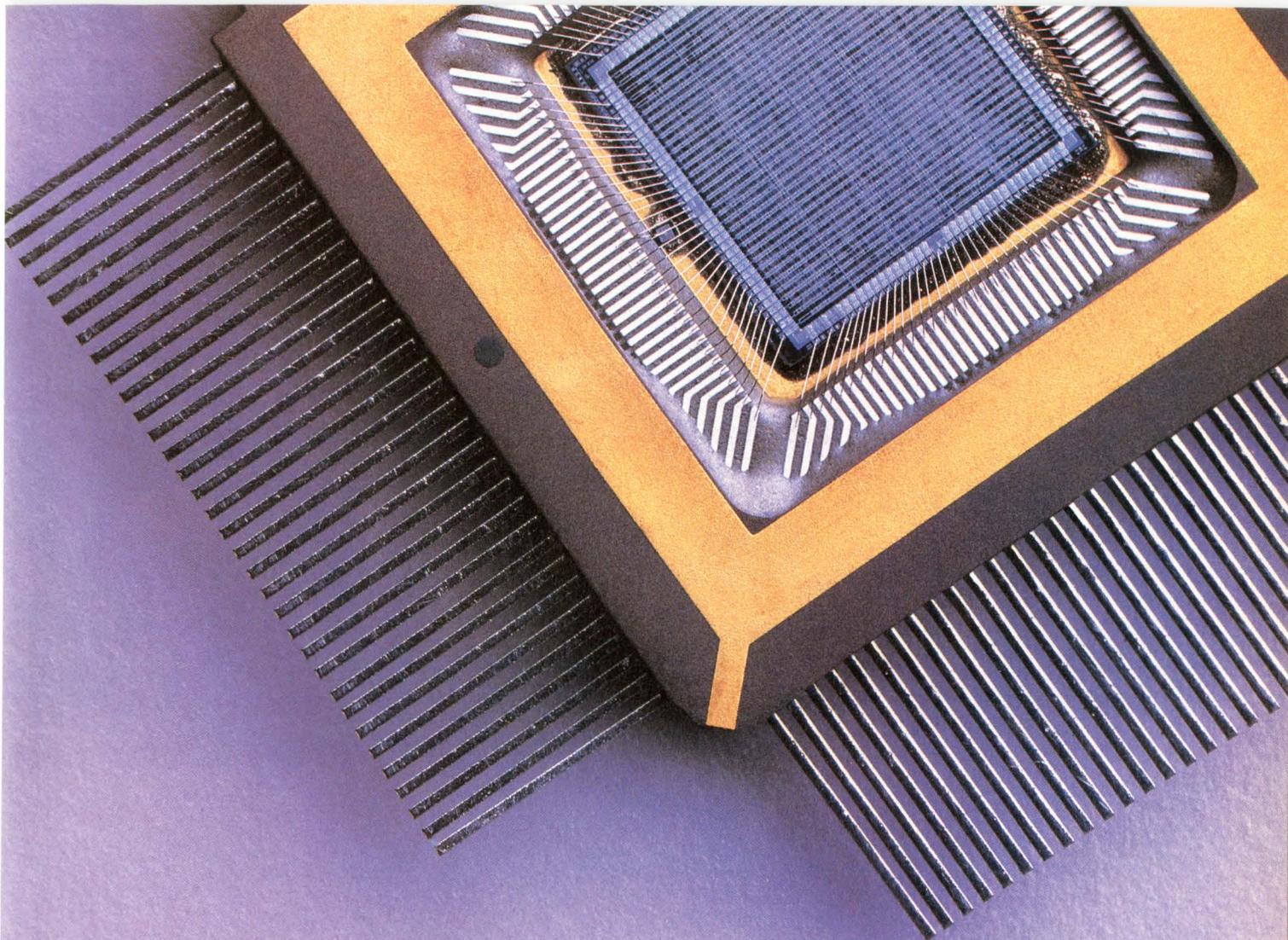
Gate and pin count, operating temperature and voltage range, I/O specifications, screening requirements.

PRODUCTION COMMITMENTS

None.

Cherry Semiconductor Corp

2000 S County Trail
East Greenwich, RI 02818
(401) 885-3600
Circle No 666



A rad-hard gate array with only one set of standards. Military.

Our UTB-R radiation-hardened gate array family is born to the highest military standards. It is functional to a total dose of 10^6 rads (Si) and operates to data sheet specifications at 2×10^7 (Si) rads.

Producing gate arrays for military and aerospace customers is nothing new to UTMIC. For years we've been providing high-reliability ICs for divisions of United Technologies Corporation.

Screened to selected tests in MIL-STD-883C, the UTB-R family's patented continuous-column architecture

increases density without sacrificing routability. It uses transistors to isolate signals and allows you to get up to 95% gate utilization.

We combine high speed with low-power consumption of CMOS double-level-metal technology. And, our VAX[®]-based HIGHLANDSM Design System, which supports front-end design on major workstations, enables maximum design flexibility.

Equivalent 2-input NAND gates range from 1,000 to 7,600, and package options include DIPs, LCCs, PGAs, and Cerquads.

Don't compromise your standards. Choose the rad-hard gate array born to the military—the UTB-R Series.

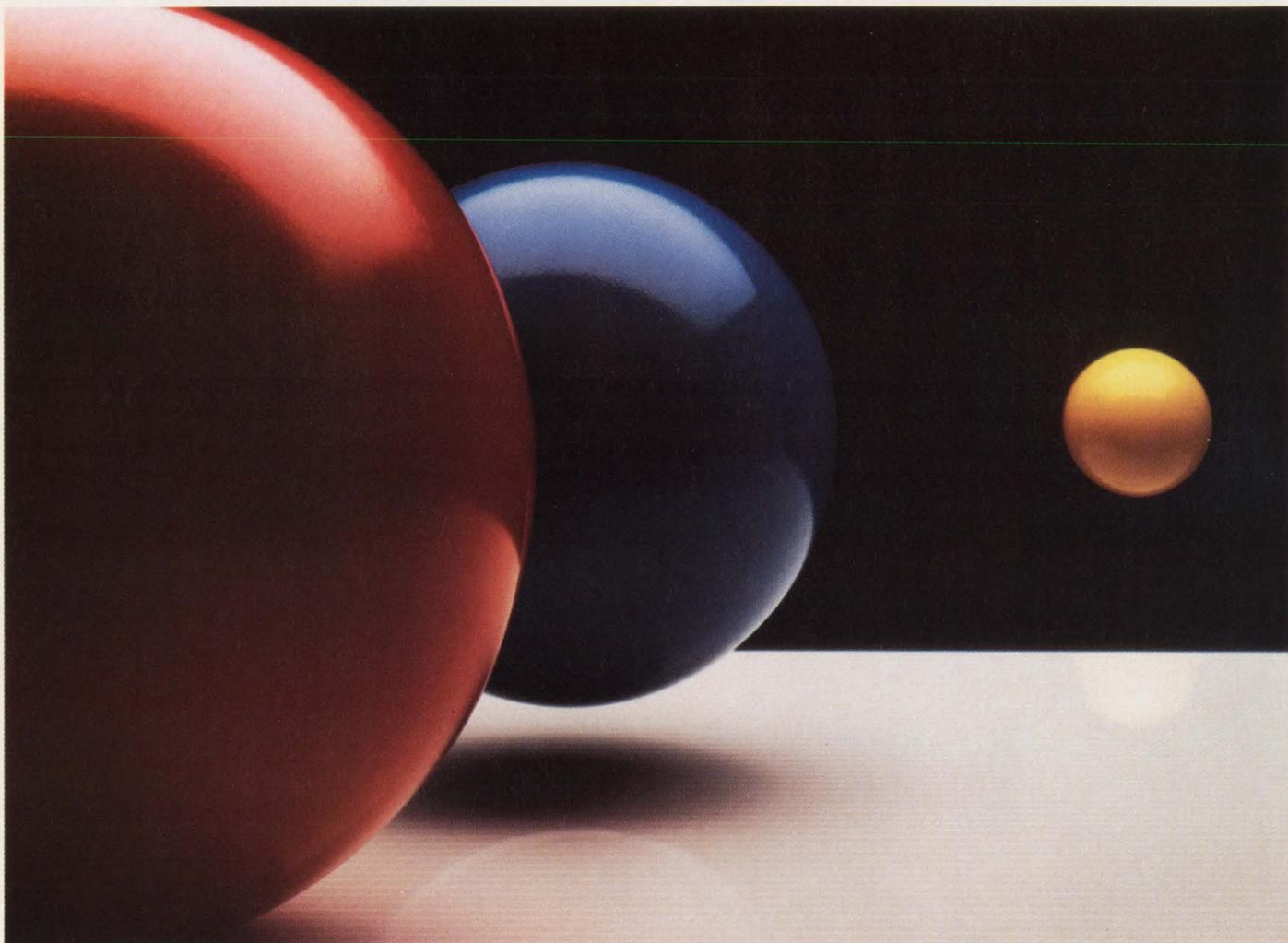
United Technologies
Microelectronics Center
1575 Garden of the Gods Road
Colorado Springs, CO 80907

1-800-MIL-UTMC



**UNITED
TECHNOLOGIES
MICROELECTRONICS
CENTER**

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Good ideas come in smaller case sizes from the capacitor choice.

Nothing moves a product to market faster than timely good ideas.

That's why some of our biggest good ideas in capacitors now come in smaller packages. Features that can offer you new opportunities for improving designs, controlling costs and automatically inserting more high CV capacitors than ever before.

A perfect example is our VX miniature aluminum electrolytic capacitor series. These compact, general purpose, radial lead capacitors have been designed to be everything you expect a high-quality, high-reliability capacitor to be.

They meet JIS C-5141 and 5102 industry standards. 2,000 hour load




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The capacitor choice.

life test requirements. And include, both, our Anti-Solvent design feature, which resists harmful cleaning agents, and our unique safety vent design on units with diameters of 6.5mm and larger.

Or, if you need reliable performance up to +105°C, specify our VT Series.

Ask your Nichicon representative or distributor for your free copies of our VX and VT Series data sheets. Or call us at (312) 843-7500.

But we warn you, once you've considered the VX Series' size, performance specifications and price, you may think they sound like an impossibly good deal.

But then, we designed them that way.

927 E. State Parkway • Schaumburg, IL 60173 • (312) 843-7500

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One good idea after another.

CIRCLE NO 14

EDN GATE-ARRAY DIRECTORY

CUSTOMER/VENDOR INTERFACE

PREFERRED: Logic schematic, system definition and block diagram, IC schematic.

DESIGN TOOLS

Applicon AGS, Pspice, IS-Spice.

WORKSTATION SUPPORT

Applicon 860 and 870.

DESIGN CYCLE

CUSTOMER PERFORMS USING OWN TOOLS: Partitioning analysis, logic design, simulation, timing analysis, logic minimization, critical-path analysis.

CUSTOMER PERFORMS USING VENDOR'S TOOLS: Layout.

VENDOR PERFORMS: Integration and packaging.

TRAINING

COURSE: None offered.

SUPPORT FACILITIES

None.

CYCLE TIMES

DESIGN: 12 to 15 weeks.

PROTOTYPING: 14 weeks.

INPUTS FOR COST ESTIMATION

Estimated gate complexity, packaging, pin count.

PRODUCTION COMMITMENTS

Depends on vendor's involvement in design process.

ALTERNATE SOURCES

Genesis 1200, 1300, and 1400: Exar

Other arrays: Exar, Ferranti/Interdesign, MCE Semiconductor; alternate sourcing effected through layout-data transfer.

Circuit Technology Inc

160 Smith St
Farmingdale, NY 11735
(516) 293-8686
Circle No 667

CUSTOMER/VENDOR INTERFACE

PREFERRED: Simulated schematic or net list.

DISCOURAGED: Black-box specification.

DESIGN TOOLS

CTI's CAE system contains cell libraries, automatic layout, network-equivalency checks, and automatic test-program generation. Tools include Hilo-2 and Hilo-3, Cadisys, and Cadigraph in addition to the Applicon AGS860 and NCA software.

WORKSTATION SUPPORT

Mentor, Daisy, Silvar-Lisco.

DESIGN CYCLE

CUSTOMER PERFORMS USING OWN TOOLS: Partitioning analysis, functional simulation, logic design, logic simulation.

CUSTOMER PERFORMS USING VENDOR'S TOOLS: Above plus testability analysis, timing analysis, fault grading.

VENDOR PERFORMS: Placement and routing, custom-cell creation, network-equivalence check, and post-routing simulation.

FUNCTION LIBRARIES

Library includes more than 100 functions built from as many as 66 2-input gates; users can define new functions based on existing library elements or discrete gates; all elements have been built and tested; simulation parameters include ID, LD, SUH, FI, and FO.

TRAINING

COURSE: 12 courses available with documentation.

DOCUMENTATION: Design manuals available without design commitment; \$250.

SUPPORT FACILITIES

Farmingdale, NY.

CYCLE TIMES

DESIGN: 3 weeks typ.

PROTOTYPING: 10 weeks.

INPUTS FOR COST ESTIMATION

Schematics, electrical specifications, environmental specifications, packaging, and screening requirements.

PRODUCTION COMMITMENT

None.

Custom Integrated Circuits

5343 Wayzata Blvd
Minneapolis, MN 55416
(612) 542-1115
Circle No 668

CUSTOMER/VENDOR INTERFACE

PREFERRED: Simulated schematic or net list.

ACCEPTABLE: Functional block diagram, unsimulated schematic or net list, layout data, PG tapes.

WORKSTATION SUPPORT

Layout data available for Calma CAD systems and systems running Logcap or Tegas software.

DESIGN CYCLE

CUSTOMER PERFORMS USING OWN TOOLS: Partitioning analysis, block-level functional simulation, logic design and simulation, timing analysis, logic-fault grading, test-program generation, custom cell creation, network-equivalency check, post-routing simulation, and timing routing.

VENDOR PERFORMS: Array routing.

FUNCTION LIBRARY

I²L: Library includes 35 cells built from as many as 300 2-input gates; users can define new functions using existing library elements or discrete gates; 90% of library cells have been built and tested; simulation parameters include ID, LD, VS, TS, PD, FI, and FO.

CMOS: Library includes 50 cells built from as many as 400 2-input gates; users can define new functions using existing library elements or discrete gates; 90% of library cells have been built and tested; simulation parameters include ID, LD, SUH, PD, FI, and FO.

TRAINING

COURSE: None offered.

SUPPORT FACILITIES

Custom Integrated Circuits maintains a design center in Minneapolis, MN.

CYCLE TIMES

DESIGN: 4 to 20 weeks.

PROTOTYPING: 4 to 8 weeks.

INPUTS FOR COST ESTIMATION

Specifications.

PRODUCTION COMMITMENTS

None required.

EDN GATE-ARRAY DIRECTORY

Custom MOS Arrays Inc

211 Topaz St
Milpitas, CA 95035
(408) 946-9111
Circle No 669

CUSTOMER/VENDOR INTERFACE

PREFERRED: Simulated schematic or net list with test vectors.

ACCEPTABLE: Unsimulated schematic or net list, layout generated by vendor's software, PG tapes.

WORKSTATION SUPPORT

Valid, Daisy, Tektronix/CAE.

DESIGN CYCLE

CUSTOMER PERFORMS USING VENDOR'S TOOLS: Partitioning analysis, functional simulation, logic design.

VENDOR PERFORMS: Logic design and simulation, timing analysis, testability analysis, test-program generation, fault analysis, all subsequent physical-design tasks.

FUNCTION LIBRARY

Library includes 275 functions built from as many as 1000 2-input gates; users can build new functions based on existing library elements or discrete gates; all elements have been built and tested; simulation parameters include ID, LD, SUH, VS, TS, PD, FI, and FO.

TRAINING

COURSE: A 5-day course is available.

DOCUMENTATION: Design manuals are available.

CYCLE TIMES

DESIGN: 2 to 12 weeks.

PROTOTYPING: 2 to 6 weeks.

INPUTS FOR COST ESTIMATION

Package type, gate count, screening-test requirements, production volumes.

PRODUCTION COMMITMENTS

None.

Custom Silicon Inc

600 Suffolk St
Lowell, MA 01854
(617) 454-4600
Circle No 670

CUSTOMER/VENDOR INTERFACE

PREFERRED: Block diagrams, net lists.

DESIGN TOOLS

Schematic capture, net-list generation, simulation, layout, and test-program generation.

WORKSTATION SUPPORT

Daisy, Mentor.

DESIGN CYCLE

CUSTOMER PERFORMS USING OWN TOOLS: Specification, logic design, schematic capture, simulation, and test-program generation.

CUSTOMER PERFORMS ON VENDOR'S TOOLS: Schematic capture, simulation, and test-program generation.

VENDOR PERFORMS: Partitioning, schematic capture, simulation, test-program generation, and physical design.

TRAINING

COURSE: On individual basis.

DOCUMENTATION: Manuals available.

SUPPORT FACILITIES

Boston, MA; Vancouver, WA; Bellevue, WA; and Worthington, OH.

CYCLE TIMES

DESIGN: 4 to 9 weeks.

PROTOTYPING: 5 to 7 weeks.

INPUTS FOR COST ESTIMATION

Circuit and system functions, gate count, ac requirements, dc requirements, and packaging.

PRODUCTION COMMITMENTS

None.

Electronic Technology Corp

2037 North Towne Lane NE
Cedar Rapids, IA 52402
(319) 395-0567
Circle No 671

CUSTOMER/VENDOR INTERFACE

PREFERRED: Functional block diagram, schematic.

DESIGN TOOLS

Simulation, Spice analysis, automatic routing, and design-rule checking.

WORKSTATION SUPPORT

Daisy, Mentor, and Calma GDS I and II.

DESIGN CYCLE

CUSTOMER PERFORMS USING OWN TOOLS: Partitioning analysis, functional simulation, logic design and simulation, timing analysis, critical-path analysis, and test-program generation.

CUSTOMER PERFORMS USING VENDOR'S TOOLS: All of above plus placement, routing, and network-equivalence check.

VENDOR PERFORMS: Custom-cell generation and PG-tape conversion.

TRAINING

COURSE: 2-day course in Cedar Rapids, IA.

DOCUMENTATION: Available.

SUPPORT FACILITIES

Cedar Rapids, IA, and Chicago, IL.

CYCLE TIMES

DESIGN: 1 to 3 weeks.

PROTOTYPING: 5 to 7 weeks.

INPUTS FOR COST ESTIMATION

Preliminary diagram, gate count, packaging, and volume.

PRODUCTION COMMITMENTS

None.

Exar Corp

750 Palomar Ave
Sunnyvale, CA 94088
(408) 732-7970
Circle No 672

CUSTOMER/VENDOR INTERFACE

PREFERRED: For digital arrays, schematic or net list. For linear arrays, completed layout design on hook-up sheets.

DESIGN TOOLS

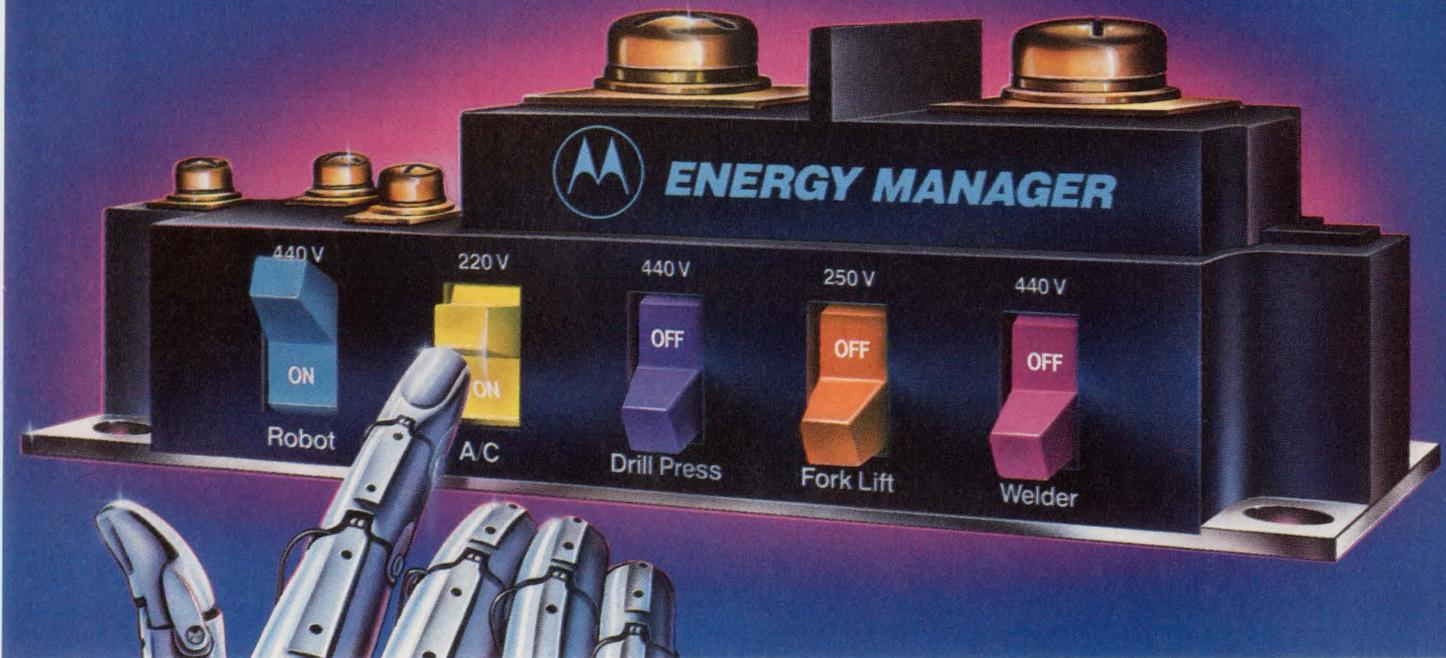
Simulation tools on VAX 8600 computer.

WORKSTATION SUPPORT

Daisy.



MOTOROLA



Master mechanics' power tool.

EMS modules do blue-collar jobs with ease.

Use rugged, reliable EMS modules to handle industrial-strength DC or off-line AC inductive loads up to 75 kW. Cut size, cost and complexity of systems, eliminate individual components and wiring and simplify circuitry.

Such as in uninterruptible power supplies, six-step and PWM motor controls, numerical controls, induction heating, discrete transistor and thyristor-replacement circuits for high-energy air conditioners, industrial ventilation systems, drill presses, robots, welding equipment and many others.



What's simplest costs least.

Heavy-duty EMS modules, replacing up to ten or more individual devices, plus wiring, contain single, dual, four or six pack configurations. They're rated at 2,500 V RMS isolation for one minute—sufficient to meet regulatory agencies' applications.

What's most important, EMS saves you time and money in system design, complexity and size. And they cut field service, that added-cost bugaboo that haunts every factory floor and dirty environment.

They're 15 to 300 A rated with sustaining voltages from 450 to 1,200 V.

Darlington and tri-stage combinations provide 80-100 min gain at rated current, crucial in motor control systems.

EMS power of choice.

All Motorola's renowned power device technologies will be available in EMS: bipolar, TMOS™ powerFET, TMOS-driven bipolar transistor combinations and our GEMFET™ (IGBT)—a high-input-impedance MOSFET that cuts output conduction losses up to 10 times.

Initial introductions encompass 24 bipolar devices in ten packages with future units capable of 1,400 V_{CEX}.

Equally important, Motorola EMS modules offer both industry-accepted terminal styles for optimum connection flexibility.

One-on-one design-in help.

Anywhere in the U.S. or Canada, get an engineer-to-engineer update on the

1-800-521-6274

latest Motorola power device technologies. Call toll-free any weekday, 8:00 to 4:30 p.m., MST.

Send the coupon to Motorola Semiconductor Products, Inc., P.O. Box 20912, Phoenix, AZ 85036 for data.

We're on your design-in team.



MOTOROLA

To: Motorola Semiconductor Products, Inc.
P.O. Box 20912, Phoenix, AZ 85036

Please send me more information on Motorola Energy Manager Series.

325EDN062587

Name _____

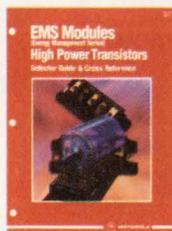
Title _____

Company _____

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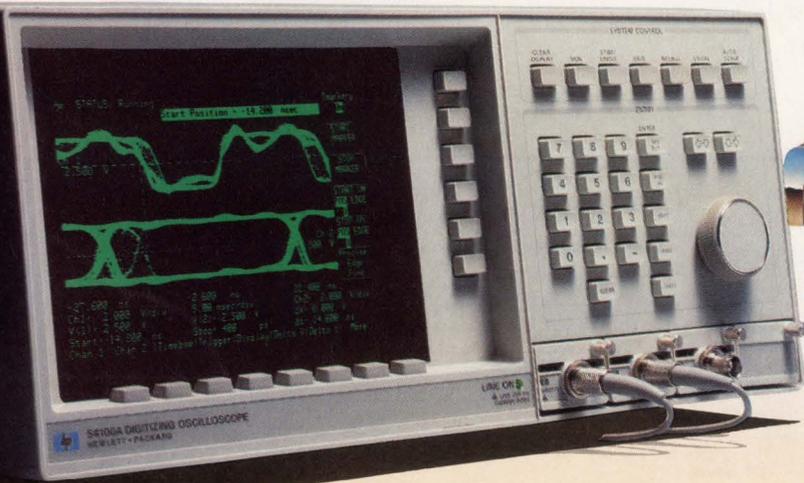
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E115708

CIRCLE NO 225

EDN GATE-ARRAY DIRECTORY

DESIGN CYCLE

CUSTOMER PERFORMS USING OWN TOOLS: Partitioning analysis, logic design and simulation, testability analysis, and test-pattern generation.

VENDOR PERFORMS: Above steps at customer's option, placement and layout, design verification.

TRAINING

COURSE: None.

DOCUMENTATION: Design manuals available prior to design commitment; \$59.

SUPPORT FACILITIES

Design center in England.

CYCLE TIMES

DESIGN: 4 to 6 weeks.

PROTOTYPING: 6 weeks.

INPUTS FOR COST ESTIMATION

Schematic, packaging, test parameters, and production volume.

PRODUCTION COMMITMENTS

25,000 units.

ALTERNATE SOURCES

All products: R-Ohm, mask transfer.

Linear products except V100, X100, W100, and XR400: Ferranti Interdesign, layout-data transfer.

ꝑL products: Cherry Semiconductor, layout-data transfer.

Fairchild Camera and Instrument Corp

1801 McCarthy Blvd
Milpitas, CA 95035
(408) 433-2500
Circle No 673

CUSTOMER/VENDOR INTERFACE

PREFERRED: Simulated schematic or net list.

ACCEPTABLE: Unsimulated schematic or net list.

DISCOURAGED: Functional block diagram, layout data generated by customer's software, PG tapes.

DESIGN TOOLS

Fairchild's technology-independent CAE system supports schematic entry, database creation, simulation, testability analysis, automatic layout, and post-routing analysis. Users connect to the system using alphanumeric or high-resolution graphics terminals. You can lease Fairchild's design system to run on your MicroVAX or other VMS computer.

WORKSTATION SUPPORT

Mentor, Daisy, Valid, and FutureNet; cell-outline data available for Silver-Lisco layout systems; internal cell data is available upon nondisclosure agreement.

DESIGN CYCLE

CUSTOMER PERFORMS USING OWN TOOLS: Partitioning analysis, block-level functional simulation, logic minimization, test-program generation, testability analysis.

CUSTOMER PERFORMS USING VENDOR'S TOOLS: Logic design, simulation, timing and critical-path analysis, testability analysis, fault grading, interactive or automatic routing, post-routing simulation.

VENDOR PERFORMS: Custom cell creation.

FUNCTION LIBRARIES

ECL: Library includes 100 functions built from as many as 60 2-input cells; users can define new functions using existing library elements; half of all library cells have been built and tested; simulation parameters include ID, LD, PD, FI, FO, and process sensitivity.

CMOS: Library includes 100 cells built from as many as 100 gates; users can define new functions based on existing elements; 50% of the library has been fabricated and tested; simulation parameters include ID, LD, SUH, PD, FI, FO, and process sensitivity.

TRAINING

COURSE: A 2-day course (\$300) in ECL design and a 1-day course (\$200) in CMOS design are available at Fairchild's gate-array design centers.

DOCUMENTATION: Design manuals are available upon design commitment.

SUPPORT FACILITIES

Cupertino, CA; Milpitas, CA; Waltham, MA; Costa Mesa, CA; Richardson, TX; Bloomington, MN; Orlando, FL; Tokyo, Japan; Reading, UK; Taipei, Taiwan.

CYCLE TIMES

DESIGN: 3 to 6 weeks depending on vendor/customer interface.

PROTOTYPING: 6 to 8 weeks.

INPUTS FOR COST ESTIMATION

Approximate gate count, device type, production volume, screening requirements.

PRODUCTION COMMITMENTS

None required.

ALTERNATE SOURCES

ECL arrays: Honeywell.

CMOS arrays: VTI.

Ferranti Interdesign Inc

1500 Green Hills Rd
Scotts Valley, CA 95066
(408) 438-2900
Circle No 674

CUSTOMER/VENDOR INTERFACE

PREFERRED: Simulated schematic, truth tables and timing diagrams, transistor-level schematic for linear arrays, breadboard for linear/digital arrays.

DISCOURAGED: Functional block diagram, unverified design.

DESIGN TOOLS

Proprietary design system runs on VAX and performs functional and dynamic simulation. Front-end design is possible on IBM PCs and Mentor workstations. Applicon systems and ECAD software support back-end design.

WORKSTATION SUPPORT

Digital arrays: FutureNet, Mentor. **Bipolar digital and linear arrays:** Mentor, Daisy, Valid. **Linear arrays:** Analog Workbench.

DESIGN CYCLE

CUSTOMER PERFORMS USING OWN TOOLS: Partitioning analysis, schematic capture.

CUSTOMER PERFORMS USING VENDOR'S TOOLS: Logic design, timing analysis, critical-path analysis, testability analysis, test-pattern generation, custom cell creation, interactive layout of some arrays.

VENDOR PERFORMS: All simulations, chip layout and post-layout analysis; any design or simulation steps at user's option.

FUNCTION LIBRARY

Each library contains as many as 65 SSI functions; users can define new functions using existing library elements or discrete gates; simulation parameters include ID, LD, TS, VS, PD, FI, and FO.

TRAINING

DOCUMENTATION: MMK Design Manual is available prior to design commitment; \$99.

EDN GATE-ARRAY DIRECTORY

SUPPORT FACILITIES

Scotts Valley, CA, and Commack, NY.

CYCLE TIMES

DESIGN: 4 to 8 weeks, depending on vendor involvement.
PROTOTYPING: 4 to 8 weeks.

INPUTS FOR COST ESTIMATION

Schematic, circuit and I/O specifications, packaging, temperature range, and testing requirements.

PRODUCTION COMMITMENTS

500 pieces/year required or preferred, depending on array type.

ALTERNATE SOURCES

MC and MO Series: MCE Semiconductors and Exar; alternate sourcing effected through layout-data transfer.

MP Series: GTE Microcircuits; alternate sourcing effected through mask, PG tape, layout-data, or net-list transfer.

Fujitsu Microelectronics Inc

3200 Scott Blvd
Santa Clara, CA 95054
(408) 727-1700
Circle No 675

CUSTOMER/VENDOR INTERFACE

ACCEPTABLE: Unsimulated schematic or net list; simulated schematic or net list. Designs in Tegas format also accepted.

DISCOURAGED: Functional block diagram, layout data, PG tapes.

DESIGN TOOLS

Fujitsu releases the specifications for its high-level language (FLDL) that accommodates circuit descriptions compatible with in-house simulation and layout tools; users create FLDL files using any text editor and transmit files to Fujitsu on block-format 1600-bps magnetic tapes. The firm also offers a test-description language (FTDL) for test-program transfers. Fujitsu routes all arrays automatically using mainframe-based tools.

WORKSTATION SUPPORT

Daisy, Valid, and Mentor.

DESIGN CYCLE

CUSTOMER PERFORMS USING OWN TOOLS: Logic capture, simulation.

CUSTOMER PERFORMS USING VENDOR'S TOOLS: Functional simulation, logic simulation, test-program generation.

VENDOR PERFORMS: Timing analysis, all layout and post-layout analysis steps.

FUNCTION LIBRARIES

CMOS: Library contains more than 110 functions built from as many as 68 2-input gates; users can define new functions based on existing library elements; all functions have been built and tested; simulation parameters include ID, LD, SUH, VS, TS, FI, and FO.

Bipolar: Library contains 96 functions built from as many as 120 2-input gates plus 70 74LS-equivalent elements; users can define new functions based on existing library elements; all functions have been built and tested; simulation parameters include ID, LD, SUH, VS, TS, FI, and FO.

TRAINING

COURSE: 3-day course at design center is available at no cost upon design commitment.

DOCUMENTATION: Design evaluation guides are offered at no cost prior to design commitment.

SUPPORT FACILITIES

Santa Clara, CA; Dallas, TX; and Boston, MA.

CYCLE TIMES

DESIGN: 1 to 3 weeks.

PROTOTYPING: 6 to 12 weeks.

INPUTS FOR COST ESTIMATION

Array type, package type, gate count, critical-speed paths.

PRODUCTION COMMITMENTS

Fujitsu prefers a production commitment of at least \$100,000 over 2 years.

ALTERNATE SOURCE

Texas Instruments Inc; alternate sourcing effected through PG-tape transfer.

GE/RCA Solid State Div

Route 202
Somerville, NJ 08876
(201) 685-6218
Circle No 676

CUSTOMER/VENDOR INTERFACE

PREFERRED: Simulated net list, layout data generated by vendor's software, PG tapes.

DISCOURAGED: Functional block diagram.

DESIGN TOOLS

Users gain access to the software through Tymnet from remote alphanumeric terminals.

WORKSTATION SUPPORT

Daisy, Mentor, Valid, DEC VAX, and Apollo.

DESIGN CYCLE

CUSTOMER PERFORMS USING VENDOR'S TOOLS: Logic design, simulation, test-vector generation.

VENDOR PERFORMS: Layout, post-layout analysis, test-program generation.

FUNCTION LIBRARY

Cell complexity depends on user's requirements; library cells combine predefined models and user-customized building blocks; all basic component models have been tested; simulation parameters include ID, LD, SUH, VS, TS, FI, and FO.

TRAINING

COURSE: A 3-day session is offered in vendor's design centers.

DOCUMENTATION: Design manuals available as part of course.

SUPPORT FACILITIES

Somerville, NJ; Santa Clara, CA; Brussels, Belgium; Hong Kong; Paris, France; Sunbury, UK; Quickborn, West Germany; and Solna, Sweden.

CYCLE TIMES

DESIGN: Depends on customer.

PROTOTYPING: 6 to 8 weeks.

INPUTS FOR COST ESTIMATION

Logic diagram or gate count, I/O count and specification, package, temperature range, clock frequency.

PRODUCTION COMMITMENTS

None required.

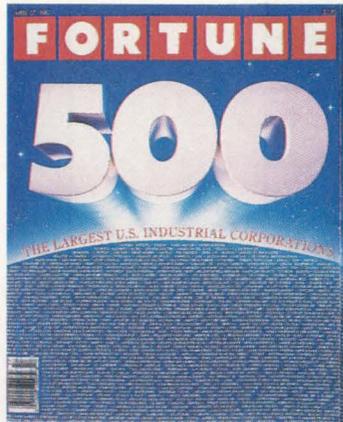
ALTERNATE SOURCE

LSI Logic; alternate sourcing effected through PG-tape transfer.

Continued on pg 170

EDN June 25, 1987

THINK...



A Fortune 500 company with 1986 sales of \$605 million

#1

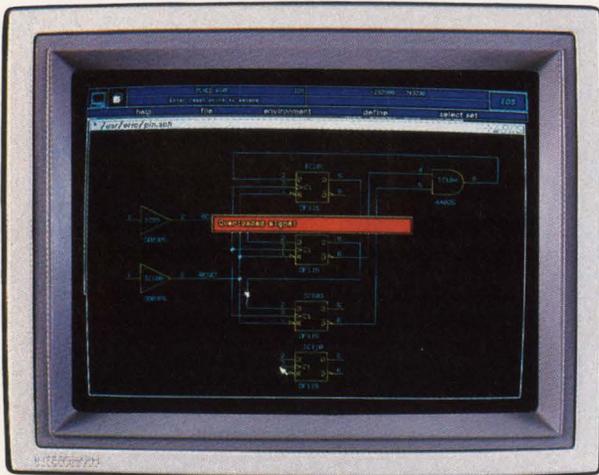
That's the world's largest independent vendor in
CAE/CAD/CAM



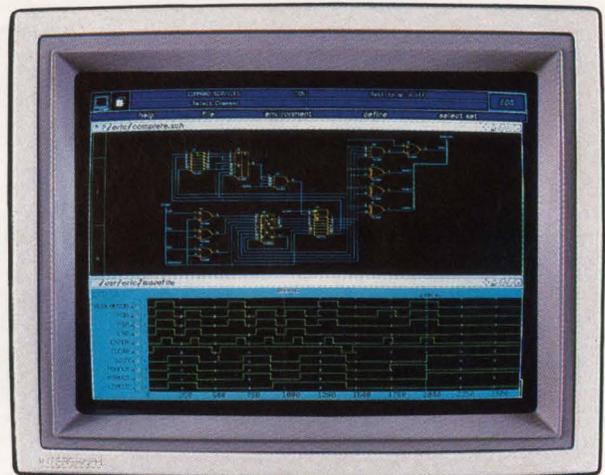
With software operating on the world's most powerful
engineering workstations

Think

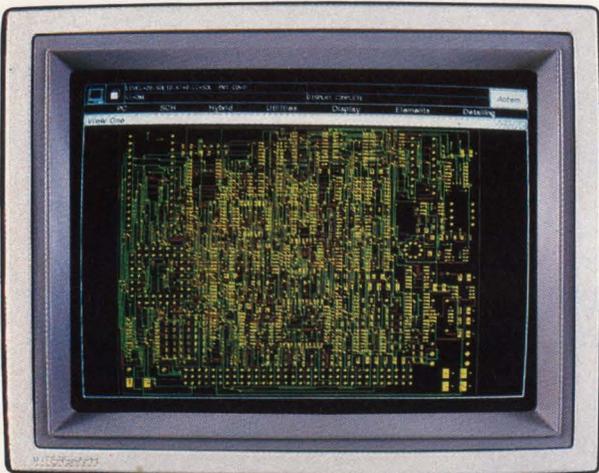
New thinking in design automation that gets your thinking to market faster . . .



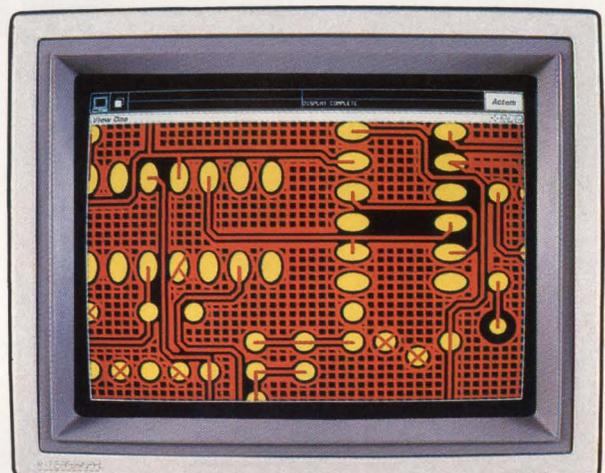
Create schematics faster with correct-by-construction design and on-line Electrical Rules Checking



Logic analyzer type display for interactive digital analysis using HILO-3



Begin PCB design with a feasibility check, then rely on a full suite of tools for autoplacement, high-completion autorouting, and design rule checking



Power and ground planes are generated automatically

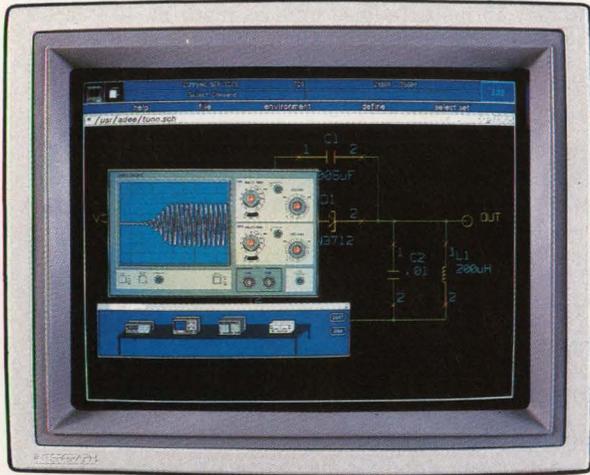
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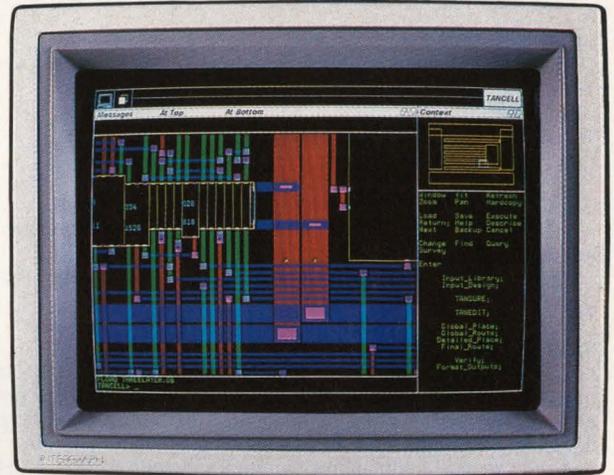
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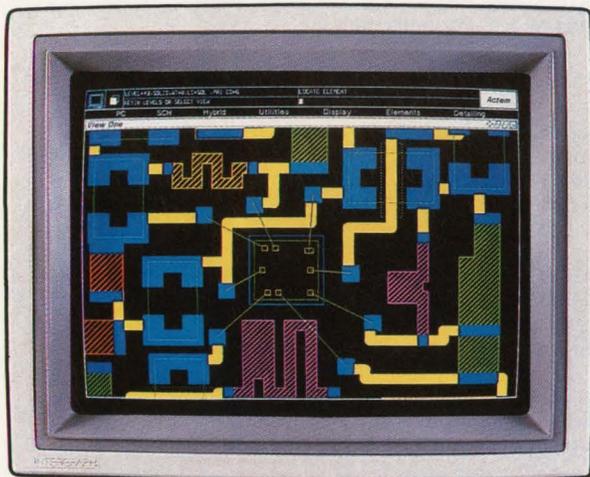
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INTERGRAPH

EDN GATE-ARRAY DIRECTORY

GE Semiconductor

1 Micron Dr
Research Triangle Park, NC 27709
(919) 549-3114
Circle No 677

CUSTOMER/VENDOR INTERFACE

PREFERRED: Simulated net list.
DISCOURAGED: Unverified schematics, block diagram.

DESIGN TOOLS

CAE software enables all design steps from schematic capture through PG-tape generation on VAX hardware.

WORKSTATION SUPPORT

Daisy, Mentor, FutureNet, and P-CAD.

DESIGN CYCLE

CUSTOMER PERFORMS USING OWN TOOLS: Schematic capture and simulation.

VENDOR PERFORMS: Layout, post-layout simulation, PG-tape generation.

FUNCTION LIBRARY

Library contains 60 (20,000 Series arrays) and 70 (10,000 Series) hard-wired macros as complex as up/down counters; users can create new cells from discrete gates or build soft macros by combining multiple hard-wired elements; all functions have been built and tested; simulation parameters include ID, LD, SUH, VS, TS, PD, FI, and FO.

TRAINING

COURSE: Courses available on gate-array design and design using P-Cad tools.

DOCUMENTATION: Design manuals available.

SUPPORT FACILITIES

San Jose, CA; Research Triangle Park, NC; Portland, OR; New Haven, CT; Basingstoke, UK; Paris, France; Munich, West Germany.

CYCLE TIMES

DESIGN: 2 to 3 weeks.
PROTOTYPING: 5 to 6 weeks.

INPUTS FOR COST ESTIMATION

Gate count, packaging, pin count.

PRODUCTION COMMITMENTS

None required.

General Instrument

Microelectronics Div
600 W John St
Hicksville, NY 11802
(516) 933-3107
Circle No 678

CUSTOMER/VENDOR INTERFACE

PREFERRED: Layout data in Calma format.
ACCEPTABLE: Simulated schematic.
DISCOURAGED: Unsimulated schematic or net list, functional block diagram, PG tapes.

DESIGN TOOLS

GI's CAE system supports data entry, simulation, and automatic routing. The system requires both alphanumeric and graphics terminals and runs on VAX and Prime minicomputers.

WORKSTATION SUPPORT

Daisy, Mentor, and Valid.

DESIGN CYCLE

CUSTOMER PERFORMS USING OWN OR VENDOR'S TOOLS: Logic design, simulation, timing analysis, test-pattern generation, testability analysis, fault grading, and post-layout simulation.

VENDOR PERFORMS: Placement and routing, custom cell creation, network-equivalence check. Any other steps at customer's discretion.

FUNCTION LIBRARY

Library includes 60 functions built from as many as 10 2-input gates; users can define new functions using existing library elements or discrete gates; all library cells have been built and tested; simulation parameters include ID, LD, SUH, VS, TS, PD, FI, and FO.

TRAINING

COURSE: Training offered in New York and California.

DOCUMENTATION: Design manuals available prior to design commitment; manuals are updated quarterly.

SUPPORT FACILITIES

None maintained.

CYCLE TIMES

DESIGN: 2 to 4 weeks.
PROTOTYPING: 7 to 9 weeks.

INPUTS FOR COST ESTIMATION

Functional description, approximate complexity, package type, special requirements.

PRODUCTION COMMITMENTS

Estimate of 18-month production volumes.

ALTERNATE SOURCES

Plessey and MCE Semiconductors Inc.

Gould Inc, Semiconductor Div

3800 Homestead Rd
Santa Clara, CA 95051
(408) 246-0330
Circle No 680

CUSTOMER/VENDOR INTERFACE

PREFERRED: Simulated net list, design database, PG tape, logic diagram.
DISCOURAGED: Functional block diagram.

DESIGN TOOLS

Design tools include simulators, automatic place-and-route software with back annotation, test generation, and design-rule checkers.

WORKSTATION SUPPORT

FutureNet, P-CAD, Viewlogic, Daisy, Mentor, and Calma.

DESIGN CYCLE

CUSTOMER PERFORMS USING OWN TOOLS: Schematic capture, simulation, test-program generation, and back annotation.

CUSTOMER PERFORMS USING VENDOR'S TOOLS: All of the above.

VENDOR PERFORMS: Custom cell generation.

FUNCTION LIBRARY

Library includes many functions; users can define new functions using existing library elements or discrete gates; all functions have been fabricated and tested; simulation parameters include ID, LD, SUH, FI, and FO.

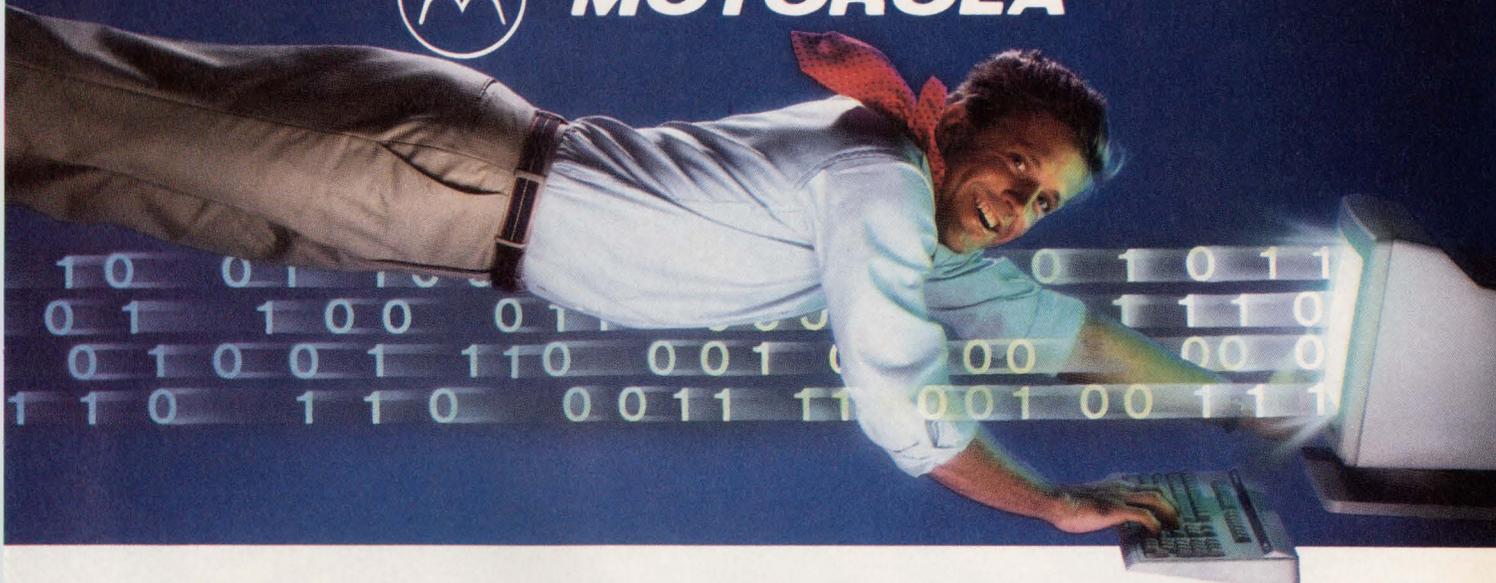
RAM, ROM, and other compilers are available.

TRAINING

COURSE: 2-day training course available at design centers.



MOTOROLA



Stick to the truth at top speed. Keep high-performance memory systems accurate, reliable with F2960/2960A control.

Fact is, today's big, fast memory arrays can separate you from reality with a single data-bit lie. Instantly, without explanation or correction.

Fortunately, there's a way to keep DRAM systems on the straight and narrow: the MC74F2960/2960A EDAC and associated LSI devices.

They do what discrete logic can't: maximize reliability, performance and economy. Without taking up usable board space.

High-speed errata eraser.

The F2960/2960A contains all logic needed to correct any single-bit error and detects all double- and some triple-bit errors. It generates 6 check bits on a 16-bit data field, 7 for 32-bits and 8 for 64 bits according to a modified Hamming code and corrects data in nanoseconds.

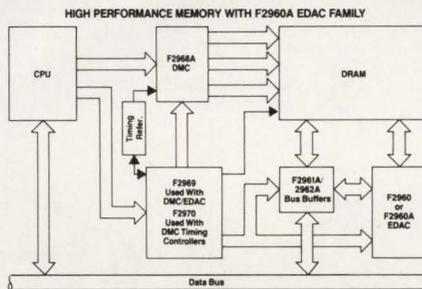
Motorola 'A' System Max Speed vs Standard System				
Mode	Path	Am2960/61	MC74F2960A/61A	% Improvement
Generate	Total Delay	57 ns	32 ns	44%
Detect	Total Delay	47 ns	29 ns	38%
Correct	Total Delay	100 ns	65 ns	35%

Featuring two diagnostic modes, the cascaded EDAC makes the error syndrome available on separate outputs for data logging.

It's pin-and-function compatible with similar units and utilizes the three-state MC74F2961A/62A inverting/non-inverting bus buffers for multiplexed bus operation.

In a 16-bit system, EDAC and buffers use about half the power of comparables.

What's more, its separate byte controls facilitate byte operations and it's fully compatible with the M68000 or comparable CPU family.



And support to make it easy.

The controller, MC74F2968A, provides complete address multiplex, refresh and drive for up to 88 DRAMs and interfaces with 16K, 64K or 256K memories.

The MC74F2969 provides all timing signals for memory control with error detection and correction, arbitrates memory cycles, handles refresh timing, memory initialization and supports error logging.

The 4-bit wide, inverting/non-inverting MC74F2961A/62A interfaces DRAMs, EDAC and data bus.

EDAC, buffers and timers are available now, the control and timer in 3Q.

One-on-one design-in help.

Get an engineer-to-engineer update on the latest Motorola LSI technology. Call

1-800-521-6274

toll-free any weekday from 8:00 a.m. to 4:30 p.m., MST, from anywhere in the U.S.

or Canada. Or contact Motorola Semiconductor Products, Inc., P.O. Box 20912, Phoenix, AZ 85036 for data.

*We're
on your
design-in
team.*



MOTOROLA

To: Motorola Semiconductor Products, Inc.
P.O. Box 20912, Phoenix, AZ 85036

Please send me more information on Motorola EDAC products.

Name _____ 326EDN062587

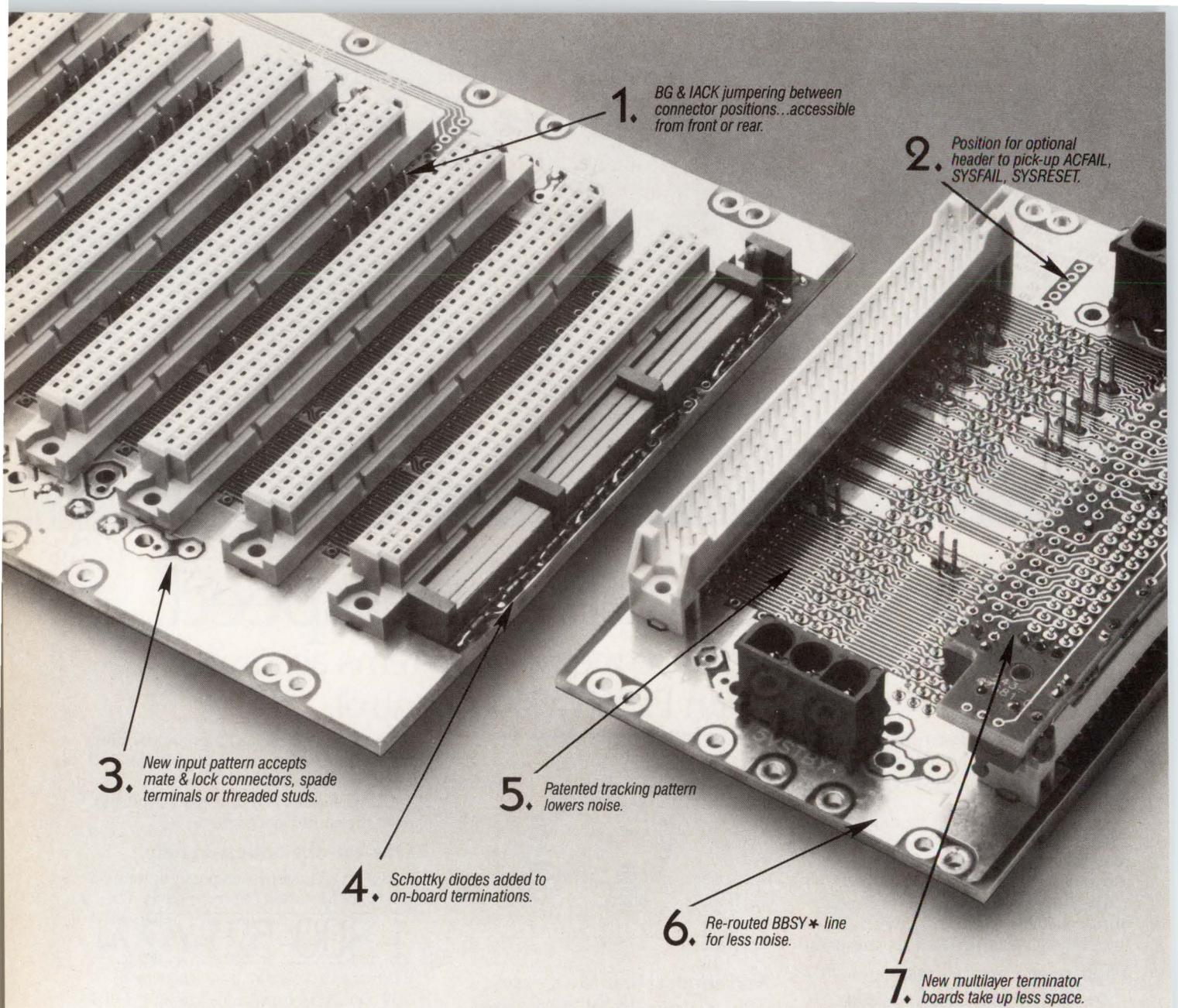
Title _____

Company _____

Address _____

City _____ State _____ Zip _____

Call me (_____) _____



1. BG & IACK jumpering between connector positions...accessible from front or rear.

2. Position for optional header to pick-up ACFAIL, SYSFAIL, SYSRESET.

3. New input pattern accepts mate & lock connectors, spade terminals or threaded studs.

5. Patented tracking pattern lowers noise.

4. Schottky diodes added to on-board terminations.

6. Re-routed BBSY* line for less noise.

7. New multilayer terminator boards take up less space.

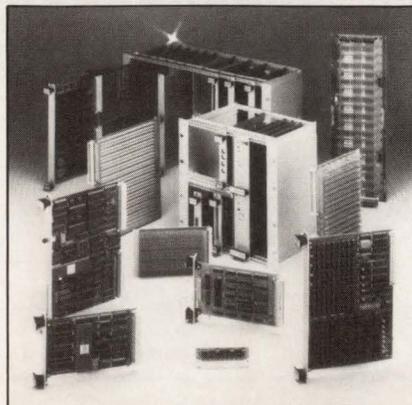
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CIRCLE NO 219

BICC-VERO ELECTRONICS, INC.

1000 Sherman Avenue
Hamden, CT 06514

(203) 288-8001 TWX: 510-227-8890

EDN GATE-ARRAY DIRECTORY

DOCUMENTATION: Available documentation includes user guides, design manuals, data books, training course notes, and application notes.

SUPPORT FACILITIES

Jericho, NY; Altamonte Springs, FL; Swindon, UK; Graz, Austria; Tokyo, Japan. Design support also available in Pocatello, ID.

CYCLE TIMES

DESIGN: 8 weeks.

PROTOTYPING: 4 weeks.

INPUTS FOR COST ESTIMATION

Clock speed, gate count, packaging, logic diagram, or net list for digital circuits; bandwidth, center frequencies, dynamic range, S/N ratio, and voltage range for analog circuits.

PRODUCTION COMMITMENTS

Minimum shipment, \$5000.

GTE Microcircuits

2000 W 14th St
Tempe, AZ 85281
(602) 968-4431
Circle No 679

CUSTOMER/VENDOR INTERFACE

PREFERRED: Simulated schematic or net list.

ACCEPTABLE: Anything.

WORKSTATION SUPPORT

Daisy.

DESIGN CYCLE

CUSTOMER PERFORMS USING OWN TOOLS: Partitioning analysis, functional simulation, logic design.

VENDOR OR CUSTOMER PERFORMS: Logic simulation, timing analysis, logic minimization, test-program generation, testability analysis, fault grading.

VENDOR PERFORMS: Critical-path analysis, chip layout, post-layout analysis.

FUNCTION LIBRARY

Library includes 50 cells built from as many as 10 2-input gates; user can create new cells from existing library elements or discrete gates; 100% of the library has been fabricated and tested; simulation parameters include ID, LD, SUH, VS, TS, PD, FI, and FO.

TRAINING

COURSE: None offered.

DOCUMENTATION: Design manuals are available prior to design commitment.

SUPPORT FACILITIES

Tempe, AZ; Ottawa, Canada.

CYCLE TIMES

DESIGN: 6 to 9 weeks.

PROTOTYPING: 4 to 6 weeks.

INPUTS FOR COST ESTIMATION

Estimated gate count, production quantity, package type.

PRODUCTION COMMITMENTS

None.

ALTERNATE SOURCES

None.

Harris Semiconductor Sector

Box 883
Melbourne, FL 32901

(305) 724-7407

Circle No 681

CUSTOMER/VENDOR INTERFACE

PREFERRED: Simulated schematic.

ACCEPTABLE: Unsimulated schematic, layout data generated by vendor's software.

DISCOURAGED: Functional block diagram, layout data generated by customer's software, PG tapes.

DESIGN TOOLS

Harris offers CAE software over a timesharing network. One system for both gate-array and standard-cell design supports all phases of chip design, including testability analysis, test-program generation, and post-routing simulation.

WORKSTATION SUPPORT

Daisy and Valid.

DESIGN CYCLE

CUSTOMER PERFORMS USING OWN TOOLS: Partitioning analysis, logic design, test-pattern generation.

CUSTOMER PERFORMS USING VENDOR'S TOOLS: Above plus logic simulation, timing analysis, testability analysis, fault grading, network-equivalence check, post-routing simulation.

VENDOR PERFORMS: Placement and routing, custom cell creation.

TRAINING

COURSE: A 5-day course is offered prior to design commitment in Melbourne; \$1500.

DOCUMENTATION: Design manuals are available prior to design commitment.

SUPPORT FACILITIES

Melbourne, FL.

CYCLE TIMES

DESIGN: 2 to 4 weeks.

PROTOTYPING: 4 to 6 weeks.

INPUTS FOR COST ESTIMATION

Schematics, production quantity, package type, specifications.

PRODUCTION COMMITMENTS

None.

Holt Inc

8 Chrysler Ave
Irvine, CA 92714
(714) 859-8800
Circle No 682

CUSTOMER/VENDOR INTERFACE

PREFERRED: Simulated or unsimulated schematic or net list.

ACCEPTABLE: Functional block diagram.

DISCOURAGED: Layout data, PG tapes.

DESIGN CYCLE

VENDOR PERFORMS: All logic-design, simulation, testability-analysis, test-program-generation, and chip-layout steps.

TRAINING

COURSE: None offered.

CYCLE TIMES

DESIGN: 4 to 6 weeks.

PROTOTYPING: 3 to 4 weeks.

INPUTS FOR COST ESTIMATION

Logic diagram or schematic.

PRODUCTION COMMITMENTS

None required.

EDN GATE-ARRAY DIRECTORY

ALTERNATE SOURCES

None.

Honeywell Digital Products Center

1150 E Cheyenne Mountain Blvd
Colorado Springs, CO 80906
(303) 577-3581
Circle No 683

CUSTOMER/VENDOR INTERFACE

PREFERRED: Simulated schematic or net list, layout data generated using vendor's software, PG tape.

DISCOURAGED: Unsimulated schematic, layout data generated by customer's software, functional block diagram.

DESIGN TOOLS

Vendor's Software Toolkit enhances workstation simulation programs and runs on Mentor workstations. Merlyn-G physical design tools are available for back-end design.

WORKSTATION SUPPORT

Mentor and Daisy.

DESIGN CYCLE

CUSTOMER PERFORMS USING OWN OR VENDOR'S TOOLS: Functional simulation, logic design and simulation, fault grading, test-vector generation.

VENDOR PERFORMS: Placement and routing, network-equivalency check, test-program generation, tooling.

FUNCTION LIBRARIES

CML HT5000 array: Library includes over 75 functions built from as many as 80 2-input gates; users can create new functions based on existing library elements; 100% of library functions have been built and tested; simulation parameters include ID, LD, SUH, VS, TS, PD, FI, and FO.

CML HE2000, HM3500 arrays: Library includes over 150 functions built from as many as 70 2-input gates; users can create new functions based on existing library elements; 75% of library functions have been built and tested; simulation parameters include ID, LD, SUH, VS, TS, PD, FI, and FO.

TRAINING

COURSE: A 4-day session is available prior to design commitment; course offered in Colorado Springs, CO, or at customer sites.

DOCUMENTATION: Manuals available prior to design commitment.

SUPPORT FACILITIES

Minneapolis, MN, and Colorado Springs, CO.

CYCLE TIMES

DESIGN: Depends on design complexity.

PROTOTYPING: 8 to 10 weeks.

INPUTS FOR COST ESTIMATION

Gate count, list of functions, package, production volume, and schedule.

PRODUCTION COMMITMENTS

None required.

ALTERNATE SOURCES

HE, HM, HT arrays: Fairchild.

Hughes Aircraft Co
Semiconductor Div
500 Superior Ave

Newport Beach, CA 92658

(714) 759-2727

Circle No 684

CUSTOMER/VENDOR INTERFACE

PREFERRED: Simulated database with test vectors.

DESIGN TOOLS

Vendor supplies proprietary software for workstations; software provides timing simulation and back annotations.

WORKSTATION SUPPORT

Mentor Graphics and Daisy.

DESIGN CYCLE

CUSTOMER PERFORMS USING OWN TOOLS: Test vector generation, fault analysis.

CUSTOMER PERFORMS USING VENDOR'S TOOLS: Schematic capture, logic and timing simulation.

VENDOR PERFORMS: Layout, back annotation, post-layout simulation, timing verification, tooling, test-program generation, prototype testing.

TRAINING

COURSE: Training course covers aspects of design cycle.

DOCUMENTATION: Support and design manuals come with courses.

SUPPORT FACILITIES

Newport Beach, CA.

CYCLE TIMES

DESIGN: 4 to 6 weeks.

PROTOTYPING: 4 to 6 weeks.

INPUTS FOR COST ESTIMATION

Schematic, screening and packaging requirement, projected volume over time.

PRODUCTION COMMITMENTS

Negotiable.

ALTERNATE SOURCES

None. VLSI Technology for manufacturing.

Integrated Circuit Systems Inc

1012 W 9th Ave
King of Prussia, PA 19406
(215) 265-8690
Circle No 685

CUSTOMER/VENDOR INTERFACE

PREFERRED: Simulated schematic.

ACCEPTABLE: Functional block diagram, unsimulated schematic, layout data generated by vendor's software, PG tapes.

DISCOURAGED: Layout data generated by customer's software.

DESIGN TOOLS

The firm's CAE system runs on VAX minicomputers and is accessible through a high-resolution graphics terminal.

WORKSTATION SUPPORT

Mentor and Daisy.

DESIGN CYCLE

CUSTOMER PERFORMS USING OWN TOOLS: Logic design.

CUSTOMER PERFORMS USING VENDOR'S TOOLS: Functional and logic simulations, timing analysis, test-pattern generation, post-routing simulation.

VENDOR PERFORMS: Partitioning analysis, testability analysis, fault grading, placement and routing, custom cell creation, network-equivalency check.

ESD testing has determined that delicate MUXes can be hazardous to your wealth.

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The moral: Perform your own MIL-STD ESD testing on MUXes before design-in (or before adding costly extra components), so field failures don't ground your system later.

The offer: For full test results, call 1-800-4-HARRIS, Ext. 1410 (in Canada, 1-800-344-2444, Ext. 1410). Or write Harris Semiconductor Products Division, P.O. Box 883, MS 53-035, Melbourne, Florida 32902-0883.

The end.



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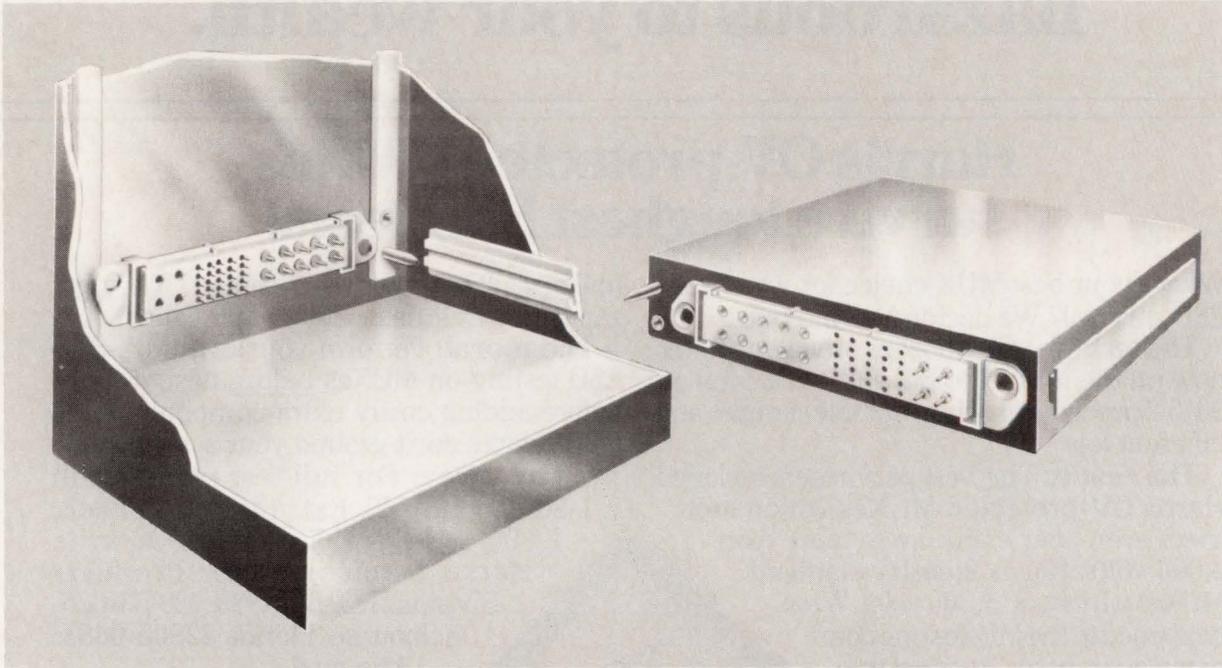


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EDN GATE-ARRAY DIRECTORY

TRAINING

COURSE: Training is available prior to design commitment.

DOCUMENTATION: Design manuals are free; available prior to design commitment; updated semiannually.

SUPPORT FACILITIES

Training area.

CYCLE TIMES

DESIGN: 1 to 3 weeks.

PROTOTYPING: 4 to 6 weeks.

INPUTS FOR COST ESTIMATION

Schematic or function diagram.

PRODUCTION COMMITMENTS

None.

ALTERNATE SOURCES

Minimum of one.

Integrated Logic

4815 List Dr
Colorado Springs, CO 80919
(303) 590-1588
Circle No 686

CUSTOMER/VENDOR INTERFACE

PREFERRED: Simulated schematic.

DESIGN TOOLS

Design tools include schematic capture, net-list generation, logic simulation, layout, design-rule check, automatic test-vector generation using scan design, and automatic test-program generation.

WORKSTATION SUPPORT

Mentor, Daisy, and FutureNet.

DESIGN CYCLE

CUSTOMER PERFORMS USING OWN TOOLS: Partitioning, schematic capture, functional simulation.

CUSTOMER PERFORMS USING VENDOR'S TOOLS: Timing simulation.

VENDOR PERFORMS: Turnkey design or layout and post-routing simulation.

SUPPORT FACILITIES

Colorado Springs, CO.

CYCLE TIMES

DESIGN: 2 to 3 weeks.

PROTOTYPING: 5 to 6 weeks.

INPUTS FOR COST ESTIMATION

Schematic preferred, gate count acceptable.

PRODUCTION COMMITMENTS

None required.

Integrated Microcircuits Inc

1515 S 6th St
Hopkins, MN 55343
(612) 933-4600
Circle No 687

CUSTOMER/VENDOR INTERFACE

PREFERRED: Simulated schematic, layout data generated by vendor's software.

DISCOURAGED: Unsimulated schematic, layout data generated by customer's software.

DESIGN TOOLS

Tools run on Calma GDS-1 CAD systems and provide simulation and interactive layout.

WORKSTATION SUPPORT

Layout information for Calma and Via Systems.

DESIGN CYCLE

VENDOR PERFORMS: All design steps.

TRAINING

COURSE: None.

DOCUMENTATION: Design manuals available prior to design commitment; \$50.

SUPPORT FACILITIES

Hopkins, MN.

CYCLE TIMES

DESIGN: 3 to 6 weeks.

PROTOTYPING: 5 to 8 weeks.

PRODUCTION COMMITMENTS

None.

Intel Corp

3065 Bowers Ave
Santa Clara, CA 95051
(408) 987-5400
Circle No 688

CUSTOMER/VENDOR INTERFACE

PREFERRED: Simulated net list and test vectors generated using company's design software.

DESIGN TOOLS

IDE design system provides schematic capture, net-list entry, worst-case delay prediction, simulation, and test-tape generation.

WORKSTATION SUPPORT

Daisy, Mentor, FutureNet, and CIEDS system on PC/AT.

DESIGN CYCLE

CUSTOMER PERFORMS USING OWN TOOLS: Logic design, prelayout, and postlayout simulation with routed delays back-annotated, and test program generation.

CUSTOMER PERFORMS USING VENDOR'S TOOLS: Testability analysis (optional Automatic Test Generation with LSSD).

VENDOR PERFORMS: Layout.

FUNCTION LIBRARIES

Libraries contain 130 functions; most functions have multiple drive levels (low, medium, high); full family of LSSD macros; user-configurable static RAMs; Intel peripheral and support-chip products in macro form; users can define new functions using existing library elements; all elements have been fabricated and tested; simulation parameters include ID, LD, SUH, VS, TS, PD, FI, and FO.

TRAINING

COURSE: 1-week course offered at design centers.

DOCUMENTATION: Manuals available to course attendees.

SUPPORT FACILITIES

Santa Clara, CA; Boston, MA; Swindon, UK.

CYCLE TIMES

DESIGN: 1 to 8 weeks.

PROTOTYPING: 3 to 6 weeks.

INPUTS FOR COST ESTIMATION

Gate count, pin count, critical path delay or system clock frequen-

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ING WITH GATES, ING YOUR TIME.

HOURS MINUTES SECONDS

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seven days using traditional schematics.

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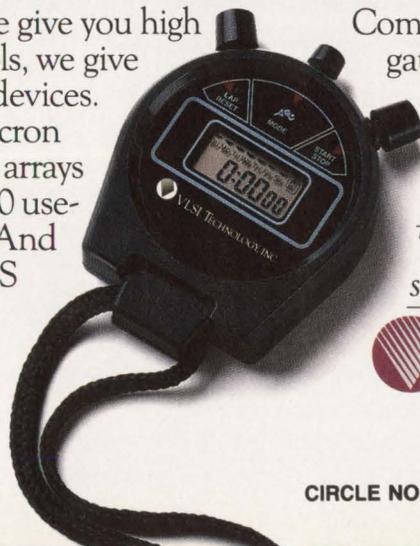
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EDN GATE-ARRAY DIRECTORY

cy, temperature range, voltage range, memory requirements.

PRODUCTION COMMITMENTS

None required.

ALTERNATE SOURCES

Pending.

International Microcircuits Inc

3350 Scott Blvd
Santa Clara, CA
(408) 727-2280
Circle No 689

CUSTOMER/VENDOR INTERFACE

PREFERRED: Simulated schematic.

ACCEPTABLE: Functional block diagram, unsimulated schematic or net list, layout data, PG tapes.

DESIGN TOOLS

IMI's CAE system runs on VAX minicomputers.

WORKSTATION SUPPORT

Mentor, Daisy, and Valid.

DESIGN CYCLE

CUSTOMER PERFORMS USING VENDOR'S TOOLS: Partitioning analysis, functional simulation, logic design and simulation, timing analysis, test-program generation, testability analysis, fault grading.

VENDOR PERFORMS: Layout and post-layout analysis.

FUNCTION LIBRARY

Library includes 110 functions; users can create library elements based on existing functions or discrete gates; all library cells have been built and tested; simulation parameters include ID, LD, SUH, TS, VS, PD, FI, and FO.

TRAINING

COURSE: A 5-day training course is available in Santa Clara, CA, prior to design commitment; \$2000.

DOCUMENTATION: Design manuals are available prior to design commitment; updated yearly; free with \$2000 Daisy macrocell library.

SUPPORT FACILITIES

Santa Clara, CA.

CYCLE TIMES

DESIGN: 4 to 20 weeks.

PROTOTYPING: 3 to 4 weeks.

INPUTS FOR COST ESTIMATION

Logic drawings.

PRODUCTION COMMITMENTS

None required.

ALTERNATE SOURCES

Multiple wafer sources.

ITT VLSI Design Center

15 Progress Dr
Shelton, CT 06484
(203) 929-9790
Circle No 690

CUSTOMER/VENDOR INTERFACE

PREFERRED: Verified net list in Mentor or Valid workstation format.

DISCOURAGED: Net list in other formats.

DESIGN TOOLS

Tools provide schematic capture, logic simulations, automatic and manual layout, layout-parameter extraction, back-annotation simulation, translation of simulation test vectors to Sentry functional-test program.

WORKSTATION SUPPORT

Mentor and Valid.

DESIGN CYCLE

CUSTOMER PERFORMS USING OWN TOOLS: Logic design, test-vector generation, design specification.

CUSTOMER PERFORMS USING VENDOR'S TOOLS: Schematic capture, initial and back-annotated simulation.

VENDOR PERFORMS: Layout, layout-parameter extraction, design-rule checks, network-equivalency check, test-vector translation.

TRAINING

COURSE: Available.

DOCUMENTATION: Design files for workstations and data-sheets available.

CYCLE TIMES

DESIGN: 8 weeks for 3000-gate array.

PROTOTYPING: 13 weeks from verified net list.

INPUTS FOR COST ESTIMATION

Schematics or circuit description, volume, schedule.

PRODUCTION COMMITMENTS

None.

Linear Technology Inc

Box 489, Station A
Burlington, Ontario, Canada L7R 3Y3
(416) 632-2996
Circle No 691

CUSTOMER/VENDOR INTERFACE

PREFERRED: Simulated schematic or net list, layout data generated by vendor's software.

ACCEPTABLE: Functional block diagram, unsimulated schematic or net list, layout generated by customer's software.

DESIGN TOOLS

LTI offers a design kit including manuals and large layout sheets. Internal layout data available for Computervision, Calma, and Applicon CAD systems under nondisclosure agreement.

DESIGN CYCLE

CUSTOMER PERFORMS USING OWN TOOLS: Partitioning analysis, functional simulation, critical-path analysis, test-pattern generation, manual routing.

VENDOR PERFORMS: Testability analysis, fault grading, placement and routing, custom cell creation, circuit breadboarding, post-routing simulation, network-equivalence check.

TRAINING

COURSE: A 1-day seminar and a 5-day training course are available in Burlington, Ontario.

DOCUMENTATION: Design manuals available on magnetic tapes; \$20.

SUPPORT FACILITIES

Burlington, Ontario, Canada; Philadelphia, PA; Ogaki, Japan; Delft, The Netherlands.

CYCLE TIMES

DESIGN: 2 to 4 weeks.

EDN GATE-ARRAY DIRECTORY

PROTOTYPING: 8 to 12 weeks.

INPUTS FOR COST ESTIMATION

Detailed design data.

PRODUCTION COMMITMENTS

None required.

ALTERNATE SOURCES

Wafer processing is available from a number of foundries.

LSI Logic Corp

1551 McCarthy Blvd
Milpitas, CA 95035
(408) 433-8000
Circle No 692

CUSTOMER/VENDOR INTERFACE

PREFERRED: Simulated net list and test vectors generated using company's design software.

DESIGN TOOLS

LDS design system provides schematic capture, net-list entry, worst-case delay prediction, simulation, and test-tape generation. Additional system level support from Modular Design Environment.

WORKSTATION SUPPORT

Daisy, Mentor, Valid, Sun, FutureNet, Apollo, VAX, Pyramid, and P-CAD systems.

DESIGN CYCLE

CUSTOMER PERFORMS USING OWN TOOLS: Logic design, simulation, and test-program generation.

CUSTOMER PERFORMS USING VENDOR'S TOOLS: Testability analysis, post-layout simulation.

VENDOR PERFORMS: Layout, manufacture.

FUNCTION LIBRARIES

Libraries contain 273 functions built from as many as 744 2-input gates; users can define new functions using existing library elements; all elements have been fabricated and tested; simulation parameters include ID, LD, SUH, VS, TS, PD, FI, and FO.

TRAINING

COURSE: Offered at design centers and cover software and silicon products.

DOCUMENTATION: Manuals available to course attendees.

SUPPORT FACILITIES

Milpitas, CA; Irvine, CA; Sherman Oaks, CA; Minneapolis, MN; Waltham, MA; Dallas, TX; Boca Raton, FL; Itasca, IL; Bethesda, MD; Bellevue, WA; Calgary, Canada; Edmonton, Canada; Kanata, Canada; Paris, France; London, UK; Munich, Dusseldorf, and Stuttgart, West Germany; Bracknell, UK; Tel Aviv, Israel; Tokyo, Osaka, and Isukuba-Gun, Japan; and over 40 distributor design centers in US and Europe.

CYCLE TIMES

DESIGN: 1 to 8 weeks.

PROTOTYPING: 2 to 5 weeks.

INPUTS FOR COST ESTIMATION

Gate count, pin count, critical-path delay or system clock frequency, temperature range, memory requirements, packaging, processing.

PRODUCTION COMMITMENTS

None required.

ALTERNATE SOURCES

AMD, Toshiba, RCA, SGS, Raytheon, Hughes.

Marconi Electronic Devices Inc

45 Davids Dr
Hauppauge, NY 11788
(516) 231-7710
Circle No 693

CUSTOMER/VENDOR INTERFACE

PREFERRED: Simulated schematic or net list.

DISCOURAGED: Black-box specification.

DESIGN TOOLS

Marconi CAE system contains cell libraries, automatic layout, network-equivalency checks, and automatic test-program generation. Tools include Hilo-2 and Hilo-3 in addition to the Applicon AGS860 ECAD.

WORKSTATION SUPPORT

Mentor, Daisy, Silvar-Lisco.

DESIGN CYCLE

CUSTOMER PERFORMS USING OWN TOOLS: Partitioning analysis, functional simulation, logic design, logic simulation.

CUSTOMER PERFORMS USING VENDOR'S TOOLS: Above plus testability analysis, timing analysis, fault grading.

VENDOR PERFORMS: Placement and routing, custom-cell creation, network-equivalence check, and post-routing simulation.

FUNCTION LIBRARY

Library includes more than 100 functions built from as many as 66 2-input gates; users can define new functions based on existing library elements or discrete gates; all elements have been built and tested; simulation parameters include ID, LD, SUH, FI, and FO.

TRAINING

COURSE: 12 courses available with documentation.

DOCUMENTATION: Design manuals available without design commitment; \$250.

SUPPORT FACILITIES

Hauppauge, NY. Marconi facilities in Wembley, UK.

CYCLE TIMES

DESIGN: 3 weeks typ.

PROTOTYPING: 10 weeks.

INPUTS FOR COST ESTIMATION

Schematics, electrical specifications, environmental specifications, packaging, and screening requirements.

PRODUCTION COMMITMENTS

None.

MCE Semiconductor Inc

1111 Fairfield Dr
West Palm Beach, FL 33407
(305) 845-2837
Circle No 694

CUSTOMER/VENDOR INTERFACE

PREFERRED: Functional block diagram, unsimulated schematic or net list, layout data generated using vendor's tools, PG tapes.

ACCEPTABLE: Simulated schematic or net list, layout data generated using customer's software.

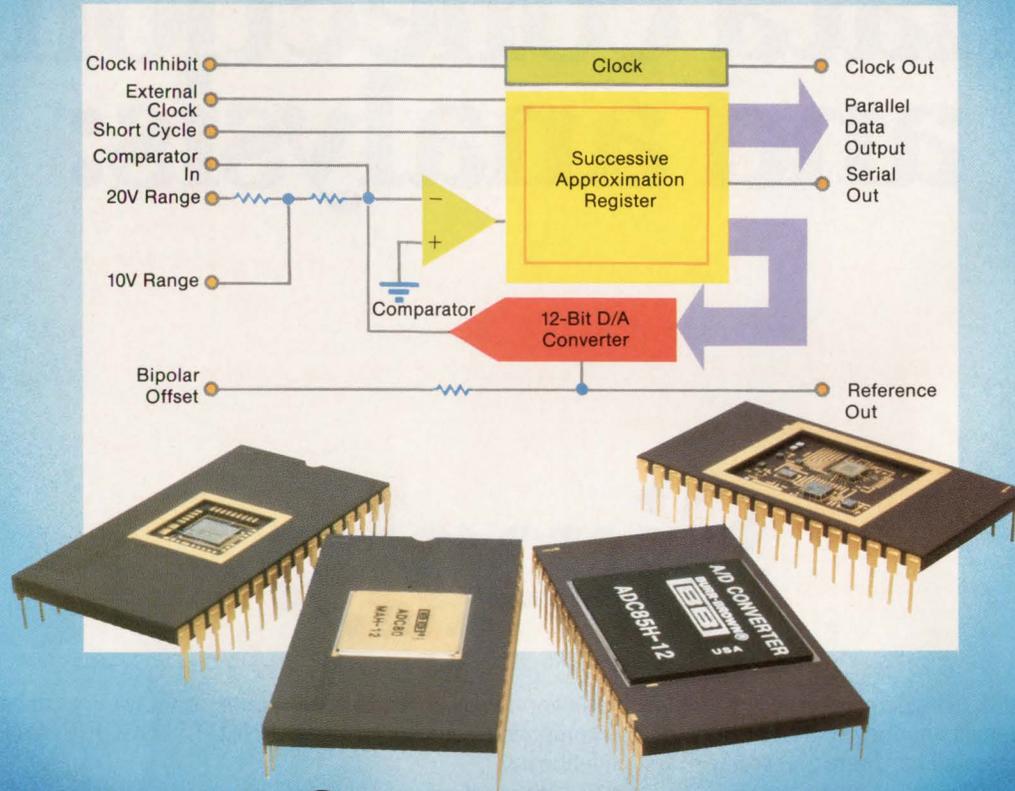
DESIGN TOOLS

MCE offers a series of breadboarding tools that aid in circuit design and verification. The firm also offers Aspec and Spice simulators for circuit analysis and several proprietary layout and verification tools for post-routing checks.

DESIGN CYCLE

CUSTOMER PERFORMS USING OWN TOOLS: Logic minimiza-

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Conversion time, max	25 μ s	10 μ s
Gain tempco, max	± 30 ppm/ $^{\circ}$ C	± 15 ppm/ $^{\circ}$ C
Package	32-pin hermetic ceramic DIP	
No missing codes	-25/+85 $^{\circ}$ C	0/+70 $^{\circ}$ C, -25/+85 $^{\circ}$ C, -55/+125 $^{\circ}$ C
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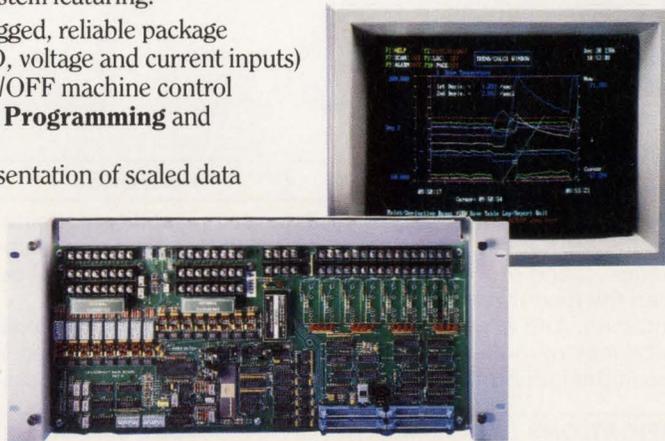
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EDN GATE-ARRAY DIRECTORY

tion and fault grading.

VENDOR PERFORMS: Logic design, simulation, timing analysis, critical-path analysis, testability analysis, all layout and layout-verification functions.

FUNCTION LIBRARIES

Users can define new functions based on existing cells or discrete components; all cells have been fabricated and tested; simulation parameters include ID, LD, VS, TS, PD, FI, and FO.

TRAINING

COURSE: A 1/2-day session is available before design commitment; a 3-day session is offered after design commitment; courses offered in US and West Germany.

DOCUMENTATION: Design manuals available without design commitment; \$5 to \$100.

SUPPORT FACILITIES

West Palm Beach, FL; Sunnyvale, CA; Tewkesbury, UK; and in Nuremburg and Munich, West Germany.

CYCLE TIMES

DESIGN: 4 to 16 weeks.

PROTOTYPING: 2 to 4 weeks.

INPUTS FOR COST ESTIMATION

Chip data, utilization, test requirements.

PRODUCTION COMMITMENTS

None required.

ALTERNATE SOURCES

None.

Mitel Semiconductor

350 Leggett Dr
Kanata, Ontario, Canada
(613) 592-5280
Circle No 695

CUSTOMER/VENDOR INTERFACE

PREFERRED: PG tape.

DESIGN TOOLS

Mitel's CAE system supports logic design, simulation, and manual layout tasks. The software runs on a VAX minicomputer and Calma and Computervision CAD systems. It accepts data in gate- or macro-level schematic diagrams. In addition, a layout kit allows chip design without CAE tools; users affix adhesive overlays to scaled layout sheets.

WORKSTATION SUPPORT

Daisy. Layout data available for Calma.

DESIGN CYCLE

CUSTOMER PERFORMS USING OWN TOOLS: Logic design.

CUSTOMER PERFORMS USING VENDOR'S TOOLS: Simulation, manual layout.

VENDOR PERFORMS: Testability analysis, test-program generation.

FUNCTION LIBRARY

Library includes 100 functions built from as many as 18 2-input gates; users can build new functions from library elements; all functions have been built and tested; simulation parameters include ID, LD, SUH, VS, TS, FI, and FO.

TRAINING

COURSE: Design courses are offered at customer's site or at Kanata, Ontario plant; price varies with depth of training.

DOCUMENTATION: Design manuals are available prior to design commitment; \$100, updated yearly.

SUPPORT FACILITIES

PML Ltd (Vancouver, British Columbia, Canada) and the Circuit Design Group (Phoenix, AZ).

CYCLE TIMES

PROTOTYPING: 12 weeks.

INPUTS FOR COST ESTIMATION

Gate count, package style, pin count, production quantity, screening level.

PRODUCTION COMMITMENTS

None required.

ALTERNATE SOURCES

Plessey and GTE Microcircuits Div.

Mitsubishi Electronics America Inc

1050 E Arques Ave
Sunnyvale, CA 94086
(408) 730-5900
Circle No 696

CUSTOMER/VENDOR INTERFACE

PREFERRED: Simulated logic diagram or net list.

DISCOURAGED: PG tape.

DESIGN TOOLS

Schematic capture, net-list generation, Tegas simulator, circuit simulation.

WORKSTATION SUPPORT

Daisy, Mentor, Valid, FutureNet.

DESIGN CYCLE

CUSTOMER PERFORMS USING OWN TOOLS: Logic design, breadboard.

CUSTOMER PERFORMS USING VENDOR'S TOOLS: Schematic capture, simulation, timing verification.

VENDOR PERFORMS: Layout, post-layout simulation, tooling.

TRAINING

COURSE: Available.

DOCUMENTATION: Available.

SUPPORT FACILITIES

Sunnyvale, CA; Durham, NH.

CYCLE TIMES

DESIGN: 2 to 4 weeks.

PROTOTYPING: 4 to 6 weeks.

INPUTS FOR COST ESTIMATION

Gate density, package, customer/vendor interface, volume.

PRODUCTION COMMITMENTS

None.

Motorola Inc

2200 W Broadway Rd
Mesa, AZ 85036
(602) 962-2516
Circle No 697

CUSTOMER/VENDOR INTERFACE

ACCEPTABLE: Simulated or unsimulated schematics or net lists, PG tapes.

DESIGN TOOLS

Motorola offers workstation-based tools for schematic capture,

EDN GATE-ARRAY DIRECTORY

logic simulation, and layout. Mainframe software performs other design steps.

WORKSTATION SUPPORT

Daisy, Mentor, P-CAD, Hewlett-Packard, Tektronix, Valid, ComputerVision, FutureNet.

DESIGN CYCLE

CUSTOMER PERFORMS USING OWN OR VENDOR'S TOOLS:

Functional simulation, logic design and simulation, timing analysis, test-pattern generation, testability analysis, fault grading. Layout and post-layout analysis for bipolar arrays. CMOS arrays need vendor software for layout.

VENDOR PERFORMS: Custom cell creation.

FUNCTION LIBRARIES

ECL: Library includes over 120 functions built from as many as 22 2-input gates; users can build new functions from library elements; 99% of all functions have been built and tested; simulation parameters include ID, SUH, PD, FI, and FO.

TTL: Library includes over 80 functions built from as many as 22 2-input gates; users can build new functions from library elements; 99% of all functions have been built and tested; simulation parameters include ID, LD, SUH, VS, TS, PD, FI, and FO.

CMOS: Library includes 65 functions built from as many as 18 2-input gates; users can build new functions from library elements; 100% of all functions have been built and tested; simulation parameters include ID, LD, SUH, FI, and FO.

TRAINING

COURSE: A 3- to 5-day course is available at Motorola Technology centers and customer sites prior to design commitment; \$3000.

DOCUMENTATION: Documentation is available free prior to design commitment.

SUPPORT FACILITIES

Dallas, TX; Atlanta, GA; Maitland, FL; Livonia, MI; Hauppauge, NY; Boston, MA; River Edge, NJ; Chicago, IL; Minneapolis, MN; Denver, CO; San Jose and Los Angeles, CA; Washington, DC; Tokyo, Japan; Munich, West Germany; Tel Aviv, Israel; Hong Kong; Vanves, France; Seoul, Korea; Singapore; Solna, Sweden; Taipei, Taiwan; Melbourne, Australia; Aylesbury, UK; and Toronto, CA.

CYCLE TIMES

PROTOTYPING: 7 to 10 weeks.

INPUTS FOR COST ESTIMATION

Array type, package type, production volume, schedule.

PRODUCTION COMMITMENTS

None required.

ALTERNATE SOURCES

National Semiconductor; NCR for CMOS arrays.

National Semiconductor Corp

2900 Semiconductor Dr
Santa Clara, CA 95051
(408) 721-4140
Circle No 698

CUSTOMER/VENDOR INTERFACE

PREFERRED: Simulated schematic or net list, layout data generated by vendor's software.

ACCEPTABLE: Functional block diagram, unsimulated schematic or net list, layout data generated by customer's software, PG tapes.

WORKSTATION SUPPORT

Daisy, Mentor, Valid, FutureNet.

DESIGN CYCLE

CUSTOMER PERFORMS USING OWN OR VENDOR'S TOOLS:

Logic design, simulation, timing analysis, logic minimization, critical-path analysis, testability analysis, fault grading, test-program generation, custom cell creation.

VENDOR PERFORMS: Array routing, network-equivalency check, post-routing simulation, partitioning analysis.

TRAINING

COURSE: A 2- to 3-day session is available prior to design commitment; course is offered in all design centers.

DOCUMENTATION: Design manuals are available prior to design commitment; updated quarterly.

SUPPORT FACILITIES

Santa Clara and Irvine, CA; Boston, MA; Bedford, UK; Stockholm, Sweden; Paris, France; Munich, West Germany; Australia; Korea; Taiwan; and Hong Kong.

CYCLE TIMES

DESIGN: Application-dependent.

PROTOTYPING: Gate arrays: 3 to 4 weeks; Standard cells: 8 to 9 weeks.

INPUTS FOR COST ESTIMATION

Schematic, I/O count, production volume and schedule, technology, package type, screening level, customer/vendor interface.

PRODUCTION COMMITMENTS

None required.

ALTERNATE SOURCES

IMP (International Microelectronic Products).

NCM Corp

1500 Wyatt Dr
Santa Clara, CA 95054
(408) 496-0290
Circle No 699

CUSTOMER/VENDOR INTERFACE

PREFERRED: Logic schematics.

WORKSTATION SUPPORT

Silicon Graphics Gemstation.

DESIGN CYCLE

CUSTOMER PERFORMS USING OWN TOOLS: Test-program generation, testability analysis.

VENDOR PERFORMS: All aspects of logic design, chip layout and design verification; test generation at user's option.

TRAINING

COURSE: Course covers design and development.

DOCUMENTATION: CMOS design manual available.

CYCLE TIMES

PROTOTYPING: 6 to 10 weeks.

INPUTS FOR COST ESTIMATION

Schematics.

PRODUCTION COMMITMENTS

None.

NCR Corp

ASIC Product Marketing
2001 Danfield Ct
Fort Collins, CO 80525
(303) 226-9500
Circle No 700

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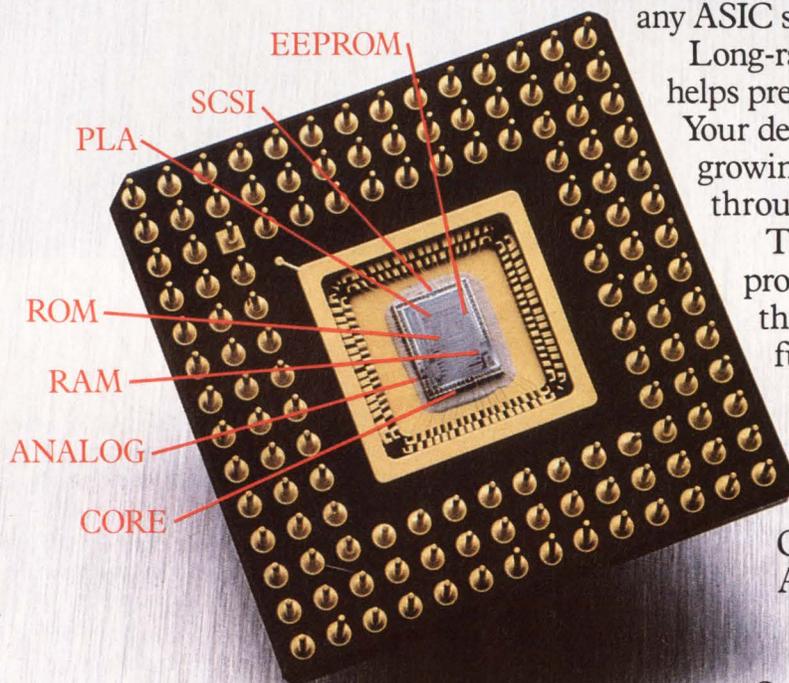
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NCR hot line 1-800-334-5454.

ONE UPMAN CHIP.



NCR

NCR Microelectronics Division

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EDN GATE-ARRAY DIRECTORY

CUSTOMER/VENDOR INTERFACE

PREFERRED: Basic specifications, schematics, verified net list, layout.

DESIGN TOOLS

Three levels of CAE options are available: 1) Schematic capture. 2) Schematic capture, simulation, timing analysis, and test generation. 3) Schematic capture, simulation, timing analysis, test generation, and layout.

WORKSTATION SUPPORT

Daisy, Mentor, Valid, and Cadnetics.

DESIGN CYCLE

CUSTOMER PERFORMS USING VENDOR'S TOOLS: Initial specification, schematic capture, simulation, timing analysis, layout, back-annotation and resimulation, test-vector generation.

VENDOR PERFORMS: Dependent on customer request.

TRAINING

COURSE: Regularly scheduled semicustom and CAE courses available at customer's site.

DOCUMENTATION: Manuals and data sheets available.

SUPPORT FACILITIES

12 locations, including northern California; Fort Collins and Colorado Springs, CO; Miamisburg, OH; and area sales offices.

CYCLE TIMES

DESIGN: 2 to 6 weeks.

PROTOTYPING: 3 to 5 weeks.

INPUTS FOR COST ESTIMATION

Block diagram, ac and dc specifications, schematics.

PRODUCTION COMMITMENTS

Negotiable; production commitment lowers engineering charges.

ALTERNATE SOURCES

Motorola.

NEC Electronics USA Inc

401 Ellis St
Mountain View, CA 94043
(415) 960-6000
Circle No 701

CUSTOMER/VENDOR INTERFACE

PREFERRED: Simulated schematic or net list.

DISCOURAGED: Unsimulated schematic or net list.

DESIGN TOOLS

NEC's CAE system supports data entry, logic simulation, timing analysis, layout, fault simulation, and automatic test generation.

WORKSTATION SUPPORT

Daisy, Mentor, Valid, FutureNet, Tektronix/CAE, and Hewlett Packard.

DESIGN CYCLE

CUSTOMER PERFORMS USING OWN OR VENDOR'S TOOLS: Partitioning analysis, schematic capture, logic and timing simulation, design-rule check.

VENDOR PERFORMS: All other steps, from logic validation to mask design.

FUNCTION LIBRARIES

TTL: Library includes 30 functions built from as many as seven 3-input gates; users can define new functions using existing library elements or discrete gates; all functions have been built and

tested; simulation parameters include ID, LD, SUH, VS, TS, PD, FI, and FO.

ECL: Libraries include as many as 70 functions built from as many as 20 2-input gates; users can define new functions using existing library elements or discrete gates; all functions have been built and tested; simulation parameters include ID, LD, SUH, VS, TS, PD, FI, and FO.

CMOS: Each library includes 150 functions with maximum complexities equivalent to 20 2-input gates; users can define new functions using existing library elements or discrete gates; all functions have been built and tested; simulation parameters include ID, LD, SUH, VS, TS, PD, FI, and FO.

TRAINING

COURSE: On an individual basis.

SUPPORT FACILITIES

Sunnyvale, CA; Dallas, TX; and Natick, MA.

CYCLE TIMES

DESIGN: 2 to 4 weeks.

PROTOTYPING: 3 to 5 weeks.

INPUTS FOR COST ESTIMATION

Estimated cell count, I/O count, packaging, production volume.

PRODUCTION COMMITMENTS

None.

ALTERNATE SOURCES

None.

Oki Semiconductor

650 N Mary Ave
Sunnyvale, CA 94086
(408) 720-1900
Circle No 702

CUSTOMER/VENDOR INTERFACE

PREFERRED: Simulated or unsimulated schematic or net list.

ACCEPTABLE: PG tape, functional block diagram.

DESIGN TOOLS

Design tools permit schematic capture, net-list generation, logic and timing simulation, fault simulation, test-program generation, and layout.

WORKSTATION SUPPORT

Mentor, Daisy.

DESIGN CYCLE

CUSTOMER PERFORMS USING OWN TOOLS: Logic design, test-vector generation, schematic capture, net-list generation, logic simulation.

CUSTOMER PERFORMS USING VENDOR'S TOOLS: All of the above.

VENDOR PERFORMS: Layout, fault simulation, test-program generation.

TRAINING

COURSE: 3-day course available; \$2000 fee waived for customers.

DOCUMENTATION: Design manual available.

SUPPORT FACILITIES

Sunnyvale, CA, and Stoneham, MA.

CYCLE TIMES

DESIGN: 2 to 3 weeks.

PROTOTYPING: 3 to 5 weeks.

EDN GATE-ARRAY DIRECTORY

INPUTS FOR COST ESTIMATION

Gate count, package, volume, special functions.

PRODUCTION COMMITMENTS

Negotiable.

Plessey Semiconductor Div

9 Parker
Irvine, CA 92718
(714) 472-0303
Circle No 703

CUSTOMER/VENDOR INTERFACE

PREFERRED: Customer performs entire design process and submits layout data.

ACCEPTABLE: Simulated net list, schematics.

DESIGN TOOLS

Plessey's CAE system runs on local DEC VAX minicomputers. The software supports chip planning, logic design, simulation, automatic routing and post-routing analysis.

WORKSTATION SUPPORT

Daisy, Mentor, Valid, FutureNet.

DESIGN CYCLE

CUSTOMER PERFORMS USING OWN OR VENDOR'S TOOLS:

Logic design, simulation, timing analysis, fault analysis, layout, post-layout simulation, test-program generation.

VENDOR PERFORMS: CAE training, design support.

FUNCTION LIBRARIES

CMOS: Library includes 115 functions; users can define new functions using existing library elements or discrete gates; all cells have been built and tested; simulation parameters include ID, LD, SUH, TS, VS, FI, and FO.

ECL: Library includes 30 functions built from as many as six 2-input gates; users must employ only predefined library elements; all cells have been built and tested; simulation parameters include ID, LD, SUH, VS, TS, PD, FI, and FO.

TRAINING

COURSE: A 3-day session available for software licensees at the company's design centers or at the customer's site.

DOCUMENTATION: Documentation available to users of company's design software.

SUPPORT FACILITIES

Irvine, CA; Marlton, NJ; Boston, MA; Dallas, TX; Gaithersburg, MD.

CYCLE TIMES

DESIGN: 2 to 6 weeks.

PROTOTYPING: 4 to 6 weeks.

INPUTS FOR COST ESTIMATION

Schematic, critical-path timing, I/O specification, packaging.

PRODUCTION COMMITMENTS

None required.

Raytheon Semiconductor

350 Ellis St
Mountain View, CA 94039
(415) 968-9211
Circle No 704

CUSTOMER/VENDOR INTERFACE

PREFERRED: Simulated or unsimulated net list or schematic.

ACCEPTABLE: Functional block diagram, layout data, PG tape.

DESIGN TOOLS

Vendor provides CAE for schematic capture, net-list generation, simulation, fault grading, layout, and test generation for digital designs. Linear designs require Spice simulation.

WORKSTATION SUPPORT

Mentor, Daisy.

DESIGN CYCLE

CUSTOMER PERFORMS USING VENDOR'S TOOLS: Logic design, simulation, net-list generation, fault grading.

VENDOR PERFORMS: Above at customer's discretion, layout.

FUNCTION LIBRARIES

CMOS: Library contains 100 SSI and MSI functions.

Bipolar: Libraries contain 25 MSI functions.

TRAINING

COURSE: A 2-day tutorial is available for \$6000.

DOCUMENTATION: Design manuals available upon design commitment.

SUPPORT FACILITIES

Mountain View, CA.

CYCLE TIMES

DESIGN: 4 to 8 weeks.

PROTOTYPING: 4 to 6 weeks.

INPUTS FOR COST ESTIMATION

Gate count, pin count, critical speed or clock frequency, temperature range.

PRODUCTION COMMITMENTS

None.

Sahni Corp

224 N Wolfe Rd
Sunnyvale, CA 94086
(408) 735-8900
Circle No 705

CUSTOMER/VENDOR INTERFACE

PREFERRED: Simulated schematic or net list, layout data generated by vendor's software.

DISCOURAGED: Functional block diagram, unsimulated schematic or net list, layout data generated using customer's software, manual layout data.

DESIGN TOOLS

Vendor uses VTI design tools and proprietary IBM PC-based tools. Kit parts for linear arrays are available for breadboarding.

DESIGN CYCLE

CUSTOMER PERFORMS USING OWN TOOLS: Partitioning analysis, testability analysis, logic design, simulation, and timing and critical-path analysis.

CUSTOMER PERFORMS USING VENDOR'S TOOLS: Building breadboard, simulation, layout, custom-cell creation.

VENDOR PERFORMS: Layout, other steps at customer's option.

TRAINING

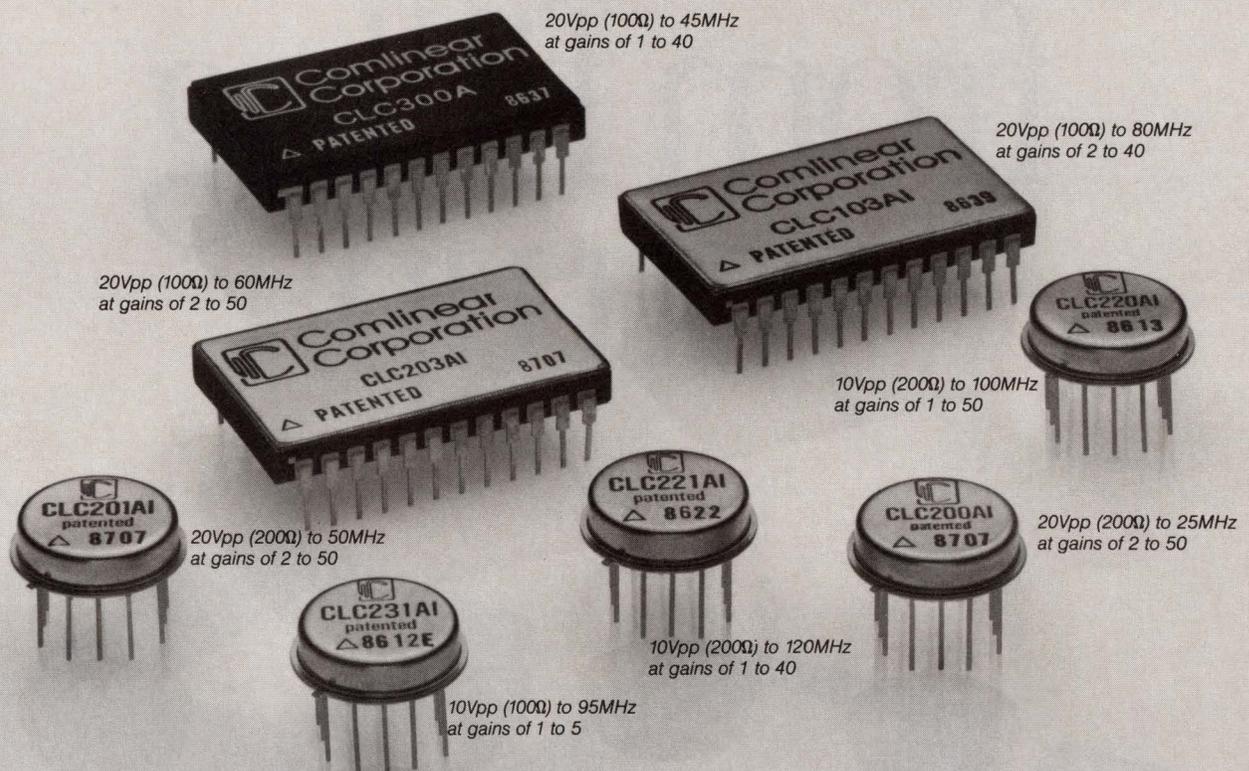
COURSE: Training available prior to design commitment.

DOCUMENTATION: Design manuals available prior to design commitment.

SUPPORT FACILITIES

Sunnyvale, CA.

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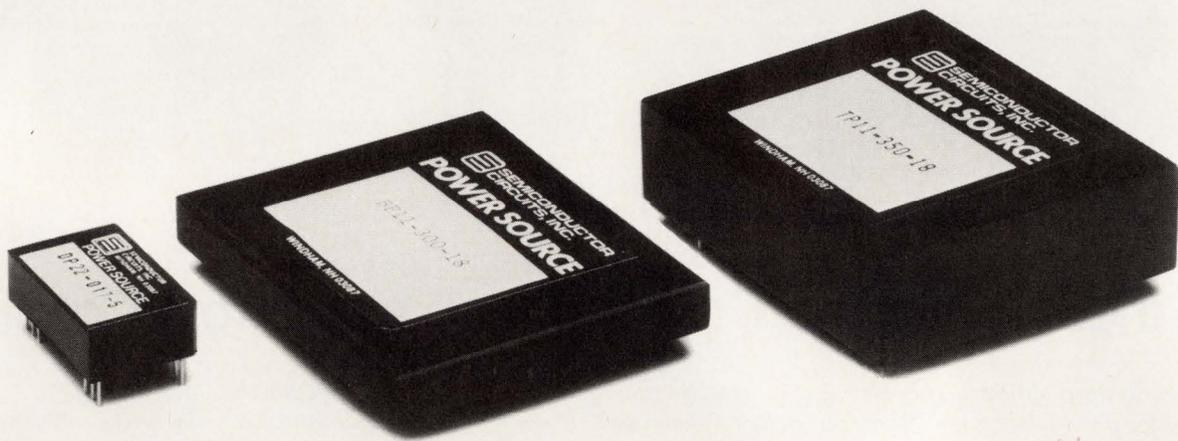
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General Purpose					
CLC103	170	130	10 (to 0.4%)	6000	11,200
CLC200	100	90	18	4000	12,100
CLC220	200	160	8	7000	12,50
CLC300	105	70	20	3000	10,100
Low Offset ($V_{os} \leq 1\text{mV}$, $10\mu\text{V}/^\circ\text{C}$)					
CLC201	100	90	18	4000	12,100
CLC203	180	130	15 (to 0.2%)	6000	11,200
CLC221	200	120	15	6500	12,50
CLC231 ¹	165 ($A_v = 1$)	120 ($A_v = 5$)	12	3000	11,100

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DP	4.75-5.25	5, 9, 12, 15, ±12, ±15	500	2.4	1.25x0.8x0.4

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EDN GATE-ARRAY DIRECTORY

CYCLE TIMES

DESIGN: 1 to 10 weeks.

PROTOTYPING: 2 to 6 weeks.

INPUTS FOR COST ESTIMATION

Packaging, gate count or logic diagram, amount of analog and digital circuitry, screening, volume.

PRODUCTION COMMITMENTS

None.

SGS Semiconductor Corp

1000 E Bell Rd
Phoenix, AZ 85022
(602) 867-6264
Circle No 706

IST Innovative Silicon Technology

Centro Direzionale Colleoni
Palazzo Orione 2
20041 Agrate Brianza, Italy
(039) 637911
(IST is a member of the SGS Group of Companies)
Circle No 707

CUSTOMER/VENDOR INTERFACE

PREFERRED: Simulated net list or schematic.

DISCOURAGED: Functional block diagram.

DESIGN TOOLS

SGS uses LDS III software running on an IBM mainframe.

WORKSTATION SUPPORT

Daisy, Mentor, Valid, FutureNet, and HILO 3.

DESIGN CYCLE

CUSTOMER PERFORMS USING OWN TOOLS: Partitioning analysis, logic design, truth tables, and timing specification.

CUSTOMER PERFORMS USING VENDOR'S TOOLS: Simulation, timing analysis, critical-path analysis, testability analysis, test-program generation.

VENDOR PERFORMS: Layout, post-layout simulation and timing analysis, tooling.

TRAINING

COURSE: A 4-day course is available.

DOCUMENTATION: Available.

SUPPORT FACILITIES

Milan, Bologna, Italy; Munich, West Germany; London, UK; Marsta, Sweden; Paris, France; Phoenix, AZ; and Singapore.

CYCLE TIMES

DESIGN AND PROTOTYPING: 3 to 4 weeks.

INPUTS FOR COST ESTIMATION

Complexity, packaging, volume, temperature, screening.

PRODUCTION COMMITMENTS

None.

Siemens AG

Balanstr 73
D 8000 Munchen 80
West Germany
(089) 4144-4253
Circle No 708

CUSTOMER/VENDOR INTERFACE

PREFERRED: Simulated net list.

DISCOURAGED: Block diagram, unsimulated net list or schematic, PG tapes.

DESIGN TOOLS

Proprietary Venus CAD system.

WORKSTATION SUPPORT

Daisy, Valid, Mentor, Siemens.

DESIGN CYCLE

CUSTOMER PERFORMS USING OWN TOOLS: Schematic capture, net-list generation.

CUSTOMER PERFORMS USING VENDOR'S TOOLS: Logic design, simulation, layout, test-program generation.

VENDOR PERFORMS: Layout, post-layout analysis, test-program generation.

TRAINING

COURSE: A course that varies in length between 2 and 5 days is available in Munich, West Germany.

DOCUMENTATION: Design manuals and cell libraries available on request.

SUPPORT FACILITIES

Munich, West Germany.

CYCLE TIMES

DESIGN: 3 to 8 weeks.

PROTOTYPING: 3 to 8 weeks.

INPUTS FOR COST ESTIMATION

Gate count, pin count, package, critical paths.

PRODUCTION COMMITMENTS

Depending on array type and complexity.

Signetics Corp

811 E Arques Ave
Sunnyvale, CA 94086
(408) 991-2000
Circle No 709

CUSTOMER/VENDOR INTERFACE

PREFERRED: Simulated net list, database tape.

DISCOURAGED: Functional block diagram.

DESIGN TOOLS

Proprietary software supports logic-rule check, timing analysis, and fault grading.

WORKSTATION SUPPORT

Mentor, Daisy.

DESIGN CYCLE

CUSTOMER PERFORMS USING OWN TOOLS: Partitioning analysis, functional simulation.

CUSTOMER PERFORMS USING VENDOR'S TOOLS: Schematic capture, logic-rules checking, simulation, test-program generation.

VENDOR PERFORMS: Layout, fault grading.

FUNCTION LIBRARIES

ECL: Library contains over 120 functions ranging in complexity from simple gates to 4-bit counters.

TRAINING

COURSE: A 4-day course is available.

DOCUMENTATION: Design manuals covering workstation use, design rules, library cells, testability, and packaging are available.

SUPPORT FACILITIES

Sunnyvale, CA.

EDN GATE-ARRAY DIRECTORY

CYCLE TIMES

DESIGN: 3 to 8 weeks.
PROTOTYPING: 8 to 10 weeks.

INPUTS FOR COST ESTIMATION

Gate count package, volumes.

PRODUCTION COMMITMENTS

Negotiable.

Silicon Systems Inc

14531 Myford St
Tustin, CA 92680
(714) 731-7110
Circle No 710

CUSTOMER/VENDOR INTERFACE

PREFERRED: Functional block diagram, simulated or unsimulated schematic or net list, layout data generated by vendor's software.

DISCOURAGED: Layout data generated by customer's software, PG tapes.

DESIGN TOOLS

SSI's CAE tools run on local minicomputers and support logic design, simulation and automatic standard-cell placement and routing. The system accepts data in schematic or net-list form.

WORKSTATION SUPPORT

Daisy, Mentor.

PRODUCTION COMMITMENTS

Estimate of 18-month production volumes.

ALTERNATE SOURCES

Plessey and MCE Semiconductors Inc.

Siliconix Inc

2201 Laurelwood Rd
Santa Clara, CA 95054
(408) 970-4107
Circle No 711

CUSTOMER/VENDOR INTERFACE

PREFERRED: Simulated schematic or net list.

DESIGN TOOLS

Logic design and simulation on workstations; timing verification and layout on IBM mainframe.

WORKSTATION SUPPORT

FutureNet, Mentor, Daisy.

DESIGN CYCLE

CUSTOMER PERFORMS USING OWN TOOLS: Schematic capture, logic verification.

CUSTOMER PERFORMS USING VENDOR'S TOOLS: Logic simulation, timing verification.

VENDOR PERFORMS: Layout, post-layout simulation.

FUNCTION LIBRARY

Library includes 125 functions built from as many as 24 2-input gates; users can define new functions using existing library elements and discrete gates; all cells have been fabricated and tested; simulation parameters include ID, LD, SUH, PD, FI, and FO.

TRAINING

COURSE: None offered.

SUPPORT FACILITIES

Santa Clara, CA; Boston, MA; and Swansea, UK.

CYCLE TIMES

DESIGN: 2 to 6 weeks.
PROTOTYPING: 4 to 8 weeks.

INPUTS FOR COST ESTIMATION

Array type, gate count, package type, screening requirements.

PRODUCTION COMMITMENTS

Only for guaranteed delivery.

ALTERNATE SOURCES

Universal Semiconductor Inc, Array Technology Corp; alternate sourcing effected through PG-tape transfer. Western Digital Inc serves as an alternate wafer source.

SMOS Systems

2460 N First St
San Jose, CA 95131
(408) 922-0200
Circle No 712

CUSTOMER/VENDOR INTERFACE

PREFERRED: Simulated net list, schematic and test vectors.

ACCEPTABLE: Layout generated by customers.

DISCOURAGED: Functional block diagram, schematic without test vectors.

DESIGN TOOLS

LADS (proprietary S-MOS Logic Array Design System); CAL-MP, TANCELL, GALS, DCS, DVS.

WORKSTATION SUPPORT

Daisy, Mentor, IBM PC-XT/AT (or compatibles), FutureNet, OrCAD, Viewlogic.

DESIGN CYCLE

VENDOR PERFORMS: Logic design and simulation, test-program generation, auto placement and routing, and post-layout simulation.

TRAINING

COURSE: A 3-day course for inexperienced users or self-teaching with users guide.

SUPPORT FACILITIES

Design centers: San Jose, CA: nine engineers; six IBM PC/ATs, two Compaq 386s, and one Daisy, one Mentor, one Micro Vax II, one Interpro 32, one Calma GDS 2; and IBM mainframe. Boston MA: one engineer; IBM PC/AT. Baltimore and Orlando.

CYCLE TIMES

DESIGN AND PROTOTYPING: 5 to 7 weeks after simulation.

INPUTS FOR COST ESTIMATION

Schematic and test vectors, package, quantity, delivery schedule.

ALTERNATE SOURCES

Siliconix, AMCC, IMI.

Sorep SA

ZJ Bellevue
BP5 35220 Chateaubourg
France
(33) 99623955
Circle No 713



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North Carolina
27709-3625.



SIECOR

In Surface Mountable Components, TDK Quality Is More Than Skin Deep.

As boards are getting thinner, TDK is helping that diet succeed by providing a variety of extra-slim surface mountable components. Nourished by TDK's expertise in ferrite and ceramic materials, these miniaturized components feed on TDK—developed multi-layerization and multi-functionalism.

How do we know the exact needs of high-quality automated board production? Well, a fair share of the world's automatic mounting equipment—the Avimount series—comes from TDK.



Product name	Type	Shape	Dimensions			Electrical Characteristics
			L (mm)	W (mm)	T (mm)	
Multilayer Ceramic Chip Capacitor	C1608		1.6	0.8	0.8	C: 0.5 ~ 470pF, 100 ~ 22,000pF
	C2012		2.0	1.25	0.6 0.85 1.25	C: 0.5 ~ 1,800pF C: 470 ~ 100,000pF
	C3216		3.2	1.6	0.6 0.85 1.1	C: 0.5 ~ 270pF C: 470 ~ 220,000pF
	C3225		3.2	2.5	1.9 max.	C: 750 ~ 8,200pF, 56,000 ~ 470,000pF
	C4532		4.5	3.2	1.9 max.	C: 2,400 ~ 18,000pF, 180,000pF ~ 1μF
Multilayer Ceramic Chip Capacitor (High Frequency, Low Loss)	FC1414		1.4	1.4	1.6	C: 0.5 ~ 100pF, 150 ~ 3,300pF
	FC2828		2.8	2.8	2.8	C: 0.5 ~ 1,000pF, 470 ~ 22,000pF
	FR1414		1.4	1.4	1.6	C: 0.5 ~ 100pF, 150 ~ 3,300pF
	FR2828		2.8	2.8	2.8	C: 0.5 ~ 1,000pF, 470 ~ 22,000pF
	Leadless Inductor (Wound Chip Inductor)		NL322522		3.2	2.5
NL453232		4.5	3.2		3.2	L: 1.0 ~ 1,000μH
NL565050		5.6	5.0		5.0	L: 1,200 ~ 10,000μH
NLF453232		4.5	3.2		3.2	L: 1.0 ~ 1,000μH (Shielded Inductor)
Multilayer Chip Inductor	MLF3216		3.2	1.6	0.6 1.1	L: 0.047 ~ 220μH
	MLF3225		3.2	2.5	1.1 1.8 2.5	
	MTT4532		4.5	3.2	2.8 max.	
Multilayer Chip Transformer	MIA4532		4.5	3.2	2.8	F: 455, 459, 464kHz
Multilayer Chip IFT	MIF4532		4.5	3.2	2.2	F: 10.7MHz
Multilayer Chip LC Trap	MXT4532		4.5	3.2	2.8 max.	F: fo ±2%
Multilayer Chip LC Filter	HPF (Tuner)	MXF4532H	4.5	3.2	2.8 max.	A variety of characteristics are available. Please specify when ordering.
	BPF (FM radio)	MXF4532B	4.5	3.2	2.8 max.	
	BPF (VCR)	MXB5050B	5.0	5.0	2.8 max.	
	LPF (VCR)	MXB5050L	5.0	5.0	2.8 max.	
	Equalizer (VCR)	MXB5050E	5.0	5.0	2.8 max.	
	Delay Line (VCR)	MXB5050D	5.0	5.0	2.8 max.	
Multilayer Chip Capacitor Network	MCN7575		7.5	7.5	0.9	C: 1 ~ 100pF (TC:CH) (10 capacitors) C: 10 ~ 1,000pF (TC:SL) (10 capacitors)
Ferrite Chip Bead	CB201209		2.0	1.25	0.9	Zo: 7, 10, 11Ω
	CB321611		3.2	1.6	1.1	Zo: 19, 26, 31Ω
	CB322513		3.2	2.5	1.3	Zo: 31, 52, 60Ω
	CB453215		4.5	3.2	1.5	Zo: 70, 120, 125Ω
SM Active Delay Line	FDL		12.0	9.5	5.6	Delay time: 20 ~ 250 nsec.
SM Transformer/ Inductor	EE5		7.4	5.3	4.75	A variety of characteristics are available. Please specify when ordering.
	ER9.5		11.5	9.5	6.3	
	ER11		12.5	11.0	6.3	
	T2		7.0	5.0	2.2	
SMD Step-up Inductor (Piezoelectric Buzzer)	OL3.3 × 1.6		5.4	3.3	1.6	Inductance values are representative. Please specify value when ordering.
	OL3.3 × 2.1		5.4	3.3	2.1	



TDK CORPORATION OF AMERICA HEAD OFFICE 4711 West Golf Road, Skokie, IL 60076, U.S.A. Phone: (312) 679-8200 CHICAGO REGIONAL OFFICE 4711 West Golf Road, Skokie, IL 60076 Phone: (312) 679-8200 INDIANAPOLIS REGIONAL OFFICE 4015 West Vincennes Road, Indianapolis, IN 46268 Phone: (317) 872-0370 NEW YORK REGIONAL OFFICE 12 Harbor Park Drive, Port Washington, NY 11050 Phone: (516) 625-0100 LOS ANGELES REGIONAL OFFICE 3102 Kashiwa Street, Torrance, CA 90505 Phone: (213) 539-6631 DETROIT DISTRICT OFFICE 3000 Town Center, Suite 2239, Southfield, MI 48075 Phone: (313) 353-9393 NEW JERSEY DISTRICT OFFICE 100 Executive Drive, Suite 310, West Orange NJ 07052 Phone: (201) 736-0023 HUNTSVILLE DISTRICT OFFICE 303 Williams, Suite 1032, Huntsville, AL 35801 Phone: (205) 539-4551 GREENSBORO DISTRICT OFFICE 620 Green Valley Road, Suite 302, Greensboro, NC 27408 Phone: (919) 292-0012 DALLAS DISTRICT OFFICE 511E. Carpenter Feeway, Suite 420 Irving, TX 75039 Phone: (214) 506-9800 SAN FRANCISCO DISTRICT OFFICE 2254 North First Street, San Jose, CA 95131 Phone: (408) 435-8565 TDK CORPORATION, TOKYO, JAPAN.

EDN GATE-ARRAY DIRECTORY

DESIGN TOOLS

Design tools run on VAX 11/750.

TRAINING

COURSE: A 5-day course is available.

CYCLE TIMES

DESIGN: 6 to 8 weeks.

PROTOTYPING: 6 to 8 weeks from PG tape.

STC Microtechnology

2270 S 88th St
Louisville, CO 80027
(303) 673-5151

Circle No 714

CUSTOMER/VENDOR INTERFACE

PREFERRED: Simulated schematic or net list, layout data generated by vendor's software.

ACCEPTABLE: Unsimulated schematic or net list.

DESIGN TOOLS

STC's CAE system supports design entry and simulation tasks. Users enter data through remote alphanumeric terminals.

DESIGN CYCLE

CUSTOMER PERFORMS USING OWN TOOLS: Partitioning analysis, block-level functional simulation, logic design and minimization.

CUSTOMER PERFORMS USING VENDOR'S TOOLS: Critical-path analysis.

VENDOR PERFORMS: Logic simulation, timing analysis, testability analysis, fault grading, test-program generation, automatic gate-array placement and routing, post-routing simulation.

FUNCTION LIBRARY

Library includes 43 functions composed of as many as 15 2-input logic gates; users can define new functions using existing library elements; all library cells have been built and tested; simulation parameters include ID, LD, SUH, VS, TS, FI, and FO.

TRAINING

COURSE: None offered.

DOCUMENTATION: Design manuals are available prior to design commitment; \$100.

SUPPORT FACILITIES

Louisville, CO.

CYCLE TIMES

DESIGN: 6 to 8 weeks.

PROTOTYPING: 6 to 8 weeks.

INPUTS FOR COST ESTIMATION

Circuit size, package type.

PRODUCTION COMMITMENTS

None required.

ALTERNATE SOURCES

None.

Telmos Inc

1925 Zanker Rd
San Jose, CA 95112
(408) 436-1906
Circle No 715

CUSTOMER/VENDOR INTERFACE

PREFERRED: Schematic, logic diagram, net list.

DISCOURAGED: Breadboard, functional block diagram, layout data, PG-tapes.

DESIGN TOOLS

Daisy workstation tools support front-end design; Calma and Dracula software supports back-end design.

WORKSTATION SUPPORT

Daisy, Calma.

DESIGN CYCLE

CUSTOMER PERFORMS USING OWN TOOLS: Schematic capture, logic design.

CUSTOMER PERFORMS USING VENDOR'S TOOLS: Schematic capture, analog and digital simulation and verification, test-pattern and test-program generation, breadboard development.

FUNCTION LIBRARIES

Libraries include 100 functions built from as many as 50 2-input gates; users can define new cells using existing library elements or discrete gates; 85 to 90% of each library has been built and tested; simulation parameters include ID, LD, SUH, VS, TS, FI, and FO.

TRAINING

COURSE: Training tailored to customer's needs.

SUPPORT FACILITIES

KMOS in Santa Clara, CA; Timark in Indianapolis, IN; Silicon Development Corp in Huntington Beach, CA, and Wakefield, MA; Integration SA in France; Dainichi Electronics in Japan; Sagantes bv in the Netherlands; Nordic VLSI in Norway; Chartered-Telmos Design Ltd in Singapore; Sicon AB in Sweden; and GME in West Germany.

CYCLE TIMES

DESIGN: 2 to 12 weeks.

PROTOTYPING: 3 to 4 weeks.

INPUTS FOR COST ESTIMATION

Maximum clock frequency, operating voltage, pin count, package type, delivery, volume.

PRODUCTION COMMITMENTS

None.

ALTERNATE SOURCES

California Devices Inc.

Texas Instruments Inc

Box 225474
8390 LBJ Freeway
Dallas, TX 75265
Phone local sales office.
Circle No 716

CUSTOMER/VENDOR INTERFACE

PREFERRED: Simulated schematic or net list, logic and test data.

ACCEPTABLE: Functional block diagram, unsimulated schematic or net list, layout data, tooling database.

DESIGN TOOLS

Schematic capture and simulation occurs on workstations.

WORKSTATION SUPPORT

Daisy, Mentor, Valid, and P-CAD.

DESIGN CYCLE

CUSTOMER PERFORMS USING OWN TOOLS: Partitioning analysis, functional simulation, logic design and simulation, timing analysis, testability analysis, test-program generation, fault-grad-

EDN GATE-ARRAY DIRECTORY

ing, layout, post-layout simulation.

CUSTOMER PERFORMS USING VENDOR'S TOOLS: Functional simulation, logic design and simulation, timing analysis, test-pattern generation.

VENDOR PERFORMS: Custom cell creation, network-equivalency check; logic and post-routing simulation as data check; layout tasks at customer's option.

FUNCTION LIBRARIES

Libraries include 100 functions using as many as 60 2-input NAND gates; users can define new functions based on existing library elements; all functions have been built and tested; simulation parameters include ID, LD, SUH, VS, TS, FI, and FO.

TRAINING

COURSE: A 3-day session is offered at all regional technology centers; tuition is refunded upon design commitment.

DOCUMENTATION: Manuals available without design commitment.

SUPPORT FACILITIES

Chicago, IL; Boston, MA; Atlanta, GA; Dallas, TX; Santa Clara and Irvine, CA; Ottawa, Ontario, Canada; Europe; and Japan.

CYCLE TIMES

DESIGN: 3 to 6 weeks.

PROTOTYPING: 4 to 6 weeks.

INPUTS FOR COST ESTIMATION

Gate and I/O counts, package type, drive requirements, volume.

PRODUCTION COMMITMENTS

None required.

ALTERNATE SOURCES

Fujitsu. All alternate sourcing effected through PG-tape transfer.

Thomson Components-Mostek Corp

MS775 ASIC Products
1310 Electronics Dr
Carrollton, TX 75006
Circle No 717

CUSTOMER/VENDOR INTERFACE

PREFERRED: Simulated net list and test vectors.

ACCEPTABLE: Detail schematic and timing diagrams.

DESIGN TOOLS

VAX mainframe-based TCAD2 system from schematic capture to manufacturing and test tooling. Libraries and translators for popular Engineering Work Stations (EWS) and PC-based design systems.

WORKSTATION SUPPORT

Daisy, Mentor, IBM PC-compatible systems.

DESIGN CYCLE

CUSTOMER PERFORMS USING OWN TOOLS: System and logic design, functional simulation, test pattern generation and coverage.

CUSTOMER PERFORMS USING VENDOR'S TOOLS: Timing simulation, critical-path analysis, fault grading, trans to vendor database format.

VENDOR PERFORMS: Layout, post-layout simulation, DRC, ERC, tooling, and test program generation.

TRAINING

COURSE: A 2-day training at customer site for EWS-based interface. A 5-day course in Carrollton, TX, for VAX-based interface.

DOCUMENTATION: Design manuals, data sheets, and application notes are available upon request.

SUPPORT FACILITIES

Carrollton, TX; Scottsdale, AZ; Grenoble and Velizy, France; Milan, Italy; Munich, Germany; and Basingstoke, UK.

CYCLE TIMES

DESIGN AND PROTOTYPING: CMOS: 18 working days. **Bipolar:** 28 working days.

INPUTS FOR COST ESTIMATION

Gate and I/O count, package style, temperature and manufacturing process screening level, quantity, and interface selection.

PRODUCTION COMMITMENTS

None required.

ALTERNATE SOURCES

AMI, Thomson Semiconducteurs.

TLSI Inc

790 Park Ave
Huntington, NY 11743
(516) 549-6300
Circle No 718

CUSTOMER/VENDOR INTERFACE

PREFERRED: Logic diagram, schematic, specification.

WORKSTATION SUPPORT

Daisy.

SUPPORT FACILITIES

Huntington, NY.

CYCLE TIMES

DESIGN: 2 to 8 weeks.

PROTOTYPING: 6 weeks.

INPUTS FOR COST ESTIMATION

Logic diagram or functional block diagram.

PRODUCTION COMMITMENTS

Preferred.

Toshiba America

1220 Midas Way
Sunnyvale, CA 94086
(408) 733-3223
Circle No 719

CUSTOMER/VENDOR INTERFACE

PREFERRED: Simulated or unsimulated schematic or net list.

DESIGN TOOLS

Toshiba's CAE system includes simulation, layout, and test-program generation.

WORKSTATION SUPPORT

Daisy, Mentor, Valid, FutureNet, Viewlogic, HP.

DESIGN CYCLE

CUSTOMER PERFORMS USING OWN TOOLS: Schematic capture.

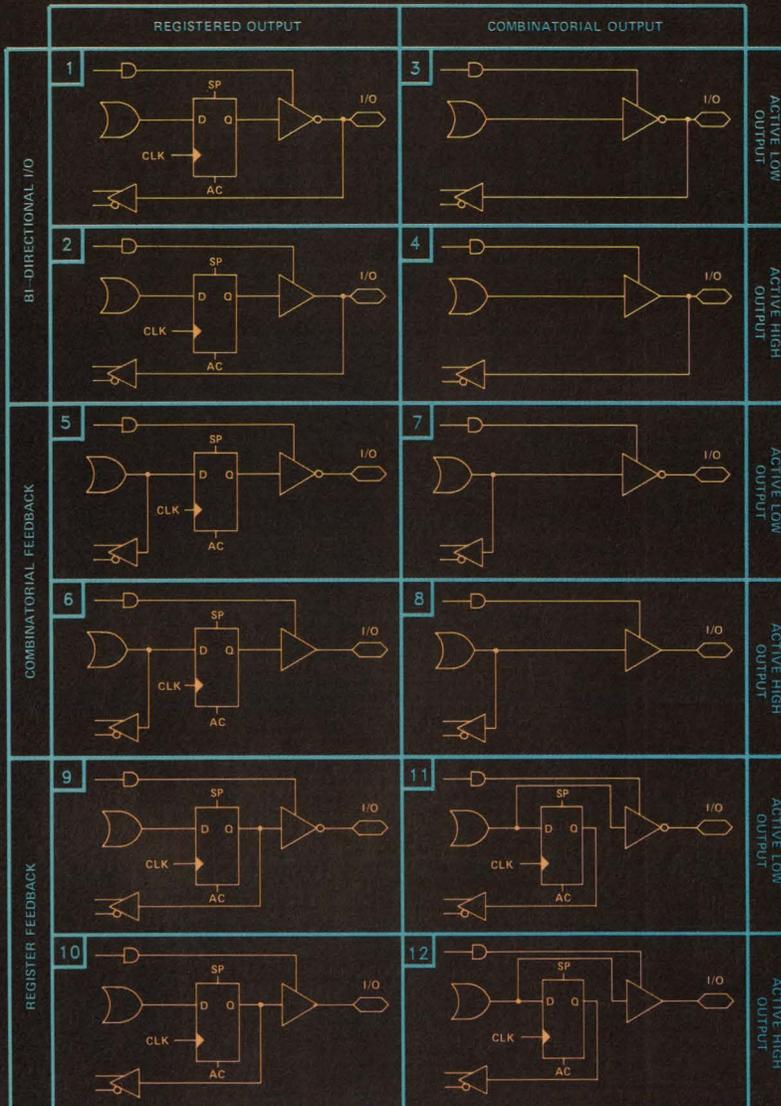
CUSTOMER PERFORMS USING VENDOR'S TOOLS: Schematic capture and simulation.

VENDOR PERFORMS: Layout and simulation.

FUNCTION LIBRARY

Users can build new functions from library elements or discrete gates; all functions have been built and tested; simulation parameters include ID, LD, SUH, VS, TS, PD, FI, and FO.

Elegant logic has a certain aPEEL.



1=12 Each I/O on a PEEL™ programmable electrically erasable logic device can be configured any one of twelve ways. So you can emulate over 30 conventional PLDs — and develop over a hundred new configurations — all with a single PEEL device.

The PEEL18CV8 is the first device in a new family of PEEL parts. It provides up to 18 inputs and eight I/Os each with independent output enables. PEEL twelve configuration I/O macro cells allow for a variety of registered and combinatorial logic functions to be implemented independently on each I/O pin. PEEL flexibility allows you to put more logic into one package. The PEEL-18CV8 emulates the majority of 20-pin PAL® devices and the EP310/320, dramatically reducing the number of different parts you need to carry in inventory. It also serves as a high-performance replacement for SSI/MSI logic, and a low-risk option to low-density gate arrays.

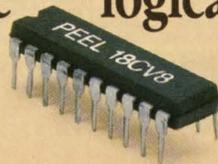
Elegant architecture is just the beginning. The PEEL18CV8 is fabricated with high-speed, low-power CMOS EEPROM technology. It erases and reprograms instantly, letting you perform design modifications or field retrofits quickly and without waste.

Unlike bipolar fuse-link PLDs, EE reprogrammability keeps your cost of PLD ownership down two ways. PEEL parts come in low cost windowless packages that are not available with UV-erasable PLDs. And every PEEL part is 100% factory tested for program and function.

The shift to PEEL devices is virtually painless. Our Instant Prototype Kit has all of the PC-based software you need for a fast, smooth transition from other PLDs to the PEEL18CV8. A JEDEC file translator automatically converts your existing PLD design to a PEEL device for easy evaluation. The kit can be yours at no charge by calling International CMOS Technology at (408) 434-0678.

If you act now, we'll also include coupons for programming two PEEL devices for you, absolutely free. Start putting elegant logic to work in your systems right away.

PEEL the logical choice™



INTERNATIONAL CMOS TECHNOLOGY, INC.

2031 Concourse Drive, San Jose, CA 95131 (408) 434-0678
FAX (408) 434-0688 Telex 910 997 1531

CIRCLE NO 124

There's only one thing our FIFOs won't do that our competitors' will. Eat power.



In fact, Plessey's MV66000 FIFOs consume a maximum of 40mA. That's almost half the current of the lowest power CMOS FIFO currently available. Anywhere.

And our FIFOs are available now. In quantity. (Unlike some of our competitors).

Plessey's 66000 Series is cascadable to 25MHz. Guaranteed. (That's something our competitors won't do).

If you should need even higher speed operation, Plessey's 65000 Series accommodates today's fastest clock rates. (Think in terms of 40MHz). All without the large

power requirements of slower NMOS and Bipolar FIFOs.

And Plessey has the only FIFOs with extremely low standby currents. Our fully static CMOS design means that standby currents less than 10mA are experienced. Even at 5.5 volts.

The family

MV 66000	64x4,5,9 bit FIFOs, 25 MHz
MV 65000	64x4,5,9 bit FIFOs, 40 MHz
MV 61900	1Kx9 bit FIFOs, 10 MHz

Package options include ceramic and plastic DIL and LCC.

Plessey FIFOs are pin compatible with MMI, Cypress, TRW and others. In 4, 5 and 9 bit widths. With or without 3-state outputs.

So you can replace those power-hungry FIFOs with Plessey's CMOS FIFOs. They do everything our competitors' do. For less power.

Call customer service in Swindon (0793) 726666. Fax: (0793) 726666 Ext. 250. After-hours Fax: (0793) 729412. Tx: 444410. In the United States, call (800) 321-0871 or (714) 472-0303. Telex 701464. Fax: (714) 770-0627.



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These are supported by agents and distributors in major countries worldwide.

Plessey and the Plessey symbol are registered trademarks of the Plessey Company plc.

EDN GATE-ARRAY DIRECTORY

TRAINING

DOCUMENTATION: Design manuals are available upon request.

SUPPORT FACILITIES

Burlington, MA; Dallas, TX; Sunnyvale and Newport Beach, CA; Atlanta, GA.

CYCLE TIMES

DESIGN: 2 to 5 weeks.

PROTOTYPING: 4 to 6 weeks.

INPUTS FOR COST ESTIMATION

Gate count and package.

PRODUCTION COMMITMENTS

Negotiable.

ALTERNATE SOURCES

LSI Logic; alternate sourcing effected through transfer of PG tape, layout data, or net list.

TriQuint Semiconductor

Group 700, Box 4935

Beaverton, OR 97075

(503) 629-4227

Circle No 720

CUSTOMER/VENDOR INTERFACE

PREFERRED: Net list.

DISCOURAGED: Schematic.

DESIGN TOOLS

Tools provide schematic capture, simulation, and net-list generation.

WORKSTATION SUPPORT

Daisy, Tektronix/CAE, Mentor.

DESIGN CYCLE

CUSTOMER PERFORMS USING OWN TOOLS: Design, simulation, net-list generation.

CUSTOMER PERFORMS USING VENDOR'S TOOLS: Design, simulation, net-list generation.

VENDOR PERFORMS: Layout, back annotation and resimulation.

FUNCTION LIBRARY

Library includes 235 macrocells including I/O cells that support CMOS, ECL, and TTL I/O signal levels.

TRAINING

DOCUMENTATION: Designer's guide, library documentation, workstation user's guide, evaluation kit.

SUPPORT FACILITIES

Beaverton, OR.

CYCLE TIMES

DESIGN: 2 to 4 weeks.

PROTOTYPING: 8 to 12 weeks.

INPUTS FOR COST ESTIMATION

Number of circuits/complexity.

PRODUCTION COMMITMENTS

Negotiable.

Universal Semiconductor Inc

1925 Zanker Rd

San Jose, CA 95112

EDN June 25, 1987

(408) 436-1906

Circle No 721

CUSTOMER/VENDOR INTERFACE

PREFERRED: Layout data generated by vendor's software.

ACCEPTABLE: Simulated schematic or net list, layout data generated by customer's software.

DISCOURAGED: Functional block diagram, unsimulated schematic or net list.

DESIGN TOOLS

Universal Semiconductor offers a CAE system that runs on an IBM PC and supports design-entry logic simulation and timing verification.

WORKSTATION SUPPORT

Daisy, Mentor, Valid.

DESIGN CYCLE

CUSTOMER PERFORMS USING OWN TOOLS: Partitioning analysis.

CUSTOMER PERFORMS USING VENDOR'S TOOLS: Functional simulation, logic design and simulation, timing analysis.

VENDOR PERFORMS: Testability analysis, test-program generation, fault grading, chip layout, post-layout analysis.

FUNCTION LIBRARIES

Libraries include 35 functions; most complex cell employs 60 2-input gates; users can define and store functions built from predefined cells or from discrete gates; 90% of all library cells have been built and tested; simulation parameters include ID, LD, VS, TS, PD, FI, and FO.

SUPPORT FACILITIES

Los Angeles, CA; Boca Raton, FL; Ottawa, Ontario, Canada; and Dallas, TX.

CYCLE TIMES

DESIGN: 3 to 5 weeks.

PROTOTYPING: 1 to 2 weeks.

INPUTS FOR COST ESTIMATION

Gate and pin counts, package style, operating frequency.

PRODUCTION COMMITMENTS

None required.

ALTERNATE SOURCES

Siliconix Inc; alternate sourcing effected at any level. Western Digital Inc serves as an alternate wafer source.

VLSI Technology Inc

1109 McKay Dr

San Jose, CA 95131

(408) 434-3000

Circle No 722

CUSTOMER/VENDOR INTERFACE

PREFERRED: Simulated schematic or net list.

DESIGN TOOLS

VLSI Technology's VLSI Design Tools System for design entry, systems partitioning, timing verification, simulation, physical design, and verification. The VLSI Design Tools System runs on Apollo, Eixsi, HP 9000/300, Ridge, VAX, Micro VAX, and SUN computer platforms.

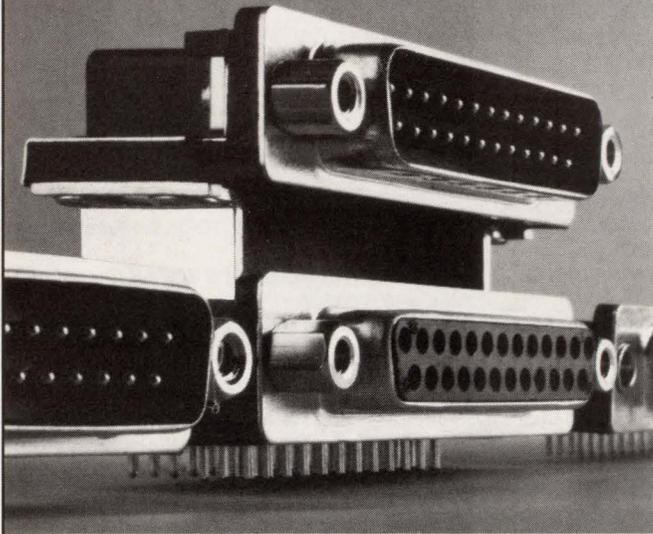
WORKSTATION SUPPORT

Contact your local VLSI Technology representative.

DESIGN CYCLE

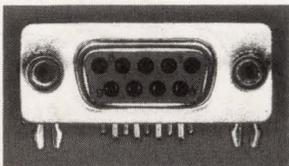
CUSTOMER PERFORMS USING OWN OR VENDOR'S TOOLS:

Highrise Architecture

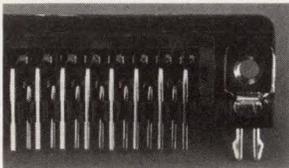


Make Smarter Real Estate Deals with Maxconn's Full Selection of Stacked D-Subs

Stacking D-sub is one of the smartest ways to maximize board real estate. Especially when you choose Maxconn Highrise™ Stacked D-sub.



Bracket-mounted D-sub



Maxconn Stacked D-sub come in a variety of styles to offer the greatest design freedom: 9- to 37-pin sizes, in all genders, and in a range of pin heights and lengths. You can even select floor-to-floor space options.

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Highrise is a trademark of
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*Patent pending.

EDN GATE-ARRAY DIRECTORY

Systems partitioning, logic design and simulation, timing analysis, fault simulation, post-routing simulation, and test development.

VENDOR PERFORMS: Placement and routing, network-equivalence check, and design-rules check. Also, any design step at customer's option.

FUNCTION LIBRARIES

VLSI Technology offers over 40 high-level functions from its Datapath Compiler library and also offers its Portable library of over 260 functions. The Portable and Datapath libraries contain identical functions for both gate arrays and standard cells. Thus, these libraries provide designers with a high degree of flexibility in implementing ASIC designs. The design can first be built on a gate array, and then, without having to re-enter the design, as a cell-based chip for high-volume production.

TRAINING

COURSE: A 1-day gate-array design course is offered. Also offered are 5-day basic and 5-day advanced courses. The 5-day courses cover topics such as hierarchical design, partitioning, and ASIC methodologies including gate array, standard cell, megacell, and silicon compilation. Extensive laboratory sessions and design examples are used throughout the courses. Courses are taught at VLSI Technology's San Jose, CA, and Boston, MA, design centers.

DOCUMENTATION: Design manuals and application notes are available.

SUPPORT FACILITIES

San Jose, CA; Boston, MA; Dallas, TX; Irvine, CA; Chicago, IL; Munich, West Germany; and Ivera, Italy.

CYCLE TIMES

DESIGN: 1 to 10 weeks.

PROTOTYPING: 3 to 6 weeks.

INPUTS FOR COST ESTIMATION

Estimated gate count, logic schematic, functions, package.

PRODUCTION COMMITMENTS

None.

ALTERNATE SOURCES

Fairchild; alternate sourcing effected through transfer of PG tapes.



Memories designed to stand the test of time ...and temperatures of -55°C to $+200^{\circ}\text{C}$.

No one likes to lose their memory...especially when it's Static RAM or CMOS EEPROM and buried in the middle of a critical microcomputer system. Our broad new family of high-performance hybrid memories is designed to be extremely reliable even in the most severe environments.

And, while very few off-the-shelf memories are designed to operate beyond the 125°C Military temperature range, ours are comfortable anywhere between -55°C to $+200^{\circ}\text{C}$. They're rugged, compact, and ideal for those tough temperature-critical High-Performance Commercial, Hi-Rel Military, and the most demanding Extended-Temperature applications. They're designed to last over time, and over temperature.

- STATIC RAMS in 8kx8, 16kx8, 64kx8, and 128kx8 configurations. Burned-in and fully tested at 200°C , with 150nSec access time and operating currents as low as 5mA.
- PROGRAMMABLE CMOS EEPROMS in 2kx8, 8kx8, 32kx8,

64kx8, and 128kx8 configurations. Three-State output, re-programmable up to 180°C , and can be read at temperatures through 200°C . Internal compensation, and 250nSec access time @ 200°C .

- COMING SOON!! A 200°C 4-Megabit SRAM with user-selectable organizations of 512kx8, 256kx16, or 128kx32 in a 2"x2" flat-pack.

Packaging is no problem either. These memories are available in ceramic, hermetic metal DIPS, and hermetic metal flat-packs. If you don't need 200°C operation, you can order the -55°C to $+125^{\circ}\text{C}$ Military version. Some Commercial temperature range devices are available, and, of course, we will make customs.

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**New cell compilers can
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really blossom,**



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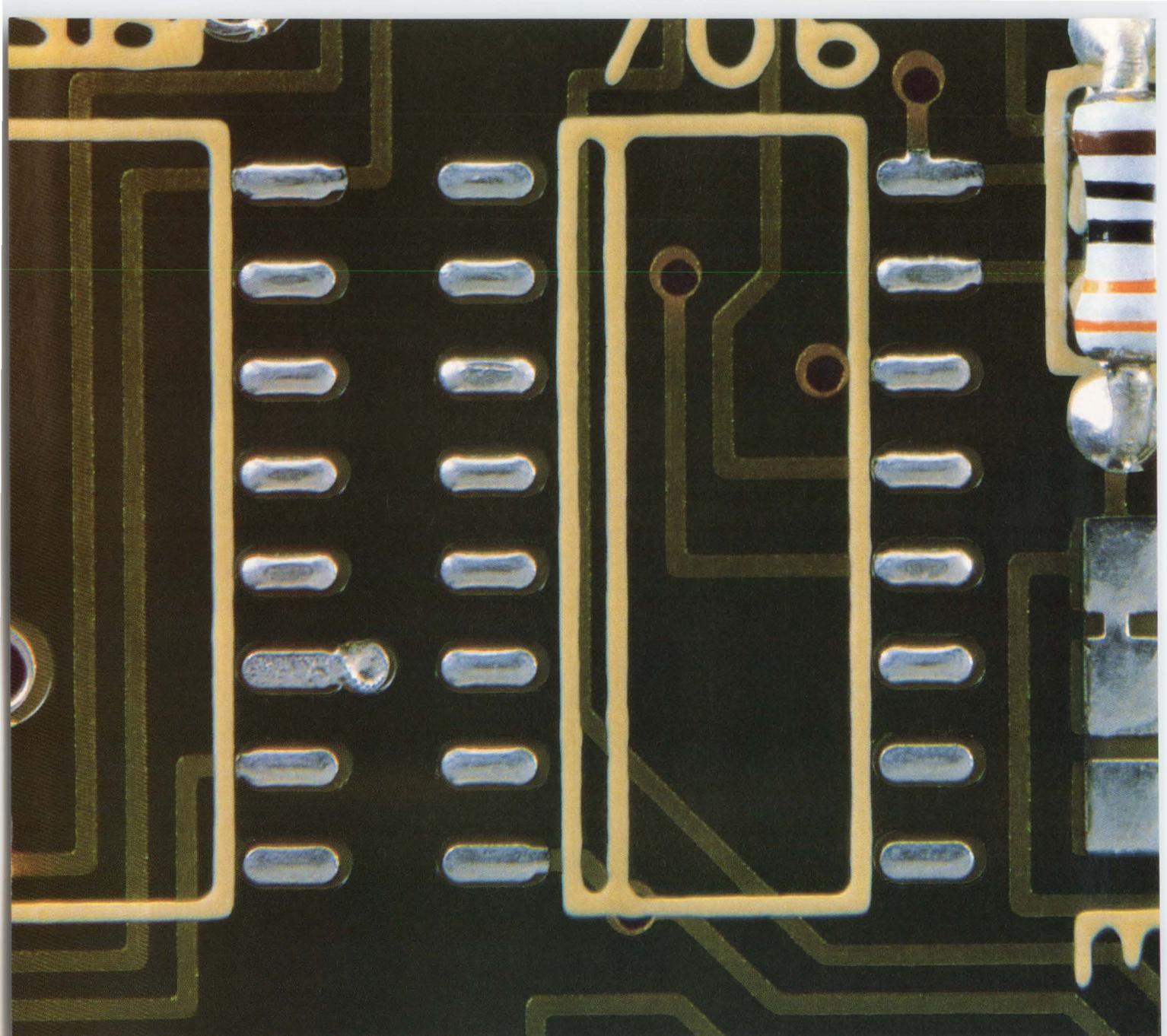
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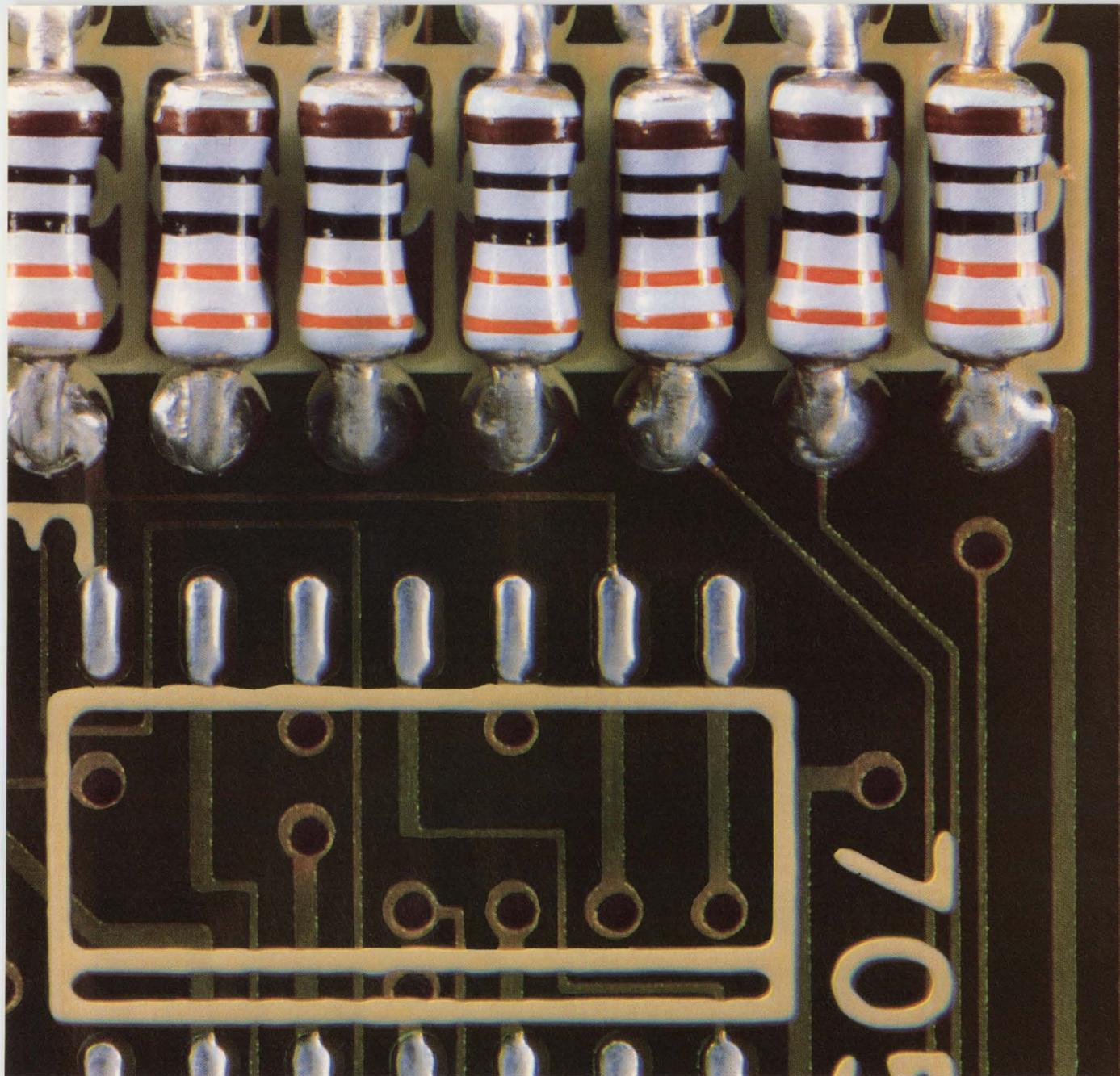
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VACREL photopolymer film solder mask (left). Total encapsulation means less damage in assembly, greater reliability in use, and reduced potential for field failures. Screen-printed solder mask (right) may leave voids, pinholes, and incomplete encapsulation.

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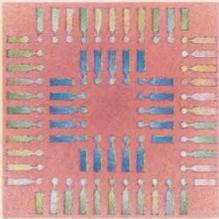
With the parts list completely converted to SMT components, we were ready to tackle the design of our SMT project board using a high-end, pc-board CAD system. What we learned about the features required to perform CAD-based SMT design applies to all CAD systems from low-end, PC-based tools to the most expensive workstations.

Lead pitches on SMT components have reached 50 mils today and will drop to 40 or 25 mils tomorrow, so you can't readily use tape, ruby-lith, and an X-acto knife to design complex, manufacturable SMT pc boards. The fine-line geometries used on SMT boards make the use of a CAD

system almost mandatory. Many CAD vendors claim that their products support SMT design, but you should be aware that these design tools have varying levels of capability. Our encounter with SMT pc-board design demonstrates the features you should look for in a pe-

Steven H Leibson, *Regional Editor*

Illustration by Michael Young



board CAD package.

Our SMT memory board, although moderately complex, does not push the limits of pc-board fabrication or SMT assembly processes. Nevertheless, it allowed us to experience and solve many problems associated with the technology. We spent extra time and effort relaxing clearances between traces and pads on the board to make our design as manufacturable as possible.

Picking out the patterns

Before sitting down at our CAD workstation, we needed to select the pad patterns. SMT Plus had given us an excellent set of patterns from the class we attended

passive-component pad patterns, we decided to use AVX's recommendations for our 1206 chip capacitors and resistors.

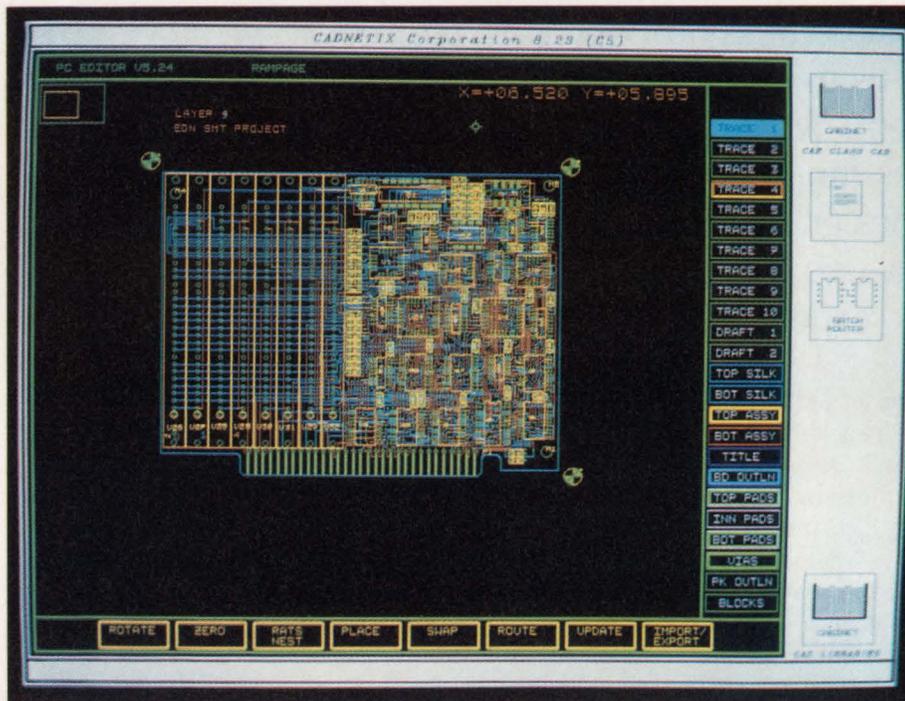
We also received pad-pattern recommendations from Dr Charles Hutchins at Texas Instruments, who agreed to help us assemble our boards. Dr Hutchins manages TI's SMT laboratory and supervises the company's SIP-memory-module assembly line. His pad recommendations are based on experiences with these two operations. TI's SIP manufacturing line uses large quantities of PLCC memory devices to build memory modules, so based on that experience, we decided to use Dr Hutchins's PLCC pad patterns, which are published in **Ref 3**.

A few of our components were odd enough that none of our sources offered pad recommendations for them. These devices included Molex's surface-mountable SIMM (single-in-line memory module) socket, Augat's Alcoswitch SMD switches, Dallas Semiconductor's DS1000 silicon delay line (in the SMD conversion of an 8-pin DIP), and Burndy's pin header. Fortunately, these products' manufacturers supplied pad patterns for their devices in the component data sheets. Having no alternatives, we adopted the manufacturers' recommendations.

Specs for ghost components

Two critical geometries did not come from component specifications but from our pc-board fabricator. We determined trace/space widths and via sizes for our board through talks with the Tektronix Printed Circuit Board Manufacturing Division. We selected Tektronix as our pc-board vendor based on a recommendation made by Cadnetix. In addition, Tektronix had already developed expertise in working with the plot and drill tapes generated by Cadnetix systems.

Tektronix provided our initial design rules at a meeting held on



After weeks of development, our pc-board plot tape was ready to ship to the fabricator. Our experiences in generating this image helped us understand what features a CAD system should have to facilitate SMT board design.

(**Ref 1**), and we used the SOIC pad patterns provided by that company. We also used recommendations from a few other sources.

AVX provided us with an application note (**Ref 2**) that contained pad patterns for passive chip components. We discussed these recommendations with John Maxwell at AVX and inspected test boards that AVX had built to test pad configurations for passive SMDs. Because of the exhaustive testing AVX performed on these

November 12, 1985. Tektronix representatives said their process could produce 2-mil lines but that a 6-mil-trace/6-mil-space rule was more routine and that boards using an 8-mil-trace/8-mil-space rule are easily fabricated. We decided to use 8-mil spacing if possible to enhance our board's manufacturability.

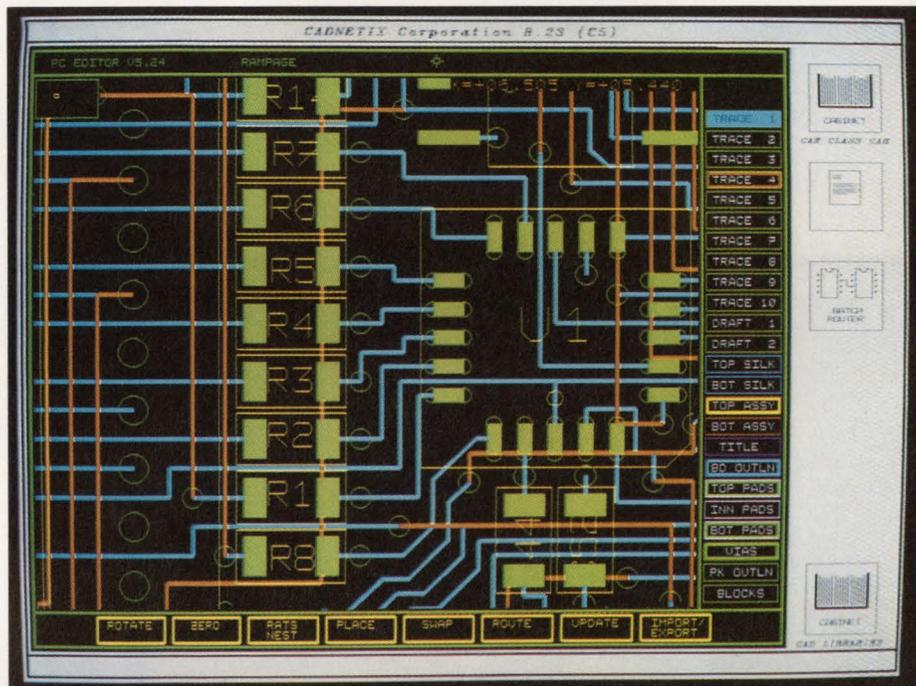
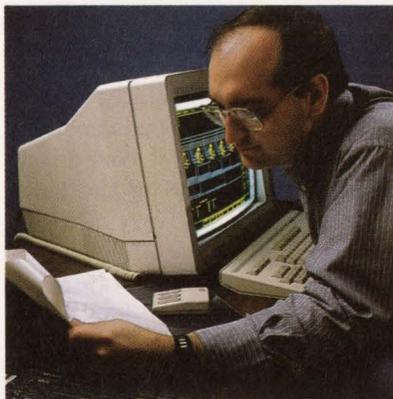
We also discussed minimum via sizes at that meeting. Vias often seem insignificant on through-hole designs because holes for the component pins provide many of the vias and because through-hole components are much larger than vias. However, complex, multilayer SMT boards need lots of vias to interconnect layers because there aren't any component pins to do the job. We settled on a design using a 40-mil pad diameter and a 28-mil hole. Although we didn't realize it at the time, the 40-mil via would become the limiting factor for our design, preventing us from designing a 4-layer board and forcing us to use six layers.

The hierarchy of CAD-based design

When you design a pc board using CAD tools, you start small and work your way up a hierarchy. You can't draw a schematic until you have built the files containing the descriptions of the components you'll use. On the Cadnetix system, component files contain electrical information about the device and designate an associated shape file. Each shape file includes a list of individual pads used to build that shape. A pad represents the lowest, atomic level of a component. The Cadnetix system stores component, shape, and pad files in separate libraries.

Although Cadnetix supplies libraries of pads, shapes, and components, we built our own files for two reasons. First, none of the Cadnetix pads or shapes matched the recommendations we planned to use. That doesn't mean the Cadnetix designs won't work. It simply means we preferred to use other patterns for reasons listed

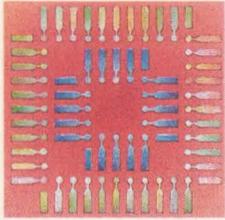
Because hand-drawn schematics allow an engineer freedom to draw any kind of symbol for a component, EDN editor Steve Leibson took extra care transferring the Rampage! schematic into the less-flexible CAD environment.



above. In addition, some of the components on our board didn't exist in the Cadnetix libraries, so even if the Cadnetix pad patterns had matched the recommendations we planned to use, we would still have built at least a few components.

As our first step, we built our pad library containing all of the pad designs we would need on our board. We initially created rectangular pads for the PLCCs because that's what all the recommendations specified. Rectangular SMT pads are extremely easy to draw on the Cadnetix system, requiring less than a minute to make. However, when we progressed to building shapes from these pads, we ran into problems when we tried generating PLCC patterns.

Manual editing of the automatically routed traces enforced the special design rules that SMT Plus provided to us. As an example, we moved all of the traces connecting to the resistors so that every trace entered the pad at the same point. The Cadnetix autorouter does not use diagonal lines, so we added them where we wanted additional clearance between traces.



At each corner of the PLCC, a vertical column of pads meets a horizontal row of similarly shaped pads (Fig 1). If the pads are rectangular, the closest corners of the pads at the end of the rows and columns come very near to each other, closing off possible routing channels. In the interest of maximizing the routability and manufacturability of the board, we decided to round the ends of the individual PLCC pads. That's when we ran into a problem.

The PLCC pads we originally built measured 70×25 mils, so we needed 25-mil diameter half-circles at each end of the pad. Although the Cadnetix pad editor allows you to use arcs and circles

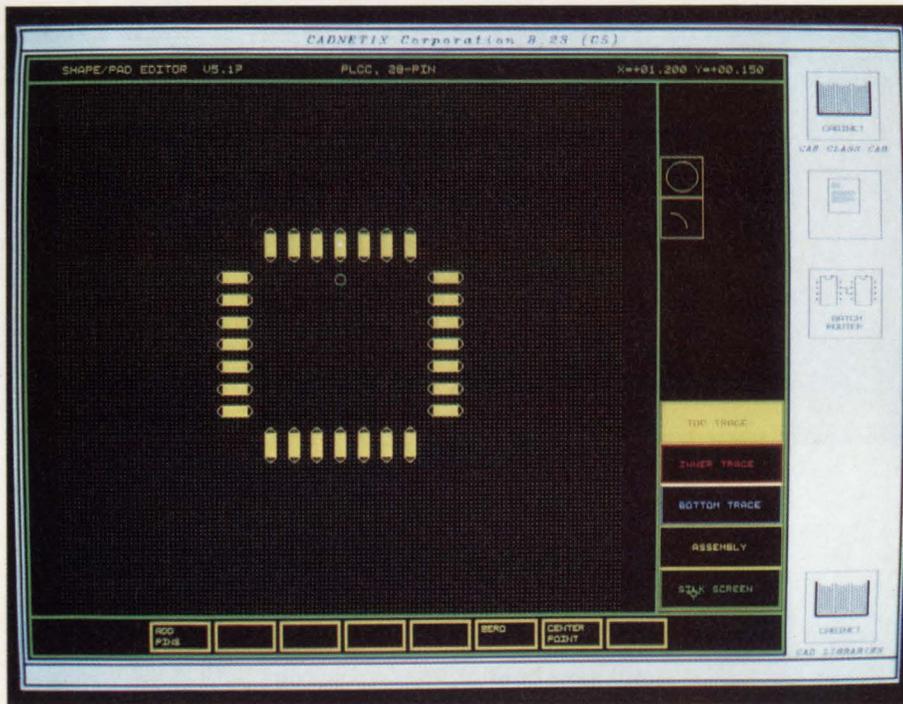


Fig 1—The four-sided PLCC pad pattern forced us to reconsider our pad design. At the intersections of the horizontal rows and vertical columns of pads, the corners of rectangular pads come too close to each other to allow us to route a trace between the corner pads.

to construct pads, it only accepts arc radii in integer mils. A 25-mil diameter pad has a 12.5 mil radius, so we couldn't build exactly the pad we wanted. We finally settled for a 70×26 mil pad (Fig 2). The 26-mil pads on 50-mil lead-pitch spacings left 24 mils between pads: exactly enough room for one 8-mil trace to run between the pads with eight mils of clearance on either side of the trace.

Another problem we encountered when building component shapes was the inability of the

Cadnetix system to treat the pc board's solder mask as a separate layer. The system assumes that the solder mask starts at the edge of the pads and covers the rest of the board. For through-hole boards, that assumption doesn't usually pose a problem. But for our SMT project board, we wanted the areas beneath our 1206 capacitors and resistors clear of solder mask.

SMT Plus recommends this approach because the solder mask can sometimes bubble, blister, or fold during pc-board fabrication. If a solder-mask imperfection occurs beneath a passive component, it can force the device off the board and create an open circuit. Passive components are especially susceptible to this manufacturing defect because passive-SMD bodies sit flush against the pc board. Active devices like transistors and ICs avoid this problem because they tend to stand up off the board on their leads. In addition, if any of the solder mask encroaches on an SMT pad, the pad becomes unsolderable, so we wanted to put around each pad a 10-mil moat that would be clear of solder mask.

After several attempts at work-around solutions to controlling the solder mask, we abandoned the effort and accepted the solder mask created by the Cadnetix system; we relied on Tektronix to give us a well-controlled solder mask, which the company did. We could have manually edited the solder-mask layer generated by the Cadnetix system after the board was finished. However, this post-processing step would be invalidated every time we went back and moved a component on the board layout. We deemed this procedure more trouble than it was worth, because we had selected a pc-board vendor and knew what the vendor could accomplish.

A similar problem occurred when we tried to find a way to prevent the Cadnetix router from

placing vias beneath passive components. For pc boards that will pass over a solder wave to solder through-hole components to the board, you'll sometimes see manufacturing defects occur when solder splashes up through a via and becomes trapped beneath a passive component. If you're lucky, the solder creates a permanent short circuit that's easy to find, but if your luck isn't too good, you'll have an intermittent short.

Passive SMDs are especially susceptible to this sort of manufacturing defect, again because the components sit flat on the board. Cleaning systems don't always remove solder and other debris from beneath these SMDs. The best solution to this problem is to exclude vias from beneath all passive SMDs.

On the Cadnetix system, our solution to this problem involved dropping small bits of trace on an unused layer underneath each passive component. The automatic router treats these bits of trace as barriers and will not place a via through one. Because we didn't plan to fabricate the layer containing these bits of trace, this technique created only one side effect: If we moved one of the passive SMDs, we had to remember to move the associated via-blocking bit of trace. Because we usually left that otherwise-unused layer undisplayed, we often forgot to move the associated bit of trace when we moved a passive SMD. This solution also points out the need for many additional layers when designing SMT boards. SMT Plus claims you need 15 CAD layers to design a 6-layer SMT board to allow for silk-screens, solder screens, land masters, pad masters, front- and back-side component locators, and computer-aided-manufacturing data.

With all the preparation required to create the component, shape, and pad libraries, schematic entry became the smallest part of this project phase. The

Cadnetix schematic editor includes one feature that certainly eased our schematic entry: buses. Our design has six buses ranging in size from five to 20 bits. We saved quite a lot of time because it's much easier to route a single 20-bit bus around a schematic than 20 individual wires. This feature was especially useful in drawing the memory array (Fig 3); we wired the address and data buses to the SIP memory modules in only a few minutes. The bus representation also makes the schematic more understandable by reducing clutter.

After entering the schematic, we were ready to place the components on the board. A good

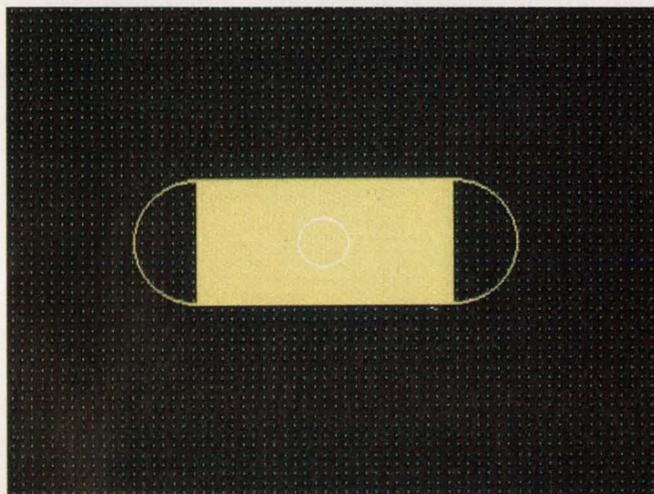
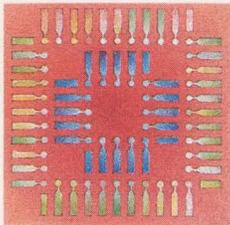


Fig 2—We solved the PLCC-pad problem (illustrated in Fig 1) by rounding the ends of the pad, but that forced us to change the pad's width from 25 to 26 mils. The Cadnetix pad editor only allowed even diameters for circles and arcs.

component placement makes a board easy to route, and a bad placement can make a board unroutable. AST's Rampage! posed a tough routing problem. Our design's six buses link components all over the board, causing trace congestion in several places. We tried several placements, and one of Cadnetix's benchmark experts, Vinnie Magnifico, tried his hand as well. We tested our trial placements by submitting each one to the route engine and stopping the routing after 10 passes. Then we selected the layout with the highest percentage of completed connections.

When we were ready to route the traces, we encountered a problem the Cadnetix automatic router has with SMT boards.



Cadnetix has a special negative-layer automatic router, which connects a selected negative layer to every pin that pierces the layer and that's supposed to connect to the selected node (that is, power or ground). That approach works great for through-hole components, but SMDs don't have any pins. To connect an inner layer to an SMD on the Cadnetix system, you must manually generate a via and route a short trace between that via and the SMD's pad on the board's outer layer. The Cadnetix automatic routers couldn't perform this task. For this reason, Cadnetix recommends that you create SMD shapes with stringers leading from the pads to vias built into the shape. However this

Fig 3—This part of our schematic shows the 256k×9-bit SIMM modules and the associated buses. Together, the memory address and data buses represent 17 signals, but on the schematic we drew only two lines. The shorthand notations for the SIMM and the buses allowed us to draw the memory-array portion of the schematic very quickly.

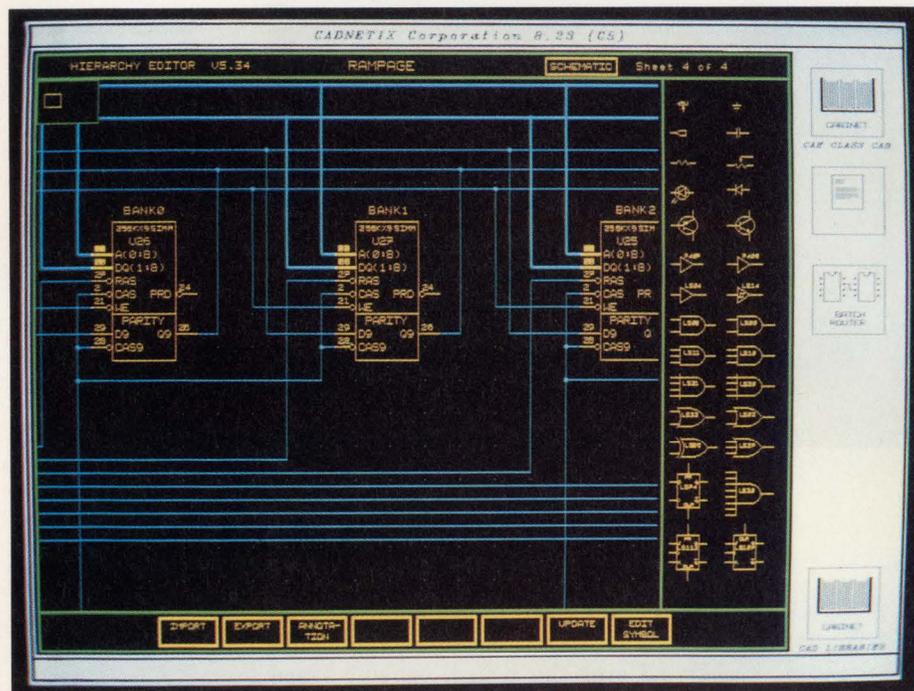
is not the case, you must manually generate a via and route a short trace between that via and the SMD's pad on the board's outer layer. The Cadnetix automatic routers couldn't perform this task. For this reason, Cadnetix recommends that you create SMD shapes with stringers leading from the pads to vias built into the shape. However this

About this time, we became concerned because the surface-mountable SIMM sockets had not arrived from Molex. We contacted the company and discovered that the other customer requesting this part was no longer interested in the SMD version. As a result, Molex had not created the tooling for this product but offered to build us enough surface-mountable sockets for our project. Instead, we switched to the company's through-hole SIMM sockets because we preferred to use a standard product.

We submitted our final layout to the route engine and let the system work on the board overnight. Initially, we instructed the route engine to complete the board using only two signal layers. The additional layers for power and ground would produce a 4-layer pc board. When we returned the next morning, the route engine had hit an impasse. It had routed traces for two hours but added no more after that time. We retrieved our file from the route engine and discovered the reason for this problem: Those 40-mil vias choked off all of the routing channels.

As an experiment, we tried routing the board with four signal layers, which would result in a 6-layer pc board. The route engine completed the entire board in less than 30 minutes. The 6-layer board didn't require nearly as many vias as the 4-layer version. Our time was running out because we were scheduled to take our plot tape to Tektronix shortly. Reluctantly, we elected to use the 6-layer board and proceeded to implement some of our SMT design rules in a manual cleanup pass.

Most automatic routers don't allow you to implement all of the



solution consumes additional real estate and limits your flexibility in dropping vias where needed.

Instead, we chose to make all power and ground connections to the SMDs manually. We dubbed this procedure "stapling," because it affixes the components to the power and ground layers and makes them hard to move. If we wanted to move a stapled component, we had to delete the short power and ground traces plus the associated vias, move the compo-

SMT design rules in the route algorithm. For example, SMT Plus recommends that each pad have only one point of entry and that the points of entry to pads for 2-lead components be balanced. Multiple traces attached to an SMD pad can drain solder from the pads during the reflow operation and in extreme cases can remove all the solder, resulting in an open joint. You plug this leak by allowing only one small trace to enter each pad. Solder draining down unbalanced traces creates a turbulence in the molten solder during the reflow operation that can drag or spin a component off its pads. We couldn't feed these rules to the route engine, so we enforced them manually after the board had been routed. Perhaps the artificial-intelligence crowd will take a crack at this problem.

We also used the manual editing pass to optimize some component placements for ease of assembly. That's when a catastrophe occurred. We were moving bypass capacitors, which turned out to be difficult because bypass capacitors were connected to all of the other components on

the board via the power and ground networks. Somewhere in tracing through these extended networks, the route editor bombed and the workstation locked up, forcing us to turn off the machine while several data files were still open.

Later, we found out that the crash occurred because someone had loaded updated software into our workstation a few days earlier. We had done our layout with a down-level version of the route editor, and the new software couldn't reliably tear up and rebuild the networks in a file created by the old route editor. The bug would only surface during use of the pin-swapping feature of the editor, but we had used that feature.

The worst effect of this crash became apparent when we tried to recover. The accident irretrievably corrupted our routed-board file, and we were forced to start over again. In the heat of doing things at the last minute, we failed to make adequate backup copies of each step and had manually edited our original copy of the routed board. Because the crash

What CAD systems really need for SMT design

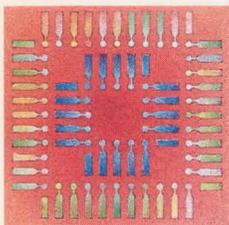
Characteristics you should look for in CAD systems for SMT designs include 1-layer pads, the ability to place components in the same location but on opposite sides of the board, placement and routing grids with 25-mil resolution or smaller, a wide variety of trace widths, and the ability to create irregular pads (not just rectangles and circles).

Without 1-layer pads, you can't route traces under the pads on other pc-board layers, which gives you more routing channels and makes your board easier to design. You must also have 1-layer pads, plus the ability to place components in the same spot but on opposite sides of the board, if you want to design SMT boards with components on both sides. Note that when you place a component on the opposite side of the board, the CAD system must provide some method of reversing the component shape, even if that method is simply to use a mirror-image shape you have previously created.

Although SMDs typically have 50-mil lead pitches, you need at least a 25-mil routing grid to

route traces between those leads. We frequently used a 5-mil grid on the Cadnetix system and could have used a 1-mil grid if it had become necessary. Another routing-grid characteristic you might need is the ability to change grids in the middle of your work. Some areas of your board can become congested with traces, and a high-resolution routing grid allows you to run more traces through the same routing channel.

You need good control over trace widths for SMT designs. Our board uses mostly 8-mil traces, but some traces that carry power are 20 mils wide. We experimentally determined that dimension by changing the trace width until we achieved a good compromise between current-carrying capability and clearances. Finally, although most of our pads are rectangular or circular, some of the pads (like those for our PLCCs) have irregular shapes. You use irregularly shaped pads to optimize some SMD shapes for good manufacturability with a minimum of real-estate use.



occurred only two days before our trip, we went to Tektronix without a tape. The moral of this story is don't upgrade your software until the current project is done, and back up your files often, on any computer system.

A reprieve for the lucky

Our second meeting with Tektronix occurred on June 26, 1986. The lack of a plot tape became an asset because it allowed us to reassess the design rules we were using. We discussed the proper clearances between the traces and the edge of the board, the number of etch targets to use for the multilayer fabrication process, the pc-board thickness tolerances, and even the proper dimensions for silk-screen lines. However, the most important topic we discussed was the via size. We explained that the 40-mil via became the decisive factor that forced us into designing a 6-layer board. Tektronix gave us the go-ahead to use 36-mil vias with 23-mil holes.

We also discussed nomenclature targets that would help the pc-board manufacturer align the silk-screen with the pads on the pc board. Such alignment is critical because silk-screen ink on an SMT pad makes the pad unsolderable. You don't need the nomen-

clature targets after the silk-screen is applied to the raw pc board, so we hid them underneath some components on our board.

Of course no one told us, until it was too late, to also include solder-screen targets. These targets aid the alignment of the solder screen with the pc board in preparation for screening the solder paste. Solder-screening machines provide three degrees of freedom for solder-screen adjustment: X, Y, and θ . Without these targets, we found aligning the solder screen to our pc board to be a bit tricky.

One more time, please

We returned to Cadnetix for another try at routing the board. Because we were using a smaller via, we again attempted to create a 4-layer pc board. Our schematic remained intact after the crash, so we proceeded with component placement using a plotted copy of our original layout as an aid. We threw this placement into the route engine and left it overnight. In the morning, the board wasn't finished but the route engine was still making headway. As a hedge against another catastrophe, we temporarily stopped the 4-layer route, ran off a quick 6-layer board, and put it safely away. Then we restarted the partially

Designing pc boards on the high end

We used an \$84,900 Cadnetix CDX 50000 CAD workstation to design the EDN SMT Project board. This system employs a 68020 μ P as its computation engine. A bit-slice graphics accelerator allows the system to pan complex schematic and pc-board images in real time. The software bundled into the CDX 50000 includes pad, shape, component, schematic, and pc-board (route) editors.

Our system communicated over an Ethernet LAN with several other CAD and CAE workstations, a \$39,900 CDX7100S file server, and a \$77,000 CDX75000S route engine. The Cadnetix route engine contains a bit-slice processor designed to automatically route traces on pc boards. Although the CDX 50000 includes an automatic router that runs on the internal 68020, the route server

accelerates pc-board routing by a factor of about 20.

In our opinion, the tools available on the Cadnetix workstation were up to the task of creating our project board. We created the necessary pads, shapes, and components; we were able to place these components on our board in a suitable layout; and we routed the board using a combination of the automatic and manual routers at hand.

Cadnetix recently released a major upgrade to its software. The company changed its workstations' operating system to Unix and converted all of its pc-board-design editors to that operating system. Also available with the upgrade are the VI editor, common to many Unix systems, and a technical publications package for documenting your designs.



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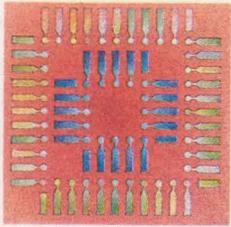
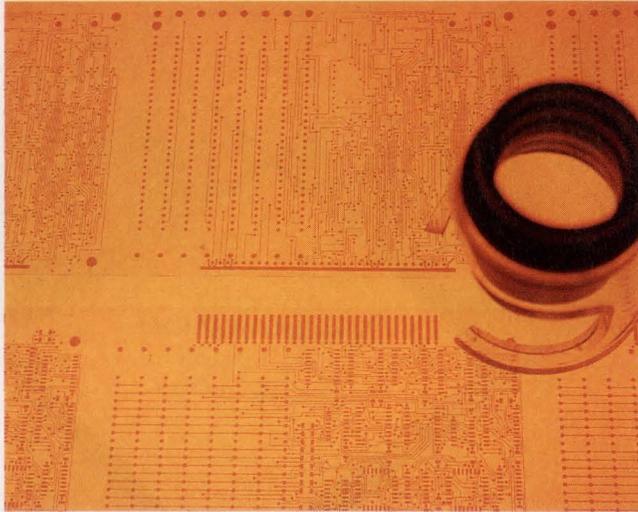


Fig 4—We caught this photplotting error just in time. The lower plot shows a normal edge connector on the board's component side, but the pads on the upper plot are rotated 90°, thus creating a shorting bar instead of an edge connector on the circuit side of the board. The error occurred when human intervention was required to transfer information from the pc-board CAD development system to the CAD system at the pc-board vendor.

complete 4-layer design and left it in the route engine for a week.

A week's worth of routing in a high-speed route engine using our 8-mil-trace/8-mil-space design rules may suggest that the engine doesn't work very well. In fact, a rule enforced by the software in the route engine was impeding our progress. At that time, the route engine required that the



routing grid meet the following restriction:

$$\text{GRID SPACING} \geq \text{TRACE WIDTH} + \text{SPACE WIDTH.}$$

In our case, because both the trace and space widths were 8 mils, we could have used a 16-mil routing grid. However SOICs and PLCCs with 50-mil lead pitches don't drop onto a 16-mil routing grid very well. We were forced to use a 25-mil routing grid to match the lead pitches of these components and still leave a channel to run one trace between leads.

Routing traces or laying track

At the end of the week, the route engine continued to chug away with 27 traces remaining to route. We decided to manually add those remaining traces. At the same time, we discovered that the software engineers at Cadnetix had developed an experimental automatic router that did not impose a routing-grid restriction, so we proposed a race. We

would manually add the missing 27 traces to our board while the experimental router attempted a 100% route using the same component placement. The first completed design would go to Tektronix. We felt something like a modern-day John Henry and beat the experimental router by one trace in a little less than a day. Since we used the Cadnetix system to design our pc board, the company has replaced its original automatic router with the experimental version, so we would have a much easier time routing our board today.

Before we sent the design to Tektronix for fabrication, we made two more manual editing passes. During the first, we applied the special SMT design rules we had learned to enhance the manufacturability of our pc board. We also used this pass to move traces around, evening out the spacing between them. We felt this step would further enhance the board's manufacturability, and besides, it looked better. Automatic routers don't seem to have much aesthetic sense for trace placement.

Adding vias for testability

During the other manual-editing pass, we added vias to make the board 100% testable on an in-circuit tester. Hewlett-Packard's Manufacturing Test Division volunteered to build the test fixture, to write the test program, and to test our assembled boards on its ATE equipment. We made sure that each circuit node contained one via that a test probe could reach. That technique ensured that our board would be completely testable from the back. Single-sided test fixtures cost less, exhibit higher reliability, and maintain signal integrity between the board and tester better than other fixture types (Ref 4).

With the design completed, our next step was to generate the plot tape for Tektronix. Although the Cadnetix system automatically

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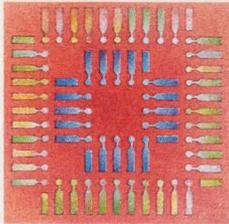
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generates plot tapes in the industry-standard Gerber-photoplotter format, you must first enter an aperture list by hand. The older Gerber photoplotters use an aperture wheel to plot images, and although many pc-board fabricators now use apertureless laser photoplotters, pc-board data is still exchanged in Gerber-format files. The fundamental problem is that the Gerber-format photoplot file doesn't contain any information about the apertures, only which aperture to use. The list describing the size and shape of each aperture used (circle, square, target, etc) is a separate document.

Human intervention invites errors

Generating an aperture list can be a very error-prone task. On the Cadnetix system, we completed a form relating various pad names from our pad library to aperture wheel numbers. The system used this list to create our plot tape. Then we wrote down a

list of the aperture wheel numbers we had used plus the shape, size, and orientation of each pad and later transcribed this sheet using an IBM PC and a word-processing program. We made two mistakes in this process that Tektronix caught before fabricating our board. We caught one more error when we received the photoplotted images for approval (Fig 4).

We found little hiccups like this problem with the aperture list somewhat disconcerting in view of all the automation brought to bear on this project. Every time we transferred information from one computer system to the next, we were reminded of the phrase "islands of automation" that General Motors uses to describe unconnected computer systems. In any event, we blessed the second photoplot, sat back, and waited for our pc boards to arrive. **EDN**

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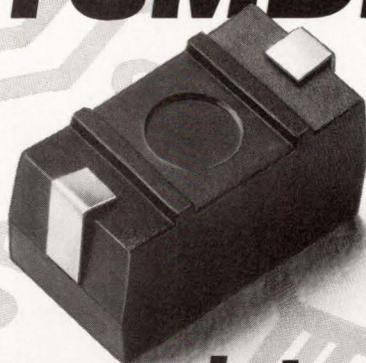
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4. *Testing Surface Mount Technology*, Part No 5954-5992, Hewlett Packard Co, Palo Alto, CA, August 8, 1986.

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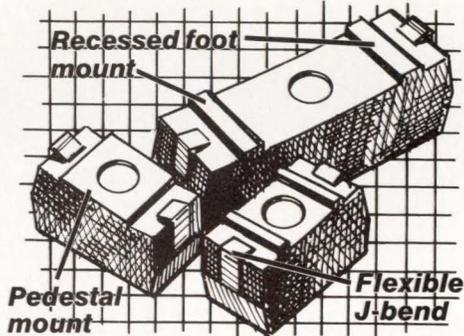
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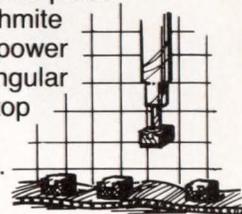
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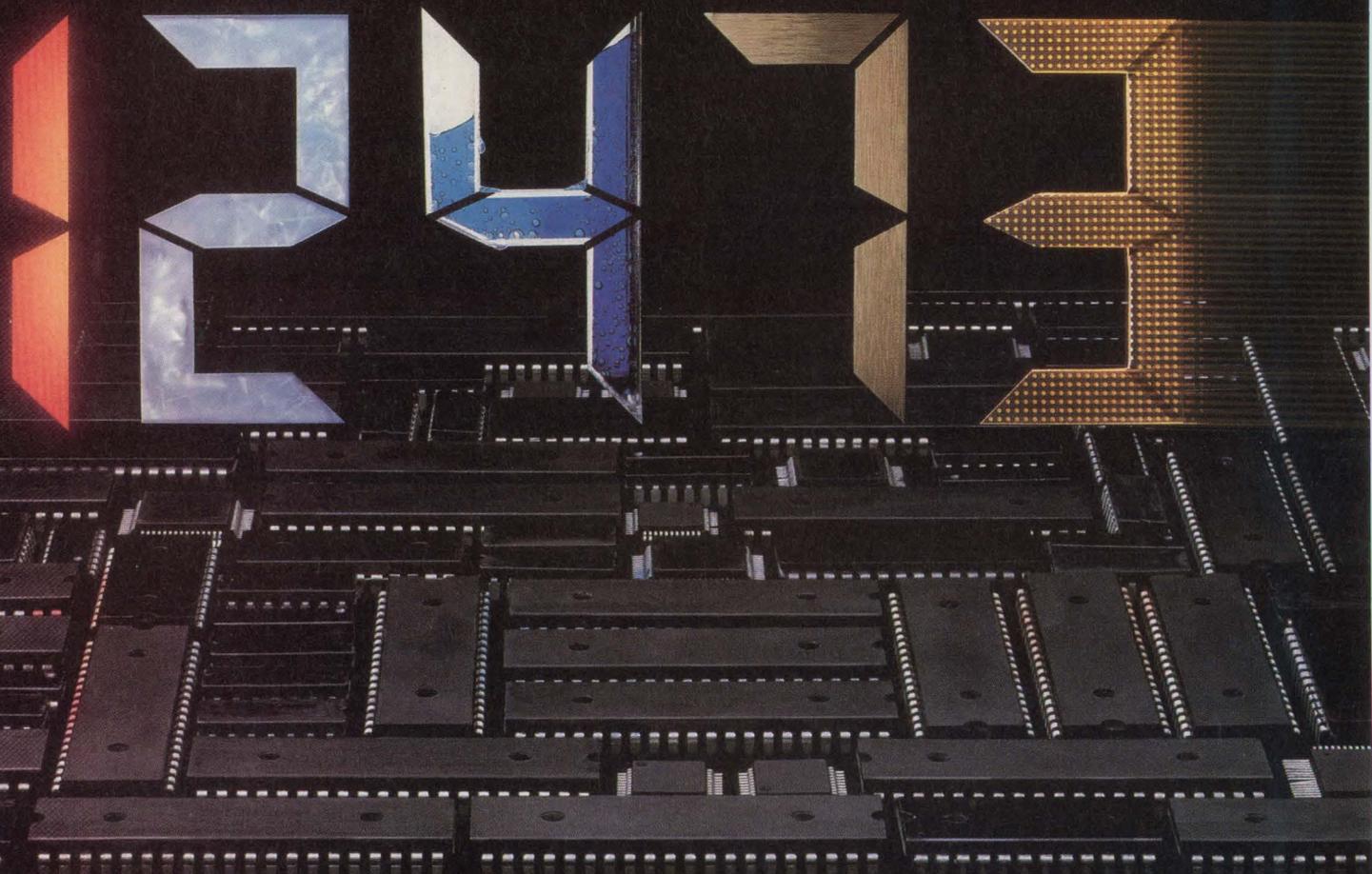
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ASIC testing mandates new role for circuit designers

No longer will you be able to check out new devices with standard benchtop tools—scopes, logic analyzers, and pulse generators. Today's ASIC devices are simply too complex to let you attack the test problem with rack-and-stack test instruments patched together from traditional GPIB lab instruments.

Alan Whiteside and Clayton Mohr, *Tektronix Inc*

New CAE tools are helping design engineers create highly complex devices that reduce entire systems or subsystems to a single application-specific integrated circuit (ASIC). These same tools are also changing the testing phases of these sophisticated designs, and thus the need for more specialized test equipment, which provides features optimized for ASICs, is becoming self-evident.

Moreover, ASICs are also redefining the designer's traditional relationship to test engineering. In many cases, due to the ASICs' complexity, only the device designer can resolve discrepancies that crop up during development of a production test program. As time proceeds, the circuit designer's involvement with production testing will certainly increase. With this fact in mind, it will help to summarize a typical ASIC test cycle.

Fig 1 shows an ASIC development process and the various testing stages. Because testing requirements vary from stage to stage, no one system is optimal for all phases. Ideally, functional and timing verification requires only a benchtop system, which should be

inexpensive enough to justify use by only a few engineers, yet still be flexible and accurate enough to verify correct functionality and timing margins at full operating speed. When a designer tests compatibility to make sure the design works correctly in the greater context of the surrounding system, a more general system-integration tool to monitor performance in the target circuit is desirable. (For a couple of specific examples of

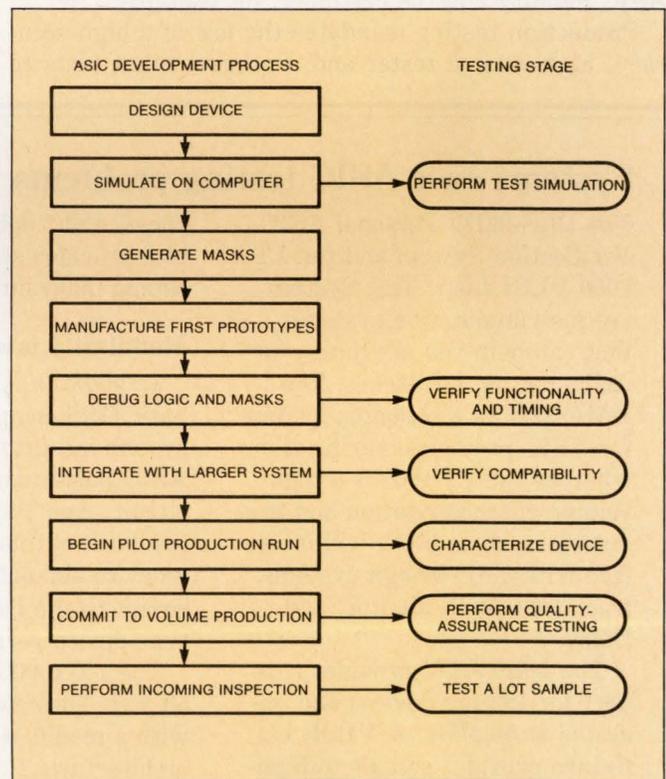


Fig 1—The numerous test stages in a typical ASIC development process range from initial simulation on the CAE workstation to production testing and incoming inspection. Test requirements vary at each stage, so you have to evaluate different ASIC test equipment and feature sets.

From a testing standpoint, ASICs challenge the capabilities of traditional test equipment and techniques.

such instrumentation, see **box**, "Systems ease ASIC testing problems.")

After you're confident that the logic design and masks are correct, a pilot production run is the next step. This representative-device sampling (50 to 100 units) determines statistical variations from device to device and stresses the devices to their limits to ascertain safe operating margins that will guarantee high yields. At this stage, an automated test program that performs the repetitive measurements and organizes the resulting data is the best investment. Unfortunately, it's difficult to justify a separate test system just for characterization, so oftentimes either the circuit designer or the manufacturing-test engineer will wind up using the prototype-verification system or the production-test system, depending on the circumstances.

Prior to full production, it is often unclear whether the designer or a test engineer is responsible for full-production test program development. In many cases, these two can represent different companies—an ASIC foundry and the customer, for example.

Production testing mandates the use of a high-accuracy, high-volume tester and a program that tests to

data-sheet specifications. Production test-system limitations and misinterpretations of the test requirements can still get the circuit designer involved—even at this stage. In the case of the ASIC user being different from the ASIC manufacturer, an incoming-inspection program is necessary to ensure reliable device quality.

The first step means first silicon

Given this quick overview of the designer's role in overall circuit development and how different stages warrant different testing tools, a detailed discussion of the actual step-by-step process will enhance your understanding. When the first prototypes arrive from the foundry, you must first verify full functional performance at reduced clock speeds. A successful functional test verifies that there are no mask or process defects in the prototypes, and confirms any preliminary tests the foundry may have performed to screen out devices with gross failures.

For realistic functional testing, the ASIC-verification system must have enough test channels to fully exercise the device under test (DUT). As is true of virtually any piece of test equipment, manufacturers have different

Systems ease ASIC testing problems

The DAS-92DV Personal ASIC Verification System and the LT-1000 VLSI Logic Test System are instrumentation systems that can help you alleviate your ASIC testing headaches. The DAS-92DV is a benchtop system for ASIC prototype verification, whereas the LT-1000 is a high-volume characterization and production system. Both will interface with CAE design systems from Tektronix, Mentor, and Daisy.

The DAS-92DV provides support for 192-pin devices and operates at 50 MHz. A VLSI test fixture provides signals to high-pin-count devices and eases device insertion and removal. Local-pattern memory, pattern editing, and compare functions

speed ASIC debugging. The unit also provides state-table and timing diagram displays.

Modularity is advantageous

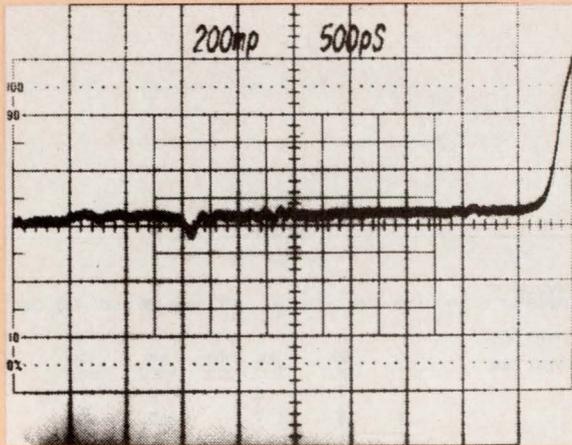
In addition, you can use the basic DAS components during system integration to verify ASIC performance in the target circuit. And you can initiate feedback of functional data from a device simulator in the target circuit to the DAS-92DV's prototype-device verification stage.

The LT-1000 is a 256-pin, 50-MHz automated test system with a modified tester-per-pin architecture. It features an interactive program that runs on the LT-PDS, a stand-alone Tektronix artificial intelligence workstation, which you can con-

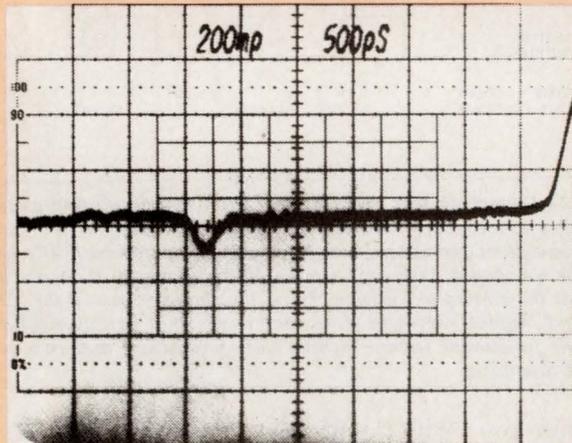
nect to the tester via Ethernet. By eliminating procedural programming, the LT-PDS lets designers or test engineers develop a complete test program (including parametric tests) in a matter of hours. You can develop tests in a stand-alone mode on the PDS and then connect the PDS to the LT-1000 to perform final device debugging.

Shmoo plots provide help

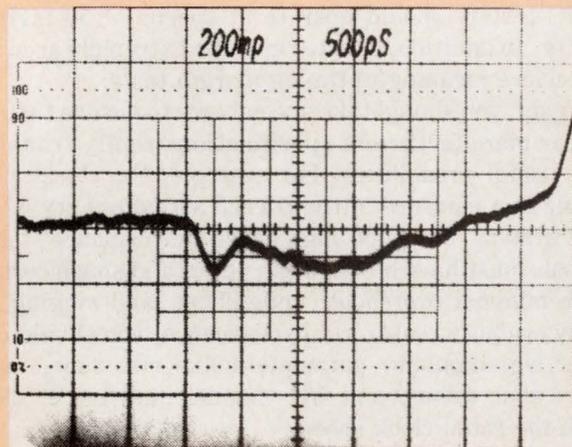
Extensive interactive debugging facilities—including fast test-pattern editing, DUT timing diagrams, and shmoo plots—let you quickly ascertain the cause of test failures. Built-in reporting facilities provide rapid statistics on prototype yields and failure mechanisms.



BEFORE FIXTURING



HIGH-QUALITY FIXTURING



CARELESS FIXTURING

Fig 3—Signal quality can limit overall test system performance. In addition to clock-cycle rates and measurement-strobe resolution, you must take into account rise time, fall time, overshoot, undershoot, and ringing.

differences in rise time and propagation delay between the channels.

You must input stimulus signal edges at the DUT pin with great accuracy, and signal acquisition must also be very accurate to provide useful information on timing margins. When you're trying to keep hundreds of test channels aligned, this task is particularly difficult.

Often, there is a temptation to use the terms edge-resolution and edge-accuracy interchangeably to describe the timing capability of a tester, but they are quite different. Edge-resolution determines the placement intervals for a stimulus edge or an acquisition strobe. Resolution alone, however, can't ensure that what the tester acquires is representative of the actual signal state. Resolution must be complemented by an appropriate degree of accuracy—the tolerance to which a signal can deviate from its programmed placement. Resolution defines the number of potential measurement points within a cycle; accuracy determines where your programmed edges will actually land, and thus affects the correctness and repeatability of your test.

Channel-to-channel skew is another parameter that affects timing accuracy (see **box**, "ASIC testers' accuracy depends on timing skew"). It is a measure of the worst-case timing error between any two channels programmed for coincident edges, and it applies to stimulus as well as acquisition strobes. Skew degrades resolution because it creates uncertainty in timing measurements.

For example, a 2-nsec skew (uncertainty) means that you cannot measure the proper response with respect to the stimulus within less than 2 nsec even though you can position the acquisition strobe at 200-psec intervals (resolution). Similarly, slow rise time on a stimulus channel can make high resolution meaningless (in terms of actual DUT measurements) if the threshold-crossing uncertainty approaches or exceeds the resolution.

What really determines a test system's true measurement capability, however, is *overall* timing accuracy. Several factors limit timing accuracy, including differences in signal-path length and delay, threshold uncertainty due to finite rise time, differences in rising- and falling-edge propagation delays, temperature-related threshold sensitivities, crosstalk between channels, a finite sampling window, and signal-amplitude dependencies. Although calibration techniques allow you to minimize some of these effects, many of them are a function of the test instrument's design and construction.

You have a choice of two basic ways of specifying the

If an ASIC user is relying on an external manufacturing source, he must develop an incoming inspection program to ensure device quality.

overall timing accuracy of an ASIC test system. One method defines the worst-case skew across all stimulus channels and the setup and hold times for the acquisition channels. As shown in Fig 4, the period of acquisition uncertainty before the strobe (in one channel or between channels) establishes the setup time; uncertainty after the strobe defines the hold time. The other method specifies timing accuracy by directly defining the allowable worst-case timing error for all combinations of input and output channels at the DUT socket. Even though you usually specify timing accuracy and skew separately, both of these affect the actual performance of a test system.

Debugging the prototype

Debugging becomes necessary when your ASIC prototype fails to meet simulation predictions. Because you don't have the luxury of probing around at various points in the circuit, you must rely on the power of the

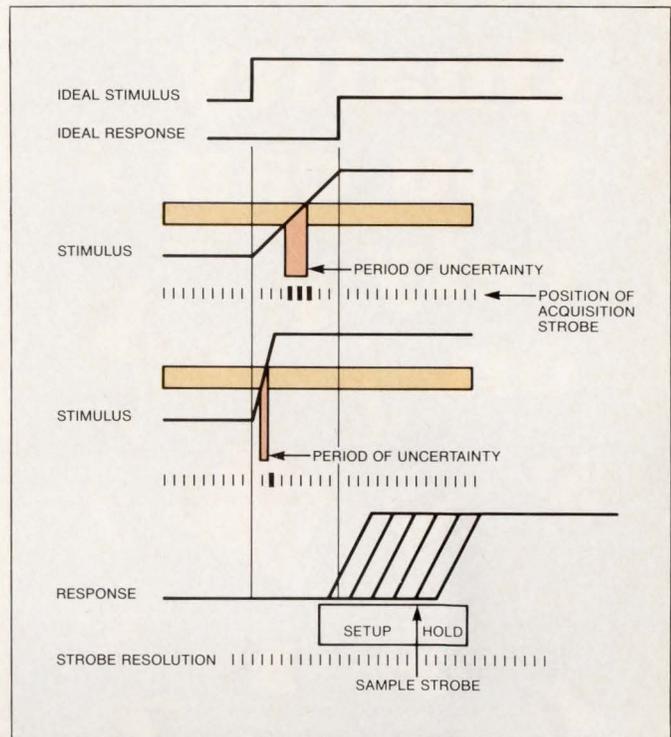


Fig 4—The overall accuracy of a tester's timing measurements depends on both its stimulus and acquisition performance. Slow driver rise times create an area of uncertainty that limits timing accuracy. System skew of both the stimulus and acquisition circuitry also places a fundamental limit on the integrity of the device measurements.

ASIC testers' accuracy depends on timing skew

When you're evaluating an ASIC test system, the timing skew between the tester channels is crucial. Overall skew is a combination of the skew between the stimulus channels and the acquisition skew of all the channels.

Output (or driver) skew is relatively easy to measure: Simply feed an identical signal to all channels and use a scope to compare each channel's output to the system reference clock. Acquisition (or comparator) skew is more difficult to determine because you can evaluate it only by looking at data in the system's acquisition memory. The following simplistic measurement technique for independently determining acquisition skew will convince you of this difficulty.

To start, apply an identical signal from a single source (other than the driver outputs) to each input channel, and make

multiple acquisition passes while incrementing the strobe at minimum-resolution intervals on all channels. Then, examine the resulting data to determine where the state change was recorded in each channel for each strobe location. You must make multiple passes because the sampling rate of a test system (20 nsec for a 50-MHz system) is usually greater than the channel-to-channel skew. A single pass would only show skew to the resolution of the system clock period.

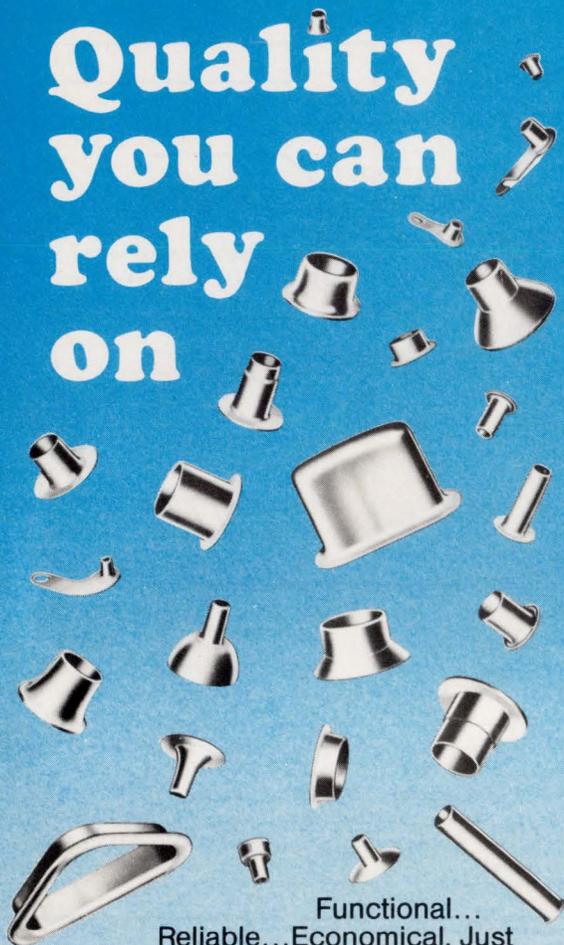
It's possible to measure input skew with one acquisition pass if you use a source frequency that's offset slightly from the test-system sampling frequency, effectively creating a moving strobe. The procedure is basically the same as above, but applying a source signal with a 19.95-nsec period while the system samples at 20-nsec intervals has

the equivalent effect of moving the strobe in 50-psec intervals.

With each sample representing a 50-psec time interval, it would take about 400 samples to record a state change of the 50-MHz input signal. You can easily determine the skew between any two channels by counting the number of samples between a state change in the respective acquisition memories.

The resolution of the source signal period and the depth of the acquisition memory (it must be at least two state changes deep, or 800 samples in this case) are the only factors that limit the resolution you can achieve with this technique. The short-term stability of the system reference clock and the stimulus signal source determine measurement accuracy.

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test system to externally gather as much information as possible to determine the problems. In a typical scenario, you observe conflicting data, hypothesize a probable cause, and then create a small set of test vectors to plant a fault in order to prove the theory.

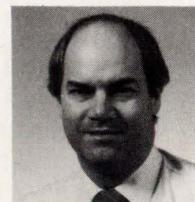
The ability to quickly and easily create and modify test vectors is critical. Two test-system features, in particular, can simplify this process. First, an efficient pattern editor allows you to quickly try many tests to prove your hypothesis. Second, the combination of local-level memory and a data-comparison capability eliminates the time-wasting delay of transmitting vectors to and from a host computer.

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Authors' biographies

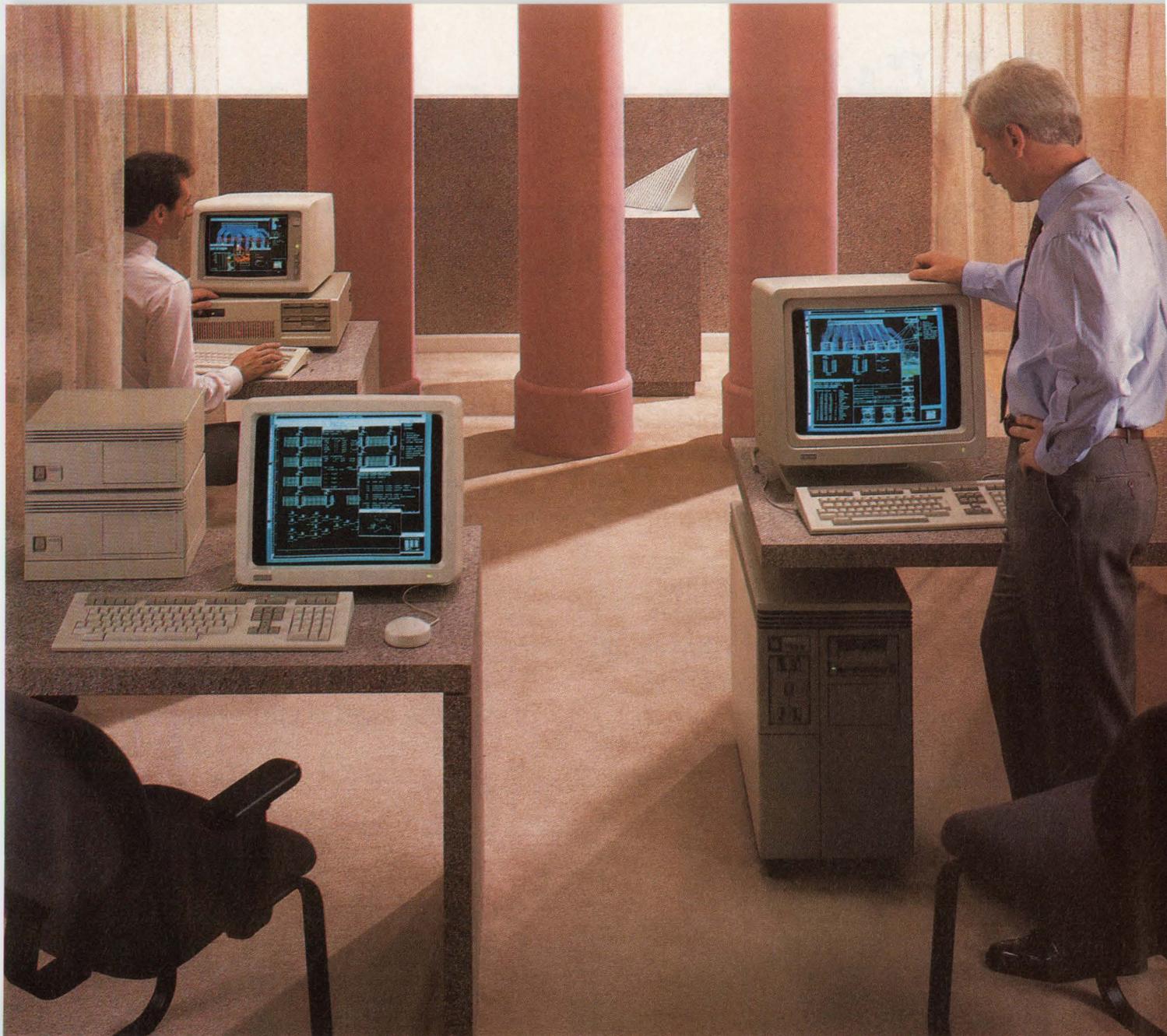
Alan Whiteside is promotions manager for the Semiconductor Test Systems Div of Tektronix Inc (Beaverton, OR). In this position, he handles marketing communications and market research. Alan has an AS degree from York College (PA) and has studied at UCLA. He likes to play the guitar in his spare time.



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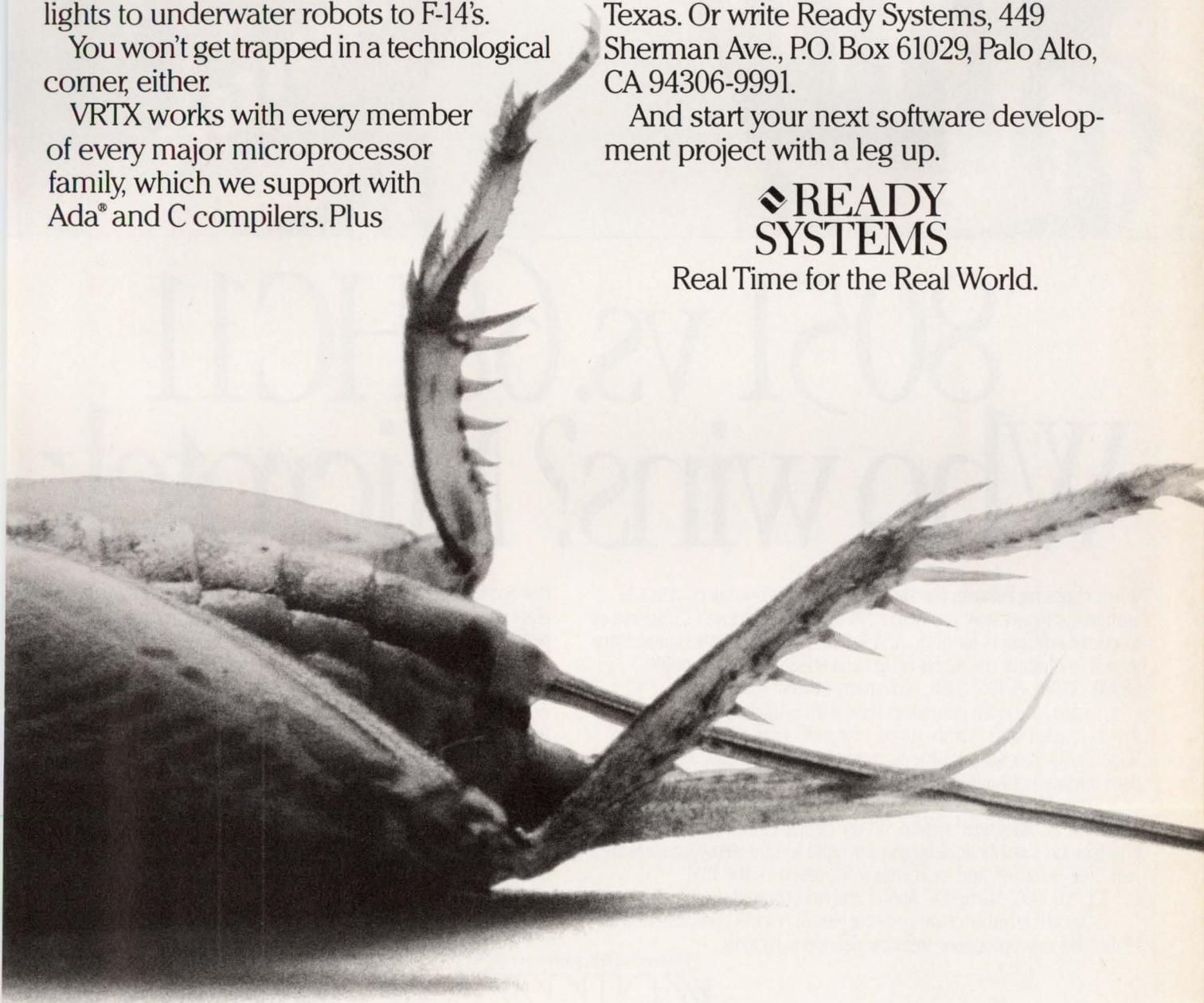
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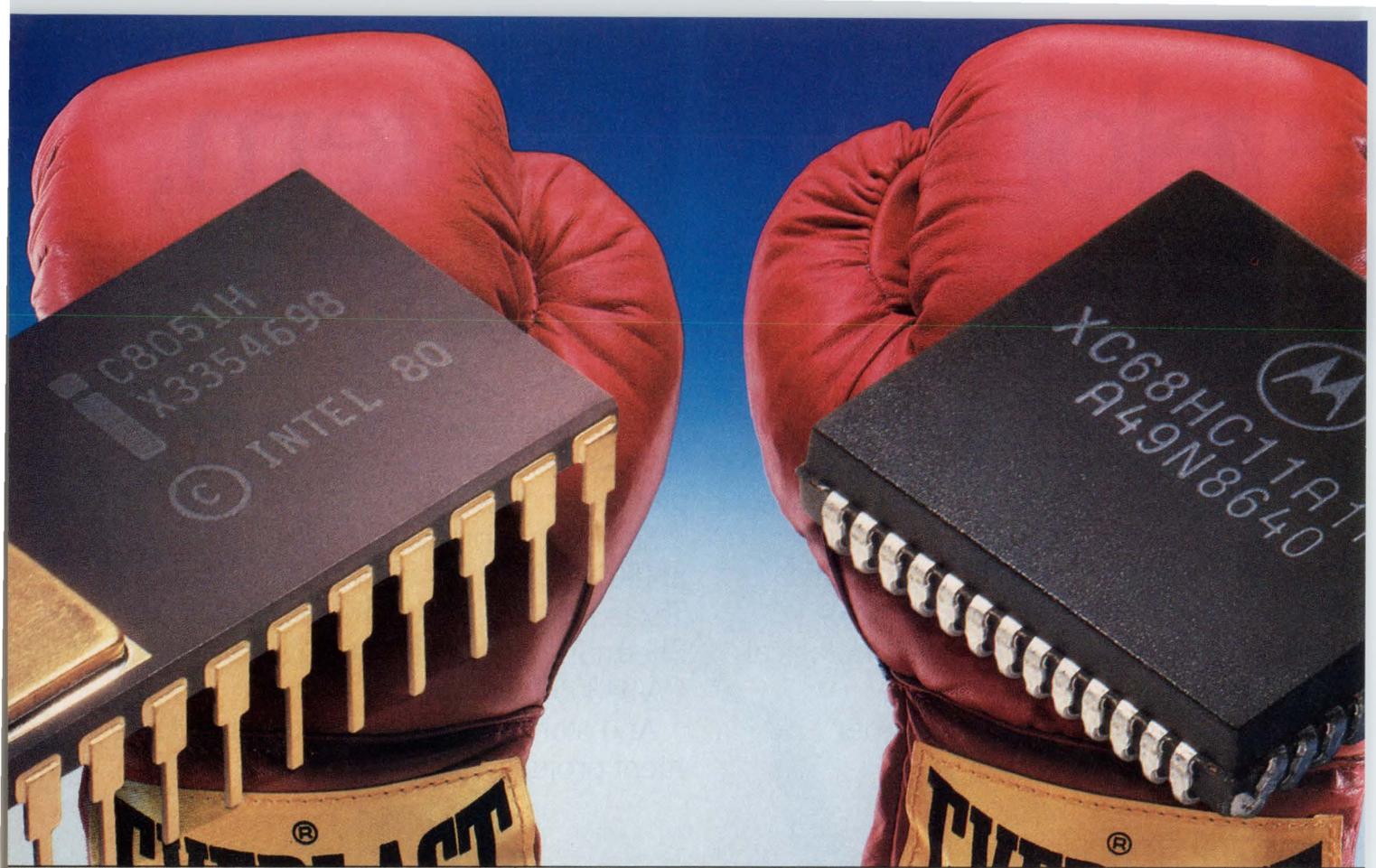
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Application dictates your choice of a multiprocessor model

The three major hardware models for modular multiprocessing systems provide different levels of both hardware and software complexity. Your choice of a hardware architecture for such a system will depend largely on the amount of effort you're willing to expend on modifying the operating system.

J Kent Peacock, *Counterpoint Computers*

It's now possible to create modular multiprocessing systems to which you can add processing capacity as easily as you add peripherals. The total processor capacity possible in such systems can be greater than that of superminicomputers and can rival that of mainframes. Your challenge, however, is to ensure that the fixed-cost framework for the largest possible processor configuration does not inflate the cost of a single-processor system.

To create a modular multiprocessing system, you can choose from a number of different architectures, including the shared-global-memory model, the processor-network model, and the shared-local-memory model. Each has certain advantages and disadvantages; your choice will to some extent be determined by how much modification of the operating system you're prepared to do.

Additional processing power can do two things for a system: It can allow the system to complete a single

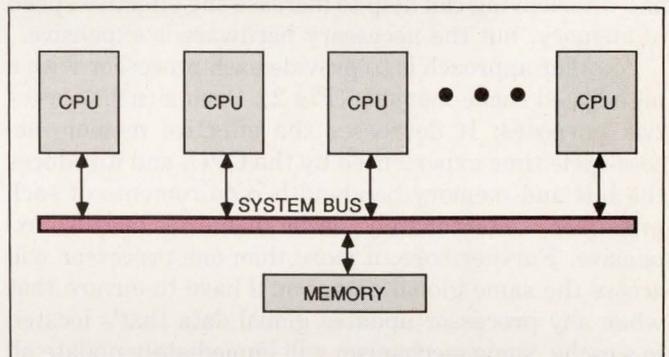


Fig 1—All processors share a single large memory and can read from or write to any location in the shared-global-memory architecture. This model requires that both the memory and the system bus have a very high bandwidth.

task faster, or it can let the system process more tasks in a given period of time. To achieve the first goal, you usually have to modify the algorithm, the language tools, or both, so that they can take advantage of the system's multiple processors. Reaching the second goal requires only that the operating system (OS) allow separate processors to handle independent tasks without interfering with one another. The OS must also distribute the task load among the processors in order to obtain a high degree of parallel operation. In both cases (but especially in the second), you'll have to ensure that the operating-system modifications that permit multiprocessing are transparent to the user.

The shared-global-memory model

The most common architecture for modular multiprocessor systems is the shared-global-memory model, in which all of the processors have access to a single main memory. A shared-global-memory system consists of a

Additional processing power can do two things for a system: It can make one task run faster or it can let the system process more tasks in a given time.

set of processors and a single large memory, to which the processors have access via a high-speed bus (Fig 1). In this model, the time required to access any memory location in the system is the same for any processor.

Further, the bandwidth of the bus/memory combination must be able to accommodate the aggregate demand for memory accesses from all of the processors; otherwise, some or all of the processors will experience delays. The solution to this requirement is complex. Obviously, you'll have to design the bus to have a very high bandwidth. However, high bus bandwidth is not enough. Memory bandwidth also influences throughput, especially if each processor retains control of the bus throughout the whole time required to perform a memory cycle. Techniques such as wide memory words and interleaving can help to increase the effective speed of memory, but the necessary hardware is expensive.

Another approach is to provide each processor with a high-speed cache memory (Fig 2). Such a cache serves two purposes: It decreases the effective memory-access-cycle time experienced by the CPU, and it reduces the bus and memory bandwidth requirements of each processor. Unfortunately, cache memories are also expensive. Furthermore, if more than one processor will access the same global data, you'll have to ensure that when any processor updates global data that's located in a cache, some mechanism will immediately update all other caches containing that data. Hardware solutions to this "cache-coherency" problem tend to be both exotic and expensive.

In spite of these complications, the shared-global-memory model has one big advantage: Balancing the load in the system is simple. When any processor finds that its current process is blocked (for example, when it must wait for input or output), that processor merely picks up from the queue the next process that's ready to run. Thus, the cost of running a process is equal for any processor in the system. For this reason, most of the currently available multiprocessor systems use the shared-global-memory model.

Processor-network model

Another approach, the processor-network model, interconnects a large number of independent processors, each with its own memory, by means of some communication network. The distinguishing feature of this model is that no processor has direct access to another processor's memory. All exchange of information among processors must take place over whatever interprocessor-communication network exists in the

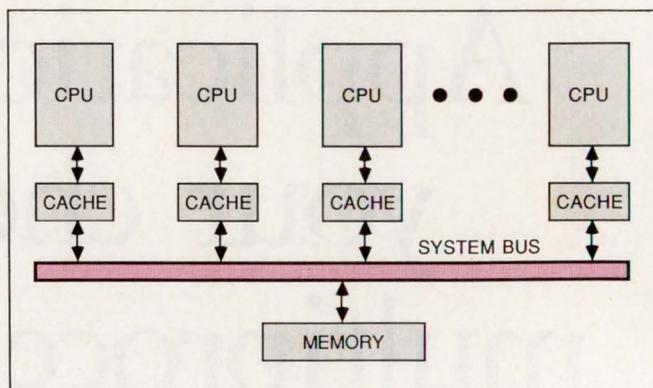


Fig 2—You can reduce bandwidth (and cost) in a multiprocessor system by providing each processor with a local high-speed cache. However, if more than one processor will access the same global data, you'll have to ensure that when any processor updates global data that's located in a cache, some mechanism will immediately update all other caches containing that data.

system (Fig 3). Thus, because it involves the exchange of messages through the communication network, global memory access takes much longer than local memory access does.

You'd select this model mainly when you want to configure large numbers of processors and have those processors run sophisticated distributed algorithms to solve very large problems. The Hypercube project originally developed at Caltech is an excellent example of a system of this type.

Shared-local-memory model

The shared-local-memory model represents a middle ground between the single-memory and the processor-network approaches. Each processor in the shared-local-memory system owns its own memory, as in the processor-network model; however, every processor can directly access all of the memory in the system, as in the shared-global-memory model (Fig 4). Thus, although there is a difference between the time required for access to local memory and the time required for access to other processors' memories, this difference is relatively small. If you've implemented the OS carefully, a given processor in the system will confine most of its memory references to its local memory, thereby reducing the bus-bandwidth requirement. In effect, the local memory provides the same facility that a local cache in the shared-global-memory model provides.

The shared-local-memory model doesn't require a number of expensive hardware items that must be present in the shared-global-memory model: an ex-

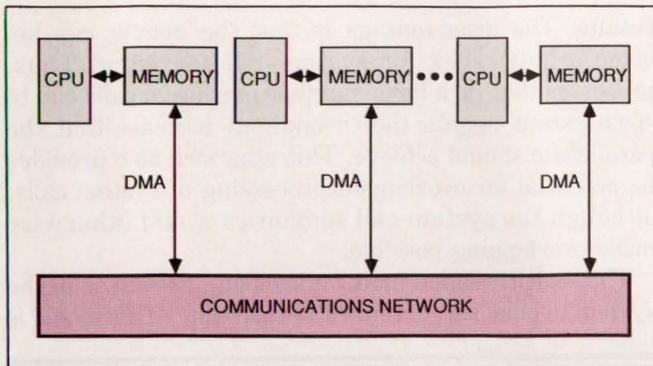


Fig 3—In the processor-network model, each processor has its own local memory, and processors communicate with each other by sending messages over a communications network. The distribution of tasks becomes a complex software problem.

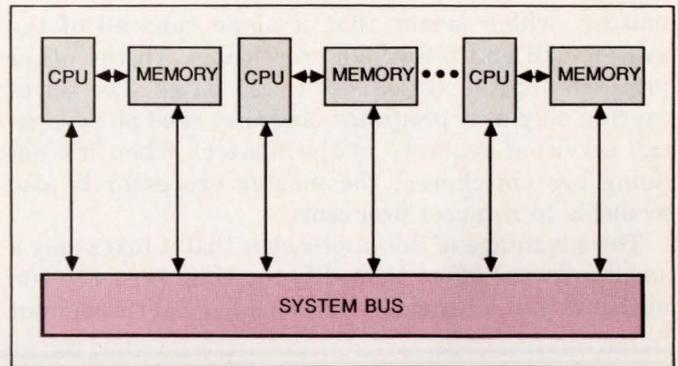


Fig 4—In the shared-local-memory model, bus- and memory-bandwidth requirements are less stringent than those of the shared-global-memory model, and moving a task from one processor to another becomes easier.

tremely high-speed bus; a high-performance memory subsystem; a high-speed cache on each processor; and circuitry to solve the cache-coherency problem. The shared-local-memory model also doesn't require as wide a bus bandwidth as the shared-global-memory model does, because in the shared-local-memory model, most memory references are satisfied locally. Similarly, the memory-access time in a shared-local-memory system can be longer because usually only one processor accesses a given memory. In a shared-global-memory system, all of the processors access the global memory. Because the shared-local-memory model doesn't create a great load on the main memory, it doesn't require a cache.

Another advantage of the shared-local-memory model is that the total amount of memory in the system is a function of the number of processors; a fully configured shared-local-memory system, such as an 8-processor Counterpoint System 19, could have as many as 40M bytes of RAM (see **box**, "A shared-local-memory multiprocessor system.") To expand a shared-global-memory system to such a large size, you'd have to include the largest memory size even in the smallest configurations.

Despite its advantages, the shared-local-memory model does have a catch, or more companies would have used this model in building multiprocessor systems. The model has, in fact, two snags. The first disadvantage is the fact that a processor takes longer to access another processor's memory than to access its own local memory. Thus, a process will run faster and take up a smaller part of the bus bandwidth when running on the local processor that owns the memory where that process resides, than when being run from a distance

by another, nonlocal, processor.

The second difficulty has to do with load balancing. In the shared-global-memory model, a process will run at the same speed and bus load on any processor, so that balancing is easy. In the shared-local-memory model, load balancing is more difficult.

Initially, you have to commit each process to one particular CPU, in whose local memory the memory image of the process will reside, and on which the process will run most of the time. When the load becomes unbalanced and you want to reassign a process to restore the balance, it's best not to try to run the process remotely from the new CPU, because that action would entail deceleration and bus-hogging. To balance the load when it becomes unbalanced, you move the process's memory image into the local memory of the newly assigned processor.

Multiprocessor software models

For each of the hardware architectures described above, there are some natural Unix multiprocessor implementations. The shared-memory models allow the easiest implementations. (Porting Unix to a processor-network architecture won't be considered here, because it involves a different set of problems. That architecture is, in any case, inappropriate for some of the semantics of System V, such as memory shared between user processes.) For shared-memory systems, you can take two basic approaches to structuring a Unix implementation: the master-slave model and the multi-threaded model.

In the master-slave model, which is embodied in a dual DEC VAX 11/780 system constructed at Purdue University, one of the processors is designated as the

In a shared-global-memory system, both the bus and the memory must be fast enough to handle the aggregate of memory accesses from all of the processors in the system.

master, which means that it alone runs all of the system-call and interrupt processing. All the other processors in the system are called slaves. The slaves execute only user programs, and they send all system-call servicing requests to the master. When it's not doing system chores, the master processor is also available to run user programs.

The advantage of this approach is that it takes only a small software effort to modify the Unix kernel to run in this way and to achieve reasonably good throughput

results. The disadvantage is that the master can become a bottleneck for system-call servicing. Thus, processes that do a large number of system calls can to some extent negate the throughput increase that the parallelism should achieve. This approach also provides no potential for overlapped processing of system calls, although the system-call semantics would otherwise make overlapping possible.

The multithreaded model allows any processor in the system to perform system-call processing. This model is

A shared-local-memory multiprocessor system

The System 19 multiprocessor family from Counterpoint uses the shared-local-memory approach. This approach yields significant cost savings in the implementation of the system, but it complicates the software design only slightly and compromises the multiprocessor throughput very little.

The System 19 multiuser computer offers multiprocessor expandability and tightly coupled graphics support. The basic board in a System 19 configuration is the main processor board, which contains a Motorola 68020 processor, a memory-management unit, an optional Motorola 68881 floating-point unit, two RS-232C serial ports, a parallel port, and an onboard Ethernet interface. A SCSI disk-controller interface board, with four additional RS-232C ports, plugs into a daughter-board connector on the main processor to provide a basic configuration that supports six ASCII terminals. The main processor bus is brought out to a connector and serves as the System Composition Bus (SCB), one of the two buses available in the system. The SCB's throughput is as high as 12M bytes/sec; it

provides the path for I/O operations and interprocessor communications in small configurations.

To add more ASCII terminals, you can connect terminal-processor boards to the SCB. Each of these boards contains a Motorola 68000 processor and 10 RS-232C ports. The 68000 offloads terminal-driver processing from the main processor.

Each application-processor board offers additional processing capability. These boards are similar to the main processor except that they have no I/O devices, and they interface to both the SCB and the second bus in the system, the Inter-Process Bus (IPB). The IPB is a high-speed, synchronous bus that increases the bandwidth available for interprocessor memory access among application processors. The IPB provides a throughput rate as high as 33M bytes/sec. In the largest configurations, the IPB would absorb all of the interprocessor traffic, leaving the SCB to operate as an I/O bus, so that the main processor takes on the characteristics of an I/O processor.

To provide tightly coupled graphics capability, you can add

one or more display-processor boards to the system. A display-processor board contains a 256k-byte frame-buffer memory and a 68020 processor that acts as a graphics accelerator. The display processor generates video signals for a 1280×1024-pixel monochrome display and accepts input from a keyboard or mouse. It interfaces to both the SCB and the IPB, so that application processors can directly manipulate portions of the frame buffer at high speed, without using the SCB.

The system can, in theory, include as many as 32 board slots, each slot providing 64M bytes of physical address space. The most significant bit of the 32-bit physical address specifies which bus a memory access will use (a 1 indicates the IPB; a 0 indicates the SCB). The next five bits of the address specify the slot number. The configurations currently available, however, are restricted to seven IPB slots and 10 SCB slots. The company can also supply bus-adaptor boards and card cages that allow you to include Multibus and VME boards in the system.

harder to implement, because it involves adding locks to the kernel in order to ensure that only one processor at a time can manipulate certain shared operating-system data. The master-slave model enforces this constraint by allowing only the master processor in the system to manipulate the data. The more processors you add to the system, the more attractive the multithreaded approach becomes, because in the master-slave model, the system-call load on the master processor (and thus the bottleneck potential) increases linearly with the number of processors. On the other hand, the more autonomous you make each processor in the handling of system calls, the greater the number of processors that you can usefully configure into the system.

Contention effects

Increasing the autonomy of each processor in the system is not just a matter of allowing system calls to run anywhere—you have to consider the far more subtle implications of contention situations. Perhaps the most important of these implications is the granularity of the locking mechanism that you must add to the kernel code. The coarsest possible lock would be a single lock that protects access to all of the kernel code and data; that is, only one processor in the system at a time would be allowed to process system calls. You'd gain very little by using such a coarse lock, because the processors would queue up, waiting for their chance to run system calls. In general, the shorter the time during which a lock is held, the greater the number of processors that can effectively access the resource protected by the lock.

Thus, the key to increasing the autonomy of each processor in a multiprocessor system is to structure the resource locks so that they are held for the smallest possible time and are accessed as infrequently as possible. How well you achieve this goal in a multiprocessor Unix system will largely determine how effectively your system utilizes the processors. Furthermore, you should apply your analysis of contention effects not only to the processors, but to all other shared hardware resources in the system, such as buses, memories, and disk storage.

A variation of the multithreaded model that is particularly suited to the shared-local-memory architecture is the "cross-processor call" (XPC) model, which Counterpoint developed for its System 19 computers. In the XPC model, the OS assigns each process in the system to a processor, which then serves as the home site on which the process's memory image resides. Each pro-

cess is also assigned a run site, the processor on which the process will execute when selected to run. When the process is running in user mode, it runs on its home processor and accesses only the local memory of that processor. During system-call processing, however, it may be necessary for the process to perform actions on another processor, such as initiating an I/O operation. Because all the system's memory is accessible from every processor, any processor in the system can become the run site. Therefore, to initiate the I/O operation, the process executes a cross-processor call; that is, the process changes its run site to the processor that's attached to the I/O device and then executes the I/O driver code on that processor.

To avoid excessive bus loading when a process is not running on its home site, the OS designer arranges system code so that all processors can fetch it locally. Because code accesses tend to account for more than half the processor cycles, this scheme reduces the bus requirement by that amount. The run-site processor need only fetch global and stack data across the bus. Because much of the state of the computation is maintained in processor registers, these accesses don't use a high percentage of bus bandwidth, either. Actual observation and measurement confirm that running across the bus in this manner causes little degradation in execution speed.

The XPC software approach and the software approach for the shared-global-memory model are somewhat different. In the XPC approach, the home site and run site of each process are explicitly associated with specific processors. The shared-global-memory model, however, implicitly allows a process to run on any processor in the system unless the process performs a system call, in which case it must run on the master processor. Thus, the run site of a process is set according to the whim of the OS scheduler, and the processors have no home sites, because all the processes reside in the single, global memory.

Although moving a process from one CPU to another incurs no apparent increase in overhead, you must nevertheless consider the effect of having to reload the cached context of the process into a cache on another CPU when the process is reassigned. This effect can be important when you use large caches to provide a high hit rate, because you would expect the process context to remain cached despite context switches.

When you consider the structure of the OS kernel, remember that the XPC model allows you to apply both the master-slave and the multithreaded approaches, on

In a processor-network system, interprocessor memory accesses take much longer than do local memory accesses.

a function-by-function basis. The first version of the System 19, for example, was a strict master-slave model, which used the memory on the main processor as a shared-global-memory. By adding OS memory-management code for the application-processor boards, the manufacturer was able to convert the original system to a shared-local-memory system. Since then, the company has added sets of locks to allow for the autonomous operation of various subsystems within the kernel. Each addition of such locks has substantially increased the aggregate multiprocessor throughput of the affected subsystem.

Load-balancing considerations

Load balancing of processes in a shared-local-memory architecture presents some interesting challenges. The System 19 implements a form of load balancing that assigns a process its home site during the execution of the *exec* system call that creates that process. The load-balancing mechanism bases its site selection on the current load average, the amount of free memory, and the paging rate of every processor in the system.

Under Unix, an application program creates a new process by means of two system calls, *fork* and *exec*. The *fork* system call first creates a clone of the process that's making the call. This clone (called the child process) and the original (called the parent) have identical code and data, and identical stack contents. Upon completion, *fork* returns a zero value to the child context and returns the nonzero process ID of the child to the parent context. At this point, the code normally checks the return value and takes one branch for the child and another for the parent.

The child branch usually does some housekeeping chores and then calls *exec* with a set of arguments and the name of a program that will replace the one that was running at the time of the *fork* call. The *exec* system call throws away the old program, and in doing so, it strips the process to a minimal context. At this point, the load-balancing mechanism assigns this minimal child context to a home site and moves it there. At the new site, the *exec* call completes its job by loading the new program into local memory.

A user-settable bit mask is associated with each process; each bit in the mask represents one processor that the load-balancing mechanism will consider as a possible home site for that process. A user program can force the process to a particular processor by setting only the mask bit representing that processor and clearing all other bits in the mask.

Of all the processors specified by the bit mask, the preferred choice for the new home site is the processor that has both the lowest average number of runnable processes, and enough free memory to hold the process in question. If no processor has enough memory, the load balancer assigns the process to the processor that has the most free memory. You may also be able to save space on the target processor if it already contains some of the code necessary for the process being transferred, because different processes on a single processor can share code segments that are common to them all. Thus, for every segment of the new program's code that is already being run by another process, you can reduce the size estimate for the new program accordingly.

In the System 19, the load-balancing strategy does not currently move a process once it has been assigned to a home site. In general, this strategy works well because most processes in Unix are very short-lived. Hence, a bad site selection usually does not affect processor utilization for very long.

On the other hand, processes are created very frequently, so that the accuracy of the average runnable-process count on each processor is important. Originally, the algorithm computed this average by sampling the count once per second over a 4-sec interval. This method isn't responsive enough, so you can increase the sampling rate to 64 samples/sec and take the average of each group of 64 samples during each clock interrupt. This change substantially improves the balancing of the process load. However, it's still possible for multiple processes to be created in quick succession; in such cases, the OS may assign all the processes to the same processor because the average is not being updated fast enough. The solution to this problem is to bias the average value temporarily upward each time a process is moved to a processor.

Although the System 19's load-balancing approach works well for a typical Unix workload, you may need to reassign some processes after *exec* makes its initial selection of their home sites. Some workloads are not typical; for example, the creation of one monolithic process per user could easily create unbalanced conditions as users log on and log off. To rebalance the workload, you could move existing processes around.

Another type of problem arises when a processor's local memory becomes overcommitted. Processes will then keep swapping between that processor and the disk, even though the total memory in the system is adequate to hold all of the processes. The best solution to this migration problem is probably to make the



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The more autonomous you make each processor in handling system calls, the greater the performance improvement per processor.

existing swapping algorithms more general. Then, when the system detects that a local memory is over-committed, a process need not be swapped out to disk, but can be moved to a processor that has enough memory to hold it. Similarly, when the averages of runnable processes become too uneven, the system can move processes from processors with heavy loads to those with lighter loads. Counterpoint plans to implement these solutions in the System 19 at some future time.

Performance measurements

Letting the processors in a multiprocessor system run autonomously improves the system's performance, as the benchmark and test results obtained by Counterpoint indicate. When the company used the well-known Dhrystone CPU benchmark to perform basic user-mode CPU tests on a System 19 with as many as eight processors, it measured a "speed-up efficiency" (the speed increase per processor) of more than 95%. For each test with n processors, n copies of the benchmark were run in parallel, one copy per processor. The Dhrystone ratings for each copy were then added together and divided by the rating for a single copy. For eight processors, the ratio was 7.8. This result is not surprising, considering that the benchmark performs only a few system calls, and hence each copy runs almost completely in its local processor.

Because of its importance in structuring parallel, multiprocess applications, one of the first kernel subsystems that the company converted to a multithreaded model was the System V message and semaphore facility. Because the System 19 shares System V among the processors, it's possible to write tightly coupled parallel applications that use semaphores for synchronization. Alternatively, you can write loosely coupled applications, using messages. A simple 2-process message benchmark was run twice, first with both processes on a single processor and then with a process on each of two processors. The single-processor throughput from the benchmark was 15,000 messages per minute, whereas the 2-processor throughput was 25,000 messages per minute. A similar benchmark, using semaphores, yielded 7500 semaphore operations per minute with one processor and 14,500 operations per minute with two.

The latest changes in the System 19 have modified the file system and particularly the method of accessing data blocks that are resident in the kernel's disk block cache. Any processor can now satisfy a disk request,

provided that the requested block is in the cache. If the desired block is not in the cache, the OS must make a cross-processor call to the main processor, which then queues a request to the disk controller to retrieve the block.

To measure the effect of these changes, the company instituted a test that forced some small files to be held completely in the block cache; the test then accessed the files from one, two, and three processors. The aggregate throughput rates were 891k, 1478k, and 2024k bytes/sec, respectively. In other words, two processors yielded a speed-up ratio of 1.66, and three processors yielded a speed-up ratio of 2.24.

The final test required the system to follow eight parallel scripts that compiled and linked the files of a small utility. This procedure represents a typical load in a program-development environment, with a typical mixture of I/O operations, processing, and creation of subprocesses. The system completed the set of compilations 2.3 times faster when using three processors than when using one. This result gives some indication of how well the *exec*-time load balancing works in distributing a number of processes. **EDN**

Author's biography

J Kent Peacock is a project manager at Counterpoint Computers (San Jose, CA), where he is responsible for designing and implementing improvements to the company's multiprocessor Unix kernel. He has been with the company for more than two years. Kent holds a BSc in electrical engineering from the University of Manitoba, Canada, and a master's degree in mathematics and a doctorate in computer science from the University of Waterloo, Canada. In his spare time, Kent enjoys golf and racquetball, flying, and playing the flute.



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Variable-pulse modulator improves power-supply regulation

A pulse regulator combines aspects of both pulse-interval modulation and pulse-width modulation to improve the regulation and the efficiency for switch-mode power supplies. The circuit is particularly useful in applications requiring line isolation.

Wayne M Austin, GE/RCA Solid State

Pulse-width modulation (PWM) has long displaced pulse-interval modulation (PIM), which was so prevalent during the early development of switch-mode power supplies. Each method of control has its advantages and disadvantages. PWM offers effective control over a wide range of power supply loads, but at the lower end of the load range, the minimum pulse width required imposes its own limitation. In addition, you must slow down the rise and fall times of the drive pulse to the power switching transistor to meet RFI and EMI requirements.

PIM can better handle low loads because the duty cycle is reduced by increasing the pulse interval, rather than by reducing the pulse width. The PIM's lower operating frequency at low loads may cause filtering-related problems in audio or instrumentation applications. Another potential problem at the low-frequency

end is an increase in transformer conversion losses. The CA1523 variable-interval pulse regulator, however, combines the advantages of both pulse-frequency and pulse-width modulation without the disadvantages encountered using just one of them.

Fig 1 shows the block diagram and external circuit used in a typical switching regulator circuit. Special features of the CA1523 include a slow-start controlled power-up, mode-sensitive logic control of the output pulse, and overcurrent sensing. The IC provides for adjustment of the pulse-width- and frequency-modulation range, making it adaptable to a variety of switching power-supply systems—especially those where line isolation is required.

When you need line-isolated power-supply voltages, you can use the CA1523 regulator in a transformer flyback-converter system like the one shown in Fig 2a. This system is particularly useful when you must meet the rigid safety standards required for workstations interfacing or for modular consumer audio and video equipment. Less stringent requirements may permit the use of regulators with a common ground for both the switching-controller and the power-supply outputs. Examples of these common-ground regulator applications are the flyback converter of Fig 2b and the buck converter of Fig 2c. Because many applications require line isolation, however, the transformer flyback-converter system is the one of most interest.

The CA1523 is primarily a PIM controller with built-in PWM correction over a 2-to-1 pulse-width

The CA1523 is a PIM controller with built-in PWM correction over a 2:1 pulse width range.

range. For a frequency (f) and an associated period (T), the pulse width reduces from a maximum width of $T/2$ (50% duty cycle), corresponding to the highest frequency at the maximum load limit, and approaches $T/4$ at the lowest frequency and minimum load. The combination of PIM and PWM control effectively compresses the operating frequency range compared with that of pure PIM control for a given load range. The advantages at minimum frequency include reduced losses and low ripple, combined with improved efficiency and regulation.

Pulse-width correction, when done simultaneously with pulse-interval correction, produces an inherent improvement in conversion gain of approximately $2\times$ at 50% duty cycle under heavy load conditions. This

feature allows the error-amplifier gain to be kept low, thus improving stability without the addition of external components.

Circuit organization and description

The CA1523 has five primary circuit functions: error amplification, pulse-width and -interval (or -frequency) modulation, pulse driver and output amplification, slow-start power-up control, and system logic control. The block diagram of **Fig 1** shows the interrelated functions of the circuit. When the system raw B+ is switched on, the slow-start function controls the pulse-width and -frequency modulator (P/FM) until the voltage at pin 10 is greater than 7V. Standby conditions then exist until switch S_1 is closed. In the standby

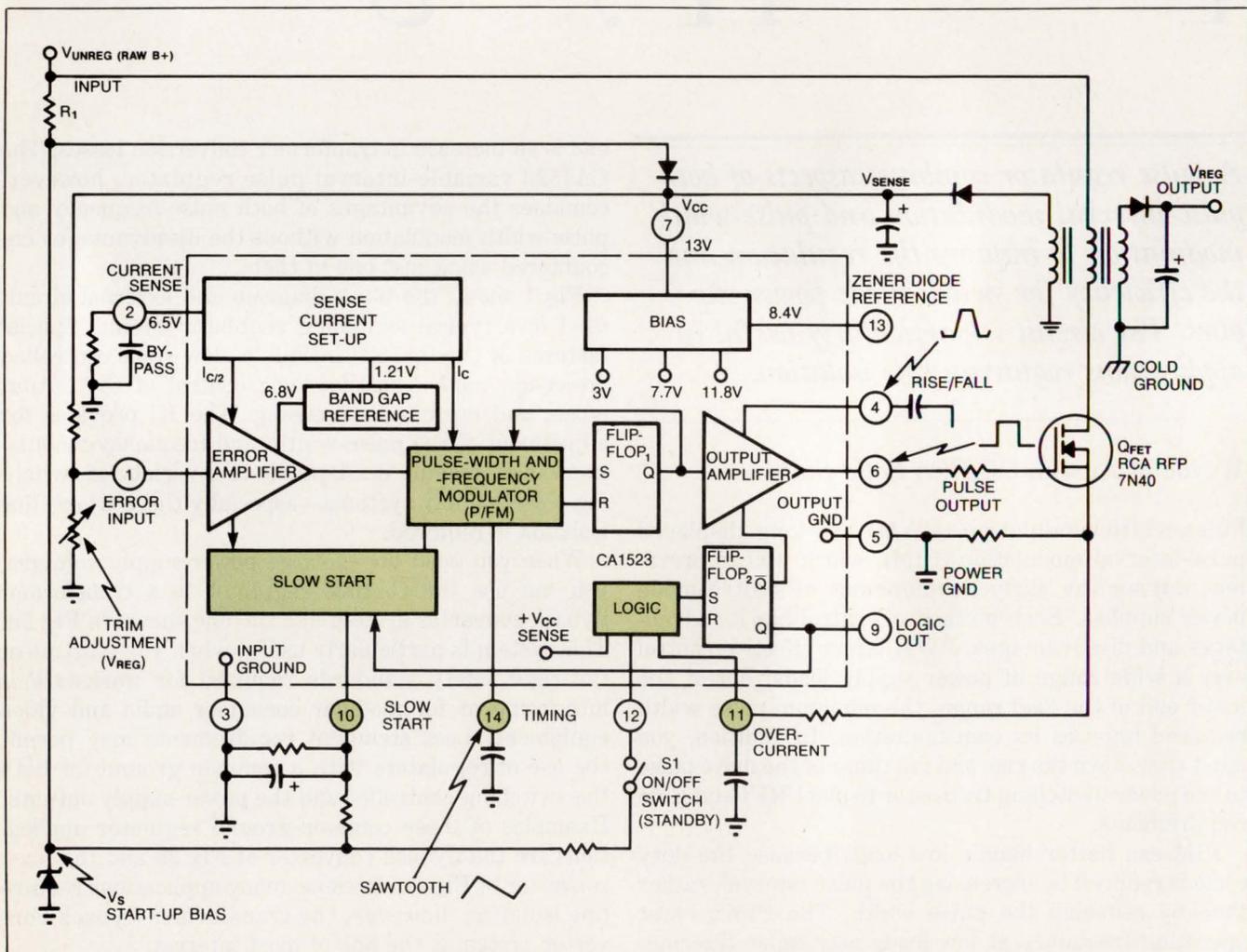


Fig 1—A typical switching-regulator power supply uses this functional block diagram and external circuitry. Features of the CA1523 control IC include a slow-start controlled power-up, logic control of the output pulse, and overcurrent sensing.

mode, the P/FM maintains a maximum frequency output with a 50% duty cycle. After switch S_1 is turned on, the output amplifier is enabled and the P/FM responds to the error voltage at pin 1. The error amplifier accepts error-correction inputs and controls the pulse-width and -frequency modulation. The P/FM output pulse is then amplified in the driver and output stage.

Fig 3 shows the timing and P/FM circuits of the CA1523. For a given timing capacitance, C_T , the current-sense bias at pin 2 determines the maximum frequency of the P/FM circuit. The fixed resistor R_S , which is connected to ground, sets the current-sense level, I_S . A resistor-divider reference at the base of Q_{92} is approximately $V_{CC}/2$. The differential amplifier (Q_{91} , Q_{92}) feeds back, via Q_{17C} , any error in amplifier balance, thus holding the pin 2 voltage at the $V_{CC}/2$ reference level. The differential amplifier's emitter current is supplied by Q_{93} and is determined by the bandgap bias voltage of 1.21V at the base of Q_{93} .

The emitter current of the differential amplifier is approximately equal to the collector current of Q_{17C} , with Q_{17A} and Q_{17B} acting as current mirrors. The currents $I_C/2$ and I_C control the P/FM charge and discharge timing, and are equal to the collector currents of Q_{17A} and Q_{17B} , respectively. The current ratio is 1/2:1 to accommodate a 50% duty cycle at maximum frequency and load conditions. When start-up conditions exist, pin 1's error voltage is low and Q_6 passes all of the $I_C/2$ current to Q_{11} . Because Q_{11} and Q_{18} are current mirrors, Q_{18} 's collector discharges the timing capacitor, C_T , at pin 14. The state of the flip-flop FF_1 determines whether Q_{15} will conduct current I_C from Q_{17B} into the timing capacitor.

When Q_{18} is discharging current from C_T at an $I_C/2$ rate, and Q_{15} is charging C_T at an I_C rate, the net charged current is $I_C/2$. This condition causes a flip-flop high state for the Q output, and Q_{16} is cut off while Q_{15} is conducting current I_C . The positive-voltage ramp at pin 14 increases until the V_H comparator toggles at the 5V reference to the inverting input, resetting the flip-flop, which then makes the Q output go low. The low Q output cuts off the Q_{15} , and no charge current passes to C_T . The timing capacitor is then discharged by Q_{18} at a maximum rate of $I_C/2$. The discharge ramp continues until the voltage at pin 14 reaches 2.5V, at which point the V_L comparator toggles the flip-flop's S input to a high state. When the Q output goes high in response to the high at the S input, the cycle of charge and discharge to timing capacitor C_T is complete.

This entire operation occurs when the error voltage

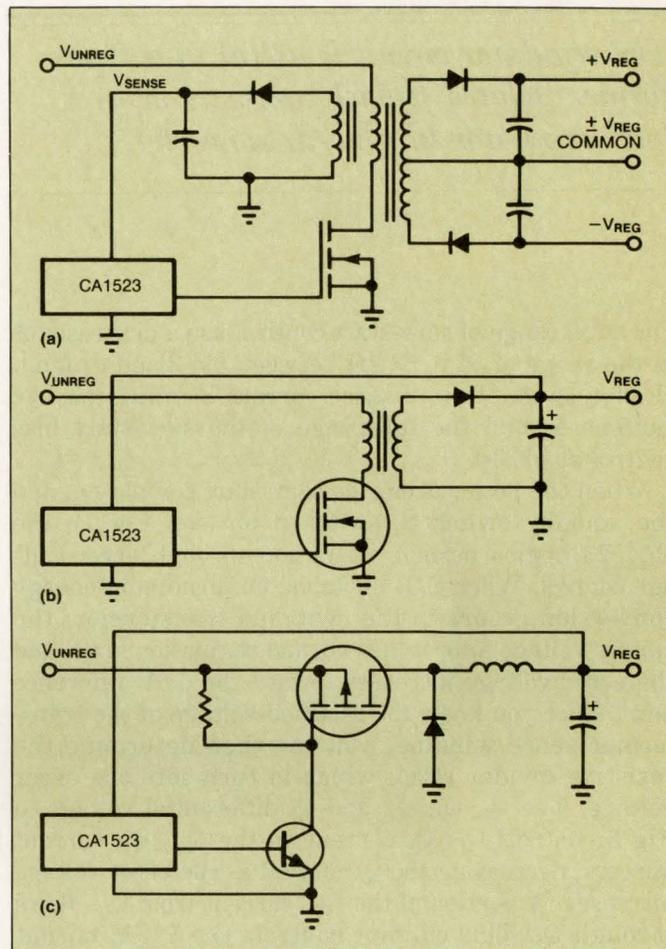


Fig 2—The CA1523 can be useful in various switching power-supply systems: a line-isolated flyback converter (a), a nonisolated flyback converter (b), and a buck converter regulator (c).

is lower than the 6.8V differential input reference, a condition that allows the full $I_C/2$ discharge of C_T by the Q_{11} and Q_{18} current mirrors. Once the slow-state function is on, it shunts the Q_6 collector current through Q_2 . As a result, the Q_{11} , Q_{18} current mirrors initially receive little or no forward bias current, and C_T cannot be discharged. As the slow-start voltage increases, the current in Q_2 decreases, allowing Q_{11} and Q_{18} to discharge C_T at an increasing rate. As long as the error voltage at pin 1 remains below the 6.8V reference level, the charge and discharge rate is at 50% of duty cycle.

In the slow-start circuit of Fig 3, an increase of the slow-start bias on capacitor C_2 at start-up exercises a decreasing degree of control over the discharge timing. If the current-sense adjustment at pin 2 is typically less than 100 μ A, a full frequency range of slow-start control will be available, and the range of increasing pulse width will be two to one. Higher pin 2 bias currents will reduce the range of frequency control. The input to pin 10 drives the base of pnp transistor Q_{34} , whose emitter is returned to an internal 7.7V bias source through a 30-k Ω resistor. Transistors Q_1 and Q_2 mirror the Q_{34} collector current and shunt the Q_6 collector current away from Q_{11} , reducing the discharge current in the timing-control circuit. This arrangement controls the discharge current over a range of 100 μ A.

The regulator circuit is useful in a transformer-isolated flyback converter or as a buck regulator in a dc/dc converter.

For a full range of slow-start control, use a bias resistor in the range of 56 to 68 k Ω between pin 2 and ground. Higher levels of pin 2 sense current increase the $I_C/2$ current beyond the full range of the slow-start bias control at pin 10.

When the power is on, the slow-start completed, and the standby switch S_1 switched on (see Fig 1), the CA1523 begins normal regulation through error-voltage control. When S_1 is switched on, maximum energy conversion occurs in the switched transformer, the supply voltage approaches normal regulation level, and the error voltage increases toward the 6.8V reference level. Once you know the rectified voltage of the transformer sense winding, you can then determine the resistive-divider ratio, which in turn sets the error voltage. The Q_5 , Q_6 , Q_7 , and Q_8 differential voltage in Fig 3 controls the Q_6 current to the Q_{11} , Q_{18} current mirrors, decreasing the Q_6 current as the error voltage increases. A portion of the $I_C/2$ current from Q_{17A} flows through Q_6 . This current controls the P/FM output pulse and maintains the regulation at the level that the adjustment of the divider at pin 1 has determined.

The pulse output continues from flip-flop 1 during

regulation but at a reduced rate and with a reduced pulse width. The Q output of the flip-flop is always high when the ramp at pin 14 is positive. At minimum load, the pin 1 voltage increases, and the net charge current for the positive ramp is higher because Q_{18} is discharging less current. For example, if the error voltage at pin 1 is forcing half of the $I_C/2$ current to Q_7 , the Q_6 current is equal to $I_C/4$, and the positive-ramp charge current at pin 14 is $I_C - I_C/4 = 3I_C/4$. The net negative-ramp charge current is then equal to $I_C/4$. What had been a maximum charge and discharge rate of $I_C/2$ at start-up is now pulse-interval and pulse-width modulated to provide a 3 to 1 charge/discharge ratio.

When the CA1523 can operate with no external system restrictions, and functions as a pulse generator, you can use very large capacitance values at pin 14 to achieve very low pulse frequencies. External resistor loading at pin 14 will contribute a nonlinear slope to the otherwise linear sawtooth. You will also note a nonlinear contribution in the waveform at pin 14 if the timing capacitor has less than 10-M Ω leakage resistance. In addition, very low values of I_S are not recommended because the base-bias and junction-leakage currents

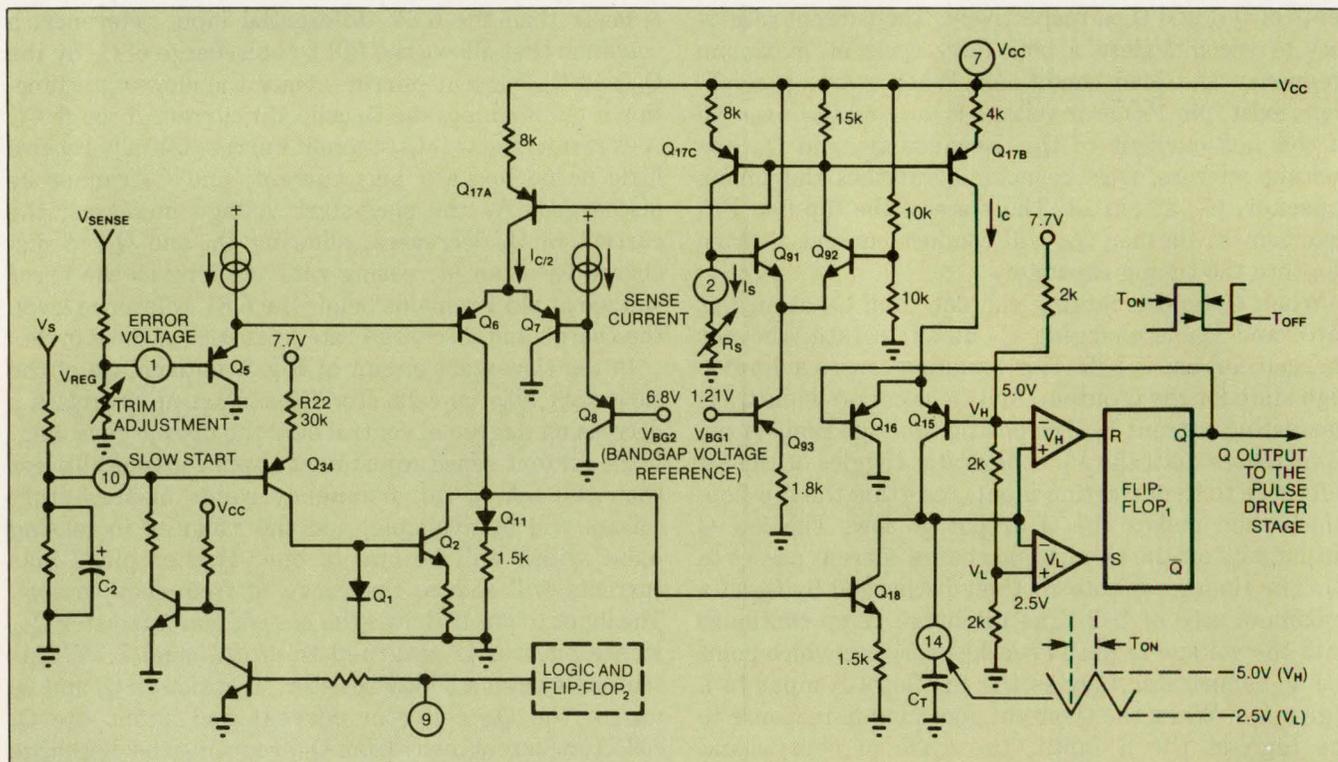


Fig 3—For a given timing capacitance, C_T , in the modulation and timing circuit of the CA1523, the maximum frequency of the P/FM circuit is determined by the current sense bias set by resistor R_S at pin 2.

affect the balance of charge and discharge currents somewhat. The minimum value you want for I_S is 20 μA ; the maximum available collector current from Q_{17C} —typically 350 μA —determines the upper limit.

Fig 4 shows a typical television receiver application. Line isolation permits the use of the TV receiver as an RGB or composite-video monitor. In this system, the switching transformer isolates the power line from the signal circuits of the TV receiver. In the block diagram, a 120V ac power line is connected through a fuse to the bridge rectifier and a step-down transformer, T_2 . The

rectified output of T_2 becomes a 16V standby power supply for the TV control module. In response to the user input controls, the control module switches Q_2 on and off to control turn-on of the circuit through the optoisolator. The bridge rectifier supplies 150V raw B+ to the CA1523's start-up circuit and to the primary of switching transformer, T_1 . After start-up, the run supply provides a regulated V_{CC} for the CA1523 from the sense feedback circuit. In normal regulation, the CA1523 drives the Q_1 power MOSFET that switches the primary of T_1 . T_1 converts regulated power to the 20V,

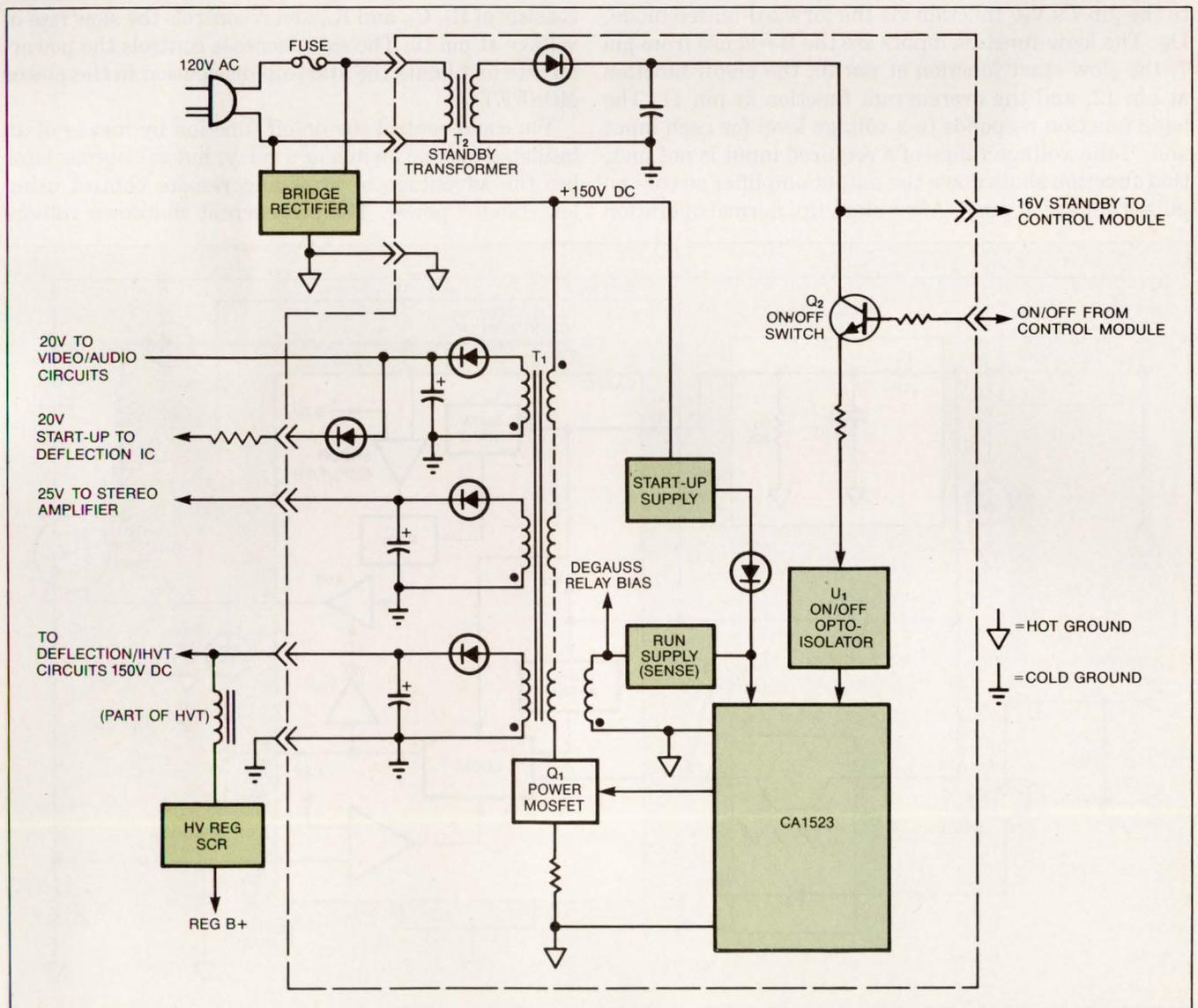


Fig 4—In a typical TV-receiver application, the switching transformer isolates the power line from the signal circuits of the receiver and provides the voltages required for the various circuit sections.

The error amplifier accepts error-correction inputs and controls the pulse-width and -frequency modulation.

25V, and 150V levels required for the power-supply outputs and the run-supply circuit.

Fig 5 illustrates the on/off operation of the switching-power-supply portion of the Fig 4 converter application. The logic function maintains control of the on/off operation of the system. When off, the system remains in a standby mode as long as the 120V ac is connected. Standby power comes from the start-up circuit consisting of R_2 and the 11V zener diode, D_3 . Continuous start-up bias is supplied to the V_{CC} function at pin 7, the on/off input at pin 12 via the optoisolator, and the slow-start circuit at pin 10. The 11V source is connected to the pin 7's V_{CC} function via the forward-biased diode, D_{13} . The logic-function inputs are the B+ sense from pin 7, the slow-start function at pin 10, the on/off function at pin 12, and the overcurrent function at pin 11. The logic function responds to a voltage level for each input and, if the voltage range of a required input is not met, that function shuts down the output amplifier so that no pulses appear at pin 6. After start-up, normal operation

resumes when the on/off input is greater than 2.5V, the peak overcurrent input is less than 1.2V, and the B+ sense has determined that V_{CC} is greater than 8.4V.

The slow-start function controls the gradual start-up of the pulse and frequency modulation functions in such a way that a slow RC rise time at pin 10 is functionally analogous to a slow decrease in the pulse interval. Likewise, as the pin 10 voltage increases, the slow start allows a gradual increase of the $I_C/2$ discharge current. As the voltage at pin 10 increases from 3 to 7V, the full range of slow-start control over the P/FM shifts from zero to maximum frequency. The RC time constant consists of R_1 , C_7 , and R_3 , and it controls the slow rise of voltage at pin 10. The slow increase controls the power-up rate and limits the start-up dissipation in the power MOSFET.

You could control the on/off function by means of an insulated manual switch or a relay, but the optoisolator has the advantage of providing remote control using low standby power. The overcurrent shutdown voltage

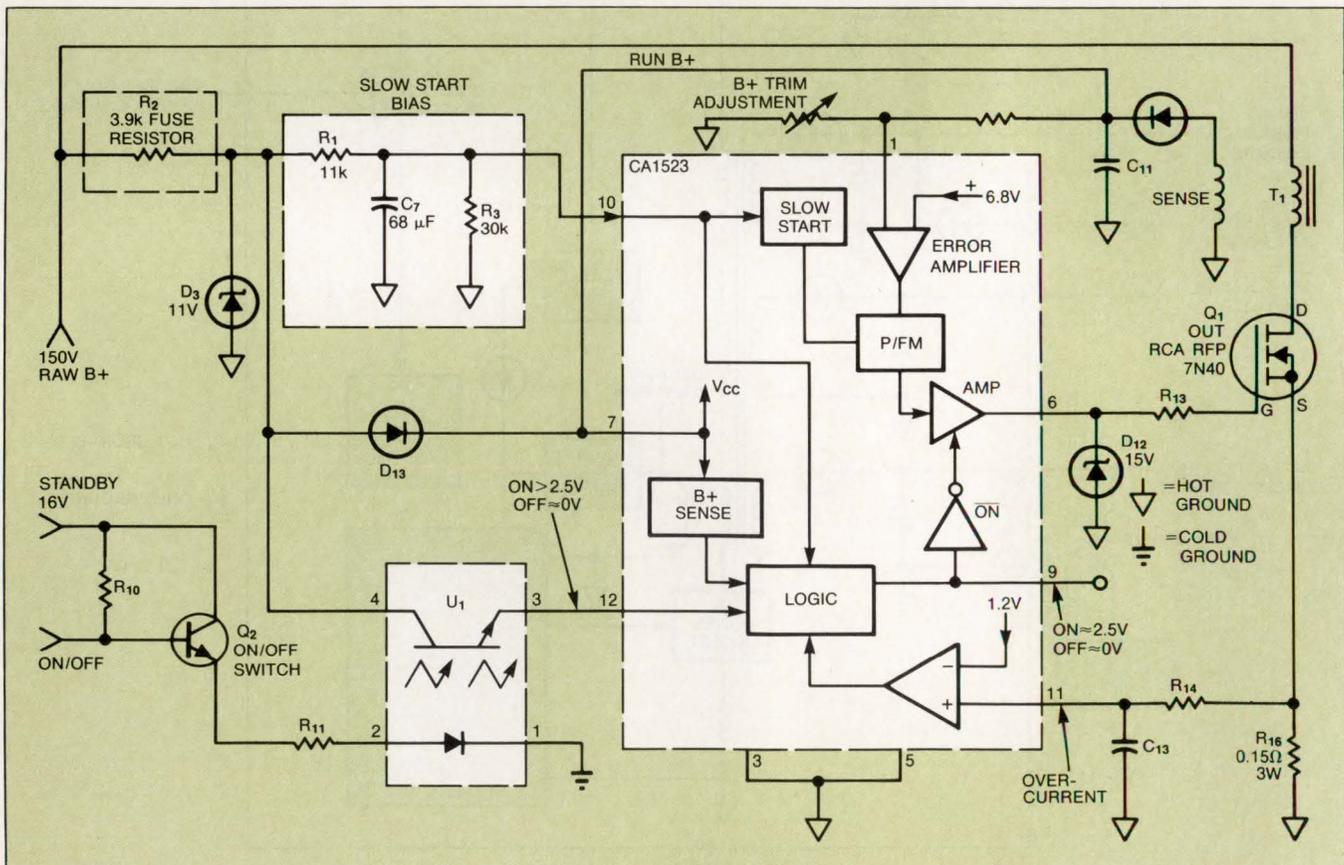


Fig 5—Within the on/off operation, logic function inputs from pin 7, slow-start bias from pin 10, opto-coupler on/off function from pin 12, and over-current protection from pin 11 control system operation.

is sampled from the source terminal of the power MOSFET to ensure that peak currents in the transformer primary circuit will be fault-mode limited. When start-up is completed, the run B+ is greater than the start-up supply voltage from the 11V zener diode, and D_{13} is reverse biased. The on/off and slow-start input circuits remain under the control of the 11V start-up source, but the CA1523 power supply is transferred to the regulated run B+ supply derived from the sense winding of the transformer.

Fig 6 shows the switching-regulator's output operation in a normal feedback mode. The error amplifier's voltage at pin 1 is differentially compared to a 6.8V internal reference. The error amplifier supplies the

correction signal for the P/FM function. The timing capacitor C_{15} and sense-current resistor R_9 control the pulse-width and -frequency modulation. The logic input controls the output amplifier; the capacitor C_{14} controls that amp's rise time. Zener diode D_{12} and resistor R_{13} protect the gate of power MOSFET Q_1 . As Q_1 switches the raw B+ current through the primary of transformer T_1 , power is supplied to the output windings and the sense winding. The pulse in the sense winding is rectified, supplying run power to the CA1523 and error feedback to pin 1 through the resistor divider. The ratio of resistor R_8 to the parallel trim resistors R_4 , R_5 , R_6 , and R_7 sets the output voltage of the CA1523. You selectively clip the trim resistors from the pc board to

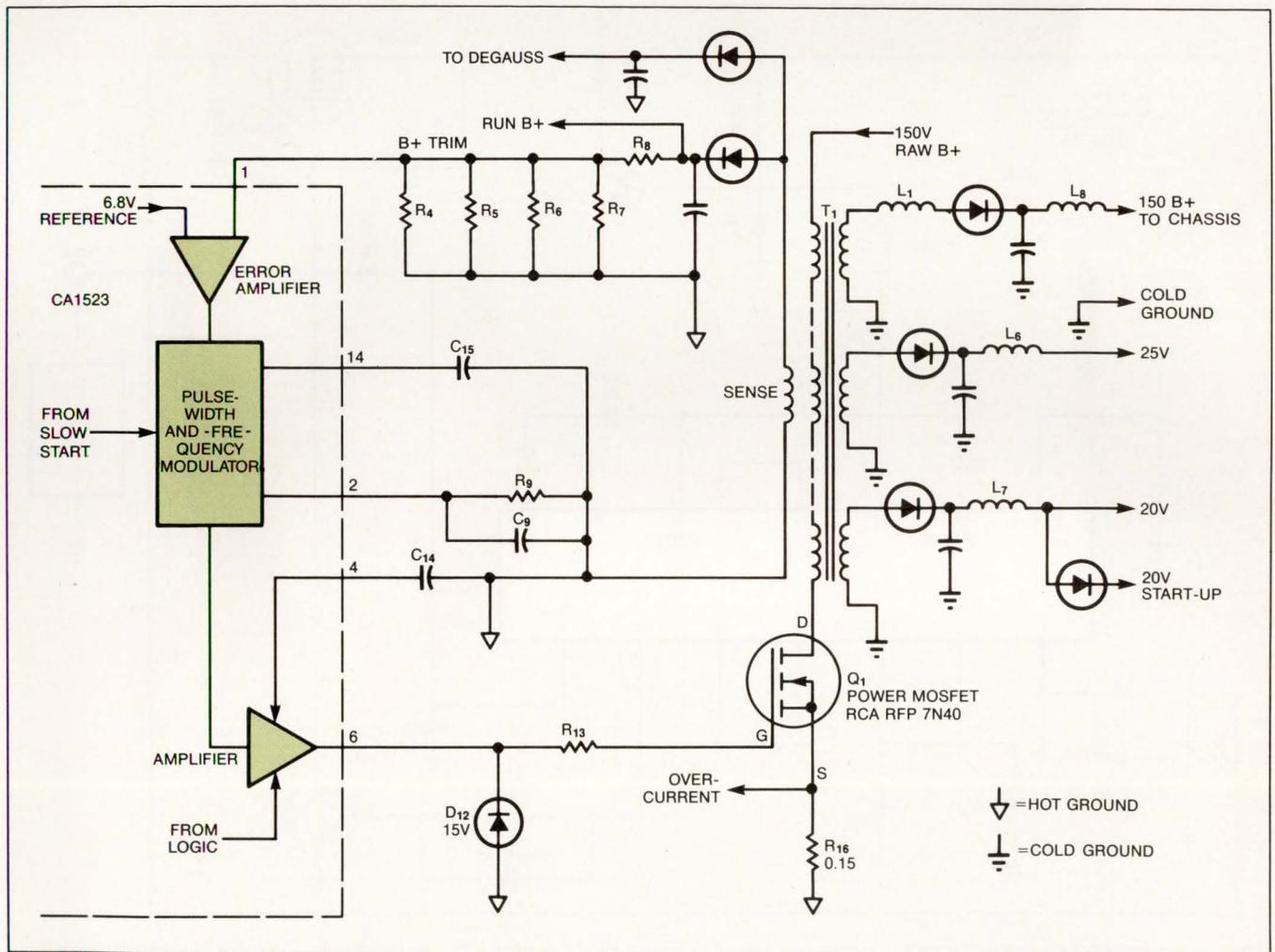


Fig 6—When the CA1523's output functions in a normal feedback mode, the input to the error amplifier from the rectified sense voltage is compared to the 6.8V internal reference and provides the correction signal for the P/FM function. Timing capacitor C_{15} and sense current resistor R_9 controls the pulse-width and -frequency modulation. The logic input controls the output amplifier, whose rise time is determined by capacitor C_{14} .

At start-up, an increase of the slow-start bias on a capacitor exercises a decreasing degree of control over the discharge timing.

adjust the output of the regulator to the required value.

You could use a limited-range potentiometer adjustment to control the regulator output, but this approach is potentially dangerous unless the high voltage of the CRT is limited in some way. For safety reasons, it's best to use the fixed resistor-divider network. Because of the tight coupling of the transformer windings, the sense winding reflects the input-voltage changes and the output-loading conditions. The preferred run B+ is 12 to 13V. The product of the resistor-divider ratio and the run B+ voltage should be approximately 6.8V. When working with direct ac-line power circuits, you must use an isolation transformer for protection.

The circuit shown in Fig 7 depicts a buck-type

regulator, useful in lower-voltage applications, with a nominal raw B+ of 28V and an input tolerance range of 18 to 38V. The start-up features in this circuit minimize standby current in zener-diode D_2 and use the internal zener diode for slow-start control. As shown, you can adjust the error feedback voltage over a range of about 6.8 to 13.5V. The pulse frequency range is typically 25 to 75 kHz, and the regulation at a nominal 12V output is typically 0.3%.

This circuit does not require an output transformer unless you want to isolate the output from the input. The 2N2102 transistor inverts the pulse output of the CA1523 and this output drives an RFP8P10 p-channel enhancement-mode power FET. The power FET is

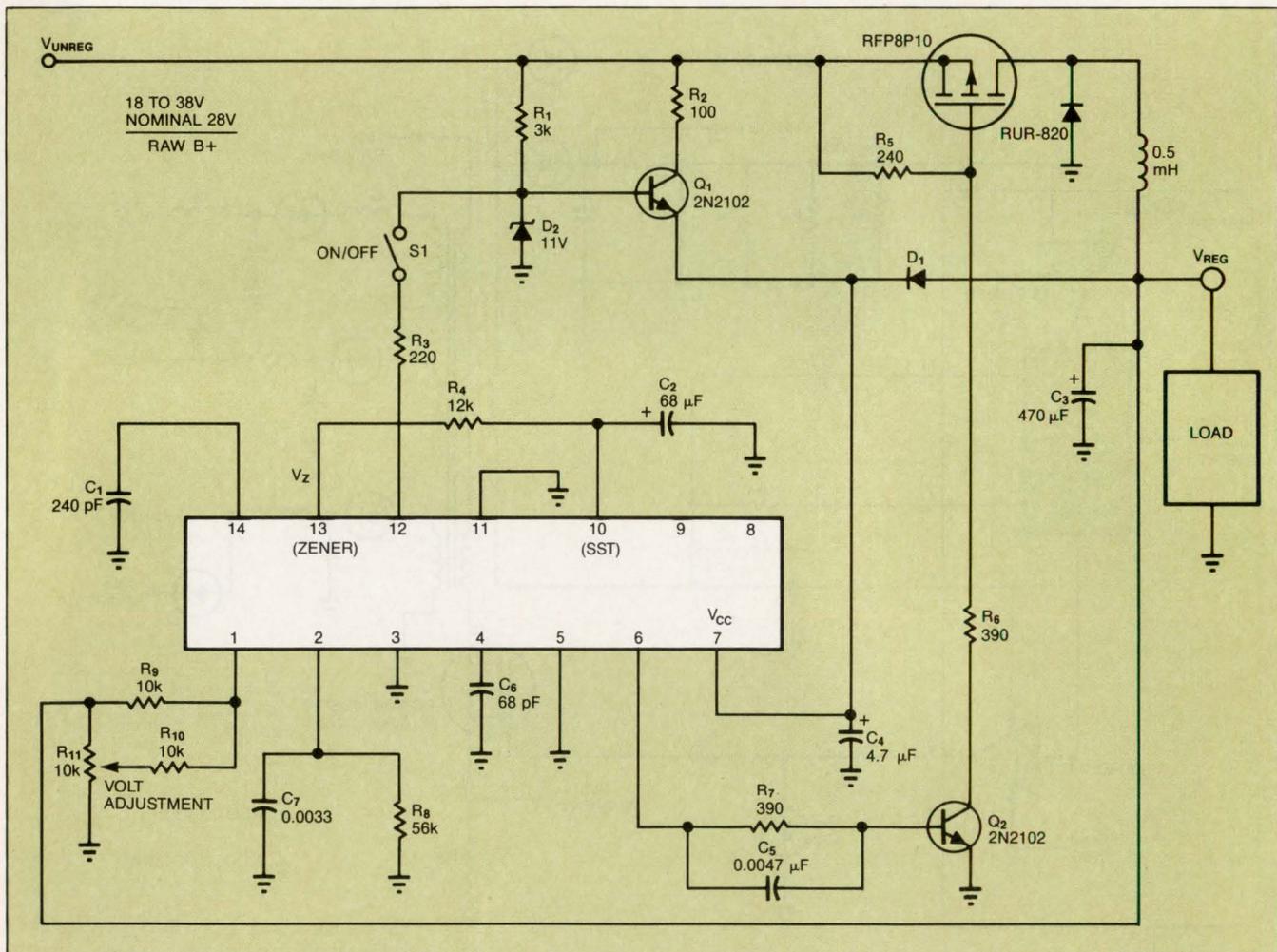


Fig 7—The buck regulator is useful in low voltage applications. It has an adjustable output voltage and a special start-up feature that minimizes the standby current in zener D_2 and makes use of the internal zener diode for slow-start control. The error feedback voltage is adjustable over a range of 6.8 to 13.5V, and the pulse-frequency range is typically 25 to 75 kHz. Regulation at a nominal 12V output is typically 0.3%.

When the engineer gets an idea the designer gets the picture

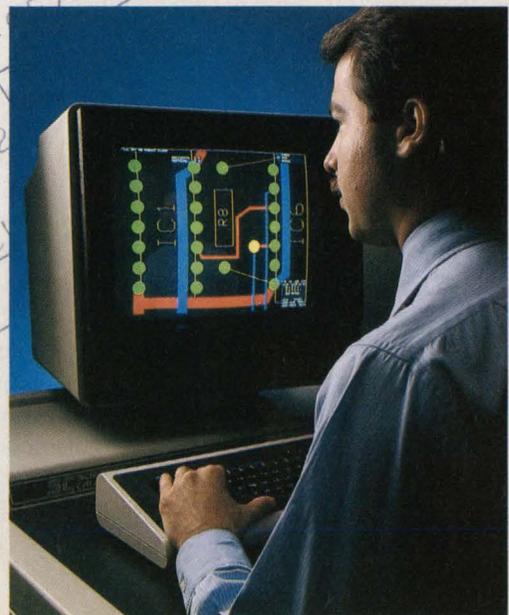
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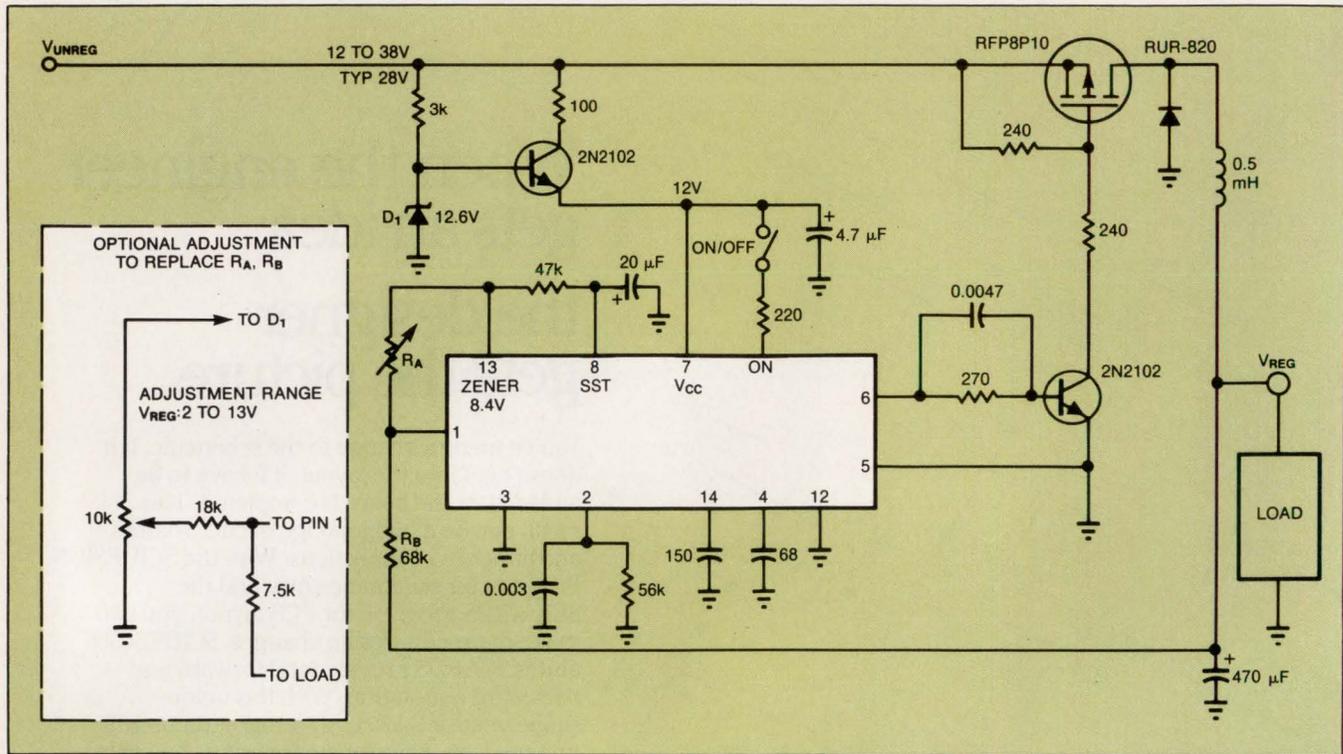


Fig 8—A buck regulator uses the internal zener diode at pin 13 as a reference for the return divider from the regulated output voltage. An optional adjustment uses the external start-up zener diode to replace the resistive divider.

driven through a resistive divider that limits the maximum source-to-gate voltage. In the output drain circuit of the power MOSFET, a shunt RUR-820 fast-switching catch diode is followed by a filtering circuit, which consists of a 0.5-mH choke and a 470- μ F capacitor.

The raw B+ input is typically a 28V battery source or the filtered output of a bridge rectifier supplied from a line-isolated step-down transformer. The start-up components are substantially different from those shown in the transformer-isolated flyback-converter circuit. However, you can use the start-up circuit shown here in either system. Assuming you choose the output voltage range of the regulator to be 11 to 13V, transistor Q_1 conducts for only a brief period after S_1 is closed. The raw B+ is supplied through diode D_1 to V_{CC} at pin 7, and the emitter of Q_1 is reverse-biased after the power-up cycle is completed. This arrangement substantially reduces the continuous power dissipation of zener diode D_2 and resistor R_1 . Even when the V_{REG} voltage is less than the zener diode's voltage, the base current to Q_1 is a fraction of a milliampere in a normal run mode. However, more base current is required to charge C_4 when the power is turned on. After start-up is complete and the standby on/off switch is closed, approximately 1.6 mA of current is supplied to pin 12. Typically, you need less than 2 mA to sustain idle current to zener diode D_2 .

A number of bias options are available for implementing the error-voltage feedback, and you can adapt most of the options to either the buck regulator or the transformer flyback-converter system. Either system must feed back a sense return voltage of approximately 6.8V to pin 1. You don't have to power the CA1523 by

the sense return voltage, but if you do, the voltage should be approximately 11 to 13V. The CA1523 will operate over a supply voltage range of 9.5 to 15V.

As shown, the buck-regulator circuit of Fig 7 has an output-voltage adjustment range of 2 to 1. This range extends from the typical 6.8V error-reference level to twice the error-reference level. If diode D_1 is removed and Q_1 used with zener diode D_2 to supply the raw B+ for regulated V_{CC} , you can set higher levels of output by changing the divider ratio using the formula $R_{10}/(R_9 + R_{10})$. With a ratio of 3 to 1, the typical output voltage will be 3 times 6.8, or 20.4V. Under this condition, the V_{UNREG} input voltage must be higher than 20.4V plus the amount of the saturated voltage drop in the power MOSFET. If the error input to pin 1 is directly connected to the V_{REG} output, the typical output voltage is 6.8V.

Two concerns are central when V_{REG} output-voltage levels are less than 6.8V. First, the return resistor divider that sets the output voltage level must be referenced to a positive voltage greater than 6.8V. Second, when using the 11V zener-diode reference, a power-down condition may allow the V_{REG} output voltage to increase when the zener voltage collapses. When that happens, the pin 1 voltage will decrease and the error voltage will increase the pulse output drive, increasing V_{REG} . If you choose the right components, you can avoid the turn-off output-voltage peaking problem when the raw B+ collapses, and even extend the low-voltage regulation range.

The circuit of Fig 8 is particularly useful for low-voltage supplies and shows the use of the internal zener diode at pin 13 as a reference for the return divider



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from the output V_{REG} voltage source. For $R_A=68\text{ k}\Omega$, the regulated output voltage is 5V. For $R_A=31.7\text{ k}\Omega$, the output voltage is approximately 3.3V. Also shown is an optional adjustment method using the start-up zener diode, D_1 . The range of this adjustment is approximately 2 to 13V. The output frequency range is 28 to 77 kHz.

The uses of the CA1523 previously discussed are application specific to a switch-mode controller for power supplies. Fig 9 shows the CA1523 used as a general-purpose voltage-controlled oscillator, pulse generator, and driver circuit with a minimum of external components. The VCO control input is at the base of the external transistor Q_1 , which provides a linear drive current to the current sense, pin 2. (You must provide the base of Q_1 with enough dc bias to generate approximately 100 μA of collector current to drive pin 2.) For a given timing capacitance at pin 14, the pin 2 current controls a 50% duty-cycle pulse frequency at the pin 6 output. The frequency is linear with the VCO input to Q_1 . The pin 1 error voltage is biased low, but you can gate it to provide synchronous burst control of the VCO output. Some of the typical characteristics of this circuit are listed in the table in Fig 9.

The current-drive capability of the pulse output from pin 6 is $\pm 50\text{ mA}$ max into an 1800-pF load. The internal zener bias and bandgap reference sources keep the output frequency very stable over a power-supply range of 10 to 15V.

EDN

Author's Biography

Wayne M Austin is a section manager with the GE/RCA Solid State Division in Somerville, NJ. His responsibilities include application engineering for standard ICs in consumer electronics and automotive electronics as well as DSP. Wayne has a BSEE from the University of Illinois, and an MSEE from Rutgers. He is a member of Tau Beta Pi, the JEDEC JC-41 committee, and the ICCE conference paper committee. In his spare time, Wayne enjoys photography and travel.



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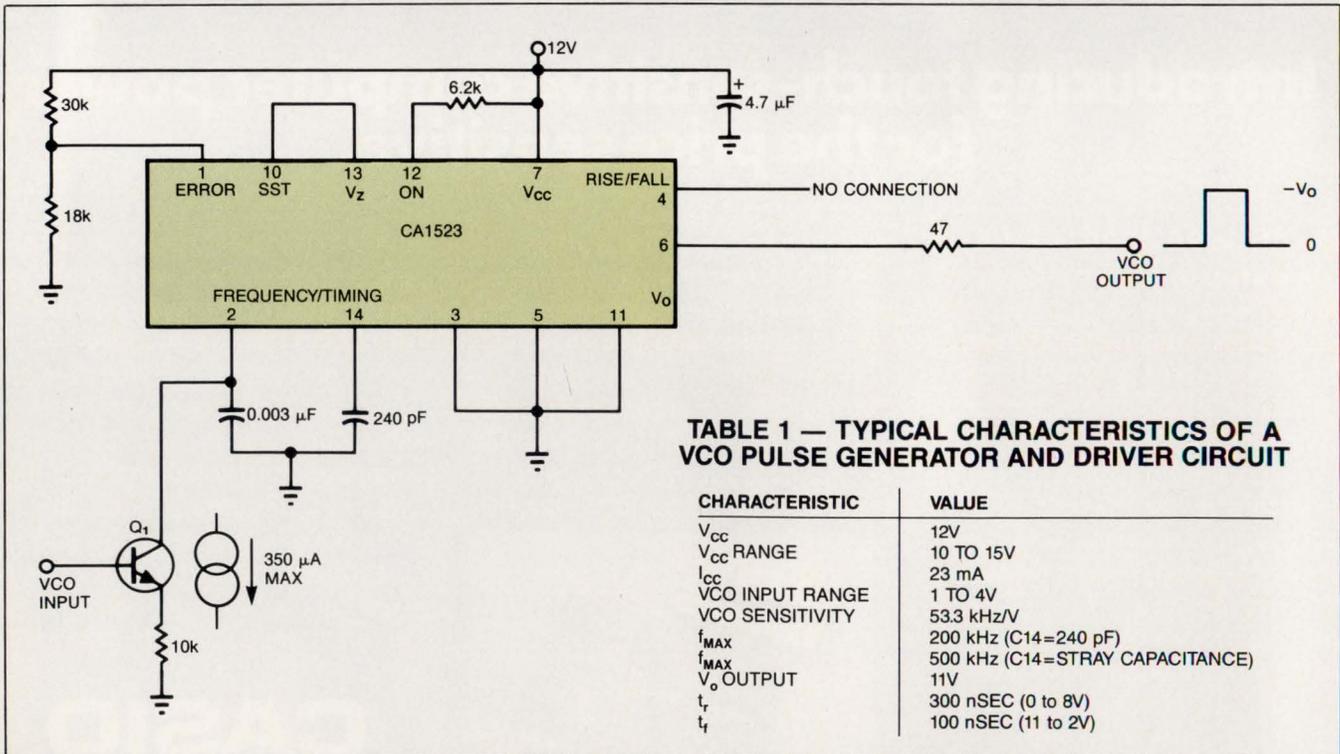


TABLE 1 — TYPICAL CHARACTERISTICS OF A VCO PULSE GENERATOR AND DRIVER CIRCUIT

CHARACTERISTIC	VALUE
V_{CC}	12V
V_{CC} RANGE	10 TO 15V
I_{CC}	23 mA
VCO INPUT RANGE	1 TO 4V
VCO SENSITIVITY	53.3 kHz/V
f_{MAX}	200 kHz (C14=240 pF)
f_{MAX}	500 kHz (C14=STRAY CAPACITANCE)
V_o OUTPUT	11V
t_r	300 nSEC (0 to 8V)
t_f	100 nSEC (11 to 2V)

Fig 9—The CA1523 can act as a general-purpose VCO pulse generator. The external transistor provides a linear drive current to the current sense input, pin 2. The timing capacitor at pin 14 controls the pulse-frequency output; pin 2 current controls the 50% duty cycle.



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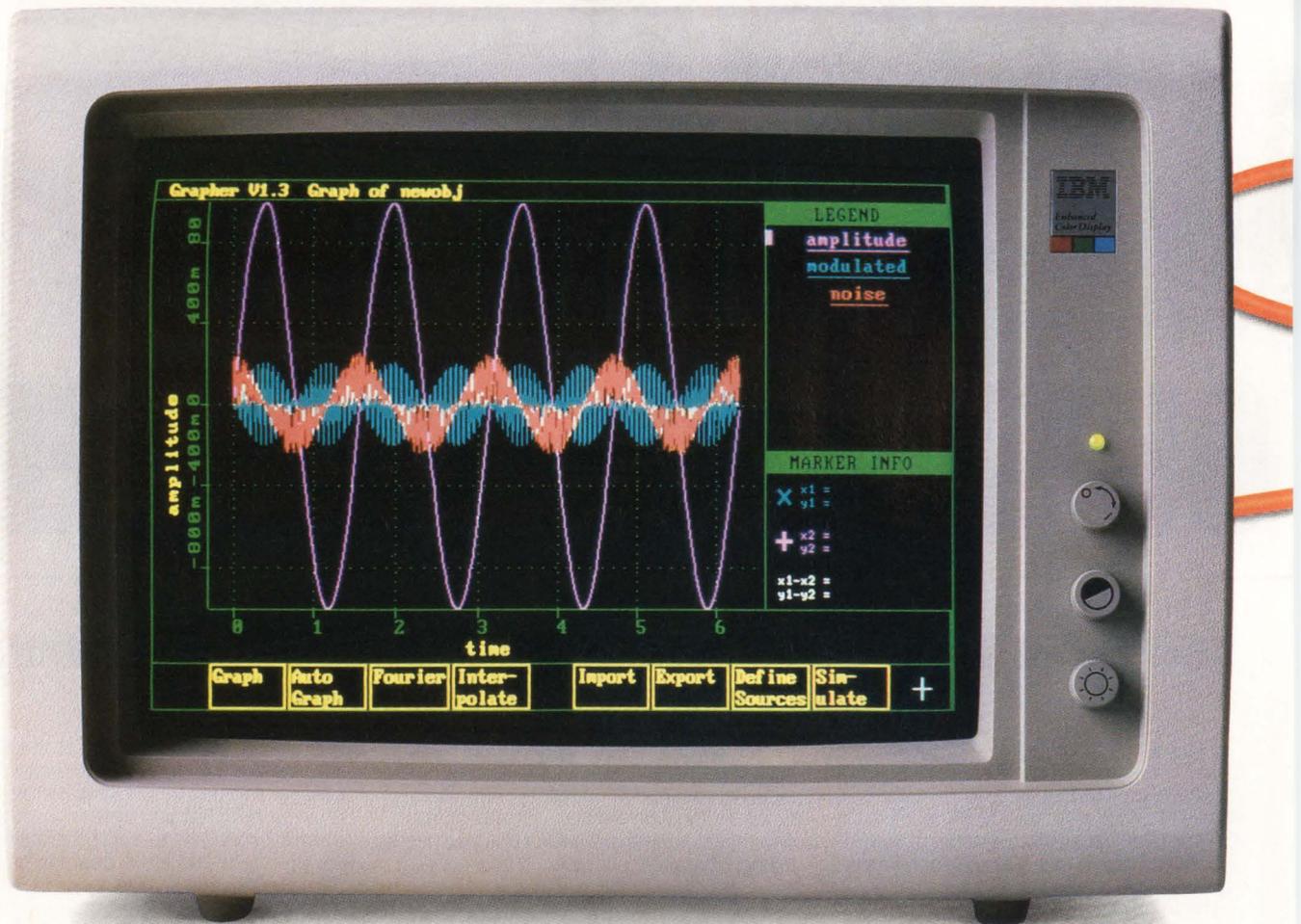
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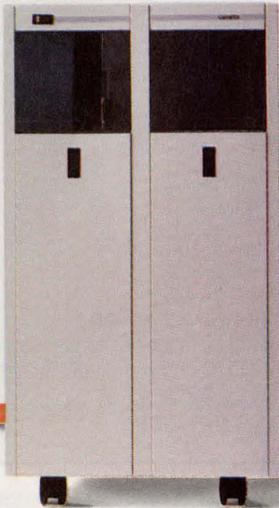
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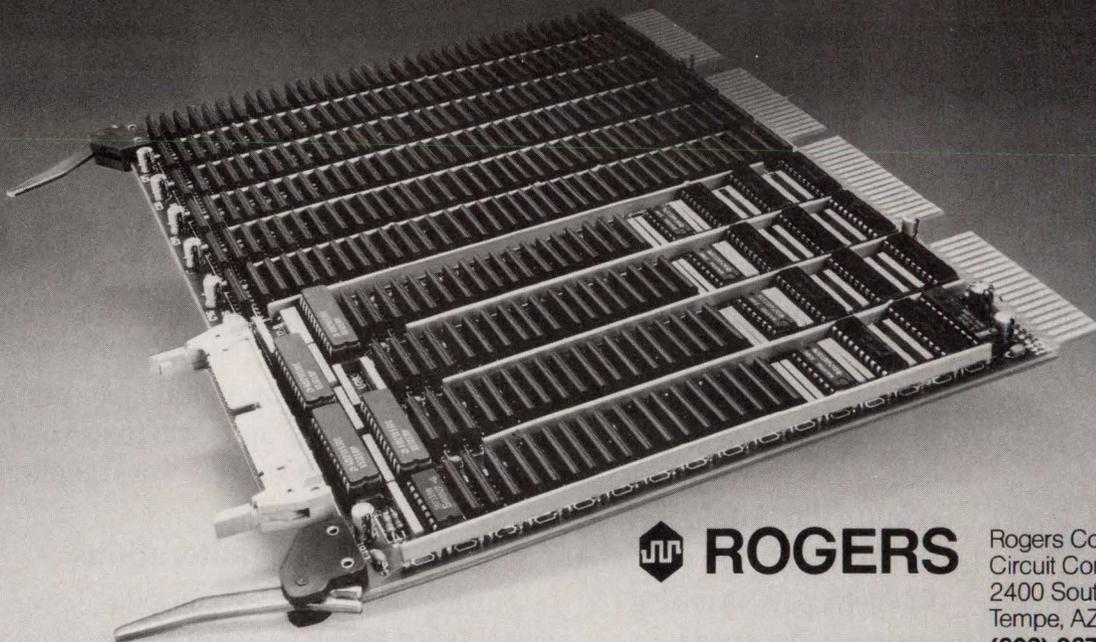
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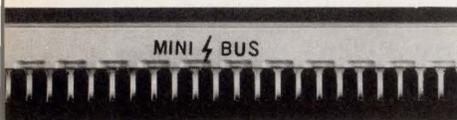
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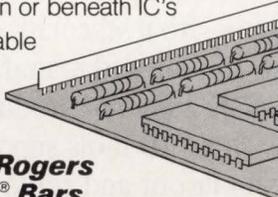
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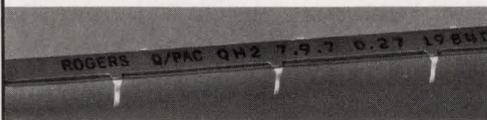
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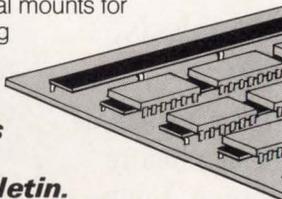
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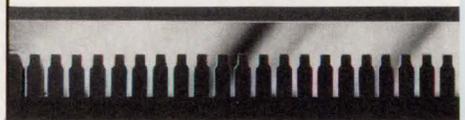
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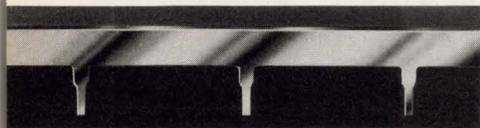
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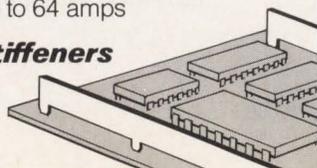
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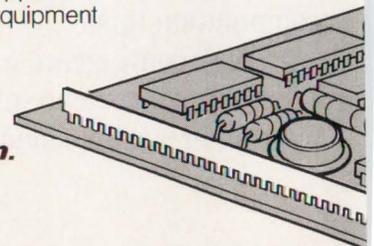


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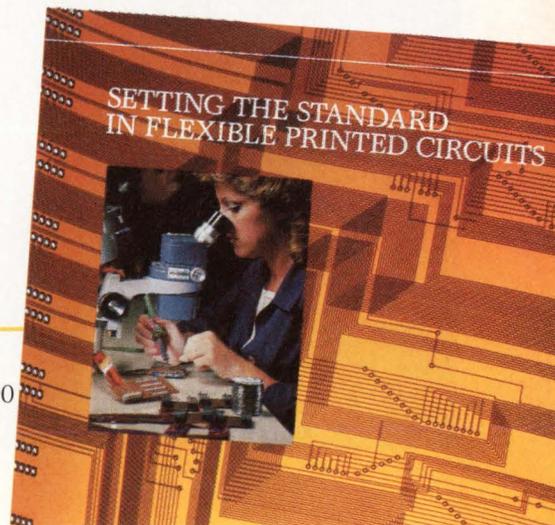
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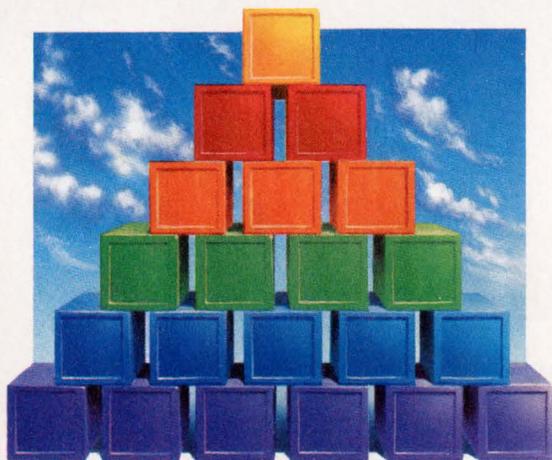
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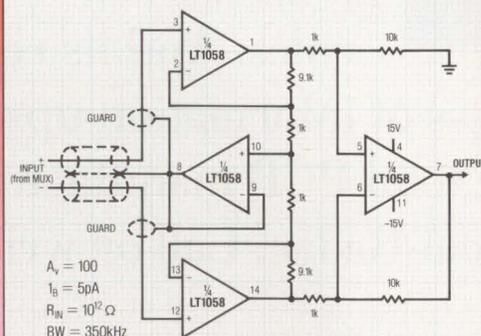
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DESIGN IDEAS

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Electrostatic voltmeter uses BiMOS op amp

Harold A Wittlinger and Robert Kumbatovic
GE/RCA, Somerville, NJ

The circuit of **Fig 1** is a noncontact-type electrostatic voltmeter capable of measuring voltages as low as 1V, suiting it for the measurement of IC packages' electrostatic potential. With this voltmeter, you can measure high voltages also. The capacitance between the voltage source and the meter's input plate forms a voltage divider with capacitor C_1 , setting the meter's full-scale value for a given source-to-plate distance. This full-scale vs distance relationship is nonlinear: 5 kV at 3.5 in., 1.7 kV at 2 in., and 700V at 1 in.

Op amp IC_1 is configured as a voltage follower in which feedback current activates the $-500\text{-}0\text{-}500\text{-}\mu\text{A}$ meter. The op amp's low bias currents (less than 1 pA

typ) provide high sensitivity, and the 100Ω resistor R_1 sets the op amp's full-scale output at $\pm 50\text{ mV}$. The slide switch S_1 turns the voltmeter on and off; also, it lets you test the positive and negative battery voltages. (A meter reading of $323\ \mu\text{A}$ or higher indicates a satisfactory battery.)

The shutter is spring-loaded in the closed position, which shorts the amplifier input to ground and discharges C_1 . To take a reading, you zero the μA meter by adjusting potentiometer R_2 and then simply open the shutter. Or, you can keep the shutter open and monitor any movement of the source with respect to the meter.

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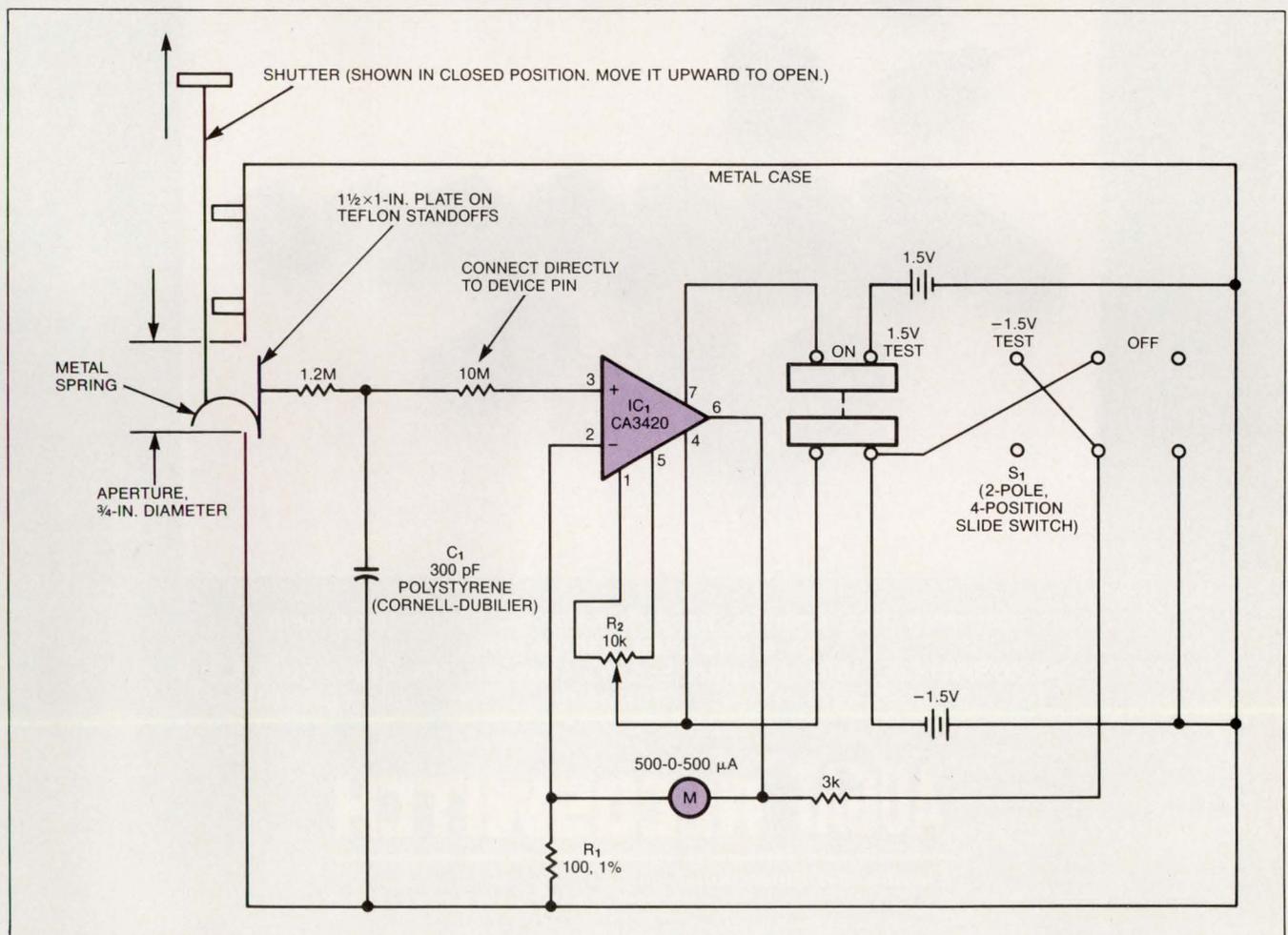


Fig 1—This voltmeter measures electrostatic potential as low as 1V without touching the voltage source. The full-scale input at 3.5 in., for example, is 5 kV.

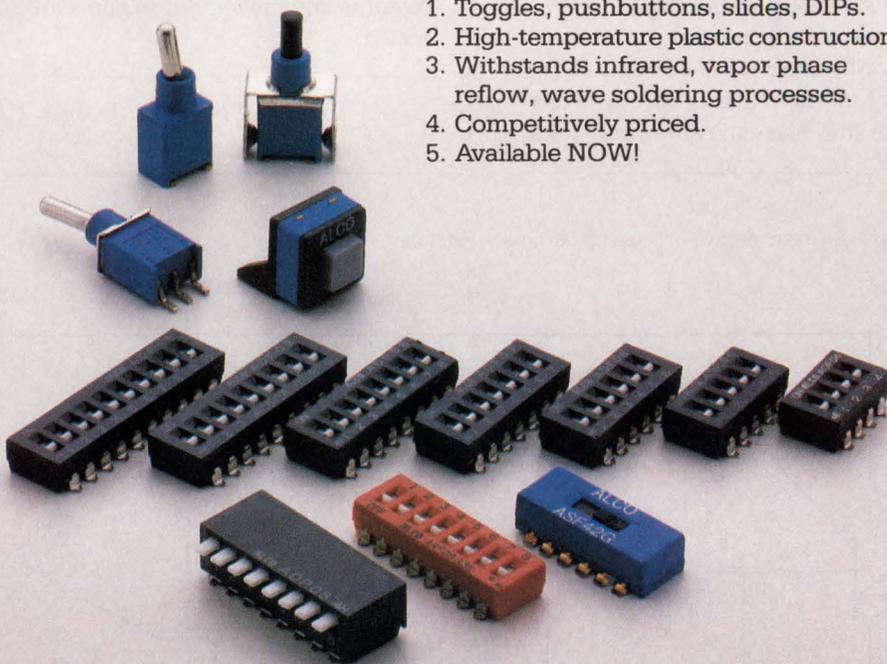
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The straightforward multiplication of two complex numbers requires the computation of four product terms (**Listing 1**). A program that first computes three intermediate terms (using add and subtract operations) can multiply complex numbers using only three product terms (**Listing 2**), thereby achieving a net reduction in the number of required CPU clock cycles.

The technique of **Listing 2** is useful in applications such as graphics transformations, digital filters, and FFT computations. You can save an appreciable amount of time if your program executes many thousands of complex multiplications. In a 1024-point FFT, for example, you save 10 msec per transform.

Multiplication of two complex numbers yields a real (R) and imaginary (I) part as follows:

$$R+jI=(A+jB)(C+jD),$$

where

$$R=AC-BD \text{ and } I=BC+AD.$$

Listing 1 simply generates the four product terms ($A*C$, $B*D$, $B*C$, and $A*D$). The routine, written for the Intel processor family, stores the 16-bit input variables A, B, C, and D in the memory locations AX, BX, CX, and DX, and it writes the 32-bit complex results to the locations RM, RL, IM, and IL. **Listing 2**, however, generates the three product terms $P_1=A*(C+D)$, $P_2=D*(A+B)$, and $P_3=C*(B-A)$, and it computes the result as $R=P_1-P_2$ and $I=P_1+P_3$.

Inspection of the code listings shows that the faster code executes three add operations and one negate operation instead of the fourth integer-multiply operation. The time savings can be significant. For example, for the 80286 μ P, eliminating one integer multiplication saves 24 cycles. The negation and three addition operations add eight cycles, for a net savings of 16 cycles. For the 80186 μ P, the savings is 34 minus 12, or 22 cycles.

The 3-multiply approach requires six additional bytes of code, but on many systems execution is still about 2 μ sec faster. Note that you must scale the input values to avoid overflow in the result or in the intermediate terms $C+D$, $A+B$, and $B-A$.

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To Vote For This Design, Circle No 747

LISTING 1—4-MULTIPLY APPROACH

```
; ----- using 4 imul instructions -----
push    ax        ;save A
mov     di,dx     ;save D
imul   dx         ;p4
mov     IL,ax
mov     IH,dx     ;save p4
pop     ax        ;get A
imul   cx         ;p1
mov     RL,ax
mov     RH,dx     ;save p1
mov     ax,di     ;get D
imul   bx         ;p2
sub     RL,ax
sbb    RH,dx     ;p1-p2
mov     ax,bx     ;get B
imul   cx         ;p3
add     IL,ax
adc     IH,dx     ;p3+p4
; ----- end complex multiply -----
```

LISTING 2—3-MULTIPLY APPROACH

```
; ----- using 3 imul instructions -----
push    ax        ;save A
mov     di,dx     ;save D
neg     ax        ;-A
add     ax,bx     ;B-A
imul   cx         ;p3
mov     IL,ax
mov     IH,dx     ;save p3
mov     ax,cx     ;get C
add     ax,di     ;C+D
pop     cx        ;get A
imul   cx         ;p1
mov     RL,ax
mov     RH,dx     ;save p1
add     IL,ax
adc     IH,dx     ;p1+p3
mov     ax,cx     ;get A
add     ax,bx     ;A+B
imul   di         ;p2
sub     RL,ax
sbb    RH,dx     ;p1-p2
; ----- end complex multiply -----
```

Circuit ensures proper RS-232C mating

Ralph L Adcock
SKP Electronics, Santa Ana, CA

Connectors for RS-232C data links aren't keyed, which increases the chance that you might plug the connector in backwards, reversing the transmit and receive pins and disabling a piece of equipment. The circuit of Fig 1 masks this mistake by automatically swapping the transmit and receive signals, allowing you to plug the connector in either way.

The RS-232C transmit and receive signals connect, via 1-k Ω resistors, to optocouplers IC₂ and IC₃. These devices produce a logic zero at their outputs (pin 6) in response to an input of either polarity having a magnitude exceeding 3.8V. (RS-232C signals are a minimum of $\pm 5V$.) In turn, the outputs cause the J-K flip-flop's output (IC₄, pin 5) to set the position of analog switch IC₁ correctly.

At power-on, active drivers at each end of the RS-232C link maintain a voltage on the transmit and receive lines—regardless of data transmission. If the plug is mated correctly, the voltages cause the optocouplers' outputs to each assert a logic zero. Consequently, the flip-flop's output remains unchanged.

If you insert the plug backwards, you remove voltage from the input of one of the optocouplers, producing a logic one output. The flip-flop will then toggle in response to the first negative clock transition, toggling the switch and restoring the proper RS-232C connections. (The clock input can be either a pushbutton contact closure or a signal of approximately 1 kHz.) The optocouplers' 250- μ sec response time prevents the circuit from directing a change of connections during the zero-crossings of a data transmission.

The LED (D₁) indicates the direction of the plug connection—that is, whether the TXD signal is on pin 2 or 3 of the RS-232C interface. Also, when you apply a continuous clock signal, the LED indicates either that there isn't any RS-232C connection or that the power is off at the other end; the system will hunt under these conditions. A given clock frequency sets a lower limit on the baud rate, though. With a 1-kHz clock, for example, the system can handle 300 to 19.2k baud, but it may exhibit false switching at 50 baud.

EDN

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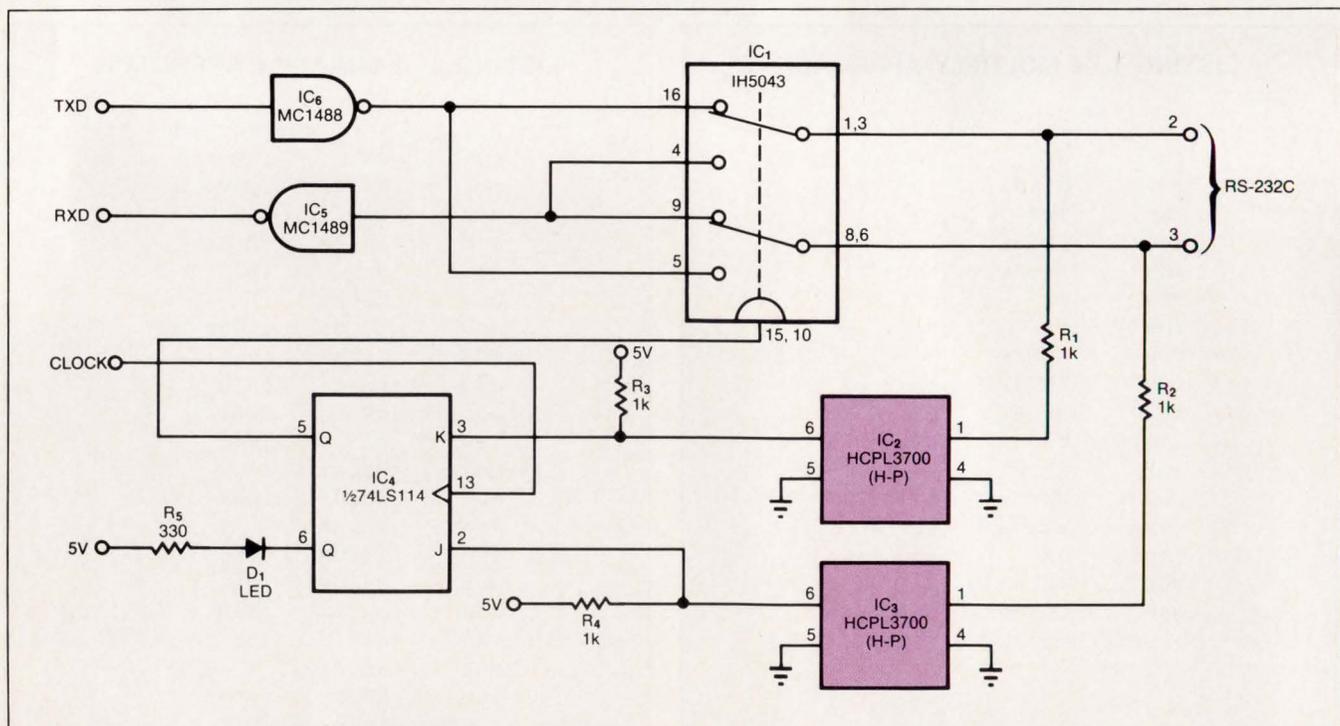
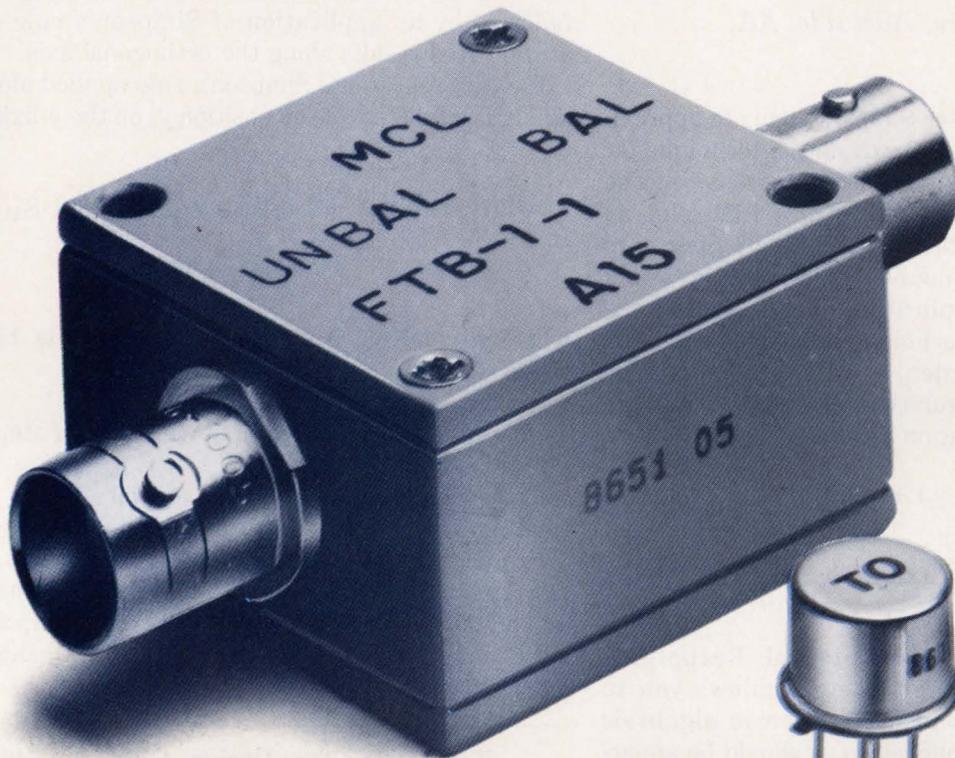


Fig 1—If you inadvertently plug in an RS-232C connector backwards (crossing the transmit and receive signals), this circuit will detect the fault and automatically swap the signals back to the proper lines.

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CIRCLE NO 91

Simpson's rule solves double integrals

A Cameron

Defence Research Centre, Adelaide, SA,
Australia

Although one generally uses Simpson's rule to approximate single integrals, you can extend the technique for use in solving double integrals. The C language routine of **Listing 1** contains the required algorithm plus an example, demonstrating that you can apply Simpson's rule to certain complex double integrals that would normally require the application of numerical techniques. In addition, the technique applies equally well to integrals of a higher order.

You can obtain the algorithm by substituting the standard Simpson integration formula,

$$S_X(y_j) = f(x_0, y_j) + f(x_n, y_j) + 4 \sum_{i=1}^{\frac{n-2}{2}} f(x_{2i-1}, y_j) + 2 \sum_{i=1}^{\frac{n-2}{2}} f(x_{2i}, y_j),$$

for the double integral's inner integral. Reapplying Simpson's rule to the outer integral allows you to express the original integral equation in algebraic terms. After further simplification, it should be apparent that this technique consists of an integration along

one axis for each interval on the orthogonal axis, followed by an application of Simpson's rule on the accumulated results along the orthogonal axis.

If $S_X(y_n)$ represents Simpson's rule applied along the x-axis as a function of the position y_n on the y-axis, then

$$\text{SIMPSON} = \frac{h_x \cdot h_y}{9} (S_X(y_0) + S_X(y_n) + 4 \cdot S_X(y_1) + 2 \cdot S_X(y_2) \dots \text{etc}),$$

where h_x and h_y represent the increments between steps:

$$h = (\text{upper limit} - \text{lower limit}) / (\text{number of steps}).$$

The example in **Listing 1** is a partial solution for the total radiated power through a hemispherical surface. Two quarter-wavelength monopole antennas, separated by a quarter wavelength and fed by signals that are out of phase by a quarter wavelength, are the source of the radiated power. (The result should be 3.829042.)

EDN

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LISTING 1—C LANGUAGE ROUTINE

```

/*-----
Simpson integration technique for
evaluating double integrals.
-----*/

#include "math.h"

float fxy[100][100],fy[100];
float pi;
main() {

float f();
float llx, lly, ulx, uly, x, y;
float hx, hy, ef, of, simpson;
int nosx, nosy, i, j;

/*-----
Simpson integration constants.

nos -> number of strips
ul -> upper limit of integration
ll -> lower limit of integration
h -> incremental value per strip
-----*/

```

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DESIGN IDEAS

LISTING 1—C LANGUAGE ROUTINE (Continued)

```
pi=3.1415926;
nosx=30; nosy=40;
llx=0.1e-8;lly=0.1e-8;
ulx=pi; uly=2.0*pi;
hx=(ulx-llx)/nosx;
hy=(uly-lly)/nosy;

printf ( " \n\nDouble integration parameters: \n");
printf ( " Step size hx and hy:  %f,%f\n",hx,hy);
printf ( " Number of steps(x,y):  %d,%d\n\n",nosx,nosy);

/*
Calculate all the points within the
integration region.
*/
for (j=0; j <= nosy; j++) {
    for (i=0; i <= nosx; i++) {
        x = hx*i+llx;
        y = hy*j+lly;
        fxy[i][j] = f(x,y);
    }
}

/*
Now perform a Simpson integration along
the x axis and accumulate results using
the y axis variable as an index.
*/
for (j=0; j <= nosy; j++) {
    of=fxy[1][j];
    ef=0.0;
    for (i=2; i <= nosx-2; i += 2) {
        ef += fxy[i][j];
        of += fxy[i+1][j];
    }
    fy[j]=fxy[0][j]+fxy[nosx][j]+2.0*ef+4.0*of;
}

/*
Lastly perform Simpson integration
along the y axis.
*/
of=fy[1];
ef=0.0;
for (j=2; j <= nosy-2; j += 2) {
    ef += fy[j];
    of += fy[j+1];
}
simpson = (hx*hy/9.0)*(fy[0]+fy[nosy]+2.0*ef+4.0*of);

printf("Result = %f\n\n",simpson);
}

/*
Enter the function to be integrated here.
*/
float f(x,y) float x,y; {
double xd,yd,zd,zd1;

    xd = x; yd = y;
    zd = pi*cos(xd)/2.0;
    zd = cos(zd);
    zd1 = pi*(1.0-sin(xd)*cos(yd))/4.0;
    zd1 = cos(zd1);
    zd = zd*zd1;
    zd = pow(zd,2.0)/sin(xd);
    return ( fabs(zd) );
}
```

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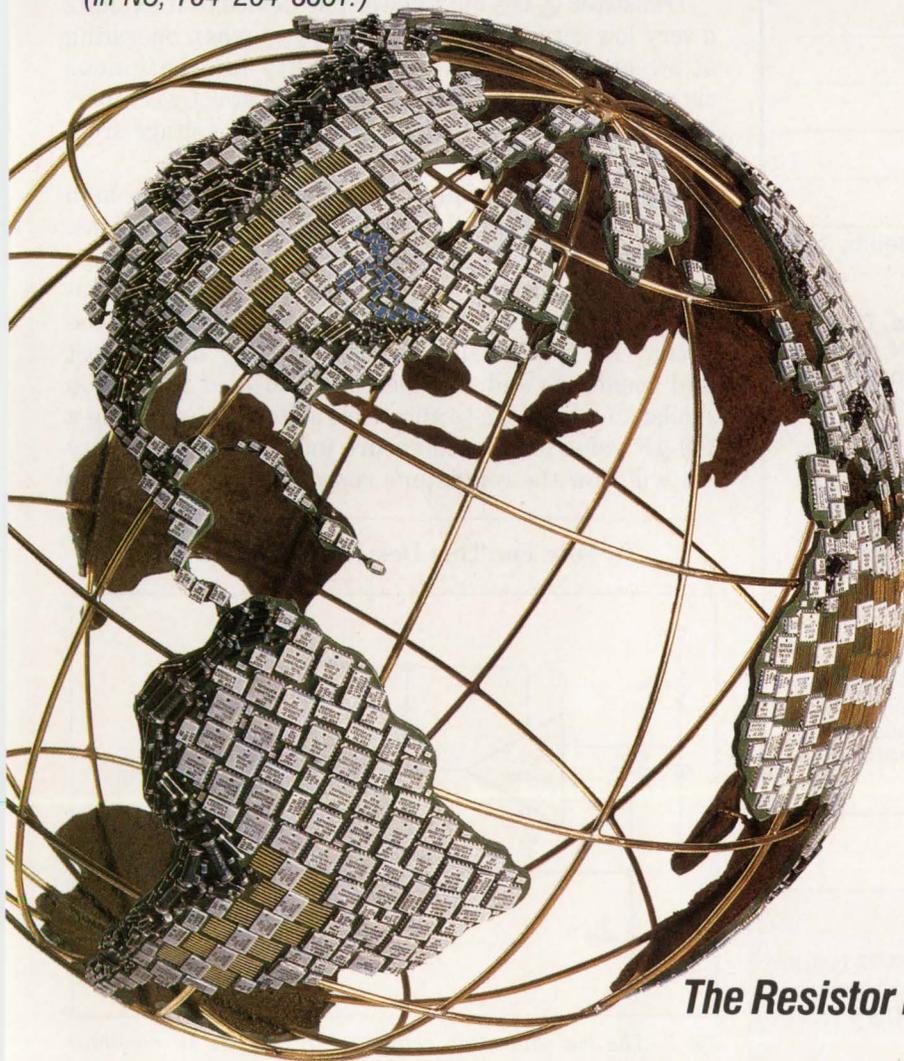
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ISSUE WINNER

The winning Design Idea for the March 31, 1987, issue is entitled "Current monitor uses Hall sensor," submitted by Paul Galluzzi of Dynamics Research Corp (Wilmington, MA).

Regulator has low drop-out voltage

Thomas C Fatur
Analog Control Systems, Greensburg, PA

The voltage regulator of **Fig 1** allows an input-output differential (drop-out voltage) as low as 0.1V. This low drop-out voltage lets you design battery-operated products in which the battery includes a minimal number of voltage cells. The circuit provides a 5V regulated output and delivers 500 mA max. You can choose R_1 and R_2 to produce other output voltages by using the following equation:

$$V_{OUT} = \left[\left(\frac{R_1}{R_2} \right) + 1 \right] V_{REF.}$$

Transistor Q_1 is a high-power pnp device that exhibits a very low saturation voltage ($V_{CE(SAT)}$) when operating at 5% or less of its rated capability for continuous current. Op amp IC_2 controls the transistor by comparing a fraction of V_{OUT} with the reference voltage from IC_1 .

Resistor R_3 allows the op amp's output to swing high enough to turn off Q_1 under light- or no-load conditions. You select R_4 based on Q_1 's h_{FE} and the op amp's current-sink capability. (R_4 and C_1 determine the regulator's output time constant.) C_1 also stabilizes the circuit. Its 10- μ F value ensures stability under most load conditions and provides line and load regulation similar to a typical 3-terminal regulator. Substituting a 100- μ F value for C_1 will ensure unconditional stability but will slow the regulator's response. **EDN**

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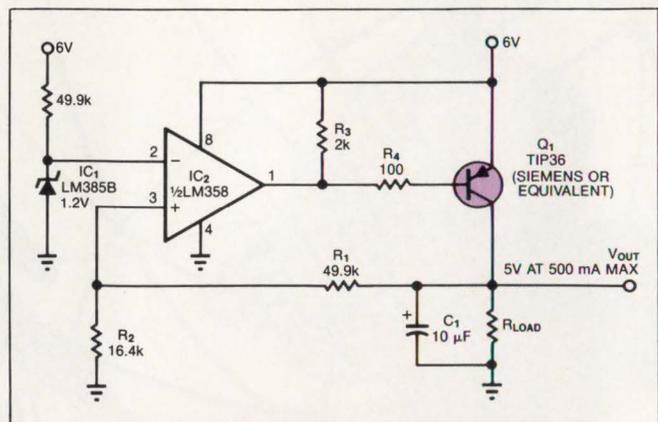
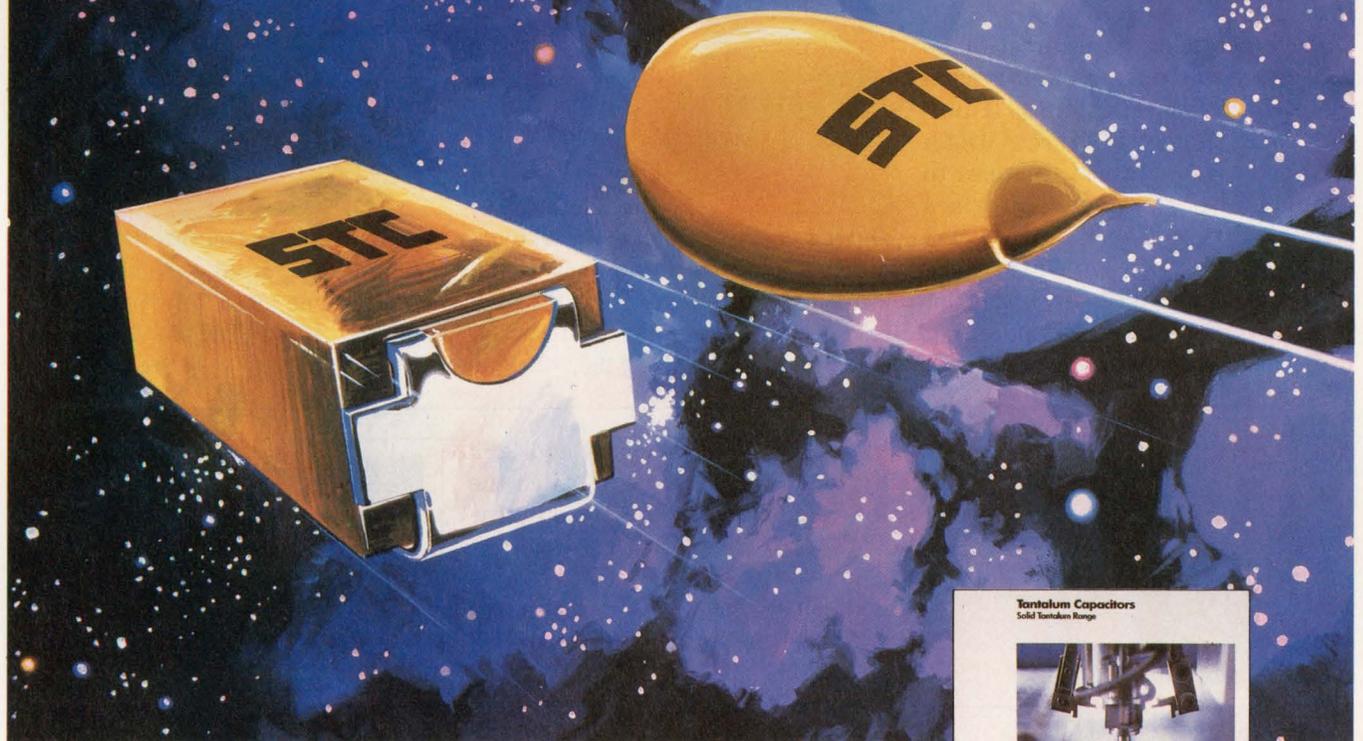


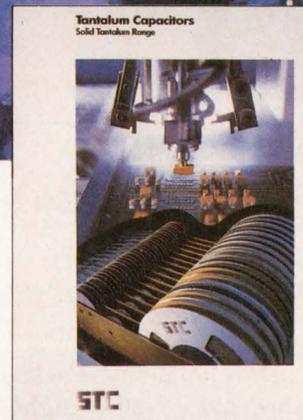
Fig 1—The low saturation voltage of Q_1 lets this 5V regulator operate with input-output differentials as low as 0.1V.

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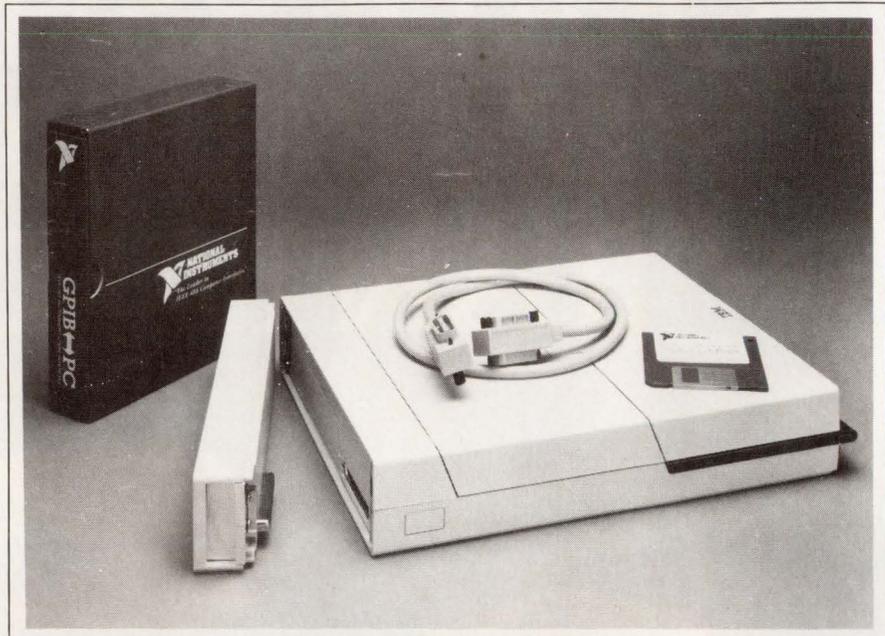
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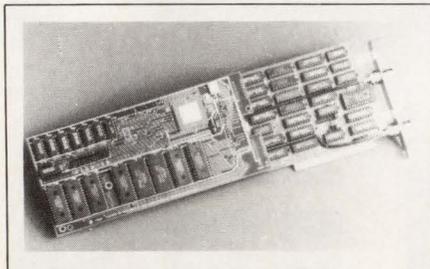
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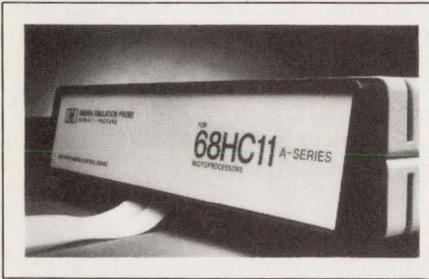
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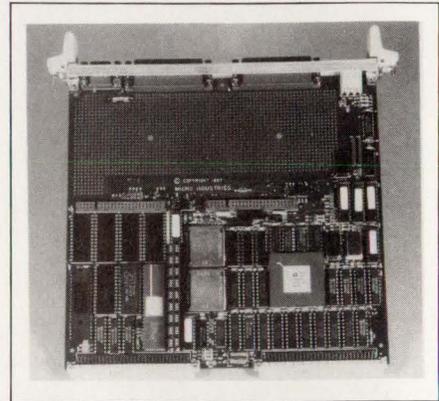
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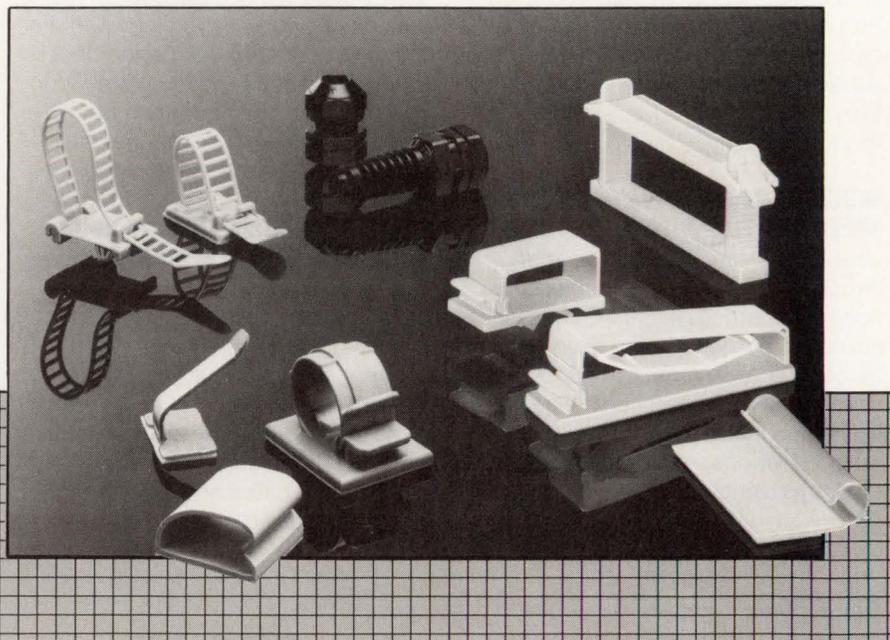
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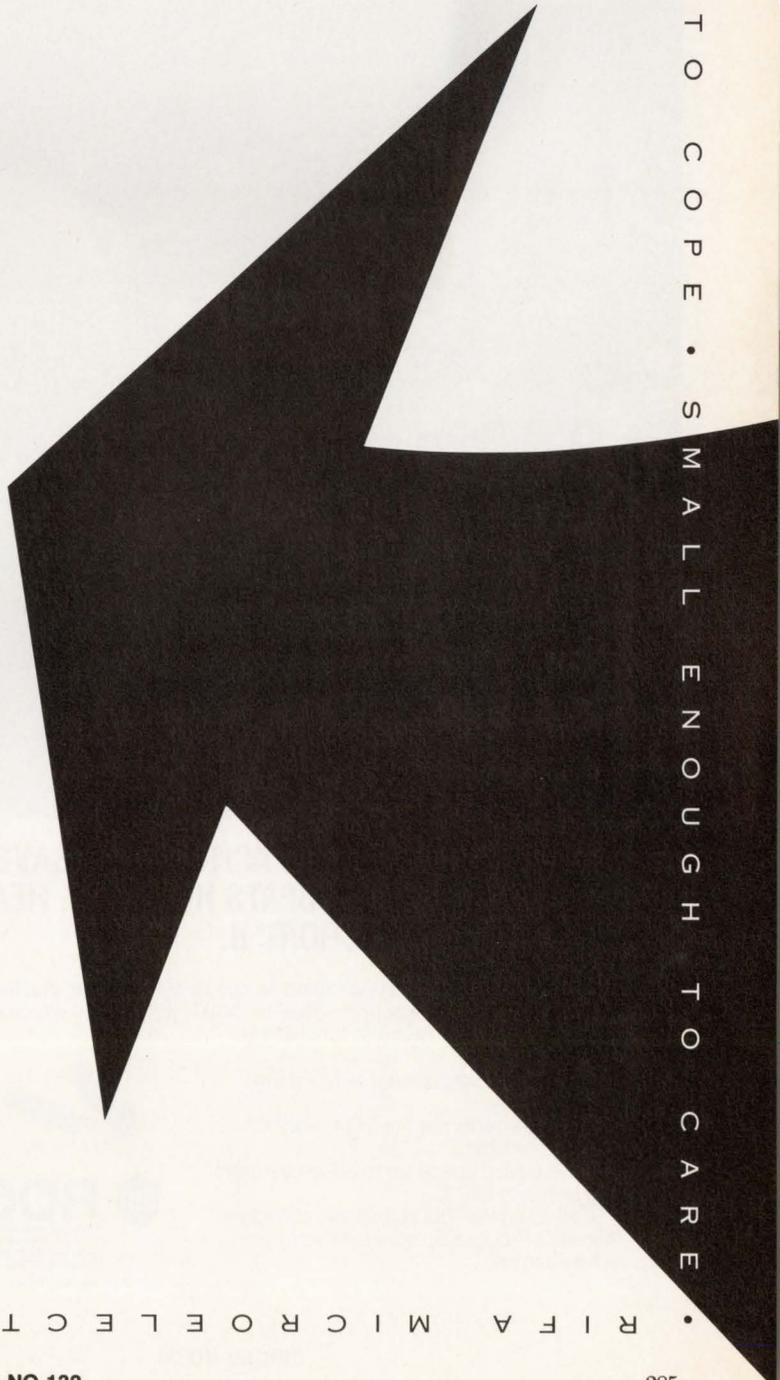
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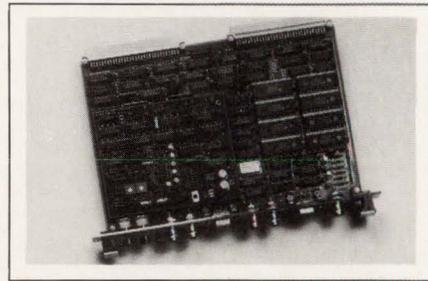
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- Digitizes video images at 20M samples/sec
- Has user-formatted frame sizing

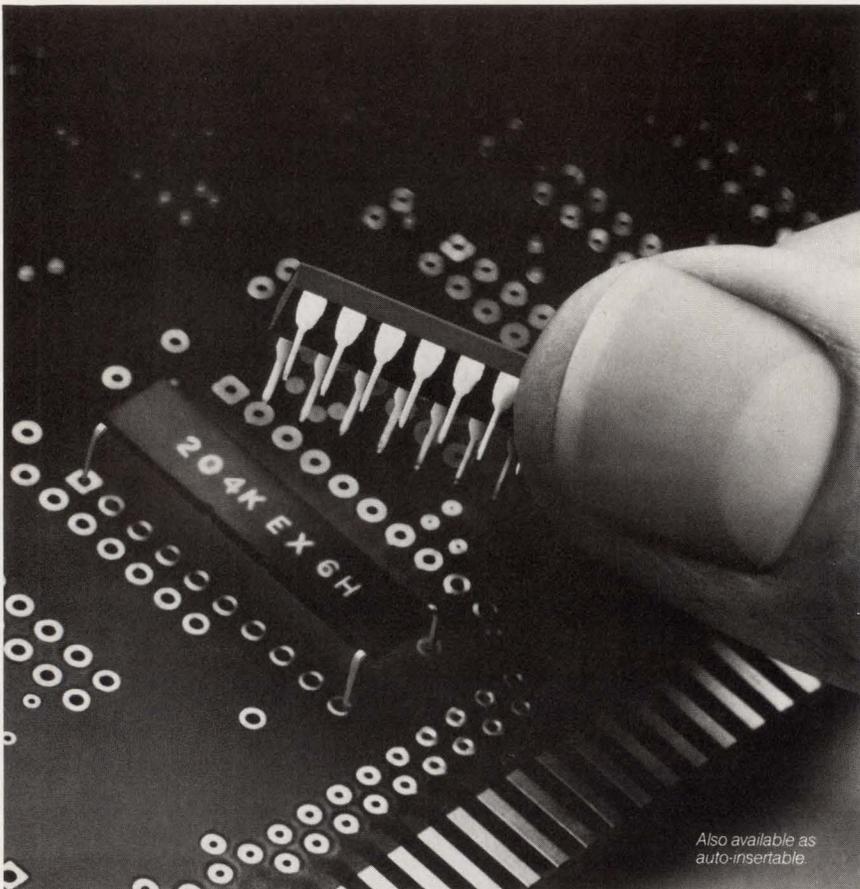
The SP-Diva video acquisition board for VME Bus systems digitizes an incoming video signal by comparing the signal to a programmable threshold level at the rate of



20M samples/sec. The resultant 1-bit pixels are stored in onboard video memory capable of holding 512k (or, optionally, 1024k) pixels. You can program the comparator's threshold to one of 256 levels via software or via up/down pushbuttons on the board's front panel, and you can read back the selected threshold level via the VME Bus. You can configure the picture format at between 64 and 1024 pixels/line and between 32 and 512 lines/frame, so you can hold one or more frames in the video RAM. Because the video RAM has ports to the VME Bus, the system's CPU can manipulate the image. The board provides an output for a video monitor and an input for a light pen. SP-Diva sells for \$2508. An image-processing system based on the board and on Motorola's VersaDOS operating system costs \$8585.

NV Spinnov SA, Pleinlaan 2, Building K-6, 1050 Brussels, Belgium. Phone (02) 6412844. TLX 61051.

Circle No 356



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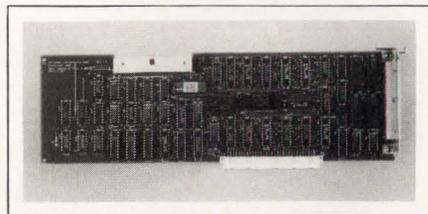
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CIRCLE NO 36



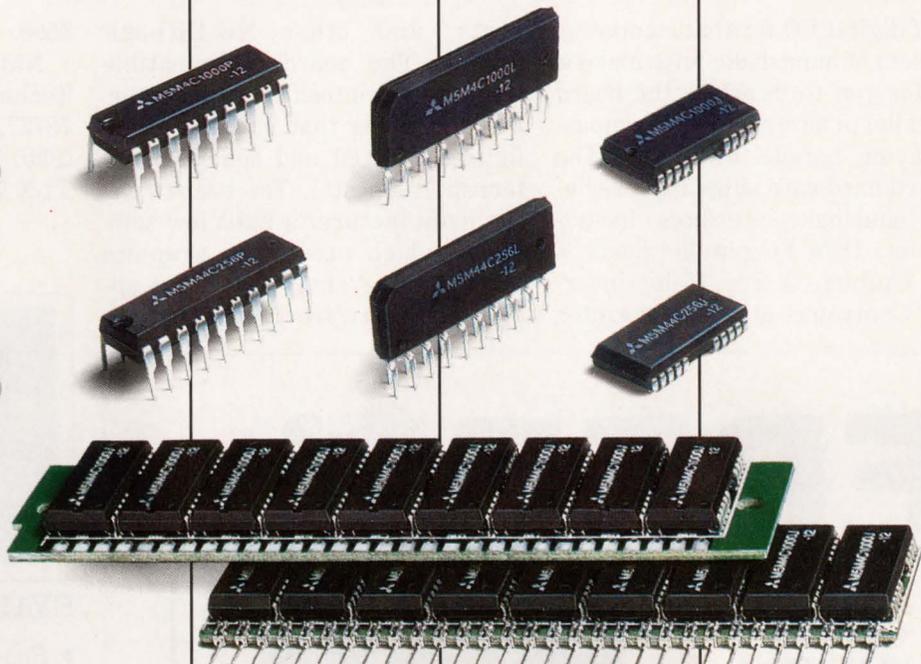
I/O BOARD

- Board provides 32 bits of I/O for the Macintosh II
- Ports are byte-programmable as inputs or outputs

The NB-DIO-32F interface board for Apple Computer's recently announced Macintosh II provides 32

The Mitsubishi CMOS 1Mb High Density DRAMs.

x 1's
x 4's
+ 2



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CMOS Optimum package selection. Fast t_{CAC} access times. Mitsubishi introduces 1Mb performance and packaging that let you design your systems the way you want.

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Mitsubishi's 1Mb ZIP package provides a cost-effective, widely sourced high density alternative to DIPs. The ZIP's low profile allows tight board-to-board spacing, plus, it's auto-insertable using traditional DIP through-hole production technology.

Part #	Configuration	Mode	Package			Access Time (ns)		
			Plastic DIP (P)	Plastic J-Lead (J)	Plastic ZIP (L)	t_{RAC} / t_{CAC} (-10)	t_{RAC} / t_{CAC} (-12)	t_{RAC} / t_{CAC} (-15)
M5M4C1000	1M x 1	Fast Page	•	•	•	100/25	120/30	150/40
M5M4C1001	1M x 1	Nibble	•	•	•	100/50	120/60	150/75
M5M4C1002	1M x 1	Static Column	•	•	•	100/25	120/30	150/40
M5M44C256	256K x 4	Fast Page	•	•	•	100/25	120/30	150/40
M5M44C258	256K x 4	Static Column	•	•	•	100/25	120/30	150/40
MH1M08	1M x 8	Fast Page	J (socketed), JA (pinned)			100/25	120/30	150/40
MH1M09	1M x 9	Fast Page	J (socketed), JA (pinned)			100/25	120/30	150/40

For high density applications, where an upgrade from a 256K x 8/9 is required, and/or height is not critical, Mitsubishi also offers 1M x 8 and 1M x 9 SOJ memory modules.

CMOS Technology

Mitsubishi's CMOS design makes two new modes of 1Mb device operation possible: static column and fast

page (a clocked static column). Both modes exhibit t_{CAC} access times twice as fast as traditional NMOS designs, making high performance microprocessor systems much easier to design.

For additional information, call or write Mitsubishi Electronics America, Inc., Semiconductor Division, 1050 E. Arques Ave., Sunnyvale, CA 94086. (408) 730-5900, ext. 2314.

1M x 1 DRAM Package Dimension Comparison

Package	Relative Density (Plane)	Relative Density (Volume)	Package Height In. (max.)
DIP (Dual In-Line)	1.0	1.0	0.18
ZIP (Zig-Zag In-Line)	1.6-2.0	0.7	0.4
SOJ (Small Outline J-Lead)	1.05* (2.1**)	1.1*	0.165
Module (1M x 9 Chips)	3.25/device	0.7/device	0.8

* Mounted only on one side of board.
** Mounted on both sides of board.

Quality Through Commitment



bits of digital I/O for that computer. Dual sets of handshake lines make it easy for you to interface the board to parallel printers or other computers having parallel interfaces. The onboard hardware supports a variety of handshake interfaces, including 8-bit, IBM PC parallel ports; a DEC Unibus; Q Bus 16-bit interfaces; Centronics-style 8-bit printer

ports; and other NB-DIO-32F boards. The board is compatible with the Macintosh II NuBus interface (including that interface's configuration ROM and nonmaster-interrupt requests). The board runs the manufacturer's LabView software, which provides a graphics programming environment for application-software construction.

\$595.

National Instruments, 12109 Technology Blvd, Austin, TX 78727. Phone (800) 531-4742; in TX, (800) 433-3488 or (512) 250-9119. TLX 756737.

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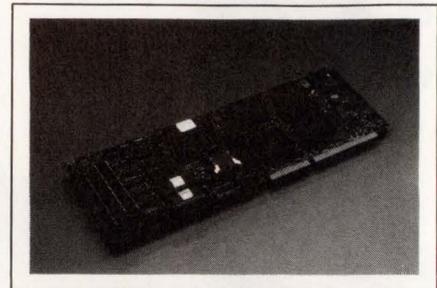
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CIRCLE NO 37



EVALUATION BOARD

- *Board is compatible with IBM PC/AT development*
- *Lets you evaluate the vendor's 4-chip IBM PC/AT set*

The ZyATB-1 board is an evaluation vehicle for the manufacturer's Poach (PC on a chip) chip family, which consists of the Poach/AT 2-chip set and the two Poach/ATB buffer chips. These four chips perform 75% of the functions of the LSI, MSI, and SSI devices found on the IBM PC/AT mother board. The evaluation board includes an 80286 μ P, an 80287 math coprocessor, an 8042 keyboard controller, a 64k-byte ROM, 512k bytes of RAM, the standard PC/AT I/O functions, and an interface to the system's expansion bus. \$1500.

Zymos Corp, 477 N Mathilda Ave, Sunnyvale, CA 94086. Phone (408) 730-5400.

Circle No 358

GRAPHICS BOARD

- *Provides hardware windowing, bit-block transfers*
- *Maintains compatibility with IBM CGA and EGA boards*

The TT786 graphics board for IBM PCs, PC/XTs, PC/ATs, and compatibles is based on the Intel 82786 graphics coprocessor. The board

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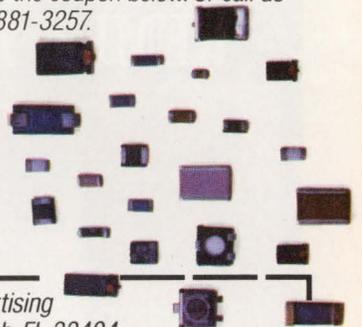
Our Thick Film Resistors are particularly well suited to surface mount circuits because of their high reliability and small size.

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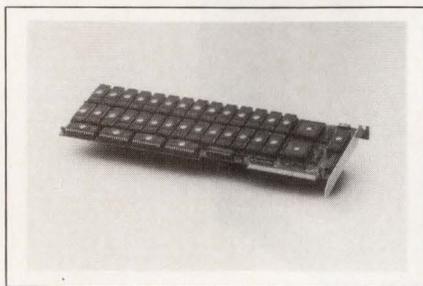
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provides hardware windowing, 19M-bps BitBlts (bit-block transfers), and fast drawing commands. For example, it performs area fills at a rate of 24M bps and draws lines at 2M pixels/sec. The TT786 comes with 512k bytes of video display memory, which typically supports a mixed text-and-graphics frame buffer of 2000x1000 pixels. You can simultaneously display 16 colors from a palette of 64 colors. The TT786 can drive an IBM EGA (Enhanced Graphics Adapter) or CGA (Color Graphics Adapter) monitor or can share a monitor with an existing IBM EGA or CGA card. Microsoft's Windows and Turbo Pascal Graphix software is currently being ported to the board. Reprogrammable logic-cell arrays on the board allow you to customize the TT786. Its programmable features include the locking of various configuration parameters, encrypted or barred access to memory or 82786 regis-

ters, interrupt vectoring, interception of PC-bus I/O or memory addresses, and control of the 82786's accelerated mode. £395 (50).

Tektite, 9 Coolhurst Rd, London N8 8EP, UK. Phone 01-341 2468. TLX 269441.

Circle No 359



STORAGE

- Disk-emulation boards provide solid-state storage
- IBM PC bus-compatible boards for harsh environments

The QPC-5211, QPC-5212, and

QPC-5213 disk-emulation boards are IBM PC bus-compatible, mass-storage devices. These solid-state-storage boards can operate in harsh environments, where vibration, shock, heat, or dust would interfere with the operation of floppy-disk or Winchester drives. The QPC-5211 holds as much as 2M bytes of PROM or EPROM or 1M byte of EEPROM. The QPC-5212 provides 512k bytes of CMOS RAM, as well as 1M byte of PROM or EPROM or 512k bytes of EEPROM. The QPC-5213 accommodates as much as 1M byte of CMOS RAM. All the RAM sockets on the QPC-5212 and QPC-5213 boards have built-in lithium batteries that provide nonvolatile data storage. Without any memory devices, the QPC-5211, -5212, and -5213 each costs \$495.

Qualogy Inc, 2241 Lundy Ave, San Jose, CA 95131. Phone (408) 434-5200. TLX 4993489.

Circle No 360

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KEMET® Electronics Corporation

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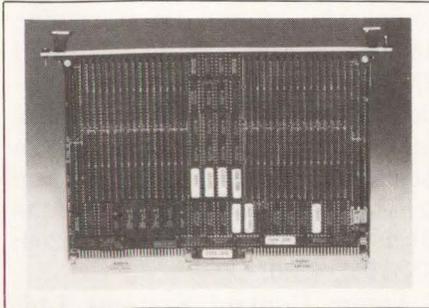


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KEMET® Electronics Corporation



MEMORY BOARD

- 16M bytes of dual-port dynamic RAM on one board
- Supports both Versabus and VME Bus interfaces

The VMEM-16MB is a dual-port VME Bus memory board that provides a full 16M bytes on one card and supports both the VME Bus and the Versabus interfaces. Utilizing 1M-bit dynamic-RAM chips, the dual-port memory ensures that each processor in a multiprocessor system has priority access through its local Versabus. The interprocessor

communication and I/O transfers take place over the VME Bus. The VME Bus's read-access time is 230 nsec; its write-access time is 180 nsec. The read-access time for the Versabus is 220 nsec; its write-access time is 200 nsec. The board has 32-bit data paths, and it performs 32-, 16- and 8-bit data transfers, so you can use it with almost any combination of processors and DMA devices on the VME Bus. \$8995.

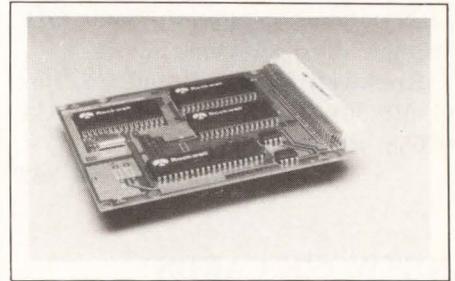
Dual Systems Corp, 2530 San Pablo Ave, Berkeley, CA 94702. Phone (415) 549-3854.

Circle No 361

MODEM BOARD

- Full-duplex synchronous operation to 14.4k bps
- 2W power consumption is typical

The R144DP is a low-power full-duplex synchronous modem board



for unconditioned or conditioned leased-line, 4-wire applications. It's capable of operating at 14.4k, 12k, 9.6k, 7.2k, and 4.8k bps. It consumes 2W typ and features full CCITT V.33 and V.29 compatibility, trellis-coded modulation, a parallel μ P bus interface that allows the host CPU to monitor and control features such as self-diagnostics, a CCITT V.24/RS-232C port, a dynamic receive range of 0 to 43 dBm, and TTL and CMOS compatibility. Two packaging options are available: a 3.94x4.73-in. module with a DIN connector and a 3.23x3.94-in. DIP module that can be placed di-

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rectly on the host system's pc board. DIN-connector version, \$400; DIP version, \$385. (1000).

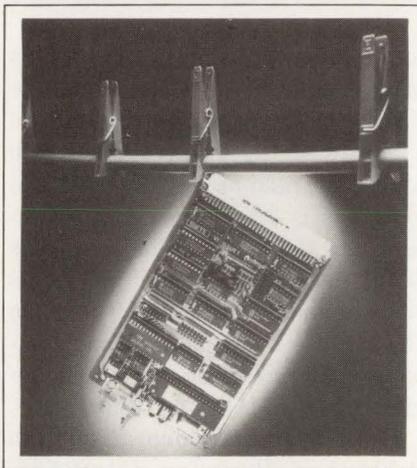
Rockwell International Co, Box C, MS 501-300, Newport Beach, CA 92658. Phone (714) 833-4700.

Circle No 362

NETWORK CARDS

- Operate as stand-alone or STE Bus-based Bitbus nodes
- Are optically isolated from the Bitbus network

The SNETS and SNETM are single-Eurocard boards that provide an interface between STE Bus systems and Bitbus networks. Both boards are based on Intel's 8044 Bitbus processor and can operate as Bitbus masters or slaves. The SNETS board operates as an STE Bus slave; an STE Bus CPU controls it via its I/O-mapped slave interface. The SNETM can operate as an STE Bus



master or as a stand-alone Bitbus node processor. In STE Bus master or stand-alone mode, commands sent via the Bitbus allow you to read or write to STE Bus or local I/O-port locations. As a result, you don't need to write firmware for the SNETM board for simple control applications. For stand-alone operation, the vendor provides an I/O connector with 16 digital lines, so

you can interface the board to the company's signal-conditioning boards. Both the SNETS and SNETM boards have optical isolation in the Bitbus data and transceiver control lines. By adding an isolated 5V power supply, you can achieve complete isolation from the Bitbus network. SNETS, £200; SNETM, £250.

Arcom Control Systems Ltd, Unit 8, Clifton Rd, Cambridge CB1 4WH, UK. Phone (0223) 242224. TLX 817114.

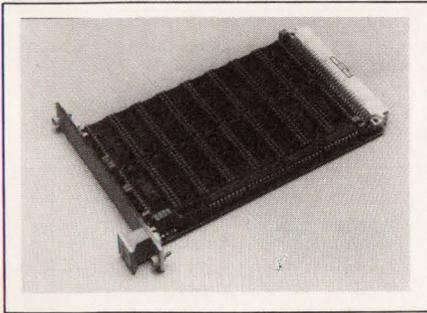
Circle No 363

RAM CARD

- Accepts 2M bytes of static RAM or ROM on a single Eurocard
- Allows separate RAM and ROM access times

The VMEM-S1 single-Eurocard VME Bus memory board has 16 32-pin sockets that are capable of

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holding as much as 2M bytes of static RAM or ROM. You can load the board with a combination of RAM and ROM as your application requires. The device-access times can range from 100 to 250 nsec, and the board is divided into two separate memory areas for which you can specify different access times. The board will accept RAM or ROM devices with capacities as high as 1M bit. The board makes provision for the battery backup of the static RAM. DM 990.

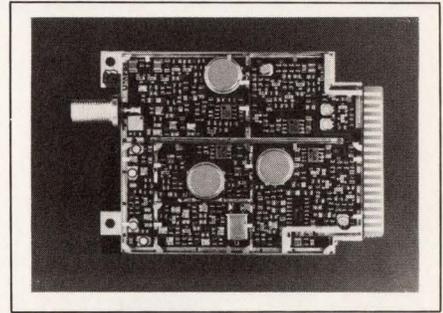
Pep Modular Computers GmbH,
Am Klosterwald 4, 8950 Kauf-

beuren, West Germany. Phone (08341) 8974. TLX 541233.

Circle No 364

Pep Modular Computers Inc,
600 N Bell Ave, Pittsburgh, PA 15106. Phone (412) 279-6661. TLX 6711521.

Circle No 365



NETWORK INTERFACE

- Provides RF portion for IBM's Personal System/2
- Module provides interface to the IBM PC network

The MHW10000 RF module provides the RF functions necessary for implementing a modem that's compatible with the IBM PC network and the IEEE-802.7 broadband specifications. The module is a full-duplex, continuous-phase, FSK transceiver that takes up 8 in² of space in your system. It plugs into the IBM PC Network Adapter card

in the IBM Personal System/2. The broadband approach to LANs permits video and security functions, as well as other broadband functions, to exist on the same cable. The unit uses T-14 (transmit) and J (receive) CATV (community-antenna TV) channels. \$275.

Motorola Inc, Semiconductor Products Sector, Box 52073, Phoenix, AZ 85018. Phone (602) 244-6394.

Circle No 366

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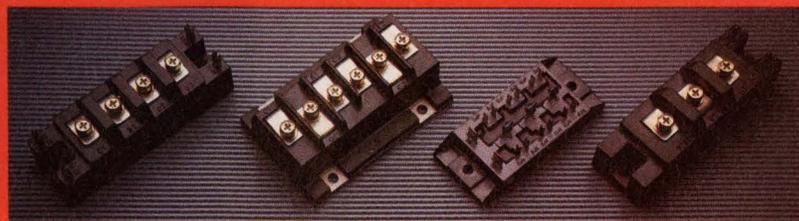
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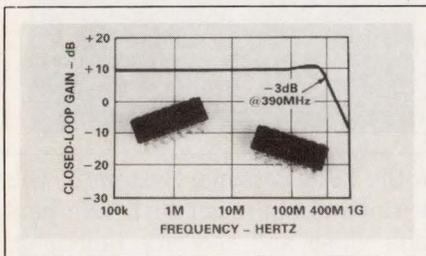
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- Settles to within $\pm 1\%$ in 12 nsec
- Full-power bandwidth is 82 MHz

The AD5539 is a monolithic, high-speed op amp that settles to within $\pm 1\%$ in 12 nsec. The device has a 1.4-GHz (typ) gain-bandwidth, a 600V/ μ sec slew rate, and an 82-MHz full-power bandwidth. It dissipates 550 mW when operating from the nominal ± 8 V power supply. A single capacitor makes the op amp unity-gain stable; gain settings of higher than five require no compensation. The dc performance is tested and guaranteed over temperature. Maximum respective J and S specs are 6 and 5 mV of input-offset voltage, 5 and 3 μ A of input-

offset current, and 40 and 25 μ A of bias current. The minimum open-loop gain is 47 dB, the minimum common-mode rejection ratio is 70 dB, and the input voltage noise is less than 4 nV/ $\sqrt{\text{Hz}}$. The amplifiers are available in 14-pin plastic or ceramic DIPs and are specified for the commercial or military temperature ranges, respectively. From \$1.65 (100).

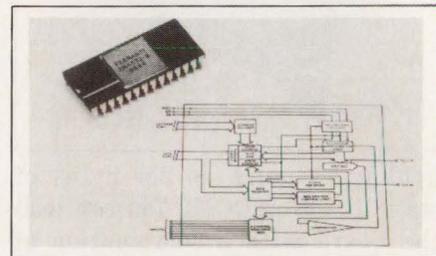
Analog Devices Inc, Box 9106, Norwood, MA 02062. Phone (617) 935-5565. TWX 710-394-6577.

Circle No 367

DATA ACQUISITION

- Converts eight bits in 20 μ sec
- Includes an 8-channel multiplexer

The ZN437 is a monolithic data-acquisition system that includes an 8-channel multiplexer, an 8-bit, successive-approximation A/D converter, an 8-word \times 8-bit RAM, 3-state output buffers, address latches, μ P control logic, and a clock predivider. It converts in 20 μ sec, and you can



program it to operate in one of four modes: single or continuous conversion on a designated channel, or single or continuous conversion on each of the eight channels. A clock predivider allows the device to operate from the clock signal of a μ P at frequencies as high as 4 MHz. The on-chip RAM stores the result of each channel's conversion, and the double-buffered latches permit a processor to read the data at any time. The device comes in a 28-pin plastic DIP. The ZN437-E7, with ± 1 -LSB linearity, \$10.51; the ZN437E-8, with ± 0.5 -LSB linearity, \$14.51 (1000).

Ferranti Semiconductors, 87 Modular Ave, Commack, NY 11725. Phone (516) 543-0200.

Circle No 368

DATA ACQUISITION

- 33k-sample/sec throughput rate
- 1-in² LCC package

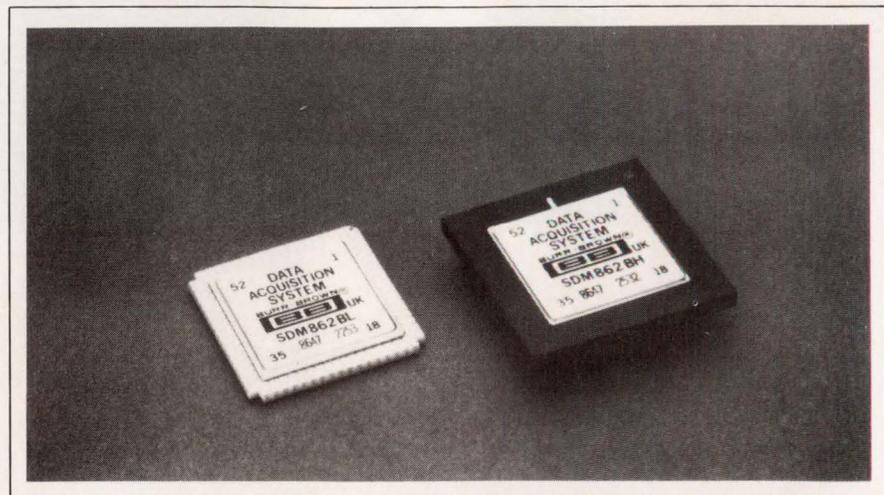
The SDM862 data-acquisition system includes a 16-channel input multiplexer (the SDM863 has an 8-channel differential mux); a jumper-selectable instrumentation amplifier with gains of 1, 10, and 100; a sample/hold amplifier; and a 12-bit A/D converter with a μ P interface and 3-state output buffers. Each device provides a maximum throughput rate of 45 kHz for 8-bit accuracy or 33 kHz for 12-bit accuracy. External connections select an input-voltage range of 0 ± 5 V, 0 ± 10 V, or ± 5 V. Integral-linearity grades include 0.024% and 0.012% (full-scale resolution). The devices

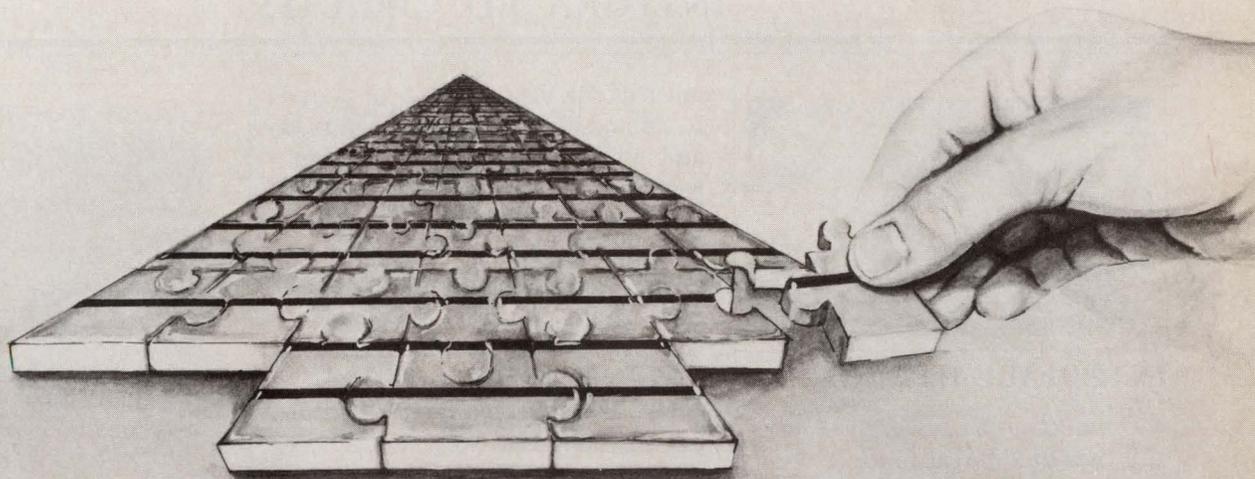
come in 68-lead, 1.1-in² grid arrays or in 1-in² ceramic LCCs and are specified for the commercial, industrial, or military temperature ranges. From \$103 (100). Delivery,

stock to eight weeks.

Burr-Brown Corp, Box 11400, Tucson, AZ 85734. Phone (602) 746-1111. TWX 910-952-1111.

Circle No 369





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FOR COMPLETE INFORMATION: Write or telephone: Edward E. Grazda, Director of Education • 17100 Norwalk Blvd., Suite 116, Cerritos, CA 90710-2750 • (213) 402-1610
Telex: 650 290 5828 (WUI) • FAX: 213 402 8814

BUSCON/87-East

The Bus Board Users Show & Conference

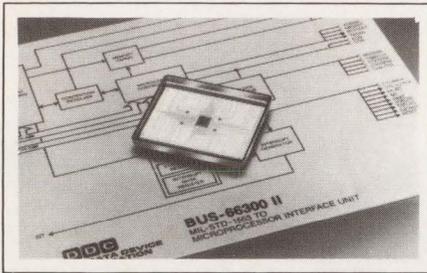
October 5-7, 1987

Royal Plaza Hotel

Marlborough, Massachusetts

CIRCLE NO 135

INTEGRATED CIRCUITS



INTERFACE HYBRID

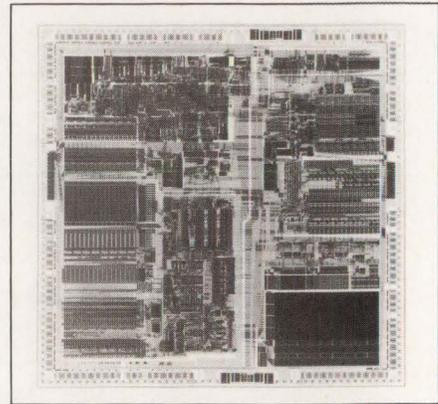
- Connects a MIL-STD-1553 terminal and a host CPU
- Screened per MIL-STD-883

The hybrid BUS-66300 II contains a chip that provides the complete 1750-to-1553 interface, allowing the device to act as an intermediary between a MIL-STD-1553 terminal and a host CPU. The host preloads 1553 control-data information, and the interface then provides terminal control, data-transfer timing and control, and response handling. Ongoing 1553 I/O is almost transparent because the hybrid operates with as

much as 64k bytes \times 16 bits of shared RAM and because the host can read and write 1553 messages concurrently with 1553 terminal activity (the hybrid handles memory contention automatically). The device operates over the military temperature range and is available in versions screened to MIL-STD-883. \$995. Delivery, stock to 12 weeks.

ILC Data Device Corp, 105 Wilbur Pl, Bohemia, NY 11716. Phone (516) 567-5600. TWX 510-228-7324.

Circle No 370



32-BIT μ P

- 4G-byte virtual and physical address spaces
- Thirty-two 32-bit general-purpose registers

The μ PD70632 (V70) is a multitasking, virtual-memory, CMOS μ P with a 32-bit addressing capacity, 32 general-purpose 32-bit registers, 24

privileged registers, and a 32-bit data bus that operates at 20 MHz. The chip uses a 2-clock bus cycle and 6-stage pipeline to achieve a peak performance of 6.6 MIPS and a peak data-transfer rate of 40M bytes/sec. The V70 supports the Itron operating system and the Unix System V. It includes an emulation mode that executes all V20/V30 and V40/V50 software. Other features include demand-paged memory management with 4G bytes of virtual space for

SOT-23 TRANSISTORS AND DIODES FOR SURFACE-MOUNT APPLICATIONS.

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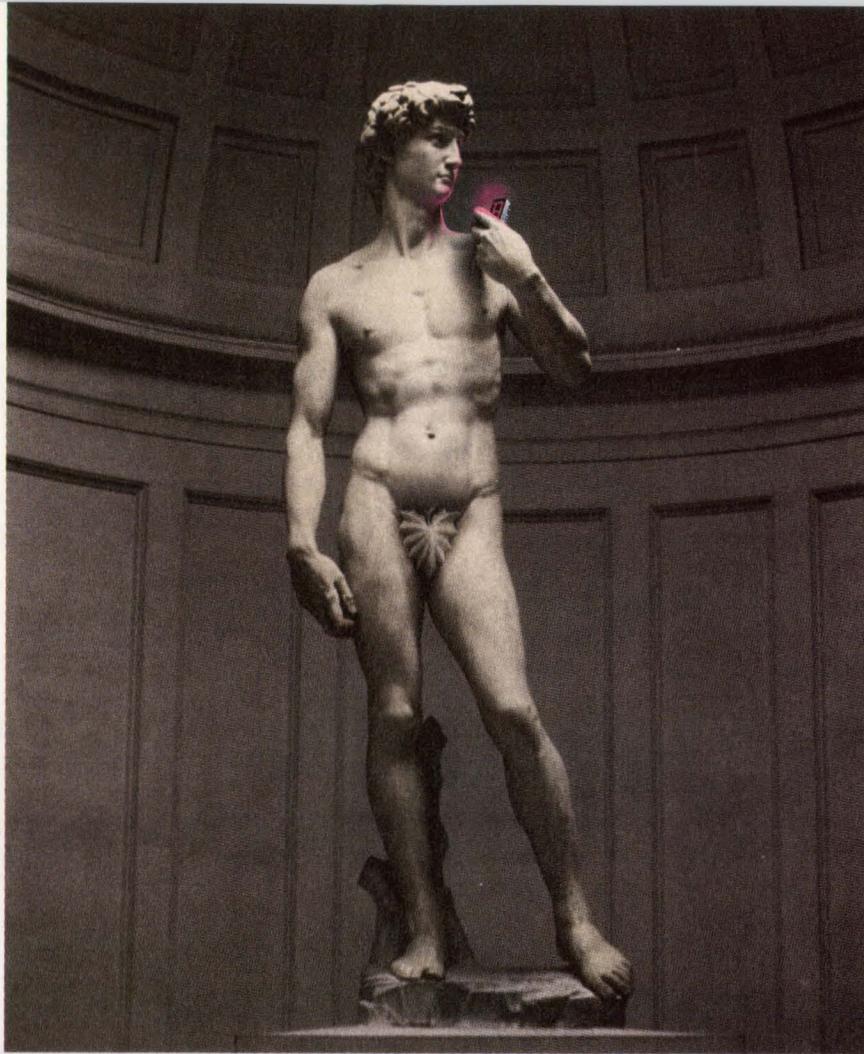
- Transistors: NPN and PNP general purpose, medium power, switching, high voltage and Darlington.
- Diodes: high-speed switching (single and dual), varactor, Schottky and Zener.
- Ferranti's optimum profile is designed for both hybrid assembly utilizing solder paste and surface mounting using adhesives.
- All devices are molded in silicone plastic to permit higher temperature performance.
- Ferranti has been supplying SOT-23's for over twelve years and is constantly increasing its production capability.

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612-290-1071; Sweden, Stockholm, 08-520720; Belgium, Antwerp, (0) 3/230-45•09 or 14.

CIRCLE NO 44



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INTEGRATED CIRCUITS

each task, IEEE 754 floating-point operations, a system-debug facility, and task management and protection. The chip measures 14.35×14.24 mm and comes in a 132-pin ceramic programmable gain amplifier. 20-MHz version in sample quantities, \$650. Production quantities will be available in August.

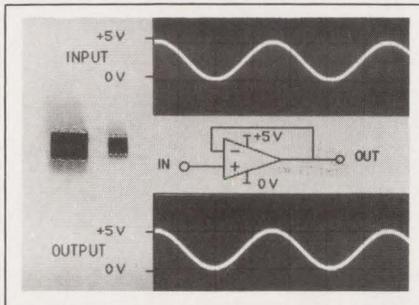
NEC Electronics Inc, Box 7241, Mountain View, CA 94039. Phone (415) 960-6000. TWX 910-379-6985.

Circle No 371

CMOS OP AMP

- Output swings rail to rail
- Draws 250 μ A from 5V supply

According to the company, the ALD 1701 is the industry's first precision CMOS op amp whose input- and output-signal ranges include the power-supply voltages (rails). The device operates from a 2 to 12V single supply or from ± 1 to ± 6 V



dual supplies; guaranteed specs are based on a 5V supply. Typical current from a 5V supply is 250 μ A. Specs include a 0.7-MHz unity-gain bandwidth, a 0.7V/ μ sec slew rate, a 1-pA input bias current (30 pA max), and internal compensation for unity-gain stability. The short-circuit-protected output can deliver 1 mA to a 10-k Ω load or can drive a 100-pF load in the unity-gain configuration. The typical open-loop gain is 120 dB. The minimum gain with a 100-k Ω load is 89.5 dB. The maximum offset-voltage grades include 0.9, 2.0, 4.5, and 10 mV. The ampli-

fiers are available in plastic or ceramic DIPs, SOIC (small outline IC) packages, or as die. From \$1.64 (100).

Advanced Linear Devices Inc, 1030 W Maude Ave, Suite 501, Sunnyvale, CA 94086. Phone (408) 720-8737. TWX 510-100-6588.

Circle No 372

D/A CONVERTER

- 9-bit resolution
- 125-MHz update rate

The IDT75C19/29 is a CMOS 9-bit video D/A converter. The device updates at 125 MHz, and it drives a 75 Ω load to video levels with a resolution exceeding 1280×1024 pixels. The IDT75C19 has ECL-compatible inputs; the IDT75C29 has TTL-compatible inputs. The device's segmented architecture decodes the six MSBs of input data into 64 coarse output levels. The remaining three

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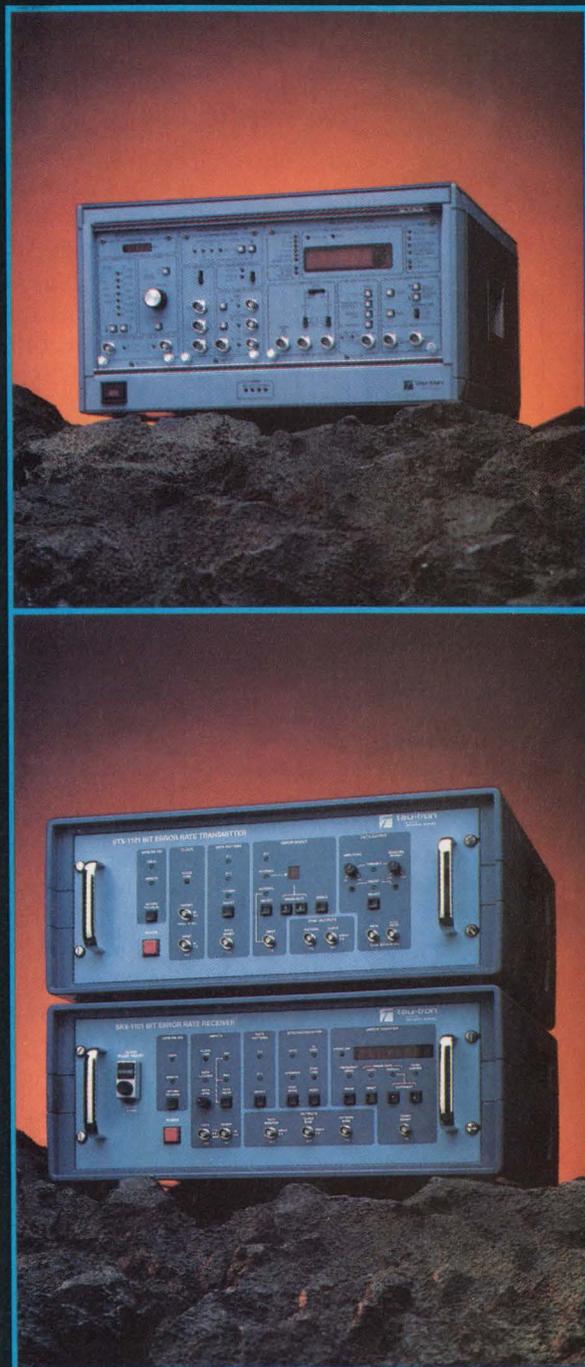
BERTS-325C

The BERTS-325C provides accurate, quantitative, end-to-end bit error rate testing with standard NRZ or RZ codes for 1kHz to 325 MHz (BERTS-650 is available for applications up to 650 MHz). Tau-tron's TMI® family offers custom instrumentation with the BERTS-325C to meet your specific needs at off-the-shelf prices. Over 10 different plug-in modules for signal generation, conditioning and detection are available. Tau-tron's commitment to the TMI® modular design concept precludes obsolescence and is ideal for satellite, fiberoptic, high-density digital tape, digital radio and digital multiplexer applications. For full-system integration capabilities, a GPIB (IEEE-448) Interface is included to control all relevant front panel functions.

BERTS-1150

The BERTS-1150 is an advanced technology bit error rate test set designed to evaluate the performance of high speed lasers, fiberoptic links, satellite links and components such as GaAs logic devices with the frequency range of 90 to 1150 MHz. Consisting of Tau-tron's highly stable STX-1101 Transmitter and SRX-1101 Receiver, the BERTS-1150 incorporates many user features such as three selectable bit patterns and internal/external error inject which truly makes it a powerful, general purpose test set. The BERTS-1150 measures total bit errors, bit error rates, or clock frequency and may be remotely controlled through either a GPIB or RS-232C interface. The BERTS-1150 will also provide hard copies of measurement data through either of these interfaces.

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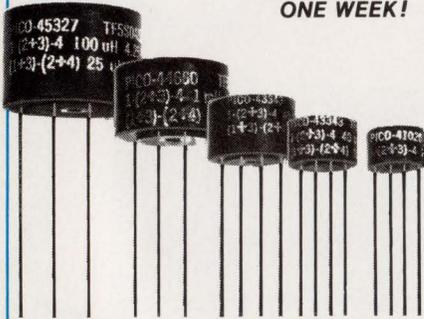
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CIRCLE NO 46

INTEGRATED CIRCUITS

LSBs drive eight appropriately weighted current switches whose total contribution is $\frac{1}{64}$ of full scale. The device then sums MSB and LSB currents at the output to produce 512 levels. These output levels correspond to the RS-343A monitor standard, allowing a simplified connection to a graphics CRT. The device comes in a 24-pin hermetic DIP, a 28-pin LCC, or a 24-pin, 300-mil plastic DIP. Commercial grade in ceramic DIP, \$38.50 (100).

Integrated Device Technology, Box 58015, Santa Clara, CA 95052. Phone (408) 727-6116. TWX 910-338-2070.

Circle No 373

DMA CONTROLLER

- Has four independent 8M-byte/sec DMA channels
- Supports command-block and data chaining

The SAB82257 16-bit DMA controller interfaces directly to 80286, 8086/186, and 8088/188 μ Ps. In addition, it operates in a remote mode that lets you use it with other processors. The controller has four independent DMA channels, capable of data transfer speeds as high as 8M bytes/sec with an 8-MHz clock in 80286 systems, or 4M bytes/sec with an 8-MHz clock in 8086/186 systems. It supports 16M-byte memory and I/O address spaces, and can transfer a maximum block size of 16M bytes. You can chain command blocks for any channel so that they are executed sequentially, and you can include conditional and unconditional stop and jump commands to create complex DMA sequences. Data chaining is also possible, allowing you to build a destination data block from multiple-source data blocks, or to break up one source block into multiple destination blocks. Where physical and logical bus widths differ, the DMA controller automatically assembles or disassembles bytes into words, or words into bytes as necessary. It also trans-

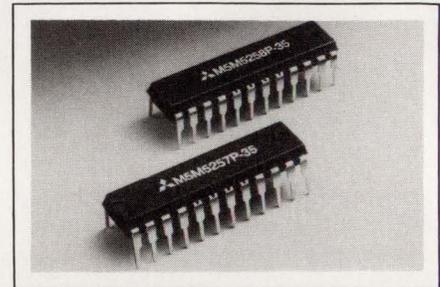
forms bytes into words (and vice versa) when the logical bus widths of the source and the destination differ. DM 35 to DM 50.

Siemens AG, Zentralstelle für Information, Postfach 103, 8000 Munich 1, West Germany. Phone (089) 2340. TLX 5210025.

Circle No 374

Siemens Components Inc, 186 Wood Ave S, Iselin, NJ 08803. Phone (201) 321-4842.

Circle No 375



STATIC RAMs

- 35-nsec access time
- 256k-bit organization

Models M5M5257 (256k \times 1 bit) and M5M5258 (64k \times 4 bit) each combine silicon-gate CMOS logic with an NMOS memory array. The devices spec 35-, 45-, or 55-nsec access times. They are the fastest 256k-bit static RAMs available, according to the manufacturer. The devices come in 24-pin, 300-mil plastic DIPs or in plastic surface-mount packages. 35-nsec M5M5257P in a DIP, \$142; 35-nsec M5M5258P in a DIP, \$152 (100).

Mitsubishi Electronics America Inc, Semiconductor Div, 1050 E Arques Ave, Sunnyvale, CA 94086. Phone (408) 730-5900.

Circle No 376

DRIVER IC

- 0.7V (typ) output saturation voltage at full load
- Protected against supply line and load transients

The 5-pin L9350 driver IC can deliver as much as 600 mA, and has a

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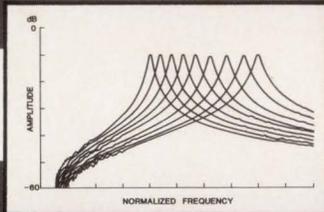


Sierra Power Systems

Division of Valor Electronics, Inc.

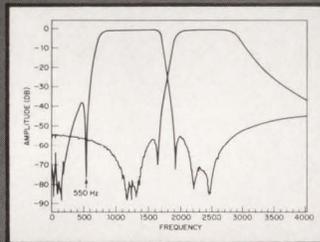
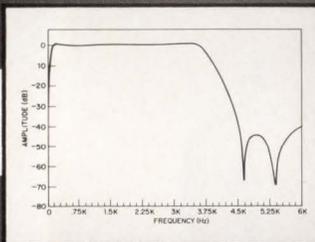
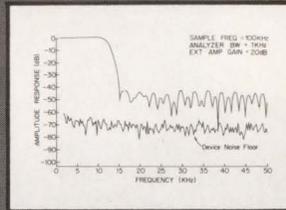
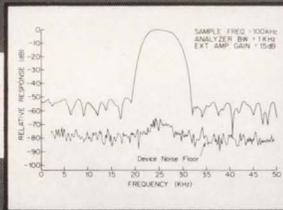


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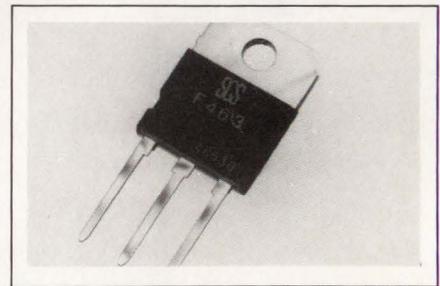
typical output saturation voltage of 0.7V at full rated output current. The driver's control input is TTL-compatible. Targeted at automotive applications, the driver operates over a supply voltage range from 4.5 to 24V. The device can withstand voltage transients of $\pm 120V$, 60V load-dump transients, and battery reversals on its power-supply input. The output stage is protected against short circuits to either supply, and against $\pm 60V$ transients. An additional safety feature ensures that the output is turned off if the control input or supply ground is disconnected. \$1.80 (100,000).

SGS Microelettronica SpA, Via C Olivetti 2, 20041 Agrate Brianza, Italy. Phone (039) 65551. TLX 330131.

Circle No 377

SGS Semiconductor Corp, 1000 E Bell Rd, Phoenix, AZ 85022. Phone (602) 867-6100. TLX 249976.

Circle No 378



POWER TRANSISTORS

- 1000V blocking voltage
- 20A peak current

The SGSF463 (plastic SOT-93 package) and the SGSF563 (TO-3 package) are fast npn power transistors suitable for use in switching supplies rated at 200W and higher. The transistors offer 1000V blocking voltage, 12A continuous-current operation, and a 20A peak current. Typical inductive fall times are 80 nsec at 100°C and 40 nsec at 25°C. \$0.98 (1000).

SGS Semiconductor Corp, 1000 E Bell Rd, Phoenix, AZ 85022. Phone (602) 867-6100. TLX 249976.

Circle No 379

NEW
Powermag A1500.
Packs 1500 Watts of
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Five volts of regulated DC power at up to 300 Amps and failsafe redundancy! That's what the new Powermag A1500 Switching Power Supply delivers.

This 5" x 8" x 11" high power-density 1500-Watt unit from Advance Power Supplies provides 3.4 Watts per cubic inch from either 110V or 220V nominal, 47 to 440 Hz input. It's perfect for systems using large amounts of solid-state mass storage.

Virtually any number of Powermag units can be interconnected to provide parallel redundancy and meet heavy power demands. Current-sharing capability is built-in, so each unit shares the load equally. Should one unit fail, the others will automatically redistribute and assume the load (up to their rated capacities). And the Powermag meets major international safety and RFI requirements.

Standard features include electronic soft-start; self-diagnostics; over-current, overvoltage and overtemperature protection; selectable dual-input voltage;

local and remote sensing; and full-cycle holdup. A variety of signal facilities and optional output voltages (2V, 12V, 24V, 48V) make the Powermag A1500 one of the most versatile power supplies available.

For complete details on the high-power, affordably priced Powermag A1500, contact your Advance Power Supplies representative. Or call (216) 349-0755.

Advance Power Supplies
32111 Aurora Road
Solon, OH 44139

 **ADVANCE
POWER SUPPLIES**

CIRCLE NO 12

COMPARATORS

- 12-bit accuracy
- Pin-compatible with the CMP-05 and RM4805

The SE/NE5105A is a precision, high-speed, TTL-compatible comparator with 12-bit accuracy. A standard-grade version, the SE/NE5105, is also available. Both are pin and function compatible with the CMP-05 from Precision Monolithics and with the RM4805 from Raytheon. Based on a proprietary design that employs a high-speed bipolar process, these comparators are suitable for use in 12-bit successive-approximation A/D converters and in precision zero-crossing detectors. The SE/NE5105A specs a 100- μ V input-offset voltage, a 3-nA input-offset current, a 36-nsec propagation delay with 1.2-mV of overdrive, 26k of gain, and 100-mW of power dissipation. These parameters remain stable over the commercial,

military, or automotive (-40 to +85°C) temperature ranges. The input-offset voltage drift is 1.5 μ V/°C. The latched outputs can drive 10 TTL gates, and a logic 1 on the latch-enable input preserves the existing output-logic level, regardless of changes in the input-signal level. The devices are available in 8-pin DIPs or in SOIC (small-outline IC) packages. SE/NE5105, from \$2.00; SE/NE5105A, from \$4.75 (100).

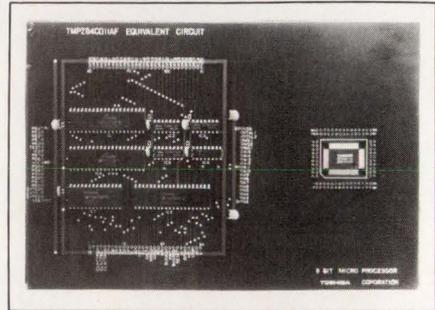
Signetics Corp., Box 3409, Sunnyvale, CA 94088. Phone (408) 991-2000.

Circle No 380

μ P-SYSTEM ASIC

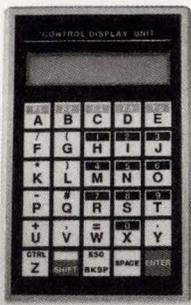
- Z80 μ P plus peripherals on one chip
- 6-MHz operation

Suited for data-communications applications, the TMPZ84C01XAX series of application-specific standard



products integrates a Z80 μ P and various groups of peripheral circuits on a monolithic CMOS chip. The TMPZ84C011AF comes in a 100-pin flat package and includes the Z80, a clock-generator controller, a counter-timer, and five 8-bit parallel I/O ports. Provided in an 84-pin plastic leaded chip carrier, the TMPZ84C013AT includes the Z80, a clock-generator controller, a clock-timer, a serial-I/O controller, and a watchdog timer. The TMPZ84C015AF is offered in a 100-pin flat package and incorporates a clock-generator controller, a count-

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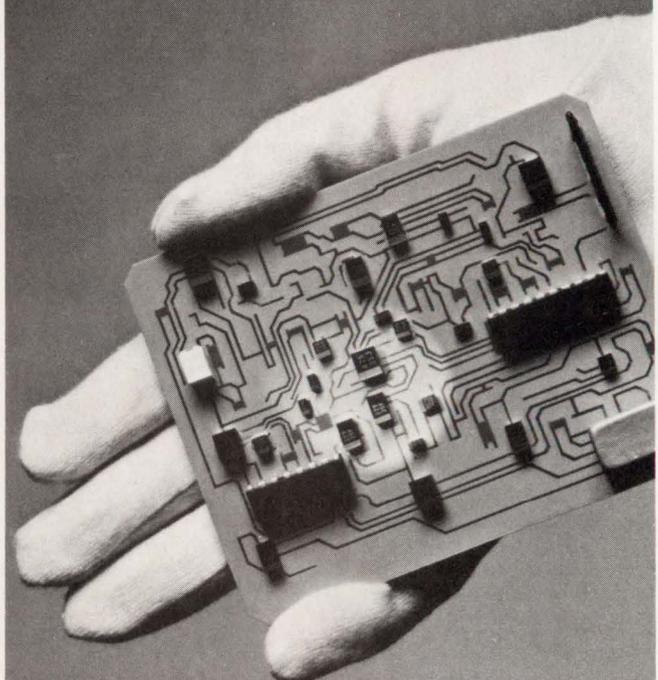
- 32 Character LCD
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- 30 Alphanumeric Keys
- Custom Graphics Available

Termiflex has taken its years of experience and leadership in control/display units (CDU) and produced the ST/32. This rugged, versatile CDU is available for overnight delivery.



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INTEGRATED CIRCUITS

er-timer, a watchdog timer, and parallel and serial I/Os. Each device is available in a 4- or a 6-MHz version. Prices for the 4-MHz versions of each are 11AF, \$15; 13AT, \$16; and 15AF, \$17 (100).

Toshiba America Inc, 2692 Dow Ave, Tustin, CA 92680. Phone local office.

Circle No 381

MULTICALL CHIP

- Supports 6-person conference calls
- Permits two simultaneous calls with three people each

The S3547 is a conference-trunk circuit that can accommodate a single conference telephone call with as many as six callers, or two simultaneous calls with as many as three callers each. This monolithic MOS chip supports all-digital, PABX, and key systems. AGC circuits maintain

a consistent, audible signal level; the chip's PCM highway interface implements the conference trunk without an additional codec or op amp. Other features include a serial T1 interface that supports the verbal exchange between callers, an 8-bit interface that allows control by a μ P, and a 500-Hz tone generator, which can be used to indicate that an additional speaker has joined the conference call. \$17.95 (1000).

Gould Inc, Semiconductor Div, 3800 Homestead Rd, Santa Clara, CA 95051. Phone (408) 246-0330.

Circle No 382

FIFO MEMORIES

- Shift-frequency operation as high as 35 MHz
- 64-byte \times 8- or 64-byte \times 9-bit organization

The CY7C408 (64 bytes \times 8 bits) and the CY7C409 (64 bytes \times 9 bits) are

CMOS FIFO memories that can operate with shift frequencies as high as 35 MHz. You can cascade them serially. Each has a dual-port-RAM architecture plus a half-full output and an almost full (or empty) output; these signals let the external systems transmit or receive new data without requiring the time for an empty location to propagate from the output to the input of an initially full FIFO. The devices are available in 28-pin plastic or ceramic DIPs, specified for the commercial range, and in 28-pin ceramic DIPs and LCCs, specified for the military temperature range. From \$56.50 (100).

Cypress Semiconductor Corp, 3901 N First St, San Jose, CA 95134. Phone (408) 943-2666.

Circle No 383

The only thing faster costs millions more.

The ST-100 32-bit array processor gives your host the power of a supercomputer. So you can get 100 megaflops of computing capability from your current mainframe or superminicomputer. And get Cray 1 speed for less than \$300,000.

Not surprisingly, this kind of price-performance relationship makes the ST-100 an ideal companion for even the fastest host.

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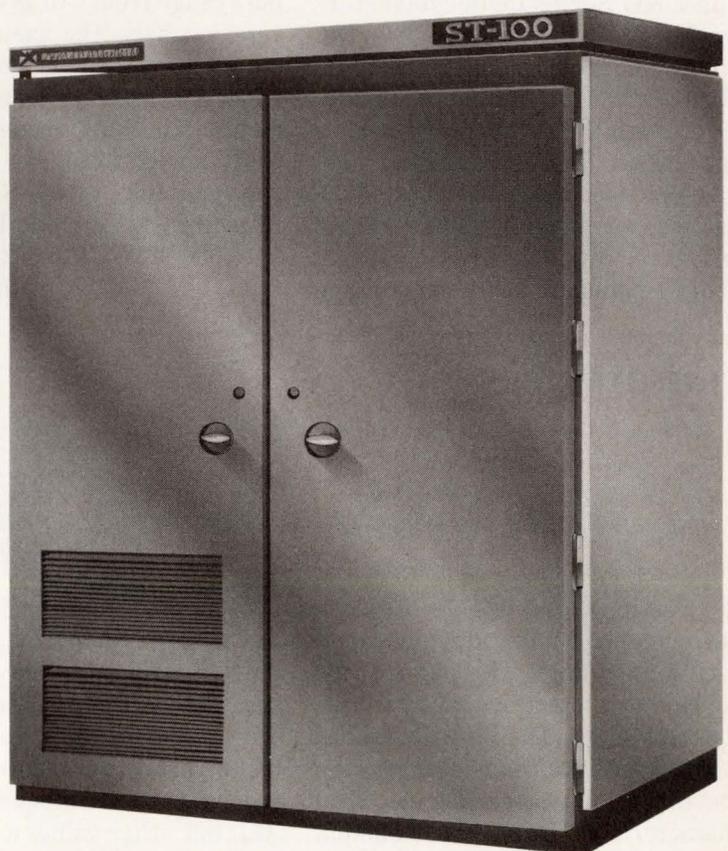
If you need the power of a supercomputer but don't have a super budget, call us today at (703) 689-4400.

And get super speed and reliability at a super price.



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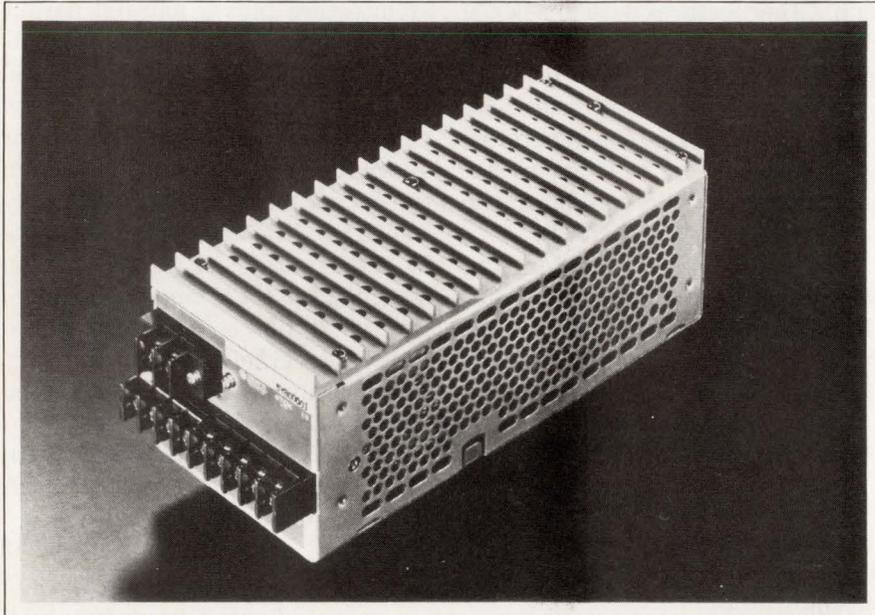
515 Shaw Road, Sterling, Virginia 22170



CIRCLE NO 50

NEW PRODUCTS

COMPONENTS & POWER SUPPLIES



DC/DC CONVERTERS

- 300-kHz switching frequency
- Offer 80% efficiency

The ERD Series dc/dc converters employ FETs switching at 300 kHz. They do not require an external cold plate or derating to an upper limit of 50°C. Both the 60 and 150W models operate at 80% efficiencies. Features include adjustable voltage output, remote error sensing, remote on/off, rectangular current limiting to drive nonlinear loads, overvoltage

protection, an LED power indicator, and a built-in EMI filter. Ten models in the 60W series have inputs of 24 and 48V, and their outputs range from 5 to 48V. The 150W versions have the same input and output specs. All units meet UL 478 and CSA C22.1-154 safety requirements. The 60W model, \$160; the 150W model, \$225.

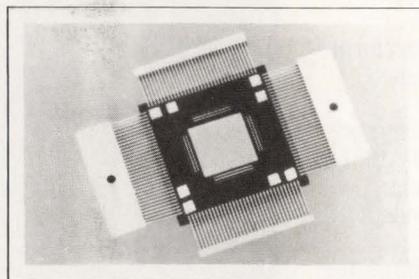
Kepeco Inc, 131-38 Sanford Ave, Flushing, NY 11352. Phone (718) 461-7000. TWX 710-582-2631.

Circle No 384

CHIP CARRIERS

- Feature microstrip signal lines with controlled impedance
- Die bonding directly to a heat sink minimizes heat problems

These chip carriers are available in two versions: Phip (polyimide high performance) and Phil (polyimide high-lead count). The devices use polyimide dielectric, which has a constant of 3.8. The Phip device has microstrip signal lines that provide controlled impedance. Its electrical characteristics include a maximum capacitance of 1 pF, an inductance of

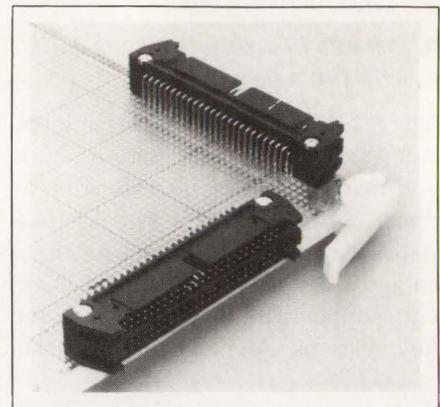


2 nH, and a resistance of 30 mΩ max. The carriers' design lets you bond the die directly to a heat sink to control heat problems. The standard controlled impedance equals 50Ω, but other values are available. The Phil units have the same 0.025-

in. pitch but without the controlled impedance feature. A kit is available that contains five 132-pin Phip and five 132-pin Phil devices and costs \$495.

Augat Microtec, 2520 Turquoise Circle, Newbury Park, CA 91320. Phone (805) 498-9643.

Circle No 385



HEADERS

- Pins shielded on all sides for contact protection
- Bodies rated 94V-0 UL

These double-stacked, right-angle headers provide a means of increasing board density while maintaining a 0.1-in. grid spacing. Available with long or short lock/eject ears, they come in position sizes ranging from dual 10 to dual 64. The contacts are made of a copper-based alloy with 50 μin. of nickel plating all over and 20 μin. of gold at the plug area. The drawn pins are shielded on all four sides for polarization and contact protection. Its moldings are glass-filled polyester with a 94V-0 UL rating. Glass-filled polyester polarizing keys are also available. A 50-position device, \$3.72 (1000).

Carrot Components Corp, 750 W Ventura Blvd, Camarillo, CA 93010. Phone (805) 484-0540. TWX 910-366-1237.

Circle No 386

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The Pulse of Industry
21541 Blythe St.
Canoga Park, CA 91304



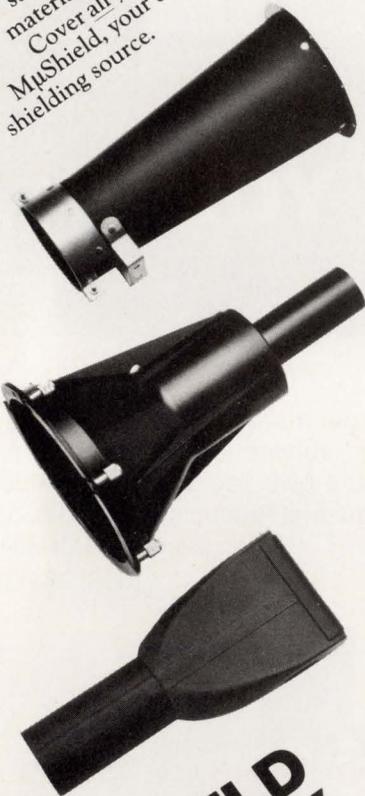
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MuShield offers you more magnetic shielding choices than any other manufacturer.

We design and build custom shields for electron microscopes, CAT and PET scan machines, computer terminals, and a host of other applications.

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103 Madison St.,
P.O. Box W
Malden, MA 02148
Tel. 617-321-4410

CIRCLE NO 51

COMPONENTS & POWER SUPPLIES



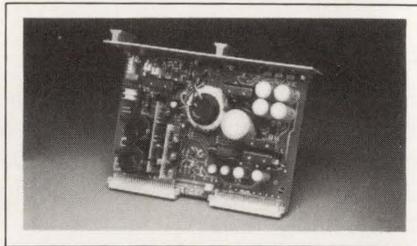
DC/DC CONVERTERS

- Feature 2:1 input voltage range
- Efficiency ranges to 82%

The Series 730 25W dc/dc converters feature input voltage ranges of 9 to 18V, 18 to 36V, and 36 to 72V. Its output combinations are 5 and $\pm 12V$, 5 and $\pm 15V$, and ± 5 and $\pm 12V$. All units have $\pm 0.5\%$ line regulation, $\pm 1\%$ load regulation, and a TTL-compatible remote on/off control input. Its efficiency can reach 82%, and voltage accuracy equals $\pm 1\%$. Each model includes an input filter to minimize reflected input ripple current. Overvoltage and overcurrent protection are standard on all models. The housing features a 6-sided shield to minimize EMI/RFI problems. \$179. Delivery, stock to six weeks ARO.

Power General, Box 189, Canton, MA 02021. Phone (617) 828-6216.

Circle No 387



POWER SUPPLY

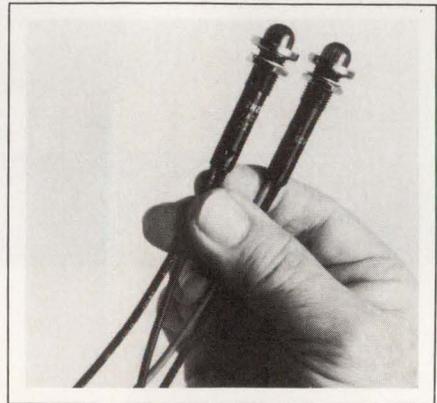
- Compatible with VME Bus
- Panel indicators monitor critical parameters

The VE100 Series 100W, double-height Eurocard-size switching power supply is plug-in compatible with the VME Bus. The supply is

available with either ac or dc inputs. Front-panel LEDs monitor power-on, overvoltage protection, and power-fail detect operation. The ac power switch is also front-panel mounted for easy access. The outputs are 5V dc at 1.8 to 9A, and $\pm 12V$ dc at 0.05 to 2A. All outputs have a 10% adjustment range. The Series includes an onboard DIN connector and features wide-input switcher technology—automatic 90 to 250V ac or 100 to 350V dc (no taps, straps, or jumpers necessary). \$184 (100). Delivery, six weeks ARO.

Converter Concepts Inc, Industrial Parkway, Pardeeville, WI 53954. Phone (800) 253-5227; in WI, (608) 429-2144.

Circle No 388

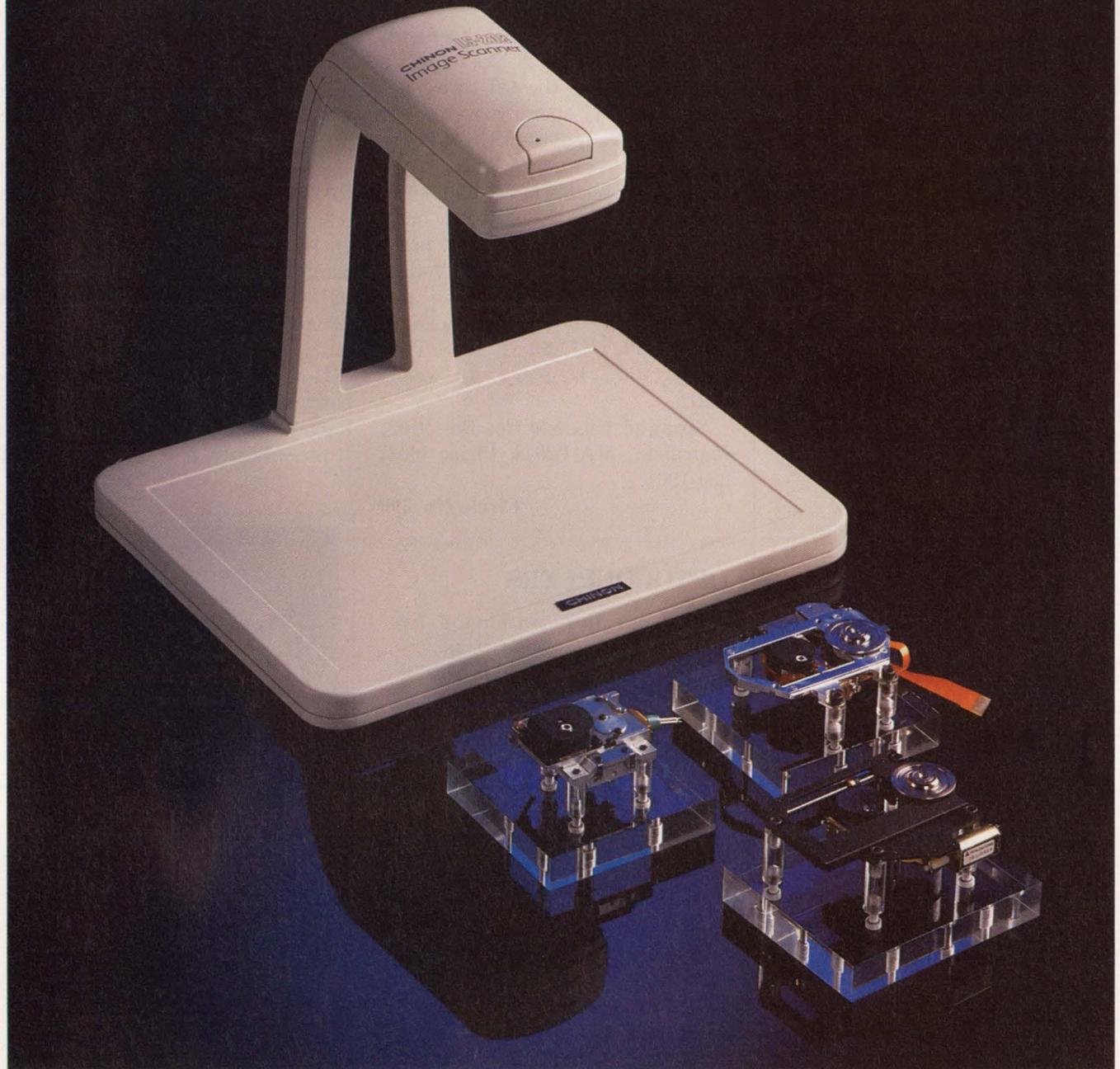


INDICATOR LAMPS

- Use two O-rings for total seal
- Available with neon lamp and LED-type light sources

The Series 6000 indicators feature two Buna-N O-rings for maximum sealing. One is located inside the indicator bezel between the lens and the housing, and the other sits in a groove in the housing. The inside ring keeps liquid out of the light; the ring under the bezel compresses as you install the indicator in the panel and forms a liquid-tight seal between the light and the panel. The catalog models use neon lamps for 125 or 250V operation in red, amber, and green, as well as a built-in current-limiting resistor. LED

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can only accept a single sheet fed through the unit. It is also extremely compact and lightweight, and is designed to set new standards of cost-effectiveness.

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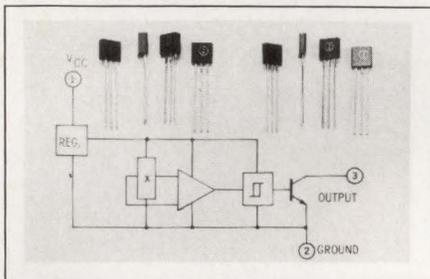
Chinon America, Inc., 6374 Arizona Circle
Los Angeles, CA 90045 (213) 216-7611 FAX: (213) 216-7646

COMPONENTS & POWER SUPPLIES

versions for 12 or 24V operation, which feature both a current-limiting resistor and a protective diode, are also available. Neon and LED models, \$1.39 and \$1.77 (1000), respectively.

Industrial Devices Inc., 7 Hudson Ave, Edgewater, NJ 07020. Phone (201) 224-4700.

Circle No 389



LATCHES

- Accommodate brushless dc motor control applications
- Available in surface-mount type packages

Small magnets switch the UGN-3077 and UGS-3077 commutation sensors. The sensors have a symmetrical duty cycle required for control of brushless dc motors. The open-collector output turns on as the strength of the magnetic field perpendicular to the chip passes the On threshold. It stays on (satu-

rated) until the magnetic flux density of equal strength but opposite polarity crosses the Off threshold. The UGN-3077 operates over a -20 to $+125^{\circ}\text{C}$ range; the UGS-3077 operates over -40 to $+125^{\circ}\text{C}$. Both types are available in two 3-pin plastic packages—a 60-mil-thick magnetically optimized U-shaped package and an 80-mil thick T-shaped package. The two units are also available in a SOT-89 package. UGN-3077 T/U, \$0.81; UGS T/U, \$1.26 (100). Delivery, 10 weeks ARO.

Sprague Electric Co., Box 9102, Mansfield, MA 02048. Phone (603) 224-1961.

Circle No 390

OPTOCOUPLERS

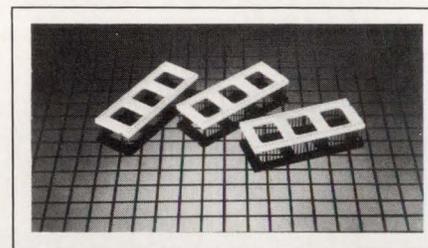
- Designed for high isolation, low input-current applications
- TTL- and CMOS-compatible units

The HCPL-2200 optocouplers are available in single- and dual-channel versions and are designed for high isolation, low input-current applications. The HCPL-2211 and HCPL-2212 single-channel 8-pin units have a $5000\text{ V}/\mu\text{sec}$ CMR. The HCPL-2232 dual-channel unit also has a $5000\text{ V}/\mu\text{sec}$ CMR. All three devices

include a Schmitt trigger and a totem-pole output, require only 1.8 mA of input current, and operate on supply voltages of 4.5 to 20V. The TTL- and CMOS-compatible units spec a 300-nsec propagation delay so they can handle 5M-baud data rates (the delay figure applies over the entire -40 to $+85^{\circ}\text{C}$ operating range). HCPL-2211 and HCPL-2212, \$4.37; HCPL-2232, \$7.43 (2500). Delivery, 8 to 10 weeks ARO.

Hewlett-Packard Co., 1820 Embarcadero Rd, Palo Alto, CA 94303. Phone local office.

Circle No 391



DIP SOCKETS

- Designed for ICs with 0.07-in. lead spacings
- Feature gold-plated inner contact

The Series ISO low-insertion-force shrink-DIP sockets are designed to accommodate IC packages with

FREE SOLUTIONS TO HAIRY LED PROBLEMS

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IDI Industrial Devices Inc., Edgewater, NJ 07020
 Telephone: (201) 224-4700

CIRCLE NO 52

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Only one logic timing analyzer slices nanoseconds into 10 perfect parts.

Take a deep breath and brace yourself. Because the logic analyzer you loved last year isn't going to cut it from this moment on.

Outlook Technology introduces the T-100. With clock speeds up to 2 GHz, new measurement techniques and its 100 psec resolution capability, this device is so sophisticated it will change forever the way you think about logic timing analysis.

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Each technique is thoroughly discussed, with screen displays, in our full color brochure. The patterns you can

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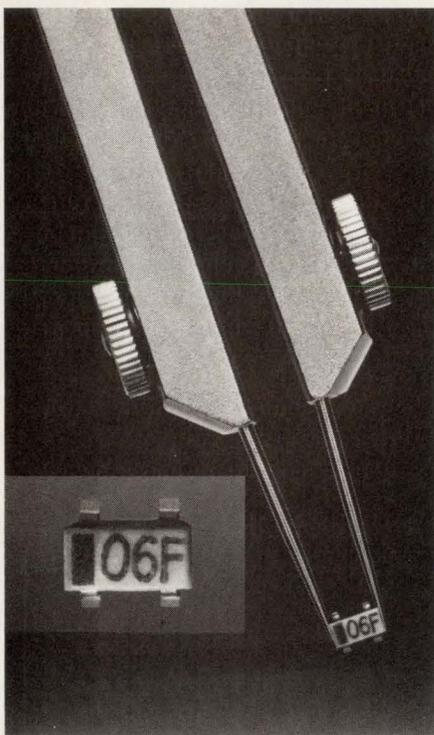
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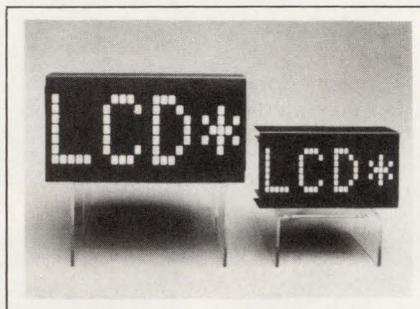
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0.070-in. lead spacings. They use screw machine pins and gold-plated beryllium-copper inner contacts. The glass-epoxy insulators have an open design, and the closed-contact feature eliminates solder or flux-wicking problems. The sockets are available in a choice of 28, 42, and 64 positions in solder-tail terminations and tin or gold plating. A socket with 30 μ m. of gold plating on the contact and tin plating on the sleeve, \$4.80 (100).

Precicontact Inc, Box 798, Langhorne, PA 19047. Phone (215) 757-1202.

Circle No 392



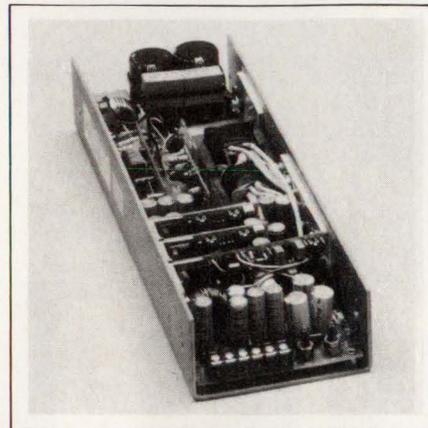
DISPLAYS

- -30 to +85°C operating range
- 2.5- and 4-in. character heights

The Supernova system consists of stackable 4-character LCD modules and a serial-ASCII input controller card. The 5x7 dot-matrix characters are available in 2.5- and 4-in. character heights. You can stack the modules to build displays 40 characters long. The operating range is -30 to +85°C. Exclusive of backlighting, the modules draw less than 30 mW/character. The CPU/controller card accepts serial ASCII data from the host system and provides all timing and control signals, and regulated power for two rows of as many as 40 characters each. Modules, \$154 (100); controller card, \$200. Delivery, four to six weeks ARO.

IEE Inc, 7740 Leona Ave, Van Nuys, CA 91409. Phone (818) 787-0311. TLX 4720556.

Circle No 393



POWER SUPPLY

- Complies with FCC and VDE EMI requirements
- 400W total output power

The 7M400 offers four fully regulated outputs and one quasi-regulated output. The unit complies with conducted EMI requirements of FCC and VDE. The outputs are 5V at 60A, 12V at 10A, -12V at 5A, -5V at 5A, and 24V at 6A. The maximum total power equals 400W. Its fully regulated outputs exhibit 0.15% load and line regulation. The 24V output has \pm 5% regulation. Remote sensing is available on the 5, -12, and -5V outputs. Additional features include protection against overload, reverse polarity, and over-temperature conditions. The fully regulated outputs can be adjusted to within \pm 5%, and feature independent current limiting and over-voltage protection. \$528. Delivery, stock to eight weeks ARO.

Sierra Power Systems, 20500 Plummer St, Chatsworth, CA 91311. Phone (818) 998-9873.

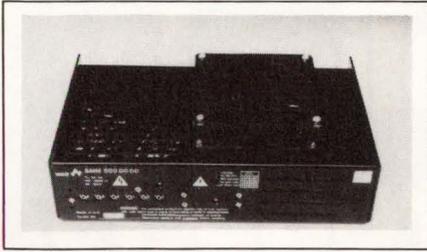
Circle No 394

SWITCHING SUPPLY

- Provides five outputs with 500W total output power
- Has integral fan cooling

Provided with integral fan cooling, the SMM500 switching power supply delivers an output power of 500W. The unit features five fully isolated and fully regulated outputs.

COMPONENTS & POWER SUPPLIES



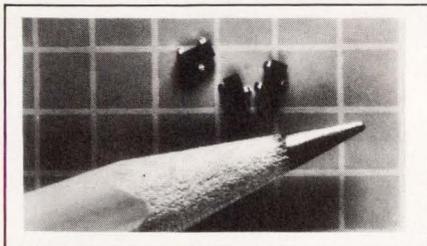
The main output provides 5V at 60A. The secondary outputs are adjustable and provide one 12 to 24V output at 5A maximum, two 12 to 15V outputs at 6A maximum, and one 5 to 15V output at 3A maximum. The main 5V output has remote sensing, which will handle as much as 0.5V of voltage drop in connecting leads. Overvoltage protection trips the main 5V output at approximately 6.2V. The unit is also provided with overtemperature protection. The power supply conforms to IEC and BS safety specifications. £300 (100).

Weir Electronics Ltd, Durban Road, Bognor Regis, Sussex PO22 9RW, UK. Phone (0243) 865991. TLX 86543.

Circle No 395

Weir Electronics Inc, 418 Third Street, Annapolis, MD 21403. Phone (301) 268-0122. TWX 510-600-7370.

Circle No 396



TRANSISTORS

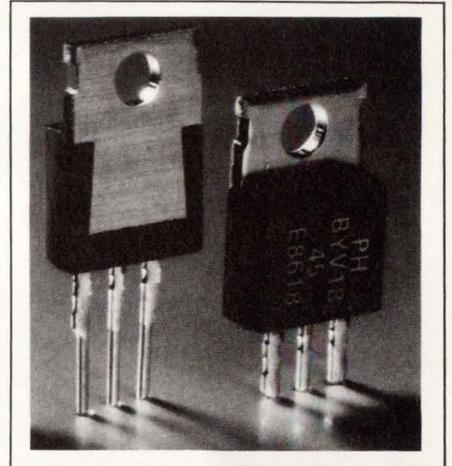
- *Surface-mount SOT-23 package for nonhermetic applications*
- *Available in tape-and-reel packaging*

The HSMX-3131 and -3635 are npn bipolar transistors housed in a plastic SOT-23 package that's designed to accommodate nonhermetic applications. Both are available in standard or low-profile versions to allow

thorough board cleaning or epoxy bonding. The -3131 has a gain of 14 dB at 1 GHz and a typical noise figure of 1.8 dB. The -3635 has a 15-dB gain and a 1.4-dB noise figure at 1 GHz. The transistors are supplied in tape-and-reel packaging for automated assembly as well as in bulk packaging. HSMX-3131, \$1; HSMX-3635, \$1.35 (1000).

Hewlett-Packard Co, 1820 Embarcadero Rd, Palo Alto, CA 94303. Phone local office.

Circle No 397



RECTIFIER DIODES

- *Configured as a common-cathode pair*
- *Monolithic*

The BYV18 Series of Schottky-barrier double rectifier diodes includes diodes with repetitive-peak reverse voltage ratings of 30, 35, 40, and 45V. Reverse current is a maximum

of 30 mA at maximum rated voltage. The maximum output current with both diodes conducting is 10A, and they have a typical forward voltage drop of less than 0.6V. Configured as a common cathode pair, both diodes are diffused onto the same silicon die, providing thermal stability and current-sharing capability. As a result, you can parallel the diodes without derating them. The housing

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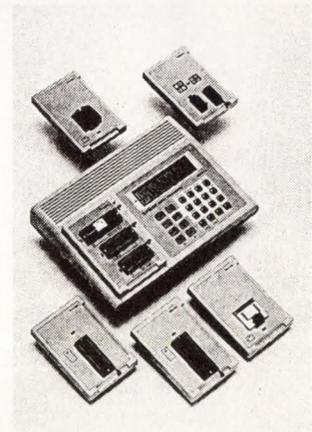
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CIRCLE NO 54

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COMPONENTS & POWER SUPPLIES

is the plastic TO-220 package. Approximately \$1.10 (1000).

Philips, Elcoma Division, Box 523, 5600 AM Eindhoven, The Netherlands. Phone (040) 757005. TLX 51573.

Circle No 398

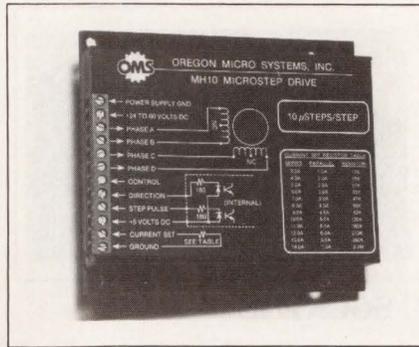
Amperex Electronic Corp., George Washington Hwy, Smithfield, RI 02917. Phone (401) 232-0500.

Circle No 399

MOTOR DRIVER

- *Microsteps 2-phase motors*
- *Opto-isolated step and direction inputs*

The MH10 can drive a 200-step hybrid permanent-magnet (PM) motor at 2000 steps/revolution. It can operate a wide range of 2-phase step motors with current ratings ranging to 14A per phase; a heat sink is required for the larger motors.



Using an external resistor, you can program the output current yourself. The supply voltage range for the driver spans 24 to 60V. The step and direction inputs are opto-isolated to minimize ground loops and improve noise immunity. The drive is packaged in a 4×4.5×1-in. module, including mounting flange. \$350.

Oregon Micro Systems Inc., 14273 NW Science Park Dr, Portland, OR 97229. Phone (503) 644-4999.

Circle No 400

DIGITAL PANEL METER

- *Incorporates an integral EMI shield*
- *Dot-matrix LED display*

The Model 100 mil-spec digital panel meter is available with either a 3½- or 4½-digit LED dot-matrix display. The unit includes an integral EMI shield. Its reading capability ranges from 2V to 1 kV dc, or 0.2 to 200 mA. All I/O devices terminate at a subminiature D connector on the rear. Other features include serial BCD output, display blank, lamp test, underrange, overrange, strobe, busy, and hold. From \$2900. Delivery, 16 to 20 weeks ARO.

International Microtronics Corp., 4016 E Tennessee St, Tucson, AZ 85714. Phone (602) 748-7900. TWX 910-952-1170.

Circle No 401

CY600 INTELLIGENT DATA ACQUISITION CONTROLLER

provides sophisticated data monitoring using 16-bit registers accessed by ASCII name (A,B,C, etc.) and ASCII operators (+ - * / <> =). Multiple independent channels store programs on-chip for scanning. Interrupt master on TRUE event.

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CIRCLE NO 56

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CIRCLE NO 60

PC-AT BUS BOARD-LEVEL COMPATIBLE

8 or 10 MHz
Zero wait states



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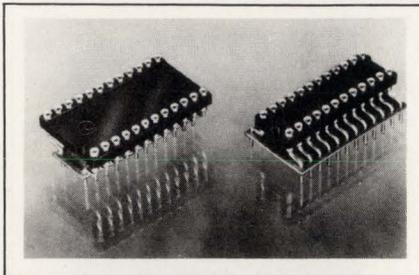


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San Diego, CA 92123 TLX: 910 240 0290

CIRCLE NO 57

COMPONENTS & POWER SUPPLIES



IC SOCKETS

- Have a 94V-0 UL rating
- Contacts feature gold plating

These adapter sockets let you use ICs with 0.300-in. centers on boards with 0.600-in. centers and vice versa. The sockets feature collet contacts with gold plating over copper-beryllium material. The brass socket body is available with either tin or gold plating. Its housing material has a 94V-0 UL flammability rating. The sockets are available in sizes ranging from 6 to 48 pins. A 24-pin device costs \$3.50 to \$6.40, depending on quantity.

Aries Electronics Inc., Box 130,
Frenchtown, NJ 08825. Phone (201)
996-6841.

Circle No 402

KEYBOARDS

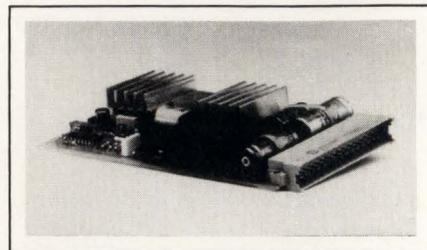
- Compatible with IBM PC/AT and PC/XT
- Available in both full-travel and micromotion versions

These keyboards are available in both full-travel (FKB 2831, FKB 2835) and micromotion (FKB 3140) versions. Each is compatible with a different IBM interface. The -2831 uses a PC/XT-compatible interface that also operates on the IBM PC system. The PC/AT- and PC/XT-compatible -2835 is automatically software switchable for use on either of the two systems. The -3140 is designed for use with PC/AT-compatible systems. The full-travel units have lifetimes of 50 million keystrokes and are available with either tactile or nontactile switches. The lifetime for the -3140 equals 10 million keystrokes. All units feature

an 84-key PC/AT layout and can be configured for custom or semicustom capabilities. FKB 2831 and FKB 2835, \$46; FKB 3140, \$89.70 (500).

Fujitsu Component of America Inc., 3320 Scott Blvd, Santa Clara, CA 95054. Phone (408) 562-1000.

Circle No 403



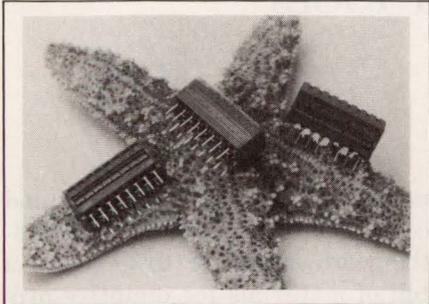
DC/DC CONVERTER

- Provides 50W of output power at 5, 12, 15, or 24V
- Has galvanic isolation between input and output

The SR851 is a 50W isolated dc/dc converter available with standard output voltages of 5, 12, 15, or 24V. Versions are available for standard input voltages of 12, 24, 48, or 60V ±25%. Load regulation for 10 to 90% load changes is 1%, and line regulation is 0.5% for ±10% input voltage changes. The output has remote sensing and is overvoltage protected. The output current is limited to 120% of its nominal value to provide short circuit protection. Output ripple and noise is 0.6% p-p, and spikes as high as 100 kHz are limited to less than 1% of the converter's output voltage. The converter has an operating range of 0 to 70°C, but requires derating at 2.5%/°C at temperatures above 50°C. Conforming to a single-Eurocard footprint, with a height of 20 mm, the SR851 is equipped with a DIN-41612 connector that is pin compatible with other supplies in the company's line. DM 280.

Brandner Vertriebs-GmbH, Siemensstrasse 26, 8755 Alzenau, West Germany. Phone (06023) 330105. TLX 4188593.

Circle No 404



DIP SWITCHES

- Withstand automatic solder and cleaning processes
- Feature gold over nickel contacts

The 53D Series right-angle slide-DIP switches are available with polyester tape seals that allow them to withstand automatic soldering and cleaning processes. They are available in 2- through 10-position spst switch configurations. The contacts are gold over nickel to ensure low contact resistance and are rated for switching loads of 5V dc at 100 mA max. Its switch actuators are

recessed to prevent accidental actuations. The blue insulator and cover material is made of a UL-listed (94V-0), flame-retardant, glass-filled thermoplastic. The white numbers on the cover identify individual switch positions. From \$0.82 (5000) for an 8-position unit. Delivery, stock to six weeks ARO.

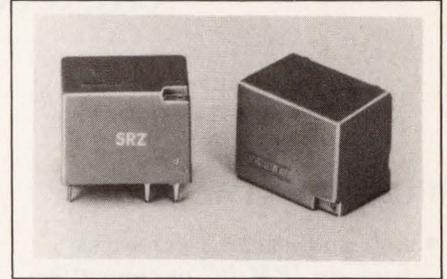
JAE Electronics Inc, 1901-A E Carnegie Ave, Santa Ana, CA 92705. Phone (800) 523-7278; in AK and CA, (714) 250-8770. TLX 681438.

Circle No 405

RELAYS

- Sealed or unsealed construction
- 100,000-operation lifetime

The SRZ 3A dpdt relays measure 0.835×0.563×0.654 in. They are available in sealed or unsealed versions. The devices feature silver cadmium contacts, switch 3A at



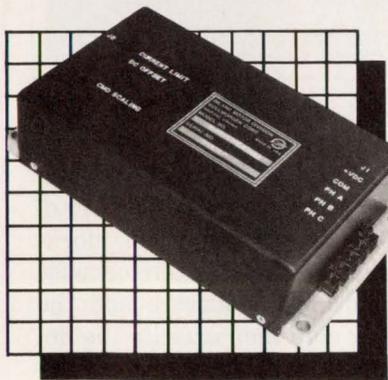
120V ac, and have a life expectancy of 100,000 operations at rated load. The available coil voltages range from 3 to 48V dc. Its coil pickup power equals 0.360 mW, and dielectric strength is 1000V ac. An unsealed 12V model, \$1.68 (1000).

Original Electric Manufacturing Co Inc, 123B Lincoln Blvd, Middlesex, NJ 08846. Phone (201) 271-5770.

Circle No 406

I N L A N D

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CIRCLE NO 61

NEW PRODUCTS

CAE & SOFTWARE DEVELOPMENT TOOLS

PC/VAX NETWORK

- Lets you use VAX resources from an IBM PC or compatible
- Can download VAX data to PC programs

PC Expander is an integrated hardware/software product that allows you to connect an IBM PC or compatible to a VAX equipped with the vendor's Distributed Network Processor. The hardware consists of a PC Controller that plugs into the PC and handles all network communications-processing tasks for the PC. The Advanced Network Management software allows PC users to access VAX files, programs, and peripherals, and to run VAX applications such as VAXmail. From the VAX, you can download data files to MS-DOS programs, such as Lotus 1-2-3, and then initiate execution of those programs. If multiple PCs are on the network, they can communicate directly with each other, as well as with the VAX host. PC Controller, \$695; Advanced Network Management, \$375.

Xyplex, 100 Domino Dr, Concord, MA 01742. Phone (617) 371-1400. TWX 910-380-4463.

Circle No 409

PART-LISTING PROGRAM

- Provides 35 levels and 35 subassemblies/level
- Can handle as many as 490,000 components/system

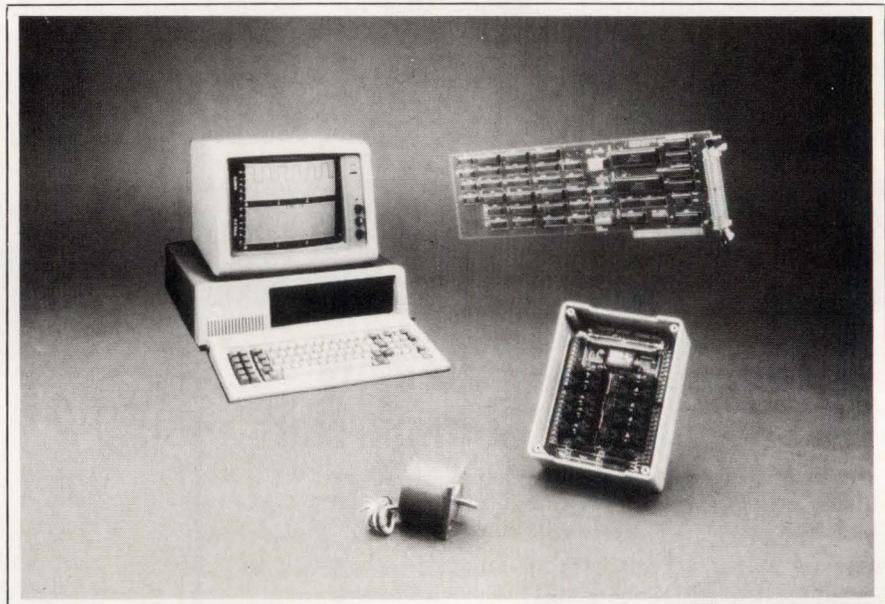
Partlister version 3.0 allows as many as 35 levels of subassembly below the main assembly (level 0); each of these levels can in turn have as many as 35 subassemblies. These 1225 subassemblies can each encompass as many as 400 components, for a total of 490,000 components per system. You enter parts by part

type, such as R (resistors), C (capacitors), SA (subassembly), or M (mechanical). The data fields include reference designator, part type or value, company part number, preferred manufacturer, MIL-spec number, and description (comments). The program can generate three reports: a parts-list that lists all components sorted by reference designator; a summary list that shows the total quantity of each component type; and a bill of materials that groups identical compo-

nents and provides the totals and costs. You can also apply an across-the-board multiplier to generate a bill of materials for quantity-production purposes. To facilitate searches, you can sort the list on multiple fields and scroll the display by line or by page. The program runs on all IBM PCs and compatibles. \$79.95.

LiveWire Software, Box 773, Pacific Palisades, CA 90272. Phone (213) 454-4492.

Circle No 410



MOTION CONTROL

- Provides two channels of step-per-motor control
- Reads two incremental shaft encoders

MStep-5 is a hardware-software subsystem that allows an IBM PC or compatible to read two incremental shaft encoders and to control two stepper motors. You can monitor encoders or control stepper motors with the aid of high-level commands. An initialization routine lets you set acceleration and deceleration

rates, maximum step rate, and any other needed parameters. Once you've initialized the subsystem, you need only provide the number of steps to move (positive for clockwise, negative for counterclockwise movement). The software and the controller chip then execute the desired movement with 24-bit resolution; that is, the maximum number of steps is 8,388,608 in either direction. You can specify a constant step rate or a controlled acceleration/deceleration profile. In addition, the subsystem has a motor-enable out-

put and five limit-switch inputs for each of the two motor channels. The limit switches provide a normal and an emergency stop at each end of the travel, and a home or reference signal at any intermediate point. You'll need a driver board capable of supplying the large currents required by stepper motors. If you don't already have such a board, you can connect the vendor's Sta-Step 2-channel driver board between the controller and the motor. The vendor can also supply the Step-Encl shaft encoder, which yields 1000 pulses per revolution, and the Step-Mot1 stepper motor, which yields a torque of 35 oz-in. and requires 200 pulses per revolution. MStep-5 controller, \$595; Sta-Step driver board, \$325; Step-Mot1 motor, \$190; Step-Encl shaft encoder, \$275.

Metrabyte Corp., 440 Myles Standish Blvd, Taunton, MA 02780. Phone (617) 880-3000. TLX 503989.

Circle No 411

LISP FOR 80386

- Provides Common Lisp development tools
- Includes an interactive tutorial

The GCLISP 386 Developer runs on the Compaq Deskpro 386 and provides software developers with a Common Lisp system for building expert systems, natural-language interfaces, and other artificial-intelligence applications. The package makes full use of the speed and large memory of the Deskpro 386, and lets you develop large, complex applications that would otherwise require the power of a dedicated Lisp machine. An important feature is the ability to integrate C programs with applications written in Lisp, eliminating the need to re-write the C programs in Lisp. The package includes an interpreter, a compiler, an on-line help system, and an enhanced editor that has more than 150 commands, uses

Emacs keychord bindings, and lets you define your own keychord bindings. The package comes with Lisp Explorer, an interactive tutorial developed by P H Winston and San Marco Associates; the *Common Lisp Reference Manual* by G Steele; and the *GCLISP 386 Developer's Manual*. \$1195.

Gold Hill Computers Inc., 163 Harvard St, Cambridge, MA 02139. Phone (617) 492-2071.

Circle No 412

TEST GENERATOR

- Cross-development system lets you create programs on a VAX
- Lets you develop test software for complex VLSI IC's

The ATG-32 software package, which runs on the vendor's 3200V computer system, as well as on most VAX and MicroVAX machines, allows you to develop test programs to run on the vendor's 227X family of



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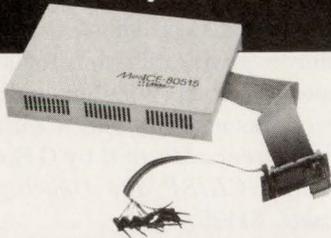


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CIRCLE NO 62

IBM PC-hosted 8051 Emulators from \$1495!



For 8051 designs that meet engineering budgets and quality standards, you'll need MetalLink's cost-effective, high-performance 8051 family of development tools.

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CAE & SOFTWARE DEVELOPMENT TOOLS

in-circuit automated-test equipment. The menu-driven interface controls and directs your access to various utilities, both automatic and interactive, which can generate test programs for use on 227X systems. By making use of the VAX's large physical memory and its virtual-memory facilities, ATG-32 can generate programs to test boards containing complex VLSI devices and ASICs. From \$30,000.

GenRad Inc., 300 Baker Ave, Concord, MA 01742. Phone (617) 369-4400.

Circle No 413

SIMULATOR

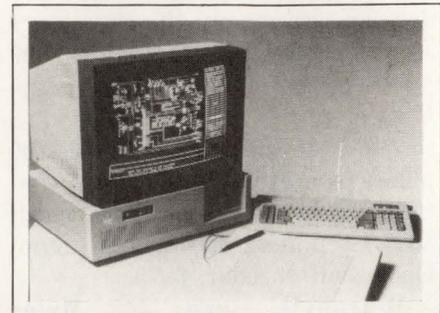
- Provides for interactive simulation of analog circuits
- Component library has more than 900 components

Mspice Plus is a software package that interactively simulates analog systems; it runs on the vendor's Idea Series workstations. The input to Mspice Plus consists of circuit data that you've created with the aid of the vendor's NetEd schematic-capture program. The package's built-in control language lets you specify system parameters before the simulation begins. You can stop the simulation at any time and change any or all of the parameters before proceeding. The control language also allows you to perform multiple temperature or statistical analyses on the simulation results. You can store the resulting waveforms and combine them in the form of histograms or multiple charts. The component library contains the technical and operating specifications of more than 900 commonly used parts, including op amps, bipolar transistors, zener diodes, and FETs. The library also contains standard component symbols for use by schematic-capture and board-layout programs. You can add new standard or customized parts to the library at any time. Mspice Plus is available either as a full option to

Idea Series products or as an upgrade to Idea Series workstations that already have Mspice or Msimon simulators. Full option, \$19,900; upgrade, \$9900. The complete analog library is \$20,000 for the first copy, \$2000 for additional licenses.

Mentor Graphics Corp., 8500 SW Creekside Pl, Beaverton, OR 97005. Phone (503) 626-1301.

Circle No 414



SCHEMATIC CAD

- Runs on IBM PCs or compatibles
- Interfaces to popular simulators and routers

Interfacing to most popular circuit simulators and routers, the ESP schematic-capture software allows you to create analog or digital circuit designs on an IBM PC or a compatible computer. A version is also available for DEC VAX computers. The package offers a hierarchical approach to design: You can start with an array of interconnected functional blocks and then create a component-level design from it. The menu-driven program has a user-definable symbol menu that allows you to enter your own symbols into the symbol library. The package's editing facilities include checking on the revision status of symbols, symbol updating, cell movement and alignment, automatic text location, and labeling. In addition, the system's net-list-extraction routines verify signal integrity both between circuit blocks and between schematic sheets. The system includes pan and zoom facilities. The macro facility lets you build

CAE & SOFTWARE DEVELOPMENT TOOLS

your own commands, and the "journaling" function allows for crash recovery or procedure duplication. Approximately £5000 for a single-user license.

Cocad Ltd, Ashford House, Tuf-ton Centre, Ashford, Kent TN23 1YB, UK. Phone (0233) 43445. TLX 966444.

Circle No 415

MULTILINGUAL UNIX

- Combines features of System V.3 and BSD 4.3
- Provides system messages and on-line help in 19 languages

The UniPlus+ System V Release 3 operating system combines the most recent features of AT&T's System V.3 and Berkeley Software Distribution's BSD 4.3 implementations of Unix. UniPlus+ includes shared libraries, mandatory and advisory record locking, the Assist menu-driven command-selection feature, Transport-Level Interface (TLI), and Transport-Provider Interface (TPI). In addition, the Korn shell combines the best features of the Bourne shell and the C shell. To improve performance, the vendor has added fast-file and large-block file systems, as well as a smart-board executive that helps to offload tasks from the host to intelligent slave processors. The operating system's power-failure-recovery feature preserves file-system integrity even after a complete power failure. Its international-language-support feature provides messages and on-line help in any of 19 languages, including French, German, and Arabic. The floating-point capability adheres to IEEE-754 data formats and is compatible with the Motorola 68881 floating-point coprocessor. The operating system makes networking easier by using the Network File System (NFS), B-NET (an implementation of the DoD TCP/IP protocol), and PC Interface (which allows UniPlus+-based systems to communicate with IBM PCs

or compatibles). Price varies according to implementation; from \$40,000 for a 68020-based VME system with a paged MMU.

UniSoft Corp, 739 Allston Way, Berkeley, CA 94710. Phone (415) 644-1230.

Circle No 416

CAE LIBRARIAN

- Merges libraries and copies or moves symbols between them
- Runs on IBM PC family

The Library Management Program is for use with the Dash schematic designers from FutureNet (Canoga Park, CA). The program can print or plot all of the symbols in a Dash library in data-book format for checking or reference purposes. It can create a drawing file (for on-line viewing) of all the symbols in a library, merge two libraries, delete groups of symbols from a library, copy or move symbols from one library to another, and create a DOS file containing a master list of all the symbols in all of your libraries. When you delete symbols, the program not only removes the part name from the symbol directory, but also removes the symbol definition and crunches the file, thereby saving you as much as 2.5k bytes of disk space for each deleted symbol. \$49.

CAE Utilities, 14819 Sherman Way, Suite 8, Van Nuys, CA 91405. Phone (818) 989-3308.

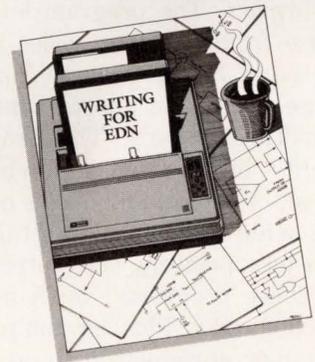
Circle No 417

GRAPHICS SOFTWARE

- Facilitates preparation of presentation art and slides
- Creates high-quality charts from spreadsheet data

Rio and ImageStation are the first two releases in the vendor's Soft-Visions line of graphics software. The programs run on the vendor's PC 6300 personal computer equipped with its TrueVision Targa

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16 or Targa 32 videographics adapter. Rio, a resolution-independent, object-oriented drawing program, lets you create and manipulate an image consisting of text, geometric shapes, and color photos captured by a Targa board. The program provides special effects such as embossing, drop shadows, and translucency to produce a three-dimensional appearance. You can produce high-quality output on either a digital film recorder or a Postscript hard-copy device. ImageStation lets you convert spreadsheet data to bar charts, pie charts, and other graphical formats. The program lets you choose from five font styles and a palette of 32,768 colors. You can merge electronic photos captured by a Targa board. The program accepts input from a keyboard, mouse, or tablet, and allows output to a wide variety of digital film recorders, printers, and plotters. To run these programs, you'll need a PC 6300, 6300 Plus, or compatible computer equipped with at least 640k bytes of RAM and a hard-disk drive. Rio-16, ImageStation, \$1250 each.

AT&T Graphics Software Labs, 10291 N Meridian, Suite 275, Indianapolis, IN 46290. Phone (317) 844-4364.

Circle No 418

C FUNCTION LIBRARY

- Provides device handlers for graphics and character I/O
- Provides string, menu, and system functions

The BlackStar C function library provides 275 fully tested functions for use with versions 3.0 and 4.0 of the Microsoft compiler and version 3.0 of the Lattice compiler. The library is organized by category. It uses logical naming conventions and function prefixes. The quick-reference section in the manual makes it easy to find and use any function in the library. For optimal speed and memory usage, some of the func-



tions are written in assembly language. The library includes device handlers for screen, graphics, keyboard, printer, and mouse devices, as well as interrupt, string, menu, date/time, and other system functions. The package includes a 317-page manual, complete source code, and a demo program. Versions for small-, medium-, and large-memory models are included on the disks. \$99.

Sterling Castle Software, 702 Washington St, Suite 174, Marina del Rey, CA 90292. Phone (800) 722-7853; in CA, (213) 306-3020.

Circle No 419

EXPERT-SYSTEM SHELL

- Incorporates both forward and backward chaining
- Probability rules make use of certainty factors

Aurora, an inference system that allows you to develop knowledge-based expert systems, uses both forward and backward chaining. Backward chaining is the primary problem solver; forward chaining uses common-sense knowledge related to the problem in order to prevent the generation of redundant or unsound questions in the reasoning process. You construct the knowledge base for a particular application by having a human expert in the field define a modular set of If . . . Then rules, which are expressed in English sentences or algebraic formulae. The expert can

assign a probability factor to each rule in the knowledge base. The program provides extensive on-line data-retrieval facilities that help you review the logic during the development of an expert system; its on-line help facilities provide additional guidance. Aurora is available in five versions for IBM PCs and for workstations. From \$1500 (Common Lisp version for IBM PC/XTs and PC/ATs).

Mystech Associates Inc, Box 220, Mystic, CT 06355. Phone (203) 536-2663.

Circle No 420

C CROSS-COMPILER

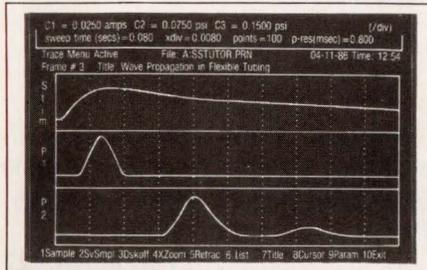
- Generates code for the 68020 and the 68881 numeric coprocessor
- Runs under MS-DOS, Xenix, or Unix

The 68020+68881 C cross-compiler runs on MS-DOS, Xenix, or Unix systems. It generates 68020 code and lets you selectively enable code generation for the 68881 numeric coprocessor. When you enable this feature, the cross-compiler encodes all C floating-point operation as in-line 68881 instructions. When you disable the feature, the compiler substitutes calls to low-overhead C functions that generate 68020 code; you don't have to perform any "register-save" operations. The cross-compiler uses all eight of the 68881's registers, and you can reserve six of these for register variables. If you wish, you can assign global floating-point variables to the registers. You can declare constants with double-precision accuracy and store floating-point constants in single-precision, double-precision, packed, and extended formats. \$595 for the MS-DOS version; \$1390 for the Xenix version; \$2790 for the Unix version.

Software Development Systems Inc, 3110 Woodcreek Dr, Downers Grove, IL 60515. Phone (312) 971-8170.

Circle No 421

CAE & SOFTWARE DEVELOPMENT TOOLS



PC STORAGE SCOPE

- Displays any eight of 16 possible channels
- Averages trigger-synchronized waveforms

Snapshot Storage Scope version 2.5, which turns an IBM PC into a digital-oscilloscope and data-acquisition system, has been enhanced to let you display any eight of 16 possible channels, define units and labels for each channel, and average trigger-synchronized waveforms. You can specify a title for each frame of data and send the data to an X-Y plotter. A data-compression algorithm reduces the file size to one-fifth that of a standard file containing the same display data, and correspondingly reduces the times needed to store or retrieve the files. This enhanced version also permits the real-time acquisition of 32,000 data points with 12-bit accuracy, and it provides a sampling rate that you can vary from as few as 2 samples/hour to as many as 130,000 samples/sec. In addition, you can now compare a newly acquired waveform to a reference trace to determine whether or not the circuitry is functioning properly. The menu-driven program prompts you for all needed setup information. As with earlier versions, this version lets you display data graphically or in tables, and it allows you to analyze the data with the aid of the vendor's other products or with spreadsheets such as Lotus 1-2-3. To run the program, you need an IBM PC/XT or PC/AT equipped with a floppy-disk or hard-disk drive; at least 384k bytes of RAM; a CGA, EGA, or Hercules graphics adapter; and an I/O analog interface board from MetraByte,

Data Translation, Analog Devices, or Burr-Brown. The vendor recommends using an 8087 math coprocessor. \$495.

HEM Data Corp, 17025 Crescent Dr, Southfield, MI 48076. Phone (313) 559-5607.

Circle No 422

CROSS-COMPILER

- Lets you develop and test software for microcontrollers
- Runs on the IBM PC and compatibles

ChipForth, which runs on the IBM PC and compatible computers, lets you develop and interactively test Forth programs for single-chip Motorola and Intel microcontrollers. The package combines the vendor's PolyForth language and operating system with cross-development tools. When you've edited and compiled your program, you can download a special "talker" program to the target machine via an RS-232C link. The talker allows you to download your application program to the target machine and then test and debug the program interactively from the PC. When debugging is complete, you can remove the talker, leaving your application code in ROMable form. The package includes an editor/assembler/compiler; terminal- and disk-I/O routines for interactive testing and debugging; and a real-time, multitasking executive that runs the application on the target machine. Versions for the Motorola 6801 and 6301 μ Cs are available now; versions for the Intel 8051 and 8096 μ Cs will be available in the third quarter of 1987. 6801/6301 versions, \$3250 each.

Forth Inc, 111 N Sepulveda Blvd, Manhattan Beach, CA 90266. Phone (213) 372-8493.

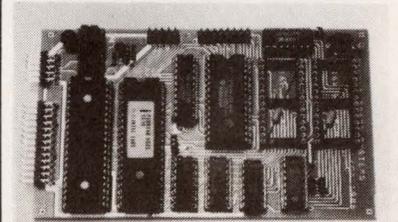
Circle No 423

Introducing....

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from

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Standard Features

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NEW PRODUCTS

TEST & MEASUREMENT INSTRUMENTS



COMM TESTERS

- *Portable units combine several functions*
- *Feature built-in keyboards and LCDs*

According to the manufacturer, the Interview 5, 5 Plus, 10 Plus, and 15 Plus each combine the functions of the following instruments: a data-line monitor, protocol analyzer/emulator, RS-232C breakout box, bit-error-rate tester, DMM, dB-level

meter, dumb terminal, continuity tester, power-line monitor, monitor alarm, and peripheral tester. Each unit weighs under 5 lbs and has a built-in keyboard and LCD. Some units have disk drives. Optional plug-in modules accommodate common protocols. From \$2995. Delivery, 60 days ARO.

Atlantic Research Corp., 7401 Boston Blvd, Springfield, VA 22153. Phone (703) 644-9190. TLX 197733.

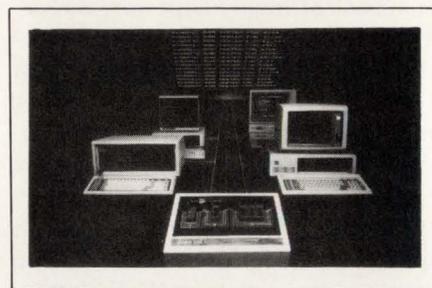
Circle No 426

Philips, Industrial & Electro-acoustic Systems Div, Box 218, 5600 MD Eindhoven, The Netherlands. Phone (040) 788620. TLX 35000.

Circle No 427

Philips Test and Measurement Instruments Inc., 85 McKee Dr, Mahwah, NJ 07430. Phone (201) 529-3800.

Circle No 428



DRAM TESTER

- *Performs functional and parametric testing*
- *Requires an IBM PC for control*

The DM700 tester performs functional and parametric testing of dynamic RAMs. The tester, which requires an IBM PC or compatible computer for control, comes with a software device library that includes tests for DRAMs with capacities from 16k to 4M bits. Two levels of testing are possible. The first level comprises a functional check; the second level performs parametric testing to ensure that devices meet their manufacturers' specifications. The instrument tests such parameters as access time, refresh function, input/output logic, and data retention. To detect marginal parts, you can perform these tests at the extremes of the device's operating supply-voltage range. A continuous-test-cycle facility allows you to detect intermittent and thermal failures in devices. You can test as many as four devices at once, and you can transmit the test results for each device to a printer for hard



PULSE GENERATOR

- *Provides pulse-repetition rates from 1 Hz to 125 MHz*
- *Provides choice of rise times*

The PM5785 pulse generator has a pulse-repetition rate of between 1 Hz and 125 MHz. It gives you a choice of fixed 2-, 1.5-, or 1-nsec rise times. You can select bipolar or positive- or negative-going pulses in any

of four amplitude ranges between 0.2 and 5V. The instrument makes pulses available from two complementary outputs, and its impedance back-matching absorbs more than 95% of the signal reflections caused by mismatched loads. Besides providing front-panel control, the generator lets you control pulse triggering, duration, and gating from external sources. The external trigger's slope and level controls allow you to synchronize the pulse generation to an external clock. Its external-gating feature permits you to generate bursts of pulses. A burst-mode option provides programmable pulse bursts containing 1 to 9999 pulses. \$3385.

copy. Including the test-head console, interface card and cabling for the IBM PC, test software (on a floppy disk), and manuals, the DM700 costs \$1475.

Computer Service Technology Inc., Amsterdamsestraatweg 23, 1411 AW Naarden, The Netherlands. Phone (02159) 40697. TLX 73413.

Circle No 429



LC METER

- Applies as much as 1000V across capacitors
- IEEE-488 option available

The LC77 Auto-Z LC meter measures capacitors from 1.0 pF to 19.99F and inductors from 1.0 mH to 19.99H. The meter also measures capacitors' dielectric leakage (with as much as 1000V applied), dielectric absorption, and equivalent series resistance. The unit is battery operated. An option dynamically tests SCRs and triacs. The instrument is programmable over the IEEE-488 bus. LC77 Auto-Z, \$1695; SCR and triac option, \$148; IEEE-488 option, \$625; battery, \$59.95; ac adapter, \$48.

Sencore Inc., 3200 Sencore Dr, Sioux Falls, SD 57107. Phone (800) 843-3338; in SD, (605) 339-0100.

Circle No 430

DMM CALIBRATOR

- 6½- and 8½-digit ac calibration is NBS-traceable
- IBM PC controls calibration

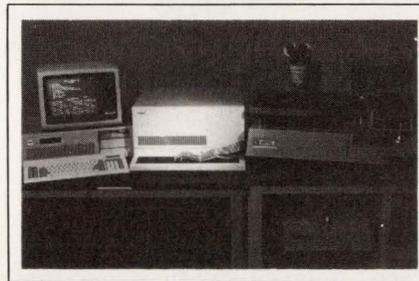
The Model 4052H Computest calibration system performs NBS-traceable ac-voltage calibration of 6½- and 8½-digit DMMs. The unit



also checks dc-voltage, ac- and dc-current, and resistance functions. The system uses the company's 1605A transfer standard and an IBM PC fitted with an IEEE-488 board to control the calibration system. The system software works with a variety of calibrators. From \$29,000. Delivery, four to eight weeks ARO.

Ballantine Laboratories Inc., Box 97, Boonton, NJ 07005. Phone (201) 335-0900.

Circle No 431



ASIC VERIFIER

- ASIC-verification system runs at 20 MHz
- System has 352 pins

The STM5200 ASIC-verification system has a 20-MHz test rate and 352 test pins. The system uses an IBM PC for control and test programming. Each of the 352 I/O pins possesses a 64k-byte-deep memory. The system also has four pin-driver power supplies with 25-mV resolution, eight timing sets, two strobe groups, a 32k-byte word-pattern generator, and high-speed voltage comparators. A parametric measuring unit is optional. From \$35,750 (32-pin model).

Cadic Inc., 7874 SW Nimbus Ave, Beaverton, OR 97005. Phone (503) 626-7902.

Circle No 432

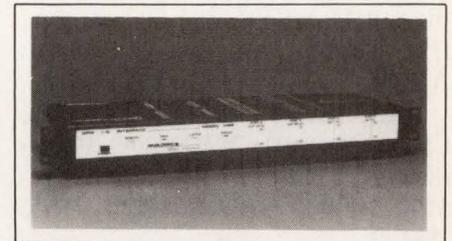
SOURCE DEBUGGER

- Debugger uses IBM PC to control in-circuit emulator
- Works with code produced by C compiler

The Microscope 68k is a source-level, C-language debugger that now controls the firm's in-circuit emulators for the 68000 and 68010 μ Ps. The debugger works with code produced by the 68000/10 C compiler and can execute from the IBM PC, PC/XT, and PC/AT; from Apollo and Sun workstations; and from DEC VAX systems. The debugger's commands accept C variables and expressions as arguments rather than as absolute locations. The debugger also does conventional assembly-level debugging. MicroScope package for PC environment, including C compiler and utilities, \$3500.

Microcosm Inc., 15275-E SW Koll Parkway, Beaverton, OR 97006. Phone (503) 626-6100. TLX 759527.

Circle No 433



IEEE-488 PORT

- Provides general-purpose ports under IEEE-488 control
- Includes optoisolated and relay ports

The Model 1488 utility module has four general-purpose, 8-bit ports under IEEE-488 control: The ports are a TTL input port, a TTL output port, an optoisolated port, and a port with eight STDP relays. You can operate each port as a parallel port or in single-bit mode. The unit measures 1¼×7×17 in. \$895.

Data Precision, Electronics Ave, Danvers, MA 01923. Phone (617) 246-1600. TLX 6817144.

Circle No 434



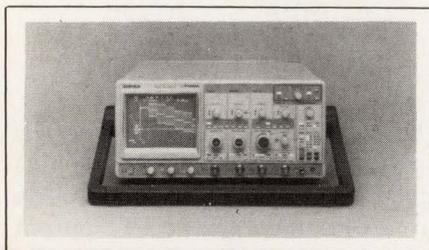
DIGITAL TESTERS

- Emulate μP of system under test
- Stimulate as many as 160 I/O pins

The 9100 Series digital testers are suitable for automated testing and troubleshooting of μP -based pc boards. The 9100A functions as both a test station and a test-software development system. The 9105A is simply a test station. The testers replace the μP in the system under test and execute various functional tests. Other test facilities include a 40-MHz manual probe and I/O modules that permit the simultaneous testing of as many as 160 10-MHz pins. 9100A/SYS, \$21,500; 9105A, from \$9000. Delivery, six weeks ARO.

John Fluke Mfg Co Inc, Box C9090, Everett, WA 98206. Phone (800) 426-0361; in WA, (206) 347-6100. TWX 910-445-2943. TLX 185102.

Circle No 435



ANALOG SCOPE

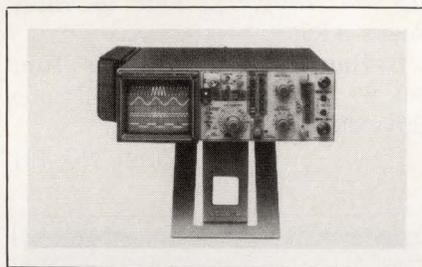
- Scope has four channels
- CRT shows parameters and settings

Model COM7100A is a 4-channel, dual-timebase, 100-MHz analog oscilloscope. The instrument's CRT

shows measured parameters and scope settings. Cursors provide measurement of ΔT , frequency, ΔV , ratio, and phase; a built-in DVM displays dc, p-p, or rms-ac voltage levels on channel 1. You can measure the frequency of trigger input with the built-in frequency counter. An IEEE-488 interface is optional. Model COM7100A, \$2295; IEEE-488 option, \$795.

Kikusui International Corp, 19601 Mariner Ave, Torrance, CA 90503. Phone (800) 545-8784; in CA, (213) 371-4662.

Circle No 461



BATTERY SCOPE

- 60-MHz oscilloscope runs from battery
- Unit fits into briefcase

The LBO-315 60-MHz is a dual-trace, delayed-sweep scope that measures $3 \times 9 \times 11\frac{3}{8}$ in. The instrument runs from a built-in 12V battery, a 10 to 20V dc external source, or 85 to 264V ac (without switching). When powered by ac voltage, the scope operates from 50- to 400-Hz power. \$1850.

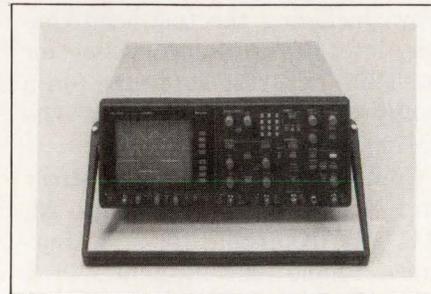
Leader Instruments Corp, 380 Oser Ave, Hauppauge, NY 11788. Phone (800) 645-5104; in NY, (516) 231-6900. TWX 510-227-9669.

Circle No 437

DIGITAL SCOPE

- Digital scope has 200-MHz analog bandwidth
- 10-bit digitizer catches 250M samples/sec

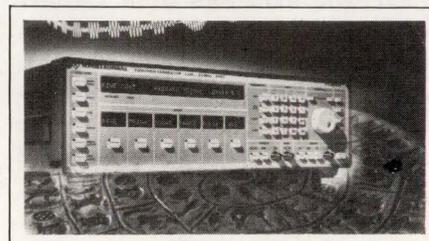
The dual-channel Model PM3320 digital oscilloscope has a pair of 512-sample, CCD-based A/D converters



with 10-bit resolution. The scope can capture data at 250M samples/sec. It has two 2048-sample memories (in single-channel mode, it has one 4096-sample memory) and can operate in repetitive-sampling or single-shot modes. The instrument has simple, built-in math functions, and its CRT features cursor and scope-setting readouts. IEEE-488 and RS-232C interfaces are optional. Model PM3320, \$9,900. Delivery, eight weeks ARO.

Philips Test & Measuring Instruments Inc, 85 McKee Dr, Mahwah, NJ 07430. Phone (201) 529-3800. TWX 710-988-5348.

Circle No 438



FUNCTION GENERATOR

- Provides standard and user-definable output waveforms
- Includes burst, sweep, and internal/external modulation modes

Covering the frequency range from 1 μ Hz to 20 MHz, the AFGU arbitrary-function generator produces sine, triangular, square, trapezoidal, and pulse waveforms. An option extends the TTL/CMOS pulse-output capability to 50 MHz. In addition, you can use 4k words of internal memory to define your own output waveforms with 10-bit amplitude resolution. You can define the start and stop addressing for this memory, so you can generate

INSTRUMENTS

segments of stored waveforms or hold several different waveforms at one time. You can select the sampling period of the memory to be between 100 nsec and 327.6 sec; this feature allows you to generate output frequencies as high as 3.33 MHz. The output amplitude can vary from 0 to 30V p-p, and you can switch the generator's output impedance between 50Ω and $<5\Omega$. The instrument's operating modes include continuous, gated, burst, half-cycle burst, harmonic frequency, and subharmonic frequency outputs, and you can perform linear or logarithmic frequency sweeps. The unit's modulation modes include internal or external FSK and pulse modulation and external AM, FM, and VCO modulation. DM 18,500.

Rohde & Schwarz GmbH & Co KG, Muhldorfstrasse 15, 8000 Munich 80, West Germany. Phone (089) 41290. TLX 523703.

Circle No 453

Rohde & Schwarz-Polarad Inc, 5 Delaware Dr, Lake Success, NY 11042. Phone (516) 328-1100. TWX 510-223-0414.

Circle No 439

68HC11 DEVELOPER

- ROM emulators support 68HC11 development
- Module works with either DIPs or PLCCs

The PAK68HC11 personality module for the 68HC11 single-chip μ P works with the company's UDL, Unilab II, and Optilab emulators. The personality module is available for either DIPs or PLCCs. The supporting software allows full access to all the μ P's registers and ports. Model PAK68HC11, \$555; emulators, from \$2995 to \$7000.

Orion Instruments Inc, 702 Marshall St, Redwood City, CA 94063. Phone (415) 361-8883. TLX 530942.

Circle No 440

Dumb keyboards. Smarter buys.



These new ASCII encoded keyboards from Cardinal Technologies are ideal for hostile working—and pricing—environments. And now they're upgraded with both parallel and serial outputs for even more flexibility.

Made in
U.S.A.

Feature for feature, dollar for dollar, Cardinal KB600 Series keyboards are smart money buys. ASCII encoding saves integration costs, and high quality and reliability keep these keyboards out in the field, not in the shop.

KB600 Series features include: spillproof, dustproof, unitized keypads; flexible membrane switches with a contact life rated at 10,000,000+ operations; finger-positioning overlay with positive, light-touch keys; high noise immunity integrated circuitry; 5V DC operation.

Both parallel and serial outputs are standard. Fully encoded 128 character alphanumeric ASCII keyboard with 58 light touch keys (plus 16 on KB671), and two user-definable keys. N-key roll-over reduces errors during data entry. Auto-key repeat.

CMOS and TTL compatible parallel output capable of driving two loads.

Three separate asynchronous serial data output modes: EIA RS232C compatible; 20mA current loop; TTL. Switch selectable format. Eight switch selectable baud rates: 110 to 19.2K. Power on/system busy LED.

Cardinal KB600 pricing gives you a competitive edge—along with Cardinal quality, proven performance, and high reliability.

Make a Smart Buy. Call 800-722-0094 (717-295-6922 in PA) for more information or to order. Or write: Cardinal Technologies, Inc., New Holland Avenue, Lancaster, PA 17604-7628.

CARDINAL
TECHNOLOGIES, INC. 

Regulation handbook

Compliance Engineering 1987, a 305-pg reference handbook, lists and explains the US regulations governing the production of electronic products. The four main sections on EMI, ESD, Product Safety, and Telecommunications present such topics as radiation hazards, setting up an open-field test site, an overview of the ESD industry, selling safely overseas, and understanding product-liability law. The two final sections consist of related topics and directories.

Compliance Engineering, 593 Massachusetts Ave, Boxboro, MA 01719.

Circle No 441

Brochure details hybrid unit

The 8-pg publication describes the MIL-STD-1553B dual redundant remote-terminal unit. The brochure contains an illustration and a description of the unit, as well as an outline drawing, schematics, detailed lists of specifications and characteristics, and pin functions.

Stantel Components, 636 Remington Rd, Schaumburg, IL 60195.

Circle No 442

Data book features A/D and D/A converters

The 320-pg book, *1987 Data Converters and Voltage References*, describes 27 A/D converters (including

16 new devices), 20 new D/A converters, and 11 voltage references. It includes a complete product listing, converter selection guides, and a section on packaging information.

Maxim Integrated Products, 510 N Pastoria Ave, Sunnyvale CA 94086.

Circle No 443

Article reports on vapor-phase process

This 3-pg reprint, *Thermosets Survive Vapor-Phase Soldering*, explains how components molded of diallyl phthalate (DAP), diallyl isophthalate (DAIP), and resol (1-step) phenolic withstand the rigors of vapor-phase soldering. It contains a 5-part diagram and two tables.

Rogers Corp, 1 Technology Dr, Rogers, CT 06263.

Circle No 444

Brochure covers services of research laboratory

This 8-pg booklet, *Where Problems and Solutions Come Together*, describes the variety of in-house contract services the company provides to manufacturers of electronic equipment and systems. It also outlines ancillary manufacturing services and discusses several company projects, ranging in size from pc boards to coiled-steel handling equipment with a 100,000-lb lifting capacity.

Missouri Research Laboratories Inc, Box 186, St Charles, MO 63301.

Circle No 445

Coupling Information	23	Component & Accessories	47
TVROs and Sintering	43	Linear Devices & Bandpass Filters	18
Filtering Standards & Receiver Noise	82	SPATV Cable System Distribution Filters	18
Filtering Block Diagrams & Receiver	88	Message Logging	20
Block Diagrams & Receiver	19	Start-Up & Receiver Setup	20
Block Diagrams & Receiver	21	Receiver Components & The	21
Block Diagrams & Receiver	22	Component & Accessories	22
Block Diagrams & Receiver	23	Block Diagrams & Receiver	23
Block Diagrams & Receiver	24	Block Diagrams & Receiver	24
Block Diagrams & Receiver	25	Block Diagrams & Receiver	25
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Catalog lists over 500 receivers for TI suppression

The MTV/87 catalog, *Filters, Data and Services for Suppression of Terrestrial Interference for C-Band TVROs (Earth Stations)*, lists more than 500 receivers and tells how to filter them. It features diagrams for standard and block down-conversion receivers that show where interference can affect the system and the choice of filters to solve the problem. Further, it includes descriptions of equipment for TVRO installations; a line of cable system distribution filters; and uplink/downlink bandpass filters.

Microwave Filter Co Inc, 6743 Kinne St, East Syracuse, NY 13057.

Circle No 446

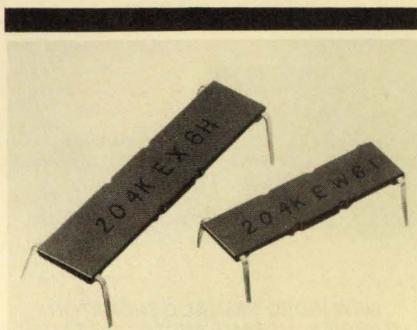
Continued on pg 324

EDN June 25, 1987

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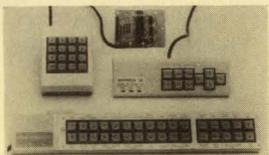


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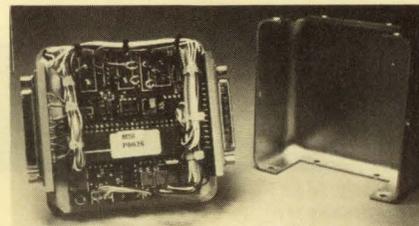
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Measurement Systems, Inc.
121 Water Street, Norwalk, CT 06854
(203) 838-5561

CIRCLE NO 327

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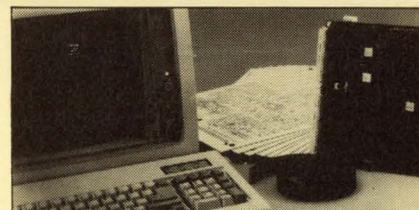
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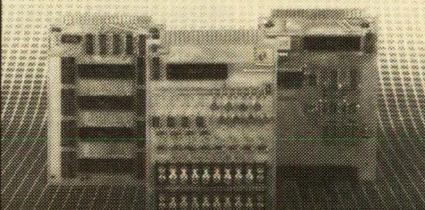
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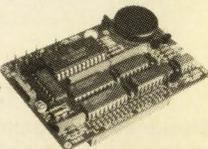
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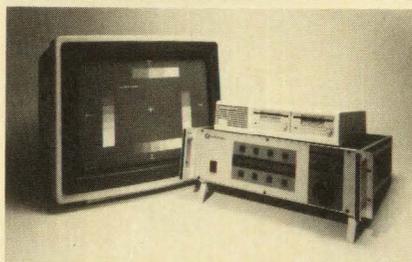


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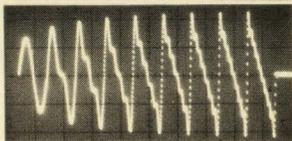
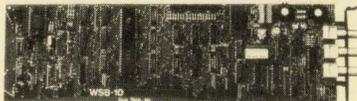
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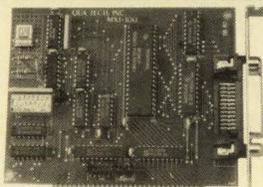
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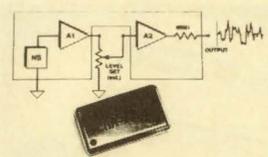
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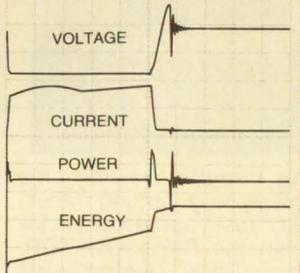
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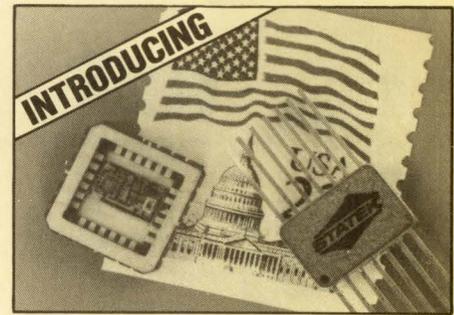
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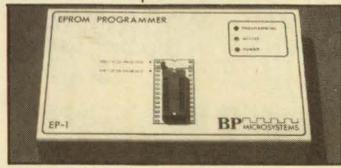
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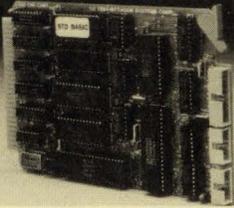
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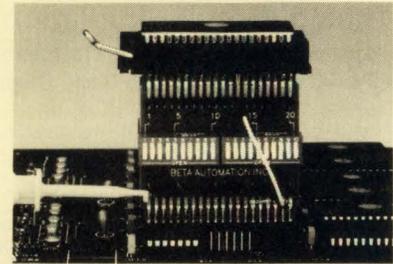
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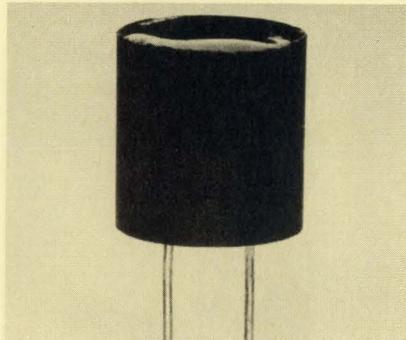
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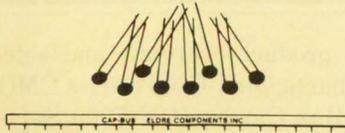
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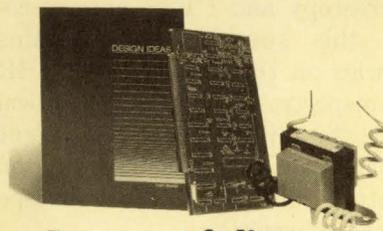
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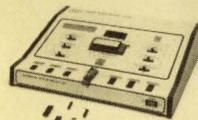
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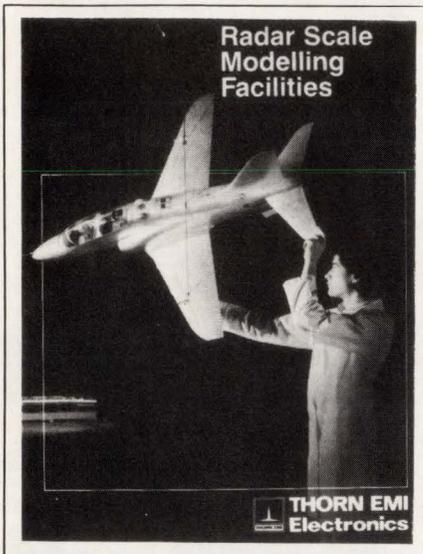


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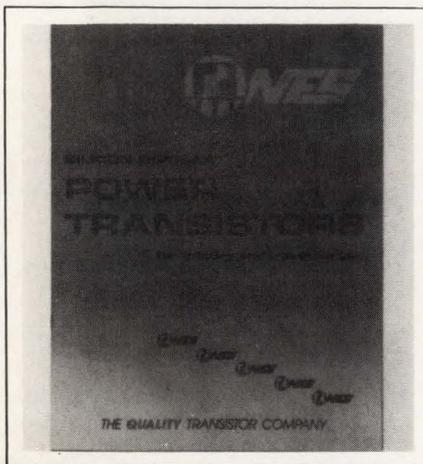


Radar scale-modeling facilities examined

This 4-color, 8-pg booklet, *Radar Scale Modelling Facilities*, comprises five sections. The first section introduces the UK National Scale Modelling Centre. The other four look at the principle of radar scale modeling, the Centre's measurement ranges, its scale models, and the theoretical studies the Centre offers.

Thorn EMI Technology Inc,
8601 Dunwoody Pl, Atlanta, GA 30338.

Circle No 447



Silicon power transistors listed

This catalog features silicon bipolar power transistors and power Darlington for military and industrial

use. It provides maximum ratings and performance specifications for more than 400 of the company's standard npn and pnp models. The 20-pg publication includes sections on power-transistor technologies and the company's military qualification program.

New England Semiconductor,
Box 514, Billerica, MA 01821.

Circle No 448



Newsletter reports on IR microspectrometry

The Spring 1987 issue of *Scan Time* is part of a continuing report on developments in IR/FT-IR. In addition to a report on the uniting of microscopy and FT-IR spectroscopy, this special issue contains articles on the development of IR microspectroscopy as an analytical tool, the optical theory of recent advances in the field, and tips on photo documentation of microscope image information.

Spectra-Tech Inc, Box 2190-G,
Stamford, CT 06906.

Circle No 449

Listing covers STD Bus product line

The 1987 product catalog for the vendor's STD Bus series features low-power CMOS designs for 80C88, Z80, and NSC800 microprocessors. The booklet is divided into five sec-

tions: product overview and selection charts; MSI-C000 Series CMOS STD Bus Cards; MSI-7000 Series STD Bus Cards; MSI-CR Series Card Racks; and other products—IBM PC/XT/AT. A block diagram or illustration accompanies each product. The table of contents lists products in order of appearance, but the catalog pages are unnumbered.

Microcomputer Systems Inc,
1814 Ryder Dr, Baton Rouge, LA 70808.

Circle No 450

Mixed-signal testing evaluated

Taking the position that product quality, time to market, factory productivity/ft², and profit margin are business objectives of every electronics manufacturer, the 20-pg brochure, *Ninety: Five Ways to Manage Integrated Testing*, addresses manufacturers' concerns about mixed-signal testing. The five subjects covered in the 4-color brochure include choices of test instrumentation, single-language software, test-system calibration techniques, test-system support strategies, and factory-automation tools.

LTX Corp, LTX Park at University Ave, Westwood, MA 02090.

Circle No 451

Brochure highlights manufacturing services

Eight Examples of How MRL Helps Companies Compete is a 12-pg brochure that provides examples of the services offered by the company. It discusses how to lower fabrication and manufacturing costs, and how the company helps telephone companies, equipment manufacturers, defense contractors, candy vendors, medical companies, and electronic companies compete. Also included is a list of metal fabrication and electronic services, and a reply card.

MRL, 3800 W Clay St, Charles, MO 63301.

Circle No 452

Programmers gain control of their designs through changes in copyright law

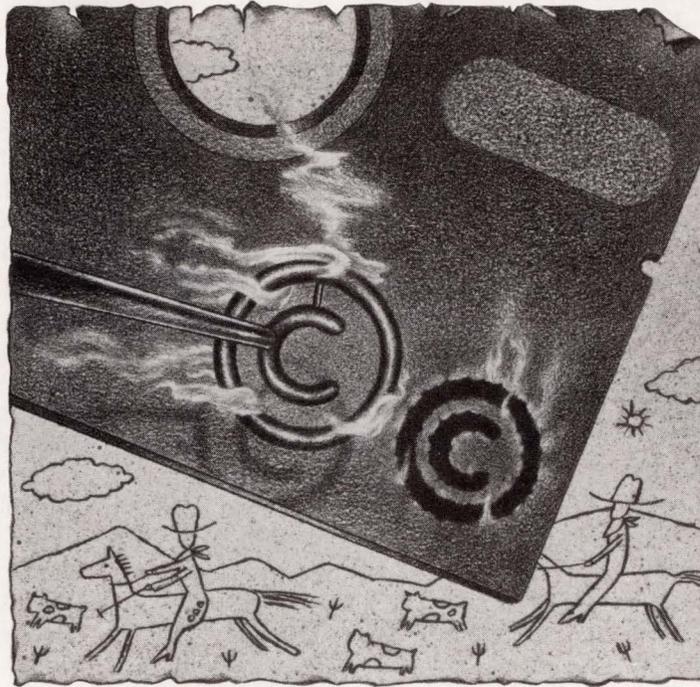
Joseph Iandiorio,
Waltham, MA

No doubt the hottest legal topic in the electronics industry is the subject of software copyright. Last fall, software makers announced that they were abandoning such restrictive measures as shrink-wrap licenses and protective hardware locks and keys. Instead, they would return to the traditional methods of product protection: copyright, patent, and trade-secret status. Now it appears

that the software makers are using these traditional devices to try to force companies that sell lower-priced software clones out of the market by suing them for copyright infringement. These clones are programs that, in the latest legal jargon, "look and feel" like more expensive copyrighted programs. Lotus Development Corp, for example, is claiming that Mosaic Software's Twin program is basically a copy of 1-2-3. How successful this tack will be for the larger software makers remains to be seen, as the cases are still in litigation.

Copyright has not always been the powerful tool for software protection that it is now. For many years, the court system struggled with the question of how—and if—the copyright system could accommodate software's specific requirements. Only recently has copyright given software programmers protective powers over their designs.

Because copyright traditionally protected authors' works, and not utilitarian objects, the courts were at first reluctant even to consider copyright protection for such commercial things as computer programs. The original purpose for copyright protection was to allow authors and composers to make their work public while still retaining ownership of it. When early programmers began submitting their programs for copyright, the Copyright Office in Washington, DC, chose to accept them and leave to the courts the final decision on



Lisa Adams

the validity of such protection for software.

Because copyright was meant to protect an expression's form, not the underlying concept, early analyses identified four programming steps—the flow chart (or algorithm), source code, assembly code, and object code—and found that only the assembly code was copyrightable. Flow charts and source code were considered unsuitable for copyright because they merely represented the program's logic, which wasn't protected by

copyright. Object code wasn't protectable because it was machine language, which was not understandable by man, and so not the work of an author, as copyright law requires.

The position that source code and object code weren't copyrightable soon gave way, as more people filed court cases claiming they were. Further, the courts also decided that copyright could protect not only source and object code, but even the machine language stored in ROM on a circuit board. For example, makers of printed-circuit boards have been enjoined from supplying boards to a fabricator that used them to make video games that infringed upon the copyrights of other parties.

The courts also decided that copyright law should also protect both programs that directly interact with the user, such as application programs, and those that only manage the computer's internal operation, such as operating systems or housekeeping systems. Even databases are protectable by copyright; any copying of someone else's database into or out of a computer is a copyright infringement.

Yet despite this seemingly widening path of copyright protection for software, much of what was innovative about a software program remained unprotected until just two years ago. Although the court system had begun to sanction expanded protection for software,

before 1985 its understanding of software development remained unclear.

At that time, copyright law did protect the software coding process, which is a comparatively small part of a program's development, but it didn't protect the development of programs' structure and logic or their debugging, documentation, and maintenance, all of which are much more expensive and difficult to create than the code. In fact, a program's algorithm often involves much more creativity and is of greater commercial value than is the program code that implements the algorithm. But because copyright law traditionally viewed an algorithm as the idea behind a software program, the courts saw the algorithm as unprotectable.

In 1985, however, the courts began to be more comfortable with software's technical aspects and with how software fit into the protective realm of copyright. In September of that year, the Massachusetts Federal District Court decided, in *Williams vs Arndt et al*, that computer languages were no different from other spoken or written languages and were therefore subject to the same restrictions.

Over the course of his 15 years as a commodities trader, Harry Williams had developed a trading method that he claimed guaranteed positive results. He taught the method in seminars that cost attendees \$3000 each. In addition to paying the steep registration fee, the attendees were required to sign a nondisclosure agreement. Step-by-step instruction in William's method was also available in a book that he sold for \$2000. When a competitor began selling a computer program that effectively carried out Williams's method, Williams brought suit.

The court that heard Williams's case agreed with him. The alleged infringer's source code was not a new or different expression of ideas, the court found; it was simply a translation of an idea from one language, English, to another language, that of the computer. If the court were to view the program as more than a mere translation of the book, then it would follow that any book could be copied and coded in source code. The court found that although the programmer might have expressed creativity, imagination, and independent thought with respect to the programming task, the system's concept was essentially Williams's.

As the Williams decision demonstrated, not only could copyright law protect software coding, but it could lend protection to a program's algorithm as well. At first blush, this situation seems a bit extraordinary. However, it's true that a painter who creates an oil painting of a copyrighted photograph infringes the copyright in the photograph, in spite of the creativity the painter displayed in rendering the oil painting.

With the Williams decision, the courts were applying the same standards to computer programs.

In the Fall 1986 decision in *Whelan Associates vs Jaslow Dental Laboratory*, the Third Circuit Court of Appeals found that a software program's algorithm was not the same thing as the essential idea behind the program, which is unprotectable. The court held that the *expression* of the idea behind a program is the way the program operates, controls, and regulates the computer in receiving, calculating, and producing information, and this expression includes the underlying algorithm as well as the coding.

After deciding to computerize its complex bookkeeping and administrative tasks, Jaslow Dental Laboratory hired Elaine Whelan to write a program that would perform these tasks. Whelan produced a program that was written in the EDL language and that

worked only on certain IBM machines. She owned the copyright in the software. Subsequently, Jaslow developed a similar program, written in Basic, that ran on a large number of other computers and therefore had greater sales potential. Whelan sued Jaslow for copyright infringement on the grounds that both programs embodied the same basic structure or system; Jaslow claimed that copyright protects only the coding of a program, not the underlying concept.

What Whelan was looking for, essentially, was protection of her algorithm. This was new ground for copyright. In software, protection of a program's algorithm had traditionally been considered to be tantamount to the protection of an idea. The question the court was forced to answer in the Whelan case was whether the algorithm or structure of a computer program is an idea or merely the expression of an idea.

Before Whelan wrote the dental-lab program, she had had to learn about the dental prosthetics trade and the lab's business—for example, how it processed or-

How to file a copyright

In terms of the cost of software protection, copyright is a bargain. It's cheaper, easier, and quicker to obtain than patent protection, and it's easier to enforce than trade-secret status.

The recommended procedure for filing a copyright on a program in the US is to place the standard copyright notice, "Copyright © (year) (owner's name)," on the disks, tapes, and ROMs containing the program, as well as on the accompanying manuals. The notice should also be in the coding, so that it prints out with a listing and appears on the title screen when the program is run. To register a copyright, send the Copyright Office a completed application form and the first and last 25 pages of the listing.

ders, what billing problems arose, and how inventory correlated with orders. After defining the problems, she outlined a solution in the form of a flow chart. A flow chart breaks down the solution to a problem into a series of smaller units, called subroutines or modules, each of which processes elements of the larger problem. A program's efficiency depends in large part on the arrangement of its modules and subroutines.

Once she completed the program's detailed design, Whelan began the coding. The amount of time she spent coding the dental-lab program was small compared with the task of organizing the modules and subroutines, as is the case with all software programs.

The court sided with Whelan, and thus faced the task of defining the idea or concept of a program that is not protectable. The unprotectable portion of the program, said the court, was the simple idea or concept of a computer program for operating a dental laboratory. The court concluded that the detailed structure or algorithm of the program is a part of the expression, not merely the idea, of that program, and therefore the algorithm is protectable along with the coding.

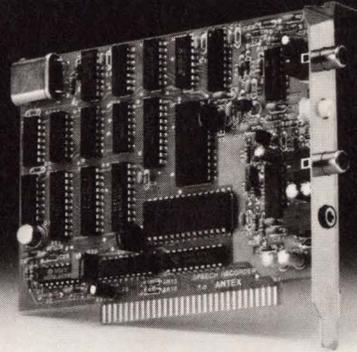
Copyright law's expanded protection for software has been a boon for end users, because as a result of the increased protection, manufacturers have lifted the license and hardware restrictions that users found onerous. Yet the pending copyright litigation between large software makers and the makers of low-priced program clones could again change the industry. If the courts find that the clone makers have infringed on the copyrights of such programs as Lotus Development Corp's 1-2-3, it could mean the end of the software-clone industry. **EDN**

Author's biography

Joseph Iandiorio is a patent, trademark, and copyright attorney in Waltham, MA. He earned a BSEE from Villanova University (Villanova, PA) and a JD from George Washington University (Washington, DC). Before opening his legal practice, he worked for three years as a patent examiner for the Patent and Trademark Office in Arlington, VA. He is a member of the boards of directors of the Small Business Association of New England and the Massachusetts Technology Corp, a state-sponsored venture-capital organization. In 1986, he was a delegate to the White House Conference on Small Business.

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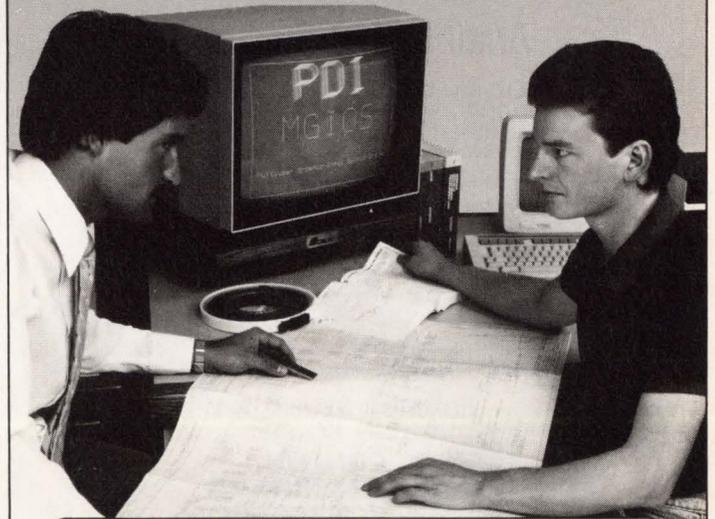
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1987 Editorial Calendar and Planning Guide

EDN

Editorial Emphasis

Issue Date	Recruitment Deadline	Editorial Emphasis	EDN News
July 23	July 2	Product Showcase-Volume II, Computers & Peripherals, Test & Measurement Instruments	Closing: June 25 Mailing: July 16
Aug. 6	July 16	Computer Boards; Digital Signal Processing, Test & Measurement; Top Ten Reader Vote Contest	Closing: July 23 Mailing: Aug. 13
Aug. 20	July 30	Military Electronics Special Issue; Fiberoptics; Software	
Sept. 3	Aug. 13	Analog ICs; CAE; ASICs	Closing: Aug. 20 Mailing: Sept. 3
Sept. 17	Aug. 27	Memory Technology; Communications Technology; Software	
Oct. 1	Sept. 10	Surface-Mount Technology; Computers & Peripherals; Industrial Product Showcase	Closing: Sept. 17 Mailing: Oct. 8
Oct. 15	Sept. 24	Test & Measurement Special Issue; Analog ICs; ASICs	
Oct. 29	Oct. 8	Computers & Peripherals; ICs & Semiconductors; Wescon '87 Product Preview	Closing: Oct. 15 Mailing: Nov. 5
Nov. 12	Oct. 22	Wescon '87 Show Issue; ICs; Computers & Peripherals	
Nov. 26	Nov. 5	Microprocessor Technology Report & Directory; Analog ICs; Sensors & Transducers	

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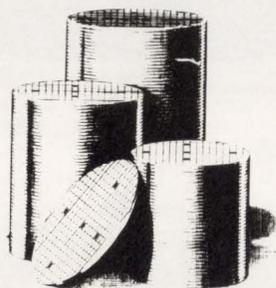
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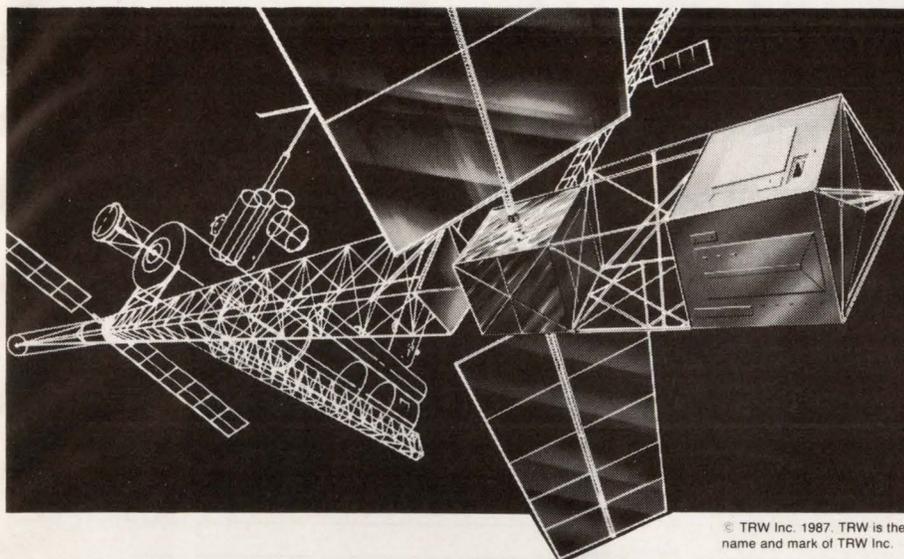
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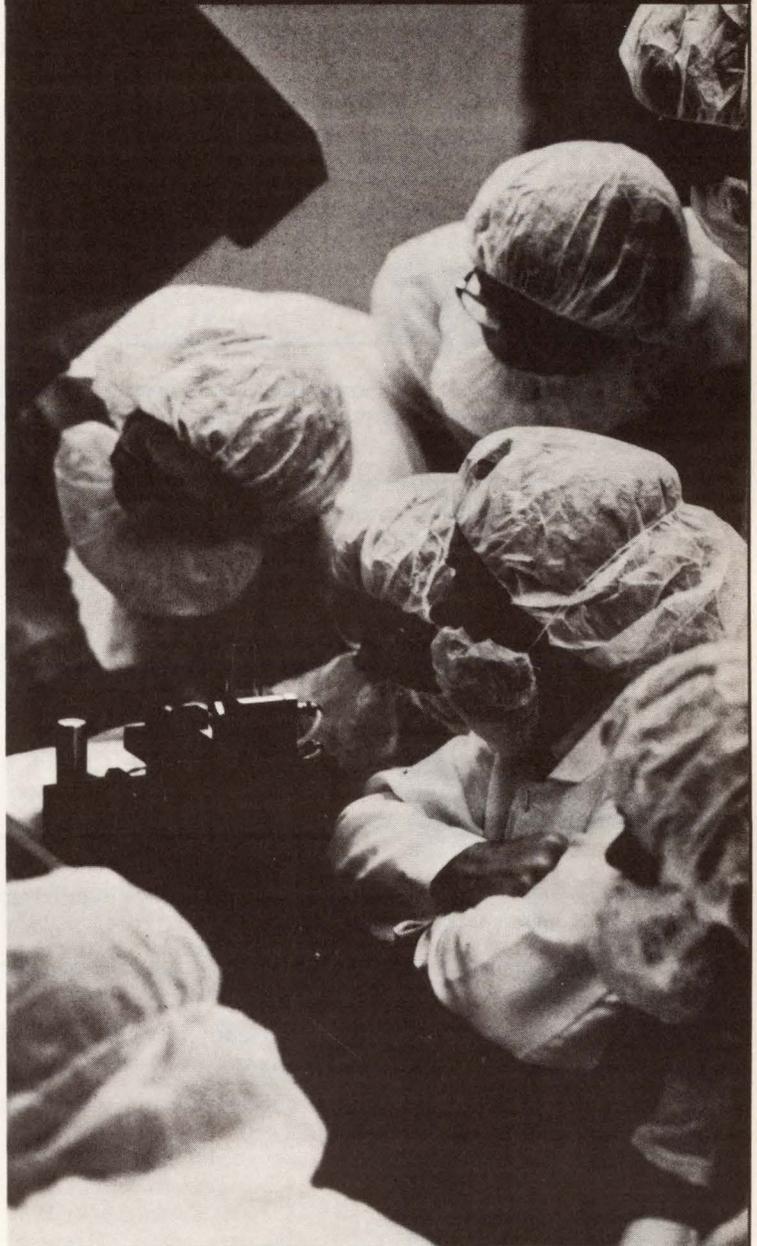
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For Crist, the addition of EDN News, with its Career News section, proves to be an outstanding recruiting resource. "We can reach more readers than ever before in lots of technical disciplines."

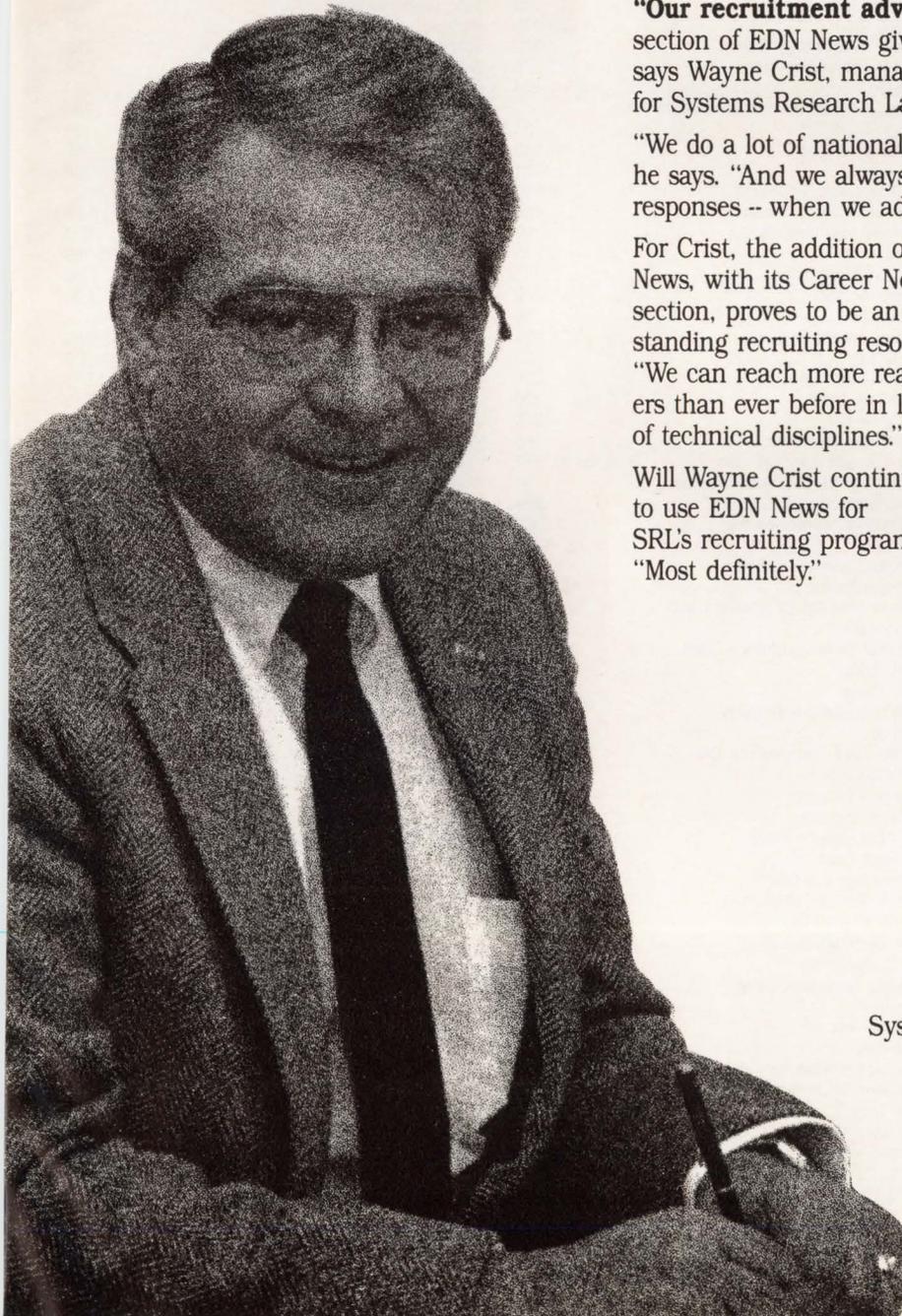
Will Wayne Crist continue to use EDN News for SRL's recruiting program? "Most definitely."



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EDN NEWS

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ADVERTISERS INDEX

ACDC Electronics	152	Hewlett-Packard Co	164	Ready Systems	238-239
Additive Products Div, Kollmorgen Corp*	103	Hughes Aircraft Co/Connecting Devices Div	208	Rifa Inc	285
ADPI	330	Hughes Aircraft Co/Industrial Products	247	Robinson-Halpern	331
Advance Power Supplies Inc*	303	Hypertronics Corp	176	Rogers Corp	266, 286, 329
Advanced Microcomputer Systems	333	I-Bus Systems Inc	316	Rohde & Schwarz**	98
AIE	332	IC Sensors	117	SBE Inc	129
Altera Corp	60-61	ICI Array Technology	217	Scanbe, Unit of Zero Corp	113
Amco Engineering	116	Industrial Devices Inc	310	Scientific Calculations	259
American Automation	96	Information Scan Technology	333	Seagate Technology	44-45
American Shizuki	307	Inland Motor	317	Semiconductor Circuits Inc	192
Amperex Electronic Corp*	68	Inmos Corp	10-11	SGS Semiconductor Corp	56-57
Antex Electronics	341	Innovative Software	333	Sheldahl Inc	267
Augat-Alcoswitch	272	Integrated Circuits*	106	Siecor Corp	195
Augat-Interconnections	330	Integrated Circuits	332	Sierra Power Systems	301
Augat/Telzon & Augat/Melco	153	Intel Corp	77, 78-79	Signal Transformer Co Inc	C4
Automated Images	141	Intergraph Corp	167, 168-169	Silicon Systems Inc	88-89
Basler Electric	333	International CMOS Technology	199	Siliconix Inc	49
Bayer**	14-15	International Rectifier	66	Single Board Systems	323
Bering Industries Inc	156	International Test Conference	224	S-MOS Systems*	104-105
Beta Automation	334	Intusoft	331	Soltec Corp	249
BICC-Vero Electronics Inc	172	IRC Inc	279	Spectrum Software	47
Bomco Inc	308	John Fluke Manufacturing Co Inc	64-65	Sprague Electric Co	35
Bourns Inc	219	Keithley Instruments	46	Stag Microsystems Inc	20
Bowmar/White Technology	203	Kepeco Inc	225-230	Stantel Components Inc	281
BP Microsystems	331	Linear Technology Corp	270	Star Technologies	305
Burr-Brown Corp	183	Linear Technology Inc	76	Statek	331
Buscon	295	Lite-On	314	Stimpson Co Inc	236
Cadic	130-131	Lockheed Electronics/Environmental Test Labs	34	Summation Inc**	205
Cadnetix Corp	264-265	Logical Devices	333	System-General	329
Calnet Electronics	331	LTX Corp	120-121	Tau-Tron Inc	299
Capital Equipment Corp	331	3M Electronic Products	54-55	TDK Corp	196
Cardinal Technologies Inc	327	Macmillan Software Inc	188	TEAC Corp**	160
Case Technology	237	Marconi Instruments*	107	Tektronix Inc	36-37, 101-102
Casio Inc	261	Masscomp	30-31	Teledyne Semiconductor	222-223
Cherry Electrical Products Inc	25	Matsuo Electronics	304	Teradyne Inc	28-29
Chinon America Inc	309	Maxiconn Inc	202	Termiflex Corp	304
C&K Components Inc	6	Maxtor	58	Thomson Components-Mostek*	108-109
Comlinear Corp	191	Measurement Systems	329	Toshiba America Inc/Memory Div	94-95
Computer Parts Mart	333	Medinova	330	Union Carbide Corp/Electronics Div	290
Conor-Winfield Corp	48	Mepco/Centralab	289	United Technologies Microelectronics Center	159
Conversion Devices	334	MetaLink Corp	320	Universal Data Systems	C3
Cooper Tools*	43	Microtek Lab	240	Valid Logic Systems Inc	12-13
Corning Electronics	42	Microware Systems Corp	48	Vector Electronic Co	118
Cybernetic Micro Systems	315	Mini-Circuits Laboratories	3, 4, 26-27, 275	VideoLog Communications	263
Cyborg	184	Mitsubishi Electronics America Inc/Semiconductor Div	287	Visionics	330, 332
Cypress Semiconductor	23	Monolithic Memories Inc	C2	VLSI Technology Inc	50-53, 178-179
Dale Electronics Inc	1	Motorola	39, 40-41	Walker Power	288
Dash, Straus, and Goodhue	2	Motorola Semiconductor Products Inc	163, 171	Wintek	330, 333
Data Display Products	315, 317, 319	Murata Erie North America Inc*	98	Xilinx	142-143
Datel	82	Nanomask**	68	Zilog Inc	277
DeGussa	38	National Semiconductor Corp	132-133		
Dek Inc	284	NCR Corp	187		
Design Computation	329	NEC Corp	154-155		
Dialight Components	180	Nichicon (America) Corp*	160		
Digital Electronics	268	Nicolet	331		
Digital Equipment Corp*	125	Nicolet Test Instruments Div	291		
Digital Research Inc	75	Nova Sensor	112		
Du Pont Co	62-63, 206-207	Octagon Systems	332		
EG&G Reticon	302	Ohmite Mfg Co	221		
EH Titchener	332	OrCAD Systems Corp	119		
Elantec Inc	8	Outlook Technology	311		
Eldre	333	Philips Elcoma Div**	18-19		
Enertec Inc**	125	Philips Test & Measuring Instruments Inc**	43		
Epotek Corp	313	Pico Electronics Inc	300		
ETA Circuit Breakers	329	Planar Systems	73		
Excel	16-17	Plessey Semiconductor	200		
Ferranti Electric	296	Polytron	333		
Force Computers Inc	32-33	Powerex Inc	292-293		
Ford Microelectronics	115	Powertec Inc	262A-D		
Fujitsu Components of America Inc*	110	Precision Diversified Industries	337		
Fujitsu Microelectronics Inc*	14-15	Precision Monolithics Inc	84		
FutureNet/Div of Data I/O	283	Qua Tech	330		
Galagraph	334	Quantum Data	330, 332		
General Instrument	297	Racal-Redac	126, 127-128, 269		
Genest Technology	329	Rapid Systems	87		
GE/RCA Solid State	91, 92-93	Raytheon	71		
Global Technologies	46				
Hamamatsu Corp	312				
Harris Semiconductor Products	175, 250, 298				
Heurikon Corp	90				

Recruitment Advertising

Clinton Electronics	338, 342
Digital Equipment Corp	340-341
Kollman	339
Micron Technology	345
SCI Systems	338
Sherwood Medical	342
TRW, Div BMD & Mead	343

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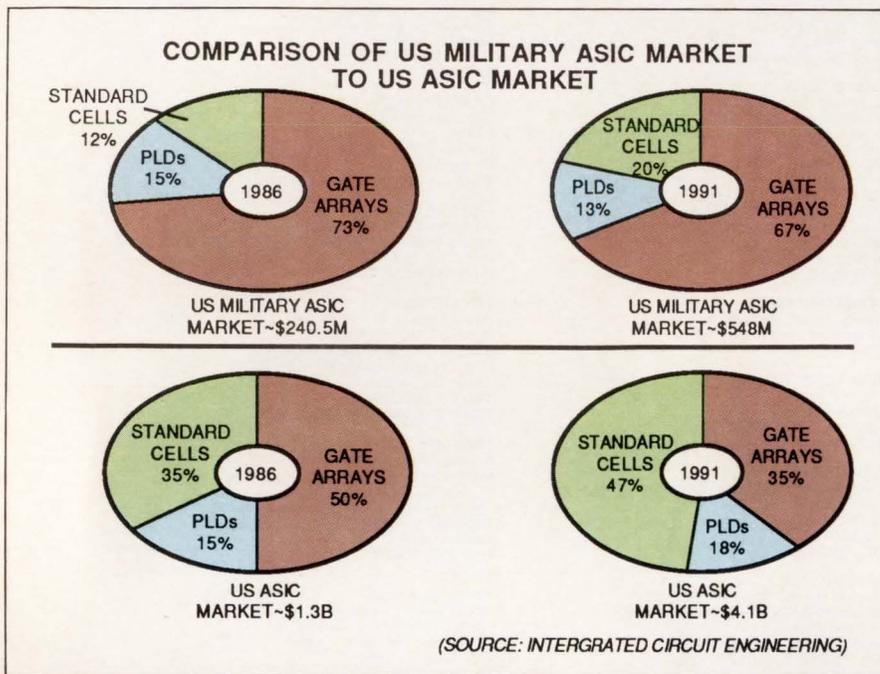
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LOOKING AHEAD

EDITED BY CYNTHIA B RETTIG



Military-ASIC market grows at 18% rate through 1991

ASICs (application-specific ICs) should enjoy an average annual growth rate of 18% in the military market through 1991. To arrive at that figure, Integrated Circuit Engineering Corp (Scottsdale, AZ) projected the annual growth rate for the three segments: Semicustom devices (gate arrays and linear arrays) should grow at a 17% rate annually, programmable logic devices should average 15%, and standard-cell devices will grow the fastest at 30%. ICE then calculated the cumulative average of these rates to reach its 18%. (These figures include the nonrecurring engineering fees and development costs for gate arrays and standard cells.)

Gate arrays will continue to claim the largest portion of this market. ICE believes the flexibility of their design, combined with their high performance and comparatively quick turnaround times, will keep gate arrays desirable for military applications. Although gate arrays will dominate the military-ASIC market, their share of the general US ASIC market will decline

15% by 1991—partly because of offshore fabrication and assembly.

Because no standards exist for military gate arrays, OEMs currently use source control drawings to avoid qualifying each design. The absence of standards also substantially increases the liability of manufacturers if equipment fails. Standards are on the horizon, however: As soon as the Rome (NY) Air Development Center completes its generic military standard for gate arrays, JAN qualifications will be possible.

Although the standard-cell market will grow the fastest, it is only expected to total \$110 million in 1991, in comparison with about \$378 million for gate arrays. The time and expense involved in making standard-cell designs are the major constraints on their popularity. By 1991 programmable logic devices will claim a market of \$67 million.

ICE generalizes that military ICs broadly reflect commercial IC trends, but also finds that the importance of long life span to the military tilts the scales considerably in favor of devices based on bipolar technology. In 1991, the total US market for gate arrays will divide

into 76% for CMOS and the remaining 24% bipolar. In contrast, the military gate-array market will split 60% and 40% for CMOS and bipolar devices, respectively.

Optical-storage market ready to burgeon

Optical disk drives are finally going to make an impact on the marketplace they share with magnetic media, microform, and paper, according to Electronic Trend Publications (ETP), a market-research company located in Saratoga, CA. Despite having fallen well short of bright predictions for the past several years, the market for optical-storage systems and media will grow from its present 1% of the overall information-storage market to 4.7% by 1991. That change will translate into a tenfold increase in dollar value of \$17.889 billion in 1991.

ETP discerns various signs of the coming boom. For one, IBM, when it introduced its latest personal computer this past spring, announced a WORM (write-once read-many) option for the system. What's more, software has at last been developed that can tie a WORM drive into some major operating systems. The software requires minimal modification or none at all.

One reason for the strong and stable interest in optical-disk storage is its promise to automate more effectively offices still groaning under the weight of paper-based information systems. That promise has manufacturers of 12-in. disk drives facing an order backlog. And related subsystem manufacturers are now selling add-ons for major computer systems by IBM and Digital Equipment Corp. In the exclusive-of-paper storage market shared by optical disks, microforms, and magnetic media, ETP predicts that optical storage will dramatically increase its market share from 7% in 1987 to 32% by 1991.

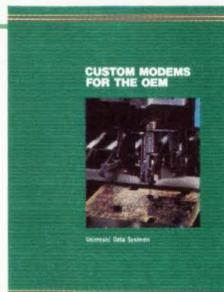


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While this imitation may be flattering to us, it could be extremely risky for you. After all, just because a transformer looks like Signal's doesn't mean it will perform like Signal's.

Our *innovation, creativity and reliability* are one-of-a-kind. We pioneered the high isolation split bobbin design.

Now our exciting new *VDE certified International Series* takes another leap forward with a dual, high-temperature bobbin and insulating shroud that provides significantly better performance at lower costs than ever before. *One-4-All™* and *More-4-Less™* transformers are so reliable they meet – or surpass – every important international specification (UL, CSA, VDE and IEC).

We also introduced low-profile, *Flathead™* plug-in transformers. Our latest series, available in five sizes, is arguably the best in the industry. The innovative non-concentric windings eliminate the need for



an electrostatic shield and feature hum-bucking construction.

Beyond that, Signal has a full line of superior low power *PC board transformers*, as well as smaller-than-ever "2-4-1" *Series*, competitively-priced rectifier *power transformers*, *chokes* and industrial-grade step-up and step-down *power isolation transformers*.

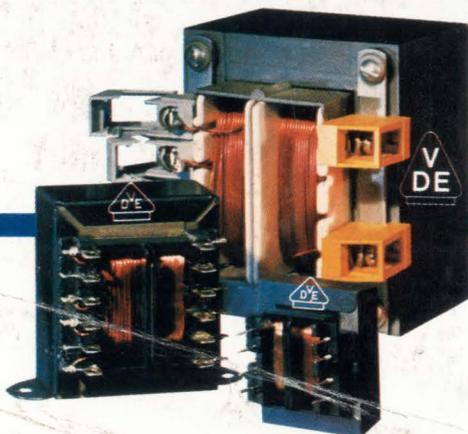
We maintain significant levels of our stock transformers and sell direct – without a middleman to slow things down – or mark prices up. Even better, we can ship to you in quantity within just 24 hours. We call it our *PRONTO service...* and it's unique in the industry.

Just let our competition try to play "follow the leader" with that!

Of course, if we don't have a standard stock item that fits your needs, our *custom engineering* department will gladly quote your specific requirements. *PRONTO.*

But for you, it's easy to follow our lead. Simply send for our complete, free catalog by contacting: Signal Transformer, 500 Bayview Avenue, Inwood, NY 11696.

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