A CAHNERS PUBLICATION

APRIL 15, 1987

EDN

High-speed digital CMOS IC families

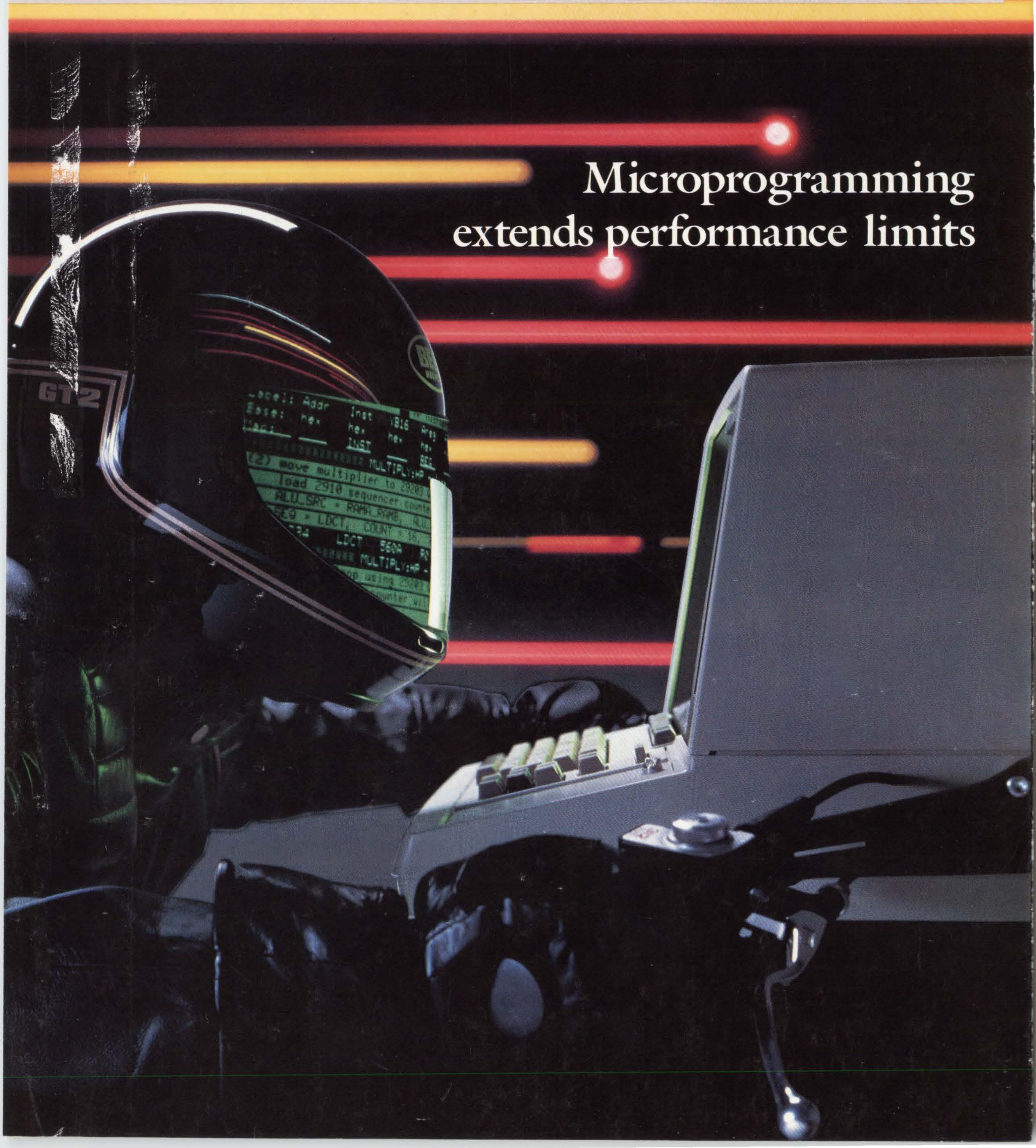
Software development for 8-bit μPs

Structured array ICs

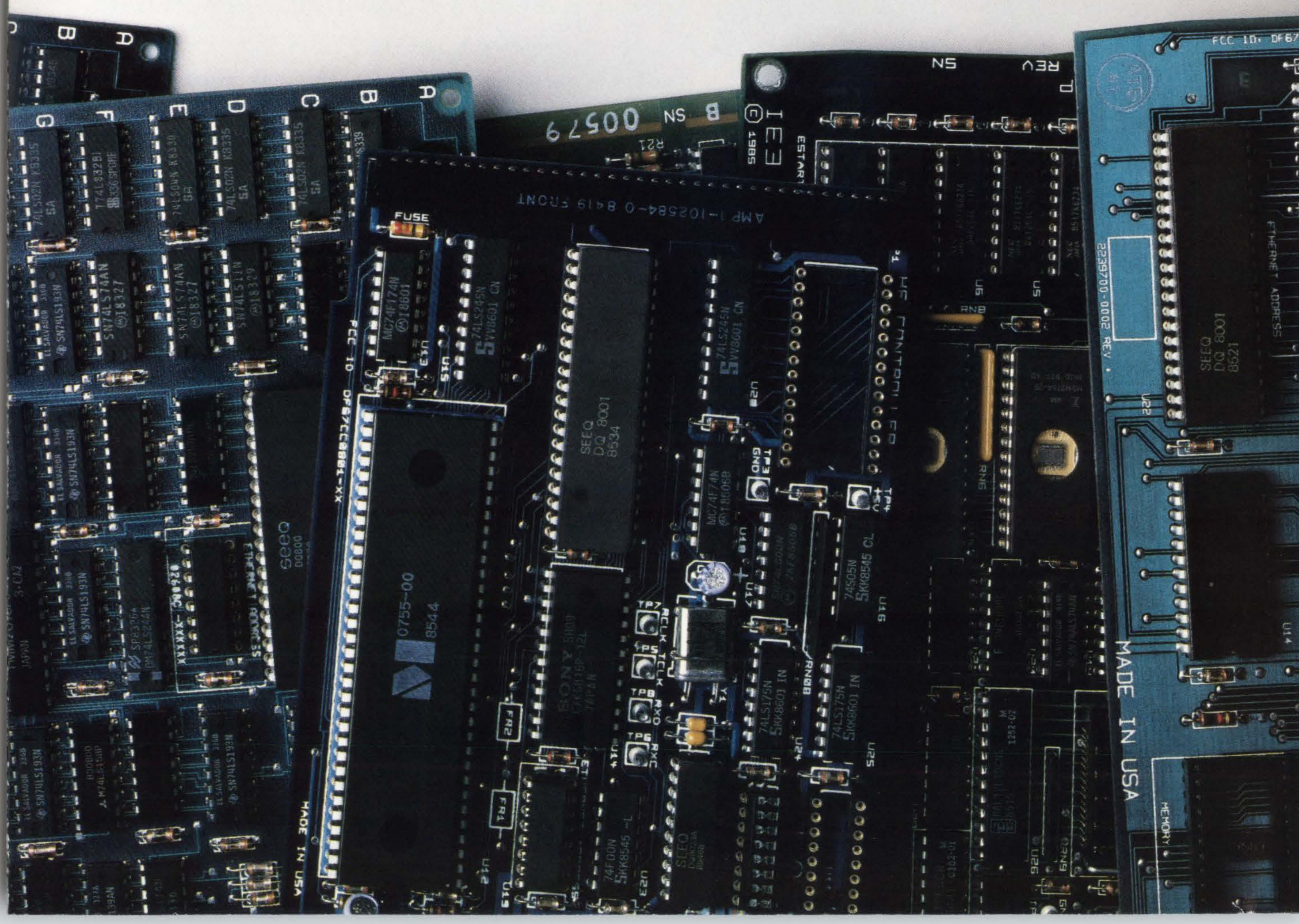
Designing for testability

External power supplies

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS



HOW TO AVOID GOING OVERBOARD.



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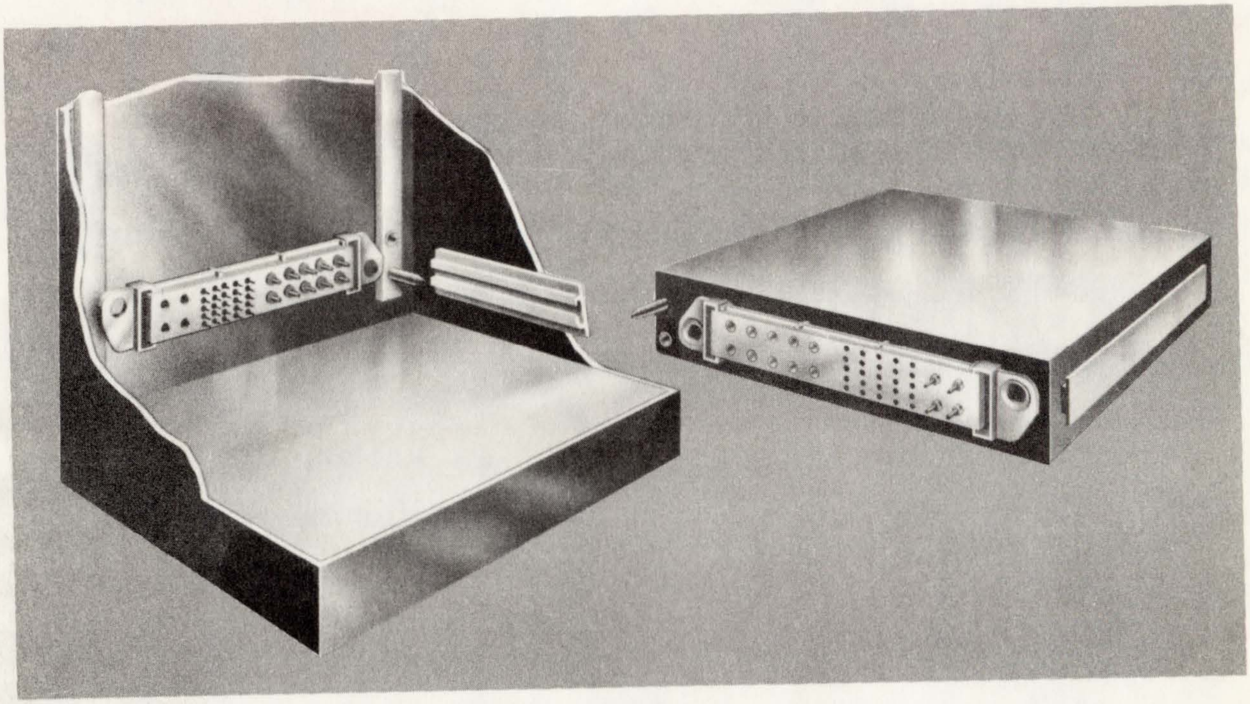

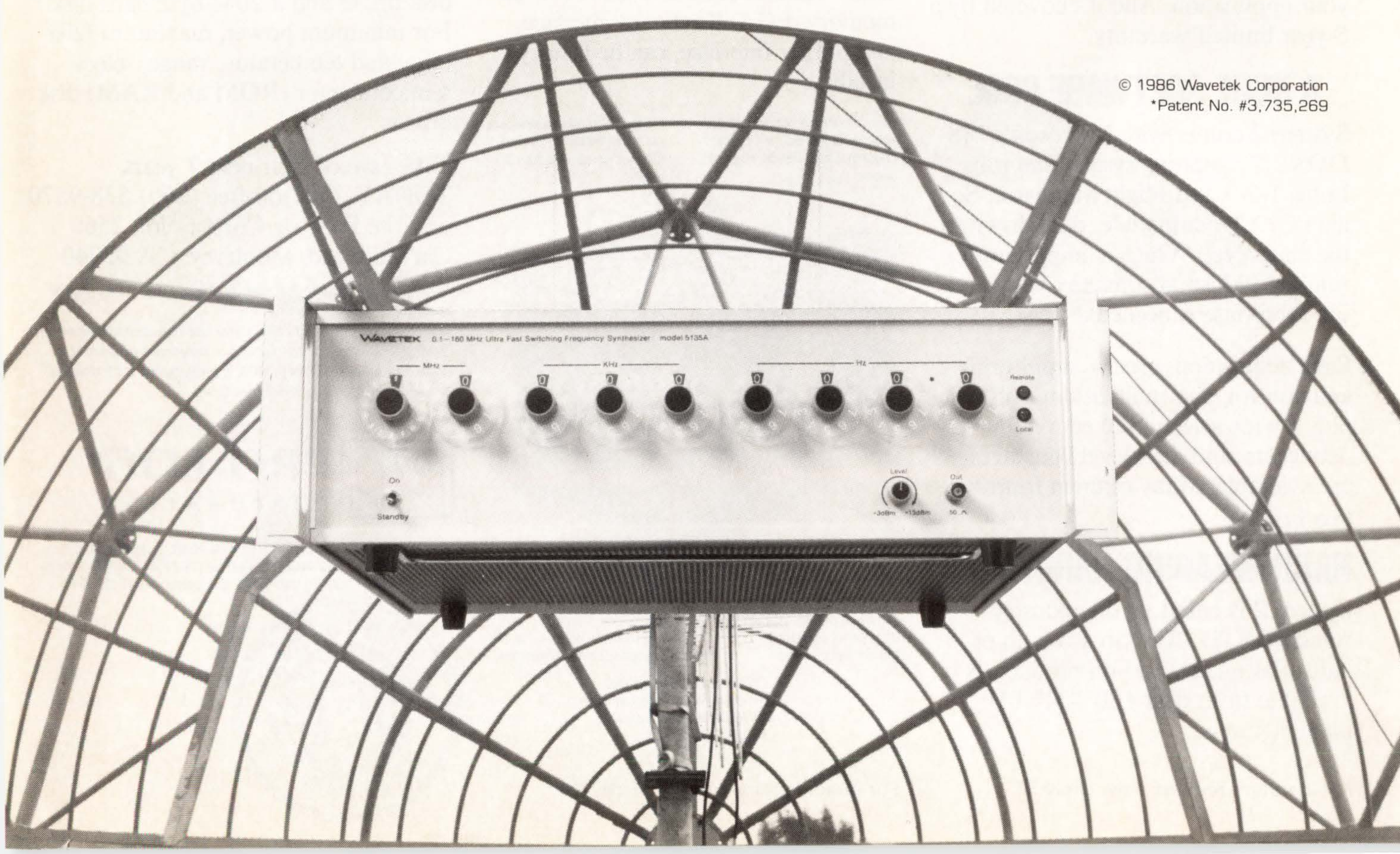

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THIS PC/XT-COMPATIBLE INDUSTRIAL COMPUTER MAY HAVE ONE FAILING...EVERY 7 YEARS.

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A HUGE SOFTWARE POOL

System 2 comes with Microsoft's MS-DOS 3.2 operating system and runs **Lotus 1-2-3** and **Flight Simulator**. So it's PC/XT-compatible, right down to the chip level. Which is important for running industrial software, where real time response is needed.

Data acquisition, process monitoring and control, and multitasking software, plus a wide selection of editors, debuggers, and high-level languages are available. Many of them from Pro-Log.

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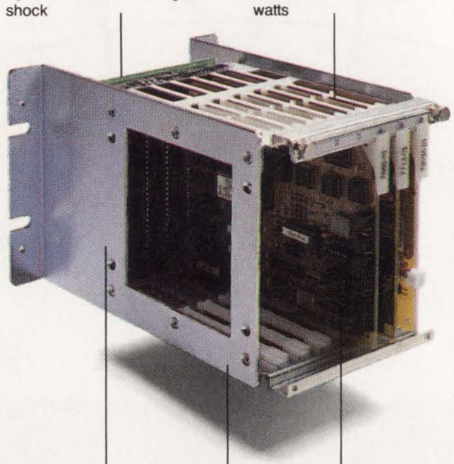
System 2 is based on the industry-standard STD BUS. So a wealth of industrial quality add-on products is available from over 100 STD BUS manufacturers.

PLUS ROOM TO EXPAND

You expand System 2 by simply plugging in additional STD BUS cards. Up to 23 expansion slots are available and many options, such as 640K bytes of memory, EGA/Keyboard interface, and printer interface, can be factory installed.

Grew up in the school of hard knocks. Secured on 4 sides, System 2 withstands 10gs of shock

No fan or heat sink needed, could be battery powered. Consumes as little as 1.25 watts



Works in places you wouldn't. 0° to 65°C operating temperature range

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*Thermal and mechanical specifications are reduced by the use of mechanical disk drives.

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PL055

INDUSTRIAL COMPUTERS PRO-LOG IN CONTROL QUALITY

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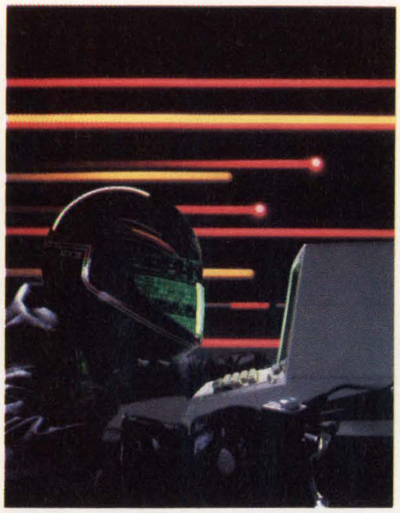
Volume 32, Number 8 EDN April 15, 1987

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS



On the cover: *Microprogrammable designs can outrun even the fastest 32-bit fixed-instruction-set μPs. What's more, development tools are making the bit-slice parts easy to program. See pg 142. (Photography by Reg Francklyn, art direction by Bob Rodgers, courtesy Hewlett-Packard)*

DESIGN FEATURES

Continued on page 7

BPA ABP

EDN (ISSN 0012-7515) is published 38 times a year by Cahners Publishing Co, a Division of Reed Publishing USA, 275 Washington Street, Newton, MA 02158. William M Platt, President; Terrence M McDermott, Executive Vice President; Jerry D Neth, Vice President of Publishing Operations; J J Walsh, Financial Vice President/Magazine Division; Thomas J Dellamaria, Vice President Production & Manufacturing; Frank Sibley, Group Vice President. Saul Goldweitz, Chairman; Ronald G Segel, President and Chief Executive Officer; Robert L Krakoff, Executive Vice President. Circulation records maintained at Cahners Publishing Co, 270 St Paul St, Denver, CO 80206. Second class postage paid at Denver, CO 80202 and additional mailing offices. Postmaster: Send address changes to EDN, 270 St Paul St, Denver, CO 80206.

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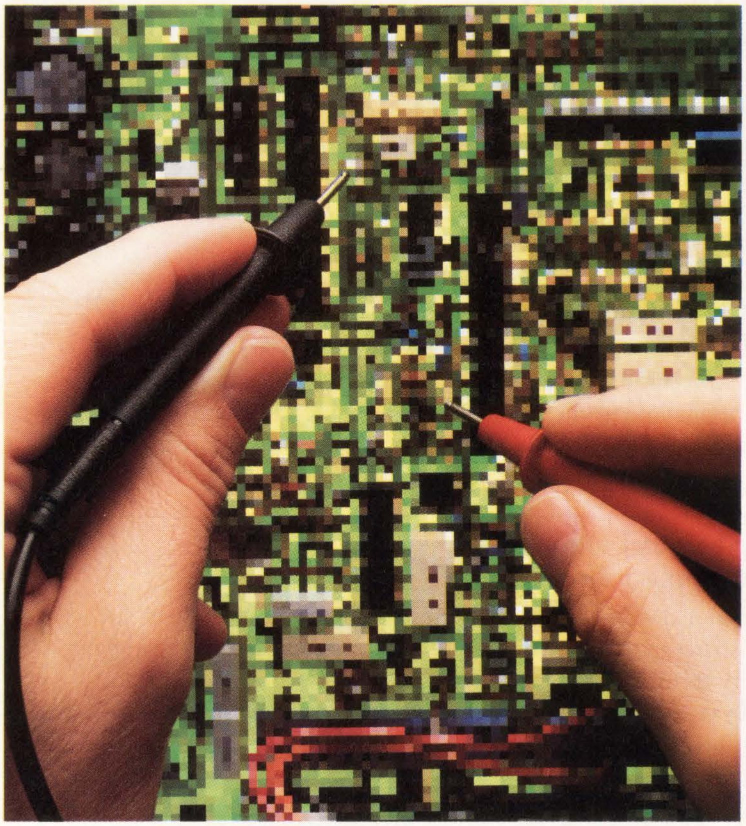

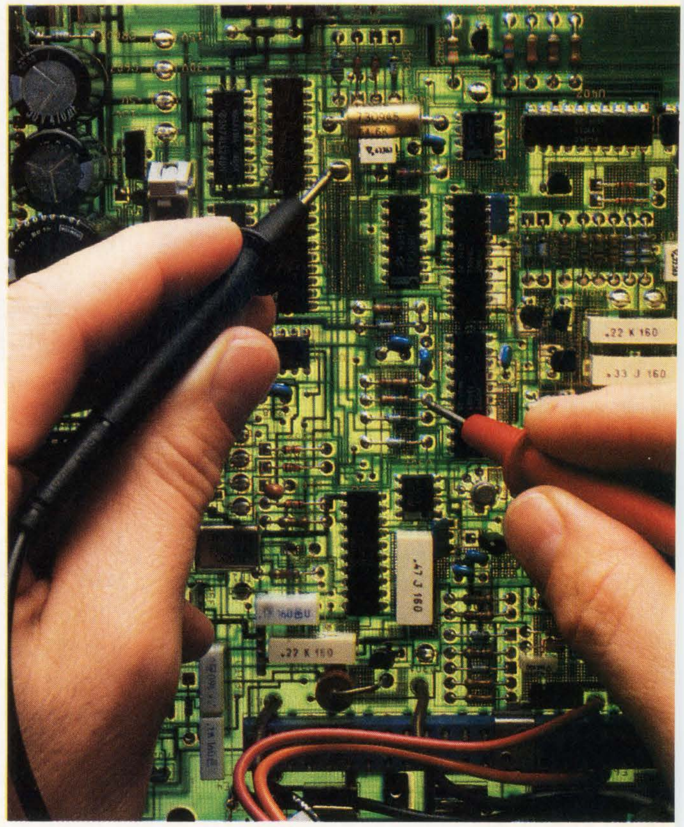

Clear up the uncertainty in your test measurements with these three versatile Fluke multimeters.

When you need performance that leaves no room for doubt, focus on the Fluke 25, 27 and 37 Analog/Digital Multimeters. With their patented A/D converters, they deliver DC volts accuracy within 0.1%. An easy-to-view display also provides a full 4 digits of resolution for readings up to 3200 counts.

Fully sealed, drop proof cases protect the handheld Fluke 25 and 27 from abuse on the job site. The unique design of the Fluke 37 is well suited for benchtop and portable use, and includes a convenient storage compartment for test leads and small accessories.

The circuitry in each model is shielded to eliminate interference — even near motors, radar, or other transmitters. And thirty-six components are dedicated to high-energy overload protection, for you and the meter.

All three instruments offer simplicity of operation. Select functions with one rotary dial. Don't worry about range selection — it's automatic. Plus, the auto-polarity digital readout and analog bar graph give you two ways to look at the signal. The 27 and 37 also add extra features like MIN/MAX Recording and Relative mode.

Next time you make a measurement, think about what you're missing. Then call us toll-free **1-800-227-3800, ext. 229** and ask about the Fluke 25, 27 and 37 meters. You'll get the picture.

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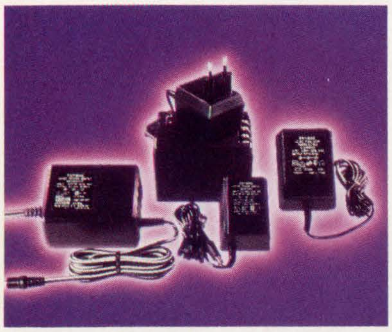
CIRCLE NO 199



***Linear wall-plug-in supplies** like these are suitable for applications requiring less than 25W; switching versions are offering outputs approaching 100W (pg 107).*

TECHNOLOGY UPDATE

PRODUCT UPDATE

DESIGN IDEAS

Continued on page 9

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THE ANSWER IS IN TEK DIGITAL STORAGE. FOR AS LITTLE AS $4150!

Now get the best of both worlds, analog and digital, in one familiar, easy-to-use package. With the 100 MHz Tek 2230 and 60 MHz 2220 you benefit from 20 MS/s *digitizing* plus analog operation to each scope's bandwidth. Just push a button for real-time display analysis!

Expect the most for your money—and get it—with Tek. You can capture events as narrow as 100 ns at any sweep speed—using Tek's proprietary peak detect mode. Trigger on complex waveforms using variable sweep holdoff. View events prior to or following a trigger event with pre/post trigger. Eliminate noise with built-in signal averaging. Store acquired waveforms as either 1K or 4K records. All with unrivalled convenience and confidence in your measurement results.

Features	2230	2220
Analog/Digital Storage BW	100 MHz	60 MHz
Max. Sampling Speed	20 MS/s	20 MS/s
Record Length	4K/1K (selectable)	4K
Save Reference Memory	One, 4K Three, 1K	One, 4K
Vertical Resolution	8 bits 10 bits (AVG mode) 12 bits (AVG mode over bus)	8 bits
CRT Readout	Yes	No
Cursor Measurements	Yes (storage mode)	No
GPIB/RS-232-C Options	Yes ($850)	Yes ($550)
Battery-Backed Memory (save 26 waveform sets)	Yes (inc. with 2230 communications options)	No
Price	$5150	$4150

Both scopes offer optional GPIB or RS-232-C interfaces. With either option the 2230 also includes battery-backed memory that provides 26K of keep-alive CMOS memory—for storing up to 26 waveform sets.

Call Tek direct to get your free video or diskette demo. Or to place an order! Ask about free Tek digital storage application notes and educational materials. Technical personnel will answer your questions, take an order and expedite delivery. Orders include complete documentation, operating manuals, worldwide service back-up and Tek's 3-year warranty that even covers the CRT.

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CIRCLE NO 200

Continued from page 7

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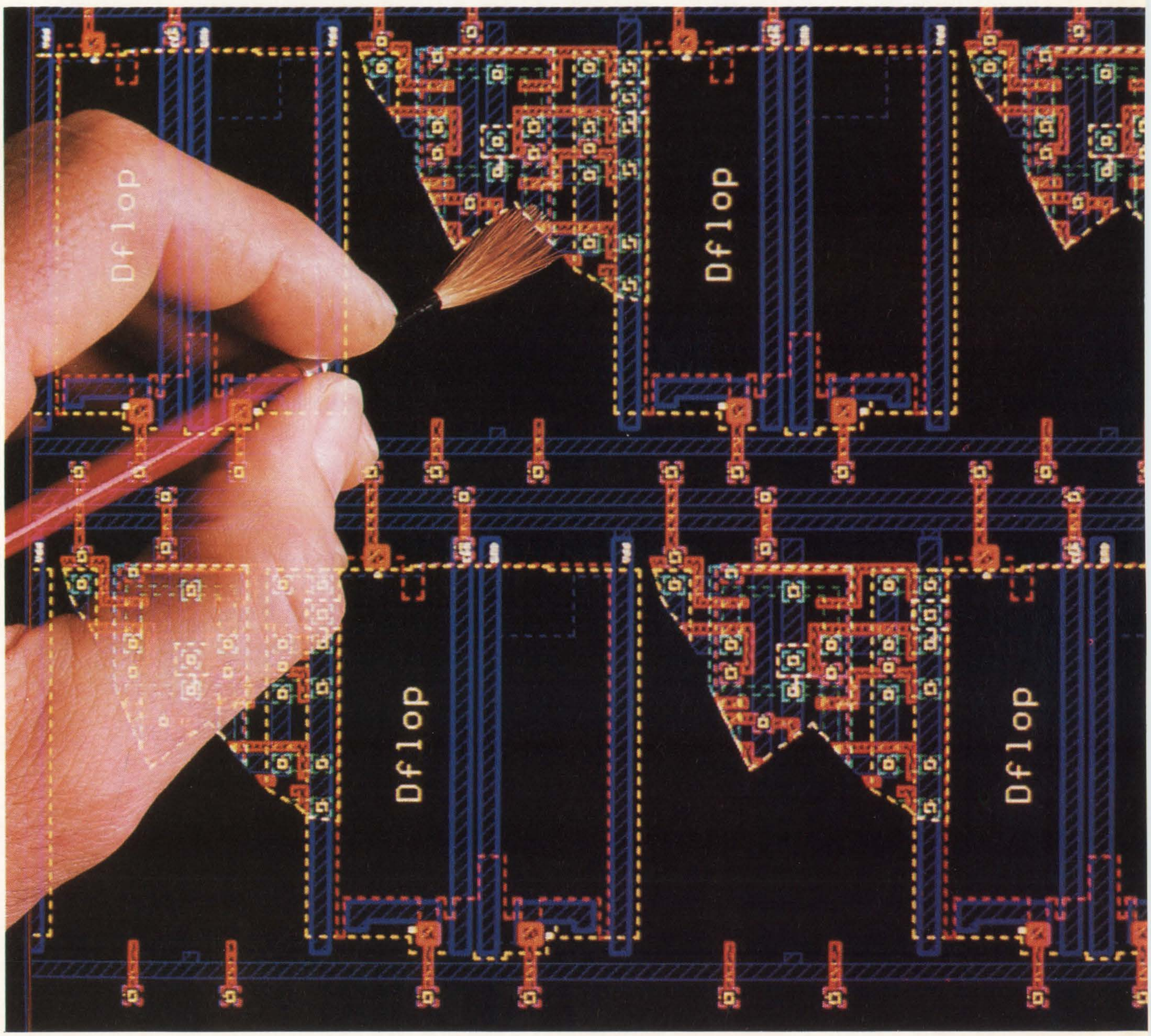
Edit in place? Only Mentor Graphics lets you edit all over the place.



During IC layout, hierarchical design delivers dramatic productivity gains.

But during global cell modifications, it can also leave you hopelessly blind.

Some layout editors let you see the one cell you're editing, but completely hide the global impact on other cells.

Other editors let you see the global impact, but totally isolate the selected cell in a separate window. So you work blindly, out of context.

Only one vendor of IC layout tools has seen the light and solved the problem.

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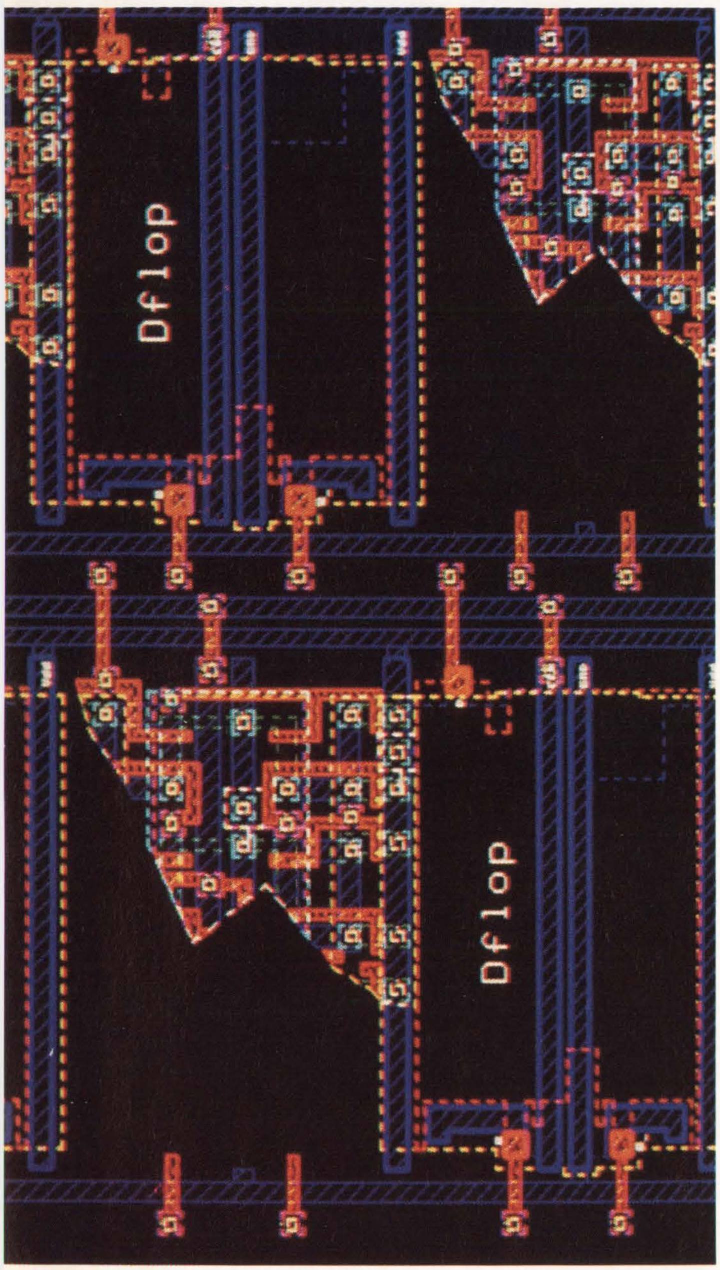
Our solution? The Chipgraph™ IC layout editor, the first such editor that lets you see it all during hierarchical editing.



With Chipgraph, you work on the selected cell directly in its layout environment. You see instantly how it relates to its surroundings. At the same time, all related cells are updated right on the screen, so you've got a complete picture of the global consequences.

You work faster. More accurately. With less iterations.

And Chipgraph lets you work bigger as well as better. Our hierarchical design system will easily accommodate the next generation of VLSI designs.

There's also boolean and edge functions to keep your editing fast and flexible. And changing technologies is no problem, because we've got all the angles covered. You can work with bipolar, linear and GaAs geometries as easily as MOS.

Plus you can put initial design rule checks in their proper place—the editor itself. Our interactive DRCs let you check as you edit. You get fast, accurate feedback on the correctness of your design. And for the final check, Chipgraph lets you run DRACULA II™ right on your workstation.

And to keep your IC designs in the industry mainstream, Chipgraph supports the GDS II input/output format. You enjoy compatibility with a wide variety of existing tools. And long-term viability for your design libraries.

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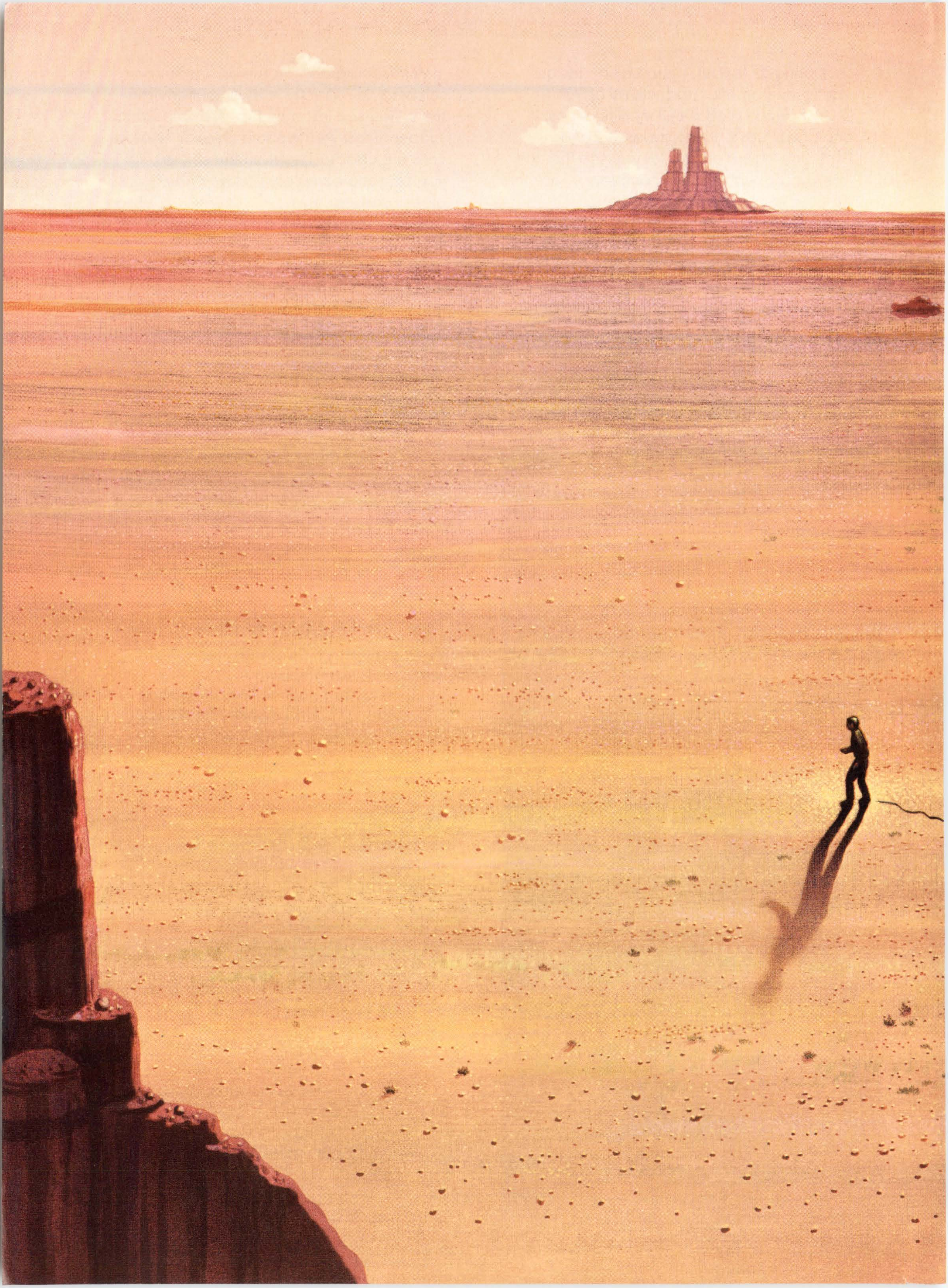

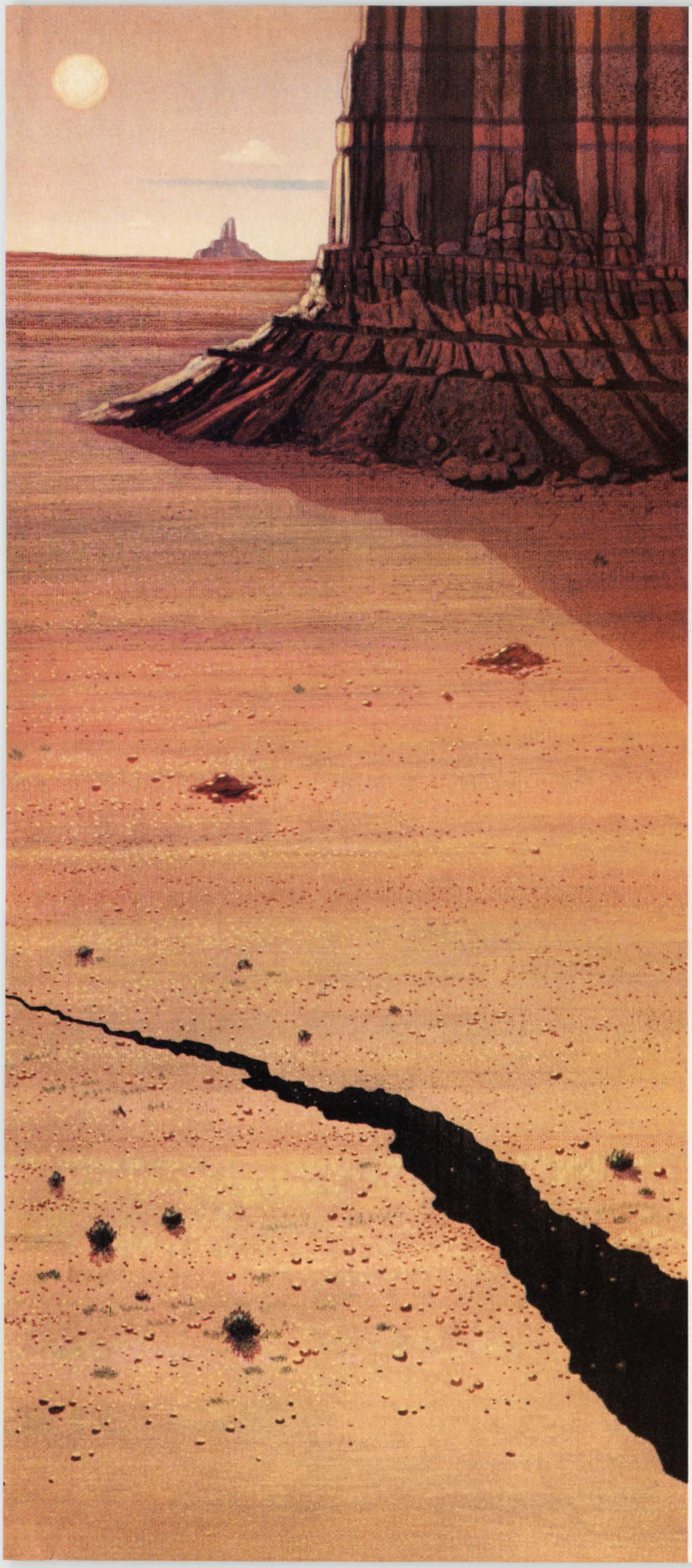

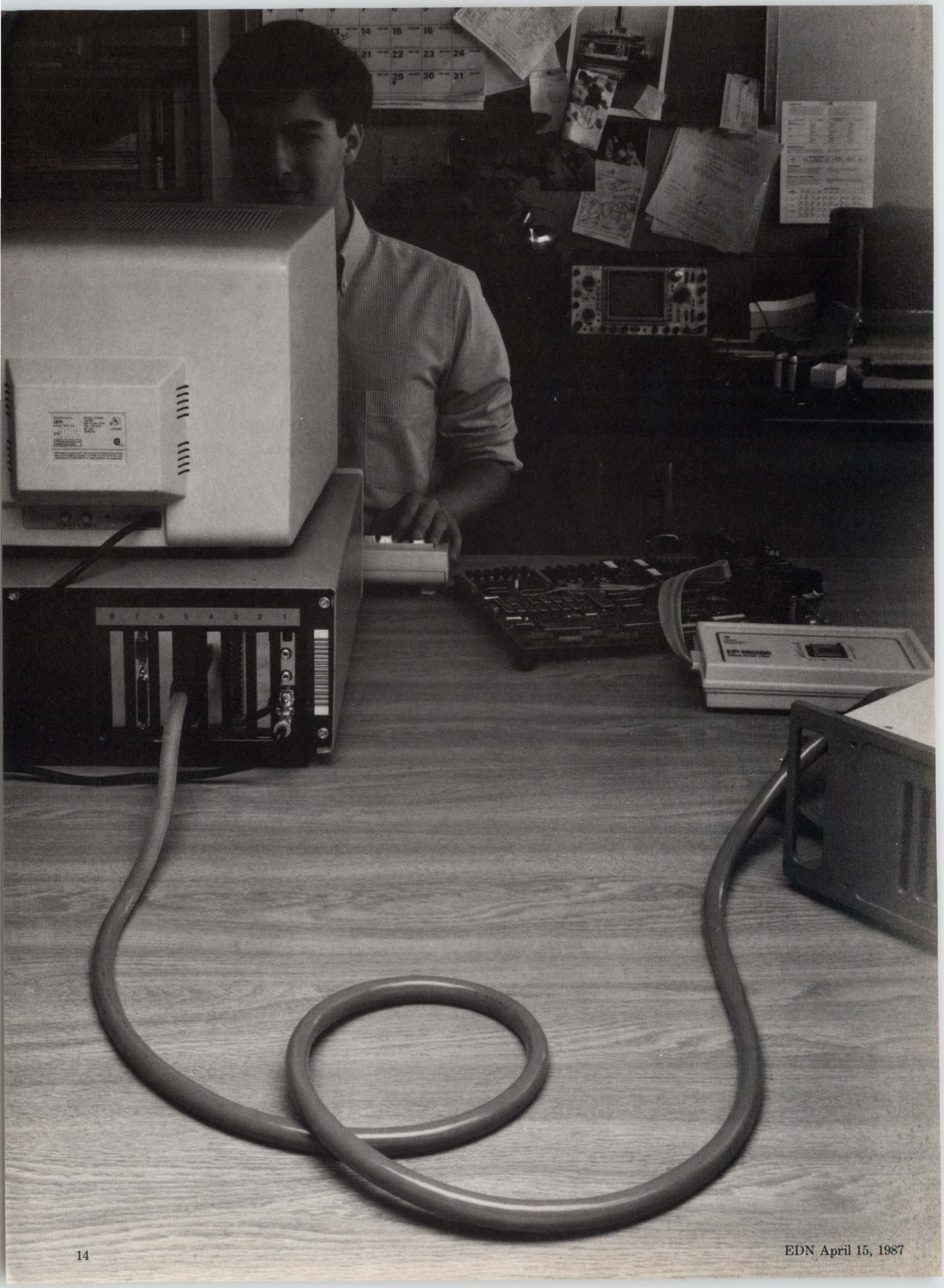

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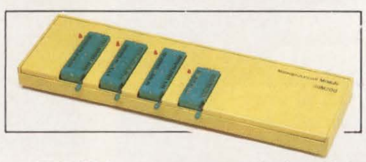

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CIRCLE NO 203

NEWS BREAKS

EDITED BY JOAN MORROW

RESOLVER-TO-DIGITAL CONVERTER POWERED BY ONE 5V SUPPLY

The HSRD1056 16-bit resolver-to-digital converter from Natel Engineering (Simi Valley, CA, (805) 581-3950) requires 10 mA and avoids ground-loop problems by requiring one 5V supply. It features an accuracy of 1.3 arc-minutes and a tracking rate of 7200°/sec. In addition, the HSRD1056 contains circuitry to ensure that it locks into an angle 180° from the true angle when a 180° step function is applied. Pricing starts at $560, depending on options; delivery is six to eight weeks ARO.—Margery S Conner

SCSI DEVELOPMENT TOOLS FILL LAB, FIELD, OR FACTORY ROLES

A set of IBM PC-based SCSI (Small Computer System Interface) development and test tools from Adaptec (Milpitas, CA, (408) 432-8600) serves lab, factory, and field test tasks. The family includes the SDS-2 SCSI development and test system, the SDS-100 SCSI test system, and the SDS-210 SCSI logic analyzer. The SDS-2 package includes an IBM PC/XT computer, a SCSI test and development board, and software. The complete package costs $19,500; you can buy the development system without the computer for approximately $16,000. Priced at $5500, the SDS-100 add-in board and software economically fit factory and field test roles. Adding the logic analyzer to either system costs $3750, or you can purchase it as an upgrade for $4500.—Maury Wright

RING-STYLE PROXIMITY SENSOR DETECTS TINY OBJECTS

The 972RS ring-style proximity sensor from the Micro Switch Division of Honeywell (Freeport, IL) detects small metal parts or continuous metal forms, such as wire and pipe with diameters as small as 0.062 in., within a 0.75-in. circular sensing window. Sensitivity to nonferrous metals is approximately one-third that of ferrous metal. You can set the device's sensitivity to accommodate various object sizes. The sensor is sealed to NEMA 1, 3, 4, 12, and 13 requirements. It sources or sinks 200 mA through normally open outputs and costs $41.13 (100).—Steven H Leibson

SCANNER CARDS BOOST MEASUREMENT PRECISION

If your application requires precise current, resistance, voltage, or temperature measurements, consider a new family of scanner cards from Keithley Instruments (Cleveland, OH, (216) 248-0400). The Model 7158 low-current, 10-channel scanner card switches between channels in 1 msec and provides 1-pA measurements for voltages as high as 30V. The Model 7067 is a Kelvin resistance scanner card with two source contacts for switching 350 mA. The 7168 nanovolt scanner is an 8-channel, 2-pole card that features a 20-nV differential contact potential between channels, an input leakage of less than 50 pA at 23°C, and an actuation time of less than 3 msec. The Model 7402 thermocouple scanner card has a 9-channel, 2-pole configuration with a contact offset voltage of less than 1 μV per channel for less than 0.025°C error. Prices range from $500 to $1995.—J D Mosley

CAD SOFTWARE SUPPORTS HYBRID-CIRCUIT DESIGN

The HP74307A hybrid-circuit design module provides several tools for developing hybrid circuits. The $4000 software package from Hewlett-Packard (Palo Alto, CA) runs under the HP74305A engineering graphics system on the company's Series 9000 Model 200 and 300 workstations. The software package includes automatic thin-film resistor generation, support for irregularly shaped conductors and dielectric crossovers, and a starter library of more than 300 hybrid parts. The software generates resistor values using user-defined resistor-paste curves. Maximum part-placement resolution is 0.00001 mil.—Steven H Leibson

NEWS BREAKS

FULL-TRAVEL KEYBOARDS STAND UP TO CONTAMINANTS

Meeting International Standard IP 65, a new line of keyboards from Preh Electronic Industries Inc (Niles, IL, (312) 647-8338) offers protection against environmental contaminants such as dust and strong water spray. These keyboards operate within spec when subjected to relative humidity as high as 93% and temperature conditions ranging from 14 to 122°F. Each unit provides 3.5 mm of key travel with tactile feedback. Prices range from $10 for a basic keypad to $200 for a full-size keyboard.—J D Mosley

I/O INTERFACE BOARD LETS MACINTOSH DO A/D CONVERSIONS

You can now use your Macintosh II computer for automated process control and monitoring, electronic testing, signal analysis, and chromatography. Just plug an NB-MIO-16 multifunction analog and digital I/O interface from National Instruments (Austin, TX, (512) 250-9119) into the manufacturer's Real-Time System Integration (RTSI) bus to perform 12-bit A/D conversions on 16 analog inputs. The board includes two 12-bit D/A converters, eight lines of TTL-compatible digital I/O, and three 16-bit counter/timer channels for timing I/O operations. A/D conversion times are 25, 15, and 8 μsec; the 8-μsec mode provides a worst-case data-acquisition sample rate of 111k samples/sec. A 16-word-deep FIFO buffer stores converted data to boost performance. Another new product, the company's NB-GPIB board, lets you use your Macintosh II for instrument control via the RTSI bus. The NB-MIO-16 costs $1195 to $1495; the NB-GPIB costs $495.—J D Mosley

ANALOG ICs OPERATE OVER −55 TO +200°C

Linear Technology (Milpitas, CA) now offers six of its analog parts with an extended-temperature operating range of −55 to +200°C for high-stress and military applications. The parts are the LM101AXH op amp, the LM118XH high-slew-rate op amp, the LM119XH dual comparator, the LM129HX precision voltage reference, the LT1001XH precision op amp, and the LT1007XH low-noise high-speed op amp. The devices are available screened to MIL-STD-883 for $17.75, $31.65, $22.55, $25.75, $25.95, and $34.45, respectively. You can order them unscreened for $12.75, $26, $17.55, $20, $22.75, $31.25, respectively.—Steven H Leibson

12-MHz VIDEO CONTROLLER EASES INTEGRATION

The 12-MHz TMS34061-12 Video System Controller (VSC) from Texas Instruments (Dallas, TX, (800) 232-3200) integrates video RAM, dynamic RAM, and CRT controls on a single chip, thus eliminating the need for separate text and graphics subsystems. You can use this controller with any μP having a frequency as high as 12.5 MHz. The chip generates sync and blanking signals, features independent system and video clocks, and lets you drive as many as 64 RAMs without external buffering. The video controller costs $22.80 (1000).—J D Mosley

POWER DRIVER ICs FEATURE FOUR ISOLATED DMOS SWITCHES

Suited to driving stepper motors, needle solenoids, or similar inductive loads, the L6114 and L6115 driver ICs from SGS-Microelettronica SpA (Agrate Brianza, Italy, TLX 330131; in the US, (602) 867-6100) incorporate four isolated DMOS power transistors with TTL/CMOS-compatible driver stages. Separate pin connections are provided for the source and drain of each transistor. An enable input allows you to turn all four transistors off. Switching frequencies extend to 200 kHz. The DMOS transistors have an on-resistance of 0.7Ω and can withstand 100V. They can conduct 1.5A in the power-DIP package of the L6114 and 3A in the Multiwatt package of the L6115. Peak current capability is 5A for both devices, and they have on-chip protection diodes for inductive load switching. The driver ICs cost $4 (500).—Peter Harold

MULTIBUS-II ANALOG I/O BOARDS SUPERVISE I/O SUBSYSTEMS

Endorsing the view that I/O boards require onboard intelligence to make optimum use of the Multibus-II architecture, Concurrent Technologies Ltd (Colchester, UK, TLX 946240; in the US, (714) 768-3332) has provided its £2300 M-AI186/080 analog-input board and M-AO186/032 analog-output board with iAPX186 μPs. The M-AI186/080 provides you with 80 single-ended or 40 differential input channels, a sample/hold amplifier, and a 12-bit A/D converter. The M-AO186/032 has 32 analog outputs driven by one 12-bit D/A converter and sample/hold circuitry.

In addition to their iPSB-bus interface, the boards have an interface connector to the company's cCBX-bus, which allows you to expand the I/O subsystem with slave I/O cards, while still being able to interrogate the additional boards via the Multibus-II interconnect space.—Peter Harold

TANDON AWARDED JAPANESE DISK-DRIVE PATENT

Tandon Corp (Chatsworth, CA) will receive a Japanese patent covering the company's technology for the manufacture of double-sided flexible disk drives used for memory storage in microcomputers. The Board of Appeals of the Japanese Patent Office notified Tandon that it will be granted a Japanese counterpart of the US patent that it received in 1979 for this technology. Tandon can now require royalty payments from those unlicensed companies who manufacture or sell the patented drives in Japan. The disk-drive manufacturer says it intends to seek royalties in the future and also wants to receive payments for past infringements.—Joan Morrow

JAPANESE VERSION OF 1-2-3 GETS NUMBER ONE RANKING

Lotus Development Corp's (Cambridge, MA) Japanese version of the 1-2-3 spreadsheet package, Release 2J, has been named the best-selling business personal-computer software package in Japan for four consecutive months. Release 2J was the product of an 18-month effort by Lotus Development Japan Limited in Tokyo. The package was enhanced to include kana-to-kanji conversion (the technique for entering the 7000 Japanese characters from a normal-size keyboard), new graph types, and the ability to sort phonetically. Current editions run on the NEC 9800 and the IBM 5550 personal-computer families. Versions for the Toshiba J-3100 and Fujitsu FM R personal computers should be available this month.—Joan Morrow

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HIGH PASS Model *HP-		50	100	150	200	300	400	500	600	700	800	900	1000
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	end, min.	200	400	600	800	1200	1600	1600	1600	1800	2000	2100	2200
Min. 20dB Stop Frequency (MHz)		26	55	95	116	190	290	365	460	520	570	660	720

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*Prefix P for pins, B for BNC, N for Type N, S for SMA   *example:* **PLP-10.7**

CIRCLE NO 204

F82-2 REV. B

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EF 6803U4	1, 1.25, 1.5	8-Bit ROMless Microcontroller	MC 6803U4 (−1,A)
EF 6809	1, 1.5, 2	High-performance 8-Bit MPU	MC 6809 (A,B)
EF 6809E	1, 1.5, 2	High-performance	MC 6809E (A,B)
16-BIT			
MK 68000	8	16-Bit Microprocessor	MC 68000-8
TS 68000	10, 12.5, 16	16-Bit Microprocessor	MC 68000-10, 12
TS 68008	8, 10, 12.5	16-Bit Microprocessor	MC 68008-8, 10, 12
MK 68200	4, 6	16-Bit ROMless Microcontroller	—

PERIPHERALS

Device	Available Speed (MHz)	Description	Alternate Source
8-BIT			
EF 6821	1, 1.5, 2	Parallel I/O (PIA)	MC 6821 (A,B)
EF 6840	1, 1.5, 2	Programmable Timer (PTM)	MC 6840 (A,B)
EF 6850	1, 1.5, 2	Serial I/O (ACIA)	MC 6850 (A,B)
EF 6854	1, 1.5, 2	ADLC Controller	MC 6854 (A,B)
16-BIT			
MK 68230	8, 10	Parallel I/O and Timer	MC 68230-8, 10
MK 68564	4, 5	Serial I/O	—
MK 68901	4, 5	Multi-Function Peripheral	MC 68901-4
MK 68451	8, 10	MMU	MC 68451-8, 10
TS 68HC901	4, 5, 8	HCMOS Version of 68901	—

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Device	Description
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EF 9367	Graphic 512 x 1024 Pixels
EF 9369	Palette Circuit 16 x 4096
EF 9370	Palette Circuit 16 x 4096
TS 68483	Graphic — Drawing Processor
TS 68493	Enhanced 68483
TS 68494	Palette 256 x 4096

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TS 68950/1/2	Modem Analog Front End Chip Set
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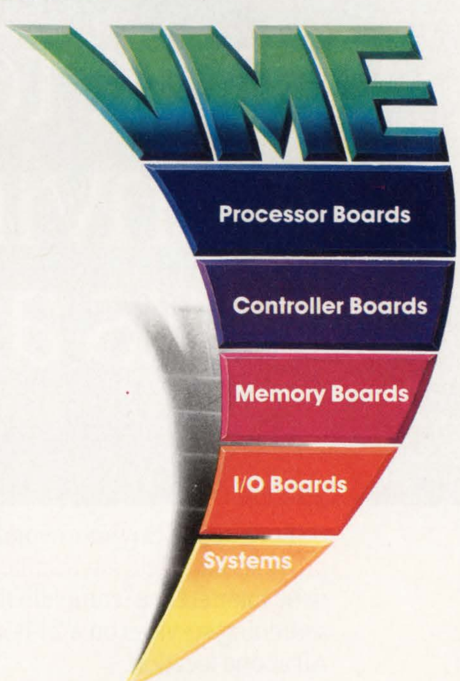
CIRCLE NO 105

intelligence



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Most TV stations use local sync generators

Dear Editor:

The Design Idea "TV sync generator acts as clock timebase" (EDN, December 11, 1986, pg 278) erroneously states that the oscillator "tracks the network signal, which is derived from atomic standards." Actually, the 3.5795454545 . . . MHz color subcarrier can be generated by an atomic clock at the network. The truth is that most TV stations run on crystal-controlled local sync generators. In many cases today, the local station sync is not locked to the network. Instead, the network signal is imported through a frame store and is locked to the local standard.

This fact does not negate the value of the Design Idea or its circuit. The article does, however, perpetuate the myth that local TV stations use network sync. Modern technology has done away with that need. Indeed, it is much safer not to have the local plant locked to the network feed, where an interruption could cause considerable problems.

Sincerely yours,
Charles L Hutchinson
Technical Editor
The American Radio Relay League Inc
Newington, CT

Avoid lock-up in RAM arbiter

Dear Editor:

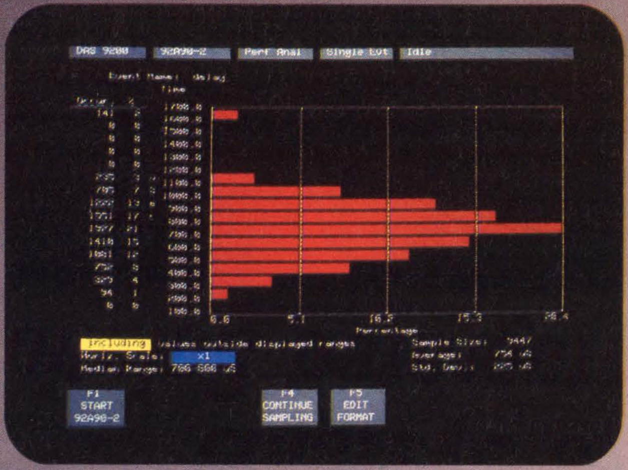
I'm writing with regard to my Design Idea "Arbiter lets two μPs use common RAM," (EDN, November 27, 1986, pg 239). The circuit as submitted and as shown represents one way to implement a first-come, first-serve access to common RAM. However, this circuit should not be considered to be the complete enabling system for a common RAM.

The article mentions that a lock-up condition could occur if both μPs tried to access the RAM at the same time. If this circuit is used as is—in other words, if the buffer enables go directly to the address and data buffers—simultaneous access will cause a lock-up and bus-contention condition to occur when both μPs' buffers are enabled. The present application of this circuit includes a lock-out method for the buffer enables that uses this circuit's buffer enables as inputs. I apologize for not mentioning this detail in the article.

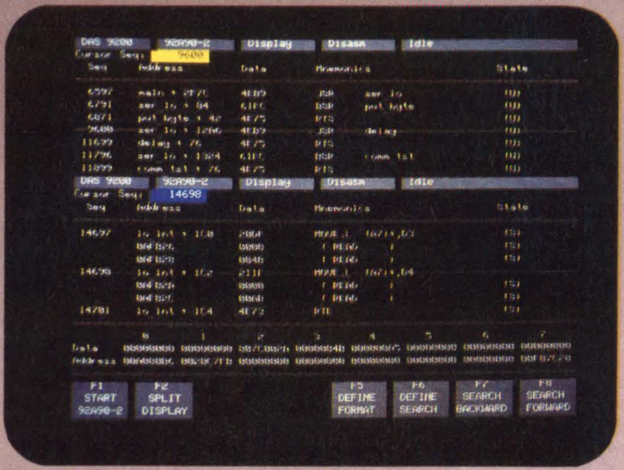
Sincerely yours,
Jim Wojcik
Allen-Bradley Co
Highland Heights, OH

Text continued on pg 34

DAS9200 DIGITAL ANALYSIS: NOW TEK MAKES THE IMPOSSIBLE LOOK EASY.



Software Performance Analysis, like this distribution of a subroutine's execution times, helps you easily understand the activity of your code.



Step backwards through acquired data, including subroutines, stack and register models, using time-correlated split-screen displays to pinpoint problems.

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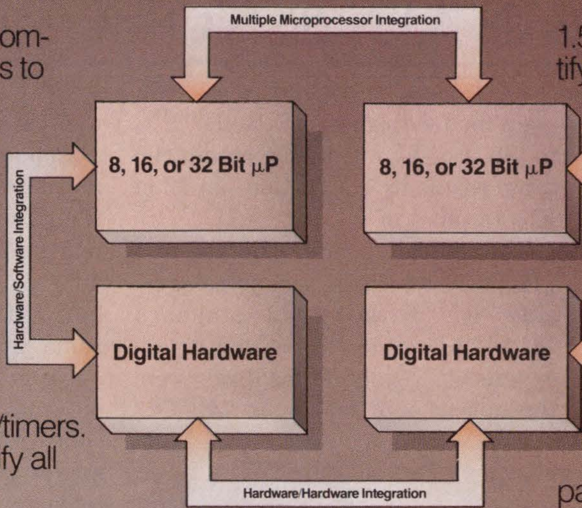
2 Symbolic, real-time software debugging. Register deduction and stack simulation let you pinpoint problems like stack overflow or incorrectly restored pointers—without breakpoints or manual notation.



3 Simultaneous integration of up to six microprocessors. Use the dual timebases and real-time handshaking between system modules to set up split-screens displays that scroll in precise time alignment.

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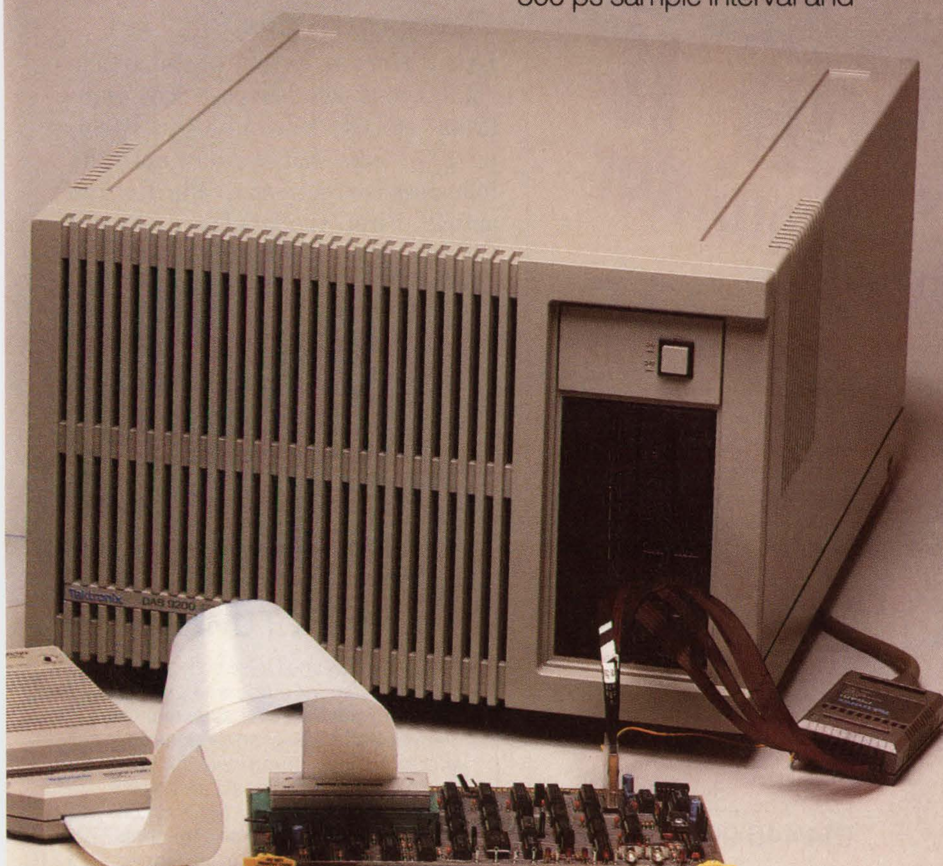

Available in desktop and rack-mount versions, the DAS9200 mainframe can be augmented with up to three expansion mainframes for a total of 28 card slots.

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Circle 4 for literature

Circle 82 for sales

Design Idea feedback

Dear Editor:

I'd like to comment on the Design Idea "Sync separator flags odd fields," (EDN, October 16, 1986, pg 233). First, in **Fig 1**, pin 5 of IC_{1B} is shorted to 5V, which will probably physically damage the IC.

Further, pin 4 of IC_{2A} is called Set, not Reset. There is really no need for feedback from pin 9 of IC_{2B} to pin 4 of IC_{2A}. You can obtain the same result by connecting pin 12 of IC_{1B} to pin 4 of IC_{2A}.

The article specifies the use of a 74LS221, which is a nonretriggerable IC. However, a standard 74LS123 is easier to get and is less expensive. A simple feedback from the output will make the 74LS123 nonretriggerable.

In addition, t_2 (in **Fig 3**) should be no more than 0.5 to 1 μsec longer than the incoming horizontal sync pulse width. Otherwise, you'd need another one-shot to regenerate the horizontal sync pulse and keep the same phase.

Finally, this circuit can operate only at a single frequency without readjustment, which, in practice, makes it useless for multiscan systems.

Sincerely yours,
Jack Gershfeld
Extron/RGB Systems Inc
Stanton, CA

(Ed Note: The short of pin 5 to 5V was not an error of the author; it was made during the editing process.)

Figure correction

Eric P Horton, author of the article "Make your own low-cost 8051 emulator" (EDN, November 13, 1986, pg 193), asks that readers note the following corrections to **Fig 1** of the article. First, the labels for CS_2 and CS_6 are transposed: CS_2 should be labeled CS_6, and vice versa.

Further, the switch connected to the 6264's $\overline{CE}$ pin should connect to the newly relabeled CS_2 (the output of the far-right NAND gate). The $\overline{CE}$ pin of the 8155 must be rerouted to the newly relabeled CS_6, which is the output of the NAND gate connected to A_{13} and A_{14}.

YOUR TURN

EDN's Signals and Noise column provides a forum for readers to express their opinions on issues raised in the magazine's articles or on any topic that affects the engineering industry. Send your letters to the Signals and Noise Editor, 275 Washington St, Newton, MA 02158. We welcome all comments, pro or con. All letters must be signed, but we will withhold your name upon request. We reserve the right to edit letters for space and clarity.


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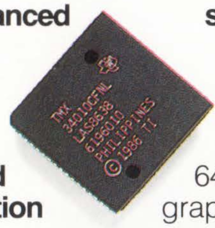

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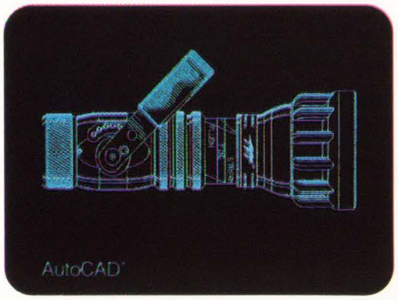

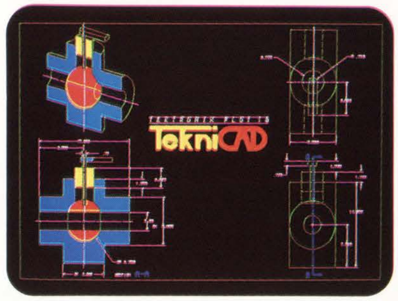

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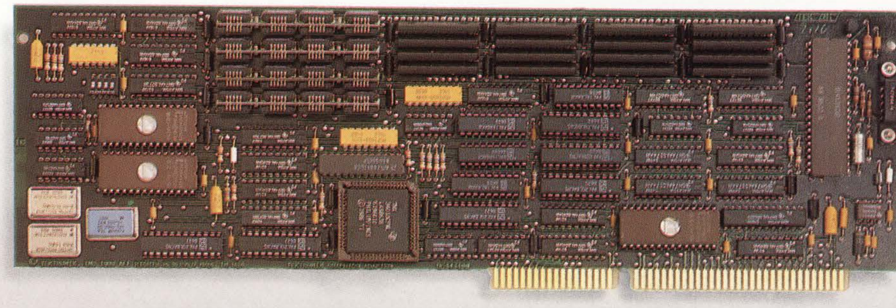

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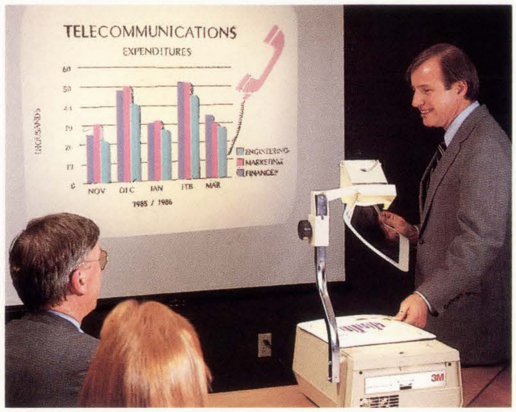

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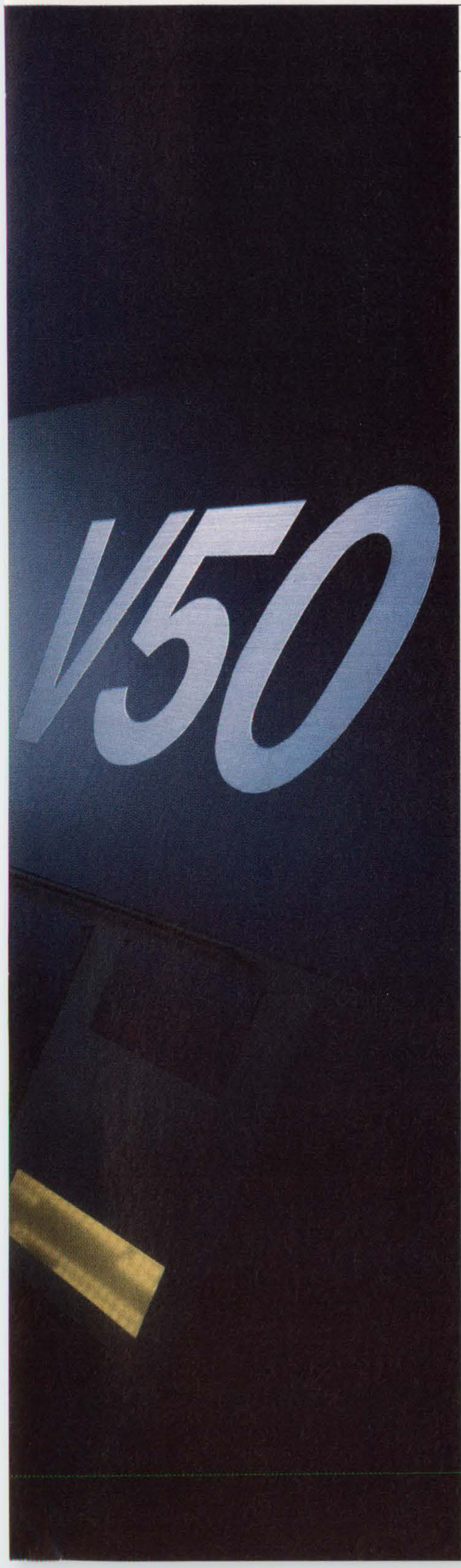

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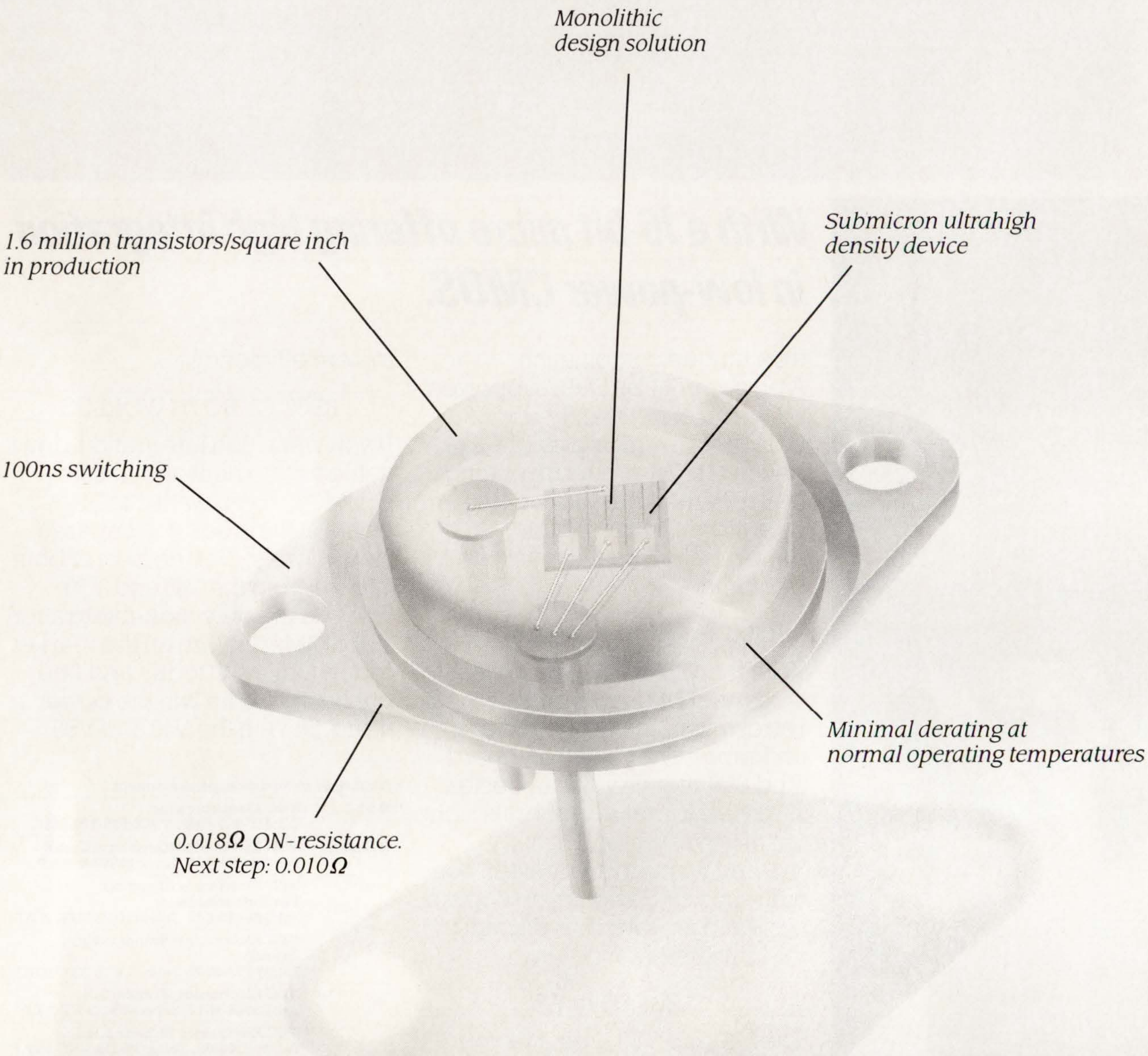

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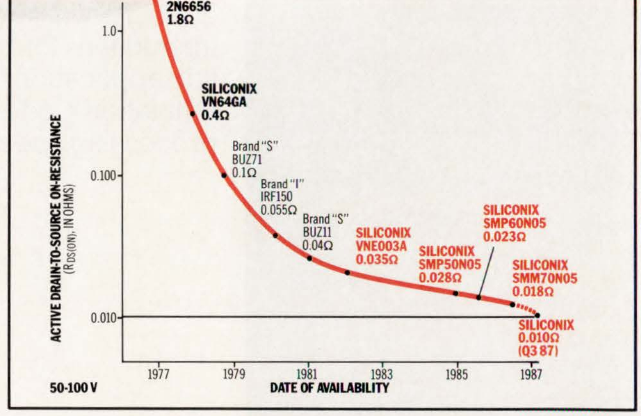

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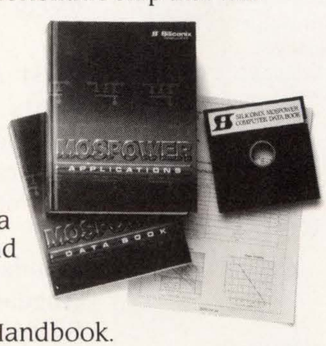

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CALENDAR

Invitational Computer Conference Computer Graphics Series, Paris, France. BJ Johnson & Associates, 3151 Airway Ave, #C-2, Costa Mesa, CA 92626. (714) 957-0171. May 5.

Custom Integrated Circuits Conference, Portland, OR. Laura Silzars, Conference Coordinator, 6900 SW Canyon Dr, Portland, OR 97225. (503) 292-6347. May 5 to 7.

Southeast Lightwave Expo, Atlanta, GA. Lightwave, 235 Bear Hill Rd, Waltham, MA 02154. (617) 890-2700. May 5 to 7.

Optical Storage Forum, Denver, CO. Cartlidge & Associates, 1101 S Winchester Blvd, Suite M259, San Jose, CA 95128. (408) 554-6644. May 6 to 8.

PC Fab Expo, San Jose, CA. PMS Industries, 1790 Hembree Rd, Alpharetta, GA 30201. (404) 475-1818. May 6 to 8.

Great Lakes Logo Conference, Cleveland, OH. Alice Friedman, Educational Computer Consortium of Ohio, 1123 S O M Center Rd, Cleveland, OH 44124. (216) 461-0800. May 7 to 8.

APL '87 (International APL Conference), Dallas, TX. APL '87 Registrar, 440 Northlake Shopping Center, Suite 210, Dallas, TX 75238. May 10 to 14.

First Annual Disk Drive Components Review, Sunnyvale, CA. Technology Review Manager, Peripheral Research Corp, (805) 963-8081 or (805) 494-4413. May 12.

Hands-on Programming in C, Los Angeles, CA. Integrated Computer Systems, Box 3614, Culver City, CA 90231. (800) 421-8166; in CA, (213) 417-8888. May 12 to 15.

Opportunities in Flat-Panel Displays, Boston, MA. Ronnie Sarkar,

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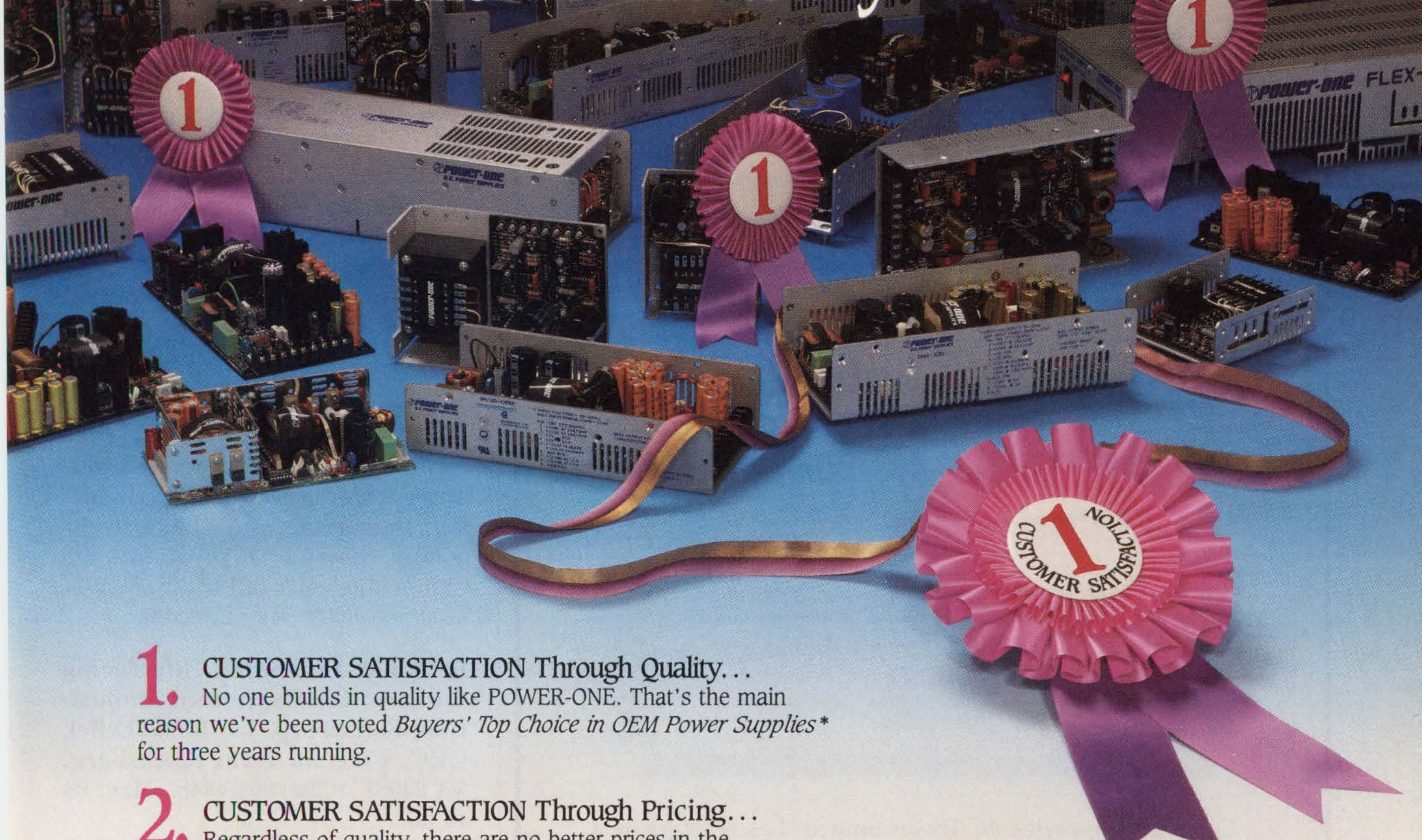

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*Electronic Buyers' News, Annual Top 100 Component Suppliers Survey. . . 1984, 1985, 1986.

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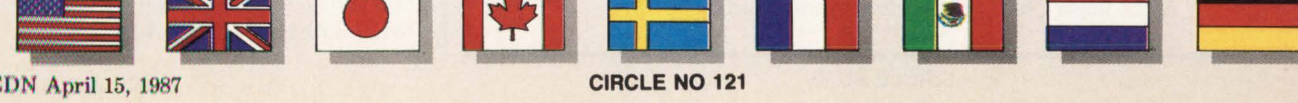


CIRCLE NO 121

CALENDAR

Arthur D Little Inc, 15 Acorn Park, Cambridge, MA 02140. (617) 864-5770, ext 2377. May 18.

EMC Expo, San Diego, CA. EMC Expo, Box D, Gainesville, VA 22065. (703) 347-0030. May 19 to 21.

Satellite Communications (short course), Sunnyvale, CA. Continuing Education Institute, 21250 Califa St, Woodland Hills, CA 91367. (818) 710-1142. May 19 to 21.

41st Annual Frequency Control Symposium, Philadelphia, PA. Synergistic Management, Box 826, Belmar, NJ 07719. (201) 280-0410. May 27 to 29.

International Workshop on Computer-Aided Software Engineering, Cambridge, MA. Index Technology Corp, 101 Main St, Cambridge, MA 02142. (617) 491-2100, ext 8000. May 27 to 29.

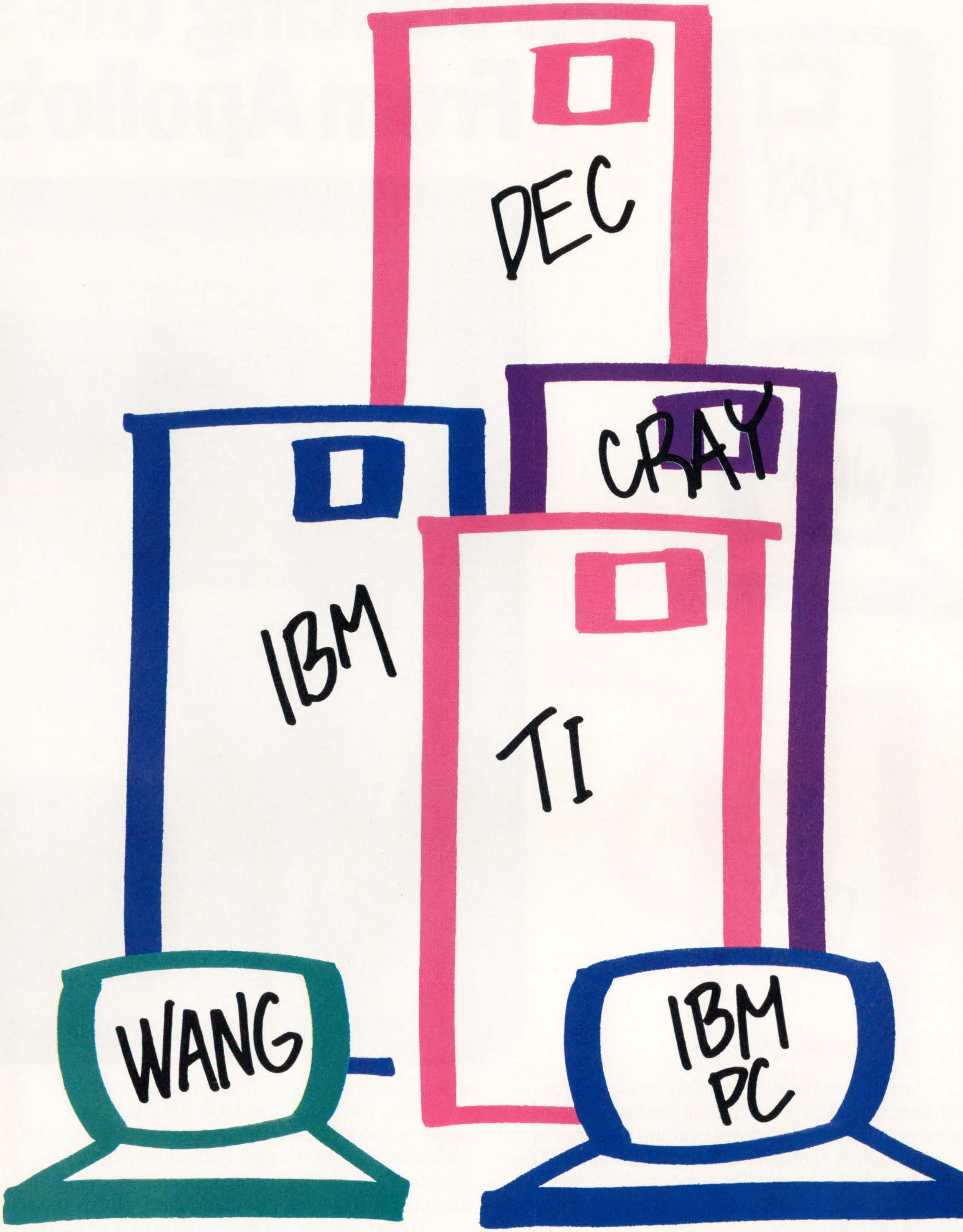
Personal Computer Interfacing for Scientific Instrument Automation, Blacksburg, VA. Linda Leffel, CEC, Virginia Tech, Blacksburg, VA 24061. (703) 961-4848. May 28 to 30.

Comdex/Spring, Atlanta, GA. Interface Group, 300 First Ave, Needham, MA 02194. (617) 449-6600. June 1 to 4.

Hands-on Programming in C, Washington, DC. Integrated Computer Systems, Box 3614, Culver City, CA 90231. (800) 421-8166; in CA, (213) 417-8888. June 2 to 5.

Troubleshooting Microprocessor-based Equipment and Digital Devices, Arlington, TX. Micro Systems Institute, Garnett, KS 66032. (913) 898-4695. June 2 to 5.

ICCE (International Conference on Consumer Electronics), Rosemont, IL. Geriann Van Calbergh, First National Bank of Chicago, 8528 W Gregory St, Chicago, IL 60656. (312) 399-1653. June 3 to 5.



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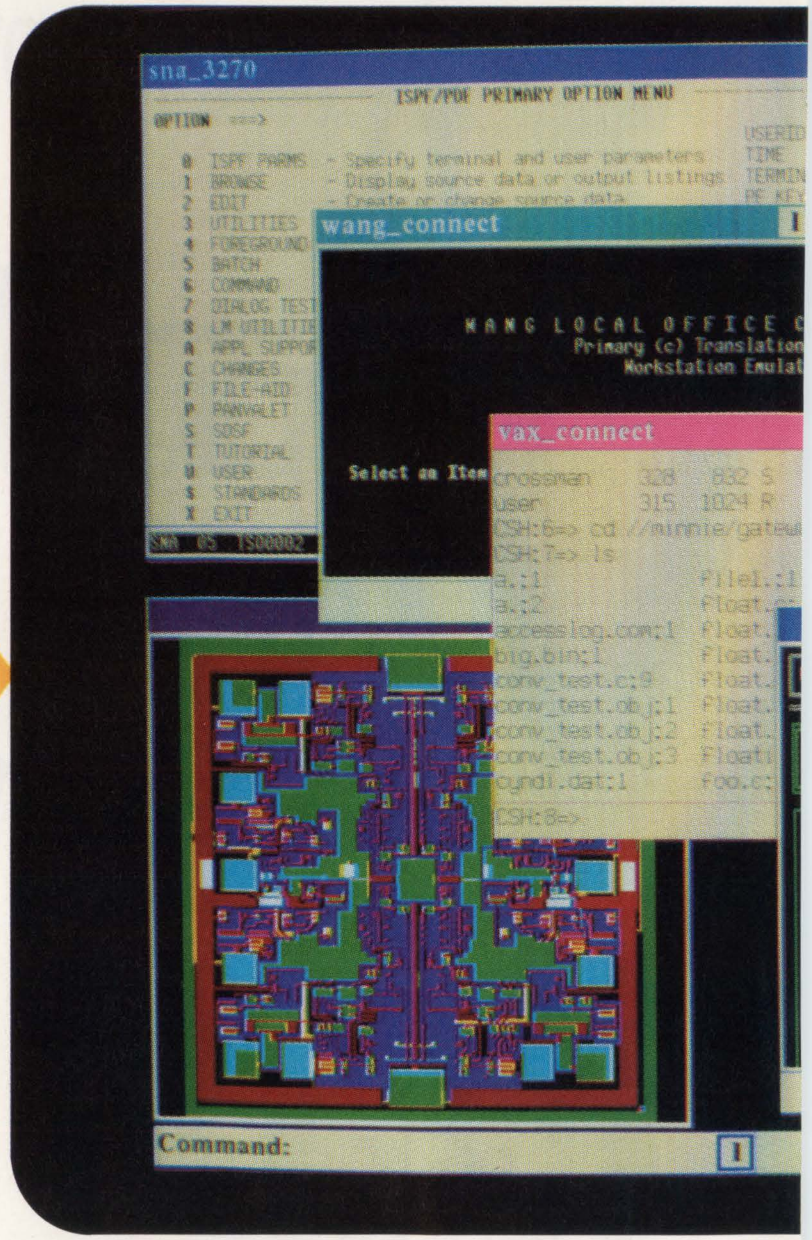

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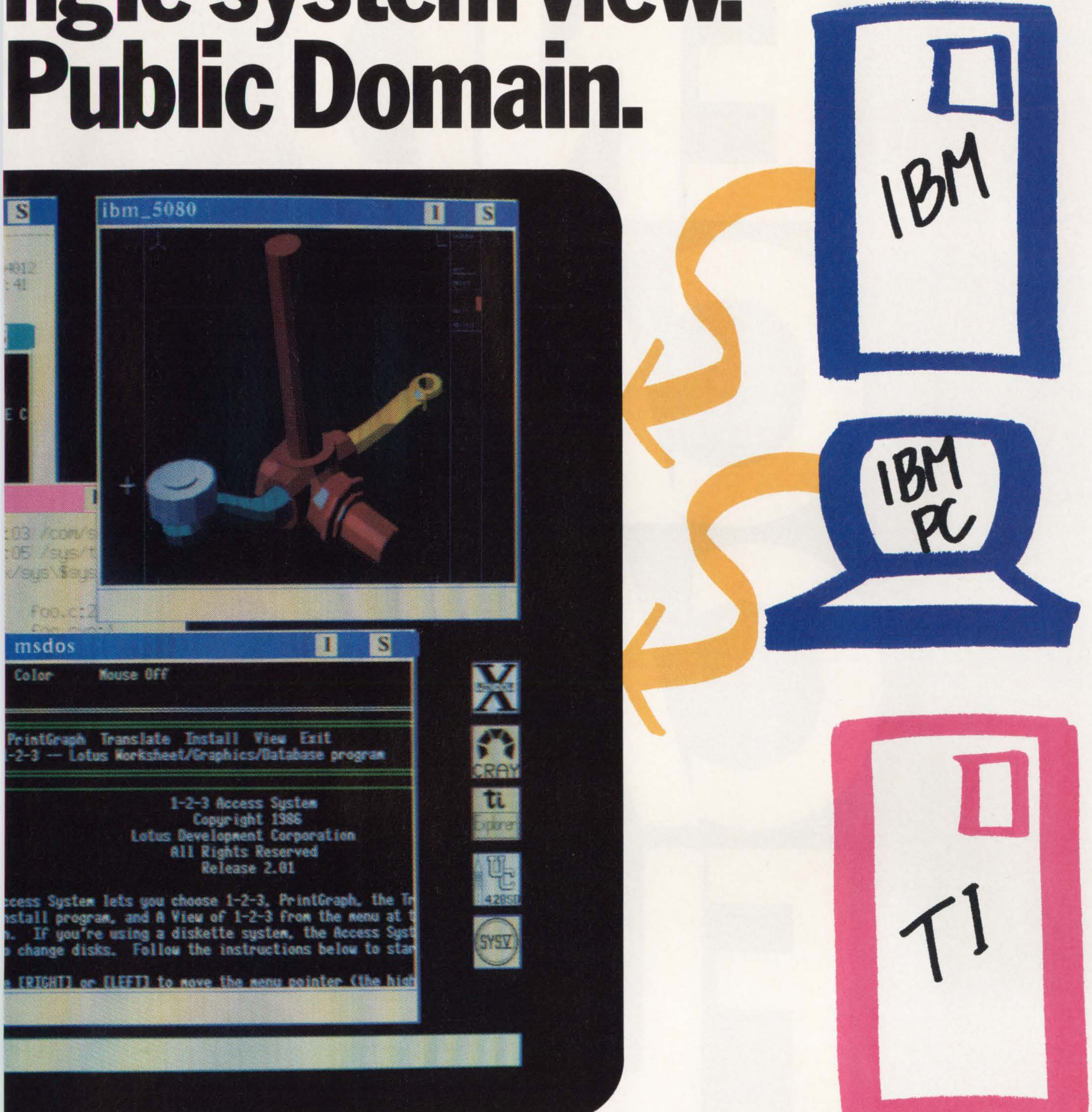

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In the old days, factories blew smoke. Now it's the salesmen who do.

"What you need is a cradle-to-grave vendor," they say. "Yeah, that's the easiest way to integrate PCB design."

What they don't say is that single-vendor integration also offers you the fastest route from cradle to grave. Simply stated, this nearsighted approach has thrown our entire industry into chaos. Creating a veritable CAD/CAM bedlam.

What you need is a CAD partner, who believes in open system architecture. Who believes in process automation, not just creating piecemeal solutions to speed isolated tasks.

Who understands that CAD is a vital link in successfully completing your PCB design and getting it to market.

Who is willing to adapt to your individual design environment.

Who understands the importance of competitive compatibility and helps you maximize your current system investment. And works with what you already have, instead of expecting you to walk away from previous investments.

Who believes making sense is just as important as making sales.

At Calay, we'd like to think we're just such a partner. And we think you'll appreciate how we can help make the entire PCB design process easier to manage. And more profitable.

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CIRCLE NO 118

For workstations that thrive in a multivendor

HP's powerful family of technical workstations fits right in with your present computing resources, as well as those added in the future. With industry standard networking, operating systems, and languages. *Plus* hundreds of advanced application packages, and performance extras to give you the competitive edge in all of your engineering and technical activities.

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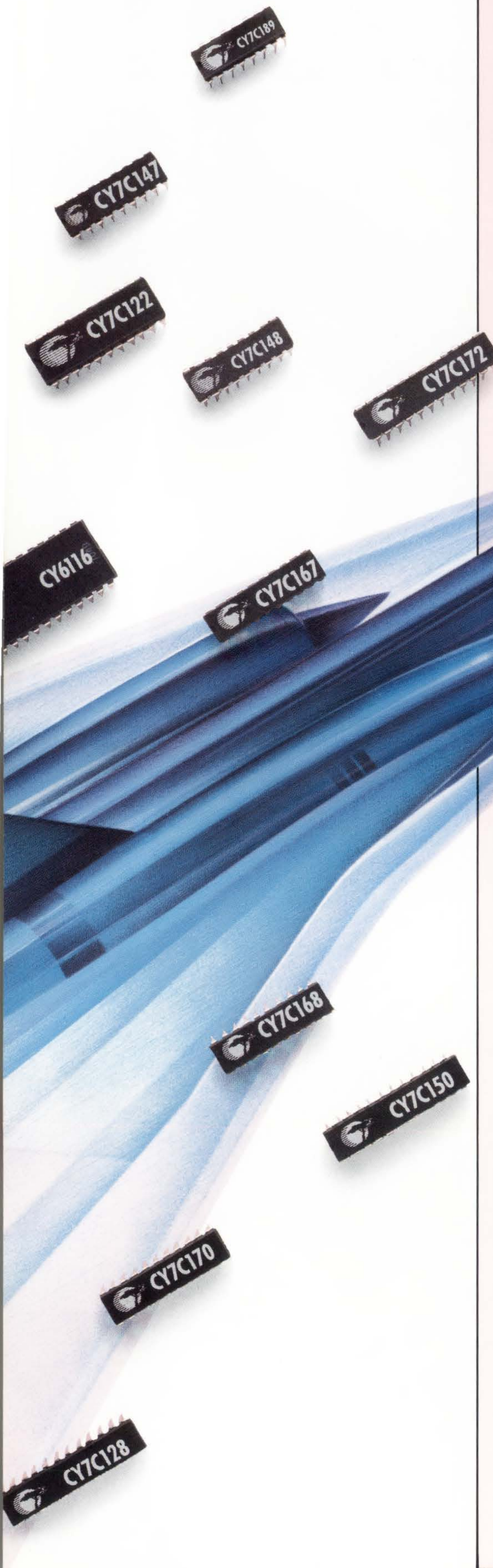
The choice is yours...from low-cost monochrome to high-resolution color monitors...from simple report

We illustrate the Lockheed SR-71 Reconnaissance aircraft, holder of the world's air speed record: 2,193 miles per hour. We're fond of speed records. Over 30 of our parts have broken or still hold speed records for integrated circuits.

UPDATE: SRAM

SRAM innovations and blazing speed put our customers at the head of the performance race.

Besides breaking speed records, our SRAM products offer very low power consumption, innovative circuitry that provides immunity to latchup and ESD tolerance > 2,000 volts per pin. Military versions available, of course. We're committed to being your #1 source for highest speed memory.



World's fastest TTL compatible CMOS SRAM: 7ns.

256x4 1K static RAM takes CMOS and TTL into the high-speed domain formerly available only through ECL.

The benefits:

First, *speed*. Second, *speed*. Third, *more speed*. Our 0.8 micron CMOS process produces *faster* transistors. Plus, we've moved to a 24-pin format from the old 22-pin format, creating a pinout better optimized to take advantage of the chip's high speeds.

Then consider power. Bipolar TTL and ECL approaches consume as much as four times the power as our CMOS parts. Ours keep your system power requirements down, and keep your system *heat* down. They're so cool, in fact, that we can even ship in convenient plastic packaging.

Finally, 300 mil packages instead of the old 400 mil packages allow designers to conserve board real estate.

New 64K SRAM: 25ns in quantity.

Seven available configurations—nibble-wide, bit-wide, byte-wide, separate I/O—give designers choice.

So whatever your configuration need, we have a 64K SRAM available in low power CMOS at the very highest level of performance available.

We offer *five* configurations with 25ns performance: 64Kx1, 16Kx4, 16Kx4 with output enable, and two 16Kx4 with separate I/O. In addition, we offer two 8Kx8 versions with 35ns performance.

Our 0.8 micron process means exceptionally small die, with exceptionally low power requirements.

As a result, we can offer a variety of packaging, *including convenient plastic*, and we can offer the space-saving 300 mil-wide package for *all* configurations.

Maximum power dissipation is a low, low, 100 mA for bytewide parts, and 70 mA for all the others, even at 25ns operating speeds! So your system overall requires less power, and produces less heat.

SRAM: Whoosh list.

CY7C189
16x4 Static RAM 15 ns
CY7C190
16x4 Static RAM 15 ns
CY74S189
16x4 Static RAM 35 ns
CY27LS03
16x4 Static RAM 65 ns
CY27S03
16x4 Static RAM 25 ns
CY27S07
16x4 Static RAM 25 ns
CY7C122
256x4 Static RAM
Separate I/O 15 ns

CY7C123
256x4 Static RAM
Separate I/O 7 ns
CY93422
256x4 Static RAM
Separate I/O 45 ns
CY93422A
256x4 Static RAM
Separate I/O 35 ns
CY93L422
256x4 Static RAM
Separate I/O 60 ns
CY93L422A
256x4 Static RAM
Separate I/O 45 ns

CY7C148
1024x4 Static RAM 25 ns
CY7C149
1024x4 Static RAM 25 ns
CY7C150
1024x4 Static RAM
Separate I/O 15 ns
CY2148
1024x4 Static RAM 35 ns
CY21L48
1024x4 Static RAM 35 ns
CY2149
1024x4 Static RAM 35 ns
CY21L49
1024x4 Static RAM 35 ns

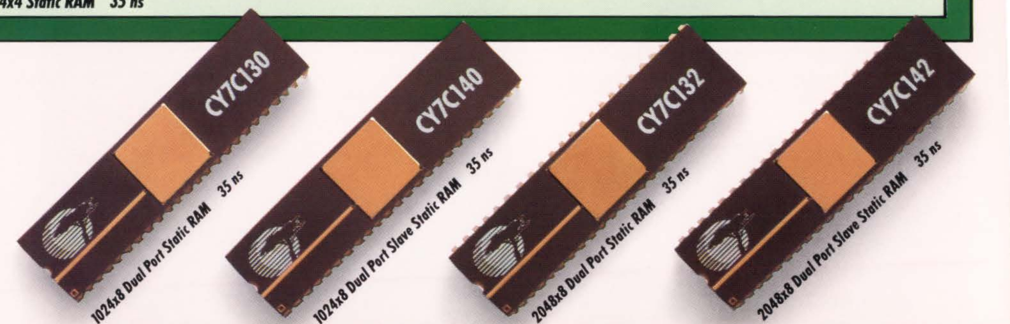
CY7C147
4096x1 Static RAM 25 ns
CY7C130
1024x8 Dual Port
Static RAM 35 ns
CY7C132
2048x8 Dual Port
Static RAM 35 ns
CY7C140
1024x8 Dual Port
Slave Static RAM 35 ns
CY7C142
2048x8 Dual Port
Slave Static RAM 35 ns

CY6116
2048x8 Static RAM 35 ns
CY7C128
2048x8 Static RAM 25 ns
CY7C168
4096x4 Static RAM 25 ns
CY7C169
4096x4 Static RAM 25 ns
CY7C170
4096x4 Static RAM 25 ns
CY7C171
4096x4 Static RAM
Separate I/O 25 ns

CY7C172
4096x4 Static RAM
Separate I/O 25 ns
CY7C167
16,384x1 Static RAM
Separate I/O 25 ns
CY7C185
8192x8 Static RAM 35 ns
CY7C186
8192x8 Static RAM 35 ns
CY7C161
16,384x4 Static RAM
Separate I/O 25 ns

CY7C162
16,384x4 Static RAM
Separate I/O 25 ns
CY7C164
16,384x4 Static RAM 25 ns
CY7C166
16,384x4 Static RAM
Output Enable 25 ns
CY7C187
65,536x1 Static RAM
Separate I/O 25 ns

**variety of configurations available, best speed is listed.*



New, ultra-fast 35ns dual-port SRAM.

Architecture minimizes arbitration bottleneck, for fastest throughput.

System designers, and especially display designers, demand an SRAM solution that eliminates the cookie jar problem of reading and writing to SRAM.

Dual-port SRAM allows access to the same data by two systems, in effect allowing one system to update memory while the other is reading.

There are, then, two limitations to the system's speed.

One is the performance of the SRAM—how fast it can read data, for example. At 35ns, our new parts are nearly 40% faster than 55ns alternatives.

The second speed limitation lies in conflict arbitration—created when there are multiple simultaneous system requests for access to the same RAM location.

All conflicts require one of the requests to *wait* while the other request goes first. This reduces the advantage of dual-port architecture for that period.

The more waiting, the slower the total *system* architecture.

Therefore, the design objective is to reduce conflicts requiring arbitration.

Our architecture reduces the potential area of conflict to the actual address location. This reduces conflicts significantly, compared to architectures that control conflict by restricting access to blocks, or even to the entire part.

The net result—35ns and minimized conflicts—creates a part whose throughput can help you dramatically enhance performance of systems such as video displays.

How our 0.8 micron processing puts you ahead:

Many of our customers tell us that even though a number of vendors are specifying very high speeds, they are having trouble actually *receiving* the highest performance parts.

Here is how our 0.8 micron process technology helps us make the highest performance parts *available* to you:

First, our 0.8 micron processing produces *faster* transistors. The faster the transistor, the faster the part.

Second, 0.8 micron process technology reduces the *loads* imposed on those transistors, allowing them to switch faster, with less power.

Third, we get tighter geometries, tighter spacing, reduced parasitic delays, and overall faster performance.

So we aren't squeezing a process or yield by tight data sheet specifications, in order to claim a best-case speed number.

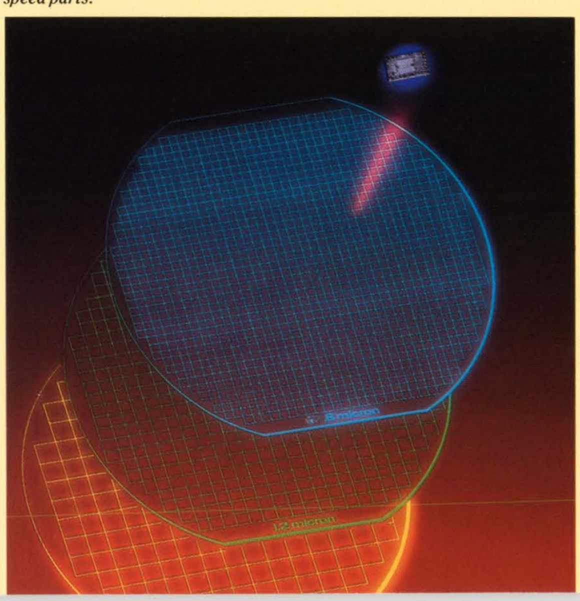
In fact, we've only *begun* to exploit the speed potential of our 0.8 micron process to deliver our ECL-eating 7ns 1K, or our 25ns 64K family.

Finally, consider the benefit of tight geometries on *yield*, and therefore on *availability*. Our 0.8 micron process *substantially* increases the number of die per wafer.

That improves the net die per wafer yields of the high speed parts, making more of the highest speed parts available to our customers.

Our high density, high performance 64K SRAM was featured in the January, 1987 EDN magazine cover story that reviewed new, high density, high performance silicon. This photograph illustrates the yield advantages of 0.8 micron process technology, compared to 1.2 micron or the now archaic 2.0 micron technology.

Yield advantages, in turn, lead to greater availability of the highest speed parts.



Why high performance silicon vendors must control their own processes:

High performance and low power can't be realized *just* through chip architecture.

It takes architecture *plus* state-of-the-art processing to deliver the highest performance silicon. That is why Cypress Semiconductor controls the fabrication process through every stage of manufacturing, in our own facilities, and not through third party silicon foundries.

UPDATE: PROM

CMOS emerges as the state-of-the-art for PROM technology.

How else can you get highest performance, highest density, and low, low power? Other significant Cypress CMOS features include reprogrammability, on-chip diagnostics, and power down options.

New 128K PROM:

At 45ns, there is none faster. High density, small footprint, 100% tested. And reprogrammable.

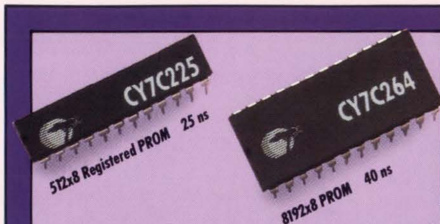
This new part really shows off the newfound strength of CMOS.

First, to our knowledge, it is the *only* high performance 128K PROM available, *regardless* of process.

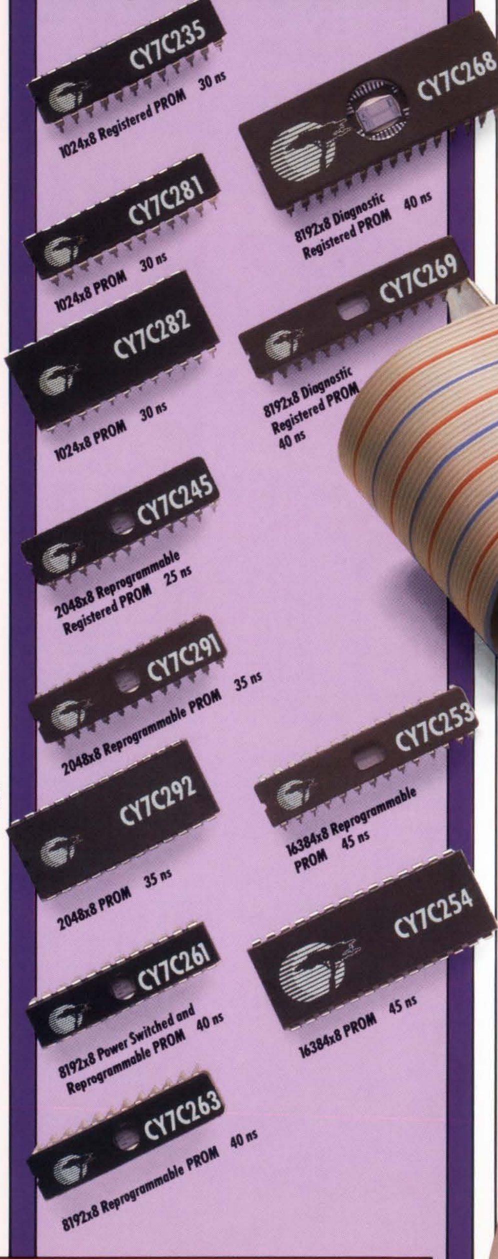
CMOS means very low power. And this new part even offers a power-down standby mode, reducing power consumption to a fraction of any other non-volatile, high-speed memory.

Floating gate technology (see sidebar) gives you 100% tested parts, many with optional windows for easy reprogrammability.

Finally, our tight geometries mean smaller die, which in turn means we can deliver the board-saving 300 mil-wide packages.



PROM: Whoosh list.



UPDATE: PLD

Innovations in high performance programmable logic give you more options.

Products such as our 22V10 illustrate our commitment to create high performance advantages that put you

How floating gate PROM technology puts you ahead:

Floating gate PROM technology is *erasable*, giving you two big benefits.

First, we can test 100%. That means every cell on every part we ship. You get the convenience of the highest incoming quality available.

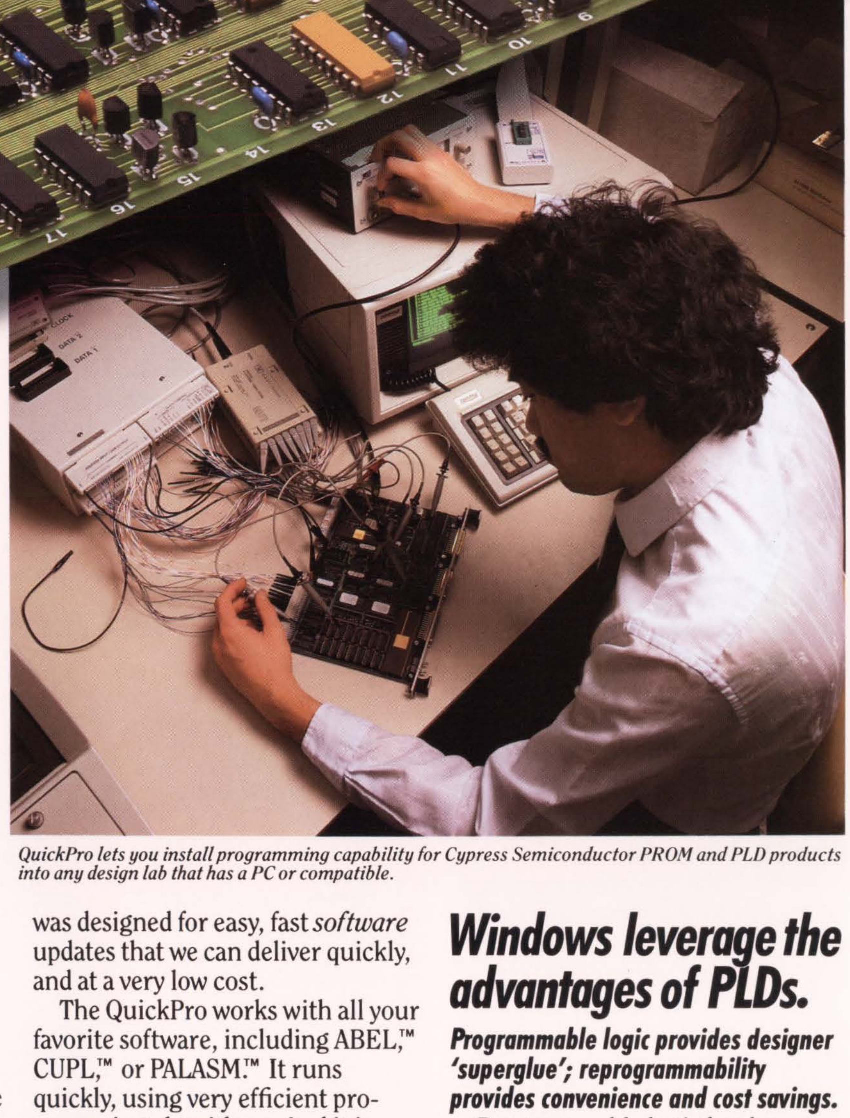
Second, with a windowed package, you've got a reprogrammable part.

That saves you time and trouble in the development lab. And it can save you *considerable* time and trouble in production, protecting you from expensive inventory obsolescence.

All Cypress PROM and PLD parts are fabricated with floating gate memory technology.

ahead. With features like high speed, reprogrammability, variable macrocell architectures, programmable outputs, and more.

QuickPro is an inexpensive development tool that works with a PC to program all present and future Cypress Semiconductor high-speed CMOS PLD and PROM parts. In addition, the QuickPro can read and reproduce the data from competitor's parts onto Cypress parts.



QuickPro lets you install programming capability for Cypress Semiconductor PROM and PLD products into any design lab that has a PC or compatible.

QuickPro™ PLD/ PROM Programmer turns your PC into a foundry.

A QuickPro programmer in your IBM® PC or compatible gives you the easiest, least expensive solution for a quality programmer in every design lab.

Take advantage of our growing family of PLD and PROM parts right now. And don't worry about the next generation of Cypress parts putting your QuickPro behind the times, or costing you an arm and a leg for your programmer upgrade. The system was designed for easy, fast *software* updates that we can deliver quickly, and at a very low cost.

The QuickPro works with all your favorite software, including ABEL,™ CUPL,™ or PALASM.™ It runs quickly, using very efficient programming algorithms. And it is easy to use, with simple menus that prompt you through the programming (or reading) steps easily and quickly.

Add QuickPro to your personal computer, and give yourself the tool you need to take best advantage of our programmable logic and memory.

Windows leverage the advantages of PLDs.

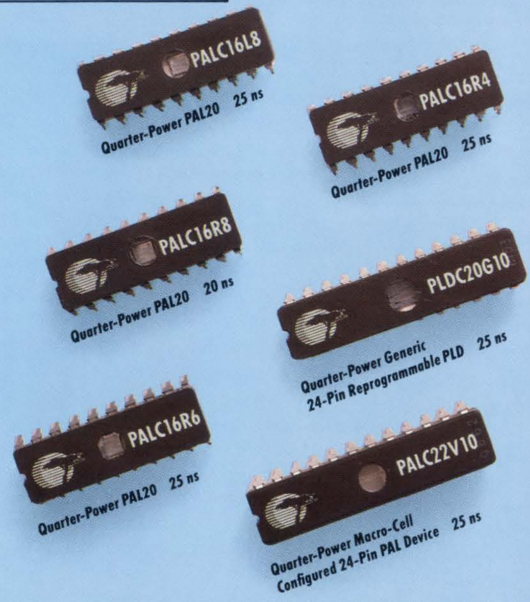
Programmable logic provides designer 'superglue'; reprogrammability provides convenience and cost savings.

Programmable logic has become a basic systems design tool. Designers can collapse multiple chip random 'glue' logic onto a single chip, reducing parts count and reducing board space.

Even better, programmable logic provides flexibility. Since the system can be easily reconfigured, the designer can better adapt to changing system requirements. It is easier

PLD CONTINUES:

PLD: Whoosh list.



to change a PLD, for example, than to redesign an entire printed circuit board, especially when the board is one of today's complex, multilayer designs.

There is also the flexibility for upgrades. New PLDs can be substituted into the original design to simplify system upgrades that take advantage of new software, new peripherals, new communications features, faster memory, and so forth. If PLD devices are used to interface between different subsystems, it is possible to upgrade one subsystem's performance, then reprogram the interface logic on other subsystems, without having to actually redesign the subsystems.

Windowed PLD parts increase that flexibility even further.

In the design lab, windowed parts let the designer try more designs without the worry of wasting expensive or hard to replace parts.

In manufacturing, reprogrammability dramatically reduces the risk and cost of program changes.

Since most manufacturers program PLD parts well before they are actually assembled, there is typically an inventory of programmed parts. Reprogrammability means those parts can simply be erased and programmed with the latest logic version.

There's no one faster. Half-power military PALs. Quarter-power PAL®s.

Featuring the fastest available military PALs (20ns) with half the power. Commercial PALs offer quarter-power with unmatched speed at 25ns.

With our CMOS technology, we offer a better speed-power ratio than bipolar. Blazing speed. Cool, low power. So you can create better performing systems.

U P D A T E :

Logic

CMOS sets the standard for highest performance logic.

Highest speeds, improved density, and substantial power savings of CMOS logic parts make bipolar processes obsolete.

DESC certifies Cypress Semiconductor operation.

Certification for JAN product will simplify qualification of our high performance circuits in military applications.

Because Cypress Semiconductor is in the business of highest performance, lowest power parts, we have always recognized the importance of military applications in our overall market.

In fact, since the company's inception, all Cypress Semiconductor military products have been processed to MIL-STD-883.

Because we regard military applications as a key part of our company strategy, we received certification as a DESC manufacturer in record time. The benefits to our military customers are several:

First, military business is a high priority, not a stepchild. That makes it easier for our military customers to do business with us than with non-military oriented semiconductor companies.

Second, we now offer the first in a series of JAN products: the JM38510/289 4Kx1 SRAM. JAN qualification makes it even easier for our military applications customers to qualify the parts they need for highest performance and lowest power—Cypress Semiconductor circuits.

The higher the performance requirement, the more likely you are to find our CMOS circuits. DESC-certification of our manufacturing facilities makes it even easier for our military customers to specify Cypress Semiconductor.

Logic: Whoosh list.

CY2901C
CMOS 4-Bit Slice 31 ns

CY2909A
CMOS Microprogram Sequencer 40 ns

CY2911A
CMOS Microprogram Sequencer 40 ns

CY2910A
CMOS Microprogram Controller 50 ns

CY3341
64x4 FIFO Serial Memory 2 MHz

CY7C401
Cascadeable 64x4 FIFO 15 MHz

CY7C402
Cascadeable 64x5 FIFO 15 MHz

CY7C403
Cascadeable 64x4 FIFO with Output Enable 25 MHz

CY7C404
Cascadeable 64x5 FIFO with Output Enable 25 MHz

CY7C408
Cascadeable 64x8 FIFO with Output Enable 35 MHz

CY7C409
Cascadeable 64x9 FIFO 35 MHz

CY7C510
16x16 Multiplier Accumulator 45 ns

CY7C516
16x16 Multiplier 38 ns

CY7C517
16x16 Multiplier 38 ns

CY7C901
CMOS 4-Bit Slice 23 ns

CY7C909
CMOS Microprogram Sequencer 30 ns

CY7C911
CMOS Microprogram Sequencer 30 ns

CY7C910
CMOS Microprogram Controller 40 ns

CY7C9101
CMOS 16-Bit Slice 30 ns

**variety of speeds available, best speed is listed.*

16-Bit Slice. 30ns.

Fast. Low power. And second sourced.

Some applications require an efficient instruction set and brute performance. Such as high-speed controllers, emulators, accelerators, and the like.

New, 64x9 Cascadeable FIFOS: 35MHz.

Creating your own custom microprocessor using bit slice and your own microcode means you can create the most *efficient* instruction set, tailored just to your requirements.

Then execute those instructions at blazing speeds, using our high performance 16-bit slice family.

This part consumes just a tenth the power of a system built from four 4-bit slice bipolar 2901-type parts, and runs *faster*.

Bipolar technology can't deliver the density needed for a 16-bit slice. That's why all the contenders are CMOS. Our pinout is the only second-sourced 16-bit slice pinout (the other pin-compatible source is AMD).

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Higher density, lower power, and breaking speed records.

Open the communications bottlenecks between your loosely coupled asynchronous systems or subsystems with these high speed, *cascadeable* FIFOs.

Here's what we've done to give you the highest available performance:

First, we've virtually eliminated the 'bubble through' that throttles registered array FIFOs down. That makes information available to the output side nearly instantaneously, increasing system throughput.

Second, we've made the parts cascadeable. So if you're using four 64x9 parts to create a 256x9 capacity, you may easily cascade the four devices and still run at full speed.

Third, we offer the extra added convenience of output enable on our 64x8 version.

Finally, we've given you up to 35MHz to work with. That's the fastest cascadeable FIFO around, by as much as 40%.

EDITORIAL

IRAs deserve another chance

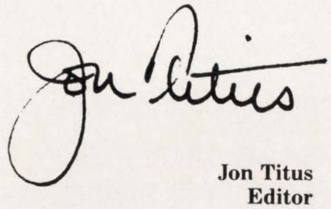
Now that many of us have made our last tax-exempt individual retirement account (IRA) contribution, it's worth taking another look at pension benefits. In particular, the tax-reform bill passed late last year changes the ways we'll plan for retirement. The new law reduces from ten years to five the maximum time for an employee to become vested in a retirement plan. For most engineers, however, the new tax legislation also renders IRA contributions taxable. To help nonvested employees, the IEEE has proposed a change in the tax law that makes IRA contributions tax free until an employee is fully vested in a retirement plan. As a consequence, new employees would gain five years of tax-exempt IRA contributions that would bolster their pension benefits.

Many workers want tax-exempt IRAs because pension coverage at work is inadequate. According to the Pension Rights Center in Washington, DC, many employees are disillusioned with private pension systems. Figures from the IEEE's Pension Committee show why workers are upset. For example, depending on their work history, pension coverage for engineers who have essentially the same job, the same salary, and the same working conditions can vary widely in the last years of employment. When all other factors are equal, an employee who works 40 years for one employer receives a significantly larger pension than a worker who labors for 40 years but changes jobs every 10 years.

The message is clear. The promise of future pension benefits pressures employees to continue working for a company, often under poor conditions. Regardless of the job, employees try to hang on until the time when they are 100% vested in a pension plan. As a result, they're subject to firings, layoffs, mergers, and other uncertainties in the life of a corporation, in the hope of regular salary increases and a reasonable pension. Cutting the maximum vesting period to five years helps many employees. Portable pensions would do even more to break the chains of servitude that bind many engineers to their employer.

IRAs can serve as a means for providing portable pensions, one that would let you move from job to job while you preserve the equivalent of pension benefits. Employer contributions would go directly to your IRA rather than be held in a nebulous accounting system. Instead of making an employee wait for a 5-year vesting period, contributions would increase over the period until they reach their maximum in five years.

You could put Social Security contributions in an IRA, too. Under a plan proposed by representative Newt Gingrich (R-GA), IRAs would replace Social Security accounts. As a consequence, Social Security withholding would go directly to your IRA, along with a maximum of 10% of your salary. Under Gingrich's plan, you would still choose where you would invest your IRA funds. All in all, it's worth considering IRAs as the basis for pension-benefit reform.



Jon Titus
Editor

Hitachi's Hi-BiCMOS™ SRAMs Deliver Explosive Speed, with Minimal Power Consumption

The red-tailed hawk is an incredible performer. For hours on end he soars effortlessly aloft in thermals, barely moving a muscle. Then, instantly, he descends upon his prey, achieving terminal velocity in a flash.

Now, Hitachi's revolutionary Hi-BiCMOS process brings you power-efficient, high-speed performance in a new series of SRAMs. Hi-BiCMOS transcends generic Bi-CMOS by intermixing true bipolar and CMOS devices *at the basic cell level.* It's a generation ahead of Bi-CMOS, and two generations ahead of pure CMOS. The results of this fantastic new process technology can be seen in products like our HM6787-25 (64K x 1) and HM6788-25 (16K x 4) 64K-bit SRAMs.

These devices have a 25ns access time, are TTL I/O compatible, yet draw no more power than ordinary CMOS. And, they're available *today*, in production quantities. Now, you can speed up the cycle time of your main and cache memories, image processing, or CAD/CAM systems without paying power consumption or heat penalties.

Hitachi's Hi-BiCMOS process is blue sky technology brought down to earth. As you well know, it's one thing to develop new product ideas—the trick is to be able to make the product. Hitachi's done *both*. That's because we've had more than two years' experience using Hi-BiCMOS internally, in our gate arrays. Being first has given us such an edge that we have a variety of Hi-BiCMOS SRAMs available now—in plentiful supply—with many more devices coming soon.

For example, we'll soon introduce 64K SRAMs with 15ns access time, ECL compatible I/O, and

Incredible

power consumption that's only one-half of standard ECL. And with our Hi-BiCMOS technology so firmly in place, 20ns 256K SRAMs with ECL or TTL I/O aren't far behind.

Soar above your competition with Hitachi. Most MOS SRAMs you're using today will never be available in much faster versions. That's because pure CMOS is getting close to its limits. This is no secret. It's the reason why everybody is struggling to bring Bi-CMOS products to market. . . everybody except Hitachi. After all, we already have Hi-BiCMOS products available *today*. With Hitachi, you're a generation ahead of where everyone else hopes to be *tomorrow*.

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TAGRAM comes in three speed grades: 20, 25 and 35ns. And every MK41H80 cache TAGRAM is available in 300 mil, 22-pin plastic and ceramic DIPs. What's more, TAGRAM's full-speed read access ensures that even copy-back designs can be implemented without ever having to wait. And it features Flash Clear – the function requested most often by cache system designers. So your cache can be wiped clean to all zeros in 40ns. Max.

High-performance cache applications demand high-speed solutions. If you'd like to realize a 30% reduction in access time compared to discrete solutions – plus a substantial reduction in the cost of component real estate – start increasing your cache flow with the newest member of our family. The MK41H80 TAGRAM.

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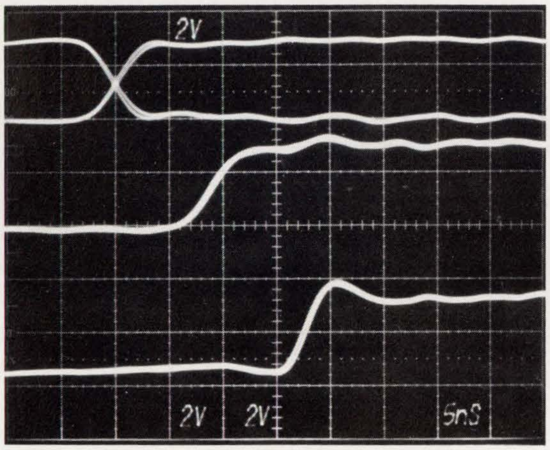
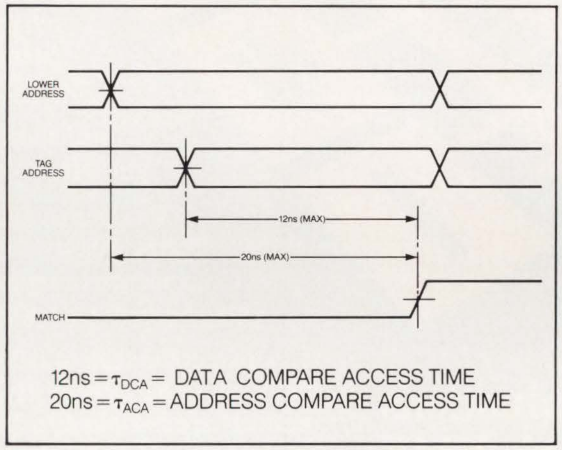
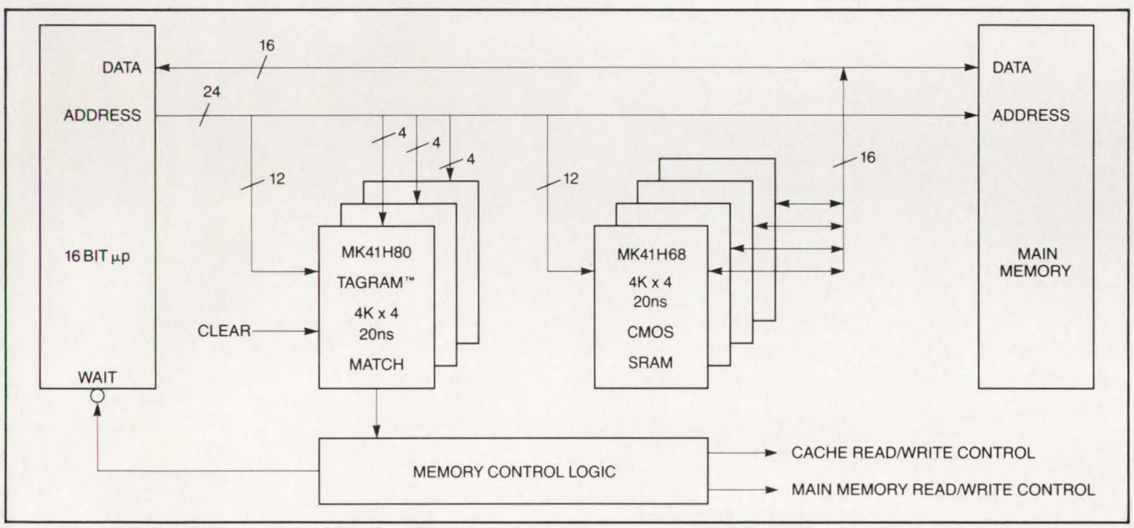


Actual MK41H80 TAGRAM Scope Trace Photograph



Match Access Timing



Direct Mapped Cache System Block Diagram

DEVICE	CONFIG	PINS	$\overline{CE}$	$\overline{CS}$	$\overline{OE}$	$\overline{CLR}$	MATCH
41H68	4Kx4	20	X				
41H69	4Kx4	20		X			
41H78	4Kx4	22	X		X		
41H67	16Kx1	20	X				
41H66	16Kx1	20		X			
41H79*	4Kx4	22	X		X	X	
41H80	4Kx4	22			X	X	X

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*To be announced. TAGRAM is a trademark of Thomson Components-Mostek Corporation.

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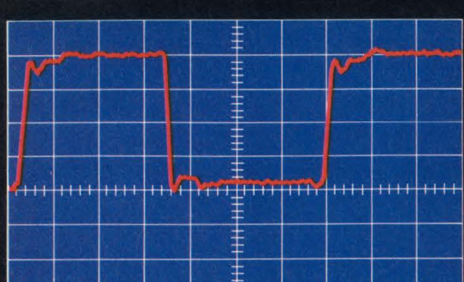

Exceptionally clean signals characterize Hybricon's backplanes. (Illustrated from actual customer photos.)

An experienced engineer knows that **safe noise margins must be "designed in,"** reliability of operation depends on it.

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- Traffic density
- Coincidence of signal currents
- Optional hardware additions

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- Signal propagation delay
- DC voltage drops

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Hybricon Engineers understand your problems; they have direct experience in high speed system design. Hybricon backplanes rate high in performance because they incorporate **basic and solid engineering principles.**

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CIRCLE NO 115

Manufacturers of fast CMOS logic families take sides in packaging controversy

J D Mosley, *Regional Editor*

Advanced CMOS logic (ACL) devices have become the focus of the most bitterly debated packaging controversy in 20 years. These ACL chips are the fastest low-power glue-logic ICs available, but the increased speed has generated severe problems for the manufacturers. As a result, Texas Instruments—the company that set the TTL packaging standards in the 1960s—has announced the forthcoming introduction of a family of logic devices with packages that deviate from those standards. This deviation is part of an attempt to solve the noise problem, but it has sparked a row about the virtues of the new packaging style, setting TI and its allies against other makers of ACL parts.

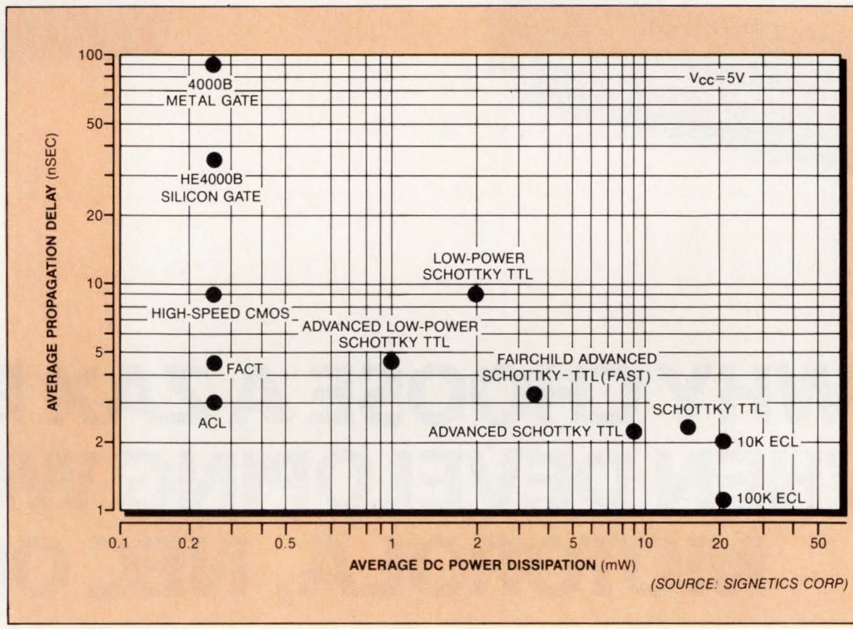

***Fig 1—Illustrating the comparative speed and power characteristics** of the various CMOS and bipolar logic families, it's clear that advanced CMOS logic offers speeds that rival those of bipolar devices with far less power consumption.*

TI, Philips International NV, and the latter's US subsidiary Signetics jointly developed the Enhanced Performance Implanted CMOS (Epic) ACL devices, which feature ground and V_{CC} pins located in the center of a DIP's pin rows. Other ACL devices—manufactured by RCA Solid State, Fairchild Semiconductor, Integrated Device Technology, and VTC—locate these pins in the corners of the standard TTL packaging scheme. Taken together as a class, these chips offer an optimal combination of high speed and low power consumption (**Fig 1**).

Featuring a 1-μm gate length, Epic ACL devices spec the fastest internal gate speeds in the industry —0.5 nsec. Yet in their attempts to achieve this impressive speed, the developers have encountered serious ground-bounce problems, which have delayed production of this logic family. It's these attempts to deal with the noise problems generated by subnanosecond internal propagation delays that have led to the change in package style.

Even so, the overall specs quoted by each ACL manufacturer are quite similar. Each company asserts that its ICs offer overall propagation delays (as opposed to internal delays) in the 2- to 3-nsec range and can operate at clock frequencies reaching 150 MHz. Although competitors have alleged that the TI and Philips/Signetics chips spec faster operating speeds, company officials at TI now deny such speculative comments and maintain that noise control is the overwhelming design consideration when selecting an ACL chip.

Center pin vs corner pin

To understand the nature of the package controversy, it would serve clarity to stand up to the welter of acronyms and terms for the various devices involved in the fray, and to establish some convenient terms that identify the rival camps (for more information on the differences, besides packaging, between the various device types, see **box,** "Features of the ACL families"). As noted, TI calls its logic family "Epic ACL." Signetics and Philips, however, simply refer to their logic family as "ACL." From this point forward, ICs based on this joint development will be called "center-pin devices."

RCA's ACL ICs, introduced in March of 1986, feature 1.5-μm geometries. The RCA ACL family may simply be called "RCA ACL." Fairchild offers the 2-μm Fast Advanced CMOS Technology (Fact) devices, which were introduced in October of 1985 as pin-compatible replacements for power-hungry bipolar and slower HCMOS logic ICs. IDT and VTC supply the 1.2-μm Fast CMOS TTL-compatible (FCT) family of

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CIRCLE NO 114

parts. IDT and VTC did not jointly develop this family, but the parts introduced by each company are so similar that the two companies agreed early in 1987 to be second sources for each other. The chips from all four companies will be jointly referred to as "corner-pin devices."

Prices for the ACL ICs currently available in production quantities can vary widely and will depend on the logic function, process technology, and manufacturer. Fact ICs range from $0.328 for a 74AC(T)00 NAND gate to $1.416 (100) for a 74AC(T)245 bidirectional transceiver. RCA quotes prices ranging from $0.31 for its 74AC(T)00 to $2.31 (100) for its 74AC(T)191 4-bit binary counter. IDT's prices for commercial-grade FCT devices extend from $1.80 for a 74FCT138 1-of-8 decoder to $19.25 (100) for a 74FCT827 10-bit buffer/line driver. VTC gives a price range of $1.95 to $13.45 (100) for its commercial FCT family.

Prices for CMOS- and TTL-compatible parts in these product lines are identical, but the military versions of each manufacturer's ICs cost more. In addition to the ACL glue-logic chips offered by its competitors, Fairchild also sells a Fact 16×16 multiplier dubbed the 74ACT1010. You can buy this 48-pin ceramic LSI IC for $57.20 (100).

Awaiting introduction

TI claims to have samples of its Epic ACL family, but it's currently quoting a price for only one ACL IC—the 74AC(T)11074 dual D-type flip-flop—which costs $0.44 (1000). By comparison, the RCA version (74AC(T)74) sells for $0.39 (1000), and Fairchild's version costs $0.34 (1000). Philips/Signetics has not yet made public the prices for its product line. (To check the availability of current parts, see the **table** starting on pg 77.)

The origins of the packaging controversy lie in a noise problem that has plagued CMOS development. As semiconductor technology has advanced, the speed of CMOS devices has steadily increased, but the faster switching speeds have resulted in reflections, ringing, and glitches, induced both on pc boards and within the device packages. This noise can result in false output signals, lost data, and improper latching.

CMOS devices are more susceptible to noise than equivalent bipolar versions, because of the significantly shorter gate lengths necessary to boost CMOS performance to bipolar levels. The shorter the gate length, the faster a CMOS device can function, and the more noise it generates.

One critical noise problem is called "ground bounce." When several devices switch simultaneously in one logic package, a voltage spike surges along the ground paths within the package. This ground-bounce surge can cause unwanted latching and produce indeterminate logic outputs. Such surges in a bipolar device can also cause transients to kick back through the input pins.

TI argues that the corner-pin package magnifies the noise problem. The leads of a bypass capacitor act as inductors at clock speeds over 100 MHz. This inductance interacts with the capacitor to create a resonant circuit. Input switching in corner-pin devices can cause this resonant circuit to create voltage spikes as high as 2V.

To increase noise immunity, decrease sensitivity to ESD, and prevent latch-up in their ACL families, TI and Philips/Signetics found it necessary to deviate from standard

Features of the ACL families

The following description of fast advanced CMOS logic devices lists the families in order of their appearance on the market. You'll note the progressive shrinking of the process geometry with each introduction.

Fact—Fairchild's Advanced CMOS Technology uses a 2-μm isoplanar silicon-gate CMOS process and features industry-standard functions and pinouts for SSI and MSI applications. Available with either CMOS- or TTL-compatible inputs, Fact family devices serve as direct replacements for more than 50 low-power Schottky and advanced low-power Schottky devices.

RCA's ACL—This process features a 1.5-μm geometry, on-chip, dual-diode ESD input protection, and an epitaxial layer that eliminates SCR latchup. You can order more than 40 devices, with CMOS- or TTL- compatible inputs, in plastic DIPs, ceramic DIPs, or small-outline packages.

FCT—Available from VTC Inc and Integrated Device Technology. This logic family features 1.2-μm effective gate lengths and a proprietary double-metal CMOS process. These FCT devices boast 5000V of input ESD protection, and they can withstand trigger currents in excess of 200 mA without latch-up.

Epic ACL—Jointly developed by TI, Philips, and Signetics. The 1-μm technology used to fabricate TI's dynamic RAM forms the basis for the Epic ACL products. The process uses a twin-well structure to produce high packing densities. Yet the shrunken geometry has fostered larger packages, different pinouts, and a flow-through architecture. Specs boast of a 24-mA output-drive capability and the fastest switching speeds in the industry, but the family is only available in sample quantities.

TTL packages. The 74AC11000 center-pin translation of a standard 74AC00 quad 2-input NAND gate adds two extra ground and power pins to the package and relocates virtually every pin on the chip. Four extra pins expand a standard 74AC240 3-state octal buffer into a 24-pin 74AC11240, resulting in a 10% increase in package dimensions and an approximately 17% increase in the number of pins **(Fig 2)**.

The center-pin package rearranges the logic devices' pins to provide a logical and continuous flow of data. Essentially, signals enter a center-pin package from the right side and exit from the left. TI and Philips/Signetics assert that the uniform signal paths produced by this flow-through architecture can reduce pc-board trace lengths and simplify board layout, thus further improving signal integrity throughout the design.

Because the ground and power pins are located much closer to each other in a center-pin package, the bypass capacitor's leads are significantly shorter than those required for a corner-pin package, which places the ground and power pins at diagonally opposite ends of the package. Shorter capacitor leads result in less parasitic lead-frame inductance and decreased resonance. The center-pin packages thus reduce the chips' internal inductance and, as a consequence, provide increased resistance to ground bounce and crosstalk. The central pin location also shortens the power-supply connections within the device, further reducing self-induction.

The Epic ACL fabrication process, like the package, differs significantly from that of the other ACL technologies and has a beneficial impact upon the noise problem. Epic ACL features a twin-well structure that facilitates high packing densities and provides 1-μm effective channel lengths. The transistors' silicide gates and drains reduce internal interconnect resistance and hasten propagation. The use of sidewall oxidation within the transistors reduces internal capacitance to boost speeds further. The TI ICs also boast an output-edge-control (OEC) feature that further reduces the impact of voltage spikes on supply pins and limits the effective dv/dt.

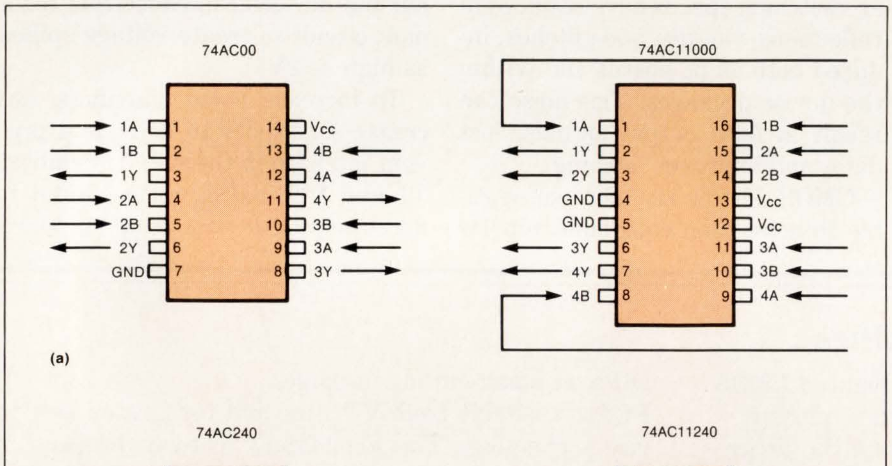

***Fig 2—The 74AC11000 center-pin translation** of a standard 74AC00 quad 2-input NAND gate adds two extra ground and power pins to the package and relocates virtually every pin on the chip. Four extra pins expand a standard 74AC240 3-state octal buffer into a 24-pin 74AC11240.*

Noise problem limited

With respect to the packaging issue, one point of contention is that the TI proposal alters the package for every device in its ACL family, even though ground-bounce is only a problem for certain logic devices—notably 8-, 9-, and 10-bit latched devices. The corner-pin proponents argue that it's unnecessary to alter the packages of an entire logic family to correct a relatively isolated problem. TI and company, however, consider the inductance reduction resulting from the flow-through architecture sufficient justification for altering the packages of the entire Epic ACL product line.

The center-pin manufacturers insist that all deviations were necessary to provide for multiple supply and ground lines. Advocates of the corner-pin packages, however, see a problem in the fact that the center-pin package is larger, with two or four more pins per package. Richard Funk, manager of standard-IC applications at RCA and chairman of the JEDEC JC40.2 committee, which standardizes electrical specifications for the semiconductor industry, insists that any benefit gained from relocating pins would be offset by the increased external interconnect inductance resulting from the additional pins; consequently, the alleged solution merely moves the noise off the chip and onto the board.

Funk suggests that, rather than depart radically from standard chip packages, chip designers concen-

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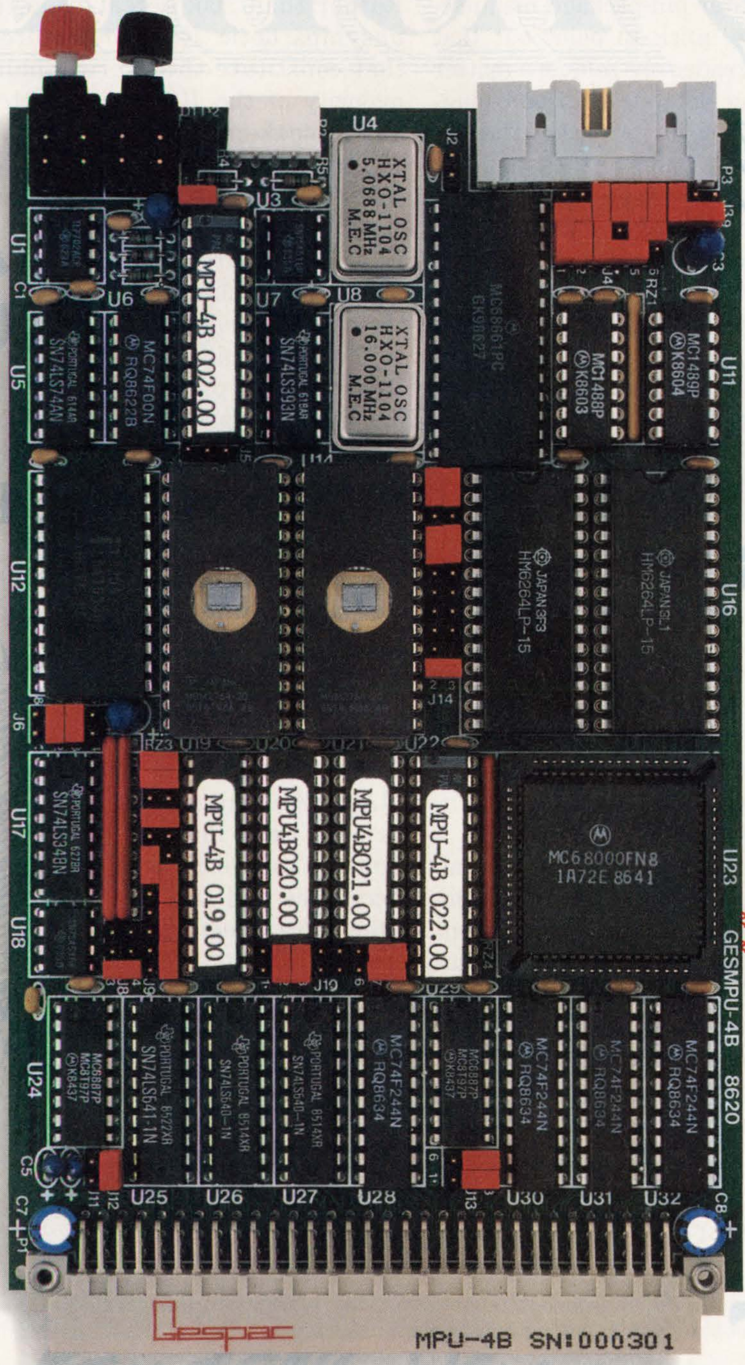

Actual Size

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trate on minimizing dv/dt, and that pc board designers use the following approach to reducing noise problems:

- Opt for the smallest IC package; use surface-mount devices, if possible. (Manufacturers of corner-pin devices also note that, as the industry converts to surfact-mount devices, noise problems will diminish because of the smaller package and shorter interconnects.)
- Follow low-level RF and ECL rules when laying out a pc board.
- Use CMOS-level parts, when feasible, because they trigger at 1.5V. TTL-level devices trigger at 0.8V.

With regard to this last point, however, you should be aware that the 0 to 5V CMOS voltage levels can translate into a higher dv/dt than TTL voltage levels, which only range from 0.3 to 3.5V. The rail-to-rail voltage swings of CMOS-level devices can result in larger transient voltage spikes travelling across a pc board.

Standard package has virtues

Makers of corner-pin devices find other reasons to stay with the standard package. They assert that no insurmountable noise problems exist in the corner-pin ACL families currently on the market. What's more, the corner-pin devices' smaller packages consume less board space than comparable center-pin packages.

Still other manufacturers of fast CMOS logic maintain that the standard corner-pin packages are not only adequate, but necessary. Jeff Hutton, VTC's CMOS product line manager, stresses that IC manufacturers have a duty to adhere to standards. In the absence of such adherence, designers cannot easily address interface considerations, upgrade existing designs, or plan future development with confidence. Right now, the standard corner-pin package style provides designers with an easy path for upward migration through the various bipolar and CMOS logic families.

The center-pin-package manufacturers are quick to point out that board upgrades are seldom a matter of popping out one chip and plugging another in its place. The designer must balance the new IC's speed or power improvements with timing and voltage considerations elsewhere on the board. Because some degree of design alteration is always necessary, TI and Philips/Signetics are betting that designers won't resist the packaging change that accompanies this faster-than-ever CMOS logic.

Charges and countercharges keep flying. Corner-pin advocates allege that the 1-μm Epic ACL is simply too fast to provide reliable operation, no matter what kind of package envelopes it, and that this fact explains why TI has not yet brought chips to market. Champions of the center-pin package brush aside this charge, stating that faster ICs are the natural result of advancing technology and must be considered a desirable result rather than an avoidable problem. The corner-pin supporters reply that integration, rather than deviation, is the solution: LSI and VLSI designs that incorporate the glue logic will replace the discrete logic families, so a new package is neither necessary nor desirable. "There will always be a need for discrete glue logic," retort the center-pin boosters.

TI has no intention of bringing the issue before a standards board. Rather than risk defeat from the unsympathetic IC manufacturers that constitute the overwhelming majority of the JC40.2 committee, TI will make no formal request for JEDEC approval of the packaging scheme. Instead, to avoid accusations of nonconformity with approved standards, the Epic ACLs have part numbers that distinguish them as center-pin devices.

The standard-logic part numbers have a 2-digit prefix: "74" for commercial parts and "54" for military parts. Two or three letters, indicating the process technology used to fabricate the IC, follow the prefix. The final two or three digits indicate the IC's logic function. TI and Philips/Signetics have added two numeral ones immediately after the process letters, and the three digits that follow indicate the logic function. For example, a center-pin version of the 74AC00 is numbered 74AC11000. This numbering scheme has let TI and Philips/Signetics circumvent the concerns of the JC40.2 committee and take the packaging alternative directly to their customers.

Even though production quantities of the center-pin logic chips aren't yet available, TI has extensively publicized data and specs for the Epic ACL family. Critics claim

For more information . . .

For more information on the advanced CMOS logic families described in this article, circle the appropriate numbers on the Information Retrieval Service card or contact the following manufacturers directly.

Fairchild Semiconductor Corp
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(408) 864-6250
Circle No 712

Integrated Device Technology Inc
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(408) 727-6116
Circle No 713

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Somerville, NJ 08876
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Signetics Corp
Box 3409
Sunnyvale, CA 94088
(408) 746-2199
Circle No 715

Texas Instruments Inc
Box 809066
Dallas, TX 75380
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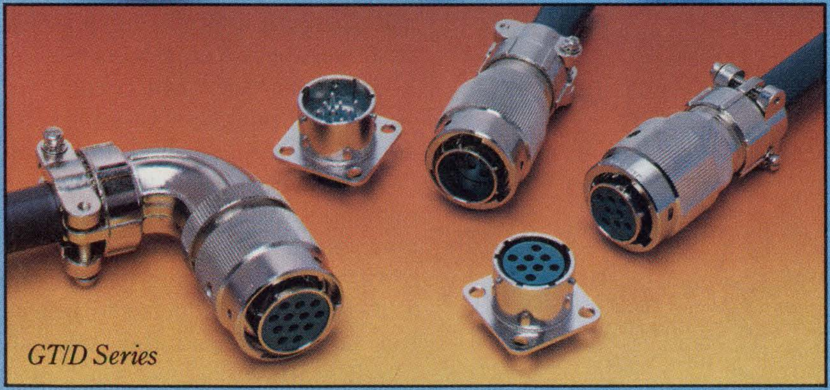
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that these specifications are meaningless if engineers can't order products that meet them. Fairchild goes so far as to maintain that there really is no packaging controversy, because there are no commercially available center-pin devices. Fairchild representatives allege that the TI camp is merely attempting to create confusion among design engineers and cripple Fairchild's early lead in the market for fast CMOS logic devices.

Through it all, as the various manufacturers take their stand on the issue, system designers are left without a clear sense of what parts to specify for glue-logic circuits. Unsure of the ultimate size and features of the next generation of glue logic, they may simply decide not to decide—thereby stalling the market for those manufacturers that are currently furnishing ACL devices as replacements for existing bipolar devices.

Another source provides one final perspective on the controversy. It is interesting to note that manufacturers of gallium-arsenide (GaAs) ICs also faced noise problems in circuits that operate at frequencies reaching 1 GHz, and they too turned to a center-pin package. Complex MSI and LSI GaAs ICs also employ multilayered ceramic packages with as many as 132 leads to further reduce transient signals. Tom Reeder, VP of GaAs-IC marketing and sales at TriQuint Semiconductor in Beaverton, OR, envisions a day when silicon ICs are capable of clocking at frequencies in the hundreds of megahertz. "Whether or not [CMOS ICs] need [a new packaging scheme] right now, they will have to have one in the future, because the signals are tending to become faster over time." **EDN**

Article Interest Quotient
(Circle One)
High 506 Medium 507 Low 508

AVAILABILITY OF ACL ICs

LOGIC FUNCTION		CORNER-PIN PACKAGES				CENTER-PIN PACKAGES	
NUMBER	DESCRIPTION	FACT	RCA ACL	VDT FCT	IDT FCT	EPIC ACL	PHILIPS/ SIGNETICS
000	QUAD 2-INPUT NAND GATE	A	A			S	
002	QUAD 2-INPUT NOR GATE	A				S	S
004	HEX INVERTER	A	A				
005	HEX INVERTER (OPEN-DRAIN)		A				
008	QUAD 2-INPUT AND GATE	A	A			S	
010	TRIPLE 3-INPUT NAND GATE	A				S	
011	TRIPLE 3-INPUT AND GATE	A					
014	HEX-INVERTER (SCHMITT TRIGGER)	A					
020	DUAL 4-INPUT NAND GATE	A				S	S
027	TRIPLE 3-INPUT NOR GATE					S	S
030	8-INPUT NAND GATE						S
032	QUAD 2-INPUT OR GATE	A	A			S	
074	DUAL D-TYPE FLIP-FLOP	A	A			A	S
086	QUAD 2-INPUT EXCLUSIVE-OR GATE		A				
109	DUAL JK FLIP-FLOP	A	A			S	S
138	3- TO 8-LINE DECODER (INV)	A	A		A		
139	DUAL 1-OF-4 DECODER	A			A		
151	8-INPUT MULTIPLEXER	A					
153	DUAL 4-INPUT MULTIPLEXER	A					
157	QUAD 2-INPUT MULTIPLEXER	A	A				
158	QUAD 2-INPUT MULTIPLEXER (INV)	A	A				
161	SYNC 4-BIT BINARY COUNTER (ASYNC RESET)	A	A		A		
163	SYNC 4-BIT BINARY COUNTER (SYNC RESET)	A			A		
164	SYNC 4-BIT BINARY COUNTER (SYNC RESET)		A				
169	SYNC 4-BIT UP/DOWN BINARY DECADE COUNTER	A					

Table continued on pg 78

KEY:
A = AVAILABLE IN PRODUCTION QUANTITIES
S = SAMPLE QUANTITIES ONLY
INV = INVERTING

AVAILABILITY OF ACL ICs

LOGIC FUNCTION		CORNER-PIN PACKAGES				CENTER-PIN PACKAGES	
NUMBER	DESCRIPTION	FACT	RCA ACL	VDT FCT	IDT FCT	EPIC ACL	PHILIPS/ SIGNETICS
174	HEX D-TYPE FLIP-FLOP (WITH RESET)	A					
182	CARRY-LOOKAHEAD GENERATOR				A		
191	SYNC 4-BIT BINARY COUNTER		A		A		
193	SYNC 4-BIT BINARY COUNTER		A		A		
238	3- TO 8-LINE DECODER		A				
240	OCTAL BUFFER/ LINE DRIVER (INV)	A	A	A	A	S	
241	OCTAL BUFFER/ LINE DRIVER	A	A				
244	OCTAL BUFFER/ LINE DRIVER	A	A	A	A	S	
245	OCTAL BUS TRANSCEIVER	A	A	A	A		
251	8-INPUT MULTIPLEXER (3-STATE)	A					
253	DUAL 4-INPUT MULTIPLEXER (3-STATE)	A					
257	QUAD 2-INPUT MULTIPLEXER	A	A				
258	QUAD 2-LINE TO 4-LINE DATA SELECTOR	A	A				
273	OCTAL D-TYPE FLIP-FLOP	A			A		
280	8-BIT ODD/EVEN PARITY GENERATOR/ CHECKER		A				
283	4-BIT FULL ADDER		A				
299	OCTAL UNIVERSAL SHIFT REGISTER				A		
373	OCTAL D-TYPE TRANSPARENT LATCH	A	A	A	A	S	
374	OCTAL D-TYPE FLIP-FLOP	A	A	A	A		
377	OCTAL D-TYPE FLIP-FLOP	A			A		
521	8-BIT COMPARATOR				A		
533	OCTAL TRANSPARENT LATCH (INV)		A	A	A		
534	OCTAL D-TYPE FLIP-FLOP (INV)		A	A	A		
540	OCTAL BUFFER/ LINE DRIVER (INV)	A	A				

Table continued on pg 80

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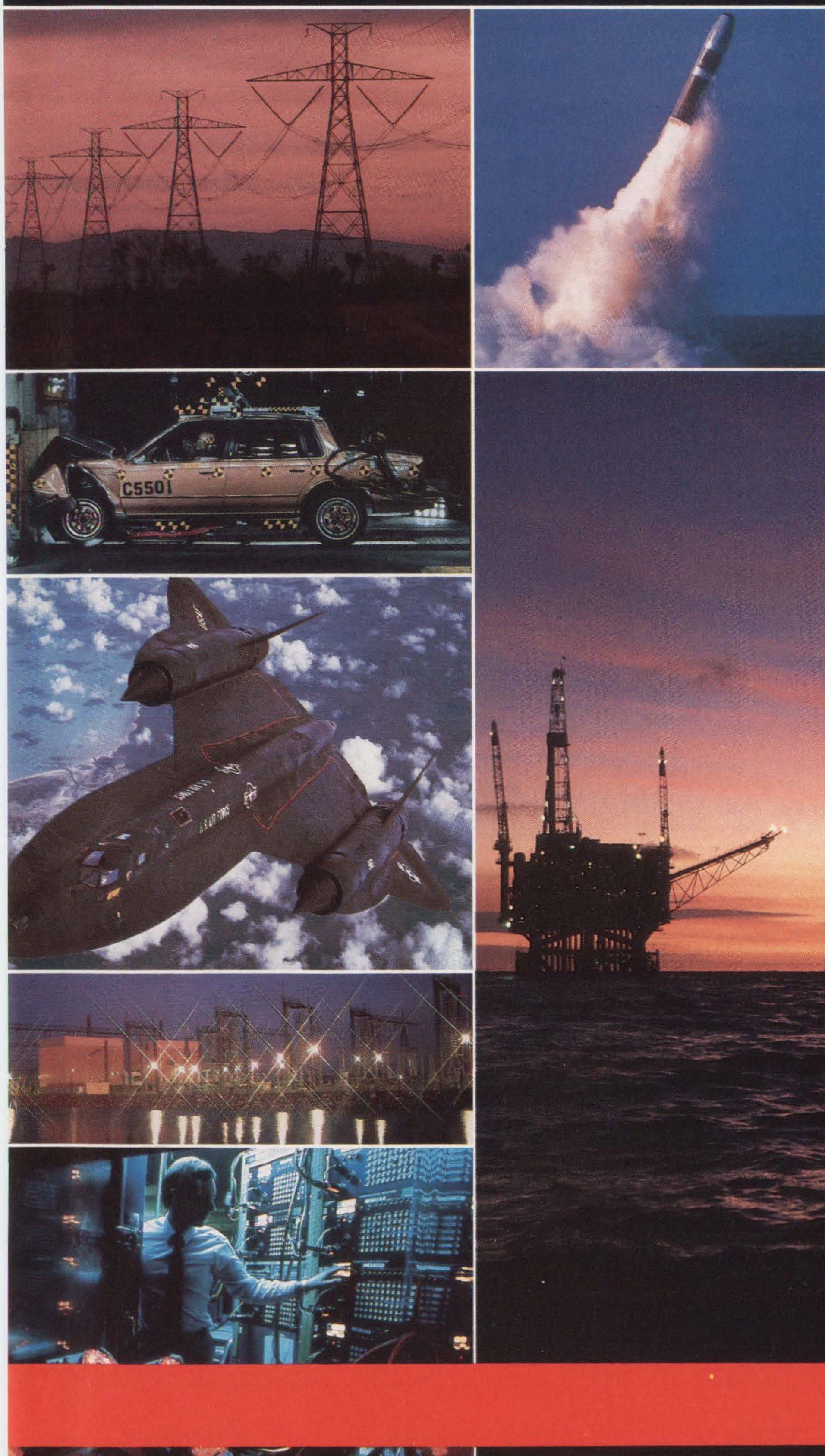

AVAILABILITY OF ACL ICs

LOGIC FUNCTION		CORNER-PIN PACKAGES				CENTER-PIN PACKAGES	
NUMBER	DESCRIPTION	FACT	RCA ACL	VDT FCT	IDT FCT	EPIC ACL	PHILIPS/ SIGNETICS
541	OCTAL BUFFER/ LINE DRIVER	A	A				
573	OCTAL TRANSPARENT LATCH	A		A	A		
574	OCTAL D-TYPE REGISTER	A		A	A		
640	OCTAL BIDIRECTIONAL TRANSCEIVER (INV)			A	A		
645	OCTAL BIDIRECTIONAL TRANSCEIVER			A	A		
646	OCTAL BUS TRANSCEIVER (INV)	A	A				
648	OCTAL BUS TRANSCEIVER (INV)		A				
821	10-BIT D-TYPE FLIP-FLOP			A			
822	10-BIT D-TYPE FLIP-FLOP (INV)			A			
823	9-BIT D-TYPE FLIP-FLOP			A			
824	9-BIT D-TYPE FLIP-FLOP (INV)			A			
825	OCTAL D-TYPE FLIP-FLOP			A			
826	OCTAL D-TYPE FLIP-FLOP (INV)			A			
827	10-BIT BUFFERS/ LINE DRIVERS			A			
828	10-BIT BUFFERS/ LINE DRIVERS (INV)			A			
841	10-BIT D-TYPE TRANSPARENT LATCHES			A			
842	10-BIT D-TYPE TRANSPARENT LATCHES (INV)			A			
843	9-BIT D-TYPE TRANSPARENT LATCHES			A			
844	9-BIT D-TYPE TRANSPARENT LATCHES (INV)			A			
845	OCTAL D-TYPE TRANSPARENT LATCHES			A			
846	OCTAL D-TYPE TRANSPARENT LATCHES (INV)			A			
861	10-BIT BUS TRANSCEIVER			A			
862	10-BIT BUS TRANSCEIVER (INV)			A			
863	9-BIT BUS TRANSCEIVER			A			
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- ☐ Menu driven operation.
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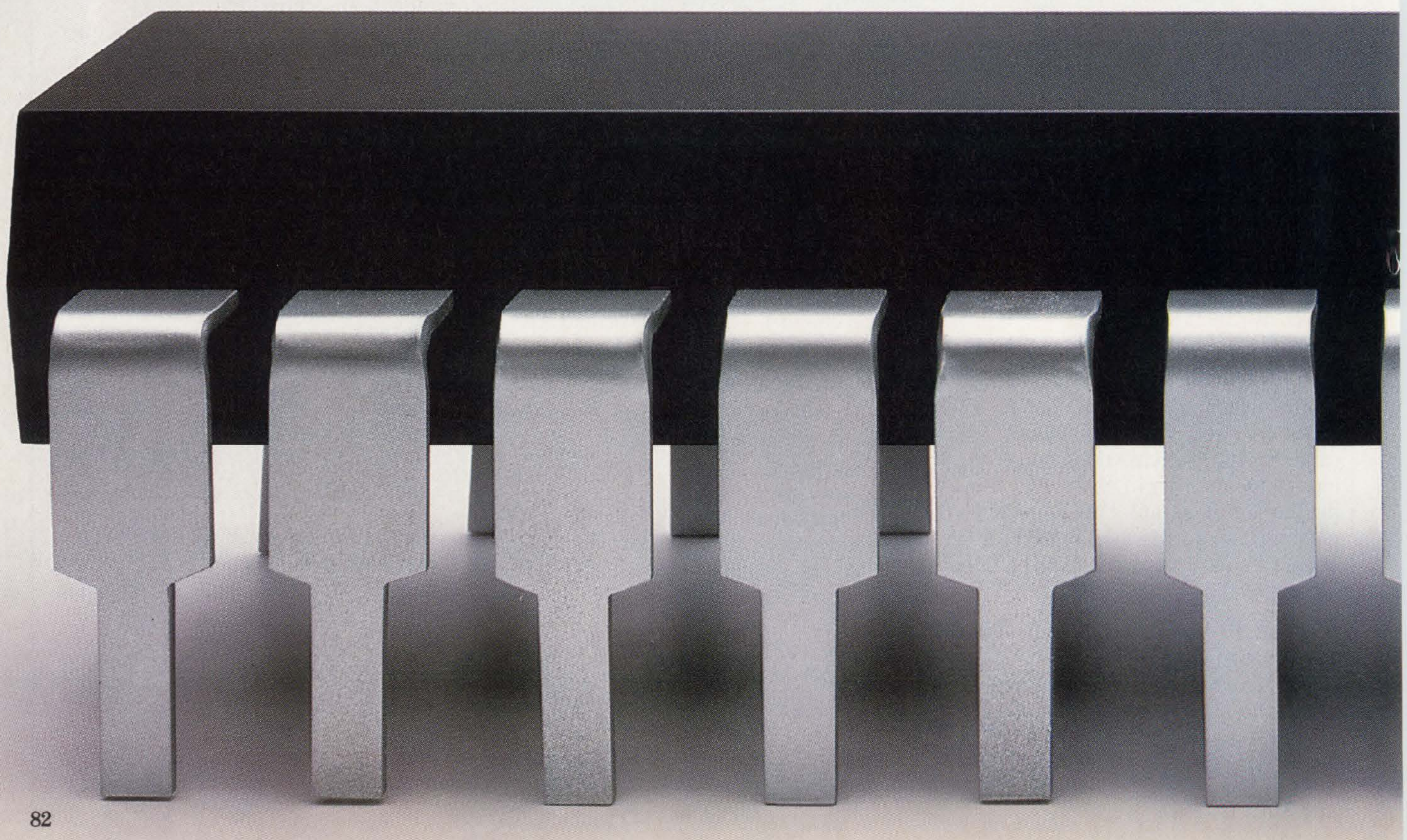

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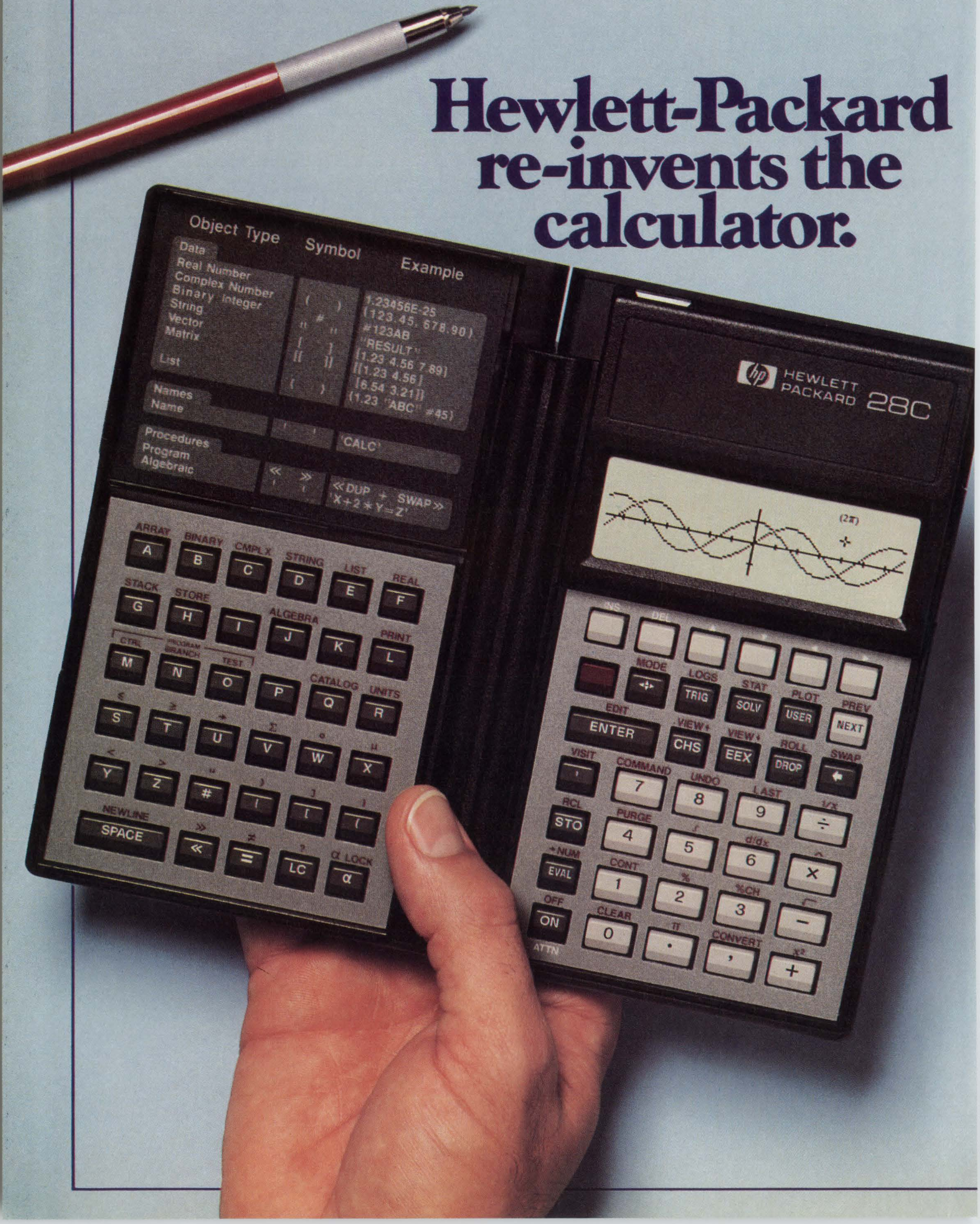

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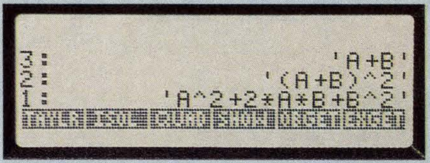

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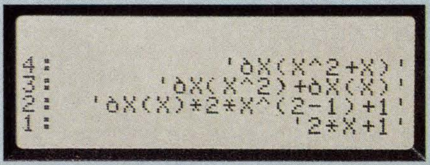

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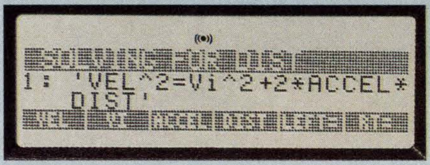

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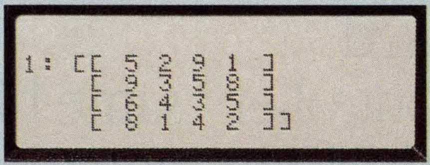

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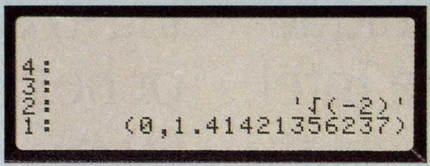

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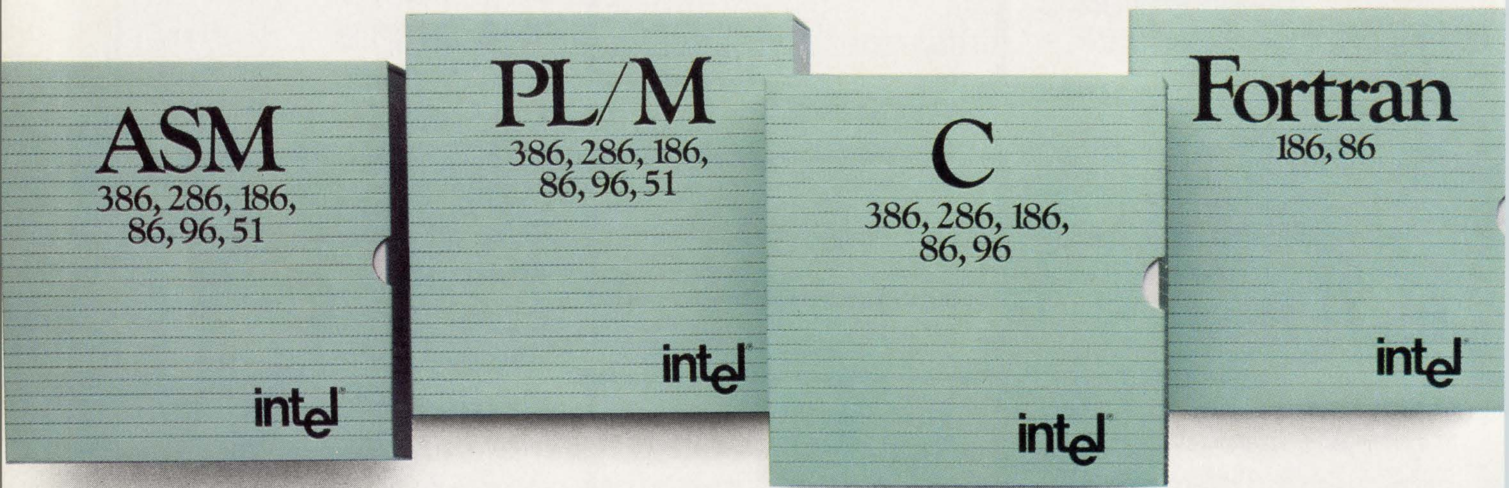

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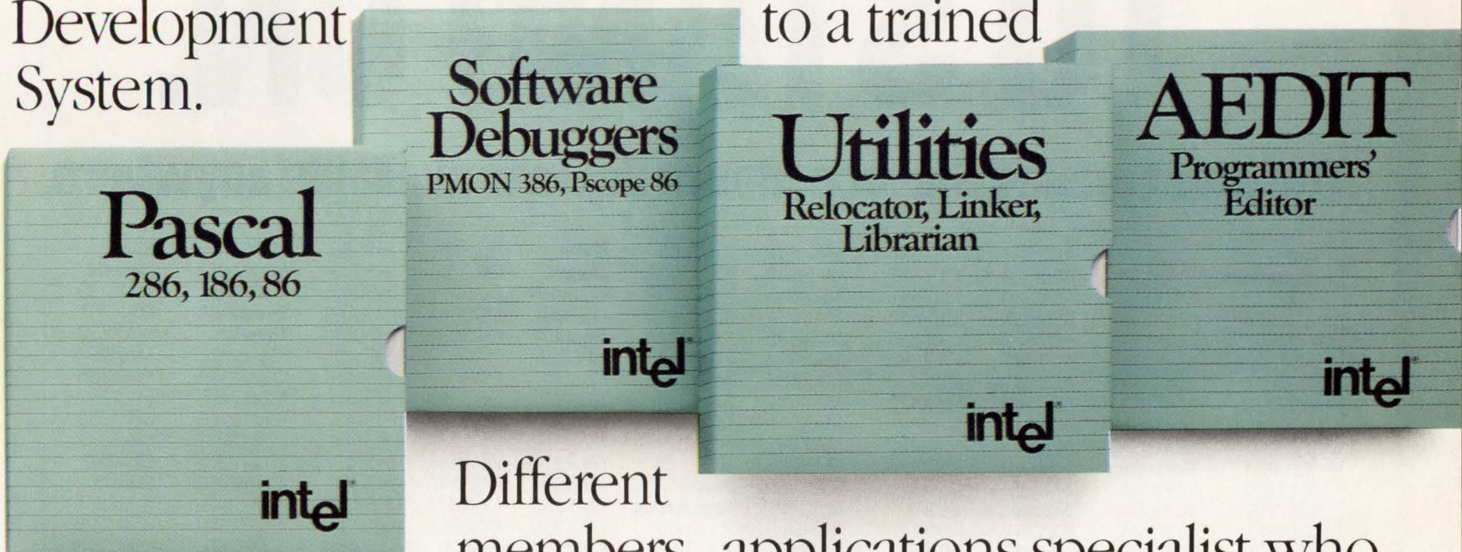

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Cross-development tools for PCs and minis let you develop software for 8-bit μPs

Chris Terry, *Associate Editor*

Using this cross-development system, *you can develop your software on an IBM PC and debug it on the target machine with the aid of an emulator. Intel's Performance Analysis Tool (PAT), shown in the foreground, monitors the execution of your program on the target and allows the PC to display histograms showing the time spent in each routine.*

When you're developing software for an 8-bit microcontroller embedded in an intelligent instrument or a process-control system, you can choose from a wide variety of cross-development tools. These tools allow you to use a PC or a minicomputer to perform all the software-development tasks for an 8-bit μP—from the initial analysis of program requirements, through module design and coding, to the debugging stages.

For most purposes, cross-development tools replace the earlier μP-specific hardware/software development packages. Because each of these earlier tools targeted only one μP or μP family, you had to buy different hardware tools for each (see **box**, "Hardware/software development systems.")

Cross-development systems, however, allow you to use your PC to develop software for almost any μP. Further, they speed up your software-design and -debugging tasks by providing Computer-Aided Software Engineering (CASE) tools.

CASE tools aid in design

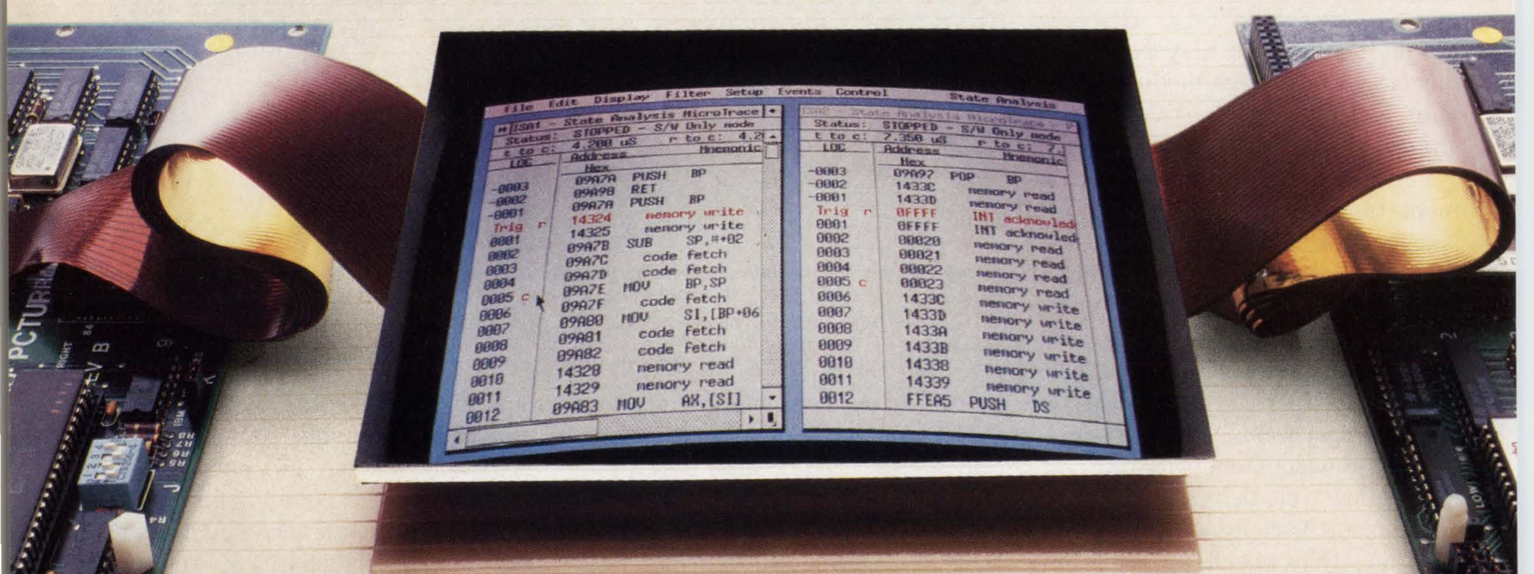
CASE tools, together with cross-compilers and cross-assemblers that generate ROMable code, are now readily available for the IBM PC/AT, the Sun and Apollo workstations, and DEC's VAX and MicroVAX minicomputers. Software development on these machines is faster and more effective than development on the target μP would be, because these computers offer graphics capabilities and computing power that 8-bit μPs don't have.

Further, CASE tools can help you to detect inconsistencies in logic and mistakes in the structure of your software even before you write a line of code. And because they allow you to develop software for an 8-bit μP on a 16-bit machine, the CASE tools also permit you to debug your software thoroughly, with the aid of a simulator, before downloading the resulting code to the target machine.

Most CASE tools—including Cadre's Teamwork (from $8900), which runs on the Apollo Domain workstation; Yourdon Engineering's $3500 Software Analyst and Promod's $9950 system, which run on the IBM PC/XT and the PC/AT; and the Tektronix SA/SD tools (from $16,500), which run on VAX/VMS machines—use the Yourdon-DeMarco technique for structured analysis. Cadre's $8900 Teamwork/RT includes recently developed extensions that facilitate the design of real-time systems. The Yourdon-DeMarco technique is currently the most widely accepted technique for structured analysis, and no other technique has so far been made available for the IBM PC family.

A Yourdon-DeMarco CASE system usually consists of several parts, including a structured-analysis program, a structured-design program, language-directed editors, and a configuration-control program. In the first stages of design, the structured-analysis program lets you define all data elements, the flow of data through the system, and the processes that modify the data. The structured-analysis tool records your definitions in several forms that provide cross-checking: data-flow diagrams, a data dictionary (which contains the definitions of all data elements), and minispecifications (which define all processes that use the data elements). In short, the structured-analysis tool defines *what* the system will do.

At last, multi-processor time-aligned trace.



Since so many embedded microcomputer designs employ more than one processor, you'd think there would be many tools to trace multi-processor dialog in both assembly-level and high-level code. And then time-align the results.

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The next stage, structured design, defines *how* the system will perform its functions. A structured-design tool allows you to define the program modules that will perform the various processes. Structure charts, based on the data dictionary and minispecs from the structured-analysis tool, show the functional responsibilities and relationships of the program modules and help you to minimize coupling between the modules.

Both of these tools perform extensive checking to ensure that the names and functions of data items and processes remain consistent from module to module. Both programs easily discover and report anomalies, such as "virgin births" (the sudden appearance of data that has no discoverable sources) and "black holes" (processes that accept and modify data but do not provide any outputs).

A CASE system may also include language-directed editors, which check the syntax of the high-level language statements you enter and provide other help in writing syntactically correct code in the language of your choice. In addition, a CASE system usually contains some form of configuration-control program, which keeps track of all changes and modifications made to the various modules of the new system. This program records the current version of each program module and places old versions in an archive; it can also recompile and relink the new system, using only the latest version of each module.

In sum, the Yourdon-DeMarco technique integrates data-flow diagrams with a data dictionary and minispecifications and provides a means by which the host computer can check for the consistency of data names and functions throughout the system under design. For a system

Hardware/software development systems

Before 1982, developing software for an embedded 8-bit μP required you to use a dedicated hardware/software development system based on the target μP. Among the typical development systems were Intel's system for its 8080/85 μPs and Motorola's Exorciser for its 6800 family.

Complete development systems of this kind could cost $10,000 to $20,000, depending on the complexity of the target μP and the development tools. The development tools usually included at least an in-circuit emulator and a PROM programmer, as well as software debugging tools. Further, nearly all the software for the target machine had to be written in assembly language, because very few of the high-level language compilers for 8-bit machines produced ROMable machine code.

Hardware/software development systems are still available, although they have been modified and improved to meet the demands of new microprocessors. The Echo system from Arium Corp, for example, comes in both a 16-bit version (for $12,980) and an 8-bit version (for $8940). For the base price you get 1M bytes of memory, one floppy-disk drive, one 20M-byte hard-disk drive, one emulator pod, one personality board, and an assembler package. Additional emulator pods cost $1295 for the 8-bit emulator and $3395 for the 16-bit emulator; additional personality boards for most popular μPs (including the 8085, Z80, 6809, 68000, and 8088 μPs) cost from $995 for the 8085 board to as much as $3695 for the 80386 board.

For each of the target machines handled by the Echo system, Arium also offers C and Pascal compilers, which produce ROMable code, at prices from $295 to $895. Other major vendors that offer modernized microcomputer-development systems and software-development tools include Hewlett-Packard, Intel, and Motorola.

You can develop software for many microcontrollers *on this 8-bit development system, the Echo from Arium. The system lets you test your software right on the target machine with the aid of an emulator and a personality board that control the execution of your programs and trap errors.*

If all your software development is for one μP or μP family, you might benefit from using one of these hardware/software development systems. However, if you're developing software for more than one microprocessor and you already have an engineering workstation or a multiuser minicomputer in place, you're probably better off buying a software cross-development system than purchasing a hardware/software microcomputer-development system.

including multiple workstations that are networked or attached as peripherals to a multiuser host computer, the data dictionary and minispecifications are available to all the programmers who are using the system, even though they may be developing different parts of the new program on different workstations.

Cross-assemblers can be versatile

When you're developing software for real-time systems, you may find that you'll need to write some of the routines in assembly language in order to maximize execution speed. Writing the code for these routines with a cross-assembler that runs on your PC or minicomputer offers you several advantages.

For example, many of the available cross-assemblers are not restricted to the instruction set of one specific μP but can interpret all the mnemonics associated with a family of chips. For instance, Avocet's Avmac85 cross-assembler can assemble code for the 8080, 8085, or Z80 μPs by using the Intel mnemonics; the AvmacZ80 handles the same chips but uses the Zilog mnemonics. You select the target machine by inserting the appropriate assembler directive at the beginning of the source code. Likewise, the Avmac68 handles all the chips in the Motorola 6800 family (as well as the compatible Hitachi 6301), and the Avmac48 handles nine single-chip microcontrollers in the Intel 8048 family. The Avmac Series includes 21 cross-assemblers that handle more than 50 4-, 8-, 16-, and 32-bit target μPs. All the cross-assemblers are available in three versions: The PC-DOS/MS-DOS versions cost $349 each; the corresponding VAX/Unix versions cost $995, and the VAX/VMS versions cost $1195.

Furthermore, most cross-assemblers allow you to use symbol names that have as many as 32 significant characters. Thus, your symbol names can explicitly describe the nature of the data or processes to which they refer. In contrast, older assemblers seldom allowed more than eight or 10 characters and constrained you to use arbitrary names that did little to help other people understand your programs.

In addition, you'll find that some of the newer cross-assemblers incorporate procedure blocks, which grew out of structured-programming practices. Procedure blocks help you to write clean, maintainable code, and they also make it easier for other programs to produce documentation by scanning and parsing the source code.

Produce ROMable code

You may wish to write your 8-bit software in a high-level language; for this purpose, you can find a wide variety of Pascal and C cross-compilers for the IBM PC, and even more of them for VAX/VMS machines. For example, Archimedes Software Inc offers C cross-compilers for the Motorola 68HC11 and 6801 microcontroller family, as well as for the Hitachi 6301 and Intel 8051 families. The PC-DOS versions cost $995 each; the MicroVAX versions, $3995 each; and the VAX (VMS or Unix) versions, $4995 each.

These cross-compilers all implement the full Kernighan and Ritchie language standard with the enhancements of the proposed ANSI standard. The cross-compilers also allow you to select small, medium, or large memory models, and they generate relocatable, PROMable code for the target machine in a single pass. The medium memory models of the 8051 version permit you to write recursive code. Archimedes Software also offers a macro cross-assembler for each family, and its linker lets you link C code to routines written in the assembly language of the target machine.

The compiler package includes C libraries, a librarian with which you can create your own relocatable library routines, and a linker. You can debug your code with the aid of host-resident utilities, such as Microsoft's CodeView, or with any software simulators and emulators.

Intermetrics offers InterTools, a line of C cross-compilers and debug-

For more information . . .

For more information on the software-development tools discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or contact the manufacturers directly.

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gers that run on IBM PC, VAX, Sun, and Apollo machines. These compilers generate assembly-language code for the target machine; they each come with a compatible assembler, a linker, a C library, and a run-time library. You can order different versions for such target μPs as the 68000, the 8086/186, the Z80, the 6809, the 68HC11, and the 6800 family. You can also obtain a cross-debugger that works with a hardware emulator to control program execution on the target machine. The debugger lets you display the source code or just the C variables. You can also display a symbolic disassembly. A logging feature lets you record all the transactions of a debugging session so that you can later reconstruct what took place. InterTools compilers that run on the IBM PC/XT or PC/AT cost $1000; the assemblers cost $800, and the debuggers sell for $1500 each.

Simulators ease debugging task

When you debug a program, your main challenge is to execute your program at full speed, yet keep strict control of it at the same time, so that any errors it contains do not make it crash. Such a crash could destroy the data that would help to identify its cause. In a hardware/software microcomputer-development system, this control is exercised by hardware-breakpoint circuitry that stops the program if it attempts to access illegal or nonexistent memory locations, or if any of a variety of other fatal conditions occur.

When you use a cross-development system, however, the host has sufficient computing power to run an exact software simulation of the target machine. One part of the simulation program acts as a virtual machine; other parts provide debugging features. The virtual machine executes your program, behaving exactly as the target machine and its on-chip peripherals would, except that the virtual machine remains under control of the simulator's debugging features at all times, so you can prevent the program from crashing.

The simulator program provides all the features of a standard symbolic debugger and lets your screen display and dynamically update the registers and flags, the stack, the currently executing code fragment, and selected data areas in memory.

In addition, the simulator provides trap features that are software equivalents of the hardware-breakpoint circuitry found on a logic analyzer. Thus, you can set sophisticated combinations of traps to stop the virtual machine if the program under test behaves in unexpected and undesired ways. By making a judicious choice of stop-on-value and stop-on-address traps, you can preserve all the data you need to identify the error. Avocet's Avsim packages ($299) are typical of this kind of tool. They currently run on IBM PCs and are available for the same chips and families that the company's Avmac cross-assemblers target.

16-bit-μP development

Just as you can use a PC or a minicomputer to develop software for 8-bit target machines, you can use a more powerful host—a VAX, for example—to develop software for 16-bit targets, such as the IBM PC family. Cross-development tools are available for development of software for μPs of all kinds. CASE tools go a step further; they're useful at any level, because you can employ them to develop any kind of program for any computer architecture. **EDN**

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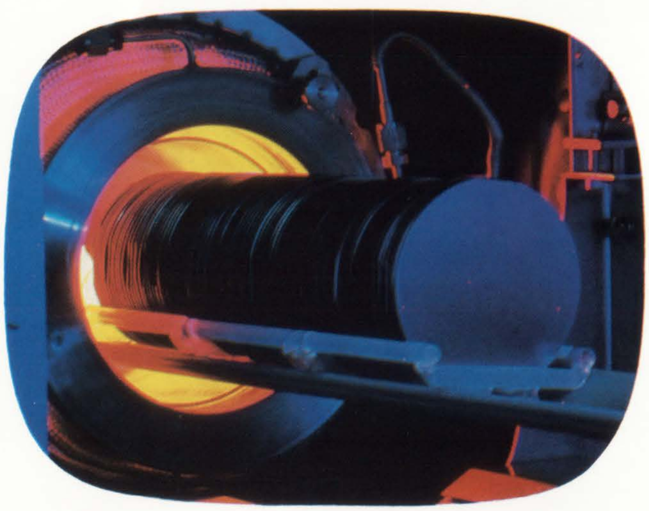

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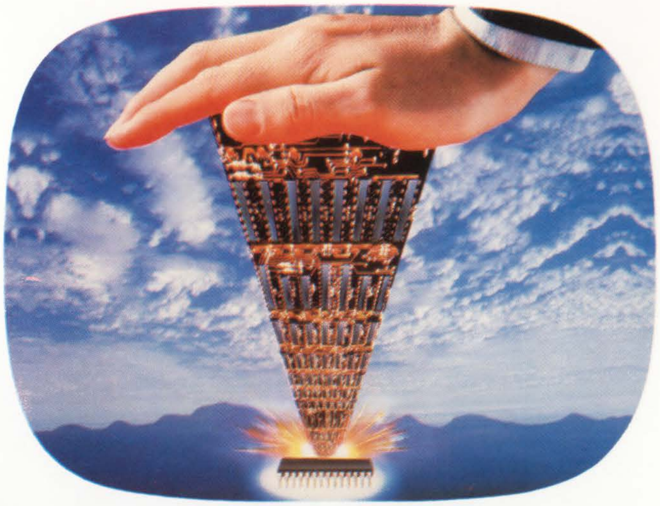

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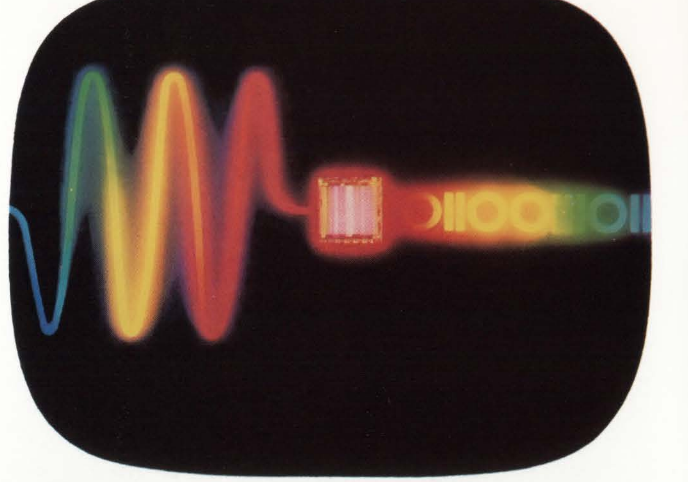

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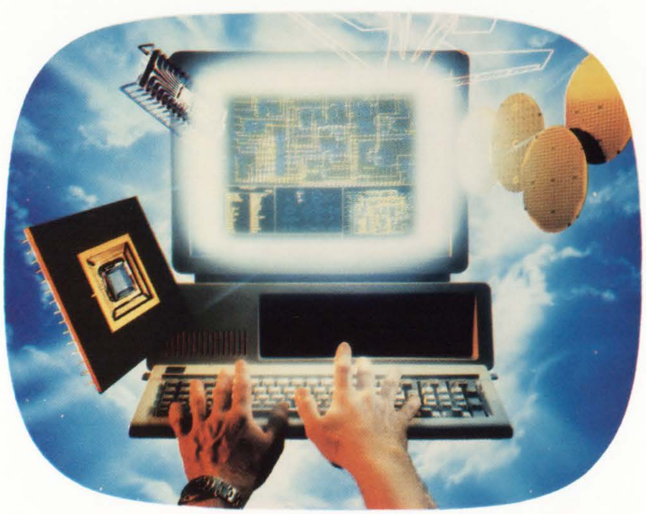

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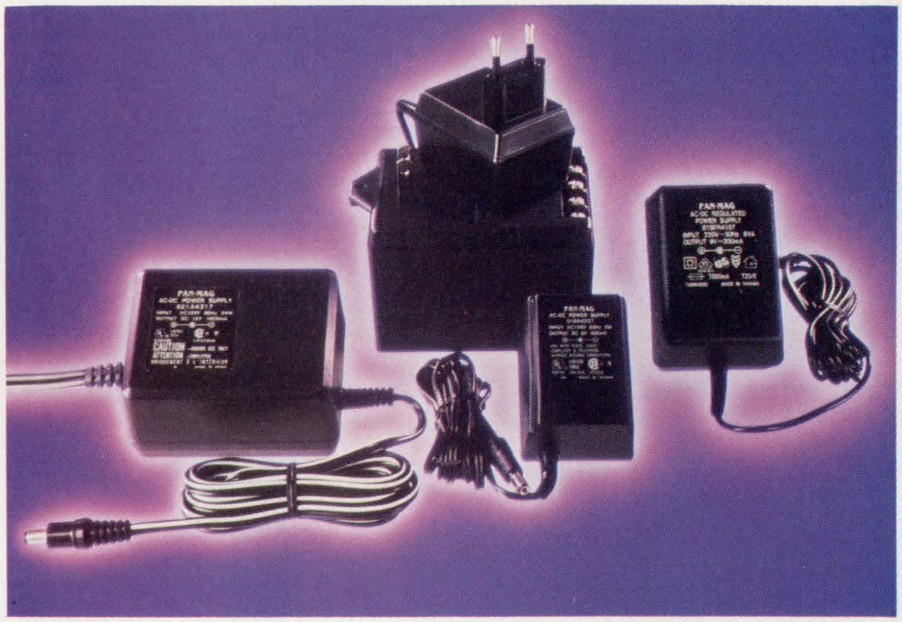
Chris Everett, *Regional Editor*



For applications requiring less than 25W, *linear wall plug-in supplies are usually preferable. These supplies from Tamura (formerly Pan-Mag) have outputs ranging from 2 to 12W.*

By using an external, or wall plug-in, supply, you can gain board space, eliminate a major source of heat in your design, and reduce EMI noise. Plus, if you're lucky, you can free yourself from the burden of getting safety regulatory approvals for your product.

Until recently, wall plug-in supplies were limited to levels below 25W, but they are now available with much higher output levels. Indeed, you'll soon be able to buy a wall plug-in unit capable of 100W. Depending mostly on the power requirements of the system you're designing, you have a choice between a linear, a switching, or a hybrid type.

Desktop versions of all three of these types are also available if your power requirements prohibit the use of wall plug-in models. The difference between a desktop and a wall unit is that a plug-in is light enough to plug into a wall socket, whereas a desktop's weight dictates that it sit on the floor or a desk.

Initially, designers used external power supplies to minimize the size and weight of an end product. In the 1970s, for instance, the electronic desktop calculator consisted of a comparatively large power transformer surrounded by electronics. Without CMOS logic and LCDs, a handheld calculator's power needs were relatively high for the package size: You needed power for desktop operation and to recharge the calculator's batteries. However, by placing the power source at the other end of the power cord, plugged into the wall, it was possible to appreciably reduce the size and weight of the calculator. You can apply the same solution to today's system design.

Moreover, if you can keep hazardous voltages out of your design, you can probably avoid the hassle of having to undergo UL approval. Underwriters Laboratories defines hazardous voltages as follows: ac voltages in excess of 30V rms, and dc voltages whose peak values exceed 42V. Despite recent changes affecting standards for wall plug-in devices (see **box,** "Publication of UL 1310 brings changes"), for the most part, whether your design will need testing depends on which regulatory agencies' product codes it falls under **(Table 1).**

An added incentive to eliminating hazardous voltages is to avoid the 6-week to 1-year period needed to complete testing and get the regulatory agencies to grant approval. (UL approvals take six to eight weeks; CSA approvals take several weeks longer. VDE approvals can take as long as one year, but you can lessen the time considerably if you go through the TUV office in New York.)

Once it comes time to decide what type of wall plug-in you want to incorporate in your design, you'll find it necessary to weigh the tradeoffs. Switching plug-in supplies offer certain blanket advantages over linear units. In general, a switching power supply runs more efficiently: 60 to 90% vs a linear supply's 30 to 55%.

A second advantage involves hold-up time, the length of time the power supply's output voltage will remain within specification following the loss of input power. A long hold-up time gives your microprocessor enough time to shut down operation without loss of data. Linear units are limited to about 2 msec of holdup time; switchers have 16 to 32 msec.

Nonetheless, linear wall plug-in supplies are the only solution for

low-power applications because of their low cost, small size, and quiet operation. For example, you can buy an unregulated-output wall plug-in supply from Tamura (formerly Pan-Mag) for $7.50. (This and all other prices quoted here are for quantities of 100.) The 6W unit has both UL and CSA approvals. An unregulated 6W supply with VDE approval is priced at $11.25.

If you need a regulated wall plug-in supply, the cost will be higher. Tamura's regulated 4.6W wall plug-in model sells for $14.50. The supply has both UL and CSA approvals. A VDE-approved 4W supply is priced at $13.90.

Obviously, Tamura isn't the only manufacturer of linear wall plug-in supplies. Arstan Products, Dynage Power, Golden Pacific Electronics, and International Components also produce low-cost off-the-shelf and custom-made linear supplies. Most of the low-cost supplies originate in the Far East, which helps to keep down costs.

Because low-powered linear wall plug-in supplies cost so little, no manufacturers of switchable wall plug-in supplies can really compete. The lowest power switching supply from Precision Components is a single-output 20W wall plug-in that costs $65 to $70. Ault's lowest powered switcher (15W) sells for $56.

As far as size is concerned, Ault's 25W linear supplies are packaged in 28-in^3 cases, whereas the company's 25W switching supplies are housed in 55-in^3 cases. For lower-power supplies, the size differential is even more dramatic. Ault's lower-power linear wall plug-in supplies are enclosed in 8-in^3 cases.

Generally, a linear power supply operates much more quietly than a switching unit. (See **Table 2** for a comparison of linear and switching supplies.) A linear can be designed with tighter line and load regulation specifications than can a switcher. Also, the linear supply tends to deliver a cleaner output as measured by the output ripple/noise specification. For example, all of Ault's regulated wall plug-in supplies, as well as Jerome Industries' comparable supplies, are specified to hold output ripple to less than 10 mV rms.

D&B Power's triple-output 7W wall plug-in supply holds line regulation to within 0.1% on all three outputs and limits ripple to less than 10 mV rms. D&B is primarily a custom house specializing in building limited quantities of supplies to

TABLE 1—REGULATORY AGENCY SAFETY AND EMI STANDARDS

AGENCY	CODE	PRODUCT COVERAGE
UL	114	ELECTRICAL OFFICE APPLIANCES AND BUSINESS MACHINES
	478	ELECTRONIC DATA-PROCESSING UNITS AND SYSTEMS
	508	ELECTRICAL INDUSTRIAL CONTROL EQUIPMENT
	544	MEDICAL EQUIPMENT
	1012	POWER SUPPLIES
	1236	BATTERY CHARGERS
	1310	WALL PLUG-IN DEVICES
	1585	TRANSFORMERS (CORD CONNECTED)
CSA	C22.2-107-1957	RECTIFYING EQUIPMENT
	C22.2-154	DATA-PROCESSING EQUIPMENT AND COMPONENTS
VDE	0804	TELECOMMUNICATIONS EQUIPMENT AND MAINFRAME DATA-PROCESSING EQUIPMENT
	0806	OFFICE EQUIPMENT (USER MAINTAINED)
IEC	380	OFFICE EQUIPMENT (SEE VDE 0806)
	435	MAINFRAME DATA-PROCESSING EQUIPMENT (SEE VDE 0804)
FCC	DOCKET 20780, PART 15 AND 18	COMPUTING DEVICES (INCLUDING ELECTRONIC GAMES, PERSONAL COMPUTERS, CALCULATORS, AND DIGITAL WATCHES)
VDE	0871	LEVEL A AND LEVEL B PRODUCTS

Publication of UL 1310 brings changes

Recently, Underwriters Laboratories combined all its standards for wall plug-in transformer devices into a single standard, UL 1310. With the publication of this standard, the organization also instituted two major changes for wall plug-in supplies.

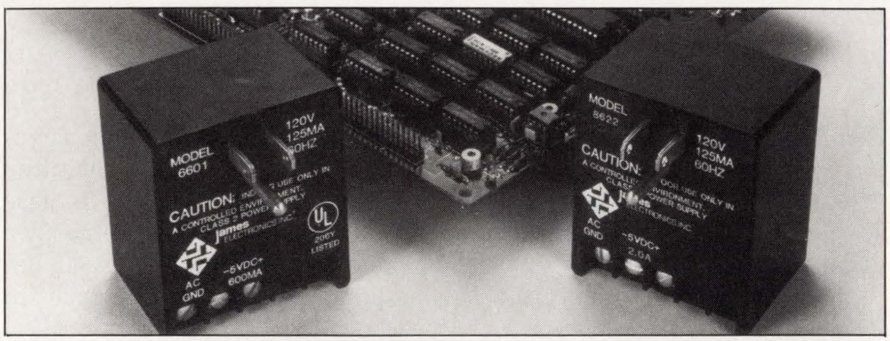
The first change affects the weight and shape of a supply that plugs into a wall socket. UL 1310 limits the weight of such a supply to 28 ounces, notwithstanding that certain limits on the power supply's center of gravity must be met. And, in some cases, mounting tabs on the supplies are now prohibited. Finally, the organization won't take into account the third blade, or grounding pin, when considering the supplies' safety and stability provisions.

The second change in UL 1310 affects the labeling of both wall plug-in and desktop power supplies. Formerly, if a potential customer saw the UL listing logo on a power supply, he could safely assume that the listing applied to both the supply and the end product. This is no longer the case. Underwriters Laboratories will only recognize wall plug-in power supplies for applications where the product and power supply are sold and shipped as a system; otherwise, the organization will only list it, and the burden of getting approval will rest with the manufacturer.

TABLE 2—COMPARISON OF LINEAR AND SWITCHING POWER SUPPLIES

CHARACTERISTICS	LINEAR	SWITCHING
OUTPUT	5 TO 150W	15 TO 1500W
REGULATOR TYPE	SERIES OR SWITCHING	SWITCHING
EFFICIENCY	30 TO 55%	60 TO 90%
OUTPUT RIPPLE/NOISE	0.5 TO 30 mV P-P	10 TO 100 mV P-P
LINE REGULATION	0.02 TO 0.1%	0.1 TO 1%
LOAD REGULATION	0.02 TO 0.5%	0.1 TO 1%
HOLD-UP TIME	2 mSEC	8 TO 32 mSEC
RECOVERY TIME	~ 50μ SEC	~ 300 μSEC
POWER DENSITY	0.2 TO 0.5W/IN^3	0.7 TO 3W/IN^3
RELIABILITY	IN GENERAL, LINEAR SUPPLIES ARE MORE RELIABLE	
WEIGHT	ABOVE 25W, LINEAR SUPPLIES WEIGH MORE	
PRICE	ABOVE 25W, LINEAR SUPPLIES COST MORE	

NOTE: THE CHARACTERISTICS DEFINE THE OPERATING RANGE FOR THE MAJORITY OF LINEAR AND SWITCHING SUPPLIES. THERE ARE MODELS FROM MANUFACTURERS IN BOTH CATEGORIES THAT CAN OPERATE BEYOND THE RANGES LISTED ABOVE.



Five-volt designs are best suited to a hybrid wall plug-in supply *such as one of these from James Electronics. A hybrid supply has a linear front-end to reduce and rectify the line voltage to an 8 to 9V range, followed by a switching regulator to translate the unregulated 8 to 9V to 5V.*

your specification with fast turnaround times. In contrast to most wall plug-ins, D&B's supplies are produced in New York. These two facts contribute to the price the company charges for its supply: $35.

Elpac Power Systems' higher-power (22W) triple-output desktop supply, which costs $39, holds line regulation to within 0.5% and ripple to less than 20 mV p-p. Whereas D&B Power can package its 7W triple-output supply in a wall plug-in case because it weighs under 28 oz, Elpac has to use a desktop case for its 22W counterpart to meet UL and CSA requirements.

Although you may want to incorporate a wall plug-in linear unit into your design, if you're using 5V logic a linear supply probably won't be suitable. Linears don't work well below six or seven volts. The hybrid supply does.

In a hybrid supply, the linear front-end reduces and rectifies the line voltage down to an unregulated 8 to 9V level. Instead of following the voltage reduction and rectification with a series regulator, a switching regulator reduces the 8 to 9V signal to a regulated 5V output. James Electronics and Ault are two manufacturers currently selling

For more information . . .

For more information on the external power supplies discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or contact the following manufacturers directly.

Arstan Products International
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Ault Inc
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TLX 753243
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(714) 993-6970
TLX 3720016
Circle No 695

International Components Corp
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Colorado Springs, CO 80915
(303) 570-6900
TLX 452427
Circle No 696

James Electronics Inc
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Chicago, IL 60618
312-473-6500
TWX 910-221-5034
Circle No 697

Jerome Industries Corp
730 Division St
Elizabeth, NJ 07201
(201) 353-5700
TLX 132001
Circle No 698

Precision Components Inc
1110 W National Ave
Addison, IL 60101
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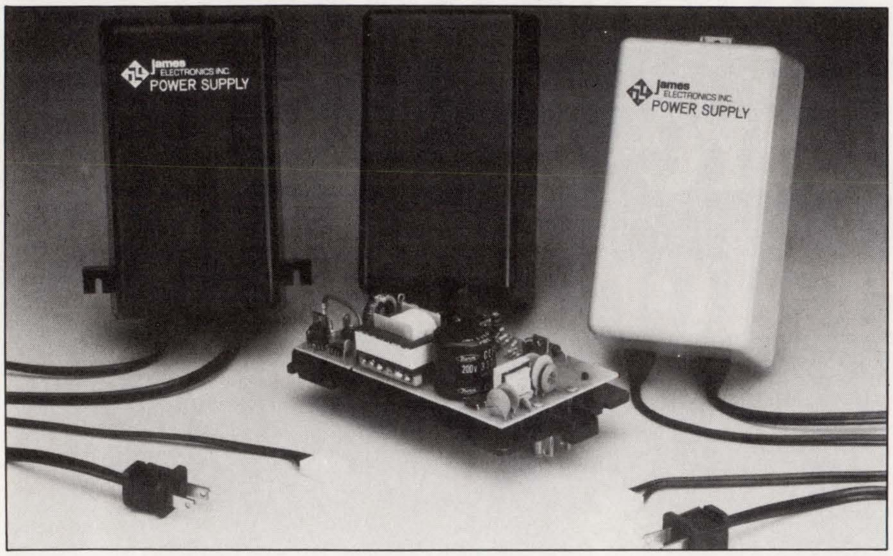

Switching wall plug-in supplies can deliver *as much as 60W. James Electronics, the manufacturer of these switchers, has a wall plug-in supply providing 100W in the tooling stage.*

such supplies; Jerome Industries is developing a line of hybrids.

For instance, Ault offers a 16W triple-output hybrid supply for European input voltages ($77.70). The 200/260V supply is designed to meet VDE and IEC 380 specifications. The 5V primary output provides 2A; the ±12V outputs are rated at 0.25A. All three outputs are fully regulated with less than 50-mV p-p ripple. The supply also has built-in protection against overcurrent and shorts. Packaged in a 16.5×9.9×5.7-cm case, it weighs 0.9 kg.

James Electronics' 5V hybrid wall plug-in power supply ($30) provides 2A. Regulation is within ±2% and output ripple is no more than 10 mV rms max. The unit is enclosed in a 2½×3×1⅞-in. case.

Once your design's power needs go above 25W, a number of factors may prove persuasive and sway you over to a switching wall plug-in supply. At the 25W output level, a linear's transformer is larger than a switcher's transformer and, due to the added heat caused by the linear supply's inefficient operation, a larger case is necessary. Secondly, at this point a linear plug-in doesn't maintain its appreciable price advantage over the switching supply.

Ault's 50W triple-output wall plug-in switcher (less than $90) weighs 22 oz and is designed to meet UL, CSA, FCC, VDE, and IEC requirements. The 5V output drives 5A, the 12V output drives 2A, and the −12V output drives 0.3A. The power supply automatically shuts off if its outputs go over a preset range, and it also has built-in overvoltage and short-circuit protection.

Precision Components' equivalent triple-output supply provides 5V at 6A and 12V and −12V outputs at 0.75A and costs approximately $80. In addition to overvoltage and overcurrent protection, the supply has transient-voltage protection. The unit also provides soft-start and remote sensing. A 9-pin D-subminiature female connector includes power, ground, and remote sensing lines.

James Electronics' 5V single-output supply ($57) is rated at 50W and has overload fold-back protection. You can add a low voltage alarm-signal and shut-down module.

As mentioned earlier, one potential disadvantage of a switching supply is the noise it generates. In the US, FCC Docket 20780 is the specification that defines the acceptable amount of noise that a switching power supply can radiate and conduct. A supply must use some type of filtering to keep the noise to an acceptable level; different manufacturers with different types of supplies intended for different applications employ filtering to varying degrees.

To meet the requirements of Part 15 of the docket, for instance, James

TABLE 3—DESKTOP SWITCHING POWER SUPPLIES

MANUFACTURER	OUTPUTS	OUTPUT VOLTAGES	OUTPUT POWER	LOAD REGULATION	MAXIMUM RIPPLE	MINIMUM LOAD	PROTECTION
AULT	SINGLE	5, 6, 12, 48	24 TO 60W	±0.5 TO ±2%	50 mV P-P	NONE	OVERCURRENT AND SHORT-CIRCUIT PROTECTED OUTPUTS. 5V OVERVOLTAGE CROWBAR AND AUTORESET FROM OVER-CURRENTS ON ALL BUT ONE 5 ±12V SUPPLY.
	MULTIPLE	±12, 5 +12, 5 ±12 5 ±15	16 TO 49W	TO ±2%	50 mV P-P	VARIES	
JAMES ELECTRONICS	SINGLE	5, 24, 48	16 TO 60W	2%	75 mV P-P	NONE	OVERLOAD FOLD-BACK PROTECTION
	MULTIPLE	±12, 5 ±12	27 TO 36W	5%	75 mV P-P	NONE	
PRECISION COMPONENTS	SINGLE	5, 12, 15, 24, 48	20 TO 48W	5%	200 mV P-P	20%	OVERCURRENT AND OVER-VOLTAGE PROTECTION, TRAN-SIENT VOLTAGE PROTECTION, SOFT-START, REMOTE SENS ING (9-PIN D-SUBMINIATURE OUTPUT CONNECTOR)
	MULTIPLE	±5; 5 +12; 5 +24, ±12, ±15; 5 ±12; 5 ±15; 12 ±5	21 TO 48W	5%	200 mV P-P	20%	

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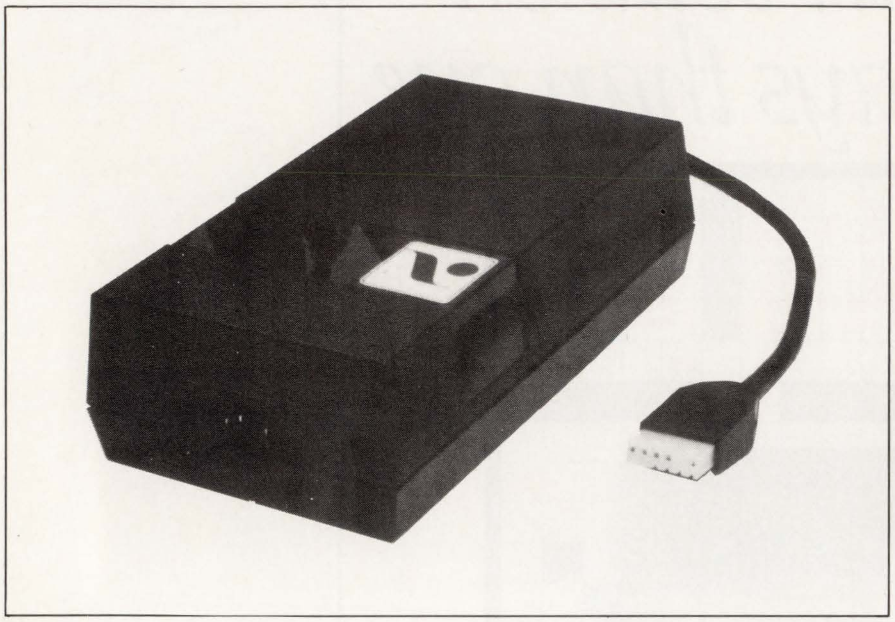

Once you plug your power cord into the IEC connector socket *that's in front of this desktop switching power supply, the supply is ready to provide as much as 50W. This unit from Ault incorporates overvoltage and short-circuit protection.*

Electronics manufactures supplies with both filtered inputs and outputs. Ault's 25W wall plug-in switching supply ($96.88) also uses filtering to eliminate noise; this supply meets FCC emission requirements for both class A (commercial) and class B (consumer) products and is designed to meet UL 1310 requirements.

You can use the Ault supply as either a single- or a triple-output unit. In the single-output mode, it provides 5.2V at 5A; in the triple-output mode, it provides 5.1V at 3A with either ±12V or ±15V auxiliary outputs. If your design doesn't require the full 3A of the 5V output, but does require more than the ½A provided by the ±12V outputs, the supply can adjust its outputs to provide more ±12V current and less 5V current. (Incidentally, a 48V version that provides 0.5A for telephone use is also available.) The supply is packaged in a 6½×3¾×2¼-in. case and weighs 19 oz.

Although most wall plug-in switching power supplies being manufacturerd today provide less than 50W, Ault does have one model that provides 60W for less than $90 (48V at 1.25A). The company is also tooling a case to hold a 100W supply that'll meet the regulatory agencies' requirements (including UL 1310).

Demand may peak at 70W

However, according to John Kennedy of James Electronics' marketing department, the maximum demand for external supplies may peak in the 50 to 70W range. (See **Table 3** for a summary of external, desktop switching-supply specs.) At this point, he thinks it may be better to include the supply within the system and apply for UL approval. If a design needs 50 to 70W output levels, then the desire to keep the supply separate from the system is no longer the overriding concern. "As an example, the IBM PC Junior has an external power supply, the IBM PC does not." **EDN**

Reference

1. *External Power Conversion Handbook*, Ault Inc, Minneapolis, MI, 1986.

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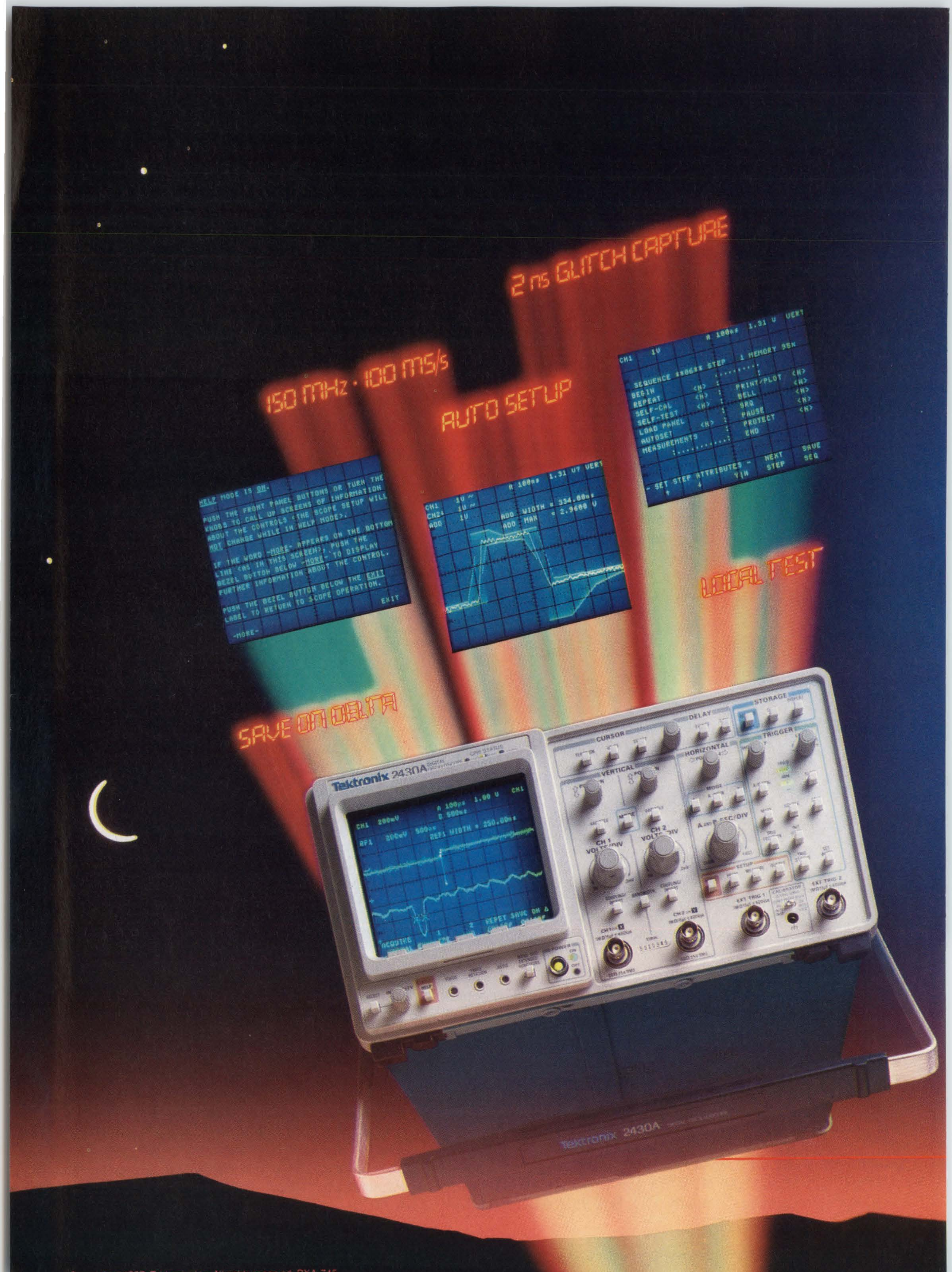
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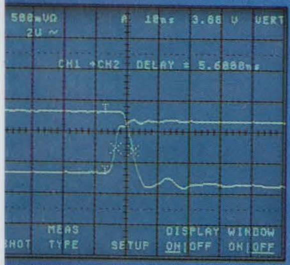

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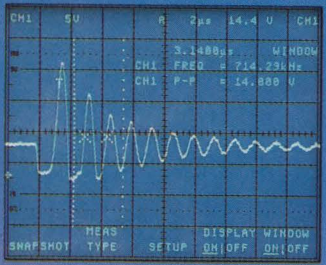

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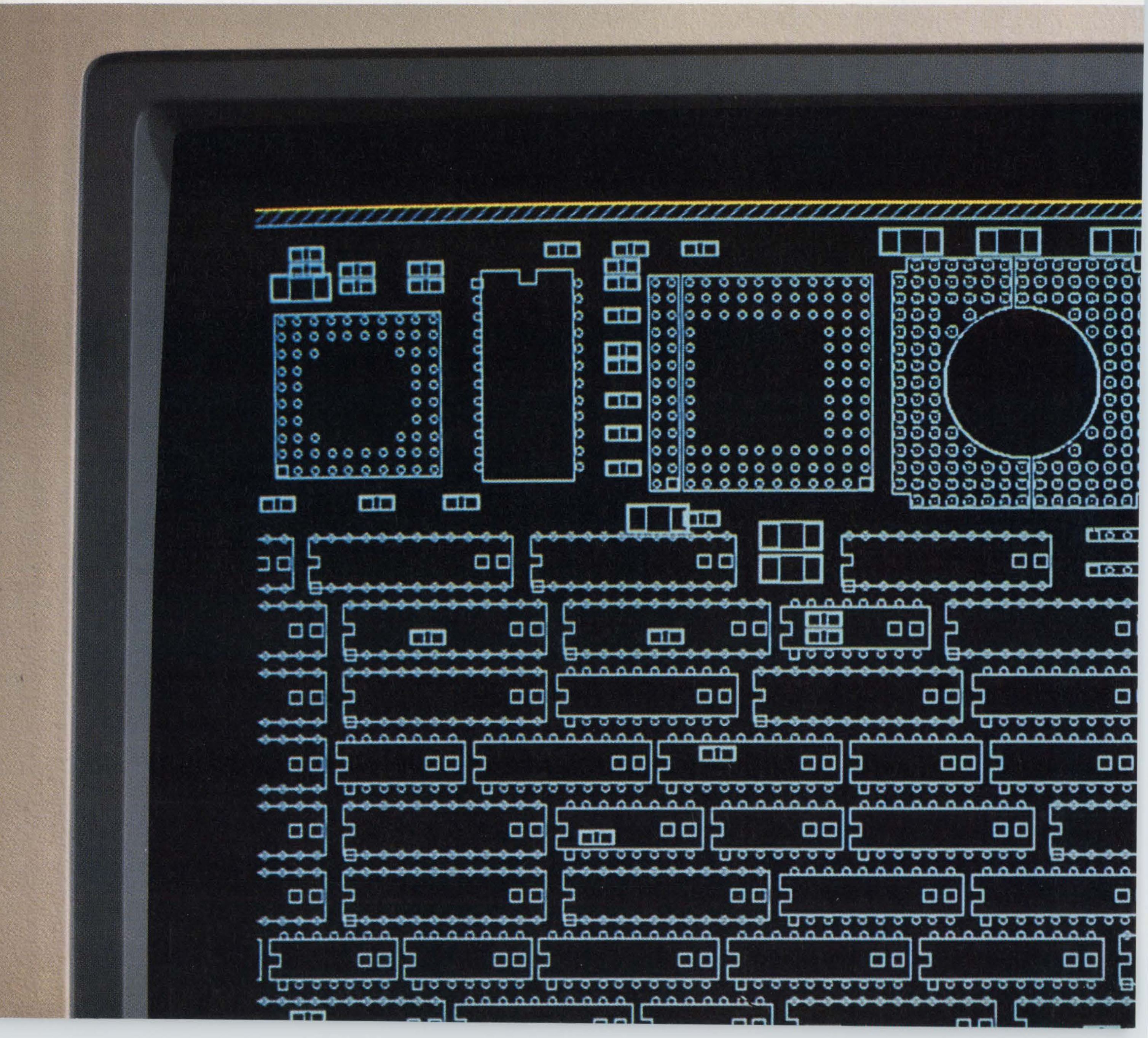

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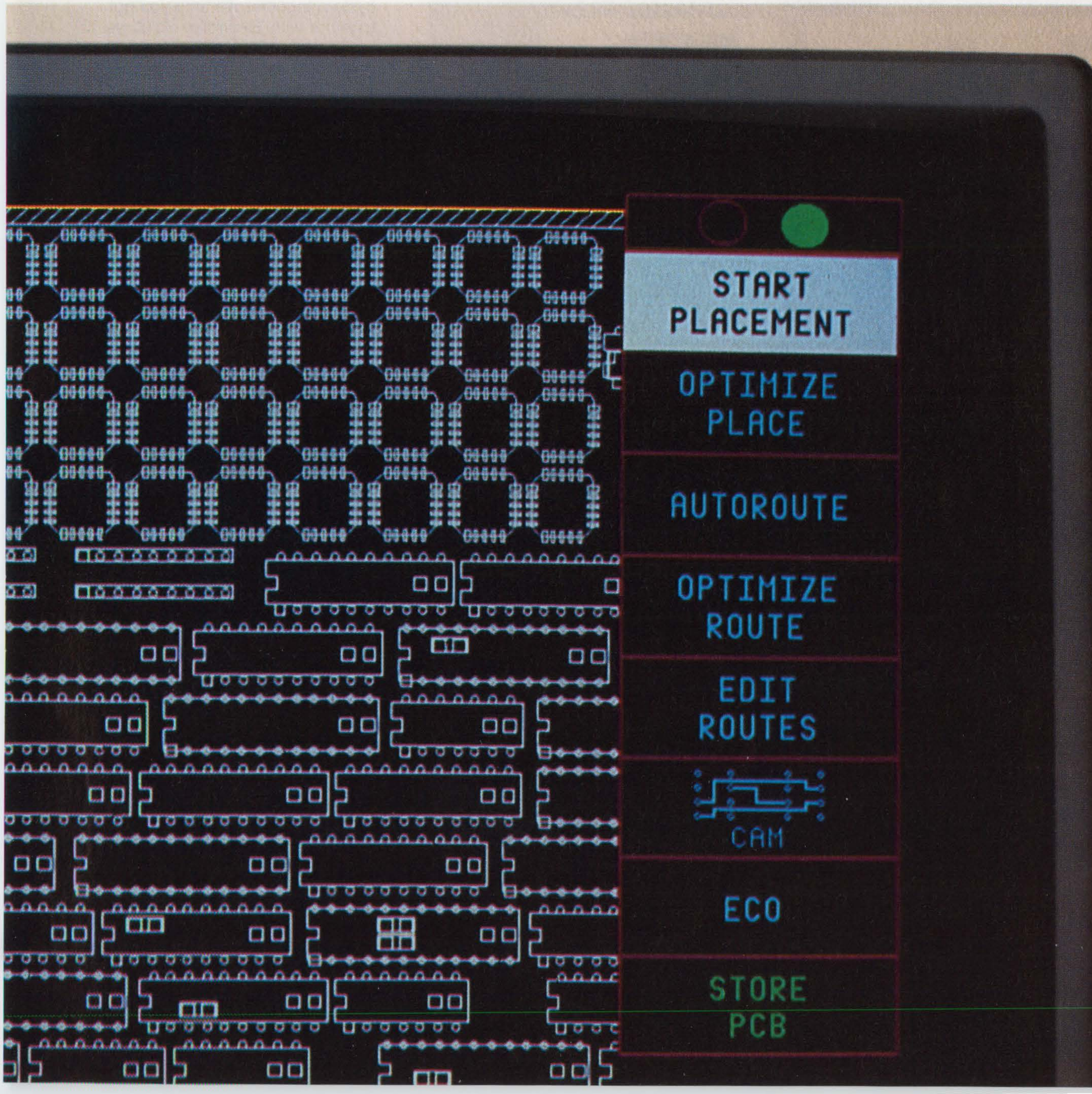

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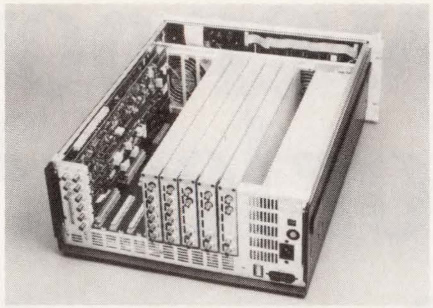


Capable of holding as many as eight modular instruments, *the 680 mainframe lets you program simple test procedures from its menu-driven front panel.*

(Fig 1). P1 (which is defined by the VME Bus standard, IEEE-1014) includes the lower 24 address bits and 16 data bits. P2 provides for the eight upper address bits and 16 upper data bits, as well as a system sync bus and a system trigger bus, both of which are accurate to 1 nsec. P2 also provides a 10-MHz and a 100-MHz system clock, both accurate to ±1 ppm; a 4-bit module ID bus; an 8-bit ECL bus; and a 20-bit TTL bus.

To obtain a timing resolution of better than 10 nsec, you can use the ECL bus for time-slicing. (Time slicing lets the bus carry both the 100-MHz clock signal and its inversion, giving you twice as many triggering edges.) You can avoid bottlenecks on

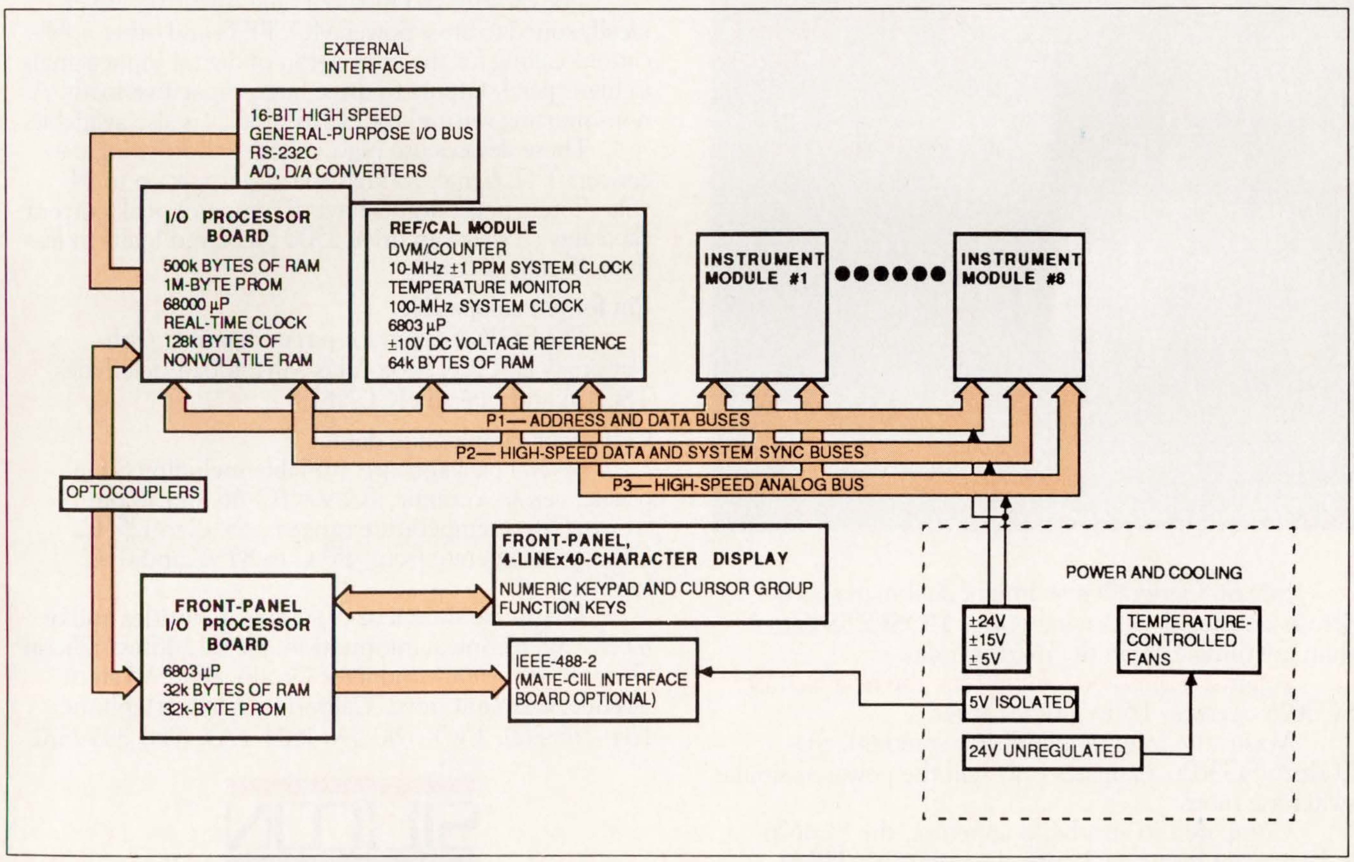


Fig 1—The high-speed modular intrumentation bus (HMIB) *is based on the VME Bus. The HMIB's connector P1 has the same pinout as the VME Bus's connector P1. The HMIB's connector P2, however, differs from that of the VME Bus in that it adds an ECL and a high-speed TTL digital data bus, as well as system trigger and sync buses. The HMIB has an additional connector, P3, which is dedicated to analog signals.*

the VME data bus by using the high-speed TTL data bus for intermodule data transfers.

The third connector, P3, supports the high-speed analog bus. The analog bus comprises the analog summing (Anasum) bus and the precision ±10V dc reference from the Ref/Cal module. The Anasum bus allows you to sum the outputs of the IACs. Because each IAC can either send or receive a signal on the Anasum bus, you can create complex waveforms with pulse-generation and arbitrary-pattern-generation IACs. The top, bottom, and fourth layers of the backplane are ground planes, and 40 of the 96 pins on P3 are either ground or power lines; these lines ensure signal separation between the analog and digital buses.

For simple test setups, you can control the system via the menu-driven front panel. For more complex test procedures, you'll need an external controller such as an IBM PC/AT or a compatible computer. The 680 comes with the IEEE-488-2 interface. For applications requiring the Air Force's Modular Automatic Test Equipment (MATE) hardware interface and the Control Intermediate Interface Language (CIIL) software interface, you can purchase the optional MATE-CIIL interface board ($1000).

The manufacturer currently offers three IACs for the HMIB: the 680-001 20-MHz arbitrary-waveform generator/synthesizer ($3000), the 680-002 pulse/timing generator ($3200), and the 680-004 high-speed pulse/timing generator ($3950). In addition, Datron (Stuart, FL) offers the 680-005, a 5½-digit, 0.02% digital voltmeter ($2950), and Racal Dana (Irvine, CA) has announced the 680-006 frequency/time-interval counter ($2800). The 680 mainframe costs $6700.

—*Margery S Conner*

Wavetek, 9045 Balboa Ave, San Diego, CA, 92123. Phone (619) 279-2200. TWX 910-335-2007.

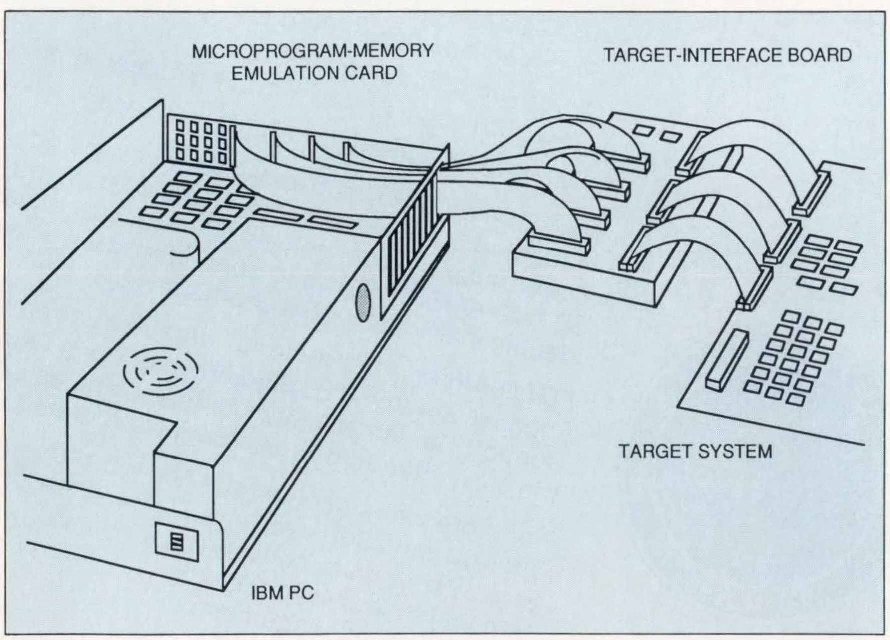
Circle No 727

Low-cost microprogramming board set adapts IBM PC for microcode development

Instead of burning scores of PROMs or resorting to microprogram development systems costing $20,000 or more (see the Special Report on microprogrammable processors, pg 142), you can use the $3995 AG-11B microprogram development tool to emulate PROM or ROM microprogram storage by loading your program into its microprogram-emulation RAM. The product includes a memory card that occupies one slot in an IBM PC or compatible computer, an external target-interface board, four shielded ribbon cables for linking the two boards, and associated software. At this budget price, you do not get symbolic-debugging features, nor can you emulate RAM-based writable control stores.

Providing a low-cost means of developing microprograms, *this microprogram-memory emulation card and target-interface board, which come with software, comprise the AG-11B microprogram development tool. The product lets you quickly load and test microcode in your target system; it also provides a hardware breakpoint signal for test purposes.*

The memory card contains 4k words of 96-bit static RAM. You can expand both the microword width and the memory depth of the microprogram memory by adding as many as three more memory cards, thus achieving a maximum memory size of 192 bits×8k words. The product employs 35-nsec RAM to attain a 50-nsec access-time rating at the target-system side of the target-interface board. All target-data outputs sink 64 mA, source 15 mA, and are terminated with 100Ω resistors on the target-interface board.



The target-interface board *supplied with the AG-11B links the product's microprogram-memory emulation card with your target system by using four shielded, 50-conductor ribbon cables between the memory card and the target-interface board and three user-supplied, 50-conductor cables between the target-interface board and the target system.*

Software supplied with the product accepts microcode produced by meta-assemblers in Amdasm, Step-hexadecimal, or Microtec-hexadecimal object formats; the software loads the microprogram RAM with your microcode. The breakpoint hardware asserts an output signal on the target-interface board when a user-programmable breakpoint address is presented to the memory card's address inputs. You can use this breakpoint output to halt your system or to trigger a logic analyzer. The software also allows you to manipulate four additional, general-purpose output lines, and it displays the state of one general-purpose input.—***Steven H Leibson***

Agility, 1290 Lawrence Station Rd, Sunnyvale, CA 94089. Phone (408) 744-0806.

Circle No 729

PRODUCT UPDATE

Half-height, 5¼-in. drive stores 53M bytes, consumes 12W

A servocontrolled, rotary voice-coil actuator *gives this 53.3M-byte, half-height, 5¼-in. Winchester disk drive its high capacity and speedy (25-msec) average access time.*

The Model 3053 Winchester disk drive achieves a 53.3M-byte (unformatted) storage capacity without resorting to using a high data-rate interface such as ESDI or SCSI. Instead, the half-height, 5¼-in. drive employs the ST412 drive interface and features a servocontrolled rotary voice-coil actuator that delivers a 25-msec average access time and a 1000-tpi density.

This product is the manufacturer's first to contain a rotary voice-coil actuator and in-spindle motor; moreover, the drive is the company's first product designed specifically for robotic assembly. These features, along with the use of low-cost, high-coercivity oxide media, allow the vendor to put the 53.3M-byte drive into a half-height package and sell it for less than the cost of a full-height, stepper-based drive that has similar storage capacity. As an extra bonus, the in-spindle motor allowed the company to eliminate the static-dissipating spindle spring, a component that tends to become audibly noisy over the operating life of many hard-disk products.

Further, although the product uses a dedicated servo platter for voice-coil-actuator positioning, the manufacturer does not use a servo writer to create the servo platter. Instead, the drive's read/write heads record the servo tracks during assembly, which further contributes to a low manufacturing cost and improves matching between the servo track and servo head.

The vast majority of installed and designed-in systems using 5¼-in. Winchesters already use the ST412 interface through embedded, bus-based, or bridge controllers. These systems are already compatible with the 3053's ST412 interface, making a system upgrade a plug-and-go affair, as long as your software can handle the greater capacity. (If you use MS-DOS, you'll need to buy an accessory program that allows the operating system to accommodate drives with capacities exceeding 32M bytes.)

The drive features low power requirements, typically consuming 0.8A from the 5V supply and 0.7A from the 12V supply, which results in an average power-consumption rating of 12W. Its maximum starting current is rated at 2A. The read/write heads park automatically on a dedicated shipping and landing zone when power is removed. The drive costs $650 (250).

—Steven H Leibson

Miniscribe, 1861 Lefthand Circle, Longmont, CO 80501. Phone (303) 651-6000. TLX 216174.

Circle No 725

Introducing OptiLab™:

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Line-by-Line Assembler	
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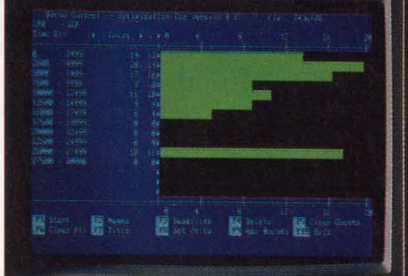
Stimulus Generator	TEST
EPROM Programmer	OPTIMIZE
	SHIP

Everything from assembly to final optimization of your software can be done with the OptiLab toolbox.

OptiLab presents a graphical display of actual program performance.



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In California: (415) 361-8883

Orion Instruments, Inc., 702 Marshall Street, Redwood City, California 94063, U.S.A. Telex: 530942

CIRCLE NO 193

Cassette-tape drive stores 5.2G bytes on a VHS tape

The VLDS (very large data store) cassette-tape drive gobbles data at a sustained rate of 4M bytes/sec for as long as 22 minutes without your having to change tapes. It stores 5.2G bytes on one premium-grade (camera quality), T-120 VHS cassette. The rack-mountable drive fits in a 44-lb box measuring 7×17×20 in. Its helical-scan recording method provides an effective head-to-tape speed of 454 ips and allows a recording density of 50M bits/in^2. Proprietary equalization and modulation techniques, data interleaving, and Reed-Solomon error-correcting codes enable this peripheral device to achieve a bit-error rate of one error in 10^{12} bits. Because the product uses standard VHS tape cassettes, data storage costs approximately $0.0021 per megabyte.

Storing 5.2G bytes on a VHS tape cassette, *the VLDS sustains a data-input rate of 4M bytes/sec and features a bit-error rate of 1 error in 10^{12} bits.*

Information enters the tape drive through dual, 8-bit, 2M-byte/sec data channels, allowing for the 4M-byte/sec maximum speed rating. The peripheral stores this data on the tape in principal blocks of 32k bytes per channel. Each principal block is numbered, so the device can search for individual blocks. An end-to-end search of a T-120 VHS cassette requires 90 sec.

The tape drive will not erase or overwrite recorded information. In addition, the company claims, because the tape used in the VHS cassettes has high coercivity (650 Oe), this product does not experience the self-erasure and print-through problems associated with conventional digital tapes.

The only ways to eradicate data recorded on a cassette with this storage peripheral are to erase the tape with a bulk eraser or a VCR. These factors, combined with the wide availability (you can buy the tape at your local video shop) and high quality of the VHS cassette tapes, make the cassettes an attractive data-storage and -archiving medium.

You can purchase the peripheral with a SCSI port or with a proprietary TTL interface having the dual data-channel inputs. The SCSI interface can support synchronous data transfers to 4M bytes/sec or asynchronous data transfers at somewhat reduced rates. The company will accept orders now for product deliveries in July. Evaluation units cost $44,000; in production quantities, the product costs $18,900 (150). The company plans to offer a VME Bus controller board for the tape drive in November.

—Steven H Leibson

Honeywell Inc, Test Instruments Div, 5105 E 41st Ave, Denver, CO 80216. Phone (303) 773-4581.

Circle No 726

Electroluminescent display is readable in sunlight

The MDS-23 electroluminescent (EL) display achieves an unfiltered pixel intensity of 225 fL at a drive voltage of 170V and a refresh rate of 300 Hz. Previous EL displays offered an unfiltered pixel intensity of 130 fL. The MDS-23's greater intensity makes the display readable in sunlight, so it's suitable for use in environments such as airplane cockpits and brightly lit factory floors.

The MDS-23's drive voltage (V_d) of 170V is about 15% lower than that of previous EL displays, which had a V_d of 200V. Because it has a lower V_d, the MDS-23's display-driver circuitry is more reliable than that of the previous displays. The MDS-23's lower threshold voltage also permits a lower power-consumption spec: The device consumes 0.3W/in^2 typ; earlier EL devices consumed 0.5W/in^2 typ (see EDN, September 4, 1986, pg 86).

In room lighting, the MDS-23 has a contrast ratio of 20:1. The contrast ratio is the ratio of the brightness of a display's characters to its background. Because the aluminized background of an EL display is a highly reflective surface, the contrast ratio decreases as the ambient light increases. In ambient lighting of 10,000 fL (the maximum ambient brightness the military specifies for high-altitude shaft lighting), you can achieve a contrast ratio of 3:1 by using the display with a polarized filter.

The decrease in contrast brightness is a disadvantage of EL displays in comparison with liquid-crystal displays (LCDs). Because an LCD creates characters by darkening dots on the screen, the LCD's contrast ratio increases as the ambient light increases. However, this advantage is offset by the LCD's

Capable of displaying graphics with its 96×160-dot matrix, *the MDS-23 electroluminescent display measures 2×3 in. and features a resolution of 50 lpi.*

restricted viewing angle (25°) and its slower response time (300 msec). The MDS-23 offers a 160° viewing angle and a response time of 10 μsec.

The MDS-23 measures 2×3 in. and supports a 96×160-dot matrix. You can also specify custom versions of the display. The manufacturer requires a one-time tooling charge of about $15,000; delivery of a sample takes eight weeks. Unit prices vary according to the quantity ordered.

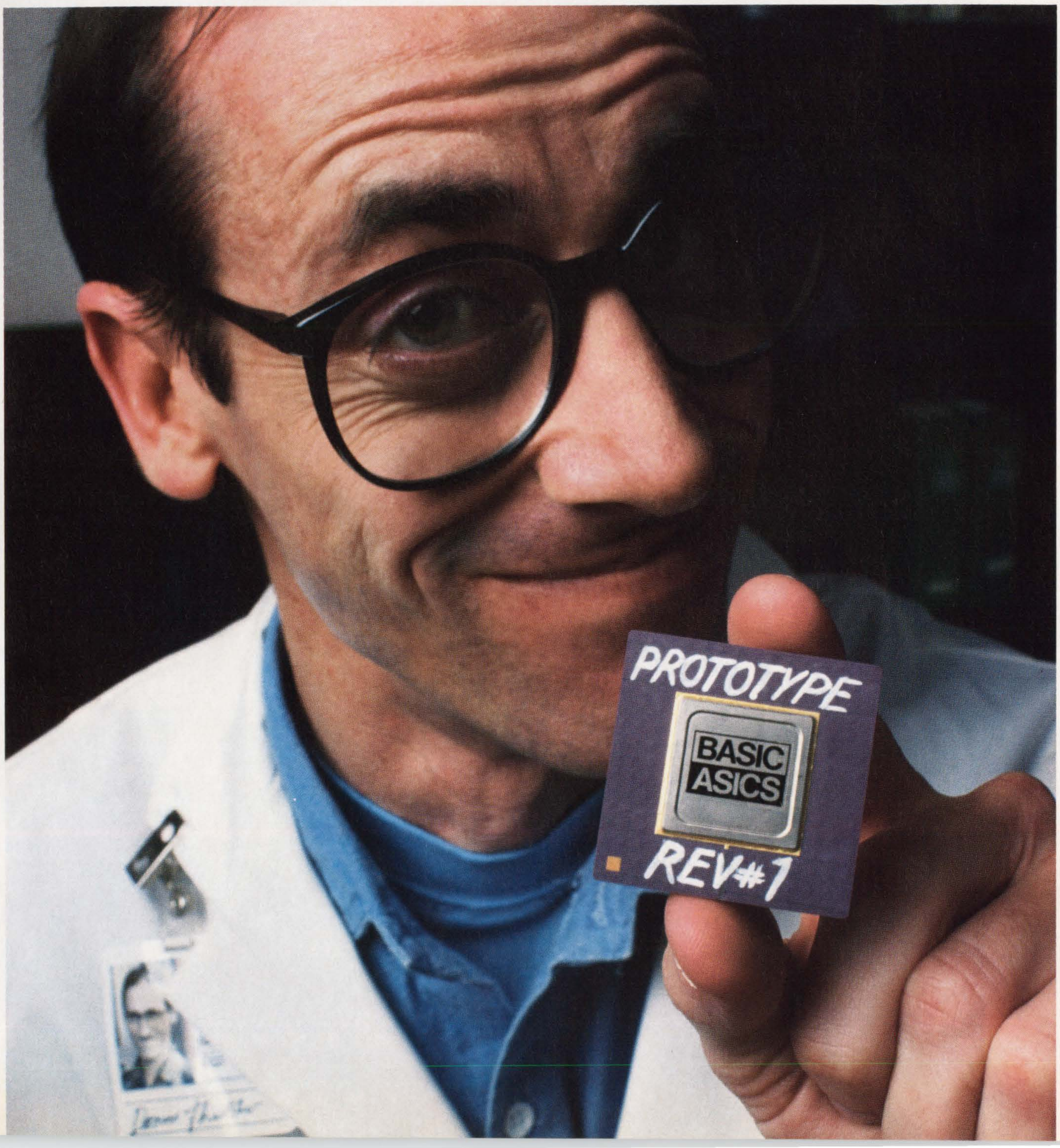
Standard versions of the MDS-23 are available off the shelf; they cost $475 with drive electronics and $375 (26) without drive electronics. The manufacturer also offers an engineering evaluation kit containing the MDS-23 display with drive electronics, a controller card with serial and parallel interfaces, and a power supply for $2585.

—Margery S Conner

Sigmatron Nova Inc, 1901 Oak Terrace Lane, Thousand Oaks, CA, 91320. Phone (805) 498-4504.

Circle No 728

JUST BECAUSE YOU'VE MADE IT...



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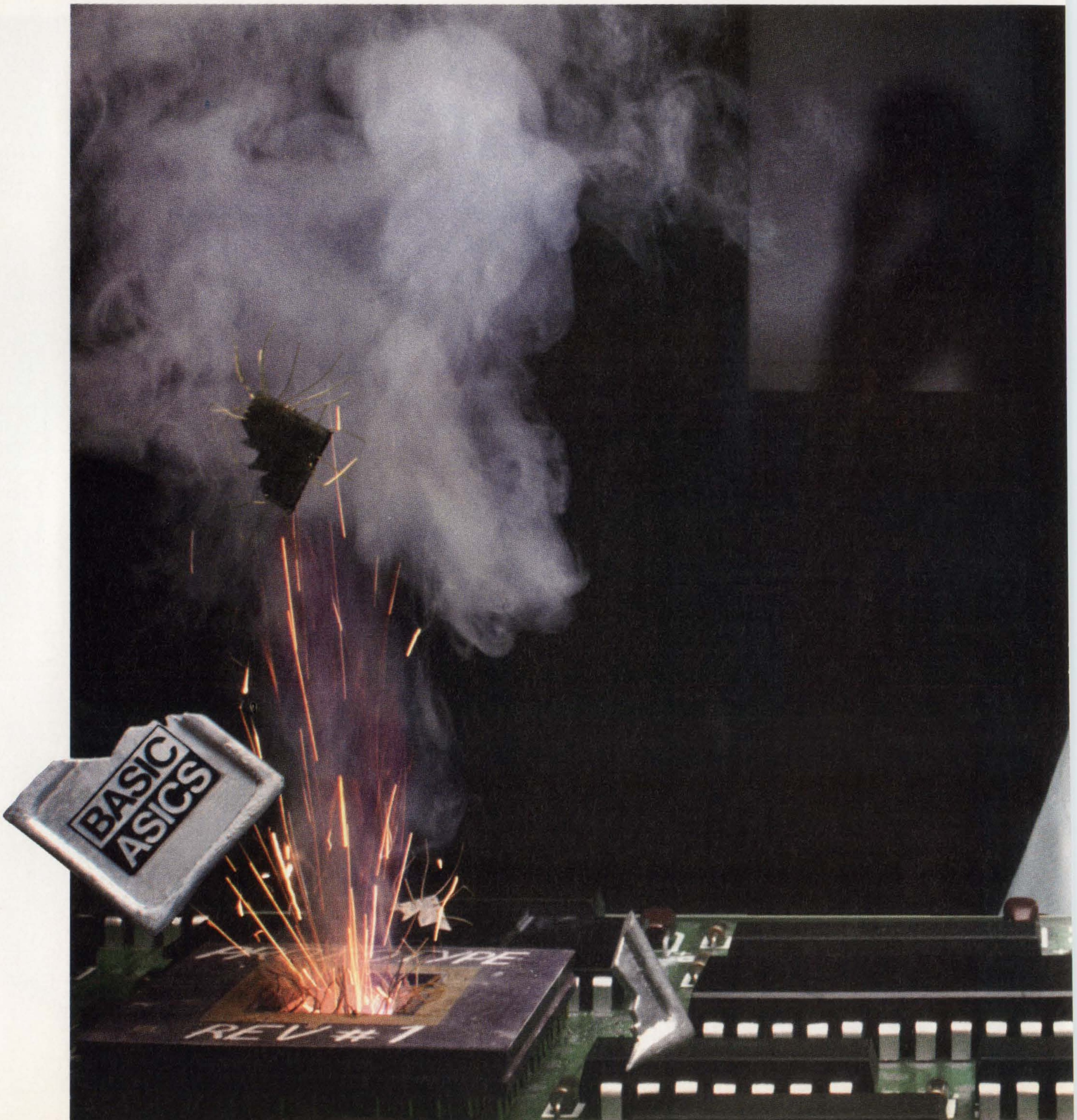

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CIRCLE NO 108

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FUJITSU MICROELECTRONICS, INC.

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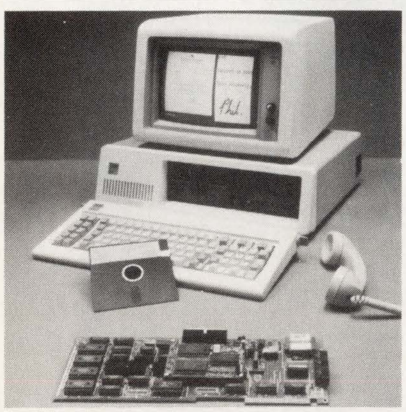
READERS' CHOICE

Of all the new products covered in EDN's **February 5, 1987**, issue, the ones reprinted here generated the most reader requests for additional information. If you missed them the first time, find out what makes them special: Just circle the appropriate numbers on the Information Retrieval Service card, or refer to the indicated pages in our **February 5, 1987**, issue.

RS-232C CHIP
Model SN75155 is a 1-chip RS-232C line-driver and -receiver IC that incorporates the driver functions of the manufacturer's earlier SN75188 and SN75189A devices, respectively (pg 215).
Texas Instruments Inc.
Circle No 603

▲ SERVO AMP
The Model 241 PWM servo amplifier delivers as much as 4.5 kW of power at 98% efficiency (pg 98).
Copley Controls Corp.
Circle No 601

▲ BOARD FABRICATOR
The Protoflex-III Model PF-IIIA prepares prototype PC boards without using chemicals. The device has a CAD interface and scans artwork optically (pg 225).
Girard Electronics.
Circle No 605



▲ FAX FOR IBM PC
Microfax is compatible with Group III facsimile equipment for IBM PCs and compatibles and includes a second modem for asynchronous communications on board (pg 199).
Datacopy Corp.
Circle No 602

DSP DEVELOPMENT
The DSP-320 development system lets you develop DSP programs on an IBM PC or compatible and provides a TMS32010 processor and an analog subsystem (pg 221).
Microcraft Corp.
Circle No 604

LEADTIME INDEX

Percentage of respondents

ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Average (weeks)	Last month's average (weeks)
TRANSFORMERS								
Toroidal	6	19	56	13	6	0	8.6	11.0
Pot-Core	11	22	34	22	11	0	9.6	10.2
Laminate (power)	7	20	60	6	7	0	8.1	9.3
CONNECTORS								
Military panel	0	25	38	25	12	0	10.8	13.7
Flat/Cable	25	25	25	25	0	0	6.6	5.1
Multipin circular	22	11	45	22	0	0	7.3	13.1
PC	15	31	39	15	0	0	6.4	6.2
RF/Coaxial	11	34	22	33	0	0	7.9	6.6
Socket	40	27	20	13	0	0	4.5	5.4
Terminal blocks	28	39	28	5	0	0	4.3	5.9
Edge card	15	39	31	15	0	0	6.0	6.3
Subminiature	22	34	22	22	0	0	6.0	5.7
Rack & panel	10	50	30	10	0	0	5.5	7.6
Power	22	34	33	11	0	0	5.4	7.6
PRINTED CIRCUIT BOARDS								
Single-sided	0	60	27	13	0	0	6.0	5.6
Double-sided	0	45	50	5	0	0	6.1	6.4
Multilayer	0	7	79	14	0	0	8.7	8.0
Prototype	0	71	23	6	0	0	4.9	4.8
RESISTORS								
Carbon film	42	16	26	16	0	0	5.0	2.5
Carbon composition	34	33	11	22	0	0	5.3	4.6
Metal film	29	24	24	23	0	0	6.2	4.0
Metal oxide	20	50	10	20	0	0	5.4	3.6
Wirewound	25	19	31	25	0	0	6.9	5.3
Potentiometers	20	16	48	16	0	0	6.8	5.9
Networks	17	16	39	28	0	0	7.9	6.1
FUSES	39	33	17	11	0	0	4.1	4.8
SWITCHES								
Pushbutton	31	19	38	12	0	0	5.5	7.5
Rotary	17	25	33	25	0	0	7.3	7.5
Rocker	31	31	31	7	0	0	4.6	7.2
Thumbwheel	34	11	33	22	0	0	6.4	10.5
Snap action	34	22	33	11	0	0	5.1	8.7
Momentary	27	9	37	27	0	0	7.4	8.7
Dual in-line	11	22	56	11	0	0	6.8	9.2
WIRE AND CABLE								
Coaxial	23	38	31	8	0	0	4.8	3.1
Flat ribbon	38	19	31	12	0	0	5.0	3.3
Multiconductor	29	28	36	7	0	0	4.8	3.8
Hookup	55	35	10	0	0	0	1.9	1.6
Wire wrap	45	33	22	0	0	0	2.8	2.1
Power cords	21	37	42	0	0	0	4.5	4.3
Other	25	0	75	0	0	0	6.0	4.9
POWER SUPPLIES								
Switching	14	7	50	22	7	0	9.4	9.8
Linear	18	18	37	18	9	0	8.6	6.2
CIRCUIT BREAKERS	20	40	27	13	0	0	5.4	7.4
HEAT SINKS	17	25	50	8	0	0	6.0	5.4

ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Average (weeks)	Last month's average (weeks)
RELAYS								
General purpose	39	22	22	11	6	0	5.6	5.5
PC board	13	20	40	27	0	0	7.9	8.0
Dry reed	12	38	12	38	0	0	7.9	5.7
Mercury	12	0	63	12	13	0	10.1	7.7
Solid state	13	33	27	20	7	0	7.9	5.6
DISCRETE SEMICONDUCTORS								
Diode	25	25	30	20	0	0	6.3	4.3
Zener	24	29	18	29	0	0	6.9	6.3
Thyristor	0	40	30	30	0	0	8.3	5.4
Small signal transistor	13	27	33	27	0	0	7.6	7.0
FET, MOS	0	56	22	22	0	0	6.9	7.6
Power, bipolar	15	31	39	15	0	0	6.4	8.1
INTEGRATED CIRCUITS, DIGITAL								
CMOS	11	34	33	22	0	0	7.1	8.2
TTL	13	34	40	13	0	0	6.3	5.5
LS	7	33	47	13	0	0	6.8	5.9
INTEGRATED CIRCUITS, LINEAR								
Communication/circuit	22	11	34	33	0	0	8.2	9.4
OP amplifier	6	31	44	19	0	0	7.3	8.5
Voltage regulator	8	39	38	15	0	0	6.6	6.7
MEMORY CIRCUITS								
RAM 16k	31	15	23	31	0	0	7.1	5.5
RAM 64k	33	17	33	17	0	0	5.8	5.2
RAM 256k	20	10	40	30	0	0	8.2	6.9
ROM/PROM	27	9	46	18	0	0	6.7	5.9
EPROM	25	38	12	25	0	0	6.0	7.0
EEPROM	11	22	34	33	0	0	8.5	7.3
DISPLAYS								
Panel meters	11	11	56	22	0	0	8.2	5.7
Fluorescent	0	0	57	43	0	0	11.2	8.4
Incandescent	0	25	50	25	0	0	8.6	7.4
LED	12	31	44	13	0	0	6.4	6.3
Liquid crystal	0	25	37	38	0	0	9.6	8.2
MICROPROCESSOR ICs								
8-bit	7	36	29	28	0	0	7.8	7.4
16-bit	11	11	56	22	0	0	8.2	7.4
FUNCTION PACKAGES								
Amplifier	11	11	22	45	11	0	11.8	9.1
Converter, analog to digital	10	20	60	10	0	0	7.0	8.0
Converter, digital to analog	11	22	45	22	0	0	7.7	8.6
LINE FILTERS	12	13	50	25	0	0	8.3	7.0
CAPACITORS								
Ceramic	32	26	32	10	0	0	4.9	6.4
Ceramic monolithic	25	38	31	6	0	0	4.6	8.1
Ceramic disc	15	54	31	0	0	0	4.7	7.5
Film	23	23	54	0	0	0	5.0	8.1
Electrolytic	28	28	33	11	0	0	5.2	6.6
Tantalum	6	44	38	12	0	0	6.3	6.8
INDUCTORS	8	31	38	23	0	0	7.6	8.5

Source: *Electronics Purchasing* magazine's survey of buyers

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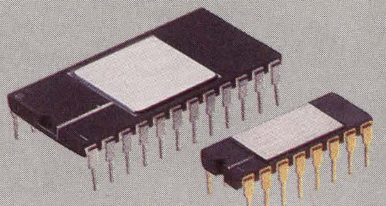

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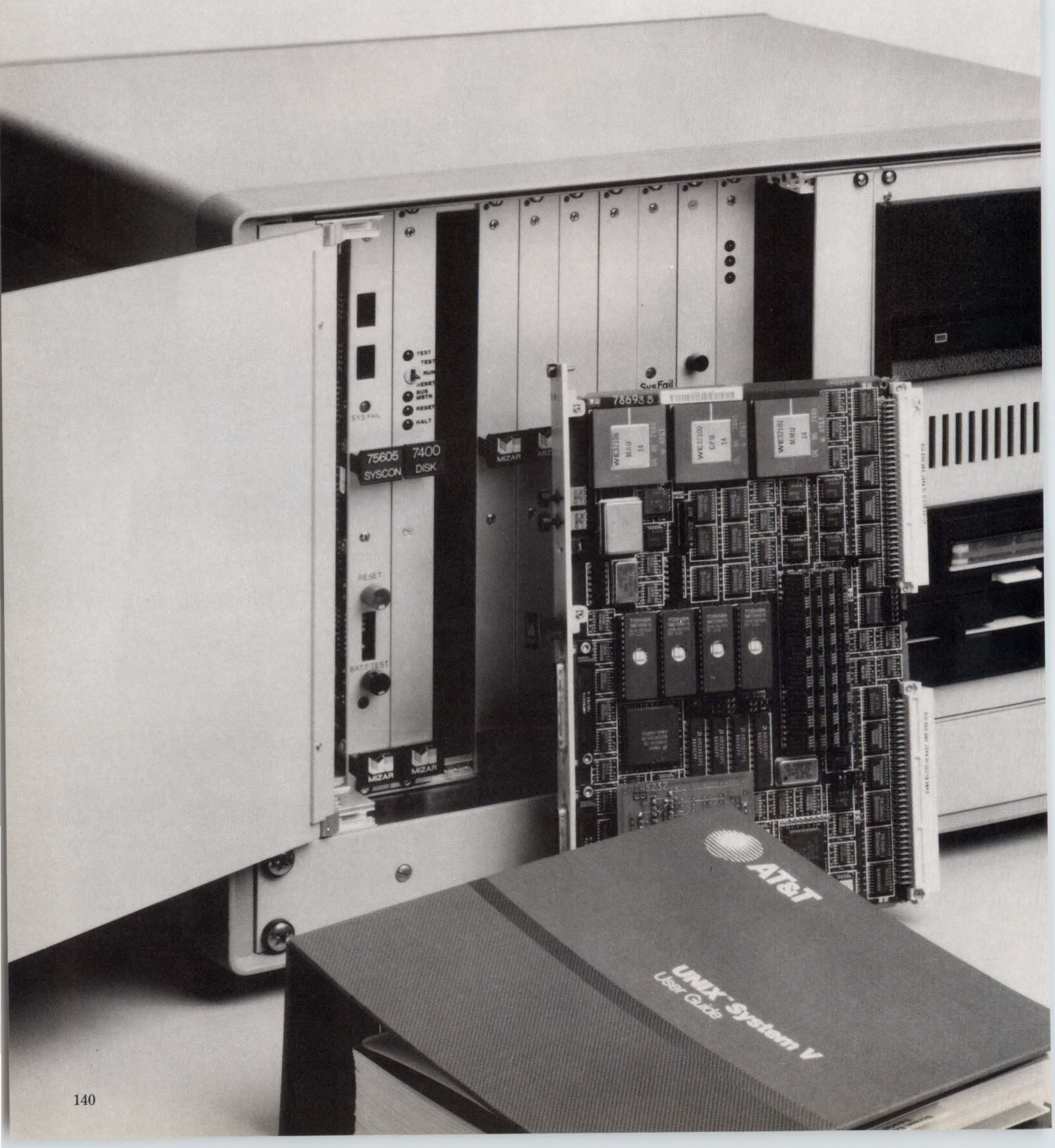
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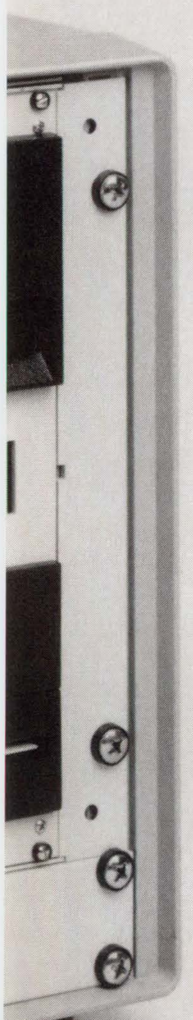

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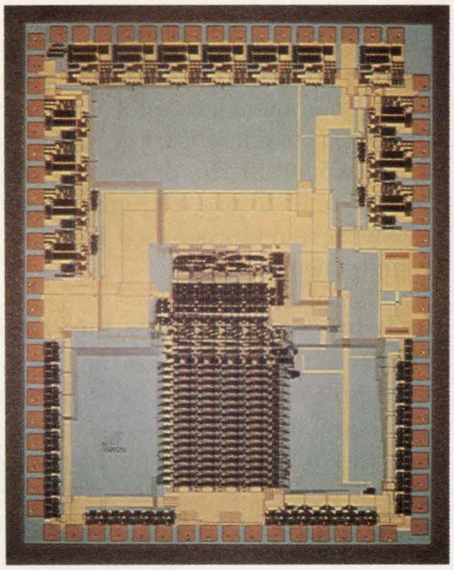
Sophisticated microprogrammable building blocks *have evolved from the industry-standard 2901 4-bit ALU slice. The new parts bring increasing flexibility to the design of high-performance systems. (Photo by Paul Ambrose Studios; courtesy Advanced Micro Devices)*

Microprogrammable processing

Fast, faster, fastest: Designers' need for high-performance computation is driving progress in advanced IC-fabrication processes and architectures for microprogrammable processors. Meanwhile, development-tool vendors are creating better meta-assemblers and linking this software to development stations.



Steven H Leibson, *Regional Editor*

After a decade of slow evolution following the introduction of the industry-standard 2901 bit-slice register/ALU, the microprogrammable-processor field has begun to bustle with activity. You can now find four 2901 slices on one chip, a configuration that improves performance and lowers power consumption. Furthermore, several ASIC manufacturers are offering devices that let you integrate your bit-slice design on a single chip. In addition, you'll find microprogrammable devices with fixed architectures. And if your application calls for high-speed number crunching, you can select a floating-point ALU that can perform operations in less than 100 nsec.

Although high-performance, fixed-instruction-set (FIS) 32-bit μPs (along with their associated coprocessors) and dedicated single-chip processors are vying for the applications—high-speed computing, graphics, and digital signal processing (DSP)—traditionally served by microprogrammable parts, the latter class retains the performance edge, thanks to the recent advances. Generating the software for these parts can be difficult, however. Because each microprogrammable architecture is unique, high-level-language compilers that support microprogramming haven't been available. Now, however, one manufacturer does offer compilers that support its fixed-architecture microprogrammable devices. To program other companies' devices, you'll still need a general-purpose meta-assembler, but today's meta-assemblers are offering high-level features that make them easier to use.

Most microprogrammable processor designs comprise two main sections: the data path and the control path **(Fig 1).** The data path includes the microprogram memory and an ALU, and it may include a multiplier or multiplier/accumulator (MAC) for accelerating calculations. (EDN will publish a Special Report on MACs in the June 11 issue.) The control path includes the

A GaAs fabrication process *allows Vitesse (French for "speed") to build the fastest discrete 2901-style ALU slice in existence. Its A,B-to-Y propagation delay is 15 nsec.*

Microprogrammable designs use extremely fast RAM or ROM for microprogram storage.

microprogram memory, a microsequencer, and a status register for making branch decisions. Because the microprogram memory resides on both paths, the access time of this memory is a key parameter determining the overall speed of the processor. Microprogrammable designs tend to use extremely fast RAM or ROM for microprogram storage (see **Ref 1** for more information on high-speed RAMs).

Early process limitations forced slicing

Because the ALU forms the core of a microprogrammable processor's data-processing section, the propagation delay through the ALU plays the major role in determining data-path performance. Density limitations of mid-1970s IC fabrication processes forced IC vendors to partition early ALUs into "slices," making the term "bit slice" almost synonymous with "microprogrammability." Although Advanced Micro Devices introduced it over a decade ago, the 2901 4-bit ALU slice remains the keystone of many of today's microprogrammable processor designs. Current versions of the 2901, however, exhibit vastly improved performance over the original.

A figure of merit generally agreed upon by vendors of 2901-type devices is the A,B-to-Y propagation delay —the time required for data to exit from a register, flow through the ALU section, and appear at the ALU's Y data output **(Fig 2)** after an address is presented to the part's A or B address inputs (the address inputs select a register within the ALU's register stack). AMD specified the original 2901's A,B-to-Y delay at 110 nsec. Fabricated in a variety of process technologies, including ECL, CMOS, and GaAs **(Ref 2)**, currently available parts exhibit significantly faster performance than the original bipolar part; for example, a GaAs part from Vitesse exhibits a 15-nsec delay. (See **Table 1** for a representative sample of these faster 2901-compatible parts, available from AMD and other vendors.)

These process improvements have led a few IC vendors to integrate multiple 2901s on one chip, along with other assorted circuitry, as a means of improving overall system performance and reducing pc-board real-estate requirements. Several of these devices are listed in **Table 2.** Cypress Semiconductor points out that, although its 16-bit CY7C9101-30 is slower than its CY7C901-23 4-bit ALU slice, the part is faster than a system built from four CY7C901-23s and a lookahead-carry generator. The discrete solution loses speed because of the off-chip and on-chip I/O delays you incur when you add the lookahead-carry generator to the ALU slices.

Logic Devices and Integrated Device Technology

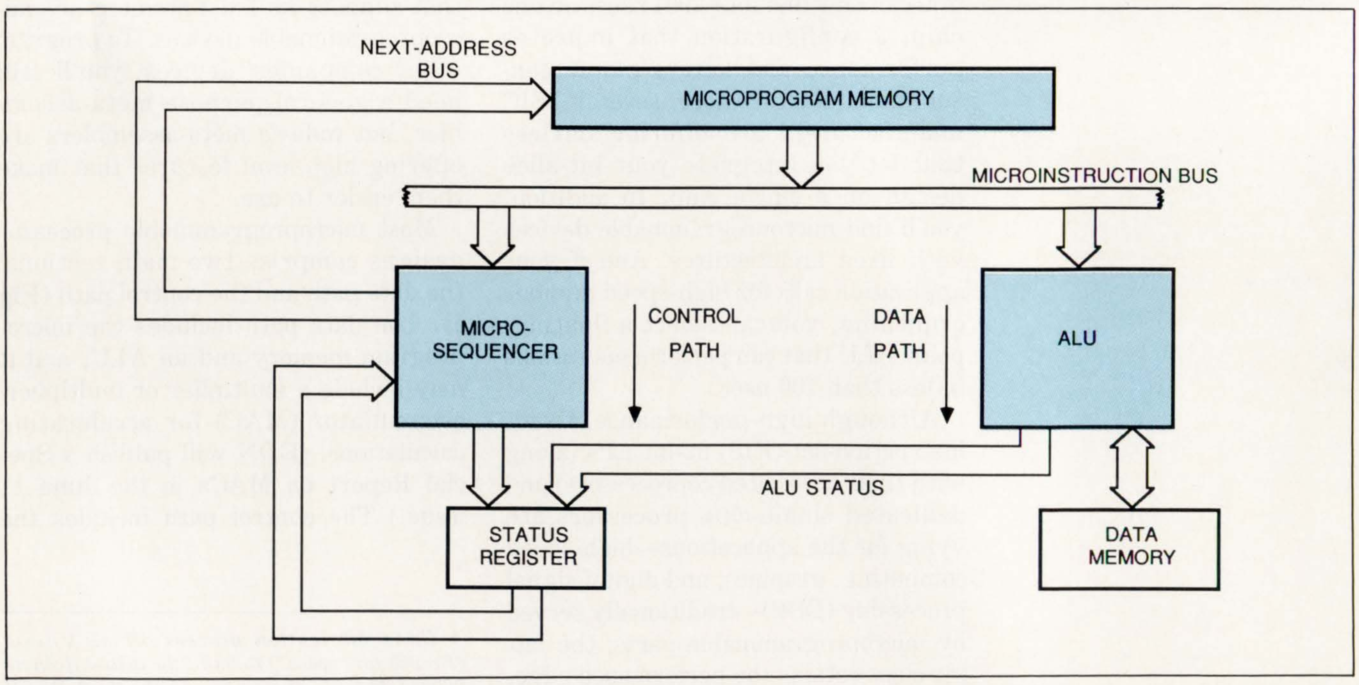
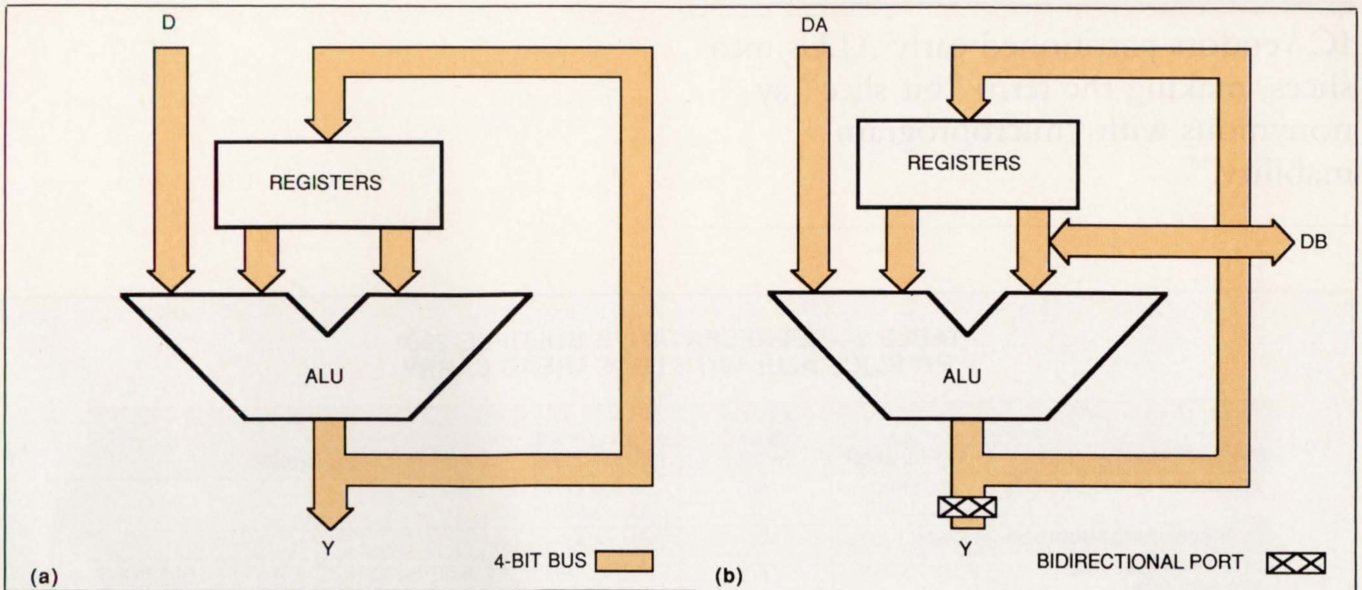


Fig 1—Microprogrammable processors generally comprise two major sections: *the data path and the control path. The slowest path determines the processor's maximum execution speed.*



(IDT) enhanced the 2901 architecture while they were in the process of integrating several of the bit-slice ALUs onto one IC. Logic Devices' L429C01 consolidates four 2901s, lookahead-carry circuits, and pipeline registers. The pipeline registers allow you to omit external registers and to use nonregistered PROMs or RAMs for microcode memory. IDT's 49C402 includes two major architectural improvements: a ninth instruction line that adds extra destinations to existing instructions, and an increase in the number of on-chip registers from 16 to 64. You can use these additional registers in a backwards-compatible, bank-switching mode, for a total of four 16-register banks. (Note that, if you do use a quad-2901 part, your choice of microsequencer for the control path is unaffected.)

Unfortunately, no packaging standards exist for the quad-2901 devices. The Cypress CY7C9101 packaged in both DIPs and PLCCs is compatible (with respect to both pinout and function) with AMD's 29101 and 29C101. The DIP version of IDT's 49C402A is pin compatible with International Microcircuits Inc's 4x2901B, but the LCC and PGA versions are incompatible, and all styles of IDT's and IMI's quad 2901s are not compatible with the pinouts of the corresponding AMD

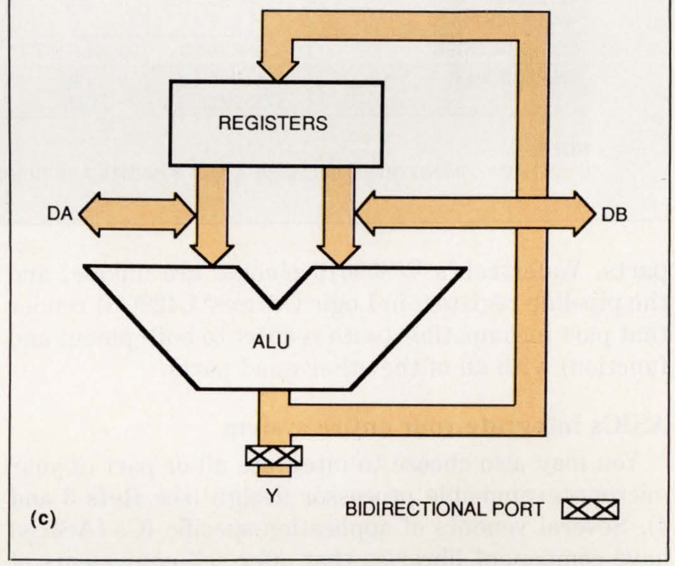


Fig 2—Today's microprogrammable ALU/register files *trace their lineage back to AMD's venerable 2901* ***(a)****, which had one input (D) and one output (Y) data port. Data movement became much easier in the 2903* ***(b)****, which gained a bidirectional DB data port and an improved, bidirectional Y port. The 29203* ***(c)*** *completed the evolution of the ALU/register-file IC by rendering all three data ports bidirectional.*

TABLE 1—REPRESENTATIVE VERSIONS OF THE 2901 4-BIT ALU SLICE

MANUFACTURER	PART NUMBER	A,B-TO-Y DELAY (nSEC)	I_{CC} (mA MAX)	PRICE (100)	COMMENTS
ADVANCED MICRO DEVICES	2901CPC 29C01-1PC	40 40	265 40 (STATIC)	\$6.45 \$6.98	ECL INTERNAL, TTL I/O CMOS
CYPRESS SEMICONDUCTOR	CY7C901-23PC	30	80	\$10.05	CMOS
INTEGRATED DEVICE TECHNOLOGY	IDT39C01EP	22	40	\$10.75	CMOS
VITESSE	VE29G01	15	850	(SEE NOTE)	GaAs
WAFERSCALE	WS5901DP	33	30 (10 MHz)	\$6.25	CMOS

NOTE:
ENGINEERING SAMPLES OF THE VITESSE VE29G01 COST \$435. THE COMPANY ESTIMATES THAT THE VOLUME PRICE OF THE PART WILL BE LESS THAN \$100 (5000/YEAR) BY THE END OF 1987.

IC vendors partitioned early ALUs into slices, making the term "bit slice" synonymous with "microprogrammability."

TABLE 2—REPRESENTATIVE MULTIPLE-2901 BIT-SLICE ALUs WITH LOOKAHEAD CARRY

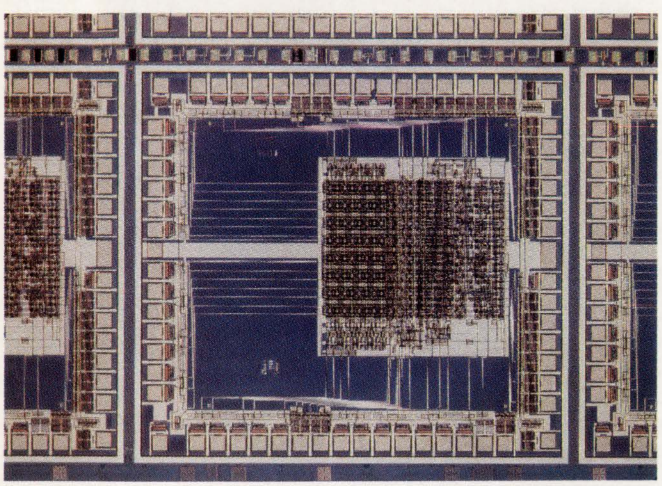
MANUFACTURER	PART NUMBER	A,B-TO-Y DELAY (nSEC)	WIDTH (BITS)	PRICE (100)	COMMENTS
ADVANCED MICRO DEVICES	29C101PC 29C101-1PC	60 37	16 16	$24.44 $28.10	
CYPRESS SEMICONDUCTOR	CY7C9101-30PC	37	16	$50.25	
INTEGRATED DEVICE TECHNOLOGY	IDT49C402AXC	37	16	$44	64 16-BIT REGISTERS, EXTRA INSTRUCTIONS
INTERNATIONAL MICROCIRCUITS	4x2901B064PB	119	16	$30	
LOGIC DEVICES	L429C01PC	90 (SEE NOTE)	16	$40.43	INCLUDES PIPELINE REGISTERS
WAFERSCALE	WS59016DJ WS59032EG	46 58	16 32	$23 $93	 32 32-BIT REGISTERS

NOTE:
CLOCK-TO-Y TIMING GIVEN BECAUSE A AND B INPUTS ARE REGISTERED.

parts. Waferscale's WS59016 pinouts are unique, and the pipeline registers in Logic Devices' L429C01 render that part incompatible (with respect to both pinout and function) with all of the other quad parts.

ASICs integrate your entire system

You may also choose to integrate all or part of your microprogrammable processor design (see **Refs** 3 and 4). Several vendors of application-specific ICs (ASICs) have component libraries that offer cell equivalents of devices in the AMD 2900 family. ASIC manufacturers supporting microprogrammable designs are listed in **Table** 3 along with the supported library components



Packing four 2901-style ALUs *and a lookahead-carry generator on one chip, this Am29C101 16-bit ALU slice from Advanced Micro Devices can save you pc-board real estate.*

for each ASIC.

Some vendors' ASICs offer unique features that complement microprogrammable processor design. Gould's (formerly AMI) Megacell ASIC product offers A/D and D/A converters, plus other analog components, in addition to the more traditional digital cells—lookahead-carry generator, microsequencer, etc. LSI Logic's structured arrays offer uncommitted gate arrays with special, optimized structures. The company's LSA2005, 2006, and 2011 respectively combine uncommitted gate arrays with four 2901s and a 32k-bit ROM, eight 2901s and a 64k-bit ROM, and four 2901s and a 16×16-bit MAC. Waferscale's Modular-Cell semicustom ASIC library contains EPROM cells with 40- to 50-nsec access times, allowing you to include reprogrammable, nonvolatile microcode storage directly on your chip.

IC manufacturers are not relying solely on faster processes to improve ALU performance. Although faster parts execute more instructions per second, architectural improvements allow the parts to do more processing during each instruction cycle, because of the increased parallelism.

Traditional μPs are at a disadvantage

Most conventional μPs bring instructions and data onto the chip over a single data bus. This situation, called the Von Neumann bottleneck, limits the maximum rate of data flow through the processor. Microprogrammable architectures enjoy a fundamental advantage over conventional μPs; they have separate instruction and data buses to give them an immediate performance boost. Architectural improvements to mi-

TABLE 3—REPRESENTATIVE ASICs SUPPORTING MICROPROGRAMMABLE COMPONENTS

MANUFACTURER	ASIC PART NUMBER	MICROPROGRAMMABLE ELEMENTS SUPPORTED IN LIBRARY (SEE NOTE 1)	IC PROCESS	2901 A,B-TO-Y DELAY (nSEC)	NRE CHARGES	PART COST
CALIFORNIA DEVICES	CHA3200	2901, 2910	CMOS	51	$18k TO $24k	$7 (10,000) IN AN 84-LEAD PLCC
GOULD INC	MEGACELL	2901, 2902, 2904, 2909, 2910, 2911	HCMOS	72	(SEE NOTE 2)	(SEE NOTE 2)
INTEGRATED LOGIC SYSTEMS	CA2000	2901, 2902, 2904, 2910	CMOS	67	$25k TO $55k	$22.77 (5000) FOR A CA2110 IN AN 84-LEAD PLCC
LSI LOGIC	LSA2005	2901, 2902, 2903, 29203, 2904, 2909, 2910, 2910A, 16-BIT 2910, 2911, 29116, 29117, 29501	HCMOS	56	$40k TO $80k	$50 TO $150 COMMERCIAL, BASED ON PACKAGE AND VOLUME
	LSA2006	SAME AS LSA2005	HCMOS	66.1	SAME AS LSA2005	SAME AS LSA2005
	LSA2011	SAME AS LSA2005	HCMOS	56	SAME AS LSA2005	SAME AS LSA2005
NATIONAL SEMICONDUCTOR	SCX6200	2901, 2909, 2911	CMOS	29	$15k TO $70k	(SEE NOTE 3)
	SCL	2901, 2909, 2911	CMOS	29	$30k TO $70k	(SEE NOTE 4)
UNICORN	COMPILE	29C01, 29C03, 29C10, 29C14	CMOS	10 (TYP)	FROM $50k	(SEE NOTE 5)
VTC	VL2000	2901, 2902	CML	3.25	$40k TO $50k	(SEE NOTE 6)
WAFERSCALE	MODULAR-CELL	8-, 16-, 32-BIT 2901s, 2910A	CMOS	30 (4-BIT)	$60k TO $125k	(SEE NOTE 7)

NOTES:

1. KEY TO 2901 FAMILY:

2901	4-BIT ALU SLICE
2902	LOOKAHEAD-CARRY GENERATOR
2903, 29C03	4-BIT EXPANDED-FUNCTION ALU SLICE
29203	4-BIT ALU SLICE WITH BCD ARITHMETIC
2904	STATUS AND SHIFT-CONTROL UNIT
2909	4-BIT MICROSEQUENCER SLICE
2910, 29C10, 2910A	12-BIT MICROSEQUENCER
2911	4-BIT MICROSEQUENCER SLICE
29116	16-BIT ALU
29117	2-PORT, 16-BIT ALU
29501	MULTIPORT, PIPELINED, 8-BIT ALU SLICE

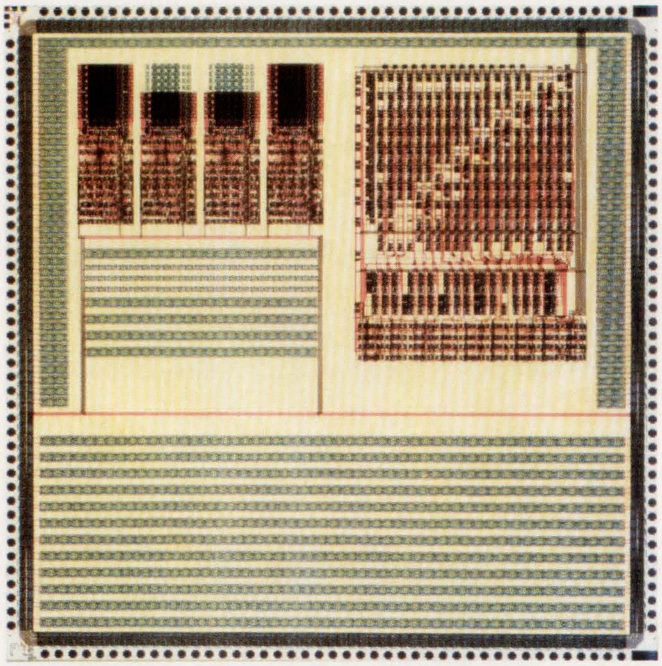
2. HYPOTHETICAL GOULD MEGACELL ASIC:

FUNCTION			% AREA CHIP USAGE
MICROCODE ENGINE COMPONENTS:	QUANTITY DEVICE		
	1 2910 MICROSEQUENCER		
	4 2901 4-BIT SLICE ALU		
	1 2902 LOOKAHEAD CARRY		
	— REGISTERS, MUXES (1000-GATE EQUIVALENT)	SUBTOTAL	29%
MICROCODE STORAGE:	1k-WORD×60-BIT ROM		22%
AUXILIARY STORAGE:	1k-WORD×16-BIT ROM		
	512-WORD×16-BIT RAM	SUBTOTAL	24%
PROPRIETARY DIGITAL COMPONENTS:	2000-GATE EQUIVALENT RANDOM LOGIC		15%
ANALOG INTERFACE CIRCUITS:	FILTER, SAMPLE AND HOLD, ANALOG SWITCHES, COMPARATOR, VOLTAGE DOUBLER, CLOCK CIRCUITS	SUBTOTAL	10%
		TOTAL	100%

USER PROVIDES GOULD WITH A SEMIVALIDATED NET LIST USING GOULD LIBRARIES. NRE COST: LESS THAN $50,000; PART COST: LESS THAN $30 (10,000/YEAR) IN 68-LEAD PLCC.

3. A NATIONAL SEMICONDUCTOR SCX6287 GATE ARRAY WITH A 16-BIT ALU REPRESENTING APPROXIMATELY 25% OF THE DIE AREA, PACKAGED IN AN 84-LEAD PLCC, WOULD COST APPROXIMATELY $39.
4. A NATIONAL SEMICONDUCTOR SCL SEMICUSTOM ASIC WITH A 16-BIT ALU REPRESENTING APPROXIMATELY 25% OF THE DIE AREA, PACKAGED IN AN 84-LEAD PLCC, WOULD COST APPROXIMATELY $32.
5. A UNICORN ASIC GENERATED FROM THE COMPILE LIBRARY WITH A 16-BIT ALU REPRESENTING APPROXIMATELY 25% OF THE DIE AREA, PACKAGED IN A 68-PIN PLCC, WOULD COST APPROXIMATELY $14 (50,000).
6. A VTC VL2000 SEMICUSTOM ASIC WITH A 16-BIT ALU REPRESENTING APPROXIMATELY 25% OF THE DIE AREA, PACKAGED IN AN 84-LEAD PLCC, WOULD COST APPROXIMATELY $50 (5000/YEAR).
7. A WAFERSCALE MODULAR-CELL ASIC WITH A 32-BIT ALU, A 1k-WORD×64-BIT EPROM, A 6k-BIT RAM, AND A 5910 MICROSEQUENCER IN A 132-PIN PLASTIC PGA COSTS APPROXIMATELY $200 (5000/YEAR).

Although faster parts execute more instructions per second, architectural improvements allow the parts to do more processing during each instruction cycle.



You can integrate an entire microprogrammable system *onto one piece of silicon using semicustom or gate-array ASIC products like this LSA2011 structured array from LSI Logic. The device incorporates four 2901 ALUs, a 16×16-bit multiplier/accumulator, and 5000 uncommitted logic gates.*

croprogrammable ALU products have focused on maximizing data flow through the ALU.

Fig 2 shows several evolutionary stages in the fundamental architecture of AMD's bit-slice ALU designs. The 2901 **(Fig 2a)** has two unidirectional data ports: a D port for input and a Y port for output. (Not shown in the figure is the separate instruction port.) The 2901 therefore enjoys improved data movement over a μP, because it's a flow-through device and because it avoids the Von Neumann bottleneck.

Microprogrammable ALUs have evolved

Although the 2901 design allows much faster data processing than a traditional μP, AMD realized that the design had far more potential than was realized in the original part. This realization led to devices with improved architectures: the Am2903ADC Superslice and the Am29203DC. Both parts cost $20.50 (these and all subsequent prices are for quantities of 100, except where otherwise noted). In the 2903 **(Fig 2b),** AMD made the Y port bidirectional and added another bidirectional port, called the DB port. This port allows the 2903 to produce data from the register stack while it's emitting a result from the ALU, and thus either driving this result out of the device over the Y port or into a register in the 2903's stack. You can also expand the device's register stack by connecting external registers to the DB port.

In the 29203 design **(Fig 2c),** the DA port also allows bidirectional data flow, and the device's enhanced ALU executes BCD instructions. IDT serves as an alternate source for the 2903 and 29203 with its IDT39C03AP and IDT39C203AP, which cost $18.25 apiece. The company also offers a quad version of the 2903, called the IDT49C403G, with an expanded, 64-word register file. This part costs $79.

Another bit-slice ALU that shares the 3-bidirectional-port architecture of AMD's 29203 is the 74AS888 8-bit ALU slice from Texas Instruments. This device includes a second shifter, called the MQ shifter, outside the ALU. The MQ shifter allows the 74AS888 to perform some double-precision operations. The register stack in the 74AS888 has three address inputs that allow the processor to take two operands from the stack, operate on these values in the ALU, and place the result in a third register location—all within one clock cycle.

High-speed ALU slices solve only part of the performance problem for designers of microprogrammable processors. They speed the data path but leave the control path unaffected, and unless you speed the control path, you don't really have a faster processor. The speed of the microprogrammable processor's microsequencer largely determines the rate at which the control path may operate.

The microsequencer contains the program counter, return-address stack, and branch-control circuitry for the microprogrammable processor. Improved fabrication processes, architectural enhancements, and deeper stacks have led to the recent advances in microsequencer performance.

AMD initially offered the Am2909 and Am2911 4-bit, sliced microsequencers for the 2901. These two parts are still available and cost $5.25 and $3.35, respectively. The company discovered that a large number of 2901-based designs used three of these 4-bit slices to create 12-bit microsequencers, so it created the single-chip, 12-bit 2910, currently available as the 2910A. Several manufacturers offer microsequencers compatible with the 2910A. Some faster and architecturally enhanced devices are also available **(Table 4).**

TI's $25 (1000) 74AS890 microsequencer slice generates a 14-bit microprogram address. Possibly more important, however, is the fact that, under program

Floating-point ALUs revive microprogrammable μPs

With the constant progress in processing power made by FIS μPs, IC vendors are hard-pressed to keep their microprogrammable designs at the top of the performance heap. Designers have called for more number-crunching capability than 16- or 32-bit fixed-point processing can provide, even at bit-slice rates. Manufacturers are responding with high-speed, floating-point ALUs that sweep away calculation-range limitations by offering advanced computational capabilities for both very small and very large numbers.

IEEE Standard 754 created a floating-point format with a dynamic range of 2^{277}. Most available floating-point ALUs use this format, and a few offer Digital Equipment Corp's floating-point format also. **Table A** lists several floating-point ALUs and their capabilities. Some products incorporate both an ALU and a multiplier on one chip, while others offer separate ALU and multiplier ICs. In addition, some products perform both integer (fixed-point) and floating-point calculations, while others support integer arithmetic by performing fixed-point to floating-point conversions (and vice versa).

The number of ports available on a part subtly affects system performance. Single-port devices require three cycles for operand loading and result extraction. Dual-port products allow a flow-through operation, but you still need two cycles to stuff operands into the inputs. A 3-port device lets you deposit two operands in one cycle while extracting the result. More ports on a device means more pins, however, and the need for more pins drives up the part and system-integration costs.

TABLE A—REPRESENTATIVE FLOATING-POINT ALUs AND MULTIPLIERS

MANUFACTURER	PART NUMBER	NUMERIC FORMATS	OPERATIONS	NUMBER OF PORTS	CYCLE TIME (nSEC)	PRICE (100)
ADVANCED MICRO DEVICES	AM29325	IEEE, DEC, INTEGER (32 BITS)	ADD, SUB, MUL, FMT	3	NOT SPECIFIED	$495
ANALOG DEVICES	ADSP-3210	IEEE, INTEGER (32 AND 64 BITS)	MUL, IMUL	2	100 TO 400	$350
	ADSP-3220	IEEE, INTEGER	ADD, SUB, ABS, NEG, CMP, IADD, ISUB, IABS, BOL, FMT	3	100	$350
BIPOLAR INTEGRATED TECHNOLOGY	2110 (TTL I/O)	IEEE, DEC, INTEGER (32 AND 64 BITS)	MUL, IMUL, DIV, SQR	3	35 TO 325	$490
	2120 (TTL I/O)	IEEE, DEC, INTEGER (32 AND 64 BITS)	ADD, SUB, ABS, NEG, CMP, MIN/MAX, IADD, ISUB, BOL, ROT, SHIFT, FMT	3	10 (INTEGER) 25 (FLOATING-POINT) 25 (CONVERSIONS)	$490
	3110 (ECL I/O)	IEEE, DEC, INTEGER (32 AND 64 BITS)	MUL, IMUL, DIV, SQR	3	35 TO 325	$640
	3120 (ECL I/O)	IEEE, DEC, INTEGER (32 AND 64 BITS)	ADD, SUB, ABS, NEG, CMP, MIN/MAX, IADD, ISUB, BOL, ROT, SHIFT, FMT	3	10 (INTEGER) 25 (FLOATING-POINT) 25 (CONVERSIONS)	$640
LSI LOGIC	L64132	IEEE, DEC, INTEGER (32 BITS)	ADD, SUB, NEG, MUL, FMT	3	60	<$300 (500)
TEXAS INSTRUMENTS	74ACT8837	IEEE, INTEGER (32 AND 64 BITS)	ADD, SUB, MUL, CMP, ABS, NEG, FMT	3	NOT SPECIFIED	$250 (1000)
WEITEK	WTL2264-100	IEEE, INTEGER (32 AND 64 BITS)	MUL, IMUL	3	100	$382
	WTL2265-100	IEEE, INTEGER (32 AND 64 BITS)	ADD, SUB, NEG, CMP, ABS, FMT, IADD, ISUB, BOL	3	100	$382
	WTL3132-100	IEEE, INTEGER (32 BITS)	ADD, SUB, MUL, MAC, ABS, FMT	1	100	$350
	WTL3332-100	IEEE, INTEGER (32 BITS)	ADD, SUB, MUL, MAC, ABS, FMT	2	100	$425

KEY:
ADD = ADDITION
SUB = SUBTRACTION
MUL = MULTIPLY
MAC = MULTIPLY/ACCUMULATE
ABS = ABSOLUTE VALUE
SQR = SQUARE ROOT
NEG = NEGATION
CMP = COMPARE
IADD = INTEGER ADDITION
ISUB = INTEGER SUBTRACTION
IABS = INTEGER ABSOLUTE VALUE
IMUL = INTEGER MULTIPLY
BOL = BOOLEAN
ROT = ROTATE
FMT = FORMAT CONVERSION

Microprogrammable architectures enjoy a fundamental advantage over conventional μPs.

TABLE 4—2901-BASED MICROSEQUENCERS

MANUFACTURER	PART NUMBER	MIN CYCLE TIME (nSEC)	PRICE (100)	COMMENTS
ADVANCED MICRO DEVICES	AM2910APC	50	$12.95	
	AM29C10APC	100	$13.62	
CYPRESS SEMICONDUCTOR	CY7C910-40PC	40	$17.25	17-WORD STACK
INTEGRATED DEVICE TECHNOLOGY	IDT39C10CP	35	$17	33-WORD STACK
	IDT49C410	35	$24.70	33-WORD STACK, 16-BIT ADDRESSING
VITESSE	VE29G10A	12	(SEE NOTE)	
WAFERSCALE	WS5910AP	51	$12.50	

NOTE:
ENGINEERING SAMPLES OF THE VITESSE VE29G10A COST $475. THE COMPANY ESTIMATES THAT THE VOLUME PRICE OF THE PART WILL BE LESS THAN $150 (5000/YEAR) BY THE END OF 1987.

control, the device can select the next microprogram address from any one of eight sources (as opposed to the 2901's four), including two address-input ports, internal registers, the microprogram stack, the program counter, and a multiway branch calculator. This last address source supports 16-way branching through external control of the four LSBs of the branch address. Additional address-generation flexibility often translates into smaller microprograms and faster program execution.

Data-address generator computes for DSP

Up to now, designers were forced to use additional ALU slices for designs, such as DSP systems, requiring complex data-address computation, because available microsequencers were not equal to the task. To accommodate the sequencing and address-generation requirements of DSP calculations, Analog Devices offers a 2-chip set: the $65 ADSP-1401 program sequencer and $45 ADSP-1410 data-address generator. Both devices feature on-chip pipeline registers that allow you to use nonregistered microprogram memory. The program sequencer features a 64-word RAM that you partition into subroutine-stack, register-stack, and indirect-jump areas through on-chip pointer registers. The ADSP-1410 performs data-address calculations for table-look-up routines commonly used for digital filtering, FFT computation, matrix manipulation, and DMA transfers.

The data address generator's highly parallel architecture can deliver a data-memory address while it's modifying a base address with an offset for the next data cycle, comparing the current address with an internal counter, and reinitializing its base-address counter if the comparison is true. This sequence supports circular data buffering and N-modulo addressing without requiring extra cycles for pointer calculations.

Observing a trend towards wider data-word widths (for more accurate calculations) in microprogrammable DSP designs, Analog Devices oriented its microprogrammable ADSP data-path ICs towards floating-point computation and DSP applications. The ADSP-3220 ALU and ADSP-3210 multiplier both operate on fixed-point and floating-point data (see **box,** "Floating-point ALUs revive microprogrammable processing"). Neither the ADSP-3210 nor the ADSP-3220 is sliced.

Advanced IC-fabrication processes have allowed vendors to offer wide microprogrammable parts without resorting to bit slicing at all. Non-bit-sliced parts for microprogrammable designs offer features unattainable using bit-slice technology. AMD's 29116 and 29117 16-bit ALUs feature funnel shifters that can shift or rotate a 16-bit word by one to 15 bits in one cycle. Bit-slice parts cannot support funnel shifting without acquiring an unrealistic quantity of I/O pins. The 29116 and 29117 are available in bipolar and CMOS versions as the Am29L116ADC, Am29C116DC, AM29117GC, and Am29C117GC, which cost $65, $49, $155, and $95, respectively.

As microprogrammable-processor parts attain 32-bit word widths, vendors are again resorting to slicing, but at the functional level rather than the bit level. Bit-slice ALU products combine the ALU and register stack in 4-, 8-, or 16-bit cascadable ICs; they give you the flexibility to create processors with unusual word widths. Functionally sliced products are noncascadable and can offer more complex internal functions, such as funnel shifters; these parts give you greater architectural flexibility, because the blocks contain elemental processor components that you can combine as your

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User interface combines menus and command line control to provide the optimum combination of speed and convenience to quickly isolate system faults.

The HMI-200 series of microprocessor in-circuit emulators combine all of the features of an emulator and a powerful logic analyzer while utilizing your own IBM PC family or UNIX-based computer. These emulators are a result of HMI's years of experience in the design and application of emulators for all popular microprocessors and offer performance and capability that is unexcelled. Units are initially available to support the 68000 family (68000, 68008 and 68010) and the 64180.

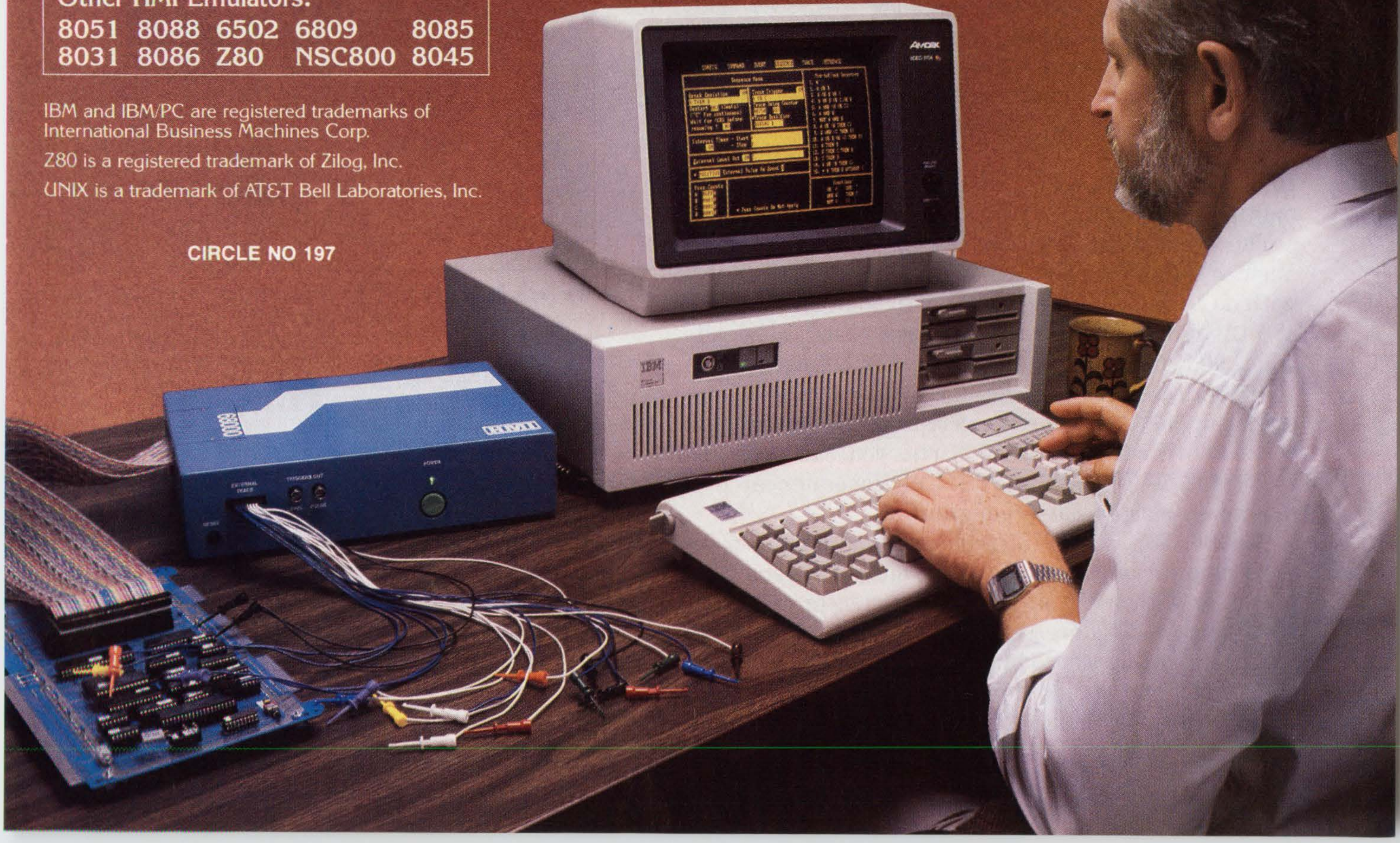
And one more big plus, HMI *delivers* technical support that others only talk about. For complete technical information write to, Huntsville Microsystems, Inc., P.O. Box 12415, 4040 South Memorial Parkway, Huntsville, AL 35802, or call (205) 881-6005. TWX 510-600-8258.

HMI

Other HMI Emulators:

8051	8088	6502	6809	8085
8031	8086	Z80	NSC800	8045

CIRCLE NO 197



High-speed ALU slices solve only part of the performance problem. They speed the data path but leave the control path unaffected.

design requirements dictate.

AMD's 29300 family of 32-bit functional slices includes the $99 29331 16-bit sequencer, the $222 29332 32-bit integer ALU, the $89 29334 4-port register file, and the $495 29325 floating-point ALU/multiplier. Like the company's earlier 16-bit 29116, the 29332 ALU incorporates a funnel shifter, which enables the device to perform *n*-bit shifts or field extractions in one cycle.

By placing the register file and ALU on separate ICs, AMD effectively created a 4-port ALU design **(Fig 3)**, resulting in even greater data-movement flexibility than the 29203's architecture can achieve. The ability to move data is enhanced through the register file's four address ports, which allow the device to perform two register-read operations and two write operations during one cycle. The 29300 family design leads to reliable system design and operation by allowing two microsequencers and ALUs to run in a redundant master/slave mode. In addition, most devices in the family generate and check byte-level parity on the 32-bit data buses.

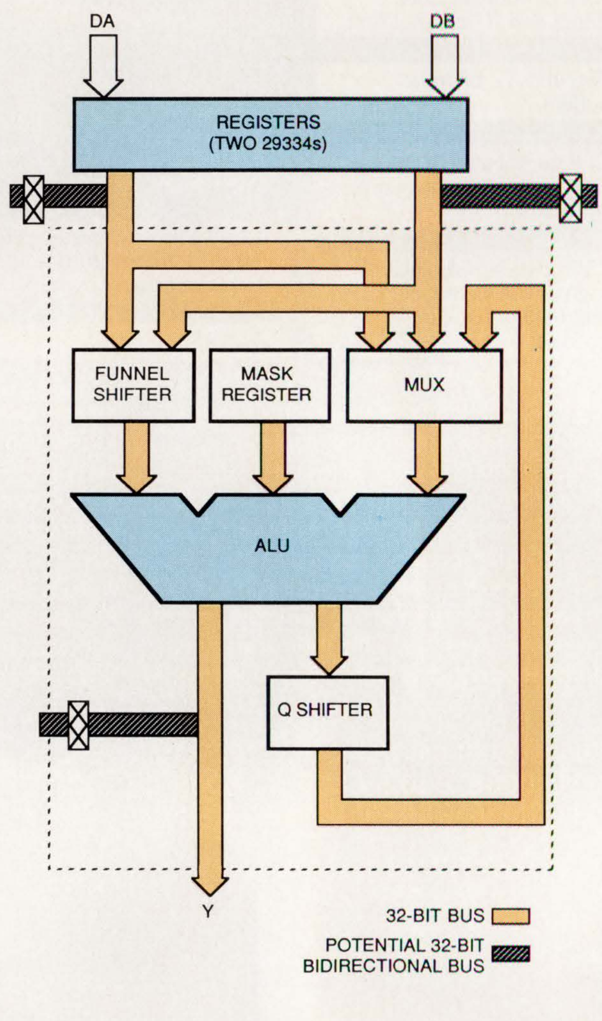


Fig 3—By separating the ALU and register file *into the Am29332 ALU and Am29334 register file, Advanced Micro Devices offers you even greater data-movement flexibility than its 29203 can provide. The 4-port register file accepts two values and delivers two values in one machine cycle, and the feedback path between the ALU and register file is external to the ICs so you can connect these parts to best suit your architectural needs.*

Configurations include SIMD engine

TI is another company that offers a 32-bit, functionally sliced set of microprogrammable devices, based on its 8-bit-sliced parts. The 74AS88XX family comprises nine components, including the $350 74AS8832 ALU and the $110 74AS8835 microsequencer. The ALU incorporates features similar to those of the 8-bit 74AS888 slice, including dual shifters and 3-operand functions. You can run the 74AS8832 as a 32-bit ALU, or you can partition its internal resources into two 16-bit or four 8-bit ALUs, creating a single-instruction, multiple-data (SIMD) engine.

The 74AS8835 operates as a 16-bit microsequencer. You can expand the address width in 16-bit increments, with no performance degradation, by ganging additional 74AS8835s. The device's 65-word stack is 20 bits wide, allowing four status bits to be stored with each 16-bit address placed on the stack. The extremely deep stack supports very deep microprogram nesting. As you can with AMD's 29300 parts, you can pair TI's 74AS8832 ALU and 74AS8835 microsequencer in a redundant master-slave configuration.

Weitek's $385 7136/7137 sequencer and integer-processor chip set implements a 32-bit microprogrammable processor with two ICs. The 7136 sequencer generates 32-bit microcode addresses and 32-bit data addresses in parallel, allowing you to build a machine with 4G words of program and an additional 4G words of data. Code- and data-memory fault interrupts support virtual microcode; if the selected word is not in physical memory, the associated memory-fault interrupt can activate a virtual-memory management routine.

The 7137 integer processor includes a 4-port register file with 3-operand addressing. Four of the registers in the file are backed by shadow registers, allowing the microcode to execute a single-instruction context swap. An integral shift/merge unit executes single-cycle *n*-bit shifts, field extractions, bit deposits, and merging. You

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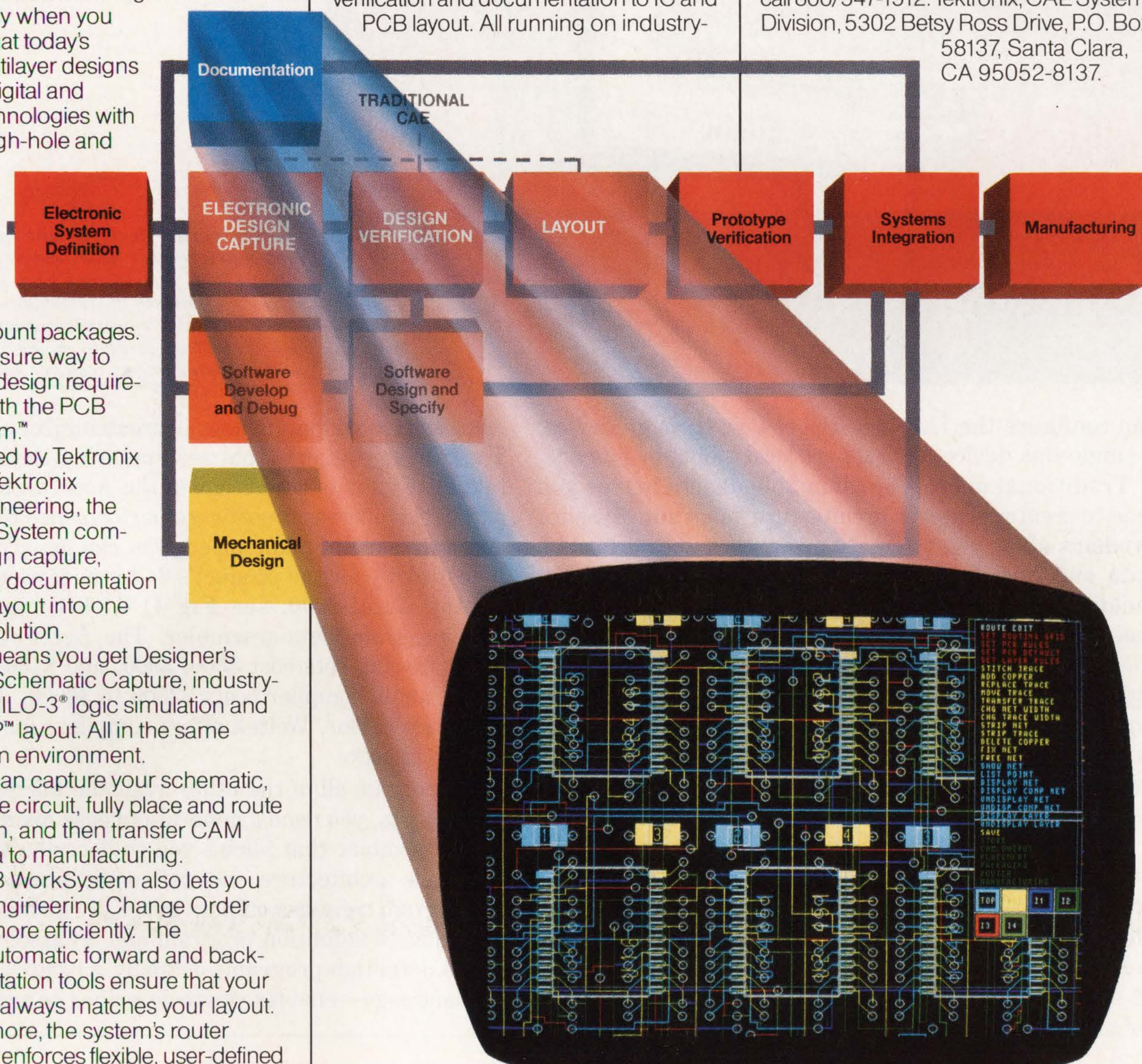

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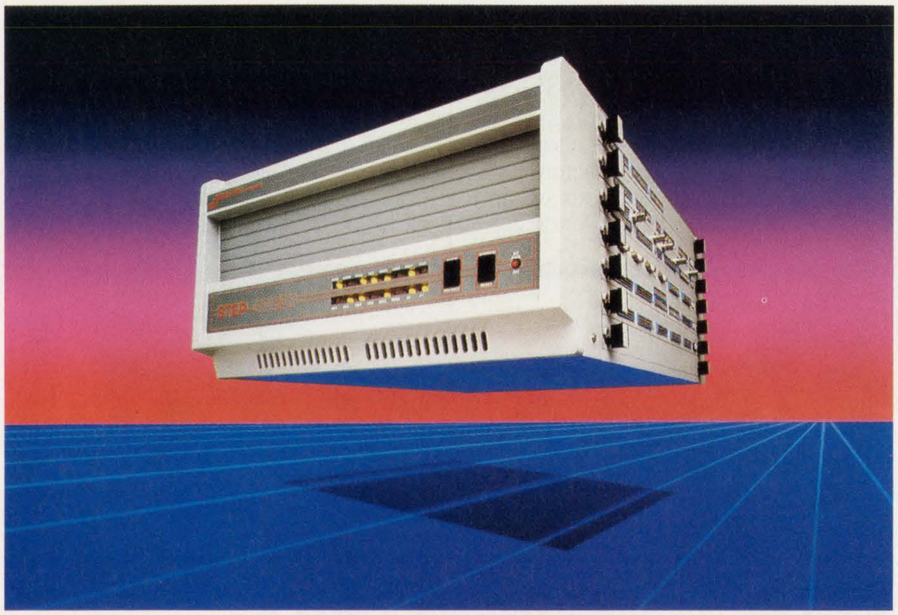
Non-bit-sliced parts for microprogrammable designs offer features that are unattainable using bit-slice technology.



Microprogram development systems give you mastery *over your evolving processor design. This Step-40 from Step Engineering accepts a variety of writable-control-store memory cards, logic-analyzer cards, and device-emulation cards to match the size and scope of your project requirements.*

can configure the 7137 as a 2-port flow-through device, a single-bus device, or a 2-port local/global-bus device.

Traditional microprogrammable design leaves you free to create whatever architecture you want. Bit-slice products allow you to create processors with arbitrary data and microprogram word widths, and functional building blocks let you arrange custom architectures to meet your needs. However, the hardware flexibility of these approaches limits microprogram-generation software. Because each microprogrammable architecture is unique, software vendors have been unable, until now, to supply high-level-language compilers for microprogrammable machines, even though such compilers are plentiful for FIS µPs.

By creating a family of fixed-architecture microprogrammable-processor chip sets, Weitek was able to develop high-level-language compilers (C, Fortran, and Pascal) that emit microcode. The three chip sets, called the Accel 8000, 8032, and 8064, offer 32-bit integer, 32-bit floating-point/32-bit integer, and 64-bit floating-point/32-bit integer computational capability, respectively.

All three Accel µPs feature separate 4G-word code and data address spaces. ICs common to the three products are the program-sequencing unit (PSU) and integer-processing unit (IPU). The 8032 and 8064 each add one floating-point unit (FPU); the 8032 FPU supports 32-bit single-precision calculations, and the 8064 FPU supports 32-bit single-precision and 64-bit double-precision calculations.

Accel compilers generate intermediate code that feeds a software parallelizer to create object microcode. The company asserts that restructuring the microcode to take maximum advantage of the Accel architecture's parallelism increases software performance by as much as 200%. For optimum speed, you can generate microcode directly for the product's 64-bit microword (32 bits for the Accel 8000; see **Fig 4**) with the company's microprogram meta-assembler. The Accel 8000, 8032, and 8064 chip sets cost $500, $900, and $1200, respectively, and a compiler costs $2500 to $6000, depending on the processor. Weitek offers compilers for VAX and IBM PC hosts.

To program all of the other available microprogrammable parts, you need a general-purpose microprogram meta-assembler that allows you to describe the target hardware architecture and define the microword. Microprogram meta-assemblers generally include two key programs: a definition program and an assembler.

The definition program—actually a hardware-definition language—enables you to describe the architecture

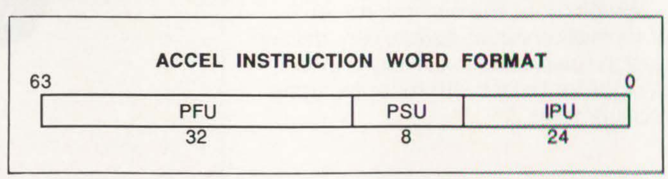


Fig 4—That a fixed-architecture processor can be microprogrammable *is evident in the 64-bit instruction word in Weitek's Accel µP Series devices. The family's 8032 and 8064 processors use the full 64-bit microword, divided into a 24-bit field for the integer processing unit (IPU), an 8-bit field for the program sequencing unit (PSU), and a 32-bit field for the floating-point unit (FPU).*

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Traditional microprogrammable design leaves you free to create whatever architecture you choose.

of your target microprogrammable processor by defining the various fields within the processor's microword, thereby creating a unique assembly language for your particular design. The assembler, like any μP assembler, takes a file containing assembly-language source code and translates mnemonics into microcode bit patterns using the microword and field definitions created with the definition program.

Early microprogram meta-assemblers, such as AMD's Amdasm, forced you to create assembly syntaxes that closely resembled the actual microcode layout. (Amdasm, which is no longer available, serves as the foundation for many of today's microprogramming software products.) Fields in the assembly-language source program exactly corresponded to bit groups within the microword, and each line of microprogram source code had to define every field in the corresponding microword.

These initial meta-assemblers did allow default field values. However, you used an empty space between field-delimiting commas to denote use of that default. Experienced microcoders frequently talk about "comma counting," referring to the painstaking process of placing the proper values in the correct field positions.

Because these early microprogram meta-assemblers created syntaxes that closely resembled the processor's architecture, hardware designers favored them for programming. Microtec's Meta29 evolved from these early meta-assemblers. The current version of this product includes improved features, including programming macros and, optionally, relocatable-code generation.

Meta29's definition program accommodates 256-bit microwords; constant, variable, and don't-care fields; default field values; and error management through illegal-value definitions for fields. The product's assembler generates relocatable modules or absolute microcode and is a superset of Amdasm. Linker and PROM-formatting programs round out the package. Meta29M, the macro-assembler, costs $1400 for MS-DOS-based machines and $2500 for minicomputer hosts. The relocatable macro-assembler Meta29R costs $1800 for MS-DOS hosts and $3000 for minicomputer hosts (these and subsequent prices for development tools are for single quantities).

Getting rid of comma counting

As microprograms grew larger and more ambitious, software engineers supplanted hardware engineers as microprogrammers, and demand grew for higher-level programming tools that matched or at least resembled software tools available for FIS μP program development. In particular, the comma counting had to go if microcoding productivity was to improve.

Several meta-assemblers that offer these higher-level features are available. Microtec's mcASM supports macros and relocatable code (as does Meta29), plus nonpositional keyword syntax, variable field formats through a case statement, microcode overlays, and mnemonic definitions localized to a field. The mcASM structured macro assembler costs $2500 for MS-DOS hosts and $5000 for the minicomputer version.

Nonpositional keyword syntax eliminates comma counting; you can define one microword using several source lines without regard to field order. You need variable field formats if some of your microword's field definitions change as a function of another field's value. (The AMD 29116 is often cited as an example of a microprogrammable part with variable instruction fields.) Microcode overlays allow you to create microprograms that are larger than the microcode memory available in the target system. With mcASM, you can create a core microprogram that's always resident and one or more overlays that are loaded as required.

Localizing mnemonics to a microword field allows one mnemonic to represent different bit values when it's used in different fields. As an example, your hardware architecture may include an ALU and an address generator that both have instructions for addition. The localized mnemonic ADD could then represent one bit pattern for the ALU instruction and a different pattern for the address generator. You do not have to make mnemonics identical.

Microcode developers also sought symbolic debugging, but this feature requires the close association of the software tools with hardware-development stations. Three manufacturers that offer such a combination are Step Engineering, Hilevel Technology, and Hewlett-Packard (HP). Step Engineering's development tools include the MetaStep language system and the Step-40 SDT microprogram development station. The company offers versions of MetaStep for the IBM PC and the VAX (running Unix or VMS) for $3000. The language includes a definition processor, a meta-assembler, a linker, and a translator to convert source code written in Amdasm to MetaStep's syntax.

MetaStep's definition processor accommodates 1024-bit-wide microwords, and field definitions can encompass noncontiguous groups of bits. Case definitions handle variable field formats. The definition processor also supports pipelined architectures; you can define pipeline delays through definition directives. An exten-

The comma counting had to go if microcoding productivity was to improve.

sive constraint-management feature lets you define allowable (and disallowed) values for fields within a microword, for a whole microword, across microwords (sequential constraints), or for a case-statement branch through check-descriptor macros.

Step provides an example of such a check-descriptor macro in its product description manual. The example illustrates a macro that counts the number of bus drivers enabled in a microword for a system built from the TI 74AS888 ALU and 74AS890 microsequencer. The macro, called "bumpDrivers," increments a counter for each of four bus drivers enabled in a microword. At the end of the macro, if the counter value exceeds 1, signifying a bus-driver conflict, the macro causes an error to print out. Your software can call this macro to check each line of source code.

MetaStep's relocatable macro meta-assembler, like its definition processor, allows you to create high-level program structures through case statements and macros. Using these statements, you can create your own programming language tailored to your processor's architecture. The assembler generates the files required by the company's Step-40 SDT development station for symbolic debugging and patching.

A basic Step-40 SDT costs $20,000; the price increases as you add capability to the base system. The product's chassis accepts six cards from a mix of writable-control-store (WCS) modules, logic-analyzer cards, and emulation boards, and you can add additional chassis for more card-slot capacity. Each WCS module

Manufacturers of microprogrammable and microprogramming products

For more information on microprogrammable ICs and microprogram development systems, circle the appropriate numbers on the Information Retrieval Service card or contact the following manufacturers directly.

Advanced Micro Devices Inc
Box 3453
Sunnyvale, CA 94088
Phone (408) 732-2400
TWX 910-339-9280
TLX 346306
Circle No 650

Analog Devices Inc
Box 280
Norwood, MA 02062
Phone (617) 329-4700
TWX 710-394-6577
Circle No 651

Bipolar Integrated Technology Inc
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Beaverton, OR 97006
Phone (503) 629-5490
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California Devices Inc
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Milpitas, CA 95035
Phone (408) 945-5000
Circle No 653

Cypress Semiconductor Corp
3901 N First St
San Jose, CA 95134
Phone (408) 943-2600
TWX 910-997-0753
TLX 821032
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Gould Inc
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3800 Homestead Rd
Santa Clara CA 95051
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TWX 910-338-0018
Circle No 655

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Phone local office
Circle No 656

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18902 Bardeen Way
Irvine, CA 92715
Phone (714) 752-5215
TLX 655316
Circle No 657

Integrated Device Technology Inc
3236 Scott Blvd
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TWX 910-338-2070
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Integrated Logic Systems Inc
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Colorado Springs, CO 80907
Phone (303) 590-1588
Circle No 659

International Microcircuits Inc
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TWX 910-338-2032
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TLX 172387
Circle No 661

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Phone (408) 733-7837
TWX 910-339-9506
Circle No 665

Texas Instruments Inc
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Phone (800) 232-3200
Circle No 666

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78140 Velizy-Villacoublay, France
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Circle No 667

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Phone (408) 433-3388
Circle No 668

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TWX 510-601-4639
Circle No 669

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Phone (612) 851-5200
TLX 857113
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47280 Kato Rd
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Phone (415) 656-5400
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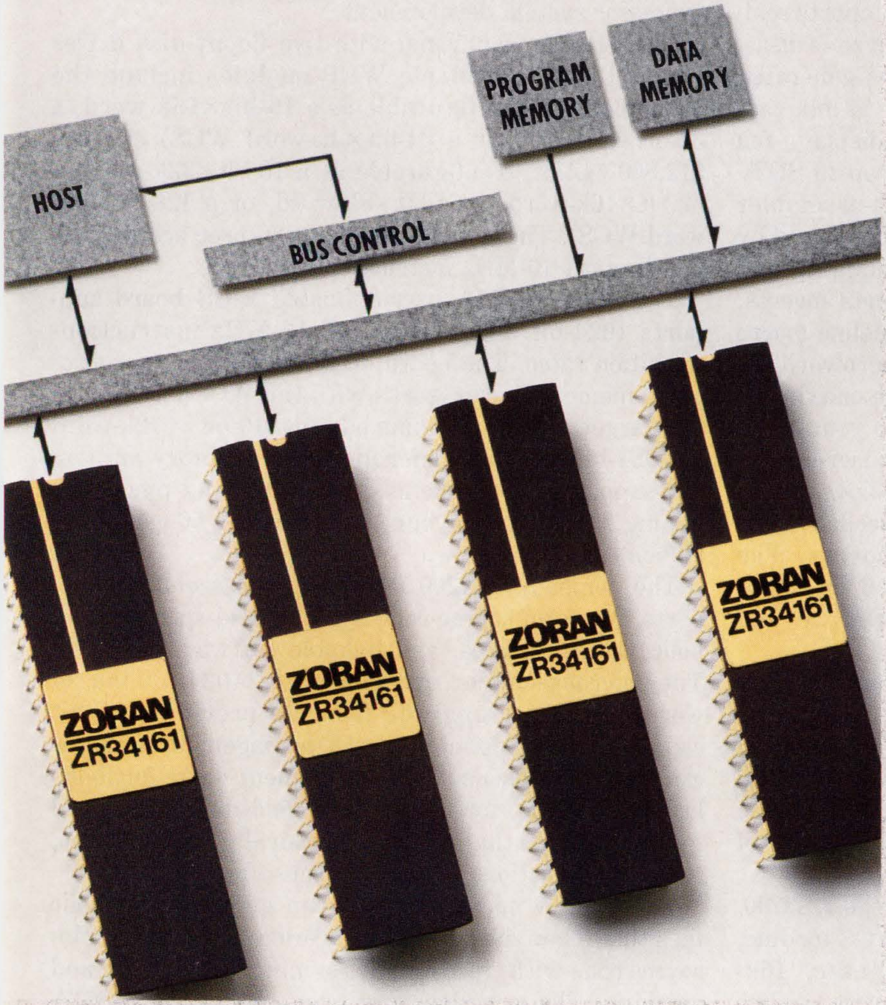

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Symbolic debugging requires the close association of the software tools with hardware-development stations.

contains 1k-word×64-bit emulation memory with a 10-nsec access time. Step advises that cable delays from the WCS card to the target system add an average of 15 nsec to that access-time rating.

The Step-40 SDT's logic-state analyzer supports real-time, 3-way trigger branching, and the analyzer's disassembly software links to the symbolic files generated by the MetaStep assembler, allowing you to mix captured logic states and source code on the display. You need an IBM PC/AT or RT PC to run a Step-40 SDT.

Hale 1.1, an Amdasm-compatible meta-assembler from Hilevel Technology, creates symbolic files used by the company's DS3700 Emulyzer for debugging and code patching. The meta-assembler supports macros, which you can nest to 15 levels. A special pipeline-macro feature allows you to define multiple microword sequences that can be overlapped to take maximum advantage of the parallelism designed into your hardware's architecture. Hale 1.1 also supports user-definable warning and error conditions that allow you to detect constraint violations and catch uncoded cases within "if . . . then . . . else . . ." statements. The product supports microword widths to 256 bits. The relocatable version costs $2300 for the IBM PC and $3500 for VAX, Sun, and Apollo computers.

The $8950 DS3700 Emulyzer mainframe accepts 16-bit WCS modules and trace cards for its integral logic analyzer. The DS3700 chassis accommodates 128 bits of WCS and 80 bits of trace-capture memory for the logic analyzer. A $2950 expansion chassis, the EXP3700, adds capacity for an additional 256 bits of WCS.

Hilevel offers several WCS modules for the DS3700. The E1K-10, a 25-nsec, 1k-word×16-bit WCS module, costs $1750, and the E16KW-15, a 30-nsec, 16k-word×16-bit WCS module, costs $4200. The access time is rated from the target side of the WCS memory pod. You can gang WCS modules to achieve microword emulation to 512-bit widths and 64k-word depths. Sixteen-bit trace modules cost $2500 for 25-MHz capture and $3500 for 50-MHz capture. You control the DS3700 over a serial port using a terminal, a PC, or some other host computer.

Emulates multiple processors in circuit

Hewlett-Packard's 64100A μP development system supports microprogram development through its $7000 64276A run-control module, a variety of WCS modules, and the 64320S 25-MHz logic-state analyzer. The logic-state analyzer with 30-, 60-, or 90-channel options costs $6250, $9750, and $13,250, respectively. A key feature of the 64100 is its ability to run in-circuit emulation for more than one processor at a time. Consequently, you can operate one or more FIS μP emulation pods in tandem with the microprogrammable WCS for multiprocessor system development.

The 64100A mainframe with two floppy-disk drives costs $13,330. Available WCS modules include the $9900 64276B (configurable as a 16-bit×16k-word, a 32-bit×8k-word, or a 64-bit×4k-word WCS) and the $12,800 64276C (configurable as a 16-bit×32k-word, a 32-bit×16k-word, a 64-bit×8k-word, or a 128-bit×4k-word WCS). These modules spec a 50-nsec access time and support 10-MHz instruction rates.

The $1400 64277A user-definable WCS board supports 1024-bit microwords and 13-MHz instruction-execution rates. The board does not contain microprogram memory, but it works with the WCS installed in the target system, accommodating 16-bit×512k-word to 1024-bit×8k-word microprogram memory arrays. HP supplies a recommended connector and pinout for linking its 65861A to your system with a 50-conductor ribbon cable.

The company's $1200 64861A microassembler supports free-form source-code syntax, field-specific symbolic values, macros, and linkable software modules. The microassembler accommodates 1024-bit microwords—a recent upgrade from its previous 128-bit capability. User-definable error-management features can catch the absence of an assignment value for fields lacking defaults, for overlapping field definitions, and for microwords that are architecturally inconsistent, such as instructions that would cause bus contention.

The 64861A microassembler can generate symbolic files that allow the 64230S to interleave microprogram source code with trace data for symbolic debugging and patching. The company offers versions of the 64861A that run on the 64100A mainframe and on HP9000 Series workstations. **EDN**

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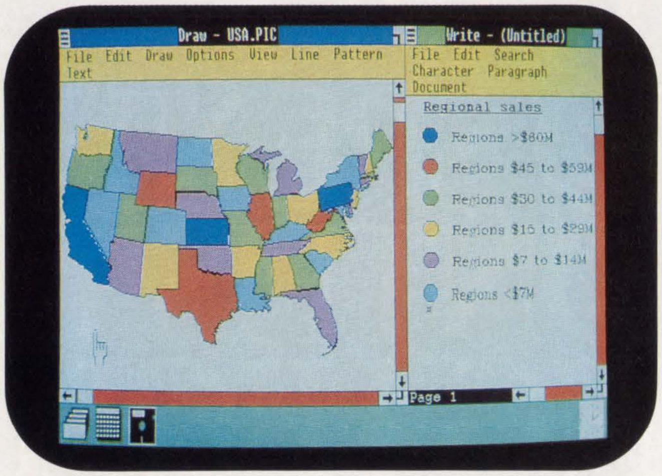

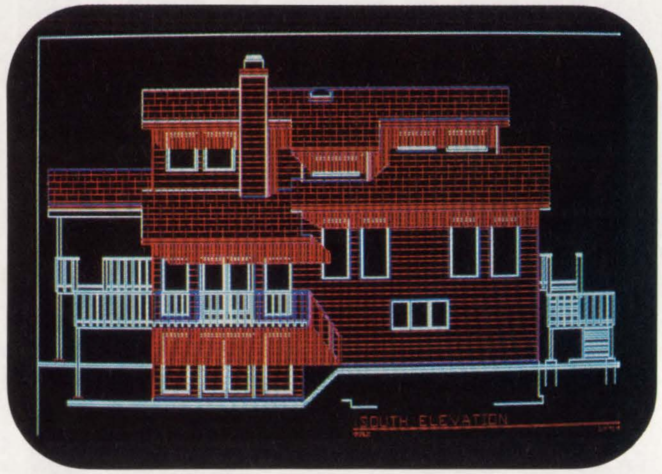

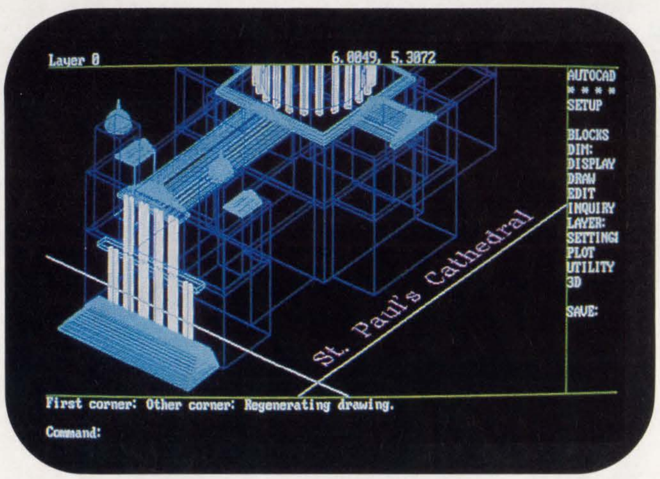

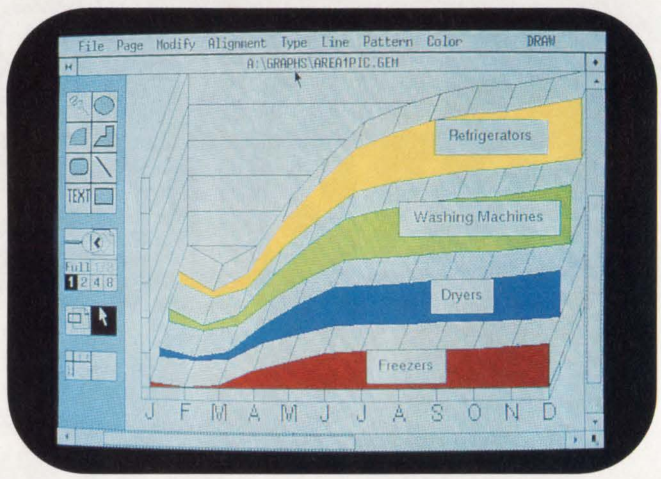

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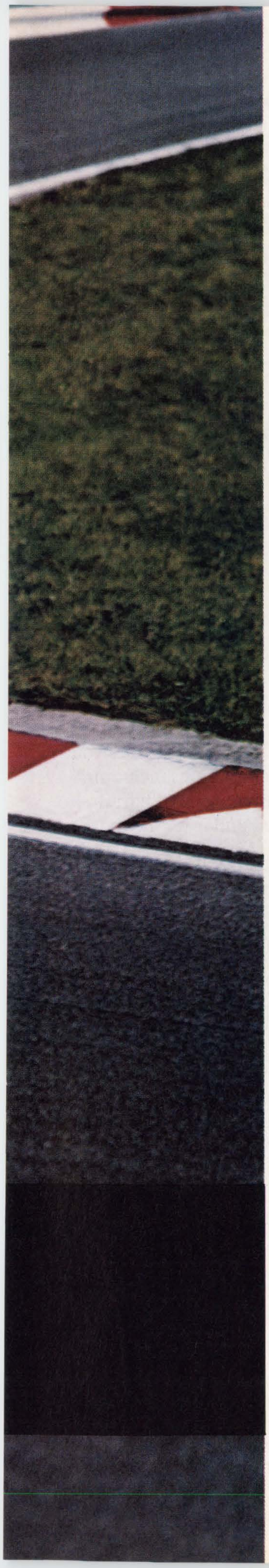

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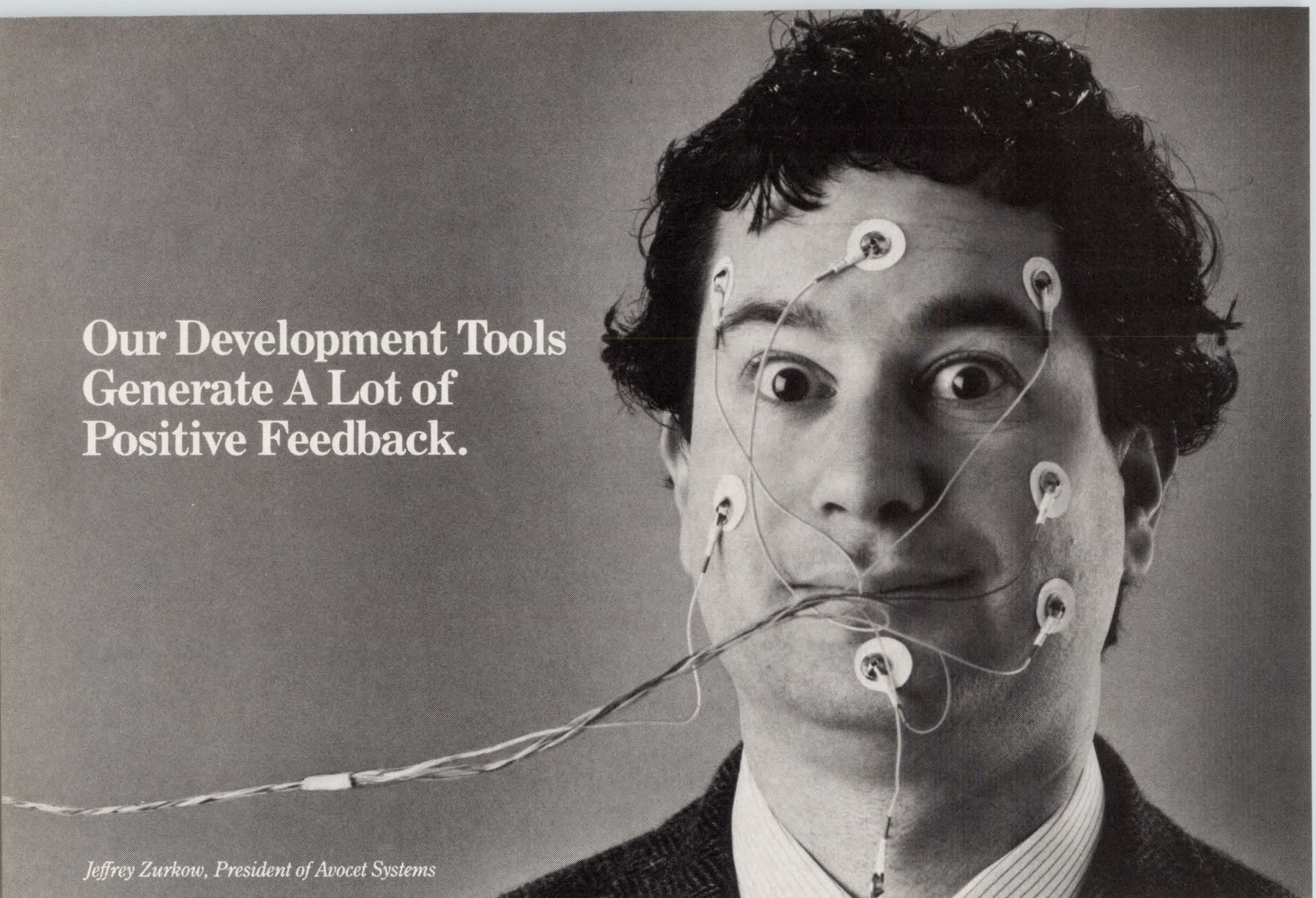

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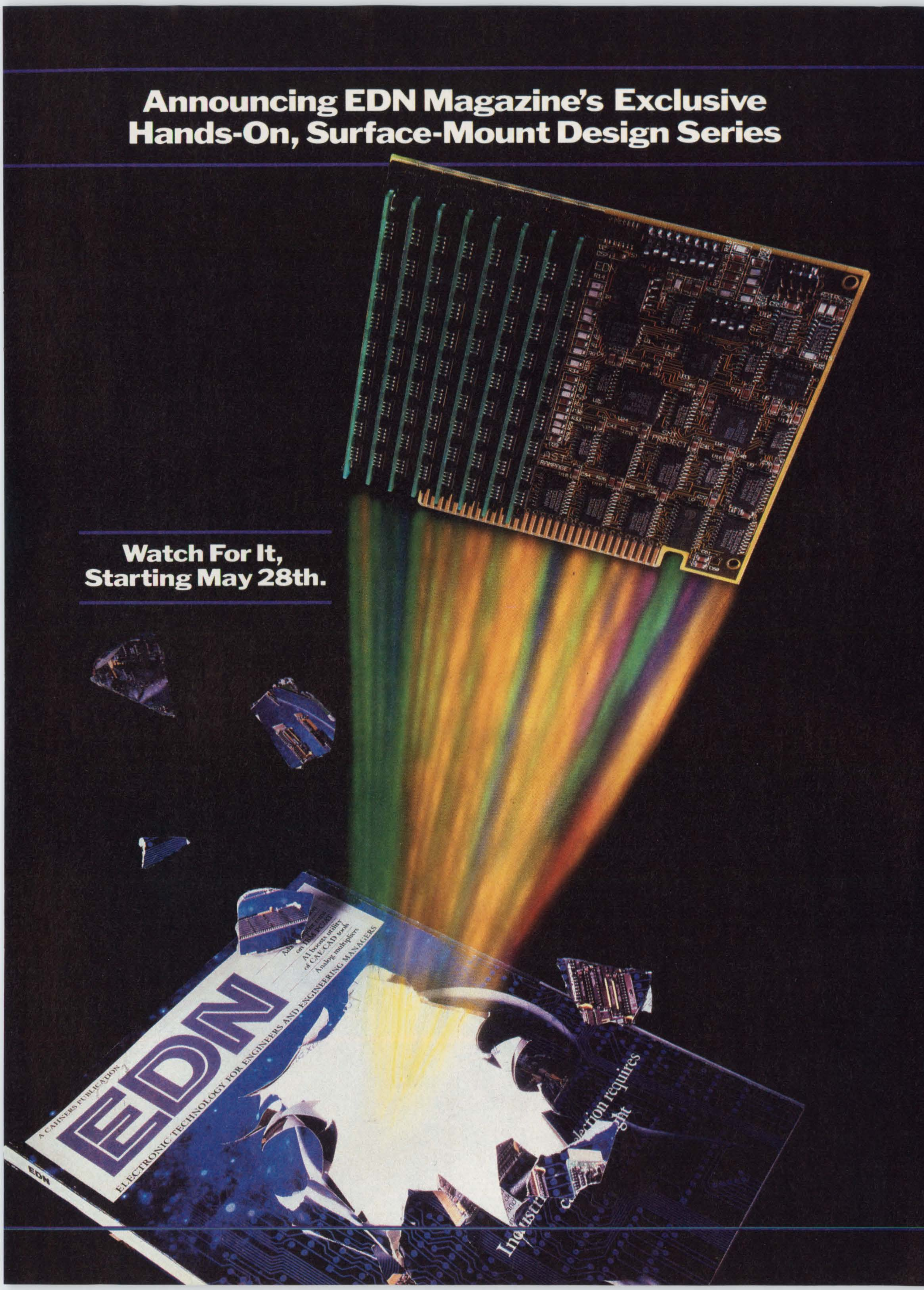
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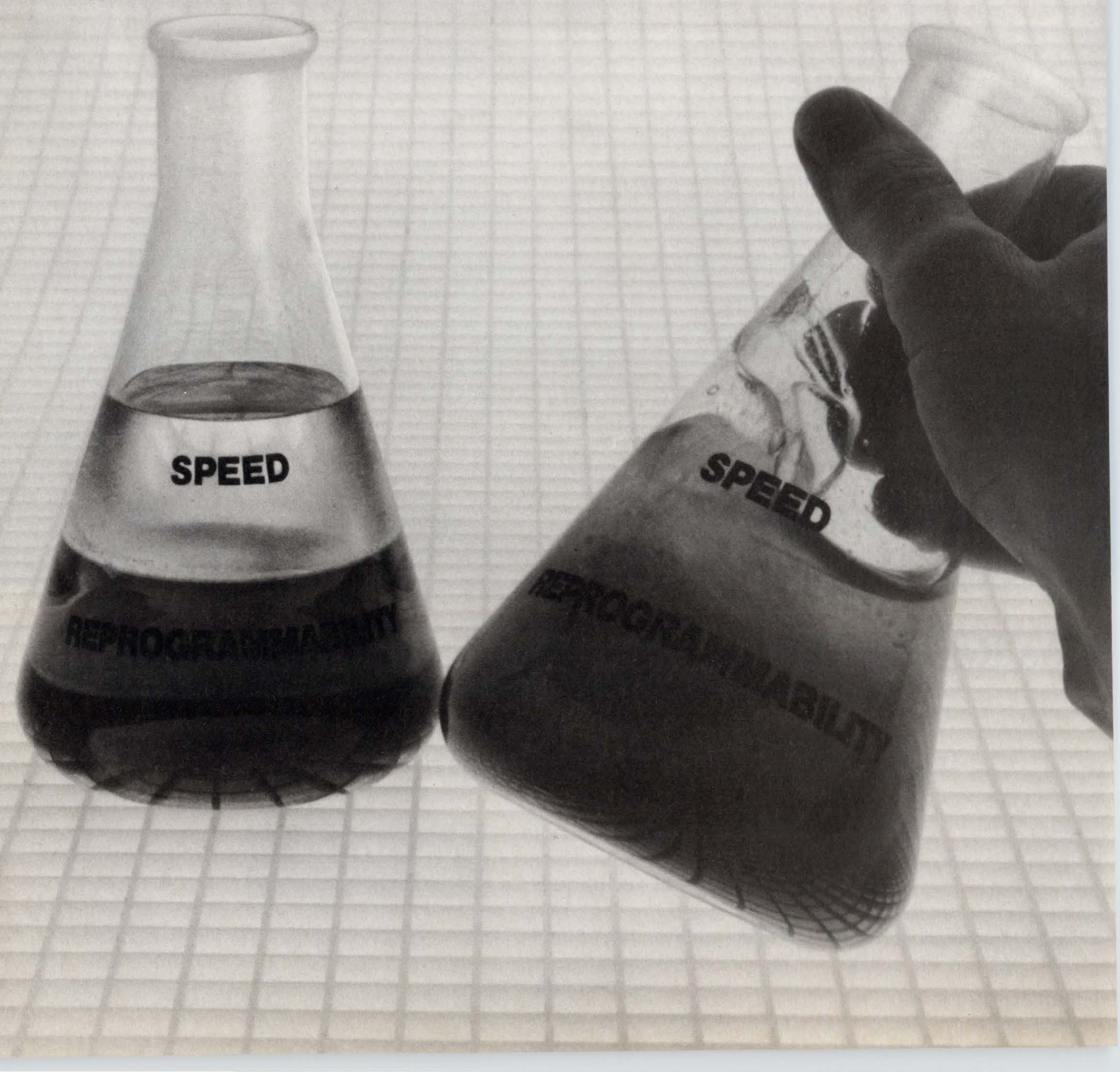

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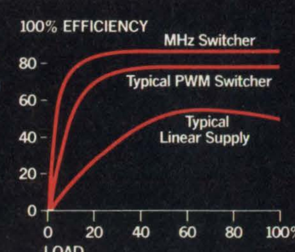

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Use structured arrays for high-performance data processing

Using one structured array and nine support ICs, you can design a 15-MHz peripheral controller. A structured array combines high-level functions, such as ROM, RAM, and ALUs, along with a gate array on a single chip.

Yen Chang and Alex Yuen, *LSI Logic Corp*

System designers have used gate arrays to implement complex logic circuitry for several years. As device geometries have shrunk and other design improvements have occurred, gate-array manufacturers have been able to pack increasing numbers of gates onto one chip. System designers, though, encounter situations where 20,000 gates provide more than enough logic circuitry. If you could substitute memory for some of that logic, then you could implement your design on a single chip.

The advantages of having all your circuitry on one chip include reduced board space requirements and component count as well as greater reliability due to a reduction in system interconnections. If all of your critical path signals can be handled "on chip," an additional improvement in circuit performance results because the signal doesn't encounter delays external to the chip. The following design example illustrates how to implement a high-speed processor using a structured-array device such as the LSA2002 (see **box**, "Structured array incorporates RAM and gate array").

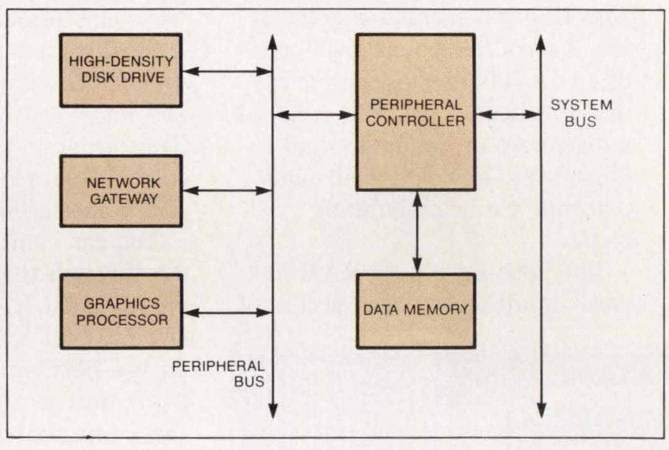


***Fig 1—This block diagram depicts the architecture** of the system that employs the peripheral controller. The controller receives commands and data from the host processor and then responds with status and data.*

In this case, the processor serves as a peripheral controller in a system that includes such devices as a high-density disk drive, a network gateway, and a graphics processor. The controller relieves the system processor of peripheral-control duties, thus allowing it to devote its resources to more computational-intensive tasks.

In the system-level diagram **(Fig 1,)** the peripherals connect to the controller via a high-speed parallel

The advantages of having all your circuitry on one chip include reduced board space requirements and component count.

peripheral bus. This bus performs error detection and correction as well as data and instruction transfers. The controller also connects to the system bus, over which it receives commands and data from the host processor and then responds with status and data. The peripheral controller stores data in a cache to improve response time. Its main responsibilities are to execute system commands, implement the data transfer protocol for each peripheral, and manage data memory.

The processor uses a RISC architecture, which because of its less complex instructions allows it to operate at higher execution speeds than a CISC (complex instruction set computer) architecture would. In addition, systems based on RISC architectures result in shorter design cycles because of the instruction set's simplicity and the concomitant simplicity of the control section. This simplicity also translates into a smaller number of components, thus increasing system reliability.

In the architecture-level block diagram of **Fig 2**, the controller comprises five modules: the processor module, the control module, the peripheral-interface module, the system-interface module, and the memory-interface module. The RISC architecture has a direct effect upon the processor and control sections of the controller.

The processor module uses the 3-port memory as the register file. This memory, with its high speed and single-cycle read-modify-write capability, is well suited to a register-file application. The file is arranged as 64 words of 32 bits with byte parity. The 32-bit ALU uses 718 gates of the on-chip gate array and operates with a

Structured array incorporates RAM and gate array

The LSA2002 combines a 2304-bit, 3-port RAM with 6000 gates of an LL7000 Series gate array in a single package. **Fig A** shows a die photo of the device and illustrates the relative size and placement of each building block.

The 2304-bit 3-port RAM allows simultaneous read access of two registers and write access of a third register. The register written to may even be one of the registers that's read from. This situation allows you to perform a 2-source read-modify-write operation.

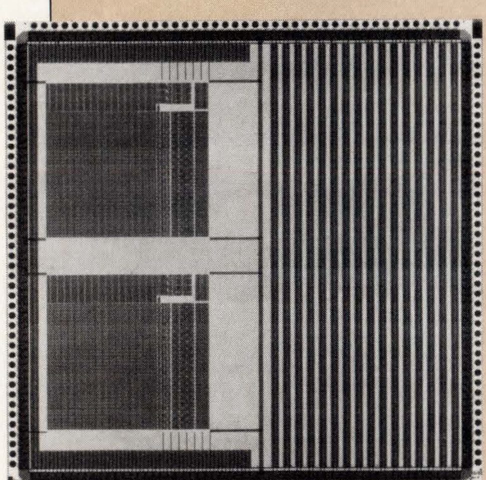


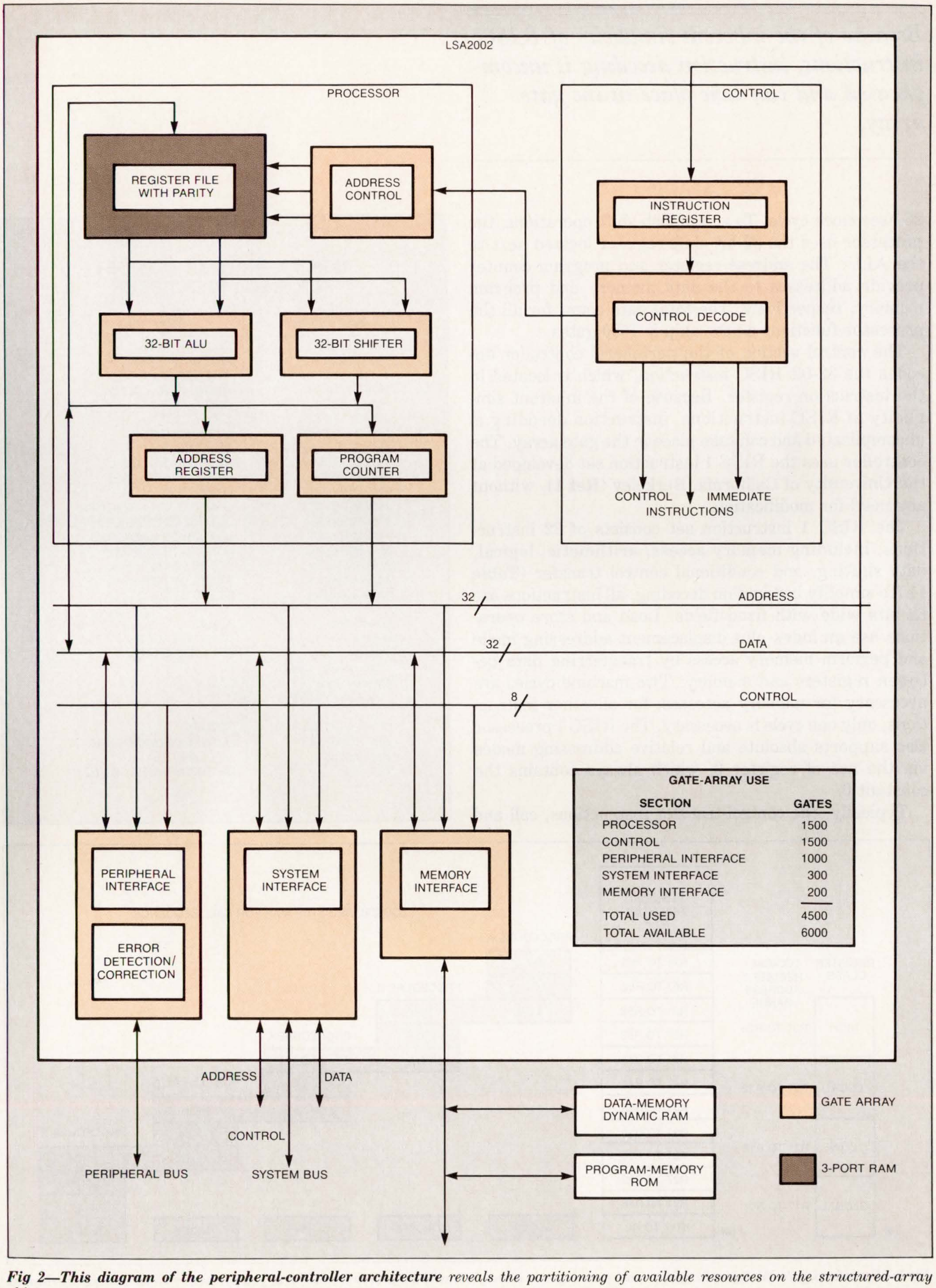
Fig A—This die photo of the LSA2002 structured array *shows the relative size and placement of each building block. The gate array is on the right, and the two 3-port RAMs are on the left.*

You can configure the memory, through the metallization, as one 2304-bit RAM or split it into two 1152-bit RAMs. You can also choose between word widths of 9, 18, and 36 bits. The RAM features input latches, output latches, and address latches to simplify timing requirements, and it presents a byte-wide interface to external circuitry.

You can use the 6000-gate array to tailor the LSA2002 to your specific application requirements; it's compatible with LL7000 Series macrocells' macrofunctions and megafunctions. These predefined functions include circuits of complexity ranging from a 2-input NAND gate to a 16×16-bit multiplier. **Table A** lists some of the functions available and the associated gate count for each of them.

TABLE A—LARGE-SCALE-FUNCTION REQUIREMENTS

FUNCTION	GATES
16-BIT ALU (74181 TYPE)	363
4-BIT RALU (2901 TYPE)	720
32-BIT 3-PORT ADDER	809
12-BIT SEQUENCER (2910 TYPE)	856
UART (6850 TYPE)	1000
MEMORY CONTROLLER (2964 TYPE)	311
32-BIT COMPARATOR	348
8×8-BIT MULTIPLIER	517
4-BIT RALU (2903 TYPE)	1215
4-BIT RALU (29203 TYPE)	1550
16×16-BIT MULTIPLIER	1796



GATE-ARRAY USE

SECTION	GATES
PROCESSOR	1500
CONTROL	1500
PERIPHERAL INTERFACE	1000
SYSTEM INTERFACE	300
MEMORY INTERFACE	200
TOTAL USED	4500
TOTAL AVAILABLE	6000

Fig 2—This diagram of the peripheral-controller architecture *reveals the partitioning of available resources on the structured-array chip.*

Because of the inherent simplicity of RISC instructions, instruction decoding is uncomplicated and can take place in the gate array.

25-nsec clock cycle. To accomplish shift operations, the processor uses the 32-bit shift register located next to the ALU. The address register and program counter provide addresses to the data memory and program memory, respectively. The total gate count for all the processor functions on the chip is 1500 gates.

The control section of the peripheral controller decodes the 32-bit RISC instruction, which is located in the instruction register. Because of the inherent simplicity of RISC instructions, instruction decoding is uncomplicated and can take place in the gate array. The controller uses the RISC 1 instruction set developed at the University of California, Berkeley (**Ref 1**), without any need for modification.

The RISC 1 instruction set consists of 32 instructions, including memory access, arithmetic, logical, data shifting, and conditional control transfer (**Table 1**). To simplify instruction decoding, all instructions are 32 bits wide with fixed fields. Load and store operations use an index-plus-displacement addressing mode and perform memory access by transferring data between registers and memory. Two machine cycles are necessary for memory accesses; for all other instructions, only one cycle is necessary. The RISC 1 processor also supports absolute and relative addressing modes via the use of register 0, which always contains the constant 0.

Typically, the control-transfer instructions, call and

TABLE 1—INSTRUCTION SET FOR RISC-1 PROCESSOR

INSTRUCTION	COMMENT
Rd=S1+S2	INTEGER ADD
Rd=S1+S2+c	ADD WITH CARRY
Rd=S1−S2	INTEGER SUBTRACT
Rd=S1−S2−c	MINUS WITH CARRY
Rd=S1&S2	AND
Rd=S1 OR S2	OR
Rd=S1 XOR S2	EXCLUSIVE OR
Rd=S1 shift by S2	SHIFT LEFT
Rd=S1 shift by S2	SHIFT RIGHT LOGIC
Rd=S1 shift by S2	SHIFT RIGHT ARITH
Rd=M[Rx+X]	LOAD LONG
Rd=M[Rx+X]	LOAD SHORT UNSIGNED
Rd=M[Rx+X]	LOAD SHORT SIGNED
Rd=M[Rx+X]	LOAD BYTE UNSIGNED
Rd=M[Rx+X]	LOAD BYTE SIGNED
M[Rx+X]=Rm	STORE LONG
M[Rx+X]=Rm	STORE SHORT
M[Rx+X]=Rm	STORE BYTE
pc=X+Rm	JUMP
pc=pc+Y	JUMP RELATIVE
Rm=pc; next, pc=X+Rn, CWP	CALL RELATIVE
Rm=pc; next, pc=pc+Y, CWP	CALL
pc=Rm+X, CWP++	RETURN
Rm<31:13>=Y	LOAD IMMEDIATE HIGH
Rm=last pc	GET LAST PC
Rm=inr	GET INTERRUPT NUMBER

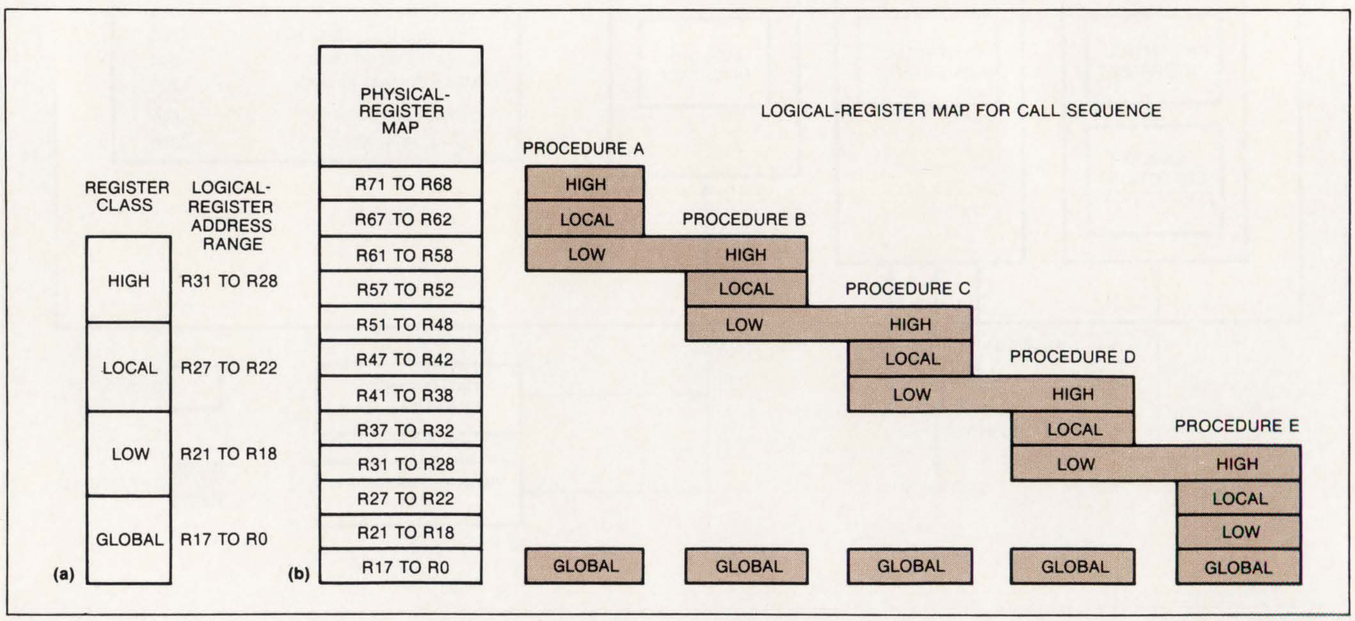


***Fig 3—By referring to the logical-register-address** ranges in **a** and following a 5-procedure call in **b**, you can understand how the overlapped register windows operate.*

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Typically, the control-transfer instructions, call and return, require several cycles for a processor to execute.

return, require several cycles for a processor to execute. When a processor executes a procedure call, it needs to store registers in memory and load input parameters into registers. At the end of the procedure, when it executes a return, the processor must load registers and output parameters into memory. To increase the speed of these control-transfer operations, many systems use a high-speed cache memory, which supports high-speed storage and retrieval of register contents and input parameters. The RISC 1, on the other hand, uses the concept of overlapped register windows to speed these operations.

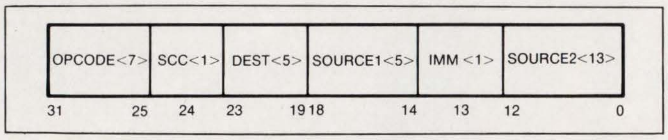
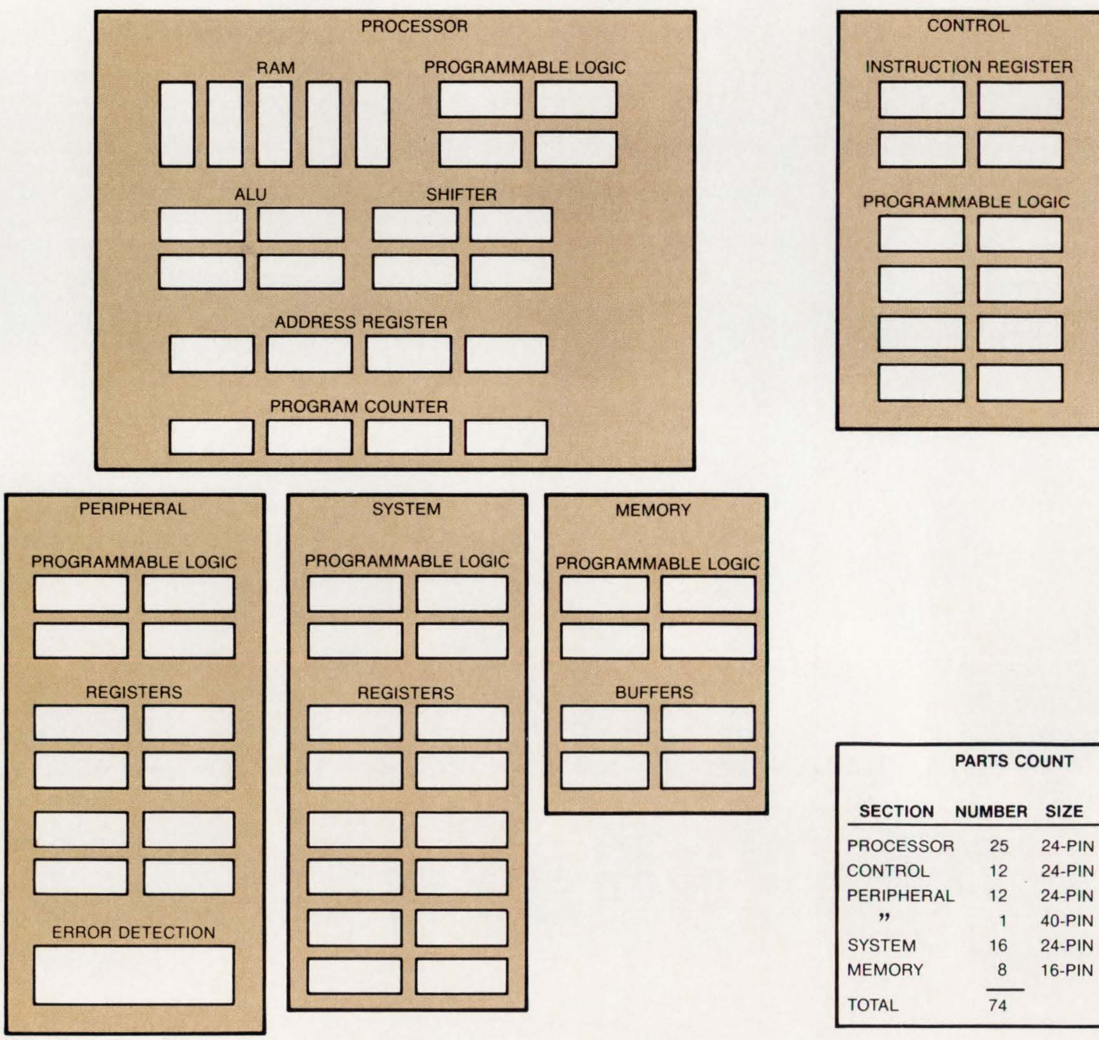


***Fig 4—The instruction format for RISC 1** is based on six fixed-length fields in the 32-bit instruction word.*

The RISC 1 processor can address a 32-register subset or "window" of the 72-physical-register set. Each window contains four classes of registers labeled high, local, low, and global. **Fig 3a** gives the logical-register address ranges for those classes. Each proce-



PARTS COUNT

SECTION	NUMBER	SIZE	POWER
PROCESSOR	25	24-PIN	17W
CONTROL	12	24-PIN	9W
PERIPHERAL	12	24-PIN	8W
"	1	40-PIN	5W
SYSTEM	16	24-PIN	10W
MEMORY	8	16-PIN	6W
TOTAL	74		55W

***Fig 5—In contrast with the peripheral controller** in **Fig 2,** which resides on one chip, the same controller implemented with standard products requires 74 devices.*

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With register overlap, it's not necessary to move parameters on call and return instructions.

dure call **(Fig 3b)** allocates a new window, and a procedure return restores the previous window.

In each window, the high registers, R31 to R28, contain the parameters passed by the calling procedure. The local registers, R27 to R22, contain variables used internal to the procedure. The low registers, R21 to R18, are used for local storage and contain variables passed to the procedure below the current procedure. These registers overlap; that is, both the calling and the called procedures use them.

Because of this overlap, it's not necessary to move parameters on call and return instructions; the correct values appear in the proper section of the window automatically. Referring back to **Fig 3b,** procedure A operates with variables intended for procedure B stored in its low registers. When procedure B is called, the window "slides" so that R61 to R58 are now mapped into the high registers, input registers, for procedure B. The global registers, R17 to R0, contain values common to all procedures. Registers 7 to 0 contain the most commonly used 32-bit constants and need not use the 3-port memory; they can be simple latches contructed from the on-chip gate array.

In the design of this peripheral controller, the number of registers allocated to each window section is different from the RISC 1 architecture. In anticipation of the controller requiring more global variables and less high, local, and low variables than a traditional CPU, the register allocation reflects this expected usage.

The memory-interface module, system-interface module, and peripheral-interface module of the controller provide the communication paths between the processor and the rest of the system. The peripheral-interface module uses error-detection and -correction logic to improve its reliability: It is the most error-prone of the interfaces. The memory-interface and system-interface modules employ parity generation and checking to enhance reliability.

In the 32-bit instruction format **(Fig 4,)** the first seven bits of the instruction always specifies the operation code. The next bit, SCC, determines whether or not the condition code bits are set by the instruction. The Dest field determines the destination register, and the Source1 and Source2 fields determine the two source registers. If the IMM field contains a 0, the low-order five bits of the Source2 field specify a register (one of the 32 which can be accessed in each window). If the IMM field contains a 1, the 13-bit Source2 field contains an immediate constant. Load and store operations use the Source1 field to specify the index register and the Source2 field to specify the offset.

The entire peripheral controller comprises one structured logic array, one ROM, and eight RAMs. The processor can operate at 15 MHz, roughly a 50% increase in performance over a discrete design. At this speed, the structured array consumes 1.5W. The design uses 4500 of the 6000 gates available, and all of the 3-port RAM is put to work.

In comparison, **Fig 5** shows the same design implemented with standard ALUs, registerd PROMs, programmable logic, and octal registers and buffers. In addition to the memory required for data and program storage, this implementation requires more than 70 chips. It consumes 55W, about 35 times that of the structured-array-based design. **EDN**

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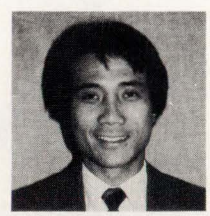
1. Patterson, David A, "RISC 1: A Reduced Instruction Set VLSI Computer," *Proceedings of the Eighth International Symposium on Computer Architecture*, May 1981, pg 443.

2. Patterson, David A, "Reduced Instruction Set Computers," *Communications of the ACM*, Vol 28, No 1 (January 1985), pg 8.

Authors' biographies



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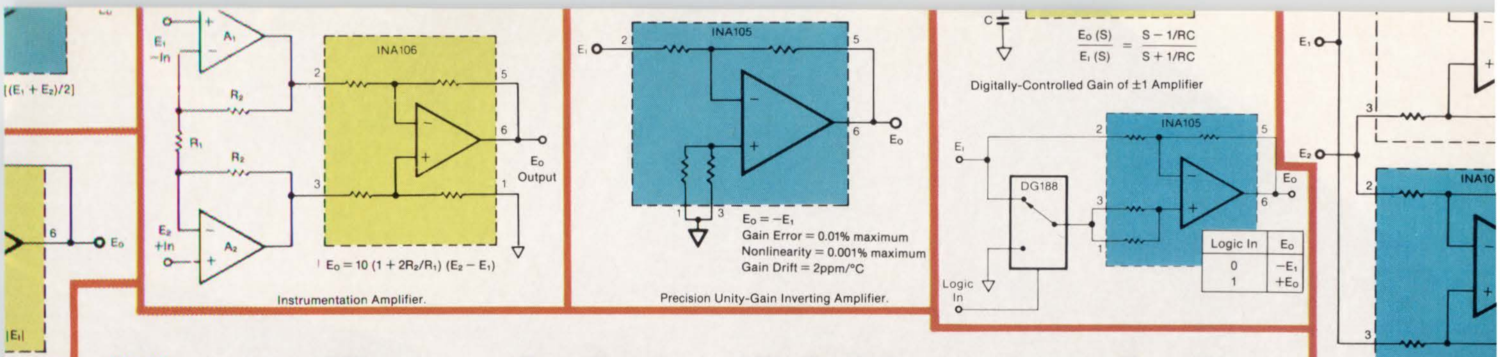

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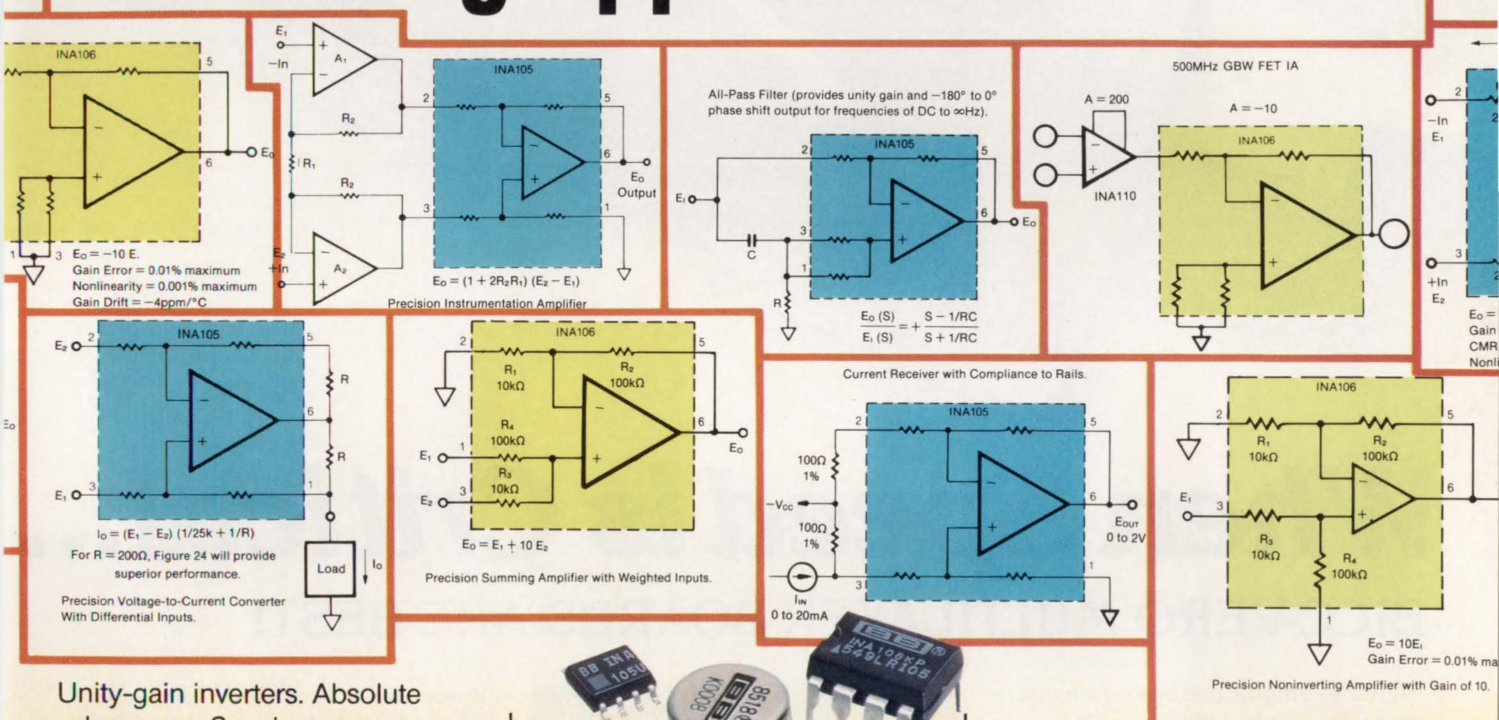

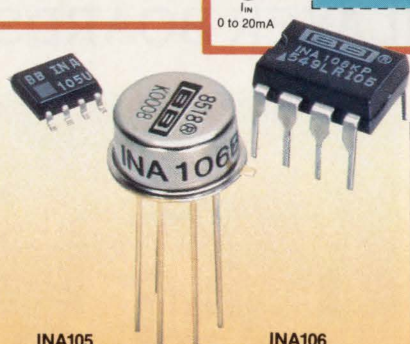

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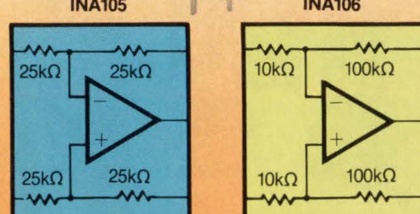

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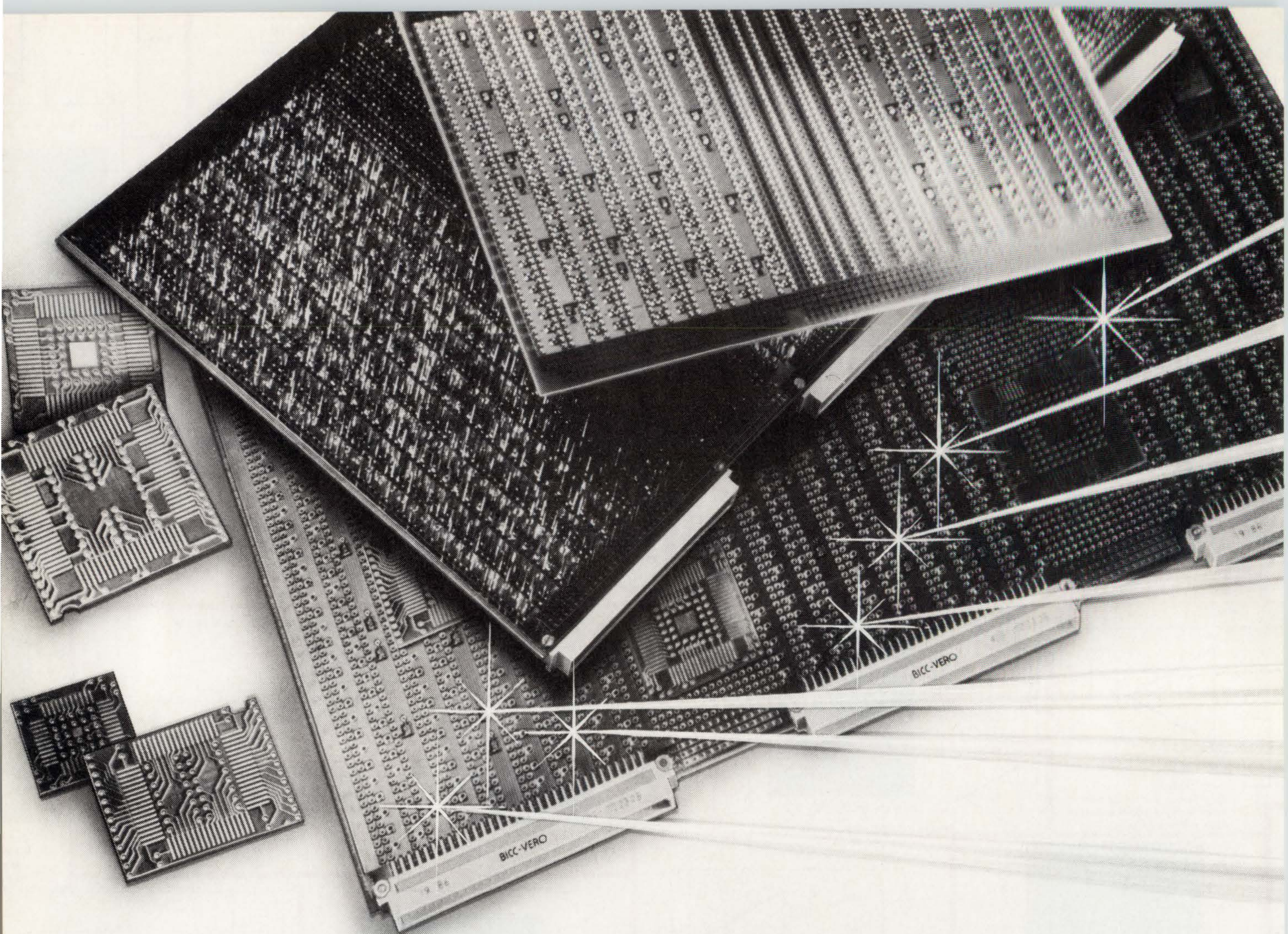

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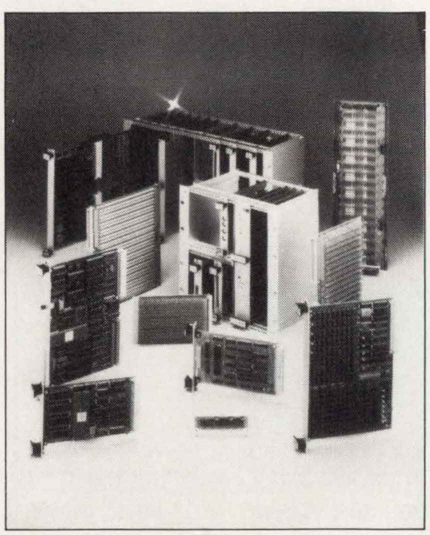

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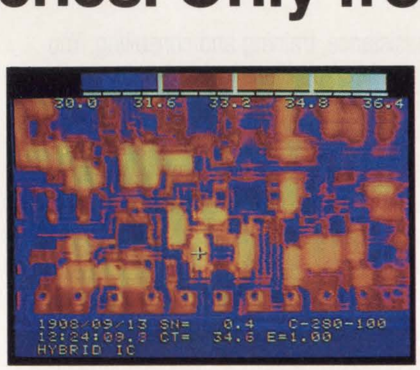

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Design-for-test techniques suit diverse applications

The four major design-for-test techniques—the ad hoc, built-in self-test (BIST), structured, and semistructured approaches—differ widely in their ability to meet a product's test needs. A few practical guidelines can help you choose the design-for-testability approach that's best for your project.

Robert D Hess, William C Berg Jr, and Gordon B Hoffman, *Caedent Corp*

Designing a product so as to make it easy to test is clearly a desirable goal—test costs contribute between 30 and 50% of the nonrecurring engineering cost of a product—but choosing among the various design-for-testability styles and techniques is not always easy. The four major techniques for designing for testability—the ad hoc, built-in self-test (BIST), structured, and semistructured techniques—are distinctly different in their ability to meet a product's various test-related requirements, so the techniques suit very different applications.

No single design-for-testability approach is best for all applications; a combination of several approaches might be the optimum solution in one case, and a single approach might be best in another situation. Furthermore, there's no right or wrong way to select a technique: The choice is often a company-wide business decision about how to spend money. But one thing is certain—if you don't address test issues early in the design process, they'll haunt you later.

In general, you'll want to choose a technique that allows you to keep the recurring costs of test-circuitry overhead to a minimum, yet lets you generate test vectors and parameters that accurately represent the product and adequately ensure its performance and functionality. The technique you choose should also let you generate test vectors that will form a reliable base for the test programs needed for manufacturing—programs that meet manufacturing requirements for tester throughput and the configuration of vectors.

A look at the four major approaches

Testability can be defined as the characteristic of a design that allows you to determine the design's status and the location of any faults within it confidently and in a timely and cost-effective manner. For the purposes of this article, this definition of testability refers to determining functional status and fault location rather than to detecting problems in the physical ac and dc parameters.

The most widely used design-for-testability technique today is the ad hoc approach. An ad hoc technique, as the name implies, is an unstructured one; it consists of inserting test points in your circuit as you design it. Ad hoc design-for-testability techniques involve designing with regard to initialization requirements, utilizing unused inputs and outputs as test points, partitioning designs to insert test points, adding test pins, breaking feedback loops with test points, adding clock control for testing, adding logic for testing long counters, and making partial use of scan circuitry (incomplete scan-path design).

Ad hoc approaches are especially useful for application-specific-IC design because they are a logical extension of common ASIC-design practices. Further, gate densities in ASICs have been low enough to make ad hoc approaches practical for ASIC design **(Ref 1)**.

Testability-analysis software, such as DFTA from Caedent, is an essential tool for the designer who uses the ad hoc approach (**Refs 2, 3,** and **4**). You can run such software on workstations and personal computers. Future refinements of the software will support other design-for-testability techniques, such as circuitry for scan support via the incomplete scan method.

Unlike ad hoc techniques, BIST techniques are highly structured. A BIST circuit is any circuit that generates its own testing signal and has a method for monitoring and reporting the response of the device to these stimuli. For example, a totally self-testing circuit might have scannable sequential storage elements and I/O, pseudorandom pattern generation, and an output response that's compressed by means of parallel or serial input-signature analysis.

The semistructured and structured approaches fall between these two extremes. Semistructured approaches (signature analysis, for example) rely heavily on planning done during the design stage to ensure that the product will operate properly at the pc-board level. Signature analysis is a data-compression technique borrowed from the telecommunications field (a cyclic redundancy check code, for instance, is a kind of signature analysis used in telecommunications). Signature analysis is best suited to bus-structured devices associated with microcomputers. The linear-feedback shift register is the key element of this approach.

As its name implies, the structured approach to design for testability is rigorous and requires a highly structured design style. It is based on the idea that if your design directly controls and observes all the sequential latches, you'll have reduced the problem to one of generating tests for combinational circuits. The structured technique includes many variations of scan approaches, in which you load test vectors into and read them out of the sequential latches in order to control and observe the vectors. (For detailed information on structured, semistructured, and BIST approaches, see **Refs 1** and 5).

IC designers who design for testability generally choose either ad hoc or BIST techniques. The ad hoc approaches, coupled with good training and software tools, are adequate for the majority of designs. For military applications, however, BIST techniques are often better, because they facilitate field testing of chips. BIST techniques also allow for lower nonrecurring design costs and lower unit-manufacturing costs.

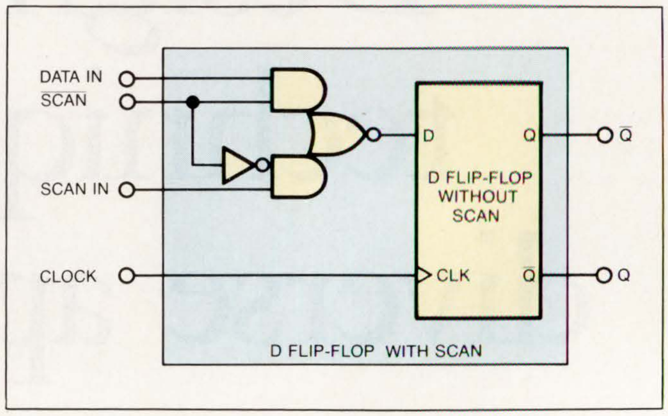

Fig 1—When you use the structured technique, your circuit overhead increases *in proportion to the number of gates required to implement the scan capability within a sequential device. For example, it might take three or four extra gates to perform the scan function for a D-type flip-flop.*

The highly structured BIST approach is also likely to emerge as the dominant technique for use in nonmilitary applications involving high gate counts (10,000 to 20,000). The more complex a circuit is, the more system maintenance it requires, so the better suited it is to using BIST techniques.

Semistructured and structured approaches are not likely to gain wide acceptance, even as more and more circuits appear that have gate counts approaching 10,000. In any case, the average size of modern circuits, including ASIC devices, is still well under 10,000 gates. Except for a few large-system manufacturers, neither manufacturers in the commercial/industrial markets nor those in the military markets have embraced the semistructured and structured techniques.

Some scan techniques will be popular, but these techniques will be less complete or rigorous than a fully structured approach is. Incomplete scan-path design, for example, in which the number of sequential devices scanned does not include all such elements on the chip, will allow you to scan difficult-to-test sections of a circuit while testing other portions of the circuit conventionally.

To evaluate each of the four major design-for-testability techniques, you can use eight criteria: silicon overhead; effect on performance; effect on yield; design privacy; accommodation of engineering changes; extendability from component to board to system testing; test type; and the cost of the design, production, and maintenance phases.

An ad hoc technique is an unstructured one; it consists of inserting test points in your circuit as you design it.

The silicon overhead incurred by the semistructured approach, for instance, depends primarily on the size of the signature-analysis register and not on the size of the overall circuit. The semistructured approach requires you to add only the signature-analysis register, making few circuit modifications. Unlike SCAN and BIST techniques, it doesn't require you to make any major circuit modifications.

The structured technique increases the silicon overhead in proportion to the number of extra gates required to implement the scan capability within each sequential device in the design. Usually, this technique also requires four or five extra I/O pins to support the test function. This technique typically requires 10 to 20% circuit overhead. For example, it might take three or four additional gates to perform the scan function for a D-type flip-flop **(Fig 1).**

The BIST technique is the most costly in terms of overhead; it typically requires between 30 and 50% of the total area of a circuit. Like the structured technique, the BIST approach requires additional I/O ports and sequential-element modifications. However, the percentage of circuit overhead required by the BIST circuitry decreases as you increase the size of the circuit or as you remove some of the BIST capability. **Fig 2** shows the worst-case overhead for a completely self-testing BIST circuit.

The effect of test techniques on performance

When you use the ad hoc testing approach, the amount of degradation of your circuit's performance depends on how well you design for testability, but it is small in any case. The semistructured technique also has little or no effect on circuit delays or speed. The effects that the structured and BIST methods have on a circuit's performance depend completely on the type of sequential devices you use in the design. For example, the logic added to perform a scan function for D-type latches in 3-μm CMOS typically exacts a 2-nsec delay. To ensure that the circuit's performance will still be acceptable during normal circuit operation, therefore, you must re-evaluate the circuit's critical paths to include this delay.

The different approaches also have different effects on the costs your design incurs. In general, the costs incurred in the design phase include expenses for personnel and for the CPU time used during the development of the test patterns. If you fault-grade your test patterns, you'll need even more CPU time. The expenses incurred in the production phase include the cost of using automatic test equipment for wafer probing and final testing. The expenses you incur after shipping the product result from the product's reliability, the number of faulty systems shipped, and the ease of field diagnosis and repair.

When you use the ad hoc technique, whatever extra costs you incur depend entirely on how well you design for testability. Note, however, that when you use the ad hoc technique of deriving test patterns for your circuit from the logic simulation, such patterns either may not cover the circuit adequately or may cover it redundantly. If your test patterns are inadequate or redundant, the costs may be high. Further, it's very difficult to use automatic-test-generation (ATG) software effectively with ad hoc techniques, because ATG software does not comprehend typical sequential circuits very well.

If you can't use ATG software, you must perform a deterministic fault simulation on your circuit. Deterministic fault grading can be impractical because it requires a lot of CPU time. Specialized hardware engines can alleviate this problem; however, most designers would find an approximation technique for fault grading more practical as a complement to software and hardware fault simulators **(Ref 6).**

When you use the semistructured technique, you must spend some CPU time on engineering and simulation so that you can develop test patterns and determine a good signature. However, the result is excellent test quality. If you wish, you can use fault simulation to further ensure test quality, but doing so will require a

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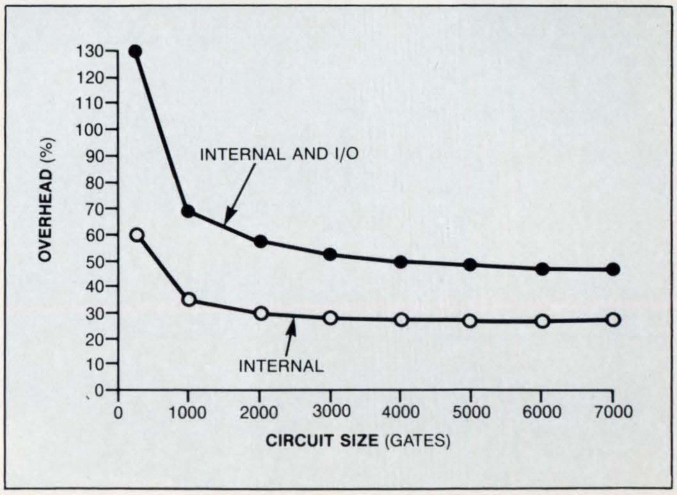

***Fig 2—Although BIST techniques require more silicon overhead** than do the other design-for-testability techniques, the percentage of circuit overhead required by the BIST circuitry decreases as you increase the size of the circuit.*

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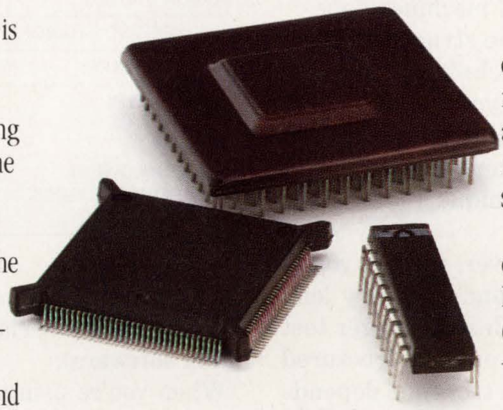

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lot of extra CPU time. The production test equipment used with this technique (for example, signature-analyzer instrumentation) is often less complex than are general-purpose ATE machines, and it requires simpler pattern-storage capability than ATE machines do.

You can use ATG software with the structured technique, however. The structured technique produces high overall test quality, because you partition the circuit into combinational elements. Because it theoretically provides 100% fault coverage and eliminates the need for fault simulation, this technique reduces the cost of test-pattern development.

The structured method does, however, require you to use production ATE that can store and test very long serial patterns. These long patterns lead to longer test times than those incurred by ad hoc or semistructured techniques. The technique's effect on test time depends on the circuit's size, pattern generation, and the length of the vector strings.

The BIST technique both produces excellent test quality and completely eliminates traditional test-pattern-development costs. You have to simulate the chip's patterns to establish a good signature. The larger the signature-analysis register, the higher the probability of catching faults. This method requires a large number of test patterns, so you'll find it very expensive to grade the faults in order to establish the fault coverage of the pseudorandom patterns. In production, however, you'll be able to test wafers with 10 or fewer probes. Finally, the BIST approach makes field maintenance relatively inexpensive.

For designs that use all four methods of designing for testability, the functional yield decreases as the overall circuit size increases, or as the active and interconnect areas on the circuit increase. The yield depends on the particular testability method you use.

One disadvantage of the highly structured techniques (the structured and BIST approaches) is that they make it easier for a prober to discover a design's logic structure by way of the serial scan ports. The ad hoc and semistructured methods, on the other hand, have no effect on how easy it is to copy a design's underlying logic.

Compared to the ad hoc and structured approaches, the semistructured and BIST methods accommodate logic changes more easily. To obtain a suitable signature, you need only create a new simulation. If you've used the structured method and you need to make engineering changes, you must consider a number of factors: the logic complexity, the extent of the change, and the availablity of special software (such as scan-overlay, pattern-serialization, and automatic-test-generation software).

COMPARISON OF DESIGN-FOR-TESTABILITY TECHNIQUES

SELECTION CRITERIA	TECHNIQUE: AD HOC	SEMI-STRUCTURED	STRUCTURED	BIST
SILICON OVERHEAD	1	2	3	4
EFFECT ON PERFORMANCE	1	1	4	4
DESIGN, PRODUCTION, AND MAINTENANCE ECONOMICS	4	3	2	1
EFFECT ON YIELD	1	2	3	4
DESIGN PRIVACY	1	1	3	3
ENGINEERING CHANGE	2	2	2	2
EXTENDABILITY	4	2	2	1
TESTING TYPE	3	2	1	2

NOTE:
1 = BEST/LOWEST;
4 = POOREST/HIGHEST

When you're using an ad hoc approach, you can add functional-test capability simply by deciding which functions to include as part of the design. You can easily extend BIST and semistructured methods from chip- to board- and system-level testing. These two techniques are excellent choices for board- and system-level diagnostics because they are part of a top-down design for testability strategy. If you use the structured approach, you can easily move from chip- to board- and system-level testing when memory is available for logic testing and when you can use a maintenance processor to compare the device data serially to test standards.

To obtain pass/fail data when you use the ad hoc approach, you must apply conventional test vectors. You can enhance fault isolation both during the design phase and by using fault dictionaries developed via fault simulation. The BIST and semistructured approaches provide easy pass/fail functional testing but poor internal fault-isolation capability. They detect faults but don't locate them—they don't show which patterns detect which fault. Finally, the structured method provides both easy pass/fail testing and excellent internal fault-isolation capabilities.

Once you have a basic understanding of the different design-for-testability techniques, you need to analyze the tradeoffs that each method involves. The decision isn't a simple one: You must compare a design technique's nonrecurring and recurring costs while considering its effect on yield and reliability. And performing top-down design—from system to board to chip—takes both time and a major corporate commitment. Still, you must make such a commitment if you wish to take full advantage of the benefits of designing for testability.

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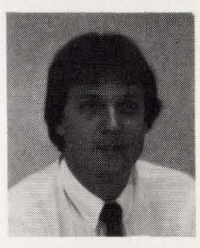
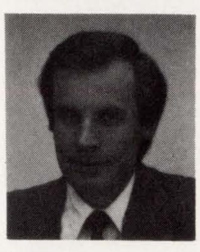
Authors' biographies

Robert D Hess is currently a consultant specializing in design for testability. Prior to forming his own consulting company, he was the vice president of strategic product planning at Caedent Corp (Colorado Springs, CO). Before cofounding the company in February 1985, he held various engineering and management positions at United Technologies Microelectronics Center and Texas Instruments. Bob holds a BS in mathematics from Missouri Valley College and an MS in computer science from the University of Missouri at Rolla.



William C Berg Jr is director of engineering and development at Caedent Corp, and has broad experience in design for testability and BIST. Prior to joining the company as a cofounder, he was with United Technologies Microelectronics Center and Texas Instruments. Bill holds a BSEE degree from Texas A & M University.



Gordon B Hoffman is CEO and chairman of Caedent. He was previously the general manager of the United Technologies Microelectronics Center (UTMC), which he founded in 1980. Before that, he held various management positions at Mostek. Gordon holds a BSEE from Illinois Institute of Technology and an MSEE from Stanford University.

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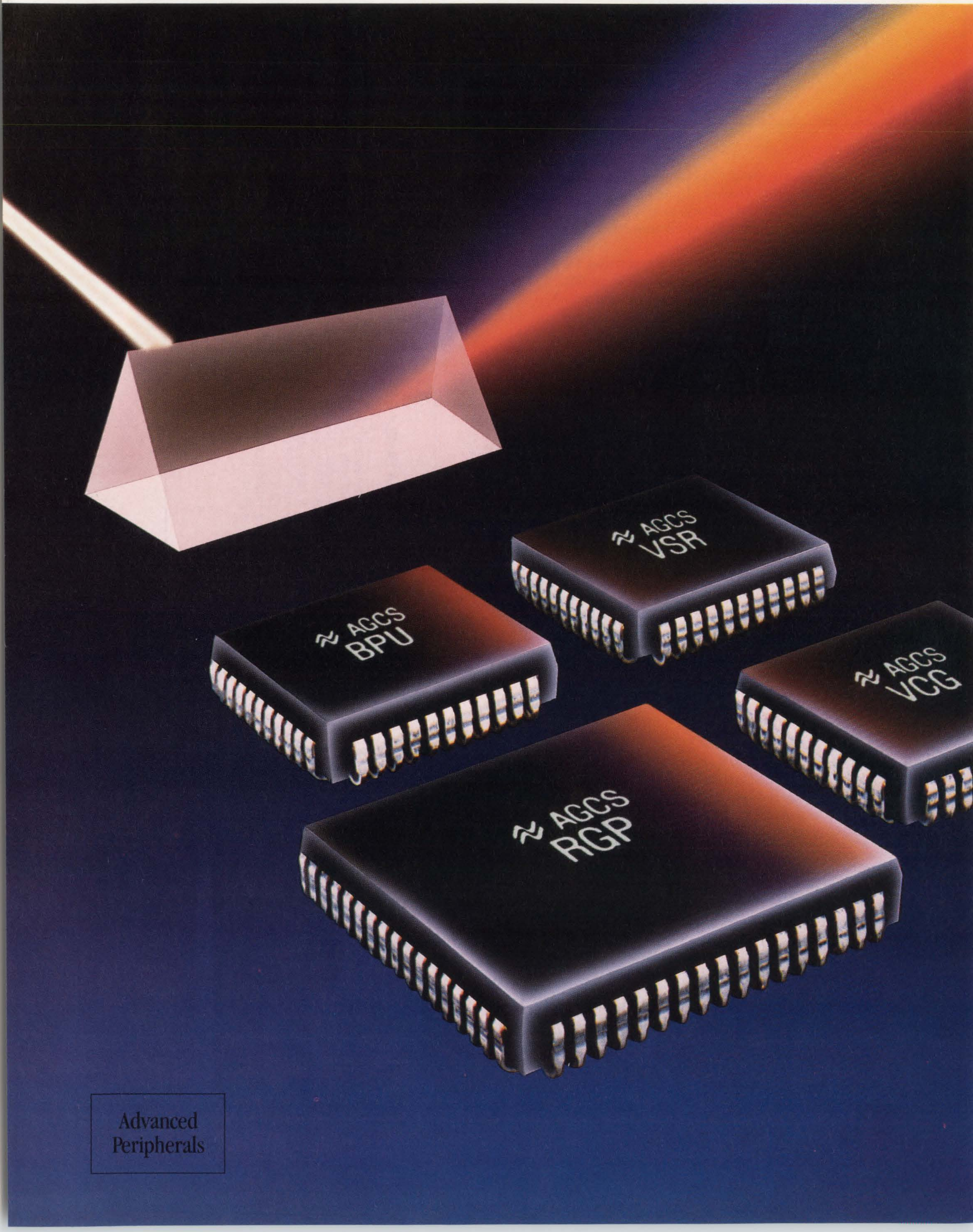

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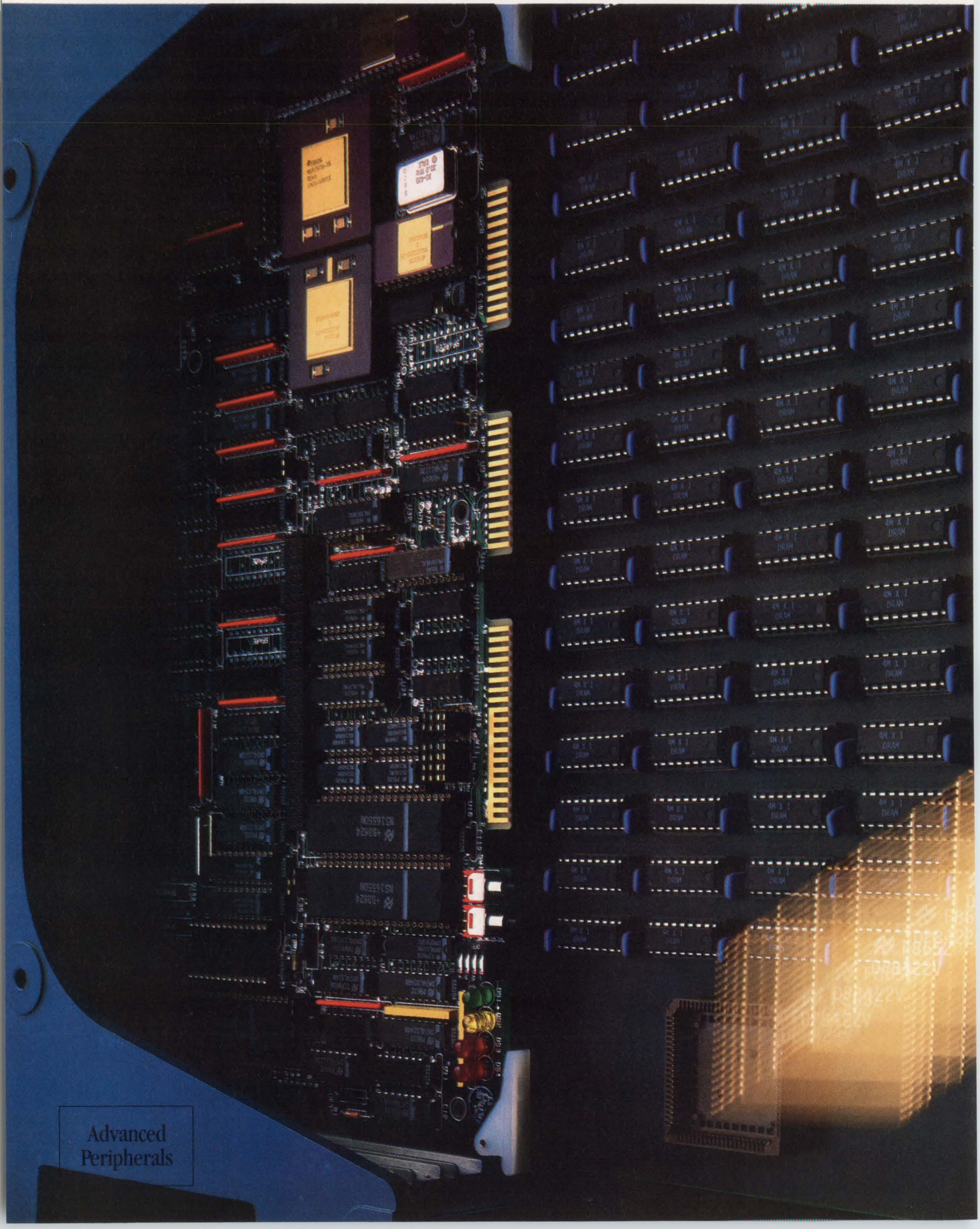

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Fuzzy logic allows creation of precise process controllers

Skilled operators don't control processes by solving equations: They use their expertise and rules of thumb. Fuzzy logic provides a way for you to program an expert operator's knowledge into a process controller or expert system.

Pedro J Guilamo, *Bailey Controls Co*

To control many processes, you must design systems that can understand and analyze imprecise data. For example, if the temperature in a process-control site rises to an unacceptable level, a controller can only open a valve to bring the temperature down to a safe level if it knows how high the temperature should be and how far to open the valve. A skilled human operator knows exactly how much to adjust a valve to lower the temperature, but unfortunately it's impossible to turn an operator's expertise into an equation that can be programmed into a process controller.

Fuzzy-set theory gives you a way to analyze imprecise quantities and develop systems that reason in the same way as people. Systems that use fuzzy logic can imitate human reasoning and thought processes (**Ref 1**) and select the same course of action that an expert operator would choose.

A system based on fuzzy logic can use linguistic variables. Using fuzzy logic, you can model such vague descriptions as "partially open valve," "satisfactory temperature," or "excessively fast speed." A typical question that a fuzzy-logic-based system can answer is "What should the temperature setting be if the input voltage drops?"

To program a fuzzy-logic-based system, you must first ask an expert operator to describe the rules of thumb that he follows. Once the expert has defined the system's process-control rules, and after you've done the programming, the system can understand words and concepts. A fuzzy-logic system doesn't need numerical input and output data: It's capable of accepting parameter descriptions such as "too low" and "satisfactory."

The way the system evaluates these imprecise concepts is to assign a membership function to each member of the fuzzy set. Boolean logic, in contrast, permits only true and false logical states. Boolean logical elements must be one or zero; members of a fuzzy set can take any fractional value from zero to one.

For example, the ordinary set of men between the ages of 15 to 25 includes all men aged 15 to 25 and excludes all other men. A fuzzy set lets you assign a value, or grade, to each age. Instead of grouping all men of 15 to 25 together equally, you can grade the ages within the set and separate the younger men from the older ones. If you want to assign grades of 0.9 to age 15, 0.5 to age 20, and 0.2 to age 25, for instance, you simply create the set

$$\{(15,0.9), (20,0.5), (25,0.2)\}.$$

As another example, consider a fuzzy-logic controller that monitors analog inputs. If you make up a fuzzy set "input is high" for voltages of 0 to 5V, the controller will scale the values 0 to 1. Thus, for an input voltage of 3.5V, the membership function is 0.7. Obviously, a controller that doesn't need to differentiate between varying input voltages doesn't need fuzzy logic. Howev-

Instead of relying on equations to solve problems, a fuzzy-logic system capitalizes on the knowledge of an expert operator.

er, if the voltage parameter that the system is controlling varies along with other parameters (such as room temperature and circuit resistance), then the controller can benefit from a fuzzy-logic design.

To enable a fuzzy-logic process controller to evaluate the relative effect of several parameters, you must operate on the membership functions with logical operators. Like standard logic, fuzzy logic uses the operators AND, OR, and NOT. The results of applying logical operators to the membership functions μ_A and μ_B are

$$\mu_A \text{ AND } \mu_B = \text{MIN}(\mu_A, \mu_B)$$
$$\mu_A \text{ OR } \mu_B = \text{MAX}(\mu_A, \mu_B)$$
$$\text{NOT } \mu_A = 1 - \mu_A.$$

For example, you can use the membership functions in **Fig 1** to control the temperature in a process-control

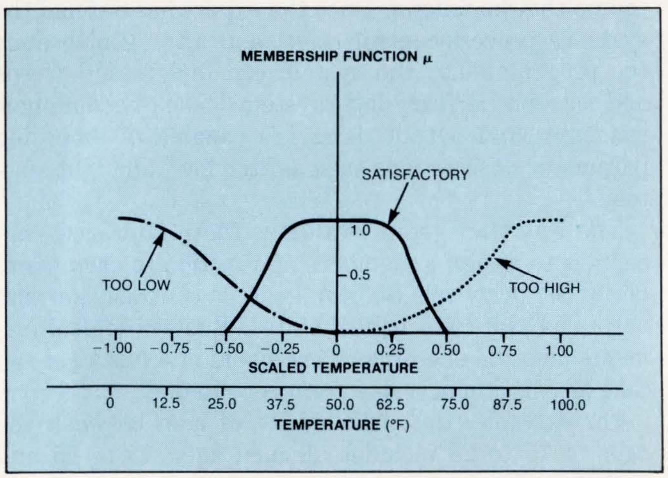

Fig 1—A typical fuzzy set's membership functions *consist of a convex curve that describes satisfactory operating conditions and a concave curve that describes unsatisfactory conditions.*

application. You must define three fuzzy sets—low temperature, satisfactory temperature, and high temperature—and you must specify the membership function of each. In **Fig 1,** the membership functions are centered on 50°F. A membership function can be as wide as you like; the width is simply an expert's estimate of the safe operating conditions of a process.

In **Fig 1,** a typical graph of membership functions, the satisfactory range is a convex function and the low and high range together form a quasiconcave function. The low-temperature curve has the value of 0.25 at 37.5°F. The satisfactory-temperature curve has the value of 0.75 at 37.5°F. If you apply fuzzy-logic operators to the membership functions at 37.5°F, you find that

μ_A AND μ_B = MIN (0.75, 0.25) = 0.25 → T1 IS SATISFACTORY AND T2 IS LOW

μ_A OR μ_B = MAX (0.75, 0.25) = 0.75 → T1 IS SATISFACTORY OR T2 IS LOW

NOT μ_A = 1 − 0.75 = 0.25 → T1 IS NOT SATISFACTORY

NOT μ_B = 1 − 0.25 = 0.75 → T2 IS NOT LOW.

The satisfactory-temperature value for T_1 is μ_A, and the low-temperature value for T_2 is μ_B.

The expressions on the right-hand side of the arrows are linguistic equivalents of the equations on the left. As you can see, the statement, "T1 is satisfactory and T2 is low," has the value of 0.25 at 37.5°F. The statement, "T2 is not satisfactory," has the value of 0.75 at 37.5°F.

Fuzzy logic is particularly useful for controlling non-

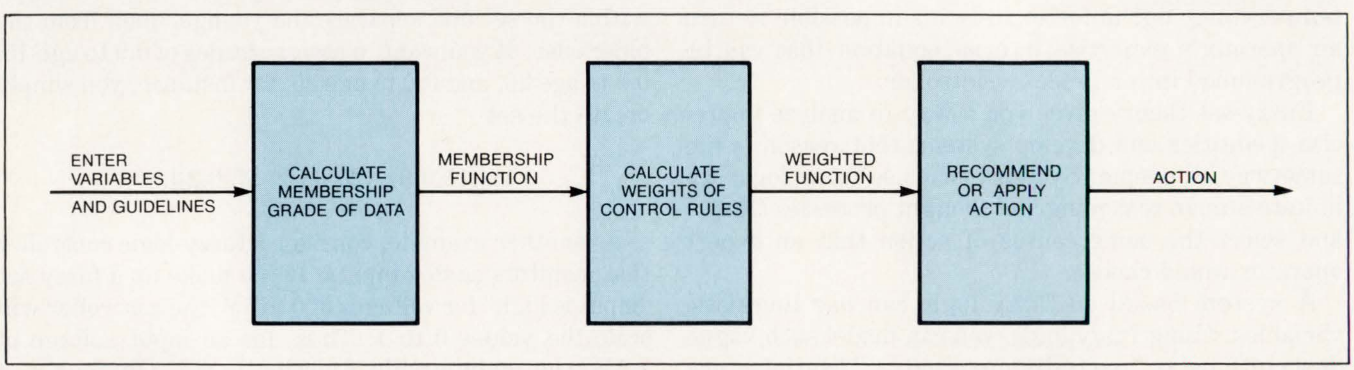

Fig 2—By following these steps, *a fuzzy-logic controller can analyze a set of process variables, find the weighted average of all control rules in the process, and perform the same action that an expert operator would.*

linear processes because these processes are hard to describe with equations. For instance, you can't control the operation of a cement kiln with a conventional controller because variables such as kiln temperature and oxygen content don't vary linearly over time. A conventional controller can regulate only a few loops in a cement kiln; the kiln operator must control the other loops manually. A fuzzy-logic process controller, however, does permit the regulation of a cement kiln **(Ref 2)**.

To control such a process, you use the guidelines that a skilled cement-kiln operator would follow and make fuzzy sets. You simply specify the kiln's membership functions and then establish a set of process-control rules. You can write a general set of control rules, where each condition is a fuzzy set, as "If condition_1 AND/OR condition_2 . . . then $(\text{action})_1$." After you've implemented the fuzzy logic in the controller, you don't need a system operator: The operator's expertise is a part of the system.

In most process-control applications, each variable, consisting of a different condition of the process, affects the other variables. To permit a controller to reach a decision, you must attribute weight to each control rule. The weight of a rule is the degree to which a variable depends on that rule. After calculating the weights of all the control rules, the center of gravity (or weighted function) of the weighted average of the control rules determines a controller's action. **Fig 2** shows the steps that you must follow to program a fuzzy-logic controller.

All expert systems, not just process controllers, follow the steps in **Fig 2.** All expert systems rely on the knowledge of an expert to solve problems, and most process data according to predicate logic or probability. (Predicate logic is similar to standard Boolean logic but adds the quantifiers "some" and "all" to "true" and "false.") Predicate logic is too restrictive to replicate human thoughts. Further, many applications of expert systems aren't based on random occurrences, and probabilistic methods thus give incorrect results. Predicate logic and probability don't take advantage of the knowledge and expertise of a human.

In an expert system without fuzzy logic, the answer or the recommended advice usually relies on a certainty factor, based on probability calculations. Because most of the problems that an expert system analyzes are imprecise (but not random), a certainty factor is unreliable. A grade of membership, on the other hand, is a rank, not a probability. You can apply membership functions to statistical quantities, though. In fact, statistical sets are often natural fuzzy sets **(Ref 3).** The membership function is still a subjective quantity, but the subjective quantity is a group value, not an individual one.

You can implement fuzzy logic in a controller or an expert system in either hardware or software. Because fuzzy-logic analysis on a conventional computer is computation intensive, fuzzy-logic programs run much faster on custom hardware. It's possible to build a circuit consisting of a DAC, ROM, and several standard-logic

Expert systems account for individuality

Expert systems that use fuzzy logic don't use probability-based certainty factors. Instead, they reach conclusions by weighing the impact of all factors.

You can use a fuzzy-logic expert system to assess the prognosis of a heart patient, for instance. A fuzzy-logic expert system might assign a grade to the effect of a high cholesterol level on a particular patient. The cholesterol level, of course, is just one of the factors that contribute to heart disease. By evaluating the grades assigned to all of the factors leading to heart disease, an expert system can calculate the likelihood that a patient will have a heart attack.

Several of the expert systems that assist physicians use fuzzy logic. The Kemp-Carraway Heart Institute's (Birmingham, AL) Flops program uses fuzzy logic to handle contradictory, uncertain, and ambiguous information **(Ref 1).** The program runs on IBM PCs. Reveal, a program from Physician Products (Mountain View, CA), also uses fuzzy logic to help physicians analyze symptoms. Incidentally, product marketers also use Reveal—to forecast sales.

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chips to convert analog signals to fuzzy logic **(Ref 4)**. Using this circuit, you can link a measurement system to a personal computer.

As an alternative to implementing fuzzy logic in standard ICs, though, a custom chip can perform the same calculations. Moreover, a computer integrating custom fuzzy-logic ICs can run fuzzy-logic software faster than a computer using standard circuits. A custom fuzzy-logic IC is capable of analyzing approximately 80,000 fuzzy-logic control rules per second, which is much faster than that of a conventional expert system using conventional ICs **(Ref 5)**. A custom IC can handle such diverse tasks as missile command and control, robotics, and manufacturing. For more information on these types of custom ICs, you might want to consult **Ref 6**. It describes nine CMOS fuzzy-logic ICs that operate in the current mode; they don't require resistors or isolation. **EDN**

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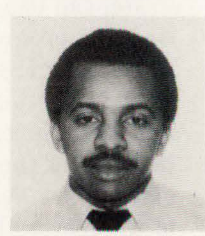
Author's biography

Pedro J Guilamo has been an engineer at Bailey Controls Co (Wickliffe, OH) since 1981. He received a BSEE from City College of New York and an MS in mathematics from Cleveland State University. In his spare time, Pedro enjoys writing programs on his personal computer and reading science fiction.



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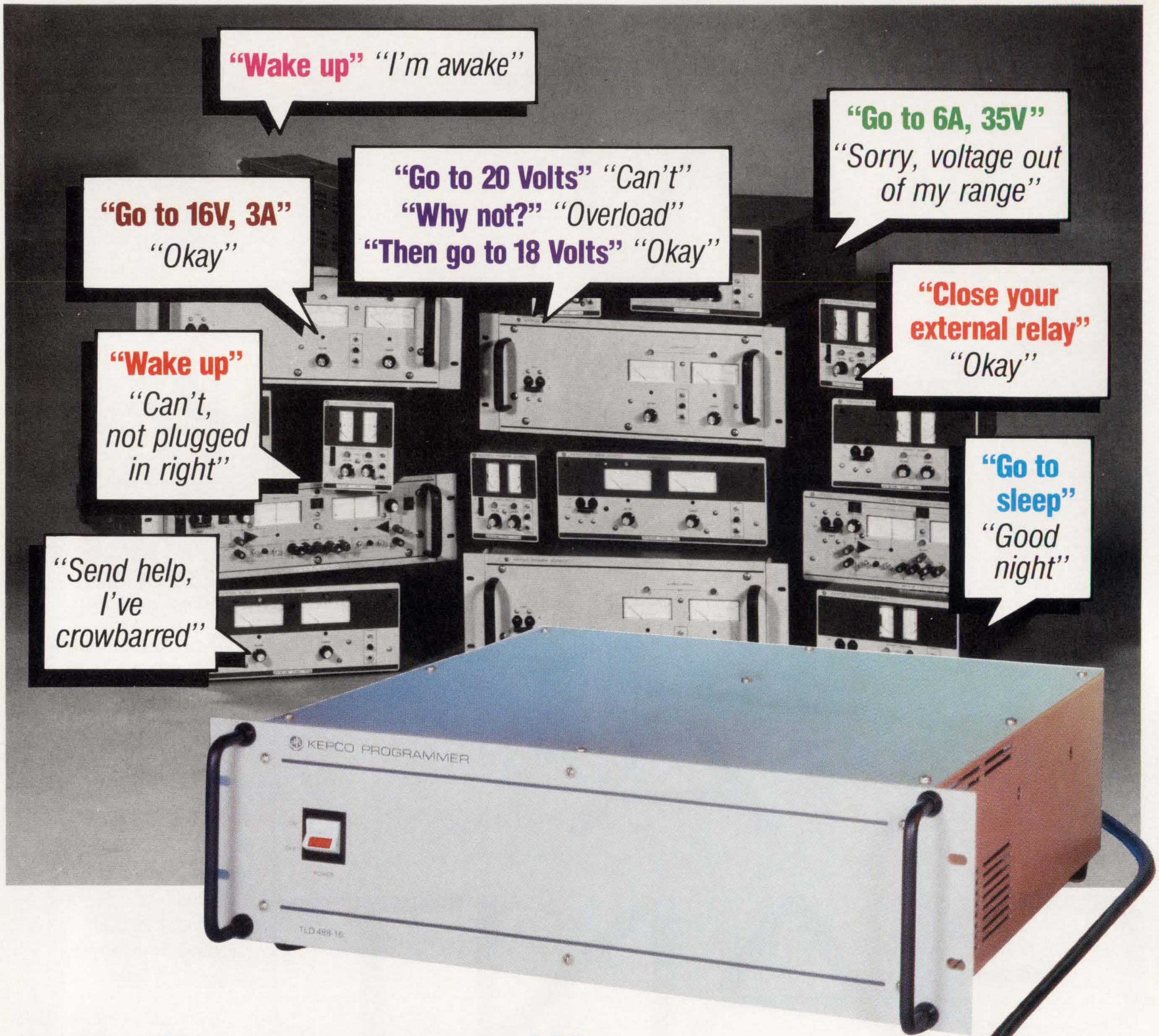

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The Kepco Power Managers are linear power supplies designed for programming applications. They can scale a uniform 0 to $\pm$1V or 0 to $\pm$10V analog control signal into any desired output up to 1000 Volts and 1000 Watts, in some hundred different Volt/Ampere combinations.

The Kepco **Digital Interfaces** were created to take full advantage of the Power Managers' precision and speed of response. They translate 12-bit digital signals into the analog control signals the Power Managers understand.

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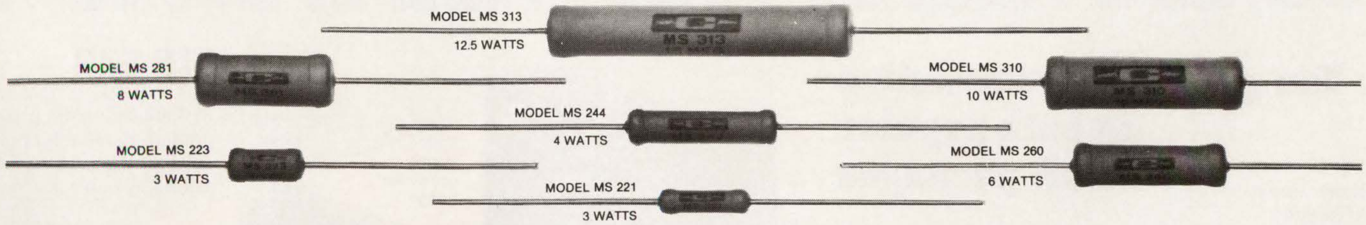
CIRCLE NO 151

Type MS Non-Inductive Power Film Resistors from CADDOCK optimize high-speed power switching:



1. Caddock's "Non-Inductive Design" can improve rise and fall times to minimize losses in power switching circuits.

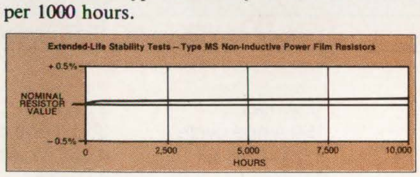
To keep the inductance to an absolute minimum, the special serpentine pattern provides for neighboring lines to carry the current in opposite directions to achieve maximum cancellation of flux fields over the entire length of the resistor.

The result is a truly non-inductive resistor that is about as inductive as a straight piece of wire the length of the resistor body.

This makes it possible for engineers to design new circuit configurations with superior non-inductive performance.

2. Extended-life stability that is typically better than 0.05% per 1000 hours.

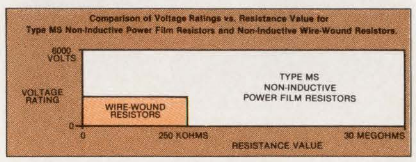
Extended load-life tests at full power have demonstrated typical stability better than 0.05% per 1000 hours.



Detailed stability data is included in the "Reliability Test Summary – Caddock Report #1" which is available on request.

3. Critical resistance values extended by higher voltage and power ratings.

Caddock's Micronox® film resistor technology permits single-resistor voltage ratings as high as 6000 volts to be combined with power ratings of 12.5 watts at +25°C. This combination of power and voltage provides a critical resistance value of 2.88 Megohms - more than 10 times higher than can be achieved with wire-wound construction.



The higher voltage rating of Type MS resistors also overcomes the resistance value limits imposed on wire-wounds by the minimum wire size and spacing.

4. The special construction of Micronox® resistors assures high performance through harsh environments.

Type MS Power Film Resistors are produced by firing high-stability Micronox® resistance films directly onto a solid ceramic core - in air - at +1400°F to achieve a structure with these special performance advantages:

- Operating temperatures as high as +275°C.
- Repeatable temperature characteristics that include a TC of only 50 PPM/°C.
- Verified reliability through environmental extremes encountered in both 'down-hole' oil exploration and deep-space instrumentation equipment.

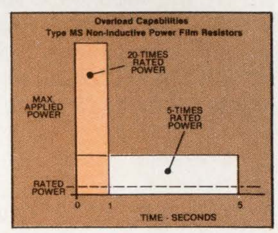
5. The family of Type MS Power Film Resistors includes 14 models with single-resistor values to 30 Megohms.

To overcome the construction *and* cost limitations inherent in wire-wound resistors, Caddock Micronox® film resistor technology gives circuit designers a *practical* balance between performance, value, size and cost, as the specifications for the Model MS 313 demonstrate:

- Non-inductive performance.
- 12.5 watt power rating.
- Resistance values from 50 ohms to 30 Megohms.
- Resistance tolerances from ±1.0% to ±0.1%.
- Maximum operating voltage of 6000 volts.
- Unit prices below $2.50 on 1000-lot orders for any value between 100 ohms and 200 Kohms.

6. Overloads of 5-times rated power for 5 seconds and 20-times rated power momentary are standard on all models.

After repeated power overload tests that apply 5-times rated power for 5 seconds, Type MS resistors have demonstrated stability typically better than 0.1%



For even higher overload situations, Type MS resistors can be subjected to 20-times the rated power for one second.

Caddock's advanced film resistor technology is the source of these outstanding advantages—advantages that are matched by a 25-year record of outstanding 'in-circuit' reliability.

Discover how easily these problem-solving resistors can improve the performance and reliability of your equipment, too. For your copy of the latest edition of the Caddock 28 page General Catalog, and specific technical data on any of the more than 200 models of the 19 standard types of Caddock High Performance Film Resistors, just call or write to—

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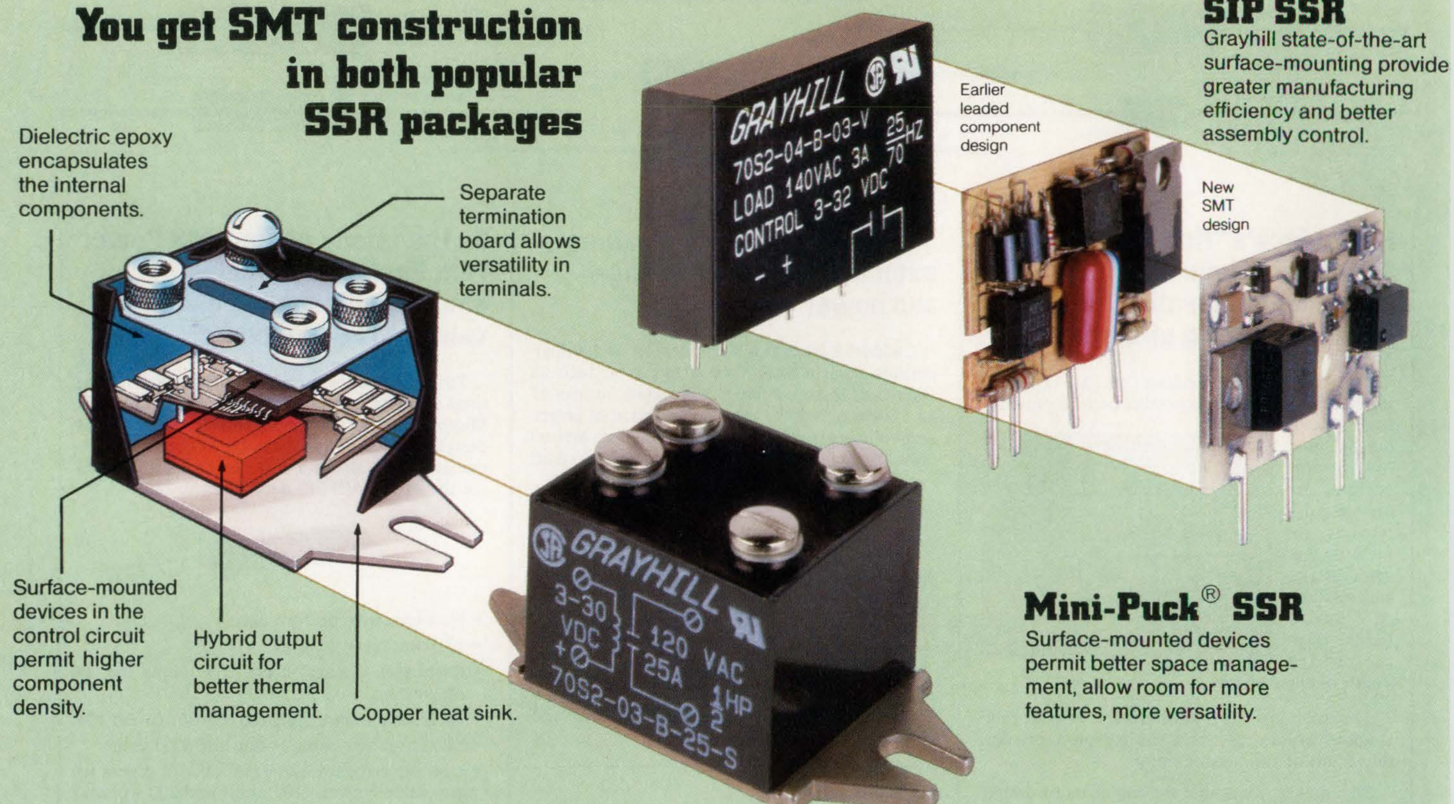

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	Leaded components	SMT design
Output circuit		
Load current	12 A max.	25 A max.
Surge current	150 A one cycle	350 A one cycle
Static dV/dT	3,000 V/μsec	4,000 V/μsec
Offset voltage	8 V max.	4 V max.
Thermal resistance	2.4 C/W	1.75 C/W
Zero crossing window	50 V AC	25 V AC
Power factor	0.5 typical	0.4 typical
General characteristics		
Isolation resistance	100 MΩ	1,000 MΩ
Dielectric voltage	2,500 V AC rms	4,000 V AC rms
Input to output capacitance	6 pF typical	4 pF typical

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CIRCLE NO 149

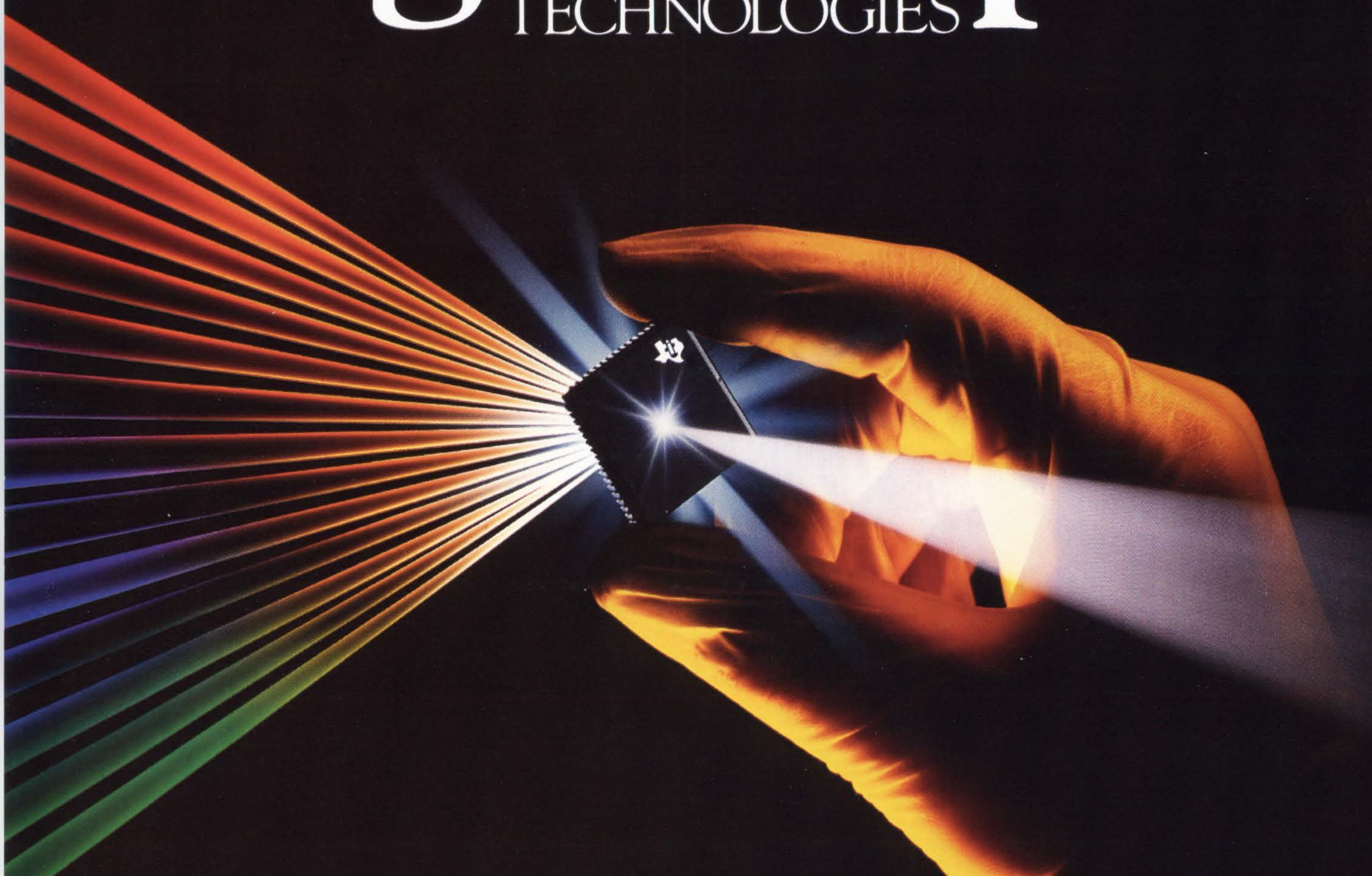
TEXAS INSTRUMENTS REPORTS ON

GRAPHICS

IN THE ERA OF

MegaChip

TECHNOLOGIES



Graphics in the Era of MegaChip Technologies:

New Texas Instrument lets you program circle

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From PC displays to laser printers, the flexibility of TI's TMS34010 processor delivers the leading-edge performance you need today and to stay out in front tomorrow.

In TI's TMS34010 Graphics System Processor, you have a n and better graphics-design approach: The first high-performance, 32-bit CMOS microprocessor optimized for graphics applications.

The 34010 can execute all functio needed by graphics operating enviror ments; hard-wired coprocessors can only execute a small part.

32-bit graphics processor around competition...

ext, and more.

Because the 34010 is pro-rammable, it is in a league all s own."

m Richards, president of VMI, is lking graphics performance. You can rogram the 34010 processor to per-rm any graphics function you want, nlike hard-wired coprocessors. This eans you can readily customize your stem to outperform your competition.

But there's an even more important aspect to consider. The 34010 will help keep your system ahead of competition because it is compatible with existing graphics hardware standards — CGA,™ EGA,™ and PGC™ — and supports graphics software standards such as CGI, DGIS,™ and MS-Windows.™

Standards like Windows and DGIS run faster on TI's TMS34010

The 34010 is also among the fastest microprocessors available. It handles six million instructions per second with a "draw" rate of up to an amazing 50 million pixels per second. Thus, it can boost total system performance.

Because of the support of MS-Windows and DGIS alone, many major applications software packages can already run on 34010-based systems.

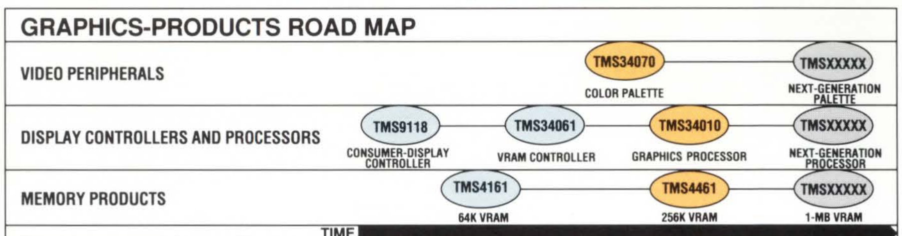
TI's MegaChip Technologies

Our emphasis on high-density memories is the catalyst for ongoing advances in how we design, process, and manufacture semiconductors and in how we serve our customers. These are our MegaChip™ Technologies, and they are the means by which we can help you and your company get to market faster with better products.

workstations, terminals, plotters, FAX, image processing, digital copiers, mass storage, robot vision, and communications.

TI's total systems solution

In implementing your design, you'll want to consider other building blocks TI has developed. Included are the single-chip TMS34070 66-MHz Color Palette that supports simultaneous display of 16 out of 4,096 colors and the



Road map to tomorrow's graphics systems: Next-generation additions to TI's innovative graphics-products family will allow you to build on your present designs to develop even higher-performance systems.

"You would think TI designed the 34010 with our technology in mind."

Luis Villalobos, Conographic president, refers to the power of the 34010 to process font outlines for desk-top publishing. Resolution up to 64K × 64K means no hardware limits for laser printers and other hard-copy devices.

Host independence and the flexibility of a device programmable in "C" language make TI's 34010 the cost/performance leader for PC displays, laser printers, desk-top publishing,

TMS70C42 Microcontroller that handles all serial interface duties.

Also included are high-speed video random-access memories (TMS4161 and TMS4461), plus linear small and large-area CCD image sensors.

To provide the host bus interface and any other customized functions you may require, TI offers quick design and production turnaround through its Application-Specific Integrated Circuits (ASICs) capabilities.

Development tools are available now for applying the 34010. Turn the page for details. ▶

"Texas Instruments had ready the full set of development tools we needed."

As William Frentz, executive vice president at Number Nine Computer, points out, TI has ready the hardware, software, and documentation you will need to make designing in the 34010 as fast and as easy as possible.

TI's 34010 software includes a full Kernighan and Ritchie "C" compiler with extensions and an assembler package for both MS-DOS™ and VAX™ operating environments.

A graphics/math library provides source code for more than 100 functions, whereas a typical controller chip offers only 15 to 20. A special font library contains more than 100 type fonts to expedite development of desktop publishing applications.

The TMS34010 XDS/22 Emulator is a flexible, realtime, in-circuit emulator. It can be used in a stand-alone mode through a standard terminal or through a host computer with a powerful debugger interface.

To see immediately what TI's new graphics processor can do for you, just plug the TMS34010 Software Development Board into an IBM® PC-compatible or TI Professional computer. The board is populated with TI's 34010 Graphics Processor, Color Palette, and VRAMs. It provides an ideal environment for developing your own high-performance graphics applications.

For more information on TI's total graphics-system solutions, including details on TI's Graphics Design Kit and design training courses, complete and return the coupon today. Or write Texas Instruments Incorporated, P.O. Box 809066, Dallas, Texas 75380-9066.

FOR FREE ON-LINE INFORMATION, dial 1-800-345-7335 with any 80-column ASCII terminal or PC and a 300 or 1200 baud modem (EVEN or IGNORE parity, 7 data bits, 1 stop bit). At "Enter Response Code," type TIGRAFX. In Conn. dial (203) 852-9201.

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To speed the design of your graphics system, TI's range of development tools includes a comprehensive design kit *(left rear)*, a realtime emulator, and a plug-in software development board. On floppy and magnetic disks: "C" compiler, assembler package, and function and font libraries. User's guides, development books, product bulletins and data sheets, and TI's newsletter, *Pixel Perspectives,* are all readily available.

Hundreds of designers must be right. Hundreds of hardware and software designers are making TI's 34010 the new graphics standard. Among them are leading board-development houses and major software vendors.

In fact, the wide range of graphics standards and application software already written for TI's 34010 makes it the easiest-to-use new graphics chip ever introduced. Here's just a sampling of the software that will run on top of Graphic Software Systems DGIS* 34010:

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Master Series™	Ashton-Tate
Freelance Plus™	Lotus GPG
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Harvard Presentation Graphics™	Software Publishing Corp.
ProDesign II™	American Small Business Computers
VersaCad™	VersaCad Corp.
Windows™†	Microsoft
Symphony™, 1-2-3™	Lotus Development
P-CAD™	Personal CAD Systems

™Trademarks are as noted.

†More than 100 graphics applications are currently available for these operating environments.

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TEXAS INSTRUMENTS

EDITED BY TARLTON FLEMING

Serial status transmitter uses low power

Bob Lelle
Retail Automation, Mesquite, TX

The status transmitter of **Fig 1** accepts as many as seven parallel bits of status information, converts them to a serial word, and presents the word to an RS-232C-compatible interface. The circuit lends itself to battery-powered applications because its three CMOS ICs operate from a 5V supply and dissipate little power.

The status signals (shown originating at open-collector outputs) connect directly to the parallel inputs of the 8-bit parallel-to-serial shift register IC_1. This IC shifts out the serial data (Q_H or its complement $\overline{Q_H}$, as required) in reverse-alphabetical order—that is, input H through input A. (You can cascade two shift registers to accommodate an 8-bit word.) The RS-232C transmitter/receiver IC_3 then formats this TTL-compatible signal for transmisssion through the serial port.

After consulting your computer's reference manual, you should program the serial port for 300-baud transmission with no parity detection. The asynchronous communications chip found in most serial ports will accept 5-, 6-, 7-, or 8-bit words with 1, 1½, or 2 stop bits. Each data word requires low-level start and stop bits.

To transmit a 5-bit word with one stop bit, for example, ground the G input (IC_1) for the start bit, ground the A input for the stop bit, and then create dummy bits by connecting a logical one to the H and SER IN inputs. To transmit a 7-bit word, ground IC_1's H and SER IN inputs (pins 6 and 10) to provide the start and stop bits, respectively.

The computer initiates transmission by asserting the DTR (data terminal ready) signal. In response, IC_1 shifts out one bit with each positive transition of the clock signal at pin 2, until DTR completes the transmission by going low after the character's last stop bit. You should set the baud-rate generator (R_1, C_1, and IC_{2A}) at no higher than 300 baud; at higher clock frequencies, the RC components' tolerance might cause timing problems for the computer.

To implement a useful capability for battery-powered applications, you can provide the computer with a DSR (data set ready) signal that tells the computer your terminal is active. Simply connect IC_3's pin 7 to pin 6 of the serial port; an internal pullup ensures that the signal is high when power is applied. **EDN**

To Vote For This Design, Circle No 746

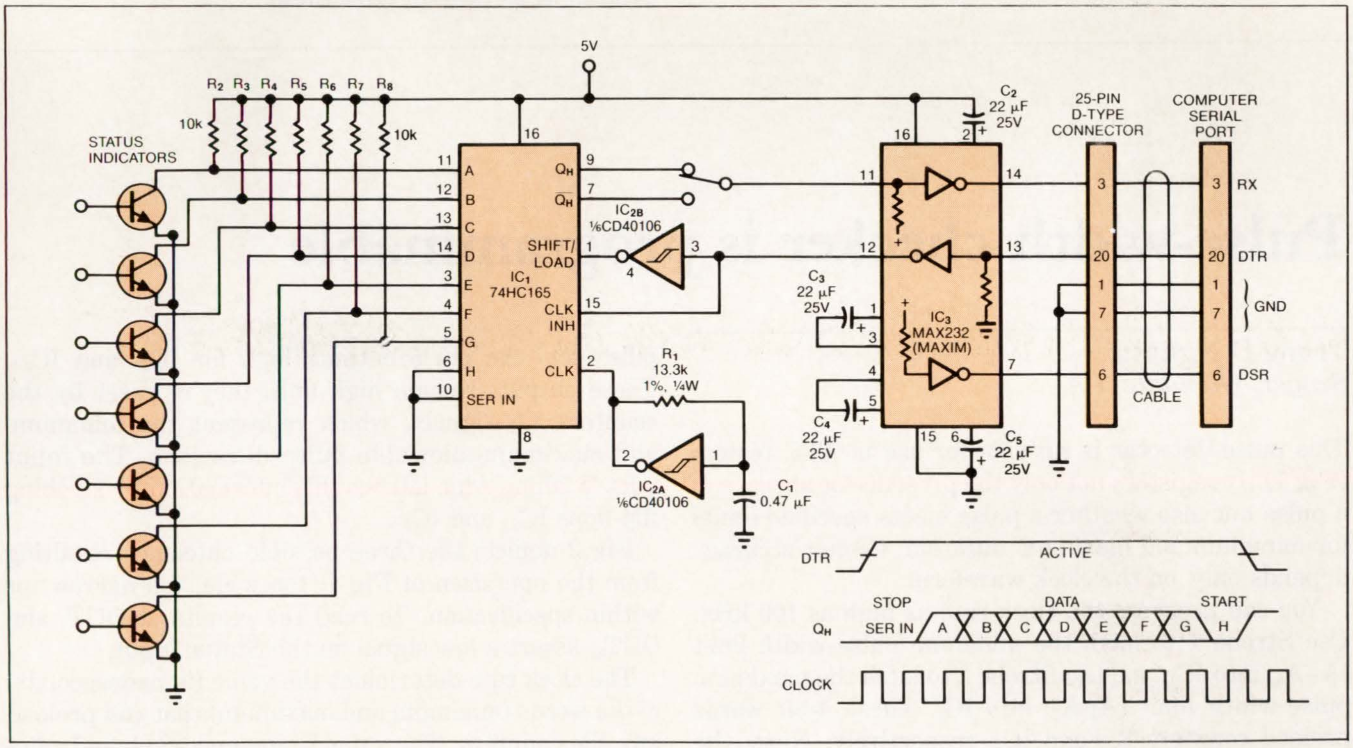

*Fig 1—**This status transmitter accepts parallel** status bits and transmits them in serial format to a host computer over an RS-232C link.*

IC replaces mechanical-interlock switches

Charles E Murphy
Elcotel Inc, Sarasota, FL

As an alternative to mechanical-interlock switches or membrane switches with latches, **Fig 1**'s circuit debounces, latches, and displays status information for a group of eight pushbutton switches in which only one switch at a time is active. The circuit's only IC is an octal latch.

Closing any one of the switches turns on transistor Q_1 and discharges capacitor C_2. Current through Q_1 then charges C_1, causing a positive transition at IC_1's CLK input (pin 11), which turns on the LED for that switch. The LED remains on until you depress another switch. Because the CLK input is edge-triggered and remains high until you release all the switches, two or more switch closures cannot register at one time unless they occur within approximately one millisecond.

Capacitor C_1 provides a delay that debounces each switch closure. Capacitor C_2 causes Q_1 to turn on briefly at power-up, which produces a pulse at IC_2's CLK input, ensuring all LEDs are off by latching all ones at the Q outputs of IC_1. **EDN**

To Vote For This Design, Circle No 750

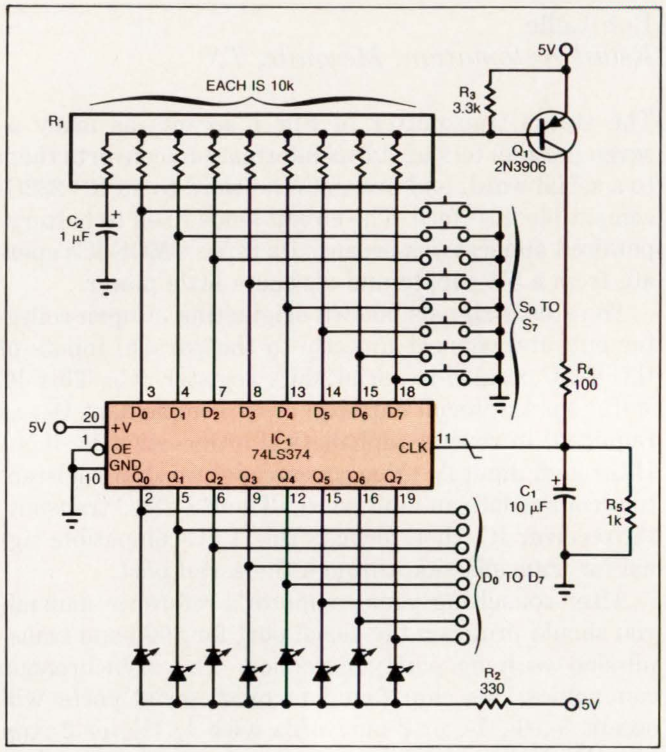

***Fig 1—This single-IC circuit debounces** a group of eight pushbutton switches, latches the last switch closure, and provides an LED indicator for the currently active circuit.*

Pulse-width checker is programmable

Trung D Nguyen
Singer, Glendale, CA

This pulse detector is suitable for use in ATE testers **(Fig 1).** It registers not only the presence or absence of a pulse but also whether a pulse meets specified limits for minimum and maximum duration. Circuit accuracy depends only on the clock waveform.

You can program the clock rate as high as 100 kHz. Use Strobe 1 to latch the minimum pulse-width limit (A_1-A_4) into IC_1, and use Strobe 2 to latch the maximum pulse-width limit (A_5-A_8) into IC_3. These 4-bit words preload counters IC_2 and IC_4, respectively. Next, the coincidence of a positive clock transition with an input pulse sets the pin 5 outputs high for IC_{5A} and IC_{5B}. These outputs remain high until they're reset by the counters' C_O signals, which represent the minimum- and maximum-allowable pulse durations. The input pulse's falling edge latches this information by strobing flip-flops IC_{6A} and IC_{6B}.

Fig 2 depicts the three possible outcomes resulting from the operation of **Fig 1:** too wide, too narrow, or within specification. To read the results at OUT_1 and OUT_2, assert a low signal on the $\overline{\text{Status}}$ input.

The clock rate determines the value (in nanoseconds) of the words (minimum and maximum) that you preload into the counters. The value (min+max)/2 should coincide with the nominal pulse width you anticipate; the

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CIRCLE NO 148

tolerance allowed on this nominal width is (max−min)/2. Using a 100-kHz clock to check for 145-nsec pulses (±5 nsec), for example, you set min=140 nsec (preload a count of 13), and set max=150 nsec (preload a count of 14). You can lower the clock rate to check wider pulses, and you can increase the measurement's resolution by a factor of 10 by cascading two counters. **EDN**

To Vote For This Design, Circle No 747

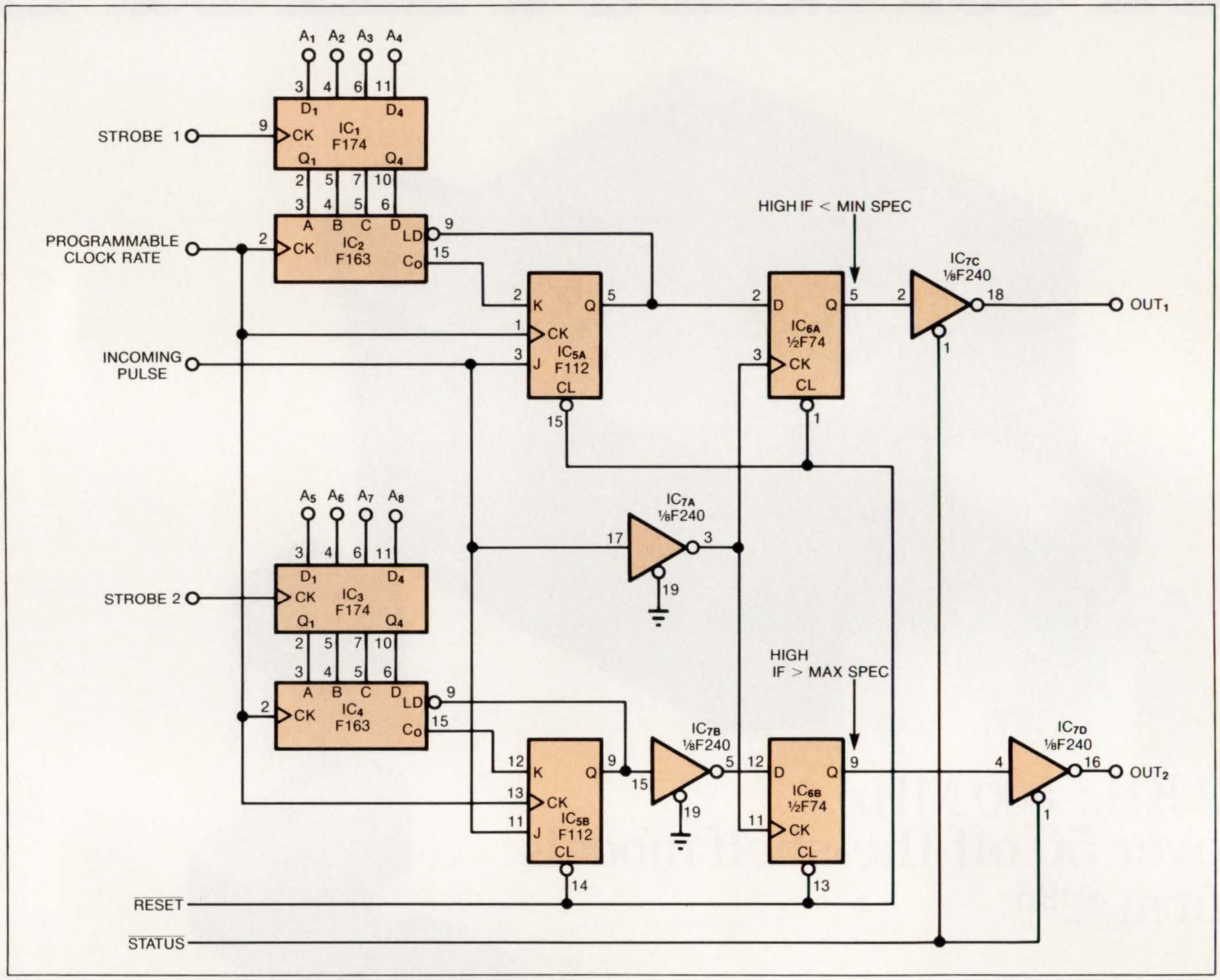


*Fig 1—**This programmable pulse checker lets you preload** the desired minimum and maximum pulse durations corresponding to a given clock rate.*

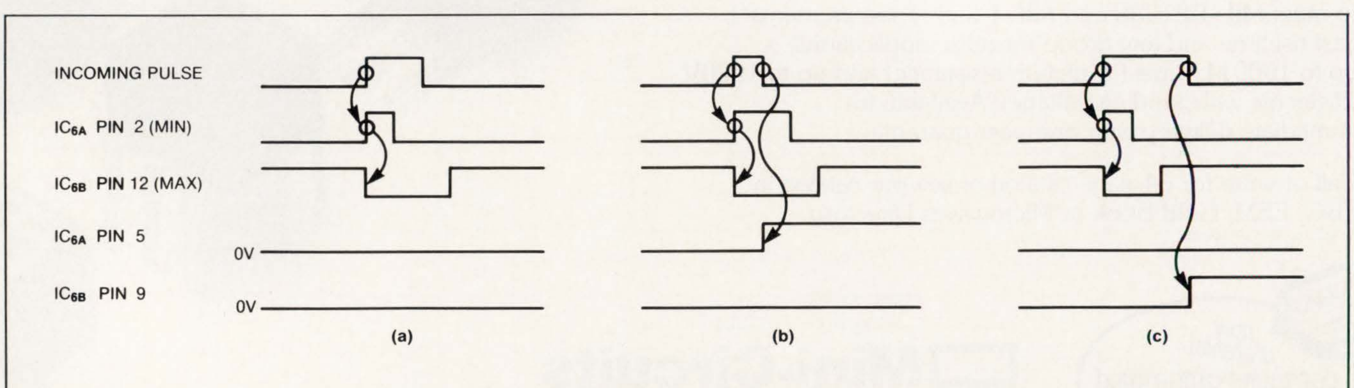
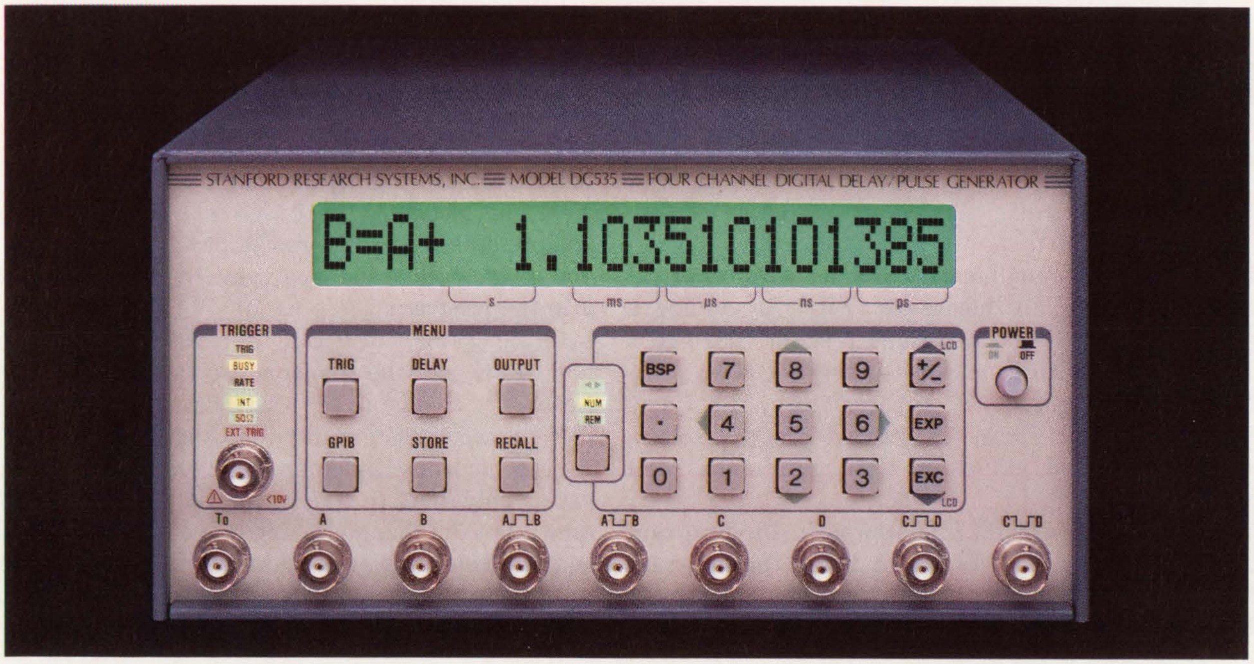


*Fig 2—**These waveforms** illustrate the three possible outcomes of pulse checking: within specification **(a)**, too narrow **(b)**, too wide **(c)**.*

New Precision Pulse Generator



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- **50 ps rms Jitter**
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CIRCLE NO 147

Basic program linearizes thermistors

Mick Murray
Lab-Line Instruments Inc, Melrose Park, IL

You can reduce the nonlinearity of a negative-temperature-coefficient (NTC) thermistor (TH-1) by adding a series resistor (RS) and a parallel resistor (R). **Fig 1** contains the resulting network, designated R_{EQ}. To define optimum values for the resistors, the Basic program of **Listing 1** uses an iterative process, selecting from standard values in data statements 480 through 560.

Using a 3-point straight-line approach, the program can linearize any NTC thermistor. First, the program prompts you for the lowest and highest temperatures of interest and the corresponding thermistor resistance (which you can find in the manufacturer's data sheet). Next, it calculates the exact mid-range temperature and prompts you for the resistance at that point as well. You divide each resistance value by 1k before entering it in the program.

In the example of **Fig 1**, thermistor TH-1 varies 127 to 2.64 kΩ over the temperature range of 20 to 130°C. Resistance change in the lower half of this range (20 to 75°C) is 9.3 times greater than that in the upper half. By comparison, the computer-selected network R_{EQ} varies only 1062 to 977Ω over the same temperature range, but the change in each half of the range is nearly equal. (Note, however, that the network's linearity error increases as you widen the specified temperature range.)

Text continued on pg 222

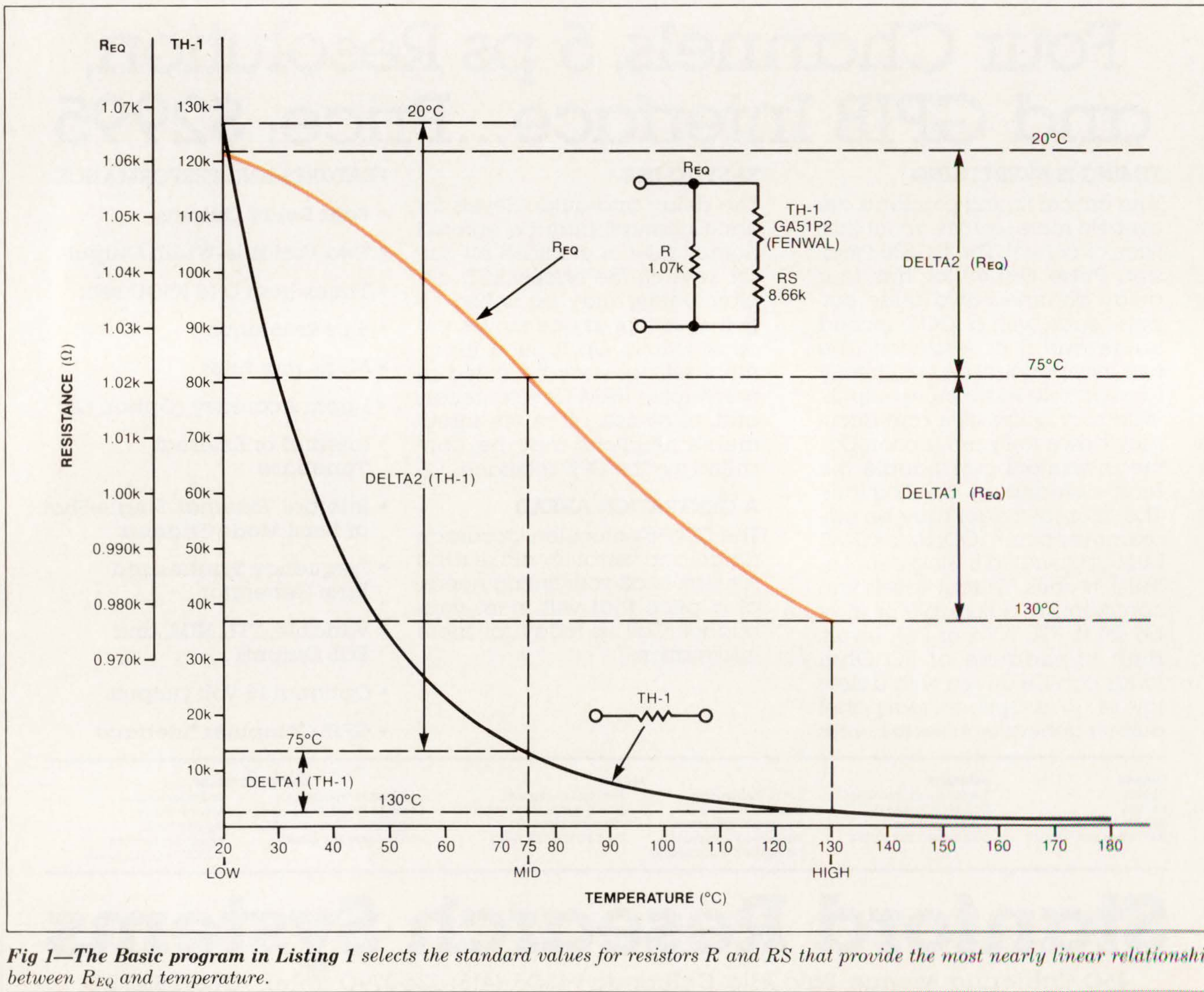

Fig 1—The Basic program in Listing 1 *selects the standard values for resistors R and RS that provide the most nearly linear relationship between R_{EQ} and temperature.*

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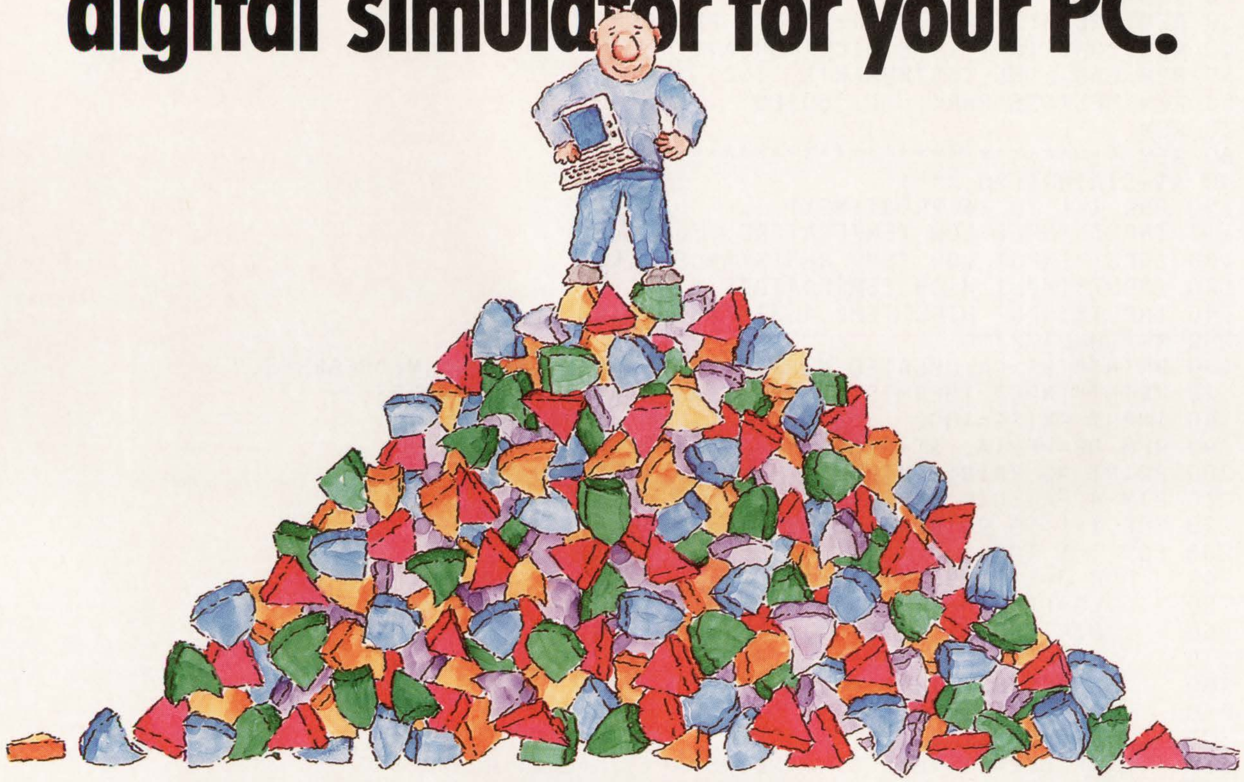

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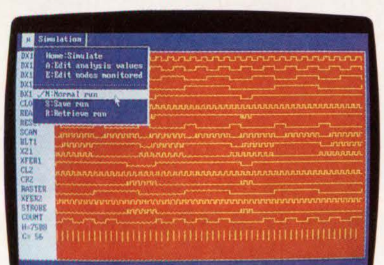

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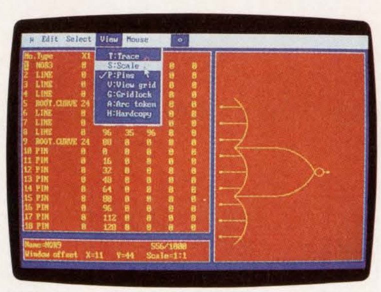

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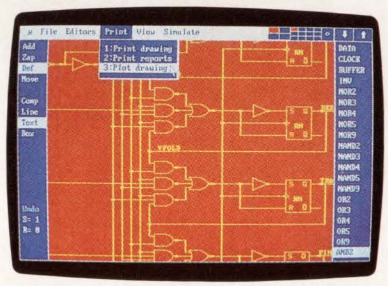

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CIRCLE NO 146

LISTING 1—LINEARIZATION PROGRAM

```
10 REM ********************************
20 REM
30 REM THERMISTOR LINEARIZATION PROGRAM
40 REM COPYRIGHT 1986 MICK MURRAY
50 REM LAB-LINE INSTRUMENTS, INC.
60 REM MELROSE PARK, IL. 60160
70 REM
80 REM ********************************
90 A$=STRING$(70,"*")
100 FOR T=1 TO 24:PRINT:NEXT
110 INPUT"INPUT LOW TEMPERATURE:";L
120 INPUT"INPUT LOW TEMP RESISTANCE:";RL
130 INPUT"INPUT HIGH TEMPERATURE:";H
140 INPUT"INPUT HIGH TEMP RESISTANCE:";RH
150 M=((H-L)/2)+L
160 PRINT"THE CALCULATED MID-POINT TEMPERATURE = ";M;"DEGREES."
170 PRINT"INPUT THERMISTOR RESISTANCE AT ";M;" DEGREES:";
180 INPUT RM:ST=1000
190 REM DE=DELTA, ST=STORE
200 PRINT A$:PRINT:PRINT
210 DIM A(96):DIM B(96)
220 FOR X=1 TO 96:READ A(X):B(X)=A(X):NEXT X
230 FOR I=1 TO 96
240   FOR J=1 TO 96
250     LO=((RL+A(I))*B(J))/(RL+A(I)+B(J))
260     MI=((RM+A(I))*B(J))/(RM+A(I)+B(J))
270     HI=((RH+A(I))*B(J))/(RH+A(I)+B(J))
280     X=ABS(HI-MI)
290     X1=ABS(MI-LO)
300     DE=ABS(X1-X)
310     IF DE<=ST THEN ST = DE:RS=A(I):R=B(J):GOSUB 380
320   NEXT J
330 NEXT I
340 IF SD=0 THEN GOTO 580
350 PRINT" END OF CALCULATIONS."
360 PRINT CHR$(7);:FORP=1TO1000:NEXT:GOTO360
370 END
380 PRINT"BEST SO FAR:"
390 PRINT"RS =";A(I);"OHMS, AND R =";B(J);"OHMS."
400 PRINT"   *** (AT";L;"DEGREES, Rth=";LO;"OHMS.)"
410 PRINT"   *** (AT";M;"DEGREES, Rth=";MI;"OHMS.)"
420 PRINT"   *** (AT";H;"DEGREES, Rth=";HI;"OHMS.)"
430 PRINT"DELTA1 =";X;"OHMS, AND DELTA2=";X1;"OHMS."
440 HL=ABS(HI-LO)
450 PRINT"THE TOTAL CHANGE IN RESISTANCE FROM";L;"TO";H;"DEGREES IS";HL;"OHMS."
460 PRINT:PRINT A$:PRINT"Working...":PRINT
470 RETURN
480 DATA 1.00,1.02,1.05,1.07,1.10,1.13,1.15,1.18,1.21,1.24
490 DATA 1.27,1.30,1.33,1.37,1.40,1.43,1.47,1.50,1.54,1.58
500 DATA 1.62,1.65,1.69,1.74,1.78,1.82,1.87,1.91,1.96,2.00
510 DATA 2.05,2.10,2.15,2.21,2.26,2.32,2.37,2.43,2.49,2.55
520 DATA 2.61,2.67,2.74,2.80,2.87,2.94,3.01,3.09,3.16,3.24,3.32
530 DATA 3.40,3.48,3.57,3.65,3.74,3.83,3.92,4.02,4.12,4.22,4.32,4.42
540 DATA 4.53,4.64,4.75,4.87,4.99,5.11,5.23,5.36,5.49,5.62,5.76,5.9
550 DATA 6.04,6.19,6.34,6.49,6.65,6.81,6.98,7.15,7.32,7.5,7.68,7.87
560 DATA 8.06,8.25,8.45,8.66,8.87,9.09,9.31,9.53,9.76
570 REM THE FOLLOWING IS FOR THE SECOND DECADE OF RS VALUES:
580 SD=1:RESTORE
590 FOR N=1 TO 96
600  READ A(N):B(N)=A(N):A(N)=10*A(N)
610 NEXT N:GOTO230
```

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CIRCLE NO 145

With each iteration, the program checks the network resistance R_{EQ} at the low, middle, and high temperatures. It seeks to achieve an equal resistance change in the upper and lower halves of the temperature range by trying all combinations of R and RS by substituting values from the data statements. It prints a result, searches for a better result, prints that, and continues (**Fig 2**). Remember to denormalize the final result by multiplying the resistance values by 1k. Typical execution time is about 10 minutes. **EDN**

To Vote For This Design, Circle No 748

```
INPUT LOW TEMPERATURE: 20
INPUT LOW TEMP RESISTANCE: 127
INPUT HIGH TEMPERATURE: 130
INPUT HIGH TEMPERATURE RESISTANCE: 2.64
THE CALCULATED MID-POINT TEMPERATURE = 75 DEGREES.
INPUT THERMISTOR RESISTANCE AT 75 DEGREES: 12.96
★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★
BEST SO FAR:
RS = 1 OHMS, AND R = 1 OHMS.
   ★★★ (AT 20 DEGREES, REQ = .9922482 OHMS.)
   ★★★ (AT 75 DEGREES, REQ = .9331552 OHMS.)
   ★★★ (AT 130 DEGREES, REQ = .7844828 OHMS.)
DELTA1 = .1486723 OHMS, AND DELTA2= .059093 OHMS.
THE TOTAL CHANGE IN RESISTANCE FROM 20 TO 130 DEGREES IS .2077653 OHMS.

★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★
                                  •
                                  •
                                  •
                          (12 ITERATIONS)
                                  •
                                  •
                                  •
★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★
Working. . .
BEST SO FAR:
RS = 8.66 OHMS, AND R = 1.07 OHMS.
   ★★★ (AT 20 DEGREES, REQ = 1.061627 OHMS.)
   ★★★ (AT 75 DEGREES, REQ = 1.019542 OHMS.)
   ★★★ (AT 130 DEGREES, REQ = .9774454 OHMS.)
DELTA1 = .0420962 OHMS, AND DELTA2= .04208481 OHMS.
THE TOTAL CHANGE IN RESISTANCE FROM 20 TO 130 DEGREES IS .08418102 OHMS.

★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★★
Working. . .
END OF CALCULATIONS.
```

Fig 2—This example of Listing 1's output *shows two of the 14 iterations that the program prints in determining the* R_{EQ} *network in* ***Fig 1****.* *R=1.07 kΩ and RS=8.66 kΩ are the final values.*

Circuit converts 7-segment code to decimal

P Mazumder
University of Illinois, Urbana, IL

The 3-IC circuit in **Fig 1** accepts 7-segment input code representing either of two commonly used numeric-character sets, converts it to an intermediate BCD code, and converts that to decimal code. The 7-segment code, defined in **Fig 2,** can be active high or active low. In addition, for convenience sake you can substitute exclusive-NOR (XNOR) gates for the exclusive-OR (XOR) gates shown.

Table 1 shows the active-high output (P_j) that corresponds to each 7-segment character in the two sets, along with the intermediate BCD code (ABCD) that

serves as the input to IC_3. Note that the BCD-to-decimal decoder IC_3 establishes a fixed relationship between ABCD and P_j, but for each character set a given character produces a different BCD code. The sets differ in their representation of "6" and "9": set #2 uses an extra segment for these characters.

Table 2 shows the connections you must make to implement each of the four possible sets of input code (character set #1, active high or low; character set #2, active high or low). You connect the signals for segments f and g to IC_{1B} **(Fig 1)** for all code sets. Each of the remaining inputs (IN_1 through IN_8) connect to 0 (GND), to 1 (V_{CC}), or to one of the segment signals, as shown in **Table 2.**

The XOR gates convert the applied 7-segment code to active-high BCD code. **Table 3** depicts the logical composition of each bit in the BCD code for each of the four possible input-code sets, using either XOR gates (top half of **Table 3**) or XNOR gates (bottom half).

Note that if you build the circuit with XNOR gates, IN_3 is the only input affected; the reason is that you make the opposite connections to IN_3 (V_{CC} as opposed to GND). Also, note that you can eliminate any XOR gate for which one input is always low because the gate's output then follows the other input. **EDN**

To Vote For This Design, Circle No 749

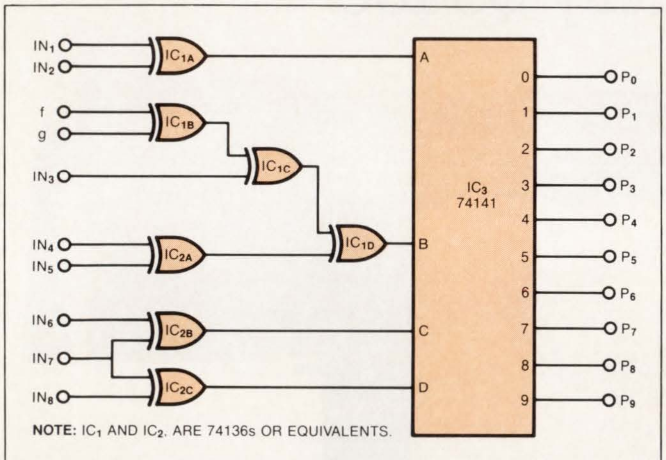

Fig 1—This 3-IC circuit converts 7-segment code *(either active-high or active-low for either of two numeric character sets) to decimal code.*

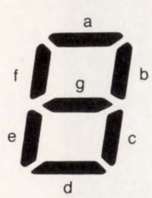

Fig 2—This standard character format *lets you represent numbers by selectively illuminating the seven segments labeled a through g.*

TABLE 1—CHARACTER SETS

CHARACTER SET #1	A	B	C	D	OUTPUT
0	0	0	0	0	P_0
1	0	0	1	0	P_4
2	1	0	0	0	P_1
3	1	0	0	1	P_9
4	1	0	1	0	P_5
5	0	0	0	1	P_8
6	1	1	0	0	P_3
7	1	1	1	0	P_7
8	0	1	0	0	P_2
9	0	1	1	0	P_6
CHARACTER SET #2	**A**	**B**	**C**	**D**	**OUTPUT**
0	1	1	0	0	P_3
1	1	0	0	1	P_9
2	0	1	0	0	P_2
3	0	0	1	0	P_4
4	0	0	0	1	P_8
5	1	1	1	0	P_7
6	1	0	0	0	P_1
7	1	0	1	0	P_5
8	0	0	0	0	P_0
9	0	1	1	0	P_6

TABLE 2—INPUT CODES

INPUT CODE	IN_1	IN_2	IN_3*	IN_4	IN_5	IN_6	IN_7	IN_8	GATES REQUIRED
CHARACTER SET #1 ACTIVE HIGH	a	f	1 (0)	a	b	1	d	e	7
CHARACTER SET #2 ACTIVE HIGH	b	g	0 (1)	d	e	e	a	1	6
CHARACTER SET #1 ACTIVE LOW	a	f	1 (0)	a	b	0	d	e	6
CHARACTER SET #2 ACTIVE LOW	b	g	0 (1)	d	e	e	a	0	5

*INPUTS IN PARENTHESES ARE FOR USE WITH XNOR GATES ONLY.

1 ≡ LOGIC 1 (V_{CC}); 0 ≡ LOGIC 0 (GND).

TABLE 3—LOGICAL MAKEUP OF BCD CODE

INPUT CODE	A	B	C	D
CHARACTER SET #1 ACTIVE 1	a ⊕ f	((f ⊕ g) ⊕ 1) ⊕ (a ⊕ b)	d ⊕ 1	d ⊕ e
CHARACTER SET #2 ACTIVE 1	b ⊕ g	(f ⊕ g) ⊕ (d ⊕ e)	e ⊕ a	a ⊕ 1
CHARACTER SET #1 ACTIVE 0	a ⊕ f	((f ⊕ g) ⊕ 1) ⊕ (a ⊕ b)	d	d ⊕ e
CHARACTER SET #2 ACTIVE 0	b ⊕ g	(f ⊕ g) ⊕ (d ⊕ e)	e ⊕ a	a
INPUT CODE	$\overline{A}$	$\overline{B}$	$\overline{C}$	$\overline{D}$
CHARACTER SET #1 ACTIVE 1	a ⊙ f	((f ⊙ g) ⊙ 0) ⊙ (a ⊙ b)	d	d ⊙ e
CHARACTER SET #2 ACTIVE 1	b ⊙ g	(f ⊙ g) ⊙ (d ⊙ e)	e ⊙ a	a
CHARACTER SET #1 ACTIVE 0	a ⊙ f	((f ⊙ g) ⊙ 0) ⊙ (a ⊙ b)	d ⊙ 0	d ⊙ e
CHARACTER SET #2 ACTIVE 0	b ⊙ g	(f ⊙ g) ⊙ (d ⊙ e)	e ⊙ a	a ⊙ 0

(⊕ MEANS EXCLUSIVE-OR; ⊙ MEANS EXCLUSIVE-NOR.)

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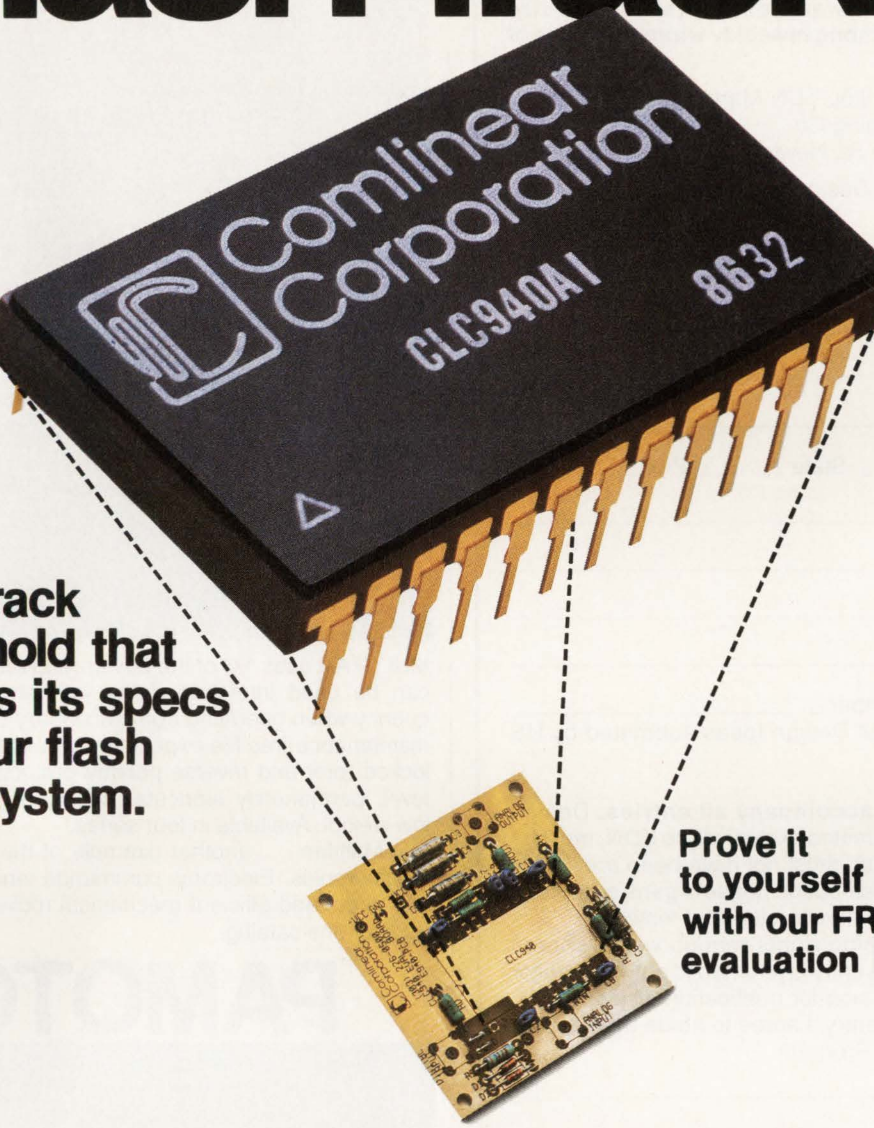

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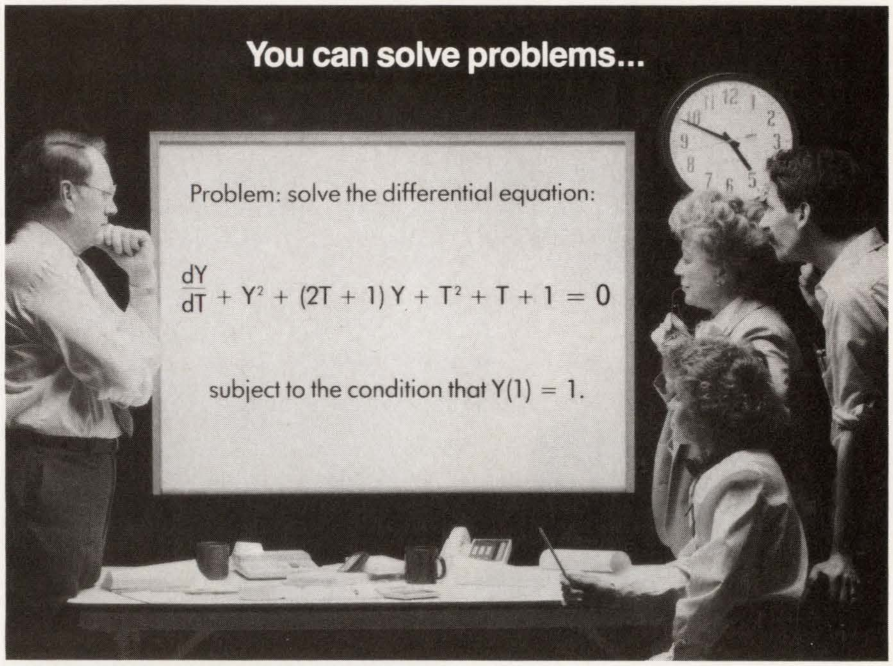

Symbolically...

(C1) DEPENDS(Y,T)$

(C2) DIFF (Y,T)+Y^2+(2*T+1)*Y+T^2+T+1;

(D2) $\frac{dY}{dT} + Y^2 + (2T + 1)Y + T^2 + T + 1$

(C3) SOLN:ODE(D2,Y,T);

(D3) $Y = -\frac{\%C\,T\,\%E^T - T - 1}{\%C\,\%E^T - 1}$

(C4) SOLVE(SUBST([Y=1, T=1],D3),%C),NUMER;

(D4) [%C = 0.5518192]

(C5) SPECIFIC_SOLN:SUBST(D4,SOLN);

(D5) $Y = -\frac{0.5518192\,T\,\%E^T - T - 1}{0.5518192\,\%E^T - 1}$

and Numerically.

```
(C6) FORTRAN(D5)$
        Y = -(0.5518192*T*EXP(T) - T - 1)
     1     /(0.5518192*EXP(T) - 1)
```

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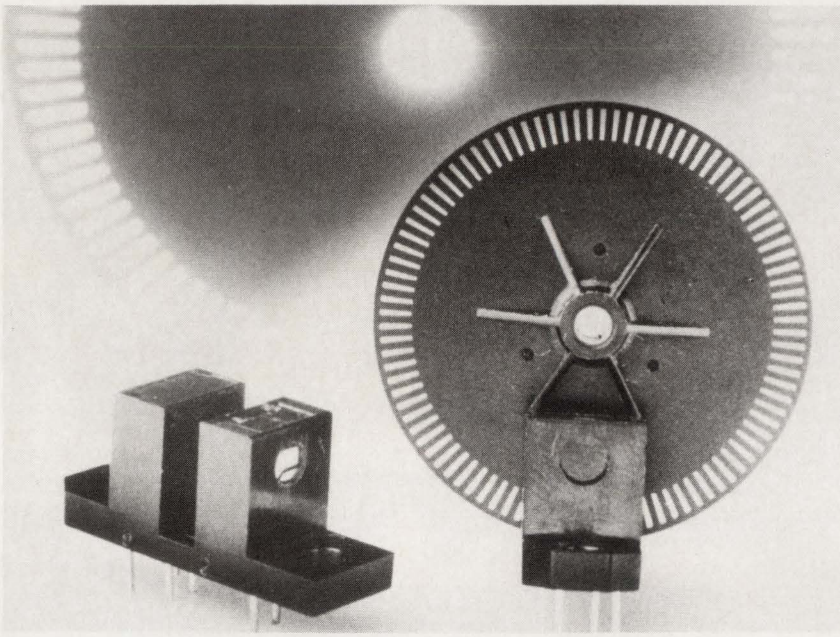

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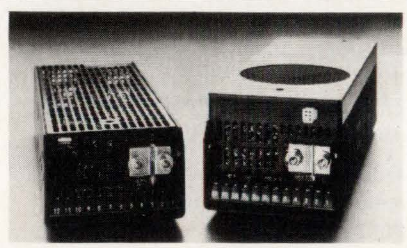
- *Main output delivers 80A*

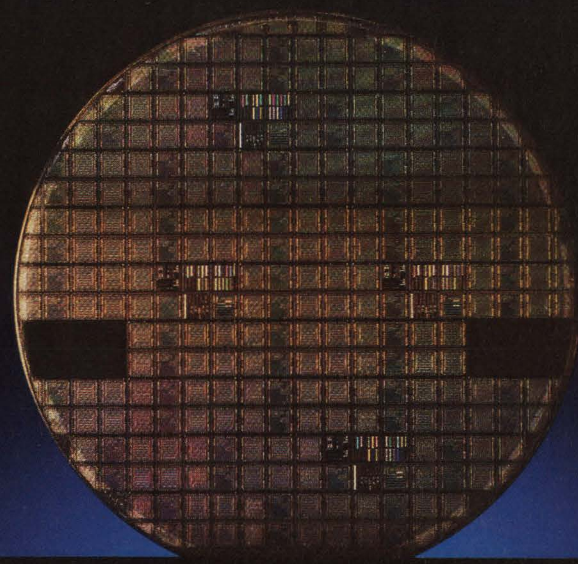
The QS-3 and QS-4 multioutput switching power supplies are UL, CSA, and TUV approved. They deliver 300 to 500W and feature as many as five fully regulated outputs. These power supplies have an 80A main ouput, three 6A auxiliary outputs, and one high-power auxiliary output (12A steady, 18A peak), which can handle the needs of applications requiring multiple Winchester disks or tape drives. Input features include jumper options for voltage-range selection, input-transient and surge-current limiting, and brownout protection. Output safety provisions include overload, overvoltage, and reverse-voltage protection. Efficiency is typically 75%, and the holdup time after loss of input power equals 20 msec. Remote on/off controls, a power-fail signal,thermal-shutdown capability, and an EMI safety cover are available as options. QS-3, $497; QS-4, $540 (100).



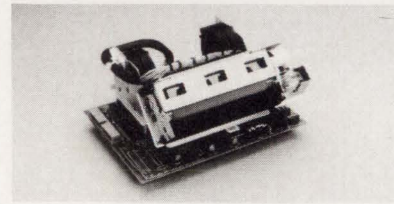
Cherokee International Inc, 8 Autry, Irvine, CA 92718. Phone (714) 951-9679. TWX 510-101-0493.

Circle No 354

Text continued on pg 232



COMPONENTS & POWER SUPPLIES



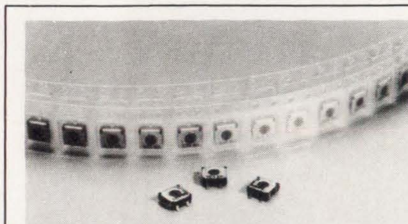
THERMAL PRINTERS

- *6-line/sec print speed*
- *Available in four configurations*

The MPX-404X Series of high-speed 42-column thermal printers consists of four configurations, each of which performs identically in terms of speed, print quality, and reliability. Each unit produces a print image at speeds approaching 6 lines/sec. The units print all upper- and lower-case ASCII letters, numbers, punctuation, and special symbols, as well as Epson-compatible, bit-image graphics. You can interject your own graphics symbols between data and text when appropriate. System options include a 7k-bit buffer (1k bit is standard), a battery-backed real-time clock, and an IEEE-488 interface. From $294 (OEM qty).

Memodyne Corp, 200 Reservoir St, Needham Heights, MA 02194. Phone (617) 444-7000. TWX 510-600-8774.

Circle No 355



SEALED TRIMMER

- *Withstands 260°C soldering temperatures for 10 sec*
- *−55 to +125°C operating range*

The ST-4 is a single-turn, sealed cermet trimmer that comes in both surface-mount and leaded packages and is available in three top-adjustment styles. The unit can withstand reflow-soldering temperatures of

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CIRCLE NO 169

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260°C for 10 sec. Trimmers in the series cover the resistance range 10Ω to 2 MΩ, and the operating range is −55 to +125°C. The trimmer is rated for 250 mW at 70°C and can accommodate 200V dc. The rotational life specs at 100 cycles. Sealed with an O-ring, the trimmer passes leak tests at 85°C and tolerates exposure to a 125°C temperature for 250 hours. $1.05 (5000). Delivery, eight to 12 weeks ARO.

Mepcopal, 11468 Sorrento Valley Rd, San Diego, CA 92121. Phone (619) 453-0332.

Circle No 356

DATA TERMINAL

- *Accepts data manually or through automatic interfaces*
- *Features a back-lit LCD*

The TM8450 microterminal accepts data manually or through automatic identification interfaces, such as bar-code wands, laser scanners, and magnetic stripe readers. The base unit features a backlit LCD and an elastomeric keyboard. Eight of the keys on the 23-position numeric keyboard can be programmed to handle as many as 16 separate functions each. Three plug-in modules—"communications," "peripheral," and "auxiliary"—expand the capabilities of the basic terminal. The 8450 can operate in four modes. You can use it as a simple display, to send and receive block-mode data, with other data terminals in a multidrop system, or as a trouble-shooting and diagnostics communications monitor. Using the function keys, you can establish operational modes, baud rates, protocols, and other parameters interactively at initial setup time. Prompts (in French, German, or English) guide you through the selections; they are then stored in local, battery-backed memory. $795.

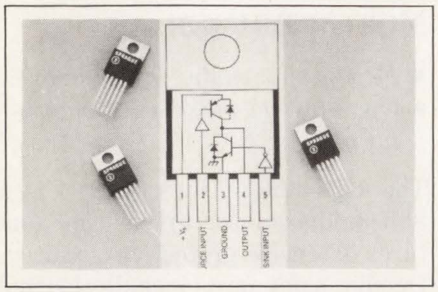
Burr-Brown Corp, Box 11400, Tucson, AZ 85734. Phone (602) 746-1111. TLX 666491. TWX 910-952-1111.

Circle No 357

MOTOR DRIVER

- *Features extensive protection*
- *Operates via pulse-width modulation*

The UDN-2943Z interface IC is a half-bridge motor driver that features extensive protective circuitry. On-chip safeguards include thermal shutdown, overvoltage shutdown,



crossover-current protection, short-circuit protection, transient suppression, and input-logic lockout, which prevents source drivers and sink drivers from turning on simultaneously. The motor driver operates via pulse-width modulation, and it has saturated outputs. The 24V/1A bipolar device is available in a modified 5-lead, power-tab, TO-220 plastic package. $1.35 (100). Delivery, 10 to 12 weeks ARO.

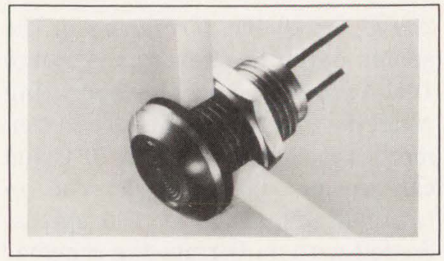
Sprague Electric Co, Technical Literature Service, Box 9102, Mansfield, MA 02048. Phone (617) 853-5000.

Circle No 358

PANEL LAMP

- *Incorporates a red/green LED*
- *Includes a Fresnel lens to improve light output*

Sealed to withstand environmental conditions in excess of those specified by the IP67 standard, the MPL34 2-color LED panel lamp is suitable for use in military or portable equipment. The panel lamp incorporates a high-intensity red/green LED, and it has a low-profile Fresnel lens assembly to maximize light output. It's available in two versions, each specifying a different brightness level. The panel lamp has a metal body and fixes to the panel with a sealing washer, lock washer, and nut. You can order lamps with either a black or an anodized aluminum bezel finish. The lamp's terminals accept soldered, wire-wrapped, or push-fit connections. The lamps meet the requirements of BS-5420 and have an operating and storage



temperature range of −30 to +85°C. $3.80.

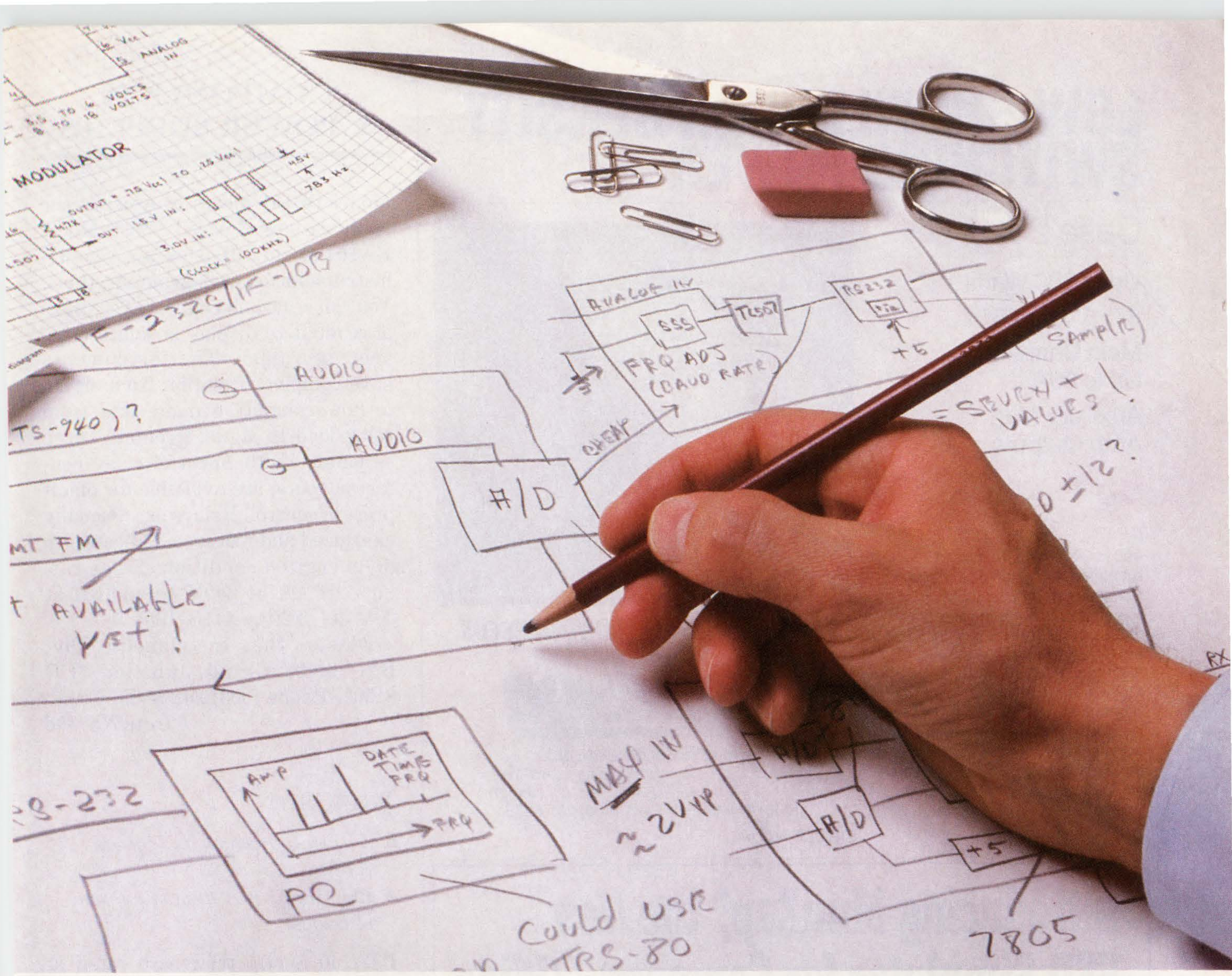
Marl International Ltd, Ulverston, Cumbria LA12 7RY, UK. Phone (0229) 52430. TLX 65100.

Circle No 359

BARGRAPHS

- *Version meets ANSI C39.1 specs*
- *Completely isolated design*

Models BA010 and BB101 bargraphs consist of 101 LED segments and an optional 4-digit display for enhanced accuracy and resolution of the process variable.



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VideoLog Communications, 50 Washington Street, Norwalk, CT. 06854

CIRCLE NO 171

COMPONENTS & POWER SUPPLIES

Model BB101 meets or exceeds the specifications of ANSI C39.1; Model BA101 is qualified as a Class 1E instrument for nuclear applications. You can scale and calibrate the digital readout to display absolute engineering values. The instruments have complete isolation from signal to power-supply ground, and from relay load to signal ground. Three setpoints, with Form C relay contact outputs, are available for on/off process control. Relays are normally energized and feature a fail-safe to a de-energized condition. Relay ratings are 2A at 250V ac and 3A at 30V dc. $229 to $415 (100).

Dixson Inc, Instruments Div, Box 1449, Grand Junction, CO 81502. Phone (303) 242-8863.

Circle No 396

TRIACS

- *Withstand surges as high as 200A*
- *Require 35 mA of gate current to trigger*

BTA140 Series triacs are rated at 25A rms, but can withstand current surges as high as 200A in 60-Hz applications or 180A in 50-Hz applications. They are available with voltage ratings of 500, 600, and 800V and require a minimum gate current of 35 mA to trigger. The triacs are glass passivated using a proprietary passivation technique, which improves device reliability, and they are encapsulated in TO-220 packages. Approximately $0.90 (10,000). Delivery, 12 weeks ARO.

Philips, Elcoma Div, Box 523, 5600 AM Eindhoven, The Netherlands. Phone (040) 757005. TLX 51573.

Circle No 397

Amperex Electronic Corp, George Washington Hwy, Smithfield, RI 02917. Phone (401) 232-0500.

Circle No 398

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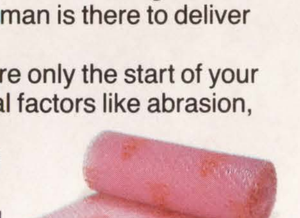

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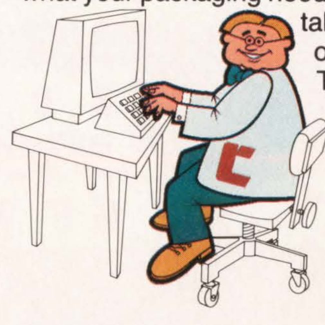

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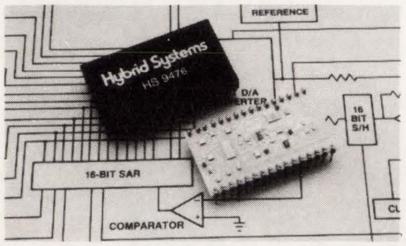


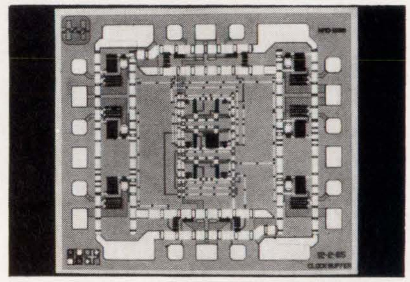
A/D CONVERTER

- *Includes sample/hold amplifier*
- *Takes 50k samples/sec with 0.003% accuracy*

According to its manufacturer, the HS 9476 is the first hybrid 16-bit A/D converter to include an S/H amplifier in the package. The combination supports typical conversion rates as high as 50k samples/sec with 14-bit resolution and 45.4k samples/sec with 16-bit resolution. At 14-bit resolution, the device specifications guarantee no missing codes over the operating range 0 to 70°C. Input ranges include ±5V, ±10V, 0 to 10V, and 0 to 20V. Other specs include an integral linearity error of 0.003% full-scale resolution (FSR), a differential linearity of 0.006% FSR max, and gain and linearity drifts of ±2 ppm/°C max. The HS 9476 operates from ±15V and 5V supplies, consumes 1520 mW max, and is pin compatible with the HS 9576, the Burr Brown ADC 76, and the Analog Devices 376. The package is a 32-pin DIP. HS 9476J, $180 (100). Delivery, four to six weeks ARO.

Hybrid Systems Corp, 22 Linnell Circle, Billerica, MA 01821. Phone (617) 667-8700. TWX 710-347-1575.

Circle No 361



GaAs BUFFER

- *ECL-compatible GaAs I/O device*
- *1.8-GHz input clock speed*

The HMD-11188-2 is a GaAs dual-clock-driver/fan-out buffer that's ECL compatible but four times faster than equivalent ECL devices. The buffer features a 1.8-GHz clock speed and a 800-psec typ propagation delay. Quad outputs provide fan-out to four 50Ω transmission lines with less than 50 psec of skew among them. A mode control lets you complement these outputs, and a third input lets you enable and disable the output data. A second driver circuit, independent of the first, provides a noninverting fan-out of two outputs. The buffer operates within the range of −55 to +85°C and comes in a 16-pin hermetic flatpack. $155 (100). Delivery, six weeks ARO.

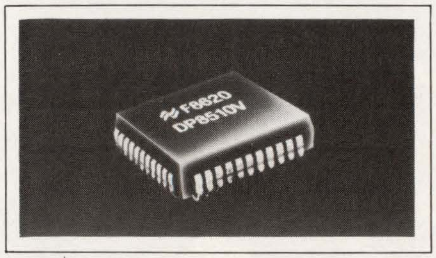
Harris Microwave Semiconductor, 1530 McCarthy Blvd, Milpitas, CA 95035. Phone (408) 262-2222. TWX 910-338-2247.

Circle No 362

GRAPHICS PROCESSOR

- *20-MHz operation*
- *Compatible with static, dynamic, and video RAMs*

The DP8510 is a slave processor that controls all data movement to and



from the bit-mapped memory planes of a multicolor graphics system. Suitable for video graphics and printer applications, the device can achieve a resolution as high as 16k×16k pixels. With one DP8510 dedicated to each pixel plane, a single raster-graphics processor can process a large number of planes simultaneously. The 20-MHz device uses pipelined logic to implement 16 data operations, including shifting and masking. The IC comes in a 44-pin plastic leaded chip carrier (PLCC) and is fabricated with a 2-μm CMOS process. It's compatible with static, dynamic, and video RAMs. You can control the processor with other members of the company's graphics chip set or with a general-purpose μP. $10 (1000).

National Semiconductor Corp, Box 58090, Santa Clara, CA 95052. Phone (408) 749-7421. TLX 346353. TWX 910-339-9240.

Circle No 363

GRAPHICS CHIP

- *Supports display resolution to 2k×2k pixels*
- *Can draw 120,000 vectors/sec*

The Am95C60 quad-pixel data-flow manager (QPDM) allows the integration of text and graphics in bit-mapped graphics systems, and it supports displays with resolutions as high as 2k×2k pixels. The maximum clock speed is 20 MHz. The QPDM can draw 120,000 vectors/sec, place 50,000 characters of text/sec, and fill polygons at a rate of one pixel every 50 nsec. The QPDM also

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CIRCLE NO 176

supports windowing, zooming, panning, and scrolling, as well as the drawing of vectors, circles, and arcs with user-defined line styles. Fully cascadable, the QPDM can handle as many as 256 memory planes without loss of performance. The CMOS device is compatible with 8-, 16-, and 32-bit buses. It comes in a 144-pin pin-grid array. 16-MHz version, $250; 20-MHz version, $278.57 (100).

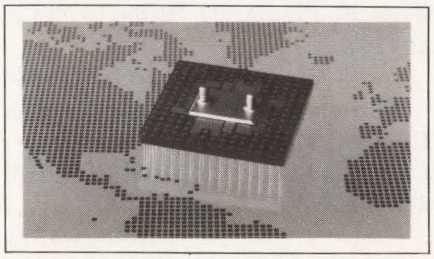
Advanced Micro Devices Inc, Box 3453, Sunnyvale, CA 94088. Phone (408) 732-2400.

Circle No 364

DIGITAL OSCILLATOR

- *Synthesizes frequencies from 1 Hz to 120 MHz*
- *ECL-compatible outputs and TTL-compatible inputs*

When used with a suitable D/A converter, the STI-2172 digital oscillator's 8-bit digital output can gener-



ate sine-wave frequencies from 1 Hz to more than 120 MHz. This monolithic device has TTL-compatible inputs, ECL-compatible outputs, and an internal oscillator that operates at frequencies as high as 300 MHz. You can program the output to 32-bit (almost 1 Hz) resolution, and you can change frequencies as often as every 110 nsec. The package is a 156-pin ceramic pin-grid-array device with heat-sink mounting studs. $625 (100).

Stanford Telecommunications Inc, 2421 Mission College Blvd, Santa Clara, CA 95054. Phone (408) 980-5684.

Circle No 365

EPROM

- *Organized as 64k×16 bits*
- *Planned availability as a one-time-programmable device*

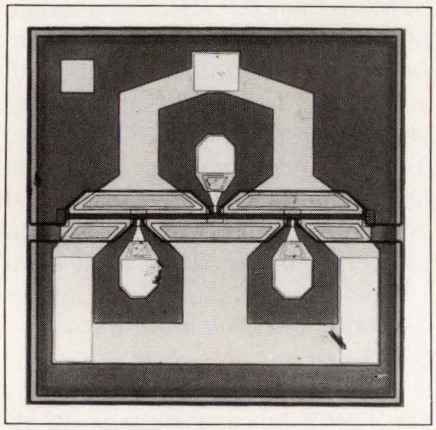
The TS27C1024 is a 1M-bit UV-erasable EPROM organized as 64k×16 bits. This CMOS EPROM is available with access times ranging from 120 to 250 nsec and consumes a maximum of 50 mA from its 5V supply. Its programming voltage is 12.5V. The device contains its own electronic signature so that PROM programmers can automatically identify the part; suitable programmers can program an entire device in approximately 30 sec. The part is available enclosed in a 40-pin ceramic DIP or in a 44-pin plastic leaded chip carrier, and soon it'll be available as a one-time-programmable part in a plastic package. Approximately $25 (1000).

Thomson Semiconducteurs, 43 Ave de l'Europe, 78140 Velizy, France. Phone (1) 39469719. TLX 204780.

Circle No 366

Thomson Components-Mostek Corp, 1310 Electronics Dr, Carrollton, TX 75006. Phone (214) 466-6000.

Circle No 375



GaAs MESFET

- *Provides 60-GHz operation*
- *Offers 16-dB gain at 12 GHz*

The NE250 is a dual-gate, small-signal GaAs metal-semiconductor FET (MESFET) that features silicon-nitride passivation, gold metallization, and an f_{MAX} of 60 GHz. The device offers a 16-dB gain at 12 GHz with a noise figure of 2.7 dB. In AGC-amplifier applications at 12 GHz, the FET provides 40 dB of signal control. $49.50 (100).

California Eastern Laboratories, 3260 Jay St, Santa Clara, CA 95054. Phone (408) 988-3500.

Circle No 367

FIFO MEMORY

- *Organized as 512×9 bits for 8-bit data plus a parity or control bit*
- *FIFO data width and depth is expandable*

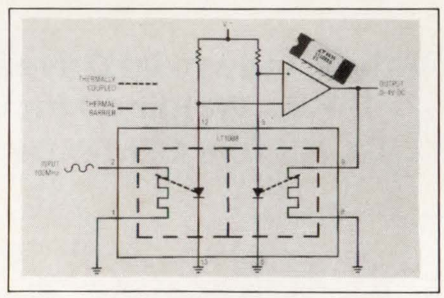
Providing asynchronous data transfer between digital systems, the MA7001 512×9-bit FIFO memory allows you to write and read FIFO data simultaneously. It has an access time of 55 nsec and a read/write cycle time of 75 nsec. FIFO-full and FIFO-empty flag outputs allow you to avoid data overflow or underflow, and a retransmit feature allows you to reset the read pointer to its initial value so that you can retransmit the data contained in the FIFO. Expansion logic in the device allows you to expand a FIFO system's word size or depth by using multiple devices. The FIFO memory is fabricated using fully static silicon-on-sapphire (SOS) CMOS technology. It's pin compatible with the MK4501 and IDT7201 FIFOs and comes in a 28-pin LCC or DIP. £18 (100).

Marconi Electronic Devices Ltd, IC Div, Lincoln Industrial Park, Doddington Rd, Lincoln LN6 3LF, UK. Phone (0522) 688121. TLX 56380.

Circle No 368

Marconi Electronic Devices Inc, 80 Smith St, East Farmingdale, NY 11735. Phone (516) 756-1900.

Circle No 376



RMS-TO-DC CONVERTER

- *Wideband, 300-MHz operation*
- *Converts rms voltages as high as 9.5V*

The LT1088 is a thermal-type rms-to-dc converter that comes in a 14-pin, side-brazed DIP, assembled with proprietary techniques to achieve the required thermal characteristics. The converter accepts rms voltages as high as 9.5V at frequencies as high as 300 MHz, and it provides an equivalent dc output voltage. It offers a 20:1 dynamic range and handles crest factors as high as 50:1. Its accuracy is 1% from dc to 50 MHz and 2% at 100 MHz. Thermal resistance between the converter's input and output sec-

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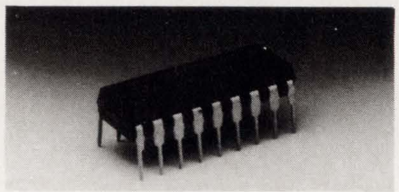
tions is 2500°C/W; from either section to ambient it's 300°C/W. Thermal and electrical matching between the sections is specified. The converter comes in two input versions: 50Ω (4.25V FS) and 250Ω (9.5V FS). $28.65 (100).

Linear Technology Corp, 1630 McCarthy Blvd, Milpitas, CA 95035. Phone (408) 942-0810. TLX 172110.

Circle No 369



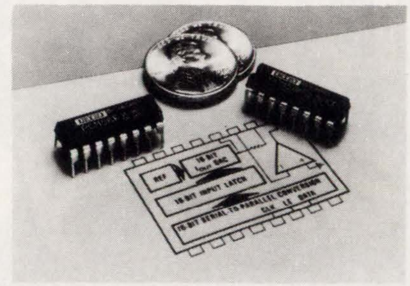
DYNAMIC RAMs

- *Row access as fast as 100 nsec*
- *Access random pixels in 50 nsec*

The MB81C1000 and MB81C1001 are 1M-bit CMOS dynamic RAMs that offer page access and nibble access, respectively. Both RAMs have a 1M×1-bit organization and provide row-access times of 100, 120, or 150 nsec. Power consumption is less than one-fifth that of four 256k-bit dynamic RAMs. The MB81C1000's page mode allows access to random bits in a single row of the memory in 50 nsec. Similarly, the MB81C1001's nibble mode gives serial access to as many as four data bits at 20 nsec/bit. Each memory cell is a 3-D stacked capacitor whose large capacitance allows refresh cycles to be as brief as 8 msec. The cell structure also improves the immunity to soft errors induced by alpha radiation. Package options include JEDEC 18-pin plastic and ceramic DIPs, a 20-lead plastic ZIP, and a 20-lead plastic small-outline J-bend (SOJ) package for surface-mount applications. 150-nsec version, $35 (50).

Fujitsu Microelectronics Inc, Integrated Circuits Div, 3320 Scott Blvd, Santa Clara, CA 95054. Phone (408) 727-1700. TWX 910-338-0190.

Circle No 370



D/A CONVERTER

- *Monolithic construction*
- *16-bit resolution*

Suitable for use in compact-disk players, the 16-bit, serial-input PCM56P is a complete D/A converter that includes a zener voltage reference, thin-film resistors, current switches, and a high-speed, low-noise-output op amp. The converter's output voltage settles to within ±0.006% FSR in 1.5 μsec, and the maximum total-harmonic distortion is 0.0025%. The unit is monotonic to a 15-bit resolution and dissipates only 260 mW max when operating from 5V supplies. The device can also operate from ±12V supplies. It comes in a 16-pin plastic DIP. Based on preliminary data, the estimated MTBF is three million hours at 35°C. $12 (100).

Burr-Brown Corp, Box 11400, Tucson, AZ 85734. Phone (602) 746-1111. TLX 666491. TWX 910-952-1111.

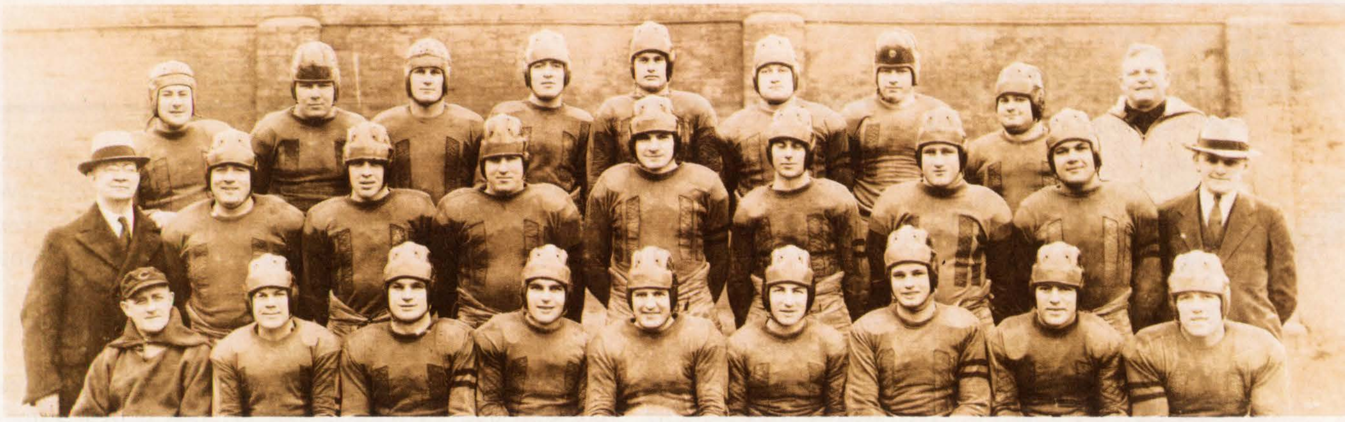
Circle No 371

FIFOs

- *Organized as 64×9 bits; burst rates as high as 40 MHz*
- *Cascadable to produce FIFOs of greater width or depth*

Suited for use as a data buffer between asynchronous systems, the 74HC7030 and 74HCT7030 64×9-bit FIFO memories have independent shift-in and shift-out controls, which allow you to perform synchronous or asynchronous data transfers at data rates as high as 25 MHz. For short bursts of data you can transmit at frequencies as high as 40 MHz. In-

Text continued on pg 252



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A ☐ Circuit/System Packaging
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C ☐ Production/Manufacturing
D ☐ Quality Control, Test & Inspection
E ☐ Purchasing
F ☐ Corporate Management
G ☐ Sales
H ☐ Research/Development
I ☐ Other

Business Category (Check only one)
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B ☐ Office or Business Machine
C ☐ Communications, Systems/Equipment
D ☐ Industrial Electronic Control Systems/Equipment
E ☐ Medical Electronics
F ☐ Aircraft, Missiles, Space, Military
G ☐ Test and Measurement Equipment, Inst.
H ☐ Electronic Components and Sub-Assemblies
I ☐ Consumer Electronic Products
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L ☐ Contract Manufacturing
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B1

put-ready and output-ready status signals indicate the full or empty condition of the FIFO. The devices have 3-state outputs that you can cascade to produce FIFOs with increased word width or FIFO depth. They come in 28-pin DIPs or small-outline packages for surface mounting. Corresponding input and output pins are positioned opposite each other on the package to ease pc-board layout. The 74HC7030 has CMOS-compatible inputs and outputs, and the 74HCT7030 has TTL-compatible inputs and outputs. Approximately $21 for samples.

Philips, Elcoma Div, Box 523, 5600 AM Eindhoven, The Netherlands. Phone (040) 757005. TLX 51573.

Circle No 372

Signetics Corp, 811 E Arques Ave, Sunnyvale, CA 94088. Phone (408) 991-4571.

Circle No 377

VIDEO DAC

- *Includes three 4-bit video D/A converters*
- *Supports pixel rate of 125 MHz min*

With the addition of a few external components, the monolithic MC10320 provides the complete interface between a color monitor and its controlling computer. The device contains three 4-bit video D/A converters, a 12-bit×16-location color palette (RAM), a voltage reference, and the necessary latches. The chip is compatible with most digital systems because the input and output circuits have separate power-supply terminals; you can connect a +5 or −5V supply to accommodate either TTL or ECL. Specs include a guaranteed 125-MHz pixel rate, 750-mW typ power dissipation, a glitch area of 20 pV/sec, and a 3-nsec settling time. Differential and integral nonlinearity errors are ±¼ LSB. $46.08 (1000).

Motorola Inc, Semiconductor Products Sector, Box 52073, Phoenix, AZ 85072. Phone (602) 897-3872.

Circle No 373

SYNCHRO CONVERTER

- *Represents angles with ±6 arc-minute accuracy*
- *Accepts synchro or resolver inputs*

The SBC40 is one of a series of 3- or 4-decade synchro-to-BCD converter modules, suitable for mounting on pc boards. The modules measure 2.6×3.1×0.82 in. Versions accept 11.8 or 90V inputs at 400 Hz or 90V inputs at 60 Hz, and they produce 3- or 4-decade BCD output data with ±6 or ±30 arc-minute accuracy. Operating temperature ranges are 0 to 70°C and −55 to +85°C. Each converter has an isolated ac reference and synchro input and an optional zero-offset adjustment. $375 (OEM qty).

Computer Conversions Corp, 6 Dunton Ct, East Northport, NY 11731. Phone (516) 261-3300.

Circle No 374

THE BEST *Schematic Capture* IS ONLY $495

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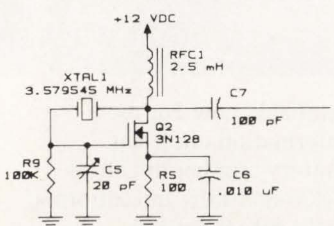

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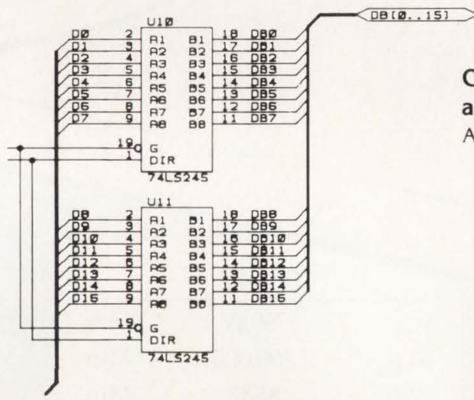

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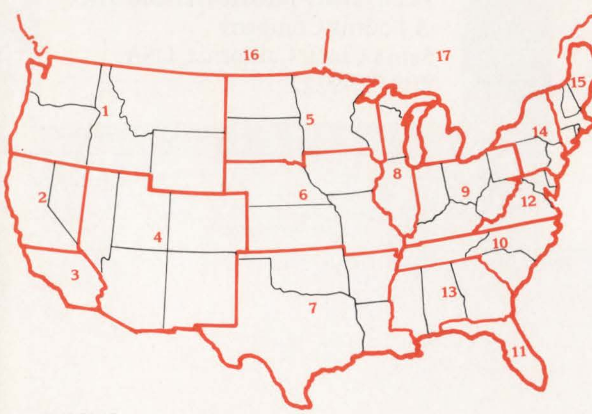

Contact your OrCAD Representative For Further Information

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503-627-0716

2. N. CA, Reno NV
Elcor Associates, Inc.
408-980-8868

3. So. CA
Advanced Digital Group
714-897-0319

4. Las Vegas, NV, UT, AZ, NM
Tusar Corporation
602-998-3688

5. ND, SD, MN, W. WI
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Beta Lambda, Inc.
201-446-1100

15. CT, RI, MA, VT, NH, ME
DGA Associates, Inc.
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16. BC, AB, SK, MB
Interworld Electronics &
Computer Industries, Ltd.
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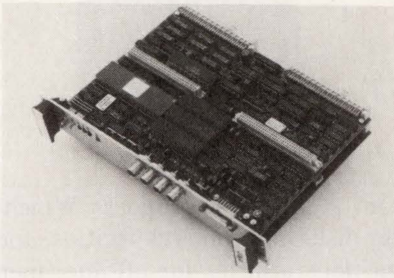
CIRCLE NO 180

COMPUTERS & PERIPHERALS



CRT CONTROLLER

- *Works with VME Bus*
- *Optional GKS-compatible software*

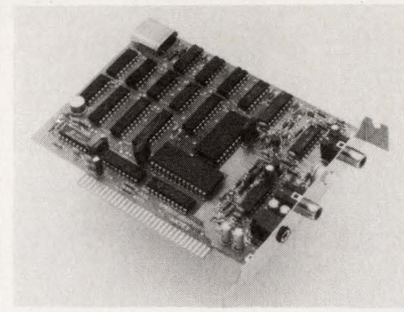
The AGC-1 graphics controller card is a VME Bus board that gives you a choice of 16 or 256 displayed colors from a palette of 16 million. The board can display 16 colors within a 1600×1280-pixel display or 256 colors within a 1160×870-pixel display. It works with CRT displays that have video bandwidths between 32 and 64 MHz. The board offers hardware zoom; vertical and horizontal smooth scroll by pixel; clipping; blinking; and conditional blinking. Its commands include Line, Rectangle, Polyline, Polygon, Circle, Ellipse, Paint, and Copy. Because you can access the 2M bytes of dual-ported video RAM directly from the VME Bus, you can update the display at the board's graphics coprocessor's maximum rate. The optional software, GKSral, provides GKS-compatible graphics functions. AGC-1, $5995; GKSral, $1990.

Force Computers Inc, 727 University Ave, Los Gatos, CA 95030. Phone (408) 354-3410.

Circle No 378

VOICE PROCESSOR

- *Runs on the IBM PC*
- *Digitizes speech or music*



The VP 600 voice processor converts audio input into a digital format for storage on a computer disk. This single-channel unit comes on a half-size IBM PC board. It requires 400 mA at 5V dc, 10 mA at −5V dc, and 30 mA at 12V dc. The card accepts standard electret microphone-level or 1V rms cassette-level signals and adjusts them for A/D conversion and for digital encoding via adaptive, differential PCM. The PC can then store the encoded signal on disk. The 20-Hz to 3.5-kHz processor has a 48-dB dynamic range and a 4- or 8-kHz sample rate. When you use a 4-kHz sample rate, the board requires 7.2M bytes to store one hour of digitized signal. $345.

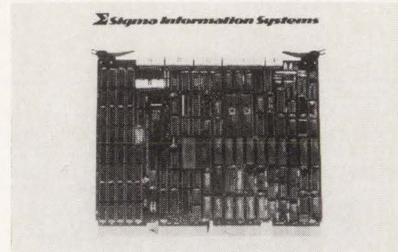
Antex Electronics Corp, 16100 S Figueroa St, Gardena, CA 90248. Phone (213) 532-3092. TWX 910-344-7381.

Circle No 379

Q BUS CARD

- *Q Bus-to-ESDI disk controller*
- *Supports Winchesters of various capacities*

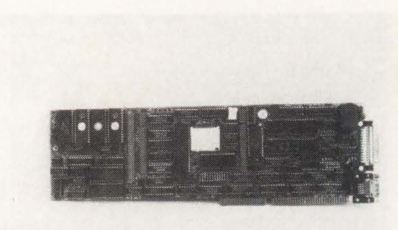
The SDC-RQD11-EC quad-height disk controller provides an interface between four ESDI drives and the Q Bus of a MicroVAX or LSI-11 sys-



tem. The board supports Winchester disks of various capacities, and it includes utilities for off-line, menu-driven formatting and diagnostics. It also has 1M byte of cache memory. Because disk and Q Bus transfers can occur simultaneously, access times for blocks within the cache memory can be as short as 2.5 msec. You can program the controller to perform look-ahead read operations in anticipation of data requests. You can also read an entire track into cache memory so that it's ready for access to the host. The controller supports the following operating systems: RT-11 V5, RSX-11M+ V2, TSX+ V5, RSTS/E V9, MicroVMS V4 or later versions, and various Unix versions. $1325.

Sigma Information Systems, 3401 E La Palma Ave, Anaheim, CA 92806. Phone (714) 630-6553. TLX 298607.

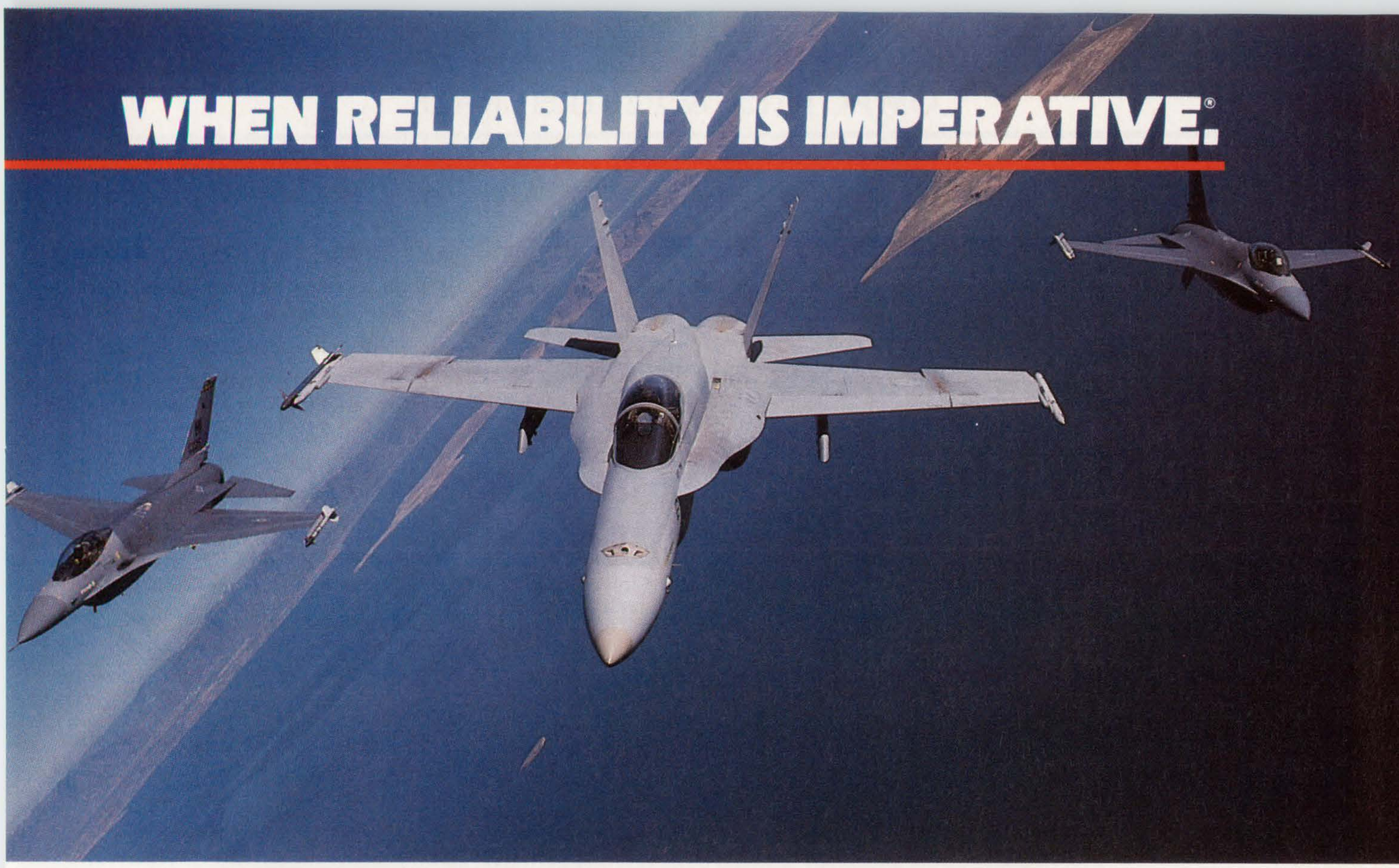
Circle No 380



PC ADD-IN CARD

- *Provides CPU and real-time multitasking operating system*
- *Communicates with PC via shared memory*

Offering real-time multitasking capabilities for industrial control, the DRTI add-in card for IBM PCs,



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Abbott's new M25 exceeds the performance of one of the best selling mil-spec power supplies; our own VN25. Our VN25 has been widely used in critical naval and airborne applications for over 10 years. Now the M25 offers higher performance in this proven design.

Higher Density. *The M25 has a 1¼ inch lower profile than our VN25 while maintaining the same footprint. This adds up to a* ***45% reduction*** *in volume.*

Better Specs. *By doubling the switching frequency, our M25 is 10% more efficient, while at the same time providing a* ***23% wider*** *operating temperature range.*

Greater Reliability. *By using innovative design techniques, the M25 achieves a* ***4-fold increase*** *in MTBF.*

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The M25 is encapsulated and hermetically sealed, and meets the stringent environmental requirements of MIL-STD-810C and MIL-S-901C.

Abbott's new M25: higher performance in a proven design.

Call or send for specs and our full line catalog.

Abbott Transistor Laboratories, Inc. Power Supply Division, 2727 La Cienega Blvd., Los Angeles, CA 90034 (213) 936-8185. Eastern Office: (201) 461-4411, Southwest Office: (214) 437-0697, London Office: 0737-82-3273.

MODEL M25 SPECIFICATIONS

DIMENSIONS	**6.25"x 2.75"x 1.5"**
Input frequency	*47-440 Hz*
Input voltage	*103.5 to 126.5 V rms*
Outputs	*5, 12, 15, 24, 28 V*
Efficiency	*70% minimum*
Ripple/noise	*20 mV rms/100 mV p-p*
Line regulation	*10 mV*
Load regulation	*25 mV*
EMI	*MIL-STD-461B*
Environment	*MIL-STD-810C*
	MIL-S-901C
Input protection	*MIL-STD-1399 sec 103*
Operating temperature range	*−20°C to 71°C*
Storage temperature range	*−55°C to 85°C*
MTBF (ground benign)*	
Standard	*176,000 hours*
ER Option	*759,000 hours*
MTBF (naval sheltered)*	
Standard	*33,000 hours*
ER Option	*125,000 hours*

**MIL-STD-217D (50°C baseplate)*

abbott

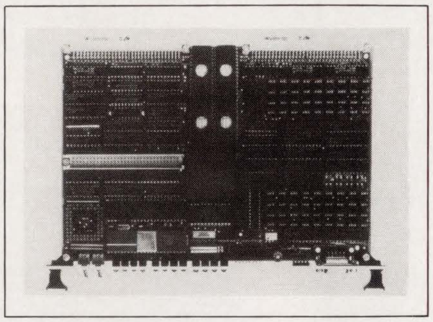
MILITARY POWER SUPPLIES

CIRCLE NO 179

PC/XTs, PC/ATs, and compatible computers provides an onboard 8-MHz 80186 μP and an RMX-nucleus OS. Onboard memory facilities include four 28-pin sockets for EPROM, EEPROM, or battery-backed CMOS RAM, and two 28-pin sockets for as much as 64k words of RAM dual ported to the 80186 and to the PC bus (the PC bus interface includes an MMU). The board can operate as a bus master on the IBM PC/AT bus, giving it direct 8- or 16-bit access to the upper address ranges of the IBM PC/AT. It includes interrupt controllers for both onboard and PC bus interrupt sources. Additional onboard facilities include two independent, full-duplex interfaces that support asynchronous and bit- and byte-oriented synchronous protocols, and a real-time clock/calender. Belgian fr 74,970.

Dolmen Engineering nv, Vaucampslaan 28, B-1511 Huizingen, Belgium. Phone (02) 3600025. TLX 61225.

Circle No 381



CPU CARD

- *Runs an 80386 μP in VME Bus systems*
- *2M bytes of local memory on board*

By employing the CPU-386 CPU card, you can use Intel operating systems and software in VME Bus systems. The double-Eurocard board runs a 16-MHz 80386 processor, and it can operate in a virtual 8086 mode, which allows you to run software written for 8086-family μPs. It has 2M bytes of zero-wait-state local RAM and a local bus-expansion interface for additional local memory, and it includes sockets for an 80387 math coprocessor and as much as 512k bytes of EPROM. The board incorporates two synchronous/asynchronous serial I/O channels that are routed to its P2 connector, plus a front-panel serial I/O port, for console/debugging operations. It also has three programmable 8-bit timers and a battery-backed real-time clock/calendar on board. The CPU card's VME Bus interface, which supports unaligned data-bus transfers and dynamic-bus sizing, also has slot-1 functions. With debugging firmware and an in-line assembler/disassembler, the card costs DM 14,950.

Force Computers GmbH, Daim-

FAST COMPANY

FAST In its "B" configuration, the UDS 208A/B moves data at 4800 bps, half-duplex, over dial-up telephone lines. Its auto-answer feature permits unattended operation, and auto-dialing capability can be added. Three simple strap changes convert the device to the "A" configuration, permitting full-duplex operation over four-wire circuits.

FASTER The 9600A/B is UDS' answer to the demand for 9.6 kbps communication. Like its 2400 bps counterpart, it can be changed from dial-up to dedicated line configuration (or vice versa) in the field. Complete self-test and remote loop-back capabilities simplify system diagnostics; the modem is available as a free-standing unit or as a rack-mountable card.

FASTEST Now you can push your dial-up data communications system all the way to 14.4 kbps! The UDS 14.4A/B is trellis coded, giving you top performance, even under undesirable line conditions. Fall-back data rates of 12 and 9.6 kbps are provided. Contact Universal Data Systems, 5000 Bradford Drive, Huntsville, AL 35805. Phone 205/721-8000; Telex 752602 UDS HTV.

UDS for fast dial-up modems.

Universal Data Systems

MOTOROLA INC.
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UDS modems are offered nationally by leading distributors. Call the nearest UDS office for distributor listings in your area.

DISTRICT OFFICES: **Apple Valley,** MN, 612/432-2344 • **Atlanta,** GA, 404/998-2715 • **Aurora,** CO, 303/368-9000 • **Blue Bell,** PA, 215/643-2336 • **Boston,** MA, 617/875-8868 • **Columbus,** OH, 614/895-3025 • **East Brunswick,** NJ, 201/238-1515 • **Glenview,** IL, 312/998-8180 • **Houston,** TX, 713/988-5506 • **Huntsville,** AL, 205/721-8000 • **Issaquah,** WA, 206/392-9600 • **Livonia,** MI, 313/522-4750 • **Mesa,** AZ, 602/820-6611 • **Milwaukee,** WI, 414/273-8743 • **Mission Viejo,** CA, 714/770-4555 • **Mountain View,** CA, 415/969-3323 • **Richardson,** TX, 214/680-0002 • **St. Louis,** MO, 314/434-4919 • **Silver Spring,** MD, 301/942-8558 • **Tampa,** FL, 813/684-0615 • **Uniondale,** NY, 516/222-0918 • **Van Nuys,** CA, 818/891-3282 • **Willowdale,** Ont, Can, 416/495-0008

Created by Dayner/Hall, Inc., Winter Park, Florida

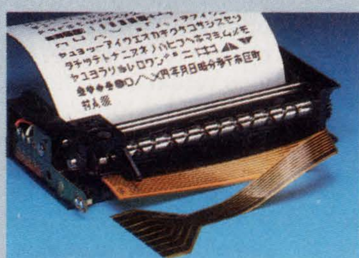
CIRCLE NO 178

Seiko's High Resolution Thermal Printers.

Not only are Seiko's family of thermal printers compact and inexpensive, they're so reliable and maintenance-free, you won't have to give them a second thought. But you can't overlook the excellent printing quality or ease of control and interfacing that make them ideal for a wide variety of applications.

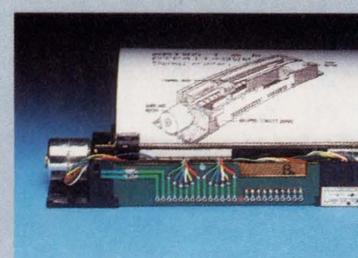
Whether you need an inexpensive printer for graphics and characters, or a high-speed printer with extremely low noise characteristics, there's a Seiko thermal printer to suit your applications.

Seiko's Family of Compact Printers Meet Your Low-Cost, High-Quality Printing Requirements.



The MTP Series character and graphics printers are compact, thermal printers designed to meet the demand for inexpensive, high-quality printing.

The high reliability and excellent quality provided by the MTP series of character and graphics printers make them ideal for a variety of applications, such as medical and measuring instruments, calculators, office machines and small computer terminals.



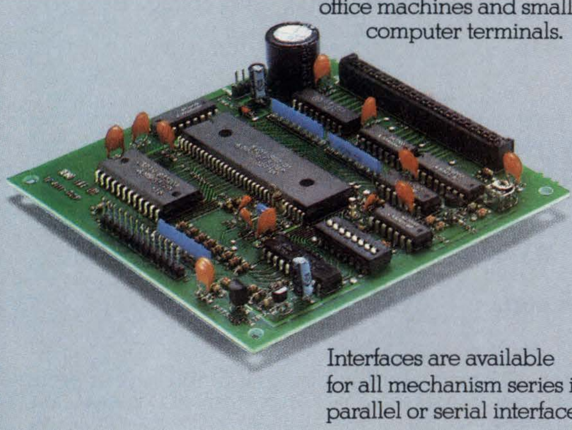
The STP Series was developed as an advanced version of the MTP series and incorporates stepper motor drive for improved print quality and reduced noise levels.

Two independent stepper motors, one for head movement and one for paper feed, reduce noise and improve print quality in the STP series. And since the stepper motors are used independently, bidirectional character printing and logic seeking printing are possible. These compact units are ideal for measuring and analysis, instrumentation, communication and medical equipment, small computers and data terminals.

The LTP series are stepper-motor driven, high-speed, high-quality line thermal printers.

The stepper-motor drive allows the LTP line printer to print both characters and graphics with very little noise. Paper out detection is also provided for the LTP series. A mechanical stop signal occurs, when paper out or head opens.

The most advanced, compact thermal printer from Seiko, the LTP series is ideal for any application where printing speed, quiet operation and excellent print quality are required.



Interfaces are available for all mechanism series in parallel or serial interface.

If you're interested in thermal printing you should be talking to Seiko Instruments. Call today!

SEIKO INSTRUMENTS U.S.A., INC. 2990 W. Lomita Blvd., Torrance, CA 90505, PHONE (213) 530-8777, TWX: 910-347-7307, FAX: (213) 539-8621.

SEIKO INSTRUMENTS

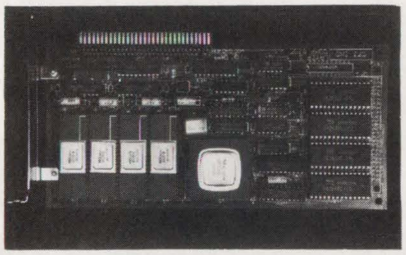
CIRCLE NO 177

lerstrasse 9, 8012 Ottobrunn/Munich, West Germany. Phone (089) 600910. TLX 524190.

Circle No 382

Force Computers Inc, 727 University Ave, Los Gatos, CA 95030. Phone (408) 354-3410.

Circle No 383



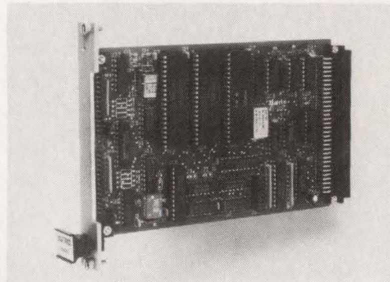
COPROCESSOR

- *Provides 20-MIPS processing for the IBM PC bus*
- *Data-flow architecture and hardware multiplier*

The DF-1 coprocessor board contains four NEC μPD7281 data-flow processors, 128k bytes of local-image memory, and a 9305 memory-access chip. The data-flow architecture and on-chip hardware multiplier combine to provide 20-MIPS performance. A single 7281 image-pipeline processor (the ImPP) can compute a 3×3 convolution of a 512×512-pixel (8 bits/pixel) image in 2.98 sec. According to the manufacturer, two ImPPs can do the same convolution in 1.5 sec, and four ImPPs can do the convolution in little more than a quarter of the time that a single ImPP would require. You can use the board for applications that require repetitive processing on large streams of data. It supports DMA transfer between its image memory and the IBM PC's memory. The DF-1 package includes a user's manual, demonstration software, sample ImPP code, a monitor program, and C interface software. $995.

Data Flow Imaging Inc, Box 116, Westwood, NJ 07675. Phone (201) 666-7970.

Circle No 384



STEPPER CONTROL

- *Dual-axis stepper-motor controller for the VME Bus*
- *Single-channel version is also available*

The MS-DSC dual-axis stepper-motor controller is an intelligent VME Bus board that simplifies the required programming and overhead

Dialight Components. For a complete selection that builds on quality.

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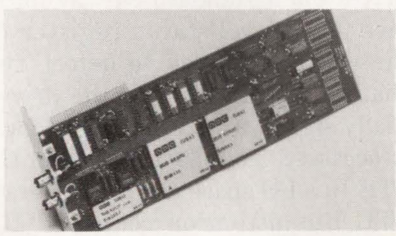
For indicator lights circle 97 | For switches circle 136 | For optoelectronics circle 175 time of the host CPU. A single-channel version, the MS-SSC, is also available. The MS-DSC features independent X- and Y-axis control, step rates from 13 to 10,000 steps/sec and full- or half-step operation. The board also provides complete software control of all motor characteristics, including travel distance, ramp-up, and ramp-down. The board automatically senses as many as five limit switches per motor. To reduce heating, you can switch the phase outputs to the motors during motor standstill. The boards are compatible with 3-, 4-, and 5-phase stepper motors. The software can control as many as four auxiliary outputs per motor. $695.

Matrix Corp, 1203 New Hope Rd, Raleigh, NC 27610. Phone (919) 833-2000.

Circle No 385



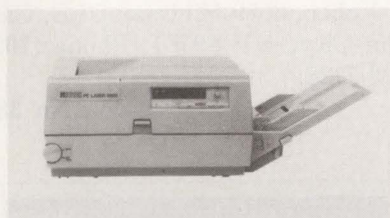
PC-MIL INTERFACE

- *Connects MIL-STD-1553 and IBM PC buses*
- *Can be a 1553 bus controller or remote terminal unit*

The BUS-65515 card provides an intelligent interface between the serial, dual-redundant MIL-STD-1553 data bus and the IBM PC bus. The card takes up a full slot in an IBM PC. You can configure it via software control for use as a 1553 bus controller or remote terminal unit. The board supports 12 mode codes, all 1553 message formats, and wraparound built-in test procedures. Using onboard jumpers, you can select both the memory mapping of the shared 4k×16-bit RAM and the interrupt priority levels. When the card is operating as a bus controller, you can program it to store and process as many as 59 messages without subsystem intervention. When you operate the device as a remote terminal, the board can process and store as many as 107 messages without external intervention. $4995.

ILC Data Device Corp, 105 Wilbur Pl, Bohemia, NY 11716. Phone (516) 567-5600. TWX 510-228-7324.

Circle No 386



LASER PRINTER

- *Produces 6 pages per minute*
- *Designed for desktop publishing*

The PC Laser 6000 is a 6-pg/minute laser printer. Its controller comes with 1M byte of RAM that's expandable to 2M bytes, so it lets you download a fully bit-mapped legal-size page. The printer features a graphics command set that includes Diablo 630 emulation. Optional emulation cards are available for the HP Laserjet Plus, the IBM Proprinter, and the Epson FX-80 printer. The 300-dot/in. printer comes with both Centronics (parallel) and RS-232C (serial) interfaces. It contains eight resident fonts; a library of font cartridges is also available. $2395.

Ricoh Corp, 5 Dedrick Pl, West Caldwell, New Jersey 07006. Phone (201) 882-2000.

Circle No 387

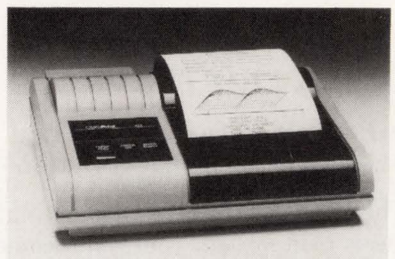
DISK DRIVES

- *Offer 40M and 80M bytes of storage*
- *Have SCSI interface*

The Owl III Models 40 and 80D provide 40M and 80M bytes of disk storage, respectively. Model 40 is a half-height 5¼-in. unit; Model 80D comes in a full-height package. Each drive provides a SCSI interface that complies with the current SCSI Rev 17B, CCS Rev 4 ANSI standard. The drives feature a 40-msec access time. The data path uses a dual-port data buffer and 1:1 sector interleaving. The 80D unit uses dual actuators, dual data paths, and multiplexing features of the SCSI bus to overlap disk I/O operations, thereby eliminating access, latency, and command-execution delays. Model 40, $750; Model 80D, $1295.

Xebec, 3579 Highway 50 E, Carson City, NV 89701. Phone (702) 883-7128.

Circle No 388



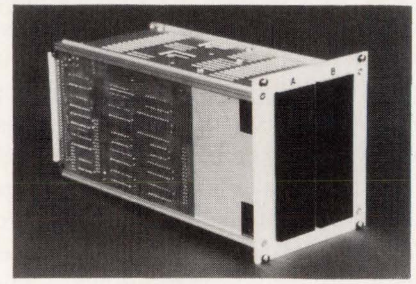
PRINTER

- *Thermal printer operates quietly at 6 lps*
- *Features only three moving parts*

The Omniprint 426 thermal printer prints at the rate of 6 lps. The device has only three moving parts. A 2k-byte buffer is standard, and an 8k-byte buffer is available. The printer features full bit-mapped graphics at 256 dots per 42-column line. Other standard features include normal and upside-down printing, as well as RS-232C- or Centronics-compatible interfaces. A watchdog circuit is provided in case of processor failure. Brownout protection is included, and you can use a self-test mode for field testing. Power is switch selectable; the standard requirements are 110/220V ac, 50 to 60 Hz. $240 (1000).

OmniPrint Inc, 1188 Elko Dr, Sunnyvale, CA 94089. Phone (408) 745-6400. TLX 350165.

Circle No 389



DISK MODULE

- *Houses two 3½-in. disk drives*
- *Plugs into an STE Bus backplane*

Residing in a 3U×21-HP Eurocard cassette, this STE Bus-compatible disk module houses two 3½-in., 1M-byte floppy-disk drives and a disk-drive controller card. Based on the WD1772 disk controller, the controller card supports as many as four 3½- or 5¼-in. single- or double-sided, single- or double-density disk drives via a standard 34-way interface. A control/status register on the card allows you to detect disk changes and to monitor the drive's ready signal. The disk-drive module is accessed as a slave device in the STE Bus I/O space and can generate STE Bus attention requests. It's available in either a 160- or a 220-mm-deep Eurocard cassette and costs approximately £495.

British Telecom Research Laboratories, Martlesham Heath, Ipswich, Suffolk IP5 7RE, UK. Phone (0473) 642933. TLX 98376.

Circle No 390

TRANSLATORS

- *Translate data between VME Bus and Multibus systems*
- *Allow real-time cooperation of alien boards*

The Syner-System line of board-level translators provides interfaces between VME Bus and Multibus systems and supplies repeaters for operations between Multibus machines or VME Bus machines. The Multibus/VME Bus unit permits data sharing (at bus-level speed) be-

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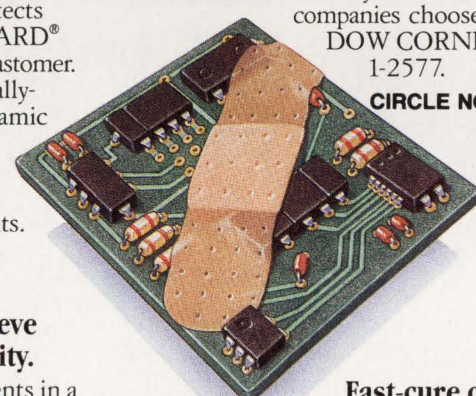
CIRCLE NO 133



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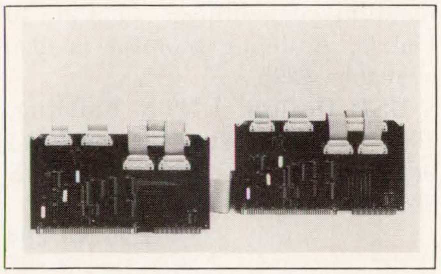
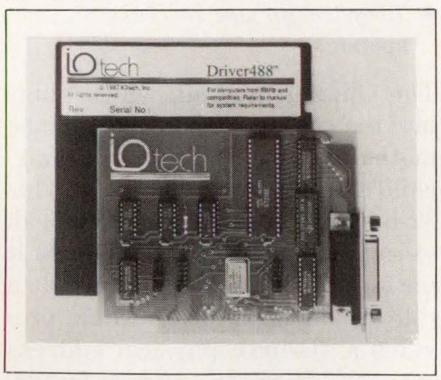


tween a Multibus computer system and a VME Bus computer system. The translator disguises the Multibus system as a typical VME Bus board by performing all the necessary VME Bus-to-Multibus signal and timing conversions. The Multibus repeater 2000 allows you to expand a Multibus system along the bus. The VME/VME system provides the same expansion capability for VME Bus systems. $1495 each.

HVE Engineering Inc, 1684 Dell Ave, Campbell, CA 95008. Phone (408) 370-4666. TLX 467956.

Circle No 391



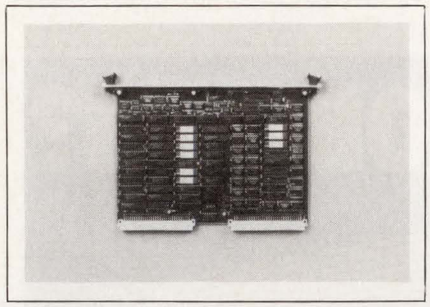
IEEE-488 CONTROLLER

- *Runs on the IBM PC*
- *Simplifies interface of PC and IEEE-488 bus*

The Personal488 consists of the GP488A board and Driver488 software. The Personal488 provides high-level programming methods that resemble those of Hewlett-Packard's dedicated bus controllers. The package requires no language-specific drivers or routines. Once installed in DOS, the software is available to the PC without reloading. The controller automatically informs the PC operator when errors such as invalid commands or bus time-outs occur. The package offers the same commands as HP's Series 80 controllers and employs the bus using the same protocol. $395.

IOtech Inc, 23400 Aurora Road, Cleveland, OH 44146. Phone (216) 439-4091.

Circle No 392



IMAGING CARD

- *Extracts histograms and features*
- *Operates at real-time video rates*

The HF-150 VME Bus, dual-function board extracts histograms and features. The board incorporates a streak feature-extraction mode that accelerates the execution of high-level image-processing functions, such as centroid location and dimensional measurement (the extraction mode accelerates the process by encoding by run length). In its detailing mode, the board processes subregions of an image in less than one-thirtieth of a second, according to the manufacturer. $2895.

Imaging Technology Corp, 600 West Cummings Park, Woburn, MA 01801. Phone (617) 938-8444. TLX 948263.

Circle No 393

CPU CARD

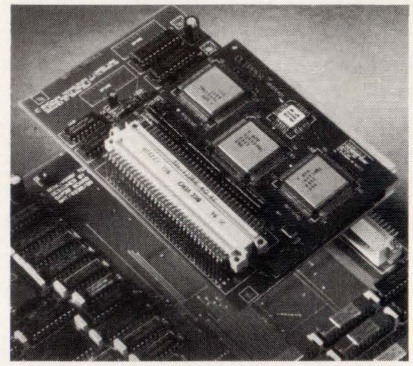
- *Runs a 6-MHz 64180 μP for use in STE Bus systems*
- *Configurable as a default bus master or slave*

The SX180 single-Eurocard CPU board for STE Bus systems incorporates a 6-MHz 64180 μP, one memory socket for as much as 32k bytes of

EPROM firmware, and a second memory socket for EPROM or battery-backed RAM. The board also includes two DMA channels, two RS-232C serial ports, and two timers. The CPU supports the STE Bus attention-request (ATNRQ) lines used as both interrupt and DMA requests, and it supports the STE Bus vector-fetch cycle. You can configure the SX180 as a default bus master that provides all the bus functions required by the STE Bus specification. Alternatively, you can operate the board as a temporary bus master or as a bus slave. Available software for the SX180 includes a version of CP/M+, and Z-system, a CP/M-compatible operating system that provides file-handling capabilities similar to Unix's. A debug monitor is also available. £295.

DSP Design, LNTN Building, 100 St Pancras Way, London NW1 9ES, UK. Phone 01-482 1773. TLX 8950511 (attn ref: 18069001).

Circle No 394



CPU MODULE

- *Incorporates Fairchild Clipper μP*
- *Targeted for use in Unix systems*

The Clipper module, which plugs into the company's b32 Unix-engine mother board, incorporates Fairchild's Clipper μP chip set. This 32-bit CPU module provides peak execution rates of 33 MIPS, and it performs floating-point math at a rate of 2M flops. The module provides a 4G-byte physical address space and hardware support for virtual memory. The Clipper module joins a range of CPU modules for the b32 mother board, including the iAPX-86, MC68000, and NS32000 processors. Clipper module, £3200 (25); b32 mother board, £2000 to £4000, depending on memory capacity and functionality.

Benchmark Technologies Ltd, Benchmark House, 2 Lower Teddington Rd, Hampton Wick, Kingston-upon-Thames, Surrey KT1 4ER, UK. Phone 01-943-4393. TLX 8952387 (attn ref: BTL/1417).

Circle No 395

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Variable Data Block Size	√	√	√	
Flexible Triggering	√	√	√	
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CIRCLE NO 185

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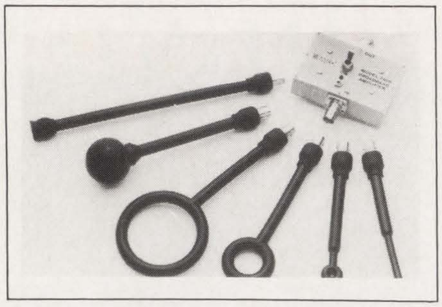


EMI PROBES

- *Probes test to FCC, VDE, Tempest, and MIL-STD EMI*
- *Frequency range spans 100 kHz to 2.3 GHz*

The 7405 probe set, comprising three loop probes, a ball probe, and a stub probe, detects E and H fields separately. The units test to FCC, VDE, Tempest, and MIL-STD EMI standards and cover the frequency range from 100 kHz to 2.3 GHz. All the probes are impedance matched. The vendor also offers an optional preamplifier having a 600-MHz bandwidth. The 7405's standard accessories include an extension handle and a carrying case. Model 7405, \$495; preamp, \$255.

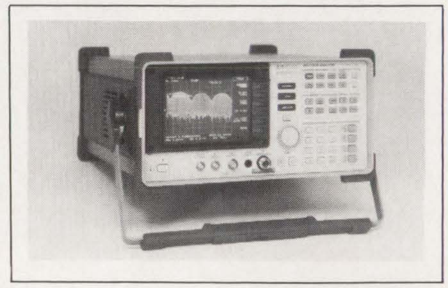
EMCO, Box 1546, Austin, TX 78767. Phone (512) 835-4684. TLX 797627.

Circle No 399

ANALYZERS

- *Spectrum analyzers cover 1 kHz to 22 GHz*
- *Instruments meet military ruggedness specs*

The HP 8562A and HP 8562B, a pair of portable, microwave spectrum



analyzers, cover a 1-kHz to 22-GHz frequency range. The HP 8562A provides tracking preselection from 2.75 to 22 GHz; the HP 8562B provides no preselection. The instruments have a 1-dB/division scale factor, and their synthesized tuners sport 100-Hz tuning steps. The analyzers' frequency response is ±1.2 dB at 2 GHz and ±4.3 dB at 22 GHz. The ratio of signal to harmonic distortion is 100 dB max; the ratio of signal to intermodulation distortion

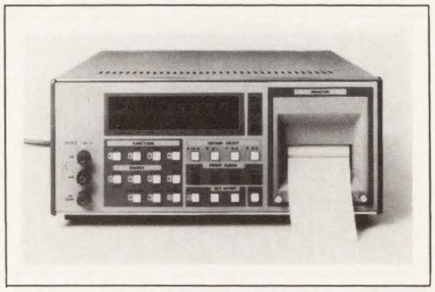
is 75 dB max. The units have over 100 built-in measurement and data-processing functions. They also have a speaker with which you can listen to demodulated AM and FM signals. The units meet MIL-T-28800C specs. Each analyzer incorporates a standard frequency counter that has 10-Hz resolution. HP 8562A, $35,000; HP 8562B, $31,000. Delivery, eight weeks ARO.

Hewlett-Packard Co, 1820 Embarcadero Rd, Palo Alto, CA 94303. Phone local office.

Circle No 400

LOGGING METER

- *Multimeter accepts scanner plug-ins*
- *Plug-ins feature cold-junction compensation*



The Model AD-5312 logging multimeter has a built-in thermal printer. You can expand the basic single-channel unit to include four, 13, or 25 channels via optional plug-in scanners. The meter measures dc and ac volts and resistance. Furthermore, the optional scanners have cold-junction compensation for common thermocouples and provide 0.1°C resolution for linearized temperature measurements. The meter has built-in math functions. Factory-installed options include IEEE-488, RS-232C, and BCD interfaces. $2120.

PrimeLine, Box 670, San Fernando, CA 91341. Phone (800) 525-5554; in CA, (818) 764-5400. TLX 4943094.

Circle No 401

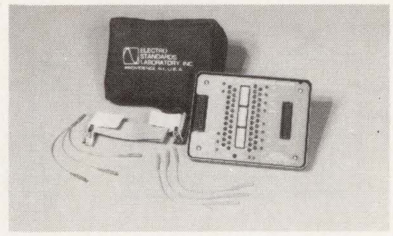
AMPLIFIER

- *Features 20-dB gain from 10 kHz to 2.5 GHz*
- *Reverse isolation specs 45 dB*

The Model 330 amplifier has a 3-dB bandwidth of 10 kHz to 2.5 GHz. Its gain flatness is ±0.5 dB typ from 20 kHz to 2 GHz (with 20-dB gain). The amplifier's typical noise figure is <7 dB, and it specs reverse isolation of 50 dB to 1.3 GHz (45 dB to 2.5 GHz). The unit measures 3.6×4.3×6.9 in. $465.

Sonoma Instrument Co, Box 9011, Santa Rosa, CA 95405. Phone (707) 542-8569.

Circle No 402



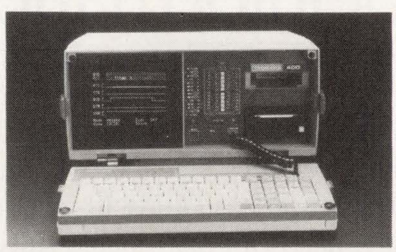
BREAKOUT BOX

- *Box has switches for each line*
- *LEDs show the status of interface lines*

The Model 500 breakout box works with RS-232C and CCITT V.24 interfaces. The unit has LEDs that display the state of all interface lines. Miniature rocker switches allow you to connect or disconnect each interface line. Small patch cords enable cross-wiring or loopback configurations. The unit comes with a carrying case and a reference chart of RS-232C signals. $98.

Electro Standards Laboratory Inc, Box 9144, Providence, RI 02940. Phone (401) 943-1164. TLX 6972057.

Circle No 403



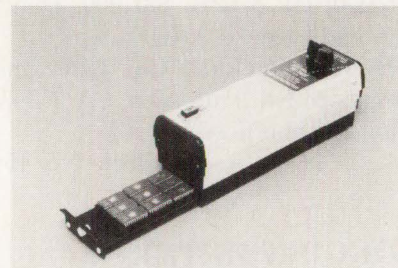
PROTOCOL ANALYZER

- *Captures serial bit streams at 72k bps*
- *Stores captured data on built-in floppy disk*

This protocol analyzer, Model 400, monitors data streams and emulates serial-communications devices at rates as high as 72k bps. It handles most common serial protocols. The unit comes with six standard bit-error-rate tests, and you can also program custom tests in the company's proprietary language. The unit has a built-in floppy disk for storing captured data and instrument setups. The analyzer has a 7-in. CRT. $7495.

Digilog Inc, 1370 Welsh Rd, Montgomeryville, PA 18936. Phone (215) 628-4530. TLX 6851019.

Circle No 404



UV EPROM ERASER

- *Holds nine to 12 EPROMS*
- *60-minute timer shuts off UV lamp*

The Model PE-140T UV EPROM eraser provides a 254-nm lamp having an intensity of 8 mW/cm^2. The unit erases nine to 12 EPROMs at a time in 11 to 15 minutes. Its conductive foam pad protects the EPROM chips from ESD. A 60-minute timer automatically shuts the unit off. The unit's case is aluminum and has a safety interlock that shuts off the lamp when opened. $139.

Spectronics Corp, Box 483, Westbury, NY 11590. Phone (516) 333-4840. TWX 510-222-5877.

Circle No 405

64180 EMULATOR

- *Provides 64k bytes of emulation memory*
- *Continuously strobes buses for low-level testing*

The m-64180 emulates the 64180 μP (an enhanced Z80) at clock speeds as high as 8 MHz. The emulator contains 64k bytes of emulation memory that's mappable over the μP's address space, beginning at each 32k-byte boundary. The unit has a 4k-event trace buffer and can stop on 99 breakpoints and a single range breakpoint. The unit has a strobe

test that continuously strobes a selected address, control, or data bus to enable low-level debugging of peripheral devices. $3495.

Ziltek Corp, 1651 E Edinger Ave, Santa Ana, CA 92705. Phone (714) 541-2931.

Circle No 406

THERMOMETER

- *Measures temperature of both probe and environment*
- *Displays temperatures from −55 to +199°F*

The Model ER108LAB digital thermometer measures both the ambient and the probe temperature. The unit displays readings from −55 to +199°F. You can use its probe for air, liquid, soft-state materials, and solid-state surfaces. The battery-powered unit has a ½-in. LCD and a 5½-in. metal probe with a 28-in. lead. $39.95.

Edmund Scientific Co, Dept 5554, 101 E Gloucester Pike, Barrington, NJ 08007. Phone (609) 547-3488.

Circle No 407

FFT SOFTWARE

- *Runs on HP 200 and 300 Series computers*
- *Converts and displays a 1024-point spectrum in 1 sec*

The Signalprobe software package runs on Hewlett-Packard 200 and 300 Series desktop computers. The software requires an Infotek (Anaheim, CA) AD200 plug-in A/D card. The software can display averaged voltage levels, time-domain waveforms, and FFT spectrums. It can

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241	541	620	862	534	824	533	844
244	827	623	863	564	825	563	845
465	828	640	864	574	826	573	846
466		643		575	874	580	880
467		645		576	876	841	
468				577	878	842	
				821	879		
				822			

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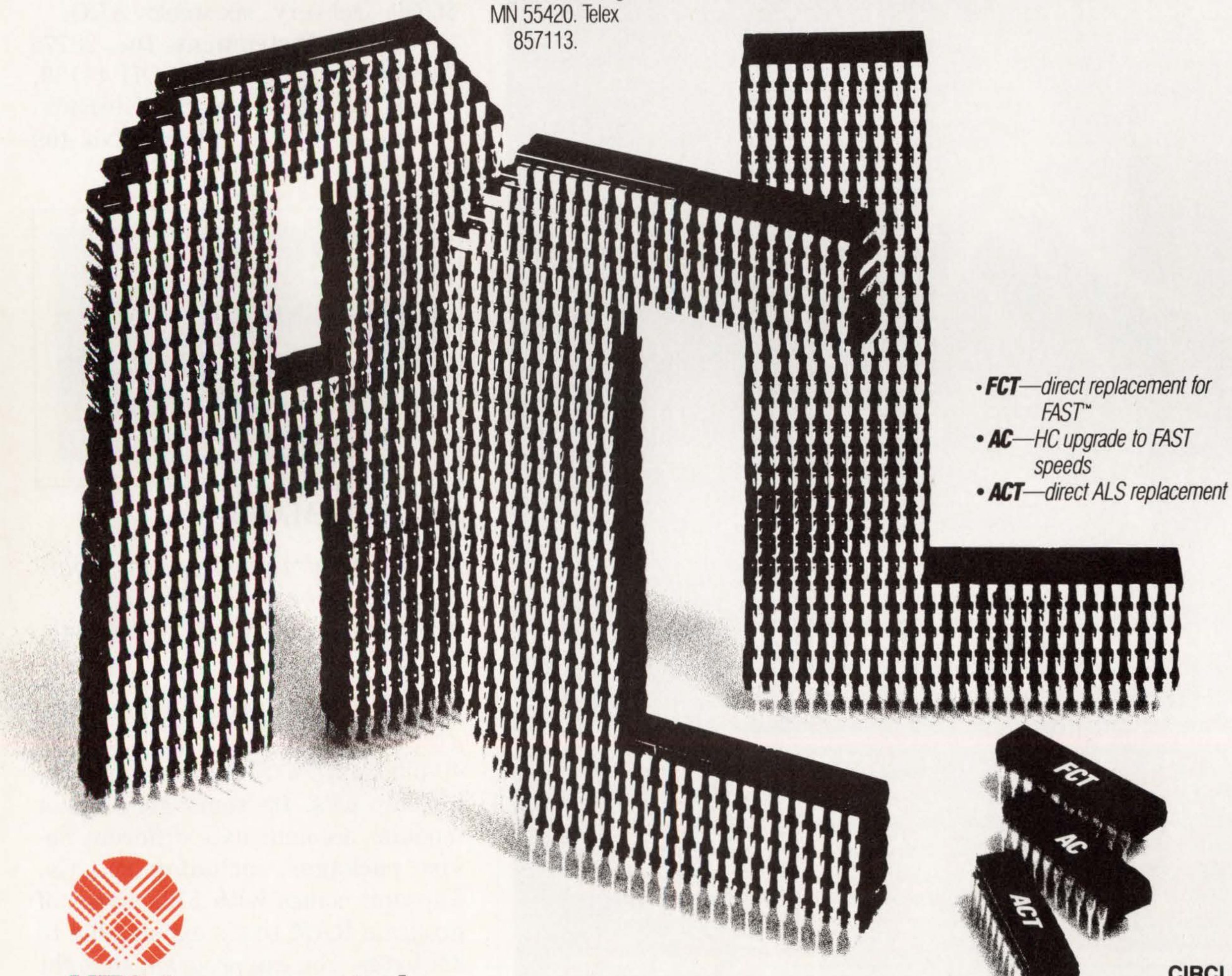

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- ***ACT***—*direct ALS replacement*

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convert a 1024-point FFT in 1 sec, yielding a real-time conversion rate of 1 kHz. A data-acquisition library is optional. $540; optional library, $390.

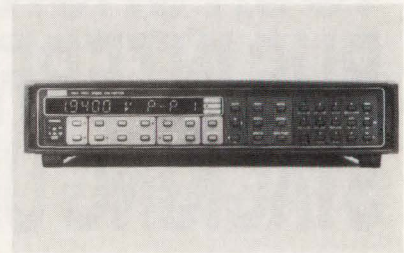
Data Physics Corp, 1210 S Bascom Ave, Suite 224, San Jose, CA 95128. Phone (408) 977-0800. TLX 4998389.

Circle No 408

DIGITIZER

- *Waveform digitizer captures 1M samples/sec*
- *Offers 16-bit resolution at lower digitizing rates*

The Model 194A waveform digitizer simultaneously samples two channels at rates as high as 1M samples/sec. The instrument's input range is



10 μV to 200V. Its resolution is 16 bits at 100k samples/sec and 8 bits at 1M samples/sec. The capture memory is 64k samples/channel max, and the sample intervals range from 1 μsec to 1.0 sec. The unit has nine built-in math functions and comes with an IEEE-488 interface. The instrument can expand short command strings to complex ones and can interpret command strings originally written for other instruments. Model 194A with one channel, $4095; with two channels, $6030. Delivery, six weeks ARO.

Keithley Instruments Inc, 28775 Aurora Rd, Cleveland, OH 44139. Phone (216) 248-0400. TLX 985469.

Circle No 409

PROGRAMMER

- *Gang programmer accepts eight EPROMs or single-chip μPs*
- *Socket assemblies accommodate PLCCs*

The 288 multiprogrammer programs as many as eight 24-, 32-, or 40-pin EPROMs. It also accepts single-chip μPs. Its removable socket modules accommodate different device packages, including PLCCs. The unit comes with 512k bytes of program RAM that's expandable to 2M bytes. You can program all eight devices with the same data or program them in word-wide groups

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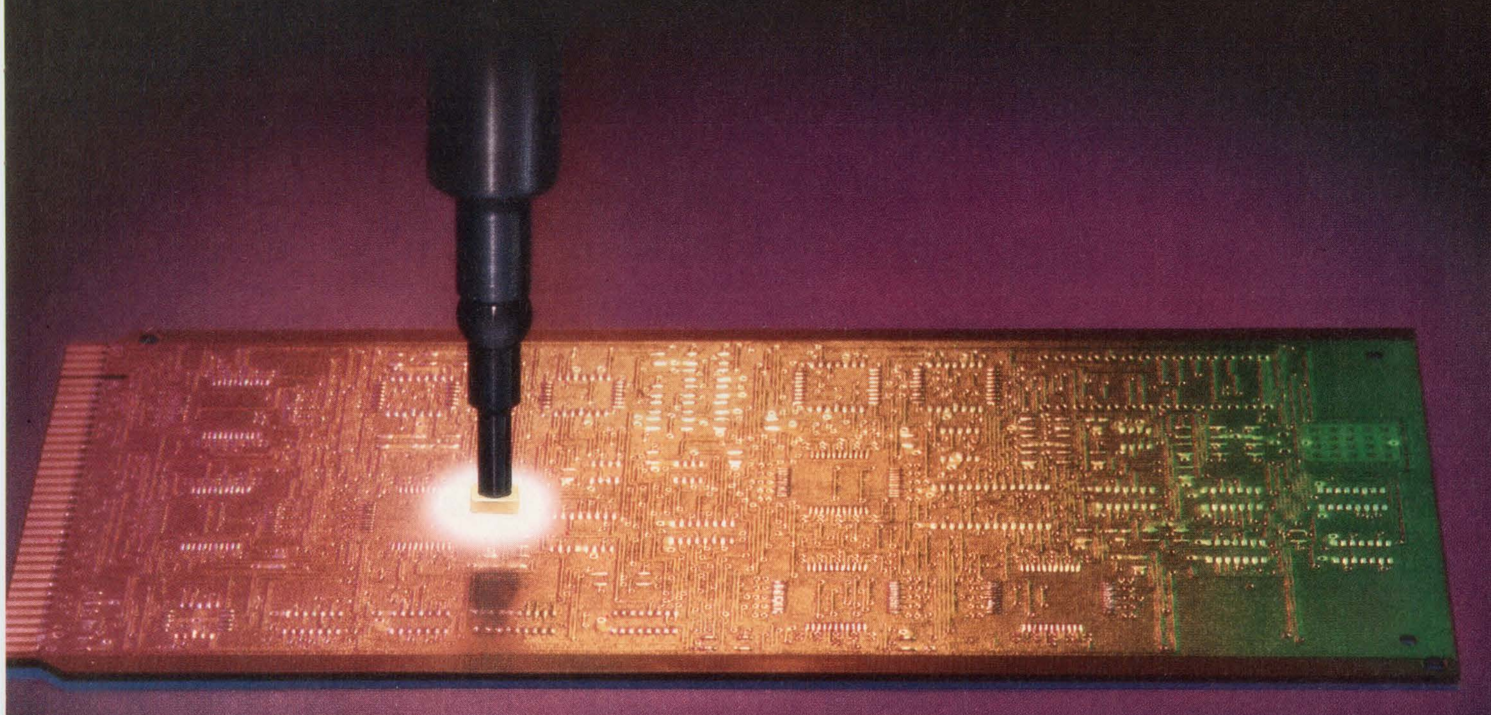

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Circle No. 1 for advance information

with sets of data. You can operate the programmer as a stand-alone unit or connect it to a host. Base unit with 512k bytes of RAM and 32- or 40-pin module, $3195; additional modules, from $1395.

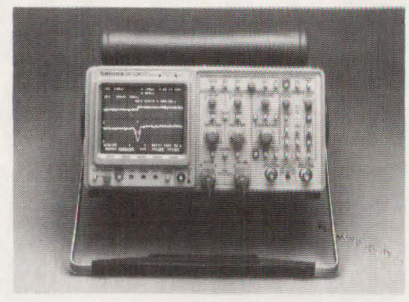
Data I/O Corp, Box 97046, Redmond, WA 98073. Phone (206) 881-6444. TLX 152167.

Circle No 410

DIGITAL SCOPE

- *Digital scope has automatic-set-up button*
- *Unit can save anomalous waveforms*

The 2430A digital oscilloscope includes two 100M-sample/sec digitizers having 8-bit resolution. The unit has a 2-nsec glitch-capture feature as well as 1k samples/channel of capture memory. The scope has an automatic-setup feature and can extract 21 waveform parameters from a captured signal. You can program the scope to go through a series of setups. The unit can babysit a circuit under test and record events that fall outside specified limits. $8900.



Tektronix, Box 1700, Beaverton, OR 97075. Phone (800) 426-2200; in OR, (503) 627-9000.

Circle No 411

COUNTER

- *Commercial universal counter with rubidium timebase*
- *Covers the frequency range from dc to 200 MHz*

The Model 1995 universal counter/timer is the first commercially available instrument having an optional rubidium timebase oscillator. The oscillator offers an aging rate of $<5\times10^{-11}$ parts per month or $<2\times10^{-7}$ parts per year. The unit measures to nine digits in one second and covers the frequency range from dc to 200 MHz. Its input sensitivity is 50 mV. Its frequency accuracy is 400 times better than that of crystal timebases, the vendor claims. The unit can make as many as 150 readings/sec when it's on the IEEE-488 bus. A MATE interface is optional. Model 1995 with optional rubidium timebase, $11,250. Delivery, 12 weeks ARO.

Racal-Dana Instruments Inc, Box C-19541, Irvine, CA 92713. Phone (714) 859-8999. TWX 910-595-1136.

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CIRCLE NO 47

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FEEDBACK ANALYZER

- *Analyzes frequency responses of control loops*
- *Runs on IBM PC family*

The Classical Controls Analysis Program (CCAP) is an interactive, menu-driven program that helps you analyze and design feedback-control systems. Using it, you can enter and modify transfer functions that contain as many as 20 real numbers and 20 quadratics in both the numerator and the denominator. The program performs all its calculations in double precision and uses techniques to minimize round-off errors. You can use it to analyze both analog and digital control loops with either root-locus or frequency-response methods. The program draws the root locus or prints the roots at each gain value as you vary the gain; you can store frequency-response information (frequency, gain, and phase) in a disk file or plot it by using a number of formats. The program includes a database library that can store as many as 80 transfer functions. The program uses Multi-Halo Graphics (from Media Cybernetics Inc, Silver Springs, MO) to ensure portability and is compatible with a wide variety of graphics interface boards and graphics printers. Version 2 includes features for solving block diagrams. It requires a PC/XT or PC/AT with at least 512k bytes of memory, a hard-disk drive, an 8087 or 80287 numerical coprocessor, and PC-DOS 2.1 or a later version. The program is not copy-protected. The Multi-Halo graphics library is also available. Version 1, $395. Version 2, $595.

Lewis Engineering Software, 4911 Hampton Rd, La Canada, CA 91011. Phone (818) 790-4801.

Circle No 413

PHOTOPLOT EDITOR

- *Lets you edit photoplots in Gerber format*
- *Runs on the IBM PC family*

The View program lets you load and display a CAD-generated image file in Gerber format; it also lets you detect any errors in the plotting data and use the CAD program to correct them before sending the file to a photoplotting center for the production of masks or prototype boards. View+ adds a graphics editor that lets you correct the errors you find without having to return to the CAD program that created the file. The editing functions of both

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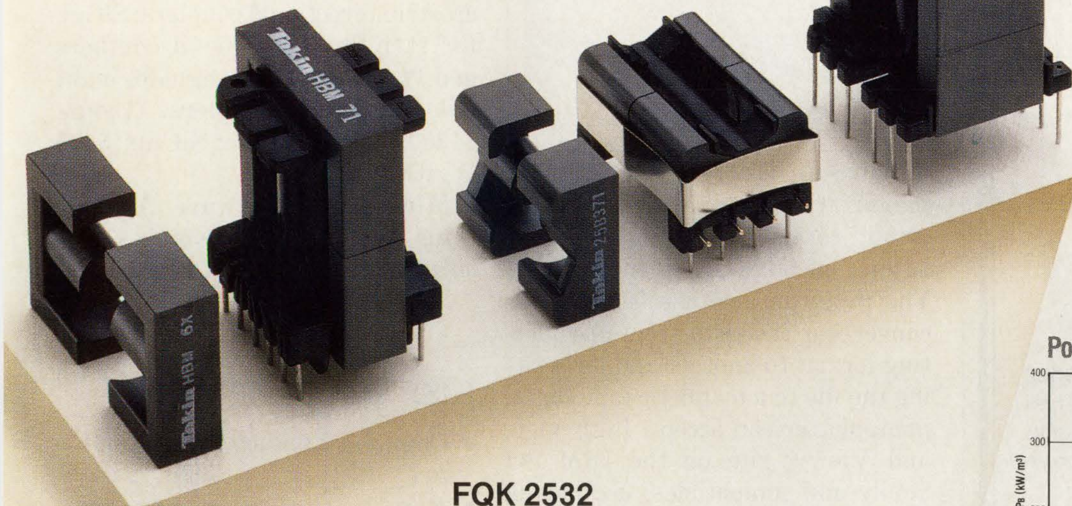
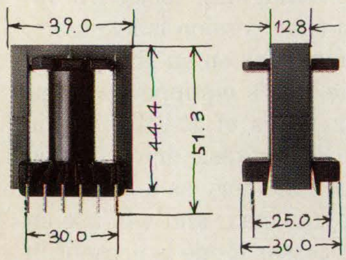
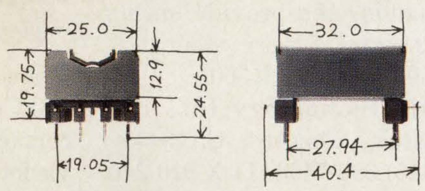


Shapes and Dimensions

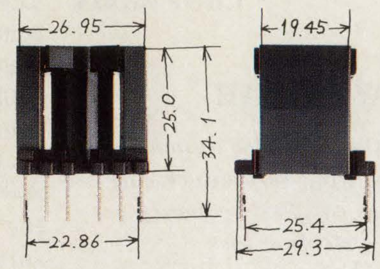
ETD 39L



FQK 2532

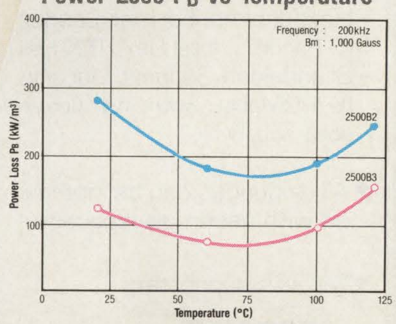


FPQ 2625

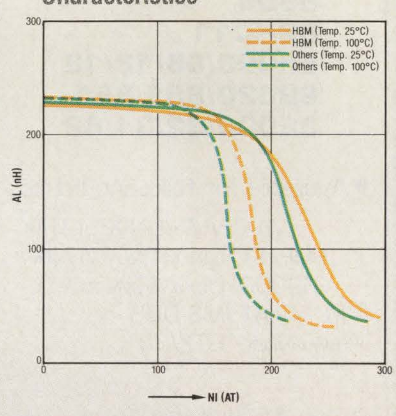


[mm]

Power Loss P_B vs Temperature



DC Premagnetization Characteristics



Material Characteristics

Material			2500B2	2500B3	HBM
AC initial permeability	μiac		2500 ± 20%	2500 ± 20%	1500 ± 20%
Effective saturation magnetic flux density*	Bms	Gauss	5000	5000	5100
		mT	500	500	510
Effective retentivity	Brms	Gauss	1300	800	1300
		mT	130	80	130
Effective coercivity	Hcms	Oersted	0.19	0.19	0.20
		A/m	15.1	15.1	15.9
Core loss (100kHz, 60°C) 100G (100mT)	P_B	kW/m^3	100	50	200
Core loss (100kHz, 60°C) 200G (200mT)			450	200	850
Curie temperature	T_C	°C	205	205	235

When Hm is at approximately 1200A/m (150e)

CIRCLE NO 188

Tokin

Tokin Corporation

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versions include step-and-repeat, panelization, mirror-image creation, rotation, and independent scaling on both the X and Y axes. The program also has facilities for converting the data from one plotting format to another and for writing the file to a magnetic tape that a photoplotter can accept. Both View and View+ run on the IBM PC family and compatibles, use menus of commands, and provide on-line help in the use of those commands. View, $500; View+, $1500.

Lavenir Technology Inc, 1041 Shary Circle, Concord, CA 94518. Phone (415) 680-7400. TLX 910-240-4273.

Circle No 414

MICROWAVE CAE

- *Synthesizes coupler dimensions from required impedance values*
- *Analyzes coupler frequency response, insertion loss*

The MSAcouplers package includes four programs that run on the IBM PC or compatibles. These programs aid in the design of the directional couplers used by the RF-microwave community. All four programs provide synthesis of coupler dimensions from the desired coupling level or from impedance values (Z_{OE} and Z_{OO}), as well as synthesis of coupler impedance values from the dimensions of the device. The programs allow you to determine the coupler's impedance sensitivity to changes in dimension caused by manufacturing tolerances. You can also determine the insertion loss caused by finite conductivity and by surface roughness in the metals used. The programs can perform a 4-port frequency analysis of the coupler. The four programs, available separately, are Lange, for microstrip interdigitated couplers; MsCup, for microstrip directional couplers; SlCup, for stripline directional couplers; and WgtCup, for waveguide, multihole, topwall couplers. Lange, $1200; MsCup, $495; SlCup, $495; WgtCup, $2200.

Microwave Software Applications Inc, Box 1736, Norcross, GA 30091. Phone (404) 441-9193.

Circle No 415

LISP DEVELOPMENT

- *Common Lisp with interface to C*
- *Runs on IBM PC and compatibles*

TransLisp Plus provides more than 400 Common Lisp primitives, an interface to the C language, and a variety of debugging tools. An optional run-time version is available. The package runs on an IBM PC or compatible that's equipped with at least 320k bytes of RAM and one 360k-byte floppy-disk drive. It can use as much memory as is available (to 640k bytes max) and will use an 8087 coprocessor if one is present in the system. The interface to Microsoft C makes the program more versatile; you can, for example, write a C program and add it as a new function to the Lisp program. Alternatively, you can add a small amount of Lisp code to an existing C program, or integrate code from C libraries into your Lisp application. You can distribute the optional run-time interpreter together with the programs that you write when using this Lisp software; your written programs thereby become stand-alone software packages. Debugging tools include a trace facility; a pretty printer that makes your source code easier to read; the Cross

Reference package, which shows where variables and functions are stored; Traceback, which steps through a top-level form; and Break, which forces the computer to break out of an infinite loop. You can invoke the fast editor, as well as DOS commands and applications, from within the program. The run-time version is available separately but requires the parent program. TransLisp Plus, $195; run-time version, $150.

Solution Systems, 335 Washington St, Norwell, MA 02061. Phone (800) 821-2492; in MA, (617) 659-1571.

Circle No 416

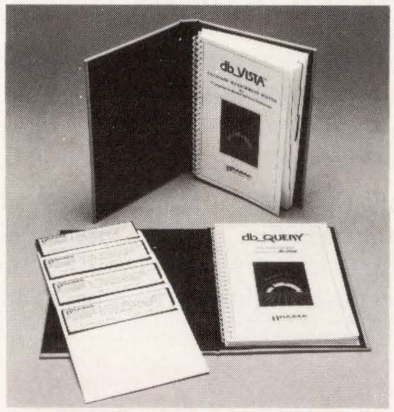
SUBROUTINE LIBRARY

- *Fortran math subroutines for IBM PC*
- *Compatible with Microsoft Fortran compiler*

The Numerical Analyst library of Fortran scientific subroutines provides mathematical programming aids for users of IBM PCs and compatible computers. The source-code routines include numerical integration; solutions of linear equations; a differential-equation solver; curve fitting; statistical procedures; and a selection of mathematical functions such as factorials, elliptic integrals, orthogonal functions, and Bessel functions. Its manual contains instructions on the use of each function and subroutine, listings of sample programs, and definitions of the library's error messages. For each error message, the manual suggests a response that will allow you to correct the error or to abort gracefully. You'll need a PC with at least 256k bytes of memory and two disk drives (an 8087 coprocessor is desirable but not essential). You'll also need Microsoft's Fortran compiler. $295.

Magus, Box 390965, Mountain View, CA 94039. Phone (916) 722-1580.

Circle No 417



DATABASE QUERY

- *Provides sorting and conditional-expression evaluation*
- *Can export results in ASCII or DIF file formats*

The db_Query program is a query-language system for use with the vendor's db_Vista, a database-management system for C-language application development. The query program is based on the Structured Query Language (SQL). According to the company, the software offers anyone developing applications in C a more familiar, relational view of a database, while retaining the speed and other advantages of the complex network database model used by db_Vista. First, you set up an environment consisting of user-oriented field-name aliases and formats, procedure files, report forms, and related data. Then you can query the database from a C program by passing a string, containing the SQL statement, to a function called d_query, which either executes the query or returns an error message. This function is part of a library that provides all the facilities you need in order to query the database and display the results. These facilities evaluate conditional expressions in the query, let you sort output on as many as 10 fields in ascending or descending order, and let you generate results in ASCII or DIF for further processing. The program is available in versions that run under MS-DOS, Unix (and its derivatives such as Xenix and Ultrix), and VAX/VMS. From $195.

Raima Corp, 3055 112th Ave NE, Bellevue, WA 98004. Phone (206) 828-4636. TWX 650-301-8237.

Circle No 418

FILTER DESIGN

- *Computes component values for Chebyshev filters*
- *Prints schematic with circuit constants*

RF Notes 3 Volume 3 is a set of programs that compute circuit constants for first- to seventh-order lowpass, highpass, bandpass, and band-reject filters with Chebyshev response. The programs all run on IBM PCs or compatibles that are equipped with 256k bytes of RAM, an IBM Color Graphics Adapter (CGA) or compatible graphics interface, and PC DOS 2.1 or later versions. The package consists of four diskettes, each of which is devoted to one of the four transfer functions. Each disk contains four programs that allow you to achieve 0.01-, 0.1-, 0.5-, or 1.0-dB ripple, respectively. Each program prompts you for all necessary inputs and, upon completing the computations, prints a schematic incorporating those circuit constants that will give the desired response. You can also print a curve of the predicted response. The program can compute the predicted loss at any specified frequency. You can use it to design filters for any frequency range from audio through UHF. Similar packages are available for Butterworth (Volume 1) and Bessel (Volume 2) responses. Butterworth, $200; Bessel, $200; Chebyshev, $220.

Etron RF Enterprises, Box 4042, Diamond Bar, CA 91765. Phone (714) 594-8741.

Circle No 419

GRAPHICS EDITOR

- *Provides graphics primitives and six text sizes*
- *Sends output to bit-mapped laser printer*

Mass-11 Draw is a mouse-driven freehand graphics editor that runs on the IBM PC/AT and on Toshiba 3100 lap-top computers. The program provides graphics primitives such as lines, circles, arcs, squares, curved-edge boxes, and other basic shapes. The package includes symbol libraries for use in making schematic diagrams and charts (you can also create and store your own icons). You have the option of working with a grid or with a plain background; on-screen rulers aid in precise work. You can read PIC and

HPGL graphics files and modify the drawings or incorporate them in documents that you create with the vendor's word processor. The graphics editor can send its output directly to full-page, bit-mapped laser printers. To run the editor, you'll need at least 512k bytes of RAM in a PC/AT, as well as the IBM Enhanced Graphics Adapter (or an equivalent graphics board). $495.

Microsystems Engineering Corp, 2400 W Hassell Rd, Suite 400, Hoffman Estates, IL 60195. Phone (312) 882-0111. TLX 703688.

Circle No 420

OPERATING SYSTEM

- *Lets you develop an application by editing a shell*
- *Occupies less than 4k bytes of EPROM*

The SK-11 is the kernel of an operating system for the 68HC11 controller-on-a-chip. It resides in EPROM and occupies less than 4k bytes. To develop a real-time process-control application, you edit the predefined shell that is included in the package, setting up a control block that defines how the kernel is to access your initialization, background, and interrupt-servicing routines. You can download data for development in RAM. The kernel has utility routines for double-precision multiplication; EEPROM erasure and reprogramming; and serial communications, which use the on-chip SCI port. The built-in commands can erase an EEPROM in bulk, cold-start the kernel software, execute your applications code, download S-records, and display help screens. You can add other commands to the kernel. The package consists of a diskette in IBM PC format that contains source code for both the 68HC11 kernel and the user-program shell, one 2764 EPROM containing the kernel object code and another containing object code for a sample user-program shell, and a user's manual that includes listings of the SK-11 software. $125.

Allen Systems, 2151 Fairfax Rd, Columbus, OH 43221. Phone (614) 488-7122.

Circle No 421

MATH LIBRARY

- *Single- or double-precision routines*
- *Runs on the MC68HC11 μP*

The 68HC11 math library includes trigonometric, logarithmic, and exponential functions; data-conversion procedures for converting ASCII characters or integers to or from the floating-point format; and floating-point utility procedures. Its floating-point number representation conforms to IEEE Standard 754. The single-precision version (FPAC) occupies 3275 bytes of code space and performs 4.9k flops on a 2.1-MHz 68HC11. The double-precision version (DPAC) occupies 4520 bytes of code space and performs 400 flops. Both versions are available for IBM PCs, PC/XTs, and PC/ATs. FPAC, $950; FPAC and DPAC together, $1250.

US Software Corp, 14215 NW Science Park Dr, Portland, OR 97229. Phone (503) 641-8446. TLX 4993875.

Circle No 422

C FOR XENIX

- *C Interpreter now available to run under Xenix*
- *Can use the full 16M-byte address space*

C-Terp is a C interpreter that was originally introduced for the IBM PC and compatibles; it's now available for the PC/AT and compatibles under Xenix 286 System V version 2.1.3 (Microsoft's implementation of Unix System V). The interpreter allows you to use multiple modules and Include files. When you press the Run key, the software condi-

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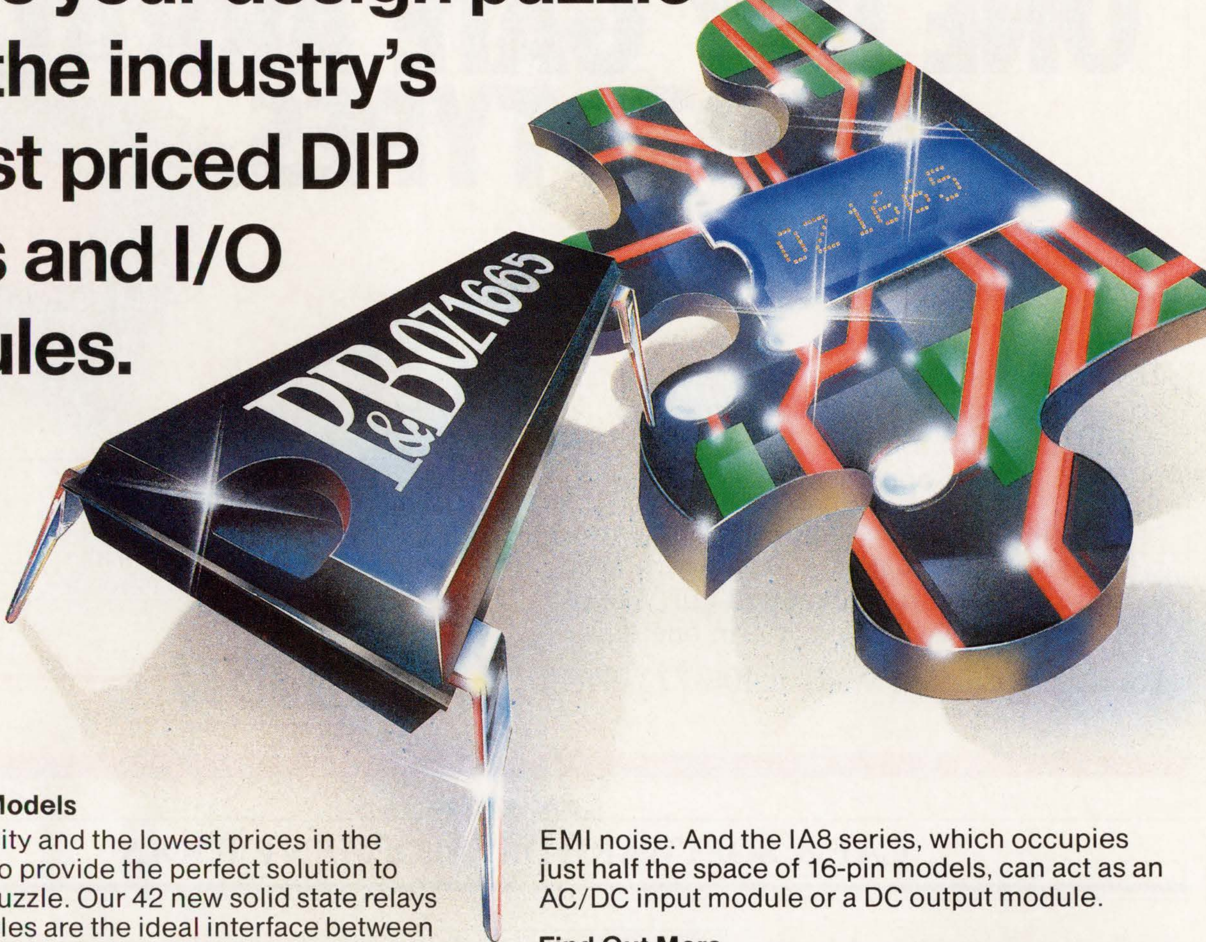

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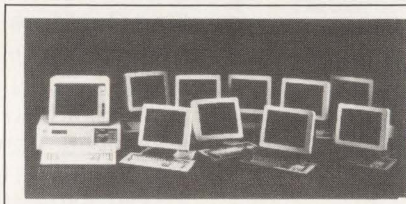
CIRCLE NO 183

CAE & SOFTWARE DEVELOPMENT TOOLS

tionally compiles each module, depending on whether it or one of its Include files has been modified since the last compilation. Interactive debugging features provide a split screen; one half lets you control the execution by commands to set breakpoints or step through your program; the other half displays the source code being executed. If the debugger detects an error, it switches you to the editor, placing the cursor at the point in the source code where the error was detected. The package comes with its own library of C functions and a batch file that can link almost any function in the Xenix C library into your program. Using the Termcap feature, you can adapt the interpreter to work on almost any terminal. $498.

Gimpel Software, 3207 Hogarth Lane, Collegeville, PA 19426. Phone (215) 584-4261.

Circle No 423



10-USER OS

- *Can share a hard-disk drive with another OS*
- *Integrated relational-database facility*

Version 2.0 of the vendor's operating system contains enhancements that let 10 users share an IBM PC/AT or compatible computer. This version also provides facilities for the use of three parallel printer ports, streaming-cartridge tape units, and high-capacity hard-disk drives. The system's chief advantage is the built-in, dictionary-driven, relational-database-management system, which lets inexperienced people set up complex databases and define the reports to be produced. To run the 10-user version, you need at least 512k bytes of RAM and single-port or multiport serial cards for the connection of user terminals. 10-user version, $1295; 6-user version, $995; 3-user version, $795.

Pick Systems, 1691 Browning, Irvine, CA 92714. Phone (714) 261-7425. TLX 655420.

Circle No 424

CROSS-DEVELOPMENT

- *Lets you develop software for NS32000 μPs*
- *10-MHz NS32032 runs Unix System V*

SYS32/20 consists of a coprocessor card that plugs into IBM PC-family computers, support software, and software-development tools. The coprocessor has a 10-MHz NS32032 μP and either 2M or 4M bytes of no-wait-state, onboard memory. You can also add the NS32082 MMU, the NS32201 timing-control unit, and the NS32081 floating-point arithmetic unit. The support software includes an operating system, an assembler, a linker, debuggers, and other tools that support optional compilers for C, Pascal, or Fortran 77. The operating system is a version of Unix System V.2 that's customized for the 32000 Series processors and operates with those μPs' optional demand-paged virtual-memory configuration. It also comes with a full-screen editor and utilities for custom-formatting documents. To run the board, you'll need an IBM PC/XT, PC/AT, or compatible computer equipped with 512k bytes of memory, a 20M-byte hard-disk drive, and PC-DOS version 3.1 or later. The board occupies one full-length expansion slot; a piggyback memory-expansion board may cover a second expansion slot. The PC/XT versions of the software come on 360k-byte disks; the PC/AT versions come on 1.2M-byte disks. With 2M bytes of memory, $2950; with 4M bytes of memory, $3950.

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UniPress Software, 2025 Lincoln Hwy, Edison, NJ 08817. Phone (201) 985-8000. TLX 709418.

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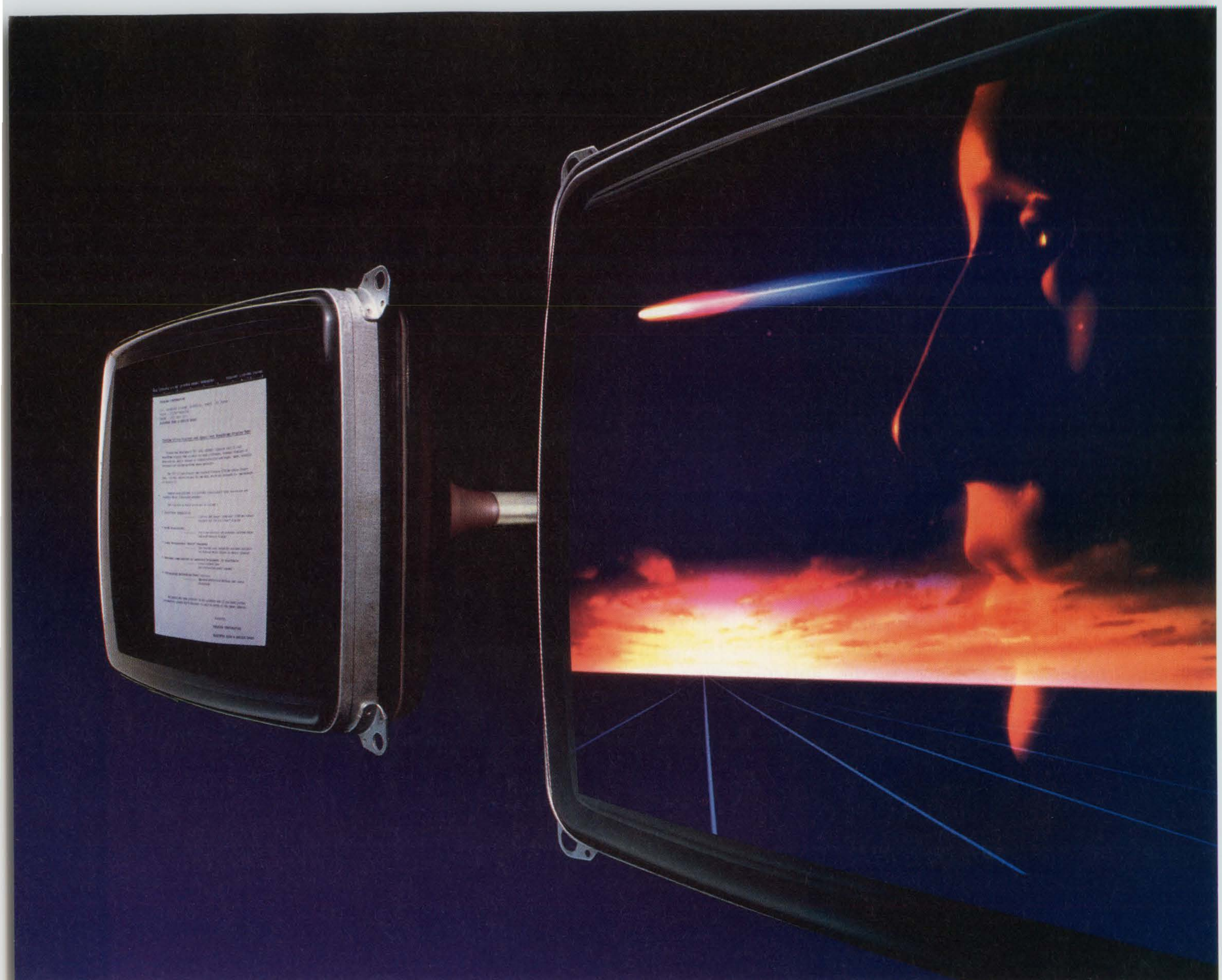

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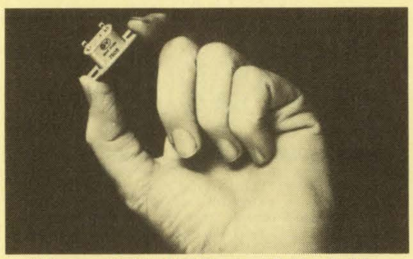

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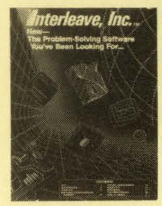

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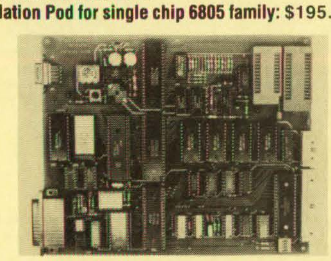

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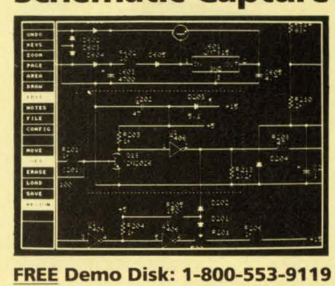

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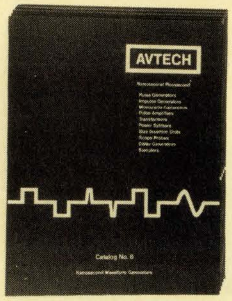

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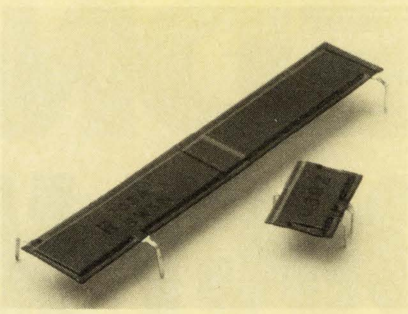

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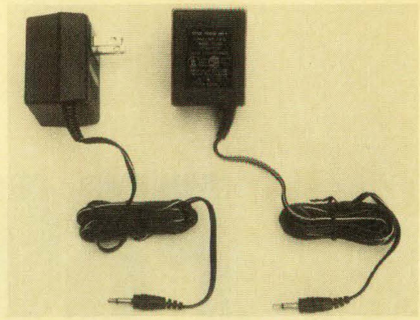

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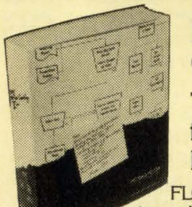

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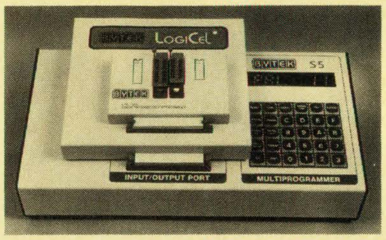

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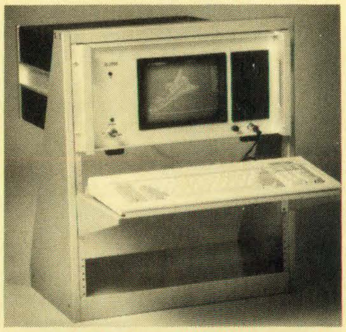

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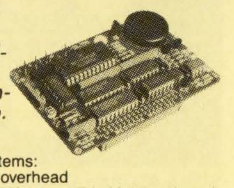

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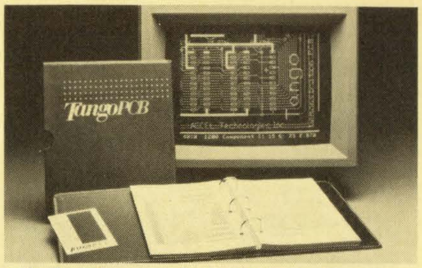

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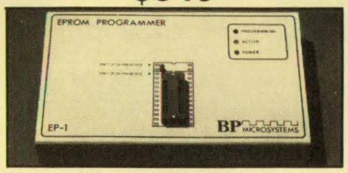

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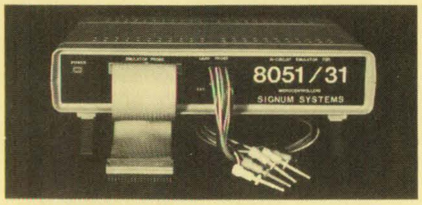

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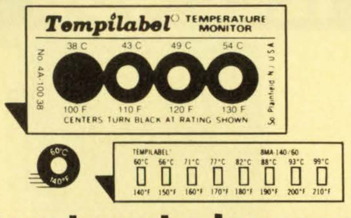

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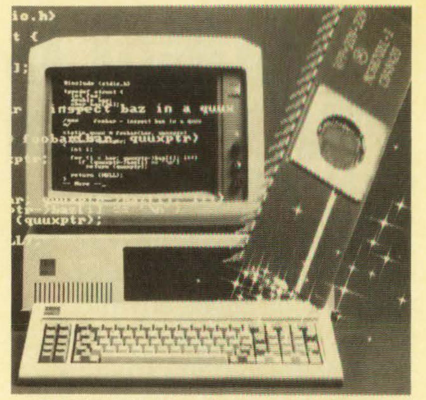

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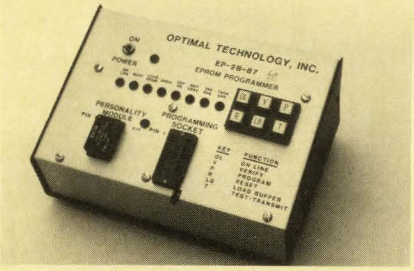

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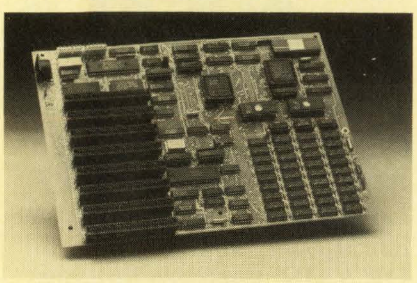

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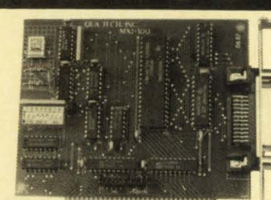
IEEE-488



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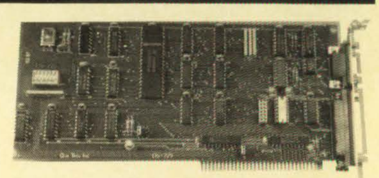

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CIRCLE NO 757

To advertise in Product Mart, call Joanne Dorian, 212/576-8015

Catalog covers products for rent (with option to buy)

This 1987 rental-product guide lists more than 1000 pieces of electronic industrial, test, and telecommunications equipment manufactured by such companies as Hewlett-Packard, Tektronix, Intel, Honeywell, Anritsu, and Fluke. The 198-pg illustrated catalog incorporates overviews, product descriptions, specifications, and selection guides. Manufacturer and product indexes and cross-reference charts are included. The company offers different rental programs, such as short-term rentals and long-term leases, as well as options to buy. Products cataloged include oscilloscopes, protocol and microwave analyzers, signal sources and generators, PROM programmers, and plotters and printers.

Leasametric, Instrument Rental Div, 1164 Triton Dr, Foster City, CA 94404.

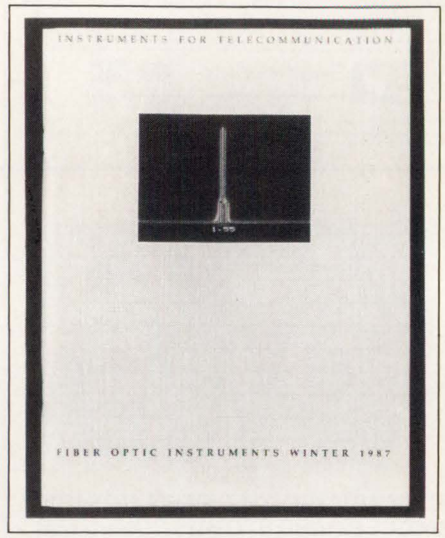
Circle No 427

Learn the basics of cooling equipment

Catalog 286 details the basics of air-moving devices and accessories necessary for cooling cabinet-mounted electronics equipment. The brochure briefly covers the different types of cooling units and presents photos and pie charts. Next, it discusses the vendor's custom units and design assistance. Following information on how to choose a cabinet-cooling blower are 27 pages that describe the company's products.

McLean Engineering, Div of Zero Corp, 70 Washington Rd, Princeton Junction, NJ 08550.

Circle No 428



Details on fiber optics

This 56-pg handbook touches on the manufacturer's line of fiber-optic measurement tools available during the winter and spring of 1987. It features testing applications, typical test configurations, and data on fiber-optic power, loss, spectral attenuation, and optical margin. Applications covered encompass optical power meters, optical-loss sets, fiber-optic sources, and attenuations. The book also contains a glossary of fiber-optic measurement terms.

Intelco Corp, 8 Craig Rd, Acton, MA 01720.

Circle No 429

Catalog features control instrumentation, components

The *Summary Catalog,* a 24-pg reference for the manufacturer's electromechanical control instruments, covers such products as free and rate gyroscopes, vertical indicators, potentiometers, accelerometers, pendulums, and solid-state rate sen-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Standard, 2 year
Product User's Name
Title
Div.
Company or Institution
Mail Stop/Dept.
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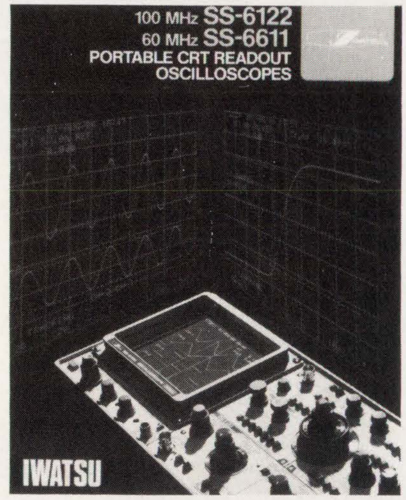
sors. In addition, it presents information on dynamic test systems, a 4-gimbal platform, stabilization systems, and magnetometers. Along with short product descriptions, the catalog contains specifications and dimensional drawings.

Humphrey Inc, 9212 Balboa Ave, San Diego, CA 92123.

Circle No 430

Brochure documents two portable oscilloscopes

This 12-pg, 4-color brochure presents data on two portable CRT-readout oscilloscopes, the 100-MHz SS-6122 and the 60-MHz SS-6611. The booklet graphically illustrates the scopes' simultaneous 4-cursor displays, high-accuracy counters, date/time displays, and accommodation of user-defined comments. In addition, it covers detailed specifications and optional accessories.



Iwatsu Instruments, 430 Commerce Blvd, Carlstadt, NJ 07072.

Circle No 431

Booklet describes properties of boron nitride

This 12-pg booklet provides details of the properties, applications, and benefits of Combat boron nitride, a material with high thermal conductivity that can withstand temperatures to 2800°C. Three-hole punched for loose-leaf filing, the catalog discusses solids, powders, and coatings and provides tables for each type.

Standard Oil Engineered Materials Co, Electronic Ceramics Div, Box 664, Niagara Falls, NY 14302.

Circle No 432

Set of books references products for 1987

These nine product handbooks are available separately or as a set. The books, which vary in price, cover such topics as memory components ($18), embedded controllers ($18), microcommunications products ($20), microprocessors and peripherals (2-volume set, $25), development tools ($18), OEM boards and systems ($18), military ICs ($18), component quality and reliability ($20), and system quality and relia-

bility ($20). The complete set costs $125. In the US and Canada, add 10% for postage (20% foreign) and, if necessary, local sales tax.

Intel Corp, Box 58065, Santa Clara, CA 95052.

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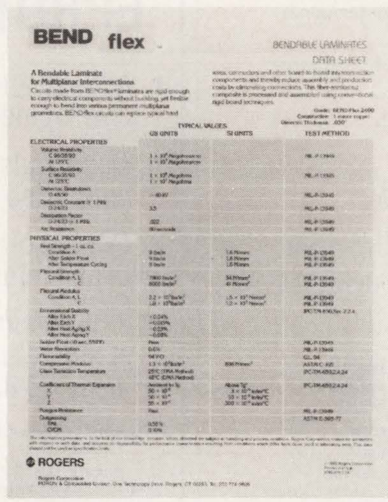

Data sheet on copper-clad epoxy

This 1-pg data sheet describes Bend/flex—a bendable laminate designed for multiplanar circuitry—which is an alternative to nondynamic flexible circuits and rigid pc boards connected with electronic conductors. The data sheet lists the copper-clad epoxy material's electrical properties, including volume and surface resistivity, dielectric constant, dissipation factor, and arc resistance. It provides information on physical properties such as peel strength, flexural strength, water absorption, and glass transition temperature.

Rogers Corp, Poron & Composites Div, 1 Technology Dr, Rogers, CT 06263.

Circle No 434

Report forecasts artificial-intelligence market

1986 AI Market Reports: A Review for the Corporate User is a 3000-pg publication that analyzes the strengths and weaknesses of 10 industry reports. The review evaluates each report and gives each an overall score based on 10 criteria, including the timeliness and accuracy of its information, its value for corporate decision making, and the depth of its technological coverage. Using charts and tables, the compendium tabulates and compares data from the various vendors. $47.50, plus $2.50 shipping and handling ($4.50 for overseas orders).

Knowledge Engineering, Box 366, Village Station, New York, NY 10014.

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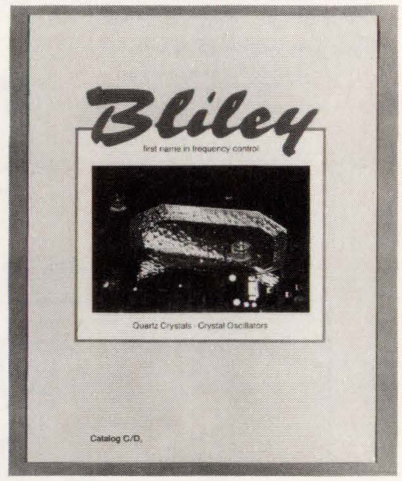


Specs for oscillators

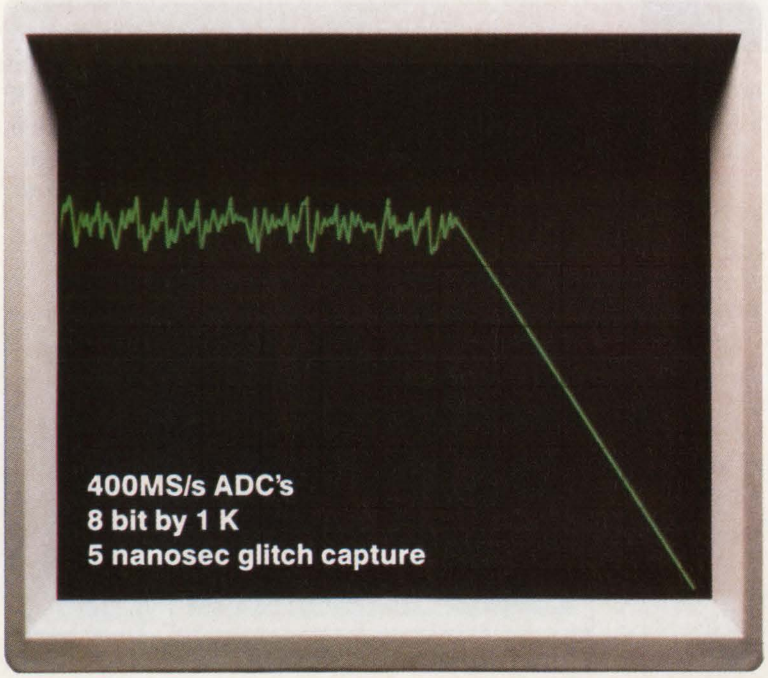
This 12-pg catalog updates the specifications for the vendor's surface-mount crystals and temperature-compensated and voltage-controlled oscillators. *Catalog C/D5* also contains an ordering-guidelines section to help in the selection of crystal and oscillator components, and it lists local factory representatives.

Bliley Electric Co, Box 3428, Erie, PA 16508.

Circle No 436

Magazine addresses information management

FYI, a magazine covering information on this corporation, provides news and features on developments, trends, and case studies. The winter 1987 edition, which contains 52



The cost of speed just went down.

Before now, if you wanted a high speed digital storage oscilloscope that didn't sacrifice accuracy, you had to pay an incredibly high price. Not any more. Because Gould's hot new 4070 series is here. Breaking the speed and price barrier with a super fast, super accurate instrument that starts at the unheard of price of $7,990.

2 or 4 channels. Incredible speed and accuracy.

Available in 2 or 4 channels, the 4070 DSO comes with 400 MS/s, 8 bit ADC's per channel. It's also the first portable DSO able to capture single shot signals to 100 MHz bandwidth (3.5 nanosec risetime). Plus Gould's low noise, low jitter design assures high measurement fidelity.

User Friendly.

Even if you've never used a DSO before, you'll find the 4070 easy to operate. As a bench instrument it offers familiar functionality, four reference set ups and a convenient *Auto Set-up*™ feature that automatically determines instrument settings for quick acquisition and display of unknown signals.

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There's also an optional integral four pen digital plotter for convenient hard copy documentation of test results. Full programmability, including front panel controls and menu selections over the IEEE-488 or RS423 bus. A 170 keypad option that quickly converts it into a powerful signal analyzer. Exclusive triggering capabilities and so much more.

So, if you want a full function DSO with speed, accuracy, and a low price, or information on any of Gould's oscilloscope, logic analysis, or recording products, call 1-800-GOULD-10 or write Gould Inc., Test and Measurement, 3631 Perkins Avenue, Cleveland, Ohio 44114.

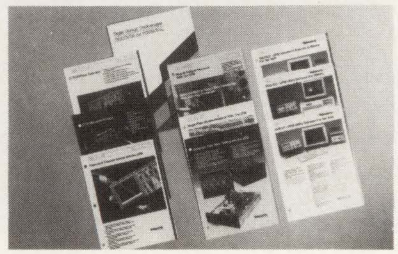
GOULD
Electronics

CIRCLE NO 208

pages, presents articles on personal-computer networks, NASA's Galileo space probe, Ada, and the Corporation for Open Systems, as well as news on company-specific projects.

Harris Corp, Melbourne, FL 32919.

Circle No 437



How to use digital storage scopes

This company is offering documentation to help you master the use of digital storage oscilloscopes. Including over 20 pieces of educational literature, the "Discover the Potential" series runs the gamut from elementary information to in-depth application notes. For instance, if you're a new DSO owner, you'll find a primer and several concept notes on waveform storage, peak detection, and transient capture. If you're more experienced, you might be interested in application notes covering such topics as disk-drive repair, process control, manufacturing-process design, and muscle-fiber and -fatigue research. To receive a copy of the 2230/2220 DSO index, which lists the literature available, phone (800) 433-2323.

Tektronix Inc, Box 500, Beaverton, OR 97077.

INQUIRE DIRECT

Data on CAD/CAE software

This brochure, which comes with data sheets, describes the vendor's line of low-cost CAD/CAE software for personal computers. The document highlights Draftsman EE, a graphics editor for schematic capture and pc-board design; DC/Check+, a package of routing tools that includes a design-rules checker; and DC/Autorouter II, a 1-mil-diagonal autorouter.

Design Computation Inc, 10 Frederick Ave, Neptune, NJ 07753.

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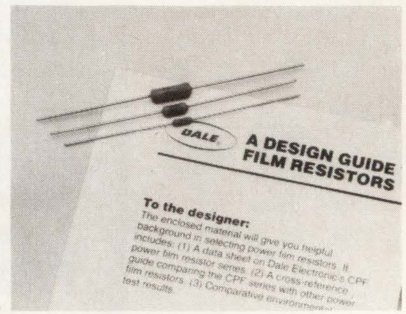


Guide reviews use of metal-film resistors

This designer's guide provides data on the company's CPF Series of flame-proof metal-film resistors, and it also cross-refers them with other types of metal-film and metal-oxide resistors. In addition to including specifications for the devices, the guide contrasts their flameproof coating with the flame-retardant coatings on many other power resistors.

Dale Electronics Inc, 2064 12th Ave, Columbus, NE 68601.

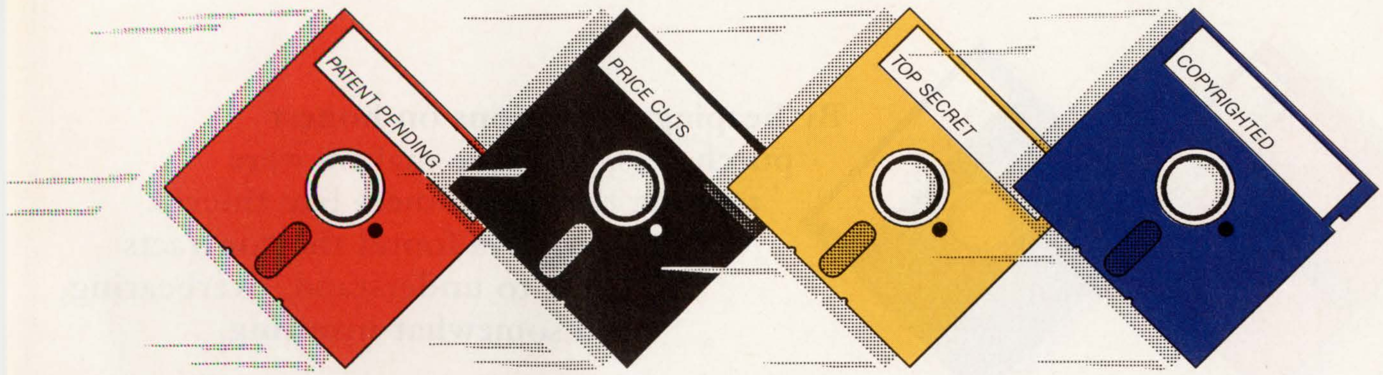
Circle No 440

Data on array processor

This 4-color, 8-pg brochure is devoted to the NMX-464, an array processor capable of single/double-precision vectoring for VAX and VAXBI systems. It uses block diagrams to illustrate the device's system architecture, memory structure, and data-processor architecture; it also lists hardware features and complete specifications.

Numerix Corp, 20 Ossipee Rd, Newton, MA 02164.

Circle No 441



Users benefit as software vendors drop bothersome guards against piracy

Joseph Iandiorio, *Waltham, MA*

Last fall, software vendors Lotus Development Corp, Ashton-Tate, and Microsoft Corp announced that they would no longer include technical and contractual restrictions in their software packages to block unauthorized duplication. Instead, the companies said, they planned to return to the traditional means of intellectual-property protection afforded by patents, trade secrets, and copyrights to fight the massive illicit copying that has eaten into software makers' profits.

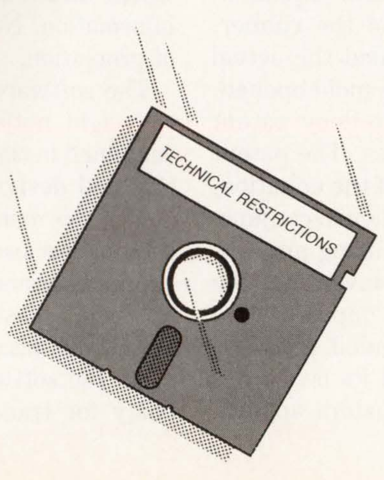
Two major considerations influenced the vendors' changes. First, both individuals and large organizations have complained loudly and often about the protective measures for software packages. Second, recent changes in patent, trade-secret, and copyright laws and procedures offer improved means of protection that better meet the needs of software vendors.

For large corporations, the changes mean that the companies can purchase more simply—and distribute more efficiently—large quantities of software products. For individuals, the changes mean that the bothersome protective devices on some (but not all) software packages will be removed, allowing them to back up their copies without risking being locked out of their disk. Also, manufacturers might cut their prices to encourage people to purchase copies rather than make them illicitly, thereby making illegal copying—and its risks—far less attractive.

Until last fall, technical and contractual restrictions were common parts of software packages. One technical scheme varied the structure and order of the data recording tracks or of the spaces in between. Some manufacturers included in their packages a hardware key containing codes that matched serial numbers on the disks. Users couldn't run the software until they inserted the keys into ports of the computers. If they gave away their copies, they had to give away their keys, too, and thus were left unable to use their own copies.

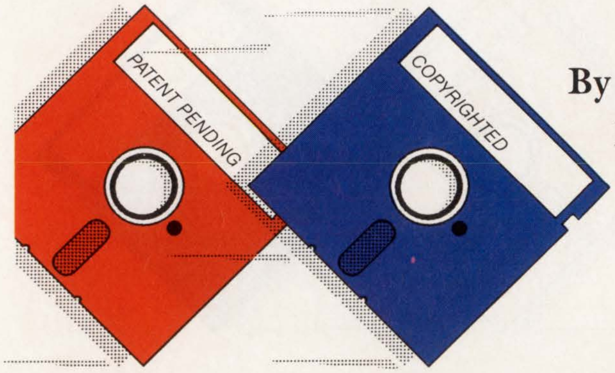
Technical schemes delayed but did not defeat copying by the dishonest and the mischievous alike. Even worse, by heaping such restrictions on honest purchasers, software makers were treating them like thieves. Furthermore, customers were unable to make archival copies and were helpless if an error or power failure damaged or destroyed their copies.

End users found the contracts that accompanied most programs equally annoying. Few of the contracts were negotiated; most were simply unsigned printed forms. Blister-packed software packages often came with shrink-wrap licenses informing buyers that, upon opening the package, they accepted the terms of the license.



Software customers disliked the criminal implications of the technical devices, and they found the contracts overbearing, difficult to understand, and somewhat insulting. Big customers began specifying only unprotected products from software makers. The Department of Defense, for example, flatly refused to accept any protected software.

Whether software makers would have responded to users' complaints without the help they received from recent changes in patent, trade-secret, and copyright protection is debatable. What's clear, however, is



By heaping restrictions on honest purchasers, software makers were treating their customers like thieves. The customers found the contracts difficult to understand, overbearing, and somewhat insulting.

that the protection for software through patents and through the coupling of trade-secret and copyright laws is ample and adequate.

The changes that occurred in the patent process had been brewing for a long time. From the mid-1960s to 1980, the software and legal communities debated whether patent protection should extend to computer programs. In 1981, the US Supreme Court ended the debate when it agreed to the patentability of a technique that permitted the altering or repositioning of parts of a computer's operating system without rebooting or using special software. The technique used firmware consisting of hardware elements that contained permanently programmed microcode; the firmware directed the data transfers between some scratchpad registers and a system base located in main memory.

The Court issued a definitive statement on software patentability later that year when it upheld the decision of a lower court that granted a patent for a software program. The Patent and Trademark Office (PTO) had earlier denied a patent for the process that listed among its patent claims the use of a digital computer and software program to operate a rubber-molding press. The software initiated an interval timer in the computer to monitor the length of each closure of the press. After receiving information on the mold's temperature, the computer calculated, using a particular equation, the proper reaction time for the cure of the rubber. When the calculated reaction time equaled the actual elapsed interval, the cycle ended and the mold opened.

The Supreme Court saw no reason to deny patent protection for the rubber-molding process. The patent claims did not seek to pre-empt the use of the equation, only to keep others from using that equation in conjunction with the other steps in the rubber-curing process. Inclusion of a computer program in an invention, the Court said, does not render the invention unpatentable.

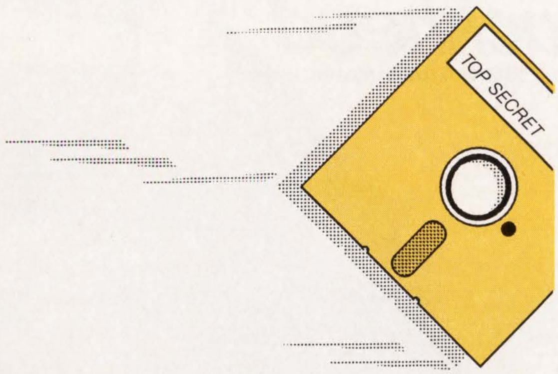
By the time the Supreme Court handed down its decision, the PTO had already proposed its own rules for the inclusion of program listings in patent applications. According to those guidelines, one could submit computer listings of 10 pages or less to be printed as part of the patent; longer listings could be submitted on paper or on microfiche as appendices and would be available separately from the PTO for inspection and purchase after the patent had been granted.

In response to the Court's decision, the PTO went further and declared that inventions that include an algorithm or computer program were indeed patentable, as long as the invention as a whole related to subject matter that was otherwise acceptable. In 1983, it granted the investment firm Merrill Lynch a patent for software that operated a cash-management account. The program automatically transferred funds among a brokerage security account, several money market funds, and a charge or checking account. The transfers consisted purely of data processing and used no new machinery or combination of machines.

Unlike the slow pace of change in the patent process, the rate of change in the trade-secret and copyright processes happened with surprising speed. In 1983, a Wisconsin software vendor's lawsuit over misuse of information in its users' manual resulted in a court decision that now lets software vendors guard the contents of their programs by obtaining both trade-secret status and copyright ownership—a seemingly unusual pairing because copyright applies to published works and trade-secret status refers to undisclosed information. No program had ever enjoyed both means of protection.

The software maker included in its users' manual a copyright notice and a warning that the information contained in the manual was proprietary: "The information and designs disclosed herein . . . are proprietary . . . ," the manual read, "and shall not be duplicated, used or disclosed, in whole or in part, except with the express permission of the owner."

When a customer provided the manual to a third party who misappropriated the trade secrets contained in it, the software vendor filed suit against the third party for trade-secret theft. Because copyright pro-



tects the form of a work and trade-secret status protects its contents or ideas, the court found no inherent conflict between federal copyright provisions and state trade-secret law. As a result, it ruled that the software vendor could indeed claim the product as a trade secret and also publish it, albeit for limited audiences such as those for users' manuals.

Copyright procedure protects trade secrets

To help protect trade secrets in software programs that are submitted for copyright, the Copyright Office has proposed a new procedure. In the past it had required software writers to submit their programs in one of the following forms: the first and last 25 pages of source code with some, but not most, portions blocked out; the first and last 10 pages of source code with no portions blocked out; and the first and last 25 pages of object code plus any 10 pages of source code with no blocked-out pages. Its new proposal includes a fourth alternative for submission that favors shorter works: Authors of computer programs of 25 pages or less can block out as much as 50% of the program, provided that there is enough substance to the remaining portions to show authorship. **EDN**

Author's biography

Joseph Iandiorio is patent, trademark, and copyright attorney in Waltham, MA. He earned a BSEE from Villanova University (Villanova, PA) and a JD from George Washington University (Washington, DC). Before opening his legal practice, he worked for three years as a patent examiner for the Patent and Trademark Office in Arlington, VA. He is a member of the boards of directors of the Small Business Association of New England and the Massachusetts Technology Corp, a state-sponsored venture-capital organization. In 1986, he was a delegate to the White House Conference on Small Business.

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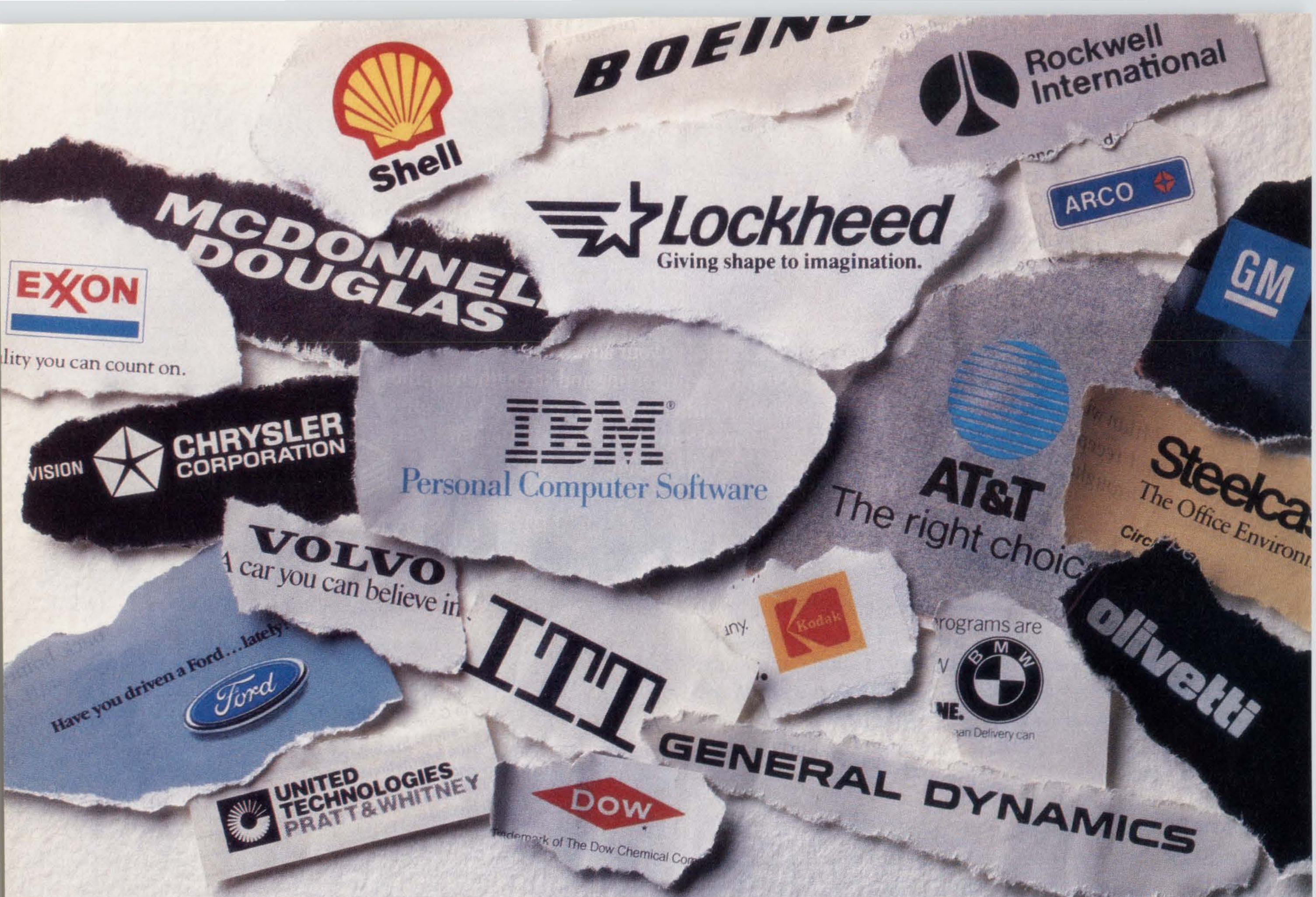

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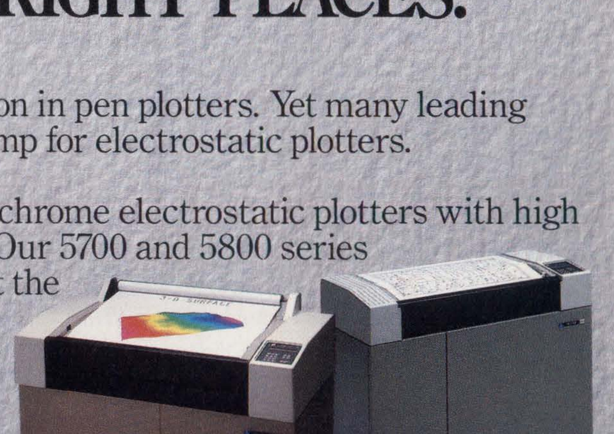

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NEW BOOKS

The 8086/8088 Family: Design, Programming, and Interfacing, by John Uffenbeck. 630 pgs; $37.95; Prentice-Hall Inc, Englewood Cliffs, NJ, 1987.

This book focuses on the 8086 family of microprocessors and microprocessor support components, as well as all of the compatible processors and coprocessors in this 16-bit microprocessor family. To understand this text, you need only a background in digital logic; the author makes no other assumptions. The four divisions of the book present information on the basic computer, the software, the hardware, and details of the 80186 microprocessor.

Optimization Using Personal Computers, by Thomas R Cuthbert Jr. 474 pgs; $44.95; John Wiley & Sons, New York, NY, 1987.

This book is a guide to optimization or nonlinear programming. It provides 33 Basic computer programs that illustrate the theory and application of methods that automatically adjust design variables. The book emphasizes the interaction between the user and the computer by offering hands-on experience with the mathematics and the computational procedures of optimization. Using concrete examples and illustrations, the author reviews matrix algebra; he avoids mathematical abstraction wherever possible.

Software Quality Assurance & Management, by Michael W Evans and John J Marciniak. 327 pgs; $37.95; John Wiley & Sons, New York, NY, 1987.

You can learn proven solutions to the recurring management and production problems involved in software development with this book. It shows you how to plan, schedule, implement, execute, and control software development in a project environment. The book teaches you how to integrate diverse disciplines, technical procedures, and administrative project controls into a cohesive, focused set of activities.

Optical-Fiber Transmission, by EE Bert Basch. 544 pgs; $69.95; Howard W Sams & Co Inc, Indianapolis, IN, 1987.

This reference book highlights issues of modern fiber-optics technology and provides fundamental engineering principles for all parts of a state-of-the-art optical-fiber communication system. Topics include nonlinear phenomena in single-mode fibers, communication theory as applied to optical systems, coherent optical systems, derivation of electromagnetic fields of single-mode fibers, and analog and digital transmission systems.

CIRCLE NO 17

NEW BOOKS

Microwave Frequency Synthesizers, by Ronald C Stirling. 189 pgs; \$37.33; Prentice-Hall Inc, Englewood Cliffs, NJ, 1987.

This book is a reference for the design of wideband microwave frequency synthesizers, with emphasis on the capability to switch between frequencies in fractions of a microsecond. It describes the methods and test equipment needed to measure sideband phase noise and introduces a new design approach where programmable frequency dividers provide a variable reference to the synthesizer's phase detector. The book also examines the advantages of using combined direct and indirect techniques to optimize performance vs complexity as a function of slower frequency switching speeds.

Integrated Circuits in Digital Electronics, 2nd ed, by Arpad Barna and Dan I Porat. 371 pgs; \$39.95; John Wiley & Sons, New York, NY, 1987.

The book combines elementary theory and practical applications. This edition provides information on the advances that have taken place in the technology since the first edition was published 13 years ago. The material includes over 400 examples and describes problems that you can solve with step-by-step procedures.

A Basic Atlas of Radio-Wave Propagation, by Shigekazu Shibuya. 778 pgs; \$69.95; John Wiley & Sons, New York, NY, 1987.

This book includes all the design elements required for VHF, UHF, and SHF radio in easy-to-follow chart form. Using a computer, you can explore every problem in this book. The book examines basic concepts; a variety of propagation paths, including free-space reflection, troposcatter, absorption, and passive-relay; noise and S/N ratio; and fading estimation and system evaluation.

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Sperry Commercial Flight Systems Division of Honeywell offers you the opportunity to let your career plan take flight. Our new and ongoing programs create opportunities for you in both our Air Transport Systems and Business Aviation Systems groups. Career opportunities are available in the following areas:

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Control Systems

In this area, you will be involved in guidance and control systems analysis and hardware/software design trade-offs. Specifications designs, including guidance, navigation and control algorithm development, as well as systems integration and installation, flight test and customer liaison activity, are a part of these areas. In addition, advanced work encompasses design of redundant digital fail-op systems, fly-by-wire and fly-by-light systems, as well as involvement with automatic flight control system analysis.

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These positions involve the development of new processor/bus architectures and specifications to support fault tolerant/redundant airborne applications. To qualify, you should have experience with embedded multiprocessor-based avionic systems.

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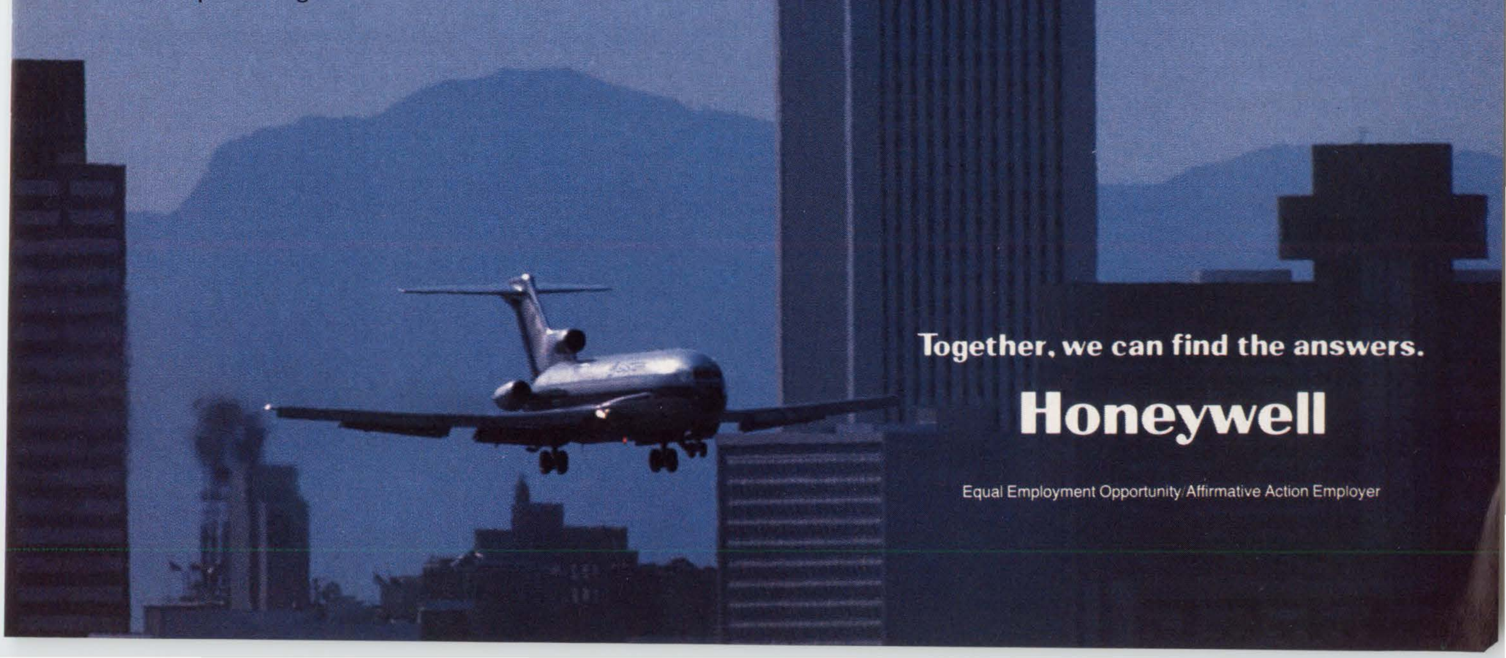

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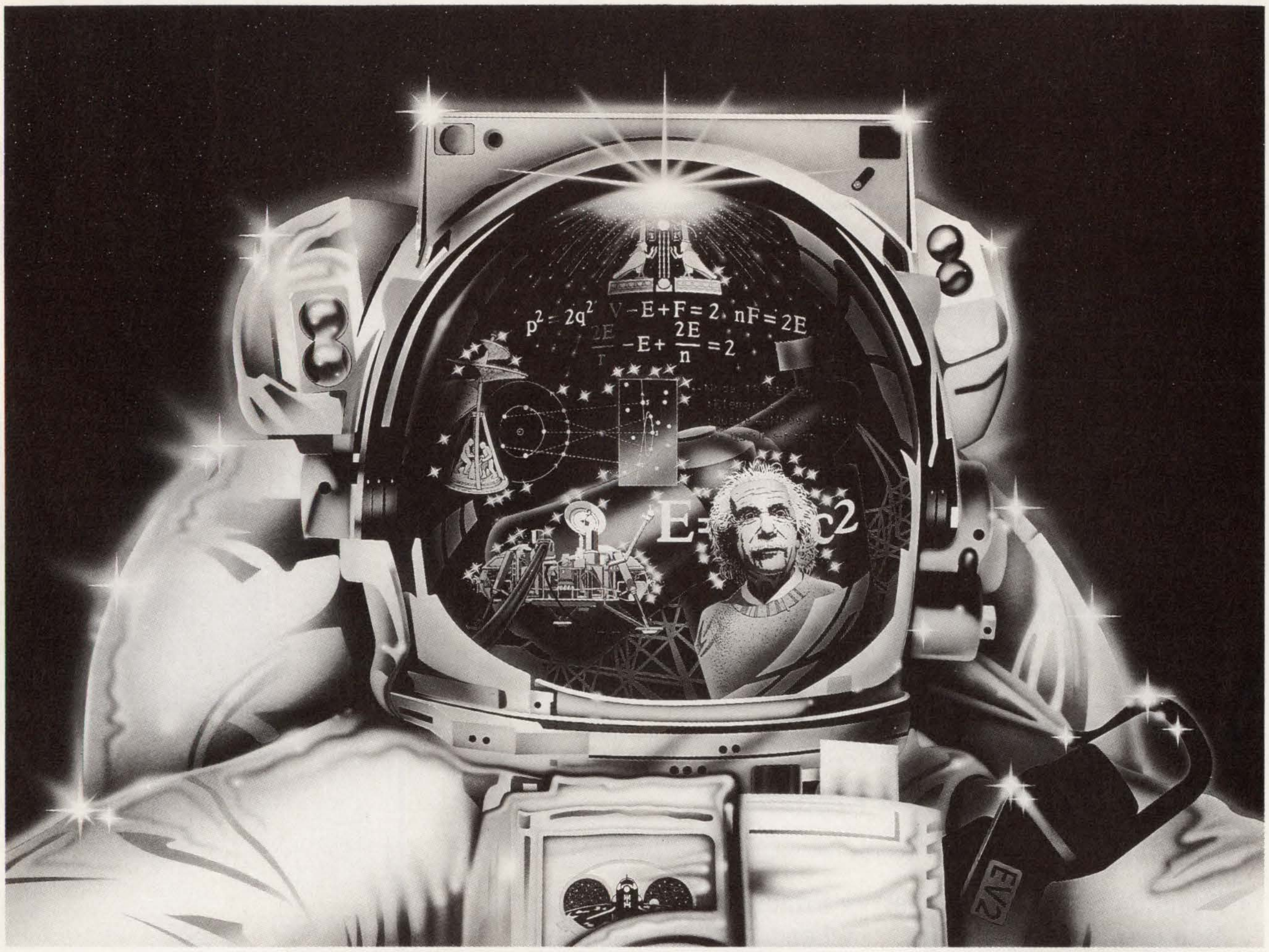

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ERIM REPORT #6a

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The 3D Sensor

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ERIM's 3D sensor technology is providing an excellent alternative to human stereo vision in control systems for future autonomous land vehicles (ALV) that will operate in environments too hostile for man. ERIM 3D sensing units are also being used in the Ohio State University Adaptive Suspension Vehicle (ASV) to provide automatic "subconscious" functions of attitude control and detailed foot placement for both forward and turning movements.

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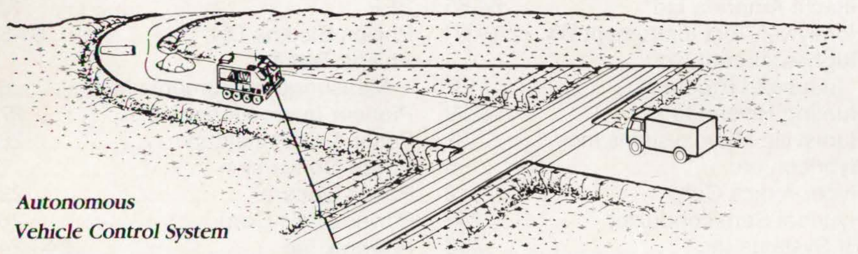

Autonomous Vehicle Control System

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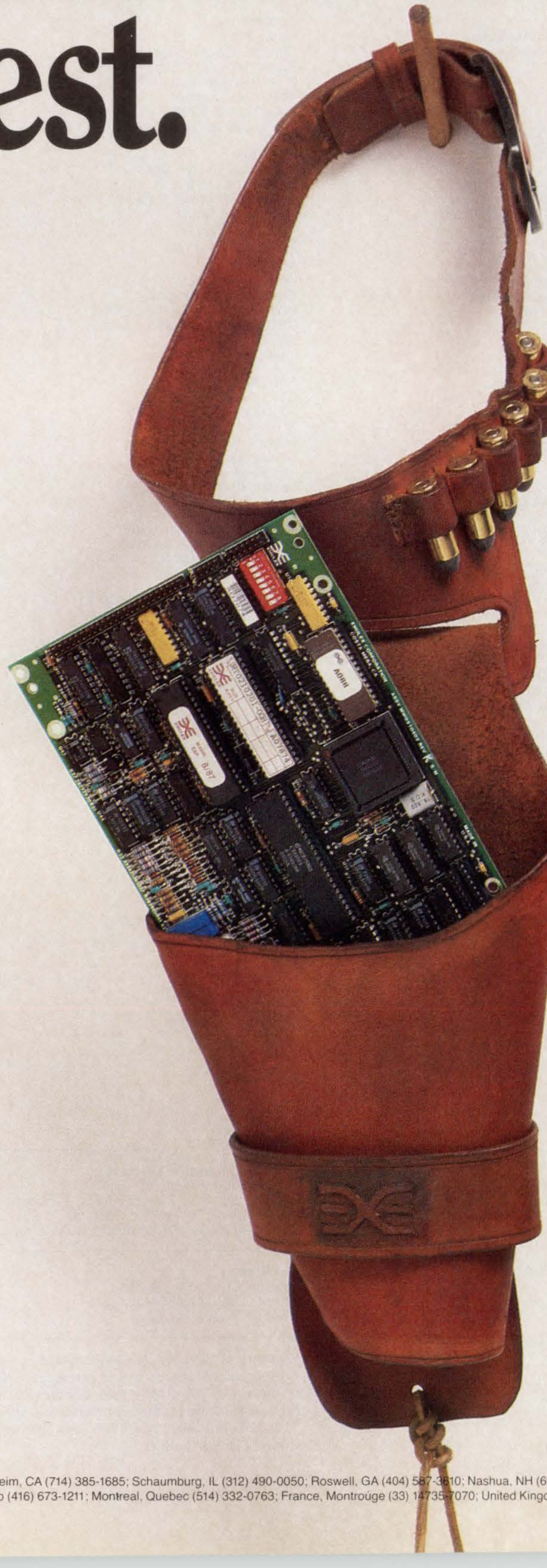

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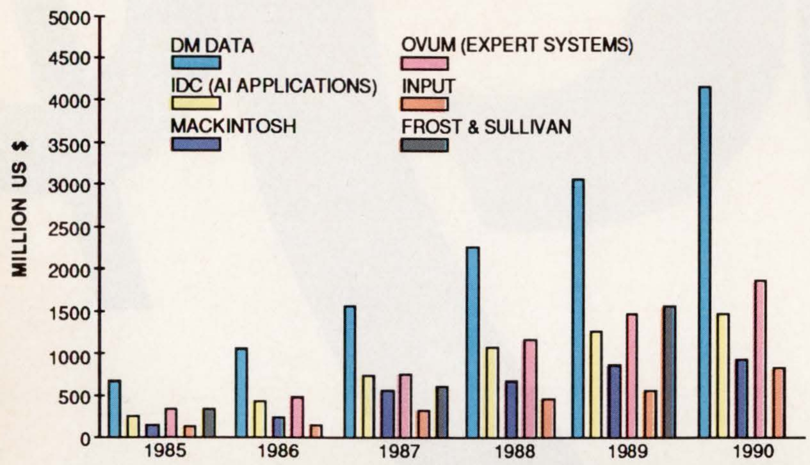
LOOKING AHEAD

EDITED BY GEORGE STUBBS

AI MARKET FORECASTS



NOTE: FIGURES ARE FOR TOTAL ESTIMATED MARKET, HARDWARE, AND SOFTWARE. REPORTS MAY COVER DIFFERENT CATEGORIES. DATA FROM OVUM AND IDC WAS GATHERED, IN EACH CASE, FROM ONE OF TWO REPORTS SUBMITTED FOR REVIEW.

(SOURCE: KNOWLEDGE ENGINEERING AND SCS ASSOCIATES)

Market forecasts vary widely for AI products through 1990

A factor of five to one measures the difference between various research companies' recent forecasts for the commercial success of artificial-intelligence (AI) products in 1990, says Knowledge Engineering (New York, NY), a publisher of a newsletter covering the AI field, and SCS Associates (Mountain View, CA), an AI consulting firm. The most optimistic prediction comes from DM Data (Scottsdale, AZ), which projects a $4.2 billion AI market in 1990. The most pessimistic prediction is Input's (Mountain View, CA)—$885 million in 1990.

Knowledge Engineering and SCS Associates joined forces to conduct an evaluation of these forecasts. They judged each with respect to such factors as timeliness and accuracy of information, depth of technological coverage, distribution of interviews conducted for trend analysis, and value as a function of information delivered per dollar spent. They found that, along with variation in market forecasts, a wide variation in attention to such factors exists—though not necessarily in direct proportion. Most companies' reports exhibited unique strengths and weaknesses. Prices for the reports range from $15,000 for Mackintosh International's (Saratoga, CA) publication on the expert systems market to $195 for DM Data's *AI Trends '86*.

The Knowledge Engineering/SCS review panel notes from the outset that an AI market is a moving target, making it difficult to derive useful comparisons between market forecasts. One company characterizes run-time expert systems as conventional software, where others regard expert systems as a prime example of a commercially ready AI application. In 1974, spelling checkers were considered AI products; today, some spreadsheet programs contain elements of AI technology.

Another factor making it difficult to compare market predictions is the forecasters' varying definitions of the associated hardware market. DM Data includes in its definition of AI hardware any machine that has ever been used for AI. Dataquest (San Jose, CA), because it views run-time expert systems as conventional software, implies that sales figures for AI hardware would include only those for symbolic processors. (Dataquest will issue an AI market report early in 1987, according to Knowledge Engineering.) Input counts only those machines used exclusively for AI work.

The review panel cautions that those professionals who are trying to extract information from these reports should be sure that the reports clearly define the market, contain up-to-date information, and describe sources of data. The panel also advises prospective report buyers that a purchasing decision should not be based on publicity; it claims that the trade press tends to give the most coverage to the most optimistic reports. In addition, report buyers should have an idea of what they are looking for before they buy; some reports provide good analysis but no projections, while others offer projections but poor analysis.

Several reports contain insights that deviate from the usual blanket optimism one finds in many market surveys. In *Natural Language Computing: Commercial Applications*, Ovum (London, UK) gives a cautious view of the development of natural-language processing: "People looking for quick results from investing their time and money should not venture into this field . . . But the markets are there, the means to serve them are in view, and for those who have the stamina, natural-language processing will prove a rewarding technology." IDC (Framingham, MA), in *AI Techniques, Tools, and Applications*, observes that artificial vision and natural-language processing are the two technologies most likely to benefit from parallel processing, because the related tasks deal with many elements simultaneously.

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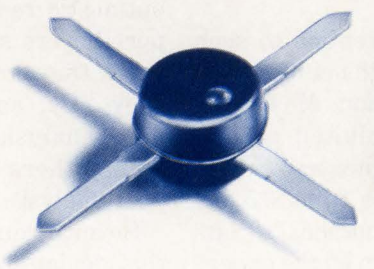

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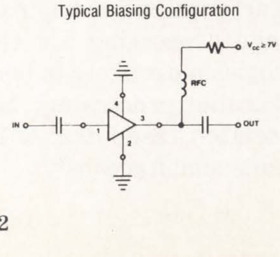

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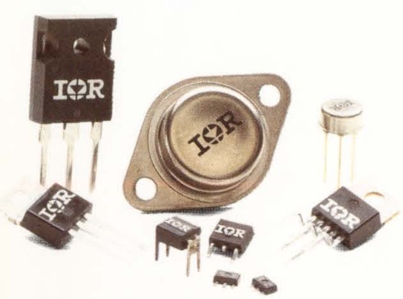

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