SEPTEMBER 16, 1981

A CAHNERS PUBLICATION

EDN

EXCLUSIVELY FOR DESIGNERS AND DESIGN MANAGERS IN ELECTRONICS

Understand noise in phase-locked loops

Implement the FFT on your personal μC

Second annual μC Operating Systems Directory

Our MD-300/SP Memory Board Test System is a new addition to our well-known MD-300 family. It dynamically tests memory boards and complete memory systems better than any system on the market. It's also suitable for testing complex memory systems and memory boards.

The MD-300/SP is a complete, stand-alone computer-controlled system, using the DEC LSI-11 computer. It's especially suited for the production test environment, offering a simple solution to complex hardware interfaces. Not to mention a powerful Interactive Program Generator which cuts applications programming time to hours instead of the usual days.

As if this weren't enough, the MD-300/SP can pay for itself. Because your savings from testing boards instead of systems are significantly larger. In fact, we'll give you a free, no-obligation return on investment presentation to prove it. You be the judge. And the free demonstration is yours for a phone call.

After you see what the return on your investment can be, you'll think $75,000 is one sweet steal.

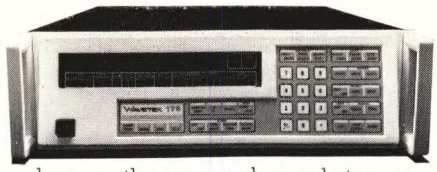
EATON Semiconductor Equipment

AT $75,000, OUR BOARD TESTER IS A STEAL.

Eaton Corporation, Memory Test Systems Division, 21135 Erwin Street, Woodland Hills, CA 91365, (213) 887-5550

CIRCLE NO 1

Using Wavetek's Model 175 Arbitrary Waveform Generator is like drawing on your oscilloscope. You have a 256 x 255 point grid to work with. Time is along one axis, amplitude is along the other. Simply program the waveform, point by point, either from the front panel or via the GPIB bus. ARB stores the shape you've programmed and will duplicate it at any frequency and amplitude you select. You can also edit point by point if you decide to



change the wave shape later on.

Operational modes include continuous, triggered, and even triggered burst—which will take care of almost any application.

If you've ever tried to generate sin x/x or any other non-standard function on ordinary equipment, you know what a breakthrough ARB represents. Now, instead of choosing just sine, square or triangle outputs, you can be completely arbitrary. Provided you've chosen Wavetek's Model 175 to be arbitrary with!

Wavetek San Diego,
9045 Balboa Ave., P.O. Box 651,
San Diego, CA 92112. Tel: (714) 279-2200; TWX 910-335-2007.

WAVETEK®

For literature, Circle no. 64

For demonstration, Circle no. 63

The ARB generates any waveform you can draw.

And we have the pictures to prove it.

Pro-Log M980 Programmer: Best in the field.

Built rugged to keep working.

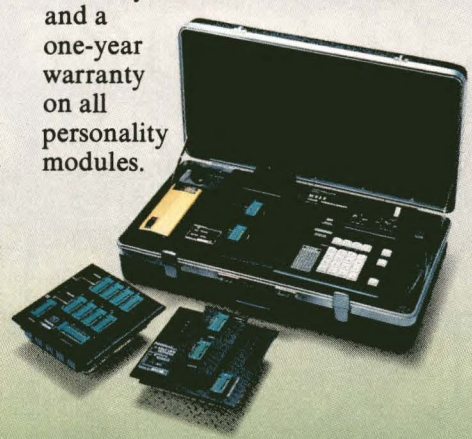
Weighing less than 22 pounds and compact enough to fit under an airplane seat, the Pro-Log M980 is still the most rugged PROM programmer for troubleshooting in the field.

Pro-Log programmers have been used on the Alaskan pipeline, in steel mills and in other hostile environments. One even survived a tornado that destroyed the building around it!

Look inside the M980 and you'll see there's little to go wrong. We designed it for reliability with a limited number of functional high-density parts and interconnects. A recent service study indicated that you can expect *10 years* of failure-free performance from the M980.

Backed by the industry's longest warranties.

Based on the proven quality of 9,000 Pro-Log programmers and 20,000 personality modules performing reliably worldwide since 1973, Pro-Log gives you a two-year warranty on M980 control units and a one-year warranty on all personality modules.



Remote control for troubleshooting and updating.

For easy diagnosis and pattern updating in the field, connect the M980 to a computer, terminal or modem via the RS232C or parallel interface.

Find out more.

For full details, send for our 32-page M980 brochure. Or better yet, ask for a free demonstration.

Write or call Pro-Log Corporation, 2411 Garden Road, Monterey, CA 93940, phone (408) 372-4593.

PRO-LOG CORPORATION

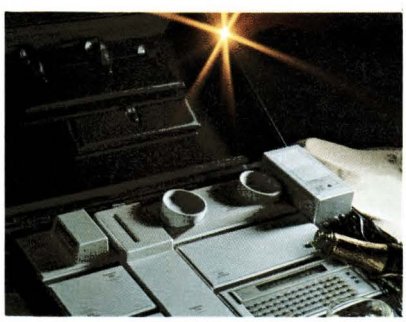
CIRCLE NO 2

EDN

SEPTEMBER 16, 1981 • VOLUME 26, NUMBER 18 • EXCLUSIVELY FOR DESIGNERS AND DESIGN MANAGERS IN ELECTRONICS

Frequency counters *span a wide spectrum of parameter choices (pg 33).*

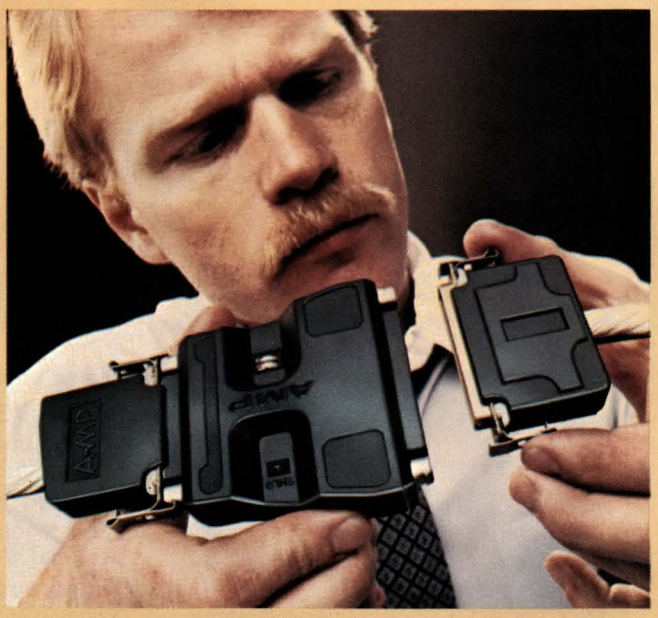
Intelligent terminals *develop along two paths to provide for varying needs (pg 45).*



On the cover: *Hardware and software innovations in hand-held computers provide problem-solving power in a host of unusual applications. Turn to pg 70. (Photo by Alexander Kruper, courtesy Panasonic Inc)*

EDN (ISSN 0012-7515) is published biweekly (except monthly in July and December) by Cahners Publishing Company, Division of Reed Holdings, Inc, 221 Columbus Avenue, Boston, MA 02116. Norman L Cahners, Chairman; Saul Goldweitz, President; William M Platt, President, Boston Division. Second class postage paid at Pontiac, IL 61764 and Oakland, CA 94623. Postmaster: Send Form 3579 to EDN, 270 St Paul St, Denver, CO 80206. Advertising and editorial offices: 221 Columbus Ave, Boston, MA 02116. Phone (617) 536-7780. Subscription offices: 270 St Paul St, Denver, CO 80206. Phone (303) 388-4511. EDN is circulated without charge to those qualified. Subscription to others in the continental US: $2/copy (special issues may vary), $30/year; international subscriptions: $5/copy ($3/copy in Canada) (special issues may vary), $70/year ($40/year in Canada), with air mail delivery available for $150. Send requests for qualification forms and/or change of address to subscription office.

RS 232 and RS 449, bring them together with our subminiature Ds. It's easy.

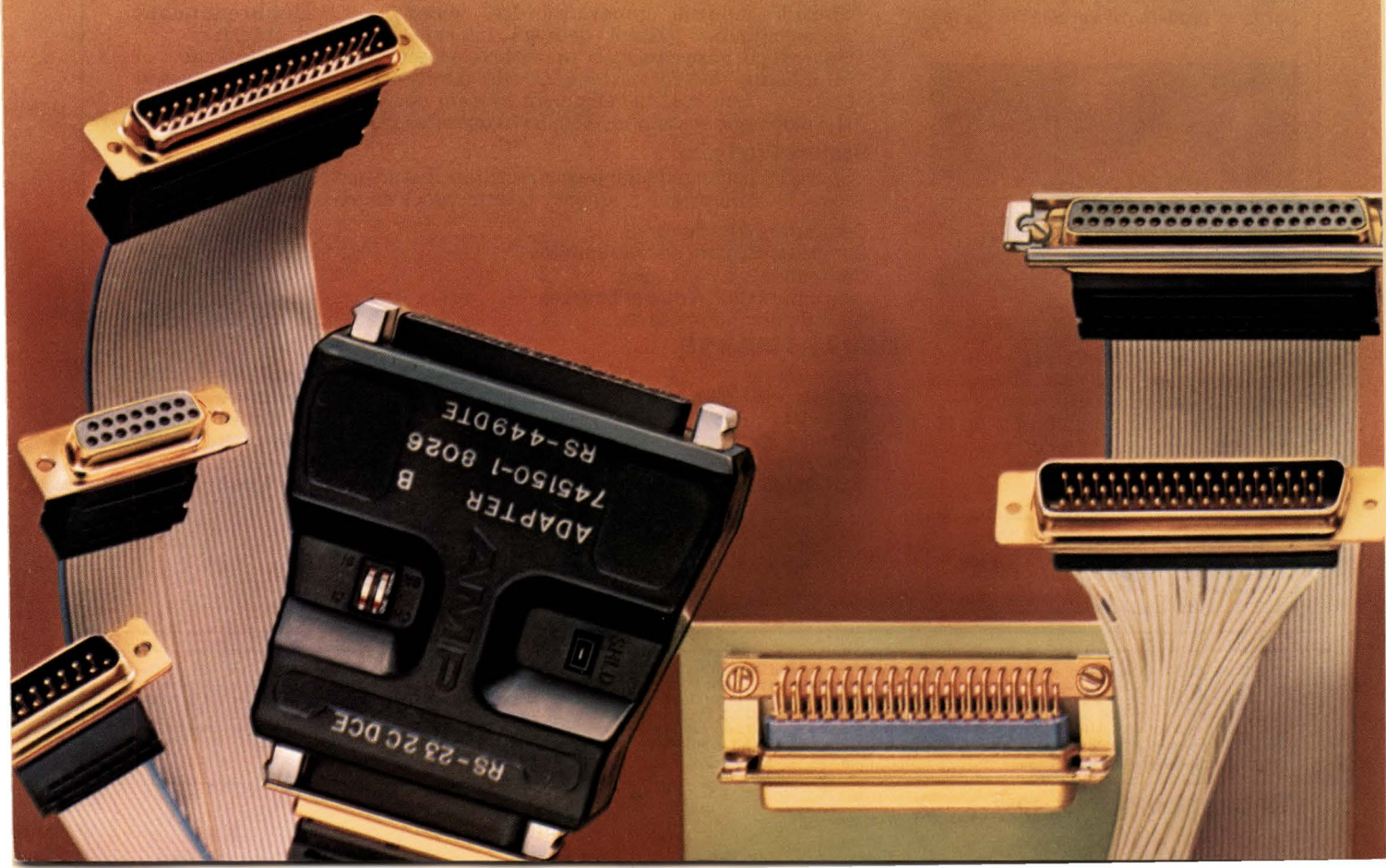


Save your systems from obsolescence. Bring them up to the standard with AMPLIMITE subminiature D adapters.

They interface RS 232 with the new RS 449 cable-to-cable or directly to your equipment. One way or the other, you save the cost of major redesign.

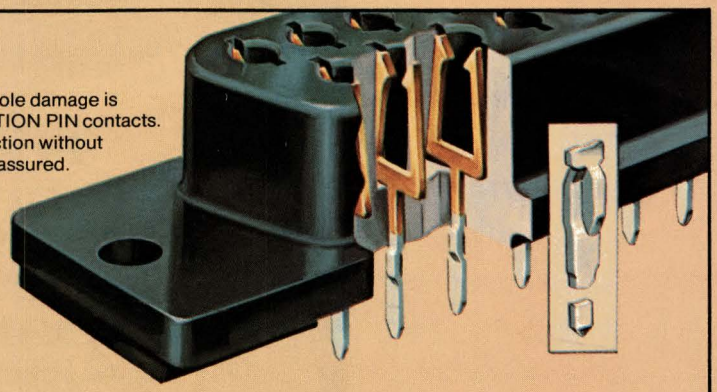
Our subminiature Ds also give you the widest choice. Metal shell and all-plastic connectors. Filtered assemblies. Mass termination styles. Standard, high density and MIL-C-24308 versions. And the most complete selection of accessories made.

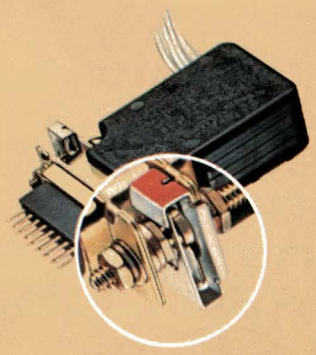
You bring a lot together with our AMPLIMITE connector system.



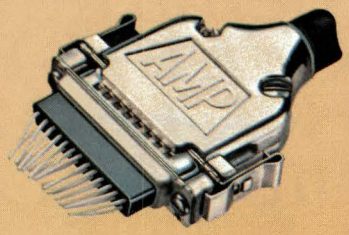
AMP Facts

Plated-through hole damage is avoided with ACTION PIN contacts. Gas-tight connection without soldering is also assured.

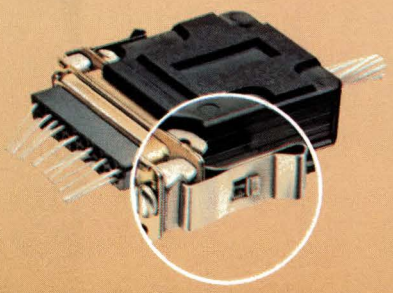




Two styles of slide latch clips simplify plug and receptacle mating.



Metal-shelled shielded connector provides EMI protection.



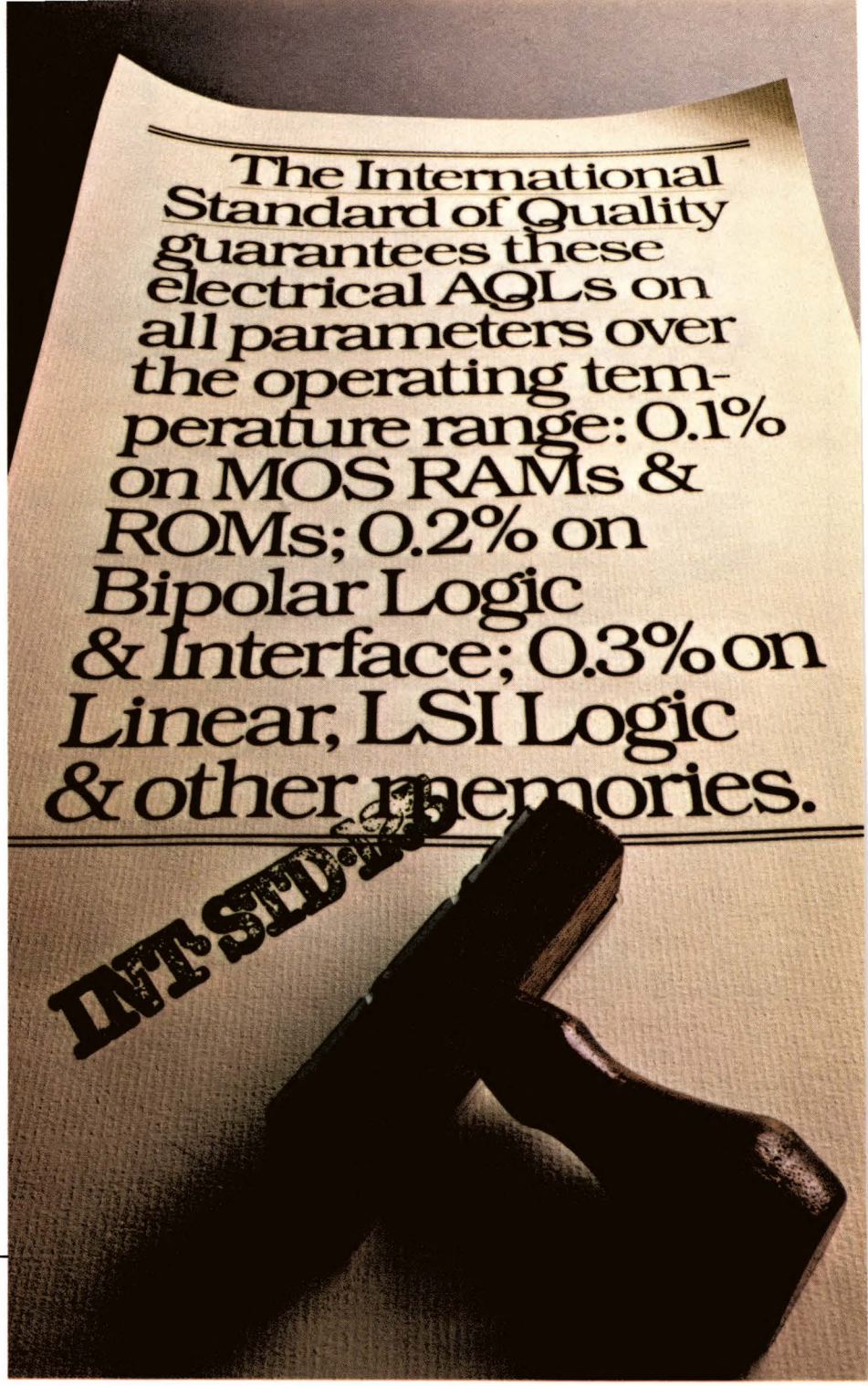
Spring latch assembly allows easy harness hook-up to RS 449 standards.

For more information, call the AMPLIMITE Connector Desk at (717) 780-8400.

AMP Incorporated, Harrisburg, PA 17105.

AMP means productivity.

CIRCLE NUMBER 253



If there's one thing this world doesn't need it's another rotten RAM. Another rejected ROM. One more paralyzed EPROM.

This is your chance to do something about it.

WE'RE ALREADY DOING OUR PARTS.

From now on, insist that all your MOS memories meet or exceed INT·STD·123, The International Standard of Quality. We do.

Fact is, nobody's MOS RAMS and ROMS come with a guaranteed AQL better than 0.1%. Not here. Not in Japan.

Technical by the

Knockouts Contender

We're The Contender – Hybrid Systems. And we're taking on the data conversion "heavyweights" with our technical strength and the most advanced, state-of-the-art production techniques in D/A and A/D conversion.

We know the other guys are tough. But they're vulnerable, too.

For example, who else but Hybrid Systems has a leak-proof commercial package that is patented? Nobody.

Our completely sealed package features a unique combination of materials that prevent any mismatch in thermal coefficient due to temperature extremes. Surface cracks, loose pins, and many other weaknesses typical of ordinary packages are eliminated. All components are arranged in an open cavity, away from messy epoxy, thereby knocking out mechanical strain, chemical degradation, and moisture problems.

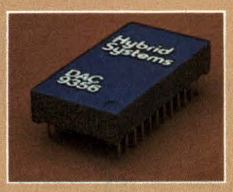
The result is data conversion products so reliable, they've moved up to a class of their own. In this new class, the powerful winning combination of price/performance is in the hands of no one else but Hybrid Systems. The Contender.

We mean it when we say we're the Contender. We know we're going to have to work even harder to get you into our corner. But once you see what we can do, you'll make going with Hybrid Systems a unanimous decision.

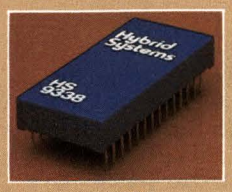
Call us today at (617) 667-8700, or write Hybrid Systems Corporation, 22 Linnell Circle, Suburban Industrial Park, Billerica, MA 01821.

The Contender Weighs In With Five Knockout Products

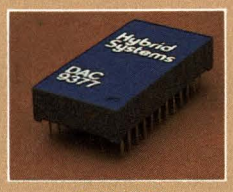
DAC 9331-16
The first D/A converters with 16-bit resolution and linearity using monolithic I/C technology. Puts everyone else with 2"x4" modules down and out for the count.



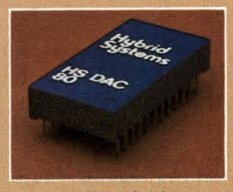
DAC 9356
DAC 80 compatible. Lowest cost, complete, low-power, 12-bit D/A converter available. The one to have in your corner when building systems that employ several DACs.



HS 9338
Complete, microprocessor-compatible, memory-mapped, 12-bit, double-buffered D/A converter. An all-around winner.



DAC 9377
Complete, buffered, voltage output D/A converter with 16-bit resolution and linearity. Flattens the competition's best price.



HS DAC 80
Low cost general purpose 12-bit D/A converter packaged in a 24-pin DIP. This one-two combination of price and performance has the "heavyweights" on the ropes.

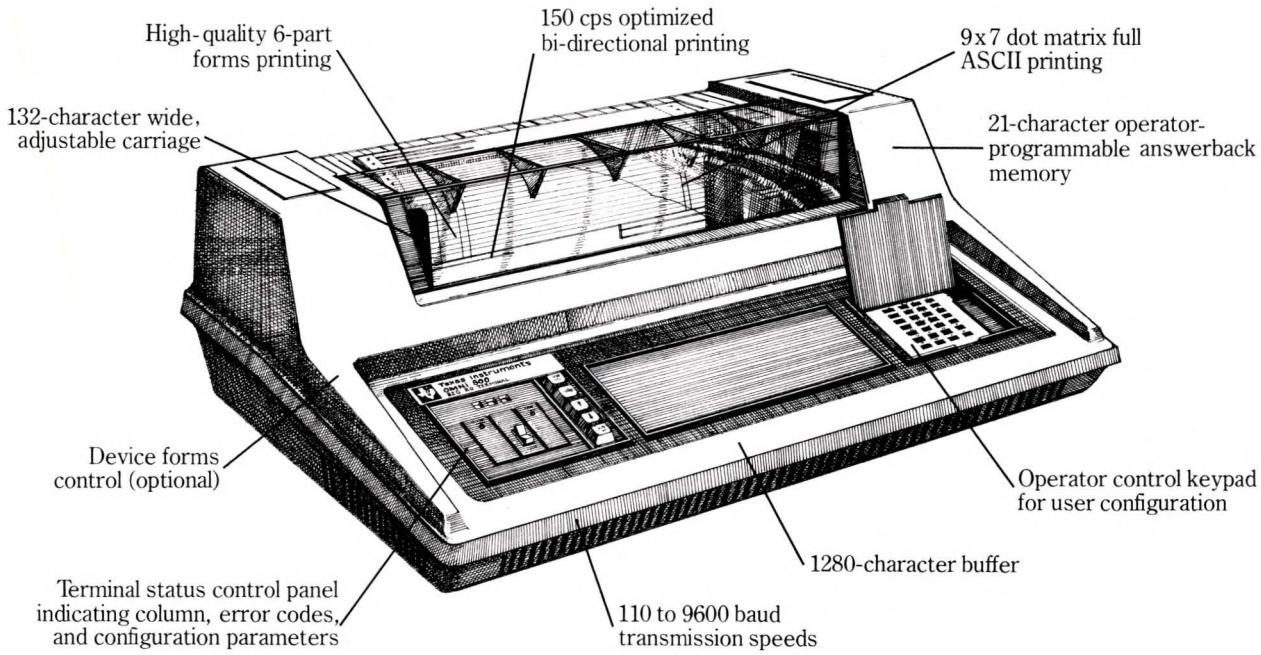
Hybrid Systems CORPORATION

CIRCLE NO 3

The Associate Producer.

IMMEDIATE DELIVERY

820 RO
Receive-Only Printer



The OMNI 800* Model 820 RO Printer has the same designed reliability as its associate, the 810 RO. With more standard features and options like expanded and compressed printing, the 820 RO offers greater flexibility for additional applications. And, should application needs change, the 820 RO is easily upgraded to a KSR model for a modest cost. The productive 820 RO Printer has all the quality and performance you associate with the OMNI 800 Family.

TI is dedicated to producing quality, innovative products like the Model 820 RO Printer. TI's hundreds of thousands of data terminals shipped worldwide are backed by the technology and reliability that come from 50 years of experience, and are supported by our worldwide organization of factory-trained sales and service representatives.

For more information on the 820 RO, contact the TI sales office nearest you, or write Texas Instruments Incorporated, P.O. Box 202145, Dallas, Texas 75220, or phone (713) 373-1050. In Canada, write Texas Instruments Incorporated, 41 Shelley Rd., Richmond Hill, Ontario L4C 5G4, or phone (416) 884-9181.

We put computing within everyone's reach.

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TEXAS INSTRUMENTS
INCORPORATED

CIRCLE NO 4

Edited by Joan Morrow

News Breaks

US SEMICONDUCTOR FIRM RECEIVES DOLBY LABS'S APPROVAL

Interdesign Inc (Sunnyvale, CA) has won the hotly contested race to be the first US semiconductor company to obtain Dolby Laboratories's approval for a single IC that meets the specs of the new Dolby C noise-reduction system. The company joins Hitachi as the only two IC suppliers currently approved by Dolby Labs.

The Dolby C noise-reduction system is based on a new dual-level processing scheme with two sliding-band processors operating in tandem at different levels to solve the problems of achieving 20 dB of compression and expansion without introducing side effects. Interdesign will use one of its Monochip bipolar linear component arrays to integrate the system. The device will be offered in a 24-pin DIP to Dolby licensees only. Full volume production is scheduled for November.—JM

68000 FAST FLOATING-POINT SOFTWARE AVAILABLE ON 8-IN. DISK

Offering single-precision (32-bit) software floating-point operations optimized for the MC68000 μP, the 68343 Fast Floating Point program comes on an 8-in. floppy disk in VersaDOS format. Simple to use and customize (the source code is included on the disk), it allows subroutine calls. While it's not based on IEEE floating-point format, conversion routines are available to output that format. Other conversion routines go back and forth from fixed to floating point, ASCII to floating point and BCD to floating point.

In addition to the standard arithmetic operations, the package performs Test, Compare, Absolute Value and Negate plus most of the transcendental functions. Execution time for an Add or Subtract is 22 μsec; Multiply, 44 μsec; Divide, 76 μsec; and Sinh, 623 μsec. These times are for the 8-MHz 68000; using the 10-MHz part drops them by 20%. Order the 86343 as M68KFFP from Motorola's Microsystems Group in Phoenix, AZ for less than $1000 with no limitation on use or redistribution (no royalties).—WT

OPERATING SYSTEM SUPPORTS PRINTERS, DISKS, 16 CONSOLES

The MP/M II operating system from Digital Research (Pacific Grove, CA) operates in systems employing an 8080, 8085 or Z80 μP. It requires 48k bytes of RAM, a clock/timer interrupt and at least one disk. The multiuser/multitasking software supports as many as 16 user consoles, printers and disk drives with storage capacity of 512M bytes each for a total on-line storage capacity of 8G bytes. It can also manage 400k bytes of system RAM, with banks being selected in blocks of 48k among eight users. Utilities include a relocatable macro assembler and a linking loader. MP/M II is compatible with CP/M files and supports the company's CP/Net networking operating system. Distributed on 8-in. single-density IBM-format diskettes, it costs $450.—CW

DESKTOP BUSINESS COMPUTER JUGGLES WORDS, NUMBERS, GRAPHS

Running under the CP/M operating system and offering a choice of five business application-software packages, the HP 125 single-user desktop computer system combines the features of a personal computer, word processor, visual display terminal, financial calculator and graphics workstation. From Hewlett Packard (Palo Alto, CA), Models 10 and 20 employ a CRT with a separate keyboard; a choice of a thermal, letter-quality or dot-matrix printers; a 1- or 8-pen plotter; and either 5¼- or 8-in. floppy-disk drives for storing 500k or 2.4M bytes of information, respectively. In addition to working as a stand-alone local processor, the HP 125 can also function as a remote station to an HP 3000-based network or a mainframe via dual RS-232C datacomm ports at speeds to 9600 baud. Prices start at $7460.—GK

News Breaks

INTERFACE PUTS STREAMER ON THE S-100 BUS

A nonintelligent interface from Scientific Enterprises Inc (Wilsonville, OR) gives your S-100 system tape-cartridge-backup protection. The S-100 Archítape interfaces any S-100 system to Archive Corp's 20M-byte streaming-tape cartridge drive, transferring data at either 2M bytes/min (the A version working with the 30-ips drive) or 6M bytes/min (the B version working with the 90-ips drive). Both versions provide read-while-write data verification and 16-bit CRC generation and checking. The A version costs approximately $500; the B version, $600 (less than 100 units).—ET

COLOR-GRAPHICS TERMINAL TO COST LESS THAN $1600

In the first quarter of next year, look for a color terminal costing approximately $1500. The Intelligent Systems Corp (Norcross, GA) terminal will support a 480 × 380 graphics matrix and several communication protocols and terminal emulations. The company says the terminal is being developed for high-volume OEMs.—CW

NONVOLATILE-MEMORY LINE EXPANDS UP AND DOWN IN SIZE

General Instrument Microelectronics (Hicksville, NY) is putting a variety of processes to work on various EAROM (EEPROM) products. The ER5816, a word-alterable, 2816-compatible, n-channel metal-gate MNOS part, has been sampling since March; the ER4201 (EDN, January 21, pg 40) is scheduled to start sampling this month. The 4201 is also fabricated in metal-gate n-channel MNOS, but the 128 × 8-bit unit also provides latches for both address and data and features a Reprogram command that combines an erase and write cycle. The word-alterable part also provides a Busy signal for μP compatibility; it accesses in 450 nsec. Production is scheduled for December, with pricing at $7 (1000).

The company's latest efforts deal with n-channel Si-gate MNOS. The first product announced using that technology is the ER5716—a 16k alternative to the 2716 EPROM. The 2k × 8 bulk-erasable part accesses in 300 nsec and serves as a second source to the HN48016.

Other things to look for: the AR5304, a 4k shadow RAM similar to parts made by Xicor, which will be available in the first quarter of 1982; and the ER1450, a 50 × 14-bit EAROM aimed at the TV-tuner industry. A spinoff from the ER1400, the new part will cost considerably less.—WT

SPEAKING OF VOICE I/O . . .

Now you can digitize your own vocabulary and make your computer system say what you want it to. A voice-development system from Centigram Corp (Sunnyvale, CA) provides this capability in a stand-alone unit. Intended for use by nonprogrammers, the real-time system is easy to use: Just speak the words into the microphone and the system digitizes them for instant use, storing the vocabulary on 500k-byte diskettes. The first version of the $25,000 system will work with Multibus systems and run under CP/M with deliveries beginning in October. The firm will also announce versions to provide a similar capability for other computer systems.—ET

ENHANCEMENTS EXTEND BUBBLE-MEMORY TESTER'S USEFULNESS

With programmable drivers that feature wider current ranges, Model Q-1012 bubble-memory test system tests a larger variety of bubble devices than earlier systems. From Megatest Corp (Santa Clara, CA), it offers parallel test capability to increase throughput: It can test two Intel 1M-bit devices or three ¼M- or 1M-bit Motorola devices at one time, using four output sense channels. Stimulus signals are applied simultaneously to the devices under test, but output error maps and bad-loop masking information are maintained individually.—AS

SIEMENS

Siemens... your reliable 8086 source

Now, a second source for the most widely used 16 bit microprocessor. The SAB 8086 family is available in quantity with the reliability and quality you expect from Siemens. It's available now in a 40 pin ceramic package with operating frequencies of 4, 5, and 8 MHz and soon with 10 and 12 MHz versions...all utilizing Siemens new VLSI processing techniques.

The SAB 8086 is the latest addition to the wide spectrum of semiconductor products offered by Siemens. So, if you have been searching for a reliable source for this widely used 16 bit microprocessor, count on Siemens for performance and price.

Obtain additional SAB 8086 information simply by contacting: Siemens Components Group, 186 Wood Avenue South, Iselin, New Jersey 08830, (201) 494-1000, Extension 2222.

For a free copy of our new, comprehensive SAB 8086 data sheet, just fill out and return the coupon below.

CIRCLE NO 5

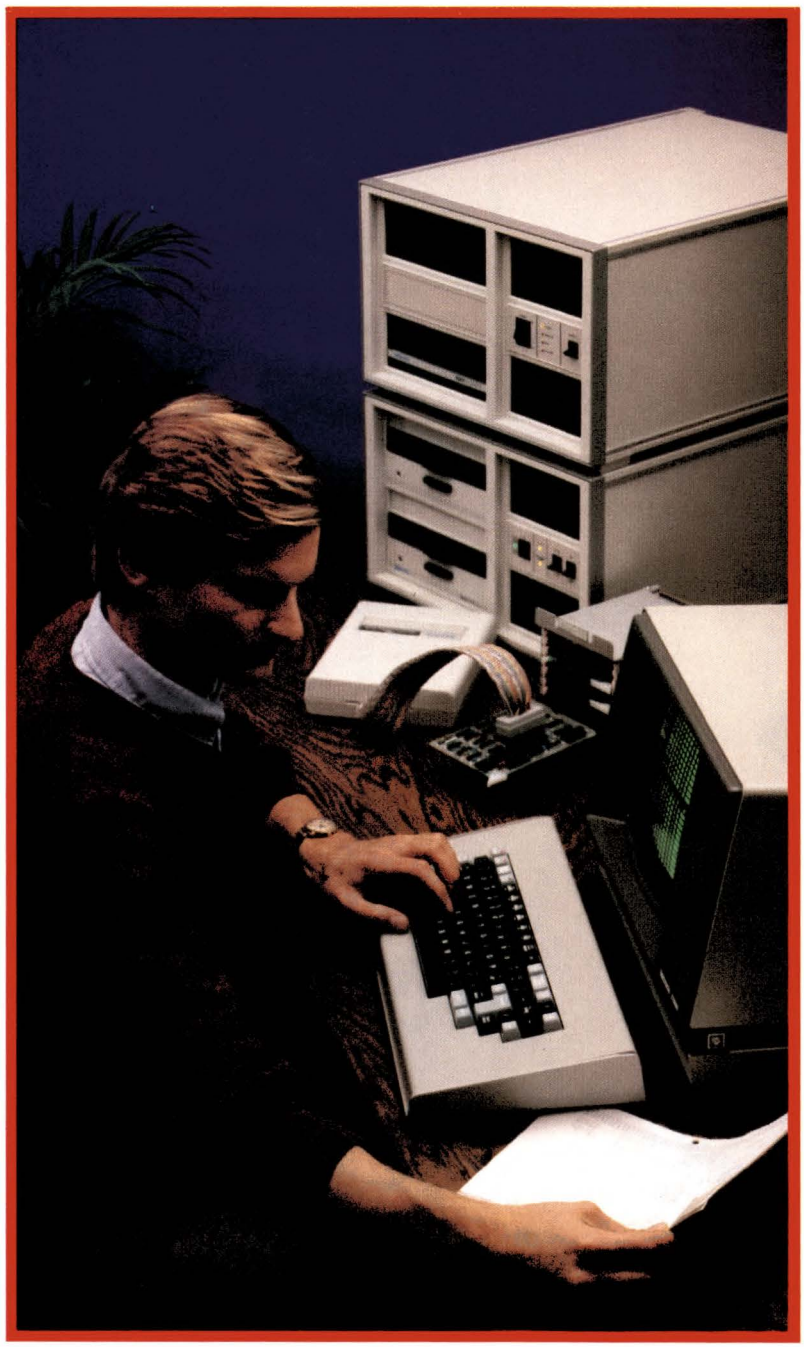
Specify Siemens and be secure.

Siemens Corporation, Box 1000, Iselin, NJ 08830 CG/2000-030 SIQ827

Please send SAB 8086 information.

Name _____ Firm _____ Address _____ City _____ State _____ Zip _____

16 bits of information



1. Self-contained and upward compatible. The 8550 Microcomputer Development Lab is the single-user member of the new 8500 Modular MDL Series, which also includes the 8560 multi-user system and the 8540 Advanced Integration Unit for the host computer environment. The 8550 is a complete microcomputer design tool, covering both software development and integration into the prototype. The 8550 can also be used as a station on Tek's forthcoming 8560 multi-user system.

2. Real-Time Emulation. Takes the concept of emulation to a new performance level. Advanced circuitry eliminates the need for wait states during program execution and debugging. The emulator processor now functions in real-time, with its operation totally transparent to the user.

3. Multi-Vendor Chip Support. The 8550 MDL supports 26 chips in all. The broadest support available anywhere, covering a wide range of vendors. With microcomputers as well as microprocessors. The ultimate in design flexibility.

on the new 8550 MDL.

4. 16-bit Support. You'll be able to choose from an entire new generation of 16-bit processors. Tektronix has the high performance tools to make it possible. Assembler support is available now for the 16-bit chips listed below. The TMS 9900 and SBP 9900 are fully supported with emulation today. Real-Time Emulation and Pascal support will be available in stages for the 68000, Z8000 and 8086.

68000 **TMS 9900**
Z8000 **SBP 9900**
8086

5. 16-bit Trigger Trace Analysis. Gives you highly sophisticated triggering ability for selective snapshots of full-speed code execution on the prototype bus. Up to four data acquisition triggers can be combined in a wide variety of ways. Bus cycle resolution to 8 MHz.

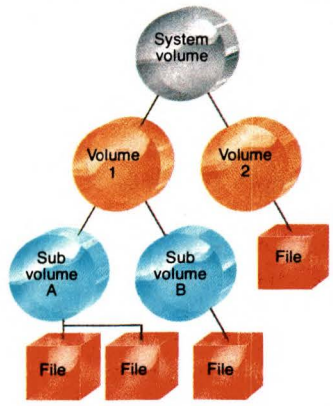
6. 8-bit Support. Besides the most up-to-date microprocessor coverage, you can also take advantage of extensive 8-bit microcomputer support. All 8-bit chip support includes real-time emulation.

6800	**8048**	**3870**
6802	**8039**	**3872**
6808	**8039-6**	**3874**
Z80A	**8035**	**3876**
8080A	**8021**	**F8**
8085A	**8022**	**1802**
8049	**8041A**	**6500/1**

7. 8-bit Real-Time Analysis. An optional Real-Time Prototype Analyzer lets you extract both bus and hardware logic at full operating speeds. You capture 48-bit words for storage in a 128-word memory. Two triggers for precise data acquisition.

8. Split-Bus Architecture. The 8550 uses one processor and bus for system operation, and another for real-time emulation. This architecture assures that the emulator processor is denied access to system memory, preventing the possibility of a system crash during prototype program execution.

9. Tree-Like File Structure. Combines ease of use, rapid access and in-depth organization. Allows files to be arranged in a predetermined hierarchy that best supports your current situation. A flexible tool that supports filing situations from very simple to extremely complex.



10. Advanced CRT-Oriented Editor. Gives you the quickest path possible to perform many editing operations. Lets you use screen-oriented editing as well as line-oriented editing. Up and down scrolling capabilities give you a total window on all of your code.

11. Macro Assembly. The most powerful assembler software available today in a development system. Lets you employ user-defined constructs and library resources. A conditional assembly feature allows sophisticated user manipulation of code at assembly time.

12. Pascal Compiler. Available in true compiler form, producing executable object code. Pascal's structured format allows a modular approach to programming. With extensions designed specifically for microcomputer development, Tektronix Pascal is ideal for the "top-down" method of product development.

13. MDL/μ Compiler. Tektronix' advanced form of Basic, with many extensions for microcomputer development. Often the quickest route from concept to fully developed code.

14. Transportable Emulators and Software. If you need to expand to a multi-user design environment, your 8550 can be incorporated as a workstation in an 8560 multi-user system. Source code and emulator modules can be readily transferred to the Tektronix 8560 system. If you move to a host environment, your 8550 emulator modules are totally compatible with the new Tektronix 8540 Advanced Integration Unit.

15. Worldwide Service. For service support, 36 centers around the globe. You get fast on-site service no matter where you are — without waiting weeks for parts or repairs.

16. Full Tektronix Support. Training, documentation, applications engineering. Nobody does it like Tektronix. An entire series of classes on microcomputer design, from high-level language to hardware/software integration. Applications engineers are available worldwide to assist you.

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Signals & Noise

Does engineering benefit from competition?

Dear Editor:

EDN's June 24 editorial has three disagreements with Mr Feerst's objections to the publicly funded advertising of the University of Massachusetts. They don't survive scrutiny.

One, the "low unemployment rate" argument, merely reflects an artificially depressed and unrewarding salary structure for engineering compared with other less contributory (and less expensive to enter) professions. Attempts to dilute the profession with promises of cheap engineering by "starving graduate students" both depress salaries further and increase the cost of entry into the profession. It's difficult to find an advantage to the nation in such an approach. More encouragement is needed; not "starvation."

Your second disagreement might be only slightly less unsupportable. Interplay between academia and industry is certainly desirable, but not the undercutting kind that is the obvious aim of U Mass.

To use the limited resources of our poorly equipped grad schools as a "cure" for the "outrageously wasteful" practice of industrial training and learning is really farcical. Virtually every other segment of the industrial world uses training in the work area, where problems can be recognized and resolved with far better focus and speed than in the classroom or isolated laboratory. The experience of US industries today shows that more training is needed in the work area, not less.

Your third objection seems irrelevant. Mr Feerst's comments relate to engineering work normally performed by

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In addition, the CF6V5.5 (also available in 12V5.5) is just one of over 40 Carefree® batteries. They're the maintenance-free rechargeables that fit more space and power requirements than any other batteries in the world . . . from the 6V½AH to the 6V50AH.

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20	Hour Rate (.28 ampere to 5.25 volts)	5.5 ampere hours
10	Hour Rate (.53 ampere to 5.10 volts)	5.3 ampere hours
5	Hour Rate (.96 ampere to 4.95 volts)	4.8 ampere hours
1½	Hour Rate (2.80 ampere to 5.25 volts)	4.2 ampere hours
1	Hour Rate (3.50 ampere to 4.50 volts)	3.5 ampere hours

Physical Size (± .05 inches):

Length	6.00 inches
Width	1.34 inches
Height	3.70 inches
Height (including terminals)	3.90 inches
Volume (excluding terminals)	29.7 cubic inches
Weight	2.7 pounds

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industrial staffs (who recommend and authorize the purchase of products advertised by your publication) and consultants (some of whom are from academia)—the very work solicited by the U Mass brochure. That is not the kind of research, contributed by Bardeen, Shockley and others, that affects the eventual mainstream of the industrial world. Those and many other contributions also deserve great reward. Their sources should not have to rely on "starving graduate students" as a resource.

On this matter, I think Mr Feerst is right. The public trough is a poor place from which to launch a competitive drive. Congratulations on your otherwise fine publication.

Loren L Krueger, PE
Minnetonka, MN

Amend those bus specs

EDN's recent Designer's Guide to μC buses (May 24, June 10 and June 24) mistakenly listed the Multibus (P796) as a 32-bit-wide bus. The Multibus can accommodate 32-bit-wide transfers via multiplexing, however, and incorporates refinements that make it an obvious step toward more powerful and wider word μPs.

Further, buses such as Fastbus and P896 represent a new category of bus design. Both are designed for maximum implementation ease and thus don't restrict designers by imposing stringent specifications that must be followed in all cases.

Note that some of the specifications for these two buses presented in the Designer's Guide were also in error (**table**). To clarify the **table** entries, note that the P896 bus only specifies an interconnection

If you have to choose, don't.

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Specify Mostek 64K ROMs instead.

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Quality: Outgoing AQL for the MK36000 and MK37000 is .25%.

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Selection: Our 24-pin MK36000 is the accepted standard. And our 28-pin MK37000 is part of the JEDEC-approved Mostek family of compatible x 8 BYTEWYDE* memories.

Packaging: Our 64K ROMs are available in plastic, cerdip, ceramic and leadless chip carrier (LCC) packages; in commercial and military grades (883-B).

Price: As competitive as you can get. Check for yourself.

If all of this still hasn't convinced you to consider our 64K ROMs, make it a point to call your Mostek sales office listed on the next page. Or write Mostek, 1215 West Crosby Road, Carrollton, Texas 75006. Attn: John Landau, M.S. 714. (214) 323-6222. In Europe, contact Mostek International at (32)2.762.18.80. In the Far East, Mostek Japan KK (03)-404-7261.

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BUS FEATURES	FASTBUS	P896
NUMBER OF LINES SPECIFIED/AVAILABLE	130/58(1)	64/64(3)
DATA-FIELD WIDTH	32M	32
TRANSMISSION MECHANISM (PM = PARTIALLY MULTIPLEXED, FP = FULLY PARALLEL)	PM	FP
SYSTEM GEOMETRY (PC = ONE PCB, OC = ONE CRATE, SC = SEVERAL CRATES)	SC	OC
UNIFIED ACCESS TO MEMORY AND I/O?	Y	Y
MULTIPROCESSOR CAPABILITY?	Y	Y
REDUNDANT TRANSMISSION PATHS SPECIFIED?	Y	Y(4)
ADDRESS LINES WIDTH (M = MULTIPLEXED)	32, M	32, M
DATA LINES WIDTH (M = MULTIPLEXED)	M	32, M
CONTROL LINES	—	4
TIMING LINES	—	6
LINES OTHERWISE SPECIFIED	—	8(5)
RESERVED LINES	19	N
FREE-USE LINES	0	N
POWER LINES (M = MULTIPLE)	M	4 + 5
DATA-LINE USE (U = UNIDIRECTIONAL, B = BIDIRECTIONAL)	B	B
ADDRESS EXPANSION POSSIBLE?	Y	N
MAXIMUM EXPANDED ADDRESS FIELD	—	32
MAXIMUM NUMBER OF DEVICES BY ELECTRICAL DRIVE CAPABILITY	≤32	32
MAXIMUM NUMBER OF DEVICES BY DEVICE ADDRESSING CAPABILITY	2^{31}(2)	2^{32}
BUS-ACCESS MANAGEMENT—CENTRALIZED?	—	N
—DAISY CHAIN?	—	N
—PARALLEL POLLING?	—	Y
—SERIAL POLLING?	—	N
—DIRECT LINES?	—	N
—OTHER?	—	—
PROGRAM-INTERRUPT MANAGEMENT—CENTRALIZED?	—	N
—DAISY CHAIN?	—	N
—PARALLEL POLLING?	—	Y
—SERIAL POLLING?	—	Y
—DIRECT LINES?	—	N
—OTHER METHODS?	—	N
MAXIMUM TIMES FOR SINGLE REQUEST—BUS-ACCESS DETECTION (AS = ASYNC)	—	AS
—PROGRAM INTERRUPT DETECTION	—	VAR
—PROGRAM INTERRUPT LATENCY	—	VAR
—PROGRAM INTERRUPT PROCESSING	—	VAR
DATA-TRANSFER TYPE—SYNCHRONOUS (FIXED TIMING)?	Y	N
—ASYNCHRONOUS?	Y	Y
—SYNCHRONOUS (HANDSHAKE)?	Y	—
SINGLE OPERATIONS ONLY?	N	N
MULTIPLE UNINTERRUPTIBLE OPERATIONS?(6)	Y	Y
MULTIPLE INTERRUPTIBLE OPERATIONS?	Y	Y
MULTIPLE-SOURCE READ?	Y	N
MULTIPLE-DESTINATION WRITE?	N	Y
DISTINCTION BETWEEN BYTE/WORD TRANSFER?	N	Y
SPECIAL LINES—HOLD?	Y	N
—WAIT?	Y	N
—INITIALIZE-RESET?	Y	N
—POWER FAIL/WARNING?	Y	N
—INTERRUPT REQUEST?	Y	N
—INTERRUPT ACKNOWLEDGE?	Y	N
—OTHERS?	—	N
LINES FOR HANDLING ERRORS—TRANSMISSION ERRORS?	Y	4
—OPERATIONAL (USER ERRORS)?	—	4

NOTES:
(1) HAS 130 LINES ON BACKPLANE AND 58 ON CABLE BUS.
(2) ≤32 DEVICES PER SEGMENT.
(3) HAS TWO LEVELS. LEVEL-1 LINES (CURRENTLY BEING DEVELOPED) ARE 64 SPECIFIED/64 AVAILABLE AND LEVEL-2 LINES (STILL NEEDING REFINEMENT) ARE 96 SPECIFIED/96 AVAILABLE.
(4) NO PROVISION EXISTS WITH THE 64-PIN ARRANGEMENT FOR REDUNDANT PATCHS WITHOUT AN EXTRA CONNECTOR. THIS IMPLEMENTATION PROBLEM IS LEFT TO DESIGNERS.
(5) BUS ARBITRATION.
(6) INDIVISIBLE —CURRENT BUS OPERATION WILL RUN TO COMPLETION.

medium and protocol with minimal emphasis on implementation. Most of the attributes listed in the **table** are left up to the system designer's choice. Items such as timing requests are implementation dependent, and special line functions are part of the interrupt structure.

Additionally, the Fastbus high-speed data bus (less than 100-nsec word transfer on a short segment), suits multicrate, multiprocessor applications that require a system-wide (over several crates) addressing

Signals & Noise

capability. Consequently, the bus definitions don't lend themselves to comparison with less capable buses (hence the lack of specs in the **table** for bus-access management and detection and program-interrupt management). You can obtain additional information on the Fastbus from R S Larsen, chairman, Fast System Design Group, Stanford Linear Accelerator Center, Box 4349, Stanford, CA 94305.

Benchmark update updated

Dear Editor:

In the box in EDN's Benchmark Update (see pg 169 in this issue), the execution times shown for the MC68000L12 are correct for a clock frequency of 12.0 MHz. However, the specified minimum clock-cycle period for the MC68000L12 is 80 nsec, which yields a maximum clock frequency of 12.5 MHz.

This clock frequency produces an approximately 4.0% execution-time reduction on the benchmarks as shown below:

Benchmark	Execution time (μsec)
A	25.6
B	257.3
E	180
F	55.7
H	96.8
I	13,878
K	293

Motorola's branding procedures do not allow fractions (½ would be too small to be read) or decimal points (also too small) in the branded part number.

Sincerely,
James J Farrell III
Manager, Technical Communications
Motorola MOS Integrated Circuits Group
Austin, TX

4 STAND-ALONE ICE

Stand-alone ICE is a new class of instrument, created by Millennium, for use in development labs to debug μP-based systems. Traditionally, microprocessor development systems were used for all development functions: code entry and edit, assembly, compilation, linkage of relocatable modules, and debug. And, the same system was used to debug hardware.

By distributing both the hardware and software debug functions into a separate instrument, development becomes "unbundled." The software development system can perform its classic functions (code entry, edit, assemble/compile), and the separate stand-alone ICE station debugs hardware or software simultaneously. The result is two users employing one "single-user" development system for two separate tasks at the same time.

This approach of unbundling debug and software development stations provides modules that may be configured to support the development task at hand. The ratio of software development stations to software/hardware debug stations may be varied to properly support the number of engineers and programmers on a project.

Development labs which use minicomputers for software development can also benefit from the unbundled approach. Stand-alone ICE debug stations can work with minicomputers as readily as with microprocessor development systems. Software can be generated using editors and cross-assemblers on the minicomputer, and downloaded to the ICE station via an RS232 port. The ICE station can be used as either a code execution vehicle, or as a hardware/software debug station. The minicomputer thus becomes a multi-user development system.

In-circuit emulation just came unbundled.

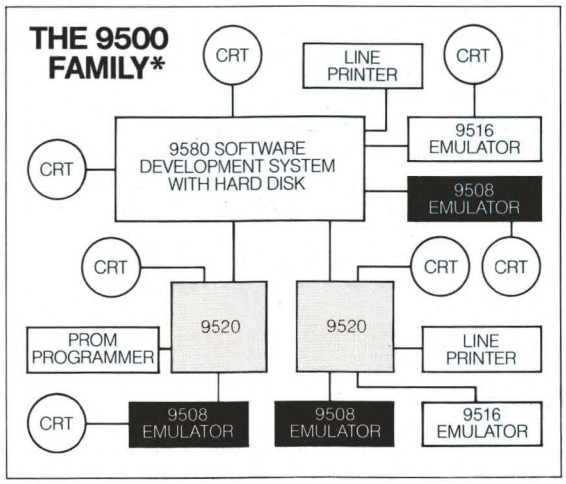
Do-it-yourself ICE.™ Start small. Think big. With the Millennium 9508 MicroSystem Emulator and a CRT, you can add a total hardware/software development and integration station to your mini or dedicated development system. Using a single RS-232 port. Or, double your equipment's productivity by using the 9508 stand-alone as a debug instrument.

Real time emulation. With speeds up to 11MHz. So, choose your μP or μC. The 9508 provides full speed emulation for the Z80A, 8085A, 6801, 6803, 6809, 8048, 8049, 8041, 8021 and 8035. With more on the way. But you don't have to buy them all. You simply buy the emulator boards you need. As you need them.

Complete cross-software. If we emulate it, we support it with complete cross macroassemblers. Simple as that. Emulation and cross-software from a single source. Debugged by Millennium.

Mappable memory. The 9508 has up to 16K of high speed memory, mappable on 1K boundaries. Program changes can be made with a line by line assembler. Thus, full memory, register and I/O can be examined and modified, quickly. And, emulation memory can be mapped anywhere in the target μP's address space. So, you can develop a system without a complete hardware prototype. In fact, software debug can begin without hardware.

Real time trace. Capture 128 events in the trace buffer. In real time. Then, display in disassembled form for quick debugging. The 9508 lets you qualify the entered events ten different ways dramatically improving the "Trace Debug Window" into your target system.



Choose your mode. External or internal emulation. Real time emulation step-by-step. Hardware development, software development or hardware/software integration. The 9508 was designed to help you analyze and correct system problems. Efficiently.

Easy to work with. Start with a straightforward command set. Just 25 commands, all of which are functionally relevant. With the command set, you can examine or change any memory location or processor register. Other special commands can help you fill or relocate large portions of memory. And four available hardware and software breakpoints speed your system design.

Systems your way. The 9508 stand-alone emulator is just the first step on the road to a multi-user, multi-tasking microprocessor development system (see diagram above). With a price/performance ratio that is melting the competition's ICE. But what else would you expect from the people who invented unbundled in-circuit emulation.

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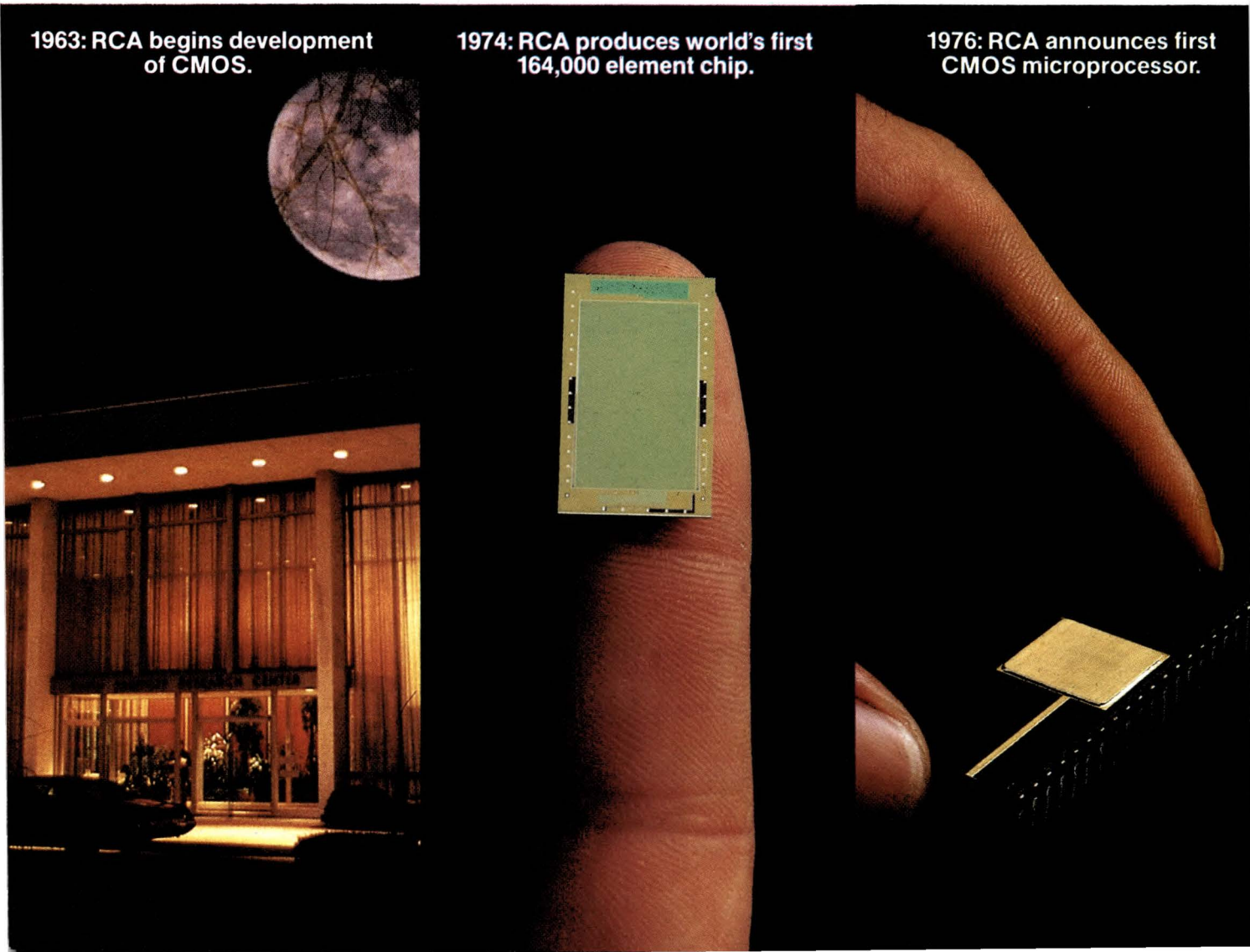
RCA has more than its share of innovations. But we've always put product reliability first.



As you can see, we've been innovators for years.

But ask people what they think of when they think of RCA, and they'll probably start talking about a company that's been around a long time (we started in 1919). They'll talk about a big, stable company that's been in the electronics industry from the very beginning. And they'll talk about the quality and reliability that they've come to expect from "Old Reliable."

What "Old Reliable" means.

To our customers, "Old Reliable" means quality and reliability in the products they buy from RCA.

Our goal is to produce components that perform to specification in your products. And continue to perform, day after day, month after month, year after year.

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We invented CMOS. We delivered the world's first CMOS logic parts as early as 1966. And today we offer you a full line of CMOS devices.

Last year, for example, we shipped more than one million CMOS microprocessors. Nobody else even came close. In addition, we shipped more than 175 million CMOS logic ICs.

In addition to commercial devices, we also supply a full line of High-Reliability parts. (In April 1981, RCA became the only supplier to qualify for Class S, Part 1 certification for CMOS radiation-hardened devices.)

Pioneers in BiMOS.

In 1976, we introduced BiMOS technology. Since then its parametric and performance advantages have set new standards in op amp technology.

Preparing for the future.

To make sure that we maintain the highest standards of quality and reliability, RCA Solid State is stepping up its investments in new equipment and personnel. Further, the RCA Princeton Laboratories plus our Solid State Technology Center provide some of the most advanced R&D capabilities in the industry.

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And of course, we'll keep those innovations coming, too. What else would you expect from the people who brought you CMOS, BiMOS and television?

RCA

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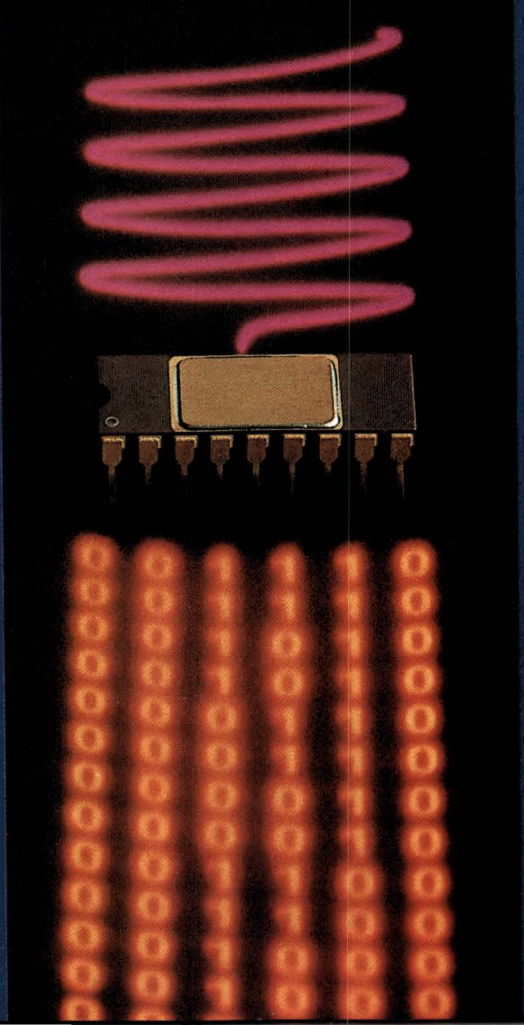
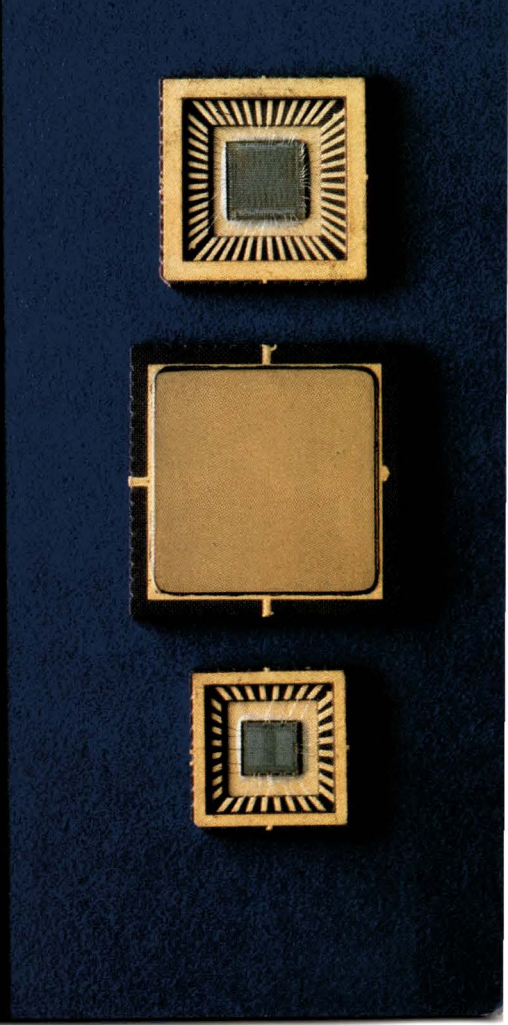
1976: RCA pioneers the first BiMOS op amp.

1980: RCA produces first CMOS 6-bit flash A/D converter.



1981: RCA announces expandable CMOS microprocessor chip set.



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Powerful, high performance architecture. That's the Synertek Z8,* the most powerful 8-bit single-chip microcomputer available today.

The Z8 gives you fast execution. Advanced architecture. Efficient use of memory. Sophisticated interrupt. Serial and parallel I/O. Programmable timer/counters. Plus easy system expansion. And you can tailor it the way you want it.

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- High Speed Instruction Execution – 8MHz Clock
- On-Chip Clock Oscillator
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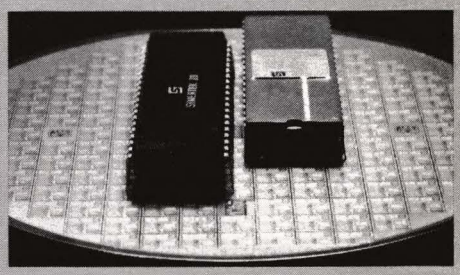
- Single +5V Supply



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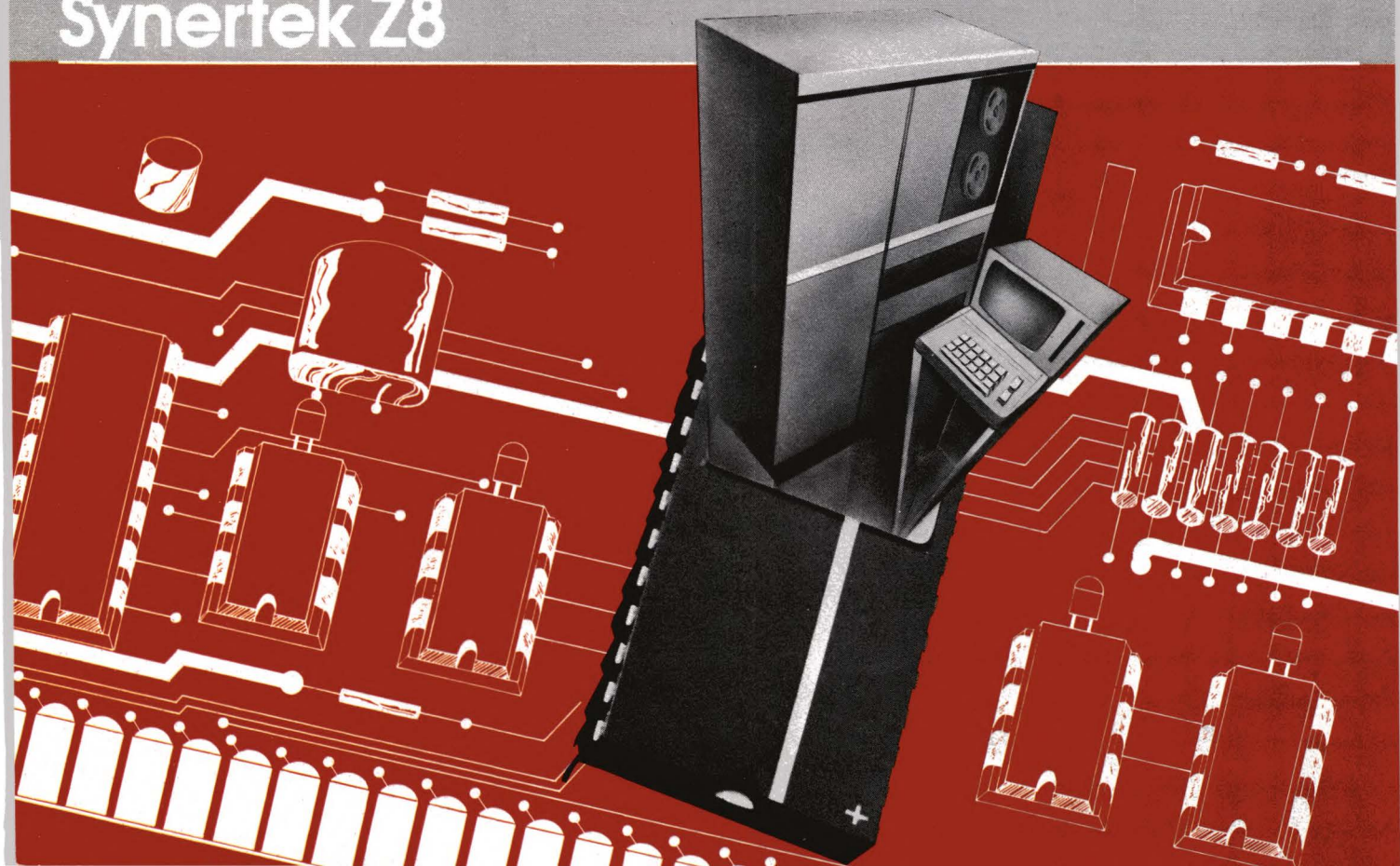

Editorial

Is there no limit to IEEE's arrogance?

Because of IEEE's apparent unwillingness over the years to represent the best interests of the bulk of its membership—working engineers—many of its members have dropped their affiliation. Additionally, many other engineers have refused to join at all. However, "unwillingness" (translate to "unresponsiveness") might be too kind in describing the Board of Directors's latest move. "Arrogant" is closer to the mark.

Once again, without consulting IEEE's membership, the Board has taken an action that appears to be self serving and ill advised. In the name of IEEE, it has filed a brief with the US Supreme Court supporting the contention of ASME (the American Society of Mechanical Engineers) that engineering societies should be exempt from the Sherman Anti-Trust Act.

ASME's appeal to the Supreme Court stems from a lower court's ruling that ASME members conspired with a manufacturer of boiler safety equipment when they met with that manufacturer and then issued a statement on ASME letterhead implying that another manufacturer's safety device did not meet ASME's boiler-code regulations. In reality, the device did meet the regulations. The second company claimed that this letter affected sales, forcing it to go out of business. The court agreed and awarded the firm $9.9 million in the resulting suit against ASME.

The basis for ASME's appeal and IEEE's brief is that the society's committees consist of volunteers who should not be held accountable for their actions in the name of ASME. IEEE contends, "Indeed, a rule of strict liability may herald the curtailment of beneficial professional society programs in any case where organizational procedures theoretically may be abused by volunteer members for individual commercial advantage. In a large society such as IEEE, a significant number of such programs may be jeopardized, in spite of the existence of reasonable, workable procedural controls, because of the impossibility of policing all society members' conduct."

EDN believes that this position is a foul-smelling smokescreen. The fact that committee members are volunteers should have no bearing on their accountability. They can do the same amount of harm (or good) whether they're paid or not. And if a society accepts the responsibility of setting industry standards and/or regulations, it must be willing to be held accountable for its actions and the actions of the members it appoints to key committees.

IEEE's Board consists of company executives and academics. It has rarely been accused of taking stands that benefit the membership when such stands conflict with its members' interests. The Board's actions have remained true to form in this case.

EDN urges IEEE to withdraw its brief. The engineering profession will never attain the respect and stature it strives for if it refuses to be held responsible and accountable for its actions.

Roy W. Forsberg

Roy Forsberg
Editorial Director

An Award*-Winning Magazine
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1978 Contributed Series—
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(**lĭk'ə tē brĭnd'l** *org. OE liccian, ME brende: a twinkling of the eye.*
1) a real trouper who's everywhere at once. 2) mercurially expeditious courier.
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HP	8413A	Phase Gain Indicator
HP	8445B	Tracking Preselector
Invertron	800T-40/5k-1	Power Supply Plug-in
HP	1615A	Logic Analyzer
HP	182T	Oscilloscope Mainframe, Non-Storage
TEK	8002A	Microprocessor Development System
HP	3964A	Instrumentation Tape Recorder
Dranetz	616A	DC/AC Voltage Disturbance Analyzer
TEK	922	Laboratory Non-Storage Oscilloscope 15 MHz
HP	6269B	DC Laboratory Power Supply
TEK	7A18	Amplifier for 7000 Series Mainframe
Brush/Gould	13-4615-00	DC Amplifier
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Staff

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Panasonic high resolution color display tubes provide color photograph-quality pictures with twice the resolution of our conventional tubes.

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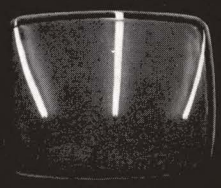

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CIRCLE NO 20

Technology Update

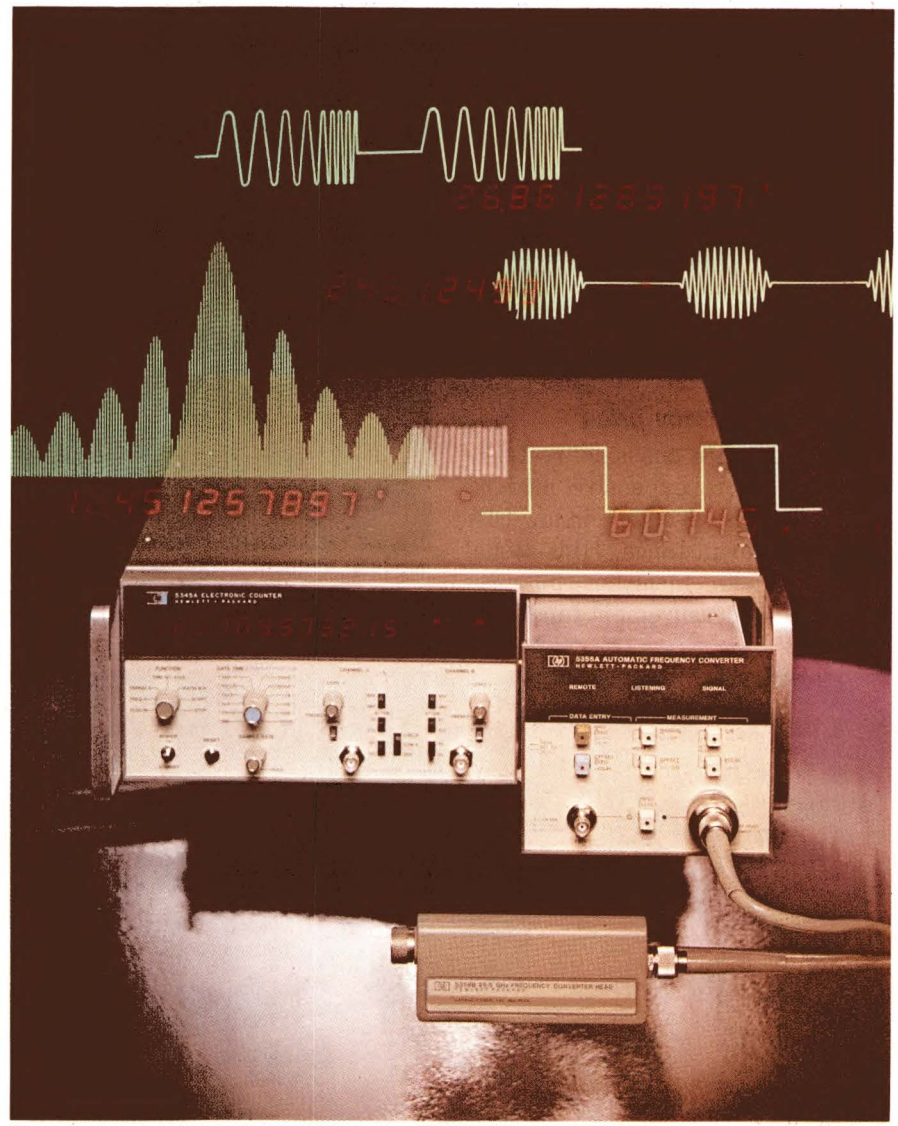
Frequency counters offer wide selection in form, function and price

Andy Santoni, Western Editor

Instrument vendors now supply a wide variety of frequency counters to meet virtually any frequency-measurement need. Monolithic counters range from low-cost instruments—some with IEEE-488 interfaces—to microwave units that reach 110 GHz. Plug-in counters provide flexibility, either as counter mainframes with plug-ins for different functions or frequencies or as general-purpose instrument mainframes that accept a variety of counter modules. And you'll also find counters in multifunction instruments or logic analyzer/counters.

When shopping for any of these instrument types, you'll encounter a multitude of suppliers offering many counter variations, notes Michael Nelson, marketing product analyst at instrument renter Leasametric Inc. There's probably one to meet virtually any need. And a handful of general-purpose models would probably cover almost every requirement. For instance, three counters—a 1-GHz battery-operated portable, a 1-GHz universal counter/timer and a microwave counter—could probably satisfy 95% of all user needs.

When renting a unit for a few days, you can afford to pay for such extra capability. But when buying in OEM quantities, the price differential between a general-purpose instrument and one more closely matching your requirements becomes significant. Then, you'll do best by reviewing the wide variety of models available and selecting the one best matched to your needs.



Counters and universal counter/timers *offer a wide range of performance and features. At the high end, Hewlett-Packard's $5200 Model 5345A covers dc to 500 MHz; plug-ins widen its coverage to 40 GHz. Single-shot time-interval measurements to 2 nsec and an optional IEEE-488 interface are also available.*

Counters cover more

Today you can select one versatile unit that handles a wide range of applications. Hewlett-Packard's Model 5335A ($2950), for example, covers dc to 200 MHz and with the optional C channel ($450) reaches 1.3 GHz. Yet its standard features, such as a GPIB interface, make it cost competitive with the older HP Model 5328A ($1450), notes Susan Davis, purchasing manager at United States Instrument Rentals. Thus, to provide performance roughly equivalent to that of the 1.3-GHz 5335A, the plug-in Model 5328A needs a bus-interface module ($350), 1.3-GHz C channel ($650) and programmable input-control module ($950)—and the 5335A still provides better single-shot time-interval averaging performance (2 vs 10 nsec) as well as built-in math and statistics capabilities.

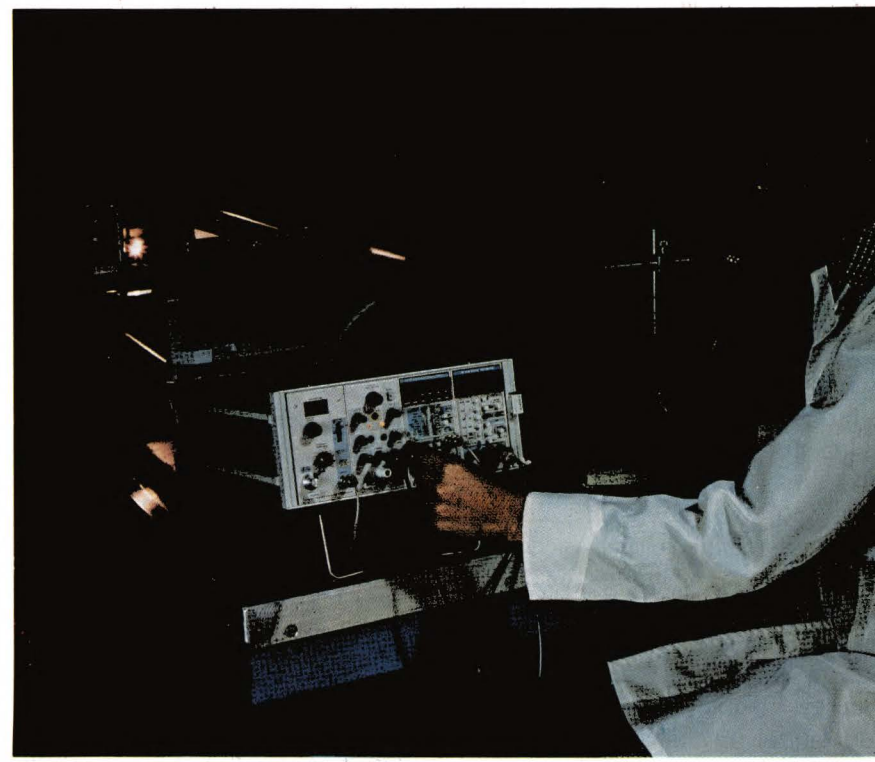
With its improved performance, Model 5335A illustrates the evolu-

tionary refinement of today's frequency-counter designs, says Leasametric's Nelson, as opposed to quantum leaps in performance. Suppliers have been "chipping away at problems," agrees Richard Watts, product marketing manager at Hewlett-Packard's Santa Clara, CA Instrument Div. Math functions, for instance, make it easier for users to get the data they want, not just a raw readout of frequency or time interval.

The latest counters also implement the devices and features becoming standard in all types of instruments—usually an IEEE-488 interface and μP control.

Bus control at any price

The IEEE-488 bus is not restricted to the more expensive models, either. It's also available in low-cost counters. For instance, HP's Model 5316A ($1500) furnishes bus-programmable measurement functions,



Modular frequency counters *in Tektronix's TM 500 Series can plug into a mainframe. Units range from the 5-digit, 80-MHz DC 504 ($525) to the 9-digit, 1-GHz DC 508 ($1250). All are compatible with the firm's TM 5000 programmable instrument system.*

Among the various programmable plug-in instruments *in Tektronix's TM 5000 Series, you'll find two counters: Models DC 5009 (135 MHz, $2200) and DC 5010 (350 MHz, $3600).*

dc trigger level and slope. And like the manually controlled Model 5315B ($1050) and the portable Model 5315A ($875), it measures frequency to 100 MHz. It also provides an optional C channel ($250) that increases capability to 1.0 GHz for both continuous-wave and pulsed RF signals as narrow as 60 msec.

All these units measure time intervals from 100 nsec to 100,000 sec. Additionally, their time-interval-averaging function provides greater resolution for repetitive events, and the time-interval-delay feature avoids spurious-signal measurements by holding off the counter's trigger point for a precise, selectable time.

You'll also find IEEE-488 interfaces at the high end of the frequency spectrum. EIP Microwave's Model 575 ($7600) covers 10 Hz to 18 GHz, and Model 578 ($8800), extends this range to 26.5 GHz; optional accessories for 110-GHz capability add another $7000 (see pg 215 in this issue).

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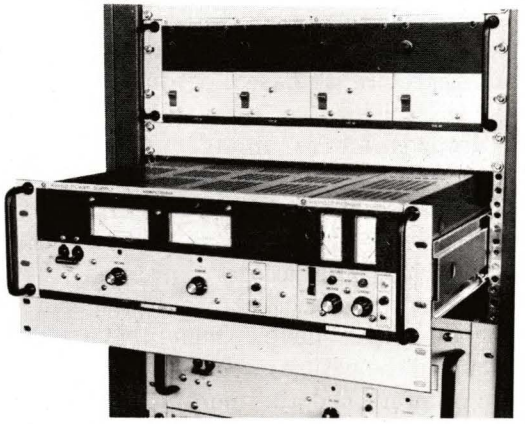

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Both instruments offer source locking, which affords broadband control of swept sources to provide synthesizer stability at relatively low cost. This feature also allows you to control a swept source via the IEEE-488 bus even if the source lacks a bus interface; you program the counters over the bus to set the source at any desired frequency.

μPs enhance features

EIP's instruments exemplify how μPs have found their way into frequency counters, as they have into almost every other instrument.

In early applications, they controlled interfaces to the keyboard, front-panel readouts and rear-panel programming inputs and outputs. Later, they added features such as arithmetic processing. More recent designs, though, use the processor in the measurement process itself, yielding a wider frequency range, shorter measurement time and simpler operation along with lower complexity and cost. Such products are therefore μP based, not merely μP controlled.

Improvements in frequency-counter designs, however, go beyond those implemented in other instrument types, notes Norbert Laengrich, international marketing manager at Racal-Dana Instruments. These developments have changed the nature of both frequency counters and the more capable universal counter/timers.

In frequency counters, the most obvious trend is to higher frequencies. Along with the record-holding 110-GHz models from EIP Microwave, units such as HP's 5345A and Systron-Donner's 6000 Series reach far into the microwave region.

EIP's instruments also typify the trend away from plug-in units to monolithic instruments. Such instruments, with internal modular designs, offer more value than mainframe/plug-in units because they are less expensive to build, explains Howard Lurie, marketing VP at EIP.

A low-cost counter *featuring IEEE-488-bus compatibility, Hewlett-Packard's Model 5316A (bottom) costs $1500. The $1050 nonprogrammable Model 5315B (center) and the $875 portable Model 5315A also provide 488 compatibility.*

To widen frequency range, Lurie's firm's instruments incorporate a second internal down converter, which is mechanically simpler than using front-panel plug-ins. Thus, you don't have to pay for an expensive mainframe more powerful than you require.

Another trend that has surfaced in the last few years is direct counting at higher frequencies, points out Racal-Dana's Laengrich. Compared to prescaler designs, direct-count instruments provide lower conversion times. For example, they can cut conversion times from 10 to 1 sec compared to a divide-by-10 prescaler.

A counter is more than a chip

Laengrich also notes that special-purpose LSI chips for frequency counting have become more widely used. These counter-on-a-chip designs, available from most major instrument vendors, reduce system chip count to achieve lower cost and better reliability.

LSI counter chips also facilitate the design of basic frequency counters, and this fact has led to many vendors offering this type of instrument. A question arises, however, about the staying power of some of these firms because their low-cost products are difficult to distribute and support.

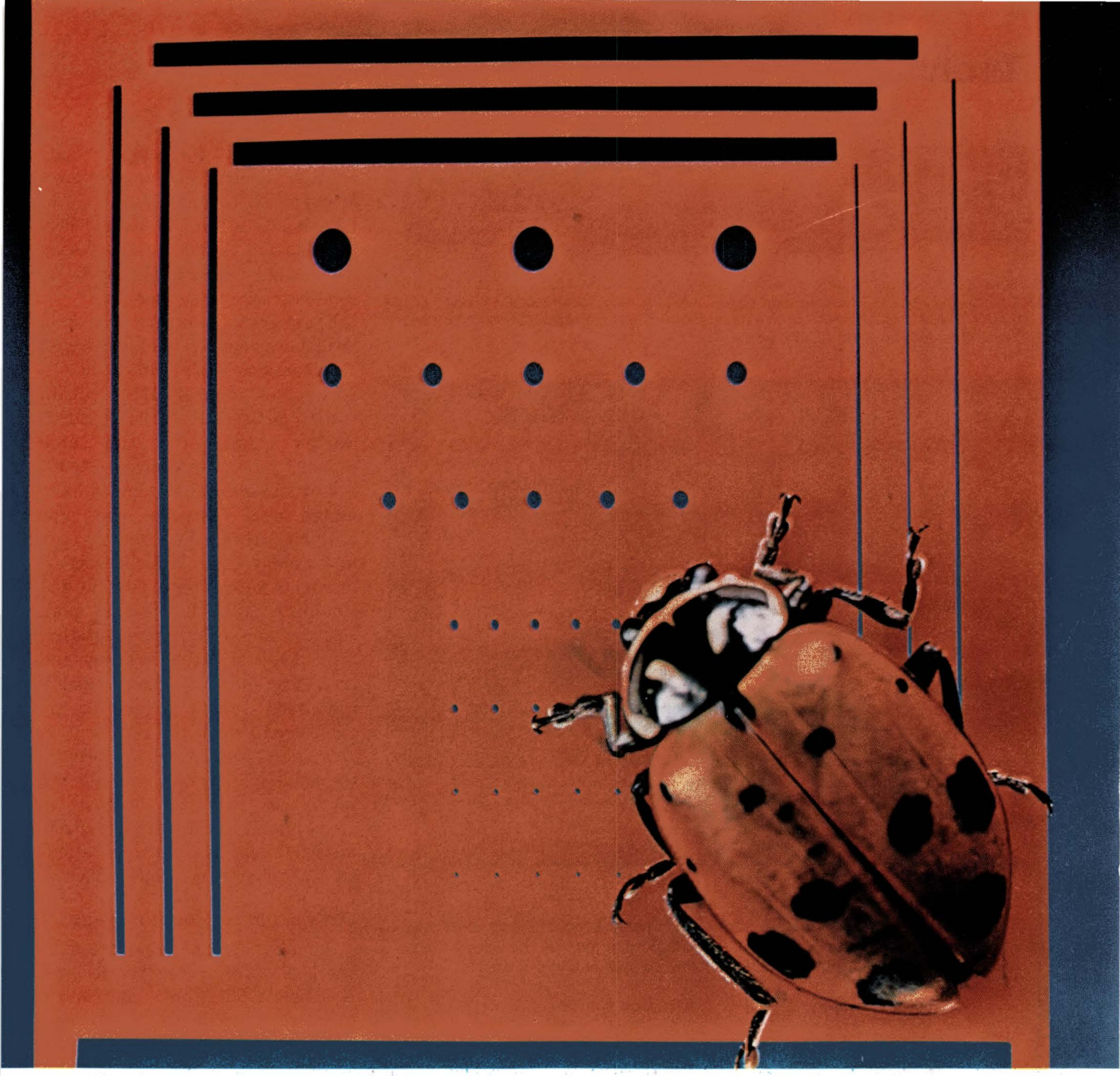
The companies best able to design and market low-cost counters are those with in-house counter-IC capabilities, believes Gail Dishong, product director for frequency and communication products at Systron-Donner. His firm does not claim such in-house capabilities; instead, for continued success it relies on its

The highest frequency you can measure today *with a frequency counter is 110 GHz, and you can measure it with EIP Microwave's Model 578. Models 575 and 578 feature source locking; they can control a swept source to achieve synthesizer-like performance at low cost.*

software and microwave expertise —including its thin-film hybrid technology—to design complex front-end circuits such as those for microwave measurements. Dishong expects Systron-Donner to continue leaving the low end to other suppliers and aim at the midrange to high-performance markets.

One instrument vendor with chip capacity is Hewlett-Packard, a firm that also develops custom circuits. Its multiple-register counter IC handles all counter functions and is in Models 5315A/B and 5316A.

Standard frequency-counter chips have also made it easier for designers to incorporate such functions into other instruments. Thus,



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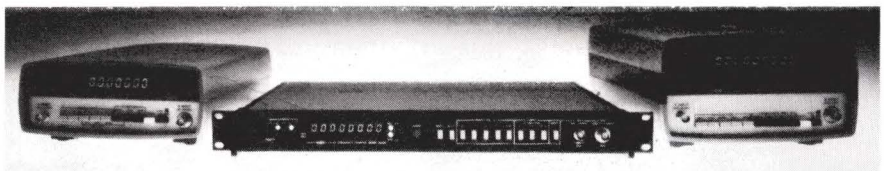
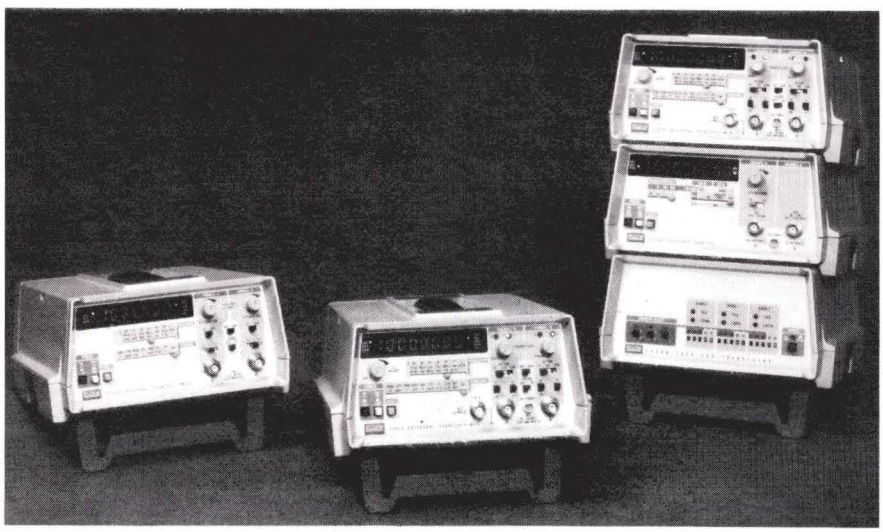


Wide-range frequency counters *from Systron-Donner include Models 6241A (100 MHz, $800) through 6244A (4.5 GHz, $3300), shown at left; thin-line, rack-mounting Models 6041A (100 MHz, $1400) through 6043A (1.25 GHz, $1900), in the center; and Models 6245 (18 GHz, $4700) and 6446A (26 GHz, $5200), on the right.*



Universal counter/timers and basic frequency counters *in Fluke's line include Models 7250A ($675), 7260A ($850) and 7261A ($995) universal counter/timers and Model 7220A counter ($1050).*

For more information...

For more information on the frequency-counter products and services described in this article, circle the appropriate numbers on the Information Retrieval Service card or contact the following manufacturers directly.

EIP Microwave Inc
2731 N First St
San Jose, CA 95134
(408) 946-5700
Circle No 636

John Fluke Mfg Co Inc
Box C9090
Everett, WA 98206
(206) 342-6300
Circle No 637

Hewlett-Packard Co
1507 Page Mill Rd
Palo Alto, CA 94304
Phone local office
Circle No 638

Leasametric Inc
1164 Triton Dr
Foster City, CA 94404
(415) 574-4441
Circle No 639

Nicolet Paratronics Inc
2140 Bering Dr
San Jose, CA 95131
(408) 263-2252
Circle No 640

Racal-Dana Instruments Inc
18912 Von Karman Ave
Irvine, CA 92713
(714) 833-1234
Circle No 641

Systron-Donner Instrument Div
2727 Systron Dr
Concord, CA 94518
(415) 676-5000
Circle No 642

Tektronix Inc
Box 1700
Beaverton, OR 97077
(800) 547-6711; in OR,
(800) 452-6773
Circle No 643

US Instrument Rentals Inc
2988 Campus Dr
San Mateo, CA 94403
(415) 572-6600
Circle No 644

Vu-Data Corp
7170 Convoy Ct
San Diego, CA 92111
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Circle No 645

you'll find counter capability in logic analyzers such as Paratronics's Model NPC-764 or System 5000. HP's Model 1611A and Model 64000 development system also provide counter-like capabilities such as time-interval measurements.

Frequency counters are also available as options in oscilloscopes; Tektronix's Model 465B has a frequency counter/DMM option costing $445, and Vu-Data's PS900 Series scopes offer the same capability for approximately $400.

Universal counter/timers have added new features, too. For example, these instruments can now usually make high-level measurements for rise time, fall time and slew rate. They also feature more selective measuring characteristics, with sophisticated arming and triggering functions. These capabilities allow you to trigger exactly where you want to, not just on voltage crossings, and synchronize the counter to any desired pulse, not just the first or largest in amplitude. And they simplify measurements, especially in applications such as radar burst measurements.

CRTs could aid counter usage

Simplifying measurements will be one goal of future counter designs. A simple CRT screen built into a counter, for instance, could help users to visualize trigger levels and frequencies and provide greater confidence in measurements.

In this regard, HP's Watts feels that too many engineers, lacking this visual aid, turn to oscilloscopes for such measurements. Scopes, however, permit relatively accurate frequency measurements at best. Watts thus foresees a monolithic counter with a CRT tailored to frequency-counter needs as a more inexpensive alternative to a modular CRT/instrument design with frequency-counter functions.

This speculation shows how valuable a counter with a built-in CRT would be in bench applications. In system applications, designers

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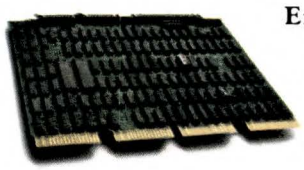

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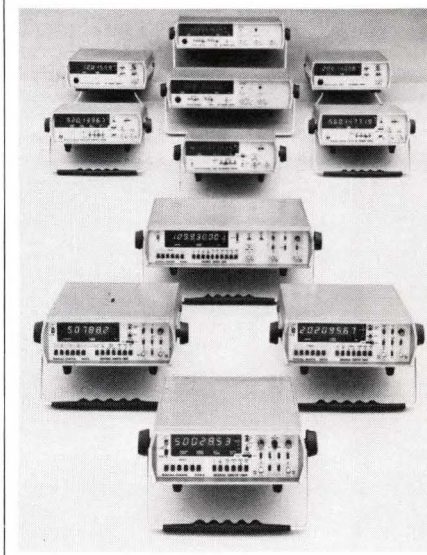

Measuring frequencies from 30 MHz to 3 GHz, *frequency counters and universal counter/timers in the 99Hundred Series from Racal-Dana ($625 to $2195) cover HF, VHF, UHF and microwave ranges and feature timebase, battery-pack and IEEE-488 options. A bipolar collector-diffusion-isolation LSI chip operating at frequencies greater than 60 MHz handles most counter functions.*

would perhaps use a counter and oscilloscope to set up the system, then use a counter tailored to the application—perhaps without panel controls—in the operating system.

A CRT, however, would probably not prove too useful in microwave applications, says EIP Microwave's Lurie: At these frequencies, the user generally deals with a well-defined signal confined to a narrow frequency range.

CRTs could also help overcome another counter problem: control complexity. To provide access to all functions, front panels have become large, complex and even intimidating to many users. A solution might be to take a lesson from logic analyzers and employ CRTs and pushbuttons to facilitate function selection via menus.

HP's Watts points out one final area of counter design that will improve—input characteristics. Today's counters have dynamic ranges too narrow to handle applications such as measuring the rise time of a TTL pulse. Tomorrow's counters, however, should overcome this limitation. **EDN**

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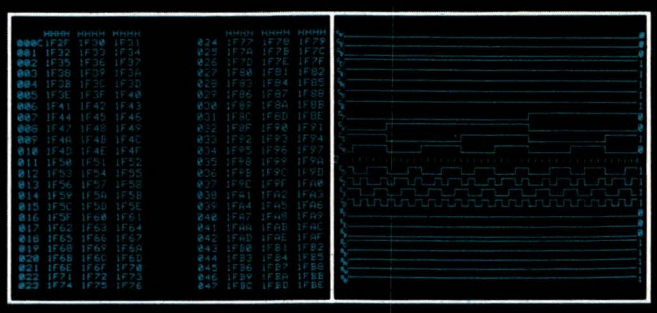

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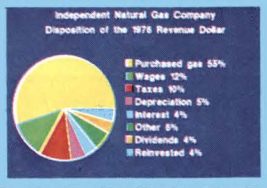

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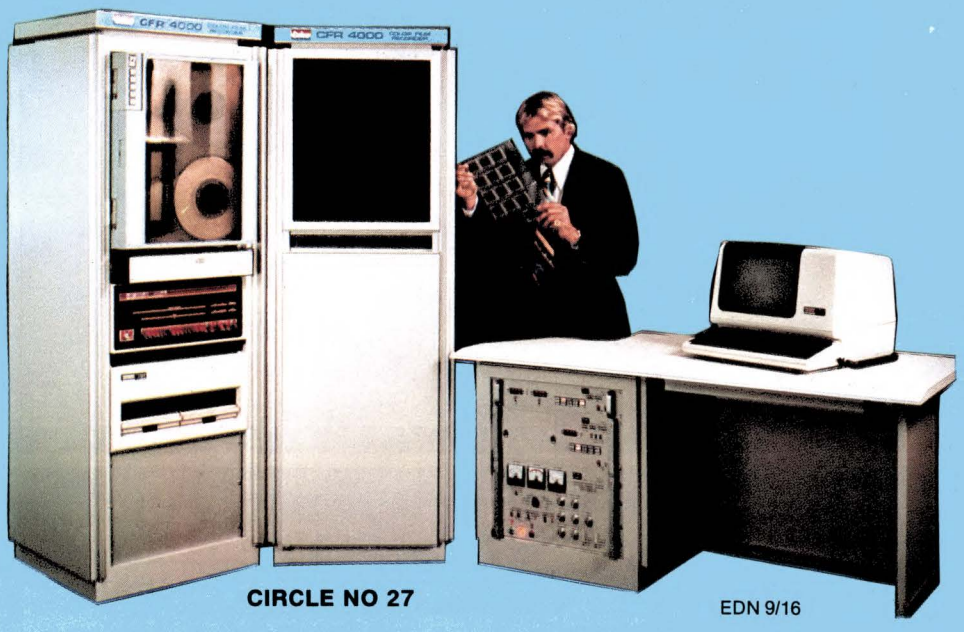


CIRCLE NO 27

EDN 9/16

Intelligent-terminal hardware, software evolves to meet dual designer needs

Patrick Kenealy and **David H Freedman,** GML Corp

With some intelligent terminals virtually indistinguishable from stand-alone systems, manufacturers are still looking for that novel combination of mass storage, μP and communications capability that will give them a niche in an as-yet-undefined market. But now two areas of competition—both with implications for OEM designers—are emerging for first-generation intelligent-terminal manufacturers who seek a market edge:

- Development of the hardware and software features to support special functions
- Improvement of the price/performance characteristics of nonspecialized, μC-like intelligent terminals.

An RS-232C-interfaced ASCII terminal, *the CTM-300 from Matrox Electronic Systems also features an 8-color CRT display. You can customize its functions from the host computer via a downloaded program.*

Defining a typical terminal

The intelligent-terminal market spans distributed-processing, office-automation, word-processing, graphics and stand-alone applications. Although this diversity of functions denies manufacturers a coherent market against which to define product features and prices, companies have nevertheless characterized first-generation intelligent terminals themselves.

Such a full-function unit typically incorporates 64k bytes of RAM, an 8-bit μP and one or more floppy-disk drives. It supports at least one programming language and offers a standard or optional serial printer.

Patrick Kenealy and **David H Freedman** are editors of *Terminals Review* and The Display Pricing Strategy Service, published by GML Corp, Lexington, MA.

Many intelligent units display sophisticated graphics, and more than a dozen current models feature multicolored displays. The user-programmable CTM-300 from Matrox Electronic Systems, for example, incorporates an 8-color CRT display and sells for less than $3000.

Average intelligent-terminal prices (**figure**) now range from $4000 to $8000 for basic units and from $6000 to $10,000 for units with bundled software and printers; prices, however, continue to drop. The wide price distribution results from the diversity of terminal applications; similar hardware configurations can command different prices depending on customers' applications and price tolerances.

You can program virtually all intelligent terminals in assembly language, and more than half support BASIC. COBOL, FORTRAN and PASCAL are also widely supported, and many intelligent terminals feature CP/M or similar operating systems with extensive multilanguage capability.

Move to specialization

As distributed processing, office automation, word processing and other intelligent-terminal applications become more standardized, intelligent-terminal manufacturers will be forced to dedicate their machines to fewer and fewer applications. Datapoint Corp and Texas Instruments, both specializing in distributed data processing, exemplify this trend. Wang Laboratories has notably stressed office automation, and still other manufacturers, such as Chromatics, have branched into the business color-graphics market.

Intelligent Systems, Televideo

and Zentec, on the other hand, continue to offer general-purpose intelligent terminals that provide users with the equivalent of a stand-alone μC. For example, Zentec's latest offering in this product area, its ZMS-35, employs a 8085 μP and sells for $1350.

Although such terminals usually cannot support extensive word-processing or shared-database capabilities, they allow users to develop and run programs off line, reducing demands on their hosts.

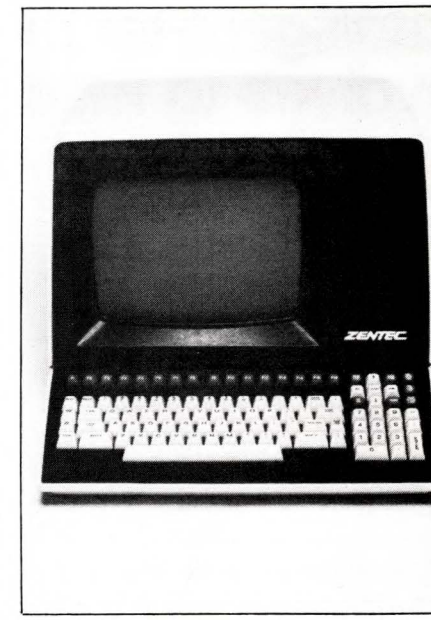
What's to come

The intelligent-terminal product area continues to develop. First-generation intelligent terminals, whether specialized or general purpose, are now being joined by second-generation hardware—128k-byte, 16-bit systems based on Winchester disk drives and backed by streaming cartridge-tape drives.

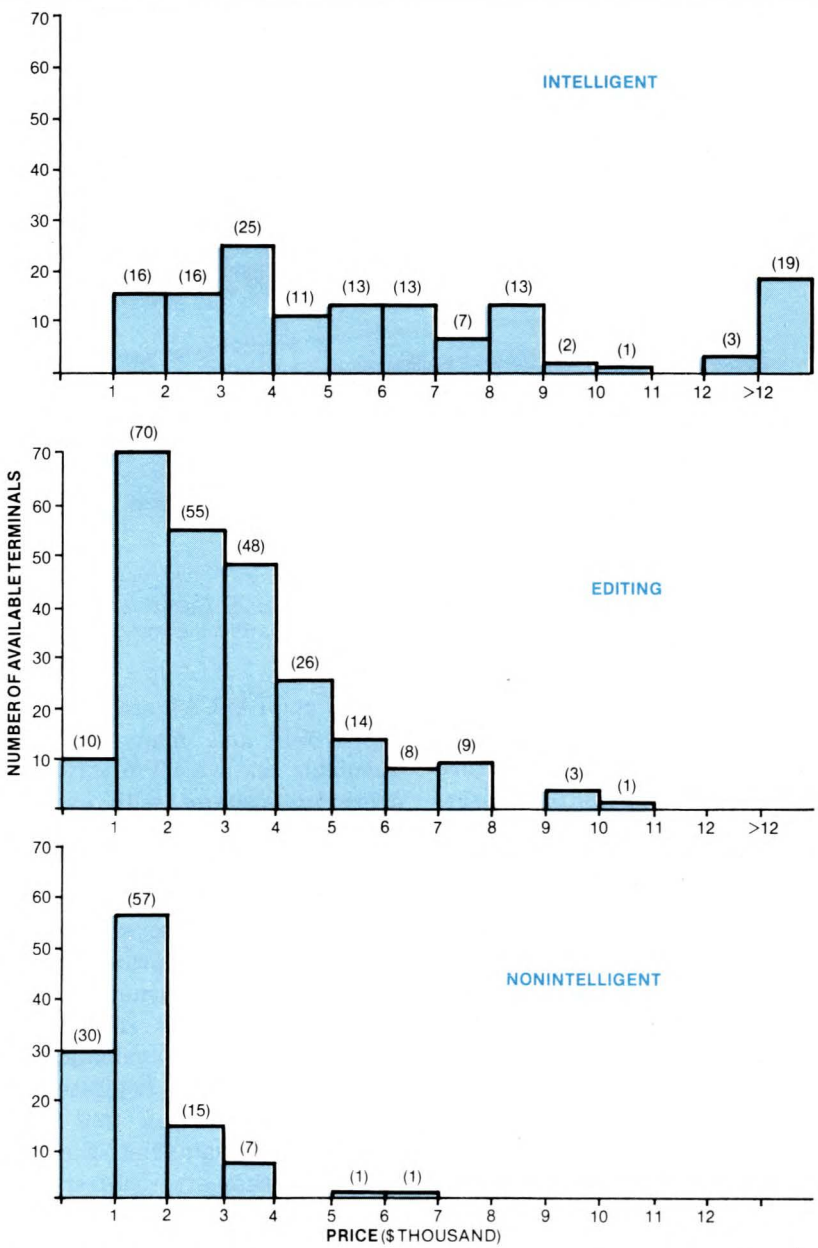
This second-generation hardware suits users designing systems for distributed-processing/office-automation applications. Additionally, prices for 8-bit μPs and memory continue to fall for firms offering basic stand-alone units. Thus, such a system should eventually sell for less than $3000, including a low-cost matrix printer. Distributed-processing units, on the other hand, should sell for $5000 to $10,000.

Memory-, μP- and diskette-system prices are stabilizing just as display-tube, keyboard and power-supply costs have, and prices for basic intelligent units should become more defined and competitive in the next 8 months.

Developments further in the future promise to be just as interesting. The intelligent-terminal industry combines high profits and high risk. Prices and profit margin both remain high and flexible, along with off-line-storage,



Based on an 8085 μP, *Zentec's ZMS-35 provides 16k bytes of user RAM, a fully configurable keyboard and a 12-in. nonglare CRT with a 128-character set.*



Plotting terminal prices against available units *shows that intelligent-terminal capabilities are not as well defined as those of editing terminals (which feature line and character insert and delete capabilities) and nonintelligent terminals (which aren't programmable and don't have editing functions). Editing-terminal prices are clustered less tightly than those of nonintelligent terminals because editing-terminal manufacturers can add features to make higher priced units competitive. The more expensive units are often ruggedized devices or cluster configurations.*

Mail us this ad

and we'll help you discover simple, effective solutions to difficult troubleshooting problems.

FAULT	STIMULUS	RESPONSE	TEST METHOD
Shorted Node	546A Pulser[1]	547A Current Tracer	• Pulse shorted node • Follow current pulses to short
Stuck Data Bus	546A Pulser[1]	547A Current Tracer	• Pulse bus line(s) • Trace current to device holding the bus in a stuck condition
Signal Line Short to Vcc or Ground	546A Pulser	545A Probe Current Tracer	• Pulse and probe test point simultaneously (short to Vcc or Ground cannot be overridden by pulsing) • Pulse test point, and follow current pulses to the short
Vcc to Ground Short	546A Pulser	547A Current Tracer	• Remove power from test circuit • Disconnect electrolytic bypass capacitors • Pulse across Vcc and ground using accessory connectors provided • Trace current to fault
Internally Open IC	546A Pulser[1]	545A Probe	• Pulse device input(s) • Probe output for response
Solder Bridge	546A Pulser[1]	547A Current Tracer	• Pulse suspect line(s) • Trace current pulses to the fault • Light goes out when solder bridge passed
Sequential Logic Fault in Counter or Shift Register	546A Pulser	548A Clip	• Circuit clock de-activated • Use Pulser to enter desired number of pulses • Clip onto counter or shift register and verify devices truth table

1. Use the Pulser to provide stimulus, or use normal circuit signals, whichever is most convenient.

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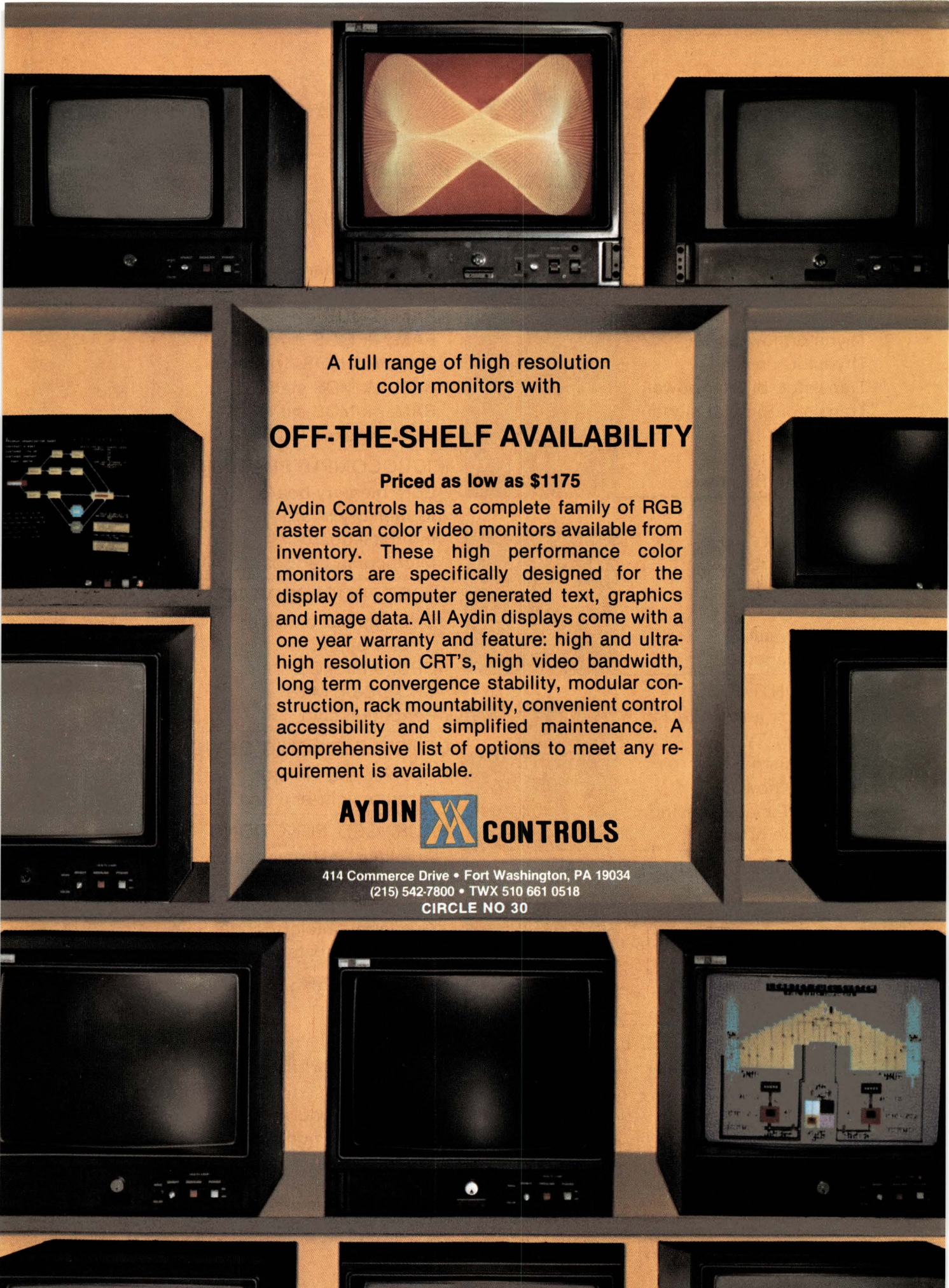
CIRCLE NO 28

printer and software-development costs. Thus, manufacturers of stand-alone, general-purpose intelligent terminals will compete with one another as well as with μC vendors. (Commercial μC systems, however, usually communicate with larger computer systems and sell for less than intelligent terminals with similar software, memory and off-line storage.)

Manufacturers of intelligent terminals for distributed-processing applications will find themselves competing as system vendors rather than terminal vendors. Datapoint, Four-Phase, Northern Telecom and others will face minicomputer manufacturers such as DEC, Honeywell and Hewlett-Packard rather than mainstream terminal firms. And as 16-bit μCs are used more frequently in intelligent terminals, those terminals will become even less distinguishable from minis and small business systems.

Proprietary operating systems, communication interfaces and other software will keep prices for such intelligent terminals high, and their manufacturers will have to offer field service, extensive peripheral-software support and flexible leasing arrangements to remain competitive with minicomputer firms. A solid intelligent-terminal-firm commitment to distributed processing will thus amount to that firm's leaving the terminal industry and entering the minicomputer industry. **EDN**



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Leadtime Index

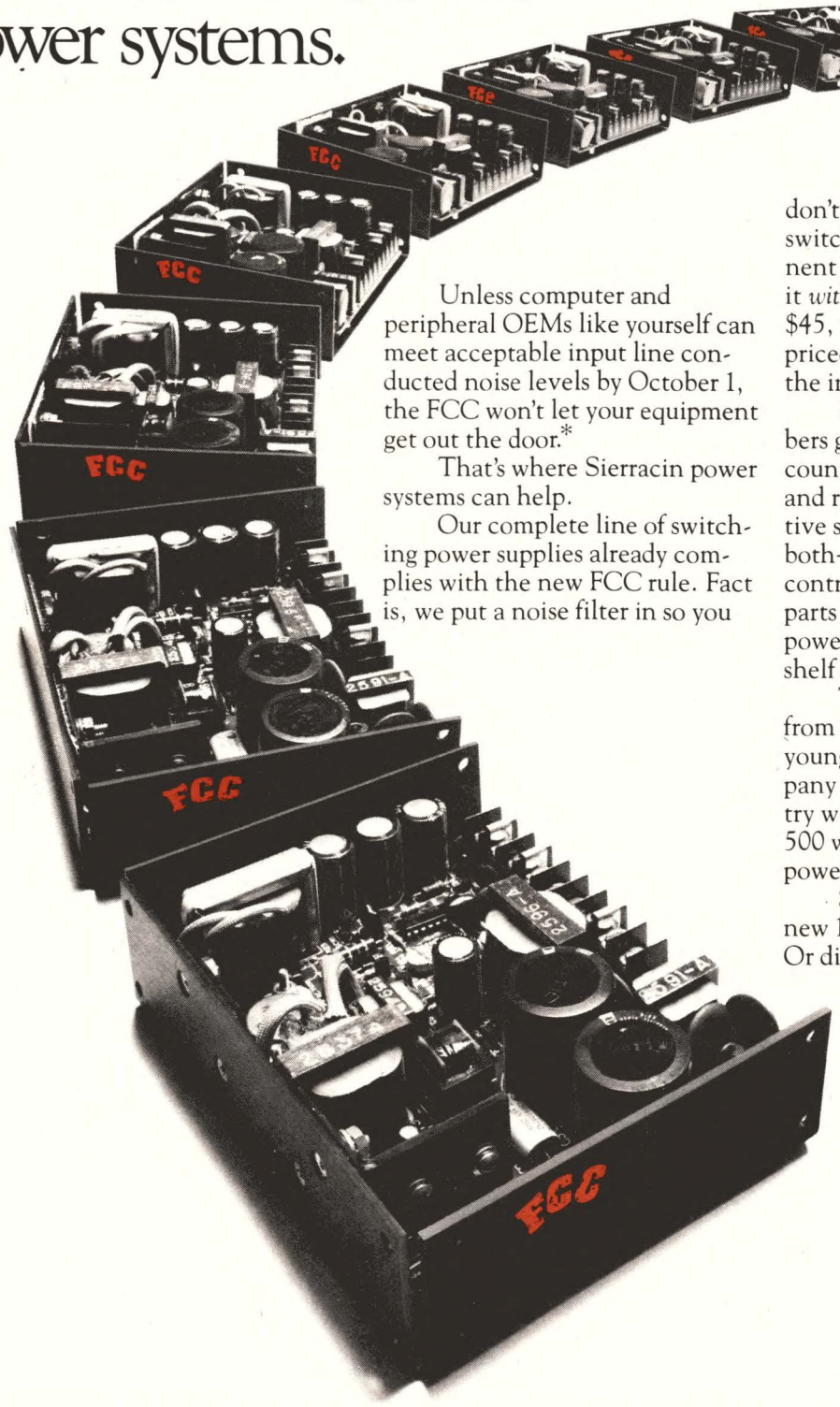
ACTIVE COMPONENTS

PRODUCT	LEADTIME IN WEEKS Min.	Max.	Trend
DISCRETE SEMICONDUCTORS			
Diode, switching	2	4	=
Diode, zener	1	5	=
Rectifier, low-power	1	5	=
Rectifier, power	1	4	=
Thyristor, low-power	1	4	=
Thyristor, power	2	7	=
Transistor, bipolar power	6	13	=
Transistor, bipolar signal	6	20	=
FET, power	5	12	=
FET, signal	4	10	=
Transistor, RF power	5	12	=
DISPLAYS			
Fluorescent	2	12	=
Gas-discharge	1	12	=
Incandescent	4	8	=
LED	2	8	=
Liquid crystal	2	10	⌂
Plasma panel	5	12	=
ELECTRON TUBES			
CRT, black and white TV	6	14	⌂
CRT, color TV	8	12	=
CRT, industrial	8	16	⌂
Industrial power	4	10	=
Light and image sensing	4	10	=
Microwave power	9	13	=
INTEGRATED CIRCUITS, DIGITAL			
CMOS	4	10	=
Diode transistor logic (DTL)	6	12	▼
Emitter-coupled logic (ECL)	4	16	⌂
Low power Schottky TTL	5	17	=
Standard Schottky TTL	6	18	=
Standard TTL	6	18	=
INTEGRATED CIRCUITS, LINEAR			
Communications circuit	6	14	=
Data converter	8	12	⌂
Interface circuit	6	15	=
Operational amplifier	1	3	=
Voltage regulator	1	4	=

PRODUCT	LEADTIME IN WEEKS Min.	Max.	Trend
MEMORY CIRCUITS			
EPROM	3	5	=
PROM, bipolar	3	4	▼
RAM, bipolar	3	14	▼
RAM, CMOS	2	10	=
RAM, 4k MOS dynamic	4	16	=
RAM, 16k MOS dynamic	4	16	=
RAM, 1k MOS static	4	16	=
RAM, 4k MOS static	4	14	=
ROM, masked MOS	5	15	▼
MICROCOMPUTER/MEMORY SYSTEMS			
Core memory board	5	9	=
IC memory board	5	9	=
Interface board	4	8	⌂
Microcomputer board	3	9	=
MICROPROCESSOR IC'S			
CPU, bipolar bit slice	3	14	⌂
CPU, 4-bit MOS	4	12	⌂
CPU, 8-bit MOS	3	12	=
CPU, 16-bit MOS	4	14	=
Peripheral chip	5	14	=
OPTOELECTRONIC DEVICES			
Coupler and isolator	7	14	▼
Discrete light-emitting diode	9	19	=
PACKAGED FUNCTIONS			
Amplifier, instrumentation	3	11	▼
Amplifier, operational	2	9	▼
Amplifier, sample/hold	5	12	=
Converter, analog/digital	5	9	⌂
Converter, digital/analog	5	9	⌂
PANEL METERS			
Analog	10	18	⌂
Digital	5	15	=
POWER SUPPLIES			
Custom	15	18	=
Enclosed modular	7	16	=
Open-frame module	11	18	⌂
Printed circuit	10	16	=

Leadtimes are based on recent figures supplied to *Electronic Business* magazine by a composite group of major manufacturers and OEMs. They represent the typical times necessary to allocate manufacturing capacity to build and ship a medium-sized order for a moderately popular item. Trends represent changes expected for next month.

Will the FCC put you in a cost-delivery crunch October 1? Not with Sierracin power systems.



Unless computer and peripheral OEMs like yourself can meet acceptable input line conducted noise levels by October 1, the FCC won't let your equipment get out the door.*

That's where Sierracin power systems can help.

Our complete line of switching power supplies already complies with the new FCC rule. Fact is, we put a noise filter in so you don't have to redesign around our switchers. Or add to your component count. Or costs. And we did it *without* increasing our prices. (At $45, we still offer you the lowest priced switching power supply in the industry.)

But anyone can play the numbers game with prices. What really counts is product performance and reliability. And our cost-effective switchers and linears give you both—the results of high quality control standards—from incoming parts inspection and testing to final power supply burn-in and on-the-shelf stocking for fast delivery.

That's what you can expect from Sierracin/Power Systems. A young, dynamic 6-year-old company that already leads the industry with the widest line of 40 to 500 watt open frame DC switching power supplies.

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*For details, ask for our free Question & Answer booklet, "The FCC and You."

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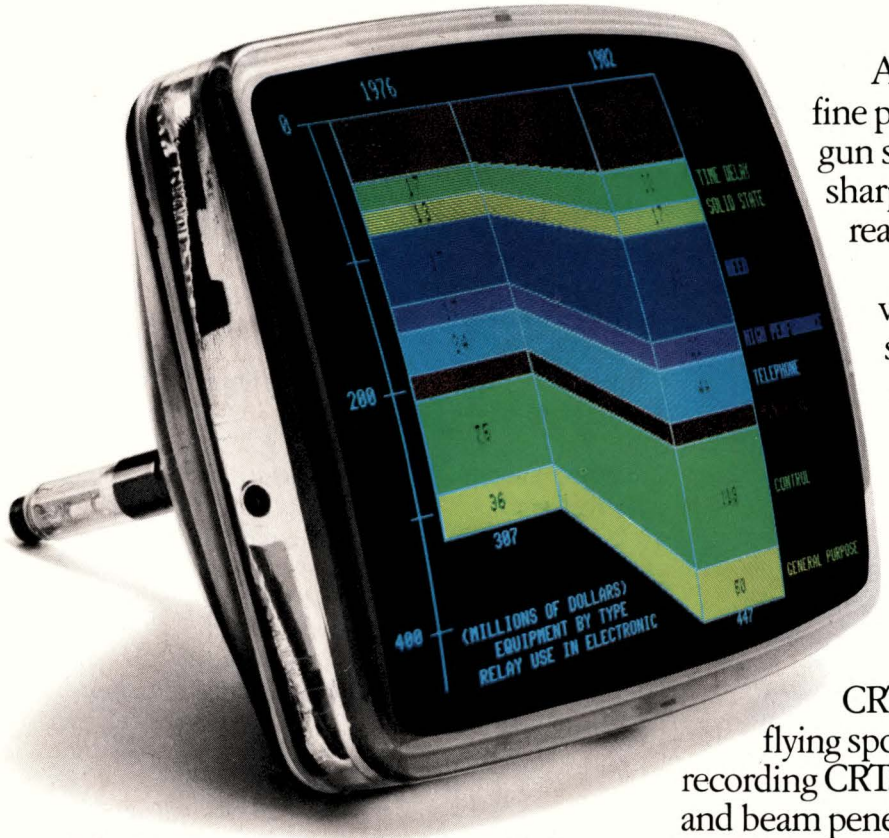
CIRCLE NO 31

FOR A CLEANER, BRIGHTER PICTURE, TRY A TUBE OF MITSUBISHI.



Mitsubishi cathode ray tubes will do wonders for your image.

Because each of our high-resolution color CRTs actually discriminates among 64 distinct colors.

Our radar CRTs give your data systems the kind of pin point clarity that assures pin point accuracy.

And our black and white CRTs differentiate between shades of grey.

We begin with our own phosphors, specially developed for their brightness. They give our screens their notably short, or long flicker-free persistence.

Our precision electron gun system insures that each beam is perfectly aligned with the shadow mask.

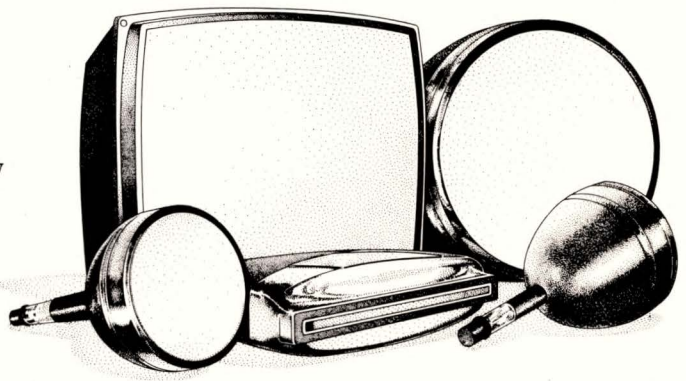
And, combined with our ultra-fine pitched shadow mask, the gun system produces a picture so sharp, it actually encourages reading fine print.

Another Mitsubishi innovation is our internal magnetic shield. It not only more efficiently eliminates exterior magnetic forces, but makes the unit much easier to service. Not to mention what the magnetic shield does for a purer image, in both monochrome and color.

Mitsubishi's complete CRT line includes high-resolution flying spot scanner CRTs. Fiber optic recording CRTs. High-precision display, radar and beam penetration CRTs.

For more information on a display that's worthy of your data system, call our Display Products Group at (213) 979-6055 (or in New Jersey, call (201) 753-1600) or write Mitsubishi Electronics of America, Inc., 2200 W. Artesia Blvd., Compton, CA 90220.

We'll gladly show you a CRT for sore eyes.



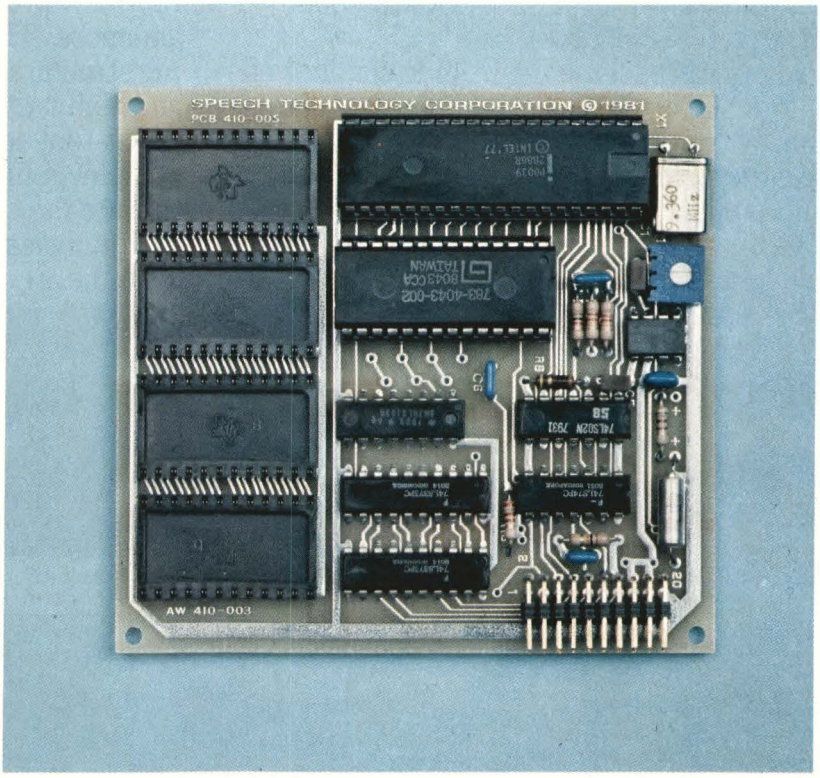
MITSUBISHI ELECTRIC COLOR CATHODE RAY TUBES

Speech module generates 120 words

Model M410 Speech Generator board uses a single-chip voice synthesizer to provide low-cost voice output for virtually any computer system. Measuring 3.75×4×0.5 in., it includes the linear-predictive-coding (LPC) speech chip, a μP, a clock, control logic and memory.

You add the board to your system via a 20-pin flat-cable connector. Designing a parallel interface for it is easy: It looks like an 8212 parallel latch and buffer to the μC and runs on a 5V power supply (225 mA typ).

For S-100-bus systems, you can even choose a larger version (Model VR/S100) that plugs directly into any bus slot.



Speaking for nearly any μC system, *the M410 speech generator provides all the flexibility you need in a voice-response peripheral.*

The word's the thing

In four 32k EPROMs, the speech generator stores approximately 120 words and phrases. (Typical word packing puts 12 to 20 words in a 16k memory or 25 to 40 words in a 32k unit.)

The manufacturer supplies a basic vocabulary in one 32k EPROM and includes the digits one through nine and the words *plus*, *minus*, *times*, *point*, *is*, *enter*, *repeat*, *error*, *what?*, *oh*, *thank you* and *goodbye*. You also get pauses of 50, 100, 200 and 400 msec, which allow you to pace the speech output and make it more intelligible.

If none of these words suits your needs, you can choose (for an extra charge) from the manufacturer's rapidly growing library of pre-encoded utterances. And if the library doesn't fill your needs, the firm will create the exact custom vocabulary you require for $200 per second of speech ($1000 minimum).

If you choose to develop such a custom vocabulary, you can select among data rates ranging from 1200 to 1600 bps for low-quality speech and from 2000 to 2200 bps for high-quality output. (The lowest data rates provide the largest vocabulary.)

Getting the words out

You connect the M410's audio output directly to an 8Ω speaker. The board outputs 0.2W and requires no additional circuitry for speech generation. You can even make the system speak on the telephone by connecting it directly over an acoustic coupler.

You address vocabulary words with an 8-bit parallel code. The on-board μP accepts 54 bytes of selector codes, storing them in its internal RAM and thus acting as a FIFO buffer.

If the buffer gets full, the board's Ready line goes LOW, inhibiting the selection of new words until the buffer has room for them. Further, if you choose an invalid selector code, the μP ignores it and looks for the next.

$95 (OEM qty); $185 (1-19) with basic vocabulary. S-100 VR/S100A version, $190 (OEM qty) with no vocabulary; $325 (1-19) with the basic vocabulary.

Speech Technology Corp, 631 Wilshire Blvd, Santa Monica, CA 90401. Phone (213) 393-0101. **Circle No 456**

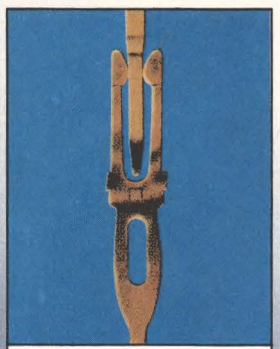
A LITTLE BASIC TRAINING FOR SMART MILITARY DESIGNERS.

The demands of military and avionics specifications put a lot of pressure on a designer. High quality, high reliability and high performance are a must, which is why you should know about Teradyne.

Teradyne has become the leading supplier of tuning fork and blade backplane interconnection systems by continuously meeting the toughest performance standards.

As a company, we are committed to solving the special challenges posed by high reliability, high performance specifications.

High reliability any way you need it.



KS1025 contacts feature special contouring and smoothing to lower insertion force and optimize performance under vibration.

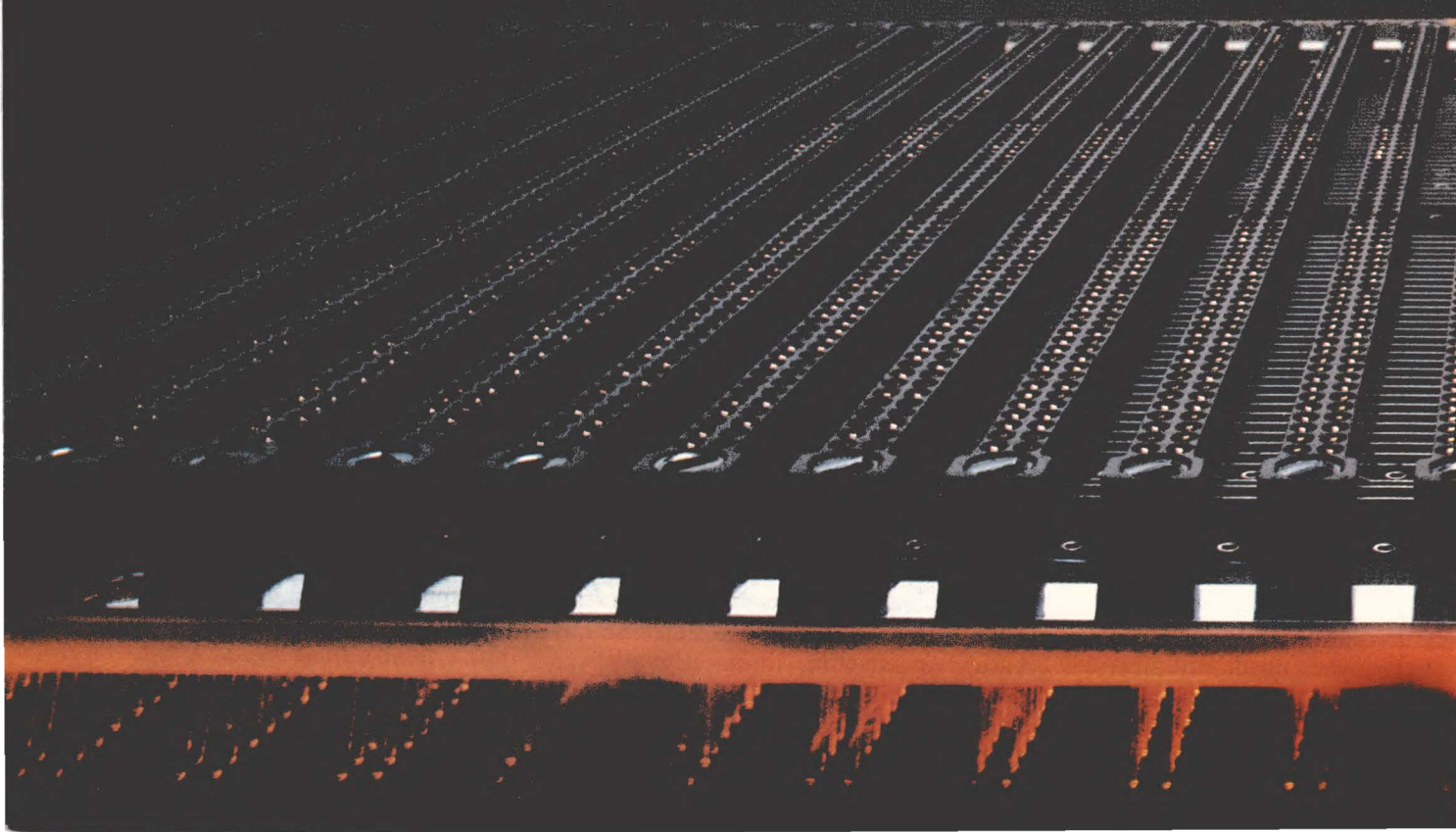
milled aluminum panels or thick copper multilayer PC panels, Teradyne can deliver.

Our S1000 Series of aluminum backplanes are routinely produced with up to 20,000 contacts and more. They are ideal for applications requiring structural rigidity, high power dissipation, and high interconnect density and flexibility.

Custom demands for unique contact patterns, complex milling and integrated voltage distribution are the challenges our reputation was built on.

Teradyne two-sided and multi-layer PC panel systems are designed for high speed and tight

S1000 multi-layer aluminum backplane for airborne radar system. Milled and laminated for maximum stiffness and interconnection density.



impedance control. Good news if you're dealing with advanced IC logic families. The KS1025 Series features Dynamic Retention* press-fit compliant contacts for unsurpassed reliability and performance. *Pat. No. RE29513

Both the S1000 and KS1025 Series can save you money, too. Thanks to the high performance and low cost achieved with Teradyne's MISER LPG™ selective gold plating technology.

VERSACON™ Headers.

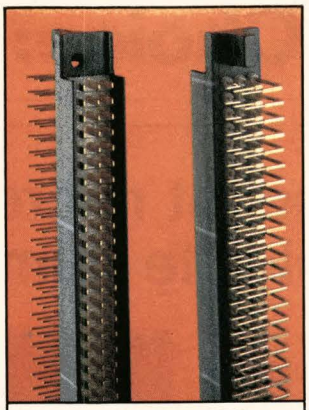
The other side (blade half) of the connection is handled by Teradyne's VERSACON headers.

Fabricated of rugged, lightweight aluminum, VERSACON completely outperforms molded headers.

Teradyne pioneered the technology which permits us to manufacture VERSACON headers as long as 20 inches to the tightest tolerances.

Other features you should know about are the special contact arrangements which require up to 30% less insertion force and VERSACON's shielding against electromagnetic interference.

Going from design concept to prototype in as little as six weeks is no particular problem, either. Teradyne can move fast and still hit your system budget.



Three row VERSACON header. Available in 2-, 3-, and 4-row 0.100", 0.125", and 0.150" grid configurations.

The list of those who have already chosen Teradyne fork and blade backplane systems is a distinguished one. F-15, F-16, F-18, Tornado, AWACS, TRI-TAC, Wavell, Trident, Aegis and Patriot are populated with Teradyne connection systems.

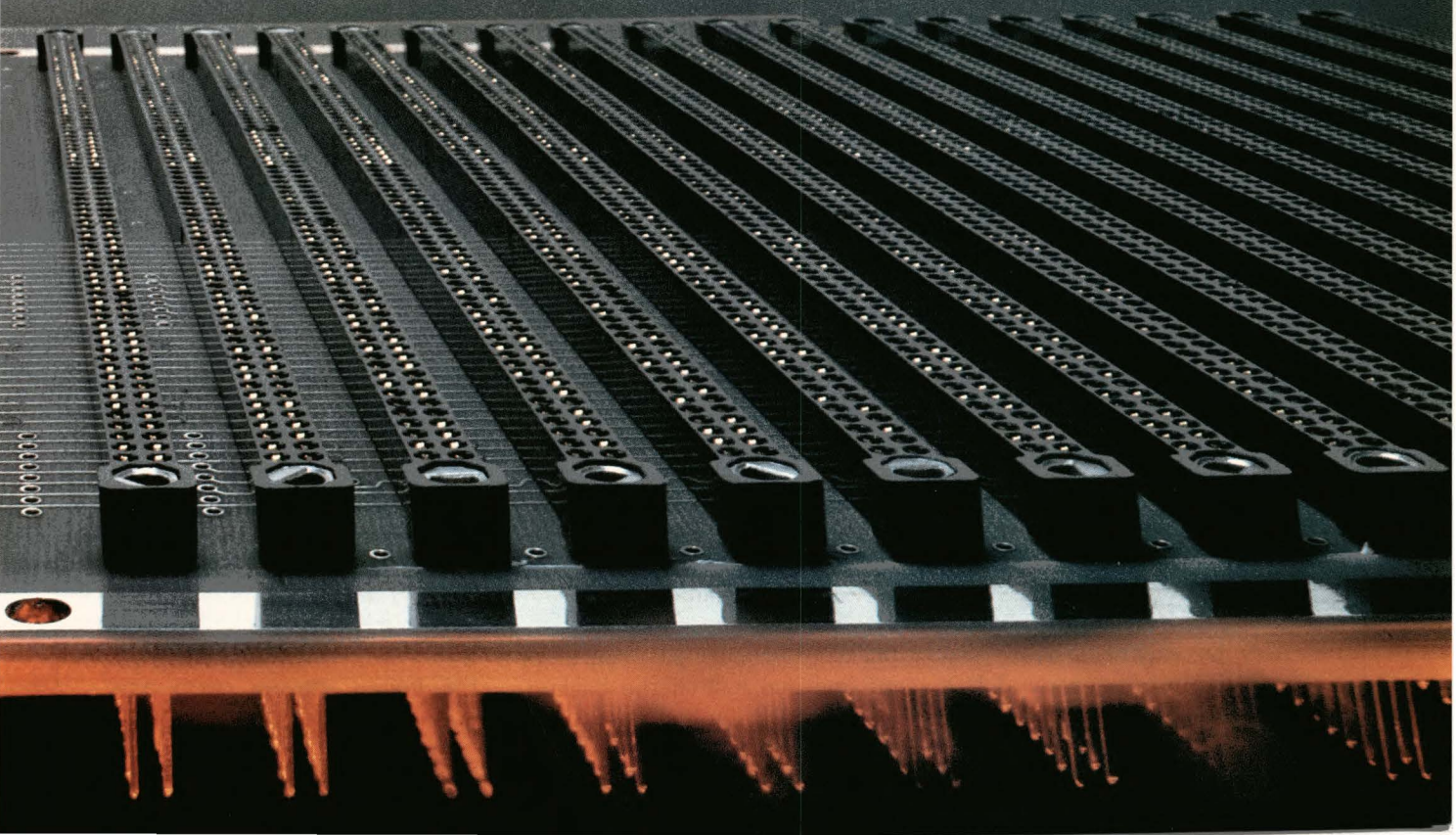
You'll also find Teradyne on the new 757 and 767 jet liners.

So if you're working with MIL-C-28859, MIL-C-28754 or WS6157, or if you simply want the highest quality backplane systems in the world, contact Teradyne.

All the facts and a complete Teradyne system design kit are yours for the asking. Write Teradyne Connection Systems, Inc., 44 Simon St., Nashua, N.H. 03060. Or call (603) 889-5156.

TERADYNE

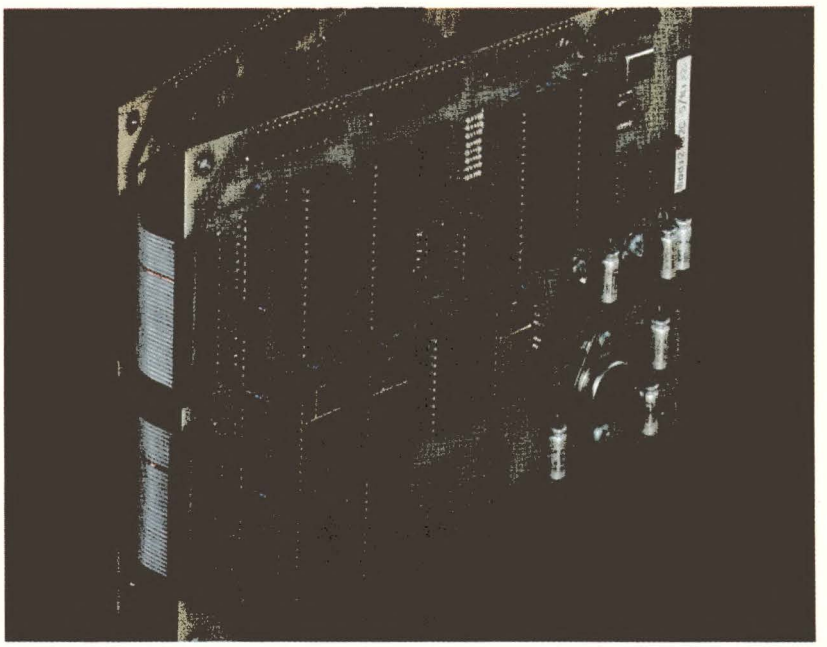
CIRCLE NO 33



Dual-redundant microcomputer system delivers fail-safe bumpless transfers

A fail-safe processor for real-time process-control applications, Model DRS2102 dual-redundant μC system executes a bumpless transfer between its primary and secondary computer boards in the event of a primary-unit fault. The dual redundancy improves computer availability (eg, percentage of total time a system is up and operating properly) in applications where loss of the computer can lead to costly or dangerous operating conditions.

Cutover from a primary to a secondary control unit usually results in a temporary loss of control, shutdown or manual operation until secondary-unit initialization and on-line placement. But the DRS2102's hardware/software design eliminates these problems by effecting a cutover in 5 to 10 μsec—fast enough to keep up with high-speed processes.



Two 8085-based μC boards *combine to produce a dual-redundant controller that ensures proper operation of real-time process-control systems. When a fault occurs in one board, the Redundancy Manager operating system pulls it off line and switches in the second board, performing a fail-safe bumpless transfer.*

Dual boards do the job

The DRS2102 comprises two identical μC boards linked by buffers that don't corrupt the receiving μP should either one fail. The linkage allows each μC board (A and B) to communicate continuously; thus, each board is always in the same state.

Each board contains an 8085 μP and 8k bytes of memory, consisting of static RAM for a real-time database and PROM or EEPROM for control firmware. Upon power shutdown, variable data goes to EEPROM or a separate 4k-byte core module.

Also on each board are six addressable bidirectional I/O ports, three programmable timers, interrupt inputs and an RS-232C port. An expansion bus allows use of a 16k-byte static-RAM board and a 4k-byte core board.

An external interface and display module contains status lights, numerical readouts and a hexadecimal keypad for manual access to the μC system. It operates via a control port on the μC system.

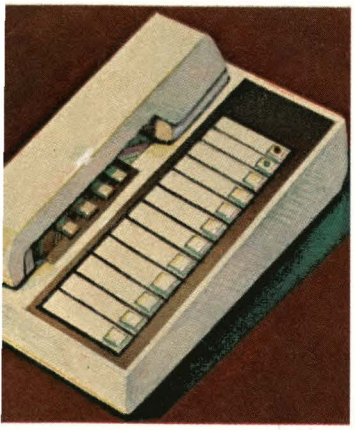
Both μC boards function under control of the Redundancy Manager operating system. This OS checks critical variables in the application-program flow for proper response and validity. If it detects a fault, it can retry on a nonfatal fault or activate the output selector to push the primary μC (board A) off line and switch the backup μC (board B) on line.

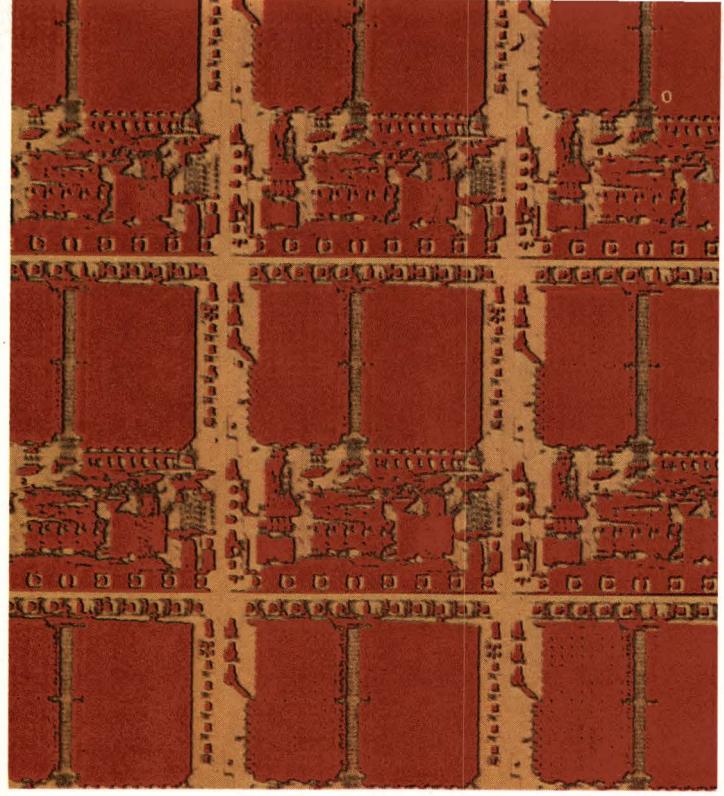
Because of the communication requirements between the A and B boards, the μC system does not employ an industry-standard bus (eg, STD, S-100 or Multibus). Instead, the manufacturer has opted for a no-bus or direct handshaking version, simplifying system expansion and circuit operation.

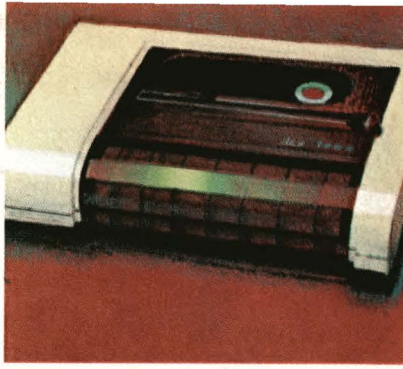
Packaged on two stackable 6×8-in. pc boards, the μC system utilizes flat cable for interconnections. Accepting raw +8 and ±16V dc power, each board contains regulators for reduced common-mode noise.

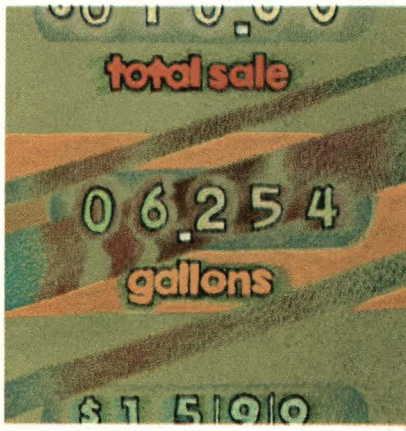
Operating over 0 to 70°C, the system costs $3250 (OEM qty) without software.

Del Rey Systems Inc, 8929 Sepulveda Blvd, Los Angeles, CA 90045. Phone (213) 641-4955. **Circle No 457**









TMS1000 products give your products microcomputer performance. At the lowest possible cost.

TI's TMS1000 Family can give your products the benefits of microcomputer intelligence at a very low cost.

More than 60 million TMS1000 4-bit microcomputers are at work in many diverse applications — radios, home appliances, air conditioners, toys, clocks, microwave ovens, scales, POS terminals, smart thermometers and metering functions.

Enhance your product

With microcomputer intelligence, your product can respond or take action from a sensor or user input. A telephone that dials a preset number on command. A scale that weighs, then calculates the price. TMS1000-enhanced products are faster. More efficient. More accurate. More reliable. And more cost-effective.

Like your product, most TMS1000 applications must be highly reliable. TMS1000 has an attained failure rate of 0.048%/1000 hours, based on 5 years and millions of device-hours of operation. Also, using TMS1000 instead of standard logic greatly reduces system connections, a major source of malfunctions.

Two new TMS1000 Products. For timing. For sensor input.

The TMS1121 Universal Timer/Controller can control up to 4 independent functions with a total of 18 time settings.

The TMS2100 Microcomputer offers an 8-bit A/D converter plus timed programmable interrupts, ideal for many industrial and appliance applications.

Design Flexibility

The TMS1000 Family provides technology and output options to closely match your application. Choose CMOS for very low power applications, or PMOS. On-chip memory from 1K to 4K bytes of ROM, 128 to 512 bits of RAM. Standard or low (9V) voltage can be specified.

Development Support

Let TI develop and test software for your application, or develop your own using TI development boards, systems and software. Our Regional Technology Centers provide courses in software and hardware design as well as design support.

For more information on TMS1000 Family microcomputer solutions, send in the coupon or call your nearest TI sales office or authorized distributor.

TI Literature Response Center
P.O. Box 202129
Dallas, Texas 75220

Please tell me more about the advantages of the TMS1000 4-bit, single chip microcomputer family.

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PHONE N3

Texas Instruments invented the integrated circuit, microprocessor and microcomputer. Being first is our tradition.

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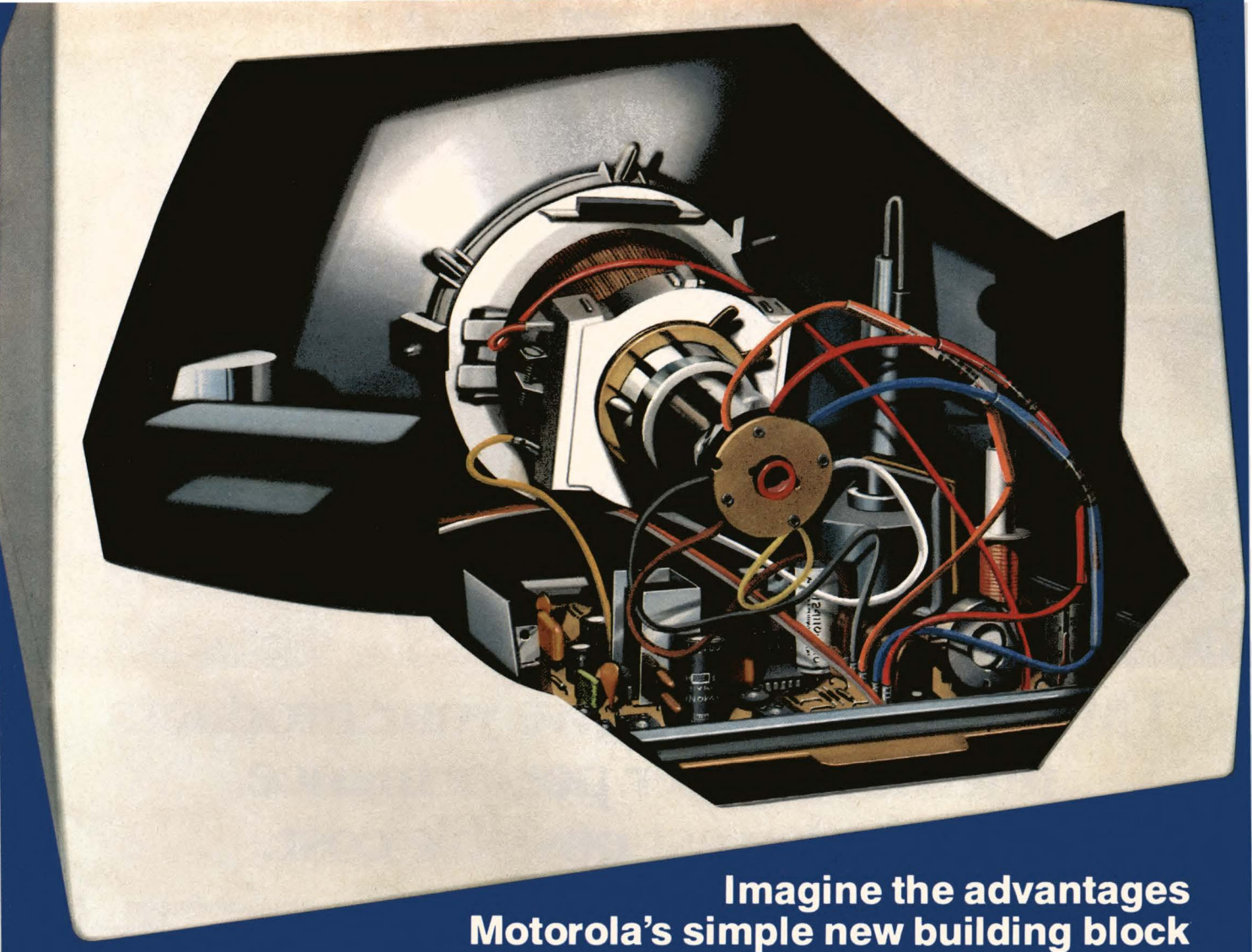


Imagine the advantages Motorola's simple new building block system will give your design engineers

Motorola's new Alpha Series is more than a new generation of 12″ and 15″ display modules. Its design, though remarkably simple, redefines the standards by which you will measure the performance of your terminals.

Greater reliability

On-going tests project a dramatic 75% increase in MTBF over even our own most reliable MD series.

Greater reliability is a result of synergistic elements at work at Motorola. Paramount is product design. The Alpha Series makes extremely efficient use of fewer components and incorporates integrated circuits throughout the system.

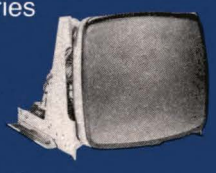
Advanced manufacturing processes and revolutionary testing equipment at Motorola's unique multi-million dollar facility in Joplin, MO, are designed to improve the quality and reliability of the Alpha Series.

Enhanced video performance

Motorola has extended resolution and bandwidth in the Alpha Series for sharper alphanumeric presentation. Center resolution has been increased from 1000 to 1200 lines; corners from 750 to 950 (P4 phosphor). Bandwidth has been stepped up from 22 MHz to 30 MHz (−3Db). Compare geometry and linearity specifications and you'll find that Motorola's Alpha Series ranks among the highest in the industry.

Design flexibility

Whether your requirements call for composite video, true TTL compatibility or direct drive, the versatile Alpha Series can handle a wide signal input variation. Horizontal scan rate is available at 15.7 or 18.7 kHz. The streamlined chassis of the new display allows you more flexibility in your mechanical design. Ease of access to the controls and unique options such as 24 vdc operation and 20 pin ribbon cable add to making the Alpha Series extremely adaptable display modules.



Motorola displays the character of your business.

MOTOROLA
Display Systems

1299 E. Algonquin Road Schaumburg, IL 60196
312/397-8000

CIRCLE NO 35

General-purpose computer joins three processors in small package

Combining three coprocessors—a 16-bit 68000 CPU, a second 68000 for virtual-memory management and a 6809 I/O processor—the 68K Miniframe general-purpose computer runs the Bell Labs UNIX operating system and operates at 12 MHz with no Wait states.

The 6809 interfaces to all I/O devices on an interrupt-driven basis and interacts with the CPU through a sophisticated high-speed DMA channel using cycle stealing. The 68000's DMA is daisy chained, with the 6809 having the highest priority.

The memory processor addresses as much as 4G bytes of RAM through a virtual-memory management unit (VMMU). This processor, which connects the CPU's address bus to a dynamic-RAM-array address bus, receives its control signals from the data bus. A modified least-recently-used page-replacement algorithm provides demand-paged virtual memory in 16M-byte increments.

Memory comes on dynamic-RAM boards that work with or without the VMMU. The boards connect to the CPU via a flat ribbon cable that terminates in dual-row 50-pin insulation-displacement connectors. You can configure the boards for as little as 128k bytes of RAM (using 16k×1 RAMs) or as much as 2M bytes (using 64k×1 RAMs).

Each byte of RAM has an associated parity bit that you can disable at the board level. An intelligent statistical-refresh method ensures refresh with maximum transparency.

A 4k×16 high-speed associative memory furnishes the page map, and it is accessible within the last 1M bytes of supervisor data-address space.

A powerful 16-bit general-purpose computer *in a small package, the 68K Miniframe supports multiple users with the Bell Labs UNIX operating system.*

Many things to many users

In multiuser and multitasking applications, the system maintains both relocation and limit registers for each user. Each version of the system works with either floppy or hard disks and provides six RS-232 ports (through six ACIAs) capable of 500k-baud transmission, plus four parallel ports (PIAs) consisting of eight bidirectional lines and two handshaking lines.

A single-user UNIX-based Miniframe starts at less than $12,000 and comes with 256k of RAM, 2M bytes of 8-in. floppy-disk storage and the complete UNIX v.7 package including FORTRAN-77, the C language, BASIC, and text-processor and file-processing utilities.

For multiuser systems, a typical configuration accommodates six or more users and comes with 512k bytes of RAM in a 16M-byte virtual space, 40M bytes of Winchester-disk storage and the UNIX package; it sells for less than $20,000.

MicroDaSys Inc, 2811 Wilshire Blvd, Santa Monica, CA 90403. Phone (213) 829-6781.

Circle No 458

YOU CAN USUALLY TELL WHEN THERE'S A NOISY POT IN THE CONTROL PANEL.

Cermet and molded carbon panel pots can have a very noisy way of attracting attention. So Bourns developed a quiet, smooth, durable alternative: Our Bourns® 91/92 family of ⅝" modular conductive plastic panel controls.

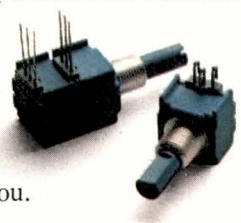
See for yourself by comparing the difference in CRV and rotational life.

MATERIAL	CRV (Noise)	ROTATIONAL LIFE
• Conductive Plastic	1% max.	2% max. CRV after 100K cycles. Useful life may go to 500K.
• Cermet	2% or higher	Typically less than 100K cycles.
• Molded Carbon	1½%	Not guaranteed after 100K cycles.

In addition, the price is competitive with the low cost of molded carbon for industrial applications. And much lower than cermet.

Terminals are in-line PC style on .100 inch centers. You can position them forward, back or down for vertical or horizontal board mounting. Choose from two bushing sizes, six tapers and three standard shaft lengths to ⅞". Resistance values from 250 ohms to 5 megohms.

It's a cost/performance combination worth making lots of noise about. So let your fully stocked local distributor hear from you.



Or call us for more information.
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BOURNS, INC., 1200 Columbia Avenue,
Riverside, CA 92507.
Phone: (714) 781-5747.
TWX: 910-332-1252.

In Europe: Bourns AG, Zugerstrasse 74,
6340 Baar, Switzerland. Phone: (042) 33-33-33.
Telex: 845-868722.

In Japan: Nippon-PMI Corporation,
Haratetsu Building, 4-11-11 Kudan Kita,
Chiyodaku, Tokyo 102, Japan. Phone: 234-1411.
Telex: 781-27632.

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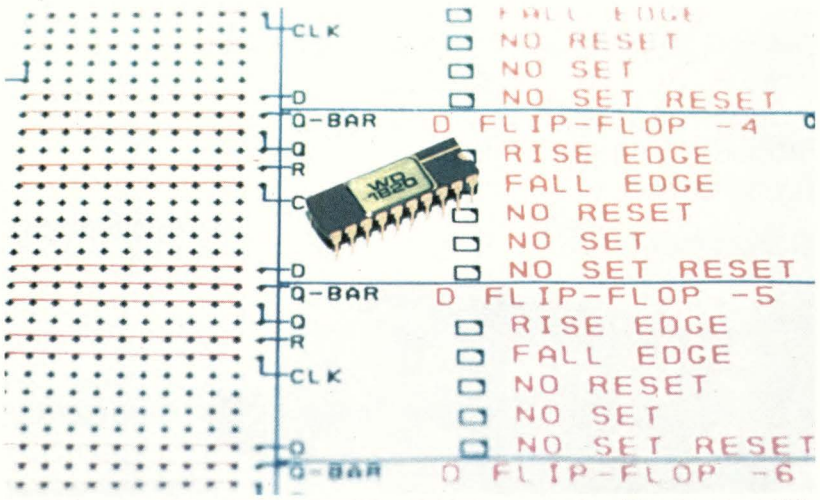
THERE IS NO EQUIVALENT.

CIRCLE NO 36

Mini-floppy-disk formatter/controller family offers full features at lower cost

Exhibiting all the features of their more expensive 179X relatives, 176X-family disk controllers are designed exclusively for mini-floppy use. All run at 1 MHz and are compatible with the 179X units, which handle 5¼- and 8-in. floppy drives.

The line consists of four parts: the 1761, -63, -65 and -67. They cover all combinations of single- and double-density, true- or inverted-data-bus and single- or double-sided drives. Single-density format is compatible with IBM's 3740; double density, with IBM's System/34. The parts can also use a non-IBM format for increased density.



Operating at 1 MHz, *176X-family 5¼-in.-mini-floppy controller chips are compatible with 179X-family controllers for 5¼- and 8-in. drives. But they cost less—$25.30 (100) in plastic.*

Designed for soft-sectored systems, the devices feature automatic track seek with verification, DMA or programmed data transfers from a double-buffered 8-bit bidirectional data bus and eight control lines for μP compatibility. Additionally, all inputs and outputs are TTL compatible, and as in the 179X family, two VFO signals are available.

The devices output write-precompensation signals, allow window extension and incorporate encoding, decoding and address-mark circuitry. In Read mode, they can either perform single- or multiple-sector read with automatic search or read the entire track. Likewise, they support single- or multiple-sector write with automatic sector search or can write the entire track for diskette formatting. They accept 11 commands and feature on-chip track and sector registers plus comprehensive status information.

The devices are available in 40-pin ceramic or plastic packages. Operating temperature spans 0 to 70°C, and power dissipation equals 600 mW max. Power-supply requirements stand at 5 and 12V. $25.30 in plastic, $36 (100) in ceramic.

Western Digital Corp, Box 2180, Newport Beach, CA 92663. Phone (714) 557-3550.
Circle No 459

NEXT TIME

EDN's September 30 issue will feature a Special Report on gate-array ICs, plus articles on a variety of additional topics:

- Optimizing flash A/D-converter operation through the use of track/hold amplifiers
- The theory and application of tone-decoder ICs
- The use of memory segmentation in Intel's iAPX 432 32-bit μP

. . . and much more. Also look for Technology Update pieces on solid-state relays and voltage regulators, plus our regular Design Ideas and A Question of Law departments. You can't afford to miss this issue!

EDN: Everything Designers Need

TESTING, TE

NOBODY CAN REDUCE YOUR COMPONENT

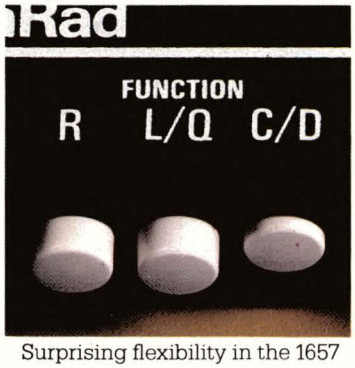
At GenRad, we have the most complete line of reasonably priced high performance products for component testing anywhere. And when you combine that fact with our experienced field service staff and expert applications engineers, it just stands to reason: nobody can reduce your component testing costs better than GenRad.

1688 Precision LC Digibridge

Testing passive components: we automated RLC testing with the Digibridge® tester.

What do you need in an RLC tester at any level of testing? Accurate performance, right? What you don't need is an inflated price.

That's why we give you four different Digibridge testers with four different performance levels in four different price ranges, beginning with our lowest priced 1657 Digibridge tester. The 1657 is the most accurate instrument you can buy for the money—with features even more expensive instruments don't have. Like 5-digit LED resolution. And a microprocessor for automatic ranging and self-calibration.



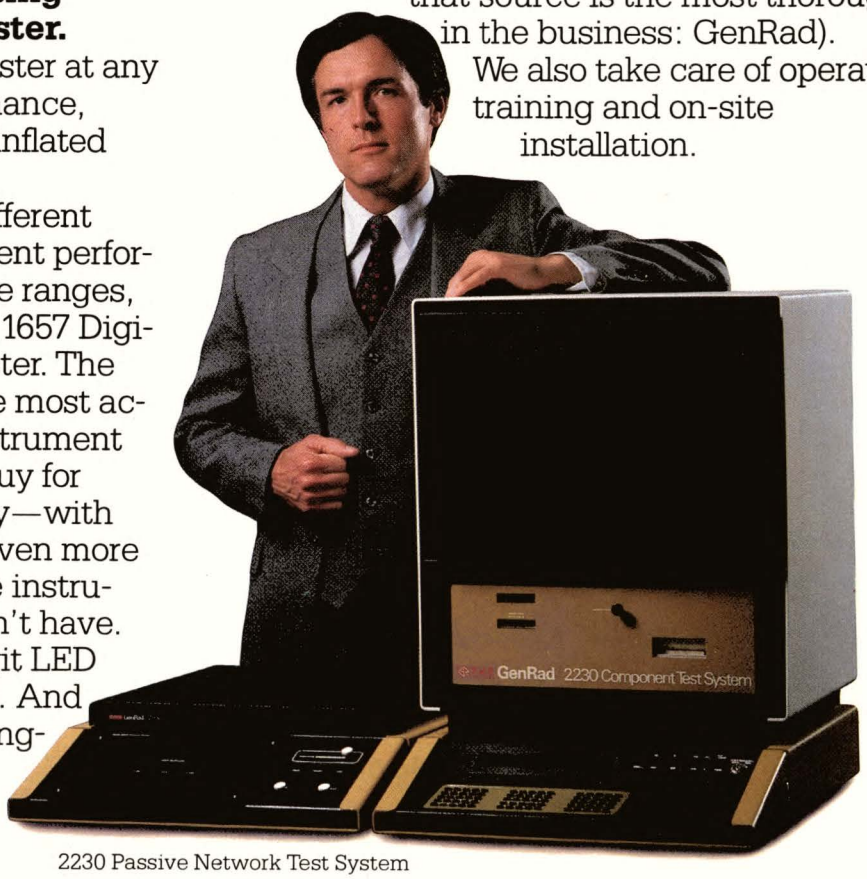
Surprising flexibility in the 1657

Now you know why nobody else comes close in numbers of RLC testers installed.

Testing RLC networks and small PC boards: our 2230 will get you on-line weeks sooner.

If you want to test packaged RLC networks, sequenced parts on reels, or even components on small PC boards, you have two choices: You can either do it with our 2230, or you can do it with a rack-and-stack system costing twice as much and lacking the necessary software. Of course, our 2230 will get you up and testing weeks sooner than a setup of unmatched units. And our 2230 is a complete system. Which means it needs service from only one source. (And that source is the most thorough in the business: GenRad). We also take care of operator training and on-site installation.

Plain-language keyboard speeds up programming



2230 Passive Network Test System

STING, TEST

TESTING COSTS BETTER THAN GENRAD.

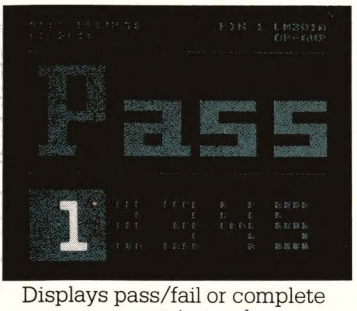
Testing ICs: our basic promise, immediate productivity, of course.

We pioneered automatic benchtop testing over a decade ago. And today more people own GenRad benchtop testers than any other brand.

The reason? Just look at our linear and digital IC systems. They're both built with the kind of architecture found only in much larger test systems. And our compact systems cost up to 75% less than the biggies.

Our productive 1731 linear IC tester.

It offers something nobody else can: immediate productivity. Thanks to a large and proven program library, covering over 1,000 different devices. The 1731 also has a built-in CRT and convenient and quick plug-in family boards for data convertors, voltage regulators and comparators, plus interfaces for all major handlers. Now you can understand why more people own a 1731 than any other low cost linear IC tester.



Displays pass/fail or complete parametric results

Our versatile 1732 digital test system.

Not surprisingly, last year more engineers bought our 1732 than any other microprocessor-based digital IC tester. One good reason? Because the 1732 can test SSI, MSI and LSI devices, up to 48 pins. A lot of engineers figure that's an insurance policy for the future. And they're right. In addition no other system is quite so easy to program or to use as the 1732, which lowers your operating costs. But then nobody understands test system software as well as we do.

Now, the ultimate test.

We're convinced we can reduce your component test costs better than anyone else today. And when it comes to products for the future, nobody is more committed to meeting your needs than we are. In fact, we're continually working on new, state-of-the-art systems to reduce your testing costs. After all, that's how we got to be the "Best in Test."

Now if you'll tell us more about your products and your component testing needs, we'll show you how you can reduce your cost to test.


1731 Linear IC System and 1732 Digital IC System

Call or write Frank Kelliher, GenRad, Inc. Component Test Division, 37 Great Road, Bolton, MA 01740. (617) 779-2811 Ext. 303.

Send to: GenRad Inc., 37 Great Road, Bolton, MA 01740
I want to know more about reducing my component testing costs.
Send details on: ____ Digibridge® Testers ____ 1731 Linear IC Test System ____ 1732 Digital IC Test System ____ 2230 Passive Network Test System
Name _____ Title _____
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THE BEST IN TEST.

Visit us at NepCon Central, Booth 232, September 22-24

CIRCLE NO 37

System-tailored VFC's ...to 10 MHZ

These VFC's meet the tougher requirements of newer instrumentation systems... providing true price/performance breakthroughs... through innovative circuitry.

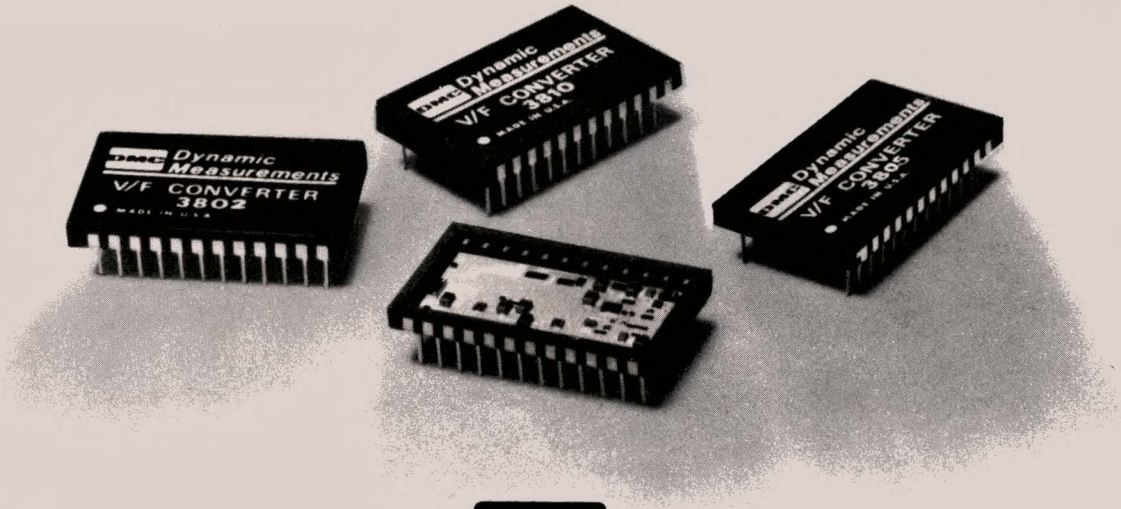
For instance, 1 MHz systems can be upgraded with minimal redesign to operate at 2 MHz... for two-fold improvement in resolution/sample performance... *at considerable cost saving.*

A family of 10, 5, and 2 MHz models is offered, with guaranteed non-linearities as low as ± 0.02% and gain temperature drifts as low as ± 15 PPM/°C.

These designs are available in both industrial and full military versions.

The performance hybrids

DMC... the acknowledged leader in voltage-to-frequency conversion... invites you to send for complete design data.



DMC

Dynamic Measurements Corp.

6 Lowell Ave., Winchester, MA 01890. (617) 729-7870. TWX (710) 348-6596

Call our toll free number 800-225-1151.

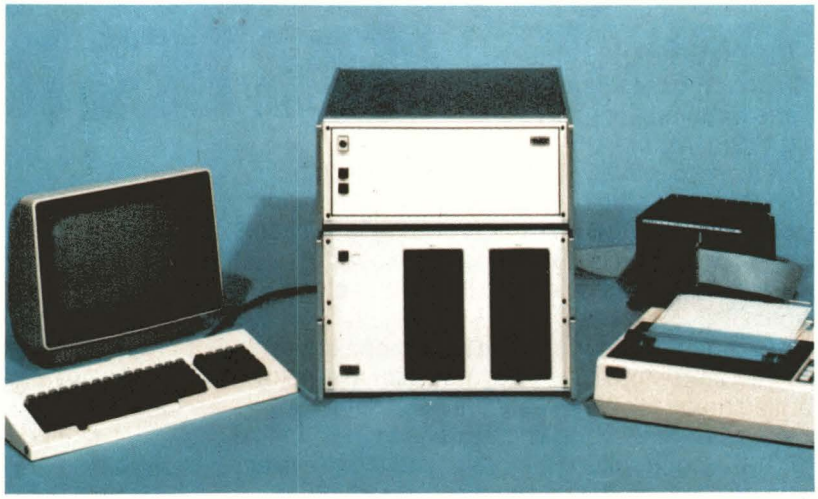
CIRCLE NO 38

Low-cost development system operates over STD bus

Providing a Z80 or 8085 CPU card that plugs into an STD Bus mainframe to simplify switching between devices, the Basis/80 development system costs less than $10,000. Yet it includes the memory, control and in-circuit-emulation features of more expensive systems.

Using the CP/M (Version 2.2) operating system from Digital Research Corp for disk-file management, the development system allows you to program in FORTRAN, BASIC, PASCAL or FORTH as well as assembly language. Development software includes a screen-oriented editor with menu-select options; the editor lets you examine 24 lines of code and make changes or additions by positioning the CRT's cursor and entering data.

The system handles devices other than Z80 and 8085 types by means of cross assemblers, which feature full macro capability, cross-reference map, algebraic-expression processor and link-file structures.



An STD Bus mainframe *packs the hardware you need to develop software on the Basis/80 for Z80 and 8085 μPs. Cross software handles 8080, 6502 and 680X devices.*

In-circuit emulation

Basis/80 includes in-bus-emulation capability for development of products designed around the STD Bus. An emulation card plugs into the target system in place of the system's CPU card, giving system control to the Basis/80.

Emulation allows you to debug hardware and software on the target system, which can address as many as 254 input and 254 output ports and 58k bytes of PROM or RAM without conflict with the emulator's workspace. Emulation features include real-time execution of program code with breakpoints set for the occurrence of either a particular input/output instruction or a memory reference to a single location within the target system. Additionally, program trace permits single-instruction execution and dumping of register contents to the CRT.

Symbolic debugging

You can also perform symbolic debugging of Z80 and 8085 programs. You download executable object files for the other supported microprocessors through an RS-232C port to either a PROM programmer or a target system for debugging.

The debugger allows you to set unlimited breakpoints and as many as eight passpoints, providing a means of monitoring program flow through code sections and examining register contents. Other single-key commands in the debugger provide for altering memory, examining registers, displaying memory contents, moving blocks of code and executing code.

Basis/80 hardware includes a Z80 or 8085 CPU, PROM bootstrap, 32k to 58k bytes of RAM and 499k bytes of disk storage on dual 8-in. drives. You also get a 15k-baud memory-mapped CRT controller providing a 25-line×80-character scrolling display, alphanumeric keyboard with cursor-control and numeric keypad and front-panel controls to reset or interrupt program execution and (via keylock) apply power to the mainframe.

$6110 to $8405; a typical system, consisting of mainframe, disk drives, terminal, 48k bytes of RAM and 132-column impact printer, costs $7495.

Antona Corp, 13600 Ventura Blvd, Sherman Oaks, CA 91423. Phone (213) 986-6651.
Circle No 460

DILOG TAPE COUPLERS FOR STREAMING OR FORMATTED DRIVES FOR DEC 11*

The DILOG DQ130 and DU130 are μP based intelligent ½" Tape Couplers for your LSI-11, 11/2, 11/23 or PDP-11 computers respectively. They're the only Couplers • for standard start-stop or streaming mode operation • capable of handling 8 drives • proven reliability and performance with an installed base *in excess of 1,000 units* • all on a single quad board that plugs into your CPU.

If you intend using your streaming tape drive in a standard start-stop mode and later wish to employ streaming mode for Winchester back-up, DILOG Couplers will handle both. You don't need to change a thing. The Dilog 'Backup/Restore' stand-alone driver software will implement and support streaming operation.

The '130' Series can also accommodate two standard ½" formatted tape drives with three slaves each, or two stand-alone formatters that handle four drives each... 9-track 800 bpi NRZI, 9-track 1600 bpi PE, or 800-1600 bpi dual density... with 7", 8½" or 10½" reels and read/write speeds from 12.5 to 125 ips and data transfer rates to 200,000 bytes per second.

The Couplers emulate the DEC TM-11/TS-03 and you'll get full software compatibility with RT-11, RSX-11, RSTS, IAS and MUMPS.

As for tape drive compatibility, both the DQ130 and DU130 interface drives from the following manufacturers:

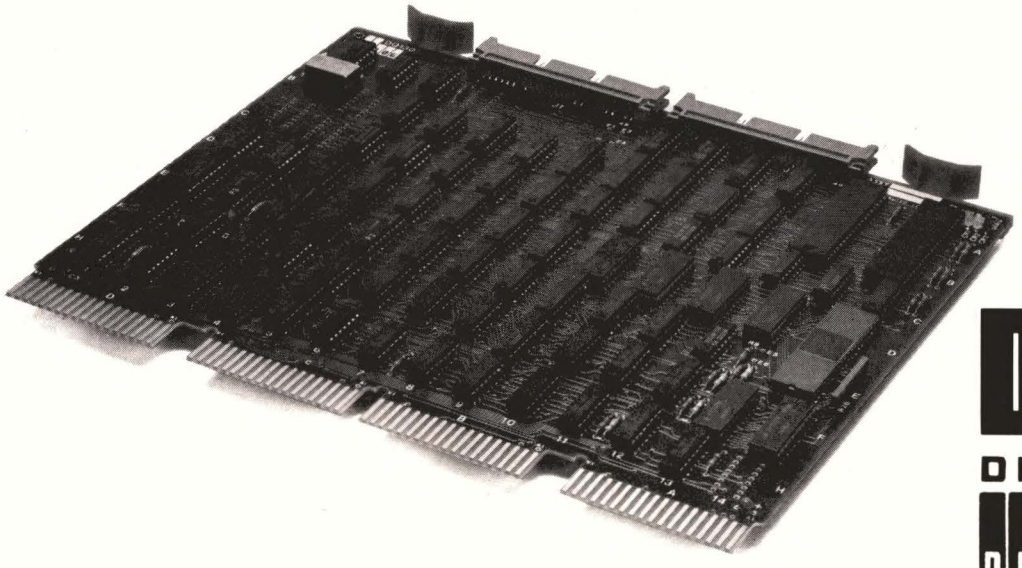
AMPEX	PERTEC
CIPHER	TANDBERG DATA (IDT)
CONTROL DATA	WANGCO (PERKIN ELMER)
DIGI-DATA	TDX
KENNEDY	EMI (SE LABS)

To insure ease of maintainability & data integrity the Couplers incorporate an automatic self-test feature, with card-edge LED status indicator, and data protect feature.

Write or call for complete details on the Coupler that lets you mix or match up to eight ½" tape drives for standard or "streaming" operation.

Distributed Logic Corp., 12800 Garden Grove Blvd., Garden Grove, California 92643 Phone: (714) 534-8950 Telex: 681 399 DILOG GGVE • EASTERN REGIONAL SALES OFFICE, 64-A White Street, Red Bank, New Jersey 07701, Phone: (201) 530-0044.

*Trademark Digital Equipment Corp.



VISIT DILOG AT SYSTEMS '81' BOOTH 57 HALL 2 U.S. SECTOR

DILOG

DISTRIBUTED LOGIC CORP.

DILOG

NUMBER 1 FOR DEC-11

CIRCLE NO 39

Development system for Z80, 3870 operates from time-shared host

For use with a host computer (including time-shared units), the Radiμs development system provides software-development capability via that host plus hardware development and hardware/software integration via in-circuit-emulation modules. It supports Z80s and 3870s.

You install the $2995 Radiμs (Remote Access Development and Integration Microcomputer System) between a CRT terminal and the host via RS-232 serial interfaces. While software development is performed on the host as usual, you can download programs to Radiμs for hardware debugging and software integration, using optional E Series AIM in-circuit-emulation modules.

In Transparent mode, the CRT has its usual access to the host. In Local mode, Radiμs can perform self diagnostics and be set for any of 11 baud rates from 50 to 9600. You can also set control characters in this mode.

In Utility mode, Radiμs can run utility programs for such tasks as in-circuit emulation, printer handling and PROM programming. Debugging and integration routines are also available in this mode.

Once AIM and user programs are downloaded to Radiμs, you can disconnect the host, saving time-sharing costs. However, the host's file-management utilities are then not available.

You can configure Radiμs for single or multiple-user environments and connect several AIM units to one host for simultaneous operation. This mode also allows you to perform separate or multiprocessor tasks.

Tied to your time-sharing or other host computer, *the Radiμs development system aids in the design of Z80- or 3870-based hardware and its integration with software.*

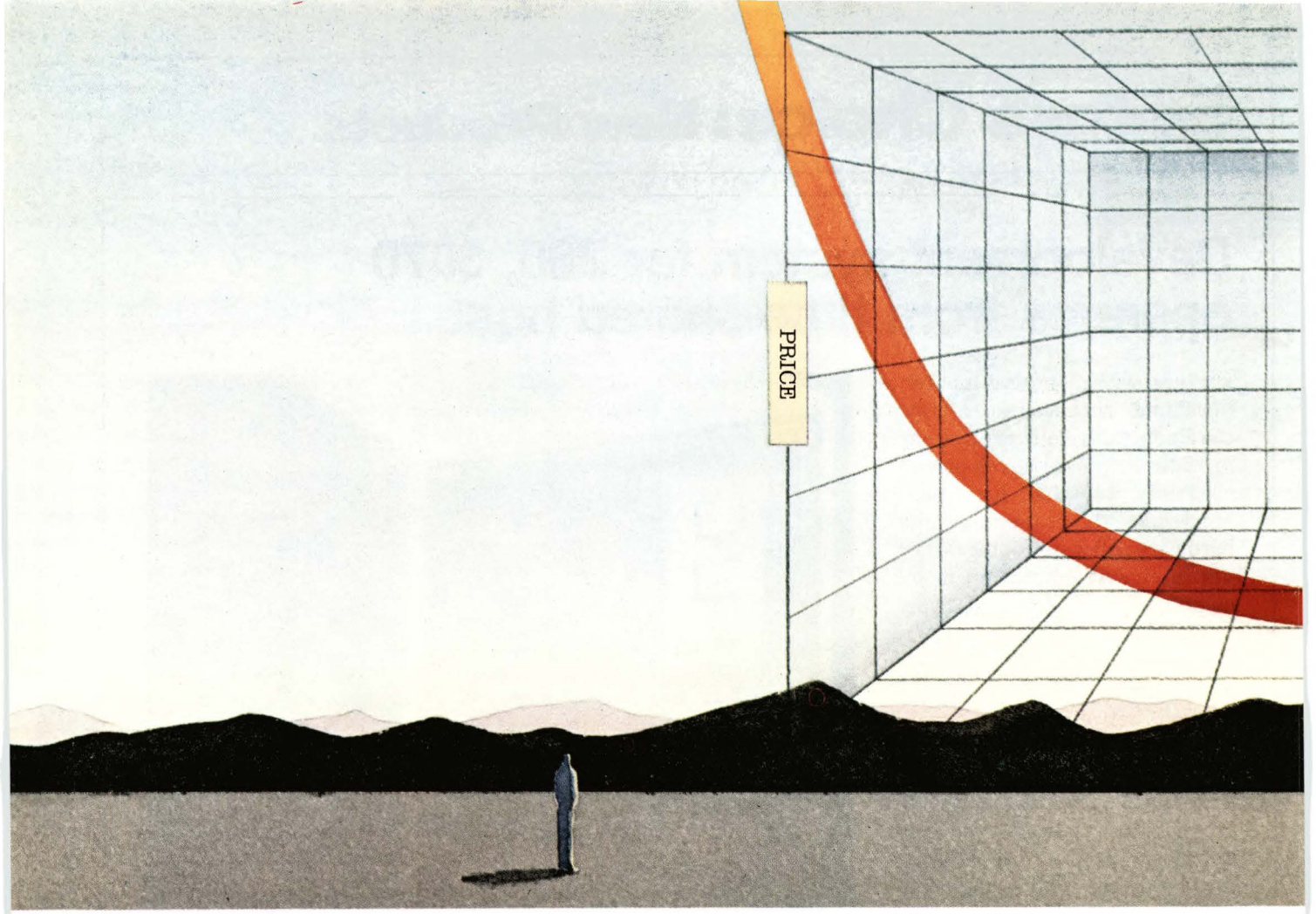
Radiμs comes with a host communications-software package for DEC PDP-11 computers working under the RSX-11M operating system (Version 2.3 or later) or on DEC VAX-11 systems working under VMS (Version 2.3 or later).

Hardware includes a structural-foam cabinet, CPU/memory board and power supply. AIM-Z80BE, AIM-7XE or future AIM modules, local PROM programming and local printing are optional. The cabinet's processing compartment houses as many as five boards: the CPU/memory board, two AIM-module boards and two expansion slots.

The CPU/memory board includes a Z80 CPU, 64k bytes of RAM and four serial I/O ports: one dedicated to the user terminal, one to the host and two for the optional printer and PROM programmer.

A translator is available to convert Tektronix 3870 and Intel hexadecimal object formats to absolute-binary form.

Mostek Corp, Box 169, Carrollton, TX 75006. Phone (214) 323-6000. **Circle No 461**



How to break the 8· without

It's not as hard as you think. Forget complex designs. And two-year waits.

All you do is get your hands on the Intel 8088.

And then leave the other 8-bit systems standing in your tracks. Without breaking the bank.

Because the 8088 gives you two to five times the performance of other 8-bit processors. For a whole lot less.

In fact, at $14.10 for 100 pieces, 75% less than last year. (Because high volume shipments are already pushing the 8088 down a super fast price curve.)

And about 20% less than you'd pay for a Z80 or MC6809 system.

For some simple reasons.

The 8088 runs at full speed with slower speed memories than you need for other 8-bit microprocessors.

And about 1/3 less memory at that. Thanks to its powerful instruction set that helps you reduce the size of assembly language programs.

Which together with the 8088's library of high level software (Pascal, CP/M, Basic and Fortran) should help you cut the other part of system costs. The part that's larger than hardware.

But even though you're paying less, you'll be getting more.

Like 1-megabyte addressing.

Extra power for 16-bit number crunching.

And faster string processing.

Fact is, our recent benchmarks show the 8088 runs circles around a Z80A, Z80B or MC6809 when it comes to terminal and small business applications.

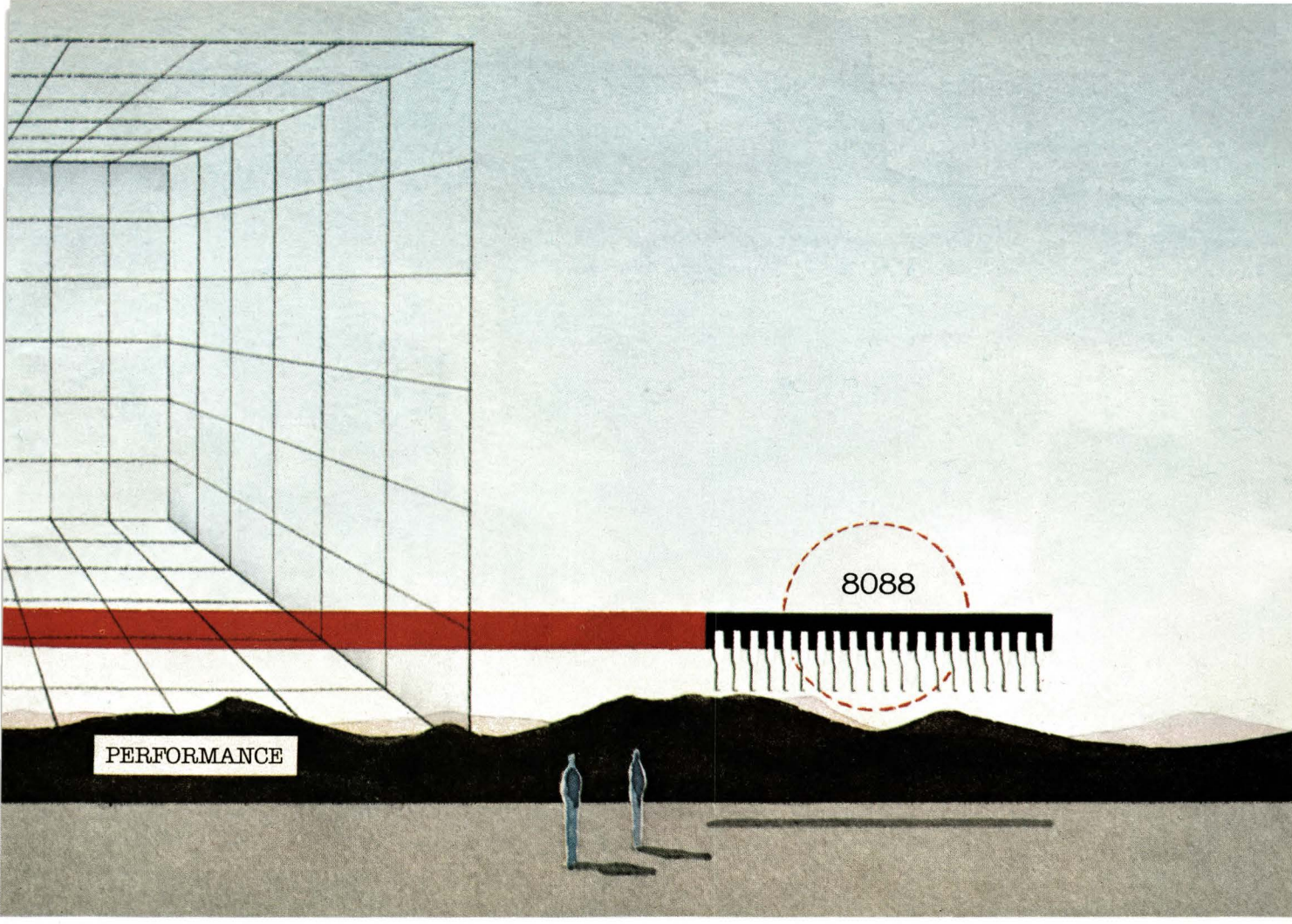
But don't think you have to stop there. With any of our iAPX 88 multiprocessor configurations, you can give performance an added boost—and still keep the cost and simplicity of an 8-bit system.

For 100 times the throughput on number crunching, just choose the iAPX 88/20 system.

Relative Performance

	Intel 8088 (5 MHz)	*Zilog Z80B (6 MHz)*	*Motorola MC6809 (2MHz)*
Computer Graphics	*1.0*	*0.1*	*0.05*
16-bit Multiply	*1.0*	*0.17*	*0.5*
Block Move	*1.0*	*0.75*	*0.49*

Full details of these benchmarks available in the iAPX 88 Book.



bit performance barrier going broke.

It combines the power of the 8088 with our 8087 numeric coprocessor.

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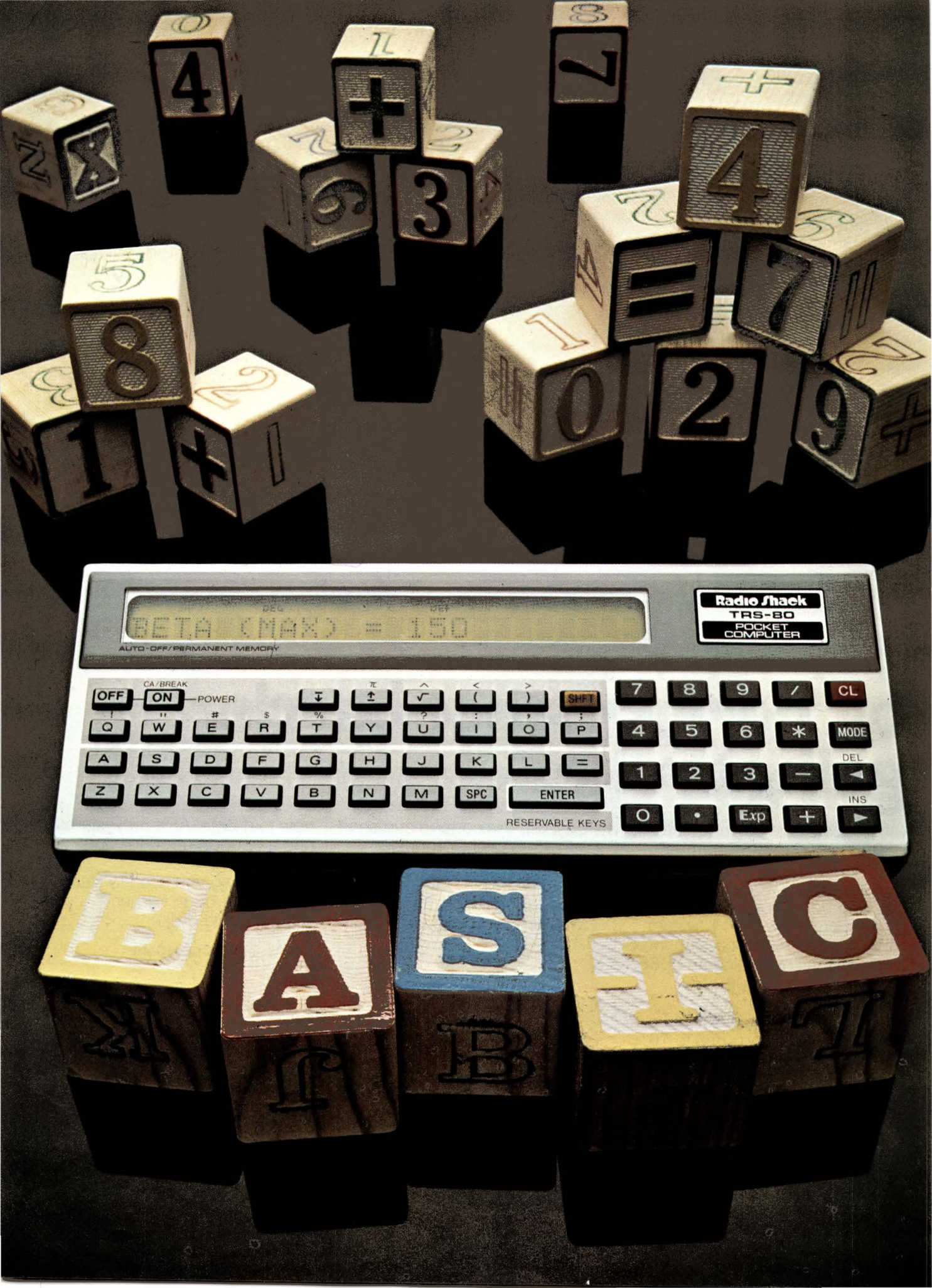
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Personal Scientific Calculators

Alphanumeric displays and keyboards and high-level-language programming combine in the newest hand-held machines.

Jim McDermott, Special Features Editor

Highlighting personal programmable scientific calculators this year is the emergence of a new generation of hand-held machines featuring extended horizontal alphanumeric displays and full-alphanumeric keyboards. Additionally, these calculators (some call them computers) are programmed not in the efficient machine language associated with standard scientific calculators, but in high-level BASIC.

Offered by Radio Shack, Sharp, Casio, Panasonic and Quasar, the horizontally stretched machines feature dot-matrix LCD screens that display 20 to 24 characters. Furthermore, such alphanumeric displays are also appearing in new lower priced scientific programmables with 11- or 13-character readouts.

Most familiar of the BASIC machines is the Radio Shack $230 TRS-80 Pocket Computer, which has been available for some time. Sharp, which manufactures the machine for Radio Shack, introduced it recently under its own label as the PC-1211 Pocket Computer. The dot-matrix display on both of these devices is remarkably like that of Sharp's EL-5100 (introduced in mid-1979), the first scientific programmable calculator into which a user could write alphanumeric formulas without first translating them into machine language (EDN, June 20, 1979, pg 97). The -5100's display also prompts the user during program runs. (Actually, the

Alphanumeric capabilities and BASIC programming *characterize programmable pocket computers. (Photo courtesy Radio Shack)*

Keyboard configurations vary; units aim at typewriter ease

-5100 is only pseudoprogrammable: It can't handle independent subroutines or loops.)

Although the EL-5100 and Pocket Computer displays can present 24 characters at a time, their display register holds up to 80. As you enter more than 24 characters, the display scrolls off screen to the left to provide space for the new input. You can recall all characters, however, whenever needed. And when you're using angle and operational modes (Deg, Rad, Grad, Run, Pro, Reserve and Def), they are flagged by small segmented LCD characters at the top of the main matrix display.

Other new hand-held computers have similar display characteristics. Casio's FX-702P Programmable Calculator displays as many as 20 alphanumeric characters, while the HHC (Hand Held Computer) from both Panasonic and Quasar shows a maximum of 26. (The HHC is marketed by both companies under their own brand names.)

Keyboard configurations in the new machines show more variety than the displays. The alphanumeric keyboards of the Radio Shack/Quasar units are laid out in typewriter-keyboard format, for example. No doubt the original idea was to pattern these keyboards after those of desktop computers, but the space allocated is

Calculators handicap horse races

Statistical analysis is traditionally boring, even if you're using a powerful statistical machine such as the Casio FX-702P. But four other statistical programmable calculators on the market guarantee to keep you wide awake—they're all programmed to handicap thoroughbred horseracing. The four are Mattel's $125 Horse Race Analyzer, APF's $100 Kel-Co Horse Racing Computer and Leisure Time Development's $50 Starshine Race Track Computers II and III (the latter for international handicapping).

If you're a programmable-calculator buff, you'll be very enthusiastic about Mattel's sophisticated machine. It's the Hewlett-Packard HP-41-equivalent in its class, providing 20 data-input keys and requiring 31 entries for each horse in a race. As you input each factor, the calculator's elaborate LCD prompts you to enter the next one in sequence. To obtain a sufficient statistical base, Mattel advises using it only for races in which at least 60% of the 3-yr-old (or older) horses have at least five races in their past performances listed in the handicapper's equivalent of EDN, the *Daily Racing Form.*

Statistics called for on the Mattel Analyzer for each horse include purse, race, distance, post position, days since last race, races run since a 30-day (or more) rest, current and previous years' performances (number of races, wins, places, shows and earnings), data on performance in the last three races and the two best speed ratings. Once you enter all this information, you press NEXT and repeat the process until you've completed it for all horses in a race. Then you press ANALYZE, and the display shows five numbers: the first two are post positions; the last three, rating numbers for the top horse. You record these numbers and repeat the procedure three more times until you've collected the five numbers for the second-, third- and fourth-rated horses.

At this point you're on your own. If the computer ratings for the top four horses are widely separated,

A sophisticated programmable machine *requiring 31 inputs for each horse in a race, the Mattel Horse Race Analyzer includes an elaborate LCD that prompts the handicapper with the name of his next required entry.*

The simplest handicapping computer, *from Leisure Time Development, requires only four entries to provide a rating.*

so compressed that you can't use them with both hands like a desk machine. It's also confusing to pick out an alphabetic sequence in a word when you "hunt and peck." And unfortunately, BASIC requires considerable amounts of word entry. Casio, on the other hand, lays its keyboard out in a 5-row A-to-Z sequence, making it easier to pick out individual letters.

Peripherals add capability

All of the newer machines provide optional peripherals. The Radio Shack and Sharp Pocket Computers, for example, furnish a $150 11×3.5-in. printer/cassette interface in which the calculators mount. The interface serves two functions: to provide an on-board printer and to allow the machine to interface with a cassette recorder for data storage and retrieval.

The printer produces as many as 16 columns per line on small standard paper rolls. The special set of adapter cables supplied with the interface connects it to the recorder. Radio Shack recommends its CTR-80A recorder for automatic program control and transfer of information because other units might not interface properly with the cables.

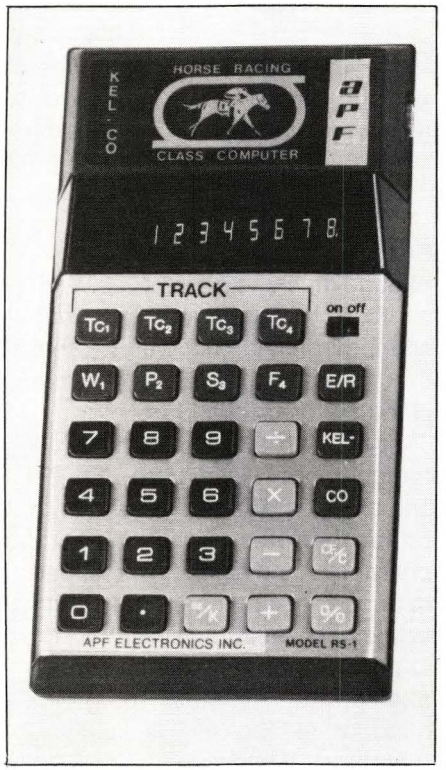
Casio's $200 FX-702P also allows you to store and retrieve programs on tape and provide printer output. For those functions, you need the optional $50 FA-2 adapter and the $90 FP-10 miniprinter (available next month). The FA-2 is not compatible with the firm's FA-1 adapter, which is used interchangeably with the older -502P and the new lower cost -602P.

the selection seems obvious, but when they're close together, you must input other factors (discussed in Mattel's instruction book) in the *Daily Racing Form.*

Mattel claims that in a sample of 500 races, the computer's top-rated horse finished first, second or third some 57% of the time. However, a limitation of the product is the time required to make all entries: For a 10-horse race, you must enter 310 inputs.

To speed up selection, try a calculator such as APF's Horse Racing Computer. The programming in this machine is adopted from a slide rule (the Kel-Co Class Calculator) first marketed in 1969. Running on a custom version of a Texas Instruments TMS 1100 μP, the APF machine's program is based on the "principle of established class ratings" for thoroughbred racehorses. It assumes that a thoroughbred class is best measured by the size of the purses for which a horse has successfully competed in the recent past. The calculator determines a horse's class rating as a function of the track on which the horse is running and its finish positions and earnings (taken from past-performance charts in the *Racing Form).*

The unit has four track keys (T_{c1}-T_{c4}) and four finish-position keys (1st, 2nd, 3rd, 4th). Only 12 or 13 entries are required for each horse to obtain an E/R (earnings rating). Specifically, a horse entered in a race with a lower purse value than called for by its established class rating is a strong potential bet. On the other hand, a horse with a lower class rating than the purse size would indicate it is seldom a serious contender.



Requiring six data inputs *for each horse in a race, this APF Electronics machine computes established class ratings—a statistically proven handicapping method.*

The simplest handicapping calculator, the Race Track II, picks winners by calculating a horse's median average. Specifically, it requires that you input (from the *Daily Racing Form*) two median ratings from the results of the horse's last three races: the speed rating and the horse's position at the finish. Then you need only two more inputs: the jockey's weight and the specific speed rating of the horse's last race. Only four data-entry keys are required: MSR (median speed rating), RC (race weight carried in today's race); LSR (speed rating for the last race run) and PAF (median position at finish). Pressing an RSMR key then gives the horse's rating, which you can compare with those of others in the race.

This 5-step procedure is fast and simple, and according to a testing-laboratory report, one of the three highest rated horses (in a 100-race sample) finished first 55% of the time, or first, second or third 95% of the time. The highest rated horse finished first only 20% of the time.

How do the pros view these computers? Says Tom Flanagan, author of *Beat the Races* (Arco Publishing): "Studying the [*Daily Racing Form]* ... gives the opportunity to apply [your] mind to something really worthwhile, because predicting the winner of a horse race is an intellectual inquiry of amazing depth and difficulty. Nowadays the PhDs and the mathematicians, armed with computers, are studying the racing game, but they'll find out that it isn't as easy as making an atom bomb."

Some units furnish extensive peripheral support

When it comes to peripherals, though, Panasonic's RL-H1000 HHC represents the most ambitious system-development program. Originally announced more than a year ago, it is now scheduled for delivery near the end of this year.

Panasonic has embarked on an extensive program of providing support peripherals, the basic philosophy behind the RL-H1000 being to provide a portable business computer with the power of a desktop system. And although packaged in an attache case, the RL-H1000 is not intended to be a low-cost system: The HHC machine itself costs about $600, but when it's configured with a full set of peripherals its price jumps to about $2500.

Even though the H1000's architecture is oriented primarily toward business users, the machine can be adapted for scientific or engineering applications with plug-in software modules. These 24-pin ICs plug into the H1000 main unit (it holds three) and add such specialized features as BASIC and/or scientific/engineering number crunching. Panasonic plans to offer approximately 12 of these specialized-application capsules within several months.

As you might have guessed, the H1000's generic operating system is not written in BASIC. Rather, it uses a language named SNAP, a derivative of FORTH. (A detailed description of the language and machine architecture appears in *Byte* magazine, January 1981). The firm chose SNAP because the language achieves a 2:1 data-compression advantage over assembly language; thus, it's fast running. Another factor in the language's favor: It permits the machine to mate easily with a wide variety of peripherals. Panasonic proposes to offer

- An acoustic telephone modem for full- or half-duplex communication via public telephone lines, spec'd at 110 or 300 bps and using asynchronous bit streams. Data is five to eight bits wide (selectable) and available with or without a parity

A software club for pocket computers

Publications of independent calculator-software clubs such as the PPC Club in Santa Ana, CA (for years publisher of a monthly *PPC Calculator Journal* devoted to Hewlett-Packard machines) and the TI Programmable Calculator Club (regular producer of *TI PPC Notes*), are now joined by the *Pocket Computer Newsletter* (Seymour, CT). Appearing 10 times a year, this newsletter chronicles developments and provides program listings and commentary from subscribers. Although previous issues have given extensive coverage to the Radio Shack/Sharp Pocket Computers, the publication will also be passing on tips on the Panasonic/Quasar HHCs and Casio FX-702P.

All the publications contain a prodigious amount of valuable information. Members of the PPC Club and the TI Programmable Calculator Club, for example, have produced and exchanged valuable software not available from the calculator manufacturers.

Richard Nelson, founder of the PPC Club, reports that synthetic-programming efforts by members with HP-41C/CVs continues to expand machine capabilities. With synthetic programming you discover surprising new features that the designers of the original machine never dreamed of.

For example, one HP-club member has discovered that he can produce 83 display characters rather than the 59 alphanumeric characters and symbols described in the owner's manual. And another member, astrophysicist William C Wickes, has produced a superb example of synthetic programming. When the -41C is digesting a problem, it lets its user know it's alive by propelling a cartoon "goose" from left to right across its display. Wickes has not only gotten a goose to face backwards, but also fly backwards, shed droppings, flap its wings, stream by in flocks of as many as nine and even collide head on with its factory-hatched predecessor. (Wickes is now an HP employee.)

Other pending software-club developments include 4k and 8k EPROMs that will complement the HP-41C/CV's 64k-ROM addressing capability. And another project, initiated in August 1979 and now about to reach fruition, is the development of a programmer's ROM that contains 153 short, efficient routines that you can call up in writing programs. Some 5000 of these ROMs, produced in collaboration with HP, have just become available to the members. The user's manual documenting the routines is 500 pgs long. For more information, contact Nelson.

Maurice Swinnen, who runs the TI Programmable Calculator Club, reports that members have discovered a Fast mode for the TI 59. In this mode, program execution occurs without calling the program into the display register. Bypassing this C register increases speed by a factor of two. However, the price you pay is that everything must be directly addressed; you can't use labels.

Another new discovery submitted to the TI club from an overseas member is an expanded Graphics mode that allows you to address all of the individual dots of the thermal-printer dot matrices. Use of this graphic programming provides control of some 300 character and symbol variations. For information, contact Swinnen.

check. The 5V power required comes from the HHC mainframe.

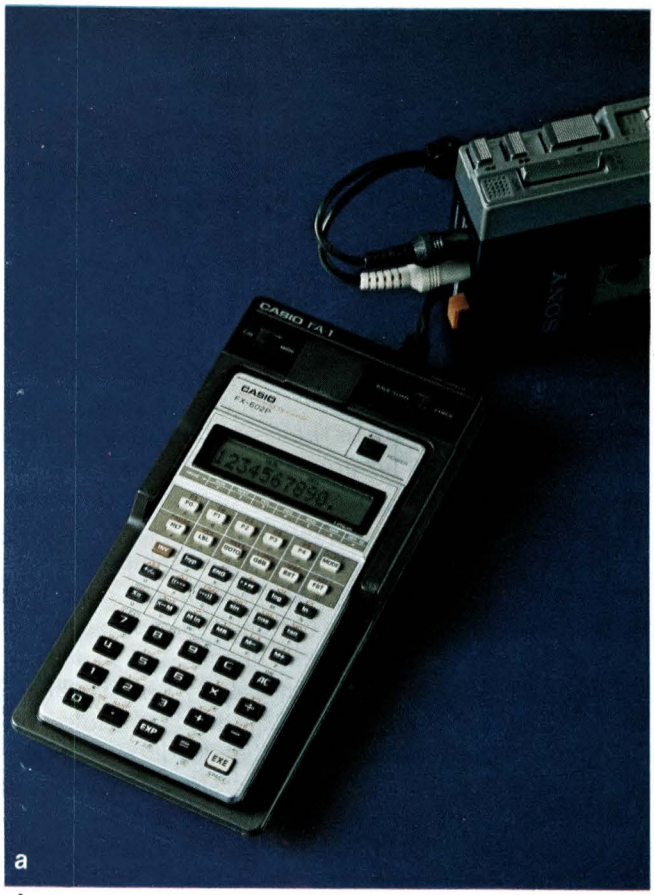
- A programmable CMOS memory protected by an internal battery backup. It has a standard capacity of 4k bytes and is expandable to 8k.
- A capsule-extender interface that allows you to connect four ROM capsules in addition to those already in the HHC. Each capsule can provide as many as 128k bits.
- A 5×8 dot-matrix thermal microprinter with a 16-character column width.
- An RS-232C serial interface using 5- to 8-bit asynchronous data and ASCII. Data-transfer rates are standard, ranging from 110 to 9600 bps.
- An I/O-driver unit that allows you to connect as many as six peripheral units through a 44-pin edge connector in the HHC main unit. (You can connect only one without the I/O adapter.)
- A cassette adapter that allows you to attach two recorders spec'ing transfer rates of 1200 bps.
- A TV adapter, termed a video RAM, that interfaces with a color TV—either indirectly through an RF terminal or directly to the video signal. With it you can display 16 lines of 32 alphanumeric characters using a 5×7-dot matrix. Other graphic display modes are also available.

Despite the HHC's extensive capabilities, though, its intrinsic calculating capability comes from a simple 4-function calculator with only percent and memory features. But for mathematical applications, an 8k capsule that converts the machine to Microsoft-BASIC operation will be available. It will provide all the trigonometric and scientific functions that BASIC offers. (The Microsoft BASIC in the HHC is a full BASIC language equal in power to that of the Apple II, Panasonic says.)

Back to BASICs

Simpler in scope than that of the Panasonic machine, the Radio Shack and Sharp Pocket Computers' BASIC capitalizes on the machines' use of an on-board calculator chip as well as a processing chip. With these chips, the machines can provide trigonometric functions and their inverses; natural and common logs; natural antilogs; square roots; decimal-to-degree/minute/second conversion (and its inverse); and integer, signum and absolute-value functions—all keyboard accessible in BASIC.

Interestingly, the Integer function in these machines converts a displayed positive nonintegral value to the next lowest integer, which is what you'd expect. However, for negative numbers you'll be surprised to find that unlike the case with most other standard personal scientific calculators, taking the integer function of −2.45 produces −3 rather than −2. In the same vein, you can raise a number to a power with simple BASIC commands, but you can't take the yth root of x without using a special subroutine. Close examination shows that Radio Shack and Sharp have sacrificed several other functions included on most powerful



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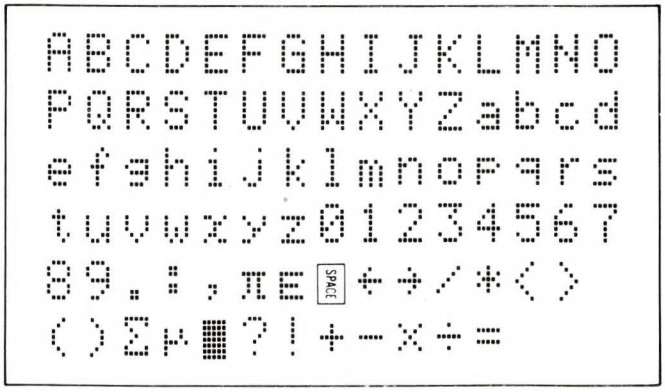
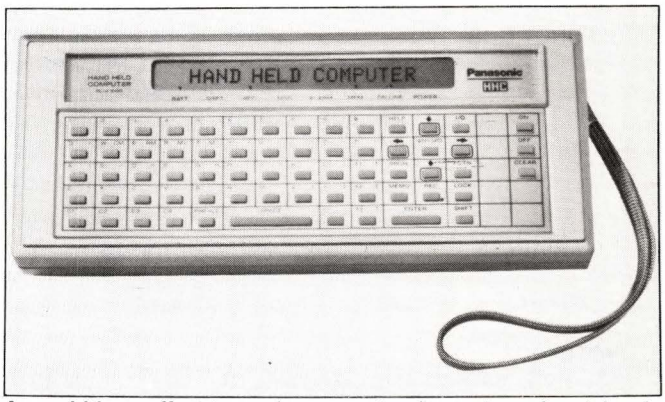


A full-alphanumeric dot-matrix display capability *is designed into the Casio FX-602P* ***(a).*** *Both upper- and lower-case characters are available in its set of 86 keyboard-accessible letters, numbers and symbols* ***(b),*** *which get displayed 11 characters at a time.*



An ambitious effort *to produce an extensive system of peripherals and a capable hand-held computer, Panasonic's RL-H1000 is aimed at business use.*

scientific machines in favor of the convenience of BASIC (see **box,** 'Who needs BASIC?').

Swap program steps for data storage

An interesting feature of the Radio Shack/Sharp Pocket Computers is a variable program memory of 1424 steps max and a fixed data memory of 26 registers (A to Z). A 16-stage function stack and an 8-stage data stack, both transparent to the user, temporarily store instructions and data for processing. However, you can call upon unused program memory to store data; hence, the memory is designated "flexible."

These machines also provide a very useful feature in their ability to tell, at any time and in any operating mode, exactly how many program steps and registers are available for data storage. When you key in a MEM command and then press the Enter key, XXXX STEPS YYY MEMORIES appears in the display. (However, the readout does not include the 26 data registers (seven characters per register) that store sequences of characters, including letters, blanks, numbers and special symbols. This MEM ENTER command works in all four of the machines' operational modes: Pro (program), Run, Def (definable) and Reserve.

Pro and Run are typical operational modes used for writing and running programs. Def and Reserve, on the other hand, exhibit powerful new features. One is the ability to assign just one key for a function or for an entire program that you use frequently.

Eighteen keys (A, S, D, F, G, H, J, K, L, =, Z, X, C, V, B, N, M, SPC) can be reserved for a particular function (or program), and once reserved, they are available for both manual calculations and programs. Forty-eight program steps are allocated for the reservable keys, and if the contents of the key allocations exceed 49 steps, the machine signals an error. You can readily check the assigned keys by reviewing them in Reserve mode. You can also assign programs to any of the 18 keys in Pro mode and execute them in Def mode.

The Panasonic/Quasar machines' programmable-key capability is less extensive than that of the Radio Shack/Sharp calculators. The HHC machines are limited to three special assignment keys (f1, f2 and f3) that you can allocate to any sequence of keystrokes, including most function keys. Pressing one of these keys produces the sequence of operations assigned to it. The keys find use in SNAP and BASIC programs.

Debugging made easy

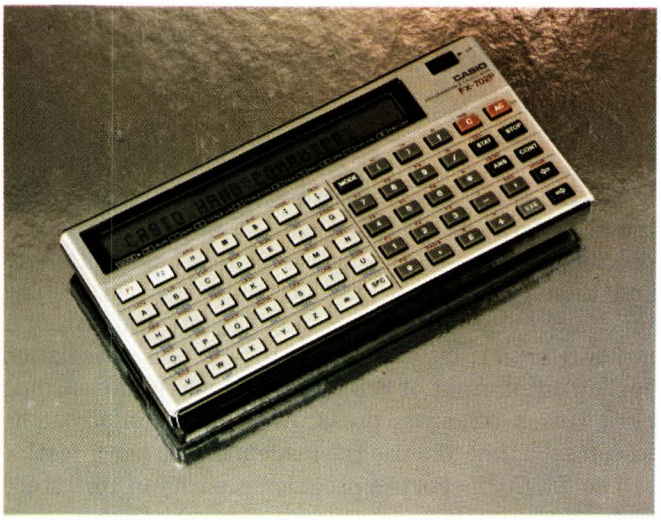
The Radio Shack/Sharp machines use a DEBUG command in Run mode and a LIST command in Pro mode, along with the Step Forward (↓) and Step Backward (↑) keys, for program debugging and

COMPARISON OF BASIC-LANGUAGE FEATURES

FEATURES	RADIO SHACK/SHARP POCKET COMPUTERS	CASIO FX-702P
COMMANDS/STATEMENTS	RUN, NEW, MEM, LIST, CONT, CLEAR, INPUT, PRINT, PAUSE, USING, LET, STOP, REM, BEEP, FOR, TO, STEP, NEXT, GOTO, GOSUB, RETURN, IF, THEN, AHEAD	RUN, VAC, LIST, DEFM, INP, PRT, WAIT, FOR, TO, STEP, NEXT, IF, THEN, GOTO, GSB, RET, SET, STOP, END, PASS, LIST V, LIST ALL, CLR, CLR ALL, DEL, LEN, MID
CASSETTE CONTROL	CSAVE, CLOAD, CLOAD?, PRINT#, INPUT#, CHAIN	SAVE, SAVE ALL, LOAD, LOAD ALL, PUT, GET, VER
OPERATIONS	+, −, *, /, ( ), >, <, >=, <>=, =	+, −, *, /, ( ), <, >, ≤, ≥, ≠, =
FUNCTIONS	SIN, COS, TAN, ASN, ACS, ATN, EXP, LN, LOG, INT, ABS, √, DEG, DMS, SGN, DEGREE, RADIAN, GRAD, π, ^, %	SIN, COS, TAN, ASN, ACS, ATN, HSN, HCS, HTN, AHS, AHC, AHT, EXP, LN, LOG INT, FRAC, ABS, SQR, RND(, DEG(, DMS, SGN, RPC, PRC, RAN# [DEGREE, RADIAN, GRAD]*, π, (×)!, ↑ (STATISTICS): MX, MY, SDX, SDY, SDXN, SDYN, LRA, LRB, COR, EOX, EOY, CNT, SX, SY, SX², SY², SYX.
VARIABLES	A~Z, A ( ), A$~Z$, A$ ( )	A~Z, A ( ), A$~Z$, A$ ( )
OTHER	, ; : " ? # !	, ; : " ? # !

NOTE:
*DEGREE, RADIAN AND GRAD ARE NOT WRITTEN IN AS WITH RADIO SHACK/SHARP MACHINES BUT ARE SELECTED USING A MODE KEY.

The printer cradle *for the TRS-80 Pocket Computer also serves as an interface to a cassette recorder that preserves programs on tape or loads them into the machine.*



Full keyboard labeling of BASIC statements *and math functions along with single-key entry of both make this Casio FX-702P programmable calculator easy to use.*

editing. The DEBUG function executes a program one line at a time, verifying not only the calculation, but also the instructions for it. LIST calls up the program, beginning with the first step, and you then step through it using the Step Forward key. Alternatively, you can call out a particular line number and go backward or forward from there. By the same token, you can readily list programs via the printer.

To edit and merge programs stored on magnetic tape, you merely transfer them into the Pocket Computer, perform the necessary operations and then transfer them back onto the tape. Radio Shack plans to expand its current software library of tape-cassette programs over the next few months.

Who needs BASIC?

Like the controversy that raged a few years ago debating the merits of reverse Polish notation vs algebraic notation, a new one questions whether BASIC is an effective language for scientifical and mathematical programming. The results of the debate aren't yet in.

BASIC is oriented toward data and information processing, and it uses a conversational language for its inputs. On the other hand, the calculator user who is programming extended numerical computations wants to concentrate on the intricacies of the solution; that is, he wants action, not words. Additionally, BASIC reduces the amount of memory space available for data storage and manipulation because a large amount of the machine memory gets used up in handling the language-compiler chores. For example, one designer tried a filter program on his Radio Shack TRS-80. He found that there was insufficient memory for that program in the TRS-80, but he was able to fit it into a TI 59 in about half that machine's memory space.

BASIC is, nevertheless, an easy-to-use language and has some advantages. And in minimizing the workload of inputting BASIC, Casio's FX-702P is superior to the other BASIC machines because Casio designers have merged the codes not only for the scientific and math functions, but also for BASIC statements. Thus, one key entry gives you both the math function and the BASIC statement. In fact, the resulting operation is very close to that of a standard scientific programmable calculator.

Casio packs the most math power

The most powerful math capability of the currently available horizontally stretched hand computing machines resides in Casio's FX-702P. Although programmed in BASIC, this machine offers several functions not usually found in that language. Indeed, it has all of the functions of the Radio Shack/Sharp Pocket Computers and several others besides (**table**). For example, you get hyperbolic and inverse hyperbolic functions, fractionalization (FRAC—removal of the integer part of a number), coordinate conversions from rectangular to polar and vice versa, a round-off feature (ROUND), a random-number generator (RAN#) and X factorial (X!). In addition, the -702P has 17 preprogrammed functions for statistical analysis, nine of which are single-key accessible, with the other eight requiring 2- or 3-letter inputs.

The -702P also features an excellent man-machine interface. For example, the surface of its keyboard's alpha section is loaded with information that guides you when you enter either math functions or BASIC-command statements.

This information appears in the form of three types of key inscriptions associated with 28 of the 35 alpha-section keys. The first is the letter, punctuation mark or BASIC symbol that's on the face of the key itself. The second is the BASIC mnemonic for the math functions, printed in red just above the keys. The third is a BASIC command printed in blue, just below the keys. You gain access to the red functions (SIN, COS, TAN, etc) by first pressing a red F1 shift key, and you call up the blue statements (FOR, TO, STEP, GOTO, etc) via a blue F2 shift key.

Swap space between program and data storage as needed

You can enter BASIC functions and statements either the hard way—by spelling them out on the keyboard—or the easy way—by using the red or blue shift keys and then pressing the key at which the red or blue function or statement is located. The latter approach is not only easier, but with all of the BASIC information spelled out in front of you, it helps shorten the learning period each time you press a key and reinforces the lesson each time you use the machine. You learn fast!

The FX-702P sports a program capacity of 1680 steps and 26 A to Z data registers. However, in a manner similar to that used in the Radio Shack/Sharp machines, you can convert program steps to data registers in groups of 10 registers, with each register taking eight program steps. Therefore, if the number of data registers is increaseed to a maximum of 226, the program steps decrease to a minimum of 80.

A DEFM (blue) command expands the data-memory bank, but should an insufficient number of program steps be available for the call, an error message appears to protect programs already written. Backup power for all registers and program memories prevents loss of data and program information.

Casio has carried over the efficient program-control architecture of the older FX-502P (EDN, June 20,

Battery life up, battery life down

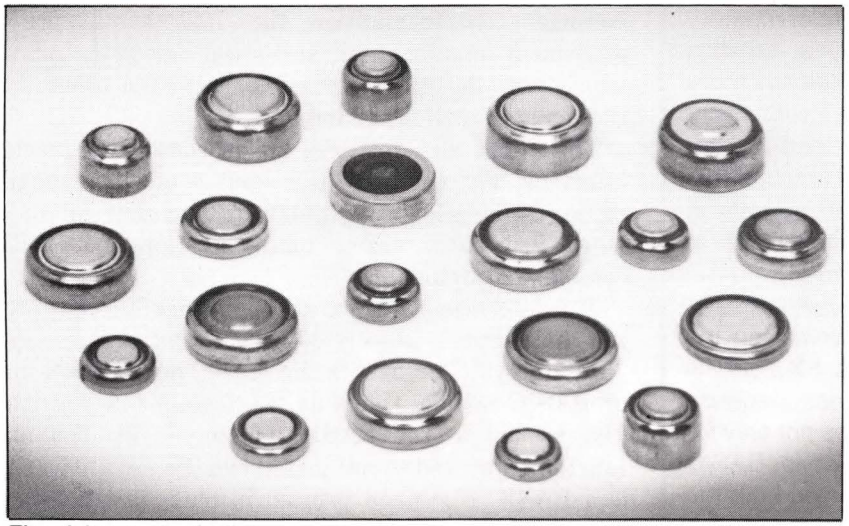
In the days of LED-display calculators, an annoying problem was the constant care required by rechargeable NiCd batteries. Then along came CMOS and LCDs, and battery drain dived to permit an unheard-of but very welcome 1000 hrs or more of continuous use with silver-oxide button cells. As a result, you could forget the battery for a year.

But the battery tide is shifting again: Battery life has decreased in the new hand-held computing machines. The Radio Shack/Sharp Pocket Computers, for example, use a 5.4V source of four Type 674 mercury cells and achieve an estimated operating life of 300 hrs. Casio's FX-702P employs two CR2302 3V lithium cells, providing an expected life of 200 hrs. And Casio's FX-602P, successor to the 1000-hr FX-502P, uses the same two CR2302 cells but achieves an expected life of 500 hrs with the FA-1 adapter.

The Panasonic and Quasar HHC main units, meanwhile, supply power to most of their peripherals and as a result require five NiCd rechargeable cells. Additionally, the thermal printers for the calculators discussed in this article also use rechargeable NiCd batteries because of their relatively high drain.

The silver-oxide cells' high cost has created an expanding interest in designing new calculators and other electronic devices around manganese-dioxide cells, according to Gilbert Merritt Jr, manager of battery engineering at Union Carbide. Alternatively, some calculator manufacturers approve the substitution of these alkaline manganese cells for the silver-oxide units in their machines. For example, Sharp calls for either three LR44 manganese-dioxide cells or three G13 silver-oxide cells in the EL-5103. (However, note that the LR44s provide only about 450 working hours, compared with 1400 for the G13 cells.)

Considering the high price of silver-cell replacement (on the order of $3.25 to $3.50), owners of other calculators might also be tempted to replace them with the manganese cells instead. But Merritt warns of possible problems if your calculator also has a clock circuit. Specifically, although most calculator circuits operate down to 1V or less, such clock circuits have a higher cutoff voltage. Additionally, although silver cells maintain a relatively constant voltage throughout their life, the voltage across manganese cells drops off gradually. Thus, with a manganese cell, the clock circuits stop working before the calculator quits. As a result, Merritt suggests staying with the silver cells if you own a clock/calculator; they're more cost effective anyway.



The rising cost of silver *is pressuring calculator designers to substitute mercury, manganese-dioxide or lithium cells for a wide variety of these silver cells from Union Carbide Corp.*

1979, pg 97) into the -702P. For instance, you can assign 10 program keys (P0 to P9) as labels for as many as 10 programs or subroutines. Additionally, you get transparent stacks for 10 levels of subroutines, eight levels of FOR-NEXT loops, 10 levels of temporary storage for numerical values and 20 for calculation elements.

Program checking and editing occur through LIST and TRACE commands, as well as with a special DEBUG command that specifies the type of error in a specific line of the program. To check and edit programs in Run mode, a LIST command automatically steps through the program, dwelling about 2 sec on each line in sequence. In Wrt mode, a LIST command allows you to step through the program one line at a time using the Exe key.

Unfortunately, the machine has no Backstep key. To accomplish this function, you must clear the line from the display and reinsert a LIST command with the desired line number.

The -702P also provides a useful feature that shows you which of the 10 program areas contains information and which are available for programs. For example, assuming that P1, P3 and P7 store programs but the remaining areas are free, if you initiate the Wrt mode, the readout displays READY P0: 0_2_456_89. Additionally, the number of program steps available appears in a small 4-digit display at the far right of the screen. As programming proceeds, the number displayed decreases with each step used, thus providing a constant check on space available for program or data allocation.

As an added feature, the -702P accepts preprogrammed ROM cartridges to extend its programming capabilities. The firm expects to offer 10 such cartridges by the first of next year.

The FX-702P lets you protect your programs by providing the ability to assign passwords or code names to them. When you don't want others to know a program's contents, or if you don't want anyone else to change a program, you assign to it a scrambled code word of as many as eight letters, numbers or symbols. These passwords are effective for each program and are attached only to P0-P9 programs.

You would use the following format to attach a password, enclosing the password in quotes:

```
PASS  "#$"      EXE
PASS  "GLUBZ"   EXE
PASS  "AZ-1"    EXE
```

You can clear the password by clearing the entire program or by reinputting it. When checking a program, if you input a password following LIST, it is temporarily canceled for that LIST command.

Older calculators are improved

Overshadowed by the interest in the new BASIC hand-held machines are two other new scientific alphanumeric programmables that use machine language: Casio's FX-602P and Sharp's EL-5103, both updated versions of earlier machines.

The -602P includes upper- and lower-case letters in its 86-character/symbol dot-matrix display repertoire. But because it's packaged in a more conventional vertical design, it can display only 11 characters at a time. However, all input commands are written on the display, simplifying program checking, correction, addition or deletion. The -602P, an improved version of the well-known -502P, plugs into the same FA-1 cassette adapter; thus, you can load -502P programs into the -602P from cassette tape. Although the

Calculator manufacturers and additional sources of programmable-machine information

For more information on personal scientific calculators and related products and activities, contact the following manufacturers or software clubs directly or circle the appropriate numbers on the Information Retrieval Service card.

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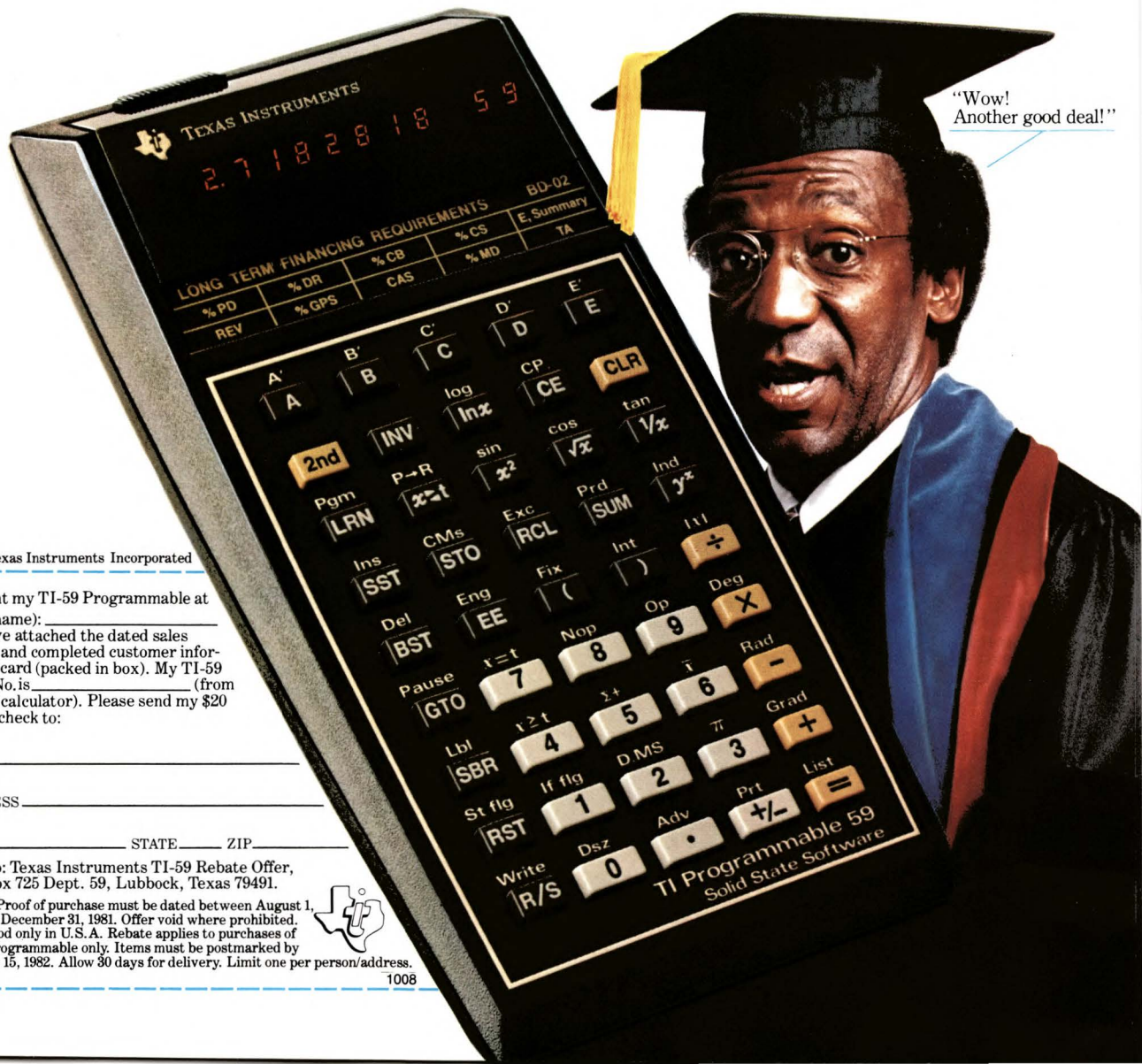

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1008

Protect programs with special passwords

converse isn't true, the lack isn't very important.

The FX-502P's keyboard is relatively unchanged in the -602P, except that Casio has added to the keyboard-face markings new letters and symbols that you can call into the display via the keys. You gain access to these new characters by putting the machine in Alpha mode, one of three new ones. (A second new mode partitions the data registers, and the third verifies partitioning upon demand.)

You can transfer programs and data from the calculator through the FA-1 adapter and reload them using microcassette, standard cassette and open-reel recorders. And for the -502P music-lover owner who programs tunes on tape, the -602P extends the repertoire from 20 to 80 notes over three octaves.

The FX-602P doubles the size of the -502P's program memory to 512 steps. All of these steps can divide into 10 programs or subroutines by means of the P0 to P9 keys. Because of its highly merged codes, the -602P minimizes effective step numbers; thus, one step generally corresponds to one function. As a result, you can easily manage 3-dimensional equations, parenthetically nested numbers and other complex formulas.

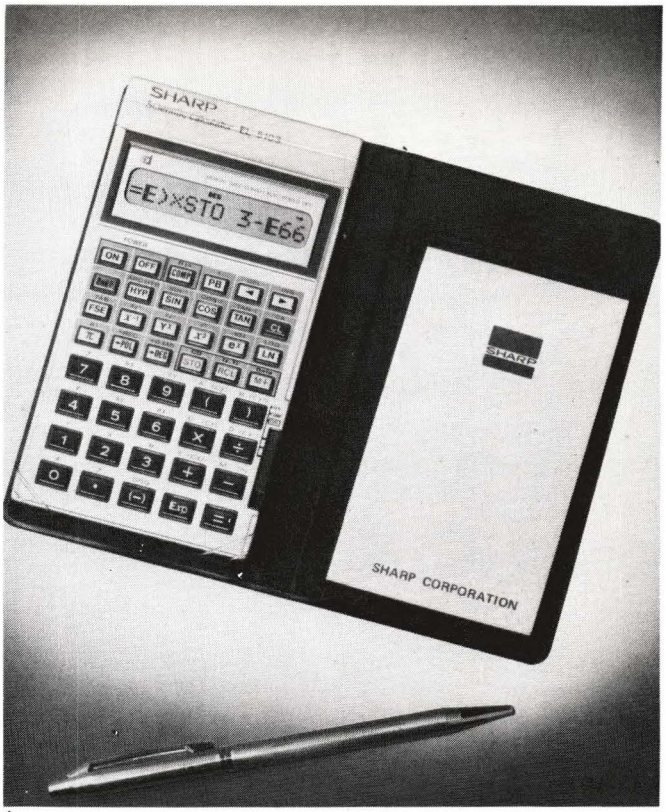
As in the -702P, the -602P's 22 data registers can be increased to a maximum of 88 by transferring unused program steps to them. And with an algebraic hierarchy similar to that of TI's Algebraic Operation System, you can nest 33 levels of parentheses in the -602P.

The FX-602P also provides the capability of designating special-function keys. You can assign the P0 to P9 keys as labels for 10 programs and digits 0 to 9 as labels for unconditional jump (GOTO) destinations. As many as nine subroutines can be called in a main program using the GSB key followed by a P1 to P9 key.

Conditional jumps for X=0 and X≥0 judge the display-register contents; X=F and X≥F compare the contents of the X and MF registers. Two other conditional jumps (IDZ and DSZ) control repeated operations running in a loop. Indirect addressing designates a jump designation.

The -602P has the same password feature as the -702P. And its calculating speed is higher than the -502P's. For example, decomposing the prime number 379721 into other primes requires 37 sec, compared with 1 min, 15 sec on the -502P.

The other new machine-language-programmable calculator, Sharp's EL-5103, furnishes a 13-character scrolling alphanumeric display. It's a lower priced repackaged version of the EL-5100, which, as noted, set the format for today's generation of pocket computers. The number of steps storable in the display register equals 80 for both machines, but data memories are reduced from 10 in the -5100 to six in the -5103. You can input expressions with as many as 15 levels of parentheses and eight levels of pending operations in the -5103.



A vertically styled wallet-type version *of its manufacturer's EL-5100, Sharp's EL-5103 has a scrolling display of 13 characters. The display buffer can hold 80 characters, however.*

Sharp has managed to package all 61 of the -5100's scientific and math functions into the -5103's more conventional vertically oriented 2.75×5-in. form factor. Power drain is reduced: You get an estimated 1400 hrs of continuous use from three silver cells, compared with 1000 hrs on the older machine. **EDN**

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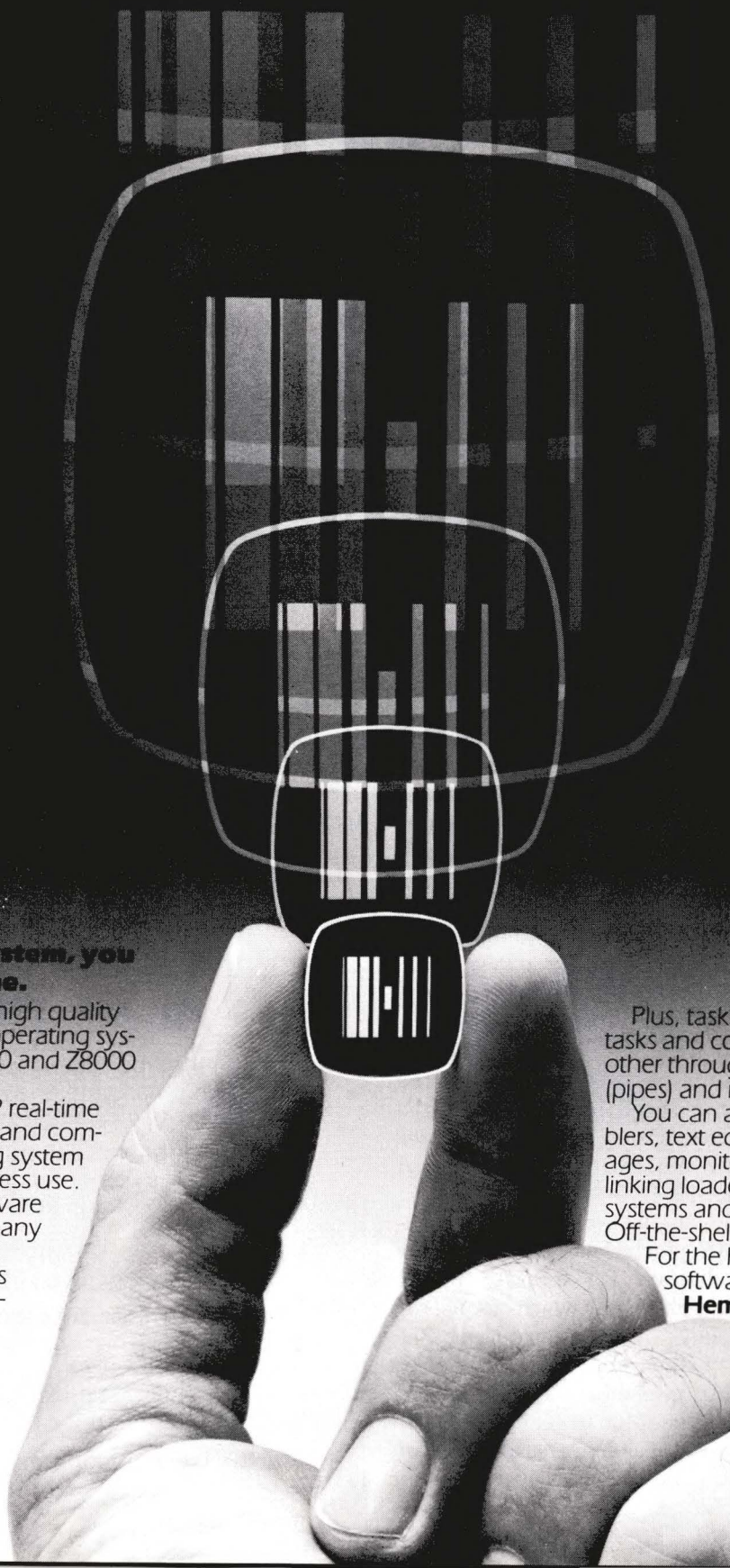

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CIRCLE NO 41

Add the FFT to your box of design tools

Implementing the fast Fourier transform and its inverse on your personal μC can increase your productivity.

Robert H Cushman, Special Features Editor

The three previous articles in this series have focused on how LSI and VLSI devices are allowing—even forcing—OEM design engineers to make greater use of number-crunching techniques. We've pointed out that number-crunching functions such as simulation, signal processing and numerical analysis will become commonplace in all aspects of designers' professional lives: They will be part of design analysis and laboratory testing and will be embodied in all sorts of products, from space-ship guidance computers to children's talking toys. Here, we wind up our miniseries on digital processing by expanding on the subject of the last article (**Ref 1**): the fast Fourier transform (FFT) and its inverse (IFT).

These tools, implemented as algorithms on your personal computer, allow you to switch between the time and frequency domains with minimal effort. They are particularly suited to personal-computer use because, unlike the concepts in other areas of digital processing, they apply primarily to one design task. Once you have this task computerized as part of your disk- or cassette-based library of design-aid programs (**Fig 1**), you'll be able to use it throughout your OEM design work.

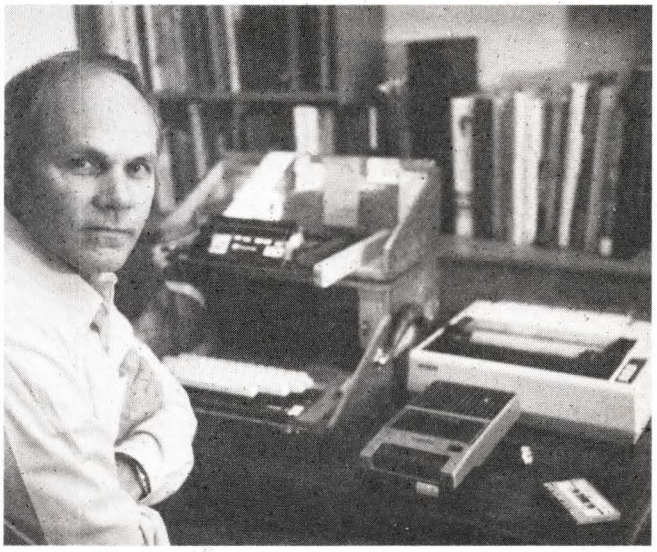


Fig 1—Personal μCs for an engineer's use in design analysis *need not be expensive. The author's system costs approximately $1000. It consists of a Rockwell Aim-65 μC with 4k RAM ($600), an Epson MX-80 printer ($400) and an audio cassette recorder ($50). It can run the FFT/IFT programs shown in* ***Figs 2*** *and* ***4*** *with as many as 128 points in about 50 sec.*

Two FFT listings start you off

The program listings for FFTs and IFTs shown in **Figs 2** and **4** are only two of the many available. We have been running them for familiarization and thus know that they work. Note that each uses different symbols; we have retained the authors' notation because we didn't want to risk introducing errors.

These programs, which come from **Refs 2** and **3**, consist of FFT and IFT subroutines callable from a main program. In **Fig 2**, the subroutine runs from line 500 to 1060; in **Fig 4**, from line 3000 to 3228. The remainder of each program consists of short main programs that prepare for the use of the subroutines. They take care of such tasks as dimensioning the arrays to hold the data and defining the main parameters. We have written these main programs so they interactively ask you for the necessary parameters and give you a painless way of learning about FFTs and IFTs.

Note that in each case the same subroutine serves for both the FFT (time domain to frequency domain) and the IFT (frequency domain to time domain). The only difference is a sign bit, which you set up by your choice of FFT or IFT at lines 11, 12 and 13 in **Fig 2** or lines 102, 103, 104 and 105 in **Fig 4.**

Both of the programs are written in Microsoft BASIC (to run on our Aim-65 μC). If your μC uses a BASIC other than the Microsoft version, you might have to make minor modifications in notation, but they shouldn't prove difficult. Some of the textbooks on BASIC for μPs provide guidelines for such conversions. For background on the programs themselves, see **Refs 2** and **3**; **Ref 3**, especially, gives a detailed explanation of FFT mechanics.

The programs occupy approximately 1700 bytes of RAM; each array element requires an additional five

Two BASIC-programmed FFT/IFT algorithms provide experience

bytes. These requirements limit us to 128-point transforms in our Aim-65, which has just 4k of RAM. It takes us approximately 50 sec to execute a 128-point FFT or IFT—far faster than the 1 hr a 128-point transform would take with the discrete-Fourier-transform (DFT) algorithm.

Today's typical personal μC has 8k or 16k of RAM and therefore should be able to execute FFTs and IFTs as large as most engineers would want—to 512 or 1024 points. These larger transforms should take approximately 5 or 10 min, respectively. (Actually, even for our shorter FFTs and IFTs, we have found that the chore of entering the input data and the long wait for results printout become annoying when we attempt transforms with more than 32 points. For larger transforms, we assume that most engineers would want to incorporate automatic data acquisition and display the results graphically on a CRT. However, the programs as presented are adequate for their primary purpose—providing a vehicle for your initial self-education in FFTs and IFTs.)

Figs 3 and **5** show demonstration runs of the two programs. These runs repeat the short 8-point FFT example from **Ref 2,** obtaining essentially the same answer (except for the imaginary sign). You can use them as a check.

If you've never used the FFT/IFT, we suggest several exercises using the **Fig 2** or **Fig 4** programs **(Fig 6).** For each exercise, we advise performing both the FFT and the IFT on the waveforms and spectra so that you can see to what degree you can go back and forth between domains.

First, perform an FFT on an elementary dc "wave" and observe that a dc level in the time domain produces only an amplitude at N=0 in the frequency domain. Then, using the IFT, try positive and negative and zero levels for both the real and imaginary values of the dc or N=0 frequency, leaving all other points zero.

Second, try the same operations on pure sine waves. You'll find that the easiest way to obtain a time-domain sine wave is to enter the spectral-line magnitude in the frequency domain and then use the IFT to plot the time-domain wave shape. Shift the time wave in phase and use the FFT to see what happens to the spectrum; observe the changes in the magnitudes of the real and imaginary components, indicating that the resultant vector is rotating in phase.

```
4 PRINT"  <<7161X>>"
5 PRINT"********************"
6 PRINT"    FFT/IFT"
7 PRINT"  AFTER WAGGENER"
8 PRINT"********************"
9 INPUT"DATE";DA$
10 INPUT"HR";HR$
11 INPUT"FWD-OR-INV";AN$
12 IF AN$="F" THEN D=0
13 IF AN$="I" THEN D=1
20 INPUT"M=";M
30 N=2^M
31 PRINT"N=";N
32 DIM X(N,2)
35 IF D=0 THEN PRINT"INPUT TIME DOMAIN DATA"
36 IF D=1 THEN PRINT"INPUT FREQ DOMAIN DATA"
40 FOR I=1 TO N
41 PRINT"-------------------"
44 PRINT"INPUT X("I;",0) X("I;",1)"
45 INPUT X(I,0),X(I,1)
50 NEXT I
51 PRINT"==================="
55 IF D=0 THEN PRINT"TIME DOMAIN INPUT DATA ARRAY IS:"
56 IF D=1 THEN PRINT"FREQ DOMAIN INPUT DATA ARRAY IS:"
57 PRINT"POINT   REAL   IMAG"
60 FOR I=1 TO N
70 PRINT I;"     ";X(I,0);"   ";X(I,1)
80 NEXT I
110 GOSUB 500
111 PRINT"//////////////////"
112 IFD=0 THEN PRINT"NOW IN FREQ DOMAIN!"
113 IF D=1 THEN PRINT"NOW IN TIME DOMAIN!"
114 PRINT"XFRMD DATA IS:"
115 PRINT"POINT   REAL   IMAG"
120 FOR I=1 TO N
130 PRINT I;"  ";X(I,0);"  ";X(I,1)
140 NEXT I
142 PRINT"==================="
145 PRINT"   -DONE-"
150 END
500 REM*********************
501 REM   FFT/IFT SUBROUTINE
502 REM*********************
550 N=2^M
560 REM***DO BIT SHUFFLE***
570 N2=N/2
580 N1=N-1
590 J=1
600 FOR I=1 TO N1
610 IF I>=J THEN 680
630 T1=X(J,0)
640 T2=X(J,1)
650 X(J,0)=X(I,0)
655 X(J,1)=X(I,1)
660 X(I,0)=T1
670 X(I,1)=T2
680 K=N2
690 IF K>=J THEN 730
700 J=J-K
710 K=K/2
720 GOTO 690
730 J=J+K
740 NEXT I
750 REM***END OF SHUFFLE***
760 S1=-1
770 IF D=0 THEN 790
780 S1=1
790 P1=3.1415926535898
800 FOR L=1 TO M
810 L1=2^L
820 L2=L1/2
830 U1=1
840 U2=0
850 W1=COS(P1/L2)
860 W2=S1*SIN(P1/L2)
870 FOR J=1 TO L2
880 FOR I=J TO N STEP L1
890 I1=I+L2
895 REM***DO BUTTERFLY***
900 V1=(X(I1,0)*U1-X(I1,1)*U2)
910 V2=(X(I1,1)*U1+X(I1,0)*U2)
920 X(I1,0)=X(I,0)-V1
930 X(I1,1)=X(I,1)-V2
940 X(I,0)=X(I,0)+V1
950 X(I,1)=X(I,1)+V2
960 NEXT I
970 REM***DO TWIDL FACTOR***
975 U3=U1
976 U4=U2
980 U1=(U3*W1-U4*W2)
990 U2=(U4*W1+U3*W2)
1000 NEXT J
1010 NEXT L
1020 IF D=1 THEN 1060
1030 FOR I=1 TO N
1040 X(I,0)=X(I,0)/N
1045 X(I,1)=X(I,1)/N
1050 NEXT I
1060 RETURN
```

Fig 2—This FFT/IFT program, *from* **Ref 2,** *was created for use in instrumentation evaluations.*

```
 1 PRINT"  -6261A"
 2 POKE4,113:POKE5,232:X=USR(X)
 3 LIST
 4 PRINT"  <<7161X>>"
 5 PRINT"********************"
 6 PRINT"     FFT/IFT"
   PRINT"  AFTER WAGGENER"


  <<7161X>>
********************
    FFT/IFT
  AFTER WAGGENER
********************
DATE? 7/25/81
HR? 10.17 A
FWD-OR-INV? F
M=? 3
N= 8
INPUT TIME DOMAIN DATA
-------------------
INPUT X( 1 ,0) X( 1 ,1)
? 1
?? 0
-------------------
INPUT X( 2 ,0) X( 2 ,1)
? 2
?? 0
-------------------
INPUT X( 3 ,0) X( 3 ,1)
? 1
?? 0
-------------------
INPUT X( 4 ,0) X( 4 ,1)
? 1
?? 0
-------------------
INPUT X( 5 ,0) X( 5 ,1)
? 3
?? 0
-------------------
INPUT X( 6 ,0) X( 6 ,1)
? 2
?? 0
-------------------
INPUT X( 7 ,0) X( 7 ,1)
? 1
?? 0
-------------------
INPUT X( 8 ,0) X( 8 ,1)
? 2
?? 0
==================
TIME DOMAIN INPUT DATA ARRAY IS:
POINT    REAL    IMAG
 1        1       0
 2        2       0
 3        1       0
 4        1       0
 5        3       0
 6        2       0
 7        1       0
 8        2       0
//////////////////
NOW IN FREQ DOMAIN!
XFRMD DATA IS:
POINT    REAL    IMAG
 1     1.625     0
 2    -.161611652
 .0883883476
 3     .25    -.125
 4    -.338388347
 .0883883476
 5    -.125     0
 6    -.338388348
-.0883883476
 7     .25     .125
 8    -.161611653
-.0883883476
==================
   -DONE-
```

Fig 3—A trial of Fig 2's program *performs a short 8-point FFT.*

```
50 PRINT"**********************"
55 PRINT"   FFT/IFT"
57 PRINT"AFTER CHAMBERLIN"
60 PRINT"**********************"
61 PRINT" 7271A - USOFT BASIC"
62 PRINT"  ON ROCKWELL AIM-65"
63 PRINT"======================"
100 INPUT"DATE:";DA$
101 INPUT"HOUR:";HR$
102 INPUT"FWD-OR-INV";AN$
103 IF AN$="F" THEN FI=1
104 IF AN$="I" THEN FI=-1
105 PRINT"FI=";FI
110 INPUT"RUN DESCR";CM$
200 PRINT"==================="
2000 PRINT"SET FFT/IFT SIZE, N"
2010 INPUT"K=";K
2011 N=2^K
2020 DIM D1(N)
2021 DIM D2(N)
2022 PRINT"N=";N
2035 PRINT"-------INPUT DATA--"
2040 FOR I=0 TO N-1
2044 PRINT"---FOR POINT,";I;"---"
2045 INPUT"REAL";D1(I)
2046 INPUT"IMAG";D2(I)
2050 NEXT I
2110 GOSUB 3000
2113 PRINT"//////////////////"
2114 PRINT"RESULTS: REAL & IMAG"
2115 IF FI=-1 GOTO 2200
2120 FOR I=0 TO N-1
2121 PRINT"------------------"
2130 PRINT I;D1(I)/N;D2(I)/N
2140 NEXT I
2142 PRINT"=================="
2143 PRINT"RESULTS: MAG VECT"
2150 FOR I=0 TO N-1
2155 PRINT"------------------"
2160 PRINT"V";I;"=";SQR(D1(I)^2+D2(I)^2)/N
2170 NEXT I
2175 PRINT"=================="
2190 PRINT"   -DONE-"
2195 END
2200 REM PRINT IFT RESLTS
2210 FOR I=0 TO N-1
2215 PRINT"------------------"
2220 PRINT I;D1(I);D2(I)
2230 NEXT I
2240 PRINT"=================="
2250 PRINT"   -DONE-"
2260 END
3000 PRINT"  -7031B-"
3001 PRINT"=================="
3002 PRINT"  FFT/IFT SUBR"
3003 PRINT"    (CHAMBERLIN)"
3004 PRINT"=================="
3110 N=2^K
3111 N1=0
3112 N2=N-1
3113 FOR N3=1 TO N2
3114 N4=N
3115 N4=N4/2
3116 IF N1+N4>N2 GOTO 3115
3117 N1=N1-INT(N1/N4)*N4+N4
3118 IF N1<=N3 GOTO 3125
3119 T1=D1(N3)
3120 D1(N3)=D1(N1)
3121 D1(N1)=T1
3122 T2=D2(N3)
3123 D2(N3)=D2(N1)
3124 D2(N1)=T2
3125 NEXT N3
3200 REM***DO CMPLX FFT***
3210 N4=1
3211 N6=2*N4
3212 FOR N3=0 TO N4-1
3213 A=FI*N3*3.14159265359/N4
3214 C=COS(A)
3215 S=SIN(A)
3216 FOR N7=N3 TO N-1 STEP N6
3217 N8=N7+N4
3218 T1=C*D1(N8)-S*D2(N8)
3219 T2=C*D2(N8)+S*D1(N8)
3220 D1(N8)=D1(N7)-T1
3221 D2(N8)=D2(N7)-T2
3222 D1(N7)=D1(N7)+T1
3223 D2(N7)=D2(N7)+T2
3224 NEXT N7
3225 NEXT N3
3226 N4=N6
3227 IF N4<N GOTO 3211
3228 RETURN
```

Fig 4—This FFT/IFT program, *from* **Ref 3,** *was produced for use in music-synthesis applications.*

```
********************
   FFT/IFT
AFTER CHAMBERLIN
********************
 7031D - USOFT BASIC
  ON ROCKWELL AIM-65
==================
DATE:? 7/15/81
HOUR:? 12.1.01 P
FWD-OR-INV? F
FI= 1
RUN DESCR? WAGGENER SAMPLE
==================
SET FFT/IFT SIZE, N
K=? 3
N= 8
-------INPUT DATA--
---FOR POINT, 0 ---
REAL? 1
IMAG? 0
---FOR POINT, 1 ---
REAL? 2
IMAG? 0
---FOR POINT, 2 ---
REAL? 1
IMAG? 0
---FOR POINT, 3 ---
REAL? 1
IMAG? 0
---FOR POINT, 4 ---
REAL? 3
IMAG? 0
---FOR POINT, 5 ---
REAL? 2
IMAG? 0
---FOR POINT, 6 ---
REAL? 1
IMAG? 0
---FOR POINT, 7 ---
REAL? 2
IMAG? 0
  -7031B-
==================
  FFT/IFT SUBR
    (CHAMBERLIN)
==================
//////////////////
RESULTS: REAL & IMAG
------------------
 0  1.625  0
------------------
 1 -.161611652
-.0883883475
------------------
 2  .25  .125
------------------
 3 -.338388348
-.0883883476
------------------
 4 -.125  0
------------------
 5 -.338388348
 .0883883475
------------------
 6  .25 -.125
------------------
 7 -.161611652
 .0883883476
==================
RESULTS: MAG VECT
------------------
V 0 = 1.625
------------------
V 1 = .18420322
------------------
V 2 = .279508497
------------------
V 3 = .349741582
------------------
V 4 = .125
------------------
V 5 = .349741582
------------------
V 6 = .279508497
------------------
V 7 = .18420322
==================
   -DONE-
```

Fig 5—A trial run of Fig 4's program, *like the trial run in* ***Fig 3,*** *performs an 8-point FFT.*

Try some basic exercises to familiarize yourself with FFT/IFTs

Third, try combinations of multiple cosine and/or sine waves. Here, too, the easiest way to construct these waveforms is to start in the frequency domain, draw in magnitudes at various harmonics and then use the IFT to generate the time-related amplitudes for the composite wave. Here, you'll see now neatly the algorithm can handle multitone signaling, such as that used in Touch-Tone dialing.

Fourth, try square waves, both single pulses and in pulse strings. Determine what size FFTs you need to handle them, the test being whether the IFT will reproduce the original square wave.

Fifth, substitute some statements to have your inputs automatically generated by equations for various curves. We found the exponentially decaying waveform from **Ref 4** quite instructive in this regard because it was backed by the rigor of that authoritative reference.

Sixth, try arbitrary waveforms, sketched by hand or obtained from an A/D converter. This exercise provides the challenging assignment of generally interpreting FFT/IFT results. It raises several questions:

- When have you exceeded the Nyquist cutoff bandwidth?
- What is the interpretation of aperiodic signals? (The FFT/IFT in theory only applies to periodic signals.)
- What is the effect of window distortion (briefly covered in **Ref 1**)?

You will soon see that although the FFT/IFT is readily usable and obviously very valuable, its exact interpretation can often be a puzzlement. At this point, your intellectual curiosity will be properly whetted, and you'll be primed to study the many excellent references on FFT/IFT theory and practice. We suggest that you start by obtaining the IEEE list of publications, which contains some of the best recent texts on the subject.

About this time you might also begin to wonder how the FFT relates to similar analysis techniques, particularly correlation (**Ref 5**). The answer is that correlation, which only works in the time-to-frequency direction (it has no IFT equivalent), can sometimes be superior for analyzing the periodicity of simpler time-domain signals. However, the FFT/IFT combination proves best for complex waveforms and is the only tool for working in both directions.

Using the FFT/IFT

To illustrate how you might use **Fig 2** and **4**'s tools, examine how three engineers have already used them. The first two are the authors of the programs; the third, a research engineer with RCA.

William Waggener, **Fig 2**'s program's author and an engineer with Sangamo Weston (Sarasota, FL), uses the FFT for evaluating the frequency response of instrumentation tape recorders. He records a known signal and then plays it back, digitizes the waveform and performs the FFT to obtain amplitude and phase response. He likes the FFT because it can be performed automatically and rapidly.

A distinct advantage of the FFT is that it allows "1-shot" tests in which you examine several frequencies of interest simultaneously. The recorded test signal can be a composite of several frequencies (perhaps constructed with the aid of the IFT), and the response spectra via the FFT show the magnitudes and phases for each of them. (Alternatively, a time-domain waveform rich in harmonics, such as a square wave, can serve as the test input.)

Waggener agrees with our experience that the printout, rather than the FFT calculation itself, is the tedious part of this analysis. His 256-point FFTs take only about a minute or so to calculate. He recommends plotting the results graphically: Even though this plotting takes time, the resulting human interpretation of the plot can be rapid. Sangamo's goal, reports Waggener, is to fully automate the test using IEEE-488-connected instruments such as a digital storage scope, HP 85 computer and plotters.

Hal Chamberlin, **Fig 4**'s program's author, explains that his prime interest in the FFT/IFT is for its use in musical analysis and synthesis. Such direct digital synthesis of music with the FFT/IFT is used by leading musical experimenters at Bell Laboratories and Stanford University.

Although music exists only in the time domain, it is best analyzed and synthesized in the frequency domain, says Chamberlin. He uses the FFT to transform musical passages into the frequency domain, then analyzes and creatively alters them, then uses the IFT to return them to the time domain to be played.

Chamberlin divides musical passages into a series of 10- to 50-msec windows and performs 128- to 512-point FFTs on these windows. The more rapidly changing the sound, the narrower the windows must be, but for a given window duration, there must be enough FFT points (enough A/D conversion samples) to provide the desired frequency resolution.

Fig 7 shows our diagramatical interpretation of the tradeoffs. The extremes go from crude fidelity at the lower left-hand corner to high fidelity at the upper right-hand one. In the lower left-hand corner, wide 50-msec windows and short 128-point transforms produce unacceptable results—only 1.28-kHz Nyquist bandwidths. At the upper right-hand corner, narrow 10-msec windows and longer 512-point transforms produce excellent 25.6-kHz bandwidths. We also plot a point for a 20-msec window and a 1024-point transform; this combination might be a goal for use in future high-fidelity music systems.

Chamberlin's company, Micro Technology Unlimited (Raleigh, NC), sells software based on the Fourier transform (currently using the slower discrete version) that allows μC owners to create multipart music. When creating compositions in the frequency domain, it's easy to specify the spectrum for more than one instrument

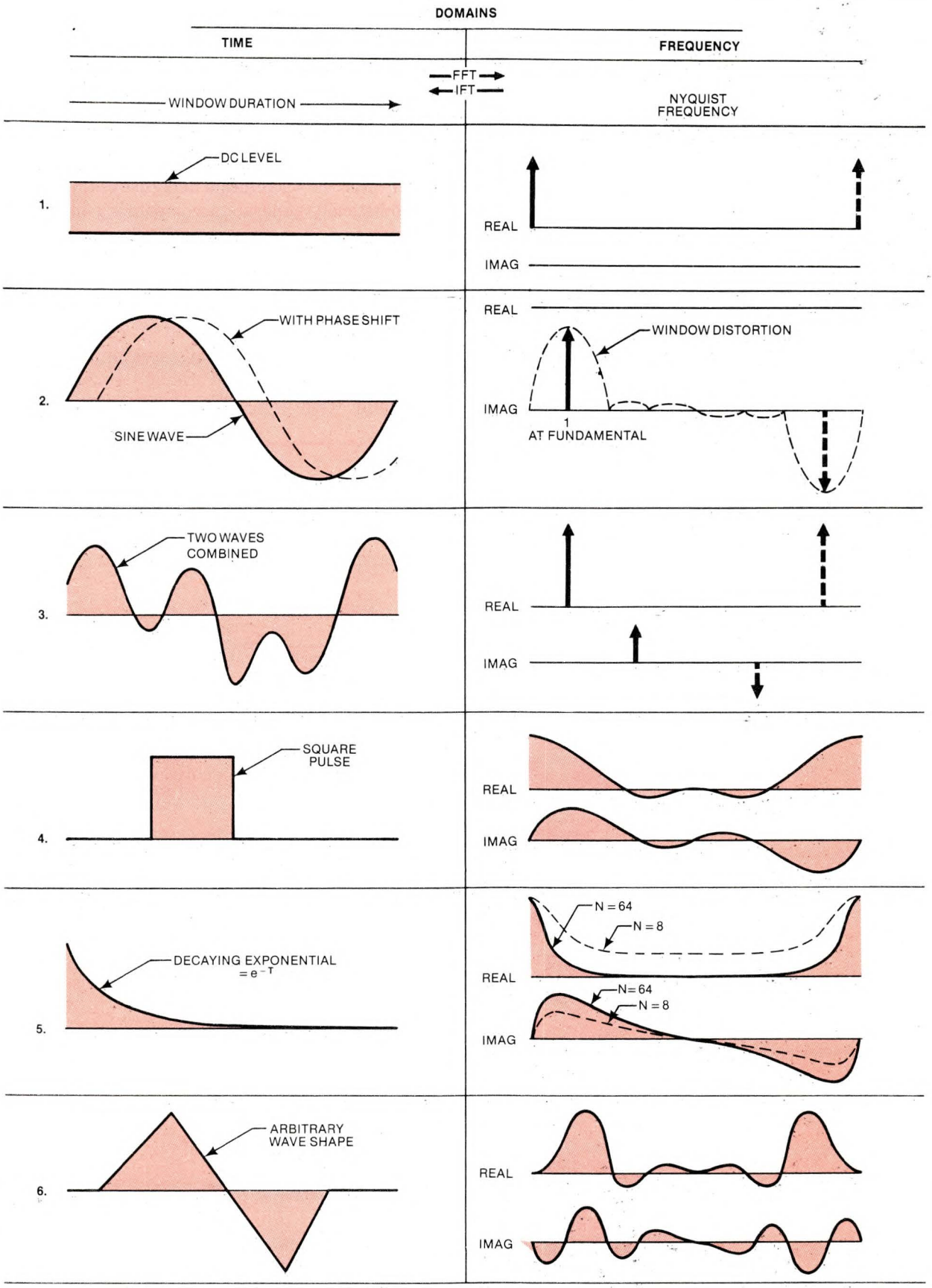


Fig 6—Perform these familiarization exercises *to gain expertise in FFT/IFT operations. By transferring back and forth between the time and frequency domains on simple, elementary curves like these, you can gain an initial familiarity with the FFT and IFT and ready yourself for more serious study of the underlying theory.*

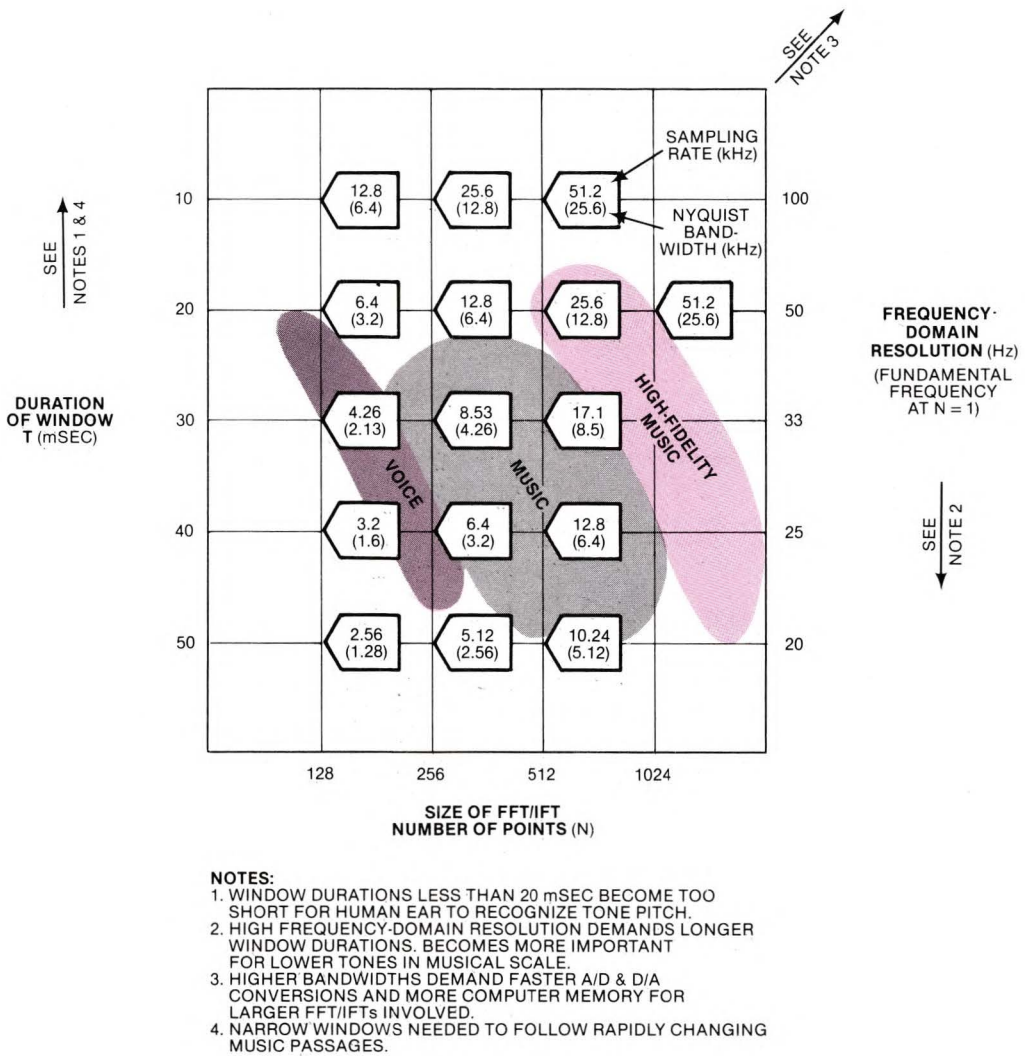
and then have all instruments play simultaneously in the time domain. It's also easy in the frequency domain to define the characteristics of the individual instruments so that they either sound like conventional instruments or have entirely original characteristics.

Chamberlin's software is used to create time-domain look-up tables, which, when scanned by a μP and fed to a DAC in real time, "play" the composition. His book **(Ref 3)** provides a good general discussion of the direct digital synthesis methods in contrast to analog ("Moog synthesizer") approaches. Even readers not interested in music will learn more about the uses of the FFT and IFT from it.

We speculate that in the future, when fast FFT/IFT chips become available at low cost, you'll see electronic musical instruments that make use of the FFT and IFT in real time. For example, you can imagine an instrument in which the keyboard inputs represent frequency-domain choices (as indeed they now do with most instruments) which are converted in real time by IFT algorithms into time-domain waveforms that drive speakers. You can also imagine how easy it will be to add software-driven real-time signal processing to further alter the waveforms being played, and perhaps to automatically generate accompanying instruments.

An impressive FFT application

Our third example of FFT/IFT use comes from Stu Perlman of RCA's Princeton, NJ Laboratories, who over a 3-yr period developed a complete digital-computer simulation for TV systems for use as a design tool. Described in **Ref 6,** Perlman's simulation covers everything from the initial light entering the TV



NOTES:
1. WINDOW DURATIONS LESS THAN 20 mSEC BECOME TOO SHORT FOR HUMAN EAR TO RECOGNIZE TONE PITCH.
2. HIGH FREQUENCY-DOMAIN RESOLUTION DEMANDS LONGER WINDOW DURATIONS. BECOMES MORE IMPORTANT FOR LOWER TONES IN MUSICAL SCALE.
3. HIGHER BANDWIDTHS DEMAND FASTER A/D & D/A CONVERSIONS AND MORE COMPUTER MEMORY FOR LARGER FFT/IFTs INVOLVED.
4. NARROW WINDOWS NEEDED TO FOLLOW RAPIDLY CHANGING MUSIC PASSAGES.

Fig 7—FFT-parameter tradeoffs *for audio applications reveal the combinations of window width and sampling frequency most useful in those applications.*

camera at the studio to the light coming out of the home viewer's set. It models the camera, broadcast link and receiving set.

The FFT and IFT are used 11 times in this computer simulation to transfer back and forth between the time and frequency domains. Such transfers are essential, because certain computations along the signal path can only be done in the time domain and others only in the frequency domain. (For example, it is only possible to check on the depth of broadcast modulation if the signal is in the time domain, but filtering can best occur in the frequency domain.)

Perlman's choice of FFT/IFT window duration and number of points involved a tradeoff that pushed him well beyond the limits of most personal-μC systems. He wanted to capture the basic periodicity of the TV signal, and that meant using a window spanning two TV horizontal lines or 127.11 μsec. Then, to achieve adequate bandwidth he was forced to a very large 4098-point FFT/IFT (resulting in a 16.11-MHz Nyquist or cutoff bandwidth). To perform these large transforms, he used an IBM 370 mainframe with 900k words of core memory.

The 370, programmed in FORTRAN IV, provides virtually instant simulation runs. Perlman believes that current 8-bit μPs, especially if programmed in interpreted BASIC like that of our **Fig 2** and 4 programs, would be impossibly slow and would not have the memory capacity to hold his large array (approximately 4M bytes, we estimate). However he acknowledges that the coming generation of 16/32-μPs might be able to handle this degree of simulation. **EDN**

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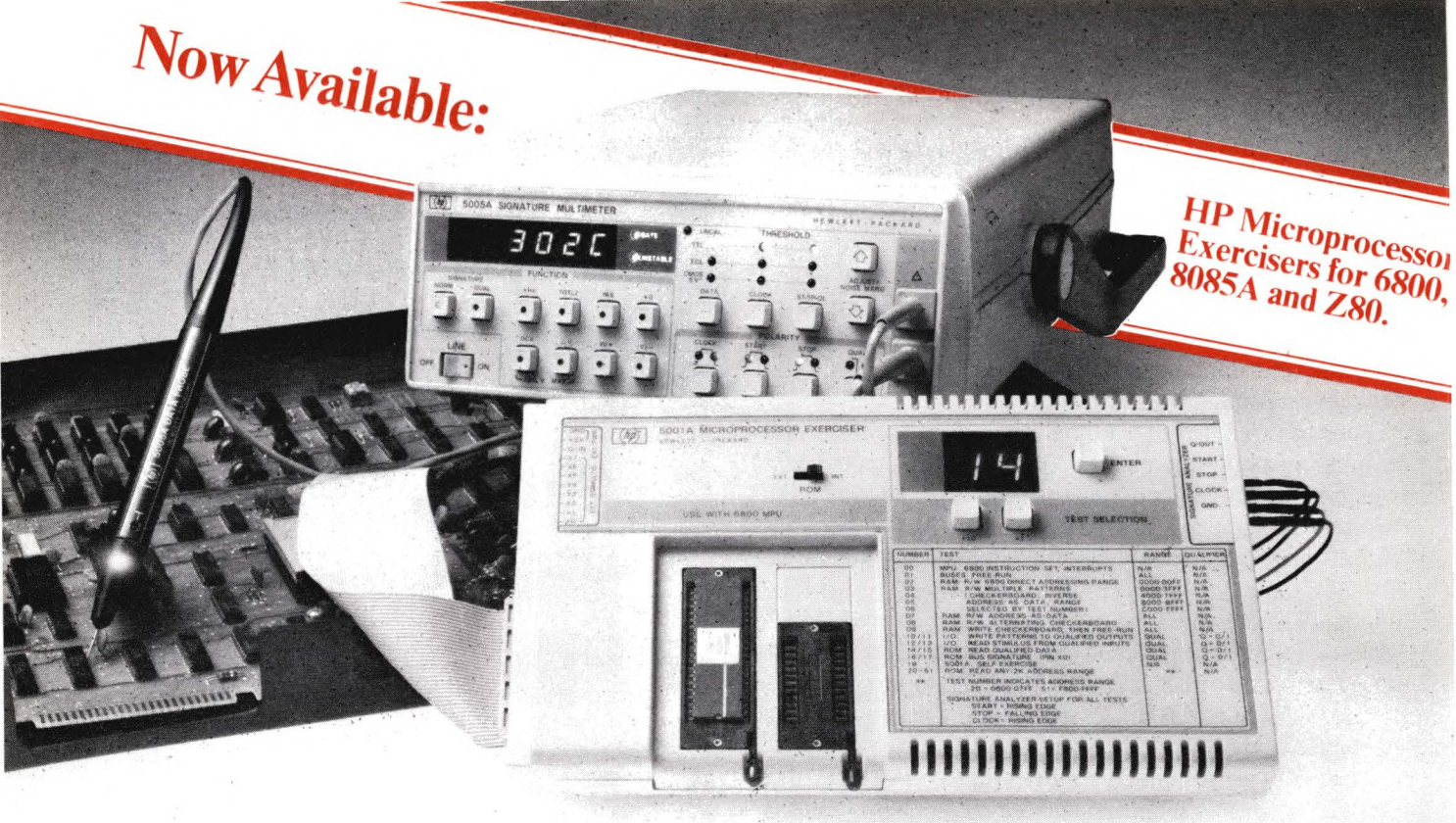

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Noise-property analysis enhances PLL designs

You can calculate phase noise based on loop-component specs and thus determine the worst-case performance of PLL systems.

Larry Martin, Consultant

With the mathematical and graphical techniques presented here for predicting phase noise in your phase-locked-loop (PLL) output, you can cost effectively specify the required performance when evaluating PLLs. This capability proves important because the phase-noise performance of subsystems such as indirect frequency synthesizers in receiver systems can determine system performance.

Review puts PLL fundamentals in perspective

Two equally valid sets of nomenclature—phase-domain or frequency-domain terms—can be used to describe PLL parameters (**Fig 1a**). The phase-domain definitions of interest are:

$\theta_R(s)$=input phase to the loop (rad)
$\theta_0(s)$=output phase of the loop (rad)
$\theta_E(s)$=phase error in the loop (rad)
$\theta_V(s)$=phase correction to the VCO (rad)
$K_P(s)$=phase-detector gain (V/rad)
A(s)=loop-amplifier gain (V/V)
$K_V(s)$=VCO transfer gain (rad/sec/V)
$K_0(s)$=VCO phase-transfer gain (rad/V).

In Laplace-transform terms, VCO phase-transfer gain relates to VCO voltage-transfer gain through

$$K_O(s) = K_V(s)/s.$$

Then, in control-theory terms, the loop's output phase in terms of its input phase is specified by

$$\theta_O(s)/\theta_R(s) = G(s)/[1 + G(s)H(s)],$$

where

$$G(s) = K_P(s)K_O(s)A(s) = K_P(s)K_V(s)A(s)/s$$

and H(s)=1/N. Here, G(s) equals system forward gain (**Fig 1b**), and H(s) represents feedback-path gain.

Frequency-domain notation, on the other hand, requires some additional definitions:

$\omega_0(s)$=loop output frequency (rad/sec)
$\omega_R(s)$=loop input frequency (rad/sec)
$f_0(s)$=loop output frequency (Hz)
$f_R(s)$ loop input frequency (Hz)
$K_\Phi(s)$=phase-detector transfer gain (V/Hz).

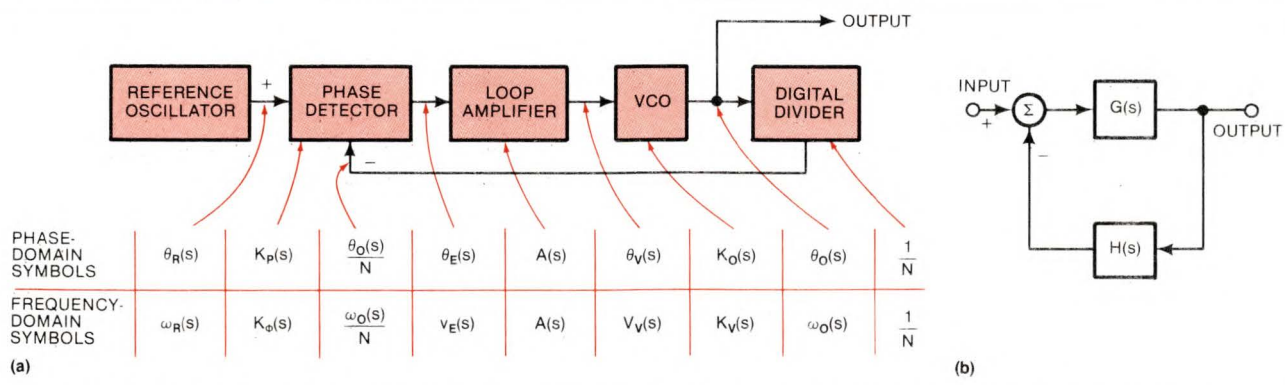

Fig 1—Two sets of nomenclature—*one relating to the frequency domain and the other to the phase domain—can describe a PLL system* ***(a).*** *In* ***(b),*** *G(s) represents the system's forward gain and H(s) equals the feedback gain.*

PLL-subsystem phase-noise level can determine system performance

In terms of frequency, the loop equation now reads

$$f_O(s)/f_R(s) = \omega_O(s)/\omega_R(s) = G'(s)/[1 + G'(s)H(s)],$$

where

$$G'(s) = K_\Phi(s)K_V(s)A(s) = K_P(s)K_V(s)A(s)/s$$

and $K_\Phi(s)=K_P(s)/s$. Thus, $G(s)=G'(s)$, and the transfer functions are identical.

Next, recognize the loop characteristic equation:

$$1 + G(s)H(s) = 0.$$

The highest degree of this equation determines the loop order, and the number of poles of the open-loop transfer function, G(s)H(s), located at the origin determines loop type. (PLLs are generally Type 1 loops because of the finite gains of loop amplifiers and other real-world components.)

With this nomenclature background, note that to change PLL parameters (**Refs 1, 2** and **3** review loop parameters) you can usually only modify A(s). **Fig 2** illustrates typical circuit configurations for changing loop type or order.

Time-domain terms describe phase noise

The output of an oscillator in the time domain is

$$v(t) = [V_O + V_A(t)]\cos[\omega_O(t) + \theta(t)],$$

where V_0 is the average signal amplitude, ω_0 is the signal's average radian frequency, $V_A(t)$ is the signal's instantaneous amplitude fluctuation and $\theta(t)$ is the signal's instantaneous phase fluctuation. Because this article focuses on signal phase properties, assume small amplitude fluctuations—usually a safe assumption because an oscillator's phase noise usually greatly exceeds its amplitude noise at small frequency offsets from the carrier. Furthermore, assume small phase fluctuations.

Now consider a signal with the small phase deviation ϕ_m, phase modulated by a sine wave of frequency ω_m:

$$v(t) = V_O\cos(\omega_O t + \phi_m\sin\omega_m t).$$

This equation expands trigonometrically to

$$v(t) = V_O\{(\cos\omega_O t)[\cos(\phi_m\sin\omega_m t)] - (\sin\omega_O t)[\sin(\phi_m\sin\omega_m t)]\}$$

and, by Bessel functions of the first kind, to

$$v(t) = V_O\{J_0(\phi_m)\cos\omega_O t + J_1(\phi_m)[\cos(\omega_O + \omega_m)t - \cos(\omega_O - \omega_m)t] + J_2(\phi_m)[\cos(\omega_O + 2\omega_m)t + \cos(\omega_O - 2\omega_m)t] + \cdots\},$$

where ϕ_m is the modulation index and $J_0(\phi_m)$, $J_1(\phi_m)$ and $J_2(\phi_m)$ are the Bessel functions. For $\phi_m<0.2$, these equations yield

$$J_1(\phi_m)/J_0(\phi_m) \approx \phi_m/2 \text{ for } \phi_m < 0.2.$$

Because the modulation index ϕ_m equals

$$\phi_m = \Delta f/f_m,$$

where Δf denotes peak frequency deviation,

$$J_1(\phi_m)/J_0(\phi_m) = \Delta f/(2f_m).$$

This expression gives the amplitude of the modulation sidebands in the frequency domain.

If the frequency deviation remains constant and independent of the modulating frequency, sideband

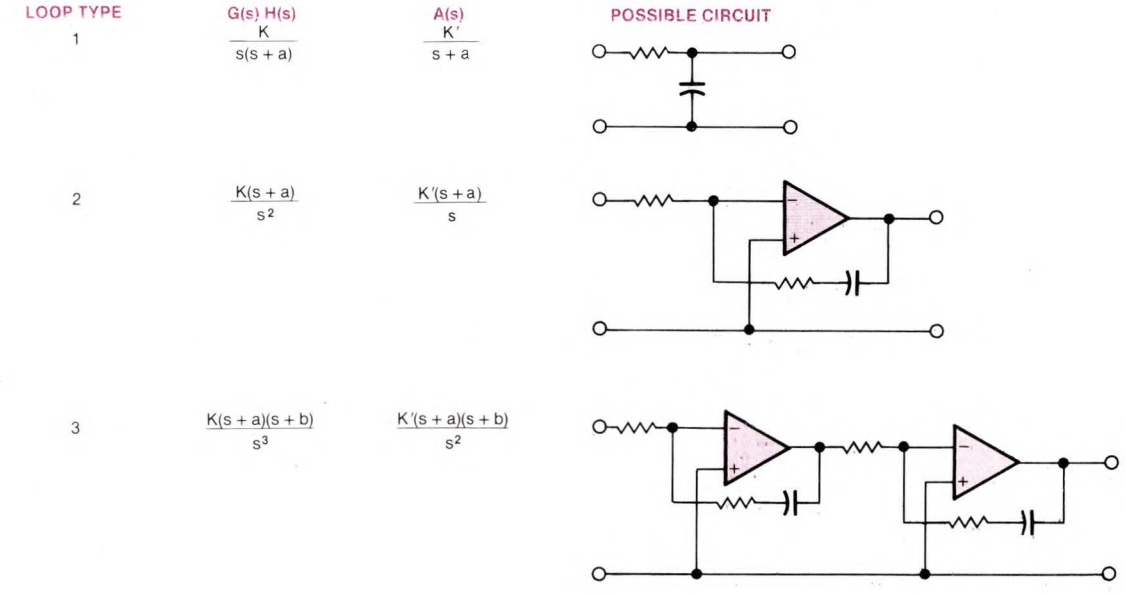

Fig 2—These circuits represent typical configurations *you can choose to change loop type or order. Here, K and K' are constants.*

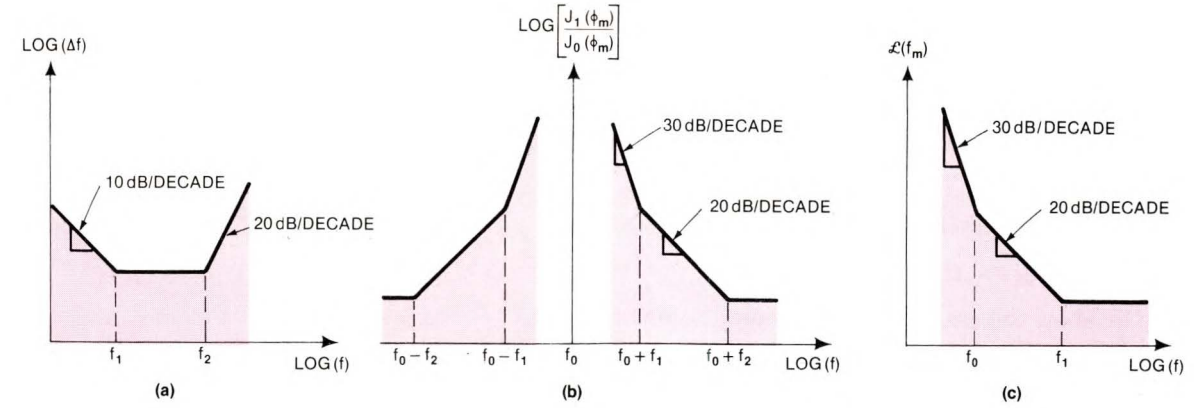

Fig 3—If frequency deviation remains constant *and is independent of modulating frequency, sideband amplitude is inversely proportional to the modulating frequency. Here,* **(a)** *shows the frequency deviation;* **(b),** *the sideband amplitudes;* **(c),** *the single-sideband amplitude.*

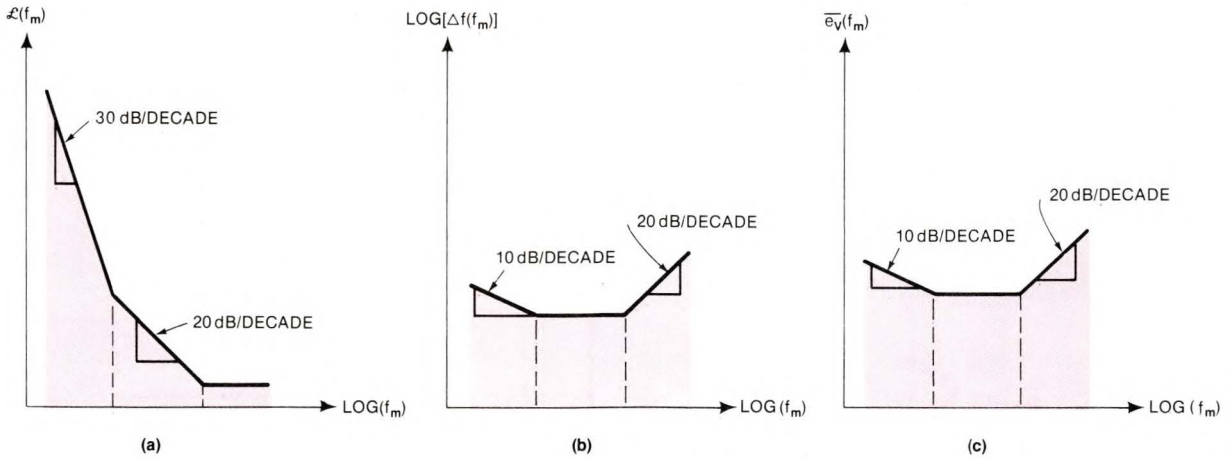

Fig 4—These curves diagram oscillator phase noise: (a) *illustrates the single-sideband phase noise;* **(b),** *the equivalent frequency deviation;* **(c),** *the equivalent input noise voltage.*

amplitude is inversely proportional to the modulating frequency (**Fig 3**). For each frequency f_m, a pair of sidebands—equal in amplitude but opposite in phase—appears symmetrically about the carrier f_0. When amplitude modulated, the carrier has sidebands equal in amplitude and phase. Thus, if a modulated carrier has unsymmetrical sidebands, it's being amplitude and phase modulated simultaneously.

So far this article has dealt with a signal's sinusoidal modulation. To generalize the discussion to noise modulation, note that mathematically noise is a summation of independent components with different frequencies and amplitudes. The average value of noise at any frequency is expressed in rms terms. Thus, you'll find a one-to-one correspondence for noise measured at a given frequency to the noise at that frequency offset from a noise-modulated carrier. This relationship holds true so long as the frequency deviations are sufficiently small and the previous assumptions permitting the Bessel-function expansion thus remain valid.

The usual method of measuring a signal with low-deviation phase modulation is to measure one sideband (because the sidebands have identical amplitudes) in a 1-Hz bandwidth. This signal is referred to by $\mathscr{L}(f_m)$, the ratio of the single-sideband power of the phase or frequency noise in a 1-Hz bandwidth, offset by f_m from the carrier frequency, to total signal power, or, in logarithmic terms

$$\mathscr{L}(f_m) = 20\log[\Delta f/(2f_m)] = 20\log[J_1(\phi_m)/J_0(\phi_m)].$$

This equation expresses signal amplitudes in terms of voltage rather than power.

VCO noise spectra yield frequency deviation

You can measure the phase noise of an oscillator using many different techniques (**Refs 4, 5, 6** and **7**). Here, assume that you already know the oscillator phase noise; **Fig 4** shows an example of such noise. Once you know this noise spectrum, you can calculate the frequency deviation with the foregoing equations. Furthermore, because you know the VCO's input-

Frequency deviation depends on oscillator noise spectra

tuning voltage sensitivity K_V, you can compute an equivalent noise voltage at the VCO input and at a particular offset frequency f_m using

$$\overline{e_V} = \Delta f_{RMS}/K_V.$$

Figs 4b and **4c** show the results of these computations.

With this information, you can model the VCO as a noise-free oscillator with a noise-voltage source at its input. **Fig 5** shows the phase-locked loop with this noise source. The loop's output frequency is given by

$$f_O(s) = \underbrace{\frac{NK_V(s)K_P(s)A(s)}{sN + K_V(s)K_P(s)A(s)} f_R(s)}_{\text{DESIRED TERM}} + \underbrace{\frac{sNK_V(s)}{sN + K_V(s)K_P(s)A(s)} \overline{e_V}(s)}_{\text{CONTAMINATING TERM}}, \quad (1)$$

where the desired term represents the output in a noise-free environment and the contaminating term results from VCO noise.

If you look at only the contaminating term and let $s=j\omega$, you can define frequency deviation as

$$\Delta f_O(j\omega) = \frac{j\omega NK_V(j\omega)}{j\omega N + K_V(j\omega)K_P(j\omega)A(j\omega)} \overline{e_V}(j\omega)$$

$$\text{or } \frac{\Delta f_O(j2\pi f_m)}{f_m}$$

$$= \frac{j2\pi NK_V}{j2\pi f_m N + K_V(j2\pi f_m K_P(j2\pi f_m)A(j2\pi f_m)} \overline{e_V}(j2\pi f_m).$$

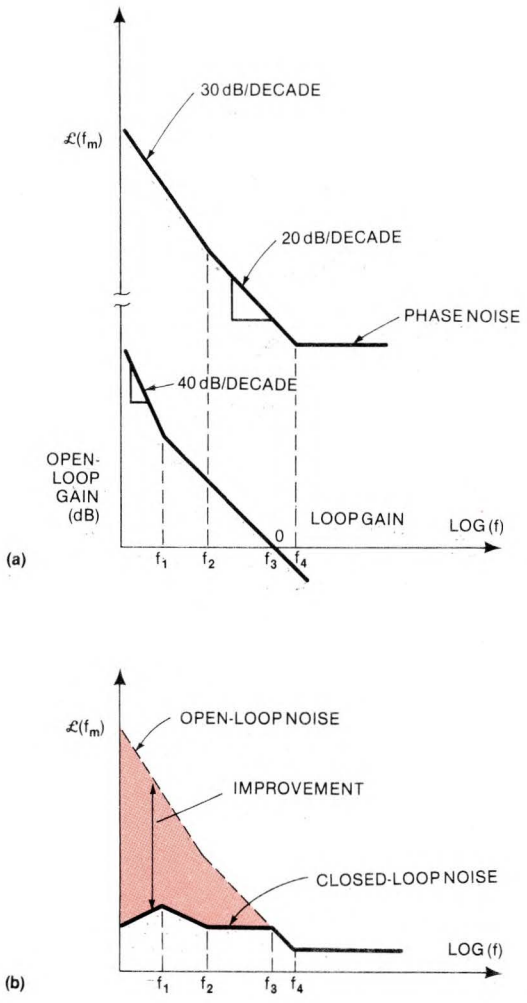

Fig 6—These Bode plots *of open-loop phase noise and gain* ***(a)*** *and closed-loop VCO noise* ***(b)*** *show the reduction of oscillator phase noise inside the loop bandwidth by the available loop gain at any offset frequency.*

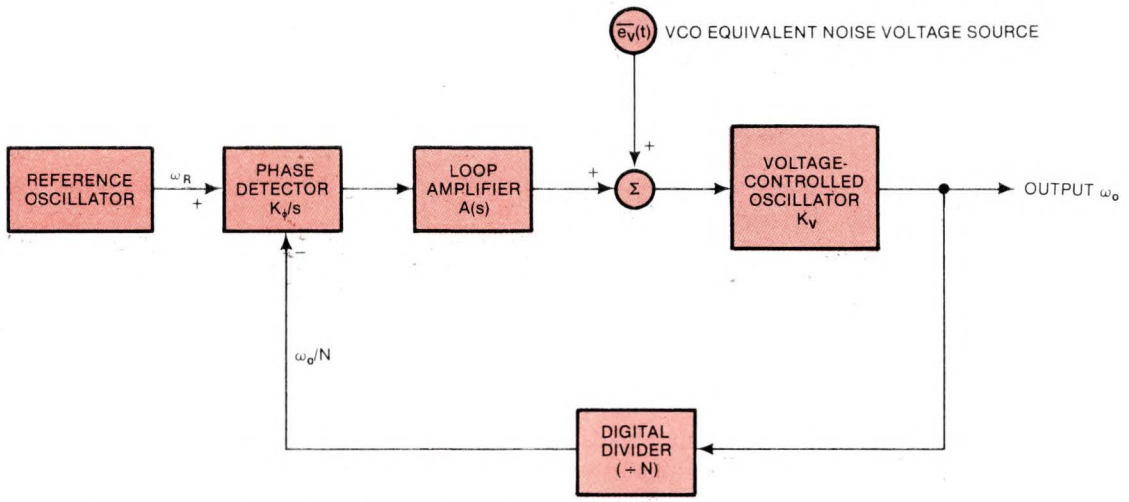

Fig 5—This block diagram of a PLL system *represents the VCO as a noise-free oscillator with a noise-voltage source at its input.*

For a phase-locked VCO, this equation yields phase-noise sideband amplitudes of

$$\mathcal{L}_0^V(f_m) = 20\log\left[\left|\frac{j\pi NK_V}{j2\pi f_m N + K_P K_V A f_m}\right| \overline{e_V}(f_m)\right].$$

Here, the subscript 0 indicates loop output noise, and the superscript V refers to the VCO's noise contribution. Thus, loop properties modify an unlocked oscillator's phase noise.

Now note that

$$\overline{e_V}(f_m) = \Delta f(f_m)/K_V = \mathcal{L}_V(f_m)2f_m/K_V.$$

where $\mathcal{L}_V(f_m)$ is the open-loop VCO noise. You can substitute this equation into the preceding phase-noise equation to yield

$$\mathcal{L}_0^V(f_m) = 20\log\left[\left|\frac{j2\pi f_m N}{j2\pi f_m N + K_P K_V A f_m}\right|\right]\mathcal{L}_V(f_m)$$

$$= 20\log\left[\frac{1}{|1 + G(f_m)H(f_m)|}\right]\mathcal{L}_V(f_m). \quad \textbf{(2)}$$

This equation says that the noise outside the loop bandwidth (defined as the frequency at which G(s)H(s)=1 and also the −3-dB point of the loop's frequency response, assuming no peaking) equals the open-loop VCO noise, and that the oscillator's phase noise inside the loop bandwidth is reduced by the amount of loop gain available at any offset frequency f_m.

Fig 6 shows an example of this effect. Many oscillators in the VHF and higher frequency ranges have low-frequency phase noise with a 30-dB/decade slope. For Type 1 loops, the noise inside the loop bandwidth still has a 10-dB/decade slope. Thus, you might choose a Type 2 loop, which has higher gain at low frequencies, to further reduce oscillator noise. However, if you choose a Type 2 or higher order loop, be careful when placing the loop's poles and zeroes to avoid any loop-gain peaking, which can degrade loop noise performance.

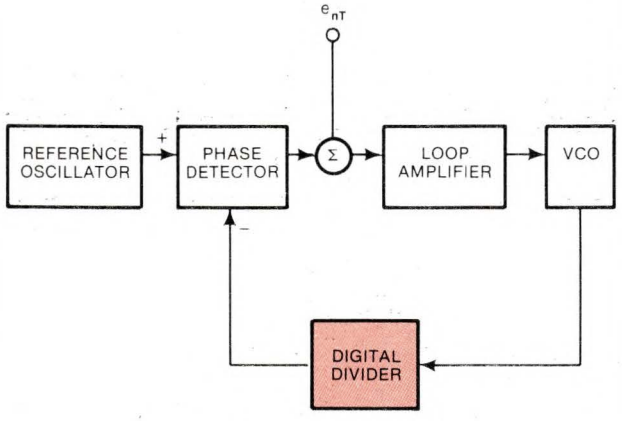

Fig 7—Modeling a loop amplifier *as if it had only a voltage noise source is usually a valid assumption, but you should check the effects of noise currents when loop-amplifier impedance levels are high.*

To summarize, you can reduce open-loop VCO noise only by the amount of loop gain. Noise performance outside the loop bandwidth equals that of an unlocked VCO unless the loop gain has peaking; in this case, the noise is higher.

Low-frequency references provide stability

Because most high-frequency oscillators lack adequate long-term stability, they can't serve as primary oscillators in many frequency synthesizers. Therefore, they are usually phase locked to a lower frequency oscillator designed for good long-term stability. Unfortunately, such oscillators have phase noise that might determine loop noise properties. Consider a reference oscillator: It has some phase noise—expressed in the frequency domain **(Eq 1)** as:

$$\Delta f_0(s) = \frac{NK_V K_P A(s)}{sN + K_P K_V A(s)}\,\Delta f_R(s).$$

Thus, the loop's output-frequency deviation becomes

$$\frac{\Delta f_0(s)}{f_m} = \frac{NK_V K_P A(s)}{sN + K_P K_V A(s)} \cdot \frac{\Delta f_R(s)}{f_m}.$$

After manipulation, the output sideband level as a function of both loop gain and reference noise equals

$$\mathcal{L}_0^R(f_m) = 20\log\left[\frac{|NK_V K_P A(f_m)|}{|j2\pi f_m N + K_P K_V A(f_m)|}\right]\mathcal{L}_R(f_m). \quad \textbf{(3)}$$

$\mathcal{L}_R(f_m)$ refers to the phase noise of the reference oscillator.

This expression says that at low offset frequencies the output noise is merely the reference noise multiplied by the division number N. However, outside the loop bandwidth, noise is not zero but instead the multiplied reference noise reduced by the attenuation provided by the loop outside the loop bandwidth. This attenuation usually has a 1/f term because A(s) is usually independent of frequency for those outside the loop bandwidth. Thus, for a large f_m,

$$\mathcal{L}_0^R(f_m) \approx 20\log\left[\frac{K_V K_P}{2\pi f_m}\,|A(f_m)|\right]\mathcal{L}_R(f_m). \quad \textbf{(4)}$$

You must, therefore, consider not only the loop gain necessary to provide for VCO noise reduction inside the loop bandwidth, but also the effects of the reference noise on the VCO outside the loop bandwidth.

Frequency dividers generate noise

The noise inherent in the frequency divider also contributes to the noise in phase-locked loops. This noise comes from the divider's active devices, but vendors unfortunately seldom specify it. You can measure the noise, but regard your measurements at best as typical, because vendors probably exercise little control over this spec during manufacturing.

Once you estimate the values, though, you can easily see whether the noise affects loop performance. Note that the loop cannot determine whether this noise comes from the phase detector's reference or divided-

Set loop bandwidth to optimize noise at a given offset frequency

VCO input; thus, if divider noise is less than reference noise, the former is not a prime noise contributor. However, if divider noise is greater than reference noise, it might constitute a prime contributor to loop noise. If they are approximately equal, the resultant noise equals their rms sum.

Mathematically, the divider's noise contribution to the loop's output noise is

$$\mathcal{L}_O^D(f_m) = 20\log\left[\left|\frac{NK_VK_PA(f_m)}{j2\pi f_mN + K_PK_VA(f_m)}\right|\right]\mathcal{L}_D(f_m),$$

where $\mathcal{L}_D(f_m)$ is the additional phase noise the divider causes, referred to the divider's output.

Check phase-detector and loop-amplifier noise

Until now, this article has expressed output noise contributions in terms of input- and output-noise spectral densities. This section, however, presents an expression that describes output contributions to loop phase noise based on the measured noise voltages at the phase-detector-output and loop-amplifier-input noise sources. Here, the loop-amplifier model has only a voltage noise source—usually a reasonable assumption, although you should compute the effects of noise currents when the loop amplifier's impedance levels are large. **Fig 7** illustrates a loop with these noises lumped together; all other components are assumed noise free.

The output frequency of such a loop is

$$\omega_O(s) = \underbrace{\frac{NK_VK_PA(s)}{sN + K_VK_PA(s)}\,\omega_R(s)}_{\text{DESIRED TERM}} + \underbrace{\frac{sK_VA(s)N}{sN + K_VK_PA(s)}\,\overline{e_{nT}}(s).}_{\text{UNDESIRED TERM}}$$

If you let $s=j\omega$, define the noise term as

$$\Delta\omega_O(s) = \frac{sNK_VA(s)}{sN + K_VK_PA(s)}\,\overline{e_{nT}}(s).$$

At a particular frequency offset f_m, you can express output noise as

$$\mathcal{L}_O^P(f_m) = 20\log\left[\frac{1}{2}\left|\frac{jNK_VA(f_m)}{j2\pi f_mN + K_VK_PA(f_m)}\right|\overline{e_{nT}}(f_m)\right].$$

This equation shows that for large loop gains (and low frequency), the noise floor is independent of loop gain, as shown by

$$\mathcal{L}_O^P(f_m) \approx 20\log\left[\frac{N}{2K_P}\,e_{nT}(f_m)\right] \text{ for small } f_m. \quad (5)$$

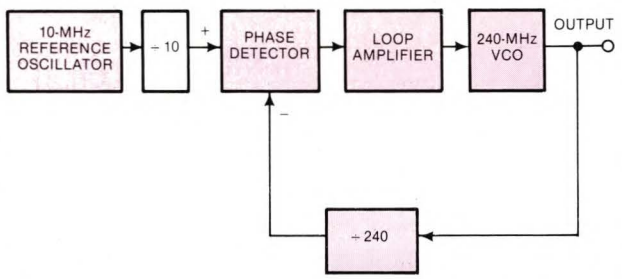

Fig 8—A block diagram of a simple frequency synthesizer *shows the major noise contributors to PLL systems. The near by* ***table*** *lists these components' measured noise.*

Furthermore, for frequency offsets greater than loop bandwidth, the noise falls off at only a 20-dB/decade rate for a flat $\bar{e}_T$, as shown by

$$\mathcal{L}_O^P(f_m) = 20\log\left[\frac{K_V}{4\pi f_m}\left|A(f_m)\right|\,e_{nT}(f_m)\right] \text{ for large } f_m.$$

If this noise limits the loop's noise floor, you can reduce it using three methods: by finding an amplifier with lower input noise or a phase detector with lower noise; by finding a phase detector with a higher gain constant; or by changing the loop's diagram to meet specs.

Example shows noise effects

Thus far, this article has described all major PLL noise contributors. However, many loops include additional components such as circuits to linearize the VCO tuning curve or pretuned circuits to tune the VCO closer to its final value. You can analyze these circuits' noise sources in a manner similar to that described or lump them together with those already reviewed.

Consider an example that shows how the equations presented in this article can predict loop output noise. **Fig 8** shows a block diagram of a frequency synthesizer. The VCO operates at 240 MHz, and frequency step size equals 1 MHz. The **table** shows the measured noise data for the loop components. Assume that the phase detector and op amp have a noise floor of 30 nV/Hz.

To predict loop output noise, first plot the phase noise of the VCO and the frequency reference, both referred to 240 MHz (**Fig 9a**). Notice that the two curves intersect at 4 kHz. Loop bandwidth is usually chosen to make these curves intersect at the loop bandwidth. The loop is assumed to be a Type 2, because the VCO noise falls at a 30-dB/decade rate. Now plot loop gain on the same curve as VCO noise (**Fig 9b**). You can determine VCO closed-loop noise by subtracting loop gain from VCO phase noise. Note the rise in noise inside the loop bandwidth below 800 Hz, until the extra gain of the Type 2 loop comes into effect (from **Eq 2**). Place the zero in the gain function at about one-fifth of the loop bandwidth, thus achieving a fair compromise between high gain at low frequencies and minimizing loop peaking (which would be caused by placing the zero at any higher frequency).

NOISE DATA

OFFSET FREQUENCY (Hz)	$\mathcal{L}(f_m)$ VCO (dBc)	REFERENCE (dBc)	DIVIDER (dBc)
10	22	87	99
100	52	92	115
1000	82	97	124
10,000	112	102	127
100,000	132	102	147

$\overline{e_{VT}} = 30\ nV/\sqrt{Hz}$
$K_P = [0.4/(2\pi)]V/RAD$
$N = 240$

You could plot similar curves for the reference oscillator, based on **Eqs 3** and **4 (Fig 9c)**. Here, loop gain has no effect inside the loop bandwidth; however, the noise outside the loop bandwidth can only be attenuated by the loop attenuation. Calculate the rms sum of the two closed-loop curves—because the noises are uncorrelated—to obtain loop noise performance assuming the rest of the loop is noise free; this represents the best performance for a given loop bandwidth. You can also move the loop bandwidth to optimize noise at a particular offset frequency **(Fig 9d)**.

Unfortunately, the rest of the loop contributes noise. The divider has a negligible effect, as the **table** shows. However, the noise from the phase detector and loop amplifier (assumed to be 30 nV/Hz and flat with no 1/f

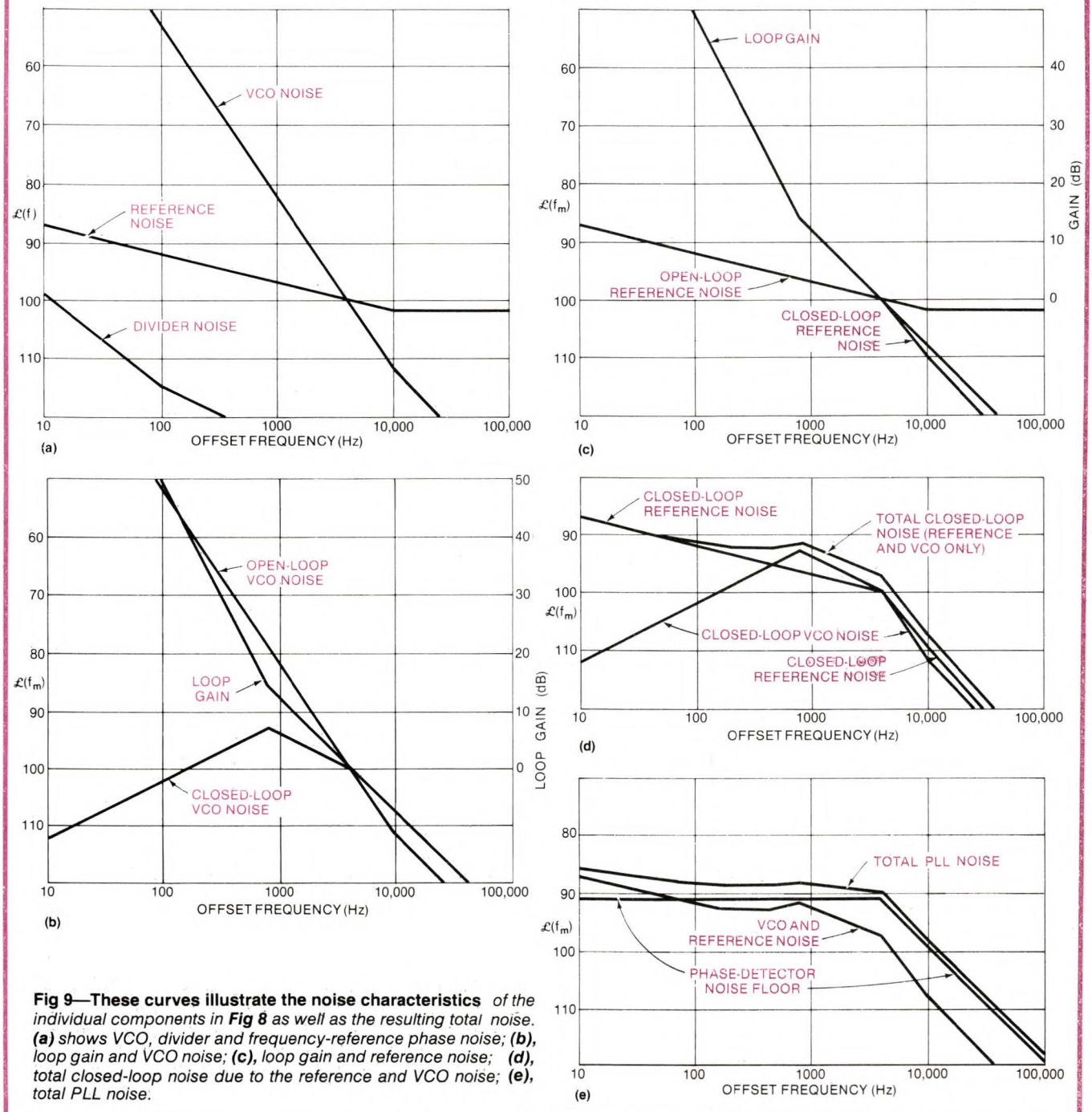

Fig 9—These curves illustrate the noise characteristics *of the individual components in* ***Fig 8*** *as well as the resulting total noise.* ***(a)*** *shows VCO, divider and frequency-reference phase noise;* ***(b),*** *loop gain and VCO noise;* ***(c),*** *loop gain and reference noise;* ***(d),*** *total closed-loop noise due to the reference and VCO noise;* ***(e),*** *total PLL noise.*

Loop attenuation can reduce noise outside loop bandwidth

contribution) result in a loop noise floor of 91 dBc (**Eq 5**). **Fig 9e** shows this effect along with the VCO and reference noise. The phase-detector noise dominates loop noise. You can add these noise curves to find the total noise expected.

Again, to optimize noise at a particular frequency, adjust the loop bandwidth. If the noise performance of this simple loop does not suffice, select lower noise components or design a more complicated loop. **EDN**

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Author's biography

Larry Martin is a consultant dealing with analog and digital circuit and system design. During preparation of this article, he was project manager responsible for spectrum-analyzer design and development at Hewlett-Packard's Santa Rosa Div (Santa Rosa, CA), where he worked for 13 yrs. He holds an MSEE from Stanford University and a BSEE from Kansas State University. In his spare time, Larry enjoys tennis, photography and electronics.

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Operating systems cost more—but they also do more

Updated and recently introduced operating systems reflect their suppliers' efforts to maintain performance parity with advances in 8- and 16-bit μC hardware.

George Kotelly, Senior Editor

Like many other products, microcomputer operating systems (OSs) are more expensive than they were a year ago. But the operating systems listed in this second annual directory also reflect augmented processor, peripheral, memory and file-management capabilities. Thanks to refinements in older versions and increased versatility in new offerings, these 80 operating systems have kept pace with the improved computational power of 8- and 16-bit μCs.

These OSs reflect several trends when compared with the 71 products documented last year (EDN, November 5, 1980, pg 301):

- In processor allocation/management, a swing to multitasking, multiuse and multiprocessing
- In peripheral management, the added capability of handling hard-disk drives
- In memory management, increased system storage capacity along with a focus on memory-protection features
- In file management, increased availability of data security and protection
- In system support, increased accommodation of networking
- In language support, a preference for BASIC, FORTRAN, PASCAL, COBOL and C in that order, with small usage gains or losses for each.

Termed the Apple Disk II housekeeper, *the DOS 3.3 operating system from Apple Computer allows turnkey operation under Apple BASIC. It automatically catalogs files by name; saves, loads, runs, renames, deletes and verifies files; permits sequential and random data access; and helps make backup diskette copies.*

Price is up

Despite the importance of these trends, though, price increases account for the most noticeable change in the operating systems covered again this year. Nearly one-third of these repeats carry a higher price tag. For the majority, the suppliers' increased cost of doing business has merely taken its toll. But in several instances, offerings exhibit extra performance along with their extra cost.

Previously not available in many OSs, such features as network support, hard-disk I/O and storage, multitasking, and additional support languages and target μCs have been incorporated in more than half of the returnees that underwent price increases. For example, network support now comes standard in MICRO COBOL BOS, MP/M II and XENIX; hard-disk I/O in RTE-XL, HDOS and SDOS; multitasking in KOS 5.2 and UCSD P-System; and BASIC and FORTRAN support in SP/ and MSP/8086/Z8000/6800.

Additionally, some OS manufacturers provide added capability at no increase in price. For example, AMIX 3.0 supports seven more μCs than it did last year, CDOS now supplies processor allocation and memory management as standard features, and UMDS supports PASCAL as well as five additional μCs.

More bits for more work

Not surprisingly, operating systems for 16-bit μCs constitute many of the 18 new entrants in the directory. Besides bearing higher prices than OSs available a year ago, they reflect a definite trend toward 16-bit-μC use. Their increased performance entails a small price increment but satisfies users' needs to handle computation and communications simultaneously. Additionally, they represent a move from single-task, single-user versions (such as CP/M and ISIS) to multitask,

New operating systems support more users, tasks and processors

multiuser and—in a few cases—multiprocessor types (such as MP/M and iRMX86).

In fact, 80% of the new entrants feature multitasking capability, whether for 8- or 16-bit μCs. To demonstrate the diversity of multitasking variations available, consider RMS68K, a 16-bit-μC OS. In theory, it handles an unlimited number of tasks, although memory capacity and overhead obviously dictate an upper limit. Another 16-bit-μC OS, ZEUS, accommodates as many as 200 tasks. And yet another offering, REX-80, serves 8- and 16-bit μCs while providing multitasking limited only by memory constraints.

Following on the heels of multitasking as a standard OS capability comes multiple-user support—a characteristic of more than half the new entrants. Again, implementation variations abound. For example, TMS, an 8-bit-μC OS, handles as many as five users and provides at least 1k bytes of RAM for each. ZEUS, however, suits as many as 64 users and furnishes nearly 64k bytes of RAM for each. Another 16-bit-μC offering, CTOS, accommodates as many as 16 users and furnishes a huge 128k bytes min of RAM for each.

Although not as prevalent as multitasking and multiple-user capability, multiprocessing has also made noticeable inroads in OSs. Some 20% of the latest OS introductions support more than one processor. The wave of the future, these OSs allow master-to-master and master-to-intelligent-slave CPUs to conduct traffic over parallel buses.

For example, CTOS supports 8086- and 8087-based μCs using a hardware synchronizing scheme. Embodying even greater capability, REX-80 works with as many as eight processors by means of test-and-set functions and interrupt synchronization. Performance advantages abound in these products because the application splits into more manageable segments for separate and more efficient CPU handling.

Following the same trends established in the directory's upgraded entries, the percentage of recently

Glossary of essential operating-system terms

Allocation (dynamic)—The reassignment of peripherals within a given program

Allocation (static)—The assignment of peripherals to a job

Allocation technique—The method of providing a process with access to a shared resource

Binding—The act of assigning absolute addresses to a program

Blocked list—A catalog of the processes waiting for μP time or for completion of an I/O operation

Blocking—The process of combining more than one record into one block to make data transfers more efficient

Buffering—The process of using areas of memory to isolate I/O devices from one another and from the CPU

Chaining—The ability of an executing program to call another program that resides on disk

COMMON—An area of memory maintained for the purpose of passing data or parameters

Constrained allocation—A resource-allocation strategy that specifies all resources a process will need but does not prevent execution unless a deadlock might occur

Contiguous allocation—An allocation method that assigns adjacent sectors to a file

Deadlock—A condition that exists when a process is blocked in a state and in all future states that the system can reach

Deadly embrace—A situation in which two processes each unknowingly wait for resources held by the other

Device independence—An OS feature that frees the user from considering device-specific details. It employs mnemonics to refer to specific devices; changing these mnemonics redirects I/O to another device

Direct memory access (DMA)—A means of providing fast peripherals with access to memory without going through the CPU

Directory—A file containing information concerning the other files on a mass-storage device; also termed a catalog

Executive—An operating-system routine responsible for decision making

File-control block (FCB)—A data structure in main memory for keeping track of files in use

File-management system—The part of an OS that controls the organization and allocation of disk files, which might consist of one or more sectors

Index—A number representing the relative position of a byte in either a record or file

Interrupt—A break in the normal flow of a system or routine from which flow can resume later

I/O supervisor—The portion of an OS that provides routines for I/O procedures

Job—The collection of activities needed to accomplish a specified amount of work

Linked list—A list formed by tying together (with pointers) several items on a disk

Lock byte—An entity used to represent a resource in synchronization schemes; also termed a semaphore

Memory protection—A method of ensuring that the contents of main memory within certain variable limits are not altered or inadvertently destroyed

Noncontiguous allocation—An allocation method that assigns physically nonadjacent sectors to a file

Nucleus—The most basic level

introduced operating systems incorporating hard-disk support capability exceeds 50%. Additionally, the percentage of new OSs with network support and file protection totals slightly less than 50%; with memory protection, just under 25%.

A move toward 16-bit hardware notwithstanding, most operating systems still serve the large 8-bit-μC marketplace. In fact, 8-bit-μC OSs in the directory outnumber their 16-bit counterparts by 2:1. Additionally, among the new OS entrants, almost half are 8-bit types. In other words, operating systems serving 8-bit μCs still dominate this OS directory and should continue to do so in the near future.

Less popular languages make a move

The breakdown of languages supported by this directory's operating systems shows small losses by the popular languages and small gains by the less commonly used ones. Specifically, BASIC continues to lead the pack; it's available for 66% of the listed OSs—a 2% decrease from last year's total.

Next in popularity, FORTRAN and PASCAL have also dropped slightly in usage: FORTRAN decreased by 2% to 50%, PASCAL by 3% to 48%.

Usage gains, however, occurred in the less popular languages, such as COBOL and C. Rising to 33% usage from 25%, COBOL has apparently benefitted from growth in small-business-system applications. Also reflecting increased user interest, C usage has jumped from 16 to 20%. (This latter increase probably arises because of PASCAL's standardization and portability limitations.) Another less popular language, FORTH, also reflects higher use: it has nudged upward to 13% usage from 11%.

A look around the corner

What do all these developments portend? During the 1980s, VLSI manufacturing techniques will mature and permit the production of μC chips with extremely high densities and many built-in processing functions. As these performance benefits slide into silicon, however, they will present users with untold operational problems. Specifically, with the advent of additional μC processing parameters, functional modes and interface

of an operating system; creates and destroys software processes used to implement abstract processes

Operating system—An organized collection of procedures for operating a computer

Overlaying—The technique of repeatedly using the same blocks of internal storage during different stages of a program; eg, when one routine is no longer needed, another routine can replace all or part of it

Polling procedure—A routine for checking each I/O device sequentially to determine whether it requires servicing

Primitive—An operation provided by a nucleus for use in synchronization

Priority—A parameter designating a task's or process's relative urgency

Process—A computation that can occur concurrently with other computations; an OS's basic unit of computation

Process - control block (PCB)—A data structure that uniquely defines a given process

Program (code)—A set of instructions that tells a computer step by step exactly how to handle a job

Re-entrant code—A program task or routine that can be executed simultaneously by more than one process

Relocation (dynamic)—The act of assigning absolute memory addresses when a program is loaded into memory

Relocation (static)—The act of assigning absolute addresses at linking time

Resource—Any device or item used by a computer, including areas of memory such as buffers

Rotational ordering—A method of organizing I/O requests to a disk to reduce total service time

Segmentation—A technique for managing variable-sized areas of memory, termed segments, that contain logical program parts

Service request—The appeal by a process or task for access to a system resource

Single contiguous allocation—A memory-allocation scheme that assigns all available memory as one block

Spin block—A loop created when a process keeps checking the state of a flag or status bit while waiting for an event to occur

SPOOLing—Simultaneous peripheral operations on line; used to convert a dedicated device into a shared one

Swapping—A technique similar to overlaying; involves moving processes between main memory and auxiliary storage in order to multiplex main memory

Sysgen—System generation, the process by which an operating system is configured out of individual system components to accommodate a particular hardware configuration

Task—A routine that forms the lowest self-contained unit of a job or process

Time slicing—A technique that shares μP time among several processes. The quantum of time allocated to a process is termed a time slice

Transient area—The space in memory available for user programs and system utilities

Urgency—The degree to which a task or process requires attention; determined by the task's or process's priority

Utilities—Routines used in housekeeping functions and I/O.

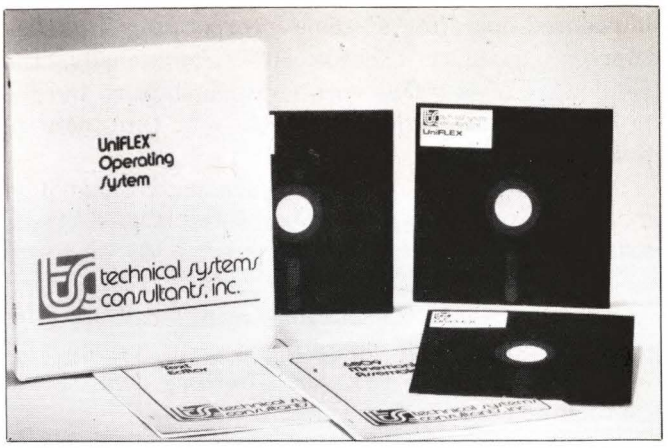
Leading support languages show no clear trends in preference

multiplexing, users will face virtually insurmountable problems when coupling designs to the outside world.

The solution? Future operating systems will be designed into VLSI devices and provide features and architectures that will insulate users from potential application pitfalls. According to Peter Palm, product marketing manager at Intel Corp, these OSs should provide modularity and configurability in the form of standard modules, layers and interfaces. For example, Intel's iRMX86 operating system currently employs object-oriented common-format interfaces to its primitives to manage jobs, tasks and messages. At a higher layer, this operating system offers common device-independent interfaces to device drivers that handle smart floppy- and hard-disk controllers. For an operating system with these built-in capabilities, VLSI implementation thus becomes merely a matter of improving manufacturing capability to a point where silicon fabrication becomes practical.

At a still higher layer, operating systems will soon provide a universal development interface (UDI) to popular languages for program development. They will also furnish a universal run-time interface (URI) to execute these developed programs. Such standard interfaces will permit common μC support languages to run on top of any UDI/URI-compatible operating system. In other words, the interfaces will serve as a standard software bus for different languages and applications.

Operating systems will also soon support local-area networks (such as Ethernet) and global-area networks (such as X.25). They will provide high-level data-link interfaces to an Ethernet controller on the Multibus via an interprocessor protocol, for example, and support standard interfaces with standard modules. Such modules, layers and interfaces should pave the way to overcoming the potential problems of VLSI technology. **EDN**



Influenced by its manufacturer's FLEX and Bell Labs's UNIX, *the UniFLEX operating system from Technical Systems Consultants serves large multitasking and multiuser 6809- or 68000-μP-based systems. It supports a hierarchical file system, permitting files of 1G bytes and disk capacities exceeding 8G bytes.*

Reference

Hemenway, J E, "EDN μC Operating Systems Directory, Chapters 1 through 5," *EDN,* November 5, 1980, pgs 275-300.

Article Interest Quotient (Circle One)
High **473** ***Medium*** **474** ***Low*** **475**

Operating systems come in three key types

This directory classifies OSs in terms of user function. A **development OS,** for example, produces software to run either on the host μC or on another target μC. The target need not incorporate the same μP type if the user develops the software by means of cross assemblers or compilers. Examples of development OSs include Intel's ISIS, Omnibyte's ODOS and Digital Research's CP/M.

A **real-time** or **process-control OS** governs industrial processes that place timing constraints on its responses: Interrupts from these external processes signal the μC system, and if the system doesn't respond in a specified time, the processes become impaired or degraded. Intel's iRMX80 and iRMX86 exemplify such operating systems.

General-purpose OSs usually deal with business or scientific applications. Digital Research's CP/M, for example, finds use in word processing, accounts-receivable generation and mailing-list maintenance.

These OS categories are arbitrary; many OSs in the directory provide capabilities in all three areas. Within each of the three categories, we list the operating systems in alphabetical order.

Another classification cuts across the three categories: You can further describe an OS as a multiuser or single-user system.

To evaluate any of these OS types' suitability for your particular application, look at its ability to carry out its primary management activities: allocating the four main system resources (processor time, memory, peripherals and files) on the basis of user needs and system capabilities. By fully understanding the management features and capabilities listed in the directory for each operating system, you can focus on a few solid candidates. Then contact the OS manufacturers for decision-making details.

8-BIT CPU 8080/8085/Z80 | DEVELOPMENT OPERATING SYSTEM | GENERAL-PURPOSE OPERATING SYSTEM | REAL-TIME OPERATING SYSTEM

CP/M 2.2

Digital Research Inc
Box 579
Pacific Grove, CA 93950
Phone (408) 649-3896

RELEASE DATE: August 1979
PRICE: $150
SUPPORT LANGUAGES: 8080 and Z80 assemblers; APL, BASIC, FORTH and LISP interpreters; BASIC, FORTRAN, C, PASCAL, PL/I and COBOL compilers
SYSGEN PROGRAM: Yes **SOURCE CODE:** Yes
LANGUAGE SYSTEM: 8080 assembler
NETWORK SUPPORT: No

SYSTEM RESIDENCY: RAM
ROMABLE SYSTEM: No
MINIMUM HARDWARE NEEDED: 20k bytes RAM, console and floppy- or hard-disk drive

PROCESSOR ALLOCATION/MANAGEMENT

Not Available

PERIPHERAL MANAGEMENT

- Supports CRTs, character and line printers, floppy- and cartridge-disk drives and modems
- Provides device independence, DMA and spooling
- Accommodates a mix of mass-storage devices

MEMORY MANAGEMENT

- Single contiguous allocation
- Overlays
- Chaining

FILE MANAGEMENT

- Named file system
- Sequential and random organizations
- Allocation type: extents
- Can access file system from HLL containing constructs

CIRCLE NO 711

16-BIT CPU Nova/Micronova | DEVELOPMENT OPERATING SYSTEM | GENERAL-PURPOSE OPERATING SYSTEM | REAL-TIME OPERATING SYSTEM

DOS

Data General Corp
4400 Computer Dr
Westboro, MA 01580
Phone (617) 366-8911

RELEASE DATE: 1977
PRICE: $735
SUPPORT LANGUAGES: Macro assembler, BASIC and Business BASIC interpreters, FORTRAN IV compiler
SYSGEN PROGRAM: Yes **SOURCE CODE:** Yes
LANGUAGE SYSTEM: Macro assembler
NETWORK SUPPORT: X.25, Bisync, HASP and RJE-80 protocols

SYSTEM RESIDENCY: Disk
ROMABLE SYSTEM: No
MINIMUM HARDWARE NEEDED: 64k bytes RAM, console and disk or diskette drive

PROCESSOR ALLOCATION/MANAGEMENT

- Multitasking: 256 tasks can start/stop/suspend other tasks via intertask communication
- Multiusage: up to four users using BASIC or Business BASIC; minimum RAM per user is application dependent
- Synchronizing schemes: semaphore and mailbox

PERIPHERAL MANAGEMENT

- Supports CRTs, character and line printers, floppy- and cartridge-disk drives, modems and magnetic-tape drives
- Provides device independence, DMA, asynchronous and synchronous I/O and A/D and D/A inputs and outputs
- Uses interrupts and I/O multibuffering
- Accommodates a mix of mass-storage devices with up to four controllers

MEMORY MANAGEMENT

- Overlays
- Swapping and chaining
- Static relocation
- Binding during linking time

FILE MANAGEMENT

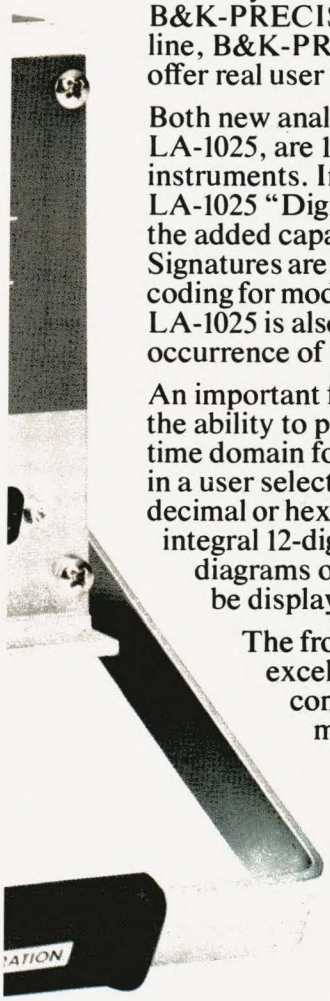
- Named file system and multilevel directory
- Contiguous and random organizations
- Indexed sequential access method (for Business BASIC)
- Allocation type: linked/index
- Can access file system from HLL containing constructs
- Password/security protection (for Business BASIC)

CIRCLE NO 714


ARM
TRIGGER
COMPLETE
LOGIC MODE
LOCATION
DATA
175
C5F7
SIGNATURE
INSTABILITY
SAMPLES
SIGNATURE MODE
SCOPE
SYNC
TRIGGER
EVENT DELAY
CLOCK DELAY
POD ACTIVITY
EVENT
SIGNATURE ANALYZER
INST
HOLD
CONT
STAT
DEC
OCT
BIN HI
BIN LO
LOGIC ANALYZER
MODE
CHANNEL A
HI
TRIGGER BITS
POWER
QUALIFI
A
B
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
B&K PRECISION
LA-1025 DIGITAL SYSTEM ANALYZER

Now the logic is clear... B&K-PRECISION is the new choice for logic analyzers.

Announcing a new line of logic analyzers ready to face all comparisons.



The very latest word in logic analysis is B&K-PRECISION. Not just another "L-A" line, B&K-PRECISION's new instruments offer real user advantages.

Both new analyzers, the LA-1020 and LA-1025, are 16 channel, 20MHz instruments. In addition to logic analysis, the LA-1025 "Digital Systems Analyzer" offers the added capability of signature analysis. Signatures are displayed in industry-accepted coding for modified hexadecimal format. The LA-1025 is also capable of recording the occurrence of unstable signatures.

An important feature of both instruments is the ability to present data in both state and time domain formats. State data is formatted in a user selected code... binary, octal, decimal or hexadecimal and displayed via the integral 12-digit LED display. Timing diagrams of 16 channels by 16 words can be displayed on most oscilloscopes.

The front panel controls provide excellent interactive capability, and complete control over a powerful measurement system. After hearing industry complaints of unnecessarily complex logic analyzer operation, B&K-PRECISION engineers devoted a considerable amount of design time to maximizing the instruments' ease-of-use and efficiency. The results are impressive. Not only is set-up time faster than on competitive instruments, but the new B&K-PRECISION instruments reduce the chance of user set-up errors.

Model LA-1020 $2075 **Model LA-1025 $2475**

A new trigger system was developed for these instruments. An 18-bit pattern recognition trigger is used to initiate storage into the 16-bit x 250 word system memory. Sixteen qualifiable channels are featured, plus two additional qualifiers to aid in meeting unique trigger requirements. Convenient front panel switches select a logic 1, 0 or "DON'T CARE" for all 18 inputs.

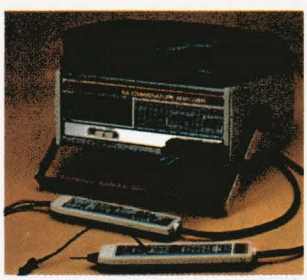
Trigger event and/or clock delays can be rapidly set from 0 to 999. The trigger word may be located anywhere within the 250 word memory. This provides PRE, POST and variable PRE/POST trigger recording.

The LA-1020 and LA-1025 interface to the circuit under test through two Model LP-1, TTL compatible, probes or LP-2 CMOS probes. Trigger capability can be increased to 34 qualifiers by adding the optional LP-3 qualifier expander probe.

An event pulse-output is provided on both analyzers, allowing interconnection of two units to expand system versatility to 32 channels, 67 qualifiers, at speeds to 10MHz.

B&K-PRECISION's LA-1020 and LA-1025 are available now for delivery or demonstration. If you're currently using logic analysis or considering a system, call B&K-PRECISION toll-free at **800/621-4627** for a no-obligation demonstration. It's the only way to see the clear choice.

For service applications, the SA-1010 Signature Analyzer is the time saving choice.



Model SA-1010 $825

(Price includes a set of user ordered probes, additional probes available as accessories).

B&K PRECISION DYNASCAN CORPORATION

6460 W. Cortland Street • Chicago, IL 60635 • 312/889-9087

International Sales, 6460 W. Cortland Street, Chicago, IL 60635 • Canadian Sales, Atlas Electronics, Ontario

For free demonstration Circle no. 68
For additional information Circle no. 69

EDN μC OPERATING SYSTEMS DIRECTORY

8-BIT CPU Z80 | DEVELOPMENT OPERATING SYSTEM | GENERAL-PURPOSE OPERATING SYSTEM | REAL-TIME OPERATING SYSTEM

ISS*

Xycom Inc
750 N Maple Rd
Saline, MI 48176
Phone (313) 429-4971

RELEASE DATE: April 1981
PRICE: Bundled with hardware
TARGET MODEL: Xycom 180, 280, 380 and 390 μC boards and packages
SUPPORT LANGUAGES: Z80 and Z8000 assemblers, PASCAL and FORTRAN 77 compilers
SYSGEN PROGRAM: Yes **SOURCE CODE:** No
LANGUAGE SYSTEM: Assembler and PASCAL
NETWORK SUPPORT: Bisync

SYSTEM RESIDENCY: RAM and disk
ROMABLE SYSTEM: Yes
MINIMUM HARDWARE NEEDED: 60k bytes RAM in development system, 16k bytes RAM in target system, keyboard, CRT and dual floppy-disk drives

PROCESSOR ALLOCATION/MANAGEMENT

- Multitasking: up to 250 tasks can start/stop/suspend other tasks via intertask communication
- Multiprocessing: up to seven processors using software-controlled bus lock, unlock and timeout instructions in CPU hardware
- Synchronizing schemes: regions and events (can implement user's monitors)

PERIPHERAL MANAGEMENT

- Supports CRTs, character and line printers, floppy-disk drives and modems
- Provides device independence and DMA
- Uses interrupts and I/O multibuffering
- Accommodates up to four floppy-disk drives

MEMORY MANAGEMENT

- Single contiguous allocation
- Overlays
- Static and dynamic relocations
- Binding during linking time
- Memory protection

FILE MANAGEMENT

- Named file system
- Sequential, contiguous and random organizations
- Allocation type: single contiguous

COMMENTS: *ISS (Industrial Software System) is UCSD-PASCAL compatible

CIRCLE NO 715

8-BIT CPU Z80/8080/8085 | DEVELOPMENT OPERATING SYSTEM | GENERAL-PURPOSE OPERATING SYSTEM | REAL-TIME OPERATING SYSTEM

I/OS

InfoSoft Systems Inc
25 Sylvan Rd South
Westport, CT 06880
Phone (203) 226-8937

RELEASE DATE: August 1977
PRICE: $225
TARGET MODEL: Z80/8080/8085
SUPPORT LANGUAGES: SAL/RLASM and Intel- and Zilog-type assemblers; BASIC, MBASIC, FORTH, PILOT and MUMPS interpreters; BASIC, FORTRAN, COBOL, PASCAL, C and RATFOR compilers
SYSGEN PROGRAM: Yes **SOURCE CODE:** Yes
LANGUAGE SYSTEM: Assembler
NETWORK SUPPORT: Asynchronous protocols

SYSTEM RESIDENCY: RAM and disk
ROMABLE SYSTEM: No
MINIMUM HARDWARE NEEDED: 24k bytes RAM, 80k bytes floppy disk and terminal

PROCESSOR ALLOCATION/MANAGEMENT

- System vs User mode
- Multitasking: dual tasks handle program and spooler
- Multiusage: structured with task-scheduler modules
- Multiprocessing: via communications network

PERIPHERAL MANAGEMENT

- Supports CRTs, character and line printers, floppy- and cartridge-disk drives and modems
- Provides spooling, DMA and device independence at link-library level
- Uses interrupts and I/O multibuffering
- Accommodates up to 15 disk drives, 65M bytes each, with table-driver handler

MEMORY MANAGEMENT

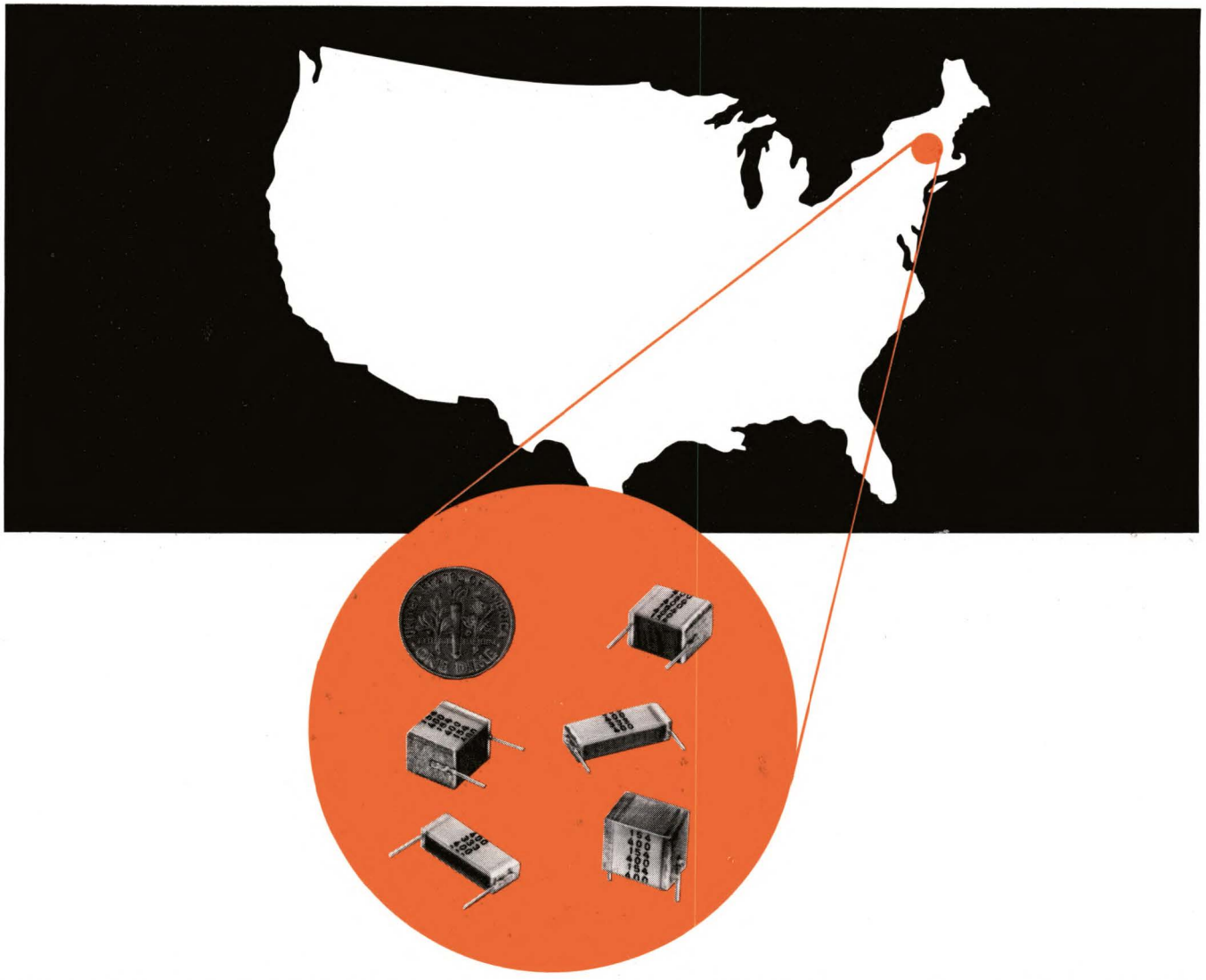
- Single contiguous allocation
- Overlays with program loader
- Chaining
- Static relocation
- Binding during linking time

FILE MANAGEMENT

- Named file system (CP/M compatible)
- Sequential and random organizations
- Module available for ISAM
- Allocation type: extents
- Can access file system from HLL containing constructs

CIRCLE NO 716

Metallized stacked-film capacitors from a NEW prime source: Sprague.



Type 451P standard design now available for automotive, EDP, telecommunication, TV, instrumentation, and industrial control.

There are good reasons for using metallized polyester stacked-film capacitors: high volumetric efficiency, low self-inductance, and high voltage stress capability—*plus* great suitability for printed wiring boards. Small base dimensions and unencapsulated construction keep size to a minimum, while insulating plates provide mechanical protection. Type 451P capacitors are available with capacitance values ranging from .001 μF to 2.2 μF and with voltage ratings of 100, 250, and 400 WVDC. Capacitance tolerance of $\pm$10% is standard . . . $\pm$5% can be ordered at a modest premium.

For detailed technical data, write for Engineering Bulletin 2056 to Technical Literature Service, Sprague Electric Co., 491 Marshall St., North Adams, Mass. 01247.

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CIRCLE NO 49

EDN μC OPERATING SYSTEMS DIRECTORY

8-BIT CPU 8086/8088 | DEVELOPMENT OPERATING SYSTEM | GENERAL-PURPOSE OPERATING SYSTEM | REAL-TIME OPERATING SYSTEM

iRMX 86

Intel Corp
5200 NE Elam Young Parkway
Hillsboro, OR 97123
Phone (503) 640-7147

RELEASE DATE: June 1981
PRICE: $6000 plus use royalty of $300
TARGET MODEL: All 8086/8088 μP types
SUPPORT LANGUAGES: ASM assembler; PL/M, PASCAL and FORTRAN compilers
SYSGEN PROGRAM: Yes **SOURCE CODE:** Yes ($5000 for listings)
LANGUAGE SYSTEM: PL/M and assembler
NETWORK SUPPORT: No

SYSTEM RESIDENCY: RAM and disk
ROMABLE SYSTEM: Yes
MINIMUM HARDWARE NEEDED: 16k bytes RAM, iAPX 86 processor, 8224 clock generator, 8253 timer and 8259A interrupt controller

PROCESSOR ALLOCATION/MANAGEMENT

- Multitasking: unlimited number of tasks can start/stop/suspend other tasks via intertask communication
- Synchronizing schemes; semaphore, mailbox and regions
- Multiprocessing: up to 16 processors on Multibus using shared memory with semaphore and interrupt mechanisms via iMMX software

PERIPHERAL MANAGEMENT

- Supports CRTs and floppy-, hard- and cartridge-disk drives
- Provides device independence and DMA
- Uses interrupts and I/O multibuffering
- Accommodates a mix of single- and double-density disk drives

MEMORY MANAGEMENT

- Single contiguous allocation
- Segmentation
- Static relocation
- Binding during linking, loading and run times

FILE MANAGEMENT

- Named file system and multilevel directory
- Sequential, contiguous and random organizations
- Allocation type: extents
- Can access file system from HLL
- Password/security protection with access lists

COMMENTS: A real-time control executive, iRMX 88 uses device drivers for flat-file system compatibility with iRMX 86; it costs $2000 with use royalty of $200

CIRCLE NO 717

8-BIT CPU Z80A | DEVELOPMENT OPERATING SYSTEM | GENERAL-PURPOSE OPERATING SYSTEM | REAL-TIME OPERATING SYSTEM

KOS 5.2*

Kontron Electronics Inc
630 Price Ave
Redwood City, CA 94063
Phone (415) 361-1012

RELEASE DATE: May 1981
PRICE: Depends on configuration
TARGET MODEL: PSI 80
SUPPORT LANGUAGES: Z80, 8080 and 8085 assemblers; BASIC interpreter; BASIC, FORTRAN, PASCAL, COBOL and FORTRAN compilers; FORTH
SYSGEN PROGRAM: Not required** **SOURCE CODE:** No
LANGUAGE SYSTEM: Z80/ASM code
NETWORK SUPPORT: Yes

SYSTEM RESIDENCY: RAM and disk
ROMABLE SYSTEM: No
MINIMUM HARDWARE NEEDED: 64k bytes RAM, 16k bytes video-refresh memory, video controller and floppy-disk controller

PROCESSOR ALLOCATION/MANAGEMENT

- Multitasking: single foreground task, up to 10 background tasks

PERIPHERAL MANAGEMENT

- Supports CRTs, character and line printers, floppy- and hard-disk drives and modems
- Provides device independence, DMA and spooling
- Uses interrupts
- Accommodates a mix of 5M- and 10M-byte Winchester drives and 5¼-in. floppy-disk drives

MEMORY MANAGEMENT

- Overlays
- Binding during loading time

FILE MANAGEMENT

- Named file system
- Random organization
- Allocation type: linked list of sectors
- Can access file system from HLL

COMMENTS: *KOS 5.2 is CP/M compatible. **Logical drivers are dynamically allocated and relocatable

CIRCLE NO 718

FEATURES

- Accomodates 4096 tasks.
- Priority scheduling algorithm.
- Interrupt-controlled input/output.
- Input/output drivers: Console Driver is standard. Other drivers-Line Printer, Floppy Disk, and Interphase SMD - available as options.
- MTOS-86MP handles up to 16 (8086 and 8088) processors on Multibus. Programs written as if single processor is used. Can be used so as to minimize contention for shared memory. To the programmer MTOS-86 and MTOS-86MP are identical: only the MTOS knows how many CPU boards are present.
- Memory management: Allows up to 32 memory pools whose space can be allocated and deallocated as required.
- Dynamic debugging package: Allows user to set break points, inspect and change memory, and control task execution.
- PL/M interface: Full services available to user programs written in PL/M language.
- Configurability: Runs on any 8086/8088 configuration. Only hardware required is clock for periodic interrupts.
- Compactness: MTOS-86 requires 8KB of storage; MTOS-86MP requires 10KB. (drivers, file system, require additional storage).

SERVICES

- Allocate (de-allocate) memory block
- Enter or exit controlled program
- Change priority
- Perform discrete I/O
- Pause for a given time
- Cancel pause
- Terminate task with timed re-start
- Terminate task with no re-start
- Start task; queue task if active
- Start task if dormant
- Send message to mailbox
- Receive message from mailbox
- Set (reset, test) event flag group
- Set event flag group after elapsed time
- Wait for event flags to be set
- Set (reset, test) semaphore
- Request I/O
- Get Date and time
- Set Date and time

TIMINGS FOR SERVICES IN MILLISECONDS

Allocate memory block	0.46
Send message	0.48
Receive message	0.54
Release memory block	0.56
Pause	0.48
Discrete I/O	0.44
Test semaphore	0.51
Change priority	0.48

THE MTOS™ FAMILY OF MICRO-PROCESSOR OPERATING SYSTEMS

86 MTOS 86MP

LANGUAGE

All MTOS products are distributed in source program form.

LICENSING POLICY

A licensee is entitled to embed object versions of MTOS in licensee's products without further charge.

Other members of the MTOS family are

MTOS-68, MTOS-80, MTOS-80MP, MTOS-68K

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100 Jericho Quadrangle
Jericho, New York 11753

iPi Industrial Programming Inc.
Software specialists since 1963

(516) 938-6600 Telex: 429808

Belgium: BETEA S.A., Chaussee de Louvain, 775, B-1140 Brussels, Phone: (02) 736 80 50, Tlx 846-23188
France: CELDIS SA, 53 Rue Charles Frerot, 94250 Gentilly, Phone: 546.13.13, Tlx 842-200485
Germany: ALFRED NEYE-ENATECHNIK, Schillerstrasse 14, 2085 Quickborn (Hamburg), Phone: 041 06 / 612-240, Tlx 841-213590
India: SARAS ELECTRONICS, N-47, Greater Kailash—I, New Delhi—110048, Phone: 698074, Tlx 011-3532
Israel: CONTAHAL LTD., 54 Ibn Gvirol St., Tel Aviv, 64364, Phone: (03) 269 379, Tlx 922-33654
Japan: TOKYO ELECTRON LIMITED, Shinjuku Nomura Bldg. 1-26-2 Nishi-Shinjuku, Shinjuku-Ku, Tokyo 160, Phone: 03-344-5893, Tlx 781-2322240
Netherlands: C.N. ROOD B.V., Cort v.d. Lindenstraat 11-13, Postbus 42, 2280 AA Rijswijk, Nederland, Phone: 070-996360, Tlx 844-31238
Scandinavia: FRONTEC MICRODATORCENTRUM AB, Box 204, Malmvagen 28, Sollentuna, Sweden, Phone: 08-359360, Tlx 854-15130
Switzerland: XMIT AG, Bellikonerstrasse 218, CH-8967 Widen, Phone: 057-54656, Tlx 845-59955
UK: HAWKER SIDDELEY DYNAMICS ENGINEERING LTD., Manor Road, Hatfield, Herts. AL10 9LP, Phone: (7072) 73439, Tlx 851-24835

CIRCLE NO 48

EDN μC OPERATING SYSTEMS DIRECTORY

8/16-BIT CPU
8 μCs, μPs*

DEVELOPMENT OPERATING SYSTEM

GENERAL-PURPOSE OPERATING SYSTEM

REAL-TIME OPERATING SYSTEM

MICRO COBOL BOS

CAP-CPP Services Inc
521 Fifth Ave
New York, NY 10175
Phone (212) 599-7000

RELEASE DATE: November 1978
PRICE: From $600
TARGET MODEL: >10 processor types
SUPPORT LANGUAGES: Most processors' assemblers; Micro COBOL compiler
SYSGEN PROGRAM: Yes **SOURCE CODE:** No
LANGUAGE SYSTEM: Micro COBOL plus assembler
NETWORK SUPPORT: Yes

SYSTEM RESIDENCY: RAM and disk
ROMABLE SYSTEM: Partially
MINIMUM HARDWARE NEEDED: 48k bytes RAM, 250k bytes each in dual floppy-disk drives and hard copier

PROCESSOR ALLOCATION/MANAGEMENT
- Multitasking: foreground/background tasks can start/stop/suspend other tasks via job management and intertask communication
- Multiusage: hardware dependent
- Multiprocessing: hardware dependent

PERIPHERAL MANAGEMENT
- Supports CRTs, character and line printers, floppy-, hard- and cartridge-disk drives and modems
- Provides device independence, DMA and spooling
- Uses interrupts and I/O multibuffering
- Accommodates a mix of floppy- and hard-disk drives

MEMORY MANAGEMENT
- Single contiguous allocation and overlays
- Swapping, chaining and segmentation
- Static and dynamic relocations
- Binding during linking time
- Memory protection

FILE MANAGEMENT
- Named file system
- Sequential, contiguous and random organizations
- Indexed sequential access method (ISAM)
- Can access file system from HLL containing constructs
- Password/security protection
- Database management

COMMENTS: *Series/1, LSI-11, 8080, 8085, 8086, Z80, 6800, 9900 and 68000

CIRCLE NO 719

8-BIT CPU
8080/8085/Z80

DEVELOPMENT OPERATING SYSTEM

GENERAL-PURPOSE OPERATING SYSTEM

REAL-TIME OPERATING SYSTEM

MP/M II

Digital Research Inc
Box 579
Pacific Grove, CA 93950
Phone (408) 649-3896

RELEASE DATE: August 1981
PRICE: $400
SUPPORT LANGUAGES: 8080 and Z80 assemblers; APL, BASIC, FORTH and LISP interpreters; BASIC, C, COBOL, FORTRAN, PASCAL and PL/I compilers
SYSGEN PROGRAM: Yes **SOURCE CODE:** Yes
LANGUAGE SYSTEM: 8080 assembler
NETWORK SUPPORT: Yes

SYSTEM RESIDENCY: RAM
ROMABLE SYSTEM: No
MINIMUM HARDWARE NEEDED: 32k bytes RAM (master station), console, floppy- or hard-disk drive and real-time clock

PROCESSOR ALLOCATION/MANAGEMENT
- Multitasking: unlimited number of tasks can start/stop/suspend other tasks via queue-based intertask communication
- Multiusage: 16 users
- Synchronizing schemes: flags, queues and poll list

PERIPHERAL MANAGEMENT
- Supports CRTs, character and line printers, floppy- and hard-disk drives, modems and magnetic-tape drives
- Provides device independence, DMA and spooling
- Uses interrupts and I/O multibuffering
- Accommodates a mix of mass-storage devices via table-driven disk definition

MEMORY MANAGEMENT
- Single contiguous allocation
- Chaining and segmentation
- Static and dynamic relocations
- Memory protection

FILE MANAGEMENT
- Named file system
- Sequential and random organizations
- Allocation type: extents
- Can access file system from HLL containing constructs
- Password/security protection
- Time and date stamping on files

CIRCLE NO 711

74LS. CMOS. SPI.

SPI's 74LS Devices In CMOS

SPI gives you 20 new reasons to celebrate.

If you're a system designer, you know that CMOS is the process of the 80s. And SPI is the CMOS innovator. We've taken 20 of the most popular 74LS devices and manufactured them in CMOS — to give you low power and increased system performance.

Our 74SC components are pin-for-pin compatible, direct plug-in replacements for low power Schottky devices. But you also get the advantages of CMOS: significantly lower power, higher noise immunity, full TTL compatibility (input and output) and the same high speed.

Best of all, they are available now at prices that will surprise you.

SPI CMOS Makes It Possible

Our 74SC devices are fabricated using a proprietary selective oxidation silicon gate process we call SPI CMOS. It's the same advanced technology that we use in our 500- and 1000-gate uncommitted logic arrays, so you know it's been proven where it counts — in the field.

SPI's new family of 74SC components covers the range of the most widely used devices. Decoders. Multiplexers. Octal drivers. Transceivers. Flip-Flops. Latches. All are direct plug-in replacements designed to solve marginal performance problems in existing designs. Or, with an eye on the future, you can design in the building blocks for tomorrow's high-speed, low-power CMOS systems.

Put SPI's CMOS 74SC products to work in existing applications where high-noise immunity and/or low power is desirable. And that's just the beginning.

On The Shelf Now

You can start using SPI's CMOS 74SC products today because they're available now. 74SC in CMOS from SPI — don't settle for anything less. Put more into your system right now and stay ahead with SPI CMOS — the process of the 80s. Call or write SPI for more information, before your competition does.

- SP74SC137 1 of 8 Inverting Decoder with Input Latches
- SP74SC138 1 of 8 Inverting Decoder
- SP74SC139 Dual 1 of 4 Inverting Decoder
- SP74SC237 1 of 8 Decoder with Input Latches
- SP74SC238 1 of 8 Decoder
- SP74SC239 Dual 1 of 4 Decoder
- SP74SC240 Octal Inverting Buffer
- SP74SC241 Octal Buffer
- SP74SC244 Octal Buffer
- SP74SC245 Octal Transceiver
- SP74SC373 Octal Transparent Latch
- SP74SC374 Octal D-Type Flip-Flop
- SP74SC533 Octal Inverted Output, Transparent Latch
- SP74SC534 Octal Inverted Output, D-Type Flip-Flop
- SP74SC540 Octal Buffer
- SP74SC541 Octal Buffer
- SP74SC563 Octal Inverted Output, Transparent Latch
- SP74SC564 Octal Inverted Output, D-Type Flip-Flop
- SP74SC573 Octal Transparent Latch
- SP74SC574 Octal D-Type Flip-Flop

SPI SEMI PROCESSES INC.

1885 Norman Avenue, Santa Clara, CA 95050, Tel: (408) 988-4004
TWX: 910-338-0025 SPI SNTA

SPI in Europe: Semi Processes Inc., Austin House, South Bar, Banbury, Oxfordshire, England, Tel: (44)-295-61138 Telex: 837594

CIRCLE NO 50

16-BIT CPU 8086 | DEVELOPMENT OPERATING SYSTEM | GENERAL-PURPOSE OPERATING SYSTEM | REAL-TIME OPERATING SYSTEM

MP/M-86

Digital Research Inc
Box 579
Pacific Grove, CA 93950
Phone (408) 649-3896

RELEASE DATE: September 1981
PRICE: $400
SUPPORT LANGUAGES: 8086 ASM, PL/I, BASIC, FORTRAN, COBOL, PASCAL and FORTH
SYSGEN PROGRAM: Yes **SOURCE CODE:** No
LANGUAGE SYSTEM: 8086 ASM
NETWORK SUPPORT: Yes

SYSTEM RESIDENCY: RAM
ROMABLE SYSTEM: No
MINIMUM HARDWARE NEEDED: 64k bytes RAM, console, floppy- or hard-disk drive and real-time clock

PROCESSOR ALLOCATION/MANAGEMENT
- Multitasking: unlimited number of tasks can start/stop/suspend other tasks via queue-based intertask communication
- Multiusage: 256 users
- Synchronizing scheme: flags, queues and poll list

PERIPHERAL MANAGEMENT
- Supports CRTs, character and line printers, floppy- and hard-disk drives, modems and magnetic-tape drives
- Provides device independence, DMA and spooling
- Uses interrupts and I/O multibuffering
- Accommodates a mix of mass-storage devices via table-driven disk definition

MEMORY MANAGEMENT
- Dynamic memory allocation
- Chaining and segmentation
- Static and dynamic relocations
- Memory protection

FILE MANAGEMENT
- Named file system
- Sequential and random organizations
- Allocation type: extents
- Can access file system from HLL containing constructs
- Password/security protection
- Time and data stamping on files

CIRCLE NO 711

16-BIT CPU Nova 4/Micronova | DEVELOPMENT OPERATING SYSTEM | GENERAL-PURPOSE OPERATING SYSTEM | REAL-TIME OPERATING SYSTEM

MP/OS

Data General Corp
4400 Computer Dr
Westboro, MA 01580
Phone (617) 366-8911

RELEASE DATE: May 1979
PRICE: $1995
TARGET MODEL: DG MP/100/200, MBC/2/3
SUPPORT LANGUAGES: Macro assembler; MP/PASCAL and MP/FORTRAN IV compilers
SYSGEN PROGRAM: Yes **SOURCE CODE:** Yes
LANGUAGE SYSTEM: Macro assembler and MP/PASCAL
NETWORK SUPPORT: Asynchronous and bisynchronous drivers

SYSTEM RESIDENCY: RAM and disk
ROMABLE SYSTEM: Yes
MINIMUM HARDWARE NEEDED: 2k bytes RAM, 4k bytes PROM, for development system—64k bytes RAM, console and floppy disk or diskette

PROCESSOR ALLOCATION/MANAGEMENT
- Multitasking: up to 256 tasks can start/stop/suspend other tasks via intertask communication
- Multiusage: via multitasking (application dependent)
- Synchronizing schemes: semaphore and mailbox

PERIPHERAL MANAGEMENT
- Supports CRTs, character and line printers, floppy- and cartridge-disk drives, modems, magnetic-tape drives and synchronous and asynchronous ports
- Provides device independence and DMA
- Uses interrupts and I/O multibuffering
- Accommodates a mix of mass-storage devices by supporting up to eight different controllers

MEMORY MANAGEMENT
- Overlays
- Swapping and chaining
- Segmentation and static relocations
- Binding during linking time
- Memory protection

FILE MANAGEMENT
- Named file system and multilevel directory
- Random organization
- Indexed sequential access method (ISAM)
- Allocation type: indexed/element structure
- Can access file system from HLL containing constructs

COMMENTS: MP/OS is compatible with AOS on Eclipse processors and AOS/VS on MV/8000 32-bit Eclipse systems.

CIRCLE NO 721

GET IN ON THE "GREAT GATOR GIVE-AWAY"

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HARRIS

EDN μC OPERATING SYSTEMS DIRECTORY

8-BIT CPU Z80 | DEVELOPMENT OPERATING SYSTEM | GENERAL-PURPOSE OPERATING SYSTEM | REAL-TIME OPERATING SYSTEM

MSOS

Monolithic Systems Corp
14 Inverness Dr
Englewood, CO 80112
Phone (303) 770-7400

RELEASE DATE: January 1978
PRICE: $900
TARGET MODEL: MSC 8001/8004/8007/8009
SUPPORT LANGUAGES: MSC assembler
SYSGEN PROGRAM: No
SOURCE CODE: Yes
LANGUAGE SYSTEM: Z80 assembly
NETWORK SUPPORT: No

SYSTEM RESIDENCY: EPROM
ROMABLE SYSTEM: Yes
MINIMUM HARDWARE NEEDED: 16k bytes RAM, CPU and floppy-disk drive

PROCESSOR ALLOCATION/MANAGEMENT
- System vs User mode

PERIPHERAL MANAGEMENT
- Supports CRTs, character and line printers and floppy-disk drives
- Provides device independence
- Uses interrupts and I/O multibuffering

MEMORY MANAGEMENT
- Single contiguous allocation
- Swapping and chaining
- Static and dynamic relocations
- Binding during assembly/compilation time
- Memory protection

FILE MANAGEMENT
- Named file system
- Multilevel directory
- Sequential organization
- Indexed sequential access method (ISAM)
- Allocation type: linked list of sectors

CIRCLE NO 722

16-BIT CPU 8086/Z8000/68000 | DEVELOPMENT OPERATING SYSTEM | GENERAL-PURPOSE OPERATING SYSTEM | REAL-TIME OPERATING SYSTEM

MSP/8086/Z8000/68000

Hemenway Associates Inc
101 Tremont St
Boston, MA 02108
Phone (617) 426-1931

RELEASE DATE: January 1981
PRICE: $900
TARGET MODEL: Various
SUPPORT LANGUAGES: Macro assembler and linking loader; PASCAL/I compiler; BASIC and FORTRAN
SYSGEN PROGRAM: Yes
SOURCE CODE: Yes
LANGUAGE SYSTEM: Assembler
NETWORK SUPPORT: No

SYSTEM RESIDENCY: Ram and disk
ROMABLE SYSTEM: No
MINIMUM HARDWARE NEEDED: 32k bytes RAM, console, real-time clock and floppy-disk drive

PROCESSOR ALLOCATION/MANAGEMENT
- System vs User mode
- Multitasking: unlimited number of tasks can start/stop/suspend other tasks via intertask communication
- Synchronizing schemes: mailbox and monitors

PERIPHERAL MANAGEMENT
- Supports CRTs, character and line printers, floppy- and cartridge-disk drives, modems, magnetic- and paper-tape drives and other devices via suitable device drivers
- Provides device independence, DMA and spooling
- Uses interrupts and I/O multibuffering
- Accommodates a mix of floppy- and hard-disk drives

MEMORY MANAGEMENT
- Overlays
- Chaining and static relocation
- Segmentation (depends on processor)
- Binding during linking time
- Memory protection (depends on hardware)

FILE MANAGEMENT
- Named file system
- Sequential and random organizations
- Allocation type: linked list of sectors
- Can access file system from HLL containing constructs
- Password/security protection

CIRCLE NO 723

We've extended the capacitance ranges of our NPO Ceramic Capacitors

(And reduced the prices)

Vitramon, Incorporated has taken a bold step to curb inflation and lower your component costs.

We've increased the capacitance ranges of our NPO monolithic ceramic chip and "VP" Radial-lead Capacitors — and reduced prices below 1980 levels. (So you'll receive more capacitance for your money.)

A new, high-quality dielectric system has enabled us to increase the capacitance ranges from 50% to 160% on our 11 body sizes of "VEE JEM" NPO Chip Capacitors. The versatile "VP" Ceramic Capacitor series is also available with similar capacitance increases.

For example, the smallest chip body size was increased from 150 pF to 390 pF — the largest from 18,000 pF to 27,000 pF.

The NPO is the most stable dielectric used in monolithic ceramic capacitors: a 0 ± 30 ppm/°C T.C., a maximum dissipation factor of 0.1% — virtually no capacitance change when subjected to voltage, frequency, temperature or time.

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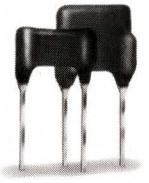
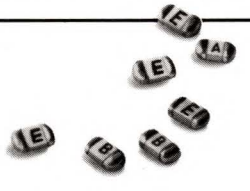


Type	Part No.	Vdc	Old Range (pF)	New Range (pF)
"VP" Radial-Lead	VP12	100	1-1800	1-3900
	VP12	50	2000-3900	100-4700
	VP22	100	180-1800	10-3900
	VP22	50	2400-3900	180-5600
	VP23	100	2400-10,000	4700-15,000
	VP23	50	11,000-15,000	4700-22,000
CHIP	VJ0504		10-150	1-390
	VJ0805		1-680	1-1000
	VJ0905		10-680	1-1200
	VJ0907		620-1100	10-1800
	VJ1505		680-1300	47-2200
	VJ1805		620-1600	180-2700
	VJ1210		1300-3900	220-4700
	VJ1808		1500-3900	680-5600
	VJ1812		1500-6800	470-.01 μF
	VJ2321		6200-15,000	1200-.022 μF
	VJ2224		6800-18,000	1200-.027 μF



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CIRCLE NO 51

8/16-BIT CPU 8080/68000 | DEVELOPMENT OPERATING SYSTEM | GENERAL-PURPOSE OPERATING SYSTEM | REAL-TIME OPERATING SYSTEM

MULTI-FORTH

Creative Solutions Inc
14625 Tynewick Terrace
Silver Spring, MD 20906
Phone (301) 598-5805

RELEASE DATE: December 1979
PRICE: $1500 to $5000
SUPPORT LANGUAGES: 8080 and 68000 assemblers; FORTH contains interpreter and compiler
SYSGEN PROGRAM: Yes **SOURCE CODE:** Yes
LANGUAGE SYSTEM: FORTH
NETWORK SUPPORT: Yes

SYSTEM RESIDENCY: RAM and disk
ROMABLE SYSTEM: Yes
MINIMUM HARDWARE NEEDED: 16k bytes RAM, one floppy-disk drive

PROCESSOR ALLOCATION/MANAGEMENT

- System vs User mode
- Multitasking: up to 64 tasks can start/stop/suspend other tasks via intertask communication
- Multiusage: up to 10 users, with 512 bytes (min) RAM per user
- Synchronizing schemes: semaphore, mailbox and monitors

PERIPHERAL MANAGEMENT

- Supports CRTs, character and line printers, floppy- and hard-disk drives, modems and magnetic-tape drives
- Provides device independence and spooling
- Uses interrupts and I/O multibuffering
- Accommodates a mix of mass-storage devices via virtual disk-access scheme

MEMORY MANAGEMENT

- Single contiguous allocation
- Overlays
- Swapping and chaining
- Binding during assembly/compilation, linking and loading times

FILE MANAGEMENT

- Named file system and multilevel directory
- Sequential, contiguous and random organizations
- Allocation type: single contiguous
- Can access file system from HLL containing constructs
- Password/security protection

CIRCLE NO 724

8-BIT CPU Z80/8080/8085 | DEVELOPMENT OPERATING SYSTEM | GENERAL-PURPOSE OPERATING SYSTEM | REAL-TIME OPERATING SYSTEM

MULTI/OS

InfoSoft Systems Inc
25 Sylvan Rd South
Westport, CT 06880
Phone (203) 226-8937

RELEASE DATE: June 1981
PRICE: $900
TARGET MODEL: Z80/8080/8085
SUPPORT LANGUAGES: SAL/RLASM and Intel- and Zilog-type assemblers; BASIC, MBASIC, FORTH, PILOT and MUMPS interpreters; BASIC, FORTRAN, COBOL, PASCAL, C and RATFOR compilers
SYSGEN PROGRAM: Yes **SOURCE CODE:** Yes
LANGUAGE SYSTEM: Assembler and C
NETWORK SUPPORT: Asynchronous protocols

SYSTEM RESIDENCY: RAM and disk
ROMABLE SYSTEM: No
MINIMUM HARDWARE NEEDED: 48k bytes RAM, 160k bytes floppy disk and terminal

PROCESSOR ALLOCATION/MANAGEMENT

- System vs User mode
- Multitasking: 1 to 16 tasks
- Multiusage: console programs or background phantom jobs
- Multiprocessing: via communications network

PERIPHERAL MANAGEMENT

- Supports CRTs, character and line printers, floppy- and cartridge-disk drives and modems
- Provides spooling, DMA and device independence at link-library level
- Uses interrupts and I/O multibuffering
- Accommodates up to 15 disk drives, 65M bytes each, with table-driven handler

MEMORY MANAGEMENT

- Multiple contiguous allocations
- Overlays with program loader
- Chaining
- Static or load-time relocation
- Binding during linking time

FILE MANAGEMENT

- Named file system (CP/M compatible)
- Sequential and random organizations with sub-directories
- Module available for ISAM
- Allocation type: 1k, 2k, 4k or 8k clusters
- Can access file system from HLL containing constructs

CIRCLE NO 712

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- Trends in Switching Power Supply Designs
- Extensions of HF Power Switching techniques to new areas of interest (e.g., motor drives, welders, ultrasonics)
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- New QPL (Government) Types

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- ITRs/RCTs
- SCR Current Capability
- Device Parameters Which Are Important for SCR Energy Efficient High-frequency Inverters
- Switching Dissipation
- Typical Commutation (Turn-off) Techniques
- Typical Sinusoidal Inverters
- Typical Non-sinusoidal Inverters
- Motor Speed Controls

(3) Power MOS/FETs.

- Historical Review of Power MOS/FETs
- Power MOS/FET Design Technologies

- Bipolar and MOS/FET Comparisons (Economic Ramifications)
- Power MOS/FET Applications
- RCA MOS/FET Product Line

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RCA

Seminar schedule

Location	Date	Co-sponsor/ Distributor	Distributor Contact	Phone
Long Island, NY	Sept. 15	Schweber	Alex Artesani	516-334-7474
North Jersey, NJ	Sept. 16	Schweber	Steve Fetics	201-227-7880
Boston, MA	Sept. 17	Sterling	Don Adams	617-894-6200
Cincinnati/Dayton, OH	Sept. 22	Arrow	Sue Littley	513-435-5563
Detroit, MI	Sept. 23	Schweber	John Sutterlin	313-525-8100
Cleveland, OH	Sept. 24	Arrow	Jim Marrie	216-248-3900
Danbury, CT	Oct. 1	Schweber	Kaki Schumacher	203-792-3500
Philadelphia, PA	Oct. 5	Schweber	Holly Fonarow	215-441-0600
Baltimore/Washington	Oct. 6	Schweber	Linda Mitchell	301-840-5900
Minneapolis, MN	Oct. 13	Arrow	Steve Turner	612-830-1819
Milwaukee, WI	Oct. 14	Taylor	Mary Houle	414-241-4321
Chicago, IL	Oct. 15	Hamilton/Avnet	Darlynne	312-860-7780
Santa Clara, CA	Oct. 19	Wyle	Rich Cimino	408-727-2500
Los Angeles, CA	Oct. 20	Schweber	Bob Rodrique	714-556-3880
Orange County, CA	Oct. 21	Marshall	Liz D'Amico	714-556-6400
San Diego, CA	Oct. 22	Arrow	Carol Dixon	714-565-4800
Atlanta, GA	Oct. 27	Arrow	Jerry Bokus	404-449-8252
Ft. Lauderdale, FL	Oct. 28	Arrow	Joe Wellisch	305-776-7790
Orlando, FL	Oct. 29	Schweber	Steve Clark	305-331-7555
Denver, CO	Nov. 9	Wyle	Mike Jaques	303-457-9953
Kansas City, MO	Nov. 10	Hamilton/Avnet	Leanna Eberenz	913-541-7921
Houston, TX	Nov. 11	Schweber	Ron Williams	713-784-3600
Dallas, TX	Nov. 12	Sterling	Liz Leonard	214-243-1600

For RCA CMOS 1800-series microprocessor seminars and workshops, call (800) 526-3862.

(In New Jersey call 201-685-5533.)

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CIRCLE NO 52

8-BIT CPU Z80 | DEVELOPMENT OPERATING SYSTEM | GENERAL-PURPOSE OPERATING SYSTEM | REAL-TIME OPERATING SYSTEM

OASIS*

Phase One Systems Inc
7700 Edgewater Dr, Suite 830
Oakland, CA 94621
Phone (415) 562-8085

RELEASE DATE: November 1979
PRICE: $850
TARGET MODEL: Z80
SUPPORT LANGUAGES: Z80 macro assembler; BASIC interpreter; RM COBOL, PASCAL and FORTRAN 77; BASIC and C compilers
SYSGEN PROGRAM: Yes **SOURCE CODE:** No
LANGUAGE SYSTEM: Z80 assembler
NETWORK SUPPORT: No

SYSTEM RESIDENCY: Disk
ROMABLE SYSTEM: No
MINIMUM HARDWARE NEEDED: 56k bytes RAM, dual floppy-disk drives and Z80 CPU

PROCESSOR ALLOCATION/MANAGEMENT

- Single vs User mode
- Multitasking: 15 tasks can start/stop/suspend other tasks
- Multiusage: 16 users with 4k bytes (min) RAM per user
- Synchronizing scheme: varies with hardware

PERIPHERAL MANAGEMENT

- Supports CRTs, character and line printers; floppy-, hard- and cartridge-disk drives; modems and magnetic-tape drives
- Provides device independence, DMA and spooling
- Uses interrupts and I/O multibuffering
- Accommodates a mix of eight disk drives of different types
- Supports up to 128M bytes of disk and 784k bytes of RAM

COMMENTS: *Multiuser; optional CONTROL RDBMS, File Sort and IBM3470 formatter packages available. Single-user version available for $500.

MEMORY MANAGEMENT

- Memory protection
- Overlays
- Chaining and segmentation
- Static and dynamic relocations
- Binding done during linking time

FILE MANAGEMENT

- Named file system
- Sequential, keyed and random organizations
- Indexed sequential access method (ISAM)
- Allocation types: linked list of sectors and single contiguous
- Can access file system from HLL containing constructs
- Password, privilege level security protection
- Automatic record and file locking

CIRCLE NO 713

8-BIT CPU Z80 | DEVELOPMENT OPERATING SYSTEM | GENERAL-PURPOSE OPERATING SYSTEM | REAL-TIME OPERATING SYSTEM

OASIS-16

Phase One Systems Inc
7700 Edgewater Drive, Suite 830
Oakland, CA 94621
Phone (415) 562-8085

RELEASE DATE: September 1981
PRICE: $1495
TARGET MODEL: 8086, Z8000, 68000
SUPPORT LANGUAGES: Z80 macro assembler; BASIC interpreter; RM COBOL, FORTH, PASCAL and FORTRAN 77; BASIC and C compilers
SYSGEN PROGRAM: Yes **SOURCE CODE:** No
LANGUAGE SYSTEM: C compiler
NETWORK SUPPORT: Yes

SYSTEM RESIDENCY: Disk
ROMABLE SYSTEM: No
MINIMUM HARDWARE NEEDED: 128k bytes RAM, dual floppy-disk drives and 16-bit CPU

PROCESSOR ALLOCATION/MANAGEMENT

- System vs User mode
- Multitasking: 15 tasks can start/stop/suspend other tasks
- Multiusage: 32 users with 4k bytes (min) RAM per user
- Interprocessor communications: pipes
- Dynamic user partitioning

PERIPHERAL MANAGEMENT

- Supports CRTs; character and line printers; floppy- hard- and cartridge-disk drives; modems; magnetic-tape drives and bubble-memory devices
- Provides device independence, DMA and spooling
- Uses interrupts and I/O multibuffering
- Accommodates a mix of 32 disk drives of different types
- Supports up to 8736M bytes of disk

COMMENTS: Optional CONTROL RDBMS, File Sort and IBM3470 formatter packages available

MEMORY MANAGEMENT

- Overlays
- Chaining and segmentation
- Static and dynamic relocations
- Binding done during linking time

FILE MANAGEMENT

- Named file system and multilevel directory
- Sequential, contiguous, keyed and random organizations
- Multikeyed indexed sequential access method (ISAM)
- Allocation types: linked list of sectors and single contiguous
- Can access file system from HLL containing constructs
- Password privilege level security protection
- Automatic record and file locking
- Dynamic file allocation and priority scheduling

CIRCLE NO 733

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CIRCLE NO 53

DISTRIBUTORS IN MOST INDUSTRIALIZED COUNTRIES

EDN μC OPERATING SYSTEMS DIRECTORY

8-BIT CPU 6800 | DEVELOPMENT OPERATING SYSTEM | GENERAL-PURPOSE OPERATING SYSTEM | REAL-TIME OPERATING SYSTEM

PETOS

Perkin-Elmer Terminals Div
360 Rte 206 South
Flanders, NJ 07836
Phone (201) 584-1400

RELEASE DATE: August 1978
PRICE: $6783 with Model 3500 terminal
SUPPORT LANGUAGES: 6800 macro assembler; BASIC interpreter
SYSGEN PROGRAM: No **SOURCE CODE:** No
LANGUAGE SYSTEM: 6800 assembler
NETWORK SUPPORT: No

SYSTEM RESIDENCY: ROM
ROMABLE SYSTEM: Yes
MINIMUM HARDWARE NEEDED: 16k bytes RAM

PROCESSOR ALLOCATION/MANAGEMENT
- Multitasking: limited only by memory capacity
- Synchronizing scheme: priority

PERIPHERAL MANAGEMENT
- Supports CRTs, character and line printers and floppy-disk drives
- Provides device independence and DMA
- Uses interrupts and I/O multibuffering

MEMORY MANAGEMENT
- Overlays
- Chaining
- Binding during linking time

FILE MANAGEMENT
- Sequential and random organizations

COMMENTS: PETOS is available only with the P-E Model 3500 intelligent terminal.

CIRCLE NO 725

8/16-BIT CPU 10 μCs, μPs* | DEVELOPMENT OPERATING SYSTEM | GENERAL-PURPOSE OPERATING SYSTEM | REAL-TIME OPERATING SYSTEM

POLYFORTH

Forth Inc
2309 Pacific Coast Hwy
Hermosa Beach, CA 90254
Phone (213) 372-8493

RELEASE DATE: 1979
PRICE: $5100
TARGET MODEL: MDS, SBC, Q-Bus, Unibus, Exorciser, TI990, Nova and Cosmac
SUPPORT LANGUAGES: Common processors' assemblers; FORTH interpreter and compiler; CP/M for 8080 and 8086
SYSGEN PROGRAM: Yes **SOURCE CODE:** Yes
LANGUAGE SYSTEM: FORTH
NETWORK SUPPORT: No

SYSTEM RESIDENCY: RAM
ROMABLE SYSTEM: Yes
MINIMUM HARDWARE NEEDED: 16k bytes RAM, serial interface, terminal, disk drive

PROCESSOR ALLOCATION/MANAGEMENT
- Multitasking: number of tasks, limited only by memory capacity, can start/stop/suspend other tasks via intertask communication
- Multiusage: number of users limited only by memory capacity, with 1k bytes (min) RAM per user

PERIPHERAL MANAGEMENT
- Supports CRTs, character and line printers, floppy- and cartridge-disk drives and magnetic- and paper-tape drives
- Provides device independence, DMA and spooling
- Uses interrupts and I/O multibuffering
- Accommodates a mix of mass-storage devices via device drivers and assigned memory areas

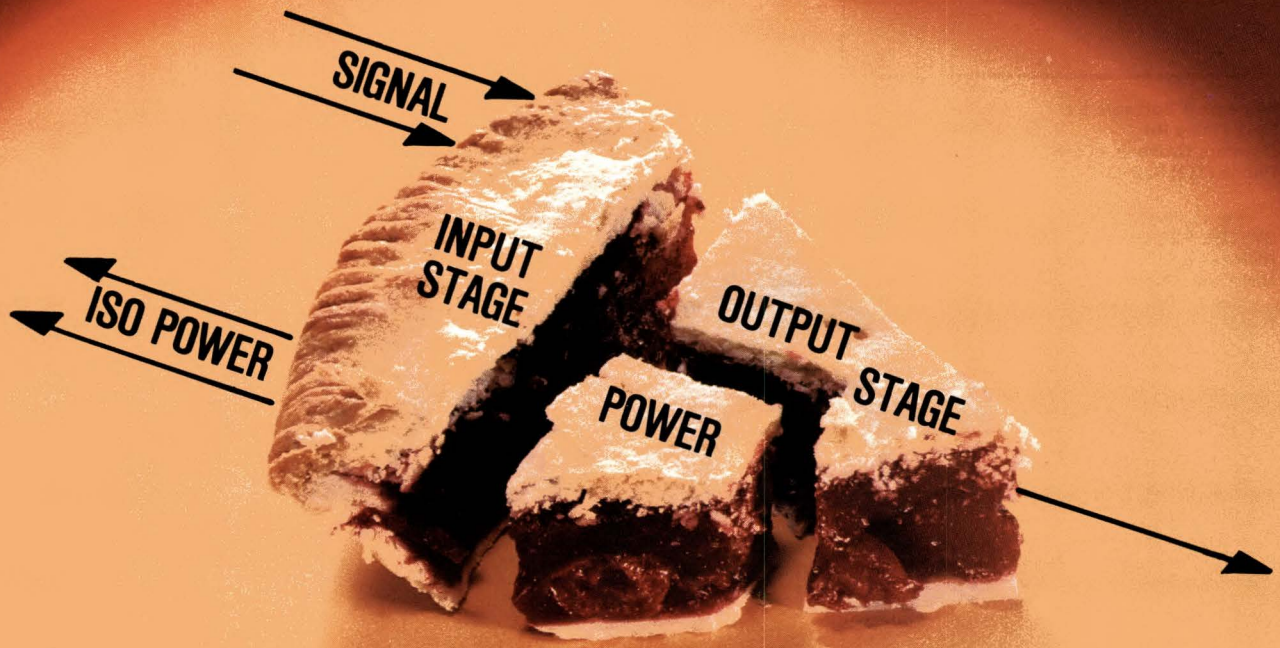
MEMORY MANAGEMENT
- Single contiguous allocation
- Overlays
- Chaining
- Binding done in single process
- Memory protection

FILE MANAGEMENT
- Named file system
- Sequential, contiguous and random organizations
- Indexed sequential access method (ISAM)
- Allocation type: single contiguous
- Can access file system using constructs
- Password/security protection

COMMENTS: *8080, 8086, 9900, 6800, 6809, 68000, 1802, LSI-11, PDP-11, Nova and IBM Series/1

CIRCLE NO 726

Now It's Easy as Pie...



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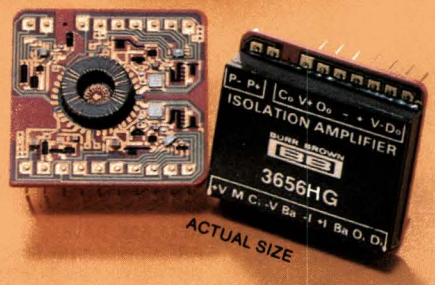

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3656HG	3500	8000	108	0.5	1.5	0.15	0 to +70	$4 + \frac{40}{G}$	$200 + \frac{1000}{G}$	$48.65
3656JG	3500	8000	112	0.5	1.0	0.1	0 to +70	$2 + \frac{20}{G}$	$50 + \frac{500}{G}$	$51.90
3656KG	3500	8000	112	0.5	1.0	0.1	0 to +70	$1 + \frac{10}{G}$	$10 + \frac{350}{G}$	$63.75

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CIRCLE NO 54

EDN μC OPERATING SYSTEMS DIRECTORY

8, 16-BIT CPU 8080, 8085, 8086, Z80 | DEVELOPMENT OPERATING SYSTEM | GENERAL-PURPOSE OPERATING SYSTEM | REAL-TIME OPERATING SYSTEM

REX-80

Systems & Software Inc
2801 Finley Rd
Downers Grove, IL 60515
Phone (312) 932-9320

RELEASE DATE: May 1978
PRICE: $1800
TARGET MODEL: Single-board computers
SUPPORT LANGUAGES: Relocatable macro assembler; C and PL/M compilers
SYSGEN PROGRAM: Yes **SOURCE CODE:** Yes
LANGUAGE SYSTEM: Assembler
NETWORK SUPPORT: No

SYSTEM RESIDENCY: RAM
ROMABLE SYSTEM: Yes
MINIMUM HARDWARE NEEDED: 2k bytes ROM, 512 bytes RAM, real-time clock and priority interrupt controller

PROCESSOR ALLOCATION/MANAGEMENT

- System vs User mode
- Multitasking: limited by memory, tasks can start/stop/suspend other tasks via 64 intertask communication channels and mailbox synchronization
- Multiprocessing: eight processors use test and set and interrupt synchronizing scheme

PERIPHERAL MANAGEMENT

- Supports CRTs, character and line printers, floppy-disk drives, modems and paper-tape drives
- Provides device independence and spooling
- Uses interrupts and I/O multibuffering

MEMORY MANAGEMENT

- Single contiguous allocation
- Segmentation
- Static relocation
- Binding done during linking time

FILE MANAGEMENT

Not Available

CIRCLE NO 748

16-BIT CPU LSI-11/2, LSI-11/23 | DEVELOPMENT OPERATING SYSTEM | GENERAL-PURPOSE OPERATING SYSTEM | REAL-TIME OPERATING SYSTEM

RSX-11M, RSX-11S

Digital Equipment Corp
One Iron Way
Marlboro, MA 01752
Phone (800) 225-9220

RELEASE DATE: 1975
PRICE: RSX-11M, $8600; RSX-11S, $560
SUPPORT LANGUAGES: Macro assembler; BASIC interpreter; FORTRAN IV, FORTRAN IV-PLUS, COBOL and BASIC-PLUS II compilers
SYSGEN PROGRAM: Yes **SOURCE CODE:** Yes
LANGUAGE SYSTEM: Macro assembler
NETWORK SUPPORT: DECNET, 2780/3780 emulation

SYSTEM RESIDENCY: Hard-disk based
ROMABLE SYSTEM: No
MINIMUM HARDWARE NEEDED: LSI-11/23 (LSI-11/2 for unmapped RSX-11S), 48k bytes RAM, RL01 disk drive, console port and clock

PROCESSOR ALLOCATION/MANAGEMENT

- Multitasking: number of tasks limited only by memory capacity
- Priority or round-robin scheduling
- Multiusage available
- Intertask communication and synchronization
- Log-in/log-out with password

PERIPHERAL MANAGEMENT

- Supports CRTs, character and line printers, floppy- and hard-disk drives, modems, paper-tape drives and TU58 cartridge-tape drives
- Provides device independence, DMA and spooling
- Uses interrupts
- Accommodates up to four hard-disk drives, four double-density floppy-disk drives and/or four TU58 cartridge-tape drives

MEMORY MANAGEMENT

- Automatic memory compaction
- Supports hardware relocation, segmentation and protection
- Binding during assembly/compilation, linking, loading, run and/or execution times
- Supports check pointing to disk
- Overlapping and shared code

FILE MANAGEMENT

- Named file system with per-user directories and protection
- Sequential, random and ISAM access
- Contiguous or mapped allocation
- Can access system from HLL

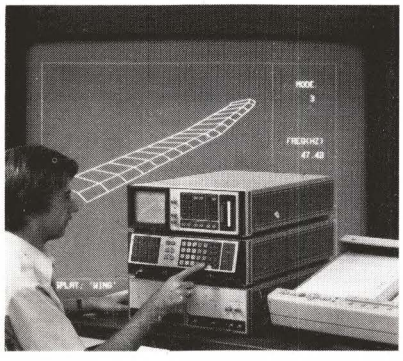
COMMENTS: RSX-11S is a memory only (no file support) subset of RSX-11M

CIRCLE NO 681

Complete and affordable dynamic analysis of your product –including modal.

☐ **HP's New 5423A Structural Dynamics Analyzer**—an entirely new kind of instrument for mechanical and electro-mechanical design and test that's far easier to use and lower in cost than available alternatives. The HP 5423A Structural Dynamics Analyzer provides state-of-the-art measurement, analysis, display, storage and plotting capabilities in a convenient transportable package.

☐ **Complete Measurement Capability** provides the accurate data you need for the analysis of dynamic behavior. These capabilities include time record, power spectrum, frequency response and coherence —just to name a few. A built-in "waveform calculator" operates on measured data as well as on real and complex constants. Easy to use, it lets you compute characteristics which are difficult or even impossible to measure directly: including non-coherent output power, open-loop gain of a control system and the synthesis of frequency response functions.



☐ **An Animated Mode Shape Display** dramatically illustrates the results of a test by depicting structural deformation for each natural resonant frequency. You can quickly identify problem points such as maximum stress, flexure or sound transmission. Additional display features include:

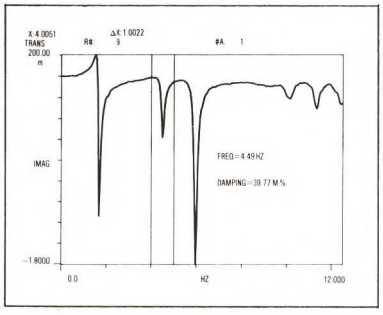
- Perspective
- Rotation about any axis
- True three dimensions using a stereoscope
- Selection of viewing direction and distance
- "Zoom" on portions of interest
- Split-screen viewing of any two modes
- Highlighting of points of interest
- Stop-motion for detailed study

Nowhere else can you get this capability at such a low cost. $41,000.*

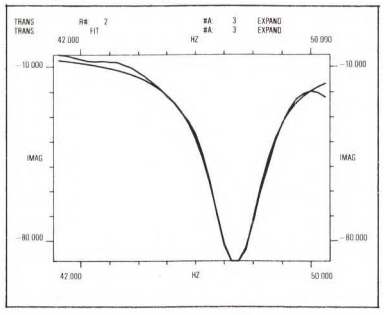
For more information on how the 5423A can help you, call your nearby HP sales office. Or write Hewlett-Packard, 1507 Page Mill Road, Palo Alto, CA 94304.

*Domestic U.S. price only.

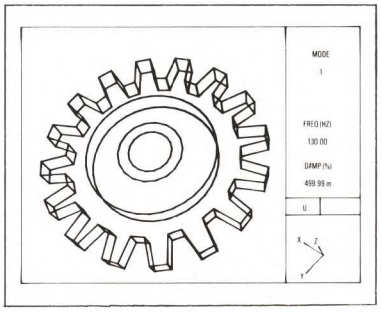
Three Simple Steps to a Complete Dynamic Analysis



1. Measure frequency response with the 5423A and identify the resonances of interest using the X-Axis cursors. Cursor settings are automatically stored for use at other points on the structure.



2. A few keystrokes graphically display the result of curve-fitting the measured data at each resonance and automatically enter the computed frequency, damping and residue information into tables for display or outputting.



3. Repeat the process at points of interest on the structure. The 5423A's Auto Sequence capability controls the instrument for you. Mode shapes for each resonant frequency are displayed using the geometry which describes your structure.

02007

HEWLETT PACKARD

CIRCLE NO 55

16-BIT CPU LSI-11/2, LSI-11/23 | DEVELOPMENT OPERATING SYSTEM | GENERAL-PURPOSE OPERATING SYSTEM | REAL-TIME OPERATING SYSTEM

RT-11

Digital Equipment Corp
One Iron Way
Marlboro, MA 01752
Phone (800) 225-9220

RELEASE DATE: 1973
PRICE: $3620
SUPPORT LANGUAGES: Macro assembler; BASIC, FOCAL, APL and Multiuser BASIC interpreters; FORTRAN IV compiler
SYSGEN PROGRAM: Yes **SOURCE CODE:** Yes
LANGUAGE SYSTEM: Macro assembler
NETWORK SUPPORT: DECNET, 1-port 2780/3780 emulation

SYSTEM RESIDENCY: Disk initially, RAM only after app program run
ROMABLE SYSTEM: FORTRAN applications only
MINIMUM HARDWARE NEEDED: 24k bytes RAM (includes RT-11 and application programs), LSI-11/2, TU58 cartridge-tape drive and console port

PROCESSOR ALLOCATION/MANAGEMENT

- System vs User mode
- Multitasking: eight tasks start asynchronous I/O via monitor call
- Synchronizing schemes: send/receive messages, mailboxes and, for I/O completion only, semaphore

PERIPHERAL MANAGEMENT

- Supports CRTs, character and line printers, floppy- and cartridge-disk drives, modems, paper-tape drives and TU58 block-addressable cartridge tapes
- Provides device independence, DMA and spooling
- Uses interrupts
- Accommodates up to four hard-disk drives, four single-density and/or four double-density floppy-disk drives and/or four TU58 cartridge-tape drives

MEMORY MANAGEMENT

- Single contiguous allocation and overlays
- Segmentation via chaining
- Static and dynamic relocations
- Binding during assembly/compilation, linking, loading, run and/or execution times
- Supports hardware relocation, segmentation and protection

FILE MANAGEMENT

- Named file system
- Sequential and random access
- Allocation type: single contiguous
- Can access system from HLL
- Protects files from deletion when locked

COMMENTS: RT-11 also runs on DEC minicomputers.

CIRCLE NO 727

16-BIT CPU HP 1000 L Series | DEVELOPMENT OPERATING SYSTEM | GENERAL-PURPOSE OPERATING SYSTEM | REAL-TIME OPERATING SYSTEM

RTE-XL

Hewlett-Packard Co
11000 Wolfe Rd
Cupertino, CA 95014
Phone (408) 257-7000

RELEASE DATE: November 1980
PRICE: $3150; additional copies $1260; execute-only license $210
TARGET MODEL: HP1000 L Series board, box or system
SUPPORT LANGUAGES: FORTRAN 4X; BASIC/1000L interpreter; PASCAL/1000; HP 1000 assembler
SYSGEN PROGRAM: Yes **SOURCE CODE:** Yes
LANGUAGE SYSTEM: Assembler
NETWORK SUPPORT: Yes, DS/1000-IV

SYSTEM RESIDENCY: RAM and disk
ROMABLE SYSTEM: Yes
MINIMUM HARDWARE NEEDED: 128k bytes RAM, L Series CPU board

PROCESSOR ALLOCATION/MANAGEMENT

- Multitasking: 255 tasks can run concurrently and start/stop/talk to other tasks via intertask communication
- Multiprocessing: manages CPU and, on each interface card, a separate I/O processor
- Time, event, program or operator scheduling of events
- Multilevel prioritized vectored interrupt system

PERIPHERAL MANAGEMENT

- Supports CRTs, character and line printers, floppy-, hard- and cartridge-disk drives, modems, magnetic-tape drives, plotters and IEEE-488-bus-related devices
- DMA on each I/O channel

MEMORY MANAGEMENT

- Up to 255 partitions
- Swapping
- Partition size to 64k bytes
- Power fail/autorestart
- Memory protection and program segmentation

FILE MANAGEMENT

- Named file system
- Sequential, contiguous and random organizations
- Allocation type: extents
- Password/security protection

CIRCLE NO 728

EDN μC OPERATING SYSTEMS DIRECTORY

16-BIT CPU 8086/Z8000/68000 | DEVELOPMENT OPERATING SYSTEM | GENERAL-PURPOSE OPERATING SYSTEM | REAL-TIME OPERATING SYSTEM

SP/8086/Z8000/68000

Hemenway Associates Inc
101 Tremont St
Boston, MA 02108
Phone (617) 426-1931

RELEASE DATE: June 1980
PRICE: $700
TARGET MODEL: Various
SUPPORT LANGUAGES: Macro assembler and linking loader; PASCAL/I compiler; BASIC and FORTRAN
SYSGEN PROGRAM: No **SOURCE CODE:** Yes
LANGUAGE SYSTEM: Assembler
NETWORK SUPPORT: No

SYSTEM RESIDENCY: RAM and disk
ROMABLE SYSTEM: Yes
MINIMUM HARDWARE NEEDED: 16k bytes RAM, console and floppy-disk drive

PROCESSOR ALLOCATION/MANAGEMENT
Not Available

PERIPHERAL MANAGEMENT
- Supports CRTs, character and line printers, floppy- and cartridge-disk drives, modems, magnetic- and paper-tape drives and other devices via suitable device drivers
- Provides device independence
- Uses interrupts and I/O multibuffering
- Accommodates a mix of floppy- and hard-disk drives

MEMORY MANAGEMENT
- Single contiguous allocation and overlays
- Chaining and static relocation
- Segmentation (depends on processor)
- Binding during linking time
- Memory protection (depends on hardware)

FILE MANAGEMENT
- Named file system
- Sequential and random organizations
- Allocation type: linked list of sectors
- Can access file system from HLL containing constructs
- Security protection

CIRCLE NO 729

16-BIT CPU 8086 | DEVELOPMENT OPERATING SYSTEM | GENERAL-PURPOSE OPERATING SYSTEM | REAL-TIME OPERATING SYSTEM

STARDOS

Micro Five Corp
17791 Sky Park Circle
Irvine, CA 92714
Phone (714) 957-1517

RELEASE DATE: May 1978
PRICE: Depends upon configuration
SUPPORT LANGUAGES: BASIC
SYSGEN PROGRAM: Yes **SOURCE CODE:** No
LANGUAGE SYSTEM: Interactive BASIC
NETWORK SUPPORT: Interprocessor

SYSTEM RESIDENCY: RAM
ROMABLE SYSTEM: No
MINIMUM HARDWARE NEEDED: Series 3000 μC system and visual display terminal

PROCESSOR ALLOCATION/MANAGEMENT
- Multitasking: available
- Multiusage: available

PERIPHERAL MANAGEMENT
- Supports CRTs and character printers
- Provides device independence and DMA
- Uses interrupts and I/O multibuffering
- Accommodates a mix of mass storage devices

MEMORY MANAGEMENT
- Fixed partitions

FILE MANAGEMENT
- Database-management system (Update)

CIRCLE NO 687

8/16-BIT CPU 6809/68000 | DEVELOPMENT OPERATING SYSTEM | GENERAL-PURPOSE OPERATING SYSTEM | REAL-TIME OPERATING SYSTEM

UNIFLEX

Technical Systems Consultants Inc
1208 Kent Ave, Box 2570
West Lafayette, IN 47906
Phone (317) 463-2502

RELEASE DATE: July 1980
PRICE: $450
TARGET MODEL: Various
SUPPORT LANGUAGES: Micro, relocating and various cross assemblers; BASIC interpreters; C, PASCAL and FORTRAN compilers
SYSGEN PROGRAM: Yes **SOURCE CODE:** No
LANGUAGE SYSTEM: Assembler
NETWORK SUPPORT: Yes

SYSTEM RESIDENCY: RAM and disk
ROMABLE SYSTEM: No
MINIMUM HARDWARE NEEDED: 96k bytes RAM, memory-management device and DMA-driven disk controllers, all I/O-interrupt driven

PROCESSOR ALLOCATION/MANAGEMENT

- System vs User mode
- Multitasking: number of tasks, limited only by hardware, can start/stop/suspend other tasks via intertask communication "pipes"
- Multiusage: number of users limited only by hardware, with 28 bytes (min) RAM per user
- Multiprocessing: handles unlimited number of processors (with software modifications)

PERIPHERAL MANAGEMENT

- Supports CRTs, character and line printers, floppy- and cartridge-disk drives, modems and magnetic- and paper-tape drives
- Provides device independence, DMA and spooling
- Uses interrupts and I/O multibuffering
- Accommodates any mix and number of interrupt-driven DMA-controlled floppy- and hard-disk drives

MEMORY MANAGEMENT

- Overlays and segmentation
- Swapping and chaining
- Static and dynamic relocations
- Binding during linking time
- Memory protection (depends on hardware)

FILE MANAGEMENT

- Named file system and multilevel directory
- Sequential and random organizations
- Allocation type: resembles bit mapping
- Can access file system from HLL containing constructs
- Password/security protection

CIRCLE NO 730

16-BIT CPU 68000 | DEVELOPMENT OPERATING SYSTEM | GENERAL-PURPOSE OPERATING SYSTEM | REAL-TIME OPERATING SYSTEM

VERSADOS

Motorola Semiconductor Products Inc
3102 N 56th St
Phoenix, AZ 85018
Phone (602) 244-5714

RELEASE DATE: March 1980
PRICE: Depends on configuration
TARGET MODEL: Exormacs development system, Versamodule 01
SUPPORT LANGUAGES: Structured macro assembler, PASCAL compiler
SYSGEN PROGRAM: Yes **SOURCE CODE:** Request quote
LANGUAGE SYSTEM: Assembly and PASCAL
NETWORK SUPPORT: No

SYSTEM RESIDENCY: RAM and disk
ROMABLE SYSTEM: Executive only
MINIMUM HARDWARE NEEDED: Exormacs, 256k bytes RAM, Exorterm 155, Exordisk III, printer or Versamodule 01 with 128k bytes RAM

PROCESSOR ALLOCATION/MANAGEMENT

- System vs User mode
- Multitasking: unlimited number of tasks can start/stop/suspend other tasks via intertask communication
- Synchronizing scheme: semaphore

PERIPHERAL MANAGEMENT

- Supports CRTs, character and line printers, floppy- and cartridge-disk drives and modems
- Provides device independence, DMA and spooling
- Uses interrupts
- Accommodates a mix of floppy- and hard-disk drives

MEMORY MANAGEMENT

- Chaining
- Segmentation
- Static and dynamic relocations
- Binding during linking time
- Memory protection

FILE MANAGEMENT

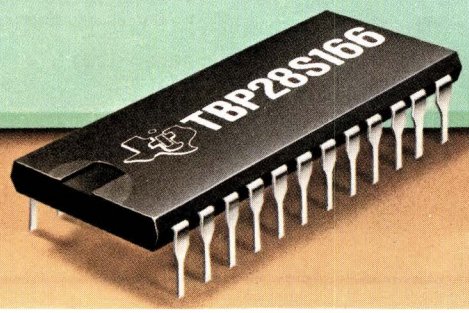
- Named file system and multilevel directory
- Sequential, contiguous and random organizations
- Indexed sequential access method (ISAM)
- Allocation type: extents
- Can access file system from HLL containing constructs
- Password/security protection

CIRCLE NO 731

TI'S GROWING PROM FAMILY

	NUMBER	ORGANIZATION	TYPICAL ADDRESS ACCESS TIME	TYPICAL POWER DISSIPATION
256 BITS	TBP18S030 TBP18SA030	32W x 8B	25 ns	400 mW
1K	TBP24S10 TBP24SA10	256W x 4B	35 ns	375 mW
2K	TBP28L22 TBP28LA22	256W x 8B	45 ns	375 mW
4K	TBP28S42 TBP28SA42	512W x 8B	35 ns	500 mW
	TBP28S46 TBP28SA46	512W x 8B	35 ns	500 mW
	TBP24S41 TBP24SA41	1024W x 4B	40 ns	475 mW
8K	TBP28S86-60 TBP28SA86-60	1024W x 8B	35 ns	625 mW
	TBP28S86 TBP28SA86	1024W x 8B	45 ns	625 mW
	TBP28L86	1024W x 8B	65 ns	275 mW
	TBP24S81-55 TBP24SA81-55	2048W x 4B	35 ns	625 mW
	TBP24S81 TBP24SA81	2048W x 4B	45 ns	625 mW
16K	TBP28S166-55 TBP28S166	2048W x 8B 2048W x 8B	35 ns 45 ns	675 mW 675 mW

= OPEN COLLECTOR; L = LOW POWER



New 16K PROM from Texas Instruments. The big family gets bigger. Covers your needs across the board.

The wider your choice, the easier your selection. So Texas Instruments steadily expands its bipolar PROM family. Latest addition: TBP28S166 16K PROM.

Organized 2Kx8, the TBP28S166 is available in two versions, with maximum address access times of either 55 ns or 75 ns. It comes in an industry-standard 600-mil, 24-pin package. Available soon: TBP28S165, a 300-mil, 24-pin version that can mean savings in board space of 50% or more.

Five more choices

TI has also redesigned five of its PROMs to give you better performance than ever before: the popular 1K; a low power 2K; two 512W x 8B 4Ks; the "by 8" 24-pin 8K. All offer faster address access times and lower power consumption than previous designs.

Programming convenience

One special reason for going with TI's PROM family is that a single specification programs all members from 1K through 16K. So if you use one of the popular programmers on the market today, one programming configuration is all you need. Result: Fewer programming problems and much lower costs.

Additional advantages

All TI PROMs incorporate titanium-tungsten fuse links. All have low current PNP inputs to permit easy interfacing with MOS and bipolar microprocessors. All are Schottky-clamped for best speed/power combinations.

Your choice of PROMS from TI is the industry's broadest. In densities. Performance. Packages. To save you time and trouble. For more information, call your nearest TI field sales office or distributor. Or write to Texas Instruments, P. O. Box 202129, Dallas, Texas 75220.

Texas Instruments invented the integrated circuit, microprocessor and microcomputer. Being first is our tradition.

TEXAS INSTRUMENTS
INCORPORATED

84324

CIRCLE NO 56

8-BIT CPU 6800 | DEVELOPMENT OPERATING SYSTEM | GENERAL-PURPOSE OPERATING SYSTEM | REAL-TIME OPERATING SYSTEM

WIZRD

Wintek Corp
1801 South St
Lafayette, IN 47904
Phone (317) 742-8428

RELEASE DATE: December 1979
PRICE: $495
TARGET MODEL: Sprint 68
SUPPORT LANGUAGES: 6800 assembler; BASIC interpreter; C and PL/W compilers
SYSGEN PROGRAM: No **SOURCE CODE:** No
LANGUAGE SYSTEM: 6800 assembly
NETWORK SUPPORT: No

SYSTEM RESIDENCY: RAM and disk
ROMABLE SYSTEM: No
MINIMUM HARDWARE NEEDED: 32k bytes RAM, serial I/O interface

PROCESSOR ALLOCATION/MANAGEMENT
- Multitasking: 64 tasks can start/stop/suspend other tasks via intertask communication
- Synchronizing scheme: monitors

PERIPHERAL MANAGEMENT
- Supports CRTs, character and line printers, floppy-disk drives and other device drivers
- Provides device independence and spooling
- Uses interrupts and I/O multibuffering
- Accommodates a mix of mass-storage devices with a general-purpose space allocator

MEMORY MANAGEMENT
- Single contiguous allocation
- Binding during assembly/compilation and linking times

FILE MANAGEMENT
- Named file system
- Random organization
- Allocation type: linked list of sectors
- Can access file system from HLL containing constructs

CIRCLE NO 732

8-BIT CPU 6502 | DEVELOPMENT OPERATING SYSTEM | GENERAL-PURPOSE OPERATING SYSTEM

CRS/DOS

CGRS Microtech
Box 102
Langhorne, PA 19047
Phone (215) 757-0284

RELEASE DATE: November 1979
PRICE: $500 source code, $150 custom
TARGET MODEL: Microtech 6502 PDS, PET, KIM, SYM and AIM
SUPPORT LANGUAGES: Machine language; BASIC and FORTH interpreters; FORTH compiler
SYSGEN PROGRAM: Yes **SOURCE CODE:** Yes
LANGUAGE SYSTEM: Machine language
NETWORK SUPPORT: No

SYSTEM RESIDENCY: RAM and disk
ROMABLE SYSTEM: Yes
MINIMUM HARDWARE NEEDED: 8k bytes RAM, 1k byte ROM and floppy-disk drive

PROCESSOR ALLOCATION/MANAGEMENT
- System vs User mode
- Multitasking: two tasks can start/stop/suspend each other through memory intertask communication
- Synchronizing scheme: mailbox

PERIPHERAL MANAGEMENT
- Supports CRTs, character and line printers, floppy-disk drives and modems
- Provides spooling in FORTH only
- Uses interrupts and I/O multibuffering
- Accommodates a mix of floppy-disk and cassette-tape drives

MEMORY MANAGEMENT
- Single contiguous allocation
- Overlays
- Swapping and chaining
- Segmentation
- Binding during assembly/compilation (optional) and linking times

FILE MANAGEMENT
- Named file system and multilevel directory
- Sequential, contiguous and random organizations
- Indexed sequential access method (ISAM)
- Allocation type: single contiguous
- Can access file system from HLL containing constructs

CIRCLE NO 735

8-BIT CPU: Most μP Types* | DEVELOPMENT OPERATING SYSTEM | GENERAL-PURPOSE OPERATING SYSTEM

DDOS, CP/M

Hughes Aircraft Co
500 Superior Ave
Newport Beach, CA 92663
Phone (714) 759-2942

RELEASE DATE: March 1979
PRICE: NA
SUPPORT LANGUAGES: Most assemblers; interpreters and compilers through CP/M
SYSGEN PROGRAM: No **SOURCE CODE:** No
LANGUAGE SYSTEM: Assembly
NETWORK SUPPORT: No

SYSTEM RESIDENCY: RAM and disk
ROMABLE SYSTEM: Yes
MINIMUM HARDWARE NEEDED: 32k bytes RAM

PROCESSOR ALLOCATION/MANAGEMENT
- System vs User mode
- Multitasking available
- Multiprocessing available
- Synchronizing scheme: mailbox

PERIPHERAL MANAGEMENT
- Supports CRTs, character and line printers, floppy-disk drives and modems
- Provides DMA and spooling (background printing)
- Uses interrupts and I/O multibuffering
- Accommodates a mix of floppy-disk drives

MEMORY MANAGEMENT
- Single contiguous allocation and overlays
- Swapping and chaining
- Segmentation and static relocations
- Binding done during linking and loading times
- Memory protection

FILE MANAGEMENT
- Named file system
- Multilevel directory
- Sequential and contiguous organizations
- Allocation type: single contiguous
- Password/security protection

COMMENTS: *1802, Z80, 8080, 8085, 1804, 8048, 6502, 6800, 6809, etc

CIRCLE NO 736

8-BIT CPU: 6800/6809 | DEVELOPMENT OPERATING SYSTEM | GENERAL-PURPOSE OPERATING SYSTEM

DOS68 (6800 CPUs), DOS69 (6809 CPUs)

Smoke Signal Broadcasting
31336 Via Colinas
Westlake Village, CA 91362
Phone (213) 889-9340

RELEASE DATE: January 1977
PRICE: $75
SUPPORT LANGUAGES: 6800 and 6809 macro assemblers; BASIC and UCSD PASCAL interpreters; BASIC, FORTRAN and COBOL compilers
SYSGEN PROGRAM: Yes **SOURCE CODE:** Yes
LANGUAGE SYSTEM: 6800/6809 assembly
NETWORK SUPPORT: No

SYSTEM RESIDENCY: RAM and disk
ROMABLE SYSTEM: Yes
MINIMUM HARDWARE NEEDED: 8k bytes RAM, CPU and disk drive and controller

PROCESSOR ALLOCATION/MANAGEMENT
- Multitasking: 16 tasks (min)

PERIPHERAL MANAGEMENT
- Supports CRTs, character and line printers, floppy- and cartridge-disk drives, modems, magnetic- and paper-tape drives
- Provides device independence, DMA and spooling
- Uses interrupts and I/O multibuffering
- Accommodates a mix of mass-storage devices

MEMORY MANAGEMENT
- Single contiguous allocation
- Overlays
- Swapping, chaining and segmentation
- Static and dynamic relocations
- Binding done during linking time

FILE MANAGEMENT
- Named file system
- Sequential, contiguous and random organizations
- Indexed sequential access method (ISAM)
- Allocation type: linked list of sectors
- Can access file system from HLL containing constructs

CIRCLE NO 738

8-BIT CPU 6800/6809 | DEVELOPMENT OPERATING SYSTEM | GENERAL-PURPOSE OPERATING SYSTEM

FLEX

Technical Systems Consultants Inc
Box 2570, 1208 Kent Ave
West Lafayette, IN 47906
Phone (317) 463-2502

RELEASE DATE: April 1977
PRICE: $100 to $150
TARGET MODEL: Various
SUPPORT LANGUAGES: Macro and cross assemblers; BASIC and Extended BASIC interpreters; C and PASCAL (6809 only) compilers
SYSGEN PROGRAM: Yes **SOURCE CODE:** No
LANGUAGE SYSTEM: Assembler
NETWORK SUPPORT: No

SYSTEM RESIDENCY: RAM and disk
ROMABLE SYSTEM: No
MINIMUM HARDWARE NEEDED: 20k bytes RAM

PROCESSOR ALLOCATION/MANAGEMENT
- Multitasking: two tasks—printer spooler runs as background task

PERIPHERAL MANAGEMENT
- Supports CRTs, character and line printers, floppy- and hard-disk drives, modems and paper-tape drives
- Provides device independence (limited), DMA and spooling
- Uses interrupts
- Accommodates a mix of mass-storage devices

MEMORY MANAGEMENT
- Single contiguous allocation
- Overlays
- Chaining

FILE MANAGEMENT
- Named file system
- Sequential and random organizations
- Allocation type: linked list of sectors
- Can access file system from HLL containing constructs

CIRCLE NO 739

8-BIT CPU 8080/Z80 | DEVELOPMENT OPERATING SYSTEM | GENERAL-PURPOSE OPERATING SYSTEM

HDOS

Heath Co
Benton Harbor, MI 49022
Phone (616) 982-3650

RELEASE DATE: 1978
PRICE: $195
TARGET MODEL: H-8, H-89
SUPPORT LANGUAGES: 8080 and Z80 assemblers; BASIC interpreter; FORTRAN and C compilers
SYSGEN PROGRAM: Yes **SOURCE CODE:** Yes
LANGUAGE SYSTEM: Assembler
NETWORK SUPPORT: No

SYSTEM RESIDENCY: RAM and disk
ROMABLE SYSTEM: No
MINIMUM HARDWARE NEEDED: 32k bytes RAM, console and floppy-disk system

PROCESSOR ALLOCATION/MANAGEMENT
Not Available

PERIPHERAL MANAGEMENT
- Supports CRTs, character and line printers, floppy- and hard-disk drives and modems
- Provides device independence (limited)
- Uses interrupts
- Accommodates 5¼-in. and 8-in. single-sided single-density and 8-in. double-sided double-density floppy-disk drives

MEMORY MANAGEMENT
- Single contiguous allocation
- Overlays
- Swapping , chaining and limited segmentation
- Static relocation
- Binding done during assembly/compilation time

FILE MANAGEMENT
- Named file system
- Sequential and random organizations
- Allocation type: linked list of sectors
- Can access file system from HLL containing constructs

CIRCLE NO 740

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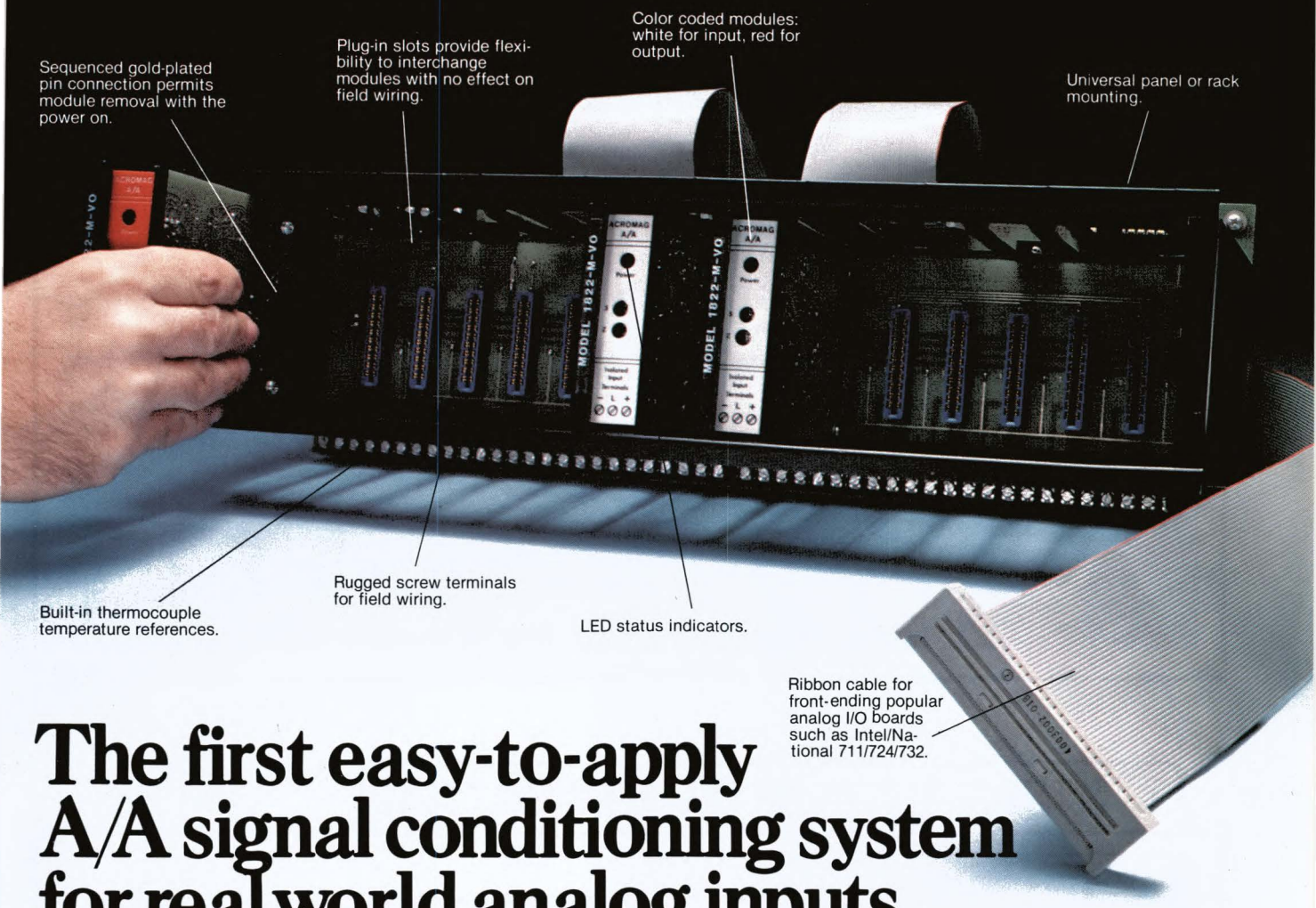

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Acromag, 30765 Wixom Rd., Wixom, MI 48096, (313) 624-1541. Telex 23/0505.

ACROMAG

CIRCLE NO 57

8-BIT CPU 8080/8085 | DEVELOPMENT OPERATING SYSTEM | GENERAL-PURPOSE OPERATING SYSTEM

HDOS

Ontel Corp
250 Crossways Park Dr
Woodbury, NY 11797
Phone (516) 364-2121

RELEASE DATE: January 1978
PRICE: Depends on configuration
TARGET MODEL: Ontel OP-1
SUPPORT LANGUAGES: LINKASM and MACASM assemblers; BASIC, OPL and PASCAL interpreters; FORTRAN compiler
SYSGEN PROGRAM: Yes **SOURCE CODE:** Yes
LANGUAGE SYSTEM: Assembler
NETWORK SUPPORT: 16 terminals with standard IOS calls

SYSTEM RESIDENCY: RAM and disk
ROMABLE SYSTEM: No
MINIMUM HARDWARE NEEDED: 32k bytes RAM and hard-disk drive and controller

PROCESSOR ALLOCATION/MANAGEMENT
- Multitasking: 16 tasks can start/stop/suspend other tasks via intertask communication (OPL only)
- Multiusage: up to eight terminals can share hard-disk system
- Synchronizing scheme: semaphore (OPL only)

PERIPHERAL MANAGEMENT
- Supports CRTs, character and line printers, floppy- and cartridge-disk drives, modems and magnetic-tape drives*
- Provides device independence, DMA and spooling
- Uses interrupts (OPL only)
- Accommodates a mix of hard- and floppy-disk drives

MEMORY MANAGEMENT
- Single contiguous allocation
- Overlays and chaining
- Segmentation and dynamic relocation (OPL only)
- Static relocation
- Binding done during linking time

FILE MANAGEMENT
- Named file system and sequential organization
- Random organization, multilevel directory and ISAM (OPL only)
- Allocation type: linked list of sectors
- Can access file system from HLL containing constructs
- Password/security protection

COMMENTS: *Modems and magnetic-tape drives are supported by LINKASM subroutines, not OS drivers.

CIRCLE NO 741

8-BIT CPU 8080/8085 | DEVELOPMENT OPERATING SYSTEM | GENERAL-PURPOSE OPERATING SYSTEM

MDOS

Ontel Corp
250 Crossways Park Dr
Woodbury, NY 11797
Phone (516) 364-2121

RELEASE DATE: September 1978
PRICE: Depends on configuration
TARGET MODEL: Ontel OP-1
SUPPORT LANGUAGES: LINKASM and MACASM assemblers; BASIC, OPL and PASCAL interpreters; FORTRAN compiler
SYSGEN PROGRAM: Yes **SOURCE CODE:** No
LANGUAGE SYSTEM: Assembler
NETWORK SUPPORT: 16 terminals with standard IOS calls

SYSTEM RESIDENCY: RAM and disk
ROMABLE SYSTEM: No
MINIMUM HARDWARE NEEDED: 32k bytes RAM and diskette drive and controller

PROCESSOR ALLOCATION/MANAGEMENT
- Multitasking: 16 tasks can start/stop/suspend other tasks via intertask communication
- Synchronizing scheme: semaphore (OPL only)

PERIPHERAL MANAGEMENT
- Supports CRTs, character and line printers, floppy-disk drives, modems and magnetic-tape drives*
- Provides device independence, DMA and spooling
- Uses interrupts (OPL only)
- Accommodates a mix of floppy-disk drives of different sizes and densities

MEMORY MANAGEMENT
- Single contiguous allocation
- Overlays
- Chaining, segmentation and dynamic relocation (OPL only)
- Static relocation
- Binding done during linking time

FILE MANAGEMENT
- Named file system
- Sequential organization
- Random organization, ISAM and multilevel directory (OPL only)
- Allocation type: linked list of sectors
- Can access file system from HLL containing constructs

COMMENTS: *Magnetic-tape drives are supported by subroutines, not OS drivers.

CIRCLE NO 742

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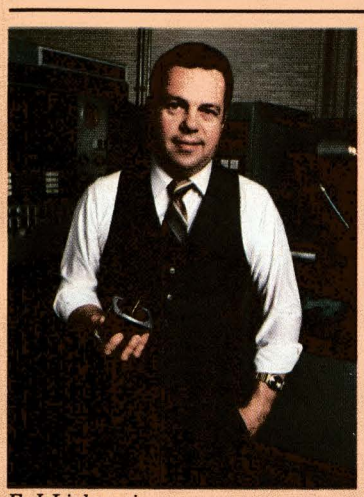

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CIRCLE NO 58

EDN μC OPERATING SYSTEMS DIRECTORY

8-BIT CPU Z80 | DEVELOPMENT OPERATING SYSTEM | GENERAL-PURPOSE OPERATING SYSTEM

M/OS-80

Mostek Corp
1215 W Crosby Rd
Carrollton, TX 75006
Phone (214) 323-6000

RELEASE DATE: May 1981
PRICE: $250 with PROMs; $199 without PROMs
SUPPORT LANGUAGES: CP/M compatible
SYSGEN PROGRAM: Yes
SOURCE CODE: No
LANGUAGE SYSTEM: Assembly
NETWORK SUPPORT: Yes

SYSTEM RESIDENCY: PROM, disk and RAM
ROMABLE SYSTEM: No
MINIMUM HARDWARE NEEDED: 32k bytes RAM, MDXFLP disk controller board and serial or parallel port

PROCESSOR ALLOCATION/MANAGEMENT
- System vs User mode
- Multitasking available

PERIPHERAL MANAGEMENT
- Supports CRT, printer, paper-tape reader and punch and dual-sided single-density floppy-disk drives
- Provides device independence, DMA and spooling
- Uses interrupts and I/O multibuffering
- Accommodates up to 15 floppy-disk drives

MEMORY MANAGEMENT
- Single management allocation
- Overlays
- Segmentation

FILE MANAGEMENT
- Named file system (CP/M compatible)
- Sequential allocated clusters
- Allocation type: extents
- Can access file system from HLL containing constructs
- Password/security protection

CIRCLE NO 700

8-BIT CPU 8085/Z80 | DEVELOPMENT OPERATING SYSTEM | GENERAL-PURPOSE OPERATING SYSTEM

O/S

Applied Systems Corp
26401 Harper Ave
St Clair Shores, MI 48081
Phone (313) 779-8700

RELEASE DATE: 1979
PRICE: Depends on configuration
TARGET MODEL: ASC/80
SUPPORT LANGUAGES: 8085 and Z80 assemblers; BASIC interpreter; FORTRAN and COBOL compilers
SYSGEN PROGRAM: No
SOURCE CODE: No
LANGUAGE SYSTEM: Assembly
NETWORK SUPPORT: Yes

SYSTEM RESIDENCY: RAM and disk
ROMABLE SYSTEM: Yes
MINIMUM HARDWARE NEEDED: 16 or 32k bytes RAM

PROCESSOR ALLOCATION/MANAGEMENT
- System vs User mode
- Multitasking available
- Multiusage: 6 to 16 users

PERIPHERAL MANAGEMENT
- Supports CRTs, character and line printers, floppy- and hard-disk drives and modems
- Provides DMA
- Uses interrupts
- Accommodates a mix of mass-storage devices

MEMORY MANAGEMENT
- Single contiguous allocation
- Overlays
- Memory protection

FILE MANAGEMENT
- Named file system
- Sequential and random organizations
- Password/security protection

CIRCLE NO 744

8-BIT CPU Z80 | DEVELOPMENT OPERATING SYSTEM | GENERAL-PURPOSE OPERATING SYSTEM

OS-CP/M

Ohio Scientific Inc
1333 S Chillicothe Rd
Aurora, OH 44202
Phone (216) 831-5600

RELEASE DATE: 1977
PRICE: $695
TARGET MODEL: C3 Series
SUPPORT LANGUAGES: 8080 assembler; BASIC interpreter; FORTRAN and COBOL compilers
SYSGEN PROGRAM: Yes **SOURCE CODE:** No
LANGUAGE SYSTEM: Z80 machine code
NETWORK SUPPORT: No

SYSTEM RESIDENCY: RAM and disk
ROMABLE SYSTEM: No
MINIMUM HARDWARE NEEDED: 56k bytes RAM and C3 Series computer

PROCESSOR ALLOCATION/MANAGEMENT

Not Available

PERIPHERAL MANAGEMENT

- Supports CRTs, line printers and floppy- and hard-disk drives
- Provides device independence
- Accommodates a mix of CD-36 and CD-74 floppy- and hard-disk drives

MEMORY MANAGEMENT

- Single contiguous allocation
- Overlays
- Chaining
- Static relocation
- Binding done during assembly/compilation time

FILE MANAGEMENT

- Named file system
- Sequential and random organizations
- Allocation type: extents
- Can access file system from HLL containing constructs

CIRCLE NO 745

8-BIT CPU 6809 | DEVELOPMENT OPERATING SYSTEM | GENERAL-PURPOSE OPERATING SYSTEM

OS-9

Microware Systems Corp
Box 4865
Des Moines, IA 50304
Phone (515) 279-8844

RELEASE DATE: January 1980
PRICE: $195, Level 1; $495, Level 2
SUPPORT LANGUAGES: Assembler, BASIC-09 and PASCAL and COBOL compilers
SYSGEN PROGRAM: Yes **SOURCE CODE:** Yes
LANGUAGE SYSTEM: 6809 assembler
NETWORK SUPPORT: Yes

SYSTEM RESIDENCY: RAM and disk
ROMABLE SYSTEM: Yes
MINIMUM HARDWARE NEEDED: 48k bytes RAM, CPU and disk drive

PROCESSOR ALLOCATION/MANAGEMENT

- Multitasking: 256 tasks

PERIPHERAL MANAGEMENT

- Supports CRTs, character and line printers, floppy- and hard-disk drives, modems and magnetic-tape drives
- Provides device independence, DMA and spooling
- Uses interrupts and I/O multibuffering
- Accommodates a mix of mass-storage devices

MEMORY MANAGEMENT

- Single contiguous allocation
- Overlays
- Swapping, chaining and segmentation
- Static and dynamic relocations
- Re-entrant code; Level 2 supports 1M bytes of RAM

FILE MANAGEMENT

- Named file system
- Sequential, contiguous and random organizations
- Indexed sequential access method (ISAM)
- Allocation type: bit map on disk
- Can access file system from HLL containing constructs

CIRCLE NO 707

8-BIT CPU Z80 | DEVELOPMENT OPERATING SYSTEM | GENERAL-PURPOSE OPERATING SYSTEM

RIO, VERSIONS 2, 3* and 4

Zilog Inc
10460 Bubb Rd
Cupertino, CA 95014
Phone (408) 446-4666

RELEASE DATE: RIO Version 2: June 1977
RIO Version 3: August 1980
PRICE: $500 (free with system purchase)
TARGET MODEL: MCZ1 Series, ZDS systems, PDS 8000 systems
SUPPORT LANGUAGES: Z80 ASM, Z8 PLZ/ASM and Z8000 PLZ/ASM assemblers; BASIC and PASCAL interpreters; FORTRAN, COBOL (single and multiterminal) and PLZ/SYS compilers
SYSGEN PROGRAM: No **SOURCE CODE:** No
LANGUAGE SYSTEM: Z80 ASM and PLZ/SYS
NETWORK SUPPORT: Version 4 only; Z-Net supports up to 255 nodes

SYSTEM RESIDENCY: RAM and disk
ROMABLE SYSTEM: Yes
MINIMUM HARDWARE NEEDED: 64k bytes RAM, Z80 MDC board, Z80 MCB board and floppy- or hard-disk drive

PROCESSOR ALLOCATION/MANAGEMENT
- System vs User mode (ZDS system only)

PERIPHERAL MANAGEMENT
- Supports CRTs, character printers, floppy- and cartridge-disk drives, modems and PROM programmers in ZDS and PDS systems
- Provides device independence, DMA and spooling (Version 3 only)
- Uses interrupts
- Accommodates up to four 600k-byte floppy-disk drives and up to four 10M-byte cartridge-disk drives concurrently

COMMENTS: *Version 3, an enhancement of Version 2, is specifically designed for business applications. It has a fast random-access file system and features sort/merge and spooler utilities.

MEMORY MANAGEMENT
- Single contiguous allocation
- Overlays and chaining
- Static relocation
- Binding done during linking time
- Memory protection

FILE MANAGEMENT
- Named file system
- Sequential organization (Version 2 only)
- Random organization (Version 3 only)
- Indexed sequential access method (COBOL only)
- Allocation types: linked list of sectors (Version 2 only) and ISAM with a random-access table of pointers to sectors (Version 3 only)

CIRCLE NO 746

16-BIT CPU 8086 | DEVELOPMENT OPERATING SYSTEM | GENERAL-PURPOSE OPERATING SYSTEM

RS-86

Language Resources
4885 Riverbend Rd
Boulder, CO 80301
Phone (303) 449-8087

RELEASE DATE: February 1981
PRICE: $8750, Source code; $2450, Object code
TARGET MODEL: Upgrade for Intel MDS 800, II, III
SUPPORT LANGUAGES: AL/M-86 assembler; PASCAL compiler
SYSGEN PROGRAM: No **SOURCE CODE:** Yes
LANGUAGE SYSTEM: PASCAL, PL/M-86
NETWORK SUPPORT: No

SYSTEM RESIDENCY: RAM and disk
ROMABLE SYSTEM: No
MINIMUM HARDWARE NEEDED: 128k bytes memory, Intel MDS 800 or Series II or III with floppy-disk drive and iSBC 86/12 or Microbar C86 CPU

PROCESSOR ALLOCATION/MANAGEMENT
Not Available

PERIPHERAL MANAGEMENT
- Supports CRTs, character printers and ISIS II and III peripherals
- Provides device independence and DMA
- Accommodates a mix of ISIS II and III devices

MEMORY MANAGEMENT
- Single contiguous allocation
- Overlays and segmentation
- Static relocation
- Binding done during linking time

FILE MANAGEMENT
- Named file system
- Sequential and random organization
- Allocation type: linked list of sectors
- Can access file system from HLL containing constructs

CIRCLE NO 671

8-BIT CPU 6800/6809 | DEVELOPMENT OPERATING SYSTEM | GENERAL-PURPOSE OPERATING SYSTEM

SDOS

Software Dynamics
2111 W Crescent, #G
Anaheim, CA 92801
Phone (714) 635-4760

RELEASE DATE: June 1978
PRICE: $700 (includes BASIC compiler)
TARGET MODEL: Midwest Scientific Instruments, Wave Mate, Pace 480, Motorola Exorciser
SUPPORT LANGUAGES: 6800 and 6809 assemblers and 6800 to 6809 cross assembler; MSI BASIC interpreter; Business BASIC and SD compilers
SYSGEN PROGRAM: Yes **SOURCE CODE:** Yes
LANGUAGE SYSTEM: Assembly
NETWORK SUPPORT: Yes

SYSTEM RESIDENCY: RAM and disk
ROMABLE SYSTEM: No
MINIMUM HARDWARE NEEDED: 48k bytes RAM, dual floppy-disk drives, CRT and printer

PROCESSOR ALLOCATION/MANAGEMENT

- Multitasking: unlimited number of tasks for I/O package only using Post, Wait, Event, Lock and Release intertask communications
- Multiusage: eight users with 32k bytes (min) RAM per user
- Synchronizing scheme: semaphore

PERIPHERAL MANAGEMENT

- Supports CRTs, character and line printers and floppy-, hard- and cartridge-disk drives
- Provides device independence and DMA
- Uses interrupts and I/O multibuffering
- Accommodates a mix of mass-storage devices
- Allows CRT-independent cursor positioning, display coloring and data entry via virtual terminal driver

MEMORY MANAGEMENT

- Single contiguous allocation
- Chaining
- Binding done during assembly/compilation time

FILE MANAGEMENT

- Named file system
- Sequential, contiguous and random organizations
- Allocation type: extents
- Can access file system from HLL containing constructs
- Multikey indexed (BASIC only)

COMMENTS: CRT-independent screen editor available

CIRCLE NO 747

8-BIT CPU 6502 | DEVELOPMENT OPERATING SYSTEM | GENERAL-PURPOSE OPERATING SYSTEM

SDS/DOS

Scientific Data Systems Inc
344 Main St
Venice, CA 90291
Phone (213) 390-8673

RELEASE DATE: June 1977
PRICE: Depends on configuration
SUPPORT LANGUAGES: 6502 macro assembler, extended BASIC, Data Management System
SYSGEN PROGRAM: Yes **SOURCE CODE:** No
LANGUAGE SYSTEM: Assembler
NETWORK SUPPORT: File transfer via RS-232C; proprietary SDLC network of up to 255 nodes over 1 km coaxial cable

SYSTEM RESIDENCY: RAM and disk
ROMABLE SYSTEM: No
MINIMUM HARDWARE NEEDED: 32k bytes memory and 1.25M bytes diskette

PROCESSOR ALLOCATION/MANAGEMENT

- System vs User mode

PERIPHERAL MANAGEMENT

- Supports CRTs, character printers, floppy- and hard-disk drives and modems
- Provides device independence, DMA and spooling
- Uses interrupts
- Accommodates a mix of floppy- and hard-disk drives up to 65M bytes of storage capacity

MEMORY MANAGEMENT

- Single contiguous allocation
- Overlays
- Chaining
- Binding and relocation done by linking loader

FILE MANAGEMENT

- Named file system
- Sequential, contiguous and random organizations
- ISAM using binary trees
- Dynamic disk allocation/deallocation using bit map
- Can access file system from HLL

CIRCLE NO 672

EDN μC OPERATING SYSTEMS DIRECTORY

8-BIT CPU Z80A | DEVELOPMENT OPERATING SYSTEM | GENERAL-PURPOSE OPERATING SYSTEM

STARPLEX-II

National Semiconductor Corp
2900 Semiconductor Dr
Santa Clara, CA 95051
Phone (408) 737-5000

RELEASE DATE: 1981 (Rev A)
PRICE: Depends on configuration
SUPPORT LANGUAGES: 8080, Z80, 8048, NSC800 and 16032/16/08 macro assemblers; BASIC interpreter; FORTRAN, PASCAL and PLM compilers; 8070 cross assembler
SYSGEN PROGRAM: No **SOURCE CODE:** No
LANGUAGE SYSTEM: PLM/assembler
NETWORK SUPPORT: No

SYSTEM RESIDENCY: RAM and disk
ROMABLE SYSTEM: No
MINIMUM HARDWARE NEEDED: 64k bytes RAM and Starplex II development system

PROCESSOR ALLOCATION/MANAGEMENT

- System vs User mode
- Multitasking: 255 tasks can start/stop/suspend other tasks using message queues
- Multiprocessing: 1 to 15 processors using interrupt and lock
- Synchronizing scheme: monitors

PERIPHERAL MANAGEMENT

- Supports CRTs, character and line printers, floppy- and hard-disk drives, modems and PROM programmers
- Provides device independence, DMA and spooling
- Uses interrupts
- Accommodates a mix of hard-disk, single-sided single-density floppy-disk and double-sided double-density floppy-disk drives

MEMORY MANAGEMENT

- Single contiguous allocation
- Overlays and chaining
- Binding done during linking time
- Memory protection

FILE MANAGEMENT

- Named file system and multilevel directory
- Sequential and random organizations
- Allocation type: linked list of sectors
- Can access file system from HLL containing constructs

CIRCLE NO 748

8-BIT CPU 6502-BASED | DEVELOPMENT OPERATING SYSTEM | GENERAL-PURPOSE OPERATING SYSTEM

SOS

Apple Computer Inc
10260 Bandley Dr
Cupertino, CA 95014
Phone (408) 996-1010

RELEASE DATE: June 1980
PRICE: $250 (free with system purchase)
TARGET MODEL: Apple III
SUPPORT LANGUAGES: UCSD 6502 assembler; BASIC interpreter; USCD PASCAL and FORTRAN (Compile-to-P-code) compilers
SYSGEN PROGRAM: Yes **SOURCE CODE:** No
LANGUAGE SYSTEM: Assembler
NETWORK SUPPORT: No

SYSTEM RESIDENCY: RAM
ROMABLE SYSTEM: Yes
MINIMUM HARDWARE NEEDED: 96k bytes RAM and Apple III system

PROCESSOR ALLOCATION/MANAGEMENT

Not Available

PERIPHERAL MANAGEMENT

- Supports CRTs, character and line printers, floppy- and cartridge-disk drives and modems
- Provides device independence and DMA
- Uses interrupts and I/O multibuffering
- Accommodates a mix of hard- and floppy-disk drives by treating devices as independent files; opens as many as necessary

MEMORY MANAGEMENT

- Single contiguous allocation
- Overlays and chaining
- Segmentation and static relocation
- Binding during linking and loading times

FILE MANAGEMENT

- Named file system and multilevel directory
- Sequential and random organizations
- Allocation type: binary-tree index structure
- Can access file system from HLL containing constructs

CIRCLE NO 692

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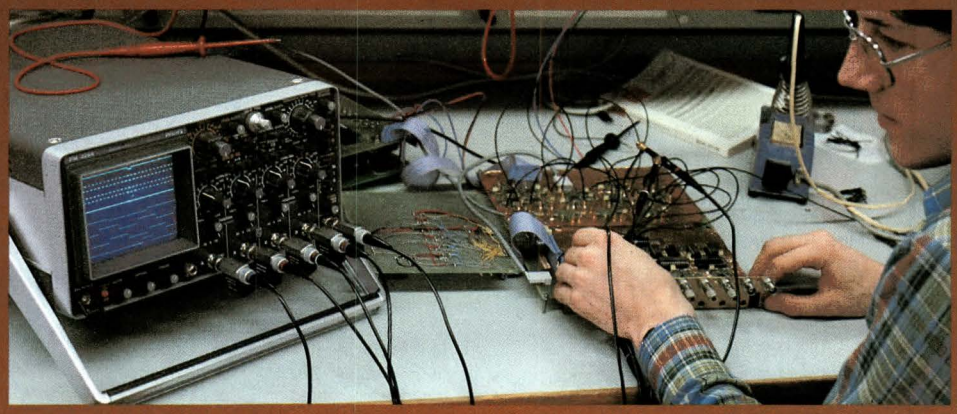

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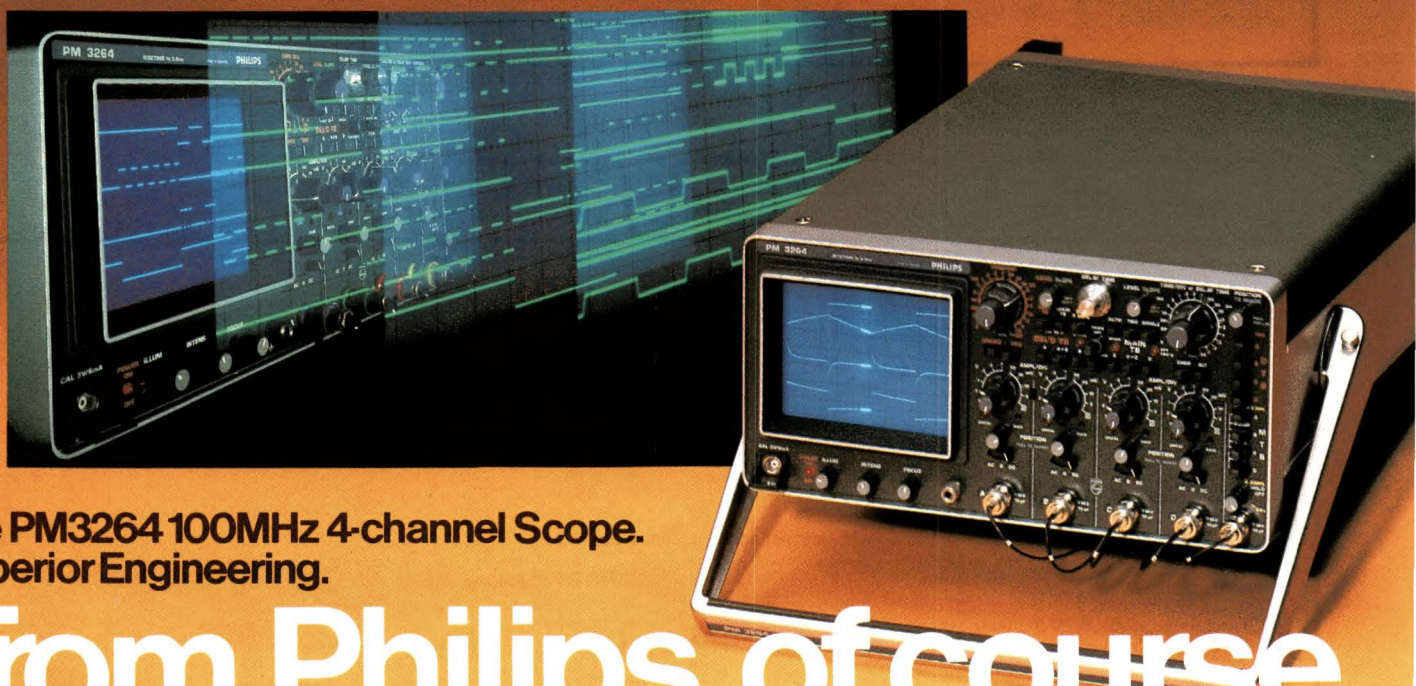

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CIRCLE NO 59

EDN-9-16-1

8-BIT CPU 6800 | DEVELOPMENT OPERATING SYSTEM | GENERAL-PURPOSE OPERATING SYSTEM

SP/68

Hemenway Associates Inc
101 Tremont St
Boston, MA 02108
Phone (617) 426-1931

RELEASE DATE: March 1979
PRICE: $150
TARGET MODEL: Various
SUPPORT LANGUAGES: Macro and various cross assemblers, structured BASIC (STRUBAL +) compiler
SYSGEN PROGRAM: No **SOURCE CODE:** Yes
LANGUAGE SYSTEM: Assembler
NETWORK SUPPORT: No

SYSTEM RESIDENCY: RAM and disk
ROMABLE SYSTEM: Yes
MINIMUM HARDWARE NEEDED: 16k bytes RAM, console and floppy-disk drive

PROCESSOR ALLOCATION/MANAGEMENT

Not Available

PERIPHERAL MANAGEMENT

- Supports CRTs, character and line printers, floppy- and cartridge-disk drives, modems, magnetic- and paper-tape drives and other devices with suitable device drivers
- Provides device independence
- Accommodates a mix of floppy- and hard-disk drives

MEMORY MANAGEMENT

- Single contiguous allocation
- Overlays
- Chaining
- Static relocation
- Binding during linking time

FILE MANAGEMENT

- Named file system
- Sequential and random organizations
- Allocation type: linked list of sectors
- Can access file system from HLL containing constructs
- Security protection

CIRCLE NO 734

16-BIT CPU WD9700, ME1600 | DEVELOPMENT OPERATING SYSTEM | GENERAL-PURPOSE OPERATING SYSTEM

UCSD PASCAL

Western Digital Computer Products
3128 Red Hill
Newport Beach, CA 92663
Phone (714) 557-3550

RELEASE DATE: May 1979
PRICE: $1000
TARGET MODEL: WD900, WD9700 and ME1600
SUPPORT LANGUAGES: Direct execution of PASCAL P code
SYSGEN PROGRAM: Yes **SOURCE CODE:** Yes
LANGUAGE SYSTEM: PASCAL
NETWORK SUPPORT: Yes

SYSTEM RESIDENCY: RAM and disk
ROMABLE SYSTEM: Yes
MINIMUM HARDWARE NEEDED: 64k bytes RAM, terminal and 8-in. floppy-disk drive

PROCESSOR ALLOCATION/MANAGEMENT

- Multitasking: number of tasks depends on memory capacity; can start/stop/suspend other tasks via intertask communication
- Synchronizing scheme: semaphore

PERIPHERAL MANAGEMENT

- Supports CRTs, character and line printers, floppy- and hard-disk drives, modems and RS-232C interface
- Provides DMA
- Uses interrupts

MEMORY MANAGEMENT

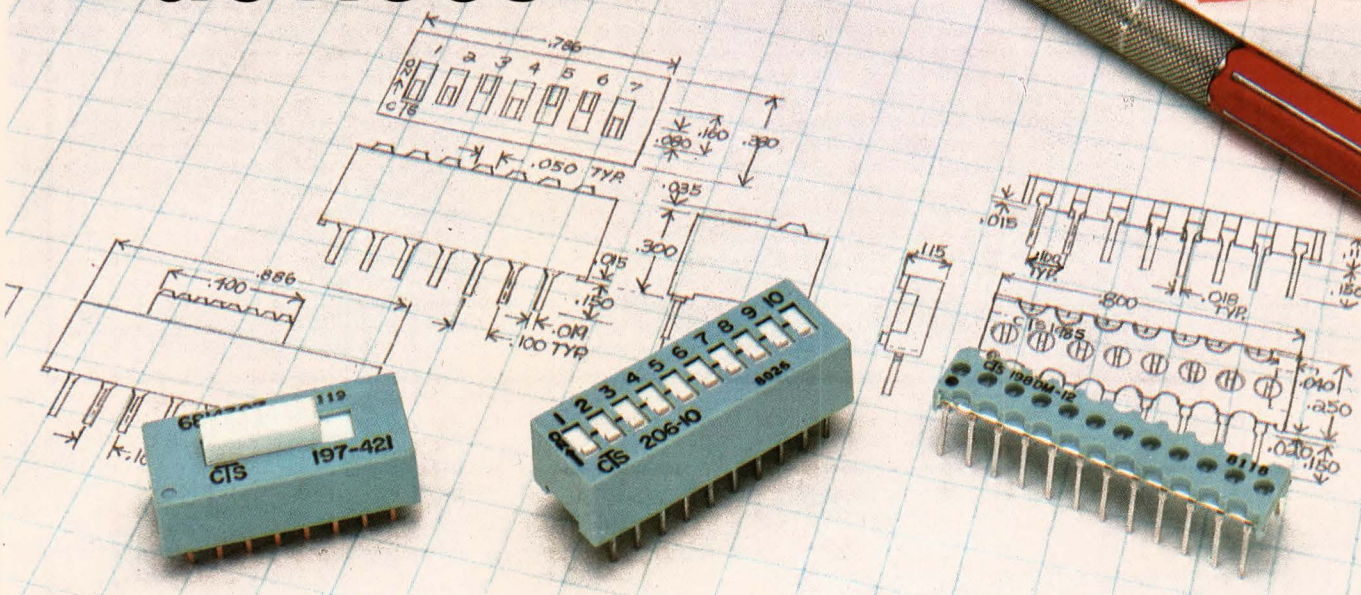
- Overlays
- Segmentation
- Binding during linking and loading times

FILE MANAGEMENT

- Named file system
- Sequential, contiguous and random organizations
- Allocation type: single contiguous
- Can access file system from HLL containing constructs

CIRCLE NO 749

CTS....a leader in programmable PC board devices.



SIP & DIP switches and shunts for increased productivity.

NEW Series 197 DIP slide switch. Here's a 4 pole, double throw slide switch that is widely used in both data processing and telecommunications. It features crisp, positive slide detent actuation, plus field-proven true self-clean contact wiping for extended switch life. Series 197 is extremely useful in "service/operate" applications, low level signal routing and digital circuit programming.

CIRCLE NO. 104

Reliable, PCB Series 206 DIP switches. Get the switch . . . SPST, SPDT, DPST, DPDT or 4PST—and options . . . low profile/extended actuators, sealed base, disposable tape sealed top or Mil approved styles you need for communication, data processing, instrumentation or consumer applications.

Each switch features crisp, positive slide detent actuation and employs time tested, true contact wiping for extended switch life. Performance engineered for high cycle life; .100" x .300" DIP centers; reliable gold plated contacts; economical.

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Series 198 programmable shunt networks. Fast and economical. For matrix and opposite terminal bussing. CTS SIP or DIP shunts are inexpensive, one-time "set and forget" programming replacements for individual jumpers and buss wiring. They're machine insertable and may be programmed in your plant or ours. Space saving SIP's in 2 through 12 pins, DIP's in 4 through 24 pins on .100" centers end to end and side by side.

CIRCLE NO. 106

For fast service and complete specs, contact your CTS distributor . . . CTS Keene, Inc., 500 Linne Road, Paso Robles, CA 93446, phone: (805) 238-0350 . . . or circle the reader number.

CTS CORPORATION
ELKHART, INDIANA

8-BIT CPU 6800 | DEVELOPMENT OPERATING SYSTEM | GENERAL-PURPOSE OPERATING SYSTEM

UCSD PASCAL

Wintek Corp
1801 South St
Lafayette, IN 47904
Phone (317) 742-8428

RELEASE DATE: July 1981
PRICE: $675
TARGET MODEL: Sprint 68
SUPPORT LANGUAGES: 6800 assembler; BASIC interpreter; PASCAL and FORTRAN compilers
SYSGEN PROGRAM: No **SOURCE CODE:** No
LANGUAGE SYSTEM: 6800 assembly, PASCAL
NETWORK SUPPORT: No

SYSTEM RESIDENCY: RAM and disk
ROMABLE SYSTEM: No
MINIMUM HARDWARE NEEDED: 56k bytes RAM

PROCESSOR ALLOCATION/MANAGEMENT
Not Available

PERIPHERAL MANAGEMENT
- Supports CRTs; dot-matrix, character and line printers; floppy- and hard-disk drives; modems and RS-232C interfaces
- Provides device independence

MEMORY MANAGEMENT
- Single contiguous allocation
- Overlays
- Swapping
- Static and dynamic relocations
- Binding during linking and loading times

FILE MANAGEMENT
- Named file system
- Sequential, contiguous and random organizations
- Allocation type: single contiguous
- Can access file system from HLL containing constructs

CIRCLE NO 673

8/16-BIT CPU 8 μC, μP Types* | DEVELOPMENT OPERATING SYSTEM | GENERAL-PURPOSE OPERATING SYSTEM

UCSD P-SYSTEM SOFTWARE

SofTech Microsystems Inc
9494 Black Mountain Rd
San Diego, CA 92126
Phone (714) 578-6105

RELEASE DATE: August 1977
PRICE: $900
TARGET MODEL: Most models for each CPU
SUPPORT LANGUAGES: All listed CPU assemblers (assembled to native code); P-code interpreter; PASCAL, FORTRAN and BASIC compilers (compiled to P code)
SYSGEN PROGRAM: Yes **SOURCE CODE:** Yes
LANGUAGE SYSTEM: PASCAL/CPU assembly
NETWORK SUPPORT: No

SYSTEM RESIDENCY: RAM and disk
ROMABLE SYSTEM: Yes
MINIMUM HARDWARE NEEDED: 48k bytes contiguous RAM, 175k bytes disk, teletypewriter or CRT display (must send and receive ASCII characters)

PROCESSOR ALLOCATION/MANAGEMENT
- Supports multitasking with arbitrary number of tasks and intertask communication
- Synchronizing scheme: semaphore

PERIPHERAL MANAGEMENT
- Supports CRTs, character and line printers, floppy- and cartridge-disk drives, modems and magnetic- and paper-tape drives
- Provides device independence and DMA
- Accommodates a mix of mass-storage devices

MEMORY MANAGEMENT
- Single contiguous allocation
- Overlays
- Dynamic relocation
- Binding done during linking and loading times

FILE MANAGEMENT
- Named file system
- Sequential, contiguous and random organizations
- Allocation type: single contiguous
- Can access file system from HLL containing constructs

COMMENTS: *LSI-11, PDP-11, 6502, Z80, 8080, 6809, 9900 and 8086

CIRCLE NO 750

EDN μC OPERATING SYSTEMS DIRECTORY

16-BIT CPU
8086/68000/Z8000/PDP-11

DEVELOPMENT
OPERATING SYSTEM

GENERAL-PURPOSE
OPERATING SYSTEM

XENIX

Microsoft
10800 NE 8th St, Suite 819
Bellevue, WA 98004
Phone (206) 455-8080

RELEASE DATE: 3rd qtr 1981
PRICE: OEM contracts
TARGET MODEL: PDP-11 Series, Z8000, 8086 and 68000
SUPPORT LANGUAGES: C compiler included; other Microsoft language compilers available
SYSGEN PROGRAM: Yes **SOURCE CODE:** No
LANGUAGE SYSTEM: C
NETWORK SUPPORT: Yes

SYSTEM RESIDENCY: RAM
ROMABLE SYSTEM: No
MINIMUM HARDWARE NEEDED: 192k bytes RAM

PROCESSOR ALLOCATION/MANAGEMENT

- System vs User mode
- Multitasking: 100 tasks, restricted by table size, can start/stop/suspend other tasks via interprocessor message buffers and software asynchronous interrupts
- Multiusage: one to 25 users
- Synchronizing scheme: file structure with user-implemented locks

PERIPHERAL MANAGEMENT

- Supports CRTs, character and line printers, floppy- and cartridge-disk drives, modems and magnetic- and paper-tape drives
- Provides device independence and user writable device driver
- Uses interrupts and I/O multibuffering
- Accommodates a mix of different mass-storage devices that support multiple file systems and device drivers

MEMORY MANAGEMENT

- Segmentation
- Swapping
- Dynamic relocation
- Binding done during assembly/compilation, linking and loading times
- Memory protection

FILE MANAGEMENT

- Named file system
- Multilevel directory
- Sequential organization
- Allocation type: linked list of sectors
- Password/security protection

COMMENTS: XENIX is a Level 7 UNIX operating system

CIRCLE NO 680

8-BIT CPU
Z80

GENERAL-PURPOSE
OPERATING SYSTEM

CDOS

Cromemco Inc
280 Bernardo Ave
Mt View, CA 94043
Phone (415) 964-7400

RELEASE DATE: 1977
PRICE: $95
SUPPORT LANGUAGES: Z80 Macro assembler, BASIC and LISP interpreters, FORTRAN, COBOL and RPG II compilers
SYSGEN PROGRAM: Yes **SOURCE CODE:** No
LANGUAGE SYSTEM: Z80 assembler
NETWORK SUPPORT: No

SYSTEM RESIDENCY: RAM
ROMABLE SYSTEM: No
MINIMUM HARDWARE NEEDED: 32k bytes RAM

PROCESSOR ALLOCATION/MANAGEMENT

Not Available

PERIPHERAL MANAGEMENT

- Supports CRTs, character and line printers, floppy- and hard-disk drives and modems
- Provides DMA
- Accommodates a mix of floppy- and hard-disk drives

MEMORY MANAGEMENT

- Single contiguous allocation
- Overlays

FILE MANAGEMENT

- Named file system
- Sequential and random organizations
- Indexed sequential access method (ISAM)
- Allocation type: linked list of sectors
- Can access file system from HLL containing constructs

COMMENTS: CDOS is upwardly compatible from CP/M

CIRCLE NO 682

EDN μC OPERATING SYSTEMS DIRECTORY

16-BIT CPU
TI990

GENERAL-PURPOSE
OPERATING SYSTEM

COS990

Ryan-McFarland Inc
2111 North Mays
Round Rock, TX 78664
Phone (512) 255-7823

RELEASE DATE: March 1980
PRICE: $2000
TARGET MODELS: 1-30
SUPPORT LANGUAGES: COBOL compiler
SYSGEN PROGRAM: No
SOURCE CODE: No
LANGUAGE SYSTEM: Assembly and POPS
NETWORK SUPPORT: No

SYSTEM RESIDENCY: RAM and disk
ROMABLE SYSTEM: Yes
MINIMUM HARDWARE NEEDED: 64k bytes memory and floppy- or hard-disk drive

PROCESSOR ALLOCATION/MANAGEMENT

- System vs User mode
- Multitasking: 110 tasks can start/stop/suspend other tasks via intertask communication
- Multiusage: 60 users with 6k bytes (min) RAM per user
- Synchronizing scheme: semaphore

PERIPHERAL MANAGEMENT

- Supports CRTs; character printers; floppy-, hard- and cartridge-disk drives and modems
- Provides device independence, DMA and spooling
- Uses interrupts and I/O multibuffering
- Accommodates a mix of disk drives

MEMORY MANAGEMENT

- Overlays
- Swapping and segmentation
- Static and dynamic relocations
- Binding done during loading time

FILE MANAGEMENT

- Named file system and multilevel directory
- Sequential and random organization
- Indexed sequential access method with 15 keys
- Allocation type: up to 23 noncontiguous extents
- Can access file system from HLL containing constructs
- Password/security protection

CIRCLE NO 674

8-BIT CPU
8080/8085/Z80

GENERAL-PURPOSE
OPERATING SYSTEM

CP/M

Lifeboat Associates
1651 Third Ave
New York, NY 10028
Phone (212) 860-0300

RELEASE DATE: 1976
PRICE: From $145
TARGET MODEL: North Star, Ohio Scientific, TRS-80 II, Heath/Zenith, Datapoint 1550 and >50 others
SUPPORT LANGUAGES: 8080, 8085 and Z80 assemblers; 1802, 8086, 6502, 6800 and 8048 cross-assemblers; BASIC and LISP interpreters; BASIC, FORTRAN, COBOL, PASCAL, APL, ALGOL and C compilers
SYSGEN PROGRAM: Yes
SOURCE CODE: No
LANGUAGE SYSTEM: 8080 assembler
NETWORK SUPPORT: No

SYSTEM RESIDENCY: RAM and disk
ROMABLE SYSTEM: No
MINIMUM HARDWARE NEEDED: 24k bytes RAM and disk system

PROCESSOR ALLOCATION/MANAGEMENT

Not Available

PERIPHERAL MANAGEMENT

- Supports CRTs, character and line printers, floppy- and cartridge-disk drives, modems, magnetic- and paper-tape drives, plotters and voice synthesizers
- Provides device independence and DMA
- Uses interrupts
- Accommodates a mix of floppy-, mini-floppy- and 8-in.-Winchester disk drives, as well as 14-in.-Winchester and cartridge-disk drives

MEMORY MANAGEMENT

- Single contiguous allocation
- Chaining
- Binding during linking time

FILE MANAGEMENT

- Named file system
- Sequential organization
- Allocation type: extents
- Can access file system from HLL containing constructs

CIRCLE NO 683

EDN μC OPERATING SYSTEMS DIRECTORY

8-BIT CPU
Z80A

GENERAL-PURPOSE OPERATING SYSTEM

CROMIX

Cromemco Inc
280 Bernardo Ave
Mt View, CA 94043
Phone (415) 964-7400

RELEASE DATE: September 1980
PRICE: $595
SUPPORT LANGUAGES: Z80A macro assembler; BASIC and LISP interpreters; FORTRAN, COBOL, RPG II and C compilers
SYSGEN PROGRAM: Yes **SOURCE CODE:** No
LANGUAGE SYSTEM: Assembler
NETWORK SUPPORT: No

SYSTEM RESIDENCY: RAM
ROMABLE SYSTEM: Yes
MINIMUM HARDWARE NEEDED: 128k bytes RAM

PROCESSOR ALLOCATION/MANAGEMENT

- System vs User mode
- Multitasking: seven tasks can start/stop/suspend other tasks via intertask communication
- Multiusage: seven users with 64k bytes (min) RAM per user
- Multiprocessing: unlimited number of processors via interrupt-driven synchronizing scheme

PERIPHERAL MANAGEMENT

- Supports CRTs, character and line printers, floppy- and hard-disk drives and modems
- Provides device independence, DMA and spooling
- Uses interrupts and I/O multibuffering
- Accommodates a mix of floppy- and hard-disk drives

MEMORY MANAGEMENT

- Single contiguous allocation
- Overlays
- Swapping and chaining
- Static relocation
- Memory protection

FILE MANAGEMENT

- Named file system and multilevel directory
- Sequential binary-tree organization
- Indexed sequential access method (ISAM)
- Allocation type: extents
- Can access file system from HLL containing constructs
- Password/security protection

COMMENTS: CROMIX resembles the UNIX operating system

CIRCLE NO 684

16-BIT CPU
8086

GENERAL-PURPOSE OPERATING SYSTEM

CTOS

Convergent Technologies
2500 Augustine Dr
Santa Clara, CA 95051
Phone (408) 727-8830

RELEASE DATE: October 1980
PRICE: Bundled
TARGET MODEL: Firm's desktop minicomputers
SUPPORT LANGUAGES: 8086 ASM; BASIC interpreter; PASCAL, COBOL and FORTRAN compilers
SYSGEN PROGRAM: Yes **SOURCE CODE:** No
LANGUAGE SYSTEM: PL/M-86
NETWORK SUPPORT: Yes [2-16 workstations and remote host(s)]

SYSTEM RESIDENCY: RAM and disk
ROMABLE SYSTEM: No
MINIMUM HARDWARE NEEDED: 128k bytes RAM and dual floppy-disk drives

PROCESSOR ALLOCATION/MANAGEMENT

- Multitasking: number of tasks depends on system mapping using intertask communication; tasks can start other tasks using mailbox synchronizing scheme
- Multiusage: up to 16 per cluster, one per workstation, with 128k bytes (min) of RAM per user
- Multiprocessing: supports 8086 and (optional) 8087 using hardware synchronizing scheme

PERIPHERAL MANAGEMENT

- Supports CRTs, character and line printers, floppy- and hard-disk drives, modems and expandable Multibus
- Provides device independence, DMA and spooling
- Uses interrupts and I/O multibuffering
- Accommodates dual floppy-disk drives or one floppy-disk drive and up to three hard-disk drives

MEMORY MANAGEMENT

- Single contiguous allocation
- Overlays
- Chaining and segmentation
- Static relocation
- Binding done during linking time

FILE MANAGEMENT

- Named file system
- Sequential, contiguous and random organizations
- Indexed sequential access method
- Allocation type: extents
- Can access file system from HLL containing constructs
- Password/security protection

CIRCLE NO 675

EDN μC OPERATING SYSTEMS DIRECTORY

8-BIT CPU
6502

GENERAL-PURPOSE OPERATING SYSTEM

DOS 3.3

Apple Computer Inc
10260 Bandley Dr
Cupertino, CA 95014
Phone (408) 996-1010

RELEASE DATE: July 1980
PRICE: $200
TARGET MODEL: Apple II
SUPPORT LANGUAGES: 6502 assembler; floating-point BASIC and integer BASIC interpreters
SYSGEN PROGRAM: No **SOURCE CODE:** No
LANGUAGE SYSTEM: 6502 assembler
NETWORK SUPPORT: No

SYSTEM RESIDENCY: RAM and disk
ROMABLE SYSTEM: No
MINIMUM HARDWARE NEEDED: 32k bytes RAM and 143k bytes Disk II floppy-disk drive

PROCESSOR ALLOCATION/MANAGEMENT

Not Available

PERIPHERAL MANAGEMENT

- Supports CRTs, character and line printers, floppy- and cartridge-disk drives, modems, A/D converters, IEEE-488 interfaces, digitizers, plotters, voice-recognition devices and speech and music synthesizers
- Provides device independence and DMA
- Uses I/O multibuffering
- Accommodates a mix of mass-storage devices using associated controllers

MEMORY MANAGEMENT

- Single contiguous allocation
- Overlays
- Chaining
- Memory protection

FILE MANAGEMENT

- Named file system
- Sequential and random organizations
- Allocation type: linked list of sectors
- Can access file system from HLL containing constructs

CIRCLE NO 737

16-BIT CPU
CS/10 Systems

GENERAL-PURPOSE OPERATING SYSTEM

ICOS

Data General Corp
440 Computer Dr
Westboro, MA 01580
Phone (617) 366-8911

RELEASE DATE: May 1977
PRICE: $2500
TARGET MODEL: DG CS/10
SUPPORT LANGUAGES: COBOL compiler
SYSGEN PROGRAM: No **SOURCE CODE:** No
LANGUAGE SYSTEM: Assembler
NETWORK SUPPORT: No

SYSTEM RESIDENCY: Disk
ROMABLE SYSTEM: No
MINIMUM HARDWARE NEEDED: 64k bytes RAM, disk or diskette, printer and CRT

PROCESSOR ALLOCATION/MANAGEMENT

- Multitasking: up to four tasks can start/stop/suspend other tasks via intertask communication
- Multiusage: up to four users
- Synchronizing scheme: monitor

PERIPHERAL MANAGEMENT

- Supports CRTs, character and line printers, floppy- and cartridge-disk drives, modems and magnetic-tape drives
- Provides device independence and spooling
- Uses interrupts and I/O multibuffering
- Accommodates two dual quad-density 1.2M-byte diskettes or one dual quad-density 12.5M- or 25M-byte Winchester disk

MEMORY MANAGEMENT

- Overlays
- Swapping and chaining
- Segmentation and dynamic relocation
- Binding during assembly/compilation time
- Memory protection

FILE MANAGEMENT

- Named file system and multilevel directory
- Sequential, contiguous and random organizations
- Indexed sequential access method (ISAM)
- Allocation type: single contiguous
- Can access file system from HLL containing constructs
- Password/security protection

CIRCLE NO 685

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Systems Engineering Laboratories, Inc., 6901 W. Sunrise Blvd., Ft. Lauderdale, FL 33313. (305) 587-2900, 1-800-327-9716.

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CIRCLE NO 60

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EDN μC OPERATING SYSTEMS DIRECTORY

16-BIT CPU
Nova Series

GENERAL-PURPOSE OPERATING SYSTEM

IRIS

Point 4 Data Corp
2569 McCabe Way
Irvine, CA 92714
Phone (714) 754-4114

RELEASE DATE: 1972
PRICE: $3600
TARGET MODEL: Micronova and Point 4 Mark III
SUPPORT LANGUAGES: Macro and absolute assemblers; BASIC and PASCAL interpreters; PASCAL compiler
SYSGEN PROGRAM: Yes **SOURCE CODE:** Yes
LANGUAGE SYSTEM: Assembly, PASCAL
NETWORK SUPPORT: Furnishes own protocol, and BSC with outboard controller

SYSTEM RESIDENCY: RAM and disk
ROMABLE SYSTEM: No
MINIMUM HARDWARE NEEDED: 48k bytes RAM, 500k bytes disk and operator's terminal

PROCESSOR ALLOCATION/MANAGEMENT

- System vs User mode
- Multitasking: up to 128 tasks can start/stop/suspend other tasks by signal statements
- Multiusage: up to 128 users with 256 bytes (min) RAM per user
- Synchronizing scheme: semaphor and monitor

PERIPHERAL MANAGEMENT

- Supports CRTs, character and line printers, floppy, and cartridge-disk drives, modems and magnetic- and paper-tape drives
- Provides device independence, DMA and spooling
- Uses interrupts and I/O multibuffering
- Accommodates a mix of floppy- and hard-disk drives, depending on local memory space

MEMORY MANAGEMENT

- Overlays
- Swapping and chaining
- Dynamic relocation
- Binding during loading time

FILE MANAGEMENT

- Named file system and multilevel directory
- Sequential, contiguous and random organizations
- Indexed sequential access method (ISAM)
- Allocation types; linked list of sectors, extents and single contiguous
- Can access file system from HLL containing constructs
- Password/security protection

CIRCLE NO 686

8-BIT CPU
6502

GENERAL-PURPOSE OPERATING SYSTEM

OS-65D

Ohio Scientific Inc
1333 S Chillicothe Rd
Aurora, OH 44202
Phone (216) 562-5177

RELEASE DATE: June 1977
PRICE: $79
TARGET MODEL: C2-C3 Series, C1P-MF, C4P-DF, C8P-DF
SYSGEN PROGRAM: No **SOURCE CODE:** No
LANGUAGE SYSTEM: 6502 machine code
NETWORK SUPPORT: No

SYSTEM RESIDENCY: RAM
ROMABLE SYSTEM: No
MINIMUM HARDWARE NEEDED: 24k bytes RAM, floppy-disk drive and C1P, C4P or C8P-DF computer

PROCESSOR ALLOCATION/MANAGEMENT

Not Available

PERIPHERAL MANAGEMENT

- Supports CRTs, line printers and floppy-disk drives

MEMORY MANAGEMENT

- Single-contiguous allocation
- Binding at program entry

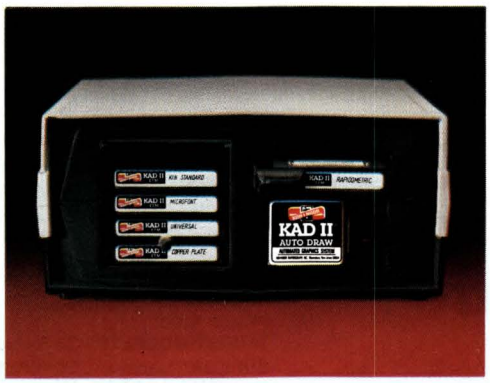
FILE MANAGEMENT

- Named file system
- Sequential, contiguous and random organizations
- Allocation type: single contiguous
- Can access file system from HLL containing constructs

CIRCLE NO 688

The KAD II Koh-I-Noor Auto Draw is electronically controlled to produce rapidly a virtually limitless library of lettering styles, symbols and designs used in engineering, electronic and architectural drawings, as well as the drawings of many other disciplines. Once demonstrated, KAD II requires no special operating skills.

KAD II consists of three components. The PLOTTER, less than four pounds, adapts to almost every drafting machine. It draws with liquid ink in any one of five preprogrammed character heights on most drawing surfaces. Servo motors operate the pen holder to produce faster and better quality characters than can be provided by any hand lettering device.



The CONTROLLER contains the logic circuitry to operate the Plotter. It drives the Plotter by commands from a standard or custom preprogrammed ELECTRONIC TEMPLATE MODULE (ETM) placed into a receptacle in the front panel. The Controller can be placed on the drawing board, on a roll-away stand, or any other handy location within cable length of the Plotter. ETM's are quickly interchangeable to provide different symbols or lettering styles as required. Each ETM has its own corresponding keyboard overlay indicating its preprogrammed functions. Send the coupon today.

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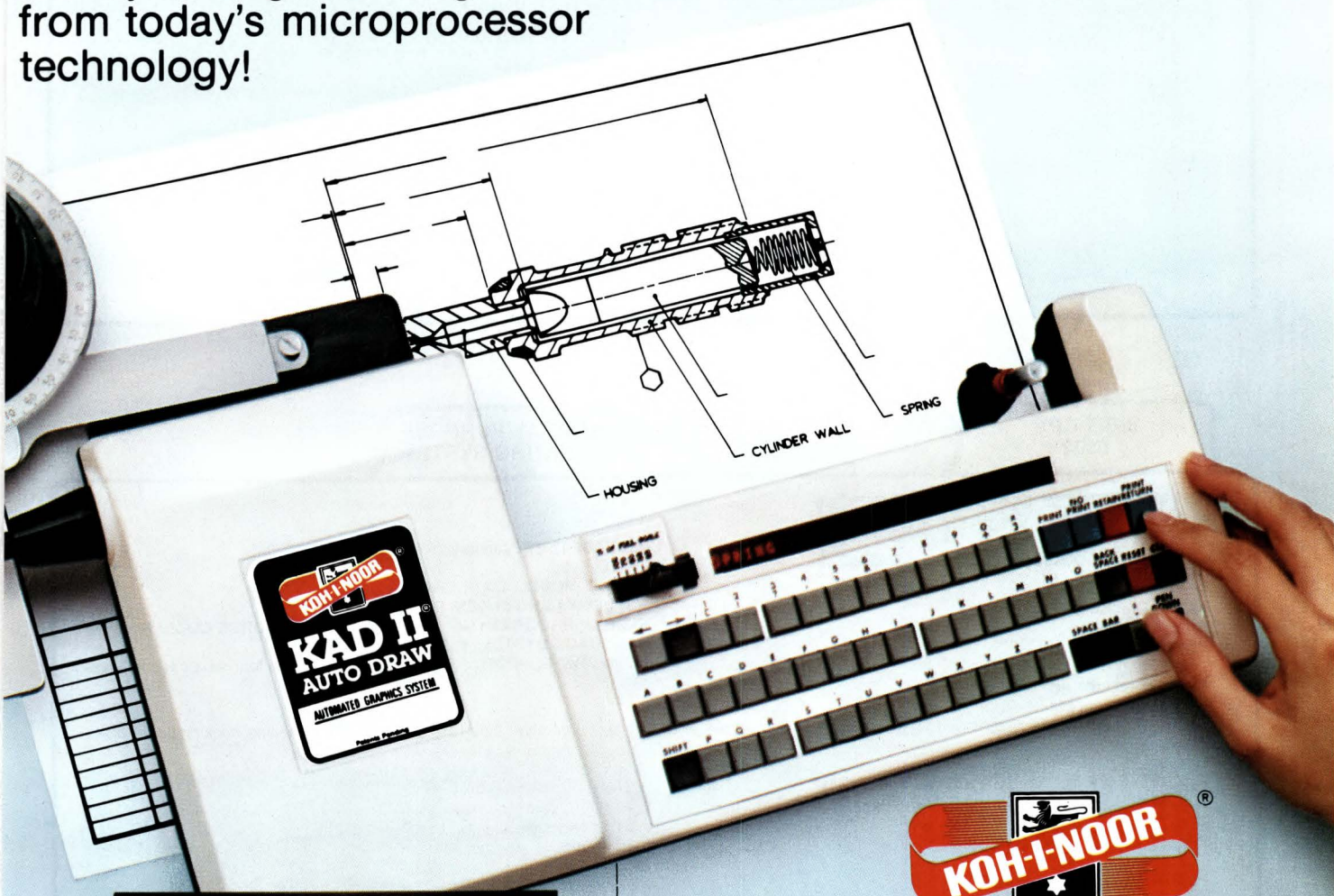

CIRCLE NO 61

KOH-I-NOOR®

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Firm _____

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City _____ State _____ Zip _____

KOH-I-NOOR RAPIDOGRAPH, INC., Bloomsbury, NJ 08804 800-631-7646.
In Canada: 1815 Meyerside Dr., Mississauga, Ont. L5T 1B4 800-268-4961.

EDN-9-16-81

8-BIT CPU
6502

GENERAL-PURPOSE
OPERATING SYSTEM

OS-65U LEVEL I

Ohio Scientific Inc
1333 S Chillicothe Rd
Aurora, OH 44202
Phone (216) 562-5177

RELEASE DATE: 1977
PRICE: $200
TARGET MODEL: C2-C3 Series
SUPPORT LANGUAGES: BASIC interpreter
SYSGEN PROGRAM: No
SOURCE CODE: No
LANGUAGE SYSTEM: 6502 machine code
NETWORK SUPPORT: No

SYSTEM RESIDENCY: RAM
ROMABLE SYSTEM: No
MINIMUM HARDWARE NEEDED: 32k bytes RAM, dual floppy-disk drives and/or hard-disk drive and C2 or C3 Series computer

PROCESSOR ALLOCATION/MANAGEMENT
Not Available

PERIPHERAL MANAGEMENT
- Suppports CRTs, line printers, floppy- and hard-disk drives and paper-tape drives
- Accommodates one hard-disk drive and two double-sided floppy-disk drives with cassette-tape backup for hard-disk drive

MEMORY MANAGEMENT
- Single contiguous allocation
- Binding at program entry

FILE MANAGEMENT
- Named file system
- Sequential, contiguous and random organizations
- Allocation type: single contiguous
- Can access file system from HLL containing constructs
- Password/security protection

CIRCLE NO 689

8-BIT CPU
6502

GENERAL-PURPOSE
OPERATING SYSTEM

OS-65U LEVEL III NET

Ohio Scientific Inc
1333 S Chillicothe Rd
Aurora, OH 44202
Phone (216) 562-5177

RELEASE DATE: January 1980
PRICE: $995
TARGET MODEL: C3-B, C3-C
SUPPORT LANGUAGES: BASIC interpreter
SYSGEN PROGRAM: No
SOURCE CODE: No
LANGUAGE SYSTEM: 6502 machine code
NETWORK SUPPORT: Two time-sharing and/or four smart terminals

SYSTEM RESIDENCY: RAM
ROMABLE SYSTEM: No
MINIMUM HARDWARE NEEDED: 104k bytes RAM, CD-74, CD-36 or CD-23 hard-disk drive, 2-port RS-232 board and real-time clock on floppy-disk controller

PROCESSOR ALLOCATION/MANAGEMENT
- Multiusage; up to eight time-sharing and/or four smart terminals with 32k bytes (min) RAM per user
- Synchronizing scheme: semaphore

PERIPHERAL MANAGEMENT
- Supports CRTs, line printers, floppy- and hard-disk drives and magnetic-tape drives
- Uses interrupts
- Accommodates one hard-disk drive and dual floppy-disk drives

MEMORY MANAGEMENT
- Single contiguous allocation
- Segmentation
- Binding at program entry

FILE MANAGEMENT
- Named file system
- Sequential, contiguous and random organizations
- Allocation type: single contiguous
- Can access file system from HLL containing constructs
- Password/security protection

CIRCLE NO 690

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50-150 VOLTS	OUR T0220 (VARO VHE2401-2403)	THEIR T0220 (UES2401-2403)
Forward Current	20A	16A
Overvoltage Protection	20%	Not specified
Thermal Impedance	1.5°c/w	1.75°c/w
High Temp. Leakage @ 100°C	50μA	150μA
Peak Surge Current (½ cycle, non-rep.)	150A	80A
Glass Passivated	Yes	No

200 VOLTS	OUR T0220 (VARO VHE2404)	THEIR T0220
Forward Current	20A	Not listed in 1980 catalog
Overvoltage Protection	20%	Not listed in 1980 catalog
Thermal Impedance	1.5°c/w	Not listed in 1980 catalog
High Temp. Leakage @ 100°C	50μA	Not listed in 1980 catalog
Peak Surge Current (½ cycle, non-rep.)	150A	Not listed in 1980 catalog
Glass Passivated	Yes	Not listed in 1980 catalog

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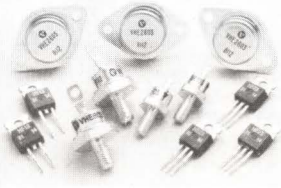

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CIRCLE NO 62

8-BIT CPU
Z80A

GENERAL-PURPOSE
OPERATING SYSTEM

RIO/CP

Zilog Inc
10460 Bubb Rd
Cupertino, CA 95014
Phone (408) 446-4666

RELEASE DATE: June 1980
PRICE: $500
TARGET MODEL: MCZ-2 Series systems, SDS 2/01
SUPPORT LANGUAGES: Z80 assembler; BASIC interpreter; COBOL and PLZ/SYS compilers
SYSGEN PROGRAM: Yes **SOURCE CODE:** No
LANGUAGE SYSTEM: Assembly and PLZ
NETWORK SUPPORT: Z-NET: single-channel packet-switched multiple-access network, transparent to OS, supports up to 255 nodes (processors)

SYSTEM RESIDENCY: RAM and disk
ROMABLE SYSTEM: No
MINIMUM HARDWARE NEEDED: 64k bytes RAM and MCZ-2 μC system (or SDS 2/01)

PROCESSOR ALLOCATION/MANAGEMENT
- Multitasking: 20 tasks start/stop/suspend other tasks through intertask communication, but all must reside concurrently in memory
- Synchronizing scheme: semaphore

PERIPHERAL MANAGEMENT
- Supports CRTs, character printers, floppy- and cartridge-disk drives and modems
- Provides device independence, DMA and spooling
- Uses interrupts
- Accommodates up to four double-sided, double-density floppy-disk drives with MCZ-2 and expands from 10M to 40M bytes of cartridge-disk storage with each SDS system

MEMORY MANAGEMENT
- Single contiguous allocation
- Overlays and chaining
- Static relocation
- Binding during linking time
- Memory protection

FILE MANAGEMENT
- Named file system and multilevel directory (SDS 2/01 only)
- Sequential and random organizations
- Indexed sequential access method (ISAM) (COBOL only)
- Accesses file system with random-access table of pointers to sectors and also from HLL
- Password/security protection for multivolume files (SDS 2/01 only)

CIRCLE NO 691

8-BIT CPU
Z80

GENERAL-PURPOSE
OPERATING SYSTEM

TIS-APL

Telecompute Integrated Systems Inc
251 Spandina Ave
Toronto, Ontario, Canada
Phone (416) 363-9295

RELEASE DATE: September 1979
PRICE: $1195
TARGET MODEL: Altos, Superbrain, TRS-80 II, North Star, Sorcerer
SUPPORT LANGUAGES: APL interpreter
SYSGEN PROGRAM: No **SOURCE CODE:** No
LANGUAGE SYSTEM: Machine language and TIS-APL assembler and disassembler
NETWORK SUPPORT: Yes

SYSTEM RESIDENCY: RAM
ROMABLE SYSTEM: No
MINIMUM HARDWARE NEEDED: 64k bytes RAM

PROCESSOR ALLOCATION/MANAGEMENT
- Multiprocessing: each node supports up to four processors

PERIPHERAL MANAGEMENT
- Supports CRTs, character and line printers and floppy- and hard-disk drives
- Provides device independence and DMA
- Accommodates a mix of floppy- and hard-disk drives

MEMORY MANAGEMENT
- Single contiguous allocation
- Overlays
- Chaining
- Binding done during loading time
- Memory protection at high end

FILE MANAGEMENT
- Named file system and multilevel directory
- Contiguous and random organizations
- Allocation type: single contiguous
- Can access file system from HLL using file commands

CIRCLE NO 693

8-BIT CPU
Z80

GENERAL-PURPOSE OPERATING SYSTEM

TPM

Computer Design Labs
342 Columbus Ave
Trenton, NJ 08629
Phone (609) 599-2146

RELEASE DATE: February 1979
PRICE: $79.95
TARGET MODEL: S-100, TRS-80
SUPPORT LANGUAGES: QSAL and Z80/8080 Macro assemblers; BASIC, APL and LIST interpreters; BASIC, FORTRAN, COBOL and PASCAL compilers
SYSGEN PROGRAM: Yes **SOURCE CODE:** Yes
LANGUAGE SYSTEM: Assembler
NETWORK SUPPORT: No

SYSTEM RESIDENCY: RAM and disk
ROMABLE SYSTEM: No
MINIMUM HARDWARE NEEDED: 32k bytes RAM, Z80 and disk controller (>15 types supported)

PROCESSOR ALLOCATION/MANAGEMENT
Not Available

PERIPHERAL MANAGEMENT
- Supports CRTs, character and line printers, floppy- and cartridge-disk drives, modems and magnetic- and paper-tape drives
- Provides device independence, DMA and spooling
- Accommodates a mix of mass-storage devices with table-driven approach; only available memory limits number of devices

MEMORY MANAGEMENT
- Single contiguous memory
- Overlays
- Swapping
- Chaining

FILE MANAGEMENT
- Named file system
- Random organization
- Allocation type: extents

CIRCLE NO 694

16-BIT CPU
Z8001

GENERAL-PURPOSE OPERATING SYSTEM

ZEUS*

Zilog Inc
10460 Bubb Rd
Cupertino, CA 95014
Phone (408) 446-4666

RELEASE DATE: November 1981
PRICE: NA
TARGET MODEL: Z-LAB 8000
SUPPORT LANGUAGES: C, PASCAL, PLZ/SYS and COBOL compilers; Z8, Z8001 and Z8002 PLZ/ASM assemblers
SYSGEN PROGRAM: Yes **SOURCE CODE:** No
LANGUAGE SYSTEM: C and PLZ/ASM
NETWORK SUPPORT: Yes, UUCP

SYSTEM RESIDENCY: Disk
ROMABLE SYSTEM: No
MINIMUM HARDWARE NEEDED: 256k byte memory and Z-LAB 8000 CPU

PROCESSOR ALLOCATION/MANAGEMENT
- System vs User mode
- Multitasking: 200 tasks can start/stop/suspend other tasks via intertask communication
- Multiusage: 16 users with 64k bytes (approx) RAM per user
- Synchronizing scheme: pipes and signals

PERIPHERAL MANAGEMENT
- Supports RS-232 terminals, character and line printers, hard-disk drives, cartridge-tape drives and modems
- Provides device independence, DMA and spooling
- Uses interrupts and I/O multibuffering

COMMENTS: *OS is an enhanced version of Bell Labs's UNIX operating system.

MEMORY MANAGEMENT
- Single contiguous allocation
- Overlays and swapping
- Static relocation
- Memory protection
- Binding done during linking time

FILE MANAGEMENT
- Named file system and multilevel directory
- Sequential, contiguous and random organizations
- Indexed sequential access method (COBOL only)
- Allocation type: linked list of sectors
- Can access file system from HLL containing constructs
- Password/security protection

CIRCLE NO 676

EDN μC OPERATING SYSTEMS DIRECTORY

16-BIT CPU
Z8000

GENERAL-PURPOSE
OPERATING SYSTEM

ZMOS

Central Data Corp
Box 2530, Stn A
Champaign, IL 61820
Phone (217) 359-8010

RELEASE DATE: August 1980
PRICE: $450
TARGET MODEL: Segmented
SUPPORT LANGUAGES: Z8000 assembler; BASIC interpreter; COBOL compiler
SYSGEN PROGRAM: Yes **SOURCE CODE:** Yes
LANGUAGE SYSTEM: Assembly
NETWORK SUPPORT: No

SYSTEM RESIDENCY: RAM and disk
ROMABLE SYSTEM: No
MINIMUM HARDWARE NEEDED: 96k bytes RAM, serial I/O port, Z8000 CPU board and floppy- or cartridge-disk drive

PROCESSOR ALLOCATION/MANAGEMENT

- System vs User mode
- Multitasking: 254 tasks can start/stop/suspend other tasks with flags and temporary and permanent common memory
- Multiusage: 64 users with 8k to 16k bytes (min) RAM per user
- Synchronizing scheme: mailbox

PERIPHERAL MANAGEMENT

- Supports CRTs, character and line printers, floppy- and cartridge-disk drives, modems and magnetic- and paper-tape drives
- Provides device independence and DMA
- Uses interrupts and I/O multibuffering
- Accommodates a mix of floppy-, cartridge- and Winchester-disk drives using device drivers

MEMORY MANAGEMENT

- Swapping
- Segmentation
- Dynamic relocation
- Binding done during assembly/compilation or linking time
- Memory protection

FILE MANAGEMENT

- Named file system
- Sequential and random organizations
- Indexed sequential access method (ISAM)
- Allocation type: extents: pointers in main directory for file; 77 entries, each entry has starting sector number and number of sectors
- Can access file system from HLL containing constructs
- Password/security protection

CIRCLE NO 695

8/16-BIT CPU
Multiple μP Types*

DEVELOPMENT
OPERATING SYSTEM

AMIX 3.0**

American Microsystems Inc
3800 Homestead Rd
Santa Clara, CA 95051
Phone (408) 246-0330

RELEASE DATE: May 1981
PRICE: $550 plus $125 per assembler
TARGET MODELS: AMI Phoenix I, Intel MDS, Motorola Exorciser and TI 990/4
SUPPORT LANGUAGES: Related processor assemblers; PASCAL and FORTRAN-77 compilers
SYSGEN PROGRAM: No **SOURCE CODE:** No
LANGUAGE SYSTEM: PASCAL
NETWORK SUPPORT: No

SYSTEM RESIDENCY: RAM and disk
ROMABLE SYSTEM: No
MINIMUM HARDWARE NEEDED: 48k bytes RAM and dual floppy-disk drives

PROCESSOR ALLOCATION/MANAGEMENT

Not Available

PERIPHERAL MANAGEMENT

- Supports CRTs, character and line printers, floppy-disk drives, modems, PROM programmers and in-circuit emulators
- Provides device independence
- Uses interrupts and I/O multibuffering

MEMORY MANAGEMENT

- Single contiguous allocation
- Overlays
- Swapping and segmentation
- Static relocation
- Binding during assembly/compilation, linking and loading times

FILE MANAGEMENT

- Named file system
- Sequential and contiguous organizations
- Allocation type: single contiguous
- Can access file system from HLL containing constructs

COMMENTS: *6800, 8080, 8085, Z80, 9900, S2000, 6502, 2650, S2200, 6801, 6805, 6809, 68000, 8021 and 8048. **Version 3.0 is an upgrade of Version 2.6 (October 1979)

CIRCLE NO 696

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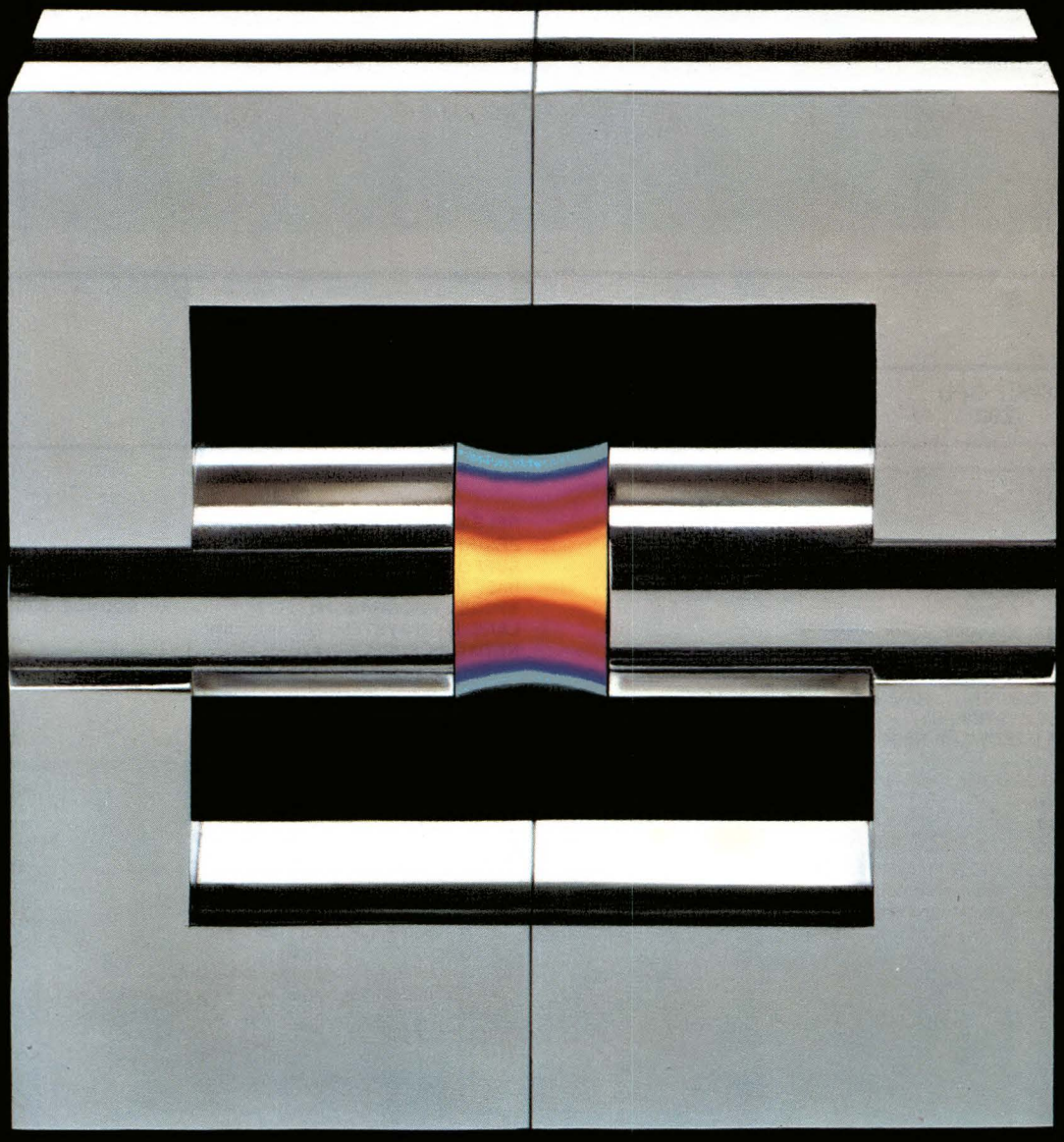

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CIRCLE NO 65

8-BIT CPU
CDP SERIES*

DEVELOPMENT
OPERATING SYSTEM

CDOS

RCA Solid State Div
Rte 202
Somerville, NJ 08876
Phone (201) 685-6599

RELEASE DATE: September 1979
PRICE: $1600
TARGET MODEL: CDP18S007, CDP18S008
SUPPORT LANGUAGES: Macro assembler; BASIC I and II, VIS interpreter; PLM 1800 and BASIC I compilers
SYSGEN PROGRAM: Yes
SOURCE CODE: No
LANGUAGE SYSTEM: Assembly
NETWORK SUPPORT: Yes

SYSTEM RESIDENCY: RAM and disk
ROMABLE SYSTEM: No
MINIMUM HARDWARE NEEDED: 28k bytes RAM and single-density floppy-disk drive

PROCESSOR ALLOCATION/MANAGEMENT
- System vs User mode

PERIPHERAL MANAGEMENT
- Supports CRTs, line printers and floppy-disk drives
- Provides device independence

MEMORY MANAGEMENT
- Single contiguous allocation
- Overlays

FILE MANAGEMENT
- Named file system
- Random organization
- Allocation type: linked list of sectors
- Can access file system from HLL

COMMENTS: *CDP1802, CDP1805 and CDP1806

CIRCLE NO 697

8-BIT CPU
Z80

DEVELOPMENT
OPERATING SYSTEM

FLP80DOS

Mostek Corp
1215 W Crosby Rd
Carrollton, TX 75006
Phone (214) 323-6000

RELEASE DATE: 1979
PRICE: $595
SUPPORT LANGUAGES: Macro Z80 and Macro 3870 assemblers; BASIC interpreter; FORTRAN compiler
SYSGEN PROGRAM: No
SOURCE CODE: Yes
LANGUAGE SYSTEM: Z80 assembler
NETWORK SUPPORT: No

SYSTEM RESIDENCY: RAM and disk
ROMABLE SYSTEM: No
MINIMUM HARDWARE NEEDED: 32k bytes RAM

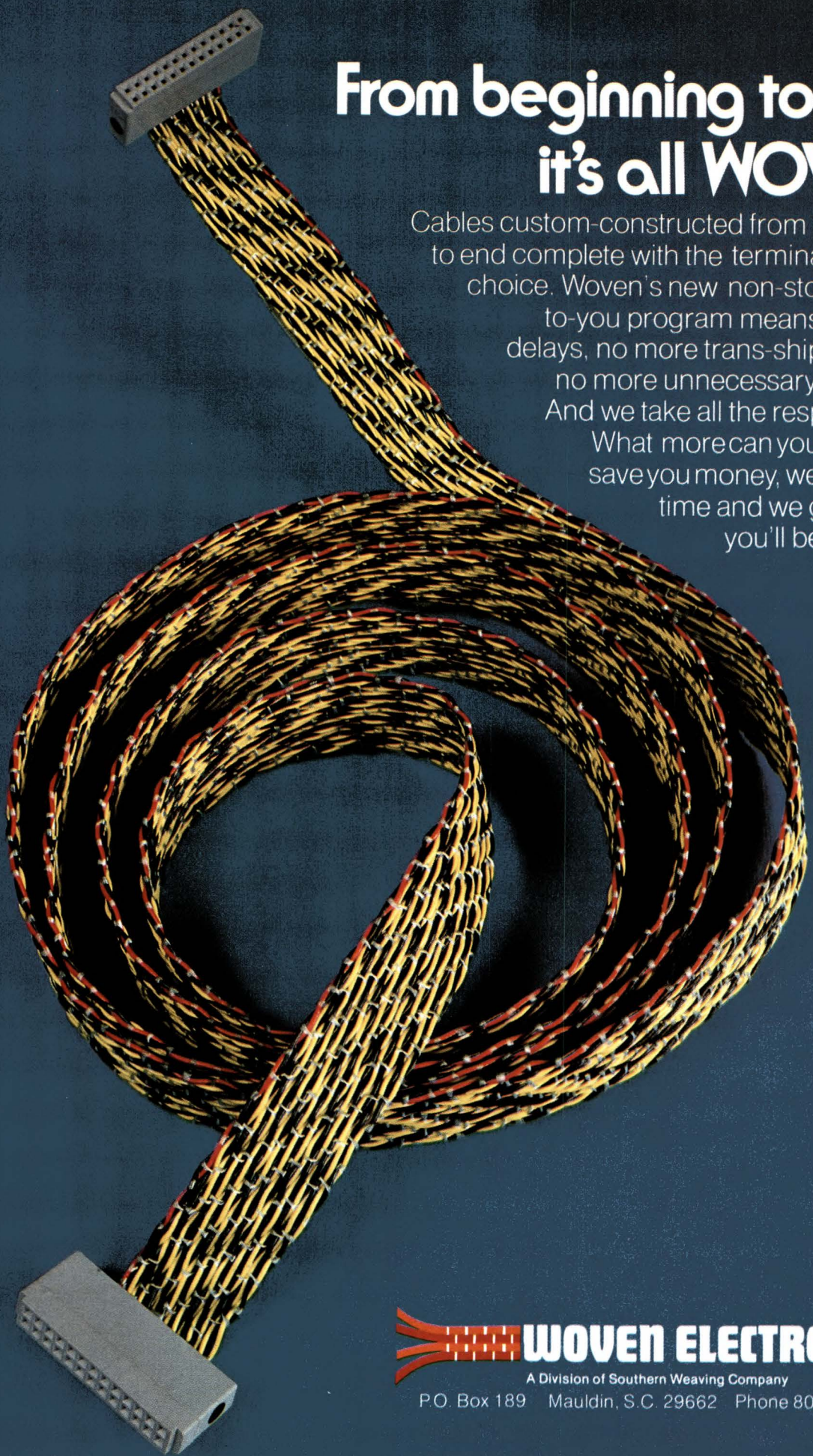
PROCESSOR ALLOCATION/MANAGEMENT
Not Available

PERIPHERAL MANAGEMENT
- Supports CRTs, character and line printers, floppy-disk drives, modems, paper-tape drives and card readers
- Provides device independence and DMA
- Uses interrupts and I/O multibuffering

MEMORY MANAGEMENT
- Single contiguous allocation
- Chaining
- Static relocation
- Binding done during assembly/compilation and linking times

FILE MANAGEMENT
- Named file system
- Sequential organization
- Allocation type: linked list of sectors
- Can access file system from HLL containing constructs

CIRCLE NO 698



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CIRCLE NO 66

EDN μC OPERATING SYSTEMS DIRECTORY

8/16-BIT CPU
8080/8085/8086/8088/8089

DEVELOPMENT
OPERATING SYSTEM

ISIS

Intel Corp
3065 Bowers Ave
Santa Clara, CA 95051
Phone (408) 987-8080

RELEASE DATE: 1977
PRICE: Bundled with hardware
TARGET MODEL: Intellec μC dev systems
SUPPORT LANGUAGES: Related processor assemblers; BASIC interpreter; FORTRAN, PASCAL, COBOL and PL/M compilers
SYSGEN PROGRAM: No **SOURCE CODE:** No
LANGUAGE SYSTEM: PL/M and assembler
NETWORK SUPPORT: Yes

SYSTEM RESIDENCY: RAM and disk
ROMABLE SYSTEM: No
MINIMUM HARDWARE NEEDED: 64k bytes RAM, floppy-disk drive and terminal or printer

PROCESSOR ALLOCATION/MANAGEMENT

- System vs User mode
- Multiprocessing: two processors using Multibus and other semaphore protocols

PERIPHERAL MANAGEMENT

- Supports CRTs, character and line printers, floppy- and cartridge-disk drives, modems, paper-tape drives and Ethernet controller
- Provides device independence, DMA and spooling
- Uses interrupts and I/O multibuffering
- Accommodates a mix of floppy- and hard-disk drives

MEMORY MANAGEMENT

- Single contiguous allocation
- Overlays, swapping and chaining
- Segmentation
- Static relocation
- Binding done after linking time

FILE MANAGEMENT

- Named file system
- Random organization

CIRCLE NO 699

8-BIT CPU
2650/Z80

DEVELOPMENT
OPERATING SYSTEM

TEKDOS

Tektronix Inc
Box 500
Beaverton, OR 97077
Phone (503) 644-0161

RELEASE DATE: April 1977
PRICE: $11,950 with 8002A; $14,300 with 8550
TARGET MODEL: 8002A μP Dev Lab
SUPPORT LANGUAGES: 8080, 8048, 8085, 6800, Z80, 9900, 3870, F8, 6502 and 1802 assemblers; MDL/8080/8085/Z80, MDL/6800, SCI-PLMX, Microsoft and FORTRAN-80 compilers
SYSGEN PROGRAM: No **SOURCE CODE:** No
LANGUAGE SYSTEM: 2650 and Z80 assemblers, PLM
NETWORK SUPPORT: Transfers files to/from host

SYSTEM RESIDENCY: RAM and disk
ROMABLE SYSTEM: No
MINIMUM HARDWARE NEEDED: 32k bytes RAM and 8002A or 8550 Microprocessor Development Lab (MDL)

PROCESSOR ALLOCATION/MANAGEMENT

- System vs User mode
- Multitasking: four system tasks permit intertask communication via monitor synchronizing scheme
- Multiprocessing: three processors (2 system, 1 user) use hardware hold/run synchronizing scheme

PERIPHERAL MANAGEMENT

- Supports CRTs, character and line printers, floppy-disk drives, modems and paper-tape drives
- Provides device independence and DMA
- Uses interrupts

MEMORY MANAGEMENT

- Overlays
- Chaining
- Static relocation
- Binding done during assembly/compilation and linking times

FILE MANAGEMENT

- Named file system
- Sequential and random organizations
- Allocation type: extents
- Can access file system from HLL containing limited constructs

CIRCLE NO 701

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EDN μC OPERATING SYSTEMS DIRECTORY

8/16-BIT CPU
> 30 μP Types*

DEVELOPMENT
OPERATING SYSTEM

UMDS

Boston Systems Office Inc
469 Moody St
Waltham, MA 02154
Phone (617) 894-7800

RELEASE DATE: July 1976
PRICE: $1200 to $3850
TARGET MODEL: Model independent
SUPPORT LANGUAGES: Most assemblers
SYSGEN PROGRAM: Yes
SOURCE CODE: No
LANGUAGE SYSTEM: Assembler, PASCAL
NETWORK SUPPORT: No

SYSTEM RESIDENCY: RAM and disk
ROMABLE SYSTEM: No
MINIMUM HARDWARE NEEDED: 64k bytes RAM and 512k bytes disk

PROCESSOR ALLOCATION/MANAGEMENT

- System vs User mode
- Multiusage: one to 75 users, depending on CPU type, with 64k bytes (min) RAM per user
- Synchronizing scheme: monitor

PERIPHERAL MANAGEMENT

- Supports CRTs, character and line printers, floppy- and cartridge-disk drives, modems and magnetic- and paper-tape drives
- Provides device independence, DMA and spooling
- Uses interrupts and I/O multibuffering
- Accommodates a mix of mass-storage devices, depending on backplane space for controllers

MEMORY MANAGEMENT

- Single contiguous allocation
- Overlays
- Segmentation
- Static relocation
- Binding done during loading time

FILE MANAGEMENT

- Named file system
- Random organization
- Allocation type: linked list of sectors
- Can access file system from HLL
- Password/security protection

COMMENTS: *8048, 8080A, 8085A, 8086, 8088, F8, 6800, 6802, 6805, 6809, Z8000, M68000, 1802, 6502, SC/MP, CDP1802, TMS9900, TMS1000, Z8, Z80, etc

CIRCLE NO 702

8-BIT CPU
8080/8085

REAL-TIME
OPERATING SYSTEM

iRMX 80

Intel Corp
5200 NE Elam Young Parkway
Hillsboro, OR 97123
Phone (503) 640-7147

RELEASE DATE: July 1981 (Version 2.0)
PRICE: $900
TARGET MODEL: All 8080/8085 μP types
SUPPORT LANGUAGES: 8080 and 8085 assemblers; BASIC interpreter; FORTRAN and PL/M compilers
SYSGEN PROGRAM: Yes
SOURCE CODE: Yes
LANGUAGE SYSTEM: PL/M and assembler
NETWORK SUPPORT: No

SYSTEM RESIDENCY: RAM
ROMABLE SYSTEM: Yes
MINIMUM HARDWARE NEEDED: 600 bytes RAM, iSBC 80/10, 80/20-4, 80/24 or 80/30 computer, iSBC 544 communication controller and iSBC 569 digital controller

PROCESSOR ALLOCATION/MANAGEMENT

- Multitasking: unlimited number of tasks can start/stop/suspend other tasks via intertask communication exchanges
- Synchronizing scheme: mailbox
- Multiprocessing: up to 16 processors on Multibus using shared memory with semaphore and interrupt mechanisms via iMMX software

PERIPHERAL MANAGEMENT

- Supports CRTs and floppy- and cartridge-disk drives
- Provides device independence and DMA
- Uses interrupts
- Accommodates a mix of floppy- and hard-disk drives

MEMORY MANAGEMENT

- Single contiguous allocation
- Overlays
- Static relocation

FILE MANAGEMENT

- Named file system
- Sequential and random organizations
- Allocation type: extents
- Can access file system from HLL

CIRCLE NO 708

8-BIT CPU
MC6809

REAL-TIME OPERATING SYSTEM

RMS09

Motorola Semiconductor Products Inc
3102 N 56th St
Phoenix, AZ 85018
Phone (602) 244-5714

RELEASE DATE: 1980
PRICE: $2700
SUPPORT LANGUAGES: Macro assembler; MPL compiler
SYSGEN PROGRAM: Yes **SOURCE CODE:** Request quotation
LANGUAGE SYSTEM: Assembler
NETWORK SUPPORT: No

SYSTEM RESIDENCY: RAM
ROMABLE SYSTEM: Yes
MINIMUM HARDWARE NEEDED: 8k bytes RAM and M68MM19 or M68MM19A Monoboard Microcomputer Module

PROCESSOR ALLOCATION/MANAGEMENT
- Multitasking: 256 tasks can start/stop/suspend other tasks
- Synchronizing scheme: event-wait

PERIPHERAL MANAGEMENT
- Supports CRTs and character printer
- Provides device independence
- Uses interrupts

MEMORY MANAGEMENT
- Single contiguous allocation
- Static relocation
- Binding done during linking time

FILE MANAGEMENT
Not Available

COMMENTS: RMS09 does not support compilation

CIRCLE NO 709

16-BIT CPU
68000

REAL-TIME OPERATING SYSTEM

RMS68K

Motorola Semiconductor Products Inc
3102 N 56th St
Phoenix, AZ 85018
Phone (602) 244-5714

RELEASE DATE: November 1980
PRICE: $5000
TARGET MODEL: Versamodule 01
SUPPORT LANGUAGES: Structured macro assembler; PASCAL compiler
SYSGEN PROGRAM: Yes (requires Exormacs)
SOURCE CODE: Request quotation
LANGUAGE SYSTEM: Assembly
NETWORK SUPPORT: No

SYSTEM RESIDENCY: RAM
ROMABLE SYSTEM: Yes
MINIMUM HARDWARE NEEDED: Versamodule 01

PROCESSOR ALLOCATION/MANAGEMENT
- System vs User mode
- Multitasking: unlimited number of tasks can start/stop/suspend other tasks via intertask communication
- Synchronizing scheme: semaphore

PERIPHERAL MANAGEMENT
- Supports CRTs, character and line printers, floppy- and cartridge-disk drives and modems
- Provides device independence, DMA and spooling
- Uses interrupts
- Accommodates a mix of floppy- and hard-disk drives

MEMORY MANAGEMENT
- Chaining
- Segmentation
- Binding during linking time

FILE MANAGEMENT
Not Available

CIRCLE NO 677

EDN μC OPERATING SYSTEMS DIRECTORY

8-BIT CPU
Z80

REAL-TIME
OPERATING SYSTEM

TMS

Ithaco Inc
735 W Clinton St, Box 818
Ithaca, NY 14850
Phone (607) 272-7640

RELEASE DATE: 1977
PRICE: $4995 (sold only with CompuDAS 1)
TARGET MODEL: CompuDAS 1
SUPPORT LANGUAGES: DABIL (form of BASIC) incremental compiler
SYSGEN PROGRAM: Not required
SOURCE CODE: No
LANGUAGE SYSTEM: Assembly
NETWORK SUPPORT: No

SYSTEM RESIDENCY: EPROM
ROMABLE SYSTEM: Yes
MINIMUM HARDWARE NEEDED: 24k bytes EPROM, 20k bytes RAM and CompuDAS 1

PROCESSOR ALLOCATION/MANAGEMENT
- Multiusage: up to 5 users with 1k bytes (min) RAM per user
- Synchronizing scheme: pipeline

PERIPHERAL MANAGEMENT
- Supports CRTs, character and line printers, magnetic- and cartridge-tape drives and modems
- Provides device independence and DMA
- Uses interrupts and I/O multibuffering
- Accommodates a mix of hard- and floppy-disk drives

MEMORY MANAGEMENT
- Binding done during loading time
- Dynamic workspace relocation

FILE MANAGEMENT
Not Available

CIRCLE NO 678

16-BIT CPU
Z8001, Z8002

REAL-TIME
OPERATING SYSTEM

ZRTS 8000

Zilog Inc
10460 Bubb Rd
Cupertino, CA 95014
Phone (408) 446-4666

RELEASE TIME: June 1981
PRICE: $300 ($3500 unlimited licensing rights)
SUPPORT LANGUAGES: Z8000 PLZ/SYS and C
SYSGEN PROGRAM: Yes
SOURCE CODE: Yes
LANGUAGE SYSTEM: Z8000 PLZ/SYS
NETWORK SUPPORT: No

SYSTEM RESIDENCY: RAM
ROMABLE SYSTEM: Yes
MINIMUM HARDWARE NEEDED: None; most systems will use real-time clock

PROCESSOR ALLOCATION/MANAGEMENT
- System vs User mode
- Multitasking: tasks can start/stop/suspend other tasks via intertask communication
- Synchronizing scheme: semaphore and mailbox

PERIPHERAL MANAGEMENT
- Supports CRTs
- Uses interrupts

MEMORY MANAGEMENT
- Single contiguous allocation
- Segmentation
- Static relocation
- Binding done during loading time

FILE MANAGEMENT
Not Available

CIRCLE NO 679

16-BIT CPU
TMS9900

GENERAL-PURPOSE OPERATING SYSTEM

REAL-TIME OPERATING SYSTEM

Component Software OS

Texas Instruments Inc
Box 1443, MS 6404
Houston, TX 77001
Phone (713) 778-6690

RELEASE DATE: July 1979
PRICE: $1000 per component
SUPPORT LANGUAGES: 9900 assembler; Power BASIC and PASCAL interpreters; Microprocessor PASCAL compiler
SYSGEN PROGRAM: No **SOURCE CODE:** Yes
LANGUAGE SYSTEM: PASCAL: 96%, assembler: 4%
NETWORK SUPPORT: Multidrop synchronous communication using HDLC protocol

SYSTEM RESIDENCY: RAM and disk
ROMABLE SYSTEM: Yes
MINIMUM HARDWARE NEEDED: 6k bytes ROM and 3k bytes RAM

PROCESSOR ALLOCATION/MANAGEMENT

- Multitasking: unlimited number of tasks can start/stop/suspend other tasks via intertask communication
- Synchronizing scheme: semaphore, mailbox and message channels

PERIPHERAL MANAGEMENT

- Supports CRTs, character and line printers, floppy-disk drives and modems
- Provides device independence and DMA
- Uses interrupts and I/O multibuffering
- Accommodates a mix of floppy-disk drives

MEMORY MANAGEMENT

- Segmentation
- Static and dynamic relocations
- Binding done during assembly/compilation, linking and loading times

FILE MANAGEMENT

- Named file system and multilevel directory
- Sequential, contiguous and random organizations
- Allocation type: extents and single contiguous
- Can access file system from HLL containing constructs
- Password/security protection

CIRCLE NO 703

8-BIT CPU
8080/8085

GENERAL-PURPOSE OPERATING SYSTEM

REAL-TIME OPERATING SYSTEM

MFTOS

Ontel Corp
250 Crossways Park Dr
Woodbury, NY 11797
Phone (516) 364-2121

RELEASE DATE: June 1979
PRICE: Depends on configuration
TARGET MODEL: Ontel OP-1
SUPPORT LANGUAGES: 8080 and 8085 assemblers; OPL and BASIC interpreters
SYSGEN PROGRAM: Yes **SOURCE CODE:** No
LANGUAGE SYSTEM: Assembler
NETWORK SUPPORT: Local—16 terminals using standard IOS calls; Remote—VHM, MDOS/VF and HDOS/VF OSs

SYSTEM RESIDENCY: RAM and disk
ROMABLE SYSTEM: No
MINIMUM HARDWARE NEEDED: 32k bytes RAM

PROCESSOR ALLOCATION/MANAGEMENT

- Multitasking: up to 64 tasks can start/stop/suspend other tasks using intertask communication
- Multiusage: up to eight terminals share hard-disk drives; up to 16 terminals share master station; 350 bytes (min) RAM per user
- Synchronizing scheme: semaphore and mailbox

PERIPHERAL MANAGEMENT

- Supports CRTs, line printers, floppy- and cartridge-disk drives, modems and, via subroutines (not OS drivers), magnetic-tape drives
- Provides device independence, DMA and spooling
- Uses interrupts
- Accommodates a mix of hard-disk drives and various floppy-disk-drive capacities and densities

MEMORY MANAGEMENT

- Dynamic relocation
- Binding done during loading time

FILE MANAGEMENT

- Named file system
- Sequential organization
- Random organization and ISAM (OPL only)
- Allocation type: linked list of sectors
- Can access file system from HLL containing constructs

CIRCLE NO 704

8/16-BIT CPU 6800/8080/8086/68000 | GENERAL-PURPOSE OPERATING SYSTEM | REAL-TIME OPERATING SYSTEM

MTOS-68K, -68, -80, -86

Industrial Programming Inc
100 Jericho Quadrangle
Jericho, NY 11753
Phone (516) 938-6600

RELEASE DATE: 1976-1981
PRICE: $3500 to $9500
SUPPORT LANGUAGES: PL/M-80, -86 and FORTRAN-80, -86 compilers; PASCAL86 and PASCAL68K
SYSGEN PROGRAM: No **SOURCE CODE:** Standard
LANGUAGE SYSTEM: Assembly
NETWORK SUPPORT: Up to 255 nodes can send messages to/from mailboxes over fixed routes

SYSTEM RESIDENCY: RAM and ROM
ROMABLE SYSTEM: Yes
MINIMUM HARDWARE NEEDED: 3k to 10k bytes ROM and 1k RAM

PROCESSOR ALLOCATION/MANAGEMENT
- Multitasking: tasks, number-limited only by memory capacity, communicate via mailboxes and priority-order synchronizing scheme
- Multiprocessing: up to 16 processors use Multibus arbitration logic

PERIPHERAL MANAGEMENT
- Supports CRTs, line printers, floppy- and hard-disk drives, modems and communication links
- Provides device independence and DMA
- Uses interrupts and I/O multibuffering
- Accommodates a mix of floppy- and hard-disk drives

MEMORY MANAGEMENT
- Single contiguous allocation

FILE MANAGEMENT
- Named file system
- Compatible with ISIS (MTOS-80 and -86)
- Compatible with VERSADOS (MTOS-68K)

CIRCLE NO 705

8-BIT CPU 6800 | DEVELOPMENT OPERATING SYSTEM | REAL-TIME OPERATING SYSTEM

ODOS

Omnibyte Corp
245 W Roosevelt Rd, Bldg 1-5
West Chicago, IL 60185
Phone (312) 231-6880

RELEASE DATE: 1978
PRICE: $200
TARGET MODEL: OB800, 850
SUPPORT LANGUAGES: Hemenway RA6800ML and Omnibyte resident assemblers; BASIC interpreter; Hemenway Strubal+ compiler
SYSGEN PROGRAM: No **SOURCE CODE:** No
LANGUAGE SYSTEM: Assembly
NETWORK SUPPORT: No

SYSTEM RESIDENCY: RAM and disk
ROMABLE SYSTEM: Yes
MINIMUM HARDWARE NEEDED: 9⅛ bytes RAM, 2k bytes PROM or 25⅛k bytes RAM, 6k bytes PROM (Strubal+ and PROM-resident ODOS); console and floppy-disk drive (5¼ or 8 in.)

PROCESSOR ALLOCATION/MANAGEMENT
Not Available

PERIPHERAL MANAGEMENT
- Supports CRTs, character printers, floppy-disk drives and paper-tape drives
- Accommodates up to four 8-in. or up to three 5¼-in. floppy-disk drives
- Transfers files between 5¼- and 8-in. floppy-disk drives via four disk-resident utility programs

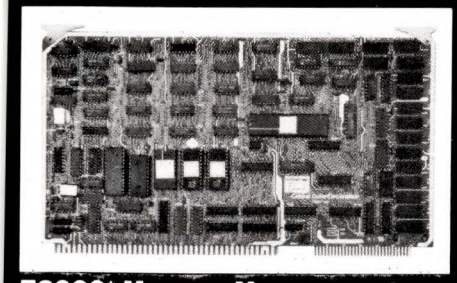
MEMORY MANAGEMENT
- Single contiguous allocation

FILE MANAGEMENT
- Named file system
- Sequential and contiguous organizations
- Allocation type: single contiguous
- Can access file system from HLL containing constructs

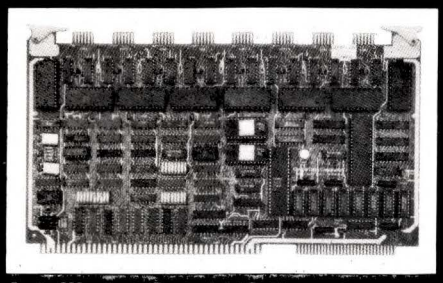
COMMENTS: ODOS is either RAM or PROM resident and has user-accessible routines to open and close files for input or output. PROM version eliminates the need to boot the OS from disk

CIRCLE NO 706

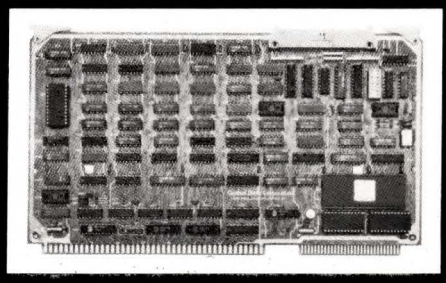
MORE NEW STARS FOR THE MULTIBUS* FROM CENTRAL DATA



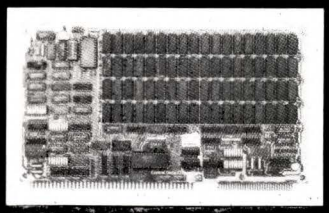
Z8000* Memory Management Processor Board features 4MHz Z8000 running with unique paged/segmented memory management. Includes interrupt controller, interval timers. Can also support PROMs and 9511 APU. Multi-User operating system available. Standard Board $795
Monitor PROMs $90
9511 APU $265



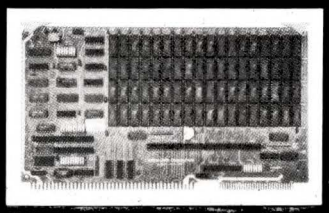
Intelligent Octal I/O Board provides 8: RS-232 ports controlled by on-board 2650 microprocessor. 16K of dual-port RAM allows data transfers with no bus overhead. Includes standard terminal driver program, can hold 4K custom driver program in PROM. $700.



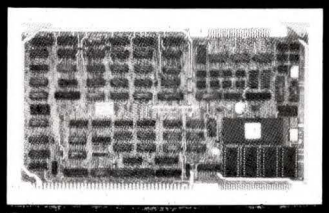
ANSI Winchester Controller fully conforms to the proposed ANSI standard for 8" winchester disk drives. Custom microprogramming available to interface with other disk drive interfaces. Controls up to eight drives. $550.



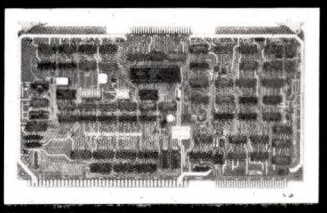
32K-128K Dynamic RAM Board features low power consumption, standard parity checking, and ultra-high reliability.
32K-$530 96K-$1080
64K-$800 128K-$1350



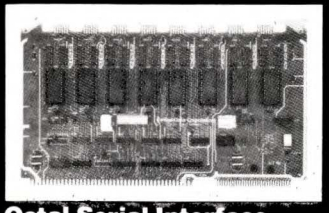
Static Ram Board adds either 16K or 32K of static memory to a Multibus system. 16K—$620
32K—$1100



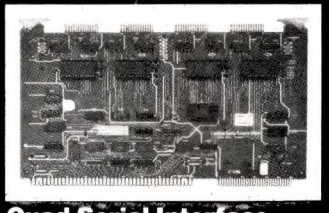
Cartridge Disk Controller Board provides DMA transfers to or from cartridge disk drives with capacities of 10 or 20 Mbytes. $435



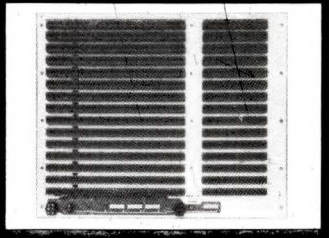
Double Density Floppy Disk Controller adds from one to four double density standard sized floppy disk drives, either single or double-sided. $315



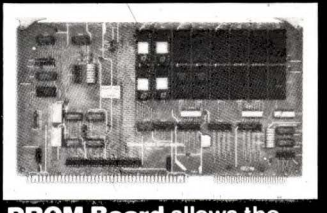
Octal Serial Interface Board allows up to eight EIA RS-232 interfaces. $330



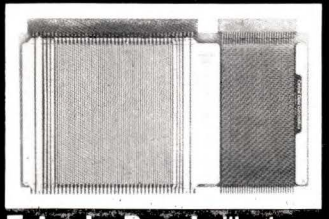
Quad Serial Interface Board hooks up to four EIA RS-232 interfaces to your system. $280



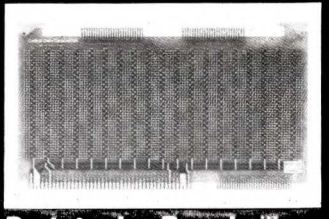
Mother Board can hold up to 15 Multibus cards with both P1 and P2 provided for each card position. $315



PROM Board allows the user to hook between 1K and 128K of PROM to a Multibus system. $140



Extender Board will raise a board being tested up to a height of 6.9 inches. $60



Prototyping Board will accommodate up to 95 16-pin sockets, allowing the user to wire wrap a prototype circuit. $55

*Multibus is a trademark of Intel Corporation
Z8000 is a trademark of Zilog Corporation

Central Data Corporation

P. O. Box 2530 Station A
713 Edgebrook Drive Champaign, IL 61820
(217) 359-8010 TWX 910-245-0787

All prices are OEM quantity 25-99.
Complete price list available on request.

CIRCLE NO 67

A SPECIAL SECTION IN THE OCT. 14, 1981
SILVER ANNIVERSARY ISSUE OF EDN

THE WORLD OF ELECTRONICS IN THE NEXT 25 YEARS

That's the fascinating subject of the 100-page editorial special section in EDN's 25th Anniversary issue.

EDN has asked more than thirty authors, each a leader in the field — as scientist, engineer, entrepreneur, author — to take on the role of visionary. Each has used his own experience as a database to project an acutely personal view of the electronic future. Some of the articles are serious, some lighthearted. Few authors are in agreement and, considering the problems inherent in making predictions even one year in advance in this field, many are likely to arouse considerable controversy.

OUTSTANDING AUTHORS

Isaac Asimov
Ray Bradbury
Alvin Toffler
Author of *Future Shock*
George Gagliardi
Electronic Systems Consultant, Arthur D. Little, Inc.
Manny Fernandez
President and Chief Executive, Zilog, Inc.
Arno A. Penzias
Executive Director, Research, Bell Labs
Jeff Montgomery
President, Gnostic Concepts
Edward Cornish
President, World Future Society
D. Howard Phillips
Director, Electronics Research Lab, The Aerospace Corp.
Robert A. Pease
Staff Scientist, National Semiconductor
Lewis Kornfeld
Director, Tandy Corp./Radio Shack
Jon Roland
Microsystems Consultant
John M. Fluke
Chairman of the Board, CEO, John Fluke Mfg. Co., Inc.
James Healy
Director of Sales & Mktg., GenRad Semiconductor Test, Inc.
Tom Lonergan
President, Wolfdata
Dr. Charles Kao
VP, Director of Engineering, ITT Cannon
Fred A. Blum
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Hal Hellman
Freelance Telecommunications Writer
Dr. Bullis
Chief of Electron Devices, National Bureau of Standards

Plus other outstanding authors and features written by EDN's editors

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16-bit-μP benchmarks—an update with explanations

*A benchmark exercise is **not** your normal performance comparison. It develops a life of its own as faster μPs are introduced and better code is written. With market shares at stake, manufacturers fight fiercely to improve their showings and to make the implementations equivalent.*

Walt Patstone, Editor

When EDN benchmarked the 8086, LSI-11/23, MC68000 and Z8002 (April 1, pgs 179-265), in the issue's accompanying Editorial (pg 39) we proclaimed "no winner in this contest—save you." Nevertheless, ads soon appeared declaring the 68000 the winner.

Reader feedback to the article was heavy and positive. And of course, Motorola was highly pleased with our results. By contrast, Zilog was displeased because we reported the times for its 6-MHz part when it had a 10-MHz version under development. Worse, Intel informed us that we had erred: The data suite used by the 8086 in Benchmark I (Quicksort) differed from that used by the other competitors; thus, the 8086's execution time for that benchmark was overly long by comparison.

Because subsequent investigations revealed additional difficulties with the April 1 article, EDN reopened the benchmark project, soliciting new data from Intel, Motorola and Zilog. The effort—a most interesting one—has produced generally better code, more comparable algorithms and fewer timing inconsistencies, plus strong areas of disagreement over the "proper" interpretation of benchmarks and major differences of opinion over proper coding practices.

During the updating project we also discovered, learned, invented, acquired, relearned or verified beyond a reasonable doubt (take your pick), **The Three Not-So-Golden Rules of Benchmarking:**

- **Rule 1—All's fair in love, war and benchmarks.**
- **Rule 2—Good code is the fastest possible code.**
- **Rule 3—Conditions, cautions, relevant discussion and even actual code never make it to the bottom line when results are summarized.**

It's impossible to get three strong competitors to agree on all aspects of a series of benchmarks. Nevertheless, EDN, Intel, Motorola and Zilog all devoted considerable effort to pointing out and resolving differences or possible errors in the seven tests. Phone calls and Express Mail packages were supplemented with a face-to-face meeting on July 31. One of the most memorable quotes of that meeting (from an IC manufacturer) was, "The history of benchmarks is one of finding ways to cut corners." Anything goes—so long as the required functions are performed and the techniques used aren't specifically forbidden.

In EDN's original benchmark exercise, we kept our guidelines somewhat vague and allowed deviations from the strictest interpretation of the Carnegie-Mellon specifications. Why? Because we wanted the manufacturers to be able to showcase the architectures of their μPs to the best advantage. "Microprocessors aren't minicomputers or mainframes," we reasoned, so we gave the contestants more flexibility than Carnegie-Mellon University did in its 1976 tests. To some extent we now regret this decision for two reasons: Because implementations weren't as comparable in the April 1 article as they could have been, and because we experienced major disagreements over the manner in which the benchmarks were implemented.

Benchmark H (Linked-list insertion) illustrates the latter problem. Intel coded this benchmark with data in a 64k-byte space because it thought this a reasonable implementation. Motorola argued that because the 8086 can address 1M bytes, it should use that larger data space. Intel's position, which EDN allowed, held that "this particular implementation demonstrates how to manipulate data that's contained in a single data segment." Subsequently, Motorola recoded its Benchmark H to also operate in a 64k space, reducing its execution time from 153 μsec (for the 68000's full 16M-byte space) to 121 μsec for a 64k space.

By contrast, in Benchmark I (Quicksort), Intel chose to demonstrate the use of the 8086's data-segmentation

capability to handle large data structures, recognizing that this benchmark's data suite exceeded one segment. However, Intel's code makes each record a segment, taking advantage of the fact that EDN specified records that measure exactly 16 bytes long. Although all three programs require modifications to work with other record lengths, the Intel code may not be optimum for some of those lengths. For example, 17-byte records would be noncontiguous in memory; that is, there would be gaps between each record.

At this point, an important philosophical question arises: Are such code variations in the true spirit of the EDN benchmarks? After all, they do create inequities among the scores, making comparisons somewhat akin to judging peaches and pears. But we couldn't give flexibility to the contestants with one hand, then arbitrarily take it back with the other. **Rule 1** holds. But to minimize confusion or possible misinterpretations, we note the discrepancies in Benchmark I in our data summary.

Go by the book, or go to win?

Rule 2 (Good code is the fastest possible code) should probably have a corollary: "If it works, it's good—by definition." A great many benchmarkers believe in this philosophy, arguing that the benchmark process traditionally implies that you fine tune the code to the maximum extent permitted. At minimum, EDN can attest that this practice makes it extremely difficult to referee benchmark tests.

Here again we have specific examples in mind. First, all of the new code for Benchmark I is optimized to some extent for the data suite that EDN used. Rather than doing comparisons on two records in memory a character at a time, Zilog, Motorola and Intel load the first character into a register, then perform a fast compare. Most of the time this comparison tells the μP whether it should do a sort on this iteration or jump immediately to the next record. This method speeds up execution times for the EDN data, but it might produce slower than optimum times with other data.

Second, also in reference to Benchmark I, Motorola noted that Intel's code makes each record a segment, then quoted from the programming guidelines in *The 8086 Family User's Manual*, 1979 Edition, pg 2-96: "Segment registers should only contain values supplied by the relocation and linkage facilities. Segment-register values may be used to and from memory, pushed onto the stack and popped from the stack. Segment registers should never be used to hold temporary values, nor should they be altered in any other way."

In rebuttal, Intel argued that "The manual states that this method is not a recommended procedure for general usage. However, if you're constructing a base to a segment, this is a perfectly acceptable technique. You do not want to redefine your segment selector to point to somewhere in the middle of your data segment. You don't, ad hoc, change the segment-register value. In our Benchmark I we do define each record as being its own segment. Therefore, we can use a segment selector to point to the base of every record we are using." Intel further explained, "The technique works, and works well. It's represented within our RMX operating system through the concept of a 'Token.' A Token is issued to pass a segment base between tasks and the operating system for access to code or data."

Finally, a disagreement arose over Intel's code for Benchmark A (FIFO interrupt handler), where the memory locations incremented by the interrupt-service routines reside within the code segment. Motorola cried "Foul!" reading from the programming guidelines on pg 2-97 of *The 8086 Family User's Manual* that "...variable data should not be placed in a code segment ...First, programs are simpler to understand if they are uniformly subdivided into segments of code, data and stack. Second, placing data in a code segment can restrict the segment's position independence. This is because, in general, the segment base address of a data item may be changed, but the offset (displacement) of the data item may not. This means that the entire segment must be moved as a unit to avoid changing the offset of the constant data. If the constant data were located in a data segment or an extra segment, individual procedures within the code segment could be moved independently." Motorola then emphasized, "In quality programming, counters are data and belong in data segments; code belongs in code segments."

In turn, Intel replied that the memory locations incremented by the interrupt-service routines are not code and are never executed. It further stated, "This is a simple implementation that is perfectly acceptable for the 8086. There is no reason why we shouldn't be allowed to demonstrate this capability." Intel also noted, "The point of disagreement here concerns the dummy service routine. This routine isn't relevant to the intent of the benchmark, which is to measure interrupt response time."

These three examples make one very important point: When studying benchmarks, beware of the influence of **Rule 2** and its corollary—the benchmark code may be too specialized to be useful in a general application without modification.

A benchmark is much more than just one number

It should be obvious to you by now that the results of even a single benchmark test are likely to contain many important pieces of information besides the execution time. Yet **Rule 3** reflects a basic truism: Whenever suites of benchmarks are run, winners invariably tend to reduce all of the explanations and cautions—not to mention the many lines of code—down to a few simple comparative performance ratios, perhaps even just one number (obtained by some form of averaging). This practice makes no sense to EDN at all. At best, it's

When faster μPs are built...

Zilog heated up the benchmark race considerably when it introduced a 10-MHz version of its Z8002 at Wescon/81. Motorola added fuel to the fire by announcing a 12-MHz 68000.

As the April 1 article pointed out, faster chips decrease execution times. Thus, it's definitely in the best interests of each manufacturer to claim the availability of a "hot" μP. But you can easily see that the fire could be just smoke if the announced product exists only in the form of a promised future mask shrink or in a nearly empty selection bin at the end of a busy production line.

EDN has attempted to verify that both the 10-MHz Z8002 and 12-MHz 68000 are "real." We have obtained data sheets and have asked for—and received—written assurances that sample quantities of both machines are now available on distributors' shelves. Thus, we feel obliged to include in this article the improved benchmark execution times that these two chips deliver **(table).**

BENCHMARK TIMES FOR FASTER μP VERSIONS

BENCHMARK	EXECUTION TIME (μsec) 10-MHz Z8002	12-MHz 68000
A	26	26.7
B	225	268
E	114	187.9
F	74	58
H	122	100.8
I	13,300	14,456
K	338	305

misrepresentative and overly simplified; at worst, it's grossly misleading.

In the April 1 article, we tried to discourage such interpretations by breaking the individual benchmark results into small tables, rather than combining them into one summary table. We scattered these individual results throughout the explanatory text, giving each its own caption and explanatory notes. Nevertheless, reports of our results focused only on execution-time data, ignoring all of our caveats.

Taking the philosophical view that **Rule 3** is unbreakable, we have summarized all of our revised and updated benchmark data in expanded tabular form. This **table** includes columns headed CLOCK SPEED, MEMORY SPACE ADDRESSED and COMMENTS; note this data carefully; we doubt that you will see it repeated elsewhere.

Finally, for those of you who are looking for some rather interesting reading, albeit with a rather dry dialog, we have included all of the code that has changed since the April 1 article. To the best of our knowledge this code is thoroughly debugged; however, time constraints have prevented us from thoroughly checking it. **EDN**

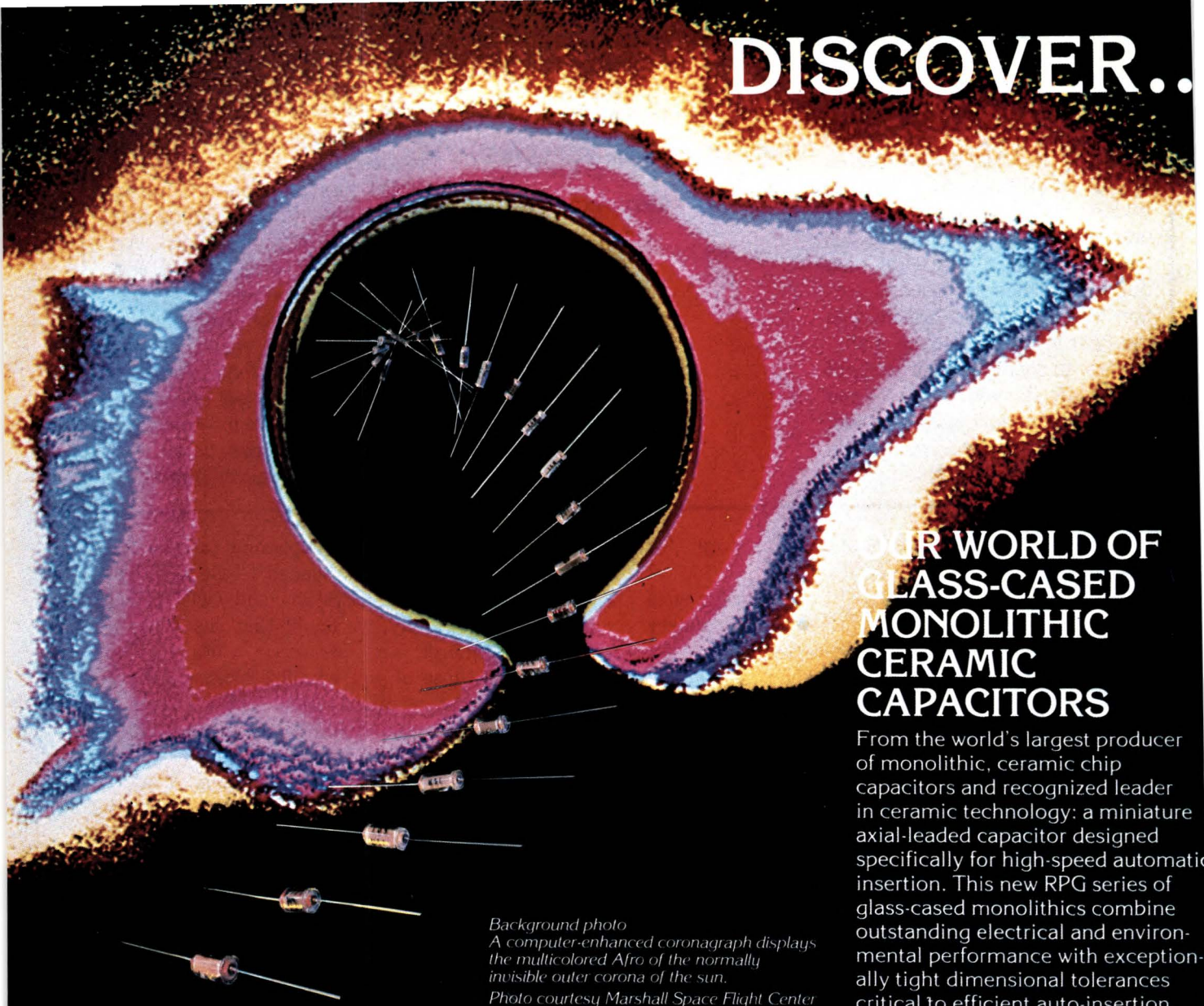
16-BIT μP BENCHMARK UPDATE

BENCHMARK	μP	CLOCK SPEED	CODE BYTES*	MEMORY SPACE ADDRESSED	EXECUTION TIME*	COMMENTS
A I/O INTERRUPT KERNEL	8086	10 MHz	24	1M BYTES	46.4 μsec	PROGRAM MAINTAINS, WITHIN THE 64k BYTES OF CODE, THE MEMORY LOCATIONS TO BE INCREMENTED BY THE INTERRUPT-SERVICE ROUTINES. THIS TECHNIQUE IS NOT RECOMMENDED FOR GENERAL USE.
	68000	10 MHz	24	16M BYTES	32 μsec	
	Z8002	6 MHz	18	64k BYTES	42 μsec	
B I/O KERNEL WITH FIFO PROCESSING	8086	10 MHz	185	1M BYTES	402 μsec	
	68000	10 MHz	130	16M BYTES	321.6 μsec	
	Z8002	6 MHz	124	64k BYTES	375 μsec	
E CHARACTER-STRING SEARCH	8086	10 MHz	44	1M BYTES	211 μsec	
	8086	10 MHz	44	16M BYTES	225.2 μsec	NEW DATA, SO NEW EXECUTION TIME.
	Z8002	6 MHz	66	64k BYTES	190.4 μsec	NEW DATA, SO NEW EXECUTION TIME.
F BIT SET, RESET, TEST	8086	10 MHz	42	1M BYTES	119 μsec	
	68000	10 MHz	36	16M BYTES	69.6 μsec	
	Z8002	6 MHz	44	64k BYTES	124 μsec	
H LINKED-LIST INSERTION	8086	10 MHz	115	64k BYTES	210 μsec	THIS IMPLEMENTATION DEMONSTRATES HOW TO MANIPULATE DATA THAT'S CONTAINED IN A SINGLE 64k SEGMENT.
	68000	10 MHz	100	64k BYTES	121 μsec	THIS BENCHMARK WAS RECODED TO RUN IN 64k, THE FIRST AND LAST 32k OF THE MEMORY SPACE. CODED FOR A 16M-BYTE SPACE, IT TAKES 106 CODE BYTES AND EXECUTES IN 153 μsec.
	Z8002	6 MHz	84	64k BYTES	203 μsec	
I QUICKSORT	8086	10 MHz	276	1M BYTES	38,254 μsec	CODE IS OPTIMIZED FOR 16-BYTE RECORDS ONLY. USES PROGRAM TECHNIQUES NOT RECOMMENDED IN *8086 FAMILY USER'S MANUAL*.
	68000	10 MHz	276	16M BYTES	17,348 μsec	
	Z8002	6 MHz	334	64k BYTES	22,211 μsec	
K BIT-MATRIX TRANSPORTATION	8086	10 MHz	95	1M BYTES	523 μsec	SUBROUTINE WILL FAIL IF THE BIT MATRIX RESIDES ABOVE A BYTE DISPLACEMENT OF 8k IN A DATA SEGMENT.
	68000	10 MHz	74	16M BYTES	366.2 μsec	
	Z8002	6 MHz	106	64k BYTES	563 μsec	

***NOTE:** DATA WAS SUPPLIED BY MANUFACTURERS. EDN SPOT-CHECKED THE EXECUTION TIMES; IT DID *NOT* VERIFY ALL OF THEM AS BEING CORRECT. ADDITIONAL DATA IS CONTAINED IN THE **BOX, "WHEN FASTER μPs ARE BUILT ..."**

Consider *ALL* the relevant data *before naming a victor in EDN's updated benchmark tests. Note in particular the memory space addressed by each machine in each test and the comments relating to some of the code—they could be critically important to your application. Observe also that Zilog benchmarked the Z8002 rather than the segmented Z8001.*

DISCOVER..



Background photo
A computer-enhanced coronagraph displays the multicolored Afro of the normally invisible outer corona of the sun.
Photo courtesy Marshall Space Flight Center

OUR WORLD OF GLASS-CASED MONOLITHIC CERAMIC CAPACITORS

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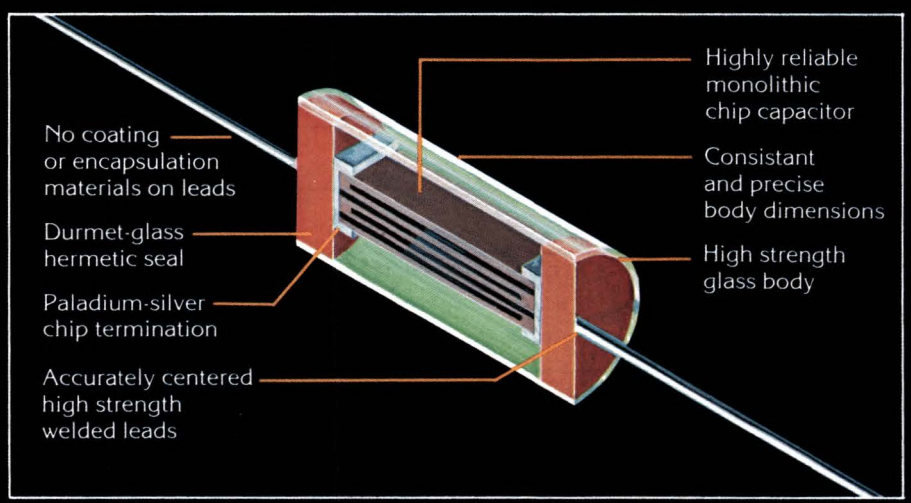

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MURATA ERIE NORTH AMERICA, INC.

CIRCLE NO 70

BENCHMARK A-8086

```
                                1     ;-------------------------------------------------------------------------------
                                2     ;
                                3     ;       EDN MAGAZINE BENCHMARK STUDY
                                4     ;
                                5     ;       BENCHMARK A (I/O INTERRUPT KERNEL, FOUR PRIORITY LEVELS)
                                6     ;
                                7     ;                                                               JULY 8, 1981
                                8     ;
                                9     ;-------------------------------------------------------------------------------
                               10     ;
                               11     ;
                               12     ;       PL/M-86 LINKAGE CONTROL
                               13     ;
                               14     CGROUP  GROUP   CODE
                               15     DGROUP  GROUP   DATA
                               16             ASSUME  CS:CGROUP, DS:DGROUP
                               17     ;
                               18     ;
                               19     ;       DATA SEGMENT DECLARATION
                               20     ;
----                           21     DATA    SEGMENT AT 80H 'DATA'
                               22     ;
0000 0000                      23     TYP0OFF DW      0
0002 0000                      24     TYP0SEG DW      0
                               25     ;
0004 0000                      26     TYP1OFF DW      0
0006 0000                      27     TYP1SEG DW      0
                               28     ;
0008 0000                      29     TYP2OFF DW      0
000A 0000                      30     TYP2SEG DW      0
                               31     ;
000C 0000                      32     TYP3OFF DW      0
000E 0000                      33     TYP3SEG DW      0
                               34     ;
----                           35     DATA    ENDS
                               36     ;
                               37     ;
                               38 +1  $EJECT
                               39     ;
                               40     ;
                               41     ;       CODE SEGMENT DECLARATION
                               42     ;
----                           43     CODE    SEGMENT PUBLIC 'CODE'
                               44     ;
                               45             PUBLIC  BNCHPROG
                               46     ;
0000                           47     BNCHPROG        PROC    NEAR
0000 C706000003E00     R       48             MOV     TYP0OFF,OFFSET(ISR0)  ; INITIALIZE INTERRUPT POINTERS
0006 C7060200----      R       49             MOV     TYP0SEG,CODE
000C C70604004400      R       50             MOV     TYP1OFF,OFFSET(ISR1)
0012 C7060600----      R       51             MOV     TYP1SEG,CODE
0018 C70608004A00      R       52             MOV     TYP2OFF,OFFSET(ISR2)
001E C7060A00----      R       53             MOV     TYP2SEG,CODE
0024 C7060C005000      R       54             MOV     TYP3OFF,OFFSET(ISR3)
002A C7060E00----      R       55             MOV     TYP3SEG,CODE
                               56                                     ;
0030 BAFCFF                    57             MOV     DX,0FFFCH       ; START TIMING COUNTER
0033 B80100                    58             MOV     AX,01H
0036 EF                        59             OUT     DX,AX
                               60                                     ;
0037 CD00                      61             INT     0               ; SIMULATE TYPE 0 INTERRUPT
                               62                                     ;
0039 B80000                    63             MOV     AX,0H           ; STOP TIMING COUNTER
003C EF                        64             OUT     DX,AX
                               65                                     ;
003D C3                        66             RET
                               67     ;
                               68     BNCHPROG        ENDP
                               69     ;
                               70     ;
                               71 +1  $EJECT
                               72     ;       -----   -----   -----   -----   -----   -----   -----   -----
                               73     ;
                               74     ;
                               75     ;       INTERRUPT SERVICE ROUTINES
                               76     ;
                               77     ;
003E 2EFF065600        R       78     ISR0:   INC     CS:COUNT0       ; INCREMENT COUNT FOR INTERRUPT 0
0043 CF                        79             IRET
                               80             ;
0044 2EFF065800        R       81     ISR1:   INC     CS:COUNT1       ; INCREMENT COUNT FOR INTERRUPT 1
0049 CF                        82             IRET
                               83             ;
004A 2EFF065A00        R       84     ISR2:   INC     CS:COUNT2       ; INCREMENT COUNT FOR INTERRUPT 2
004F CF                        85             IRET
                               86             ;
```

BENCHMARK A-8086 (continued)

```
0050 2EFF065C00      R      87      ISR3:   INC     CS:COUNT3       ; INCREMENT COUNT FOR INTERRUPT 3
0055 CF                     88              IRET
                            89              ;
                            90              ;
0056 0000                   91      COUNT0  DW      0               ; COUNT FOR INTERRUPT 0
0058 0000                   92      COUNT1  DW      0               ; COUNT FOR INTERRUPT 1
005A 0000                   93      COUNT2  DW      0               ; COUNT FOR INTERRUPT 2
005C 0000                   94      COUNT3  DW      0               ; COUNT FOR INTERRUPT 3
                            95      ;
----                        96      CODE    ENDS
                            97      ;
                            98      ;
                            99              END
```

BENCHMARK B-8086

```
                              1     ;               BENCHMARK B
                              2     ;
                              3     ;               FOR THE EDN ALGORITHM AND DATA:
                              4     ;               185 BYTES       402.2 MICROSECONDS AT 10MHZ 0 WAITSTATES
                              5     ;
                              6     ;*****************************************************************************
                              7     ;
                              8     ;               THE PERFORMANCE IS FOR INDIVIDUAL INTERRUPTS ON 1,2,3 AND
                              9     ;               4 FOLLOWED BY 3 SUCCESSIVE INTERRUPTS ON 2 FOLLOWED BY FIVE
                             10     ;               SUCCESSIVE LEVEL 3 INTERRUPTS.  THE INDIVIDUAL INTERRUPTS
                             11     ;               ARE INDIVIDUALLY SERVICED AND DO NOT FORCE QUEUING OF
                             12     ;               INTERRUPTS.  THE THREE LEVEL 2 INTERRUPTS CAUSE QUEUING OF
                             13     ;               LEVEL TWO INTERRUPTS.  AFTER ALL LEVEL 2 INTERRUPTS ARE
                             14     ;               SERVICED, THE FIVE LEVEL THREE INTERRUPTS ARE ISSUED TO
                             15     ;               CAUSE QUEING OF THESE INTERRUPTS.  THE SUCCESSIVE LEVEL 2
                             16     ;               AND LEVEL 3 INTERRUPTS ARE ISSUE SEPARATELY SUCH THAT LEVEL
                             17     ;               3 INTERRUPTS ARE NOT QUEUED WITH LEVEL 2 INTERRUPTS.  THIS
                             18     ;               HAS BEEN INTEL'S INTERPRETATION OF THE REQUESTED TEST SUITE.
                             19     ;
                             20     ;*****************************************************************************
                             21     ;
                             22     ;
                             23     ;
                             24     ;       THIS ROUTINE ASSUMES AN 8259A PIC PROGRAMMED IN THE AUTOMATIC END
                             25     ;       OF INTERRUPT MODE WITH INTERRUPTS FOR THE I/O DEVICES PROGRAMMED AT
                             26     ;       32 THROUGH 35 HEX.  THE ROUTINE QUEUES I/O INTERRUPTS IN A 128 WORD
                             27     ;       FIFO AND SERVICES THE INTERRUPTS BY COUNTING THE NUMBER OF
                             28     ;       INTERRUPTS OF EACH TYPE.  EACH I/O HAS ITS OWN 16 BIT COUNT REGISTER.
                             29     ;
                             30     ;
                             31     ;               REGISTER USAGE:         AX = TEMPORARY
                             32     ;                                       BX = FIFO OUT POINTER
                             33     ;                                       DI = DEVICE ID
                             34     ;                                       DS = QUEUE, DATA SEGMENT
                             35     ;
                             36     ;
                             37     ;               THIS IMPLEMENTATION ASSUMES THE COUNTING REGISTERS
                             38     ;               FOR THE DUMMY I/O SERVICE TASKS ARE CONTAINED IN THE
                             39     ;               THE SAME DATA SEGMENT AS THE QUEUE.
                             40     ;
                             41     ;               THE QUEUE AND INTERRUPT SERVICE ROUTINES MAY BE LOCATED
                             42     ;               ANYWHERE IN THE 8086'S 1 MEGABYTE ADDRESS SPACE.
                             43
                             44
                             45     ;       EQUATES
                             46
0000                         47             DEV32_ID        EQU     0H
0002                         48             DEV33_ID        EQU     02H
0004                         49             DEV34_ID        EQU     04H
0006                         50             DEV35_ID        EQU     06H
00FF                         51             ON              EQU     0FFH
                             52
                             53
----                         54     INTR_POINTERS           SEGMENT
0080                         55                     ORG 32*4
                             56
0080 0000----        R       57             TYPE_32         DD      DEV32_INTR
0084 2700----        R       58             TYPE_33         DD      DEV33_INTR
0088 4E00----        R       59             TYPE_34         DD      DEV34_INTR
008C 7500----        R       60             TYPE_35         DD      DEV35_INTR
                             61
----                         62     INTR_POINTERS           ENDS
                             63
                             64
                             65
                             66
```

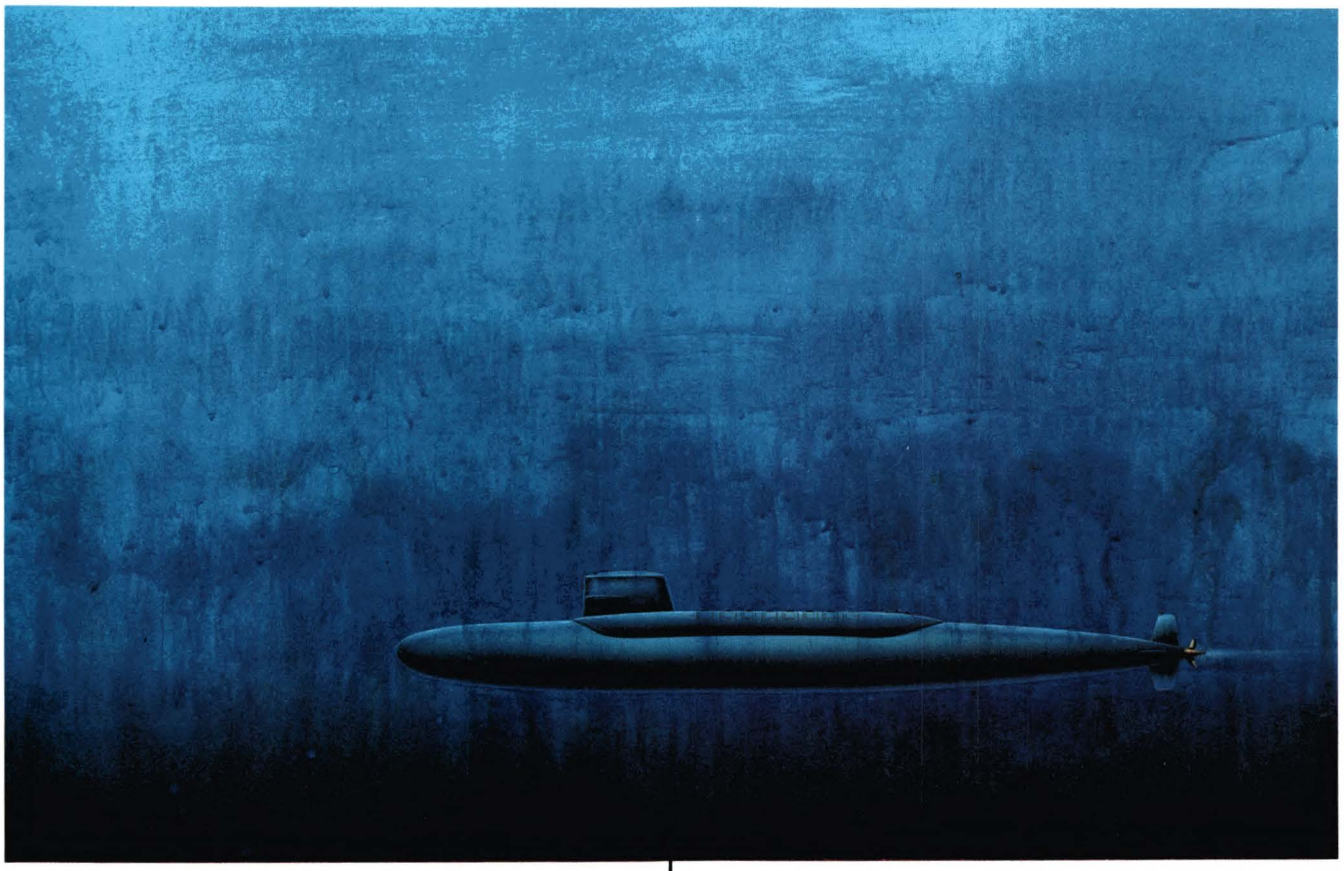
BENCHMARK B-8086 (continued)

```
----                    67      DATA                    SEGMENT WORD    PUBLIC 'DATA'
                        68
0000 (128               69              QUEUE           DW      128 DUP(0) ;I/O FIFO AREA
     0000
     )
0100 (2                 70              RUNFLAG         DB      2 DUP(0)   ;RUNFLAG
     00
     )
0102 ????               71              QUEUE_IN        DW      ?          ;POINTER TO NEXT QUEUE ENTRY
0104 (4                 72              INTR_COUNTERS   DW      4 DUP(0)   ;I/O INTERRUPT COUNTERS
     0000
     )
----                    73      DATA                    ENDS
                        74
                        75
----                    76      CODE            SEGMENT PARA    PUBLIC  'CODE'
                        77              ASSUME CS:CODE,DS:DATA
                        78
                        79
0000                    80              DEV32_INTR      PROC FAR
0000 53                 81                      PUSH    BX                 ;SAVE REGISTERS
0001 50                 82                      PUSH    AX
0002 57                 83                      PUSH    DI
0003 1E                 84                      PUSH    DS
                        85      ;
0004 BF0000             86                      MOV     DI,DEV32_ID        ;LOAD DEVICE ID
                        87      ;
0007 B8----     R       88                      MOV     AX,SEG QUEUE       ;LOAD DATA SEGMENT ADDRESS
000A 8ED8               89                      MOV     DS,AX              ;OF THE FIFO.
                        90      ;
000C A10201     R       91                      MOV     AX,QUEUE_IN        ;GET POINTER TO THE NEXT
000F 8BD8               92                      MOV     BX,AX              ;FIFO ENTRY.
                        93      ;
0011 893F               94                      MOV     [BX],DI            ;PUT I/O ID IN THE FIFO.
0013 0402               95                      ADD     AL,2               ;ADJUST FIFO INPUT POINTER.
0015 A30201     R       96                      MOV     QUEUE_IN,AX        ;SAVE UPDATED QUEUE_IN PNTR.
                        97      ;
0018 B0FF               98                      MOV     AL,ON              ;TEST AND SET THE RUNFLAG
001A 86060001   R       99                      XCHG    AL,RUNFLAG
001E A8FF              100                      TEST    AL,ON
0020 747A              101                      JZ      SERVICE_NEXT       ;GO SERVICE THIS INTERRUPT
                       102                                                 ;IF NO OTHERS IN THE QUEUE.
                       103      ;
0022 1F                104                      POP     DS                 ;RESTORE REGISTERS
0023 5F                105                      POP     DI
0024 58                106                      POP     AX
0025 5B                107                      POP     BX
0026 CF                108                      IRET
                       109              DEV32_INTR      ENDP
                       110
                       111
0027                   112              DEV33_INTR      PROC FAR
0027 53                113                      PUSH    BX                 ;SAVE REGISTERS
0028 50                114                      PUSH    AX
0029 57                115                      PUSH    DI
002A 1E                116                      PUSH    DS
                       117      ;
002B BF0200            118                      MOV     DI,DEV33_ID        ;LOAD DEVICE ID
                       119      ;
002E B8----     R      120                      MOV     AX,SEG QUEUE       ;LOAD DATA SEGMENT ADDRESS
0031 8ED8              121                      MOV     DS,AX              ;OF THE FIFO
                       122      ;
0033 A10201     R      123                      MOV     AX,QUEUE_IN        ;GET POINTER TO THE NEXT
0036 8BD8              124                      MOV     BX,AX              ;FIFO ENTRY.
                       125      ;
0038 893F              126                      MOV     [BX],DI            ;PUT I/O ID IN THE FIFO.
003A 0402              127                      ADD     AL,2               ;ADJUST FIFO INPUT POINTER.
003C A30201     R      128                      MOV     QUEUE_IN,AX        ;SAVE UPDATED QUEUE_IN PNTR.
                       129      ;
003F B0FF              130                      MOV     AL,ON              ;TEST AND SET THE RUNFLAG.
0041 86060001   R      131                      XCHG    AL,RUNFLAG
0045 A8FF              132                      TEST    AL,ON
0047 7453              133                      JZ      SERVICE_NEXT       ;GO SERVICE THIS INTERRUPT
                       134                                                 ;IF NO OTHERS IN THE QUEUE.
                       135      ;
0049 1F                136                      POP     DS                 ;RESTORE REGISTERS
004A 5F                137                      POP     DI
004B 58                138                      POP     AX
004C 5B                139                      POP     BX
004D CF                140                      IRET
                       141              DEV33_INTR      ENDP
                       142
                       143
004E                   144              DEV34_INTR      PROC FAR
004E 53                145                      PUSH    BX                 ;SAVE REGISTERS
004F 50                146                      PUSH    AX
```

BENCHMARK B-8086 (continued)

```
0050 57                          147                     PUSH    DI
0051 1E                          148                     PUSH    DS
                                 149             ;
0052 BF0400                      150                     MOV     DI,DEV34_ID             ;LOAD DEVICE ID
                                 151             ;
0055 B8----              R       152                     MOV     AX,SEG QUEUE            ;LOAD DATA SEGMENT ADDRESS
0058 8ED8                        153                     MOV     DS,AX                   ;OF THE FIFO.
                                 154             ;
005A A10201              R       155                     MOV     AX,QUEUE_IN             ;GET POINTER TO THE NEXT
005D 8BD8                        156                     MOV     BX,AX                   ;FIFO ENTRY.
                                 157             ;
005F 893F                        158                     MOV     [BX],DI                 ;PUT I/O ID IN THE FIFO.
0061 0402                        159                     ADD     AL,2                    ;ADJUST FIFO INPUT POINTER.
0063 A30201              R       160                     MOV     QUEUE_IN,AX             ;SAVE UPDATED QUEUE_IN PNTR.
                                 161             ;
0066 B0FF                        162                     MOV     AL,ON                   ;TEST AND SET THE RUNFLAG.
0068 86060001            R       163                     XCHG    AL,RUNFLAG
006C A8FF                        164                     TEST    AL,ON
006E 742C                        165                     JZ      SERVICE_NEXT            ;GO SERVICE THIS INTERRUPT
                                 166                                                     ;IF NO OTHERS IN THE QUEUE.
                                 167             ;
0070 1F                          168                     POP     DS                      ;RESTORE REGISTERS
0071 5F                          169                     POP     DI
0072 58                          170                     POP     AX
0073 5B                          171                     POP     BX
0074 CF                          172                     IRET
                                 173             DEV34_INTR      ENDP
                                 174
0075                             175             DEV35_INTR      PROC FAR
0075 53                          176                     PUSH    BX                      ;SAVE REGISTERS
0076 50                          177                     PUSH    AX
0077 57                          178                     PUSH    DI
0078 1E                          179                     PUSH    DS
                                 180             ;
0079 BF0600                      181                     MOV     DI,DEV35_ID             ;LOAD DEVICE ID.
                                 182             ;
007C B8----              R       183                     MOV     AX,SEG QUEUE            ;LOAD DATA SEGMENT ADDRESS
007F 8ED8                        184                     MOV     DS,AX                   ;OF THE FIFO.
                                 185             ;
0081 A10201              R       186                     MOV     AX,QUEUE_IN             ;GET POINTER TO THE NEXT
0084 8BD8                        187                     MOV     BX,AX                   ;FIFO ENTRY.
                                 188             ;
0086 893F                        189                     MOV     [BX],DI                 ;PUT I/O ID IN THE FIFO.
0088 0402                        190                     ADD     AL,2                    ;ADJUST FIFO INPUT POINTER.
008A A30201              R       191                     MOV     QUEUE_IN,AX             ;SAVE UPDATED QUEUE_IN PNTR.
                                 192             ;
008D B0FF                        193                     MOV     AL,ON                   ;TEST AND SET THE RUNFLAG.
008F 86060001            R       194                     XCHG    AL,RUNFLAG
0093 A8FF                        195                     TEST    AL,ON
0095 7405                        196                     JZ      SERVICE_NEXT            ;GO SERVICE THIS INTERRUPT
                                 197                                                     ;IF NO OTHERS IN THE QUEUE.
                                 198             ;
0097 1F                          199                     POP     DS                      ;RESTORE REGISTERS
0098 5F                          200                     POP     DI
0099 58                          201                     POP     AX
009A 5B                          202                     POP     BX
009B CF                          203                     IRET
                                 204             DEV35_INTR      ENDP
                                 205
                                 206
                                 207
                                 208
009C                             209             SERVICE_NEXT    PROC NEAR
                                 210             ;
009C                             211             CONTINUE_SERVICING:
009C 8B3F                        212                     MOV     DI,[BX]                 ;GET I/O ID
009E FB                          213                     STI                             ;ENABLE INTERRUPTS
                                 214
                                 215
                                 216
009F                             217             DUMMY_IO_SERVICING:
009F FF850401            R       218                     INC     INTR_COUNTERS[DI]
                                 219
00A3                             220             RETURN_FROM_IO_SERVICING:
00A3 FA                          221                     CLI                             ;DISABLE INTERRUPTS
00A4 80C302                      222                     ADD     BL,2                    ;DELETE THIS I/O REQUEST
00A7 3B1E0201            R       223                     CMP     BX,QUEUE_IN             ;TEST IF DONE
00AB 75EF                        224                     JNE     CONTINUE_SERVICING      ;GO BACK IF MORE I/O REQUESTS
                                 225
                                 226
00AD 33C0                        227                     XOR     AX,AX                   ;NO MORE I/O REQUESTS, RESET
00AF A20001              R       228                     MOV     RUNFLAG,AL              ;RUNFLAG.
                                 229
00B2 1F                          230                     POP     DS
00B3 5F                          231                     POP     DI                      ;RESTORE MACHINE STATE
00B4 58                          232                     POP     AX
```

When reliability is imperative.



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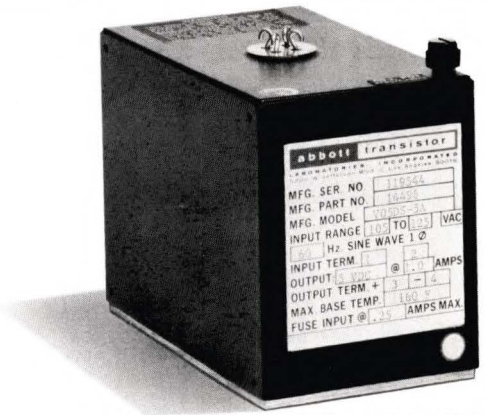

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MILITARY POWER SUPPLIES

CIRCLE NO 71

BENCHMARK B-8086 (continued)

```
00B5 5B                 233                     POP     BX
00B6 CF                 234                     IRET                    ;RETURN TO INTERRUPTED PROGRAM
                        235
                        236             SERVICE_NEXT    ENDP
                        237
                        238
----                    239     CODE            ENDS
                        240
                        241                     END
```

BENCHMARK B-MC68000

```
                                        OPT     BRS,FRS
                                *
                                *               MC68000  EDN BENCHMARK B
                                *
                                *     FIFO I/O INTERRUPT HANDLER, FOUR INTERRUPT LEVELS
                                *
                                *     NOTES: 1) FOUR INTERRUPT VECTORS ARE ASSUMED TO
                                *               POINT TO THE INTERRUPT ENTRY POINTS.
                                *            2) THE MC68000 INTERRUPT SEQUENCE TAKES 44
                                *               CYCLES WITH AN ASSUMED INTERRUPT
                                *               ACKNOWLEDGE BUS CYCLE OF 4 CYCLES.
                                *            3) INTERRUPTS ARE TAKEN FROM ANYWHERE IN
                                *               THE MC68000 16 MEGABYTE ADDRESS SPACE.
                                *
                                *                       LINES:  44
                                *                       BYTES: 130
                                *
                                *       MC68000L10 BENCHMARK TIME:  268.800 MICROSECONDS
                                *       MC68000L12 BENCHMARK TIME:  224.000 MICROSECONDS
                                *
                                *
                                *     REGISTER USE:  A0 - ADDRESS POINTER
                                *
                                *        INTERRUPT HANDLERS
 0 00000000 2F08        INTRPT1 MOVE.L  A0,-(SP)        SAVE WORK REGISTER
 0 00000002 3078008A            MOVE    QUEUEIN,A0      FIND NEXT ENTRY IN QUEUE
 0 00000006 30BC0082            MOVE    #COUNTER1,(A0)  PLACE COUNTER ADDRESS IN
 0 0000000A 5438008B            ADD.B   #2,QUEUEIN+1    UPDATE TO NEXT QUEUE ENTRY
 0 0000000E 4AF8028C            TAS     FLAG            TEST FOR NESTED INTERRUPT
 0 00000012 6A4C                BPL     PROCESS         BRANCH IF NOT TO PROCESS
 0 00000014 205F                MOVE.L  (SP)+,A0        RESTORE REGISTER
 0 00000016 4E73                RTE                     RETURN FROM INTERRUPTS

 0 00000018 2F08        INTRPT2 MOVE.L  A0,-(SP)        SAVE WORK REGISTER
 0 0000001A 3078008A            MOVE    QUEUEIN,A0      FIND NEXT ENTRY IN QUEUE
 0 0000001E 30BC0084            MOVE    #COUNTER2,(A0)  PLACE COUNTER ADDRESS IN
 0 00000022 5478008B            ADD     #2,QUEUEIN+1    UPDATE TO NEXT QUEUE ENTRY
 0 00000026 4AF8028C            TAS     FLAG            TEST FOR NESTED INTERRUPT
 0 0000002A 6A34                BPL     PROCESS         BRANCH IF NOT TO PROCESS
 0 0000002C 205F                MOVE.L  (SP)+,A0        RESTORE REGISTER
 0 0000002E 4E73                RTE                     RETURN FROM INTERRUPTS

 0 00000030 2F08        INTRPT3 MOVE.L  A0,-(SP)        SAVE WORK REGISTER
 0 00000032 3078008A            MOVE    QUEUEIN,A0      FIND NEXT ENTRY IN QUEUE
 0 00000036 30BC0086            MOVE    #COUNTER3,(A0)  PLACE COUNTER ADDRESS IN
 0 0000003A 5478008B            ADD     #2,QUEUEIN+1    UPDATE TO NEXT QUEUE ENTRY
 0 0000003E 4AF8028C            TAS     FLAG            TEST FOR NESTED INTERRUPT
 0 00000042 6A1C                BPL     PROCESS         BRANCH IF NOT TO PROCESS
 0 00000044 205F                MOVE.L  (SP)+,A0        RESTORE REGISTER
 0 00000046 4E73                RTE                     RETURN FROM INTERRUPTS

 0 00000048 2F08        INTRPT4 MOVE.L  A0,-(SP)        SAVE WORK REGISTER
 0 0000004A 3078008A            MOVE    QUEUEIN,A0      FIND NEXT ENTRY IN QUEUE
 0 0000004E 30BC0088            MOVE    #COUNTER4,(A0)  PLACE COUNTER ADDRESS IN
 0 00000052 5478008B            ADD     #2,QUEUEIN+1    UPDATE TO NEXT QUEUE ENTRY
 0 00000056 4AF8028C            TAS     FLAG            TEST FOR NESTED INTERRUPT
 0 0000005A 6A04                BPL     PROCESS         BRANCH IF NOT TO PROCESS
 0 0000005C 205F                MOVE.L  (SP)+,A0        RESTORE REGISTER
 0 0000005E 4E73                RTE                     RETURN FROM INTERRUPTS

                        * PROCESS NEXT INTERRUPT
 0 00000060 3F08        PROCESS MOVE    A0,-(SP)        SAVE QUEUE LOCATION ON STACK
 0 00000062 46FC2000            MOVE    #$2000,SR       ENABLE INTERRUPTS

                        * SIMULATE DEVICE HANDLER
 0 00000066 3050                MOVE    (A0),A0         LOAD COUNTER'S ADDRESS
 0 00000068 5250                ADD     #1,(A0)         INCREMENT IT BY ONE

                        * FINISH INTERRUPT PROCESSING
 0 0000006A 46FC2700            MOVE    #$2700,SR       DISABLE INTERRUPTS
 0 0000006E 542F0001            ADD.B   #2,1(SP)        GO TO NEXT ENTRY IN THE QUEUE
 0 00000072 305F                MOVE    (SP)+,A0        LOAD ITS ADDRESS
```

BENCHMARK B-MC68000 (continued)

```
78 0 00000074 B0F8008A              CMP       QUEUEIN,A0          TEST END OF LIST
79 0 00000078 66E6                  BNE       PROCESS             PROCESS IT IF NOT
80 0 0000007A 4238028C              CLR.B     FLAG                SHOW NO ELEMENTS QUEUED
81 0 0000007E 205F                  MOVE.L    (SP)+,A0            RESTORE WORK REGISTER
82 0 00000080 4E73                  RTE                           RETURN FROM INTERRUPT
83
84                          * INTERRUPT COUNTERS
85 0 00000082 0000          COUNTER1 DC       0                   INTERRUPT COUNTER ONE
86 0 00000084 0000          COUNTER2 DC       0                   INTERRUPT COUNTER TWO
87 0 00000086 0000          COUNTER3 DC       0                   INTERRUPT COUNTER THREE
88 0 00000088 0000          COUNTER4 DC       0                   INTERRUPT COUNTER FOUR
89
90                          * QUEUE POINTER
91 0 0000008A 008C          QUEUEIN  DC       QUEUE               NEXT ENTRY TO USE
92
93                          * QUEUE PROPER
94 0 0000008C 00000000      QUEUE    DCB      256,0               DEFINE THE QUEUE
95
96                          * INTERRUPT IN PROGRESS FLAG
97 0 0000028C 00            FLAG     DC.B     0                   INTERRUPT IN PROGRESS INDICATOR
98
99                                   END
```

BENCHMARK B-Z8002

```
                    !Example B: I/O Interrupt Kernel, FIFO Processing!
                    $rel 0
                    !In this benchmark, the four devices each have unique
                     vectors for interrupts. The order of the devices on the
                     diasy chain is irrelevant, as the priority processing is
                     done in the FIFO processing routine.
                    !

                    INTRPT1:
0000 93F1                   PUSH @SP,ADRPT          !Save working register !
0002 6101                   LD ADRPT,QUEIN          !Address of next entry !
0004 0012'
0006 0D15                   LD @ADRPT,#COUNTER1     !Counter adr on queue  !
0008 0008'
000A 6801                   INCB QUEIN+1,#2         !Update QUEIN to next entry !
000C 0013'
000E 4C05                   TSETB FLAG              !Test if nested interrupt !
0010 0010'
0012 ED26                   JR PL,PROCESS           !No, process current one  !
0014 97F1                   POP ADRPT,@SP           !Restore working register !
0016 7B00                   IRET                    !Return from interrupt    !
                    INTRPT2:
0018 93F1                   PUSH @SP,ADRPT          !Save working register !
001A 6101                   LD ADRPT,QUEIN          !Address of next entry !
001C 0012'
001E 0D15                   LD @ADRPT,#COUNTER2     !Counter adr on queue  !
0020 000A'
0022 6801                   INCB QUEIN+1,#2         !Update QUEIN to next entry !
0024 0013'
0026 4C06                   TSETB FLAG              !Test if nested interrupt !
0028 0010'
002A ED1A                   JR PL,PROCESS           !No, process current one  !
002C 97F1                   POP ADRPT,@SP           !Restore working register !
002E 7B00                   IRET                    !Return from interrupt    !
                    INTRPT3:
0030 93F1                   PUSH @SP,ADRPT          !Save working register !
0032 6101                   LD ADRPT,QUEIN          !Address of next entry !
0034 0012'
0036 0D15                   LD @ADRPT,#COUNTER3     !Counter adr on queue  !
0038 000C'
003A 6801                   INCB QUEIN+1,#2         !Update QUEIN to next entry !
003C 0013'
003E 4C05                   TSETB FLAG              !Test if nested interrupt !
0040 0010'
0042 ED0E                   JR PL,PROCESS           !No, process current one  !
0044 97F1                   POP ADRPT,@SP           !Restore working register !
0046 7B00                   IRET                    !Return from interrupt    !
                    INTRPT4:
0048 93F1                   PUSH @SP,ADRPT          !Save working register !
004A 6101                   LD ADRPT,QUEIN          !Address of next entry !
004C 0012'
004E 0D15                   LD @ADRPT,#COUNTER4     !Counter adr on queue  !
0050 000E'
0052 6801                   INCB QUEIN+1,#2         !Update QUEIN to next entry !
0054 0013'
0056 4C05                   TSETB FLAG              !Test if nested interrupt !
0058 0010'
005A ED02                   JR PL,PROCESS           !No, process current one  !
```

BENCHMARK B-Z8002 (continued)

```
005C 97F1               POP ADRPT,@SP           !Restore working register !
005E 7B00               IRET                    !Return from interrupt    !

                    PROCESS:
0060 93F1               PUSH @SP,ADRPT          !Save queue location !
0062 7C05               EI VI                   !Enable interrupts   !
0064 2111               LD ADRPT,@ADRPT         !Get counter's adr from queue !
0066 2910               INC @ADRPT              !Increment counter !
0068 7C01               DI VI                   !Disable interrupts !
006A 97F1               POP ADRPT,@SP           !Restore last saved ADRPT !
006C A891               INCB ADRPTL,#2          !De-queue entry !
006E 4B01               CP ADRPT,QUEIN          !End of queue?  !
0070 0012'
0072 EEF6               JR NE,PROCESS           !No, keep processing !
0074 4C08               CLRB FLAG               !Yes, show no elements queued !
0076 0010'
0078 97F1               POP ADRPT,@SP           !Restore working register !
007A 7B00               IRET                    !Return from interrupt    !

007C                end KERNEL
```

BENCHMARK E-8086

```
                                1     NAME SEARCH
                                2
                                3     DGROUP  GROUP   DATA
----                            4     DATA    SEGMENT PUBLIC  'DATA'
                                5
0000 30303030303030             6     TABLE_START     DB      '00000000000000000000000000000000'
     30303030303030
     30303030303030
     30303030303030
     3030
001E 30303030303030             7     S1              DB      '00000000000000000000000000000000'
     30303030303030
     30303030303030
     30303030303030
     3030
003C 48455245303030             8     S2              DB      'HERE0000000000000000000000000000'
     30303030303030
     30303030303030
     30303030303030
     3030
005A 48455245204953             9     S3              DB      'HERE IS A MATCH0000000000000000'
     2041204D415443
     48303030303030
     30303030303030
     3030
0078 00                        10     TABLE_END       DB      0
                               11
0079 48455245204953            12     STRING_START    DB      'HERE IS A MATCH'
     2041204D415443
     48
0088 00                        13     STRING_END      DB      0
                               14
                               15     ; THE DATA TABLE IS 120 CHARACTERS IN LENGTH.  A PARTIAL MATCH
                               16     ; IS FOUND IN POSITION 60.  THE ACTUAL MATCH IS IN POSITION 90.
                               17
                               18
----                           19     DATA    ENDS
                               20
                               21     CGROUP  GROUP   CODE
                               22             ASSUME  CS:CGROUP, DS:DGROUP, ES:DGROUP, SS:DGROUP
                               23     PUBLIC  BNCHPROG
----                           24     CODE    SEGMENT PUBLIC  'CODE'
                               25
0000                           26     BNCHPROG        PROC
                               27     ;SETUP POINTERS FOR SEARCH
                               28
0000 B8----          R         29             MOV     AX,SEG TABLE_START      ;ES:DI IS TABLE PTR
0003 8EC0                      30             MOV     ES,AX
0005 BF0000          R         31             MOV     DI,OFFSET TABLE_START
                               32
0008 B97800          R         33             MOV     CX,OFFSET TABLE_END
                               34                                     ;GET START ADDRESS OF SEARCH
                               35                                      TABLE
000B 81E90000        R         36             SUB     CX,OFFSET TABLE_START
                               37                                     ;CX IS TABLE LENGTH
                               38
000F 8ED8                      39             MOV     DS,AX           ;DS:SI IS STR_PTR
0011 BE7900          R         40             MOV     SI,OFFSET STRING_START
                               41
```

BENCHMARK E-8086 (continued)

```
0014 BB8800     R       42              MOV     BX,OFFSET STRING_END
                        43                                      ;LOAD END OF CHARACTER BUFFER
0017 81EB7900   R       44              SUB     BX,OFFSET STRING_START
                        45                                      ;BX IS STR_LNGTH
                        46
                        47      ;START THE CLOCK
                        48
001B BAFCFF             49              MOV     DX,0FFFCH       ;INITIALIZE PORT ADDRESS
001E B80100             50              MOV     AX,1            ;CONTROL WORD TO START COUNTER
0021 EF                 51              OUT     DX,AX           ;START COUNTER
                        52
                        53      ;  THE BENCHMARK PROCEDURE
                        54
                        55
                        56      ;               EDN BENCHMARK FOR IAPX 86
                        57      ;               CHARACTER SEARCH
                        58      ;
                        59      ;
                        60      ;       ASSUMPTIONS:  1 VALID DATA FOR SRCHLNGTH
                        61      ;                       AND MINLNGTH (SRCHLNGTH>MINLNGTH)
                        62      ;                     2 PARAMETERS ARE PASSED IN REGISTERS AS FOLLOWS:
                        63      ;                               ES:DI   TABLE_PTR
                        64      ;                               DS:SI   STR_PTR
                        65      ;                               CX      TABLE_LNGTH
                        66      ;                               BX      STR_LNGTH
                        67      ;                     3 THE LOCATION OF THE STRING IS RETURNED IN DI
                        68      ;                     4 WORKING REGISTERS (AX & DX) ARE PUSHED
                        69                              AND POPPED
                        70      ;
                        71      ;
                        72
                        73      ;SAVE WORK REGISTERS
0022 50                 74              PUSH    AX
0023 52                 75              PUSH    DX
0024 51                 76              PUSH    CX              ;SAVE LENGTH
0025 FC                 77              CLD
0026 8A04               78              MOV     AL,[SI]         ;LOAD FIRST CHAR
0028 2BCB               79              SUB     CX,BX           ;LENGTH DIFFERENCE
002A 41                 80              INC     CX              ;POSSIBLE SEARCH COUNT
                        81      ;FIND MATCH TO FIRST CHARACTER
                        82
002B                    83      TRYNXT:
002B F2                 84        REPNE SCASB                   ;SCAN WHILE NOT EQUAL
002C AE
002D 7406               85              JE      MATCH1          ;JUMP ON MATCH
002F BFFFFF             86      NOTFND: MOV     DI,-1           ;SET NOT FOUND FLAG
0032 EB1790             87              JMP     DONE            ;EXIT
                        88
                        89      ;FIRST CHARACTER MATCH HAS BEEN FOUND
                        90      ;COMPARE THE REST OF THE STRING
                        91
0035 8BD1               92      MATCH1: MOV     DX,CX           ;SAVE POSSIBLE SEARCH COUNT
0037 57                 93              PUSH    DI              ;SAVE PLACE IN TABLE
0038 8BCB               94              MOV     CX,BX           ;LOAD STR_LNGTH
003A 56                 95              PUSH    SI              ;SAVE STR_PTR
003B 4F                 96              DEC     DI              ;RETEST FIRST (IN CASE LEN=1)
003C F3                 97         REPE CMPSB                   ;COMPARE STRING
003D A6
                        98
                        99      ;DROP THROUGH IF THE STRING DOES NOT MATCH OR WHEN
                       100      ;  CX=0 (THE ENTIRE STRING MATCHES)
                       101
003E 5E                102              POP     SI              ;RESTORE STR_PTR
003F 5F                103              POP     DI              ;RESTORE PLACE IN TABLE
0040 8BCA              104              MOV     CX,DX           ;RESTORE POSSIBLE SEARCH COUNT
0042 7404              105              JE      FOUND           ;STRING MATCHES
0044 E3E9              106              JCXZ    NOTFND          ;END OF STRING, NO MATCH
0046 EBE3              107              JMP     TRYNXT          ;TRY NEXT BYTE IN TABLE
                       108
0048 5F                109      FOUND:  POP     DI              ;GET TABLE_LENGTH
0049 2BFA              110              SUB     DI,DX           ;COMPUTE PTR TO STR IN TABLE
                       111
                       112      ;RESTORE REGISTERS
                       113
004B 5A                114      DONE:   POP     DX
004C 58                115              POP     AX
                       116
004D C3                117              RET                     ;RETURN TO CALLING ROUTINE
                       118      BNCHPROG ENDP
                       119
----                   120      CODE    ENDS
                       121
                       122              END
```

BENCHMARK F-8086

```
                        1       ;       CARNEGIE-MELLON BENCHMARK SERIES [F]
                        2       ;
                        3       ;       BIT TEST, SET, OR RESET FOR 8086
                        4       ;
                        5       SEGA    SEGMENT
----                    6               ASSUME CS:SEGA,DS:SEGA,ES:SEGA,SS:SEGA
                        7       ;
                        8       ;       THREE PARAMETERS ARE PASSED TO THE ROUTINE IN THE FOLLOWING REGISTERS:
                        9       ;
                       10       ;       A1=POINTER TO BIT STRING                IN REG. BX
                       11       ;       N=NUMBER OF ADDRESSED BIT (0<=N<=1000)  IN REG. CX
                       12       ;       F=FUNCTION CODE (1=TEST,2=SET,3=RESET)  IN REG. DX
                       13       ;
                       14       ;       IT IS ASSUMED THAT THE BIT ARRAY IS LOCATED WITHIN THE CURRENT DS REG.
                       15       ;       THE ORIGINAL BIT STATE (0 OR 1) IS RETURNED IN REG. AX
                       16       ;
                       17       BENCHF  PROC
0000                   18               PUSH    SI              ;WILL BE USED FOR ARRAY ACCESSING
0000 56                19       ;       PUSH    CX              ;IF BIT NUMBER MUST BE RETURNED UNALTERED
                       20       ;       PUSH    DX              ;IF FUNCTION CODE MUST BE RETURNED UNALTERED
                       21               MOV     AX,CX           ;LOAD BIT ADDRESS FOR FIELD SEPARATION
0001 8BC1              22               SAR     AX,1            ;SHIFT RIGHT ONE BIT WITH ZERO FILL
0003 D1F8              23               SAR     AX,1
0005 D1F8              24               SAR     AX,1
0007 D1F8              25               MOV     SI,AX           ;STORE ENCOMPASSING BYTE ADDRESS IN INDEX REG.
0009 8BF0              26               AND     CL,00000111B    ;MASK BIT POSITION WITHIN BYTE FIELD
000B 80E107            27               MOV     AL,[BX][SI]     ;ACCESS SI'TH ELEMENT OF ARRAY BX (BIT STRING)
000E 8A00              28               ROR     AL,CL           ;ROTATE LOW BYTE CIRCULARLY BY (CL) BITS
0010 D2C8              29       ;
                       30       ;       BIT TO BE TESTED/ALTERED NOW IN LSB OF REGISTER AL
                       31       ;
                       32               DEC     DX              ;REDUCE FUNCTION CODE TO 0 (=SET) OR 1 (=RESET)
0012 4A                33               DEC     DX
0013 4A                34               CMP     DX,1            ;CHECK BOUNDS OF ARGUMENT (NO ACTION IF >1)
0014 83FA01            35               JA      NOCHANGE
0017 770C              36               MOV     AH,AL           ;SAVE BIT PATTERN FOR LATER USE AS RETURN CODE
0019 8AE0              37               OR      AL,1            ;FORCE ADDRESSED BIT (STILL IN AL) SET
001B 0C01              38               XOR     AL,DL           ;COMPLEMENT BIT TO 0 IF FUNCTION CODE = RESET
001D 32C2              39               ROL     AL,CL           ;REALIGN ORIGINAL DATA BYTE WITH MODIFIED BIT
001F D2C0              40               MOV     [BX][SI],AL     ;REPLACE MODIFIED BYTE IN BIT ARRAY
0021 8800              41               MOV     AL,AH           ;RESTORE ADDRESSED BIT TO LSB OR AL
0023 8AC4              42       NOCHANGE:
0025                   43               AND     AX,0001H        ;MASK IRRELEVENT BITS SO RETURN CODE = 0 OR 1
0025 250100            44       ;       POP     DX              ;RESTORE FUNCTION CODE IF REQUIRED
                       45       ;       POP     CX              ;RESTORE ACCESSED BIT ADDRESS IF REQUIRED
                       46               POP     SI              ;RESTORE REGISTER USED FOR ARRAY ELEMENT ACCESS
0028 5E                47               RET
0029 C3                48       ;
                       49       BENCHF  ENDP
                       50       ;
                       53       ;
                       54       ;       TEST SEQUENCE FOR ABOVE ROUTINE:
                       55       ;
002A BB7F0090          56               MOV     BX,OFFSET T_ARRAY
002E B90A00            57               MOV     CX,10           ;BIT NUMBER = 10
0031 BA0100            58               MOV     DX,1            ;FUNCTION CODE = TEST
0034 E8C9FF            59               CALL    BENCHF
0037 B90B00            60               MOV     CX,11           ;BIT NUMBER = 11
003A BA0100            61               MOV     DX,1            ;FUNCTION CODE = TEST
003D E8C0FF            62               CALL    BENCHF
0040 B97B00            63               MOV     CX,123          ;BIT NUMBER = 123
0043 BA0100            64               MOV     DX,1            ;FUNCTION CODE = TEST
0046 E8B7FF            65               CALL    BENCHF
0049 B90A00            66               MOV     CX,10           ;BIT NUMBER = 10
004C BA0200            67               MOV     DX,2            ;FUNCTION CODE = SET
004F E8AEFF            68               CALL    BENCHF
0052 B90B00            69               MOV     CX,11           ;BIT NUMBER = 11
0055 BA0200            70               MOV     DX,2            ;FUNCTION CODE = SET
0058 E8A5FF            71               CALL    BENCHF
005B B97B00            72               MOV     CX,123          ;BIT NUMBER = 123
005E BA0200            73               MOV     DX,2            ;FUNCTION CODE = SET
0061 E89CFF            74               CALL    BENCHF
0064 B90A00            75               MOV     CX,10           ;BIT NUMBER = 10
0067 BA0300            76               MOV     DX,3            ;FUNCTION CODE = RESET
006A E893FF            77               CALL    BENCHF
006D B90B00            78               MOV     CX,11           ;BIT NUMBER = 11
0070 BA0300            79               MOV     DX,3            ;FUNCTION CODE = RESET
0073 E88AFF            80               CALL    BENCHF
0076 B97B00            81               MOV     CX,123          ;BIT NUMBER = 123
0079 BA0300            82               MOV     DX,3            ;FUNCTION CODE = RESET
007C E881FF            83               CALL    BENCHF
                       84       ;
                       85       ;       TEST DATA STRUCTURE FOR BIT ARRAY:
                       86       ;
```

BENCHMARK F-8086 (continued)

```
007F (125                87      T_ARRAY DB      125 DUP(10101010B)
      AA
      )

----                     88      ;
                         89      SEGA    ENDS
                         90      ;
                         91              END
```

BENCHMARK H-8086

```
                          1      ;       CARNEGIE-MELLON BENCHMARK SERIES [H]
                          2      ;
                          3      ;       LINKED LIST INSERTION FOR 8086
                          4      ;
----                      5      SEGA    SEGMENT
                          6              ASSUME CS:SEGA,DS:SEGA,ES:SEGA,SS:SEGA
                          7      ;
                          8      ;       TWO PARAMETERS ARE PASSED TO THE SUBROUTINE IN THE FOLLOWING REGISTERS:
                          9      ;
                         10      ;       BX=POINTER TO LIST COMMAND BLOCK:       HEAD (2-BYTE POINTER)
                         11      ;                                               TAIL (2-BYTE POINTER)
                         12      ;                                               NUMENT (2 BYTES)
                         13      ;       DI=POINTER TO NEW RECORD TO INSERT:     KEY (32-BIT SIGNED VALUE)
                         14      ;                                               NEXT (2-BYTE POINTER)
                         15      ;                                               PREV (2-BYTE POINTER)
                         16      ;
                         17      ;       IT IS ASSUMED THE CURRENT LIST, CONTROL BLOCK, AND NEW DATA
                         18      ;       ARE ALL IN THE ACTIVE DATA SEGMENT
                         19      ;
----                     20      CONTROL STRUC                   ;CONTROL BLOCK STRUCTURE
0000                     21      HEAD    DW      ?               ;FIRST WORD OF CONTROL BLOCK = LIST HEAD
0002                     22      TAIL    DW      ?               ;SECOND WORD = LIST TAIL
0004                     23      NUMENT  DW      ?               ;THIRD WORD = NUMBER OF ENTRIES IN LIST
----                     24      CONTROL ENDS
                         25      ;
----                     26      ENTRY   STRUC                   ;DEFINITION OF EACH ENTRY DATA STRUCTURE
0000                     27      KEY_LO  DW      ?               ;FIRST WORD OF RECORD = LOW-ORDER DATA
0002                     28      KEY_HI  DW      ?               ;SECOND WORD = HIGH-ORDER DATA
0004                     29      NEXT    DW      ?               ;THIRD WORD = NEXT RECORD POINTER
0006                     30      PREV    DW      ?               ;FOURTH WORD = PREVIOUS RECORD POINTER
----                     31      ENTRY   ENDS
                         32      ;
  REG                    33      NEW     EQU     DI              ;POINTER TO RECORD TO BE INSERTED
  REG                    34      LIST_CB EQU     BX              ;POSITION OF LIST CONTROL BLOCK
  REG                    35      PRESENT EQU     SI              ;POSITION IN SEGMENT OF RECORD BEING TESTED
                         36      ;
0000                     37      BENCHH  PROC
0000 50                  38              PUSH    AX              ;REGISTER WILL BE USED FOR KEY(HIGH) COMPARISON
0001 52                  39              PUSH    DX              ;REGISTER USED FOR KEY(LOW) COMPARISON
0002 51                  40              PUSH    CX              ;USED TO COUNT CYCLES THROUGH KEY TEST SEQUENCE
0003 56                  41              PUSH    SI              ;REGISTER WILL BE USED FOR RECORD ACCESSING
                         42      ;
0004 8B4F04              43              MOV     CX,[LIST_CB].NUMENT     ;LOAD COUNT OF RECORDS IN LIST
                         44      ;
                         45      ;       INITIALIZE LIST ENTRY AND CONTROL BLOCK IF LIST EMPTY:
                         46      ;
0007 E35A                47              JCXZ    EMPTY                   ;VERIFY THAT RECORD LIST NOT EMPTY
                         48      ;
                         49      ;       LIST NOT EMPTY, SO INITIALIZE REGISTERS FOR KEY TEST SEQUENCE:
                         50      ;
0009 8B37                51              MOV     PRESENT,[LIST_CB].HEAD  ;POINT TO FIRST RECORD
000B FF4704              52              INC     WORD PTR [LIST_CB].NUMENT
000E 8B4502              53              MOV     AX,[NEW].KEY_HI         ;LOAD HIGH-ORDER PORTION OF NEW KEY
0011 8B15                54              MOV     DX,[NEW].KEY_LO         ;LOAD LOW-ORDER PORTION
0013 EB03                55              JMP     SHORT TSTKEY
                         56      ;
0015 8B7404              57      LNKNXT: MOV     PRESENT,[PRESENT].NEXT  ;FOLLOW LINK TO NEXT RECORD
                         58      ;
                         59      ;       COMPARE KEY OF NEW RECORD WITH KEY OF CURRENT RECORD.
                         60      ;       WHILE NEW.KEY >= PRESENT.KEY & PRESENT.NEXT>0 DO PRESENT:=PRESENT.NEXT;
                         61      ;
0018 3B4402              62      TSTKEY: CMP     AX,[PRESENT].KEY_HI     ;PERFORM SIGNED-COMPARE OF HIGH WORD
001B 7F06                63              JG      DONCHK                  ;BRANCH IF NEWKEY<CURRENT KEY
001D 7C06                64              JL      INSERT                  ;BRANCH IF NEWKEY>CURRENT KEY
001F 3B14                65              CMP     DX,[PRESENT].KEY_LO     ;PERFORM UNSIGNED-COMPARE OF LOW WORD
0021 7202                66              JB      INSERT                  ;BRANCH IF NEWKEY>CURRENT KEY
0023 E2F0                67      DONCHK: LOOP    LNKNXT                  ;REPEAT LOOP IF NOT AT END OF LIST
                         68      ;
0025                     69      INSERT:
                         70      ;       AT THIS POINT, THE CONTENTS OF CX INDICATE HOW TEST LOOP WAS EXITED
                         71      ;       (CX=0 IF NEW.KEY >= PRESENT.KEY, CX>0 IF NEW.KEY < PRESENT.KEY)
                         72      ;
```

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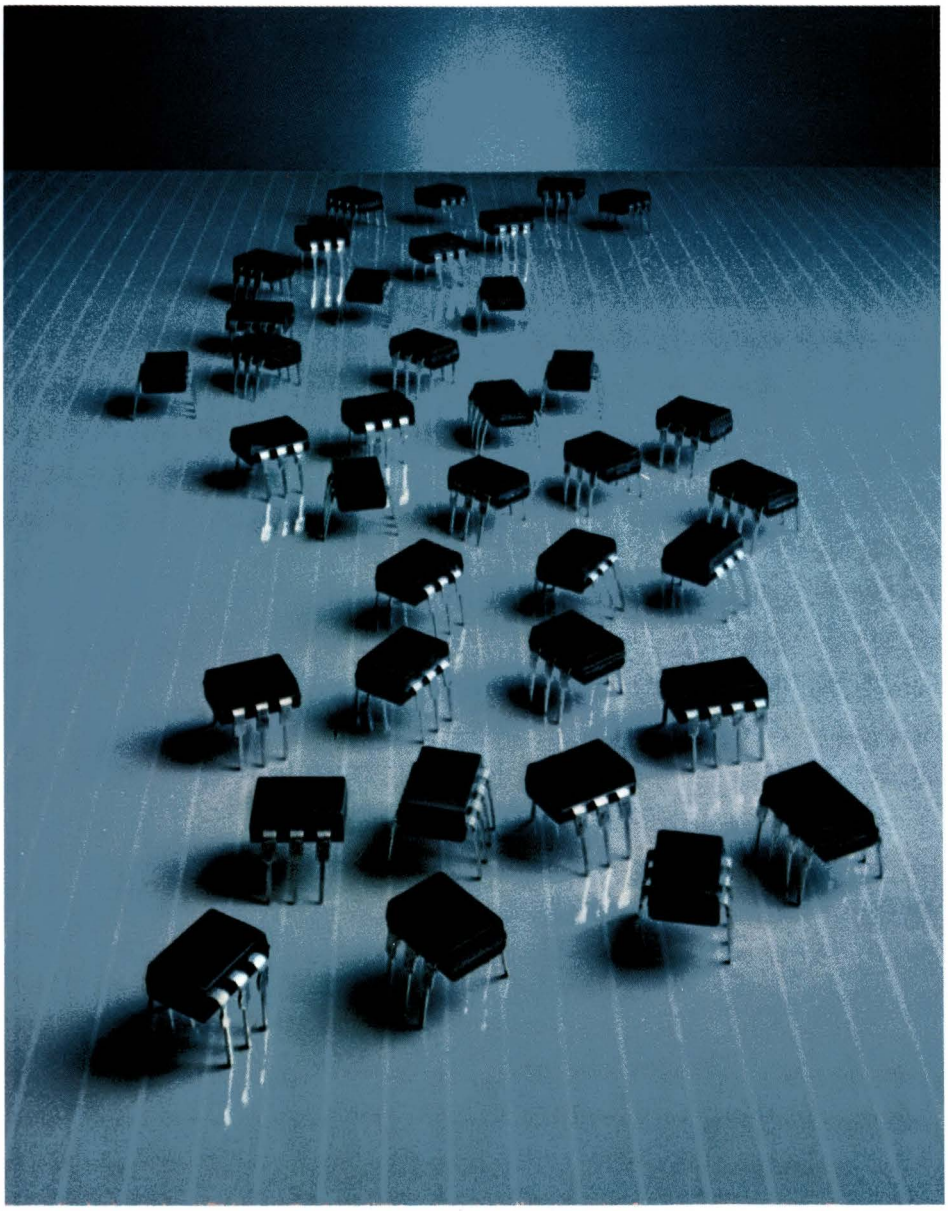

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BENCHMARK H-8086 (continued)

```
                        ;       IF PRESENT.PREV = 0 AND NEW.KEY < PRESENT.KEY THEN "NEW LIST HEAD"
                        ;
0025 33C0               XOR     AX,AX                   ;CLEAR AX REGISTER
0027 3B4406             CMP     AX,[PRESENT].PREV
002A 750F               JNZ     ELSE1                   ;BRANCH AHEAD IF PRESENT.PREV > 0
002C E30D               JCXZ    ELSE1                   ;    OR IF NEW.KEY >= PRESENT.KEY
                        ;
                        ;       INSERT NEW AT HEAD OF LIST
                        ;
002E 893F               MOV     [LIST_CB].HEAD,NEW
0030 894506             MOV     [NEW].PREV,AX           ;NOTE THAT AX=0
0033 897C06             MOV     [PRESENT].PREV,NEW
0036 897504             MOV     [NEW].NEXT,PRESENT
0039 EB23               JMP*    SHORT LST_RET
                        ;
003B                    ELSE1:
                        ;       IF NEW.KEY >=.PRESENT.KEY THEN "NEW LIST TAIL"
                        ;
003B 0BC9               OR      CX,CX                   ;TEST CONTENTS OF CX
003D 750E               JNZ     ELSE2                   ;BRANCH AHEAD IF CX>0
                        ;
                        ;       INSERT AT TAIL OF LIST
                        ;
003F 897C04             MOV     [PRESENT].NEXT,NEW
0042 897F02             MOV     [LIST_CB].TAIL,NEW
0045 894504             MOV     [NEW].NEXT,AX           ;NOTE AX=0
0048 897506             MOV     [NEW].PREV,PRESENT
004B EB11               JMP     SHORT LST_RET
                        ;
004D                    ELSE2:
                        ;       INSERT IN MIDDLE:
                        ;
004D 897504             MOV     [NEW].NEXT,PRESENT
0050 8B4406             MOV     AX,[PRESENT].PREV
0053 894506             MOV     [NEW].PREV,AX
0056 897C06             MOV     [PRESENT].PREV,NEW
                        ;
                        ;       BACK UP AND LINK WITH PREDECESSOR:
                        ;
0059 8BF0               MOV     PRESENT,AX              ;AX LOADED WITH PRESENT.PREV ABOVE
005B 897C04             MOV     [PRESENT].NEXT,NEW
                        ;
005E                    LST_RET:
005E 5E                 POP     SI
005F 59                 POP     CX
0060 5A                 POP     DX
0061 58                 POP     AX
0062 C3                 RET
                        ;
0063 893F               EMPTY:  MOV     [LIST_CB].HEAD,NEW
0065 897F02             MOV     [LIST_CB].TAIL,NEW
0068 FF4704             INC     WORD PTR [LIST_CB].NUMENT
006B 894D04*            MOV     [NEW].NEXT,CX           ;CLEAR POINTER FIELDS (NOTE CX=0)
006E 894D06             MOV     [NEW].PREV,CX
0071 EBEB               JMP     LST_RET
                        ;
                        BENCHH  ENDP
                        ;
                        ;=======
                    +1  $EJECT
0073 90                 EVEN                            ;ALIGN DATA ON WORD BOUNDARIES
                        ;
                        ;       DATA STRUCTURES AVAILABLE TO TEST ABOVE ALGORITHM:
                        ;
0074 ????               TBLOCK  DW      ?
0076 ????               DW      ?
0078 0000               DW      0
                        ;
007A 4523               TREC_1  DW      2345H
007C 0100               DW      0001H
007E ????               DW      ?
0080 ????               DW      ?
                        ;
0082 0023               TREC_2  DW      2300H
0084 0100               DW      0001H
0086 ????               DW      ?
0088 ????               DW      ?
                        ;
008A 4433               TREC_3  DW      3344H
008C 0100               DW      0001H
008E ????               DW      ?
0090 ????               DW      ?
                        ;
0092 4523               TREC_4  DW      2345H
0094 0100               DW      0001H
0096 ????               DW      ?
```

BENCHMARK H-8086 (continued)

```
0098 ????                159             DW      ?
                         160     ;
009A 2641                161     TREC_5  DW      4126H
009C 0300                162             DW      0003H
009E ????                163             DW      ?
00A0 ????                164             DW      ?
                         165     ;
                         166     ;       TEST SEQUENCE TO VERIFY ABOVE ALGORITHM:
                         167     ;
00A2 BB7400              168     TEST_H: MOV     BX,OFFSET TBLOCK
00A5 BF7A00              169             MOV     DI,OFFSET TREC_1
00A8 E855FF              170             CALL    BENCHH
00AB BF8200              171             MOV     DI,OFFSET TREC_2
00AE E84FFF              172             CALL    BENCHH
00B1 BF8A00              173             MOV     DI,OFFSET TREC_3
00B4 E849FF              174             CALL    BENCHH
00B7 BF9200              175             MOV     DI,OFFSET TREC_4
00BA E843FF              176             CALL    BENCHH
00BD BF9A00              177             MOV     DI,OFFSET TREC_5
00C0 E83DFF              178             CALL    BENCHH
00C3 EBFE                179             JMP     $
                         180     ;
----                     181     SEGA    ENDS
                         182     ;
                         183             END
```

BENCHMARK H-MC68000

```
 1                                       OPT     BRS
 2
 3                                *
 4                                *              MC68000  EDN BENCHMARK H
 5                                *
 6                                *       LINKED LIST INSERTION (SHORT ADDRESSES)
 7                                *
 8                                *  ATTRIBUTES:  * 64K BYTES ADDRESSING RANGE
 9                                *               * POSITION INDEPENDENT
10                                *               * REENTRANT
11                                *               * NO REWRITE NEEDED FOR DIFFERENT ADDRESSING
12                                *                 RANGE SINCE THE MC68000 HAS NO CUMBERSOME
13                                *                 SEGMENT HANDLING REQUIREMENTS
14                                *
15                                * INPUT:      A0 - LIST CONTROL BLOCK
16                                *             A1 - NEW LIST ENTRY POINTER
17                                *
18                                * OUTPUT:     THE NEW ENTRY IS PROPERLY CHAINED IN THE LINK
19                                *
20                                *       ALL OTHER REGISTERS ARE TRANSPARENT OVER THIS ROUTINE
21                                *
22                                *                       LINES:  33
23                                *                       BYTES: 100
24                                *
25                                *       MC68000L10 BENCHMARK TIME:  121.000 MICROSECONDS
26                                *       MC68000L12 BENCHMARK TIME:  100.833 MICROSECONDS
27                                *
28
29
30                               * DEFINITION OF LIST CONTROL BLOCK
31           00000004            NUMENTRY EQU     4                      COUNT OF ENTRIES
32           00000002            TAIL     EQU     2                      CURRENT TAIL
33           00000000            HEAD     EQU     0                      CURRENT HEAD
34
35                               * DEFINITION OF LIST ENTRY
36           00000006            PREV     EQU     6                      PREVIOUS ENTRY IN CHAIN
37           00000004            NEXT     EQU     4                      NEXT ENTRY IN CHAIN
38           00000000            KEY      EQU     0                      32 BIT BINARY KEY
39
40                               * LIST INSERT SUBROUTINE
41 0 00000000 4A680004           INSERT   TST      NUMENTRY(A0)           TEST IF LIST IS EMPTY
42 0 00000004 660C               BNE      NOTEMPTY                       BRANCH IF NOT
43
44                               * LIST IS EMPTY - START IT UP
45 0 00000006 30C9                        MOVE     A1,(A0)+               SET FIRST HEAD
46 0 00000008 30C9                        MOVE     A1,(A0)+               SET FIRST TAIL
47 0 0000000A 5250                        ADD      #1,(A0)                INCREMENT ENTRY COUNT
48 0 0000000C 42A90004                    CLR.L    NEXT(A1)               CLEAR NEW.NEXT AND PREV
49 0 00000010 4E75                        RTS                             RETURN TO CALLER
50
51                               *  REGISTER USAGE:
52                               *     D0 - NEW KEY VALUE     A0 - LISTCB POINTER
53                               *     D1 - NEXT CURRENT      A1 - NEW ENTRY POINTER
54                               *                            A2 - CURRENT ENTRY POINTER
55
56 0 00000012 48A7C020           NOTEMPTY MOVEM    D0/D1/A2,-(SP)         SAVE WORK REGISTERS
57 0 00000016 52680004                    ADD      #1,NUMENTRY(A0)        INCREMENT ENTRY COUNT
58 0 0000001A 2011                        MOVE.L   KEY(A1),D0             LOAD NEW KEY
```

BENCHMARK H-MC68000 (continued)

```
59 0 0000001C 3450                  MOVE     HEAD(A0),A2          START LIST SCAN
60 0 0000001E B092                  CMP.L    KEY(A2),D0           TEST IF IN VERY FRONT
61 0 00000020 6C1A                  BGE      SEARCH               BRANCH IF NOT NEW FIRST
62
63                            * ADD TO VERY BEGINNING
64 0 00000022 3089                  MOVE     A1,HEAD(A0)          SET NEW HEAD
65 0 00000024 35490006              MOVE     A1,PREV(A2)          OLDFIRST.PREV TO NEW
66 0 00000028 334A0004              MOVE     A2,NEXT(A1)          SET NEW.NEXT TO OLD FIRST
67 0 0000002C 42690006              CLR      PREV(A1)             ZERO NEW.PREV
68 0 00000030 602C                  BRA      FINISH               GO FINISH UP
69
70                            * ADD TO TAIL END
71 0 00000032 31490002      ADDEND  MOVE     A1,TAIL(A0)          NEW ENTRY IS NOW TAIL
72 0 00000036 234A0004              MOVE.L   A2,NEXT(A1)          SET NEW.NEXT ZERO AND NEW.PREV
73 0 0000003A 601E                  BRA      FINISHL              GO FINISH UP
74
75                            * SEARCH FOR CORRECT PLACEMENT
76 0 0000003C 322A0004      SEARCH  MOVE     NEXT(A2),D1          TO NEXT LIST ENTRY ADDRESS
77 0 00000040 67F0                  BEQ      ADDEND               ADD NEW TO END IF NO MORE
78 0 00000042 3441                  MOVE     D1,A2                READY NEW CURRENT POINTER
79 0 00000044 B092                  CMP.L    KEY(A2),D0           TEST IF BEYOND KEY VALUE
80 0 00000046 6CF4                  BGE      SEARCH               LOOP IF GREATER OR EQUAL
81
82                            * INSERT IN MIDDLE BEFORE CURRENT ENTRY
83 0 00000048 334A0004              MOVE     A2,NEXT(A1)          SET NEW.NEXT TO CURRENT
84 0 0000004C 336A00060006          MOVE     PREV(A2),PREV(A1)    SET CURRENT EARLIER TO NEW.PREV
85 0 00000052 35490006              MOVE     A1,PREV(A2)          SET CURREN.PREV TO NEW
86 0 00000056 34690006              MOVE     PREV(A1),A2          LOAD CURRENT EARLIER ADDRESS
87 0 0000005A 35490004      FINISHL MOVE     A1,NEXT(A2)          SET EARLIER.NEXT TO NEW
88
89                            * RESTORE REGISTERS AND RETURN
90 0 0000005E 4C9F0403      FINISH  MOVEM    (SP)+,D0/D1/A2       RESTORE REGISTERS
91 0 00000062 4E75                  RTS                           RETURN TO CALLER
92
93                                  END
```

BENCHMARK H-Z8002

```
                        BENCHMARK_H module

                        !Example H -- Insertion in a doubly linked list.

                                CALL INSERT  with the following arguments:
                                        R5 = Pointer to List Control Block
                                        R4 = Pointer to element to be inserted

                        !

                        constant


                                HEAD     := 0     ! Structure of list control block !
                                TAIL     := 2
                                NUM      := 4

                                KEYI     := 0     ! Structure of each entry !
                                NEXT     := 4
                                PREV     := 6

                                KEY      := RR0   ! Register allocation !
                                NEXTAD   := R2
                                PREVAD   := R3
                                NEWENTRY := R4    ! Address of element to be linked !
                                LISTCB   := R5    ! Address of list control block !
                                SP       := R15

                        global INSERT procedure
0000                    $rel 0
                        entry
0000 91F0                       PUSHL    @SP,RR0          ! Save work registers !
0002 91F2                       PUSHL    @SP,RR2
0004 8333                       SUB      PREVAD,PREVAD    ! Clear back ptr. !
0006 4D54                       TEST     NUM(LISTCB)      ! Check for first entry !
0008 0004
000A EE05                       JR       NZ,NOTFIRST

000C 8322                       SUB      NEXTAD,NEXTAD    ! Clear forward ptr. !
000E 2F54                       LD       @LISTCB,NEWENTRY! Set head in LCB !
0010 6F54                       LD       TAIL(LISTCB),NEWENTRY ! Set tail in LCB !
0012 0002
0014 E818                       JR       UPNEW

                        NOTFIRST:
0016 1440                       LDL      KEY,@NEWENTRY    ! Get the new key !
0018 2152                       LD       NEXTAD,@LISTCB   ! Start scan at head !
```

BENCHMARK H-Z8002 (continued)

```
                        SCAN:
001A 1020                       CPL     KEY,@NEXTAD     ! Compare keys !
001C E906                       JR      GE,TRYNEXT
001E 8D34                       TEST    PREVAD
0020 EE0E                       JR      NZ,UPMID
0022 2F54                       LD      @LISTCB,NEWENTRY
0024 6F24                       LD      PREV(NEXTAD),NEWENTRY
0026 0006
0028 E80E                       JR      UPNEW

                        TRYNEXT:
002A A123                       LD      PREVAD,NEXTAD   ! Goto next in the list !
002C 6132                       LD      NEXTAD,NEXT(PREVAD)
002E 0004
0030 8D24                       TEST    NEXTAD          ! At tail ? !
0032 EEF3                       JR      NZ,SCAN
0034 6F34                       LD      NEXT(PREVAD),NEWENTRY
0036 0004
0038 6F54                       LD      TAIL(LISTCB),NEWENTRY
003A 0002
003C E804                       JR      UPNEW

                        UPMID:
003E 6F24                       LD      PREV(NEXTAD),NEWENTRY
0040 0006
0042 6F34                       LD      NEXT(PREVAD),NEWENTRY
0044 0004

                        UPNEW:
0046 6950                       INC     NUM(LISTCB)     ! Update count field in LCB !
0048 0004
004A 5D42                       LDL     NEXT(NEWENTRY),RR2      ! Set ptrs in new entry
004C 0004
004E 95F2                       POPL    RR2,@SP         ! Restore registers !
0050 95F0                       POPL    RR0,@SP
0052 9E08                       RET

0054                    end INSERT


                        end BENCHMARK H
```

BENCHMARK I-8086

```
                          1                     name    test_benchmark_I
                          2     ;
                          3     ;               For the EDN algorithm and data:
                          4     ;
                          5     ;           276 bytes       38.254 msec with 8086-1 at 10 Mhz 0 wait
                          6     ;
0000                      7     code            segment public  'code'
                          8                     assume  cs:code
                          9     ;
                         10     ;           Define local values for records
                         11     ;
0007                     12     key_length      equ     7
0003                     13     key_offset      equ     3
0010                     14     record_size     equ     16
                         15     ;
                         16     ;           Quicksort function
                         17     ;
                         18     ;           Four parameters are passed in the registers:
                         19     ;
                         20     ;       n       number of elements 0 < N <= 10000       cx
                         21     ;       rec     pointer to start of record series       ds
                         22     ;       m       transfer point to insertion sort        bx
                         23     ;
                         24     ;       All registers are transparent except for the flags.
                         25     ;
                         26     ;           Define abbreviations commonly used.
                         27     ;
0008                     28     word_rec_size   equ     8
00FF                     29     largest_key     equ     0ffh
                         30     ;
                         31     ;           The following local variables are initialized and restored
                         32     ;       with pushes and pops.
                         33     ;
000A[]                   34     rec_ptr         equ     word ptr [bp+10]        ; Save area for rec_ptr
000C[]                   35     n               equ     rec_ptr+2               ; Save area for n
000E[]                   36     m               equ     n+2                     ; Save area for m
-0010[]                  37     temp_area       equ     byte ptr [bp-record_size]
                         38     ;
```

BENCHMARK i-8086 (continued)

```
                        39      ;               Start of sort function
                        40      ;
0000                    41      quick_sort      proc    far
                        42
0000 55                 43              push    bp                      ; Establish stack addressibility
0001 53                 44              push    bx                      ; Set m in local area
0002 51                 45              push    cx                      ; Set n in local area
0003 1E                 46              push    ds                      ; Set rec_ptr in local area
                        47
0004 50                 48              push    ax                      ; Save working registers
0005 52                 49              push    dx
0006 56                 50              push    si
0007 57                 51              push    di
0008 06                 52              push    es
0009 8BEC               53              mov     bp,sp                   ; Identify base of save area
                        54
000B 8CDB               55              mov     bx,ds                   ; Form .rec(0)
000D 43                 56              inc     bx                      ; bx = .rec(1)
000E 8BD3               57              mov     dx,bx                   ; dx,1 = .rec(1)
0010 03D9               58              add     bx,cx                   ; bx = .rec(N+1)
0012 4B                 59              dec     bx                      ; r = .rec(N)
0013 33C0               60              xor     ax,ax                   ; Indicate empty r,l save stack
0015 50                 61              push    ax                      ; Will be popped before insertion sort
                        62      ;
                        63      ;         Outer loop of quicksort before the insertion sort.
                        64      ;
                        65      ;         Register usage:
                        66      ;
                        67      ;       l       dx      Note:   r >= l + m
                        68      ;       r       bx              rec(l-1) <= rec(i) <= rec(r+1) for l <= i <= r
                        69      ;
0016                    70      outer_loop:
                        71
0016 55                 72              push    bp                      ; Save stack base
0017 53                 73              push    bx                      ; Save r for later
0018 43                 74              inc     bx                      ; Form j = r+1 in bx
0019 8BEA               75              mov     bp,dx                   ; Set i = l
001B                    76      restart_i_loop:
001B B80600             77              mov     ax,key_length-1
001E 8EC2               78              mov     es,dx                   ; es = .rec(l)
                        79      ;
                        80      ;         Skip over left part of subfile.
                        81      ;
                        82      ;       Register usage:
                        83      ;               es = ss
                        84      ;               bp      .rec(i)
                        85      ;               bx      .rec(j)
                        86      ;               ax      length-1 of key
                        87      ;               dx      .rec(l)
                        88      ;               ij      is pushed on stack holding either i or j
                        89      ;
0020                    90      i_loop:
0020 45                 91              inc     bp                      ; i = i+1
0021 8EDD               92              mov     ds,bp                   ; ds = .rec(i)
0023 BE0300             93              mov     si,key_offset
0026 8BFE               94              mov     di,si                   ; Set offset for v
0028 A6                 95              cmpsb                           ; Look at first byte of key
0029 72F5               96              jb      i_loop
002B 7706               97              ja      j_loop
                        98
002D 8BC8               99              mov     cx,ax                   ; Else examine the rest of the key
002F F3                100        repe  cmpsb                           ; Compare rec(i) - rec(l)
0030 A6
0031 72ED              101              jb      i_loop                  ; Continue while rec(i) < rec(l)
                       102      ;
                       103      ;       Assert: i <= j          es = .rec(l)
                       104      ;
                       105      ;         Skip over right part of subfile.
                       106      ;       Registers same as before except ax,ds = .rec(j).
                       107      ;
0033                   108      j_loop:
0033 4B                109              dec     bx                      ; j = j-1
0034 8EDB              110              mov     ds,bx                   ; ds = .rec(j)
0036 BE0300            111              mov     si,key_offset
0039 8BFE              112              mov     di,si                   ; Set offset for v
003B A6                113              cmpsb                           ; Look at the first byte of the key
003C 77F5              114              ja      j_loop
003E 7206              115              jb      compare_ij
                       116
0040 8BC8              117              mov     cx,ax                   ; Else look at the rest of the key
0042 F3                118        repe  cmpsb                           ; Compare rec(j) - rec(l)
0043 A6
0044 77ED              119              ja      j_loop                  ; Continue while rec(j) > rec(l)
                       120      ;
                       121      ;       Assert: j >= i-1        es = .rec(l)  ds=bx
                       122      ;
```

BENCHMARK I-8086 (continued)

```
                        123     ;           Compare j and i for swap test.
                        124     ;
0046                    125     compare_ij:
0046 33F6               126             xor     si,si                   ; Prepare for exchange of records
0048 8BFE               127             mov     di,si
004A B90800             128             mov     cx,word_rec_size        ; Get word size of a record
004D 3BEB               129             cmp     bp,bx
004F 730E               130             jae     swap_loop2              ; Jump if i >= j
                        131
0051 8EC5               132             mov     es,bp                   ; es = .rec(i)  ds = .rec(j)
                        133     ;
                        134     ;           Exchange rec(i) with rec(j).
                        135     ;
0053                    136     swap_loop1:
0053 268B05             137             mov     ax,es:[di]
0056 8704               138             xchg    [si],ax
0058 46                 139             inc     si                      ; Bump source pointer
0059 46                 140             inc     si
005A AB                 141             stosw                           ; Auto bump of destination pointer
005B E2F6               142             loop    swap_loop1
                        143
005D EBBC               144             jmp     restart_i_loop          ; Continue preorder loop
                        145     ;
                        146     ;           Save subfile definitions on the stack area.
                        147     ;       But first exchange rec(l) with rec(j).
                        148     ;
005F                    149     swap_loop2:
005F 268B05             150             mov     ax,es:[di]
0062 8704               151             xchg    [si],ax
0064 46                 152             inc     si                      ; Bump source pointer
0065 46                 153             inc     si
0066 AB                 154             stosw                           ; Auto bump of destination pointer
0067 E2F6               155             loop    swap_loop2
                        156     ;
                        157     ;       Assert: ds,bx = .rec(j)
                        158     ;               dx,es = .rec(l)
                        159     ;
                        160     ;           Compare the subfile sizes of j-l and r-j to determine the
                        161     ;       the next subfile to sort.  Note: Subfiles do not include j!
                        162     ;
0069 8BC3               163             mov     ax,bx                   ; Save j
006B 5B                 164             pop     bx                      ; Get bx=r
006C 8BF3               165             mov     si,bx                   ; si,bx = r
006E 2BF0               166             sub     si,ax                   ; si = r-j
0070 8BF8               167             mov     di,ax                   ; di = j
0072 2BFA               168             sub     di,dx                   ; di = j-l
0074 5D                 169             pop     bp                      ; Restore stack addressing
0075 8B4E0E             170             mov     cx,m                    ; cx = m
                        171     ;
                        172     ;           Register usage:
                        173     ;                   dx,es   .rec(l)
                        174     ;                   bx      .rec(r)
                        175     ;                   ax      .rec(j)
                        176     ;                   cx      m
                        177     ;                   si      subfile size of r-j
                        178     ;                   di      subfile size of j-l
                        179     ;
0078 3BF9               180             cmp     di,cx
007A 770C               181             ja      jl_bt_m                 ; Jump if j-l > m
                        182
007C 3BF1               183             cmp     si,cx
007E 771A               184             ja      set_new_l               ; Jump if r-j > m
                        185     ;
                        186     ;           Both subfile sizes <= m.
                        187     ;       Get next r,l pair from the stack if not empty
                        188     ;
0080 5B                 189             pop     bx                      ; See if the stack is empty
0081 0BDB               190             or      bx,bx                   ; Test r value
0083 741B               191             jz      end_outer               ; Do insertion sort if empty
                        192     ;
                        193     ;           Set l and r from the stack.
                        194     ;       Stack ordering is r,l,r,l,....
                        195     ;
0085 5A                 196             pop     dx                      ; Get l from stack
0086 EB8E               197             jmp     outer_loop
                        198     ;
                        199     ;           j-l > m,  See if r-j > m
                        200     ;
0088                    201     jl_bt_m:
0088 3BF1               202             cmp     si,cx                   ; Compare r-j with m
008A 7606               203             jbe     set_new_r               ; Jump if r-j <= m
                        204     ;
                        205     ;           See which subfile is largest, both are larger than m.
                        206     ;
008C 3BFE               207             cmp     di,si                   ; Compare j-l with r-j
008E 7208               208             jb      stack_lj                ; Jump if j-l < r-j
```

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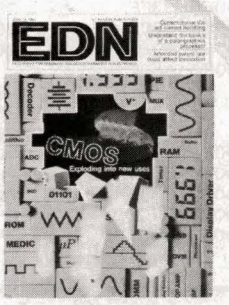

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BENCHMARK I-8086 (continued)

```
                        209     ;
                        210     ;         Push lower and upper limits of j-1, (the larger subfile).
                        211     ;       Stack ordering is: r,l,r,l,. . .
                        212     ;
0090 52                 213             push    dx                      ; Stack l = l
0091 50                 214             push    ax                      ; Stack r = j
0092                    215     set_new_r:
0092 8BD8               216             mov     bx,ax                   ; Set new r = j-1
0094 4B                 217             dec     bx                      ; l remains same
0095 E97EFF             218             jmp     outer_loop
                        219     ;
                        220     ;         Push lower and upper limits of r-j, (the larger subfile).
                        221     ;
0098                    222     stack_lj:
0098 52                 223             push    dx                      ; Stack l = l
0099 50                 224             push    ax                      ; Stack r = j
009A                    225     set_new_l:
009A 8BD0               226             mov     dx,ax                   ; Set l as j+1
009C 42                 227             inc     dx                      ; r remains same
009D E976FF             228             jmp     outer_loop
                        229     ;
                        230     ;         Perform an insertion sort on the entire record array.
                        231     ;
00A0                    232     end_outer:
00A0 83EC10             233             sub     sp,record_size          ; Allocate space for temp
00A3 8B5E0C             234             mov     bx,n                    ; Get original array length
00A6 035E0A             235             add     bx,rec_ptr              ; Form i = .rec(n)
00A9                    236     enter_last_loop:
00A9 B80600             237             mov     ax,key_length-1         ; Set key length
00AC BA0300             238             mov     dx,key_offset           ; Set key offset
                        239     ;
                        240     ;         Note: bx = i+1
                        241     ;
00AF                    242     last_loop:
00AF 4B                 243             dec     bx                      ; Form i = i - 1
00B0 3B5E0A             244             cmp     bx,rec_ptr              ; Test for .rec(0) implying i = 0
00B3 7653               245             jbe     done
                        246
00B5 8EDB               247             mov     ds,bx                   ; ds = .rec(i)
00B7 43                 248             inc     bx
00B8 8EC3               249             mov     es,bx                   ; es = .rec(i+1)
00BA 4B                 250             dec     bx                      ; Restore i
00BB 8BF2               251             mov     si,dx                   ; Set source and destination offset
00BD 8BFA               252             mov     di,dx
00BF A6                 253             cmpsb                           ; Compare 1st bytes of keys
00C0 72ED               254             jb      last_loop
00C2 7706               255             ja      move_down
                        256
00C4 8BC8               257             mov     cx,ax                   ; Examine rest of key
00C6 F3                 258       repe  cmpsb                           ; Compare rec(i) - rec(i+1)
00C7 A6
00C8 72E5               259             jb      last_loop               ; Loop while rec(i) < rec(i+1)
                        260     ;
                        261     ;         Move the entire subfile down one element until a record >= rec(i)
                        262     ;       is found.
                        263     ;
00CA                    264     move_down:
00CA B80800             265             mov     ax,word_rec_size        ; Get word count of a record
00CD 53                 266             push    bx                      ; Save i
00CE 8CD2               267             mov     dx,ss                   ; Save rec(i)
00D0 8EC2               268             mov     es,dx
00D2 8D7EF0             269             lea     di,temp_area            ; Set address of temp area
00D5 33F6               270             xor     si,si
00D7 8BC8               271             mov     cx,ax                   ; Set move count
00D9 F3                 272       rep   movsw                           ; v = rec(i)
00DA A5
00DB 8EC3               273             mov     es,bx                   ; j-1 becomes i in bx
                        274     ;
                        275     ;         Use es = ds = .rec(j-1).
                        276     ;       Assert: dx=ss
                        277     ;
00DD                    278     move_down_loop:
                        279
00DD BE1000             280             mov     si,record_size          ; si is offset for rec(j)
00E0 33FF               281             xor     di,di                   ; di is offset for rec(j-1)
00E2 8BC8               282             mov     cx,ax                   ; Set move length
00E4 F3                 283       rep   movsw                           ; rec(j-1) = rec(j)
00E5 A5
                        284     ;
                        285     ;         Note: si is offset for rec(j+1) now.
                        286     ;
00E6 43                 287             inc     bx                      ; j = j + 1
00E7 8EC2               288             mov     es,dx                   ; es:di = .v
00E9 8D7EF3             289             lea     di,temp_area+key_offset ; Set address of temp area
00EC 83C603             290             add     si,key_offset           ; si has offset for rec(j) key
00EF B90700             291             mov     cx,key_length           ; Set size of compare string
```

BENCHMARK I-8086 (continued)

```
00F2 F3              292       repe  cmpsb                           ; Compare rec(j) with v
00F3 A6
00F4 8EC3            293             mov     es,bx                   ; Set new base address
00F6 8EDB            294             mov     ds,bx
00F8 72E3            295             jb      move_down_loop          ; Continue while rec(j) < v
                     296       ;
                     297       ;       Copy v to rec(old j).
                     298       ;
00FA 33FF            299             xor     di,di                   ; Set offset to rec(j-1)
00FC 8EDA            300             mov     ds,dx                   ; Get address of v in ds:si
00FE 8D76F0          301             lea     si,temp_area            ; Set address of temporary area
0101 8BC8            302             mov     cx,ax                   ; Set move length
0103 F3              303       rep   movsw                           ; rec(j-1) = v
0104 A5
0105 5B              304             pop     bx                      ; Restore i
0106 EBA1            305             jmp     enter_last_loop
                     306       ;
                     307       ;       All done, restore registers.
                     308       ;
0108                 309       done:
0108 8BE5            310             mov     sp,bp                   ; Clear stack area
010A 07              311             pop     es
010B 5F              312             pop     di
010C 5E              313             pop     si
010D 5A              314             pop     dx
010E 58              315             pop     ax
                     316
010F 1F              317             pop     ds                      ; Restore rec ptr
0110 59              318             pop     cx                      ; Restore n
0111 5B              319             pop     bx                      ; Restore m
0112 5D              320             pop     bp
0113 CB              321             ret
                     322
                     323       quick_sort    endp
                     324 +1    $eject
                     325       ;
                     326       ;       Define EDN data characteristics
                     327       ;
  0064               328       n_value       equ     100
  0009               329       m_value       equ     9
                     330       ;
                     331       ;       Define local stack area.
                     332       ;
----                 333       stack         segment
0000 (96             334                     dw      96 dup (?)              ; I,R values are saved here
     ????
     )
00C0                 335       stack_top     label   word                    ; Start of stack area
----                 336       stack         ends
                     337       ;
                     338       ;       Define local data area.
                     339       ;
----                 340       data          segment
0000 (1632           341                     db      (n_value+2)*record_size dup (?)
     ??
     )
----                 342       data          ends
                     343       ;
                     344       ;       Mainline function to initialize memory, invoke sort, and
                     345       ;     test result.
                     346       ;
0114                 347       start:
0114 B8----      R   348             mov     ax,stack                ; Setup stack space
0117 8ED0            349             mov     ss,ax
0119 BCC000          350             mov     sp,offset stack_top
011C FB              351             sti                             ; Allow debugging interrupts
                     352       ;
                     353       ;       Run the benchmark
                     354       ;
011D                 355       restart:
011D B8----      R   356             mov     ax,data                 ; Get start of data segment
0120 8ED8            357             mov     ds,ax
0122 8EC0            358             mov     es,ax
0124 33FF            359             xor     di,di                   ; Clear starting address
0126 8BC7            360             mov     ax,di                   ; Clear initial value
0128 FC              361             cld                             ; Clear direction flag
0129 B96006          362             mov     cx,record_size*(n_value+2) ; Zero out all the entries
012C F3              363         rep stosb
012D AA
                     364       ;
                     365       ;       Initialize all the data entries in reverse order.
                     366       ;
012E B0FF            367             mov     al,0ffh                 ; Largest key entry
0130 B96400          368             mov     cx,n_value              ; Set loop count
0133 BF1000          369             mov     di,record_size          ; Form address of first entry
0136                 370       init_loop:
```

BENCHMARK I-8086 (continued)

```
0136 8805                371             mov     [di],al                 ; Set flag entry
0138 884503              372             mov     [di+key_offset],al      ; Set first byte of key
013B 48                  373             dec     ax                      ; Bump to next lowest key
013C 83C710              374             add     di,record_size          ; Go to next record
013F E2F5                375             loop    init_loop
                         376     ;
                         377     ;         Set last element in array to largest key possible.
                         378     ;
0141 83C703              379             add     di,key_offset           ; Point at key entry
0144 B90700              380             mov     cx,key_length           ; Get length of key
0147 B0FF                381             mov     al,largest_key          ; Largest key
0149 F3                  382       rep   stosb                           ; Set value
014A AA
                         383     ;
                         384     ;         Setup registers for function parameters
                         385     ;
014B B96400              386             mov     cx,n_value              ; Set record count
014E BB0900              387             mov     bx,m_value              ; Set subfile sort length
                         388     ;
                         389     ;            Time the function with SDK-86 counter.
                         390     ;
0151 BAFEFF              391             mov     dx,0FFFEH               ; Initialize counter
0154 B89292              392             mov     ax,9292H
0157 EF                  393             out     dx,ax
0158 BAFCFF              394             mov     dx,0FFFCH               ; Start counter
015B B80200              395             mov     ax,2
015E EF                  396             out     dx,ax
015F B80100              397             mov     ax,1
0162 EF                  398             out     dx,ax                   ; Go!
                         399
0163 9A0000----    R     400             call    far ptr quick_sort      ; Do the benchmark
                         401
0168 33C0                402             xor     ax,ax                   ; Timer stop command
016A EF                  403             out     dx,ax                   ; Stop timer!
                         404     ;
                         405     ;         Calculate the elapsed time in clocks
                         406     ;
016B BAF9FF              407             mov     dx,0FFF9H               ; Get counter value
016E ED                  408             in      ax,dx                   ; Read bits 31-24
016F 8AF8                409             mov     bh,al                   ; Save value
0171 BAF8FF              410             mov     dx,0FFF8H
0174 ED                  411             in      ax,dx                   ; Read bits 23-16
0175 8AD8                412             mov     bl,al
0177 BAFBFF              413             mov     dx,0FFFBH
017A ED                  414             in      ax,dx                   ; Read bits 15-8
017B 8AC8                415             mov     cl,al
017D BAFAFF              416             mov     dx,0FFFAH
0180 ED                  417             in      ax,dx                   ; Read bits 7-0
0181 8AE1                418             mov     ah,cl                   ; 32 bit clock count in dx:ax
0183 8BD3                419             mov     dx,bx
                         420     ;
                         421     ;         Test results to see if everything is in order
                         422     ;
0185 FC                  423             cld                             ; Autoincrement direction
0186 BB----        R     424             mov     bx,data                 ; Get starting address
0189 8D6500              425             mov     bp,n_value+1            ; Set loop count
018C                     426     compare_loop:
018C 8EDB                427             mov     ds,bx                   ; Set record addresses
018E 43                  428             inc     bx
018F 8EC3                429             mov     es,bx
0191 B90700              430             mov     cx,key_length
0194 BE0300              431             mov     si,key_offset
0197 8BFE                432             mov     di,si
0199 F3                  433       repe  cmpsb
019A A6
019B 7709                434             ja      exit                    ; Out of order!
                         435
019D 4D                  436             dec     bp                      ; Test for end
019E 75EC                437             jnz     compare_loop
                         438
01A0 33C9                439             xor     cx,cx                   ; Indicate all is well
01A2 CC                  440             int     3                       ; All done...enter monitor
01A3 E977FF              441             jmp     restart                 ; Restart benchmark
01A6                     442     exit:
01A6 B9FFFF              443             mov     cx,0FFFFH               ; Indicate misordered items
01A9 CC                  444             int     3                       ; All done...enter monitor
01AA E970FF              445             jmp     restart                 ; Restart benchmark
                         446
----                     447     code    ends
                         448
  0114                   449             end     start
```

BENCHMARK I-MC68000

```
1                                       OPT      BRS
2
3                                *
4                                *               MC68000  EDN BENCHMARK I
5                                *
6                                *                     QUICKSORT
7                                *
8                                *  ATTRIBUTES:  * 16 MEGABYTES ADDRESS RANGE
9                                *               * POSITION INDEPENDENT
10                               *              -* REENTRANT
11                               *
12                               *  INPUT:  D0 - "N" RECORD COUNT
13                               *          D1 - "M" THRESHOLD FOR INSERTION SORT
14                               *          A0 - "REC" ADDRESS OF THE SORT ARRAY
15                               *
16                               *  OUTPUT: THE SORT DATA ARRAY IS SORTED
17                               *
18                               *     ALL REGISTERS ARE TRANSPARENT OVER THIS ROUTINE
19                               *
20                               *                     LINES: 93
21                               *                     BYTES: 276
22                               *
23                               *   MC68000L10 BENCHMARK TIME:  17,348.200 MICROSECONDS
24                               *   MC68000L12 BENCHMARK TIME:  14,456.833 MICROSECONDS
25                               *
26
27
28                               * MISCELLANEOUS EQUATES
29                00000010       ENTRYLEN EQU      16                    SORT ENTRY RECORD LENGTH
30                00000003       KEY      EQU      3                     OFFSET TO KEY WITHIN RECORD
31                00000007       KEYLEN   EQU      7                     SORT KEY LENGTH
32
33
34                               *                      QUICKSORT SUBROUTINE
35  0 00000000 48E7FFFE          QUICK    MOVEM.L  D0-D7/A0-A6,-(SP)     SAVE ALL REGISTERS
36  0 00000004 2400                       MOVE.L   D0,D2                 COPY NUMBER OF RECORDS OVER
37  0 00000006 E988                       LSL.L    #4,D0                 CALCULATE POINTER TO LAST RECORD
38  0 00000008 43F008F0                   LEA      -ENTRYLEN(A0,D0.L),A1 A1 <- POINTER TO LAST RECORD = R
39  0 0000000C E989                       LSL.L    #4,D1                 FIND TOTAL SIZE OF M RECORDS
40  0 0000000E 2C41                       MOVE.L   D1,A6                 KEEP VALUE IN A6 FOR LATER
41  0 00000010 48E7A040                   MOVEM.L  D0/D2/A1,-(SP)        SAVE DUMMY, COUNT, AND TOP ON STACK
42  0 00000014 42A7                       CLR.L    -(SP)                 MARK SORT STACK EMPTY
43
44                               *                      QUICKSORT PHASE
45                               * REGISTER USE:  A0 - FIRST RECORD OF SUBFILE    A1 - LAST RECORD OF SUBFILE
46                               *                A2/A3 - KEY POINTERS            A4/A5 - WORK POINTERS
47                               *                A6 - LENGTH OF "M" RECORDS      SP - RECURSIVE CALL ARGUMENTS
48
49  0 00000016 45E80003          SORT     LEA      KEY(A0),A2            A2 -> KEY(I) = REC(L)
50  0 0000001A 47E90013                   LEA      ENTRYLEN+KEY(A1),A3   A3 -> KEY(J) = REC(R+1)
51  0 0000001E 49E80003          LOOP1    LEA      KEY(A0),A4            A4 -> V FOR CURRENT RECORD
52  0 00000022 1E14                       MOVE.B   (A4),D7               D0.B = FIRST BYTE OF KEY
53  0 00000024 45EA0010          LOOP1A   LEA      ENTRYLEN(A2),A2       I <- I+1
54  0 00000028 BE12                       CMP.B    (A2),D7               COMPARE FIRST KEY BYTE
55  0 0000002A 62F8                       BHI      LOOP1A                IF REC(I)<V CONTINUE COMPARING
56  0 0000002C 650C                       BLO      LOOP2                 IF REC(I)>V SCAN OTHER DIRECTION
57  0 0000002E 2A4A                       MOVE.L   A2,A5                 A5 TEMP FOR I
58  0 00000030 7006                       MOVE.L   #KEYLEN-1,D0          D0=LOOP COUNTER
59  0 00000032 B90D              CMP1     CMP.B    (A5)+,(A4)+           COMPARE V-REC(I)
60  0 00000034 56C8FFFC                   DBNE     D0,CMP1               LOOP WHILE EQUAL
61  0 00000038 62EA                       BHI      LOOP1A                IF REC(I)<V CONTINUE COMPARING
62
63  0 0000003A 47EBFFF0          LOOP2    LEA      -ENTRYLEN(A3),A3      J <- J-1
64  0 0000003E BE13                       CMP.B    (A3),D7               COMPARE FIRST KEY BYTE
65  0 00000040 65F8                       BLO      LOOP2                 LOOP WHILE REC(I)>V
66  0 00000042 620C                       BHI      LOOP2A                BRANCH REC(I)<V
67  0 00000044 2A4B                       MOVE.L   A3,A5                 A5 = TEMP FOR J
68  0 00000046 7006                       MOVE.L   #KEYLEN-1,D0          LOOP COUNTER
69  0 00000048 BB0C              CMP2     CMP.B    (A4)+,(A5)+           COMPARE REC(J)-V
70  0 0000004A 56C8FFFC                   DBNE     D0,CMP2               LOOP WHILE EQUAL
71  0 0000004E 62EA                       BHI      LOOP2                 IF REC(J)>V CONTINUE COMPARING
72  0 00000050 B5CB              LOOP2A   CMP.L    A3,A2                 I >= J
73  0 00000052 6436                       BCC      END1ST                BRANCH IF I >= J
74  0 00000054 4CEA000FFFFD               MOVEM.L  -KEY(A2),D0-D3        SWAP
75  0 0000005A 4CEB00F0FFFD               MOVEM.L  -KEY(A3),D4-D7        .      REC(J)
76  0 00000060 48EB000FFFFD               MOVEM.L  D0-D3,-KEY(A3)        .            WITH
77  0 00000066 48EA00F0FFFD               MOVEM.L  D4-D7,-KEY(A2)        .                 REC(I)
78  0 0000006C 60B0                       BRA      LOOP1                 CONTINUE
79
80                               * DECIDE SUBFILE DIRECTION
81  0 0000006E B28E              NEWLR0   CMP.L    A6,D1                 (R-J) <= MSIZE? (R-J) SUBFILE SMALLER?
82  0 00000070 6F08                       BLE      NEWR                  BRANCH IF SO
83  0 00000072 B481                       CMP.L    D1,D2                 DETERMINE SMALLER SUBFILE
84  0 00000074 650A                       BCS      STACK1                BRANCH IF (J-L) IS SMALLER
85  0 00000076 2F09                       MOVE.L   A1,-(SP)              STACK R
86  0 00000078 2F0B                       MOVE.L   A3,-(SP)              STACK J
87                               *                                      (R-J) SUBFILE SMALLER, SET L & R TO
88                               *                                      LARGER SUBFILE LIMITS
89  0 0000007A 43EBFFF0          NEWR     LEA      -ENTRYLEN(A3),A1      R <- J-1, L STAYS THE SAME
90  0 0000007E 6096                       BRA      SORT                  CONTINUE SORT
91                               *                                      (J-L) SUBFILE SMALLER, SET L & R TO
92                               *                                      LARGER SUBFILE LIMITS
93  0 00000080 48E70090          STACK1   MOVEM.L  A0/A3,-(SP)           PUSH L & J ONTO SORT STACK
94  0 00000084 41EB0010          NEWLR1   LEA      ENTRYLEN(A3),A0       L <- J+1, R STAYS THE SAME
95  0 00000088 608C                       BRA      SORT                  CONTINUE SORT
```

BENCHMARK I-MC68000 (continued)

```
 96
 97                                    * NEW SUBFILE FOUND, NOW DETERMINE NEXT STAGE
 98 0 0000008A 578B                    ENDIST   SUB.L    #KEY,A3              -KEY TO GET TO BEGINNING OF RECORD
 99 0 0000008C 4CD0000F                         MOVEM.L   (A0),D0-D3           SWAP
100 0 00000090 4CD300F0                         MOVEM.L   (A3),D4-D7           .     REC(L)
101 0 00000094 48D3000F                         MOVEM.L   D0-D3,(A3)           .           AND
102 0 00000098 48D000F0                         MOVEM.L   D4-D7,(A0)           .               REC(J)
103 0 0000009C 2209                             MOVE.L    A1,D1                D1 <- R
104 0 0000009E 240B                             MOVE.L    A3,D2                D2 <- J
105 0 000000A0 9282                             SUB.L     D2,D1                D1 <- R-J
106 0 000000A2 9488                             SUB.L     A0,D2                D2 <- J-L
107 0 000000A4 B48E                             CMP.L     A6,D2                COMPARE (J-L) <= MSIZE
108 0 000000A6 62C6                             BHI       NEWLR0               BRANCH IF NO
109 0 000000A8 B28E                             CMP.L     A6,D1                COMPARE (R-J) <= MSIZE
110 0 000000AA 62D8                             BHI       NEWLR1               BRANCH IF NO
111 0 000000AC 4CDF0300                         MOVEM.L   (SP)+,A0/A1          POP NEXT L AND R FROM STACK
112 0 000000B0 2008                             MOVE.L    A0,D0                TEST IF STACK IS EMPTY
113 0 000000B2 6600FF62                         BNE       SORT                 CONTINUE SORT IF NOT EMPTY
114
115                                    * FALL INTO INSERTION SORT AS ALL SUBFILES BELOW OR EQUAL M RECORDS
117                                    *                    INSERTION SORT PHASE
118                                    *
119                                    *  REGISTER USE: D0 - LOOP CONTROL              A0 - REC(I)
120                                    *                D1 - COUNTER AND SWAP REGISTER A1 - REC(J)
121                                    *                D2/D4 - SWAP REGISTERS         A2/A3 - WORK REGISTERS
122                                    *                D5/D7 - "V" SAVE REGISTERS     A4 - REC(J-1)
123                                    *                                               A5 - "V" SAVE REGISTER
124                                    *                                               A6 - FRAME POINTER
125                                    *
126                                    *       NOTE:  STACK SPACE IS RESERVED FOR "V" KEY COMPARE RECORD COPIES
127                                    *
128
129 0 000000B6 4CDF0101                          MOVEM.L   (SP)+,D0/A0          RELOAD RECORD COUNT AND TOP RECORD
130 0 000000BA 4E56FFF0                          LINK      A6,#-ENTRYLEN        ALLOCATE "V" KEY COPY AREA ON STACK
131 0 000000BE 5540                              SUB       #2,D0                DO RANGES FROM N-2 THROUGH 0
132
133 0 000000C0 41E8FFF0                LOOPOUT   LEA       -ENTRYLEN(A0),A0     I <- I-1
134 0 000000C4 45E80003                          LEA       KEY(A0),A2           A2 -> KEY(I)
135 0 000000C8 47E80013                          LEA       ENTRYLEN+KEY(A0),A3  A3 -> KEY(I+1)
136 0 000000CC 7206                              MOVE.L    #KEYLEN-1,D1         LOOP COUNTER FOR COMPARE
137 0 000000CE B50B                    CMPII1    CMP.B     (A3)+,(A2)+          COMPARE KEY(I)-KEY(I+1)
138 0 000000D0 56C9FFFC                          DBNE      D1,CMPII1            LOOP WHILE EQUAL
139 0 000000D4 6332                              BLS       ENDIF                BRANCH IF KEY(I) <= KEY(I+1)
140
141 0 000000D6 4CD020E0                          MOVEM.L   (A0),D5-D7/A5        V  <-  REC(I)
142 0 000000DA 48D700E0                          MOVEM.L   D5-D7,(SP)           AND ON STACK FOR KEY COMPARE
143 0 000000DE 43E80010                          LEA       ENTRYLEN(A0),A1      A1 -> REC(J) = REC(I+1)
144 0 000000E2 2848                              MOVE.L    A0,A4                PRIME A4 -> REC(J-1)
145
146 0 000000E4 4CD1001E                LOOPIN    MOVEM.L   (A1),D1-D4           TEMP <- REC(J)
147 0 000000E8 48D4001E                          MOVEM.L   D1-D4,(A4)           REC(J-1) <- TEMP
148 0 000000EC 2849                              MOVE.L    A1,A4                A4 -> NEXT REC(J-1)
149 0 000000EE 43E90010                          LEA       ENTRYLEN(A1),A1      J = J+1
150 0 000000F2 45EF0003                          LEA       KEY(SP),A2           A2 -> KEY(V)
151 0 000000F6 47E90003                          LEA       KEY(A1),A3           A3 -> KEY(J)
152 0 000000FA 7206                              MOVE.L    #KEYLEN-1,D1         LOOP COUNTER IN D1
153 0 000000FC B50B                    CMPVJ     CMP.B     (A3)+,(A2)+          COMPARE KEY(V)-KEY(J)
154 0 000000FE 56C9FFFC                          DBNE      D1,CMPVJ             LOOP WHILE EQUAL
155 0 00000102 62E0                              BHI       LOOPIN               IF KEY(V) > KEY(J) CONTINUE LOOP
156
157 0 00000104 48D420E0                          MOVEM.L   D5-D7/A5,(A4)        REC(J-1) <- V
158
159 0 00000108 51C8FFB6                ENDIF     DBRA      D0,LOOPOUT           CONTINUE LINEAR INSERT
160
161 0 0000010C 4E5E                              UNLK      A6                   FREE AND RESTORE STACK
162 0 0000010E 4CDF7FFF                          MOVEM.L   (SP)+,D0-D7/A0-A6    RESTORE REGISTERS
163 0 00000112 4E75                              RTS                            RETURN TO CALLER
164
165
166                                              END
```

BENCHMARK I-Z8002

```
QUICKSORT module
!Revised Quicksort/Insertion Sort for EDN Benchmark I
        CALL QUICK
                R0 = N (number of records)
                R1 = M (changeover interval width)
               R13 = REC (base address of array to be sorted
        Returns with array sorted and all registers unchanged

 Arguments:  !
constant
        N       := R0
        M       := R1
        REC     := R13
!Working registers
  Quicksort phase: !
        SP      := R15
```

BENCHMARK I-Z8002 (continued)

```
                        MLEN    := Rl4  !Length (bytes) of M records!
                        L       := Rl3  !(=REC) Left boundary of range!
                        R       := Rl2  !Right boundary of range!
                         NEWLR  := RRl2 !L and R as a pair!
                        KI      := Rll  !Key pointer for REC(I)!
                        KJ      := Rl0  !Key pointer for REC(J)!
                         KIJ    := RRl0 !I and J as a pair!
                        CNT     := R9   !Count register for block operations!
                        Wl      := R8   !Work registers!
                        W2      := R7
                        VKEY    := R6   !Key pointer for REC(V)!
                        VVAL    := RH5  !First byte of VKEY !
                        !(R0 - R7 used for exchanging items)!
                !Insertion sort phase: !
                        I       := Rl4  !Pointer to REC(I)!
                        J       := Rl3  !Pointer to REC(J)!
                        JMl     := Rl2  !Pointer to REC(J-l)!
                        VKEYl   := Rll
                        LCNT    := Rl0  !Counter for outer loop!
                        !CNT    := R9    (as in Quicksort phase)!
                        !Wl     := R8    (as in Quicksort phase)!
                        !W2     := R7!
                        !(R0 - R7 used for moving items)!
                !General definitions: !
                        ESIZE   := l6   !Bytes per entry!
                        KEY     := 3    !Position of key in entry!
                        KEYLEN  := 7    !Bytes per key!
                !Initialization!
0000                    global QUICK procedure entry
0000 030F               SUB SP,#30              !Save R0 - Rl4!
0002 001E
0004 1CF9               LDM @SP,R0,#l5
0006 000E
0008 Al03               LD R3,N                 !Compute adr of last item!
000A AB30               DEC R3
000C 1902               MULT RR2,#ESIZE
000E 0010
0010 Al3C               LD R,R3
0012 81DC               ADD R,REC
0014 Al13               LD R3,M                 !Compute size of M items!
0016 1902               MULT RR2,#ESIZE
0018 0010
001A Al3E               LD MLEN,R3
001C 93FC               PUSH @SP,R              !Save top!
001E 93F0               PUSH @SP,N              !Save number of items!
0020 9200               SUBL RR0,RR0            !Mark sort stack empty!
0022 91F0               PUSHL @SP,RR0
                !Quicksort phase!
0024 94CA       SORT:   LDL KIJ,NEWLR
0026 A9B2               INC KI,#KEY             !KI points at key for I!
0028 010A               ADD KJ,#KEY+ESIZE       !KJ points at key for J!
002A 0013
                LOOP0;
002C AlD6               LD VKEY,L               !VKEY points at key for pivot!
002E A962               INC VKEY,#KEY
0030 2065               LDB VVAL,@VKEY          !VVAL holds first byte of V key
0032 A9BF       LOOPl:  INC KI,#ESIZE           !I gets I+l!
0034 0AB5               CPB VVAL,@KI            !Compare first byte explicitly !
0036 EBFD                 JR UGT,LOOPl          ! REC(I) < V !
0038 E706                 JR ULT,LOOP2          ! REC(I) > V !
003A Al68               LD Wl,VKEY              !Wl points at V key!
003C Al37               LD W2,KI                !Copy I for block comparison!
003E BD97               LDK CNT,#KEYLEN         !Count for comparison!
0040 BA86               CPSIRB,@W2,@Wl,CNT,NE   !Compare I,V!
0042 097E
0044 E7F6                 JR ULT,LOOPl          !REC(I) < V!
                LOOP2:                          !REC(I) >= V; now move J!
0046 ABAF               DEC KJ,#ESIZE           !J gets J-l!
0048 0AA5               CPB VVAL,@KJ
004A E7FD                 JR ULT,LOOP2
004C EB06                 JR UGT,LOOP2A
004E AlA7               LD W2,KJ                !Set up block comparison!
0050 Al68               LD Wl,VKEY
0052 BD97               LDK CNT,#KEYLEN
0054 BA76               CPSIRB @Wl,@W2,CNT,NE   !Compare V,J!
0056 098E
0058 E7F6                 JR ULT,LOOP2          !V < REC(J)!
005A 3BAB       LOOP2A: CP KI,KJ                !Compare I,J!
005C EFl9                 JR UGE,ENDlST         !Done if I >= J!
                  !Exchange REC(I),REC(J)!
005E 5CAl               LDM R0,-KEY(KJ),#4; LDM R4,-KEY(KI),#4
0060 0003
0062 FFFD
0064 5CBl
0066 0403
0068 FFFD
```

BENCHMARK I-Z8002 (continued)

```
006A 5CA9               LDM -KEY(KJ),R4,#4; LDM -KEY(KI),R0,#4
006C 0403
006E FFFD
0070 5CB9
0072 0003
0074 FFFD
0076 5CA1               LDM R0,ESIZE/2-KEY(KJ),#4; LDM R4,ESIZE/2-KEY(KI),#4
0078 0003
007A 0005
007C 5CB1
007E 0403
0080 0005
0082 5CA9               LDM ESIZE/2-KEY(KJ),R4,#4; LDM ESIZE/2-KEY(KI),R0,#4
0084 0403
0086 0005
0088 5CB9
008A 0003
008C 0005
008E E8CE               JR LOOP0
                      !New subfile found - now determine next stage!
0090 ABA2           END1ST: DEC KJ,#KEY             !Point at REC(J)!
                      !Exchange REC(J),REC(L)!
0092 1CA1               LDM R0,@KJ,#4; LDM R4,@L,#4
0094 0003
0096 1CD1
0098 0403
009A 1CA9               LDM @KJ,R4,#4; LDM @L,R0,#4
009C 0403
009E 1CD9
00A0 0003
00A2 5CA1               LDM R0,ESIZE/2(KJ),#4; LDM R4,ESIZE/2(L),#4
00A4 0003
00A6 0008
00A8 5CD1
00AA 0403
00AC 0008
00AE 5CA9               LDM ESIZE/2(KJ),R4,#4; LDM ESIZE/2(L),R0,#4
00B0 0403
00B2 0008
00B4 5CD9
00B6 0003
00B8 0008
00BA A1C0               LD R0,R                 !R0 gets R-J!
00BC 83A0               SUB R0,KJ
00BE A1A1               LD R1,KJ                !R1 gets J-L!
00C0 83D1               SUB R1,L
00C2 8BE1               CP R1,MLEN              !J-L <= M? !
00C4 EA06                 JR GT,NEWLR0          !  No - try R-J!
00C6 8BE0               CP R0,MLEN              !  Yes - try R-J!
00C8 EA0F                 JR GT,NEWLR1          !    R-J > M!
00CA 95FC               POPL NEWLR,@SP          !Both <= M - pop another range!
00CC 8DC4               TEST R                  !Sort stack empty?!
00CE EEAA                 JR NZ,SORT            !  No - continue!
00D0 E30E               JR INSORT               !  Yes - do insertion phase!
                      !Decide subfile direction!
00D2 8BE0           NEWLR0: CP R0,MLEN          !R-J <= M? !
00D4 E204                 JR LE,NEWR            !  Yes - right range done!
00D6 8B10               CP R0,R1                !R-J <= J-L? !
00D8 EA05                 JR GT,STACK1          !  No - left range smaller!
00DA 93FA               PUSH @SP,KJ             !  Yes - right is smaller, stack
00DC 93FC               PUSH @SP,R
00DE A1AC           NEWR:   LD R,KJ             !New range is (L,J-1)!
00E0 ABCF               DEC R,#ESIZE
00E2 E8A0               JR SORT
00E4 93FA           STACK1: PUSH @SP,KJ         !Stack (L,J) range!
00E6 93FD               PUSH @SP,L
00E8 A1AD           NEWLR1: LD L,KJ             !New range is (J+1,R)!
00EA A9DF               INC L,#ESIZE
00EC E89B               JR SORT
                      !Insertion sort phase!
00EE 97FA           INSORT: POP LCNT,@SP        !Saved N, minus 1, becomes !
00F0 ABA0               DEC LCNT                !  outer loop count!
00F2 97FE               POP I,@SP               !Saved "R" becomes I!
00F4 A9E2               INC I,#KEY              !point I at key!
00F6 ABFF               DEC SP,#ESIZE           !Allocate V on stack!
00F8 A1E7           OUTLP:  LD W2,I             !W2 points at KEY(old I)!
00FA ABEF               DEC I,#ESIZE            !I gets I-1!
00FC A1E8               LD W1,I                 !W1 points at KEY(new I)!
00FE BD97               LDK CNT,#KEYLEN         !Count for key comparison!
0100 BA76               CPSIRB @W1,@W2,CNT,NE   !Compare KEY(I),KEY(I+1)!
0102 098E
0104 E71D                 JR ULT,ENDIF          !  KEY(I) < KEY(I+1)!
0106 5CE1               LDM R0,-KEY(I),#ESIZE/2 !V gets REC(I)!
0108 0007
010A FFFD
010C 1CF9               LDM @SP,R0,#ESIZE/2
```

BENCHMARK I-Z8002 (continued)

```
010E 0007
0110 A1FB               LD VKEY1,SP             !point VKEY1 at key!
0112 A9B2               INC VKEY1,#KEY
0114 A1ED               LD J,I                  !J gets I+1!
0116 A9DF               INC J,#ESIZE
0118 A1EC               LD JM1,I                !J-1 gets I!
011A 5CD1       LOOPIN: LDM R0,-KEY(J),#ESIZE/2 !REC(J-1) gets REC(J)!
011C 0007
011E FFFD
0120 5CC9               LDM -KEY(JM1),R0,#ESIZE/2
0122 0007
0124 FFFD
0126 A1DC               LD JM1,J                !J-1 gets J!
0128 A9DF               INC J,#ESIZE            !J gets J+1!
012A A1D7               LD W2,J                 !W2 points at KEY(J)!
012C A1B8               LD W1,VKEY1             !W1 points at KEY(V)!
012E BD97               LDK CNT,#KEYLEN
0130 BA86               CPSIRB @W2,@W1,CNT,NE   !Compare KEY(J),KEY(V)!
0132 097E
0134 E7F2                 JR ULT,LOOPIN         !  KEY(V) > KEY(J)!
0136 1CF1       INSRT:  LDM R0,@SP,#ESIZE/2     !REC(J-1) gets V!
0138 0007
013A 5CC9               LDM -KEY(JM1),R0,#ESIZE/2
013C 0007
013E FFFD
0140 FAA5       ENDIF:  DJNZ LCNT,OUTLP         !Keep looping if more!
0142 A9FF               INC SP,#ESIZE           !Done - give back V allocation!
0144 1CF1               LDM R0,@SP,#15          !Restore all registers!
0146 000E
0148 010F               ADD SP,#30              !Give back register stack space!
014A 001E
014C 9E08               RET
014E            end QUICK
                end QUICKSORT
```

BENCHMARK K-8086

```
                ;                               CARNEGIE-MELLON BENCHMARK 1K3
                ;
                ;                               MATRIX TRANSPOSE FOR 8086
                ;       1 2 3 4 5
                ;       2 2 . . .       XB = X BIT OFFSET       X = X OFFSET
                ;       3 . 3 . .       YB = Y BIT OFFSET       Y = Y OFFSET
                ;       4 . . 4 .
                ;       5 . . . 5       B0 = BIT ORIGIN OF MATRIX (A2)
                ;
                ;   LOGIC FOR SQUARE MATRIX INVERSION:
                ;                           FOR X = 1 TO N - 1
                ;                               Y = X * N
                ;                               XB = X + B0
                ;                               YB = Y + B0
                ;                               WHILE (XB NOT EQUAL YB) DO
                ;                                   SWAP (XB,YB)
                ;                                   XB = XB + N
                ;                                   YB = YB + 1
                ;                                   END
                ;                           END
                ;
                        NAME    BENCHK
                ;
----------      SEGA    SEGMENT AT 010H
                        ASSUME  CS:SEGA,ES:SEGA,DS:SEGA,ES:SEGA
                ;
                ; DEFINITION OF PASSED PARAMETERS:
000C[]          A2      EQU     WORD PTR [BP+12]  ;BIT OFFSET FOR FIRST MATRIX BIT
0008[]          A1      EQU     DWORD PTR [BP+8]  ;ADDRESS FOR FIRST BYTE OF MATRIX
0006[]          N       EQU     WORD PTR [BP+6]   ;MATRIX SIDE SIZE (NXN=TOTAL BITS)
0002[]          RETADR  EQU     DWORD PTR [BP+2]  ;CALLERS RETURN ADDRESS
                ;
                ;   CREATE FRAME POINTER TO ADDRESS PARAMETERS
0000 55                 PUSH    BP                ;SAVE CALLERS BP
0001 8BEC               MOV     BP,SP             ;CREATE FRAME POINTER
                ; SAVE REGISTERS
0003 50                 PUSH    AX                ;SAVE AX
0004 53                 PUSH    BX                ;SAVE BX
0005 51                 PUSH    CX                ;SAVE CX
0006 52                 PUSH    DX                ;SAVE DX
0007 56                 PUSH    SI                ;SAVE SI
0008 57                 PUSH    DI                ;SAVE DI
```

BENCHMARK K-8086 (continued)

```
0009 1E                 PUSH    DS                      ;SAVE DS
000A C54608             LDS     AX,A1                   ;SETUP DS REGISTER WITH MATRIX SEGMENT

                ; RUN X INDEX FROM 1 TO N - 1
000D B80100             MOV     AX,1                    ;START MATRIX COLUMN COUNT (X)
0010 50         LOOPX:  PUSH    AX                      ;SAVE INDEX ON STACK
0011 8BD8               MOV     BX,AX                   ;DUPLICATE X FOR Y CALCULATION
0013 F76606             MUL     N                       ;COMPUTE START OF ROW (Y)
0016 03460C             ADD     AX,A2                   ;CORRECT FOR MATRIX BIT OFFSET (YB)
0019 035E0C             ADD     BX,A2                   ;CORRECT FOR MATRIX BIT OFFSET (XB)

                ; SAVE ROW AND COLUMN BIT POSITIONS
001C 50         NEXTBIT: PUSH   AX                      ;SAVE ROW (YB)
001D 53                 PUSH    BX                      ;SAVE COLUMN (XB)

                ; NOW CALCULATE ABSOLUTE ADDRESSES FOR AXIS INVERSION AND SWAP

                ; COMPUTE ROW PHYSICAL ADDRESS, LOAD BYTE, AND FORM MASK
001E 8AC8               MOV     CL,AL                   ;COPY ROW BIT ADDRESS LOW BYTE
0020 80E107             AND     CL,07H                  ;ISOLATE BIT OFFSET INTO BYTE
0023 8BF0               MOV     SI,AX                   ;STARTING ROW INTO SI
0025 D1EE               SHR     SI,1                    ;FIND
0027 D1EE               SHR     SI,1                    ;  BYTE
0029 D1EE               SHR     SI,1                    ;    ADDRESS
002B 037608             ADD     SI,WORD PTR A1          ;RESOLVE BYTE ADDRESS
002E 8A24               MOV     AH,[SI]                 ;LOAD ROW AXIS BYTE
0030 D2E4               SHL     AH,CL                   ;SET AH HIGH BIT TO DESIRED ONE
0032 80E480             AND     AH,080H                 ;ISOLATE THE BIT
0035 B07F               MOV     AL,7FH                  ;PREPARE TO MAKE ROW MASK BYTE
0037 D2C8               ROR     AL,CL                   ;SET ALL BUT DESIRED BIT ON
0039 8AE9               MOV     CH,CL                   ;SAVE ROW SHIFT VALUE
003B 8AC3               MOV     CL,BL                   ;MOVE IN COLUMN LOW ADDRESS BYTE
003D 80E107             AND     CL,07H                  ;ISOLATE BIT OFFSET
0040 D1EB               SHR     BX,1                    ;ISOLATE THE
0042 D1EB               SHR     BX,1                    ;  COLUMN BIT
0044 D1EB               SHR     BX,1                    ;    BYTE ADDRESS
0046 035E08             ADD     BX,WORD PTR A1          ;RESOLVE BYTE ADDRSS
0049 8A37               MOV     DH,[BX]                 ;LOAD OPPOSITE AXIS COLUMN BYTE
004B D2E6               SHL     DH,CL                   ;SHIFT OPPOSITE TO BIT ZERO
004D 80E680             AND     DH,80H                  ;ISOLATE BIT OF INTEREST
0050 B27F               MOV     DL,7FH                  ;CREATE COLUMN BYTE MASK
0052 D2CA               ROR     DL,CL                   ;SET ALL BUT DESIRED BIT ON
                ; NOW AH = ROW BIT AL = ROW BYTE MASK CH = ROW BYTE SHIFT COUNT
                ;     DH = COL BIT DL = COL BYTE MASK CL = COL BYTE SHIFT COUNT
0054 D2EC               SHR     AH,CL                   ;SHIFT BACK COLUMN'S REPLACMENT BIT
0056 8AC9               MOV     CL,CH                   ;RESTORE ROW'S SHIFT COUNT
0058 D2EE               SHR     DH,CL                   ;SHIFT BACK ROW'S REPLACEMENT BIT
005A 2017               AND     [BX],DL                 ;FORCE OFF COLUMN BYTE BIT
005C 0827               OR      [BX],AH                 ;OR IN OPPOSITE AXIS VALUE
005E 2004               AND     [SI],AL                 ;FORCE OFF ROW BYTE BIT
0060 0834               OR      [SI],DH                 ;OR IN COLUMN BYTE BIT VALUE

                ;  CONTINUE ROW AND COLUMN ADVANCEMENT TILL DIAGONAL REACHED
0062 5B                 POP     BX                      ;RESTORE COLUMN BIT (XB)
0063 58                 POP     AX                      ;RESTORE ROW BIT (YB)
0064 035E06             ADD     BX,N                    ;DOWN TO NEXT COLUMN POSITION
0067 40                 INC     AX                      ;OVER TO NEXT ROW POSITION
0068 3BC3               CMP     AX,BX                   ;REACHED DIAGONAL?
006A 75B0               JNE     NEXTBIT                 ;BRANCH IF MORE RANGE HERE

                ; LOOP BACK UNTIL X REACHES N
006C 58                 POP     AX                      ;RESTORE X INDEX
006D 40                 INC     AX                      ;TO NEXT X VALUE
006E 3B4606             CMP     AX,N                    ;CHECK AGAINTS MATRIX SIZE
0071 7299               JB      LOOPX                   ;CONTINUE IF STILL BELOW

                ; FINISHED
0073 1F                 POP     DS                      ;RESTORE DS
0074 5F                 POP     DI                      ;RESTORE DI
0075 5E                 POP     SI                      ;RESTORE SI
0076 5A                 POP     DX                      ;RESTORE DX
0077 59                 POP     CX                      ;RESTORE CX
0078 5B                 POP     BX                      ;RESTORE BX
0079 58                 POP     AX                      ;RESTORE AX
007A 5D                 POP     BP                      ;RESTORE BP
007B C3                 RET                             ;RETURN TO CALLER

------

                SEGA    ENDS

                        END
```

BENCHMARK K-Z8002

```
MATRIX module

!Example K: Boolean Matrix Transpose!

constant

!procedure arguments !

N       := R0           ! size of N * N Matrix  !
OFF     := R1           !offset of first bit    !
A       := R2           !address of first word  !

!working registers (preserved over call) !

T       := R4           !temp for bits !
TH      := RH4
TL      := RL4
IJBYTE  := RH5          !byte at I,J    !
JIBYTE  := RL5          !byte at J,I    !
 BYTES  := R5           ! combined pair of bytes!
IJBX    := R6           !index of bit at I,J    !
JIBX    := R7           !index of bit at J,I    !
 JBX    := RR6          ! combined J bit ptrs   !
IJWX    := R8           !index of byte at I,J   !
JIWX    := R9           !index of byte at J,I   !
 JWX    := RR8          ! combined J byte ptrs  !
IROW    := RR10         !index of bit A[I,1]    !
ICOL    := RR11         !index of bit A[1,I]    !
 IBX    := RR10         ! combined I bit ptrs   !
ICNT    := RR12         !I loop counter (N-I)   !
MASK    := RR13         !temp for mask bits     !

!stack pointer !

SP      := R15

0000            global BMTRAN procedure entry
0000 030F               SUB     SP,#20          !save registers         !
0002 0014
0004 1CF9               LDM     @SP,R4,#10
0006 0409
                ! FOR I := 2 TO N !
0008 A10C               LD      ICNT,N          !ICNT := N-1            !
000A ABC0               DEC     ICNT
000C A11B               LD      ICOL,OFF        !I := 1. ICOL := OFF!
000E A11A               LD      IROW,OFF        !        IROW := OFF!
                ILOOP:                          !new I value !
0010 810A               ADD     IROW,N          !IROW to next row       !
0012 A9B0               INC     ICOL            !ICOL to next col.      !
                ! FOR J := 1 TO I-1 !
0014 94A6               LDL     JBX,IBX         !set inner loop ptrs!
                JLOOP:                          !new J value !
                ! A[I,J] <-> A[J,I] !
0016 9468               LDL     JWX,JBX         !compute byte addrs     !
0018 B381               SRL     IJWX,#3
001A FFFD
001C B391               SRL     JIWX,#3
001E FFFD
0020 8344               SUB     T,T             !clear temp for mask!
0022 2406               SETB    TH,IJBX         !mask bit for IJ        !
0024 0400
0026 8B89               CP      JIWX,IJWX       !IJ, JI same byte?      !
0028 E60D                 JR      EQ,SAMEIJ     !  yes                  !
002A 8128               ADD     IJWX,A          !  no   !
002C 2085               LDB     IJBYTE,@IJWX    !load A[I,J]    !
002E 8129               ADD     JIWX,A
0030 209D               LDB     JIBYTE,@JIWX    !load A[J,I]    !
0032 2407               SETB    TL,JIBX         !mask bit for JI        !
0034 0C00
0036 A14D               LD      MASK,T          !save mask      !
0038 8754               AND     T,BYTES         !extract bits           !
003A 88C4               XORB    TH,TL           !same (parity even)?!
003C E40C                 JR      PE,NEXTJ      ! same:  done   !
003E 89D5               XOR     BYTES,MASK      !different: flip bits   !
0040 2E9D               LDB     @JIWX,JIBYTE    !store bytes    !
0042 E808               JR      STOREIJ
0044 8128       SAMEIJ: ADD     IJWX,A          ! IJ and JI in same byte !
0046 2085               LDB     IJBYTE,@IJWX    !load A[I,J]    !
0048 2407               SETB    TH,JIBX         !mask bit for JI        !
004A 0400
004C A14D               LD      MASK,T          !save mask      !
004E 8654               ANDB    TH,IJBYTE       !extract bits   !
0050 E402                 JR      PE,NEXTJ      ! same (parity even)!
0052 89D5               XOR     BYTES,MASK      ! different: flip bits  !
                STOREIJ:
0054 2E85               LDB     @IJWX,IJBYTE    !store IJ byte  !
0056 A960       NEXTJ:  INC     IJBX            !move I,J across        !
0058 8107               ADD     JIBX,N          !move J,I down          !
005A 8B76               CP      IJBX,JIBX       !hit diagonal?          !
005C EEDC                 JR      NE,JLOOP      !       no: loop        !
                NEXTI:                          !step outer loop to next I !
005E FCA8               DJNZ    ICNT,ILOOP      !dec & test loop count  !
0060 1CF1               LDM     R4,@SP,#10      !restore registers      !
0062 0409
0064 010F               ADD     R15,#20
0066 0014
0068 9E08               RET                     !exit   !
006A            end BMTRAN

                end MATRIX
```

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PSCQ-2-10.5	9.0-11.0	25	20	0.4	0.7	3.0	1.2	12.95	(5-49)
PSCQ-2-13	12-14	29	25	0.4	0.7	3.0	1.2	12.95	(5-49)
PSCQ-2-14	12-16	30	25	0.3	0.6	3.0	1.8	16.95	(5-49)
PSCQ-2-21.4	20-23	30	25	0.4	0.7	3.0	1.2	12.95	(5-49)
PSCQ-2-50	25-50	30	20	0.3	0.7	3.0	1.5	19.95	(5-49)
PSCQ-2-70	40-70	25	20	0.3	0.7	3.0	1.2	19.95	(5-49)
PSCQ-2-90	55-90	30	20	0.3	0.7	3.0	1.2	19.95	(5-49)
PSCQ-2-120	80-120	25	18	0.3	0.7	3.0	1.5	19.95	(5-49)
PSCQ-2-180	120-180	23	15	0.3	0.7	4.0	1.2	19.95	(5-49)
PSCQ-2-250	150-250	23	18	0.4	0.8	4.0	1.5	19.95	(5-49)
PSCQ-2-400	250-400	22	16	0.4	0.9	4.0	1.5	19.95	(5-49)
PSCQ-2-450	350-450	22	16	0.4	0.9	4.0	1.5	19.95	(5-49)
ZSCQ-2-50	25-50	30	20	0.3	0.7	3.0	1.5	39.95	(4-24)
ZSCQ-2-90	55-90	30	20	0.3	0.7	3.0	1.2	39.95	(4-24)
ZSCQ-2-180	120-180	23	15	0.3	0.7	4.0	1.2	39.95	(4-24)
ZMSCQ-2-50	25-50	30	20	0.3	0.7	3.0	1.5	49.95	(4-24)
ZMSCQ-2-90	55-90	30	20	0.3	0.7	3.0	1.2	49.95	(4-24)
ZMSCQ-2-180	120-180	23	15	0.3	0.7	4.0	1.2	49.95	(4-24)

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Optocoupler saves battery-backed RAMs

Dan Garcia
Pellerin Milnor Corp, Kenner, LA

When backing up a μP system's RAMs, you must ensure that the μP's memories can't be inadvertently selected or undergo a read/write operation when the system's power supply is failing or completely off. This design (**figure**) not only isolates the RAMs from the μP, it further transient-protects the ICs by using an optocoupler as a mains-failure sensor.

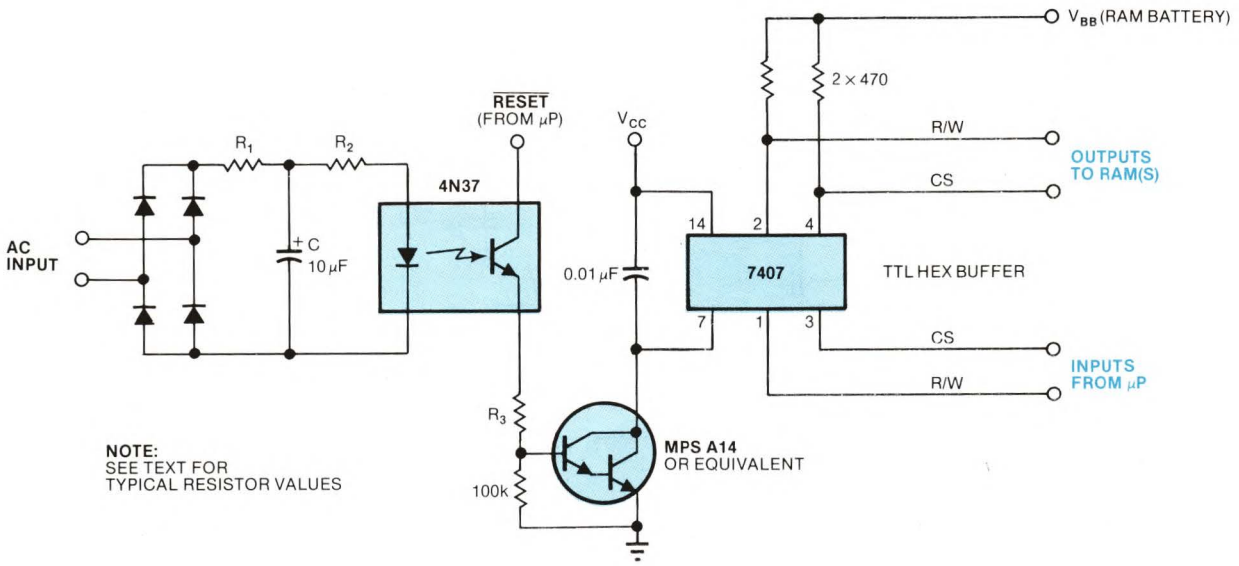
By directly monitoring the mains, this optocoupler provides the additional advantage of allowing you to initiate the RAMs' isolation before the system's supply voltage actually starts failing. The ac line gets rectified and filtered to provide the drive current to the optocoupler's input LED. Thus, so long as an ac line voltage exists, the LED is ON. This condition—via the optocoupler's phototransistor—drives the Darlington device ON and grounds the 7407 TTL-type buffer. And when the buffers are ON, the μP's Chip Select (CS) and Read/Write (R/W) signals get passed to the CMOS RAMs for normal usage.

When an ac-mains power failure occurs, however, the process reverses: The LED's bias disappears—after a period determined by the R_2C time constant—and the TTL buffer disconnects the RAMs from the μP. (Note how the optocoupler's phototransistor also connects to the μP's Reset function.)

The time constants you employ depend upon several factors; the ac input level, optocoupler and Darlington transistor all enter into the picture. For the devices shown in the **figure,** R_1=470Ω, R_2=1 kΩ and R_3=47 kΩ with an ac input voltage of 8V rms. This combination disables the RAMs within 15 msec after an ac input loss.

Only two considerations apply in selecting the active devices. First, the Darlington transistor's β should be very high (1000 in this case) at 50 mA. Second, you should account for the optocoupler's transfer characteristics: A highly sensitive (ie, high-β) device might not shut off as rapidly as a less sensitive unit. Why? The LED's drive current might not drop far enough soon enough to isolate the RAMs before a dropout by the system's dc power supply. Optimize the resistors' values to meet your application's and the devices' requirements. **EDN**

To Vote For This Design, Circle No 452



Disable battery-backed-up CMOS RAMs *so that memory-stored data can't be disrupted after an ac-mains dropout. So long as an ac input exists, the LED (and therefore the buffer) is ON and the μP remains connected to the RAMs.*

Pipeline scheme speeds slow memories

Steven Bennett
Harris Semiconductor, Melbourne, FL

Employ a pipelining technique—normally used to enhance instruction-throughput rate or maximize the usage of bus bandwidth—to permit high-speed operation of low-speed memories in ordinary μC-based designs. Although the scheme shown in the **figure** conforms to an 8085A, you can adapt this approach to other processors, especially those that require fast read-LOW-to-data-valid memories. With the scheme as implemented here, a 2708 EPROM's effective read-access time drops from 120 to 6 nsec.

This improvement arises when the address/data bus (AD_0-AD_7) is demultiplexed by an address latch (IC_1) and fed with the high-order address bits (A_8-A_{15}) to the 16-bit comparator (IC_6 and IC_7). That device compares the new address with the previous address plus one, and the result latches into IC_{10} on the trailing edge of ALE.

If the two addresses are arithmetically equal, nothing happens until the μC issues a Read command, causing a 3-state buffer (IC_8) to gate the already accessed data onto the system's data bus. If, however, an address inequality exists, the Q output of the equality latch (IC_{10}) causes the Wait-state generator (IC_{11}) to parallel-load a hardwired number of states. (This version uses three single-clock states.)

The Wait-state circuit's LOW output extends the Read period, resets the equality latch and causes a 16-bit address counter ($IC_{2\text{-}5}$) to parallel-load a new address. This trick allows you to access noncontiguous memory locations. When the Wait state clocks out, the Read signal again gates data onto the system bus. Thus, by employing a program counter external to the CPU and incrementing this counter with the Read pulse's trailing edge, you can make the memory produce instruction N + 1 while the μC is executing instruction N.

As an example, the 5-MHz 8085A-2 is usually limited to 4-MHz operation when interfaced to 2708 EPROMs using standard methods. With this pipeline scheme, however, you can achieve a 5-MHz operating speed and could reach 6.7 MHz if a faster 8085 becomes available. **EDN**

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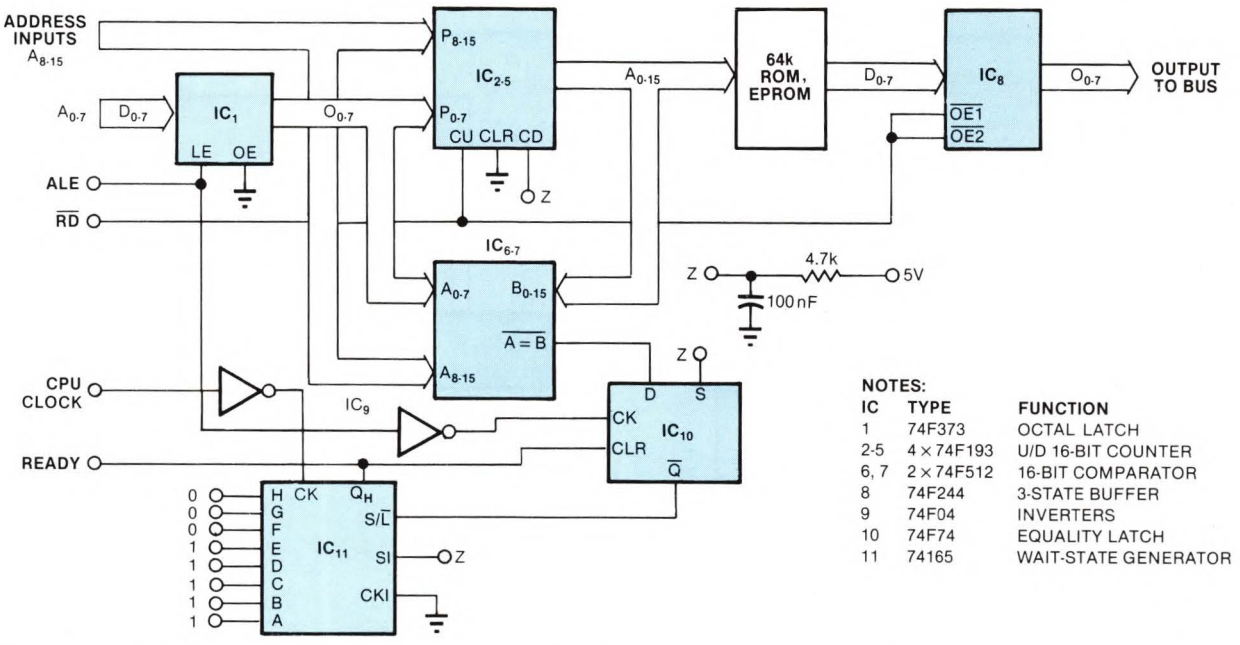

NOTES:

IC	TYPE	FUNCTION
1	74F373	OCTAL LATCH
2-5	4 × 74F193	U/D 16-BIT COUNTER
6, 7	2 × 74F512	16-BIT COMPARATOR
8	74F244	3-STATE BUFFER
9	74F04	INVERTERS
10	74F74	EQUALITY LATCH
11	74165	WAIT-STATE GENERATOR

Slow memories act faster *when the next-to-be-accessed location is pipelined, stored and acquired before the system expects the data. Then, when the system's μC (not shown) issues a Read command (RD), the already available data is gated onto the system data bus.*

Pulser provides variable start, stop times

Marian Stofka
Bratislava, Czechoslovakia

When testing a digital circuit design, you're apt to need a pulse generator whose turn-on and -off times you can delay by a precise and programmable amount. The scheme shown in the **figure** accomplishes this function with a resolution of one part in 256, and it's easily expandable to even higher accuracies.

First, enter the output pulse's start and stop times into two 16-bit MUXs via four rotary switches. Then set both start and stop times independently with switches for coarse (×16) and fine (×1) values in hexadecimal format. (You could also realize a decimal format by using the first nine inputs to the MUXs.)

Thus, for example, to start a pulse at position 56, enter three into the ×16 MUX (giving 48) and eight into the ×1 MUX. Also note how the open-collector inverters isolate the start and stop signals (Q and $\overline{Q}$) from each other, allowing you to set equal or overlapping times without interference.

The output pulse starts (goes HIGH) when both counter-driven MUXs' preset inputs are decoded and the MUXs' outputs trigger the JK flip flop. The counter continues until reaching the appropriate stop code and the flip flop's output goes LOW. (The flip flop's clock-preset requirement is satisfied because both the flip flop and the counter respond equally to the clock's positive-going edge.) Note that the output pulse's change of state is delayed by one clock period relative to the counter's state.

In the configuration shown, the output pulse's start and stop times can be resolved to within $\pi/128$ radians and not overlap. You can increase the setting's resolution by cascading additional MUXs and counters. Additionally, you can employ the flip flop's otherwise unused JK inputs—pulled HIGH in the **figure**—to further control the output pulse. **EDN**

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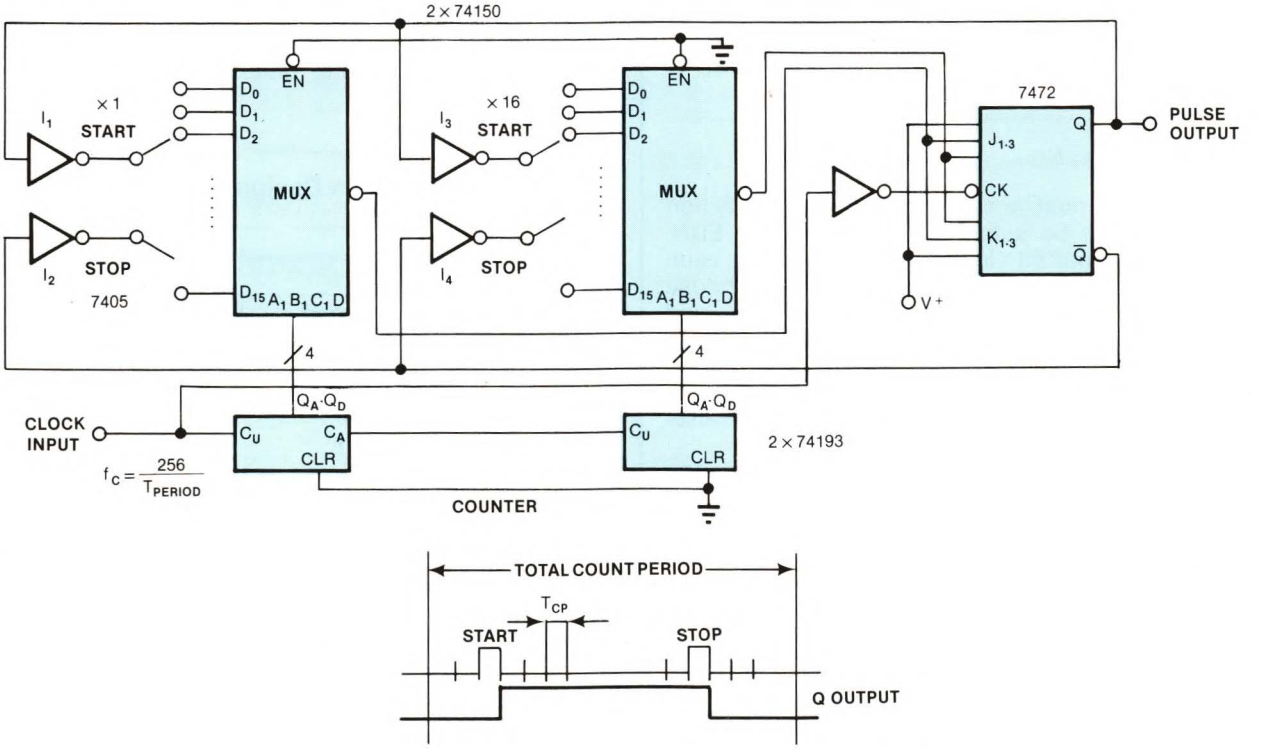

Precisely program a pulse's start and stop times *by setting the values into a pair of MUXs and waiting for the counter to reach the appropriate code. With this design, you can start the output during any of the first 128 time slots and stop it during any of the succeeding 128 positions. Note how the Q output is delayed by one clock period.*

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Single one-shot senses frequency limits

Rudy Schneider
Carco Electronics, Menlo Park, CA

Unlike a previously published Design Idea ("One-shots detect frequency levels," January 21, pg 148), this frequency-discriminator scheme **(figure)** requires only a single one-shot IC and its associated timing components. You set the frequency detector's threshold by selecting a single RC combination:

$$T_2 = 0.45RC.$$

Thus, for example, with R=100 kΩ and C=0.022 μF, T_2=990 μsec and the discriminator's threshold frequency is $1/T_2$=1010 Hz. (Note, however, that the 0.45 factor applies only if you use the indicated LS Series one-shots. If you employ a standard 74122 instead, the factor becomes 0.28.)

You can extend this technique to realize bandpass sensing. Use a double one-shot IC such as a 74LS123 and set up two different time constants: one at each frequency limit. (The 7474 D flip flop is itself a dual unit and thus can be used as is.) Then, by adding the appropriate AND/OR gates to the outputs of both flip flops, you can flag under-, over- and in-band frequencies. **EDN**

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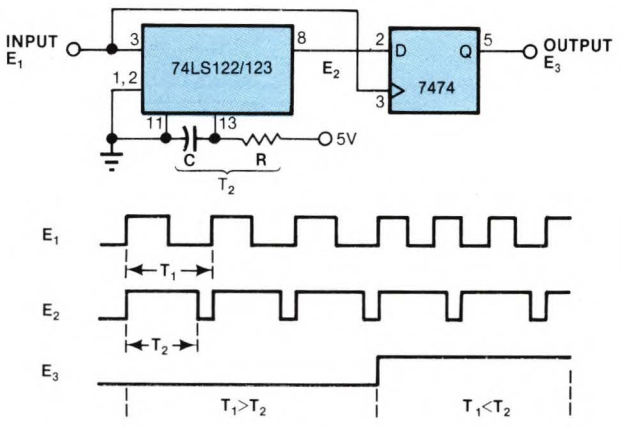


Input-frequency discrimination *occurs when the unknown signal's period (T_1) exceeds that of the retriggerable one-shot (T_2). The output signal (E_3) stays LOW so long as the input frequency is lower than the one-shot's frequency and goes HIGH when the input frequency is HIGH.*

μC Design Techniques

RAM failure analysis speeds test

Herb Perten
Irex Medical Systems, Ramsey, NJ

The memory-testing code presented in Software Note #62 (EDN, February 4, pg 90) runs slowly because it performs all tests serially. But if you analyze the ways RAMs can fail, you can speed the algorithm by using just two WRITE and two READ instructions for each memory location.

RAMs fail in two areas: the data section and the address section. Data errors result in stuck bits. If you write and then read first a ONE and then a ZERO to each bit of every memory location, you'll identify every data error.

Address errors result from stuck bits; they cause access to one location by two or more addresses. If, for example, the least significant address bit were stuck at ZERO, each odd address would map to the even address immediately preceding it.

Because addressing is a binary process, any incorrect address mapping results in the overlay of 2^n locations (n is the byte size) onto another 2^n locations. To catch this error, write a sequence of non-2^n words (such as three different values) to successive memory locations until the RAM is full. Then, when you read the RAM (in the same order), you'll see the error. If the RAM has less than 2^n locations, load each location with its relative address.

The **figure** shows sample coding of this test, written for a Z80. **EDN**

```
;EACH LOCATION OF THE RAM IS LOADED WITH ITS POSITION NUMBER. THEN,
;EACH LOCATION IS READ TO SE IF IT HAS THE CORRECT CONTENTS. NEXT,
;EACH LOCATION IS LOADED WITH THE 1'S COMPLEMENT OF ITS POSITION NUMBER
;AND IS READ FOR CORRECTNESS.  THESE TESTS WILL PICK UP ANY PROBLEMS
;WITH THE ADDRESSING OR DATA SECTIONS OF THE RAM AND ITS BUSSES.

RAMTEST:LD    A,1
        LD    HL,RAM      ;START OF RAM
        LD    B,64        ;SIZE OF RAM
RAMLD:  LD    (HL),A      ;LOAD RAM LOCATION
        INC   A           ;NEXT VALUE
        INC   HL          ;NEXT LOCATION
        DJNZ  RAMLD

        LD    A,1         ;READ THE RAM LOCATIONS FOR CORRECTNESS
        LD    HL,RAM
        LD    B,64
RDRAM:  CP    (HL)        ;IS CONTENTS OF LOCATION OK?
        JR    NZ,RAMNG    ;JP IF NO
        INC   A           ;NEXT VALUE
        INC   HL          ;NEXT LOCATION
        DJNZ  RDRAM

        LD    A,0FEH      ;LOAD RAM WITH 1'S COMPLEMENT OF PREVIOUS TEST
        LD    HL,RAM
        LD    B,64
RAMLDC: LD    (HL),A      ;LOAD RAM LOCATION
        DEC   A
        INC   HL
        DJNZ  RAMLDC

        LD    A,0FEH      ;CHECK CONTENTS
        LD    HL,RAM
        LD    B,64
RDRAMC: CP    (HL)        ;CORRECT VALUE?
        JR    NZ,RAMNG    ;JP IF NOT
        DEC   A
        INC   HL
        DJNZ  RDRAMC

RAMOK:                    ;RAM OK

RAMNG:                    ;RAM BAD

A>
```

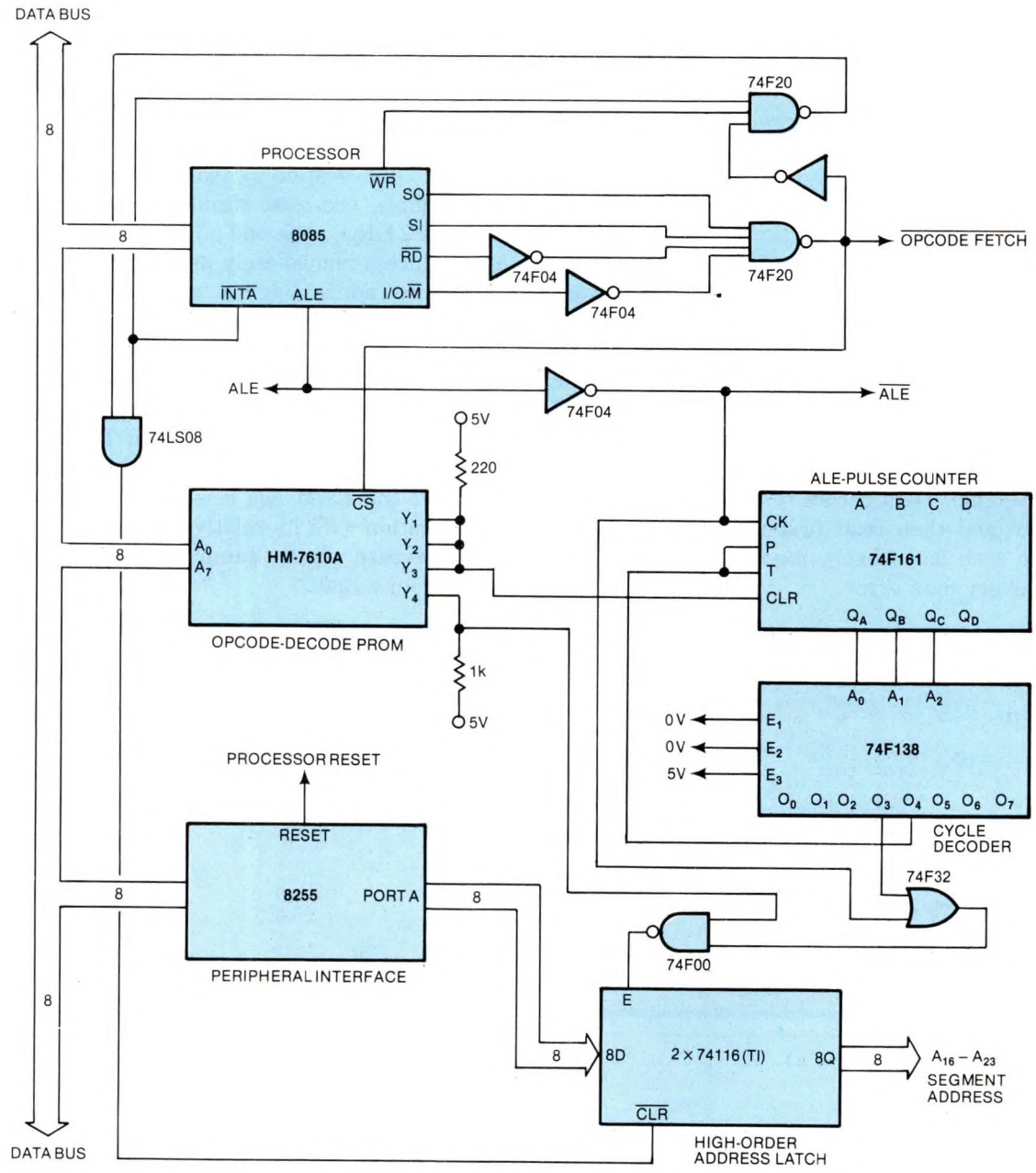
Knowing the two types of RAM failure *allows you to write a simple but thorough memory test.*

Memory controller handles 16M bytes

Steven Bennett
Harris Semiconductor, Melbourne, FL

Is there life after 64k? If your answer is no, you might be considering a costly move to a 16-bit machine. But a less traumatic solution is available. With a handful of TTL devices and a spare I/O port, you can build a memory controller that permits global jumps and calls within a 16M-byte address space. (Don't confuse this technique with the "page-boundary crossing only" afforded by some memory-management ICs.)

The circuit shown in the **figure** implements the technique for the 8085. To use it, you must first program the HM-7610A opcode-decode PROM so that outputs Y_1, Y_2 and Y_3 are LOW when addressed by JUMP unconditional and CALL unconditional opcodes. Similarly, program Y_4 LOW for RETURN unconditional opcodes. The PROM then serves to detect these opcodes on the data bus. It gets strobed



Expand system RAM *on an 8-bit μC with a handful of TTL devices and a spare I/O port.*

by the $\overline{\text{OPCODE FETCH}}$ signal, which is decoded from the 8085 status-bus signals.

When the circuit detects a JUMP/CALL opcode on the data bus, a pulse from the PROM clears the 74F161 ALE-pulse counter, which then increments on the trailing edge of ALE. The resulting count gets decoded by the 74F138 cycle decoder. When the counter has counted three ALE pulses (JUMP/CALL instructions are three bytes long), the μP contains a 16-bit branching address, which it starts outputting on the address bus.

The same ALE pulse that outputs this 16-bit JUMP/CALL address also loads the two 74116 high-order address latches with an 8-bit address

supplied by port A of the 8255 peripheral interface. Therefore, before executing a global JUMP or global CALL instruction, the μP should load the segment address to the appropriate port of the 8255. Executing a JUMP or CALL instruction without first reloading the 8255 merely results in a jump or call within the current segment. (The system supports 256 segments, each 64k bytes long.)

Note that any memory-mapped I/O or RAM accesses must occur within the 64k segment that is currently running the program—otherwise the program becomes lost.

To return to the interrupted or called main program, the μP must merely execute an unconditional RETURN. This command gets detected by the opcode-decode PROM, which issues a pulse on its Y_4 output to reload the high-order address latch from port A of the 8255. The segment number at port A must not get changed by the interrupt-handler subroutine; otherwise, the program will become lost. For this reason, all interrupt handlers and subroutines must reside within the 64k of segment 0.

	PROM ADDRESS	PROM OUTPUTS Y_1	Y_2	Y_3	Y_4
JUMP UNCONDITIONAL	C3	0	0	0	1
CALL UNCONDITIONAL	CD	0	0	0	1
RETURN UNCONDITIONAL	C9	1	1	1	0
ALL OTHER ADDRESSES	XX	1	1	1	1

Program the PROM *as shown so that it works in the* ***figure****'s circuit.*

You can safely use all JUMP, CALL and RETURN instructions except the unconditional forms within a segment, because they will not precipitate a global branch.

You can modify this basic system to suit most applications for a large memory controller. View the system shown as a guideline and develop your own variants. The **table** shows how to program the HM-7610A for the circuit presented. **EDN**

EDN Software Note #73

Access routines increase total system ROM

David M Gardner
Tekno Industries Inc, Bensenville, IL

When your 8-bit μC lacks sufficient ROM address space, you can implement a software-controlled ROM-bank selection mechanism that pages-in a portion of the total system ROM. This process is analogous to loading an overlay from a mass-storage device (such as a floppy disk) but provides much shorter access time because it doesn't involve a mechanical device.

When developing software mechanisms to manage this additional ROM, pay attention to the operating environment and program-interface considerations. Specifically, choose an access method that's easy to use and that, depending on conditions, works in an environment where you can initiate bank selection with interrupts. Additionally, the bank-selection process shouldn't affect the CPU registers.

The code shown in the **figure** meets these requirements for the 8080/85. It is based on the assumption that an always available—or common—

```
ISIS-II 8080/8085 MACRO ASSEMBLER, V4.0     MODULE   PAGE    1

 LOC  OBJ     LINE        SOURCE STATEMENT

                    1 $NOPAGING PAGEWIDTH(80) MACROFILE PRINT(:TO:)
                    2 ;
 27FF               3 RBREG   EQU     27FFH   ;READ/WRITE
                    4 ;       REGISTER FOR ROM BANK SELECTION
                    5 ;
                    6 ;REENTRANT ROM-BANK LINKAGE MACRO -
                    7 ; PLACED ON NON-BANKED SELECTED ROM.
                    8 ; COMPLETELY INVISIBLE TO CALLED & CALLING
                    9 ; PROCEDURES--NO REGISTERS MODIFIED.  NOTE:
                   10 ; REQUIRES 264 8085 T-STATES TO PERFORM LINK
                   11 ; & UNLINK.
                   12 ; 8080/85 1-BYTE RESTART INSTRUCTIONS ARE
                   13 ; USED IN PLACE OF 3-BYTE CALLS TO 'RSTRT1' &
                   14 ; 'RSTRT2' TO REDUCE EACH LINKAGE ROUTINE
                   15 ; TO 9 BYTES EACH.
                   16 ; ACCESS POINTS AND ROUTINES REFERENCED:
                   17 ;       ROUTINE 'CLGRTN' IS CALLING
                   18 ;       ROUTINE 'TARGET' (LOCATED ON
                   19 ;       ROM BANK 'BANK') VIA A LINKAGE
                   20 ;       ROUTINE GENERATED BY MACRO 'LINK' &
                   21 ;       UTILIZED BY A CALL TO 'LINKPT'.
                   22 LINK    MACRO   LINKPT,BANK,TARGET
 -                 23         EXTRN   TARGET
 -                 24         PUBLIC  LINKPT
 -                 25 LINKPT: PUSH    H
 -                 26         MVI     L,BANK
 -                 27 ;; SAVE CURRENT ROM BANK - SELECT NEW ONE
 -                 28         RST     1
 -                 29         XTHL    ;;SAVE CURRENT BANK ON STACK
 -                 30         CALL    TARGET
 -                 31 ;; RESTORE OLD ROM BANK AND RETURN
 -                 32         RST     2
```

Paging ROM into a μC system *provides access to larger amounts of total-system ROM.* *(Listing continues on pg 212)*

```
                    33          ENDM
                    34 ;----------------------------------------
0008                35          ORG     8H
                    36 RSTRT1: ;WRITE (L) TO RBREG TO SELECT 'TARGET'S'
                    37 ; BANK.  RETURN WITH (H)='CLGRTN'S' BANK.
                    38 ; WORD @(SP)=RETURN ADDRESS TO 'LINKPT'
                    39 ; WORD @((SP)+2)= OLD (HL)
                    40 ; WORD @((SP)+4)=RETURN ADDRESS TO 'CLGRTN'
0008 F5             41          PUSH    PSW         ;SAVE A & F
0009 3AFF27         42          LDA     RBREG       ;CURRENT BANK
000C 67             43          MOV     H,A
000D C34000         44          JMP     RST1        ;CONTINUED
                    45 ;----------------------------------------
0010                46          ORG     10H
                    47 RSTRT2: ;RESTORE 'CLGRTN'S' BANK & RETURN
                    48 ; WORD @(SP)='LINKPT' RETURN ADDRESS
                    49 ; BYTE @((SP)+3)='CLGRTN'S' ROM BANK
                    50 ; WORD @((SP)+4)='CLGRTN'S' RETURN ADDRESS
0010 E3             51          XTHL        ;DUMP 'LINKPT' RET
0011 E1             52          POP     H
0012 E3             53          XTHL        ;(H)=OLD PAGE
0013 F5             54          PUSH    PSW         ;SAVE A & F
0014 7C             55          MOV     A,H
0015 C34600         56          JMP     RST2        ;CONTINUED
                    57 ;----------------------------------------
0040                58          ORG     40H
                    59 RST1:    ;RESTART 1 CONTINUED
0040 7D             60          MOV     A,L
0041 32FF27         61          STA     RBREG       ;SELECT NEW BANK
0044 F1             62          POP     PSW         ;RESTORE
0045 C9             63          RET
                    64 ;
                    65 RST2:    ;RESTART 2 CONTINUED
0046 32FF27         66          STA     RBREG
0049 F1             67          POP     PSW         ;RESTORE
004A E1             68          POP     H           ;RESTORE (HL)
004B C9             69          RET
                    70          END

PUBLIC SYMBOLS

EXTERNAL SYMBOLS

USER SYMBOLS
LINK    + 0000    RBREG  A 27FF    RST1   A 0040    RST2   A 0046
RSTRT1 A 0008    RSTRT2 A 0010

ASSEMBLY COMPLETE,  NO ERRORS
```

block of ROM exists to service at least the interrupt vectors. For each routine in banked ROM, the VECTOR macro generates nine bytes of code. (Restarts one and two are used to save space.)

The code is easy to use; accessing the TARGET routine requires only a call to the proper LINKPT. Because the call and its associated return modify no registers and are themselves re-entrant, the code is invisible to both the called and calling routines.

One final note: Because this macro's execution time is relatively long, you should locate short, frequently used utilities and fast-response interrupt handlers in the common ROM. **EDN**

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AT-6	6	±0.3dB	DC-1500	0.6dB	0.8dB	1.3:1	1.5:1	1W
AT-10	10	±0.3dB	DC-1500	0.6dB	0.8dB	1.3:1	1.5:1	1W
AT-20	20	±0.3dB	DC-1500	0.6dB	0.8dB	1.3:1	1.5:1	1W

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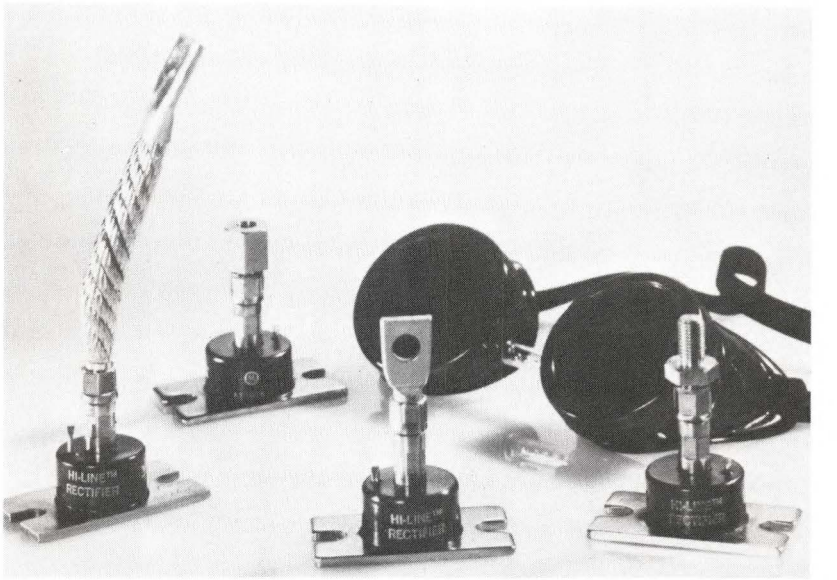

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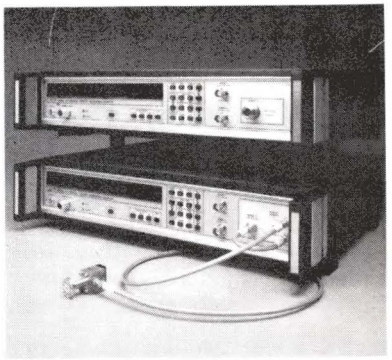

Source-locking capabilities *on Models 575 and 578 microwave frequency counters allow you to control swept sources to achieve synthesizer-like stability.*

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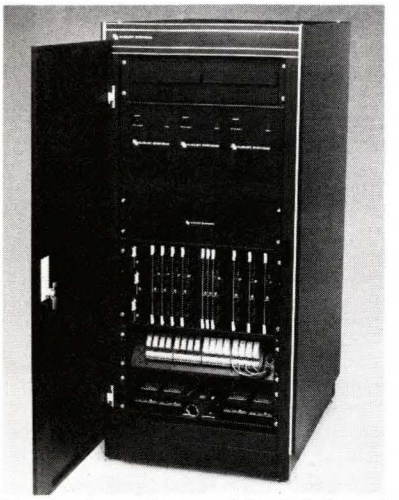
The computer comprises three control-computer modules (CCMs) based on the 16-bit 8086 μP, process-interface modules and termination modules. Optional peripherals include diskette drives and CRT terminals.

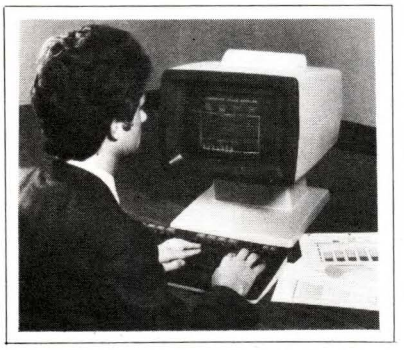
A Real-Time Task Scheduler (RTTS) operating system performs all software fault-tolerance functions and provides utilities and drivers. Control applications software is developed as it is with a conventional control computer using a μC development system.



Employing advanced fault-tolerant technology *to provide nonstop, error-free operation during a hardware failure, the Series 300 Can't Fail computer serves real-time control and monitoring applications where a failure could cause serious or catastrophic results.*

The CCMs provide 23k bytes of memory, expandable to 1M bytes, in any mix of RAM, ROM and EPROM. Diskette-drive and CRT-terminal interfaces come standard. Additionally, the CCMs permit expansion using available Multibus-compatible interface, communications and controller boards. From <$50,000.

August Systems Inc, 2757 19th St Southeast, Salem, OR 97302. Phone (800) 547-9168.
Circle No 150



GRAPHICS TERMINAL. The HP2623A features 512×390-dot screen resolution and can draw vectors at rates to 9600 baud. Graphic and alphanumeric memories are independent and prevent system messages from interfering with the graphics application. The unit utilizes its manufacturer's DSG/3000 and GRAPHICS/1000-II business-oriented graphics software and is also compatible with other software packages, including Tektronix's PLOT 10 for 4010/12 display terminals. Terminal, $3750; optional integral thermal printer, $1210; $105 for line-drawing character set or national-language and keyboard options. Delivery, 12 wks ARO. **Hewlett-Packard Co,** 1507 Page Mill Rd, Palo Alto, CA. 94304. Phone local office.
Circle No 151

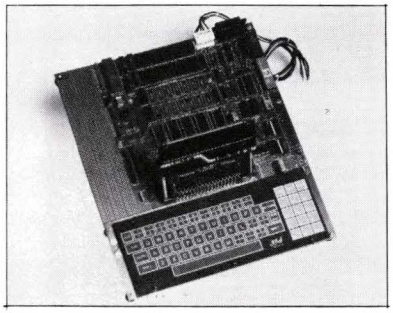
SOFTWARE. A high-level procedure-oriented system-implementation language for the Z8000 μP, Z8000 PLZ/SYS is designed for construction of operating systems, compilers, database-management systems and other system software for the segmented Z8001 and unsegmented Z8002. It combines elements of the PASCAL, ALGOL, PL/1 and C languages, permitting expression of algorithms in a high-level, structured fashion. Programs written for the Z80 in Z80 PLZ/SYS can be easily transported to the Z8000 via Z8000 PLZ/SYS. $700. **Zilog Inc,** 10340 Bubb Rd, Cupertino, CA 95014. Phone (408) 446-4666. **Circle No 152**

ASSEMBLY-CODE TRANSLATOR. The XLT86 program translator reads an assembly-language program compatible with ASM, MAC or RMAC assembler format and produces an output file of 8086-assembly-language statements acceptable to the ASM-86 assembler. Unlike code converters that translate one 8080 instruction into as many as 10 8086 instructions, the software performs extensive data-flow analysis to determine register usage throughout the original program. The information collected through analysis is then used during program translation to eliminate unnecessary flag save and restore operations. Programs the unit translates run on CP/M-86 and MP/M-86 16-bit single- and multiuser operating systems. CP/M version, $150; VAX version, $8000. **Digital Research,** Box 579, Pacific Grove, CA 93950. Phone (408) 649-3896. TWX 910-360 5001.
Circle No 153

Evaluation/test system-design kit aids microcontroller implementation

Taking approximately 5 to 10 hrs to assemble and test, the SDK-51 system-design kit contains hardware and software for building an evaluation/prototyping tool for its manufacturer's MCS-51 microcontroller family.

A standard keyboard and display provide full user access to all system capabilities. The keyboard interface features a 51-character ASCII subset, typewriter format and a 12-key matrix, and the LED panel displays as many as 24 alphanumeric characters. The kit supplies 1k bytes of RAM and includes provision for an additional 15k bytes of on-board RAM as well as 8k of ROM.



A monitor package, single-line assembler/disassembler, ASCII keyboard and LED display *combine in the SDK-51, a system-design kit for component evaluation and design testing.*

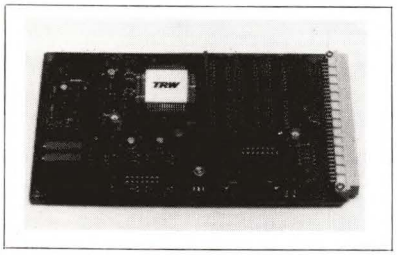
A monitor package furnishes system utilities such as command interpretation, user program debugging and interface control. Users enter software code with a subset of the MCS-51 assembler.

A single-line assembler permits program entry in assembly language from the keyboard, and a disassembler permits review of mnemonic instructions during system interrogation. Its single-step capability proves useful in code verification and debugging, as do hardware breakpoints. $950. Delivery, 4 to 6 wks ARO.

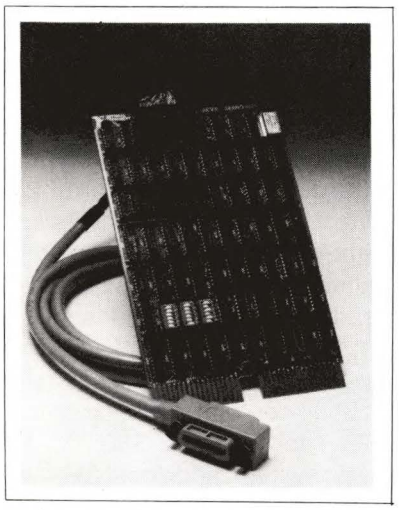
Intel Corp, 5200 NE Elam Young Parkway, Hillsboro, OR 97123. Phone (503) 640-7792.
Circle No 144

New Products

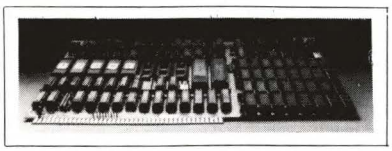
COMPUTER-SYSTEM SUBASSEMBLIES



A/D-CONVERTER BOARD. The TDC1025E1C 8-bit unit accepts analog input signals with a 20-MHz bandwidth and supplies the corresponding 8-bit digital output. Both the Convert signal and 8-bit binary outputs are buffered single-ended ECL. The 100×160-mm board obtains its 75M-samples/sec performance from a monolithic triple-diffused flash A/D converter. Full-scale analog input ranges of 1 to 10V are selectable by means of on-board resistors, providing input impedances of 50Ω to 1 kΩ. Offset adjustments are provided for unipolar or bipolar inputs. $1360. **TRW/LSI Products,** Box 2472, La Jolla, CA 92038. Phone (714) 578-5990. TLX 697957. **Circle No 145**



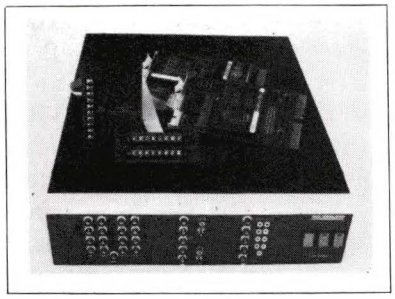
DMA INTERFACE. The GPIB11V-2 DMA interface between the IEEE-488 bus and the DEC LSI-11 Q-bus provides data-transfer speeds to 250k bytes/sec. Permitting 16-, 18- or 22-bit addressing on the LSI-11 bus, it furnishes all GPIB functions, including extended talker, extended listener and controller. The interface allows the LSI-11 to connect to as many as 14 GPIB-compatible devices and works in a single- or multiple-controller environment with a programmable system-controller feature. Support software includes drivers, utilities and an interactive control program. The standard software package supports BASIC-, FORTRAN- and MACRO-callable subroutines under RT-11 and RSX-11 operating systems. $1495, including interface card, software, a 4m cable with GPIB connector and documentation. **National Instruments,** 8900 Shoal Creek Blvd, Austin, TX 78758. Phone (512) 454-3526. **Circle No 146**

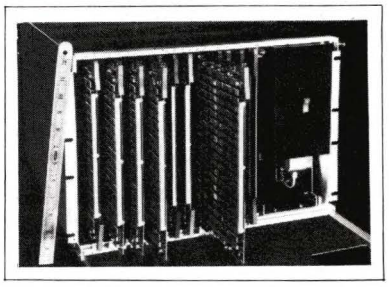


GRAPHICS VIDEO BOARD. A single-board Multibus-compatible unit that provides 512×512-pixel resolution and permits the mixing of graphics and alphanumerics, the M-2000 video-controller board features full 20-bit addressing capability. An on-board high-speed (5-MHz) μP controls all board functions, including scrolling, drawing lines and boxes, displaying intermixed text and graphics and setting the on-board time and date clock. Also provided are software selection of three character sizes and point-by-point dot display. $995. **Metacomp Inc,** 7290 Engineer Rd, Suite F, San Diego, CA 92111. Phone (714) 278-0635. **Circle No 147**

COMPUTER-SYSTEM SUBASSEMBLIES

ANALOG INPUT SYSTEM. The wide-range isolated Model LDT2765 features four differential input channels that withstand ±250V common-mode voltages and support a 60-Hz CMRR of 126 dB. It functions with the manufacturer's Lab-Datax LSI-11-based data-acquisition systems. An optional panel-mounted ambient-temperature compensation circuit provides thermocouple cold-junction-compensation capabilities. The companion LDT2775 isolated input expander features eight isolated differential input channels. As many as seven expanders can augment each LDT2765 for a total 60 isolated channels. LDT2765, $965; LDT2775, $720, including front panels. **Data Translation,** 100 Locke Dr, Marlboro, MA 01752. Phone (617) 481-3700. **Circle No 148**





MEMORY SYSTEM. Using array boards mounting 288 64k dynamic-RAM chips, MMS3000 accommodates as much as 32M bytes of memory. The standard package includes a card cage, power-supply module, interface card, mother board, address-control card, error-correction card, two terminator boards, interconnect cables and 2M bytes of RAM. A 64M-bytes/sec data-transfer rate can be established through use of parallel read with sequential addressing. At the memory-bus level, the system exhibits an access time of 350 nsec with error correction, 275 nsec without. $30,700 for basic system; additional 2M-byte card, $16,800. **Motorola Semiconductor Products Inc,** 3501 Ed Bluestein Blvd, Austin, TX 78721. Phone (512) 928-6776. **Circle No 149**

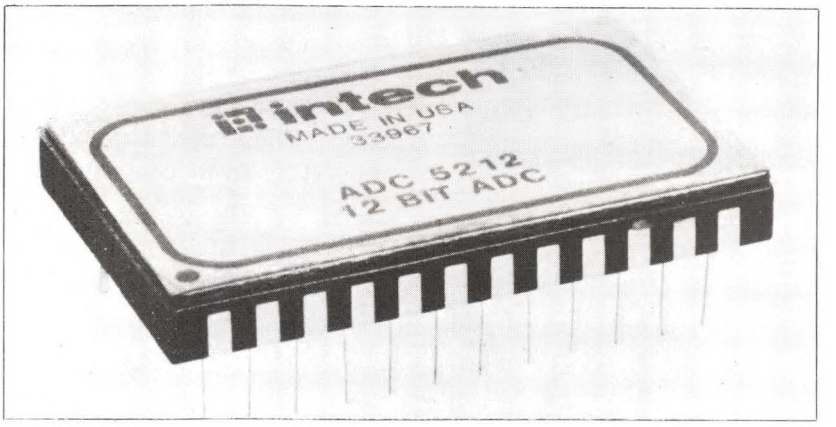
ADC achieves high-speed conversion

Operating at a 1-MHz clock rate, the ADC-5212 resolves an analog input (±10V max) to a corresponding digital output in just 13 μsec. A 12-bit successive-approximation hybrid design, it limits nonlinearity to ±½ LSB.

At 25°C, converter absolute-accuracy error specs at ±0.05% FSR and is guaranteed not to exceed ±10 ppm/°C over temperature. Two versions are available: a commercial type that operates over 0 to 70°C and a military model, processed to MIL-STD-883 method 5088.

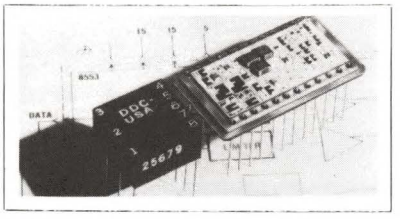
Pin compatible with similar parts from Micro Networks and Analog Devices, the 5212 is housed in an industry-standard 24-pin DIP and operates from 5 and ±15V supplies.

$190 to $485. Delivery (production qty), stock to 8 wks.



Aimed at high-speed applications, *the ADC-5212 A/D converter features a 13-μsec conversion time. It provides a ±0.05% absolute-accuracy error at 25°C and comes in commercial and military versions.*

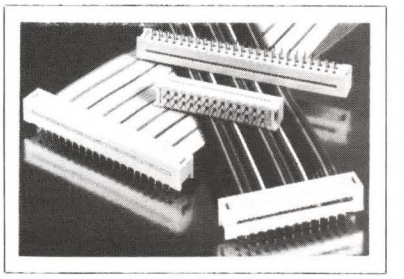
Intech Inc/Microcircuits Div, 2270 Martin Ave, Santa Clara, CA 95050. Phone (408) 727-0500. **Circle No 154**



HYBRID TRANSCEIVER. For use in automatic test equipment requiring a variable transmitter output, the BUS-8559 is housed in a 1.4×0.8×0.2-in. 24-pin DIP and weighs 0.4 oz. Meeting MIL-STD-1553A and -B, it operates over −55 to +125°C and from ±12 to ±15V and ±5V power supplies. Its transmitter section accepts biphase TTL data at the input and produces a 0 to 27V (nominal) p-p differential signal across a 145Ω load. The module can be coupled to the data bus with the manufacturer's BUS-25679 transformer. $325. Delivery, 4 to 8 wks ARO. **ILC Data Device Corp,** 105 Wilbur Pl, Bohemia, NY 11716. Phone (516) 567-5600. TWX 510-228-7324. **Circle No 155**

CONNECTORS. Designed to terminate 0.050 - in. - center round-conductor flat cable and mate with 0.062-in.-thick pc boards with pads on 0.1-in. centers, Edge-Card II connectors come in 11 sizes with 10 to 64 positions. Bifurcated contacts permit redundant connection to the pc board, and 0.013-in.-thick beryllium-copper contacts maintain spring characteristics and high normal force after repeated insertion and withdrawal. The units come in three styles: with mounting ears, with mounting slots and without mounting ears. **Du Pont Berg Electronics Div,** Rte 83, New Cumberland, PA 17070. Phone (717) 780-2044.
Circle No 156

CONNECTOR. This socket-header eliminator (SHE) connector features a footprint identical to that of standard 0.1×0.1-in. headers and suits applications not requiring the mateability benefits of headers and sockets.

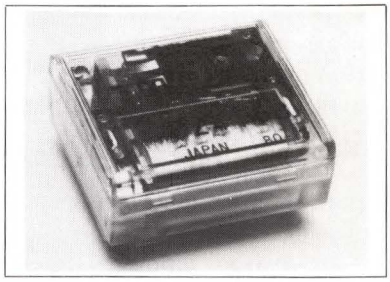


For 50-μm flat ribbon cable, it comes in nine sizes with 10 to 60 contacts. Positive connection between the U contact and 28-gauge stranded or 30-gauge solid round conductors is ensured by a double-action slot design utilizing two cutting surfaces. Insulation surviving the first cut is displaced by the second cutting edge, with a gas-tight connection formed by subsequent abrasion of the conductor by the slot. Gold-over-nickel plated contact areas are provided. $4.12 for 34-position unit. **Belden Corp,** 2000 S Batavia Ave, Geneva, IL 60134. Phone (312) 565-1200.
Circle No 157

New Products

COMPONENTS & PACKAGING

DIRECTIONAL COUPLERS. For use as taps or feeds in multiterminal local networks, multiplexing and other applications, these 3- and 4-port optical directional couplers accommodate digital and analog transmission. They permit full-duplex operation over one fiber and exhibit low insertion loss, high directivity and passive operation, according to the manufacturer. Available with Corning SDF fiber and a variety of graded-index fibers, the $1\times4\frac{1}{4}\times\frac{3}{8}$-in. units feature a broad range of splitting ratios and can operate at all standard transmission wavelengths. <$200 (OEM qty). **Phalo Optical Systems Div,** 9240 Deering Ave, Chatsworth, CA 91311. Phone (213) 998-3177. **Circle No 158**



LATCHING RELAY. Featuring bifurcated cross-bar contacts and a card-lift-off operating system, the polarized Model BZB incorporates flux-free construction and dual-in-line pitch terminals. Equipped with gold-overlay silver-palladium stationary contacts and silver-palladium movable ones, it has a life expectancy of five million mechanical operations and one million electrical operations. Contact arrangements are 4pdt (B-M), dpdt (B-M) and dpdt (M-B). Maximum current flow equals 2A; at resistive load the maximum switching power equals 50W; maximum switching voltage, 60V dc; and maximum switching current, 2A dc. Designed for direct pc-board mounting on a 0.1-in. grid spacing, the relay operates over −30 to +80°C. 4pdt unit, $7.75 (1000). Delivery, 8 to 10 wks ARO. **ITT Components,** Box 2197, Santa Ana, CA 92707. Phone (714) 751-3900.
Circle No 159

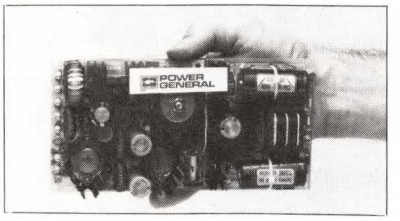
Quad-output 100W switcher series features small size, low cost

Claimed the smallest, lightest and least expensive 100W 4-output switchers available, Series 4100 supplies suit μC-system, CRT-terminal, disk-drive and modem applications.

Mounted on a pc board, the switchers furnish rated output over a 0 to 40°C ambient-temperature range with 2%/°C derating to 71°C.

The four models in the series provide the following ratings:

- +5V at 10A, ±12V at 1.5A and −5V at 1A
- +5V at 10A, ±15V at 1.5A and −5V at 1A
- +5V at 10A, ±12V at 2A and −5V at 1A
- +5V at 10A, ±15V at 2A and −5V at 1A.



Small size (4×8×1.7 in.) and light weight (24 oz) *highlight 4100 Series switchers. The $159 4-output supplies deliver 100W outputs from 85 to 130 or 170 to 250V ac inputs.*

Pin-strappable inputs allow the supplies to operate on 85 to 130 or 170 to 250V (47 to 440 Hz) voltage ranges. And Schottky rectifiers combined with a half-bridge configuration give them 70% min efficiency and ripple and noise specs of 50 mV p-p, 15 mV rms.

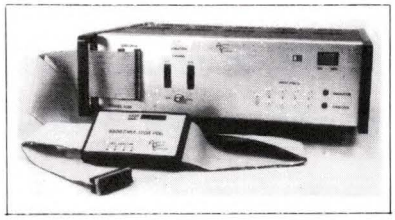
Other specs include ±0.1% line regulation, load regulation of ±0.2% for the primary output and ±1% for the other outputs, a 0.02%/°C TC, and standard current limiting, soft starting, 15A max input surge current and convection cooling.

The 24-oz supplies measure 4×8×1.7 in. and furnish a 30,000-hr min MTBF, per MIL-HDBK-217B. $159.

Power General, 152 Will Dr, Canton, MA 02021. Phone (617) 828-6216. **Circle No 128**

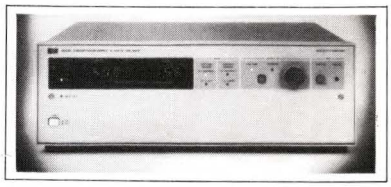
INSTRUMENTATION & POWER SOURCES

EMULATOR/LOGIC ANALYZER. Model 4009 combines features of a real-time 68B09/E emulator and a 12/20-MHz, 18-channel logic analyzer. Its menu-oriented display allows a



user to disassemble a program in mnemonic form. A terminal or host computer can control the unit through three general-purpose communication ports; two RS-232C communication cards and one cassette interface are provided. GPIB and Centronics printer-interface communication cards are optional. Other features include four break events (40-bit-wide trigger conditions) and a real-time, 2k×56-bit trace memory, configured so that the operator can examine the trace while in emulation. $4995. **Advanced Digital Technology Inc,** 13400 Northrup Way, Bldg 15, Bellevue, WA 98005. Phone (206) 643-2382.

Circle No 129

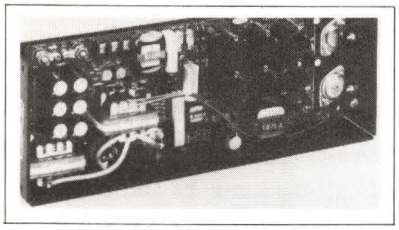


SYSTEM POWER SUPPLY. An IEEE-488 dc power supply with a bidirectional interface and autoranging for systems applications, HP 6034A combines an internal μP-based HP-IB programmer with FET switching technology to provide laboratory-grade performance specs and autoranging capability. Its firmware permits programming of the output voltage and current directly in volts and amps with 12-bit resolution. The unit also provides remote output voltage and current metering over the bus with 15-mV and 2.5-mA resolution, respectively. An overvoltage-protection circuit can be directly programmed in volts with 8-bit resolution. Other features include built-in diagnostics and a removable front panel for access to the calibration board. $2700. **Hewlett-Packard Co,** 1507 Page Mill Rd, Palo Alto, CA 94304. Phone local office.

Circle No 130

New Products

INSTRUMENTATION & POWER SOURCES



250W SWITCHERS. 5F Series open-frame dc units feature a dual input range of 90 to 132 and 180 to 264V ac and 16-msec input carryover. Ripple and noise equal 40 and 75 mV p-p max typ, respectively, at full load. Line and load regulation spec at 0.15% for all outputs except the 24V output of the 5-output Model 5FXMP, where they equal 8%. Overvoltage protection, foldback current limiting, remote sensing, output-voltage adjustment, enable/inhibit function and LED status indicators for each dc output are provided. From $249 for single-output units; from $379 for multiple-output models. Delivery, 6 to 8 wks ARO. **Sierracin/Power Systems,** 20500 Plummer St, Chatsworth, CA 91311. Phone (213) 998-9873. **Circle No 131**

IN-CIRCUIT TEST SYSTEM. Including a high-speed Nova 4X minicomputer with 128k words of MOS memory and an enhanced test executive, Series 30/303S test system provides automatic test-program-generation software that offers near-total-fault-detection production programs. Features include advanced test algorithms, an LSI debugger, QA-check program and pin-to-node identifier. The software package includes the PIN-CHECK program, which verifies complete interconnection between the test fixture and the board under test. It is executed before each board test begins, identifies pins not contacting the board and halts the test sequence to permit corrections. Typical system, $180,000; foreground/background programming option, $4100. **Fairchild Corp Subassembly Test Systems,** 299 Old Niskayuna Rd, Latham, NY 12110. Phone (415) 962-3533. **Circle No 132**

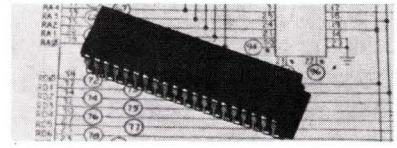
POWER ANALYZER. Model 636 multifunction power analyzer measures ac voltage, current and time. Using those measurements, it can calculate and display watts, watt-hours, VARs, VAR-hours, volt-amps, phase angle, power factor and frequency. Features include high resolution and true-rms measurements with crest factors of 3 for current and 2 for voltage. $5670. Delivery, 6 to 8 wks ARO. **RFL Industries,** Powerville Rd, Boonton, NJ 07005. Phone (201) 334-3100. **Circle No 133**

OPEN-FRAME SUPPLIES. With a shielded transformer, socketed semiconductors, dual ac input, barrier-block terminals and an MTBF to 100,000 hrs, HVQ Series single-output linear units achieve current ratings to 3A. Input ratings equal 105 to 125 or 210 to 250V, 47 to 440 Hz; outputs include 5V/3A, 12V/1.7A, 15V/1.5A and 24V/1.2A, adjustable ±5%. Line and load regulation equal 0.1%. Ripple and noise spec at 1.0 mV rms, 5 mV p-p. Remote sensing and reverse voltage protection come standard. $21. **Deltron Inc,** Box 1369, North Wales, PA 19454. Phone (215) 699-9261. TWX 510-661-8061. **Circle No 134**

Low-cost speech-synthesizer IC speaks in as many as five languages

You can now give your product some "say so" in its usage by incorporating a Custom ROM Controller (CRC) voice-synthesizer IC into its design. It could then speak in an assortment of English vocabularies, including one for calculators (24 words) plus standard (64 words), ASCII (64 words) and 119-word basic sets. The calculator voice is also available in Arabic, French, German and Japanese.

When the CRC combines with the vocabulary RAM, a simple passive filter and an op amp, the resulting speech is an emotionless, nonhuman-like robotic sound.



Voice output *occurs when the Custom ROM Controller (CRC) IC decodes a 6-bit data word, fetches the digital equivalent from memory and reconstructs the desired word(s). The resulting robotic-sounding words are easily concatenated without conflicting inflections.*

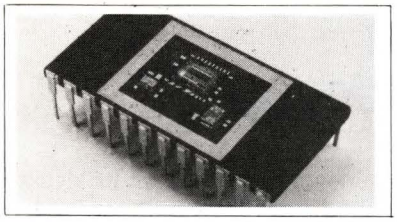
The CRC performs two functions: It's a speech synthesizer and a speech-data controller. In a typical application, you input a 6-bit data word to it. It then retrieves the corresponding word(s) from memory and reconstructs the message.

Based on the techniques developed by Dr Forrest Mozer, algorithms convert the original human speech into digital data to yield approximately 1k bits per speech-second. Thus, because the CRC can directly address up to 32k-byte-wide ROMs, you can generate approximately 30 sec max of speech (64 sec max with extra decoding).

The CRC voice-synthesizer IC costs $65 at the sample level or approximately $20 (5000).

Telesensory Speech Systems, 3408 Hillview Ave, Palo Alto, CA 94304. Phone (415) 856-8255. **Circle No 125**

ICs & SEMICONDUCTORS



12-BIT DAC. A self-contained hybrid unit, DAC 1280A provides feedback resistors, output op amp and reference on three dice. Output current equals 0 to 2 mA, and settling time to full-scale accuracy equals 300 nsec in Current mode and 2.5 μsec in Voltage mode. Power dissipation in either mode specs at 500 mW. Internally supplied resistor options provide low-drift bipolar output-voltage ranges of ±2.5, ±5 and ±10V and unipolar ranges of 0 to 5 or 0 to 10V. $22.95 (100) in 24-pin DIP. **National Semiconductor,** 2900 Semiconductor Dr, Santa Clara, CA 95051. Phone (408) 737-5000. TWX 910-339-9240. **Circle No 126**

MONOLITHIC PWM. A monolithic pulse-width modulator for dc motor control, the SG1731 provides bidirectional pulse-train output in response to the magnitude and polarity of analog input signals. It features externally programmable deadbands to control power consumption, stiffness and stability and an internal amp. Its triangle-waveform oscillator requires only one external capacitor to set frequency as high as 350 kHz; a summing/scaling network permits level-shifting the triangle waveform for pulse-width modulation. Supply voltage to the output drivers can come from dual positive and negative supplies or from single-ended ones. Output voltage equals ±35V; supply-voltage range specs at ±3.5 to ±15V. The SG1731 operates over −55 to +125°C; the SG2731, −25 to +85°C; the SG3731, 0 to 70°C. SG3731J, $7 (1000) in a 16-pin Cerdip. Delivery, 10 wks ARO. **Silicon General Inc,** 11651 Monarch St, Garden Grove, CA 92641. Phone (714) 892-5531. TLX 692411. TWX: 910-596-1804. **Circle No 127**

A Question of Law

Be sure of a device's patent status before incorporating the part in a design

David Pressman, Attorney at Law
San Francisco, CA

If you want to incorporate a competitor's circuit into your design, can you do so without being sued? How can you determine a product's patent status and whether you can copy the product without liability?

That the circuit or device doesn't appear to be patented provides no guarantee of safety: It could be the subject of a pending—and secret—patent application. However, several rules and guidelines can help you determine a device's patent status and if it's relatively safe to manufacture. Thus, this second article in a 3-part series on aspects of patent law focuses on the procedures involved in obtaining clearance for copying a manufactured product.

First, remember that patent professionals do not consider it immoral or unethical to copy any circuit or device not patented or on which the patent has expired. The patent laws' purpose is to disseminate new developements to the public by inducing inventors to reveal the details of their inventions with the promise of a limited-term monopoly. Once a patent expires, therefore, the public is free to use the patent specifications to make and use formerly patented devices.

Thus, if the circuit or device you're interested in is not currently patented, the patent probably has expired and it's in the public domain. And by copying it you're doing just what the law intended: using and building upon the knowledge disseminated by a patented invention.

Unpatented device open to copying

Even if the circuit was never patented, you're still within your rights in copying it. By producing a commercial product without patenting it, the inventor (or the inventor's company) has, in effect, said: "I don't want a monopoly on this product; anyone interested in it is free to use it, provided that he takes the trouble to reverse-engineer the device."

Next, remember that the law prohibits you from copying any nonfunctional aspects of an unpatented product, such as its novel shape, color or design. These aspects could be considered a trademark or the equivalent of a trademark. And nonfunctional features not serving as a trademark are often protected under the law of unfair competition (EDN, July 22, pg 390).

The law in this area, though, is currently in a state of flux, so it's impossible to offer definitive rules or guidelines. Generally, however, you'll be safe if you make your equipment's exterior design (shape, color and other nonfunctional features) sufficiently different so it won't be confused with your competitors'.

You can see that although it's morally and legally permissible to copy an unpatented device in public use, determining a product's patent status is not always easy.

The first step is to examine the circuit's or device's enclosure, instruction manual, advertising literature and package to see if they contain any indication of patent status. (A patent owner or applicant, though, has no legal obligation to label a product with this information.) In this regard, every invention has three possible patent statuses: patent pending, patent in force and patent expired.

"Patent pending" confers no rights

If the circuit is marked "patent pending" or "patent applied for," it means that a patent application has been filed in the Patent and Trademark Office but no patent has yet been issued (or the application hasn't yet been abandoned if the device is found unpatentable). But note that a patent application and patent-pending status confer no rights; *technically* you're free to make and sell any invention whose patent is pending. You'd be unwise to do so, though, because a patent might eventually be issued and you'd then infringe it.

You're not relegated, however, to copying at your peril with a patent-pending invention. If you're interested enough in it, you can make a Patent Office patentability search and obtain a patent attorney's opinion to determine whether the invention is patentable. If so, its owner will likely obtain a patent; in this case, then, don't waste your capital tooling up because you'll likely be charged with infringement once the patent issues.

But if you discover that the invention is old and not

covered by an in-force patent, you're free to use it. In this case, you'll merely be practicing the "prior art," and the patent application's owner won't be able to obtain a valid patent on his invention.

One word of caution: Patent law isn't always black and white, so you should consult a patent attorney before you copy a product to make sure you haven't missed any important points.

Name search can determine patent's status

If the invention of interest simply carries the label "patented," you can't be sure whether it's covered by an in-force patent—one issued within the past 17 yrs—or by an expired patent that places the device in the public domain.

An invention in use for approximately 21 yrs (17 yrs for its patent term, plus about 4 yrs comprising the 1-yr grace period between first commercial use and a patent application and the patent-pending period) can almost certainly be manufactured with impunity. If you can't be sure, however, that the invention has been publicly available for 21 yrs, you can have a patentability or name search conducted in the Patent Office to determine the exact status.

A name search pulls all the patents issued in the name of the company manufacturing the product (or its inventor, if you know his identity). This procedure is not generally recommended, though: There could be simply too many patents issued in the company's name to make an identification practical, or the patent you're interested in might not be issued in the manufacturing company's name at all.

If there's no patent marking on the device or its housing or packaging (as is frequently the case), and it hasn't been publicly available for 21 yrs, you run a definite risk if you copy or manufacture it—it could be covered by an in-force or pending patent. In this case, then, follow the aforementioned procedures outlined for a patent-pending invention.

Trying to break a patent is not immoral

If an in-force patent covers the circuit or device you want to manufacture and it can't be designed around, only three courses of action remain: breaking the patent, a "damn the torpedoes" approach or obtaining a license.

You can try to break the patent by making an extended validity search and study of the Patent Office's file on it. This process, however, requires an experienced patent attorney and could cost several thousand dollars. And although it's been said that given enough money almost any patent can be broken, most patent attorneys would disagree. In fact, hundreds of patents are held valid every year after extended and extremely expensive court challenges. It wouldn't be a bad idea, though, to carefully study any patent you're interested in and make a regular patentability search before considering the alternatives previously noted; even a preliminary study can point out potentially fatal flaws.

As to the morality of seeking to break a patent, remember that a patent grants a valuable 17-yr monopoly. Thus, finding a good reason why the monopoly should not have been granted in the first place (the Patent Office makes mistakes like everyone else) constitutes a public service in helping to rescind an improperly granted monopoly.

Under the patent-law amendments recently adopted (EDN, June 24, pg 133), if you've found a good reason to challenge a patent, you can cite pertinent prior art to the Patent Office and have it placed in the patent's file or even request that the Patent Office re-examine the patent. The re-examination fee runs $1500 plus attorney fees, but this sum is still far cheaper than a full-blown court test.

As an alternative to trying to break the patent, you can go full speed ahead and "damn the torpedoes" by simply making and selling the patented invention and hope that the patent's owner won't catch you. If caught, you can then try to break the patent or negotiate a license. This approach isn't considered the most moral of positions, but it's followed frequently in industry. And it's adopted particularly with inventions not readily identifiable from an infringer's product, such as electronic circuits or semiconductor devices, especially if they can be incorporated in an IC.

If you do follow this approach, though, be sure to set aside a reserve fund equal to a reasonable patent royalty on the device you're going to use—a sum usually 1 to 10% of its factory price, depending upon the invention's value and importance to the final product. And be aware that if your infringement is discovered and you're sued, the patent owner can obtain an injunction prohibiting you from further manufacture or sale of the device. He can also collect damages equal to reasonable royalties for the past use of his product.

Asking for a license can be risky

The third method of copying a patented invention is the most moral of all: Ask the patent owner for a license to make and sell the device. But unless you know he's willing to license (eg, if he's already granted licenses to others), this approach can be risky because he can refuse to grant a license or can offer one only on very expensive terms. Thus, by inquiring about a license, you could tip your hand needlessly and lose most of the possible advantages if you decide to finally "damn the torpedoes."

A Question of Law

Most companies, however, are delighted to grant licenses on their patented inventions because they provide immediate extra income without risk or capital outlay. And the disadvantage of having you as an additional competitor is usually outweighed by the other considerable advantages of licensing; the company is probably already the market leader, and having a second source helps sales.

Finally, if the circuit or device you want to copy carries a patent number (eg, "Patent Nr 4,205,483"), your course is simplified. Simply order the patent by number for $0.50 from the Patent Office, Washington, DC 20231 or photocopy it in a Patent Depository Library—listed in the front of any current issue of the *Official Gazette*.

When you get the patent, note its date of issue; if it's more than 17 yrs old, the invention is now in the public domain. If not, you'll have to determine with the help of a patent attorney whether your circuit would infringe the patent's claims. (See the next article in this series for guidance.) If your circuit would infringe, you're left with one of the three alternatives just discussed.

Don't make your copy too literal

If you find, happily, that you can copy a device with impunity, remember not to make your copy too literal. One manufacturer sent a device to the Orient to be inexpensively copied—in quantity. It came back in huge quantities faithfully reproduced down to the last detail—including the competitor's embossed trademark, which of course had to be obliterated at great expense before the device could be legally sold. **EDN**

David Pressman, JD, BSEE, received the Juris Doctor degree from George Washington University and a BSEE from Penn State University. Formerly a field engineer at Philco-Ford Corp, a patent examiner with the US Patent Office and a patent attorney for Philco-Ford, Elco Corp and Varian Associates, Pressman is currently in private practice specializing in patent law.

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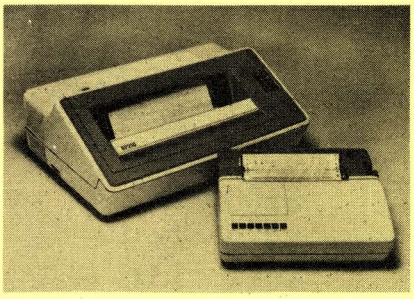

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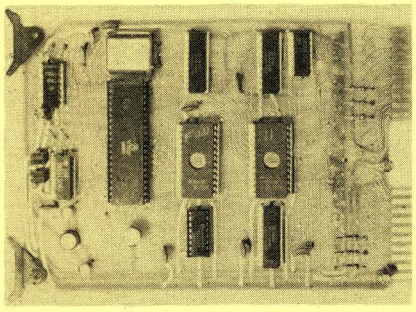

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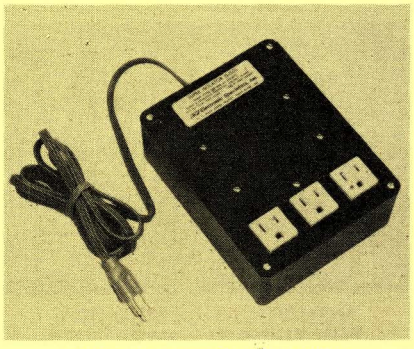

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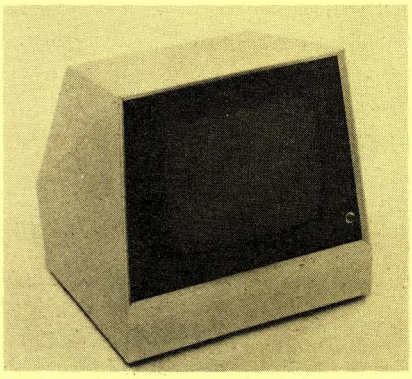

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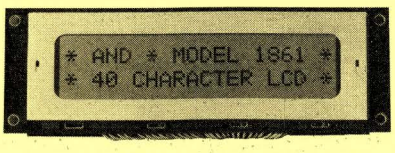

40 Character Alphanumeric LCD Module

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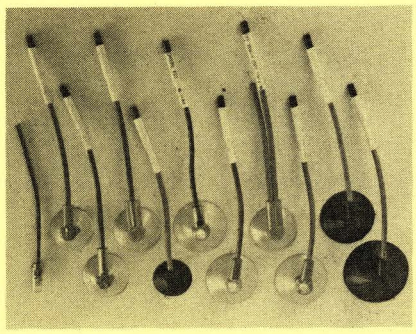

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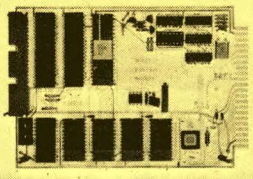

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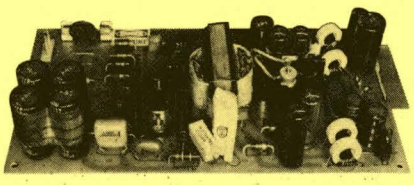

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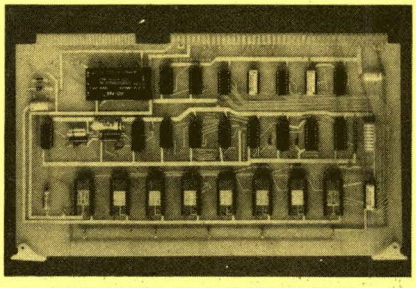

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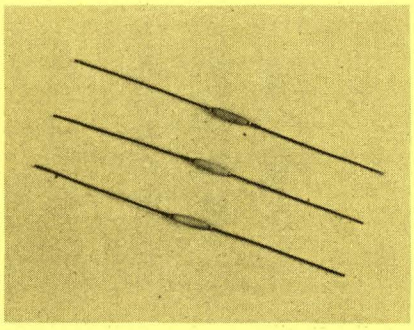

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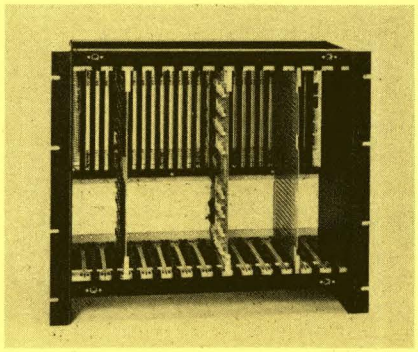

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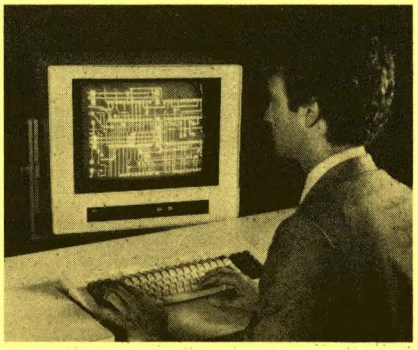

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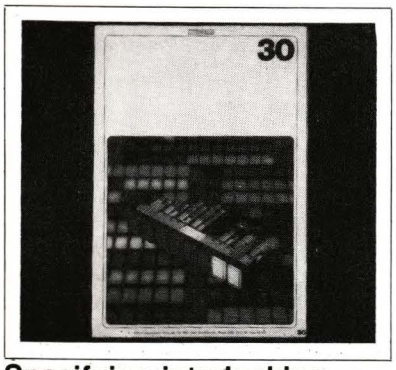
Literature



Specifying interlocking switch assemblies

This 6-pg brochure details Series 30 Interlock switch systems, actuators, switching elements, spacers and accessories. Its line drawings enhance technical data. A dimensional outline, mounting diagram and pad of order forms conclude the booklet. **EAO Switch Corp,** 255 Cherry St, Milford, CT 06460.

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Fold-out chart highlights resin uses

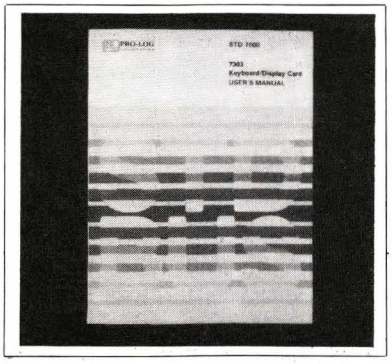
This epoxy-resin guide details products for encapsulation, impregnation, potting or casting applications. Providing specs for 26 1- and 2-part systems, it also contains a cure guide and temperature classification chart. **Acme Chemicals and Insulation Co,** Box 1404, New Haven, CT 06505. **Circle No 136**

Data details statistical MUXs

Bulletin 5264 describes features and applications of the DCX836, -840 and -850 statistical multiplexers. Photos and callout diagrams detail the operation of the MUXs' various diagnostic and networking modules, and block diagrams show how to incorporate them into different networks. A spec chart differentiates models by such features as number of input channels and composite links, buffer size and automatic-repeat-request capability. **Rixon Inc,** 2120 Industrial Parkway, Silver Spring, MD 20904. **Circle No 137**

Shopping for μC software

Listing more than 50 media formats, CP/M-compatible disk-operating systems, hard-disk integration modules, languages, language and application tools and word-processing systems, this 35-pg guide catalogs single-source tested and service-supported microcomputer software. Data-management and mail-list systems, financial accounting packages, numerical problem-solving tools and professional and office aids are also referenced. **Lifeboat Associates,** 1651 Third Ave, New York, NY 10028. **Circle No 138**



Utilizing a keyboard/display card

This 88-pg manual details the 7303 STD Bus keyboard card, a general-purpose control-panel unit providing data-input and display capability. Separate sections focus on the card's features, its operation and programming, installation and specifications, software and maintenance. An appendix describes the unit's front-paneling mounting. **Pro-Log Corp,** 2411 Garden Rd, Monterey, CA 93940.

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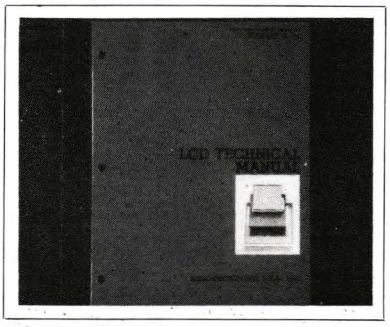

Designing with LCDs

Highlighting principles of operation, driving techniques, surface treatments, sealing, cost and reliability, a 20-pg handbook details liquid-crystal displays. In addition, it provides data on multiplexing drive techniques. Field-reliability information, 7-yr life data and graphs and illustrations explain the devices' operation. **Seiko Instruments USA Inc,** 2990 W Lomita Blvd, Torrance, CA 90505.

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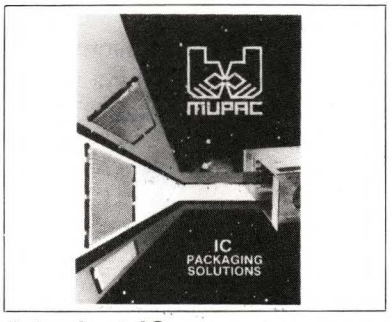

A look at IC packaging solutions

This literature kit includes a 152-pg catalog and 24-pg price list for microelectronic packaging systems and accessories. It features a μC-panel family, which serves prototyping and interface applications compatible with DEC hardware, including PDP-11 and LSI-11 systems. A spec table detailing rack assemblies, terminals, cable types and pc boards concludes the catalog. **Mupac Corp,** 10 Mupac Dr, Brockton, MA 02401.

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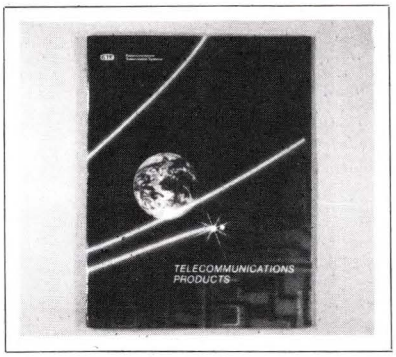
Literature



Data on more than 80 telecomm units

Featuring a line of video, voice and data-transmission systems, this 36-pg catalog details microwave radio transmitter/receivers and subsystems, fiber-optic transmission systems, multiplex systems, FDM cable-carrier systems, N-type repeatered line equipment, PCM digital multiplex equipment and cable-carrier systems. It also provides specs and illustrations of auxiliary data equipment, supervisory and control systems and voice-frequency and signaling equipment. Specs outlined include number of channels, frequency range and channel frequency response. **GTE Lenkurt Inc,** Dept C720, 1105 County Rd, San Carlos, CA 94070.

Circle No 142

Data illustrates power-line filters

This 16-pg catalog covers a line of RFI power-line filters, highlighting 3, 6 and 10A filters at 115/250V ac rated voltage, for common- and differential-mode operation in linear and switching power supplies. It also discusses FCC and VDE emission limits, noise modes, insertion loss, terminology and cost-effectiveness factors. A cross-referenced chart compares various manufacturers' units. **Curtis Industries Inc,** 800 W Tower Ave, Milwaukee, WI 53223.

Circle No 143

Books

On surviving in a technical hierarchy

Putt's Law and the successful technocrat, *by Archibald Putt; ix+165 pgs; $9.25; Exposition Press, Smithtown, NY, 1981.*

Addressing himself directly to technology-oriented industries, the author of this book provides insights into the nature of their hierarchies. Not content with Dr Peter's famous management principles, he applies the same type of observation to research and production facilities and finds some exciting differences between technological hierarchies and the rest of the world.

One of Putt's most innovative sections deals with the laws of failure. Failure isn't inherently a problem, he says. You must understand how to fail, however, if you expect to become a successful technocrat.

Using fictional case histories and a fictional model technocrat named Dr I M Sharp, Putt explores the mysteries of innovation management, the art of giving advice, decision making and how to communicate.

For those of you who are thinking of venturing out as consultants, Putt offers a stern warning. Most technical consultants fail, he says, because they think that their function is to give information and advice. You'll have to read his book to see the naivete of this notion.

— Ed Teja

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Circle No. 5003 (on page 240 of **EDN**)

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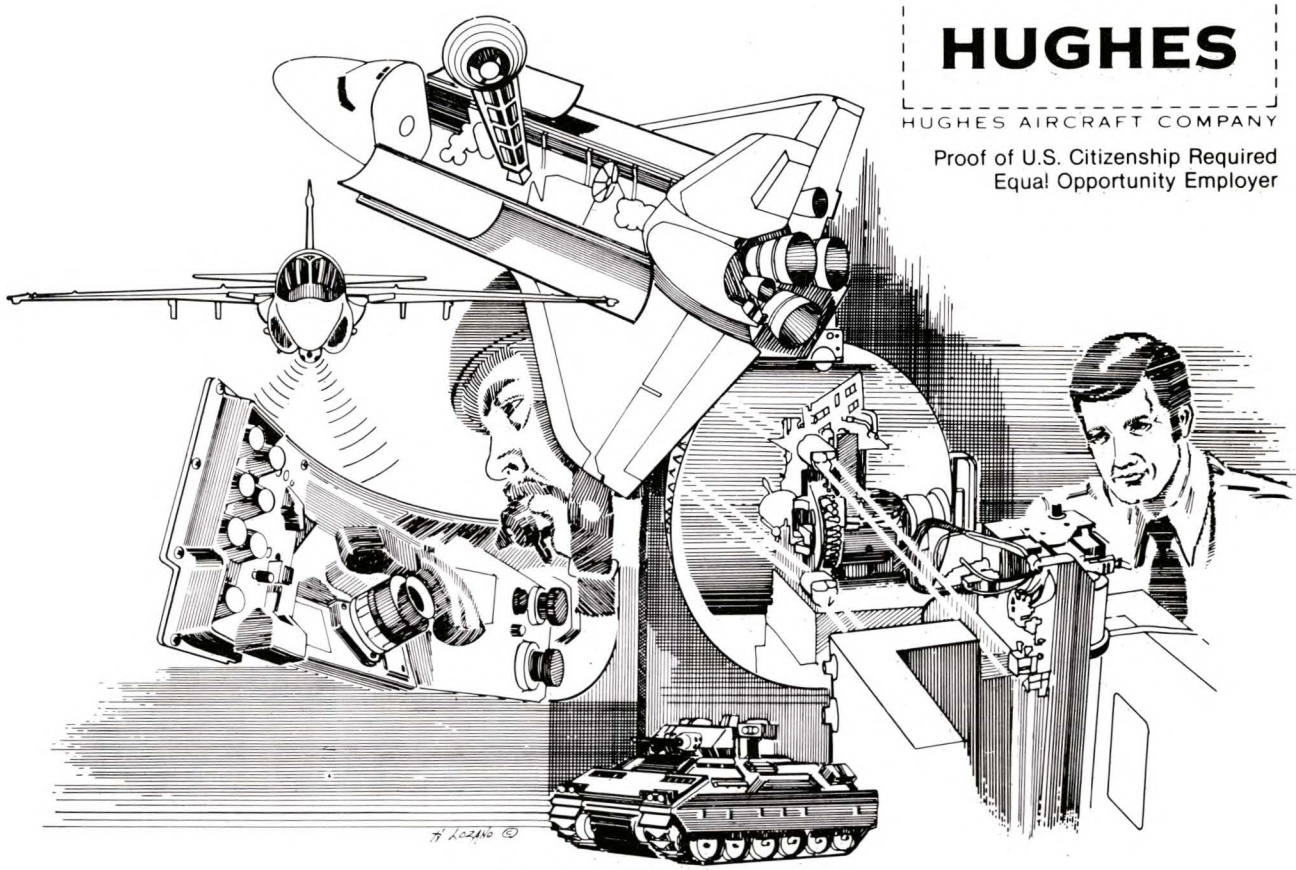

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Circle No. 5005 (on page 240 of **EDN**)

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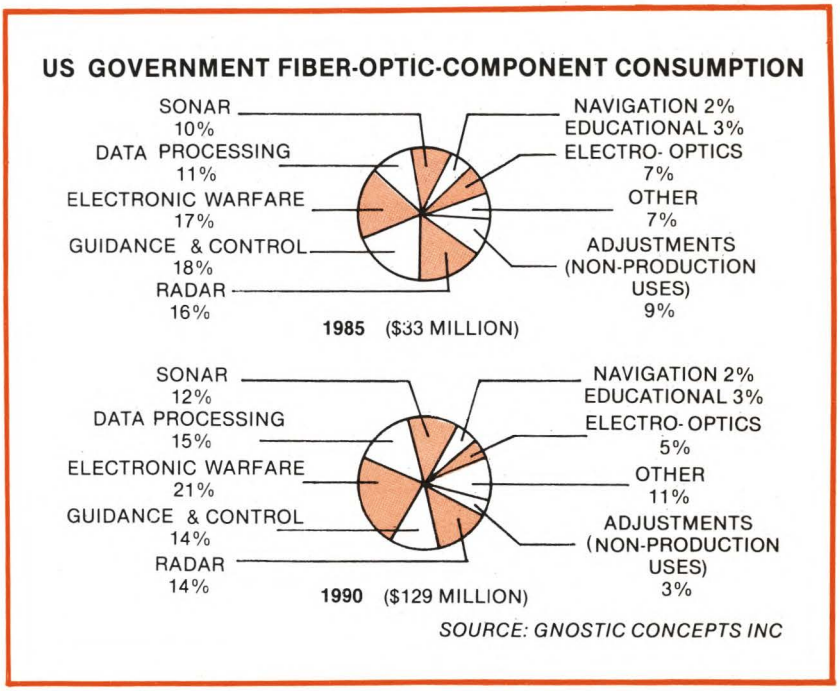
Advertisers Index

Looking Ahead: Trends and Forecasts

'80s' F-O gov't sales to top $1.9 billion

The 1980s will see total US production of fiber-optic components for government/military applications skyrocket to more than $1.9 billion, fueled by rapidly rising sales of point-to-point analog and digital communications equipment. Government data-bus fiber-optic applications—including radar, data-processing, guidance/control, sonar and electronic-warfare systems—will account for a $23 million market by 1985, predicts Gnostic Concepts Inc (Menlo Park, CA). And production in these five equipment categories should reach $99 million in 1990.



Standardization of components used for government applications will be completed by 1983 in time for broad-scale fiber-optics usage, says Bill Walsh, Gnostic Concepts military analyst. As fiber-optic architecture grows more complex, optical-frequency and multiplexing techniques will be employed, and wavelength dividers will utilize planar and concave diffraction gratings and wavelength-sensitive fibers, integrated on substrates with other components.

Walsh also expects data-bus architectures to emerge by 1985 and foresees increased usage of 1.3- to 1.6-μm devices in the latter half of the decade to capitalize on the lower attenuation and dispersion possible at those wavelengths. Development of long-wavelength sources and detectors using quaternary III-V compounds should additionally permit repeater spacings of tens of kilometres—and possibly 100 km—by the end of the decade.

Production by the mid-1980s of fibers and components using fluoride-based glasses will result in low-loss optical transmission lines utilizing the longer wavelengths, Walsh predicts.

Mass-produced electric cars by 2000?

Long promised but never delivered, practical electric vehicles (EVs) (EDN, September 5, 1980, pg 105) could finally start rolling down American roads in significant mass-production quantities soon after the turn of the century, says Harry W Mathews Jr, consulting engineer at Arthur D Little Inc (Cambridge, MA).

Limited mass production of this country's first generation of modern electric cars is scheduled for 1986, with 2-seater General Motors passenger EVs expected to be ready for the 1986-7 model year. GM electric vans are due on the market in 1983.

The greatest obstacle to widespread electric-car use is the battery: Today's models last only 30,000 mi (500 recharges) and cost $1500 to $2500 to replace.

However, by the early 1990s, Mathews predicts, power-source improvements should result in a power plant lasting the life of the car and providing a 150-mi range between charging cycles.

Early EVs will cost $3000 to $6000 more than their gasoline-powered counterparts, although this price differential should be halved once 250,000-unit-per-yr production levels are reached.

Material for this page developed from *Electronic Business* magazine and other sources by Jesse Victor, Assistant/New Products Editor, and Joan Morrow, Assistant Editor.

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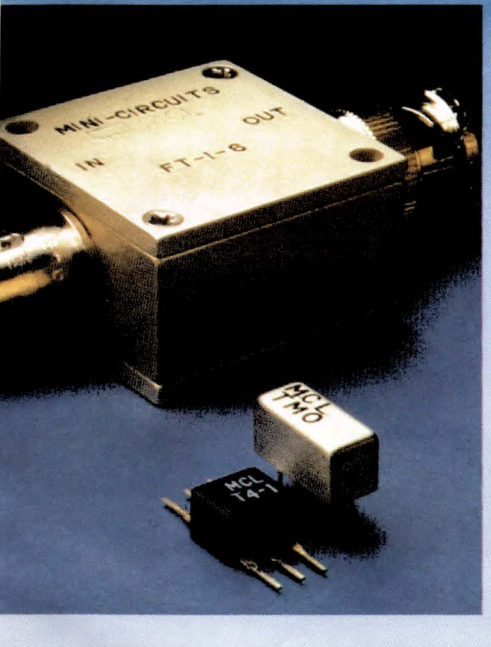

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Imped. Ratio	1	1	1.5	2.5	4	9	9	16	16
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TMO model (10-49)	$4.95		$6.75	$6.45	$6.45	$6.45		$6.45	

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Imped. Ratio	1	2	2.5	3	4	4	5	13
Freq. (MHz)	.05-200	.07-200	.01-100	.05-250	.2-350	8-350	.3-300	.3-120
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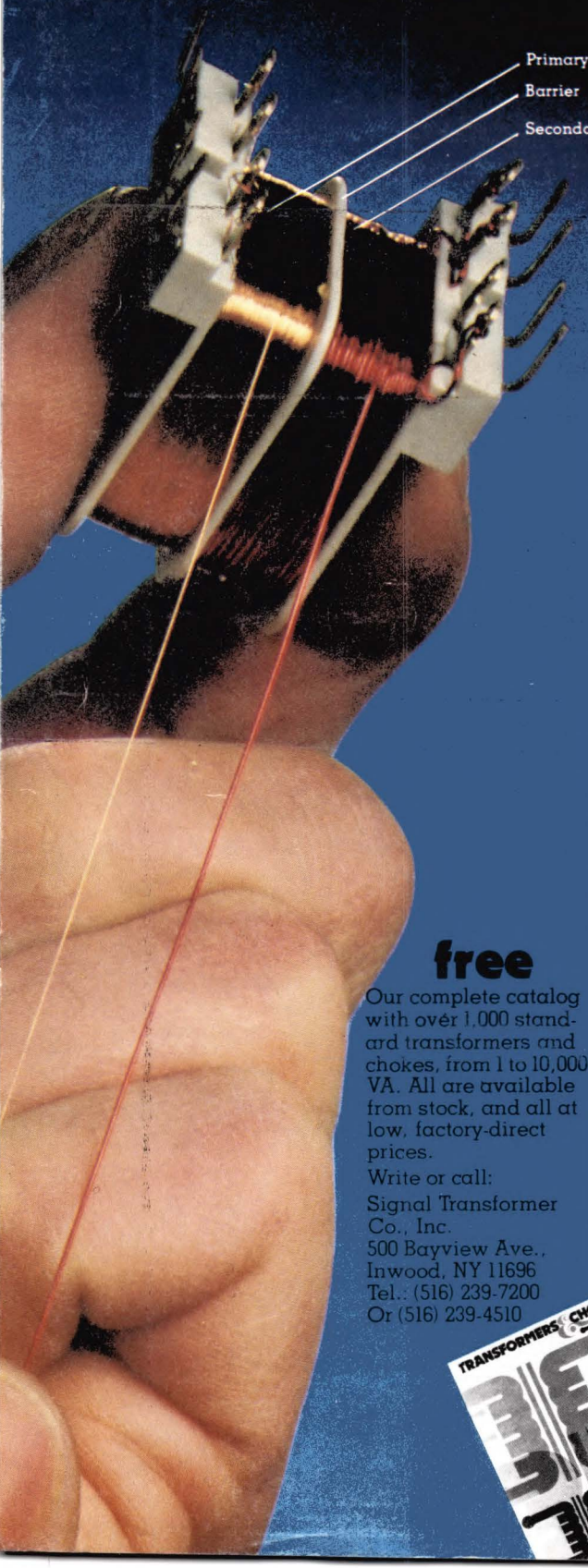

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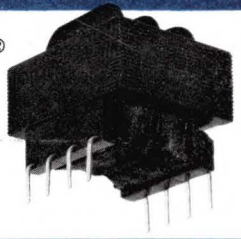

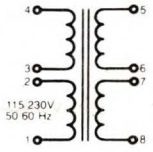

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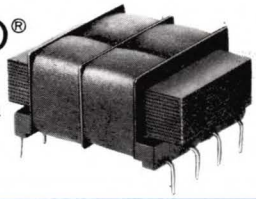

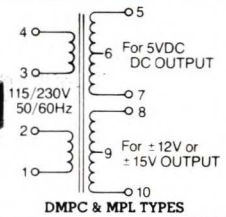

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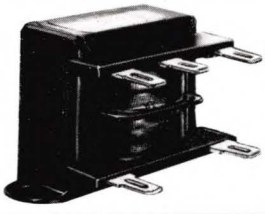

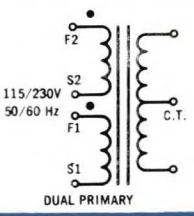

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